AN ADAPTIVE APPROACH FOR DISTANCE PROTECTION OF POWER TRANSMISSION LINES

A DISSERTATION

Submitted in partial fulfillment of the
requirements for the award of the degree
of
MASTER OF TECHNOLOGY
in
ELECTRICAL ENGINEERING
(With Specialization in System Engineering and Operations Research)

By

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CANDIDATE'S DECLARATION

I hereby declare that the work that is being presented in this dissertation report entitled as "**An *Adaptive Approach for Distance Protection of Power Transmission Lines***" submitted in partial fulfilment of the requirements for the award of **Master of Technology** in **Electrical Engineering** with specialisation in **System Engineering and Operations Research**, to the department of **Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee, India** is an authentic work carried by me under the supervision of **Dr. H.O.GUPTA** Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee.

Date: 29th June 2011
Place: Roorkee

Manish Kumar
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CERTIFICATE

This is to certify that above statement made by the candidate is true to the best of my knowledge.

29/6/11

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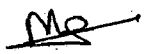

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ABSTRACT

The author in this report presents the development of adaptive distance relay and its real-time simulation. The Relay includes adaption against fault in series capacitor compensated line that identifies the location of fault with respect to the installed series capacitor and takes appropriate action to make the relay to look the fault in the correct zone. It takes care of circuit breaker failure by providing the backup protection by issuing trip signal to the upstream circuit breaker in the case of main breaker failure condition. And it describes its adaptiveness in close in fault conditions where polarising voltage to the relay collapses to a very small quantity. These adaptive features have been developed along with the normal distance protection. The distance relay model has been built using MATLAB environment.

A Real-Time hardware setup has been described which has been prepared in the Power System Laboratory at IITR for testing the Relay at different conditions as stated above. The control of the power circuit has been done using the control circuit developed by the author. The series capacitor has been installed in the line which checks the adaptiveness of the relay in case of fault including the series capacitor in the fault loop.

Also a power system model has been created in the Matlab/Simulink for verifying the results of the real time simulation and testing the relay against the cases which is not possible to simulate with the real time setup.

CONTENTS

Glossary of Acronyms

A/D	Analog to Digital
ADC	Analog to Digital Converter
C	Capacitance
CB	Circuit Breaker
CT	Current Transformer
DAQ	Data Acquisition Card
DFT	Discrete Fourier Transform
FFT	Fast Fourier Transform
I	Current
I/O	Input Output
IEEE	Institute of Electronic and Electrical Engineers
L	Inductance
MOV	Metal Oxide Varistors
NI	National Instruments
PT	Potential Transformer
R	Resistance
V	Voltage
X_c	Capacitive Resistance
X_l	Inductive Resistance
Z	Impedance

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CHAPTER 1

INTRODUCTION

1.1 Importance of Protection System:

Modern electrical power systems catering to huge energy demands are spread over extensive areas and contain several major components like generators, transformers, transmission and distribution lines. In spite of all the precautions taken in the design and installation of such systems, there are bound to arise abnormal conditions or faults. It may prove extremely damaging to the faulty component and the neighboring components and also to the power system as a whole. It is of vital importance to limit the damage to a minimum by speedy isolation of the faulty section without disturbing the working of the rest of the system.

The importance of the services that power system offers and the high amount of investment, make the normal and constant operation of power system critical and strategic for every society. Power system needs an auxiliary system that must take corrective actions on the occurrence of a fault. This auxiliary system is known as protection system.

Protection systems are sets of equipments, schemes and policies combined in different manners to achieve certain kind of dedicated protection.

1.2 Introduction of Protective Relays:

One of the most important equipment employed in the protection of power systems are protective relays. Relay is defined by the IEEE as "an electric device that is designed to interpret input conditions in a prescribed manner, and after specified conditions are met, to respond to cause contact operation or similar abrupt changes in associated electric control circuits", and protective relays as "a relay whose function is to detect defective lines or apparatus or other power conditions of an abnormal or dangerous nature and to initiate appropriate control circuit action".

Protection has been provided since the beginning of the electrical industries, and has encountered great transformations with time as power system has grown in size and complexity. If we go historically, protective relays design was started with electromagnets. Those relays were bulky and heavy devices but because of their robustness they have been used for several decades. And still continued to be used in older substations.

Next to it was solid state relays which replaced electromechanical components by analog electronic elements.

The advent of microprocessors both in the mainframe structure and the compact personal computer form has led to its utility in replacing the traditional analytical tools used in electrical power engineering. Digital relaying is a very promising area of thought with the advent of digital computing technology.

1.3 Introduction to Distance Relays:

Distance relays, as the name sounds, should measure distance. In fact this is true, as in case of transmission line, distance relay measures the impedance between the relay point and the fault location. This impedance is proportional to the length of the conductor, and hence to the distance between the relaying point and the fault.

Principle of operation: The basic principle as illustrated in figure 1.1, involves the division of the voltage at the relaying point by the measured current. The apparent impedance is compared with the reach point impedance. If the measured impedance is less than the reach point impedance, it is assumed that a fault exists on the line between the relay and the reach point. The reach point of the relay is the point along the line impedance locus that is intersected by the boundary characteristics of the relay. Distance relay is the broader name of the different types of impedance relay [3].

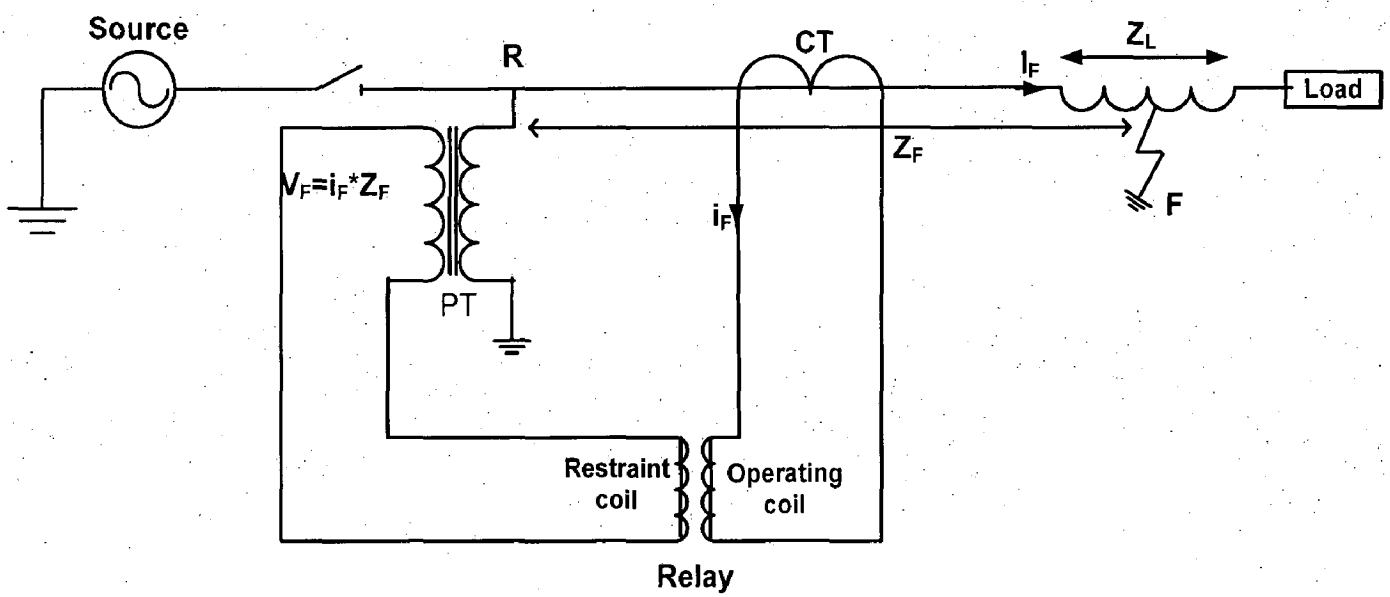


Figure 1.1 Principle of operation of distance relay

The relay is connected at position, R and receives a secondary current i_F, equivalent to a primary fault current, I_F. The secondary voltage V_F, is equivalent to the product of the fault current I_F and impedance of the line up to the point of fault Z_F. The operating torque of this relay is proportional to the fault current I_F, and its restraining torque is proportional to the voltage V_F. Taking into account the number of turns of each coil, there will be a definite ratio of V/I at which the torque will be equal. This is the reach point setting of the relay. The relay will operate when the operating torque is greater than the restraining torque. Thus any increase in current coil ampere-turns, without a corresponding increase in the voltage coil ampere-turns, will make the operating torque more than the restraining torque of the relay. This means the V/I ratio has fallen below the reach point. Alternatively if the restrain torque is greater than the operating torque, the relay will restrain and its contacts will remain open. In this case the V/I ratio is above the reach point. The reach of a relay is the distance from the relaying point to the point of fault. Voltage on the primary of voltage transformer, VT, is:

$$V = \frac{EZ_F}{(Z_S + Z_F)}$$

The fault current, I_F

$$I_F = \frac{E}{(Z_S + Z_F)}$$

The relay compare the secondary values of V and I, as to measure their ratio which is an impedance Z_m ,

$$Z_m = \frac{\frac{V}{P.T.\,ratio}}{\frac{I}{C.T\,ratio}}$$

$$Z_m = Z_F * \frac{C.T.ratio}{P.T.ratio}$$

Z_m is the measured impedance called secondary impedance [3].

Zones of protection: Basic distance protection will comprise instantaneous directional Zone 1 protection and one or more time delayed zones. Numerical distance relays may have up to five zones, some set to measure in the reverse direction. Numerical relays usually have a reach setting of up to 85% of the protected line impedance for instantaneous Zone 1 protection. The resulting 15% safety margin ensures that there is no risk of the Zone 1 protection over-reaching the protected line due to errors in the current and voltage transformers, inaccuracies in line impedance data provided for setting purposes and errors of relay setting and measurement. of the distance protection must cover the remaining 15% of the line. The reach setting of the Zone 2 protection should be at least 120% of the protected line impedance. In many applications it is common practice to set the Zone 2 reach to be equal to the protected line section +50% of the shortest adjacent line. Zone 3 reach should be set to at least 1.2 times the impedance presented to the relay for a fault at the remote end of the second line section. Typical reach for a 3-zone distance protection are shown in Figure1.2.

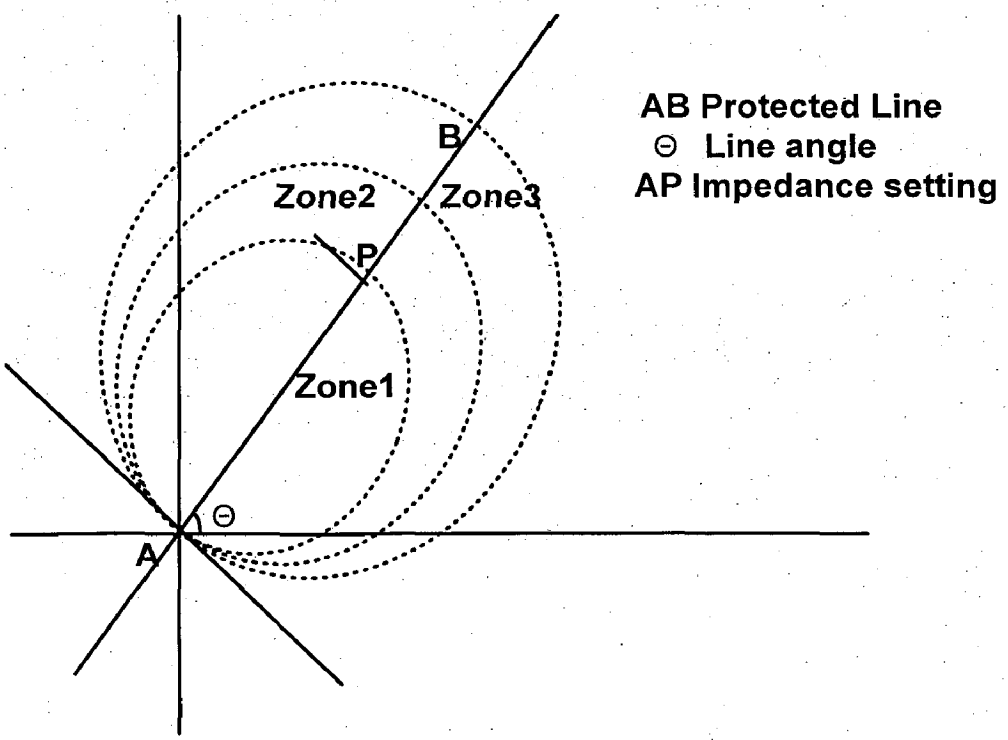


Figure 1.2. Typical 3 zones distance protection

1.4 Concept of Adaptive Relaying:

"Adaptive Protection is a protection philosophy which permits and seeks to make adjustments to various protection functions in order to make them more attuned to prevailing power system conditions" [6].

1.5 Architecture of Numerical Relays:

Computer relays consist of subsystems with well defined functions. Although a specific relay may be different in some of its details. The block diagram in Figure 1.3 shows the principal subsystems of a computer relay. The processor is central to its organization. It is responsible for the Execution of relay programs, maintenance of various timing functions, and communicating with its peripheral equipment [2].

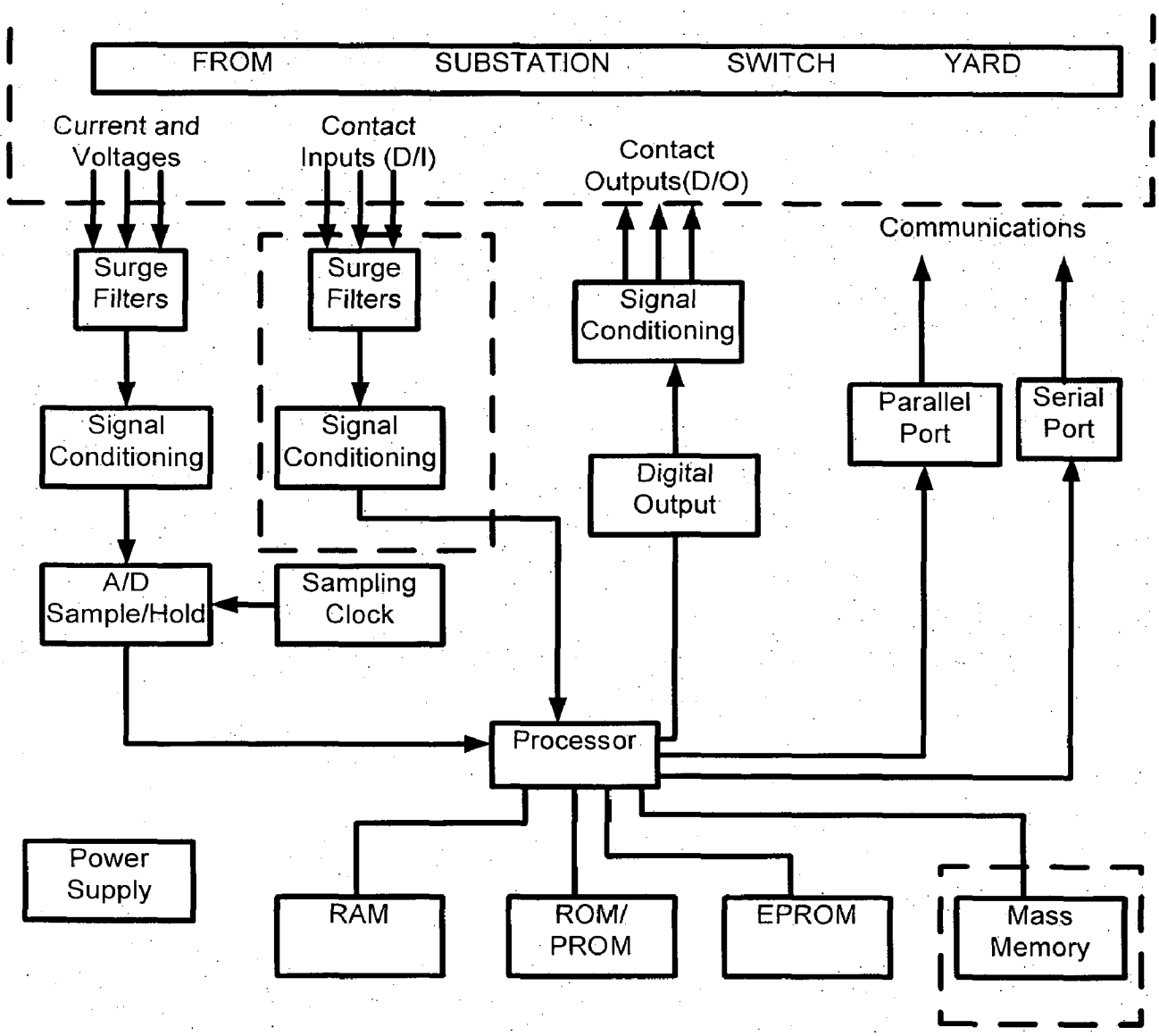


Figure 1.3 Architecture of Numerical Relay [2]

The Random Access Memory (RAM) holds the input sample data as they are brought in and processed. It may also be used to buffer data for later storage in a more permanent medium. In addition, RAM is needed as a scratch pad to be used during relay algorithm execution. The Read Only Memory (ROM) or Programmable Read Only Memory (PROM) is used to store the programs permanently. In some cases the programs may execute directly from the ROM, if its read time is short enough. If this is not the case, the programs must be copied from the ROM into the RAM during an initialization stage, and then the real-time execution would take place from the RAM. The Erasable PROM (EPROM) is needed for storing certain parameters (such as the relay settings) which may be changed from time to time, but once set must remain fixed, even if the power supply to the computer is interrupted. Either a core type memory or an on-board battery backed RAM may be suitable for this function.

The Analog to Digital Converter (ADC) converts an analog voltage level to its digital representation. The principal feature of an ADC is its word length expressed in bits. Ultimately this affects the ability of the ADC to represent the analog signal with a sufficiently detailed digital representation. For example each bit of the 12bit ADC word represents 10/2048volts, or 4.883millivolts (Considering that the analog input signal may range between ±10 volts). The equivalent input change for one digit change in the output (4.883milli volts in case of a12bit A/D converter) is an important parameter of the ADC. It describes the uncertainty in the input signal for a given digital output. Thus an output of hexadecimal 001 represents any input voltage between 2.442 and 7.325 mill volts. This is the quantization error of the ADC. In general, if the word length of the ADC is N bits, and the maximum input voltage for the ADC is V volts, the quantization error q is given by

$$q = \frac{\mathrm{V}}{2-2^{N-1}} = 2^{-N}\,\mathrm{V}$$

And normalized to the largest possible input voltage of V, the per unit quantization error is

$$\text{Per unit } q = 2^{-N}$$

Clearly, the larger the number of bits in a converter word, the smaller is the quantization error. There are various types of ADC available which are:

1 Successive approximation ADC

2 Delta-sigma ADC

3 A direct conversion ADC or flash ADC

4 Ramp-compare ADC

Since the relay in general requires several inputs, several conversions are performed at each sampling instant. There are various approaches to achieve it which has been figured in Fig 1.4.

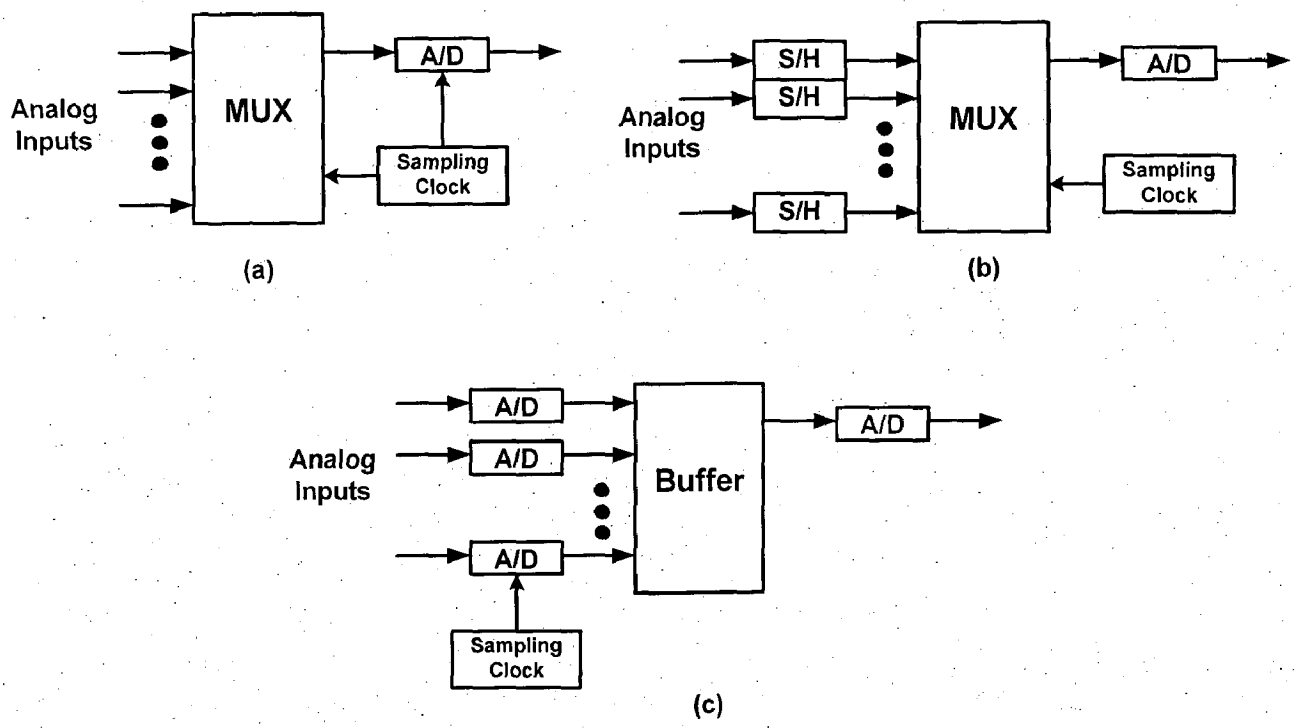


Figure 1.4 Multiple Signal Sampling Process And Its Organization. (a) Single ADC with Multiplexed Input. (b)Sample And Hold Added To Each Channel. (c) Separate ADC for Each Channel

Returning once again to Figure 1.3, digital output from the processor is used to provide relay output in the form of open or close contacts. A parallel output port of the processor provides one word (typically two bytes) for these outputs. Each bit can be used as a source for one contact. The computer output bit is a Transistor to Transistor Logic (TTL) level signal, and would be optically isolated before driving a high speed multi-contact relay, or thyristors, which

in turn can be used to activate external devices such as alarms, breaker trip coils, carrier control etc.

Finally, the power supply is usually a single DC input multiple DC output converter powered by the station battery. The input is generally 125 volts DC, and the output could be 5 volts DC and ±15 volts DC. Typically the 5 volt supply is needed to power the logic circuits, while the 15 volt supply is needed for the analog circuits. The station battery is continuously charged from the station AC service.

1.6 Motivation

With advents of technology the requirement of power is increasing day by day. To meet these requirements one needs to generate more power but along with production we need to take care of its transmission and distribution. With the increasing population it's hard to get the right of way for erecting the new power transmission lines, so the science gives an alternate way for it and that was the installation of series capacitor in the existing line which can increase the power transmission capability. But this is not so promoted because of its demerit of posing threat to the well functioning of the distance relay which is common in long transmission line. This led to the author to work on the subject so that power requirement can be met in the future.

1.7 Literature Review:

Bhuvanesh Oza, Nirmal Kumar, Rashes Mehata, Vijay Makwana, **"Power system protection and switchgear,"** [1] gives the basic concepts of relaying and the real time problems in power system. It offers a blend of application practices and theoretical concepts to comprehend the subject of power system protection. It gives the concept of control circuits in substation for controlling the relay operation. Real field data and system conditions are provided for relay setting calculations.

Arun G. Phadke and James S. Thorp, **"Computer relaying for power systems,"** [2] present the concept of using digital computers and mathematical basis for relaying. It gives the understanding of how an algorithm works i.e. its procedural structure.

In the year of 2009, **"Advances in series compensated line protection,"** by H.J.Altuve, J.B.Mooney, G.E. Alexander, [4] reviews the series-compensated line protection challenges that include voltage inversion, current inversion, and distance estimation errors. They suggested

modern solutions to improve directional, distance, and differential element operation on series-compensated lines.

In the year of 2001, **"First zone algorithm for protection of series compensated line,"** by Murari M. Shah, Bogdan Kasztenny, [5] presented an algorithm which on-line estimates the instantaneous value of voltage drop across the series capacitor and compensates it while calculating the impedance for taking the decision.

In the year of 1999, **"Distance protection aspects of Transmission lines equipped with series compensation capacitors,"** by Clint T. Summers [6] presented a method to distinguish a fault before and after the series capacitor which was on the sub harmonic contents in the fault current.

In the year of 1987, **"Adaptive transmission system relaying,"** by S. H. Horowitz, A. G., Phadke, and J. S. Thorp [7] presented the possibilities of using digital techniques to adapt transmission system protection and control to real-time power system changes.

In the year of 1995, **"Removal of dc offset in current waveforms using digital mimic filtering,"** by G. Benmouyal [8] compared digital filters used in relaying applications to suppress DC offset in current waveforms over a broad range of time constants, and explained concept of the FIR type of digital mimic filter.

In the year of 1995, **"Removal of Decaying DC Offset in Current Signals for Power System Phasor Estimation,"** by Amir A. A. Eisa, K. Ramar [9] presented a method to remove the DC component from the fault current which is based on the averaging of the current signal over a cycle. It takes full cycle plus one sample of post fault data to calculate the DC component.

In the year of 2008, **"Enhanced Numerical Breaker Failure Protection,"** by Bogdan Kasztenny, Vijayasarathi Muthukrishnan, and Tarlochan Singh [10] presents the narrow stability limit that is available to backup breaker to isolate the fault in the case of main circuit breaker fail

condition. It presents a novel algorithm for numerical current-based BF function with a fast 0.5-cycle reset time even under severe subsidence current.

In the year of 2008, **"Distance relaying algorithm using a DFT-based modified phasor estimation method,"** by Dong-Gyu Lee, Ye-Jim Oh, Sang-Hee Kang, Han, and B.M. [11] presents a modified phasor estimation method to eliminate the adverse influence of decaying DC offsets. It calculates the error due to DC offsets in a DFT and eliminates it using the outputs of an even sample set DFT and odd sample set DFT.

In the year of 1970, **"Digital calculation of impedance for transmission line protection,"** by B. J. Mann and I.F.Morrison [12] proposes a method of distance type protection suitable for on line digital protection of transmission lines and describe the results of experimental work on a model transmission line and on a high voltage transmission system.

In the year 1982, **"A Prototype of Multi Processor Based Distance Relay,"** P. Bornard and J.C.Bastide [13] presented the design and realization of a digital relay for EHV system and also described the algorithm. This paper explained how a prototype has been built with four 16-bit microprocessors, to allow the simulations real time computation of three apparent impedances. The hardware and software architecture are also described.

In the year 2009, **"Modeling of Numerical Distance Relays Using Matlab,"** A.A Abdlrahem and H.H.Sherwali, [14] described distance relay modeling using Matlab environment and the distance relay model verified by the Electromagnet Transient Program. This paper demonstrates the benefits achieved when using a computer simulation of a relay in conjunction with a transient power system simulation.

1.8 Author's Contribution

In long transmission line series capacitor installation are common now a day. But along with increasing the power carrying capability of the line, it makes the distance relay to mal-operate by looking the second or third zone fault in the first zone. Author has developed an algorithm based on DC component to detect the presence of the series capacitor in the fault loop. And then took the appropriate action to avoid the mal-operation due to the stated problem.

The complete protection does not include only sensing the fault and issuing the trip signal but also it should ensure that the faulty section has been removed. But it may be hindered due to fault in the circuit breaker or the cable carrying the trip signal to the circuit breaker trip coil. In the presented report author has given backup to this type of condition with user settable backup time.

During the close in fault the polarizing voltage of the relay collapses to a very small value such that it cannot be taken for further processing i.e. impedance calculation. In this case too distance relay fails to operate. Author has included a scheme of voltage memory action with resettable memory time which takes care of the presented problem.

1.9 Dissertation Outline:

The dissertation report has been organized in six chapters. The outline has been presented here.

Chapter 2 discusses the architecture of The Adaptive Distance Relay. It presents the Algorithm used for achieving the Adaptiveness and discusses the theory used behind them.

Chapter 3 discusses the Laboratory setup for the Real Time Simulation of the presented Relay. It presents the details of Power and control circuit of the setup and discusses working of the same. It provides the information and method for acquiring data to and from the computer.

Chapter 4 details the zone setting of the relay and explains how to create the different situations for checking the adaptiveness of the Relay.

In **Chapter 5** test results of the Real-Time and Matlab/Simulink simulation of the Relay for different cases has been given. Impedance trajectories followed at different conditions are shown in this chapter.

Chapter 6 discusses the results presented in chapter 5, draws conclusion of the dissertation, and gives the future scope of the work.

CHAPTER 2

ARCHITECTURE OF THE ADAPTIVE DISTANCE RELAY

2.1 Introduction

This chapter details the architecture of the adaptive distance relay and the functionality of each of the internal modules of numerical relay such as, sample and hold module, phasor estimation module, data processing module etc. Fig. 2.1 represents the block diagram of the relay. The highlighted blocks are the special features of the relay.

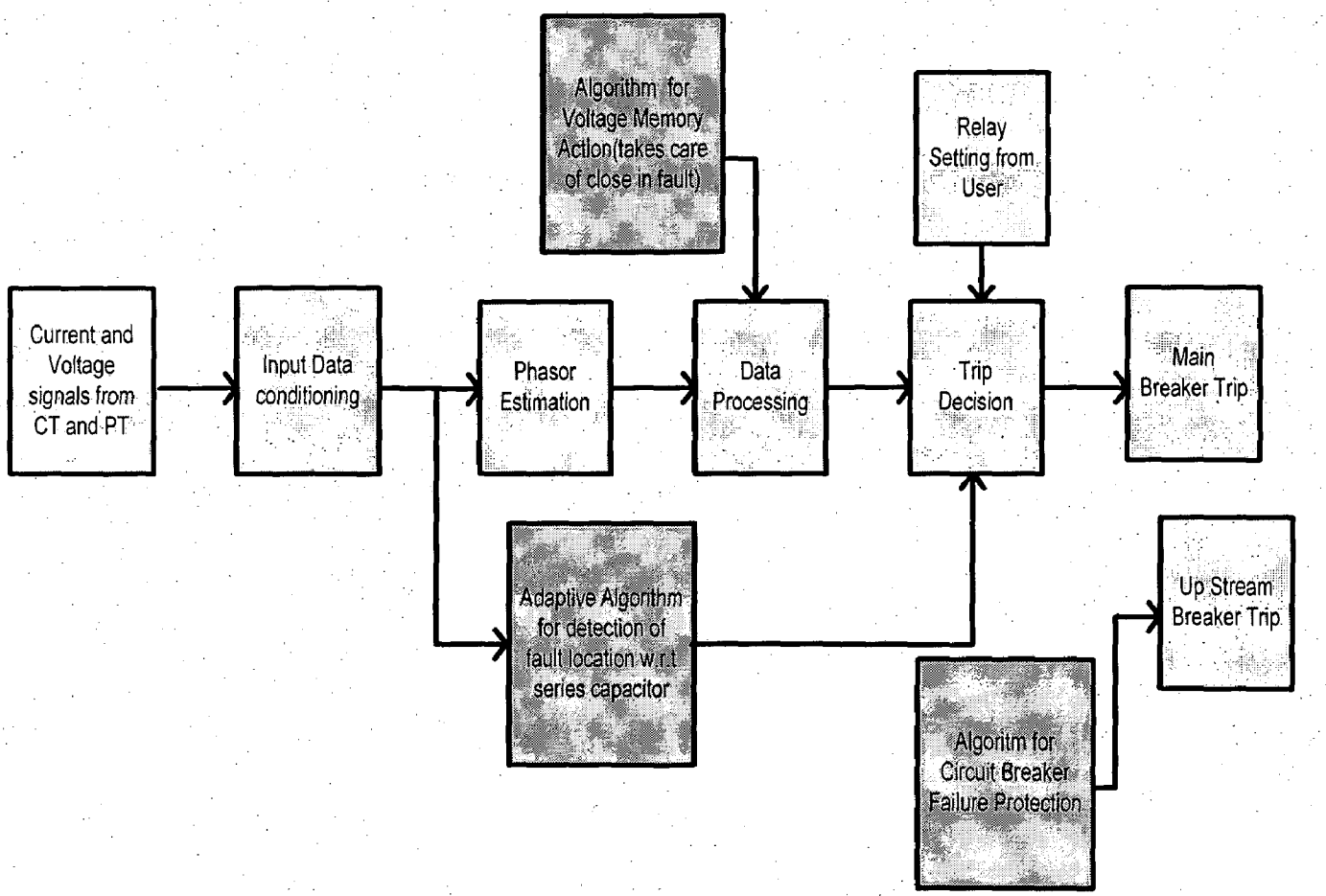


Figure 2.1 Block diagram of the adaptive Distance Relay

2.2 Input Data Conditioning

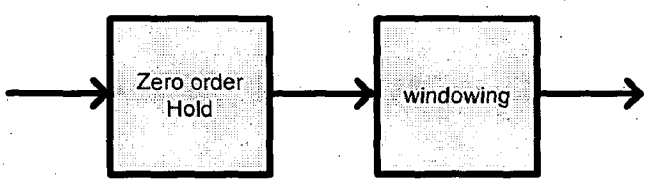


Figure 2.2 Block diagram of the input data conditioning

In a digital signal the relative phasor information between two samples is not preserved so to overcome this, two consecutive samples have to be interpolated and for interpolation hold circuit has been used.

A buffer is a region of memory used to temporarily hold data while it is being moved from one place to another. The data is stored in a buffer as it is retrieved from the input device or just before it is sent to the next processing level. A buffer often adjusts timing by implementing a queue (or FIFO) algorithm in memory, simultaneously writing data into the queue at one rate and reading it at another rate.

The computed phasor has the correct magnitude but will be rotating by angle θ at each sample instant [2].

Let

V (t) = The instantaneous value of an AC Voltage waveform

V^k = Voltage at k_{th} sample

ω_0= The fundamental power system frequency in radians per second

θ = The fundamental frequency angle between samples, i.e. $\theta = \omega_0 \Delta t$

Let the voltage V (t) is in the form of

$$V(t) = V_C \cos \omega_0 t + V_s \sin \omega_0 t$$

Where V_C and V_s are real numbers

In polar form they can be written as

$$V^k = \sqrt{(V_c^k)^2 + (V_s^k)^2}$$

$$\varphi^k = \tan^{-1}\frac{V_s^k}{V_c^k} = \tan^{-1}\frac{V_s}{V_c} - k\theta$$

Lets the data window has the word length of three samples, that is, as a new sample becomes available, the oldest of the three sample values is discarded and the new sample value is included in the calculation.

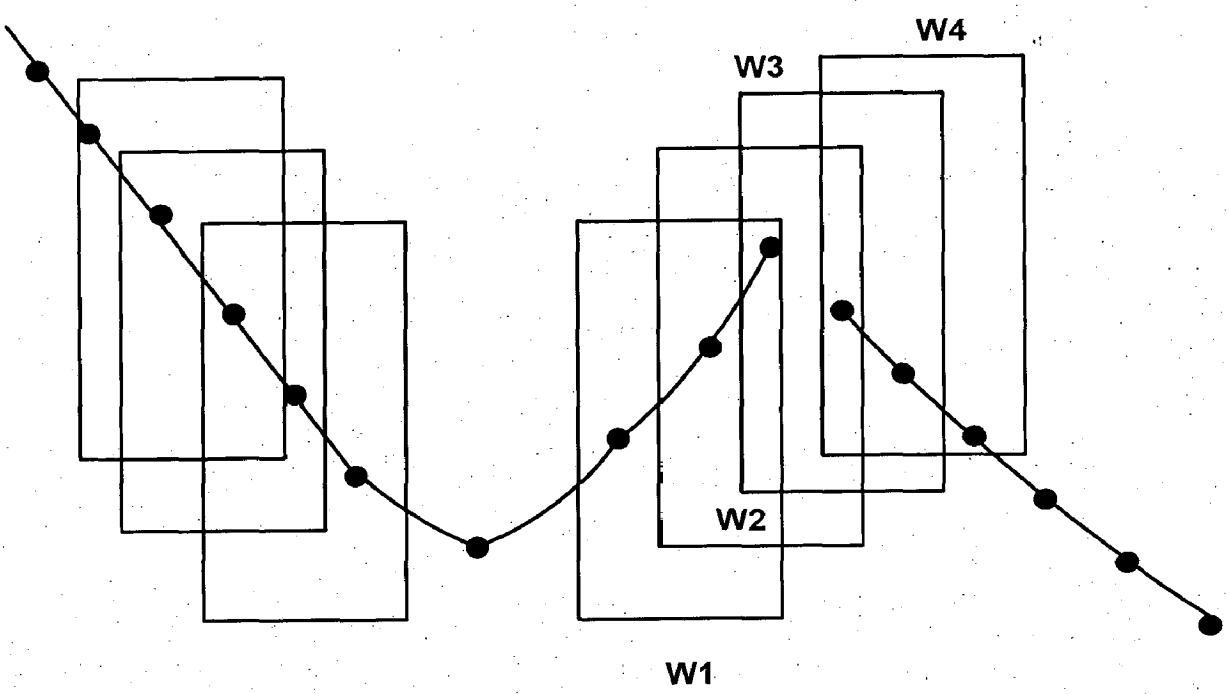


Figure 2.3 Moving three sample data window on a voltage waveform [2].

The window labelled W1 (Fig.2.3) contains three samples of pre-fault data, the windows W2 and W3 contain both pre- and post-fault data, and the window W4 has only post-fault data. The calculations will produce the correct phasor in the windows containing pure pre-fault or post-fault samples. The data in the windows W2 and W3, however, cannot be fitted to a pure sinusoid and the computed phasor is of little meaning.

The length of the data window is one of the important factors to be properly decided. Recognizing that the results obtained when the window contains both pre-fault and post-fault samples are unreliable, it seems reasonable to wait until the results are reliable (when the window contains only post-fault data) before making relaying decisions. Since a longer window takes longer to pass over the fault instant, it is clear that faster decisions can be made by short window algorithms. Unfortunately, the ability of an algorithm to reject non-fundamental

frequency signals is a function of the length of the data window. In other words, there is an inherent inverse relationship between relaying speed and accuracy.

In the presented relay design the length of the data window is taken as 10

2.3 PHASOR ESTIMATION

When a power system is operating under steady state conditions, both the voltage and the current signals are periodic and the fundamental frequency component of each is at the power frequency. But during the fault condition the current and voltage signals are heavily distorted and may contain different harmonics, therefore it is necessary to calculate the impedance corresponding to a given voltage and current by determining the fundamental components of voltage and current using a discrete Fourier transform (DFT) technique.

Mathematical Background [3]

Signal at any given time may be described by a phasor. Phasor actually is a vector rotating in the complex plane with a speed ω radian/sec, a snap-shot in time, the signal at that time, is given in rectangular form by

$$x(t)(t = T) = (real\ coordinate) + j(imaginary\ coordinate) \quad (1)$$

$$x(t) = a + jb \quad (2)$$

And in polar form by

$$x(t) = Ae^{j\omega t} \quad (3)$$

Or in general it is

$$x(t) = Ae^{j(\omega t+\alpha)} \quad (4)$$

The above discussion is related to a simple cosine or sine function ($\cos \omega t = \frac{1}{2}(e^{j\omega t} + e^{-j\omega t})$ and $\sin \omega t = \frac{1}{2j}(e^{j\omega t} - e^{-j\omega t})$) of a single frequency, most signals are composed of many cosine and sine waves. Therefore any complex periodic signal can be described as sum of many phasors. Fourier series assumes that a set of phasors have frequencies which are multiples of some fundamental frequency, f_0, i.e.

$$X(t) = \sum_{k=-N}^{N} A_k e^{j(k\omega_0 t)} \quad (5)$$

The individual frequency components are known as harmonics. If the complex signal is not periodic the phasor frequencies are not related, thus the Fourier general form may be written as;

$$X(t) = \sum_{k=-N}^{N} A_k e^{j(k\omega_k t)} \quad (6)$$

In digital domain (discrete time), replace the continuous function, t, with a function progresses in jumps of ωt thus phasor description of single frequency signal would be;

$$x(n) = Ae^{j(n\omega T_s+\alpha)} \quad (7)$$

$$e^{j(n\omega T_s)} = \cos(n\omega T_s) + j\sin(n\omega T_s) \quad (8)$$

Where, T_s is the sampling interval

A real signal can be described using Fourier in discrete domain called (Discrete Fourier Series) as,

$$X(n) = \sum_{k=-N}^{N} A_k e^{j(n\omega_0 T_s n)} \quad (9)$$

which is a simple phasor model that describes a general discrete signal. The discrete Fourier transform (DFT) is a digital filtering algorithm that computes the magnitude and phase at discrete frequencies of a discrete time sequence. Fast Fourier transforms are computationally efficient algorithms for computing DFTs. FFTs are useful if we need to know the magnitude and/or phase of a number individual or band of frequencies. The DFT is ideal method of detecting the fundamental frequency component in a fault signal.

2.4 DATA PROCESSING

The phasors computed in the previous section has been utilized for calculating the resistance and reactance of the line instantaneously. Figure 2.4 shows the block diagram of data processing process.

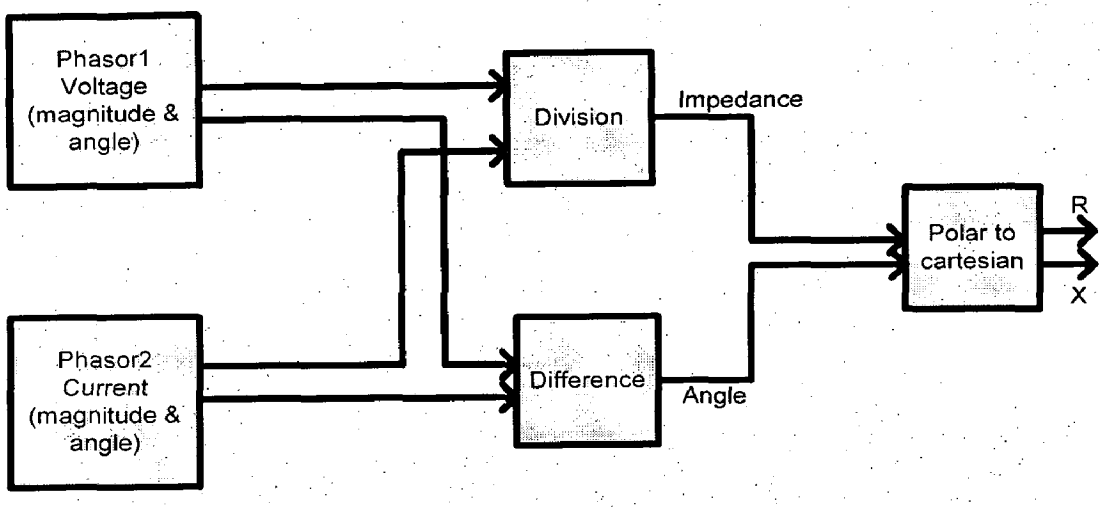


Figure 2.4 Block diagram for Data processing

2.5 ADAPTIVE ALGORITHM FOR DETECTION OF PRESENCE OF SERIES CAPACITOR W.R.T THE FAULT

Effect of Series Capacitor on Impedance Measurement:

Protective distance relays, which make use of impedance measurement in order to determine the presence and location of faults, are fooled by installed series capacitor. Even though its presence is known in advance it cannot be taken into account for distance relay settings. This is because of the protection provided across the capacitor, which keeps on changing its conduction level as per the fault condition. And fault reactance seen by relay varies accordingly therefore the relay may perceive a fault to be in its first zone when the fault is actually in the second zone of protection (as shown in Fig.2.5). Similarly, first zone faults can be perceived to be reverse faults [4].

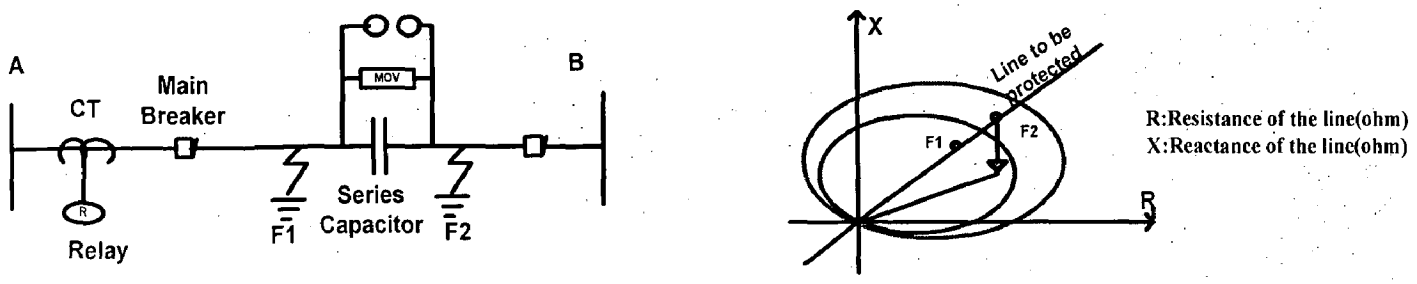


Figure 2.5 Second zone fault perceived to be in first zone because of presence of series capacitor [1]

For the fault at F1 the relay will get the impedance as

$$Z_{L1} = R_1 + jX_{L1}$$

This is in zone1 of protection. But for the fault at F2 it will be

$$Z_{L2} = R_2 + j\,(X_{L2} - X_c).$$

So it will be perceived in zone1 even though the fault is in zone2.

These all happenings are function of protection provided to the series capacitor i.e. MOV and spark gap across the capacitor. For high current faults, the MOV starts conducting or spark gap flashes and removes the capacitor from service. In this case relay measures the correct line impedance. But For low-current faults, the spark gap or MOV does not conduct completely and the capacitor partially remains in service. And hence the capacitive reactance modifies the impedance estimate. One can think to set the distance characteristic as per the calculations done by including X_c, but even though one knows the compensation level he doesn't know what percentage of current will flow through the capacitor. Again it is because of the protection provided across the capacitor whose conduction depends on the V-I characteristic of the MOV [6].

So in the presented scheme the current signal from the data window has been process separately to extract the DC component. There are various methods of calculating the DC component. Benmouyal [8] has proposed a digital mimic filtering technique to attenuate the decaying dc component. This filter, however, achieves its best performance once the time constant of the decaying dc component is equal to the time constant of the mimic filter. Another shortcoming of the mimic filter is that it acts as a high-pass filter that amplifies high frequency noise. So here it has been achieved by averaging the current signal over a cycle because the fact

that sinusoidal signals and exponential signals have different mathematical properties. Namely, a purely sinusoidal signal has a zero average over a full cycle or multiples of the full cycle of its fundamental frequency, whereas an exponential signal has a nonzero average over that same interval [9].

Let the signal of interest be represented by:

$$y(t) = Ae^{-t/\tau} + \sum_{n=1}^{M}(A_n \cos(n\omega t + \varphi_n) \qquad (10)$$

where

A	magnitude of the decaying dc offset;
τ	time constant of the decaying dc offset;
A_n	amplitude of the nth harmonic;
φ_n	phase angle of the nth harmonic;
F	frequency in Hz;
ω	$2*\pi*F$ rad/s.

The signal contains an exponential component along with AC signal if we take the average value of both sides of (10) over a complete cycle (T) of the fundamental frequency we get:

$$\frac{1}{T}\int_0^T y(t)dt = \frac{1}{T}\int_0^T e^{-t/\tau}\,dt + \frac{1}{T}\int_0^T \sum_{n=1}^{M}(A_n \cos(n\omega t + \varphi_n)\,dt \quad (11)$$

The average value of the sinusoidal part of the signal over a complete cycle of the fundamental frequency is zero. Therefore, (11) becomes:

$$\frac{1}{T}\int_0^T y(t)dt = -\tau\frac{A}{T}(e^{-t/\tau} - 1) \qquad (12)$$

If the signal $y(t)$ is sampled by taking N samples per cycle then these samples can be used to numerically compute the integral on the left-hand-side of (12). After computing the value of the integral we have two unknowns on the right-hand-side of (12), the initial value A and the time constant τ of the exponential component. In order to evaluate these two unknowns a second equation is required. If the sampling interval is given by

$$\Delta t = T / N \qquad (13)$$

then we can obtain a second equation by taking the average value of both sides of (11) over the interval $[\Delta t, \Delta t + T]$. This results in:

$$\frac{1}{T}\int_{\Delta t}^{\Delta t+T} y(t)dt = \quad -\tau\frac{A}{T}\left(e^{-t/\tau}-1\right)e^{-\Delta t/\tau} \qquad (14)$$

To solve (12) and (14) for the unknowns A and τ, let:

$$Avg_0 = \frac{1}{T}\int_0^T y(t)dt,$$

$$Avg_1 = \frac{1}{T}\int_{\Delta t}^{\Delta t+T} y(t)dt,$$

and

$$E = e^{-\Delta t/\tau}.$$

Equations (12) and (14) become:

$$Avg_0 = -\tau\frac{A}{T}\left(E^N-1\right), \qquad (15)$$

$$Avg_1 = -\tau\frac{A}{T}\left(E^N-1\right)\mathrm{E}, \qquad (16)$$

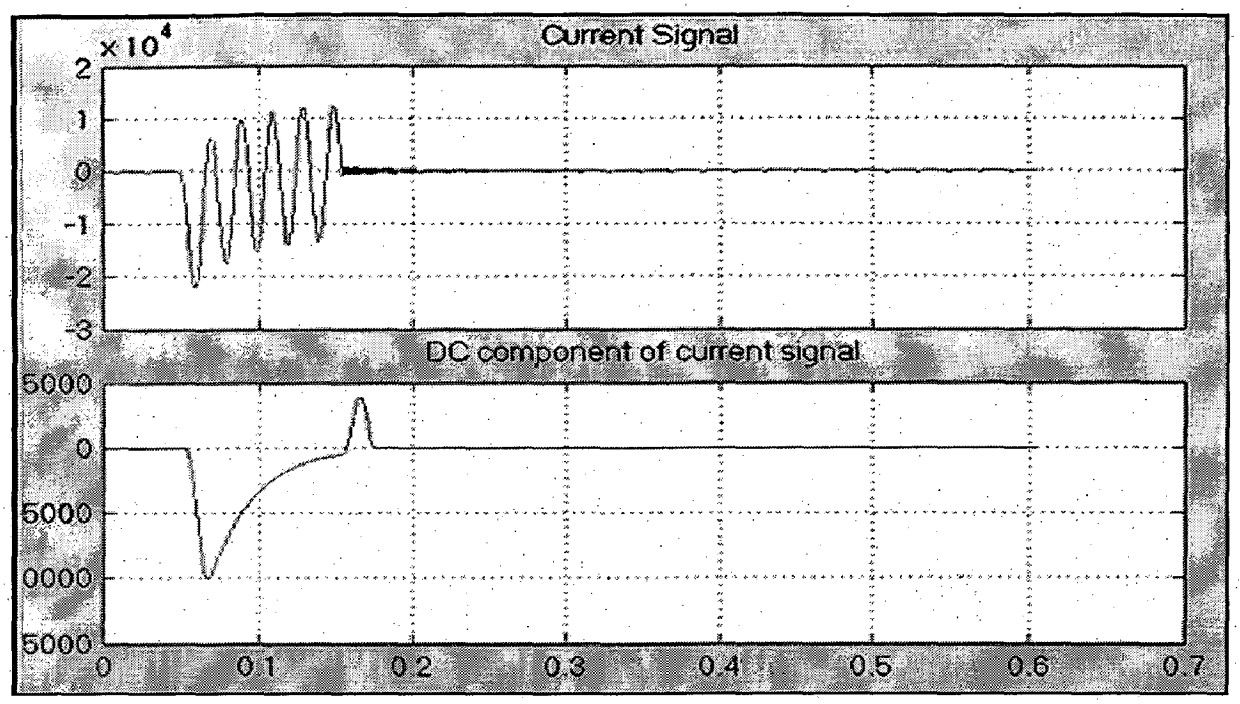
From (15) and (16) we can easily conclude that:

$$E = \frac{Avg_0}{Avg_1} \qquad (17)$$

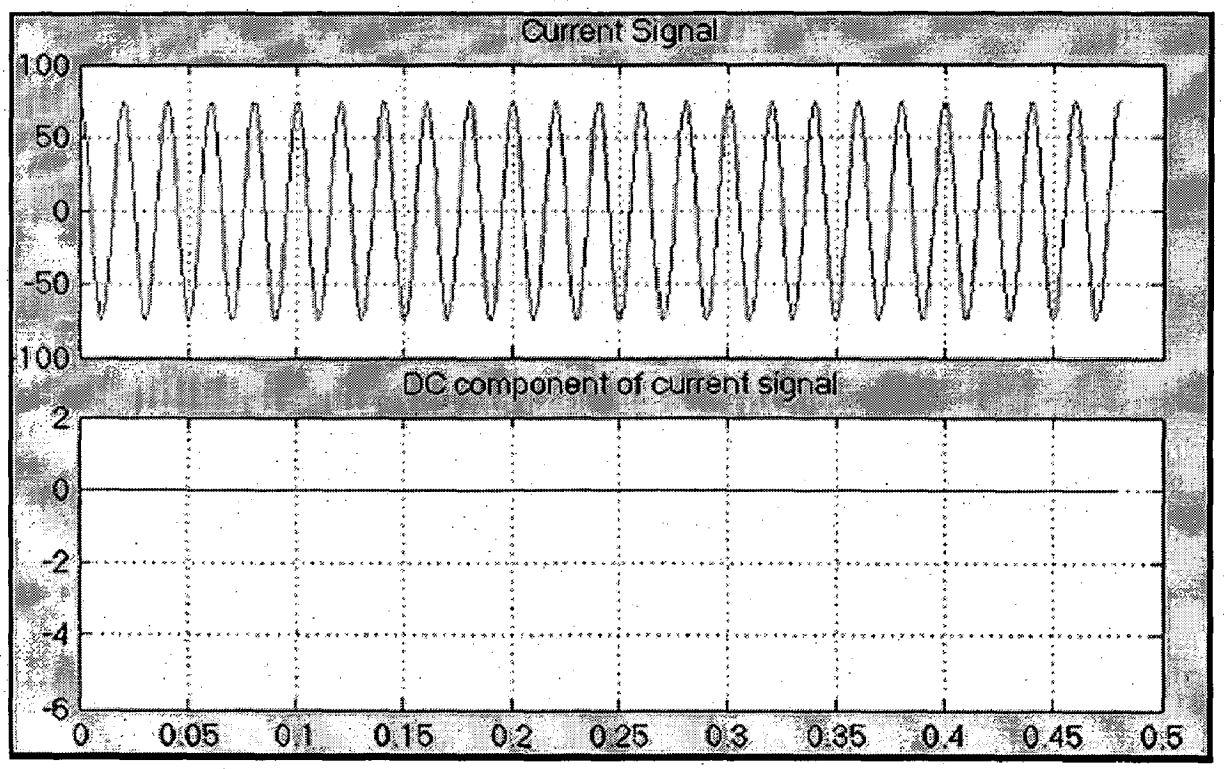
$$A = \frac{N\,Avg_0\ln(E)}{(E^N-1)} \qquad (18)$$

$$\mathbf{y_{DC\ component}=AE^k} \qquad (19)$$

Full cycle plus on sample of post fault data are required to apply the proposed method. Fig. 2.6(a) and (b) shows the current signal and its DC component of the faulty and healthy case respectively.



(a)



(b)

Figure 2.6 DC component extraction of sinusoidal signal in case of (a) fault (b) normal

DC component for the fault before and after the capacitor has been shown in figure 2.7 and 2.8 respectively. As can be seen from the graph that for the fault before the capacitor the DC component is of decaying nature and the two consecutive zero crossing after the fault inception takes a very long time (of the order of 200ms), whereas for the fault after the capacitor the DC wave form is of oscillatory nature and the two consecutive zero crossing after the fault inception takes a less time (less than 35ms). This time depends on various parameters such as the fault inception angle, MOV conduction level, reactance to resistance ratio etc. this feature has been utilized for deciding the location of fault w.r.t the installed series capacitor.

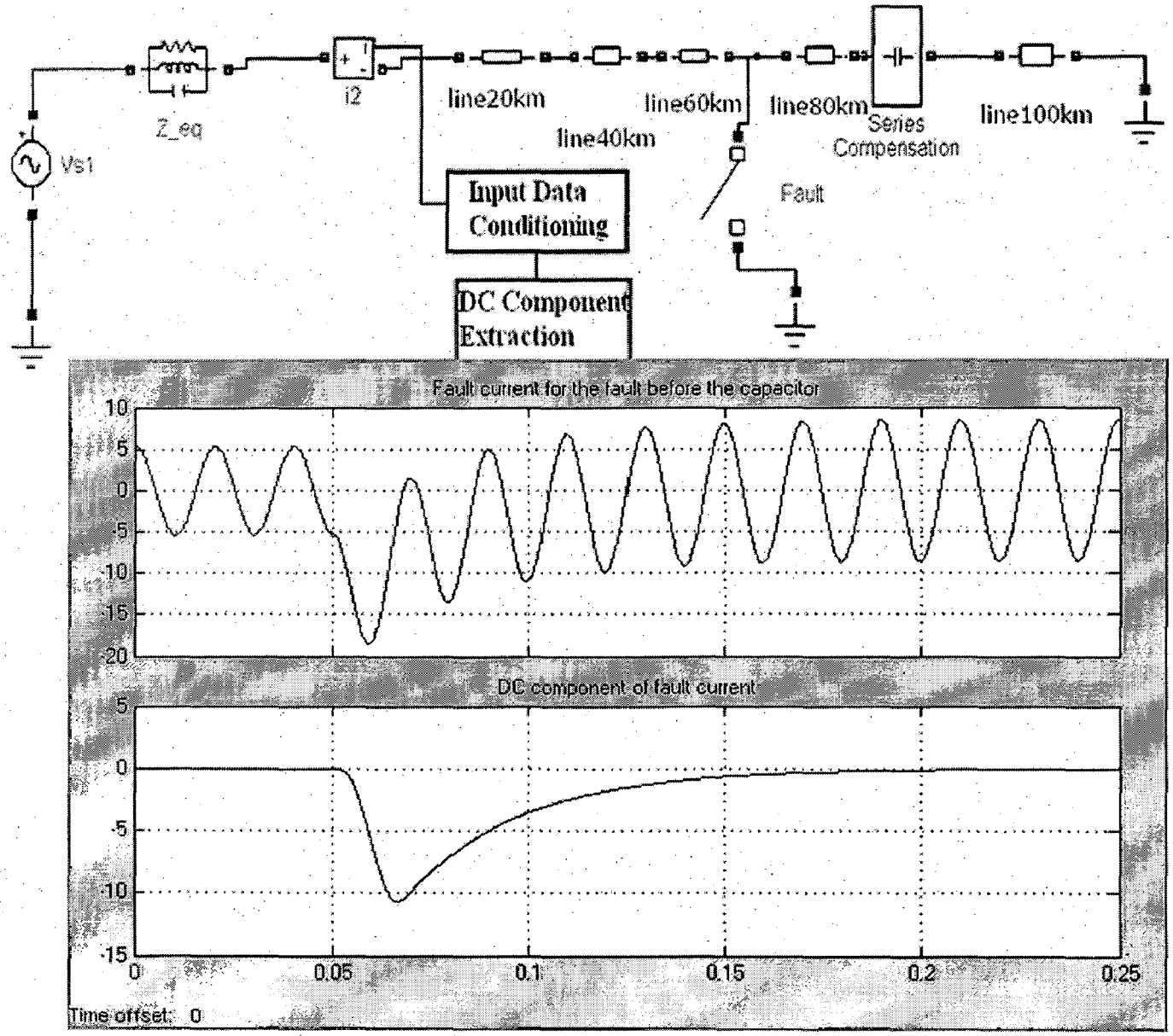


Figure 2.7 DC component of the fault before the capacitor

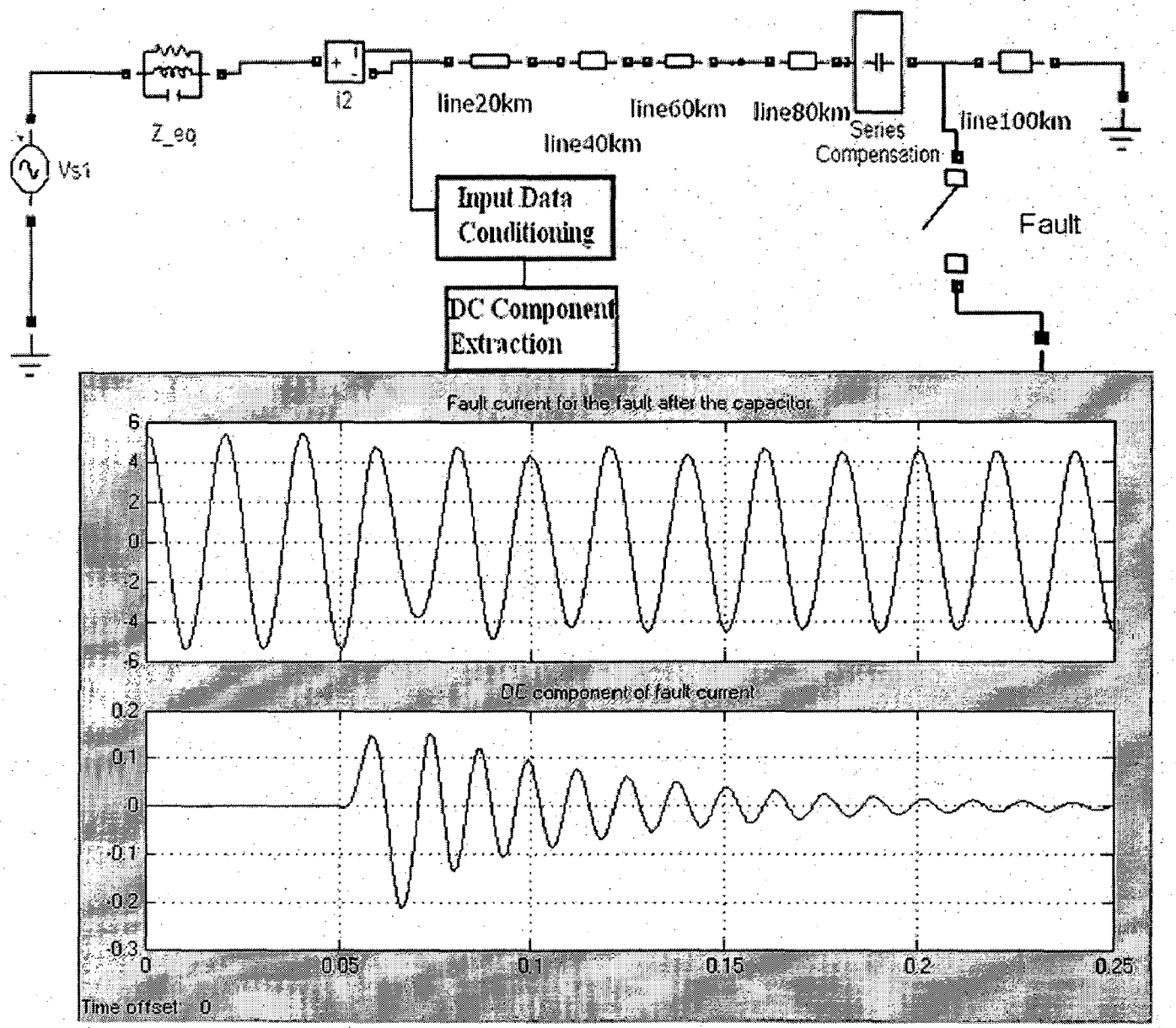


Figure 2.8 DC component of the fault after the capacitor

Author suggests installing the series capacitor in the second zone (anywhere before the starting of second line section).It will make the algorithm less complex because fault after the series capacitor is surely will be in the second zone. Figure 2.9 shows the block diagram for the above stated procedure. The decision from figure 2.9 can be utilized for either blocking the trip in zone 1 or for compressing the zone 1 so that the fault after the capacitor can reappear in zone 2.

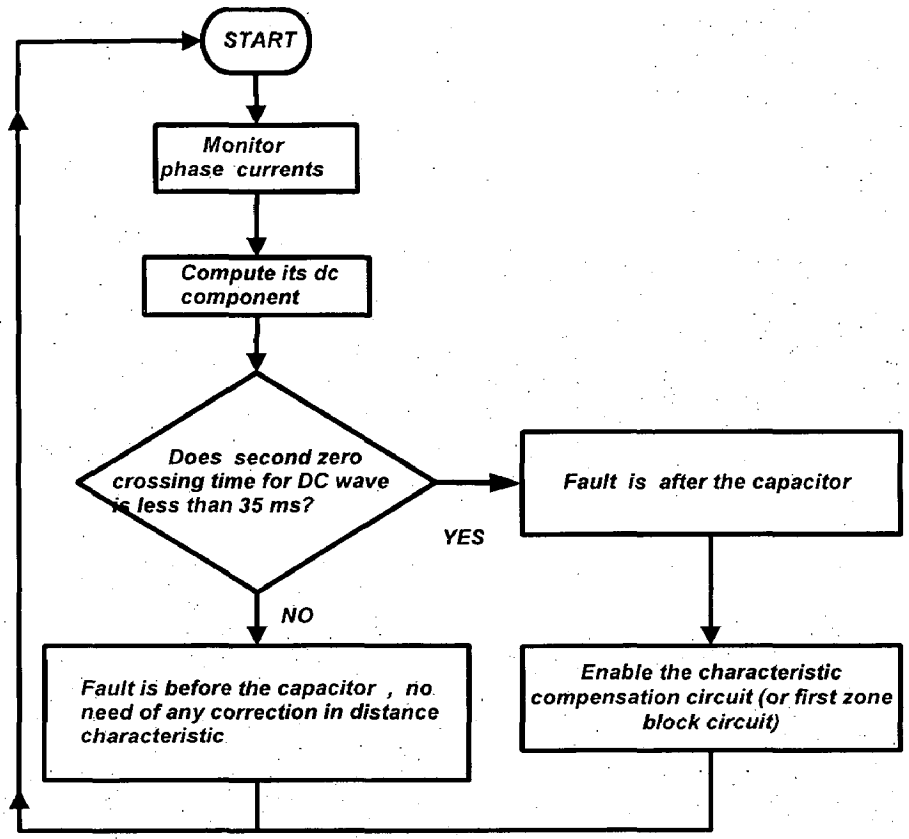


Figure 2.9 Algorithm for adaptive relay against series capacitor

2.6 TRIP DECISION

The computed resistance and reactance is compared with the set zone values (zone values are set in terms of resistance and reactance of the line section to be protected). And if the computed parameters are within the set zone values it issues a trip signal (theoretically it should be instantaneously). Here in the relay design this has been called as conventional trip signal. There is one more trip signal called as adaptive trip signal will be issued as a result of algorithm presented in fig.2.9. These two conditions will be combined to form four output logics, which will take care of the stated problem.

Table 2.1 Conventional and Adaptive Trip signal combination

Case	Conventional Trip Signal (C)	Adaptive Trip Signal (A)	(C) & (A) = Output Logic
1	0	0	0
2	0	1	0 , Not Possible
3	1	0	0
4	1	1	1

Table 2.1 gives the combination of conventional and adaptive trip logic. In case 1 (Referring to table 2.1) both signals are zero which means there is no fault. Case 2 is not possible because if there is no fault there will be no oscillating DC, as can be seen from figure 2.6 (b). Case 3 states a case in which there is a fault after the capacitor i.e. conventional trip signal has been issued but blocked by the adaptive trip logic. Hence it will prevent the false operation. Case 4 describes the situation of a fault before the capacitor, so both the blocks give high logic. And hence a trip signal to the breaker will be issued.

2.7 Algorithm for Circuit Breaker Failure Backup

Once the required tripping criteria are satisfied relay will issue a trip signal. In a conventional relay once it issued a trip signal its job is done. But in the case when either the circuit breaker is faulty or the cable carrying the trip signal to the circuit breaker is wrecked, even though relay is working correctly our job will not be furnished. So in the presented relay author has included an algorithm to check the integrity of the circuit breaker at the time of fault and if something is not favorable it will arrange for some backup. It has been explained in detail in the next paragraph.

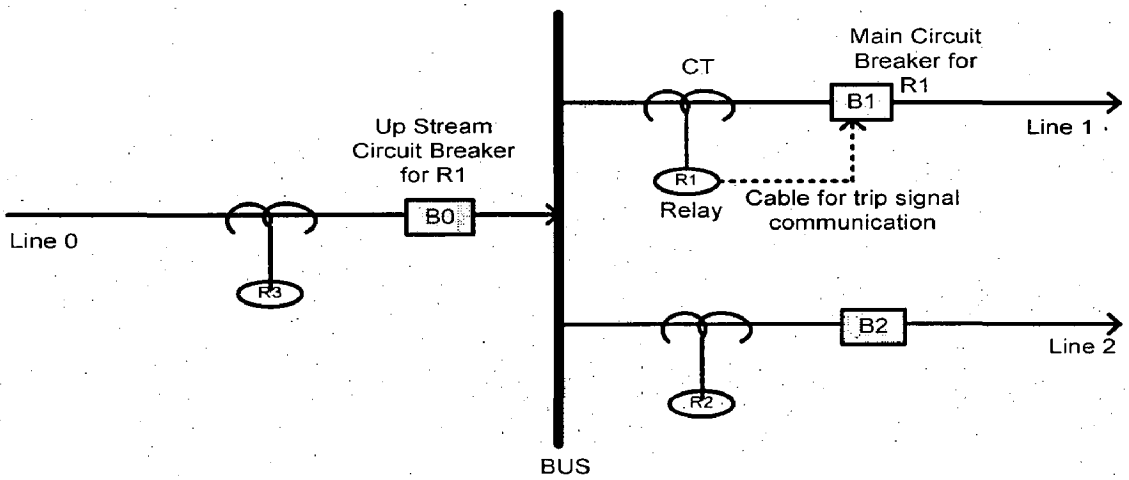


Figure 2.10 Single line diagram showing circuit breaker arrangement

Lets we are concerned with the protection of line 1 (referring to Fig.2.10) which is being protected by relay R1. Let's for any fault at line 1 tripping criteria is satisfied and relay R1 issued a trip signal, but due to wreckage in cable or fault in the main circuit breaker it could not operated. Then in this case the presented relay will check whether breaker has been operated or not for user specified period and if it detects that breaker has not operated it will issue the same

trip signal to the up upstream breaker (Breaker B0). This has been achieved using the algorithm presented in Fig. 2.11.

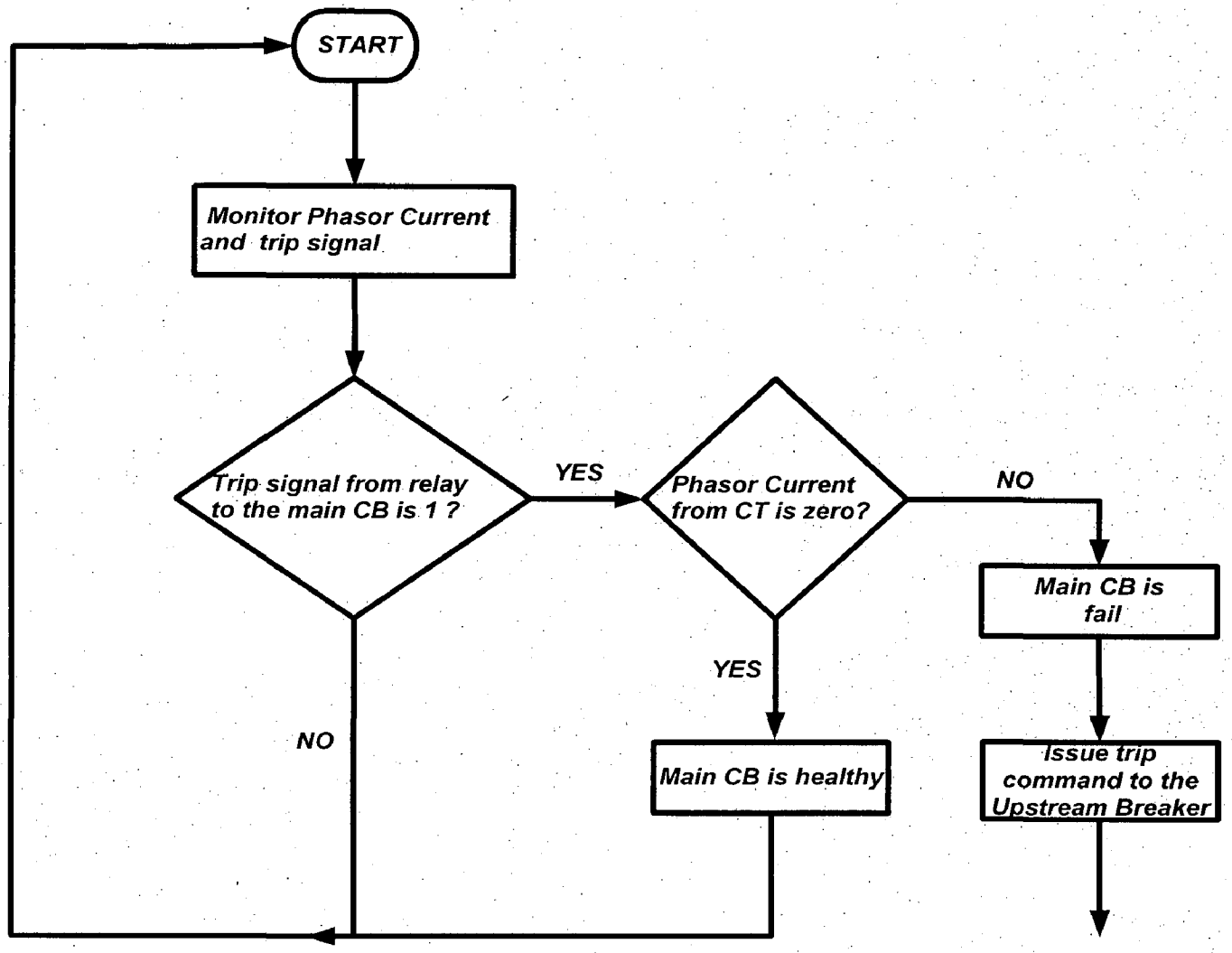


Figure 2.11 Algorithm for Circuit Breaker Failure Backup

In the presented scheme the relay checks for the current signal from CT and trip signal from the relay. If the relay has issued a trip signal and circuit breaker and cables are healthy the circuit breaker will operate and the current through CT will be zero and hence there will be no need to send a signal to the upstream breaker. But in the case of circuit breaker fail or cable wreckage even though the relay will issue a trip signal it will not operate and the current through CT will not be zero hence the relay will send a trip signal to the upstream breaker after a specified period of time. Table 2.2 summarizes the above stated conditions.

Table 2.2 Logic Combination for Upstream Breaker Operation

Case	Trip Signal (C)	Current through CT (I= 0 then A= 1,Else if I > 0 then A=0)	(C) & (A) = Output Logic to Upstream breaker
1	0	0	0
2	0	1	0
3	1	0	0
4	1	1	1

2.8 Algorithm for Close in fault protection

In case of the fault just after the relaying point, the distance relay may fail to operate because of absence or significance reduction of polarizing voltage.

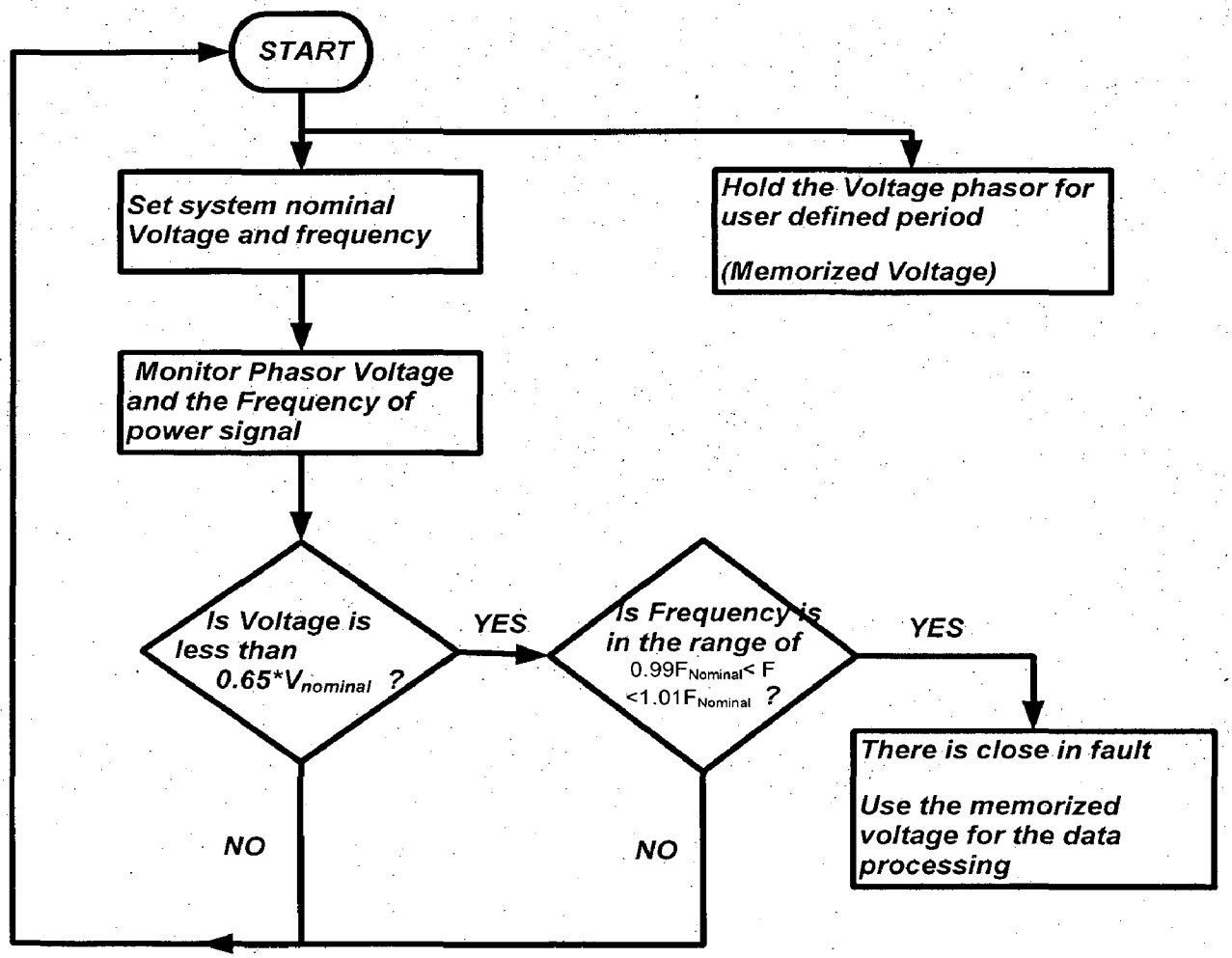


Figure 2.12 Algorithm for Close-in Fault Protection

For the purpose $V_{Nominal}$ has been taken as the reference voltage, which depends on the system voltage. When a close in fault occurs the voltage drops to around 0.65 times the system voltage [21]. This is one of the conditions to be considered. The voltage drop to this level does not solely because of close fault but it may happen because of change in the excitation level of the alternator. So we need to take that also in to account.

Hence the voltage $V_{Nominal}$ is the reference voltage for the voltage memory. If the measured voltage drops below the 0.65 $V_{Nominal}$ and the frequency is not in the range of [21].

$$0.99\ F_{Nominal} < F_{Nominal} < 1.01\ F_{Nominal}$$

the relay will enable the voltage memory action. We need to check the second condition because voltage drop may be because of lowering the excitation of the alternator. This is not a fault condition, so the relay should not enable the voltage memory block. The time for which the memory block should retain the pre-fault voltage can be set by the end user. Fig. 2.12 gives the algorithm for voltage memory action during close in fault and Table 2.3 tabulates the above stated conditions.

Table 2.3 Logic Combination for Voltage Memory Enabling

Case	Voltage condition	Frequency Range	Voltage memory enable
1	0	0	0
2	0	1	0
3	1	0	0
4	1	1	1

CHAPTER 3
LABORATORY SETUP FOR REAL TIME SIMULATION OF ADAPTIVE DISTANCE RELAY

3.1 Introduction of Power and Control Circuit of the Real -Time Setup

The laboratory setup has been made in power system laboratory at Indian Institute of Technology Roorkee, Roorkee. This chapter describes the detail of the components of the scaled model that are custom designed and build for the specific needs of the system. Figure 3.1 shows the actual hardware implementation. Fig.3.2 shows the photographs of different components used for the setup.

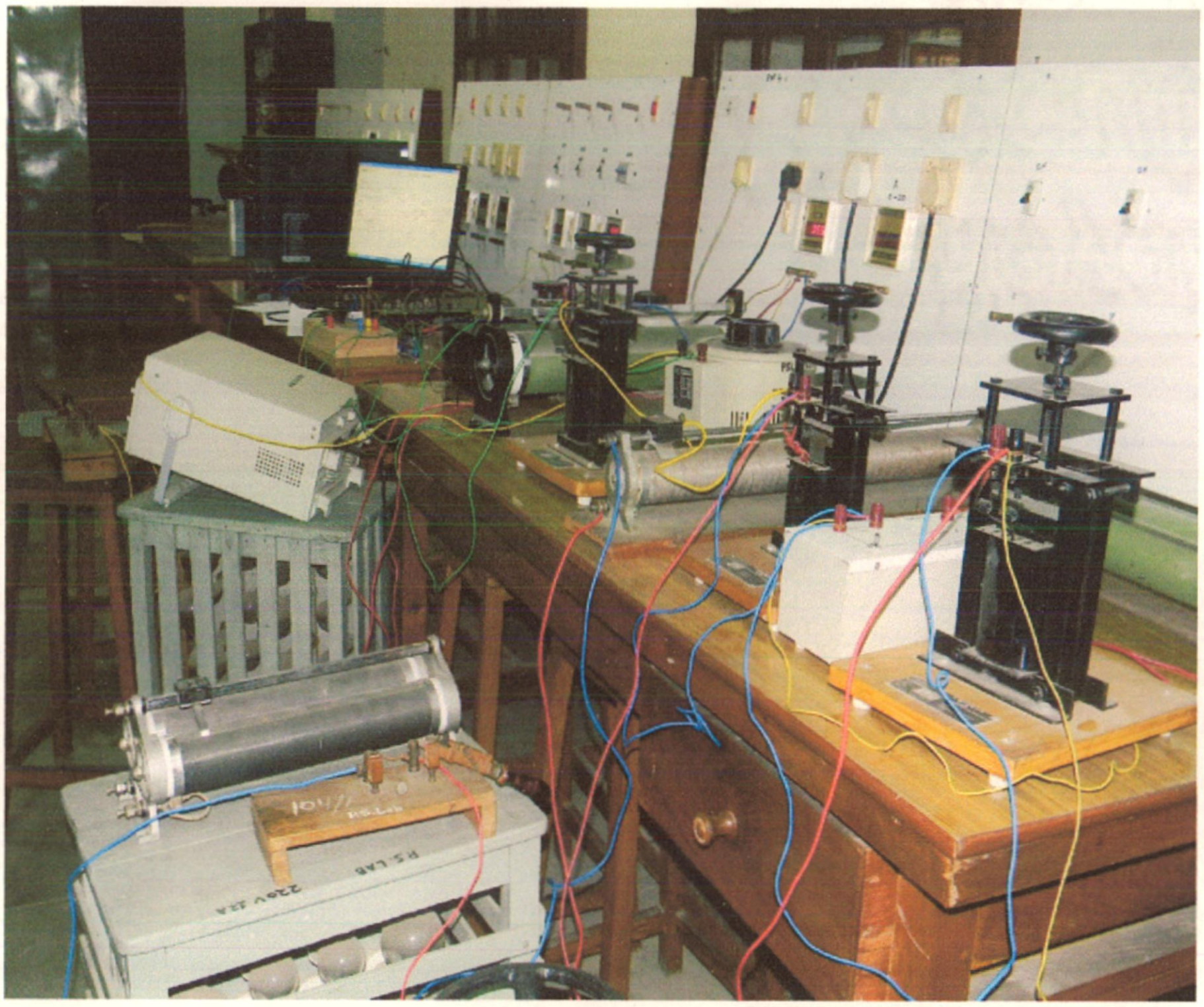
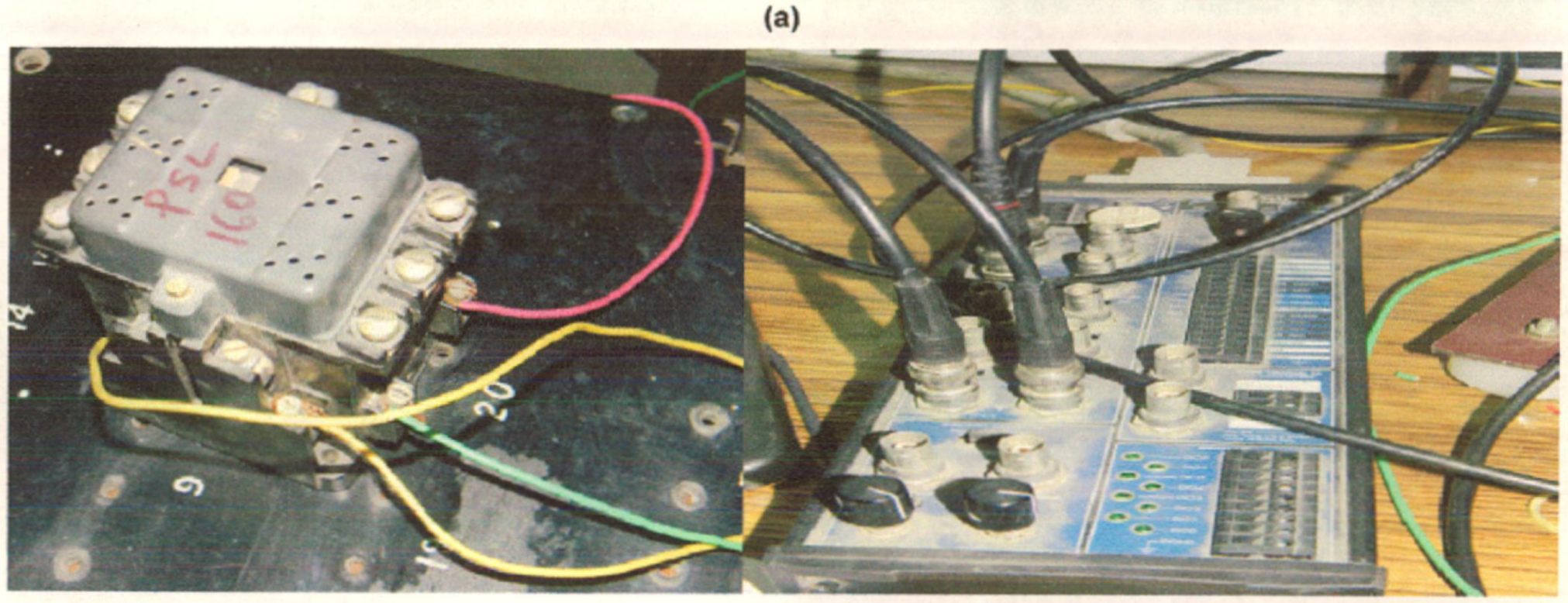
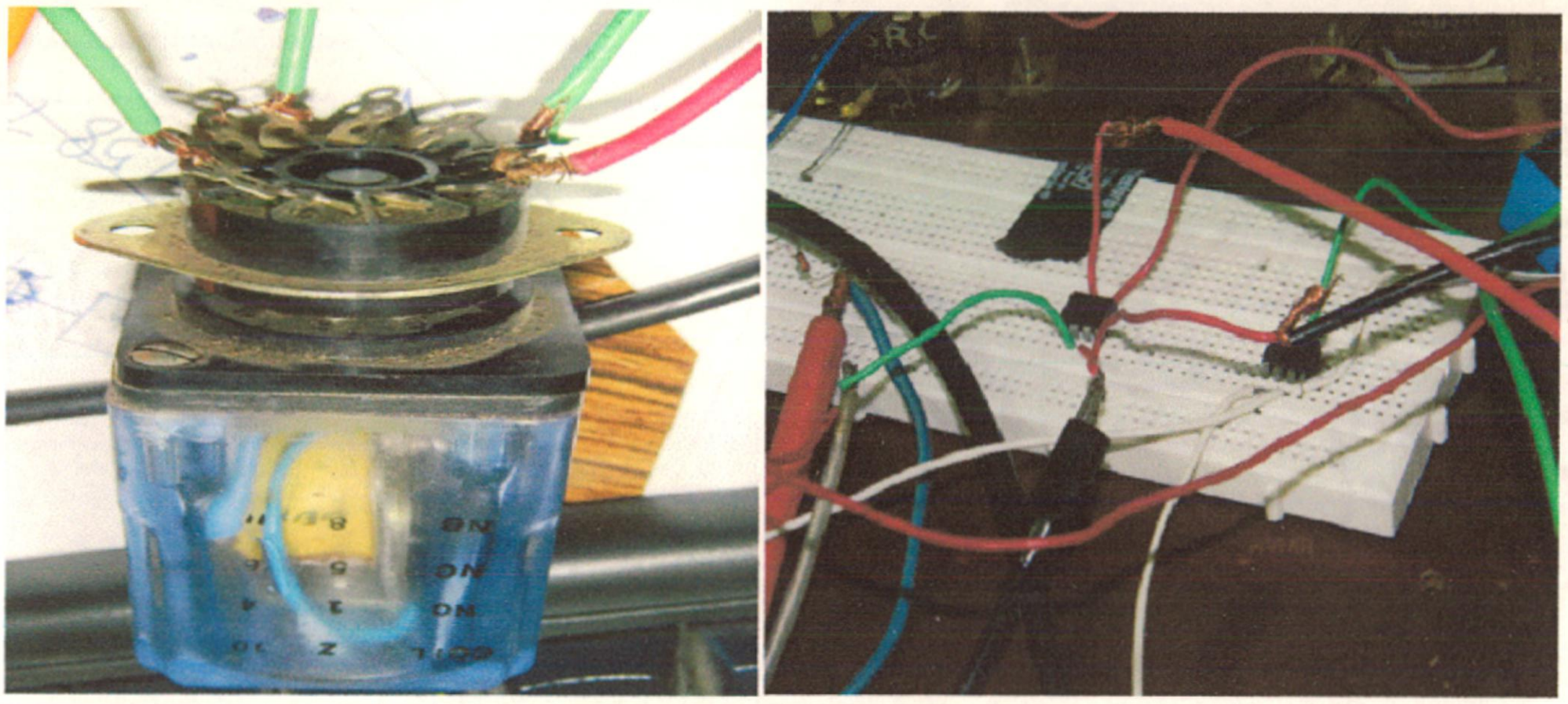


Figure 3.1 Laboratory Hardware Implementation

(a)



(b) (c)



(d) (e)

Figure 3.2 (a) Real Time setup (b) CB (c) BMC2120 connector (d) auxiliary relay (e) Op-amp connection

A. Voltage source

The input voltage has been taken from single phase, 230 volts, 50 Hz AC supply, which is used to energize the transmission network through an autotransformer.

B. Transmission network

For simulating the transmission line Rheostats, Variable Inductors, and Series Capacitor has been used along with the Inductive Load Bank.

C. Power flow in the system

1. *To energize the system:* The system is energized by moving the manual switch to 6 volts (Fig.3.3).

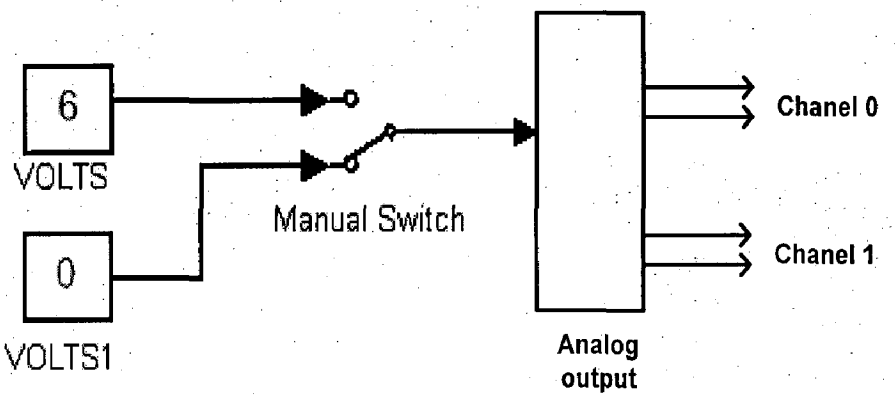


Figure 3.3 Matlab Switch for Energizing or de-energizing the System

As it is done and run it will send 6 volts signal to analog output channel 0. Referring to figure 3.5(b) this 6 volt signal will be applied to the op-amp 741 which has been configured in non-inverting mode (driver circuit). Output of the op-amp will energize the DC relay R_{DC1} which will close its NO contact RDC1 -1 which will further energize the auxiliary relay A1 and hence it's NO contact A1-1 will be closed which will energize the energizing coil of the contactor C1 (figure 3.5(a)) , which will result in closing of its NO contact C1-1 in figure 3.4 and C1-2 will seal on the contact in figure 3.5(a) which will relieve the contact A1-1. Because of the closure of C1-1 line will be energized.

2 *To de-energize the system:* To de-energize the system move the manual switch to 6 volts (Fig.3.3) again. This time it will send 6 volts signal to analog output channel 1. Output of the op-amp will energize the DC relay R_{DC2} which will close its NO contact R_{DC2} -1 which will further energize the auxiliary relay A2 and hence it's NC contact A2-1 opens up which de-energizes the coil of the contactor C1, which results in opening of its NO contact C1-1 (figure 3.4). And the line will be de- energized

D. Fault creation system: Manual switch 1 and 2 in figure 3.4 has been used for creating the fault before and after the series capacitor respectively at different locations.

E. Circuit Breaker Failure creation: for creating the CB fail condition open the CB fail switch provided in control circuit in figure 3.5(b). So that even though the trip signal has been issued from channel 1 which closes the NO contact R_{DC2}-1 but due to wreckage in the control cable i.e. opening of CB fail switch it will not energize A2 and hence A2-1 will remain closed. So current will continue to flow through the system.

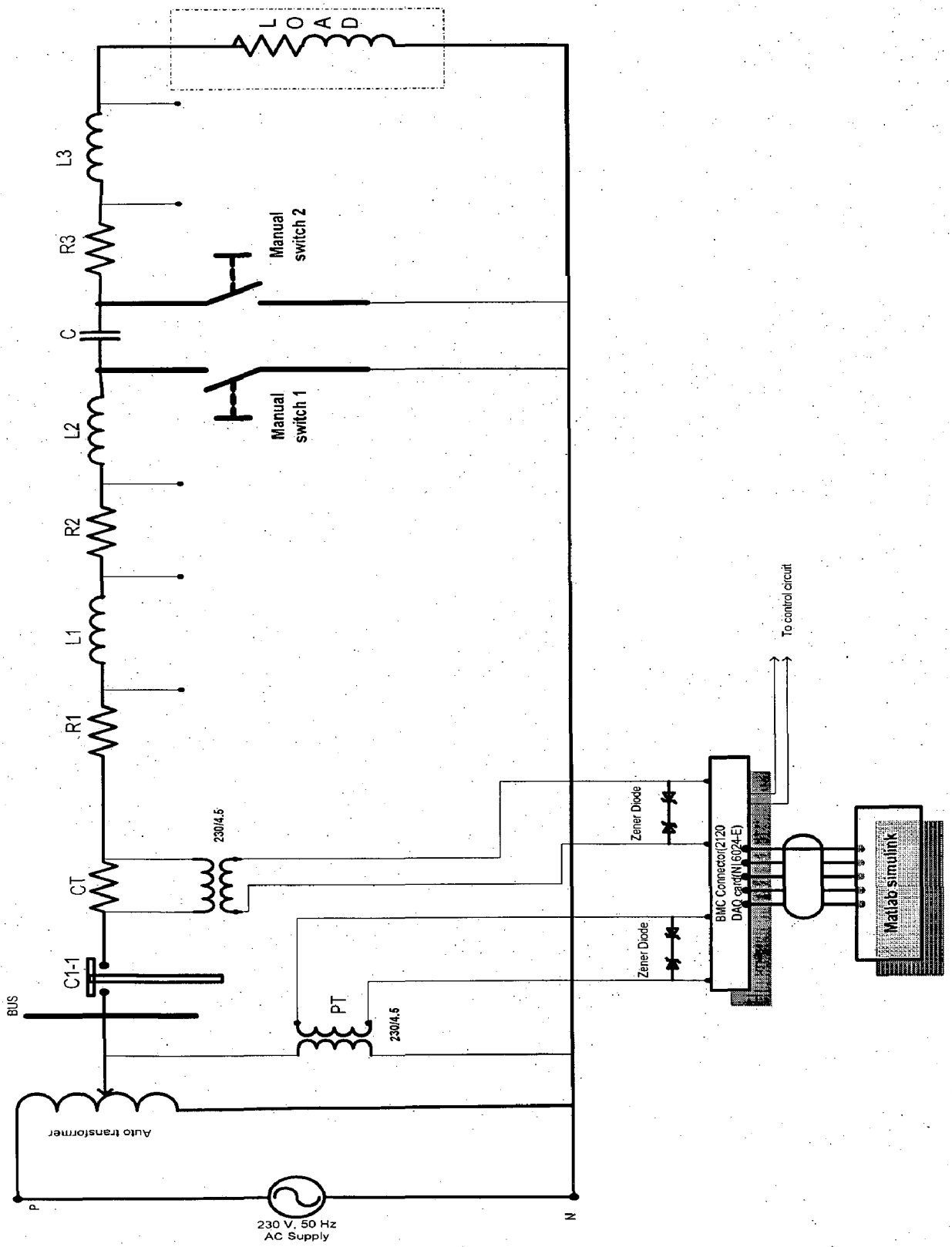
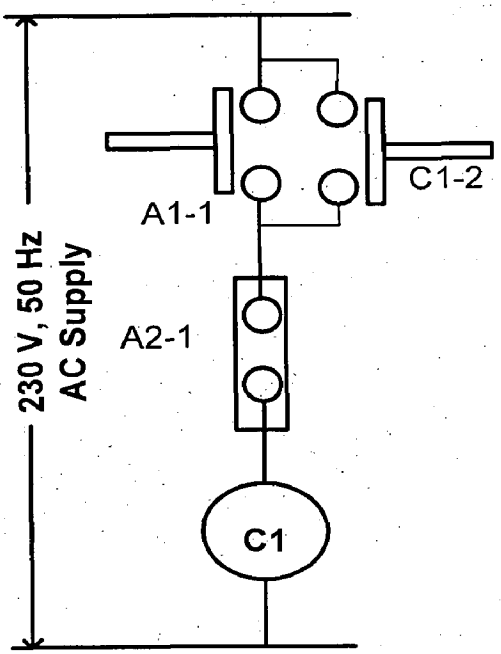


Figure 3.4 Power Circuit of Laboratory Setup for Testing the Adaptive Relay



(a)

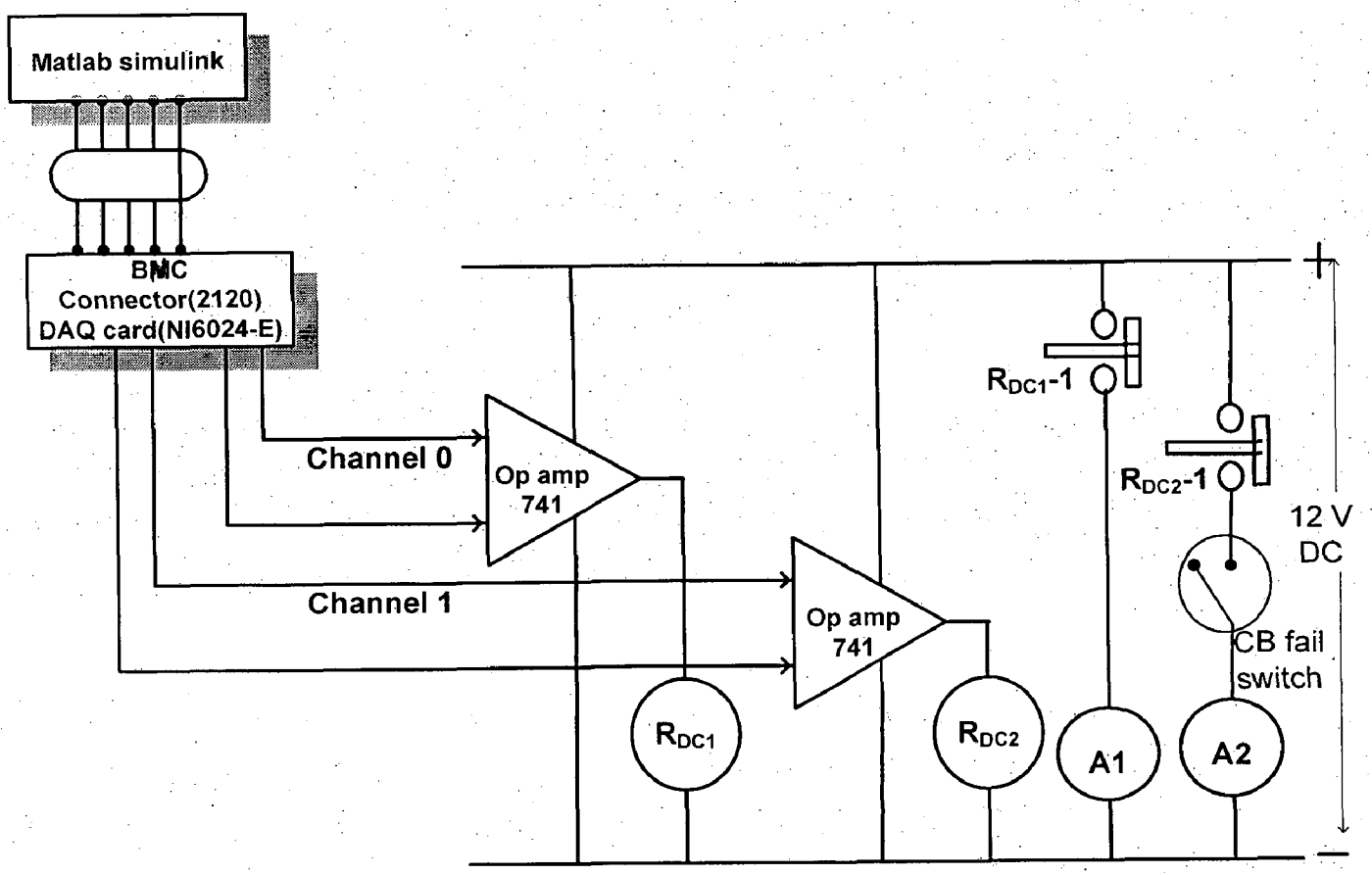


Figure 3.5 (b) Control Circuit of the Power Circuit

Since we need to give signals (voltage and current) from real word to computer we need some transducer to bring down the actual current and voltage signal to the level which is compatible with the computer. So for the purpose voltage and current transducer has been used.

3.2 Voltage Transducer:

Here step down transformer is used as P.T in the emulated model. The transformer isolates the voltage at the primary side of 230V to its secondary side of 4.5V. The secondary side is connected in differential mode to the DAQ card as shown in figure 3.6. The zener diode of breakdown strength 5.2V has been connected in the secondary of the step down transformer to prevent the voltage input exceeding 5.2 V to the DAQ card.

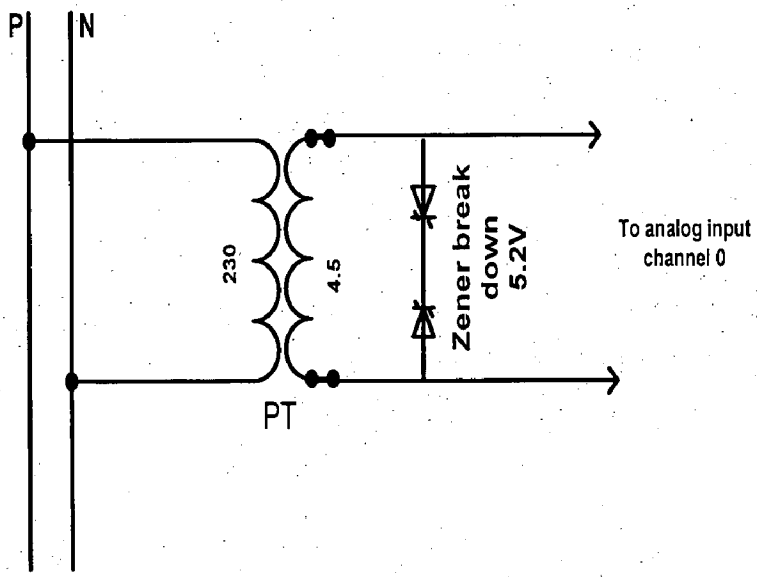


Figure 3.6 Voltage transducer- voltage fed to the DAQ

3.3 Current Transducer

Resistance of 12.2 Ω has been connected in series with the line (same has been used for making line resistance also) and the voltage drop across it

$$V_R = 12.2 * I_{phase}$$

will be applied across the step down transformer and then to the DAQ card in differential mode as shown in Fig.3.7. The zener diode has been connected for the same reason as in the voltage transducer.

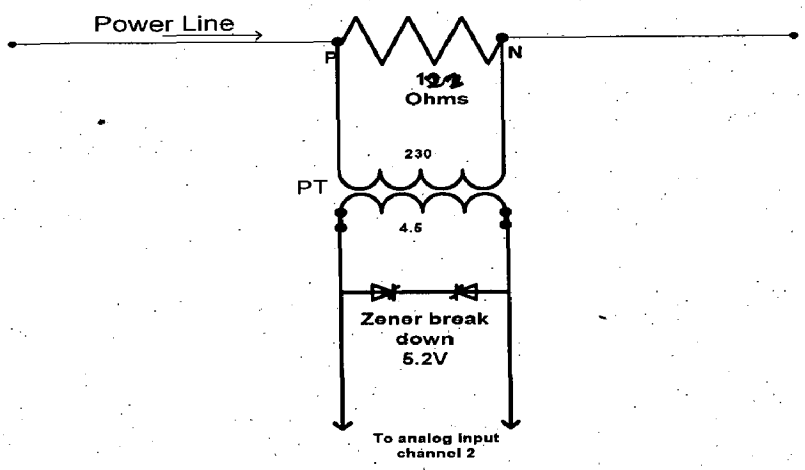


Figure 3.7 Current Transducer- Equivalent Voltage Fed to the DAQ

3.4 Driver Circuit

Driver circuit consists of op-amp 741 and 6 Volt DC relay. The circuit has been shown in figure 3.8. The op-amp has been configured in non-inverting mode.

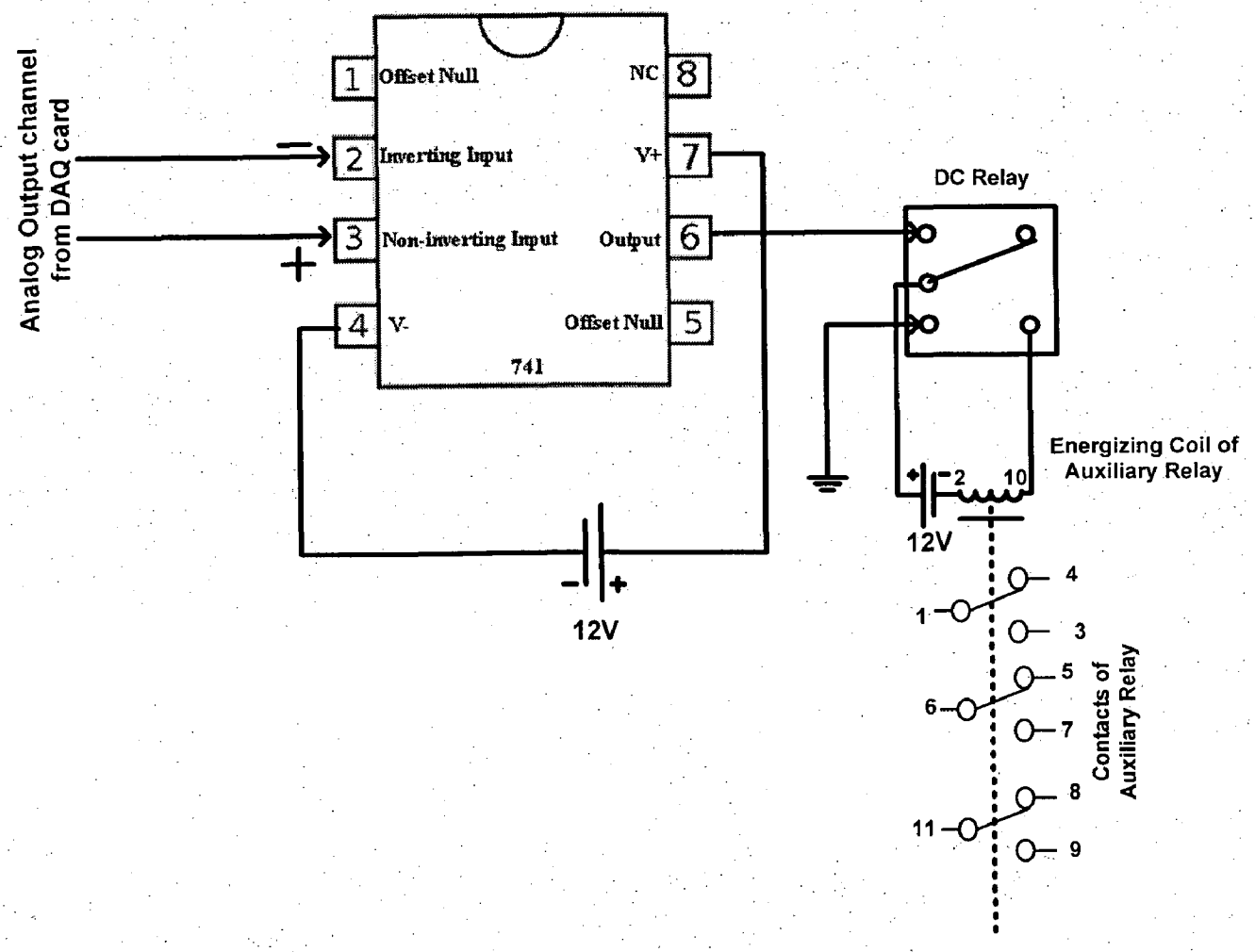
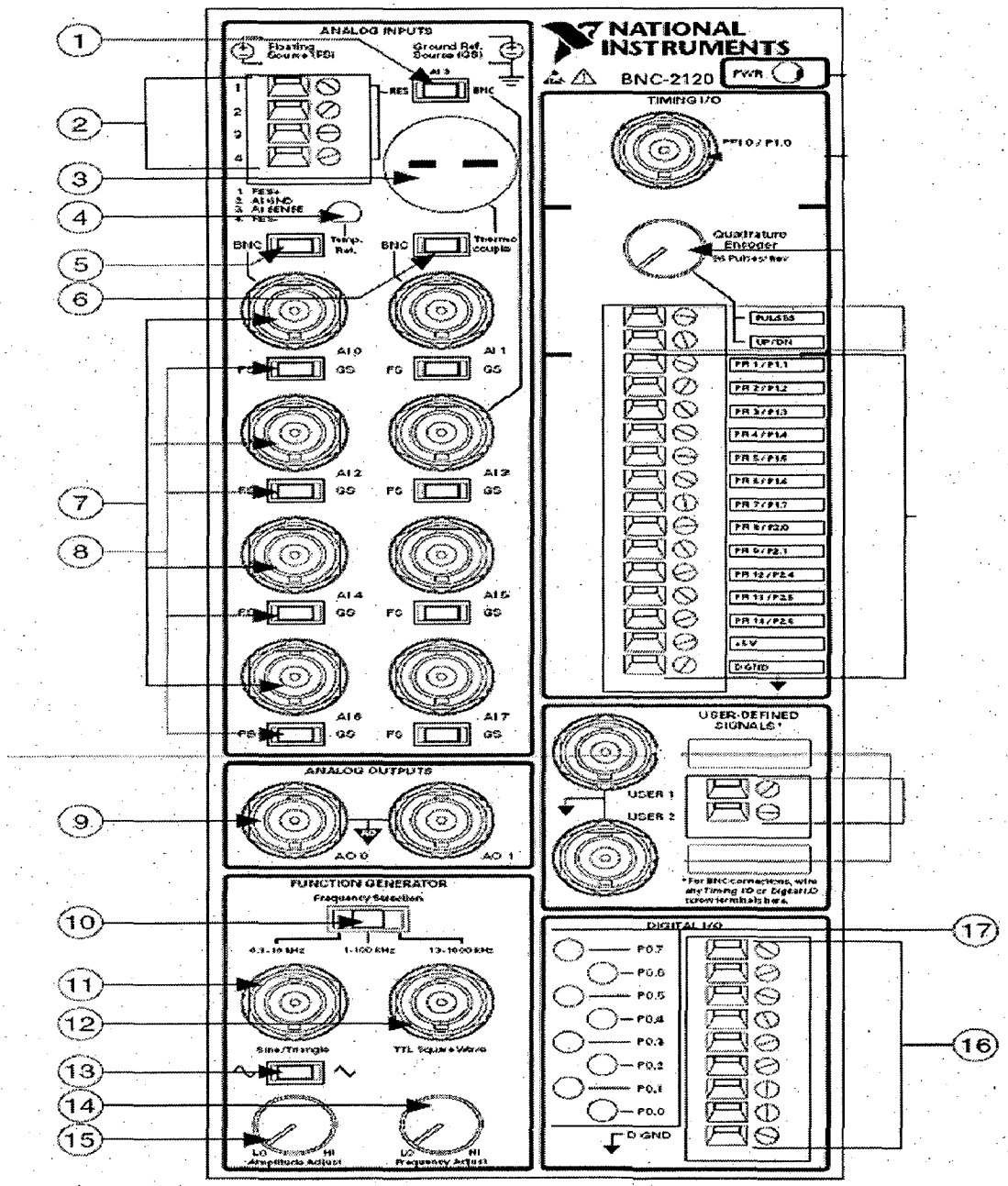


Figure 3.8 Driver circuit

3.5 Data Acquisition [19]



1	RES/BNC Switch (AI 3)	9	Analog Output BNC Connector
2	Resistor Measurement Screw Terminals	10	Frequency Range Selection Switch
3	Thermocouple Input Connector	11	Sine/Triangle BNC Connector
4	Temperature Reference	12	TTL Square Wave BNC Connector
5	BNC/Temp. Ref. Switch (AI 0)	13	Sine/Triangle Waveform Switch
6	BNC/Thermocouple Switch (AI 1)	14	Frequency Adjust Knob
7	Analog Input BNC Connectors	15	Amplitude Adjust Knob
8	FS/GS Switches	16	Digital I/O Screw Terminals
		17	Digital I/O LEDs

Figure 3.9 BNC Connector 2120 Schematic [19]

Fig.3.9 shows the schematic of BNC connector2120. Here the connector has been used with NI6024-E DAQ card, which has been mounted in the PCI slot of Personal computer.

Connecting Analog Input Signals:

- It can measure differential AI signals, Connected in Differential Analog Input Signals mode.
- It can measure analog temperature and Resistance.

Connecting Differential Analog Input Signals

It can be used to connect AI0 to AI7 signals to NI DAQ device. It is *only* intended for differential analog input signals. The number of connectors we use depends on our DAQ device and application.

Connecting Analog Output Signals

Analog output channel AO0 andAO1 on BNC connectors on the BNC-2120 front panel has been used for connecting the analog output signals from the DAQ device.

The DAQ card has been interfaced with the Personal computer using Simulink Data acquisition block. The block has been configured in non-synchronous mode, with the input/ output range of -10V to +10V. The input has been given in differential mode with a sampling rate of 500 samples per second.

Specifications of the BNC 2120 have been given in appendix-B.

NI DAQ CARD 6024E [20]:

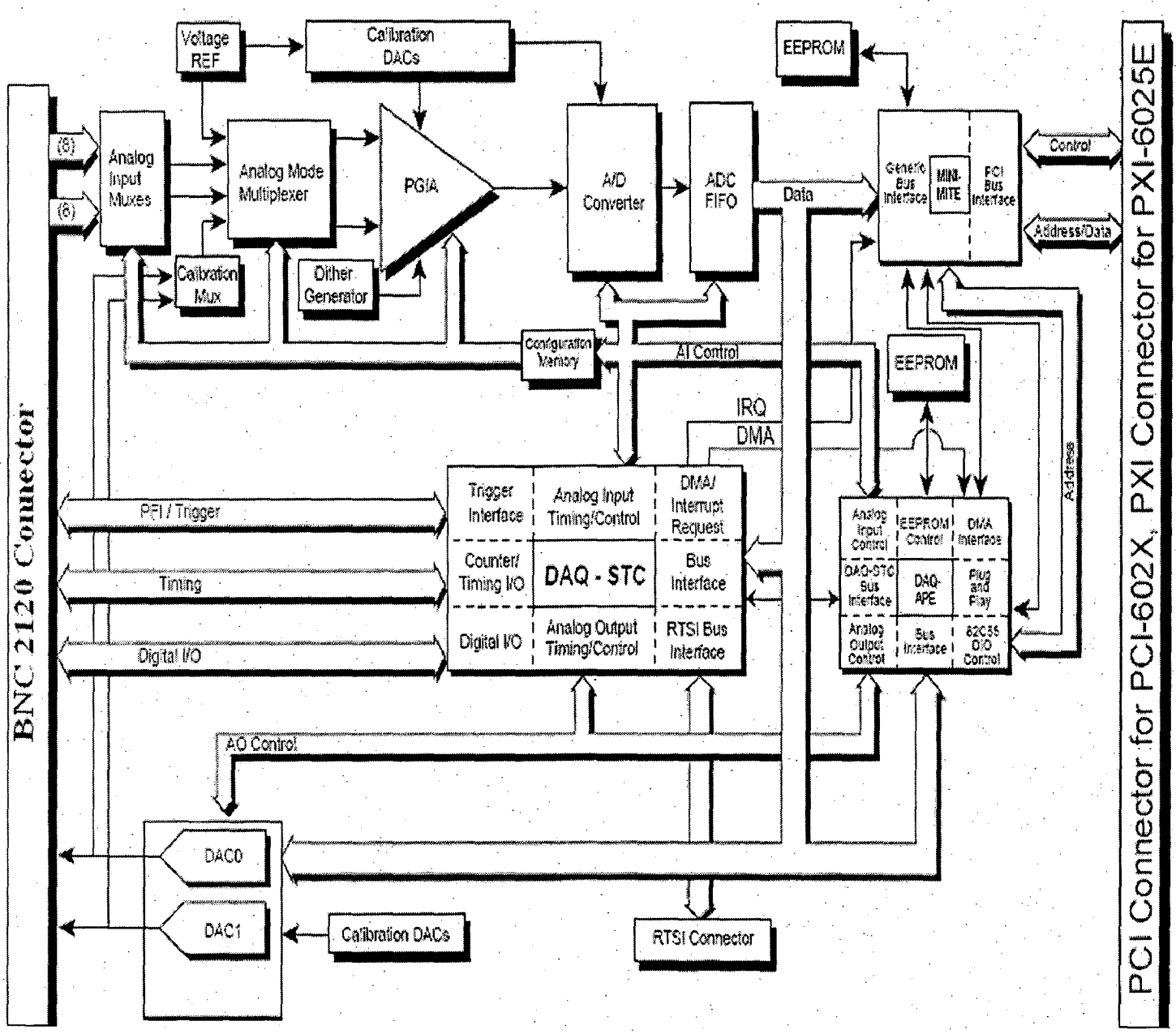


Figure 3-10 NI DAQ 6024E Block Diagram [20]

Analog Input

The boards have a bipolar input range that changes with the programmed gain. Each channel may be programmed with a unique gain of 0.5, 1.0, 10, or 100 to maximize the 12-bit analog-to-digital converter (ADC) with the proper gain setting, we can use the full resolution of the ADC to measure the input signal.

Table 3.1. Analog Measurement Precision of NI DAQ 6024E

Gain	Input Range	Precision
0.5	–10 to +10 V	24.41 mV
1.0	–5 to +5 V	2.44 mV
10.0	–500 to +500 mV	244.14 mV
100.0	–50 to +50 mV	24.41 mV

Analog Output

The boards supply two channels of analog output voltage at the I/O connector. The bipolar range is fixed at ±10 V. Data written to the digital-to-analog converter (DAC) is interpreted as two's complement format.

Specifications of the N-6024E have been given in appendix-C.

CHAPTER 4

REAL TIME SIMULATION OF THE PRESENTED RELAY

4.1 Zone Setting and Description for Simulating the Adaptive Feature of the Relay In The Presence Of the Series Capacitor

Figure 4.1 shows the single line diagram of the network presented in figure 3.4

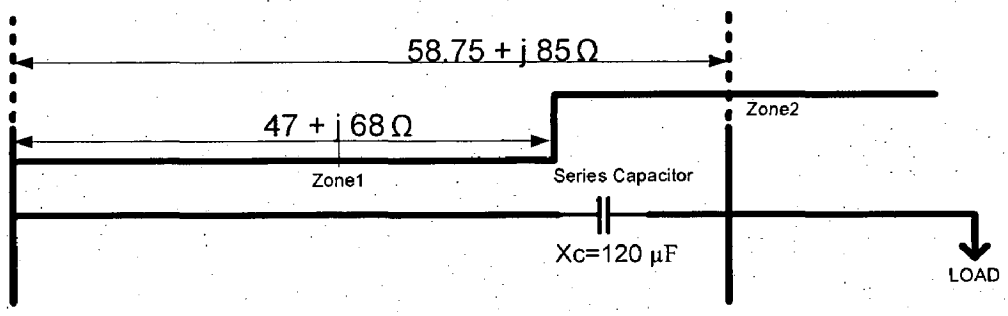


Figure 4.1 Zone setting for Power System Network

Series capacitor has been installed in the second zone as it has been proposed in section 2.5.

Line impedance is

$$58.75 + j\,85\ \Omega^*$$

Load is

$$2.8 + j\,24\ \Omega$$

As per the convention first zone setting is around 70-85%. Here 80% has been taken for first zone setting

So it is

$$0.80^* (58.75 + j\,85\ \Omega)$$

$$= 47 + j\,68\ \Omega$$

Fault has been created by closing the manual switch 1 and 2 in Fig.3.4 respectively for creating the fault before and after the capacitor.

*The XL/R ratio is very small because of the inherent resistance of the inductor but it favors the results because in a long transmission line ratio can never be less than it. Whereas as the ratio increases the presented discriminatory feature will be more pronounced.

Figure 4.2 and 4.3 show the impedance trajectory of the fault for the fault before and after the series capacitor respectively.

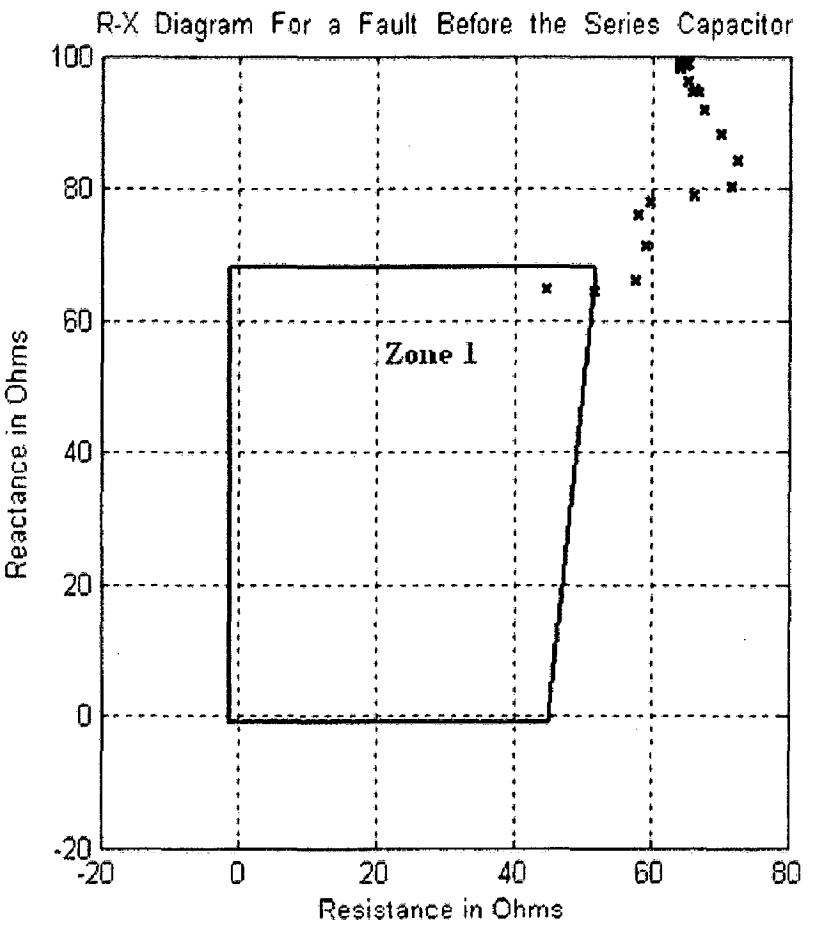


Figure 4.2 Impedance Trajectory of the Fault for the Fault before the Series Capacitor (Simulated in Real Time)

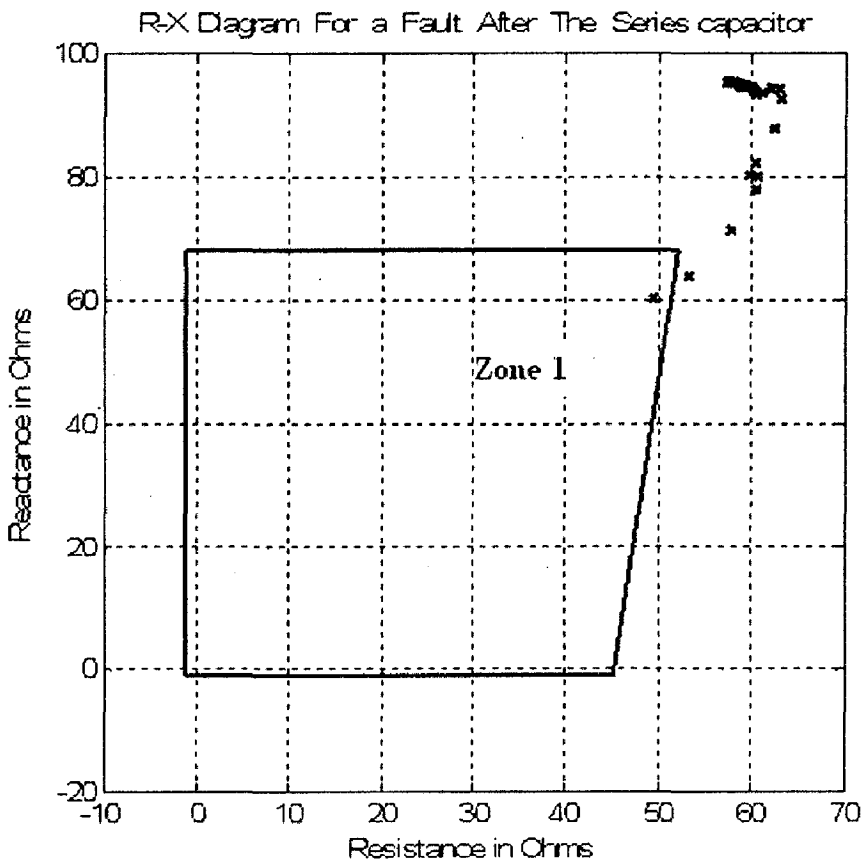


Figure 4.3 Impedance Trajectory of the Fault for the Fault after the Series Capacitor (Simulated in Real Time)

As can be seen from the Fig.4.3 & 4.4 the fault just before the capacitor is in the first zone of protection as it should be. But the fault just after the capacitor is also seen in the first zone, actually which should be in the second zone since the area at and after the series capacitor is in the second zone. It can be understood in a better way by looking at figure 4.4.

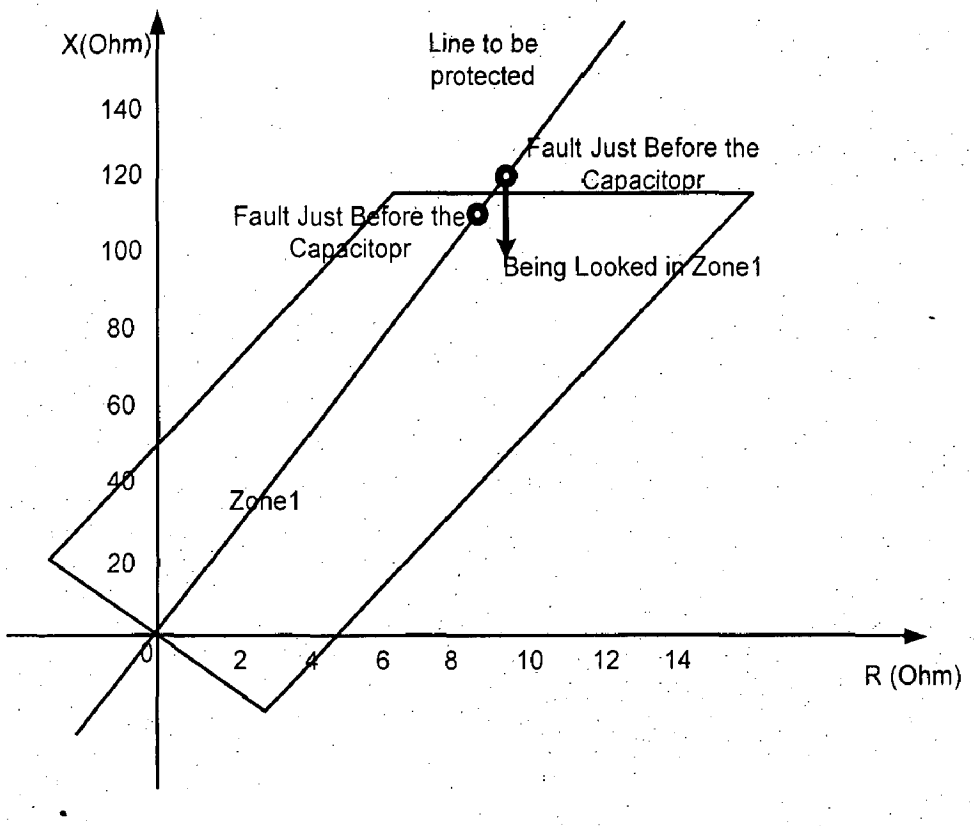


Figure 4.4 Effect of Series Capacitor on Impedance Measurement

The algorithm proposed in section 2.5 takes care of the above stated problem.

4.2 Description for Simulating the Adaptive Feature for Taking Care of Circuit Breaker Failure

For creating the circuit breaker fail opens up the switch named as CB fail switch in figure 3.5(b). So that even though the relay issues a trip command which will energies R_{DC2}, and hence it's NO contact R_{DC2}-1 will be closed but due to opening of CB fail switch A2 will not be energized and thus NC contact A2-1 in figure 3.5(a) will remain close and hence the relay will have to send a trip signal to the upstream circuit breaker as it has been explained in section 2.7. The trip signal for upstream breaker has been simulated by LED.

4.3 Description for Simulating the Adaptive Feature for Taking Care of Close in fault protection (voltage memory action)

This has been simulated in Matlab only because in real time if we reduce the voltage to the specified level, current will also reduce so, even the fault situation will become the normal condition. Further the frequency variation cannot be shown in the presented real-time setup. For creating such a situation of close in fault in Matlab the bus voltage has been lowered by lowering the alternator terminal voltage (as given in section 2.8), at the same time frequency variation has been taken care of. When the voltage has been lowered at the same power frequency, voltage memory will be enabled whereas if voltage magnitude is reduced to different frequency (as given in section 2.8) it will not enable the voltage memory.

CHAPTER 5

REAL TIME AND MATLAB SIMULATION RESULTS

5.1 Results for adaptiveness against fault in series capacitor compensated line

The impedance trajectory for real time simulation has already been shown in chapter 4. So figure 5.1 to 5.3 shows the impedance trajectory for Matlab simulation.

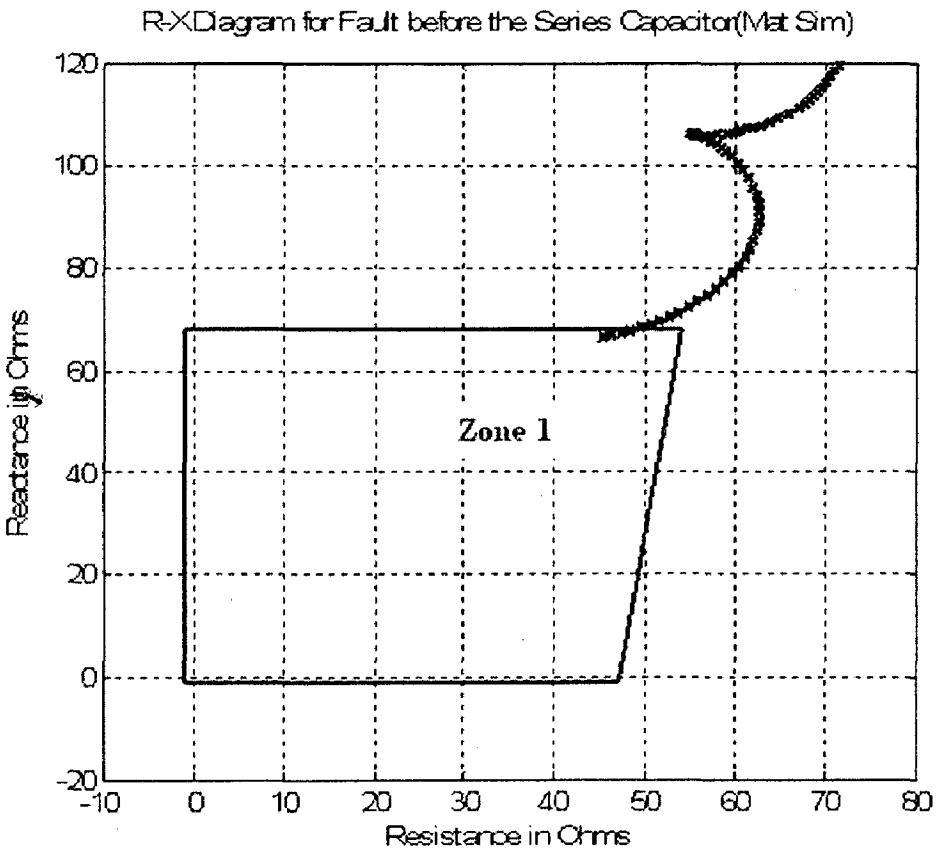


Figure 5.1 Impedance Trajectory of the Fault for the Fault before the Series Capacitor (Simulated in Matlab)

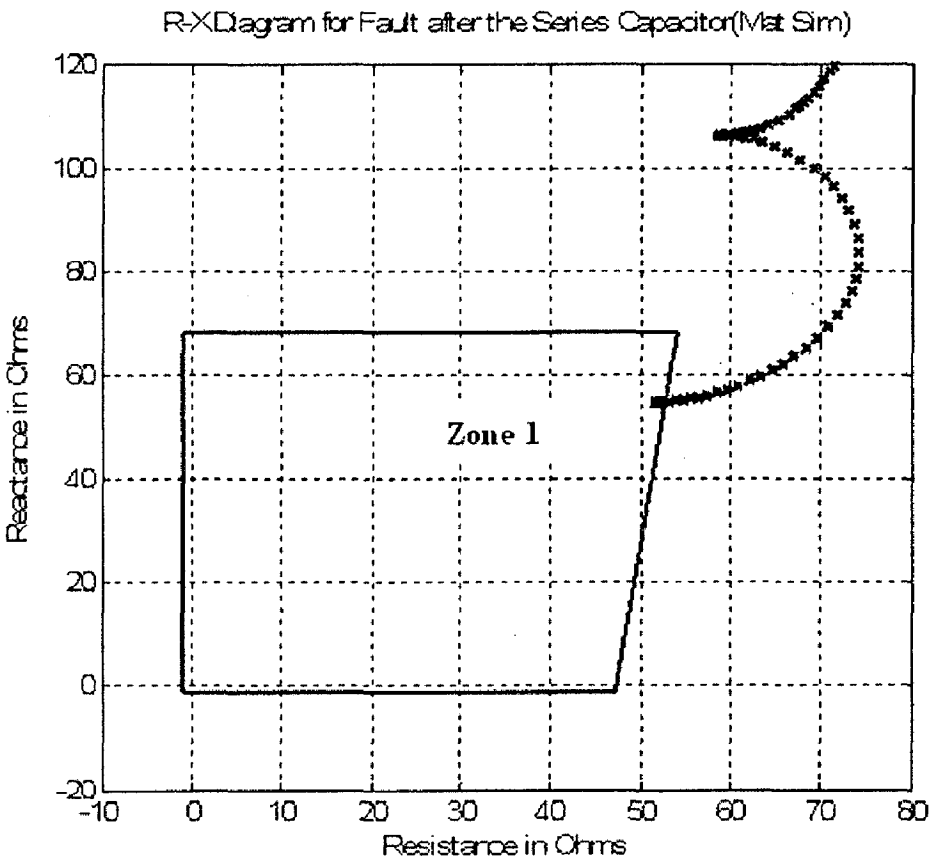


Figure 5.2 Impedance Trajectory of the Fault for the Fault after the Series Capacitor (Simulated in Matlab)

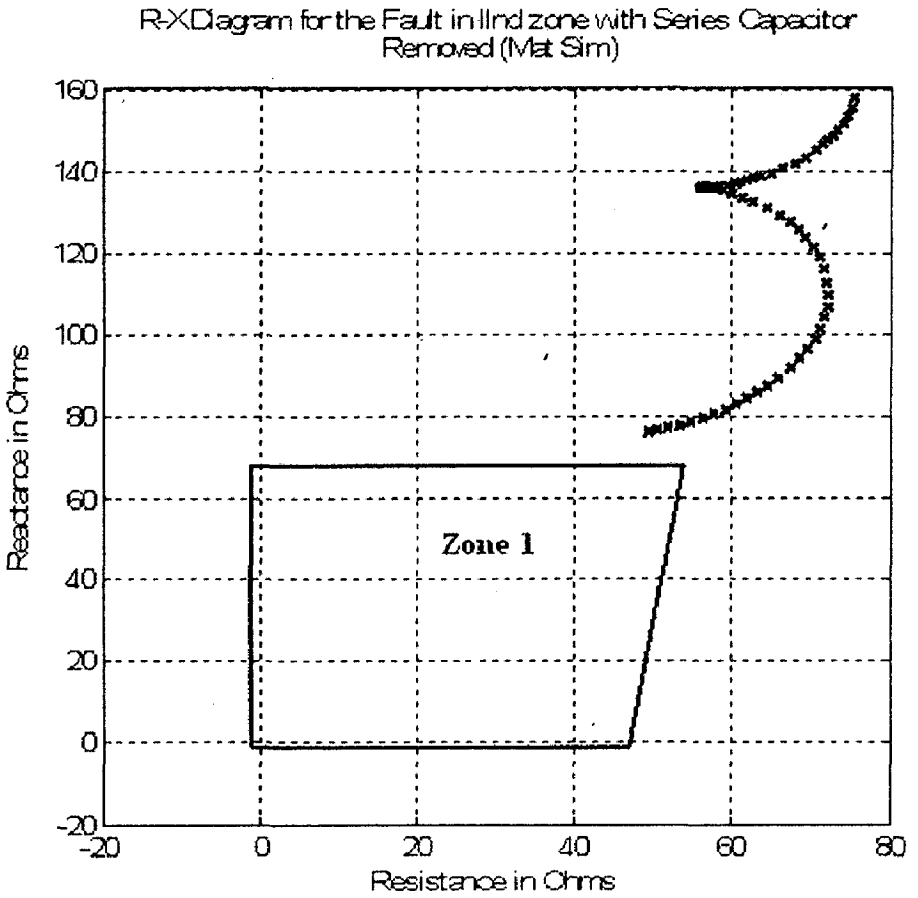


Figure 5.3 Impedance Trajectory of the Fault for the Fault with Series Capacitor Removed (Simulated in Matlab)

As it can be seen from figure 5.3 if series capacitor is not installed in the line the fault in the second zone will remain in the second zone whereas it will come in first zone in the case of series capacitor installed line (Figure 5.2).

Figure 5.4 to 5.7 shows the results of Real time simulation on the network shown in Fig. 3.4. It includes phase voltage, phase current, DC component of fault current, and the trip signal status.

Figure 5.4 shows the details for the fault just before the series capacitor

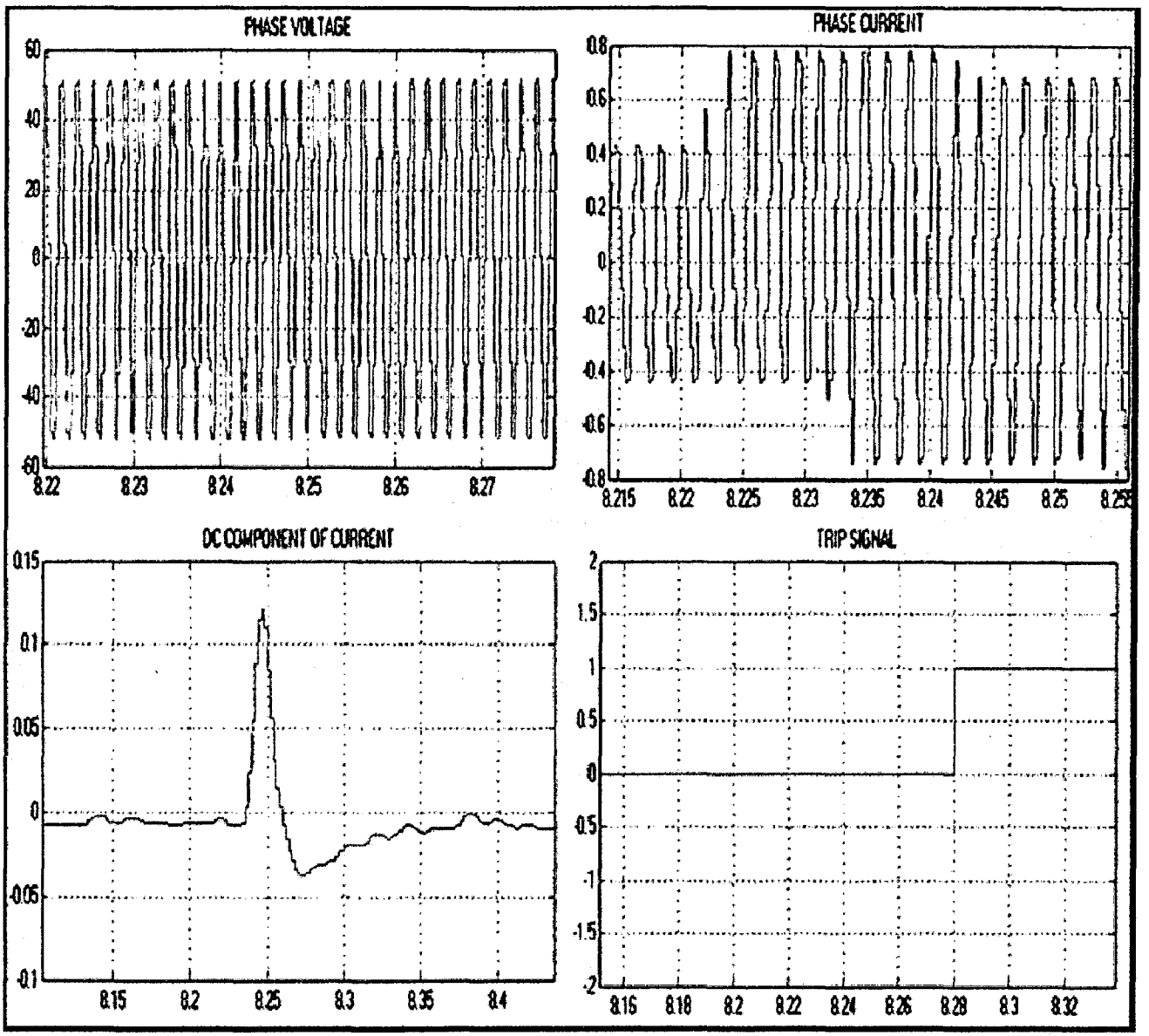


Figure 5.4 Results of Fault before the Capacitor (Real Time Simulation)

As per the description in section 2.5, figure 5.5 shows the case no. 4 i.e. fault is in zone one and before the capacitor. Hence the relay issued a conventional trip signal as well as adaptive trip signal, so the final trip decision is true.

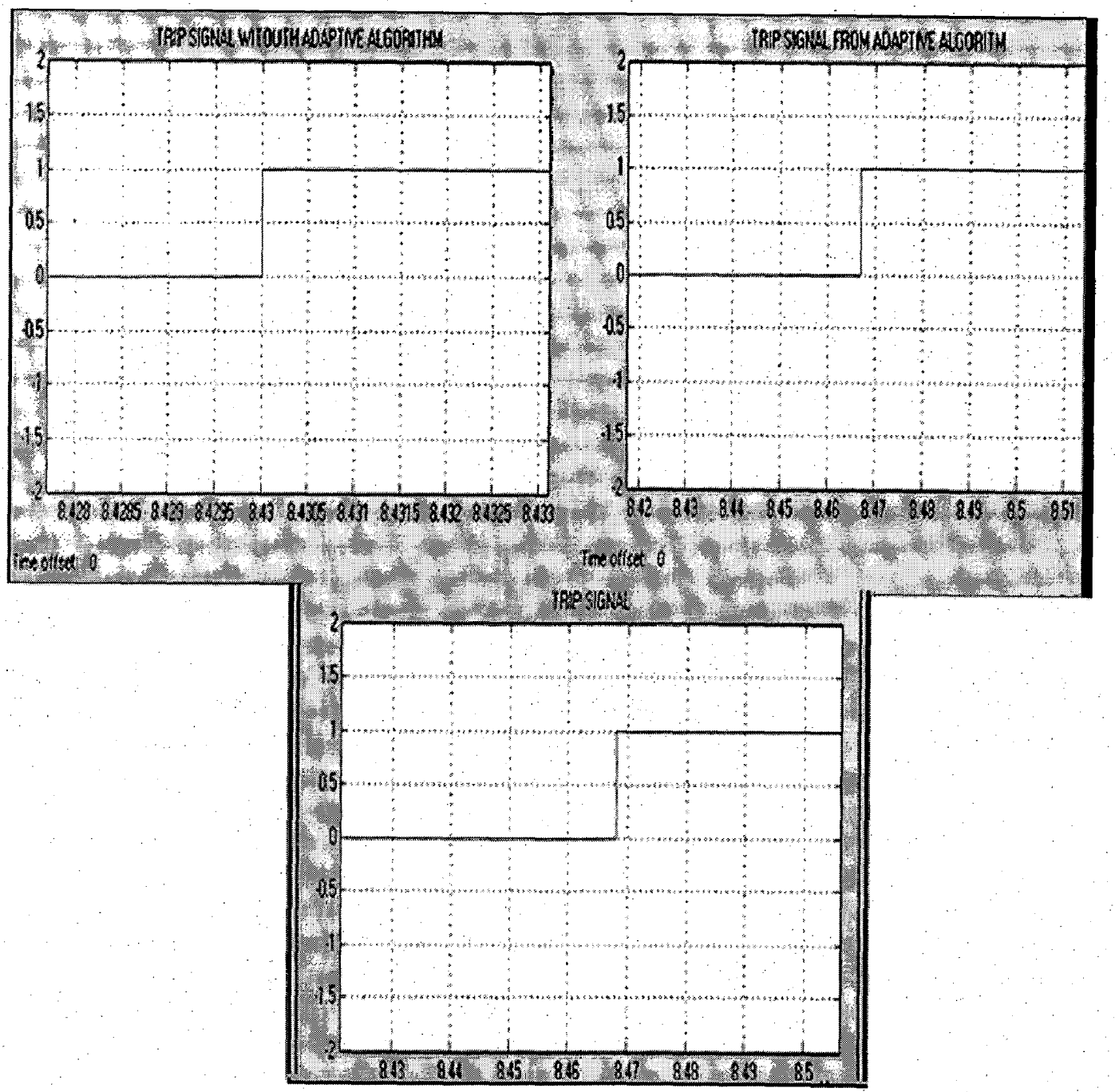


Figure 5.5 Conventional, Adaptive and Final trip signal (For fault before the capacitor)

Figure 5.6 shows the details for the fault just after the series capacitor

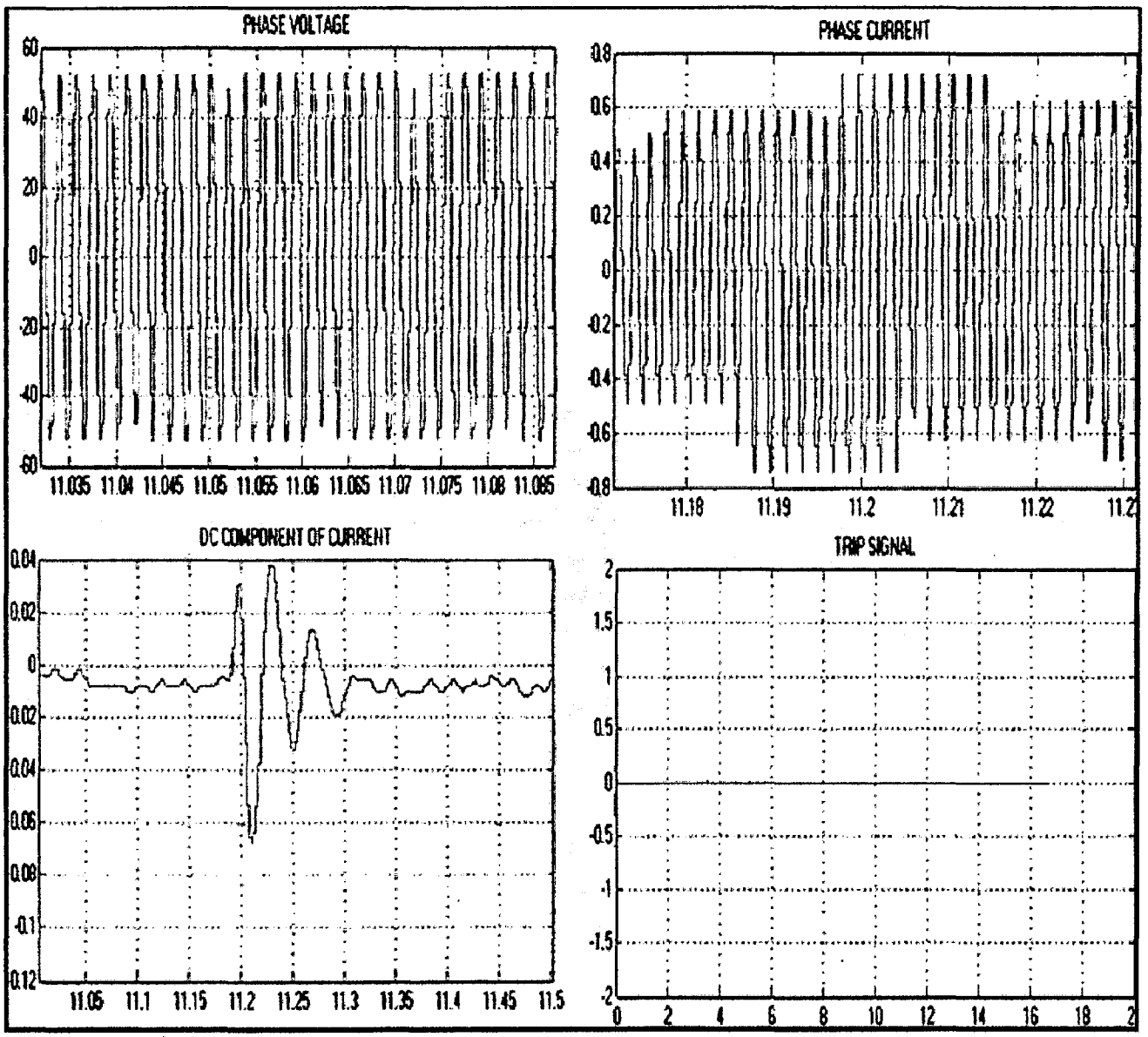


Figure 5.6 Results of Fault after the Capacitor (Real Time Simulation)

As per the description in section 2.5, figure 5.7 shows the case no. 3 i.e. fault is in second zone but looked as if it is in zone one so relay issued a conventional trip signal but since it is after the capacitor the first zone is blocked by adaptive trip signal, so the final trip decision is false.

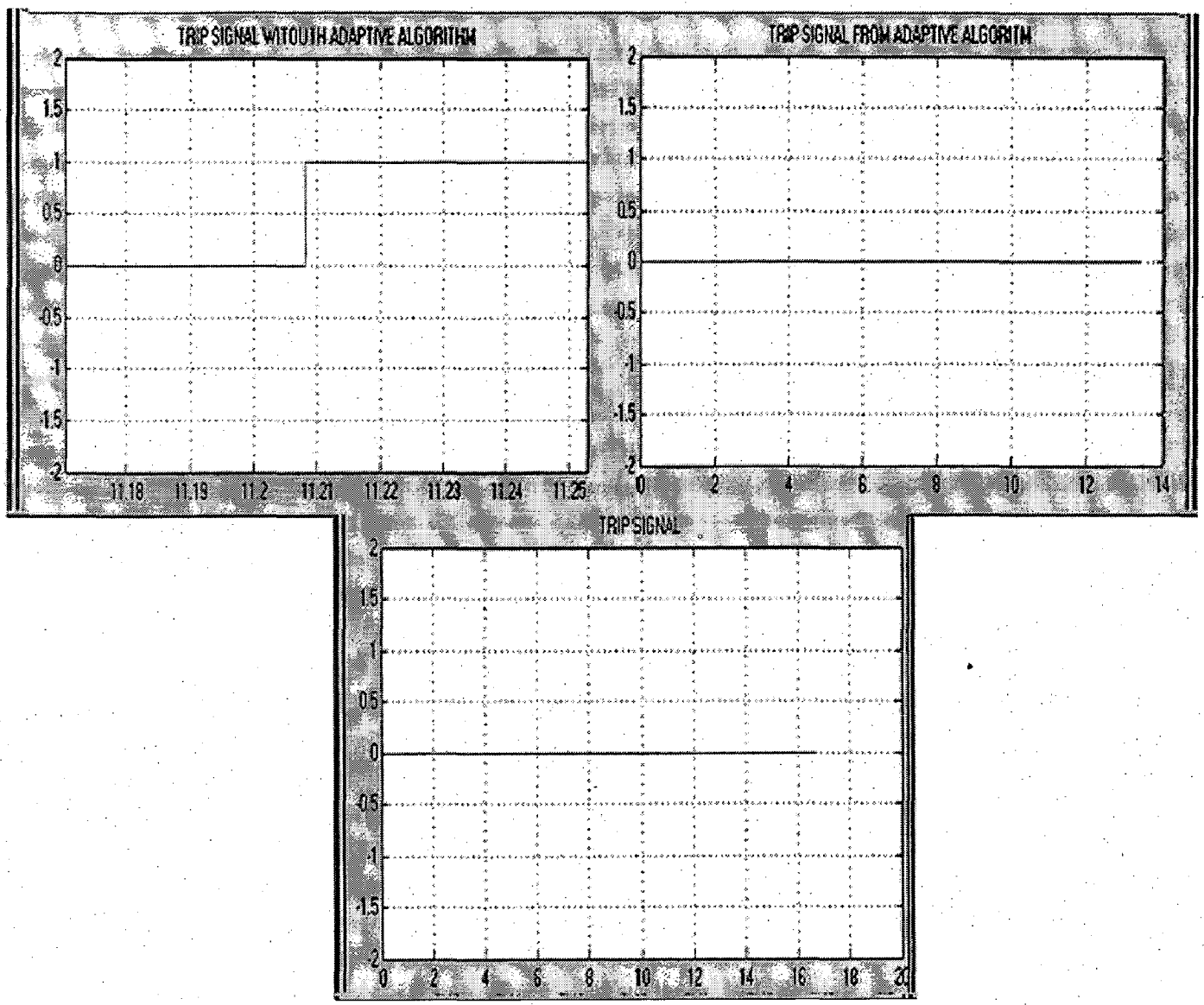


Figure 5.7 Conventional, Adaptive and Final trip signal (For fault after the capacitor)

Figure 5.8 to 5.11 shows the of matlab/Simulink simulation results. It includes phase voltage, phase current, DC component of fault current, and the trip signal status.

Figure 5.8 shows the results for the fault just before the series capacitor. The description for the result is exactly same as that for the real time system described in the previous pages.

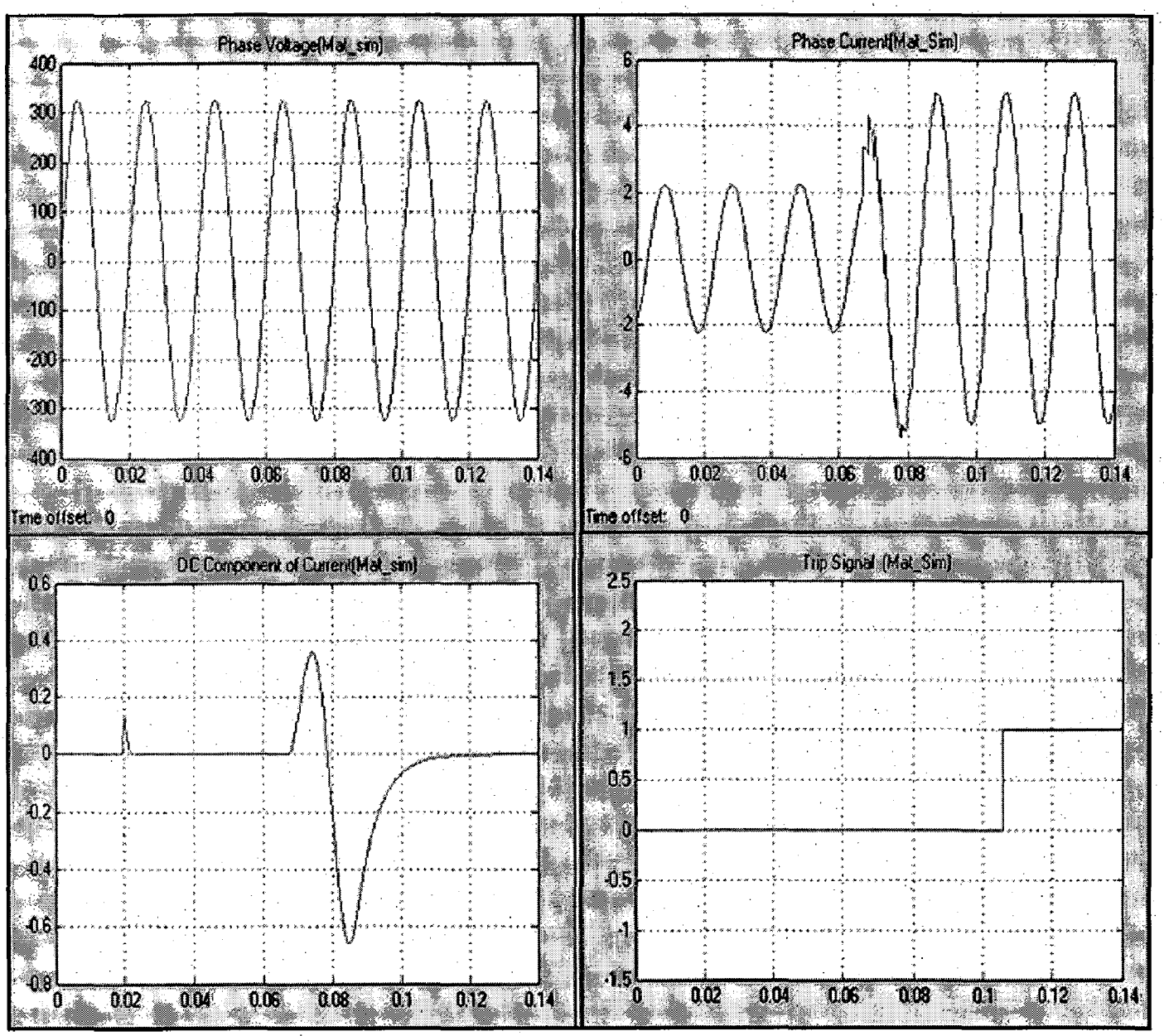


Figure 5.8 Results of Fault before the Capacitor (Matlab Simulation)

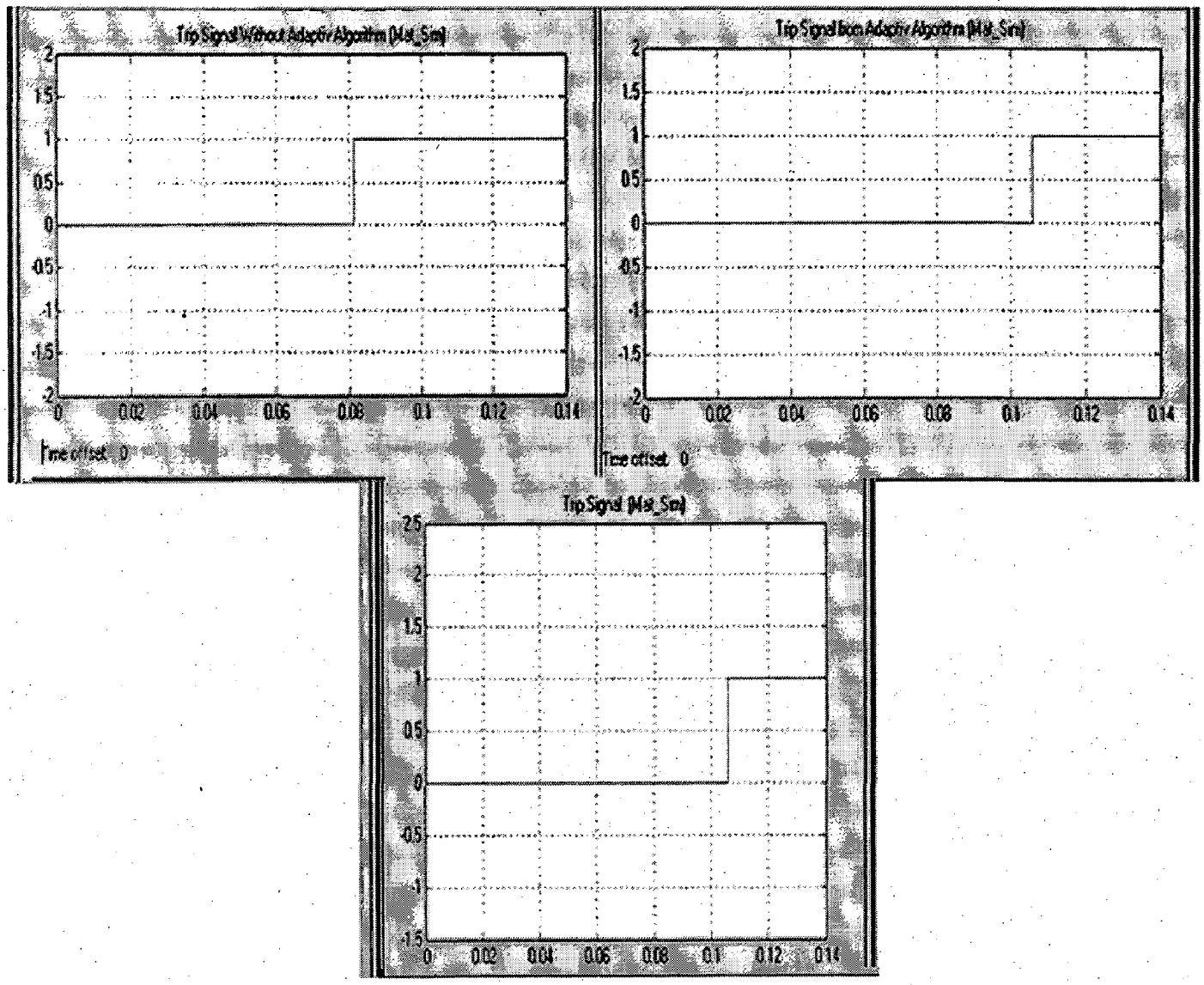


Figure 5.9 Conventional, Adaptive and Final trip signal
(For fault before the capacitor)

Figure 5.10 shows the details for the fault just after the series capacitor

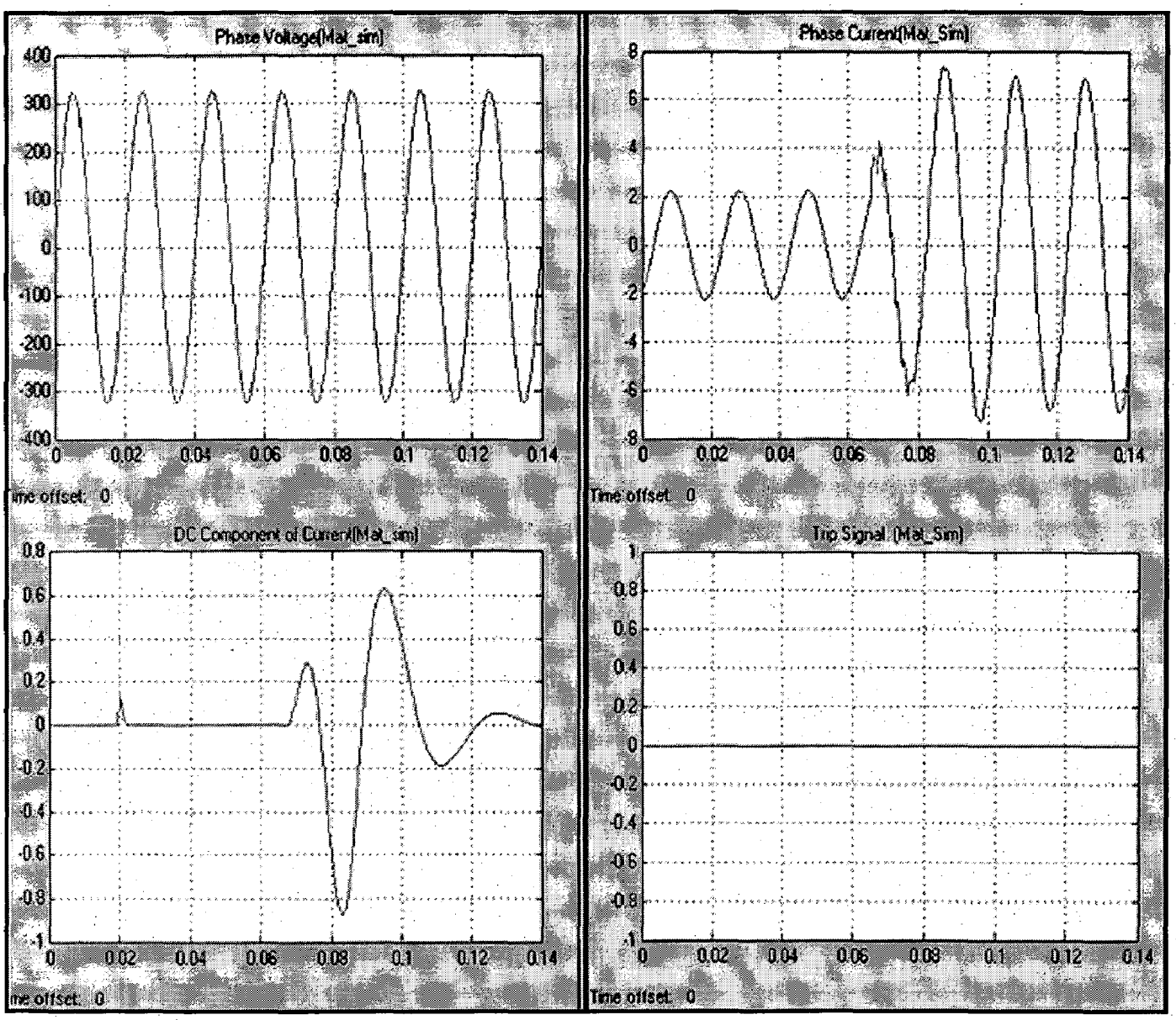


Figure 5.10 Results of Fault after the Capacitor (Matlab Simulation)

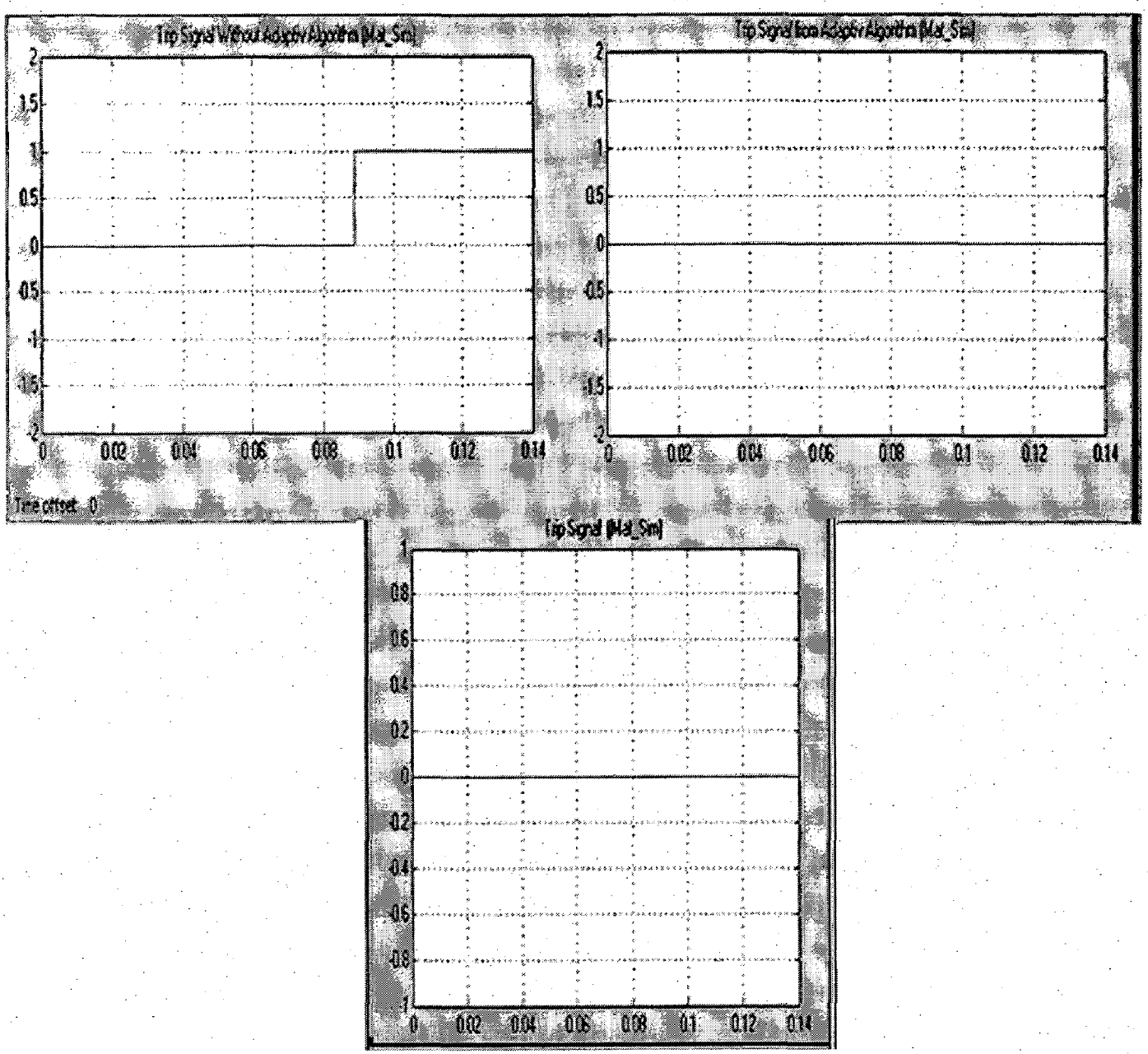


Figure 5.11 Conventional, Adaptive and Final trip signal

(For fault after the capacitor)

Table 5.1 details the time taken for series capacitor location detection at different fault inception angles.

Table 5.1 Zero Crossing Time Analysis of Different Fault Conditions

Fault inception Angle [degree]	**Fault inception Time [sec.]**	**Time for first zero crossing [sec.] after fault inception**		**Time for second zero crossing [sec.] after fault inception**		**Time taken to cross second zero [Millisecond] for fault after capacitor**
		Before Capacitor	After Capacitor	Before Capacitor	After Capacitor	
	tx				ty	t =ty -tx
0	**0.5000**	**0.708**	**0.514**	**Inf(very large)**	**0.5300**	**30.00**
15	**0.5008**	**0.6255**	**0.5146**	**Inf**	**0.5296**	**28.8**
30	**0.5017**	**0.6255**	**0.5145**	**Inf**	**0.5298**	**28.15**
45	**0.5025**	**0.6125**	**0.5140**	**Inf**	**0.5300**	**27.50**
60	**0.5033**	**0.600**	**0.5145**	**Inf**	**0.5295**	**15.00**
75	**0.5041**	**0.585**	**0.5153**	**Inf**	**0.5291**	**13.8**
90	**0.5050**	**0.5238**	**0.5140**	**Inf**	**0.5313**	**26.30**
120	**0.5066**	**0.5958**	**0.5109**	**Inf**	**0.5247**	**18.00**
150	**0.5083**	**0.5970**	**0.511**	**Inf**	**0.5245**	**13.5**
180	**0.5100**	**0.717**	**0.5230**	**Inf**	**0.5399**	**29.9**

5.2 Circuit Breaker Failure Backup Result:

Figure 5.12 represents the condition of healthy circuit breaker. So when fault occurred the relay issued the trips signal which tripped the circuit breaker and hence the current becomes zero. In this case relay does not need to send any signal to the upstream breaker as explained in section 2.7

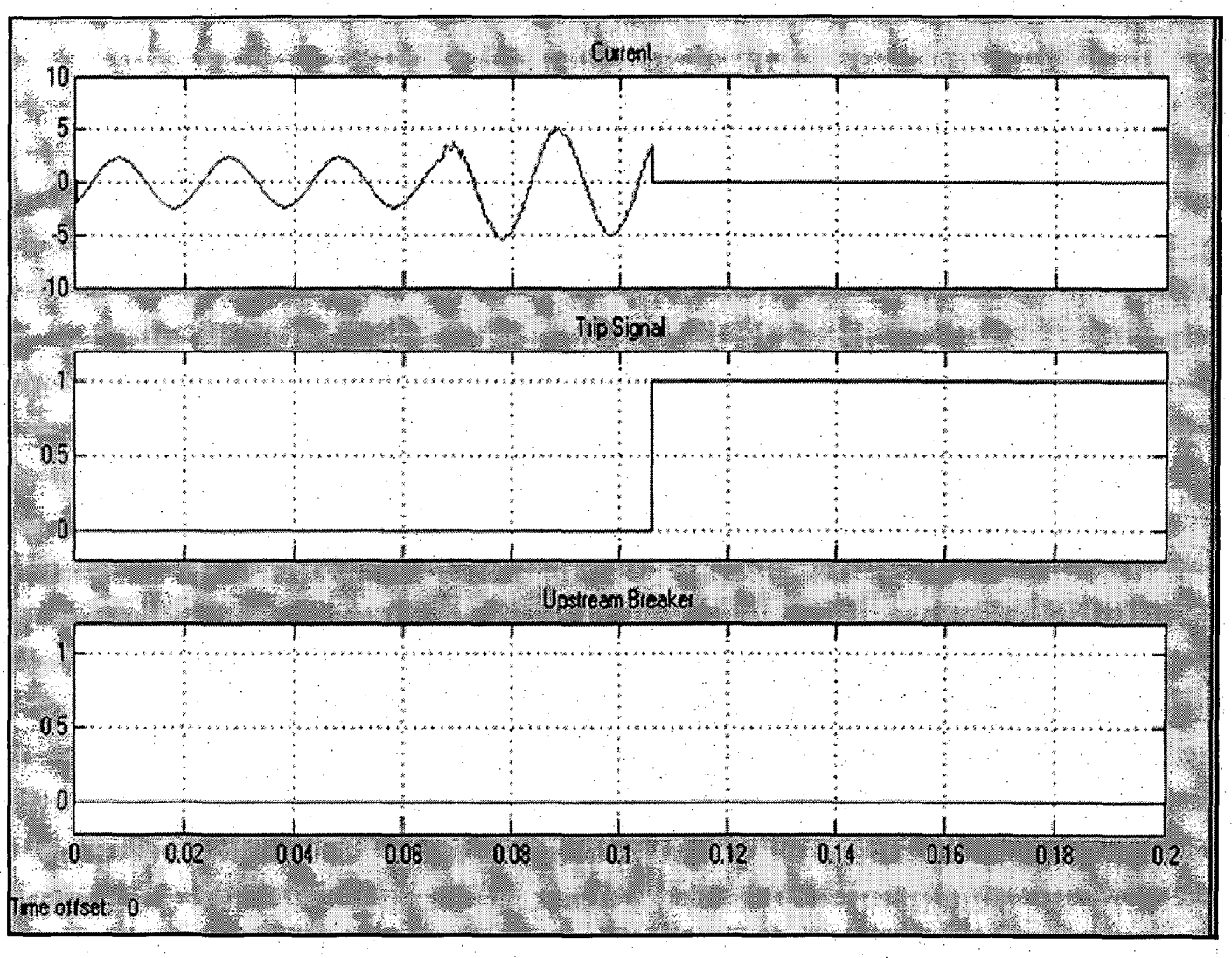


Figure 5.12 Relay Trip Signal to Main and Upstream CB in Healthy Circuit Breaker Condition

Figure 5.13 represents the condition of faulty circuit breaker. So when fault occurred the relay issued the trips signal but it didn't tripped the circuit breaker and hence the current continues to be of the fault level. In this case relay need to send a trip signal to the upstream breaker. End user can define the period after which he wills the trip signal to be issued to the upstream CB, in case of main breaker failure. In the presented simulation it has been taken as 0.2046 sec.

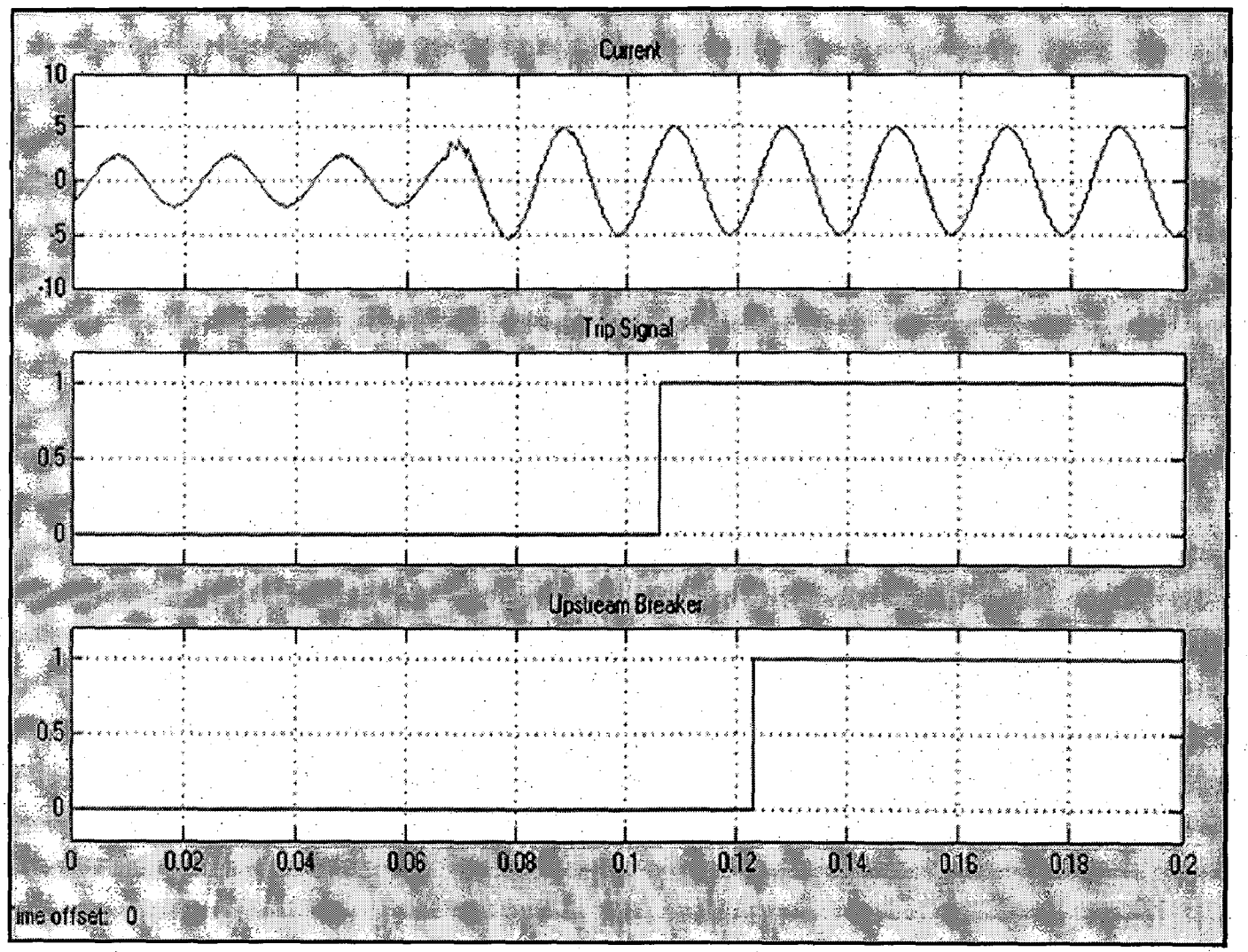


Figure 5.13 Relay trip signal to Main and Upstream CB in Faulty Circuit Breaker Condition

5.3 Result of Voltage Memory Action Scheme:

Figure 5.14 shows the plot for voltage memory action, when the voltage and frequency of the input signal satisfy the criteria set in section 2.8 voltage memory action is enabled. And the memorized voltage is used for impedance calculation. Here the memorized voltage has been retained for 2 sec. But it can be set by the end user as per the requirement.

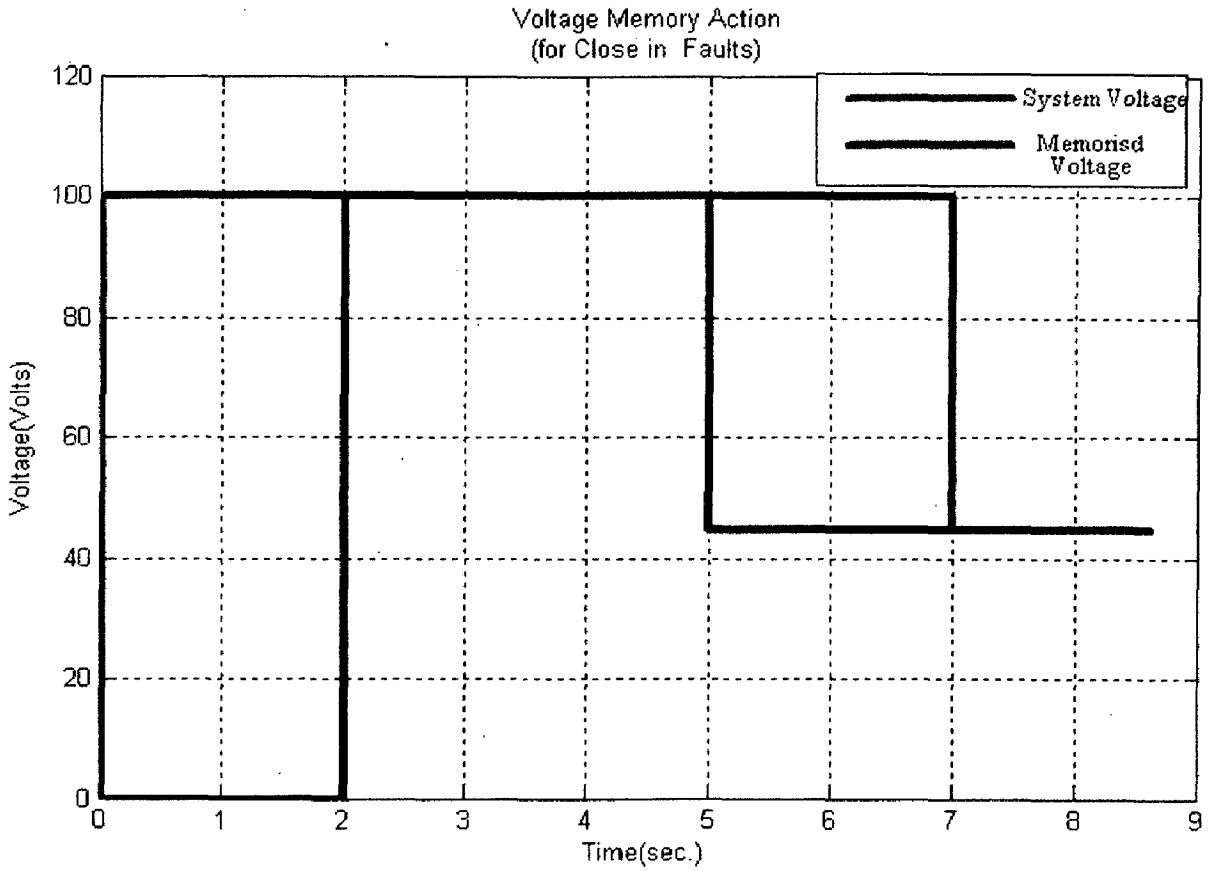


Figure 5.14 Plot for Voltage Memory Action

CHAPTER 6
DISCUSSION OF RESULTS, CONCLUSION AND FUTURE SCOPE

6.1 Discussion of Results and Conclusion

The adaptive distance relay has been developed which along with conventional functions takes care of installation of series capacitor, circuit breaker failure backup and close in faults. The results of various protections has been plotted and tabulated in the previous chapter. There is some differences in the real time and Matlab simulation which is because of well distribution of transmission line parameters and ideal components in Matlab simulation whereas it is lumped and practical in the case of real time simulation. But the overall adaptiveness of the relay for the presented problems is reasonably same.

The presented algorithm for discriminating the fault before and after the capacitor takes less than two cycles for detecting the fault and issuing a trip signal, which is maximum at the fault inception angle of 0°. It discriminates the fault for almost all the cases of fault inception. Since in the presented real-time setup series capacitor compensation level is only 25%. So it will serve much better in actual transmission line where compensation level is much more than the presented case, even though if later is equipped with MOV.

Circuit breaker failure backup algorithm issued the trip signal to the upstream CB in 0.2046 sec (which was the user specified backup time) in the case of main CB fail. And remain idle in the other case. User can change the time for issuing the trip signal to the upstream circuit breaker so that in future it can cope up with the reduced backup protection time, which may be because of advent of new technology in switchgear and protection.

Voltage memory was enabled when there was a fault in the system and the voltage has been dropped to less than 0.65 times the system voltage with the same power frequency of 50 Hz. The voltage memory was enabled for 2 sec. Time for the memory action in case of close in fault is also user settable.

The Real-Time setup that has been prepared in the Power system laboratory can be used for testing any type of relay (for line protection) with slight modifications and parameters can be set as per the requirement.

6.2 Future Scope

The presented relay has been developed for single phase. In future this can be extended to three phase system which will just need to triplicate the transmission line.

In the laboratory setup fault has been created manually because of which fault inception time cannot be controlled. If it can be made through computer itself, fault inception time could be controlled. And hence more extensive and controlled testing can be performed.

Only three cases have been worked out and simulated in the present work. Still there are lots of problems and threat to the distance protection such as mal-operation of distance relay due to power swing, effect of delta-wye transformer between relay and a fault etc, which needs to be worked out.

Further the Simulink model of the relay can be implemented on a single chip digital signal processor.

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APPENDIX A

SOURCES, TRANSMISSION LINE AND CONTROL CIRCUIT PARAMETER SPECIFICATION

Autotransformer:

0 to 260Volts, 50Hz

10Amps

Air Break Contactor:

Siemens make LBO/k 915III-2

Contact Rating: 25 Amps (cont.)

$$\frac{110/240\ V}{3/7.5kw}\sim$$

$$\frac{415/500\ V}{13.5/15kw}\sim$$

2N/0, 2N/C contacts

Rheostat: 0-75 ohms, 5Amp

Inductor: 0-230V,

20-110mh

15Amp

Variable Load bank: 230V

50Amps

Auxiliary relay:

Energizing quantities, rated values and limits

Rated voltage UN: 12 V DC

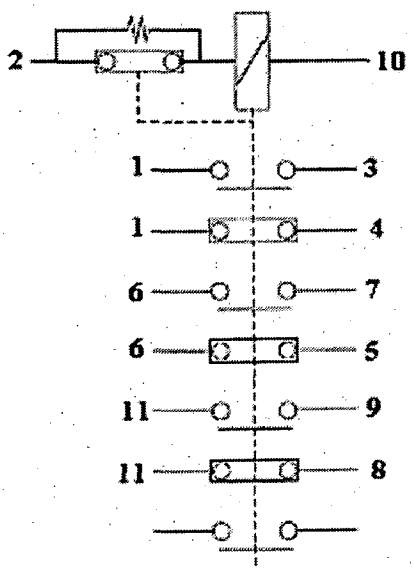
Coil Resistance: 150 Ohms

Operative voltage range: +10%, -20%

Permitted ambient temperature range: 0°C to +55°C

Contact Rating: 5 Amps (cont.)

Contact Connection:



4NO + 3NC

DC Relay: Sc5-s-dc06v

Coil: 06 vdc

Main contact: 7amps, 300V AC, 50 Hz

Appendix B
SPECIFICATIONS OF THE BNC-2120 CONNECTOR

Specifications

This appendix lists the specifications of the BNC-2120. These specifications are typical at 25 °C unless otherwise specified.

Analog Input

Number of channels (default) .....8 differential

Optional inputs

AI 0 .....Temperature sensor

AI 1 .....Thermocouple

AI 3, AI 11 .....Resistor measurement (requires RSE configuration)

Optional connections

Thermocouple .....Uncompensated miniature connector, mates with 2-prong miniature or subminiature connector

Resistor measurement range .....100 Ω to 1 MΩ

Resistor measurement error .....≤5%

Switches

Floating source/grounded source 8

BNC/temperature reference IC 1

BNC/thermocouple connector.....1

BNC/resistor screw terminals.....1

Analog Output

Field connection.....2 BNC connectors

Digital Input/output

Screw terminals.....9 positions, 28–16 AWG wire

LED state indicators.....8, 1 each for lines P0.<0..7>

Protection (DC max V)

Powered off .....±5.5 V

Powered on.....+10/–5 V

Drive

V_{ol} .....0.6 V, 8 mA

1.6 V, 24 mA

V_{oh} .....4.4 V, 8 mA

4 V, 13 mA

Function Generator

Square wave .....TTL-compatible

Frequency range.....100 Hz to 1 MHz

Frequency adjust .....Through the Frequency Adjust knob

Rise time .....250 ns

Fall time .....50 ns

Sine/triangle wave

Frequency range.....100 Hz to 1 MHz

Frequency adjust .....Through the Frequency Adjust knob

Amplitude range .....60 mV_{p-p} to 4.4 V_{p-p}

Amplitude adjust.....Through the Amplitude Adjust knob

Comparison.....Triangle wave is approximately 2 times the sine wave output 4.4 Vp-p maximum

Output impedance .....600 Ω

Timing Input/output

Screw terminals.....14 positions, 28–16 AWG wire

BNC connector .....1, for PFI 0/AI START TRIG

Protection (DC max V)

Powered off .....±1.7 V

Powered on.....+6.7/–1.7 V

Power Requirement

+5 VDC (±5%) .....200 mA

Appendix C

SPECIFICATIONS OF THE NI-6024E DAQ

This appendix lists the specifications of 6024E board. These specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels ..... 16 single-ended or 8 differential (software-selectable per channel)

Type of ADC..... Successive approximation

Resolution ..... 12 bits, 1 in 4,096

Sampling rate ..... 200 kS/s guaranteed

Input signal ranges..... Bipolar only

Gain	Input Range
0.5	–10 to +10 V
1.0	–5 to +5 V
10.0	–500 to +500 mV
100.0	–50 to +50 mV

Input coupling .....DC

Max working voltage

(Signal + common mode)..... Each input should remain within ±11 V of ground

Overvoltage protection

Gain	Powered On	Powered Off
ACH<0..15>	±42	±35
AISENSE	±40	±25

FIFO buffer size.....512 S

Data transfers .....DMA, interrupts,

Programmed I/O

DMA modes .....Scatter-gather

(Single transfer, demand transfer)

Configuration memory size .....512 words

Amplifier Characteristics

Input impedance

Normal powered on ..... 100 GW in parallel with 100 pF

Powered off..... 4 kW min

Overload..... 4 kW min

Input bias current..... ±200 pA

Input offset current..... ±100 pA

CMRR (DC to 60 Hz)

Gain 0.5, 1.0..... 85 dB

Gain 10, 100..... 90 dB

Stability

Recommended warm-up time.....15 min.

Offset temperature coefficient

Pregain.....±15 μV/°C

Postgain .....±240 μV/°C

Gain temperature coefficient .....±20 ppm/°C

Output Characteristics

Number of channels.....2 voltage

Resolution.....12 bits, 1 in 4,096

Max update rate

DMA..... 10 kHz, system dependent

Interrupts..... 1 kHz, system dependent

Type of DAC.....Double buffered, multiplying

FIFO buffer size ..... none

Data transfers .....DMA, interrupts, programmed

Voltage Output

Range .....± 10 V

Output coupling .....DC

Output impedance.....0.1 W max

Current drive.....±5 mA max

Protection.....Short-circuit to ground

Power-on state (steady state) .....±200 mV

Dynamic Characteristics

Settling time for full-scale step.....10 µs to ±0.5 LSB accuracy

Slew rate .....10 V/µs

Noise.....200 µVrms, DC to 1 MHz

Stability

Offset temperature coefficient .....±50 µV/°C

Gain temperature coefficient .....±25 ppm/°C

Number of channels

6023E and 6024E..... 8 input/output

Compatibility..... TTL/CMOS

Calibration

Recommended warm-up time ..... 15 minutes

Power Requirement

+5 VDC (±5%)

PUBLICATIONS

1. Manish Kumar and H.O. Gupta, "Adaptive Decision Making Algorithm for Protection of Series Capacitor Compensated Line," The International Conference on Power and Energy Engineering 2011 (ICPEE 2011) and Advanced Materials Research Journal. (Accepted)