A THEORETICAL STUDY OF A TERNARY III-V COMPOUND MIS-FIELD EFFECT DEVICE

A THESIS

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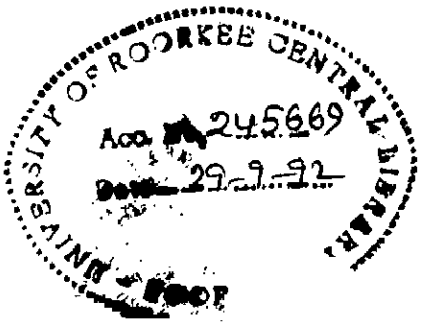

By

RAJ KUMAR SHAR.

DEPARTMENT OF PHYSICS
UNIVERSITY OF ROORKEE
ROORKEE-247 667 (INDIA)

MARCH, 1991

Dedicated

To

My Parents

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled "A THEORETICAL STUDY OF A TERNARY III-V COMPOUND MIS-FIELD EFFECT DEVICE" in fulfilment of the requirement for the award of the Degree of Doctor of Philosophy, submitted in the Department of PHYSICS of the university, is an authentic record of my own work carried out during a period from NOVEMBER 1984 to MARCH 1991 under the supervision of DR. V.K. TONDON, Lecturer, Department of Physics and DR. SANKAR SARKAR, Reader, Department of Electronics and Computer Engineering, University of Roorkee, Roorkee.

The matter embodied in this thesis has not been submitted by me for the award of any other Degree.

RK Sharma

(RAJ KUMAR SHARMA)

This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

Sankar Sarkar

(SANKAR SARKAR)
Reader,
Department of Electronics
and Computer Engineering,
University of Roorkee,
ROORKEE - 247667
INDIA

V.K. Tondon

(V.K. TONDON)
Lecturer,
Department of Physics,
University of Roorkee,
ROORKEE - 247667
INDIA

Date: March 30, 1991.

The Ph.D. Viva-Voce examination of Shri RAJ KUMAR SHARMA, Research Scholar has been held on

Signature of Guides

Signature of External Examiners

ABSTRACT

The growing need for high-speed digital circuits and high-frequency applications are generally met by devices made on high carrier mobility III - V semiconductors such as GaAs, InP, InGaAsP and InGaAs. Considerable attention needs to be focused on the development of III - V compound MIS-technology. In view of the reports that the fabrication of n-channel inversion-mode MISFETs in InP, InGaAsP and InGaAs substrates is a possibility. Experimental investigations show that of these, the InGaAs-based MISFETs are of highest inversion layer mobility and best insulator-semiconductor interface properties. As InGaAs has turned out to be the most useful semiconductor for photodetector applications, InGaAs MISFET is also a competent device for applications such as integrated optics.

An analysis of the properties of inversion layer formed on p-type InGaAs shows that in an inversion-mode InGaAs MIS device an excellent control of surface potential can be achieved by the application of a gate voltage. Onset of strong inversion in InGaAs MIS device requires much lower effective gate voltage than other known MISFET materials. Normal effective field in an inverted InGaAs substrate is relatively higher than in an inverted silicon surface. The effective carrier mobility in an n-type inversion layer in InGaAs is extremely high because of its lower electron effective mass and thicker inversion layer. Furthermore, the lower electron effective mobility in n-inversion layer on InGaAs degrades severely with increase in gate voltage. The analysis shows that this is caused by a high rate of decrease of channel thickness with increase in gate voltage. InGaAs is the ternary limit of the quaternary alloy system of $In_{1-x}Ga_xAs_yP_{1-y}$. Considering the effective mobility in InGaAs MISFET is compared

with that in other members of the quaternary family. In the past, the effective mobility of InGaAsP MISFETs have been reported to be alloy composition dependent. A degradation of effective mobility with increase in gate voltage was also reported. In order to explain these observations, a Matthiessen's rule approach is taken in the present thesis. In the process two factors, namely, the scattering and screening factors have been identified. These factors are dependent on the gate as well as on alloy composition. In agreement with the experimental observations available in literature, the analysis shows that the effective mobility degradation with increase in gate voltage becomes more and more pronounced if the y-composition parameter is increased.

The study of the drain characteristics (drain current-drain voltage characteristics) of the n-channel inversion-mode long-channel InGaAs MISFETs is carried out through the development of an appropriate MISFET-model. The model uses an effective mobility model that has been widely used in silicon MISFET analysis. This mobility expression involves a number of mobility parameters which are generally determined by elaborate laboratory experiments. It has been shown that using the basic MISFET-model developed, the mobility parameters can be approximated with nominal experimental data. The model is then used to study the drain characteristics of InGaAs MISFET. The validity of the model is first checked by comparing the calculated drain characteristics with experimental data available in literature. The MISFET-model is then used to study the effects of substrate doping level on the drain characteristics of an InGaAs MISFET. It is found that for higher doping levels, the saturation drain current and the drain voltage for pinch-off are both lower.

For the sake of comparison, the model is applied to InP and silicon MISFETs. It is observed that the level of operating drain current in InGaAs MISFET is comparatively higher than in InP and silicon MISFETs. A high drain conductance in InGaAs MISFET is also indicated by the study.

The MISFET-model is self-sufficient to give a picture of potential and electric field variation along the channel. It is also capable of determining the distribution of gate induced and drain induced carriers along the channel. It has been shown that these quantities vary in a similar manner as in silicon MISFETs. However, the magnitudes of each of these quantities are higher in InGaAs MISFET. The analysis also considers the variation of effective mobility along the channel. It is shown that effective mobility decreases towards the drain end. This mobility degradation is enhanced by lowering of gate voltage.

In a MISFET the channel carrier concentration is enhanced by impact ionization at high drain voltages and also there is possibility of avalanche breakdown in the p-n junction formed by the drain and substrate. In order to account for the influence of current multiplication by the above two processes, it is necessary to deal with drain breakdown mechanism and its effect on the characteristics of an InGaAs MISFET. The analysis of the drain breakdown mechanism has been carried out in the light of the well established impact ionization theories. To this effect the breakdown parameters for InGaAs and related semiconductors are first analysed. It is shown that for $In_{1-x}Ga_xAs_yP_{1-y}$, the breakdown voltage and breakdown fields are both dependent on the alloy composition parameters. InGaAs, which is the ternary limit

of the quaternary alloy system has the lowest breakdown voltage and breakdown field. The breakdown field in InGaAs is a slowly varying function of the doping level. A most important breakdown parameter is multiplication factor. Two distinct multiplication factors are defined for a MISFET, viz., the channel multiplication factor and drain-diode multiplication factor or substrate multiplication factor. The channel multiplication factor is related to impact ionization in the channel of the MISFET, while the other multiplication factor arises out of avalanche breakdown in the drain-diode at high drain voltage. It has been shown analytically that the channel multiplication factor is controlled by the gate voltage. It decreases with increase in gate voltage. The drain-diode multiplication factor on the other hand is independent of gate voltage.

For the analysis of the influence of impact ionization on the drain characteristics of the InGaAs MISFET, the drain current is assumed to be composed of two components. One of the component is the multiplied channel current and the other is the drain-diode current. The multiplied channel current is obtained by the product of channel multiplication factor and the drain current obtained from the MISFET-model developed. The analysis shows that influence of impact ionization in channel and drain-diode depletion layer on the drain characteristics of an InGaAs MISFET is similar to what has been observed in silicon MISFETs. The analysis also shows that the drain breakdown voltage at which avalanche breakdown occurs either in the channel or drain-diode, increases with increase in gate voltage. Furthermore, the drain breakdown voltage in a silicon MISFET is comparatively lower than that in a comparable InGaAs MISFET.

LIST OF PUBLICATION

(i) R.K. Sharma, S. Sarkar and V.K. Tondon, "Influence of normal field on electron mobility in inverted p-InGaAsP surface", Int. Conf. on Semiconductor Materials, New Delhi, Dec.13-16, 1988.

(ii) R.K. Sharma, S. Sarkar and V.K. Tondon, "A theoretical analysis of inversion mode InGaAsP-MISFETs", Foundation Meeting of the Materials Research Society of India, Hyderabad, Feb.10, 1989.

(iii) R.K. Sharma, S. Sarkar and V.K. Tondon, "An improved Matthiessen's rule based mobility model for MIS-inversion layer", NACONECS-89, Roorkee, Nov.2-4, 1989.

(iv) S. Sarkar, R.K. Sharma and V.K. Tondon, "Gate voltage control of surface potential in inversion mode InGaAsP-MISFETs", Accepted for Publication in Solid-State Electronics.

(v) R.K. Sharma, S. Sarkar and V.K. Tondon, "Modeling inversion mode InGaAs-MISFET", Communicated to IEEE Trans. Electron Devices.

(vi) V.K. Tondon, R.K. Sharma and S. Sarkar, "An analysis of MIS-inversion layer effective mobility", Communicated to J. of Microelectronics.

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R K Sharma

(RAJ KUMAR SHARMA)

CONTENTS

chapter I

1.1 INTRODUCTION

The introduction of the concept of a surface field-effect device dates back to the early 30s, when Lilienfeld and Heil [36,220], independently proposed a device in which current through a thin layer of semiconductor is controlled by a surface electric field. In their field-effect devices, the controlling electric fields were created by the application of a potential drop across an insulator with the semiconductor and metal as the two electrodes. The modern version of these devices are known as the metal-insulator-semiconductor field-effect transistors (MISFETs). This device has two other acronyms, namely, MOSFET (metal-oxide-semiconductor field-effect transistor) and IGFET (insulated-gate field-effect transistor). Although the basic principle of operation of the MISFETs was conceived in the first half of the century, the major break-through in MIS-technology had to wait a long time for the want of a reliable insulator-semiconductor combination. In 1959, Atalla [8] demonstrated that by thermally growing SiO_2 on a Si-surface, a MIS device grade insulator-semiconductor system can be achieved. A year later Kahng and Atalla [114] proposed a Si-SiO_2 MISFET. The device was further developed by Hofstein and Heiman [104]. Thus, silicon MISFET emerged as a potential device for many electronic applications.

The MISFET device essentially consists of a lightly doped silicon substrate into which two lightly doped regions are diffused. These regions are known as the source and the drain. A potential difference between the source and drain makes a majority carrier current conduction through the space between

them. The conducting path between the drain and source is known as the channel. If the carriers in transit through the channel are electrons, the device is an n-channel MISFET. If the current is due to transit of holes between source and the drain, the device is a p-channel MISFET. Hofstein and Heiman [91,104] also demonstrated that the MISFETs can operate in two distinct modes, namely, inversion-mode operation and depletion-mode. In inversion-mode operation, the channel is formed by surface inversion of the semiconductor. In the depletion-mode operation, the channel is provided by the bulk of the semiconductor lying under a surface depletion layer. In either case, a voltage applied at the metal electrode on the insulator surface modulates the channel conductivity, thereby controlling the current. This metallic film is known as the gate of the device. As appreciable surface inversion requires substantive gate voltage, an inversion-mode MISFET does not conduct a significant current at zero or very low gate voltage. Thus, an inversion-mode MISFET is a normally 'off' device. On the other hand, a depletion-mode MISFET operates even at zero gate voltage. Because of this characteristics, a depletion-mode MISFET is categorized as a normally 'on' device.

The pressing need for microminiaturization led to the emergence of integrated circuit (IC) technology. Once again silicon turned out to be the most suitable material as substrate for the IC-chips. SiO_2 proved to be a versatile impurity mask and surface passivation layer for silicon IC-wafers. The common intrests in IC-technology and silicon MIS-technology made the two benefit from the progress of one another. It was soon realized that a MISFET is more compatible with the integrated circuits

than the bipolar and junction field-effect transistors. Comparatively lesser number of processing step and smaller area requirements made the MISFETs to be more convenient for IC-applications. These advantages of MISFETs have made LSIs and VLSIs to be possible. As elements in integrated circuits, the silicon MISFETs found wide applications in semiconductor memories, switching circuits, logic circuits, microprocessors and many other circuits, subsystems and systems. Because of the normally 'off' character, the inversion-mode MISFETs find an ample use in the switching and logic circuits. As speed is of concern in these applications, n-channel inversion-mode MISFETs with high channel carrier mobility are more commonly used.

The trends of microminiaturization and demand for economy and reliability led microwave, millimeter wave and opto-electronics to adopt semoconductor technology. The parameter of primary concern for high-frequency devices is short carrier transit time, while direct and wide bandgap which are of utmost importance for a semiconductor to be useful for opto-electronic applications. Carrier transit time can be shortened to some extent by reducing device dimension. But technological constraints put limit to this technique of transit time reduction. An alternative is the use of a high mobility and high saturation velocity semiconductor. For opto-electronic applications a direct and wide gap semiconductor is essential as it ensures efficient operation in the optical range of the electromagnetic spectrum. Unfortunately, silicon with its fully mature device technology does not quite meet these requirements. Consequently, attention was drawn towards the high electron mobility and wide bandgap III - V compound semiconductors such

as GaAs, InP etc. By mid sixties, several III - V compound semiconductors microwave and opto-electronic devices such as Gunn's, GaAs-IMPATT's, GaAs-varactor's, p-n junction LASER's, PIN photodetector's, avalanche photodetector's and a few other were developed. Side by side with these inventions, more III - V compound semiconductors were found to be useful for opto-electronic and high-frequency applications. Prominent amongst these are InGaAsP, InGaAs, GaAlAs and GaAsP.

The seventies and eighties were marked by advances in low-loss-low-dispersion silica fibre for the 1.0 - 1.7 μm wavelength transmission. Investigations show that wavelength which offers minimum loss extends from 1.3 μm to 1.6 μm region [151]. This opened a new era for communication systems. Systems using silica fibre as transmission line and semiconductor optical sources and detectors began to develop concurrent with these developments the concept of integrated optics also found its place in the communication systems [108]. The implementation of the idea of integrated optics along with the fact that an optical communication signal is usually modulated at microwave frequencies, necessitates the use of a semiconductor that satisfy both bandgap and mobility requirements. The semiconductor that meets these requirements happens to be $In_{1-x}Ga_xAs_yP_{1-y}$ grown on InP under lattice match condition of $y \simeq 2.2\ x$. From its binary limit of InP ($y = 0$) to the ternary limit InGaAs ($y = 1$), the bandgap of the quaternary varies from 1.35 eV to 0.75 eV. Between the same limits the electron mobility of InGaAsP varies from 0.46 to approximately 1.0 $m^2/V\text{-}s$. The most satisfactory feature from the optical fibre communication point of view is the fact that the bandgap range of this alloy system corresponds to a

wavelength range from 0.9 μm to 1.65 μm. Another attractive property of InGaAsP is that it has a direct bandgap over its entire alloy composition range. On the basis of these properties, InGaAsP is finding immense application in optical communication systems, especially as the substrate material for LASER and photodetectors [176]. Investigations also show that of all the possible compositions of the quaternary, InGaAs suits best for photodetectors. From these results it can be safely said that InGaAs is a potential candidate for use as substrate material in an integrated optical receiver. Such an application of InGaAs will be possible, if all the devices comprising a receiver unit can be built in the semiconductor. The recent communication systems make extensive use of digital signal processing. Thus due to the fact that n-channel inversion-mode MISFETs are important components in signal processing circuits, the development of InGaAs-based n-channel inversion-mode MISFETs is of much practical significance.

The success of silicon MIS-technology encouraged scientists and technologists to embark upon the development of III - V compound MIS-technology. Initial efforts were concentrated on GaAs MIS devices. However, these efforts were not rewarded, as high density of interface states pins Fermi level in the lower half of the bandgap. More recently, with the growing importance of $In_{1-x}Ga_xAs_yP_{1-y}$ alloy family for electronic applications, attentions were drawn towards the possibility of fabricating MISFETs on InP, InGaAsP and InGaAs substrates. Ultimately, it was demonstrated that n-channel inversion-mode MISFETs on InP, InGaAsP and InGaAs are possible [65,71,202]. Investigations showed that the InGaAs MISFETs are the most

promising of these devices. Reasonably low interface state density and extremely high field-effect mobility has been reported for n-channel inversion-mode InGaAs MISFETs [65,71].

Notwithstanding the bright prospects that the preliminary investigations suggest for InGaAs MISFET, the technology of this device has yet to earn maturity. Interface state density in SiO_2-InGaAs or Al_2O_3-InGaAs systems vary over the range of 10^{15} - 10^{16} m^{-2} [65,71] as compared with 10^{14} m^{-2} for SiO_2/Si that is achieved with silicon MIS-technology of the present times [220]. Another most menacing disadvantage with the InGaAs MISFETs is the drain current drift caused by the presence of traps in the insulator-semiconductor interfacial layer. However, it may be hoped that with time, these technological hurdles will be overcome and inversion channel InGaAs MISFETs will turn out to be a potential device for many applications, such as G-bit signal processing and integrated optical communication systems.

The development of any device immensely depends on the understanding of its physics. Such an understanding is achieved through theoretical analysis and the modeling of the device. So far most of the work carried out in the area of InGaAs MISFET are laboratory oriented. Very little analysis of the physics of the device has been made. In absence of a strong theoretical background, the laboratory developments of the device relied on the presumption that the silicon MISFET theory is applicable to all other MISFTEs, irrespective of the substrate material. Although some success has been achieved with this approach, the applicability of the existing MIS-theory to the case of InGaAs needs to be thoroughly analysed.

The present thesis analyses and models n-channel inversion-mode InGaAs MISFET in the light of the existing MIS-theory developed with silicon MISFET in view. The theoretical approach presented in the thesis is a study of three fundamental aspects of the device. These are :

1. evaluation of InGaAs as a substrate material for inversion-mode MISFETs,
2. basic device physics that leads to the observed characteristics and
3. the factors governing the limits imposed on the operating current and voltage of the device.

1.2 STATEMENT OF THE PROBLEM

In an inversion-mode MISFET, the substrate material parameters such as the permittivity, intrinsic carrier concentration, carrier effective mass and doping level have profound influence on the behaviour of the channel. The channel behaviour is characterized by several independent parameters. These are surface potential, effective normal field, effective carrier mobility etc. The control of gate voltage on these channel parameters depend to a very great extent on the material parameters of the semiconductor used. The assessment of the suitability of a semiconductor for inversion-mode MISFET applicaton therefore requires an analysis of the channel parameters as functions of the various material parameters. The present thesis meets this objective through the well established MISFET relations which have been successfully applied to the study of the silicon MISFETs. Experimental data as reported in literature show that the effective electron mobility in n-channel

inversion-mode InGaAs MISFET is generally extremely high. In search of explanations for such observations a Matthiessen's rule approach is adopted in the present analysis and the factors governing effective mobility are identified. The influence of the material parameters on these factors is then studied. For a meaningful analysis of the device physics that leads to the observed output characteristics of the n-channel inversion-mode InGaAs MISFTEs, a suitable MISFET-model is developed. The model is used to study the MISFET under various bias conditions. Finally, impact ionization in InGaAs is studied and the analytical results are applied to analyse drain breakdown in n-channel inversion-mode InGaAs MISFET. Thus, the salient features of the study of n-channel inversion-mode InGaAs MISFET may be stated as below :

1. study of InGaAs as a material for n-channel inversion-mode MISFET,
2. analysis of channel field, carrier distribution, channel mobility and drain characteristics (drain current-drain voltage) for an n-channel inversion-mode InGaAs MISFET,
3. study of drain breakdown in n-channel inversion-mode InGaAs MISFET and
4. assessment of performance capabilities of n-channel enhancement-mode InGaAs MISFET on the basis of the above analytical studies.

1.3 ORGANIZATON OF THESIS

The thesis consists of six chapters. First chapter (that is the present chapter) focuses on the objectives, scope and importance of an analytical study of InGaAs MIS field-effect

devices.

The second chapter is a review of the earlier work in the area of III - V compound semiconductor MISFETs. In view of decisive role played by high electron mobility and low interface state density for high-speed applications, a large amount of work has been carried out in search of a suitable material for this purpose. Most of the available informations on III - V compound semiconductor demonstrate that the InGaAs MISFETs are potential devices for meeting high-speed requirements of the modern electronic circuits and systems.

The successful application of a semiconductor in inversion-mode depends upon the influence of normal electic field on inversion layer parameters. The primary parameters which characterize an inversion channel are surface potential, channel charge density and channel carrier mobility. From inversion-mode theory, it is well known that channel properties greatly depend upon material parameters such as bandgap, effective mass and semiconductor permittivity which are composition dependent. Thus InGaAsP MISFETs of differing alloy composition have different channel properties and performance as a device. The third chapter presents a comprehensive theoretical analysis of the behaviour of these parameters of an InGaAsP MIS device. Through this analysis InGaAs is assessed as a material for inversion-mode MISFET.

The performance of MISFET depends on the electric field profile and carrier distribution in the channel. In order to study the internal fields and carrier distribution, a MISFET-model is developed and presented in the fourth chapter of

the thesis. This chapter is thus devoted to the analysis of the characteristics of InGaAs MISFET by the aid of the MISFET-model. In the process a simple method for mobility parameter extraction is also suggested. The dependence of effective carrier mobility on the various parameters of the channel are also analysed in this chapter.

The fifth chapter of the thesis deals with drain breakdown in n-channel inversion-mode InGaAs MISFET. The impact ionization in the channel and in the drain-diode depletion regions are studied with the help of existing theories and relevant experimental data available in the literature. The effect of impact ionization in channel and drain-diode on the drain characteristics are studied. The influence of gate voltage on drain breakdown is also investigated.

A critical examination of all the analytical results obtained is presented in the sixth and final chapter. Important conclusions are drawn and the inferences as well as limitations of n-channel inversion-mode InGaAs MISFET are highlighted. The scope for further work in this area is also discussed.

chapter II

III - V COMPOUND SEMICONDUCTOR MISFETs - A REVIEW

2.1 INTRODUCTION

The growing demand for digital processing at frequencies higher than a few G-bits or more resulted in an interest in developing a high-speed MISFETs. In spite of its highly developed technology the silicon MISFETs fail to meet such requirements owing to limited carrier mobility. In this respect, the III - V compound semiconductor alloy such as GaAs, InP, InGaAsP and InGaAs with high electron mobility, are better candidates for the purpose. Recently, the applications of binary, quaternary and ternary semiconductors have increased manifold and have reached a stage where indium based compounds have emerged as the most important semiconductors. While these materials have already established themselves as materials for various opto-electronic applications (LEDs, APDs and LASERs etc.), some effort have also been made to use them as the basic material for a high-speed MIS-technology.

The aim of this chapter is to present a review of the important developments in the area of III - V compound semiconductor MIS-technology. The review begins with a brief look at the III - V compound semiconductor MIS (or MOS)-technology, its present status and problem. Subsequently the emergence of III - V compound semiconductor MISFETs which derive much of its technology from that of the Si MISFET is discussed. The achievements and failures of this new MIS-technology are all critically reviewed in this chapter.

2.2 III - V COMPOUND SEMICONDUCTOR FOR MIS DEVICES

The utilization of the advantages of a III - V compound semiconductor insulated gate FET to a great extent depends upon the electrical properties of its semiconductor-dielectric interface and the control of drain current drift. Therefore, a thorough understanding and technological control of interfaces between these semiconductors and their native oxides and synthetic dielectric layers are equally important. In III - V compound MISFETs, drift in drain current with applied steady state drain and gate voltage, is the most serious problem that degrades the performance of these devices. This section deals with past studies on interfacial and drain current drift parameters of III - V compound MIS devices.

2.2.1 Semiconductor-Dielectric Interfaces

A MISFET material is required to have high low-field carrier mobility, peak carrier velocity and Γ-L intervalley separation. Besides these, another requirement which is of particular importance for successful MIS application is low surface state densities at the semiconductor-dielectric interafce. III - V semiconductors which satisfy the first three requirements are GaAs, InP and InGaAs. In order to develop a viable III - V semiconductor MIS-technology, the dielectric-semiconductor interface properties of these three semiconductors have been extensively studied.

Chye et al. [35] and Van Laar et al. [236] obtained most reliable data on surface band structure of $In_{1-x}Ga_xAs_yP_{1-y}$

semiconductor on (110) surface cleaved in ultra-high vacuum. The surface with few cleavage steps have a surface Fermi level E_f^* as the same energy level as the bulk Fermi level E_f. They also reported that unlike Si, in $In_{1-x}Ga_xAs_yP_{1-y}$, E_f^* is not pinned by intrinsic surface states. These are located within the valence and conduction bands and not in the bandgap. Duke and Meyer [52] explained the non-existance of intrinsic states in the bandgap by assuming that surface atoms relax forming a distorted tetrahedral environment, the anions move outward and the cations move inward. Theoretical calculations suggest that such a relaxation may force the surface states into the bandgap producing a slight overlap of the respective band edges but these results could not explain satisfactorily pinning of E_f^* within the bandgap.

Extensive X-ray photo-emission (XPS) and ultraviolet photo-emission spectroscopic (UPS) measurements by Spicer et al. [211] indicate that E_f^* is displaced from its bulk position if a fraction of a monolayer of oxygen or metal is adsorbed on the surface of an originally clean, cleaved (110) surface. The steady state position of E_f^* is a specific material parameter. The defect model of Fermi level pinning supposes that defects are created in the surface region of semiconductor when another species is adsorbed upon it, such defects may have energy levels located within the semiconductor bandgap and control the position of E_f^*. It is these extrinsic surface states that play a significant role in determining the surface and interfacial properties of the III - V semiconducting compounds that have special relevance for FET and other devices.

The performance of MISFET is dependent not only on the

semiconductor surface properties but also on semiconductor-insulator interface. In III - V compound semiconductor MIS device, the insulator-semiconductor interfaces are of great technological significance today, since the operation of semiconductor devices and integrated circuits rely upon such interfaces. Therefore, the understanding and technological control of the interfaces between these semiconductors and their native oxides that evolve upon contact with the ambient environment and of synthetic dielectric layers deposited on their surfaces. The native oxides are neither stoichiometric nor spatially homogeneous and are much too conductive to qualify as dielectric layers adequate for MISFETs. However, the native oxide plays an important role in affecting device performance, as they grow quite unintentionally on the surface of the semiconductor.

Homomorphic and heteromorphic dielectric layers on GaAs have been the most extensively investigated III - V compound MIS-structure with the expectation that a suitable dielectric interface will be formed to make GaAs MISFET-technology feasible. Homomorphic layers have been made by Hasegawa et al.[85,86], Hasegawa and Hartnagel [87] with anodic oxidation, Weinreich [250] with microwave plasma oxidation, Sugano and Mori [216] with rf gaseous oxidation and Chang and Sinha [26] with magnetically confined plasma beam oxidation. A large number of investigations were made on anodically oxidized dielectric layers using an aqueous solution of glycol as well as other electrolytes by Weimann and Schlapp [249]. Detailed investigation made by Chang et al.[25] using AES augmented by neutron activation analysis indicates that the free oxide surface is As deficient while the

oxide in the vicinity of the semiconductor interface contains a gradient of excess As that may occupy up to 20 % of the total oxide thickness. Meiners [140] reported that the fast surface states respond to frequencies in excess of 10 MHz.

Heteromorphic MIS-structure on GaAs have been tried by Wilmsen and Szpak [256], Zeisse et al.[267] and Semushkina et al. [196] with a variety of insulators. It was observed that the location of a high density of surface states, near the middle of the GaAs fundamental bandgap, pins the Fermi level. Meiners [140] studied both p- and n-type MIS-structures with homomorphic and heteromorphic dielectric layers. He observed that the position of zero gate bias E_f^* lies between 0.6 and 0.7 eV above the valence band maximum for p-type and between 0.8 and 0.9 eV below the conduction band minimum for n-type GaAs. These observations were made on the basis of C-V and G-V measurements and were in good agreement with XPS measurement of Fermi level pinning on clean GaAs surfaces. The surface state density distribution was U-shaped. The surface potential excursion was limited to 0.45 eV in the lower half of the bandgap with a minimum of 2×10^6 $m^{-2}eV^{-1}$ surface state density which rises to more than 10^{17} $m^{-2}eV^{-1}$ at the zone boundaries. Neither flat-band nor surface inversion could be attained in either p-type or n-type MIS-structures. Meiners [140] also suggested that these properties are independent of deposition procedure for anodic oxide, silicon oxide or silicon nitride dielectric layers.

Lile and Collins [129] pointed out that surface state density is not the only cause which limits GaAs for MIS-structure. The major impediment is the location of the Fermi

level pinning position near the midgap. This results in limited displacement of surface potential which reduces the dynamic range of such MISFETs. Furthermore, these surface state appear to be quite slow, thereby affecting low-frequency response of MIS-structures for more than the high-frequency response. At low-frequencies the surface potential is pinned by filling of the surface traps. It was observed that 1 V change in gate voltage produces a surface potential change of a about 0.45 V at high-frequencies (> 1 kHz), the same gate voltage swing produces a surface potential change of only 0.02 V at low frequencies (≈ 1Hz). C-V measurements showed hysteresis as well as frequency dispersion in GaAs MIS-system [89,209]. Hysteresis seen in C-V curves are consistent with trap filling mechanism and indicate deep depletion for high gate voltage sweep rates. Frequency dispersion in GaAs MIS-system is generally very high [61]. Traps distributed in a metamorphic layer between GaAs and insulator appears to be the cause of much abnormally high-frequency dispersion.

On the whole the available homomorphic and heteromorphic dielectric layers in GaAs MISFET applications are unsatisfactory and most of the GaAs-dielectric interfacial problem remains unanswered. It would be highly desirable to find a more suitable dielectric layer that would eliminate Fermi level pinning near midgap, reduces hysteresis of C-V loops and surface states density by at least one order and preferably two order of magnitude.

The properties of thermally grown oxides (dry oxygen) on InP were investigated by Wager and Wilmsen [245]. They reported

that oxides composed of 70-75 % In_2O_3 and 25-30 % P_2O_5, grow very slowly at temperature below 340 ^0C and rapidly above this temperature. The composition of such oxides differs from that of native oxide. Wilmsen [254] was the first to investigate the properties of InP MIS capacitors with elctrochemically anodized insulating layers. He found that the surface potential can be varied by an applied gate voltage. This is in contrast with MIS capacitors made with sputter deposited SiO_2, which had their Fermi level pinned in accumulation. Probably this was due to a high density of fixed positive density of surface donor centers on the InP substrate. Meiners [141] deposited SiO_2 layers on InP substrates by means of low temperature, rf plasma-assisted chemical vapor deposition (CVD) process. From measured data, Meiners [141] obtained surface state density as a function of energy within the fundamental bandgap. He found that in comparison with n-type, the p-type InP surface is strongly depleted. The equilibrium surface Fermi level E_f^* = 1.12 eV for p-type substrate was much larger than that of the n-type InP (E_f^* = 0.12 eV)[141]. This value is in good agreement with Fermi level pinning at 1.1 eV determined by Spicer et al.[210] using XPS measurements on (110) oriented cleaved InP. It is also in fair agreement with the measurements of Waldrop et al.[247] which were made on (100) oriented native oxide covered p-type InP surface. E_f^* values between 1.2 and 0.9 eV were obtained by Waldrop et al.[247]. Furthermore, from their data it is evident that surface preparation and thermal treatment can affect the position of E_f^* within the bandgap. Similar conclusions have been reached by Brillson and Shapira [22]. They used surface photo voltage and Auger electron spectroscopic measurments to investigate ultra-high vacuum cleaved and chemically treated InP

(110) surfaces.

Fermi level pinning near the conduction band edge of p-type InP allows the displacement of Fermi level over a substantial portion of the bandgap. Inversion of the surface of p-type InP MIS-structure is feasible because the Fermi level is pinned near conduction band minimum in contrast with GaAs MIS-structures. All these measurements [22,141,210,247] demonstrate the presence of a surface acceptor level $E_{as} \simeq 0.5$ eV and a surface donor level $E_{ds} \simeq 0.1$ eV with respect to the conduction band edge of n-type InP. It is also indicated that surface state density distribution is V-shaped within the bandgap of InP. These measurements are also consistent with the theoretical analysis of Dow and Allen [50]. The acceptor center ($E_{as} \simeq 0.5$ eV) is considered to be due to an antisite P_{in} defect and the shallow donor center ($E_{ds} \simeq 0.1$ eV) is attributed to V_p, a phosphorus vacancy. Furthermore,the surface state density near midgap is smaller by approximately one order of magnitude compared to that of GaAs. The above investigations also reveal that, the position of equilibrium E_f^* for zero gate bias is near the conduction band minimum in InP. This is of great significance for MISFET applications.

Wager and Wilmsen [244] investigated the thermodynamics of reactions between the depositing dielectric species and the InP substrate. For deposition temperature in excess of 350 ^{0}C a substantial oxidation of InP coupled with out diffusion of In from the substrate into the SiO_2 was found to occur. This was found to be thermodynamically stable in the presence of InP or its native oxides. While Si and SiO_2 were predicted to reduce the

InP native oxide producing either SiO_2 or a combination of elemental In, P or their suboxides. Wager and Wilmsen [246] reported that rf plasma-assisted growth of SiO_2 profiles indicate the presence of 10 - 25 Å thick native oxide. This is presumed to be primarily $InPO_4$, whose composition appears to be relatively independent of the deposition process. Wager et al.[243] found that the oxide growth rate is a function of the reactor configuration and is greater than the thermal oxidation rate for temperature less than 350 ^{0}C.

More recently, a range of variable bandgap III - V compounds of the form $In_{1-x}Ga_xAs_yP_{1-y}$ has been available. This alloy system can be lattice matched to semi-insulating InP to a high degree of perfection. Shinoda and Kobayashi [202] reported a study of $In_{1-x}Ga_xAs_yP_{1-y}$ interface. The dielectric layer was deposited by CVD technique using aluminium triisopropoxide. They observed that interface state density is compositional dependent. Wieder [252] studied $Ga_{0.47}In_{0.53}As$ dielectric interface and reported that for zero bias, equilibrium surface Fermi level (E_f^* $\simeq$ 0.2 eV). These results are consistent with the Schottky barrier height measurements of Kajiyama et al.[115]. It is also consistent with the barrier height measurements for p-type $Ga_{0.47}In_{0.53}As$ as reported by Veteran et al.[240] and $E_f^* \simeq 0.2$ eV reported by Mullin and Wieder [158]. Based on their theoretical calculations, Allen and Dow [3] predicted that the antisite defect In_{As} produces a donor level $E_{ds} \simeq 0.7$ eV and the antisite defect In_{As} is associated with a donor level $E_{ds} \simeq 0.65$ eV. They calculated density of the surface donor and surface acceptor concentrations for zero gate bias, from C-V and galvanomagnetic measurements. $N_{ds} \simeq 5x10^{16}$ and $N_{as} \simeq 10^{15} m^{-2}$ were obtained.

The value of N_{ds} thus obtained is smaller by more than one order of magnitude and that of N_{as} is smaller by nearly two order of magnitude in comparison with the corresponding values for InP. The Fermi level pinning position within 0.2 eV of the conduction band minimum was obtained for both n-type and p-type $Ga_{0.47}In_{0.53}As$. This is similar to that of InP. The low density of interface state are factors of significance for MISFET applications of InGaAs. Mullin and Wieder [158] reported that low temperature annealing of MIS-structure decreases density of sruface acceptor and allows the displacement of the surface potential over a substantial portion of the bandgap in $Ga_{0.47}In_{0.53}As$ MIS-structure with Al_2O_3 dielectric layers. Similar results were obtained by Kaumanns et al.[117] and Shinoda and Kobayashi [203] for Al_2O_3-$Ga_{0.47}In_{0.53}As$ MIS-system. Interface state density variation within the bandgap is U-shaped. Annealing brodens the minimum and reduces its value by one order of magnitude as compared to that of virgin speciman.

2.2.2 Drain Current Drift

An important requirement of a MISFET operation is that the inversion charge density is time invariant under dc bias condition. In practice, however, most III - V semiconductor MISFETs exhibit a gradual decay in drain current with time, even under dc bias condition. This phenomenon is known as the drain current drift (DCD).

The first discussion of drain current drift was provided by Fritzsche [64]. He interpreted the change in the channel conductivity with time in inversion-mode operation of MISFET in

terms of electron tunneling into traps distributed throughout native oxide. The density of oxide traps was assumed to increase abruptly above a few kT/q of the InP conduction level minimum. This explains the temperature dependence of the drain current drift. Van Staa et al.[238] interpreted their constant capacitance deep level transient spectroscopy (CC DLTS) measurements in terms of spatial and energetic distribution of traps within the native oxide. The traps were assumed to be distributed both spatially and energetically within the InP-bandgap. Electrons from the conduction band were captured by the traps via tunneling while emission occurs by two-stage process involving first tunneling and then a thermally activated transition.

For an Al_2O_3-III - V compound semiconductor system, Okamura and Kobayashi [167,168] proposed a model that indicate one trapping level in the synthetic dielectric Al_2O_3 layer and a second trapping level located in the native oxide. Tunneling into the former is considered the primary transport mechanism with a long time constant and this trap which is located below the Fermi level, is presumed to be insensitive to temperature. The trap in the native oxide is above the Fermi level; it is presumed to be temperature dependent. Thus according to this model, the elimination of the native oxide should reduce the contribution of these traps. These assumptions were confirmed by their experimental data. Using HCl to etch and remove the native oxide prior to the deposition of the synthetic dielectric, they were able to reduce the trap induced instability. Kobayashi et al.[121] reported that by first oxidizing the InP surface and then depositing the Al_2O_3 gate dielectric layer also led to a

reduction in drift.

Lile and Taylor [132] employed drain current drift model [167,168] to analyse their MIS-systems and estimated an activation energy of 16 MeV, which is in good agreement with that obtained by Okamura and Kobayashi [167,168]. Wager et al.[242] carried out an extensive study of dielectric-InP interface. Based on the results of these studies Goodnick et al.[77] developed an analytical model. The model illustrates occurance of thermally activated tunneling of electron within the InP conduction band into an In_2O_3 conducting layer. The layer of In_2O_3 is seperated from the InP by a wider gap $InPO_4$.

Hasegawa and Sawada [88,89] developed an interface state band (ISB) model to account for various dynamic properties of compound semiconductor-insulator interfaces. They suggested the formation of an amorphous, nonstoichiometric layer at the semiconductor surface and the interface states associated with this layer are responsible for many of the anomalous dynamic properties of III - V compound semiconductor MIS devices.

Van Vechten and Wager [239] suggested that in InP MIS devices wafer processing P-vacancies (V_P) are induced near the interface. They concluded that these vacancies are responsible for the observed drift in drain current. It was also pointed out that from one of the four nearest neighbours an In atoms could hop into the V_P, thereby annihilating the V_P. As a consequence a new defect complex consisting of an In vacancy and an antisite defect is created. As electrons are required for each annihilation, electrons are trapped in the process. This loss of

electrons from the channel results in drain current drift. Wilmsen et al.[257] and Geib et al.[73] suggested that traps located within deposited dielectric layers are responsible for drain current drift. Hence insulators or deposition techniques which produce insulators with traps within or near the InP conduction band are not desirable for MIS device applications. Geib et al.[73] studied SiO_2-InP systems. The interfaces were prepared by various techniques. They found no detectable traps in SiO_2-InP system which could cause drain current drift. On this basis SiO_2 seems to be a better choice than Si_3N_4 and Al_2O_3.

Shinoda and Okamura [202,206] reported experimental studies on n-channel InGaAsP MISFETs with Al_2O_3 as dielectric layer. The dielectric was deposited by CVD using aluminium triisopropoxide. The current drift behaviour of the InGaAsP MISFETs exhibited almost the same form as that for InP MISFETs, which has been attributed to channel electron trappings. The dominant trapping centers appears to be located in an InP-native oxide surface layer and in the CVD-Al_2O_3 gate insulator. These studies indicated that it is quite likely that the current drift in InGaAsP MISFETs stems from the same origin as that for InP MISFETs.

Fritzsche et al.[66] were the first to report on the behaviour of $Ga_{0.47}In_{0.53}As$-dielectric interface. Their studies indicated sufficiently low electron trap densities which is in the range of 10^{16} $m^{-2}eV^{-1}$. Fritzsche et al.[65] also reported interfacial properties of $Ga_{0.47}In_{0.53}As$ and CVD-SiO_2 deposited with HCl addition at 310 - 340 ^{0}C. A drain current drift of approximately 15 % was observed for the first 1000 s. This is

less pronounced than in similar InP MISFETs (~ 30 %). Fritzsche et al.[65] attributed this to electron tunneling into interfacial layer. The interface state density near the conduction band edge was found to be negligibly small, while in the bandgap center a high density of donor traps was obtained as in case of InP MIS-system. Gardner et al.[71] also studied drain current drift in n-channel $Ga_{0.47}In_{0.53}As$ MISFETs which were fabricated by using low temperature deposited SiO_2. They observed annealing in hydrogen at 300 ^0C for several hours substantially improves the interface properties. Interface state densities of about 5 - $7x10^{14}$ $m^{-2}eV^{-1}$ were measured near flat-bands. The fixed oxide charge density was $4x10^{14}$ m^{-2} . The 1 MHz C-V curve had a clockwise hysteresis at room temperature of about 0.6 V. They developed non-self-aligned gate MESFETs in which anomalous inversion layer was found with negative gate bias. The drain current drifts with time and the drain current-time curve indicates that there are possibly three time constants involved. This agrees with the model of Shinoda and Kobayashi [205] in which there is a donor trap below the Fermi level in addition to the two acceptor like traps above the Fermi level. They also suggested that some of the drain current instabilities may be due to charge injection, trapping and space charge buildup within a leaky dielectric. Furthermore, the ion-implanted self-aligned gate MISFETs showed minimum (less than 2 %) drift in drain current and insignificant anomalous inversion layer formation, giving very encouraging results. The reason for the dramatic improvement in drain current drift for the ion-implanted self-aligned gate devices are not as yet understood. This requires further study to elucidate the mechanism involved.

Selders and Beneking [195] reported the drift behaviour of GaInAs n-channel inversion-mode MISFETs with CVD-SiO_2 gate dielectric layer. They observed that rapid thermal cycle with a maximum temperature of 700 ^{0}C reduces the short-term drift, for times up to 10 s. The instabilities for the time region 10 and 10^4 s are not affected by the annealing step. A reduction of the oxide deposition temperature down to 250 ^{0}C results in improved stability with only 5 % reduction in drain current after 10^4 s of operation. Splettstosser and Beneking [214] dealt with an observed increase in drain current in n-channel inversion-mode GaInAs MISFET at negative gate bias. They were of the opinion that the increase of drain current for a negative gate bias could be caused by the omission of electrons from donor like traps located in the residual native oxide. Due to increase of positive charge at the interface, the drain current increases. For a positive applied bias, traps at interface are filled with electrons. This leads to a decrease of positive charges at the interface, and consequently drain current decreases. From the shift in threshold voltage a total saturated captured charge at the interface of 10^{15} m^{-2} after 10^5 s was estimated.

Thus for III - V compound MISFETs, large number of models have been discussed to explain drift in drain current. Briefly speaking, it is possibly due to native oxide, distributed traps, discrete traps and traps in insulating layer. The native oxide which is present at the semiconductor-insulator interface, may have been intentionally formed but more often results from the unintentional growth during device processing. There is no general agreement whether a native oxide is an advantage or a liablity. Pande and Gutierrez [171] suggest that native oxide

improves device performance, at the same time Okamura and Kobayashi [167,168] eliminate the native oxide to improve device performance. Therefore, at this stage of III - V compound MISFET development, there is no general agreement over the accuracy of the models reported in literature so far. The topic of drain current drift on III - V MIS-structures requires detailed study for better understanding and its elimination.

2.3 III - V SEMICONDUCTOR MIS-TECHNOLOGY

As mentioned earlier, options available for the development of high-speed MISFET technology critically depends on the fundamental surface and interfacial properties of the binary,quaternary and ternary III - V compounds. The basic interface requirements are that it must be possible to accumulate electrons at the interface, these electrons must remain in the channel and not be trapped and they must travel with high velocity under the gate and with high mobility in the channel. Considering these important MIS requirements, various alloy and dielectric growth techniques suitable for III - V compound semiconductors have been tried by many authors. This section reviews these activities.

2.3.1 Semi-Insulating Substrates

The prospects for a VLSI device technology based on the properties of III - V compound MISFETs are enahanced by the availability of semi-insulating GaAs and InP substrates. Pruniaux et al.[181] reported Cr-compensated GaAs substrate for MIS device applications. Mullin et al.[157], Antypas [4] and

Henery and Swiggard [93] reported preparation of SI-InP from liquid phase encapsulation Czochralski (LEC) growth using boric oxide as an enacapsulant and Cr as a compensating impurity. Mizuno and Watanabe [154] have shown that Fe-compensated SI-InP has larger resistivity than Cr-doped InP. The SI-substrates are expected to provide isolation between devices on the same chips and such isolation appears adequate for GaAs MSI it is likely to be less than satisfactory for LSI and VLSI unless sidegating between adjacent FETs is eliminated. This interaction between adjacent FET depends on the type, distribution, density and time constant of electron traps in the SI-substrates and on their homogeneity and distribution following post ion-implatation annealing. When SI-GaAs and InP are used as substrate, lattice matched $In_{1-x}Ga_xAs_yP_{1-y}$ alloy can be grown whose bandgap spans the energy range between $0.6 < \lambda < 0.9$ μm on GaAs and $0.95 < \lambda < 1.7$ μm on InP substrates.

2.3.2 Growth of III - V Compound Semiconductors

The development of a device technology requires high quality device grade material. For semiconductors these requirements are more stringent than any other materials. Two important requirements are that the semiconductor must be available in a single crystal form and it should be of high purity. Over the years several methods of growing III - V compound semiconductors have been developed. Full advantage of these techniques are taken for growing semiconductors for the fabrication of III - V compound semiconductor MISFETs. The most commonly used methods are (i) Liquid Phase Epitaxy (LPE) (ii) Vapor Phase Epitaxy (VPE) (iii) Molcular Beam Epitaxy (MBE). The

applications of these methods are briefly discussed in the following paragraphs.

(i) Liquid Phase Epitaxy - LPE growth of GaAs depends for its operation on the fact that the solubilities of As in Ga-rich solution decreases with increase in temperature. LPE growth of GaAs was first reported by Nelson [161] using tipping technique. In this technique growth is initiated by tipping the furnace containing growth tube and contents so that melt covers the substrate and is terminated by tipping the furnace back to its original position. Rupprecht [183] reported dipping technique for LPE growth of GaAs. In this technique, growth is initiated by lowering the holder to immerse the substrate in the solution and is terminated by raising the holder to its original position. These techniques are not suitable for growing multilayer structures. Panish et al.[173] reported multiwell graphite sliding boat arrangement for growing multilayer structure. Antypas and Moon [5], Nahory et al.[168], Sankaran et al.[187,188] and Pollack et al.[180] reported growth of InGaAsP and InGaAs layers on SI-InP substrate. The grown crystals are not delequescent and are chemically stable in the atmosphere. For these compounds surface oxidation is also a lesser problem than that for crystals containing Al. Therefore, complicated structures can be prepared by a two step LPE growth and/or selective etching technique. However, with LPE techniques to growing reproducible InP and InGaAsP alloys having low carrier concentration level (10^{21} m^{-3}) is still an unsolved problem. LPE technique is simple and inexpensive. Its drawbacks include growth problem with InGaAsP alloys for wavelength greater 1.4 μm. Furthermore, non-uniform growth, melt carry over and terrace

formation are some of the problems yet to be solved.

(ii) Vapor Phase Epitaxy - Shaw [199,200] Olson and Zamerowski [169], Genter and Cadoret [74] and Heyen and Balk [95,96] reported growth of GaAs layers by chloride transport technique. The trichloride and hydride processes are both variations of chloride transport system in which Ga is transported in the form of chloride of gallium and reacted with arsenic. The surface morphology of the grown layers is superior to that produced by LPE growth. Sugiyama et al.[217], Enda [57], Hyder [106], Hyder et al.[107], Susa et al.[219] and Vohl et al.[241] reported growth of InP, InGaAsP and InGaAs layers on SI-InP. The process has demonstrated good thickness compositonal uniformity, flexible control of alloy composition and ability to be scaled up for mass production. Its drawbacks include difficulties in growing compounds with Al and Sb contents potential for hillock, haze formation and interfacial decomposition during 'preheat' stage.

Low Pressure Metal Organic Chemical Vapor Deposition - MOCVD growth of GaAs involves the pyrolysis of a vapor phase mixture of arsenic and triethylgallium (TEG) or trimethylgallium (TMG). Free Ga atoms and arsenic molecules thus formed and these components recombine on the substrate surface to form GaAs. Bass and Oliver [13], Manasevit and Simpson [135], Duchemin et al. [51] and Hersee and Duchemin [94] reported growth of GaAs layers by MOCVD. Manasevit and Hess [134], Yoshino et al.[266] and Hirtz et al.[101,102] reported growth of $In_{1-x}Ga_xAs_yP_{1-y}$ layers on SI-InP by metal organic chemical vapor deposition. This deposition process is based on the pyrolysis of alkyls of group

III element in an atmosphere of the hydrides of group V elements, is a widely applied growth technique for the preparation of a wide range of III - V materials and heterostructures such as InAs, InP, InGaAsP and InGaAs on InP. The low pressure growth offers an improved thickness uniformity and compositonal homogeniety in addition to the suppression of autodoping memory effects. This, coupled with the reduction of parasitic decomposition in the gase phase, allows the growth of a high purity and good quality material over a large surface area for growth. Its main drawbacks are the use of toxic gases and relatively slow growth rate.

(iii) Molecular Beam Epitaxy - Cho[32], Cho and Arthur [33] and Wood [261] reported growth of GaAs layers by the impingement of directed, thermal energy atomic or molecular beams on a crystalline surface under ultra-high vacuum conditions. Chang et al.[24], Wood [261], Foxon and Joyce [62] and Cheng et al. [28,29] reported growth of $In_{1-x}Ga_xAs_yP_{1-y}$ layers on SI-InP with special attention to the problems associated with background gas and non-congruent sublimation, interface exchange and strain induced interdiffusion. This growth technique has low temperature and excellent thickness control, expensive ultra-high vacuum requirement and difficulty of growing III - V compounds containing phosphorus.

2.3.3 Ion-Implantation

The most common technique of doping an elemental semiconductor is diffusion of impurity which is a high temperature process. Such a process does not suit a III - V

compound semiconductor as the group V element tends to undergo outdiffusion from the surface of the semiconductor. This results in vacancies and antisite defect near the surface. An useful alternative to high temperature diffusion is the implantation of energetic impurity ions into the semiconductor. In this process a beam of impurity ions is accelerated to kinetic energies ranging from several keV to several MeV and is directed on the surface of the semiconductor. As the impurity atoms enter the crystal, they give up their energy to the lattice by collisions and finally come to rest at some average penetration depth, called the 'projected range' which depends upon impurity and its implantation energy.

The most important application of ion-implantation is in the n- or p-type doping of the material for fabricating semiconductor devices and integrated circuts. N-type doping of GaAs by ion-implantaion can be achieved by doping ions either column VI elements (Se, Te, S) or column IV elements (Si, Sn). Davies et al.[42], Eisen and Welch [54], Eisen et al.[55], Gamo et al.[67] and Inada et al.[109] reported implantaion of Se, Te and S ions in GaAs. For the implantated ions to become electrically active they must occupy substitutional lattice sites, but since GaAs is a binary compound this introduces the extra complication of placing the implanted ions on the correct sublattice. It was observed that for high dose ($\geq 10^{18}$ ions m^{-2}), the implantation of Se, Te and S must be carried out into heated substrates ($\geq$ 150 ^{0}C) for the dopants to be substitutionally located following post-implantation annealing. Sze and Irvin [222], Miyazaki and Mimura [152] and Tandon et al.[227] reported implantation of Si ions in GaAs. Si and Sn impurity atoms behave

in a different manner since in order to act as donor atoms they must occupy gallium sites. Woodcock et al.[262] and Donnelly et al.[49] reported that implantaion of Si^+ at elevated temperatures results in a smaller increase in doping efficiency than is observed for column VI dopants. Woodcock et al.[262] also observed that Sn was found to behave like group VI ions showing substantial increase in electrical actvity after 'hot' implantation.

Nishioka and Ohmachi [163] reported the implantation of Si as n-type dopant in InP. Donnelly and Ferrante [47] and Davies et al.[41] observed good activation of low doses of implanted dopants but activation decreased as the implanted dose is raised above 10^{18} m^{-2}. They also observed that the maximum electron concentration available in InP by implantation are about 2-3 times larger (i.e. 10^{25} m^{-3}) than those obtained in GaAs. The electron mobility in samples implanted at elevated temperatures (200 ^{0}C) is about a factor of 2 higher than those measured in samples implanted at room temperature. Implantation at 200 ^{0}C also gives broadening of electron concentration profile in comparison to that observed for samples implanted at room temperature with 10^{19} m^{-2} doses of silicon. Donnelly and Armiento [46] reported the use of Be as p-type dopant in InP and measurements on Be implanted InP suggest that the diffusion behaviour is similar to that observed in InGaAs and excessive diffusion is observed when Be concentration exceeds $3x10^{24}$ m^{-3}. Law et al.[122] and Donnelly and Armiento [46] reported the use of Be as p-type dopants in GaInAsP and it may be possible to achieve hole concentration as high as $(2 - 3)x10^{24}$ m^{-3}.

Ion-implantation has advantages that it can be done at low temperature, implanted-ions can be blocked by metals or photo resist layers and very shallow doping levels can be achieved by this method. Ion-implantation has the major advantage that precise control of impurity concentration is possible. Since the ion beam current can be measured accurately during implantation, a precise quantity of impurity can be added. The distribution of impurities about the projected range is approximately Gaussion. A uniformly doped region can be created by performing several implantation at different energies. The control over impurity level, along with the impurity of the implant over the wafer surface, make ion-implantation praticularly attractive for the fabrication of integrated circuits.

During ion-implantation in III - V compound alloys, there are chances of lattice damage which results from collision between ions and the lattice atoms. However, most of this damage can be minimized by heating the crystal after ion-implantation. This process is called annealing.

In III - V compound alloys during implantation performed at elevated temperature elements of group V dissociate. In GaAs and InP, substantial vaporization of the As or P can occur at the temperatures required for post-implantation annealing. This dissociation may be prevented or minimized by encapsulating the semiconductor wafer with a suitable material or by maintaining an overpressure of the volatile constituent from the wafer. Harris et al.[82], Foyt et al.[63] and Eisen [53] have used Si_3N_4, SiO_2 and AlN as encapsulants on GaAs. Eisen [53] also suggested that the activation of high-speed of the group VI n-type dopants

(S, Se and Te) has been found to be strongly affacted by the choice and method of deposition of the encapsulating material on GaAs. Donnelly and Hurwitz [48], Gleason et al.[75] and Nishioka and Ohmachi [163] used phosphosilicate glass (PSG), Si_3N_4 and SiO_2 as encapsulants for InP. Shinoda and Kobayashi [202] used CVD-SiO_2 for encapsulation in InGaAsP. Woodall et al.[260] and Doerbeck et al.[44] reported suitable methods for maintaining overpressure to prevent loss of group V constituents during implantation.

The temperature required for post-implantation annealing varies with particular III - V material. Donnelly [45], Eisen and Welch [54] and Eisen et al.[55] reported that annealing temperature for ion-implanted GaAs is usually between 800 and 900 ^0C, although both higher and lower temperature have been used in some special cases. Eisen and Welch [54] and Eisen et al.[55] reported that annealing temperature has been maintained between 700 to 750 ^0C for successful ion-implantation of InP. Law et al.[122] reported that annealing temperature was maintained at 560 ^0C for Be^- implanted GaInAsP.

2.3.4 Dielectric Growth Techniques

The most remarkable features of Si MIS-technology are the fortuitous native oxide (SiO_2) and the electrical properties of the Si/SiO_2 system. An attractive feature of a native oxide-semiconductor system is the homomorphic nature of the interface. Such an interface is free from mismatch and associated trap states. Since the oxidation process results in the formation of a subsurface interface, the contamination problems are avoided

or at least minimized. In view of these advantages, earlier III - V semiconductor MIS-technology relied on the use of native oxides grown by wet anodization, thermal oxidation, plasma anodization and so forth. The native oxides thus grown on III - V semiconductor were studied by Hartnagel [83], Sugano and Mori [216], Hasegawa et al.[85] and Wilmsen and Meiners [255]. Unfortunately, the native oxides of the III - V semiconductors were found to be neither stoichiometric nor spatially homogeneous. Native oxides of GaAs are composed of Ga_2O_3 and As_2O_3 , while those of InP are constituted by In_2O_3 and P_2O_5. Such heterogeneous dielectrics display interfacial polarization due to accumulation of charge at phase boundaries. The III - V native oxides also allow ionic transport and are conductive. Some of these native oxides are highly porous and hygroscopic, which makes them unstable. As a result of these undesirable characterization, the native oxides are not suitable for III - V semiconductor MIS-technology.

An alternative approach of forming a dielectric on III - V semiconductor is deposition of a metal, such as aluminium and subsequently oxidation of the metal is a wet anodization, plasma oxidation or some other technique [15,98,190]. The dielectrics produced by this approach yielded some success. However, these dielectrics are of poor quality and it is difficult to terminate oxidation at the metal-semiconductor interface.

The deposition techniques have given the most successful results so far. Chemical vapor deposition (CVD) has been most widely used for dielectric growth on the III - V compound semiconductors. The most straight forward method of this family

is thermal CVD or pyrolysis where reactive gases are introduced into a heated chamber in which the substrate is located. An important requirement of treating a III - V semiconductor is maintaining a low substrate temperature. This is to avoid loss of group V constituents. This constituent can, however, be avoided by maintaining a group V overpressure. Peters [178] suggested two alternatives, plasma-enhanced and photo-enhanced CVD techniques. These methods rely upon excitation of gas species to enhance the reaction and thus permit lower temperature for growth and to minimize the surface damage by plasma. For such a process it would be desirable to seperate the growth zone from the vicinity of the ionized gas. Woodward et al.[263] used various combinations of SiH_4, N_2, NH_3 and H_2 as reactant gases for Si_3N_4 deposition. For the SiO_2 deposition, tetraethoxysilane (TEOS) vapor was decomposed in an oxygen plasma. Meiners [142] reported indirect plasma-enhanced CVD technique which is convenient and appropriate for low temperature and low energy growth of a variety of dielectrics on III - V semiconductors.

Okamura and Kobayashi [167,168] reported deposition of Al_2O_3 gate insulator on InGaAsP wafer at 350 ^{0}C by conventional CVD technique using alumunium triisopropoxide [$Al(OC_3H_7)_3$] in N_2. Gardner et al.[71] reported deposition of SiO_2 layers on InGaAs by photo stimulated reaction of N_2O and SiH_4 at substrate temperature of 170 ^{0}C. Such a low temperature process minimizes the formation of native oxide on III - V semiconductor surface during SiO_2 deposition. Cameron et al.[23] reported that Al_2O_3 film shows higher dielectric constant both at higher and lower (100 kHz and 10 Hz) freqencies in comparison with SiO_2 and Si_3N_4. On the other hand, Si_3N_4 shows higher resistivity and

breakdown field under optimized conditions for deposition.

2.4 III - V SEMICONDUCTOR MISFETs

As the III - V compound semiconductor MIS-technology developed, several MISFETs, using different III - V compound semiconductors were fabricated. The performance of some of the MISFETs were encouraging, while those of others were frustrating. The profound influence of the technology used and the inherent properties of the substrate material on the performance of these MISFETs were observed. In this section the characteristic behaviour and performance of the various III - V compound MISFETs, as reported in literature are discussed.

2.4.1 GaAs MISFET

Fermi level pinning near midgap and the restricted displacement of the surface potential of GaAs MIS-structures limit the application of GaAs MISFET to depletion-mode devices. Furthermore, the surface states near midgap have a time constant in exeess of 0.1 s and, consequently, a sharp reduction in the transconductance of such transistors at low-frequencies is observed. At higher frequencies where the surface states fail to follow the gate potential, the transconductance of a GaAs MISFET becomes comparable to that of GaAs MESFETs of the same geometrical aspect ratio.

The first report on GaAs MISFET appeared in 1965, when Becke et al.[16] reported n-channel depletion-mode MISFET using CVD-SiO_2 as the gate insulating layer. The device exhibited

transconductance (g_m) of 16 mS/mm and effective channel mobility of 0.0178 m^2/V-s. The high value of surface state density N_{ss} in excess of 10^{16} $m^{-2}eV^{-1}$ prevented the operation of the enhancement-mode device and also led to an increasing value of g_m with frequency in the depletion structures. Charlson and Weng [27] were next to report thin film GaAs MIS transistor in 1968. Ito and Sakai [112] reported development of an inversion-mode GaAs MISFET exhibiting a channel mobility of 0.224 m^2/V-s with low-frequency transconductance showing a variety of anomalies. A MISFET structure with gate dielectric made by the thermal oxidation of GaAs in As_2O_3 vapor was reported by Takagi et al. [223]. He used an n-type epilayer grown on semi-insulating substrate to fabricate a D-MISFET which had a low-frequency transconductance 1 mS. Lile et al.[128,131] used epitaxially grown GaAs layers to make D-MISFET. To obtain a gate oxide, they used electrochemical anodization of GaAs surface. This process is similar to one described by Hasegawa [85]. The device showed a high density of surface states $\simeq 10^{16}$ $m^{-2}eV^{-1}$ with a continum of time constants. These states do not respond to frequencies above 1 GHz and thus do not affect microwave power gain.

Mimura et al.[150] used a low temperature plasma oxidation of GaAs to obtain gate dielectric layers for D- and E-MISFETs. In D-MISFET, the surface state density rises from a minimum of 2×10^{16} $m^{-2}eV^{-1}$ near midgap to extremely large values $\simeq 10^{18}$ $m^{-2}eV^{-1}$ near the band edge. These results indicated that even at their minimum, the surface state densities are an order of magnitude larger than those acceptable for MISFET applications. For these devices the transconductance degraded due to surface state trapping. It was observed that at frequencies in

the range of 100 Hz, the GaAs surface operates in deep depletion. Under this condition, relatively few surface states were presumed to interact with the excitational signal. At dc, however, all the surface states were found to respond to the excitation and the transconductance becomes negligible. These characteristics appear to be a fundamental property of the GaAs-oxide interfaces. For the E-MISFET, the field-effect mobility and transconductance were 0.32 $m^2/V\text{-}s$ and 55 mS respectively.

Ito and Sakai [112] and Miyazaki et al.[153] reported that inversion condition on GaAs-insulator interface could not be achieved for satisfactory device operation. This is due to the fact that n-type GaAs surface is possessed of a quiescent surface potential nearby 0.85 eV and very high density of surface states, which is more than 10^{16} $m^{-2}eV^{-1}$. An attempt to drive the surface into inversion is thwarted not only by the large surface state density but also because the surface potential must be initially moved through 0.8 eV to achieve the onset of strong inversion. The use of high-frequencies to incapacitate the surface traps is precluded in the inversion range of operation because of the decreased response time of traps close to the conduction band edge. A different technique was employed by Mimura et al.[150] and Yokoyama et al.[265] to make enhancement/depletion (E/D), all enhancement (E/E) MISFETs and integrated circuits. The enhancement MISFETs were made by using a recessed gate structure that was thin enough so that the depletion region penetrated the entire channel and positive gate voltage was required to induce channel conduction. MISFETs with gate length of 1.5 μm had a power gain of 3 dB at 10 GHz. Mimura and Fukuta [149] combined E/D-MISFETs to make integrated circuit inverters. They observed

that at 1 kHz a large hysteresis occurs in characteristics. The hysteresis disappeared when the inverter was driven by a 25 kHz triangular wave. They found that 1.5 μm long gate MISFETs used for integrated circuit E/E logic performed at approximately one quarter the speed of comparable gate length MISFETs but with three to four orders in magnitude lower power dissipation.

The search for alternative methods for producing GaAs MISFETs led Pruniaux et al.[181] to consider the use of compensated, nearly semi-insulating GaAs as a gate insulating layer in the device structure. They found that the surface potential in such a MISFET can be modulated by positive and negative gate voltage and the device showed transconductance of 5 mS for a gate length of 500 μm. Macksey et al.[133] also used similar procedure to fabricate GaAs MISFET with semi-insulating 0.2 μm thick gate dielectric layers. They employed localized ion bombardment with 30 keV Ar^+ ions at the dose of 10^{18} ions m^{-2} for the purpose. They found that such MISFETs had higher gate breakdown voltage and greater ratios of gate breakdown voltage to pinch-off voltage. At high drain voltage, the increased gate breakdown voltage contributed to the achieved high output power and power saturation of such MISFETs. Bhat et al.[17] reported thermal oxidation of n-GaAs under high pressure conditions. The native oxide formed in this fashion is an attractive candidate for GaAs MIS-gate oxide. MIS devices thus obtained gave better results in terms of hysteresis in C-V characteristics, frequency dispersion of the accumulation capacitance, interface state density and fixed oxide charge density.

It is apparent from the results discussed on GaAs that a

vast variety of dielectrics and interfacial treatment have been applied to GaAs with the hope of developing a III - V analogue of Si/SiO_2 system. In large measure these efforts would appear to have led to somewhat disappointing results, suggesting to many groups that the likelihood of low trap density MIS-structures on GaAs was, atleast in the forseable future remote.

2.4.2 InSb MISFET

InSb is very attractive for ultra high-speed transistors because it has very high electron mobility 8.0 $m^2/V\text{-}s$ at room temperature and four times higher peak electron velocity than Si. For InSb, there are few reports on the n-channel operation because of poor processing technology. Shappir et al.[198] reported p-channel transistor using SiO_2 and anodic oxide as gate insulators. They also demonstrated that InSb native oxide grown in boiling water under high pressure conditions, gives good C-V characteristics in comparison to those of conventional thermal oxide, but the electrical characteristics are not satisfactory. Takagi et al.[224] reported InSb MIS-structure using thermally grown oxide as gate insulator. The interface state density was found to be in V-shaped form with the minimum value of less than 10^{16} $m^{-2}eV^{-1}$ and field-effect mobility of holes was 0.03 $m^2/V\text{-}s$ at 77 K. Takashaki et al.[226] reported an improved thermal oxidation method for InSb MIS double gate structure. C-V characteristics showed no hysteresis. Both n-channel and p-channel InSb MISFETs operated successfully. The effective electron mobility was found to be 0.78 $m^2/V\text{-}s$ and for holes, effective mobility was 0.03 $m^2/V\text{-}s$ at 77 K. These mobility values were far from ideal and can be further improved by

optimising the process steps.

2.4.3 InP MISFET

The more favourable dielectric-InP interface properties compared to that of GaAs make depletion-mode and inversion-mode InP MISFETs feasible. Messick [144] and Messick et al.[146] reported fabrication of depletion-mode InP MISFETs using n-type InP layers grown by LPE on Fe-doped semi-insulating InP. They used CVD deposited SiO_2 layers for gate oxide. They observed that microwave power gain, noise figure and maximum power added efficiency are same as those of GaAs MESFETs, while the maximum power output of InP MISFET is greater than that of GaAs MESFET of the same geometery. Lile and Collins [129] reported frequency dispersion of InP D-MISFET with SiO_2-gate dielectric layer. The output voltage was found to be almost constant in the frequency range 0 - 100 kHz. Messick [145] demonstrated properties of D-MISFET in a 5 μm thick LPE-grown epilayer of InP with an electron density of $9x10^{21}$ m^{-3} and mobility of 0.27 $m^2/V-s$. It was also observed that the device has a power gain cutoff frequency of nearly 18 GHz along with a good low-frequency range.

Gardner et al.[70] reported the fabrication and microwave performance of aligned-gate depletion-mode InP MISFET with gate lengths of 1.5 - 1 μm. A power density of 1.26 W/mm gate width with 29.2 % power added efficiency and 5.1 dB of power gain was obtained at 4 GHz. At 12 GHz, a power density of 0.75 W/mm gate width 22 % power added efficiency and 4.4 dB of power gain was achieved. At 18 GHz, a power density of 0.59 W/mm gate width with 15.7 % power added efficiency and 3.1 dB of power gain was

measured. These devices had a power gain of 3 dB at 20 GHz at power density of 0.44 W/mm gate width with 10.7 % efficiency. These promising results coupled with those reported by Armand et al.[6,7] and Tokuda et al.[231] demonstrate the potential of depletion and accumulation-mode InP MISFETs for achieving high power densities at microwave frequencies.

Inversion-mode n-channel InP MISFET (I-MISFET) was first reported by Lile et al.[130]. The device was made of symmetrical source and drain on acceptor doped InP and pyrolytically deposited SiO_x as insulating layer. The transconductance was found to be 10 mS/mm gate width which is nearly 3 times smaller than that of InP D-MISFET having the same geometrical configuration. However, the tranconductance was not frequency dependent in constrast with GaAs MESFETs. The field-effect mobility was only 0.04 m^2/V-s and it was much smaller than bulk mobility. Ferry [58] suggested that low field-effect mobility in InP I-MISFET can be attributed to surface roughness scattering and potential fluctuations at the insulator-InP interface. This might also be a function of interface states density as demonstrated by Dinger [43]. Fritzsche [64] demonstrated that InP I-MISFET can have a considerably larger field-effect mobility. He used an acceptor-doped epilayer-substrate grown by LPE or VPE. The insulator SiO_x was deposited by low temperature pyrolysis of silane in presence of HCl. The field-effect mobility that could be achieved was 0.1 m^2/V-s for (111) and $(1\bar{1}1)$ facets. A much lower field-effect mobility of 0.05 m^2/V-s was achieved in substrates of (100) orientation.

Kawakami and Okamura [118] fabricated inversion-mode

n-channel InP MISFET by using CVD-Al_2O_3 as gate insulator. Sulphur diffusion process was used for formation of source and drain, sulphur diffusion was preferred to minimize low resistance of source and drain as this is helpful for attaining high gain and high-frequency performance in FET. The n-channel inversion-mode device exhibited normally-off behaviour. A maximum dc transconductance of 87 mS/mm and electron inversion layer effective mobility 0.25 m^2/V-s were achieved.

Okamura and Kobayashi [166] reported fabrication and performance of a p-channel inversion-mode InP MISFET. An n-InP wafer was used as the substrate and beryllium was ion-implanted on the InP wafer to make a thin p^+ layer on n-InP. The gate dielectric was CVD-Al_2O_3. A very low surface hole mobility (μ_s) of about $16x10^{-4}$ m^2/V-s was measured. This was very small in comparison to the bulk hole mobility (μ_B) of $150x10^{-4}$ m^2/V-s. Analysis of C-V data revealed, surface state density of nearly 10^{16} $m^{-2}eV^{-1}$ near the valence band edge. Okamura and Kobayashi [166] also improved current drift in InP MISFET by introducing in situ HCl vapor etching technique prior to gate insulator deposition. Ohmachi and Nishioka [165] reported the performance of n-channel ion-implanted InP MISFET fabricated on InP (100) surface. Fe-doped semi-insulating InP and SiO_2 were used as substrate and gate insulator respectively. The interface state density measured by Terman method [229] was $3x10^{16}$ $m^{-2}eV^{-1}$ and transconductance obtained from I_{DS} - V_{DS} characteristics was 80mS/mm. It was also observed that device operated at frequencies as low as 10^{-1} Hz without transconductance degradation with frequency. This is an improvement compared to the device reported by Lile and Collins [129]. This improvement in low-frequency

operation is believed to result from the long average time constant of surface states that enable them to respond to frequencies of 10^{-1} Hz or lower.

Henery et al.[92] reported the performance of n-channel enhancement and depletion-mode InP MISFETs. These were fabricated on the (100) oriented Fe-doped semi-insulating InP wafers. Selenium implantation was used for formation of n-type layers. The gate insulator was Al_2O_3 and this was deposited by electron gun-evaporation technique. The device exhibited transconductance of 7 mS/mm and 12 mS/mm in enhancement and depletion-modes respectively. The device exhibited minimum channel mobility for low dose of selenium ion-implanted in the channel region and mobility increased with increasing selenium ion concentration in the enhancement-mode of operation. The low dose ion-implantation adjusted the threshold voltage for logic circuits. The channel mobilities increased with implantation dose from 0.075 to 0.155 $m^2/V\text{-}s$. The lowest value is assumed to be surface controlled mobility, while the highest value seems to be a combination of surface and bulk mobility. This can be explained by the existence of a buried channel. Low parasitic capacitances were obtained by using semi-insulating substrates and self-alignment techniques. The low parasitic capacitances along with low and adjustable threshold voltage show that these devices are very suitable for low-power high-speed logic applications.

Kobayashi and Hirota [120] fabricated n-channel inversion-mode InP MISFETs employing phosphorus nitride (P_3N_5) as gate insulator which was deposited at 800 ^0C. The film was pyrolytically grown onto InP surface by the use of PH_3 and NH_3

reagents. Therefore, evaporation of phosphorus from InP wafer was small and high temperature migration of phosphorus atoms into the insulator film was also limited. This resulted in lesser thermal damage to InP-surface. The deposited film exhibited ohmic conduction with a breakdown field intensity as high as 10^9 V/m. The measured effective mobility of electrons of the device was 0.1 - 0.164 m^2/V-s.

Shinoda and Kobayashi [204] reported n-channel inversion-mode InP MISFETs which were fabricated on p-InP substrates with (100) orientation and pyrolytic Al_2O_3 gate insulator was deposited at 350 ^{0}C by using $[Al(OC_3H_7)_3]$ as source gas. The InP MISFET exhibited low value of effective mobility (μ_{eff}). They also proposed a physical model for the Al_2O_3-InP interface to account for the observed very low μ_{eff} and almost zero temperature coefficient of μ_{eff}. By taking interface state density distribution and statistically varying surface potential into account, they carried out an analysis which demonstrates the experimental results semi-quantitatively. From comparison of theory and the experimental results, the effective height of the surface potential fluctuation was estimated to be 10 - 20 mV. It was also found that the surface potential fluctuation effect becomes less significant with decrease in surface state density.

Matsui et al.[138] reported fabrication and performance of InP MISFETs with native oxide film interlayed between plasma anodic Al_2O_3 film and InP substrate. They observed that slow trapping of electrons at the interface can be reduced by growing a native oxide film which is thick enough to prevent tunneling. The effective electron mobility was found to be 0.21 - 0.26 m^2/V-s at room temperature. For samples annealed at 350 ^{0}C the

density of states had a minimum of $3x10^{15}$ $m^{-2}eV^{-1}$ and it increased to $6x10^{17}$ $m^{-2}eV^{-1}$ near the conduction band. The characteristics of MIS-diode with interlayed native oxide film showed smaller hysteresis than in a MIS-diode without native oxide. With the presence of native oxide the instability of drain current reduced to less than ± 4 % for the periods from 5 μs to $5x10^{4}$ s. This reduction in drift has a positive impact on the fabrication technology of InP MISFETs. Sawada et al.[191] demonstrated enhancement-mode InP MISFETs with anodic Al_2O_3/native oxide double layer for gate insulator. Presence of this anodic native oxide interlayed between Al_2O_3 and InP greatly improved the device performance. High effective electron mobilities 0.15 - 0.3 m^2/V-s were achieved together with marked reduction of drift in drain current. Such improvements are consistent with the reduction of interface state density. InP MISFET inverters as well as ring oscillators were also fabricated to demonstrate the stability of the circuit at low-frequency and to show the capability of the process employed.

Pande and Nair [172] reported n-channel InP MISFET with SiO_2 gate oxide deposited at low temperatures of 250 - 300 ^{0}C. They used a novel plasma-enhanced chemical vapor deposition technique where the substrate was not directly exposed to the plasma, thereby minimizing radiation damage to both the film and the substrate. The oxide film deposited had resistances greater than 10 Ωm, dielectric constant of 3.95 and breakdown fields greater than $5x10^{8}$ V/m. MIS capacitors showed sharp interfaces with density of states in the range of $5x10^{15}$ $m^{-2}eV^{-1}$. Enhancement-mode MISFETs processed on InP substrates showed no hysteresis and the device channel current at zero gate bias was

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also zero. An effective electron channel mobility of 0.26 m^2/V-s was obtained for the transistors which exhibited a threshold voltage of 0.22 V and transconductance in the range of 40 mS/mm. This high electron mobility data indicates that the device should exhibit high performance for microwave and digital applications.

Hirota et al.[99] demonstrated InP MISFET employing an infra-red lamp annealing technique for post annealing Si ion-implanted InP substrates. The effective electron mobility of the SiO_2-InP MISFET thus fabricated was remarkably temperature dependent. Effective mobility of 1.1 m^2/V-s at 75 K and 0.15 - 0.25 m^2/V-s at room temperature were observed. The temperature dependence of μ_{eff} was explained on the basis of reduction in thermal degradation at the InP surface during the post annealing process. The temperature dependence and high value of μ_{eff} can also be due to improvement in recrystallisation of Si-implanted layer during infra-red lamp annealing. Yamaguchi [264] discussed the thermal degradation of InP surface based on phosphorus which are caused by the evaporation of phosphorus atoms from InP substrates during high temperature treatment. Hirota et al. [99] fabricated MISFET on Fe-doped semi-insulating (100) InP wafers using a photochemical phosphorus nitride (PN) film as a gate insulator. Using the photochemical process, the deposition temperature was reduced to 200 - 300 ^{0}C which improved MISFET characteristics. The device exhibited effective electron mobility of about 0.17 to 0.22 m^2/V-s. Drain current maintained more than 80 % of its initial value after 10^3 s at room temperature. These results are improvements over the results obtained from InP MISFETs using thermally deposited phosphorus nitride gate insulators. These improvements are probably caused by the

reduction of thermal degradation of InP substrate through the application of the photochemical CVD technique. Hirota et al. [100] investigated the surface carrier transport of electrons in inversion-mode InP MISFETs. The devices were fabricated on Fe-doped high resistivity (100) orientation InP substrates and had photochemically deposited phosphorus nitride (PN) film as gate insulators. Experimental investigation indicated that electron mobility depends on temperature as $T^{-(1-1.5)}$ and on induced electron density (N_s) as $N_s^{-1/3}$ for more than $5x10^{15}$ m^{-2} over temperature range of 296 to 100 K. Furthermore, below 60 K and for lower N_s, electron mobility has a different temperature dependence and it dramatically decreases as temperature decreases. In the opinion of Hirota et al.[100] these temperature and induced electron density dependence of electron mobility are probably caused by acoustic phonon scattering in the high temperature region and by the screened Coulomb scattering and Anderson localization of electrons in the low temperature region. The maximum values for effective and field-effect mobilities are about 0.9 and 1.5 m^2/V-s respectively in the above temperature range.

Serreze et al.[197] fabricated and studied InP MISFETs using plasma-deposited amorphous as the gate insulator. This material was selected because it provides low interface state densities of the order of 10^{16} $m^{-2}eV^{-1}$ at the phosphorus-InP interface. The transconductance of a 10 μm channel length enhancement-mode transistors was 10 mS/mm and a channel mobility of 0.18 m^2/V-s was obtained. They also observed that there is drift in drain current with this insulator. The drain current decays by about 50 % after 3 min. at room temperature. The drift

is believed to be due to nearest neighbor hopping of phosphorus vacancies at the InP-insulator interface. Saunier et al.[189] reported millimeter wave power performance of SiO_2-InP MISFET. The combination of high intrinsic transconductance (120 mS/mm), current density (1 A/mm) and gate-source and gate-drain breakdown voltage (35 V) led to a higher power density of 1.8 W/mm and 20 % power added efficiency at 30 GHz.

2.4.4 InGaAsP and InGaAs MISFET

InGaAsP and InGaAs are two very promising semiconductors which exhibits higher electron mobility, drift velocity and superior semiconductor-insulator interface properties than GaAs and InP. Shinoda et al.[206] fabricated n-channel I-MISFETs on p-type $Ga_{0.13}In_{0.87}As_{0.29}P_{0.71}$ which was grown epitaxially on semi-insulating (100) oriented Fe-doped InP. The gate insulator Al_2O_3 was deposited onto $Ga_{0.13}In_{0.87}As_{0.29}P_{0.71}$ wafer at 350 ^0C by CVD technique using aluminium triisopropoxide [$Al(OC_3H_7)_3$]. Hysteresis was observed in slowly increasing drift occuring inside the gate insulator. Because of this slow drift, the pinch-off characteristics seem to be degraded. From the slope of drain conductance-gate voltage curve, the effective mobility was estimated to be 0.26 m^2/V-s. Shinoda and Kobayashi [202] reported the fabrication and performance of n-channel I-MISFET made in the quaternary system of $In_{1-x}Ga_xAs_yP_{1-y}$ with $0 < y < 0.55$. The $In_{1-x}Ga_xAs_yP_{1-y}$ quaternary layers were grown on Fe-doped semi-insulating InP with the lattice matching condition of $y \simeq 2.2\ x$. LPE growth technique was used for the quaternary layer. Silicon was ion-implanted to create a thin n^+ layer which was followed by hydrogen annealing. For gate insulation Al_2O_3 was

deposited by CVD technique that used $[Al(OC_3H_7)_3]$. The device exhibited compositional dependence of effective electron mobility μ_{eff}. μ_{eff} monotonically increased with increasing As molar fraction y, in the range of $0 < y < 0.55$. At room temperature, the highest mobility achieved was 0.23 $m^2/V\text{-}s$. This is higher than that of InP MISFETs. The transconductance was found to increase with As molar fraction for entire gate voltage range. These excellent characteristics of the quaternary and ternary MISFETs were attributed to the lower of surface state densities near the conduction band edge of the quaternary and ternary alloys. The interface state density was estimated to be 10^{16} m^{-2} eV^{-1} in $In_{0.76}Ga_{0.24}As_{0.55}P_{0.45}$ which increased to 10^{17} for InP (y = 0) interface as the y-composition parameter was reduced. Shinoda and Kobayashi [202] also presented an analysis, which includes the effect of interface state density on MISFET characteristics. They explained the experimental results for InP and $In_{1-x}Ga_xAs_yP_{1-y}$ MISFETs satisfactorily. Very large temperature variation in threshold voltage and zero temperature coefficient of μ_{eff} were observed for InP (y = 0) devices. In constrast small temperature variation in threshold voltage and dependence of μ_{eff} on temperature were observed in $In_{1-x}Ga_xAs_yP_{1-y}$ MISFETs.

Wieder et al.[253] demonstrated an n-channel inversion-mode MISFET made in p-type $Ga_{0.47}In_{0.53}As$. An alloy of 20 % Sn and 80 % Au was used to form the source and drain blocking electrodes. SiO_2 layer grown by low temperature plasma-assisted pyrolysis of silane in presence of NO_3 was used as the gate insulator. The transconductance per unit gate width was found to be as 25 - 50 μS and field-effect mobility 0.003 $m^2/V\text{-}s$ was observed. The low transconductance was believed to be

partly due to poor quality of alloyed n-p source and drain junctions and partly due to scattering of electrons at the dielectric-semiconductor interface. Liao et al.[126] described the fabrication and performacnce of n-channel $Ga_{0.47}In_{0.53}As$ MISFET with Si_3N_4 gate insulating layer. They obtained transconductance per unit gate width of 2 mS/mm, which repersents an order of magnitude improvement over the results of Wieder et al.[253]. The effective mobility was found to be 0.0325 m^2/V-s. This low value of mobility believed to be an effect of surface roughness or enhanced scattering at the semiconductor-insulator interface.

Gardner et al.[69,72] reported the microwave performance of $Ga_{0.47}In_{0.53}As$ depletion-mode MISFETs. They used VPE-grown n-type layers on semi-insulating InP as the substrate material. A SiO_2 layer was grown on the n-InGaAs layer to form gate insulator. Employing this technique they reported that a 3 μm long gate gives 4 dB gain at 6 Hz with power output on 57 mW and power added efficiency of 19.7 %. They also carried out capacitance-voltage and conductance-voltage measurements on InGaAs MIS-diodes. These measurements demonstrated interface state densities of $2.5x10^{16}$ to $2x10^{14}$ $m^{-2}eV^{-1}$ from inversion to accumulation and only slight hysteresis. The effective mobility determined to be 0.52 m^2/V-s which is considerably higher than those reported for InP and $Ga_xIn_{1-x}As_yP_{1-y}$ MISFETs. Ishii et al. [110] developed a $Ga_{0.47}In_{0.53}As$ E-MISFET. The ternary layer was grown on (100) oriented SI-InP by LPE. Anodic Al_2O_3/anodic native oxide, double layer was used as the gate insulator. The insulating double layer yielded superior interface property than single layer anodic Al_2O_3, which was in agreement with the

observations of Sawada et al.[190]. The device exhibited effective channel mobility of 0.14 $m^2/V\text{-}s$ and dc transconductance of 0.17 mS/mm. The density of interface state in the double layer structure was $2x10^{17}$ $m^{-2}eV^{-1}$ near the conduction band edge and $8x10^{15}$ $m^{-2}eV^{-1}$ near midgap. It was evident that further optimization of the process would improve the interface properties of $Ga_{0.47}In_{0.53}As$ double layer MIS, and thus FET characteristics.

Liao et al.[127] described the fabrication and operation of an $In_{0.53}Ga_{0.47}As$ p-channel inversion-mode MISFET with plasma grown native oxide as gate insulator and compared its performance with that of Si_3N_4 insulated gate FET. The p-channel structure was chosen because the well established Zn diffusion process could be used for source and drain formation in this type of device. The device exhibits a transconductance 4 mS/mm and effective channel hole mobility 0.0145 - 0.0163 $m^2/V\text{-}s$ which is very close to that of the Si_3N_4 insulated gate MISFET. In Si_3N_4 MISFET the hole mobility was found to be 0.015 $m^2V^{-1}s^{-1}$ by the same method as used for the native oxide insulated gate FET. The effective hole mobilities are 50 % of bulk hole mobilities. Surface roughness of the semiconductor material and enhanced scattering in the very thin inversion layer as commonly observed in Si MISFETs are probably responsible for the observed hole mobility.

Gardner et al.[72] studied the performance of depletion and inversion-mode $Ga_{0.47}In_{0.53}As$ MISFETs. For these MISFETs the gate insulators were formed by CVD grown SiO_2. Lattice matched $Ga_{0.47}In_{0.53}As$ layers were grown on SI-InP by hydride synthesis

technique originally developed by Olsen and Zamerowski [170]. In this way submicrometer n- and p-layers of InGaAs with excellent surface morphology and lattice mismatch less than 0.05 % were grown. In undoped n-layers with carrier concentrations of 10^{21} m^{-3}, electron mobilities of 1.0 and 4.6 m^2/V-s were realized at 300 and 77 K respectively. With 1.5 μm channel length and 600 μm channel width the depletion-mode MISFETs gave 120 mW power with 3.7 dB power gain and 31 % power added efficiency at 6 GHz. At 12 GHz, 100 mW power with 3.4 dB gain and 15 % power added efficiency was obtained from 1 μm channel length device. This is several dB better than that of GaAs MESFETs of similar geometery. Fritzsche et al.[65] fabricated an n-channel inversion-mode MISFET. The InGaAs layer was grown by LPE with low impurity concentration to achieve high inversion mobility. The device showed normal enhancement characteristics with a threshold voltage of -1.5 V. The drain current drift due to electron tunneling into the interfacial layer is nearly 15 % of its initial value for the first 1000 s. This is less pronounced than 30 % drift observed in similar InP MISFETs. For the InGaAs MISFET the interface state density near the conduction band was found to be negligibly small while in the bandgap center a high density of donor traps appeared. The device exhibited a field-effect mobility of 0.25 m^2/V-s and a normalized transconductance of 150 - 200 mS/mm gate width and μm gate length was achieved.

Gardner et al.[71] reported the fabrication and properties of SiO_2-$Ga_{0.47}In_{0.53}As$ MISFETs. $Ga_{0.47}In_{0.53}As$ layers lattice matched to SI and n^+-InP substrates were grown by VPE using hydride synthesis technique. Both n-type (Se-doped) and p-type (Zn-doped) layers with good electrical properties,

excellent surface morphology and good lattice matching were grown. The SiO_2 layers used were deposited by the photostimulated reaction of N_2O and SiH_4 at substrate temperature of 170 ^{0}C. The relatively low substrate temperature of 170 ^{0}C minimized the formation of the native oxide on InGaAs surface during SiO_2 deposition. Anealing in hydrogen at 300 ^{0}C for several hours improved the interface properties. Interface state densities of about 5 - 7x10^{14} $m^{-2}eV^{-1}$ were measured near flat-band. The fixed oxide charge density was found to be 4x10^{14} $m^{-2}eV^{-1}$. For the InGaAs MIS-diodes fabricated by the same process the 1 MHz C-V curve had a clockwise hysteresis of about 0.6 V at room temperature. The initial n-channel inversion-mode devices showed significant drain current drift with time and anomalous inversion layer formation with negative gate bias. By the aid of ion-implanted self-aligned gate technology, n-channel inversion-mode MISFETs showing minimum (less than 2 %) drain current drift and insignificant anomalous inversion layer formation were developed later. These devices exhibited field-effect mobilities as high as 0.52 m^2/V-s. This is the highest inversion-mode field-effect mobility measured in any semiconductor at 300 K. These devices had threshold voltage consistent with the acceptor doping level and measured interfacial parameters. Gardner et al.[68] also reported self-aligned gate GaInAs MISFETs suitable for microwave applications. These devices showed a power density of 49 mW/mm gate width with a drain voltage of 5.5 V, power added efficiencies of 48 and 39 % were obtained at 4 and 8 GHz, respectively. The estimated carrier velocity was 1.7x10^5 m/s in these devices. The InGaAs MISFETs with gate lengths 0.9 µm and oxide thickness of 80 nm exhibited a maximum transconductance of

107 mS/mm , corresponding to a carrier velocity of 2.5×10^5 m/s.

Upadhyayula et al.[235] developed self-aligned gate inversion-mode GaInAs MISFETs. The MISFETs were fabricated on p-type $Ga_{0.47}In_{0.53}As$ epitaxially grown on SI-InP substrates. Using these MISFETs ring oscillator (RO) circuits were designed where enhancement-driver/enhancement-load type large gates were used, propagation delay as low as 50 ps was measured in a nine-stage ring oscillator. An unit of 1.2 μm gate length when operated with supply voltage of 8 V exhibited a minimum propagation delay of 50 ps at 9 mW gate power dissipation. At supply voltage of 2 - 2.5 V, the observed propagation delays were in the range of 250 - 300 ps with power dissipation range of over 0.08 - 0.1 mW. The corresponding delay-dissipation product ranged over 25 - 30 fJ. These results amply demonstrate the suitablity of InGaAs MISFETs for digital applications in microwave range. Selders and Beneking [195] discussed long- and short-term stability of InGaAs MISFETs fabricated on Fe-doped (100) oriented SI-InP with CVD SiO_2 as gate insulator. They showed that by applying, a rapid thermal annealing cycle with a suitable maximum temperature, the number of fast interface states could be reduced. By this means stable device performance in the time range between 1 μs and 10 s can be achieved. However, the drain current drift for longer times is not affected by the annealing step. Furthermore, a reduction of the dielectric deposition temperature down to 250 ^0C results in improved long-term stability with a drain current decrease of only 5 % after 10^4 s of operation at room temperature. Martin et al.[137] studied the performance of InP/InGaAs IGFET which employ a hetrojunction to isolate the channel electrons from the InGaAs-insulator

interface. SiO_2 deposited by plasma enhanced chemical vapor deposition was used for gate insulation. The SiO_2 based device exhibited maximum transconductance of 130 mS/mm and 210 mS/mm at 300 K and 77 K respectively for 1.5 μm gate lengths. Use of SiO_2 as the gate insulator also resulted in extremely high gate-drain breakdown voltage which was in excess of 20 V, with leakage current less than 1 nA at these biases.

Splettstosser and Beneking [214] reported fabrication and performance of $Ga_{0.47}In_{0.53}As$ MISFET, for which $Ga_{0.47}In_{0.53}As$ layers were deposited on semi-insulating InP by metal organic vapor phase epitaxy (MOVPE). The n^+- and n-epilayer doping level were $2x10^{24}$ m^{-3} and 10^{23} m^{-3} respectively. For a gate insulation SiO_2 was deposited by CVD process, using silane and oxygen (SiH_4 to O_2 ratio of about 1) at 250 ^0C. Just before SiO_2 deposition, InGaAs surface was oxidized in H_2O_2 and the native oxide was removed by buffered HF thereafter. A high temperature rapid thermal annealing (700 - 800 ^0C) was used to improve the quality of oxide and the interface. For source and drain contacts, Ti/Pt/Au alloy was deposited. For gate metallization Al was used. The device in enhancement-mode exhibited very high transconductance of 300 and 250 mS/mm for gate lengths of 1.5 and 3 μm respectively. The effective channel mobility was found to be 0.58 m^2/V-s and carrier saturation velocity in the channel turned out to be $3.5x10^5$ m/s. High-frequency measurements performed on 1.5 and 3 μm gate length device resulted in current gain cutoff frequencies of 14 and 6 GHz respectively.

2.5 CONCLUSION

Over the year several binary, quaternary and ternary III - V semiconductors have been developed for various electronic applications. These semiconductors are of wide range of bandgap, electron and hole mobilities, carrier saturation velocities. The review just presented show that GaAs, InP and InGaAs have been extensively studied for exploring a III - V compound semiconductor suitable for MISFET applications. Considering the fact that GaAs has the most advanced technology of all III - V semiconductors, earlier efforts were concentrated on developing a GaAs MIS-technology. However, these efforts were frustrated by Fermi level pinning at the surface. Interest ultimately shifted towards InP and InGaAs for MIS applications. Both materials with acceptor doping exhibit considerable variation of surface potential over the bandgap, which is essential for inversion-mode MISFET operation. The basic parameters which play important roles in governing the performance of a MISFET are interface state density and effective carrier mobility in the channel. While the former should be low, the latter must be as high as possible. The interface state density in InP is of order of 10^{17} $m^{-2}eV^{-1}$ and it is 10^{16} $m^{-2}eV^{-1}$ for InGaAs. The highest electron effective mobility reported for InP MISFET is 0.3 $m^2/V\text{-}s$ which is comparatively much less than 0.58 $m^2/V\text{-}s$ as reported for InGaAs MISFET. Furthermore, drain current drift of the order of 20 % of the intial value after 1000 s as observed in InP MISFET is inferior to 5 % current drift after 10000 s exhibited by an InGaAs MISFET. All these data indicate that InGaAs happens to be the most suitable material for the development of a III - V compound MISFET-technology. The success of the development of a MIS-technology lies in an indepth understanding of the device physics. While efforts have been made to perfect the fabrication

process for inversion-mode InGaAs MISFETs, analysis of the dependence and material parameters is still wanting.

chapter III

ELECTRON MOBILITY IN $In_{1-x}Ga_xAs_yP_{1-y}$ MISFETs

3.1 INTRODUCTION

On the surface of a p-type semiconductor, an n-type inversion layer may be formed by the application of an electric field in a direction normal to the surface. A major application of such an inversion layer is the formation of the conductivity channel of the n-channel inversion-mode MISFETs. In an n-channel inversion-mode MISFET, the normal field is produced by applying a potential drop across an insulator which is either directly deposited or grown on the surface of the semiconductor. To facilitate the application of the voltage drop across the insulator, an electrode, commonly known as the gate electrode is formed on the free surface of the insulator. The normal field thus produced at the semiconductor surface, results in a potential difference between the surface and bulk region of the semiconductor. This potential difference controls the electrical behaviour of the inversion channel and is known as the surface potential.

The parameters which characterize the electrical behaviour of an inversion layer are mainly the surface potential, channel mobility and inversion charge density. All these parameters are in one way or the other related to one another. These relationships are now well established through exhaustive and elaborate theoretical and experimental studies on inversion layers formed in Si/SiO_2 system [20,36,162,184,194,218,220,233]. The theoretical equations are also applicable to MIS-structures made on semiconductors, as they have been successfully applied for the

analysis of some aspects of III - V semiconductor MISFETs [202,204]. However, no detailed analysis of the behaviour of the surface potential and inversion layer parameters of InGaAs MISFETs are available in literature. The purpose of this chapter is to present a quantitative analysis of the influence of gate voltage on surface potential, charge density and electron mobility of an inverted p-type InGaAs. As InGaAs is the ternary limit of quaternary system of $In_{1-x}Ga_xAs_yP_{1-y}$, the analysis also encompasses n-type inversion layer of InP (y = 0) and other members of the quaternary system. The analysis presented, assumes that the surface inverted semiconductor is grown on a SI-InP substrate with the lattice match condition of $y \simeq 2.2\ x$ satisfied. In this chapter the basic MISFET equations relevant to the purpose mentioned are first reviewed. Using these equations the influence of gate voltage on surface potential in inverted InGaAsP and other MISFET materials is analysed. Considering the gate voltage dependence of inversion and depletion charge density, the control of normal effective field in InGaAs-surface is then analysed. Finally with a brief exposure to the existing knowledge and theories of effective carrier mobility in inversion channel, the composition dependence of effective mobilities in InGaAsP MISFETs has been analysed. InGaAs being the ternary limit of the InGaAsP-alloy system, effective mobility in n-channel inversion-mode MISFET is compared with that in MISFETs made on other members of the alloy system.

3.2 SURFACE POTENTIAL IN INVERTED p-InGaAs AND RELATED COMPOUND SEMICONDUCTORS

An important requirement for a MISFET is satisfactory

control of surface potential by the application of a gate field. A material is considered to be fit for MIS-applications if its surface potential is variable over a large range, by reasonable variation in gate bias voltage. This section presents an analysis of the gate control of surface potential in an InGaAs inversion-mode MIS device. The dependence of surface potential on various material parameters are all examined.

3.2.1 Fundamental Equations

It is well known that when gate voltage V_G is applied on a MIS device, a space charge region is formed which extends from the insulator-semiconductor interface to some depth within the bulk of the semiconductor. For lower gate voltage, this is essentially a depletion layer. However, if the gate voltage exceeds a critical value, generally known as the threshold gate voltage V_T, a thin inversion layer is formed on the surface. Thus, for $V_G \geq V_T$ an inversion layer with an underlying depletion layer is formed. In MIS-terminology, the thin region in which the inversion and depletion layers are formed is called the 'surface region' of the device. Below the depletion layer, the semiconductor is neutral and this neutral portion of the semiconductor is referred to as the bulk region. As a result of the space charge in the surface region an electric field is produced there and the potential of this region differs from that in the bulk. The potential drop across the surface region is called the surface potential ϕ_s. Deep in the bulk semiconductor the potential is called bulk potential ϕ_B. Fig. 3.1 defines ϕ_s and ϕ_B for an inverted p-type semiconductor. It is easily shown that for a p-type semiconductor [220]

$$\phi_B = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \tag{3.1}$$

where

N_A = acceptor concentration (per unit volume)

n_i = intrinsic carrier concentration

T = lattice temperature

k = Boltzmann constant

q = electron charge.

The surface potential, however, is complicated function of material and device parameters. It is also related to the gate bias voltage V_G, through its dependence on normal field. Solving Poisson's equation and considering charge balance across the MIS-insulator, it can be shown that [20,220]

$$C_i(V_G' - \phi_s) = q\, N_A\, L_D\sqrt{2}\left[\, [\, \exp(-\beta\phi_s) + \beta\phi_s - 1\,] + \left(\frac{n_i}{N_A}\right)^2 [\, \exp(\beta\phi_s) - \beta\phi_s - 1\,]\,\right]^{1/2} \tag{3.2}$$

where

C_i = insulator capacitance

$\beta = q/kT$ (3.3)

L_D = bulk Debye length and is given by

$$L_D = (kT\epsilon_s\epsilon_0 / q^2 N_A)^{1/2} \tag{3.4}$$

In Eq. (3.4), ϵ_s is the semiconductor relative permittivity and ϵ_0 is the permittivity of free space. V_G' is the effective gate voltage and is given

$$V_G' = V_G - V_{FB} \tag{3.5}$$

where V_{FB} is the flat-band voltage. Thus, if the flat-band voltage for a semiconductor-insulator system is known, then by solving Eq. (3.2) the surface potential (as a function of gate

voltage) can be determined [220].

3.2.2 Quantitative Analysis

Treating InP (y = 0) and InGaAs (y = 1) respectively as the binary and ternary limits of $In_{1-x}Ga_xAs_yP_{1-y}$-alloy system, surface potential for inverted p-type InP, $In_{0.86}Ga_{0.14}As_{0.3}P_{0.7}$ and $In_{0.53}Ga_{0.47}As$ are calculated from (3.2). The calculations are carried out for acceptor concentration of 10^{22} m^{-3} and lattice temperature of 300 K. The insulator capacitance is taken to be $6.5x10^{-4}$ Fm^{-2}. As can be seen from (3.2) and (3.4), alloy composition dependent material parameters like the ϵ_s and n_i are involved in the calculations. For the calculation of relative semiconductor permittivity, the empirical relation [59]

$$\epsilon_s = 12.35 + 1.62y - 0.055y^2 \qquad (3.6)$$

is used. The intrinsic carrier concentration is calculated from the relation [220]

$$n_i = 4.9x10^{22} \left(m_{de}\, m_{dh}/m_0^{\,2} \right)^{3/4} T^{3/2} \exp\left(E_g/2kT\right) \qquad (3.7)$$

where

m_{de} = density of state effective mass for electron
m_{dh} = density of state effective mass for hole
m_0 = electron rest mass
E_g = bandgap energy.

The alloy composition dependence of the intrinsic carrier concentration comes through m_{de}, m_{dh} and E_g. The alloy composition dependence of the bandgap energy is determined by [59]

$$E_g = 1.35 - 0.72y + 0.12y^2 \text{ eV} \qquad (3.8)$$

the density of state effective mass for the hole is [220]

$$m_{dh} = \left(m_{lh}^{*3/2} + m_{hh}^{*3/2} \right)^{2/3} \quad (3.9)$$

where m_{lh}^* and m_{hh}^* are the light hole and heavy hole effective mass respectively. The alloy composition dependence of these two masses for $In_{1-x}Ga_xAs_yP_{1-y}$ with $y \simeq 2.2\,x$ are given by [59]

$$\frac{m_{lh}^*}{m_0} = 0.12 - 0.078y + 0.02y^2 \quad (3.10)$$

and

$$\frac{m_{hh}^*}{m_0} = 0.6 - 0.218y + 0.07y^2 \quad (3.11)$$

The density of state effective mass for the electron is calculated from the empirical relation for electron effective mass, which is

$$\frac{m_e^*}{m_0} = 0.07 - 0.0308y \quad (3.12)$$

Thus, m_{de} and m_{dh} are calculated from (3.9) - (3.12).

Considering the involved nature of dependence of surface potential on gate voltage, Brews [20] suggested an iterative process for solving Eq. (3.2). In the present work, a relatively simpler iterative approach is taken. Surface potential thus calculated is normalized to bulk potential ϕ_B as given by (3.1). This is done to assess the degree of inversion directly from the calculation of surface potential as function of effective gate voltage V_G'. As silicon is most commonly used material for MIS-technology, thus for the sake of comparison surface potential for silicon of same doping and insulator capacitance is also calculated. Fig. 3.2 illustrates the effective gate voltage dependence of normalized surface potential for all the four

materials considered. The calculated values of material parameters ϵ_s, E_g and n_i for the III - V compounds are given in Table 3.1 along those taken for silicon.

Table 3.1: Material Parameters Used in Surface Potential Calculation.

Material	y	ϵ_s	E_g(eV)	$n_i(m^{-3})$	ϕ_B(V)
InP	0.0	12.35	1.35	8.47×10^{12}	0.541
$In_{0.86}Ga_{0.14}As_{0.3}P_{0.7}$	0.3	12.83	1.145	4.66×10^{14}	0.437
$In_{0.53}Ga_{0.47}As$	1.0	13.92	0.75	8.2×10^{17}	0.244
Silicon	-	11.90	1.1	1.45×10^{16}	0.348

According to MIS-theory, inversion sets in when the surface potential just equals the bulk potential. From Fig. 3.2, it is evident that of the four potential candidates for MIS device application, the effective gate voltage required for onset of inversion is minimum of InGaAs (0.75 V). This is followed by silicon, requiring an effective gate voltage of 0.85 V. The effective gate voltage requirement for InP is the highest as it is 1.2 V. For the quaternary alloy system of InGaAsP, the effective gate voltage required for onset of inversion is composition dependent. This is obvious from the fact that with composition parameter y = 0.3, the required effective gate voltage is about 1.05 V. This lies between the effective gate voltage required for the binary and ternary limits of the quaternary. In other words, effective gate voltage required for onset of inversion decreases with increase in the y-composition parameter.

In MIS-theory, strong inversion is said to occur when

$$\phi_s = 2\,\phi_B \tag{3.13}$$

From Fig. 3.2, it can be seen that strong inversion in InP, InGaAsP (y = 0.3), InGaAs and silicon sets in at effective gate voltages of 2.1 V, 1.7 V, 1.2 V and 1.45 V respectively. Thus, for strong inversion to set in, the effective gate voltage requirement in InGaAs is minimum and it is maximum for InP. It is also clear from Fig. 3.2 that the degree of inversion in InGaAs is much higher than what it is for other semiconductors, which have been tried for MIS-applications.

For MIS-applications it is desirable that the surface potential varies over a large range of gate voltage. Fig. 3.2 shows that in this respect also InGaAs is a better semiconductor than silicon and InP. Higher values of ϕ_s/ϕ_B-ratio means stronger inversion. Thus, for the same effective gate voltage much stronger inversion can be achieved in InGaAs. The analysis on which these results are based, however, does not take into account the existance of interface charges, oxide charges etc. In reality these charges do exert and have substantial effect on surface potential variation with gate voltage. These effects primarily depend on the process technology. The present analysis, therefore indicate that an excellent gate control on an inversion channel in InGaAs can be realized if good insulator-semiconductor interface properties can be achieved.

3.3 CHARGE AND FIELD IN INVERSION LAYER

Application of a gate voltage results in a normal field on the surface of the semiconductor. This field depends on the

density of the charge present at the surface. In inversion-mode MISFETs, the charge in the surface inversion layer are of two types, namely, the inversion charge and the depletion charge. The densities of these charges are controlled by the gate voltage. In this section, the gate voltage dependence of the inversion and depletion charges, and the consequent effect, on the normal field in an n-channel inversion- mode InGaAs MISFET are analysed.

3.3.1 Depletion and Inversion Charge Densities

The normal field produced at the surface of a MIS-system produces a depletion region by depleting the surface region of the majority carriers. Thus, in the case of a p-type semiconductor, in the surface region negative acceptor ions form a space charge region. Across this depletion region the potential drop ϕ_s appears. Solving Poisson's equation with the assumption that there is no potential variation along the channel, it can be shown that the depletion layer charge density per unit area is [20]

$$Q_B = q N_A L_D [2 (\beta\phi_s - 1)]^{1/2} \qquad (3.14)$$

Thus, if W is the thickness of the depletion region then substituting (3.3) and (3.4) in (3.14)

$$W = [2 \epsilon_s \epsilon_0 (\phi_s - \frac{kT}{q}) / qN_A]^{1/2} \qquad (3.15)$$

When the gate voltage is increased to the extent of making

$$\phi_s = \phi_B \qquad (3.16)$$

surface inversion sets in. Under this condition, the normal field becomes large enough to hold the minority carrier in a thin layer at the insulator-semiconductor interface. For gate voltage beyond this limit, the normal field increases thereby increasing the

minority carrier concentration. Thus, in a p-type semiconductor a sufficiently high positive gate voltage, induces two type of negative charges, the electron and the negatively charged acceptor ions.

The total charge induced is, therefore

$$Q_{ind} = Q_B + Q_n \tag{3.17}$$

where Q_n is the inversion charge (electron charge in this case) density per unit area. As Q_{ind} is the result of positive charge on the gate electrode, field theory requires

$$C_i (V_G' - \phi_s) = Q_B + Q_n \tag{3.18}$$

Substituting (3.14) in (3.18)

$$Q_n = C_i (V_G' - \phi_s) - q N_A L_D [2 (\beta\phi_s - 1)]^{1/2} \tag{3.19}$$

If n_s is the electron density (per unit area) in the inversion layer then

$$Q_n = q n_s \tag{3.20}$$

and thus from (3.19) and (3.20)

$$n_s = \frac{1}{q} C_i (V_G' - \phi_s) - N_A L_D [2 (\beta\phi_s - 1)]^{1/2} \tag{3.21}$$

Knowing ϕ_s from the solution of (3.2), it is therefore possible to calculate inversion layer carrier density from (3.21).

The inversion layer carrier density plays a very significant role in the operation of a MISFETs as it is one of the parameter that determines the channel conductivity. In order to assess the gate voltage control on the inversion carrier densities in p-type InGaAs, InGaAsP, InP and silicon, n_s is calculated using (3.2) and (3.21). Lattice temperature, acceptor concentration and

insulator capacitance taken for this purpose are the same as those for the calculations presented in subsection 3.2.2. Fig. 3.3 shows the effective gate voltage dependence of the semiconductors considered. It can be seen that, for lower effective gate voltages the surface electron concentration in all these semiconductor is almost same. At higher gate voltages, some difference in the response of inversion layer carrier concentration is noticeable.

The inversion layer carrier concentration is an increasing function of the surface potential [20]. Thus, as surface potential increases with increase in gate voltage (Fig. 3.2), the inversion carrier density also increases (Fig. 3.3). For the same effective gate voltage, surface potential is different for different material (Fig. 3.2). The result is differing inversion carrier densities in defferent semiconductors for the same effective gate voltage. However, the pattern remains the same as for surface potential, in the sense that InGaAs has the highest inversion carrier concentration followed by silicon and InP. For obvious reasons, InGaAsP has a carrier concertration in between InGaAs and InP. Both Figs. 3.2 and 3.3 show that the behaviour of inversion layers in InGaAs and silicon are similar. Silicon MIS-technology is already well established. The present calculations show that InGaAs is a close competitor of silicon for MIS-applications.

3.3.2 Effective Normal Field

The normal field in the surface region is determined by the charge content of the region. From Gauss's law the peak field in this region is by [218]

$$E_{peak} = \frac{1}{\epsilon_s \epsilon_0} [Q_B + Q_n] \quad (3.22)$$

From quantum-mechanical considerations, it has been shown [76,78] that the inversion carriers are distributed in a Gaussian profile over certain width (50 - 100 Å) and the peak field exists at a position determined by doping level and surface potential. Thus, most of the carriers in the inversion layer do not experience the peak field. Thus for all calculation purposes, it has been found more appropriate to use an average normal field which in MIS-terminology is known as the effective field. The effective field has been worked out to be

$$E_{eff} = \frac{1}{\epsilon_s \epsilon_0} [Q_B + \frac{1}{2} Q_n] \quad (3.23)$$

Substituting (3.14) and (3.19) in (3.23)

$$E_{eff} = \frac{1}{2 \epsilon_s \epsilon_0} \left[(q N_A L_D [2 (\beta\phi_s - 1)]^{1/2} + C_i (V_G' - \phi_s) \right] \quad (3.24)$$

Through its dependence on Debye length L_D, the effective field as given by (3.24) is dependent on the material parameter ϵ_s. Besides this, the effective field is dependent on doping level, lattice temperature, gate voltage and gate insulator.

The effective gate voltage dependence of the effective normal field E_{eff}, is illustrated in Fig. 3.4, along with those of depletion charge density Q_B, and inversion charge density Q_n. In general, for both materials E_{eff} increases with increase in gate voltage. However, for the same gate voltage, E_{eff} is higher in InGaAs surface than in silicon surface. For lower gate voltages this is primarly an effect of higher ϵ_s in InGaAs, as Q_B and Q_n do not differ significantly in the two materials. At moderate gate voltages also total charge remains almost same in the two

materials, Q_B being lower and Q_n being higher in InGaAs. Thus, for moderate gate voltages also, higher semiconductor permittivity is the cause for higher E_{eff} in InGaAs. The difference in E_{eff} for the two materials widens in higher ranges of effective gate voltage. Similar increase in the difference between the inversion charge densities is also indicated by Fig. 3.4. This shows that for higher gate voltages, higher inversion charge density in InGaAs also makes its contribution in making E_{eff} to be higher in InGaAs than in silicon.

3.4 CARRIER MOBILITY IN INVERSION CHANNEL

Carrier mobility in the channel region of a MIS-system plays an important role in characterizing device performance. The carriers in the channel region move under the influence of a normal electric field caused by gate voltage. These carriers suffer various scattering mechanism in the channel and insulator-semiconductor interface regions, thereby giving smaller value of carrier mobility. An analysis of these phenomena is presented in this section.

3.4.1 Scattering Mechanism in Inversion Channel

In a MISFET the inversion layer forms the conducting channel between the drain and source contact. The channel conductivity is modulated by varying the gate voltage. As a consequence of this the output current (drain current) varies in accordance with variation in the gate voltage. Naturally, the drain current depends on the carrier mobility in the channel. Since the current flows through inversion layer, mobility is

expected to be influnced by the electric fields in the channel. Experimental investigations show that inversion layer mobility is a unique function of normal field [38,71,184,194,214]. It has been observed that mobility decreases with increase in normal field, that is gate voltage. Another interesting feature of inversion layer mobility is that, it is much lower than bulk mobility of the semiconductor. Many authors [193,202,204] are of the opinion that the inversion layer mobility is about 50 % of bulk mobility. Others [184,194], however, pointed out that, it is not necessarily so, and such an assumption may be in considerable error under certain conditions.

Carrier mobility depends on the scattering mechanism involved. Lower mobility in an inversion layer indicates that carrrier scattering in addition to lattice and impurity ion scattering occur near the insulator-semiconductor interface, by mechanism intrinsic the interface. Several workers have studied the scattering process in the inversion layers of the MIS-systems [30,31,79,84,119,179,186,193]. These investigations reveal that considerable irregularties in the form of uneven surface exists at the insulator-semiconductor interface. In addition, different types of charge centres of varying origin exists in the vicinity of the interface. These charges are inversion layer carrier charge, insulator fixed charge, ionized impurity charge and interface state charge. As stated earlier, the inversion layer carrier charge is distributed over a thin region within the semiconductor. The insulator charge is distributed inside the insulator and some of these are very close to the interface, so that they are able to scatter the carrier in the inversion channel. The surface state charge is spatially distributed on the

interface and their charge density changes with gate bias voltage in accordance with interface state density distribution over the bandgap. The interface charges can be either acceptor type or donor type. The ionized impurity distribution depends on the doping process.

The surface roughness resulting from uneven surface at the interface gives rise to various modes of vibrations, which include surface acoustic phonons and optical phonons. Surface phonon scattering plays an important role at room temperature and above. It is however, insignificant at very low temperatures. Under the strong inversion condition, the high normal field confines the inversion layer carriers within a very narrow region along the surface. Thus, for strong inversion the scattering due to surface roughness becomes a mojor scattering process. This is because of the fact that most of the carriers are closer to the surface and the scattering probability arising out of surface roughness increases.

Besides various phonon scattering mechanism, Coulomb scattering in an inversion channel influences carrier mobility to a very great extent. The charge centres, which include fixed oxide charge, interface state charge and the ionized impurity atoms are all involved in this type of scattering mechanism at the insulator-semiconductor interface. In a very strongly inverted surface, however, the Coulomb scattering processes are less effective. This is because of the fact that, a high concentration of mobile charge (electrons or holes) surround the charge centres which results in a reduction of their scattering cross-section. Thus, in a lightly inverted surface, the Coulomb scattering

process is more dominant.

The channel mobility is releted to bulk mobility through its dependence on Coulomb scattering by the ionized impurity atoms and the vibrational modes of the host semiconductor atoms present in the channel.

In order to include the effect of bulk scattering mechanism, Many [136] employed Matthiessen's rule to combine bulk mobility (μ_B) and surface mobility (μ_s) contributions towards channel mobility. Schwarz and Russek [194] later extented this idea to develop semi-empirical equations for Si-MIS inversion layers. In elemental semiconductors, such as silicon, the lattice vibration and impurity ion are the dominant factors for the bulk scattering processes. In compound semiconductors, however, polar optical phonon scattering, alloy scattering and deformation potential scattering also make considerable contributions. For alloy semiconductors, such as, InGaAsP or InGaAs, these scattering mechanism are alloy composition dependent [176]. Numerous experimental data regarding the alloy composition dependence of bulk carrier mobility in $In_{1-x}Ga_xAs_yP_{1-y}$ system are available in literature [1,2,18,90,177]. These data show that for quaternary system lattice matched to InP, electron mobility increases with increase in the y-composition parameter. The electron mobility is highest for the ternary limit of y = 1, that is InGaAs. Thus, a Matthiessen's rule based calculation of channel mobility from the relation

$$\frac{1}{\mu_{ch}} = \frac{1}{\mu_B} + \frac{1}{\mu_s} \qquad (3.25)$$

should yield highest channel mobility for InGaAs inversion layers.

Experimental data also support this [71].

3.4.2 Effective Mobility

When an inversion channel forms the carrier path between source and drain of a MISFET, quantitative assessment of carrier mobility becomes important. If carrier diffusion is negligible, the drain current in terms of carrier mobility μ, concentration (per unit area) N, channel width Z and channel length L is

$$I_{DS} = - \frac{q \cdot Z}{L} \int_0^{V_{DS}} \mu \, N \, dV \qquad (3.26)$$

where the source and substrate are assumed to be at the ground potential and V_{DS} is the drain-source voltage. Both μ and N are known to be the functions of potential V, which varies along the length of the channel. μ being a complicated function of V, the evaluation of the integral is a formidable task. Very often the calculations are simplified by defining an effective mobility μ_{eff}, such that [20,36]

$$I_{DS} = \mu_{eff} \frac{q \, Z}{L} \int_0^{V_{DS}} N \, dV \qquad (3.27)$$

where μ_{eff} is treated as a constant. It is obvious that for μ_{eff} to be a useful parameter

$$\mu_{eff} = \frac{\int_0^{V_{DS}} \mu \, N \, dV}{\int_0^{V_{DS}} N \, dV} \qquad (3.28)$$

However, the formal definition of μ_{eff} given by (3.28) is not useful for analytical purposes, as this involves the same integral as in (3.26). Therefore, in practice μ_{eff} is determined empirically [81,113,124,218,248]. Such an approach, however, require elaborate experimentation for the determination of various constants involved in the empirical equations for effective mobility. For long-channel devices, it is more convenient to determine μ_{eff} from drain conductance measurements. Effective mobility is related to drain conductance g_d by [218]

$$\mu_{eff} = [\, L\, g_d \,/\, Z\, q\, n_s \,]_{V_{DS} \to 0} \qquad (3.29)$$

The effective mobility is gate voltage dependent, because of the influence of gate voltage on drain conductance and inversion carrier density n_s. This influence is well supported by experimental evidences [71,218]. A decrease in effective mobility with increase in gate voltage is generally observed. This mobility degradation is attributed to onset of degenerate conditions at higher gate fields [36]. As the alloy composition parameters (x and y) influence channel parameters like surface potential, normal field etc., in inversion layers on $In_{1-x}Ga_xAs_yP_{1-y}$ system, it is of interest to know the alloy composition dependence of μ_{eff} in such inversion layers. Experimental work of Shinoda and Kobayashi [204] provides data for gate voltage dependence of drain conductance of InGaAsP MISFETs of different alloy composition parameters. Some of these data will now be used for the purpose of analysing the gate voltage dependence of effective mobility of InGaAsP MISFETs.

The MISFETs considered in the present analysis are InP(I96),

$In_{0.87}Ga_{0.13}As_{0.29}P_{0.71}$(Q11) and $In_{0.76}Ga_{0.24}As_{0.55}P_{0.45}$(Q31) MISFETs of Ref.[204]. As reported by Shinoda and Kobayashi [204], these MISFETs have 1000 Å thick Al_2O_3 as gate insulator and gold as the gate electrode. The channel length and width of these MISFETs are 10 μm and 120 μm respectively. For calculation purposes an insulator capacitance of 6.3×10^{-4} Fm^{-2} is assumed on the basis of dielectric constant of 7.12 for Al_2O_3. Using the threshold voltage equation [220]

$$V_T = V_{FB} + 2\,\phi_B + \frac{1}{C_i}\,[\,2\,\epsilon_s\,\epsilon_0\,q\,N_A\,(2\phi_B)\,]^{1/2} \qquad (3.30)$$

and by calculating ϕ_B from (3.1), the flat-band voltage for the three MISFETs are determined. The calculated flat-band voltages along with the values of N_A and V_T as taken from Ref. [204] are given in Table 3.2. Since the $In_{1-x}Ga_xAs_yP_{1-y}$-substrates of Shinoda and Kobayashi were all lattice matched to InP, the relation

$$y \simeq 2.2\,x \qquad (3.31)$$

is assumed and while referring to alloy composition, only the y-composition parameter will be stated from now on.

Table 3.2 : Substrate Carrier Concentration, Threshold Voltage and Flat-Band Voltage.

Substrate	y	N_A (m^{-3})	V_T (V)	V_{FB} (V)
InP	0.00	7×10^{22}	1.41	- 2.44
$In_{0.87}Ga_{0.13}As_{0.29}P_{0.71}$	0.29	10^{23}	0.56	- 3.46
$In_{0.76}Ga_{0.24}As_{0.55}P_{0.45}$	0.55	10^{23}	- 0.067	- 3.74

The calculated values of flat-band voltage show that V_{FB} increases in magnitude with increase in y-composition parameter. As V_{FB} depends on modified work function and interface charge density, its dependence on alloy composition can be expected. Surface state density and energy bandgap decrease with increase in y [59,176,204]. Furthermore, the bulk potential ϕ_B, is alloy composition dependent through its relation with intrinsic carrier concentration n_i. The semiconductor work function being determined. Thus, flat-band voltage, which is given by

$$V_{FB} = \phi_{Wm} - \phi_{Ws} - \frac{Q_{ss}}{C_i} \qquad (3.32)$$

is a function of alloy composition. In (3.32) ϕ_{Wm} and ϕ_{Ws} are the metal and semiconductor work function.

The calculated flat-band voltages are used to determine surface potential by solving (3.2). Fig. 3.5 illustrates the variation of surface potential with gate voltage for the three MISFETs considered. It shows that reverse is the case for normalized surface potential plotted in Fig. 3.2. This is because of the fact that Fig. 3.2 illustrates the gate voltage dependence of relative surface potential and it only indicates the strength of inversion. On the other hand, Fig. 3.5 shows actual surface potential. Making use of the calculated values of surface potentials and flat-band voltages, the carrier densities in the inversion layers of the MISFETs under consideration are calculated from (3.21). Fig. 3.6 shows the gate voltage dependence of inversion layer carrier concentration. It is interesting to note that for same gate voltage carrier density is higher for higher y (Fig. 3.6) while surface potential is higher for lower y

(Fig. 3.5). At the same time, both carrier density and surface potential increases with increase in gate voltage for all values of y. This shows that inversion carrier density is not only determined by the magnitude of surface potential, but also by its value relative to the bulk potential (Fig. 3.2).

Because of y-dependence of inversion layer carrier density, on the basis of (3.29) one can expect the effective mobility to vary with y-composition parameter. Fig. 3.7 illustrates the gate voltage dependence of effective mobility of the three MISFETs for which calculations are carried out. The effective mobilities are determined by the aid of calculated inversion layer carrier densities, drain conductance data of Shinoda and Kobayashi [204] and (3.29). Fig. 3.7 shows that effective mobility increases with increase in y-composition parameter. In this respect, effective mobility follows bulk mobility. This is to be expected as bulk mobility makes a contribution to channel mobility as discussed in subsection 3.4.1. The most striking feature of effective mobility variation with gate voltage is that considerable mobility degradation occurs at higher gate voltages for larger values of y-composition parameter. For InP, that is when y is zero, effective mobility is more or less independent of gate voltage over a fairly wide range of 0 - 4 V. For an InGaAsP MISFET with a y value of 0.29, a nominal effective mobility degradation can be seen. But when y-composition parameter is as large as 0.55, effective mobility degrades by about 31 % as gate voltage changes from 1 V to 3 V. The y-composition parameter has the highest value of unity for InGaAs. Gardner et al. [71] determined effective mobility of an InGaAs MISFET (y = 1) using (3.29). Their data show that an effective

mobility degradation of about 50 % takes place when gate voltage is increased from 1 V to 3 V. For the sake of comparison the effective mobility data of Gardner et al. are also plotted in Fig. 3.7. The effective mobility data of Gardner et al. further highlights the fact that higher effective mobility can be realized by increasing y-composition parameter. This is, however, achieved at the expense of poorer mobility degradation with increase in gate voltage.

Influence of increasing gate voltage, however, is not necessarily a case of effective mobility degradation. This can be varified from the nature of gate voltage dependence of effective mobility for y = 0.55. For this case, as gate voltage increases from a low value, effective mobility first increases, reaches a peak and then decreases. Interestingly such is not the case for either InGaAsP MISFET with y = 0.29 or InP MISFET with y = 0. These differences in effective mobility behaviour results mainly from two factors, which depend on the substrate material. An increase in effective mobility with increase in gate voltage is possible, if ionized impurities in channel are screened by the enhancement of carrier concentration. A decrease in effective mobility with increase in gate bias may result from decrease in channel thickness. Decrease in channel thickness makes the inversion charge carriers to suffer more surface scattering. As a consequence, the surface mobility μ_s, decreases. Thus, whether effective mobility rises or falls with increase in gate voltage is determined by the more dominant of the two factors.

Based on (3.25), effective mobility of a MISFET can be shown to be given by [194]

$$\mu_{eff} = \frac{\mu_B}{1 + \frac{\mu_B m_e^* v_{th}}{2q}\left[\frac{\bar{p}_0}{z_i} + \frac{\sigma_0 N_f}{(z_i^3 n_s)^{1/4}}\right]} \qquad (3.33)$$

where

v_{th} = thermal velocity of the carriers

$\bar{p}_0$ = probability of scattering by surface phonon and surface roughness

σ_0 = a constant related to scattering cross-section of interface fixed charge

N_f = interface fixed charge density (per unit area)

z_i = inversion layer thickness.

The gate voltage dependent quantities in (3.33) are z_i and n_s. The two terms within parenthesis accounts for the surface scattering process. The first term which varies as $1/z_i$ is the contribution of phonon and surface roughness scattering. The second term, which varies as $(z_i^3 n_s)^{-1/4}$ is the contribution of interface fixed charges and screening by inversion carriers. The inversion layer thickness z_i, is a function of y-composition parameter through effective field and carrier effective mass. From quantum-mechanical considerations, the channel thickness may be expressed by [194]

$$z_i = \frac{3kT}{2q\mu_{eff}} + \left[\frac{9\hbar^2}{4m_e^* q E_{eff}}\right]^{1/3} \qquad (3.34)$$

where $\hbar$ is reduced Planck's constant. As the effective field E_{eff}, increases with increase in gate voltage (Fig. 3.4), channel thickness decreases. Calculating E_{eff} and m_e^* from (3.2), (3.4), (3.12) and (3.24), inversion layer thickness for the three values of y-parameter have been evaluated.

These calculations show that channel thickness increases with increase in y-parameter. This variation of channel thickness is a reflection of the decrease in effective mass m_e^* with increase in y-composition parameter. There is, however, an increase in E_{eff} with increase in y-parameter. But this increase is nominal and is over shadowed by the decrease in effective mass. Table 3.3, illustrates the y-dependence of m_e^* and E_{eff}.

Table 3.3 : Electron Effective Mass (m_e/m_0) and Surface Effective Field.

$m_0 = 9.1 \times 10^{-31}$ Kg

Substrate	y	m_e^*/m_0	Effective Field (V/m) V_G=1.5 V	V_G=2 V	V_G=3 V
InP	0.00	0.07	2.23×10^7	2.43×10^7	2.75×10^7
$In_{0.87}Ga_{0.13}As_{0.29}P_{0.71}$	0.29	0.061	2.73×10^7	2.88×10^7	3.25×10^7
$In_{0.76}Ga_{0.24}As_{0.55}P_{0.45}$	0.55	0.053	3.67×10^7	2.84×10^7	3.13×10^7

The effect of finite channel thickness on effective mobility is gate voltage dependent because of two reasons. Firstly, with increase in gate voltage, channel thickness decreases thereby bringing the inversion carrier closer to the interface. This increases the probability of scattering by surface phonons and surface roughness. As it has been already mentioned this is accounted for by a $1/Z_i$-dependent term is effective mobility equation. Fig. 3.8, shows the gate voltage dependence of $1/Z_i$ for two values of y-composition parameter. From the behaviour of $1/Z_i$, it is clear that with increase in gate voltage, $\bar{p}_0/Z_i$

increases (Eq. 3.33) and surface scattering tends to reduce mobility. Fig. 3.7 shows that, such a mobility degradation effect is not perceptible at lower gate voltage, especially for MISFETs of lower y-composition parameter. As previously mentioned, this mobility degradation is likely to be compensated by screening effect. With increase in gate bias, inversion carrier concentration increases and for higher y-parameter, the inversion carrier concentration is higher (Fig. 3.6). Thus as the gate voltage is increased, the increase in surface carrier concentration n_s, along with decrease in channel thickness increases volume concentration of free carrier concentration in the channel. This enhancement of free carrier concentration tends to screen out the effect of the fixed charges on carrier mobility. In (3.33) this effect is accounted for by the term $\sigma_0 N_f/(Z_i^3 n_s)^{1/4}$. The gate bias dependent factor, that is, $(Z_i^3 n_s)^{-1/4}$ is plotted as a function of gate voltage in Fig. 3.9, for the y values of 0.29 and 0.55. It can be seen that the quantity $(Z_i^3 n_s)^{-1/4}$ indicates enhancement of screening effect. It is interesting to note that, as gate voltage increases, the screening factor first decreases rapidly and then with a gradually decreasing rate. It means that at higher gate voltage screening cannot sufficiently compensate the mobility degradation arising out of reduction in channel thickness and the resulting surface scattering processes. Thus, at sufficiently higher gate voltage, effective mobility degradation becomes significant.

The rate of decrease of $(Z_i^3 n_s)^{-1/4}$ with increase in gate voltage is lower for higher values of y-composition parameter (Fig. 3.9). As a result of this, for MISFETs with higher y-values effective mobility degradation becomes significant at

comparatively lower gate voltages. Fig. 3.7 clearly shows these effects. Effective mobility degradation with increase in gate voltage is most significant for InGaAs MISFET for which y has the maximum value of unity. For InGaAsP MISFET with a y of value 0.55 effective mobility is fairly independent of gate voltage till about 1.5 V and degradation sets in beyond the gate bias. For InGaAsP MISFET with y = 0.29 and the InP MISFET (y = 0), effective mobility improves with increase in gate voltage for lower values of the latter. Effective mobility thus remains more or less constant over the range of gate voltage considered, indicating that degradation sets in at much higher voltage. The initial rise in mobility for the last two cases, is due to high rate of fall in $(Z_i^3 n_s)^{-1/4}$ factor at lower gate voltages, which over compensetes the effect of decrease in channel thickness leading to increased surface scattering. Thus, briefly speaking, very high effective mobility is achieved in InGaAs MISFETs because of thicker inversion channel and lower electron effective mass. However, because of a thick inversion layer, volume concentration of inversion carrier fail to increase sufficiently to screen out the Coulomb scattering centres and this leads to substantial effective mobility degradation at higher gate voltages. InP MISFETs are of lower effective mobility, but the mobility degradation is pronounced only at very high gate voltages.

Another form of mobility that is widely used in MISFET consideration is field-effect mobility, μ_{FE}. A small signal excitation on the gate produces a mobility variation. It is this differential mobility which is termed as field-effect mobility. The differential mobility will naturally depend on the effective mobility variation with gate voltage. In other words, the

field-effect mobility and effective mobility are related [218]. As a result, field-effect mobility decreases with decrease in effective mobility. Thus, a MISFET with considerable effective mobility degradation with increase in gate bias also suffers from a corresponding field-effect mobility degradation. As field-effect mobility determines, the transconductance of a MISFET, degradation of field-effect mobility is undesirable. From this point of view, InP MISFETs have a definite advantage over MISFETs of higher y-composition parameter. Gardner et al. [71] determined field-effect mobility for InGaAs MISFET and observed considerable degradation with increase in gate voltage.

3.5 CONCLUSION

The inversion channel properties of n-channel InGaAs and related MISFETs have been considered in this chapter. Through an analytical approach it is observed that InGaAs-surface is more easily inverted by a normal field. The properties of InGaAs inversion channel are similar to those of inverted silicon surface in many respect. One definite advantage that InGaAs offers over other materials for MISFET application is high effective channel mobility. Mobility degradation in InGaAs MISFET is, however, more severe than what it is in other MISFETs.

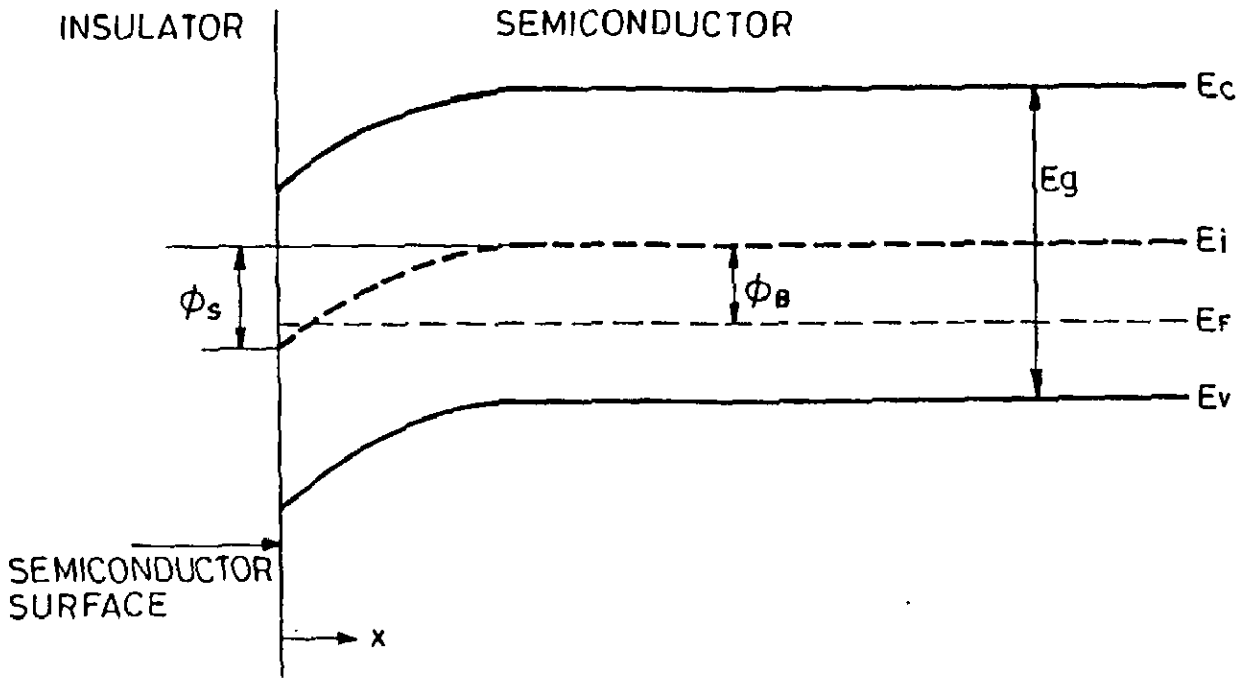

FIG. 3.1 BAND DIAGRAM AT THE SURFACE OF INVERTED p-TYPE SEMICONDUCTOR.

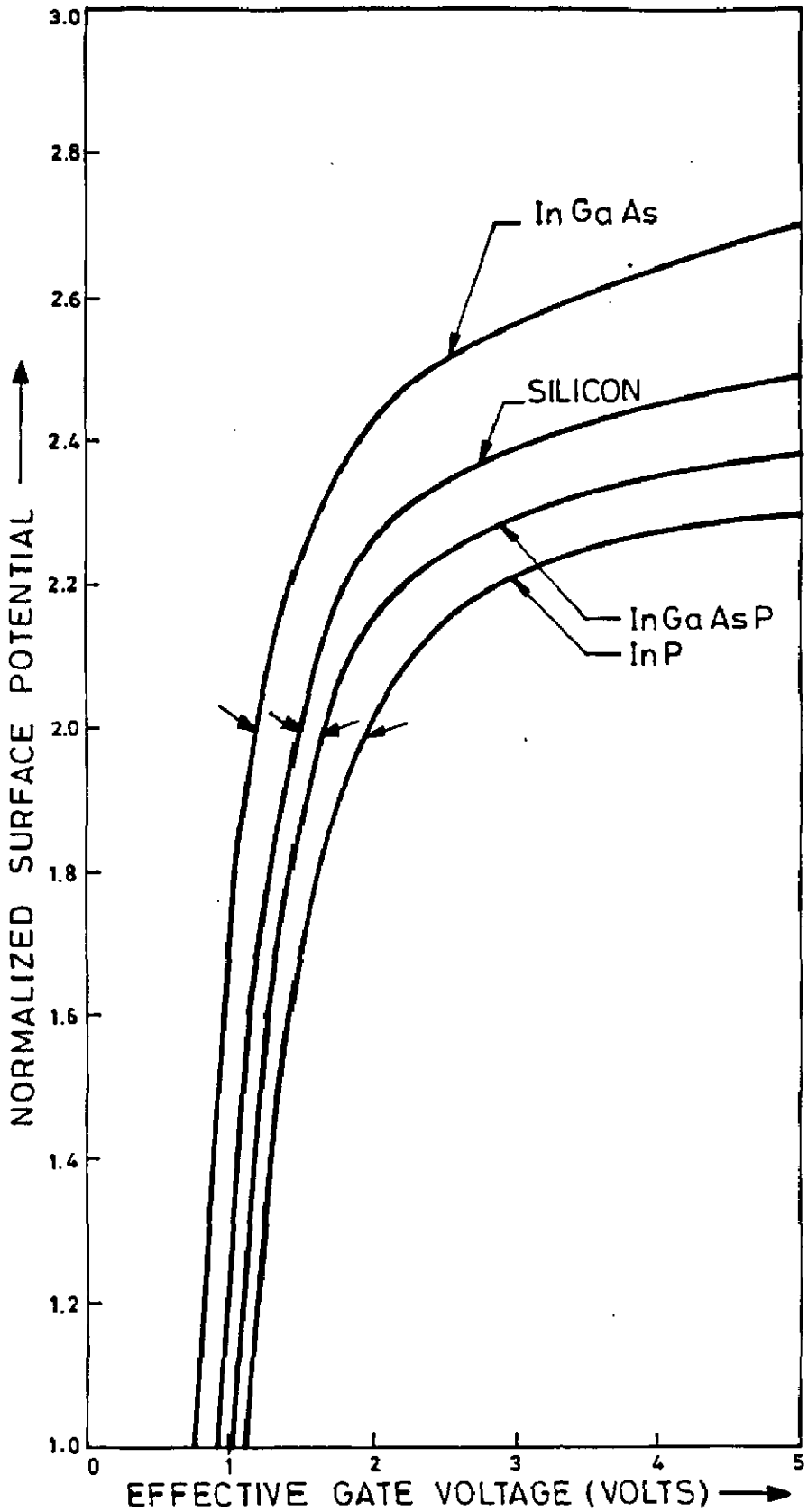

FIG. 3.2 SURFACE POTENTIAL AS A FUNCTION OF EFFECTIVE GATE VOLTAGE (ARROW HEADS INDICATE ONSET OF STRONG INVERSION).

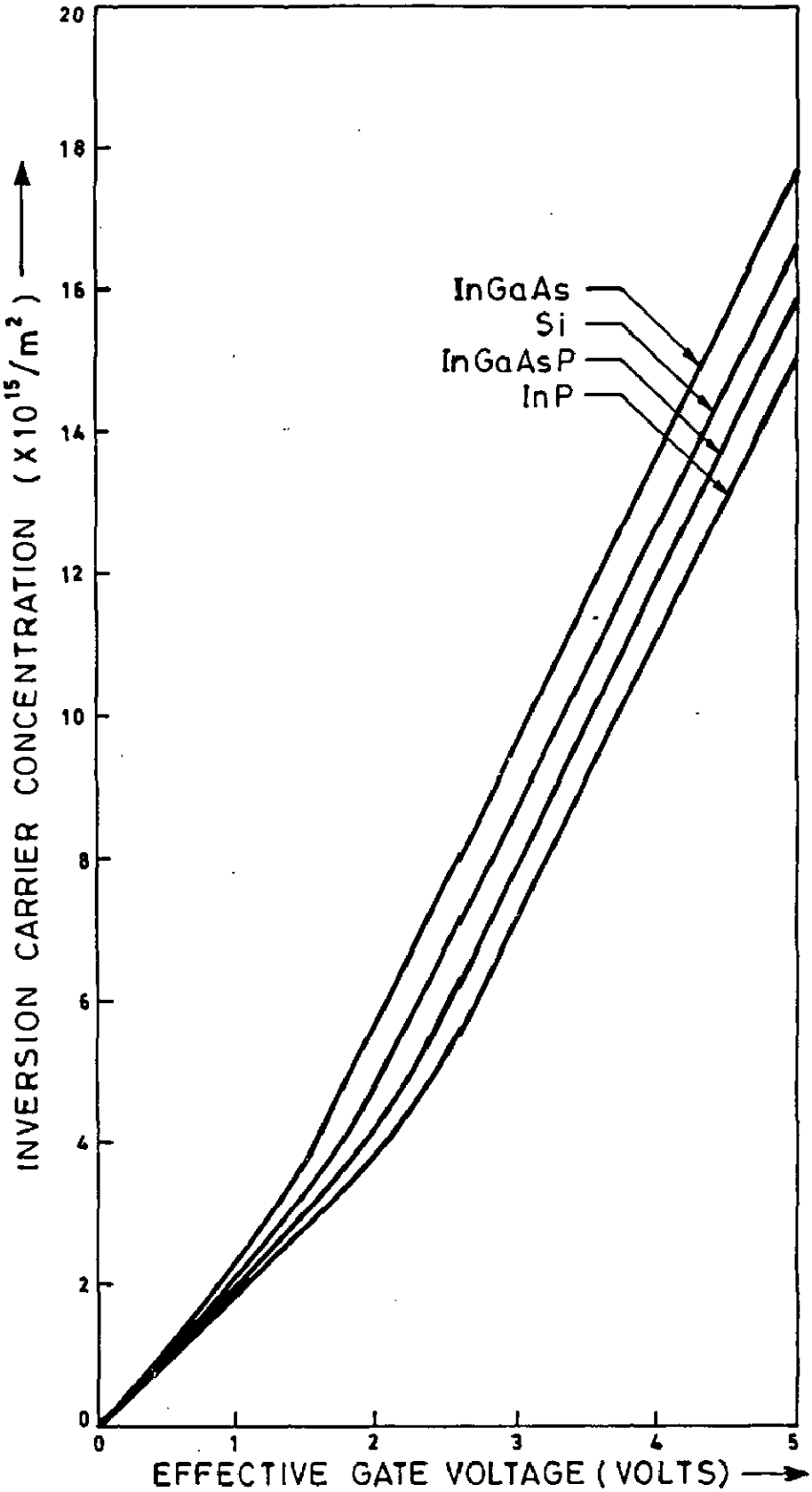

FIG. 3.3 CHANEL CARRIER CONCENTRATION AS FUNCTION OF EFFECTIVE GATE VOLTAGE.

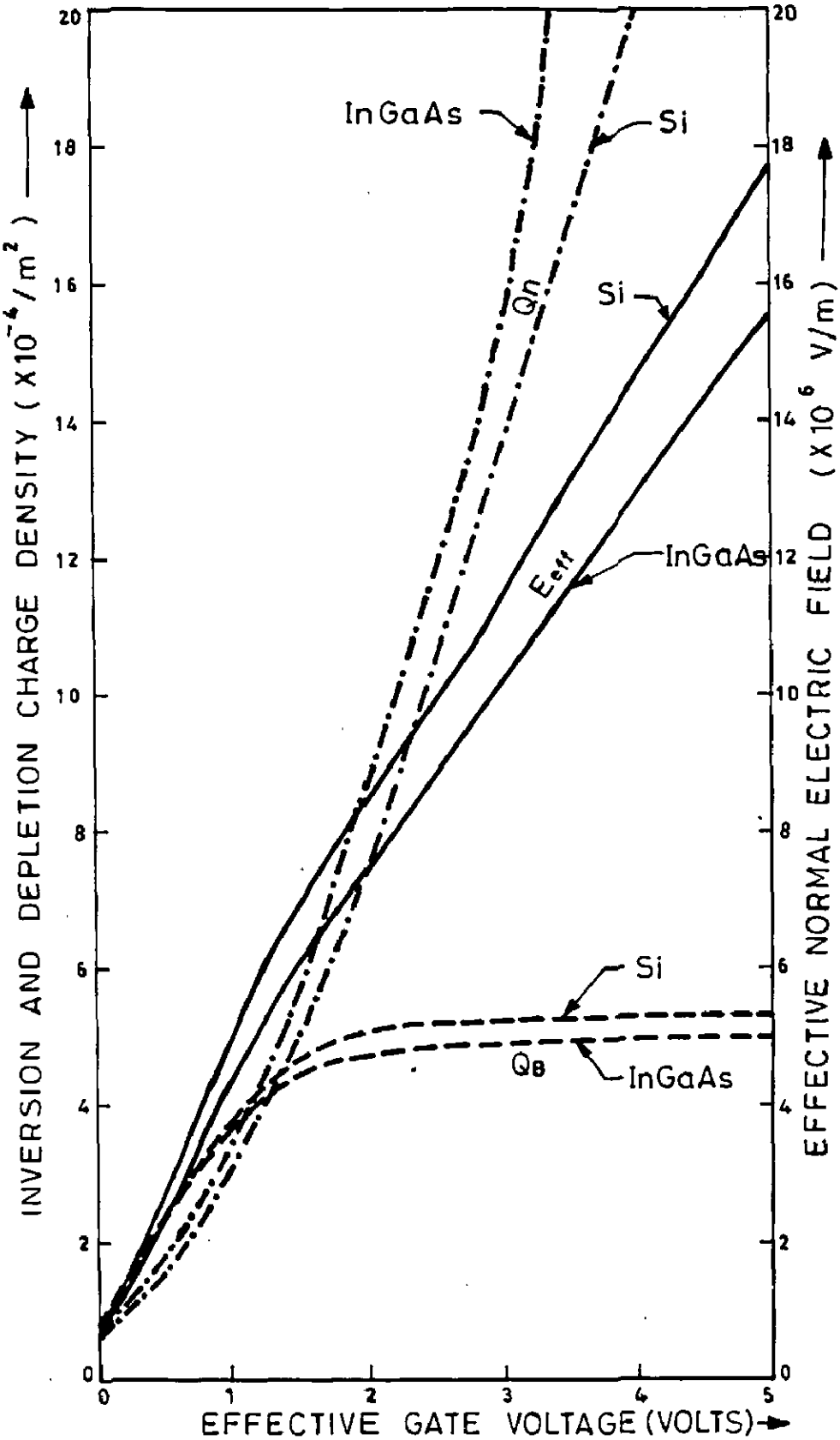

FIG. 3.4 INVERSION AND DEPLETION CHARGE DENSITIES AND EFFECTIVE NORMAL FIELD AS FUNCTION OF EFFECTIVE GATE VOLTAGE FOR InGaAs AND Si MISFET.

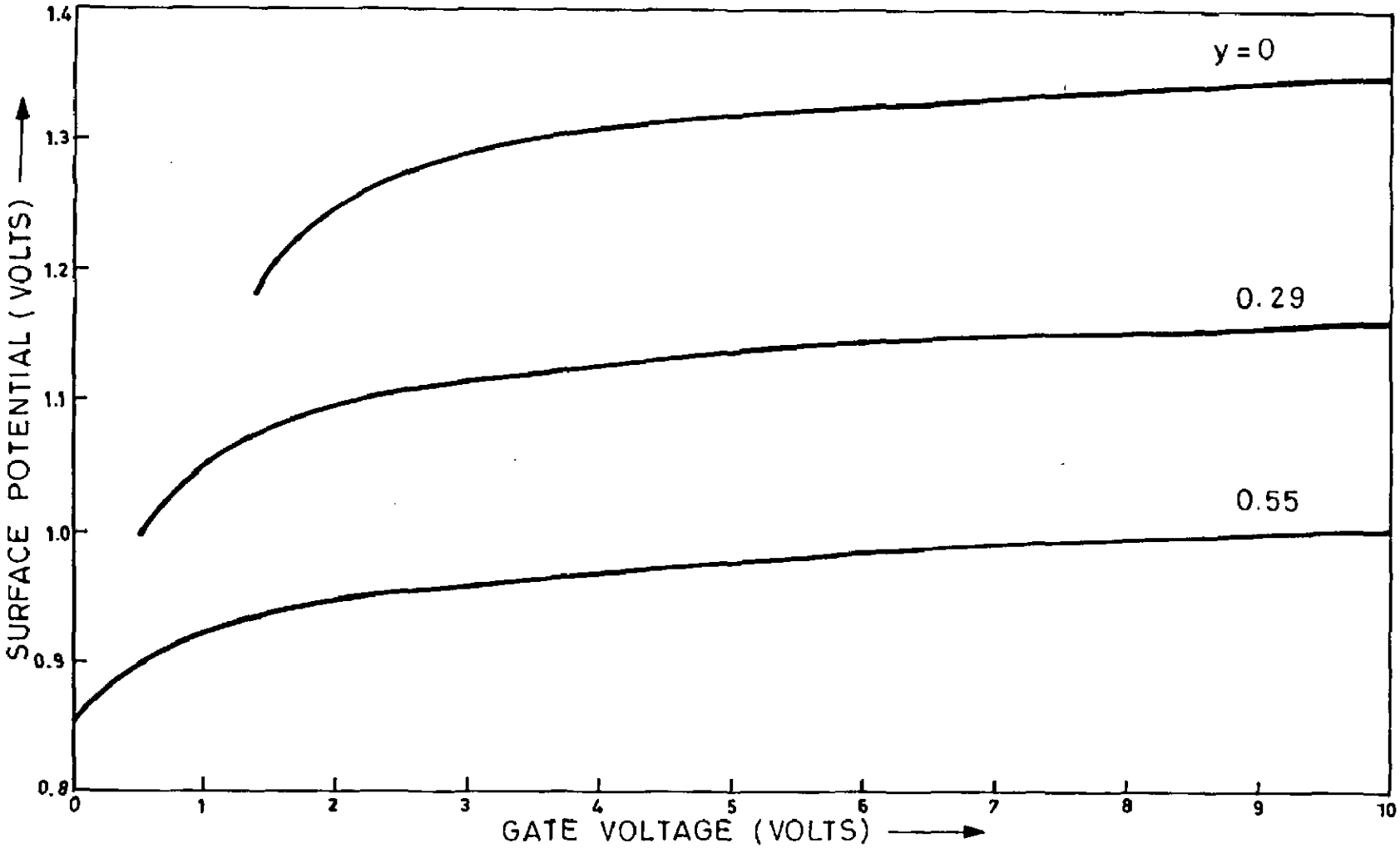

FIG. 3.5 SURFACE POTENTIAL AS FUNCTION OF APPLIED GATE VOLTAGE WITH y AS A PARAMETER.

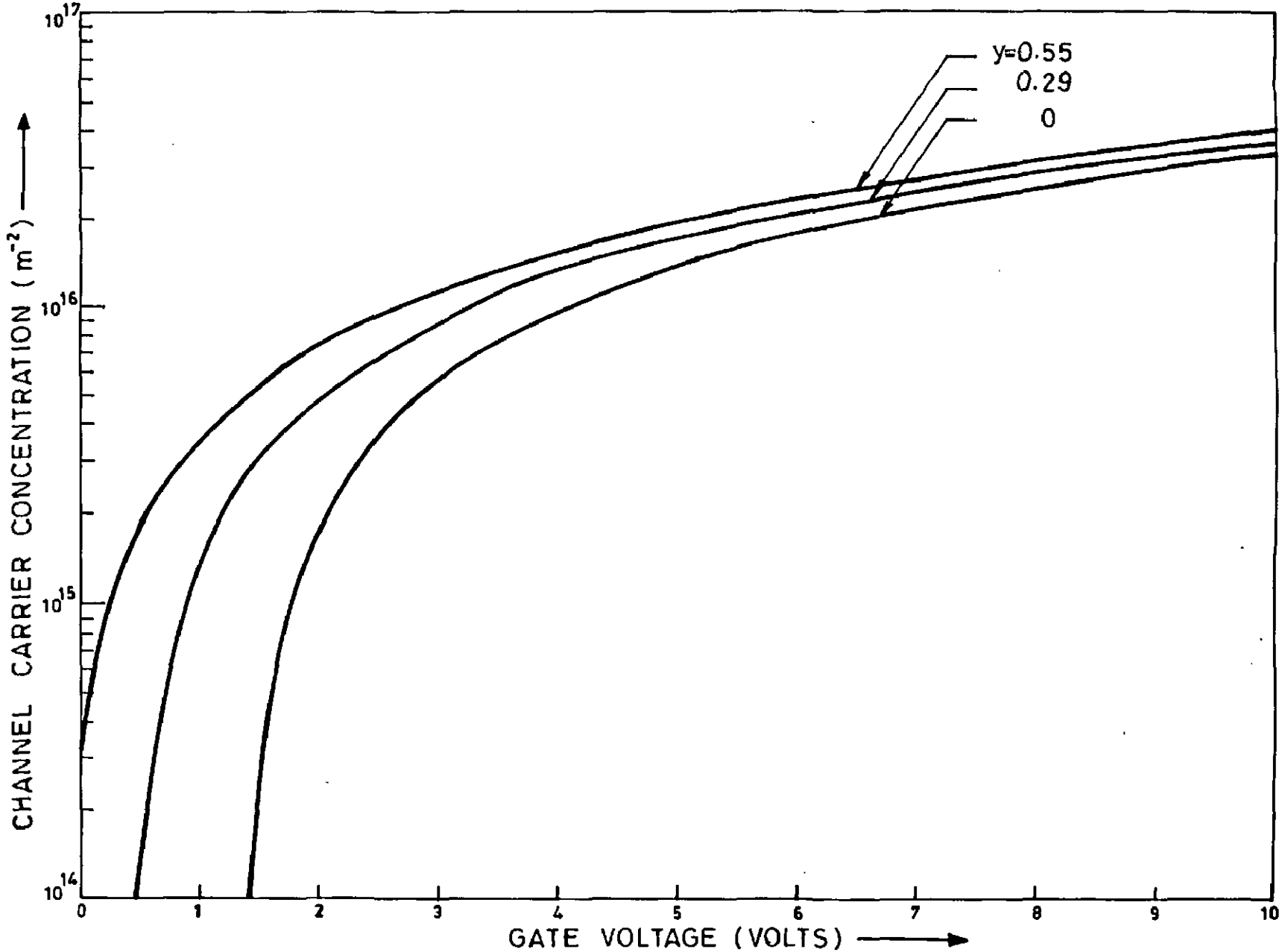

FIG. 3.6 CHANNEL CARRIER CONCENTRATION AS FUNCTION OF GATE VOLTAGE WITH y AS A PARAMETER.

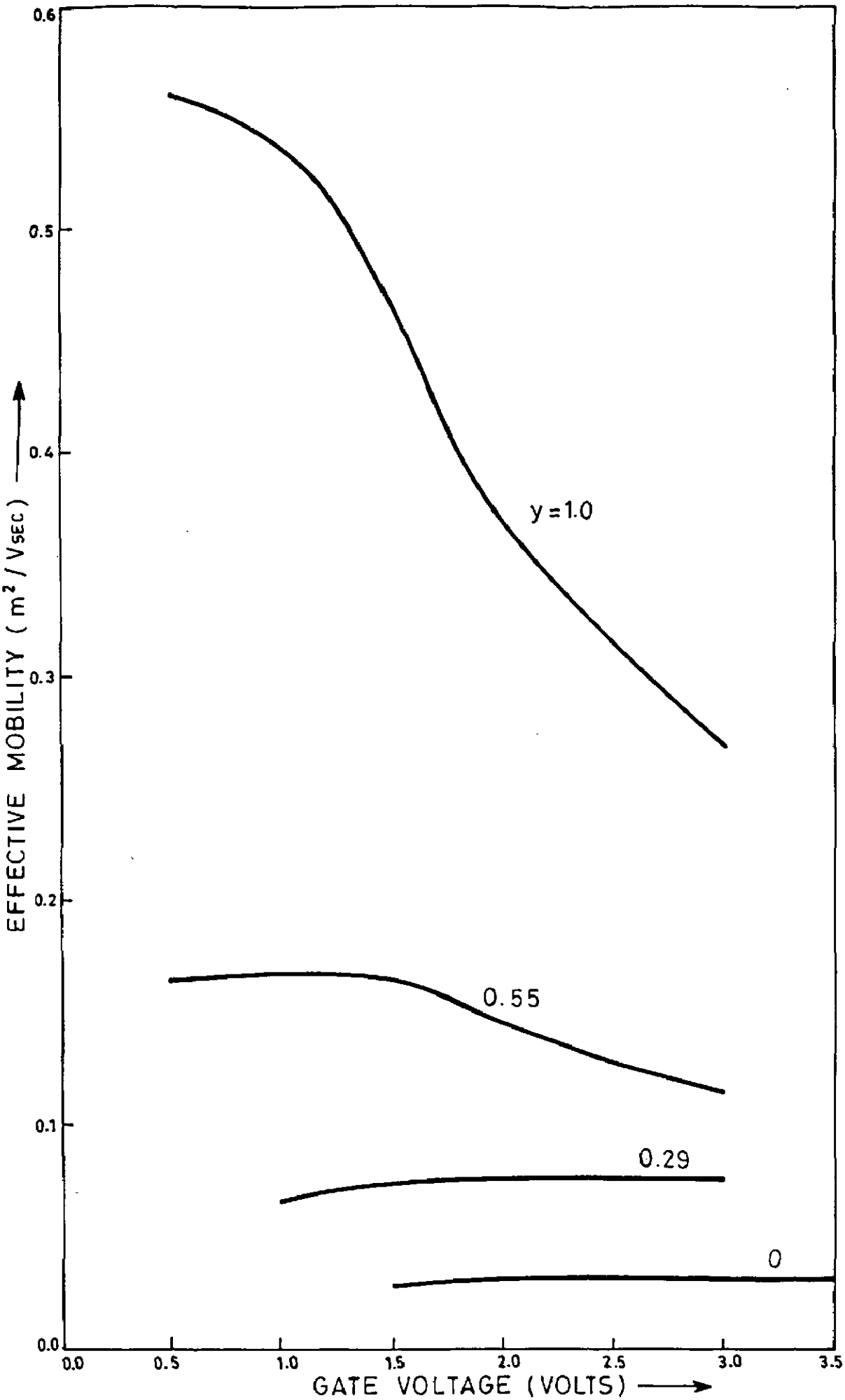

FIG. 3.7 GATE VOLTAGE DEPENDENCE OF EFFECTIVE MOBILITY WITH y AS A PARAMETER.

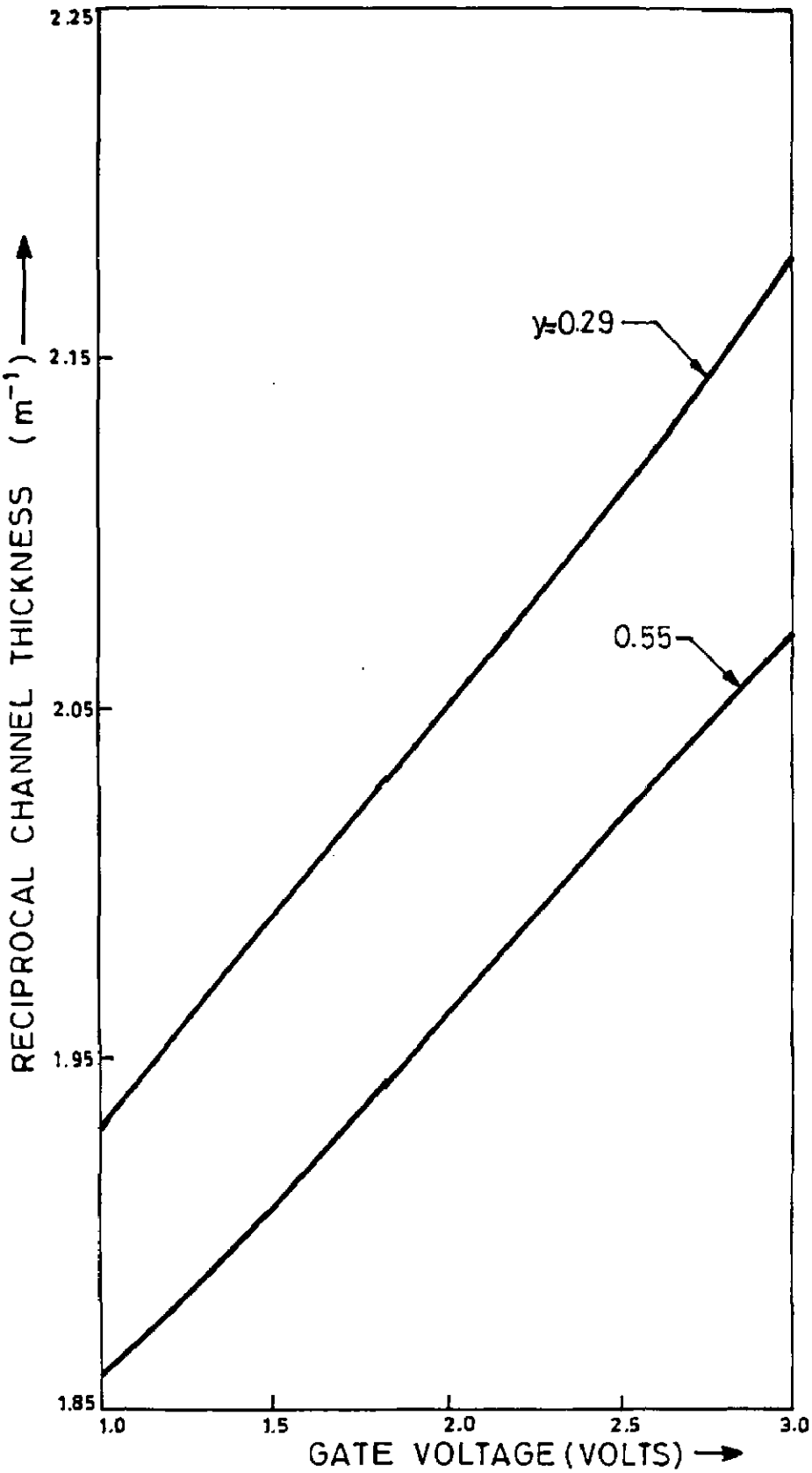

FIG. 3.8 GATE VOLTAGE DEPENDENCE OF RECIPROCAL OF CHANNEL THICKNESS .

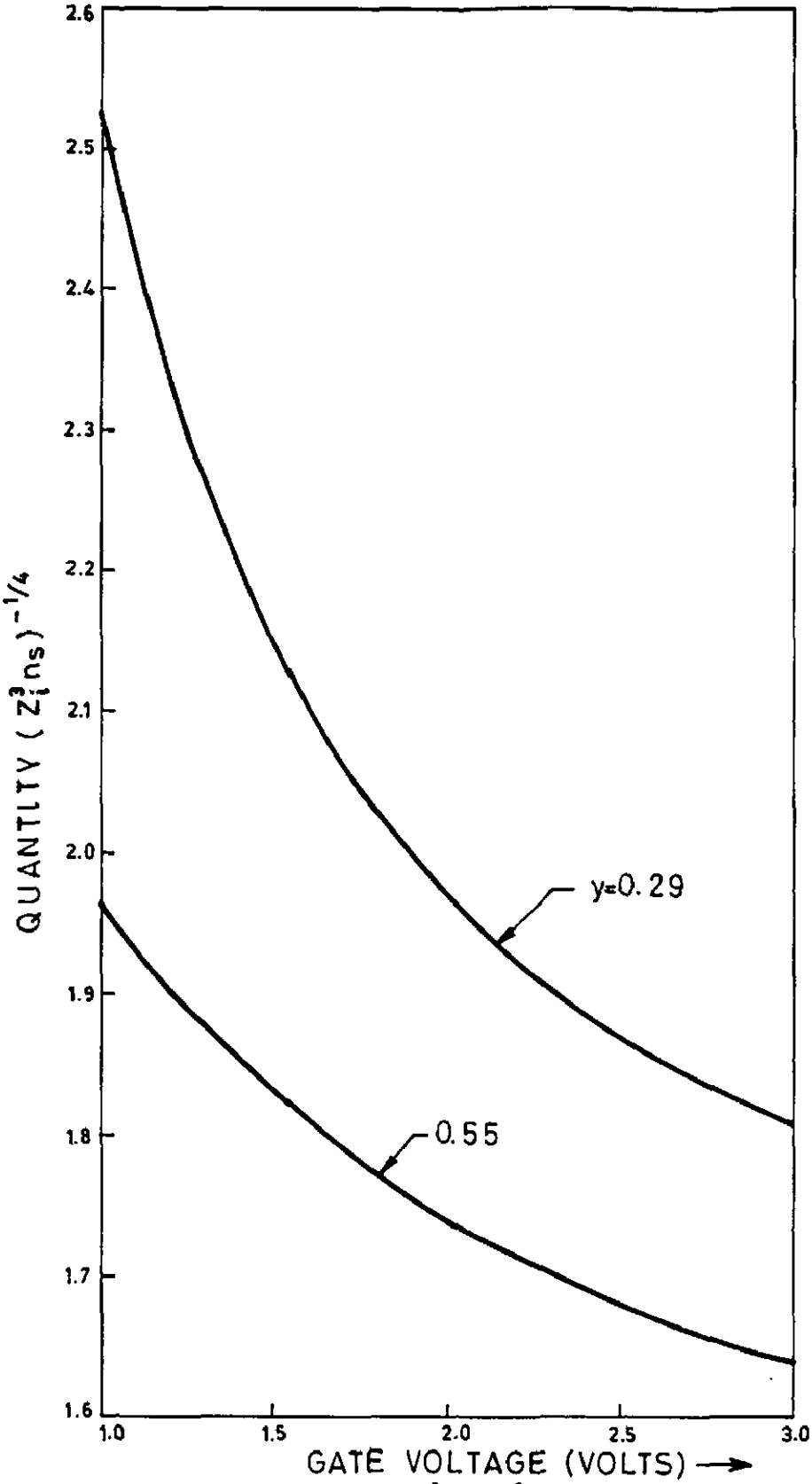

FIG. 3.9 THE QUANTITY $(Z_i^3 n_s)^{-1/4}$ AS FUNCTION OF GATE VOLTAGE.

chapter IV

ANALYSIS OF n-CHANNEL INVERSION-MODE InGaAs MISFET

4.1 INTRODUCTION

The analysis presented in the third chapter highlights many important characteristics of an n-type inversion layer formed in InGaAsP and InGaAs MIS-structures. While this provides sufficient information for assessment of InGaAs as a material for MIS device application, a complete analysis of the operation of an InGaAs MISFET is in order. To meet this end, a long-channel MISFET-model and its application for the complete characterization of n-channel inversion-mode InGaAs MISFET is presented in this chapter. The proposed model for InGaAs MISFET, is 2-dimensional in the sense that it accounts for the influences of both normal and lateral electric fields on the inversion channel formed between the source and drain.

The drain current-voltage behaviour of silicon MISFETs have been extensively studied by many authors. The simple MISFET theory based on gradual channel approximation [185] is applicable for computation of drain characteristics of the InGaAs MISFETs. This approach, however, has its own limitation. More accurate models taking the non-linearity of source-drain field and this field dependence of channel mobility have yielded useful results [9,11,12,14,19,20,21,56,143,159,164,174,228,232,234,237,251]. As the electric fields in the channel largely depend on the device dimensions, two distinct types of models, namely, the long-channel and short-channel models have been developed. The long-channel models [268] as reported in the literature are mostly meant for silicon MISFETs and have ignored the diffusion component

of the drain current. This omission make such a model applicable to only linear and saturation regions irrespective of the semiconductor in which the device is housed. Considering the fact that electron diffusion constant is high in InGaAs, the present model takes into account both drift and diffusion components of the drain current. The inclusion of the diffusion component broadens the scope of its application. Its application for subthreshold analysis, however, would require a suitable subthreshold mobility model. In this chapter, the MISFET-model developed is used to extract effective mobility parameters of an InGaAs MISFET. The model is further used to study the drain characteristics of InGaAs MISFETs. These characteristics are also compared with those of InP and Si MISFETs. The model is then used to analyse the dependence of InGaAs MISFET drain characteristics on the substrate doping level. The distribution of potential, electric field, carrier density and effective mobility variation along the channel of n-channel inversion-mode InGaAs MISFET, are all analysed in this chapter.

4.2 THE BASIC MODEL

The drain current of a MISFET is constituted by two components, that is the drift and diffusion components. If the hole current in the channel is neglected, then for an n-channel inversion-mode MISFET, the drain current I_{DS}, can be expressed as

$$I_{DS} = Z\, q\, N(x)\, \mu_{eff}\, E(x) + (Z\, q/\beta)\, \mu_{eff}\, [dN(x)/dx] \qquad (4.1)$$

where

Z = channel width

x = distance along the channel with source as reference

$N(x)$ = electron concentration (per unit area)

μ_{eff} = effective mobility of the carriers

$E(x)$ = lateral electric field along the channel.

As both gate and drain voltage induces carriers in the channel, the electron concentration $N(x)$, has two components, namely, gate induced carrier density $N_g(x)$, and drain induced density $N_d(x)$. Thus,

$$N(x) = N_g(x) + N_d(x) \tag{4.2}$$

The electrons are mainly confined within a bulk Debye length L_D, from the surface and the electron density decreases rapidly as distance from the surface increases. From these considerations it is a good approximation, if the normal electric field is assumed to be constant throughout the width of the channel. On this basis it can be easily shown that [268]

$$N_d(x) = \epsilon_s \epsilon_0 L_D \frac{d^2\phi_s(x)}{dx^2} \tag{4.3}$$

where

$$\phi_s(x) = \phi_{s0} + V(x) \tag{4.4}$$

ϕ_{s0} being the surface potential at the source and $V(x)$ is the potential due to source-drain voltage drop at a distance x from the source.

Thus, from (4.3) and (4.4)

$$N_d(x) = \epsilon_s \epsilon_0 L_D \frac{d^2V}{dx^2} \tag{4.5}$$

substituting (4.2) in (4.1)

$$I_{DS} = Z\, q\, \mu_{eff} [\, N_g(x) + N_d(x)\,]\, E(x)$$

$$+ \frac{Z\ q}{\beta}\ \mu_{eff}\left(\frac{dN_g(x)}{dx} + \frac{dN_d(x)}{dx}\right) \qquad (4.6)$$

It can be seen from (4.6) that the drain current is dependent on the effective carrier mobility of the channel. The influence of normal field on the effective mobility has been discussed in chapter III, from consideration of various physical processes involved. As previously mentioned, strating from Matthiessen's rule one can express effective mobility by (3.33). It is possible to show that (3.23) and (3.33) can be combined to express the effective mobility in the form [201]

$$\mu_{eff} = \frac{\mu_0}{\left[\ 1 + \theta_s(V_G - V_T) + \left(\frac{Q_B}{\epsilon_s \epsilon_0\ E_c}\right)\ \right]} \qquad (4.7)$$

where

μ_0 = low-field mobility

$$\theta_s = C_i\ /\ 2\ \epsilon_s \epsilon_0\ E_c \qquad (4.8)$$

and

E_c = is a critical normal electric field at which the effective mobility is half of the low-field value μ_0.

The values of the parameters μ_0, θ_s and E_c are difficult to justify rigrously from purely theoretical point of view. Thus, it is a common practice to evaluate these from experimental measurements (37).

Substituting (4.7), (4.8) and (4.5) in (4.6) and

$$E(x) = dV/dx \qquad (4.9)$$

it can be shown that with rearrangement of terms

$$I_{DS}\left[\ (1+\theta_s(V_G - V_T) + \frac{Q_B}{\epsilon_s\epsilon_0 E_c}\right] =$$

$$Zq\mu_0\left[\left[N_g(x) + \frac{\epsilon_s\epsilon_0 L_D}{q}\frac{d^2V}{dx^2} + \frac{1}{\beta}\frac{dN_g(x)}{dV}\right]\frac{dV}{dx} + \frac{\epsilon_s\epsilon_0 L_D}{q\ \beta}\frac{d}{dx}\left(\frac{d^2V}{dx^2}\right)\right] \quad (4.10)$$

It is obvious that (4.10) is a second order non-linear differential equation. Integrating over the distance between source and an arbitary point 'x',

$$\frac{\epsilon_s\epsilon_0 L_D}{q\ \beta}\int_0^x \frac{d}{dx}\left(\frac{d^2V}{dx^2}\right)dx = \frac{1}{Zq\ \mu_0}\int_0^x I_{DS}\left[1 + \theta_s(V_G - V_T) + \frac{Q_B}{\epsilon_s\epsilon_0 E_c}\right]dx$$

$$-\int_0^V \left[N_g(x) + \frac{\epsilon_s\epsilon_0}{q}\frac{d^2V}{dx^2} + \frac{1}{\beta}\frac{dN_g(x)}{dV}\right]dV \quad (4.11)$$

On the basis of (3.19), gate induced carrier concentration may be expressed as

$$N_g(x) = \frac{1}{q}\left[C_i[V_G' - \phi_{s0} - V(x)] - \sqrt{2\epsilon_s\epsilon_0 q\ N_A[\phi_{s0} + V(x) - \frac{1}{\beta}]}\right] \quad (4.12)$$

From (4.12)

$$\frac{1}{\beta}\frac{dN_g(x)}{dV} = -\frac{1}{q\beta}\left[C_i + \sqrt{\frac{\epsilon_s\epsilon_0 q\ N_A}{2}}\ [\phi_{s0} + V(x) - \frac{1}{\beta}]^{-1/2}\right] \quad (4.13)$$

Substituting (4.12) and (4.13) in (4.11)

$$\frac{\epsilon_s\epsilon_0}{q\ \beta}\left[\frac{d^2V}{dx^2} - \left(\frac{d^2V}{dx^2}\right)_{x=0}\right] = \frac{I_{DS}}{Z\ q\ \mu_0}\ [1 + \theta_s(V_G - V_T) + \frac{Q_B}{\epsilon_s\epsilon_0 E_c}]\ x -$$

$$\frac{1}{q}\left[\int_0^V C_i(V_G' - \phi_{s0})dV - \int_0^V C_i V dV + \sqrt{2\epsilon_s\epsilon_0 q N_A}\int_0^V (\phi_{s0} + V - \frac{1}{\beta})^{1/2} dV + \right.$$

$$\left. \frac{1}{q\beta}\left[\int_0^V C_i dV + \frac{\sqrt{\epsilon_s\epsilon_0 q N_A}}{2}\int_0^V (\phi_{s0} + V - \frac{1}{\beta})^{-1/2} dV\right] - \frac{\epsilon_s\epsilon_0 L_D}{q}\int_0^V \frac{d^2V}{dx^2} dV\right]$$

(4.14)

Since at source (i.e. x=0), the drain induced carrier concentration $N_d(x)$ is negligibly small. Therefore, at source end, we can safely assume $(d^2V/dx^2)_{x=0} = 0$. With this assumption, after rearrangement of terms (4.14) may be written as

$$\frac{1}{\beta}\frac{d2V}{dx^2} = \frac{I_{DS}\left[(I + \theta_s(V_G - V_T) + \frac{Q_B}{\epsilon_s\epsilon_0 E_c}\right]}{Z\,\mu_0\,\epsilon_s\,\epsilon_0\,L_D} x$$

$$- \frac{V\,C_i}{\epsilon_s\epsilon_0 L_D}\left(V_G' - \phi_{s0} - \frac{1}{\beta} - \frac{V}{2}\right)$$

$$+ \frac{2}{3}\frac{\sqrt{2\,\epsilon_s\epsilon_0 q\,N_A}}{\epsilon_s\epsilon_0 L_D}\left[(\phi_{s0} + V - \frac{1}{\beta})^{3/2} - (\phi_{s0} - \frac{1}{\beta})^{3/2}\right]$$

$$+ \frac{\sqrt{2\,\epsilon_s\epsilon_0 q\,N_A}}{\epsilon_s\epsilon_0 L_D}\left[(\phi_{s0} + V - \frac{1}{\beta})^{1/2} - (\phi_{s0} - \frac{1}{\beta})^{1/2}\right]$$

$$- \frac{1}{2}\left[\left(\frac{dV}{dx}\right)^2 - \left(\frac{dV}{dx}\right)^2_{x=0}\right] \qquad (4.15)$$

The quantity, $(dV/dx)_{x=0}$ is electric field at the source, where x=0, V=0 and $d^2V/dx^2=0$. Furthermore, at and in the vicinity of the source N(x) is more or less constant [$dN(x)/dx \approx 0$]. Thus (4.10) may be reduced to the form

$$[N_g(x) + \frac{1}{\beta}\frac{dN_q(x)}{dV}](\frac{dV}{dx})_{x=0} = \frac{I_{DS}[1+\theta_s(V_G - V_T) + \frac{Q_B}{\epsilon_s\epsilon_0 E_c}]}{Z\, q\, \mu_0} \quad (4.16)$$

Substituting (4.12) and (4.13) in (4.16)

$$(\frac{dV}{dx})_{x=0} = [\, I_{DS}(1+\theta_s(V_G - V_T) + (Q_B/\epsilon_s\epsilon_0 E_c)]\Big[Z\mu_0[C_i(V_G' - \phi_{s0}) - \sqrt{2\epsilon_s\epsilon_0 q\, N_A(\phi_{s0} - \frac{1}{\beta})} - \frac{C_i}{\beta} - \frac{1}{2\beta}\sqrt{2\epsilon_s\epsilon_0 q\, N_A(\phi_{s0} - \frac{1}{\beta})}]\Big]^{-1} \quad (4.17)$$

The source electric field as given by (4.17) is thus a function of drain current.

The Eq. (4.15) is a second order differential equation of the form

$$f'' = f(x,V,V') \quad (4.18)$$

which may be solved numerically with the initial conditions such as $x = 0$, $V = 0$ and $(dV/dx)_{x=0}$ = source field (4.19)

The equation, however, cannot be further simplified to obtain a closed form solution. In the present analysis, the numerical solution of (4.15) is obtained by the application of Runge-Kutta method [192]. The calculation error has been confined to a tolerable limit by a process of error estimation and subsequent error minimization, over the entire range from source ($x = 0$) to drain ($x = L$) (Appendix I). For a given set of gate voltage V_G and drain current I_{DS}, potential V, at each point along the channel is obtained by step by step solution of (4.15). The potential at $x = L$, is taken to be the drain-source potential drop V_{DS}. In a similar 2-dimensional MISFET analysis, Zhang and Schroder [268] obtained a pair of first order differential

equation. In their approach,the diffusion component of the drain current was neglected. The difficulty with these equations, were that, when solved numerically, one of the equation was not convergent near the drain, while the other was not convergent near the source. The problem was solved by solving the first equation from the source end upto a point $x = L_s$, where the equation diverges. From this point onwards, the second equation was solved till the drain end was reached. No such problem has been encountered in the case of (4.15). This second order differential equation can be solved continuously from the source end, right upto the drain end to obtain potential distribution (as discussed subsequently) all along the channel. As only one equation needs to be handled, the present model therefore offers some computational advantages.

4.2.1 Effective Mobility Parameter Extraction

The application of (4.15) and (4.17) in MISFET analysis requires the knowledge of the value of effective mobility parameters μ_0, θ_s and E_c. The parameters are generally estimated by elaborate experimental work [37,97,201]. These approaches are laborious and require extensive device fabrication facilities. As such laboratory facilities were not available for the present work, a simpler method has been adopted. This method essentially uses drain characteristics of a MISFET with a very small drain-source potential drop.

Substituting (4.8) in (4.7)

$$\mu_{eff} = \frac{\mu_0}{\left[1 + \frac{C_i(V_G - V_T)}{2\,\epsilon_s\epsilon_0 E_c} + \frac{Q_B}{\epsilon_s\epsilon_0 E_c}\right]} \tag{4.20}$$

For $V_G \gg V_{DS}$, a commonly used expression for drain conductance is [220], thus

$$g_d = \frac{\mu_{eff}\ Z\ C_i}{L}(V_G - V_T) \tag{4.21}$$

Substituting (4.20) in (4.21)

$$g_d = \frac{\mu_0\ Z\ C_i}{L} \frac{(V_G - V_T)}{\left[1 + \frac{C_i(V_G - V_T)}{2\,\epsilon_s\epsilon_0 E_c} + \frac{Q_B}{\epsilon_s\epsilon_0 E_c}\right]} \tag{4.22}$$

Thus, if g_{d1} and g_{d2} are drain conductances at gate voltage of V_{G1} and V_{G2} respectively, then from (4.22) it follows that

$$\frac{g_{d1}}{g_{d2}} = \frac{E_c + \frac{C_i(V_{G2} - V_T)}{2\,\epsilon_s\,\epsilon_0} + \frac{Q_B}{\epsilon_s\,\epsilon_0}}{E_c + \frac{C_i(V_{G1} - V_T)}{2\,\epsilon_s\,\epsilon_0} + \frac{Q_B}{\epsilon_s\,\epsilon_0}} \tag{4.23}$$

Thus, from experimentally obtained g_d vs. V_G plot and using (3.14), it is possible to estimate E_c from (4.23). The accuracy of E_c-estimation, however, will depend on how small is the value of V_{DS} for which the g_d vs. V_G plot is obtained. Knowing E_c, it is then possible to calculate μ_0 and θ_s from (4.22) and (4.8) respectively.

As the estimated value of E_c is used for the determination of μ_0 and θ_s, the accuracy of the estimation of the last two parameters will also depend on the accuracy of E_c-estimation. Obviously, the estimated values of E_c, μ_0 and θ_s will vary with V_{G1} and V_{G2} and for that matter there will be variations in the estimated values, with the range of V_G over which V_{G1} and V_{G2} are

selected. In order to demonstrate this and also to find a viable approach for the extraction of the mobility parameters, the experimental data for an $In_{0.53}Ga_{0.47}As$ MISFET as reported by Gardner et al. [71] is taken as an example. For this MISFET, the estimated μ_0, θ_s and E_c are tabulated in Table 4.1. The estimations are made over five different gate voltage ranges. E_c value for any range is the mean value obtained from several different pairs of V_{G1} and V_{G2} over the range.

Table 4.1: Estimated Value of θ_s, E_c and μ_0 over Different Ranges of Gate Voltage.

Set No.	Gate Voltage Range (V)	$\theta_s (V^{-1})$	E_c (V/m)	$\mu_0 (m^2/V\text{-}s)$
1	4.5 - 5.0	0.28	5.99×10^6	0.71
2	3.9 - 5.0	0.28	6.05×10^6	0.74
3	2.9 - 4.0	0.26	6.46×10^6	0.79
4	2.5 - 4.0	0.25	6.72×10^6	0.79
5	1.9 - 4.0	0.25	6.80×10^6	0.85

The dependence of the estimated values of the mobility parameters on the gate voltage range, is clearly indicated by Table 4.1. This makes it imperative to ascertain the most accurate set of values. To achieve this the drain current variation with drain-source voltage for gate voltage of 3 V is calculated by solving (4.15) for each set of the mobility parameter values. The values of the various parameter involved in (4.15) as taken from Gardner et al.[71] are as follows:

$L = 1.5\ \mu m$

$Z = 150\ \mu m$

$C_i = 3.94 \times 10^{-4}\ Fm^{-2}$

$V_T = +\ 0.4\ V$

$N_A = 4 \times 10^{22}\ m^{-3}$

$T = 300\ K$

The effective gate voltage V_G', is determined by (3.5). The flat-band voltage is determined by using (3.30) and the known value of threshold voltage. The material parameters of ϵ_s and n_i are taken from Gardner et al. [71]. The depletion layer charge density Q_B is determined from (3.14) and (4.4). Fig. 4.1 shows the I_{DS} - V_{DS} characteristics thus obtained for the different sets of mobility parameters along with the experimental data of Gardner et al. (approximated by the circles). It can be seen that over the lower range of V_{DS}, very good fit with the experimental data is obtained using mobility parameters determined over the widest range of gate voltage (1.9 - 4.0 V). There is, however, some deviation occurs for higher values of V_{DS}. The model which forms the basis of (4.15) is essentially a long-channel model. In this model many of the high-field effects that are likely to take place at higher drain-source and gate-source bias voltages have been ignored. The deviation of the calculated results from the experimental ones are likely to be caused by the failure of the model to account for these high-field effects.

In order to confirm the influence of the high-field effect in the calculated I_{DS} - V_{DS} characteristics, curves are plotted for four different gate voltages in Fig. 4.2. Mobility parameters calculated over the gate voltage range of 1.9 - 4.0 V are taken. It is clear that deviation from experimental data not only

increases with drain-source voltage, but it also increases with increase in gate voltage. Several factors may be attributed to the deviations. First, (4.4) is valid for $V_G >> V_{DS}$. Thus, as V_{DS} is increased to fairly large values, the Eq. (4.22) becomes less accurate. Secondly, it may be seen in Fig. 4.2, that for lower gate voltages, the calculated characteristics agrees well with the experimental results. At lower gate voltages, the normal field is also of a lower magnitude. It has been shown by Coen and Muller [37], that at lower normal fields the velocity saturation effect sets in at higher drain-source voltage. As the present model does not incorporate the velocity saturation effect in drain current estimation, the calculated results are less precise at higher drain-source voltage when gate voltage is high. Thus, for the estimation of the mobility parameters by the present model, calculations at lower gate voltage is recommended. The best fit at gate voltage of 2 and 1 V (Fig. 4.2) indicates that the mobility parameters for the MISFET treated are :

$$\mu_0 = 0.85 \text{ m}^2/\text{V-s}$$

$$E_c = 6.8\text{x}10^6 \text{ V/m}$$

$$\theta_s = 0.25 \text{ V}^{-1}$$

and the effective mobility is

$$\mu_{eff} = 0.85 \; / \; [\; 1 + 0.25(V_G - V_T) \; + (Q_B/6.8\text{x}10^6 \epsilon_s \epsilon_0)\;] \qquad (4.24)$$

Thus after determining Q_B from (3.14) and (4.4) and ϵ_s from Gardner et al.[71], the effective mobility for the InGaAs MISFET considered may be calculated from (4.24). The close agreement between the calculated $I_{DS} - V_{DS}$ characteristics with experimental data for several gate voltage (Fig. 4.2) indicate that the method adpoted for effective mobility parameter estimation is fairly

accurate. The agreement between calculated results and the experimentally obtained data also proves that (4.15) is a valid equation. It may be noted that the critical electric field for the InGaAs MISFET is of the same order as it is observed to be in the case of silicon MISFETs [201].

4.3 ANALYSIS OF THE DRAIN CHARACTERISTICS OF InGaAs MISFET

The MISFET-model developed in the preceding section involves low-field mobility. The low-field mobility is known to be a function of doping level in the substrate material. The approach adopted so far is one of determining the low-field mobility from experimental data. In order to make the model more self-sufficient, in this section a suitable low-field mobility expression is incorporated in the MISFET-model. This modified model is then used to study the dependence of drain conductance of an InGaAs MISFET on substrate impurity concentration.

4.3.1 A More Generalized Effective Mobility Expression

The drain characteristics of a MISFET is essentially the I_{DS} - V_{DS} characteristics. Another important output parameter is the drain conductance. It is well known that the doping level in the channel influences the output characteristics as well as the drain conductance. As can be seen from (4.15) and the basic definition of drain conductance [220], effective mobility plays an important role in determining the output characteristics and the drain conductance. In subsection 4.2.1, method for the estimation of effective mobility parameters has been described. The effective mobility expression thus obtained is true for the particular

device considered [71]. For the analysis of the output characteristics a generalized effective mobility experssion is essential. Keeping this in view, in this section the basic effective mobility expression (4.7) is given a more generalized form, so that the effect of channel doping level can be appropriately accounted for. To meet this end the factors affecting the effective mobility parameters of μ_0, θ_s and E_c are critically examined.

All effective mobility parameters to some extent are dependent on the process technology employed. The parameter E_c depends on the surface conditions which in turn is determined by wafer processing and insulator deposition or growth process [259]. As given by (4.8), the parameter θ_s is dependent on E_c and hence it is also a surface dependent parameter. These two parameters do not depend on the impurity concentration. However, the low-field mobility μ_0, to some extent is dependent on impurity concentration. This dependence is because of its relationship with bulk mobility μ_B, as [259]

$$\mu_0 = \mu_B \; / \; [\; 1 + \mu_B \, K' \, \{ \, N_{fs} + \int_0^{\phi_s(x)} D_{it}(\phi) d\phi \; \}] \qquad (4.24)$$

where

N_{fs} = number density of all charges at the insulator-semiconductor interface that include oxide and interface charges

D_{it} = density of interface state (per unit area)

K' = a constant dependent on permittivity of interfacial layer and the mobility effective mass.

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$$\mu_0 = \mu_B \; / \; [\; 1 + \mu_B \, K' \, \{ \, N_{fs} + \int_0^{\phi_s(x)} D_{it}(\phi) d\phi \, \}] \qquad (4.24)$$

where

N_{fs} = number density of all charges at the insulator-semiconductor interface that include oxide and interface charges

D_{it} = density of interface state (per unit area)

K' = a constant dependent on permittivity of interfacial layer and the mobility effective mass.

It is clear from (4.25) that the low-field mobility besides being dependent on lattice and impurity scattering, is dependent on interface state and oxide charge density. These two quantities are mainly dependent on the device technology employed. Thus, the low-field mobility like the other two effective mobility parameters is technology dependent. Assuming that a factor p takes into account, the effect of the scattering due to the interface charge and oxide charge, μ_0 as given by (4.25) may be written as

$$\mu_0 = \mu_B/[1 + \mu_B\, p] \tag{4.26}$$

$$\text{where } p = K' \left[N_{fs} + \int_0^{\phi_s(x)} D_{it}(\phi)\,d\phi \right] \tag{4.27}$$

A simple relation between μ_B and impurity concentration N_A, is [97]

$$\mu_B = \mu_L/[1 + (N_A/10^{23})^{1/2}] \quad m^2/V\text{-}s \tag{4.28}$$

where μ_L is the lattice mobility in $m^2/V\text{-}s$ and N_A is in m^{-3}. Substituting (4.28) in (4.26)

$$\mu_0 = \mu_L/[1 + \mu_L p + (N_A/10^{23})^{1/2}] \quad m^2/V\text{-}s \tag{4.29}$$

Thus, μ_0 can be determined from (4.29), provided μ_L, p and N_A are known. Such a calculation is generally avoided as it is difficult to estimate p from experimental data. However, for analytical purposes, (4.29) is useful if the scattering factor p, is appropriately approximated. In section (4.2), μ_0 is estimated to be 0.85 for an InGaAs MISFET of $N_A = 4\text{x}10^{22}\ m^{-3}$ and $\mu_B = 0.9$

m^2/V-s [71]. Using these data in (4.29) and μ_L = 1.0 m^2/V-s [71], p is calculated to be 0.25. It is worth noting that the value of p depends on the process technology of the device.

4.3.2 Effect of Channel Doping on Drain Characteristics

The analysis presented in subsection 4.2.1 shows that the Eq. (4.15) may be solved to obtain the I_{DS} - V_{DS} characteristics of MISFET with fair amount of accuracy (Fig. 4.2). The characteristic curves shown in Fig. 4.2, however, were for an InGaAs MISFET, the carrier mobility of which is given by (4.24). Following the same method of solving (4.15) by Runge-Kutta method using (4.29) for estimation of μ_0 drain current as function of drain-source voltage is obtained for an n-channel InGaAs MISFET of the following parameters : L = 3 μm, Z = 300 μm, N_A = 10^{22} m^{-3} and C_i = 3.84 Fm^{-2}. Flat-band voltage of - 2.5 V is taken (Appendix II). The threshold voltage V_T, is determined from (3.1) and (3.30). The calculated threshold voltage comes out to be - 0.9023 V.

In order to find the effective mobility parameter u_0, the lattice mobility μ_L, is assumed to be 1.0 m^2/V-s [71]. Using (4.29), μ_L is calculated to be 0.76 m^2/V-s for N_A = 10^{22} m^{-3}. Assuming good insulator semiconductor interface properties, p is taken as 0.13. Thus from (4.29) μ_B is obtained as 0.69 m^2/V-s. The critical field is assumed to be 10^7 V/m, the parameter θ_s is calculated to be 0.17 V^{-1}.

Fig. 4.3 shows the I_{DS} - V_{DS} characteristics of the MISFET for three different gate voltage. A comparison with Fig. 4.2 shows

that the basic nature of the characteristics are identical. However, for the device of larger geometery (Fig. 4.3), the operating points are at much higher levels of current and voltages.

In order to study the effect of channel doping level on the I_{DS} - V_{DS} characteristics of an InGaAs MISFET, the calculations are carried out for different impurity concentrations, keeping other parameters same. Fig. 4.4 shows the effect of channel doping level on the I_{DS} - V_{DS} characteristics at gate voltage of 3 V. It can be seen that for a higher impurity concentration, the saturation drain current and the drain voltage at pinch-off are both lower. Furthermore, if the channel doping level is low, then the level of drain current may be extremely high. Thus, if a lightly doped substrate is to be used, the gate area should be reduced to keep the current level within control.

Fig. 4.5 compares the current-voltage characteristics of InGaAs MISFET with MISFETs formed in InP and silicon substrates. All the three devices are assumed to have the same channel length, channel width, channel doping and gate insulator capacitance which are respectively 3 μm, 300 μm, 10^{22} m^{-3} and 3.84×10^{-4} Fm^{-2}. It is further assumed that the factor p is 0.13 for both InGaAs and InP MISFET. To determine μ_0 for InP, a knowledge of lattice mobility of the semiconductor is essential. With the same mobility data as used by Shinoda and Kobayashi [202,204] and (4.29), the lattice mobility for InP estimated as 0.608 m^2/V-s. Thus from (4.29) and for p = 0.13, μ_0 is 0.44 m^2/V-s. Assuming E_c to be 10^7 V/m, θ_s for the InP MISFET as obtained from (4.8) is 0.78 V^{-1}. For a silicon MISFET of channel doping 10^{22} m^{-3}, μ_0 is typically 0.1046 m^2/V-s

[259]. For $E_c = 10^7$ V/m, θ_s is 0.182 V^{-1}. Typical values for flat-band voltages for InP and silicon devices are selected on the basis of discussion given in Appendix II. These values are - 4.7 V and - 0.84 V respectively for InP and silicon MISFETs. The threshold voltages of the two devices as calcutated by the aid of (3.1) and (3.30) yields - 2.014 V and 1.1078 V for InP and silicon respectively.

Fig. 4.5 shows that the $I_{DS} - V_{DS}$ characteristics of the three devices differ mainly in two aspects. First, the current level in InGaAs MISFET is highest while in silicon MISFET it is the lowest. The drain voltage at pinch-off is highest for the InGaAs MISFET and it is lowest for the silicon MISFET. The InP MISFET has these two quantities in between those of the other two MISFETs. From simple considerations, in the linear region the drain current of a MISFET may be approximated by [220].

$$I_{DS} = \frac{Z}{L} \mu_{eff} C_i \left[\left(V_G' - 2\phi_B - \frac{V_{DS}}{2} \right) V_{DS} - \frac{2}{3} \sqrt{\frac{2 \epsilon_s \epsilon_0 q N_A}{C_i}} \left[(V_{DS} + 2\phi_B)^{1/2} - (2\phi_B)^{1/2} \right] \right] \quad (4.30)$$

It is obvious from (4.30) that, the rate of change of drain current with drain voltage is directly proportional to the effective carrier mobility in the channel. From the discussion presented in subsection 3.4.2 and the mobility parameter evaluated for the InGaAs, InP and silicon MISFETs, it is clear that, InGaAs has the highest effective mobility followed in descending order by InP and silicon. Thus higher drain current and its rapid rise in

the drain voltage for InGaAs is mainly due to high effective carrier mobility in the channel.

When pinch-off occurs, the gate induced carrier density at the drain vanishes. At the drain, this carrier density $N_g(L)$, may be approximated by [220]

$$q\, N_g(L) = -\,(V_G' - V_{DS} - 2\phi_B)\, C_i + \sqrt{2\,\epsilon_s\epsilon_0 q\, N_A (V_{DS} + 2\phi_B)} \qquad (4.31)$$

If V_{DP} is the drain voltage at pinch-off, then for $V_{DS} = V_{DP}$, $N_g(L) = 0$ and [220]

$$V_{DP} = V_G' - 2\phi_B - K^2 \left[\left(1 + \frac{2V_G}{K^2} \right)^{1/2} - 1 \right] \qquad (4.32)$$

where

$$K = \frac{1}{C_i} \sqrt{\epsilon_s\epsilon_0 q\, N_A} \qquad (4.33)$$

Substituting (3.5) in (4.33)

$$V_{DP} = V_G - V_{FB} - 2\phi_B - K^2 \left[\left(1 + \frac{2V_G}{K^2} \right)^{1/2} - 1 \right] \qquad (4.34)$$

It is now evident from (4.34) that the difference in drain voltage for pinch-off in the cases of the three MISFETs under consideration is governed by three parameters, viz. V_{FB}, ϕ_B and K. The flat-band voltage depends on the oxide charge and interface state densities and the modified work function. ϕ_B depends on intrinsic carrier concentration and K depends on the semiconductor permittivity. These parameters as calculated from the relevant equations and experimental observations (Appendix II) are given in Table 4.2.

Table 4.2 : Flat-Band Voltage, Bulk Fermi Potential and Threshold Voltage in InGaAs, InP and Si System.

Substrate	V_{FB}(V)	ϕ_B(V)	K(V)	V_T(V)
InGaAs	- 2.51	0.25	1.12	- 0.9023
InP	- 4.71	0.54	1.10	- 2.014
Silicon	- 0.84	0.35	1.07	+ 1.078

As indicated by (4.34), a negative flat-band voltage gives rise to higher V_{DP} than positive ones. As seen in Table 4.2, for all the three devices, the flat-band voltage is negative. This is mainly because of negative modified work function. In the III - V compound MISFETs, the flat-band voltage are generally of higher magnitude, owing to the comparatively poorer quality of insulator-semiconductor interface properties. High interface state density in the compound semiconductor is mainly responsible for higher flat-band voltage. On the other hand, the silicon MIS-technology has advanced so much that the interface charge density is minimized to yeild devices of very small flat-band voltage.

Fig. 4.5, shows very low value of V_{DP} for silicon MISFET. This is also confirmed by (4.34) and Table 4.2. Low flat-band voltage and high bulk potential ϕ_B, result in a very low V_{DP} in silicon devices. For InP MISFET, the flat-band voltage is very high. This is because of high interface state density. However, an extremely high bulk potential compensates the effect of flat-band voltage in determining V_{DP}. InGaAs MISFET having a moderate

flat-band voltage has a high V_{DP} because of lower bulk potential which results from a very high intrinsic carrier concentration. The effect of permittivity is, however, more or less same for all the three cases.

Current saturation occurs when drain voltage is increased beyond pinch-off. Even in the saturation region, a MISFET is known to have some increase in drain current with drain voltage, although it is very small. This effect is most predominant in the case of InGaAs MISFET and least for silicon MISFET (Fig. 4.5). The significant variation of drain current with drain voltage in InGaAs MISFET is indicative of a high drain conductance in saturation region. Fig. 4.6, shows the variation of drain conductance

$$g_d = [dI_{DS}/dV_{DS}]_{V_{GS} = \text{constant}} \tag{4.35}$$

for an InGaAs MISFET. These plots are obtained for the MISFET treated in subsection 4.2.2, by the use of (4.15). The drain conductance curves are similar to what has been reported for silicon MISFETs. The high drain conductance is because of high effective mobility of the electrons.

4.4 ELECTRIC POTENTIAL VARIATION ALONG THE CHANNEL AND ITS EFFECT

As the drain current flows through the channel, it produces a potential drop across its path. The channel conductance being a non-linear function of distance from the source, potential along the channel also has a non-linear variation with the lateral electric field along the channel. These facts have been confirmed by analysis of silicon MISFETs [268]. This section deals with

analysis of the electric potential variation along the channel of an InGaAs MISFET. Its effects on other channel parameters are also studied.

4.4.1 Potential and Field Variation along the Channel

In order to find the nature of potential variation along the channel of InGaAs MISFET, (4.15) is solved for MISFET parameters used in subsection 4.3.2. Fig. 4.7 shows the variation of potential along the length of the MISFET for a drain current of 25 mA, at gate voltage 2, 3 and 4 V. It can be seen that at high gate voltage (e.g. V_G = 4 V), the variation is more or less linear. Some of the MISFET analysis make the assumption of a linear potential variation along the channel [164]. Thus, it may be concluded that such an assumption is true for higher gate voltages. As seen in Fig. 4.7 decrease in gate voltage produces deviation from the linear relationship between potential V(x) and distance x from the source. According to the existing theories which mainly deal with silicon devices, near the drain, in general gate induced carrier density is low. The decrease in gate voltage results in more significant fall in gate induced charge density as the drain is approached. The result is lower channel conductivity at points closer to the drain. The decrease in conductivity with increasing x is itself a non-linear function of x. As a result, for lower gate voltages, rate of increase of V(x) rises towards the drain in a non-linear fashion. It is therefore in order to investigate whether the same reason leads to sharp increase in V(x) near the drain end.

From a knowledge of the variation of potential V(x) along

the channel it is possible to determine the gate induced carrier concentration $N_g(x)$, by the application of (4.12). As already mentioned in section (4.2), besides the gate induced carrier in the channel of a MISFET, there are carriers induced due to flux coming out of the drain contact. The concentration of these drain induced carriers can be calculated from (4.3). Both gate induced and drain induced carrier concentration have been calculated as function of relative distance from source for the InGaAs MISFET, presently considered. Fig. 4.8 shows the variation of the induced carriers along the channel. Considering the nature of variation of the drain current with drain voltage and the conduction mechanism responsible for this, the operation of a MISFET is broadly classified into two regions. These are the linear region and the saturation region. The two regions of operation are reported by the *pinch-off condition. Pinch-off occurs when gate induced* carrier concentration at the drain end of the MISFET just vanishes. According to MISFET theory, the gate induced carrier concentration is reduced to zero by the expanding drain depletion layer at high drain voltage. Calculations show that for the MISFET presently considered, pinch-off at a gate voltage of 3 V occurs when drain current is 46.2 mA. The distribution of gate induced and drain induced carrier concentration at pinch-off are shown in Fig. 4.8. In this figure, carrier distribution for drain current levels of 25 mA and 50 mA are also shown, which are respectively operations in linear and beyond (saturation) regions.

The plots in Fig. 4.8 show that, gate induced carrier concentration in general decreases as the drain is approached. For operation at low drain current levels (i.e. in the linear region), the rate of fall of gate induced carrier concentraion decreases

towards the drain as the drain current (drain voltage) is increased, vanishing at the drain at the critical drain current of 46.2 mA. The drain voltage at pinch-off is 2.1 V. As the drain current (or drain voltage) is increased the pinch-off point (vanishing gate induced carrier concentration) recedes away from the drain. The solid curve labelled 'beyond pinch-off' in Fig. 4.8 is an example of this effect. The variation of the drain induced carrier concentration is a reversal of the manner of variation of the gate induced carrier concentration. As only a few flux lines from the drain contact are able to reach the source contact, the drain induced carrier concentration is minimum at the source. As drain is approached, the drain induced carrier concentration gradually increases with increase in the density of flux emanating from drain. The drain induced carrier concentration reaches its maximum at the drain end when the gate induced carrier concentration is minimum.

An interesting point that may be noted is that, with increase in drain current, that is drain voltage, the gate induced carrier concentration decreases while the drain induced carrier concentration increases. The cause is of course, the increase in electric flux density emanating from drain and terminating within the channel. However, the drain induced carrier concentration is relatively lower than the gate induced carrier concentration till the pinch-off point is reached. Between the pinch-off point and the drain contact, carriers are all drain induced ones. In a similar analysis of silicon MISFET Zhang and Schroder [268] also obtained similar result.

In order to compare the induced carrier distribution in

silicon and InGaAs MISFETs, calculations are carried out for a silicon MISFET of same gate length, gate width, channel doping and insulator capacitance (silicon MISFET treated in Fig. 4.5). Fig. 4.9 shows the induced carrier concentrations in linear region, at pinch-off and beyond pinch-off are similar for InGaAs and silicon MISFETs. The major difference is in the level of the concentrations both of gate induced and drain induced curves. The silicon MISFET has relatively lower level of concentrations.

The factors affecting gate induced carrier concentration have been extensively discussed in subsection 3.3.1. Material prameters such as intrinsic Debye length and surface potential influence the gate induced carrier concentration. For the same effective gate voltage V_G', an InGaAs MISFET has a higher gate induced carrier concentration than a comparable silicon MISFET, (Fig. 3.3). Furthermore, the flat-band voltage for an InGaAs MISFET is generally higher than that of a silicon MISFET. With the presently available technology. This is mainly because of large surface state density that are encounters in the III - V compound semiconductor surfaces. Keeping this in view all calculations are carried out in the present work have taken $V_{FB} = -2.51$ V for InGaAs and $V_{FB} = -0.84$ V for silicon MISFET. Thus, for a gate voltage of 3 V, the effective gate voltage for the InGaAs MISFET is 5.51 V while it is 3.84 V for silicon MISFET. The higher effective gate voltage for InGaAs MISFET further adds to the cause for higher gate induced carrier concentration in InGaAs MISFET. Like the gate induced carrier concentration, the drain induced carrier concentration is also higher in InGaAs MISFET. The reason for this is that the permittivity of InGaAs being higher, the drain flux density penetrating into the channel is higher in

comparison with what it is in silicon MISFET. Moreover, as indicated by (4.3), the drain induced carrier concentration also depends on the rate of change of the slope of the V(x) vs. x profile. As can be seen in Fig. 4.7, this slope is quite considerable in the case of InGaAs MISFET, while it is not so for silicon MISFETs [268].

As a result of higher induced carrier concentration in InGaAs MISFET, the total induced carrier concentration is also higher for these MISFETs than their silicon counterpart (Fig. 4.10). The relatively higher drain current in InGaAs MISFETs is partly because of the high induced carrier concentration. Fig. 4.10, also shows that the total induced carrier concentration falls towards the drain contact in a non-linear fashion. This confirms that the non-ninear rise in potential V(x) towards the drain contact is caused by the same phenomenon as in case of silicon MISFETs.

The rate of change of V(x) with x is the lateral electric field in the channel. The variation of lateral electric field along the channel of the n-channel inversion-mode MISFET, under consideration are shown in Fig. 4.11. Obviously, for reasons mentioned above, the lateral electric field is a non-linear function of distance from the source and its increase is more and more rapid as the drain is approached, especially for lower gate voltage. Fig. 4.12, illustrates the variation of lateral electric field under the three distinct operating conditions. As can be seen, the electric field variation is nominal for low drain currents in the linear region. The variation becomes more and more significant as the pinch-off condition is approached. Beyond

pinch-off or in the saturation region, the lateral field increases very rapidly as the distance from the source increases. This is the reason why, drain induced carrier concentration also rises very sharply when the device is operated in the saturation region. The electric field variation in the channel of the silicon counterpart of the InGaAs MISFET is shown in Fig. 4.13. It shows that the nature of variation of the lateral electric field in the channel of the two devices are identical. However, because of comparatively lower electric potential in the channel of the silicon device and lower rate of change of the potential with distance from the source, the lateral electric field is comparatively lower.

4.4.2 Effective Mobility Variation along the Channel

The entire analysis presented so far centres around Eq. (4.15), where effective mobility of the form of (4.7) has been used. In most MISFET analysis [201,248,268] the same form of effective mobility is used. However, in these analysis, the effect of channel potential variation in the effective mobility is ignored. The variation of channel potential V(x), in fact has an effect on effective mobility μ_{eff}, through the involvement of depletion charge density Q_B.

Substituting (4.4) in (3.14)

$$Q_B = q N_A L_D [2 \{\beta(\phi_{s0} + V(x)) - 1 \}]^{1/2} \qquad (4.36)$$

Thus, as seen in (4.36), Q_B is a function of x, through its dependence on V(x). Substituting (4.36) in (4.7)

$$\mu_{eff} = \mu_0 \; / \; [\; 1 + \theta_s (V_G - V_T) + C' \; \{\; 2 \; (\beta(\phi_{s0} + V(x)) - 1 \;)\}^{1/2}] \qquad (4.37)$$

where $C' = q \, N_A \, L_D \; / \; \epsilon_s \, \epsilon_0 \, E_c$

It is now clear from (4.37) and Fig. 4.7 that μ_{eff} should decrease towards the drain end. Fig. 4.14 illustrates the variation of μ_{eff} with distance from the source end for the InGaAs MISFET considered in the last section. In general, μ_{eff} decreases as the drain is approached. The rate of decrease is enhanced with reduction in gate voltage. This is because, at lower gate voltages, potential V(x) increases more rapidly towards the drain end. To be more precise, the fall in mobility is a result of increase in impurity scattering near the drain. This is a consequence of fall in free carrier concentration near the drain. In regions away from the drain, high induced carrier concentration screens the impurity ions, thereby minimizing mobility degradation due to impurity scattering. Fig 4.10 shows that with increase in drain current depletion region increases. This causes increased impurity scattering near the drain for operation at higher drain currents (Fig. 4.15).

Thus it is concluded that at lower gate voltages and higher drain currents, especially beyond the pinch-off condition, it is essential to take into account the effect of increase in depletion charge density on effective mobility. Fig. 4.16 shows the variation of effective mobility in the silicon counterpart of the InGaAs MISFET under consideration. It shows that the effect of lateral field on effective mobility in silicon MISFETs is similar to what it is in the InGaAs MISFETs.

4.5 CONCLUSION

A MISFET-model based on the various physical mechanism involved in the operation of a MISFET has been developed. The model takes into consideration the two dimensional effects resulting from gate and drain fields. Unlike the previous models, the diffusion current in the channel is also taken into consideration. The model yields a working equation, that can be solved numerically to obtain drain characteristics, distribution of induced carriers in the channel and also the variation of electric potential and lateral field in the channel.

A commonly used effective mobility model is used. The parameters of effective mobility are determined by a simple method that requires no elaborate laboratory experimentations. Mobility parameter extraction shows that for InGaAs MISFETs the depletion field required to make the effective mobility to be half of the low-field mobility is of the same order as that for the silicon MISFETs.

A comparison of I_{DS} - V_{DS} characteristics of InGaAs, InP and silicon MISFETs of comparable dimensions, channel doping and insulator capacitance, show that, InGaAs MISFETs operate at higher drain current. Furthermore, the drain voltage at pinch-off is higher in InGaAs MISFETs. This is partly because of insulator-semiconductor interface properties. The InGaAs MISFET also have higher induced carrier density and lateral electric field along the channel. The analysis also takes into consideration the effect of depletion charge on effective mobility of the carriers. It is seen that as a consequence of the increase

in electric potential towards the drain contact, the effective mobility degrades as the drain is approached. Similar effects also take place in the silicon devices.

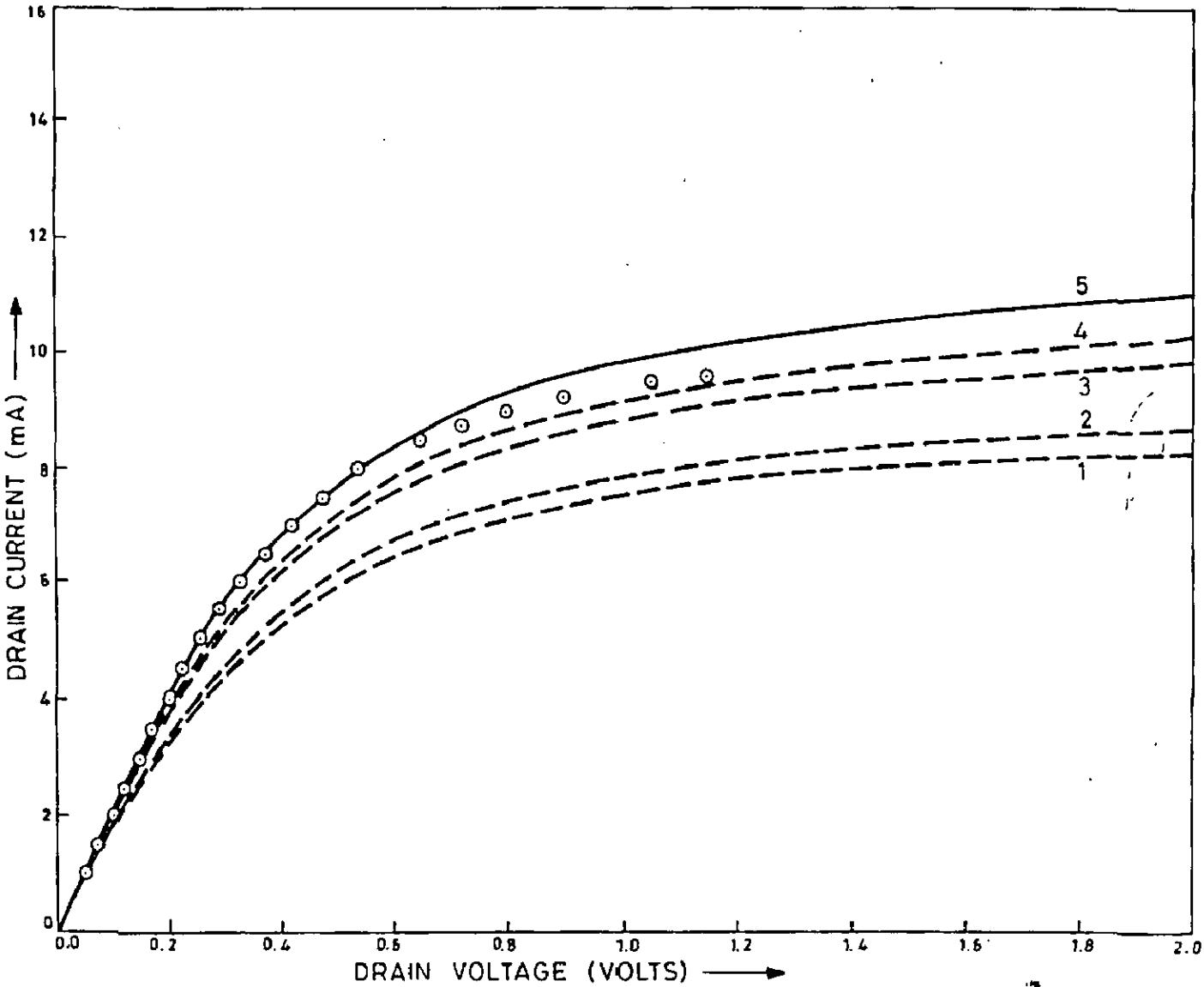


FIG. 4.1 DRAIN CURRENT VOLTAGE CHARACTERISTICS OF InGaAs MISFET FOR DIFEERENT μ_o, θ_s AND E_c VALUES FOR GATE VOLTAGE (= 3V) EXPERIMENTAL DATA TAKEN FROM REF[71] ARE INDICATED BY CIRCLES.

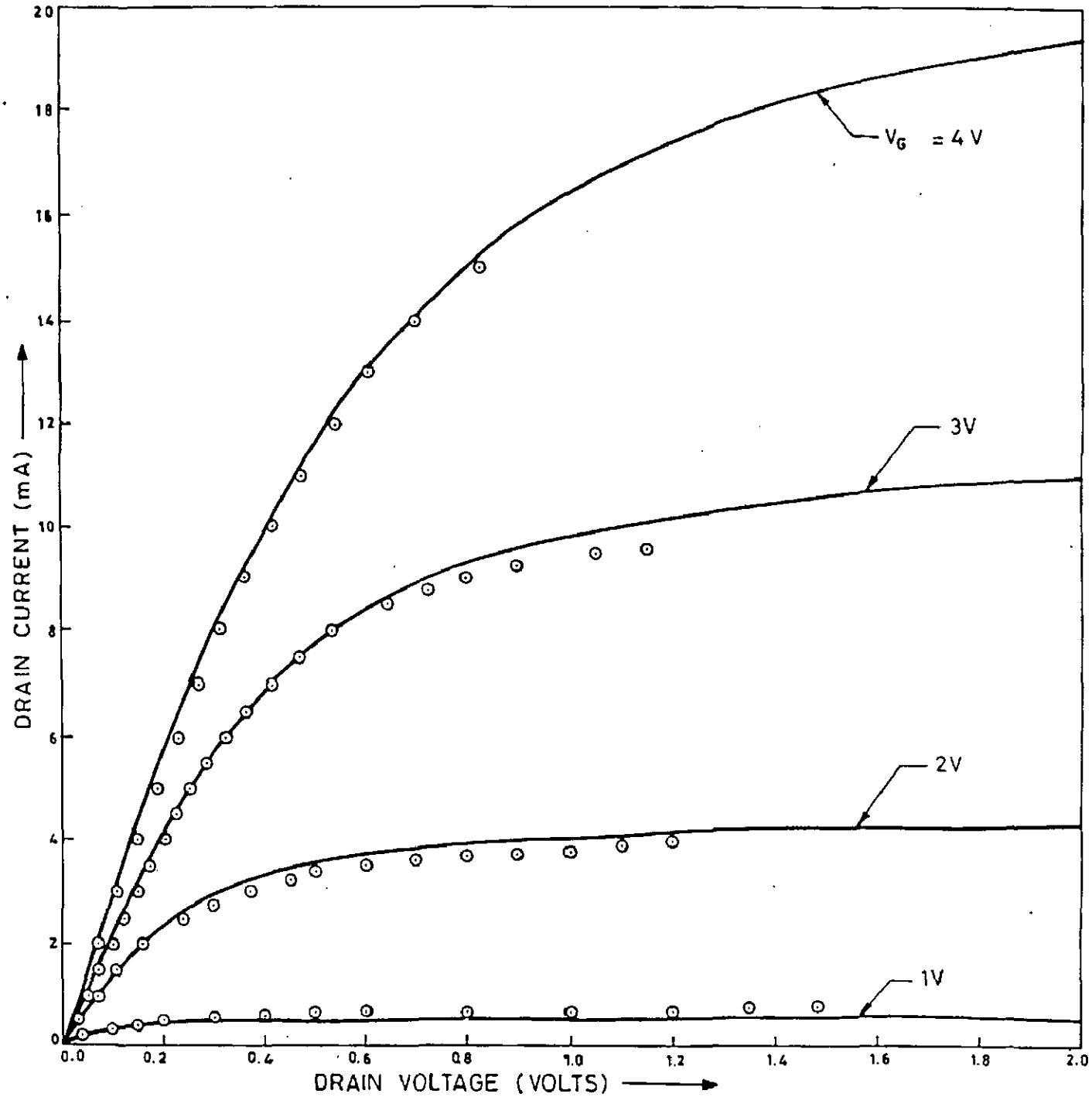


FIG. 4.2 DRAIN CURRENT-VOLTAGE CHARACTERISTICS OF N-CHANNEL INVERSION-MODE InGaAs MISFET FOR FOUR DIFFERENT GATE VOLTAGE THE CIRCLES INDICATE EXPERIMENTAL DATA TAKEN FROM REF.[71].

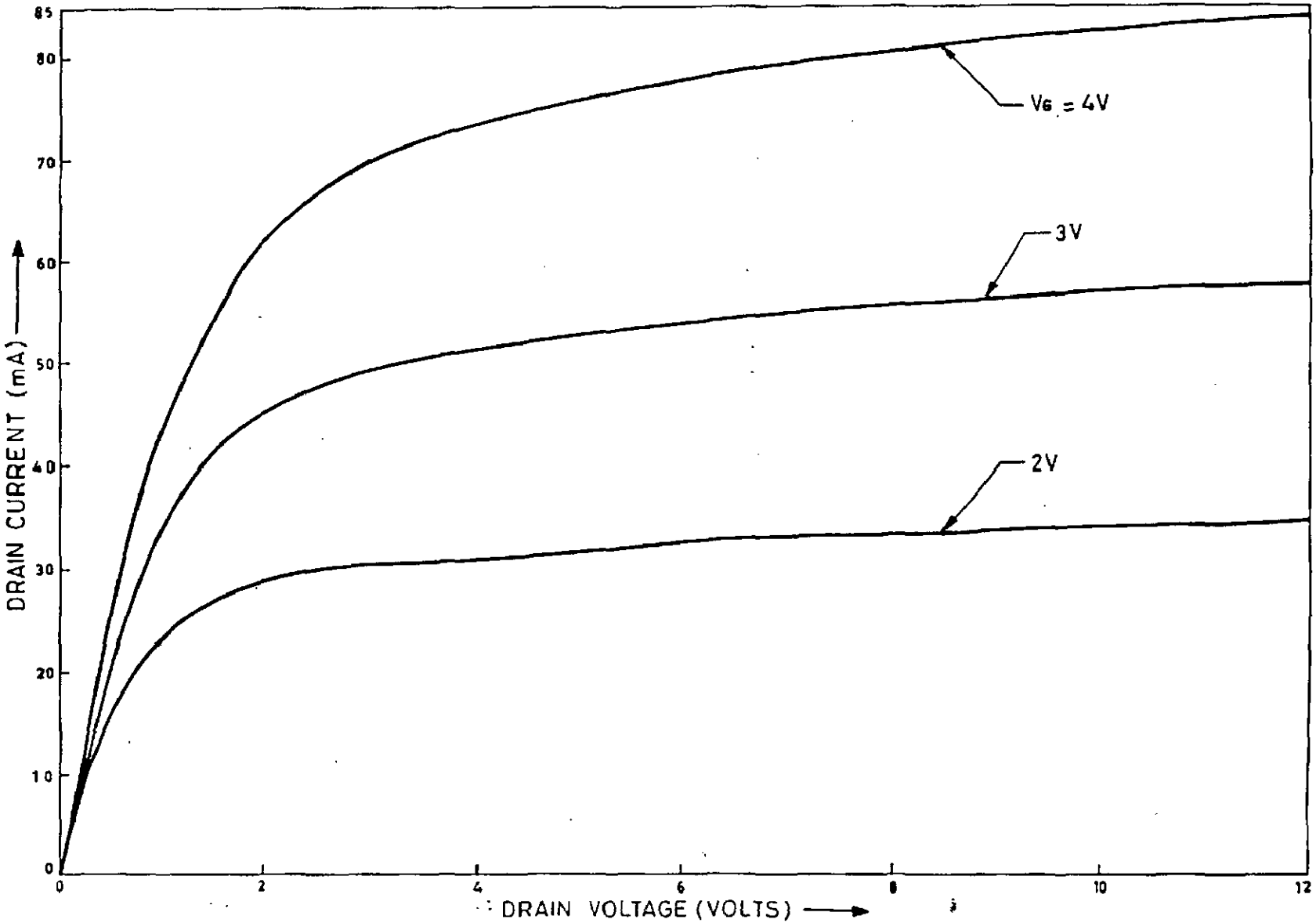


FIG. 4.3 DRAIN CURRENT AS FUNCTION OF DRAIN VOLTAGE WITH GATE VOLTAGE AS A PARAMETER IN InGaAs MISFET ($L = 3\,\mu m$, $Z = 300\,\mu m$, $N_A = 10^{22}\,m^{-3}$).

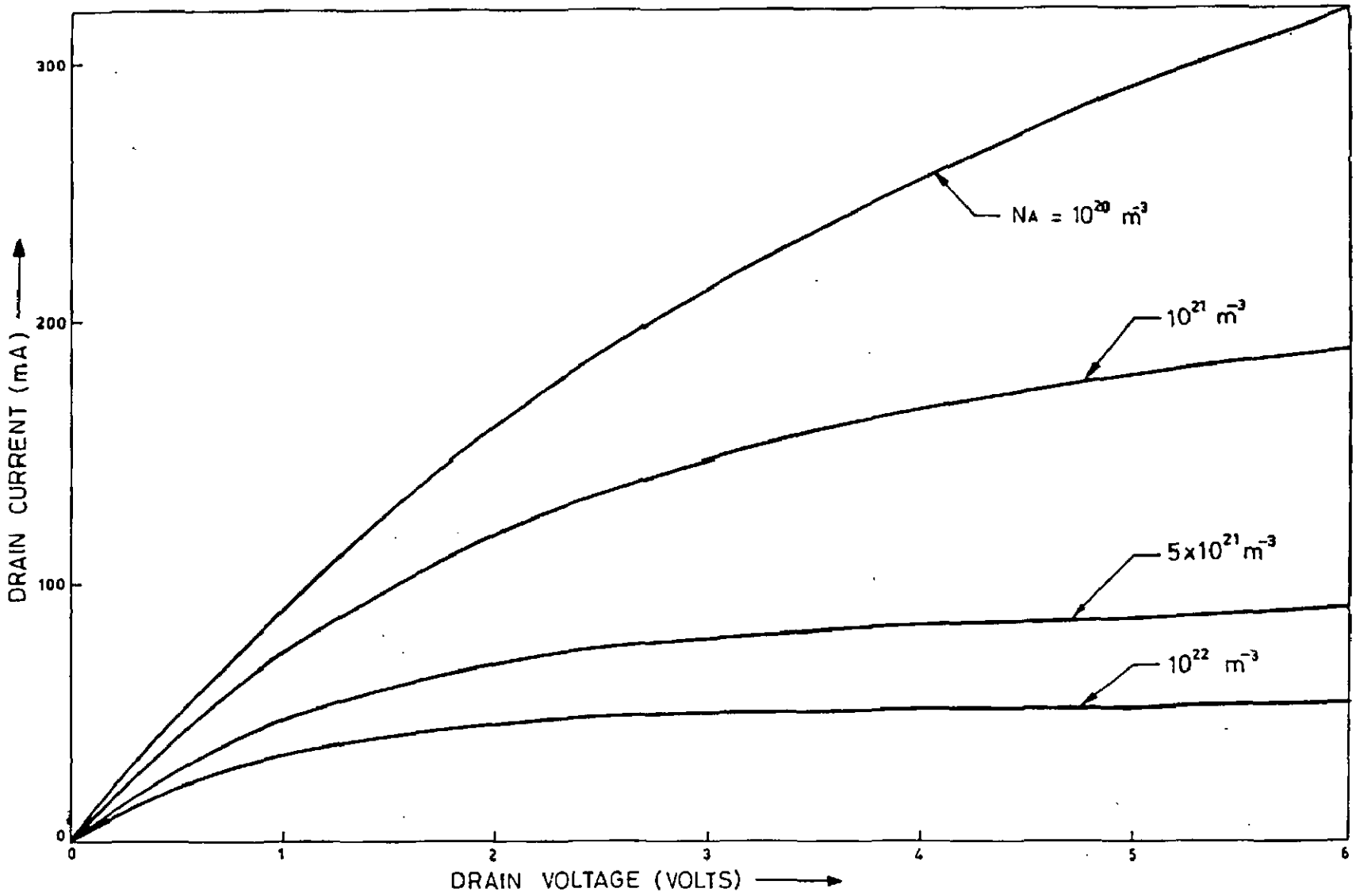


FIG. 4.4 DRAIN CURRENT AS FUNCTION OF DRAIN VOLTAGE IN InGaAs MISFET WITH CHANNEL DOPING AS PARAMETER AND $V_G = 3V$.

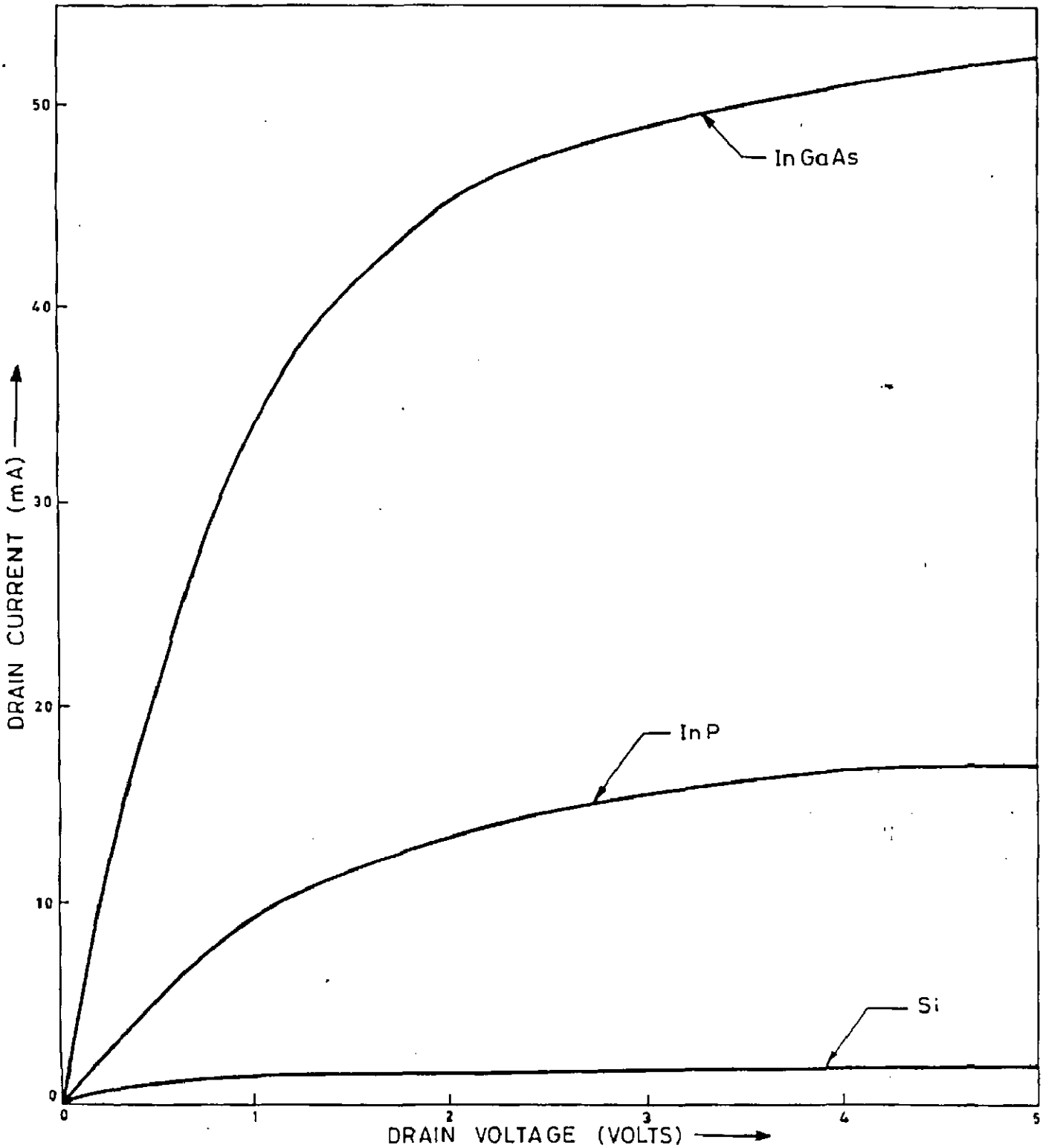


FIG. 4.5 $I_{DS}-V_{DS}$ CHARACTERISTICS OF InGaAs, InP AND Si MISFETS AT $V_G = 3V$ FOR ALL MISFETS $L = 3\mu m$, $Z = 300\ \mu m$ AND $N_A = 10^{22}\ m^{-3}$.

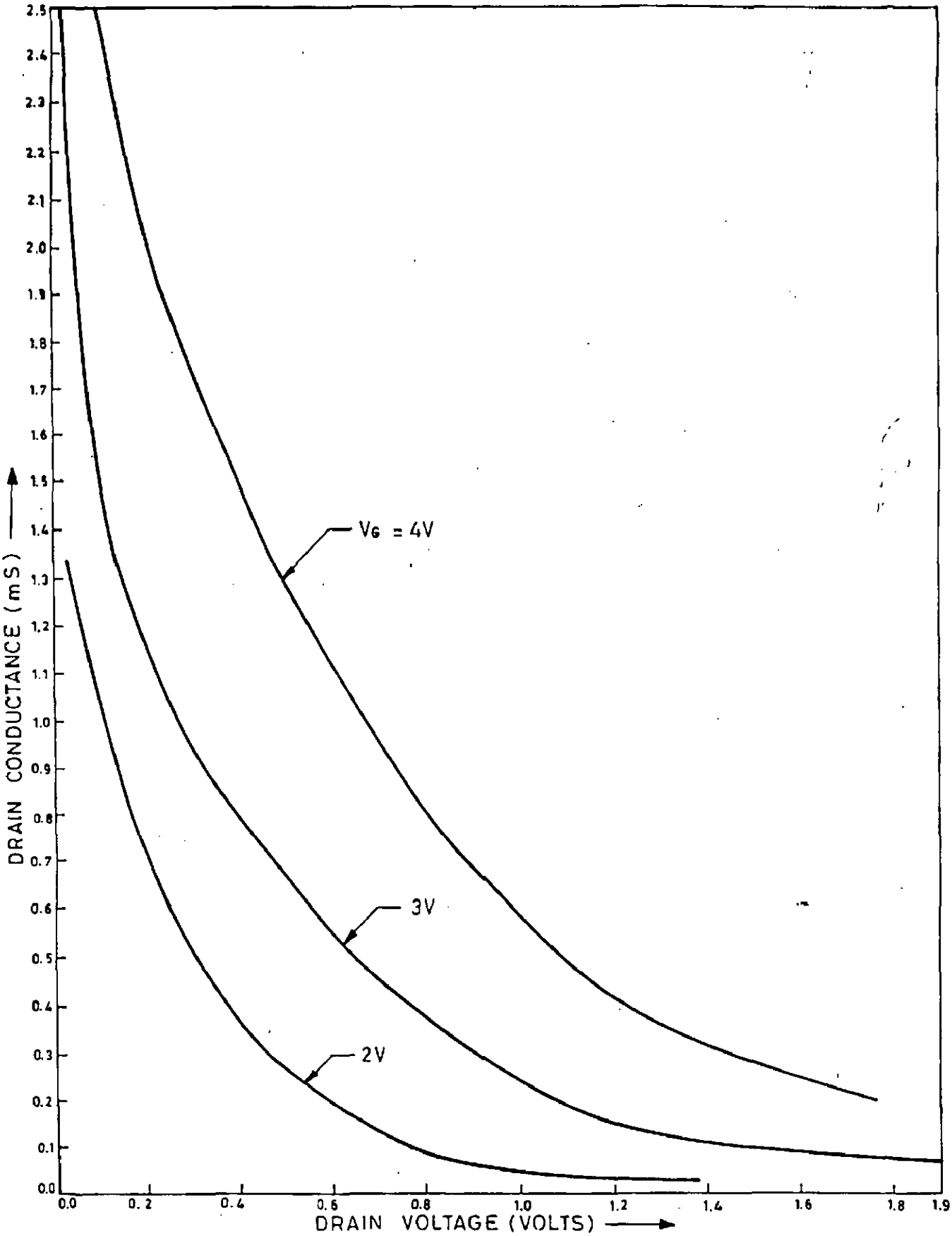


FIG. 4.6 DRAIN CONDUCTANCE VARIATION IN InGaAs MISFET, REF[7]AT DIFFERENT GATE VOLTAGE.

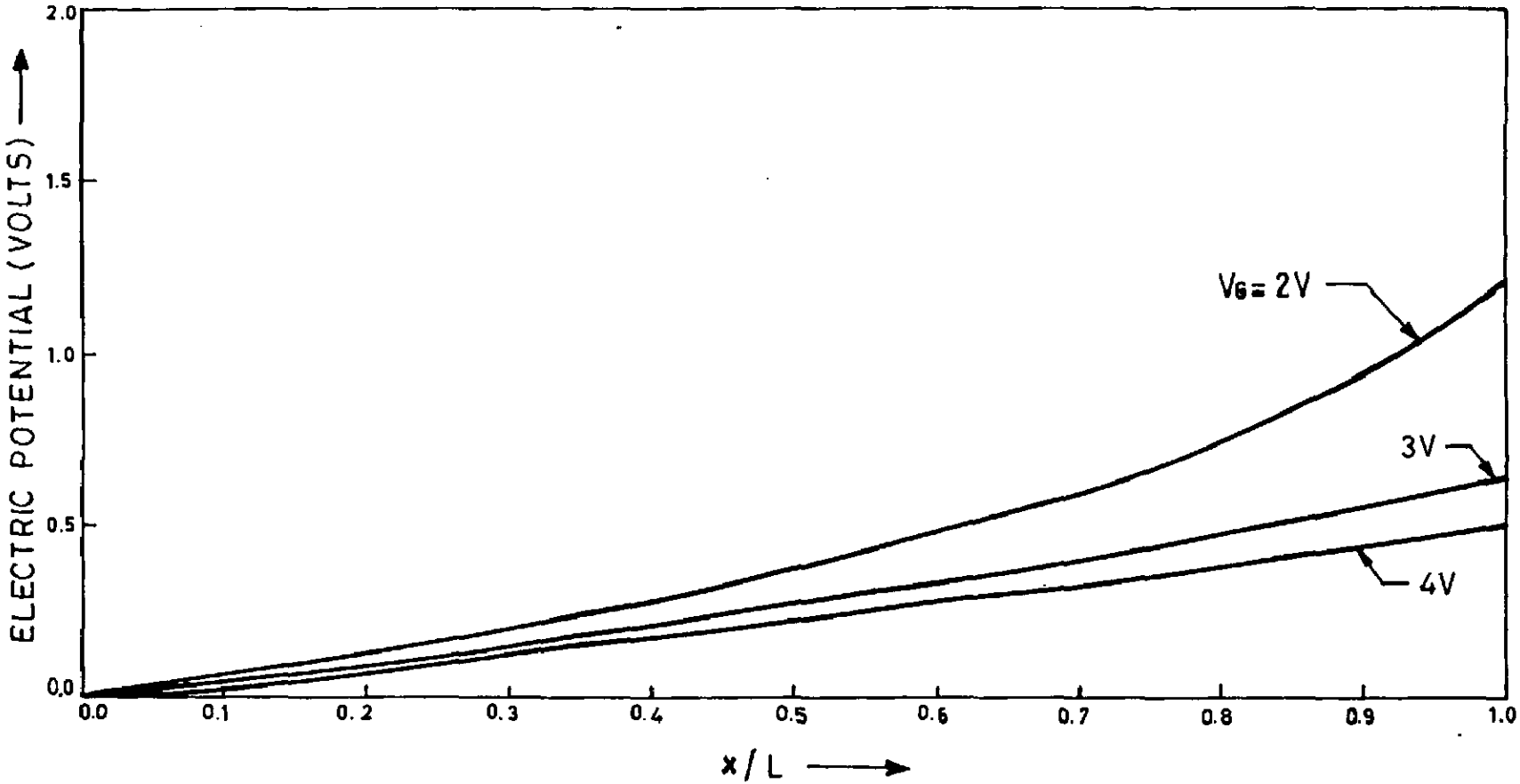
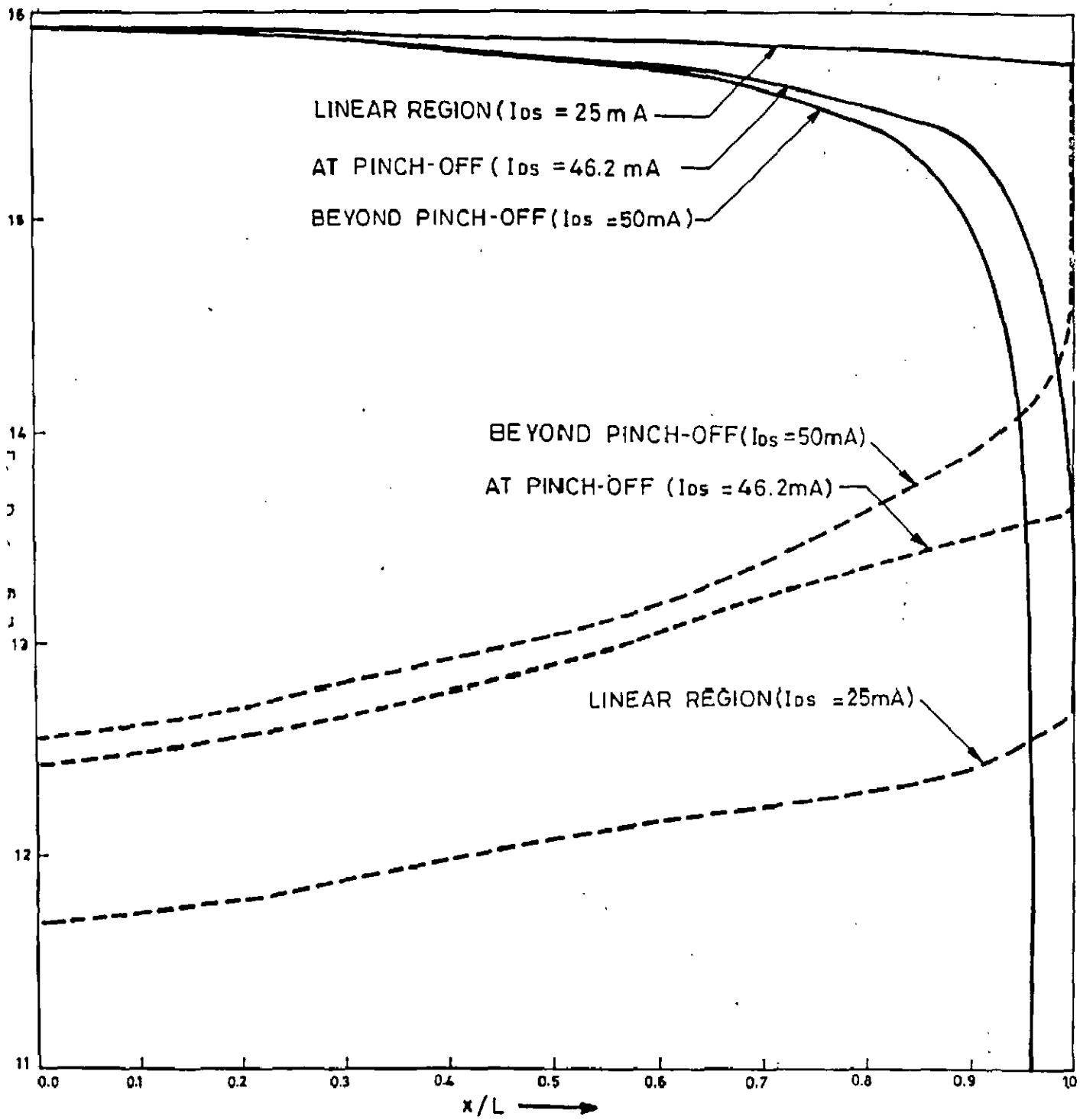


FIG. 4.7 VARIATION OF ELECTRIC POTENTIAL ALONG THE CHANNEL OF InGaAs MISFET ($L = 3\mu m$, $Z = 300\mu m$, $N_A = 10^{22} m^{-3}$) FOR $I_{DS} = 25$ mA .



IG. 4.8 GATE INDUCED (SOLID LINES) AND DRAIN INDUCED (DOTTED LINES) CARRIER CONCENTRATION VARIATION ALONG THE CHANNEL FOR DIFFERENT OPERATING CONDITIONS OF InGaAs MISFET (L = 3 μm, Z = 300 μm, $N_A = 10^{22}$ m^{-3}) AT GATE VOLTAGE = 3V.

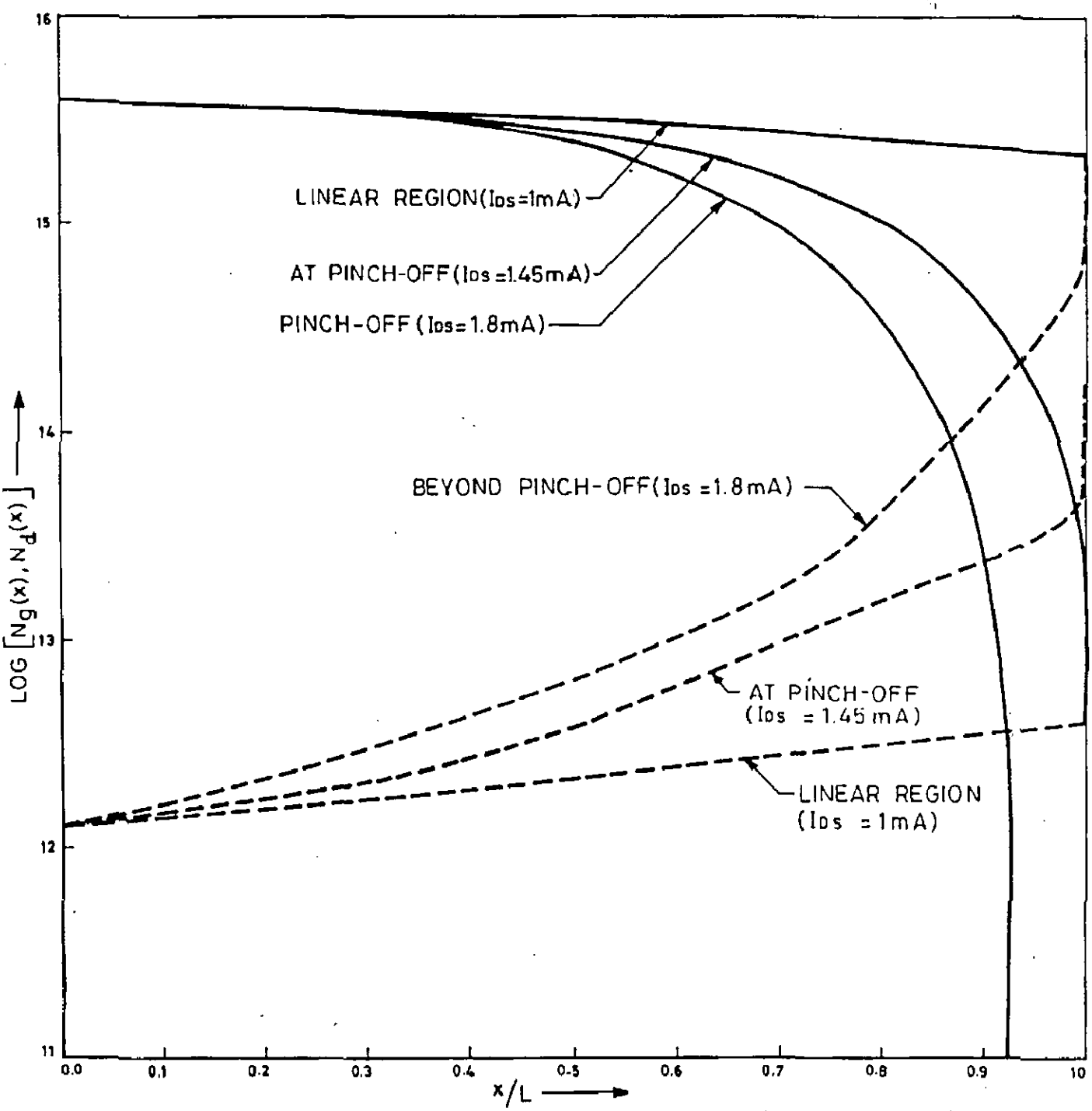


FIG. 4.9 GATE INDUCED (SOLID LINES) AND DRAIN INDUCED (DOTTED LINES) CARRIER CONCENTRATION VARIATION ALONG THE CHANNEL FOR DIFFERENT OPER-ATING CONDITIONS OF Si MISFET $L = 3\,\mu m$, $Z = 30\,\mu m$, $N_A = 10^{22}\ m^{-3}$ AT GATE VOLTAGE = 3V.

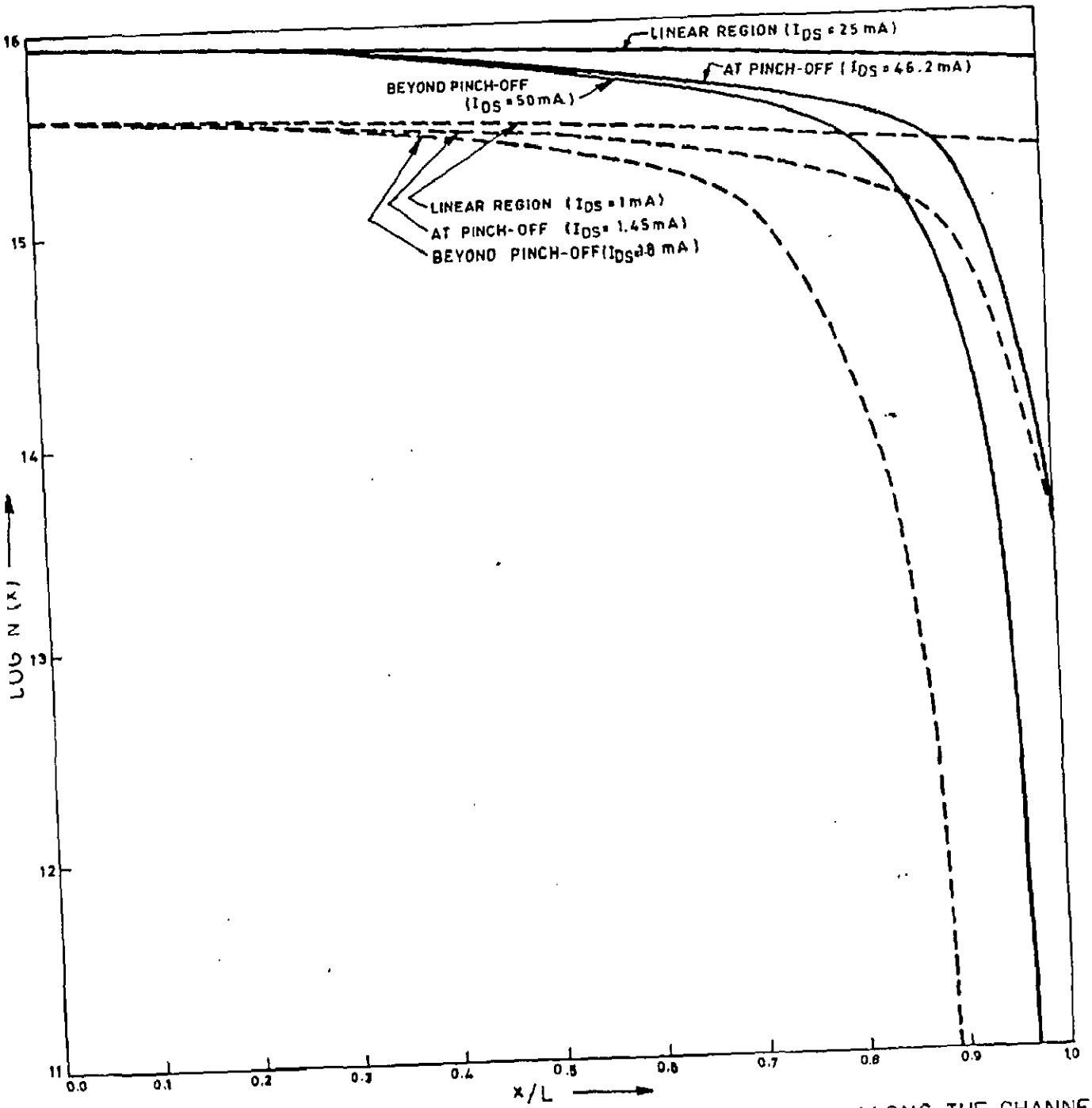


FIG. 4.10 VARIATION OF TOTAL INDUCED CARRIER CONCENTRATION ALONG THE CHANNEL OF InGaAs (SOLID LINES) AND SILICON (DOTTED LINES) MISFET UNDER DIFF—ERENT OPERATING CONDITIONS [$L = 3\,\mu m, Z = 300\,\mu m, N_A = 10^{22}\ m^{-3}$] AT GATE VOLTAGE = 3V.

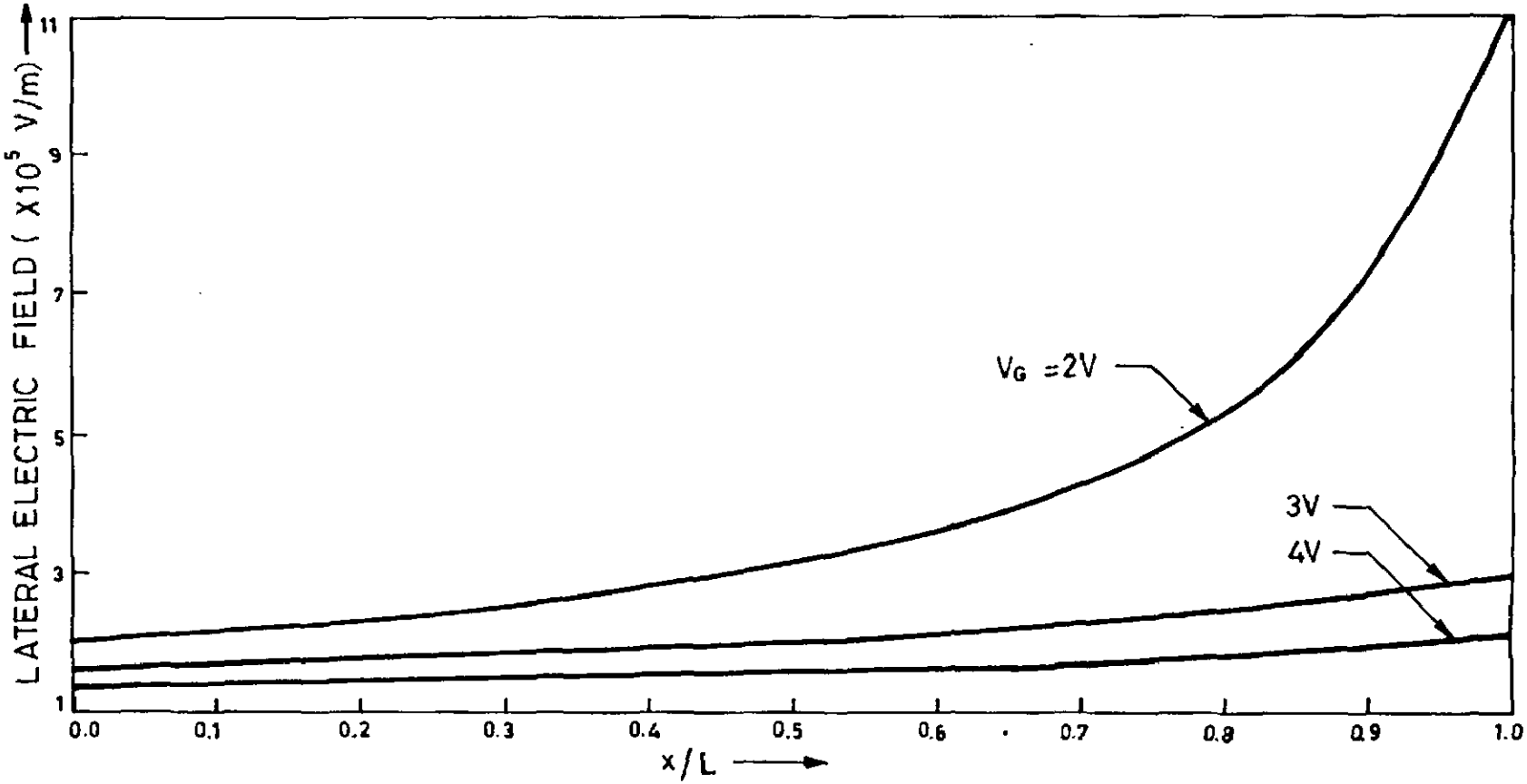


FIG.4.11 VARIATION OF ELECTRIC FIELD ALONG THE CHANNEL OF InGaAs MISFET [L = 3 μm , Z = 300 μm , $N_A = 10^{22}\ m^{-3}$] FOR I_{DS} = 25 mA GATE VOLTAGE IS THE PARAMETER.

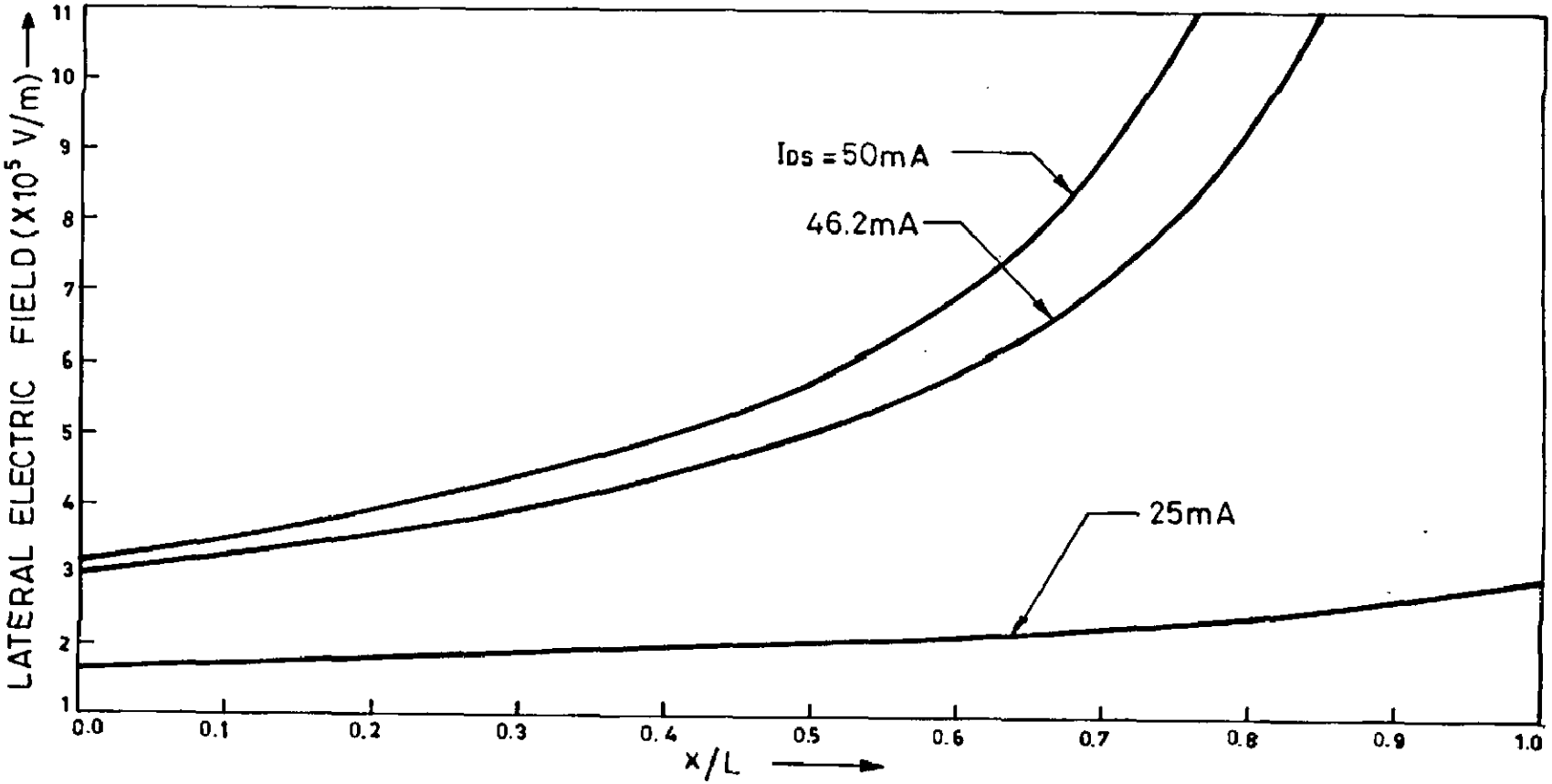


FIG. 4.12 ELECTRIC FIELD VARIATION ALONG THE CHANNEL OF InGaAs MISFET ($L = 3\,\mu m$, $Z = 300\,\mu m$, $N_A = 10^{22} m^{-3}$) WHEN THE MISFET IS OPERATED IN LINER REGION ($I_{DS} = 25\,mA$), AT PINCH-OFF ($I_{DS} = 46.2\,mA$) AND BEYOND PINCH-OFF ($I_{DS} = 50\,mA$) GATE VOLTAGE = 3V.

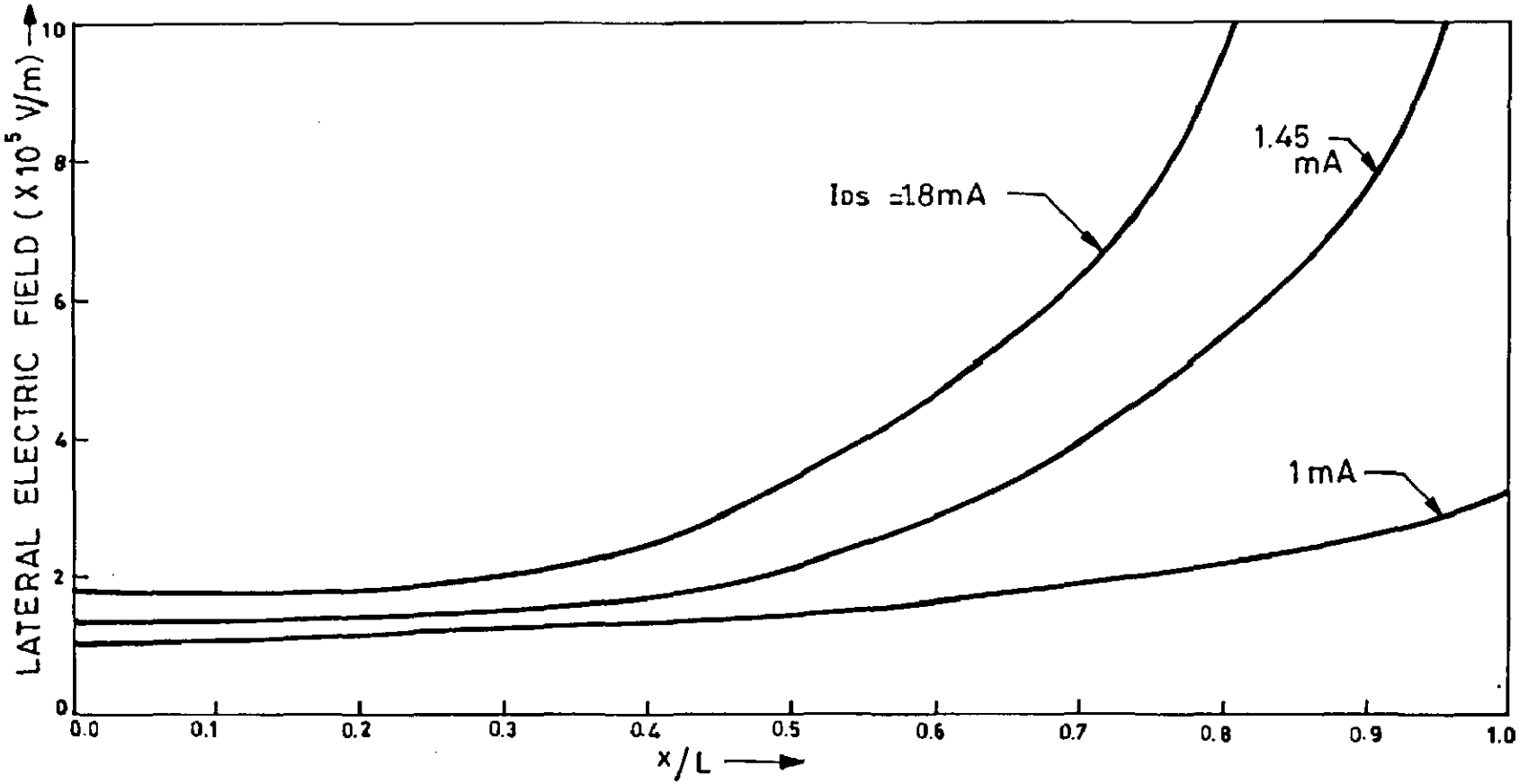


FIG. 4.13 ELECTRIC FIELD VARIATION ALONG THE CHANNEL OF A SILICON MISFET [$L = 3\,\mu m$, $Z = 300\,\mu m$, $N_A = 10^{22}\,m^{-3}$] WHEN THE DEVICE IS OPERATED IN LINEAR REGION ($I_{DS} = 1.0\,mA$), AT PINCH-OFF ($I_{DS} = 1.45\,mA$) AND BEYOND PINCH-OFF ($I_{DS} = 1.8\,mA$) GATE VOLTAGE = 3V .

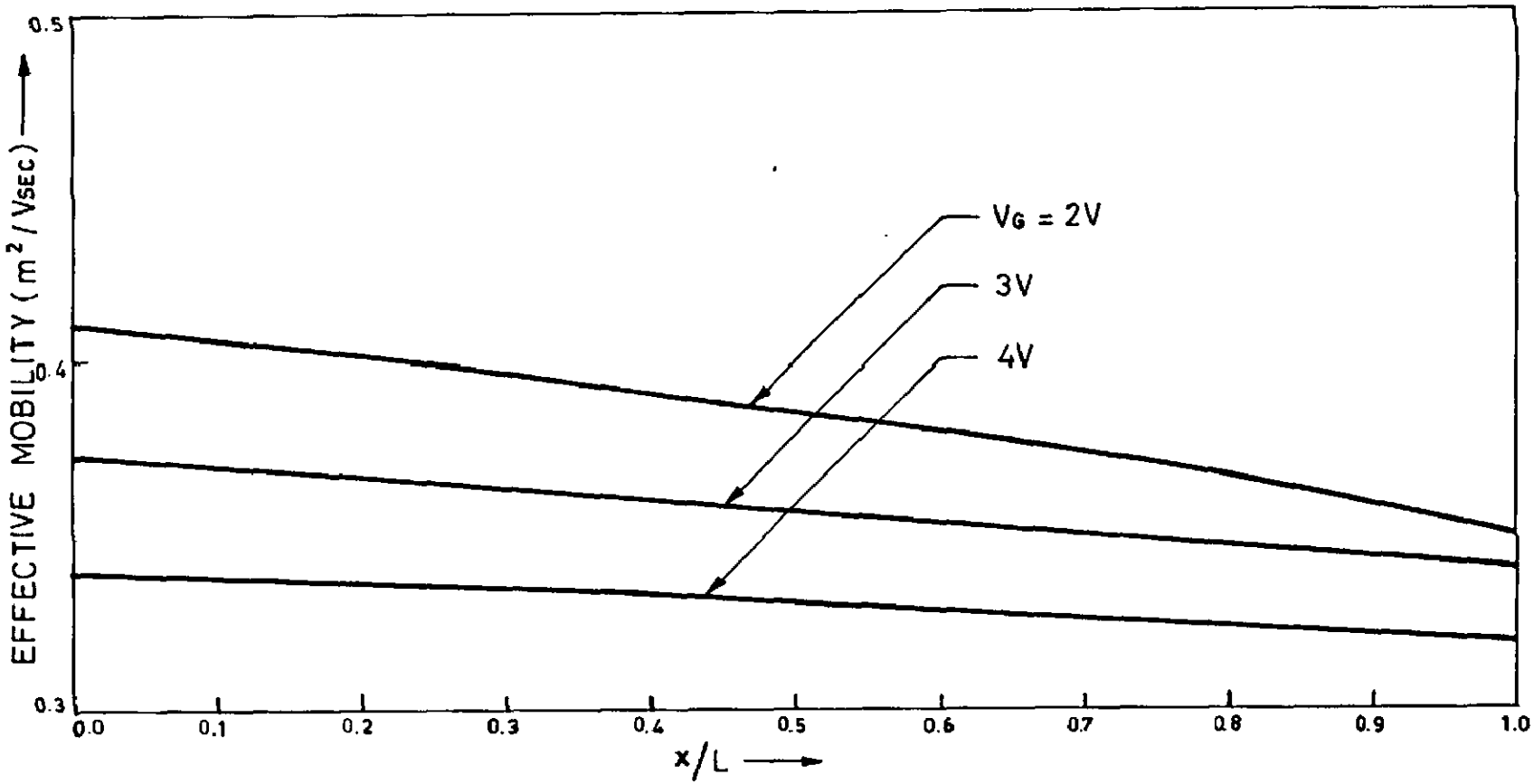


FIG. 4.14 ELECTRON EFFECTIVE MOBILITY VARIATION ALONG THE CHANNEL OF In Ga As MISFET [L = 3 μm, Z = 300 μm, $N_A = 10^{22} m^{-3}$] FOR DIFFERENT GATE VOLTAGES AT THE DRAIN CURRENT OF 25 mA .

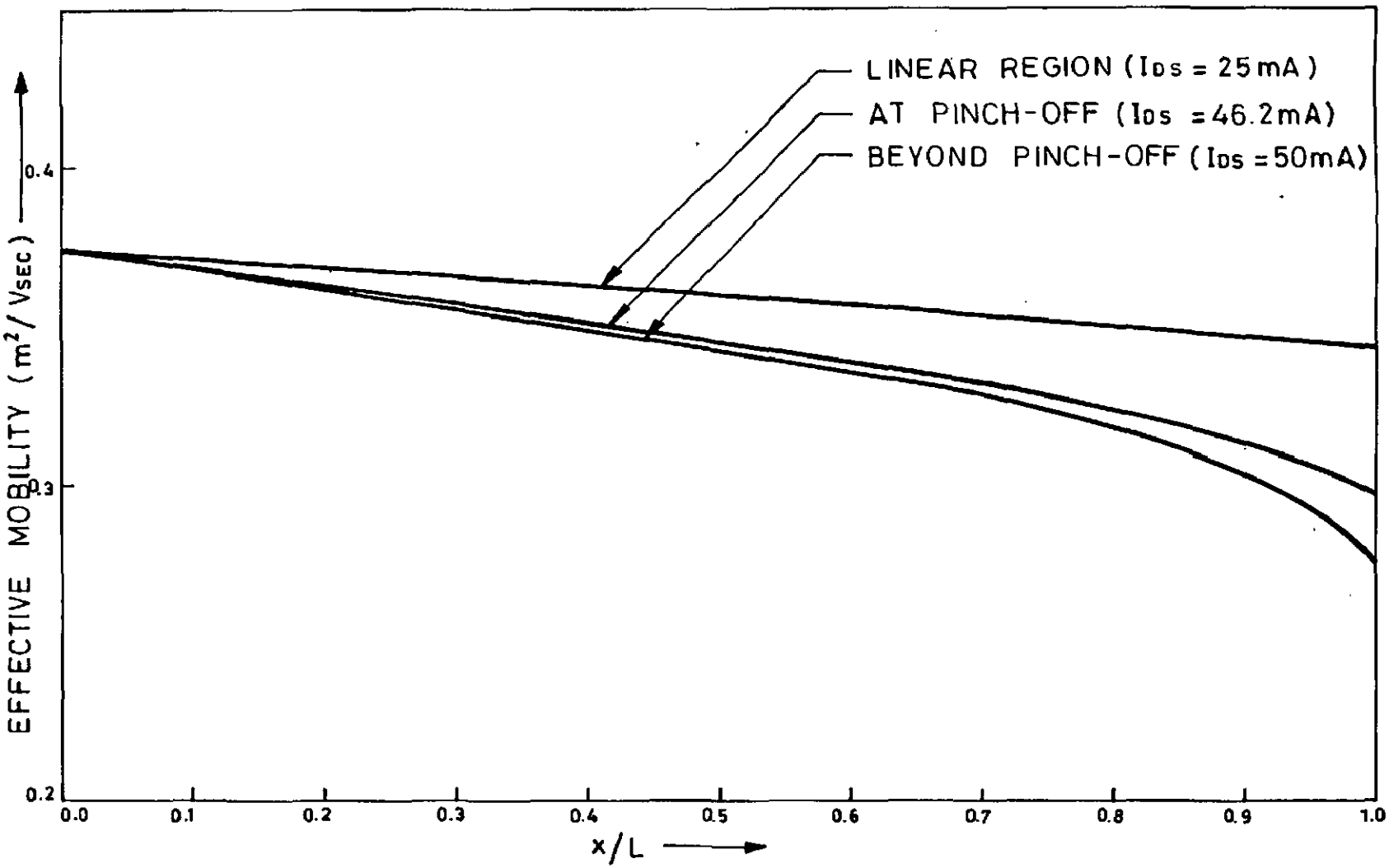


FIG. 4.15 ELECTRON EFFECTIVE MOBILITY VARIATION ALONG THE CHANNEL OF InGaAs MISFET ($L = 3\mu m$, $Z = 300\,\mu m$ AND $N_A = 10^{22}\,m^{-3}$) WHEN THE DEVICE IS OPERATED IN LINEAR REGION ($I_{DS} = 25$ mA) AT PINCH-OFF ($I_{DS} = 46.2$ mA) AND BEYOND PINCH-OFF ($I_{DS} = 50$ mA) GATE VOLTAGE = 3V.

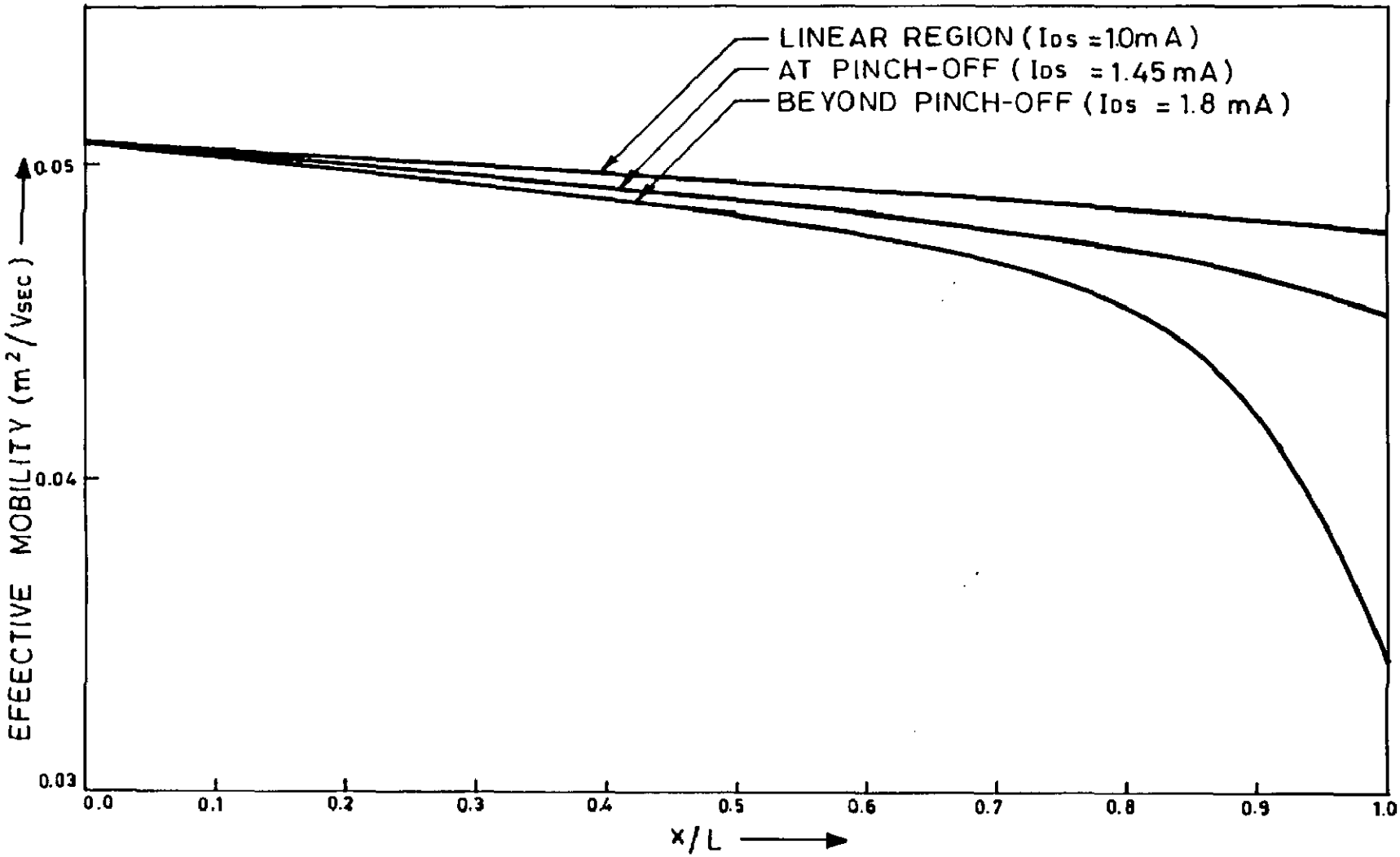
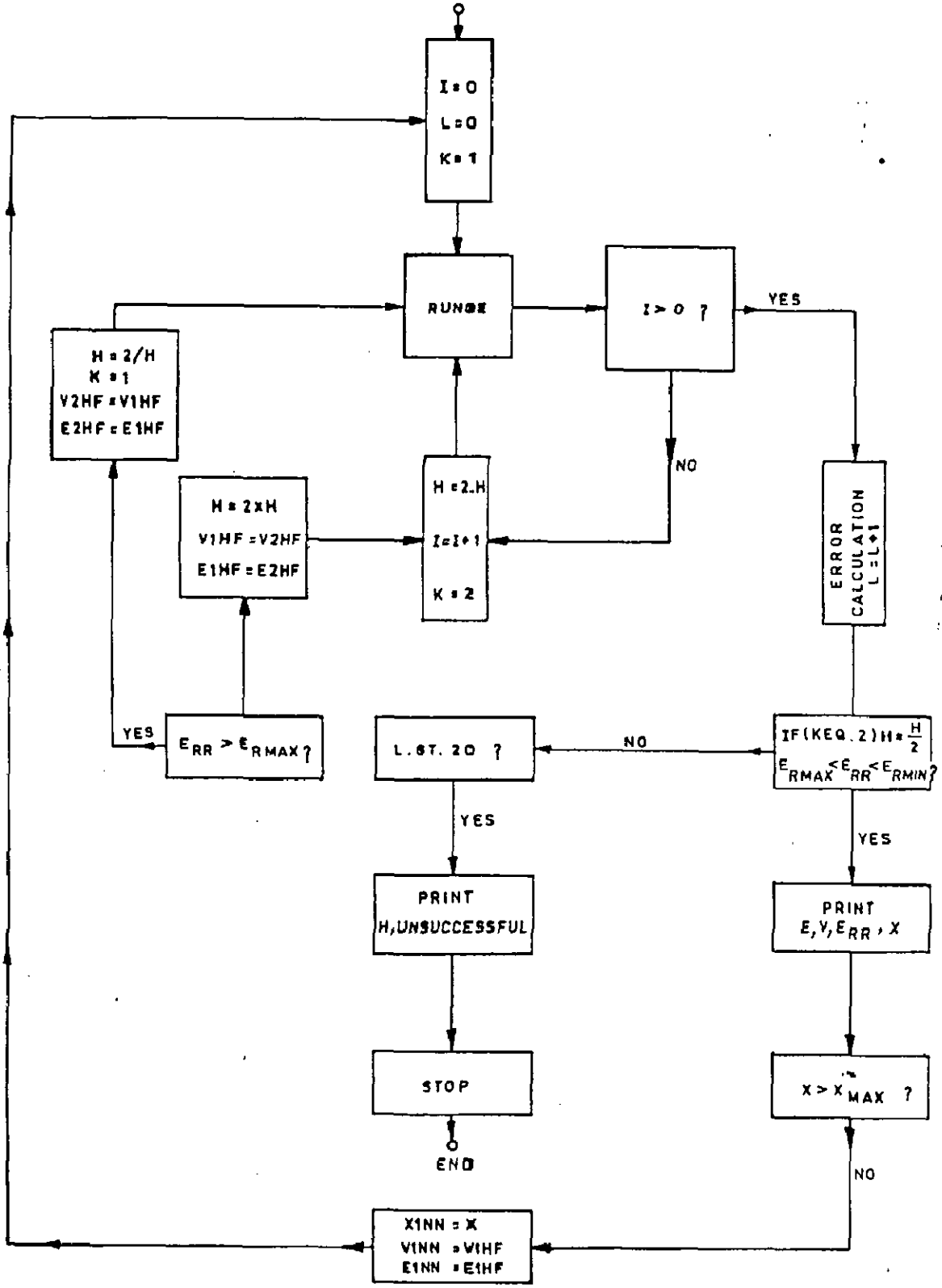


FIG. 4.16 ELECTRON EFFECTIVE MOBILITY VARIATION ALONG THE CHANNEL OF SILICON MISFET (L = 3 μm, Z = 300 μm, $N_A = 10^{22} m^{-3}$) WHEN THE DEVICE IS OPERATED IN LINEAR REGION (Ios = 1.0mA) AT PINCH-OFF (Ios = 1.45 mA) AND BEYOND PINCH-OFF (Ios = 1.8mA) GATE VOLTAGE = 3V .

APPENDIX 1



FLOW CHART RUNGE-KUTTA METHOD.

Important Parameters for InGaAs, InP and Si Semiconductors

Substrate	Bandgap(Eg) (eV)	Relative Permittivity	Intrinsic Carrier Concentration (n_i) (m^{-3})	Electron Affinity (χ)
InGaAs	0.75 [71]	13.0 [71]	7×10^{7} [71]	4.35 [71]
InP	1.35 [176]	12.5 [64]	8.47×10^{12} [220]	4.40 [176]
Si	1.12 [220]	11.9 [220]	1.45×10^{16} [220]	4.05 [220]

In the present MIS study, work function for Al as a gate metal is taken 4.2 [71] and SiO_2 relative permittivity 3.9 [220]. The work function difference ϕ_{ms} for a p-type semiconductor is given by [220]

$$\phi_{ms} = \phi_{Wm} - \phi_{Ws}$$
$$= \phi_{Wm} - \{ \chi + (E_g/2) + \phi_B \} \qquad \text{(A-2.1)}$$

where

ϕ_{Wm} = metal work function

ϕ_{Ws} = semiconductor work function.

The threshold voltage in a MISFET is [220]

$$V_T = V_{FB} + 2 \phi_B + (Q_B / C_i) \qquad \text{(A-2.2)}$$

where Q_B is depletion layer charge (per unit area) and at the onset of strong inversion [220] and bulk potential ϕ_B is given by

$$\phi_B = (kT/q) \ln(N_A/n_i) \qquad \text{(A-2.3)}$$

Thus flat-band voltage, bulk Fermi potential and threshold voltage can be calculated from (A-2.1),(3.32),(A-2.3) and (A-2.2). These values calculated for (C_i = 3.84 Fm^{-2} and $N_A = 10^{23} m^{-3}$) InGaAs, InP and Si MISFETs are tabulated in Table 4.2.

chapter V

DRAIN BREAKDOWN IN InGaAs MISFET

5.1 INTRODUCTION

The phenomenon of drain breakdown determines the highest applicable voltage and power handling capability of discrete MISFET or MIS integrated circuits. Therefore, the study of breakdown voltage is as important as the study of transconductance or threshold voltage. In the past, there have been some theoretical studies which account for the source-drain breakdown voltage of the MISFETs [103]. In an inversion-mode MISFET breakdown occurs due to impact ionization in the inversion channel and the reverse biased drain-substrate p-n junction. It is well established that avalanche multiplication (or impact ionization) is the dominant mechanism in drain-substrate junction breakdown and channel breakdown of a MISFET. Thus, avalanche breakdown voltage imposes an upper limit on the drain voltage of a MISFET. At high drain voltage both channel current and reverse saturation current in drain-substrate p-n junction is multiplied by impact ionization. This leads to an excessive drain current, which if left uncontrolled damages the device. The multiplication process depends on several material parameters, such as electron and hole ionization coefficients, bandgap energy etc. In this chapter, impact ionization in InGaAs and its effect on the drain characterstics of InGaAs MISFET have been studied. To begin with the chapter briefly reviews the basic theory of impact ionization. Various approaches to the estimation and evaluation of ionization rates and breakdown parameters such as breakdown voltage, breakdown field and multiplication factor are all discussed. With these background the breakdown parameters in InGaAs and related

semiconductors are estimated. Next, drain breakdown in InGaAs MISFET is analysed. In this analysis the influence of gate voltage on channel and drain-diode multiplication factors, drain characteristics, substrate current and drain breakdown voltage are analysed. The influence of substrate doping level on drain breakdown is also studied. Finally, drain breakdown in InGaAs and silicon MISFETs are compared.

5.2 THEORY OF IMPACT IONIZATION

Impact ionization in the semiconductor is one of the most extensively studied topic. As this phenomenon is encountered in a large number of semiconductor devices, a basic theory of impact ionization has evolved out of the experimental and theoretical investigations. As impact ionization occurs in the channel and the p-n junction of a MISFET, the theory of impact ionization is of importance to MISFET studies. In this section, the features of theory of impact ionization which are relevant to MISFET operation are briefly discussed.

5.2.1 Avalanche Breakdown and Ionization Integrals

Avalanche multiplication occurs when a high electric field is applied to a semiconductor. If the electric field is large enough to make an electron gain kinetic energy in excess of energy bandgap during a collision with host atom, the electron breaks the lattice bonds creating an electron-hole pair. This is called impact ionization. The newely created electron and hole (the secondaries) acquire kinetic energy from the field and create more electron-hole pairs. As the process continues a very large number

of electron-hole pairs are created. This process is called avalanche multiplication. For avalanche multiplication to occur, a sufficiently high field region is essential to accelerate the electron to ionization potential. It is for this reason a lightly doped p-n junction usually give rise to avalanche multipliction at high reverse voltages.

The condition for breakdown by avalanche multiplication process is best described by the ionization integral. The development of ionization integral may be achieved by the simple consideration of flow of minority carriers across a reverse biased p-n junction. If an electron current (reverse biased) I_{e0} is incident on the left side of the depletion region of width W (Fig. 5.1), the electrons constituting I_{e0} are accelerated by the field in the depletion region.

If the field is sufficiently high so that avalanche multiplication process can take place, the electron current I_e, increases with distance through the depletion region and attains a value of MI_{e0} at x = W.

The factor M_e is given by

$$M_e = I_e(W) / I_{e0} \qquad (5.1)$$

is known as the multiplication factor for electrons.

Similarly, the hole current I_h increases from I_{h0} at x = W to $I_h(W)$ at x = 0. The incremental electron current at x equals the number of electron-hole pairs generated per second in a small length dx and mathematically

$$d\left(\frac{I_e}{q}\right) = \left(\frac{I_e}{q}\right)\alpha_n\,dx + \left(\frac{I_h}{q}\right)\alpha_p\,dx \qquad (5.2)$$

where

α_n = ionization rate for electrons

α_p = ionization rate for holes.

Based on (5.2), Lee et al.[123], related multiplication factor for electron with ionization coefficients. This relation for the electron is given by

$$1 - \frac{1}{M_e} = \int_0^W \alpha_n \exp\left[-\int_0^x (\alpha_n - \alpha_p)\,dx'\right] dx \qquad (5.3)$$

and similarly for holes

$$1 - \frac{1}{M_h} = \int_0^W \alpha_p \exp\left[-\int_x^W (\alpha_p - \alpha_n)\,dx'\right] dx \qquad (5.4)$$

The expression (5.3) and (5.4) are referred to as the ionization integrals. The breakdown voltage due to avalanche mechanism is that particular voltage where multiplication factor approaches infinity. Hence from (5.3) for electron initiated avalanche mechanism, the breakdown condition is

$$\int_0^W \alpha_n \exp\left[-\int_0^x (\alpha_n - \alpha_p)\,dx'\right] dx = 1 \qquad (5.5)$$

Similarly for hole initiated avalanche mechanism, the breakdown condition is

$$\int_0^W \alpha_p \exp\left[-\int_x^W (\alpha_p - \alpha_n)\,dx'\right] dx = 1 \qquad (5.6)$$

For semiconductors of equal ionization coefficients for electrons and holes,(5.3) and (5.4) may be written as

$$1 - \frac{1}{M} = \int_0^W \alpha_n \, dx \tag{5.7}$$

and the breakdown condition is

$$\int_0^W \alpha_n \, dx = 1 \tag{5.8}$$

From the above considerations, it is obvious that, the evaluations of ionization integral is of importance for analytical study of avalanche process in any device.

5.2.2 Ionization Rates

From (5.3) and (5.4) it is seen that, a description of the impact ionization process can be assessed, provided the behaviour of the ionization rates, especially as functions of electric field is known. The theoretical studies of impact ionization are in general based on solving the Boltzmann transport equation. These studies are complicated by the fact that, an electron energised to ionization potential or even higher energy can lose its energy in either optical phonon generation or impact ionization. Thus, for proper treatment of the ionization process, these two processes must be considered as being parallel operation. Furthermore, multiple scattering processes must also be included. It must also be taken into account that the optical phonon energy is much smaller than ionization potential of a carrier and hence an energetic carrier can have energy for impact ionization even after

several scattering processes, involving generation of optical phonons [155,156,207,208].

Considering general drift and diffusion transport of carriers at high electric fields, Wolff [258], predicted that the ionization rate of carrier is inversely proportional to the square of the electric field. Shockley [207] used a low-field streaming approximation to express electron-hole pair production by what he called as the 'Lucky carriers'. Ionization rates obtained by this approach, when extrapolated to higher fields yielded values higher than what are obtained by Wolff's [258] diffusion model.

Baraff [10] calculated ionization rates by solving the time dependent Boltzmann transport equation. In this approach both extreme approximations of Shockley [207] and Wolff [258] were included. In the process a more general picture of impact ionization was obtained in terms of three parameters, namely, threshold energy for pair production E_I, phonon energy loss E_R and phonon scattering mean free path. This three parameters theory of Baraff well explains the electric field dependence of the ionization rates and the intricacies of the scattering processes. Crowell and Sze [39] extended Baraff's theory to include the dependence of ionization rate on lattice temperature and the effects of phonon absorption. They numerically fitted the results of avalanche experiments and showed that the ionization rate α of a carrier may be expressed as

$$\alpha\lambda = \exp\left[- \left(a_0 + a_1 Z_1 + a_2 Z_1^2 \right) \right] \qquad (5.9)$$

where

$$a_0 = \left(757\ r^2 - 75.5\ r + 1.92 \right) \qquad (5.10a)$$

$$a_2 = \left(- 46\ r^2 + 11.9\ r - 1.75 \times 10^{-2} \right) \qquad (5.10b)$$

$$r = E_R / E_I \tag{5.11}$$

and

$$Z_1 = E_I / \lambda E \tag{5.12}$$

The error in the fit of the above equation to the data of Crowell and Sze [39] is within ± 2 % over the range $0.01 < r < 0.06$ and $5 < Z_1 < 16$. The average energy lost by a carrier, after phonon scattering is

$$E_R = \phi_R \tanh(q \phi_R / k T) \tag{5.13}$$

where ϕ_R is Raman optical phonon energy and the optical phonon mean free path is given by

$$= \lambda_0 \tanh(q \phi_R / k T) \tag{5.14}$$

where λ_0 is the limiting free path as the absolute temperature approaches zero.

Chwang et al. [34] used a finite Markov chain formulation to study impact ionization and combined this approach with Baraff's theory [10] to obtain a meaningful expression for ionization rate as a function of electric field. Ever since these developments a number of expressions for electron and hole ionization rates have been proposed by several authors [148,182,221,230].

One of the most useful and widely used expression for the ionization rate of electrons and holes is of the form [221]

$$\alpha_n , \alpha_p = A_{n,p} \exp\left(- \frac{b_{n,p}}{E} \right)^m \tag{5.15}$$

The parameters $A_{n,p}$, $b_{n,p}$ and m depend on the material. For most semiconductors, m = 1. For some semiconductors, such as

GaAs and GaP, m = 2.

5.2.3 The Breakdown Field

As discussed previously, the breakdown occurs when the ionization integral assumes the value of unity. That is when (5.5) and (5.6) are satisfied. The critical electric field at which these conditions are satisfied is commonly termed as the breakdown field. In a p-n junction avalanche breakdown occurs when the peak field at the metallurgical junction attains this critical value. In semiconductors, the breakdown field is of the order of 10^7 V/m. Since breakdown in a p-n junction occurs with the peak field reaching the value of breakdown field, it is possible to relate breakdown field with depletion layer width W. Thus, solution of (5.5) and (5.6) yields breakdown field. The highly non-linear relationship between ionization rate and electric field forbids an exact solution for (5.5) and (5.6). Therefore, evaluation of breakdown field from breakdown condition given by (5.5) and (5.6) calls for a numerical approach by iteration [221].

While breakdown field can be determined with fairly high accuracy by the numerical approach, a good approximation of the field can be made by relating breakdown voltage with the breakdown field. If E_{BR} and V_{BR} are the breakdown field and voltage of an one sided abrupt p-n junction, then from p-n junction theory

$$V_{BR} = [\, \epsilon_s \epsilon_0 \, E_{BR}^2 \, / \, 2 \, q \, N_I \,] \qquad (5.16)$$

where N_I is the base impurity concentration of the one sided diode. Based on experimental data on the dependence of breakdown voltage on the base impurity concentration of one sided abrupt

junctions in Si, Ge, GaAs and GaP and approximate universal expression

$$V_{BR} = 60 \left(E_g/1.1 \right)^{3/2} \left(N_I/10^{22} \right)^{-3/4} \text{ volts} \qquad (5.17)$$

was proposed by Sze and Gibbons [221]. A similar expression for linearly graded junction was also proposed. Eq. (5.16) and (5.17), for abrupt junction

$$E_{BR} = \left[(120\, q\, N_I/\epsilon_s\epsilon_0)\, (E_g/1.1)^{3/2}\, (10^{22}/N_I)^{3/4} \right]^{1/2} \qquad (5.18)$$

Thus breakdown field in terms of material parameters can be obtained from (5.18). Obviously, by the same method, an expression for breakdown field for linearly graded junction can be obtained.

5.2.4 Evaluation of Multiplication Factors

One of the most important parameter of impact ionization process is the multiplication factor M, which relates the multiplied current to the primary current flowing through a semiconductor in breakdown condition. As already mentioned, the multiplication factor is related to the ionization integral, given by (5.5) and (5.6). The difficulties of evaluating the ionization integrals for electrons and holes, makes it imperitive to develop some analytical expression for multiplication factor.

Miller [148] presented an empirical relation for multiplication factor for a p-n junction biased at a voltage V. This relation is

$$M = \frac{1}{\left[1 - (V/V_{BR})^{n} \right]} \qquad (5.19)$$

To some extent (5.19) serves the purpose of an analytical expression for multiplication factor. This expression, however, leads to considerable errors in case of low level multiplication. Furthermore, the parameter n varies over a range of 2 and 6, requiring measurements on each individual device seperately.

Mckay [139] showed that it is possible to analyse avalanche breakdown process by a somewhat simplified approach. In this approach, the actual function is approximated by a junction having an uniform field equal to the peak field E_m at metallurgical junction and a depletion width W_{eq} so that the multiplication factor is same for the actual and equivalent junction. Spirito [212,213] applied this method to obtain analytical expressions for multiplication factor from (5.5) and (5.6). For an abrupt junction the expressions thus obtained are

$$1 - \frac{1}{M_n} = \frac{\alpha_{nm}}{\alpha_{pm} - \alpha_{nm}} \left[\exp[(\alpha_{pm} - \alpha_{nm}) W_{eq\ n}(E_m)] - 1 \right] \qquad (5.19)$$

$$1 - \frac{1}{M_p} = \frac{\alpha_{pm}}{\alpha_{nm} - \alpha_{pm}} \left[\exp[(\alpha_{nm} - \alpha_{pm}) W_{eq\ p}(E_m)] - 1 \right] \qquad (5.20)$$

where α_{nm} and α_{pm} are ionization rates at E_m. The equivalent depletion layer width W_{eq} is related to the actual depletion layer width W by a parameter m, such that

$$W_{eq} = m\ W \qquad (5.21)$$

For $E_m \ll E_{BR}$, the parameter m for electrons and holes is

seperately given by

$$m_n = \int_0^{E_m} \frac{\alpha_n \, dE}{\alpha_{nm} \, E_m} \tag{5.22a}$$

$$m_p = \int_0^{E_m} \frac{\alpha_p \, dE}{\alpha_{pm} \, E_m} \tag{5.22b}$$

and for $E_m = E_{BR}$, the parameter m assumes a value m_B given by

$$m_B = \left[\frac{\ln (\alpha_{nB} / \alpha_{pB})}{\alpha_{nB} - \alpha_{pB}} \right] \frac{q \, N_I}{\epsilon_s \epsilon_0 \, E_{BR}} \tag{5.23}$$

where α_{nB} and α_{pB} are ionization rates at the breakdown field E_{BR}. The analytical expressions (5.20a) and (5.20b) have been found to approximate experimental data with fair accuracy. These expressions were used for analysis of avalanche breakdown in MISFET by Das et al.[40] and good agreement between theoretical predictions and experimental observations were obtained.

5.2.5 A Therotical Estimation of Breakdown Parameters in InGaAs and Related Semiconductors

The most convenient method of determining the breakdown parameters of a semiconductor is to carry out investigations on p-n junction operating at high reverse voltages. Such investigations have been made in considerable details on p-n junctions in Ge, Si, GaAs and GaP [220]. Very little experimental data from such studies on InGaAs and its most closely related quaternary InGaAsP have been reported in the literature. Some informations are, however, available regarding the ionization

rates of the carriers in these materials [111,116,147,175,176,225]. It has been observed that the electron and hole ionization rates in InGaAsP is dependent on alloy composition. For $In_{1-x}Ga_xAs_yP_{1-y}$ system, lattice matched to InP substrates ($y \simeq 2.2\ x$), the ratio α_p/α_n first sharply falls from a value greater than unity (2 - 5) to some value less than unity (0.4 - 0.3) as y increases from 0.0 to 1.0, when electric field is oriented in the (100) direction. The binary limit of the quaternary is InP i.e. $y = 0$. For this case, α_p/α_n ratio is found to be as high as 4.0 [116]. This ratio falls to about 0.3 when y is approximately 0.5. Thereafter, α_p/α_n increases to about 0.5 when $y = 1.0$ (InGaAs). Thus, in InGaAs, electron ionization dominates, while it is the hole ionization process that dominates in the case of InP.

Pearsall [175] determined breakdown voltage in InGaAs, by using (5.17) and showed that, the universal relation hold for the ternary semiconductor. The theoretically calculated breakdown voltages for different impurity concentrations agreed well with experimental data. In the present work (5.17) is used to determine breakdown voltage as function of composition parameter y, of the $In_{1-x}Ga_xAs_yP_{1-y}$ quaternary system. The y-dependence of breakdown voltage comes through the bandgap E_g as indicated by (5.17). The y dependence of E_g is accounted for by (3.8). Fig. 5.2 illustrates the variation of breakdown voltage in $In_{1-x}Ga_xAs_yP_{1-y}$ abrupt p-n junction with y-composition parameter, for impurity concentration, $N_A \simeq 5\times10^{21}$, 10^{22}, 7×10^{22} and $10^{23}\ m^{-3}$. As can be seen that InP ($y \simeq 0$) p-n junction has the highest breakdown voltage and InGaAs ($y \simeq 1.0$) junction has the lowest breakdown voltage for the impurity range considered. This is due to decrease in bandgap with

increase in y. The most important parameter, which is responsible for occurance of breakdown is the breakdown field E_{BR}. This field is calculated from (5.18) as function of y-composition parameter for $In_{1-x}Ga_xAs_yP_{1-y}$ junction. Fig. 5.3 shows the variation of breakdown field in $In_{1-x}Ga_xAs_yP_{1-y}$ as a function of y-composition parameter. It may be seen that like breakdown voltage, breakdown field also decreases with increase in y-composition parameter. As indicated by (5.18), the composition dependence of breakdown voltage results from its dependence on bandgap energy and semiconductor permittivity. As shown in Table 3.1, while bandgap energy decreases with increase in y-composition parameter, the reverse is true for semiconductor permittivity. Thus, the variation of both bandgap energy and semiconductor permittivity with y, jointly make contribution to the fall in breakdown voltage with increase in composition parameter y. Fig. 5.3 also shows that breakdown field increases with increase in impurity concentration. This indicates, that as the collision frequency increases with increase in impurity concentration, the carriers suffer a number of non-ionizing collisions, thereby requiring higher field to acquire ionization threshold energy.

Fig. 5.4 shows the variation of breakdown field with impurity concentration for abrupt InGaAs p-n junction as calculated from (5.18). The material parameters for InGaAs as reported by Gardner et al.[71] are taken. In InGaAs, the breakdown field increases very slowly between 1.71 - 5×10^7 V/m for a four order of increase in impurity concentration, as it is clearly shown in the figure. Thus, as a first approximation, we can assume that for InGaAs, E_{BR} has a fixed value as it is in the case of many other semiconductors. Since E_{BR} is a slowly varying function

of impurity concentration through (5.18), the breakdown voltage as a first order approximation varies as N_A^{-1} for one sided abrupt junction.

5.3 DRAIN BREAKDOWN IN MIS TRANSISTOR

In this section, the effect of impact ionization on drain characteristics of InGaAs MIS field-effect transistor under high drain bias condition is examined. Hofstein and Warfield [105] suggested two mechanism for current multiplication due to impact ionization, which depending on the biasing conditions, appear to be responsible for the drain voltage breakdown characteristics of MIS transistor. These are : channel breakdown and drain-diode breakdown.

The channel breakdown is characterized by the relatively gradual increase in drain current with drain voltage when the device is biased in the conducting region. Typically, for a smaller gate voltage, saturation drain current at first gradually increases as the drain-source voltage is increased, then at a critical drain voltage, the increase in drain current is fairly sharp. In drain characteristics of MISFET, it is observed that the region of gradual increase becomes less evident as gate voltage is increased. The mechanism dominating the channel breakdown is generally attributed to impact ionization of carriers in the channel region. In the vicinity of drain end of the channel electric field is high. Depending on the bias conditions the field may be high enough to accelerate the carriers to ionization energy. As a consequence electron-hole pair generation by impact ionization may take place. The total generation rate for

electron-hole pairs is a function of electric field and drain current. Hence it is expected that as gate voltage approaches threshold voltage this mechanism should be less significant becoming negligible when gate bias equals threshold voltage.

The drain-diode of an inversion-mode MISFET is constituted by the drain and the substrate which is of opposite conductivity type with respect to the drain. Under normal biasing condition, this diode is reverse biased. The reverse bias increases with increase in drain-source voltage. Thus, at a critical value of the drain-source voltage, the reverse bias becomes high enough to produce reverse current multiplication by impact ionization process. The drain-diode breakdown is characterized by a sharp increase in drain current in the neighbourhood of the breakdown voltage. The drain-diode breakdown takes over from channel breakdown, when gate voltage is lower than the threshold voltage and drain-source voltage is sufficiently high. For a gate voltage greater than threshold voltage, the channel breakdown appears to be the only breakdown mechanism. It has been observed that for a gate voltage higher than the threshold voltage, the drain-source breakdown voltage is comparatively less. This reduction in breakdown voltage is a direct result of the influence of gate voltage on the drain-substrate electric field [80]. In drain region of n-channel MISFET consisting of n^+-p junction, the depletion layer thickness near the corner region is shorter than that away from the surface [79,80]. In the corner region, the n^+-p junction field lines and insulating layer field (oxide field) line reinforce each other leading to a high electric field. As gate voltage is made more negative, the corner field increases and avalanche multiplication of carriers in the corner region results

in drain-substrate breakdown causing a reduction of the drain-substrate breakdown voltage. Thus, the drain junction breakdown can be controlled by gate bias.

5.4 INFLUENCE OF IMPACT IONIZATION ON DRAIN CHARACTERISTICS

In a MISFET both channel breakdown and drain-diode breakdown may occur simultaneously. The drain current in such an event is the sum of the two avalanche currents. The channel breakdown mainly occurs in the pinch-off region close to the drain. In case of an n-channel inversion-mode MISFET, the electrons are collected by the drain, while the holes, which are created by impact ionization process flow into the substrate. This flow of holes into the substrate constitute what is known as the substrate current. In case of short-channel devices, a part of the substrate current also flows into the source contact giving rise to bipolar transistor action. In case of the long-channel MISFETs, however, this effect does not occur, as the drain-source seperation is relatively larger. Thus, in the long-channel MISFETs the effect of substrate current may be safely neglected.

In chapter IV, the output characteristics of MISFET is obtained by solving (4.15) which is a second order differential equation describing the effects of two dimensional field on carrier transport in the channel. The current obtained by this 2-dimensional model is the channel current. The word 'channel current' has a specific significance in this context. The channel current is a component of drain current and not the drain current itself. The flow of the charge under the influence of source-drain field constitutes the channel current I_{ch}. The channel current

mainly flows on the surface of the substrate till it enters the drain depletion region. Upon entering the drain depletion region, the current flows deeper into the substrate and the carriers are accelerated by the high electric field in the depletion region. Because of this acceleration, the carriers gain sufficient energy to produce ionization. The number of carriers which are able to ionize the substrate atoms, increases with increase in drain voltage. Thus, if M_{ch} is the channel multiplication factor then as a result of impact ionization, the resultant channel current I_{cr} is

$$I_{cr} = M_{ch} I_{ch} \tag{5.24}$$

While impact ionization multiplies the channel current, avalanche multiplication process also takes place in the reverse biased drain-substrate junction. The result of this multiplication process gives rise to a resultant diode current which is

$$I_{dr} = M_{sub} I_{sn} \tag{5.25}$$

where M_{sub} is the multiplication factor of the reverse biased drain-substrate diode and I_{sn} is the reverse saturation current. The drain current is thus,

$$I_{DS} = M_{ch} I_{ch} + M_{sub} I_{sn} \tag{5.26}$$

5.4.1 Avalanche Ionization in the Channel

In this subsection, the current multiplication in the channel by impact ionization is analysed. The increase in channel current is mainly due to impact ionization of the substrate atom by electrons, which are accelerated by the lateral field in the channel. As the channel current is dierctly obtained from the 2-D

analysis (chapter IV), to find the multiplied channel current only parameter required is M_{ch}. It is assumed that impact ionization is only appreciable beyond the pinch-off point.

The present analysis of channel impact ionization is confined to electric fields upto the breakdown field for the substrate material, which is InGaAs. As pointed out previously, the determination of avalanche multiplication factor requires the difficult task of numerical evaluation of the ionization integral. Thus, approximate calculations have been carried out by the aid of Spirito's analysis [212,213]. Spirito's approach is applicable to a p-n junction for which the maximum electric field at the metallurgical junction is known and an equivalent depletion layer width W_{eq} as given by (5.21) is defined. The channel region beyond the pinch-off point P, is basically the depletion region of the drain-substrate p-n junction (Fig. 5.6). Thus, Spirito's approach of evaluating the multiplication factor is applicable in the present context. Since, the potential drop between the pinch-off point and the drain is $(V_{DS} - V_{DP})$, the maximum field in this case is

$$E_m = \left[\frac{2}{K_0} (V_{DS} - V_{DP}) \right]^{1/2} \qquad (5.27)$$

When the drain voltage is increased to a point such that the charge in the inversion layer Q_n at $x = L$ reduces to zero, the number of mobile carriers (electrons) at the drain experiences a drastic fall and pinch-off is said to have occured at this stage of operation. With the occurance of pinch-off the drain current saturates. The potential at the drain when the pinch-off just sets

in is V_{DP}, with further increase in drain voltage, the pinch-off point P, approaches the source and V_{DP} is given by (4.34). Substituting (4.34) in (5.27)

$$E_m = \sqrt{\frac{2}{K_0}\left[V_{DS} - \left[V_G - V_{FB} - 2\,\phi_B - K^2 \left(\left(1 + \frac{2V_G}{K^2}\right)^{1/2} - 1 \right)\right]\right]} \tag{5.28}$$

where

$$K_0 = \epsilon_s \epsilon_0 \,/\, q\, N_A \tag{5.29}$$

The Eq. (5.17) shows that the uniform field in Mckay's approximation [139] is a function of both drain voltage and gate voltage.

Considering an n-channel inversion-mode MISFET, the channel multiplication factor is evaluated by using (5.20a).Since, electrons are the only carriers, that make contribution to channel current, impact ionization, due to electrons is considered. Thus,

$$M_{ch} = \left[1 - \frac{\alpha_{nm}}{\alpha_{pm} - \alpha_{nm}} \left[\exp\left((\alpha_{pm} - \alpha_{nm})\, W_{eq}(E_m)\right) - 1\right]\right]^{-1} \tag{5.30}$$

where

$$\alpha_{nm} = A_n \exp\left[- (b_n / E_m)\right] \tag{5.31a}$$

$$\alpha_{pm} = A_p \exp\left[- (b_p / E_m)\right] \tag{5.31b}$$

The field E_m being given by (5.28). The saturation voltage (drain voltage for pinch-off) is obtained from the variation of inversion charge density profile (chapter IV). It is the drain voltage which, the gate induced carrier concentration just vanishes at the drain end. For the determination of the equivalent

depletion layer width, the relation given by (5.21) is used in the form

$$W_{eq}(E_m) = m_n W \tag{5.32}$$

as only electrons are assumed to be involved in the multiplication process. For the evaluation of the factor m_n, the approximation [213]

$$m_n = [\, E_m / b_n \,] \tag{5.33}$$

is used. From p-n junction theory

$$W = K E_m \tag{5.34}$$

Thus, substituting (5.33) and (5.34) in (5.32)

$$W_{eq}(E_m) = \frac{K E_m^2}{b_n} \tag{5.35}$$

Substituting (5.35) in (5.30)

$$M_{ch} = \left[1 - \frac{\alpha_{nm}}{\alpha_{pm} - \alpha_{nm}} \left[\exp \left((\alpha_{pm} - \alpha_{nm}) \frac{K E_m^2}{b_n} \right) - 1 \right] \right]^{-1} \tag{5.36}$$

Thus, substitution of (5.36) in (5.24) gives

$$I_{cr} = \frac{I_{ch}}{1 - \frac{\alpha_{nm}}{\alpha_{pm} - \alpha_{nm}} \left[\exp \left((\alpha_{pm} - \alpha_{nm}) \frac{K E_m^2}{b_n} \right) - 1 \right]} \tag{5.37}$$

as the channel current under impact ionization. The primary channel current I_{ch} is obtained from the solution of second order differential equation (4.14).

5.4.2 Junction Breakdown in MIS Device

As mentioned previously, a component of drain breakdown current results from drain-substrate p-n junction breakdown. This

component is a result of multiplication of reverse saturation current I_{sn}, of the junction. The electrons are minority carriers in the bulk of the p-type substrate and move towards the drain under the reverse bias condition. The reverse saturation current due to electrons flow is expressed by the relation [220]

$$I_{sn} = (A_{ds}\ q\ D_n\ n_{p0})/L_n \tag{5.38}$$

where

A_{ds} = drain-substrate junction area

D_n = bulk diffusion coefficient for electrons

n_{p0} = electron concentration in p-type substrate

L_n = electron diffusion length in p-type substrate.

As can be seen from (5.38), electron reverse saturation current I_{sn} depends on the drain-substrate junction area, electron diffusion coefficient and electron diffusion length. While diffusion coefficient can be evaluated from the knowledge of bulk electron mobility [$\mu_B = (kT/q)\mu_n$], the determination of L_n requires the knowledge of electron life time in p-type substrate. The electron life time depends upon the capture cross-section and density of bulk traps. As not much of work has been carried out for the determination of these parameters in InGaAs, it is presently difficult to predict the life time for electrons as such. However, some estimate can be made for junction breakdown phenomenon for n-channel inversion-mode InGaAs MISFET by assuming a suitable value for I_{sn}. If I_{sn} is assumed then resultant avalanche current

$$I_{dr} = M_{sub}\ I_{sn} \tag{5.39}$$

where M_{sub} is the multiplication factor for the drain junction

under avalanche breakdown. Thus only parameter required for calculation of I_{dr} is M_{sub}. Assuming the substrate to be at ground potential ($V_{sub} = 0$), the maximum field at the drain-substrate junction is

$$E_{msub} = \sqrt{\frac{2\, q\, N_A}{\epsilon_s\, \epsilon_0}\, V_{DS}} \tag{5.40}$$

substituting (5.20) and (5.32 - 5.35) in (5.25)

$$I_{dr} = \frac{I_{sn}}{1 - \frac{\alpha_{nms}}{\alpha_{pms} - \alpha_{nms}} \left[\exp\left((\alpha_{pms} - \alpha_{nms}) \frac{K\, E_{msub}^2}{b_n} \right) - 1 \right]} \tag{5.41}$$

where

$$\alpha_{nms} = A_n \exp\left(- \frac{b_n}{E_{msub}} \right) \tag{5.42a}$$

$$\alpha_{pms} = A_p \exp\left(- \frac{b_p}{E_{msub}} \right) \tag{5.42b}$$

Thus from (5.36), M_{sub} can be calculated.

5.4.3 Substrate Current

This substrate current is caused by the flow of avalanche produced holes into the substrate terminal and the multiplied reverse saturation current. The substrate current I_{sub} is given by

$$I_{sub} = (M_{ch} - 1)\, I_{ch} + M_{sub}\, I_{sn} \tag{5.43}$$

This current is often taken as a measure of avalanche process in the channel. For most of the drain voltage range, $M_{sub}\, I_{sn}$ is negligible. However, when M_{sub} approaches infinity,

the second term on R.H.S. of (5.43) is no longer negligible.

5.5 INFLUENCE OF GATE VOLTAGE AND IMPURITY CONCENTRATION ON InGaAs MISFET DRAIN CHARACTERISTICS IN THE BREAKDOWN RANGE

The carrier multiplication by impact ionization is a high field effect. As the gate voltage creates an electric field in the channel, the process of channel multiplication becomes dependent on the gate voltage. Furthermore, the impurity concentration of the substrate to some extent determines the channel current produced by impact ionization. These factors affect the drain current of a MISFET biased to drain breakdown condition. In this section, these aspects of drain breakdown are studied.

5.5.1 Effect of Gate Voltage on Drain and Substrate Current in the Breakdown Region

The variations of channel multiplication factor M_{ch}, and substrate multiplication factor M_{sub}, with drain voltage as calculated from (5.36) and (5.41) for n-channel inversion-mode InGaAs MISFET of L = 1.5 μm, Z = 150 μm, $N_A = 4\times10^{22}$ m^{-3} and $C_i = 3.84\times10^{-4}$ Fm^{-2} are shown in Fig. 5.7 for gate voltages of 2, 3 and 4 V. Material parameters are taken from Gardner et al.[71].

The multiplication factors M_{ch} and M_{sub} are functions of the maximum electric fields E_m and E_{msub} which are given by (5.24) and (5.35) respectively. The field E_m is dependent on gate voltage through its relation with V_{DP}. To incorporate the influence of gate voltage on E_m, Eq. (4.15) is solved for different gate voltages. As multiplication factor is dependent on ionization

rates, its calculation requires the knowledge of ionization rate constants A_n, b_n, A_p and b_p, for the substrate material. Pearsall [175] measured the ionization rates for electrons and holes in InGaAs. From these experimental data the ionization rate constants are determined from the slope of α_n, α_p vs. E^{-1} curves and (5.15). The calculated ionization rate constants are illustrated in Table 5.1.

Table 5.1 : Ionization Rate Constants of InGaAs.

Carrier	$A_{n,p}$ (m^{-1})	$b_{n,p}$ (V/m)
Electron	2.68×10^8	1.42×10^8
Hole	3.05×10^8	1.58×10^8

As in any other MISFET, in an InGaAs MISFET channel current flows under the influence of source-drain field on the surface of the substrate and then it enters the drain depletion region. In the depletion region, carriers are accelerated by a high electric field and because of this acceleration carrier gain sufficient energy to produce ionization of the substrate atoms. The ionization process is enhanced by the increase in drain voltage. Breakdown occurs when E_m equals the critical field E_{BR}. From (5.28), the drain voltage for channel breakdown is

$$V_{DBR} = \frac{K_0}{2} E_{BR}^2 + V_G - V_{FB} - 2\phi_B + K^2 \left[\left(1 + 2V_G K^{-2} \right)^{1/2} - 1 \right] \tag{5.44}$$

The factor K being defined by (4.33). The Eq. (5.44) shows that,

with increase in gate voltage the channel breakdown voltage increases. The breakdown points for each curve in Fig. 5.7 is indicated by an arrow head. The maximum electric field E_m depends on drain and gate voltages as can be seen from (5.28) and for a constant gate voltage it increases with increase in drain voltage. A careful examination of (5.30) shows that the channel multiplication factor M_{ch}, increases with increase in E_m. Thus, the channel multiplication factor increases with increase in drain voltage as shown in Fig. 5.7. Near breakdown voltage, M_{ch} attains large value and increases abruptly. As seen in Fig. 5.7, M_{ch} is relatively lower at higher gate voltages, which is more evident, at higher drain voltages. This is because of the fact that increase in gate voltages reduces the field E_m, which in turn reduces M_{ch}. For lower drain voltages, E_m being too small to produce appreciable ionization, M_{ch} is close to unity. In reverse biased drain-substrate junction, avalanche multiplication process also takes place. The maximum electric field in the substrate E_{msub}, increases with increase in drain voltage. Thus substrate multiplication factor M_{sub}, which is a function of E_{msub} increases with increase in drain voltage shown by the broken curve in Fig. 5.7. E_{msub} being independent of gate voltage, M_{sub} is not affected by change in gate voltage.

The variation of drain characterstics in the breakdown region for InGaAs MISFET with L = 1.5 μm, Z = 150 μm and N_A = $4\times10^{22}m^{-3}$ for gate voltages 2, 3 and 4 V is illustrated in Fig. 5.8. Here the resultant drain currents, which are the sum of multiplied channel and drain-diode current are plotted as a function of drain voltage. With increase in drain voltage, both channel multiplication factor, M_{ch} and substrate multiplication

factor, M_{sub} increase. As a consequence the multiplied current I_{cr} and I_{dr} increases with increase in drain voltage. This in turn increases the total drain current. Beyond pinch-off for lower drain voltages M_{ch} and M_{sub} increases at slower rates with drain voltage. As a result the total drain current shows a marginal increase as long as the drain voltage is below the critical value for on set of breakdown, as given by (5.44). As shown in Fig. 5.7, the channel multiplication factor M_{ch}, decreases with increase in gate voltage. This effect, however, is not seen in Fig. 5.8. The reason being the larger primary channel currents for higher gate voltages. In other words, increase in gate induced carrier concentration at higher gate voltage dominates over the maximum field (E_m) lowering by increase in gate voltage. The abrupt increase in drain current at critical drain voltages reflect the effect of the maximum field attaining the critical value of E_{BR}.

The substrate current I_{sub}, is due to flow of avalanche produced holes into the substrate terminal and the multiplied reverse saturation current I_{sn}. As indicated in (5.38), I_{sn} is a function of electron diffusion coefficient and diffusion length. Since reliable data on carrier diffusion length in InGaAs is not available, it is assumed that $I_{sn} = 5\times10^{-9}$ A [60]. It has been shown that for lower drain voltages M_{ch} and M_{sub} increase gradually with increase in V_{DS}. The dependence of substrate current on M_{ch} and M_{sub} as given by (5.43), therefore shows that, the substrate current should also shows the increasing trends. In low drain voltage range, reverse saturation current contribution is negligible and substrate current is mainly a part of channel current. Near breakdown voltage, I_{sub} increases sharply and is dependent on gate voltage (Fig. 5.9). At breakdown, contribution

of reverse saturation component is very small owing to the negligibly small value of I_{sn} for InGaAs MISFET. The gate voltage dependence of the drain characteristics is dominated by gate induced carrier density and the decrease in M_{ch} with increase in gate voltage not reflected is shown in Fig. 5.9.

5.5.2 Effect of Impurity Concentration on Drain Current in the Breakdown Region

As can be seen in Fig. 5.4, the breakdown field is a slowly varying function of impurity concentration and breakdown field increases with increase in impurity concentration. The drain current variation with drain voltage of an InGaAs MISFET of L = 3 μm, Z = 300 μm, $C_i = 3.84 \times 10^{-4} Fm^{-2}$, $\mu_0 = 0.7\ m^2/V\text{-}s$, $\theta_s = 0.166 V^{-1}$ and $E_c = 10^7$ V/m at a gate voltage of 3 V and for substrate impurity concentrations N_A of 10^{21}, 5×10^{21} and $10^{22}\ m^{-3}$ in Fig. 5.10.

From (5.18), it can be seen that for lower impurity concentration the breakdown field E_{BR}, is lower. In spite of that, Fig. 5.10 shows that breakdown in MISFETs built in comparatively lightly doped substrates occur at higher drain voltages. This is because of the fact that the breakdown voltage V_{DBR} is increased by decrease in impurity concentration. This is clearly indicated by (5.44). Thus, breakdown at lower drain voltages are encountered if a MISFET is built in a heavily doped substrate. On the other hand, a lightly doped substrate may fail to give any saturated drain current, due to a larger primary channel current. Thus, while selecting the doping level of the substrate a compromise between breakdown voltage and range over which drain current

remains constant has to be made.

Fig. 5.11 shows the variation of substrate current with drain voltage for the same MISFET. For a low impurity concentration such as 10^{21} m^{-3}, M_{ch} is also low resulting in a low substrate current. The substrate current increases very slowly with increase in drain voltage and breakdown occurs at a fairly high drain voltage. For high impurity concentration such as 10^{22} m^{-3}, M_{ch} increases rapidly with drain voltage. This gives rise to higher substrate current and breakdown occurs at a lower value of drain voltage.

5.5.3 A Comparison with Silicon MISFET

For the sake of comparison of drain breakdown in InGaAs and silicon MISFETs, Eq. (4.15) is solved for a silicon MISFET of same channel length, channel width, insulator capacitance and substrate impurity concentration as those for the InGaAs MISFET treated in subsection 5.5.1. Other parameters for the silicon MISFETs are V_{FB} = - 0.87 V, $C_i = 3.84 \times 10^{-4}$ Fm^{-2}, μ_o = 0.1046 $m^2/V\text{-}s$, θ_s = 0.18 V^{-1} and $E_c = 10^7$ V/m. These have been selected on the basis of experimental data available in literature [103]. Calculations are carried out at gate voltages, which yield for the two cases, the same relative increase in the strength of inversion from the threshold level. Fig. 3.2 shows that the nature of variation of strength of inversion with gate voltage in InGaAs and silicon MISFET are more or less identical. The difference being of level of inversion. In Fig. 5.8, the drain characteristics of the InGaAs MISFET at gate voltages of 2, 3 and 4 V are shown. The threshold voltage for this MISFET being 0.4 V, the three gate

voltages are respectively, 1.6, 2.6 and 3.6 V above threshold. The threshold voltage of silicon MISFET is calculated by using (3.30). The calculated threshold voltage is 2.54 V. Thus, for the silicon MISFET, gate voltages of 4.14, 5.14 and 6.14 V approximately result in same relative increase in strength of inversion above the threshold level as gate voltages of 2, 3 and 4 V respectively does in case of InGaAs MISFET.

Fig. 5.12 illustrates the drain characteristics of the silicon MISFET at gate voltage of 4.14, 5.14 and 6.14 V. Here, the drain current is the sum of the multiplied channel and drain-diode currents. Comparing Fig. 5.12 with Fig. 5.8, it is seen that impact ionization in the channels and drain-diode of InGaAs and silicon MISFETs have similar effects on their respective drain characteristics. Furthermore, the drain characteristics (Fig. 5.8 and 5.12) calculated by present approach agree with experimental observations reported in literature [103]. However, the drain breakdown voltages as calculated from (5.44) are significantly different. The drain breakdown voltages for the two devices at the three gate bias levels which are 1.6, 2.6 and 3.6 V above the respective threshold voltages are tabulated in Table 5.2. It shows that the drain breakdown voltages for the silicon MISFET is higher than that for InGaAs MISFET. A careful inspection of the various

Table 5.2 : Drain Breakdown Voltages for InGaAs and Si MISFETs.

($V_G^* = V_G - V_T$)

Semiconductor	Drain Breakdown Voltages (V)		
	$V_G^* = 1.6$ V	$V_G^* = 2.6$ V	$V_G^* = 3.6$ V
InGaAs	17.63	19.34	21.29
Si	29.14	30.72	32.26

parameters involved in (5.44) shows that the major contribution for this difference in drain breakdown voltage is the fairly wide difference in breakdown field for the two materials. For example, the breakdown field in InGaAs having an impurity concentration of 10^{22} m^{-3} is 3.65×10^7 V/m, whereas for the same impurity concentration the breakdown field in silicon is 5.15×10^7 V/m. The drain breakdown voltage being approximately proportional to square of breakdown field, the drain breakdown voltages for the two cases differ appreciably.

As can be seen from (5.44), several material parameters other than breakdown field also determine the drain breakdown voltage of a MISFET. These are bulk potential ϕ_B and the constants K_0 and K. In addition to this the parameter: V_{FB} which is the flat-band voltage also determines the drain breakdown voltage. As mentioned previously, the flat-band voltage is partly technology dependent. Flat-band voltage for InGaAs MISFET is determined from experimental data available in literature is larger in magnitude than that in silicon MISFETs. Calculations show that flat-band voltage along with ϕ_B, K and K_0 make a comparatively smaller

contribution towards the difference in drain breakdown voltages of InGaAs and silicon MISFETs. Table 5.3, shows the values of these parameter for the two MISFETs compared.

Table 5.3 : Material Parameters ϕ_B , K and K_0.

Semiconductor	Material parameters			
	ϕ_B(V)	K^2(V)	K_0(m^2/V)	V_{FB}(V)
InGaAs	0.28	5.01	1.8×10^{-14}	- 2.55
Silicon	0.38	4.58	1.64×10^{-14}	- 0.88

It is therefore clear that silicon MISFET has an advantage over InGaAs MISFET so far as drain breakdown voltage is concerned. A higher drain breakdown voltage is desirable, as it enlarges the operating drain voltage range of a MISFET. While the drain currents in InGaAs and silicon MISFETs are similarly affected by impact ionization processes, the substrate currents in the two devices are also similarly affected. This may be seen from the comparison of Fig. 5.13 and Fig. 5.9.

5.6 CONCLUSION

Based on the existing theories on impact ionization in semiconductors and p-n junctions, drain breakdown in InGaAs MISFET has been analysed. This analysis also takes the help of 2-D MISFET-model developed in the preceding chapter. It has been shown analytically, that the influence of channel and drain-diode breakdown in InGaAs MISFETs give rise to similar effects on the drain characteristics as has been observed in the case of silicon

MISFET. The analysis brings out the fact that an InGaAs MISFET has a disadvantage over the silicon counterpart, as it has a relatively lower breakdown voltage.

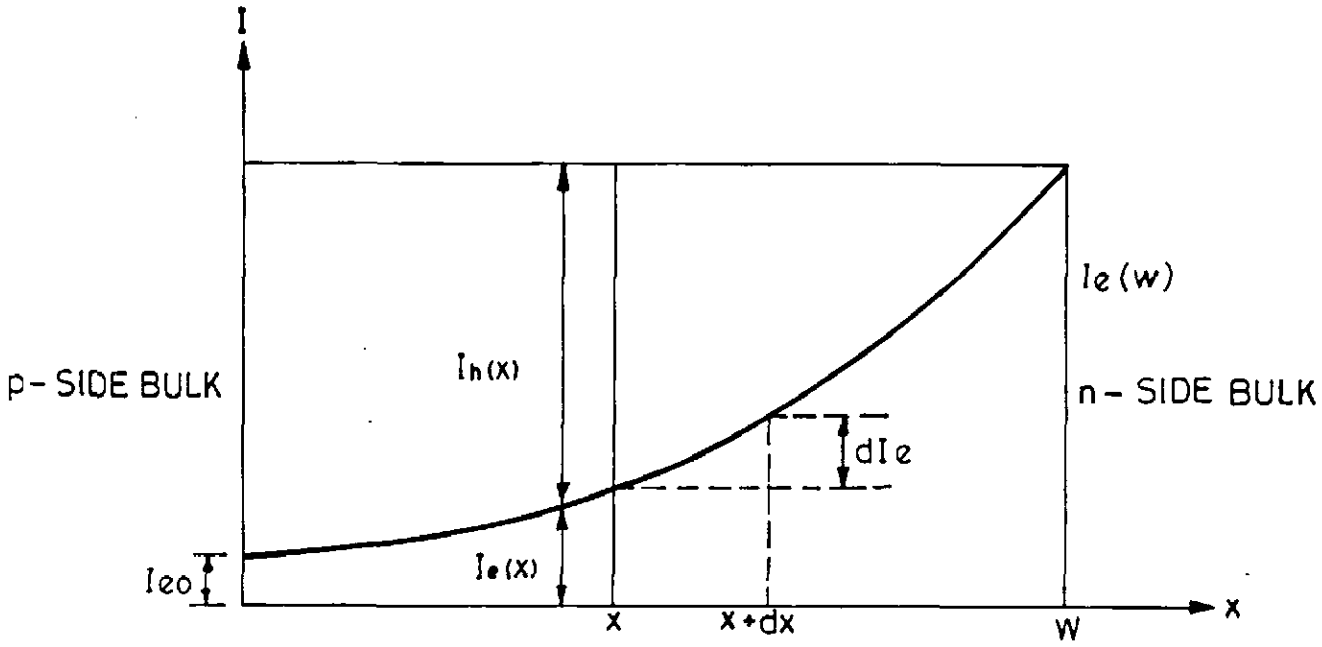


FIG. 5.1 DEPLETION REGION IN A p-n JUNCTION.

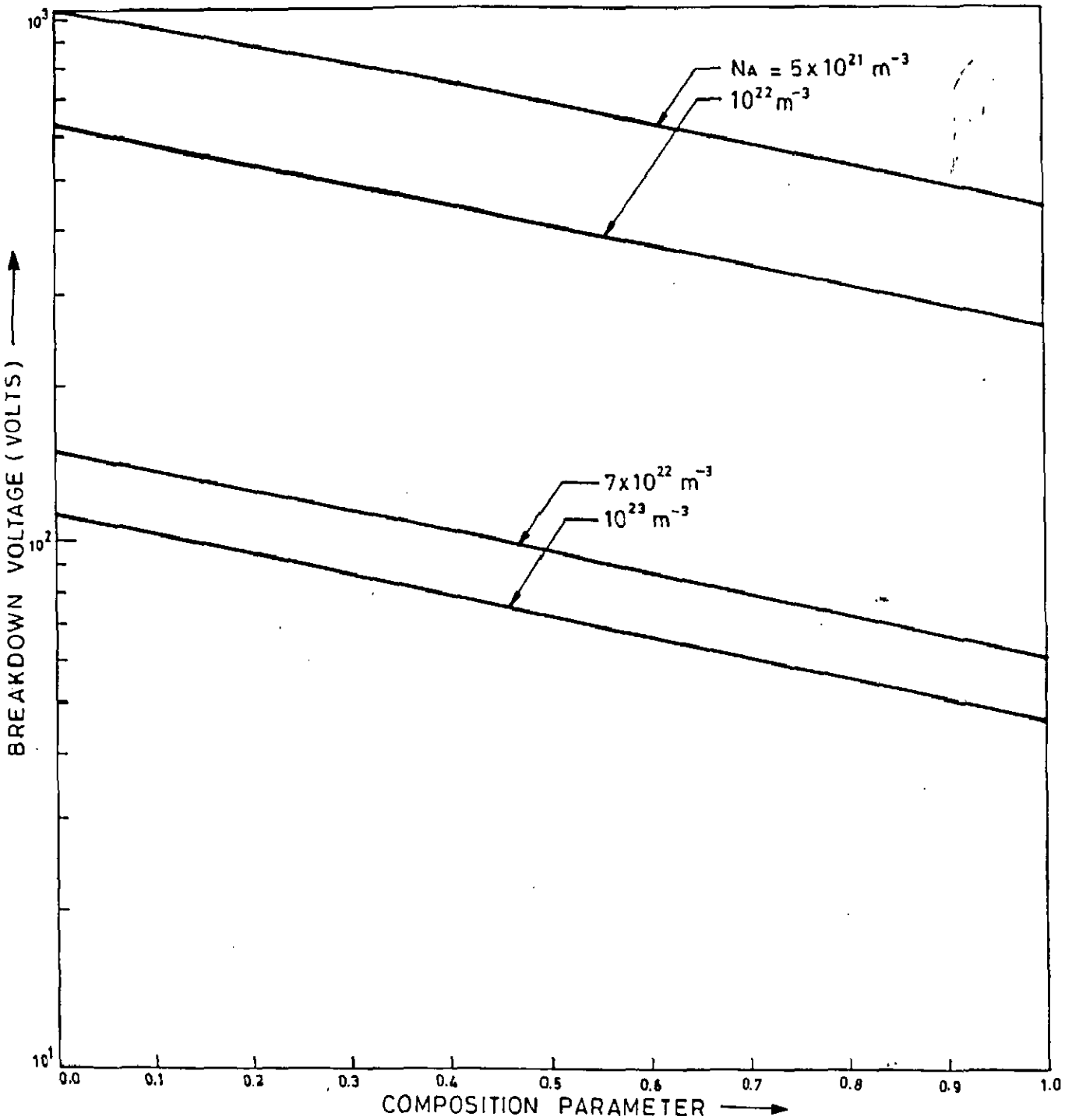


FIG. 5.2 BREAKDOWN VOLTAGE AS FUNCTION OF COMPOSITION PARAMETER FOR DIFFERENT IMPURITY CONCENTRATION.

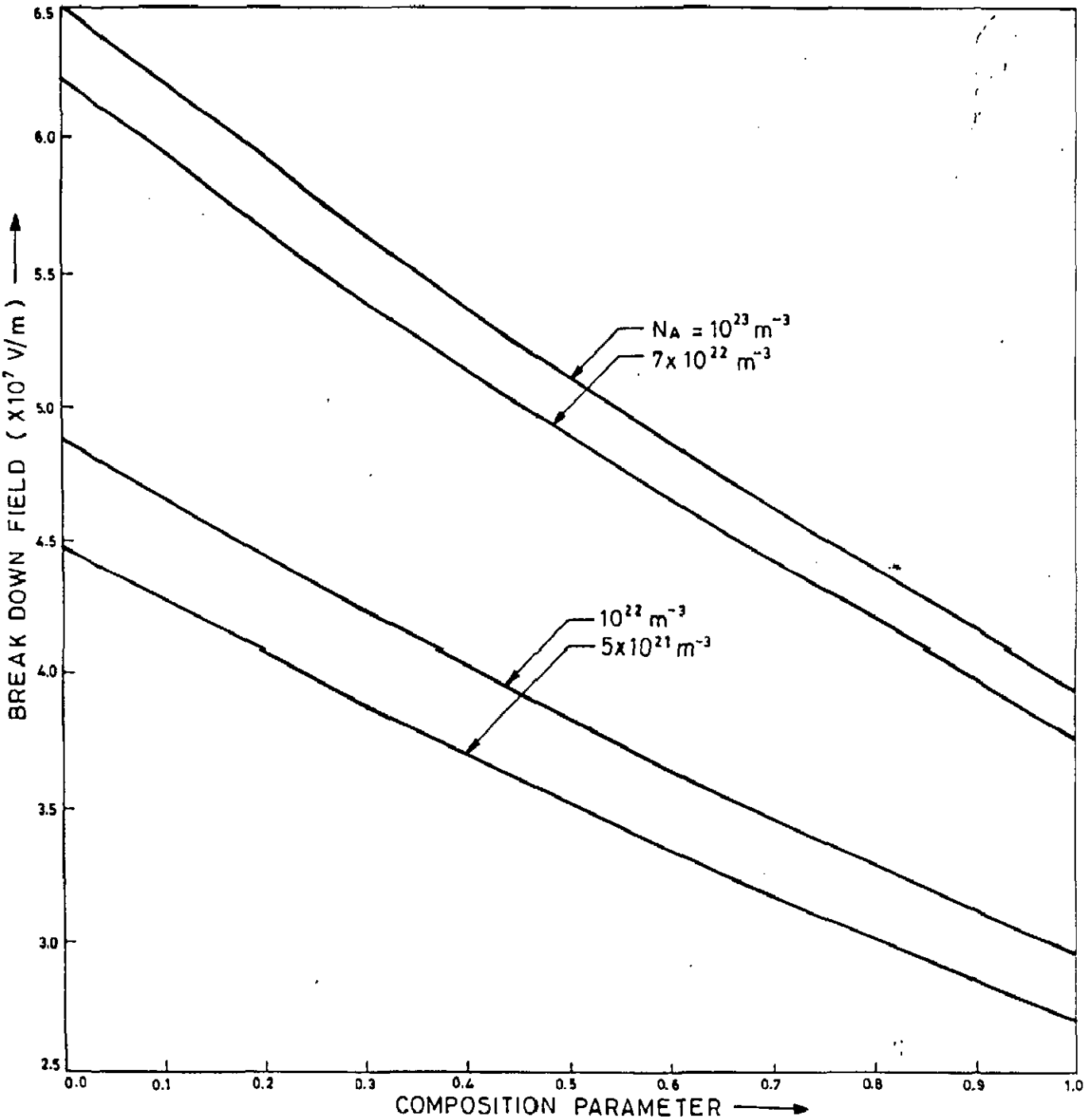


FIG. 5.3 BREAK DOWN FIELD AS FUNCTION OF COMPOSITION PARAMETER FOR DIFFERENT IMPURITY CONCENTRATION.

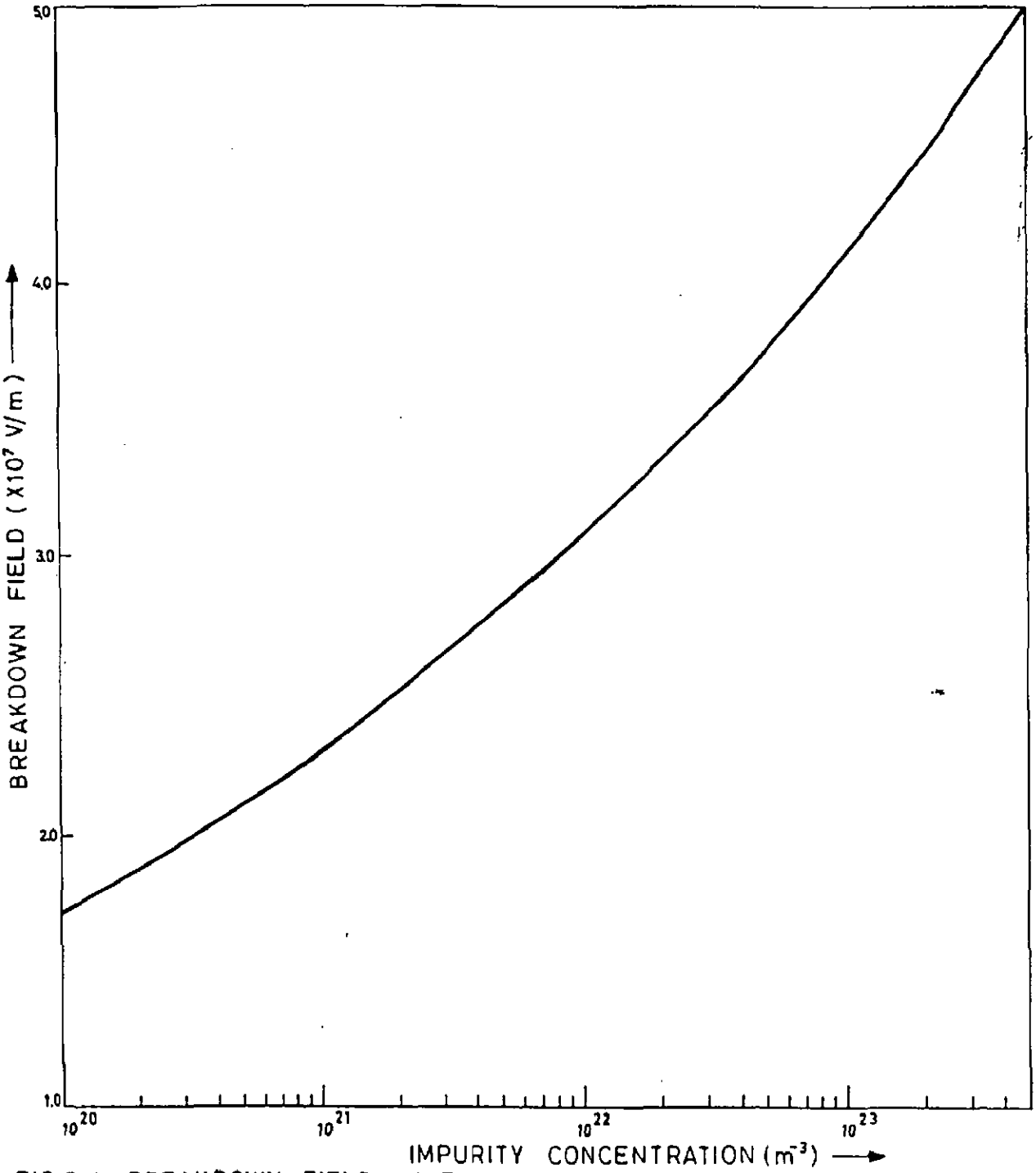


FIG.5.4 BREAKDOWN FIELD AS FUNCTION OF IMPURITY CONCENTRATION IN InGaAs p-n JUNCTION.

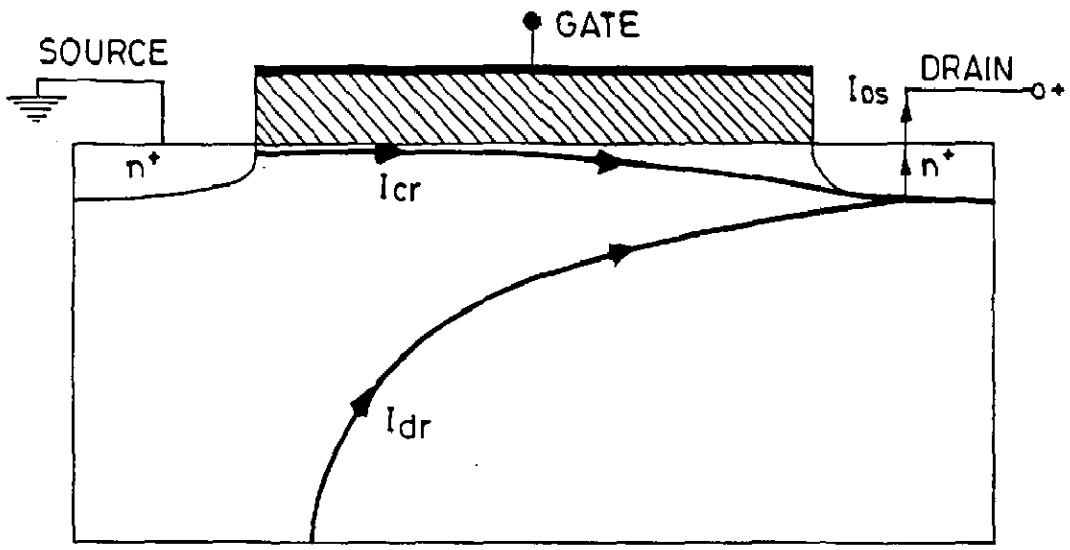


FIG. 5.5 DEPICTS THE PATTERN OF THE TWO COMPONENTS OF DRAIN CURRENT.

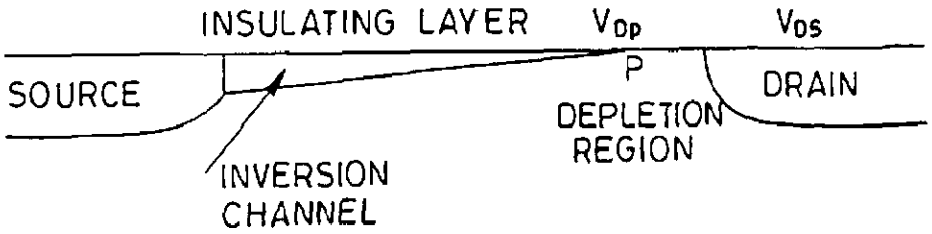


FIG. 5.6 INVERSION AND DEPLETION REGIONS IN THE CHANNEL.

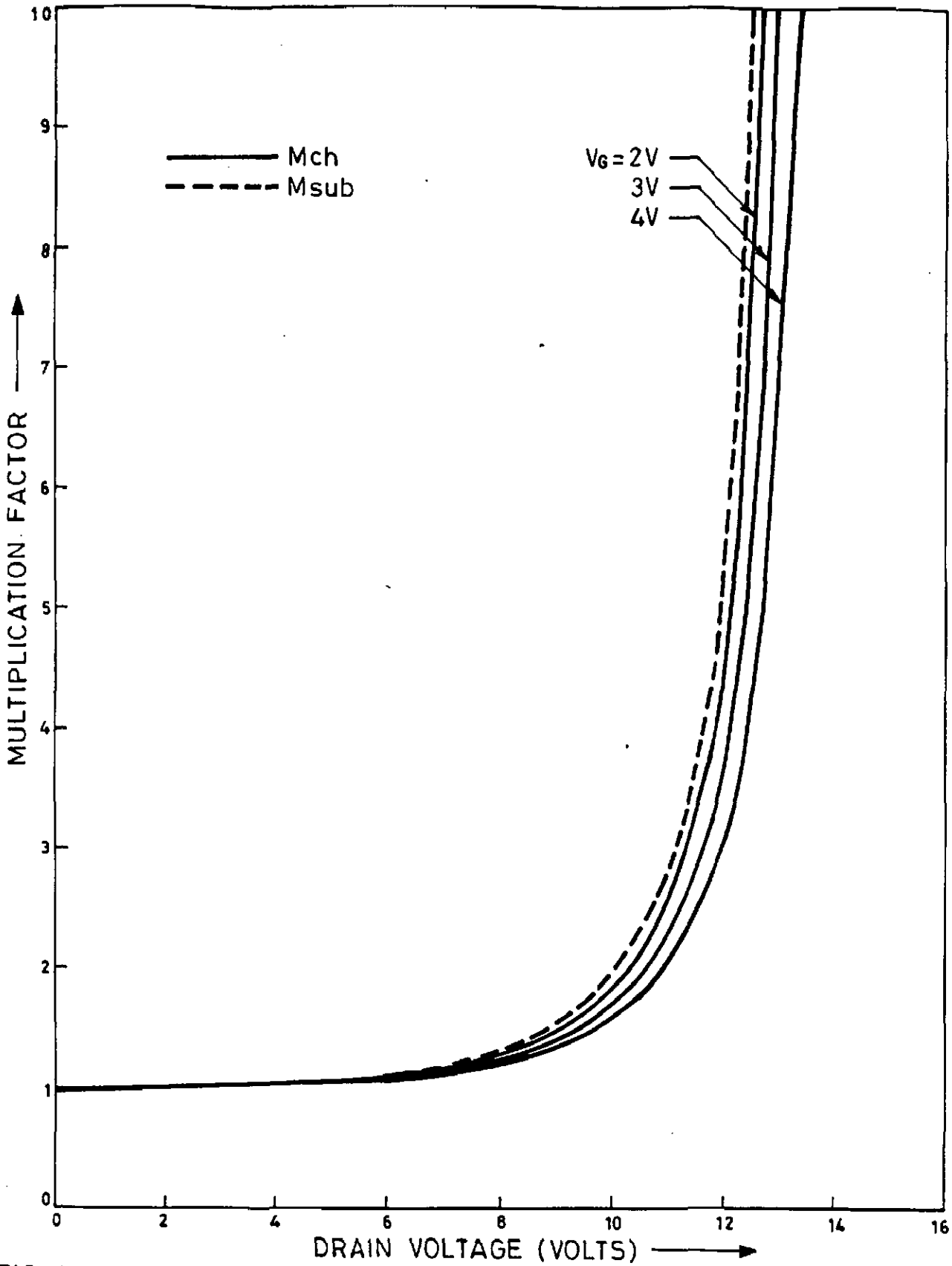


FIG. 5.7 CHANNEL AND DRAIN-DIODE MULTIPLICATION FACTOR AS FUNCTION OF DRAIN VOLTAGE FOR DIFFERENT GATE VOLTAGE IN InGaAs MISFET.

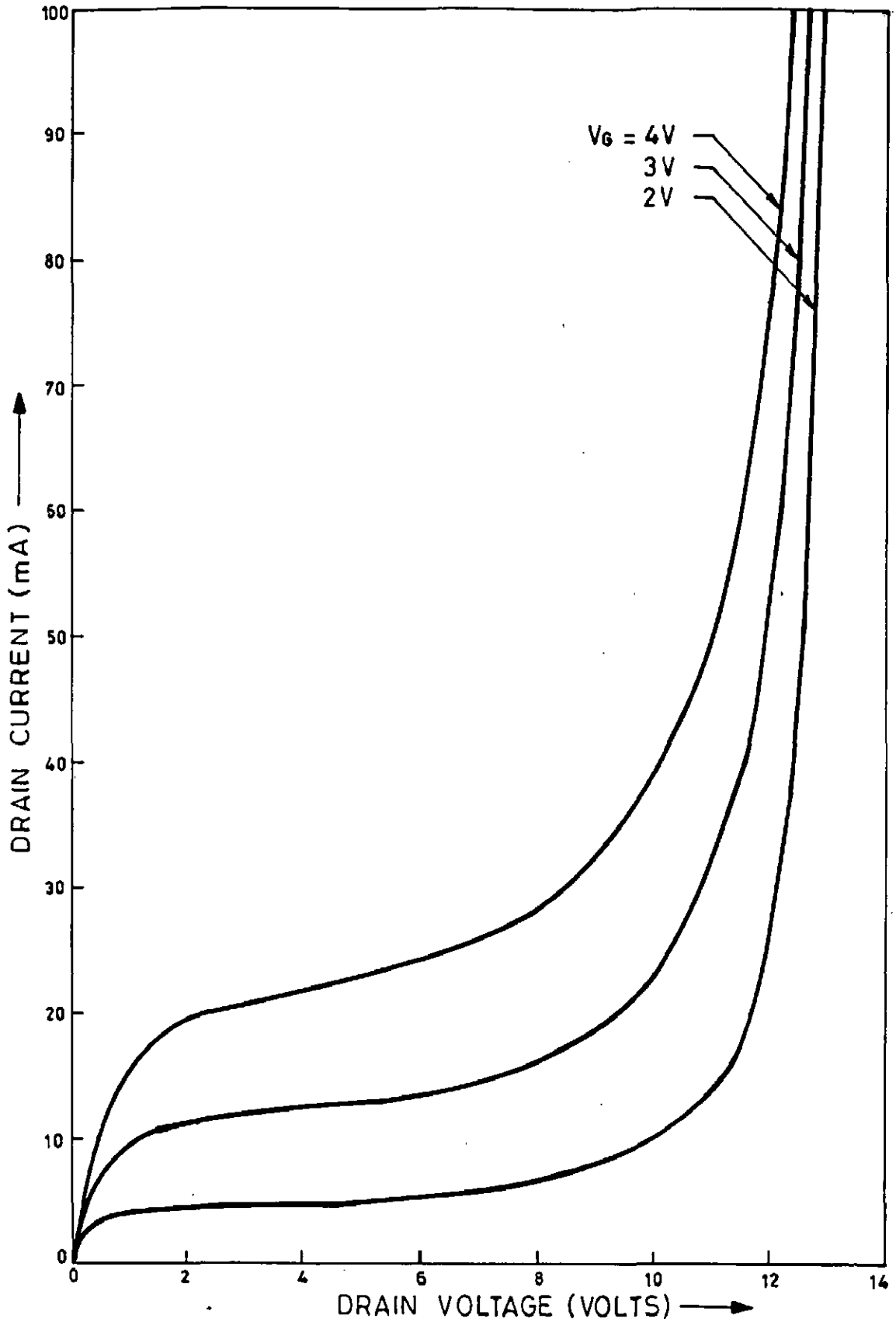


FIG. 5.8 DRAIN CHARACTERISTICS IN THE BREAKDOWN REGION WITH GATE VOLTAGE AS PARAMETER IN InGaAs MISFET.

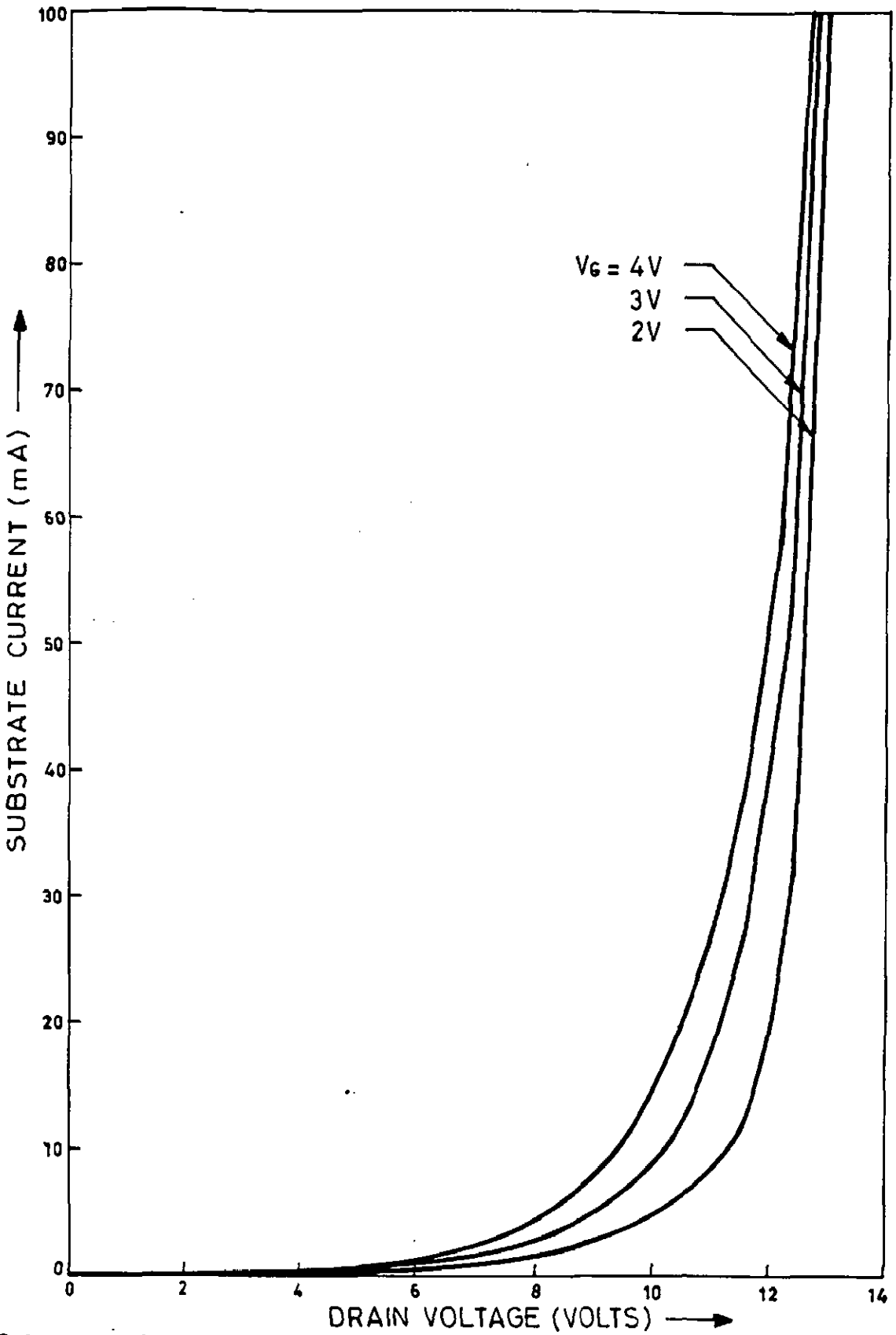


FIG. 5.9 SUBSTRATE CURRENT AS A FUNCTION OF DRAIN VOLTAGE WITH GATE VOLTAGE AS PARAMETER IN InGaAs MISFET.

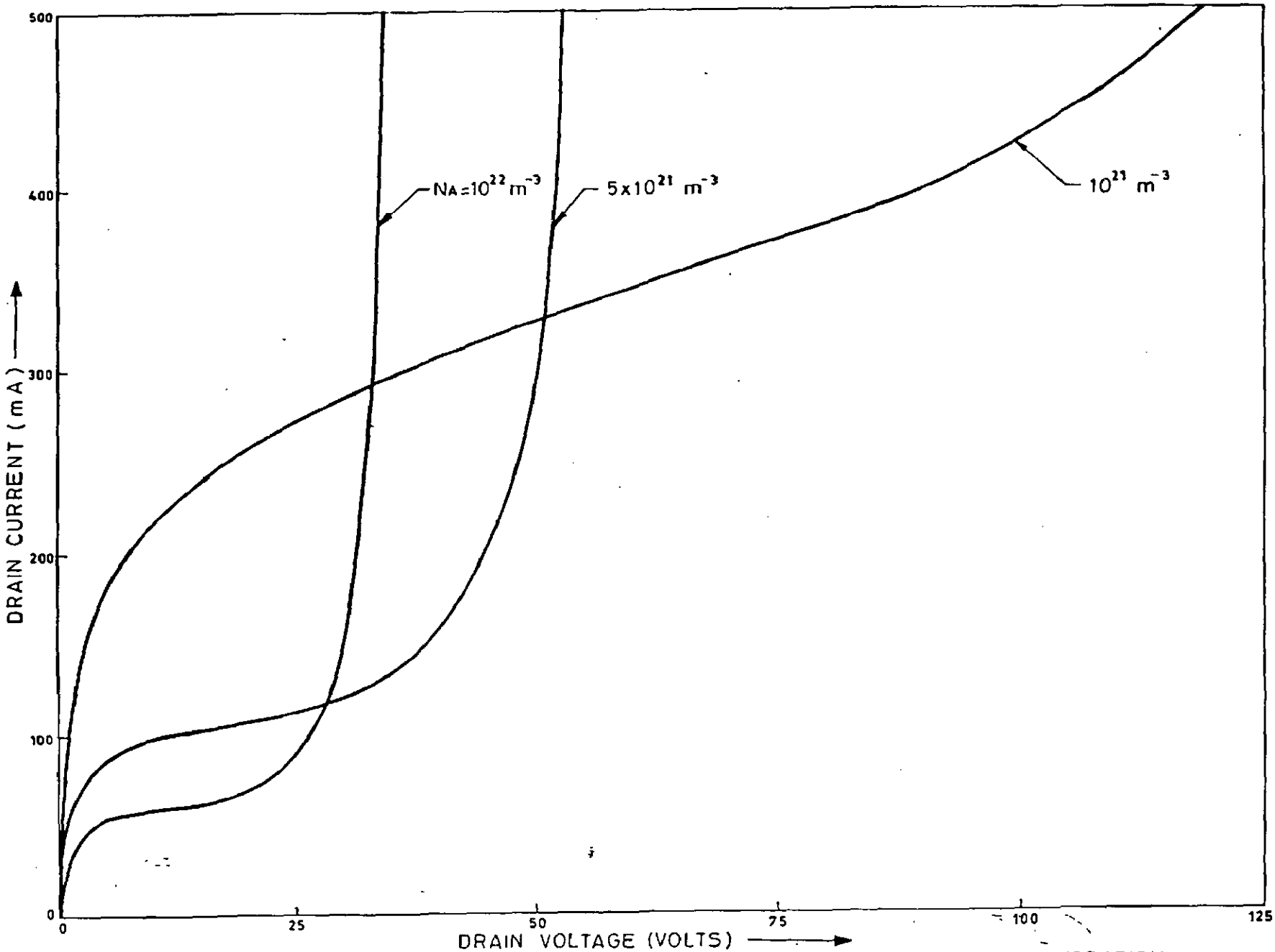


FIG. 5.10 DRAIN CHARACTERISTICS IN THE BREAK DOWN REGION WITH IMPURITY CONCENTRATION AS PARAMETER IN InGaAs MISFET.

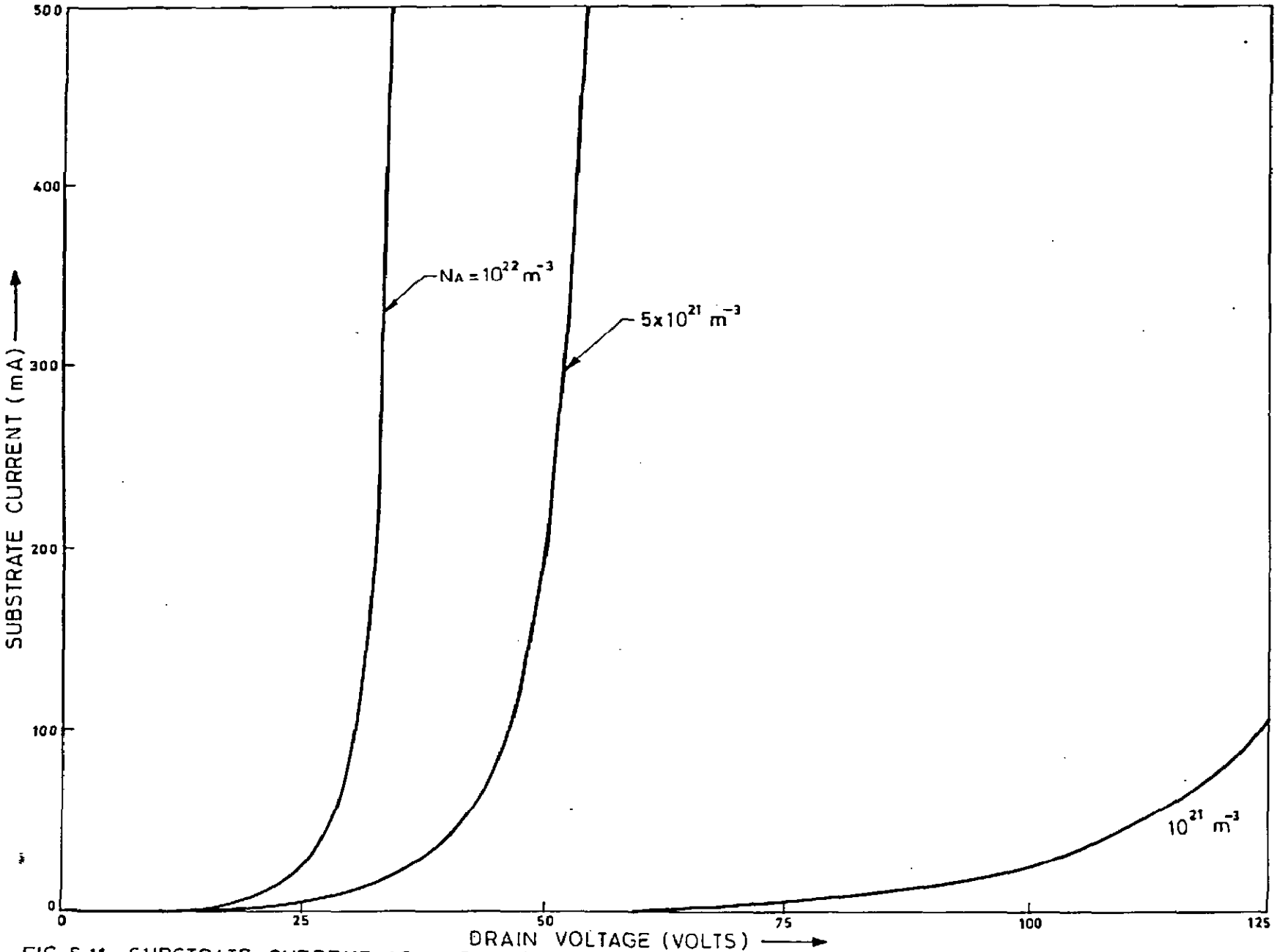


FIG. 5.11 SUBSTRATE CURRENT AS A FUNCTION OF DRAIN VOLTAGE WITH IMPURITY CONCENTRATION AS PARAMETER IN InGaAs MISFET.

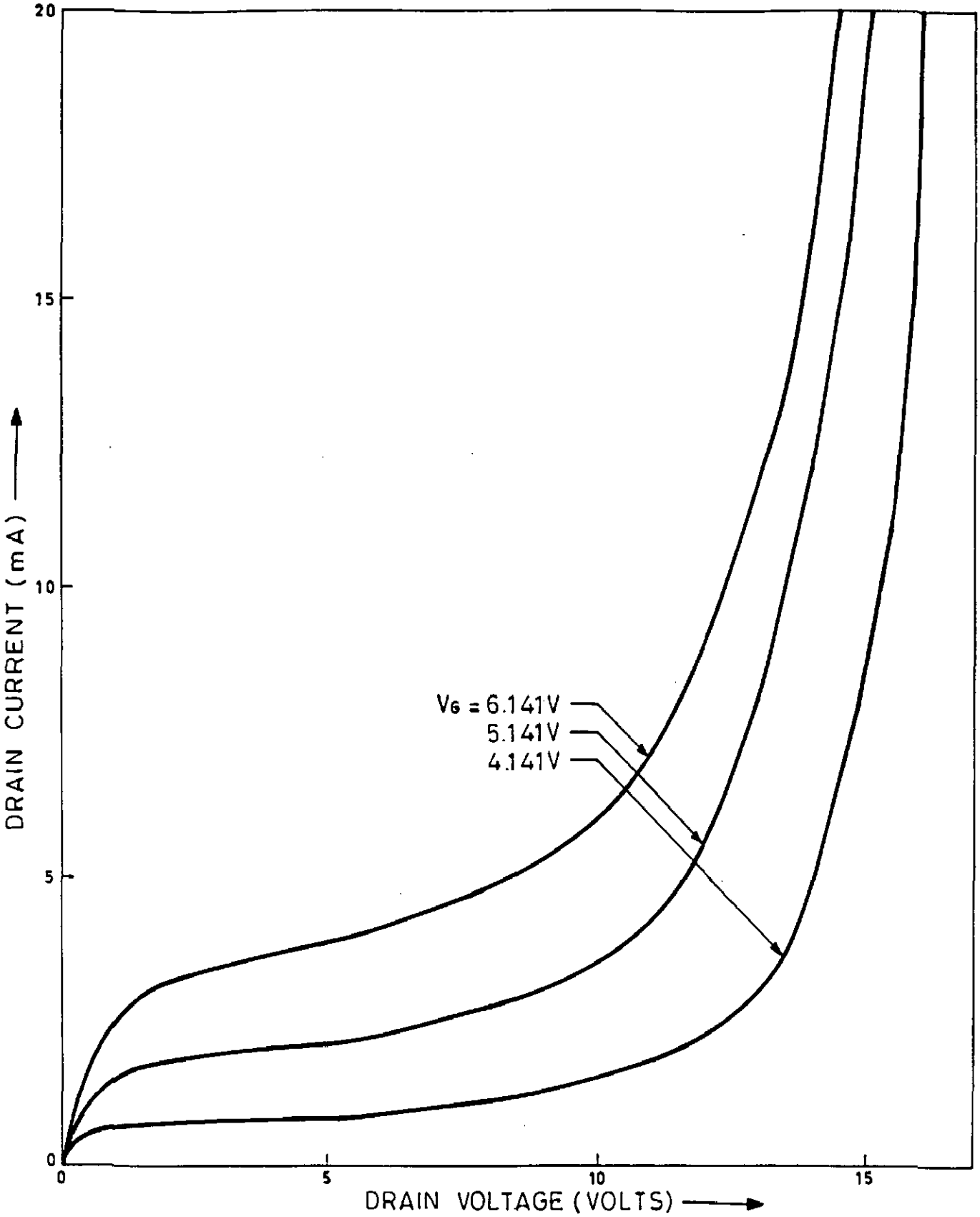


FIG. 5.12 DRAIN CHARACTERISTICS IN THE BREAKDOWN REGION WITH GATE VOLTAGE AS PARAMETER IN Si MISFET.

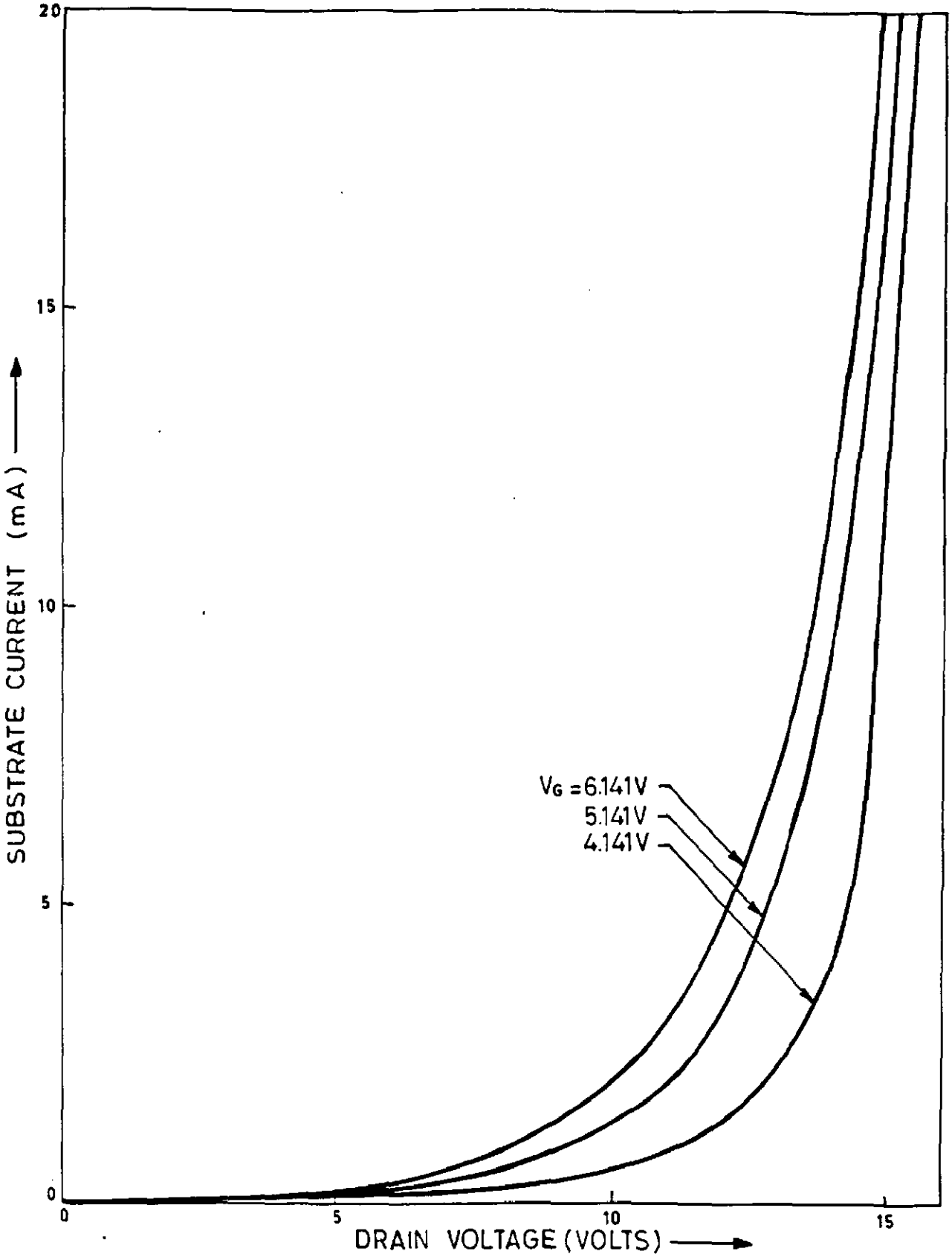


FIG. 5.13 SUBSTRATE CURRENT AS A FUNCTION OF DRAIN VOLTAGE FOR DIFFERENT GATE VOLTAGE IN Si MISFET.

chapter VI

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

6.1 INTRODUCTION

A very promising future seems to opening up for III - V semiconductors for applications in the fabrication of advanced discrete and integrated circuits involving high-speed digital, microwave and opto-electronic devices. The III - V compound semiconductors such as GaAs, InP, InGaAsP and InGaAs with high electron saturation velocities and mobilities are capable of meeting high-speed requirements in microprocessors and semiconductor memories. However, the compound semiconductors are not so much in use as substrate materials for integrated circuits. This is due to the fact that synthesis and material technology of such alloys are more complicated than those of silicon. Furthermore, the physical and chemical properties of the surfaces and interfaces between these alloys and insulating layers impose severe constraints on their technological utilization. In spite of these limitations the compound semiconductors are superior than silicon for many potential applications.

In view of high electrical qualities and the capability of meeting high-speed requirements, considerable attention has been focused on the development and analysis of n-channel inversion-mode $In_{1-x}Ga_xAs_yP_{1-y}$ MISFET. As a consequence efforts have been made to develop a III - V compound MISFET technology. The most well understood III - V compound semiconductor is GaAs. In spite of its impressive electrical properties, the advancement of GaAs MISFET-technology is delayed

due to non-availability of ideal insulating film for gate insulator. This arises out of the fact that high density of surface states at the GaAs-insulator interface confines the Fermi level to the lower portion of bandgap. This prevents formation of n-inversion layer in the GaAs MIS-system. More recent investigations reveal that n-channel inversion-mode MISFETs are feasible in $In_{1-x}Ga_xAs_yP_{1-y}$-system. In these alloy system the material parameters change with change in composition parameters x and y. This in turn changes carrier mobility and surface state density. Experimental investigations have shown that InGaAs/InP based MISFETs have highest carrier mobility and lowest surface state density. These impressive results for InGaAs MISFETs further enhanced the scope of the InGaAs MISFETs for high-speed digital circuit applications. However, these devices are not yet fully developed and several technological problems will have to be sorted out before a viable InGaAs MIS-technology is established and the device is commercialized. Most of the investigations carried out so far are experimental in nature and very little theoretical analysis of carrier mobility, drain characteristics and breakdown voltage in InGaAs MISFETs have been made. Such analysis of physical processes involved in the operation of a device not only helps in understanding the device behaviour but also makes contributions towards its further development. The preceding chapters of the thesis have been devoted to an analytical study of n-channel inversion-mode MISFETs. These analysis discusses the conclusions drawn on the basis of the analytical studies. The scope for further studies in the area of thesis is also briefly described.

6.2 SUMMARY AND CONCLUSIONS

The work presented in this thesis first analyses the electrical properties of inversion channel on p-type InGaAs and related semiconductor of the InGaAsP-family. In an n-channel MISFET, p-type surface is inverted by an electric field. The field is developed as a result of potential drop across gate insulator. This electric field controls the electrical behaviour in the channel region. The parameters characterizing the electrical behaviour in the inversion channel are primarily the surface potential, inversion channel carrier concentration and channel mobility. For the same gate voltage the surface field in $In_{1-x}Ga_xAs_yP_{1-y}$ MISFET is different for different composition parameter y owing to its dependence on material parameters, such as semiconductor permittivity, bandgap energy and intrinsic carrier concentration etc. Using the gate-channel charge balance equation, surface potential as a function of effective gate voltage is calculated for several y-composition parameters. The calculated results demonstrate that the effective gate voltage required for the onset of strong inversion is composition dependent and it is lowest for InGaAs MISFET. It is also shown that the degree of inversion in InGaAs MISFET is relatively much higher than in MISFETs made on other semiconductors including silicon. The surface potential is also dependent on interface and fixed oxide charge. The present analysis, therefore, indicates that an excellent gate control on an inversion channel in InGaAs can be realized if good insulator-semiconductor interface properties can be achieved.

With the application of gate voltage, inversion charge is induced in the channel. The induced channel charge along with depletion layer charge plays an important role in determining the

channel conductivity. By the aid of established MISFET equations the channel carrier concentrations in $In_{1-x}Ga_xAs_yP_{1-y}$ MISFETs of various compositions along with that for silicon MISFET are determined as a function of effective gate voltage. The calculations show that the inversion carrier concentration is not significantly different in MISFETs of different materials. However, marked increase in carrier concentration takes place at higher gate voltages. Furthermore, in InGaAs MIS-system, inversion carrier concentration increases with increase in y-composition parameter. This difference in channel carrier concentration comes through the material parameter dependence of surface potential. The pattern of channel carrier concentration variation with effective gate voltage follows that of surface potential. The calculation also show that InGaAs MIS-system relatively has the highest channel carrier concentration as compared to those in InP, InGaAsP and Si MIS-system.

In a MIS-system, the effective field at the semiconductor surface due to gate voltage, depends upon depletion layer and inversion layer charge densities which are functions of gate voltage. Using a commonly used expression for effective field in MISFETs it is found that effective field is relatively higher in InGaAs MISFET than in Si counterpart. For lower gate voltage this is primarily due to higher semiconductor permittivity in InGaAs. The calculated results also demonstrate that inversion layer charge density is lower and depletion layer charge density is higher in Si than in InGaAs-system. The difference in InGaAs and Si widens in the higher effective gate voltage range. Higher inversion charge density in InGaAs MISFET is mainly responsible for relatively higher effective field in the higher gate voltage

range. These results indicate that InGaAs MISFET is more sensitive to gate voltage control than silicon. Thus, it may be concluded that InGaAs is a close competitor of silicon for MIS device applications.

In a MISFET, the inversion layer forms the conducting path between source and drain contact. The channel conductivity is modulated by varying gate voltage. As a consequence of this to a great extent the drain current varies in accordance with variation in carrier mobility under the influence of normal and lateral electric fields. Under this situation quantitative assessment of carrier mobility becomes important. The parameter, effective mobility characterizes the field dependence of channel mobility. It is a well accepted fact that effective mobility is a function of drain conductance and channel carrier concentration. The drain conductance being itself a function of channel carrier concentration it is the latter that is the controlling factor. For $In_{1-x}Ga_xAs_yP_{1-y}$ MISFET, the channel carrier concentration is a function of the composition parameter y. Thus effective mobility varies with alloy composition. The effective mobility is found to decrease with increase in effective field in the channel. Thus as effective field increases with increase in gate voltage the effective mobility decreases.

For the purpose of quantitative assessment of composition dependence of effective mobility in $In_{1-x}Ga_xAs_yP_{1-y}$ MISFETs, the effective mobilities in such MISFETs are calculated from experimental data reported by Shinoda and Kobayashi [202] and simple drain conductance expression used in MIS-theory. Experimental data for three cases of y = 0, 0.29 and 0.55 are

taken. The channel carrier concentration for three cases are determined by using the gate-channel charge balance equation. The results show that effective mobility increases with increase in y-composition parameter. Considering the fact that effective mobility is inversely proportional to the channel carrier concentration which is an increasing function of y-composition parameter, the increase in effective mobility with y is attributed to increase in drain conductance. The dependence of effective mobility on gate voltage for MISFETs of different y-parameter is also studied. It is observed that there is significant degradation in mobility with increase in gate voltage for higher values of y. For InP MISFET (y = 0),effective mobility is almost constant over a wide range of gate voltage. For y = 0.29, a nominal mobility degradation occurs, for y = 0.55, effective mobility degrades significantly. Gardner et al.[71] also reported similar mobility degradation in InGaAs MISFET. These results indicate that higher effective mobility can be realized by increasing y-composition parameter. However, this is achieved at the expense of severe mobility degradation with increase in gate voltage.

To explain the observed degradation of effective mobility with increase in gate voltage, a Matthiessen's rule approach is taken. An expression for effective mobility in terms of various governing factors has been obtained. One of the parameters involved in the expression is the bulk mobility. Experimental and theoretical investigations carried out in the past confirm that in InGaAsP-system, the bulk mobility increases with incerase in y-composition parameter. Thus it may be concluded that the increase in effective mobility with increase in the composition

parameter y, is partly because of the corresponding increase in bulk mobility. Another y-dependent parameter in the expression for effective mobility is the electron effective mass. The expression indicates that decrease in effective mass increases effective mobility. Numerous experimental investigations reported in literature established that electron effective mass in InGaAsP-system decreases with increase in y-composition parameter. Furthermore, lower effective mass means higher bulk mobility. Thus, decrease in effective mass with increase in y-composition parameter has a two-fold effect on the effective mobility.

In the expression for effective mobility, two factors are identified as the scattering factor and the screening factor. Decrease in channel thickness confines the inversion carriers closer to the surface. As a consequence, with reduction in channel thickness surface scattering (due to surface roughness and phonons) increases. This makes the scattering factor in the effective mobility expression to be inversely proportional to the channel thickness. Quantum-mechanical considerations show that channel thickness decreases with increase in gate voltage, through its dependence on effective field on the semiconductor surface. The effective field being a function of alloy composition, makes the channel thickness in InGaAsP MISFET to be dependent on the y-composition parameter. The present analysis shows that the channel thickness increases with increase in y-composition parameter. These results lead to the conclusion that with a thicker channel, InGaAs MISFETs have the benefit of lesser surface scattering and hence higher effective mobility. Effective mobility obtained as function of y-composition

parameter also confirms this.

As the gate voltage is increased, channel thickness in a MISFET decreases and effective mobility tends to fall as a result of increased surface scattering. At the same time, with increase in gate voltage, channel carrier concentration also increases. The decrease in channel thickness along with increase in channel carrier concentration gives rise to an enhancement of volume concentration of carriers in the channel. With this the surface fixed charges are screened from the carriers, thereby reducing fixed charge scattering and tending to improve effective mobility. This is accounted for by a screening factor in the effective mobility expression. Thus, with increase in gate voltage two competitive mechanism come into play which have opposite effects on the effective mobility. The present analysis shows that the screening factor decreases as the gate voltage is increased. The fall in screening factor with increase in gate voltage has varying rates. The rate of fall of the screening factor is very rapid over the lower ranges of gate voltage. At the higher ranges of the gate voltage, the rate of change of the screening factor is considerably reduced. The variation of effective mobility with gate voltage is, therefore, jointly determined by the rate of change of the scattering and screening factor. In the lower range of the gate voltage the screening factor either dominates over or neutralizes the scattering factor. This is the reason why in some MISFETs (e.g. MISFETs of $y = 0.29$ and 0.0) some increase in effective mobility with increase in gate voltage is observed over the lower range of the gate voltage.

At higher gate voltages, the channel being extremely thin, surface scattering dominates over screening. This explains why effective mobility degradation with increase in gate voltage is usually observed at the higher gate voltages. As both scattering and screening factor are composition dependent in InGaAsP MISFETs, the two processes have their effects on effective mobility by different degrees if the y-composition parameter is different. For example, over a large range of gate voltage, no effective mobility degadation is observed in InP MISFET. In such a case, the two factors cancel the effect of one another over a wide range of gate voltage. Analysis of alloy composition dependence of the screening and scattering factor show that the two factors decrease with increase in y-composition parameter. For higher values of y, the scattering factor increases much more rapidly in comparison with the fall rate of the screening factor. This difference in rate of change of the two factors is the cause of severe effective mobility degradation that results from increase in gate voltage in case of high-y InGaAsP MISFETs. The case of InGaAs MISFET is a typical example of this phenomenon. On the other hand for smaller values of y, the screening and scattering factors vary almost at the same rate as gate voltage is varied. In such cases, therefore, no appreciable change in effective mobility is observed when gate voltage is changed. InP MISFETs are example of such transistors.

The analysis of the behaviour of surface potential and effective mobility under the influence of gate voltage give ample evidence that InGaAs is a promising material for MISFET application. The high electron mobility and low threshold voltage of the n-channel inversion-mode InGaAs MISFET make it an

attractive device for high-speed digital applications.

After an assessment of InGaAs as a substrate material for MISFET application, the thesis devotes itself to the study of various aspects of n-channel inversion-mode InGaAs MISFET operation. A MISFET is best analysed by the aid of a suitable model. To meet this end a long-channel MISFET-model is developed. The model takes into account the influences of both gate and drain fields on the electrical properties of the inversion channel. The drain current is formulated as being composed of drift and diffusion components. The model is, therefore, different from many other models reported in literature as the diffusion current in the channel is not neglected. The intentions behind retaining the diffusion component of the drain current are to serve two purposes. Firstly, the electron effective mobility in inversion channel formed on InGaAs-surface is extremely large. Such a high mobility results in a large diffusion constant for the electrons. With a high diffusion constant, the contribution of the diffusion current is not necessarily a negligible quantity. The other purpose served is one of mathematical advantage. If the diffusion component of drain current is neglected, one arrives at a first order non-linear differential equation, that describes potential distribution along the length of the channel. Such an equation when solved numerically, fails to converge at all points along the channel. In such a situation, two equations are required. One convergent over certain distance from the source, while other convergent over the rest of the channel [268]. By retaining the diffusion current component, the model developed yields a second order non-linear differential equation, which could be solved numerically, over the entire

length of the channel extending between the source and the drain. Furthermore, the retention of the diffusion current component also widens the scope of the model, as it can be used to analyse the subthreshold region of the MISFET operation.

One of the important physical quantity involved in the MISFET-model is the effective mobility. The effective mobility expression, derived by Matthiessen's rule approach involves certain parameters which cannot be easily estimated in practice. An alternative is to express effective mobility in terms of measurable parameters commonly designated as μ_0, E_c and θ_s. The parameter μ_0 is the low-field carrier mobility in the channel, E_c is critical electric field that characterizes both μ_0 and θ_s. The parameter θ_s is also dependent on the insulator thickness. As the measurements of the mobility parameters μ_0, E_c and θ_s are comparatively easier than some of the parameters involved in the Matthiessen's rule based effective mobility expression, effective mobility as function of μ_0, E_c and θ_s is widely used in silicon MISFET analysis and modeling. The measurements of μ_0, E_c and θ_s is, however, not too simple. These measurements require elaborate laboratory facilities and laborious experimentation. In order to avoid these complications, a simpler approach is used in the present work. In this method of extracting the mobility parameters, the MISFET-model itself is used. Only experimental data required is a set of measured drain conductance at different gate voltage, for an extremely low drain voltage. To demonstrate the technique, data for InGaAs MISFET as available in literature are taken.

The method of effective mobility parameter estimation

relies on accurate determination of the parameter E_c. From the well known relationship between E_c and μ_0 and that between E_c and θ_s, the other two parameters are determined. For the estimation of E_c, the commonly used drain conductance equation has been used to develop a suitable working equation. The parameters have been determined for various gate voltages and then averaged. The average values of the parameters are then used to determine the drain characteristics of the InGaAs MISFET with the aid of the model developed. It is found that, if the parameters are averaged over a very wide range of gate voltage, very good agreement between the calculated and experimentally obtained characteristics is achieved. The agreement is better at lower gate and drain voltages. This is attributed to the facts that the model is basically a long-channel model and it does not account for velocity saturation effect. At very high drain voltage, there is a tendency for the carrier velocity to saturate. Also, if the gate voltage is high then, the drain voltage for velocity saturation is lower. From these observations, it is concluded that the model is suitable for long-channel devices only. If the device is not so long, then the model is applicable to lower gate voltages only. However, the agreement between the experimental and the theoretical results indicate the validity of the model. At the same time it also shows that effective mobility expression in terms of parameter μ_0, E_c and θ_s can well be applied to InGaAs MISFET as successfully as it is applied in the case of silicon MISFETs.

After establishing the validity of the MISFET-model, the same is applied for further analysis of InGaAs MISFET. The low-field mobility parameter μ_0, which appears in the effective

mobility expression is dependent on substrate doping level. An expression for μ_0 in terms of substrate impurity concentration, by combining the mobility analysis of Wong [259] and Hilsum [97]. This expression is incorporated in the present MISFET-model. With this modification, the substrate doping dependence of drain characteristics of a long-channel InGaAs MISFET are analysed. It is seen from the analysis that for higher doping levels the saturation drain current and drain voltage for pinch-off are both lower. Extremely high level of drain current is obtained at comparatively lower doping levels. The model is also applied to the cases of InP and silicon MISFETs. It is found that the III - V compound semiconductors yield MISFETs of higher operating current than silicon MISFETs. Of the two III - V MISFETs, InGaAs-one has higher operating current. The analysis shows that the level of operating current is closely related to effective mobility. InGaAs MISFETs having the highest effective mobility, are of highest operating current level.

The comparison between InGaAs, InP and silicon MISFETs show that the drain voltage for pinch-off is highest in InGaAs MISFET and it is lowest for the silicon MISFET, with the pinch-off drain voltage for InP MISFET lying between the two extremes. It is shown analytically that the cause of this substrate material dependence of pinch-off drain voltage is due to two factors :

1. interface state density and
2. bulk potential.

The interface state density in the III - V compound semiconductor MISFETs is much higher than what it is in silicon MISFETs. The high interface state density gives rise to a high flat-band voltage which increases the pinch-off drain voltage. Higher bulk

potential means higher pinch-off drain voltage. The bulk potential in silicon is relatively lower because of its lower intrinsic carrier concentration. InGaAs, having the highest intrinsic carrier concentration has the highest bulk potential. The high bulk potential in InGaAs is primary reason for the high drain voltage for pinch-off. Making use of the MISFET-model, the drain conductance variation with drain voltage in InGaAs MISFET is also studied. It is found that owing to relatively larger increase in drain current in saturation region, the saturation drain conductance in InGaAs MISFET is comparatively higher than what it is in silicon MISFET.

The output characteristics of any device is governed by internal fields, potential and charge distribution. The model developed is self-sufficient to estimate these quantities at all points in the channel of MISFET. Using this model the potential distribution along the channel of an InGaAs MISFET is determined. It is seen that the potential variation from source end to the drain end is in general non-linear. Such non-linear potential distribution is also known to exist in inversion-mode silicon MISFET. The calculations for silicon MISFET with the present model also varify this. It is also found that the non-lineaity is increased with reduction in gate voltage. At very high gate voltages the potential distribution can be approximated to be linear without much loss in accuracy. The non-linearity in potential distribution results from the non-linear decrease in channel conductivity towards the drain end. This is of course a result variation in carrier concentration along the length of the channel.

The two dimensional model, which considers the contribution of both gate and drain fields to the induction of carriers in the channel, is used to estimate the gate and drain induced carrier distribution along the channel. The results show that the distribution of gate and drain induced carriers are similar in both InGaAs and silicon MISFETs. However, both type of carriers are of relatively higher concentration in InGaAs MISFET. The present analysis, shows that in InGaAs MISFET the gate induced carrier concentration is higher because of the large flat-band voltage. The high drain induced carrier concentration in InGaAs MISFET is a result of the high permittivity of the substrate material. From the potential variation along the channel, it is seen that the lateral field in InGaAs MISFET is relatively much higher than in silicon MISFET. This is also partly responsible for higher drain induced carrier concentration in the InGaAs MISFET. Thus, the total carrier concentration in the channel of an InGaAs MISFET is higher than in silicon counterpart. As a consequence the drain current in InGaAs MISFET is comparatively higher than an otherwise comparable silicon MISFET.

It is well known that carrier mobility in a semiconductor is a function of electric field. The effective mobility expression used in the model has depletion charge involved in it. The depletion charge being a function of both normal and lateral field makes the effective mobility field dependent. Analysis has been carried out to examine the variation of effective mobility as a function of distance from the source. It is seen that effective mobility decreases towards the drain end. Furthermore, the variation in effective mobility is more prominent at lower gate voltage. These effects indicate that, the fall in carrier

effective mobility with distance from the source results from increased ion scattering in the drain-depletion region. At very high gate voltages enhanced carrier density screens out the ions, and mobility degradation towards the drain end is minimized.

The amplitude of the output signal of a MISFET is limited by, how large a drain voltage can be applied. The upper limit for the drain voltage is set by the power handling capacity of the device. Naturally, this means the allowed drain current level. It is well known that under extremely high electric fields carrier multiplication by impact ionization takes place in semiconductors. As the drain voltage of a MISFET is increased lateral electric field in the channel increases along with an increase in electric field in the depletion layer of the drain-diode. When these field exceeds the critical field for avalanche breakdown by impact ionization, drain breakdown is said to occur. When drain breakdown occurs, an extremely high drain current flows, causing enormous power dissipation and possible damage to the device. Thus, the limit for the drain voltage is determined by impact ionization process in the semiconductor of which MISFET is made. The last chapter of the thesis is devoted to an analysis of drain breakdown in InGaAs MISFET.

The drain breakdown analysis of the MISFET is based on the existing theories on impact ionization in the semiconductors. Considering the fact that InGaAs is the ternary limit of quaternary $In_{1-x}Ga_xAs_yP_{1-y}$, impact ionization in the quaternary is first analysed. The analysis shows that for lattice match condition ($y \simeq 2.2x$) on InP substrate, the breakdown voltage and critical field for breakdown in InGaAsP depends on the alloy

composition parameter y. For all doping levels both breakdown voltage and field decreases with increase in y-composition parameter. Furthermore, the breakdown field is a slowly varying function of the impurity concentration in InGaAs. It has been found that the breakdown field in InGaAs increases with increase in impurity concentration and the breakdown voltage may be approximated by an inverse relation with the doping level.

The analysis is next extended to the study of influence of impact ionization on the drain characteristics of InGaAs MISFET. The analysis assumes that the breakdown occurs by two mechanism, that is, channel breakdown and drain-diode breakdown. The channel breakdown occurs as a result of impact ionization in the drain depletion layer beyond the pinch-off point. The drain-diode breakdown is due to avalanche breakdown in the reverse biased drain-substrate p-n junction. With channel breakdown, the saturated drain current is multiplied by electron-hole pair generation by impact ionization. The primary channel current is determined by the aid of the MISFET-model developed in the preceding chapter. The multiplication factors for both channel and drain-diodes are calculated by the application of Spirito's approximation [212,213]. After calculating the multiplied channel current and drain-diode current, the total drain current is obtained by the sum of the two multiplied currents. Following this approach drain characteristics for InGaAs MISFET are obtained. It is shown that the influence of impact ionization process on the drain characteristics are similar to what has been obtained in silicon MISFETs in the past.

In order to have a better insight into the dependence of

drain breakdown voltage on its various determining factors, a simple expression for drain breakdown voltage is obtained. The expression shows that the drain breakdown voltage is dependent on the semiconductor material parameters through the critical field for breakdown, bulk potential and depletion charge density. In addition to these, the drain breakdown voltage is also determined by insulator capacitance, flat-band voltage and doping level in the substrate. A dependence of drain breakdown voltage on the gate voltage is also indicated. The expression indicates that the drain breakdown voltage increases with increase in gate voltage. This results from decrease in drain depletion region electric field with increase in gate voltage. This effect also reduces channel multiplication factor,thereby reducing the multiplied channel current. The analysis also shows that while channel multiplication factor decreases with increase in gate voltage, the drain-diode multiplication factor is independent of gate voltage.

The drain characteristics obtained by the above approach show the characteristic rise in drain current from on saturation level at very high drain voltages. This rise is very slow for relatively lower drain voltages. As the drain voltage is increased the rate of rise in drain current increases and ultimately undergoes a sudden increase. This behaviour of drain current is a result of the nature of variation of multiplication factors, first increases slowly and then very rapidly. An interesting point to be noted is that while multiplication factor is reduced by increase in gate voltage. This is because of the fact that increase in gate voltage makes the primary channel current to rise by increasing channel carrier concentration.

Thus, although the multiplication factor is decreased, the product of the multiplication factor and channel current is increased. As the multiplied channel current constitutes the major component of drain current, the latter increases with increase in gate voltage. The analysis further shows that the drain breakdown voltage is increased with decrease in impurity concentration in the substrate. This means that in a heavily doped substrate the current saturation occurs over a small range of drain voltage. Normally, it is desired that the drain current saturates over a wider range of drain voltage. In other words, a higher drain breakdown voltage is desirable. Thus, a lightly doped semiconductor is preferable. It is also shown analytically that, in a lightly doped MISFET substrate, the substrate current is also lower. This is also an advantage, as for a small dimension MISFET, the substrate current has some undesirable effects on the operation of the device.

Finally, the effects of channel and drain-diode impact ionization on the drain characteristics of InGaAs and silicon MISFETs have been compared. It is found that, while the basic effects are same, the drain breakdown voltage of a silicon MISFET is comparatively larger than that of an InGaAs MISFET. This is a clear advantage for silicon MISFET. The analysis shows that the major factor responsible for this advantage of silicon MISFET arises out of its relatively higher breakdown field in comparison with InGaAs MISFET.

The study summarized above leads to the conclusion that InGaAs is a potential semiconductor for n-channel inversion-mode MISFETs. Its major advantages are wide variation in surface

potential with gate voltage variation, extremely good response to application of normal field and high channel effective mobility. For analysis of the InGaAs MISFETs, the theories develpoed for silicon MISFET are all applicable. Mobility models developed for silicon MISFETs can be applied to InGaAs MISFET analysis without any error. The study also shows that, elaborate experimentation for the extraction of mobility parameters of a MISFET mobility model can be avoided, if a suitable MISFET-model is available. The distribution of channel electric fields, potentials and carrier densities are similar in InGaAs and silicon MISFETs. However, in InGaAs MISFETs all three quantities are relatively higher. The drain breakdown characterization in InGaAs MISFET are also similar to those in silicon MISFETs. However, the InGaAs MISFETs have relatively lower drain-drain breakdown voltage compared with a silicon MISFET.

6.3 SCOPE FOR FURTHER WORK

The work presented in this thesis mostly centres around a MISFET-model, which is applicable to any inversion channel MISFET, irrespective of the substrate material. This model is basically a long-channel model. There is, however, scope of improving the model to make it applicable to short-channel devices. This would require, modification of the effective mobility model, so that the short-channel effect of velocity saturation is incorporated. The present model can also be applied to subthreshold analysis, provided suitable effective mobility for subthreshold condition is worked out. Thus, further work may be carried out by incorporating provisions to account for velocity saturation and the subthreshold conditions.

The present thesis mainly deals with analysis of the performance of InGaAs MISFETs. It is well known that the InGaAs MISFETs and other III - V compound MISFETs suffer from what is known as drain current drift. Minimization of drain current drift in these MISFETs is one of the major problem that needs more attention than it is given. As these aspect of the InGaAs MISFET have not been considered in the present thesis, further analysis taking into consideration the sources and causes of drift in drain current is suggested.

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