ANALYSIS OF INTERCONNECT PERFORMANCE USING FDTD TECHNIQUE

By

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Enrolment no.: 10550010

A dissertation submitted in partial satisfaction of the
Requirements for the degree
Of
Master of Technology

in

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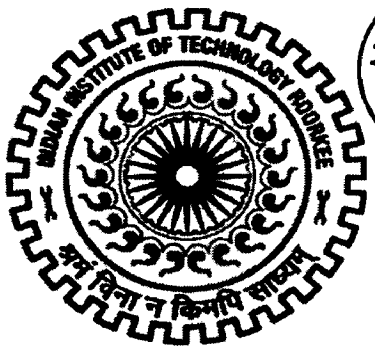

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April, 2012

CANDIDATE'S DECLARATION

I hereby declare that the work presented in this seminar report entitled **"Analysis of Interconnect Performance using FDTD Technique"** for the partial fulfillment of the requirements for the award of the degree of "**Master of Technology**" in "**Solid State Electronic Materials**" is submitted in the Department of Physics, Indian Institute of Technology Roorkee. This report is authentic records of my own work carried out under the guidance of **Dr. K. L. Yadav** (Department of Physics) and **Dr. B. K. Kaushik** (Department of Electronics & Computer Engineering), Indian Institute of Technology Roorkee.

The matter embodied in this report work has not been submitted for the award of any other degree.

Date: 30/04/12
Place: Roorkee

Shailesh Mittal
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CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge and belief.

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ABSTRACT

Device scaling in deep Submicron technology shrinkage the spacing between adjacent interconnect, which leads to increase coupling effect between wires. Continuous device scaling much improved the gates delay. However, interconnect delays have not scaled in that proportion Therefore a need for accurate and computationally effective models in the early stages of the chip design process to assess or optimize issues affecting these interconnects becomes necessary.

This thesis presents the description of a finite difference time domain (FDTD) method that is intended for estimation of voltages and currents on transmission line. Interconnect performance such as crosstalk, delay, crosstalk induce delay are analyzed using FDTD technique. For motivation, analytical results based on proposed model is also compared with HSPICE simulated result. Analytical results are observed in closed agreement with HSPICE results, which proves the validity of proposed model.

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Chapter 1

Introduction

On-chip interconnect system is used for distributing the clock and power supply and connecting signals among circuits. Interconnects in an integrated circuit can be loosely divided into local, intermediate and global interconnects depending on their length, size and metal layer. Local interconnects are the first, or lowest, level of interconnects. They usually connect gates, sources and drain in MOS technology, whereas the semi-global interconnect spanning over large circuits block to connecting devices. Global interconnect span the entire chip connecting the separate functional blocks on integrated circuits. Actually, Global interconnects are used as on-chip interconnect for distributing clock and power signals

In early days, the operating speed of an integrated circuit was limited by speed of a logic gate. Interconnects between the gates were considered as ideal conductors that propagated signals instantaneously and had little effect on circuit operation. However, after introduce of submicron semiconductor devices, this ideal behavior of interconnect is no longer remain adequate [1].

1.1 Deep Submicron Effects

Deep submicron technology build very complicated chips with millions of very fast transistors. Much improvement in chip performance has been due to technology scaling, allowing increased densities at higher clock frequencies. Gate delays which are reduced as their dimensions become smaller. On the other hand, delay of fixed-length wire increases, when its dimensions are scaled [2]. Unfortunately, interconnect delay does not scale with the feature size.

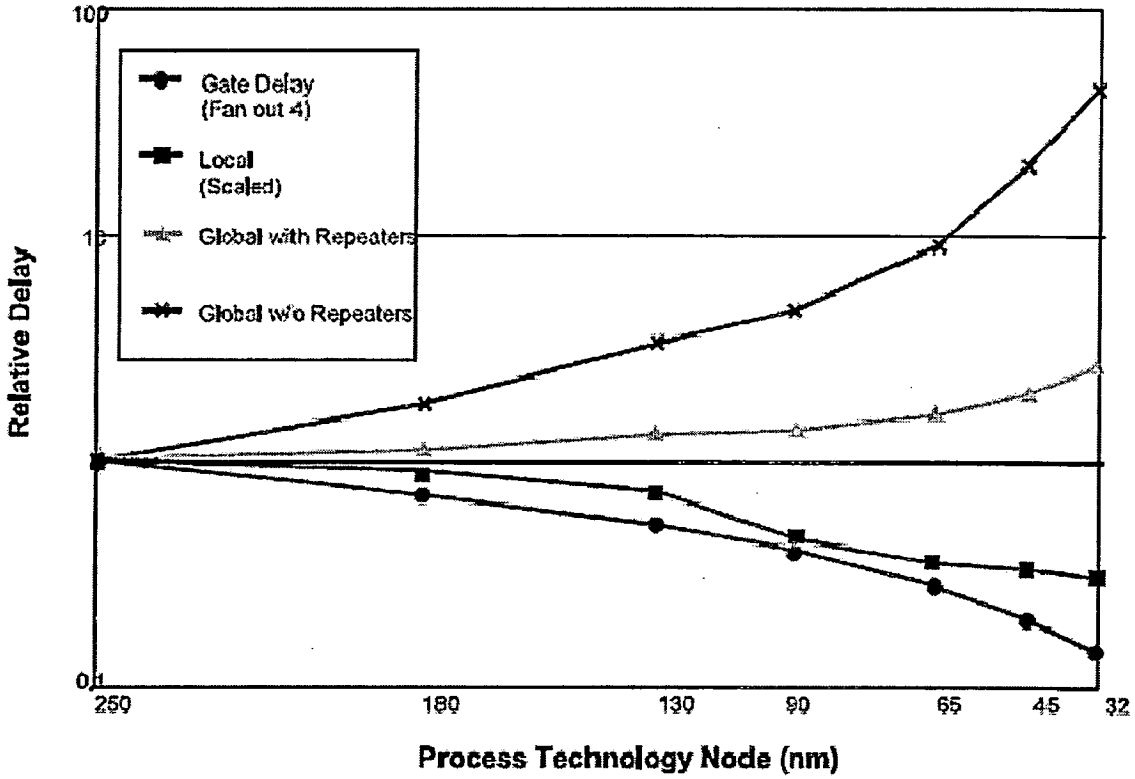

Figure 1.1 Delay for interconnect [3].

Figure 1.1 shows the projections of gate and interconnect delays. The local interconnect is scaled with feature size, while intermediate and global interconnections certainly do not.

For local wires this delay increase is alleviated by the fact that their length is reduced with scaling since they need to connect nearby gates whose sizes diminish with scaling. However, the length of global wires is not scaled with technology since they may need to run across the chip. This has resulted in a growing delay gap between gates and global interconnect.

As the number of devices per unit area increases, interconnection between them must evolve towards a reduced cross-sectional dimension. The reducing cross-sectional dimension leads to more tightly coupled interconnections, and therefore a higher probability of unwanted crosstalk interference between them.

Crosstalk noise can affect the circuit performance in two ways, either by disturbing a quiet line, or by changing the response speed of adjacent switching line. The current is injected into quiet line (victim) during the switching of adjacent line (aggressor) is defined as functional crosstalk. On the other hand, dynamic crosstalk appears due to the simultaneous switching at adjacent lines either in same phase or in opposite phase. Both functional and dynamic coupling noises have equal importance due to the following reasons: (1) the first type of crosstalk noise can cause device or logic failure due to unexpected voltage spike, (2) the second type impacts the critical issue of timing by changing the response time.

In addition, the increase in device density forces a reduction in cross-sectional dimensions that increases Resistance of interconnect wire. This increase in Resistance produces a double effect: one hand, adding to the delay, and on the other hand, producing a signal distortion. Device (transistor) driving capability increases as a result of technology scaling. This means higher frequency components in signals are transmitted through interconnections. as chip speed continually increases, the inductance effect of interconnects tends to increase, which will cause ringing at signal rise/fall edge and changes of crosstalk characteristics. In addition, aggressive usage of high-speed circuit families, scaling of power supply and threshold voltages, and mixed-signal integration combine to make the chips more noise-sensitive [4].

1.2 Problem Statement

The impact of interconnects on circuit performance is ever increasing. No longer interconnects can be treated as ideal wire. Crosstalk, delay, ringing and reflection are just some issues that degrading the time-domain performance of interconnect. Due to these growing delay, signal integrity in interconnects, there has been a shift of focus from devices to wires. This has resulted in a need for novel design tools and models that can be used to analyze and optimize on-chip interconnect.

The investigation reported in this thesis is aimed to develop a finite difference time domain (FDTD) model, for accurate analysis of time-domain performance of interconnect.

1.3 Thesis Organization

This thesis addresses time-domain effects in long on-chip interconnect. More specifically, the focus is on multiple parallel coupled interconnects that are a commonly a part of integrated circuits. The FDTD based model is developed in this thesis for time-domain analysis of coupled interconnect line. Thesis has the following section.

- Chapter 1 introduces the effect of deep submicron technology on Interconnect performance and discusses our research objective.
- Chapter 2 presents different approaches for accurate CMOS-gate driven interconnect. Interconnect modeling and CMOS-gate modeling using alpha-power law model is also discussed.
- Chapter 3 presents a numerical based finite difference time domain, which analytically developed for analysis of interconnect performance.
- Chapter 4 analyze time domain behavior of coupled interconnect based on result obtained through FDTD model. Analytical results also compared with HSPICE simulated result.
- Chapter 5 summarized the work present in this thesis. Future work that can be carried out on this interesting problem is also suggested here.

Chapter 2

Review of Literature

2.1 Interconnect Parasitic

As discussed in last chapter, careful and in-depth analysis of the role and the behavior of the interconnect wire in a semiconductor technology is not only desirable, but even essential. With the introduction of deep-submicron semiconductor technologies, this picture is undergoing rapid changes. The parasitic effects introduced by the wires display a scaling behavior that differs from the active devices such as transistors, and tend to gain in importance as device dimensions are reduced and circuit speed is increased. In fact, they start to dominate some of the relevant metrics of digital integrated circuits such as speed, energy-consumption, and reliability [1].

2.1.1 Interconnect Resistance

It is also called line resistance of interconnect. The resistance of a rectangular interconnects having length L and cross section area A can be expressed as:

$$R=\frac{\rho L}{A}=\frac{\rho L}{HW} \tag{2.1}$$

where the constant ρ is the resistivity of the material (in Ω-m). H and W are height and width of interconnect wire respectively. Aluminum is the interconnect material most often used in

integrated circuits because of its low cost and its compatibility with the standard integrated-circuit fabrication process.

Eq. (2.1) is sufficient at low signal frequencies when the entire cross section of the wire carries the current. However, as the signal frequency increases, the current density starts to fall off exponentially into the conductor. This phenomenon is called skin effect since most of the current is now flowing through the "skin" of the conductor. The skin depth is the depth at which the current density has decreased by a factor e^{-1} of its value at the surface and is given by:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \tag{2.2}$$

Where f is signal frequency and μ is permeability. The onset of the skin effect occurs for frequencies above f_s, the skin frequency. For micro strip interconnects, f_s is the frequency at which δ equals the interconnect thickness and can be solved for by setting $\delta = H$ and $f = f_s$ in equation (2.2), which gives:

$$f_s = \frac{\rho}{\pi H^2 \mu} \tag{2.3}$$

Skin effect decreases the effective cross sectional area that carries the current, which causes resistance to increase. Around 63 % of the total current flows within one skin depth, but one usually makes the approximation that all current flows uniformly within this outer shell of thickness δ. Thus, at high frequencies, the AC-resistance per unit length for a micro strip interconnects is given by:

$$R_{ac} = \sqrt{\frac{\rho \pi f \mu}{W}} \tag{2.4}$$

highly resistive interconnects cause large signal attenuation. As chip complexity and device density increases, wires have to be made narrower, which increases wire resistance according to the basic Eq. (2.1). By making interconnects taller, the cross sectional area of the conductor grows, which helps to lower the resistance.

2.1.2 Interconnect Capacitance

Interconnect Capacitance of a wire is a function of its shape, its environment, its distance to the substrate, and the distance to surrounding wires. Consider first a simple micro strip structure in which, rectangular interconnect wire placed above the semiconductor substrate, as shown in figure 2.1. If the width of the wire is substantially larger than the thickness of the insulating material, it may be assumed that the electrical-field lines are orthogonal to the capacitor plates,

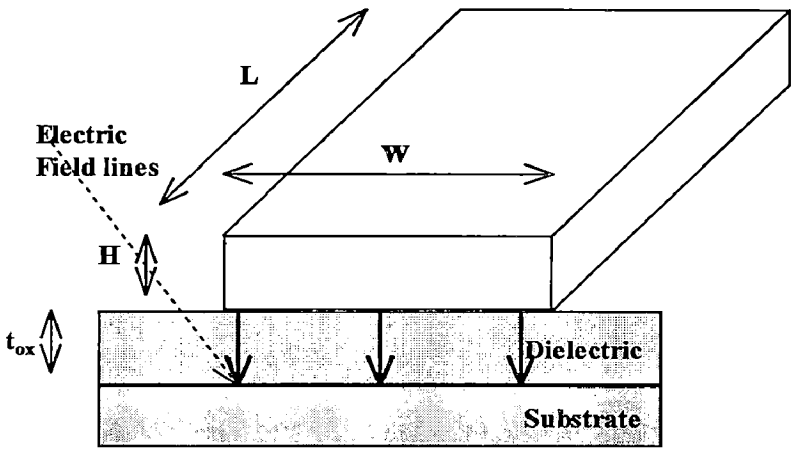

Figure 2.1: Parallel-plate capacitance model of interconnect wire.

and that its capacitance can be modeled by the parallel-plate capacitor. For this, the total capacitance of the wire can be approximated as equation (2.5).

$$C_{\text{int.}} = \frac{\varepsilon_{ox}}{t_{ox}} WL \tag{2.5}$$

where W and L are respectively the width and length of the wire, and t_{ox} and ε_{ox} represent the thickness of the dielectric layer and its permittivity.

The capacitance between the side-walls of the wires and the substrate, called the fringing capacitance, can no longer be ignored and contributes to the overall capacitance. This effect is illustrated in Figure 2.2. So, capacitance per unit length for the single isolated interconnect wire

can be approximated by:

$$C = C_{pp} + C_{fring} = \frac{W\varepsilon_{0x}}{t_{0x}} + \frac{2\pi\varepsilon_{0x}}{\ln(t_{ox}/H)} \tag{2.6}$$

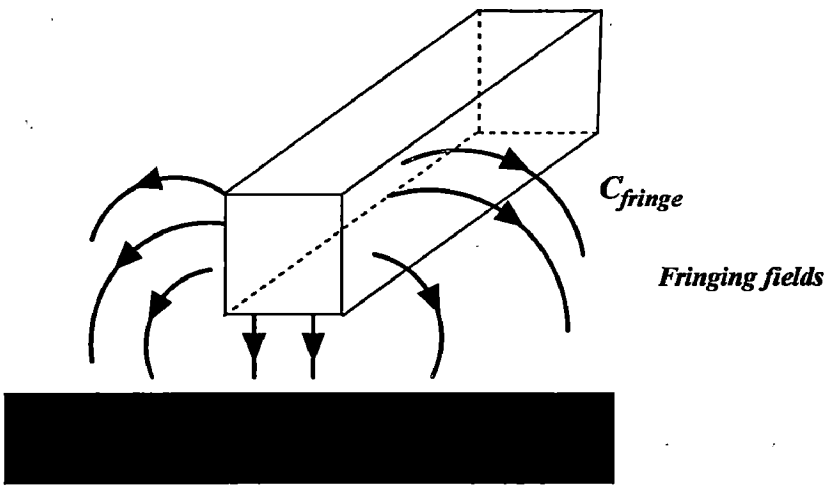

Figure 2.2: Fringing field Capacitance.

where C_{pp} is the "parallel-plate" (bottom area-to-substrate) capacitance, C_{fring} is the fringing (side-wall-to-substrate) capacitance per unit length. This simplification is only useful for estimating rough capacitance values. In reality, a wire is surrounded by a large number of other wires on the same layer and adjacent layers of the multi-level interconnect hierarchies offered in today processes.

2.1.3 Interconnect Inductance

The most basic definition of inductance originates from a fundamental relation between the voltage, V, and the current, I associated with the loop. A voltage drop is created when the current flow through the loop changes:

$$\Delta V = l\frac{dI}{dt} \tag{2.7}$$

In cases when a conductor is completely surrounded by a homogeneous uniform dielectric, the capacitance, C, and inductance, l, per unit length are related by:

$$lC = \varepsilon\mu \tag{2.8}$$

where ε is the dielectric constant and μ is the permeability For lossless lines, inductance can also be calculated from capacitance through Eq. 2.9, which describes the speed, v, at which an electromagnetic wave travels through a medium

$$v = \frac{1}{\sqrt{lC}} = \frac{1}{\sqrt{\mu\varepsilon}} \tag{2.9}$$

2.2 Different approaches for analysis of interconnect performance

In the early days of VLSI design, signal integrity effects include interconnect delay, crosstalk, transmission line effects, substrate coupling, power supply integrity, and noise-on-delay effects were negligible because of relative slow chip speed and low integration density. However, with the introduction of technology generations at about the 0.25μm scale and below, there are many significant changes in wiring and electrical characteristics [6]. Interconnect started to be a dominating factor for chip performance and robustness. In Integrated circuit, the signal on interconnect is routed through CMOS driver. There are three approaches for analysis of CMOS-gate driven interconnects.

One approach focuses on CMOS-gate modeling with the load interconnect approximated by a lumped circuit and gate is modeled using alpha-power law model.

2.2.1 Interconnect Modeling

The circuits parasitic of a wire are distributed along its length and are not lumped into a single position. Yet, when only a single parasitic component is dominant, when the interaction between the components is small, or when looking at only one aspect of the circuit behavior, it is often useful to lump the different fractions into a single circuit element. As long as the resistive component of the wire is small and the switching frequencies are in the low to medium range, it is meaningful to consider only the capacitive component of the wire, and to lump the distributed capacitance into a single capacitor as shown in Figure 2.3.

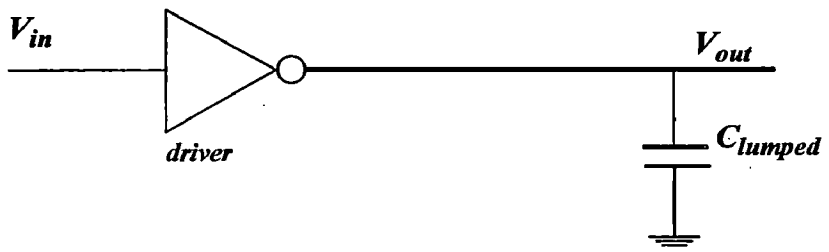

Figure 2.3: Lumped Capacitor model for interconnect.

Delay formulas were developed for CMOS gate driving interconnects line [7], [8]. In which Interconnect is modeled in lumped (C) model and then extended to include the influences of short-circuit current and gate-drain coupling capacitance [9].

On-chip metal wires of over a few millimeter lengths have a significant resistance. The equipotential assumption, presented in the lumped-capacitor model, is no longer adequate, and a resistive-capacitive model has to be adopted. With the resistive component of interconnect becoming comparable to the gate output impedance, modeling of CMOS gate driving resistor-capacitor (*RC*) line was presented in [10]–[12]. A first approach lumps the total wire resistance of each wire segment into one single *R* and similarly combines the global capacitance into a single capacitor *C*. This simple model, called the lumped *RC* model is pessimistic and inaccurate for long interconnect wires, which are more adequately represented by a distributed *RC* model. Now, current operating frequencies are reached in GHz range, which make necessary to include inductance effect in interconnect analysis. Kaushik *et al.* [13] has analyzed CMOS gate driving resistor-inductor-capacitor (*RLC*) line to allow for inductive effect of interconnects.

The second approach performs interconnect analysis by simplifying CMOS driver gate as a resistor. With this linear driver model, the Elmore delay model was first developed for lumped *RC* lines in [14] and then extended for lumped *RLC* lines in [15] and [16]. Crosstalk noise models for lumped *RC* coupled lines were given in [17]–[20]. Bai [20] improved the linear driver model by calculating the effective resistance of victim driver considering the nonlinearity. With the transmission line effect taken into account, Davis proposed a closed-form delay model for a distributed *RLC* line [21] and a crosstalk model for two and three coupled distributed *RLC* lines [22]. Based on even-odd mode propagated in lossless transmission lines, a crosstalk model was proposed for two-coupled lossless lines and then modified for low-loss lines to capture noise peak [23].

The third approach cosimulate nonlinear CMOS gates and distributed interconnects. The analysis of distributed transmission lines in the presence of nonlinear elements suffers from the mixed frequency/time problem, which arises from the fact that transmission lines are described by partial differential equations which are traditionally solved in the frequency domain, whereas the nonlinear elements are described only in the time domain [24].

2.2.2 Alpha-power law MOSFET Model

There is two main discrepancies with Shockley model. One is Saturation voltage is different from the predicted value. The other is that drain current in the saturation region does not show Shockley's square-law dependence on gate-source voltage. These two discrepancies, that is, the shift of drain saturation voltage and discrepancies in the saturation region *I-V* curve, both come from the velocity saturation effects observed in short-channel MOSFET's [25].

So, a new MOSFET's model, namely alpha-power model is proposed to include the velocity saturation effect in short channel MOSFETs. PMOS and NMOS currents are represented by the alpha-power law MOS model in equation (2.10) and (2.11) respectively.

$$i_p = \begin{cases} 0 & V_s \geq V_{dd} - |V_{tp}| \quad (off) \\ K_{lp}(V_{dd} - V_s - |V_{tp}|)^{\alpha_p/2}(V_{dd} - V_1) & V_s < V_{dd} - |V_{tp}| \;\&\; V_1 > V_{dd} - |V_{Dsat_p}| \quad (lin) \\ K_{sp}(V_{dd} - V_s - |V_{tp}|)^{\alpha_p} & V_s < V_{dd} - |V_{tp}| \;\&\; V_1 > V_{dd} - |V_{Dsat_p}| \quad (sat) \end{cases} \tag{2.10}$$

where *lin, sat and off* denote linear, saturation and cut-off regions, respectively. The drain saturation current for PMOS is denoted as

$$V_{Dsat_p} = \frac{K_{sp}}{K_{lp}}(V_{dd} - V_s - |V_{tp}|)^{\alpha_p/2} \tag{2.11}$$

$$i_n = \begin{cases} 0 & V_S \le V_{dd} - |V_{tp}| \quad (off) \\ K_{\ln}(V_S - V_{tn})^{\alpha_n/2}(V_1) & V_S > V_{tn} \,\&\, V_1 < V_{Dsat_n} \quad (lin) \\ K_{sn}(V_S - V_{tn})^{\alpha_n} & V_S > V_{tn} \,\&\, V_1 \ge V_{Dsat_n} \quad (sat) \end{cases} \tag{2.12}$$

The drain saturation current for NMOS and PMOS is denoted as

$$V_{Dsat_n} = \frac{K_{sn}}{K_{\ln}}(V_S - V_{tn})^{\alpha_n/2} \tag{2.13}$$

The parameters of alpha-power law model used are velocity saturation index α, the transconductance parameters K_l and K_s, and threshold voltage V_t. The subscript n and p denote for NMOS and PMOS, respectively.

2.3 Motivation

The main focus of aforementioned research work is towards the functional crosstalk category. But, for complete analysis of crosstalk noise it is necessary to include dynamic crosstalk noise also. A brief discussion of dynamic crosstalk is given by Agarwal *et al.* [23], which is based on decoupling of symmetric coupled line in single one. Furthermore, a dynamic crosstalk noise model based on even-odd mode is also discussed [26], but applicable to lossless (low-loss) coupled lines only that to limited to two lines in number only.

This paper proposes a numerical based FDTD model for accurate analysis of dynamic crosstalk induced glitch and delay in lossy coupled transmission line. This concept can be further extended for multi-transmission lines as well. Non-linear termination in algorithm, lesser numbers of assumptions and accurate accounts of transmission line effects increase the importance of FDTD over other existing methods.

Chapter 3

The FDTD Technique

3.1Introduction

Finite-difference time-domain (FDTD) is a popular computational electrodynamics modeling technique. This firstly implemented to solve Maxwell's equation. The time-dependent partial differentials are discretized using central-difference approximations to the space and time partial derivatives. The resulting finite-difference equations are solved in either software or hardware in a leapfrog manner, firstly implemented by Yee *et al.* [20] for Maxwell's equation solution. In this thesis FDTD is implemented on transmission line equation where relative parameters are line voltage (V) and current (I) like as electrical field (E) and magnetic field (H) in Maxwell's equation.

To implement an FDTD solution of transmission's equations, a computational domain must first be established. The computational domain is simply the physical region over which the model will be performed (here, interconnect modeled into *RLGC* transmission line is computational domain with relative parameter V and I). The V and I fields are determined at every point in space within that computational domain. The Line parasitic such as Resistance (R), Capacitance (C), Conductance (G) and Inductance (L) of each cell within the computational domain must be specified. For coupled line configuration the coupling factors such as coupling capacitance (C_c) and mutual inductance (M) should be added in computational domain.

Once the computational domain is established a source is specified. The source can be linear or non linear voltage source. Current source can be also used. Likewise for computational domain a termination load is also specified, which is almost capacitor in case of on-chip interconnects. After specifying the load and source, the boundary condition is used at the

interference of computational domain and terminals end to matching the FDTD solution for voltage and Current at that time and space point.

3.1.1 Working with FDTD method

When transmission's differential equations are examined, it can be notice that the change in the voltage (V) in time (the time derivative) is dependent on the change in the current (I) across space (the curl). These results in the basic FDTD time-stepping relation that, at any point in space, the updated value of the V in time is dependent on the stored value of the V and the numerical curl of the local distribution of the I in space.

The I is time-stepped in a similar manner. At any point in space, the updated value of I in time is dependent on the stored value of I and the numerical curl of the local distribution of the V in space. Iterating I and V updates results in a explicit marching-in-time process where in sampled-data analogs of the continuous electromagnetic signal under consideration propagate in a numerical grid stored in the computer memory [20].

3.1.2 Strengths of FDTD technique

- FDTD technique used to solve differential equation. It is intuitive, so can easily understand who to use in a model.
- It is a time domain technique. In which response of the system over a wide range of frequencies can be obtained with a single simulation.
- FDTD calculate relative parameter such as E and H in case of Maxwell's equation and V and I in case of transmission line equation, everywhere in the computational domain as they evolve in time. That provides the importance picture of field movement throughout the model. This type of display is useful in understanding what is going on in the model, and to help ensure that the model is working correctly.
- The FDTD technique allows the user to specify the computational domain. A wide variety of linear and nonlinear medium can be naturally and easily modeled.

3.1.3 Stability Criterion for FDTD

The numerical stability of the FDTD method is determined by the Courant-Friedrichs-Lewy (CFL) condition, which simply requires a signal that cannot be allowed to travel more than one space size during one time step. The CFL condition is a necessary condition for convergence while solving certain partial differential equations numerically by the method of finite differences. It arises when explicit time-marching schemes are used for the numerical solution [21].

For stability of the FDTD solution, the position and time discretization must satisfy the Courant condition. Numerically the time and space discretization should follow the following equation.

$$\Delta t \leq \frac{\Delta z}{v} \tag{3.1}$$

where v is signal velocity in line. The Courant stability condition provides that for stability of the solution the time step must be no greater than the propagation time over each cell.

3.1.4 Central difference approximation

Consider a function of one variable $f(t)$. Expanding this in a Taylor series in a neighborhood of a desired point t_0 gives

$$f(t_0+\Delta t)=f(t_0)+\Delta t f^{'}(t_0)+\frac{\Delta t^2}{2!}f^{''}(t_0)+\frac{\Delta t^3}{3!}f^{'''}(t_0) \ \ldots\ldots\ldots\ldots \tag{3.2}$$

where the primes denote the various derivatives with respect tot of the function. Solving this for the first derivative gives

$$f'(t_0)=\frac{f(t_0+\Delta t)-f(t_0)}{\Delta t}-\frac{\Delta t}{2!}f''(t_0)-\frac{\Delta t^2}{3!}f'''(t_0)\ \ldots\ldots\ldots\ldots \tag{3.3}$$

Thus first order derivative can be approximated as

$$f'(t_0)=\frac{f(t_0+\Delta t)-f(t_0)}{\Delta t}+\theta(\Delta t) \tag{3.4}$$

Where $\theta(\Delta t)$ denotes that the error in truncating the series is on the order of Δt .So the first derivative may be approximated with the forward difference

$$f'(t_0)\cong\frac{f(t_0+\Delta t)-f(t_0)}{\Delta t} \tag{3.5}$$

This amounts to approximating the derivative of $f(t)$ as with its region of the desired point. If we expand the Taylor's series as

$$f(t_0-\Delta t)=f(t_0)-\Delta t f'(t_0)+\frac{\Delta t^2}{2!}f''(t_0)-\frac{\Delta t^3}{3!}f'''(t_0)\ \ldots\ldots\ldots\ldots \tag{3.6}$$

which can be approximate by

$$f'(t_0)\cong\frac{f(t_0)-f(t_0-\Delta t)}{\Delta t} \tag{3.7}$$

This gives the backward approximate equation for derivative.

Other approximations known as central differences can be found by subtracting equation (3.3) from equation (3.6) to yield the first derivative central difference approximation

$$f'(t_0) \cong \frac{f(t_0) - f(t_0 - \Delta t)}{\Delta t} \tag{3.8}$$

with a truncation error of Δt^2. Similarly, the second derivative central difference is obtained by adding (2) and (5) to yield

$$f''(t_0) \cong \frac{f(t_0 + \Delta t) - 2f(\Delta t) + f(t_0 - \Delta t)}{\Delta t^2} \tag{3.9}$$

with a truncation error on the order of Δt^2. Due to second order error truncation in central difference approximation, FDTD termed as FDTD solution with second order accuracy.

3.2FDTD MODEL

This section presents the formalization of a finite difference time domain (FDTD) method that is intended for estimation of voltages and currents on interconnects which are modeled as *RLGC* transmission line.

3.2.1 Transmission line's equation

In general, interconnect behaves as a waveguide that can be analyzed using Maxwell's equations. Interconnect can also be analyzed using transmission line equations, if it is assumed that the waves on the line propagate in the transverse electromagnetic (TEM) mode [22]. Interconnect

models based on transmission lines with distributed *RLGC* segments are thus normally used in on-chip interconnect analysis

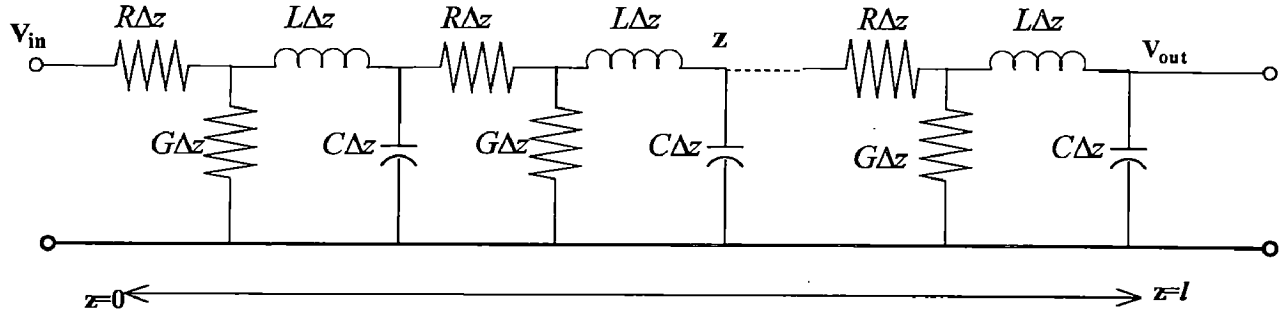

Figure 3.1: distributed *RLGC* transmission line.

Figure 3.1 show the *RLGC* distributed transmission line, where *R, L, G, C* per unit length resistance, inductance, conductance and capacitance of transmission line of length *l*, respectively. Consider the point *z* along the transmission line of Figure 3.1 at time *t*. The following set of equations holds:

$$\frac{d}{dz}V(z,t) = -RI(z,t) - L\frac{d}{dz}I(z,t) \tag{3.10a}$$

$$\frac{d}{dz}I(z,t) = -GV(z,t) - C\frac{d}{dz}V(z,t) \tag{3.10b}$$

3.2.2 Discretization in space and time

To implement FDTD on equation (3.10), first we divide transmission line into *Nz* section, each of length Δz as shown in figure 3.2. Similarly, we divide the total solution time into *Nt* segments of length Δt. Discretization of voltage and current and relation with time and space is shown in figure 3.3. In order to ensure stability of the discretization and to ensure second-order accuracy,

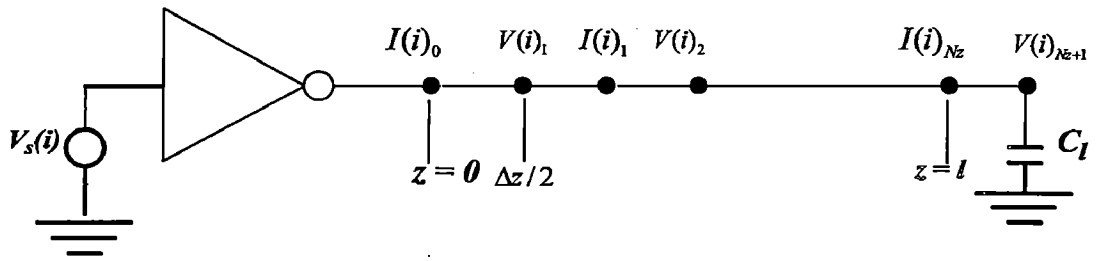

Figure 3.2: Illustration of the discretization of the i th line for the implementation of the FDTD

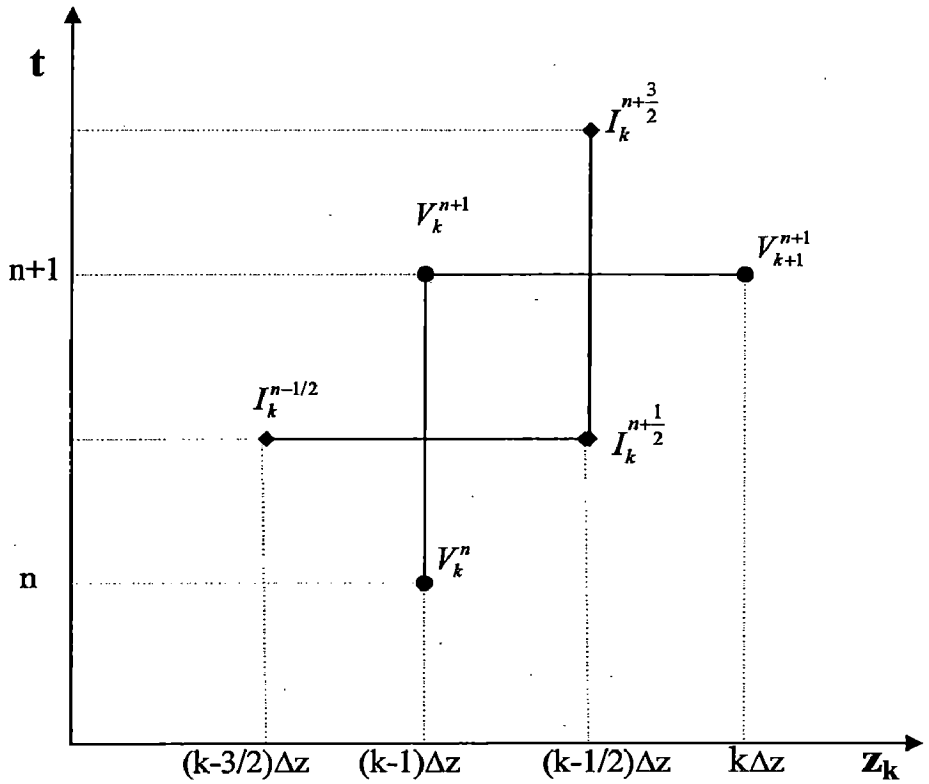

Figure 3.3: Interlacing the current and voltage solutions in space and time for the FDTD analysis.

we interlace the Nz +1 voltage points, V_1, $V2$,..., V_{Nz} and the Nz current points, I_1, I_2,....I_{Nz} . Each voltage and adjacent current solution point is separated by $\Delta z/2$. The time points also be interlaced and each voltage time point and adjacent current time point are separated by $\Delta t/2$, as also shown in figure 3.3. Now using central differential approximation on equation (3.10a)

$$\frac{V_{K+1}^{n+1}-V_K^{n+1}}{\Delta z}+L\frac{I_K^{n+3/2}-I_K^{n+1/2}}{\Delta t}+R\frac{I_K^{n+3/2}+I_K^{n+1/2}}{2}=0 \tag{3.11}$$

for K =1, 2, 3, ..., *Nz* and similarly applying central difference approximation on equation (3.10b) become

$$\frac{I_K^{n+1/2}-I_{K-1}^{n+1/2}}{\Delta z}+C\frac{V_K^{n+1}-V_K^{n}}{\Delta t}+G\frac{V_K^{n+1}+I_K^{n}}{2}=0 \tag{3.12}$$

for K= 2, 3, 4, ..., *Nz*, where we denote voltage and current as

$$V_i^j=V\left[(i-1)\Delta z, j\Delta t\right] \tag{3.13a}$$

$$I_i^j=I\left[(i-1/2)\Delta z, j\Delta t\right] \tag{3.13b}$$

Now by rearranging equation (3.11) and (3.12) the recursive relation of voltage and current at interior point of interconnect can be given as

$$V_k^{n+1}=ABV_k^n+\frac{A}{\Delta z}\left(I_{k-1}^{n+1/2}-I_k^{n+1/2}\right) \tag{3.14}$$

for K =1, 2, 3, ..., *Nz* and

$$I_k^{n+3/2}=EFI_k^{n+1/2}+\frac{E}{\Delta z}\left(V_k^{n+1}-V_{k+1}^{n+1}\right) \tag{3.15}$$

for K= 2, 3, 4, ..., *Nz*

where

$$A=\left(\frac{C}{\Delta t}+\frac{G}{2}\right)^{-1},\quad B=\left(\frac{C}{\Delta t}-\frac{G}{2}\right),\quad E=\left(\frac{L}{\Delta t}+\frac{R}{2}\right)^{-1} \text{ and } F=\left(\frac{L}{\Delta t}-\frac{R}{2}\right) \tag{3.16}$$

Equation (3.14) and (3.15) are recursive relation is used to estimation the voltage and current at different point of line at different time for signal transmission line. This can be extended for multi-transmission line. For N transmission line the Voltage and Current can be can be replaced by vector of order of $1\times N$ as

$$V=[V(1)\,V(2)\,V(3).....V(N)]^T \tag{3.17a}$$

$$I=[I(1)\,I(2)\,I(3).....I(N)]^T \tag{3.17b}$$

where $V(1)$, $V(2)$... are voltage point for line 1 ,2 ...respectively, similarly apply for current points. line parameter such as R, L, G, C and all other derived parameter as A, B, E, F are replaced by $N\times N$ matrix for N transmission line.

3.2.3 Leapfrog time-stepping

As shown in the previous section, Current is updated at $t=(n+1/2)\Delta t$ using the previous current value at $t=(n-1/2)\Delta t$ and voltage at $t=n\Delta t$. Voltage, on the other hand, is updated at $t=(n+1)\Delta t$ using the previous at $t=n\Delta t$ and current at $t=(n+1/2)\Delta t$. Figure 3.4 shows timeline when I and V are updated.

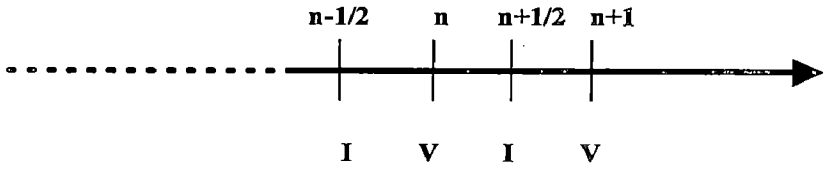

Figure 3.4: Timeline showing when E and H fields are updated.

To remain numerically stable, the time-step must obey the Courant Stability Condition

$$\Delta t < \frac{1}{C\Delta z} \tag{3.18}$$

To obtain good spatial resolution, the cell size should be less than a tenth of the shortest wavelength [24]

$$\Delta z < \frac{\lambda_{\min}}{10} \tag{3.19}$$

3.2.4 Incorporation of boundary condition

This section considers incorporation of terminal condition with FDTD solution. The essential problem in incorporating the terminal conditions is that the FDTD voltages and currents at each end of the line, V_1, I_1, and V_{Nz+1}, I_{Nz} are not collocated in space or time, whereas the terminal conditions relate the voltage and current at the same position and at the same time [23]. This section can be divided into two parts such as (1) boundary matching at source and line interface and (2) boundary matching at load and line interference.

3.2.4.1 Boundary matching at source end

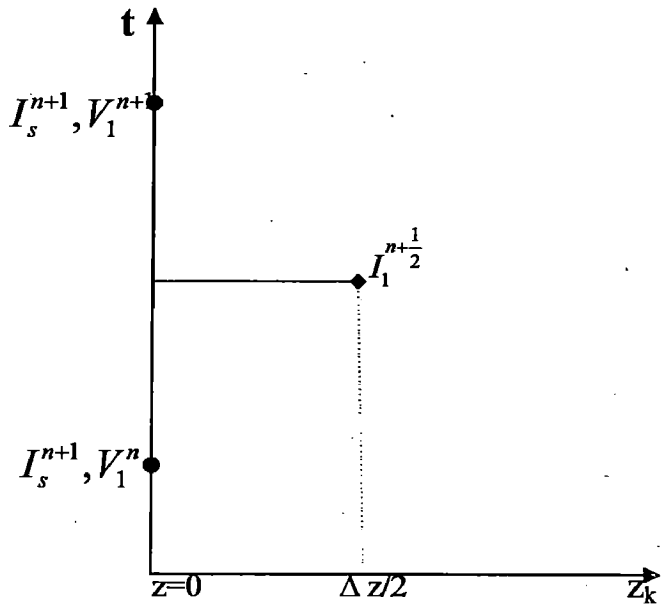

Figure 3.5: Discretizing the terminal voltages and currents of the line at source end in order to incorporate the terminal constraints.

Let the source current is I_S at source terminal ($z=0$) as shown in figure 3.6. To match the source current at boundary Equation (3.14) is discretized at the source by averaging the source currents I_S to obtain a value that is located in time at the same time point at $I_0^{n+1/2}$ as,

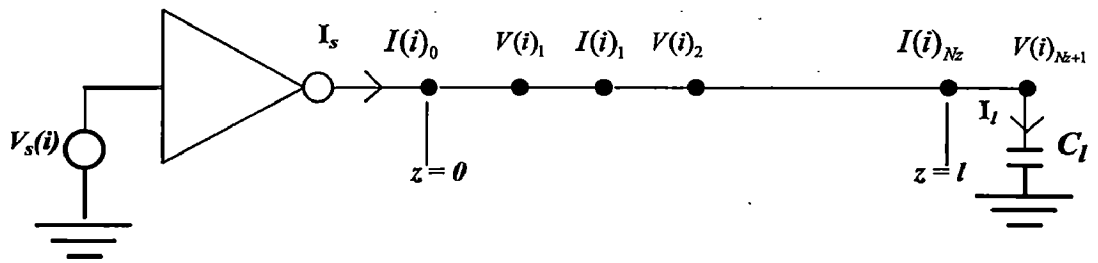

Figure3.6: Discretizing of line with source and load current.

$$I_0^{n+1/2} = \frac{I_s^{n+1} + I_s^n}{2} \tag{3.20}$$

Now using equation (3.14) and (3.20), recursive relation for voltage and current at source and line interference can be given as

$$\frac{1}{\Delta z/2}\left[I_1^{n+1/2} - \frac{I_s^{n+1} + I_s^n}{2}\right] + \frac{1}{\Delta t} C\left[V_1^{n+1} - V_1^n\right] + \frac{G}{2}\left[V_1^{n+1} + V_1^n\right] = 0 \tag{3.21}$$

3.2.4.2 Boundary matching at load end

The load current at load terminal is shown in figure 3.6. Similarly, the transmission-line equation (3.14), is discretized at the load by averaging the load currents I_l in order to obtain a value that is located in time at the same point as $I_{Nz}^{n+1/2}$ as

$$I_{Nz+1}^{n+1} = \frac{I_l^{n+1} + I_l^n}{2} \tag{3.22}$$

Now using equation (3.14) and (3.22), recursive relation between voltage and current at load end and line interference can be written as

$$\frac{1}{\Delta z/2}\left[\frac{I_l^{n+1} + I_l^n}{2} - I_{Nz}^{n+1/2}\right] + \frac{1}{\Delta t} C\left[V_{Nz+1}^{n+1} - V_{Nz+1}^n\right] + \frac{G}{2}\left[V_{Nz+1}^{n+1} + V_{Nz+1}^n\right] = 0 \tag{3.23}$$

First, the voltages along the line are obtained, for a fixed time, from equation (3.14) in terms of

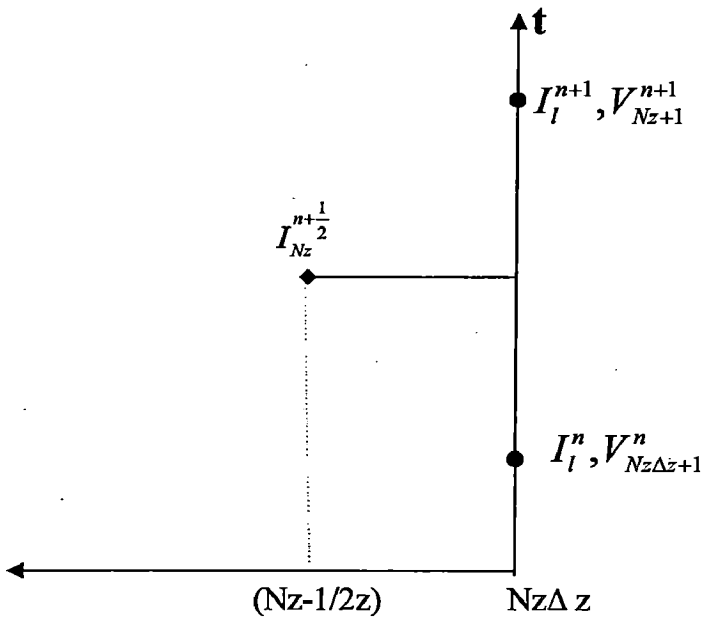

Figure 3.7: Discretizing the terminal voltages and currents of the line at load end in order to incorporate the terminal constraints.

the previous solutions. Then the currents are obtained from (3.15) in terms of the voltages as well as previously obtained current values.

3.3 FDTD Model for Interconnect terminated by Resistive load

Let interconnect is terminated by resistor at load end. Now using figure 3.8 the relation between load current I_l and load voltage V_l (zero in mostly cases, where line is terminated by ground resistive load) can be given as

$$V_{Nz+1} = V_l + I_l R_l \tag{3.24}$$

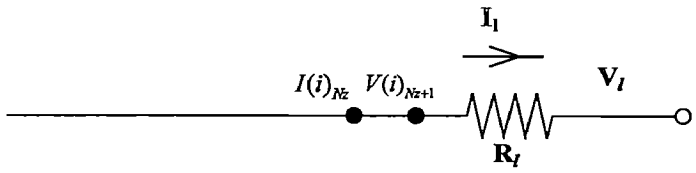

Figure 3.8: Interconnect terminated by Resistance.

Discretizing this into time domain simply gives

$$V_{Nz+1}^{n+1} = V_l^{n+1} + I_l^{n+1} R_l \tag{3.25}$$

On rearranging equation (3.25)

$$I_l^{n+1} = \frac{V_{Nz+1}^{n+1} - V_l^{n+1}}{R_l} \tag{3.26}$$

Now using equation (3.26) and relation derived in equation (3.23), recursive relation for voltage at resistive load can be given as

$$V_{Nz+1}^{n+1} = K_1 K_2 V_{Nz}^{n} + \frac{2A}{\Delta z}\left[I_{Nz}^{n+1/2} + \frac{V_l^{n} - V_l^{n+1}}{R_l} \right] \tag{3.27}$$

where

$$K_1 = \left[1 + 2A/\Delta z\right]^{-1} \text{ and } \quad K_2 = \left[AB - 2A/\Delta z\right] \tag{3.28}$$

3.4 FDTD Model for Interconnect terminated by capacitive load

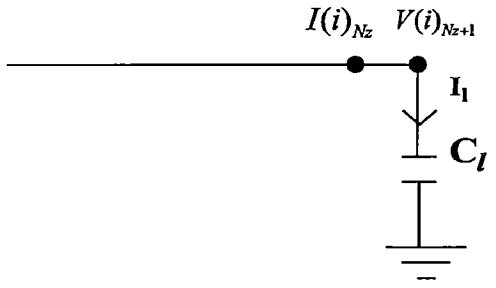

Figure 3.9: Interconnect terminated by capacitive load

Let the second case in which interconnect is terminated by capacitor at load end. Again using figure 3.9 the relation between load current I_l and load voltage V_{Nz+1} can be given as

$$I_l = C_l \frac{d}{dt} V_{Nz+1} \tag{3.29}$$

Discretizing the equation (3.29) in time domain

$$I_l^{n+1} = C_l \frac{\left(V_{Nz+1}^{n+1} - V_{Nz+1}^{n} \right)}{\Delta t} \tag{3.30}$$

Now, using equation (3.30) and (3.23), the interface equation for voltage at capacitive load end is given by

$$V_{Nz+1}^{n+1} = K_1 K_2 V_{Nz}^{n} + \frac{2A}{\Delta z} \left[I_{Nz}^{n+1/2} \right] \tag{3.31}$$

where

$$K_1 = [1 + 2AC_l / \Delta t \Delta z]^{-1} \text{ and } K_2 = [AB - 2AC_l / \Delta t \Delta z] \tag{3.32}$$

3.5 FDTD Model for Interconnect driven by Resistive driver

CMOS driver is usually represented by a linear circuit which uses the equivalent PMOS resistance for falling ramp input or the equivalent NMOS resistance for rising ramp input. In CMOS-gate driven interconnect, for simplification CMOS driver is replaced by its equivalent on resistance in series with power supply. The equivalent MOS resistance R_{eq} can be approximated by just averaging the values of the resistance at the midpoint (where MOS transistor is in saturation state) during switching, which is in the form of [24].

$$R_{eq} = \frac{3}{4}\frac{V_{dd}}{I_{sat}}\left(1 - \frac{7}{9}\lambda V_{dd}\right) \tag{3.33}$$

where V_{dd} is power supply voltage, I_{Sat} is the drain saturation current, and λ is channel-length modulation. In this section the CMOS driver is modeled into linear resistor in series with voltage source. The CMOS driver is replaced by equivalent thevnin resistance (R_{eq}).

The termination circuit as shown in figure 3.10, at the source end of interconnect line consists of a resistor and voltage source connected in such a way that can be described by following relation

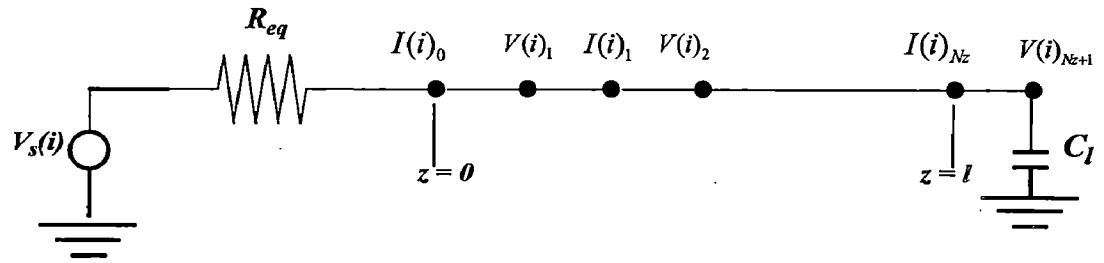

Figure 3.10: Interconnect driven by Resistive driver

$$I_S = \frac{V_1 - V_S}{R_{eq}} \tag{3.34}$$

On rearranging (3.34)

$$V_1 = V_S - I_S R_{eq} \tag{3.35}$$

To implemented FDTD equation (3.35) should be discretized in time domain as

$$V_1^{n+1} = V_S^{n+1} - I_S^{n+1} R_{eq} \tag{3.36}$$

Using equation (3.21) and (3.36) recursion relations at source interface for V_1 can be given as

$$V_1^{n+1} = K_1 K_2 V_1^n + K_1 K_3 (V_s^n + V_s^{n+1}) - 2K_1 K_3 R_{eq} I_1^{n+1/2} \tag{3.37}$$

and $K_1 = \left(U + K_3\right)^{-1}$, $K_2 = \left(AB - K_3\right)$ and $K_3 = A/\Delta z R_S$ (3.38)

3.6 FDTD Model for coupled transmission line

In this section, two distributed coupled *RLC* lines are considered. Let *R, L* and *C* be per unit length line resistance, self-inductance, and ground capacitance of the line, respectively. Subscription 1 and 2 is used for line 1 and line 2, respectively. C_c and M represent the coupling capacitance per unit length and mutual inductance per unit length between the lines. At any point z along the line, voltage and current waveforms on line 1 and line 2 satisfy the following set of differential equations,

$$\frac{\partial}{\partial z}V_1(z,t)+L_1\frac{\partial}{\partial t}I_1(z,t)+M\frac{\partial}{\partial t}I_2(z,t)+R_1I_1(z,t)=0 \tag{3.39a}$$

$$\frac{\partial}{\partial z}V_2(z,t)+L_2\frac{\partial}{\partial t}I_2(z,t)+M\frac{\partial}{\partial t}I_1(z,t)+R_2I_2(z,t)=0 \tag{3.39b}$$

$$\frac{\partial}{\partial z}I_1(z,t)+(C_1+C_c)\frac{\partial}{\partial t}V_1(z,t)-C_c\frac{\partial}{\partial t}V_2(z,t)+G_1V_1(z,t)=0 \tag{3.39c}$$

$$\frac{\partial}{\partial z}I_2(z,t)+(C_2+C_c)\frac{\partial}{\partial t}V_2(z,t)-C_c\frac{\partial}{\partial t}V_1(z,t)+G_2V_2(z,t)=0 \tag{3.39d}$$

which can be written in matrix form as,

$$\frac{\partial}{\partial z}V(z,t)+L\frac{\partial}{\partial t}I(z,t)+RI(z,t)=0 \tag{3.40a}$$

$$\frac{\partial}{\partial z}I(z,t)+C\frac{\partial}{\partial t}V(z,t)+GV(z,t)=0 \tag{3.40b}$$

where I and V are in 2×1 matrix form and R,L,G,C are in 2×2 matrix form given as

$$R=\begin{pmatrix} R_1 & 0 \\ 0 & R_2 \end{pmatrix},\quad L=\begin{pmatrix} L_1 & M \\ M & L_2 \end{pmatrix},\quad G=\begin{pmatrix} G_1 & 0 \\ 0 & G_2 \end{pmatrix},\quad \text{and}$$

$$C=\begin{pmatrix} C_1+C_c & -C_c \\ -C_c & C_1+C_c \end{pmatrix} \tag{3.41}$$

for N number of coupled transmission lines, I and V are converted into $N\times 1$ matrix and R, L, G, C are in $N\times N$ matrix. Now equation (3.40) can be solved similarly as the equation (3.14). All previous recursive relation derived for interconnect is applicable for coupled line just changing the parameter matrix.

3.7 FDTD Model for CMOS-gate driven Interconnect

In chapter 3, CMOS driver is simplified as a linear circuit in which a constant resistance is used to approximate the nonlinear and time-varying MOS resistance. FDTD is implemented for linear behavior of driver in that section, whereas this chapter presents a FDTD method for transient analysis of lossy transmission lines in the presence of the nonlinear behavior of CMOS gates.

Signal integrity is strongly affected by both the transmission line behavior of interconnects and the nonlinear behavior of CMOS drivers. Therefore, accurate prediction of time delay and crosstalk noise should combine the effect of transmission line that propagates quasi TEM with precise transistor level modeling of CMOS-gate [24]. The nonlinear behavior of CMOS gates is represented by alpha-power law model [31], with the drain current described by piecewise linear function of the drain voltage and discretized in time domain for the FDTD implementation.

Figure 3.11 shows M coupled transmission lines driven by CMOS gates. The input signal is $N\times$ 1 vector of voltage, denoted as $V_S=\left[V_S(1)\,V_S(2)\,V_S(3).....V_S(N)\right]^{-1}$. The alpha power-law

model [31] is used for modeling the CMOS gates. A detail of alpha power model is given in section 2.3. Figure 3.12 shows the macro model used for FDTD implement.

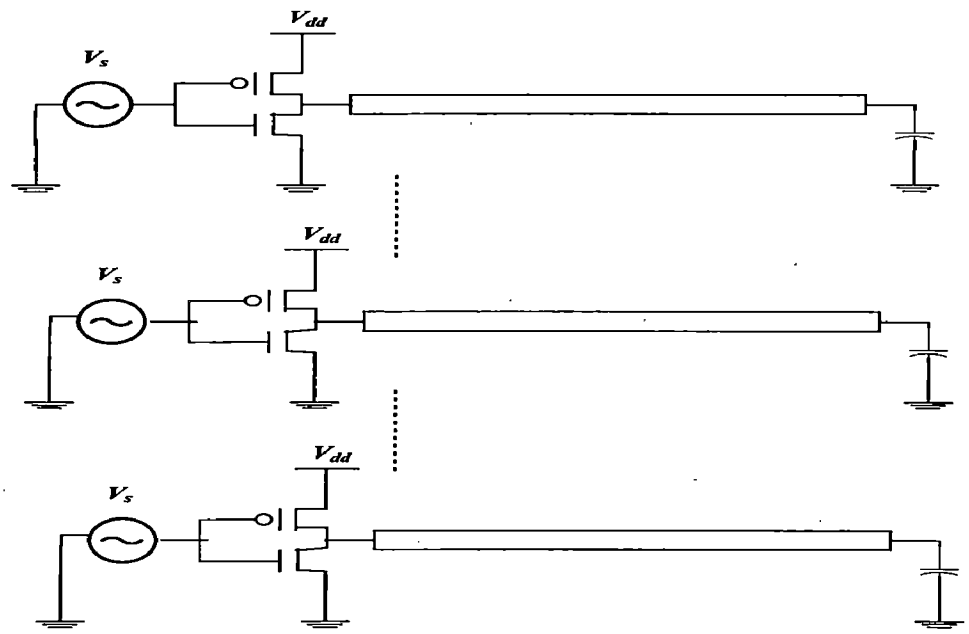

Figure 3.11: *M* coupled transmission lines driven by CMOS gates.

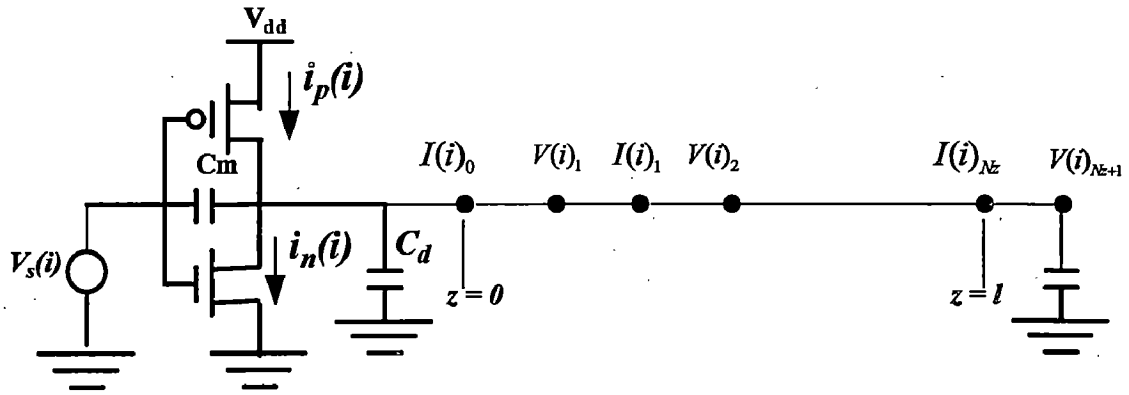

Figure 3.12: Macro model for CMOS-gate driven interconnect.

PMOS and NMOS currents are represented by the alpha-power law MOS model and discretized in time domain, shown in (2) and (3), respectively.

$$i_p^{n+1} = \begin{cases} 0 & V_s^{n+1} \geq V_{dd} - |V_{tp}| \\ K_{lp}(V_{dd} - V_s^{n+1} - |V_{tp}|)^{\alpha_p/2}(V_{dd} - V_1^n) & V_s^{n+1} < V_{dd} - |V_{tp}| \;\&\; V_1^n > V_{dd} - |V_{Dsat_p}^n| \\ K_{sp}(V_{dd} - V_s^{n+1} - |V_{tp}|)^{\alpha_p} & V_s^{n+1} < V_{dd} - |V_{tp}| \;\&\; V_1^n > V_{dd} - |V_{Dsat_p}^n| \end{cases} \tag{3.42}$$

$$i_n^{n+1} = \begin{cases} 0 & V_s^{n+1} \leq V_{dd} - |V_{tp}| \\ K_{\ln}(V_s^{n+1} - V_{tn})^{\alpha_n/2}(V_1^n) & V_s^{n+1} > V_{tn} \;\&\; V_1^n < V_{Dsat_n}^n \\ K_{sn}(V_s^{n+1} - V_{tn})^{\alpha_n} & V_s^{n+1} > V_{tn} \;\&\; V_1^n \geq V_{Dsat_n}^n \end{cases} \tag{3.43}$$

where discretized saturation current is represented as

$$V_{Dsat_p}^n = \frac{K_{sp}}{K_{lp}}(V_{dd} - V_s^n - |V_{tp}|)^{\alpha_p/2} \tag{3.44}$$

$$V_{Dsat_n}^n = \frac{K_{sn}}{K_{\ln}}(V_s^n - V_{tn})^{\alpha_n/2} \tag{3.45}$$

Applying KCL at source and interconnect interface according to figure 3.12, results in

$$I_S = C_m\left[\frac{d(V_S - V_1)}{dx}\right] + i_p - i_n - C_d\frac{dV_1}{dx} \tag{3.46}$$

where C_m and C_d are drain to coupling capacitance and the drain diffusion capacitance of CMOS driver.

Source Current I_s, in discretized form can be written as

$$I_S^{n+1} = C_m\frac{V_S^{n+1} - V_S^n}{\Delta t} + i_p^{n+1} - i_n^{n+1} - (C_m + C_d)(\frac{V_1^{n+1} - V_1^n}{\Delta t}) \tag{3.47}$$

Now solving equation (3.47) and (3.23) the recursive relation for voltage at CMOS-gate and interconnect interface can be given as

$$V_1^{n+1} = K_1 V_1^n - K_2 I_1^{n+1/2} + \frac{K_2}{2}\left[i_p^{n+1} - i_n^{n+1}\right] + K_3 \tag{3.48}$$

where

$$K_1 = \left[\Delta z\Delta t U + A(C_m + C_l)\right]^{-1}\left[\Delta z\Delta t AB + A(C_m + C_l)\right]$$

$$K_2 = 2A\Delta t\left[\Delta z\Delta t U + A(C_m + C_l)\right]^{-1},\ K_3 = \frac{K_2}{2}\left[I_S^n + \frac{C_m}{\Delta t}(V_S^{n+1} - V_S^n)\right] \tag{3.49}$$

Chapter 4

Analysis of Interconnect Performance

As discussed in earlier chapter, interconnects are used for distributing clock-signals, power supply and connecting signals among integrated circuits. In other manner, we can say that interconnects are medium in IC for propagation of signals from one device to other connect device. So, interconnect perform well, if the propagating signal at far end of interconnect reach at desired time and desired waveform shape.

However, after introduces of sub micron device technology a significant change is noticed in interconnect performance. Typical time-domain effects include interconnect delay, crosstalk, transmission line effects, noise-on-delay effects highly degraded the performance of interconnects. This chapter presents a detail time-domain analysis based on FDTD model developed in last chapter for coupled interconnect configuration.

4.1 Crosstalk Noise

Aggressive usage of high-speed circuit families, scaling of power supply and threshold voltages, and mixed-signal integration combine to make the chips more noise-sensitive. Crosstalk noise in IC is results of coupling effects between interconnect line. Noise, cause by one signal, being coupled into a different signal is called crosstalk. Crosstalk noise can affect the circuit performance in two ways, either by disturbing a quiet line, or by changing the response speed of adjacent switching line.

4.1.1 Functional Crosstalk

The current is injected into quiet line (victim) during the switching of adjacent line (aggressor) is defined as functional crosstalk. Or, an undesirable voltage spike generated at quiet line (victim) during the switching of adjacent line is defined as functional crosstalk. This type of crosstalk noise can cause device or logic failure due to unexpected.

A simple set-up for functional-crosstalk analysis is presented here. Figure 4.1 shows the experimental set-up for coupled interconnect configuration driven by resistive driver. One of the lines is identified as aggressor and the other as victim. The driver of aggressor line is excited by a rising ramp source of V_s = 1.2V with 50ps transient time, in series with a linear resistance R_s=75Ω. On the other hand, the driver of victim line is grounded through a linear resistance R_v=50 Ω.

Coupled interconnect wire of 2mm length is considered for crosstalk analysis. The interconnect wire has parameters such as ground capacitance (C) = 257fF, self-inductance (L) = 2.15nH, coupling capacitance (C_c) = 184fF and mutual- inductance (M) = 1.68nH. Interconnect is terminated by a load capacitance (C_l) of 30fF.

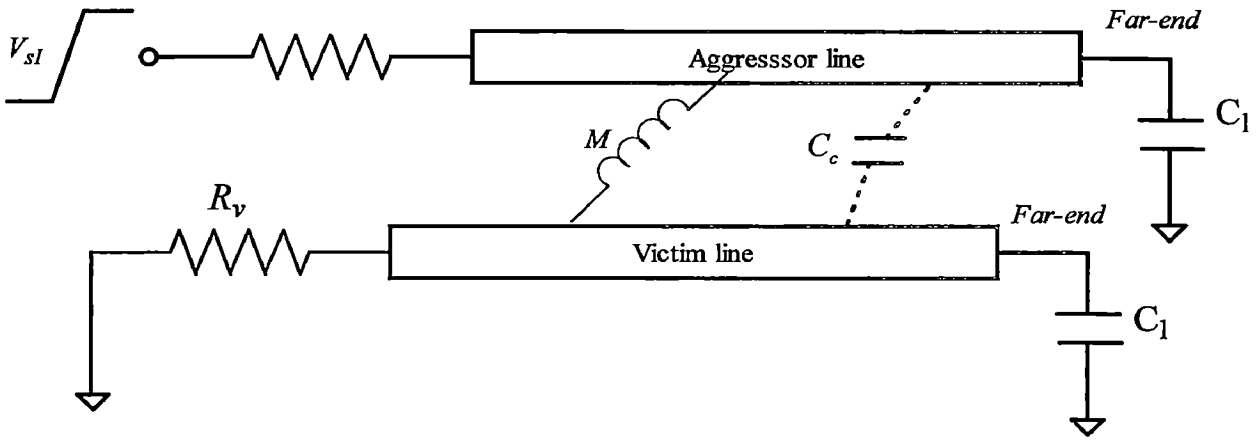

Figure 4.1: Coupled *RLGC* interconnect configuration for functional crosstalk.

The response of victim line at far-end is shown in Figure 4.2. An aggressor line switching, results in a voltage spike of 0.234 V at far end of victim-lime. If a device connected at far end of victim has threshold voltage in this range, a logical failure or false switching of gate may occurs.

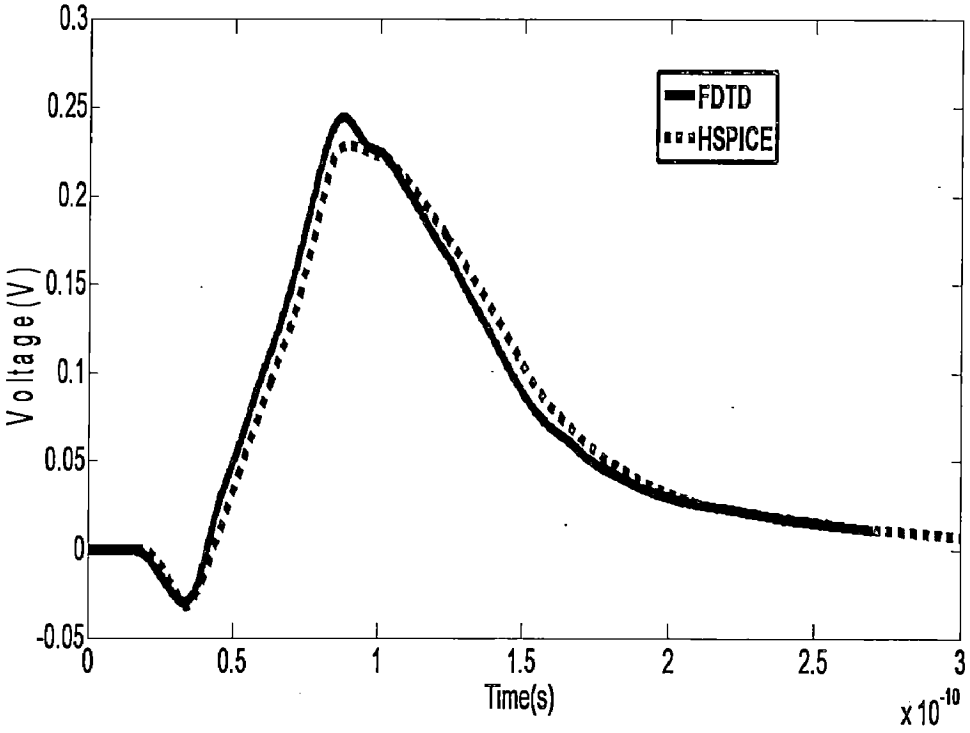

Figure 4.3: Comparison of SPICE and FDTD generated waveforms at far-end of victim line.

4.1.2 Dynamic Crosstalk

Dynamic crosstalk appears due to the simultaneous switching at adjacent lines either in same phase or in opposite phase. This noise impacts the critical issue of timing by changing the response time of adjacent signal.

Analyzing the dynamic crosstalk noise case is equally important as modeling of functional crosstalk noise, particularly since CMOS logic gates tend to have very good functional-noise rejection capabilities, so dynamic case is essential for complete analysis of on-ship performance.

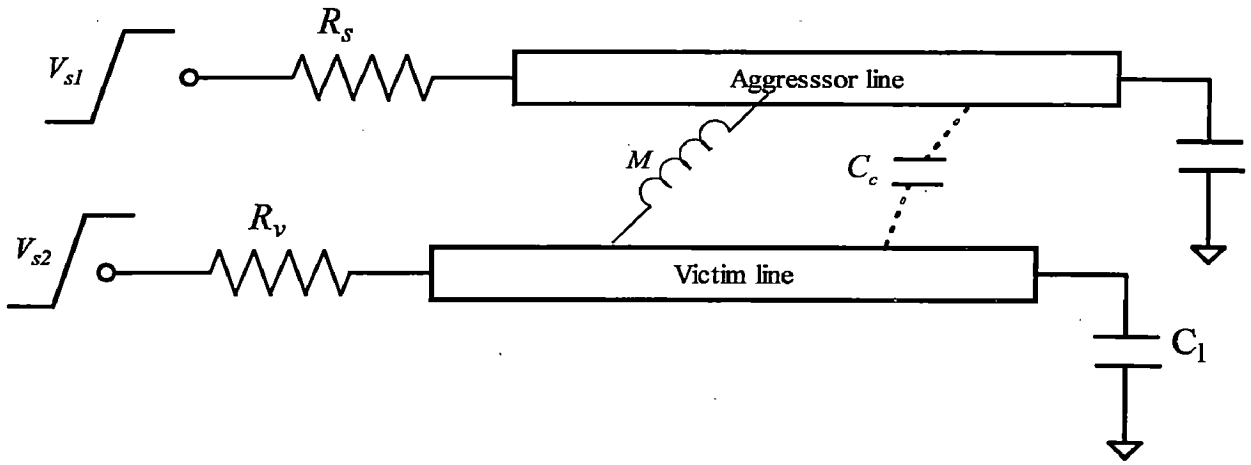

Figure 4.3: Coupled line configurations for dynamic crosstalk analysis (in-phase switching).

Using Set-up shown in figure 4.3, dynamic crosstalk is analyzed, when both aggressor and victim lines are simultaneously switched in same phase by rising ramp signal (0-V_s) with 50ps

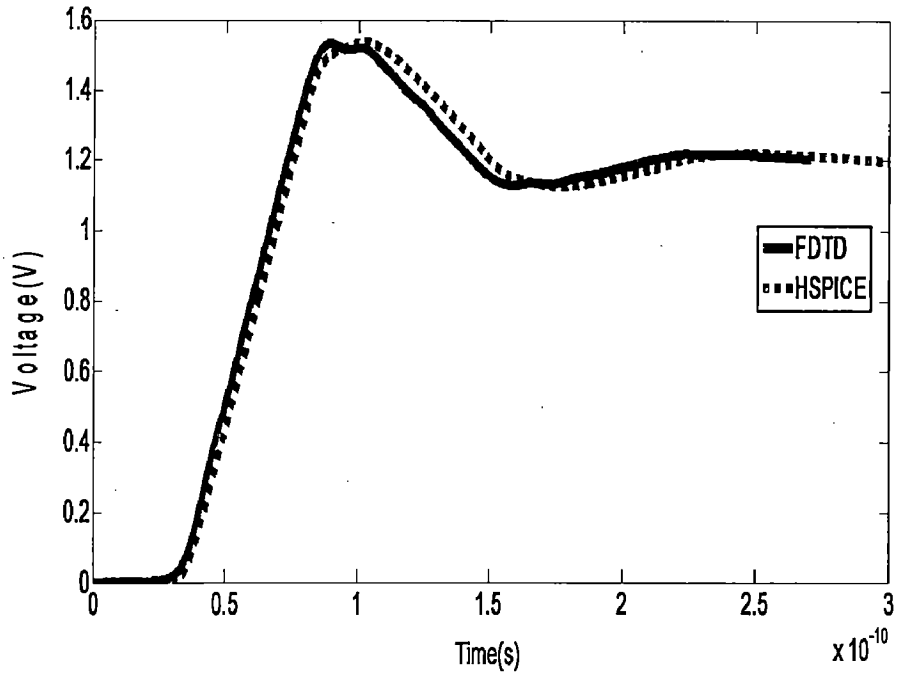

Figure 4.4: Comparison of SPICE and FDTD generated waveforms at far-end of victim line for under in-phase switching.

transition time. Time domain response is shown in Fig. 4.4. The positive peak at far end of victim line reached up to 1.57V for 1.2V input ramp signal.

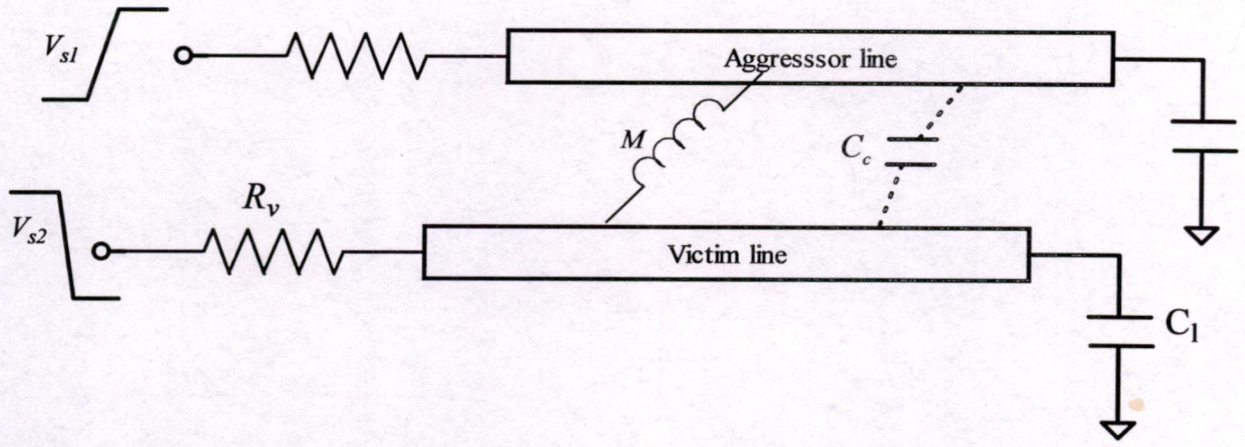

Figure 4.5: Coupled line configurations for dynamic crosstalk analysis (Out-of-phase switching).

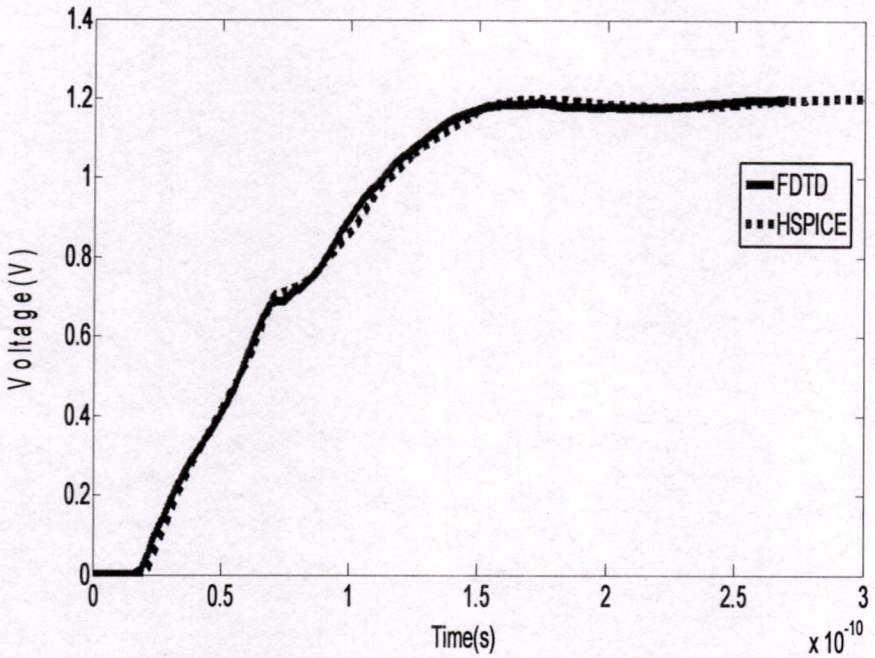

Figure 4.6: Comparison of SPICE and FDTD generated waveforms at far-end of aggressor line under out-of–phase switching.

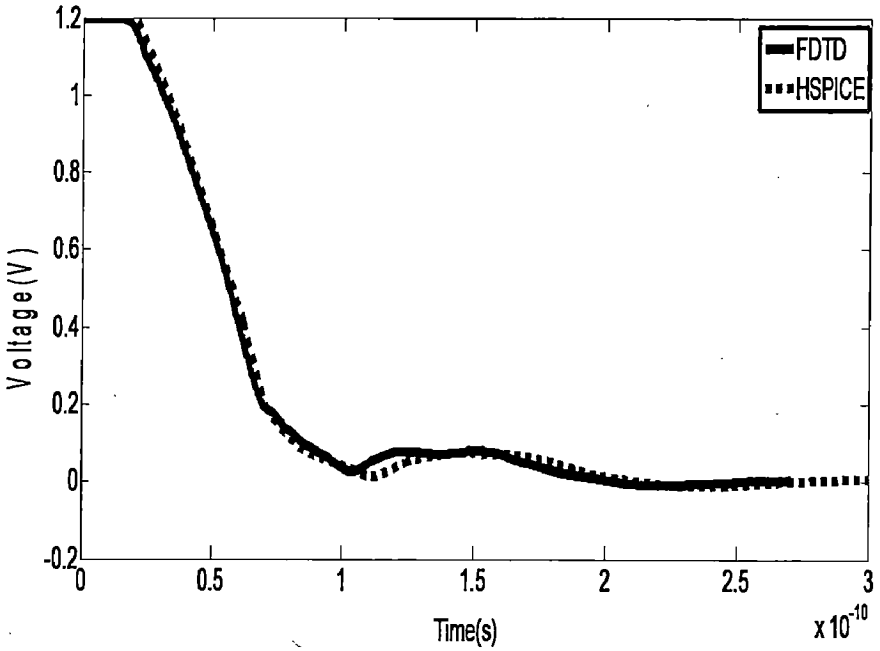

Figure 4.7: Comparison of SPICE and FDTD generated waveforms at far-end of victim line under out-of-phase switching.

In second case of dynamic crosstalk interconnects lines is excited in out-of-phase as shown in figure 4.5. A rising-ramp signal is applied at aggressor line where falling–ramp is used for victim line. The time domain response at far end of both lines is shown in Figure 4.6 and figure 4.7, respectively.

4.2 Crosstalk-induce delay

As discuses earlier, dynamic crosstalk highly influence the timing issue of signal. The change is response time of a signal due to switching in adjacent line is known as crosstalk-induce delay.

The delay of interconnect line is reduces, when adjacent line is switching in same case. It can be easily understand using couple transmission line theory, that when both line switching in same direction the effecting coupling capacitance between lines is reduces. That's way delay is also reduced. Similarly, in other case the delay is increase when adjacent line is switched in out-of-phase, because in this case effect coupling capacitance is doubled.

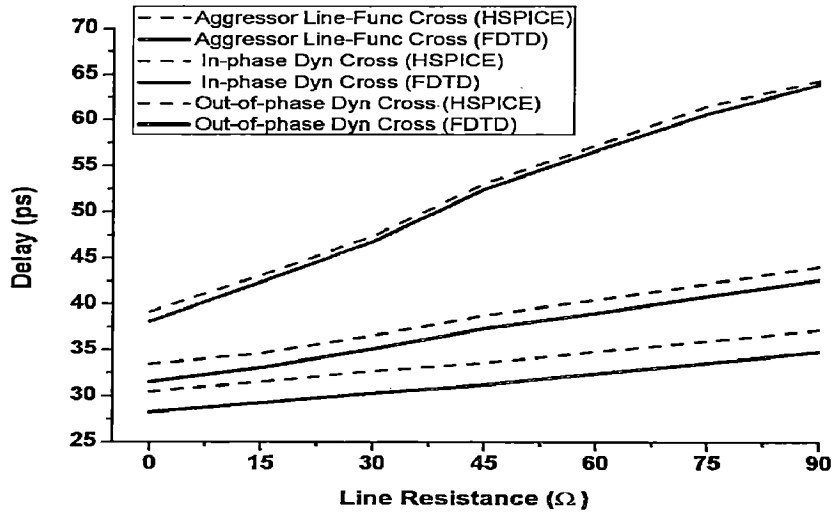

Figure 4.8: 50% Propagation delay variation with line resistance.

4.3 Effect of Line Resistance Variation

Fig. 4.8 presents the variation of 50% propagation delay with line resistance for three cases *viz.* (i) Aggressor line under functional crosstalk scenario (*Aggressor Line-Func Cross*) (ii) In-phase dynamic crosstalk scenario (*In-phase Dyn Cross*); (iii) Out-of-phase dynamic crosstalk scenario (*Out-of-phase Dyn Cross*). It has been observed that the delay reduces for in-phase case, while, it increases for out-of-phase switching scenario. However, as the line resistance increases, the propagation delay for all three cases increases due to increase in RC delay of line.

4.4 Effect of interconnect length Variation

A similar functional crosstalk analysis set-up is used. Interconnect length is vary from 1mm to 4mm. In all case line parasitic is calculated, and FDTD model is implemented for output response. Figure 4.9 shows the variation in noise peak at far-end of victim line with

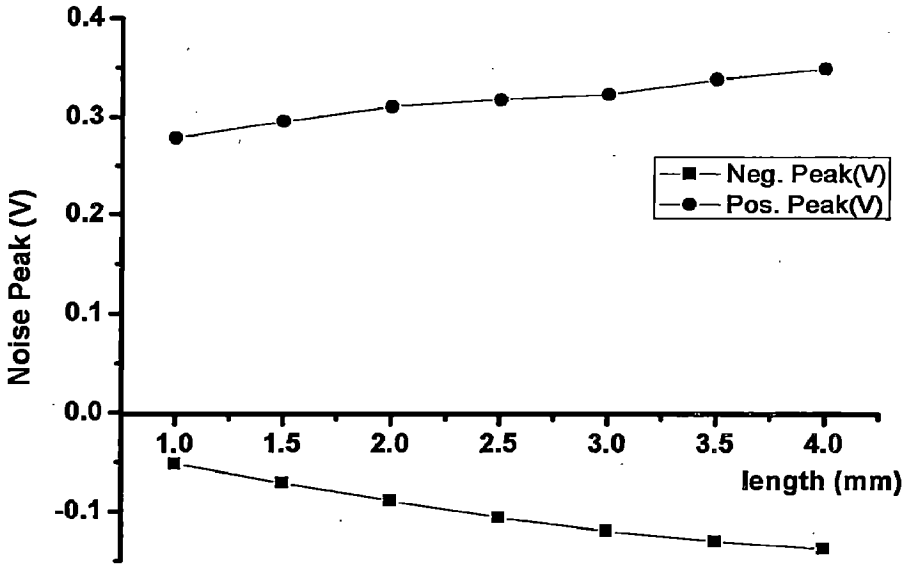

Figure 4.9: Noise Peak variation with interconnect length.

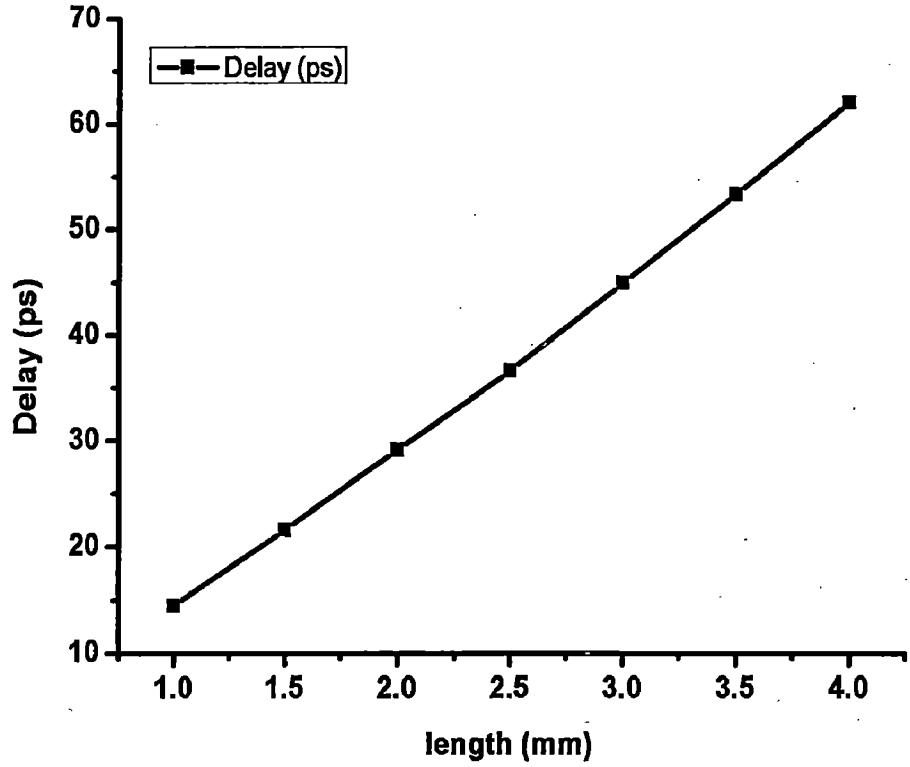

Figure 4.10: 50% delay variation with interconnect length.

interconnect length. Where figure 4.10 show the delay variation at aggressor line end with respect to interconnect length. According to figure 4.10, increment in delay is linearly vary with interconnect line.

TABLE 4.1

DELAY ANALYSIS OF FUNCTIONAL AND DYNAMIC CROSSTALK WITH VARIATION IN LINE RESISTANCE

Line Resistance (Ω)	Propagation Delay in 2mm Long Interconnect								
	Dynamic Crosstalk Delay						*Functional Crosstalk (Aggressor Line Delay)*		
	In- Phase			*Out-of-Phase*					
	FDTD (ps)	*HSPICE (ps)*	*Error (%)*	*FDTD (ps)*	*HSPICE (ps)*	*Error (%)*	*FDTD (ps)*	*HSPICE (ps)*	*Error (%)*
0	28.20	30.49	7.5	38.10	39.16	2.7	31.50	33.46	5.8
15	29.25	31.53	7.3	42.40	43.10	1.6	33.10	34.67	4.5
30	30.30	32.72	7.3	46.80	47.37	1.2	35.10	36.58	4.0
45	31.20	33.59	7.1	52.50	53.13	1.1	37.30	38.76	3.7
60	32.40	34.78	6.8	56.70	57.25	0.9	39.00	40.45	3.5
75	33.60	35.97	6.6	60.70	61.19	0.8	40.80	42.19	3.3
90	34.80	37.16	6.3	63.90	64.35	0.7	42.60	44.04	3.2

4.5 HSPICE Simulation

The HSPICE simulation used W element model to represent a transmission line. RLGC parameter matrix is external define for W-element model. For all above discusses cases the HSPICE simulation result is also obtain for same RLGC matrix.

For self motivation and to verify the analytically result based on FDTD model, comparison with HSPICE is also made. In almost cases, the FDTD based waveforms closely matches with HSPICE waveforms, which validates the accuracy of proposed method.

Table 4.1 compares propagation delay between proposed FDTD model and HSPICE simulation results. Propagation delay is presented for line resistance varying from 0 to 90Ω. It has been observed that the percentage error reduces with increasing line resistance. For the proposed model an average error of 4.1% with respect to HSPICE results is observed. The comparisons of FDTD results with HSPICE demonstrates that the proposed method captures waveform shapes, peak timing and 50% propagation delay with high accuracy for both functional and dynamic crosstalk scenarios. As compared to HSPICE, the analytical model results in an error that ranges from 0.7% to 7.5% only.

Therefore, it can be concluded that the analytical results for proposed FDTD model is in close agreement with HSPICE results.

Chapter 5

Conclusion and Future Scope

5.1 Conclusion

In this dissertation, a set of general finite-difference time-domain updating equations is derived for interconnect analysis. The accuracy of FDTD is improved by using appropriate discretization in space and time point. All analyses were carried out on practical problems and they are supported with simulation results. The measurement results were in good agreement with simulation results, thus leading to the conclusion that all stipulated theories are accurate.

5.2 Future Scope

All the objectives aimed for are achieved at the end of the project. However, there is future work to be continued more on this direction. Following are the potential areas where future work can be extended:

- The effect of crosstalk and crosstalk induce delay is estimate for two coupled line interconnect. It can be extended for more number of lines.

- Although the FDTD method is widely used in the field of computational electromagnetic, the long computational time and large memory requirement have always been a concern with the technique. A deep research can be done in this area.

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List of Publication

[1] Shailesh Mittal, B. K. Kaushik, K. L. Yadav, Manoj Kumar Majumder, "Dynamic Crosstalk Analysis in RLC Modeled Interconnects using FDTD Method," submitted to IEEE International Conference on Computer and Communication Technology (ICCCT), 23-25 Nov. 2012, MNNIT Allahabad. (Review result awaited)

[2] Shailesh Mittal, B. K. Kaushik, K. L. Yadav, Manoj Kumar Majumder," Analysis of Dynamic Crosstalk Delay in Coupled Interconnect using FDTD," submitted to International Conference on Communication, Computing & Security (ICCCS), 8-10 Oct. 2012, NIT Rourkela ,. (Review result awaited)