AN ANALYTICAL STUDY OF DOUBLE GATE MOSFET

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

SOLID STATE ELECTRONIC MATERIALS

By

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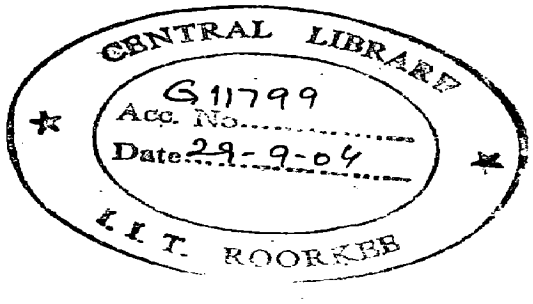

DEPARTMENT OF PHYSICS

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CANDIDATE'S DECLARATION

I hereby declare that the work that is being presented in this dissertation report entitled, **"An Analytical Study of Double Gate MOSFETs"**, for the partial fulfillment of the requirement for the award of degree of, **"Master of Technology"**, in **Solid State Electronic Materials** submitted in the Department of Physics, I.I.T. Roorkee, Roorkee. This is an authentic record of my own carried out under the supervision of **Dr. S. Sarkar**, Professor, Department of Electronics and Computer Engineering, I.I.T. Roorkee, Roorkee and **Dr. V. K. Tandon**, Associate Professor, Department of Physics, I.I.T. Roorkee, Roorkee.

I have not submitted the matter embodied in this dissertation work for the award of any other degree.

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CERTIFICATE

This is to certify that the work related to the dissertation report entitled, "**An Analytical Study of Double Gate MOSFETs**", has been carried out by **Miss Shweta Sharma** under our supervision.

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I would like to dedicate this work to my late father's memory.

I would also like to thank everyone whose help I have taken wittingly or unwittingly.

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ABSTRACT

In the present work, an improved analytical model for current-voltage relationship for DG MOSFET is developed by taking into account the effects of Multi-subband occupancy and Drain Induced Barrier Lowering (DIBL). The current-voltage characteristics obtained by the use of this model are compared with experimental and simulation results reported in literature. The effects of backscattering on current-volatge characteristics are also studied.

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Chapter - 1

INTRODUCTION

1.0 INTRODUCTION:

MOSFETs of channel lengths in the nanometer region are finding ample applications in the ultra-large scale integration (ULSI) chips. According to the updated 2000 edition of the International Roadmap for semiconductors the MOSFET will reach below 20 nm channel lengths by 2016 [1]. At the same time the theoretical studies indicate that the field effect action can be maintained to channel lengths below 10 nm where direct source to drain tunneling may take over the gate control. But the scaling of the field effect transistor below this milestone requires intolerably thin gate oxide and unacceptably high channel doping and therefore advocates a departure from the conventional MOSFET concepts [1].

One of the most promising new device structures, scalable to dimensions below 10 nm is the double gate MOSFET [2]. The structure with two gates and an extremely thin body suppresses short channel effects due to better control of the channel region. The double gate (DG) MOSFET has been identified in the International Technology Roadmap for Semiconductors (ITRS) as the most promising device structure that enables further CMOS scaling for its higher drive current, improved short channel effect control and potential circuit design flexibility.

While the majority of DG MOSFET research has focused on numerical simulations, compact physics based device models are highly desirable in order to gain physical insight into the device's operating principles, facilitate device designs, identify key technological challenges to its fabrication, investigate its application in circuitry and project its ultimate scaling capability. So, in this work, an analytical

model for double gate MOSFET is developed that accounts for quantum mechanical effects of-

(a) Band splitting into sub bands.

(b) Two-dimensional effect like Drain induced barrier lowering (DIBL).

The model thus developed is used for the study of-

(a) the effect of Multi-subband occupancy on I-V Characteristics of the model developed.

(b) the effect of DIBL on I-V Characteristics.

(c) the combined effect of. Multi-subband occupancy and DIBL on the I-V Characteristics.

Conventional sub-micrometer MOSFETs is well described by a transport model based on carrier mobility. The model assumes that the device size is far larger than the carrier mean free path, and carriers undergo many scattering events in the course from the source to the drain. In recent nanoscale MOSFETs, however, the device size approaches the length of the mean free path and carriers undergo only a small number of scattering events from the source to the drain. Such nanoscale MOSFETs are mostly analyzed in terms of the mobility theory [3]. However, these "quasi-ballistic" MOSFETs can be better analyzed by treating carrier transport as quasi-ballistic with a limited number of scattering events [3].

So, in this work, first the I-V characteristics will be obtained without considering any scattering event and then the effect of scattering will be studied by introducing backscattering parameter in the drain current model developed.

A detailed flow-chart showing various steps undertaken in the work reported is shown in Figure 1.1

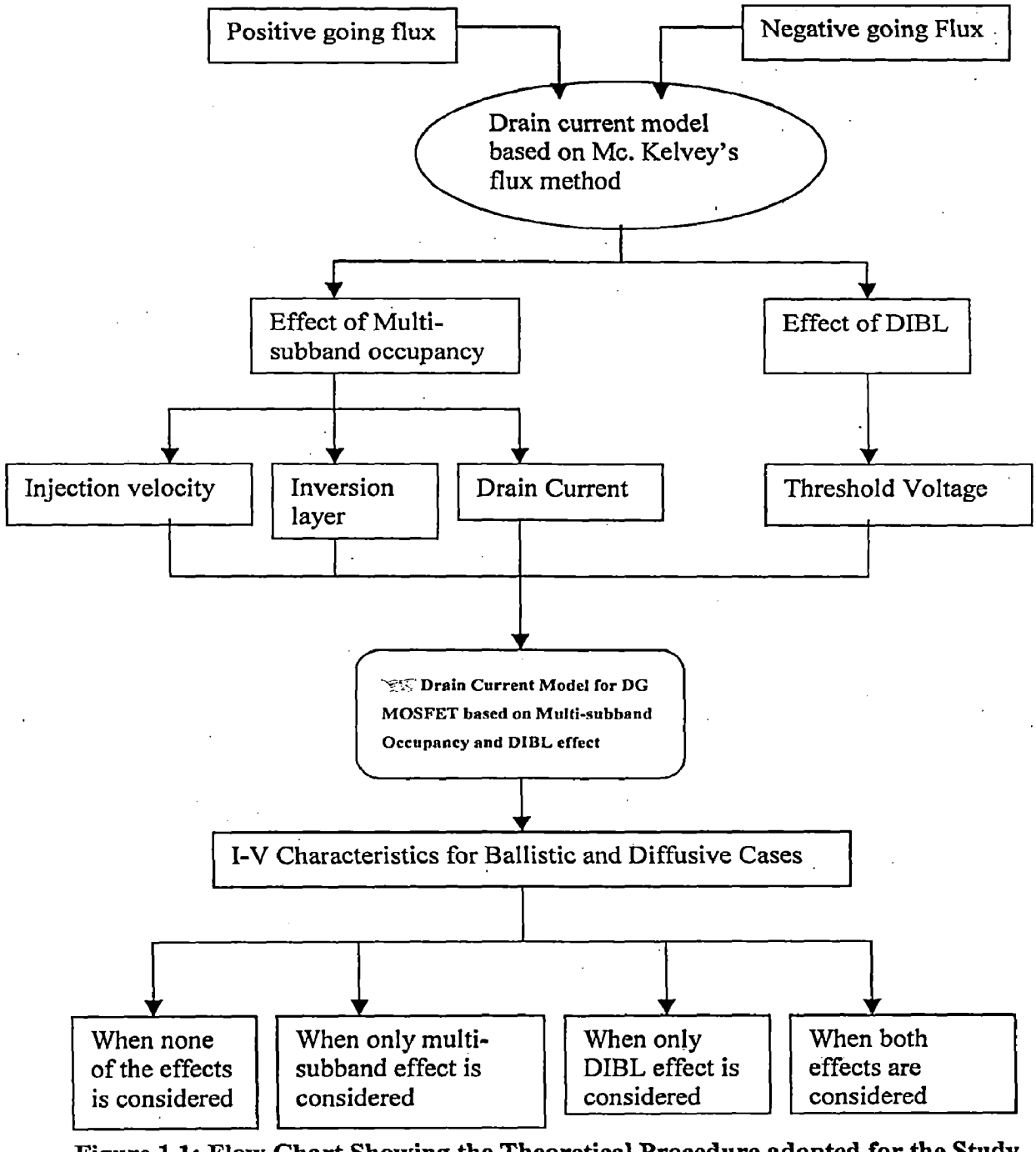


Figure 1.1: Flow Chart Showing the Theoretical Procedure adopted for the Study

Chapter - 2

OVERVIEW OF DEVELOPMENTS IN NANO-METER MOS-TECHNOLOGY

2.0 OVERVIEW OF DEVELOPMENTS IN NANO-METER MOS-TECHNOLOGY

2.1 Introduction:

The technology of choice for high-speed, low power dissipation, and high packing density in VLSI applications is silicon CMOS. Downscaling for the past 30 years has produced high performance chips with low cost per function [1]. As can be seen from [4], the transistor gate length scaling down to 9nm is projected to continue through 2016. Even if lithography and etching techniques can provide the necessary dimensions, bulk CMOS will run into a number of short channel effects associated with transistor scaling. The short channel effect (SCE) is characterized by threshold voltage (V_t) roll off, drain induced barrier lowering (DIBL), and subthreshold swing S. As the gate length (L_G) of a MOSFET is scaled with all other device parameter held constant, S increases and V_t decreases, which degrades MOSFET performance. The ratio of on current to off current (I_{ON}/I_{OFF}) is reduced, giving designers a tradeoff between circuit speed and static power dissipation.

Currently, a number of front-end process solutions can be employed for scaling bulk CMOS to avoid unwanted SCE. These include high-k dielectrics, incorporation of metal gates, and elevation of source and drain regions [5], [6]. High-k dielectrics can be used to decrease the effective oxide thickness without increasing I_{OFF} by reducing oxide-tunneling current. Metal gates solve the gate poly-Si depletion problem, which causes an increase in the oxide capacitance and lowers I_{ON} [2]. Elevated source/drain regions allow for lower series resistance and thus, greater on current. Also, tailoring the doping profile with retrograde channel profiles [6], halo ion implants [7], and ultra-shallow junction depths is

often performed in order to tame the SCE. However, these improvements are not expected to push CMOS scaling down below the 65nm technology node, which is anticipated to be in production lines by 2007 (highlighted in Table 1) [2]

2.2 Scaling Problems in Nano-meter range:

As the limit of bulk Si CMOS scaling approaches, new devices with slight variations to classical bulk CMOS have brought much attention to university labs and industry alike. Some of these devices include partially and fully depleted silicon-on-insulator (SOI) [8], the gate all around or surrounding-gate MOSFET [9], SiGe MOSFETs [10], low temperature CMOS [11], and double-gate (DG) MOSFETs [1] [12].

A MOS transistor is called a short channel device if its channel length is on the same order of magnitude as the depletion region thickness of the source and the drain junctions. Alternatively, a MOSFET can be defined as a short channel device if the effective length L_{eff} is approximately equal to the source and drain junction depth x_j. As we go on reducing the channel length following problems can occur:

Punch-through: As the channel length is on the same order of magnitude as the source and drain depletion region thickness, for large drain bias voltages, the depletion region surrounding the drain can extend farther toward the source, and the two depletion regions can eventually merge as can be seen from the figure 2.21 [16]. This condition is termed punch-through, the gate voltage loses its control upon the drain current, and the current rises sharply once punch-through occurs. Being able to cause permanent damage to the transistor by localized melting of material, punch-through is obviously an undesirable condition and should be prevented in normal circuit operation.

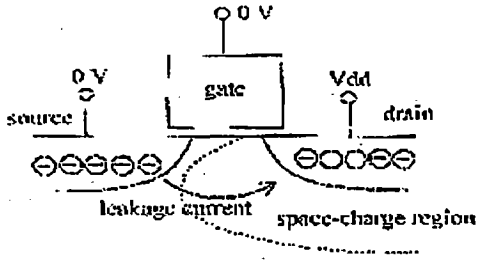


Figure 2.21: Short channel effect in a MOSFET.

Scaling of gate oxide thickness: Scaling of gate oxide thickness is restricted by processing difficulties involved in growing very thin, uniform silicon-dioxide layers. The major problems are the following:

(i) ***Pinholes:*** Localized sites of nonuniform oxide growth, called *pinholes,* may cause electrical shorts between the gate electrode and substrate.

(ii) ***Oxide Breakdown:*** Another limitation on the scaling of gate oxide thickness is the possibility of *oxide breakdown.* If the oxide electric field perpendicular to the surface is larger than a certain breakdown field, the silicon-dioxide layer may sustain permanent damage during operation, leading to the device failure.

High-Field Effects: Advances in VLSI fabrication technologies are primarily based on the reduction of device dimensions, such as channel length, the junction depth and the gate oxide thickness. This decrease in critical device dimensions to nanometer ranges, accompanied by increasing substrate doping densities, results in a significant increase of

the horizontal and vertical electric fields in the channel region which will give rise to following effects:

(i) ***Hot carrier induced Degradation:*** As the device dimensions are reduced horizontal and vertical electric fields increase, electrons and holes gaining high kinetic energies in the electric field (hot carriers) may, however, be injected into the gate oxide, and cause permanent changes in the oxide interface charge distribution, degrading the current voltage characteristics of the MOSFET as can be seen from figure 2.22 [16].

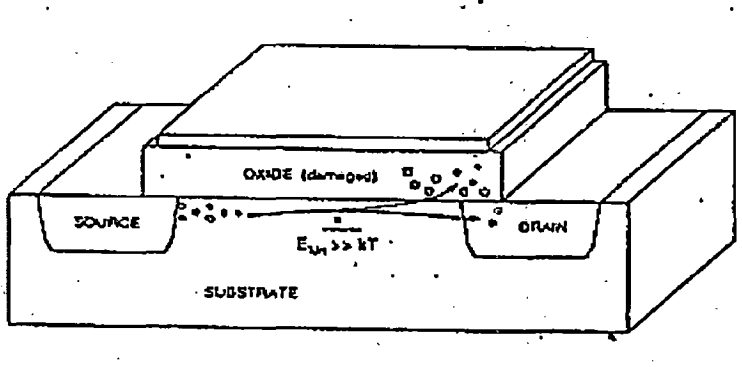


Figure 2.22: Hot-carrier injection into the gate oxide and resulting oxide damage.

Since the likelihood of hot carrier induced degradation increases with shrinking device dimensions, this problem can be considered as one of the most important factors that may impose strict limitations on maximum achievable device densities in VLSI circuits. The channel hot electron effect is caused by electrons flowing in the channel region, from the source to the drain. This effect is more pronounced at large drain to source voltages, at which the lateral electric field in the drain end of

the channel accelerates the electrons. The electrons arriving at the Si-SiO_2 interface with enough kinetic energy to surmount the surface potential barrier are injected into the oxide. Electrons and holes generated by impact ionization also contribute to the charge injection. The damage caused by the hot carrier injection affects the transistor characteristics by causing degradation in transconductance, a shift in the threshold voltage, and a general decrease in the drain current capability. This performance degradation in the device leads to the degradation of circuit performance over time. Hence new MOSFET technologies based on smaller device dimensions must carefully account for the hot carrier effects.

(ii) Velocity Overshoot Effect: It is one of the most important effects from the practical point of view as it is directly related with the increase of current drive and transconductance experimentally observed in short channel MOSFETs [17]. It has been shown that an electric field causes the electron velocity to overshoot the value that corresponds to the higher field for a period shorter than the energy relaxation time (the time needed by the electron to once again reach equilibrium with the lattice) therefore as the longitudinal electric field increases the electron gas starts to be in disequilibrium with the lattice. There is an insufficient number of phonon-scattering events experienced by the electron during its flight, with the result that electrons can be accelerated to velocities higher than the saturation velocity, thus approaching ballistic transport conditions. This effect is due to the non-equivalence of momentum and energy relaxation time.

Effect of external source and drain resistance: Another limiting factor on CMOS scaling is the effect of external source and drain resistance in shallow junction devices.

One of the fundamental challenges in modern device performance is the trade-off between short-channel effects and the impact of source-drain series resistance [18]. When making the gate length small, the space charge region near the drain touches the source in a location below the surface where the gate bias cannot control the potential, resulting in a leakage current between the source and drain via the space charge region as shown in figure 2.2 (a) the so called short channel effect of MOSFETs. For a MOSFET to operate as a VLSI component, the capability of switching off this current path and suppressing short-channel effects is a major priority in MOSFET design. In the on state, reduction of gate length is desirable to minimize the channel resistance. However, when the channel resistance becomes as small as the source and drain resistance, further improvements in drain current can not be expected because increase in these resistances suppress the short channel effects.

2.3 Architecture and operating principle of DG MOSFET :

DG MOSFETs are fully depleted SOI structures, where an ultra-thin Si channel is surrounded by a gate on each side of the channel. Different configurations of the DG MOSFET include planar, vertical, finFET. Fig. 2.3 (a) illustrates a typical Symmetric DG MOSFET (SDG), with both gates of an identical material. If each gate has a different workfunction, then it is called an Asymmetric DG MOSFET (ADG) which is shown in figure 2.3 (b) [15].

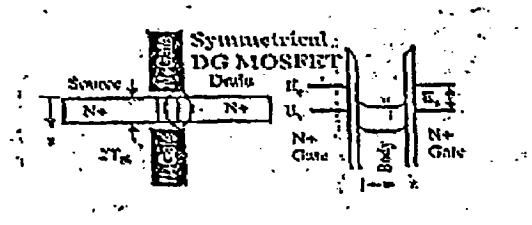


Figure 2.3 (a): Transistor Structure and Energy band Diagram for Symmetrical DG MOSFET.

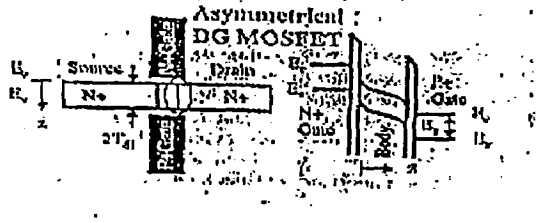


Figure 2.3 (b): Transistor Structure and Energy band Diagram for Asymmetrical DG MOSFET.

Both gates are electrically connected and jointly modulate the channel, where $V_{G2}=V_{G1}(t_{ox2}/t_{ox1})$ to compensate for different front and back oxide thickness. Unlike single-gate SOI MOSFETs, $t_{ox1}=t_{ox2}$ in DG MOSFETs for effective SCE control.

SCE is suppressed in this structure because no part of the channel is far away from a gate electrode. The drain electric field lines are terminated on the dual gates, which allows the source to be unaffected by the drain potential. Thus, leakage current is controlled and V_t roll off is suppressed along with DIBL. Estimates have been made that gate length for a DG MOSFET can be scaled two-three times shorter than a fully depleted SOI MOSFET [8].

Due to the increased coupling of the gate to the channel, and decoupling of the drain field to the channel, the double gate field effect transistors (DGFET) offers significant advantages. In double gate FETs, the bottom gate and top gate are usually connected together. DGFETs provide the maximum electrostatic control of channel, have the best current drive, and have the best scaling potential. Double gate MOSFETs can be scaled further than their bulk counterparts due to the suppression of short channel effects. Also it is argued that only DG MOSFETs have the potential of reaching the ballistic limit current. Kim and Fossum [13] conclude that optimally designed DG MOSFET can potentially yield the ultimate ballistic-limit current. They also conclude that this will not be the case for scaled bulk-Si or SOI MOSFETs due to the high transverse electric field caused by high gate-induced surface charge density and impurity scattering.

As far as electrostatics of DG MOSFET is considered there are two types as shown in Figure 2.31.

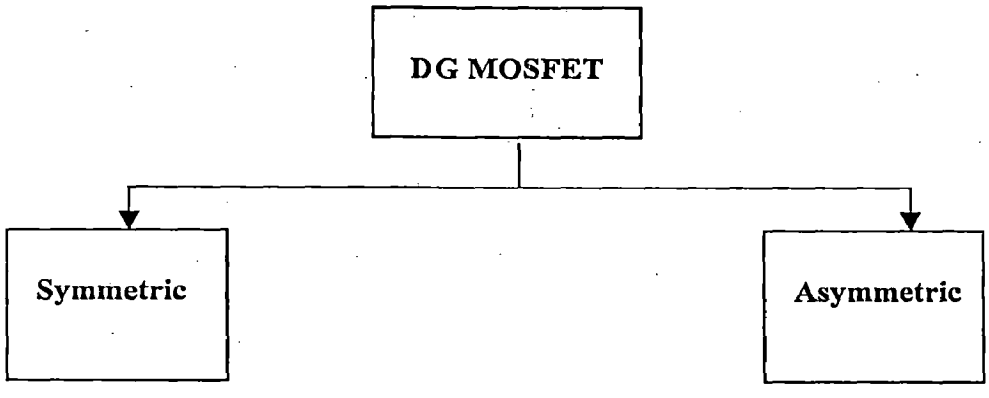


Figure 2.31: Types of DGMOSFET

For the Symmetric type, both the front gate and back gate have the same work function and are tied to the same bias, so the both of the surface channels turn on the same time. For the Asymmetric DG MOSFET the gates are fabricated using different work functions and/or are biased at different voltages, so that one of the surface channels turns on before the other and as the gate voltage is increased the other channel also inverts. For both types of DGMOSFET the on current doubles compared to a single gate device. The different modes of operation of DG MOSFET and its band diagrams are shown in figure 2.31 (a) and (b) [14].

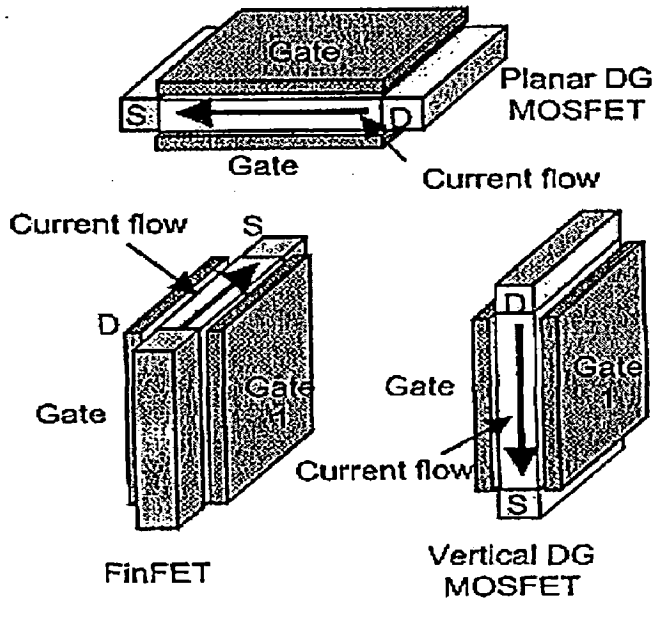


Figure 2.31(a): Different structures of DG MOSFET

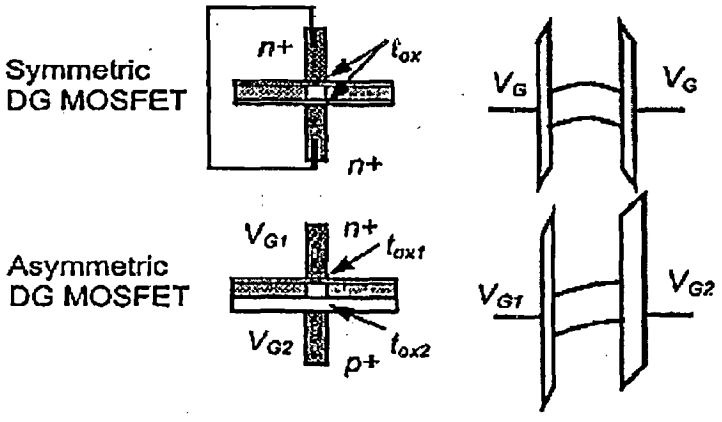


Figure 2.31(b): The two operation modes for DG MOSFETs

2.4 Fabrication of DG MOSFET:

The primary motivation for scaling CMOS devices is the increased functionality per cost and the improved performance of devices. As the scaling continues it becomes harder to fabricate devices without compromising performance due to undesirable effects such as threshold voltage roll-off, drain induced barrier lowering (DIBL) and degraded subthreshold slope. These effects cause device-to-device variations, increase the off current, and decrease the on current. Beside the short channel effects a number of technological barriers exist. As the gate length is reduced the wavelength of the light for the lithography equipment needs to reduce. Manufacturing such optical equipment at smaller wavelength becomes harder due to the availability of materials that should be used for these wavelengths. As gate length is reduced, gate oxide thickness must also be reduced, resulting in an increase in quantum mechanical tunneling excessively high electric fields. Eventually silicon oxide must be replaced with a high-k material so the

physical thickness of the material can be increased. The doping profile of the device needs to be controlled more accurately with each new generation, and the implantation and annealing technology needs to keep up with the stringent requirements of very sharp doping profiles. Parasitic resistance of the source and drain is also becoming a major issue that needs to be solved. A number of solutions have been proposed to these problems. Employing a Double Gate Field Effect Transistor (DGFET) structure instead of using bulk-Si transistors is one of these solutions. As the Double gate structure offers immunity to short channel effects and decreased parasitic capacitances, it can be scaled further than bulk-Si given that some of the technological problems are solved.

DG MOSFETs may be fabricated using a number of methods and in various configurations. Most methods are process challenging but are based on conventional bulk processing. An efficient DG fabrication process typically involves a uniform ultra-thin Si channel film and allows for variable transistor width, low series resistance, and short gate lengths.

The simplest method is planar formation of the DG by using bonded wafers and the local oxidation of silicon (LOCOS) technique [2]. After the thin body is defined from a bulk Si wafer by LOCOS, it is oxidized and the back-gate is defined. The structure is then bonded to a wafer handle, and the back of the active wafer is etched down to the LOCOS dielectric. Final processing forms the front gate and front oxide. Gate alignment is difficult and the etch-stop oxide layer must be precisely controlled for uniform oxide thickness.

In general, it is assumed that the ideal DG MOSFET is has symmetrical self-aligned front and back gates. SDG devices are difficult to fabricate due to alignment difficulties.

Some degree of asymmetry between front and back gate alignment is acceptable and has shown to have slightly degraded V_t roll off [2]. Gate delay, however, degrades significantly because of the extra source/drain overlap capacitance. Therefore it is ideal to have self-aligned front and back gates. The strength and weaknesses of DG MOSFET are given in Table 2.1.

TABLE 2.1: The strength and weakness of DG MOSFET

Double Gate (DG)	(a) Maximum electrostatic control of channel and best scaling potential. (b) Best current drive and performance. (c) OR logic function within single device.	(a) Difficult to fabricate. (b) Mis-aligned top and bottom gates result in extra capacitance and loss of current drive. (c) V_T control difficult by conventional means.

2.5 Conclusion:

In the push to make MOSFETs smaller than 0.1 micron in gate length, it may become necessary to change the structure of MOSFETs in order to achieve satisfactory electrical behavior. In several respects the double-gated MOSFET offers better characteristics than the conventional bulk Si MOSFETs. When there are two gates, the electric field generated by the drain electrode is better screened from the source end of the channel. Also, two gates can control roughly twice as much current as a single gate resulting in stronger switching signals.

With the possibility for scaling down to 10nm gate lengths, DG MOSFET devices show much promise. The benefits include higher drive current, improved subthreshold swing, greater SCE control, and circuit design flexibility. According to the 2002 ITRS update, "This architecture may be incorporated into the manufacturing process by about 2007".

Chapter - 3

AN IMPROVED ANALYTICAL MODEL FOR DG MOSFET

3.0: AN IMPROVED ANALYTICAL MODEL FOR DG MOSFET

3.1 Introduction:

Numerical simulation with different levels of approximation and compact models describing the ballistic transport in DG MOSFET are begin to appear in the literature [6] [18] [19]. These approaches are mainly based on two hypotheses:

(a) The carrier transport is assumed to be one dimensional in very thin (~ 1.5 nm thick) double gate devices and

(b) The carrier quantum mechanical tunneling through the source-drain potential barrier is often neglected.

However, this will lead to following problems:

(a) The drain-induced barrier lowering (DIBL) effect is an important feature that cannot be described in a one-dimensional (1-D) approximation.

(b) Secondly, quantum mechanical tunneling can be significant when a device is scaled in the 10 nm range and may even dominate in some regions.

Later on work has been done which fully accounts for quantum confinement and carrier degeneracy assuming single sub band conduction and without considering two-dimensional effects like Drain-Induced Barrier Lowering (DIBL) and also Gate-Induced Drain Leakage (GIDL) effect is not considered [6], [19]. Also, to take into account the higher sub band approximation Natori *et al* [20] used effective one-sub band approximation, where higher sub band contribution is effectively renormalized by slightly modifying the parameter, which originally indicated the number of lowest valleys. But, there is no work available in the literature that takes into account the multisubband effect

and Drain induced barrier-lowering effect in one model. So, in this work a new compact model for double gate MOSFET based on Mc. Kelveys flux theory is developed which will take into account the Multi-sub band conduction and Drain induced barrier lowering effect. This is the only model in which both these effects are fully accounted for.

When the bands at the surface are bent strongly, as in strong inversion where the Fermi level approaches the conduction band, the potential well formed by the insulator-semiconductor surface and the electrostatic potential in the semiconductor can be narrow enough that quantum mechanical effects become important. The motion of the electrons in the direction perpendicular to the surface is constrained to remain within the potential well, and if the thickness is comparable to the electron wavelength, size effect quantization leads to widely spaced sub bands of electron energy levels. The electron energy levels are grouped into these sub bands, each of which corresponds to a particular quantized level formation in the direction perpendicular to the surface [21].

In a quantized electron inversion layer at the surface of (100)-oriented silicon, the six equivalent minima of the bulk silicon conduction band split into two sets of sub bands. One set consists of the sub bands arising from the two valleys that show the longitudinal mass in the direction perpendicular to the surface. This set has energy levels E_0, E_1, E_2..... in the notation of Stern and Howard [22], [23]. The lowest sub band at the surface belongs to this set. The other set of sub bands arises from the four equivalent valleys that show a transverse mass in the direction normal to the surface. This set has energy levels designated as E_0', E_1', E_2'.....Generally, these levels line up such that E_0' is almost

degenerate with E_1 of the twofold set. ***Except at very low temperatures, it is unreasonable to assume that all the electrons are in the lowest sub band*** [21].

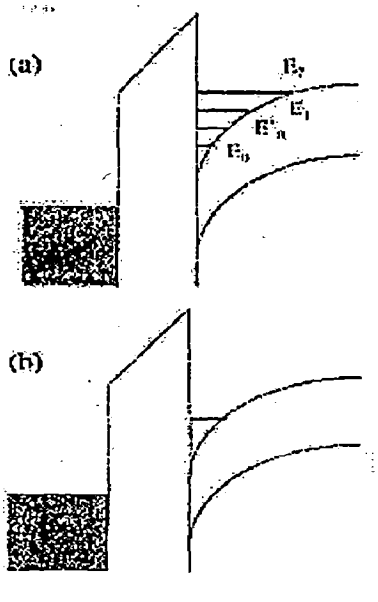


Figure 3.11(a): Multi-subband model (MSM) where many sub band structures in n- Si six valleys are considered

3.11(b): One sub band approximation where the lowest sub band is considered.

The effect of this quantization is two-fold:

(a) The density of carriers in the inversion layer is generally large enough to generate a self-energy correction to the surface potential, necessitating a self-consistent solution for ψ including the details of the charge density and its wave functions.

(b) The two-dimensional nature of the electron modifies the density of states and hence, modifies the transport devices.

As shown by the work done by D. K. Ferry [21] ***these quantum effects are expected to be more pronounced in small, sub micron devices.*** So, it is justifiable to take Multi sub band conduction into account.

Secondly, as the device size is reduced to the sub quarter micrometer range, two dimensional effects come into picture and DIBL i.e. drain induced barrier lowering effect is an important two dimensional effect and hence it is not reasonable to neglect DIBL effect in short channel MOSFETs.

The GIDL effect i.e. Gate-Induced Barrier Lowering effect is not considered in this work, as the work done in literature shows that the benefit of the Symmetrical DG MOSFET (the structure that is considered in this work) is the elimination of GIDL essentially [24].

Also, in very small transistors the channel and drain cannot be treated as the perfect absorbers for electrons injected from the source. Conventional sub-micrometer MOSFETs is well described by a transport model based on carrier mobility. The model assumes that the device size is far larger than the carrier mean free path, and carriers undergo many scattering events in the course from the source to the drain as can be seen from the figure 3.12.

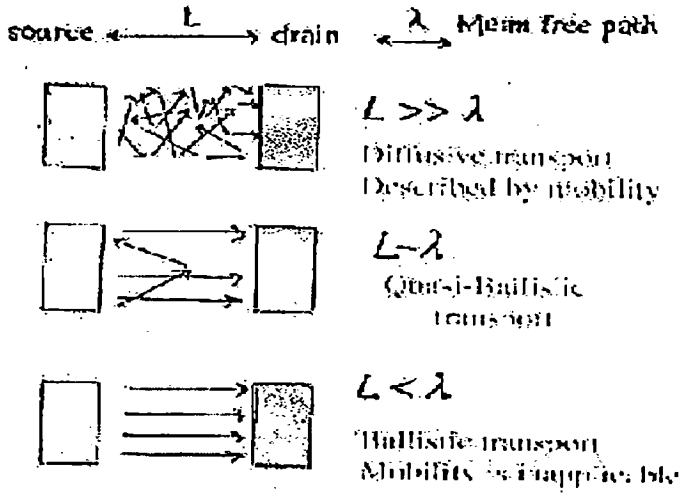


Figure 3.12: Classification of carrier transport in MOSFETs

In recent Nanoscale MOSFETs, however, the device size approaches the length of the mean free path and carriers undergo only a small number of scattering events from the source to the drain as can be seen from the figure 3.12. Such nanoscale MOSFETs are still usually analyzed in terms of the mobility theory but these "quasi-ballistic" MOSFETs are better analyzed by starting from the ballistic MOSFET characteristics without any scattering in the channel, and also by introducing a limited number of scatterings. So, the use of backscattering coefficient is necessary for analytical study of Double gate MOSFET.

3.2 Model Development:

Conventional transport models are based on the net current [6] [8] [9], but Mc. Kelvey's flux method decomposes the current into directed flux traveling in the positive and negative directions. The application of the flux method to nano-scale devices has been reported in [25]. Figure 4.21 illustrates the directed fluxes in a MOSFET. Fluxes at the top of the source-to-channel barrier are focused, which is defined as the beginning of the channel [27]. The positive directed flux $F^{+}(0)$ is due to thermal emission from the source over a barrier whose height is determined by MOS elecrostatics and the negative directed flux contains two components, one arising from the portion of the flux injected from the drain that transmits to the top of the barrier and the other due to the backscattering of the positive directed flux.

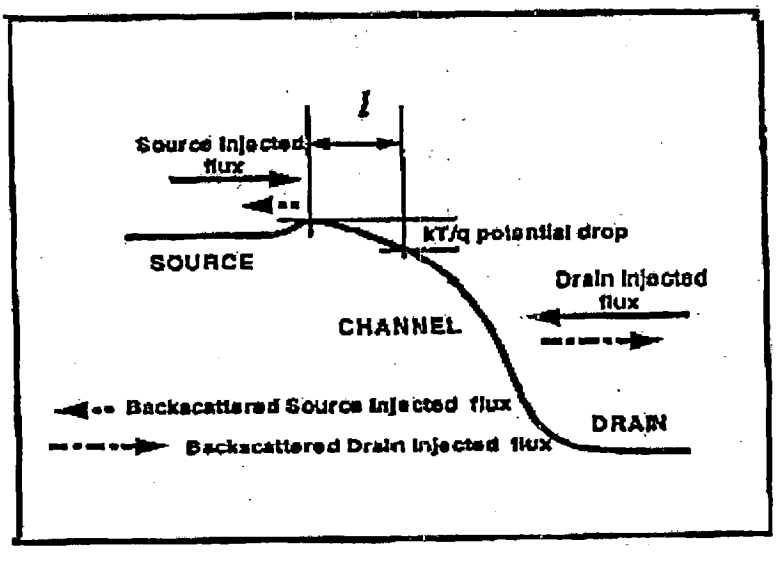


Figure 4.21: Illustration of carrier backscattering in a MOSFET under high drain bias.

Having defined the directed fluxes, the drain current is readily evaluated from the difference of the positive going flux and negative going flux. The drain current is thus obtained is [25]:

$$\frac{I_{DS}}{W} = Q_i(0)\frac{(1-r)}{(1+r)}\left\{v_{inj}\frac{\Im_{1/2}(\eta_F)}{\Im_0(\eta_F)}\right\}\left[\frac{1-\frac{\Im_{1/2}(\eta_F-U_D)}{\Im_{1/2}(\eta_F)}}{1+\left(\frac{1-r}{1+r}\right)\frac{\Im_0(\eta_F-U_D)}{\Im_0(\eta_F)}}\right] \quad \text{.....(i)}$$

The first factor on the RHS of the above equation is the inversion layer charge at the top of the source-to-channel barrier, which is determined by MOS electrostatics. The second factor describes the reduction of current due to carrier backscattering. The third factor is the degenerate thermal injection velocity. The fourth factor accounts for the drain bias dependence, it is proportional to $U_{DS}=V_{DS}/k_BT/q$ for low drain bias and approaches one for high drain bias. The above current model is based on following assumptions:

(a) one-subband occupation i.e. only lowest sub band is filled at room temperature and

(b) two-dimensional effects like Drain induced barrier lowering effect (DIBL) and punchthrough are not considered.

In order to incorporate the effect of Multi-subband occupancy and DIBL effects equation (i) has to be modified, as these effects will affect the expressions for charge, injection velocity etc. So, in the next section these effects are discussed and then after substituting the expressions for the charge, injection velocity etc. in equation (i) a drain current model will be developed for DG MOSFET that will take into account both the Multi-subband effect and Drain induced barrier lowering effect.

3.21 Effect of Multi-Subband Occupancy:

The thickness of the silicon body is only a few nanometers, so the charge inside the channel can be modeled as two-dimensional gas in a quantum well [14,15]. The Si-SiO_2 interface is parallel to (100) plane of Si, and such confinement removes the six-fold valley degeneracy of bulk Si [28]. Instead, there appear two ladders of energy levels from two different values of effective masses. The first ladder results from higher longitudinal effective mass m_l^* and has a two-fold valley degeneracy. The second ladder has four-fold valley degeneracy. In this work, it is assumed that not only the lowest sub band with its two degenerate valleys is occupied but also the upper sub-band with fourfold valley degeneracy is also occupied. Now, this consideration of Multi sub band Occupancy will affect drain current, charge and injection velocity in the following way:

(a) Effect on Charge- Due to the confinement of electron motion normal to the Si-SiO_2 interface the conduction band within the transistor channel is split in several sub bands, each of which is associated with the corresponding energy eigen value. The channel charge per unit area Q_c may be expressed as:

$$Q_c = 2C_g(V_{GS} - V_T) \quad \text{.....(ii)}$$

The multi sub band conduction effect may be incorporated into the expression of Q_c through the expression for V_T which is [29]:

$$V_T = \phi_M - \chi + V_A - V_D + \frac{k_B T}{q}\log\left(\frac{2C_g k_B T}{q^2 N}\right) \quad \text{.....(iii)}$$

where,

ϕ_M = work function of gate material

χ = electron affinity of the semiconductor

N is the sum of the density of states in the lower and upper sub bands

i.e. $N = \sum_{k=1}^{2} N_k$

and $N_k = \frac{m_{dk}^{\times} k_B T}{\pi \hbar^2}$ represents the density of states in the sub band at energy $E_{n,k}$; $m_{dk}^{\times}$ is the density of states effective mass.

Also, $V_A = \frac{qN_A}{2C_g}$

$V_D = \frac{qN_D}{2C_g}$ are the contributions to the gate voltage due to the channel but since the channel is undoped in the considered device hence,

$V_A = V_D = 0.$

So, N_1 and N_2 are calculated by properly substituting the values of effective masses and then they are added and substituted in the expression for V_T which in turn is substituted in the expression for charge in order to evaluate charge. So, in this way it will reflect the change in charge i.e. effect on charge due to splitting of sub bands.

(b) Effect on Injection Velocity- Injection velocity will be different in different subbands. The injection velocity in the i^{th} sub band is given as[28]

$$v_{inj}^{i} = \sqrt{\frac{2k_B T m_{C_i}}{\pi m_{D_i}^2}} \quad \text{.....(iv)}$$

where, m_{Di} = density of states effective mass for the i^{th} sub band,

m_{Ci} = conductivity effective mass for subv band i.

Given as:

For first sub band,

$$m_{Ci} = 4m_t$$

$$m_{Di} = 2m_t$$

for second sub band,

$$m_{Ci} = 4(\sqrt{m_t} + \sqrt{m_l})^2$$

$$m_{Di} = 4\sqrt{m_t m_l}$$

where, m_l = longitudinal effective mass

$= 0.916\ m_0$

and, m_t = transverse effective mass

$= 0.19\ m_0$

After substituting the values of the relevant parameters the injection velocities for lower and upper sub bands are calculated as:

$$v_{inj}^{1} = 4.492 \times 10^5\ m/s$$
$$v_{inj}^{2} = 2.1594 \times 10^4\ m/s$$

Which shows that the carrier in the higher sub band has a velocity considerably lower than that of the carrier in the lowest sub band the result which is similar to the result reported in [20].

(c) ***Effect on Drain Current-*** When the SiO_2/Si interface is parallel to the [100] plane, the six equivalent minima of the bulk silicon conduction band split into two sets of sub bands [28] . The first set consists of the two equivalent valleys with-in-plane effective density-of-states mass $m_D=2m_t$ (where a factor of two accounts for the valley degeneracy) and perpendicular effective mass of m_l. the second set (Δ_4-band) consists of the four equivalent valleys with $m_D=4\sqrt{m_t m_l}$ (again factor of four accounts for valley degeneracy) and the perpendicular effective mass is m_t. The energy levels associated with the first set comprise the so called unprimed ladder of sub bands, whereas those associated with the second set comprise the primed ladder of sub bands [28].

The drain current is the sum of the contributions from the unprimed and primed sub bands.

3.22 Drain Induced Barrier Lowering Effect (DIBL):

Device performance can be greatly improved by reducing the gate length to enhance the transconductance and reduce the gate capacitance. But as the gate lengths are crossing the sub quarter micrometer range, short channel effects are becoming increasingly significant. One of the most important short channel effects is the drain-induced barrier lowering. This effect limits the minimum gate size to a greater extent and degrades the device performance.

In long channel devices, the source and drain are separated far enough that their depletion regions have no effect on the potential or field pattern in most part of the device. Hence, for such devices, the threshold voltage is virtually independent of the

channel length and drain bias. In a short-channel device, however, the source and drain depletion width in the vertical direction and the source drain potential have a strong effect on the band bending over as a significant portion of the device. Therefore, the threshold voltage and consequently the subthreshold current of short channel devices vary with the drain bias. The effect is referred to as drain induced barrier lowering. As the drain voltage increases, the drain to channel depletion region widens, resulting in a significant increase in the drain current.

One way to describe DIBL is to consider the energy barrier at the surface between the source and drain. Under off conditions, this potential barrier prevents electrons from flowing to the drain [30]. For a long channel device, the barrier height is mainly controlled by the gate voltage and is not sensitive to V_{th}. However, the barrier of a short channel device reduces with an increase in the drain voltage, which in turn increases the subthreshold current due to lower threshold voltage.

DIBL occurs when the depletion region of the drain interacts with that of the source near the channel surface. When a high drain voltage is applied to a short channel device, it lowers the potential barrier height and the source then injects carriers at the channel surface independent of the gate voltage. The channel length reduction in MOS transistors induces DIBL effects, resulting in a lowering of the source/substrate potential barrier after application of a high drain voltage. Devices with shorter channels experience a stronger DIBL effect and thus have severely reduced threshold voltages at high drain biases.

The threshold voltage reduction due to Drain induced barrier lowering effect is given as:

$$V_T = V_{T0} - \sigma V_{DS} \quad \text{.....(v)}$$

where σ is the DIBL coefficient which is defined in saturation as [31]:

$$\text{DIBL coefficient} = \frac{d\ln(I_d)}{dV_d} \quad \text{.....(vi)}$$

Calculation of DIBL coefficient is shown in Appendix A.

3.23 Backscattering Parameter:

In the case of full ballistic transport in the channel, the source injected positive going flux, crosses the channel and then reaches drain without any backscattering and r=0. The backscattering coefficient is determined by both carrier scattering and by the potential drop within the channel. According to the scattering theory, carriers are injected from the source to the low field region at the beginning of the channel over source potential barrier as shown in figure(3.23).

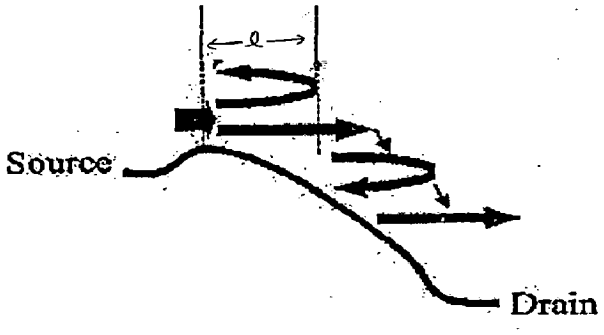


Figure 3.23: Backscattering of carriers

Some of the injected carriers backscatter in this low field region, which has length of 'l'. The length of this low field critical region is the distance over which the channel

potential drops by approximately kT/q (called kT layer). The carriers that cross the kT layer feel the high drain electric field, which acts as a absorber for the carriers and sweeps them towards the drain. Although the carriers scatter in the high field part of the channel, all of them cannot return to the source because of the field. The fraction that backscatters and returns to the source is defined as 'r', the backscattering coefficient. If backscattering occurs beyond a certain critical distance (denoted as l in figure 3.23) [27] then it is unlikely that the carrier will have sufficient longitudinal energy to surmount the barrier and exit into the source. More likely, it will be reflected by the channel potential, perhaps undergo several scattering/electric field reflections and exit from the drain. The critical layer for backscattering in a MOSFET is also roughly the distance over which the first k_BT/q of channel potential drops, typically a small fraction of the channel length. This occurs because the longitudinal energy of the backscattered electrons is randomized to have an average energy of k_BT so that carriers that scatter beyond the point have little chance of returning to the source. A simple expression that relates l to r is given as [25]:

$$r = \frac{l}{l+\lambda} \quad \text{.....(vii)}$$

where,

λ = low field momentum relaxation length

= 4.7nm

and $$l = L\left(\beta \frac{k_BT/q}{V_{DS}}\right)^{\alpha}$$

where α and β are the fitting parameters given as [25]:

$\alpha = 0.57$

$\beta = 1.18$

Hence, after incorporating all these effects, the drain current model that describes multi sub band conduction and drain induced barrier-lowering effect is developed as:

$$\frac{I_D'}{W} = 2C_g(V_{GS} - \sigma V_{DS})\left(\frac{1-r}{1+r}\right)v_{inj}' \frac{\Im_{1/2}(\eta_{Fi})}{\Im_0(\eta_{Fi})} \frac{\left[1 - \frac{\Im_{1/2}(\eta_{Fi} - U_D)}{\Im_{1/2}(\eta_{Fi})}\right]}{\left[1 + \left(\frac{1-r}{1+r}\right)\frac{\Im_0(\eta_{Fi} - U_D)}{\Im_0(\eta_{Fi})}\right]} \quad \text{... (A)}$$

$$I_D = \sum_i I_D' \quad \text{.....(B)}$$

where,

I_D' = drain current contribution due to ith sub band

$$\eta_{Fi} = \frac{E_F - \varepsilon_i}{k_B T}$$

and ε_i is the energy of the i^{th} sub band given as:

$$\varepsilon_i = \frac{n^2 h^2}{8mt^2}$$, t = 1.5nm.

By substituting proper value of mass for upper and lower set of subbands energy for different subband may be calculated.

First term in the Equation (A) is the charge which is given by equation (ii), second term denotes the current reduction due to backscattering given by equation (iv), third term denotes the injection velocity which can be substituted by equation (iv), fourth term contains the Fermi Dirac integrals of order one half and order zero as defined by Blakemore [32] (Appendix B)

Equation (A) and (B) are the final equations that take into account the Sub band splitting effect and Drain induced barrier-lowering effect both.

Chapter - 4

RESULTS & DISCUSSION

4.0 RESULTS AND DISCUSSION

4.1 Device Under study:

Figure 4.1 shows the model device considered in this work, a symmetrical double gate (DG) MOSFET. The simple geometry of this model facilitates the development of analytical models. This device was previously considered in [25].

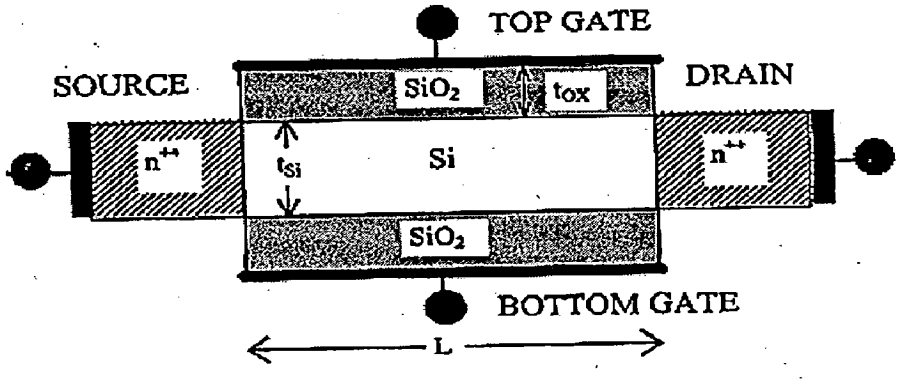


Figure 4.1:Schematic representation of Symmetrical DG MOSFET used as the Model Device in this work

The gate length is L, is, 20 nm and the Si-SiO_2 interface is parallel to (100) plane. The top and bottom gate oxide thickness are t_{ox}=1.5 nm, which is assumed to be scaling limit of oxide thickness before excessive gate tunneling current can be tolerated. The Si body thickness, t_{Si} , is taken as 1.5 nm. The same gate voltage, V_{GS}, is applied to both gates. The channel is undoped since the volume of the channel of this device is of the order of

10^{-19} cm^3, so even doping at a level as high as $10^{20}/cm^3$ would result in only few dopants in the whole channel. The n^+ source and drain are degenerately doped at a level of $10^{20}/cm^3$ while the value of carrier mobility inside such ultrathin Si channel is still an open question (simulated and measured values can be found in [26]), it is clear that though the undoped channel increases the channel mobility by eliminating ionized impurity scattering, the overall mobility will be reduced due to the proximity of two Si-SiO_2 interfaces and hence increased surface roughness scattering. In the present work, a low field mobility of 120 cm^2/V-sec [25] is assumed in the channel. All calculations are done for temperature T=300K.

Tables 4.1(a) and 4.1(b) shows the various parameters used in this work.

TABLE 4.1(a)

Device Parameter	Value
Gate length, L	20 nm
Channel width W	200 nm
Extended S/D junction depth	2 nm
Top and Bottom Gate Oxide Thickness t_{ox}	1.5 nm
Si Body Thickness t_{Si}	1.5 nm
Source Doping Conc. N_S	$10^{20}/cm^3$
Drain doping Conc. N_D	$10^{20}/cm^3$
Si-SiO_2 interface	parallel to (100) plane

TABLE 4.1(b)

Parameter	Value
Range for drain Source voltage V_{DS} [volts]	0.1-0.6 (in steps of 0.1)
Range for Gate Source voltage V_{GS} [volts]	0.4-0.5 (in steps of 0.05)
Source Series Resistance (R_S)	0
Temperature [in K]	300
Low field mobility [cm^2/V-sec]	120

4.2 Results and discussion:

Based on the developed analytical model for drain current for Double Gate MOSFET and using various parameters as shown in Tables 4.1(a) and 4.1(b), I-V characteristics are obtained on the basis of equations (A) and (B) and then following effects are considered-

(a) The effect of Muti-subband occupation on I-V Characteristics as can be seen from Figures 5.1(a)-5.1(d) for Ballistic case and Figures 5.4(a)-5.4(d) for Diffusive case.

(b) The effect of DIBL on I-V Characteristics, Figures 5.2(a)-5.2(d) for Ballistic case and Figures 5.5(a)-5.5(d) for Diffusive case depict this effect.

(c) The effect of both Multi-subband occupation and DIBL effect on I-V Characteristics as can be seen from Figures 5.3(a)-5.3(d) for Ballistic case and Figures 5.6(a)-5.6(d) for Diffusive case.

(d) The effects of varying drain bias at fixed gate voltage on drain current.

(e) The effect of varying gate voltage.

(f) Figure 5.7(a)-5.7(b) compares the I-V Characteristics for different cases.

Also, I-V Characteristics are obtained and above effects are considered for both the following cases:

(a) For ***Ballistic case*** i.e. without considering backscattering coefficient.

(b) For ***Diffusive case*** i.e. after taking into account backscattering effect.

From figures 5.1(a)-5.1(c), it is observed that drain current first increases with varying drain bias and then the current becomes almost constant in the saturation region and figure 5.1(d) denotes that the drain current increases with increasing gate bias.

Again, from figures 5.2(a)-5.2(c) it is clear that when DIBL effect is included it is observed that in this case the drain current increases slightly in the saturation region unlike the case with when only Multi-subband effect is considered.

And when both effects are considered simultaneously as can be seen from the Figures 5.3(a)-5.3(b), then in that case the drain current increases because of Multi-sub band effect and also, in the saturation region it does not become constant but it increases with varying drain bias because of DIBL effect.

Figure 5.7 shows the comparison and from it, it is observed that the drain current increases when we consider the Multi-subband effect then when none of the effects is considered. The drain current is further increased when DIBL effect is taken into account because DIBL effectively lowers the barrier potential source then injects more electrons and hence drain current increases because of DIBL effect. Figure 5.7(b) shows that the in drain current increases by 4.18% when Multi-subband effect is taken into account.

Also, it is seen that the current is reduced drastically as can be seen from Figures 5.8(a)-(c), 5.9(a)-(c) and 6.0(a)-(c), when we consider the diffusive case that is when we consider the backscattering parameter the drain current decreases from its value for the ballistic case i.e. for collision free case. Table 4.2 shows the percentage decrease in the drain current due to backscattering. The reduction in drain current is due to the increased number of scattering events and hence because of that lesser number of electrons will then reach to the drain and will constitute reduced drain current. So, the drain current reduces when backscattering parameter is taken into account that is also in agreement with the simulated result of [33].

Table 4.2: Percentage decrease in drain current when scattering is considered

Effect Considered	**Decrease Percentage of Drain Current at V_{DS}=0.5 volts**		
	V_{GS}=0.40volts	**V_{GS}=0.45volts**	**V_{GS}=0.50volts**
Only Multi-subband effect	66.87	66.95	66.95
Only DIBL effect	66.89	67.06	66.96
Both effects i.e. Multi-subband and DIBL	66.96	67.12	66.97

When the results obtained, based on the developed drain current model for DG MOSFET, are compared with the results due to Experimental work [34] and results due to Simulations [35], they show good agreement. Also, Figure 5.0(a)-5.0(d) shows the I-V Characteristics when none of the effect is considered and that shows that the drain current remains constant in the saturation region, which is in agreement with the work done in the literature

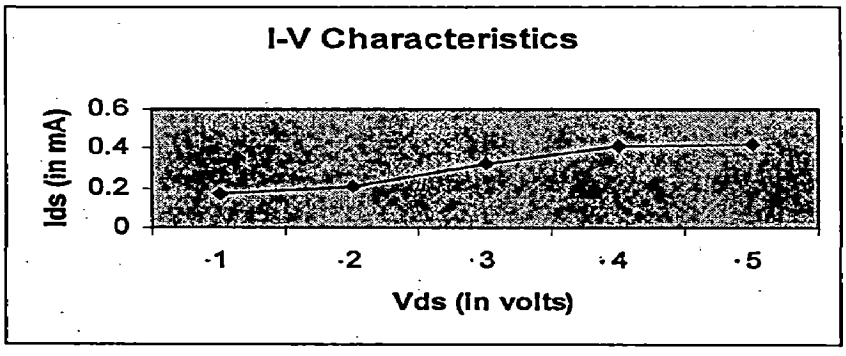


Figure 5.1(a) : Graphs showing the variation of drain current with drain bias
When only Multi-subband effect is considered
When Vgs=0.40 volts ,

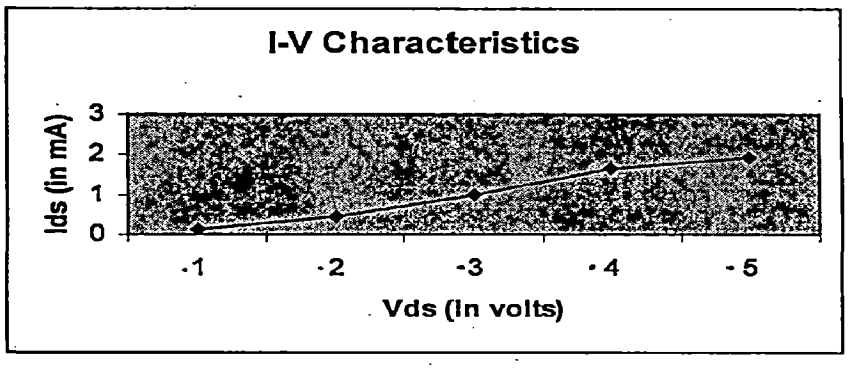


Figure 5.1(b) : Graphs showing the variation of drain current with drain bias
When only Multi-subband effect is considered
When Vgs=0.45 volts

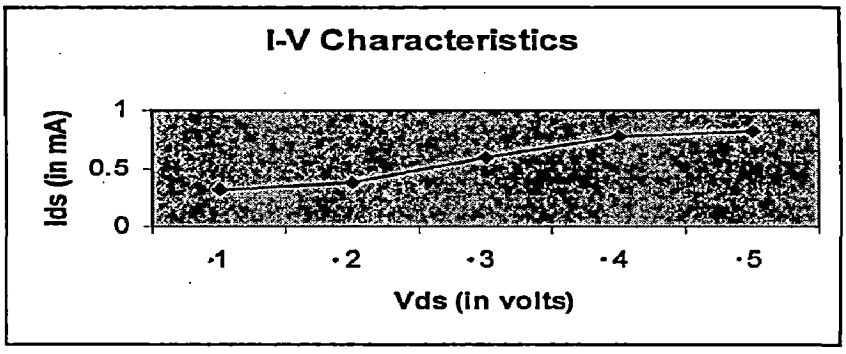


Figure 5.1(c) : Graph showing the effect on drain current with varying drain bias when only Multi-subband effect is considered at Vgs=0.50 volts.

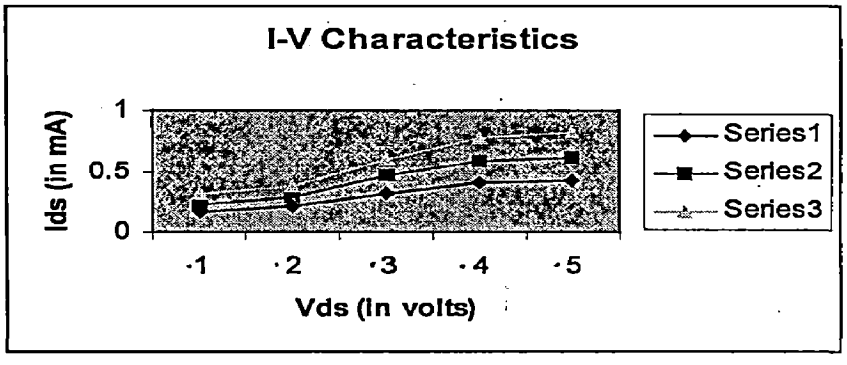


Figure 5.1(d): Graph showing the effect on drain current with varying Vds and Vgs. When only Multi-Subband effect is considered. Series 1 for Vgs=0.40 volts, Series 2 for Vgs=0.45 volts and Series 3 for Vgs=0.50 volts.

For Ballistic Case

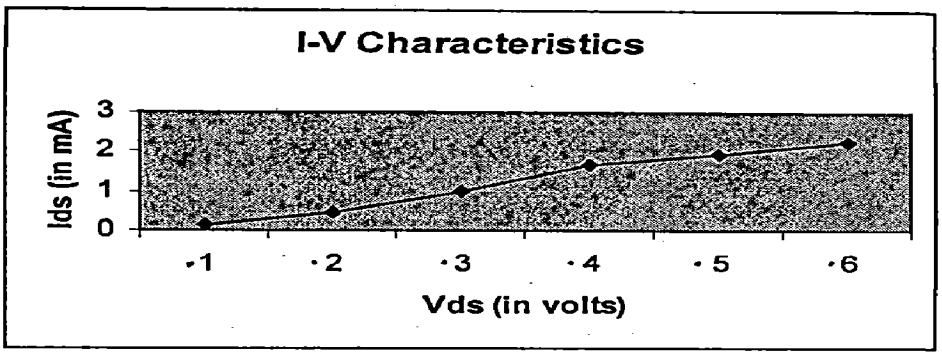


Figure 5.2(a): Graphs showing the effect of varying drain bias on drain current when only DIBL effect is considered , when Vgs=0.40 volts

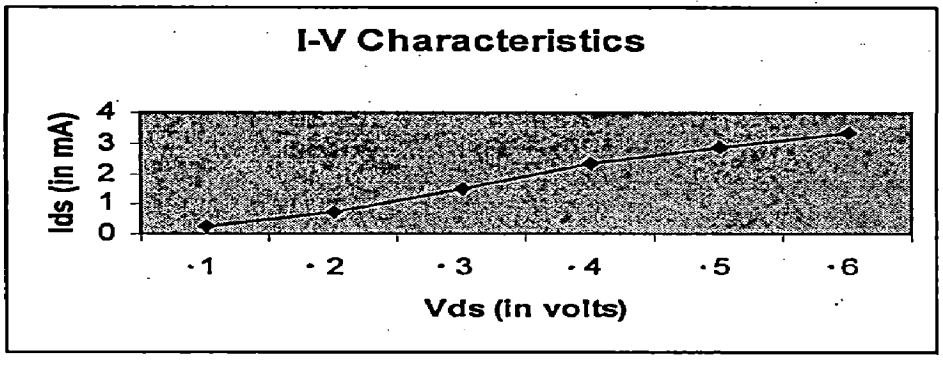


Figure 5.2(b): Graphs showing the effect of varying drain bias on drain current when only DIBL effect is considered , when Vgs=0.45 volts.

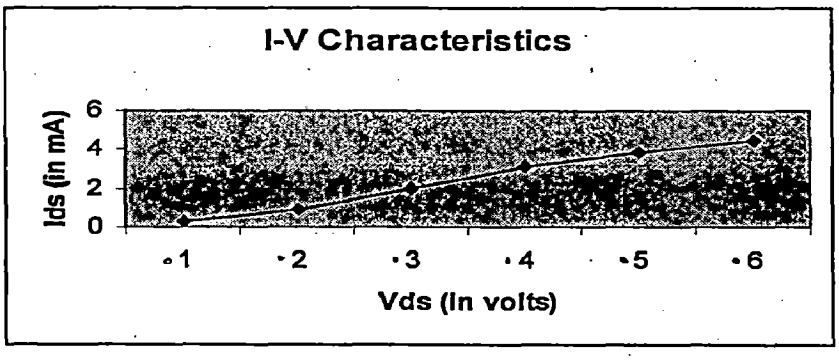


Figure 5.2(c) : Effect of varying drain bias on drain current when only DIBL effect is considered with Vgs=0.50 volts.

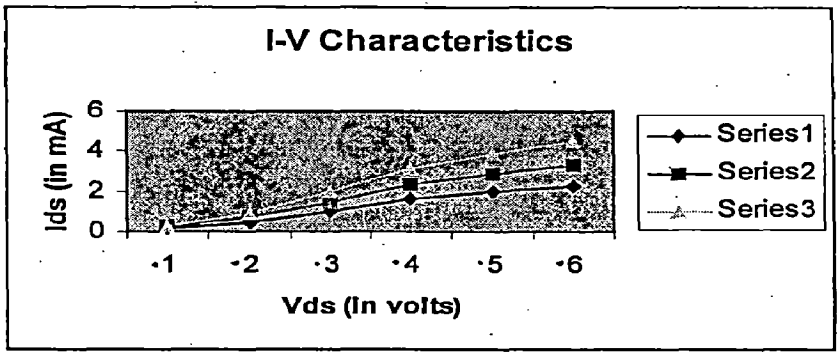


Figure 5.2(d): Graph showing Effect of varying drain bias and gate bias on drain current when only DIBL effect is considered. Series 1 for Vgs=0.40 volts, Series 2 for Vgs=0.45 volts and Series 3 for Vgs=0.50 volts.

For Ballistic Case

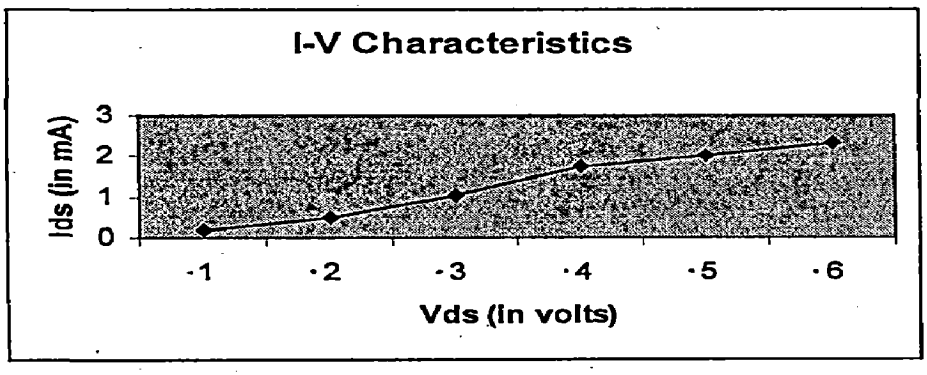


Figure 5.3(a): Graphs showing the variation of drain current with drain bias When both Multi-subband and DIBL effects are considered When Vgs=0.40 volts ,

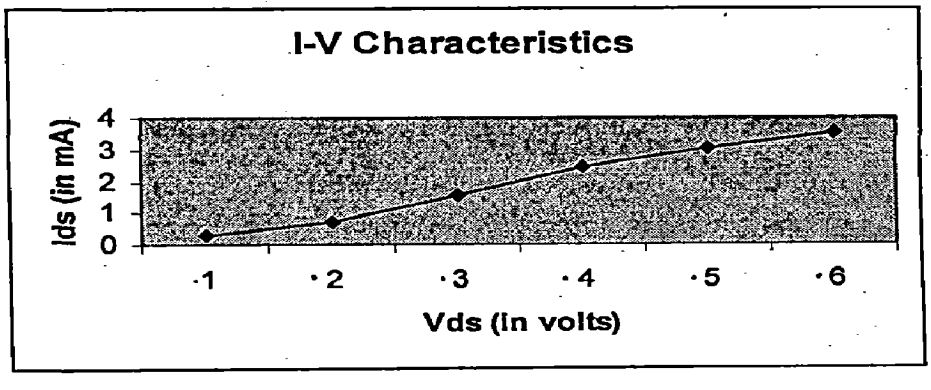


Figure 5.3(b): Graphs showing the variation of drain current with drain bias When both Multi-subband and DIBL effects are considered When Vgs=0.45 volts

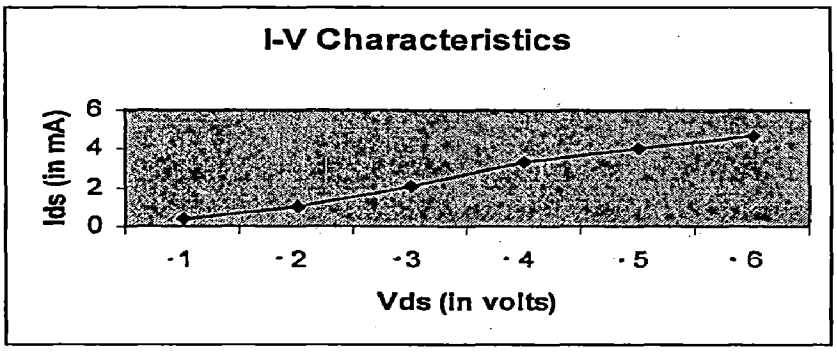


Figure 5.3(c) : Effect of varying drain bias on drain current when both Multi-Subband and DIBL effects are considered with Vgs=0.50 volts.

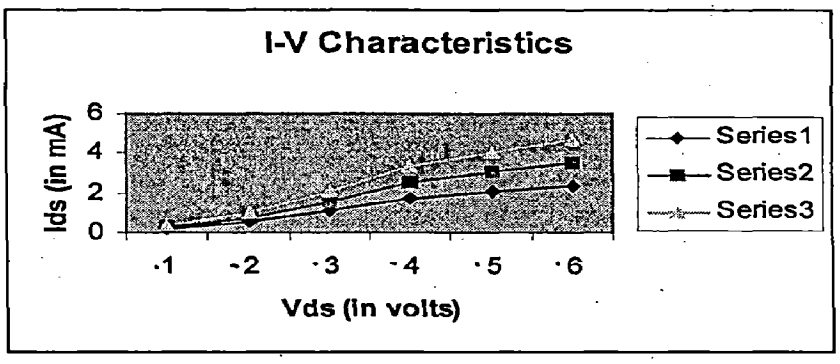


Figure 5.3(d): Graph showing Effect of varying drain bias and gate bias on drain current when both Multi-subband and DIBL effects are considered. Series 1 for Vgs=0.40 volts, Series 2 for Vgs=0.45 volts and Series 3 for Vgs=0.50 volts.

For Ballistic Case

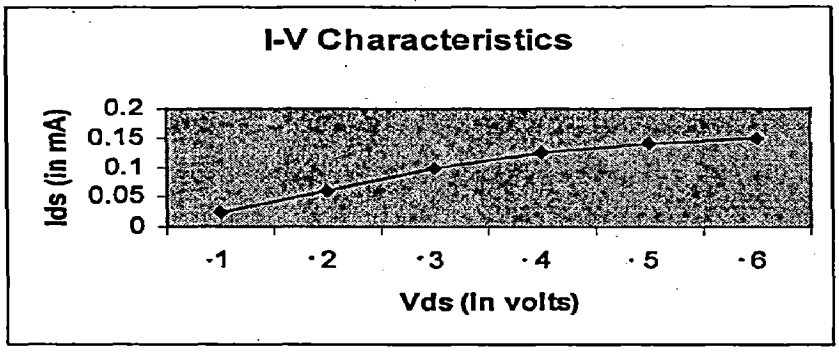


Figure 5.4(a): Graphs showing the variation of drain current with drain bias
When only Multi-subband effect is considered
When Vgs=0.40 volts

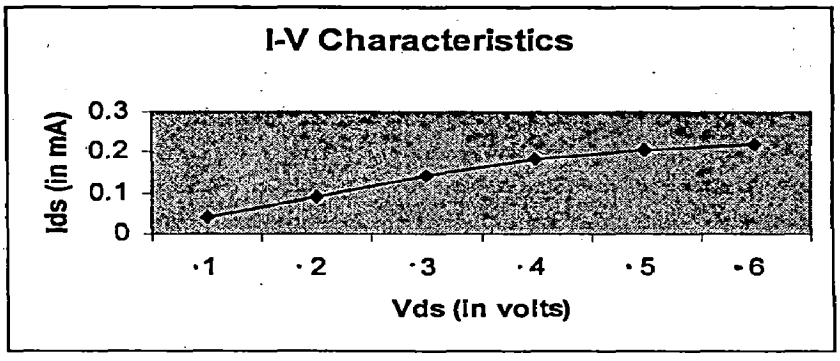


Figure 5.4(b): Graphs showing the variation of drain current with drain bias
When only Multi-subband effect is considered
When Vgs=0.45 volts

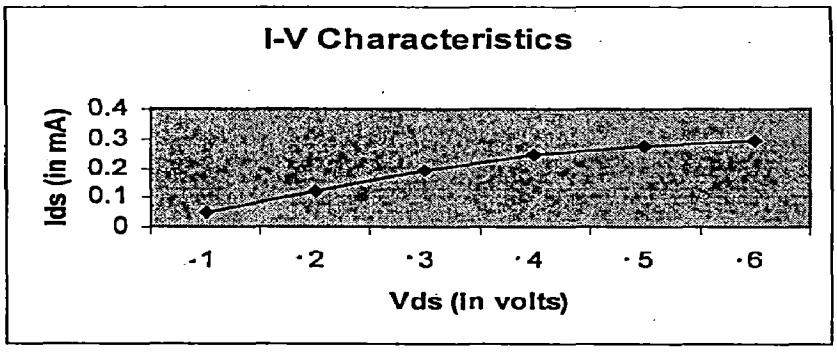


Figure 5.4(c) : Graph showing the effect on drain current with varying drain bias when only Multi-subband effect is considered at Vgs=0.50 volts

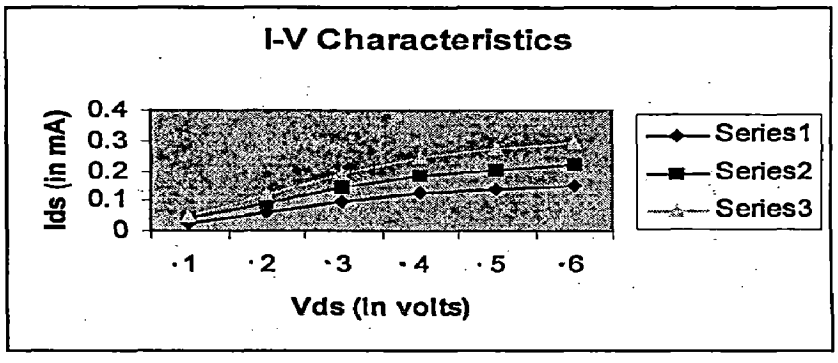


Figure 5.4(d): Graph showing the effect on drain current with varying Vds and Vgs. When only Multi-Subband effect is considered. Series 1 for Vgs=0.40 volts, Series 2 for Vgs=0.45 volts and Series 3 for Vgs=0.50 volts.

For Diffusive Case

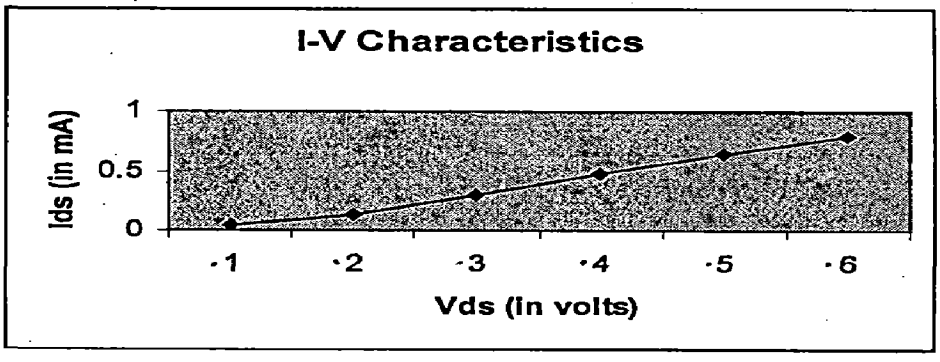


Figure 5.5(a): Graphs showing the effect of varying drain bias on drain current when only DIBL effect is considered when Vgs=0.40 volts

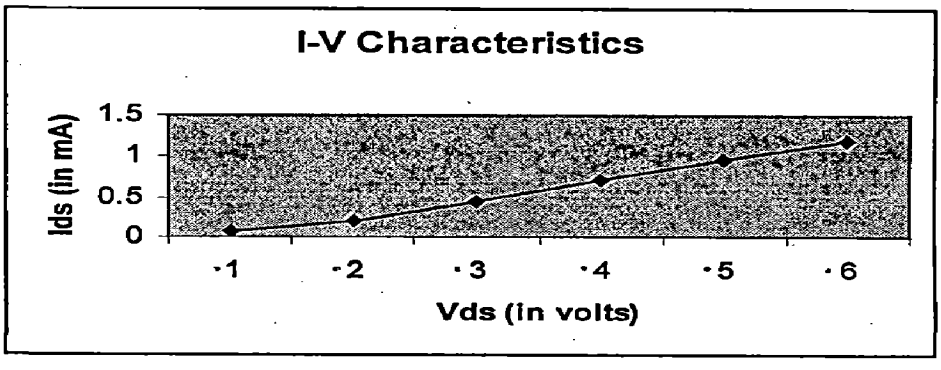


Figure 5.5(b): Graphs showing the effect of varying drain bias on drain current when only DIBL effect is considered , when Vgs=0.45 volts

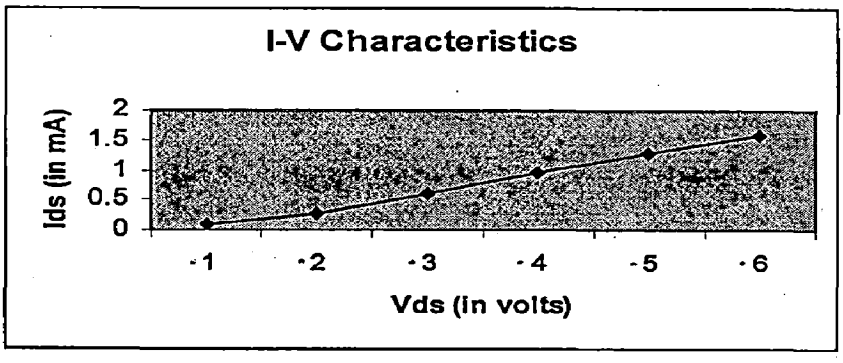


Figure 5.5(c) : Effect of varying drain bias on drain current when only DIBL effect is considered with Vgs=0.50 volts.

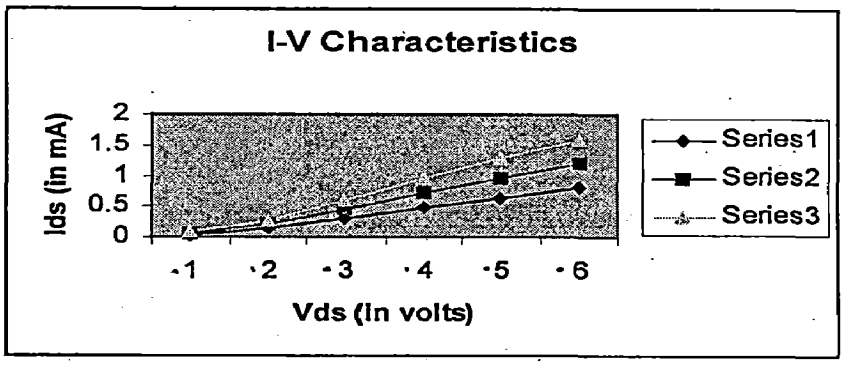


Figure 5.5(d): Graph showing Effect of varying drain bias and gate bias on drain current when only DIBL effect is considered. Series 1 for Vgs=0.40 volts, Series 2 for Vgs=0.45 volts and Series 3 for Vgs=0.50 volts.

For Diffusive Case

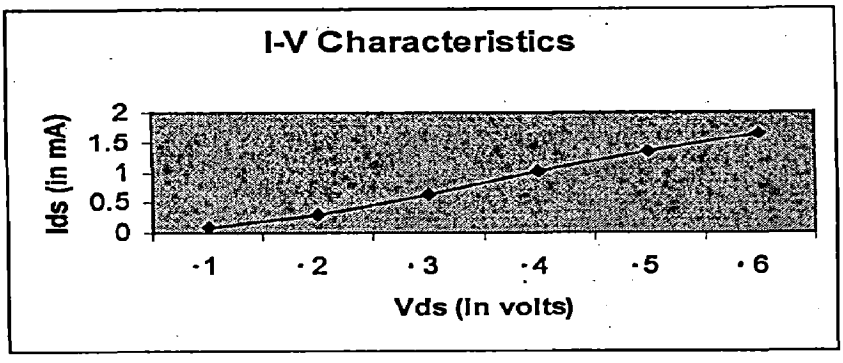


Figure 5.6(a): Graphs showing the variation of drain current with drain bias When both Multi-subband and DIBL effects are considered When Vgs=0.40 volts,

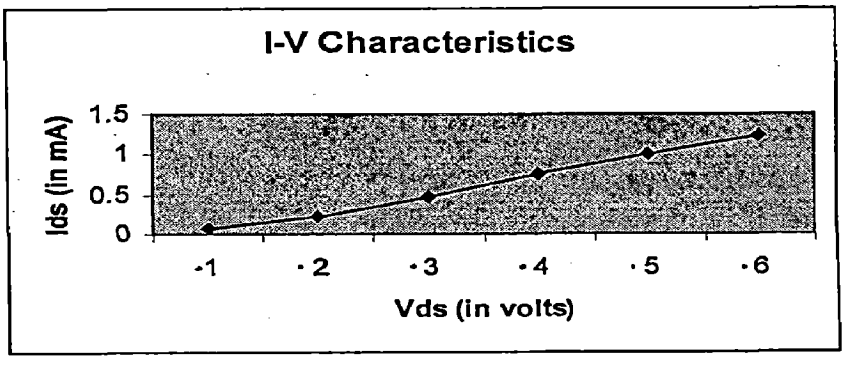


Figure 5.6(b): Graphs showing the variation of drain current with drain bias When both Multi-subband and DIBL effects are considered When Vgs=0.45 volts

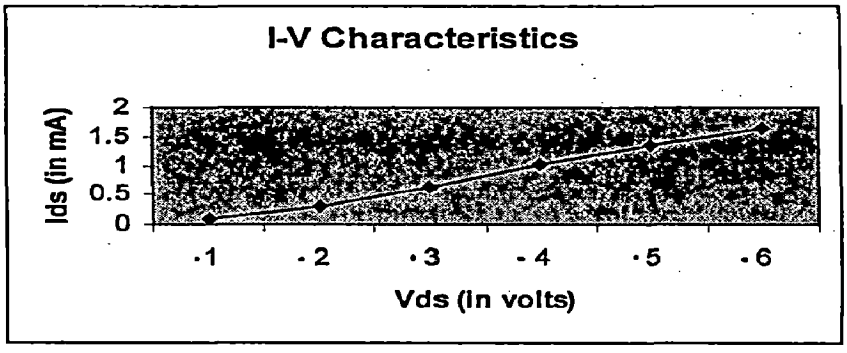


Figure 5.6(c): Effect of varying drain bias on drain current when both Multi-Subband and DIBL effects are considered with Vgs=0.50 volts.

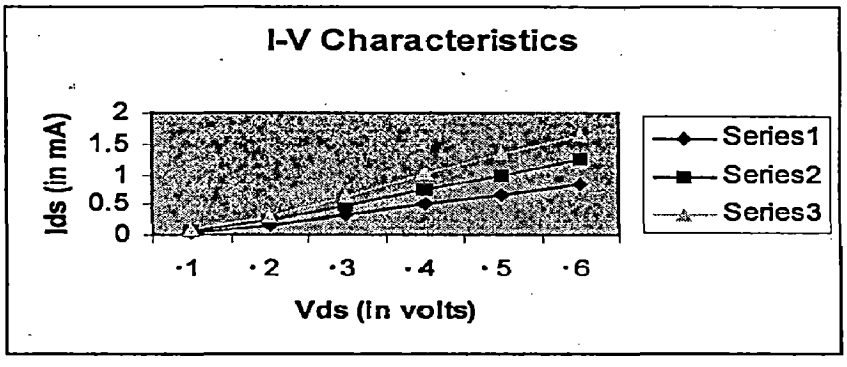
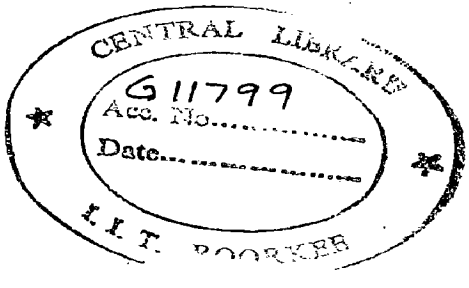


Figure 5.6(d): Graph showing Effect of varying drain bias and gate bias on drain current when both Multi-subband and DIBL effects are considered. Series 1 for Vgs=0.40 volts, Series 2 for Vgs=0.45 volts and Series 3 for Vgs=0.50 volts.

For Diffusive Case



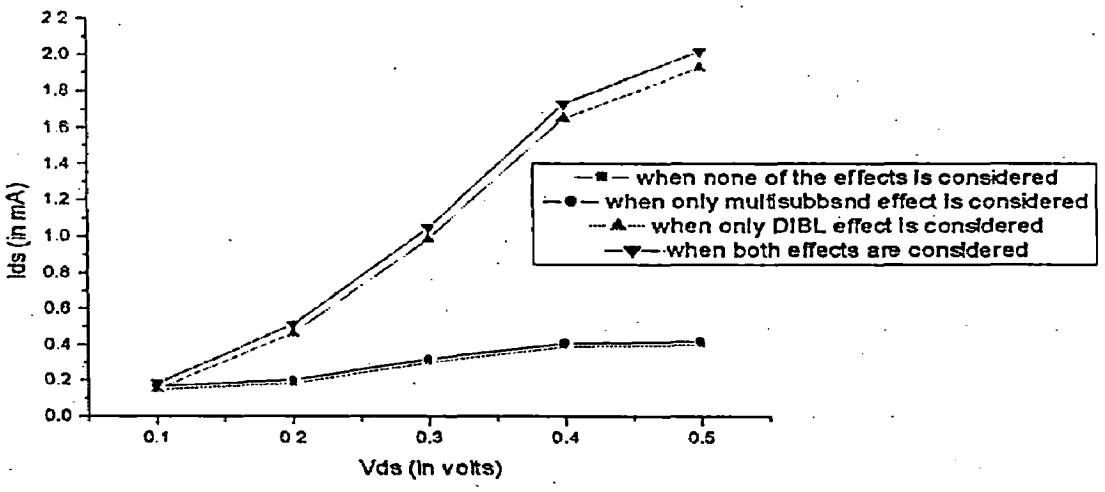


Figure 5.7: Graphs showing the change in drain current when different effects are considered and when no effect is considered at Vgs=0.40 for Ballistic case.

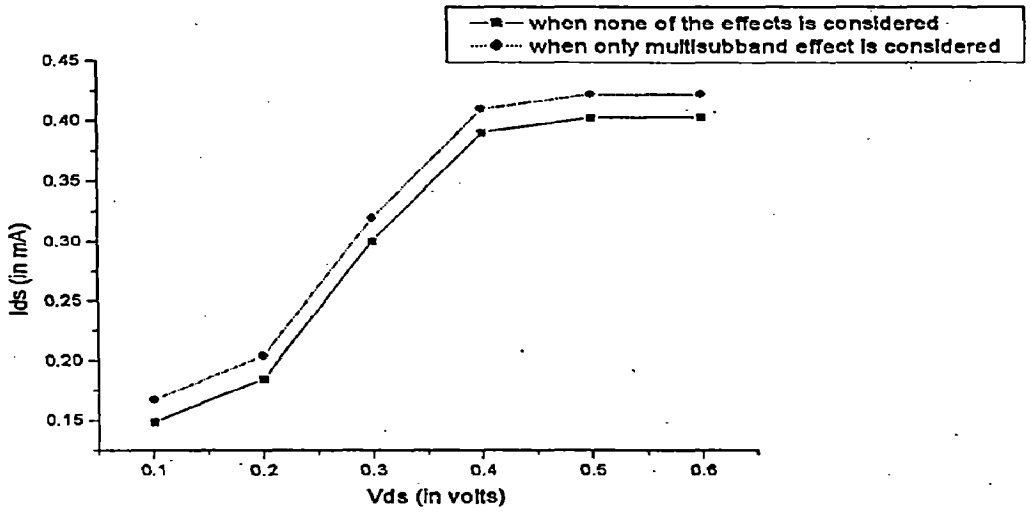


Figure 5.7 (a): Graph showing the effect of Multi-subband conduction on the drain current at Vgs=0.40 volts.

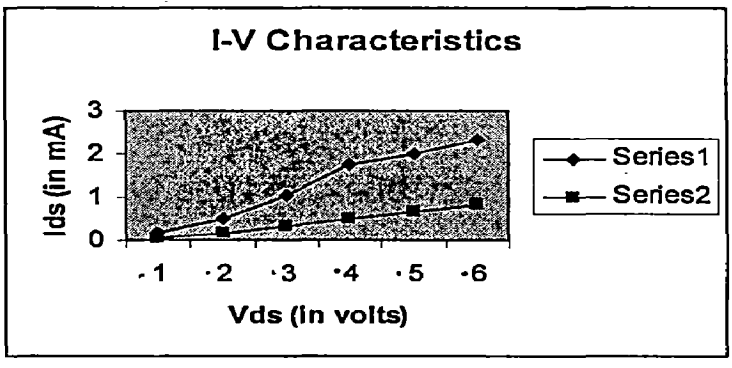


Figure 5.8(a): Graphs showing the comparison between ballistic and diffusive case

I-V Characteristics when both effects are considered

Series 1 for Ballistic case and Series 2 for Diffusive case, V_{GS}=0.40V

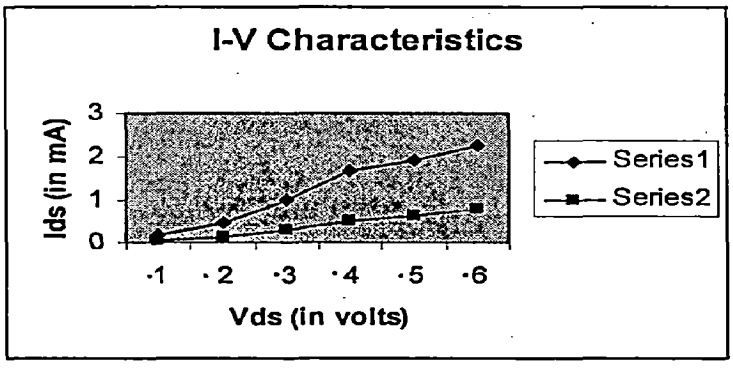


Figure 5.8(b): Graphs showing the comparison between ballistic and diffusive case

I-V Characteristics when only DIBL effect is considered

Series 1 for Ballistic case and Series 2 for Diffusive case, V_{GS}=0.40V

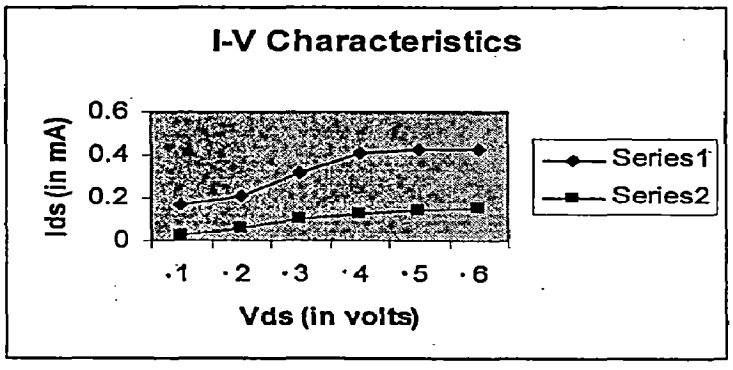


Figure 5.8 c: Graph showing comparison between ballistic and diffusive case for Vgs=0.40volts and when only Multi-Subband effect is considered Series 1 for Ballistic case and Series 2 for Diffusive case.

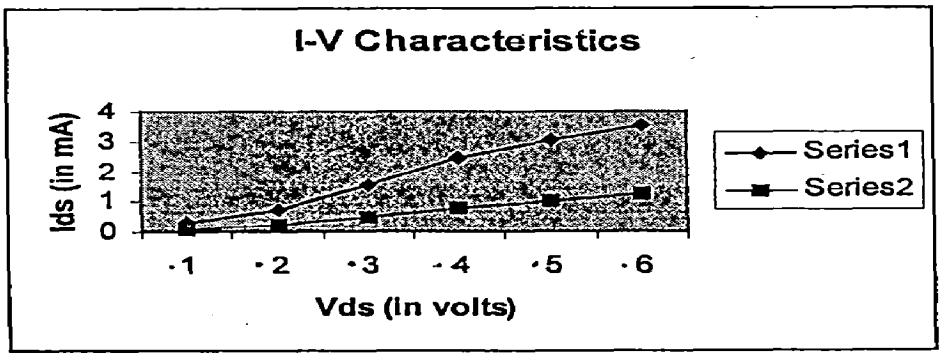


Figure 5.9(a): Graphs showing the comparison between Ballistic and Diffusive case when both the effects are considered at V_{GS}=0.45V

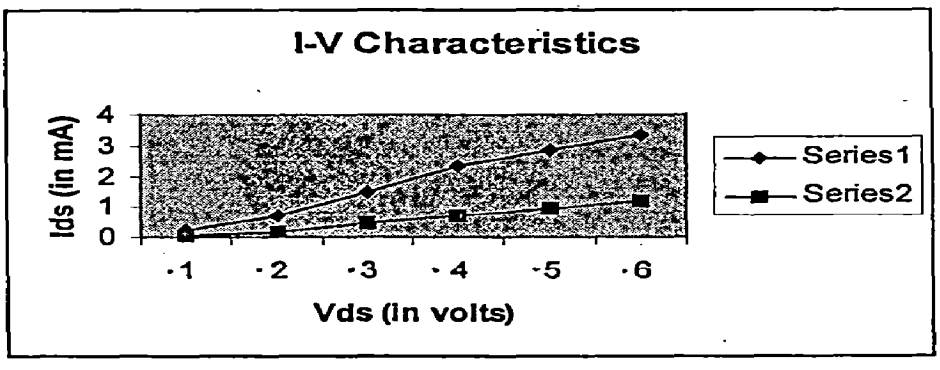


Figure 5.9(b): Graphs showing the comparison between Ballistic and Diffusive case when only DIBL effect is considered, at Vgs=0.45 volts.

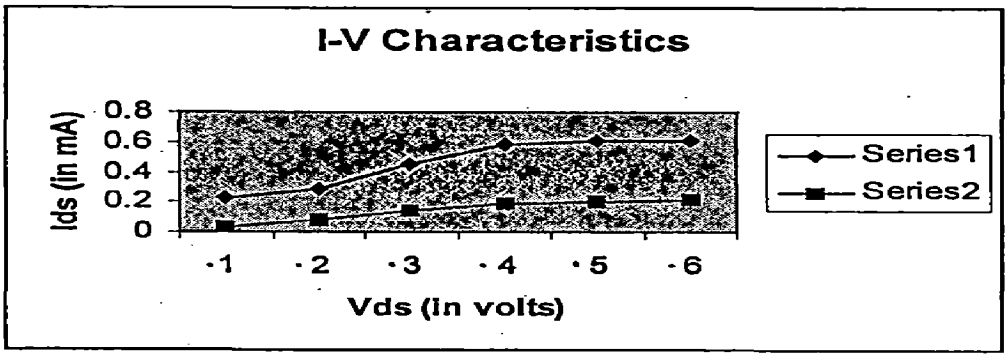


Figure 5.9 (c): Graph showing the change in drain current for both ballistic and diffusive case when only Multi-subband effect is considered with Vgs=0.45 volts.
Series 1 for Ballistic case
Series 2 for Diffusive case

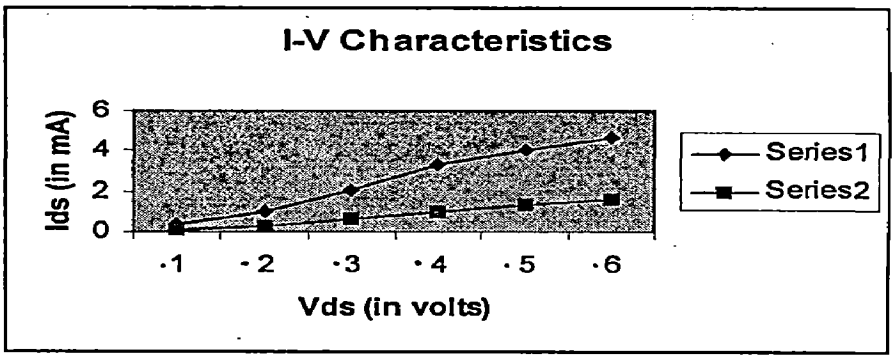


Figure 6.0(a): Graphs showing comparison between Ballistic and Diffusive case at Vgs=0.50 volts when both effects are considered

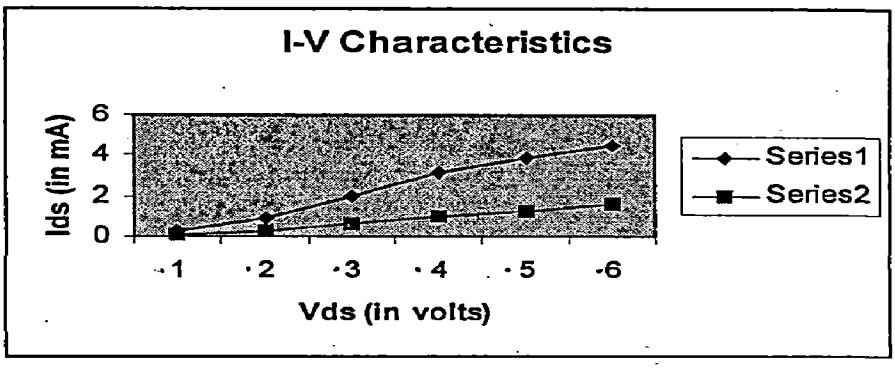


Figure 6.0(b): Graphs showing comparison between Ballistic and Diffusive case at Vgs=0.50 volts when only DIBL effect is considered
Series 1 for Ballistic case and Series 2 for Diffusive case

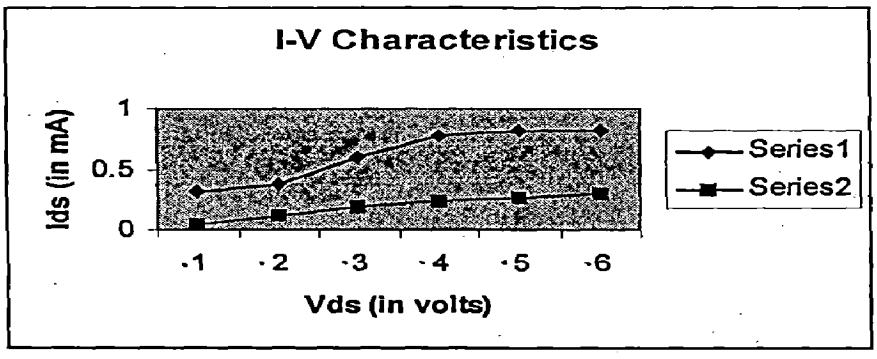


Figure 6.0 (c): Graph showing the comparison between Ballistic and Diffusive Case when only Multi-subband effect is considered at Vgs=0.50 volts Series 1 for Ballistic case and Series 2 for Diffusive case

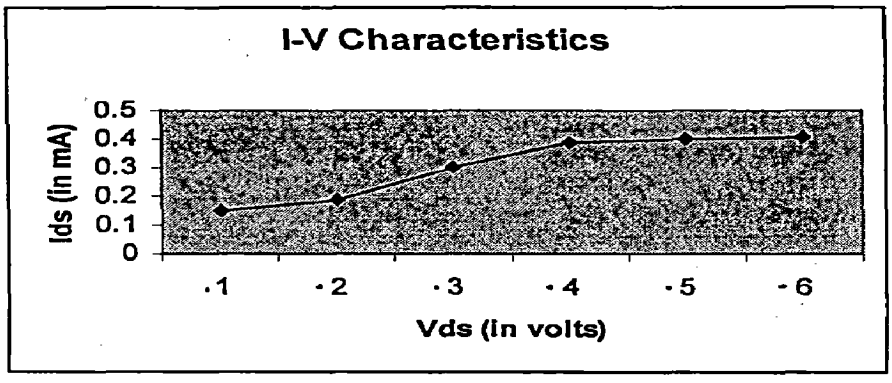


Figure 5.0(a): Graphs showing the variation of drain current with drain bias
When none of the effect is considered
When Vgs=0.40 volts ,

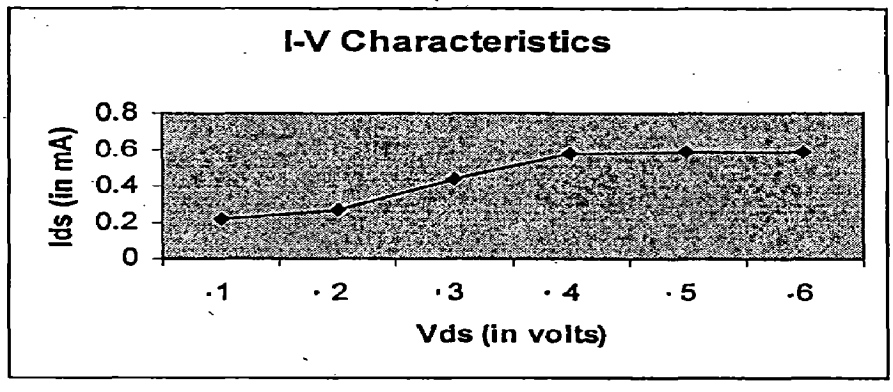


Figure 5.0(b): Graphs showing the variation of drain current with drain bias
When none of the effect is considered
When Vgs=0.45 volts

Dr. A.K. Saxena
Electronics & Computer Engg. Dept.

Please find enclosed herewith a copy of dissertation of M. Tech. (SSEM) of Ms. Shweta Sharma for consideration and evaluation at your end. The date of viva-voce will be informed you at later stage.

Encl: As above.

(Ishwar Singh)
Prof. and Head

Copy to: 1. Dr. S. Sarkar, Guide, Electronics & Computer Eng. Dept., IITR, along with a copy of dissertation. Guide
2. Dr. V.K. Tandon, Physics Dept., IITR, along with a copy of dissertation.
3. Dr. R. Nath, Coordinator, M. Tech (SSEM), Physics Deptt. along with a copy of dissertation.

Ishwar 6/7/04

(Ishwar Singh)
Prof. and Head

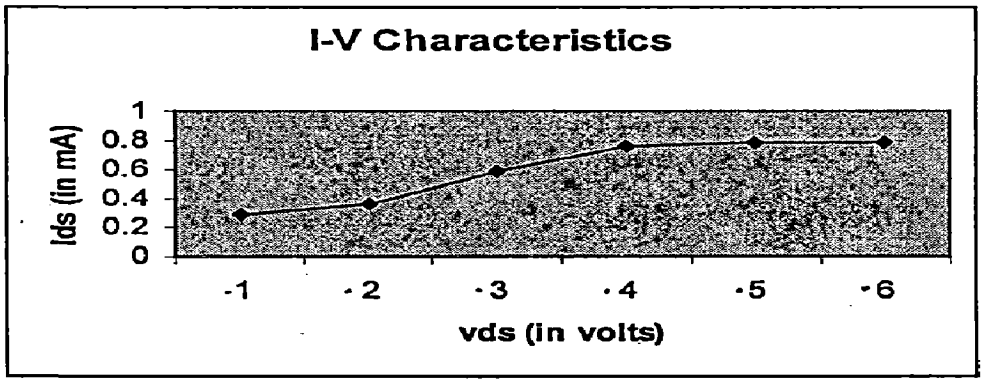


Figure 5.0(c): Graph showing the effect on drain current with varying drain bias when none of the effect is considered at Vgs=0.50 volts.

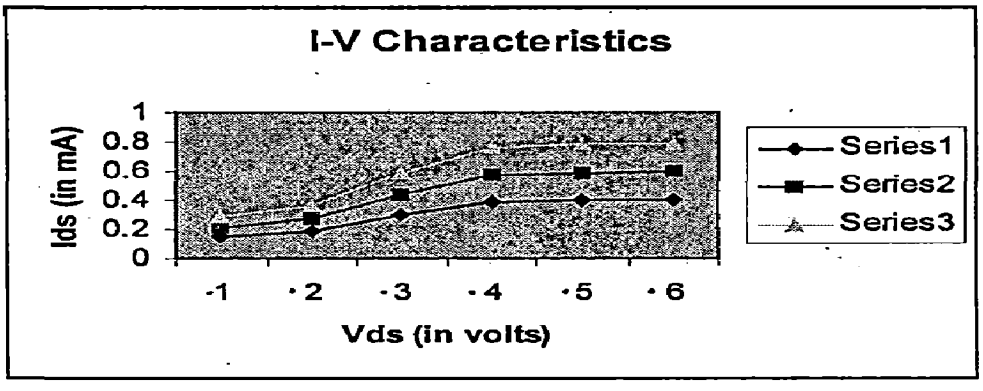


Figure 5.0(d): Graph showing the effect on drain current with varying Vds and Vgs. When none of the effect is considered. Series 1 for Vgs=0.40 volts, Series 2 for Vgs=0.45 volts and Series 3 for Vgs=0.50 volts.

For Ballistic Case

Chapter - 5

CONCLUSION

5.1 CONCLUSIONS:

From the developed drain current model it is seen that the multi sub band effect has significant effect on drain current. Because of this effect drain current increases as compared to when only one sub band occupation is considered. Also, Drain induced barrier lowering (DIBL) effect affects drain current drastically and because of it the drain current increases very much and it also increases in the saturation region. The I-V characteristics obtained on the basis of developed analytical model are compared with the simulated results available in the literature and it shows very good agreement with that. So, this suggests that the equations (A) and (B) have the potential for predicting device behavior.

5.2 RECOMMENDATIONS FOR FUTURE WORK:

Although the developed model has the potential to take into account the effects of multi sub band occupation and DIBL but for further development of this model, several additional factors have to be addressed. The factors include:

(i) *Effects of source and drain series resistance:* Since as we go on reducing the channel length source and drain series resistance no longer become negligible as compared to the channel resistance. So, for further improvement of current requires proper modeling of drain and source series resistance.

(ii) *Two-dimensional effect like punch-through:* Punch through is an important phenomenon that has to be taken into account when we deal with very short length transistors.

(iii) *Range of DIBL parameter:* In this work, the DIBL coefficient is defined only for saturation region so for gaining more physical insight into the device's operating principles it is necessary to define DIBL parameter for whole range i.e. from linear to saturation region.

Although, we have focused on a specific device, the DG MOSFET, this work is an example how flux method can be used to model nanotransistors more generally. New models of this class can provide a useful conceptual guide for device development as well as circuit models for new, unconventional transistors.

APPENDIX A

In the saturation region DIBL parameter is defined as:

$$\text{DIBL parameter} = d\ln(I_d)/dVds$$

In order to calculate the DIBL parameter the numerical simulation results given in [25] are used. From the numerical simulation results drain current is found, corresponding to drain biases. Then logarithms of these values are calculated. Then graphs are plotted between the $\ln(I_d)$ and drain source voltage Vds which are shown in figure (A) , (B) and (C). The slopes of these plots are taken as the DIBL parameter.

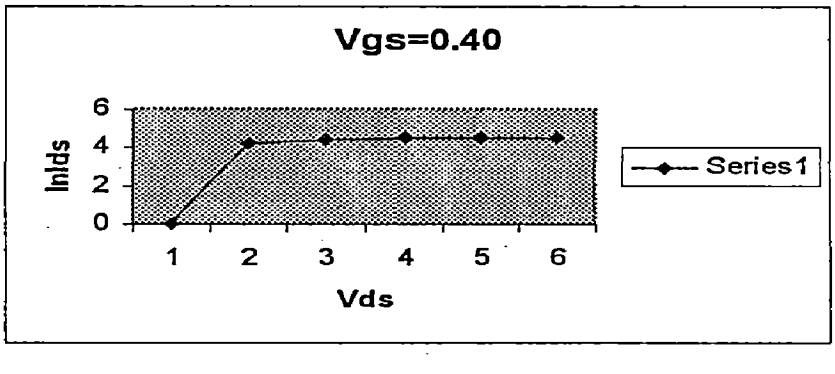


Figure (A)

DEPARTMENT OF PHYSICS
INDIAN INSTITUTE OF TECHNOLOGY
ROORKEE

NO: Phy/M. Tech (SSEM)/ 348

Dated: July 21, 2004

NOTICE

The M. Tech. (SSEM) Viva-Voce Examination of Ms. Shweta Sharma on his dissertation entitled "An Analytical Study of Double Gate MOSFET" will be held on Friday, the 23nd July, 2004 at 12.00 noon in the Seminar room. All are cordially invited to attend the same.

(S. Auluck)
Prof. and Officiating Head

Copy to: 1. A.R. (Acad.), UOR, Roorkee
2. The Examiner
3. Prof. S. Auluck, Chairman, DRC, Physics Deptt., IIT Roorkee
4. Dr. S. Sarkar, Guide, E&CE Deptt., IIT Roorkee
5. Dr. V.K. Tandon, Guide, Physics Deptt., IIT Roorkee
6. Dr. R. Nath, Coordinator, M. Tech (SSEM), Physics Deptt., IIT, Roorkee

(S. Auluck)
Prof. and Officiating Head

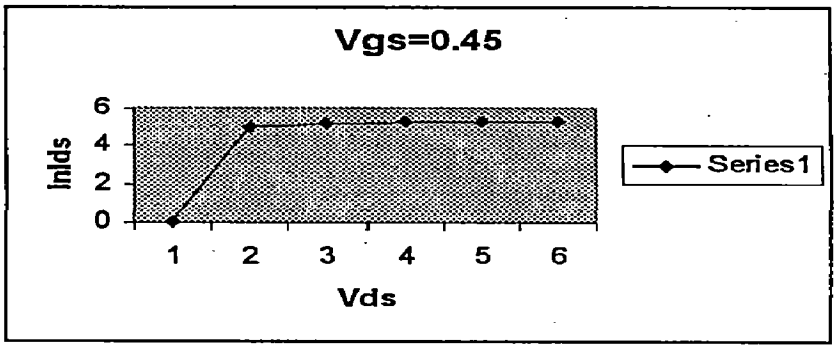


Figure (B)

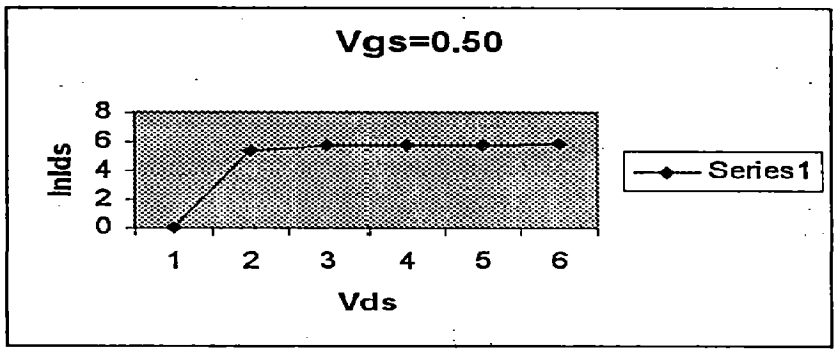


Figure (C)

APPENDIX B

k-Boltzman Constant

q- Electron charge

n_i- Intrinsic electron density, $1.45*10^{10}$ cm^{-3} at 300 K

t_{ox}- Gate oxide thickness

t_{Si}- Silicon film thickness

E_g- Silicon band gap, 1.12 eV at 300 K

I_D- Drain current

L_{eff}- Effective channel length

V_{DS}- Drain to source voltage

V_{GS}- Gate to source voltage

V_{th}- Threshold voltage

ΔV_{th}- Threshold voltage roll-off

ε_0- Dielectric constant of vaccum, $8.854*10^{-12}$ Fm^{-1}

ε_{Si}- Relative dielectric constant of Silicon, 11.9

ε_{ox} – Relative dielectric constant of Silicon dioxide, 3.9

Φ_B- Difference between Fermi level and Intrinsic level in Silicon

Φ_I- Work function of intrinsic Silicon, 4.71 eV at 300 K

χ – Electron affinity in Silicon, 4.05 eV

U_{DS} – Normalized Fermi Level

Ψ- Electrostatic potential referenced to fermi level

APPENDIX C

CALCULATIONS OF FERMI-DIRAC INTEGRALS:

Fermi-Dirac integrals of order half and order zero used in the present work can be calculated as in [32]-

$$\Im_{1/2}(\eta) = \left(\frac{4}{3}\right)\sqrt{\pi}\eta^{3/2}\left[1+\left(\frac{\pi^2}{8\eta^2}\right)-\left(\frac{7\pi^4}{640\eta^4}\right)\right] \quad \text{when } \eta>0$$

$$\Im_{1/2}(\eta) = e^{\eta} - \left(\frac{e^{2\eta}}{\sqrt{8}}\right)+\left(\frac{e^{3\eta}}{\sqrt{27}}\right) \qquad \text{when } \eta \leq 0$$

$$\Im_{0}(\eta) = \ln\left(1+e^{\eta}\right)$$

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