INFLUENCE OF HIGH FIELDS ON STANDBY POWER DISSIPATION OF CMOS GATES

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

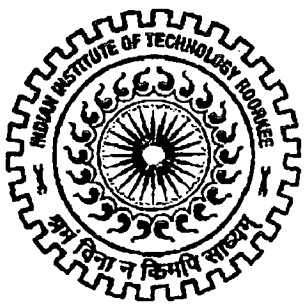
MASTER OF TECHNOLOGY

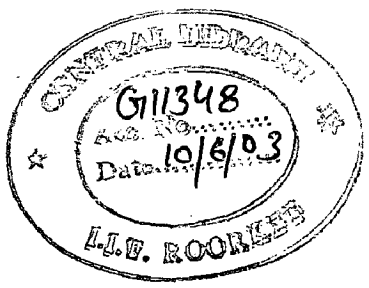
in

SOLID STATE ELECTRONIC MATERIALS

By

SANGHAMITRA GHOSH





DEPARTMENT OF PHYSICS
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE -247 667 (INDIA)
February, 2003

CANDIDATE'S DECLARATION

I hereby declare that the work which is being presented in this dissertation entitled " **INFLUENCE OF HIGH FIELDS ON STANDBY POWER DISSIPATION OF CMOS GATES** ", in partial fulfillment of the requirements for the award of the degree of **Master of Technology** in Solid State Electronic Materials, submitted in the Department of Physics, Indian Institute of Technology Roorkee, Roorkee, is an authentic record of my own work carried out during the period from June 2002 to February 2003, under the supervision of Prof. S. Sarkar, Department of Electronics and Computer Engineering and Prof. R. Nath, Department of Physics, Indian Institute of Technology Roorkee, Roorkee.

The matter embodied in this dissertation has not been submitted by me for the award of any other degree.

Date: 24.02.2003

Place: IIT Roorkee.

(Sanghamitra Ghosh)

CERTIFICATE

It is certified that the above statement made by the candidate is correct to the best of my knowledge and belief.

Date: 24.02.2003

Place: IIT Roorkee.

(Prof. S. Sarkar)

(Prof. R. Nath)

ABSTRACT

The main contribution to standby power dissipation comes from the subthreshold leakage current. Hence, it is mandatory to develop a holistic model which accounts for all important physical phenomena taking place in the subthreshold regime. These include drift-diffusion, thermionic emission, short channel effects and high field effects. The subthreshold model has been specifically modified to include the high field effect in subthreshold region i.e., impact ionization which ultimately leads to avalanche breakdown. The standby power dissipation of a CMOS circuit is calculated using the concept of dominant leakage states, input state probabilities and the model mentioned above. Finally, the effect of multiplication on the standby power dissipation of the circuit is studied with respect to the applied inputs.

ACKNOWLEDGEMENT

I wish to convey my deep regards to Prof. S. Sarkar, Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee, Roorkee, for his esteemed guidance and healthy initiative at all stages of this dissertation. I specially thank him for his patience and readiness to help at all times in the course of this work.

I express my sincere gratitude to Prof. R. Nath, Department of Physics, Indian Institute of Technology Roorkee, Roorkee for his direction, help and support.

My sincere acknowledgement to Prof. Ishwar Singh Tyagi, Head, Department of Physics, Indian Institute of Technology Roorkee, Roorkee for providing the necessary facilities to carry out this work.

I thank my friends for their kind cooperation and encouragement.

I owe it to the blessings of my parents that I have been able to complete this work in due time.

Date: 24.02.2003

(Sanghamitra Ghosh)

CONTENTS

CANDIDATE'S DECLARATION		i
ABSTRACT		ii
ACKNOWLEDGEMENTS		iii
CONTENTS		iv
LIST OF FIGURES		vi
LIST OF TABLES		viii
NOMENCLATURE		x
CHAPTER 1	INTRODUCTION	1
	1.1 Overview	1
	1.2 Objectives	2
	1.2.1 Statement of purpose	2
	1.2.2 Problem Statements	2
	1.3 Organization	3
CHAPTER 2	LITERATURE RIVIEW	4
CHAPTER 3	NMOS SUBTHRESHOLD CURRENT MODEL	9
	3.1 Long channel model	9
	3.2 Short channel effects	11
	3.2.1 Charge sharing	11
	3.2.2 Drain induced barrier lowering	14
	3.3 Drain current due to thermionic emission	19
	3.4 Conclusion	20

CHAPTER 4	EFFECTS OF HIGH FIELDS AND SCALING ON SUBTHRESHOLD CURRENT	21
	4.1 Impact ionization	21
	4.2 Scaling	25
CHAPTER 5	STANDBY POWER ESTIMATION OF A DIGITAL CIRCUIT	27
	5.1 Dominant leakage states	28
	5.2 Determination of state probabilities	31
	5.2.1 Correlation coefficients and state probabilities	32
	5.2.2 Observability	36
	5.2.3 Algorithm	37
	5.3 Standby power calculation for each dominant leakage state.	39
CHAPTER 6	RESULT AND DISSCUSSION	41
CHAPTER 7	CONCLUSION	62
REFERENCES		63
APPENDICES		
A	DEVICE PARAMETERS AND PHYSICAL CONSTANTS	A.1
B	NUMERICAL COMPUTATION OF NMOS DIBL COEFICIENT	B.1
C	GRAPHICAL DEDUCTION OF THRESHOLD VOLTAGE SHIFT	C.1
D	PROGRAMS	D.1

LIST OF FIGURES

Fig. No.	Figure Name	Page No.
3.1	NMOS energy and potential profile at the interface.	13
3.2	Schematic illustration of depletion zones in an NMOS.	13
3.3	Distribution of induced charge in an NMOS.	16
3.4	Simplified model of the drain bias induced charge.	16
5.1a	Circuit diagram of a NAND3 gate.	29
5.1b	Euler Graph of a NAND3 gate.	29
5.2	Fig. 5.2: V_T drop across the ON NMOS in an NMOS inverter.	31
5.3	Extension of the rules in Table 5.2 to calculate $C_{l,m}$ for two AND gates.	35
6.1	Variation of subthreshold ideality factor with scale factor.	41
6.2	Variation of DIBL coefficient with drain source voltage for different scale factors.	42
6.3	Power dissipation (P_{Leak}, P_{dd}, P_{te}) versus drain source voltage.	43
6.4	Power dissipation versus drain-source voltage with and without threshold voltage shift correction.	44
6.5	Power dissipation versus scale factor.	45
6.6	Multiplication factor versus scale factor.	46
6.7	Power dissipation (P_M) versus drain source voltage.	47
6.8	Power dissipation (P_M) versus scale factor.	47
6.9	Gate level diagram of a two input multiplexer.	48

Fig. No.	Figure Name	Page No.
6.10	CMOS circuit diagram of a two input multiplexer.	49
6.11	Gate level diagram of a D flip flop.	51
6.12	CMOS circuit diagram of a D flip flop.	52
C.1	Variation of threshold voltage shift versus gate source voltage.	C.2
C.2	Variation of m_1 versus drain source voltage.	C.3
C.3	Variation of C_1 versus drain source voltage.	C.3
C.4	Variation of threshold voltage shift with drain source voltage.	C.4
C.5	Variation of m_2 with gate source voltage.	C.4

LIST OF TABLES

Table No.	Name	Page No.
5.1	Rules for calculating the node signal probability through the correlation coefficients.	33
5.2	Rules for determining the output correlation coefficients of a pair of signals given the input correlation coefficients and the input probabilities.	34
5.3	Rules for calculating the node observabilities through the correlation coefficients.	37
6.1	Leakage power calculations for a NAND3 circuit with substrate doping of value 5×10^{22} m^{-3}.	54
6.2	Leakage power calculations for a NAND3 circuit with substrate doping of value 10^{23} m^{-3}.	55
6.3a	Input states for DC connected components of a two input multiplexer.	56
6.3b	Transistors contributing to leakage in each DC connected component of a two input multiplexer.	56
6.4	Power dissipation of dominant leakage states for each DC connected component of a two input multiplexer.	57
6.5a	Node probabilities corresponding to each DC connected component of a two input multiplexer.	58
6.5b	Output observabilities probabilities corresponding to each DC connected component of a two input multiplexer.	58
6.5c	State probabilities corresponding to each DC connected component of a two input multiplexer.	58
6.6	Standby power dissipation of a two input multiplexer without considering the effect of multiplication.	59

Table No.	Name	Page No.
6.7	Standby power dissipation of a two input multiplexer considering the effect of multiplication.	59
6.8	Input states of a two input multiplexer in descending order of power dissipation.	60
6.9	Average standby power dissipation of a two input multiplexer.	60
6.10a	Input states for DC connected components of a D flip flop.	61
6.10b	Transistors contributing to leakage in each DC connected component of a D flip flop.	61
6.11	Total and average standby power dissipation of a D flip flop.	61

NOMENCLATURE

Symbol	Description
α_n	Electron ionization coefficient
β_p	Hole ionization coefficient
α_B	Electron ionization coefficient at E_B
β_B	Hole ionization coefficient at E_B
α_M	Electron ionization coefficient at E_M
β_M	Hole ionization coefficient at E_M
δ	Effective channel thickness
ε_{ox}	Oxide permittivity
ε_s	Substrate permittivity
η	Subthreshold ideality factor
$\phi_b = V_{th} \log (N_a/ n_i)$	Position of Fermi level relative to the intrinsic level of the doped substrate
ϕ_{ms}	Metal to semiconductor work function difference
μ_n	Effective mobility
χ	Ratio of depletion charges induced in the channel to the total additional depletion charge
σ	Drain induced barrier lowering coefficient
$\psi(x, y)$	Two dimensicnal potential of the channel w.r.t source
ψ_{ST}^{o}	Interface potential in the channel region at threshold

ψ_s^o	Constant interface potential in the absence of drain bias below threshold
$\psi_s(x)$	Interface potential at a position x in the channel on applying a drain bias
ψ_{sn}^o, ψ_{sp}^o	NMOS and PMOS interface potential below threshold
A	Richardson's constant
$C_{dep}(x)$	Channel depletion capacitance per unit area
$C_{ox} = \varepsilon_{ox} / t_{ox}$	Gate oxide capacitance
d_{dep}	Gate depletion width on application of a drain bias
$D_n = \mu_n V_{th}$	Electron diffusion coefficient
d_o	Gate depletion width in the absence of drain bias
E_B	Breakdown electric field
E_g	Band gap
E_M	Maximum electric field
E_{nM}, E_{pM}	Maximum electric field in NMOS and PMOS channel
E_s	Electric field at the Si-SiO_2 interface
F_x	Electric field component along the interface
F_y	Electric field component normal to the Si-SiO_2 interface
$F_y(o)$	Normal component of electric field component at the interface
I_d	Subthreshold drain current
I_{dd}	Subthreshold drift diffusion current
I_{dn}, I_{dp}	Electron and hole subthreshold drain current
I_{DS}	Total drain source current considering multiplication

I_{DSn}, I_{DSp}	NMOS and PMOS avalanche current
$I^{o}_{s\to d}$	Thermionic emission current from source to drain at equilibrium
$I^{o}_{d\to s}$	Thermionic emission current from drain to source at equilibrium
$I_{s\to d}$	Thermionic emission current from source to drain
$I_{d\to s}$	Thermionic emission current from drain to source
I_{te}	Net thermionic emission current
J_n	n-channel current density per unit area
K	Boltzman's constant
L	Length of Gate
M	Avalanche multiplication factor
M_n, M_p	Elecron and hole initiated multiplication
N_a	Substrate doing per unit volume
N_d	Source and drain contact doping per unit volume
n_i	Intrinsic carrier concentration per unit volume
$n = n(x)$	Electron density per unit area at position x

P_{Avg}	Average standby power dissipation
P_{dd}	Standby power dissipation due to I_{dd}
P_{Leak}	Standby power dissipation due to I_d
P_M	Standby power dissipation due to multiplication
P_{MAvg}	Average standby power dissipation due to multiplication
P_{MN}, P_{MP}	Total standby power dissipation due to multiplication in NMOS and PMOS
P_{te}	Standby power dissipation due to I_{te}
Q	Electron charge
Q_b	Bulk charge in the MOS channel
ΔQ	Total additional depletion charge
$\Delta q(x)$	Sheet charge distribution along the channel
ΔQ_1	Drain biased induced charge in the substrate
ΔQ_2	Drain biased induced charge at the gate
ΔQ_{ch}	Induced channel depletion charge
T	Temperature
t_{ox}	Gate Oxide thickness
$V = V(x)$	Positive contribution to the potential due to drain bias
$V_{bi} = V_{th} \log (N_a N_D / n_i^2)$	Built in voltage between the source contact and the substrate
V_{DD}	Supply voltage
V_{DS}	Applied drawn source voltage
V_{FB}	Flat band voltage
V_{GS}	Applied gate source voltage

V_{min}	Potential at the source-channel junction
V_T	Threshold voltage
ΔV_T	Threshold voltage shift
$V_{th} = KT/q$	Thermal voltage
V_{To}	Threshold voltage at zero drain vias
W	Width of Gate
W_{eq}	Equivalent junction width
W_{eqn}, W_{eqp}	Equivalent junction width for n^+p and p^+n-junction
x_d	Drain-channel depletion width
x_s	Source-channel depletion width

INTRODUCTION

1.1 Overview

For the last four decades, the semiconductor industry has been improving itself with rapid pace by betterment of its products. These have resulted principally from the industry's ability to continually follow Moore's Law i.e., exponentially scale down the minimum feature sizes of devices used to fabricate integrated circuits. As per the current scaling trend, the number of components per chip doubles every 18 months.

Standby power dissipation in a CMOS circuit occurs due to the existence of leakage currents in the NMOS and PMOS transistors even when they are not undergoing any switching event. Of the two leakage components, the subthreshold current is due to carrier diffusion between the drain and source of a MOS transistor in the weak inversion region of operation. A MOSFET is said to operate in the subthreshold region when the applied gate voltage is below the threshold voltage i.e., the conducting channel is weakly inverted. This region corresponds to the OFF state of the MOS device. But, there always exists some leakage current due to finite amount of charge at Si-SiO_2 interface. Another component, the reverse saturation current flows when the pn-junction between the drain and the bulk of a transistor is reverse biased. Since, junction leakage is two to three orders of magnitude smaller than the subthreshold component, it can be ignored for all practical purposes.

With decreasing feature sizes, the power supply voltage is also reduced. Hence, the threshold voltage of transistors is scaled down to maintain a constant switching speed. Since, the subthreshold leakage rises exponentially with decreasing threshold voltage, the leakage power dissipation in the standby mode increases significantly with scaling. Therefore, the contribution

of standby power dissipation to total average power dissipation increases with reduction in device dimensions.

As a MOS device is scaled down, the electric field in the subthreshold regime rises, leading to impact ionization. This finally causes avalanche breakdown. Therefore, the study of effect of impact ionization on CMOS circuits is important as high electric fields put a practical limit on the power handling capability of CMOS gates. So, the main objective of this work is to determine the standby power dissipation of a CMOS circuit, with and without the impact ionization consideration and compare the two results.

1.2 Objectives

1.2.1 Statement of Purpose

To study the influence of high fields on standby power dissipation of CMOS gates.

1.2.2 Problem Statements

a. To select an accurate subthreshold current model, its interpretation and complete mathematical analysis, for simulation purposes.
   - Calculation of subthreshold ideality factor (η) and its variation with scaling.
   - Calculation of threshold voltage shift/ DIBL coefficient (σ) and study of its behavior.
   - Determination of model parameters as a function of the scale factor.
   - Extension of the model to PMOS device.

b. To include the effect of high fields on this model and hence develop a modified current model.
   - Calculation of maximum electric field.
   - Calculation of multiplication factor.
   - Extension to a PMOS device.

c. To devise a method to calculate the standby power dissipation of a digital circuit using this model.

- Segregation of the circuit into DC-Connected Components (DCC).
- Calculation of Input State Propagation Probalilities for each DCC.
- Determination of Dominant Leakage States (DLS) for each DCC.
- Determination of standby power for each DLS using the model developed.
- Combining the results for different DCCs using state probabilities.

1.3 Organization

This report is divided into six chapters. The first chapter is introduces the reader to the problems of this dissertation. The remaining part of the dissertation is organized as follows:

Prior work carried out in context of this dissertation is discussed in chapter 2. In chapter 3, the NMOS subthreshold current model used for the purpose of this study is discussed. The effects of constant electric field scaling and impact ionization on the drain current are presented in chapter 3. In chapter 4, a method to estimate the standby or leakage power dissipation of a digital circuit is described. Chapter 5 presents the results. In chapter 6 the study is concluded.

LITERATURE REVIEW

Estimation of standby power dissipation is time-consuming and expensive because of repeated leakage current evaluation using non-linear simulation models in large digital circuits. Leakage current calculation is complicated due to highly nonlinear behavior of the MOS drain current with respect to the drain-source voltage in the subthreshold regime of operation.

The basic theory for subthreshold current of MOSFETs [1] works well for long channel devices and with minor adjustments, can even account for some short channel effects. However, as device dimensions continue to scale down drastically to submicron range and further, constraints on the drain current increase [2]. One of the most important short channel effects is the lowering of the energy barrier between the source and the channel known as Drain Induced Barrier Lowering or DIBL [3]. Experimental studies [4] confirmed that DIBL leads to threshold voltage shift in short channel MOSFETs. Many theoretical models have been developed for the subthreshold current. For example, the BSIM current model [5] takes the threshold voltage shift into consideration. But, being empirical in nature, it is not suitable for modeling deep submicron devices. Fjeldly and Shur proposed a completely analytical model for the subthreshold regime [6]. This model is based on the concept of charge sharing. The drain induced depletion charge in the channel is estimated using this concept and an expression for the distribution of charge along the channel is found by using two-dimensional Poisson's equation. It is possible to determine the DIBL and hence the threshold voltage shift using this distribution.

Two mechanisms, namely the phenomenon of drift-diffusion and thermionic emission determine the current in the MOS channel. The currents corresponding to both the

mechanisms depend on the Si-SiO_2 interface potential, which is a function of the threshold voltage shift among other parameters. The current limiting mechanism that leads to the highest impedance dominates the total channel current. This implies that the drain current is dominated by the smaller of the two.

With device scaling, electric field in the channel region increases. In the submicron regime, the field may rise to the order of 10^7 Vm^{-1} for a moderate drain voltage. Such a high field may bring about multiplication in the subthreshold regime. Multiplication factors must account for the different ionization rates in electron and holes. Analytical approximations for the multiplication factors due to holes and electrons in germanium and silicon one-sided abrupt junctions are available in Ref. [9]. This analysis is quite accurate. The approach followed is that of a uniform field equivalent junction. The actual depletion width of the drain junction is replaced by an equivalent width corresponding to an equivalent electric field with the same multiplication factor. The ratio of equivalent width to actual width is calculated for an abrupt junction using the condition that, the magnitude of multiplication factor tends to infinity just at the point of breakdown. Resulting expressions for multiplication factors are quite accurate and have zero error at the breakdown field, which is important when using it for high multiplications. Spirito [9] also discusses different cases corresponding to low multiplication levels (which depend on single ionization rate i.e., either electron ionization rate or hole ionization rate) and high multiplication levels.

Troutman [10] presents a model specifically developed for low level multiplication in MOSFETs and discusses the results of both theoretical and experimental analyses. At high multiplication levels, the ionization integral is a function of ionization rates of both electrons and holes. For example, in an NMOS channel when the electric field is high enough, the secondary holes can also gain enough energy to cause impact ionization. In the saturation

region, channel current consists of electrons that are thermally emitted over the potential barrier at the source. Since, electric field is maximum just beneath the drain, electrons are collected by the reverse biased drain junction. Some of the primary electrons can gain enough energy to cause impact ionization of an electron-hole pair. The secondary electrons with energy higher than the Si-SiO_2 energy barrier are injected into the gate oxide. The secondary holes thus collected at the drain are prevented from reaching the source by the built in potential and are collected at the substrate. Therefore, experimental values of multiplication factor in the saturation regime are determined by measuring channel and substrate currents.

Assumptions used in deriving the expression for multiplication in the saturation region are invalid in the subthreshold region. An approximation used in calculation of ionization integral is that the drain junction is a one-dimensional abrupt n^+p-junction. On application of drain-source voltage, electric field from source to drain reaches peak value in a linear fashion. Implicit in the above assumption is that only the lateral field or the field parallel to the channel current is important for determining subthreshold multiplication behavior. Such an approximation is not valid for saturation region where gate-source voltage plays an equally important part. In the subthreshold region, unlike saturation region, multiplication hardly depends on gate source voltage.

The model leads to reasonable agreement with experimental data for a long channel device in the range of low-level multiplication. Comparison with experimental results for variation of multiplication with drain source voltage when extended to higher multiplication levels for subthreshold regime, indicate a sharper breakdown than indicated by the model.

As the device thresholds are reduced to maintain performance in large circuits, the subthreshold current becomes significant due to the exponential relation between device

current and threshold voltage. This necessitates the need for developing accurate standby power estimation techniques.

Chen et al. [13] have developed a simple model for leakage estimation using the concept of transistor stacks. The subthreshold current of MOSFETs constituting the stack is modeled using the BSIM2 subthreshold current equation. Steady state leakage values are estimated as a function of the number of transistors that are turned off. Since, the subthreshold current flowing through each transistor in a series stack is the same, the current through each transistor is equated and solved for voltage across each transistor. These voltages are then used to determine the magnitude of current and finally the power dissipation. The standby power of a circuit for a given primary input state is calculated by simply summing the leakage power consumed by off transistors. The voltage across on transistors is assumed to be negligible due to small amounts of currents involved and they are treated as short circuit. This is one of the major disadvantages of this model leading to erroneous leakage estimation. Not all on transistors in the stack can be treated as a short circuit because of the threshold voltage drop across some of them.

Chen et al. [13] mainly focus on calculating the maximum leakage across all permutations of the unspecified inputs using genetic algorithm technique. However, a leakage model is meaningful only when the device has been idle for some time. A device becomes idle many times during the lifetime of its battery, each time with a random setting for the unspecified input signals. Furthermore, the state of a circuit's inputs is typically partially defined when the device enters standby mode. To obtain a reliable estimate of average battery lifetime, the average rather than the maximum circuit leakage must be calculated.

Sirichotiyakul et al. [14] describe a new approach for efficient estimation of standby power dissipation. The method proposed by them uses a variety of problem reduction techniques like dominant leakage states and state probabilities [15] combined with graph reduction techniques. The average standby power dissipation of a circuit is obtained from leakage of individual DC connected components. The notion of dominant leakage states is introduced for each DC connected component. A state with more than one off transistor in the V_{DD}-ground leakage path is far less leaky than a state with only one transistor off in the V_{DD}-ground path. The latter states are called dominant leakage states, which are usually very small compared to the number of all possible states. This eliminates the need to simulate all possible states for a DC connected component, saving simulation time. The leakage power of each dominant leakage state of a DC connected component is obtained from precharacterized tables of current values based on Newton-Raphson iterations. These iterated values are derived from a subthreshold current model similar to the BSIM2. The average leakage of a circuit for a particular primary input state is obtained from leakage of individual DC connected components and from their state probabilities. This method claims to achieve speedups of three to four orders of magnitude over exhaustive SPICE simulations while maintaining very good accuracy.

NMOS SUBTHRESHOLD CURRENT MODEL

The existing subthreshold current model as proposed by Fjeldly and Shur [6] is described below.

3.1 The long channel model

In the subthreshold region, the MOSFET behaves almost like a Bipolar Junction Transistor with the channel as a long base. The n^+ source acts as an emitter and the drain acts as the collector. Therefore, for a long channel device, most of the voltage applied at the drain will drop across the reverse biased n^+p junction, the longitudinal electric field component being much smaller than the component normal to the Si-SiO_2 interface. The current is then simply the sum of drift and diffusion terms as for a BJT. The current density is given by [6]

$$J_n = -q\left(-n\mu_n \frac{d\psi}{dx} + D_n \frac{dn}{dx}\right) = -qD_n\left(-\frac{n}{V_{th}}\frac{d\psi}{dx} + \frac{dn}{dx}\right) \qquad \ldots(3.1)$$

Multiplying (3.1), by the integrating factor $exp(-\psi/V_{th})$, and integrating from source ($x = 0$) to drain ($x = L$), gives

$$J_n = qD_n \frac{n(0)\exp\left(-\frac{\psi(0,y)}{V_{th}}\right) - n(L)\exp\left(-\frac{\psi(L,y)}{V_{th}}\right)}{\int_0^L \exp\left(-\frac{\psi(x,y)}{V_{th}}\right)dx} \qquad \ldots(3.2)$$

Implicit in (3.2), is the assumption that the current density is independent of position of carriers in the channel. Disregarding degeneracy, the source contact concentration $n(0)$ and the drain contact $n(L)$ are both equal, i.e., $N_d \neq N_a$. Conventionally, the source contact being the potential reference, $\psi(0, y) = 0$ and $\psi(L, y) = V_{DS}$.

The drift-diffusion current is then obtained by integrating (3.2) over the cross-section of the conducting channel,

$$I_{dd} = q N_d W \delta D_n \frac{\left[1 - \exp\left(-V_{DS}/V_{th}\right)\right]}{\int_0^L \exp\left(-\frac{\psi(x,y)}{V_{th}}\right) dx} \quad \ldots(3.3)$$

The effective channel thickness δ, normal to the Si-SiO_2 interface depends on the interface potential. At threshold, the interface potential in the channel is given by

$$\psi_{sT}^{o} = -V_{bi} + 2\phi_b \quad \ldots(3.4)$$

Below threshold, the interface potential can be expressed as

$$\psi_s^o = \psi_{sT}^o + \frac{V_{GT}}{\eta} = -V_{bi} + 2\phi_b + \frac{V_{GT}}{\eta} \quad \ldots(3.5)$$

where, the subthreshold ideality factor η [7] reflects division of gate voltage between the depletion layer capacitance and the gate oxide capacitance. The voltage, $V_{GT} = V_{GS}$-V_T. The threshold voltage V_T is given by

$$V_T = \phi_{ms} - \frac{Q_{ss}}{C_{ox}} - \frac{Q_b}{C_{ox}} + 2\phi_b = V_{FB} - \frac{Q_b}{C_{ox}} + 2\phi_b \quad \ldots(3.6)$$

where [2],

$$\phi_{ms} = -\frac{E_g}{2q} - \phi_b \quad \ldots(3.7)$$

Since, the electron density in the channel is exponentially dependant on the interface potential ψ_s^o, δ corresponds to the thickness of the channel with respect to the interface where the potential has decreased by V_{th} [1]. Therefore,

$$\delta = V_{th} / E_s \quad \ldots(3.8)$$

From Gauss's law,

$$E_s = -Q_b / \varepsilon_s \qquad \ldots(3.9)$$

where,

$$Q_b = -\sqrt{2q\varepsilon_s N_a(\psi_s^o + V_{bi})} \qquad \ldots(3.10)$$

Therefore,

$$\delta = V_{th}\sqrt{\frac{\varepsilon_s}{2qN_a(2\phi_b + V_{GT}/\eta)}} \qquad \ldots(3.11)$$

The above expression is valid when $-2\varphi_b < V_{GT}/\eta < 0$ i.e., in the weak inversion and depletion region.

3.2 Short channel effects

As the gate length of the MOS device is reduced, departures from long channel behavior take place due to two dimensionality of the electric field. The potential distribution now depends on both the transverse field due to the gate and the longitudinal field due to the drain bias. Therefore, the potential distribution becomes two-dimensional and GCA is no longer valid.

3.2.1 Charge sharing

At short gate lengths, the drain depletion region and the source depletion region may represent a considerable fraction of channel length. The source and drain depletion regions intrude into the channel even without bias and in effect take part of the channel charge otherwise controlled by the gate. Therefore, in the denominator of (3.3), the integral becomes very small in the junction depletion zones as the potential increases rapidly. Hence, one of the considerations of the short channel effect is to replace the limits of the integral from $0 \rightarrow L$ to $x_s \rightarrow L\text{-}x_d$.

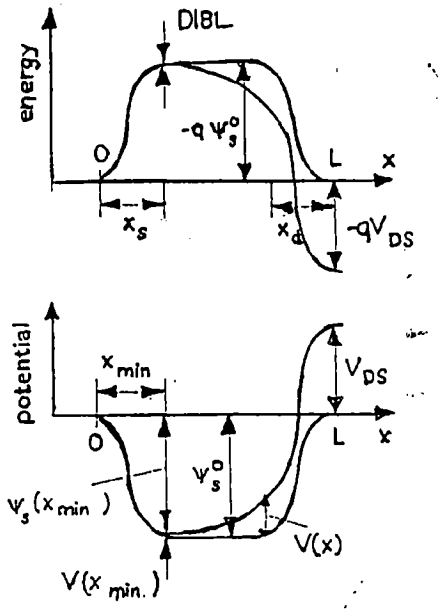


Fig. 3.1: Band diagram (top) and potential profile (bottom) at the semiconductor-insulator interface of an n-channel MOSFET. The symmetrical profiles correspond to V_{DS} = 0, and the asymmetrical profiles to V_{DS} > 0. The figure indicates the origin of DIBL. The symbols are defined in the text.

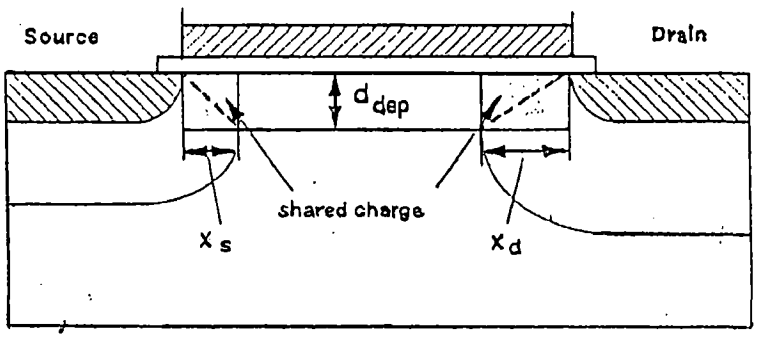


Fig. 3.2: Schematic illustration of the depletion zones associated with the source, drain and gate for an applied V_{DS}. The shaded areas near source and drain indicate the regions of charge sharing.

3.2.2 Drain induced barrier lowering (DIBL)

With increase in positive drain bias, the drain depletion zone can grow to the extent that it begins to interact with the source channel junction. This is responsible for two basic effects:

a. The drain bias induces a positive shift $V(x)$ in potential such that $V(0) = 0$ and $V(L) = V_{DS}$. Therefore,

$$\psi_s = \psi_s^o + V(x) \qquad \ldots(3.14)$$

The interface potential is now a function of x as shown in Fig. 3.1. At the source channel boundary, $V(x) = V(x_s) = V_{min}$. Therefore,

$$\psi_s(x_s) = \psi_s^o + V(x_s) \qquad \ldots(3.15)$$

The reduction in the potential at the source leads to a lowering of the interface energy barrier between the source and channel by $-qV_{min}$. As a result, the charge injection from the source to the channel increases.

b. With a large depletion region, the additional induced drain depletion charge is distributed non-uniformly from drain to source (Fig. 3.3). Using, the principle of charge sharing, the charges and their counter charges can be paired, such that, a fraction of the additional drain charge ΔQ_{ch} has its counter charge $-\Delta Q_{ch}$ on the gate electrode. The remaining charges and counter charges are between the drain and the substrate (ΔQ_1, $-\Delta Q_1$) and between drain and gate (ΔQ_2, $-\Delta Q_2$).

Both these effects can be taken care of by beginning with the Poisson's equation for the depletion region under the gate, away from source and drain depletion zones.

$$\frac{\partial F_x}{\partial x} + \frac{\partial F_y}{\partial y} = -\frac{qN_a}{\varepsilon_s} \qquad \ldots(3.16)$$

Integrating with respect to y from the Si-SiO_2 interface through the depletion region yields

$$\left\langle \frac{\partial F_x}{\partial x} \right\rangle d_{dep} - F_y(0) = -\frac{qN_a d_{dep}}{\varepsilon_s} \qquad \ldots(3.17)$$

From one dimensional theory,

$$d_{dep} \approx \sqrt{\frac{2\varepsilon_S}{qN_a}(\psi_s + V_{bi})} = d_o\sqrt{1+\frac{V(x)}{\psi_s^o + V_{bi}}} \qquad \ldots(3.18)$$

From the principle of continuity of electric field across a boundary,

$$F_y(0) = \frac{C_{ox}}{\varepsilon_s}(V_{GS} - V_{FB} - \psi_s - V_{bi}) \qquad \ldots(3.19)$$

Away from source and drain, $<\partial F/\partial x> = 0$ when $V_{DS} = 0$. Considering (3.17) with and without an applied drain bias and taking the difference,

$$\frac{\partial^2 V}{\partial x^2} d_{dep}(x) - \frac{C_{ox}}{\varepsilon_s} V(x) = \frac{qN_a}{\varepsilon_s}\left[d_{dep}(x) - d_o\right] \qquad \ldots(3.20)$$

Since, V(x) and its x-derivatives are small outside the drain depletion region, first order expansion of (3.20) in $V(x)$ yields

$$\frac{\partial^2 V}{\partial x^2} - \frac{V}{\lambda^2} = 0 \qquad \ldots(3.21)$$

where,

$$\lambda = d_o\left(1+\frac{\varepsilon_{ox} d_o}{\varepsilon_s t_{ox}}\right)^{-1/2} \qquad \ldots(3.22)$$

Without much error, it can be assumed that (3.21) is valid for $x<x_s$ also. Therefore, the boundary condition becomes $V(x = 0) = 0$.Using this Condition, the solution of (3.22) is

$$V(x) = V_o \sinh(x/\lambda) \qquad \ldots(3.23)$$

where, V_o is a constant to be determined.

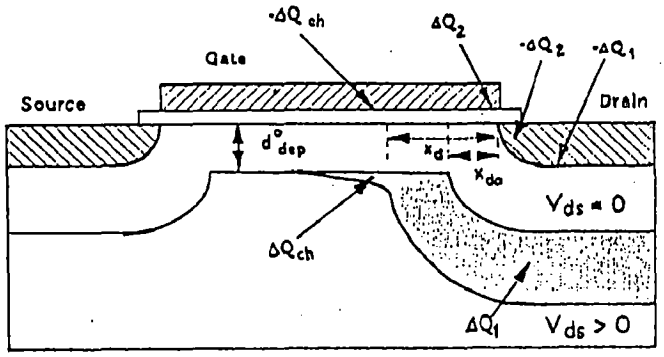


Fig. 3.3: Distribution of depletion charge induced by an applied drain-source bias, indicated by the shaded region ΔQ_{ch} is part of the induced charge located in the central channel region and has its counter charge on the gate electrode.

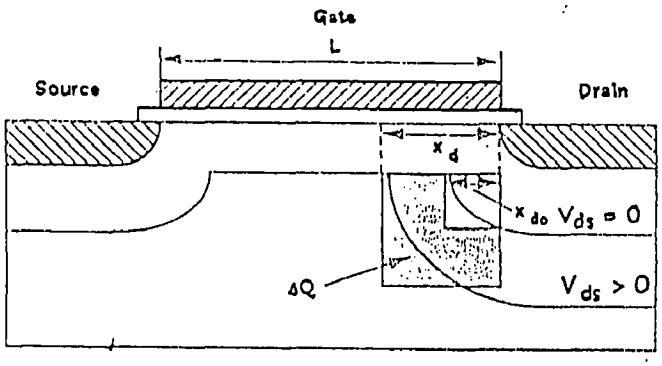


Fig. 3.4: Simplified model of the drain-bias induced charge ΔQ in the substrate under the gate. The induced channel charge ΔQ_{ch} is taken to be a fraction of ΔQ, according to the principle of charge sharing.

The charge distribution at any point x in the channel is given by

$$\Delta q(x) = C_{dep} V(x) \approx \frac{V_o \varepsilon_s}{d_o} \sinh(x/\lambda) \qquad \ldots(3.24)$$

where,

$C_{dep}(x)$ has been expanded to lowest order in $V(x)$. Assuming that, in the range $x_s \le x \le L\text{-}x_d$, the integral of $\Delta q(x)$ is ΔQ_{ch}, V_o is obtained as

$$V_o = \frac{\Delta Q_{ch} d_o}{W \lambda \varepsilon_s} \left[\cosh\left(\frac{L - x_d}{\lambda}\right) - \cosh\left(\frac{x_s}{\lambda}\right) \right]^{-1} \qquad \ldots(3.25)$$

The shaded region in Fig. 3.4 gives an approximate estimate of the additional depletion charge under the gate electrode.

$$\Delta Q \approx qWN_a (x_d^2 - x_{do}^2) \qquad \ldots(3.26)$$

Let ΔQ_{ch} be some fraction χ of the charge ΔQ. With $x_{do} \approx x_s$,

$$\Delta Q_{ch} \approx \chi qWN_a (x_d^2 - x_{do}^2) \approx 2\chi W \varepsilon_s V_{DS} \qquad \ldots(3.27)$$

From (3.24) and (3.26), V_o is obtained as

$$V_o \approx \frac{2\chi V_{DS} d_o}{\lambda} \left[\cosh\left(\frac{L - x_d}{\lambda}\right) - \cosh\left(\frac{x_s}{\lambda}\right) \right] \qquad \ldots(3.28)$$

Therefore, the potential corresponding to the barrier lowering at the source channel boundary is

$$V(x_s) \approx \frac{2\chi V_{DS} d_o \sinh(x_s/\lambda)}{\lambda} \left[\cosh\left(\frac{L - x_d}{\lambda}\right) - \cosh\left(\frac{x_s}{\lambda}\right) \right]^{-1} \qquad \ldots(3.29)$$

As a consequence of barrier lowering, there is a drain-bias-induced shift in the threshold voltage. From (3.5), the threshold voltage shift can be taken as,

$$\Delta V_T = -\eta V(x_s) \qquad \ldots(3.30)$$

Combining (3.29) and (3.30) gives,

$$\Delta V_T = -\eta V(x_s) = -\sigma V_{DS} \qquad \ldots(3.31)$$

where, σ is the drain induced barrier lowering coefficient.

The main improvisation on the model proposed by Fjeldly and Shur is the numerical computation of the subthreshold ideality factor and the DIBL coefficient. Although, the model given in [6] is purely analytical, both η and σ are calculated numerically with the constraint that they both satisfy $L >= x_s + x_d$ and equation (3.29). This is done to account for the effect of these parameters on the model current equation. The method used for numerical computation is bisection method because of surety of convergence of this particular numerical method. The detailed calculation of η and σ are given in appendix C.

Considering the above mentioned short channel effects, the integrand in the denominator of (3) can now be evaluated. Since, the integrand is exponentially dependent on the potential, the hyperbolic sine function in (3.23) can be expanded to first order in x, i.e.,

$$\begin{aligned} &\int_{x_S}^{L-x_d} \exp(-\frac{\psi(x)}{V_{th}})dx \approx \exp(-\frac{\psi_S^o}{V_{th}}) \int_{x_S}^{L-x_d} \exp\left(-\frac{V_o x}{V_{th}\lambda}\right)dx \\ &\approx \frac{\lambda V_{th}}{V_o}\exp\left(-\frac{\psi_S^o + V(x_S)}{V_{th}}\right)\left\{1-\exp\left(-\frac{V_o(L-x_s-x_d)}{V_{th}\lambda}\right)\right\} \end{aligned} \qquad \ldots(3.32)$$

Therefore, the drift diffusion current is obtained as

$$I_{dd} = \frac{qN_d W\delta D_n V_o}{\lambda V_{th}} \frac{\exp\left((\psi_S^o + V(x_S))/V_{th}\right)\left[1-\exp(-V_{DS}/V_{th})\right]}{1-\exp(-V_o(L-x_s-x_d)/V_{th}\lambda)} \qquad \ldots(3.33)$$

3.3 Drain Current due to thermionic emission

The net drain current due to thermionic emission is zero at zero drain-source bias. Therefore, the equilibrium thermionic emission current from source to drain, $I^{o}_{s\to d}$, and from drain to source, $I^{o}_{d\to s}$, are given by

$$I^{o}_{s\to d} = I_{d\to s}{}^{o} = I_o \exp(\frac{\psi^{o}_{s}}{V_{th}}) \qquad \ldots(3.34)$$

and

$$I_o = W\delta AT^2 \qquad \ldots(3.35)$$

where A is the Richardson's constant. When a finite voltage is applied to the drain, the phenomenon of DIBL also contributes to the current. Thus,

$$I_{s\to d} = I_o \exp(\frac{\psi_s(x_s)}{V_{th}}) = I_o \exp(\frac{\psi^{o}_{s} + V(x_s)}{V_{th}}) \qquad \ldots(3.36)$$

$$I_{d\to s} = I_{s\to d} \exp(-\frac{V_{DS}}{V_{th}}) \qquad \ldots(3.37)$$

The net thermionic emission current under a drain-source bias from (3.36) and (3.37) is

$$I_{te} = I_{s\to d} - I_{d\to s} = I_o \exp(\frac{\psi^{o}_{s} + V(x_s)}{V_{th}})[1 - \exp(-\frac{V_{DS}}{V_{th}})] \qquad \ldots(3.38)$$

It is observed that the mechanisms of drift-diffusion and thermionic emission act predominantly in a serial fashion. The drain current will be limited by the one, which corresponds to the highest impedance. Therefore, the total drain current can be written as a combination of (3.33) and (3.38) as

$$I_d \approx \left[\frac{1}{I_{dd}} + \frac{1}{I_{te}}\right]^{-1} \qquad \ldots(3.39)$$

As can be seen from the above expression, the current limiting mechanism at small gate lengths is thermionic emission, whereas drift-diffusion dominates at larger gate lengths. Consequently, the standby power dissipation is given by

$$P_{Leak} = I_d V_{DS} \qquad \ldots(3.40)$$

3.4 Conclusion

The expressions for NMOS drain current and leakage power dissipation ignoring impact ionization are given by (3.39) and (3.40). Further analysis presented in this dissertation is based on these equations. The model equations for PMOS have been obtained as well through similar analysis. Therefore, PMOS modeling is not being described here.

EFFECTS OF HIGH FIELDS AND SCALING ON SUBTHRESHOLD CURRENT

The model of Fjeldly and Shur [6] ignores the effects of very high fields in the MOS channel. This is a good approximation for long channel and above submicron devices. As the channel length is reduced, electric field in the channel increases. One of the important high field effects is impact ionization. For large drain voltages, impact ionization can become a deciding factor for drain current and hence, leakage power dissipation.

4.1 Impact ionization

When a semiconductor is subjected to an increasing electric field, a point is reached where the carrier velocities approach their saturation values. Any further increase in electric field leads to an increase in their average kinetic energies. At fields of the order of 10^7 Vm^{-1}, significant numbers of carriers acquire energies higher than the band gap. These primary hot carriers collide with the lattice atoms to generate secondary electron hole pairs (EHPs). This process continues resulting in carrier multiplication and is known as the avalanche process.

In connection with the secondary EHP generation, the ionization coefficient (α for electrons and β for holes) is defined as number of EHPs produced per carrier on moving a unit distance along the electric field. For the given MOS device, the electric field is highest just below the Si-SiO_2 interface. The drain current in NMOS due to electron multiplication is given by [8]

$$I_{DS} = M_n I_{dn} \qquad \ldots(4.1a)$$

Similarly, drain current in PMOS due to hole multiplication is given by

$$I_{DS} = M_p I_{dp} \qquad \ldots(4.1b)$$

The ionization integral, is a measure of number of secondary EHPs generated per electron or hole.

For electron initiated multiplication, ionization integral is given by

$$1-\frac{1}{M_n}=\int_o^{E_M}\alpha_n \exp\left(-k_n\int_o^{E}(\alpha_n-\beta_p)\,dE'\right)dE \qquad \ldots(4.2a)$$

For hole initiated multiplication, ionization integral is given by

$$1-\frac{1}{M_p}=\int_o^{E_M}\beta_p \exp\left(-k_p\int_E^{E_M}(\beta_p-\alpha_n)\,dE'\right)dE \qquad \ldots(4.2b)$$

where,

$$\alpha_n = A_n \exp(^{-b_1}/_{E_M}) \qquad \ldots(4.3)$$

$$\beta_p = B_p \exp(^{-b_2}/_{E_M}) \qquad \ldots(4.4)$$

$$k_n=\frac{\varepsilon_s}{N_a} \qquad \ldots(4.5a)$$

and

$$k_p=\frac{\varepsilon_s}{N_d} \qquad \ldots(4.5b)$$

Considering the drain as an one dimensional abrupt junction, the actual depletion width, say W, can be replaced by an equivalent one, W_{eq}, with the same multiplication of the actual junction such that [9]

For an n^+p-junction,

$$1-\frac{1}{M_n}=\frac{\alpha_M}{\beta_M-\alpha_M}\left[\exp\left((\beta_M-\alpha_M)W_{eqn}(E_M)\right)-1\right] \qquad \ldots(4.6a)$$

For an p^+n-junction,

$$1-\frac{1}{M_p}=\frac{\beta_M}{\alpha_M-\beta_M}\left[\exp\left((\alpha_M-\beta_M)W_{eqp}(E_M)\right)-1\right] \quad \ldots(4.6b)$$

where,

$$W_{eqn}(E_M)=m_nW_n=m_nk_nE_M \quad \ldots(4.7a)$$

and

$$W_{eqp}(E_M)=m_pW_p=m_pk_pE_M \quad \ldots(4.7b)$$

m_n and m_p are proportionality factors less than 1.

The multiplication factor is now a function of peak electric field through the equivalent junction width and carrier ionization coefficients as can be seen from equations (4.3), (4.4) and (4.7).

The breakdown field E_B, is that critical value of electric field, above which carrier multiplication by impact ionization sets in. If the electric field increases any further on account of increase in the drain-source voltage, the drain looses control of the current because of avalanche breakdown. The typical value of breakdown field for silicon is about 3 $\times 10^7$ Vm^{-1}. For $E_M >> E_B$, $M \rightarrow \infty$ and hence, $1\text{-}1/M \rightarrow 1$. Therefore, for $E_M \geq E_B$, m_n and m_p can be approximated as

$$m_{nB}=\frac{\ln(\alpha_B/\beta_B)}{\alpha_B-\beta_B}\frac{1}{k_nE_B} \quad \ldots(4.8a)$$

$$m_{pB}=\frac{\ln(\alpha_B/\beta_B)}{\alpha_B-\beta_B}\frac{1}{k_pE_B} \quad \ldots(4.8b)$$

At breakdown,

$$m_n=m_{nB}(E_M/E_B) \quad \ldots(4.9a)$$

$$m_p=m_{pB}(E_M/E_B) \quad \ldots(4.9b)$$

Using, (4.9a) in (4.6a), the multiplication factor for electrons is obtained as

$$M_n = 1/\left[1-\alpha_M/(\beta_M-\alpha_M)\left(\exp(m_{nB}E_M/E_B)-1\right)\right] \quad \ldots(4.10a)$$

Using, (4.9b) in (4.6b), the multiplication factor for holes is obtained as

$$M_p = 1/\left[1-\beta_M/(\alpha_M-\beta_M)\left(\exp(m_{pB}E_M/E_B)-1\right)\right] \quad \ldots(4.10b)$$

The maximum field depends on the drain source voltage as well as the gate source voltage through the following relation [10], [11]

$$E_{nM} = \sqrt{\frac{2qN_a}{\varepsilon_s}\left(V_{DS}-b_n\phi_{bn}+V_{bin}\right)} \quad \ldots(4.11a)$$

$$E_{pM} = \sqrt{\frac{2qN_d}{\varepsilon_s}\left(V_{SD}+b_p\phi_{bp}-V_{bip}\right)} \quad \ldots(4.11b)$$

where,

$$b_n = \left|\frac{\psi_{sn}^o}{\phi_{bn}}\right| \quad \ldots(4.12a)$$

$$b_p = \left|\frac{\psi_{sp}^o}{\phi_{bp}}\right| \quad \ldots(4.12b)$$

The NMOS interface potential below threshold, ψ_{sn}^o is given by equation (3.5) of chapter 3. The PMOS interface potential, ψ_{sp}^o can be obtained similarly.

For the subthreshold region, $1< b <2$. Therefore, (4.11) can be written as

$$E_{nM} = \sqrt{\frac{2qN_a}{\varepsilon_s}\left(V_{DS}-\psi_{sn}^o+V_{bin}\right)} \quad \ldots(4.13a)$$

$$E_{pM} = \sqrt{\frac{2qN_d}{\varepsilon_s}\left(V_{SD}+\psi_{sp}^o-V_{bip}\right)} \quad \ldots(4.13b)$$

Equation (4.10) describes the impact ionization model for electron as well as hole initiated multiplication. A complete subthreshold impact ionization current model can now be obtained from (4.1). The NMOS drain current for this model is

$$I_{DSn} = \frac{I_{dn}}{\left(1-\alpha_M /(\beta_M - \alpha_M)\left(\exp(m_{nB}E_M / E_B)-1\right)\right)} \quad \ldots(4.14a)$$

The PMOS drain current can be written as

$$I_{DSp} = \frac{I_{dp}}{\left(1-\beta_M /(\alpha_M - \beta_M)\left(\exp(m_{pB}E_M / E_B)-1\right)\right)} \quad \ldots(4.14b)$$

Consequently, the leakage power dissipation for an NMOS is given by

$$P_{MN} = I_{DSn}V_{DS} \quad \ldots(4.15a)$$

Similarly, the PMOS leakage power dissipation is given by

$$P_{MP} = I_{DSp}V_{SD} \quad \ldots(4.15b)$$

It can be concluded from equation (4.13a) and (4.13b) that, interface potential and built-in voltage being small quantities compared to bias voltage, the peak electric field is dominated by the bias voltage. This leads to high multiplication factors (4.10) for slight increase in the applied voltage finally affecting P_{MN} and P_{MP}.

4.2 Scaling

A long geometry device is reduced to a small geometry device by scaling it down. According to the constant electric field scaling model, the scaling rule [12] is

$$V_{sf} = sV \quad \ldots(4.16a)$$

$$x_{sf} = sx \quad \ldots(4.16b)$$

For NMOS,

$$N_{asf} = \frac{N_a}{s} \qquad \ldots(4.16c)$$

For PMOS,

$$N_{dsf} = \frac{N_d}{s} \qquad \ldots(4.16d)$$

where the scale factor, $s \leq 1$.

This implies that N_{asf} and N_{dsf} increase with scaling leading to higher electric fields in smaller MOS devices (refer to equations 4.13a and 4.13b). Therefore, power dissipation as may be obtained from equations 4.15a and 4.15b is now an increasing function of scaling. The dependence of power dissipation on scaling is through drain current. The increase in power dissipation is expected to be sharp for small values of scale factors.

STANDBY POWER ESTIMATION OF A DIGITAL CIRCUIT

A novel approach for accurate and efficient calculation of standby power dissipation is given by Sirichotiyakul et al. [14]. This is done, by introducing the concepts of Dominant Leakage States and state probabilities combined with graph reduction techniques. This method claims to achieve speedups of three to four orders of magnitude over exhaustive SPICE simulations while maintaining very good accuracy. Therefore, the method proposed in [14] is used in conjunction with the subthreshold impact ionization model developed in previous chapters to determine circuit leakage.

Simulation complexity is overcome through a series of techniques mentioned below.

- Segregation of the circuit into DC-Connected Components (DCC).

This eliminates the need to simulate the entire network, instead simulating only one DCC at a time, thus reducing complexity.

- Calculation of State Probalilities for each DCC.

State probabilities are calculated using primary input probabilities.

- Determination of Dominant Leakage States (DLS) for each DCC.

This implies that for each DCC, only a small subset instead of all possible 2^N states are evaluated for leakage. Here, N is the number of primary inputs.

- Determination of standby power for each DLS using the model developed.

Each state in the dominant leakage set of a DCC is simulated using the subthreshold impact ionization model.

- Combining the results for different DCCs using state probabilities.

5.1 Dominant Leakage States (DLS)

It is known that leakage of a gate is significantly less in some states than in others. A state with more than one transistor OFF in a path from V_{DD} to GND is far less leaky than a state with only one transistor OFF in any V_{DD}-GND path. The latter states are called Dominant Leakage States (DLS). The set of DLSs is usually very small compared to the set of all possible states. The key idea is to ignore the leakage of insignificant or nondominant states in the average leakage calculation without loosing significant accuracy. For example, for a two input NAND gate, the set of DLSs are D={01, 10, 11}, i.e. the total number of DLS are three. Whereas, the number of DLS in a three input NAND are four and in four input NAND, only five. Considering only these states, the average leakage is, at the most, only about 5 % less than the exact average. Such accuracy is obtained by simulating only three out of eight possible states for a NAND3 gate. This tradeoff becomes even more attractive for DCCs with a large number of inputs.

Stepwise procedure to obtain DLS

a. Draw the Euler graph for each DCC. Let G(V, E) be an Euler graph representing a DCC in the circuit, such that each $v \in V$ represents a node in the DCC and each $e \in E$ represents a transistor in the DCC whose drain and source nodes are the end points of e. Since, G represents a DCC, it has only one connected component. Also $|V| > 1$, as there are at least two nodes, V_{DD} and GND.

For example, a NAND3 gate can be represented as

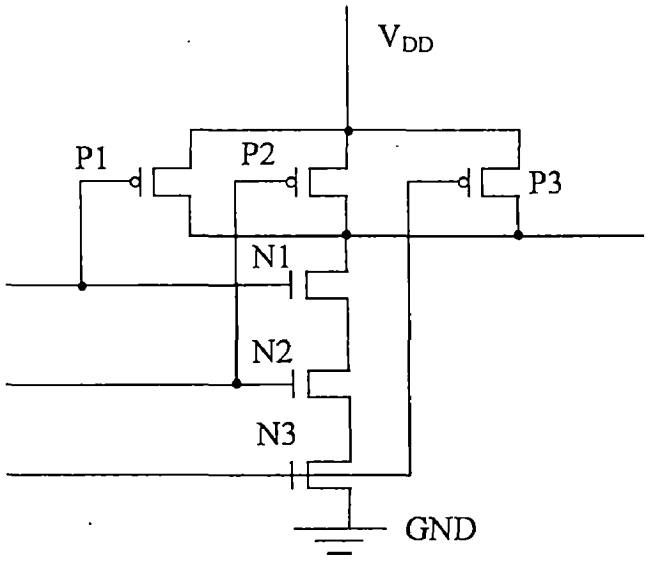


Fig. 5.1a: A NAND3 gate.

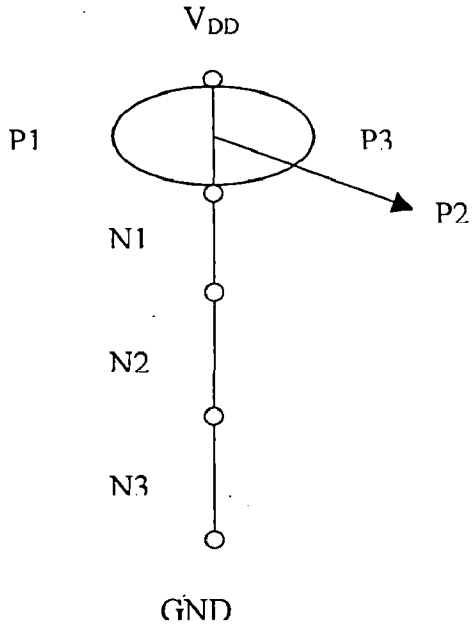


Fig. 5.1b: Euler Graph of a NAND3 gate.

A disconnecting set of edges in a connected graph G is any set of edges in G whose removal results in more than one connected component. If $F \subseteq E(G)$ is a disconnecting set, G(V, E-F) has more than one component. For example, for Fig. 5.1, {P1, P2, P3}, {N1}, {N2}, {N3}, {N1, N2}, {N2, N3}, {N1, N3}, {N1, N2, N3} are all disconnecting sets.

A cutset of G is defined as a minimal disconnecting set of G. Since it is minimal, a cutset always leaves a graph with exactly two components. Given a non empty set $S \subset V(G)$, [S, S'] denotes a cutset of G, the set of edges each having one end point in S and another in S'. For example, for Fig. 5.1b, {P1, P2, P3}, {N1}, {N2}, {N3} are all cutsets.

V_{DD} is always in S.

b. Determine the set of OFF transistors for each DCC for a particular input state. Let this set be called OFF(b). Let B be the set of all possible Boolean states for a gate's inputs such that

b∈B. An edge is called an OFF edge if its corresponding transistor is OFF in a given state. It is imperative that OFF(b) is a disconnecting set for G such that V_{DD} and GND lie in different components of G(V, E-OFF(b)). Otherwise, there will be a short circuit in b.

c. Determine the subset of transistors out of these OFF ones, which contribute to leakage. Let this set be called LEAK (b) i.e., LEAK(b) is a set of transistors that contribute to subthreshold leakage in state b. It is clear that LEAK(b) $\subseteq$ OFF(b) and that the end points of each edge of LEAK(b) are in different components of G(V, E-OFF(b)). If both the drain and source nodes of a transistor are in the same component of G(V, E-OFF(b)), then there is a conducting path between them consisting of other transistors of the component. Such a transistor will not contribute to subthreshold leakage. LEAK(b) is also a disconnecting set of G.

d. Check if LEAK (b) is a minimal set. A state b is said to be a Dominant Leakage State if LEAK (b) is minimal i.e., if there exists no other state a∈B such that LEAK(a)⊂ LEAK(b). If b is a DLS, LEAK(b) is a dominant-leakage set. This will happen for those input states where a single transistor in a series stack is OFF or all the transistors connected in parallel are OFF.

By above definition, a dominant leakage set is a minimal disconnecting set of G, and is hence, a cutset [S, S'] of G, such that V_{DD} is in S and GND is in S'. That is, when b is a DLS, G(V, E-LEAK(b)) has exactly two components, with V_{DD} and GND in different components. Vice versa, a cutset is qualified as a dominant leakage set only if 1) removing its edges partitions V_{DD} and GND into different partitions and 2) all of its edges can be logically OFF at the same time.

Therefore, {P1, P2, P3}, {N1}, {N2} and {N3} are dominant leakage sets for the input states {111}, {011}, {101} and {110} respectively. Hence, these input states are called Dominant Leakage States for the NAND3 gate.

For each DLS, there are two types of ON transistors, which contribute to leakage. If in a transistor stack, two transistors are in series such that the ON transistor is connected to V_{DD} and the OFF transistor is connected to GND, there is a V_T drop across the ON transistor as shown in Fig. 5.2.

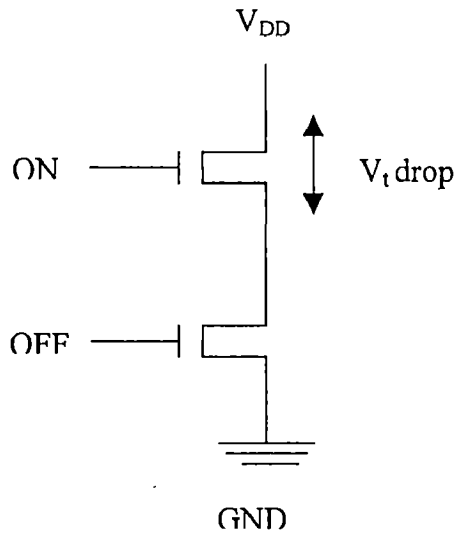


Fig. 5.2: V_T drop across the ON NMOS in an NMOS inverter.

On the other hand, if a transistor is of native type, there will be no V_t drop across the transistor when it is ON i.e., its source and drain nodes will be at equal potentials. In Fig. 5.1, for the input state {110}, there is a potential drop of V_t across N2 whereas there is practically no voltage drop across N1 and {P1, P2, P3}. Therefore, the voltage drop across the leaking transistor N3 is now V_{DD}-V_t. Since, the subthreshold current is a non-linear function of the voltage drop, the leakage power dissipation decreases significantly.

5.2 Determination of State Probabilities

Ercolani et al. [15] describe a procedure for propagating the probabilities of primary inputs to all internal and primary output signals while accounting for the first order spatial

correlation between signals. The procedure uses correlation between every pair of signals and hence is called Correlation Coefficient Method (CCM). The coefficients are propagated along with the probabilities. This procedure is applied to calculate the probabilities and correlation coefficients of all signals in the circuit and thereby calculate the state probabilities of the DCCs.

Notations and definitions [15]:

a. The quantity $p(j)$ is the signal probability of node j, namely, the probability that a randomly selected vector sets j to 1. Considering the possible interaction between different nodes, $p(j/i)$ is the probability of node j being 1 conditioned by node i being 1.

b. $B(j)$ is the probability that a randomly selected vector propagates the value on j to at least one of circuit primary inputs.

c. $B1(j)$ ($B0(j)$) is the probability that a randomly chosen vector among all those controlling j at 1(0) allows j to be observed at primary outputs.

d. $d1(j)$ ($d0(j)$) is the probability that a randomly selected vector detects j stuck at 1 or 0.

e. $d1(j/f=x)$ ($d0(j/f=x)$) is the detection probability of node j stuck at 1(0) conditioned by node f being at the logic value x.

5.2.1 Correlation Coefficients and Signal Probabilities

The correlation coefficient method explicitly accounts for the effects of statistical correlation between signals.

From probability theory, given two events A and B, the probability $P(AB)$ of $AB = A \cap B$ is given by $P(AB)=P(A/B)P(B)$,where $P(A/B)$ represents the probability of A given B.

In terms of correlation coefficients $C_{A,B}$, defined by the equation $P(AB)=P(A)P(B)C_{A,B}$. Hence,

$$C_{A,B} = \frac{P(AB)}{P(A)P(B)} = \frac{P(A/B)}{P(A)} = \frac{P(B/A)}{P(B)} \quad \ldots(5.1)$$

If A and B are independent events,

$$P(AB)=P(A)P(B) \quad \ldots(5.2)$$

Thus, $C_{A,B}=1$.

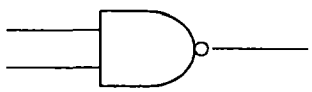
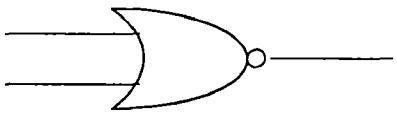
In a combinational network, an event is a node at 1; hence $P(A) = P(j = 1) = p(j)$ and

$$C_{i,j} = C_{j,i} = \frac{p(ij)}{p(i)p(j)} = \frac{p(i/j)}{p(i)} = \frac{p(j/i)}{p(j)} \quad \ldots(5.3)$$

$$p(i/j) = p(i)C_{i,j} \quad \ldots(5.4)$$

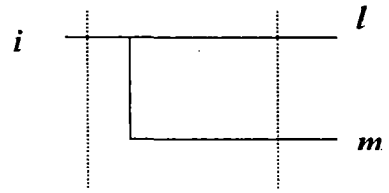
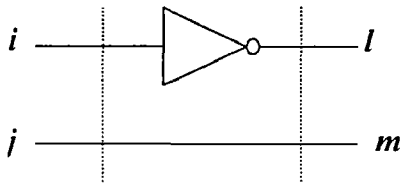
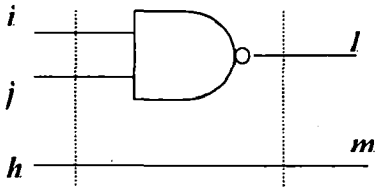
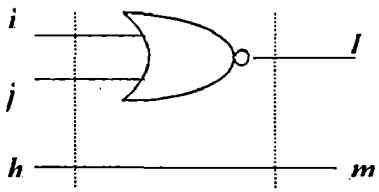
Given a gate with two inputs (i, j), the probability $p(l)$ at the output l can be calculated by means of p(i), p(j) and their correlation coefficient C_{ij} as shown in Table. 5.1.

Table 5.1 Rules for calculating the node signal probability through the correlation coefficients.

	$p(l) = 1 - p(i)p(j)C_{i,j}$ $0 \le p(l) \le 1$ $0 \le C_{i,j} \le \frac{1}{p(i)p(j)}$
	$p(l) = 1 - p(i) - p(j) + p(i)p(j)C_{i,j}$ $0 \le p(l) \le 1$ $\frac{p(i)+p(j)-1}{p(i)p(j)} \le C_{i,j} \le \frac{p(i)+p(j)}{p(i)p(j)}$

The correlation coefficients can be derived analytically by means of the set of basic rules given in Table. 5.2.

Table 5. 2. Rules for determining the output correlation coefficients of a pair of signals given the input correlation coefficients and the input probabilities.

Primary Inputs	Signals are assumed to be independent: $p(i/j) = p(i), p(j/i) = p(j)$ $C_{i,j} = 1$
	$i \equiv l \equiv m \Rightarrow p(l) = p(m) = p(i)$ $p(l/m) = 1$ $p(l)C_{l,m} = 1$ $C_{l,m} = \frac{1}{p(i)}$
	$i \equiv \bar{i} \Rightarrow p(l) = 1 - p(i)$ $p(l/m) = 1 - p(i/j)$ $p(l)C_{l,m} = 1 - p(i)C_{i,j}$ $C_{l,m} = \frac{1 - p(i)C_{i,j}}{1 - p(i)}$
	$l \equiv \overline{i \cap j} \Rightarrow p(l) = 1 - p(i)p(j)C_{i,j}$ $p(l/m) = 1 - p(i/h)p(j/h)C_{i,j}$ $p(l)C_{l,m} = 1 - p(i)p(j)C_{i,h}C_{j,h}C_{i,j}$ $C_{l,m} = \frac{1 - p(i)p(j)C_{i,h}C_{j,h}C_{i,j}}{1 - p(i)p(j)C_{i,j}}$
	$l \equiv \overline{i \cup j} \Rightarrow p(l) = 1 - p(i) - p(j) + p(i)p(j)C_{i,j}$ $p(l/m) = 1 - p(i/h) - p(j/h) + p(i/h)p(j/h)C_{i,j}$ $p(l)C_{l,m} = 1 - p(i)C_{i,h} - p(j)C_{j,h} + p(i)p(j)C_{i,h}C_{j,h}C_{i,}$ $C_{l,m} = \frac{1 - p(i)C_{i,h} - p(j)C_{j,h} + p(i)p(j)C_{i,h}C_{j,h}C_{i,j}}{1 - p(i) - p(j) + p(i)p(j)C_{i,j}}$

In Table 5.2, an approximation has been introduced while calculating the correlation coefficients in the last two cases. The correlation of two signals to a third is neglected i.e., the effect of higher order conditional probabilities are not taken into account. To verify this approximation, exhaustive simulations were made on several circuits by Ercolani et al. [15]. It was found that the simulated values considering higher order conditional probabilities and those calculated by means of above equations are comparable even at gates presenting signal reconvergencies.

Because of this approximation, the calculated coefficients lead to gate output probabilities outside the 0-1 interval. To avoid this, the correlation coefficients are limited within the bounds given in Table 5.1.

By using the rules of Table 5.2, it is possible to compute the correlation coefficients between any two signals at the output of a circuit block. Consider, for example the two NAND gates on the left hand side of Fig. 5.3.

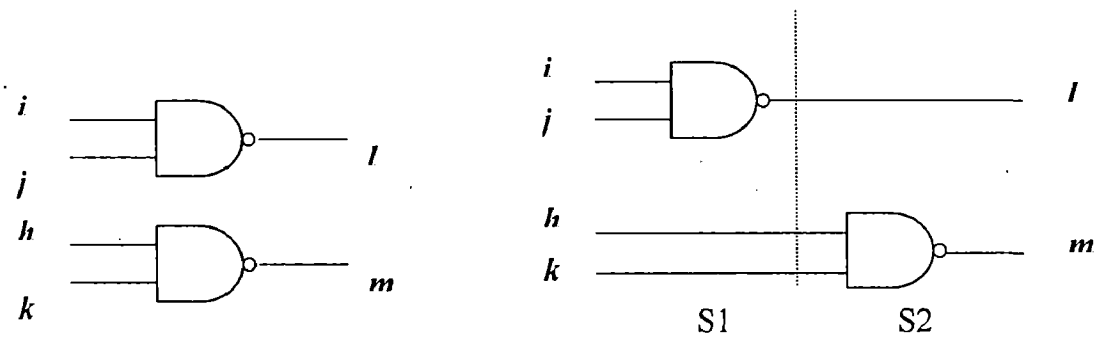


Fig. 5. 3. An example of extension of the rules in Table 5.2 to calculate $C_{l,m}$ for two AND gates.

By splitting the circuit as shown on the right hand side, and applying rules in Table 5.2 to S1, $C_{l,h}$ and C_{lk} are calculated. Then, $C_{l,m}$ is computed by applying the same rule to S2. The

rules given here are only for two input gates, but can be easily extended to the multiple-input case by simply considering a multiple input gate as a cascade of two input elementary devices.

The above method can be used only for combinational circuits. Sequential circuits or in circuits with feedbacks, the nodes with feedbacks are assigned initial values for signal probabilities and correlation coefficients. The procedure mentioned above is then applied on the whole circuit in an iterative loop until a particular accuracy for the updated values is reached.

5.2.2 Observability

For each signal j, the conditional observability is given by $B1(j)$ and $B0(j)$. To illustrate the rules for their computation, a NAND gate with inputs (i, j) and output l is considered as an example. Then,

$B1(i)$ = Prob (observe (l) & $j = 1/\ i = 0$) ...(5.5a)

$B0(i)$ = Prob (observe (l) & $j = 1/\ i = 1$) ...(5.5b)

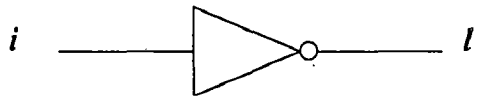
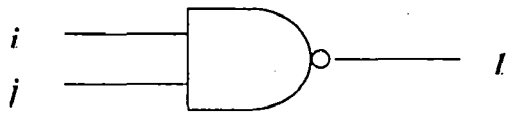
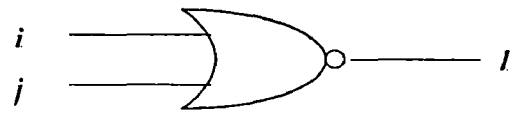
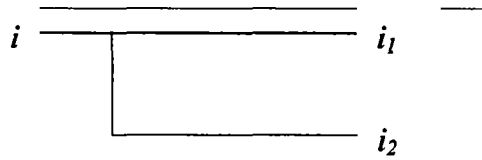
It is assumed for simplicity, that the observability of the gate output l, is independent of the value of its inputs (i, j). Introducing the correlation coefficients,

$$B1(i) = B0(l)p(j)\frac{1 - p(i)C_{i,j}}{1 - p(i)} \qquad \text{...(5.6a)}$$

$$B0(i) = B1(l)p(j)C_{i,j} \qquad \text{...(5.6b)}$$

This assumption is correct as long as the observability of l does not depend on signals statistically correlated to i or j. Table 5.3 summarizes the rules used to calculate the observability at output (1/0) of a gate. As can be easily verified, the rules for calculating $B1$ for an NAND gate and $B0$ for an NOR gate include the equivalence conditions.

Table 5.3 Rules for calculating the node observabilities through the correlation coefficients.

	$B1(i) = B0(l)$ $B0(i) = B1(l)$
	$B1(i) = B0(l)p(j)\dfrac{1-p(i)C_{i,j}}{1-p(i)}$ $B0(i) = B1(l)p(j)C_{i,j}$
	$B1(i) = B0(l)(1-p(j)\dfrac{1-p(i)-p(j)+p(i)p(j)C_{i,j}}{1-p(i)})$ $B0(i) = B1(l)(1-p(j)C_{i,j})$
	$B1(i) = 1-(1-B1(i_1))(1-B1(i_2))$ $B0(i) = 1-(1-B0(i_1))(1-B0(i_2))$

5.2.3 The Algorithm

The Correlation Coefficient Method (CCM) for a combinational circuit splits the calculation of state probabilities into two phases. A first step is used to compute signal probabilities by means of rules of Tables 5.1 and 5.2, successively applied proceeding from primary inputs to outputs. Then from the rules of Table 5.3, backtracking is performed to derive node observabilities. Finally, the state probability is obtained by multiplying the corresponding signal probability and observability.

The pseudocode for the algorithm is

ccm( )

```
{
for (each primary input j )
{/* initialize primary input values*/
        p(j) = 0.5;
        for (each primary input i ≠ j)
        {C_ij = 1;}
}
for (each level in the network, from the inputs)
{/*forward step, for signal probabilities and correlation coefficients */
        for (each node j of level)
        {
        p(j) = SignalProbability(level); /* from rules of Table 4.1*/
        for (each node i of level, i ≠ j )
        {
        C_ij = CorrelationCoefficients(level); /* from rules of Table 4.2 */
                }
        }
}
for (each primary output j)
{/* initialize output observabilities */
B0(j) = B1(j) = 1;
}
```

```
for (each level in the network, from the outputs)
{/* backtracking, for observability computation */
        for (each node j of that level)
        {
        B0(j)= ObservabilityAtZero(level); /* from rules of Table 4.3*/
        B1(j)= ObsevabilityAtOne(level);   /* from rules of Table 4.3*/
        }
}
for (each node j)
{/* calculate the state probabilities */
        d0(j)=p(j)B1(j);
        d1(j)=(1-p(j))B0(j);
        }
}
```

To save computation time it is useful to recognize during circuit compilation all the couples of independent signals and the gates not involved in fan-out reconvergencies.

5.3 Standby Power calculation for each DLS

To determine the standby power dissipation for a DLS, the gate-source voltage (V_{GS}) and the drain-source voltage (V_{DS}) for each leaking transistor must be calculated. It is observed that either a single OFF transistor in series or all the OFF transistors connected in parallel between two nodes contribute to leakage in a particular Dominant Leakage State for a DCC. The potential drop across a native ON transistor is zero whereas the potential drop across a non-native one is V_T. Therefore, both V_{DS} and V_{GS} are functions of the threshold voltage V_T,

which in turn is a function of the threshold voltage shift (ΔV_T). Hence, ΔV_T must be determined correctly for different scale factors. For this purpose, ΔV_T is plotted against V_{GS} for varying V_{DS} using the subthreshold model described in chapter 2 and the equation, which best fits the curve is considered. In case, the plots are linear in nature,

$$\Delta V_T = m_1(V_{DS})\, V_{GS} + C_1 \qquad \ldots(5.7)$$

where, both m_1 and C_1 are functions of V_{DS}. From plots of m_1 versus V_{DS} and C_1 versus V_{DS}, equations for m_1 and C_1 in terms of V_{DS} are determined and substituted back in (5.7).

Similarly, ΔV_T is plotted against V_{DS} for different V_{GS} and a linear fit is considered such that

$$\Delta V_T = m_2(V_{GS})\, V_{DS} + C_2 \qquad \ldots(5.8)$$

It can be safely assumed that C_2 is zero and m_2 is a function of V_{GS}. From plots of m_2 versus V_{GS}, equations for m_2 in terms of V_{GS} is determined and substituted back in (5.8). Equations (5.7) and (5.8) are then added to obtain an empirical relation of ΔV_T in terms of V_{GS} and V_{DS}, which are functions of ΔV_T. The value of ΔV_T can now be obtained for a particular supply voltage by solving the empirical relation so developed and used directly in the subthreshold impact ionization model to determine leakage power dissipation.

RESULT AND DISCUSSION

DIBL is one of the most important short-channel phenomena in the subthreshold regime, which leads to threshold voltage shift, ΔV_T. A method of calculating ΔV_T is given in appendix-B. All calculations have been carried out using data given in appendix-A. Calculations based on this method predict non-linear increase in magnitude of ΔV_T with V_{DS}. This behavior is more in concurrence with the experimental results [4] as compared to [6] which predicts linear rise of ΔV_T with V_{DS}. Such a difference arises because ΔV_T has been calculated numerically here whereas [6] describes an analytical model. The numerical calculation also takes care of the dependence of V_{DS} on the subthreshold ideality factor (η), gate depletion capacitance and source-channel junction depletion width instead of just the drain-channel junction depletion width as in [6]. The subthreshold ideality factor represents the subthreshold slope. The subthreshold ideality factor decreases with scaling as can be seen from Fig. 6. 1.

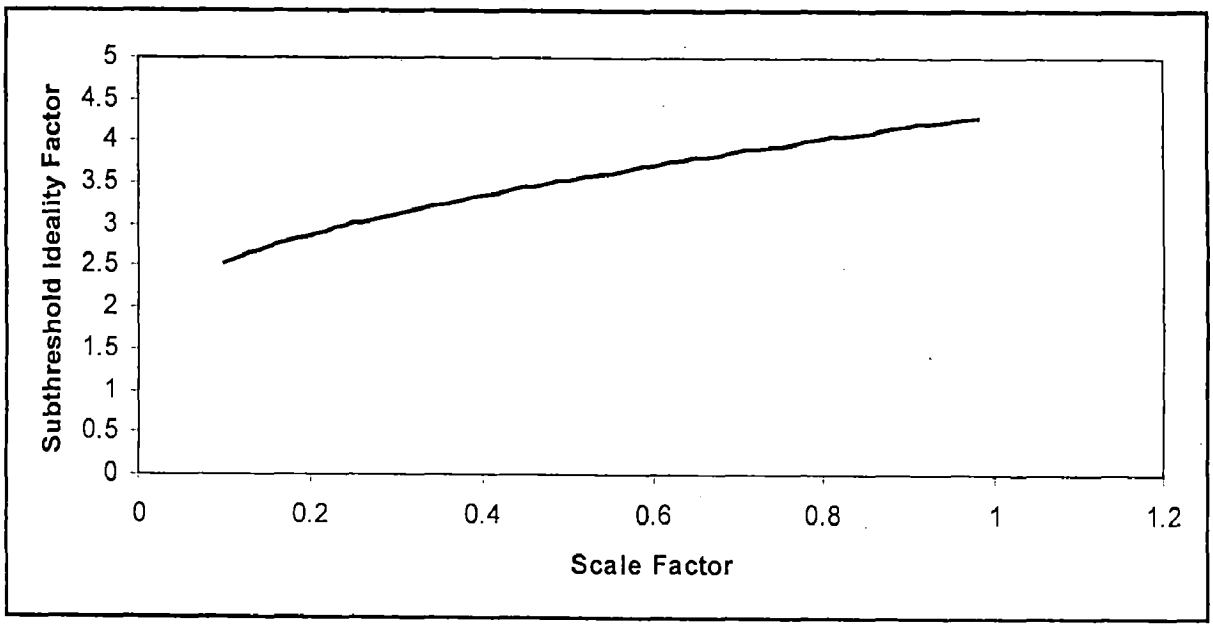


Fig. 6.1: Variation of Subthreshold Ideality Factor with Scale Factor.

The DIBL coefficient (σ) is a measure of barrier lowering in MOS transistors. It is plotted against the drain-source voltage, V_{DS} for different scale factors in Fig. 6.2. This shows that σ increases monotonically with V_{DS} and contradicts [6] according to which σ is a constant for a particular gate length. The increase in σ is all the more pronounced for low scale factors.

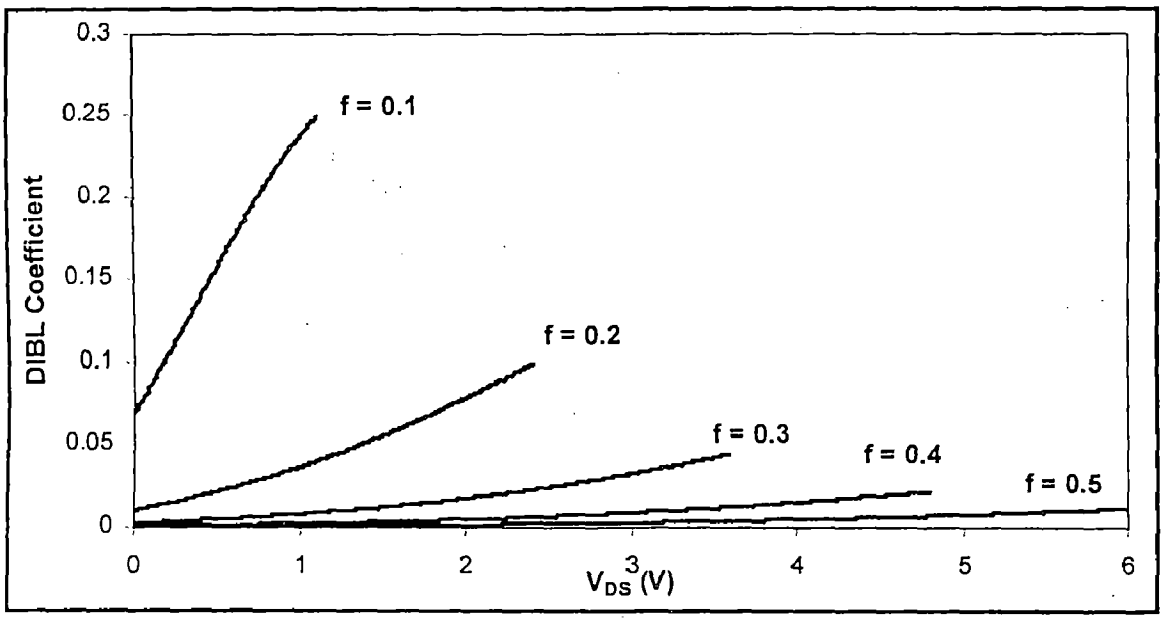


Fig. 6.2: Variation of DIBL coefficient with drain source voltage for different scale factors.

In Fig. 6.3, the lowermost curve shows the total NMOS standby power dissipation (P_{Leak}) with respect to the drain-source voltage (V_{DS}). The second curve depicts the power dissipation P_{dd} with respect to the drain-source voltage where P_{dd} occurs due to flow of drift-diffusion current I_{dd} (equation 3.33 of chapter 3) in the MOS channel. The uppermost curve shows the NMOS power dissipation P_{te} with respect to the drain-source voltage where P_{te} occurs due to flow of drift-diffusion current I_{te} (equation 3.38 of chapter 3) in the MOS channel.

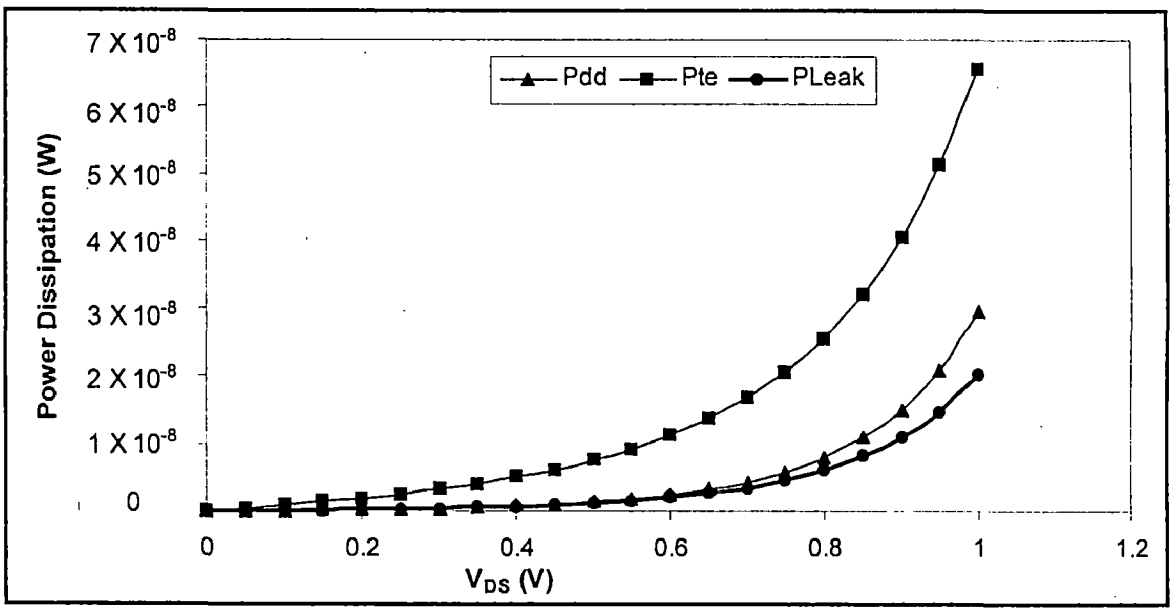


Fig. 6. 3: Variation of power dissipation with drain source voltage

where, $P_{dd} = I_{dd} V_{DS}$ and $P_{te} = I_{te} V_{DS}$.

The total standby power dissipation (P_{Leak}) versus V_{DS} considering both drift-diffusion and thermionic effects are shown in Fig. 6.4. Two curves are shown here, one taking into account ΔV_T and the other without considering ΔV_T. It is obvious that the power dissipation considering ΔV_T is much higher than the power dissipation without considering ΔV_T.

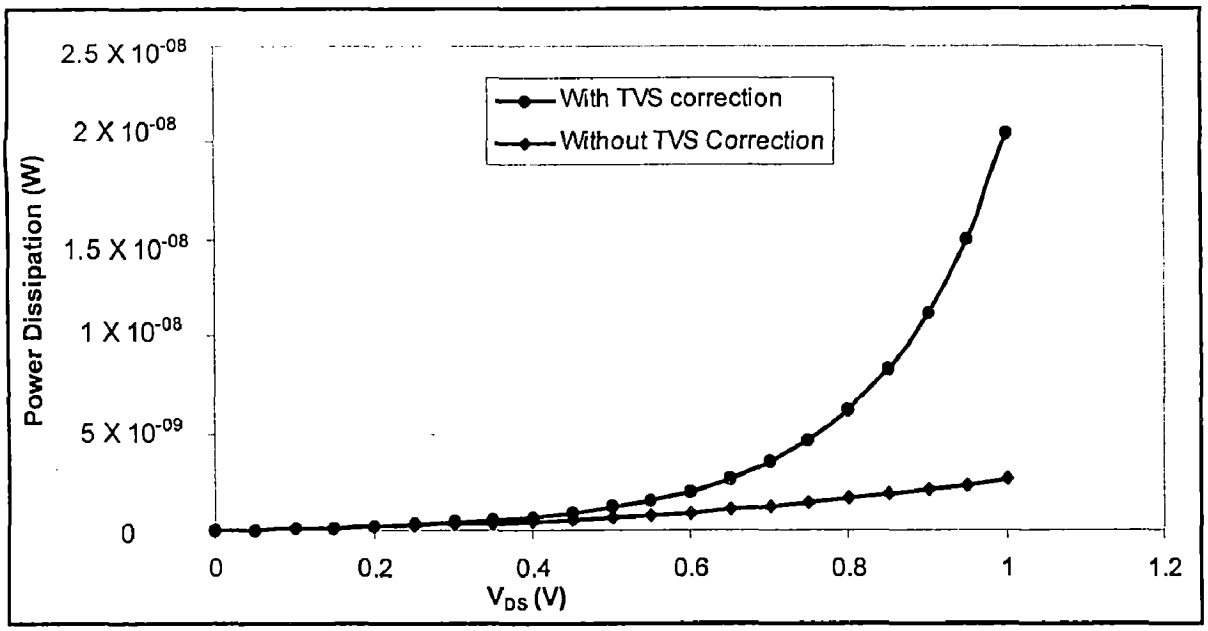


Fig. 6.4: P_{Leak} versus V_{DS}. Power dissipation is higher for the curve with Threshold Voltage Shift (TVS) correction.

Fig. 6.5 compares the power dissipation of a NMOS and PMOS transistor with respect to the scale factor. The power dissipation increases with decreasing scale factor.

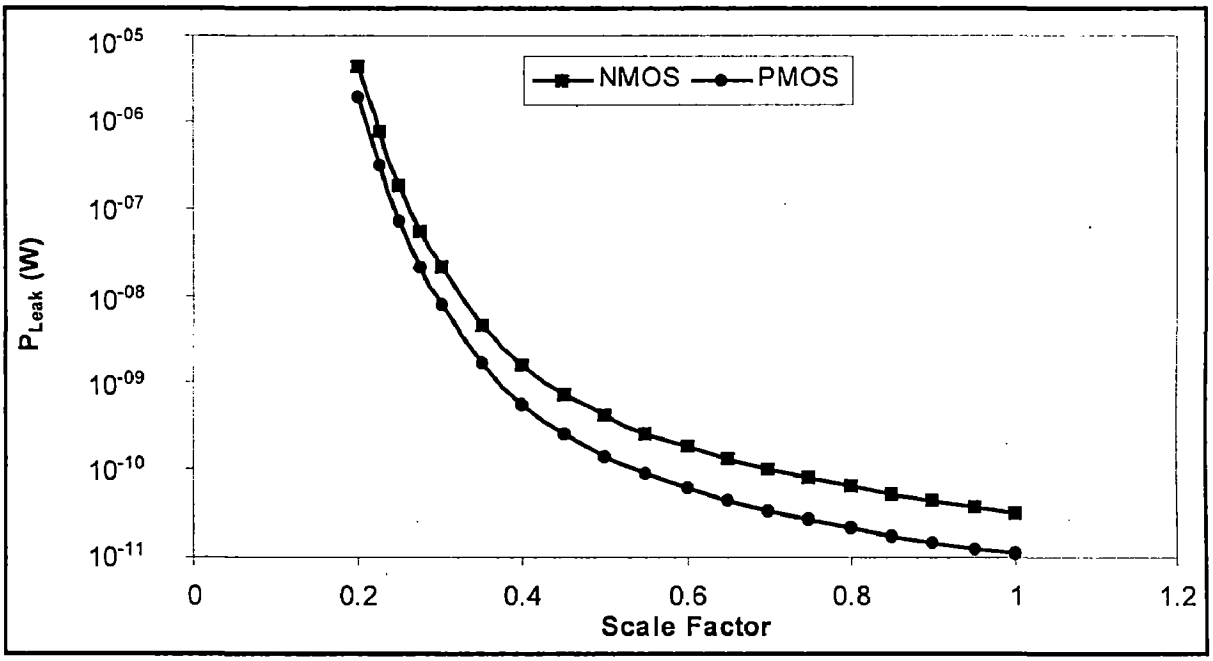


Fig. 6.5: Power dissipation versus scale factor.

The multiplication factor (M) depends exponentially on the peak field. M_n and M_p are plotted against the scale factor in Fig. 6.6.

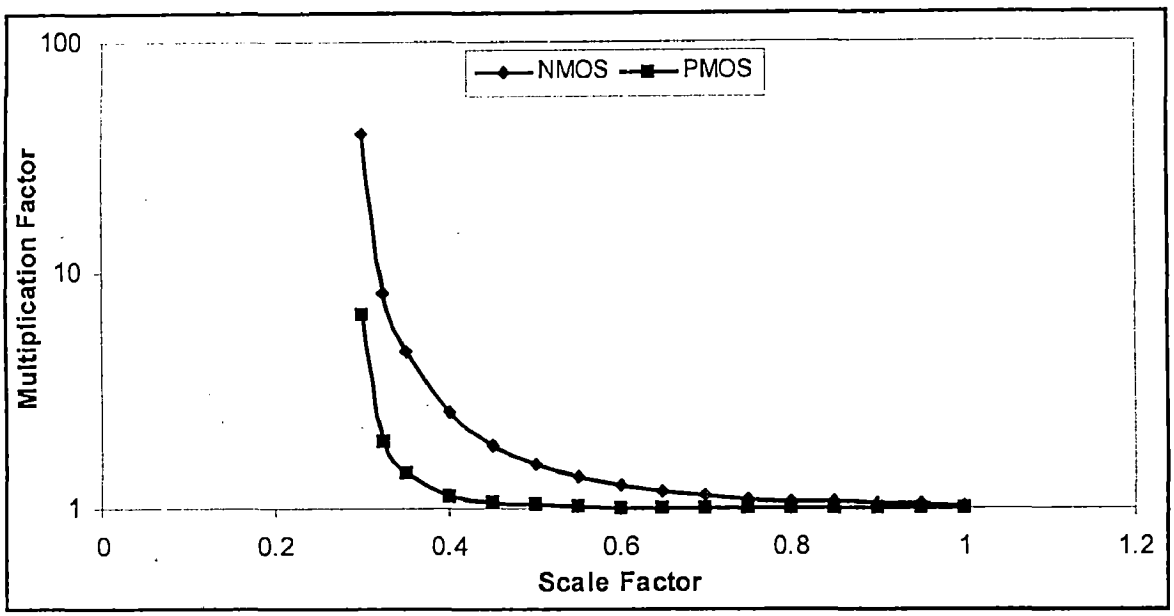


Fig. 6.6: Multiplication factor (M) versus scale factor.

The multiplication increases manifold with decreasing scale factors. This is because for a particular V_{DS}, the peak field increases for a decrease in scale factor. Therefore with increase in V_{DS}, there comes a point when for a very small increase in V_{DS}, the NMOS power dissipation (P_{MN}) increases by many orders of magnitude as shown in Fig. 6.7 in the next page. This increase is characterized by a sharp knee point, which corresponds to the breakdown voltage.

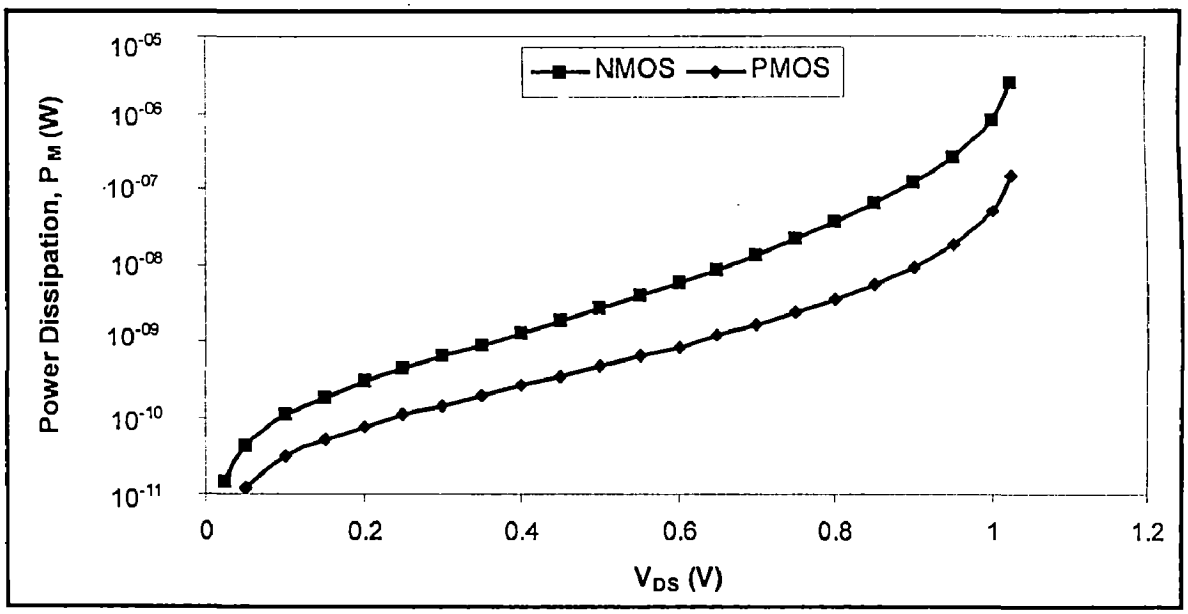


Fig. 6.7: Power dissipation (P_M) versus drain source voltage.

Fig. 6.8 shows that the contribution of the multiplication factor to the power dissipation increases with decreasing scale factors.

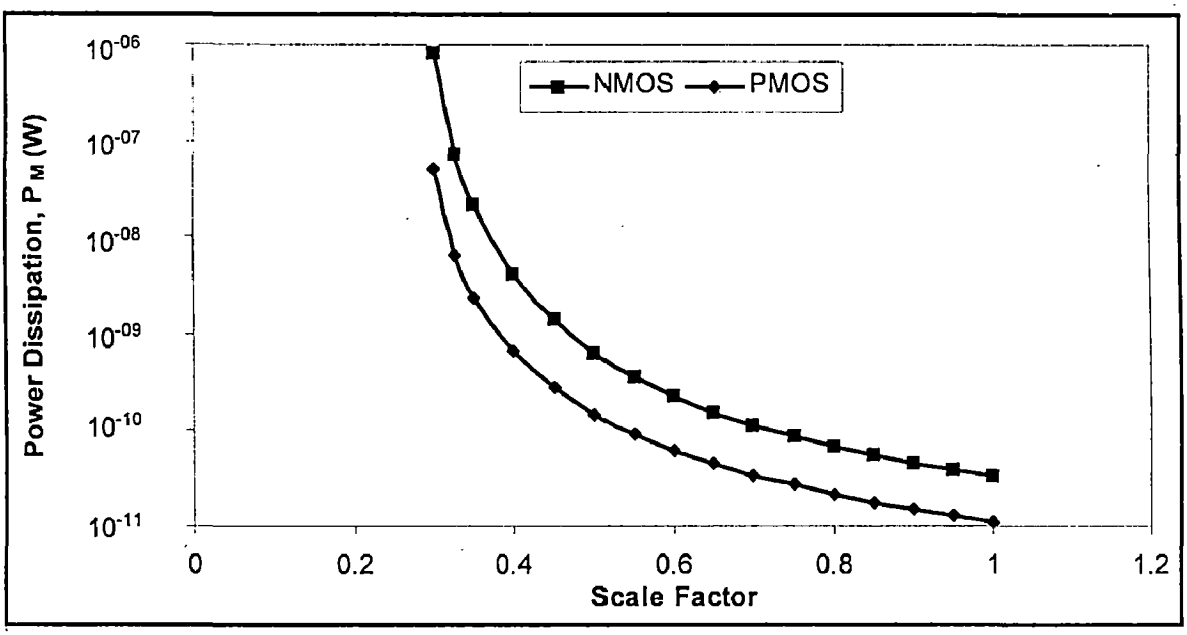


Fig. 6.8: Power dissipation (P_M) versus scale factor.

Results shown previously confirm the accuracy of the subthreshold impact ionization model. The leakage power dissipation of a combinational circuit is calculated using this model and the method described in chapter 5. For this purpose, a NAND3 (Fig. 5.1) gate is simulated first. The threshold voltage shift for a particular supply voltage for each DLS is determined using the method described in chapter 5 (Section 5.3). Graphical deduction of threshold voltage shift is given in detail in appendix C. Simulation results for a supply voltage V_{DD} = 1 V and $N_a = 5 \times 10^{22}$ $m^{-3}$are shown in Table 6.1 and for $N_a = 10^{23}$ m^{-3} in Table 6.2. Comparing Table 6.1 with Table 6.2, it can be said that although ΔV_T is lower for higher N_a for each scale factor, the electric field and hence the multiplication factor becomes high enough to cause breakdown for low scale factors. Therefore, including the effect of multiplication constraints the choice of N_a further.

Fig. 6.9 shows the circuit diagram for a two input multiplexer in terms of inverters, NAND and NOR gates. The CMOS circuit for the same is shown in Fig. 6.10.

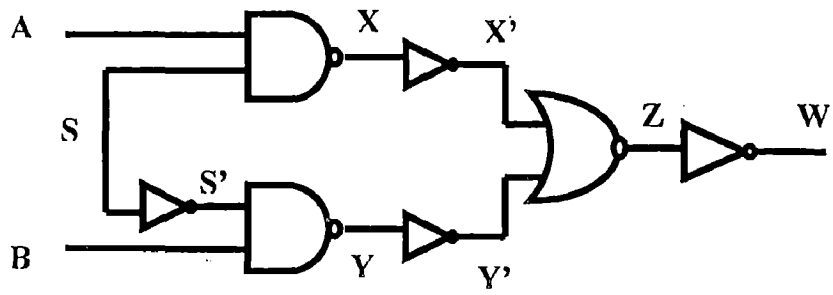


Fig. 6.9: Gate level diagram of a two input multiplexer.

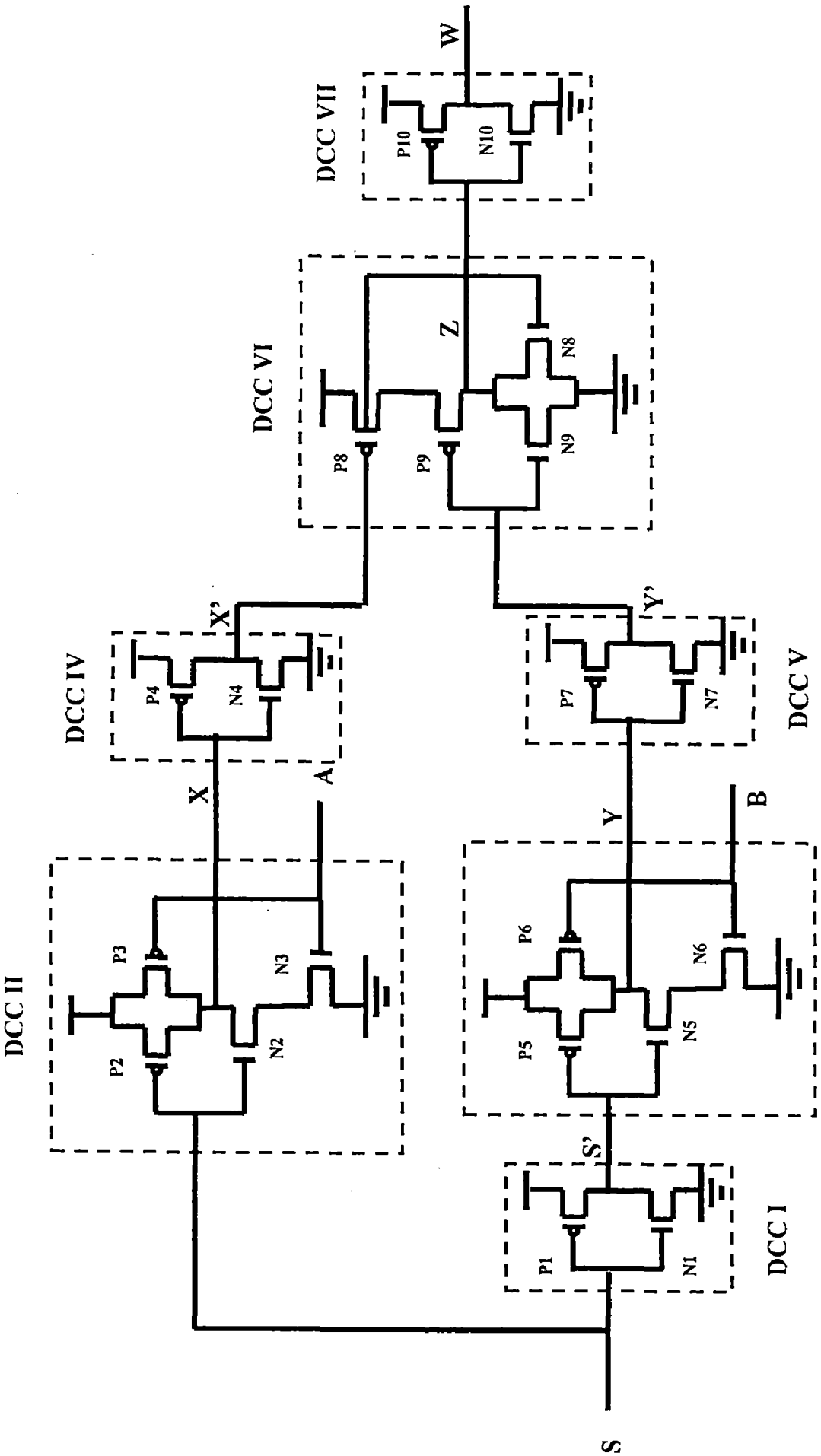
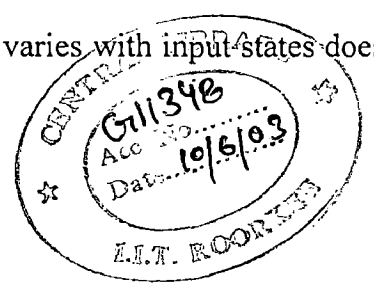


Fig. 6.10: CMOS equivalent of a two input multiplexer. A and B are inputs and S is the selection signal.

The inputs applied to each gate or DCC as well as the outputs are shown in Table 6.3a. The transistors contributing to leakage in each DCC for each input state is shown in Table 6.3b. The power dissipation of each DLS for each DCC in the circuit is shown in Table 6.4. Table 6.5 gives the state probabilities corresponding to each DCC. Using the data given in the tables mentioned above, the total circuit leakage not considering multiplication is calculated (Table 6.6) by summing the leakage components corresponding to each DCC. The total circuit leakage considering multiplication is calculated in Table 6.7. The results in Table 6.6 and 6.7 show that the leakage power dissipation of a circuit is highly dependent on the state of a circuit. In Table 6.8, the input states of a two input multiplexer are sorted in descending order of total power dissipation. The total standby power dissipation of a circuit is maximum for the input state where the number of leaking transistors is the maximum i.e., the power dissipation corresponding to the states {100}, {110}, {111} and {011} are higher than the states {000}, {010}, {101} and {001}. Among the cases, where the number of leaking transistors is same, standby power is higher where larger number of NMOS transistors contribute to leakage. For example, the power dissipation decreases from the input states {100} to {111}. However from {111} to {011} state, although the number of leaking NMOS transistors increase, there is a threshold voltage drop across the ON NMOS in one of the NAND gates (DCC II) and leakage across the PMOS instead of the NMOS (as for {111} state) in one of the inverters (DCC VII). This leads to lesser leakage in {011} state. For the cases, where the input A is same as B, the leakage would have been the same but for the selection signal S. For S = 0, the NMOS in DCC I leaks and leads to higher power dissipation than for S = 1 where the PMOS contributes to leakage. For each DLS in each DCC, the magnitude of the multiplication factor is different. But, when the circuit is considered as a whole, the order in which power dissipation varies with input states does not



change when M is considered. This suggests that although multiplication brings about a significant rise in the standby power dissipation, it does not dominate the behavior of the standby power dissipation. Further testing on benchmark circuits must be carried out to strengthen the above statement.

The average leakage is calculated by multiplying leakage component of a DCC with its corresponding state probability and adding all such terms (Table 6.9). Since, a device enters standby mode many times during the lifetime of its battery, the average leakage needs to be calculated to obtain a reliable estimate of average battery lifetime.

Out of the total eight input states, {000}, {001}, {011} and {100} lead to the standby or sleep state. Here, sleep state is taken as that primary input state for which the circuit output is zero. Out of these, {001} leads to minimum standby power dissipation. Therefore, this particular set of inputs can now be applied to the circuit in the standby mode to minimize average as well as total standby power dissipation. Similarly if all other requirements are satisfied in the active mode, {101} can be applied to minimize standby power dissipation.

Fig. 6.11 shows the gate level diagram for a D flip-flop. Fig. 6.12 shows the CMOS circuit for the same.

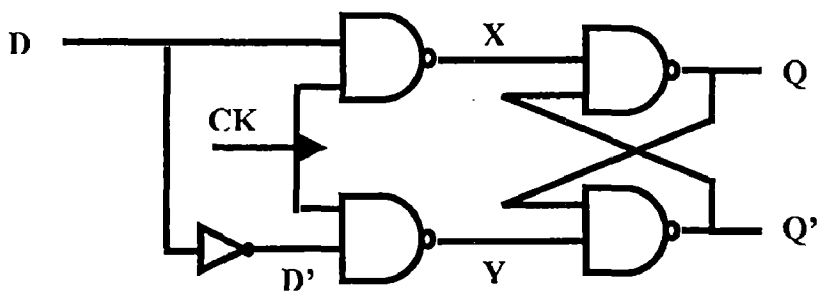


Fig. 6.11: Gate level diagram for a D flip-flop.

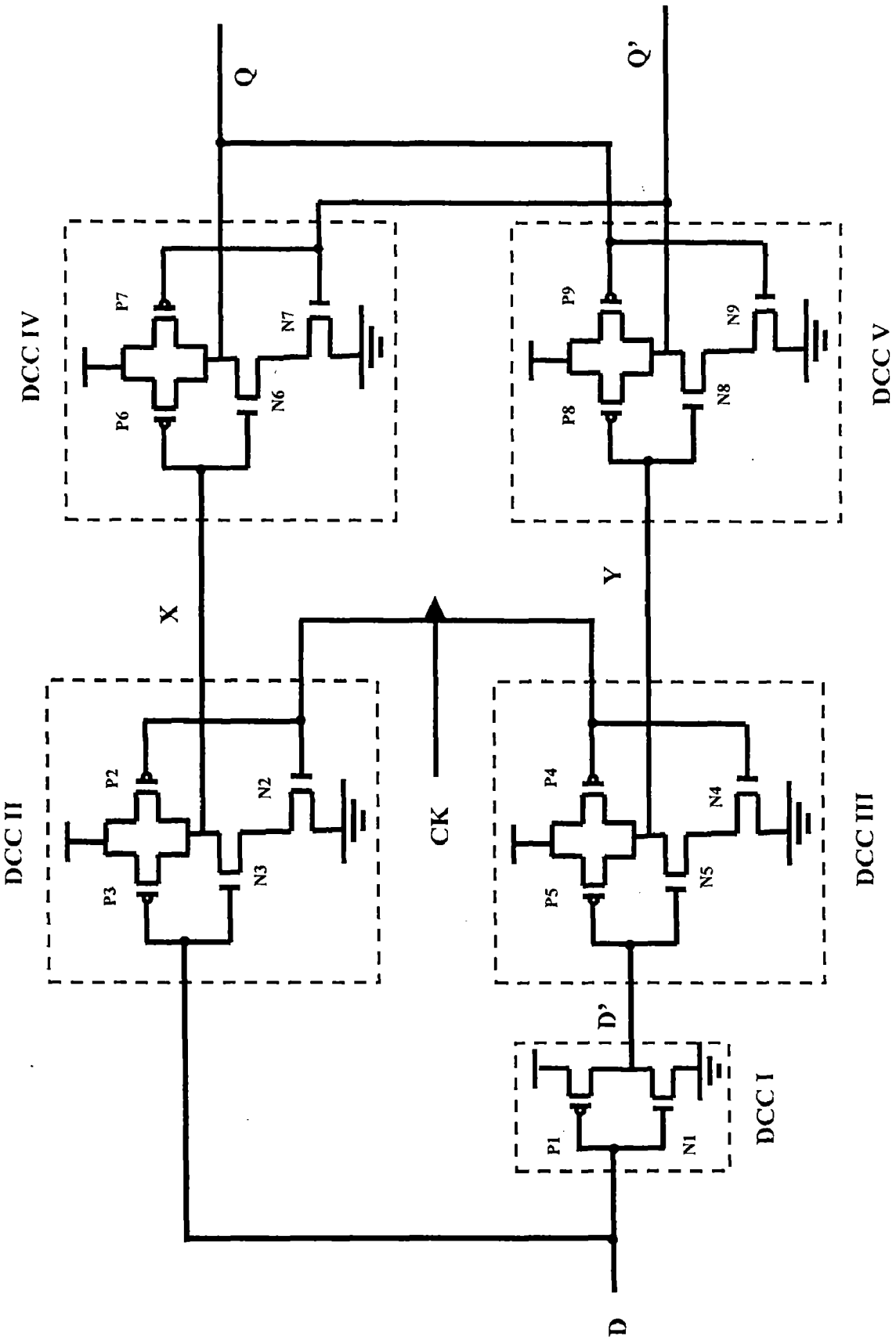


Fig. 6.12: CMOS circuit for a D flip-flop. CK is the clock signal.

The inputs applied to each gate or DCC as well as the outputs are shown in Table 6.10a. Transistors contributing to leakage in each DCC for each input state of the D flip flop is shown in Table 6.10b. Table 6.11 compares the total as well as the average power dissipation of a D flip flop with multiplication (P_M, P_{MAvg}) and without multiplication (P_{Leak}, P_{Avg}). The method of leakage power estimation is exactly same as that for a combinational circuit except for the determination of signal probabilities and correlation coefficients (section 5.2.1, chapter 5). A program for determination of signal probabilities and correlation coefficients in re-convergent nodes Q and Q' of a D flip flop is given in appendix-D.

Comparing the results of the two input multiplexer and D flip flop indicate certain similarities between them in terms of leakage patterns. For example, in both cases the standby power dissipation depends on the total number of leaking transistors, ratio of number of NMOS to PMOS transistors and threshold voltage drop across ON transistors. Results for D flip flop confirm dependence of leakage power on primary input states once again. Also, P_{Leak} and P_M vary in the same order with changing input states. Differences arise only because the two circuit topologies are different. Minimum total standby power dissipation is obtained when clock and D input are both high. Maximum power is dissipated when clock and D input are both zero. Flip flops being basic data storage elements, standby power dissipation in sequential circuits will depend on the data bits being stored.

Table 6.1: Leakage power calculations for a NAND3 circuit with each transistor having the same gate length L, W/L = 3, $N_a = 5 \times 10^{22}$ m^{-3}, V_{DD} = 1V. LEAK T is the set of transistors contributing to leakage. Power dissipation is given in Watts.

Table 6.1a: Scale factor, $f = 0.3$.

DLS	LEAK T	ΔV_T	V_{DS}	P_{Leak}	M	P_M
011	N1	-0.199465	1	9.75×10^{-08}	216	2.10×10^{-05}
101	N2	-0.115608	0.71	1.00×10^{-08}	4.47	4.49×10^{-08}
110	N3	-0.115608	0.71	1.00×10^{-08}	4.47	4.49×10^{-08}
111	P1, P2, P3	+0.199465	-1	1.14×10^{-07}	38.8	4.41×10^{-06}
			Total	2.32×10^{-07}		2.55×10^{-05}
			Average	2.89×10^{-08}		3.19×10^{-06}

Table 6.1b: Scale factor, $f = 0.4$.

DLS	LEAK T	ΔV_T	V_{DS}	P_{Leak}	M	P_M
011	N1	-0.029499	1	1.61×10^{-09}	2.53	4.08×10^{-09}
101	N2	-0.009541	0.53	3.36×10^{-10}	1.37	4.59×10^{-10}
110	N3	-0.009541	0.53	3.36×10^{-10}	1.37	4.59×10^{-10}
111	P1, P2, P3	+0.029499	-1	1.69×10^{-09}	1.14	1.93×10^{-09}
			Total	3.97×10^{-09}		6.93×10^{-09}
			Average	4.97×10^{-10}		8.66×10^{-10}

Table 6.1c: Scale factor, $f = 0.5$.

DLS	LEAK T	ΔV_T	V_{DS}	P_{Leak}	M	P_M
011	N1	-0.013201	1	4.18×10^{-10}	1.53	6.38×10^{-10}
101	N2	-0.003332	0.47	1.15×10^{-10}	1.11	1.27×10^{-10}
110	N3	-0.003332	0.47	1.15×10^{-10}	1.11	1.27×10^{-10}
111	P1, P2, P3	+0.013201	-1	4.30×10^{-10}	1.03	4.44×10^{-10}
			Total	1.08×10^{-09}		1.34×10^{-09}
			Average	1.35×10^{-10}		1.67×10^{-10}

Table 6.2: Leakage power calculations for a NAND3 circuit with $N_a = 10^{23}$ m^{-3}, V_{DD} = 1V. LEAK T is the set of transistors contributing to leakage. Power dissipation is given in Watts.

Table 6.2a: Scale factor, $f = 0.3$. The avalanche breakdown condition is represented as "BR".

DLS	LEAK T	ΔV_T	V_{DS}	P_{Leak}	M	P_M
011	N1	-0.016211	1	1.41×10^{-10}	BR	Invalid
101	N2	-0.005078	0.38	3.54×10^{-11}	BR	Invalid
110	N3	-0.005078	0.38	3.54×10^{-11}	BR	Invalid
111	P1, P2, P3	+0.016211	-1	1.46×10^{-08}	BR	Invalid

Table 6.2b: Scale factor, $f = 0.4$.

DLS	LEAK T	ΔV_T	V_{DS}	P_{Leak}	M	P_M
011	N1	-0.00735	1	4.49×10^{-11}	BR	Invalid
101	N2	-0.001651	0.23	8.19×10^{-12}	2.75	2.25×10^{-11}
110	N3	-0.001651	0.23	8.19×10^{-12}	2.75	2.25×10^{-11}
111	P1, P2, P3	+0.00735	-1	4.61×10^{-11}	BR	Invalid

Table 6.2c: Scale factor, $f = 0.5$

DLS	LEAK T	ΔV_T	V_{DS}	P_{Leak}	M	P_M
011	N1	-0.00255	1	2.11×10^{-11}	BR	Invalid
101	N2	-0.000345	0.14	2.44×10^{-12}	1.34	3.28×10^{-12}
110	N3	-0.000345	0.14	2.44×10^{-12}	1.34	3.28×10^{-12}
111	P1, P2, P3	+0.00255	-1	2.15×10^{-11}	BR	Invalid

Table 6.2d: Scale factor, $f = 0.6$

DLS	LEAK T	V_{DS}	P_{Leak}	M	P_M
011	N1	1	1.21×10^{-11}	8.65	1.04×10^{-10}
101	N2	0.05	4.40×10^{-13}	1.09	5.01×10^{-13}
110	N3	0.05	4.40×10^{-13}	1.09	5.01×10^{-13}
111	P1, P2, P3	-1	1.23×10^{-11}	2.00	2.45×10^{-11}
	Total		2.53×10^{-11}		1.30×10^{-10}
	Average		3.16×10^{-12}		1.62×10^{-11}

Table 6.3a: Input states for each DC Connected Component. (The nodes are as per the circuit diagram in Fig. 6.11a.)

A	B	S	S'	X	Y	X'	Y'	Z	W
0	0	0	1	1	1	0	0	1	0
0	0	1	0	1	1	0	0	1	0
0	1	0	1	1	0	0	1	0	1
0	1	1	0	1	1	0	0	1	0
1	0	0	1	1	1	0	0	1	0
1	0	1	0	0	1	1	0	0	1
1	1	0	1	1	0	0	1	0	1
1	1	1	0	0	1	1	0	0	1

Table 6.3b: Transistors contributing to leakage in each DCC for each input state. (The DCCs are represented as I, II... as per Fig. 6.9. The transistors are represented as per Fig. 6.10.)

Input	DC Connected Components						
ABS	I	II	III	IV	V	VI	VII
000	N1	-	N6	P4	P7	N8, N9	P10
001	P1	N3	-	P4	P7	N8, N9	P10
010	N1	-	P5, P6	P4	N7	P9	N10
011	P1	N3	N5	P4	P7	N8, N9	P10
100	N1	N2	N6	P4	P7	N8, N9	P10
101	P1	P2, P3	-	N4	P7	P8	N10
110	N1	N2	P5, P6	P4	N7	P9	N10
111	P1	P2, P3	N5	N4	P7	P8	N10

Table 6.4: Power dissipation of DLSs for each DCC of a two input multiplexer with each transistor having the same gate length L or scale factor f = 0.3, W/L = 3, $N_a = 5 \times 10^{22}$ m^{-3}, V_{DD} = 1V. LEAK T is the set of transistors contributing to leakage. Power dissipation is given in Watts.

Table 6.4a: DCC I (INV)

S	LEAK T	ΔV_T	V_{DS}	P_{Leak}	M	P_M
0	N1	-0.199465	1	9.75×10^{-08}	216	2.10×10^{-05}
1	P1	+0.199465	-1	3.63×10^{-08}	33.22	1.21×10^{-06}

Table 6.4b: DCC II (NAND2)

S	A	LEAK T	ΔV_T	V_{DS}	P_{Leak}	M	P_M
0	1	N2	-0.199465	1	9.75×10^{-08}	216	2.10×10^{-05}
1	0	N3	-0.115608	0.71	1.00×10^{-08}	4.47	4.49×10^{-08}
1	1	P2, P3	+0.199465	-1	7.26×10^{-08}	33.22	2.41×10^{-06}

Table 6.4c: DCC III (NAND2)

S'	B	LEAK T	ΔV_T	V_{DS}	P_{Leak}	M	P_M
0	1	N5	-0.199465	1	9.75×10^{-08}	216	2.10×10^{-05}
1	0	N6	-0.115608	0.71	1.00×10^{-08}	4.47	4.49×10^{-08}
1	1	P5, P6	+0.199465	-1	7.26×10^{-08}	33.22	2.41×10^{-06}

Table 6.4d: DCC IV (INV)

X	LEAK T	ΔV_T	V_{DS}	P_{Leak}	M	P_M
0	N4	-0.199465	1	9.75×10^{-08}	216	2.10×10^{-05}
1	P4	+0.199465	-1	3.63×10^{-08}	33.22	1.21×10^{-06}

Table 6.4e: DCC V (INV)

Y	LEAK T	ΔV_T	V_{DS}	P_{Leak}	M	P_M
0	N7	-0.199465	1	9.75×10^{-08}	216	2.10×10^{-05}
1	P7	+0.199465	-1	3.63×10^{-08}	33.22	1.21×10^{-06}

Table 6.4f: DCC VI (NOR2)

X'	Y'	LEAK T	ΔV_T	V_{DS}	P_{Leak}	M	P_M
0	1	P9	+0.115608	-0.71	3.6×10^{-09}	1.40	5.02×10^{-09}
1	0	P8	+0.199465	-1	3.63×10^{-08}	33.22	1.21×10^{-06}
1	1	N8, N9	-0.199465	1	1.95×10^{-07}	216	4.21×10^{-05}

Table 6.4g: DCC VII (INV)

Z	LEAK T	ΔV_T	V_{DS}	P_{Leak}	M	P_M
0	N10	-0.199465	1	9.75×10^{-08}	216	2.10×10^{-05}
1	P10	+0.199465	-1	3.63×10^{-08}	33.22	1.21×10^{-06}

Table 6.5: State probabilities corresponding to each DCC.

Table 6.5a: Node Probabilities

Node Probability	A	B	S	S'	X	Y	X'	Y'	Z	W
$P(j)$	0.5	0.5	0.5	0.5	0.75	0.75	0.25	0.25	0.5	0.5
1- $p(j)$	0.5	0.5	0.5	0.5	0.25	0.25	0.75	0.75	0.5	0.5

Table 6.5b: Output Observabilities

Obsevability	A	B	S	S'	X	Y	X'	Y'	Z	W
$B1(j)$	0.5	0.5	0.33	0.5	0.66	0.66	1	1	1	1
$B0(j)$	0.5	0.5	0.5	0.33	1	1	0.66	0.66	1	1

Table 6.5c: State Probabilities

State Probability	A	B	S	S'	X	Y	X'	Y'	Z	W
$d1(j)$	0.25	0.25	0.25	0.167	0.25	0.25	0.5	0.5	0.5	0.5
$d0(j)$	0.25	0.25	0.167	0.25	0.5	0.5	0.25	0.25	0.5	0.5

Table 6.6: Standby power dissipation of a two input multiplexer without considering the effect of multiplication. Power dissipation is given in Watts.

Input	DC Connected Components							Total
ABS	I	II	III	IV	V	VI	VII	(P_{Leak})
000	9.75×10^{-08}	-	1.00×10^{-08}	3.63×10^{-08}	3.63×10^{-08}	1.95×10^{-07}	3.63×10^{-08}	4.11×10^{-07}
001	3.63×10^{-08}	1.00×10^{-08}	-	3.63×10^{-08}	3.63×10^{-08}	1.95×10^{-07}	3.63×10^{-08}	3.50×10^{-07}
010	9.75×10^{-08}	-	7.26×10^{-08}	3.63×10^{-08}	9.75×10^{-08}	3.6×10^{-09}	9.75×10^{-08}	4.05×10^{-07}
011	3.63×10^{-08}	1.00×10^{-08}	9.75×10^{-08}	3.63×10^{-08}	3.63×10^{-08}	1.95×10^{-07}	3.63×10^{-08}	4.48×10^{-07}
100	9.75×10^{-08}	9.75×10^{-08}	1.00×10^{-08}	3.63×10^{-08}	3.63×10^{-08}	1.95×10^{-07}	3.63×10^{-08}	5.09×10^{-07}
101	3.63×10^{-08}	7.26×10^{-08}	-	9.75×10^{-08}	3.63×10^{-08}	3.63×10^{-08}	9.75×10^{-08}	3.77×10^{-07}
110	9.75×10^{-08}	9.75×10^{-08}	7.26×10^{-08}	3.63×10^{-08}	9.75×10^{-08}	3.6×10^{-09}	9.75×10^{-08}	5.03×10^{-07}
111	3.63×10^{-08}	7.26×10^{-08}	9.75×10^{-08}	9.75×10^{-08}	3.63×10^{-08}	3.63×10^{-08}	9.75×10^{-08}	4.74×10^{-07}

Table 6.7: Standby power dissipation of a two input multiplexer taking into account the effect of multiplication. Power dissipation is given in Watts.

Input	DC Connected Components							Total
ABS	I	II	III	IV	V	VI	VII	P_M
000	2.10×10^{-05}	-	4.49×10^{-08}	1.21×10^{-06}	1.21×10^{-06}	4.21×10^{-05}	1.21×10^{-06}	6.68×10^{-05}
001	1.21×10^{-06}	4.49×10^{-08}	-	1.21×10^{-06}	1.21×10^{-06}	4.21×10^{-05}	1.21×10^{-06}	4.69×10^{-05}
010	2.10×10^{-05}	-	2.41×10^{-06}	1.21×10^{-06}	2.10×10^{-05}	5.02×10^{-09}	2.10×10^{-05}	6.66×10^{-05}
011	1.21×10^{-06}	4.49×10^{-08}	2.10×10^{-05}	1.21×10^{-06}	1.21×10^{-06}	4.21×10^{-05}	1.21×10^{-06}	6.80×10^{-05}
100	2.10×10^{-05}	2.10×10^{-05}	4.49×10^{-08}	1.21×10^{-06}	1.21×10^{-06}	4.21×10^{-05}	1.21×10^{-06}	8.78×10^{-05}
101	1.21×10^{-06}	2.41×10^{-06}	-	2.10×10^{-05}	1.21×10^{-06}	1.21×10^{-06}	2.10×10^{-05}	4.80×10^{-05}
110	2.10×10^{-05}	2.10×10^{-05}	2.41×10^{-06}	1.21×10^{-06}	2.10×10^{-05}	5.02×10^{-09}	2.10×10^{-05}	8.76×10^{-05}
111	1.21×10^{-06}	2.41×10^{-06}	2.10×10^{-05}	2.10×10^{-05}	1.21×10^{-06}	1.21×10^{-06}	2.10×10^{-05}	6.9×10^{-05}

Table 6.8: Input States for two-input multiplexer in descending order of dissipating total power. LEAK T is the set of transistors contributing to leakage. N and P represent NMOS and PMOS transistors respectively.

S. No.	ABS	P_M/P_{Leak}	Leak T	No. of Leak T
1	100	114	3P, 5N	8
2	110	315	4P, 4N	8
3	111	164	5P, 3N	8
4	011	102	4P, 4N	8
5	000	146	3P, 4N	7
6	010	127	4P, 3N	7
7	101	174	5P, 2N	7
8	001	146	4P, 3N	7

Table 6.9: Average standby power dissipation of a two input multiplexer. Power dissipation is given in Watts.

ABS	P_{Avg}	P_{Mavg}	P_{MAvg} / P_{Avg}
000	1.53×10^{-07}	2.58×10^{-05}	169
001	1.36×10^{-07}	2.26×10^{-05}	166
010	1.61×10^{-07}	2.60×10^{-05}	162
011	1.69×10^{-07}	2.78×10^{-05}	166
100	1.77×10^{-07}	3.10×10^{-05}	175
101	1.70×10^{-07}	2.34×10^{-05}	138
110	1.85×10^{-07}	3.13×10^{-05}	169
111	1.94×10^{-07}	2.87×10^{-05}	148

Table 6.10a: Input States at different nodes of a D flip-flop. The clock levels are indicated by "↑" for high and "↓" for low.

CK	D	D'	X	Y	Q	Q'
↑	0	1	1	0	0	1
↓	0	1	1	1	0	1
↑	1	0	0	1	1	0
↓	1	0	1	1	1	0

Table 6.10b: Transistors contributing to leakage in each DCC for each input state. (The DCCs are represented as I, II... as per Fig. 6.11. The transistors are represented as per Fig. 6.12.)

Inputs		DC Connected Components				
CK	D	I	II	III	IV	V
↑	0	N1	N3	P4, P5	P6, P7	-
↓	0	N1	-	N4	P6, P7	N9
↑	1	P1	P2, P3	N5	-	P8, P9
↓	1	P1	N2	-	N7	P8, P9

Table 6.11: Data for standby power dissipation of a D flip flop. Power dissipation is given in Watts. Each transistor has the same gate length L or scale factor $f = 0.3$, W/L = 3, $N_a = 5 \times 10^{22}$ m^{-3}, $V_{DD} = 1$V.

Inputs		Power dissipation			
CK	D	P_{Leak}	P_{Avg}	P_M	P_{MAvg}
↑	0	2.53×10^{-07}	3.79×10^{-08}	25.9×10^{-06}	1.21×10^{-06}
↓	0	2.77×10^{-07}	5.76×10^{-08}	44.5×10^{-06}	4.74×10^{-06}
↑	1	1.92×10^{-07}	4.40×10^{-08}	6.11×10^{-06}	1.42×10^{-06}
↓	1	2.16×10^{-07}	6.37×10^{-08}	24.7×10^{-06}	4.95×10^{-06}

CONCLUSION

Standby power dissipation is dealt with at two levels of hierarchy i.e., at the transistor level and at the circuit level.

The transistor level requires mathematical modeling of physical phenomena contributing to subthreshold current. These include drift-diffusion, thermionic emission, short channel effects and high field effects. The first three have been accounted for in models available in literature. Because of continuous scaling of MOS devices, high field effects become dominant. Therefore, in this dissertation the focus in on increase in power dissipation brought about by the threshold voltage shift and the phenomenon of impact ionization in the MOS channel. A holistic model has been developed which includes the effect of multiplication of carriers in the subthreshold regime. Results prove that multiplication considerably enhances the channel current and hence power dissipation. This becomes all the more prominent with scaling. Infact at very low scale fcators (0.1 – 0.2), electric field is high enough to cause breakdown even below 1 V drain source voltages.

At the circuit level, two specific circuits namely a two input multiplexer and a D flip flop have been studied for standby power dissipation. Since the number of input states is smaller, all the primary input combinations are assessed without largely affecting simulation time unlike [14]. Typically, multiplication enhances standby power dissipation by an order of magnitude or more. However in both the circuits, including multiplication effects do not change the input states corresponding to maximum and minimum standby power. It will be interesting to study the variation of power dissipation due to multiplication with respect to primary input states in larger benchmark circuits i.e., whether multiplication simply enhances the power dissipation or is also capable of changing the leakage bounds.

REFERENCES

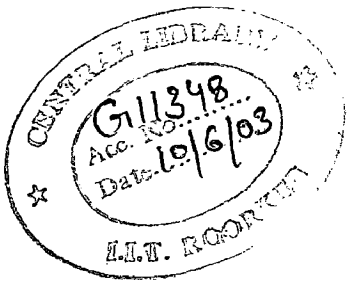
1. S.M. Sze, Physics of Semiconductor Devices. New York. Wiley, 1981.
2. Yuan Taur, Tak. H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, New York, 1998.
3. R.R. Troutman, " VLSI limitations from drain-induced barrier lowering", IEEE Trans. Electron Devices, ED-26, p. 461, 1979.
4. J. E. Chung, M. C. Jeng, J. E. Moon, P. K. Ko, and C. Hu, "Performance and reliability design issues for deep submicrometer MOSFET's", IEEE Trans. Electron Devices, vol. 38, no. 3, pp. 545-554, 1991.
5. B. J. Sheu et al., "BSIM: Berkley short-channel IGFET model for MOS transistors", IEEE J. Solid State Circuits, vol. SC-22, pp. 558-566, June 1987.
6. T.A. Fjeldly, M. Shur, " Threshold voltage modeling and the sub threshold regime of operation of short channel MOSFETS", IEEE Trans. Electron Devices, Vol. ED-40, p. 137, 1993.
7. M. Shur, T.A., Fjeldly, T. Ytterdal, and K.Lee. "Unified MOSFET model," Solid State Electronics, 1992.
8. N.C. Das, W.S. Khokle, and S.D. Mohanty, "Visible light emission from Silicon MOSFETS," Solid state Electronics, Vol. 28, pp. 967-977, 1985.
9. P. Spirito, IEEE Trans. Electron Devices, ED-21, pp. 226, 1974.
10. R.R. Troutman, "Low level avalanche multiplication," ED-23, pp. 429, 1976.
11. R.R. Troutman, " Subthreshold characteristics of MOSFETS," IEEE Trans. Circuit Theory, CT-20, pp. 659, 1973.

12. D. A. Pucknell, K. Eshraghian, Basic VLSI Design, 1995.

13. Zhanping Chen, Liqiong Wei, Mark Johnson, and Kaushik Roy, " Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of transistor Stacks", Proc. Int. Symp. Low Power Electron. Design, 1998, pp. 239-244.

14. S. Sirichotiyakul, T. Edwards, C. Oh, R. Panda, D. Blaauw, "Duet: An Accurate Estimation and Optimization Tool for Dual-V_t circuits", IEEE Transactions on Very Large Integration Systems, Vol. 10, p. 79, April 2002.

15. S. Ercolani, M. Favalli, M. Damiani, P. Olivo, and B. Ricco,"Testability Measures in Pseudorandom Testing", IEEE Trans. Computer-Aided Design, Vol. 11, p. 794, June1992.



DEVICE PARAMETERS AND PHYSICAL CONSTANTS

Symbol	Value
W	3 μm
L	1 μm
t_{ox}	30 °A
N_a	5×10^{22} m^{-3}, 10^{23} m^{-3}
N_D	10^{25} m^{-3}
n_i	1.5×10^{16} m^{-3}
Q_{ss}	1.6×10^{-5} Cm^{-2}
μ_n	0.06 m^2 V^{-1} s^{-1}
μ_p	0.02 m^2 V^{-1} s^{-1}
E_g	1.12 eV
χ	0.5
E_B	3×10^7 V m^{-1}
ε_o	8.854×10^{-12} Fm^{-1}
ε_s	11.8 ε_o
ε_{ox}	4 ε_o
T	300 K
K	1.38×10^{-23} JK^{-1}

NUMERICAL COMPUTATION OF NMOS DIBL COEFFICIENT, σ

The threshold voltage shift ΔV_T, depends on the DIBL coefficient. The DIBL coefficient σ can be obtained from equations (2.29) and (2.31) as

$$\sigma = \frac{2\eta\chi d_o}{\lambda} \frac{\sinh(\frac{x_s}{\lambda})}{\left[\cosh(\frac{L-x_d}{\lambda}) - \cosh(\frac{x_s}{\lambda})\right]} \quad \ldots(B.1)$$

In (B.1), x_s, x_d, d_o and λ all depend on the interface potential which is given by

$$\psi_s^o = -V_{bi} + 2\phi_b + \frac{V_{GT}}{\eta} \quad \ldots(B.2)$$

where,

$$V_{GT} = V_{GS} - V_T$$

The threshold voltage,

$$V_T = V_{To} + \Delta V_T$$

V_{To} is the zero drain bias threshold voltage. The interface potential in terms of threshold voltage shift ΔV_T can now be written as

$$\psi_s^o = -V_{bi} + 2\phi_b + \frac{V_{GTo}}{\eta} - \frac{\Delta V_T}{\eta} \quad \ldots(B.3)$$

where, $V_{GTo} = V_{GS} - V_{To}$

or

$$\psi_s^o = -V_{bi} + 2\phi_b + \frac{V_{GTo}}{\eta} + \frac{\sigma V_{DS}}{\eta} \quad \ldots(B.4)$$

where,

$$\eta = 1 + \frac{C_d}{C_{ox}} \qquad \ldots(B.5)$$

and C_d is the depletion layer capacitance given by

$$C_d = \frac{\varepsilon_s}{d_{dep}}$$

where

$$d_{dep} \approx \sqrt{\frac{2\varepsilon_S}{qN_a}(\psi_s + V_{bi})} = d_o\sqrt{1 + \frac{V(x)}{\psi_s^o + V_{bi}}}$$

Therefore,

$$d_o \approx \sqrt{\frac{2\varepsilon_S}{qN_a}(\psi_s^o + V_{bi})} \qquad \ldots(B.6)$$

Expanding d_{dep} to the lowest order in d_o, using equation (3.18)

$$C_d \approx \frac{\varepsilon_s}{d_o}$$

therefore, η can be written as

$$\eta = 1 + \frac{\varepsilon_s}{C_{ox}d_o} \qquad \ldots(B.7)$$

From (B.6) and (B.4),

$$d_o = \sqrt{\frac{2\varepsilon_s}{qN_a}(2\phi_b + \frac{V_{GTo}}{\eta} + \frac{\sigma V_{DS}}{\eta})} \qquad \ldots(B.8)$$

Let $x_o = \sqrt{\frac{2\varepsilon_s}{qN_a}}$ and $x_1 = \frac{x_o C_{ox}}{\varepsilon_s}$

Then,

$$\frac{1}{d_o} = \frac{1}{x_o}\left(2\phi_b + \frac{(V_{GTo} + \sigma V_{DS})}{\eta}\right)^{-\frac{1}{2}} = \frac{1}{x_o\sqrt{2\phi_b}}\left(1 + \frac{(V_{GTo} + \sigma V_{DS})}{2\phi_b\eta}\right)^{-\frac{1}{2}} \qquad \ldots(B.9)$$

Using binomial expansion and retaining up to first order gives

$$\frac{1}{d_o} = \frac{1}{x_o\sqrt{2\phi_b}}\left(1 - \frac{(V_{GTo} + \sigma V_{DS})}{4\phi_b \eta}\right) \qquad \ldots(B.10)$$

Substituting (B.10) in (B.7), a quadratic equation in η is obtained as

$$\eta^2 - x_z\eta + \frac{x_y x_w}{4} = 0 \qquad \ldots(B.11)$$

The solution to the above equation is given by

$$\eta = x_z \pm \left(x_z^2 - x_y x_w\right)^{\frac{1}{2}} \qquad \ldots(B.12)$$

where, $x_z = 1 + x_y$, $x_y = \frac{1}{x_1\sqrt{2\phi_b}}$ and $x_w = \frac{(V_{GTo} + \sigma V_{DS})}{\phi_b}$.

Therefore, η is now a function of the DIBL coefficient. Rejecting the negative root,

$$\eta = x_z + \left(x_z^2 - x_y x_w\right)^{\frac{1}{2}} \qquad \ldots(B.13)$$

The depletion widths as functions of the DIBL coefficient can be written as

$$x_s = x_o\sqrt{(-V_{bi} + 2\phi_b + \frac{V_{GTo}}{\eta} + \frac{\sigma V_{DS}}{\eta})} \qquad \ldots(B.14)$$

$$x_d = x_o\sqrt{(V_{DS} + V_{bi} - 2\phi_b - \frac{V_{GTo}}{\eta} - \frac{\sigma V_{DS}}{\eta})} \qquad \ldots(B.15)$$

From one dimensional theory,

$$\lambda = d_o\left(1 + \frac{\varepsilon_{ox} d_o}{\varepsilon_s t_{ox}}\right)^{-1/2} \qquad \ldots(B.16)$$

Since, λ depends on d_o, it is also a function of the DIBL coefficient.

The right hand side of equation (B.1) can now be explicitly written as a function of σ using equations (B.8), (B.13), (B.14), (B.15) and (B.16).

$$\sigma \approx g(\sigma) \Rightarrow \sigma - g(\sigma) \approx 0$$

or

$$f(\sigma) \approx 0 \qquad \ldots(B.17)$$

Equation (B.17) can now be solved by any one of the numerical methods to obtain σ and hence the threshold voltage shift. Bisection method has been used in this dissertation as it ensures convergence.

GRAPHICAL DEDUCTION OF THRESHOLD VOLTAGE SHIFT

In the subthreshold model described in chapter 3, the threshold voltage shift has been calculated numerically for a particular V_{DS} and V_{GS}. But in case of a circuit, only the supply voltage is known and many a times, V_{DS} is a function of the threshold voltage shift. For such problems, graphical solutions are often the best as they are less cumbersome. Here, the problem has been solved in detail only for scale factor of 0.1. The threshold voltage shift can be determined for other scale factors in a similar manner.

Using the numerical computation method described in appendix-B and equation (3.31) of chapter 3, the threshold voltage shift can be determined for different gate source voltages and different drain source voltages. Fig. 1 shows the variation of threshold voltage shift with the gate source voltage V_{GS} for different values of drain source voltages. It is observed that the plots are linear in nature. Therefore, each line for a particular V_{DS} can be expressed as a linear equation.

$$\Delta V_T = m_1(V_{DS})\, V_{GS} + C_1 \qquad \ldots(C.1)$$

where, both the slope m_1 and intercept C_1 are functions of V_{DS}. All such slopes and intercepts for different drain source voltages are determined and plotted against V_{DS}.

From the nature of the plot of m_1 versus V_{DS} as shown in Fig. 2, equation of m_1 in terms of V_{DS} is obtained as

$$m_1 = 0.1906V_{DS}^2 + 0.0757V_{DS} + 0.0002 \qquad \ldots(C.2)$$

Similarly from plot of C_1 versus V_{DS} as shown in Fig. 3,

$$C_1 = -0.1489V_{DS}^2 - 0.0544V_{DS} + 0.0002 \qquad \ldots(C.3)$$

Equations (C.2) and (C.3) substituted back in (C.1), such that

$$\Delta V_T = (0.1906\, V_{DS}^2 + 0.0757 V_{DS} + 0.0002) V_{GS} - 0.1489 V_{DS}^2 - 0.0544 V_{DS} + 0.0002 \quad \ldots(C.4)$$

Fig. 4 shows the variation of threshold voltage shift with V_{DS} for different gate source voltages. For simplicity, linear fits are considered such that

$$\Delta V_T = m_2(V_{GS})\, V_{DS} \quad \ldots(C.5)$$

Since the threshold voltage shift is negative for an NMOS, the intercept of the equation is considered zero. The slope m_2 is a function of V_{GS}. m_2 can now be determined from the linear fits shown in Fig. 4 for different V_{GS}.

From plot of m_2 versus V_{GS} as in Fig. 5, equations for m_2 in terms of V_{GS} is determined as

$$m_2 = 0.2265 V_{GS} - 0.1547 \quad \ldots(C.6)$$

Back substituting (C.6) in (C.5) gives

$$\Delta V_T = 0.2265 V_{GS} V_{DS} - 0.1547 V_{DS} \quad \ldots(C.7)$$

Equations (C.4) and (C.7) are then added to obtain an empirical relation of ΔV_T in terms of V_{GS} and V_{DS}, which are functions of ΔV_T. The value of ΔV_T can now be obtained for a particular supply voltage by solving the empirical relation so developed.

Fig. C.1: Variation of Threshold Voltage Shift versus gate source voltage (V_{GS}).

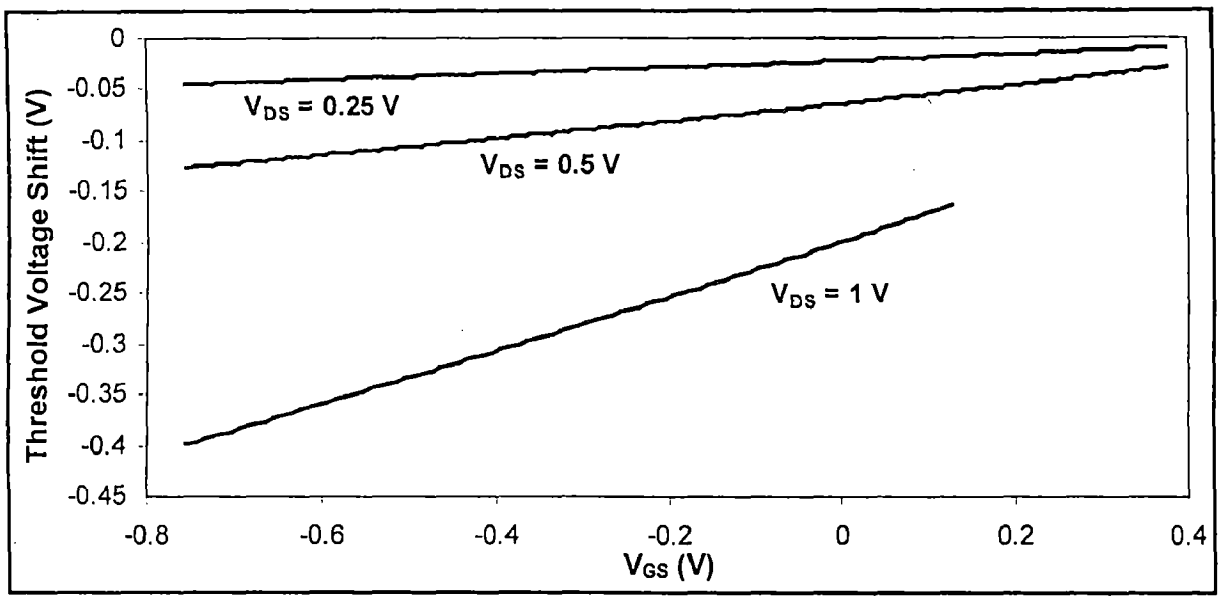


Fig. C.2: Variation of m_1 versus drain source voltage (V_{DS}).

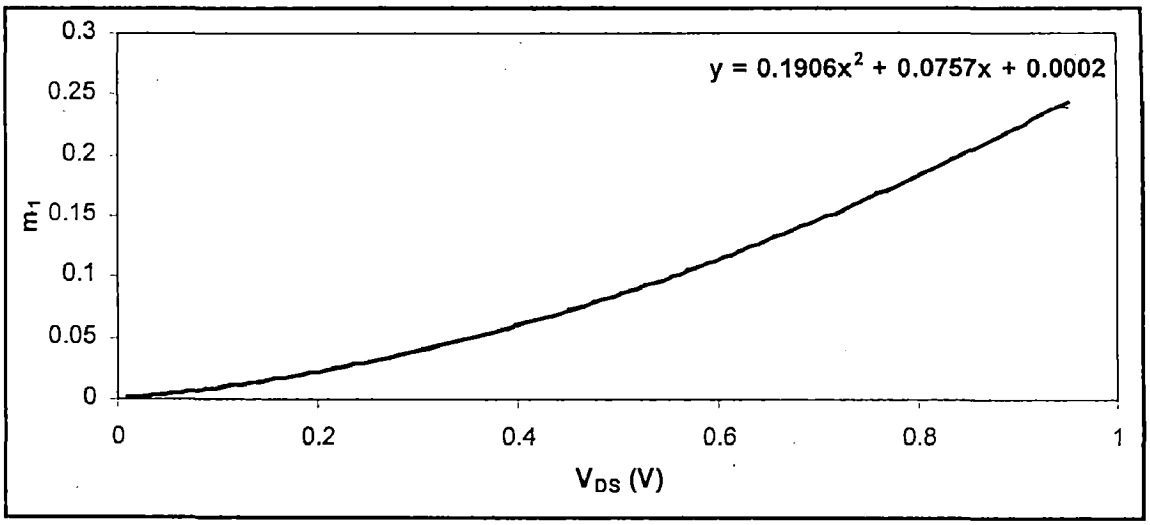


Fig. C.3: Variation of C_1 versus drain source voltage (V_{DS}).

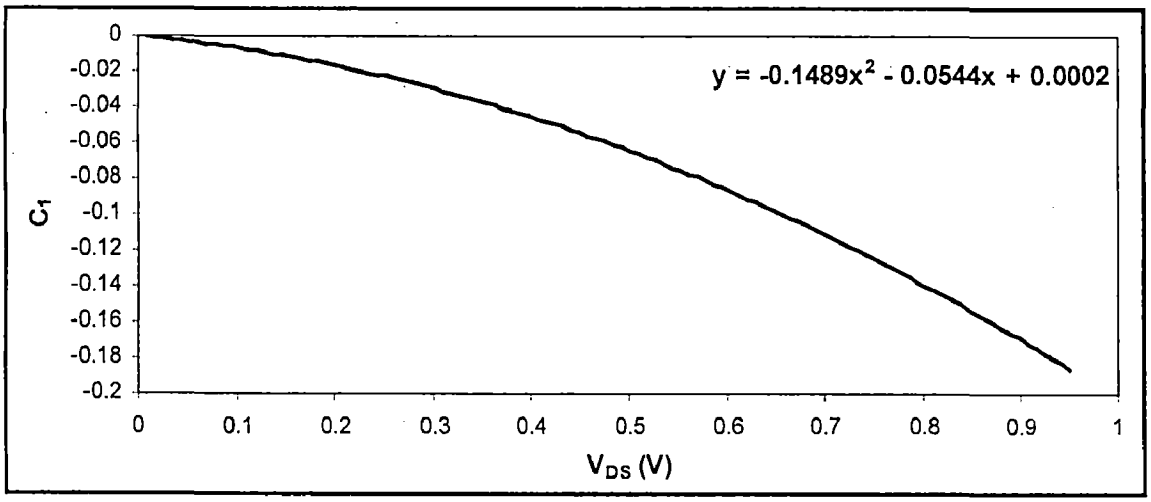


Fig. C.4: Variation of threshold voltage shift with drain source voltage (V_{DS}).

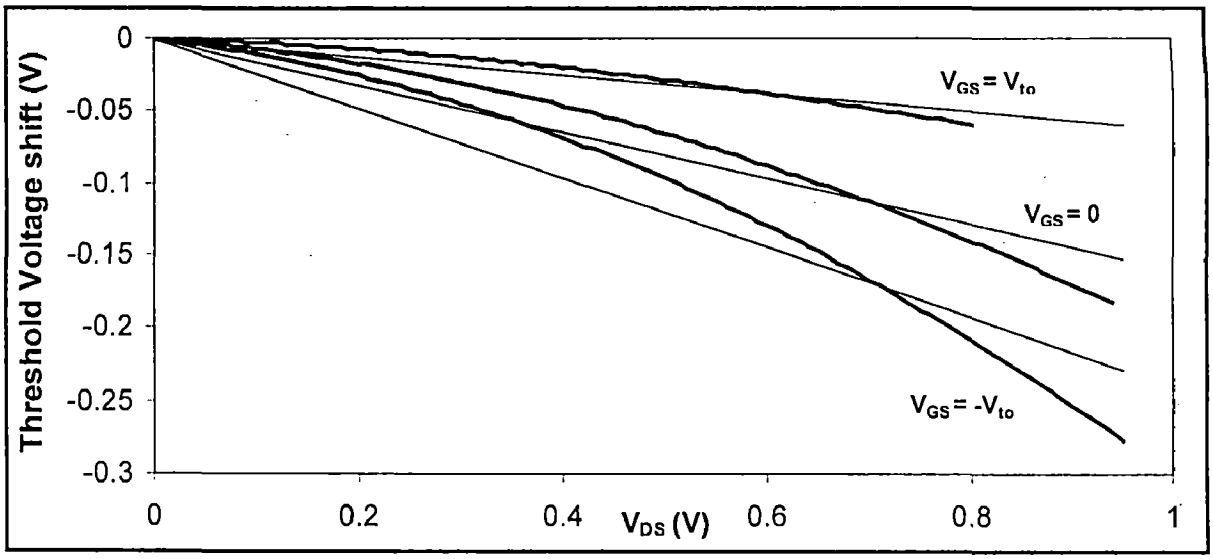
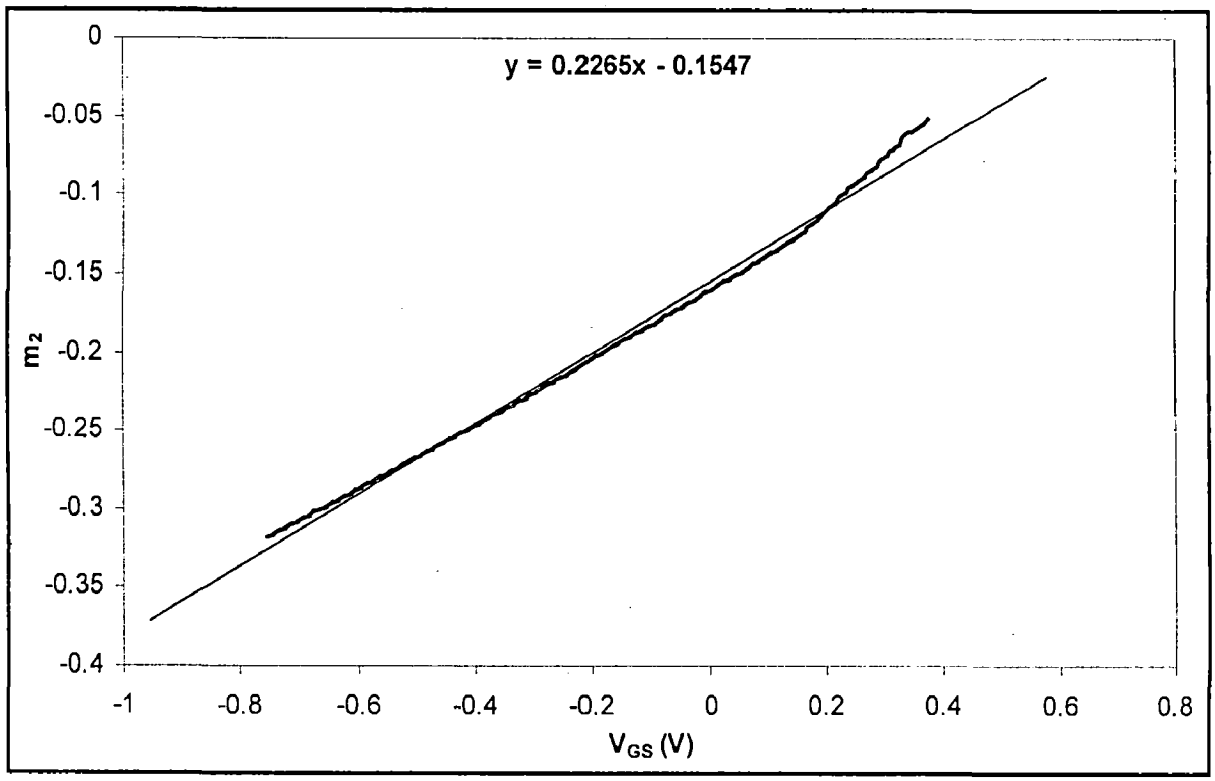


Fig. C.5: Variation of m_2 with gate source voltage (V_{GS}).



PROGRAMS

Program D.1: Numerical computation of threshold voltage shift.

```
#include<iostream.h>
#include<math.h>
#include<conio.h>
#include<fstream.h>

long double l,f,eta,chi,vds,phibf,vbif,vgto,xy,xz,psioso,x0,x1;
//function for determining DIBL coefficient
long double n(long double root)
{
long double xl,y0,y1,y2,y3,y4,y5,y6,y7,y8,y9,xw,x2,x3,x4,x5,x6,theta;
/*
cout<<"x0= "<<x0<<endl;
cout<<"x1= "<<x1<<endl;
cout<<"xz= "<<xz<<endl;
cout<<"f= "<<f<<endl;
cout<<"l= "<<l<<endl;
cout<<"chi= "<<chi<<endl;
*/
xw=(vgto+root*vds)/(phibf);
//eta as obtained from quadratic equation
eta=xz+sqrt((xz*xz)-xy*xw);
//cout<<"\neta= "<<eta<<endl;
```

```
psioso=-vbif+2*phibf+vgto/eta;
//cout<<"psioso= "<<psioso<<endl;
x2=psioso+vbif;
//cout<<"x2= "<<x2<<endl;
x3=-psioso;
//cout<<"x3= "<<x3<<endl;
theta=vds/eta;
//cout<<"theta="<<theta<<endl;
y0=sqrt(x2+root*theta);
//cout<<"y0= "<<y0<<endl;
y1=sqrt(x3-root*theta);
//cout<<"y1= "<<y1<<endl;
y2=sqrt(vds+x3-root*theta);
//cout<<"y2= "<<y2<<endl;

x4=x0*y1;
x5=x0*y2;
//effective length under gate control
x6=f*l-x4-x5;
//cout<<"x4= "<<x4<<" x5= "<<x5<<" l= "<<f*l<<endl;
if(x6>=1e-08)
{
y3=sqrt(1+x1*y0);
//cout<<"y3= "<<y3<<endl;
```

```
y4=y1*y3/y0;
//cout<<"y4= "<<y4<<endl;
y5=(f*l-x0*y2)*y3/(x0*y0);
//cout<<"y5= "<<y5<<endl;
y6=sinh(y4);
y7=cosh(y5);
y8=cosh(y4);
//cout<<"y8= "<<y8<<endl;
//xl=(2*chi*eta*y3*y6/(y7-y8));
//cout<<"xl= "<<xl<<endl;
y9=root-(2*chi*eta*y3*y6/(y7-y8));
//cout<<"y9= "<<y9<<endl;
}
else
{cout<<"punch through"<<endl;}
return(y9);
}
//bisec. method for finding the root of above function
long double bisec(long double z1,long double z2)
{
long double y1,y2,y3,z3;
do
{
y1=fabsl(n(z1));
```

```
y2=fabsl(n(z2));
z3=(z1+z2)/2;
y3=fabsl(n(z3));
if(y1>y2)
{
z1=z3;
}
else
{
z2=z3;
}
}
while(y3>1e-06);
return (z3);
}

void main()
{
clrscr();
ofstream fout("tvs.dat");
long double na,phi,tox,eox,es,un,t,ni,k,q,nd,qss;
long double e,xr,sigma,dvt,vdsf;
long double qtotf,coxf,vtf,naf;
long double b,Dn,phib,vbi,qtot,cox,vgs,vt,delta,psios,xs,xd;
```

```
long double g;

long double root1,root2;

long double vto;


l=10e-07; na=0.5e23; nd=1e25; tox=30e-09; eox=4*8.854e-12;

es=11.8*8.854e-12; un=0.06; t=300; ni=1.5e16; chi=0.5;

//eta=1.5;

qss=1.6e-05; q=1.602e-19; k=1.38e-23;


b=k*t/q;

cox=eox/tox;

vbi=b*log(na*nd/(ni*ni));


for(f=0.3;f<=0.7;f+=0.1)

{

coxf=cox/f;


//cout<<"naf= "<<naf<<endl;

naf=na/f;

phibf=b*log(naf/ni);

//cout<<"phibf= "<<phibf<<endl;

phi=-0.56-phibf;

vbif=b*log(naf*nd/(ni*ni));

//cout<<"vbif= "<<vbif<<endl;
```

```
qtot=sqrtl(4*es*q*naf*phibf);
//cout<<"qtot= "<<qtot<<endl;
vto=phi-qss/coxf+2*phibf+qtot/coxf;
cout<<"vto= "<<vto<<endl;
vdsf=12;
for(vds=1;vds<=f*vdsf;vds+=20)
{
//for(vgs=-vto;vgs<=vto;vgs+=1.5)
//{
vgs=0;
vgto=vgs-vto;

x0=sqrt(2*es/(q*naf));
//cout<<"x0= "<<x0<<endl;
x1=coxf*x0/es;
//cout<<"x1= "<<x1<<endl;
xy=1/(x1*sqrt(2*phibf));
//cout<<"xy= "<<xy<<endl;
xz=1+xy;
//cout<<"xz= "<<xz<<endl;

/*
for(root1=0;root1<=0.1;root1+=1e-08)
{
```

```
cout<<"vds= "<<vds<<" root= "<<root1<<" func= "<<n(root1)<<endl;
}
*/
root1=0; root2=0.3;
//cout<<"vds= "<<vds<<" sigma= "<<bisec(root1,root2)<<endl;
sigma=bisec(root1,root2);
cout<<"tvs= "<<-sigma*vds<<endl;
xr=(vgto+sigma*vds)/(phibf);
cout<<"\nxr= "<<xr<<endl;
e=xz+sqrt((xz*xz)-xy*xr);
cout<<"\neta= "<<eta<<endl;
//}
}
}
getch();
}
```

Program D.2: Determination of drain source voltage as function of threshold voltage shift across a transistor in a circuit.

```
#include<iostream.h>
#include<math.h>
#include<conio.h>
#include<fstream.h>
long double vds,vgs,vdd,vto;
//function to determine threshold voltage shift using appendix-C.
long double g(long double root)
{
long double m1,m2,c1,dvt1,dvt2,y;
vds=vdd;
//vds=vdd-vto-root;
//cout<<"vds= "<<vds<<endl;
vgs=0;
//cout<<"x0= "<<vgs<<endl;
m1=0.0026*pow(vds,3)-0.0031*pow(vds,2)+0.0042*pow(vds,1);
//cout<<"x0= "<<m1<<endl;
c1=-0.0025*pow(vds,3)-0.0012*pow(vds,2)-0.0037*pow(vds,1);
//cout<<"x0= "<<c1<<endl;
m2=0.0168*pow(vgs,2)+0.004*pow(vgs,1)-0.0252;
//cout<<"x0= "<<m2<<endl;
dvt1=m1*vgs+c1;
//cout<<"x0= "<<dvt1<<endl;
```

```
dvt2=m2*vds;
//cout<<"x0= "<<dvt2<<endl;
y=root-((dvt1+dvt2)/2);
//cout<<"x0= "<<y<<endl;

return(y);
}

long double bisec(long double z1,long double z2)
{
long double y1,y2,y3,z3;
do
{
y1=fabsl(g(z1));
y2=fabsl(g(z2));
z3=(z1+z2)/2;
y3=fabsl(g(z3));
if(y1>y2)
{
z1=z3;
}
else
{
z2=z3;
```

```
}
}
while(y3>1e-04);
return (z3);
}

void main()
{
clrscr();

long double root1,root2,dvt;
vdd=1;vto=0.666848;
cout<<vdd<<vto<<endl;
root1=-0.1; root2=0;
//cout<<" dvt= "<<g(root1)<<endl;
cout<<" dvt= "<<bisec(root1,root2)<<endl;
dvt=bisec(root1,root2);
vds=vdd-vto-dvt;
cout<<"vds= "<<vds<<endl;
getch();
}
```

Program D.3: Determination of power dissipation in an NMOS transistor.

```
#include<iostream.h>
#include<math.h>
#include<conio.h>
#include<fstream.h>
//channel potential at any point x
#define v(x) (vo*sinh(x/lambda))

void main()
{
clrscr();
ofstream fout("c1.dat");
long double w,l,na,nd,phi,tox,eox,es,un,t,ni,chi,qss,q,k,A,h,me;
long double eta,x0,x1,xy,xz,xw;
long double idd,ite,idt,id,it,ido,d,i1,i2,i3,pd,pdm;
long double f,phibf,qtotf,vbif,coxf,naf,pf,vdsf;
long double b,Dn,cox,vgs,vds,vto,dvt,vt,vgt;
long double delta,Io,psios,xs,xd,dodep,lambda,vo,c,x;
long double bp,an,b1,b2,eb,a,alpham,betam,alphab,betab,term,em,m;

w=3e-06; l=1e-06; na=0.5e23; nd=1e25; tox=30e-09; eox=4*8.854e-12;
es=11.8*8.854e-12; un=0.06; t=300; ni=1.5e16;
chi=0.5; qss=1.6*1e-05; q=1.602*1e-19;k=1.38e-23;
an=7.03e+07; bp=1.58e+08; b1=1.23e+08; b2=2.04e+08; eb=3e+07;
```

```
h=6.64e-34;me=1.1*9.1e-31;
A=4*3.14*me*q*k*k/(h*h*h);
//cout<<" A= "<<A<<endl;

b=k*t/q;
Dn=b*un;
cox=eox/tox;
alphab=an*expl(-b1/eb);
betab=bp*expl(-b2/eb);

for(f=0.3;f<=1;f+=1)
{
coxf=cox/f;

naf=na/f;
pf=es/(q*naf);

phibf=b*log(naf/ni);
//cout<<"phibf= "<<phibf<<endl;
phi=-0.56-phibf;
vbif=b*log(naf*nd/(ni*ni));
//cout<<"vbif= "<<vbif<<endl;
qtotf=sqrtl(4*es*q*naf*phibf);
//cout<<"qtot= "<<qtot<<endl;
```

```
vto=phi-qss/coxf+2*phibf+qtotf/coxf;

cout<<"vto= "<<vto<<endl;

//enter val. of threshold voltage shift as obtained from program 2.

dvt=-0.029499;

vt=vto+dvt;

vdsf=12;

vds=1;


vgs=0;

vgt=vgs-vt;

x0=sqrt(2*es/(q*naf));

//cout<<"x0= "<<x0<<endl;

x1=coxf*x0/es;

//cout<<"x1= "<<x1<<endl;

xy=1/(x1*sqrt(2*phibf));

//cout<<"xy= "<<xy<<endl;

xz=1+xy;

//cout<<"xz= "<<xz<<endl;

xw=vgt/phibf;

cout<<"xw= "<<xw<<endl;

eta=xz+sqrt((xz*xz)-xy*xw);

cout<<"\neta= "<<eta<<endl;


delta=b*sqrtl(es/(2*q*naf*(2*phibf+vgt/eta)));
```

```
psios=-vbif+2*phibf+vgt/eta;
//r=-psios/phibf;
xs=sqrtl(2*es*(-psios)/(q*naf));
dodep=sqrtl(2*es*(psios+vbif)/(q*naf));
lambda=dodep/sqrtl(1+eox*dodep/(es*f*tox));
//cout<<" psios="<<psios<<"xs= "<<xs<<" dodep= "<<dodep<<" lambda=
"<<lambda<<endl;

xd=sqrtl(2*es*(vds-psios)/(q*naf));
//cout<<"xd= "<<xd<<endl;
c=lambda*coshl((f*l-xd)/lambda)-lambda*coshl(xs/lambda);
//cout<<"c= "<<c<<endl;
vo=2*chi*vds*dodep/c;
//cout<<"vo= "<<vo<<endl;

a=2/pf*(vds+psios+vbif);
em=sqrtl(a);
//cout<<"electric field = "<<em<<endl;
alpham=an*expl(-b1/em);
betam=bp*expl(-b2/em);
term=(alpham/(betam-alpham))*(expl((betam-alpham)*log(alphab/betab)*em/(eb*(alphab-
betab)))-1);
m=1/(1-term);
```

```
ido=q*nd*f*w*delta*Dn*vo/(lambda*b);

d=1-expl(-vo*(f*l-xs-xd)/(b*lambda));

//cout<<d;

id=expl((psios+v(xs))/b)*(1-expl(-vds/b));

//cout<<" "<<id;

//drift-diffusion current

idd=ido*id/d;


Io=f*w*delta*A*t*t;

//thermionic current

ite=Io*id;

//total current

idt=1/((1/idd)+(1/ite));

//pd=idt*vds;

//cout<<"pd= "<<pd<<endl;

//i1=idd*m;

//i2=ite*m;

//total current considering multiplication

i3=idt*m;

// power dissipation considering multiplication

pdm=i3*vds;

//cout<<"pdm= "<<pdm<<endl;


//fout<<"  "<<vds<<"      "<<idt<<"      "<<"      "<<i3<<endl;
```

```
//fout<<f<<"  "<<dvt<<"  "<<vds<<"  "<<pd*2<<"  "<<m<<"
"<<pdm*2<<endl;
//fout<<"  "<<vds<<"  "<<pdm<<endl;
//fout<<"  "<<f<<"  "<<idt*vds<<"  "<<i3*vds<<endl;
/*
cout<<"alpham= "<<alpham<<" betam= "<<betam<<endl;
cout<<"em= "<<em<<endl;
cout<<" xd= " <<xd<<endl;
cout<<" ido= "<<ido<<endl;
cout<<" idden= "<<d<<" id= "<<id<<endl;*/
//cout<<" idt= "<<idt<<endl;
//cout<<"i3= "<<i3<<endl;
//cout<<"m= "<<m<<endl;
cout<<" "<<endl;
}


//}
//}
getch();
}
```

Program D.4: Detemination of PMOS power dissipation.

```
#include<iostream.h>
#include<math.h>
#include<conio.h>
#include<graphics.h>
#include<fstream.h>
//channel potential at any point x
#define v(x) (vo*sinh(x/lambda))

void main()
{
clrscr();
ofstream fout("cp.dat");
long double w,l,na,nd,phi,tox,eox,es,up,t,ni,chi,qss,q,k,A,h,mh;
long double eta,x0,x1,xy,xz,xw;
long double idd,ite,idt,id,it,ido,d,i1,i2,i3,pd,pdm;
long double f,phibf,qtotf,vbif,coxf,ndf,pf,vdsf;
long double b,Dp,cox,vgs,vds,vto,vtp,dvt,vt,vgt;
long double delta,Io,psios,xs,xd,dodep,lambda,vo,c,x;
long double bp,an,b1,b2,eb,a,alpham,betam,alphab,betab,term,em,m;

w=3e-06; l=1e-06; nd=0.5e23; na=1e25; tox=30e-09; eox=4*8.854e-12;
es=11.8*8.854e-12; up=0.02; t=300; ni=1.5e16;
chi=0.5; qss=1.6*1e-05; q=1.602*1e-19;k=1.38e-23;
```

```
an=7.03e+07; bp=1.58e+08; b1=1.23e+08; b2=2.04e+08; eb=3e+07;

h=6.64e-34;mh=0.549*9.1e-31;

A=4*3.14*mh*q*k*k/(h*h*h);

//cout<<" A= "<<A<<endl;


b=k*t/q;

Dp=b*up;

cox=eox/tox;

alphab=an*expl(-b1/eb);

betab=bp*expl(-b2/eb);


for(f=0.4;f<=1;f+=1)

{

coxf=cox/f;

ndf=nd/f;

pf=es/(q*ndf);


phibf=-b*log(ndf/ni);

//cout<<"phibf= "<<phibf<<endl;

phi=0.56-phibf;

vbif=-b*log(ndf*na/(ni*ni));

//cout<<"vbif= "<<vbif<<endl;

qtotf=-sqrtl(4*es*q*ndf*-phibf);

//cout<<"qtot= "<<qtot<<endl;
```

```
vtp=phi+qss/coxf+2*phibf+qtotf/coxf;

cout<<"vto= "<<vtp<<endl;

vto=-vtp;

//enter dvt val.

dvt=-0.009541;

vt=vto+dvt;

vdsf=12;

vds=0.534119;


vgs=0;

vgt=vgs-vt;

x0=sqrt(2*es/(q*ndf));

//cout<<"x0= "<<x0<<endl;

x1=coxf*x0/es;

//cout<<"x1= "<<x1<<endl;

xy=1/(x1*sqrt(2*-phibf));

//cout<<"xy= "<<xy<<endl;

xz=1+xy;

//cout<<"xz= "<<xz<<endl;

xw=vgt/-phibf;

//cout<<vgt<<endl;

eta=xz+sqrt((xz*xz)-xy*xw);

//cout<<"\neta= "<<eta<<endl;
```

```
delta=b*sqrtl(es/(2*q*ndf*(2*-phibf+vgt/eta)));
psios=vbif-2*phibf+vgt/eta;
//cout<<"psios"<<psios<<endl;
xs=sqrtl(2*es*(-psios)/(q*ndf));
dodep=sqrtl(2*es*(psios-vbif)/(q*ndf));
lambda=dodep/sqrtl(1+eox*dodep/(es*f*tox));
//cout<<"  psios="<<psios<<"xs=  "<<xs<<"  dodep=  "<<dodep<<"  lambda=
"<<lambda<<endl;
xd=sqrtl(2*es*(vds-psios)/(q*ndf));
//cout<<"xd= "<<xd<<endl;
c=lambda*coshl((f*l-xd)/lambda)-lambda*coshl(xs/lambda);
//cout<<"c= "<<c<<endl;
vo=2*chi*vds*dodep/c;
//cout<<"vo="<<vo<<endl;

a=2/pf*(vds+psios-vbif);
em=sqrtl(a);
//cout<<"electric field= "<<em<<endl;
alpham=an*expl(-b1/em);
betam=bp*expl(-b2/em);
term=(betam/(alpham-betam))*(expl((alpham-betam)*log(alphab/betab)*em/(eb*(alphab-
betab)))-1);
m=1/(1-term);
```

```
ido=q*na*f*w*delta*Dp*vo/(lambda*b);

d=1-expl(-vo*(f*l-xs-xd)/(b*lambda));

//cout<<d;

id=expl((psios+v(xs))/b)*(1-expl(-vds/b));

//cout<<" "<<id;

idd=ido*id/d;


Io=f*w*delta*A*t*t;

ite=Io*id;


idt=1/((1/idd)+(1/ite));

pd=idt*vds;

cout<<"pd= "<<pd<<endl;

//i1=idd*m;

//i2=ite*m;

i3=idt*m;

pdm=i3*vds;

cout<<"pdm= "<<pdm<<endl;

fout<<f<<"  "<<vds<<"  "<<dvt<<"  "<<pd<<"  "<<m<<"  "<<pdm<<endl;

cout<<" idd= "<<idt<<endl;

cout<<"ite= "<<i3<<endl;

cout<<"m= "<<m<<endl;

cout<<" "<<endl;

}
```

```
getch();
}
```

Program D.5: Determination of node probabilities and correlation coefficients at reconvergent nodes.

```
#include<iostream.h>
#include<math.h>
#include<conio.h>
#include<fstream.h>
float pq,pqb,cxqb,cyq,a,b,c,d,h;
void main()
{
clrscr();
//initial values of node probabilities and correlation coefficients.
pq=0;pqb=0;cxqb=0;cyq=0;h=1e-04;
do
{
a=pq;b=pqb;
//calculation of node probabilities and correlation coefficients
pq=1-0.75*pqb*cxqb;
pqb=1-0.75*pq*cyq;
cxqb+=h;cyq+=h;
c=fabs(a-pq);
d=fabs(b-pqb);
}
while(c>1e-06 && d>1e-06);
```

```
cout<<pq<<" "<<pqb<<" "<<cxqb<<" "<<cyq<<endl;
getch();
}
```

Program D.5: Determination of node probabilities and correlation coefficients at reconvergent nodes.

```
#include<iostream.h>
#include<math.h>
#include<conio.h>
#include<fstream.h>
float pq,pqb,cxqb,cyq,a,b,c,d,h;
void main()
{
clrscr();
//initial values of node probabilities and correlation coefficients.
pq=0;pqb=0;cxqb=0;cyq=0;h=1e-04;
do
{
a=pq;b=pqb;
//calculation of node probabilities and correlation coefficients
pq=1-0.75*pqb*cxqb;
pqb=1-0.75*pq*cyq;
cxqb+=h;cyq+=h;
c=fabs(a-pq);
d=fabs(b-pqb);
}
while(c>1e-06 && d>1e-06);
```

```
cout<<pq<<" "<<pqb<<" "<<cxqb<<" "<<cyq<<endl;
getch();
}
```