ANALYTICAL MODELING OF DOUBLE GATE FinFET AND ITS APPLICATIONS TO SRAM CELL DESIGN

A THESIS

Submitted in partial fulfilment of the requirements for the award of the degree

of

DOCTOR OF PHILOSOPHY

in

ELECTRONICS AND COMPUTER ENGINEERING

by

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DECEMBER, 2009

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I hereby certify that the work which is being presented in the thesis entitled "ANALYTICAL MODELING OF DOUBLE GATE FinFET AND ITS APPLICATIONS TO SRAM CELL DESIGN" in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electronics and Computer Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from July 2006 to December 2009 under the supervision of **Dr. A. K. Saxena**, Professor and **Dr. S. Dasgupta**, Assistant Professor, Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee, Roorkee.

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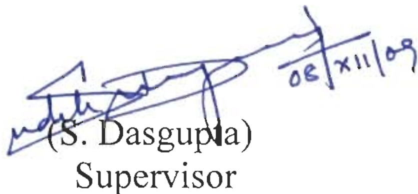

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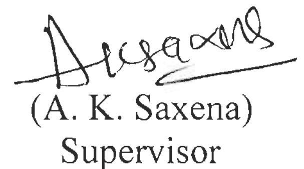

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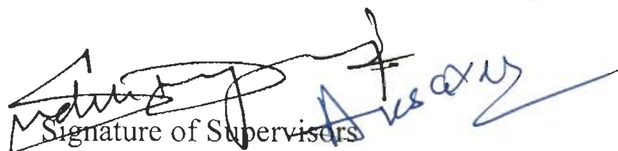

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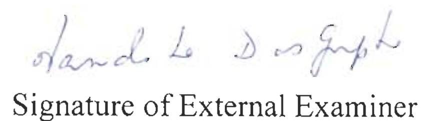

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Abstract

Transistor dimensions have been scaled down to nanoscale dimensions to enhance the driving capability and switching speed. International Technology Roadmap for Semiconductor (ITRS)-2007 report shows an industry wide consensus on the "best current estimate" of the industry's research and development needs. Silicon has taken a vital role in semiconductor industry while III-V semiconductor devices play a major role for various electronics applications. The limiting factors in the bulk MOSFET downscaling is the power consumption due to Short Channel Effects (SCEs), leakage current and subthreshold slope degradation. Novel devices are being investigated very rigorously to continue the scaling trends. In the device research community, researchers are looking for such a device which has low leakage and low threshold voltage without compromising on performance, resulting in multiple gate structures. Such examples are the Double Gate MOSFET and FinFET device. A self aligned Double Gate (DG) FinFET reduces leakage currents, process parameter variations and also eliminates short channel effect.

This thesis deals with modeling and simulation of FinFET device and subsequent application to the design of FinFET based 6T-SRAM cell as well as analysis of design issues and performance metrics. In this thesis, an extensive literature survey of the state of the art in the area of study is presented. Many important research papers are referred and cited which allows one to fully appreciate the usefulness of such novel devices in present day circuits. Various research gaps are also investigated.

One dimensional potential modeling of single or double gate MOSFET is not enough to explain its various physical facts within the device in nanoscale regime. At extremely low dimensions, electric field in both longitudinal and transverse directions becomes substantially large. Hence, two dimensional (2D) device modeling is required to enhance the accuracy of the results. 2D models gives a more accurate result but at the cost of the computation time. The Quantum Mechanical (QM) analytical modeling of potential for the FinFET device under study carried out. This gives closed form solution of surface potential.

Further, the threshold voltage evaluation becomes an important issue in order to undertake power dissipation characteristics. Hence extractions of threshold voltage and parasitic source/drain resistance modeling have been also carried out in order to understand the switching behaviour of the device. Various potential profiles such as surface potential, front gate to back gate potential, source to drain potential and 3D potential plot for the FinFET device under study have also been presented. Key issues including FinFET device structure, design parameters, potential modeling, process parameter variation effects and device scaling limit have been undertaken quantitatively as well as qualitatively. The results obtained on the basis of our proposed analytical model have been compared and contrasted with the reported experimental results and a close match was found.

The analytical modeling for Quantum mechanical (QM) inversion charge, field dependent mobility and drain current for nanoscale Double Gate (DG) FinFET have been evaluated. As the device dimensions are excessively reduced and the dimensions of the device becomes of the order of the de-Broglie wavelength of electron, it is imperative to undertake an extensive Quantum Mechanical (QM) modeling for the device under study. An extensive analytical modeling of FinFET

device has been carried out for extracting QM inversion charge. Analytical model has been developed to estimate the drain current. Further, variation of drain current with various process/device parameters is carried out for the FinFET device structure under study. The effect of fin thickness (T_{fin}) and fin height (H_{fin}) on drain current has been modeled and discussed. In order to evaluate the output drain current, a comprehensive mobility model for the charge carriers has been carried out. Various mobility models have been studied and implemented during the course of work and appropriate mobility model is taken up in order to evaluate the drain current. The results obtained on the basis of our model are compared with our TCAD Sentaurus simulation result as well as reported experimental results for the purpose of validation.

The analytical modeling and estimation of various types of leakage currents associated with the FinFET device are presented, as low leakage devices are required for low power consumption for various applications. The various leakage current components in FinFET device have been evaluated such as subthreshold leakage current, gate tunneling leakage current and its dependence on various device/process parameters. The subthreshold leakage current is primarily due to diffusion of carriers and has been modeled analytically. Gate to channel leakage is primarily due to tunneling of electrons from inverted surface channel to gate. We have also analytically calculated subthreshold swing for FinFET to evaluate the subthreshold leakage current. As the device dimensions are reduced, the off state leakage current substantially increases because of many QM effects. This result in larger power dissipation of the device and the matter assumes critical importance in SRAM, as FinFET SRAM designs are prone to larger power dissipation. The results obtained have shown that at same technology node, the leakages in FinFETs are lower as

compared to DG-MOS devices. Further, our analysis shows the improvement in the performance due to reduction in leakage current of FinFET device.

It can be appreciated that the devices by themselves don't add to the existing integration era. But until, a circuit analysis using the proposed devices is undertaken, the full benefits of integration cannot be captured. Logic and memory circuit design in nanoscale regime requires control over leakage currents with device level parameter variations. FinFET based 6T SRAM cell design using device/circuit co-design approach also carried out. Our analysis shows that use of FinFET devices with intrinsic body doping reduces leakage current and short channel effects. Hence, we conclude that FinFET devices can emerge as one of the promising candidate for reducing leakage components with minimum body transition time, making it efficient for low power and high performance circuit design in nanoscale regime. Further, FinFET based SRAM cell usually uses the smallest device on chip packed very closely together to achieve high density. Thus they are more sensitive to process variations.

The FinFET based 6T SRAM cell uses cross coupled inverter structure to store bits. The mismatch between cell devices can cause data flipping during read operation. Thus the primary goal of the proposed design includes maximizing stability and minimizing leakage in SRAM, besides achieving maximum density. Design considerations for maximizing performance and yield of FinFET-based 6-T SRAM at the 32 nm have been examined. It is shown that, FinFET based SRAM cells have enhanced performance over planar bulk-Si MOSFET SRAM cells. Our proposed FinFET based 6T-SRAM cells have improved the 'read' and 'write' margin, without compromising on the area requirement. The simulations have been carried out in HSPICE with appropriate structuring of model file containing various device

parameters both independent and extracted. The analysis for the performance metric of FinFET based SRAM cell such as SNM, RNM, WNM, power, delay have been also carried out.

Our analysis shows that, use of FinFET device with intrinsic body reduces leakage current and enhances the driving capability. Hence, we conclude that FinFET can emerge as one of the promising candidate for reducing leakage components making it efficient for low power and high performance SRAM cell design in nanoscale regime.

Acknowledgement

I wish to express my heartfelt regards and gratitude to Dr. S. Dasgupta, Assistant Professor and Dr. A. K. Saxena, Professor, Semiconductor Devices and VLSI Technology (SDVT) Group, Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee for their invaluable guidance and inspiration in successful completion of the present work. Their creative ideas, constant monitoring research activities, hardworking nature, encouragement and moral support were extremely beneficial for this research work. With their wide experience, sharp and incisive intellect, maestro ability combined with astute research methodology and deep insight of subject have unerringly steered the work on smooth and steady course. I sincerely appreciate their pronounced individualities, humanistic and warm personal approach which have given me the strength and will to carry this research work. I humbly acknowledge a lifetime deep gratitude to my supervisors.

I am thankful to Dr. S. Manhas and Dr. Anand Bulusu, Asst. Professors, SDVT Group, E & CE, IIT Roorkee for providing guidance and support. I am also grateful to Dr. S. N. Sinha, Professor and Head, E & CE, DRC Chairman, Prof. R. Mitra, Prof. M. J. Nigam, Professor, E & CE, Prof. R. Nath, Department of Physics for being member of my research committee and sparing their time for critically examining the work and providing valuable suggestions.

My sincere thanks to Mr. Naveen and Mr. Dinesh Sharma, SDVT Group, E & CE, IIT Roorkee for their constant help during the research work. I would like sincerely thank to research scholars of SDVT group, Jitendra Kanungo, R. S. Rathod, Ramesh Vaddi, Gaurav Koshal and M. Tech. friends for discussing technical

problems. My sincere thanks to my Ph.D. seniors of SDVT group Mr. S. K. Visvakarma and Dr. Brajesh Kaushik for guiding me at various stages of research. I also want to express my sincere thanks to my friends Dr. Gaurav Raheja, Dr. Samarjeet Rawat, Dr. Nilesh Sharma, Dr. Vikas Chawla, Dr. Ramesh Sunkaria and many more those who helped me directly or indirectly in various aspects to improve the quality of thesis and pleasant stay in IIT campus. Special thanks to my friends Vinod, B.B Gupta, Rajiv, Balwinder Singh, Pushpinder Singh and RK.Vishvakarma who always encouraged me throughout research tenure.

My special thanks and heartfelt gratitude goes to Mrs. T. Dasgupta and Mrs. Shobha Saxena for ever making me feel owned, loved and a part of their families.

Finally, I wish to express my sincere appreciation to my father Shri. Krishan Lal, mother Smt. Parkasho Rani, my elder brothers Balwan Chand and Balwant Raj, my family and relatives without their efforts, cooperation and support this research effort would not have been possible.

This thesis is dedicated to my teachers and family.

Date:

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List of Symbols

L_{eff}	Effective Channel Length
L_g	Physical Gate Length
H_{fin}	FinFET Height
T_{fin}	FinFET Thickness
t_{ox}	Equivalent Oxide Layer Thickness
Λ	Scale Length
q	Electronic Charge
N_A	Channel Doping Concentration
$N_{D/S}$	Drain/Source Doping Density
n_i	Intrinsic Carriers Concentration
ε_{si}	Silicon Permittivity
ε_{ox}	Oxide Permittivity
ε_{ins}	Insulator Permittivity
ψ_s	Surface Potential
ψ_o	Centre Potential
φ	Electron Wave Function
V_{gs}	Gate Voltage
V_{ds}	Applied Drain to Source Voltage
V_S	Potential at Source Terminal
V_{bi}	Built in Potential
V_{FB}	Flat Band Voltage

V_T	Thermal Voltage
V_{th}	Threshold Voltage of the Device
ΔV_{th}	Threshold Voltage Roll-off
$V_{th,QM}$	Quantum Mechanical Threshold Voltage
I_{ds}	Channel Current from Drain to Source
I_{sub}	Subthreshold Current
C_{ox}	Capacitance of Oxide Layer Per Unit Area
k_B	Boltzman's Constant
E_g	Band Gap Energy
$E_{G(ins)}$	Energy Band Gap for Insulators
E_{ins}	Electric Field in the Insulator Region
E_F	Fermi Energy Level
E_{eff}	Effective Electric Field
Q_b	Bulk Charge
q_i	Inversion Charge
C_{ins}	Insulator Capacitance
C_{si}	Channel Capacitance
C_g	Gate Capacitance
C_{dep}	Depletion Capacitance
m_{ox}	Electron Effective Mass of Insulators
m_o	Free Electron Mass
m_t^*	Effective Mass of Electron in Transverse Direction
m_l^*	Effective Mass of Electron in Longitudinal Direction

h	Planck's Constant
μ_n	Mobility of Electron
μ_p	Mobility of Hole
μ_{eff}	Effective Mobility
v	Channel Potential
S	Subthreshold Slope
S_f	Subthreshold Slope Factor
T	Temperature
η	Fitting Parameter
X_j	Source/Drain Junction Depth
ρ_{int}	Contact Resistivity
ρ_{ext}	Resistivity of the S/D Extension
L_{ext}	Length of the Fin Extension Region
T_{poly}	Thickness Ploysilicon Layer

List of Abbreviations

AC	Access
BL	Bit Line
BOX	Buried Oxide
CMOS	Complementary Metal Oxide Semiconductor
CR	Cell Ratio
DG	Double Gate
DIBL	Drain Induced Barrier Lowering
DOS	Density of States
DRAM	Dynamic Random Access Memory
EC	Electrical Confinement
EOT	Effective Oxide Thickness
FDSOI	Fully Depleted Silicon-On-Insulator
FinFET	Fin Field Effect Transistor
GAA	Gate-All-Around
GIDL	Gate Induced Drain Lowering
HDD	Heavily Doped S/D
IC	Integrated Circuits

ITRS	International Technology Roadmap for Semiconductor
MOSFET	Metal Oxide Semiconductor Field effect Transistor
MuGFET	Multi Gate Field Effect Transistor
PD	Pull Down
PDSOI	Partially Depleted Silicon-On-Insulator
PTM	Predictive Technology Model
PU	Pull Up
QG MOS	Quadruple Gate MOS
QME	Quantum Mechanical Effects
R&D	Research and Development
RDF	Random Dopant Fluctuations
RNM	Read Noise Margin
S/D	Source/Drain
SC	Structural Confinement
SCEs	Short Channel Effects
SNM	Static Noise Margin
SoC	System on Chip
SOI	Silicon on Insulator
SP	Schrodinger-Poisson

SRAM	Static Random Access Memory
ULSI	Ultra Large Scale Integration
UTB	Ultra Thin Body
VTC	Voltage Transfer Characteristics
VLSI	Very Large Scale Integration
WL	World Line
WNM	Write Noise Margin

Chapter 1

Introduction

1.1 Introduction

Continued miniaturization of bulk silicon Complementary Metal Oxide Semiconductor (CMOS) transistors is being limited by Short Channel Effects (SCE's). SCE is the decrease of the MOSFET threshold voltage as the channel length is reduced. Other SCE's are mobility degradation and Drain Induced Barrier Lowering (DIBL). Higher channel doping, shallower source/drain junctions and thinner gate dielectrics have been employed to improve gate control and enhance performance as the gate length is scaled down [40]. However, these techniques are rapidly approaching present material and process limits. Alternate transistor architectures such as the planar Ultra-Thin Body (UTB), Double-Gate Metal Oxide Semiconductor Field Effect Transistor (DG MOSFET) and Fin Field Effect Transistor (FinFET) may be necessary to continue gate length scaling down to the sub-32 nm regime [20, 80].

The silicon-based microelectronics industry has been growing rapidly for the past four decades following Moore's law of scaling [45, 46]. However, fundamental physical limits are nearly at the end of conventional linear scaling of transistor dimensions and the new era of MOS scaling constrained by power dissipation and process-induced variations. FinFET is the most promising double-gate structure for integrated circuit manufacturing [62] in the near future. With MOSFET as an unit component of most high-performance ICs, the focus is on developing transistors that are faster and smaller than their predecessors, maintaining a high degree of reliability

and low cost. These often-conflicting goals are the driving force behind transistor research in academia and industry. With many groups working on near and long-term solutions to the demands of the IC industry, one type of device has garnered attention of some prominent researchers and industry heavyweights – the FinFET. This device presents a solution that promises excellent performance and scalability, while carrying with it a great degree of risk in a manufacturing environment or fabrication [27, 43].

Fundamental changes in device architecture may be necessary to continue scaling trends with thin-body MOSFETs such as UTB-FETs and FinFETs emerging as leading contenders. Constant scaling of CMOS devices is the well-known driver of advancement and growth in the microelectronic industry with today's advanced technology delivering high-performing devices at the 90nm and 65nm technology nodes [57, 60, 90]. A major problem in scaling MOS devices with nanoscale gate length is the difficulty in controlling the leakage current when the device is switched off. In standard planar MOS technology, doping profile may be used to mitigate part of this problem. But the drawback of increased channel doping would result in reduction of mobility and hence the driving capability of the device. One can reduce the oxide layer thickness to maintain the device performance but below a certain limit, the gate leakage current exceeds more than the tolerance limit. Advanced devices have focused on highly confined channel to improve source-drain isolation. Practical structures utilize a vertical configuration such as FinFET [29], also known as trigate MOSFET. Such devices in general provide a good source to drain isolation but offer somewhat moderate current rate [16].

Semiconductor memory arrays capable of storing large quantities of information are essential to all digital system. The amount of memory required in a particular system depends on the type of application with the requirement of high

density on-chip memory for digital systems. Conventional MOS based memory would not be able to meet such demand due to reasons stated earlier such as SCEs, leakage, power dissipation etc. Hence, the requirement of FinFET as memory element would be essential to mitigate above problems. The ever increasing demand for large storage capacity has driven the fabrication technology and memory development towards more compact design rules and consequently towards higher data storage densities. On-chip memory arrays have become widely used subsystems in VLSI circuits and commercially available single chip read/write memory capacity has reached more than 2 GB [36, 55].

The semiconductor memory is generally classified according to the type of data storage and data access. Read/Write memory or Random Access Memory (RAM) must permit the modification of data bits stored in the memory array, as well as their retrieval demand [39]. Based on the operation type of individual data storage cells, RAMs are classified into two main categories:

1. Dynamic RAM (DRAM)
2. Static RAM (SRAM).

As the continuing trend for high-density memories favors small memory cell sizes, the dynamic RAM cell with a small structure has become a popular choice, where binary data are stored as a charge in a capacitor and the presence or absence of stored charge determines the value of the stored bit. The data stored in a capacitor cannot retain indefinitely, because the leakage currents eventually remove or modify the stored data. Thus the DRAM cell requires a periodic refreshing of the stored data, so that unwanted modifications due to leakage are prevented before they occur [22]. The usage of a capacitor as a primary storage device generally enables the DRAM cell to be realized in a much smaller silicon area compared to the typical SRAM cell.

The FinFET based SRAM cell consists of latch so the cell data is kept as long as power is turned on and refresh operation is not required. SRAM is mainly used for the cache memory in microprocessor, mainframe computers, engineering workstations and memory in handheld devices due to its high speed and low power consumption. Memories are said to be static if no periodic clock signals are required to refresh and retain the stored data indefinitely. Memory cells in these circuits have a direct path to supply or ground or both. Read-Write memory cell arrays based on flip-flop circuits are commonly referred to as SRAMs. The FinFET based SRAM cell consists of two cross-coupled inverters and two access transistors. The access FinFET's are connected to the wordline at their respective gate terminals and the bitlines at their source/drain terminals. The wordline is used to select the cell while the bitlines are used to perform read or write operations on the cell. Internally, the cell holds the stored value on one side and its complement on the other side. The two complementary bitlines are used to improve speed and noise rejection properties [41, 90].

This chapter provides an introduction and brief idea about the whole work carried in this thesis. Section 1.1 deals with introduction and international technology roadmap for semiconductor with reference to ITRS-2007 report, section 1.2 describes the scaling of semiconductor devices. Section 1.3 gives the motivation behind the research work carried. Further, section 1.4 deals with the problem description and section 1.5 describe the thesis organization. The conclusion of this chapter is drawn in section 1.6.

In particular, the International Technology Roadmap for Semiconductors (ITRS) has identified several types of devices such as Ultra Thin Body (UTB), Double Gate MOSFET and FinFET that could augment or eventually replace classical

CMOS devices. The Emerging Research Devices section of the ITRS report [65] discusses several emerging technologies including UTB multiple gate field effect transistors.

All of these improvement trends, sometimes called "scaling" trends, have been enabled by large R&D investments. In the last two decades, the growing size of the required investments has motivated industry collaboration with many R&D partnerships and other cooperative ventures. The ITRS has been successful worldwide cooperation endeavor. It presents an industry-wide consensus on the "best current estimate" of the industry's research and development needs to a 15-year horizon. As such, it provides a guide to the efforts of companies, research organizations and governments. The ITRS has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that truly need research breakthroughs. ITRS to large extent helps to do technology forecasting within semiconductor industry as well as in academic domain.

1.2 Scaling of Semiconductor Devices

Moore's law describes the rate of increase in transistor density with progressing years as shown in figure 1.1. Reduction of the physical MOS device dimensions have improved both circuit speed and density [46, 58]. The major aim of pursuing Moor's law or finding alternative solution is to further increase the performance. It can be inferred from figure 1.1 that:

a) Circuit operational frequency 'f' increases with a reduction in gate length, L_g, as $\sim 1/L_g$; allowing for faster circuits,

b) It can be shown that chip area decreases (due to increased density) as ~ L_g^2; enabling higher transistor density and cheaper ICs.

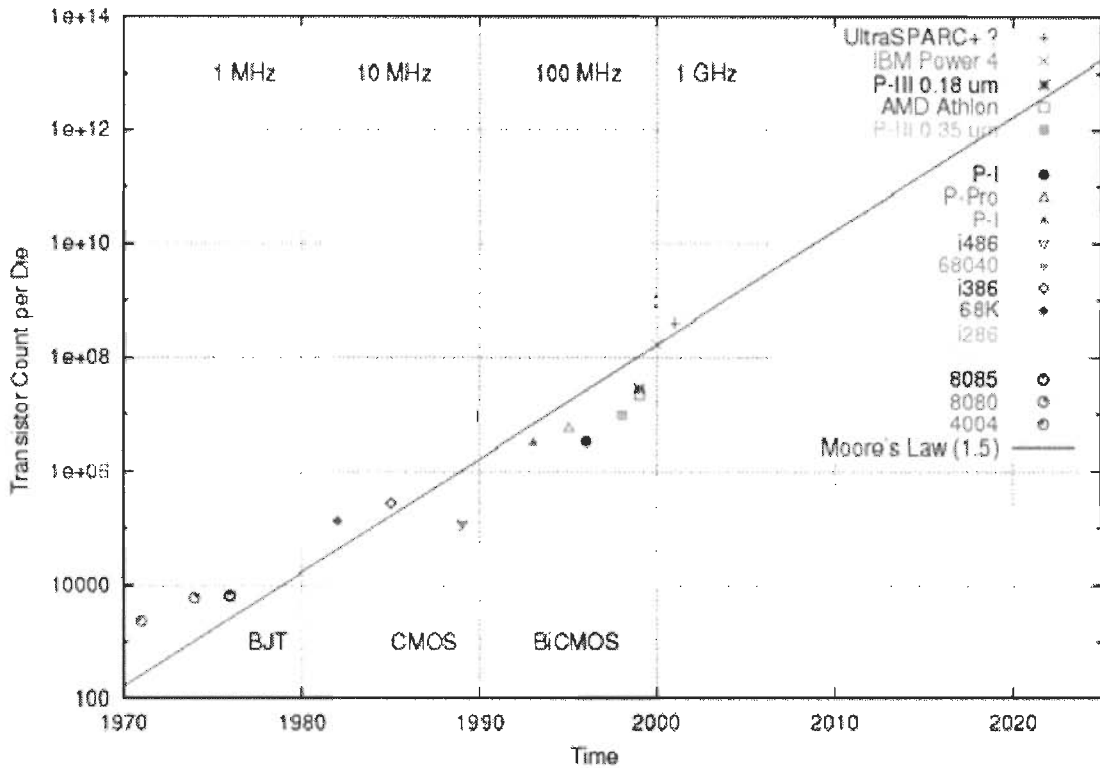


Figure 1.1 Moore's law of scaling [Source: Intel, IBM, TI, Polsson].

Since its conception, there has been an exponential scaling down of transistor dimensions (following the trend predicted by G. E. Moore [46].) targeted towards making the circuits smaller in order to fit more and more functionalities in a given chip area. The modern day circuits have over 100 million transistors per chip and this exponential growth since early 1960s is expected to continue for at least another decade [65]

The main goals behind scaling down transistors in a circuit are to achieve improved performance, more on-chip functionality and reduced cost per functionality.

The transistors in ICs have been traditionally implemented using Bulk Silicon CMOS technology. As the lateral and vertical dimensions of the transistor are scaled down, several effects come into play which make further scaling down of the traditional device architecture increasingly challenging [12]. As the gate length (L_g) of a transistor is decreased (lateral scaling), the source and drain regions come closer and the drain electric field starts reducing the source-channel potential barrier. The capacitively coupled gate tends to lose control on the channel, especially in the sub-surface region. This capacitive coupling can be improved by decreasing the gate dielectric thickness (vertical scaling). The chief outcome of this is an increase in the off-state leakage current (I_{OFF}) of the transistors which contributes to the total stand-by power in a circuit [13, 23].

1.3 Motivation of Work

Microelectronic devices have evolved rapidly in terms of size, cost and performance. Scaling of device dimensions has been the engine of the semiconductor industry [123] allowing manufacturers to produce consecutive generations of integrated circuits of ever decreasing dimensions and increasing transistor densities. This trend has resulted in feature sizes with nanometer dimensions. Current physical gate lengths of transistors used in high performance integrated circuits are around 50 nm and will go down to 32 nm and 18 nm by 2010 and 2016 respectively, according to projections made in the 2007 International Technology Roadmap of Semiconductors (ITRS) [65]. Prototype transistors with gate lengths as small as 22 nm have already been fabricated in research labs around the world [18, 43].

Clearly the microelectronic industry has entered the nanotechnology era and is manufacturing millions of nanoscale transistors on a phenomenal scale.

Consequently, scaling of FinFET device dimensions is important in order to improve the drivability and to achieve higher-performance and functional VLSI's. Hence, an accurate assessment of device characteristics and performance in nanoscale range is of fundamental importance to understand the ultimate limits of FinFET device as well as to develop innovative device concepts. Nanometer scale dimensions (1-100 nm) are comparable to (if not smaller than) the mean free path (~100 nm) as well as the de-Broglie wavelength (~ 10 nm) of electrons in typical semiconductors and metals. Hence, standard macroscopic models (for example, the drift diffusion model of current flow) which include scattering effects using lumped parameters (like mobility) and neglecting quantum effects (like the wave nature of electrons) are not applicable to nanostructures and new models and methods need to be developed.

It is well known fact that as the channel length reduces, more Short Channel Effects (SCEs) are prevalent in the device which tend to degrade the performance and hence the functionality of the chip. The control of SCEs is more challenging in progressive scaling of MOSFETs. The double gate MOSFET and FinFET structures have emerged as the main candidates to provide the electrostatic integrity needed to scale down FinFETs to minimal channel lengths. In addition to better electrostatics than the single gate MOSFETs, the use of these devices have the advantages relative to the carrier transport mainly due to 1) reduced surface roughness scattering and 2) reduction of the coulomb scattering because the channel is made up of undoped/ low doped Silicon. Compact analytical and semi-empirical models of these device structures remain an issue and have been looked into in this thesis.

Technology trends have resulted in static power dissipation (leakage) emerging as a first design consideration in high-performance processor design. Historically, architectural innovations for improving performance relied on exploiting ever larger number of transistors operating at higher frequencies. To keep the resulting switching power dissipation at bay, successive technology generations have relied on reducing the supply voltage. In order to maintain performance, however, a corresponding reduction in the transistor threshold voltage (V_{th}) is required. Since the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) sub-threshold leakage current increases exponentially with reduced V_{th}, static power dissipation has grown to be a significant fraction of overall chip power dissipation in modern deep-sub-micron processes. Analysis of nanoscale device such as FinFET provides high performance and reduced leakage currents with reduced sensitivity to process parameter variations.

Since leakage power is proportional to the number of FinFETs, much of the recent work in reducing static power has focused on Static Random Access Memory (SRAM)-based structures, such as the caches that comprise the vast majority of on-chip transistors. Existing circuit-level leakage reduction techniques are oblivious to program behavior and trade off performance for reduced leakage where ever possible.

1.4 Problems Description

The proposed work during the period of research is expected to yield an optimized design for a conventional 6T based FinFET SRAM for its operation in low power domain showing less SCEs, ultra small access time and high stability. It is felt that in order to properly understand the FinFET based SRAM design, one has to undertake a study to evaluate the full output characteristics of FinFET so that we are

able to appreciate the variation of output characteristics with process parameter variations which are quite substantial at such low dimensions.

In view of the above observations, the whole work during the period of research has been divided into two primary phases. Initially, during the starting phase, the study of FinFET as a device has been carried out. The device dimensions taken during the study is primarily dictated by the technology node as predicted by ITRS report. Subsequently, the results obtained in the first phase have been utilized for FinFET based SRAM design in the second phase of the research work. The requisite design parameters have been obtained through reported literature or nodes predicted by ITRS. Since the work carried out is purely theoretical in nature, verification and validation of the results obtained becomes an issue of prime importance in order to substantiate our work. In order to do so, comparison of our results with those obtained through reported experimental/simulated results have been undertaken during each stage of the work.

After extensive literature survey, various technical gaps came to light for the current research work in this area. These are stated as under:

(i) For the prediction of device performance of FinFET structure, 2D/3D device simulation is inevitable. There are research papers where FinFET 2D/3D model have been proposed but detailed study of variation in the output characteristics with process parameters variation, device structure etc have not been carried out.

(ii) It is felt that a full Quantum Mechanical (QM) analytical modeling needed to be carried out in order to appreciate qualitatively the behavior of FinFET under various bias/process conditions.

(iii) No universal mobility model has been proposed for charge carriers in FinFET structure. The evaluation of effective mobility under all conditions of process parameters variation would be required for determining the driving capability of FinFET structure.

(iv) Extensive QM corrections are required for predicting accurate picture of device. Density of State (DOS) based correction model is not well reported in literature. Moreover outputs from TCAD simulator have not been reported in literature.

(v) To the best of our knowledge, very few research papers have actually dealt with the leakage aspect of FinFET. The study is critical in order to estimate analytically or otherwise the power dissipation of FinFET device under bias. Evaluation of subthreshold and gate leakage current of FinFET have not been reported extensively.

(vi) At subsystem level, very few papers have been reported on FinFET based SRAM design. Most of the papers in this area are based on fabrication/process technology for generation of SRAM cell by DG MOSFET.

In view of above research gaps, the detailed research problems have been presented as:

1.4.1 QM Analytical Modeling of Nanoscale DG FinFET: Evaluation of Potential, Threshold Voltage and Source/Drain Resistance

In order to evaluate the output current, it is essential to find out the potential variation within the active area of the device. In order to approach such a problem, analytical modeling scheme for FinFET has been carried out with device parameters. Key issues including FinFET device structure, design parameters, potential modeling,

process parameter variation effects and device scaling limit have been undertaken quantitatively as well as qualitatively. Variation of potential along source-to-drain region as well as from gate to gate has been presented. The threshold voltage evaluation becomes an important issue in order to undertake power dissipation characteristics. Hence extraction of threshold voltage is also carried out in order to understand the switching behaviour of the device. The analytical modeling for threshold voltage and parasitic source/drain resistance has been carried out for the FinFET device structure under study. The results obtained on the basis of our proposed analytical model have been compared and contrasted with the reported experimental results.

1.4.2 Analytical Modeling of Nanoscale Double Gate FinFET: Evaluation of Inversion Charge, Mobility and Drain Current

As the device dimensions are excessively reduced and the channel length of the device becomes of the order of the de-broglie wavelength of electron, it becomes imperative to undertake an extensive Quantum Mechanical (QM) modeling for the device under study. The QM inversion charge analytical modeling of FinFET device has been carried out. Further, evaluation of quantum inversion charge is to be taken up in order to appreciate the amount of charge storage under various external bias conditions. This has been essential to understand SRAM behaviour. In order to evaluate the output drain current, a comprehensive mobility model for the charge carriers has been carried out. Various mobility models are studied and implemented during the course of study and appropriate model is taken up in order to evaluate the drain current. The results obtained on the basis of our model are compared with our TCAD Sentaurus simulation result as well as reported experimental results. The aim

of the work carried out is to explore FinFET with ultra thin body. They are chosen because of their high scalability. The problem stated above has been overcome by doing a full quantum mechanical treatment of the FinFET device.

1.4.3 Modeling of Subthreshold Leakage Current, Subthreshold Swing factor and Gate Leakage Currents for DG FinFET Device

As the device dimensions are reduced, the off state leakage current substantially increases because of many Quantum Mechanical (QM) effects. This results in a larger power dissipation of the device and the matter assumes critical importance in SRAM as FinFET SRAM designs are prone to larger power dissipations. Reported results have shown that at the same technology node, the leakage in FinFET is lower as compared to bulk MOSFET. The various leakage current components in FinFET device have been evaluated such as subthreshold, gate tunneling leakage current and its dependence on various device/process parameters. This information would be critical in arriving at those device/process dimensions which would result in minimizing the power dissipation.

1.4.4 FinFET Based Nanoscale Static Random Access Memory (SRAM) Cell Design: Analysis of Performance metric, Process variation, Underlapped FinFET and Temperature effect

Embedded SRAM arrays are expected to contribute the largest fraction of chip area and device count in future ICs. These arrays are likely to be the primary source of chip leakage. Further, FinFET based SRAM cell usually uses the smallest device on chip packed very closely together to achieve high density. Thus they are more sensitive to process variations. The FinFET based 6T SRAM cell uses cross coupled

inverter structure to store bit. The mismatch between cell devices can cause data flipping during read operation. Thus the primary goal of the proposed design includes maximizing stability and minimizing leakage in SRAM, besides achieving maximum density. To the best of our knowledge, very few research papers are available that explore FinFET structure/technology from an SRAM circuit standpoint. The existing literature assumes promise for scaling CMOS into the sub-45nm regime, particularly for low-power applications such as memory [115, 170].

Design considerations for maximizing performance and yield of FinFET-based 6-T SRAM at the 32 nm have been examined. It is known that SCEs are effectively suppressed by a narrow silicon fin which allows for gate-length scaling down to the 32 nm regime without the use of heavy channel/body doping. But at such low dimensions of FinFET, there might be issues related to reliable fabrication. There might be a large increase in the parasitic, which would result in hindrance for high speed applications. It also allows FinFET devices to have negligible depletion charge and capacitance, which yield a steep sub-threshold slope. In addition, FinFETs have lower parasitic device capacitance because both depletion and junction capacitances are effectively eliminated, which reduces the bitline capacitive load. Finally, the elimination of heavy doping in the channel minimizes V_{th} variations due to statistical dopant fluctuation effects. Therefore, FinFET based SRAM cells have enhanced performance over planar bulk-Si MOSFET SRAM cells. FinFET based SRAM cell have improved 'read' and 'write' margin of the SRAM cell without compromising on the area requirement. The simulations have been carried out in HSPICE with appropriate structuring of model file containing various device parameters both independent and extracted.

1.4.5 Performance Evaluation of FinFET based SRAM

1.4.5.1 Static and Dynamic Noise Margin

The Static Noise Margin (SNM) is the maximum amount of noise voltage that can be introduced at the outputs of the two inverters such that the cell retains its data. SNM quantifies the amount of noise voltage required at the internal nodes of a bit cell to flip the FinFET based SRAM cell's contents. When the bit cell is holding data, its wordline is 'LOW' so the nFinFET access transistors are 'OFF'. In order to hold its data properly, the back-to-back inverters must maintain bi-stable operating points. The best measure of the ability of these inverters to maintain their state is the bitcell's Static Noise Margin (SNM). For the 32 nm node FinFET, we have evaluated the SNMs under various bias conditions and process conditions. This would be useful for fabrication engineers to design benchmarks for future nanoscale FinFET based SRAM with respect to process tolerances.

1.4.5.2 Read/Write Noise Margin

Utilizing higher FinFET threshold voltages also negatively impact the access time due to the lower read current. However, it improves the 'read' and 'write' margins. While high threshold voltage pFinFET loads decreases the inverter trip point, high threshold nFinFET Pull-Down Device (NPD) tends to increase it. Since the current driving ability of the NPD is larger than that of the pFinFET load, increasing the threshold voltage of the nFinFET transistors tends to have a stronger impact on the trip voltage, thus resulting in larger read and write margins.

1.4.5.3 Power Evaluation

Large FinFET based SRAM consumes a significant portion of the overall power of an application processor. Power consumption in an SRAM consists of short active periods and very long idle periods. For SRAM, standby power consumption is a major issue. Therefore, leakage reduction in large memory arrays has become essential for low-power VLSI applications. FinFET based SRAM cell leakage is commonly suppressed by either using longer channel lengths or higher transistor threshold voltages. Another method is to use multiple threshold voltage devices. Using longer channel lengths increases the cell area and in addition, also increases word line and bit line capacitances, thus increasing access time and active power. Therefore, longer channel lengths are used sparingly.

1.5 Thesis Organization

This thesis is organized into seven chapters as follows:

Chapter 1 Deals with introduction portion.

Chapter 2 The review of existing literature for modeling of proposed device is presented in chapter 2. This chapter contains the literature review on bulk MOSFET, advanced MOSFET structures such as UTB, DG and FinFET, various leakage currents associated with the MOSFET and FinFET devices and circuit aspect of FinFET based nanoscale SRAM design.

Chapter 3 Deals with the full quantum mechanical analytical modeling of two dimensional potential with surface potential approach for the work function engineered Double Gate FinFET device. This chapter also evaluates the threshold voltage and parasitic source/drain resistance analytical modeling of FinFET device.

Chapter 4 Describes the analytical modeling of the quantum inversion charge, field dependent mobility and drain current for FinFET device.

Chapter 5 Describes the analytical modeling and estimation of various types of leakage currents associated with the FinFET device.

Chapter 6 Deals with the FinFET based nanoscale SRAM cell design with device/circuit co-design approach.

Chapter 7 Summarizes all key findings and discussion on them to reach targeted conclusion and finally we will list out the potential directions for future work.

1.6 Conclusion

In this chapter, the reader is introduced with various concepts of FinFET device and nanoscale SRAM design. A brief idea about the international technology roadmap of semiconductor and its applications with reference to ITRS-2007 is also given in this chapter. It concludes by giving a brief organization of the thesis. The outcome of the present work is expected to help future VLSI/ULSI designer and device modeling community to develop such integration schemes that will not only enhance the performance criterion in terms of speed but also a reduction in the overall power dissipation.

Chapter 2

Literature Review

2.1 Introduction

Transistor dimensions have been scaled down to nanoscale dimensions with passing years. Down scaling has the advantage in term of low power consumption, high speed and high packaging density. Microelectronic devices will play a key role in the future of nanoelectronics. Traditional microelectronic devices such as CMOS (Complementary Metal Oxide Semiconductor) transistors are entering the nanoscale regime and are giving rise to extremely inexpensive but extraordinary powerful circuits and systems. Also current CMOS circuits and process technology will be used as a foundation on which to build future nanoelectronic structures. It is not unthinkable that a hybrid between microelectronic and nanoelectronic technology will give rise to powerful structures and systems. Certain novel nano devices with some modifications in traditional CMOS transistors such as Double Gate (DG) MOSFET, Silicon on Insulator (SOI), Metal Gate (MG) MOSFET and FinFET device are also becoming popular. Understanding the operation and the limitations of CMOS transistors is important to understand these new device structures.

Scaling of CMOS into nanometer regime requires new device architectures. Suitable candidates are SOI devices with multiple gates such as double-gate FinFET structures, which can be scaled more aggressively than conventional bulk-Si devices [30, 68, [illegible] 73]. The key feature of multi-gate SOI MOSFETs is strong gate control of the channel region suppressing effectively the short-channel effects. Moreover the

role of Quantum Mechanical (QM) effects becomes more important in these devices with an ultra-thin gate dielectric and Si body. Scaling conventional CMOS transistors much below 50 nm is difficult due to high Short Channel Effects (SCE's) and leakage currents [141, 164]. Control of leakage currents require gate dielectrics so thin and bodies doped so heavily that a process window sufficiently large for manufacturing might not be found. Double-Gate FinFET structures can overcome these and other limitations to transistor scaling [110, 153, 162]. By placing a second gate on the opposite side of the device, the channel to gate capacitance is doubled and the channel potential is better controlled by the gate electrode, thus limiting the leakage current [52]. With this perspective in mind, fully-depleted devices such as FinFETs are very promising candidates due to their immunity against short-channel effects [19, 50]. FinFET devices with a gate width of only 10 nm have already been reported [17].

In contrast to bulk MOSFETs, these devices inherently require two-dimensional investigations [70, 103, 117]. Unfortunately with shrinking device dimensions, classical device simulation becomes more inaccurate. A rigorous Schrödinger-Poisson solver would be necessary to accurately describe the device behavior. As such, simulations are computationally extremely demanding due to the large number of grid points in two-dimensional problems. They are normally not appropriate. Instead, classical device simulations with additional quantum correction models can be used. However, the validity of these models for ultra thin silicon layers is currently under discussion.

FinFETs were developed due to their process simplicity and compatibility with current process flow for bulk planar MOSFETs. The self alignment for the FinFET structure makes it inherentaly advantageous as compared to bulk CMOS technology or standard double gate MOSFET because of lower values of intrinsic gate

to source and gate to drain capacitances, which in turn result in high speed of operation. Further, by vary nature of structure of the FinFET, there is a reduction in the leakage current and hence an increase in I_{on}/I_{off}. MOSFET device size has been scaled quite aggressively due to the fast progress of process techniques. As MOSFET device is scaled down, short channel effects increase and leakage currents are enhanced. Double Gate FinFET was proposed to suppress the short channel effects in future nanoscale device [93, 125]. For extremely scaled devices within the tiny volume of the Si channel, even a small variation in the number of impurity atoms will have a very significant impact on the effective doping density. Hence, according to the classical relationship between the threshold voltage and doping density, controlling V_{th} very precisely will remain a challenging task and is likely to become a critical issue due to doping density fluctuation. Although some early papers [3, 67, 71, 79] have addressed this issue, this mainly focused on the conventional high doping strategy for controlling V_{th}.

To extend the scaling limits for nanoscale technologies, advanced Fully Depleted (FD) SOI and double-gate (DG) FinFET [20, 40] with undoped or low-doped ultra-thin body are emerging [33]. The increase in threshold voltage has been observed in thin-body structure device. Previous works calculated the threshold voltage shift numerically [51, 105, 106] and treated the quantum effect with the effect of a high doping concentration. A simple analytical model is desirable for understanding the experimental data and providing quick guide to the threshold voltage adjustment for Ultra Thin Body Field Effect Transistor (UTBFET).

Given such a promising importance, device modeling of FinFET has become a necessity for possible future applications. The leakage currents associated with bulk MOSFET and Double Gate FinFET have been described in detail [52, 82] while the

circuit aspects of FinFET based SRAM have been studied by Nowak et, al., [39]. Qin et. al., [56] and Sriram et, al., [80] showed that because of excellent control of short channel effect in FinFET, there is a lower subthreshold leakage current and therefore, FinFET emerged as one of the most promising device for circuit design in nanoscale regime.

In this chapter, the review of existing literature is presented. Various research papers, books and monographs are referred which take care of various aspects such as: classical and QM modeling of FinFET device in order to understand the timeliness of the work being carried out as well as to understand the various technical gaps in the area of FinFET modeling and its application to FinFET based nanoscale memory design. Section 2.2; covers the literature on scaling of bulk MOSFET device and section 2.3; deals with a survey of various advanced MOSFET structures, inversion charge density and drain current. Further, in this chapter, section 2.4; describes the review of FinFET device, section 2.5; enumerates the research done on leakage currents associated with the FinFET device. The circuit aspect of FinFET device has been presented for design of FinFET based SRAM through various research papers in section 2.6 and this chapter concludes with section 2.7.

2.2 Scaling of Bulk MOSFET

The planar bulk-silicon MOSFET shown in Figure 2.1 has been the workhorse of the semiconductor industry over the last 4 decades. In 1980's, many alternative models to bulk silicon MOSFET's have been proposed. However, the scaling down of bulk MOSFET becomes increasingly difficult for gate lengths below ~20 nm expected by the year 2010. As the gate length is reduced, the capacitive coupling of the channel

potential to the source and drain increases relative to the gate, leading to significantly degraded Short-Channel Effects (SCE). The main driving forces for reducing the dimensions have increased circuit density per unit chip area, increased speed of operation and lower cost per function. Device scaling requires a balance between device functionality and device reliability. Both of these have to be maintained as one scales channel length to smaller sizes. As critical transistor dimensions are scaled, reliability concerns become more pronounced. This manifests itself as [31, 57, 58, 59, 133, 134]: a) Increased OFF-state leakage, b) Threshold voltage (V_{th}) roll-off, c) reduction of V_{th} with increasing drain bias due to a modulation of the source-channel potential barrier by the drain voltage, also called Drain-Induced Barrier Lowering (DIBL).

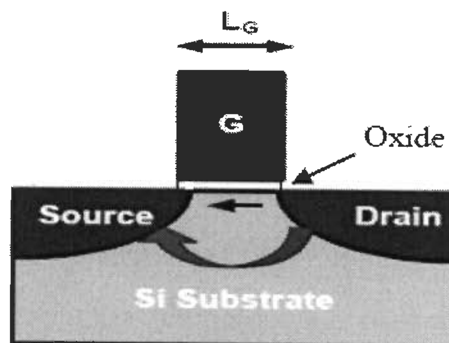


Figure 2.1 Bulk MOSFET.

In order to maintain the relatively strong gate control of the channel potential in bulk devices, various technological improvements such as ultra-thin gate dielectrics [97], ultra-shallow source/drain junctions [167], halo implants [27, 28] and advance channel dopant profile engineering techniques such as super-steep retrograde wells [86] have been necessary. Each of these technologies is now approaching fundamental physical limitations which may, in turn, limit further scaling of device dimensions [66, 97].

In MOS devices, the gate dielectric thickness is the single most important device dimension to enable device scaling and has also been the most aggressively scaled one. A thin gate dielectric increases capacitive coupling from gate to channel, thereby reducing the source/drain influence on the channel. A larger gate capacitance also leads to a larger inversion charge density or increased ON-state drive current. However, gate dielectrics are already so thin that quantum mechanical direct tunneling through them results in significant gate leakage currents below ~20Å. The use of alternative high-k gate dielectric materials can provide a small effective oxide thickness to maintain adequate gate control needed for L_g scaling while providing a large physical barrier to gate-oxide tunneling, thereby reducing gate leakage [58, 89]. In order to scale bulk-Si transistors, heavy body doping is also necessary to eliminate leakage paths far from the gate dielectric interface and to increase back-gate (substrate) control of the body. For sub-100nm gate length devices, a strong halo implant is generally used to suppress sub-surface leakage, but this tends to increase the average channel doping in small L_g devices. High channel doping concentration, however, reduces carrier mobility due to impurity scattering and increased transverse electric field increases subthreshold slope, enhances band-to-band tunneling leakage and increases depletion and junction capacitances. These factors may combine to significantly degrade device performance [1, 11, 15, 17, 22].

In summary, from a device design point of view, in order to achieve good electrostatic integrity or good control of Short Channel Effects (SCE), the gate dielectric thickness, T_{OX}, the source/drain junction depth (X_J), and the channel depletion depth X_{DEP}, need to be scaled down. The scale length for a bulk device, l_{BULK}, is an indication of how short L_G can be made before the SCE are excessive. For a bulk MOSFET, gate leakage limits T_{OX} scaling, X_{DEP} scaling is limited to about

10 nm due to substrate-to-drain and band-to-band tunneling current limitations on body doping. X_J is limited by process limits for forming ultra shallow junctions with abrupt doping profiles [60, 181, 182, 183].

2.2.1 Bulk CMOS Challenges

Bulk CMOS technology faces other challenges as well. In order to keep short channel effects under control, ultra shallow junctions with very high doping abruptness and yet high degree of dopant activation are required. Although methods such as laser annealing and flash lamp annealing are currently being investigated, these may not work for future technology nodes [171, 172]. In addition, the poly-Si gate depletion effect contributes significantly towards the effective oxide thickness and hence the threshold voltage and performance. This effect can be completely eliminated by moving back to metal gate technology. NMOS and PMOS devices, however, need separate gate materials to achieve the required work functions, leading to process integration challenges. Even though bulk CMOS technology with SiO_2 gate dielectric and poly-Si gates has been the most suitable and well-understood technology, the above mentioned challenges strongly push the need for alternate device structures and processing techniques [150, 151, 181, 165, 166].

The main challenges posed by the limits of downscaling are the static power consumption due to short channel effects (SCEs), [13, 57, 64] and the leakage currents [118, 122, 160]. The leakage currents are due to quantum-mechanical tunneling, the subthreshold leakage, junction leakage, direct tunneling between source and drain through the channel potential barrier. Replacing the traditional SiO_2 insulator by alternative materials with high-k dielectrics will be required to reduce

some of leakage problems. Since subthreshold leakage current is not suppressed by introducing new materials, it is going to be one of the ultimate limitations to scaling. In addition, the polysilicon gate electrode has the limitation associated with the depletion region and boron out-diffusion, reducing beneficial effects of device scaling. As a result, new metal gate materials will be needed in conjunction with high-k dielectrics. Innovations in the both the device structures and the materials will ensure high-performance operation of nanoscale electronic devices. Some of the more promising approaches are silicon on insulator (SOI), strained silicon-germanium, high-k electrode, metal gate electrode, double gate MOSFETs etc.

2.2.2 Disadvantages of Bulk MOSFET

From a purely theoretical standpoint, a CMOS device created on SOI offers many advantages over those made on bulk Si [29, 120] For example, devices made in bulk silicon have to contend with: i) Several sources of parasitic capacitance: source/drain to body or source/drain to isolation oxide. (ii) The continued scaling of devices implying higher substrate doping concentrations, in turn increasing the parasitic capacitances. (iii) Degrading transistor performance.

2.2.3 Nanoscale CMOS Design Problems

1. CMOS Latch up,
2. Hot Carrier Gate Dielectric Degradation,
3. Punch Through
4. Degradation in Carrier Mobility,
5. Source /Drain Series Resistance
6. Discrete Doping Effect.

CMOS Latch up: A byproduct of the bulk CMOS structure is a pair of parasitic bipolar transistors. The collector of each BJT is connected to the base of the other transistor in a positive feedback structure. A phenomenon called latchup can occur when both BJT's conduct, creating low resistance path between power supply and ground. The latchup phenomenon also occurs when the product of the gains of the two transistors in the feedback loop is greater than one. The result of the latchup is at the minimum when a circuit malfunctions and in the worst case, the destruction of the device.

Hot Carrier Gate Dielectric Degradation: If a region of high electric field is located near the Si-SiO_2 interface and if the electric field is high enough, some of the electrons or holes can gain sufficient energy from the electric field to surmount the interface barrier and enter the SiO_2 layer. In general, the injection from Si into SiO_2 is much more likely for hot electrons than holes because of two main reasons: (a) Electrons can gain energy from the electric fields much more readily than holes due to their smaller effective mass. (b) The Si-SiO_2 interface energy barrier is larger for holes (4.5eV) than for electrons (3.1eV). This effect is called hot carrier injection. The hot carrier effect is also a major source of power dissipation in nanoscale CMOS.

Punch Through: In short channel devices, due to the proximity of drain and source, the depletion regions at the drain-substrate and substrate-source junction extend into the channel. As the channel length is reduced, with constant doping, the separation between the depletion region boundaries decreases. Increase in the reverse bias across the junctions (with increase in V_{ds}) also leads to the boundaries pushed further away from the junction and nearer to each other. When the combination of channel length and reverse bias causes the depletion regions to merge, then punch-through is said to have occurred [57]. In sub-micron MOSFETs, a V_{th}-adjust implant

is used to have a higher doping at the surface than in the bulk. This causes greater expansion of the depletion region below the surface thus giving rise to punch through.

Degradation in Carrier Mobility: As channel lengths shrink below 100nm, MOS processes require gate oxides less than 1.5nm. Due to this feature, the transverse electric field reaches much higher than 10^5 V/cm even when the device is biased at threshold. This much high electric field always leads to mobility degradation as scattering near the Si/SiO_2 increases. In addition, the high channel doping used to lower SCE (short channel effects) and to adjust V_{th} results in mobility degradation due to coulomb scattering with ionized dopants [26]. Although due to quantum effects, the inversion charge has a peak below the surface leading to increase of oxide thickness of around 10Å leading to decrease in effective electric field, but then also the degradation is large enough to decrease the drive current.

Source/Drain Series Resistance: Another limiting factor on CMOS scaling is the effect of external source and drain resistance in shallow junction devices. One of the fundamental challenges in modern device performance is the trade-off between short-channel effects and the impact of source-drain series resistance [6]. For a MOSFET to operate as a VLSI component, the capability of switching off this current path and suppressing short-channel effects is a major priority in MOSFET design. In the ON-state, reduction of gate length is desirable to minimize the channel resistance. However, when the channel resistance becomes as small as the source and drain resistance, further improvements in drain current cannot be expected because increase in these resistances tend to suppress the short-channel effects. Even though the ITRS roadmap predicts Source and Drain Extension (SDE) depths as shallow as 10 nm to achieve a 50 nm transistor, too shallow a junction leads to high external resistance, which in turn results in degradation of driving current.

Discrete Doping Effect: As the feature size of MOSFET is being scaled down to sub 50nm, the total number of dopants implanted inside the channel becomes very less. The effect is that even a small fluctuation can give rise to significant variations in threshold voltage [51]. The name discrete dopants comes from the fact that total count of dopants comes only to few hundreds, and thus even a small number change appears to be significant resulting in variation of V_{th}. In fact, that is only a short list of problems that have a varying degree of impact on device performance and reliability. While indigenous approaches to scaling have alleviated some of these problems, it became clear that a technological breakthrough may be needed to push conventional CMOS further into the submicron regime. In the late 1980's, a different approach to Si substrates gained momentum and drew the attention of industry – Silicon-on-Insulator, also known as SOI [74, 75].

2.3 Advanced MOSFET Structures

In order to mitigate some of the issues of the bulk MOSFET, following advanced transistor structures have been proposed:

1. Ultra-Thin Body FET (UTB FET),
2. Double-Gate FET (DG-FET),
3. SOI MOSFET.
4. Multiple-Gate MOSFET (MG MOSFET).

2.3.1 Ultra-Thin Body (UTB) MOSFET: UTB MOSFET has been shown in Figure 2.2. The basic concept of the UTB MOSFET is to use an extremely thin (< 20 nm) Silicon on Insulator (SOI) film to eliminate subsurface leakage current. The

self-aligned source and drain (S/D) are required to minimize parasitic series resistance and achieve high drive current. The key benefit of these structures is that the conduction is confined to a thin silicon film, thereby [33, 98, 169, 170]:

1. Physically eliminating the sub-surface leakage component.
2. The layouts and process steps are very close to the conventional bulk CMOS flow.
3. An undoped channel is used to reduce the effect of statistical dopant fluctuations.

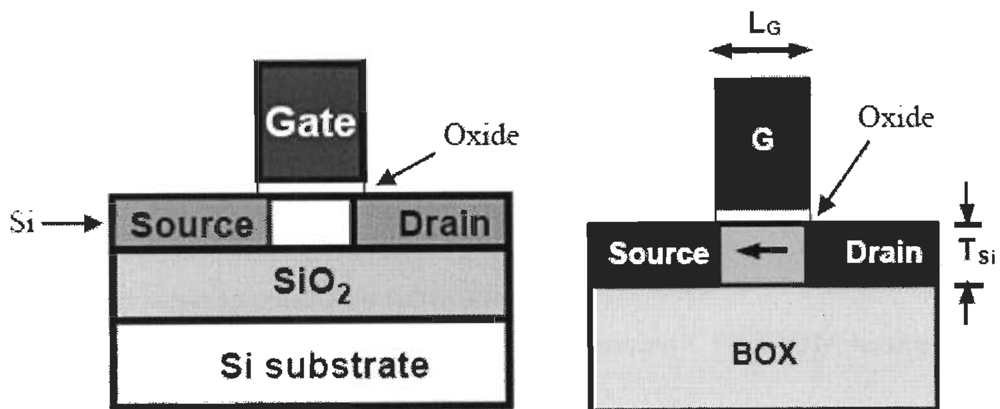


Figure 2.2 Ultra Thin Body MOSFET.

4. They also have additional benefits of better short channel control.
5. Reduced parasitic capacitance (no source or drain-bulk capacitances exist).
6. Overall, these devices show superior performance (I_{ON}/I_{OFF} as well as intrinsic delay) compared to their bulk counterpart [96, 97, 98].

2.3.2 DG MOSET

The thin body requirement can be relaxed by adopting the double-gate (DG) MOSFET structure shown in Figure 2.3, in which two gates control the channel

potential. The DG-FET achieves better gate control and thereby has improved SCE for a given body thickness [61, 62, 174, 177]. The body thickness can be twice that of a single-gated UTB device in order to achieve the same degree of SCE. The DG MOSFET does not suffer from electric field penetration from the source/drain to the channel through the buried oxide and is, therefore, more scalable. The thin body requirement is highly desirable from a manufacturability point of view since the formation of a uniform ultra-thin film can pose major technological challenges. Simulation results show that a DG MOSFET has the best scalability down to sub-30 nm L_G devices [96, 97]. The improved scalability of thin-body devices makes them attractive for future generations of CMOS technology and so they have been included in the International Technology Roadmap for Semiconductors [65].

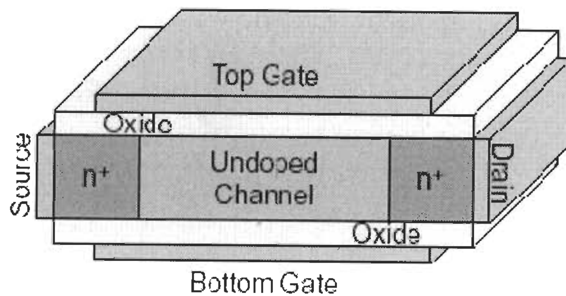


Figure 2.3 Double gate MOSFET.

Double gate MOSFET such as the FinFET is promising structure to be scaled into the sub-25nm regime [31, 62, 171]. DG-MOSFET usually are designed to have a very thin Si channel that is fully-depleted in order to cut-off sub-surface leakage paths, thereby making them more scaleable. The use of lightly doped or undoped channels leads to enhanced immunity to dopant fluctuation effects, smaller drain-to-body capacitance and higher carrier mobility arising from a lower transverse electric

field. With no doping in the channel, metal gates with suitable work function are required to achieve reasonable threshold voltages in fully-depleted devices [16, 33].

One of the challenges introduced by a thin silicon channel is the extremely high parasitic series resistance and contact resistance at the source and drain (S/D) regions. While parasitic resistance is a serious challenge in bulk devices [77], the problem is more severe in thin-body devices and various process technologies have been proposed to reduce it [181, 182]. This chapter discusses device optimization methodology to identify the device design tradeoffs involved in order to find the balance between good-control of short channel effects (SCE) and minimizing external parasitic resistance. The tradeoffs between the various device parameters in determining the short-channel behavior can be studied using the framework of the scale length [89]. This is important from the viewpoint of device scalability.

2.3.3 SOI MOSFET

Silicon on Insulator (SOI) materials are currently under intense investigation for the fabrication of advanced integrated circuits with unique properties: full isolation, reduced parasitic capacitances, vertical junctions, high speed, reduced hot carrier injection and short channel effects, simpler design and excellent tolerance to radiation effects. Many important features of the MOS transistors fabricated on SOI result from the dual-gate control of the electrostatic potential in the Si island [147] SOI MOSFETs are nowadays replacing conventional bulk devices in high speed VLSI and other high frequency CMOS applications [9, 30]. Compared to their planar bulk counterparts, Silicon-On-Insulator (SOI) MOSFETs exhibit, in general, smaller short-channel effects because of their inherent physically thin channel region. In this

respect, these are the ideal candidates to enable further dimensional downscaling of ICs.

From a practical circuit point of view, the advantage of smaller short-channel effects means that SOI CMOS structures have a smaller power-delay product than bulk technology for a given CMOS generation. Moreover, as CMOS generations evolve with time (i.e. the dimensions decrease), the advantage of SOI in power-delay product increases. Some fundamental benefits of the SOI structure over the traditional bulk MOSFETs have motivated research in the field. These are suppression of latch-up, greater immunity to radiation, potential for higher speed and lower circuit power consumption. Some of the recent applications which have evidenced the superiority of SOI with respect to bulk technology are: SOI microprocessors with more than 20% speed improvement, SOI RF power amplifiers with higher power efficiency and low noise amplifiers in the low-GHz range. Due to the ongoing downscaling of the dimensions in bulk transistor technology, the numbers of metal layers have been increasing in order to be able to connect the growing number of transistors. Because of this inescapable trend, interconnect complexity and thus interconnect delay is becoming a progressively more dominant factor in circuit performance. According to researchers' point of view, SOI technology should emerge very soon as the core CMOS technology because it allows 3-D integration and therefore, it reduces interconnect complexity.

All these features point to the SOI MOSFET as the structure capable to extend Moore's Law far below the 0.1μm node to the nanometer scale. The present evolving status of three dimensional multiple-gate SOI MOSFETs clearly indicates that this novel technology is rapidly becoming the mainstream CMOS technology for high speed use, both for microprocessors and related components, as well as for wireless

applications. Because CMOS-based transceivers are quickly taking on the wireless market and at the same time SOI is becoming the mainstream CMOS technology, SOI CMOS is making strong inroads into an ever growing number of RF applications. Of course many crucial issues still remain to be solved, such as the development of appropriate higher dielectric constant materials for the gate dielectric, lower dielectric constant materials for interconnect isolation, metallic materials for the gates, RF passive components, etc. Nevertheless, it is already evident that as of today 3-D SOI structures represent the most promising means to enable MOSFET devices to continue to progress along Moore's Law predictions into the nanometer scale generation.

2.3.4 Multiple-Gate MOSFET

Multiple-gate structures on undoped SOI (Silicon on Insulator) are promising architectures likely to overcome short channel effects (SCE) in nanometer-scaled MOSFET. Contrary to bulk MOSFETs, Double-Gate (DG), Triple-Gate (TG) and Quadruple-Gate (QG) MOS transistors do not need drastic doping channel engineering. Moreover, they allow relaxing the oxide thickness T_{ox} and the body thickness T_{Si} requirements, which are severe in fully depleted Single Gate MOSFETs (SG) on SOI. The benefits of multigate structures are:

- Higher current drive thus better performance
- Prophesized to show higher tolerance to scaling.
- Better integration feasibility, raised source-drain structure, ease in integration.
- Large number of parameters to tailor device performance
- Undoped structures, so no discrete dopant effect

The most promising approach is the structure where multiple number of gates are used to control the channel carriers. This device structure is accordingly called Multiple-gate MOSFETs (MuGFETs). This device structure has the advantage of reducing the short channel effects and improving the subthreshold slope, as well as providing higher packing densities. The importance of subthreshold performance is tied to the decreasing power supplies in low power portable applications. By improving the subthreshold slope, lower threshold voltages can be used to maintain the ON-state current drive without increasing leakage currents. Unfortunately, multiple-gate devices are hampered by process complexity. Still, as of today, MuGFETs are recognized as having the best potential among the advanced device structures to maintain the node to node performance improvement predicted by Moore's law.

The salient features of the MuGFET are [57]:

1) Control of short-channel effects by device geometry, as compared to bulk FET, where the short-channel effects are controlled by doping (channel doping and/or halo doping); 2) A thin silicon channel leading to tight coupling of the gate potential with the channel potential.

These features provide potential advantages that include

1) Reduced 2D short-channel effects leading to a shorter allowable channel length compared to bulk FET; 2) A sharper subthreshold slope (~60 mV/dec compared to ~80 mV/dec for bulk FET) which allows a larger gate overdrive for the same power supply and the same off-current; 3) Better carrier transport as the channel doping is reduced (in principle, the channel can be undoped).

Reduction of channel doping also relieves a key scaling limitation due to the drain-to-body and band-to-band tunneling leakage current. A further potential advantage is more current drive (or gate capacitance) per device area. Carrier transport in the MuGFET with an undoped channel is superior to that in conventional bulk FETs for two reasons: reduced coulomb scattering due to fewer ionized dopants in the undoped/low-doped channel, and reduced surface roughness scattering due to a lower surface electric field. In bulk FETs, channel doping is employed to set the threshold voltage and halo or pocket dopings are employed to control the short-channel effects. These ionized depletion charges contribute appreciably to the surface electric field.

In a MuGFET with an undoped channel, there is no ionized depletion charge, therefore, the surface electric field is contributed entirely by inversion carriers. Even though the carrier mobility follows the "universal mobility" curve, at the same gate overdrive the carrier mobility can be significantly higher compared to a bulk MOSFET, because the effective field is lower at the same gate overdrive. While the bulk MOSFET operates at an effective field above 1 mV/cm, the MuGFET with an undoped channel operates at around 0.5 MV/cm, thereby, improving the mobility by almost two times. This improves transport because in the DG MOSFET capacitance C is doubled, the current I is improved by more than two times because of the better transport. The MuGFET is very promising for miniaturization below 50 nm. The main reasons behind this conclusion are the following-

1) The drain current increases in subthreshold region as $\exp\left[q\left(V_{gs}-V_{th}\right)/\left(K_bT\right)\right]$, with an ideality factor equal to 1, because of the almost ideal subthreshold slope of 60mV/decade. This is extremely important to reduce the leakage current at low

threshold voltages; 2) The shield effect of the extra gates makes the MuGFET more immune to the short-channel effect than any bulk or SOI MOSFET; 3) The shielding effect of the extra gates prevents punch through to occur even at zero doping concentration within the channel, which is important to prevent degradation of the output characteristics and excess leakage currents at zero V_{gs}; 4) The current increase due to velocity overshoot is very substantial at the dimensional limits afforded by the MuGFET. Also, the transit time across the channel can be kept less than 1 ps, which exceeds the performance of a BJT with a corresponding base thickness; 5) For any given device size, the MuGFET transconductance is at least twice as large as that of any standard MOSFET because of the action of at least two gates.

In view of the above considerations, the MuGFET is expected to offer outstanding performance in digital logic provided the source/drain resistance can be kept below the intrinsic device resistance. Because of the thin silicon channel, the series resistance of the MuGFET is of particular concern. Some form of raised source/drain process would be required in order to achieve a source/drain fan-out. Growing selective epitaxial silicon on thin (<15-nm) silicon substrates (or fins) is still difficult because the thin starting silicon tends to break up during or prior to the epitaxial growth. In addition, as the silicon channel thickness is reduced to less than 10 nm, optimization of the series resistance and parasitic capacitance may prove difficult.

2.4 FinFET Device: A Review

FinFET structure (Figure 2.4b) evolved from an earlier device known as a fully DEpleted Lean channel Transistor (DELTA, Figure 2.4a), was originally

introduced in 1989 [27]. The concept of multiple-gate FETs was already familiar [59, 73, 86], but the novelty of the DELTA implementation resulted in development of similar devices.

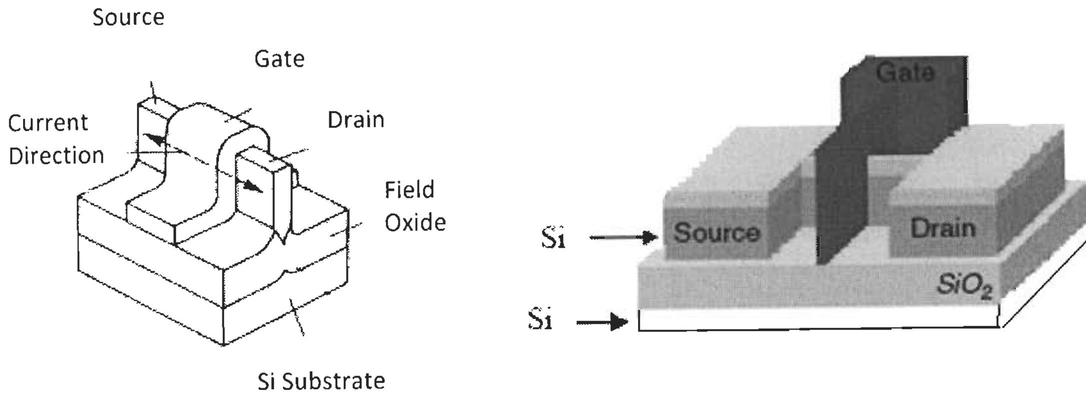


Figure 2.4 (a) DELTA transistor [27], (b) FinFET transistor, adapted from [128].

The DELTA and FinFET transistor both function on same principle. The body of the device (fin) is a relatively thin structure that connects the large source/drain pads. With a gate dielectric formed on the side of the fin, a conformal gate material is deposited to cover both sides of the fin, creating a tied double-gate transistor. The current conduction is thus on the side of the fin that connects source and drain and the device channel width is often approximated as twice the fin height. The device current drive is easily increased by adding more parallel fins to the structure as allowed by the source/drain dimensions. Although familiar for over a decade, these devices have garnered a lot of attention as of late. There have been several groups working on FinFET devices in recent years with most research coming from University of California at Berkeley (UCB), IBM, and Intel.

Due to the unconventional nature of the device (sidewall channel conduction), transistor metrics can be interpreted in several ways. It is important to note that for FinFETs, channel width is often defined by fin height. However, when compared to

classical MOSFETs, the channel width that should be compared is actually twice the fin height. These concepts should be kept in mind when evaluating device performance from literature. The approaches taken in fin creation employ a variety of techniques: from electron-beam lithography [163, 164] to conventional deep ultraviolet photolithography [16] and combinations of ultraviolet photolithography and spacer-based lithography [173]. Research has often focused on the development of ultra-thin body structures to ensure full depletion with some efforts concerned with reduction of etch damage in the channel region.

2.4.1 FinFET Benefits, Drawbacks and Alternatives

The multiple research efforts in the FinFET have already produced impressive results from both academia and industry. However, FinFETs are not the only solution to the problems of continued scaling. The first and most obvious approach is to continue with traditional planar CMOS technologies until a fundamental barrier, such as the size of the silicon atom, is achieved. The cost associated with transition to entirely new types of devices are immensely prohibitive considering the time and investment needed to establish new design and manufacturing processes. Thus, the transition to new and riskier solutions is a tremendous undertaking with the industry focusing on an approach that works now. Still, most major manufacturers and researchers have investigated alternatives to both planar CMOS and FinFETs [20, 129, 138, 139].

The "multi-gate" FET device group, to which FinFETs belong, contains several proposed solutions to scaling problems. For example, researchers have already demonstrated functioning of Double-Gate (DG) planar devices [117] and Gate-All-

Around (GAA) devices [141]. These types of FETs offer benefits similar to those of FinFETs: improved short-channel effects and subthreshold slope with an increased drive current density. However, while the effective transistor width of a FinFET is controlled by the number of fins present, planar DG devices are thought to be limited in width to less than a micron, while GAA devices often present tremendous design and process difficulties in manufacturing [120, 122, 141]. Issues such as top-and-bottom gate size matching and alignment and parasitic capacitance make process integration difficult.

2.4.2 FinFET Device Modeling: Potential, Threshold Voltage, S/D Resistance, Inversion Charge, Mobility and Drain Current Modeling

Accurately predicting the behavior of fabricated devices using device models and simulators saves time and money. As a result, FinFET modeling is an ongoing topic of research for many engineers and device physicists. Simple analytical models of the MOS transistors are needed for computer-aided design of digital and analog integrated circuits containing thousands to millions transistors on a silicon chip. The purpose of modeling is to derive simple, fast and accurate analytical (mathematical equations) representations of the terminal electrical (DC, switching, and also small-signal) characteristics of FinFETs. Compact transistor models are needed to compute analytically the transistor characteristics, rapidly enough, for use in circuit simulators to design and optimize the performance of silicon monolithic integrated circuits (or chips) containing thousands to millions of similar and dissimilar transistors for switching and analog applications. [149, 163, 163, 179]. By the mid 1990s, however interest in low-power, low-voltage circuits led efforts to provide designers with improved transistor models and design methods [28, 49, 66]. The EKV model,

continuous through weak, moderate, and strong inversion, allowed designers to improve the accuracy of their hand calculations and simulations of low-voltage, low-power circuits [30, 49].

Analytical modeling of Double Gate FinFET has been carried out by many workers [111, 112, 113, 166, 173]. The double gate FinFET operation and inversion charge has been evaluated by Munteanu *et. al.,* [35]. Conde *et. al.*, [10] presented a generic implicit surface potential solution for undoped DG FinFET, physically scalable applied gate biases and insulator/channel thickness variations and catering to applied gate biases to both gates using one dimensional Poisson's equation approach based on classical domain. For nanoscale device dimension, we require two dimensional approach for double gate FinFET device which will be valid for classical as well as in quantum domain.

The quantum surface potential can be developed with the consideration of quantum mechanical effects (QMEs) which play a major role within the device for such a nanoscale dimension [35, 47]. Short channel effects (SCEs) in nanoscale DG FinFETs have been examined extensively [29, 32] and show the need for UTB thickness thinner than or comparable to the De Broglie wavelength. Modeling of QMEs in these devices has received less attention. Since, carriers in UTBs are subjected to structural confinement (SC) [156, 179], in addition to the field induced electrical confinement (EC) [149], QM effects on the subthreshold electrostatics must be considered. When channel carriers are spatially confined in one dimension, by either SC or EC, carrier energy quantization for DG FinFETs becomes significant [22, 24, 45, 179].

Threshold voltage is an important device parameter which governs switching of any FET device. Various modeling approaches of threshold voltage have been

discussed [29, 32, 93, 104, 178] for DG FinFET device. Katti *et. al.,* [51] reported the evaluation of threshold voltage based on pure quantum charge. The model developed by Chiang *et. al.,* [104] is a 2D approach of threshold voltage evaluation with the consideration of minimum sheet density of inversion carriers which reaches to a value of threshold charge adequate for identifying the turn on condition and it is a fully classical approach. Sherony *et. al.* approach [105] is based on physics based threshold voltage for SOI MOSFET while Wong *et. al.,* [58] has simulated on FIELDAY simulation for the evaluation of threshold voltage of undoped channel DG FinFET.

Source/Drain (S/D) extension region resistances are an important concern when designing such structures because these resistances can be very high (due to the use of an ultra-thin body), thus limiting device performance. Analysis of the parasitic and total Source/Drain resistance in FinFET device has been presented by Dixit, *et. al.,* [6]. The use of undoped ultra-thin bodies also reduces the possibility of adjusting V_{th} by varying the body doping. Gate stack engineering has to be performed to obtain an appropriate V_{th} either by employing new contact materials with desirable work functions, or maintaining an offset voltage between the different gate electrodes to mimic different work functions [33, 144]. Quantum effects (subband splitting) can become significant as the confinement of carriers becomes stronger within ultra-thin bodies, which in turn translates into an increased sensitivity of V_{th} to the body thickness. This effect poses an additional challenge as fluctuations in T_{fin} have to be strictly controlled.

The inversion charge modeling using one dimensional potential approach has been discussed analytically as well as numerically [50, 109, 134]. Discussion on inversion charge with varying device parameters to achieve the volume inversion in the channel has been presented by Munteanu, *et. el.,* [35]. But very few groups have

estimated analytical inversion charge using two dimensional approaches. The drain current models have been carried out with quantum mechanical approach [8, 10]. In most of drain current models, it has been found that the estimation of drain current has been carried out with the calculation of self consistent potential within the active silicon region. Accurate gate capacitance modeling has been carried out by Lazaro *et. al.,* [8] and electron mobility for DG FinFET by Majkusiak [14].

To be able to better predict the I-V characteristics of FinFET device, accurate mobility model are required to incorporate all of the basic scattering mechanism operating in the inversion layer. Numerous models for carrier mobility for both the inversion layer and bulk silicon have been reported in literature but most of them suffer with some limitation, for example, the validity of the temperature range [82], the difficulty of implementation in simulators of completely generalized (nonplanar) devices [157]. It has already been reported that the electron and hole mobilities in the inversion layer on a (100) surface follow the universal curves at room temperature independent of the substrate impurity concentration or the substrate bias when plotted as a function of effective normal fields [2, 8, 24]. Esseni *et al.* [26] reported that the normal field dependence of the electron mobility is well explained in terms of electron quantization.

2.5 Leakage Currents in Bulk MOSFET and FinFET Device

Reducing the thickness of the gate oxide at each technology node can help to improve the on-state current of a MOSFET. Larger 'on state' current can charge the capacitors of the MOSFET more easily reducing the device delays. As the gate oxide thickness becomes fantastically thin, the gate oxide will be the constraints of scaling

MOSFETs due to high gate leakage current. First, electrons and holes continuously leak through such thin gate oxide. In other words, the leakage problems become serious and power dissipation will increase a lot [53]. The leakage currents in nanoscale devices have been described by number of authors [83, 131, 153]. Choi *et al.*, [82] described the leakage current in FinFET with scaling theory. One solution for increased leakage current is to replace the traditional SiO_2 dielectric layer with a material with higher dielectric constant layer than that of silicon dioxide and other is alternative advanced MOS structures like FinFET. The major contribution of leakage current in FinFET devices is due to subthreshold leakage current and gate leakage current.

2.5.1 Subthreshold Leakage Currents

The dominant components of static power dissipation in VLSI chips are subthreshold leakage currents and power dissipation. It also creates problem in switching the device off. Due to small current, there will be a small voltage present at the output node of CMOS circuits. The major components of subthreshold currents are DIBL and diffusion of electrons from source to drain below the threshold voltage. Chin, *et al.*, [125] described the subthreshold leakage current in FinFET and its scaling limits. The subthreshold currents are very sensitive to changes in V_{th} and thus with threshold voltage scaling, subthreshold leakage currents will increase exponentially. The effect of DIBL is to reduce the barrier and thus more electrons are able to cross the barrier and run to drain side thus producing a small leakage current even if gate voltage is less than threshold voltage. The other component comes from diffusion of electrons from source to drain as diffusion current is proportional to

$\partial n/\partial y$, where n is electron concentration. With decrease of feature size (i.e. channel length) the gradient of charge increases resulting in increase of leakage current. Figure 2.5 shows the variation of subthreshold current with gate voltage. The subthreshold current has been calculated from the subthreshold slope (mV/decade of current) as shown in figure 2.5.

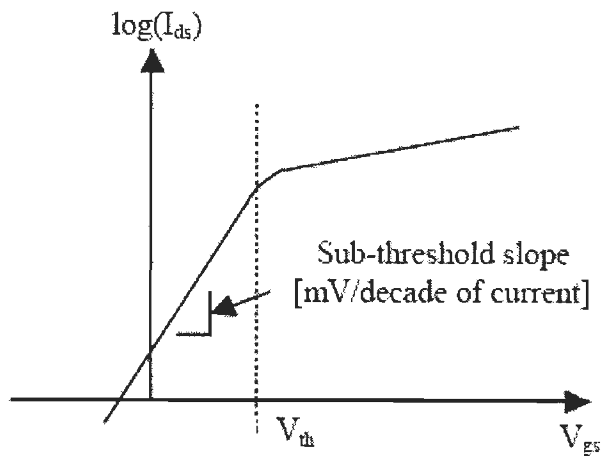


Fig 2.5: Variation of subthreshold current with gate voltage

2.5.2 Gate Leakage Current

The downsizing of MOSFETs has been accomplished in large part by decreasing the oxide thickness to obtain high current drive and good short channel control. It has been predicated by ITRS that gate oxide thicknesses of 1 nm to 1.2 nm will be required for sub-50 nm CMOS [145]. In this thin gate oxide regime, direct tunneling current increases exponentially with decreasing oxide thickness which is of primary concern for CMOS scaling. Gate direct tunneling current is produced by the quantum mechanical wave function of a charged carrier through the gate oxide

potential barrier into the gate, which depends not only on the device structure but also bias conditions.

It is evident that in nanoscaled devices, all of the different leakage components become important and their magnitude depends strongly on the device structure and doping profile [84]. DG FinFET has been promising for extending scaling into the nanometer regime [20]. In DG FinFET device, because of excellent control of the short channel effect, there is a lower subthreshold leakage current [127].

2.6 FinFET Based SRAM Design Issues

Static Random Access Memory (SRAM) is by far the dominant form of embedded memory found in today's Integrated Circuits (ICs) occupying as much as 60-70% of the total chip area and about 75%-85% of the transistor count in some IC products. The most commonly used memory cell design uses Six Transistors (6-T) to store a bit, so all of the issues associated with nano scale MOSFET scaling apply to scaling of SRAM [7, 21, 130, 143]. As memory will continue to consume a large fraction of the area in many future IC chips, scaling of memory density must continue to track the scaling trends of logic [180]. Statistical dopant fluctuations, variations in oxide thickness and line-edge roughness increase the spread in transistor threshold voltage and thus on- and off- currents as the MOSFET is scaled down in the nanoscale regime [3]. Increased transistor leakage and parameter variations present the biggest challenges for the scaling of 6T SRAM memory arrays [55, 108].

To overcome the limitations of CMOS based SRAM cell, new device based SRAM cell design is required with minimum leakage current and low power consumption [142]. FinFET device structure has its unique properties which may be

the right candidate to replace the CMOS based circuit design due to reduced SCE's and leakage current. Unlike planar single and double-gate devices, the FinFET effective channel width is perpendicular to the semiconductor plane [80, 82]. Therefore, it is possible to increase the effective channel width and drive current per unit planar area by increasing the Fin-height. Interconnect dominated circuits such as memory arrays are likely to get benefited from the increased driving current. An estimated 70% of the transistors in a billion-transistor superscalar microprocessor are expected to be used for memory arrays, especially for large SRAM data caches. Therefore, it is essential to develop a low power SRAM design technique for the new device such as FinFET.

To our knowledge, only few published material exists that explores the FinFET technology design from an SRAM circuit standpoint. Joshi et al. [132] have studied the impact of width quantization on FinFET based SRAM cell metrics, but technology design choices have not been investigated. A substantial volume of research on process variations in FinFET exists [57, 58]. None of these, however, consider the implications at the circuit level. Sriram et al. [80] have considered the impact of variations on FinFET based SRAM cell read current and stability, but the analysis was done at a single device design point and the advantage of quasi-planarity for SRAM was not considered.

The functionality and density of a memory array are its most important properties. Functionality is guaranteed for large memory arrays by providing sufficiently large design margins (to be able to be read without changing the state, to hold the state, to be writable and to function within a specified timeframe), which are determined by device sizing (channel widths and lengths), the supply voltage and marginally by the selection of transistor threshold voltages. Increase in process-

induced variations results in a decrease in FinFET based SRAM cell read and write margins which prevent the stable operation of the memory cell and is perceived as the biggest limiter to SRAM scaling [39].

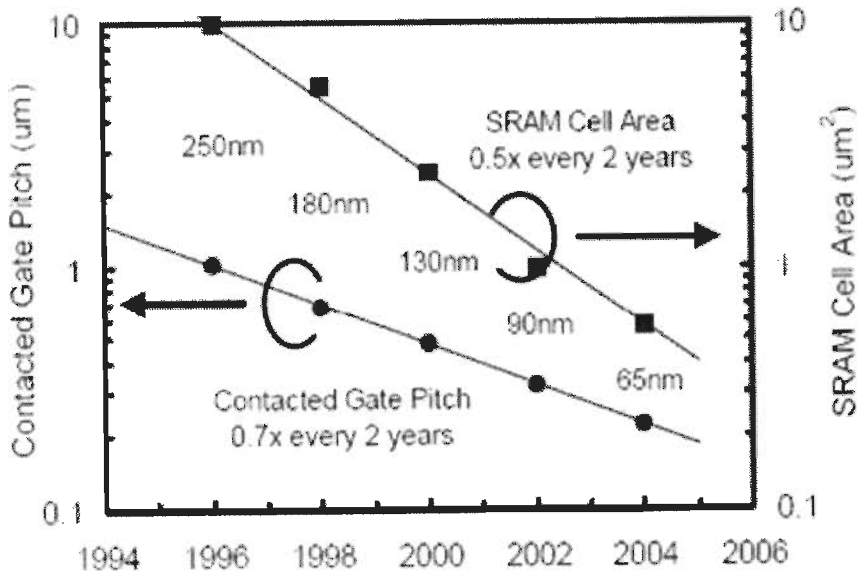


Figure 2.6 SRAM cell size has been scaling at ~0.5 x per generation.

The 6T SRAM cell size, thus far, has been scaled aggressively by ~0.5x every generation (Figure 2.6). However it remains to be seen if this trend will continue with the help of FinFET based SRAM cell design. Since the control of process variables does not track the scaling of minimum features, design margins will need to be increased to achieve large functional memory arrays. Moving to more lithography friendly regular layouts with gate lines running in one direction, has helped in gate line printability [119] and could be the beginning of more layout regularization in the future. Also, it might become necessary to slow down the scaling of FinFET dimensions to increase noise margins and ensure functionality of large arrays, i.e., tradeoff cell area for FinFET based SRAM robustness. [180]. SRAM cells based on advanced transistor structures such as the planar UTB FETs and FinFETs have been

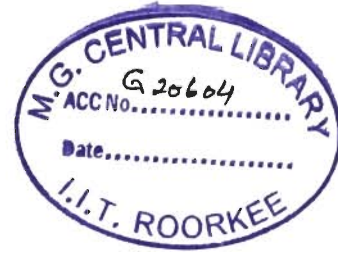
demonstrated [40, 152] to have excellent stability and leakage control. Some techniques to boost the SRAM cell stability, such as feedback [119] are best implemented using FinFET technology because there is no associated layout area or leakage penalty. FinFET-based SRAM are attractive for low-power, low voltage applications [95, 108].

2.7 Conclusion

In this chapter, we have presented an existing literature review of FinFET device and various modeling techniques. This literature survey has helped to identify various technical gaps in this area of research. Through our work, we have tried to bridge these technical gaps in order to have a better device for low power applications in future. Various research papers, books, monographic and articles have also been studied in the area of nanoscale device modeling and memory circuits design. Article on implementation of FinFET based 6T-SRAM cell which is having low leakage, high SNM and high speed were also studied.

Chapter 3

Quantum Mechanical Analytical Modeling of Nanoscale DG FinFET: Evaluation of Potential, Threshold Voltage and Source/Drain Resistance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3.1 Introduction

ITRS indicates that the improved electrostatic control of the channel will be needed to continue with the same speed enhancement [30]. Thus, as the scaling of CMOS structure is approaching its limits, multiple gate architecture, such as Double Gate FinFET structure presents significant advantages to fulfill long range ITRS requirements. The Poisson's equation based numerical modeling of Double Gate FinFET device has been carried out by many workers [5, 10, 32, 125] which presents generic implicit surface potential solution for FinFET device. For nanoscale multi-gate devices, two dimensional analytical approach would be required which will be valid under Quantum Mechanical (QM) domain of FinFET device under study. For this purpose, we present a fully quantum mechanical surface potential model for the channel region of FinFET device using analytical modeling.

For a CMOS technology to keep pace with down scaling, improved carrier transport and low parasitic source/drain resistance are required. Pei *et.al.,* (2002) [50], investigated FinFET simulation and analytical modeling. Double gate FinFET has been considered as one of the most promising candidate for sub 50 nm designs. But double gate structure suffers from possible misalignment between source/drain with gate region, thereby increasing the overlap capacitances as well as source to drain series resistance. This would result in a slower device and hence, high frequency

operation of the device would be restricted. Fin height and Fin thickness are modified in order to achieve optimized operation of the device. Potential in the active area of FinFET device and threshold voltage have also been evaluated. Dixit *et. al.,* (2005) [6], used a 45 nm FinFET structure to understand the implication of source/drain resistance on the device characteristics. Sub-20 nm FinFET using SiGe as a gate material was developed by Hisamoto *et. al.,* (2000) [29], they showed the ease of fabrication using planer MOSFET process technology. Double Gate FinFET structure offers higher driving capabilities and reduces SCE [73, 74]. To develop sub 50 nm MOSFETs, double gate FinFET structure has been widely studied [137]. For the double gate MOSFETs, the gate controls the energy barrier between source and drain effectively [137]. Further studies have shown [8, 9, 89, 117] that controlling threshold voltage and parasitic for ultra thin body is a difficult task.

The threshold voltage of a transistor is one of the key parameters in the design of FinFET circuits. Katti *et al.* [51] have modeled fully depleted SOI MOSFETs using the solution of three-Dimensional (3-D) Poisson's equation. As the device dimensions continue to scale down to deep sub micrometer regime to obtain better performance, analytical modeling of these devices becomes even more challenging. Although Kedzierski *et al.* (2003) [71] have addressed this issue and proposed a technology solution, an analytical understanding of parasitic series resistance in the FinFET device is desirable. In this chapter, a full quantum mechanical analytical modeling for FinFET structure has been carried out. The subsequent section deals with 3D FinFET structure followed by quantum mechanical potential modeling, threshold voltage modeling and source/drain (S/D) resistance modeling. The results obtained based on our model are compared and contrasted with reported, experimental and simulated results for the purpose of validation and verification of our proposed analytical model.

3.2 FinFET Structure

Figure 3.1 shows 3D view of FinFET. The gate 'wraps' over the thin Si Fin, yielding a quasi-planar symmetrical Double-Gate FinFET structure with two inversion channels that are charge-coupled. Both the front and back gates might have the same work function. They are further tied to same applied potential. The key challenges in the fabrication of Double Gate FinFET devices are [19, 162] self-alignment of the two gates and formation of an ultra-thin silicon film. In FinFET device, the fin is a narrow channel of silicon patterned on an SOI wafer. The gate wraps around the fin on three faces. The top insulator is usually thicker than the side insulators, hence the device has effectively two channels. The top insulator may be reduced in thickness in order to control the channel as well.

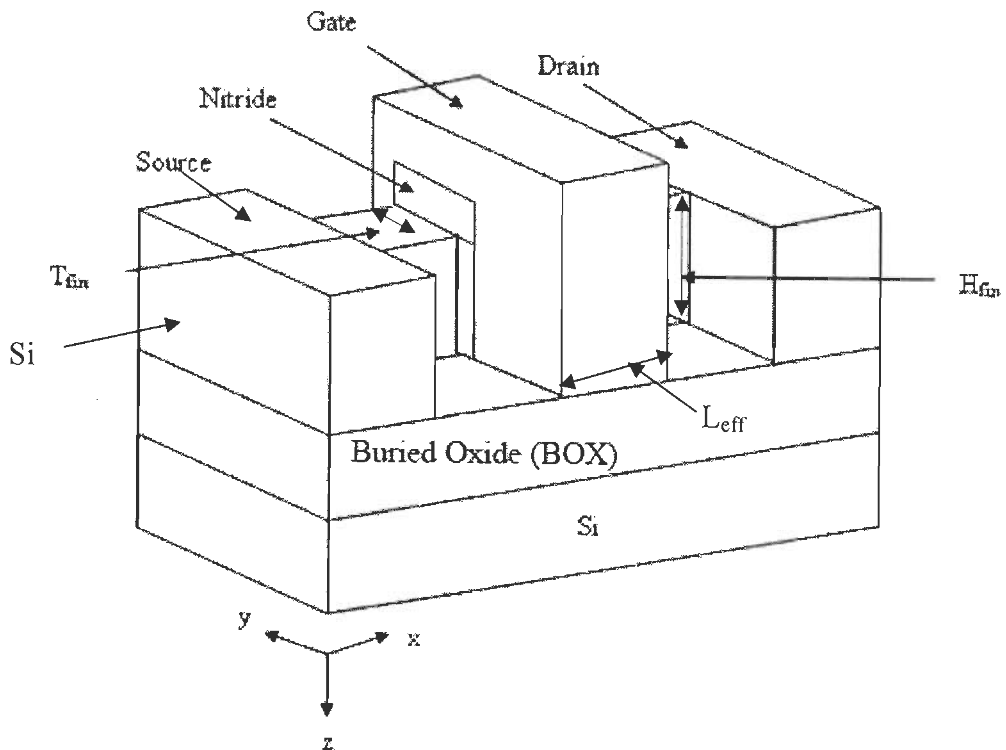


Figure 3.1 Structure of FinFET

3.2.1 Design Parameters

The geometrical parameters of FinFET are indicated in the figure. The definitions of the various parameters seen in figure 3.1 are : L_{eff}: effective channel length of FinFET, which is the actual distance between source and drain region, H_{fin}: height of silicon fin defined by the distance between top gate and buried oxide, T_{fin}: thickness of silicon fin defined as the distance between front and back gate oxides, W_{fin}: geometrical channel width defined as: $W_{fin} = (2 \times H_{fin}) + T_{fin}$. When the thickness of silicon film (T_{fin}) is much larger than its height (H_{fin}) or when top gate oxide is much thinner than the front and back oxides, FinFET can be approximately treated as single-gate Fully Depleted (FD) SOI MOSFET [50].

On the other hand, when height of the silicon film (H_{fin}) is much larger than its thickness (T_{fin}) or top gate oxide is much thicker than the front and back oxides, FinFET can be approximately treated as Double Gate FET device. The two limits of FinFET namely, FD-FET and DG-FET have been widely studied and well understood [10, 89, 117, 134]. To our understanding in the regime where both fin height and thickness have control over short channel effects (SCE), the dependence of SCE on device dimensions is not well extracted or known. For the purpose of understanding the dependence of output characteristics of FinFET with respect to various device/process parameters, a full quantum mechanical analytical potential modeling is carried out in the next section.

3.3 Quantum Mechanical (QM) Potential Modeling

In order to extract full two-dimensional potential profile within the active area of the device, QM solution is carried out. For this purpose, several methods have been proposed [136, 140, 175], where the potential function is divided into two parts, the first one being, the long channel solution and the second one, a short channel evaluation. But the evaluation of short channel term takes into account the functional dependence of device parameters, which is a complicated issue and takes large computational time. For the purpose of simplification and also to have a reduced complexity in time, we have assumed the following dependence of potential, where two dimensional potential is broken down into 1D surface potential and a 2D function [35] as given below:

$$\psi(x,y)=\psi_s(x)\times A(x,y) \tag{3.1}$$

where $\psi_s(x)$ is the surface potential and $A(x,y)$ is the vertical distribution of the envelop function.

A(x, y) as given in equation (3.1) can be written as [35]:

$$A(x,y)=\frac{Z(x,y)}{Z(x,y=1)} \tag{3.2}$$

where Z(x, y) can be written as [35]

$$Z(x,y)=\psi_0(x)-\frac{2}{\beta}\ln\left\{\cos\left[\sqrt{\frac{q^2 n_i}{2kT\varepsilon_{Si}}e^{\frac{\beta(\psi_0(x)-V_F(x))}{2}}}\left(y-\frac{T_{fin}}{2}\right)\right]\right\} \tag{3.3}$$

Where $\beta = q/kT$

The behavior of center potential $\psi_0(x)$ as a function of effective gate voltage is given as [10]:

$$\psi_0(x)=U-\sqrt{U^2-(V_{gs}-V_{FB})\psi_{0\max}(x)} \tag{3.4}$$

where $\psi_{0\max}(x)$ is the maximum potential that can be obtained at the center of the channel under a given bias at the terminal and U is given as

$$U=\frac{1}{2}\left[(V_{gs}-V_{FB})+(1+r)\psi_{0\max}(x)\right] \tag{3.5}$$

$\psi_{0\max}(x)$ can be evaluated as:

$$\psi_{0\max}(x)=V_F(x)+\frac{1}{\beta}\ln\left(\frac{2\pi^2\varepsilon_{Si}kT}{q^2n_iT_{fin}^2}\right) \tag{3.6}$$

where r in equation (3.5) is defined as smoothing parameter which weakly depends on oxide and silicon thickness and quasi Fermi potential which is given by [35]:

$$r=(At_{ox}+B)\left(\frac{C}{T_{fin}}+D\right)e^{-EV_F(x)} \tag{3.7}$$

The optimized value of A, B, C, D and E are given as 0.0267 nm^{-1}, 0.0270, 0.4526 nm, 0.0650 and 3.2823 V^{-1} respectively. The optimized values obtained are for the device dimensions of $t_{ox} < 10$ nm and $T_{fin} > 5$ nm [35]. Extensive numerical simulations show that quasi fermi potential also depends on gate voltage, effective channel length and fin thickness and is given by a semi empirical relationship as

$$V_F(x)=\frac{2kT}{q}\frac{m}{n}\ln\left[\left(\exp\left(-\frac{V_{ds}(m/n)^{-1}}{kT/q}\right)-1\right)\left(\frac{x}{L_{eff}}\right)^{\frac{c}{V_{gs}-V_{FB}}}+1\right]^{-1}\times(a\times T_{fin})^{\frac{V_{ds}}{3c}} \tag{3.8}$$

where $\frac{m}{n}=2+b(V_{gs}-V_{FB})$, a=0.2 nm^{-1}, b=7.5 V^{-1}, c= 1 V and V_{ds} is the applied drain voltage. The quasi fermi potential given in equation (3.8) is a function of position along the channel length and drain voltage V_{ds}. Substituting the value of $\psi_0(x)$ from equation (3.4) and $V_F(x)$ from equation (3.8) in equation (3.3), we obtain Z(x, y) as:

$$Z(x,y) = (U - \sqrt{U^2 - (V_{gs} - V_{FB})\psi_{0\max}(x)}) - \frac{2}{\beta}\ln$$

$$\left\{ \cos\left[\sqrt{\frac{q^2 n_i}{2kT\varepsilon_{Si}}} e^{\frac{\beta\left(\left(U-\sqrt{U^2-(V_{gs}-V_{FB})\psi_{0\max}(x)}\right)-\left(\frac{2kT}{q}\frac{m}{n}\ln\left[\left(\exp\left(-\frac{V_{ds}(m/n)^{-1}}{kT/q}\right)-1\right)\left(\frac{x}{L_{eff}}\right)^{\frac{c}{V_{gs}-V_{FB}}}+1\right]^{-1}\times(a\times T_{fin})^{\frac{V_{ds}}{3c}}\right)\right)}{2}} \left(y - \frac{T_{fin}}{2}\right) \right] \right\}$$

(3.9)

An expression of Z(x, y) is used to obtain the analytical solution of the function A(x,y). The solution of one-dimension Poisson equation is:

$$\psi_s(x) = C_1 \exp(m_1 x) + C_2 \exp(-m_1 x) - \frac{R}{m_1^2} \qquad (3.10)$$

where C_1, C_2, m_1 and R are calculated by putting the following boundary conditions based on the physics of the device as:

$\psi_s(x=0) = \phi_s$ and $\psi_s(x = L_{eff}) = \phi_s + V_{ds}$

We obtained the values of the parameters as:

$$C_1 = \frac{\phi_S[1-\exp(-m_1 L_{eff})] + V_{ds} + \frac{R[1-\exp(-m_1 L_{eff})]}{m_1^2}}{2\sinh(m_1 L_{eff})} \qquad (3.11)$$

$$C_2 = -\frac{\phi_S[1-\exp(+m_1 L_{eff})] + V_{ds} + \frac{R[1-\exp(+m_1 L_{eff})]}{m_1^2}}{2\sinh(m_1 L_{eff})} \qquad (3.12)$$

$$R = \frac{\eta}{\varepsilon_{Si} T_{fin}}\left[qN_a T_{fin} - 2C_{ox}(V_{gs} - V_{FB} - \phi_F)\right] \qquad (3.13)$$

$$m_1 = \sqrt{\frac{2\eta C_{ox}}{\varepsilon_{Si} T_{fin}}}$$

where η is a fitting parameter which incorporates the effects of the variation of the lateral field on the depleted film under the channel. As demonstrated by Harrison,

et.al., 2004 [63], η is lower than 1 for $V_{gs} \leq V_{th}$ and depends on the channel doping concentration and thickness. Therefore, this parameter has to be calibrated for each technology. $C_{ox} = \varepsilon_{ox} / t_{ox}$ is the oxide capacitance per unit area and N_a is the channel doping. Substituting the value of C_1, C_2 *and* R in equation (3.10), surface potential, $\psi_s(x)$ is obtained as:

$$\psi_s(x) = \left(\frac{\phi_S[1-\exp(-m_1 L_{eff})] + V_{ds} + \dfrac{R[1-\exp(-m_1 L_{eff})]}{m_1^2}}{2\sinh(m_1 L_{eff})} \right) [\exp(m_1 x)] + \left(\frac{\phi_S[1-\exp(+m_1 L_{eff})] + V_{ds} + \dfrac{R[1-\exp(+m_1 L_{eff})]}{m_1^2}}{2\sinh(m_1 L_{eff})} \right) [\exp(-m_1 x)] - \frac{\left(\dfrac{\eta}{\varepsilon_{Si} T_{fin}} \left[q N_a T_{fin} - 2C_{ox}(V_{gs} - V_{FB} - \phi_F) \right] \right)}{m_1^2} \tag{3.14}$$

From equation (3.2) and equation (3.14), we obtained the full QM two dimensional surface potential as:

$$\psi(x,y) = \left[\left(\frac{\phi_S[1-\exp(-m_1 L_{eff})] + V_{ds} + \dfrac{R[1-\exp(-m_1 L_{eff})]}{m_1^2}}{2\sinh(m_1 L_{eff})} \right) [\exp(m_1 x)] + \left(\frac{\phi_S[1-\exp(+m_1 L_{eff})] + V_{ds} + \dfrac{R[1-\exp(+m_1 L_{eff})]}{m_1^2}}{2\sinh(m_1 L_{eff})} \right) [\exp(-m_1 x)] - \frac{\left(\dfrac{\eta}{\varepsilon_{Si} T_{fin}} \left[q N_a T_{fin} - 2C_{ox}(V_{gs} - V_{FB} - \phi_F) \right] \right)}{m_1^2} \right] \times \frac{Z(x,y)}{Z(x,y=1)} \tag{3.15}$$

3.4 Threshold Voltage Modeling

The threshold voltage of a FinFET can be defined as that voltage (gate) which would be able to invert all the channels within the Fin structure simultaneously. We can derive the QM threshold voltage, $V_{th,QM}$ of the DG FinFET as [104]:

$$V_{th,QM} = V_{FB} + \psi_{s(inv)} - \frac{Q_b}{2C_{ox}} + \Delta V_{th,QM} \tag{3.16}$$

where $\psi_{s(inv)}$ is the surface potential at threshold, $\Delta V_{th,QM}$ is the threshold voltage change due to QME's, which can be approximated as a function of the ratio of the carrier effective mass in the direction of confinement to the free electron mass and silicon film thickness which is given as [156]:

$$\Delta V_{th,QM} \cong \frac{S}{(kT/q)\ln(10)} \times \frac{0.3763}{(m_x/m_o)T_{fin}^2} \tag{3.17}$$

where S is the subthreshold slope, T_{fin} is fin thickness and m_x/m_o is the ratio of the carrier effective mass in the direction of confinement to the free electron mass (e.g., 0.92 for electrons and 0.29 for holes).

The bulk charge Q_b is given as:

$$Q_b = -qN_aT_{fin} \tag{3.18}$$

When considering the quantum-mechanical confinement of inversion-layer carriers, $V_{th,QM}$ of equation (3.16) should be augmented with $\Delta V_{th,QM}$. The surface potential at threshold is given by:

$$\psi_{s(inv)} = 2\psi_b \tag{3.19}$$

$$\psi_b = \frac{kT}{q}\ln\left(\frac{N_a}{N_i}\right) \tag{3.20}$$

Substituting the value of ψ_b from equation (3.20) into equation (3.19), we obtained:

$$\psi_{s(inv)} = 2\left(\frac{kT}{q}\ln\left(\frac{N_a}{N_i}\right)\right) \tag{3.21}$$

Substituting the value of Q_b from equation (3.18), $\psi_{s(inv)}$ from equation (3.21) and $\Delta V_{\mathrm{th,QM}}$ from eq. 3.17 into threshold expression eq. 3.16, the final expression for the threshold voltage with QM corrections is obtained as:

$$V_{th,QM} = V_{FB} + 2\left(\frac{kT}{q}\ln\left(\frac{N_a}{N_i}\right)\right) - \frac{\left(-qN_aT_{fin}\right)}{2C_{ox}} + \frac{S}{(kT/q)\ln(10)} \times \frac{0.3763}{(m_x/m_o)T_{fin}^2} \tag{3.22}$$

3.5 Source/Drain (S/D) Resistance Modeling

The quasi nonplanar devices suffer from a high parasitic resistance due to narrow width of their source/drain (S/D) regions. The series resistance in the S/D regions of a FinFET has contributions from its components arising from different parts of the S/D geometry. The enhanced total resistance of FinFET reduces the driving capability of the device at all applied biases. We analyzed the parasitic S/D resistance and the total resistance of FinFET device using analytical model. The sheet resistance R_{sh} in the S/D extension is given by [6]:

$$R_{sh} = \rho_{ext}\left(\frac{W_{sp}}{H_{fin} \times W_{fin}}\right) \tag{3.23}$$

where ρ_{ext} is the resistivity of the S/D extension, W_{sp} is the length of S/D extension.

Spread resistance (R_{sp1}) is due to the spread of current from the thin accumulation layer into the S/D extension which can be written as [6]:

$$R_{sp1} = \frac{1}{2} \times \left[\frac{2\rho_{ext}}{\pi H_{fin}} \ln\left(0.75 \frac{\left(\frac{W_{fin}}{2}\right)}{x_c} \right) \right] \tag{3.24}$$

where x_c is the channel thickness. R_{sp2} is the resistance due to the spread of current from S/D extensions into the wider Heavily Doped S/D (HDD) region and is given as [6].

$$R_{sp2} = \frac{\rho_{hdd} \times \left[\ln(0.75) + \ln(W_{sd}) - \ln(W_{fin}) \right]}{\pi\left(H_{fin} + T_{SEG} - T_{SIL}\right)} \tag{3.25}$$

where T_{SIL} is the thickness of the S/D silicide and T_{SEG} is S/D SEG thickness.

R_{sd} has been modeled as series combination of two resistances: R_1 and R_2 and is given be:

$$R_{sd} = 2 \times (R_1 + R_2) \tag{3.26}$$

R_1 is the resistance between the gate and S/D spacer edge.

$$R_1 = R_{sp1} + R_{sh} \tag{3.27}$$

Substituting the value of R_{sh} and R_{sp1} from equation (3.23) and equation (3.24) in equation (3.27), we get the value of R_1 as:

$$R_1 = \left(\frac{1}{2} \times \left[\frac{2\rho_{ext}}{\pi H_{fin}} \ln\left(0.75 \frac{\left(\frac{W_{fin}}{2}\right)}{x_c} \right) \right] \right) + \left(\rho_{ext} \left(\frac{W_{sp}}{H_{fin} \times W_{fin}} \right) \right) \tag{3.28}$$

Also R_2 is the parallel combination of resistance of plane A-A' and plane B-B' (Figure 3.2) and is given by

$$R_2 = \frac{R_a \times R_b}{R_a + R_b} \tag{3.29}$$

$R_a = R_{conA}$ and $R_b = R_{sp2} + R_{conB}$, R_{conA} is contact resistance of plane A-A' and R_{conB} is contact resistance of plane B-B'.

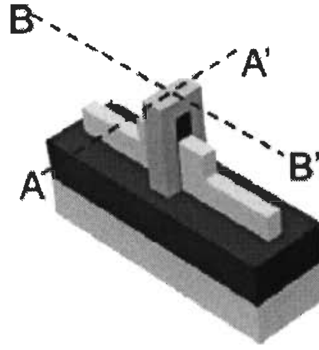


Figure 3.2 Geometry of the FinFET device [6]

Contact resistance in plane A-A' (Figure 3.2) is given:

$$R_{conA} = \frac{\rho_{\text{int}}}{W_{fin} \times T_{SIL}} \tag{3.30}$$

where ρ_{int} is the contact resistivity. Contact resistance in plane B-B' (Figure 3.3) is given by:

$$R_{conB} = \frac{\rho_{\text{int}}}{\left(L_{transfer} \times W_{sd}\right)} \coth\left(\frac{L_{con}}{L_{transfer}}\right) \tag{3.31}$$

where L_{con} is the physical length and W_{sd} is the width of HDD region. In case of the current conduction parallel to a semiconductor-metal interface, a minimum contact length exists before this conduction current is actually transferred from the semiconductor to the metal. This length is known as transfer length ($L_{transfer}$).

Substituting the value of R_1 and R_2 from equation (3.28) and equation (3.29) in eq (3.26), we get the S/D resistance (R_{sd}) as:

$$R_{sd} = 2\times\left(\left(\left(\frac{1}{2}\times\left[\frac{2\rho_{ext}}{\pi H_{fin}}\ln\left(0.75\frac{\left(\frac{W_{fin}}{2}\right)}{x_c}\right)\right]\right)+\left(\rho_{ext}\left(\frac{W_{sp}}{H_{fin}\times W_{fin}}\right)\right)\right)+\left(\frac{R_a\times R_b}{R_a+R_b}\right)\right) \tag{3.32}$$

The total resistance is obtained as:

$$R_{total} = \frac{V_{ds}}{I_s} = R_{ch} + R_{sd} \tag{3.33}$$

where R_{ch} is the resistance of channel region. From eq (3.32), substitute the value of R_{sd} in eq (3.33). The final expression for the total resistance is obtained as given below:

$$R_{total} = R_{ch} + \left(2\times\left(\left(R_{sp1}+R_{sh}\right)+\left(\frac{R_a\times R_b}{R_a+R_b}\right)\right)\right) \tag{3.34}$$

3.6 Results and Discussion

A full two dimensional potential analytical modeling scheme taking into consideration various quantum mechanical effects has been presented for FinFET structure for a channel length of 30 nm, fin thickness of 10 nm and fin height of 30 nm. For the purpose of validation of our analytical model, the results obtained have been compared and contrasted with reported simulated results as well as experimental results.

Figure 3.3 shows the variation of surface potential with distance along the channel length obtained on basis of our model and reported simulation results. The device parameters used for the analysis are shown within the figure. It can be seen from the figure that there is a good match between the reported and result obtained through our modeling at any point along the channel length from source to drain. It

can be observed that the potential initially falls to a minimum value near the source end and then monotonically increases at the drain end. At any point along the channel length, our model predicts a lower value of surface potential as compared to the simulated results. The small deviation seen in the results might be due to variation of carrier mass due to quantum confinement at an applied drain and gate voltage of 0.4 V and 1 V respectively.

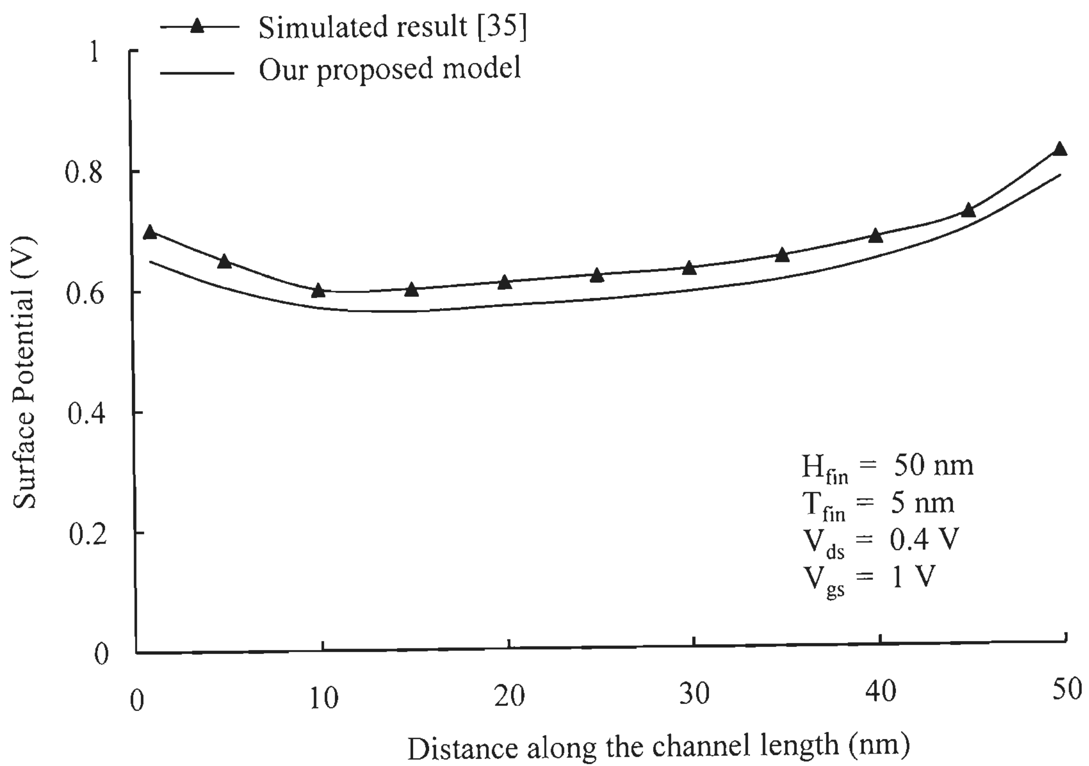


Figure 3.3 Surface potential variations along the channel length for comparing our quantum result and through reported simulation result [35]

Figure 3.4 shows the variation of three-dimensional surface potential profile in the active region of the device. It can be seen from the figure that there is an increase in the potential along the channel length toward the drain end. It can be also be observed that the potential variation from the gate to gate at drain is more pronounced

as compared to the variation at the source end. This is due to a large transverse as well as longitudinal direction electric field within the channel near the drain end as compared to source end.

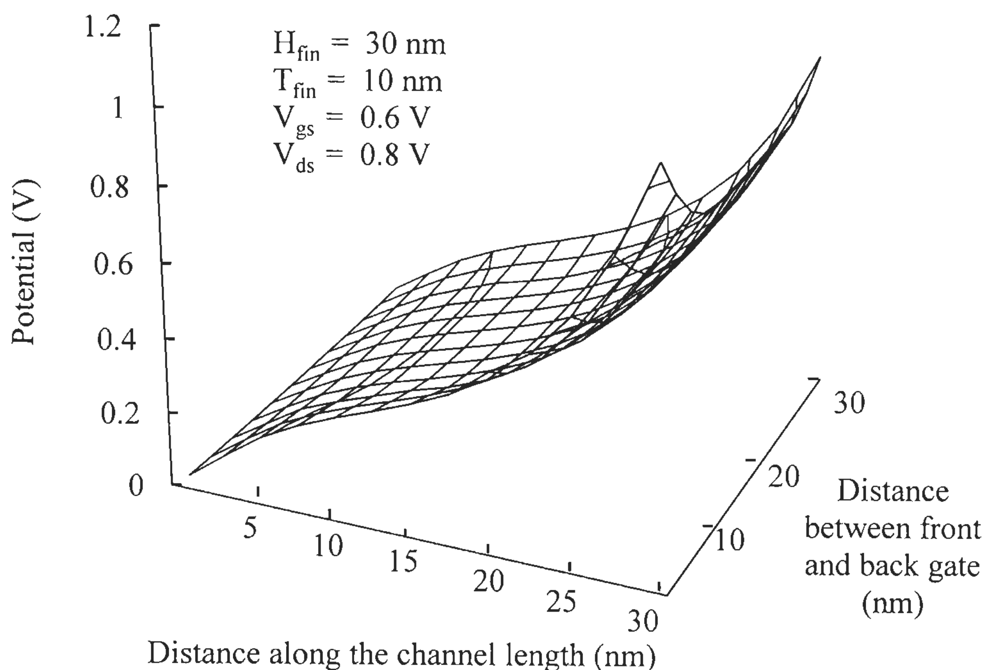


Figure 3.4 3D potential plot of FinFET for 30 nm channel length

The variation of channel potential from front gate to back gate at various distances from source side for fixed drain and gate bias is shown in figure 3.5. The gate length, fin height and thickness have been taken as 30 nm, 30 nm and 10 nm respectively. It can be seen from the figure that as we move from source end of the gate to the drain end of the gate, there is substantial increase in the potential at any point in the channel. This is attributed to the increased value of longitudinal electric field at the drain end on application of a drain to source voltage. It can be further observed that near the source end, the potential is almost constant as one moves from

front to back gate. But near the drain end, the variation of potential near either of the gates is very drastic. This is because of larger effective gate voltage at the drain end of the device as compared to the source end. This also implies that the longitudinal electric field is enhanced near the Si-SiO_2 interface due to its proximity to metal gates.

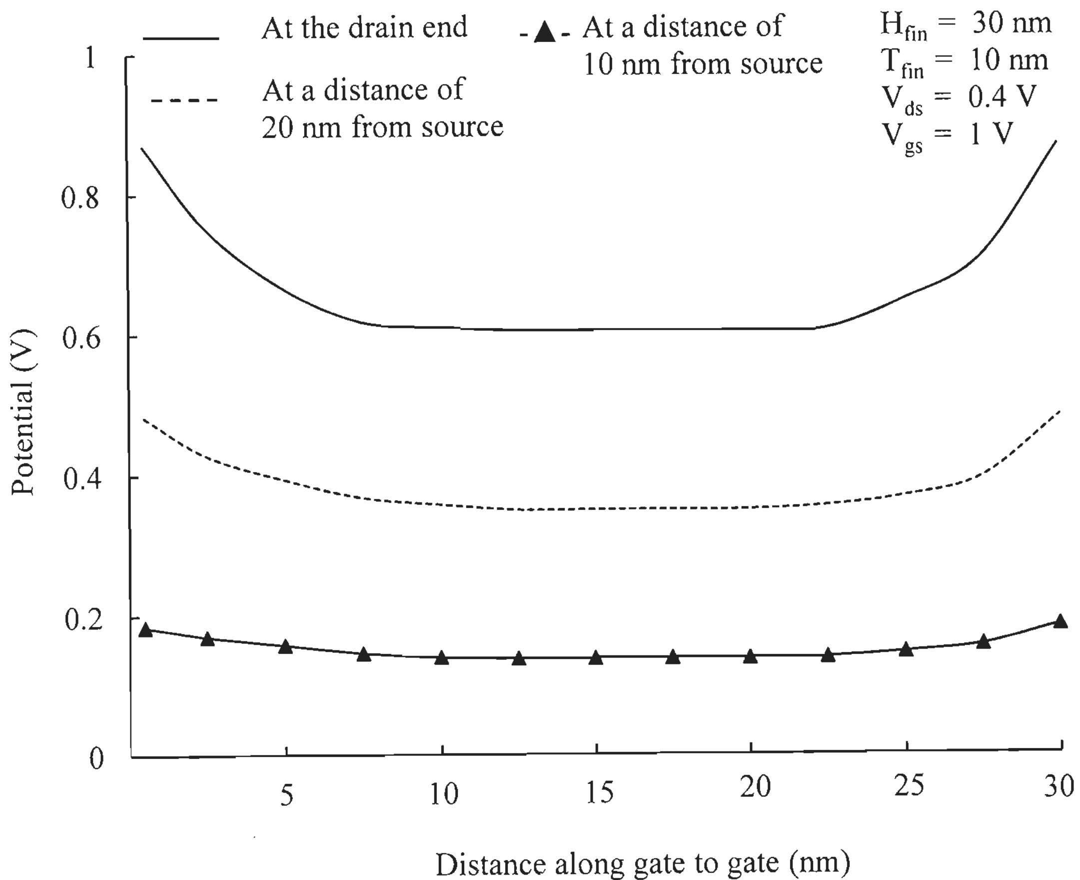


Figure 3.5 Potential variations from front gate to back gate at various positions along the channel length

Variation of threshold voltage with fin thickness for our quantum mechanical model and experimental results has been shown in figure 3.6 for the purpose of comparison. A threshold voltage roll-off with fin thickness is observed for both theoretical and experimental results. The fin thickness is varied from 5 nm to

55 nm. The percentage roll-off for our model is 77 % and that for experimental result it is 75 %. It can be inferred, therefore that there is a close match of percentage variation between our results and experimental measurement, given the fact that the device process parameters undergo fluctuations at such low dimensions.

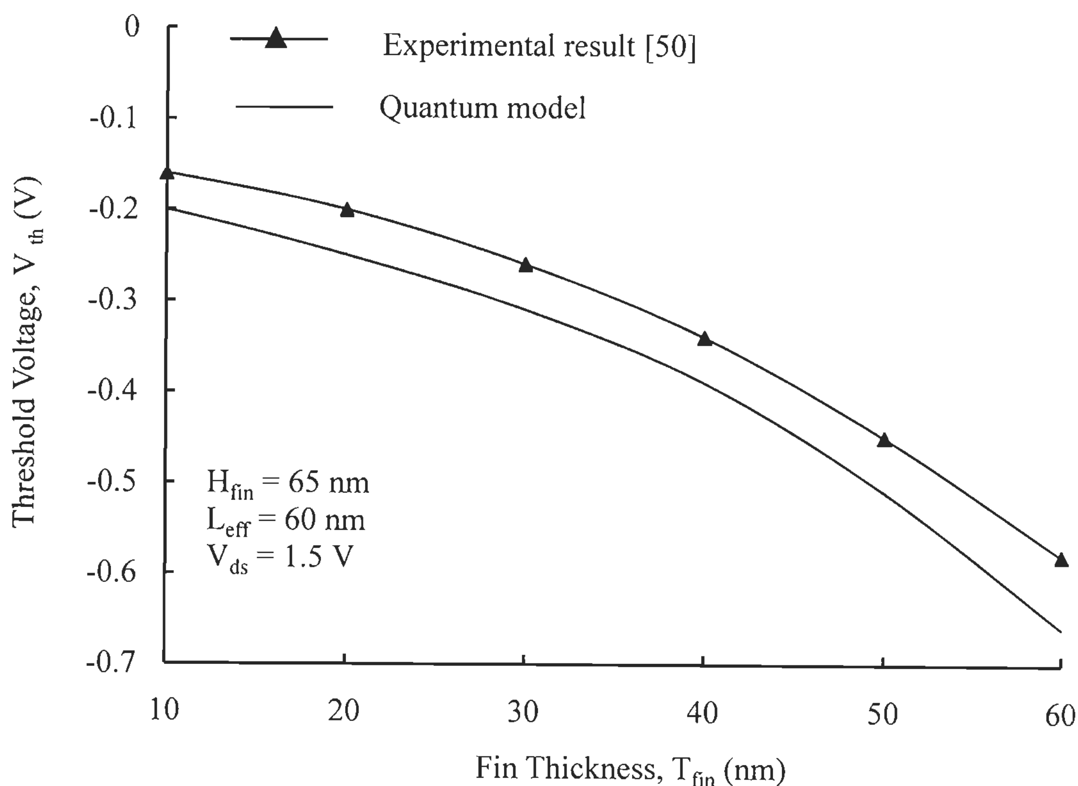


Figure 3.6 Variation of threshold voltage with Fin thickness for our proposed QM model and experimental reported result [50]

Figure 3.7 shows the variation of threshold voltage with fin thickness for varying fin height. It can be seen from the figure that as the fin height increases, the rate of reduction of threshold voltage with fin thickness also increases. Moreover, the absolute value of threshold shows an enhancement with larger fin thickness. This is because at larger fin thickness, the top gate of the fin is able to control the channel

charge to a lesser amount. Hence, there is an increase in threshold voltage. It can be further seen that as fin thickness increases, the transverse electric field reduces and hence a larger gate voltage is required in order to form channel, thereby increasing threshold voltage.

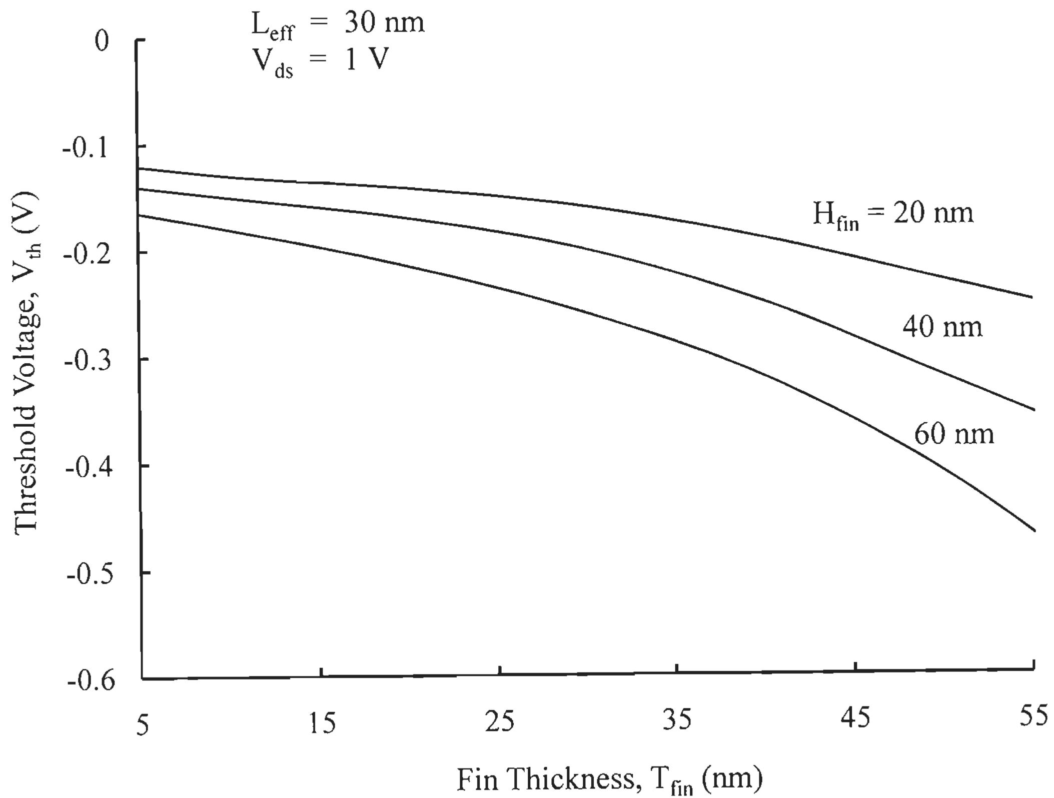


Figure 3.7 Variation of threshold voltage with fin thickness for various fin height

The Variation of threshold voltage with fin height for varying fin thickness is shown in figure 3.8. From this figure, it may be seen that as the fin thickness increases, the rate of reduction of threshold voltage with fin height also increases. This is because as the fin thickness increases, the effective area under the gate also increases, thus increasing threshold voltage.

Figure 3.9 shows the variation of parasitic S/D resistance with varying fin width for our proposed analytical model and reported numerical result [6] for the purpose of validation for all fin width. A close match is found between the two results for channel length of 30 nm.

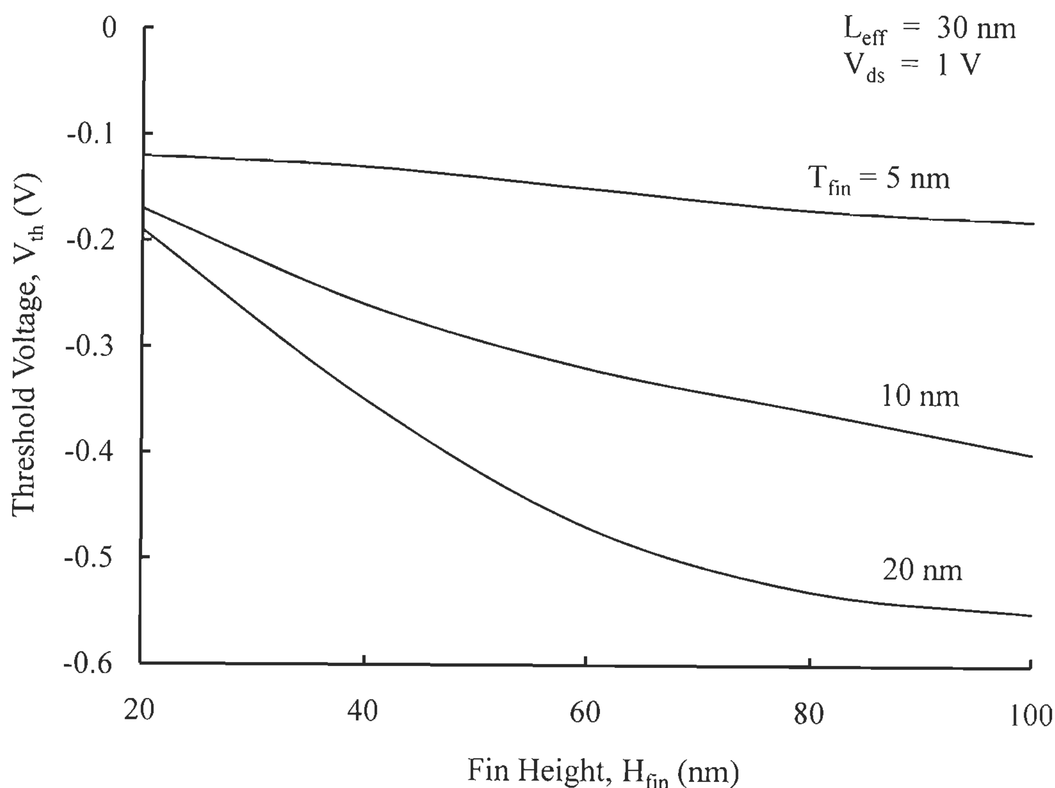


Figure 3.8 Variation of threshold voltage with fin height for various fin thickness

It can be seen from the figure that as the fin width increases, there is a decrease in the parasitic resistance for all values of channel length. As the fin width increases, the total area through which drain current flows also increases. This results in a decrease in the parasitic resistance. Further it is observed that for a fixed fin width, as the channel length increases, there is an enhancement in the parasitic S/D resistance. This can be inferred from the fact as the channel length decreases,

quantum confinement along the S/D direction becomes more extensive. This results in an enhancement in the mobility of charge carriers which in turn increase the drain current and hence the parasitic S/D resistance decrease.

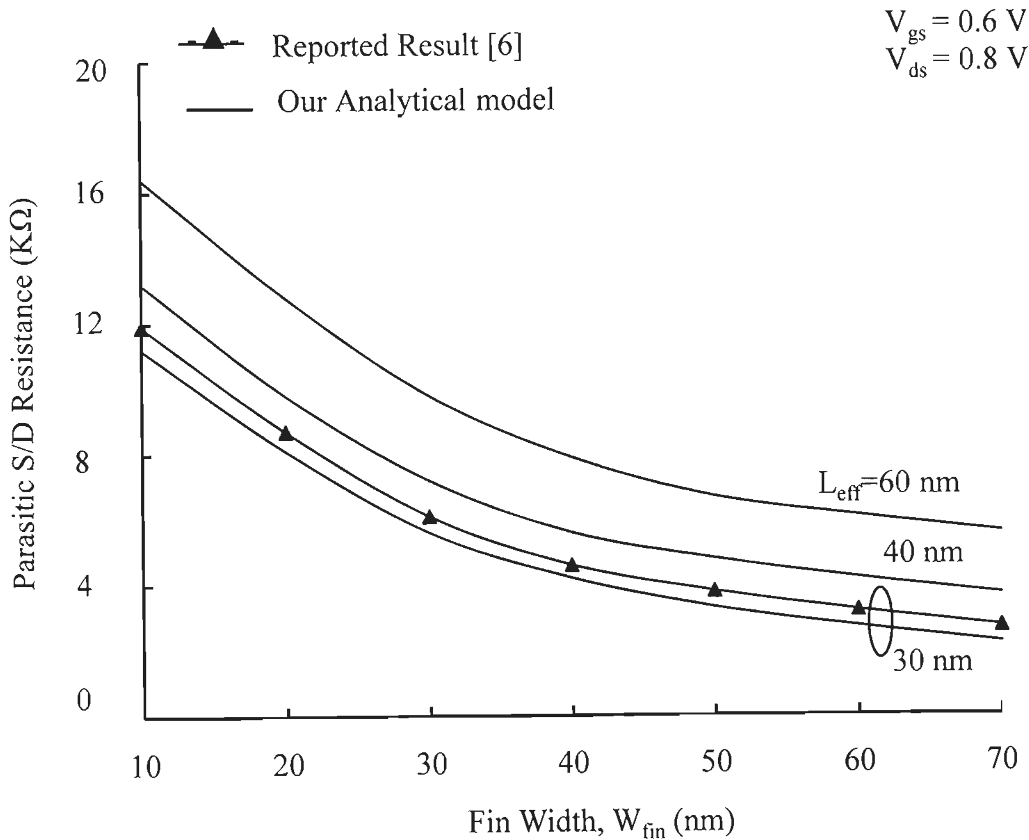


Figure 3.9 Variation of Parasitic S/D Resistance with varying Fin width for proposed analytical model and reported result [6]

Figure 3.10 shows the variation of total resistance between S and D with variation of gate voltage. The results obtained by our analytical model have been compared with the reported numerical result [6] for W_{fin} = 18 nm. The variation is also shown for fin width of W_{fin} = 40 nm and 80 nm. It observed that as the fin width increases, there is almost linear decrease in the total resistance for a fixed applied gate

voltage. Further for large gate voltage, the total resistance becomes almost independent of applied gate voltage.

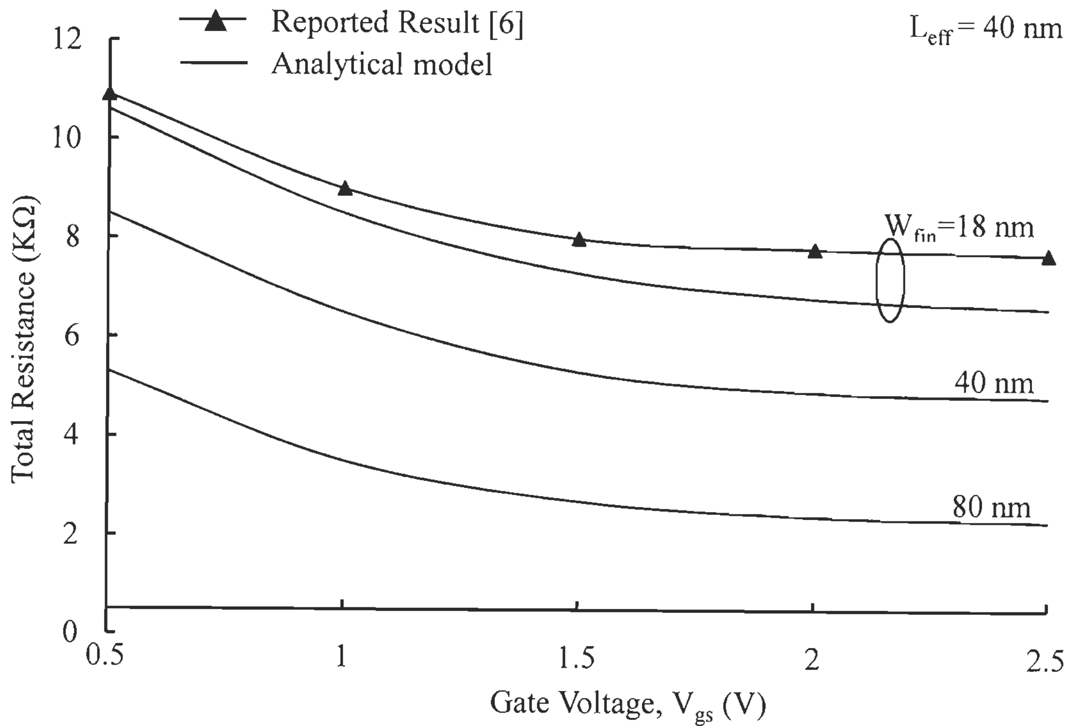


Figure 3.10 Variation of total Resistance with variation of gate voltage for varying Fin width

3.7 Conclusion

In this chapter, a full 2D quantum mechanical analytical modeling has been presented in order to evaluate the 2D potential profile within the active area of FinFET structure. The key issues related to device parameters and structures are also shown in the chapter. The variation of potential from gate to gate is also reported in this chapter. For potential profile, there is close match between our results and reported experimental results. The results obtained would be useful to design device and for fabricating future nanoscale devices. Various potential profiles such as

surface, back to front gate and source to drain potential have been presented in order to appreciate the usefulness of the device for circuit simulation purposes. Further, in this chapter, the detailed study of threshold voltage and its variation with the process parameters is presented for our proposed devices and a close match is obtained with the results through analytical model and reported experimental results.

Chapter 4

Analytical Modeling of Nanoscale Double Gate FinFET: Evaluation of Inversion Charge, Mobility and Drain Current

4.1 Introduction

The advantages advocated for DG FinFETs are excellent scalability due to superior immunity to SCE, near-ideal subthreshold slope, near-ballistic drive current and low subthreshold intrinsic capacitance. FinFET devices are used for low power applications such as portable devices where the reliability and durability are the most important factors. Analytical modeling of FinFET device has been of great interest. For FinFET nanoscale device, large numbers of parameters are required to improve the accuracy. Inversion charge and mobility are the key physical quantities, based on which the characteristics such as current-voltage can be easily obtained. Hence, modeling of inversion charge, mobility and drain current analytical modeling has been carried out in this chapter.

Further, for the DG FinFET device, the condition of "volume inversion" [102] can be beneficial with regard to carrier mobility and source-drain transport. The design of optimal DG FinFET devices will require new insights into the underlying physics, especially the quantum mechanics of the carriers confined in very thin (≈nm) Si films. Quantum Mechanical (QM) confinement of inversion-layer carriers significantly affects the threshold voltage and gate capacitance of highly scaled FinFETs. For FinFET device, because of the restricted momentum in the direction normal to the surface, inversion carriers must be treated quantum-mechanically as a two-dimensional (2-D) gas [102, 116]. Thus, the energy levels of the carriers are

grouped in discrete subbands each of which corresponds to a quantized level for the lack of motion in the normal direction with a continuum of levels for the free motion in the plane parallel to the surface.

The scaling of the MOSFET to nano scale dimensions also demands high channel doping concentrations. At such short gate lengths, the statistical fluctuations of the doping in the channel introduce an appreciable dispersion of threshold voltages which may become an important limitation [3]. Furthermore, a large channel doping increases the source–drain junction capacitance and reduces effective mobility thus affecting the device performance for a given channel length. In order to face these scaling challenges, a different approach is to move on to new device architectures [14, 17, 23]. The double gate (DG) FinFET realized on Ultra-Thin (UT) silicon films is usually considered as the most promising architecture for scaling CMOS into the sub-50 nm regime, enabling higher drive currents, improved subthreshold slope and short channel effects and/or relaxing technological constraints encountered in the conventional bulk architecture [82-85].

The double-gate ultrathin-body structure such as FinFETs has attracted much attention because of the superior immunity to SCE and the mobility enhancement due to the volume inversion. For device and circuit simulations, it is not clear how the anisotropy in mobility can be accommodated in the models for accurate prediction of device and circuit behavior. Hence, a method to extract the field dependent mobility would help process and device optimization and also accurate transport modeling. A large channel doping increases S/D junction capacitance and reduces the effective mobility [2, 26, 158].

In this chapter, we have carried out a full quantum `mechanical analytical modeling for a FinFET structure with electrical channel length of 30 nm, fin thickness

20 nm and fin height 30 nm for the purpose of evaluating charge and output characteristics. The quantum inversion charge has been evaluated in the active area of device taking into account carrier confinement in the silicon film. The subsequent section deals with field dependent mobility modeling and drain current modeling for extracting output characteristics. The results obtained based on our model are compared and contrasted with reported experimental results and our simulated TCAD results for the purpose of validation and verification of our proposed analytical model.

4.2 Quantum Inversion Charge Modeling

It may be noted that 3D FinFET device architecture can be approximated as a 2D double gate MOSFET architecture if we consider top gate oxide thickness to be large, hence as compared to top gate, front and back gate control the channel more effectively. In order to take into account carrier confinement in silicon fin, the expression for the inversion charge can be quantum mechanically evaluated as [35]:

$$q_i(x) = \frac{qkT}{\pi\hbar}\sum_{l,t}\sum_{i} m_{2D}^{l,t} g_{l,t} \times \ln\left[1+\exp\left(-\beta\left(\widetilde{E}_{l,t}^{i} + \frac{E_g}{2} - \psi_s(x) + V_F(x)\right)\right)\right] \tag{4.1}$$

where $m_{2D}^{l} = m_t^*$, $m_{2D}^{t} = \sqrt{m_l^* m_t^*}$, $m_t^* = 0.19 \times m_0$

$m_l^* = 0.98 \times m_0$, $g_l = 2$, $g_t = 4$ [35].

where m_t and m_l are the effective masses of electron in transverse and longitudinal directions respectively and E_g is the band gap energy. In eq. (4.1) $\widetilde{E}_{l,t}^{i}$ are the energy levels calculated using standard method for first order perturbation applied to energy levels of an infinite rectangular well and is given as [63]:

$$\widetilde{E}_{l,t}^{i} = E_{l,t}^{i} + \Delta E^{i} \tag{4.2}$$

where $E^{i}_{l,t}$ are the energy levels of infinite rectangular well given by:

$$E^{i}_{l,t} = \frac{\hbar^2 \pi^2 i^2}{2qm^{*}_{l,t} T^2_{fin}} \tag{4.3}$$

where i correspond to various energy levels and $m^{*}_{l,t}$ is effective mass of electron in longitudinal or transverse direction. For our model, we have taken i=1 for the lowest energy level where the carrier population is maximum. Considering the parabolic nature of the potential profile in the silicon film, the first-order correction applied to the energy levels in the well ΔE^{i} is given by [63]:

$\Delta E^{i} = \langle \varphi^{i} | H | \varphi^{i} \rangle$ and $H = -q(-\alpha T_{fin} y + \alpha y^2)$

where H is Hamiltonian of the perturbation, φ^{i} are the electron wave functions associated to energy levels $E^{i}_{l,t}$. An elementary calculation gives ΔE^{i} in the case of an infinite rectangular well as [63]:

$$\Delta E^{i} = \frac{\alpha T^2_{fin}}{6} \left[1 + \frac{3}{\pi^2 i^2} \right] \tag{4.4}$$

Substituting the value of $E^{i}_{l,t}$ from eq. (4.3) and ΔE^{i} from eq. (4.4) in eq (4.2), we obtain $\widetilde{E}^{i}_{l,t}$ as:

$$\widetilde{E}^{i}_{l,t} = \frac{\hbar^2 \pi^2 i^2}{2qm^{*}_{l,t} T^2_{fin}} + \frac{\alpha T^2_{fin}}{6} \left[1 + \frac{3}{\pi^2 i^2} \right] \tag{4.5}$$

Substituting the value of $\widetilde{E}^{i}_{l,t}$ from eq. (4.5) and $V_F(x)$ from eq. (3.8) in Chapter 3 on to quantum inversion charge formulation eq. (4.1), we obtain the final value of space dependent quantum inversion charge as:

$$q_i(x) = \frac{qkT}{\pi\hbar} \sum_{l,t} \sum_{l} m_{2D}^{t,l} g_{t,l}$$

$$\times \ln \left[1 + \exp \left(-\beta \left(\left(\frac{\hbar^2 \pi^2 i^2}{2qm_{l,t}^* T_{fin}^2} + \frac{\alpha T_{fin}^2}{6} \left[1 + \frac{3}{\pi^2 i^2} \right] \right) + \frac{E_g}{2} - \psi_s(x) + \left(\frac{2kT}{q} \frac{m}{n} \ln \left[\left(\exp \left(-\frac{V_{ds}(m/n)^{-1}}{kT/q} \right) - 1 \right) \left(\frac{x}{L_{eff}} \right)^{\frac{c}{V_{gs} - V_{FB}}} + 1 \right]^{-1} \times (a \times T_{fin})^{\frac{V_{ds}}{3c}} \right) \right) \right) \right] \tag{4.6}$$

4.3 Mobility Modeling

For the purpose of evaluating the field dependent mobility of the charge carriers in FinFET, the electric field in the transverse direction is to be evaluated. This can be found out from the potential variation of one gate to another. The model assumes that the channel mobility is the sum of the reciprocal mobility derived from three different scattering mechanisms. These three different scattering mechanisms are coulomb, phonon, and surface roughness scattering.

$$\frac{1}{\mu} = \frac{1}{\mu_c} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} \tag{4.7}$$

The coulomb limited mobility term based on the Boltzman transport equation has been extensively studied [34, 100, 109]. This includes scattering of electrons from both the repulsive coulomb potential due to ionized acceptor atoms and the attractive coulomb potential due to positive interfacial charge for electrons as charge carriers. The coulomb mobility is given as [34]:

$$\mu_c = a_1^{-1} T \tag{4.8}$$

where a_1 is a parameter to be extracted [2] and T is the absolute temperature. The phonon scattering limited mobility is taken into consideration with dependency of crystallographic orientation. This interface- state density dependent mobility shows the dependency on temperature. The mobility μ_{ph} is given as [34]

$$\mu_{ph} = a_2^{-1} T^{-n} E_{eff}^{-1/\gamma} \tag{4.9}$$

where a_2 is a parameter to be extracted [2]. This constant can be empirically derived. Surface roughness scattering limited mobility constitutes a major cause of scattering at high electron concentrations. At low temperatures and high transverse electric fields, the surface roughness scattering strongly degrades the surface mobility and field effect mobility. As surface roughness scattering is independent of temperature and can be modeled for high electric fields as [34]

$$\mu_{sr} = a_3^{-1} E_{eff}^{-2} \tag{4.10}$$

where a_3 is a parameter to be extracted [2]. From these above models, the effective mobility model for electric field at room temperature can be obtained by putting the values of μ_c, μ_{ph}, μ_{sr} from equations (4.8), (4.9) and (4.10) in equation (4.7). Thus we get:

$$\mu_{eff} = \frac{1}{a_1/T + a_2 T^n E_{eff}^{1/\gamma} + a_3 E_{eff}^{2}} \tag{4.11}$$

4.4 Drain Current Modeling

For calculating the quantum mechanical drain current in FinFET device, the drift and diffusion components of the drain current have been evaluated. The modeling of drain current is carried out using current density expression [35, 93] as:

$$J = -q\mu_{eff} n(x,y) \frac{dV_F(x)}{dx} \tag{4.12}$$

where μ_{eff} is the effect mobility of the charge carriers and $n(x, y)$ is the space dependent electron concentration. Integrating eq. (4.12) in y and z direction, we obtain the drain current flowing through the active area of the device as:

$$I_{ds}(x) = \mu_{eff} W_{fin} q_i(x) \frac{dV_F(x)}{dx} \tag{4.13}$$

where W_{fin} is the width of the FinFET device. Integrating eq. (4.13) within lengths 0 to L_{eff}, we obtain the drain current expression as:

$$I_d = \mu_{eff} \frac{W_{fin}}{L_{eff}} \int_0^{V_{ds}} q_i(x) dV_F(x) \tag{4.14}$$

Substituting the quantum inversion charge, $q_i(x)$ from eq. (4.1) into eq. (4.14), to obtain the drain current as:

$$I_D = \mu_{eff} \frac{W_{fin}}{L_{eff}} \int_0^{V_{ds}} \frac{qkT}{\pi\hbar^2} m_{2D}^{l,l} g_{l,l} \times \ln\left[1+\exp\left(-\beta\left(\widetilde{E}_{l,l}^{i} + \frac{E_g}{2} - \psi_s(x) + V_F(x)\right)\right)\right] dV_F(x) \tag{4.15}$$

$$I_D = ab \int_0^{V_{ds}} \ln\left[1+\exp\left(-\beta\left(\widetilde{E}_{l,l}^{i} + \frac{E_g}{2} - \psi_s(x) + V_F(x)\right)\right)\right] dV_F(x) \tag{4.16}$$

where: $a = \mu_{eff} \frac{W_{fin}}{L_{eff}}$, $b = \frac{qkT}{\pi\hbar^2} m_{2D}^{l,l} g_{l,l}$

Assuming $\exp\left(-\beta\left(\widetilde{E}_{l,l}^{i} + \frac{E_g}{2} - \psi_s(x) + V_F(x)\right)\right) << 1$ the drain current expression can be approximated as:

$$I_D = ab \int_0^{V_{ds}} \left(-\beta\left(\widetilde{E}_{l,l}^{i} + \frac{E_g}{2} - \psi_s(x) + V_F(x)\right)\right) dV_F(x) \tag{4.17}$$

After the integration and algebraic manipulation, the final expression for FinFET drain current under quantum mechanical scheme is obtained as:

$$I_D = -ab\beta\left[\left(\widetilde{E}_{l,t}^{i} + \frac{qE_g}{2} - \psi_s(x)\right)V_{ds} + \frac{V_{ds}^2}{2}\right] \tag{4.18}$$

4.5 Results and Discussion

An analytical modeling scheme taking into consideration various quantum mechanical effects has been presented for FinFET structure for a channel length of 30 nm, fin thickness of 20 nm and fin height of 30 nm. Results obtained through our analytical model are compared and contrasted with reported experimental results. The results have also been compared with simulation done on Synopsys TCAD tool Sentaurus.

Figure 4.1 shows the two-dimensional FinFET structure used for the purpose of Sentaurus simulations. This diagram depicts a view from the top of the device. The various regions have been marked on the figure such as gate, source, drain, Fin, Spacers and SiO_2. All the parameters used for the analysis are shown in Table 4.1.

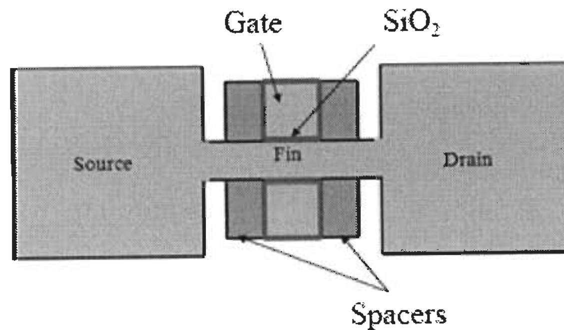


Figure 4.1 FinFET 2D Structure used in the Sentaurus simulations

Table 4.1 Value of Parameters

Parameters (in eq. 4.8, 4.9, 4.10)	Values [2]
a_1	6.6 e-8
a_2	1.82 e-8
a_3	3.27 e-16
n	1.62
γ	4.89

The variation of drain current with drain voltage for the above FinFET device is shown in Figure 4.2 for a gate to source voltage of 0.75 V. For the purpose of verification and validation of the results obtained through our analytical model, it has been compared and contrasted with reported experimental results [29] and our Sentaurus simulation results with devices of the same dimensions and parameters. It may be seen from the figure that the characteristics follow the same graph qualitatively as bulk MOS devices. It shows a linear, followed by non-linear and a saturated drain current. It may be further observed that the results obtained through our model matche to large extent with the reported experimental results. It may be noted that the match is better in the saturation region. This proves that our proposed model can work typically within V_{ds} range of 0.3 V on wards.

In the linear and non-linear region of the characteristics, a relatively close match is found between our model and reported experimental result. Whereas in the saturated region, our analytical and simulated results are relatively close as compared

to reported experimental result. This is because at lower gate voltage quantum mechanical phenomena are less dominant as compared to conventional device phenomena. But at higher gate voltage, it is due to electrical and structural confinement and quantum mechanical phenomena starts to play a major role. From the figure it can be inferred that there is a close match for all the three results, thus validating our analytical approach.

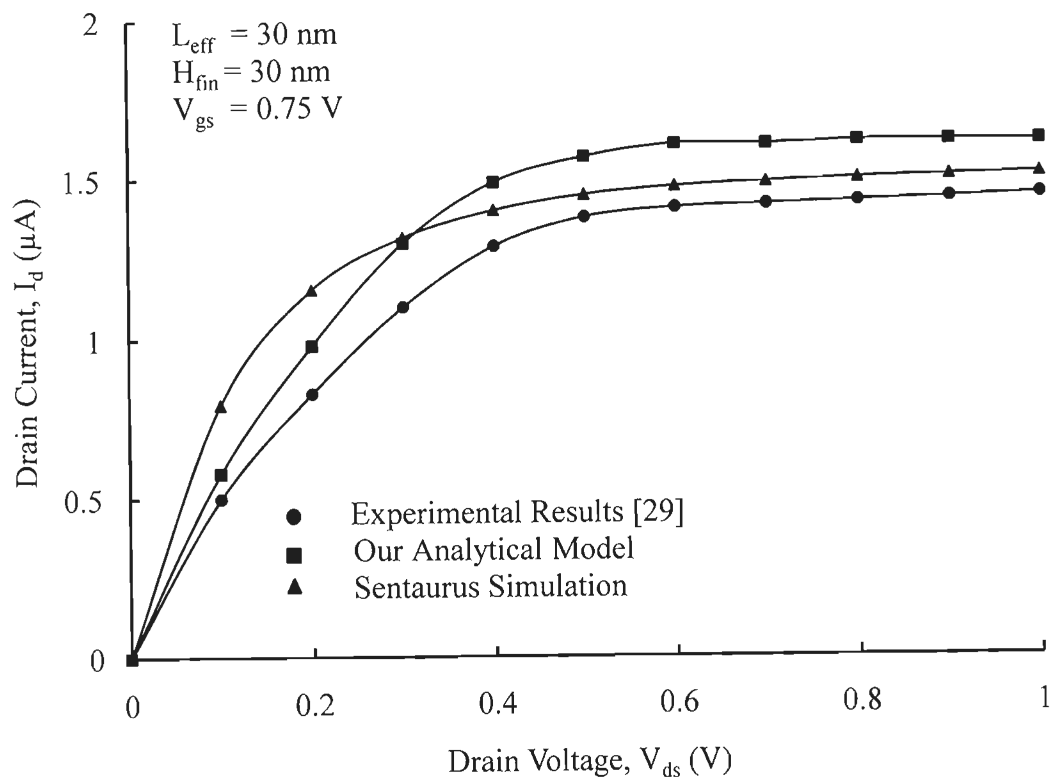


Figure 4.2. Variation of drain current with drain voltage according to our analytical quantum mechanical model, reported experimental results [29] and our Sentaurus simulation results.

Qualitatively our analytical model and experimental result match with each other to a large extent. The drain voltage at which saturation tendency of drain current is visible is larger for simulated result as compared to our analytical or reported

experimental results. This is primarily due to choosing a model for simulation which proposes a lower drain voltage for carrier quantization. Further the driving capability of the device seems to be higher for analytical proposed model which makes it better as compared to even experimentally demonstrated results.

For further validating our proposed quantum mechanical analytical model for the FinFET device under study, the results obtained have been compared and contrasted with reported experimental results [29] for the output characteristics for various gate voltages and this is shown as figure 4.3.

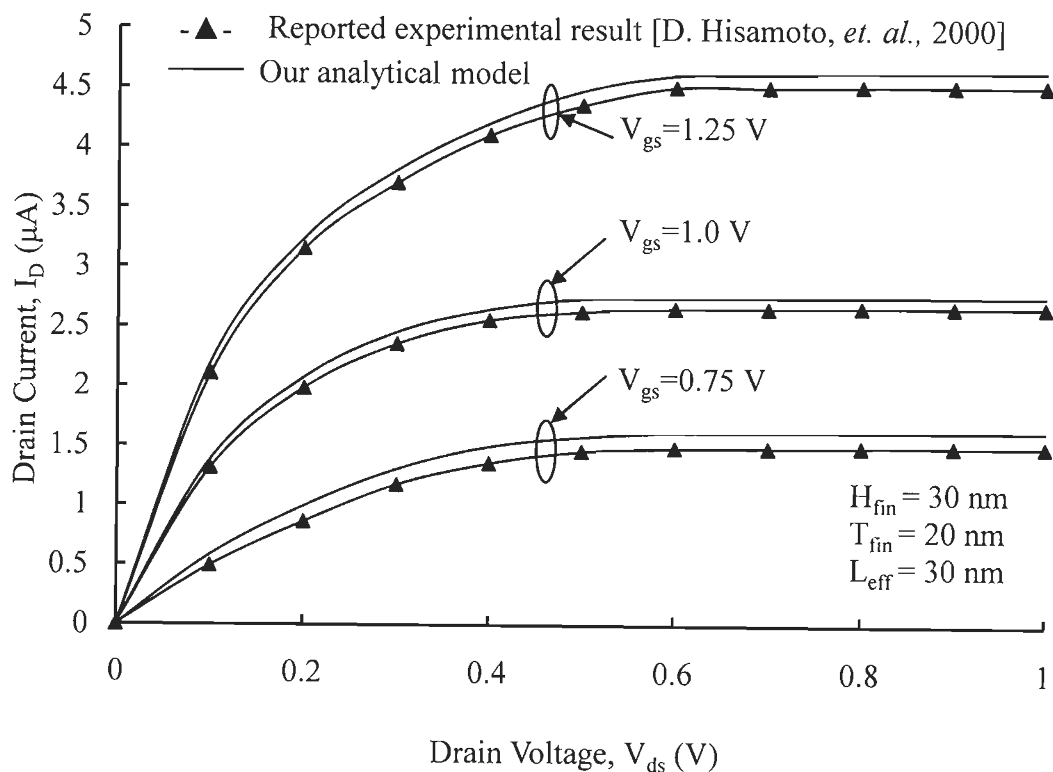


Figure 4.3 Variation of drain current with drain voltage obtained through our model and reported experimental results [29]

It can be seen from the figure that there is a close match between the two results at all values of drain and gate voltages, thereby validating our approach for the

drain current evaluation. Our analytical model slightly overestimates the drain current as compared to experimental result. The possible reason is that excess quantum confinement in transverse direction results in a relatively small degradation in electron mobility. Moreover as the gate voltage increases, there is an enhancement of carriers near the 'Fin' thereby increasing the current.

Figure 4.4 shows the variation of drain current with applied drain voltage for the FinFET structure under study for channel lengths of 30 nm, 40 nm, 50 nm and 60 nm respectively.

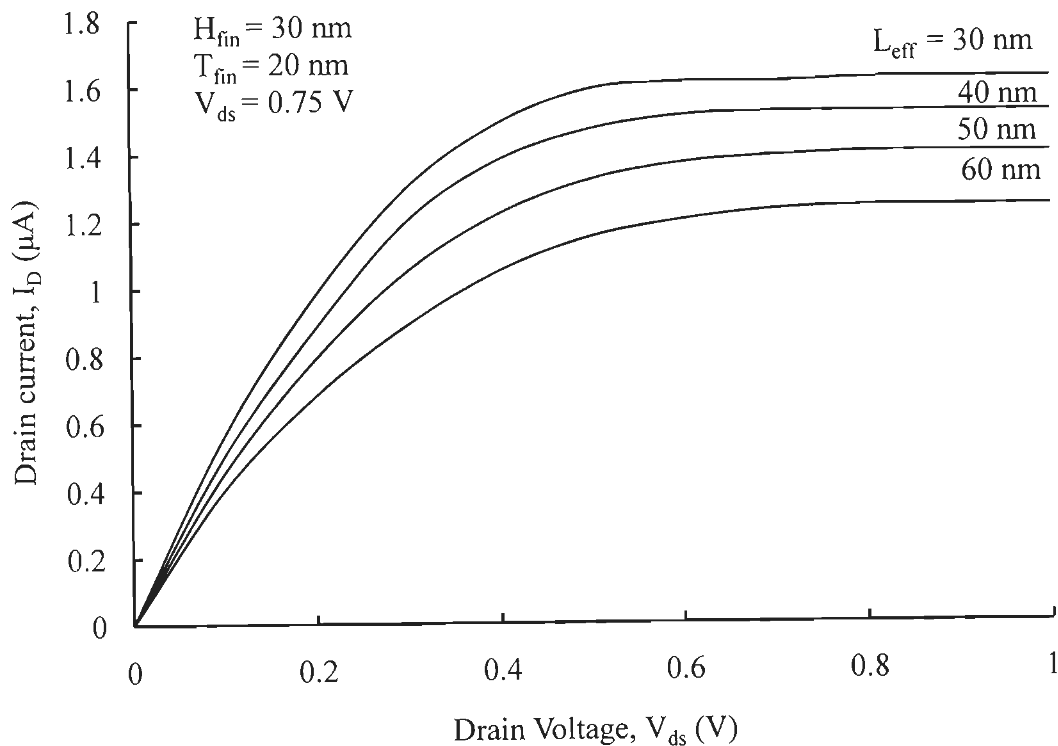


Figure 4.4 Variation of drain current with drain voltage for various effective gate lengths

It can be seen from the figure that for an applied drain to source voltage, the drain current corresponding to lower channel length is higher as compared to drain

current for the larger channel length. This can be attributed to the fact that as the channel length decreases, longitudinal electric field enhancement takes place which results in a larger current. Further in the linear region of operation, the drain current for lower channel length is lower as to higher channel length. With the lowering of channel length, the drain current increases which results in reduction in drain resistance. The variation of drain current with applied drain to source voltage for three different Fin thicknesses is shown in figure 4.5.

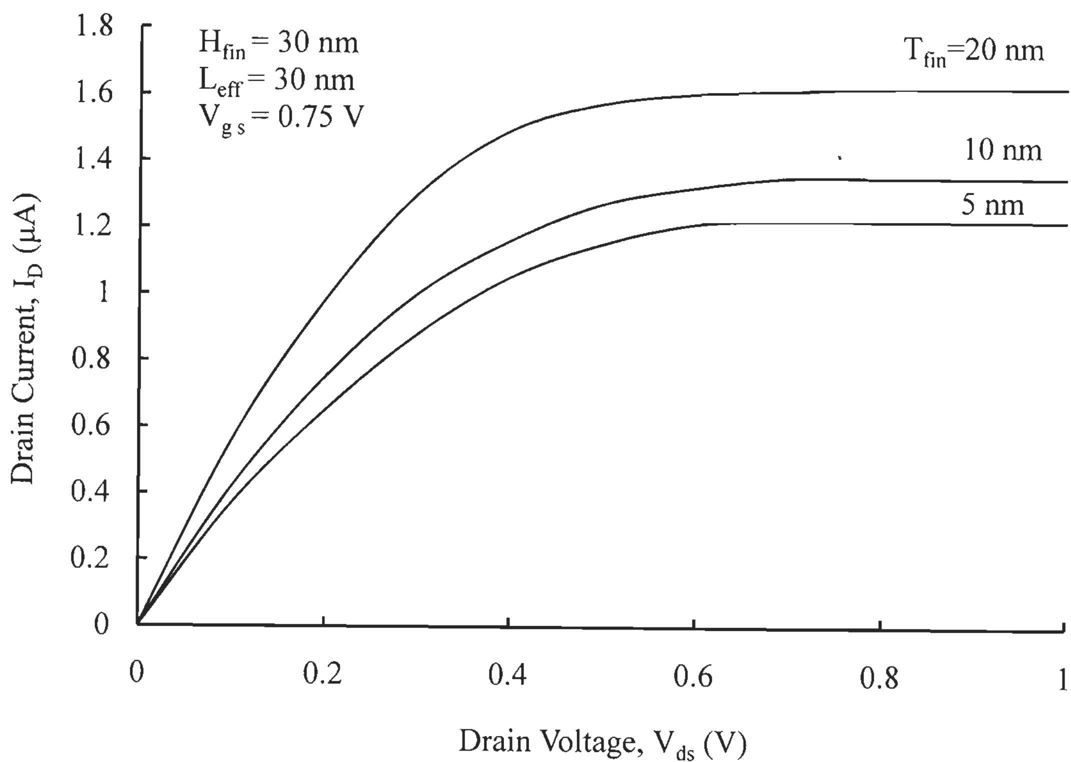


Figure 4.5 Variation of drain current with applied drain voltage for varying Fin thickness

It can be observed that for any applied drain to source voltage there is an increase in the driving capability of the device as the Fin thickness increases. This is due to the fact that as the Fin thickness increases, more of electrons are available for contributing towards inversion layer charge and hence the drain current shows an

increase. As the fin thickness increases, the effective area under the gate also increases and hence a large inversion charge can be accommodated which results in a large drain current. However, it may also be noted that the transverse electric field reduces as the Fin thickness increases. Therefore, the confinement of carriers is not substantially enhanced. Figure 4.6 shows the variation of drain current with the applied gate voltage for our proposed analytical model, reported experimental result and our simulated results. The gate length and fin height have been taken as 30 nm and fin thickness as 20 nm. The applied gate to source voltage is 1 V.

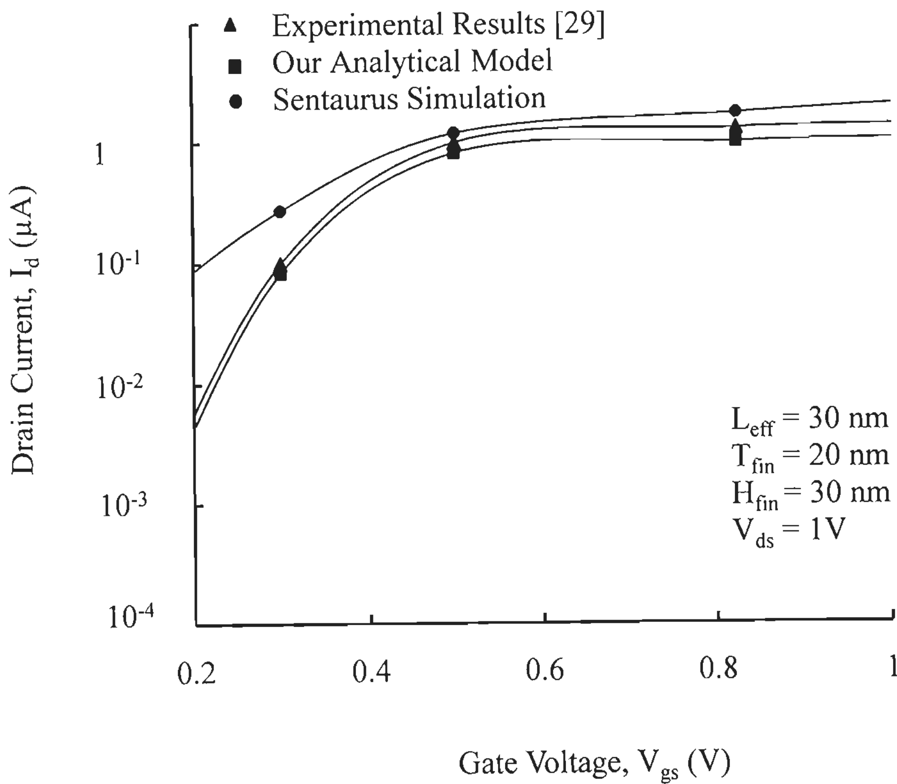


Figure 4.6. Variation of drain current with gate voltage for our analytical model, reported experimental results [29] and Sentaurus simulated results.

It can be seen from the figure that it is a close match between our result and experimental result [29] for all values of gate voltage. In the sub threshold region of

operation, the simulated result does not match with the reported experimental result or our model. This might be due to the fact that the drain current in the subthreshold region is primarily due to diffusion rather than drift, which might not be true for simulated results. It can be seen from the figure that there is abrupt increase in the drain current for a gate voltage range of 0.3 V to 0.5 V. The channel impurity concentration has been taken to be very low, which results in suppressed subthreshold leakage current. There is relatively close match between our results and reported experimental results, thus validating our approach.

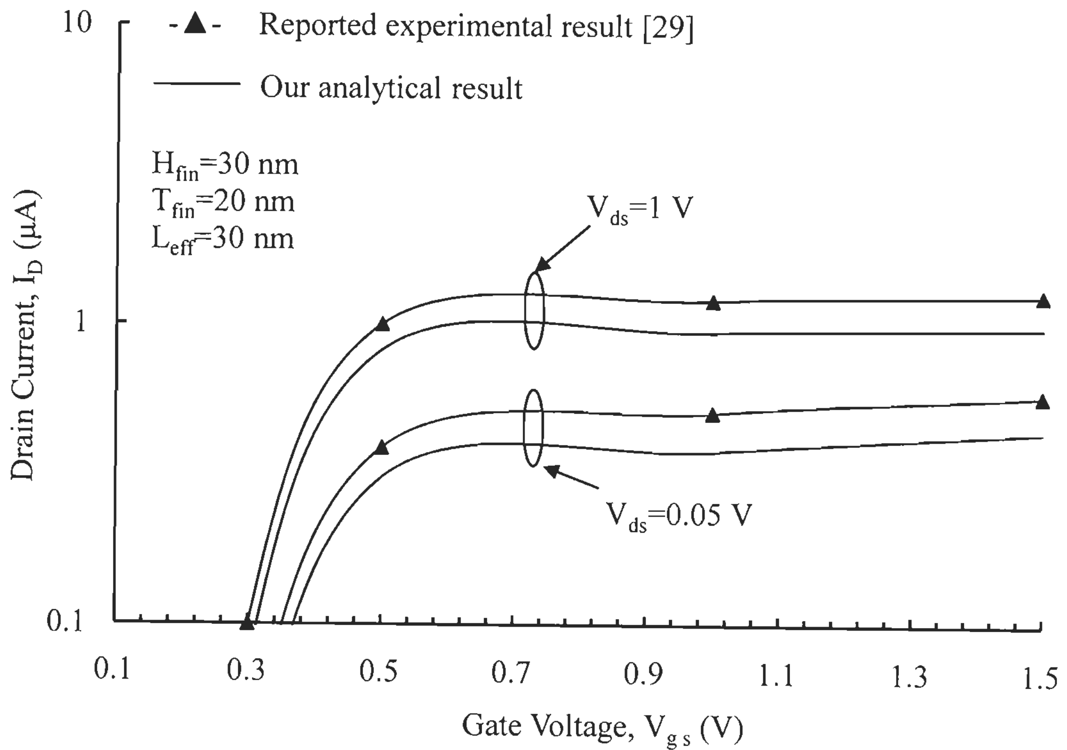


Figure 4.7. Variation of drain current with applied gate voltage for our model and reported experimental results [29]

For further validation of our model, variation of drain current with gate voltage for our quantum mechanical analytical model and reported experimental results [29] is shown in figure 4.7. As in the previous case, our model slightly

underestimates the drain current as compared to reported experimental result for higher applied gate voltage. Moreover, the trans-conductance as evaluated from our model is lower as compared to that of experimental results.

Figure 4.8 shows the variation of drain current with applied gate voltage for the FinFET structure for varying channel length. It can be seen from the figure that for an applied gate voltage, the drain current corresponding to lower channel length is higher as compared to drain current for the larger channel length.

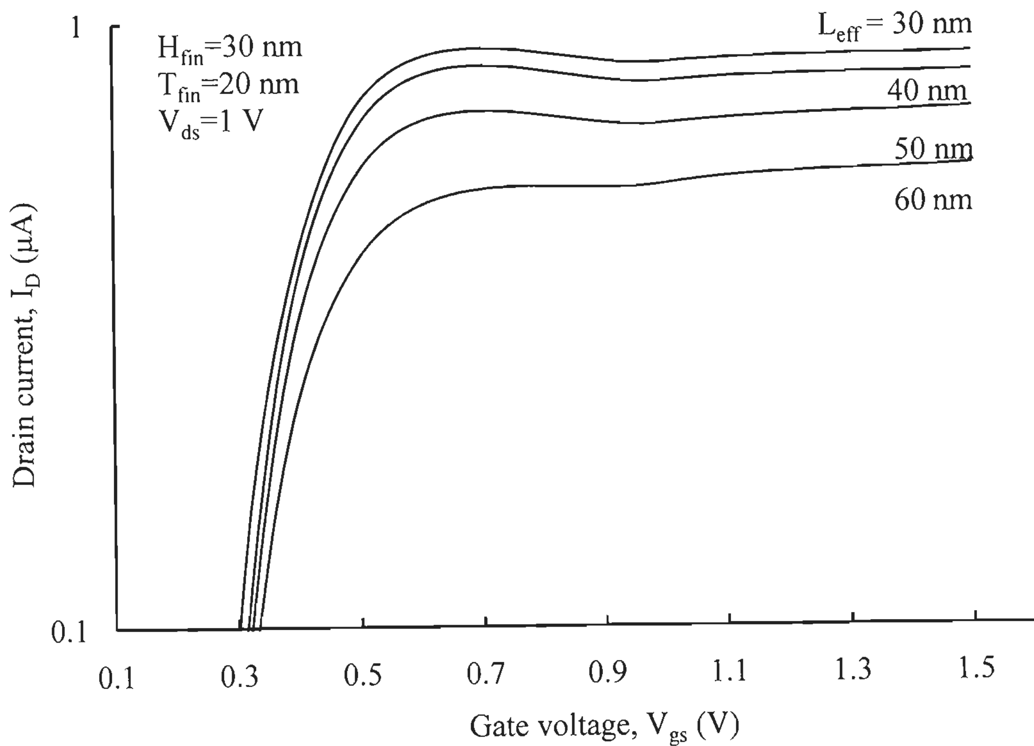


Figure 4.8 Variation of drain current with applied gate voltage for various effective gate lengths

Moreover, for lower channel lengths (30 nm and 40 nm), there is a kink in the drain current for an applied gate voltage of 0.6 V. From the figure it can be inferred that in the subthreshold operation, drain current drastically reduces with the reduction

in gate voltage as is true for bulk MOSFET as well. As the effective length reduces, the drain current also increases.

Figure 4.9 shows the variation of drain current with applied gate voltage for three different fin thicknesses. It can be observed that for any applied gate voltage, as the fin thickness increases, there is an increase in the drain current of the device. This is because device with larger fin thickness would be able to accommodate larger inversion layer charge and hence a large drain current.

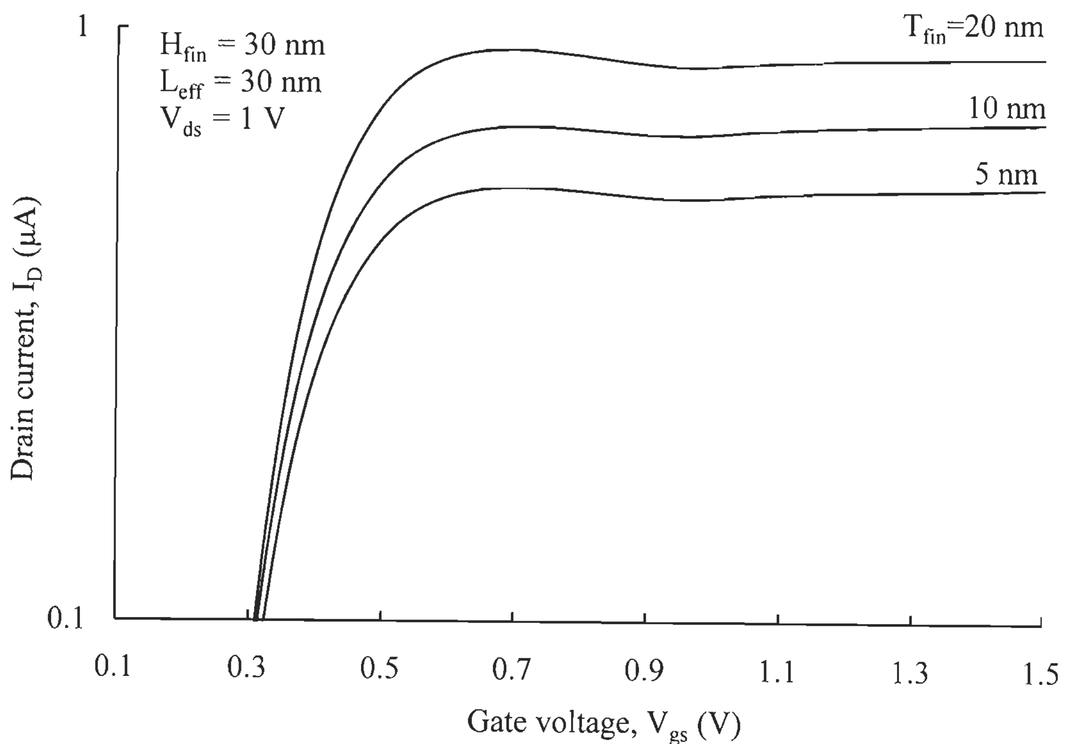


Figure 4.9 Variation of drain current with gate voltage for fin thickness of 5 nm and 20 nm for the comparison between classical and quantum model

The variation of drain current with applied drain voltage for our analytical model and our simulated result for two gate lengths namely 30 nm and 50 nm is shown in figure 4.10. The Fin Thickness and Fin height have been taken to be 20 nm

and 30 nm, respectively. The applied gate voltage is kept to be 0.75 V. It can be seen from the figure that the results are comparatively matched in the saturation region as compared to the linear region. This is due to the reason that at lower drain voltage, the longitudinal electric field from source to drain is typically low which results in a larger mobility of the charge carriers resulting in larger drain current for simulated results as compared to our proposed analytical model.

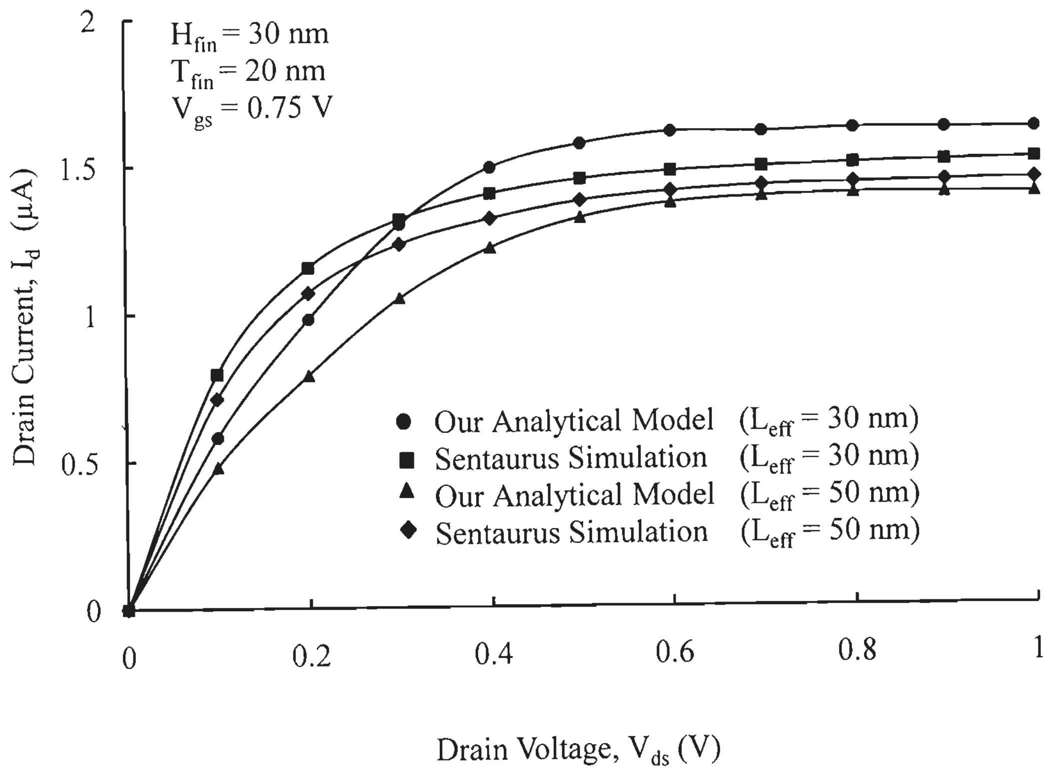


Figure 4.10. Comparison of our analytical quantum mechanical model with Sentaurus simulation results for I_d-V_{ds} characteristics for gate lengths of 30 nm and 50 nm.

It is further observed that in the saturation region, the matching of the drain current for any applied drain voltage is better for larger channel length as compared to a shorter channel length. This is primarily due to the fact that a larger channel length incorporates larger S/D resistance which results in the reduction in the saturation drain current. Further, the drain current cited with larger channel length is lower as

compared to shorter channel length because for everything rest being equal, a shorter channel length would result in a larger longitudinal electric field which would enhance the current. Figure 4.11 shows the variation of drain current with the applied drain voltage for our proposed analytical model and our simulated results for two fin thickness as namely 5 nm and 20 nm. The gate length has been taken to be 30 nm and fin height as 30nm. The applied gate to source voltage is 0.75 V.

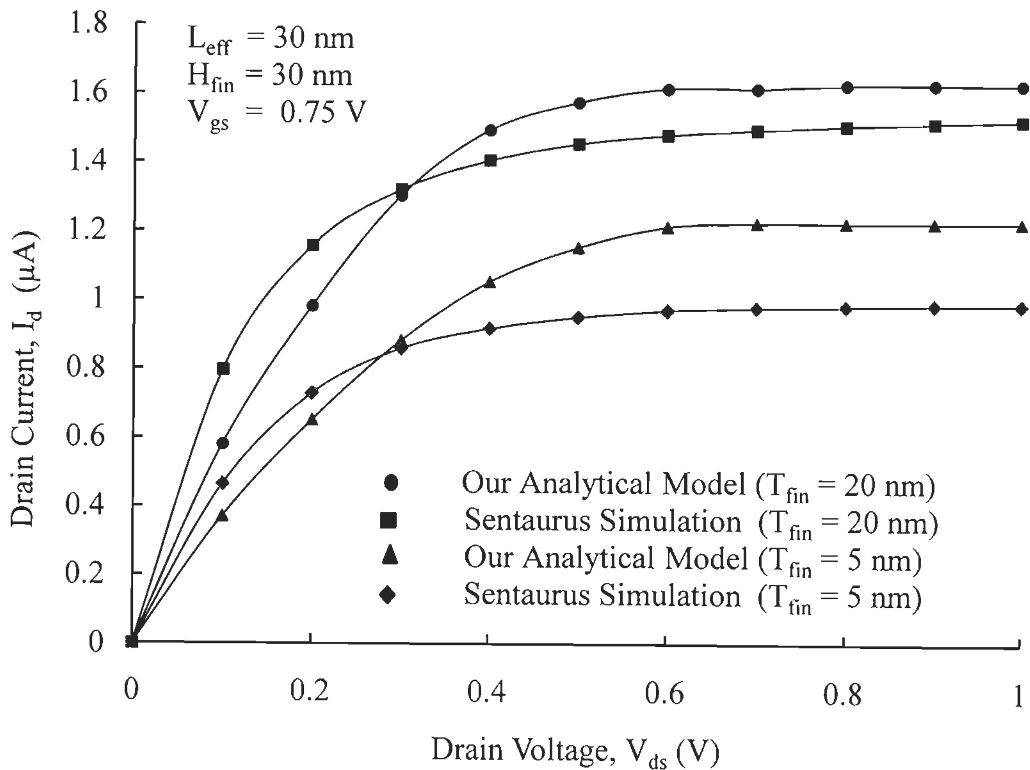


Figure 4.11. Variation of drain current with drain voltage and comparison for our analytical quantum mechanical model and Sentaurus simulation results for T_{fin} of 20 nm and 5 nm.

It can be observed from the figure that in the linear region of operation, there is a close match for a lower fin thickness, whereas the match is better for higher fin thickness in saturation region. At lower fin thickness, since the cross-sectional area of channel reduces, this results in a larger resistance being offered. This results in a

lower drain current. Further, the energy quantization of free charge carriers at lower fin thickness is more stringent as compared to higher fin thickness. This results due to the fact that the first valley and the sub-band are fully populated and hence a relatively close match is seen between our proposed model and our simulated result in the linear and non-linear region of operation. In the saturation region, the match is close in case of higher fin thickness.

Figure 4.12 shows the variation of drain current with the applied gate voltage for a fixed drain to source voltage of 0.05 V and for three channel lengths simulated results. The fin thickness and height have been taken to be 20 nm and 30 nm respectively. It can be seen from the figure, as the gate length reduces, there is slight increase in drain current for same applied drain voltage.

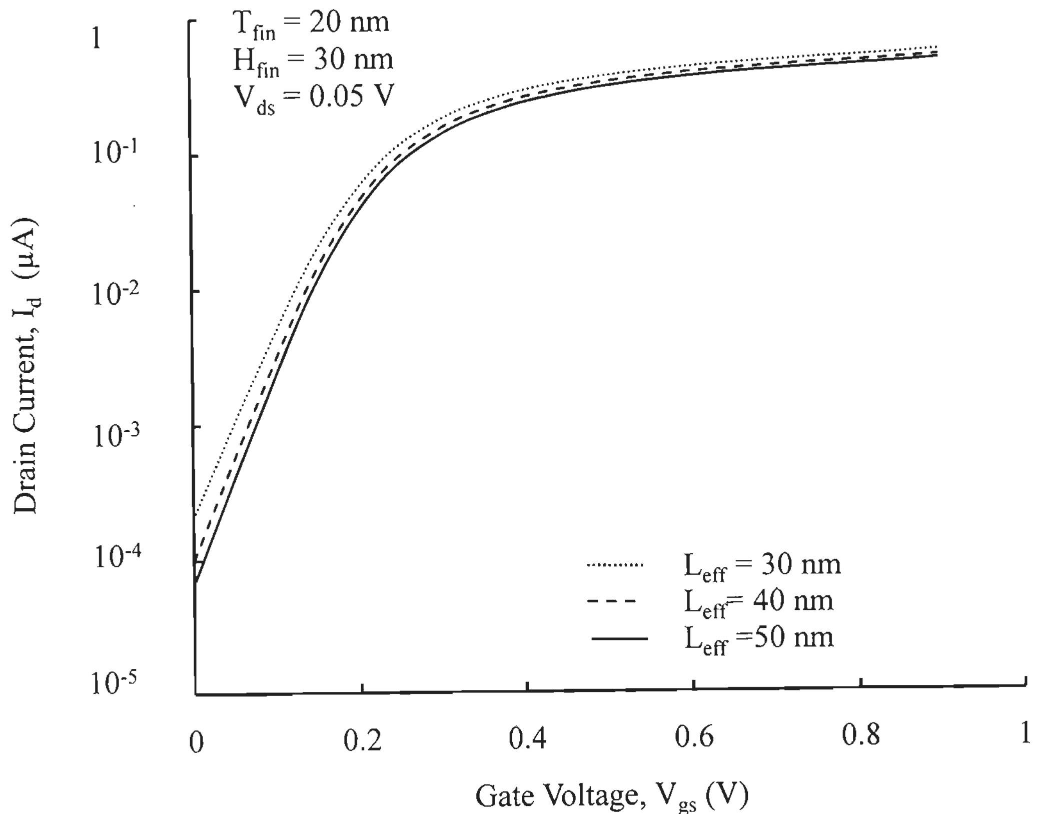


Figure 4.12 Variation of drain current with applied gate voltage for varying channel length of 30 nm, 40 nm and 50 nm using Sentaurus.

The variation of drain current with applied gate voltage for three fin thicknesses is shown in figure 4.13 for our simulated results. The gate length and fin height have been taken to be 30 nm and drain to source voltage is 0.05 V.

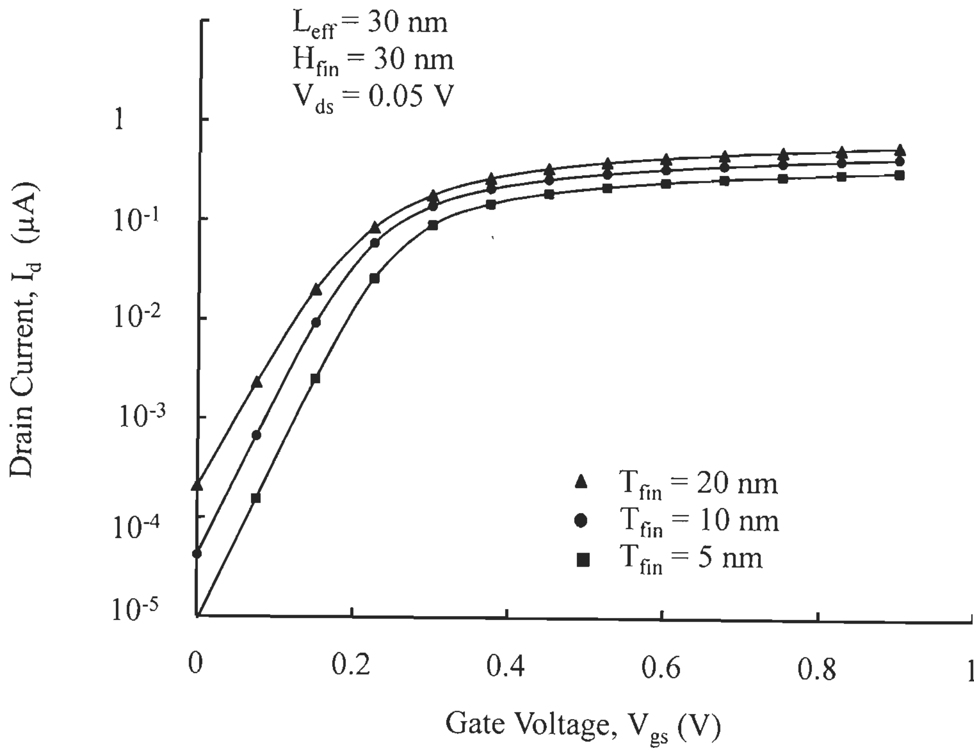


Figure 4.13. Variation of drain current with applied gate voltage for Fin thicknesses of 5 nm, 10 nm and 20 nm using Sentaurus.

It can be observed from the figure that as the fin thickness increases, there is an increase in the drain current for a fixed gate voltage. This is due to the fact that as the fin thickness increases, there is a decrease in the total resistance of the channel, resulting in a lower drain current. Further as the fin thickness increases, the sub threshold slope also tends to increase. This is due to the fact that with larger fin thicknesses, large numbers of carriers have to be depleted in order to achieve a one decade drop in the drain current as the overall area under the gate actually increases.

4.6 Conclusion

In this chapter, an extensive quantum mechanical analytical modelling has been carried out to evaluate quantum inversion charge, effective mobility and the drain current of FinFET structure with varying device dimensions. Analytical modelling of FinFET structure has been carried out in this chapter to evaluate the various characteristics using extensive quantum mechanical simulations. For the purpose of validation, the results obtained on the basis of our model have been compared and contrasted with reported experimental and simulated results. A relatively good match has been found This validates our approach for modelling FinFETs. For the driving capability of the device, we have presented the output characteristics for our proposed device for effective mobility.

Chapter 5

Modeling of Subthreshold Leakage Current, Subthreshold Swing Factor and Gate Leakage Currents for DG FinFET Device

5.1 Introduction

High subthreshold leakage current and gate leakage current makes down scaling of bulk MOSFET technology inevitable. Double gate devices such as FinFET reduce Short Channel Effects (SCE's) and leakage current. Further fabrication of FinFET devices using conventional bulk technology is also possible. Therefore, without excessive change in fab-line, new technology can be easily adapted for better performance and scalability [33, 99].

Under high frequency operation, temperature rises due to large active power consumption. The high temperature, increases the sub-threshold leakage (which is strong function of temperature). If heat cannot be dissipated effectively, a positive feedback between leakage power and temperature can result in thermal runaway [82]. To predict thermal runaway, it is important to account for all the components of power dissipation self-consistently with respect to temperature. Many research works have been conducted to estimate leakage current under process variation [52, 83, 131]. In previous works, however, the temperature dependence of leakage current was not considered and the impact of dynamic power on leakage and temperature was not appropriately accounted for. CMOS with gate length of 50–70 nm needs an oxide thickness of around 1.5–2.0 nm, which corresponds to 2–3 layers of silicon atoms [10, 33, 34, 61, 100, 101]. With such a thin oxide, direct tunneling occurs resulting in an exponentially increasing gate leakage current. This gate leakage current increases

power dissipation and deteriorates device performance and circuit stability [145, 176, 179]. The key feature of multi-gate FinFET is strong gate control of the channel region suppressing effectively the short-channel effects and leakage current.

Moreover, the role of Quantum-Mechanical (QM) effects becomes more important in these devices with an ultra-thin gate dielectric and Si body. One of such QM effects which has been recently predicted for ultra-thin body single-gate (SG) and double-gate (DG) FinFET is the reduced gate tunneling currents compared to planar bulk-Si devices due to the reduced transverse electric field and less quantum carrier confinement [96, 101, 153]. The above gate current reduction was predicted to be enhanced for the increased physical dielectric thickness and hence for higher-k dielectrics [149, 179]. This is a promising finding since it may relax the restrictions on the gate oxide thickness scaling. The biggest contributor to leakage currents is the subthreshold leakage current. Due to the lowering of the threshold voltage with the evolution to ultra-deep submicron technologies, this leakage current has increased. The dependency of the subthreshold current on bias and drain induced barrier lowering (DIBL) has been clearly demonstrated. The other small channel effects can be taken into account by the FinFET width W_{fin} and length L_{eff}.

In this chapter, we investigate the combined effect of process variation and die temperature on leakage current for FinFET devices. The analytical modeling of subthreshold leakage current, subthreshold swing and gate leakage current have been carried out in this work. The effect of the process variation on various leakage currents and subthreshold swing factor in FinFET device has been analytically formulated in this work. These variations cause a large spread in leakage power, since it is extremely sensitive to process variations, which in turn results in larger temperature variations across different dies. Due to large temperature variation within

the die, we have also investigated the variation of various leakage currents with absolute die temperature. The analytical modeling of subthreshold leakage current, subthreshold swing, gate leakage current and its variation with process parameters have been carried out in this chapter. The results obtained on the basis of our model have been compared and contrasted with reported numerical and experimental results. A close match was found which validate our analytical approach.

The organization of this chapter is as below: introduction about the different leakage currents in FinFET device have been given in section 5.1. Section 5.2 deals with the subthreshold swing modeling. In section 5.3, the subthreshold leakage current modeling has been carried out. Section 5.4 describes the gate leakage current modeling. Results and discussion have been given in section 5.5. The conclusion has been provided in section 5.6

5.2 Subthreshold Swing Modeling

A commonly used parameter in characterizing leakage behavior is the subthreshold swing (also called subthreshold slope). The subthreshold swing (S) is the amount of variation required in gate-to-source voltage (V_{gs}) in order to vary the weak inversion current by one decade [66, 72, 91, 179]. Two key characteristics of a DG FinFET that are particularly important to digital applications are threshold voltage (V_{th}) and subthreshold swing. As the effective channel length (L_{eff}) of a DG FinFET is reduced, threshold voltage (V_{th}) typically decreases and subthreshold swing *(S)* increases. These are commonly known as short-channel effects (SCE). Consequently, the ratio of the drive current to the leakage current is reduced, which results in

significantly increased stand-by power. The analytically evaluated subthreshold swing factor is given by [126]:

$$S = \left[1 - 2\Gamma_1 \cos\left(\frac{T_{fin}}{4\lambda_1}\right)\exp\left(-\frac{L_g}{2\lambda_1}\right)\right]^{-1} \frac{kT}{q}\ln 10 \qquad (5.1)$$

where k is Boltzmann constant, T is the temperature, q is the electron charge, L_g is physical gate length and the parameter λ_1 is determined by the vertical dimensions

$$\lambda_1 = \frac{1 + 1/r}{1 + \pi/2} T_{fin} \qquad (5.2)$$

where $r = \varepsilon_{ox} T_{fin} / \varepsilon_{si} t_{ox}$, t_{ox} is the gate oxide thickness, and ε_{ox} and ε_{Si} are the permittivity's of the gate oxide and silicon, respectively. The parameter Γ_1 is given as [126].

$$\Gamma_1 = \frac{2\lambda_1}{T_{fin}}\sqrt{1 + \frac{T_{fin}^2}{r^2\lambda_1^2}} \Bigg/ \left(\frac{1}{r} + \frac{1}{2} + \frac{1}{2}\frac{T_{fin}^2}{r^2\lambda_1^2}\right) \qquad (5.3)$$

We define a new term subthreshold swing factor (S_f) as the ratio of subthreshold swing of device to that of ideal value of subthreshold swing (60 mV/dec).

5.3 Subthreshold Leakage Current Modeling

In the weak inversion mode, current conduction between the source and drain (the subthreshold leakage current) is primarily due to diffusion of the carriers [148, 149, 179]. Figure 5.1 shows the subthreshold and gate leakage currents. Subthreshold leakage current (I_{sub}) is a sensitive function of effective gate length and fin width. As the channel length increases, I_{sub} decreases because longer channel reduces DIBL and SCE [149, 179]. On the contrary, I_{sub} increases with larger fin width (W_{fin}). It is because thinner body allows gates to gain a better control over the channel, thus

reducing SCE. Hence, while modeling sub-threshold leakage, careful attention should be given to the combined effect of temperature as well as device parameters such as effective gate length and fin width.

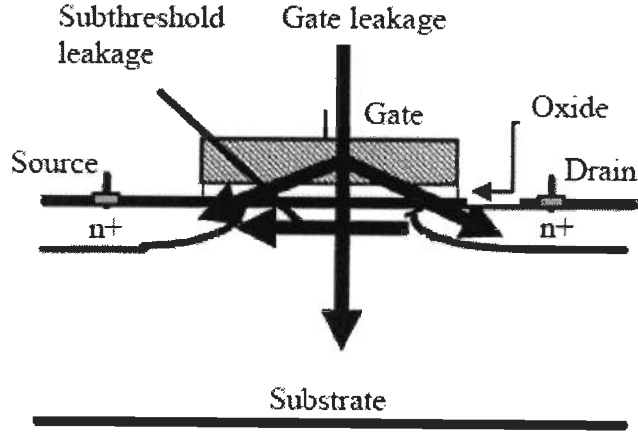


Figure 5.1 Subthreshold and Gate Leakage Currents [4]

An empirical relationship was developed through curve fitting to estimate subthreshold leakage current variation with temperature. Sub-threshold leakage current (I_{sub}) in double-gate FinFET devices is expressed as [83]

$$I_{sub} = 2\frac{W_{fin}}{L_g}C_{ox}\mu_{eff}\left(\frac{kT}{q}\right)^2 e^{\left(\frac{-qV_{th}}{SkT}\right)} \quad (5.4)$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the effective oxide capacitance per unit area, μ_{eff} is electric field dependent effective mobility, k is the Boltzmann constant, T is the absolute temperature, q is the electron charge, V_{th} is the threshold voltage of the device and S is the sub-threshold swing factor. Note that the temperature dependence of I_{sub} is dominated by the exponential term and that I_{sub} has exponential dependence on threshold voltage V_{th}.

5.4 Gate Leakage Current Modeling

Gate insulator leakage current (direct tunneling current) increases with the down-scaling of the gate oxide thickness (t_{ox}). The scaling of the gate oxide thickness is crucial to enhance the performance of MOS devices. Reducing the thickness of the gate oxide increases the oxide capacitance per unit area, thereby enhancing the drain current of MOS devices [75, 145, 149, 159, 179,]. Figure 5.2 shows the gate leakage current in double gate finFET device.

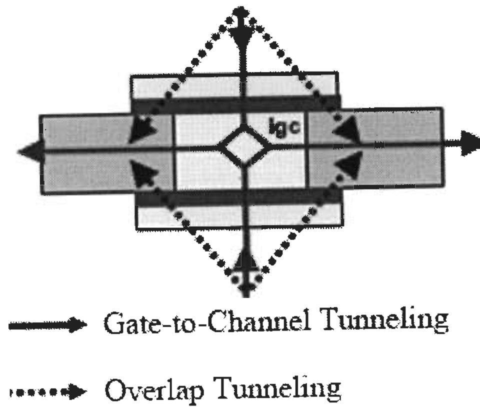


Figure 5.2 Gate Leakage Current in Double Gate FinFET Device [145]

Continued reduction of t_{ox} makes accurate modeling of gate tunneling current an important aspect of compact FinFET device. As the minimum gate length of FinFET is scaled into sub-50-nm range, substantial gate leakage current has been observed experimentally [164]. The tunneling current density at any point x within the channel is given by [165]:

$$J_g(x) \cong J_0 D(x) F_s(x) \tag{5.5}$$

where $J_0 = \frac{qm^* k^2 T^2}{2\pi^2 \hbar^3}$ (5.6)

where m^* is the effective electron mass, k is Boltzmann constant, T is absolute temperature, $D(x)$ and $F_s(x)$ are transmission probability and supply function respectively. An analytical expression for $D(x)$ is given as [165]:

$$D(x) = \exp\left[-B_0 f\left(z_g\right)\right] \quad (5.7)$$

where $B_0 = \frac{4t_{ox}\sqrt{m_{ox} q\Phi_B}}{3\hbar}$

$f(z_g) = \frac{1-(1-z_g)^{3/2}}{z_g}$ and $z_g = \frac{V_{ox}}{\Phi_B}$

After substituting the value of B_0 and $f(z_g)$ in eq. (5.7), we obtained the expression for $D(x)$ as:

$$D(x) = \exp\left[-\frac{4t_{ox}\sqrt{m_{ox} q\Phi_B}}{3\hbar} \times \frac{1-(1-z_g)^{3/2}}{z_g}\right] \quad (5.8)$$

where m_{ox} is the electron effective mass in SiO_2 in the tunneling direction, $q\Phi_B$ is the conduction band offset at the Si/SiO_2 interface and $V_{ox} = V_g - V_{fb} - \psi_s(x)$. V_g is the gate voltage, V_{fb} is the flat band voltage and $\psi_s(x)$ is the surface potential at point 'x'. The supply function ($F_s(x)$) in eq (5.5) is given by [165]:

$$F_s(x) = \log\left\{\frac{1+\exp\left[\frac{\psi_s - \varphi_n - \alpha_b - \psi_t}{\phi_t}\right]}{1+\exp\left[\frac{\psi_s - V_{gb} - \alpha_b - \psi_t}{\phi_t}\right]}\right\} \quad (5.9)$$

where φ_n is the channel voltage at point x. $\psi_t = 0$ for $V_{ox} \geq 0$ and $\psi_t = -(V_{ox} - G_0\phi_t)$ for $V_{ox} < 0$, where G_0 is an adjustable parameter. ψ_t (V_{ox}) dependence we set as [165]:

$$\psi_t = \frac{1}{2}\left[\sqrt{(V_{ox}+G_0\phi_t)^2+0.01}-(V_{ox}+G_0\phi_t)\right] \tag{5.10}$$

Substituting the value of J_0 from eq. (5.6), $D(x)$ from eq. (5.8), and $F_s(x)$ from eq. (5.9) in eq. (5.5), we obtain the final expression for the tunneling current density, $J_g(x)$ as:

$$J_g(x) = \left(\frac{qm^* k_B^2 T^2}{2\pi^2\hbar^3}\right) \times \left(\exp\left[-\frac{4t_{ox}\sqrt{m_{ox}q\Phi_B}}{3\hbar} \times \frac{1-(1-z_g)^{3/2}}{z_g}\right]\right) \times \left(\log\left\{\frac{1+\exp\left[\frac{\psi_s-\varphi_n-\alpha_b-\psi_t}{\phi_t}\right]}{1+\exp\left[\frac{\psi_s-V_{gb}-\alpha_b-\psi_t}{\phi_t}\right]}\right\}\right) \tag{5.11}$$

Table 5.1 Values of Parameters

Parameters	Values
L_{eff}	28 nm [82]
H_{fin}	35 nm [82]
T_{fin}	7 nm [82]
t_{ox}	1.2 nm [82]
G_0	7.891 [165]

5.5 Results and Discussion

In this chapter, the analytical modeling for subthreshold leakage current and gate leakage current in the Double Gate FinFET device has been carried out. For the purpose of validity of our approach, we have compared our results with the reported numerical results. A close match was found which validate our analytical modeling approach for leakage current estimation in double gate FinFET device.

Figure 5.3 shows the variation of subthreshold leakage current (I_{sub}) with variation of temperature for our proposed model and reported numerical result [83]. The design parameter used are L_{eff} = 28 nm, H_{fin} = 35 nm, T_{fin} = 7 nm and t_{ox} = 1.2 nm. It can be seen from the figure that there is a close match between our proposed model and reported numerical model. It is known that subthreshold current and gate leakage current vary with temperature but subthreshold leakage current variation is more sensitive to temperature variation.

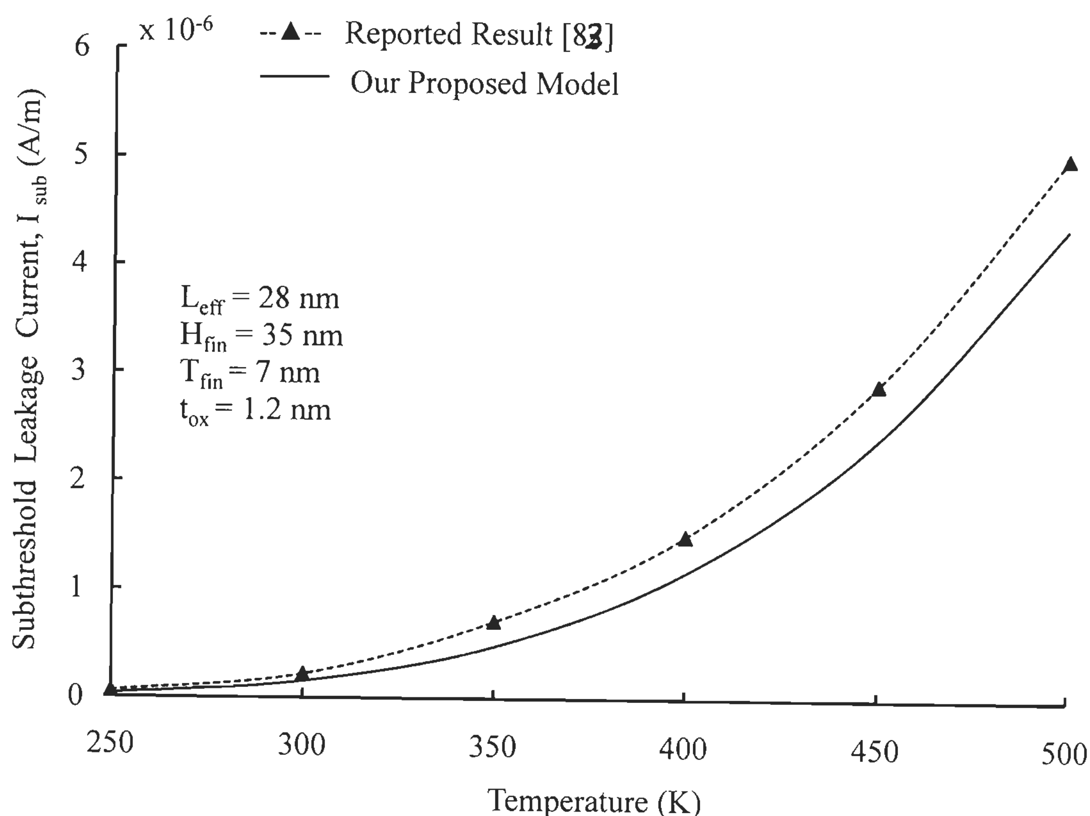


Figure 5.3 Variation of subthreshold leakage current (I_{sub}) with variation ofabsolute temperature for our proposed model and reported result [83].

It can be seen from the figure that subthreshold leakage current increases with an increase in temperature. The major portion of leakage current component is

through diffusion current which is primarily composed of minority carriers, whose concentration increases with an increase in the temperature. Because of high temperature sensitivity, subthreshold leakage current is a major component of the total static power consumption at high temperatures. Figure 5.4 shows the variation of direct tunneling current density with the applied gate voltage for three different values of fin thicknesses. The results have been compared and contrasted with reported numerical result [145]. A close match is found for fin thickness of 5 nm between our model and reported numerical results.

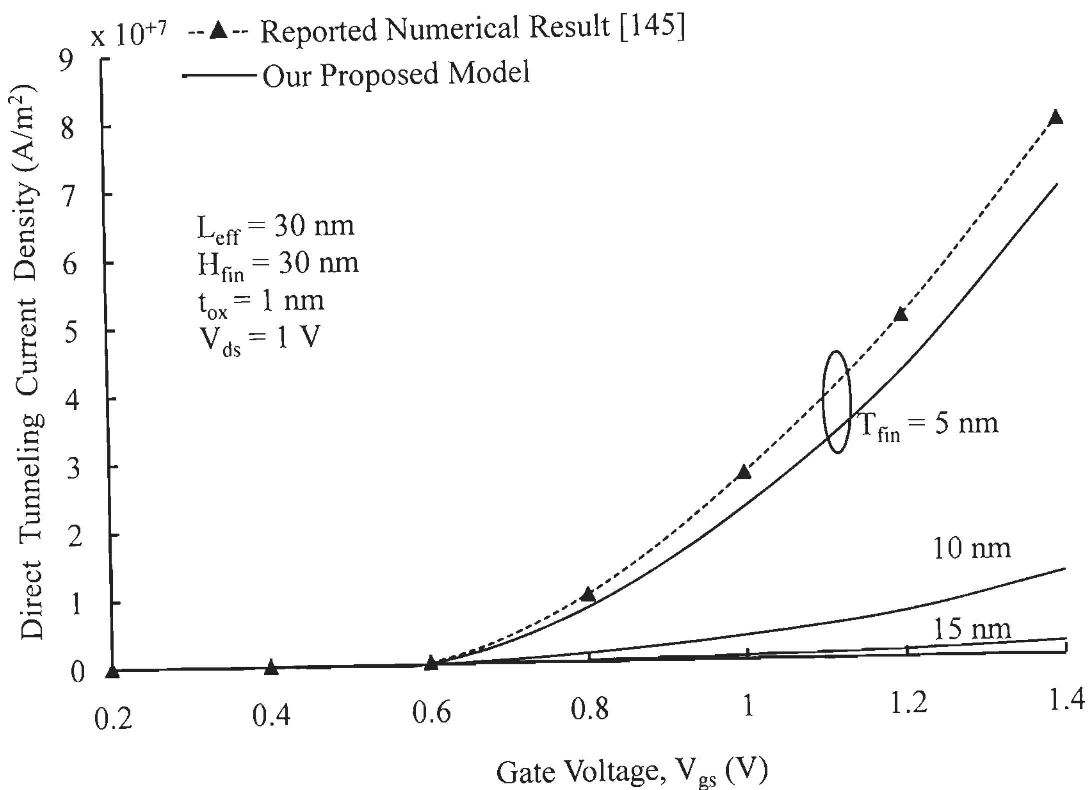


Figure 5.4 Variation of direct tunneling current density with gate voltage for Fin thickness (T_{fin}) of 5 nm, 10 nm, and 15 nm.

The direct tunneling current is obtained from first sub-band of first valley of the potential well within the active area of device. It is seen from the figure that the

direct tunneling density is reduced to very negligible value for gate voltage of 0.6 V and below. This is due to the fact that the transverse direction electric field reduces drastically as the gate voltage is below 0.6 V. It is further observed that as the fin thickness increases, there is a decrease in the direct tunneling current density. This can be attributed to lower value of quantum confinement in the transverse direction with increasing fin thickness. The proposed analytical model is verified with reported numerical results [145] for the purpose of validation and verification and is shown in figure 5.5. The variation of direct tunneling current density with the applied gate voltage for various oxide layers thickness and its comparison with reported numerical results is shown in figure 5.5.

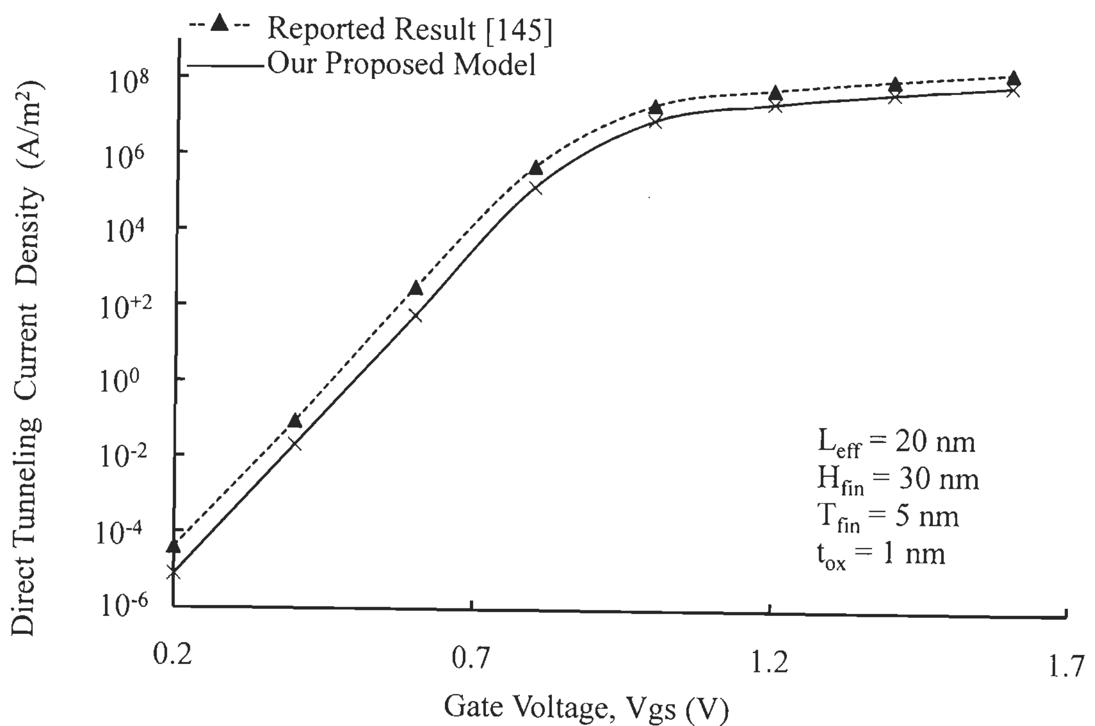


Figure 5.5 Variation of direct tunneling current density with gate voltage for our proposed model and reported result [145].

It can be seen from the figure that there is a close match between our proposed model and reported numerical model [145]. As the gate voltage increases, the direct

tunneling density increases initially in linear fashion followed by non-linear behavior and finally, it saturates. This is because of the fact that as the gate voltage increases, transverse electric field also increases, thereby increasing the probability of direct tunneling current. Figure 5.6 shows the variation of subthreshold leakage current with absolute temperature for four effective channel lengths. It can be seen from the figure that for same temperature, as the channel length increases, there is decrease in subthreshold leakage current.

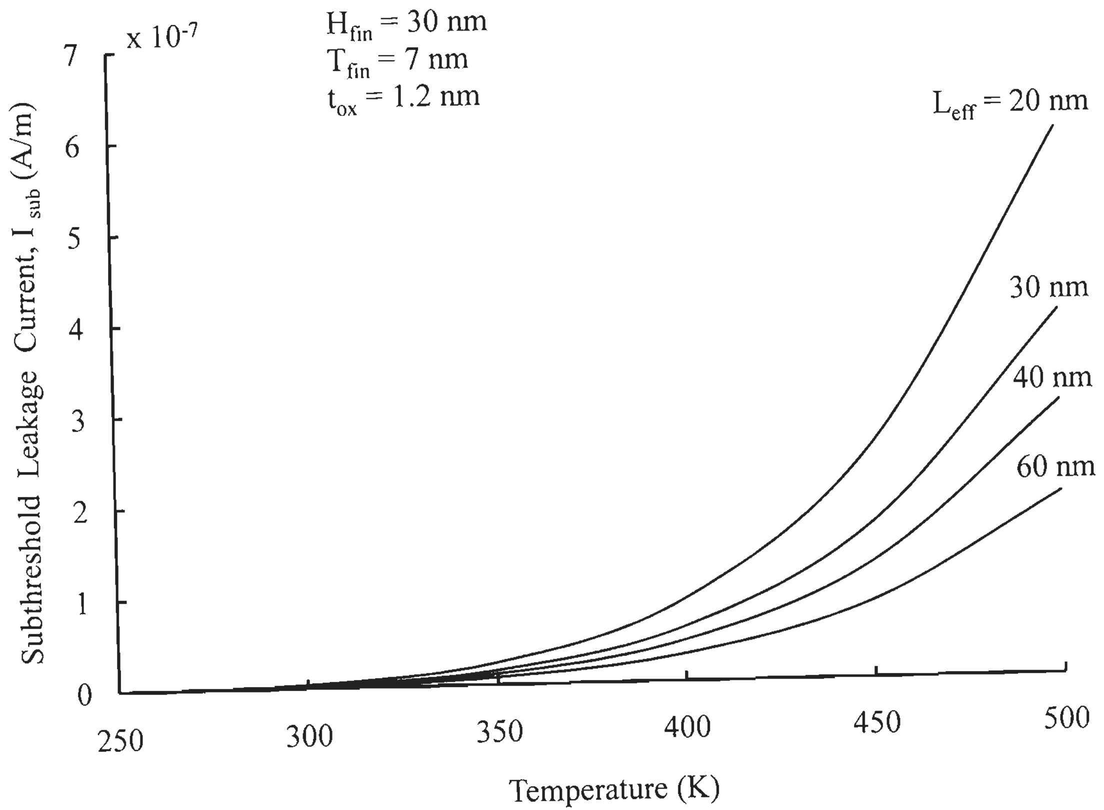


Figure 5.6 Variation of subthreshold leakage current (I_{sub}) with variation of absolute temperature for channel length of 20 nm, 30 nm, 40 nm and 60 nm.

Since subthreshold currents are essential drift currents, therefore, as channel length increases, the longitudinal direction electric field decreases, thereby,

decreasing the drift velocity of the of the carriers and hence the decrease in the current. At 450 K, there is a decrease of 2 x 10^{-7} A/m for a decrease in effective channel length (L_{eff}) of 40 nm. Further, the sensitivity of subthreshold leakage current for a shorter channel length is more as compared to longer channel. So for the purpose of optimizing subthreshold leakage current, it is necessary to operate at higher effective channel length.

Variation of subthreshold leakage current with the absolute temperature for various fin height is shown in figure 5.7. For any fin height, as the absolute temperature increases, there is an increase in the subthreshold leakage current.

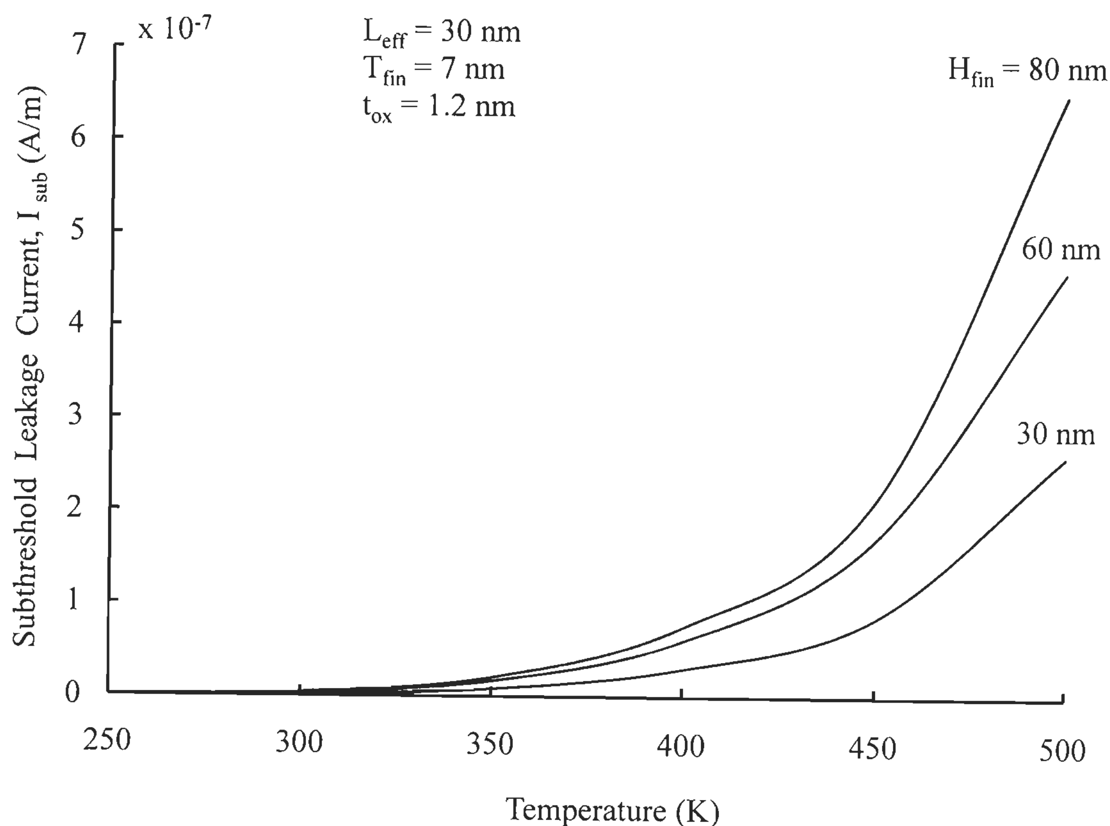


Figure 5.7 Variation of subthreshold leakage current (I_{sub}) with variation of absolute temperature for Fin height of 20 nm, 60 nm and 80 nm.

This can be attributed to the rise in thermal voltage and hence an increased value of minority carrier concentration resulting in an enhancement in the

subthreshold leakage current. Further as the fin height decreases, there is a decrease in subthreshold leakage current as well. This is because of the total width of device decreases with the decrease in the value of the fin height, which results in lower subthreshold leakage current. Figure 5.8 shows the variation of subthreshold leakage current with variation in absolute temperature for three values of subthreshold swing factor (S).

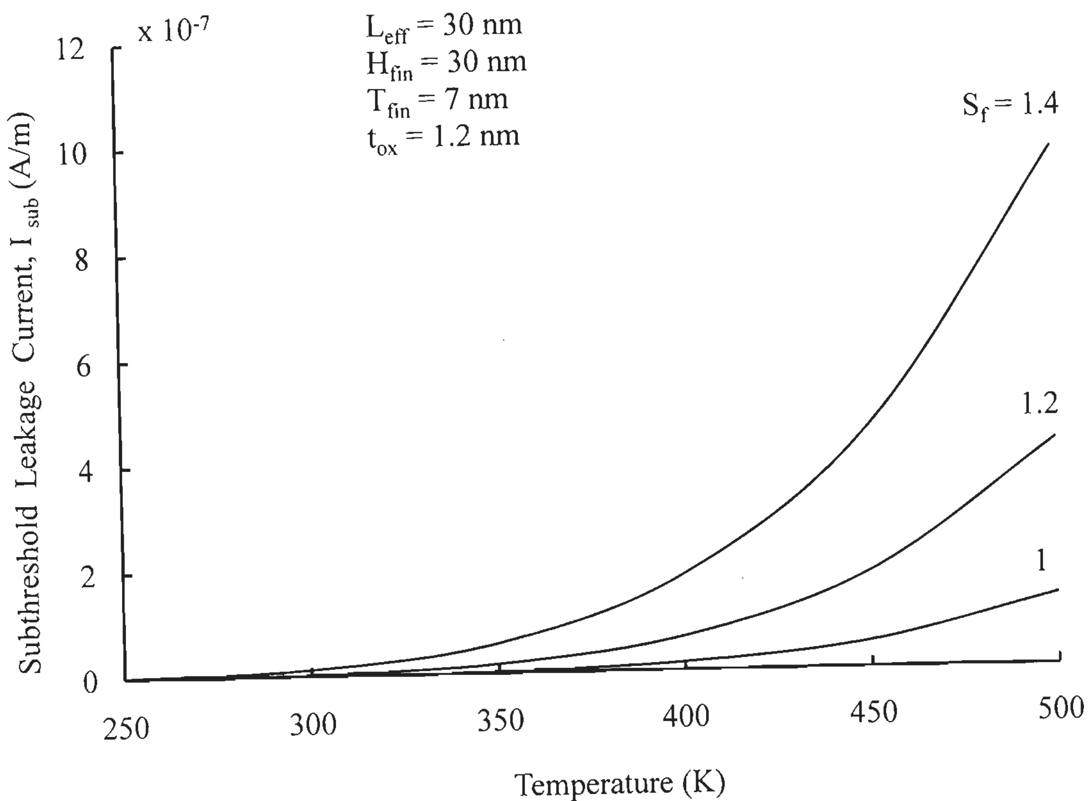


Figure 5.8 Variation of subthreshold leakage current (I_{sub}) with variation of absolute temperature for subthreshold swing factor of 1, 1.2 and 1.4.

It can be observed from the figure, as the subthreshold factor increases, there is an increase in the subthreshold leakage current at a fixed temperature. A larger subthreshold swing factor value primarily implies a larger variation in gate voltage to

change the current by one decade factor. This would primarily mean a larger effective gate voltage on drain side for FinFET structure under study. This would result in larger subthreshold leakage current.

Variation of direct tunneling current density with gate voltage for various oxide thicknesses is shown in figure 5.9. It can be seen from the figure, as the gate voltage increases, there is almost exponential rise in direct tunneling current characteristics. This is because of increased value of transverse electric field through the oxide layer which increases the probability of direct tunneling current.

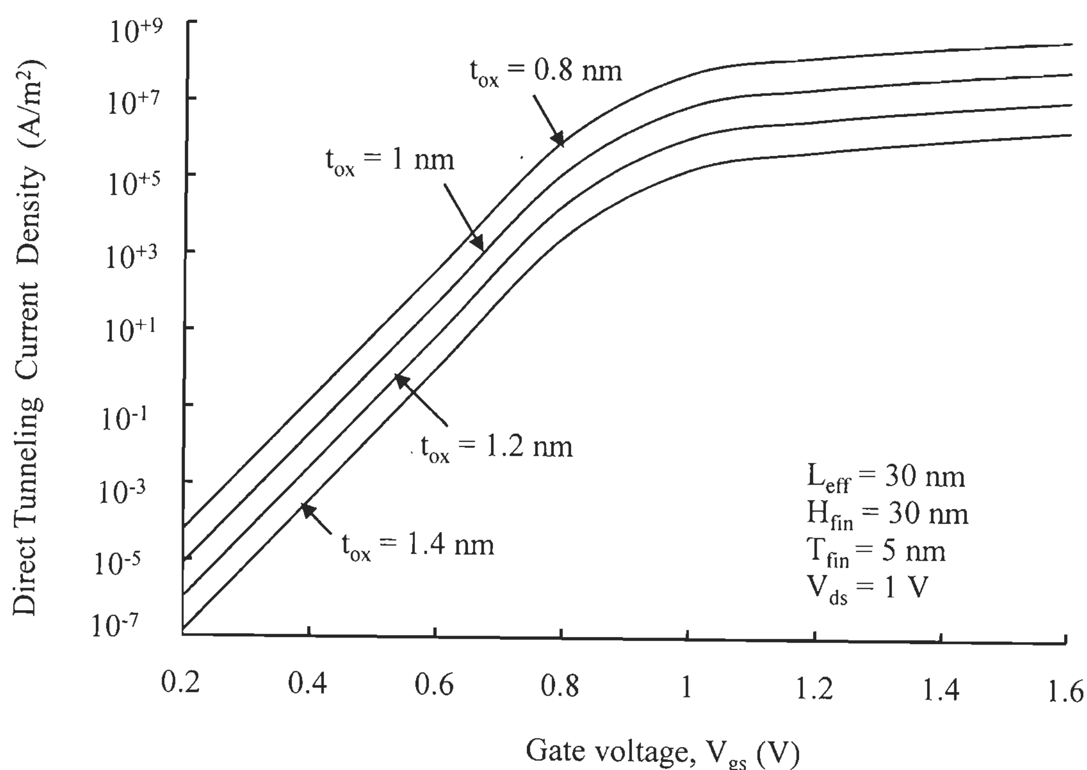


Figure 5.9 Variation of direct tunneling current density with gate voltage for oxide thickness (t_{ox}) of 0.8 nm, 1 nm, 1.2 nm and 1.4 nm.

For the purpose of validation, the results obtained on the basis of our proposed model have been compared with those obtained through reported experimental result

[17] for the variation of subthreshold swing factor with variation of effective channel length as shown in figure 5.10. It can be seen from the figure that there is a close match between the two, thus, validating our approach.

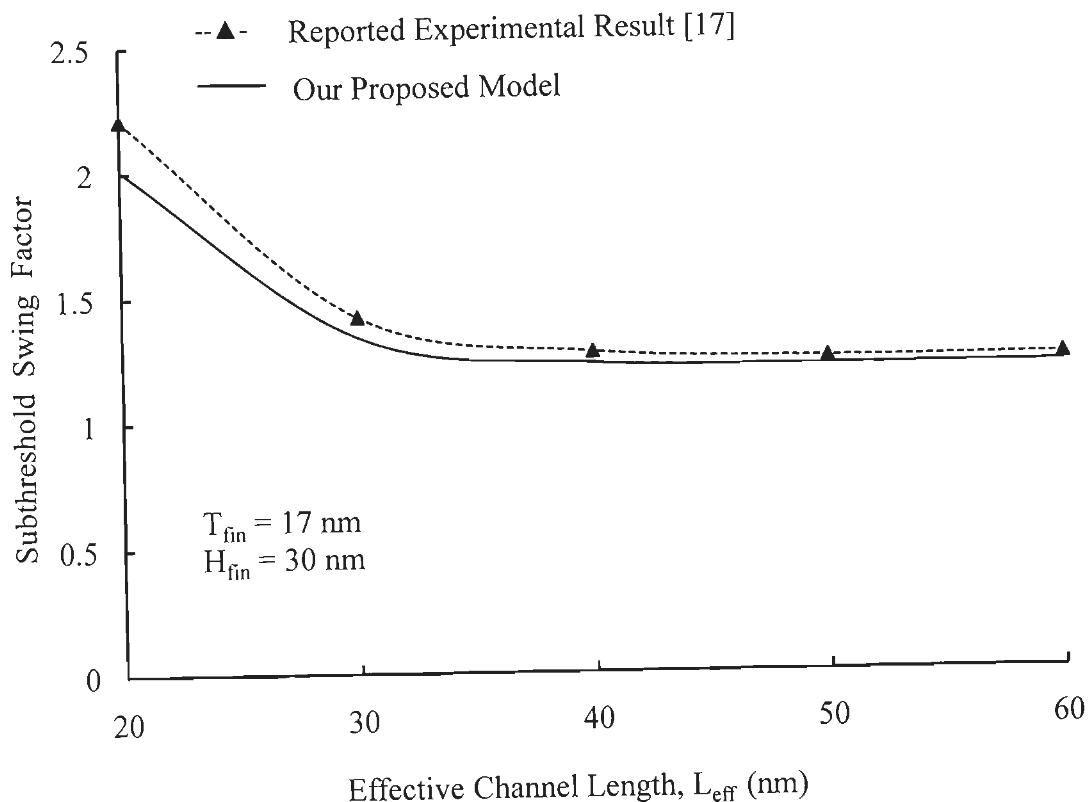


Figure 5.10 Variation of subthreshold swing factor with the variation of channel length for Our proposed model and reported experimental result [17].

The variation of subthreshold swing factor with variation of channel length for various fin thickness is shown in figure 5.11. It can be seen from the figure that the minimum value of subthreshold swing factor reaches asymptotically to unity. Further, it can be seen from the figure that, as the effective channel length reduces below 30 nm, there is gradual increase in the value of subthreshold swing factor. This increase in subthreshold swing factor is primarily because of access to short channel effects at

such small dimensions. Further it can be observed that, as the fin thickness increases, there is an increase in subthreshold swing factor. This is primarily due to larger cross-section area across which the channel formation has taken place and hence a larger inversion charge requirement is needed, which results in an increased value of subthreshold swing factor.

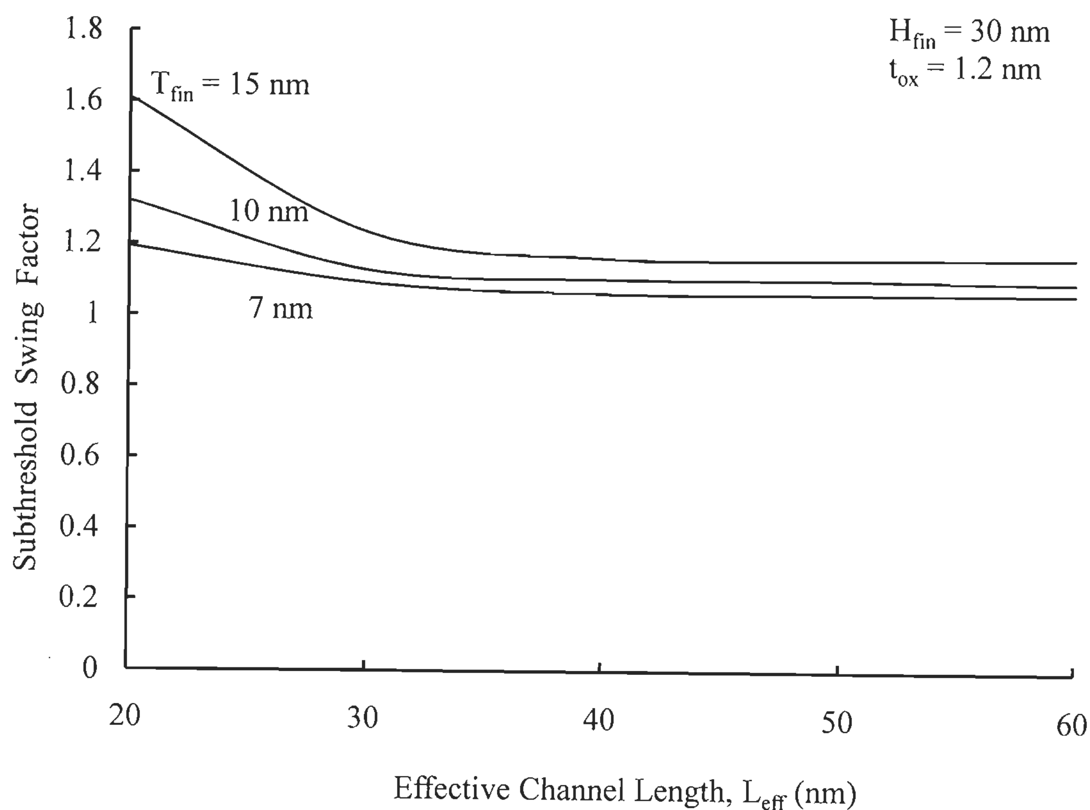


Figure 5.11 Variation of subthreshold swing factor with the variation of channel length for Fin thickness of 7 nm, 10 nm and 15 nm.

Variation of subthreshold swing factor with fin thickness for three devices with different channel length is shown in figure 5.12. It can be observed from the figure that, as the fin thickness increases, there is an increase in subthreshold swing factor. As the fin thickness increases, so does the area under the insulator across

which the inversion charge can be found. This requires a larger gate voltage variation in order to generate the same amount of increment/decrement of inversion charge. Further, it is seen that for a shorter channel length, the increase in subthreshold swing factor is higher as compared to a device with longer channel length. This is due to increased short channel effects for low dimension devices.

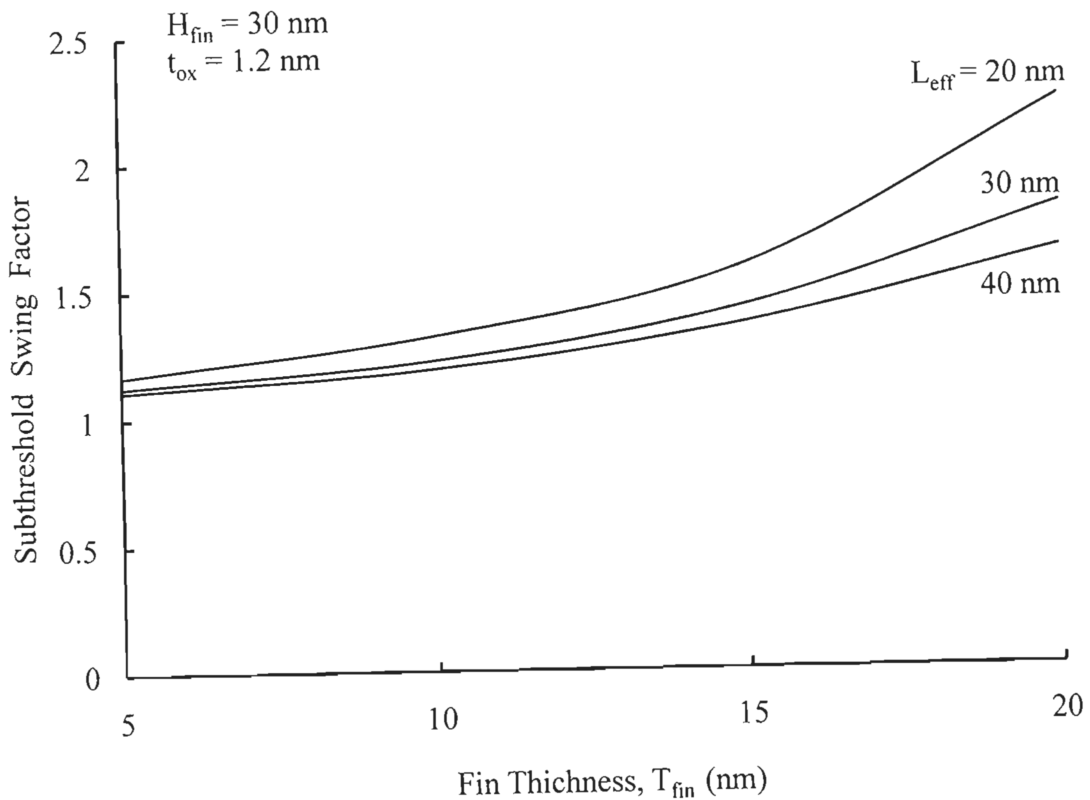


Figure 5.12 Variation of subthreshold swing factor with the fin thickness for channel length of 20 nm, 30 nm and 40 nm.

Figure 5.13 shows the variation of subthreshold swing factor with oxide thickness for various fin thickness. It can be seen that, for any fin thickness, as the oxide thickness increases, so does the subthreshold swing factor. This is due to the fact that with increasing oxide thickness, an enhancement in gate voltage is required

in order to generate same amount of inversion charge, which results in a larger subthreshold swing factor. Further, as the oxide thickness decreases, the subthreshold swing factor tries to reach its ideal value (one).

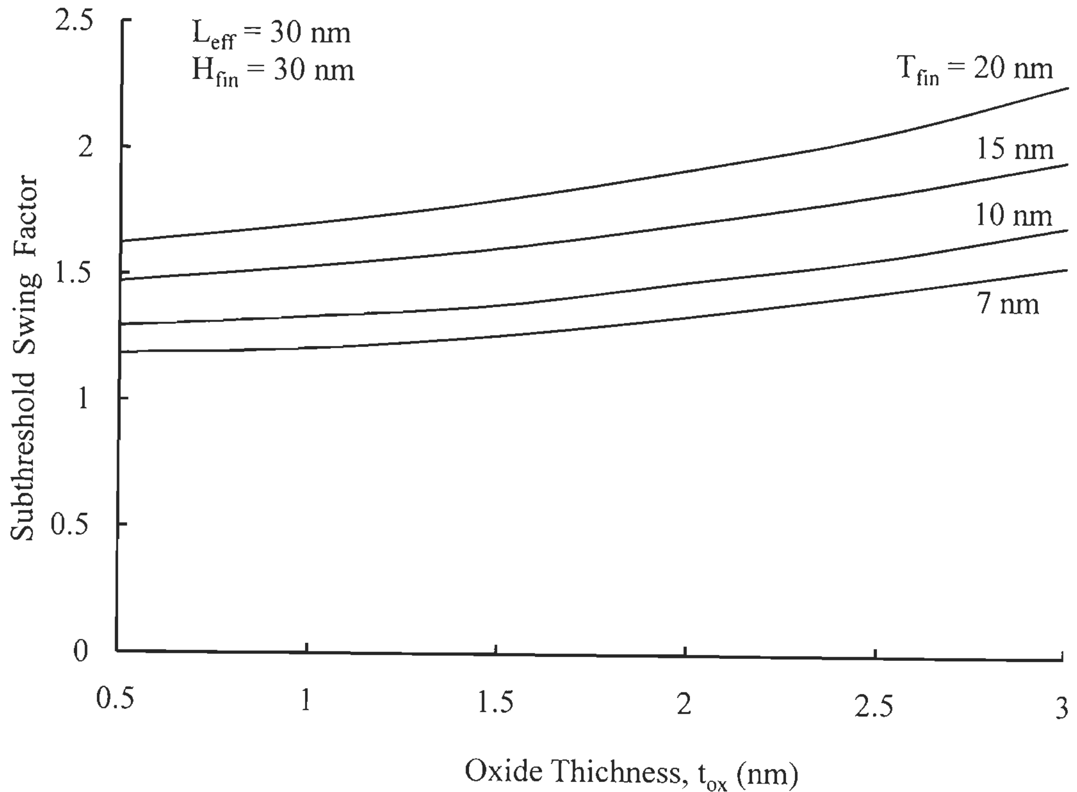


Figure 5.13 Variation of subthreshold swing factor with oxide thickness for Fin thickness of 7 nm, 10 nm, 15 nm and 20 nm.

Figure 5.14 shows the variation of sub threshold swing with fin height for three various fin thicknesses. It can be seen that for a fin thickness of 5 nm and fin height of 20 nm, we obtained near ideal sub threshold swing. Further, as fin height increases, the sub threshold swing tends to increase. This is primarily due to reduced transverse direction electric field. Moreover, for a fixed fin height, the sub threshold

swing increases with fin thickness. This implies that a larger fin height and fin thickness reduce the sensitivity of the device in sub threshold domain.

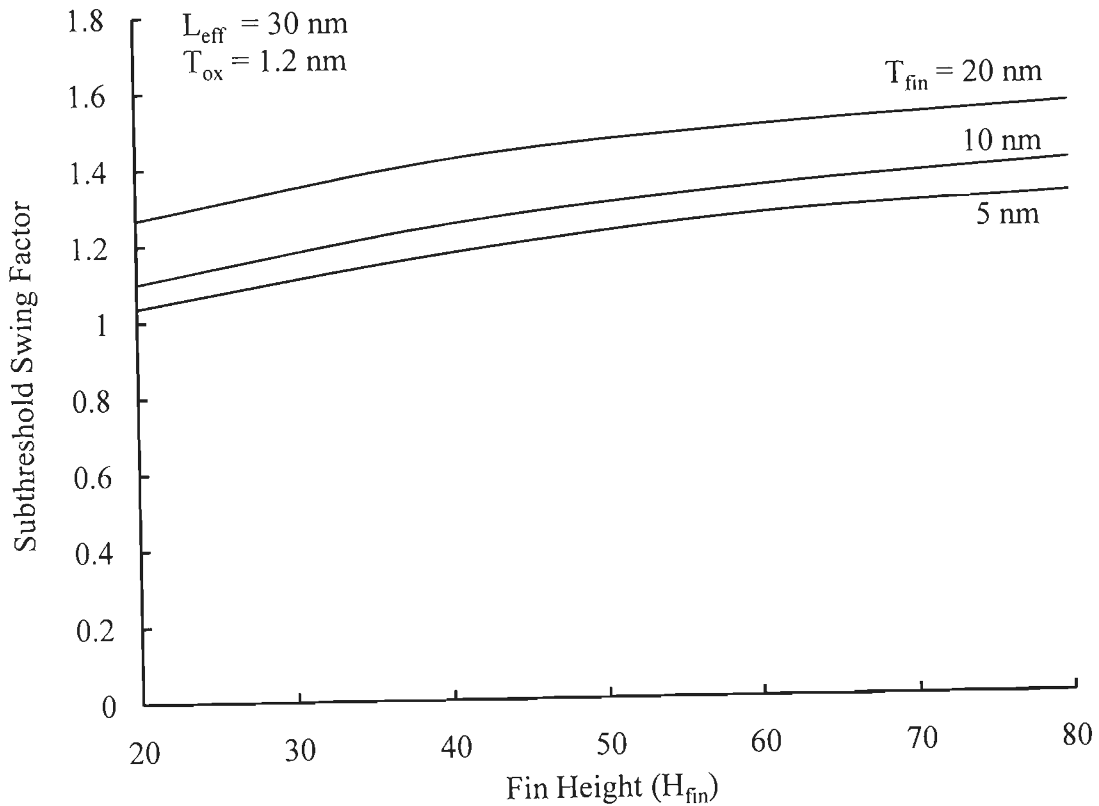


Figure 5.14 Variation of subthreshold swing with fin height for various fin thickness

5.6 Conclusion

This chapter presents the analytical modeling for estimation of leakage currents and subthreshold swing factor in Double Gate FinFET device. We have evaluated subthreshold swing factor, subthreshold leakage current and direct tunneling current in FinFET including process parameter variations. It is seen from our study that subthreshold swing factor increases below effective gate length of

30 nm. We have considered the temperature effect variation in subthreshold leakage currents. As the temperature increases the subthreshold leakage current also increases. The results obtained through our analytical model are compared with the reported numerical and experimental results. A close match between our proposed analytical model and reported results validate our approach. The study undertaken would help to design of robust FinFET structures which are process variation tolerant and less dependent on temperature variation.

FinFET Based Nanoscale Static Random Access Memory (SRAM) Cell Design: Analysis of Performance metric, Process variation, Underlapped FinFET and Temperature effect

6.1 Introduction

According to International Technology Roadmap for Semiconductors (ITRS) [65] by the year 2014, 94% of chip area will be occupied by the memory. Aggressive scaling in memory can occur in two manners. One is the cell miniaturization, which can be achieved by device modeling. Other being the peripherals and interconnect scaling. Device scaling to nanoscale regime brings many problems which are sensitive to process variation.

In recent times, it has been proposed to replace bulk transistors in SRAM with novel structures such as DG-SOI or FinFET structure [18, 29]. Such a proposal can be justified from the fact that these devices are easily scalable without showing SCE's. Further, the leakage current in typically less in FinFET as can be observed from the previous chapters. FinFET seems to be a promising candidate to be applied in the next generation SRAM technology [80, 88, 94] due to its superior scalability for a given gate insulator thickness, higher channel mobility, absence of random dopant fluctuation effects without compromising its performance.

Read stability is often used as the measure of the robustness of an SRAM cell against flipping during read operation. The hold stability is measured by fitting the largest square into the Voltage Transfer Characteristic (VTC) of the cross coupled inverters within the SRAM cell at the time the wordline of the cell is disabled. The

read stability and hold stability of SRAM cells is of significant importance in FinFET based SRAM design. Consequently, an accurate and efficient estimation of the FinFET based SRAM cell stability is necessary in the design phase to ensure the correct functioning of the SRAM as well as to achieve good yield of the cache system. The Static Noise Margin (SNM) has been widely adopted as a measure of the stability of SRAM cells [42, 94, 146, 180]. Maintaining sufficient Read Noise Margin (RNM) is always the main challenge of the scaling of SRAM technology [7, 21]. It has been reported that variations in Write Noise Margin (WNM) also have a profound impact on SRAM's stability during write operation for partially depleted SOI technology [91-92]. So far, the read and write margins (RM and WM) have been optimized by arranging the gate width of MOSFETs. However, this method will not be sufficient for the scaled CMOS technology in the near future, where process-induced random variation in the device performance will become serious. Then, it will be very difficult to manage the trade-off between RM and WM and ensure both the RM and WM only by the gate-width arrangement. In this case, some novel circuit approaches to enhance both RM and WM are helpful to overcome this difficulty [36-37].

The performance of SRAM subsystem is determined primarily by the delay involved in driving large loads on the bitline and the wordline. Due to the large size of the on chip SRAMs in microprocessors designed in nanometer nodes, leakage current is the major contributor to the total power dissipation in SRAMs. The exponential increase in leakage current results in large standby power. Increased transistor leakage and parameter variation present challenges for scaling of conventional six-transistor (6-T) SRAM cells [25, 49, 180]. The SRAM array parametric standby leakage contributors include well isolation leakage [54-56], subthreshold device leakage [82] and gate-oxide tunneling current [161-162]. The major concern in future SRAMs is

the leakage power consumption. Due to the reduced threshold voltage in future technologies, leakage power is increasing rapidly. Different SRAM cell designs have been proposed to target leakage control [143, 148, 154, 155]. To overcome these difficulties, optimization of the device structure is extremely important for low-power and robust SRAM cell design in sub-30 nm FinFET technologies.

FinFET based SRAM's immunity to mismatch induced by process variation becomes quite imperative. Although there are some reports on the impact of parameter fluctuations in FinFETs by direct measurement [7, 17, 50], the sensitivity of FinFET SRAM's stability to process variation and methods to enhance such stability have not yet been systematically addressed to the best of our knowledge. A FinFET uses an intrinsic body. It greatly suppresses the device-performance variability caused by the fluctuation in the number of dopant ions, while a planar-bulk MOSFET requires a heavily doped channel which causes serious process variability. It is preferable to extend the 6-transistor SRAM ability by effectively taking advantage of the FinFET-based technology together with the novel circuit technique.

Increased process variation in short channel transistors is reducing the robustness of bulk Fin based SRAM. FinFET based SRAM design has been proposed as an alternative solution to the bulk devices. This also results in reduced stability of SRAM cell. FinFET is suitable for future nanoscale memory circuits design due to its reduced Short Channel Effects (SCE) and leakage current. In this chapter, the analysis of Static Noise Margin (SNM), Read Noise Margin (RNM), Write Noise Margin (WNM) and static power with variation of width of access, load and driver transistor have been carried out for the stability of FinFET based SRAM cell. HSPICE simulation results have been presented for the SNM, RNM and WNM. Robust FinFET based SRAM design at 32 nm technology should ensure minimum sensitivity

to process variations along with proper functionality and low leakage power. In this chapter, we also analyze the effect of process variation and power consumption of FinFET based SRAM cell. Monte Carlo analysis was carried out to gauge the sensitivity of FinFET based SRAM cell to process variations. In this chapter, we also attempt to design a robust FinFET based 6-T SRAM cell using Predictive Technology Model (PTM) [124] and study its performance in the presence of process variations. We analyze the variation in Static Noise margin (SNM), Read Noise Margin (RNM), Write Noise Margin (WNM), and power with change in driver, load and access transistor widths. In order to limit static power dissipation in large caches, lower supply voltage can be used [76, 78, 107]. However, a low supply voltage coupled with large transistor variability compromises cell stability measured as Static Noise Margin (SNM) [41]. Although several attempts have been made to analyze the impact of process variations on SRAM [4, 7, 154], optimization of the cell has not been done for 32 nm technology.

This chapter is organized as follows: In Section 6.2; bulk SRAM cell design problems are discussed. Section 6.3; describes SRAM design trade off's. In Section 6.4; FinFET based SRAM design and performance metrics are analyzed. In Section 6.5; the effects of process variation on FinFET based SRAM are discussed. In Section 6.6; underlapped FinFET device is explained. Section 6.7; describes effect of temperature on FinFET. Results are discussed in section 6.8 and conclusion is provided in Section 6.9.

6.2 Bulk SRAM cell Design Problems

Bulk MOSFET structure scaling into the sub-50 nm regime requires heavy channel doping to control Short Channel Effects (SCE) and heavy super-halo implants

to control sub-surface leakage currents. Heavy doping degrades mobility due to impurity scattering and a high transverse electric field in the on state worsens sub-threshold swing and increases parasitic junction capacitance. Thus, for a given off-state leakage current specification, on-state drive current is degraded. Off-state leakage current is enhanced due to band-to band tunneling between the body and drain. Threshold voltage (V_{th}) variability caused by random dopant fluctuations is another concern for nanoscale bulk MOSFETs. With increasing variations, it becomes difficult to guarantee near-minimum-sized SRAM cell stability for large arrays in embedded low-power applications. Increasing transistor size, on the other hand, is counterproductive to the fundamental reason for scaling in the first place – to increase density. Access time is dependent on wire delays and column height. To speed up arrays, segmentation is commonly employed. With further reductions in bit-line height, the overhead area of sense amplifiers becomes substantial.

In a bulk MOSFET based SRAM array, exponential increase in leakage current results in large standby power. Furthermore, process variations result in mismatch in the strength of different devices in an SRAM cell. Such a mismatch can result in parametric failures, thereby degrading the design yield. Due to large leakage current and increased parametric variation, designing low-power and robust SRAMs is a major challenge in nanoscale technologies. Due to enhanced short channel effect (SCE), scaling single gate bulk CMOS devices beyond sub-50nm node is becoming increasingly difficult. Ultrathin body double-gate MOSFET (DGFET) devices are suitable in sub-50nm technologies due to their higher immunity to SCE, better scalability and increased on current compared to single gate devices. Furthermore, DGFET has negligible junction capacitance which significantly reduces the circuit delay. Moreover, body in DGFET devices is lightly doped and threshold voltage (V_{th})

is principally controlled using metal gate work function. The lightly doped body eliminates V_{th} variations due to random dopant fluctuation (RDF).

6.3 SRAM Design Tradeoffs

6.3.1. Area vs. Yield: The functionality and density of a memory array are its most important properties. Functionality is guaranteed for large memory arrays by providing sufficiently large design margins which are determined by device sizing (channel widths and lengths), the supply voltage and marginally by the selection of transistor threshold voltages. Although upsizing the FinFET's increases the noise margins, it increases the cell area and, thus, lowers the density [180].

6.3.2. Read vs. Write Stability: The Read Voltage (V_{read}) defined as the minimum voltage that the storage nodes can reach during read operation. It is determined by the voltage division between a Pull Down (PD) FinFET and an Access (AC) FinFET. The weaker the access FinFET's driving strength, the smaller the V_{read}, leading to a larger Read stability. The Write Voltage (V_{write}) defined as the maximum voltage the storage nodes can reach during write operation, is determined by the voltage division between the access FinFET and the Pull Up (PU) FinFET. The stronger the access FinFET's driving strength, the smaller V_{write}, leading to larger write stability. Thus, a trade-off relationship exists between read stability and write stability.

6.3.3. Speed vs. Leakage Current: A fast SRAM cell dissipating low leakage power is required. This is increasingly at odds with a fundamental technology trade-off between transistor speed and leakage. The lower the threshold voltage (V_{th}) of a transistor, the faster it becomes and the more leakage power it dissipates. As the supply voltage is scaled down, the FinFET threshold voltage is also scaled to maintain

performance. As a result of the low threshold voltage, leakage power increases rapidly due to the exponential relationship between leakage and V_{th}. Leakage can be reduced by using higher-V_{th} transistors, but by using all-high-V_{th} transistors, SRAM cell performance degrades by an unacceptable margin.

6.4 FinFET based SRAM cell Design

FinFETs have emerged as the most suitable candidate for DGFET structure as shown in figure 6.1 [42, 80]. Proper optimization of the FinFET devices is necessary for reducing leakage and improving stability in FinFET based SRAM. The supply voltage (V_D), Fin height (H_{fin}) and threshold voltage (V_{th}) optimization can be used for reducing leakage in FinFET SRAMs by increasing Fin-height which allows reduction in V_D. [44, 108]. However, reduction in V_D has a strong negative impact on the cell stability under parametric variations. We require a device optimization technique for FinFETs to reduce standby leakage and improve stability in an SRAM cell.

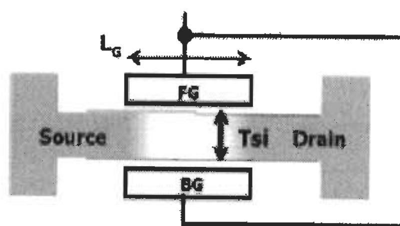


Figure 6.1 Double Gate FinFET

FinFET based SRAM cells are used to implement memories that require short access times, low power dissipation and tolerance to environmental conditions. FinFET based SRAM cells are most popular due to lowest static power dissipation among the various circuit configurations and compatibility with current logic

processes. In addition, FinFET cell offers superior noise margins and switching speeds as well. Bulk MOSFET SRAM design at sub-45 nm node is challenged by increased short channel effects and sensitivity to process variations. Earlier works [121, 180] have shown that FinFET based SRAM design shows improved performance compared to CMOS based design. Functionality and tolerance to process variation are the two important considerations for design of FinFET based SRAM at 32nm technology. Proper functionality is guaranteed by designing the SRAM cell with adequate read, write, static noise margins and lower power consumption.

SRAM cells are building blocks for Random Access Memories (RAM). The cells must be sized as small as possible to achieve high densities. However, correct read operation of the FinFET based SRAM cell is dependent on careful sizing of M1 and M5 in figure 6.2. Correct write operation is dependent on careful sizing of M4 and M6 as shown in the figure 6.2. As explained [44, 49, 72], the critical operation is reading from the cell. If M5 is made of minimum-size, then M1 must be made large enough to limit the voltage rise on Q' so that the M3-M4 inverter does not inadvertently switch and accidentally write a '1' into the FinFET based SRAM cell.

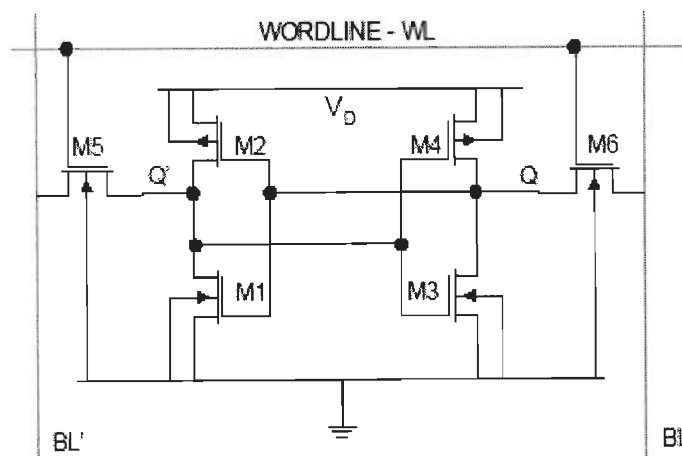


Figure 6.2 6T SRAM cell [44]

As explained [44], the sizing of the FinFET M5 and M6 is critical for correct operation once sizes for M1-M2 and M3-M4 inverters are chosen. The switching threshold for the ratioed inverter (M5-M6)-M2 must be below the switching threshold of the M3-M4 inverter to allow the flip-flop to switch from Q=0 to Q=1 state. The sizes for the FinFET's can be determined through simulation, where M5 and M6 can be taken together to form a single transistor with a length twice the length of the individual transistors. It is well-understood that sizing affects noise margins, performance and power [72, 94, 95]. Therefore, sizes for pFinFET and nFinFET must be carefully selected to optimize the tradeoff between performance, reliability and power. We have studied FinFET based SRAM design issues such as: read and write cell margins, Static Noise Margin (SNM), power evaluation, performance and how they are affected by process induced variations [44].

6.4.1 FinFET Based SRAM Performance Metrics

A. Static Noise Margin (SNM): Stability, the immunity of the cell to flip during a read operation, is characterized by Static Noise Margin (SNM). SNM is calculated by the side of the largest square inside the FinFET based SRAM cross-coupled inverter characteristic measured during the read condition (BL = BL' = V_D, and WL = V_D) [180]. Static Noise Margin is the standard metric to measure the stability in SRAM bit-cells. The SNM depends on the choice of the V_{th} for the FinFET's used in the SRAM cells. A high V_{th} means that drive current of these devices is small making the write operation more difficult, thus, increasing the SNM. One approach to achieve a low power cell with high stability is to use high V_{th} devices at the cost of performance. FinFETs provide a high drive current even with larger V_{th}, thereby, achieving high noise margins along with good write stability [80]. The SNM is seen

to be the most sensitive to threshold voltage fluctuations in the access and pull-down nFinFETs and least sensitive to the fluctuations in the pull-up pFinFET device. For FinFETs, the effect of L_g variation on V_{th} is small, so the effect on the SNM is also small.

B. Read Noise Margin (RNM): RNM is often used as the measure of the robustness of an SRAM cell against flipping during read operation [135]. For read stability (High RNM) of FinFET based SRAM cell, pull down FinFET is typically stronger than access FinFET. The read margin can be increased by upsizing the pull-down transistor i.e nFinFET, which results in an area penalty and/or increasing the gate length of the access FinFET increasing the 'WL' delay and hurting the write margin. A careful sizing of the FinFET device is required to avoid accidentally writing a 1 into the cell while trying to read a stored "0", thus, resulting in a read upset. The ratio of the widths of the pull-down FinFET to the access FinFET commonly referred to as the cell ratio (CR) determines how high the "0" storage node rises during a read access [41]. The Cell Ratio (CR) = $(W_1/L_1)/(W_5/L_5)$ is as shown in figure 6.2,. Smaller cell ratios translate into a bigger voltage drop across the pull-down FinFET requiring a smaller noise voltage at the "0" node to trip the cell. During a read operation, the conducting access FinFET lies in parallel to the pull-up PMOS, lowering the gain of the static transfer characteristic and further decreasing cell immunity to noise.

C. Write Noise Margin (WNM): Write Noise Margin (WNM) is the maximum bitline (BL) voltage that is able to flip the state of the FinFET based SRAM cell while bitline bar (BL') voltage is kept high [80, 132]. Higher the WNM, greater is the stability. Use of a weaker pull up (pFinFET) and a stronger access FinFET helps the

node storing “1” to discharge faster, thus facilitating a quicker write of “0”. The write margin can be measured as the maximum BL’ voltage that is able to flip the cell state while BL is kept high. Hence, the write margin improves with a strong access and a weak pull up FinFET at the cost of cell area and the cell read margin.

D. Power and Delay: Power dissipation of the FinFET SRAM cell assesses the utility of the cell in portable devices. The fundamental advantage of the FinFET based SRAM is in its low access time and power dissipation due to low SCE’s and leakage current in FinFET device. While a strong driving current reduces the access time, it also increases the power dissipation in the SRAM cell. In SRAM, the propagation delay depends on the column height and wire delays. Thus segmentation is employed to reduce the delay. Since the power-delay-product is constant for a device, increasing one decreases the other and vice-versa. Upsizing the FinFET device in SRAM cell decreases the delay at the cost of slightly increased power dissipation. However to reduce power dissipation, leakage currents need to be minimized which warrant an increase in the channel length or higher transistor threshold voltages. Larger channel length results in higher delay and there exists a trade-off between these two performance indices.

6.5. Effect of Process Variation on FinFET

With scaling, process imperfections result in significant variation in FinFET device characteristics. Furthermore, process variations result in mismatch in the strength of different FinFET devices in an SRAM cell. Such a mismatch can result in parametric failures, thereby degrading the design yield. Due to increased parametric

variation, designing low-power and robust FinFET based SRAM cell is a major challenge in nanoscale technologies.

Process variations comprise of FinFET parameters (Channel length (L_{eff}), Threshold voltage (V_{th}) etc.) which are no longer deterministic and die-to-die and within-die variations may be random or correlated. Die-to-die fluctuations (from lot to lot and wafer to wafer) result from factors such as processing temperature and equipment properties. Conversely within-die, variations result from factors such as nondeterministic placement of dopant atoms and channel length variation across a single die. The reason behind the observed random distribution is due to the limited resolution of the photolithographic process which causes W/L variations in FinFET device. The variations in W and L are not correlated because W is determined in the field oxide step while L is defined in the poly and source/drain diffusion steps. In case of random variations, the design parameters are totally uncorrelated. As for instance, variations in FinFET length are unrelated to V_{th} variations.

With the scaling of technology, process imperfection is becoming a major concern in maintaining the reliability of an SRAM cell. The major sources of parameter variations in FinFET are T_{fin} and L_{eff}. In FinFET based SRAM, these parameters include Fin width (W_{fin}), Fin thickness (T_{fin}) and threshold voltage (V_{th}). FinFET based SRAMs are built using minimum size FinFET device to minimize area, making it highly vulnerable to process variations [42]. Memory designs are optimized for 6σ variations. SRAM failure can occur due to an increase in access time, failure to write a bit into the cell, accidental writing into memory during read or loss of stored bit in standby mode. In scaled technologies, an optimal design strategy of FinFET based SRAM should consider minimization of area and access times in conjunction with reducing the failure probabilities due to variations.

Table 6.1 Parameters used in simulation

Parameters	**Values**
L_{eff}	32 nm
T_{fin}	8.6 nm
t_{ox}	1.4 nm
Channel Doping	Intrinsic
Source/Drain Doping	10^{26} m^{-3}
$Vt_{0,n}$	0.29 V
$Vt_{0,p}$	-0.25 V

6.6 Underlapped FinFET Device

The Predictive Technolog Model (PTM) used in our study models the FinFET device as a self-aligned Double Gate (DG) MOSFET, but without the fin extension regions. This model is satisfactory to understand the characteristics of the FinFET device and to appreciate its merits. A typical under lapped FinFET device structure is shown in figure 6.3. However, technology constraints prevent thin fins and abrupt junctions from being fabricated [156]. Thus, the double gate structure given in the PTM model [124] needs to be modified for FinFET to cater for the fin extension regions that result due to technological limitations.

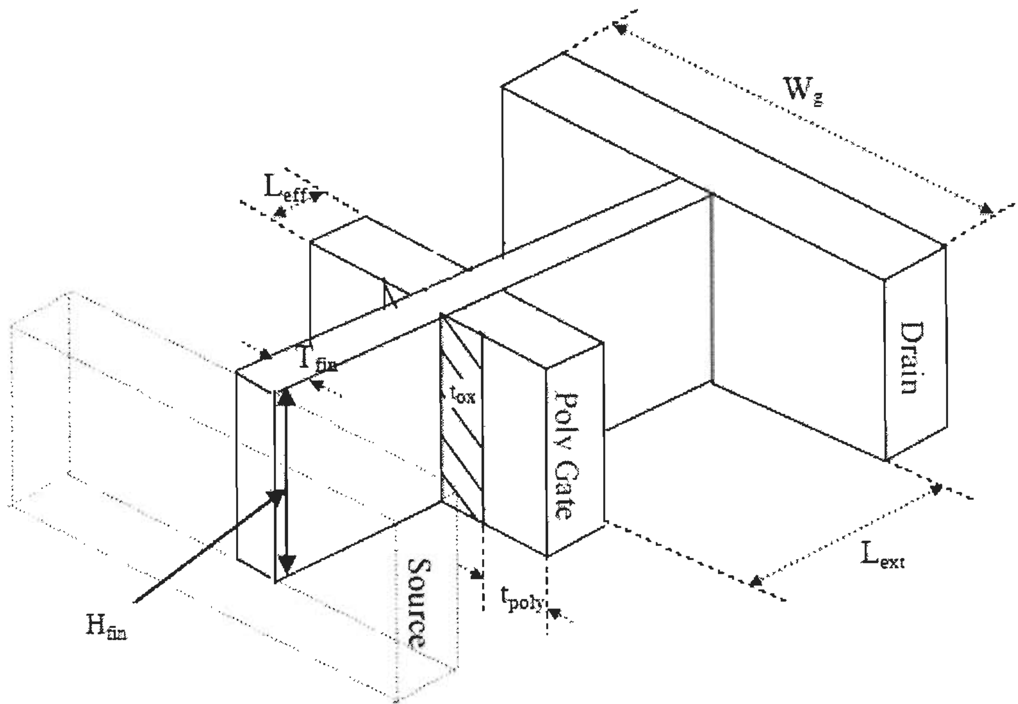


Figure 6.3 A typical underlapped FinFET device

The introduction of the fin extension regions in FinFET device leads to parasitic resistances (due to constriction/expansion of the current path, electric field lines and ohmic nature of the extension, respectively) and parasitic capacitances (due to electrodes in close proximity) [6, 87]. The underlapped FinFET structure with fin extension regions, however, has lesser Gate Induced Drain Lowering (GIDL) due to physical separation of the gate and drain region which prevents the gate from straggling the drain.

As discussed before in FinFET device, the channel is largely undoped (fully depleted) to avoid mobility degradation and V_{th} variation due to doping fluctuations. The extension regions of FinFET if left undoped offer a large resistance to the drain current, severely restricting their utility for low power applications with low voltage supplies. The current driving capability of the FinFET is expected to be severely degraded as a result of this. Gulzar A. Kathawala et al [48] showed that the current in

fact drops nonlinearly with fin extension length. The resistivity of the extension region is decreased in the fabrication process itself by silicidation process in which a layer of titanium doped Si is implanted to increase the conductivity of the extension region in FinFET.

Inspite of the aforesaid reasons, the FinFET effectively reduces leakages as compared to the overlapped device (PTM), follows a direct process flow from the CMOS technology and hence it is easy to fabricate without major overhead costs. The introduction of the fin extension also makes the voltage just outside the channel on the source side, higher than ground. This effectively reduces the effect of the gate in inverting the channel and thus, the drive current is further reduced.

6.6.1 Various Parameters of Underlapped FinFET

The parameters as mentioned in the figure 6.3 are: L_{eff} – Gate Length, T_{fin} – Thickness of the fin layer, H_{fin} – Height of the fin, t_{poly} – Thickness of the polysilicon layer present over the gate oxide, t_{ox} – Thickness of the oxide film, L_{ext} – Length of the fin extension region between the gate-source or the gate-drain region, W_g – Width of the source/drain regions, $W_{S/D}$ – Length of the source/drain contact regions.

6.6.2 Monte Carlo Analysis of FinFET Process Variations

The reason behind the observed random distribution of FinFET device parameters is due to the limited resolution of the photolithographic process which causes W/L variations in MOS transistors. The variations in W and L are not

correlated because W is determined in the field oxide step while L is defined in the poly and source/drain diffusion steps. In FinFET based SRAM, the process parameters variation include FinFET width (W_{fin}), fin thickness (T_{fin}) and threshold voltage (V_{th}). These variations affect the noise margins, power consumption and delay. Memory designs are optimized for 6σ variations [42]. To assess the impact of process parameters on FinFET SRAM, we carried out Monte Carlo simulations on HSPICE for 1000 sample values assuming 3σ equal to 10% of the mean value.

6.6.3 Effect of Temperature on FinFET's Performance

Increased packing density has led to power dissipation to become a critical bottleneck in the design of nanoelectronics. The local temperature rise can result in circuit malfunction and can also impact performance, power and reliability. For every 10°C increase in temperature, a FinFET's drive current decreases approximately by 4% and interconnect (Elmore) delay increases approximately by 5% [82, 168]. Power density (power dissipation per unit area) of a CMOS chip is given by = $CV_D^2 f$, where C is the node capacitance per unit area and is based on the average switching activity of the signal, V_D is the supply voltage and f is the clock frequency. With increase in temperature, the leakage current increases exponentially, (a difference of 30° C will affect the leakage by 30%) and hence, the power dissipation increases substantially in FinFET device. This, in-turn, further increases the temperature and the cycle continues until thermal runaway occurs. Hence, temperature is one of the most important performances metric in future VLSI circuit designs.

6.7. Results and Discussion

Figure 6.4 shows the variation of butterfly curve for load FinFET M2 with variation of its width. It can be seen that the high Static Noise Margin (SNM) reduces and low SNM increases with decrease in the width of load FinFET M2. Thus, as width of the load FinFET reduces, so does the driving capability of the load device. This implies that Q reaches to V_{OH} at a much higher voltage, thus, resulting in a decrease in high SNM. It is further observed that as the widths of the pull-up device decreases, the switching threshold also tends to reduce. Since the driving capability of M2 reduces with the reduction in width, therefore, it requires lesser amount of voltage at BL' for the purpose of switching threshold.

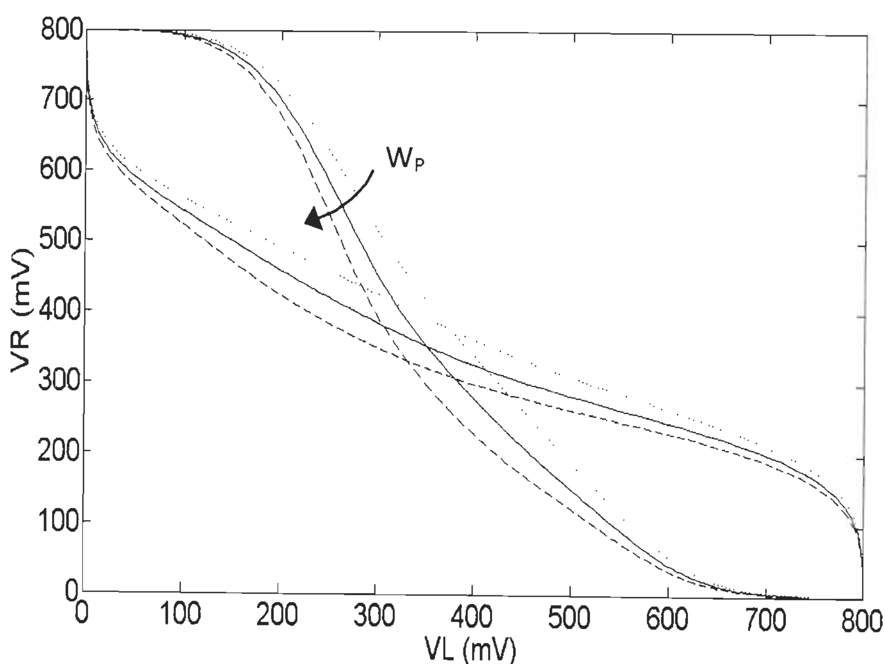


Figure 6.4 SNM variations with width of Load

The variation of Static Noise Margin (SNM) for driver FinFET M1 with variation of its width is shown in figure 6.5. It can be inferred from the figure that with increase in the width of driver FinFET M1, the high SNM reduces and low SNM

increases. This is due the fact that the leakage current is considerably reduced due to increased control of the FinFET device structure, resulting relatively in high I_{on}/I_{off} ratio. In the case of RNM, the stability of the cell is most seriously compromised as the node containing '0' is pulled up to a voltage determined by the relative sizing of driver and access FinFET's.

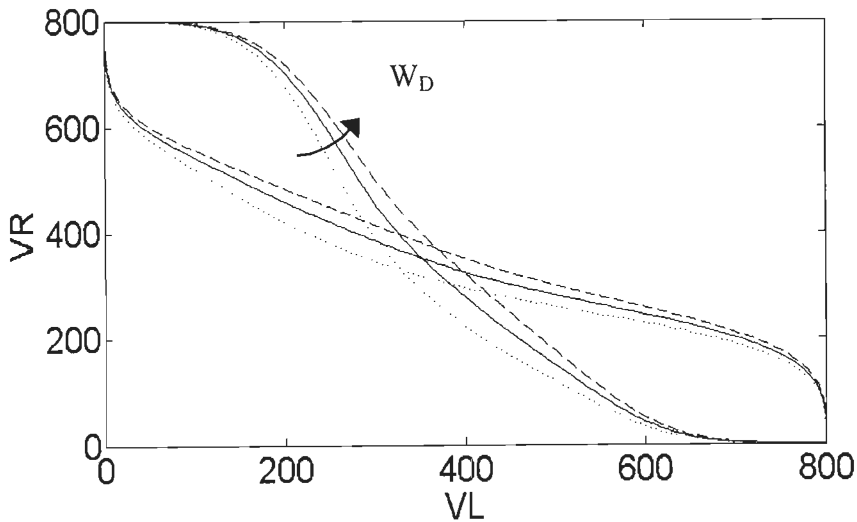


Figure 6.5 SNM variations with width of Driver

Figure 6.6 show the variation of WNM and RNM of a cell with the width of the load FinFET. A stronger pFinFET gives a higher RNM as it is difficult to pull down the '1' node. This is so because with an increase in the width of the pFinFET, its resistance decreases and hence the potential drop. With an increase in width of the access FinFET, the drop across it decreases, making it difficult to pull up the node '0', thus resulting in an increase in RNM. Further WNM decreases with an increase in the width of load FinFET. As the width increases, its current driving capability also increases. It makes the node Q' vary more closely with V_D as compared to the BL'

and hence, there is a decrease in WNM. For an increase of 70 nm of width of load FinFET, there is a 32 % fall in WNM for 30 nm technology.

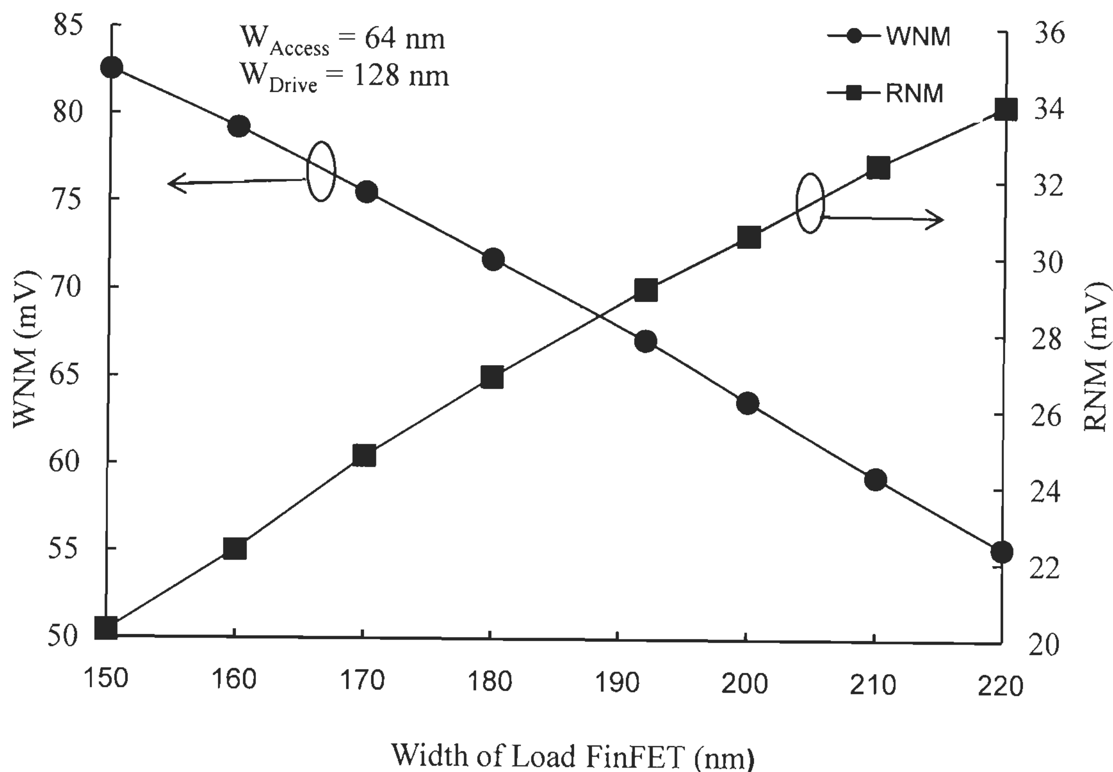


Figure 6.6 WNM and RNM variation with width of Load FinFET

Variations of WNM and RNM with the driver FinFET are shown in Figure 6.7. During write cycle, the write failure is said to occur if the bitline is unable to write '0' in the node '1'. Write Noise Margin denotes the voltage that must be added to the node '1' during the write cycle for write failure to occur. In this case, the nodal voltage is determined by the access and the load FinFET's which forms a potential divider. A stronger load FinFET and/or a weaker access FinFET make it difficult for the data to be flipped at the node storing '1'initially and hence WNM goes down. The

RNM increases with width of driver FinFET. Larger the width of the driver FinFET, easily it can pull down the node voltage at Q' which results in increased RNM.

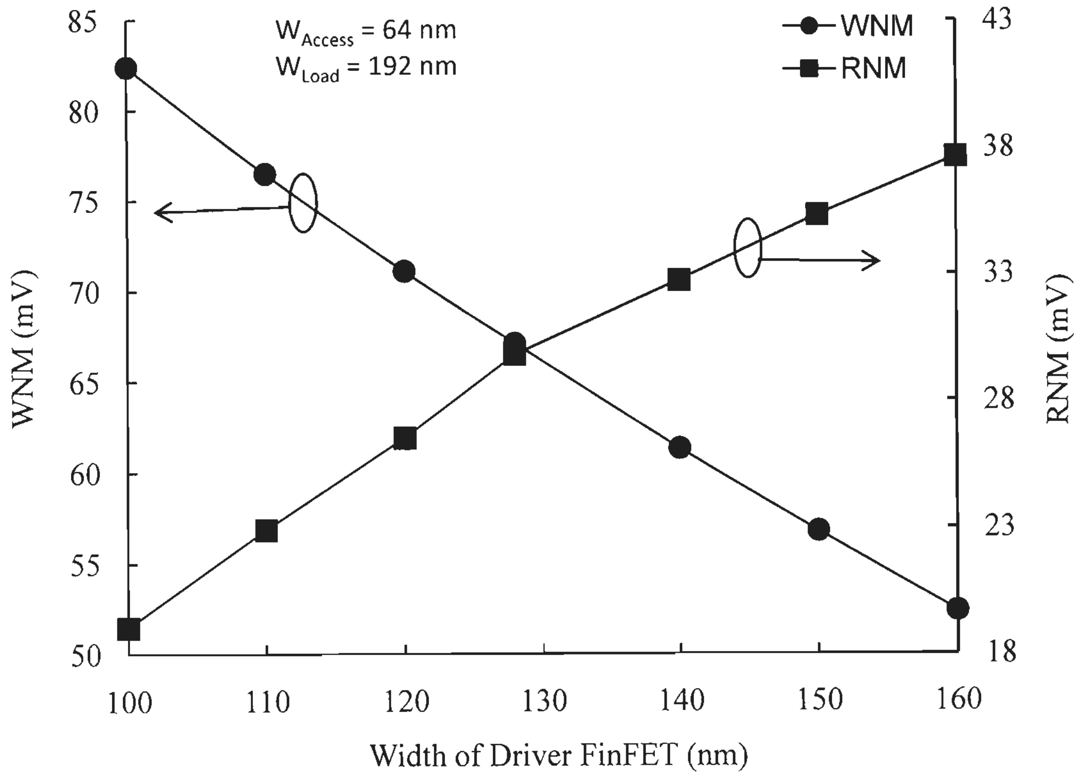
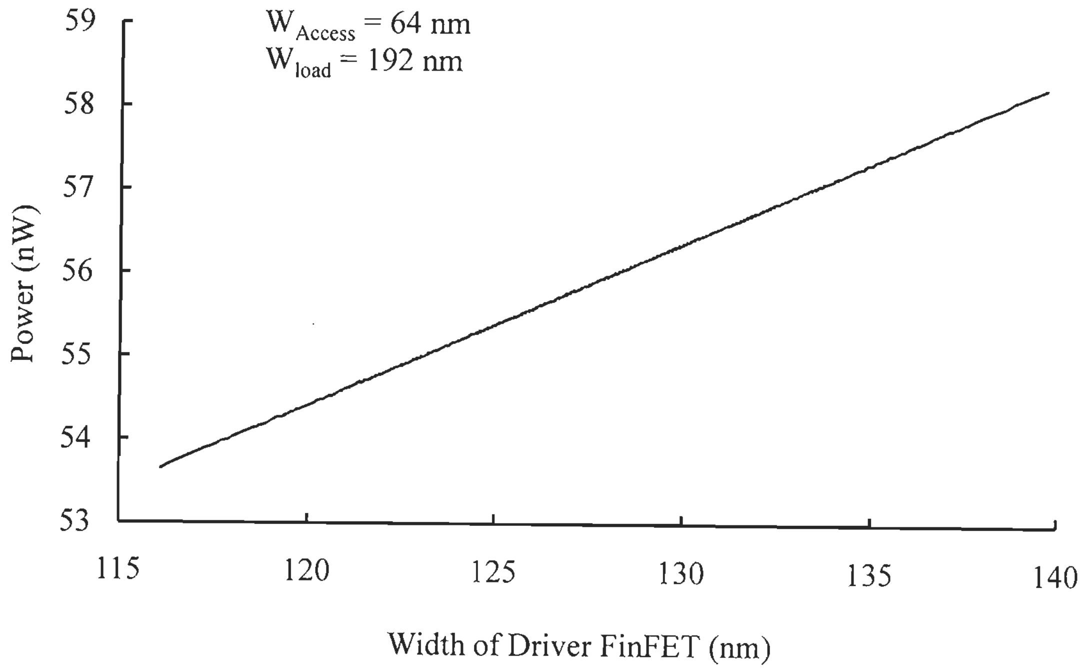


Figure 6.7 WNM and RNM variation with width of Driver FinFET

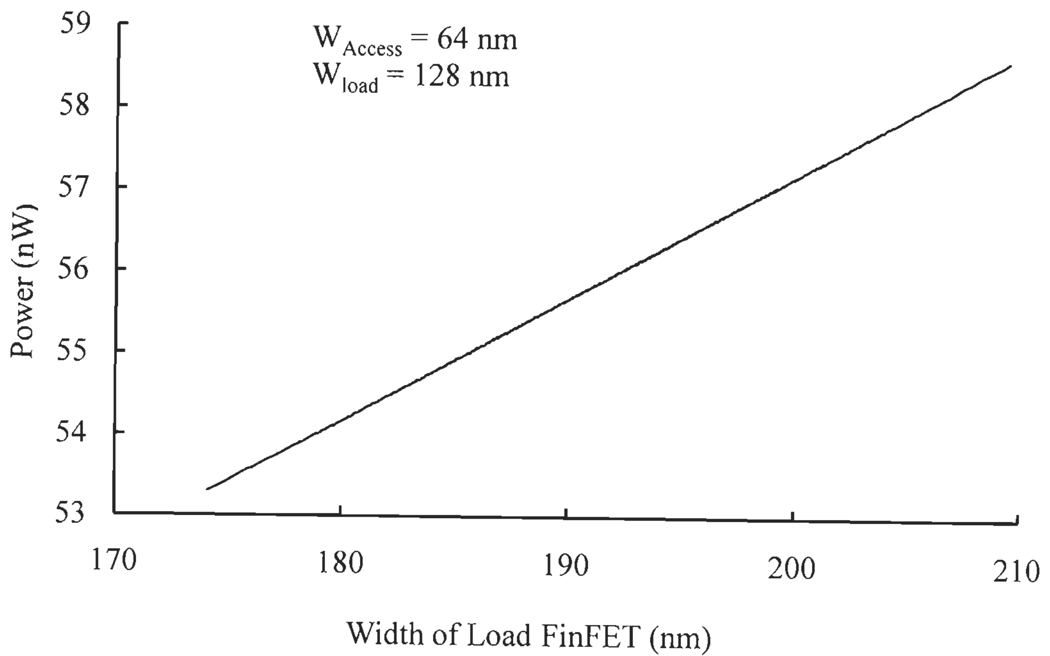
Figures 6.8.a and b show the variation of static power with varying width of driver FinFET and load FinFET, respectively. It can be seen from the figure that the static power dissipation increases with an increase in width of both driver as well as load FinFET. As the width increases so does the total current flow to the device resulting in largest power dissipation.

Figures 6.9.a and b show the Monte Carlo simulation results for RNM and WNM to quantify the effect of process variation arising due to variation in FinFET's widths. The simulation was carried out for 1000 values, assuming 3σ equal to 10% of

the mean value. Tables 6.2.a and b show the mean and standard deviation values for RNM and WNM variation.



Figurer 6.8.a Static Power variation with width of Driver FinFET



Figurer 6.8.b Static Power variation with width of Load FinFET

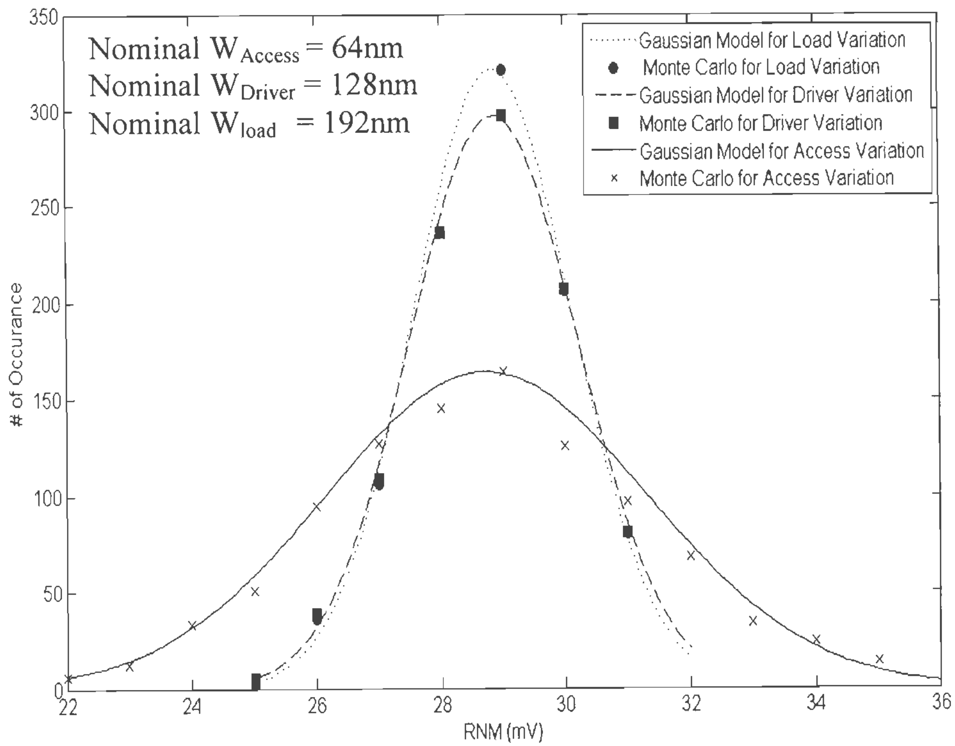


Figure 6.9.a Variations and Distribution of RNM

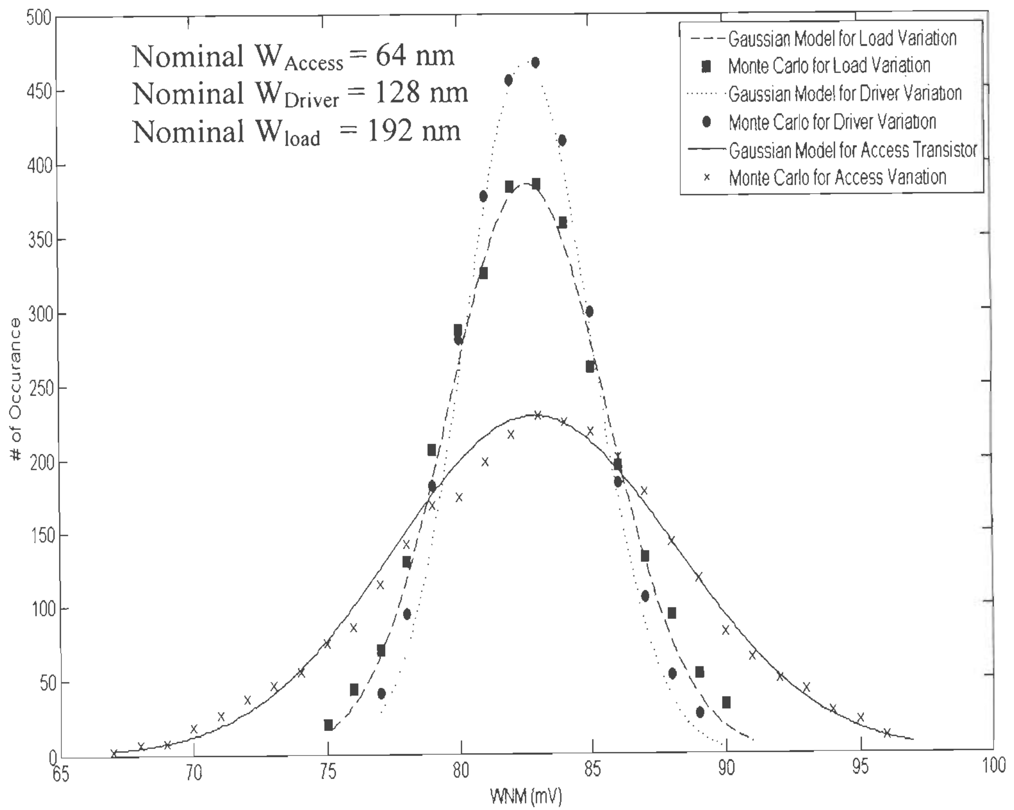


Figure 6.9.b Variations and Distribution of WNM

Table 6.2.a Mean and Standard Deviation of RNM Monte Carlo Analysis

	Load	**Driver**	**Access**	**All W**
Mean (mV)	28.8394	28.8461	28.7201	29.0572
Standard Deviation (mV)	1.2505	1.3389	2.5833	3.2620

Table 6.2.b Mean and standard Deviation of WNM Monte Carlo analysis

	Driver	**Load**	**Access**	**All W**
Mean (mV)	82.6377	82.6057	82.8486	66.7410
Standard Deviation(mV)	2.3682	2.9959	5.3513	5.9785

In our proposed FinFET model, we have assumed the entire fin extension regions doped with a concentration of 10^{26} m^{-3}. The silicide implants could be modeled with undoped extension regions after exploring the current distribution using device simulators, but we have neglected these implants. The source/drain regions have been assumed to be doped with a density of 10^{26} m^{-3}.

Figure 6.10 shows the on and off drain current with varying values of L_{ext}. It was attempted to optimize the L_{ext} for the best I_{ON}/I_{OFF} ratio with I_{ON} measured for $V_G = 0.8V$. However, as the graph shows the trend was found to be monotonously decreasing. Also it has been shown that symmetrical extension regions offer the best performance. The L_{ext} was arbitrarily assumed to be 64 nm on each side for all the simulations. It has been realized that for the underlapped FinFET, because of the series resistance at the source side, the net voltage available to invert the channel is now lesser. Thus, it is expected that the drain current has been decreased for the same gate voltage compared to the normal PTM based FinFET.

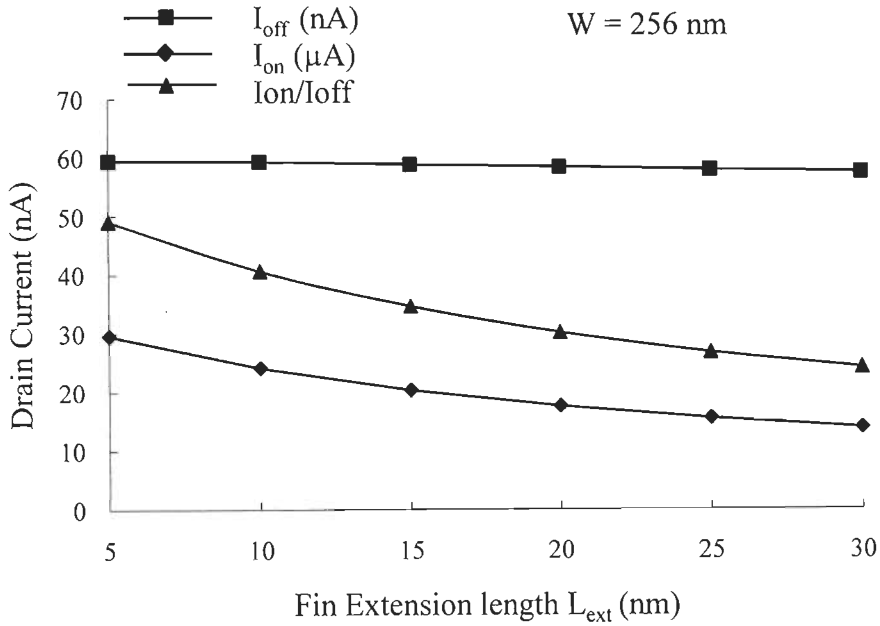


Figure 6.10 Variation of I_{ON} and I_{OFF} with Fin Extension Length (L_{ext})

The underlapped FinFET model obtained after the insertion of the parasitics into the PTM model is shown figure 6.11. The parasitic capacitances have been lumped to the gate. Two fictitious terminals have been added at the gate and the source side. The parasitic series resistances have been added between these terminals and the actual source/drain terminals of the original model. In this way, the net voltage at the source/drain of the original model is reduced because of the resistive drop across the series parasitic resistances. Table 6.3 summaries the parameters of the underlapped FinFET device used for the simulations.

Table 6.3 Parameters for the Underlapped FinFET device

Parameter	**Value**
L_{eff}	32 nm
L_{ext}	64 nm
T_{fin}	8.6 nm
t_{ox}	1.4 nm
$N_{S/D}$	10^{26} m^{-3}
$N_{channel}$	Intrinsic (Si)
$W_g \approx (2t_{poly}+T_{fin}+2t_{ox})$	76 nm
t_{poly}	32 nm

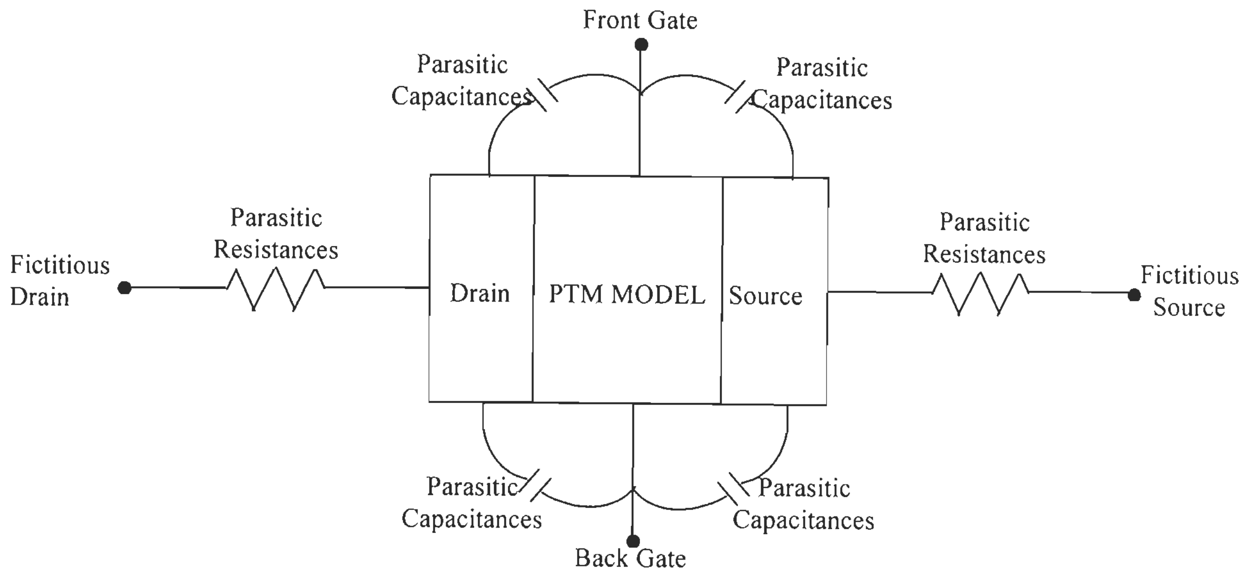
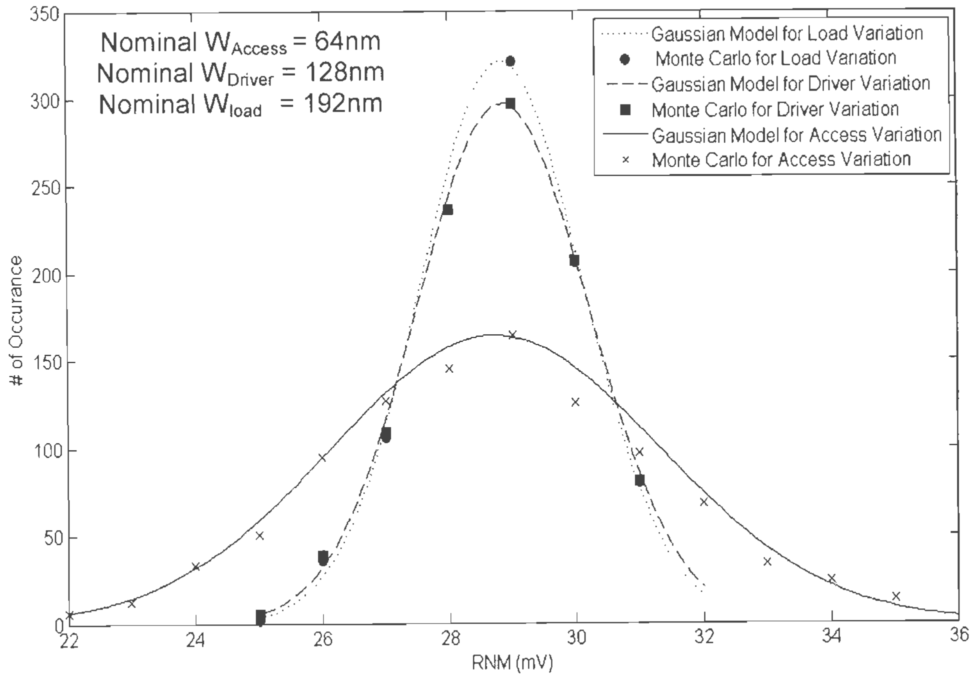
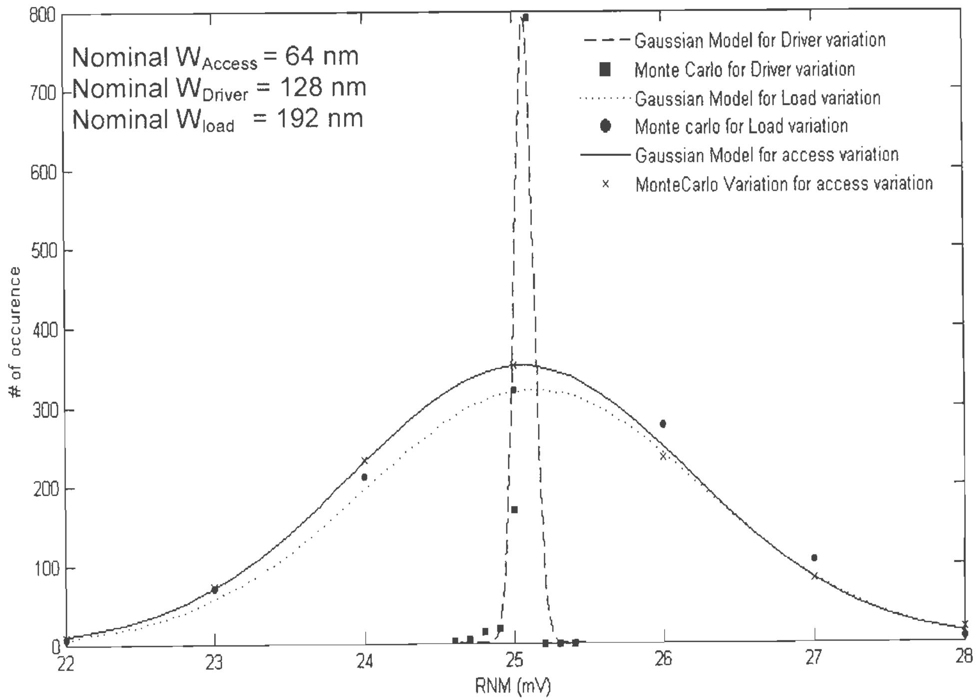


Figure 6.11 Underlapped FinFET derived from PTM model

In our simulations, it was observed that the SNM was relatively insensitive to variations in widths of driver and load FinFET's for both the PTM model and the modified underlapped. Figures 6.12.a and b show the Monte Carlo results for RNM of PTM based FinFET and underlapped FinFET respectively. It is evident that both the designs are most susceptible to variations in width of access FinFET as the graphs show greatest variation around the nominal value. The mean value of RNM for the PTM FinFET model based SRAM is however higher than that of the underlapped FinFET model for all the cases. This is primarily due to the fact that because of the introduction of the series resistance, the voltage after the channel to the source region gradually goes to zero owing to the ohmic drop across the extension region. Thus in case of RNM, the voltage at the storing '0' logic is not zero but infact has some nonzero value. This voltage offsets the RNM as lesser noise voltage would be able to flip the state of the cell during read cycle now. Consequently the RNM decreases.



(Fig 6.12.a)



(Fig. 6.12.b)

Figure 6.12 Monte Carlo results for variation of RNM with load, driver and access FinFET widths for (a) PTM model (b) Underlapped model (with fin extension regions)

Table 6.4 summarizes the mean and standard deviation of RNM for the Monte Carlo simulations with varying widths of driver, load and access FinFET's. An important observation that can be made is that the sigma value is lesser for the variation corresponding to FinFET having larger nominal value of width. This presents a new design challenge as a new tradeoff has been identified. This line of reasoning is seconded by the fact that the deviation is maximum for the access variation which infact has the least width amongst the three FinFET's. Another interesting observation is that the deviation for the underlapped FinFET case is lesser in all the three cases. This is attributed to the fact that the relative impact of FinFET width variation has been toned down with the introduction of the series resistance due to the fin extension regions. The relative change in drain current is now lesser and hence the relative impact on the metric is also lesser.

Table 6.4 Mean and Standard Deviation values of RNM with variation in FinFET widths

		Driver	Load	Access
RNM with PTM Model (mV)	Mean	28.8461	28.8394	28.7201
	Std. Dev.	1.3389	1.2505	2.5833
RNM with Underlapped Model (mV)	Mean	25.1167	25.0707	25.046
	Std. Dev.	1.0674	0.0605	1.1123

Similarly Figures 6.13.a and b show the results of process variations for WNM with the FinFET widths. It is observed that while RNM was more sensitive to driver FinFET width variation, WNM is more sensitive to load FinFET width variation. However as expected WNM is most sensitive to variation in access width because of its minimum size. The WNM is found to decrease in the underlapped device. This is because of the resistive drop across the load FinFET such that the effective voltage

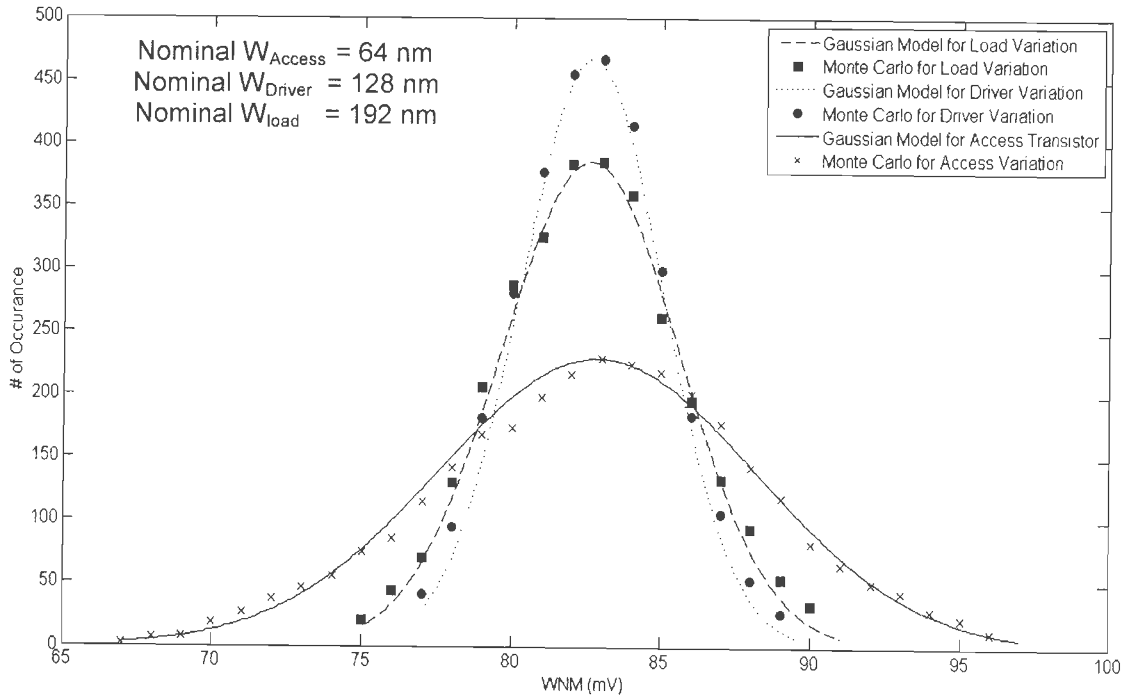
value for logic '1' is less than 0.8V. This is equivalent to scaling of V_D which results in decrease of WNM. The sigma and the mean values of the WNM are compiled in Table 6.5.

Table 6.5 Mean and Standard Deviation value of WNM with variation in FinFET widths

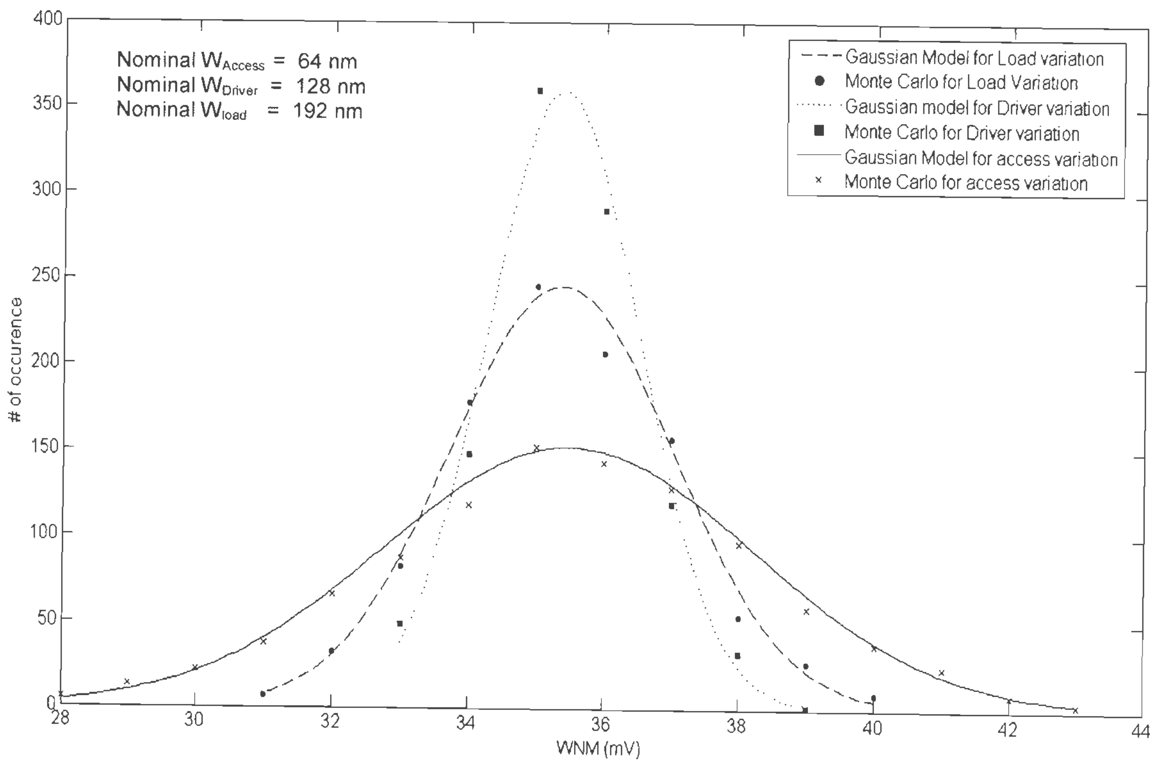
		Driver	Load	Access
WNM PTM model (mV)	Mean	82.6377	82.6057	82.8486
	Std. Dev.	2.3682	2.9959	5.3513
WNM Underlapped Model (mV)	Mean	35.3719	35.3648	35.4785
	Std. Dev.	1.1045	1.6279	2.7287

In case of FinFET based SRAM array, most of the cells are in idle state for a large portion of operation period. Hence static power consumption contributes to majority of the power dissipation. Figure 6.14 shows the dependence of static power with temperature for overlapped and underlapped FinFET based SRAM cell respectively. Since subthreshold current is the dominant source of leakage for FinFETs and it increases exponentially with temperature, the static power also increases exponentially.

As the temperature increases, the leakage current increases exponentially and causes reduction in the I_{on}/I_{off} ratio. This decreases the sub threshold slope and hence the voltage swing. As a result, the SNM and RNM of the FinFET SRAM cell decrease. As the voltage swing decreases, it becomes easier to flip the voltage at the nodes. Hence the amount of voltage required to cause write failure increases resulting in increase in WNM of the cell. Figure 6.15 shows the variation of SNM, RNM and WNM with increase in on-chip temperature for the PTM model of FinFET device.



(Fig. 6.13.a)



(Fig. 6.13.b)

Figure 6.13 Monte Carlo results for variation of WNM with load, driver and access FinFETs widths for (a) PTM model (b) Underlapped model (with fin extension regions)

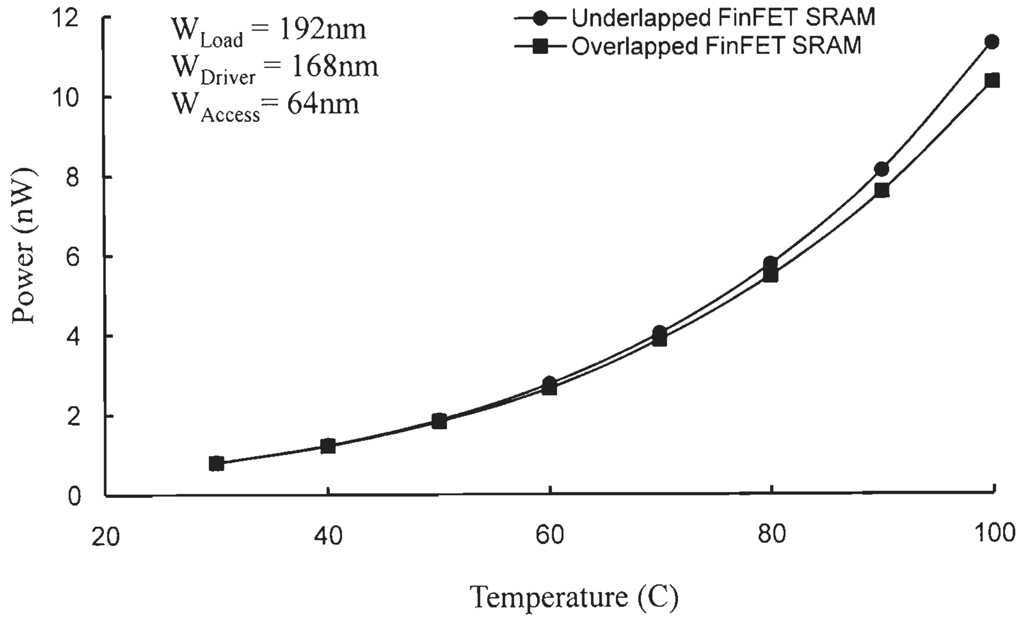


Figure 6.14 Effect of Temperature Variation on Static Power for PTM FinFET model and Underlapped FinFET model SRAM

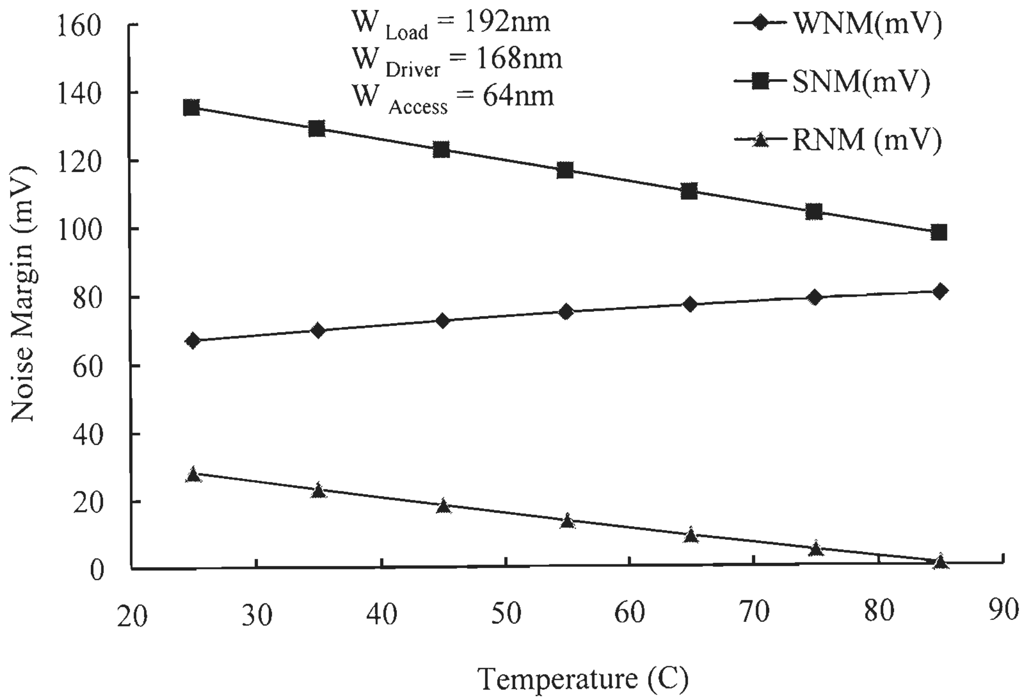


Figure 6.15 Effect of Temperature Variation on Static Noise Margin, Read Noise Margin and Write Noise Margin for PTM FinFET model

6.8 Conclusion

In this chapter, we have analyzed different tradeoffs involved in the design of FinFET based SRAM and optimized the performance of the cell for robustness. The analysis of SNM, RNM, WNM and static power variation with width of access, load and driver have been carried out. Further, the effect of process variation on the SRAM cell performance was analyzed using Monte Carlo simulation on HSPICE. The performance of a 6T FinFET based SRAM cell was analyzed using HSPICE CAD tool. Two structures of the FinFET viz. the standard PTM model and an underlapped FinFET have been used for the simulations. It was identified that while the relative levels of the noise margins were lower for the underlapped case, the standard deviation was considerably lower too. It was also found that smaller FinFET widths give rise to larger deviations than larger ones. Thus in future FinFET SRAM based on minimum FinFET width, would be prone to process variations. The temperature dependence of noise margins and static power was also observed for FinFET based SRAM. While SNM and RNM decreased with increasing temperature, WNM increased. Since the stability of the FinFET based SRAM cell in the idle state is the most important metric, temperature effects have to be accounted for in design of memory circuits.

CONCLUSION AND FURTHER SCOPE

7.1 Conclusion

This thesis addresses FinFET device physics, modeling, design issues of nanoscale FinFET at quantum levels and Double Gate FinFET based nanoscale SRAM design. The FinFET device structure studied have scaled channel lengths of 32 nm. To accomplish the objectives, analytical modeling and TCAD Sentaurus simulations have also been carried out. The fundamental physical equations that were solved which dictates the electrostatics in the devices and describing the transport and distribution of carriers in the FinFET device. Accurate field dependent mobility modeling for FinFET device has also been carried out using semi-empirical approaches.

As the dimensions of transistors are shrunk, short channel effects (SCEs) become predominant which tend to degrade the performance of the device and enhance the leakage currents. Alternative device structures would be required in order to ward off the SCEs without compromising on the performance and capabilities of the device. Self aligned Double Gate FinFET is one of the alternative device structures which meet the above criteria. FinFET have many advantage over the bulk MOSFET, such as FinFET developed with a process (fabrication) flow similar to conventional SOI CMOS process where as DGMOSFET has complex fabrication process. FinFET has large packaging density compared to other DG MOSFET structures.

The first stage of the work focused on analytical modeling of FinFET structures. Attempt has been made to get the potential profile in a nanoscale double gate FinFET device. Two dimensional potential modeling has been carried out for intrinsic doped double gate FinFET device under appropriate boundary conditions which are governed by the physics of the device. The variation of potential from gate to gate is reported. The key issues related to device parameters and structure is also discussed. The detailed study of threshold voltage has also been carried out. Variation of threshold voltage with various process parameters has been presented for our proposed device. Further, source/drain parasitic and total resistance modeling has also been carried out. For validation of our model, results ware compared and contrasted with reported experimental and simulated results. The results obtained on the basis of our model were found to be a close match with the reported results thus ensuring the accuracy of the model developed.

In the second stage of work, the analytical modeling to evaluate quantum mechanical inversion charge, field dependent mobility and drain current have been carried out. Analytical modeling of FinFET structure has been carried out in this chapter to evaluate the various characteristics using extensive quantum mechanical simulations. The results obtained on the basis of our analytical model have been compared and contrasted with reported experimental results and TCAD Sentaurus simulation. There is relatively good match between the results, which validates our analytical modeling approach.

In the third stage of work, analytical modeling and estimation of various leakage currents associated with FinFET device have been carried out. Various types of leakage currents are associated with FinFET device such as subthreshold leakage current and gate to channel leakage current. Subthreshold swing factor was also

evaluated for the FinFET device. It is seen from our study that subthreshold swing factor increases below effective gate length of 30 nm. Our analysis shows that use of FinFET device with intrinsic channel doing reduces leakage currents. We have considered the effect of temperature variation on the subthreshold leakage currents. As the temperature increases the subthreshold leakage current also increases. The results obtained through our analytical model are compared with the reported numerical and experimental results. A close match between our proposed analytical model and reported results validate our approach. Further, the analysis shows that FinFET device is one of the emerging devices to get optimized leakage currents to reduce the power dissipation.

The final stage of the work, analysis of double gate FinFET based 6T SRAM cell has been carried out at 32 nm technology. FinFET based SRAM cell has been designed using HSPICE simulator. The performance metric of FinFET based SRAM cell, such as Static Noise Margin (SNM), Read Noise Margin (RNM), Write Noise Margin (WNM), static power variation have been analyzed. Further, the effect of process variation on the SRAM cell performance was analyzed using Monte Carlo simulation on HSPICE. The performance of a 6T FinFET based SRAM cell was analyzed using HSPICE CAD tool. Two structures of the FinFET viz. the standard PTM model and an underlapped FinFET have been used for the simulations. It was identified that while the relative levels of the noise margins were lower for the underlapped case, the standard deviation was considerably lower too. It was also found that smaller FinFET widths give rise to larger deviations than larger ones. Thus in future FinFET SRAM based on minimum FinFET width, would be prone to process variations. The effect of temperature variation and process variation on FinFET SRAM cell has been also analyzed. It has been analyzed in our study that as

the temperature increases the power increases. We also analyzed the effect of temperature on WNM, RNM and SNM. The results obtained would be useful to device design and for fabricating future nanoscale devices and circuits.

7.2 FUTURE WORK

No work is complete as knowledge is infinite. To go further, we briefly point out some directions in which we think further research should be carried on.

1. The overlapping of source and drain regions with the channel regions has been ignored. This effect can substantially change the various characteristics of the device.
2. In this thesis work, two dimensional analytical modeling has carried out. It may be appreciated that a clear picture of the device functionality is achievable using three dimensional modeling approach. This might be carried out in future. In this regard, it is felt that using 3D approach may increase the accuracy of the model but at the cost of excessive computational time. So proper optimization of the proposed algorithm in 3D domain should be done in order to optimize the computational time.
3. We have analyzed FinFET device structure with single Fin. Multi-Fin FinFET device can be used to enhance the driving capability of the device. However the fabrication techniques required to meet such stringent guidelines would be an issue which can be looked into in future.

4. The different spacer materials can change the potential modeling and hence various leakage components estimation is expected to change in FinFET device. This might be a good area of further research.
5. This work can be extended to design a robust SRAM cell in nanometer regime with reduced cell failure probability and under the process variation effects.
6. We have not worked for the peripheral circuit design such as sense amplifier, decoder etc. These peripheral circuits are required to access the data from SRAM cell. The study of these circuits using nanoscale FinFET models developed here can be taken in future.

Appendix: Physical Constants and Device Parameters

Description	Symbol	Value and Unit
Electrical Charge	q	1.6×10^{-19} C
Temperature	T	300 K
Boltzmann's Constant	k	1.38×10^{-23} J/K
Vacuum Permittivity	ε_o	8.85×10^{-12} F/m
Silicon Permittivity	ε_{si}	1.04×10^{-10} F/m
Oxide Permittivity	ε_{ox}	3.45×10^{-11} F/m
Planck's Constant	h	6.63×10^{-34} J-s
Thermal Voltage (T = 300 K)	kT/q	0.0259 V
Angstrom	A^o	$1\ A^o = 10^{-10} m$
Electron Volt	eV	1 eV = 1.6×10^{-19} J
Electron Mobility	μ_n	0.1350 $m^2/V.s$
Hole Mobility	μ_p	0.0480 $m^2/V.s$
Free Electron Mass	m_o	9.1×10^{-31} kg
Electrons Effective Mass	(m^*/m_o)	$m_l^* = 0.98$, $m_t^* = 0.19$
Holes Effective Mass	(m^*/m_o)	$m_{lh}^* = 0.16$, $m_{hh}^* = 0.49$
Mass of Electron in SiO_2	m_{SiO_2}	0.6 m_o
Mass of Hole in SiO_2	m_p	0.98 m_o
Bandgap of Si	$E_{g,Si}$	1.12 eV
Bandgap of SiO_2	$E_{g\,SiO_2}$	$\approx$ 9 eV

Bandgap of Si_3N_4	$E_{gSi_3N_4}$	4.7 eV
Dielectric Constant of SiO_2	k_{SiO_2}	3.9
Dielectric Constant of Si_3N_4	$k_{Si_3N_4}$	7.5
Insulator Thickness	t_{ins}	1 nm and 1.2 nm
Channel Doping Density	n_i	1.45×10^{16} m^{-3}
Fermi Energy Level of Metal	E_{max}	4.4 eV
Conduction Band of n^+ Drain	E_{min}	4.05 eV

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List of Publications

Based upon the research work carried out, following papers are published/in press/accepted/under review/communicated for publications to various peer reviewed International Journals and Conferences.

International Journals:

1. Balwinder Raj, S. K.Vishvakarma, A. K. Saxena and S. Dasgupta, "Analytical Modeling of Nanoscale Double Gate FinFET Device" , *International Journal of Intelligent Electronics System*, vol. 1, pp. 66-71, 2007.
2. Balwinder Raj, A. K. Saxena and S. Dasgupta, "A Compact Drain Current and Threshold Voltage Quantum Mechanical Analytical Modeling for FinFETs, " *Journal of Nanoelectronics and Optoelectronics (JNO), American Scientific Publishers (ASP), USA*, vol. 3, no. 2, pp. 163-170, 2008.
3. Balwinder Raj, A. K. Saxena and S. Dasgupta, "Analytical Modeling for the Estimation of Leakage Current and Subthreshold Swing Factor of Nanoscale Double Gate FinFET Device, " *Microelectronics International, UK,* vol. 26, no. 1, pp. 53-63, 2009.
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5. Balwinder Raj, Jatin Mitra, Deepak Kumar Bihani, Rangharajan V, A.K. Saxena and S. Dasgupta "Analysis of Noise Margin, Power and Process Variation for 32 nm

FinFET Based 6T SRAM Cell", in *Journal of Computer (JCP), Academy Publisher, Finland*, vol 5, issue 6, pp. 1-7, 2010.

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13. Balwinder Raj, A. K. Saxena and S. Dasgupta, "Quantum Mechanical Analytical Drain Current Modeling and Simulation for Double Gate FinFET Device using Quasi Fermi Potential Approach," *10th International Symposium on Quality Electronics Design (ISQED-09),* San Jose, CA, USA, March 16-18, 2009.
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15. Balwinder Raj, S. K.Vishvakarma, A. K. Saxena and S. Dasgupta , "Design of Fin-FET for future Nanosacle Technology," *National Conference on Nanoscale Devices and System,* Muthayammal Enginnering College Rasipuram, Tamilnadu, India, pp.24-26, 30-31, March, 2007.
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