GROWTH AND STUDIES OF INSULATING FILMS FOR SILICON DEVICES

A THESIS

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By

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **'GROWTH AND STUDIES OF INSULATING FILMS FOR SILICON DEVICES'** in fulfilment of the requirement for the award of the Degree of Doctor of Philosophy, submitted in the Department of ELECTRONICS AND COMPUTER ENGINEERING of the University is an authentic record of my own work carried out during a period from Jul. 1979 to Oct. 1988 under the supervision of Dr. RAGHUVIR SINGH, Professor, Department of Electrical Engineering, College of Technology, Malla, University of Aden, Aden (P.D.R.Y.) and Dr. R.P. AGARWAL, Professor, Department of Electronics and Computer Engineering, University of Roorkee, Roorkee, INDIA.

The matter embodied in this thesis has not been submitted by me for the award of any other degree.

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ABSTRACT

In recent years the growth and or deposition of insulating films on the surface of a semiconductor material has received considerable attention as it is used for passivation, masking, isolation, dielectric purposes (gate dielectric) etc. Quality of the insulating films govern the performance of the device and to a some extent the packing density in integrated circuits. Silicon is by far the most widely used semiconductor material for fabrication of discrete, integrated circuits, LSI, VLSI, etc. due to its well established technology and its native oxide possess the outstanding qualities. Various techniques have been developed for the growth of oxide films on silicon such as thermal oxidation, plasma anodization and wet anodization. Thermal oxidation of silicon is the most commonly used technique for the growth of oxide film, due to superior $Si-SiO_2$ interface properties. However temperature involved in oxidation generates stacking faults and dislocations; produces stress and wafer warpage; and changes the impurity profiles previously formed in the substrate. With the advent of VLSI's it was realised that for further increasing the packing density on the single chip some low temperature technique should be evolved for the growth of oxide films so that the high temperature effects may be minimized.

In order to avoid the undesired effects of thermal oxidation and the encouraging results of anodic oxide films on GaAs, there is a renewed interest in growing thin insulating films on silicon by anodic oxidation. Present thesis deals with the growth and or deposition of insulating films on silicon at low temperatures. Due to the ease in fabrication, simplicity of structure and the sensitivity of the C-V characteristics to physical properties, MOS structures were used to study the influence of process parameters on the properties of insulating films. The material used in the investigation was n-type epitaxially grown silicon wafer of $\langle 111 \rangle$ orientation having resistivity of 6 to 8 ohm-cm. The resistivity of the substrate was 0.005 ohm-cm. A stringent cleaning procedure based on hydrogen peroxide solutions was used for surface preparation of samples. The electrolytic bath used for anodization was freshly prepared 0.04N KNO_3 solution in Ethylene-Glycol. Anodization parameters were optimised experimentally with a view to grow thin compact SiO_2 layers for applications in integrated circuit technology. The anodization was carried out at constant current density followed by a constant voltage mode. Anodically oxidised samples were annealed in H_2 atmosphere, ohmic contacts were made at the back of anodized samples. The MOS structure was completed by evaporating ultrapure Al through a metal mask over the grown oxide film in a vacuum coating unit. The suitability

of the grown SiO_2 film for devices was analysed by studying C-V, G-V and I-V curves. Interfacial and electrical properties such as surface state density, dielectric breakdown strength and dielectric constant were determined to assess the quality of grown oxide film. Experimental results reveal that the quality of anodically grown film of the order of 300 A° is comparable with that of thermally grown oxide films. It was also noted that the dielectric properties of the grown films deteriorates as the film thickness increases.

During investigations it was observed that the anodization of silicon samples at higher current density in an electrolytic bath of KNO_3 in Ethylene-Glycol mixed with small quality of water at elevated temperature results in porous films. The characteristics of such anodically grown films vary with the humidity of the surrounding environment. The capacitance of the such MOS structure was measured as a function of relative humidity. Results show that the porous SiO_2 films can be used to realise humidity sensors. The proposed sensors may be suitable to realise I.C. sensors as it can be fabricated on silicon I.C. chips as an integral part of the circuit.

Insulating Al_2O_3 films were also deposited on silicon samples and on anodically grown layers by reactive evaporation of Aluminium to fabricate and study the MAS and MAOS structures. Aluminium oxide has higher dielectric constant,

higher density and large impermeability for impurity diffusion, further Al_2O_3 films gives a positive values of threshold voltage and stops fast diffusing alkali ions. Evaporation parameters and the annealing temperature were optimized for the fabrication of MAS and MAOS samples. From the measurements and results it was concluded that Al_2O_3 film deposited by reactive evaporation method is useful for use as gate insulator in MOS devices alone or as an auxiliary dielectric with SiO_2.

Essentially the anodization and reactive evaporation technique here used is a low temperature fabrication technique and may be suitable in VLSI and MOS technology. With the scaling down of device dimensions the use of thin SiO_2 films with high dielectric breakdown strength are finding importance in MOS technology. Therefore anodically grown SiO_2 films of thickness of the order of 300 A° is a promising substitute of the thermally grown films for VLSI and MOS technology.

CONTENTS

CHAPTER - I

INTRODUCTION AND STATEMENT OF THE PROBLEM

1.1 INTRODUCTION

The integrated circuit complexity has advanced from small scale integration (SSI) to very large scale integration (VLSI), which has 10^5 or more components per chip. Present improvements on chip integration complexity are being achieved by scaling down lateral and vertical dimensions of individual devices. The shrinkage of lateral dimensions will continue to be achieved by improvements in photo-lithography. The reduction of vertical dimensions requires that the processing temperature, such as deposition of growth of oxide films on solicon substrate used to fabricate chips be lowered [1].

Silicon is by far the most widely used semiconductor material for fabricating discrete and integrated electronic devices and circuits as its processing technology is well established and the oxide of silicon possesses the outstanding qualities for applications. The growth or deposition of insulating films over silicon is necessary during the entire process of fabricating modern integrated circuits. The oxide layers are used for various purposes such as:

(i) For surface passivation: Passivation is accomplished

by forming a thin insulating layer on the semiconductor surface. It minimises the electrical activity of the device surface, and protects the surface from environmental contamination. Thus passivation results in a marked improvement of device performance, stability, and uniformity of characteristics from device to device.

(ii) The oxide acts as a barrier (mask) against the diffusion of impurities into the silicon underneath thus, by cutting windows into the oxide film, impurities can be diffused into the silicon through these windows.

(iii) The oxide provides insulation between the metallization pattern interconnecting devices in the circuit and the silicon substrate.

(iv) The oxide insulates the gate from the silicon in field effect devices.

(v) The oxide acts as a dielectric layer in capacitors and MOS Sensors.

The oxide films in general should have the following characteristics:

(i) Ideal interface (i.e. virtually zero surface state density) on an interface characterized by an ideal

C-V curve shifted along the voltage axis to a predetermined value.

(ii) Good insulating properties, i.e. high breakdown strength, high dielectric constant, low dielectric losses and low leakage current.

(iii) Resistant to ionic motion at elevated temperature and/or high fields.

(iv) High resistance to atmospheric effects.

(v) High resistance to radiation.

The condition for a perfect-interface between semiconductor and insulating oxide films are as follows:

(a) Strong chemical bonds between the semiconductor and the oxide layers, preventing the existence of dangling bonds.

(b) No impurities in the interface.

(c) The oxide layer should be chemically stable to serve as a passivating film for the interface.

1.2 TECHNIQUES USED TO FORM SILICON DIOXIDE FILMS ON SILICON

The techniques used to form silicon dioxide films

on silicon fall into two broad categories.

(i) The deposition process

(ii) The native oxide Growth process.

Both these processes are briefly described in the following two sub-sections.

1.2.1 THE DEPOSITION PROCESS

Silicon dioxide can be deposited by various vapour phase chemical reactions. The simplest method of vapour phase deposition is oxidation of silane SiH_4, by oxygen at low temperatures at about 500°C [2-4]. The chemical reactions for phosphorus - doped oxides are

$$SiH_4 + O_2 \longrightarrow SiO_2 + 2H_2$$

$$4PH_3 + 5O_2 \longrightarrow 2P_2O_5 + 6H_2$$

The deposition can be carried out at atmospheric pressure in a continuous reactor (Fig. 1.1b) or at reduced pressure in an LPCVD reactor (Fig. 1.1a). The main advantage of Silane-Oxygen reaction is low deposition temperature, which allows films to be deposited over aluminium metallization. Consequently, these films can be used for passivation coatings over the final device and for insulation between aluminium levels. The main disadvantages of Silane - -oxygen

reaction is poor step coverage and particles caused by loosely adhering deposits on the reactor walls.

Silicon dioxide is also deposited at 650 to 750°C in an LPCVD by decomposing tetraethoxysilane, $Si(OC_2H_5)_4$ [5,6]. The over all reaction is

$$Si\ (OC_2H_5)_4 \longrightarrow SiO_2 + \text{by products}$$

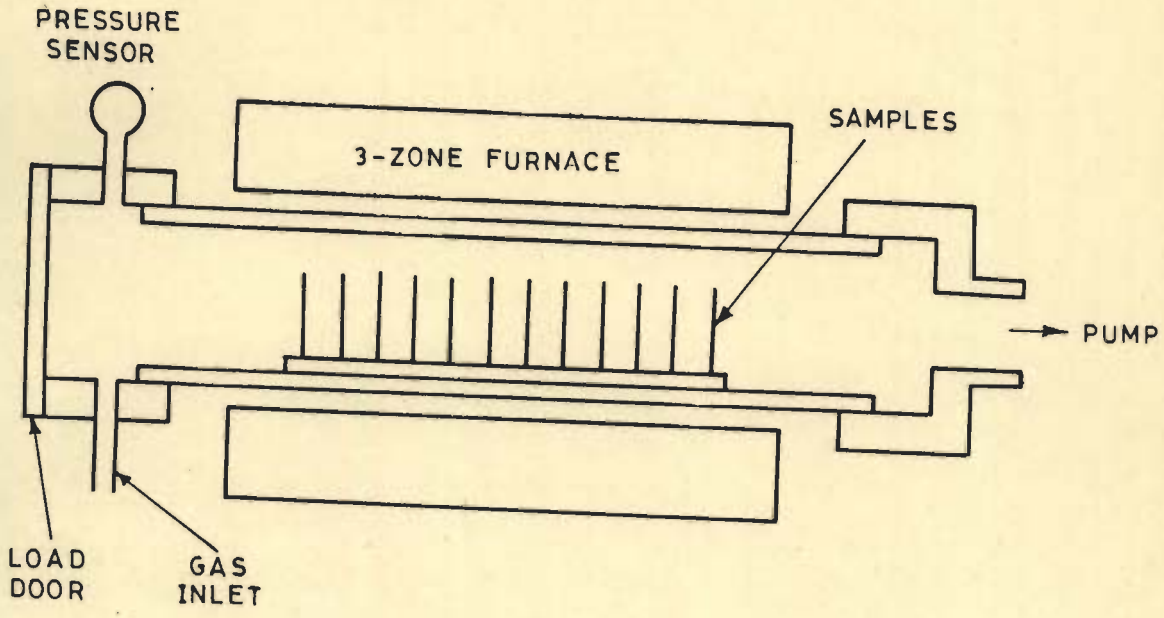
where the by-products are a Complex mixture of organic and organosilicon compounds. The decomposition of $Si(OC_2H_5)_4$ is useful for depositing insulators over polysilicon gates. The advantages of this method are excellent uniformity, conformal step coverage. The disadvantages are the high-temperature and liquid source requirements.

Silicon dioxide is also deposited at temperatures near 900°C and at reduced pressure by reacting dichlorosilane with nitrous oxide [2,7,8].

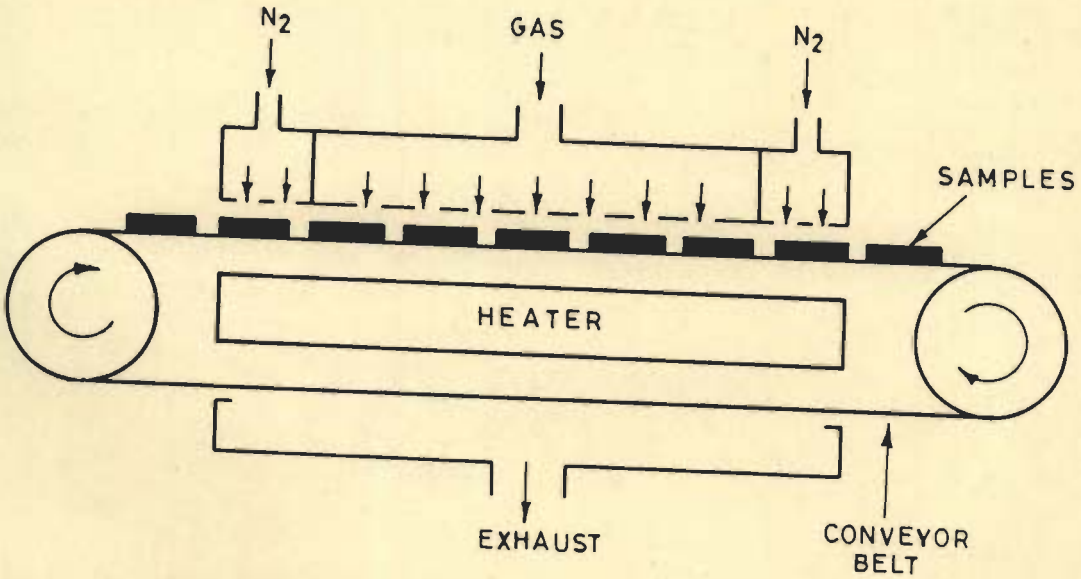
$$SiCl_2H_2 + 2N_2O \longrightarrow SiO_2 + 2N_2 + 2HCl$$

This process, is used to deposit insulating layers over polysilicon; however, the oxide frequently contains small amounts of chlorine which may react with the polysilicon or cause film cracking [8].

Other deposition methods for dielectric, such as vacuum evaporation and reactive sputtering are not widely



(a) Reduced Pressure Reactor



(b) Conveyor belt atmospheric pressure reactor

FIG. 1·1: CHEMICAL VAPOUR DEPOSITION REACTORS

used for VLSI processing [9]. The major problems include nonuniform depositions over many wafers, poor step coverage, and low throughput. The structure of evaporated and sputtered oxides is characterized by the composition as SiO_x where the value of x varies from one to two depending upon the deposition conditions.

1.2.2 THE NATIVE OXIDE GROWTH PROCESS

The native oxide of silicon may be grown in two ways:

(i) By thermal oxidation

(ii) By Anodic oxidation.

1.2.3 THERMAL OXIDATION [10 - 26]

1.2.3.1 DESCRIPTION OF THERMAL OXIDATION PROCESS METHODS

The term thermal oxides refers to those oxides formed from a thermally activated reaction of silicon with dry oxygen, wet oxygen, steam, and high - pressure steam. The first three methods are conducted in an open-tube reactor where the silicon wafers are heated to a temperature in the range of 900°C to 1200°C in a steam of water vapour, oxygen, or a mixture of the two oxidants.

A wet - oxygen source is obtained by bubbling oxygen through a constant - temperature, high - purity water

bath whose temperatur determines the partial pressure of water vapour in the gas stream for a specified oxygen flow rate.

For steam oxidation, the temperature of the water bath generating the steam provides a measure of the partial pressure and flow rate. Live steam yields poor grades of oxide because of the etching action of excess water. Properties of the various types of oxides grown by thermal oxidation are shown in Table I [27].

Table - I

Oxide Properties

Type	Density (gm/cm^3)	Resistivity (ohm - cm)	Dielectric strength 10^6 V/cm
Dry O_2	2.24 - 2.27	$3x10^{15}$-$2x10^{16}$	2
Wet O_2	2.18 - 2.21		
Steam (1 atm)	2.0 - 2.20	10^{15} - 10^{17}	6.8 - 9.0

The apparatus for the high pressure steam oxidation of silicon consists of a tight constant - volume enclosure, usually made of metal, into which a predetermined quantity of high purity water is introduced along with the silicon. The inside of the enclosure is often lined with gold or

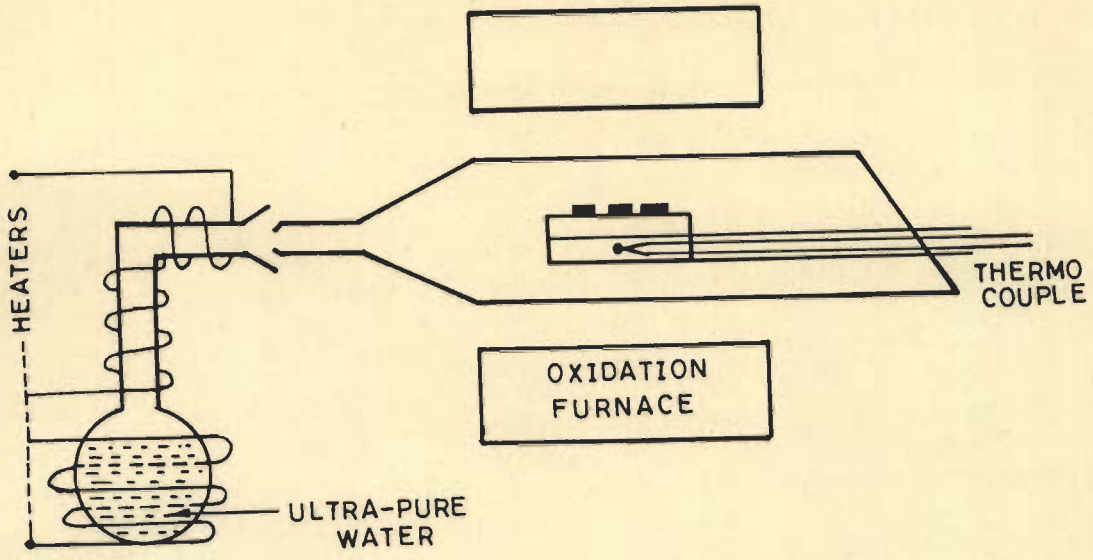


FIG. 1·2 : STEAM OXIDATION APPARATUS

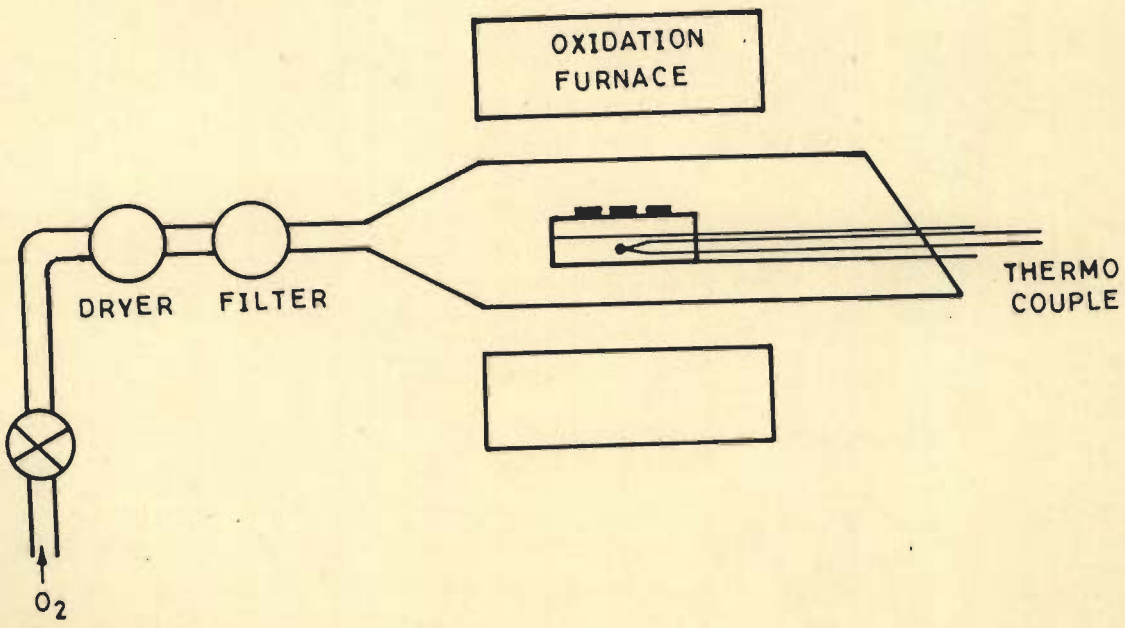


FIG.1·3 : DRY OXYGEN OXIDATION APPARATUS

other inert material to prevent undesired reactions between the water and the walls of the chamber. The entire system is heated to the oxidation temperature. High-pressure oxidation of silicon is particularly attractive, because thermal oxide layers can grow at relatively low temperatures comparable to typical high temp., 1-atm conditions. At 10-atm pressure and 750°C, a 300 A°-thick oxide can be grown in 30 min, the time, temperature, and pressure can be changed to vary the thickness. Such a technique has been applied to the growth of a thin gate oxide in the process to fabricate MOS dynamic RAM [28] and in the fabrication of MOS LSI [29]. In the oxidation at elevated pressure, several complications arise such as: Continuous Variations in pressure during pressurization, Small temperature variations that occur during pressurization and during the early part of the oxidation at full pressure, varying partial pressure of steam during depressurization, and grown film thickness variations from run to run and across a wafer.

1.2.3.2 DEFECTS INDUCED BY THERMAL OXIDATION

In integrated circuit technology there are following important effects of thermal oxidation of silicon on bulk electrical properties of the silicon substrate and grown oxide films.

(i) Thermal Oxidation - Induced Stacking Faults

(ii) Redistribution of Dopants at interface

(iii) Thermal oxidation induced oxide stresses.

1.2.3.2 (i) THERMAL OXIDATION INDUCED STACKING FAULTS

The thermal oxidation process can induce stacking faults that extend from the silicon surface into the interior of the silicon [30-32]. These planar faults are structural defects in the silicon lattice consisting of an extra plane of silicon atoms bounded along the edges by dislocations. The dislocations are the transition between the extra plane of silicon atoms and the normal silicon lattice structure. Stacking faults are important in integrated circuit technology because they can be electrically active may enhance junction leakage currents and reduce minority carrier life time. The growth of oxidation-induced stacking faults is a strong function of substrate orientation, conductivity type, and defects present in nuclei. Observations show that the growth rate is greater for $\langle 100 \rangle$ then $\langle 111 \rangle$ substrates. Additionally, the density is greater for n-type conductivity than for p-type conductivity. The stacking fault length is a strong function of oxidation temperature [33].

1.2.3.2 (ii) DOPANT IMPURITY REDISTRIBUTION

Dopant impurities near the silicon surface will be redistributed during thermal oxidation [34]. Redistribution

of dopant impurities in the silicon is important both from the stand point of device characteristics and in the interpretation of measurements of interface trap properties and oxide fixed charge. When silicon in thermally oxidized, an interace is formed separating the silicon from the SiO_2. As oxidation proceeds this interface advances into the silicon. A doping impurity (initially present in the silicon) will redistribute at the interface until its chemical potential is the same on each side of the inteface. This redistribution may result in an abrupt change in impurity concentration across the interface. The ratio of the equilibrium concentration of the impurity (dopant) in silicon to that in SiO_2 at the interface is called the equilibrium segregation coefficient. Two additional factors that influence the redistribution process are the diffusivity of the impurity in the oxide and the rate at which the interface moves with respect to the diffusion rate [35]. The segregation coefficient, as defined above increases with increasing temperature, and is orientation dependent with values for $\langle 100 \rangle$ orientation being greater than $\langle 111 \rangle$ orientation. Reported coefficients [36-38] are generally 0.1 to approximately 1.0 over the temperature range 850 to 1200°C.

1.2.3.2 (iii) THERMAL OXIDATION INDUCED OXIDE STRESSES

Stress is another effect of oxidation on silicon. Growth of an oxide film on silicon at high temperatures

puts the silicon under stress at room temperature because of the mismatch in the coefficient of thermal expansion between silicon dioxide and silicon. This stress does not directly affect the electrical properties of most devices used in integrated circuits, but if the silicon wafer is two thin, the mismatch stress can cause the wafer to warp or bow, film cracking and defect formation in the underlying silicon. Room temperature measurements following thermal oxidation of silicon show Sio_2 to be in a state of compression on the surface. Stress values of 3×10^9 dynes/cm^2 are reported [39] with the stress attributed to the difference in thermal expansion for Si and SiO_2. During device processing, windows are out into the oxide resulting in a complex stress distribution. At these discontinuities exceedingly high stress level can occur. In IC fabrication, several lithography processes are repeated, so alignment among the patterns is very important when they are done on one over another. In forming patterns 2 μm or less, no more than 0.5 μm misalignment can be permitted [40]. Possible cause of the misalignment are (i) A difference in thermal expansion coefficients between silicon and silicon dioxide (ii) Shrinkage or expansion of the silicon wafer by thermal oxidation (iii) deformation of the silicon wafer or the mask plate by stress when they are brought into contact for printing.

1.2.4 ANODIC OXIDATION

1.2.4.1 PLASMA ANODIZATION [41-43]

Plasma anodization is a vacuum process usually carried out in a pure oxygen discharge. The plasma is produced either by a high - frequency discharge or a DC electron source. Placing the wafer in a uniform density region of the plasma and biasing it positively below the plasma potential allows it to collect active charged oxygen species. The growth rate of the oxide typically increases with increasing substrate temperature, plasma density, and substrate dopant concentration. In the plasma anodization a high temperature (1000°C in H_2) annealing treatment is required to obtain interfacial electrical properties comparable to thermally grown oxide films. Thus the over all process is a high temperature one. Plasma grown oxides are not superior to thermally grown oxides, and both are high temperature processes, but the apparatus needed to plasma anodization is more expensive and require more skill to use than that for thermal oxidation. Therefore, plasma anodization is not used in silicon integrated circuit manufacture.

1.2.4.2 ANODIZATION IN A LIQUID ELECTROLYTE

In this process the silicon wafer is made the anode of an electrolytic-cell containing an electrolyte

with an oxygen bearing component, which does not dissolve silicon or its oxide, and a current is passed between the anode and an inert cathode such as platinum by applying a suitable voltage across them. An oxide film grows on the silicon surface as the current, which is predominantly electronic with a small ionic component, flows through the growing oxide layer under the applied electric field. Such a growth can be carried out at room temperature or even at temperature lower than the room temperature. The thickness of the grown oxide layer is directly proportional to the value of the forming voltage.

1.3 FUTURE TRENDS IN VLSI TECHNOLOGY

The total number of electronic circuit components per silicon chip increased from one in 1959 to 600,000 in eighties [44]. Although the rate of growth has slowed down in recent years because of difficulties in defining, designing and procesing complicated chips, a complexity of over 1 million devices per chip will be available before 1990 [9]. This increase is made possible primarily by the advancements in photolithography process of transferring geometric shapes on a mask to a wafer surface, resulting in a continuous decrease in the device dimension from over 10 microns in the early 1960's to one micron in the early 1980's. VLSI devices having very small dimensions require not only the precise lithography and pattern transfer

but also very shallow junctions. These conditions impose new requirements on the oxide film growth process. The major requirements are low processing temperature to prevent movement of the shallow junctions and low process-induced defects. One of the factors which affects the ultimate accuracy in the transfer of pattern on the wafer is the oxide thickness used in the photolithographic process. Thinner the oxide layer higher is the accuracy achieved in the pattern generation. With the scaling down of device dimensions, the use of thin SiO_2 films of the order to 100A° will soon become common in MOS technology [45].

The wet anodization technique, which is essentially a low, temperature technique for growing oxide films offers vast potential for manufacturing VLSI. The low-temperature processing suppresses defect formation and minimizes movement of previous diffusions.

1.4 STATEMENT OF THE PROBLEM

Literature survey shows that in sixties and senventies efforts were made to grow anodic-oxide films over silicon wafers under different conditions and their characteristics were studied. Due to the poor qualities of the grown films in comparison to that grown by thermal oxidation the wet anodization methods were rejected and not explored further. In order to avoid high temperature effects and the encouraging results of anodic oxide films on GaAs, there is a renewed

interest in growing insulating films on silicon by anodic oxidation. An understanding of silicon-silicon dioxide interface is necessary in order to fabricate highly reliable devices. Therefore it is proposed to grow the oxide layers on silicon by anodization technique and to study the interfacial properties of the $Si-SiO_2$ interfaces in detail. Anodization parameters were optimized to obtain the best interfacial properties suitable for the fabrication of IC's.

Here an electrolytic bath consisting of KNO_3 in ethylene glycol was standardised by conducting various experiments. This was done by growing oxide films on silicon in the anodic baths having different molarity of KNO_3 in ethylene glycol and then evaluating the quality of grown films by determining the interface state density and dielectric breakdown strength of the fabricated MOS samples. The effects of different anodization current densities and annealing temperature in H_2 atmosphere were studied to get the best results. For evaluating the electrical properties of grown films and their associated $Si-SiO_2$ interfaces MOS structures were formed on n-type $\langle 111 \rangle$ epitaxial silicon wafers. During investigations it was observed that under certain anodization conditions the anodically grown SiO_2 films become porous and humidity sensitive, therefore the use of these films for fabrication of MOS humidity sensor was also studied.

Metal - Aluminium oxide-silicon (MAS) and metal-Aluminium oxide Silicon dioxide-Silicon (MAOS) structures have also been the subject of extensive investigations. In this thesis MAS and MAOS structures are also investigated. For that Al_2O_3 films were deposited by evaporating high purity Al (99.999%) in a partial pressure of O_2. The reactive evaporation of Aluminium is also a low temperature process. In the MAOS structures silicon dioxide film is grown by anodic oxidation technique.

1.5 ORGANISATION OF THE THESIS

The present work consists of seven chapters. First chapter reviews various oxidation processes and the drawbacks of thermal oxidation of silicon. The second chapter presents the critical review of anodic oxidation of silicon reported so far. Chapter III deals with the fabrication of MOS samples by anodic oxidation technique, which includes the surface preparation of silicon wafers, anodization process and optimisation of anodization parameters, annealing of the samples, formation of ohmic contacts and Gate electrodes. The electrical properties of anodically grown films and the $Si-SiO_2$ interfaces are evaluated in chapter IV. In the V chapter fabrication of MAS, MAOS structures, their electrical and interfacial properties are described. For the fabrication of MAS structures 300A° Al_2O_3 film is deposited on silicon by reactive evaporation technique of aluminium, for the MAOS

structures 300 A° of SiO_2 layer is grown on silicon wafers by anodic oxidation technique and the composite structure is compelted by depositing 300 A° Al_2O_3 film on SiO_2 film by reactive evaporation technique. Chapter VI considers the fabrication and performance characteristics of humidity sensitive SiO_2 insulating films for MOS sensors. Humidity sensitive porous films are grown on the silicon by the anodic oxidation technique in an aqueous bath of KNO_3 and ethylene glycol at temperature 50°C and high anodization current density 30mA/cm². The last chapter VII is a concluding chapter in which conclusions are drawn on the basis of the results of IV, V and VI chapters, the scope for further work is also discussed. The APPENDIX A is devoted for the development and fabrication details of the Automatic C-V plotter and the micromanipulator developed in the laboratory.

CHAPTER - II

CRITICAL REVIEW OF THE SILICON WET ANODIZATION

The anodization technique had been mostly used for anodizing the metallic films in particular aluminium for making capacitors [46, 47]. Gunter - Schulze and Betz [48] were the first Scientists who used the anodization technique for growing dense oxide films on silicon by anodic oxidation in concentrated H_2SO_4.

In 1957 Schmidt and Michel [49] tried the production of dense oxide films on n- and p-type single crystalline $\langle 111 \rangle$ oriented silicon of resistivity of 2-5 ohm cm using three different electrolytes viz. (i) concentrated acids, (ii) Borate electrolytes (iii) 0.04N solution of potassium nitrate in N-methylacetamide at room temperature. KNO_3 was added in order to increase the conductivity of the electrolyte and in order to supply the oxygen for the anodic reaction. N-methylacetamide was used due to its high dielectric constant. In all the three above mentioned electrolytes the anodization was carried at constant current density of 4 ma/cm^2. It was reported that in concentrated acids (HNO_3) or (H_3PO_4) growth of the film does not take place beyond 160 volts, because of the large concentration of the acid anion. In ammonium borate a dense oxide of comparatively low resistivity is formed, porous oxides are formed

in oxilic acid or chromate solutions. The solution of KNO_3 in N-methylacetamide permits forming upto 350V. If anodization at constant current density is continued after the voltage has risen to 350 volts, the oxide breaks down, the voltage starts to oscillate without rising any further, while severe damage to the oxide results. If a silicon sample is held at a constant voltage of 300V for some time, forming thereafter can be continued upto 560V. At 560 volt bright sparks appear in the solution. Thus they succeeded in forming oxide layers as thick as 2200A° at 560 volts. However they pointed out that forming at constant voltage more than 300V induces structural changes in the oxide. The field during forming is of the order 2.6×10^7 V/cm corresponding to a thickness increment of about 3.8A°/V. The thickness of oxide films was measured by direct weighing of the smaple, by interference colours, and by capacitance measurements. The ionic current efficiency of film growth is very low. In methylacetamide it can be increased by addition, of chloride ions or by fluoride ions.

The anodic current is in the reverse direction for a barrier on n-type silicon, consequently, the rate of the anodic growth is limited by the supply of minority carriers, holes, to the Si-oxide interface. This fact was verified by conducting anodization experiments on n-type silicon in dark and under illumination. The curve taken under illumination of the wafer is similar to that on p-type silicon.

They also reported that during the anodization process heat is generated by power dissipation across the barrier in the silicon. The measurement indicated that the temperature at a distance of 3 miles from the front surface of silicon rose to approximately 65°C within 30 sec of anodization at a current density of 6 ma/cm², the bath temperature being 25°C.

In 1964 Schmidt et. al [50] reported the preparation of phosphorus doped anodic oxide films on silicon. They also suggested that these oxide films can be used as phosphorus diffusion sources during heat treatment. The anodization was carried out in a solution of 15 percent by volume of pyrophosphoric acid in tetrahydrofurfuryl alcohol, at a constant current density in the range between 3 and 5 mA/cm². The current densities below 2.5 mA/cm² lead to poor oxide quality and current densities above 5 mA/cm² were not used in order to avoid Joule heating of the solution. When the desired anodization voltage was reached, the operation was continued at a constant voltage for 30 minutes, this being sufficient time for the leakage current to decay to a small value and to become practically independent of further anodization at constant voltage. Anodizations were in general carried out in non-stirred solutions at room temperatures or slightly above room temperature. At 65°C the thickness of the oxide film per volt forming voltage increases noticeably, indicating the beginning

of porosity, temperature higher than 45°C were therefore avoided. The thickness/voltage increment was 5.81A°/V ± 5% for constant voltage operation, and 4.66A°/V ± 5% for constant current operation (3 mA/cm²).

In 1964 Duffeck et. al [51] used N-methylacetamide (NMA) + KNO_3 solutions and studied the effect of water in the anodizing solution on the grown oxide, using silicon and oxide weight analysis. The electrolysis products and reactions during anodization of silicon were examined. High purity single crystal silicon 1-2 ohm - cm p and n-type were used. Prior to anodization the silicon was etched in CP-6 (1: 5, HF: HNO_3) or CP-8 (6: 10, HF HNO_3), dipped in HF for several seconds, rinsed in deionized water and dried. The temperature of electrolyte was held as close to 35°C as possible. Oxide film thickness measurements vs net forming voltage at 5 mA/cm² and with 0.1 - 0.5% water in NMA showed the rate of growth of film as 5.3 A°/V from 100 to 425 volts. They investigated the effect of water concentration and current density onthe Si: O_2 ratio in the oxide and concluded that 0.5% to 3% water and current densities between 3 to 10 mA/cm² produced the most Stochiometric films.

In 1965 Duffeck et. al [52] used the reagent grade ethylene glycol and 0.04N KNO_3 as electrolyte to grow SiO_2 films and studied the characteristic of the grown

films. For pretreatments raw, lapped silicon wafers were chemically polished in CP-6 (1: 5, HF: HNO_3) or CP-8 (3: 5, HF: HNO_3), dipped in HF, rinsed in deionized (DI) water and dried. Chemically polished silicon wafers were also used, they were degreased in hot trichloroethylene and rinsed in the order, acetone, deionized water, HF (49%) for 20 sec., D.I. water and dried. the temp. of electrolyte was kept at 25° - 30°C. Anodizations were carried out at constant current with current densities ranging from 1 to 25 mA/cm². Anodization was terminated when the predetermined forming voltage was reached. The anodized wafers were rinsed in D.I. water, dried and evaluated. The thickness of films grown were measured by means of interference colour comparison to known standards. The refractive index of these films were measured. The experimental results shows that stoichiometric SiO_2 films canbe obtained on a reproducible basis. It is reported that the use of ethylene glycol as a solvent has the advantage of low cost, high purity, electrolyte solubility and good stability toward heat and electrolysis.

In 1966 R.Dreiner [53] anodized low resistivity (0.02 ohm-cm) $\langle 111 \rangle$ oriented, p-type silicon slices in a solution of 0.04N KNO_3 in ethylene glycol containing 2% water, and the dielectric behaviour of the system Si/Anodic/Sio_2/ electrolyte was studied. The samples were anodized at constant current to desired voltages. No constant voltage

phase followed. It was observed that the oxide started to peeloff from some areas of the substrate when low formation current densities were applied, but no such effect was observed with high current densities. Preliminary experiments indicated that the pretreatment of the substrate had an influence. The onset of peeling was delayed when the samples were chemically polished prior to formation. It was concluded that the thinner films were of better quality.

In 1967 Akos G.Revesz [54] oxidized silicon anodically using constant voltage method. The $Si-SiO_2$ interface was investigated with the MOS capacitance method. The primary purpose of this investigation was to compare anodic oxidation with the thermal one on the basis of MOS interface behaviour. It was shown that constant voltage oxidation under clean conditions in a nonaqueous electrolyte followed by a short time annealing in helium at high temperature results in an interface that is comparable with that obtained by thermal oxidation. Chemically polished 10 ohm-cm- p-type silicon of $\langle 111 \rangle$ and $\langle 100 \rangle$ orientations were used. The specimens were carefully cleaned and just before anodization were submerged in hydrofluoric acid and rinsed with distilled water. The electrolyte chosen was 0.04N Solution of KNO_3 in N-methylacetamide (NMA). Since it was known that this electrolyte is hygroscopic and the oxidation process is influenced by its water content, fresh electrolyte was

used for each oxidation. No attempt was made however to avoid water absorption during oxidation. The temperature during anodization was about 50°C. The cathode was a platinum sheet. The constant current density was varied from 5 to 10 mA/cm², the highest forming voltage was 300V, and the lowest current density obtained during the constant voltage mode was 0.04 mA/cm² in about 300 min. After oxidation the specimens were rinsed in water. Some specimens were than treated in hydrogen at 500°C for 15 min., or in helium at 800°C - 1000°C. The hydrogen treatment was done in a conventional vitreous silica tube furnace, whereas the helium annealing was performed in an air cooled silica tube with radio frequency (rf) heating. For MOS capacitance measurements with a mercury probe the specimens were provided with nickel back contacts. The differential capacitance of the MOS diode as function of bias was measured at 1 MHz with an automatic measuring apparatus. The density of surface states is determined by the anodization conditions. High values were obtained by constant current anodization. In the case of constant voltage anodization the surface state density generally decreases with the anodization time i.e., with the final oxidation rate. Constant voltage anodization to low final current densities followed by annealing in helium at elevated temperature can result in 2×10^{11} cm^{-2} surface density. The relatively high perfection of this interface is shown by the lack of interface

instability effects at 300°C under high field. Under these conditions the shift of the C-V curves is quite small and voltage symmetric.

In 1968 A.G.Revesz and K.H.Zaininger [55] observed that the oxidation of silicon can be performed electrolytically by applying a sufficient overvoltage in an electrolyte that does not dissolve the oxide. The most interesting feature of anodic oxidation of silicon is the very low oxidation efficiency i.e. 0.4 to 1.6%, corresponding to a current that is overwhelmingly electronic rather than ionic. This is quite in contrast to the anodization behaviour of, say, tantalum and aluminium. During constant current oxidation, the field across the oxide is constant, 1.2×10^7 to 1.9×10^7 volts/cm, depending on current density and the orientation of silicon. The oxidation rate is about 6 A°/V. The oxidation rate and efficiency show definite and parallel trends, they increase with increasing oxide thickness and current density. Under constant voltage anodization, the oxide thickness and current density vary with the logarithm and reciprocal of time, respectively. The oxidation rate and efficiency decreases with time and thickness. This decrease could be due to decreasing current density and/or structural changes in the oxide.

The main advantage of anodic as opposed to thermal oxidation is that it can be performed at much lower tempera-

tures. Hence processes that deteriorate the minority carrier lifetime, can be avoided. Also, unwanted changes in the doping profile within silicon can be minimized. The disadvantages of anodic oxidation are limited thickness (2000-3000 A°) because of breakdown effects.

In 1969 C.R.Fritzsche [56] studied the dielectric breakdown in anodically grown SiO_2. 1 ohm-cm single crystalline silicon wafers polished on one side and nickel plated on the backside was anodized in a solution of 0.4 g KNO_3 in 100 c.c. ethylene glycol at 25°C. Platinum was used as cathode and its distance from the silicon was 1.2 cm. The water content of the glycol was checked by Karl Fischver titrations and in, most cases kept between 0.06 and 0.08%. Aluminium electordes 0.5 mm in diameter were evaporated for breakdown measurement. Breakdown voltage was measured with dc as well as pulse methods, an improved pulse amplifier was used and the current limiting resistor was only 220 ohm at pulse measurement. The self-healing breakdown as well as the final breakdown which destroys the sample definitively were noted. These two types of breakdowns were called as first breakdown and definitive breakdown. It was reported that the probability of breakdown at specific point defects depends upon electrode diameter. The dielectric strength of the grown oxide layer decreases with increasing temperature and the water content of the electrolyte. It is reported

that impact ionization takes place during anodic growth of SiO_2. It is found that avalanch multiplication of electrons and ionic conductivity are closely related. An improved theory is given which supplies equations for efficiency of anodization, growth at constant current, and current decay at constant voltage in excellent agreement with experimental results. The effective mass ratio of electrons to ions, the mean free time of the electrons, the mean time between ionizing collisions and the electron drift velocity are estimated from experimental data.

In 1970 R.Nannoni [57] reported that an abundant literature has been dedicated to thermal oxidation of silicon and to anodic oxidation of metal like Al, Ta, Ti, Nb, but a very few works related to the anodic oxidation of silicon have been carried out. Nannoni observed that the electrical properties of anodic oxide films and of the semiconductor oxide interface have not been investigated in detail. The results of the complex capacitance method used to characterize the semiconductor surface properties were described.

For the fabrication of MOS capacitors the silicon epitaxial wafer of $\langle 111 \rangle$ orientation is cleaned in boiling CCl_4 and in boiling HNO_3 rinsed in deionized water and dryed in twice distilled methylic alcohol and then in

ethylic ether. The wafer was anodized in a teflon cell containing the solution of 8 gm/litre of KNO_3 in twice distilled diethylene glycol as electrolyte. The electrolyte bath was replaced for each preparation. A platinum grid was used as a cathode. A three step anodization process is used. In the first step the current is exactly zero. In the second step the current follows a linear increase of 0.5 mA/cm² per minute upto a density of 10 mA/cm². In the third step the voltage limiter takes control and keeps a constant voltage U_{ox} across the terminals, the current I_{ox} decreases freely reaching for instance 10 A/cm² for t_{ox} = 24 h, U_{ox} = 200V, the oxidation temperature T_{ox} being kept constant at 30°C. After its oxidation the sampe is rinsed in ethylene alcohol then in methylic alcohol and dried in ethylic ether, then immediately stored under vacuum of 5×10^{-6} torr. For electrical measurements seven gold electrodes 2 mm in diameter about 1000 A° in thickness were evaporated. The equivalent series capacitance C_{series} and the loss tangent $(\tan \delta)_{MOS}$ of the MOS capacitor were determined by using a capacitance bridge. These measurements were made at controlled temperature in a dry nitrogen atmosphere and in darkness. The AC voltage was maintained smaller than KT/q volts. To characterize the electrical properties of the anodic oxide MOS capacitors complex impedance values were considered and not only the imaginary part. The impedance Z^*_{mos} was calculated from the equivalent

series capacitance C_{series} and the loss factor $(\tan\delta)_{mos}$. Since the limit values (at a zero and infinite frequency) reached by the impedance are only capacitive, the compelx capacitance of MOS capacitor was introduced by

$$C^*_{mos} = C'_{mos} - i\, C''_{mos} = \frac{1}{i\, Z^*_{mos}}$$

C^*_{mos} representation was used in the complex plane (C''_{mos} as a function of C'_{mos}) currently used for dielectric study.

The anodic oxide can be either 'dry' (moisture exposure reduced to a minimum) or 'wet' (after voluntary exposure to moisture). The study of the complex capacitance C^*_{mos} of MOS capacitors has shown the important influence of the moisture on the properties of anodic oxide MOS structures. The unambiguous determination of surface state parameters from the variations of C^*_{mos} as a function of frequency, temperature, and applied bias is discussed. A method of characterizing the distribution of Surface states was proposed. The utilization of this method permitted to explain some apparently contradictory results published in the literature, and showed that:

(i) Whatever the oxide 'Wet' or 'Dry' and Silicon-Oxide interfaces are characterized by the same energy distribution of surface states, whose density is

hgih (about 10^{13} ev^{-1} cm^{-2}) and nearly symmetrical with respect to the middle of the gap.

(ii) The mobile protons contained in 'Wet' oxide have no influence on the distribution of surface states.

(iii) In order to reduce the density of surface states by thermal treatments at low temperatures (about 150°C) the oxide must be of 'wet' type.

In 1973 J.D.E.Beynon et. al [58] used the insulating SiO_2 layers grown anodically to fabricate MOS capacitors and MOS transistors. The MOS capacitor structures were used for investigating the electrical properties of the oxide and also the characteristics of the Si/SiO_2 interface. The threshold voltages of MOS structures were measured as a function of oxide thickness. Furthermore, the Hall mobility of the carriers in the channel of MOS transistors were ascertained by means of the specially designed Hall MOS transistor.

Mechanically polished 10 ohm-cm n-type $\langle 111 \rangle$ silicon substrates were used. The silicon slices were cleaned using sulphuric acid and hydrogen peroxide, followed by immersing alternately in hydroflouric acid and boiling aqua regia three times. Conventional diffusion techniques were used to form the p-type source and drain diffusion

regions of the MOS transistor. Electrical contact with the silicon slice was made via a diffused P region on the back of the slice, this provided a low resistance contact to the silicon (which was made the anode in the electrolytic cell). The cathode was a thin sheet of platinum having a total surface area of 2 cm^2. Several electrolytes were used but the most successful films were obtained using a mixture of 0.02N KNO_3 and 0.02N KNO_2 in ethylene glycol. Each silicon slices were anodised in the following way: a constant current source was maintained at an initial current density of 7 mA/cm^2. As the film grew, the potential difference across it increased. When this reached to a predetermined value, the voltage was maintained at this value and the current allowed to decay. The forming voltage was maintained until the current dropped down to about 200 $\mu A/cm^2$. Forming voltages between 10V and 200V were used to produce oxide thickness ranging 80 A° to 100 A°. The thickness of the oxide film was determined by ellipsometry. Due to depletion layer formation in n-type silicon at the silicon/electrolyte interface, the slice was illuminated to generate sufficient electron-hole pairs to allow growth to proceed at current densities of 7 mA/cm^2 at low voltages. Two metals aluminium and molybdenum were used for forming the gate. The metals were evaporated and then etched to form source, drain and gate regions. The slices were finally annealed in a mixture of hydrogen 40% and nitrogen 40%

for 15 min. at 500°C.

The following electrical tests were conducted on the fabricated samples. Using a keithley electrometer leakage current as low as 10^{-13} Amp at 10V were measured for 1100 A° films, the resistivity of the anodic oxide film for thickness ranging from 200 A° to 1100 A° was found to be $7 \pm 1 \times 10^{15}$ ohm - cm. The breakdown field strength of the oxide was deduced from the voltage required for catastrophic breakdown of the MOS capacitor. Breakdown of the oxide .was measured for positive bias voltage such that the surface of the n-type silicon immediately under the gate was in accumulation. Results indicated that the breakdown voltage is proportional to film thickness i.e. the breakdown field strength is constant. Its value was approximated 8×10^6 V/cm. From C-V measurements on aluminium MOS capacitors, it was deducted that there was a surface charge density of $2\text{-}3 \times 10^{11}$ electronic charges/cm², this charge was found to be independent of oxide thickness. To determine the stability of the oxide, bias-temperature stress experiments were carried out on the MOS capacitors. The capacitors were heated to 150°C and maintained at this temperature for 15 min and then allowed to cool with a continuous biasing field of 10^6 V/cm produced by positive gate voltage. The C-V curves of the capacitors were plotted before and after the bias temperature stress to determine the shift

in flat band voltage no significant shift was detected. The threshold voltages of the MOS transistors were measured for drain currents of 1 μ amp. A quite good agreement between the calculated and measured values of threshold voltage was reported. Hall mobility measurements were made only on device with a gate oxide thickness of 1100 A°. The average value of hall mobility of holes in the inversion layer was found tobe 210 ± 20 $cm^2/V.sec$.

In 1977 W.D.Mackintosh and H.H.Plattner [59] identified the mobile ions during the anodic oxidation of silicon. During anodic oxidation either the cation or the anion or both must migrate across the thickening oxide film. The mobile ion can be identified or, if both move, the relative mobilities can be deduced by tagging a thin surface layer with a completely immobile marker atom and determining its position after anodizing the speciman. If the marker is found at the surface then oxidation has taken place by inward migration of the anion to form the film beneath the marked layer. If the marker is found at the substrate/oxide interface the opposite process has occured. An intermediate position indicates both cation and anion have moved and the relative mobilities are proportional to the relative thickness of the oxide on either side of the marker atoms. The inert gas atoms were chosen as markers on the grounds that they are the most likely to remain unchanged within

the oxide lattice and hence are not influenced by the application of the electrical field. In addition their large size suggests that they should not diffuse through the lattice at room temperature. The marker locations were determined by Rutherford backscattering analysis.

A variety of specimens were used. Some were thin wafers cut very closely parallel to the $\langle 111 \rangle$ plane while others were tablets 3/8 inch thick cut from 10° off the $\langle 111 \rangle$ plane, most were p-type boron-doped although one n-type phosphorus doped speciman was also used. The surfaces of all specimens were prepared by vibratory polishing with 0.3 μm alumina, followed by ultrasonic cleaning to remove the abrasive. They were then degreased in trichloroethylene, etched for 5 min. in 0.5N HF and washed thoroughly. Oxidations were carried out in a Teflon cell constructed for this purpose in such a way that only 0.7 cm² of polished surface was exposed to the electrolyte. The electrical connection was made by diffusing gold into a small area on the back of the speciman and firmly contacting this area to a copper plate contained in the body of the cell. Experiments were carried out with the following electrolytes:

(a) 0.1N aqueous solution of H_3BO_3 and $Na_2B_4O_7 \cdot 10H_2O$.

(b) 0.4N solution of KNO_3 in N-methylacetamide and

(c) 0.3N solution of KNO_2 in tetrahydrofurfuryal alcohol.

The inert gas atoms Kr or Xe were introduced into the Si surface layers with a low energy mass separator. The amounts implaned were 5×10^{14} atoms/cm² for Xe and 1×10^{15} for Kr. These are the minimum amounts conveniently detected by Rutherford back scattering analysis. Specimens with prepared surfaces were anodized to give a film thickness of $\backsim 16 \mu g/cm^2$. They were then implanted with the chosen marker at an energy that would insure that the greater part of the implanted material was located within the oxide film. Rutherford backscattering spectra were obtained. The specimens were then further anodized to a chosen voltage and analysed again. Computer analysis of the data was then carried out to obtain the position of the markers, the thickness of the oxide films, and the count of He ions back-scattered from the implanted atoms. In every case the markers were found to be very close to the outer oxide surface, showing that inward movement of the anion is responsible for oxide growth. In this respect anodic oxidation resembles thermal oxidation.

In 1979 G.C.Jain et. al [60] studied the mechanism of the constant voltage anodic oxidation of Si in a solution of ethylene glycol + 0.04N KNO_3. They found that the thickness of the formed oxide vary linearly with the forming voltage

at a rate of 6.3 A°/V. The anodization current for a fixed value of forming voltate decays exponentially with a linear tail. The thickness of the grown oxide obeys a parabolic law, and the ionic current efficiency tends to decrease with time up to a field ∽20 MV/cm.

Experiments were performed on rectangulared shaped silicon single crystal chips of size 45 mm x 5 mm and of thickness 300 μm. The crystals were p-type with a resistivity of 8 ohm-cm cut parallel to the $\langle 111 \rangle$ plane lapped flat and then polished mechanically using a submicron alumina powder as slurry followed by a light etch in the HF, HNO_3 and H_2O system. The electrolyte used was ethylene glycol + 0.04N KNO_3. trace of water (0.1 - 1%) was present in ethylene glycol. The cathode was of a noble metal (gold) foil. The thickness of the oxide was found by a comparison of the oxide colour with a standard interference colour chart.

CHAPTER III

ANODIC OXIDATION OF SILICON AND FABRICATION OF MOS STRUCTURES

3.1 INTRODUCTION

The literature survey shows that in last two decades efforts were made to grow anodic - oxide films over silicon wafers using different electrolytes and their characteristics were studied. However the electrical properties of anodically grown oxide films and the semiconductor oxide interfaces were not fully investigated. As the oxide films grown by thermal oxidation were found superior as compared to anodically grown films and therefore they were widely investigated and were used for fabricating insulating films for the applications in semiconductor and I.C. Technology.

As the integration of large number of devices in a single chip is increases it was realised that high temperature processes are not suitable for VLSI technology, particularly the high temperature oxidation limits the further integration of devices in a single chip and degrades the performance of the devices. Therefore it is proposed to grow high quality SiO_2 films at low temperatures using anodic oxidation technique for VLSI applications. Due to the ease of fabrication, simplicity of structure and

the sensitivity of the C-V characteristics to physical properties MOS structures are used as a test vehicle to study the influence of process parameters on properties of insulating films grown on silicon and to study Si-SiO_2 interfaces. For the fabrication of MOS samples.

A stringent cleaning procedure was used to minimise the surface contamination of the samples. A proper electrolyte and its composition was selected, anodization parameters and annealing conditions were optimized. In order to grow high quality films and for obtaining the best results a large number of experiments and measurements were carried out and discussed in this chapter.

3.2 THE MOS STRUCTURE

The MOS capacitor offers an incredibly powerful test structure for evaluation of the dielectric properties of grown films and for the study of electrical and interfacial properties of semiconductor - oxide interface. Schematic of MOS structure is shown in fig. 3.1. Essentially it consists of an n- or p-type semiconductor, covered by a thin oxide film with a metal electrode (gate) on top of the insulator and an ohmic contact to the semiconductor. Such devices can be an important research tool because their capacitance versus bias (C-V) characteristics contain information about the surface states present in this

system. The performance of MOS system depends on the interface properties of the semiconductor and the oxide film grown over the semiconductor. Interface state density and dielectric breakdown strength are used to assess the quality of oxide film. Low value of interface state density and high value of breakdown field are the desired characteristics of a good insulating film. Therefore the measurement of interface state density and breakdown field are important to assess the quality of the oxide film grown on semiconductor and to optimise the process parameters associated with the fabrication of the oxide layers. To evaluate the surface states density either capacitance or conductance methods can be used. The conductance method gives the accurate results as compared to capacitance method, but it requires large number of time consuming measurements. Therefore to compare the characteristics for optimization of anodization parameters capacitance method is used. For final assessment of the grown films conductance method was used as described in chapter IV. In the MOS capacitance method, a d-c electric field is applied between the metal electrode on the oxide and the silicon. For a given value of this field, a definite charge distribution in the MOS system will arise. The differential capacitance of the silicon space charge region is then measured by superimposing a small ac voltage on the dc bias. The differential capacitance as a function of the applied dc bias is determined. These

measurements were taken with Boonton Bridge. The obtaned capacitance vs voltage (C-V) curve is compared with a calculated ideal curve [61], i.e. characteristics of a silicon-vacuum interface without surface states. If, for each value of the D.C. field, equilibrium had been established and the frequency of the small ac signal is so high that no electronic transfer between various states outside the silicon (i.e. interface, oxide states) and the space - charge region can take place during one period, then this comparison gives the density of charges residing in these states as a function of the silicon surface potential, or, what is equivalent to this, as a function of the energy position of these states in the Si forbidden band. The density of states at flatband condition i.e. $V_s = 0$ is designated as N_o and is frequently used to characterize the MOS sample. The voltage difference between the measured and ideal C-V curves (ΔV at flat band) can be used to calculate the surface states at flat band condition. The density of surface states in unit of cm^{-2} is determined by Gauss law as:

$$N_o = \frac{C_i \Delta V}{q}$$

where C_i is the insulator capacitance in strong accumulation region and q is the electronic charge.

3.3 SURFACE PREPARATION OF SILICON

The material used in the investigation was n-type

epitaxially grown silicon wafers of ⟨111⟩ orientation having resistivity of 6 to 8 ohm-cm. The resistivity of the substrate was 0.005 ohm-cm. The purpose of using $n\text{-}n^+$ epitaxial wafers are to minimise the bulk series resistance to a negligible value as it causes a serious error in the extraction of interfacial properties from admittance measurements. Further it is easy to make good ohmic contact on n^+ silicon substrate. For the fabrication of test MOS samples wafers were cut into 8 mm x 8 mm square pieces using diamond tool scriber.

Wafer cleanliness before, during, and after oxidation is perhaps the most important requirement for growing high quality oxides [62]. Impurities present on the silicon surface prior to oxidation or during the oxide growth itself influence the homogeneity of the film, the interfacial and electrical properties of the grown films. There are three broad categories of surface contaminants:

(a) molecular,

(b) ionic and

(c) atomic

Typical molecular contaminants are natural and synthetic waxes, resins and oils. They may also include grease from fingers and greasy films that are deposited when surfaces are exposed to room air or stored in plastic

containers. Layers of such molecular impurities in contact with the substrate surface are usually held by weak electrostatic forces. Organic contaminants on silicon devices, especially on surface-sensitive MOS structures, may cause polarization [63] and ionic drift [64] due to the transport of protons [65]. Water insoluble organic compounds tend to make semiconductor and oxide surfaces hydrophobic, thus preventing the effective removal of absorbed ionic or metallic impurities. The removalof molecular contamination is threfore the first step in a cleaning process.

Ionic contaminants are left on the surface of the wafer after etching it in etchants containing HF acid, out of these ionic contaminants, alkali ions are particularly harmful as they may move under the influence of electric fields or at elevated temperatures, causing inversion layers, surface leakage drifts during device operation, and other instabilities [66].

Atomic contaminants present on a silicon surface include heavy metals such as gold, silver and copper. They originate from acid etchants and are usually present in the form of metallic deposits [67]. The removal of this type of contaminant generally requires reactive agents that dissolve the metal and complex the ionic from to prevent redeposition from the solution. Atomic impurities, especially the heavy metals, can seriously

affect minority - carrier lifetime, surface conduction, and other device parameters governing stability of the devices [68].

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Since a contaminated surface is likely to contain all three types of impurities, it is necessary to first remove the gross organic residues masking the surface,

then the residual organic materials, and finally the residual ionic and atomic contaminants. The following procedure was used to clean the samples.

The samples were first boiled in trichloroethylene and then ultrasonirated in acetone. The samples were treated with a solution of H_2O - H_2O_2 - NH_4OH (typically five parts by volume of H_2O, one part 30% unstabilized H_2O_2 and one part NH_4OH). It removes organic contaminants by solving action of the ammonium hydroxide and the oxidizing action of the peroxide. The sampels were then rinsed with deionized water. The samples were treated with second solution of H_2O - H_2O_2-HCl (typical composition is six parts H_2O, one part H_2O_2 and one part HCl by volume). The samples were rinsed thoroughly in deionized water with several changes. Metal impurities are oxidized by the action of both the hydrogen peroxide and the chlorine in the solution resulting stable chloride complexes, the solution removes metallic impurities from the silicon surface and prevents their displacements plating back onto the silicon [69]. The main advantage of these two cleaning solutions is that they are composed of volatile components and thus leave no residues on the silicon surface. Finally the slices were dipped in dilute HF acid rinsed in deionized water treated with alcohol and blown dry before immersing them in the anodization cell.

3.4 CLEANING OF ACCESSORIES

Pyrrex Glass accessories such as beakers, sample holders, stirrer etc. used in the experimental work were cleaned thoroughly to remove organic and inorganic contaminants, and dust particles etc. Otherwise the impurities introdeuced from the accessories during the handling of the samples may adversely effect the quality of oxide grown. Based on experimentation the following cleaning procedure was found appropriate which gave the most satisfactory results.

(i) Boil the glasswares in teepol.

(ii) Wash the glasswares thoroughly in water.

(iii) Boil the glasswares in the solution of NaOH for five minutes.

(iv) Wash the glasswares with distilled water.

(v) Dip the glasswares in hot concentrated chromic acid for five minutes.

(vi) Wash the glasswares again with distilled water and dry with hot air.

(vii) Rinse ultrasonically in acetone for 5 minutes.

(viii) The glasswares thus cleaned were placed in a dust free hot electric oven.

The anodization process was carried out on the horizontal laminar flow clean bench placed in the clean room. Electronic grade chemicals and ultrapure water having resistivity of the order of 14.5 M Ohm-cm were used. The ultrapue water was prepared by first distilling the tap-water, the distilled water was subjected to ultra-violet light to minimize the bactria count [70]. Finally it was passed through the sybron/Bransted water purification system.

3.5 THE EXPERIMENTAL SET-UP AND FABRICATION OF MOS TEST SAMPLES

The complete anodization set-up is shown in Fig.3.2. Essentially it consits of d.c. power supply, a variable series resistance, an electrolytic-cell, a FET Nanoammeter (Aplab TF M13 Model). The electrolytic cell consits of a pyrex glass beaker having freshly prepared electrolyte. A spring loaded platinum tipped probe in contact with the sampel serves as anode of the anodization cell. The cathode must be of such conducting material which does not dissolve in or contaminate the electrolyte. Its shape should allow easy cleaning and enough surface for exposure to electrolyte, the cathode was made of a platinum flat strip of size 4 cm x 0.5 cm. Before use it was thoroughly cleaned. The electrolytic cell was placed on a magnetic stirrer (Martin and Harris Magstir) so that electrolyte

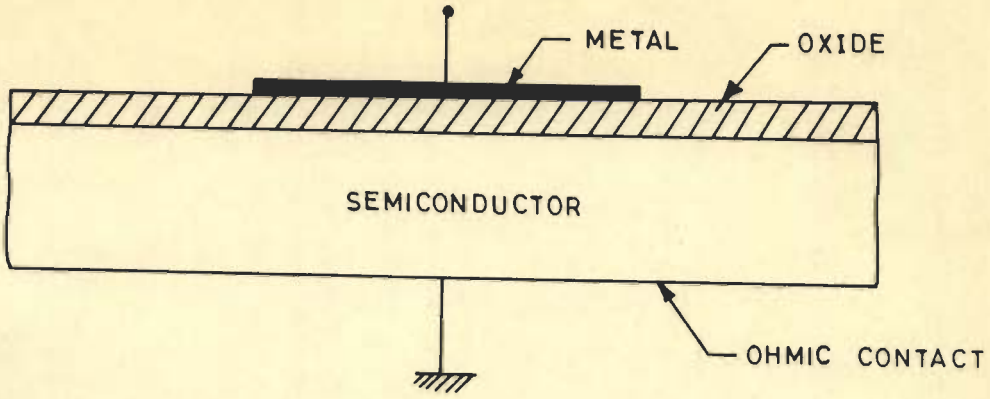


FIG. 3·1: METAL - OXIDE - SEMICONDUCTOR (MOS) STRUCTURE

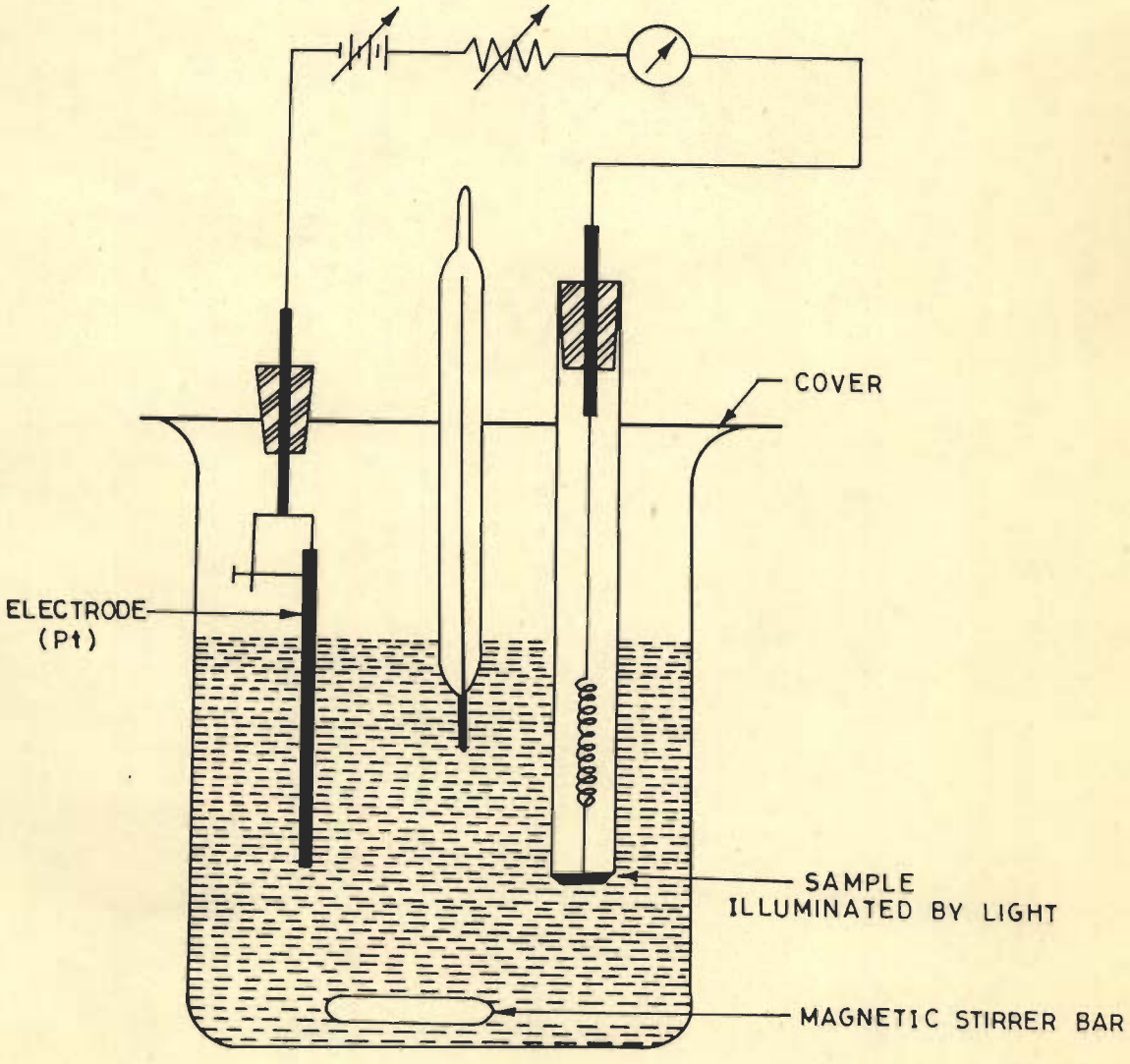


FIG 3·2: SCHEMATIC OF ANODIZATION SET-UP

may be stirred during the anodization process as shown in Fig. 3.3.

In the experimental set up a colliminated light source was used to illuminate the test sample to provide holes by photo generation.

The sample to be anodized was fixed onto the sample holder as shown in Fig. 3.4 and explained as follows. The sample holder was made of pyrex glass tube. One end of this tube was made flat and had a hole of about 2 mm diameter in the centre. The sample was fixed on the sample holder by Apiezone wax. The sample edges were covered with the Apiezone wax to eliminate edge effects during anodization [71].

The anodic cell should have uniform spacing between electrodes to have uniform anodic current density, therefore the sampel holder and cathode were mounted on the lid ensuring that they are parallel to each other at every point in the electrolyte. Further it was also ensured that they do not touch either the side walls or the bottom of the beaker. The lid was placed on the beaker with stirrer in position. This set-up was placed on the beaker with stirrer in position. This set-up was placed in the horizontal laminar flow clean bench and is shown in Fig.3.5.

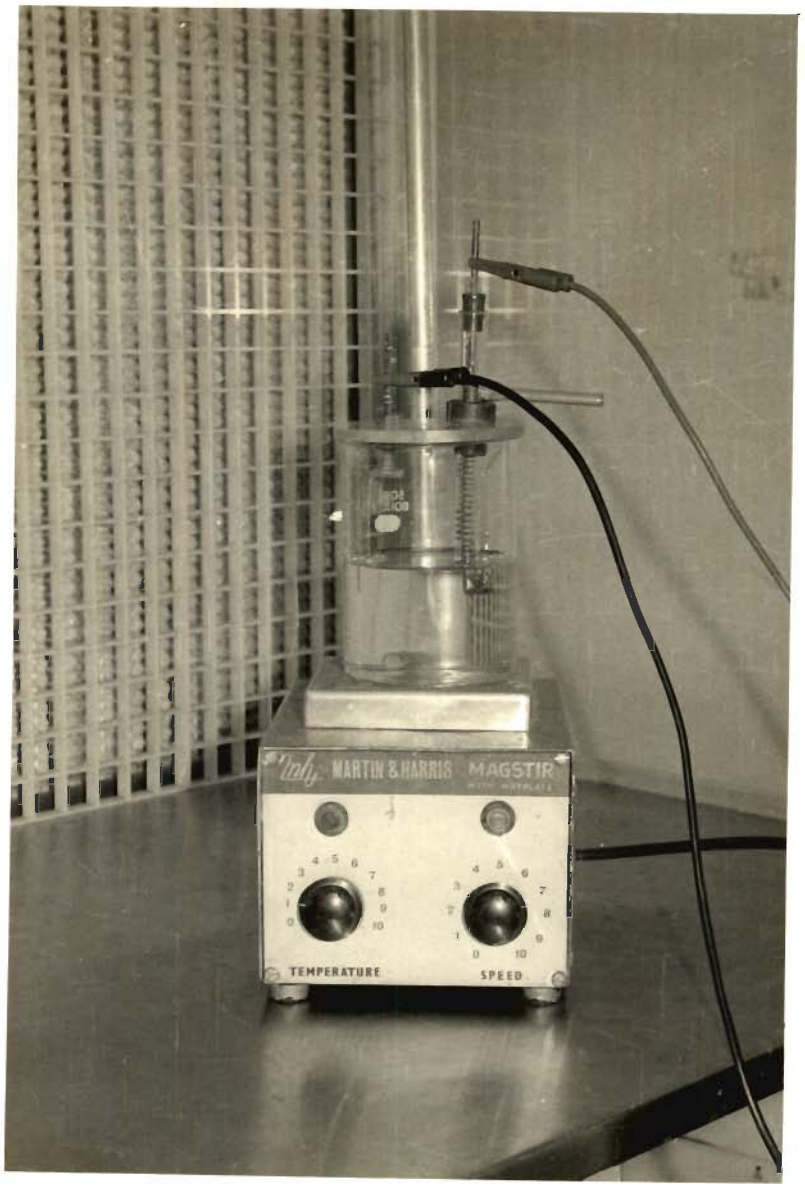


FIG. 3·3 : ELECTROLYTIC - CELL

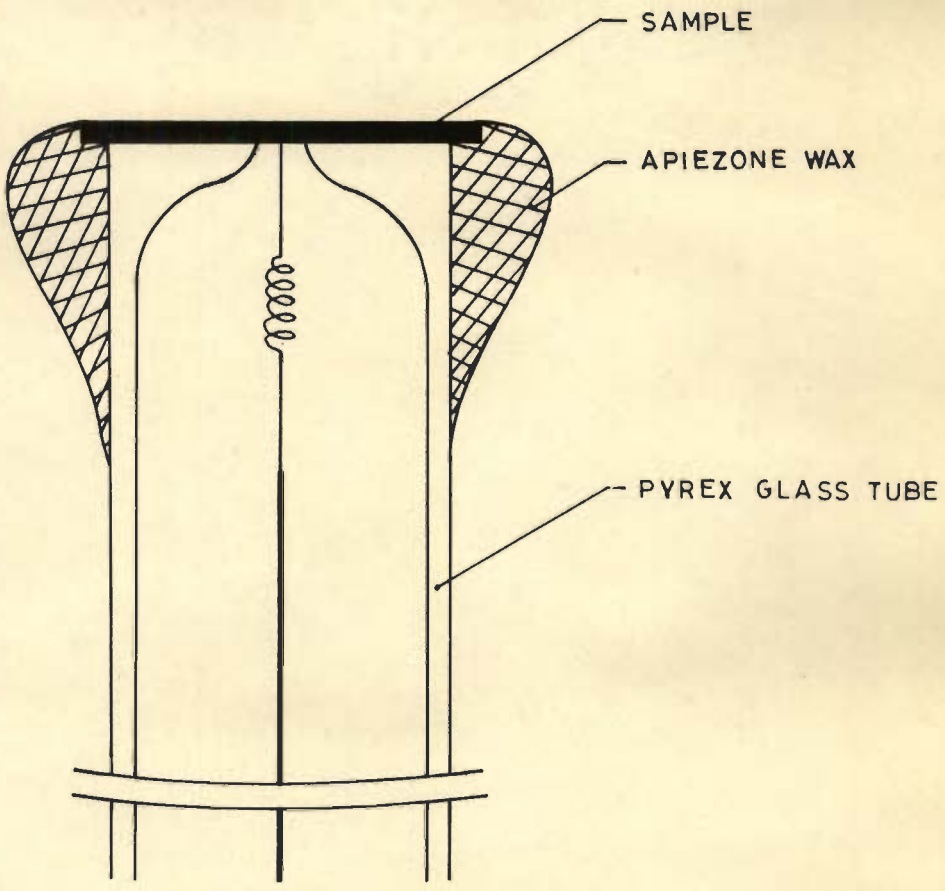


FIG. 3·4 : SAMPLE HOLDER

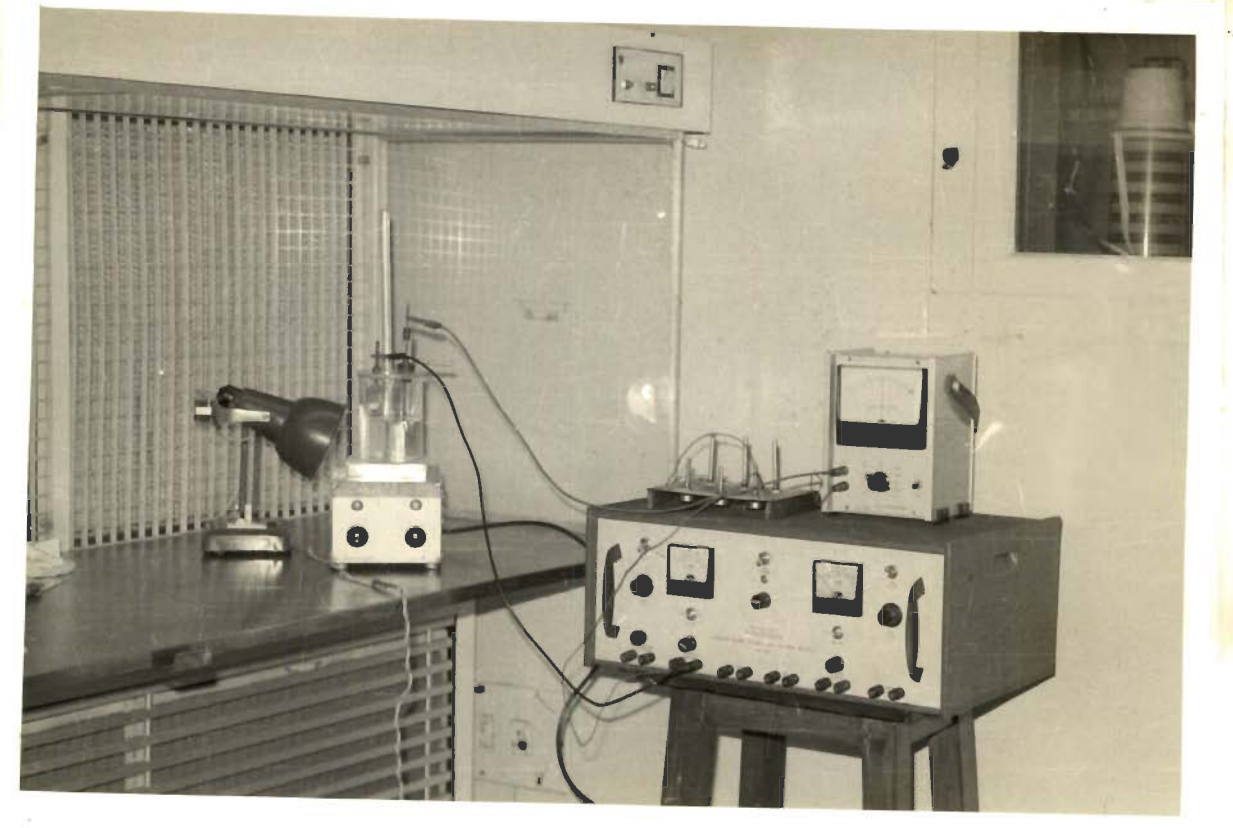


FIG. 3·5 : EXPERIMENTAL ARRANGEMENT FOR ANODIZATION

3.5.1 ELECTROLYTIC BATH

The electrolytic bath used for anodization was freshly prepared KNO_3 solution in Ethylene-Glycol. The use of ethylene glycol as a solvent has the advantage of low cost, high purity and good stability toward heat and electrolysis. An accurately measured quantity of KNO_3 was added to the Ethylene-Glycol. The solution was then stirred with a magnetic stirrer until all the solid KNO_3 material was completely dissolved in the ethylene glycol. The solution was carefully filtered to remove any solid particle in the solution. The ethylene-glycol is hygroscopic in nature and absorbs water from the atmosphere. A trace of water was found necessary for the best oxide characteristics which is absorbed by the ethylene-glycol itself from the atmosphere. If the excess water is absorbed by the electrolyte it will deteriorate the quality of grown oxide film. Therefore a freshly prepared bath was used for the anodization of each set of samples.

3.5.2 ANODIZATION PROCESS

Anoxidization may be carried out either in constant current mode or constant voltage mode. In the constant current mode the anodization current density was maintained constant throughout the anodization cycle by increasing the amount of the voltage across the anode and cathode

electrodes to the predetermined forming voltage by decreasing a series resistance connected to the anodization circuit. On the other hand under the constant voltage mode a predetermined voltage is applied across the anode and cathode of the anodization bath and it is maintained constant throughout the anodization process while the current decreases as the oxide film grows on the sample. In the present work the anodization was first carried out under constant current mode to a predetermined forming voltage followed by a constant voltage mode until the current was reduced to a minimum final value. Most of the oxide is grown during the constant current mode while the subsequent constant voltage mode improves the quality of the grown oxide film.

3.5.3 ELECTROLYTE MOLARITY

For optimizing the molarity of electrolyte, the solutions of Potassium Nitrate Salt (KNO_3) of molarity 0.02N, 0.04N, 0.06N and 0.08N in Ethylene Glycol ($C_2H_6O_3$) were prepared. The wafers were cleaned as described in section (3.3). The test MOS samples were fabricated by growing oxide films on separate Si pieces using the electrolytes of four different molarity as given above.

For each sample the anodization was carried at a constant current density of 10 mA/cm² while forming voltage

increases gradually until it reached a predetermined value of 100V at this point forming voltage was kept constant and the current density was allowed to decrease. Immediately after anodization, the sample was removed from the tube and cleaned with, DI water, trichloroethylene and acetone. SiO_2 film thickness was estimated by a colour comparison chart. The samples were annealed in hydrogen ambient at 300°C. The MOS capacitors were formed by the vacuum deposition of aluminium through a metal mask. The field plate area of gate was typically 3.3×10^{-3} cm^2. For C-V measurements a Boonton Direct capacitance Bridge (Model No. 75C - S 23) was used. The density of surface states at flat band position was determined by high frequency C-V technique given by Zaininger et. al. [72]. For comparison of Ideal C-V curves with the measured curves, Ideal C-V curves calculated by Goetzberger [61] were used. The dielectric strength of samples were also determined. The results are given in Table I. Results indicate that surface state density is minimum for the samples fabricated at 0.02 Molar concentration. Surface State density increases as the molar concentration of electrolyte increases.

Further it was observed that the dielectric break down strength is maximum for samples fabricated using electrolyte of 0.04 Molar concentration. Although surface density was found minimum for the samples fabricated

using electrolyte of 0.02 molar concentration but the dielectric breakdown is at lower side for such samples. Hence the optimum value of Molar concentration of the electrolyte is chosen 0.04N.

3.5.4 ANODIZATION CURRENT DENSITY

In order to determine the optimum value of current density the samples were fabricated as described in Section 3.5.3 using an electrolyte bath of 0.04N KNO_3 molarity in Ethylene Glycol. The anodization cycle was carried in the electrolytic bath in constant current mode followed by constant voltage mode. samples were fabricated at four different constant current densities 20 mA/cm², 10 mA/cm², 5 mA/cm² and 1 mA/cm² at a forming voltage of 100V. Film thickness was estimated to 600 A°. The C-V curves were plotted with the help of Boonton Bridge at 500 KHZ. The surface state density was calculated at Flat band condition. The dielectric strength of each sample was calculated by measuring the dielectric breakdown voltage. The influence of current density on the surface state density and the dielectric strength is summarized in Table II. Results show that samples fabricated at 5 mA/cm² current density resulted in lower value of surface state density and higher value of dielectric strength. Hence for subsequent fabrication of MOS samples a current density of 5 mA/cm² was chosen. The quality of grown film at 1 mA/cm² was poor.

TABLE - I

Film Thickness 600 A° Samples Fabricated at Constant Current Density of 10 mA/cm²

Molarity	Surface state density measured at Flat Band Voltage (States cm^{-2})	Dielectric strength (Volts/cm)
0.02 N	7.0×10^{11}	5.5×10^{6}
0.04 N	7.5×10^{11}	5.7×10^{6}
0.06 N	1.0×10^{12}	5.2×10^{6}
0.08 N	3.5×10^{12}	4.8×10^{6}

TABLE - II

Film Thickness 600 A°

Anodization current density (mA/cm^2)	Surface state density measured at flat band (states cm^{-2})	Dielectric strength (volts/cm)
20.0	8×10^{11}	3.5×10^6
10.0	7.2×10^{11}	4.2×10^6
5.0	6.0×10^{11}	5.9×10^6
1.0	-	2.5×10^6

3.5.5 APPLIED FORMING VOLTAGE AND THICKNESS OF THE GROWN FILM

Test MOS samples were fabricated as described in Sub-section 3.5.3 using an electrolyte bath of 0.04N KNO_3 molarity in Ethylene-Glycol at constant current density of 5 mA/cm^2 followed by constant voltage mode. The samples were fabricated at different forming voltages that is 50 V, 100 V, 150 V, 200 V, 250 V, 300 V and 350 V. The thickness of the grown oxide film on the samples were estimated by the comparison of the grown oxide films colour with a standard interference colour chart [73] as the film thickness measuring instruments were not available in laboratory hence to verify the estimated thickness, the film thickness of few samples were measured at IRDE Dehradun. It was observed that the estimated values were within ± 50 A°.

The forming voltages and their corresponding thickness of the grown oxide films are shown in Fig. 3.6. The slope of the straight line shows that the growth proceeds at the rate of 6.0 $A° V^{-1}$ and the growth of oxide film is directly proportional to the forming voltage. For subsequent measurements, the thickness of the grown films were estimated by the applied forming voltage.

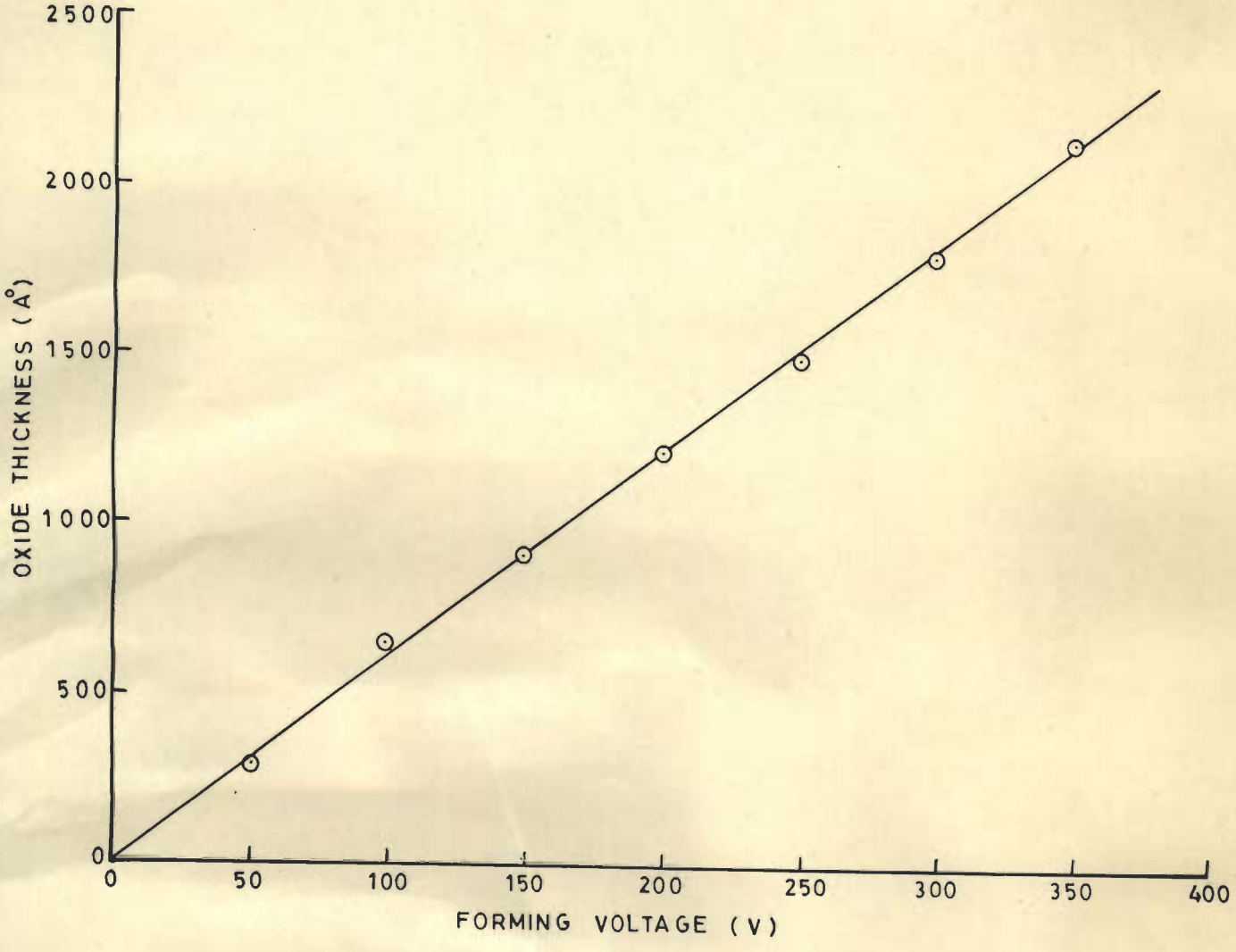


FIG. 3·6 : VARIATION OF GROWN OXIDE THICKNESS WITH FORMING VOLTAGE

3.5.6 ANNEALING

Anodically oxidized samples were annealed in a resistance heated Quartz tube furnace in an atmosphere of hydrogen. For this purpose a resistance heated Quartz-tube furnace as shown in Fig. 3.7 was used. Before the annealing the Quartz tube was thoroughly cleaned to avoid the sodium ion contamination during annealing process. High priority hydrogen gas was used to create an atmosphere of hydrogen inside the Quartz tube. To optimize the annealing temp. the test samples were fabricated with an oxide thickness of 600 A°. The different fabricated samples were annealed at different temp in hydrogen ambient, that is at 100°C, 200°C, 300°C, 400°C, 500°C and 600°C respectively for 30 minutes. After annealing the samples were allowed to cool slowly inside the Quartz tube in the atmosphere of hydrogen. Samples were taken out from the furnace when they were cooled down upto the room temperature. The C-V curves were plotted for the different annealed samples. Fig. 3.8 shows the plotted curves. It is observed that the C-V curves becomes steep, and the flat band voltage decreases with increasing annealing temperature upto 500°C. However the C-V characteristic for sample annealed at 600°C differed from the samples annealed at or less than 500°C. The surface state density was evaluated for the sample annealed at 500°C and an unannealed sample. The results are shown in Fig. 3.9.

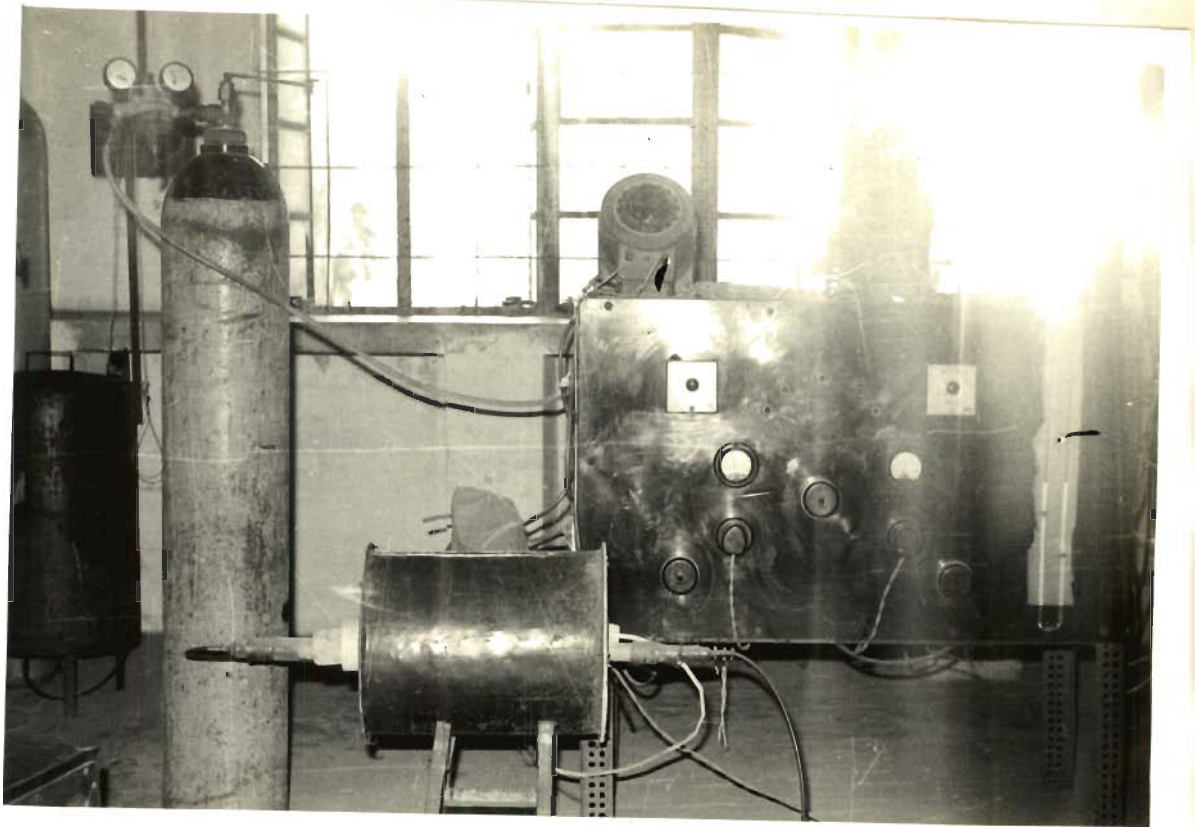


FIG. 3·7 : RESISTANCE HEATED QUARTZ-TUBE FURNACE FOR ANNEALING OF SAMPLES

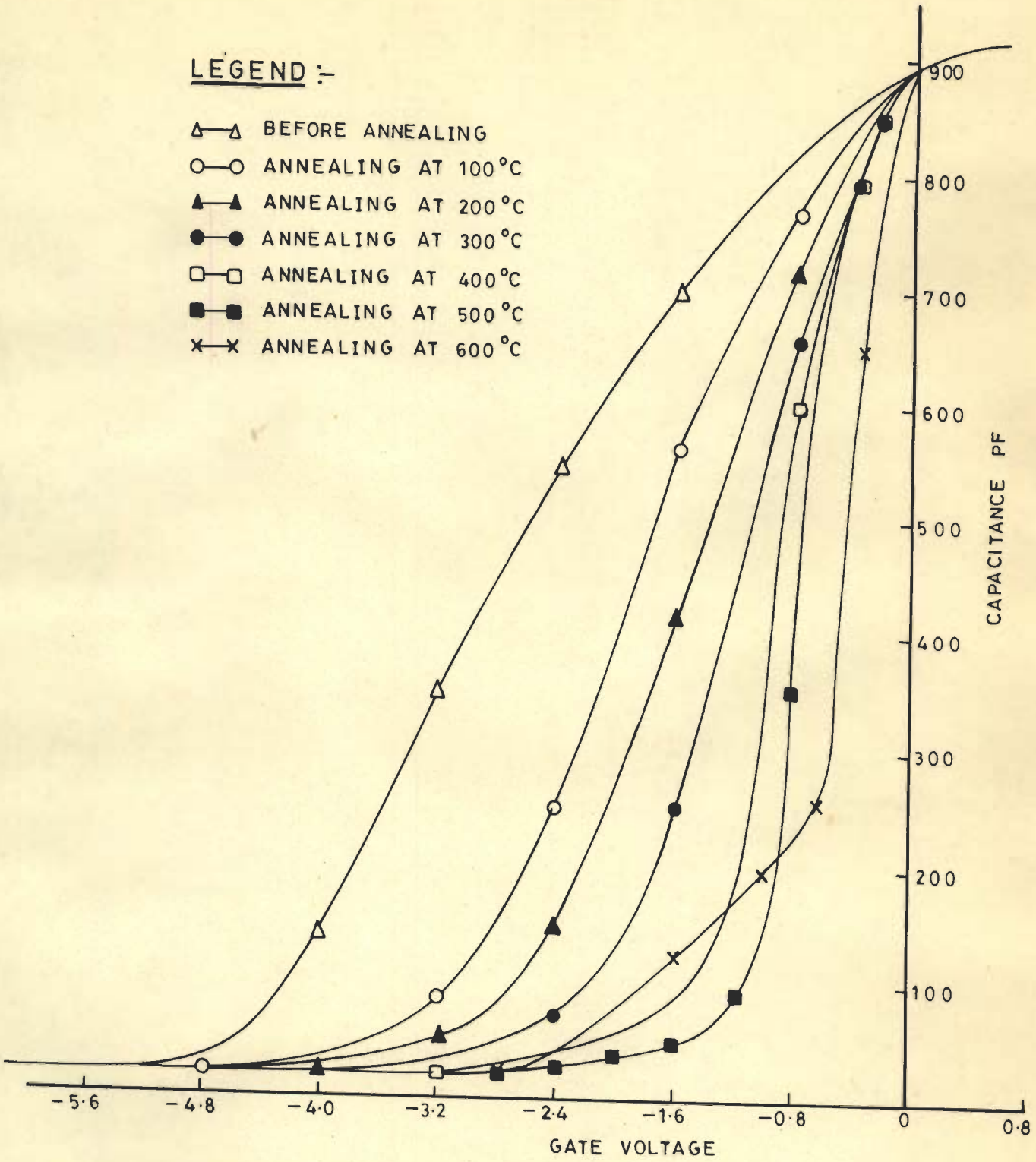


FIG.3·8 : C-V CHARACTERISTICS OF MOS SAMPLES ANNEALED AT DIFFERENT TEMPERATURES

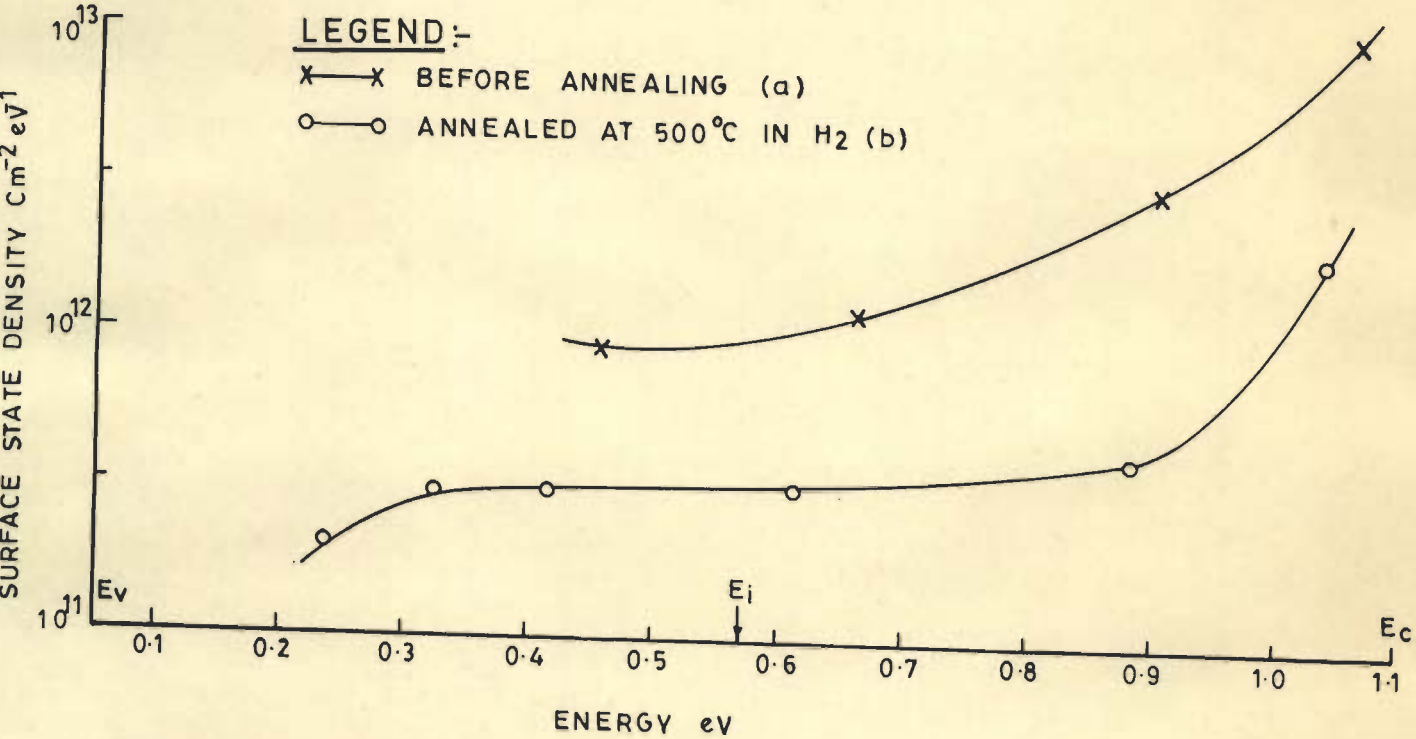


FIG. 3·9 : VARIATION OF SURFACE STATE DENSITIES ACROSS THE BAND GAP OF Si
(a) UNANNEALED SAMPLE
(b) ANNEALED SAMPLE

The result shows that the interface state density decreases for the sample annealed at 500°C in comparison to the unannealed sample. It was also observed that due to the heat teatment at 500°C the interface state density was not only reduced near the mid gap but also in a comparatively wide energy range.

3.5.7 GATE ELECTRODE AREA

To study the effect of Gate Electrode area a large number of MOS samples were fabricated having a film thickness of 600 A°. The area of Gate Electrode varied from 3×10^{-3} cm^2 to 3×10^{-2} cm^2. It was observed that dielectric strength of the grown oxide film depends on the electrode area. For the samples with larger electrode area smaller dielectric strength values were observed. This is due to the probability of finding a weaker link when the electrode area is large. The experimental results are shown in Fig. 3.10.

3.5.8 FORMATION OF OHMIC CONTACTS

Ohmic contacts between a metal and a semiconductor are defined as those which exhibit linear current-voltage characteristics, and it must have a low electric resistance fraction of a ohms.

For fabrication of ohmic contacts a Hind High Vacuum Coating Unit Model No. 12A shown in Fig.3.11 was used.

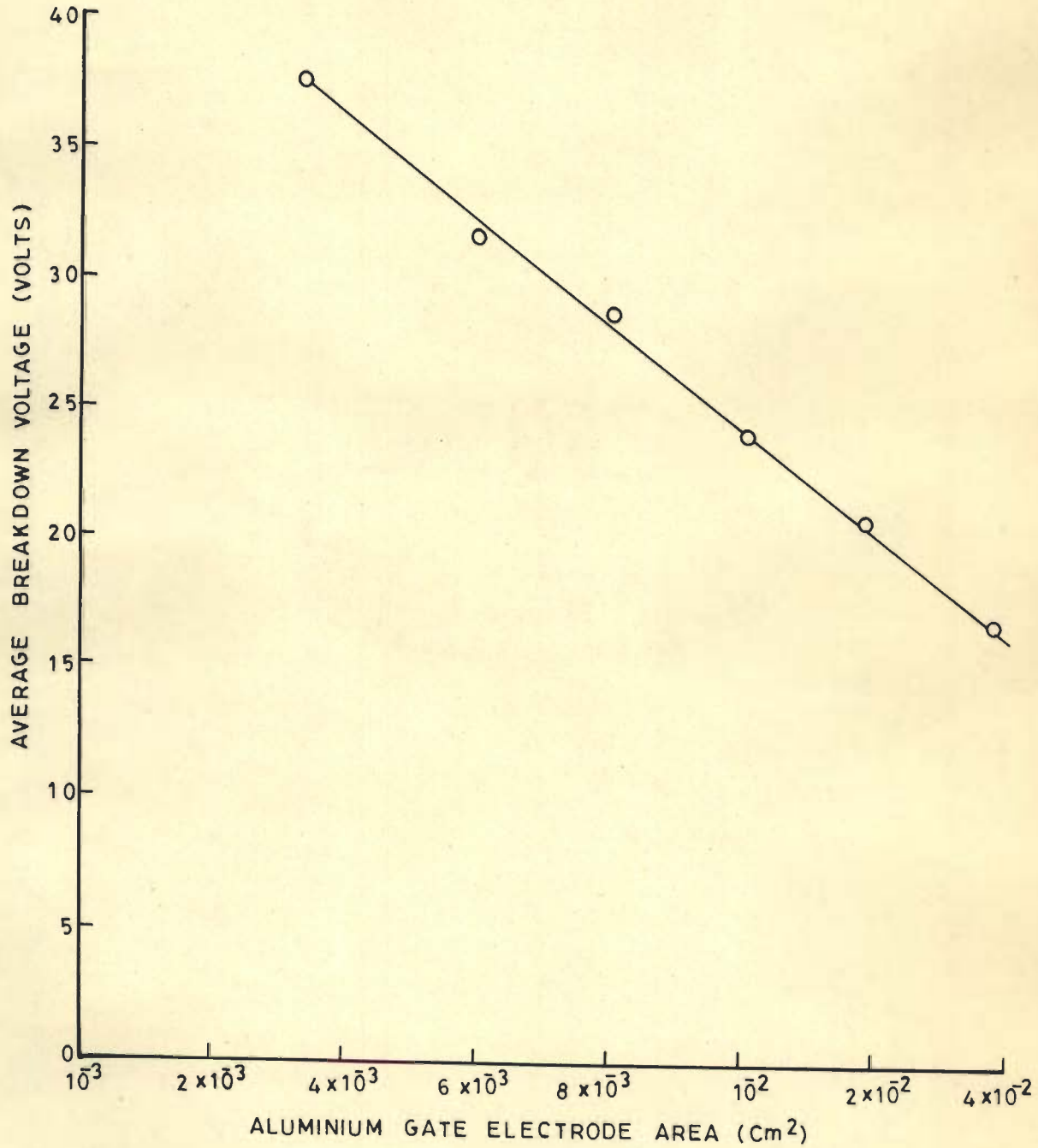


FIG. 3·10 : VARIATION OF BREAKDOWN VOLTAGE WITH ELECTRODE AREA

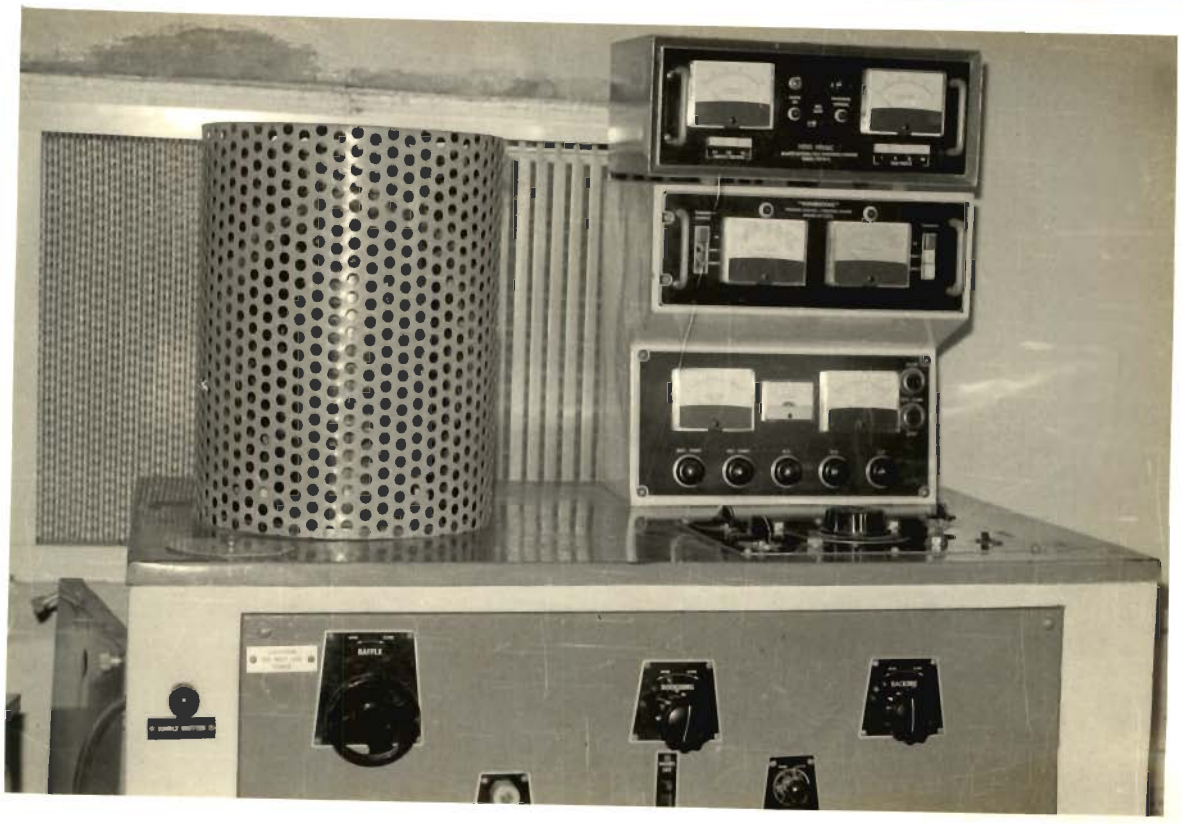


FIG. 3·11 : VACUUM COATING UNIT

Before evaporation all accessories of the vacuum chamber and the inner surface of the belljar was thoroughly cleaned by acetone. For the evaporation of aluminium, tungston wire in the form of V notch was used as a source. The tungston source was thoroughly boiled in trichloroethylene and then ultrasonirated in acetone. The cleaned source in the form of V-notch was connected between low Tension electrodes of the vacuum coating unit. For deposition 99.999% pure aluminium in the form of wire was used. The ultrapure aluminium wire was cut into small pieces and made small riders in the form of U's. Before loading to the tungston source the aluminium riders were thoroughly cleaned by boiling in trichloroethylene and ultrasonirated in acetone. The ohmic contacts were fabricated at the back of anodized samples by depositing aluminium film and then alloying it upto eutectic temperature. But before depositing the aluminium film it is necessary to etch-off the oxide layer from the back side. The anodized surface was protected from HF by covering it with high quality wax and the oxide layer of back side is etched off in the buffered HF. Then the samples were washed in deionized water, boiled in trichloroethylene and cleaned in acetone. For holding the silicon samples inside the vacuum coating unit stainless steel tweezers were used. The samples were tightly held between the tips of the tweezer with the help of a screw as shown in Fig. 3.12. The tweezers holding the samples were mounted on the substrate

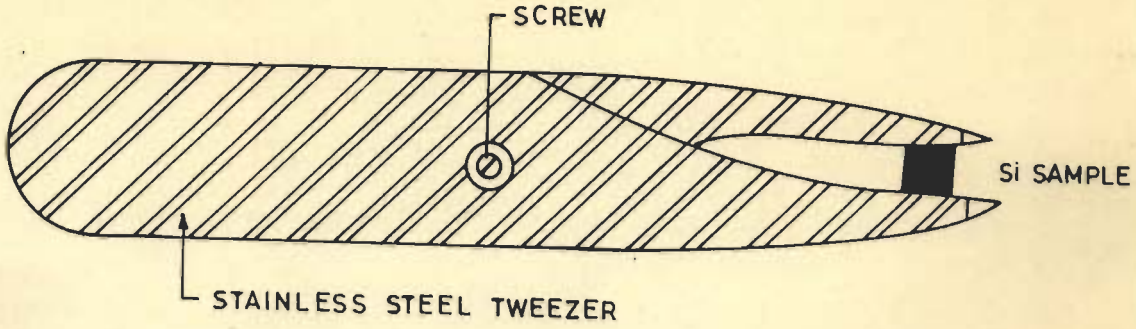


FIG. 3·12– SAMPLE HOLDER

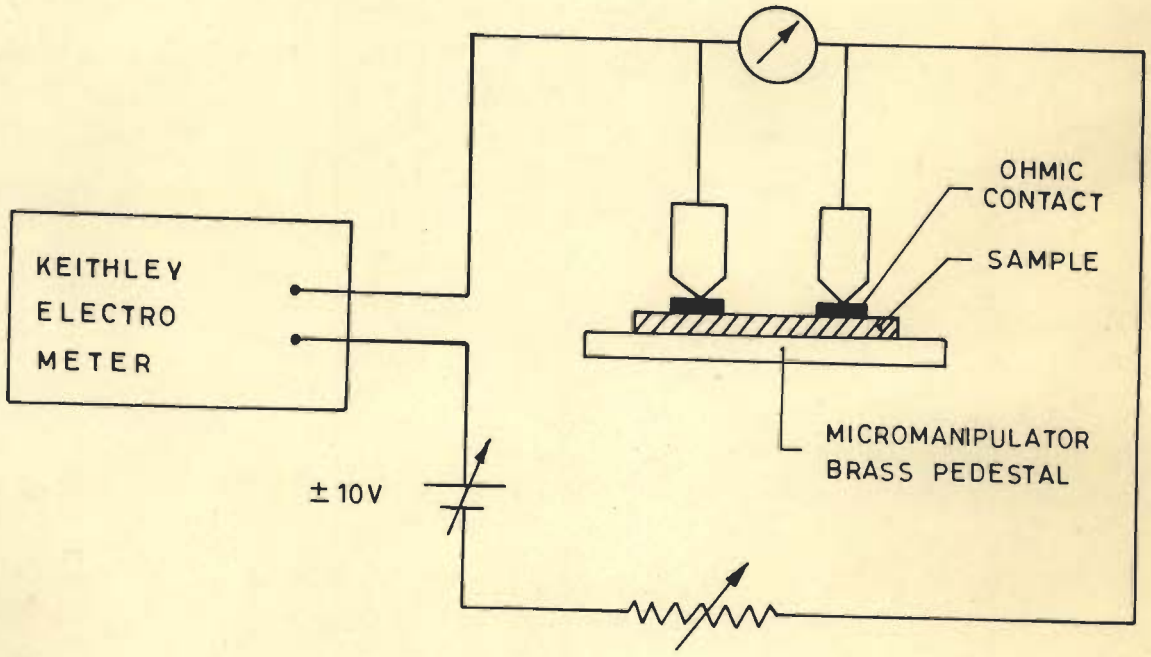


FIG. 3·13 : SCHEMATIC OF V–I CHARACTERISTIC MEASUREMENT

holder of the vacuum coating unit which was fixed just below the radiant heater. After mounting the silicon samples and charging aluminium riders on the source the evacuation of the unit was started. When the pressure reduced to 5×10^{-6} torr, degassing of the system was done by applying the supply voltage to the radiant heater so that its temperature rises to about 300°C. The system was allowed to cool down till a lower pressure is attained. This process of alternate heating and cooling was repeated until the system was completely degassed. Finally as the system attains a stabilised vacuum better than 5×10^{-6} torr the temperature of the tungston source was increased slowly by increasing low tension supply voltage. After waiting for some tome, the temperature was raised to the evaporation point of Aluminium. Some of the aluminium was allowed to evaporate while the shutter was closed between the source and the substrate holder. This was essential to evaporate the impurities which might have left on the surface of source and the material. The samples were then exposed to aluminium evaporation by removing the shutter. The rate of evaporation of aluminium was controlled by controlling the source temperature. The thickness of deposited film was monitored by the crystal thickness monitor fitted in the vacuum coating unit. As soon as the film of desired thickness that is 2000 A° was deposited on the samples the deposition was stopped by

closing the shutter and the source supply was reduced to zero. The system was allowed to cool down to the room temperature. A heated molybdenum strip was used for alloying the aluminium film to the silicon. The strip was thoroughly cleaned by boiling in trichloroethylene and ultrasonirated in acetone. the Bell Jar of the vacuum coating unit was opened and the cleaned molybdenum strip was connected between the low-tension electrodes of the unit. The samples were taken out from the sample holder and placed over the molybdenum strip, the side of the samples having deposited aluminium film was in touch with the molybdenum strip. The Bell Jar was closed and the evacuation of the chamber was started. When the vacuum of the order of 5×10^{-6} torr was stabilised the temperature of the molybdenum strip was raised rapidly upto eutectic temperature of 577°C by increasing the low tension voltage supply. After maintaining the temperature at 577°C for 30 seconds the low tension supply was closed. The temperature was monitored by a thermocouple whose temperature sensing tip was in contact with molybdenum strip at the point where the samples were placed on the strip. After the alloying the system was allowed to cool down upto the room temperature and the samples were taken out.

To evaluate the performance of ohmic contacts thus formed were characterized by measuring the V-I curve and the contact resistance. For this purpose two ohmic

contact points of the diameter 0.2 cm were fabricated as described above on the back side of the epitaxial wafer which is heavily doped having a resistivity of 0.005 ohm-cm (doping concentration 2×10^{19} cm^{-3}). The two ohmic contact points were separated by a distance of 0.6 cm apart. For measuring the V-I characteristics a micromanipulator was designed. The design details are given in Appendix A). The circuit diagram used for the measurement of V-I characteristics is shown in Fig. 3.13. A variable dc voltage source (± 10V) was used to supply the suitable bias voltage. A Keithley electrometer model 610C was used for measuring the forward and reverse currents. The entire set up was placed in an electrically shielded metallic box to minimise the effects of noise etc. as shown in Fig.3.14. The V-I characteristics of the sample having two ohmic contacts on the N^+ side of the silicon wafer were measured under forward as well as reverse bias condition. The observed results are shown in fig. 3.15 which shows that the current increases linearly with the rise of voltage in both directions, the measured value of contact resistance is 4.905 ohm.

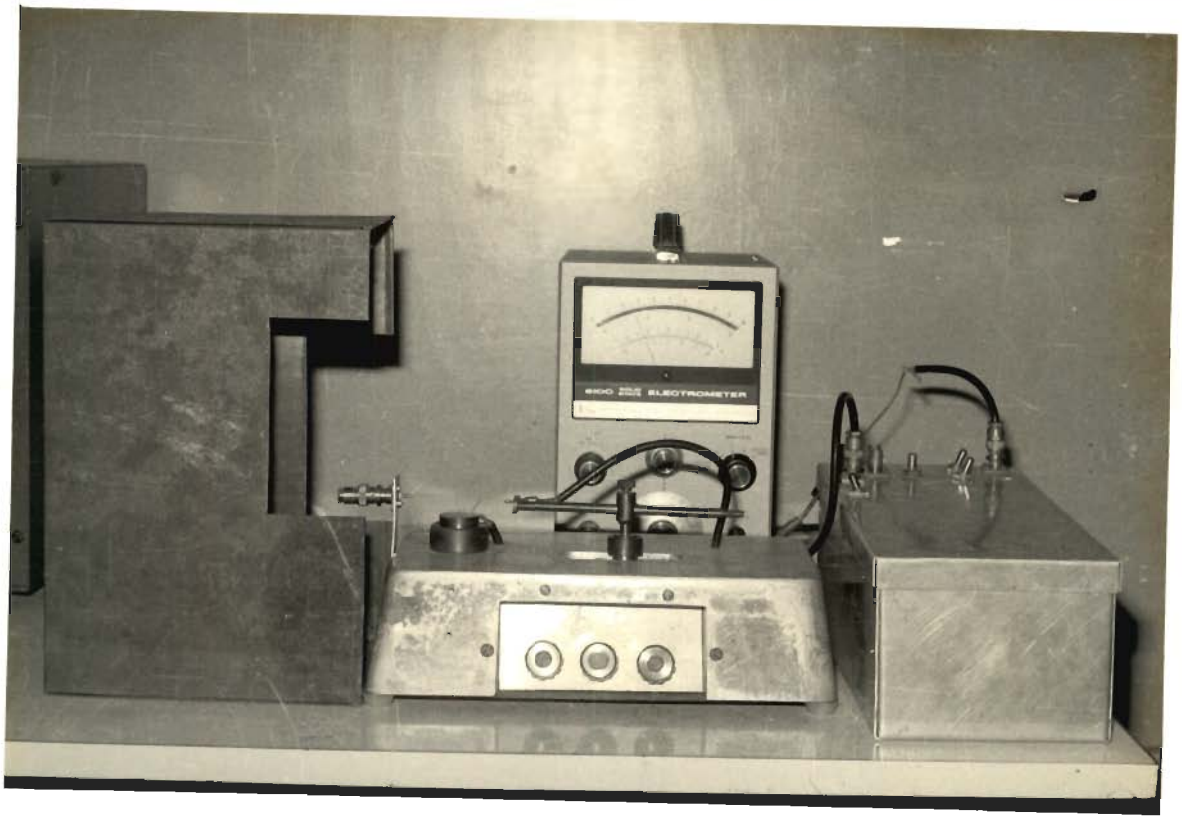


FIG. 3.14 : EXPERIMENTAL ARRANGEMENT FOR V-I CHARACTERISTIC MEASUREMENTS

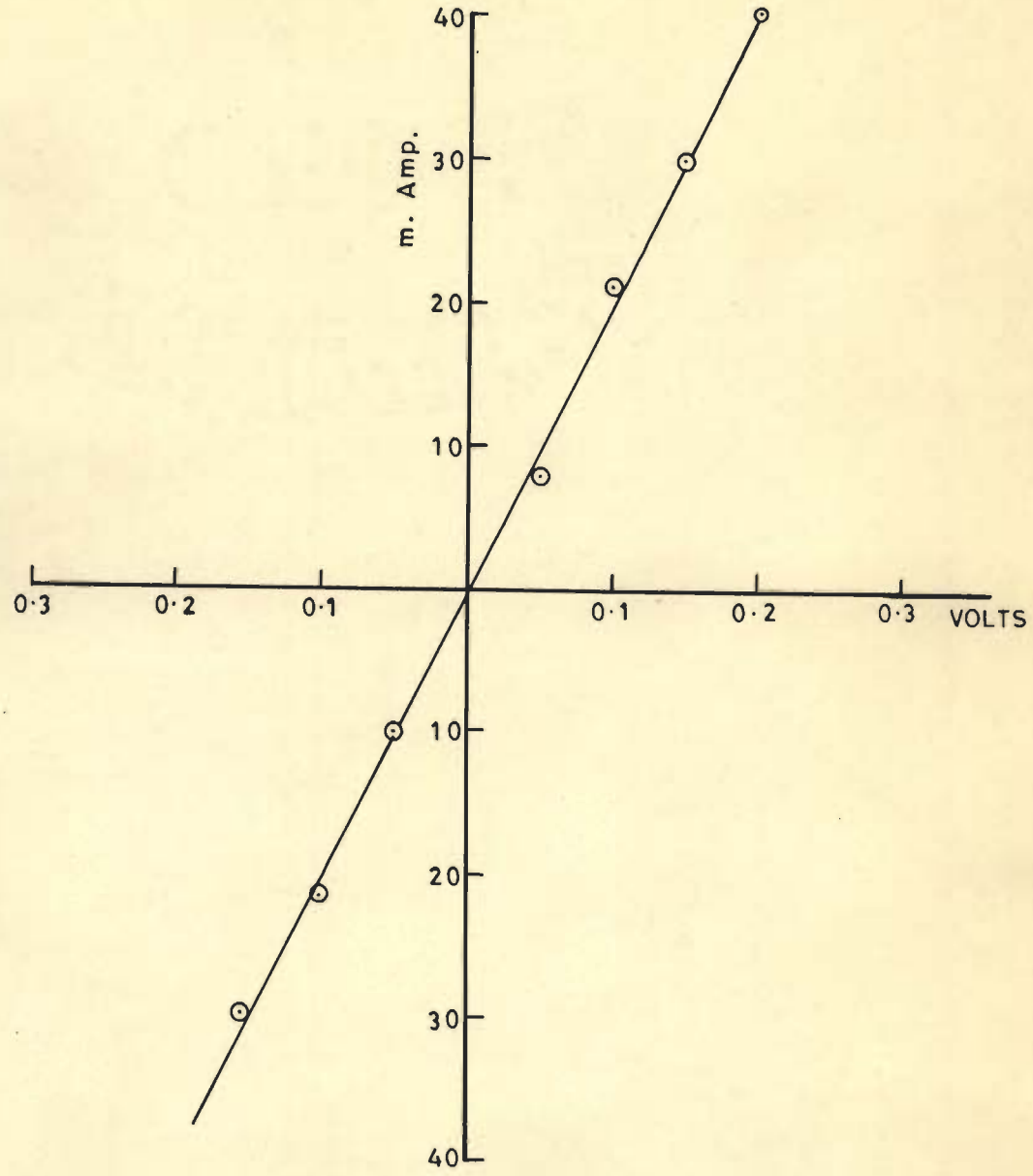


FIG. 3·15: V-I CHARACTERISTIC OF THE OHMIC-CONTACT

CHAPTER IV

CHARACTERIZATION OF ANODICALLY GROWN SiO_2 LAYERS AND Si - SiO_2 INTERFACES

4.1 INTRODUCTION

The performance of MOS system depends on the electrical properties of the oxide film grown and the interfacial properties of oxide-semiconductor interface. To evaluate the electrical and interfacial properties of the oxide layers the C-V, G-V and I-V characteristics of the fabricated MOS samples were investigated and studied. To calculate the interface state density the conductance method suggested by Nicollian and Goetzberger [74] was used. The dielectric breakdown strength was measured for catastrophic breakdown of the fabricated MOS samples.

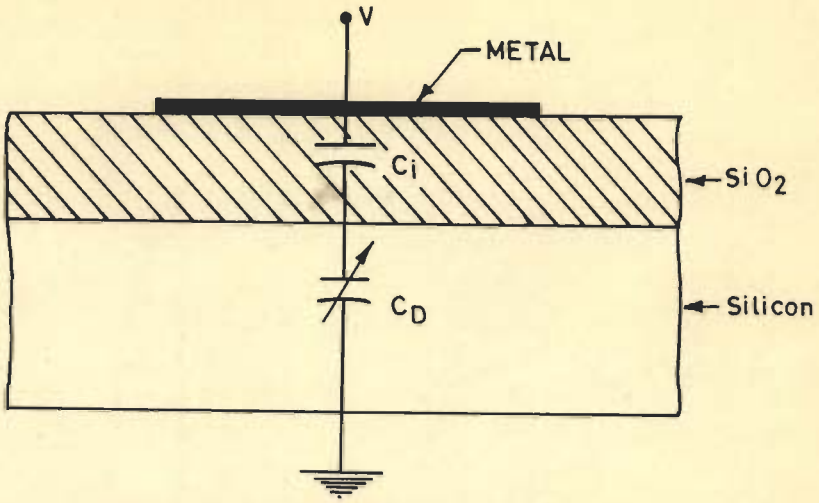
4.2 SURFACE STATES

Surface states or interface states are defined as energy levels within the forbidden band gap of the semiconductor. These states can exchange charges with the semiconductor in a short time or long time. The surface states have been theoretically studied by Tamm [75], Shockley [76] and others [77], [78] and have been shown to exist within the forbidden gap of the semiconductor due to the interruption of the periodic lattice structures

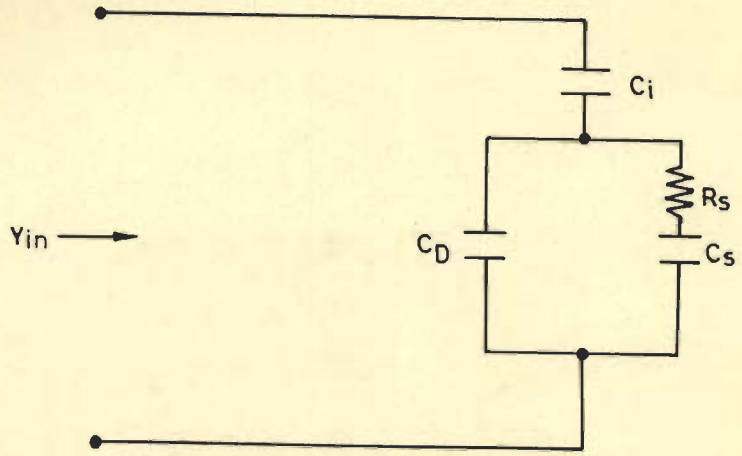
at the surface of a crystal. The existence of surface states was first observed by Shockley and Person [79]. Surface states have been classified into fast and slow states. The fast states exchange charge with the conduction or valence band rapidly, and are assumed to lie close to the semiconductor - Insulator interface. Slow states, on the other hand, exist at the interface of the air and insulator and require a longer time for charge exchange. The present investigations deals only with the surface states or interface states at the insulator-semiconductor interface, which comes under the category of fast states.

The basic equivalent circuit [80] of the MOS structure incorporating the surface states effect is shown in Fig.4.1(b), C_i and C_D respectively represent the capacitances arises due to the insulator and the semiconductor depletion- region. C_s and R_s are the capacitance and resistance associated with the surface states which depend on the value of the surface potential. The product $C_s R_s$ is defined as the surface state lifetime which determines the frequency behavior of the surface states. The parallel branch of the equivalent circuit in fig, 4.1(b) can be converted into a frequency dependent capacitance C_p in parallel with a frequency-dependent conductance G_p as shown in Fig. 4.1(c) where

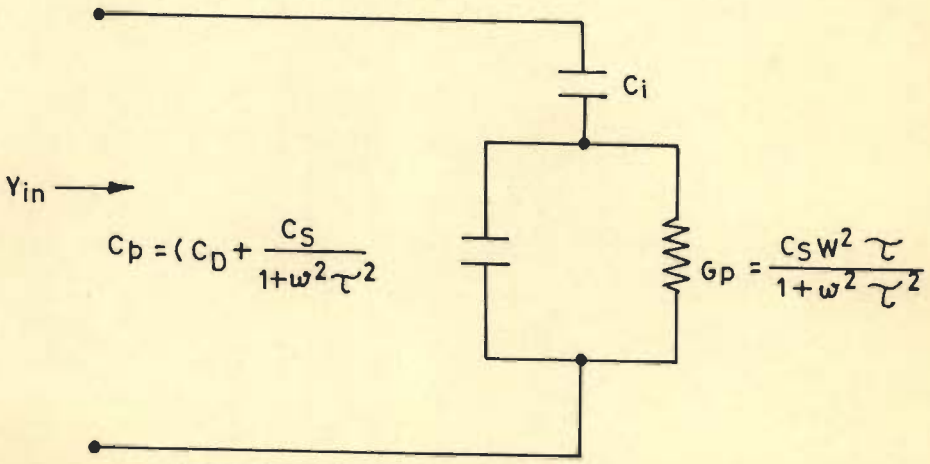
$$C_p = C_D + \frac{C_s}{1 + \omega^2 \tau^2} \qquad \ldots (4.1)$$



(a) WITHOUT INTERFACE STATES



(b) WITH INTERFACE STATES



(c) THE PARALLEL BRANCH OF b CONSISTING OF FREQUENCY DEPENDENT C_p AND FREQUENCY DEPENDENT G_p

FIG. 4.1: EQUIVALENT CIRCUIT OF A MOS CAPACITOR

and

$$\frac{G_p}{\omega} = \frac{C_s \omega \tau}{1 + \omega^2 \tau^2} \qquad \ldots (4.2)$$

where,

$$\tau \equiv C_s R_s .$$

The input admittance Y is given by

$$Y_{in} = G_{in} + j\omega C_{in} \qquad \ldots (4.3)$$

where,

$$G_{in} = \frac{\omega^2 C_s \tau C_i^2}{(C_i + C_D + C_s)^2 + \omega^2 \tau^2 (C_i + C_D)^2} \qquad \ldots (4.4)$$

$$C_{in} = \frac{C_i}{c_i + C_d + C_s}\left[C_D + C_s \frac{(C_i + C_D + C_s)^2 + \omega^2 \tau^2 C_D (C_i + C_D)}{(C_i + C_D + C_s)^2 + \omega^2 \tau^2 (C_i + C_D)^2}\right] \qquad \ldots (4.5)$$

To evaluate the surface states one can either use the capacitance measurement or the conductance measurement since eqs. (4.4) and (4.5), both the input conductance and the input capacitance contain similar information about the surface states. The evaluation of surface-state density using capacitance measurement can be achieved, by differentiation procedure suggested by Terman [81], the integration procedure proposed by Berglund [82] or the temperature procedure proposed by Gray and Brown [83].

The capacitance technique, however, has severe limitations [84]. The main difficulty is that interface state

capacitance is extracted from measured capacitance which consists of oxide capacitance, depletion layer capacitance, and interface state capacitance. This difficulty does not apply to the equivalent parallel conductance because conductance arises solely from the steady-state loss due to the capture and emission of carriers by interface states and is thus, a more direct measure of these properties [80]. Conductance measurements yield more accurate and reliable resutls.

4.3 CONDUCTANCE METHOD

The priciple of the MIS conductance technique is based on the simplified equivalent circuit shown in Fig.4.1(c). The admittance of the MIS diode is measured by a bridge. The insulator capacitance is measure by a bridge. The insulator capacitance is measured in the region of strong accumulation. The admittance of the circuit is then converted into an impedance. The reactance of the insulator capacitance is subtracted from this impedance and the resulting impedance converted back into an admittance. This leaves C in parallel with the series $C_s R_s$ network of the surface states. The capacitance and equal parallel conductance divided by ω are given by eqs. (4.1) and (4.2). Equation (4.2) i.e. $\frac{G_p}{\omega} = \frac{C_s \omega \tau}{(1+\omega^2\tau^2)}$ is independent of the C_D and is purely a function of τ, C_s and ω, moreover value of G_p/ω is maximum at a frequency ω_{max} when $\omega_{max}\tau = 1$. At a given bias voltage G_p/ω can be measured as a

function of frequency and plotted against $\omega\tau$. Knowing the maximum value of $\frac{G_p}{\omega} = \frac{C_s}{2}$ and the frequency ω_{max}, C_s and $\tau = C_s R_s = \frac{1}{\omega_{max}}$ can be determined from the measured conductance. Once C_s is known, the surface-state density is obtained by using the relation $N_{ss} = \frac{C_s}{qA}$ where A is the metal plate area.

4.3.1 MEASUREMENT OF THE EQUIVALENT PARALLEL CONDUCTANCE (G_p) OF THE MOS CAPACITOR

The following precautions were taken while carrying out the conductance measurement for determining the interface state densities.

- The maximum swing of the surface potential caused by the applied a.c. signal should be less than KT/q volts, to avoid the effects of harmonics generated due to the non-linear characteristics of the MOS structures at higher voltages.

- The values of conductance measured vary from few nano-mhos to 10 μmhos. Such small conductance values require that current leakage path along the air-oxide interface should be minimum. Therefore the measurement should be conducted in a well shielded and grounded chamber having dry atmosphere.

- To avoid scratching in the field plate, a gold

wire of diameter 125 micron mounted on a micro-manipulator was used to make electrical contact to the field plate.

Boonton Direct capacitance Bridge Model No. (75C-523) shown in Fig. 4.2 was used to measure small signal differential capacitance over the range 1-1000 PF and small signal equivalent parallel conductance from about 1 nano-mho-1 mho over the frequency range 5-500 KHz. To avoid the effect of stray capacitance a coaxial cable was used between MOS capacitor and the bridge terminal. The length of the cable was kept just sufficient i.e. less than 30 cms. Boonton-Bridge uses three-terminals for capacitance and conductance measurements of the MOS samples. Two terminals are for connecting the MOS capacitor and the third terminal is for grounding the metal enclousre surrounding the MOS capacitor. Further care was taken to choose the following parameters.

1. Frequency
2. Signal Amplitude
3. Gate Bias.

To avoid spurious conductance and capacitance values, due to harmonics of the signal frequency, for all measurements signal level of 30 mv was maintained throughout the frequency range. The signal voltage amplitude

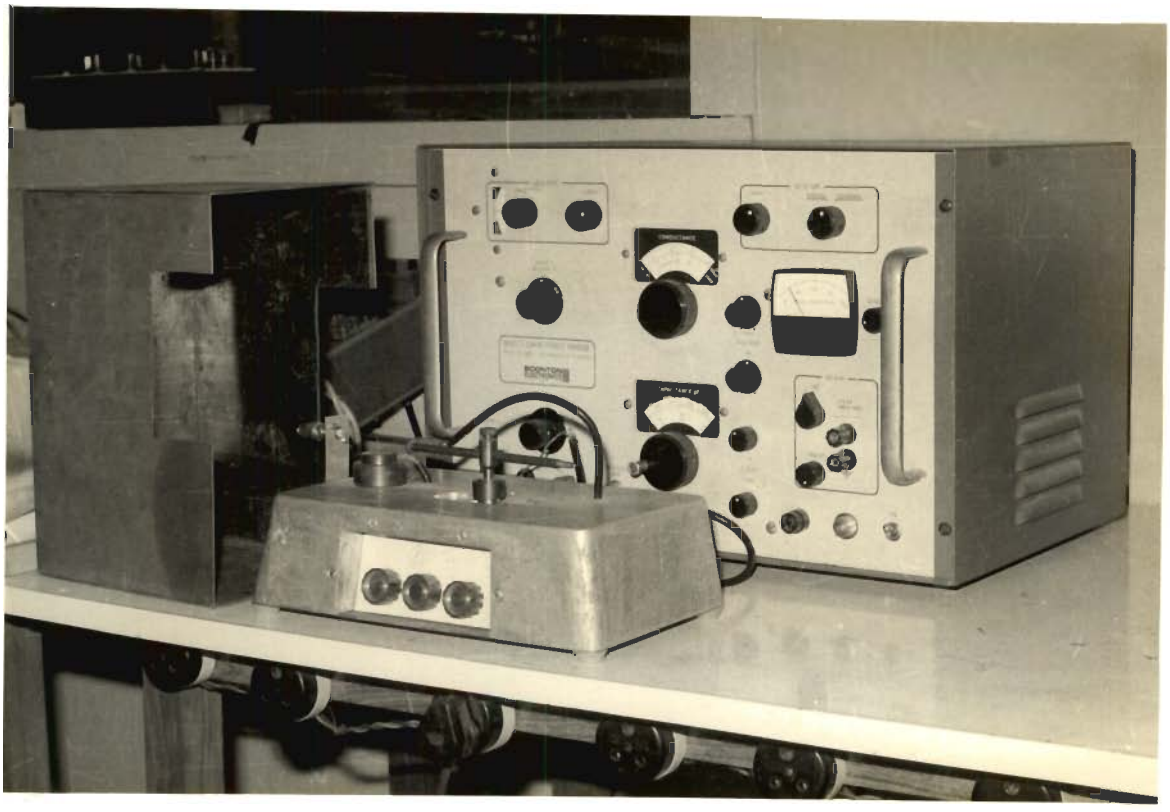


FIG. 4·2 : BOONTON BRIDGE

was measured and readjusted whenever the frequency was changed. During readjustments signal amplitude was monitored by an oscilloscope.

Gate bias voltage was measured using high input impedance D.C. micro voltmeter (Philips pp 9004). Gate bias voltage was measured across the MOS capacitor rather than across the supply voltage as the gate bias is supplied to the MOS capacitor through a voltage divider in the bridge which draws current from the bias supply.

Due to the non-availability of equipments measurements were carried out only over the frequency range of 5 KHz to 500 KHz. It is important to use an oxide layer as thin as practicable to get large values of capacitance and equivalent parallel conductance for a given N_{ss} and to minimize the error in extracting C_i. The MOS A.C. conductance technique gives the most accurate results. Due to this fact the work in this disseration is based almost entirely on conductance method.

4.4 DETERMINATION OF THE ENERGY POSITION OF THE SURFACE STATE DENSITIES (N_{ss}) ACROSS THE BAND GAP OF SILICON

The relation between surface potential ψ_s and the applied gate voltage V was obtained with the help of the high frequency experimental and theoretical C-V curves for a given oxide thickness [85].

The relation between the surface potential ψ_s and the energy postion E of the surface state density under investigation was obtained [86] from the equation.

$$E = E_F + q\,\psi_s$$

The energy position E under investigation is determined both by the position of the Fermi level and by the surface potential. Surface potential is varied by bias voltage, and the Fermi level depends on the temperature. The value of Fermi energy at room temperature is taken from the book of Paul Richman [87].

4.5 EXPERIMENTAL RESULTS AND DISCUSSIONS

Capacitance and conductance measurements were carried at frequencies 5 KHz, 10 KHz, 50 KHz, 100 KHZ, 200 KHz, 300 KHz, 400 KHz and 500 KHz with the help of Boonton Direct capacitance bridge (Model No. 75C-S23) Signal amplitude was maintained at about 30 mv to have small-signal conditions. The experimental C-V curves were compared with the theoretical one, C-V curves (Fig.4.3) shows that the accumulation, depletion and inversion regions of the experimental curve are on the left side (negative voltage side) of the theoretical curve. This indicates [88, 89] that the donor types of surface states were present in the upper-half of the Si band gap in the

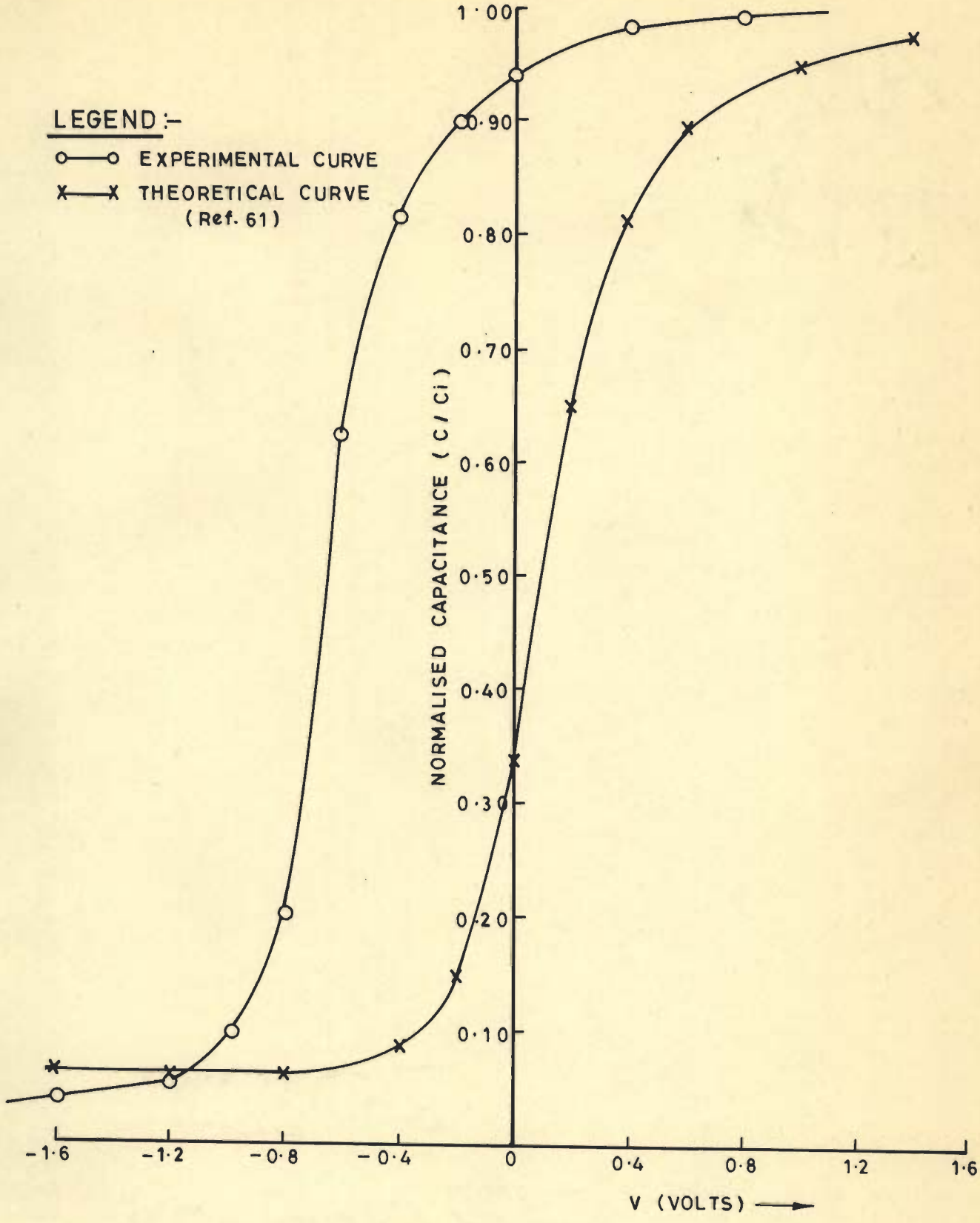


FIG. 4·3 : THEORETICAL AND EXPERIMENTAL C-V CURVES FOR OXIDE THICKNESS OF 300 A°

fabricated MOS structures. The presence of exclusively donor like surface state in the band gap will always result in net positive change in the states. This in turn will shift the C-V curves to the negative voltage side. Shifting or frequency dispersion of the curves depend on both the location and the manitude of these states in the band gap.

Figs. (4.4 to 4.7) shows the measured C-V curves for different samples fabricated in the laboratory having Sio_2 film thickness of the order of 300 A°,600A° 900A° and 1200A° respectively. It is observed that C-V curves are well defined. The curves show saturation in the inversion region mode at negative bias voltage, then increases in value in the depletion mode as the bias voltage is made less negative,and then become saturated at the oxide capacitance value in the accumulation mode at positive bais voltage. Frequency dispersion is almost negligible in sample having a film thickness of the order of 300 A°. In the samples with oxide thickness of the order of 600A° and 900A° frequency dispersion is observed in the accumulation and depletion regions. As the film thickness is further increased to a value of 1200A° frequency dispersion is osbserved in the inversion region also. The frequency dispersion effect is most probably due to the limited capability of the surface states to follow the A.C. probing signals of

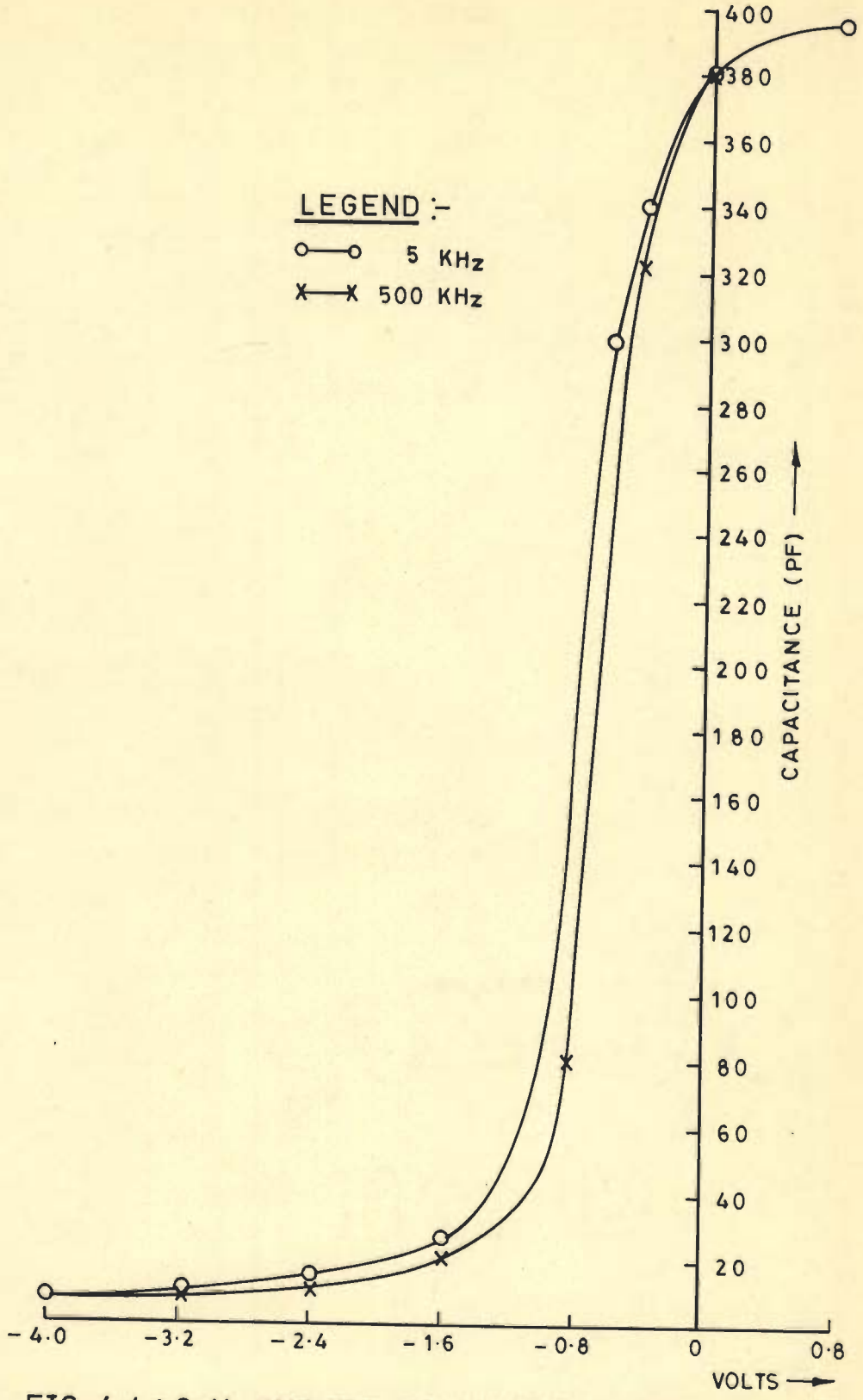


FIG. 4·4 : C-V CURVES FOR VARIOUS FREQUENCIES: OXIDE THICKNESS OF THE ORDER OF 300 A°

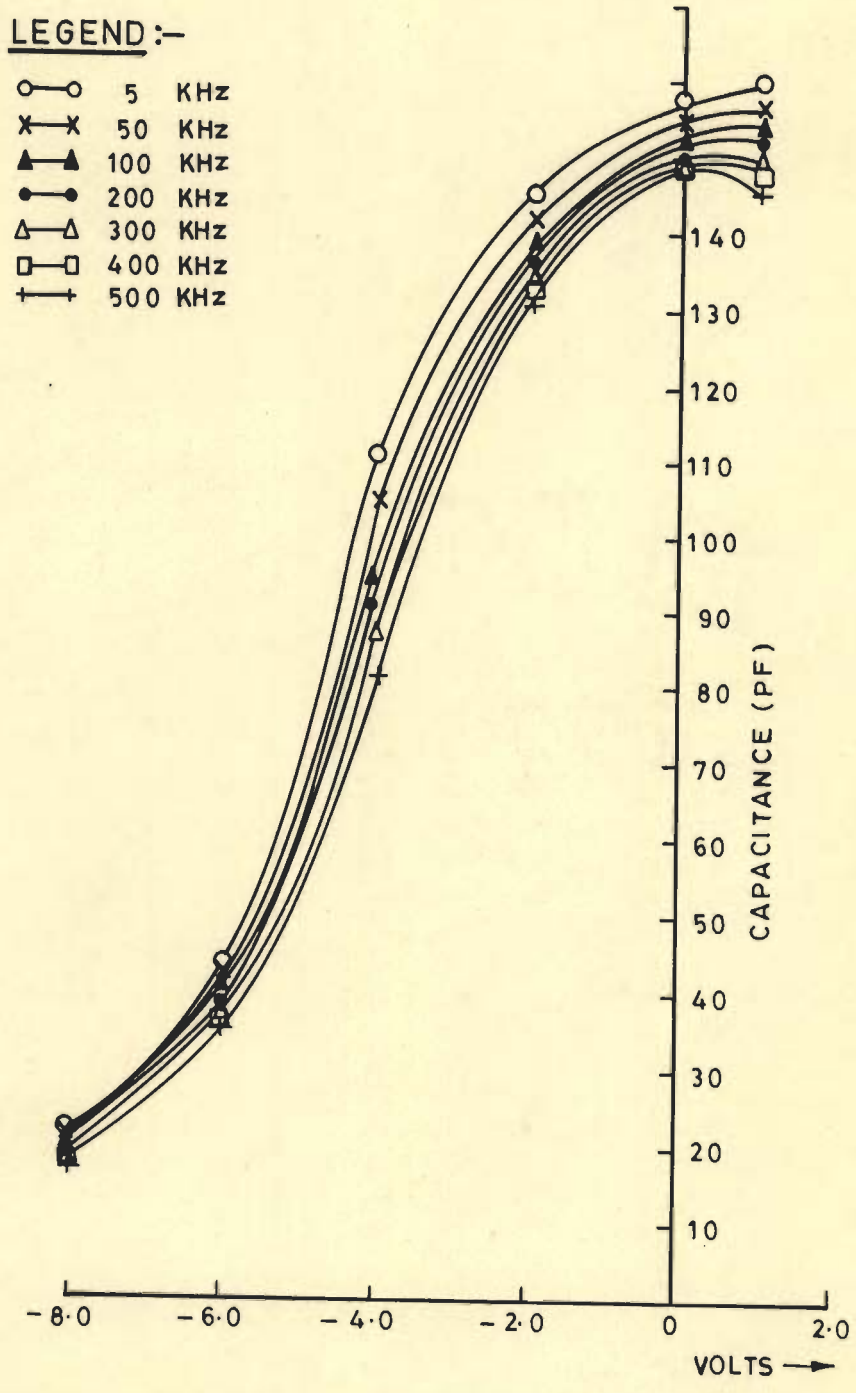


FIG. 4·5 : C-V CURVES FOR VARIOUS FREQUENCIES: OXIDE THICKNESS OF THE ORDER OF 600 A°

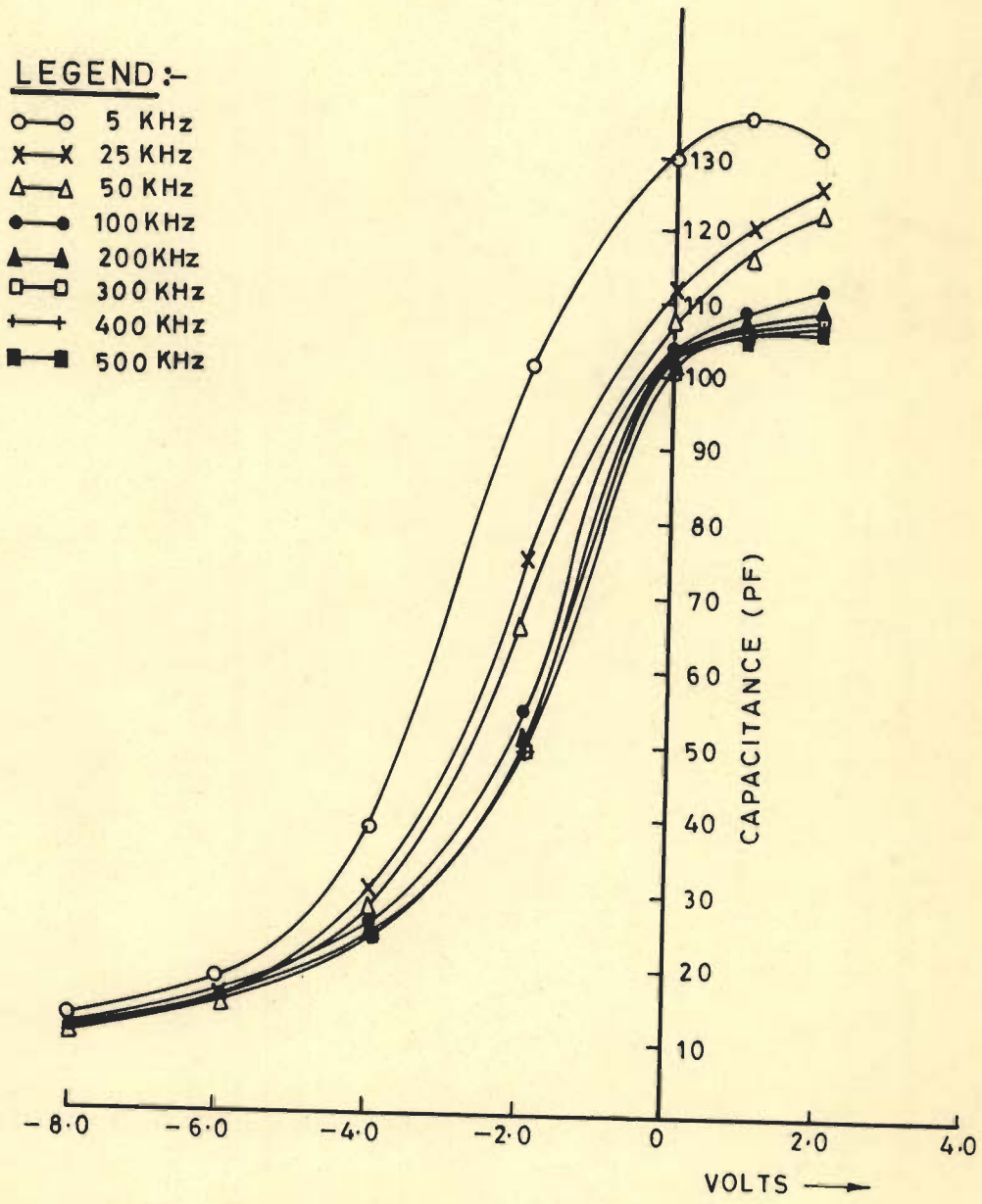


FIG. 4·6 : C-V CURVES FOR VARIOUS FREQUENCIES : OXIDE THICKNESS OF THE ORDER OF 900 A°

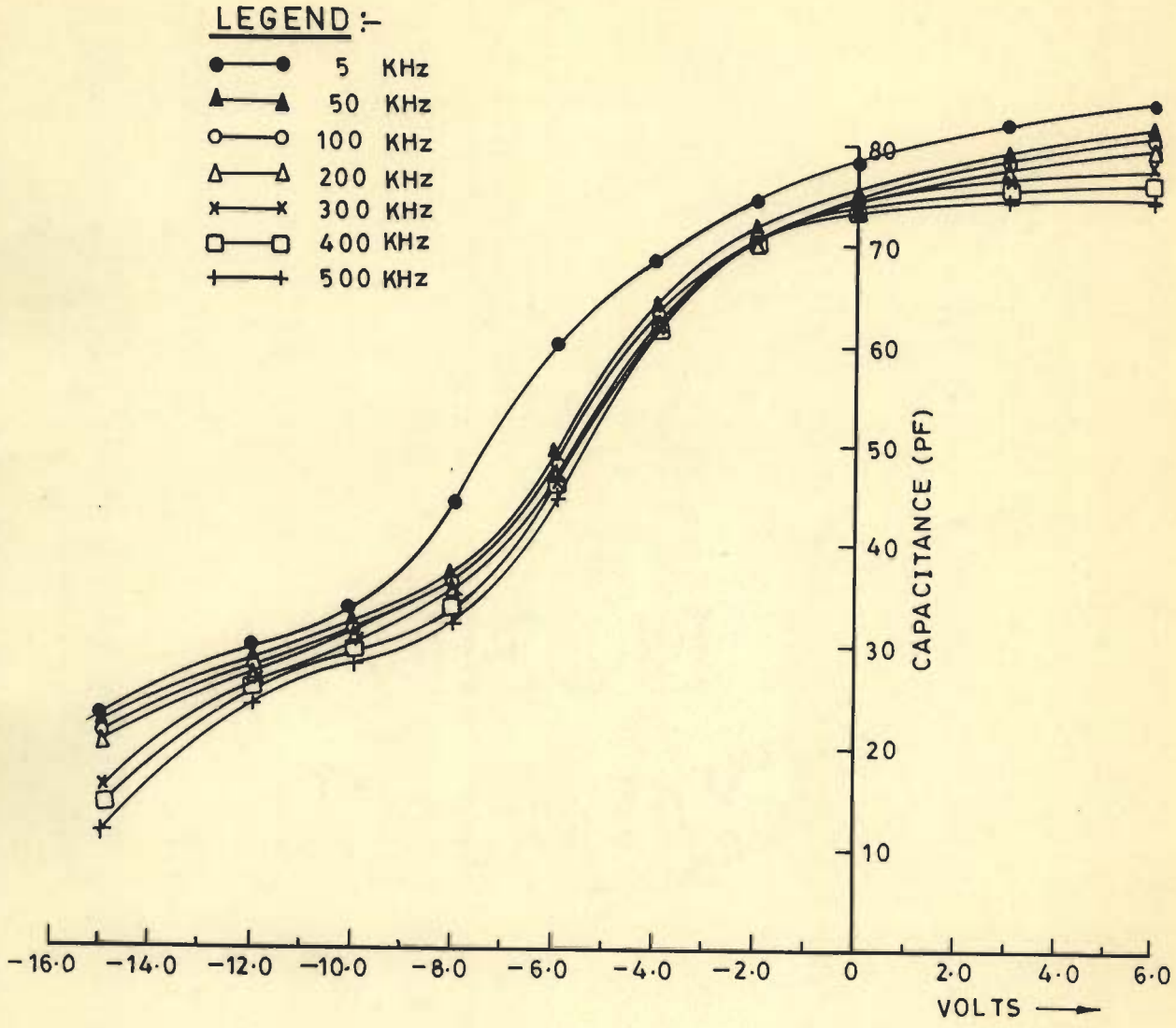


FIG. 4·7 : C-V CURVES FOR VARIOUS FREQUENCIES : OXIDE THICKNESS OF THE ORDER OF 1200 A°

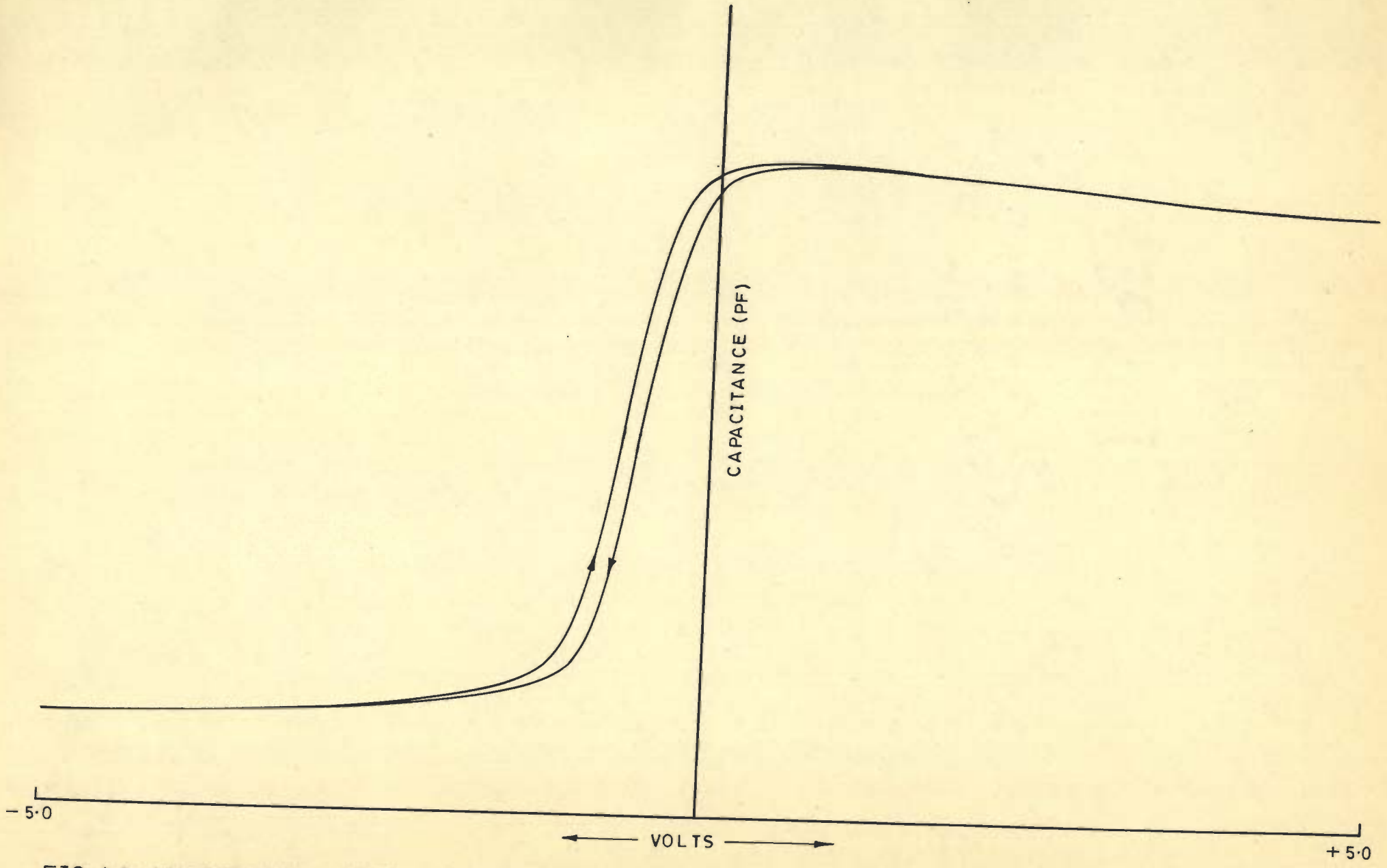


FIG. 4·8 : HYSTERESIS EFFECT IN THE MOS SAMPLE WITH OXIDE THICKNESS 300 A°

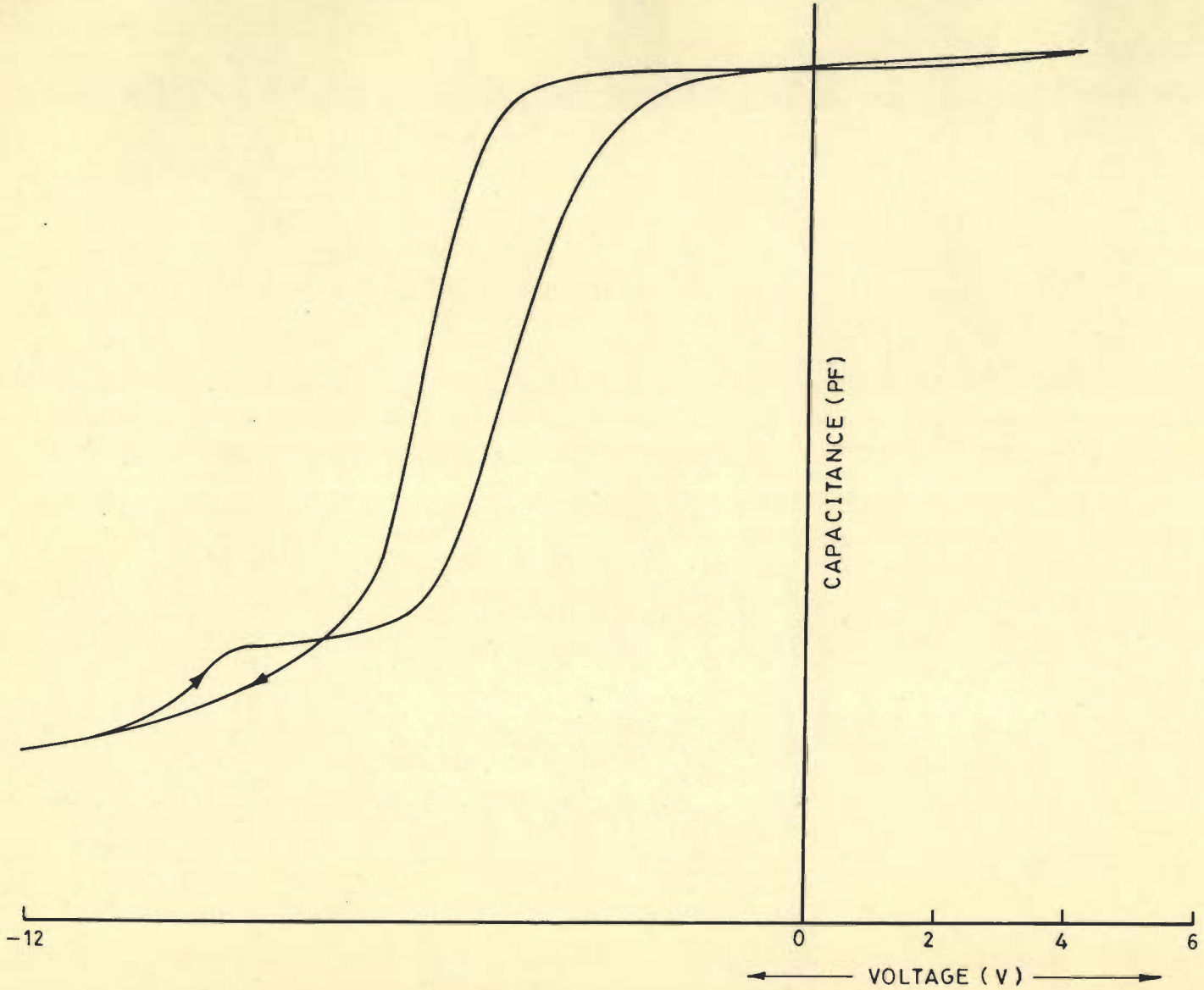


FIG. 4·9 : HYSTERESIS EFFECT IN THE SAMPLE WITH OXIDE THICKNESS 1200 A°

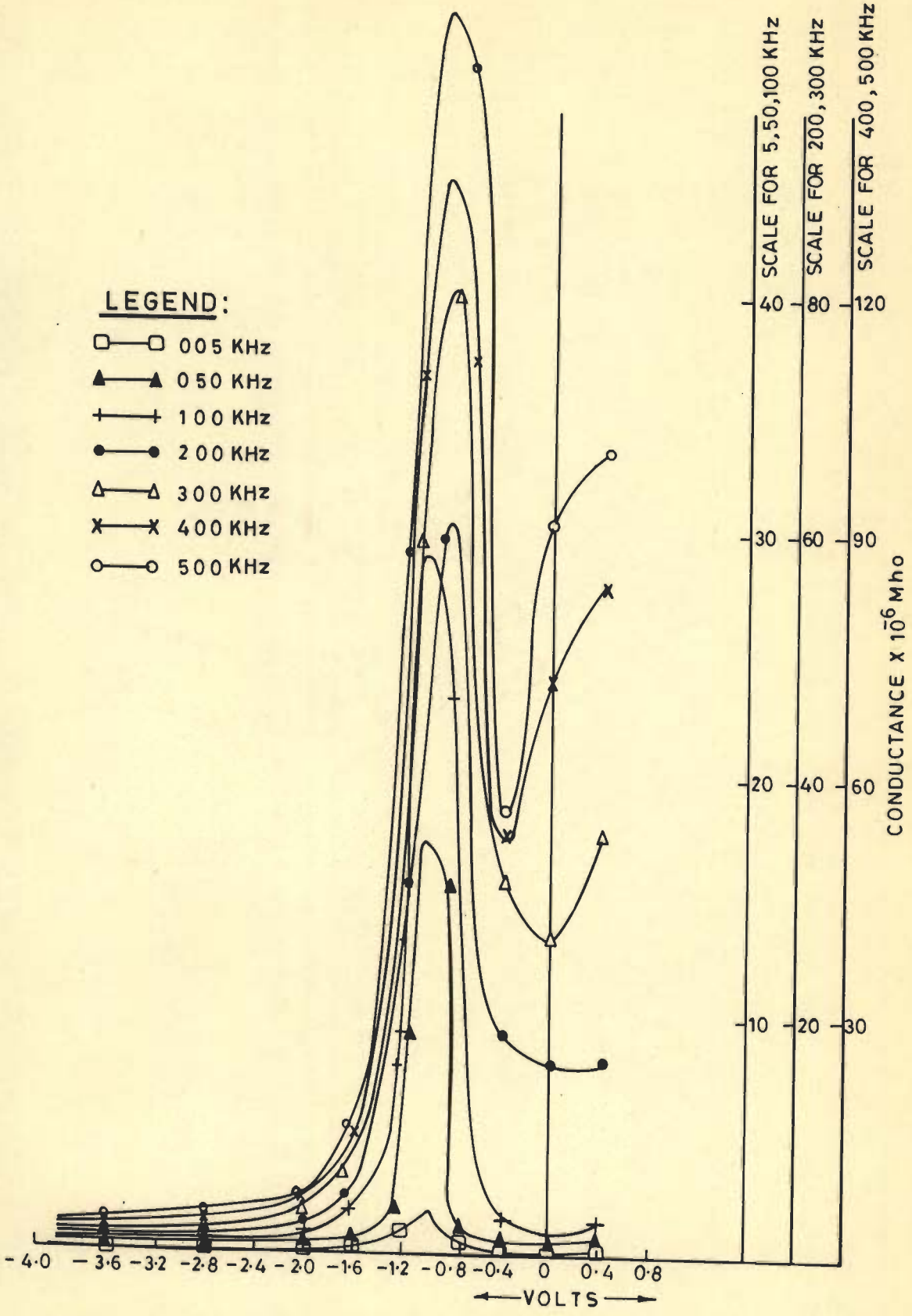


FIG. 4·10 : G-V CURVES FOR VARIOUS FREQUENCIES : OXIDE THICKNESS OF THE ORDER OF 300 A°

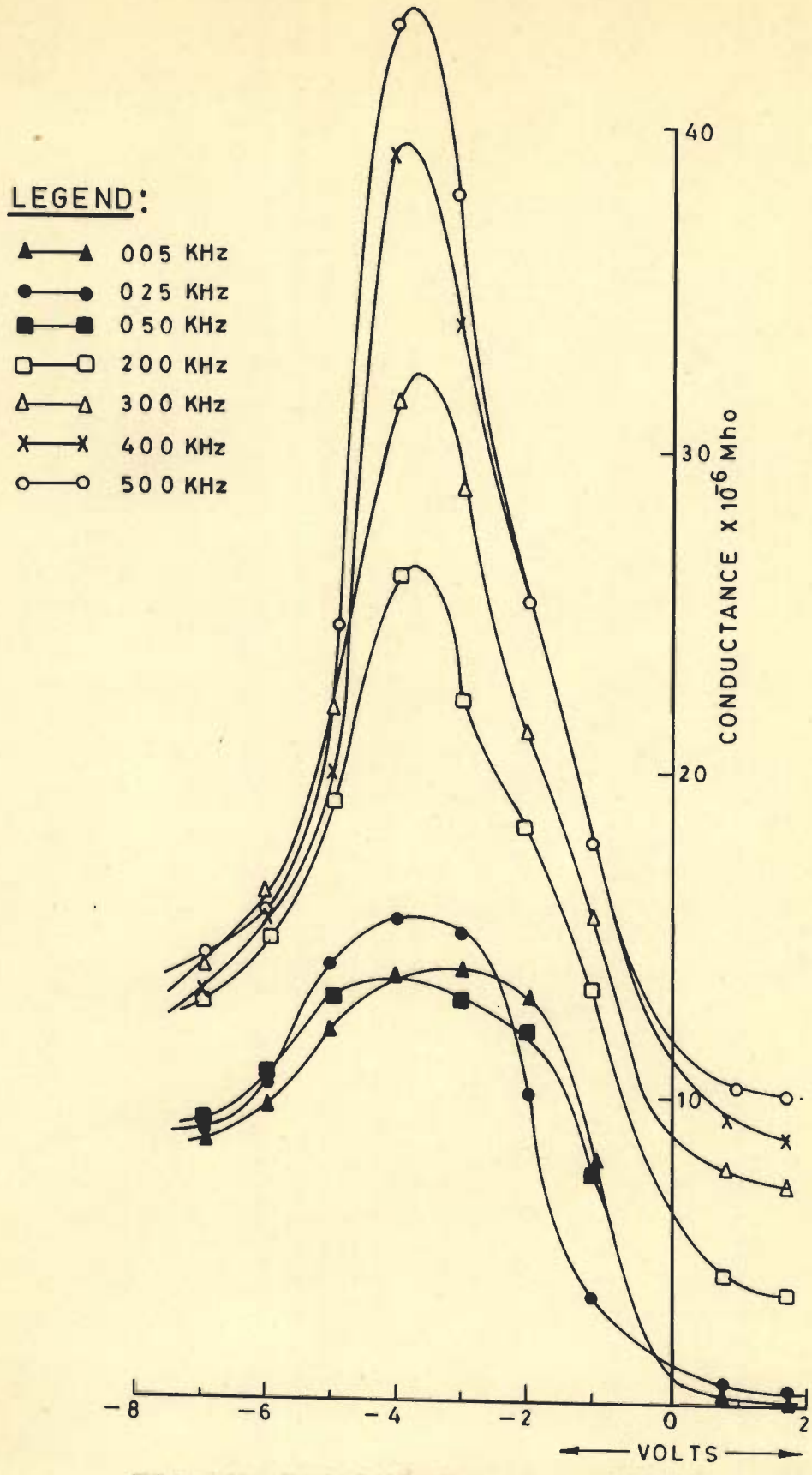


FIG. 4·11: G-V CURVES FOR VARIOUS FREQUENCIES: OXIDE THICKNESS OF THE ORDER OF 600 A°

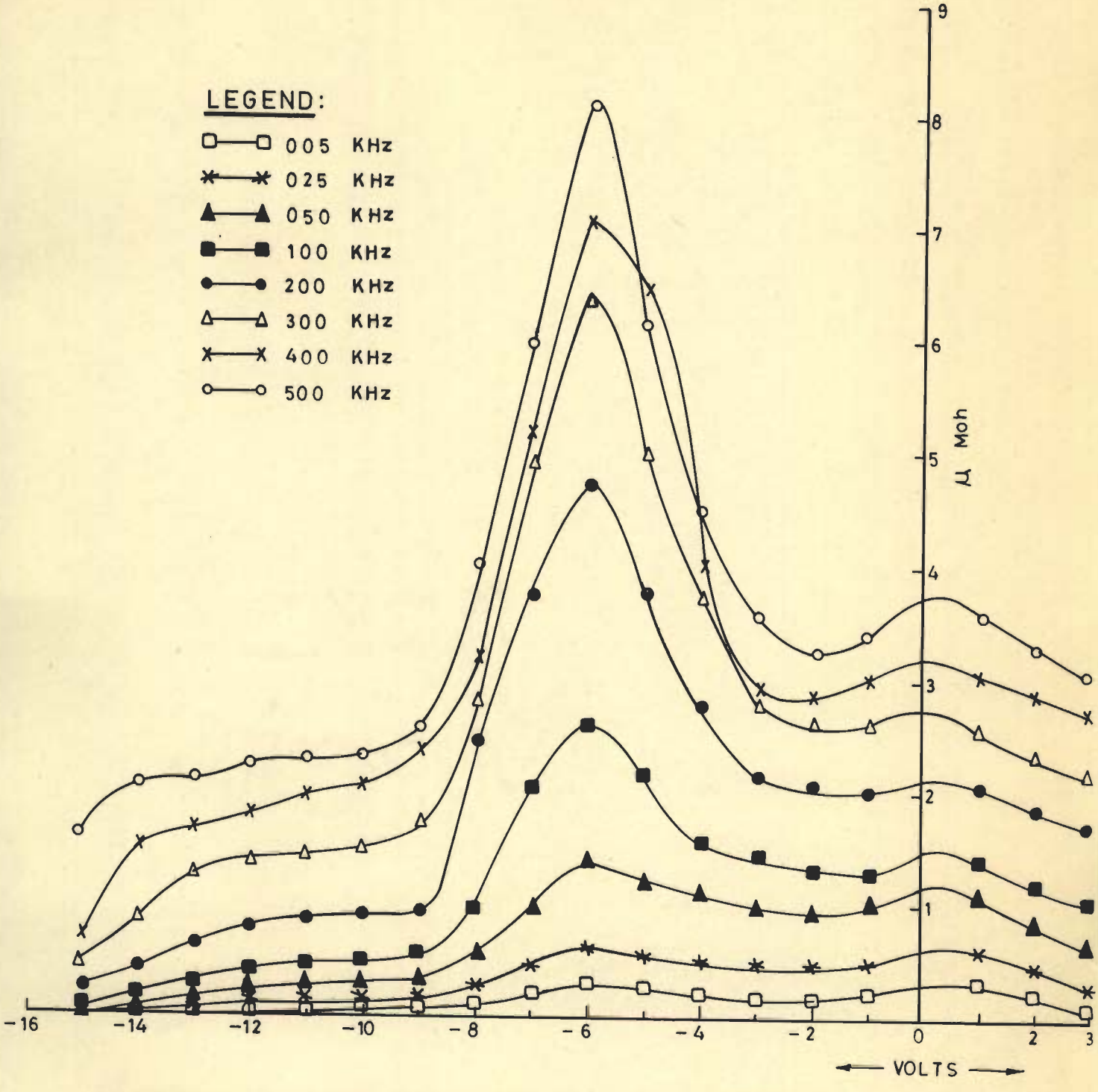


FIG. 4·12 : G-V CURVES FOR VARIOUS FREQUENCIES OXIDE THICKNESS OF THE ORDER OF 1200 A°

different frequencies. The anomalous frequency dispersion may be due to the permittivity of the bulk oxide or the formation of a metamorphic layer near the interface [90] which may be a lossy dielectric. An additional cause of the frequency dispersion could be the Maxwell-Wanger effect [91] according to which the dielectric is considered to be a combination of two layers with different conductivities and dielectric constants. A thin layer of high conductivity may exist between the oxide and the semiconductor (Si). This could be a region of incomplete oxidation and high disroder.

Negligible hysteresis effect is observed in the sample having a film thickness 300A° hysteresis effect is observed as the film thickness (SiO_2) is increased. (Fig. 4.8,4.9).

In Fig.4.10 to 4.12 measured conductance curves (G-V) are plotted. The conductance curves for different signal frequencies show only one peak and approaches zero on either side. The peak magnitude of the equivalent parallel conductance increases with increasing frequency because of Ci in series with the interface trap R-C network. where as the a-c capacitance ariases from variation of the stored charge with the sinusoidal variation of the electrical signal, the ac conductance represents the loss of electrical energy in the charging and discharging

processes. In the MOS structures, the most prominent loss process is the charing and discharging of the interface states. At a given bias voltage, therefore this process occurs in the states lying close to the Fermi-level and which have time constants smaller than or comparable to the time period of the signal frequency. Since the position of Fermi-level with respect to the band edges depends on the surface potential which changes with the bias voltage, by sweeping the bias, different portions of the interface state distribution are probed. Thus the shape of the conductance versus bias voltage curve represents the distribution of interface states and the time constants associated with them.

Figs. 4.13 to 4.16 represents plots of G_p/ω versus frequency for different applied bias voltages as parameter. As the applied voltage changes from the accumulation to depletion and subsequently to inversion regions the magnitude of the peak changes. For samples having film thickness 900A° and 1200A° we were unable to get peaks within our measurement frequency range, the lower limit of which was 5 KHz and upper limit was 500 KHz.

Figs. 4.17 to 4.20 gives theplot of surface state density observed from the conductance technique and its distribution in the energy band gap. The interface state

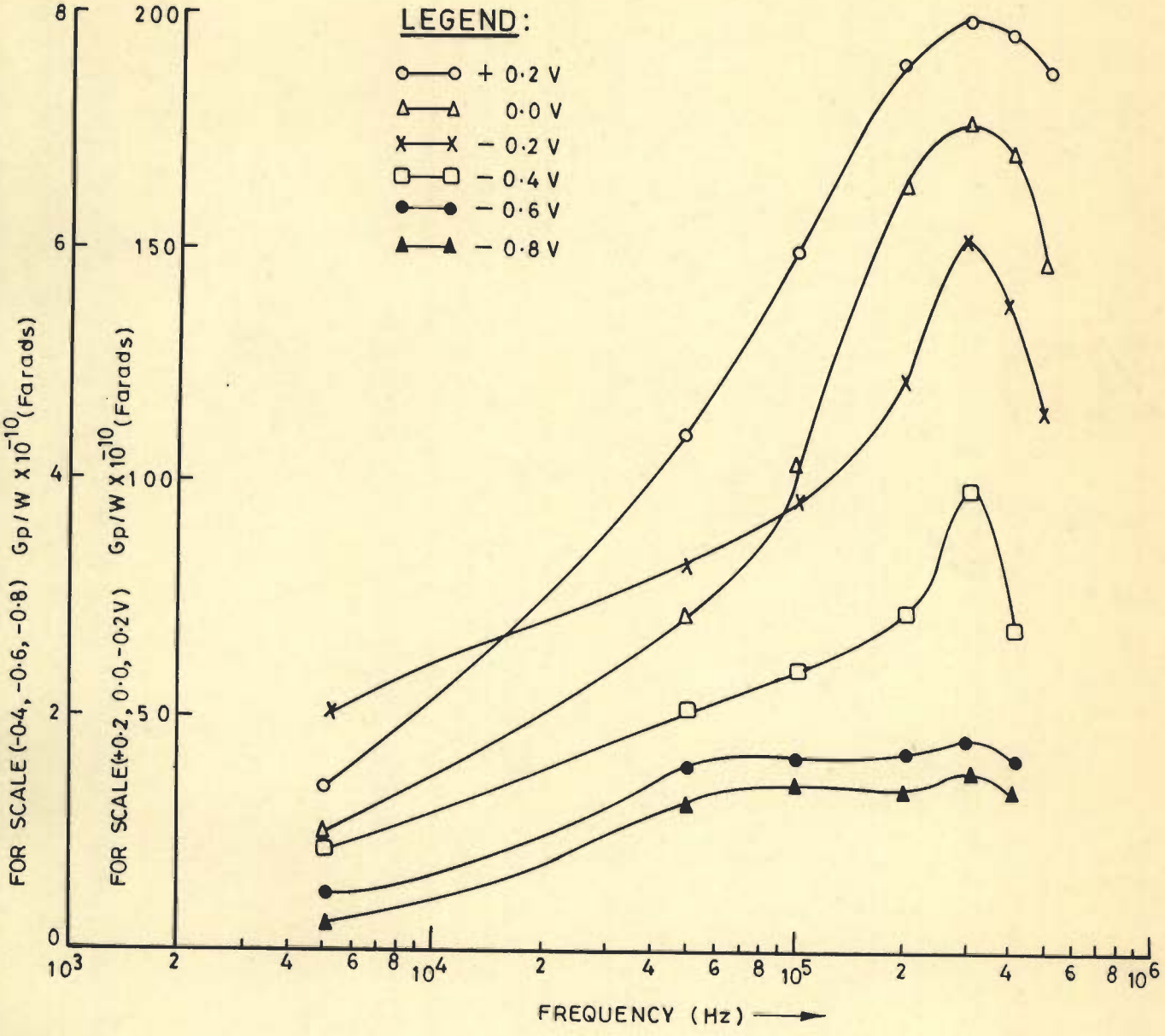


FIG. 4·13 : VARIATION OF PARALLEL CONDUCTANCE (G_p/ω) WITH FREQUENCY AT SEVERAL GATE VOLTAGES FOR MOS SAMPLES SiO_2 THICKNESS OF THE ORDER OF 300 A°

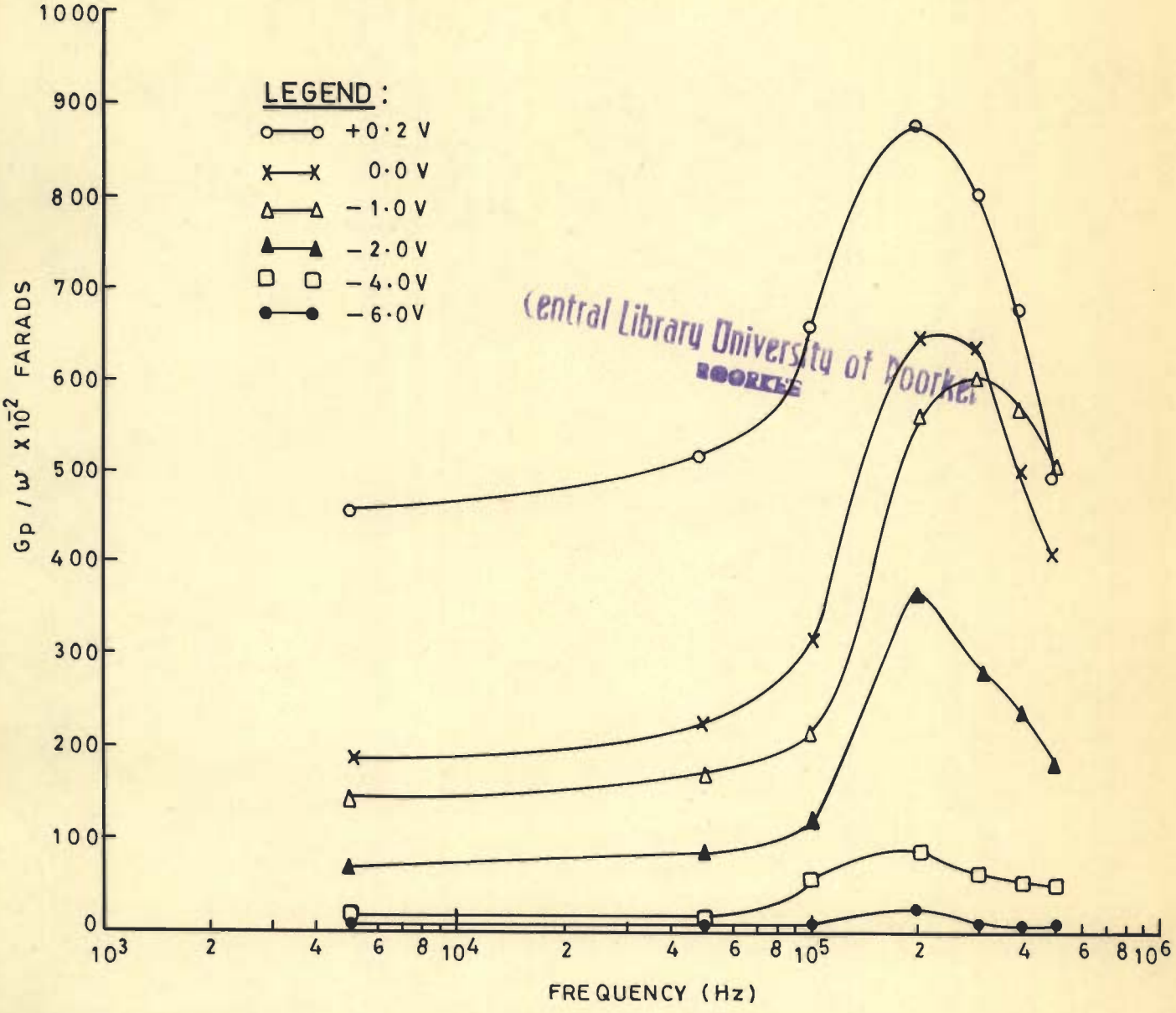


FIG. 4·14 : VARIATION OF PARALLEL CONDUCTANCE (G_p/ω) WITH FREQUENCY AT SEVERAL GATE VOLTAGES FOR MOS SAMPLES SiO_2 THICKNESS OF THE ORDER OF 600 A°

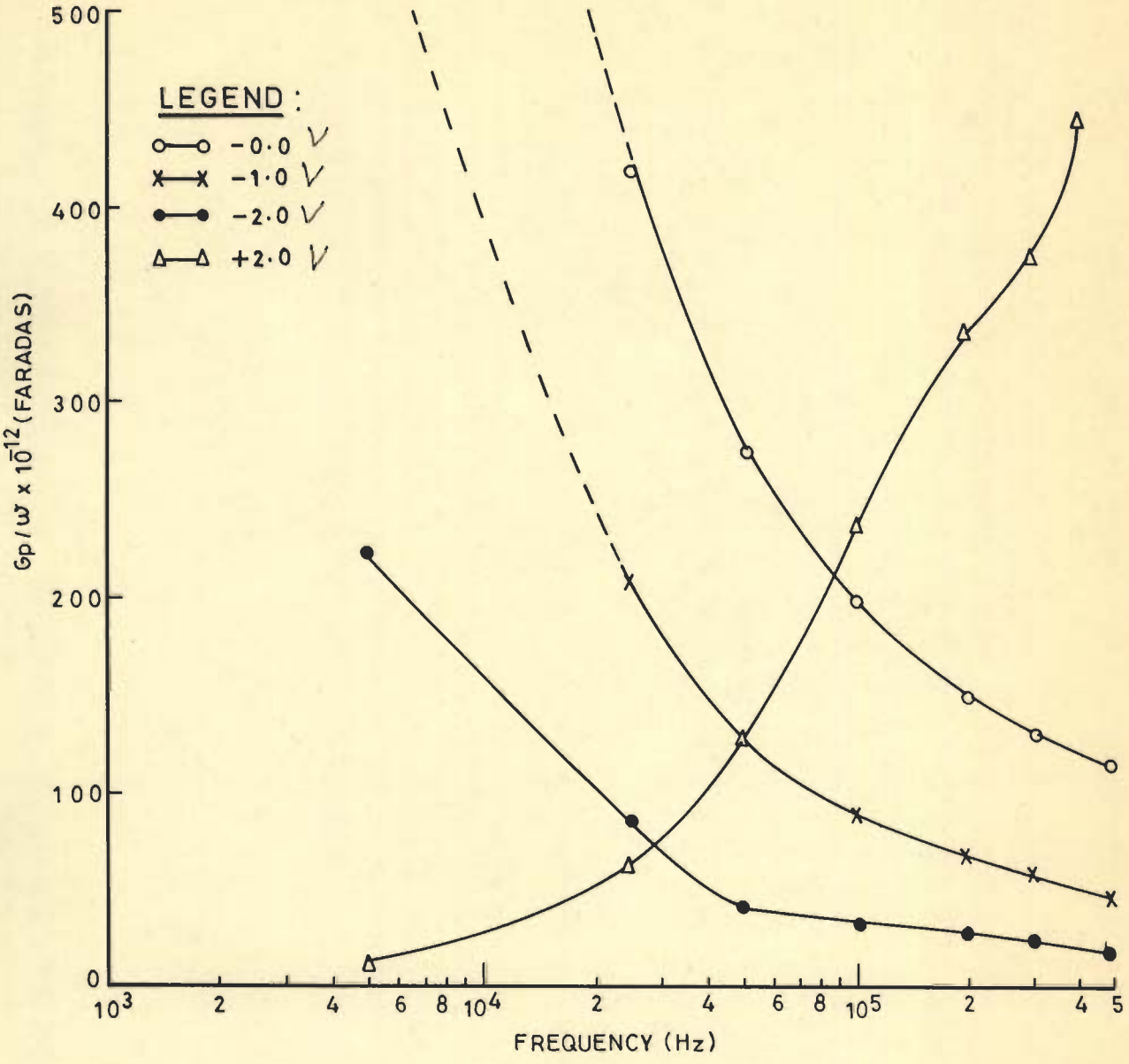


FIG. 4.15 : VARIATION OF PARALLEL CONDUCTANCE (G_p/ω) WITH FREQUENCY FOR SEVERAL GATE VOLTAGES FOR MOS SAMPLE SiO_2 THICKNESS 900 A°

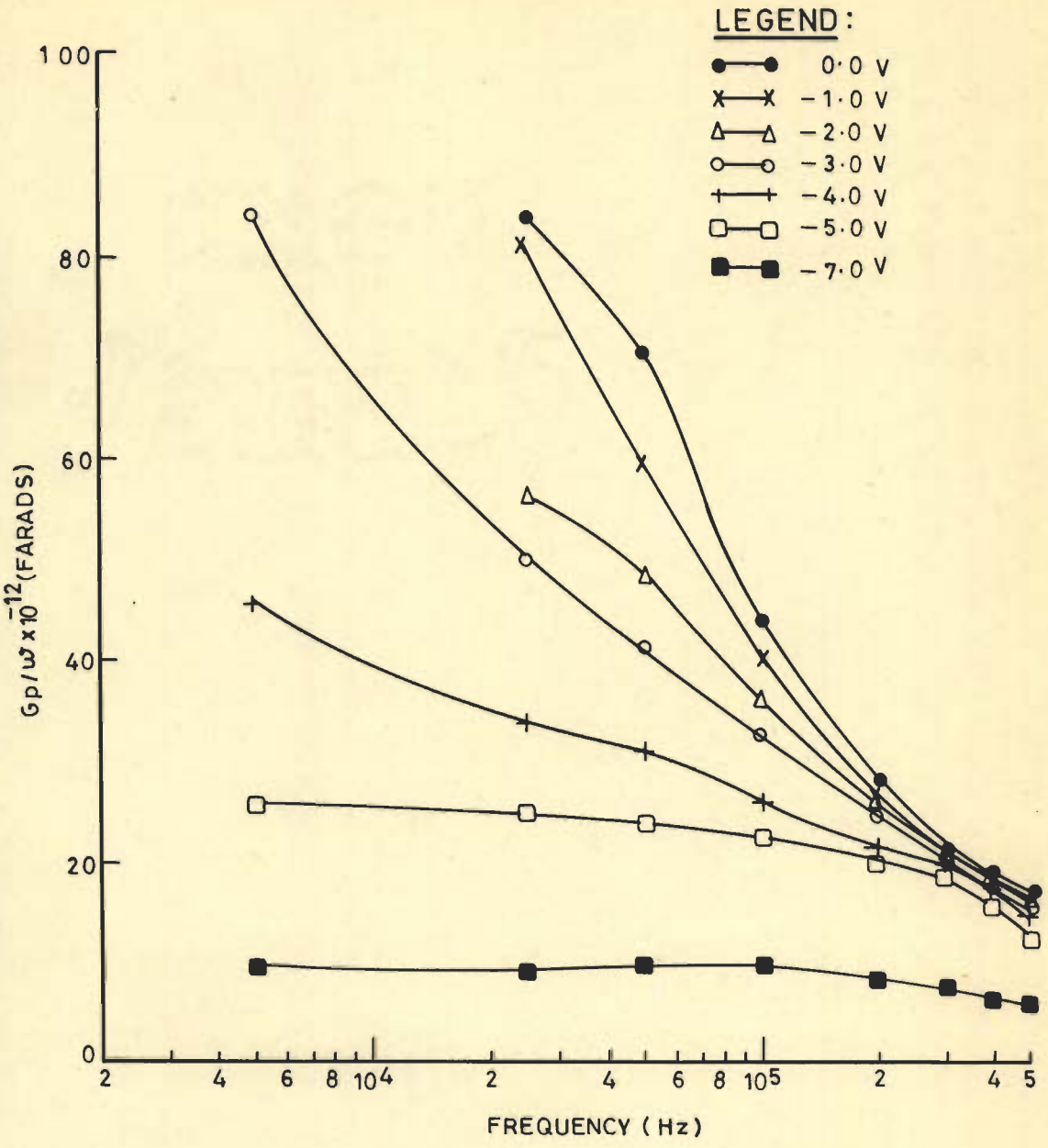


FIG. 4·16 : VARIATION OF PARALLEL CONDUCTANCE (G_p/ω) WITH FREQUENCY FOR SEVERAL GATE VOLTAGES FOR MOS SAMPLE : SiO_2 THICKNESS 1200 A°

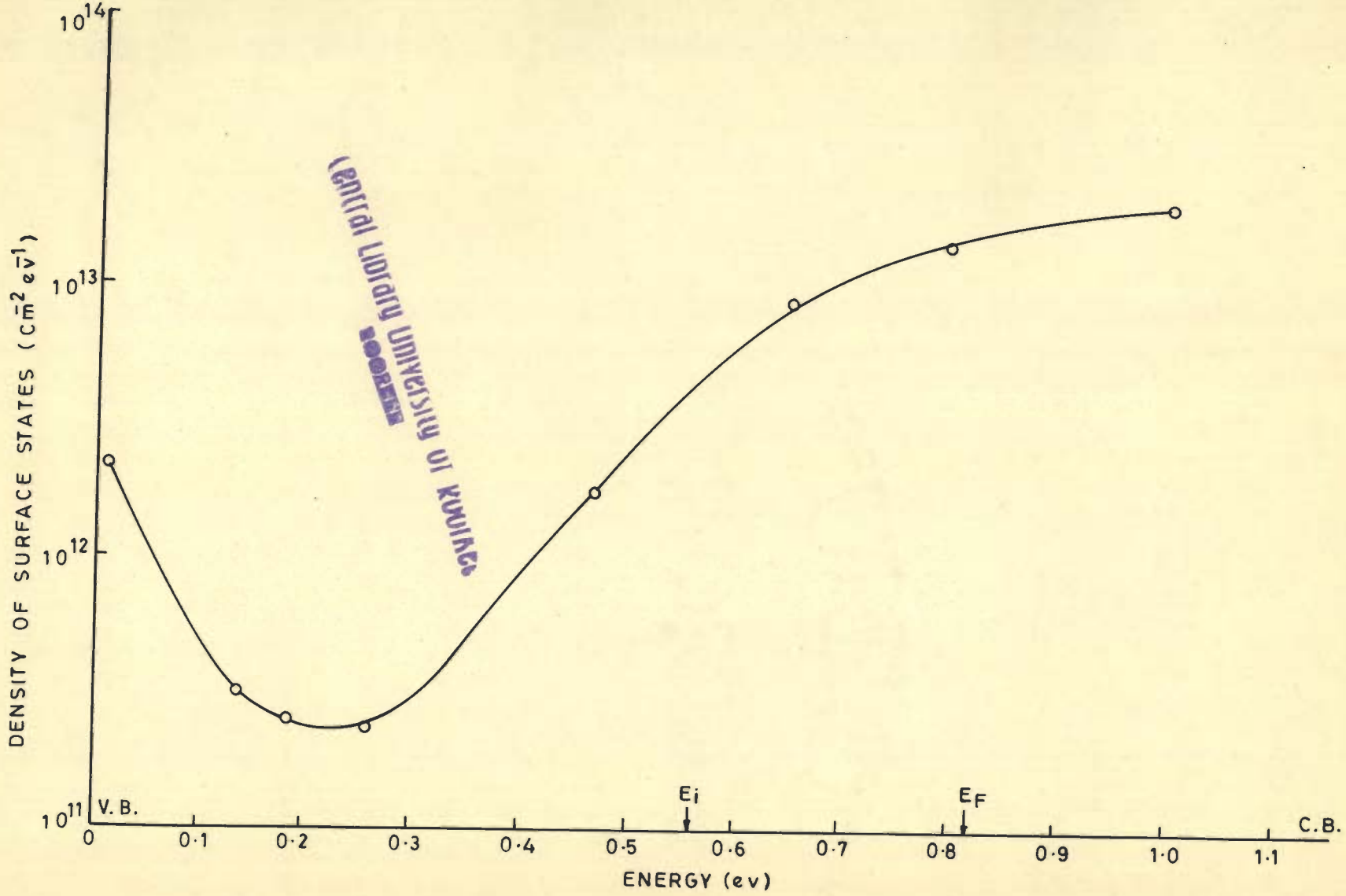


FIG. 4·17 : VARIATION OF SURFACE STATE DENSITIES Nss ACROSS THE BAND GAP OF Si EVALUATED BY CONDUCTANCE METHOD OXIDE THICKNESS (SiO_2) 300 A°

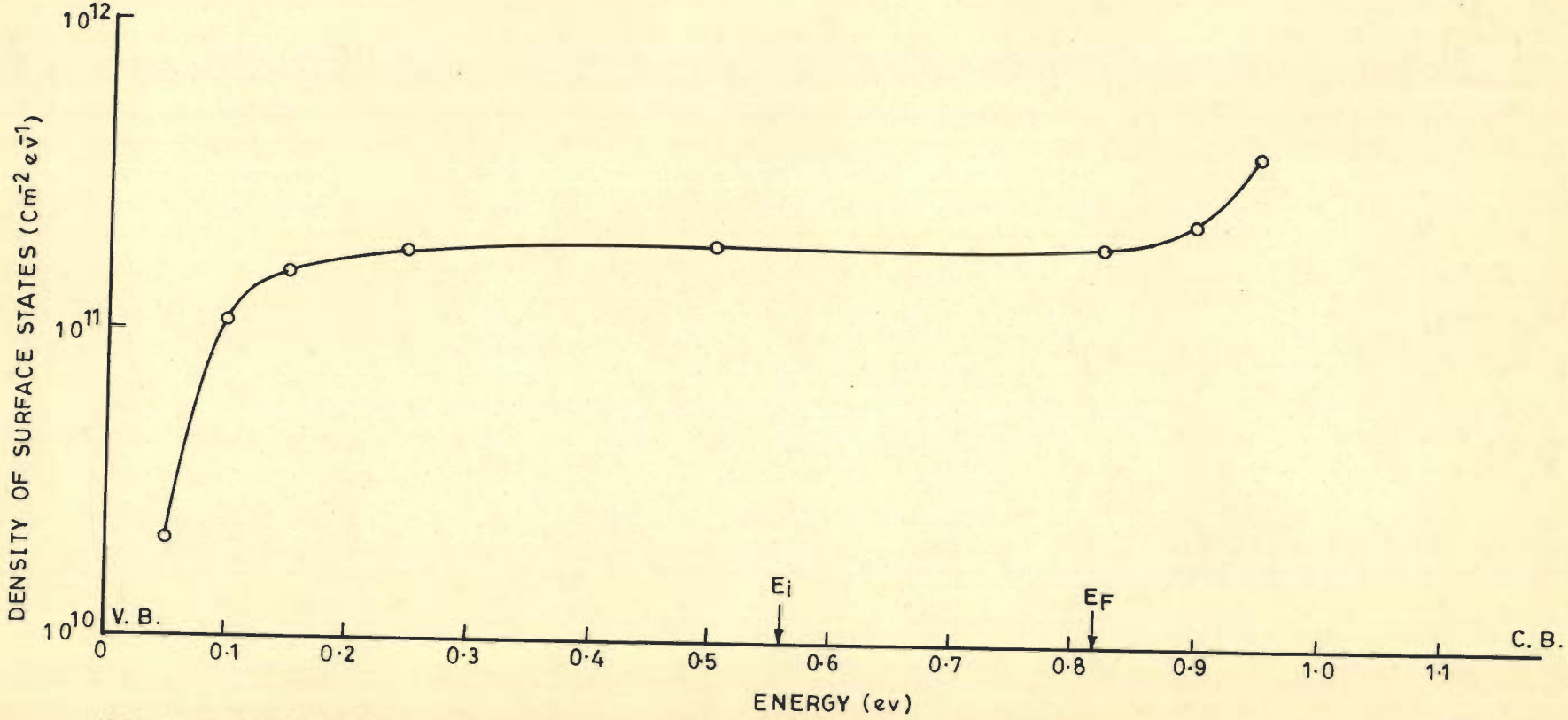


FIG. 4·18 : VARIATION OF SURFACE STATE DENSITIES Nss ACROSS THE BAND GAP OF Si EVALUATED BY CONDUCTANCE METHOD OXIDE (SiO_2) THICKNESS 600 A°

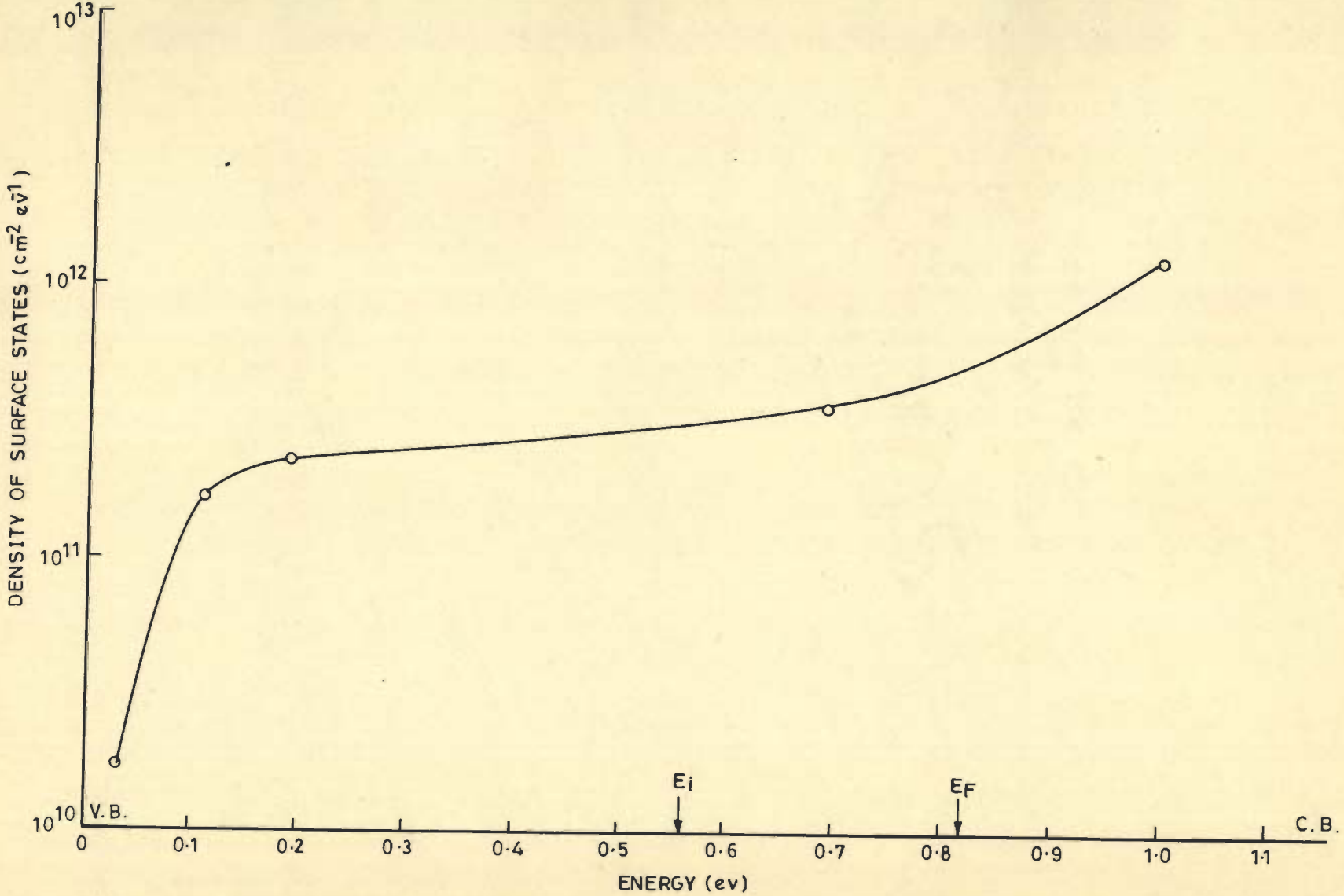


FIG. 4·19 : VARIATION OF SURFACE STATE DENSITIES Nss ACROSS THE BAND GAP OF Si EVALUATED BY CONDUCTANCE METHOD OXIDE (SiO_2) THICKNESS 900 A°

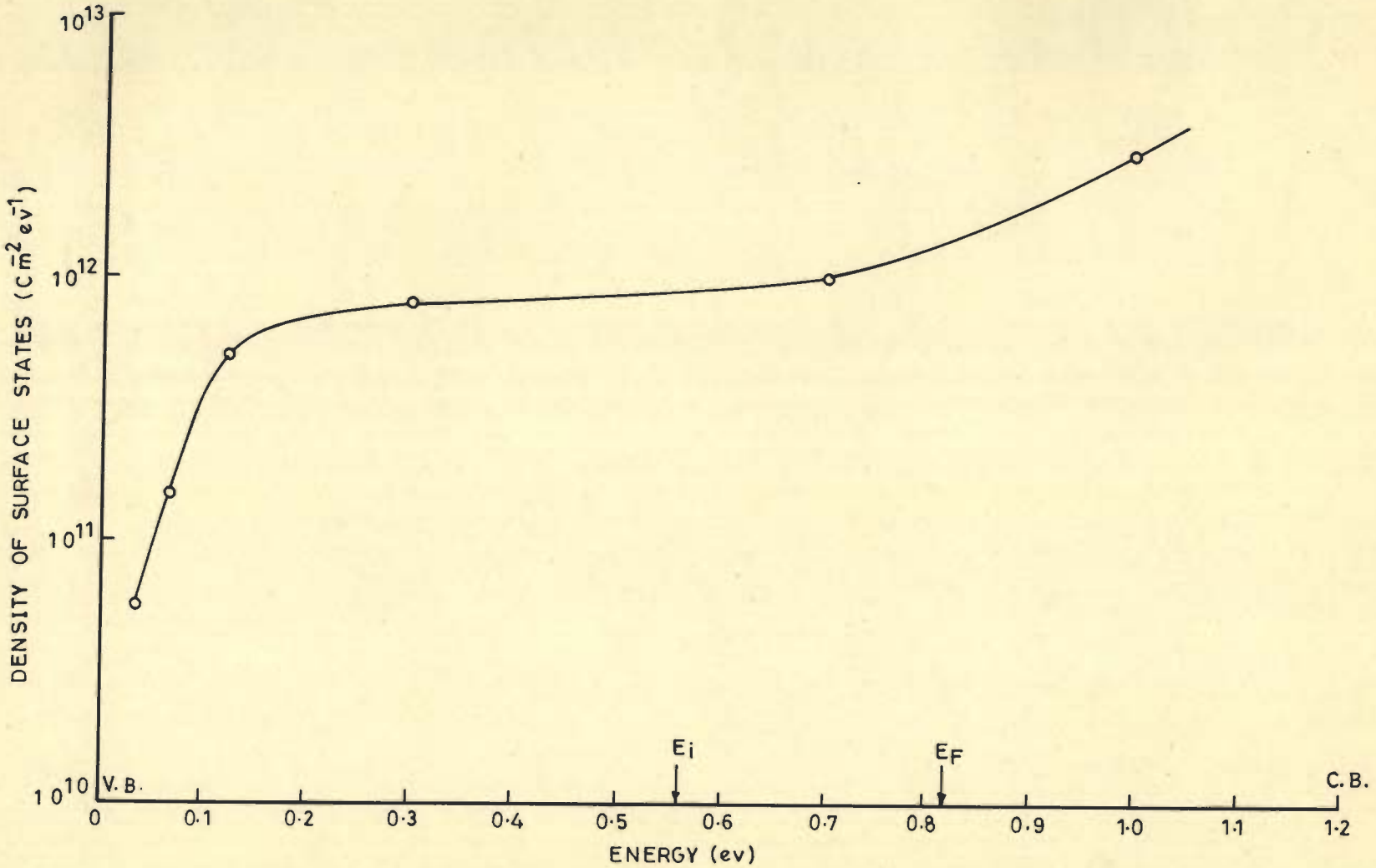


FIG. 4·20: VARIATION OF SURFACE STATE DENSITIES Nss ACROSS THE BAND GAP OF Si EVALUATED BY CONDUCTANCE METHOD OXIDE (SiO_2) THICKNESS 1200 A°

profile measured for the sample having a film thickness 300A° shows a broad minimum between 0.15 ev and 0.3 ev above the valence Band edge having an interface state density 4×10^{11} states cm^{-2} ev^{-1}, and an increasing concentration towards the band edges. In other samples of film thicknesses 600A°, 900A° and 1200A° the surface state density decreases from high values near the conduction band to low values near midgap and a minimum low value at the valence band edge.

Figs. 4.21 to 4.23 shows the current voltage curves for three MOS samples with oxide thickness of the order of 300A°, 600A° and 1200A° respectively. Keithley electrometer model No.610C was used for measuring the leakage currents of the samples. A heavily grounded and shielded enclosure was used for these measurements. Resistivities of the grown films calculated from these curves are 5.33×10^{15} ohm-cm, 2.46×10^{15} ohm-cm and 3.79×10^{13} ohm-cm respectively.

The breakdown field strength of the oxide was deduced from the voltage required for catastrophic breakdown of the MOS sample. Results are shown in Fig.4.24. The result shows that the dielectric strength of the anodically grown SiO_2 film decreases as the film thickness increases. The dielectric constant of the film was calculated for a known area of aluminium counter electrode from the standard parallel-plate capacitance formula, $\varepsilon_r = \frac{C_i t}{\varepsilon_o A}$ where

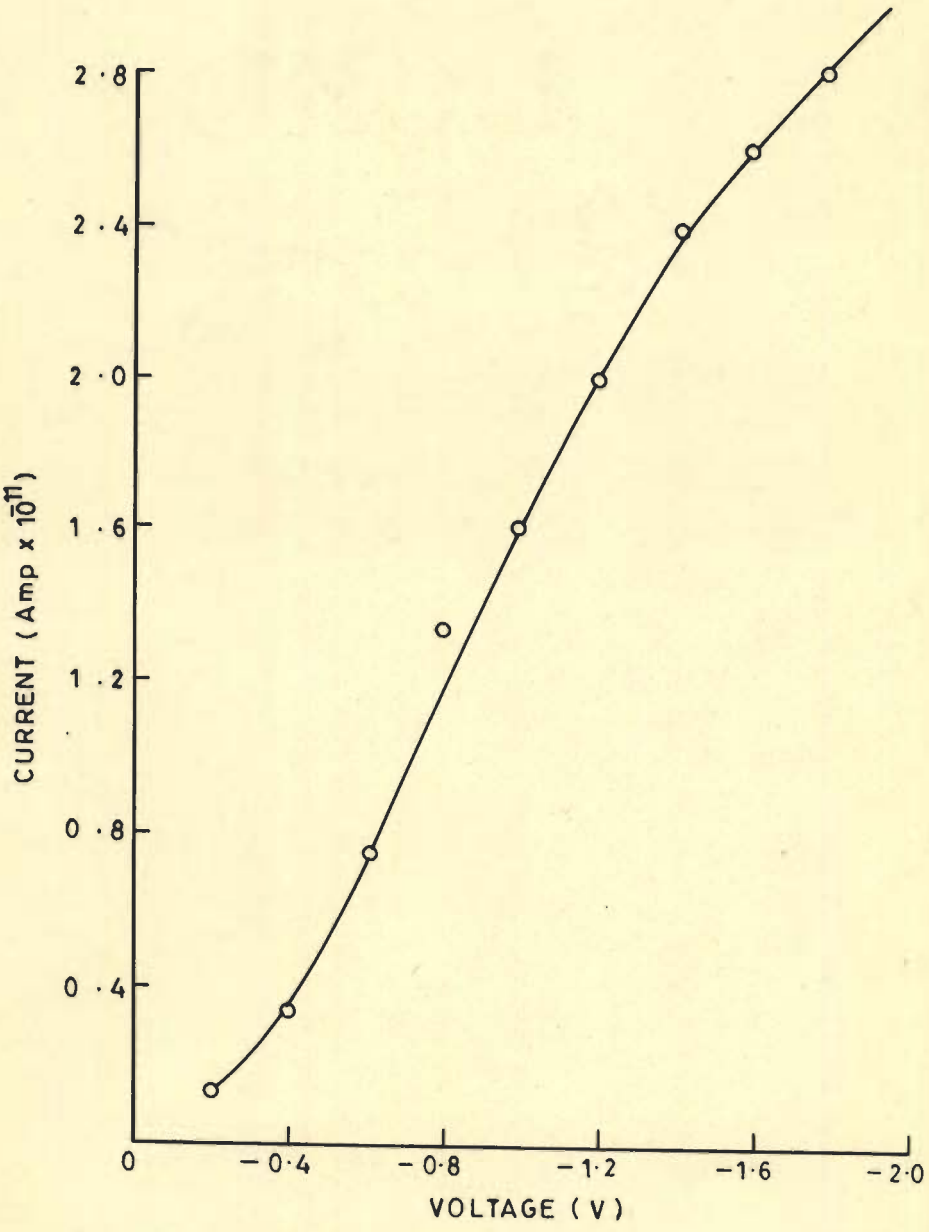


FIG. 4·21 : CURRENT VOLTAGE CHARACTERISTIC OF MOS SAMPLE OXIDE THICKNESS 300 A°

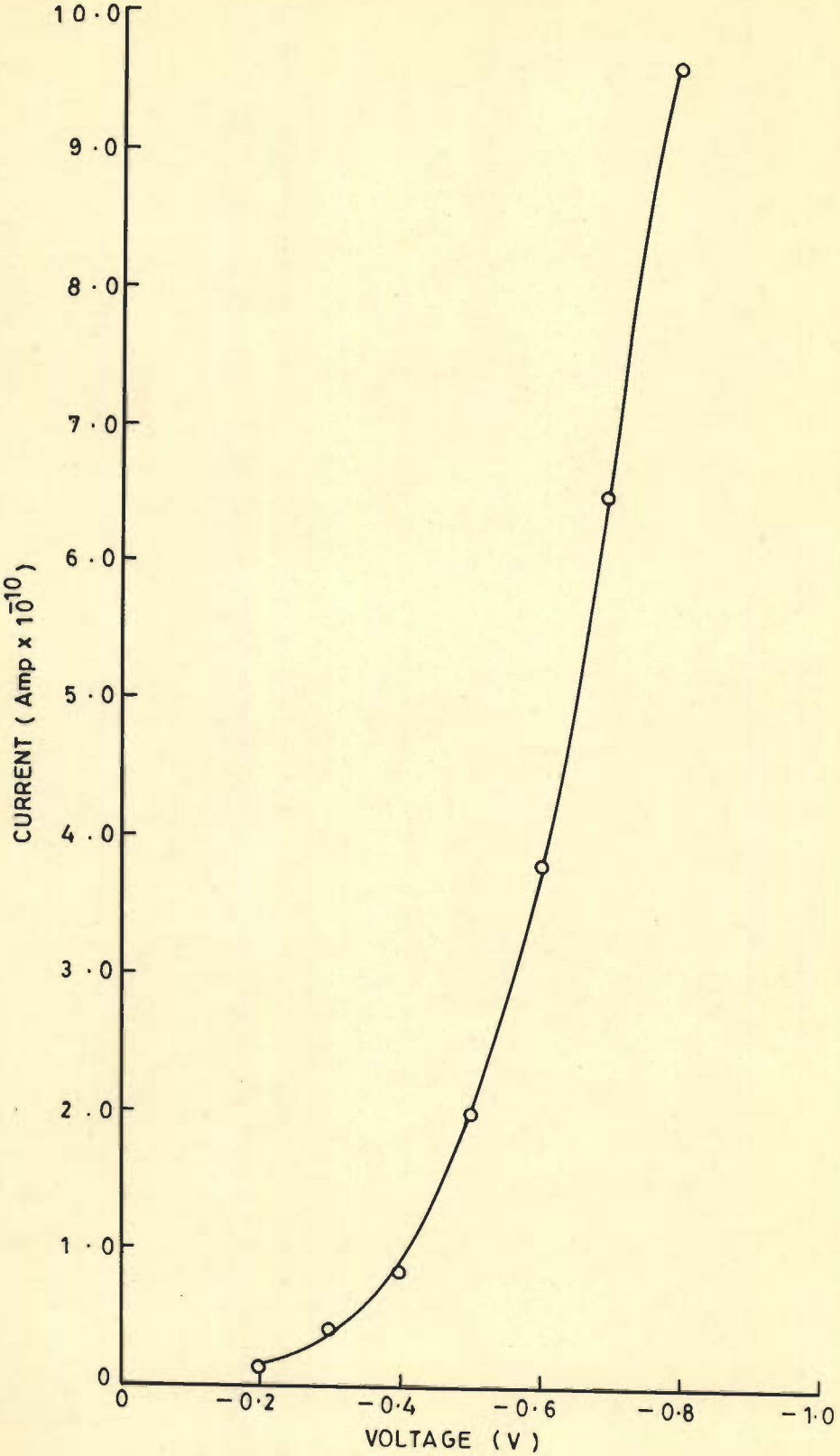


FIG. 4·22 : CURRENT VOLTAGE CHARACTERISTIC OF MOS SAMPLE OXIDE THICKNESS 600A°

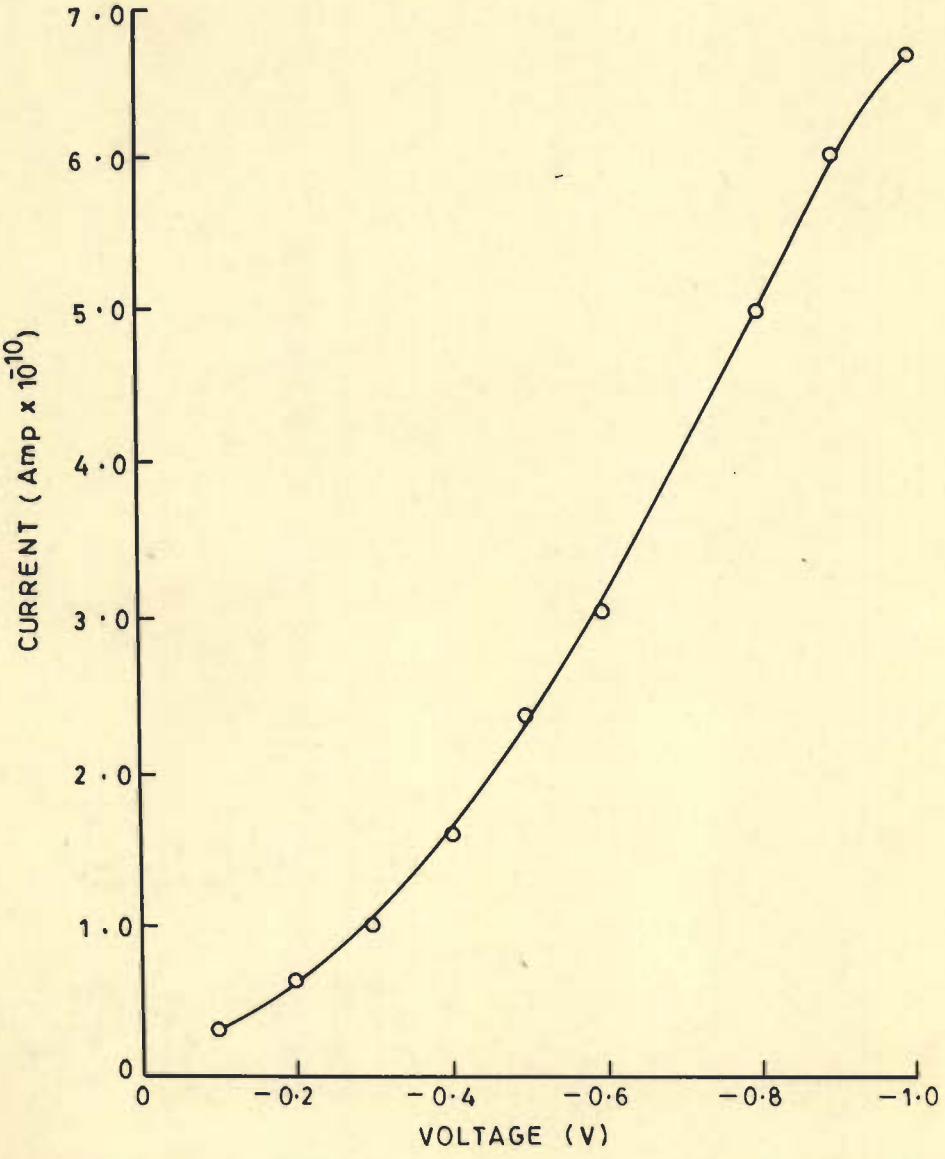


FIG. 4·23 : CURRENT VOLTAGE CHARACTERISTIC OF MOS SAMPLE, OXIDE THICKNESS 1200 A°

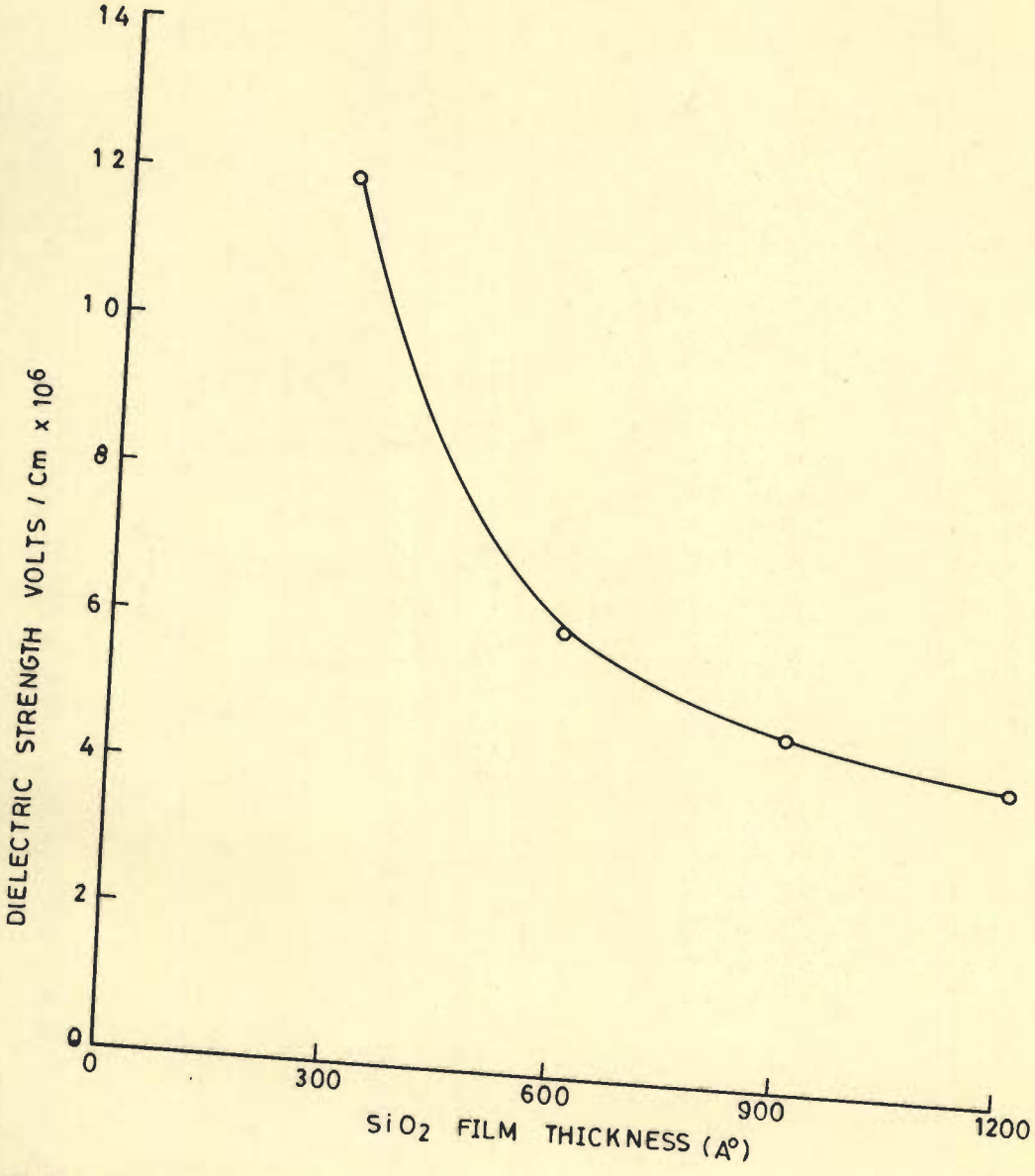


FIG. 4-24 : VARIATION OF DIELECTRIC STRENGTH WITH THE THICKNESS OF THE OXIDE (SiO_2) FILM

C_i, t, A and ε_o are capacitance of grown film in farad, thickness of the film in meters, area of the counter electrode in square meters and the premittivity constant respectively. The dielectric constant of 300A° thick grown film was found to be 4.08 at 500 KHz. As the thickness of the grown film increases the dielectric constant decreases, for a grown silicon dioxide layer of thickness 1200A° it was calcualted to be 3.08 at 500 KHz frequency. The above noted observations shows that there is a deterioration of the dielectric quality of the grown film with increasing film thickness, but the quality of the films of the order of 300A° are comparable with that of thermally grown films.

CHAPTER V

MAS, MAOS STRUCTURES AND THEIR INTERFACIAL PROPERTIES

5.1 INTRODUCTION

In recent years Metal-Aluminium Oxide-Silicon (MAS) and Metal-Aluminium oxide-silicon dioxide-silicon (MAOS) structures have been the subject of extensive investigations due to the superior bulk properties of aluminium oxide as compared to those of silicon dioxide. Aluminium oxide has higher dielectric constnat [92], higher density [93], higher radiation resistance [94] and large impermeability for impurity diffusion [95,96]. Further it gives a positive value of threshold voltage [97], it stops fast diffusion alkali ions such as sodium [96,98] which provides a passivating layer.

The results of MOS samples fabricated by anodization technique discussed in the preceding chapter show that the properties of anodic oxide fims of SiO_2 of the order of 300 A° are comparable with those grown thermally. In addition to that these films are grown at a low temperature. However the quality of these anodically grown oxide films deteriorates as the thickness of the film increases. One of the important basic parameters involved in the design of field effect devices employing MOS

structures is the thickness of the oxide layer used. It is interesting to note that the oxide thickness should be as thin as possible. For enhancing the field effects in MOS devices, the transconductance of a MOSFET is an inverse function of the oxide thickness. Unfortunately as the oxide layer becomes thinner, leakage currents through the oxide increases rapidly, with deterimental effects on the space charge in the semiconductor due to the non-equilibrium conditions. Thus the optimum oxide thickness that can be employed in a field - effect device depends on the physical properties of the oxide layer. In view of improving the over all physical properties of the oxide layer efforts were made to fabricate and investigate the composite sutructures Al-Al_2O_3-SiO_2-Si (MAOS). In the MAOS structures silicon dioxide films were grown at low temperature by anodic oxidation technique already described in chapter III. Al-Al_2O_3-Si (MAS) structures were also investigated.

Several techniques have been reported in the literature for growing or depositing the aluminium oxide films namely Anodization [92,94], Reactive sputtering [99,100], R.F.Sputtering [93,101], chemical vapor deposition (CVD) using an aluminium halide-CO_2-H_2 reaction [103], RF plasma CVD using $AlCl_3$-O_2 reaction [104] and RF plasma-enhanced chemical vapour deposition (PECVD) [105]. In the present investigations Al_2O_3 films were fabricated by evaporating

high purity Al (99.999%) in partial pressure of O_2. The advantage of this technique is that the temperature of semiconductor silicon wafer does not exceed more than 400°C and does not require elaborate costly facilities.

5.2 DEPOSITION OF Al_2O_3 THIN FILMS AND FABRICATION OF MAS STRUCTURES

The silicon wafers were cleaned as per procedure given in section 3.3. The cleaned silicon wafers were placed inside the Zig fitted above the source inside the bell-jar. Aluminium of purity 99.999% in the form of small wire (U's) were placed over the aluminium coated tungsten filament fitted between the electrodes. In the begining the shutter was placed over the source of evaporation. The whole system inside the bell-jar was evacuated with the help of rotary and the diffusion pumps to a pressure lower than 2×10^{-6} torr. Bell jar was then outgassed by heating all the accessories in the chamber using a radiant heater placed at the top inside the bell-jar. However the temperature was raised slowly watching the pressure in the bell jar. Whenever the pressure crossed 2×10^{-4} torr the radiant heating was stopped and the chamber was allowed to cool down. This cycle of heating and cooling was continued until a stabilised pressure is achieved. Finally the source was degassed by raising its temperature slowly to 500°C and then allowing it to cool down, till the pressure is reached

again to a value lower than $2x10^{-6}$ torr. It was carefully noted that the shutter should cover the silicon substrate holder entirely from the exposure to the source during source degassing, otherwise some of the impurities coming out of the source may be deposited on the silicon substrate during this period. Now oxygen was leaked into the chamber through a needle valve. The flow meter and the gas leak valves were adjusted such that the pressure inside the chamber was in the range of 10^{-3} torr. The tungsten filament was brought to a high temperature by passing an electric current through it. The substrate temperature during the deposition of the film was adjusted at 300°C and measured using a thermocouple touching the jig holding the silicon substrate. Now the shutter was opened and the oxidized aluminium was allowed to deposit on the silicon substrate. Deposition rate of aluminium oxide was adjusted as low as possible ranging from 10 to 15 A°/min using a quartz crystal thickness monitor. After depositing the desired thickness of the film the samples were annealed for 30 minutes in an oxygen ambient inside the vacuum coating unit at a temperature of 400°C.

A set of aluminium dots of area $3.3x10^{-3}$ cm^2 and thickness about 2000 A° were deposited onto the oxide surface. Ohmic contacts were fabricated at the backside of the wafers as described in Sub-section 3.5.8.

5.2.1 STANDARDISATION OF DEPOSITION PARAMETERS OF Al_2O_3

The main evaporation parameters adjusted during the deposition of Al_2O_3 films are:

(i) The partial pressure of oxygen

(ii) Source to substrate distance

(iii) The rate of deposition of Al_2O_3 film

(iv) The substrate temperature.

The oxygen pressure inside the chamber was maintained at 10^{-3} torr. as reported by Nazar et.al. [106], and Nisha Sarwade [107]. The source to substrate distance was kept 17 cm as reported by Nisha Sarwade [107]. For optimising the third and fourth parameters the Al_2O_3 films of the thickness 500 A° were deposited on six n-type epitaxial silicon substrates at three-different substrate temperatures i.e. 100°C, 200°C and 300°C at two deposition rates i.e. 10 A°/min and 25 A°/min. The dielectric breakdown was determined for all the six samples thus fabricated under different conditions. Fig.5.1 shows the variation of the breakdown voltage against the substrate temperature for two deposition rates of Al_2O_3 film of a thickness of 500 A°. Highest dielectric strength is obtained for the film deposited at 300°C substrate temperature and 10 A°/min deposition rate.

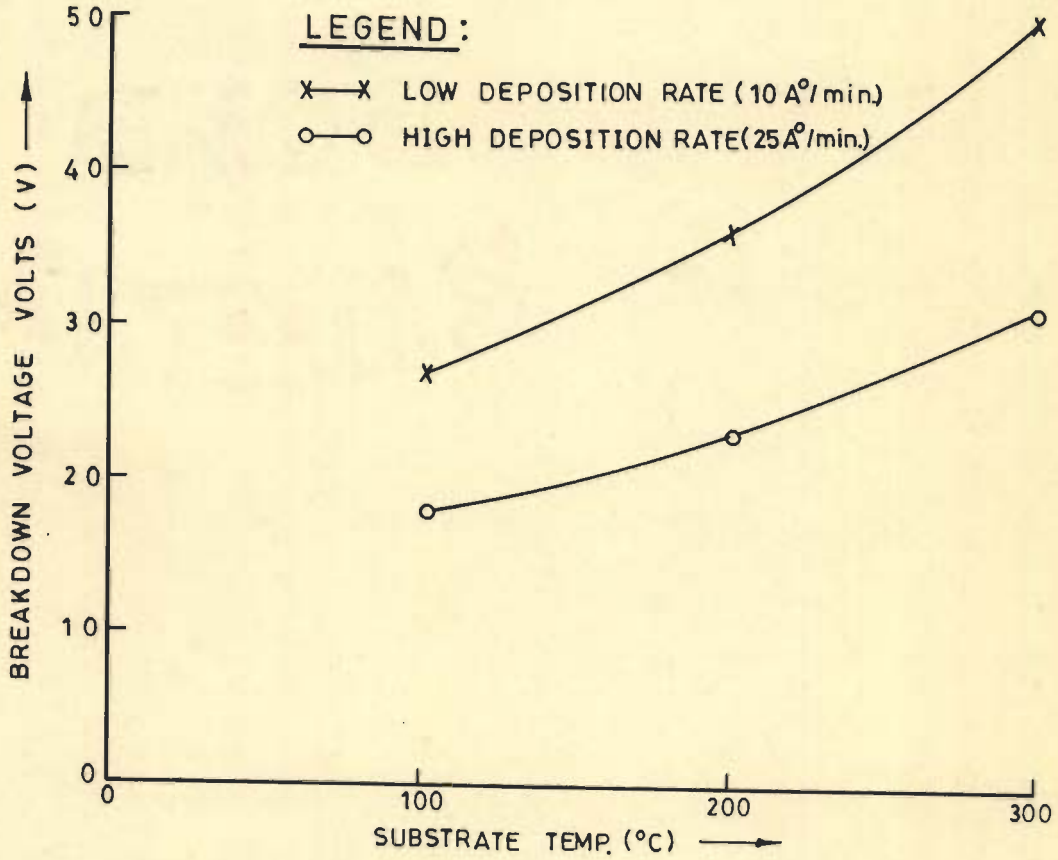


FIG. 5·1: BREAKDOWN VOLTAGE OF MAS STRUCTURES AS A FUNCTION OF SUBSTRATE TEMPERATURE

5.2.2 THE ANNEALING OF MAS SAMPLES

It is reported by several research workers that the dielectric and interfacial properties of MIS structures improves by annealing the fabricated MIS structures in suitable ambient. In our experimental arrangement Al_2O_3 films were deposited by reactive evaporation of aluminium in the presence of oxygen. During this process it is possible that some of the Al atoms are unable to react with oxygen and are deposited as such making the deposited Al_2O_3 film, they were annealed in an oxygen ambient. The annealing of the samples were carried out for 30 minutes in the oxygen ambient. Five different samples were annealed at Five different temperatures i.e. 100°C, 200°C, 300°C, 400°C and 500°C. For estimating the quality of annealed films the C-V curves were plotted with the help of automatic C-V plotter developed in the laboratory (described in APPENDIX A). Fig. 5.2 shows C-V curves at 500 KHz for MAS samples annealed in O_2 atmosphere at different temperatures. Fig. 5.2(a) shows the C-V behavior of an unannealed sample. A large hysteresis is present in the sample. In the samples annealed at 100°C, 200°C, 300°C and 400°C the hysteresis effect is gradually reduced respectively. The C-V curve of the sample annealed at 500°C get distorted. Hence it was concluded that the effectiveness of a post-deposition

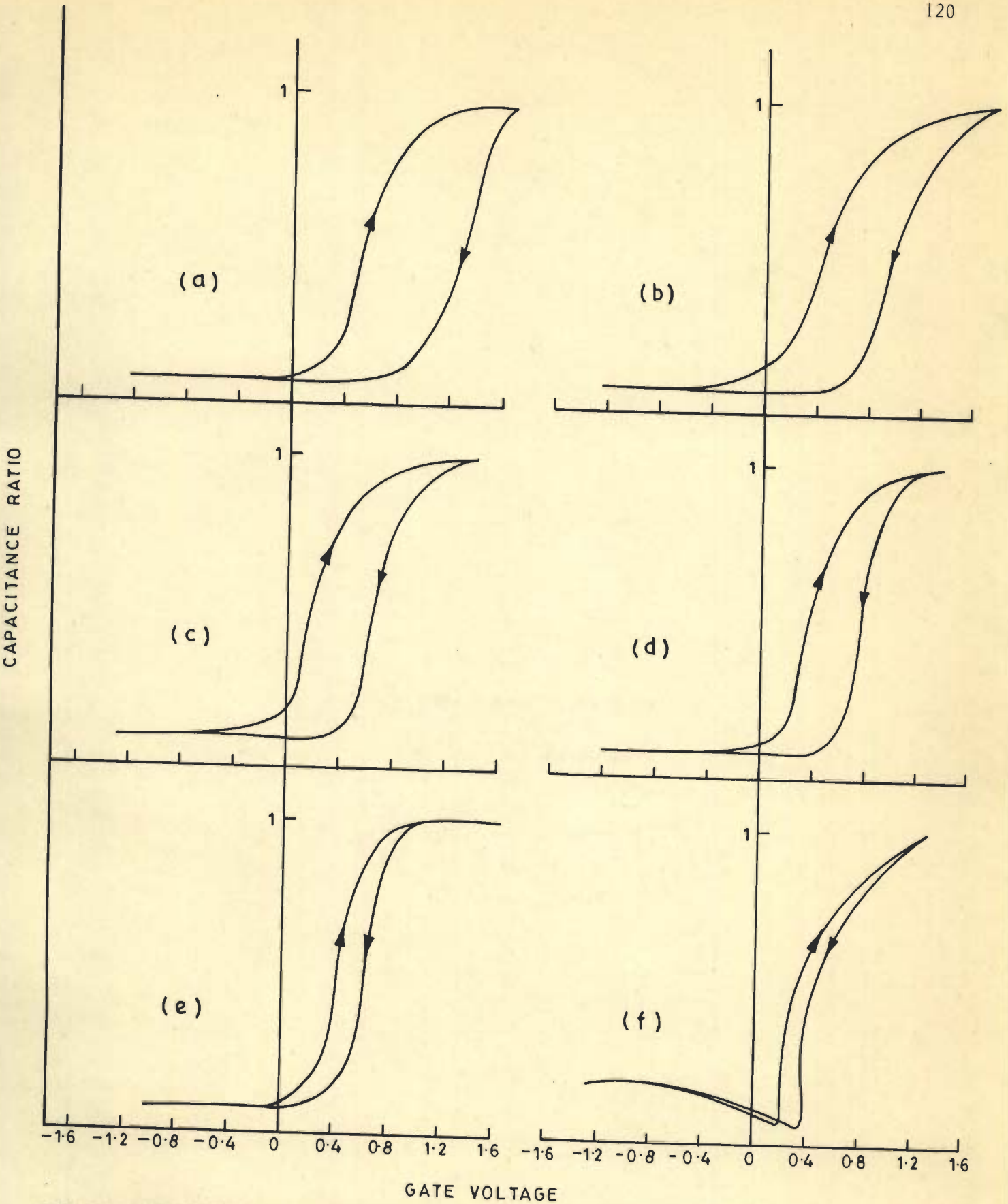


FIG. 5·2 : HYSTERESIS EFFECT IN MAS SAMPLES AT 500 KHz ANNEALED IN O_2 ATMOSPHERE AT DIFFERENT TEMPERATURES
(a) BEFORE ANNEALING (b) 100 °C (c) 200 °C (d) 300 °C
(e) 400 °C (f) 500 °C

O_2 treatment in eliminating the hysteresis increases as the annealing temperature is increased upto 400°C. The diminished hysteresis obtained in the annealed samples in O_2 at 400°C suggests that this effect is associated with incomplete oxidation of the Al. Another possibility is that the O_2 treatment modifies the defect structure of the Si-Al_2O_3 interface. Such a process could also be a modification of the defect structure of the residual SiO_2(30A°) on the silicon surface.

5.3 ELECTRICAL AND INTERFACIAL PROPERTIES OF Al-Al_2O_3-Si (MAS) STRUCTURES

MAS samples were fabricated on n-type epitaxial silicon wafers of ⟨111⟩ orientation and 6-8 ohm-cm resistivity at partial pressure of oxygen in the range of 10^{-3} torr, substrate temperature 300°C, deposition rate 10 A°/min and annealed in oxygen ambient at 400°C as described in Section 5.2.

Capacitance voltage (C-V) and conductance-voltage (G-V) characteristics of the fabricated MAS samples were measured at frequencies 500 KHz, 400 KHz, 300 KHz, 200 KHz, 100 KHz, 50 KHz and 5 KHz by Boonton Bridge. The measured C-V and G-V characteristics are plotted in Fig. 5.4 and 5.5 respectively. From the analysis of these measurements dielectric constant and interface

state density (states cm^{-2}. ev^{-1}) were determined. Interace properties were studied by MOS conductance method. Dielectric strength was determined from dielectric breakdown measurements.

With the aim of comparing the experimental results with the ideal C-V curves an experimental C-V curve obtained at 500 KHz is plotted along with the theoretically calculated [61] C-V curve in Fig. 5.3.

By comparing the theoretical and experimental curves the following observations are made.

(i) The experimental C-V curve is shifted to the right showing a positive flat band voltage of about 0.3 volts.

(ii) The slope of the experimental curve is lower than that of the theoretical curve.

(iii) The minimum capacitance Cmin of the sample at the steady state condition (i.e. with the inversion layer formed) is higher than expected from the theoretical Cmin.

(iv) The accumulation layer capacitance does not seem tobe reached even with a field strength of $6x10^5$V/cm. The capacitance in this region

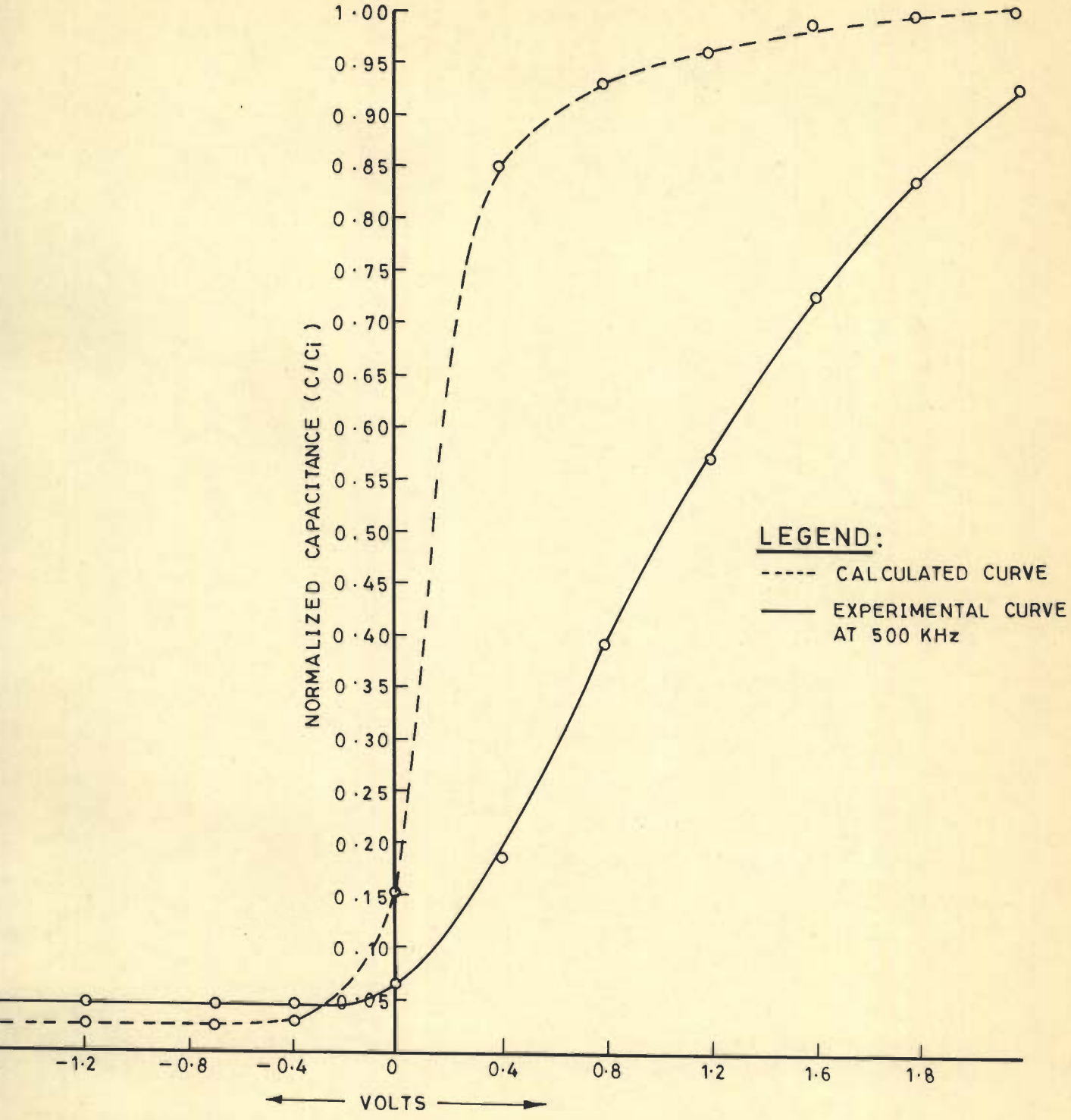


FIG. 5·3 : THEORETICAL AND EXPERIMENTAL C-V CURVES AT 500 KHz FOR MAS SAMPLES : OXIDE THICKNESS (Al_2O_3) 300 A°

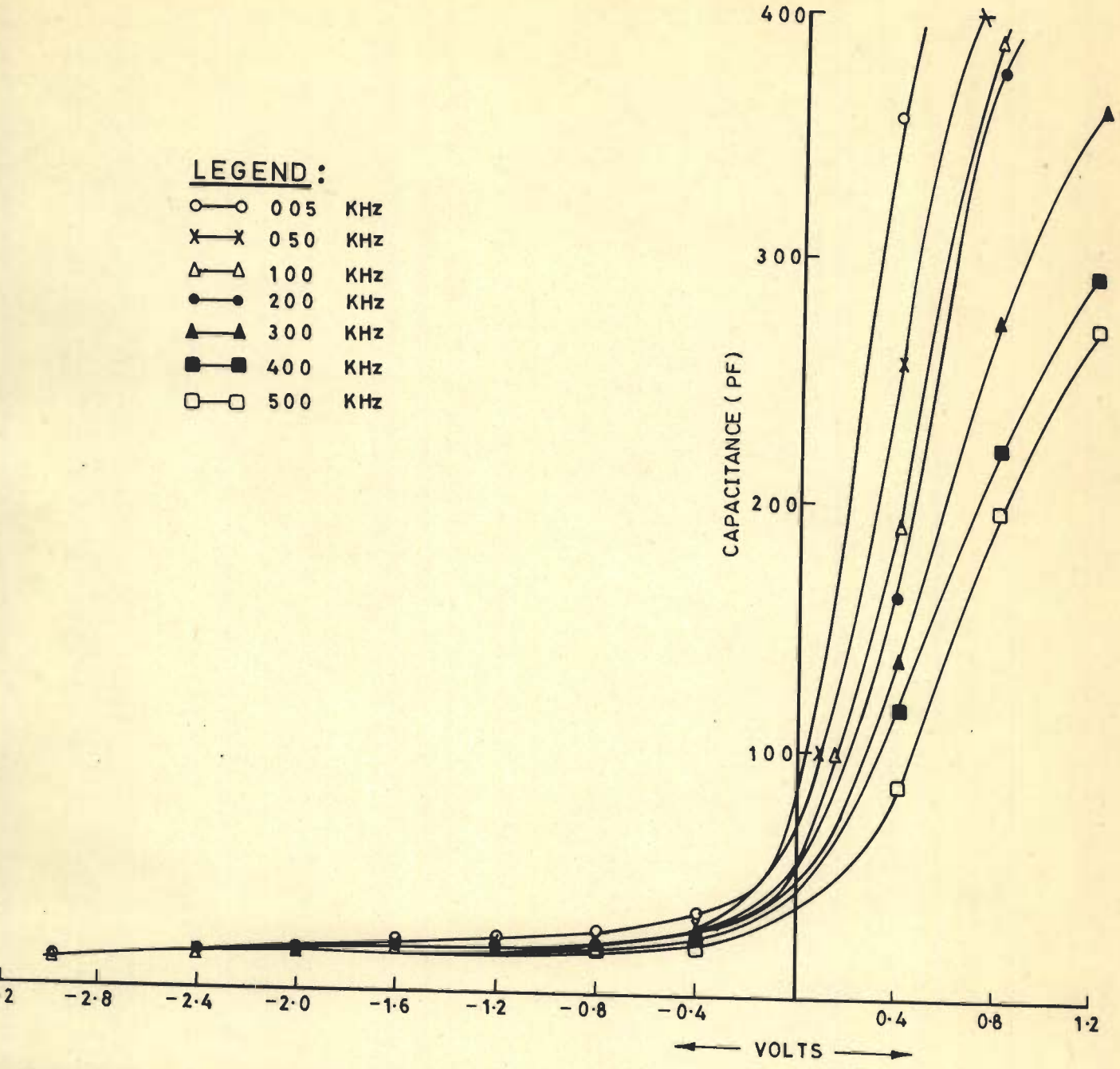


FIG. 5·4 : C-V CURVES FOR MAS SAMPLES : OXID THICKNESS OF THE ORDER OF 300 A°

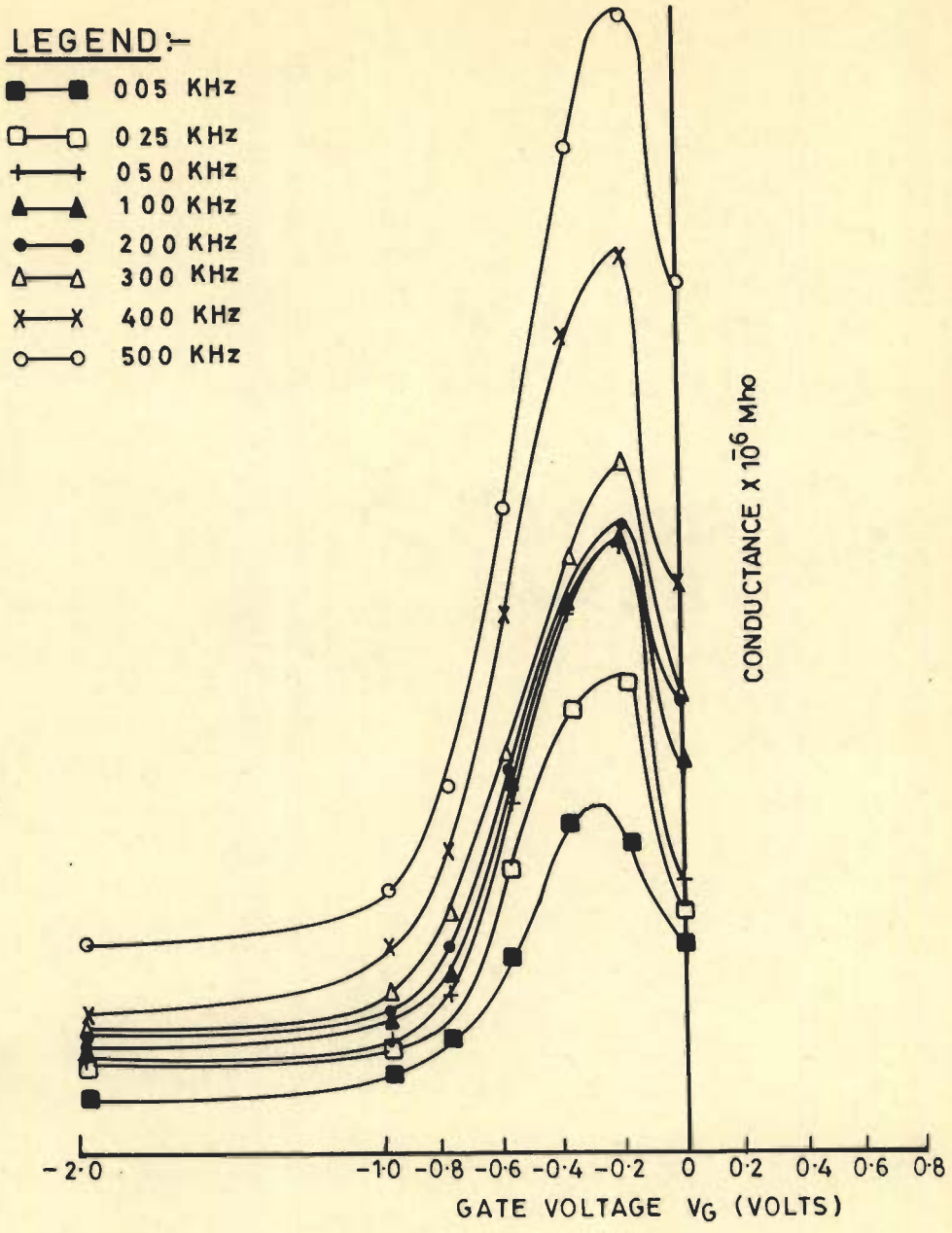


FIG. 5·5 : G-V CURVES FOR MAS SAMPLES OXIDE THICKNESS OF THE ORDER OF 300 A°

continues to rise with the applied bias voltage.

The results of the capacitance and conductance measurements on MAS samples are given in Figs. 5.4 and 5.5 . The frequency dispersion of the measure capacitance in the accumulation region shows that there are capacitance contributions from interface states even at measuring frequencies around 500 KHz. In the inversion region however it can be seen that there is no frequency dispersion. The observed hystersis effect in C-V curve is clockwise which is characteristic of electron trapping.

The G_p/ω versus frequency curves are shown in Fig.5.6. The curves shows a distinct peak which shifts to higher frequencies as the surface potential approaches to accumulation.

Fig. 5.7 shows the distribution of surface state density in the energy band gap calculated by conductance method, at the middle of the gap the surface state density is about 4×10^{11} states cm^{-2} ev^{-1}, while at the conduction band edge there is a steep increase of surface state density in the range of 2×10^{13} states cm^{-2} ev^{-1}.

The dielectric constnat of the films were determined as explained in Section 4.5. The value of dielectric constant varies between 7.5 to 8.

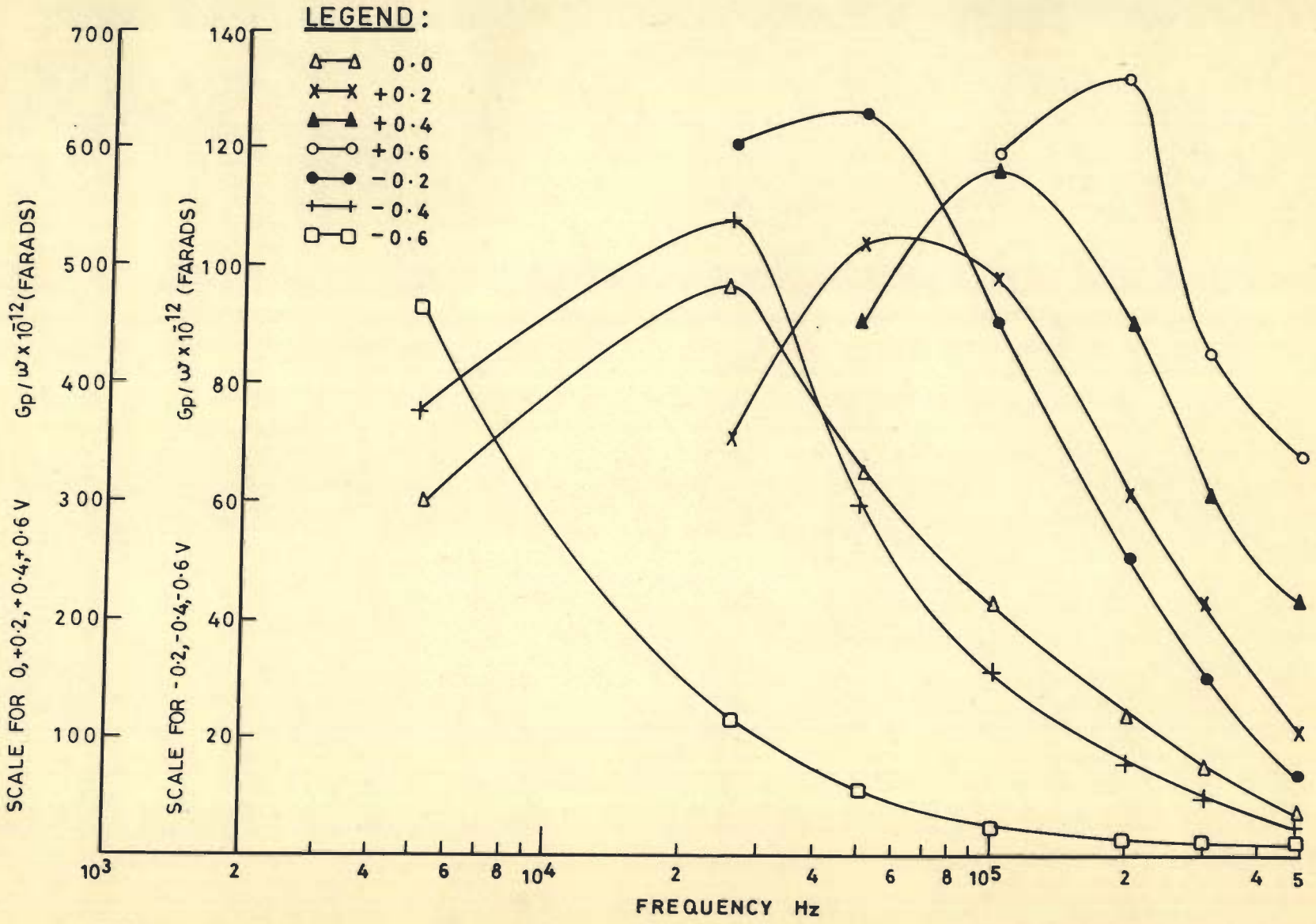


FIG.5·6: VARIATION OF PARALLEL CONDUCTANCE (Gp/w) WITH FREQUENCY AT SEVERAL GATE VOLTAGES FOR MAS SAMPLES

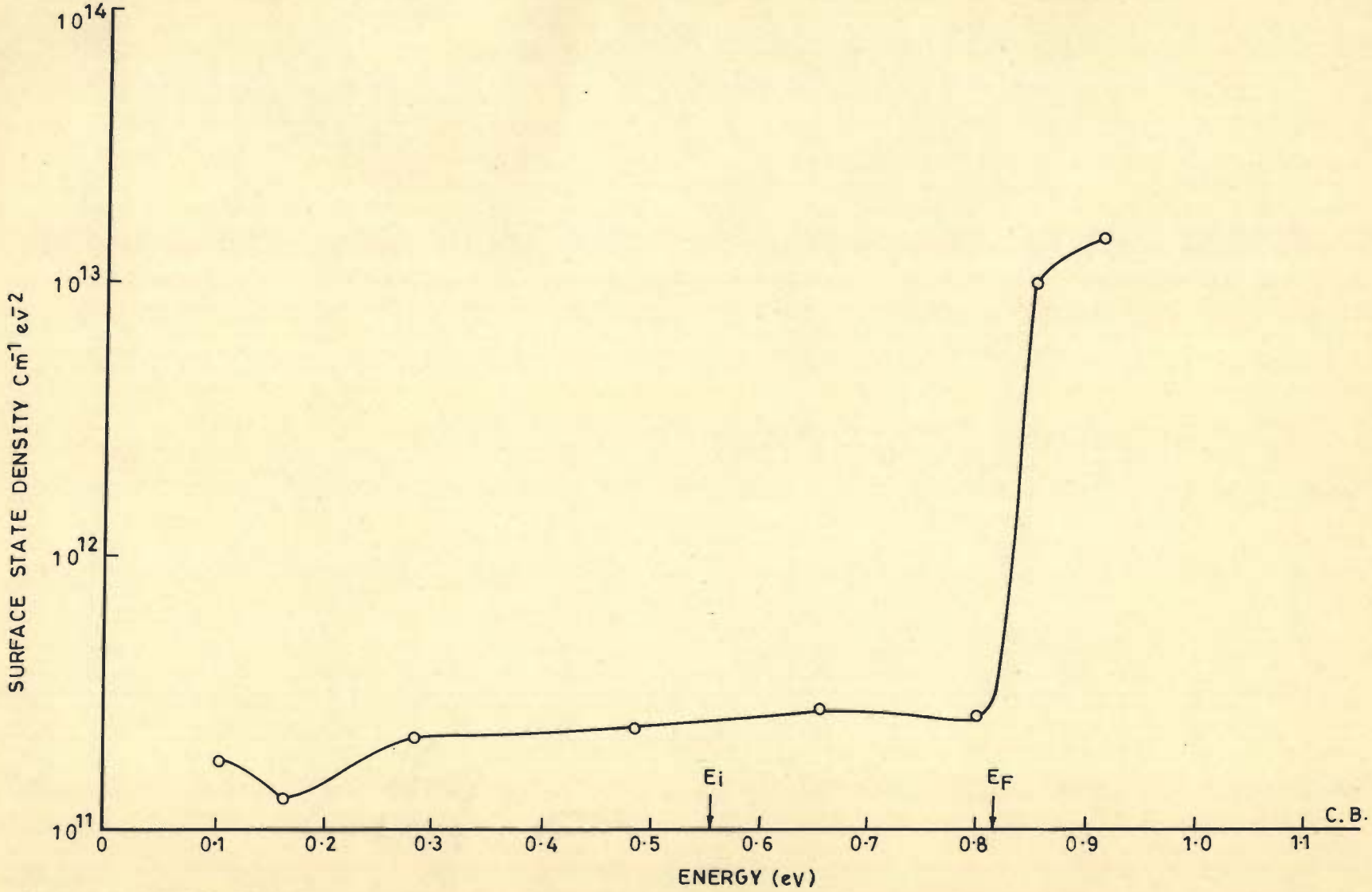


FIG.5·7 : VARIATION OF SURFACE STATE DENSITIES Nss ACROSS THE BAND GAP OF Si EVALUATED BY CONDUCTANCE METHOD FOR MAS SAMPLE : OXIDE THICKNESS (Al_2O_3) 300 A°

5.4 THE FABRICATION AND CHARACTERIZATION OF Al-Al_2O_3-SiO_2-Si (MAOS) STRUCTURES

MAOS samples were fabricated on n-type ⟨111⟩ orientation epitaxial silicon wafers having resistivity 6-8 ohm-cm. First SiO_2 film of 300 A° was grown on the epitaxial wafer by anodic oxidation technique as described in Section 3.5. Oxidised wafers were annealed in H_2 at a temperature of 500°C for 30 min. A film Al_2O_3 of thickness 300 A° was deposited over the silicon dioxide layer as described in Section 5.2. Now the fabricated MAOS samples were annealed in O_2 atmosphere at a temperature of 400°C for 30 minutes. Ohmic contacts were made at the back side of the samples as described in Sub-Section 3.5.8. A set of aluminium dots of area 3.3×10^{-3} cm^2 and thickness about 2000 A° were evaporated on the composite oxide surface.

On the fabricated MAOS samples capacitance-voltage (C-V) and conductance voltage (G-V) measurements were made at frequencies 500 KHz, 400 KHz, 300 KHz, 200 KHz, 100 KHz, 50 KHz, and 5 KHz by Boonton-Bridge. Figs.(5.8, 5.9) shows measured C-V and G-V curves. The measured C-V curves shows that the frequency dispersion in accumulation and depletion region is decreased as compared to the MAS samples.

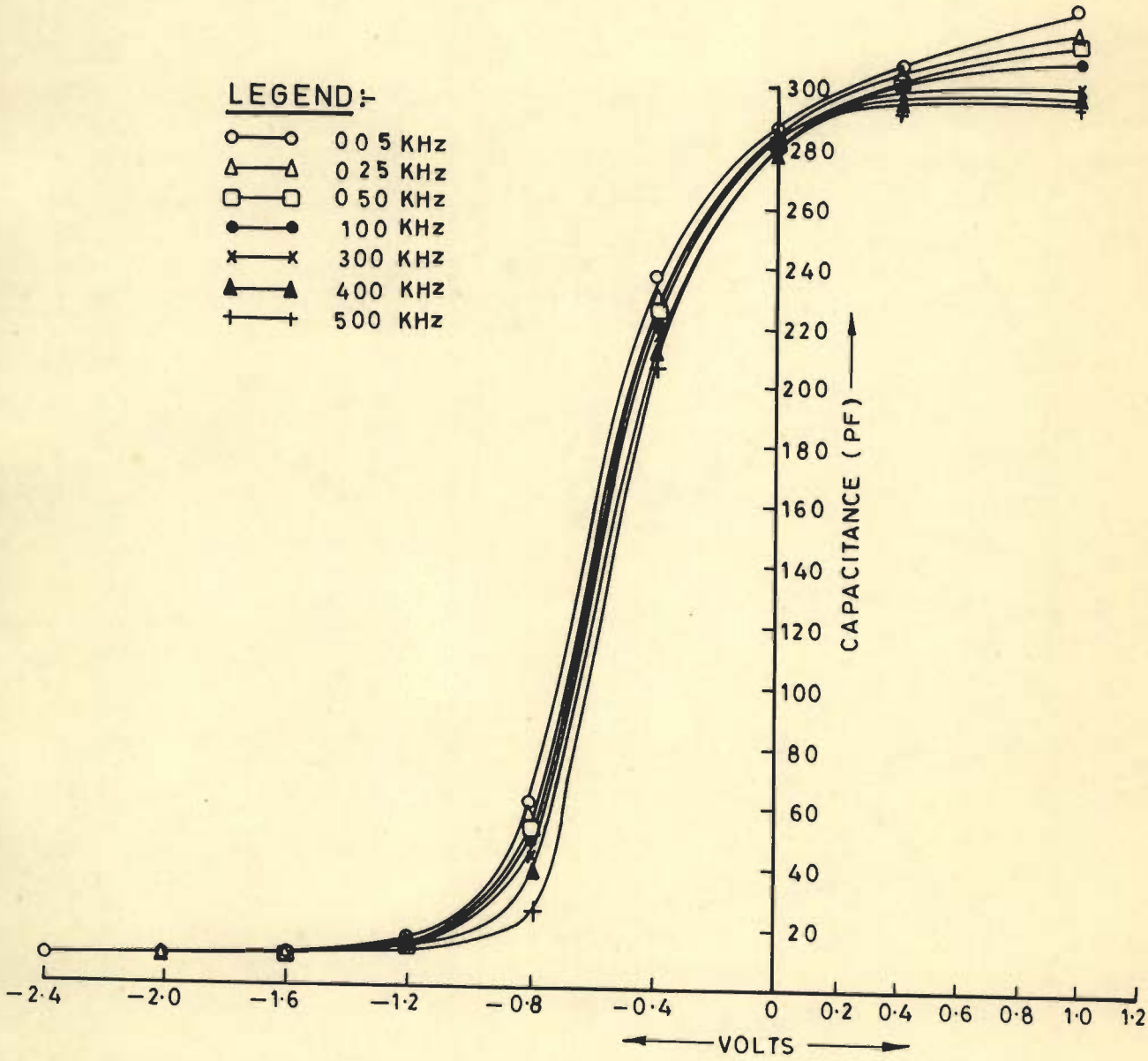


FIG. 5·8 : C–V CURVES FOR MAOS STRUCTURES : OXIDE THICKNESS (300 A° SiO_2 + 300 A° Al_2O_3)

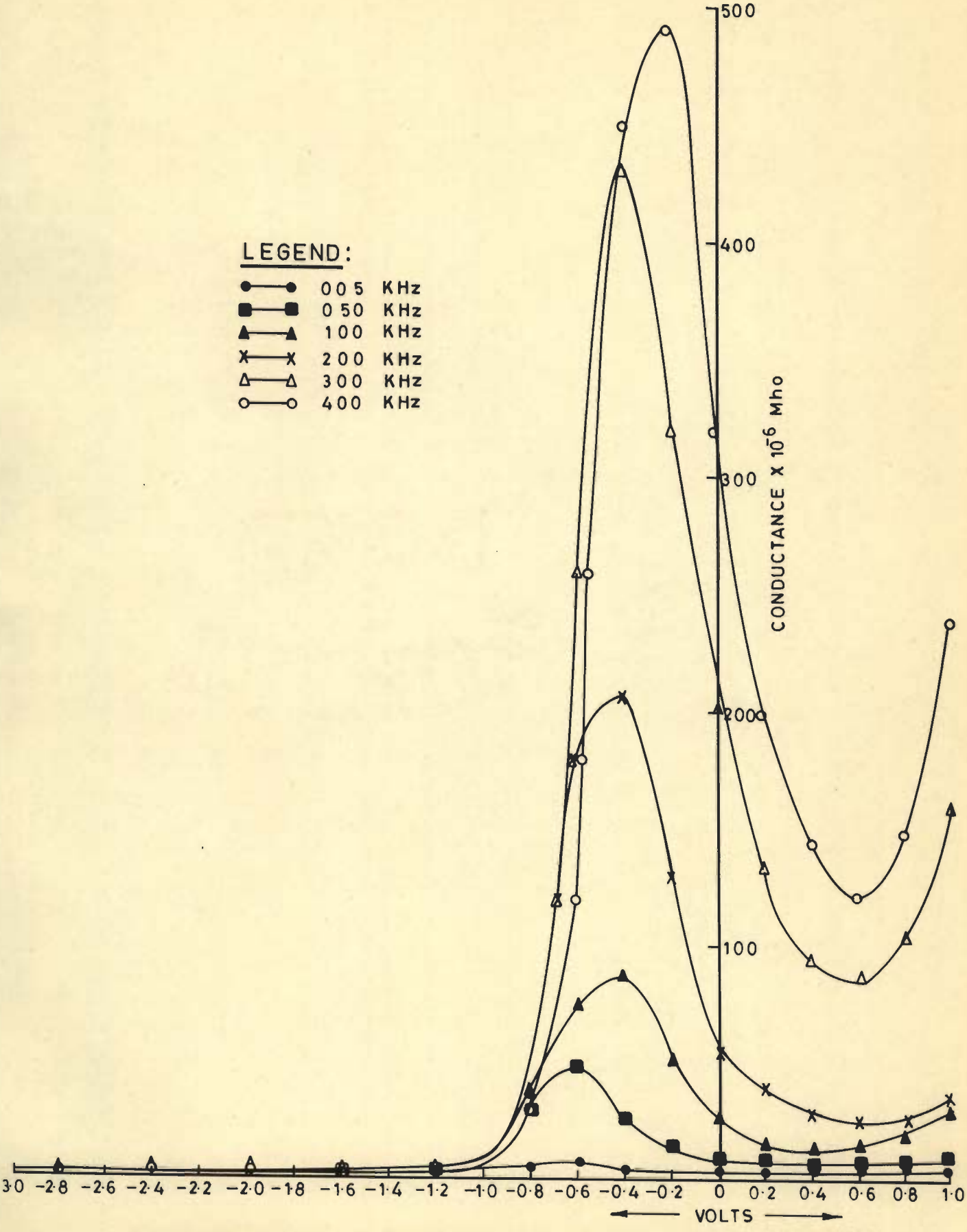


FIG. 5·9 : G-V CURVES FOR MAOS STRUCTURES: OXIDE THICKNESS (300 A° SiO_2 + 300 A° Al_2O_3)

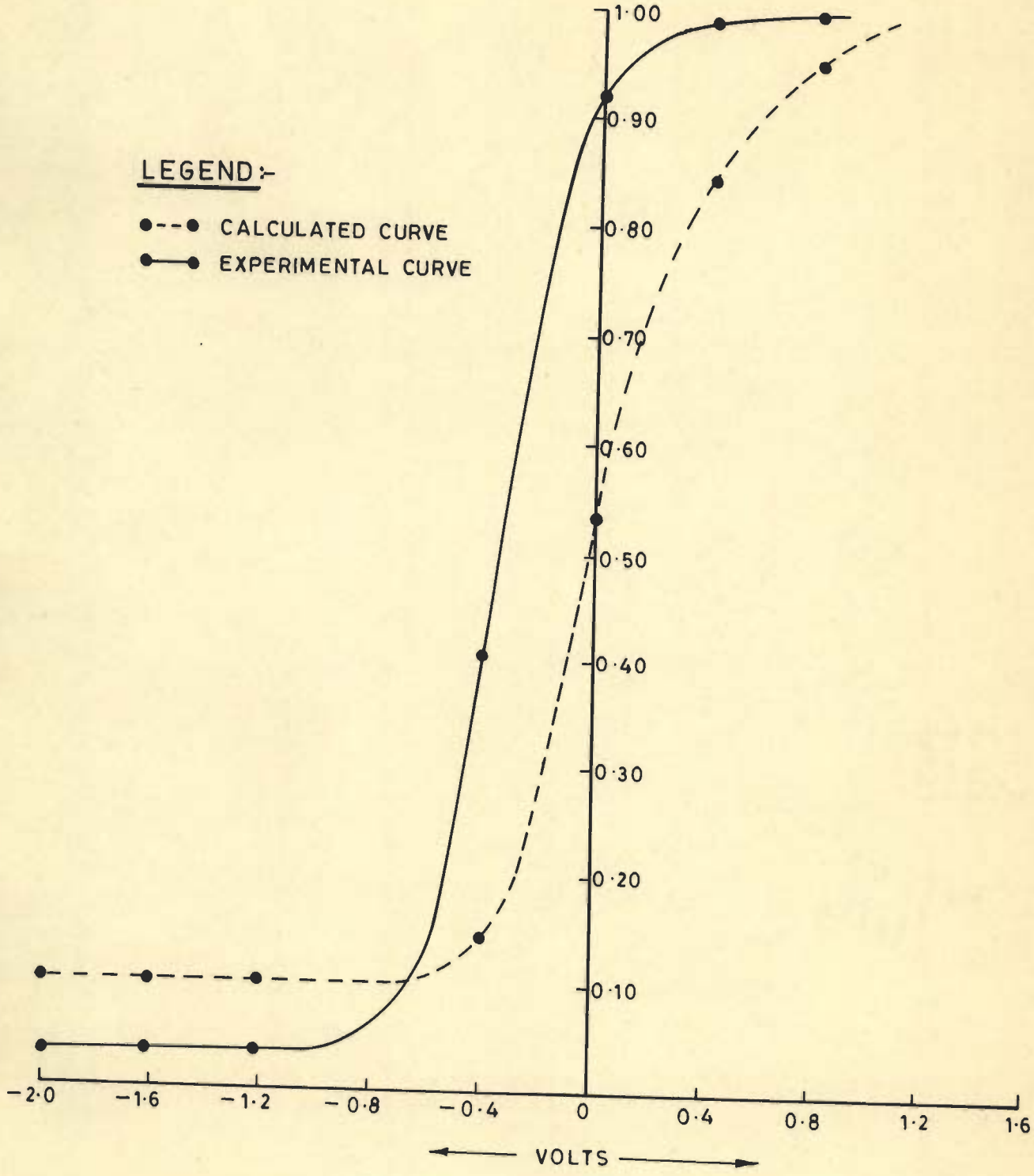


FIG. 5·10 : THEORETICAL AND EXPERIMENTAL C-V CURVES FOR MAOS SAMPLES AT 500 KHz

Fig. 5.10 shows experimental and theoretical C-V curve at 500 KHz. By comparing the theoretical and experimental curves the following observations are made.

(i) The experimental curve is shifted to the left showing a negative flat band voltage of about -0.34 volts.

(ii) The slope of the curve is higher than that of the theoretical curve.

(iii) The minimum capacitance Cmin of the sample at the steady state condition (i.e. with the inversion layer formed) is lower than expected from the theoretical Cmin.

(iv) The accumulation layer capacitance is achieved at a field strength of about 6.6×10^8 V/cm.

The G_p/ω versus frequency curves are shown in Fig. (5.11). Fig. 5.12 shows the distribution of surface state density calculated in the energy band gap. At the middle of the gap the surface state density is about 1.4×10^{11} states cm^{-2} ev^{-1}. The double insulator structure did not show any hysteresis effect. The dielectric constant of the composite structure is calculated to be 6.01. The dielectric breakdown field strength measured is about 2×10^7V/cm.

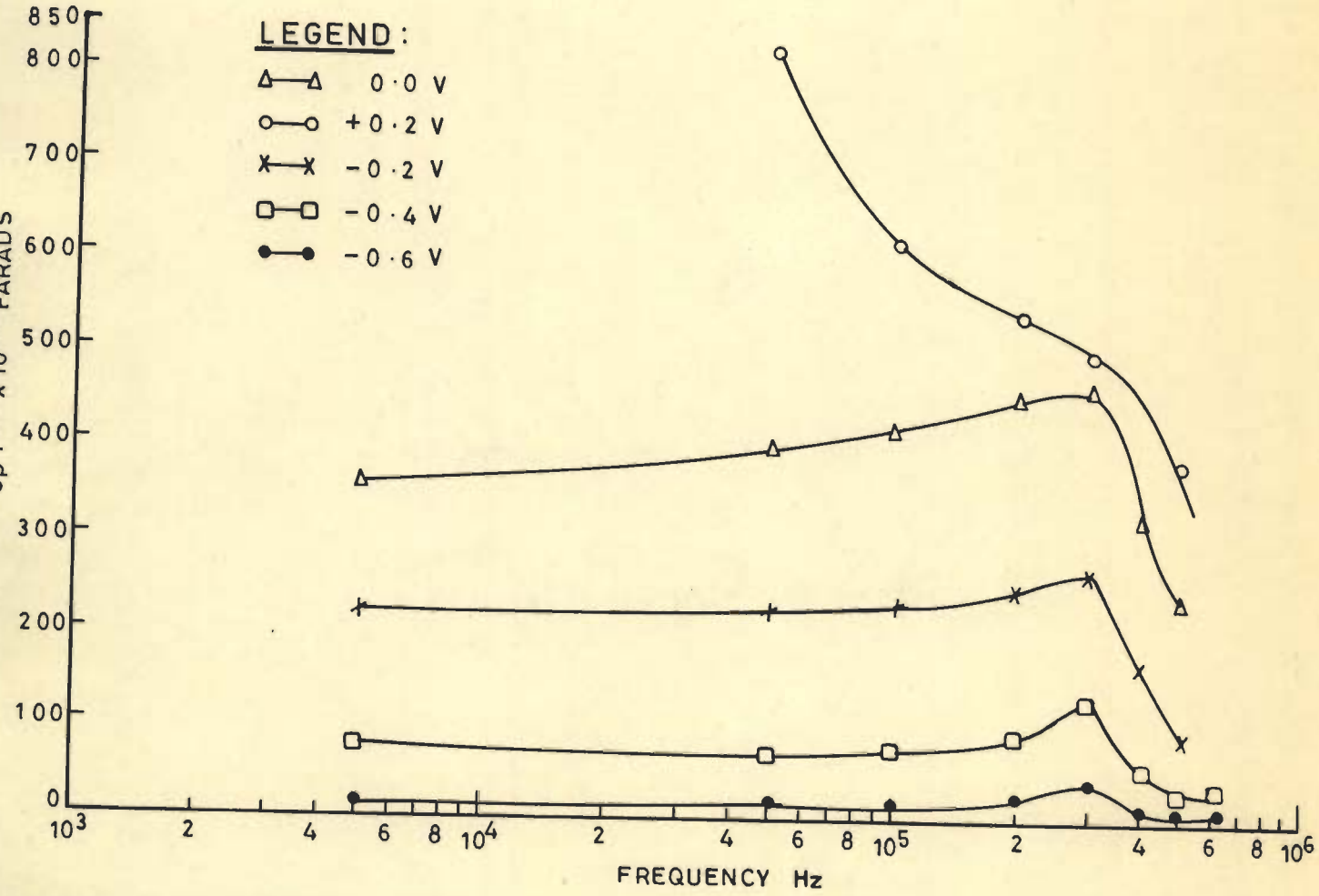


FIG. 5·11 : VARIATION OF PARALLEL CONDUCTANCE (G_p/ω) WITH FREQUENCY AT SEVERAL GATE VOLTAGES FOR MAOS SAMPLE : OXIDE THICKNESS (300 A° SiO_2 + 300 A° Al_2O_3)

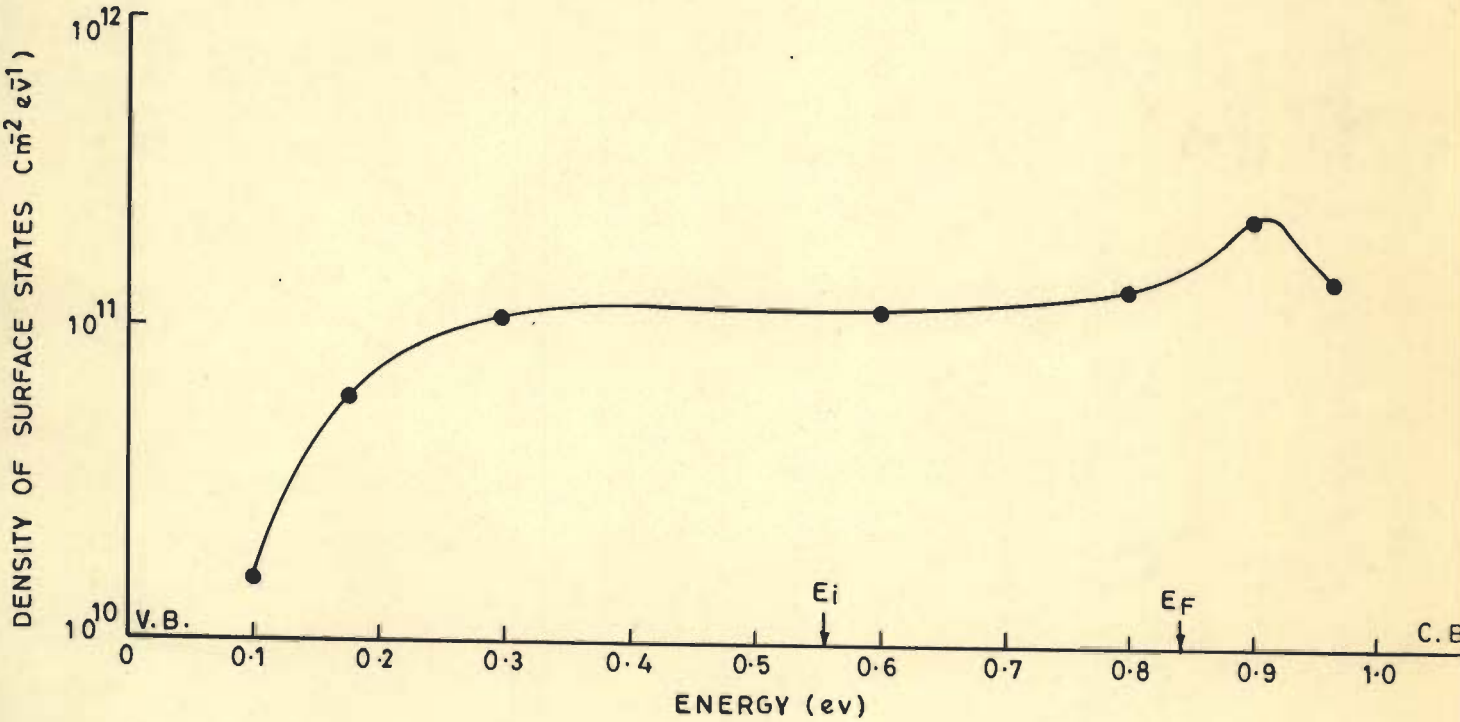


FIG. 5·12: VARIATION OF SURFACE STATE DENSITIES (Nss) FOR MAOS SAMPLES

Experimental results shows that Al_2O_3 film deposited by Vacuum evaporation method is useful for use as gate insulator in MOS devices, either alone or as an auxiliary dielectric with SiO_2. In the reactive evaporation process the substrate is maintained at a low temperature. In the MAOS structure Al_2O_3 may be used in MOS devices to increase the effective dielectric constant of the insulator while maintaining the properties of the silicon/silicon-dioxide interface.

CHAPTER VI

FABRICATION AND PERFORMANCE CHARACTERISTICS OF HUMIDITY SENSITIVE SiO_2 INSULATING FILMS

6.1 INTRODUCTION

In recent years there has been increasing interest in the development of humidity sensors which could be applied to automatic control systems, in industrial scientific and commercial applications as well as in engineering research. In many industries the success of the manufacturing process depends on the control and maintenance of a constant humidity. Therefore there is a need of a reliable, rugged and cheap humidity sensor which could be integrated with the circuits. Several authors have reported the fabrication and performance characteristics of humidity sensors based on MIS structures using porous insulating films as dielectric [108 to 113].

During the C-V measurments on fabricated anodic MOS samples it was observed that some samples which were anodized at higher current densities (i.e. more than 20 mA/cm^2) in an 0.04N KNO_3 Ethylene Glocyol baths which were not freshly prepared were found to be humidity sensitive, their C-V characteristics changed markedly during rainy session when the atmospheric humidity was high in comparison to the C-V measurements conducted on the same samples

during the summer when the humidity was low. On the basis of these observations it was concluded that as the Ethylene Glycol is hygroscopic and since the anodization was not carried out in a freshly prepared electrolyte it has absorbed higher percentage of water and at a higher current density anodization, silicon-dioxide film grown has become porous. Of-course such results were not observed in the samples which were fabricated at low current density and in a freshly prepared bath. On further literature survey it was observed that films grown by anodic oxidation of silicon [114] in an aqueous electrolytes have a high density of pores, where as those produced in a non-aqueous electrolyte were reported to be very dense. Further Schmidt and Owen et. al. [115] reported that Anodic-Oxide films (SiO_2) grown at higher temperatures [65°C] becomes porous. On the basis of the observations noted above it was thought to grow porous films on silicon by anodic oxidation technique at higher current density in an aqueous electrolyte bath at higher temperature and to use these porous films for the fabrication of humidity sensors.

6.2 HUMIDITY SENSITIVE MOS CAPACITOR STRUCTURE

The device as shown Schematically in Fig. 6.1 is a MOS capacitor with a hygroscopic dielectric (i.e. the dielectric absorbs water from the air). The amount of water absorbed depends on the humidity of the air. The high dielectric

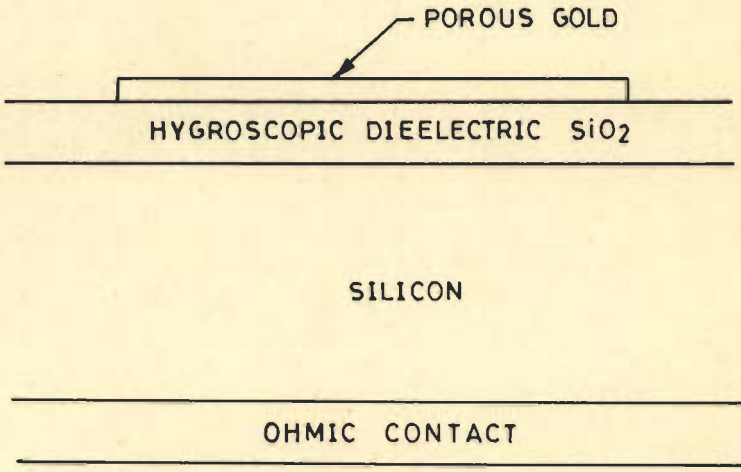


FIG. 6·1 : HUMIDITY SENSITIVE MIS CAPACITOR

constant of water means that this adsorption process will result in a capacitive change in the device. The capacitive change is hence, a measure of the surrounding humidity of the ambient. The top layer of the capacitor is thin and porous and allows free movement of the water vapour.

6.3 SENSOR FABRICATION

The MOS capacitor proposed as humidity sensor was fabricated on 6-8 ohm-cm. n-type epitaxial silicon wafer. The silicon wafer was cut into the chips of size 1 cm x 1cm. The chips were ultrasonically degreased in trichloro-ethylene and rinsed in acetone. An anodization bath was prepared in Ethylene Glycol with 0.04N KNO_3. A 2% water by volume is added to the electrolyte. The anodization set-up is same as described in Section 3.5. The temperature of Electrolyte was kept above the room temperature (Max. was 50°C) during the anodization. The current was first adjusted to 30 mA/cm² by means of the variable series resistance at the 250 volts set on the power supply. Initially the anodization was carried out at a constant current density of 30 mA/cm² by continuously reducing the series resistance from maximum to zero and the process was then allowed to continue at constant voltage until the anodization currnet density decreases to an ultimate minimum limit at which point the anodization was switched

off. The sample holder was taken out from the electrolytic cell and was dipped in Ethylene Glycol for few minutes, and then anodized wafer was removed form the sample holder by dissolving Apiezon Wax in trichloroethylene and finally washed with acetone. An ohmic contact was made at the other side of the chip. The porous top gold film was deposited through a very fine stainless steel gauze and a metallic mask to define a gate area of 0.785 sq. milimeter on the dielectric film. The contacts to the gate and back side were made by connecting very fine copper wires with the silver paint.

6.4 EXPERIMENTAL RESULTS

The capacitance of the sensor was measured as a function of relative humidity on a vector impedance meter. The arrangements used for the measurement of capacitance versus Relative humidity is shown in Fig.6.2. Nitrogen gas was bubbled through water. The flow of the gas was controlled by a needle valve. After that the gas was passed through a copper coil to trap any water coming with the gas. The moisture laden gas then passed in a glass tube containing the sensor, and the outlet from this tube was connected to another sealed glass chamber containing the hygrometer. The entire system was made air-tight. The relative humidity in this system could be increased from 40 percent R_H to 90 percent R_H by adjustment

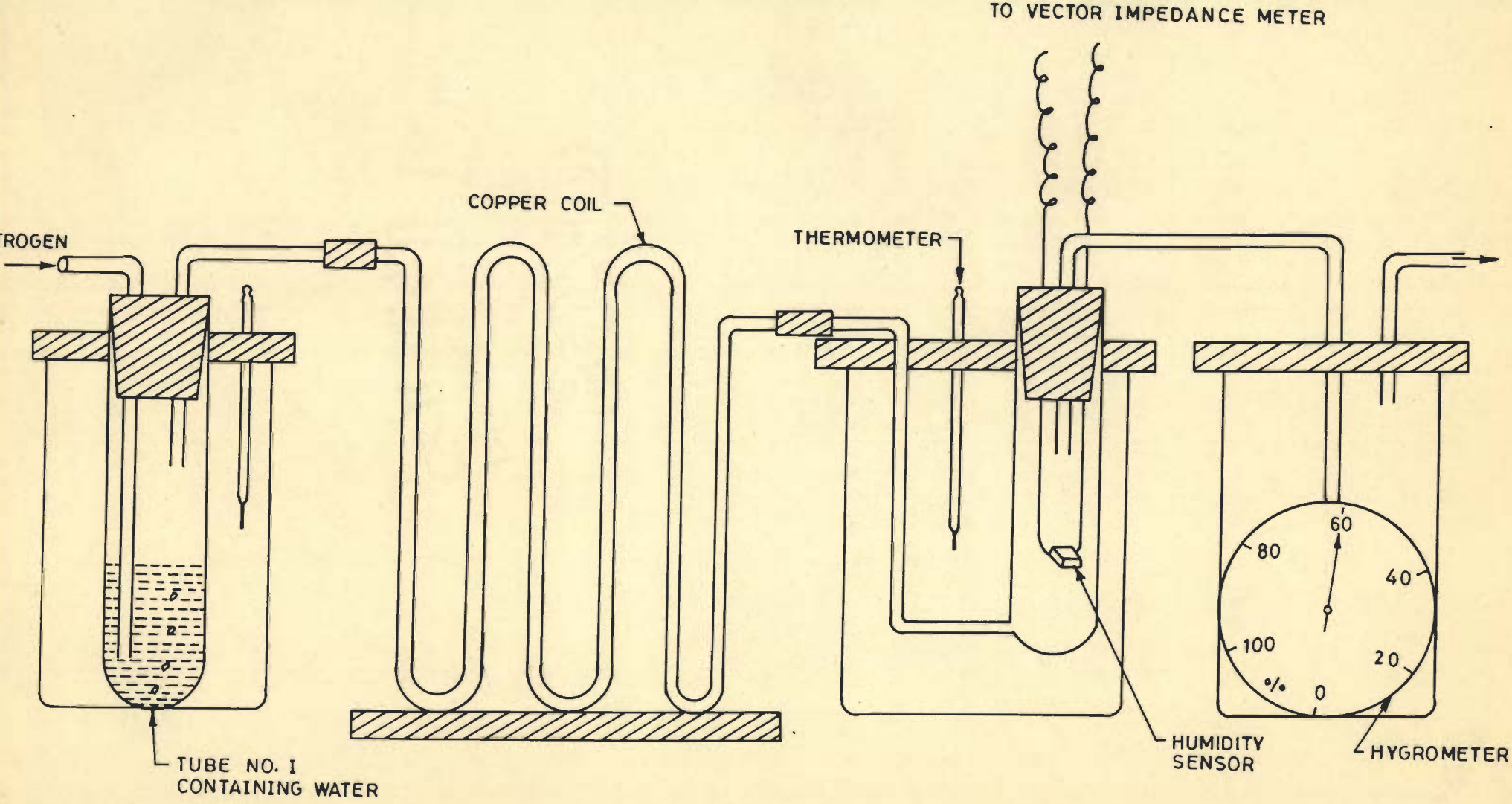


FIG.6·2 : EXPERIMENTAL ARRANGEMENT FOR INCREASING HUMIDITY ABOVE ATMOSPHERIC HUMIDITY

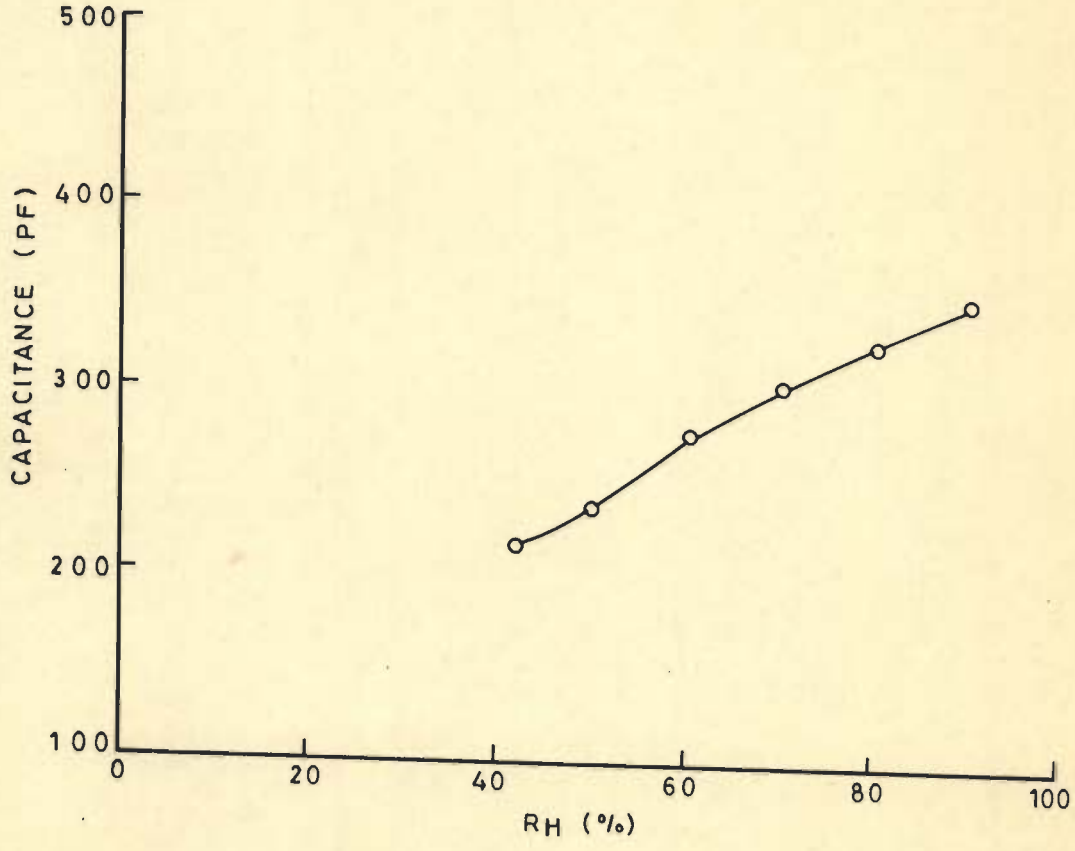


FIG.6·3 : CAPACITANCE VS RELATIVE HUMIDITY (%) CHARACTERISTICS

of gas flow rate and time of flow. Fig. 6.3 shows the typical dependence of capacitance on humidity.

The humidity sensitive characteristics of the MOS structure fabricated by the anodic oxidation of silicon may be used for the fabrication of IC humidity sensors. Silicon is still a dominant material for manufacture of integrated circuits, hence this type of sensors can be fabricated on silicon IC chip as an integral part of the circuit simultaneously with all the other components of the chip preferably using the same processing steps and masks.

CHAPTER VII

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

7.1 INTRODUCTION

The Solid State Electronic Device revolution of the past 20 years has been dominated by devices made from the elemental semiconductor silicon. The complexity of silicon devices during this period has increased from single transistor to thousands of devices on a single chip. With continuous increase in operational functions a new revolution is taking place in the form of VLSI and VVLSI where system or sub-systems are placed on a chip. The growth or deposition of insulating films over silicon is necessary during the entire process of fabrication of modern integrated circuits. With the increase in number of components on a chip it was realized that insulating films grown by thermal oxidation are not very suitable for such high density chips because the high temperature process creates some adverse side effects. To overcome these problems research workers begin to look for some low temperature technique to grow the insulating films on the silicon. In recent years high quality insulating thin solid films has been grown over GaAs wafers by Anodic oxidation technique [71,116,117,118] noting the encouraging results of anodic oxide films on the GaAs, efforts have been made to grow dense oxide film on silicon wafers

using improved anodic oxidation technique and stringent cleaning procedure. The characteristics of the grown films were studied in detail by forming MOS structures.

During investigations it was observed that insulating films of SiO_2 grown under certain anodization conditions becomes porous. Such films may be used to fabricate humidity sensors.

MAS and MAOS structures were also investigated and their characteristics were studied in detail. The present chapter summarizes the work carried out and the conclusions drawn. The scope of future work has also been outlined.

7.2 SUMMARY AND CONCLUSIONS

n-type, $\langle 111 \rangle$ orientation silicon wafers of resistivity 6-8 ohm-cm were used for investigations. A stringent cleaning procedure based on hydrogen-peroxide solutions was used to minimize the contamination of the samples as the stability and reproducibility of device characteristics depends on cleaning procedure used. The electrolytic bath used for anodization was optimized to be a freshly prepared 0.04N KNO_3 solution in Ethylene-Glycol. The anodization was carried out at a constant current density to a predetermined formation voltage and then followed by a constant voltage mode until the current decayed

to an ultimate minimum limit. The constant current density was optimised to be 5 mA/cm², further it was observed that the oxidised samples annealed at 500°C for 30 minutes in an hydrogen ambient gives the best results. Ohmic contacts were made at the back of anodized samples by allowing aluminium film at eutectic temperature (577°C). V-I characteristics of the ohmic contacts were measured which was found to be linear for both the forward and reverse bias voltages, contact resistance of the ohmic contact was measured to be 4.905 ohms. The MOS capacitors were formed by the vacuum deposition of aluminium through a metal mask. The field plate area was typically 3.3×10^{-3} cm^2. Capacitance and conductance measurements were carried over a frequency range of 5 KHz to 500 KHz with the help of Boonton bridge. Signal amplitude was maintained at about 30 mV to have small signal conditions. Surface state density and its distribution in the energy band gap was calculated by the conductance technique. The breakdown field strengthy of the oxide was deduced from the voltage required for castastrophic breakdown of the MOS sample. The dielectric constant of the film was calculated for a known area of aluminium electrode using standard parallel plate capacitance formula. I-V curves were measured with the help of Kiethley Electrometer in a heavily grounded and shielded enclosure. From the I-V curves the resistivity of the grown films were calculated.

The experimental results reveal that the anodically grown films of the order of 300 A° are dense and stable. The frequenecy dispersion and the hysteresis effects in C-V curves are negligible. The dielectric breakdown strength is 1.2×10^7 V/cm, the calculated value of dielectric constant is 4.08, and the resistivity of the dielectric layer is of the order of 5.33×10^{15} ohm-cm. The minimum value of interface state density determined by conductance method is 4×10^{11} states cm^{-2} ev^{-1}.

The reported [119,120] values of dielectric breakdown strength of a carefully grown silicon dioxide film by thermal oxidation varies from 6×10^6 to 10^7 volt/cm, resistivity varies from 10^{15} to 10^{17} ohm-cm, and surface state density near midgap is 10^{10} states cm^{-2} ev^{-1}. The comparison shows that the dielectric properties of anodically grown films of the order of 300 A° are comparable to that of thermally grown films. The surface state density of fabricated samples are on the higher side, the vlaue may be reduced further by improving the clean room facilities and by using chemicals of semiconductor grade purity.

The anodic oxidation for the growth of the films of thickness of the order of 300 A° has following distinct advantages over the thermal oxidation process:

(i) Growth of the oxide take place at room temperature and therefore the Si/SiO_2 interface is not subjected

to any thermal stress as in the case of thermal oxidation process.

(ii) Maximum temperature used during the sample fabrication is 500°C hence there are less chances of producing the stacking faults and shifting of shallow diffusion junctions previously formed in the chips.

(iii) The thickness of the oxide layer can be controlled easily by adjusting the forming voltage.

With the scaling down of device dimensions the use of thin, oxide films of the order of 100 A° having high dielectric breakdown strength and resistivity are finding importance in VLSI and MOS technology.

The quality of the anodically grown films deteriorates as the thickness of the grown films increases above 600 A°. The deterioration of the dielectric properties in the anodically grown films may be due to heat produced by high constant current density at higher forming voltages applied across the anode and cathode in the electrolyte. Since the growth rate of anodically grown silicon dioxide films is of the order of 6 A°/V, therefore to grow a SiO_2 film of the order of 1200 A° a forming voltage of 200 V is desired hence more heat will be produced in the electrolyte

bath causing deterioration to the grown film.

On further investigations it was observed that the anodization of silicon at higher current density of the order of 30 mA/cm² in an electrolytic bath of 0.04 N KNO_3 in Ethylene-Glycol with 2% of water by volume at elevated temperatures results in porous films whose characteristics varies with the humidity of the surrounding environment. The capacitance of the MOS structure using porous films of SiO_2 was measured as a function of relative humidity. Results show that the since capacitance-humidity characteristic is practically liner. Hence SiO_2 films can be used to realise humidity sensors. The proposed sensors may be suitable to fabricate I.C. Sensors as it can be fabricated on silicon I.C. chips as an integral part of the circuit.

Silicon dioxide films are unable to provide positive flat-band voltage values relative to silicon, further the films are also radiation sensitive. The dielectric constant of Sio_2 is also relatively low. To overcome these shortcoming Al_2O_3 films have been used by several workers.

As the aim was to grow or deposit the insulating films at low temperatures, it was opted to deposit the Al_2O_3 films on silicon by reactive evaporation which is essentially a low temperature technique. Characteristics of MAS and MAOS structures were studied in detail.

For the fabrication of MAS structures Al is evaporated in a vacuum coating unit under partial pressure of oxygen. During evaporation the partial pressure of oxygen was maintained in the range of 10^{-3} torr. The deposition rate of Al_2O_3 was optimised to be 10 A°/min, and the films were deposited on the substarte kept at 300°C. The fabricated MAS samples were annealed in the atmosphere of oxygen at a temperature of 400°C. The ohmic contacts were made at the back of the samples and Al electrodes were deposited onto the oxide surface. C-V and G-V characteristics of the fabricated MAS samples were measured in the frequency range of 5 KHz to 500 KHz. The dielectric constant, dielectric strength and interface state density were determined. Experimental results reveals that the C-V curves are shifted to the right side in comparison to ideal curve showing a positive flat band voltage of about 0.3 volts. Measured C-V curves show a frequency dispersion in the accumulation region, and the plotted C-V curves shows a hysteris effect in the clockwise direction which indicate electron trapping. The hysteresis effects are diminished by post deposition annealing in O_2. The dielectric constant of the films lies in the range of 7.5 to 8. At the middle of the gap the surface state density is about 4×10^{11} states cm^{-2} ev^{-1}.

MAOS samples were fabricated first by growing SiO_2 film of thickness of the order of 300 A° by anodic oxidation technique on n-type epitaxial silicon wafers. Oxidised

wafers were annealed in H_2 atmosphere at a temperature of 500°C for 30 min. A film of Al_2O_3 of thickness of the order of 300 A°was deposited by reactive evaporation of Aluminium over the silicon dioxide layer. The fabricated MAOS samples were annealed in O_2 atmosphere at a temperature of 400°C for 30 minutes. Ohimic contacts were made at the back side of the samples and aluminium dots of area 3.3×10^{-3} cm^2 were evaporated on the composite oxide surface. C-V and G-V measurements were carried out at frequencies in the range of 5 KHz to 500 KHz. The experimental results show that for MAOS structure C-V curves are having negative flat band voltage. A negligible frequency dispersion. The structure did not show any hysteresis effect. The dielectric constant of the composite structure is of the order of 6.0. At the middle of the gap the surface state density is about 1.4×10^{11} states cm^{-2} ev^{-1}. It is concluded that MAOS structures may beused in MOS devices to increase the effective dielectric constant of the insulator while maintaining the properties of the silicon-silicon dioxide interface.

7.3 SUGGESTIONS FOR FUTURE WORK

Rao et al. [121] has investigated the properties of Al-Al_2O_3-Al capacitors formed by the anodization of aluminium films at 0°C and compared their properties with the capacitors formed at room temp. and reported that an improved dielectric formaition resulted from anodization

at 0°C. Similar results were also observed in case of growth of native oxides on GaAs by anodic oxidation techniques at low temperatures (below room temperatures) [122 to 124]. These observations suggests that if the anodic oxidation of silicon may be performed in electrolytes at temperatures preferably below 0°C more encouraging results may be achieved, the dielectric films grown may have higher dielectric strength and resistivity and more thicker films may be grown without deterioration of their electrical and interfacial properties.

APPENDIX

AUTOMATIC C-V PLOTTER AND MICROMANIPULATOR PROBE STATION

A.1 INTRODUCTION

C-V characteristics of MOS structures play an important role in the study of the hystersis effects and the interfacial properties of the devices. Point to point measurements are very laborious and time consuming. Therefore for the automatic and rapid plotting of C-V characteristic, a system was developed and fabricated [125].

In 1975 K.E.Forward et. al [126] reported an automatic C-V plotter which employes a noval current sensing circuit. The system was highly sensitive and enabled the capacitive component to be distinguished from the conductive component. A current sensing circuit similar to Forward et. al. is used to plot the incremental capacitance as a function of bias voltage. IC LM1496 is used as a phase sensitive detector to detect the inphase component of the applied voltage which is proportional to the capacitive current flwoing through MOS sample. A linear ramp-generator is used to apply the variable bias. In addition to phase-sensitive detector and the ramp-generator, a laboratory standard signal generator and X-Y recorder were also used.

A schematic block diagram of the complete system is shown in fig. A-1. The system comprises of an input Circuit, low frequency and high frequency amplifiers, variable ramp-generator, phase-sensitive detector, output amplifier, sinusoidal signal generator and X-Y recorder. The details of each one of these units except the signal generator and the X-Y recorder which were available in the laboratory have been described here.

A.2 CURRENT SAMPLING CIRCUIT

The basic principle used here is that a sinusoidal signal V(w) is applied to the capacitor C under test in series wich a standard capacitor C_s of the value much larger than C, as shown in Fig. A.2. The voltage across the standard capacitor $v_s = v \frac{C}{C_s}$; v_s would be in phase with v if C and C_s are purely capacitive. A resistance R_s of very high value is connected across C_s to provide the required d.c. bias voltage across the capacitor under test. To obtain accurate results, the values of R_s and C_s are shown such that $C_s >> C$, $R_s >> \frac{1}{\omega C_s}$ and $R << R_{dc}$ where R_{dc} represents the leakage resistance of the sample under test.

A.3 AMPLIFIERS

The output voltage from the currrent sampling capacitor being small is required to be amplified. The C-V plotter

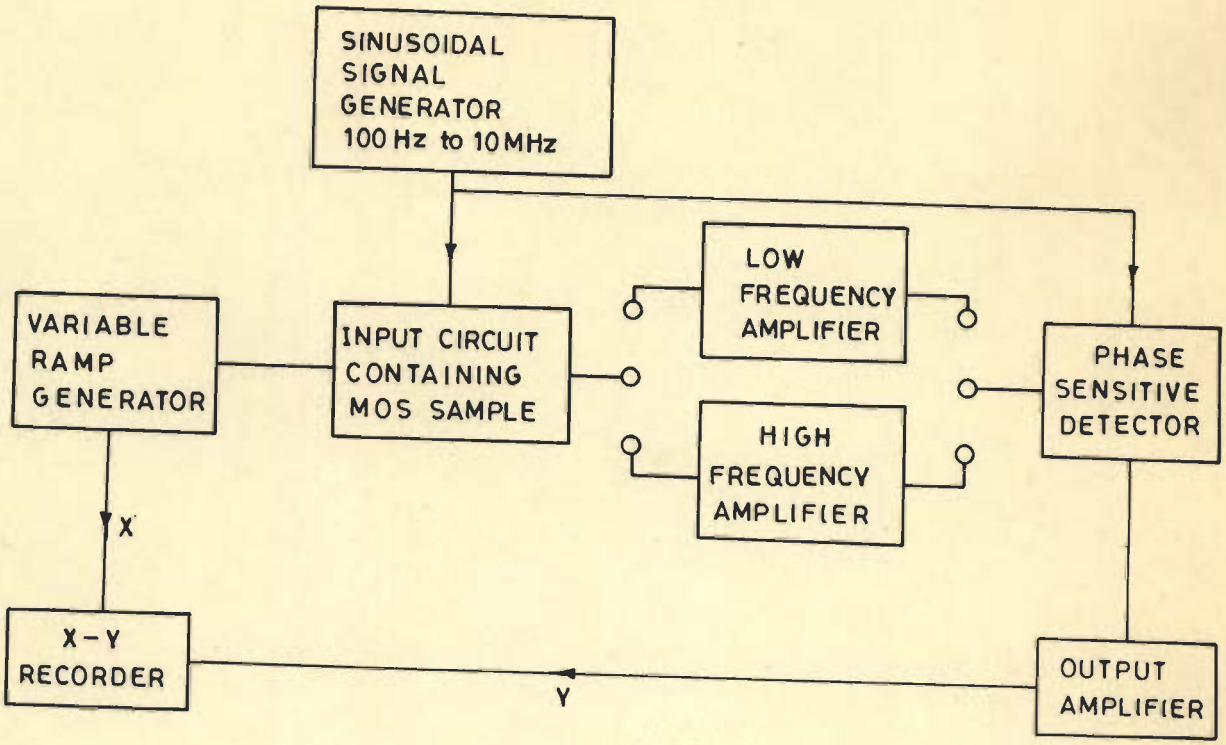


FIG. A·1: BLOCK DIAGRAM OF AN AUTOMATIC MOS C-V PLOTTER

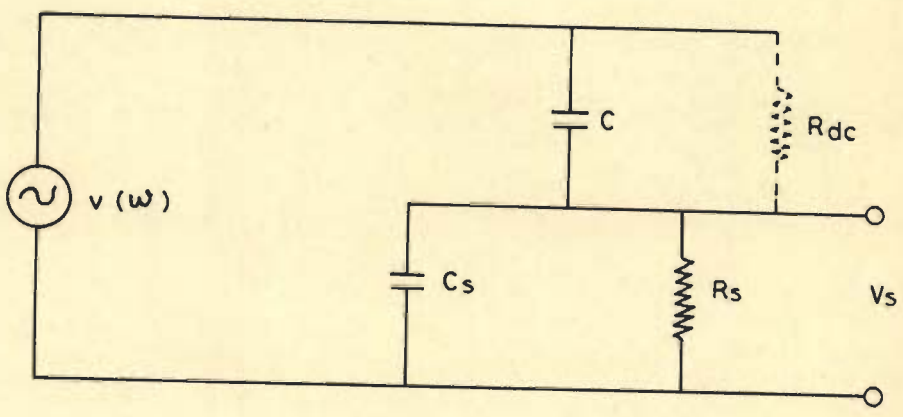


FIG. A·2: INPUT CIRCUIT

has been designed to operate from 100 Hz to 1 MHz. Two amplifier circuits have been designed and fabricated to cover the entire frequency range. One to amplify low frequencies in the range of 100 Hz to 100 KHz and another to amplify high frequency from 100 KHz to 1 MHz. The low frequency amplifier is a 3 stage R-C coupled transistorised amplifier with a FET at input stage to obtain high input impedance. For amplifying high frequencies two stages of IC differential video amplifier LM 733C is used. The gain of first stage was adjusted to 40 dBs and the second stage 20 dBs. High frequency amplifier is assembled on a glass EPOXY printed circuit board, to obtain good results, to reduce noise pickup circuit was properly grounded and shielded.

A.4 VARIABLE RAMP GENERATOR

A R-C circuit has beenused as an integrator to integrate a step-input. Three resistances of (1M ohm, 20M ohm, 50M ohm) have been employed to provide different sweep rates to the integrator. A switch S_1 is used to select one of the required resistances. To obtain a particular value of the voltage for a given time, a switch S_2 was provided. During the hold position the dual junction FET 2SK18 provides a low drift rate to the integrator. The complete circuit is shown in Fig. A.3.

A.5 PHASE-SENSITIVE DETECTOR

The phase sensitive detector compares the amplified information signal v_s (the current strength through the MOS sample) against the reference signal v and produces a d.c. output signal which is proportional to the capacitive current flowing throgh the MOS capacitor under test. IC LM1496 is used as a phase sensitive detector which operate upto 100 MHz. The output signal is fed as one input to the X-Y recorder, (Philips PM 8120). The d.c. bias across the MOS sample was fed to second input to X-Y recorder. For fast sweep rates an X-Y oscilloscope may also be used for displaying the C-V curves. The circuit of the phase sensitive detector is shown in Fig. A.4.

A.6 SAMPLE HOLDER AND PROBE STATION

The C-V, G-V, and I-V measurements of MOS structures are desirable to be made immediately after their fabrication at room temperature and in air. For this purpose a special sample holder, shown in Figs. A.5, A.6 was developed and fabricated in the laboratory. Two terminals of the capacitor are the gate electrode and the back ohmic contact. The grounded metal enclosure around the MOS capacitor provides the effective shielding and works as the third terminal for the measurement.

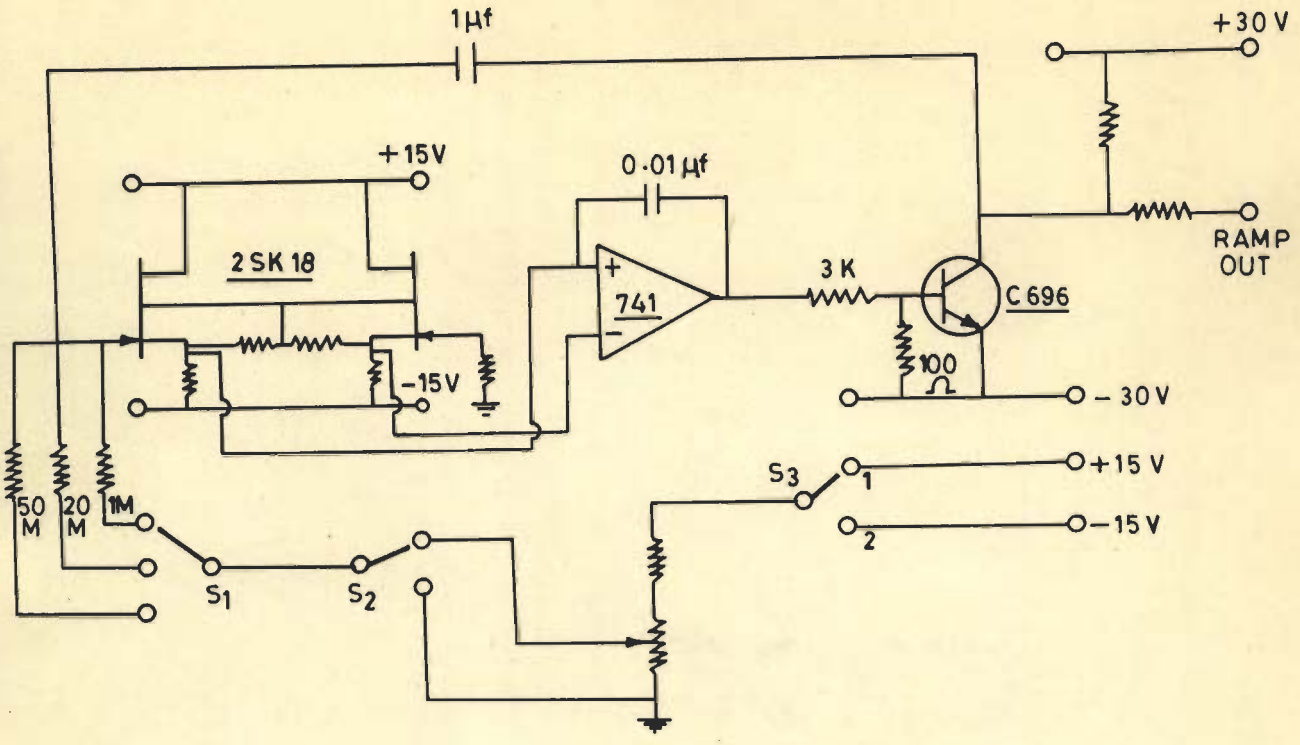


FIG. A·3 : VARIABLE RAMP GENERATOR

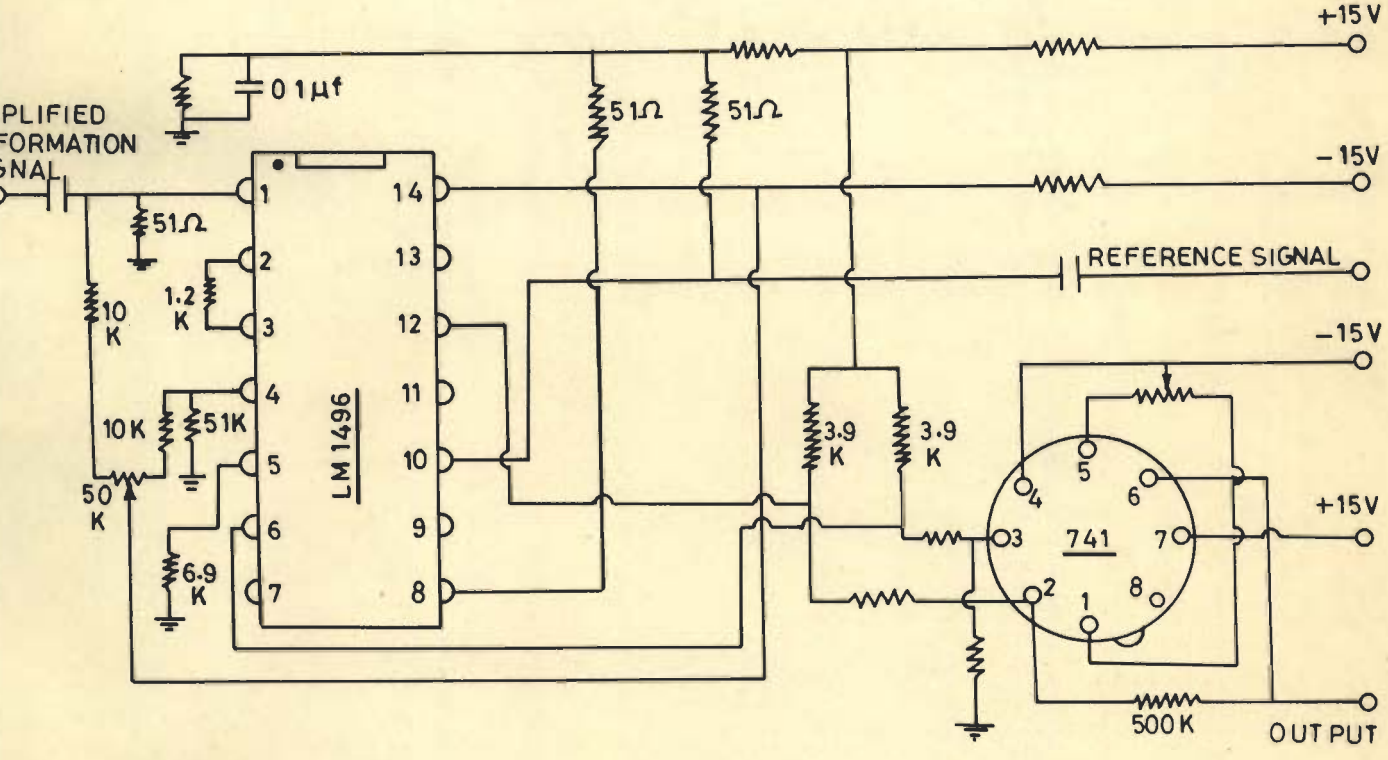


FIG. A·4 : PHASE SENSITIVE DECTOR

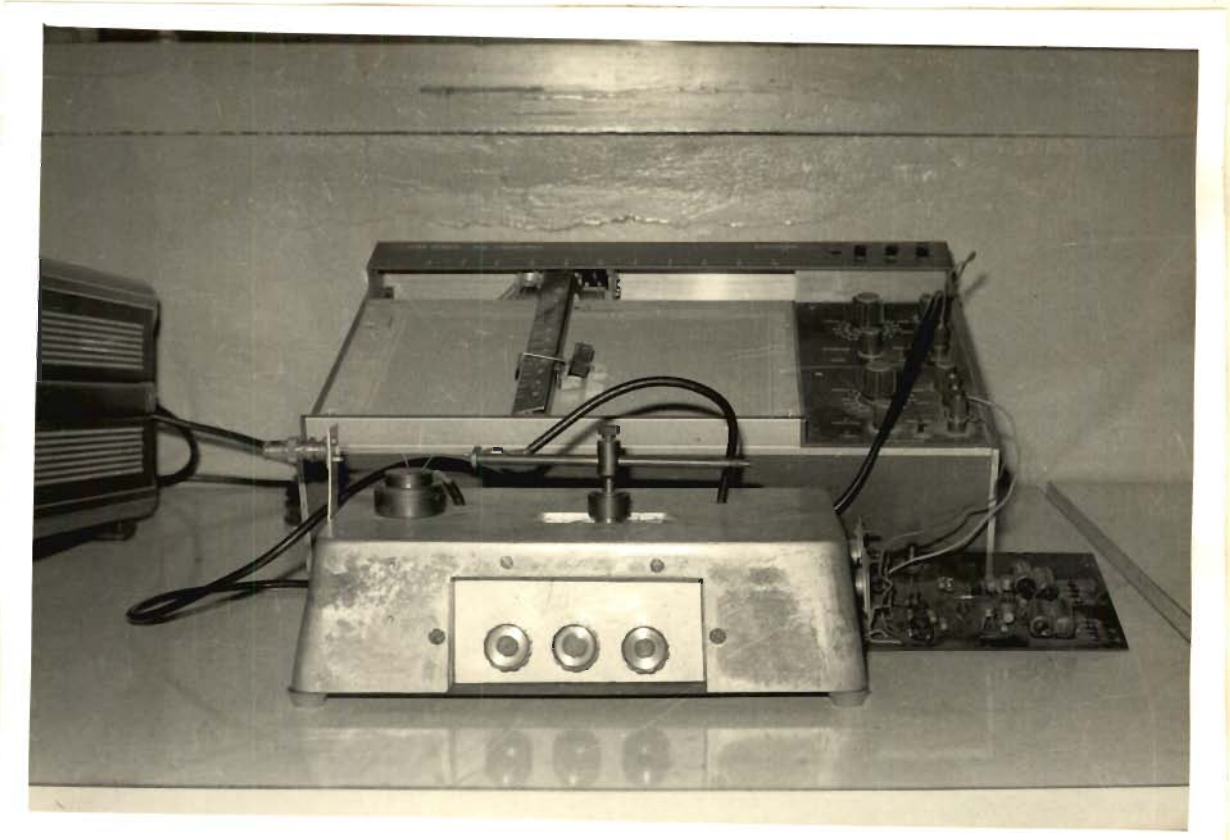


FIG. A·6 : MICROMANIPULATOR PROBE STATION WITH X-Y RECORDER

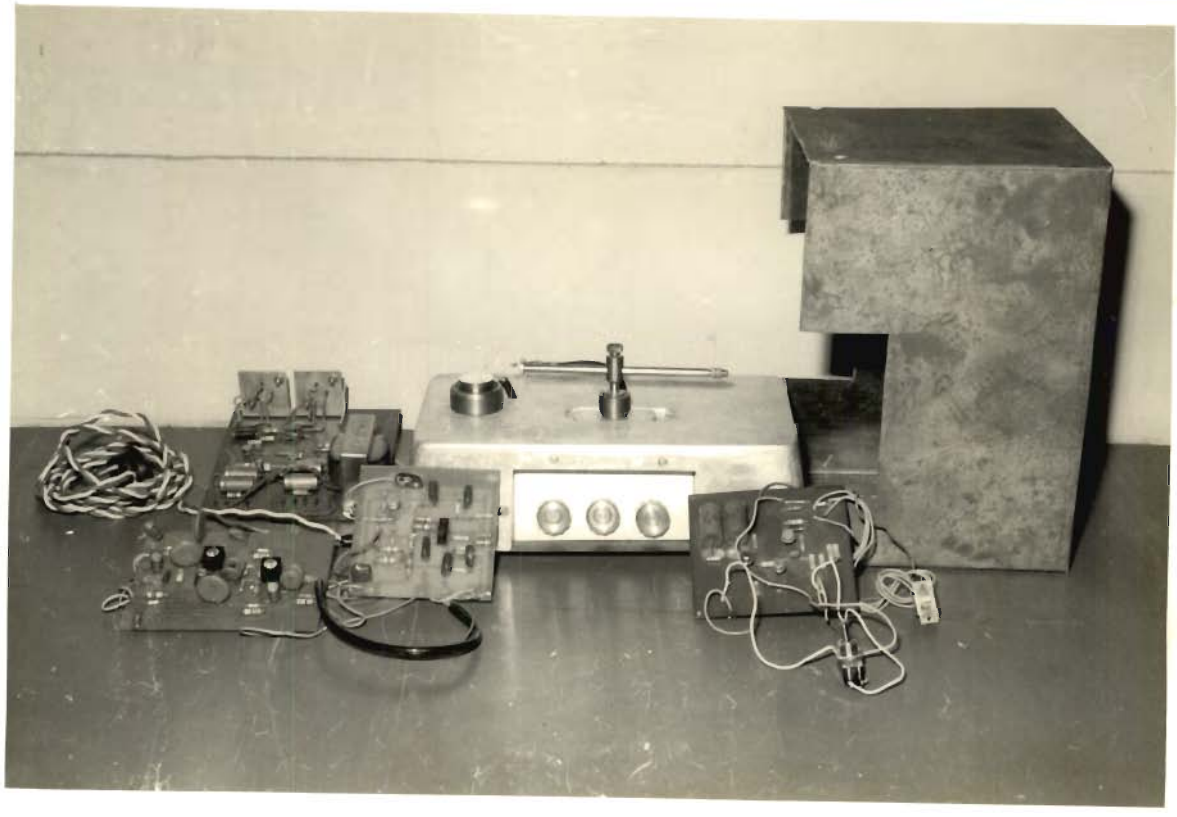


FIG. A·5 : MICROMANIPULATOR PROBE STATION

A.6.1 PROBE BOX

The probe box was designed to meet the following three requirements.

(i) To make three-terminal capacitance measurement, the probe box must be made of metal maintained at ground potential.

(ii) The metal box must be light proof.

(iii) The ambient in the metalbox must be dry to avoid leakage currents flowing along the oxide surface between the gate electrode and the back contact of the MOS sample.

The metal enclosure was fabricated of aluminium sheet and was connected to a specially prepared earth point.

A wire probe mounted on the micromanipulator and insulated from the ground is used to contact the gate of an individual MOS capacitor on a fabricated sample. To avoid high contact resistance to aluminium gates a gold wire 5 to 10 mils in diameter of about one inche length is used. The gold wire is mounted horizontally and having a bend of 15-20° angle to the horizontal to provide the pressure to the contact. Mechanical arrangement

were made to move the probe wire in three mutually perpendicular directions, labeled X,Y,Z making it easy to position the probe wire on a small gate or contact pad area.

A.6.2 PEDESTAL

To make good electrical contact to the wafer a gold plated brass plate or pedestal is used. The pedestal is designed making three-dimensional capacitance measurements. To ensure a good electrical contact the pedestal is gold plated to avoid oxide layers. To hold the wafer tightly against the pedestal, Pedestal was connected to vacuum pump to hold the wafer through a small hole. To make three-terminal capacitance measurements and to isolate the pedestal from the ground, it is supported in the probe station on TEFLON base.

All the connections were made through BNC connectors by 50 ohms coaxial cable.

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