IMPROVED SCHEMES FOR BUSBAR AND BREAKER-FAILURE PROTECTION

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STUDENT'S DECLARATION

I hereby certify that the work presented in the thesis entitled "**IMPROVED SCHEMES FOR BUSBAR AND BREAKER-FAILURE PROTECTION**" is my own work carried out during a period from July, 2015 to November, 2019 under the supervision of Dr. Bhavesh R. Bhalja, Associate Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee.

The matter presented in the thesis has not been submitted for the award of any other degree of this or any other Institute.

Dated: **(SOUMITRI JENA)**

SUPERVISOR'S DECLARATION

This is to certify that the above mentioned work is carried out under my supervision.

Dated: (**Bhavesh R. Bhalja)**

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Abstract

Electric power substations across the globe have undergone immense transitions in the past decade. With the introduction of state-of-art modern equipment and power electronics overhaul, complexity of busbar configurations has been significantly increased. Busbar in a substation, as a converging point of transmission lines and connection point of sophisticated equipment, requires meticulous and reliable protection. Though busbar faults are relatively fewer, the consequences are severe in terms of damaged equipment and widespread supply interruption. These repercussions alarm protection engineers about the need for reliable and secure busbar protection. The high MVA levels, extensive interconnections, complex arrangements, and safety of connected equipment further necessitates faster operation of the busbar relay. Clearance of a busbar fault requires the opening of all line circuit breakers (CBs) connected to the busbar, which results in supply interruption in no small part of the power system.

On the contrary, the consequences of an unprotected bus during a bus fault is catastrophic. The present practice is to reduce the fault clearance time of the relay rather than developing new arc extinction methods for the CBs. Hence, busbar protection should be designed and implemented in such a way that it operates in every single instance of bus fault and avoids unwanted tripping because of any possible reason. Stability is another prime aspect while designing a bus zone relay as its mal-operation causes power outage to a large portion of the power system. Hence, bus protection is challenging in terms of reliability and speed. By implementing bus sectionalizers and duplicated bus arrangements, the part of the circuit to be interrupted can be minimized. An internal bus fault, in this case, disturbs only a smaller part of the substation and fewer components are affected. Enhanced numerical data processing units introduce implementation of numerical relays into the area of busbar protection. They provide greater flexibility and possible on-chip implementation of smart solutions.

Hence, choosing excellent mathematical analysis tools and algorithms has the utmost significance to provide highly reliable and fast busbar protection, which also ensures stable and secure operation of the entire grid.

Further, to improve the system reliability, all the protection equipment are duplicated at a substation. However, duplication of a CB is not suitable because of economic and functional constraints. A CB is monitored by Breaker-Failure Protection (BFP) implemented as a supplementary function inside existing relays. For several years, power system engineering has provided realistic BFP as a local solution to high-voltage (HV) and EHV (EHV) systems. The role of BFP is to identify a failed breaker to interrupt current and to operate with a pre-defined time delay. Owing to the limitations of current technology, such as inaccurate timers with slow-reset over-current elements, BFP has been historically seen as the main reason for mal-operation of large number of relays and subsequent blackout situations. Keeping the severe consequences of a busbar fault in mind, protection engineers try to clear the fault in the minimum possible time. This time must be within the critical fault clearance time as determined from the system stability point of view. With the shrinking of stability limits, a fast BFP function is more challenging to achieve. The total BFP time is decided from the worst-case scenarios of principal protection operating time, tripping time of primary breaker, and pickup/dropout time of BF threshold functions. Within the total BFP time of 10 - 12 cycles, often only one cycle is available for the BFP reset/response time in case of mal-operations. The recent developments in the field of numerical relaying, digital signal processing, and high-class Current Transformers (CTs) allow the implementation of improved BFP modules with substantial performance enhancement.

The work presented in this thesis is concentrated upon the development of improved busbar and BFP techniques. In this work, using both numerical and statistical analysis such as LR, alpha plane characteristics, travelling wavefronts and dq-components, it has been demonstrated that the sensitivity and response speed of existing busbar protection schemes can be improved. This work also emphasizes on the development of an integrated busbar and breaker-failure scheme that prevents the mal-operation from subsidence current. Furthermore, the probable on-field implementation procedures and architectures of the proposed schemes has also been discussed in details.

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List of Abbreviations

29	Isolator
50BF	Breaker-Failure over current element
52	Circuit Breaker
52a	Circuit breaker auxiliary contact
62	Delay timer
87	Differential relay
87B	Low-impedance busbar differential protection
87Z	High-impedance busbar differential protection
87BD	Low-impedance differential protection based on direct-axis current
87BW	Low-impedance differential protection based on wavelet coefficients
μs	micro seconds
A	Ampere
AC	Alternating Current
ACC	Accuracy
ADC	Analog-to-Digital Converter
AI	Artificial Intelligence
ANN	Artificial Neural Network
AUC	Area Under the Curve
BC	Bus Coupler

BFI	Breaker Failure Initiation
BFP	Breaker-Failure Protection
BFPN	Breaker-Failure Protection (New)
CB	Circuit Breaker
CCVT	Coupling Capacitor Voltage Transformer
CCS	Code Composer Studio
CF	Correction Factor
Coif	Coiflets
CSSCC	Current Sensor Signal Conditioning Circuit
CSV	Comma Separated Values
CT	Current Transformer
CWT	Continuous Wavelet Transform
Db	Daubechies
dB	decibel
DAC	Digital to Analog Converter
DAU	Data Acquisition Unit
DC	Direct Current
DFT	Discrete Fourier Transform
DSO	Digital Storage Oscilloscope
DSP	Digital Signal Processing
EHV	extra-high-voltage
emf	Electromotive force
EMTDC	Electro-Magnetic Transient Design and Control
FIA	Fault Inception Angle
FN	False Negative

FP	False Positive
GAP	Generalized Alpha Plane
GHz	Giga Hertz
GOOSE	Generic Object Oriented Substation Event
GPS	Global Positioning System
GS	Giga Samples
GT	Generator Transformer
HIF	High Impedance Fault
hp	horse power
HV	high-voltage
HVDC	High-voltage Direct Current
Hz	Hertz
ICT	Inter Connection Transformer
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IS	Isolators
kA	kilo Ampere
kb	kilo byte
kHz	kilo Hertz
kV	kilo Volt
kW	kilo Watt
LES	Least Error Square
LG	Line to Ground
LL	Line to Line
LLG	Line to Line to Ground

LLLG	Line to Line to Line to ground
LR	Logistic Regression
Mbps	Megabits per second
MDFT	Modified Discrete Fourier Transform
MODWT	Maximum Overlap Discrete Wavelet Transform
MOV	Metal Oxide Varistor
ms	milli seconds
MU	Merging Unit
MVA	Mega Volt Ampere
MWSV	Maximum Wavelet Singular Values
NC	Normally Closed
NO	Normally Open
PC	Personal Computer
PSCAD	Power Systems Computer-Aided Design
PSD	Power Spectral Density
RBF	Radial Basis Function
RMS	Root Mean Square
ROC	Receiver Operating Characteristics
RST	Reset
RVM	Relevance Vector Machine
RX	Receiver
SAS	Substation Automation Systems
SI	Source Impedance
SNR	Signal-to-Noise ratio
SV	Sampled Values

SVM	Support Vector Machine
Sym	Symlets
TN	True Negative
ToA	Time of Arrival
TP	True Positive
TW	Travelling Wave
TX	Transmitter
UAT	Unit Auxiliary Transformer
UHV	ultra-high-voltage
VA	Volt Ampere
WM	Wavelet Matrix
WPT	Wavelet Packet Transform
WT	Wavelet Transform
WTMM	Wavelet Transform Modulus Maxima

Chapter 1

Introduction

Traditionally, implementing busbar protection is one of the difficult aspects of power system protection. A busbar is one of the most critical elements in the power system as it is the connection point of various substation equipment. The occurrence of a busbar fault may cause loss of all connected equipment, which has the same disastrous effect as that of a large number of simultaneous faults. If busbar protection is not implemented then all the remote-end sources have to be tripped in the event of a busbar fault. The busbar section in a substation is not physically very complicated but several aspects need to be entertained to provide reliable bus protection.

The occurrence of busbar faults is rare compared to the transmission lines. Out of the total number of faults in a power system only 6-7% faults occur on the busbar, while 60% of the faults occur on transmission lines. One set of statistics on the causes of busbar faults and the frequency of occurrence has been shown in Fig. 1.1. It is interesting to note that the highest number of faults are caused by human error, like leaving the safety ground connected to the busbar after regular maintenance or accidental contacts. It is evident from Fig. 1.2 that a major portion of busbar faults involve ground [1]. Apart from this, insulation failure and flashover are the major reasons of busbar fault.

Protection of busbar is very critical as clearance of bus fault would need tripping of all the breakers of the bays (lines) connected to the faulted busbar. Such a tripping can potentially lead to widespread instability of a power system [2]. Due to increase in voltage level, complex configuration of busbar arrangements and extensive interconnection, the stability of generators becomes a critical condition, which requires faster and

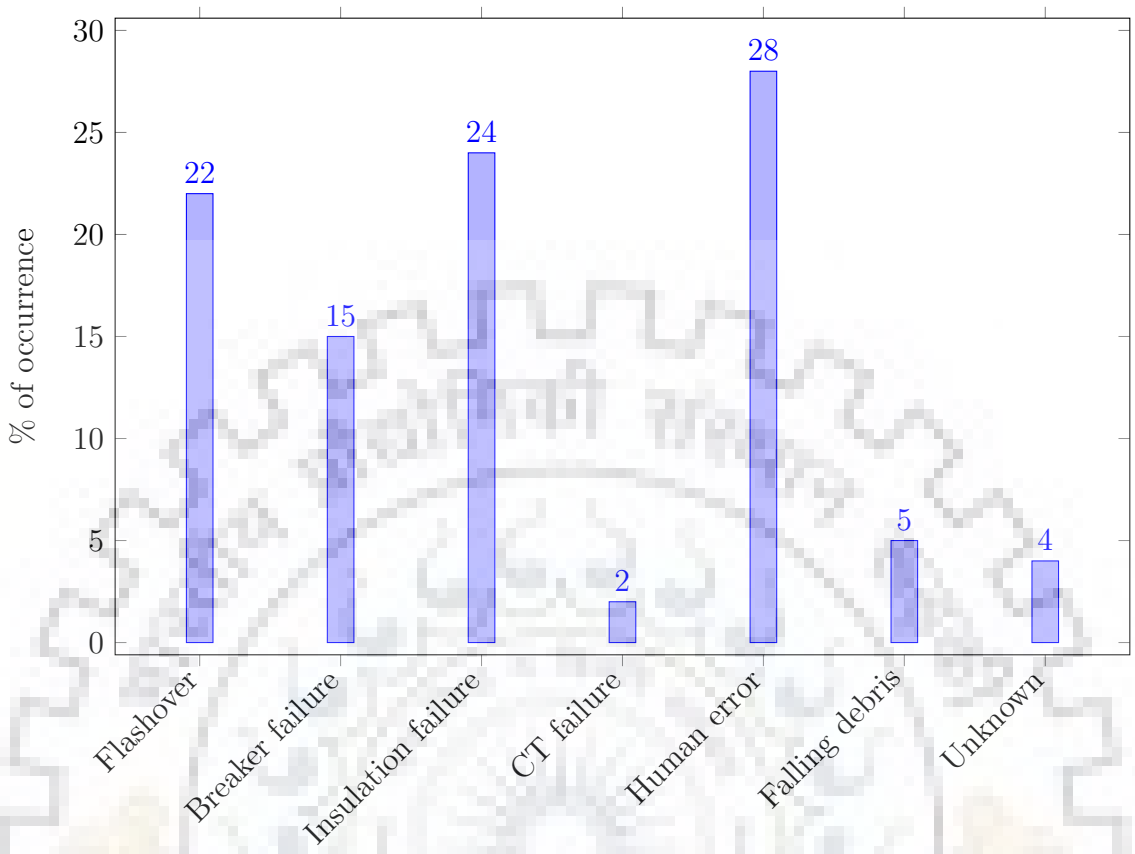

Fig. 1.1: Causes of busbar fault with their percentage of occurrence.

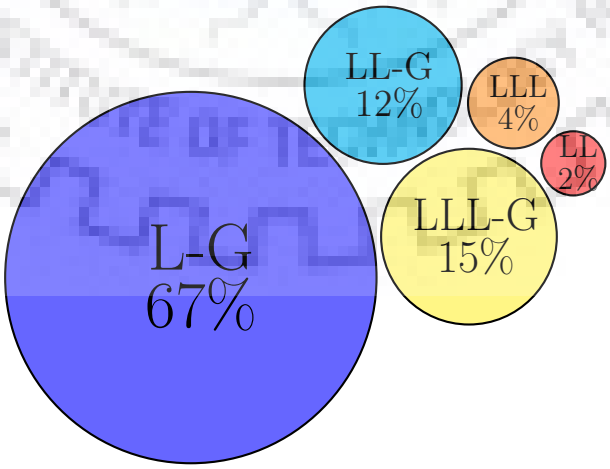

Fig. 1.2: Different types of busbar faults.

reliable operation of the relay for a severe bus fault [3]. Therefore, it is vital to develop separate busbar protection scheme that not only prevents hazards to the system but also minimizes interruption of power by utilizing a sectionalized and duplicated busbar arrangement. At the same time, it also prevents unwanted tripping of all the bays in heavy through faults. The high MVA level associated with the bus zone area demands a fast and reliable protection scheme for different busbar configurations [4]- [5].

Conventionally, differential protection schemes are employed in utilities for the primary protection of the buses. Although busbar faults are not frequent, occurrence of it leads to disruptive consequences. Busbar relays are to be designed for fast and reliable operation in case of busbar faults and stable operation in worst case close-in external fault scenarios. Maintaining both reliability and stability of busbar protection schemes have remained challenging over a very long time.

1.1 Busbar Protection Requirements

A counter-argument is usually presented against the employment of dedicated busbar protection, as it may lead to unnecessary tripping of a large portion of the power system. Accidental tripping maybe because of the failure of instrument transformers, human error, improper relay settings, or any other operational failure. If dedicated protection is not practiced in the substation, a busbar fault may be cleared by the backup protection provided for the lines connected to the bus. However, clearance of the fault is rather slow, which can not be compromised because of its severity. Slow clearance of the busbar fault may lead to transient stability problems as a busbar fault may lead to multiple line outages. Furthermore, slow clearance is also very dangerous for the working personnel in the substation. Hence, though infrequent, busbar faults require a dedicated protection unit.

Selectivity is one of the prime aspects of busbar protection. The bus zone relay should restrict itself to faults on that particular bus zone. In this way, the CBs corresponding to that particular region are disconnected, and the remaining healthy part is unaffected. With dynamic bus configurations, the relay should be fast enough to adapt any change in zone configurations. This discriminating property minimizes supply interruption and enhances system reliability.

Stability against a wide range of external faults, particularly in CT saturation scenarios, remains the primary concern for protection engineers while designing a busbar relay. To restrain the operation of the relay in such scenarios, the fast few milliseconds of fault inception are crucial. If such mal-operations are not prevented, supply interruption to a large portion of the power system is inevitable.

High-speed tripping is necessary to limit the damage caused by busbar fault, which becomes more significant in case of high voltage substations because of high fault current. The fault clearance time of the busbar protection unit should be less than that of the backup protection of the connected lines. If backup protection fault clearance time is less than that of the busbar protection unit, then there is no need of the dedicated unit.

Security of the protection unit can be improved by appropriate substation design and dividing the bus zone into multiple zones. An internal busbar fault, in this case, affects only a smaller part of the substation and fewer components are affected. Hence, larger busbar protection zones should be divided into smaller zones to improve security. Some may argue that with a perfect substation design, there is little need of separate protection unit.

Digital relays are the most economical and effective means of busbar protection which requires fewer hardware alterations for new system changes. The first commissioned digital busbar system has taken many alterations. Now more than 500 types of systems are used worldwide with different types of bus configuration. The commercialization of these relays has encouraged innovative designs to provide security, speed, and sensitivity. The fast fault clearance time has also ensured greater generator stability [6]. However, selectivity is still a significant issue. The last two decades have seen remarkable success in microprocessor-based relaying scheme. The combination of microprocessor, microcontroller, digital signal processors, and Artificial Intelligence (AI) techniques have revolutionized the protection trends.

In the case of Substation Automation Systems (SAS), the digital relays facilitate easy and fast fault analysis and monitoring. It is impossible to implement process bus-based substation protection without SV based digital relays. The modern-day relays come with self-checking functions that detect any fault in the relay circuitry or connecting wires. Hence, this function can be monitored to ensure the readiness

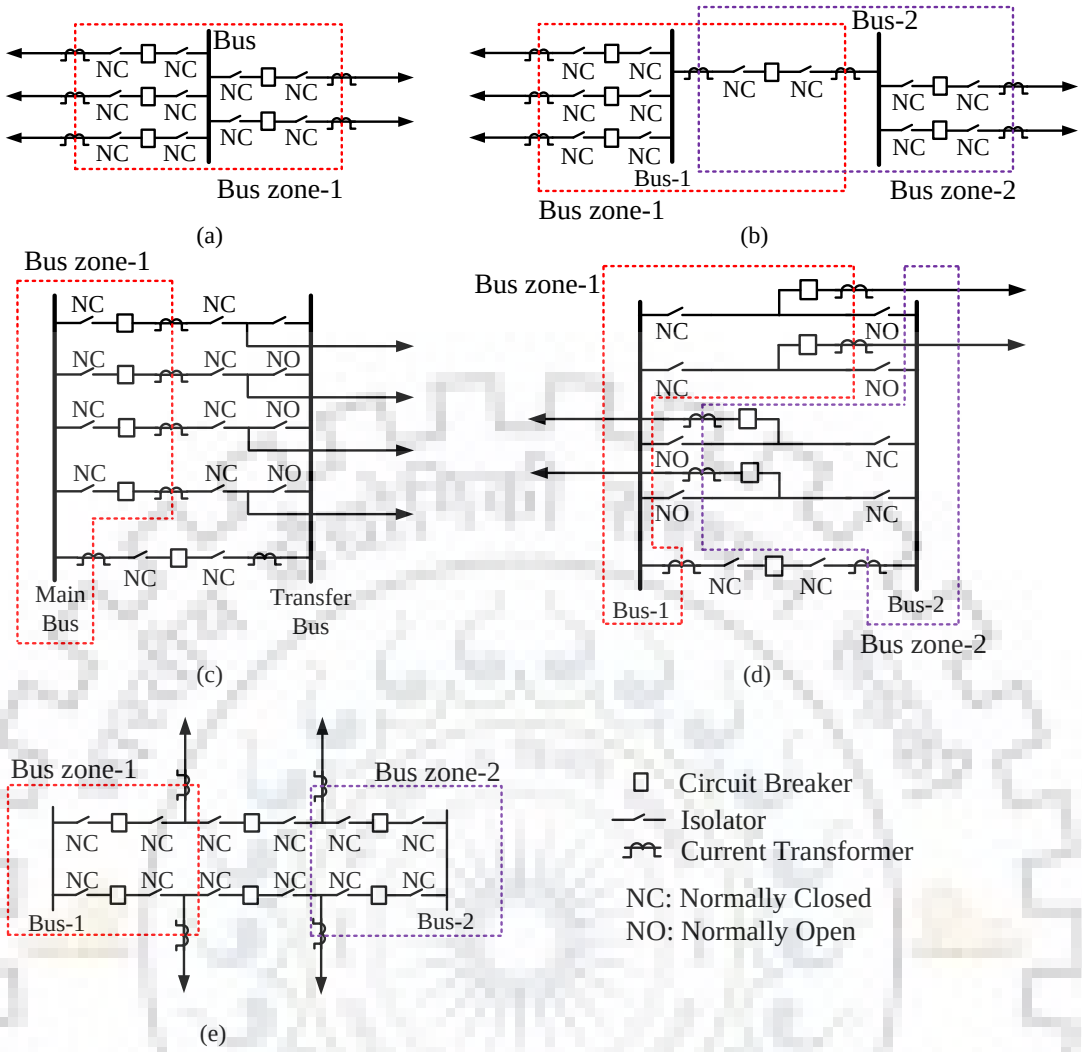

Fig. 1.3: Illustration of different busbar configurations: (a) single breaker single bus (b) single breaker with tie bus (c) main and transfer bus (d) double bus (e) breaker-and-half bus.

of the relay at all times. Modern-day substation protection schemes utilize Merging Units (MUs) to acquire and process currents, voltages, CB, and isolator status of the lines connected to the busbar. With proper networking infrastructure and meticulous planning, ultra-high-speed busbar protection is feasible in the present scenario.

1.2 Typical Busbar arrangements

Busbar arrangement in a substation is primarily decided based on the economics and flexibility in system operation. Different types of busbar arrangements are discussed in this section. Busbar arrangement mainly depends on the switching arrangements. Each of these different configurations has its advantages and disadvantages. High

voltage substations may implement a different busbar arrangement depending upon the ease of operation. However, distribution and industrial substations implement a less complicated busbar arrangement.

1.2.1 Single Breaker-Single Bus

It is the most basic and simple busbar arrangement widely used across distribution and low voltage transmission substations. As shown in Fig. 1.3 (a), only one protective zone encloses the whole substation. This configuration does not provide any operational flexibility. In case of a fault on the busbar, all connected lines need to be tripped. Maintenance of any bus equipment leads to unnecessary outages.

1.2.2 Single buses with tie bus

This arrangement provides flexibility when the substation is fed from two different sources. A tie-breaker is either open or closed depending upon the operational conditions. As seen in Fig. 1.3 (b), two different protection zones are identified and each zone requires individual protection unit. However, in the case of a busbar fault, the affected zone can not be supplied from the healthy zone. A fault in the overlapping section requires tripping of both the zones.

1.2.3 Main and transfer bus

In this arrangement, as shown in Fig. 1.3 (c), a transfer bus is provided in addition to the main bus to improve operational flexibility. However, it requires only one protection zone. In normal operating conditions, only the main bus is energized. In the case of maintenance of any circuit, the line can be transferred to the transfer bus by closing the tie-breaker. The closing of the tie-breaker results in the formation of a different bus zone. Hence, the relay settings should be adaptive to the change in bus zone.

1.2.4 Double bus

A double busbar arrangement, as shown in Fig. 1.3 (d), has more flexibility than the previously discussed arrangements. Both of the buses remain energized all of the time and work independently to each other. A bus tie breaker connects two different bus

zones. Fault on any of the buses requires tripping of the lines connected to it. However, a line can be alternatively connected to the other bus after momentary interruptions, and the tie-breaker is closed for the transfer of the load. Hence, this arrangement improves the supply reliability. However, the relay settings become complicated in the case of a large substation.

1.2.5 Breaker-and-half bus

This arrangement, as shown in Fig. 1.3 (e), is most widely used in case of high voltage substations. Three breakers are used for every two lines; hence, the term one-and-half breaker is used. As shown in Fig. 1.3 (e), two separate protection zones are formed. In the normal case, the lines are supplied from both of the buses. However, in case of a fault on any of the buses, corresponding CB and isolators are closed. Then, the supply is resumed from the healthy bus. Hence, this arrangement provides better operational flexibility and superior protection.

1.2.6 Impact of bus configuration

Different bus arrangements require complicated bus zone arrangements. The bus zone should be identified, and CTs should be available at the end of the protection zone. Breakers should also be present in the end zone. In the case of sectionalized buses, the overlapping region should be minimum to avoid unnecessary tripping of the healthy bus. However, some overlapping region is required to cover all of the protective zone.

1.3 State-of-the-art in busbar protection

Kirchoff's current law is the fundamental principle behind all complex busbar protection schemes. CTs are installed at the equipment and lines connected to the busbar to monitor the current flow. As busbar is a stationary device and length of the busbar is very small in comparison to the transmission lines, differential protection is widely adopted. In the case of normal operating conditions, the vector sum of currents entering the bus zone should be equal to that of leaving the bus zone, and deviations indicate the possibility of an internal busbar fault. Then, the differential protection unit trips all the connected equipment.

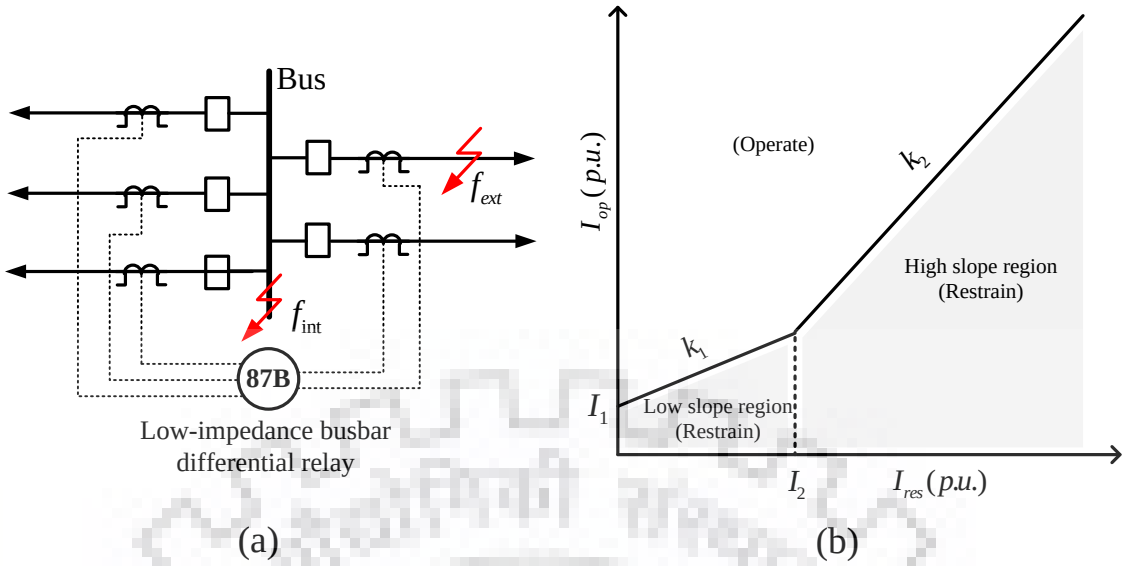

Fig. 1.4: (a) Low-impedance current differential scheme, (b) Relay Characters tics.

Bus zone differential protection is unlikely to be same as transformer differential protection. A transformer differential protection should compensate for the magnitude and phase angle difference between the primary and secondary side. Conversely, busbar protection is believed to be more straightforward as no phase compensation is required. However, the difficulty arises because of the reason that all the CTs in busbar differential protection needs to be in parallel, hence, should have the same ratio to ensure secondary currents in the same base. This situation is further complicated because of the saturation phenomenon in iron core CTs. Ideally, in the case of normal and external fault conditions, there should be no current in the operating winding of the differential relay (87) for all scenarios including heavy through fault and asymmetrical DC offset waveforms resulting because of high X/R sources.

Iron core CTs regardless of their accuracy class, are prone to core saturation. During CT saturation, the CT may not be able to differentiate between the actual differential current in case of an internal fault and false differential current in case of a heavy external fault. The simple overcurrent differential protection can provide stability in case of CT saturation by delaying the operation. However, delayed operations should be avoided. Two of the most commonly used differential protection schemes come in the form of low-impedance and high-impedance current differential schemes.

1.3.1 Low-impedance current differential scheme (87B)

Low-impedance bus differential protection offers low impedance to the flow of CT secondary current. Hence, a very high current flows in the CT secondary and thus leading to saturation of the core. Fig. 1.4 (a) shows the single-phase diagram of 87B showing an external fault (f_{ext}) and an internal fault (f_{int}). This protection scheme requires each CT to have the same ratio, which requires tap settings. It increases the CT burden and makes the saturation problem more significant.

As shown in Fig. 1.4 (b), the relay operates when the operating current (I_{op}) exceeds by a certain percentage of restraining current (I_{res}). This characteristic is inspired by the idea of having a higher restraint for larger magnitude of external faults with CT saturation. The relay characteristics for lower (k_1) and higher slope (k_2) regions are defined by equations. (1.1) and (1.2), respectively.

$$I_{op} \geq k_1 I_{res} + I_1 \tag{1.1}$$

$$I_{op} \geq k_2 I_{res} - (k_2 - k_1) I_2 + I_1 \tag{1.2}$$

Under normal operating conditions or the event of an external fault, the operating current is close to zero as the vector sum of outgoing currents is equal to that of the incoming currents. However, a small finite restraining current always exist. In the case of an internal fault, all the line currents flow into the bus; hence, they have the same phase. The vector sum of the currents, in this case, increases drastically and the operating point moves into the tripping region.

1.3.1.1 Tripping Logic

Fig. 1.5 shows the tripping scheme for 87B with 1-out-of-1 and 2-out-of-2 logic. The start-up element detects the rate of change of restraining current with respect to time (dI_{res}/dt), whereas the differential element monitors equations (1.1) and (1.2). Following a positive output from the start-up element, the output of the differential element is checked every 1/4 cycle. A count is initiated to monitor the number of times the output of the differential element is positive in every 1/4 cycle. If the outputs of both start-up and differential element remain positive for a quarter cycle, a trip signal is

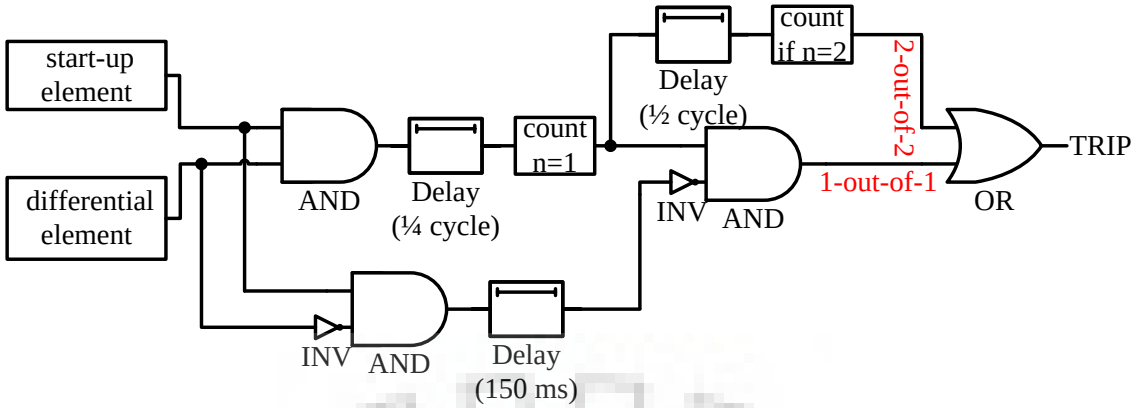

Fig. 1.5: Tripping logic in 87B

issued by the 1-out-of-1 logic element. Conversely, if the output of the differential element is negative following an increase in restraining current, the 1-out-of-1 logic element is blocked for a preset period (usually set to 150 ms). The aforementioned situation occurs when one of the CTs connected to the busbar saturates. An external fault is identified in this case, and the 2-out-of-2 logic element can only generate the trip signal. The 2-out-of-2 logic element checks if the output of the differential element is positive for two consecutive 1/4 cycles (or 1/2 cycle). In case the count value is 2, the 2-out-of-2 logic issues a trip signal. Thus, evolving external-to-internal faults can be identified.

1.3.1.2 CT Performance

As per ideal requirements, it is desired that the CT should faithfully transform the primary current in case of normal as well as heavy fault currents. In reality, CT saturation is an unavoidable phenomenon. Therefore, the 87B protection should avoid substantial CT saturation, as otherwise, it leads to unwanted tripping.

As shown in Fig. 1.6, saturated CT waveforms represent a non-sinusoidal waveform with reduced peak magnitude. The energy of the waveform is reduced with an advanced phase angle (zero-crossing is advanced in comparison to the non-saturated waveform).

According to IEEE standards [7], the accuracy of the CT is determined based on its ability to produce secondary output current within 10 percent of the primary current, reflected to the CT secondary base at 20 times rated CT secondary current. A CT with 5 A rated secondary current can faithfully produce CT secondary currents up to 100A. Assuming a burden of 2-ohm, a C200 class CT can produce a secondary emf

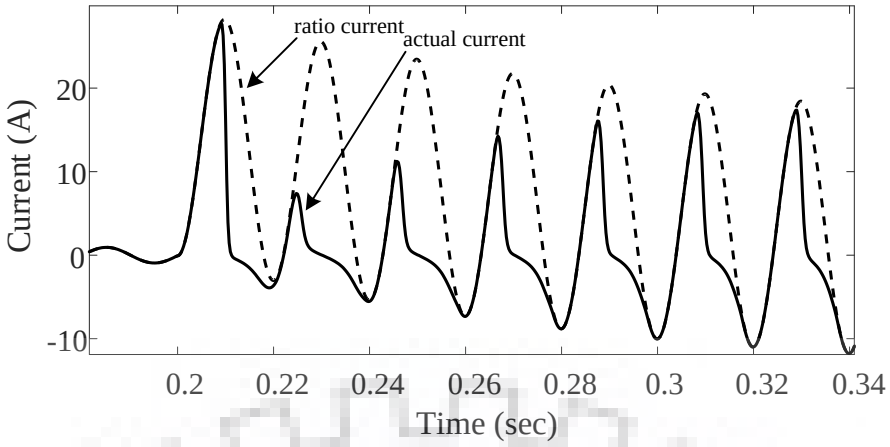

Fig. 1.6: Saturated CT waveforms

of 200V (5A $\times 20$ $\times 2$ Ω = 200V) without going into saturation. The voltage required to produce 10 percent of the primary current is called the saturation voltage.

Iron core CTs possess unwanted saturation property. Due to economic constraints, some utilities employ low-accuracy and low-ratio CTs. Load side generators and power transformers have very high X/R ratio because of their predominantly inductive nature and introduce a DC offset to the asymmetrical saturated current waveform. Modern-day microprocessor-based CTs implement sophisticated techniques to overcome CT saturation effect. 87B uses the first few milliseconds of the rising current in each half-cycle before the saturation effect sets in. The differential current remains low for the period of linear operation of the CT. Once the CT saturates, the differential current starts to increase. However, during an internal fault, both of the restraining and operating currents start to increase simultaneously from the instant of fault inception. Hence, a saturation signal is required to be generated in a few milliseconds of the first half cycle.

1.3.2 High-impedance current differential scheme (87Z)

The problem of CT saturation still exists in a low-impedance differential scheme for close-in external faults. To overcome the effect, particularly, in EHV substations, high voltage differential protection is implemented. The relay differentiates between internal and external faults based on the voltage magnitude across a differential element (87Z). The connection of the relay is shown in Fig. 1.7.

The CTs are connected in parallel across a voltage differential relay (87Z). Under

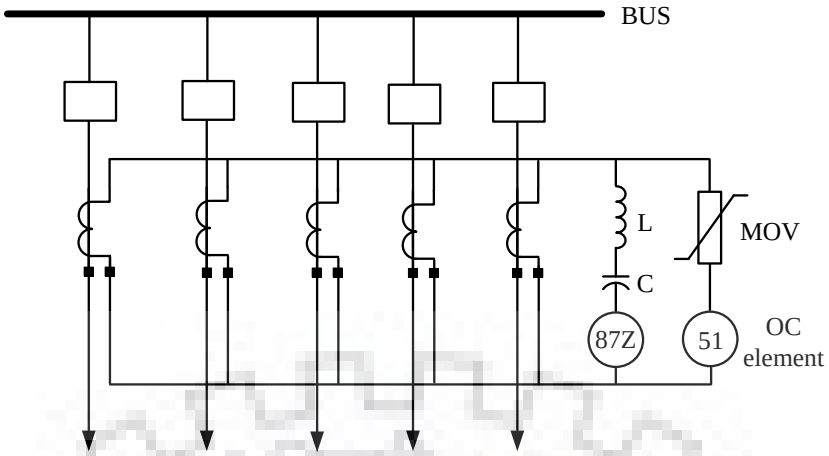

Fig. 1.7: High-impedance current differential scheme

normal and through fault conditions, the CT secondary currents add up to zero, and there is no circulating current in the differential element (87Z). However, in the case of a busbar fault, the CT secondary currents are in the same phase and a very high circulating current flows through the differential element. An L-C circuit tuned to the fundamental frequency (50Hz) is connected in series with the voltage differential unit. The tuned circuit protects the relay from mal-operation from DC offset and harmonic currents. The voltage differential relay (87Z) creates a high impedance path for the circulating current. A Metal Oxide Varistor (MOV) is connected across the high voltage circuit to prevent the circuit from dangerously high voltages. An overcurrent relay is connected in series with the MOV to provide backup protection in case of relay failure. The circuit bypasses high magnitude currents, hence, provides faster tripping.

1.3.2.1 CT Performance

Assuming ideal CT characteristics, under normal operating conditions, the CT secondary currents circulate among the parallel combination of the CTs. A two-CT equivalent circuit is shown in Fig. 1.8 (a). The current source CT-A is the summation of all CT outputs except CT-B. As all of the CTs are in parallel, then the series impedance and exciting reactance are divided by $n-1$, where n is the total number of CTs. Assuming all CTs having the same magnetization characteristics, under normal operating conditions, the current from CT-A would be equal to that of CT-B. Hence, no current flows through the high impedance path consisting of 87Z and a stabilizing

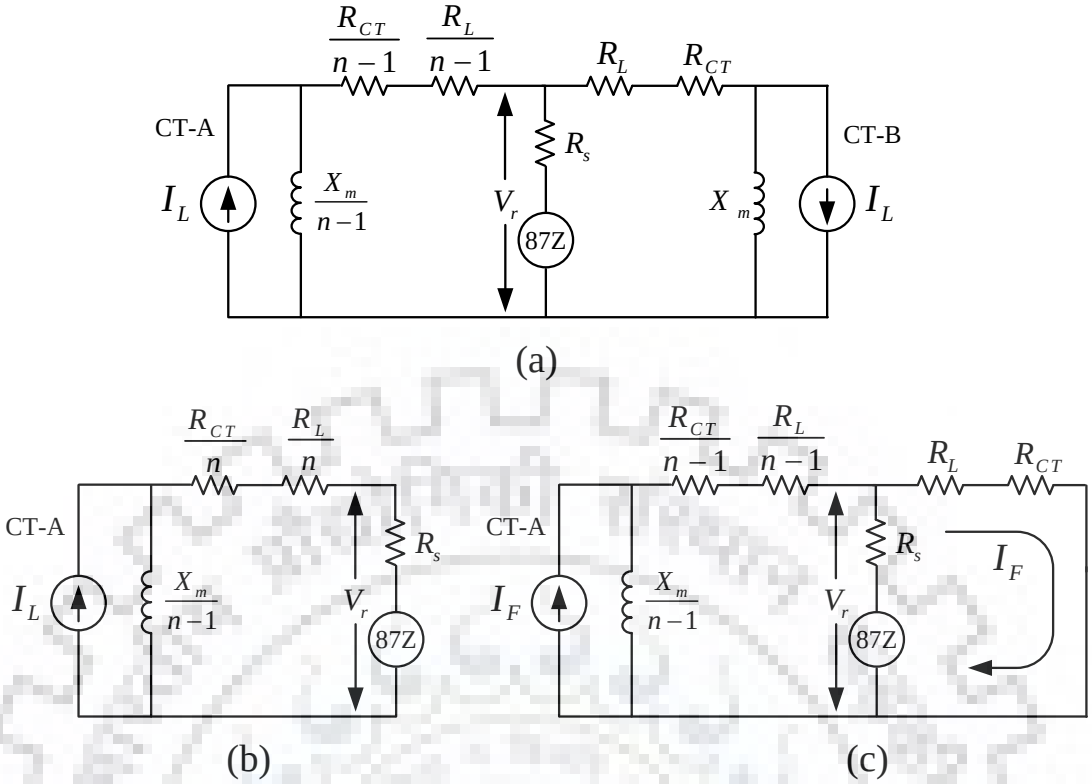

Fig. 1.8: Two-CT equivalent diagrams in (a) normal operating condition, (b) internal fault, (c) CT saturation scenario.

resistance (R_s). Due to this, the voltage difference between the differential unit (87Z) is close to zero, and no tripping signal is sent.

In the case of an internal fault, all the CT secondary currents have the same phase. Hence, the CT secondary currents can be added as an equivalent single current source (Fig.1.8 (b)). The equivalent current sum flows through the high impedance differential relay producing a very high voltage. If this voltage exceeds the pick-up voltage, the relay issues a trip signal. The MOV clamps the high voltage spikes to prevent any damage to the relay.

In the case of an external fault, CT corresponding to the faulted line is most likely to saturate. The high impedance differential scheme must be set above the voltage generated across the differential terminals for the most severe fault. In the case of a highly saturated core, all the primary current flows through the excitation branch. Hence, a completely saturated CT produces zero current. As shown in Fig. 1.8 (c), the saturated CT can be represented only by the internal resistance. The CT lead resistance (R_L) and CT internal resistance (R_{CT}) are small when compared to the internal resistance of the high-impedance path. Hence, the voltage across the relay

Table 1.1: Comparative analysis between low and high-impedance differential protection

Properties	High-Impedance (87Z)	Low-Impedance (87B)
Sharing of CTs	No	Yes
Different CT ratios	No	Yes
Dynamic zone reconfiguration	No	Yes
Speed	$>$ 1.5 cycles	$<$ 1 cycle
Sensitivity	Moderate	High
Security	Moderate	High
Breaker Failure Protection	No	Yes
Complexity	Low	Moderate
Cost	Low	Moderate

(V_r) in external LLL faults is considered as the pick-up setting of the relay.

1.3.3 Comparative analysis

Table. 1.1 provides a comparative analysis between the low and high-impedance busbar differential relays [8]. The security aspects have been defined in terms of the ability of the relays to restrain itself from operating in case of external faults specifically in case of CT saturation conditions. Whereas, sensitivity has been defined in terms of its ability to sense busbar faults regardless of the magnitude of fault current. The speed of protection may be defined in time requirements to generate the trip signal in case of busbar faults. The end-users or utilities need to evaluate each of these relays based on the intended application and installation costs. The 87B offers the flexibility of sharing the line end CTs, different CT ratios, offer dynamic zone reconfiguration, whereas, 87Z provides less complexity and lower installation costs. However, in terms of speed, sensitivity in detecting internal faults, and security against CT saturation scenarios, 87B provides better performance in comparison to 87Z. Hence, 87B has been widely adopted across power utilities.

1.4 Breaker-Failure Protection

Busbar protection schemes use connection status of breaker and isolators to allocate bus zones to each transmission line and substation elements. The same information is used in case of breaker failure situations. It encourages integration of a breaker-

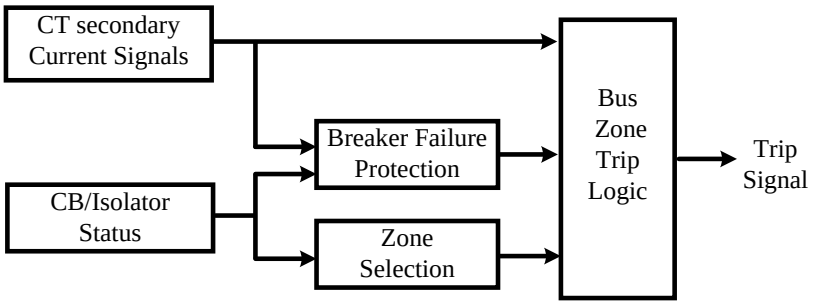

Fig. 1.9: Integration of breaker-failure function in busbar protection

failure function inside the busbar relay. In this regard, Fig. 1.9 shows the schematic diagram for the integration of breaker failure function inside the busbar relay. This implementation would eliminate duplication of the common functionality, minimize the wiring, and simplify the protection design [9].

A breaker failure may be defined as a failure of the breaker to open contacts to interrupt fault current after receiving a trip signal. Hence, a breaker-failure signal is issued when two conditions are satisfied [10]:

- Trip signal from the relay (BFI) is available.
- The current is still flowing through the CB (50BF)

An overcurrent element (50BF) is set at a fraction of rated CT secondary current to detect current flowing through a CB. The breaker-failure scheme is started by using the contact of primary relay, which is further supervised by normally open auxiliary contact (52a) of the CB. It is worthwhile to note that auxiliary contacts (52a) of CB are not reliable indicators and also proven to be historically inaccurate. In all types of bus configurations, breaker-failure schemes are applied per breaker. In each scheme, a BFP signal should trip all breakers in its zone to isolate the fault. In several cases, the necessity to trip at least one remote breaker also arises. An efficient breaker-failure scheme should try to re-trip the failed breaker before tripping adjacent breakers as a false tripping leads to massive power outage or possible blackouts [11].

Fig. 1.10 shows the basic structure of the breaker failure protection scheme. After the detection of fault by the primary relay, the BFI element asserts, and after some delay, the 50BF element activates. When the output of AND logic goes high, a timer (62) starts. The time delay is set in terms of the critical fault clearance time with addition to a safe margin time. If the primary relay trip input (BFI) and 50BF element

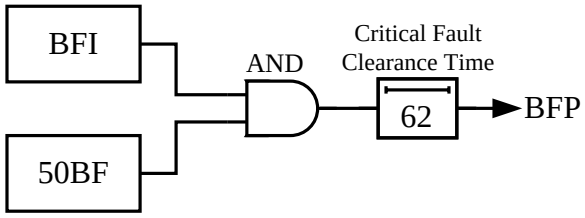

Fig. 1.10: Basic breaker-failure scheme.

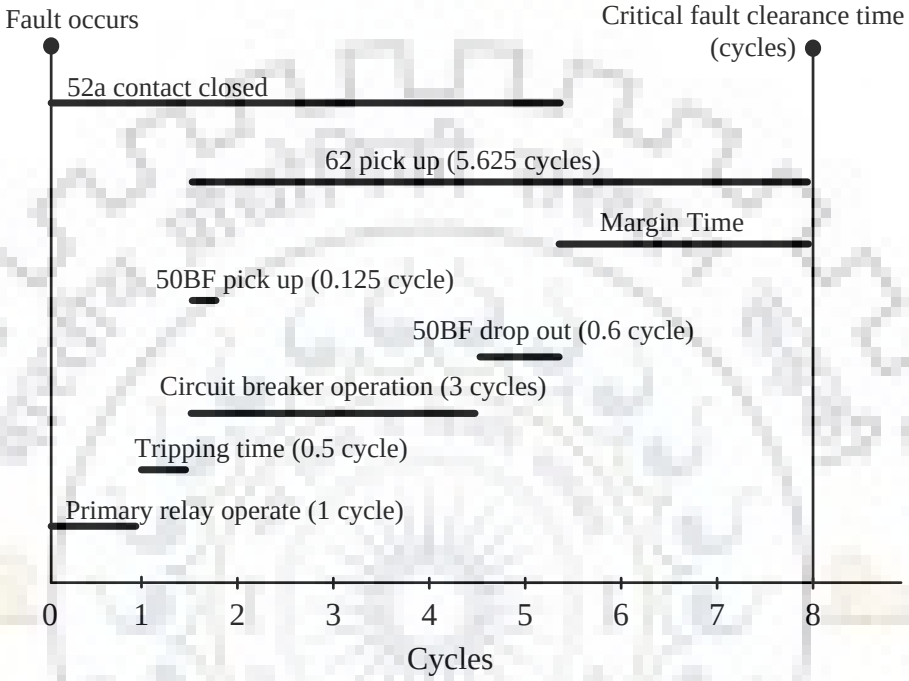

Fig. 1.11: Timeline of occurrence of fault and breaker failure settings.

remains asserted till 62 expires, the scheme declares a breaker failure situation and subsequently trips the adjacent breakers. The (BFP) signal resets if one of the signals (either BFI or 50BF) drops.

Fig. 1.11 shows the timeline of breaker failure settings. After the inception of fault, the primary relay, depending on the Root Mean Square (RMS) magnitude of the current takes about one cycle for the trip decision. An additional half-cycle delay incurs due to the auxiliary relay tripping circuits and communication process. Hence, the BFI element activates after 1.5 cycles of fault inception. Upon receiving the trip signal, the CB typically clears the fault within 3 cycles. In the meantime, the BF threshold (50BF) picks up after a short delay (0.125 cycle). The RMS magnitude of current decreases after the opening of auxiliary contacts of CB (52a). The expected time limit for it to drop out below the preset 50BF threshold is 0.6 cycles. If this delay crosses a predefined margin ($\approx$ 2 cycles), the BFP issues a trip signal and subsequently

adjacent breakers are tripped. In similar terms, if both BFI and 50BF function remain energized for a preset time delay ($\approx$ 5.625 cycles), the BFP function is activated. Hence, out of the critical fault clearance time of 8 cycles, 5.625 cycles are available for the timer setting (62) of BFP. The reset signal needs to be asserted within the critical fault clearance time to prevent mal-operation of BFP function, if any.

1.5 Literature Review

Last few decades have witnessed remarkable accomplishments in the field of numeric relaying in busbar protection schemes. The implementation of microprocessors, microcontrollers, signal processing, networking devices along with cutting-edge mathematical analysis of different techniques has paved the way for the development of futuristic protection schemes. Comprehensive literature analysis of such schemes is discussed in the following subsections.

1.5.1 Microprocessor-based protection

Owing to the advancement in high-speed microprocessor technology in the past few decades, its applications in busbar protection are widely-spread. Keneddy *et al.* [12] in 1938 were first to propose a microprocessor-based busbar differential relay utilizing harmonic current restrain principle. However, if the harmonic current exceeds certain limiting value, the relay fails to operate. Later, Andow *et al.* [13] proposed a busbar protection scheme which remains stable during CT saturation. However, the proposed scheme remains blind to CT saturation scenarios for a pre-defined period after fault inception, which is indeed crucial for the prevention of mal-operation.

Royle *et al.* [14] proposed a solid-state busbar protection scheme which detects the saturated CTs by using electronic circuits. However, in case of higher degrees of saturation, the electronics circuit bypasses the operating coil by overriding the CT saturation pick-up element. Peck *et al.* [15] proposed a busbar protection scheme that can adjust the operating and restraining characteristics in the case of CT saturation for heavy through faults. The delayed operations in case of internal bus faults is the major drawback in the proposed scheme. After that, Kang *et al.* [16] proposed a modified scheme which can generate initial trip decision within the first few milliseconds in

case of internal faults. However, the proposed scheme rules out the possibility of CT saturation in the first few milliseconds of fault inception. This assumption may turn the relay futile in case of early CT saturation. Afterwards, Kasztenny *et al.* [17] presented a combined busbar protection scheme based on differential and directional principles. To the brighter side, it enhances security of the busbar relay; however, it delays trip signals in case of critical internal bus fault scenarios.

At last, Gill *et al.* [18] proposed a microprocessor-based protection scheme based on the positive and negative sequence components. However, the proposed scheme requires both current and voltage data with a large number of input signals. Discrepancy in one of the input signals would result in total failure of the scheme.

1.5.2 Directional protection

These schemes work on the basic principle of power flow direction. During an external fault, power flow directions in all the circuits are towards the faulted line, whereas, in case of a bus fault, the power flow directions are towards the busbar. This differentiating criteria has been previously implemented in terms of current, superimposed current or impedance parameters. Directional protection schemes presented in [19–23] are based on superimposed impedance, hence, require both acquisition and synchronization of current and voltage data as per IEC-61850 protocol [24] which increases financial burden and decreases reliability. Moreover, synchronization of current and voltage data is a major challenge as high-speed sampling is not feasible with Coupling Capacitor Voltage Transformers (CCVTs). Furthermore, the reliability of these schemes is marginalized if the number of lines connected to the busbar is very high. In another major setback, these schemes are unable to detect high impedance faults (HIFs) as the current components remain very small [25].

1.5.3 Differential Protection

87B are primarily used for fast tripping, whereas 87Z is installed for their low installation cost [26]. Primarily, because of the adaptability in case of dynamic configurations and flexibility in using line-end CTs with different CT ratios, 87B is more suitable. In this regard, Kasztenny *et al.* [27] proposed a differential protection scheme with a customized adaptive CT saturation algorithm. However, a large number of input

and output nodes with complex processing requirements decrease the reliability of the scheme. Kumar *et al.* [28] proposed a differential protection scheme with improved operating and differential characteristics. However, due to the filtering process, the proposed scheme initiates delayed trip signals in case of internal bus faults. Several phase-segregated busbar differential relays [29, 30] have been presented in the past. The phase segregation results in low cost and simplicity. However, it increases the computational and communication burden.

Overcoming CT saturation problems remain the primary focus while designing a differential relay [31–33]. Over the years, researchers have proposed numerous techniques to improve the performance of busbar differential protection in case of CT saturation. Several algorithms have been proposed in the literature for CT saturation detection. These techniques can be broadly classified into two groups depending on the input current, 1) CT secondary current 2) differential current. Algorithms used in the group (1) detect CT saturation based on the unusual CT secondary waveforms that differ from the CT secondary waveforms during normal operating conditions. The algorithms used in the group (2) detect CT saturation by the fact that, during the inception of a fault, a low magnitude differential current is followed by a higher differential current because of the saturation of one of the CTs.

One of the earlier reported methods [34] depends on the calculation of core flux in the case of saturated CTs and compensate it using compensating currents. Some of the methods assume the fact that if CT secondary waveform is perfectly sinusoidal, then the mean should be zero. The summation of instantaneous current samples and the second-order derivatives over a cycle are zero for a perfectly sinusoidal curve, which is not valid for a saturated CT secondary waveform. A CT saturation detection algorithm based on impedance measurement instead of CT secondary current measurement was proposed in [35]. The impedance seen by the relay is calculated as the ratio between incremental voltage and current at the relay location. If the CT enters into the high saturation region, the magnetizing behavior of the CT can be approximated by a straight line parallel to the H axis in the B-H plane. In these conditions, the incremental CT secondary current reduces to zero. Hence, the impedance seen by the algorithm tends towards infinity.

To overcome the CT saturation problems in busbar differential protection, Eissa

[36] proposed a scheme based on phase comparison. It produces improved results than previous magnitude comparison schemes, but delays relay operation. Guzman *et al.* [37] proposed a busbar protection scheme with advanced zone selection having better stability against heavy CT saturation. In addition to the differential settings, the proposed scheme requires a directional element which reduces the overall reliability. Furthermore, the filtering process also adds a significant delay to the trip decision. Kang *et al.* [38–40] proposed algorithms by compensating current to distorted CT secondary currents. However, this method is not suitable for severe CT saturation cases. The proposed busbar differential protection scheme in [16] detects the start of saturation period based on the third difference of CT secondary current signal. The proposed scheme provides better stability in wide range of CT saturation scenarios. However, an evolving external to internal fault during the saturation period remains unnoticed in the proposed scheme.

1.5.4 Travelling Wave-based protection

TW-based schemes provide ultra-high-speed protection with less than 1 ms operating time. The relative time of arrival (ToA) of wavefronts at relay locations are used to construct the relaying algorithm. As TWs are detected before the starting of CT saturation, these schemes remain inherently immune from CT saturation conditions.

In this regard, Wang *et al.* [41] have used the initial current transient waves to detect in-zone or out-of-zone faults. Similarly, Lin *et al.* [42] proposed a protection scheme for transmission line and busbars based on the polarity of current TWs. Both of these schemes fail in case of close-in faults where the incident and reflected TWs appear at the relay location concurrently. Song *et al.* [43] proposed a reliable solution to busbar protection by utilising the polarities of superimposed current at the relay location of all the lines connected to the busbar. As the magnitude of fault current is minimal in case of high-impedance faults, it is difficult to identify the fault based on superimposed current. The TW-based scheme presented by Zou *et al.* [44] provides real-time high-speed protection. As the fault is identified before the starting of CT saturation, the mal-operation in these cases can be avoided. However, faults with small inception angle do not produce TWs of sufficient magnitude to be detected by the relay.

1.5.5 Wavelet Transform-based protection schemes

The feasibility of both time and frequency localization in WT makes it attractive towards fault analysis. The wavelet coefficients obtained from post-fault voltage or current samples contain a great deal of information about the fault [45].

In this regard, Eissa [36] proposed a busbar differential protection based on continuous wavelet transform (CWT). While CWT offers good time-frequency localisation, the computational requirements are very high. Busbar protection, in particular, requires high-speed protection and signal transmission. Hence, the use of CWT for high-speed protection applications would be unsuitable. Thereafter, Mohammed [46] proposed a busbar differential protection scheme based on wavelet packet transform (WPT). It offers better time and frequency resolution than CWT. However, the computational burden in case of WPT is doubled as it requires down-sampling and decomposition of both approximate and detailed coefficients. Valsan and Swarup [47] have utilized power coefficients to differentiate between internal and external bus zone faults. The proposed scheme offers better performance in case of HIFs. However, it requires synchronized 3-phase current and voltage signals. Hence, the data requirement and computations are high. Gafoor and Rao in [48] proposed transient based scheme based on bi-orthogonal wavelet. The number of wavelet coefficients in this scheme is very high, which results in increased computational requirements. Recently, Silva *et al.* [49] proposed a busbar differential protection scheme based on energy coefficients. The differential and restraining energy coefficients are mapped to conventional differential protection principles. The proposed scheme offers better performance in case of CT saturation and evolving external-to-internal faults. However, the number of filter coefficients are more, and it requires phase-segregated relays with inter relay communication functionality.

Similarly, Vásquez and Silva [50] proposed a differential protection scheme based on instantaneous power coefficients. The proposed scheme is faster than the conventional 87B in case of noisy and evolving external-to-internal faults. However, it requires both instantaneous current and voltage components. Further, the prepossessing of current samples such as the normalization and filtering adds significant delay to relay operation.

1.5.6 Statistical learning theory-based protection

Previously, researchers have proposed AI and machine learning-based approaches to identify the fault zone for busbar protection. Primarily, these schemes develop a statistical model and train it with a database representing a wide variation of fault and other system abnormalities.

In this context, several researchers [51–54] have proposed busbar protection schemes based on artificial neural network (ANN). In these schemes, a network consisting of layers of neurons are trained, and the associated weights to the connections are optimized based on a learning mechanism. Despite their higher accuracy, a large number of neurons with a tedious training process does not appeal relay engineers for practical implementation.

Support Vector Machine (SVM) and relevance vector machine (RVM) based bus zone identification schemes have been proposed in [55–59]. The schemes above produce high accuracy when tested on a large number of fault scenarios with wide variations in parameters. However, it would be difficult to achieve probabilistic predictions because of the unexpected behavior of the kernel or cost functions. To overcome these limitations, Narayan and Bhalja [60] proposed a busbar protection scheme based on random forest algorithm. Despite its high accuracy, it introduces enormous complexities for on-chip implementation. As an alternative solution, Allah [61, 62] has proposed busbar protection schemes based on alienation coefficient. These schemes offer better stability against CT saturation. However, re-configurable dynamic busbar arrangements present greater challenges.

1.5.7 Breaker Failure Protection Schemes

As a part of the local backup strategy, BFP is called upon when the CB fails to clear a fault. In this situation, the BFP isolates the fault by opening adjacent CBs. The same can be achieved by opening the remote-end CBs as a part of the backup strategy. However, it results in forced curtailment of some of the loads and adds significant delay to fault clearance time because of the involvement of direct transfer trip command through communication channel [63]. Hence, as a local solution, integration of BFP function inside commercial protection relays has gained momentum in the recent past [64, 65].

Subsidence current in CT secondary presents the main challenge to the BFP function. Momentary interruption of current by the breaker following an offset decaying fault current results in subsidence current in the CT secondary which energizes the overcurrent element. Subsequently, the BFP function mal-operates. It is a peculiar situation as BFP trips the adjacent breakers when the breaker itself has cleared the fault. The tripping of the BFP function leads to unnecessary power outage or possible blackout of the system. To this end, a reset algorithm by analyzing the CT secondary current passed through a pair of orthogonal sine and cosine filters is proposed in [66]. Subsequently, a BFP reset scheme by identifying the crossing points of CT secondary current, and its derivative signals is proposed in [67]. Though these schemes provide reliable reset signals to prevent the mal-operation of BFP function, they may not provide reliable results particularly when the fault current consists of a higher degrees of DC decaying component followed by longer subsidence current.

1.6 Research Opportunities

The broader challenging aspects, as discussed in the previous section, attract researchers to develop sophisticated busbar protection schemes. With higher voltage levels at EHV/UHV substations, the speed of protection has become more critical. Furthermore, dynamic system configurations and load transfers add challenges to reliable busbar protection. Hence, there exists a vast void to be filled up in achieving an all-round universal busbar protection. To develop innovative busbar protection solutions, the following research areas have been outlined in this work:

1.6.1 Instantaneous current sample-based busbar protection

Majority of the published work in busbar protection depend on the calculation of phasor quantities. However, the accurate estimation of current phasors in presence high decaying DC components is troublesome. In this regard, as an alternative solution, statistical learning theory-based schemes can be utilized. However, as discussed in the previous section, AI and machine learning-based schemes offer enormous complexities, which hinders their on-field application. A clear and more straightforward approach to busbar protection based on statistical learning would be instrumental for possible on-

chip implementation. With the implementation of high-frequency data accusation units and faster signal processing devices, these schemes could see light of the day in recent future. Large scale data analysis based research in other power system applications is well established, whereas, its slowly keeping pace in power system relaying applications.

1.6.2 Improved numerical busbar differential protection

Busbar differential protection schemes in both low and high-impedance versions come with their challenges. While 87B is exposed to mal-operations owing to CT saturation, high-impedance protection schemes are prone to CT ratio errors. In the last two decades, improvement in the differential characteristics has remained as the most challenging aspect in busbar protection. Researchers have proposed differential adaptive characteristics over the years. Furthermore, researchers have investigated the effect of differential and restraining components derived in terms of positive/negative sequence, power, energy, and wavelet components. The results in these cases have indicated improved relay characteristics in terms of both reliability and stability. Nevertheless, high computational requirements throw significant challenges for the implementation of these schemes. State-of-art signal processing algorithms and excellent mathematical tools have created enough room for the development of improved numeric busbar protection schemes.

1.6.3 Ultra-high-speed busbar protection

To limit the widespread damage, high-speed tripping during bus faults is one of the essential requirements of busbar protection. The present practice to speed up fault clearance is concentrated upon reduction of tripping time rather than developing new arc extinction methods for CBs [68–70]. Primarily, majority of the bus protection schemes that work on power frequency components require phasor computation of voltage and current signals, which adds significant delay to the relay operation. Also, filtering processes further delay relay operation. On the contrary, transient component-based schemes such as TW and WT provide instantaneous protection with tripping speed less than 1 ms. These schemes are used in supplement to the primary protection scheme as they mal-operate in case of over-damped oscillations.

Further, high sampling requirements limit their more extensive applications. In

positive advancements, recent developments in the field of high processing electronic components has opened the door for research in transient component-based protective relaying, which was not possible previously. On-field implementation of transient component-based busbar protection schemes to accomplish ultra-high-speed protection require more research and developments.

1.6.4 Busbar protection with dynamic zone selection

To improve the continuity of supply and flexibility of operation, some of the substations use complex busbar arrangements, which demands sophisticated busbar protection schemes for each of the bus zones. In this regard, the zone selection logic assigns bus zones to transmission lines and substation elements. The zone selection is performed based on AND/OR logic on the current status of CB and isolators. Finally, it assigns the line currents to appropriate differential and restraining elements without the need of disabling the busbar protection during load transfers. Majority of the proposed bus protection algorithms are not adaptive to zone changes. In such cases, a fault trips all CBs, which unnecessarily isolates a large part of the substation. These events call for the development of innovative busbar protection algorithms with advanced zone selection logic. In this regard, the introduction of ethernet-based process bus applications and SV protection would facilitate faster dynamic zone selection logics with improved busbar protection. Still, much scope survives for further improvements in busbar protection schemes with advanced dynamic zone selection logic.

1.6.5 Improved breaker failure protection

Keeping the stability and operational consequences of a fault in EHV substations in mind, the narrower margin for fault clearance is always preferred. Some of the utilities mandate further reduction of this margin. Hence, it has become more challenging to accommodate the BFP trip time. Selection of excellent mathematical tools to provide reliable BFP has the utmost priority in this regard.

Subsidence current resulting because of CT saturation and large BF pickup to fault current ratio results in longer time for reset of simple overcurrent BFP functions. Hence, a substantial reduction in BFP reset time is required to prevent mal-operation of connected CBs. The recent developments in the field of numerical relaying, digital

signal processing, and high-class CTs allow implementation of improved BFP modules with substantial performance enhancement.

1.7 Proposed Objectives

In order to overcome the research gaps discussed in the previous sections, the following objectives are outlined in this thesis work:

- To apply cutting edge numerical analysis and statistical learning theories for the development of phasor free (instantaneous current based) high speed busbar protection schemes with least computational and communication requirements.
- To develop improved busbar differential protection schemes in terms of better stability in case of CT saturation scenarios with hardware validation in laboratory environment.
- To present a breaker-failure reset algorithm to prevent mal-operation arising due to subsidence current.

1.8 Thesis Organization

The work presented in this thesis has been divided into the following chapters:

Chapter 1: This chapter presents an introductory section into busbar protection and BFP schemes. A detailed analysis of state-of-art protection in this regard has been carried out. Thereafter, a comprehensive review of published literature has been presented, and the research gaps have been outlined. At last, the proposed research objectives for this work has been defined.

Chapter 2: This chapter presents a fault zone identification scheme for busbar based on the LR binary classifier. Practicability of the proposed scheme has been verified by simulating a large number of fault scenarios on an existing 400-kV power system model. The proposed model, when tested on a large database of diversified fault scenarios, achieves very high accuracy. The versatility of the proposed scheme has also been tested for different busbar configurations. At last, a comparative evaluation with contemporary schemes suggest its superiority.

Chapter 3: An improved digital differential busbar protection scheme based on GAP has been presented in this section. Its performance has been tested on an existing 400-kV substation simulation model. The results indicate better sensitivity for internal busbar faults. The stability against CT saturation conditions is found to be superior to 87B. The response time of the proposed scheme has been on-par with modern transient based busbar protection schemes.

Chapter 4: A high-speed busbar protection scheme based on aerial mode traveling waves has been presented in this chapter. A 750-kV existing substation has been developed to test the performance of the scheme. The initial traveling wavefronts appearing at the substation has been extracted in the form of WTMMs. Fault zone identification and classification has been carried out based upon their polarity and magnitudes. A comparative evaluation with existing transient based schemes in terms of computational and communication requirements shows its superiority.

Chapter 5: This chapter presents a sampled-value based busbar protection scheme based on dq-components. These components have been utilized for the development of improved differential characteristics. Its performance has been validated on double-bus-single-breaker and breaker-and-half configurations. The feasibility of on-field implementation with IEC-61850 substation automation systems has been discussed in details. The results obtained during different internal and external fault scenarios show its effectiveness.

Chapter 6: A reliable BFP scheme with improved safety margins has been presented in this chapter. A new algorithm to effectively discriminate between true fault current and subsidence current in CT secondary has been proposed. It has been tested under wide variation in system and fault parameters. A comparative evaluation with existing schemes has also been presented.

Chapter 7: This chapter highlights the major contribution made by the authors in this thesis. Some suggestions about future research scope in busbar and BFP have been put forward.

In the end, system parameters of the developed simulation models are given in the appendices section.

Chapter 2

Fault Zone Identification using Logistic Regression Classifier

Due to the severity, high responsiveness in case of internal busbar faults is the most critical aspect in designing a busbar protection relay. The major challenge to this comes in the form of the need of phasor computation. In order to break the phasor computation barriers, instantaneous current based schemes can be effectively utilized. In this chapter, a clear and straight-forward approach to busbar protection utilizing logistic regression classifier (87BLR) has been proposed. The scheme has been trained with diversified fault scenarios. It's performance in critical fault conditions has been discussed in the subsequent sections.

2.1 Introduction

Protection of busbar is very critical as clearance of bus fault would need the tripping of all the breakers of the bays (lines) connected to the faulted busbar. Such a tripping can potentially lead to widespread instability of a power system. Owing to the increase in voltage level, complex configuration of busbar arrangements and extensive interconnection, stability of generators becomes an critical condition which requires faster and reliable operation of the relay for a severe bus fault [3]. Therefore, it is essential to develop separate busbar protection scheme which not only prevents hazards to the system but also minimises interruption of power by utilising a sectionalised and duplicated busbar arrangement. At the same time, it also prevents unwanted trip-

ping of all the bays in case of heavy through fault. The high MVA level associated with the bus zone area demands fast and reliable protection scheme for different busbar configurations [4, 5, 19, 68]. This study presents the development of a new fault zone identification scheme for busbar using LR binary classifier by utilizing one cycle post-fault current signals of all the bays connected to the busbar. Practicability of the presented scheme has been verified by modeling an existing 400-kV Indian power generating station in PSCAD/EMTDC software package. The presented scheme has been tested on enormous cases (38,400) which were generated by varying system and fault parameters.

2.2 State-of-the-art

Techniques for busbar protection are classified as non-unit protection and unit protection. The faults cleared by non-unit protection scheme which uses back-up overcurrent, earth fault and distance relays are usually found to be non-discriminative and slow in operation. Sometimes, busbar protection schemes are classified based on the type of relays used, such as directional relay and differential relay. Though the directional comparison scheme provides good classification in case of busbar faults, its reliability can be compromised by too many series contacts and complex circuitry. Moreover, an instantaneous overcurrent relay is required along with the directional relay to identify the existence of fault, which increases cost. A directional comparison-based busbar protection scheme was proposed by Zadeh *et al.* [21] that incorporate IEC-61850 substation protocol and utilises superimposed components of currents. However, higher cost and increased complexity due to the requirement of voltage signals along with current signals are the prime limitations of the above scheme. Afterwards, Zou and Gao [44] proposed a busbar protection scheme based on TWs which distinguish internal faults with external faults. However, the reliability reduces in a case when the transient fault signal is weak.

Afterwards, various wavelet transform-based digital protection schemes have been proposed [46–48]. Nevertheless, high-frequency noise signals during decomposition of current signals may reduce its accuracy. Subsequently, a new digital protection scheme for busbar is presented [22] which depends on comparison of relative phase angle dif-

ference of sequence components of currents. However, assembling sequence networks and their solutions is troublesome. Hence, a scheme based on symmetrical components may not be practicable. Afterwards, Chothani *et al.* [55] and Chothani and Bhalja [59] proposed fault zone identification schemes based on SVM and RVM. However, the prime limitation of the above schemes is that they do not give satisfactory results due to the behaviour of the kernel function which needs to fulfil the Mercers condition, and hence probabilistic predictions may not be feasible. Thereafter, Song and Zou [43] presented a busbar protection scheme by integrating the polarity of superimposed travelling-wave currents with a new phase-mode transformation matrix. Nevertheless, the above scheme fails to identify the fault zone in case of severe CT saturation and high resistance internal faults.

2.2.1 Limitations of the conventional current differential protection scheme

The biased percentage current differential protection scheme having dual slop characteristic has been widely used in practice [71]. The standard practice is to set the percentage bias, as defined by equation 2.1, more than 15% for the lower slope region and more than 50% for the higher slope region.

$$\%Bias = \frac{OC}{RC} \times 100 \tag{2.1}$$

where, OC is the ac vector sum of all bay currents, and RC is the dc scalar sum of all bay currents.

The primary advantage of the biased percentage differential protection scheme is the reduced requirement of dedicated CTs, and its ability to be used for high-speed tripping. However, it may mal-operate in case of close-in external faults due to saturation of CT because of the secondary currents may not sum up to zero due to saturation of the CT in the faulted section. Moreover, the transient component of fault current (decaying dc component) may issue nuisance tripping of the relay. To offset the effect of transient component of fault current, sometimes, stabilizing resistance is used. However, the use of stabilizing resistance reduces the sensitivity of the relay. Fig. 2.1 shows the response of the biased percentage differential scheme in case of a

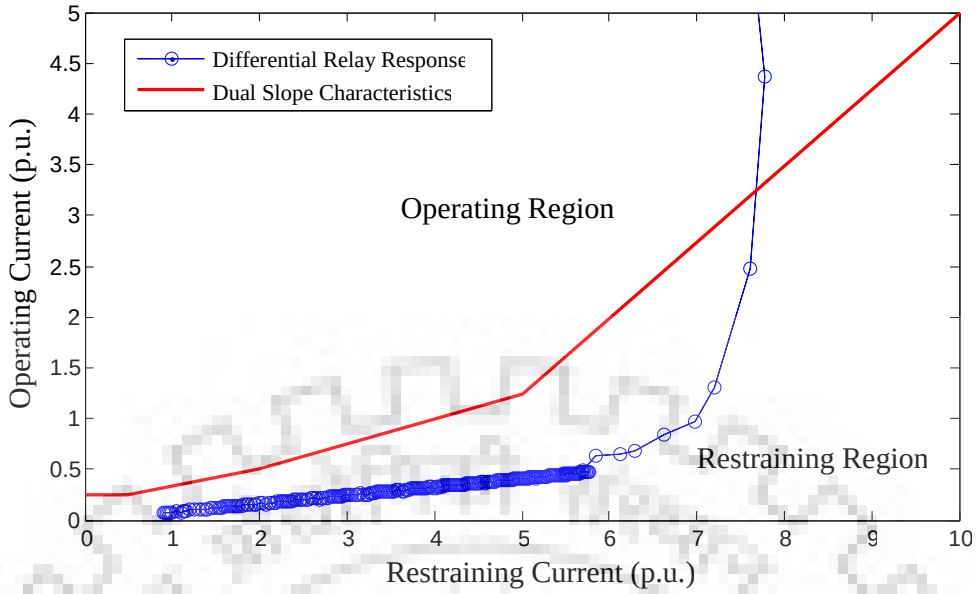

Fig. 2.1: Response of differential protection scheme during CT saturation.

heavy through fault during which CT saturates. Here regarding Fig. 2.1, a through (3-phase) fault is simulated at a distance of 1 km from the bus under consideration on the bay L1. It is to be observed from Fig. 2.1 that the locus of the relay characteristic has moved into the operating region during heavy through fault and hence, nuisance tripping is initiated.

2.2.2 Logistic Regression (LR) Classifier

LR is one of the most efficient algorithms available in Machine learning, which is particularly suitable for classifications tasks that deal with dichotomous (binary) classification. LR classifier is sometimes confused with being a linear classifier. However, it is called a linear classifier because the output of the hypothesis function is in a linear relationship with its prediction. However, the relationship between the attributes and the predictions may be nonlinear. LR classification algorithm tries to predict the probability of one feature vector falling in one category as opposed to the other, depending on the dependent variable (attributes). The predicted class in LR is always evaluated by probabilities determined by the hypothesis function, which always lies between 0 and 1. The hypothesis function is given by:

$$h_\theta(X) = g(\theta^T x) \tag{2.2}$$

and

$$g(z) = \frac{1}{1 + e^{-z}} \tag{2.3}$$

$$\theta = [\theta_0, \theta_1, \theta_2, \theta_3, \ldots \theta_n] \tag{2.4}$$

$$X = [x_0, x_1, x_2, \ldots x_n] \tag{2.5}$$

where, X is the feature vector and θ is the set of weights associated with the feature vector. The value of weight vector is to be adjusted during the training process. The probability that a given input feature vector belongs to the class 0 is given by the conditional probability statement

$$h_\theta(X) = p(D = 0|x_1, x_2, \ldots, x_n; \theta) \tag{2.6}$$

The probability of a given input feature vector, which belongs to class 1, is given by the conditional probability statement:

$$h_\theta(X) = p(D = 1|x_1, x_2, \ldots, x_n; \theta) \tag{2.7}$$

From equations 2.6 and 2.7 the following equation can be concluded,

$$p(D = 0|x_1, x_2, \ldots, x_n; \theta) + p(D = 0|x_1, x_2, \ldots, x_n; \theta) = 1 \tag{2.8}$$

or

$$p(D = 0|x_1, x_2, \ldots, x_n; \theta = 1 - p(D = 1|x_1, x_2, \ldots, x_n)) \tag{2.9}$$

Equations 2.8 and 2.9 are used to predict the probability of the feature vector belonging to class 0 or class 1. In order to fit the parameters in *logit* transformation (denoted by *logit* $p(x)$), following equations are used:

$$logit\ p(x) = \ln \frac{p(x)}{1 - p(x)} \tag{2.10}$$

where, $p(x)$ is the logistic model as defined in the equations 2.6 and 2.7.

$$p(x) = \frac{1}{1 + \exp -(\theta_0 + \theta.X)} \tag{2.11}$$

The denominator term in equation 2.10 can be written as,

$$1 - p(x) = 1 - \frac{1}{1 + \exp -(\theta_0 + \theta.X)} = \frac{\exp -(\theta_0 + \theta.X)}{1 + \exp -(\theta_0 + \theta.X)} \tag{2.12}$$

Dividing, $p(x)$ by $1 - p(x)$ we get,

$$odds = \frac{p(x)}{1 - p(x)} = \frac{\frac{1}{1+\exp -(\theta_0+\theta.X)}}{\frac{\exp -(\theta_0+\theta.X)}{1+\exp -(\theta_0+\theta.X)}} = \exp(\theta_0 + \theta.X) \tag{2.13}$$

The term, $\frac{p(x)}{1-p(x)}$ gives the ratio between the probabilities of a feature vector belonging to a particular class to that of not belonging to the particular class, described as the *odds* of happening of an event. By applying natural logarithm in equation 2.13, the *logit* transformation is given by equation 2.14.

$$\ln \frac{p(x)}{1 - p(x)} = \ln \exp(\theta_0 + \theta.X) = \theta_0 + \theta.X \tag{2.14}$$

where, θ_0, is the bias term used while flitting a decision boundary. The input data set that consists of post fault current values is highly nonlinear. This complex nonlinear values can fit LR by modelling them by a polynomial regression method. Polynomial regression method gives a polynomial set as per the relationship between the attribute and prediction that fits LR model [72]. Now, we have a polynomial function in terms of θ and x as input to our hypothesis function.

$$h_\theta(X) = g(\theta_0 + \theta_1 x_1 + \theta_2 {x_2}^2, \dots) \tag{2.15}$$

Equation 2.15 gives a nonlinear decision boundary. So the data set, which is not linearly separable were taken to a multi-dimension space, may now become separable.

2.2.3 Cost function

Cost function is used to fit the weight vector given by equation 2.4. The weights are finalized during the training process. Linear regression uses the squared average between the output of hypothesis function and actual output over the entire training

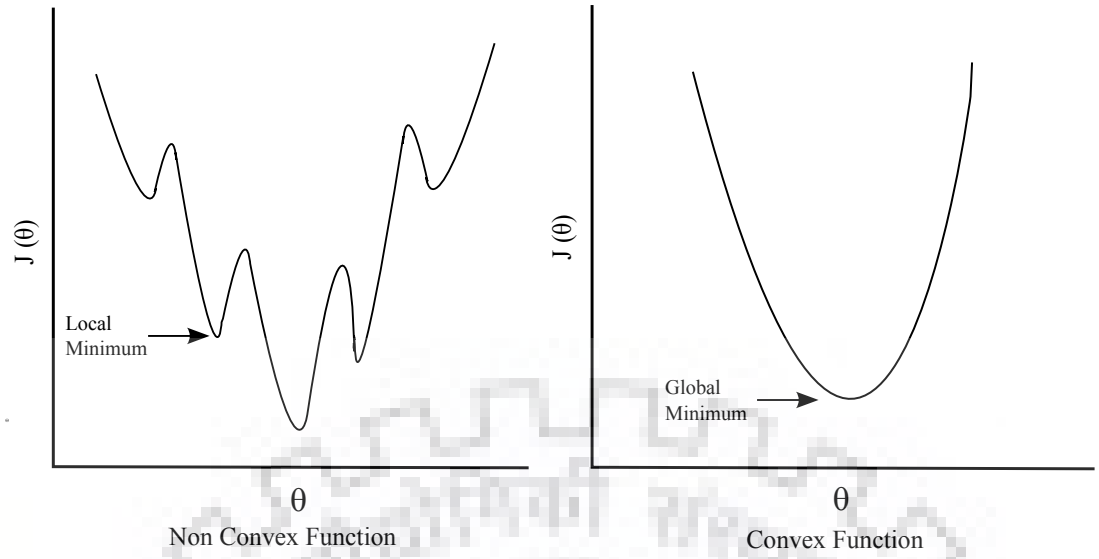

Fig. 2.2: Non convex and convex cost function.

data set as the cost function.

$$J(\theta) = \frac{1}{m}\sum_{i=1}^{m}\frac{1}{2}(h_\theta(x_i) - D_i)^2 \tag{2.16}$$

where, m is the total number of training samples. A cost function is defined as the cost the learning algorithm would pay if the hypothesis function has an output $h_\theta(X)$ for an actual output of D. Attention to be given that the $h_\theta x$ is a binary sigmoidal function, which is a nonlinear function and if we apply equation 2.16 to it to calculate cost function then the cost function is a nonconvex function having many local minima (Fig. 2.2). Then the gradient descent may strike at a local minima, and the global optimum point(minima) may not be found during convergence. So, a convex cost function is used in this paper which is having only one global minimum point. So $J(\theta)$ can be redefined as

$$J(\theta) = \frac{1}{m}\sum_{i=1}^{m} Cost(h_\theta(x^{(i)} - D^{(i)})) \tag{2.17}$$

which is the sum of cost functions across the entire training set, and

$$Cost(h_\theta(x), D) = \begin{cases} -\log(h_\theta(x), D) & \text{if } D = 1 \\ -\log(1 - h_\theta(x)) & \text{if } D = 0 \end{cases}$$

Because of binary classification, we can combine the two conditions as:

$$Cost(h_\theta(x), D) = -D \log h_\theta(x) - (1 - D) \log(1 - h_\theta(x)) \tag{2.18}$$

So, our cost function with a convex function can be written as

$$J(\theta) = -\frac{1}{m} \sum_{i=1}^{m} D^{(i)} \log h_\theta x^{(i)} + (1 - D^{(i)}) \log(1 - h_\theta x^{(i)}) \tag{2.19}$$

In order to regularize the decision boundary, a regularization parameter is added to the cost function as given by equation 2.19.

$$J(\theta) = -\frac{1}{m} \sum_{i=1}^{m} D^{(i)} \log h_\theta x^{(i)} + (1 - D^{(i)}) \log(1 - h_\theta x^{(i)} + \frac{\lambda}{2m} \sum_{j=1}^{n} \theta_j^2) \tag{2.20}$$

where, m is the size of the training data and λ is the regularization parameter. It is to be noted that the term $\frac{\lambda}{2m}$ becomes very small with a large value of m, which underfits the decision boundary, whereas smaller value of m overfits the decision boundary. With the given cost function in equation 2.19, we have to fit the values of θ so that $J(\theta)$ is minimized. By setting the values of θ, we are setting the parameters for future predictions during the testing phase. With the gradient descent algorithm, some initial values of θ are assumed, and with each iteration, the values are updated simultaneously with the following equations.

$$\theta_j = \theta_j - \alpha \frac{dJ(\theta)}{d\theta_j} \; for \; j{=}1 \; to \; n \tag{2.21}$$

and,

$$\theta_j = \theta_j - \alpha \sum_{i=1}^{m} (h_\theta(x^{(i)}) - D^{(i)}) x_j^{(i)} \; for \; j{=}1 \; to \; n \tag{2.22}$$

where, α is the learning rate. A smaller value of learning rate lowers the processing speed of the algorithm, whereas a higher value of α may overshoot the cost function and leads to a higher value of cost function. The details of the processes involved in logistic regression classifier is shown in Fig. 2.3

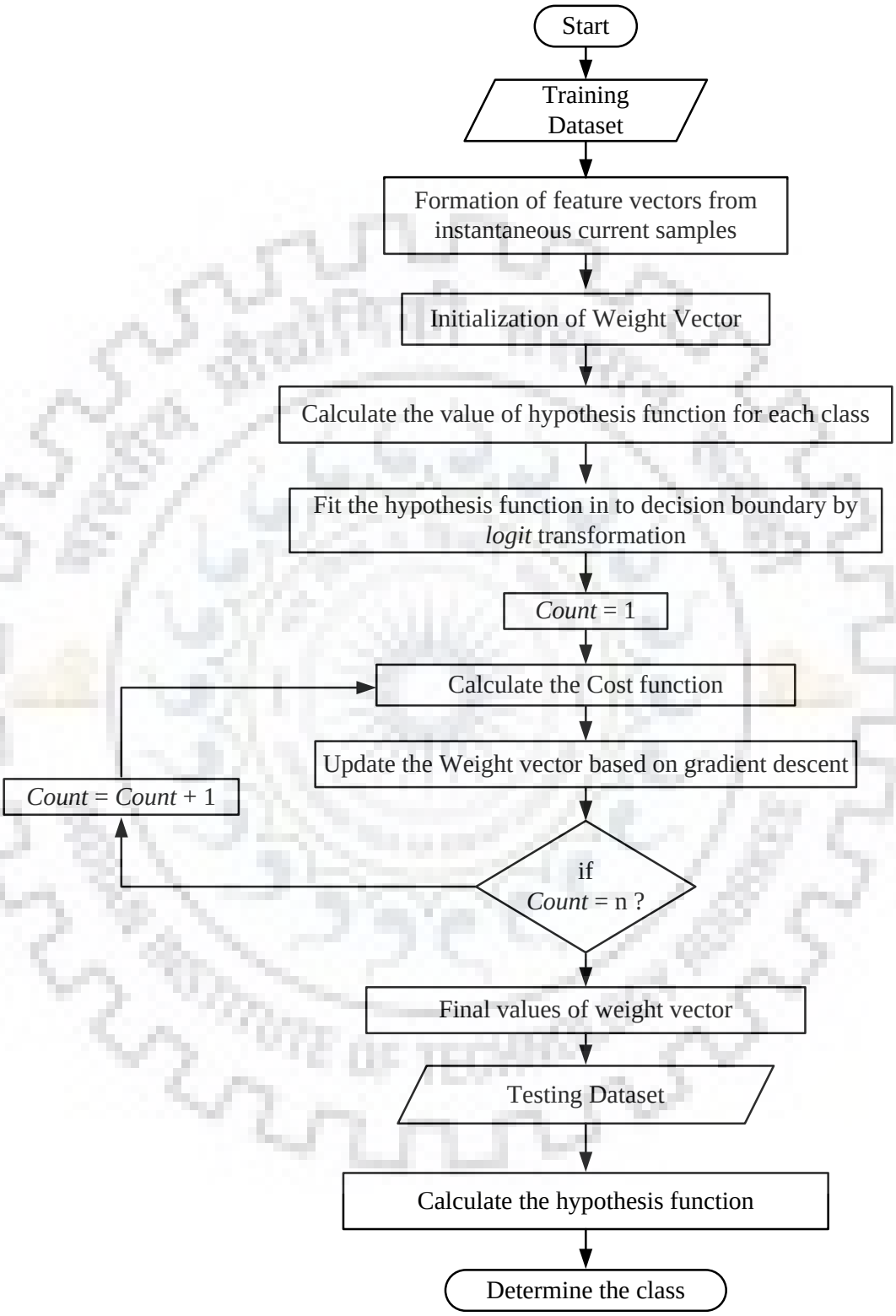

Fig. 2.3: Flow chart of Logistic Regression Classifier

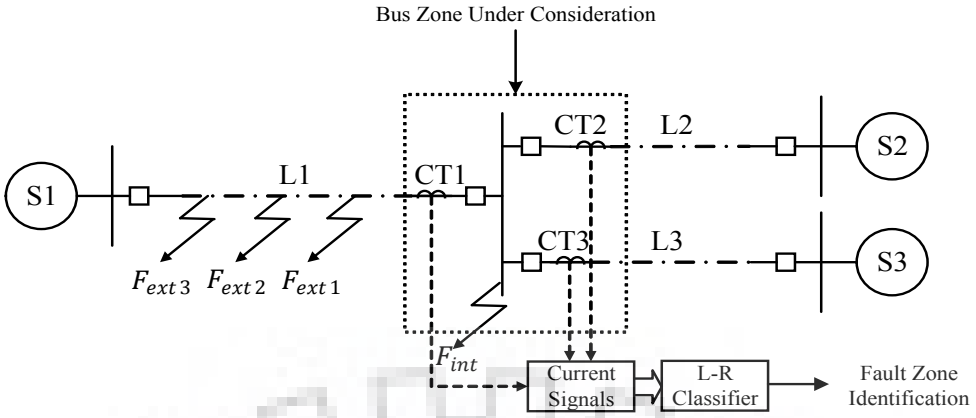

Fig. 2.4: Single line diagram for the system under study

2.3 System under study

Fig. 2.4 shows the single line diagram of an existing 400-kV Indian power system. As shown in Fig. 2.4, three generators (S1, S2, and S3) are connected to the busbar through bays L1, L2 and L3. The three CTs, installed on each bay, are used to acquire current signals. In this study, a sampling frequency of 1 kHz with a fundamental frequency of 50 Hz is used. The line and system parameters can be referred from Appendix-I.

2.4 Selection of system and fault parameters

The effectiveness of the proposed scheme has been evaluated for variations in source impedace (Z_{G1}, Z_{G2} & Z_{G3}) with eight different combinations (C1 to C8) as shown in Table 2.1. In order to incorporate wide variation in fault parameters, for each of source impedance (SI) combinations as shown in Table 2.1, four values of load angles (0, 10, 20 and 30 degrees), six values of fault resistance (0 Ω to 50 Ω in 10 Ω steps), five values of Fault Inception Angle (FIA) (0, 45, 90, 135 and 150 degrees) and ten types of faults have been considered. This results in generation of 1200 cases (4 × 6 × 5 × 10) for internal faults. Furthermore, external faults at three different locations (F_{ext1}, F_{ext2} and F_{ext3}) at 10%, 30% and 50%, respectively, on bay L1 have been simulated. Hence, a total of 4 (δ) × 6 (R_f) × 5 (FIA) × 10 (F_{type}) × 3 (F_{loc}) = 3600 external faults have been simulated. In this fashion, 9,600 (1200 × 8 (SI)) internal faults and 28,800 (3600 × 8 (SI)) external faults have been investigated in this work. Hence, a total of $38,400(9,600 + 28,800)$ cases have been used for validating the authenticity

Table 2.1: Different combination of source impedance

Cases	$Z_{G1}\%$	$Z_{G2}\%$	$Z_{G3}\%$
C1	100	100	100
C2	100	80	100
C3	100	100	80
C4	80	100	100
C5	100	120	120
C6	100	120	100
C7	100	100	120
C8	120	100	100

Table 2.2: Division of training and testing data

Fault Zone	Cases	Fault type	$R_f(\Omega)$	FIA°	δ°	$F_l\%$	Total data
Internal	C1-C8	10	0,20 30,40 50	0,45 90,150	10, 30	-	8×10 × 5 ×4×2 = 3200
External	C1-C8	10	0,20 30,40 50	0,45 90,150	10, 30	10, 50	8×10 × 5 ×4×2 ×2 = 6400
Total training data							9600

of the presented scheme. The variations of fault and system parameters along with total data generated for training and testing of the proposed LR classifier are shown in Table 2.2. To avoid manual error and also to make the simulation process more straightforward, a model has been designed in PSCAD/EMTDC. This model generates fault data automatically and stores them in the corresponding file. The Bergeron line model is used to represent transmission lines.

2.5 LR classifier based proposed scheme (87BLR)

The basic block diagram of the proposed scheme (87BLR) is shown in Fig. 2.5. Initially, one cycle post fault current signals from CTs of all bays (3) are obtained by the Data Acquisition Units (DAUs). The relay is configured off-line with 9,600 training cases consisting internal as well as external faults. The sampling frequency of 1 kHz for 50 Hz fundamental frequency (i.e., 20 samples per cycle) is used. Hence, one cycle post fault current signals of all three phases from all three CTs produce 180 samples. (20 samples for one cycle × 3 phases × 3 signals from three bay CTs). So, 180 samples in each row is utilized to formulate a feature vector for LR classifier. Therefore, for 9,600

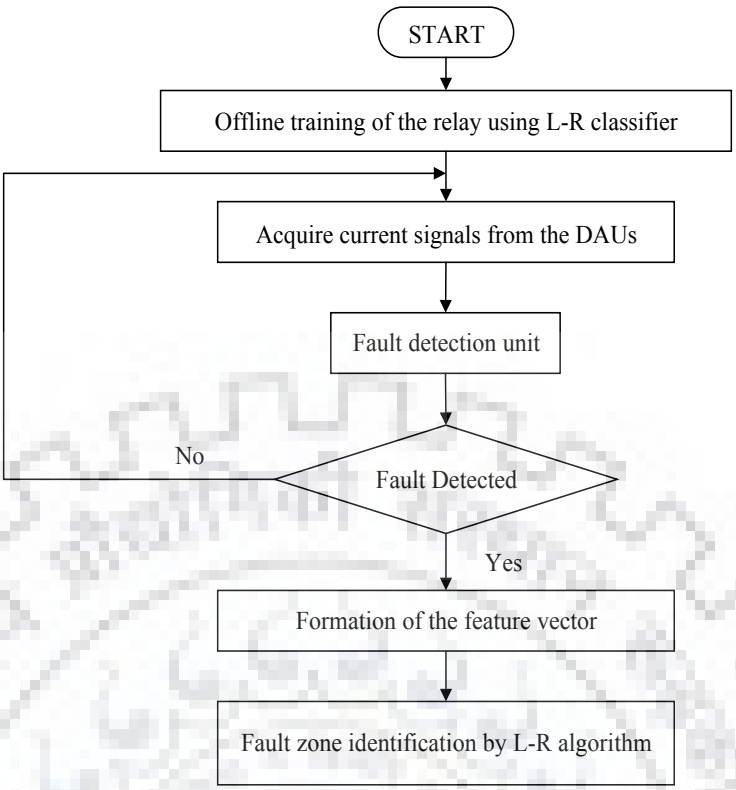

Fig. 2.5: Block diagram of the proposed scheme

training cases, a training set of size 9,600 $\times$ 180 is formulated.

2.5.1 Selection of training data size and regularization parameter

It is worthwhile to note that the training set must contain fault cases considering wide variation in system and fault parameters. Subsequently, the size of the training data set should be sufficient to minimize the misclassification rate. Therefore, to evaluate performance of the presented LR classifier in contradiction to the size of training data set, authors have generated training data sets with different size and remaining cases have been utilized to prepare the testing data sets. The results are provided in Table 2.3. It has been observed from Table 2.3 that at first, the misclassification rate is relatively higher for a small-sized training data set (2% and 2.5 %) because the training data set is not reasonable to reflect wide variation in system disturbances. For this purpose, the authors have considered different combinations of system and fault pa-

Table 2.3: Results obtained from different size of training dataset

Testing Data	Training Data	Testing Data (%)	Training Data (%)	False clsf. data	Mis. clsf. rate (%)	Accuracy (%)
37632	768	98	2	3354	8.91	91.09
37440	960	97.5	2.5	2381	6.40	93.60
36480	1920	95	5	1970	5.40	94.60
34560	3840	90	10	1697	4.91	95.09
32640	5760	85	15	774	2.37	97.63
30720	7680	80	20	252	0.82	99.18
28800	9600	75	25	88	0.31	99.69
26880	11520	70	30	81	0.30	99.70
24960	13440	65	35	73	0.29	99.71
23040	15360	60	40	67	0.29	99.71
21120	17280	55	45	60	0.28	99.72
19200	19200	50	50	54	0.28	99.72

rameters to construct the training data set instead of using random split. It can also be seen from Table 2.3 that the misclassification rate (%) decreases with increase in the size of training dataset. Moreover, for training data set size above 25%, the enhancement in misclassification rate is not found to be much noteworthy for the increase in size of training data set.

A larger dimensional training may over-fit the decision boundary, which turns out to be a bad predictor for unseen dataset. It is to be noted from equation 2.20 that the term $\frac{\lambda}{2m}$ becomes very small with large value of m, which under-fits the decision boundary whereas smaller value of m overfits the decision boundary. The variation in accuracy given by the proposed classifier with different values of the regularization parameter (λ) and training set size (m) is shown in Table 2.4. In Table 2.4, the value of λ is varied from 0.1 to 1.0 whereas the value of m (which indicates percentage training data size with reference to total data size) is varied from 15% to 30%. It has been observed from Table IV that $\lambda = 0.6$ and $m = 25\%$ gives the highest accuracy of 99.69%, and hence, they are chosen for the proposed classifier.

2.5.1.1 Performance Evaluation Parameters

Application of modelling techniques without proper validation may result in poor results if new subjects are tested. Model validation is the most important step to validate the stability and reasonableness of the classifier. The confusion matrix presented in

Table 2.4: Variation in accuracy for different values of λ and m

λ	Accuracy for different values of m			
	m=5760 (15%)	m=7680 (20%)	**m=9600 (25%)**	m=11520 (30%)
0.1	97.41	98.70	99.11	98.62
0.2	95.73	99.01	98.97	98.62
0.3	98.15	98.61	98.85	99.23
0.4	98.31	98.02	99.11	98.90
0.5	97.46	97.91	97.76	97.22
0.6	98.78	99.21	**99.69**	99.14
0.7	98.31	98.56	99.00	99.61
0.8	98.11	98.22	98.61	98.50
0.9	97.62	98.21	98.05	98.14
1	98.45	97.82	97.50	98.21

Table 2.5: Confusion Matrix

		Predicted	
		Positive	Negative
Actual	Positive	True Positive (TP)	False Negative (FN)
	Negative	False Positive (FP)	True Negative (TN)

Table. 2.5 defines the terminologies used for binary classification. The overall accuracy of the model is the proportion of the true results when compared to the total number of cases.

$$\text{ACC} = \frac{\text{TPs} + \text{TNs}}{\text{TPs} + \text{TNs} + \text{FPs} + \text{FNs}} \tag{2.24}$$

Some of the indices used to evaluate the model are,

$$\text{True Positive Rate (TPR)} = \frac{\text{TPs}}{\text{TPs} + \text{FNs}} \tag{2.25}$$

$$\text{False Negative Rate (FNR)} = 1 - \text{TPR} = \frac{\text{FNs}}{\text{TPs} + \text{FNs}} \tag{2.26}$$

A high value of TPR and low FNR reflects the goodness of the model in predicting the positive class samples. In this fashion, a high TNR and low FPR reflects the goodness of the model in predicting the negative class samples.

$$\text{True Negative Rate (TNR)} = \frac{\text{TNs}}{\text{TNs} + \text{FPs}} \tag{2.27}$$

$$\text{False Positive Rate (FPR)} = 1 - \text{TNR} = \frac{\text{FPs}}{\text{TNs} + \text{FPs}} \tag{2.28}$$

Table 2.6: Confusion Matrix

True Positive 6346	False Negative 54
False Positive 34	True Negative 22366

Precision is the measure of true results over all positive results. It is the measure of correctness when it predicts a positive value for true positive value, whereas, *recall* is the fraction of positive values predicted over all the positive samples. It is the ratio of the true positives over all the actual positive values.

$$Precision = \frac{\text{TPs}}{\text{TPs} + \text{FPs}} \tag{2.29}$$

$$Recall = \frac{\text{TPs}}{\text{TPs} + \text{FNs}} \tag{2.30}$$

Another index *F1-Score* is used as the weighted average between precision and recall given by the equation

$$F1\text{-}Score = 2 \times \frac{Precision \times Recall}{Precision + Recall} \tag{2.31}$$

Mathematically, it is the ratio between the square of the Geometric mean and the arithmetic mean between *Precision* and *Recall*. F1 Score gives the arithmetic average when the two are very close to each other. An ideal F1-Score would be 1 for the best case against 0 for the worst case. ROC (Receiver Operating Characteristics) curve is a plot between the FPR and TPR as X and Y axes, respectively. AUC (Area Under the Curve) of ROC for a classifier measures the ability to determine true positive cases against false positive cases. Usually, AUC lies between 0.5 for a worst classifier to 1 for a perfect classification case.

2.6 Results and discussion

The above-discussed indices convey the idea that true identification of positive values (TPs) is more important than false identification of a negative value (FNs). Identification of an external fault as an internal one may disrupt the supply for a few hours, but non-detection of an internal fault may have severe consequences. So, for our study, we

Table 2.7: Performance Evaluation Indices

Performance evaluation indices	value
True Positive Rate (TPR)	0.9916
False Negative Rate (FNR)	0.0084
True Negative Rate (TNR)	0.9984
False Positive Rate (FPR)	0.0016
Precision	0.9946
Recall	0.9916
F1-Score	0.9930
AUC	0.9815
ACC	0.9969

have labelled the internal faults as positive class and external faults as negative class. The following subsections show the results obtained by varying different parameters, as discussed in the earlier sections.

As seen in the confusion matrix from Table 2.6, out of 6,400, total internal faults simulated 6,346 cases are identified correctly and out of 22,400 external faults simulated 22,366 cases are identified correctly. So, it can be concluded that identification of a fault zone with an overall accuracy of 99.69% has been achieved. The performance evaluation indices has been presented in Table 2.7. The high precision value indicates that the model is reliable when it predicts an internal fault. The true indices are consistently observed to remain near to 0.99 by varying various parameters and fault scenarios. The accuracy and reliability of the model is found encouraging for further studies. From the ROC curve, as shown in Fig. 2.6, and AUC (Area Under the Curve) it can be concluded that that the model is reliable in predicting actual internal faults (True positives) against predicted positives (False Positives).

2.6.1 Performance evaluation during varying fault and system parameters

The effectiveness of 87BLR has been estimated for different combinations of source impedance values (as mentioned in Table 2.1, which reflects system disturbances) and also for various types of faults. The simulation results are presented in Table 2.8 and Table 2.9, respectively. It has been noted from Table 2.8 and Table 2.9 that 87BLR can provide effective fault zone identification with an accuracy of more than 99% for

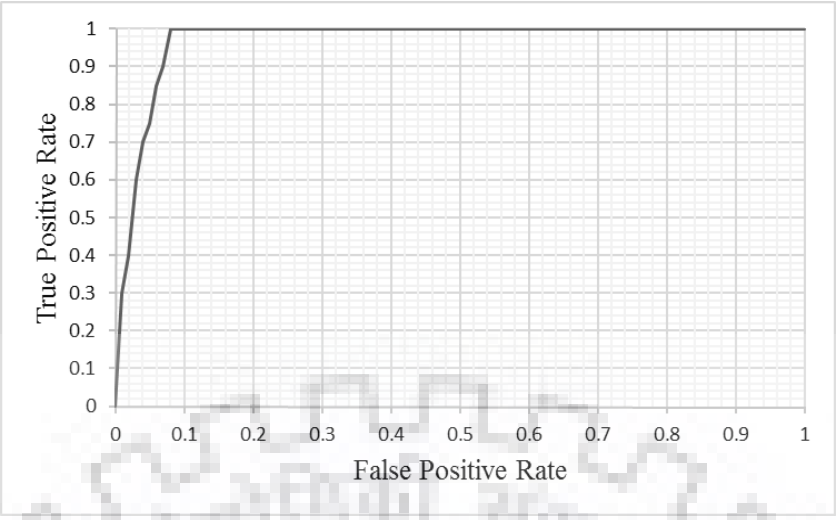

Fig. 2.6: ROC Curve

Table 2.8: Output of the proposed scheme for different source impedance combinations

Cases	Internal Faults		External Faults		Accuracy (%)
	TPs	FNs	TNs	FPs	
S1	790	10	2796	4	99.61
S2	798	2	2797	3	99.86
S3	790	10	2797	3	99.64
S4	797	3	2795	5	99.78
S5	793	7	2795	5	99.67
S6	795	5	2796	4	99.75
S7	792	8	2796	4	99.67
S8	791	9	2794	6	99.58

different combination of source impedances and fault types.

It is worthwhile to ensure the sensitivity of 87BLR in case of high resistance internal faults with varying fault inception angles and load angles. Fig. 2.7 depicts the fault zone identification accuracy produced by 87BLR during different values of load angle, fault inception angle, and fault resistance. It is to be noted from Fig. 2.7 that the presented scheme is able to detect high resistance internal faults with an overall

Table 2.9: Output of the proposed scheme for different type of faults

Fault Type	Internal		External		Accuracy (%)
	TPs	FNs	TNs	FPs	
L-G	1920	0	6684	34	99.60
LL-G	1894	26	6720	0	99.69
LLL-G	639	1	2240	0	99.96
LL	1893	27	6720	0	99.68

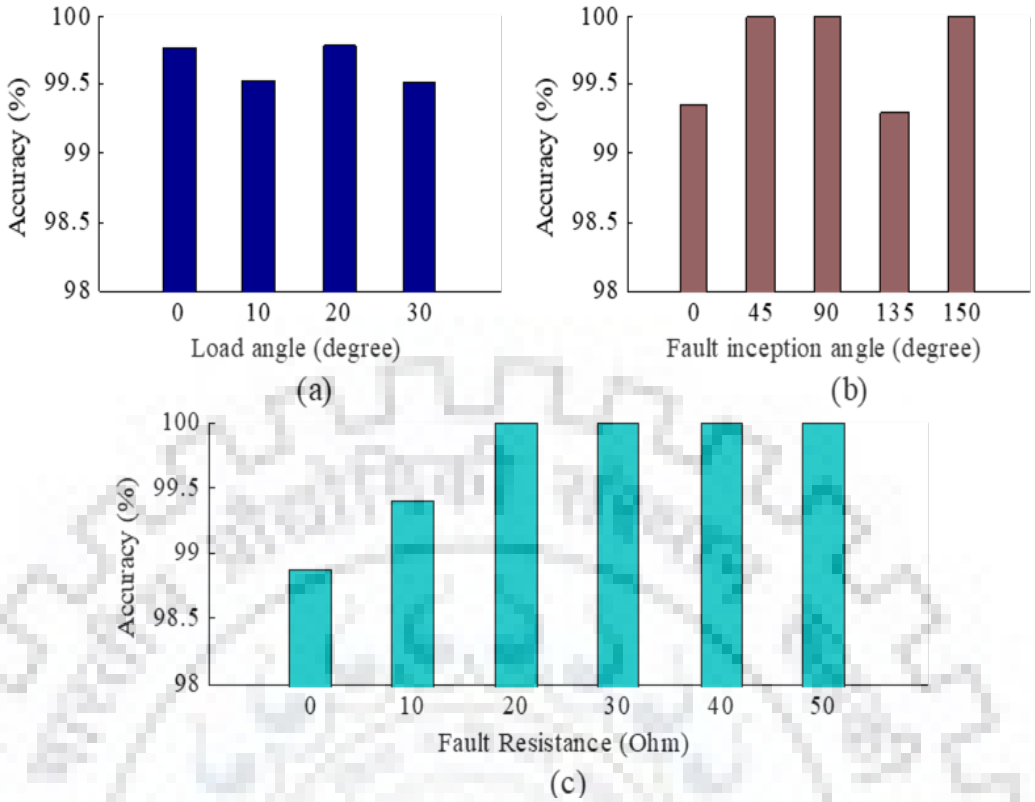

Fig. 2.7: Response of the proposed scheme in case of varying (a) δ (b) FIA (c) R_f

accuracy of 99% even with extensive change in FIAs and load angles.

2.6.2 CT saturation and inter-circuit faults

The effectiveness of the proposed LR based scheme has been evaluated by simulating various close-in faults with different fault location (50 m to 100 m from the bus under consideration) on bay L1. Different degrees of CT saturation has been obtained by changing the burden of the CT [73].

Moreover, it is also required to test the effectiveness of the presented scheme during inter-circuit faults on various bays. Different events like lightning or human errors may lead to a fault at different remote locations simultaneously, known as inter-circuit fault. To simulate inter-circuit faults, bay L1 has been altered from the single circuit transmission line to double circuit transmission line. The simulation results for both scenarios are shown in Table 2.10. It is to be observed from Table 2.10 that 87BLR produces an accuracy of 99.81% in case of saturation of CT during heavy through faults, which ensures its stability against mal-operation. At the same time, it also remains inoperative during inter-circuit faults.

Table 2.10: Output of the proposed scheme during CT saturation and inter-circuit faults

Fault case	Number of cases	Identification		Accuracy (%)
		TNs	FPs	
CT Saturation	540	539	1	99.81
Inter-circuit	1080	1080	0	100

2.6.3 Effectiveness of the proposed scheme in different busbar configurations

In order to evaluate the performance of proposed LR based scheme, double busbar arrangement, and one-and-half breaker busbar arrangement, as shown in Fig. 2.8 (a) and (b), have been modelled in PSACD/EMTDC software.

In Fig. 2.8 (a) both of the buses remain energized all of the time and work independently to each other. A bus tie breaker connects two different bus zones. Fault on any of the buses requires tripping of the lines connected to it. However, a line can be alternatively connected to the other bus after momentary interruptions, and the tie-breaker is closed for the transfer of the load. Hence, this arrangement improves the supply reliability. However, the relay settings become complicated in the case of a large substation.

In Fig. 2.8 (b) three breakers are used for every two lines; hence, the term one-and-half breaker is used. Here, two separate protection zones are formed. In the normal case, the lines are supplied from both of the buses. However, in case of a fault on any of the buses, corresponding CB and isolators are closed. Then, the supply is resumed from the healthy bus. Hence, this arrangement provides better operational flexibility and superior protection.

In case of both configurations, post-fault current signals of all the bays connected to the busbar have been acquired by the CTs. In total, 2,400 cases consisting of internal faults (1,200) and external faults (1,200) have been generated for each busbar arrangement. The effectiveness of the proposed classifier has been evaluated on the said data set, and the results are shown in Table 2.11. It is to be noted from Table 2.11 that 87BLR gives an accuracy of more than 99% for both double busbar arrangement and one-and-half breaker arrangement. Hence, 87BLR is applicable to different busbar arrangements and provides equally compatible accuracy.

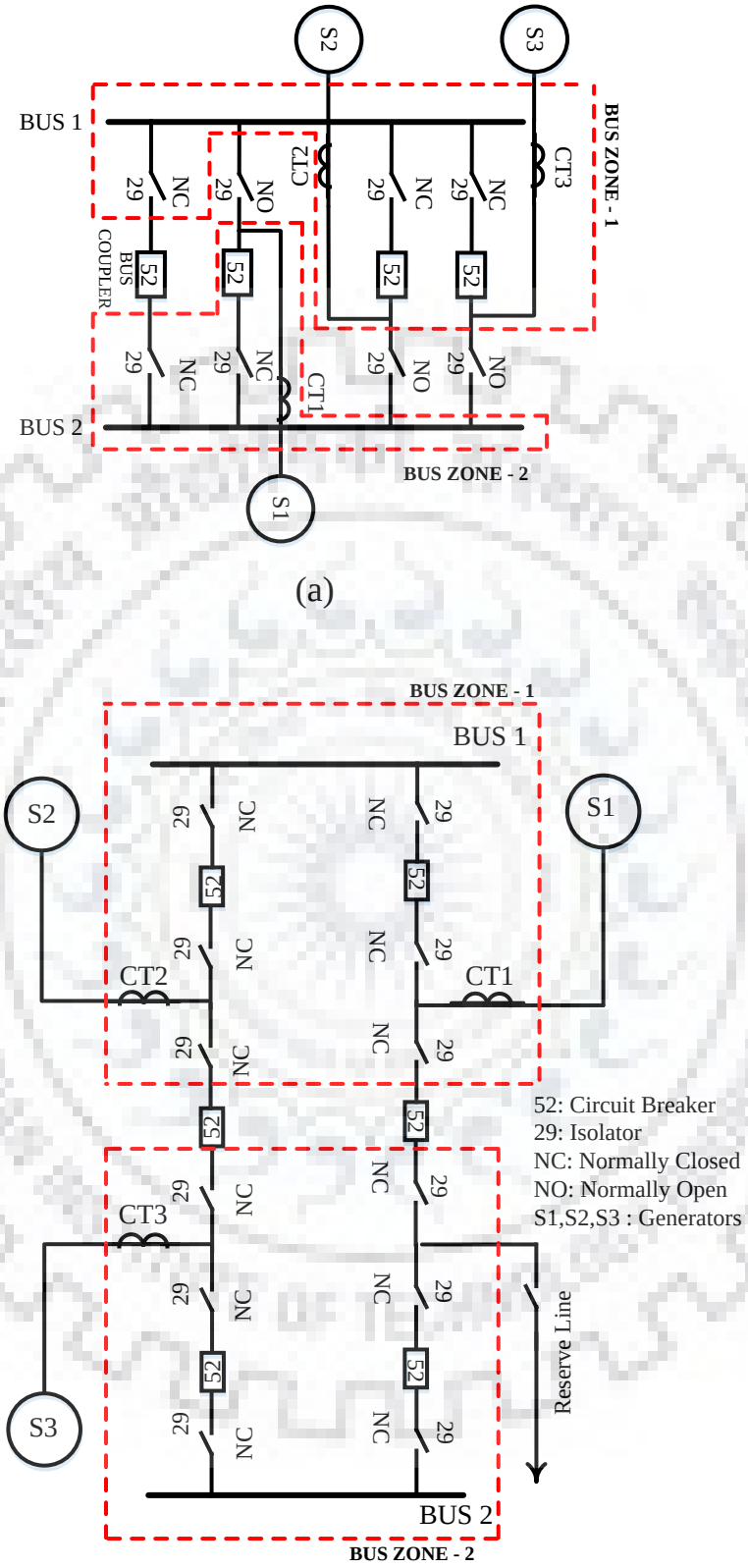

Fig. 2.8: Single line diagram of (a) double busbar arrangement (b) one-and-half breaker busbar arrangement

Table 2.11: Performance of the proposed classifier for double bus and one-and-half breaker busbar arrangement

Busbar arrangements	Fault type	Total cases	True	False	Accuracy (%)
Double busbar	Internal	1200	1188	12	99.0
	External	1200	1195	5	99.5
	Overall	2400	2383	17	99.3
One-and-half breaker	Internal	1200	1185	15	98.8
	External	1200	1195	5	99.6
	Overall	2400	2380	20	99.2

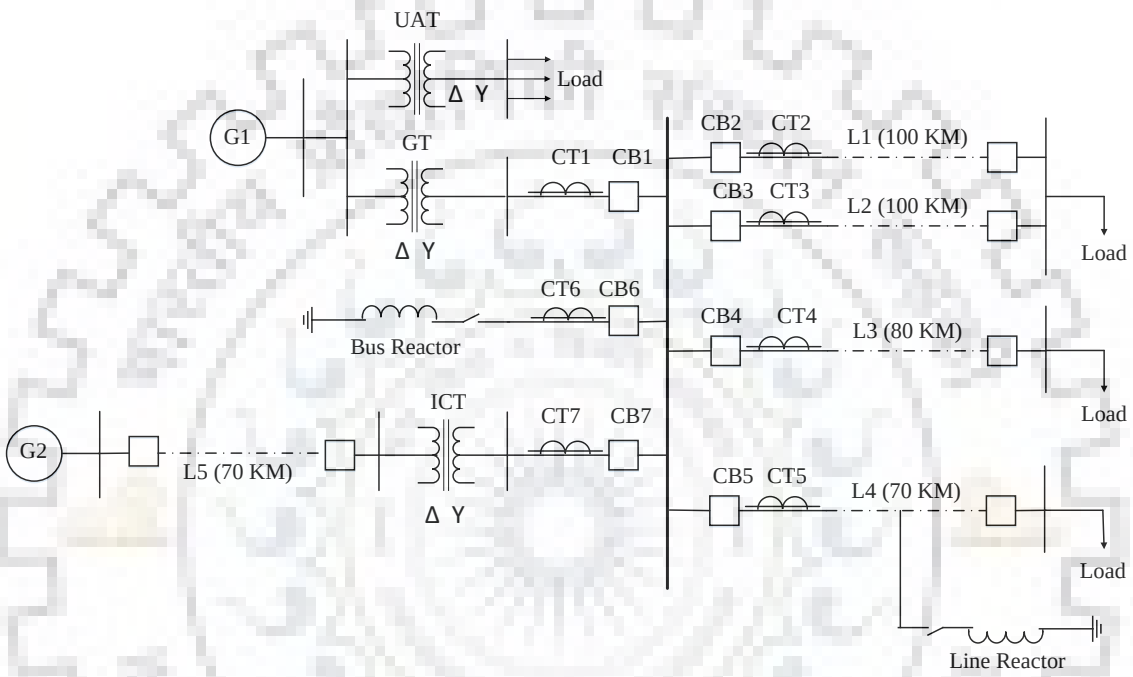

Fig. 2.9: Single line diagram of an existing 220-kV sub-station.

2.6.4 Robustness of the proposed scheme for different system configuration

The robustness of 87BLR, for an entirely different power system network with a different voltage level (220-kV), has been tested. The single line diagram of this network is shown in Fig. 2.9. A completely different test data set has been generated by varying fault and system parameters, as shown in Table 2.12. This newly generated test dataset also includes external faults on uncompensated/compensated transmission lines along with parallel circuits considering mutual effects. As shown in Fig. 2.9, generator G1 is connected to the 220-kV busbar through Generator Transformer (GT) and Unit Auxiliary Transformer (UAT). Another generator (G2) is connected to the same 220-kV busbar through bay L5 and Inter Connection Transformer (ICT). The bus reactor is

Table 2.12: Generation of test cases for 220-kV system.

Location	Fault type	FIA (°)	δ (°)	R_f (Ω)	Total test cases
1. On Gen G1 Terminal 2. GT internal fault 3. UAT internal fault 4. Faults at a distance 15% from the busbar on Line L4 5. Line-reactor 6. Bus-ractor 7. ICT internal fault	L-G (3) LL (3) LL-G (3) LLL-G (1)	0, 45, 90 115	10, 20 30	0, 5, 10, 15	$7 \times 10 \times 4 \times 3 \times 4 = 3360$

Table 2.13: Output of the proposed scheme for different system configuration

Fault type	SI variation	Test cases	Identification		Accuracy (%)
			TN	FP	
External	Z_{G2}-100%	3360	3168	192	94.29
	Z_{G2}-25%	3360	3251	109	96.76
	Z_{G2}-25%	3360	3174	186	94.46
Total		10,080	9593	487	95.16

also connected to the same busbar. Bays L1, L2, and L3 are emanated from the busbar and supplying the power to the load. Bays L1 and L2 are double circuit transmission line sharing the same right of way. A reconfigurable bus reactor bay is also connected to the busbar. The system and equipment parameters are given in Appendix-II.

The output of 87BLR in terms of fault zone identification accuracy in case of varying source impedance (SI) are shown in Table 2.13. It has been observed from Table 2.13 that 87BLR provides an overall accuracy of more than 95% in case of external faults on various equipment even with varying source impedance which indicates the stability of the proposed LR based scheme for a different system configuration.

2.6.5 Comparative evaluation of the proposed scheme with other existing schemes

In order to compare the performance of the proposed LR based scheme with other schemes based on ANN/SVM, the same training data set of 9,600 cases have been generated. In case of SVM, out of different kernel functions that are used to transfer the samples to a multidimensional space, the Gaussian RBF kernel is used by the au-

Table 2.14: Comparative evaluation of the proposed LR based scheme with SVM and ANN based schemes

Cases	No. of Test cases	LR		ANN		SVM	
		TP	Acc (%)	TP	Acc (%)	TP	Acc (%)
In-zone	6400	6346	99.16	5864	91.62	5551	86.73
Out-of-zone	22400	22366	99.85	21680	96.78	22163	98.94
Overall	28800	28712	99.69	27544	95.64	27714	96.23

thors. It has been widely reported in the past research papers/literature that Gaussian RBF kernel outperforms polynomial kernels in case of nonlinear classification [74–76]. Moreover, for tuning of the parameters such as cost function (C) and variance (g), different combinations have been considered. It is to be observed that a small value of C under-fits the hyperplane whereas a high value of C over-fits the decision boundary and turns out to be bad predictor. On the other hand, smaller/higher value of g indicates large/small variance among the features. The value of C is varied from 1 to 1000, whereas the value of g is varied from 0.001 to 1. Out of the large number of combinations, C=100, and g= 0.01 produces the highest accuracy of 96.23% and hence, chosen for the SVM based scheme.

Furthermore, a multi-layer perceptron model (deep-ANN) with three layers is used for the ANN-based scheme. As there are 180 features in our feature vector, the input layer consists of 180 nodes. To decreases the computation time, a single hidden layer with 200 nodes is selected. The output layer consists of two nodes. Initial weights are assigned to be 0.1, whereas a moderate learning rate of 0.025 is considered. An error tolerance of 1×10^{-7} is achieved in 63 number of iterations, and an overall classification accuracy of 95.64% is achieved.

Considering the above parameters (which are best for SVM and ANN-based scheme), comparative evaluation of the proposed LR based scheme is carried out with SVM and ANN-based schemes. The simulation results are shown in Table 2.14. It is to be noted from Table 2.14 that the accuracy given by the proposed LR based classifier (99.69%) is higher than ANN (95.64%) and SVM (96.23%) based classifiers.

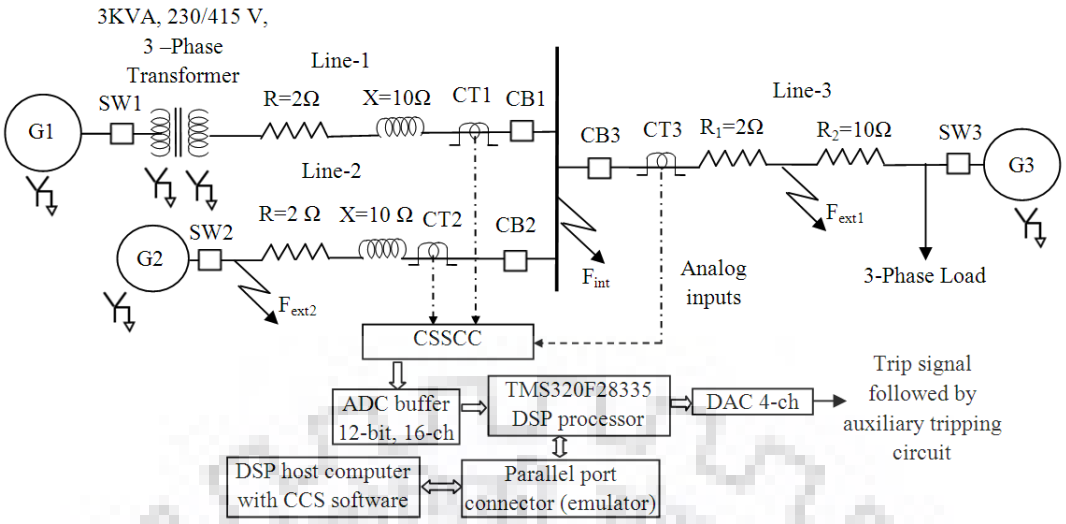

Fig. 2.10: Single line diagram of laboratory prototype

2.7 Testing of the proposed algorithm using laboratory prototype

2.7.1 Description of laboratory prototype

The single line diagram of the developed laboratory prototype is shown in Fig. 2.10. The 3-phase grid supply (415 V, 50 Hz) is utilized as the main source (G1). On the other hand, two 3-phase alternators (G2 and G3) are used to supply to the prototype. Four-pole contactors replicate the CBs. In order to develop bay-1, main source (G1), a three phase transformer (3 kVA, 415/230 V), variable resistor (R) and inductor (L) are utilized. Similarly, synchronous generator (G2) is connected to the busbar through a variable resistor (R) and inductor (L), which forms the bay-2. Similarly, bay-3 is developed by connecting synchronous generator (G3) to the busbar through variable resistor. A 3-phase star connected R-L load is also connected at bay-3. Initially, in order to synchronize all three bays, utility supply is synchronized with other two generators (G2 and G3) with the help of synchro-scope, voltmeter, and phase sequence meter. In order to simulate faults, four toggle switches are used. Variable rheostats having high continuous current carrying capacity (18 Ω, 12 A) are connected in series with fault path to limit the magnitude of fault current. In order to reproduce the effect of transmission line, parameters of transmission lines are modelled using variable rheostats of 18 Ω, 12 A and variable inductors of 5/10/20 Ω.

Moreover, in order to reduce the magnitude of current and also to achieve isola-

tion between power circuit and control circuit, protective class CTs having a rating of 10/5 A with burden of 25 VA are utilized. Furthermore, to obtain currents of all the three bays, CT secondary currents are acquired by the Analog to Digital Converter (ADC) of TMS320F28335 processor through Current Sensor Signal Conditioning Circuit (CSSCC). The purpose of using CSSCC is to scale down the input current signal prior to supplying to the ADC. It also converts CT secondary signal into its equivalent voltage signal (3 V peak-to-peak). The DSP processor with peripheral components is interfaced to a host PC through XDS510PP+ emulator pod.

The algorithm of the proposed LR based scheme is written in MATLAB 2014b software. It is interfaced with DSP processor through code composer studio (CCS 5.1). An emulator pod (XDS510PP+) is utilized for communication between the processor and host personal computer (PC). The program written in processor is linked/compiled with MATLAB software and finally executed using CCS 5.1. The signals of all the bay currents which represent internal/external faults are acquired with a sampling frequency of 1 kHz for a fundamental frequency of 50 Hz. Afterward, these signals are stored in the DSP processor. Later on, these signals are used for preparing feature vectors of LR classifier.

2.7.2 Prototype Results

To verify authenticity of the proposed LR based scheme on the laboratory prototype, various kinds of internal and external faults have been simulated. Various test cases have been generated by performing Line to Ground (LG), Line to Line (LL), Line to Line to Ground (LLG) and Line to Line to Line to Ground (LLLG) faults. The value of fault resistance is also changed from 0 Ω to 25 Ω. It is confirmed by performing numerous test cases that a signal is initiated by DSP processor to Digital to Analog Converter (DAC) port (5 V) during an internal fault. By evaluating a number of internal fault events acquired from the laboratory prototype, the digital signal processor issues a command to 5 volt DAC port. The output port of the DAC issues the final trip signal to the control circuit, which in turn gives final trip command to all CBs (contactors). Conversely, in case of external faults (simulated on bay-2 and bay-3), the DSP processor does not issue a trip signal, and hence, no tripping is issued by the auxiliary tripping circuit.

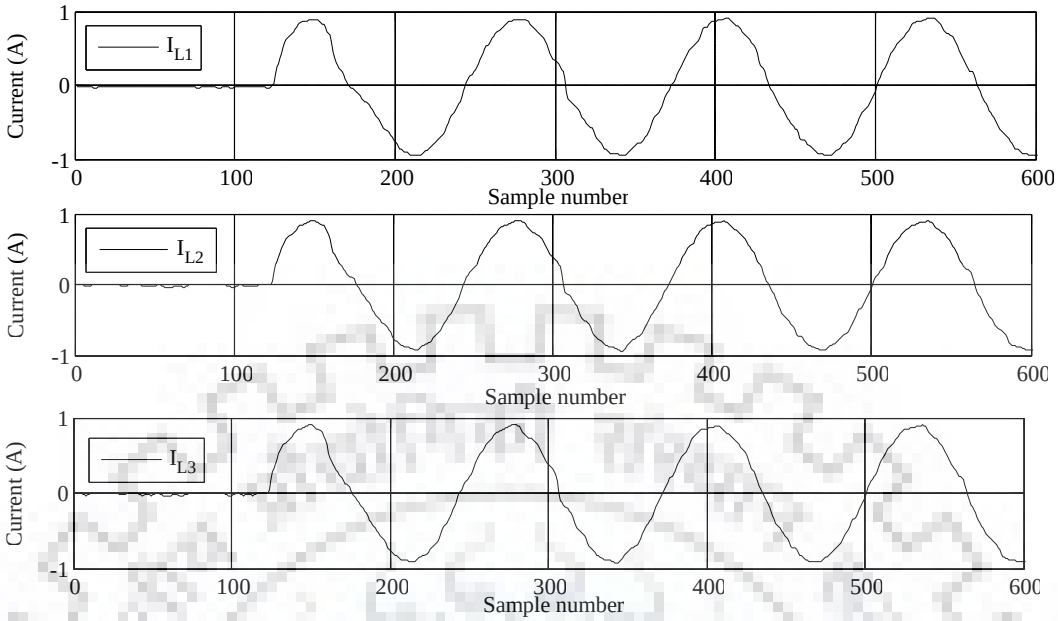

Fig. 2.11: Waveform of R-phase CT secondary current during LG internal fault

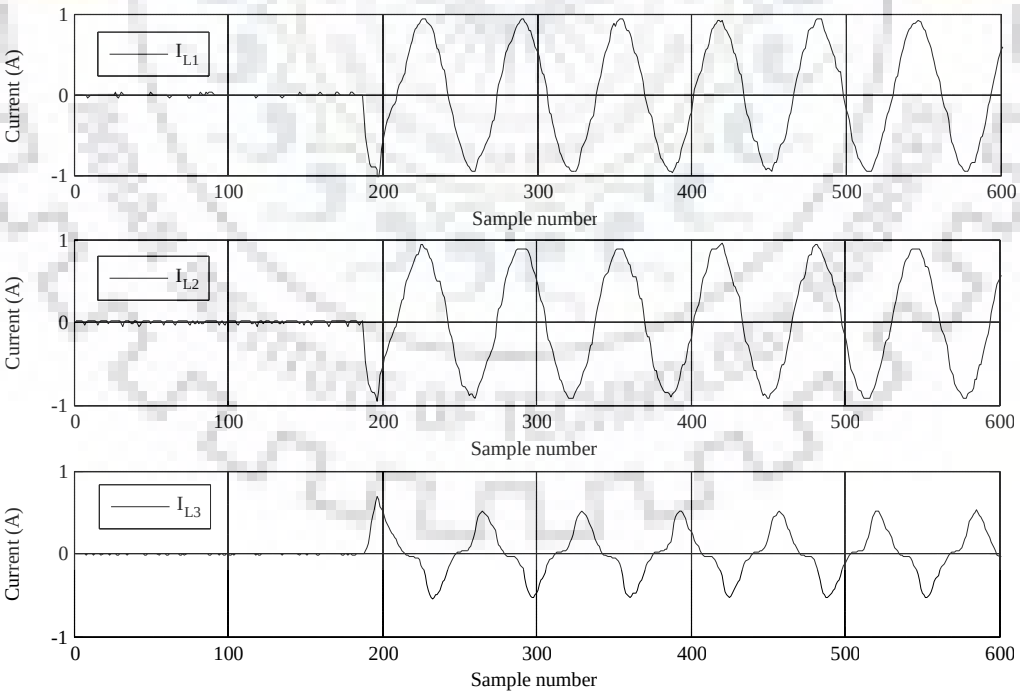

Fig. 2.12: Waveform of R-phase CT secondary current during LG fault on bay-3 with saturation of CT3

CT secondary waveforms are recorded with a high resolution (vertical resolution = 12 bit and sampling rate = 1 GS/sec per channel) four-channel Digital Storage Oscilloscope (DSO). The data samples from the DSO are exported in comma-separated values (CSV) format and then stored in the host PC. Fig. 2.11 shows captured waveforms of CT secondary current of one phase (R-phase) of all three bays in case of an internal fault on busbar. Moreover, the CT secondary current waveforms of R-phase of all the bays during LG out-of-zone fault on bay-3 with severe saturation of CT3 are shown in Fig. 2.12. It is to be noted from Fig. 2.11 that the waveforms of all bay currents have a similar pattern which indicates the occurrence of an in-zone fault on the busbar as all bay currents are directed towards the busbar. Conversely, as observed from Fig. 2.12, the waveform of bay-3 is in the opposite direction to the waveforms of the other two bays i.e., bay-1 and bay-2 which indicates external fault as the direction of one of the bay current is away from the busbar.

Table 2.15 shows the outcome of 87BLR when tested on the various internal and external fault signals acquired from the laboratory prototype. Here, the total 20 fault cases consisting of 12 internal faults and 8 external faults have been generated using laboratory prototype. It is to be noted from Table 2.15 that 87BLR accurately distinguishes internal faults with external faults. It is capable of detecting all the 12 in-zone faults correctly and issues trip signals to all the CBs. On the other hand, it remains stable during out-of-zone faults and does not initiate any trip signal. Moreover, it has been observed from Table 2.15 that the tripping time of 87BLR is of the order of 23 ms, which includes initiation of fault, sampling time, execution time, tripping time of contactor and some specific time delay. In addition, as the value of fault resistance increases in the case of LG and LLG faults, the overall tripping time of 87BLR also increases.

2.8 Conclusion

In this chapter, a new fault zone identification scheme for busbar using LR classifier is presented. The proposed scheme can produce very high fault zone identification accuracy of 99% when tested on an extensive data set of 28,800 cases with a minimal training data set of 9,600 cases. Moreover, it remains unaffected in case of heavy through faults

Table 2.15: Performance of the prototype during different types of fault.

Fault zone	Fault Type	Fault Resistance (Ω)	Response	Tripping time (ms)	Overall performance
In-zone	LG	5	Trip	22.758	Total cases: 12
		10	Trip	22.824	True classified: 12
		15	Trip	23.192	False classified: 0
		20	Trip	23.223	
		25	Trip	23.452	
	LL	0.1	Trip	23.928	
	LLG	5	Trip	22.841	
		10	Trip	22.005	
		15	Trip	23.112	
		20	Trip	23.452	
		25	Trip	23.656	
	LLLG	0.1	Trip	23.101	
Out-of-zone	LG	5	Restrain	–	Total cases: 8 True classified: 8 False classified: 0
		10	Restrain	–	
		15	Restrain	–	
		20	Restrain	–	
		25	Restrain	–	
	LL	0.1	Restrain	–	
	LLG	0.1	Restrain	–	
	LLG	0.1	Restrain	–	

with CT saturation condition. Furthermore, the proposed scheme 87BLR provides equally compatible accuracy (more than 99%) for double bus and one-and-half breaker busbar arrangement. The robustness of the proposed scheme has also been verified on a separate configuration with different voltage level. In addition, the performance of the proposed scheme has also been verified on the laboratory prototype. In this situation, it can classify internal and external faults accurately. The average tripping time of the proposed scheme is of the order of 23 ms for all types of internal faults even with considerable value of fault resistance. At last, comparative evaluation of the proposed scheme with other existing schemes indicates its superiority in case of different fault and system parameters.

Chapter 3

Numerical Busbar Differential Protection using Generalized Alpha Plane

In the previous chapter, development and performance of the statistical learning theory based protection scheme has been discussed. Despite its high accuracy in classifying internal and external busbar faults, the on-chip implementation is a major challenge. On the contrary, the operating characteristics of well-established differential protection can be improved for challenging CT saturation scenarios. In this regard, this chapter presents the development a busbar differential protection scheme based on Generalized Alpha Plane Approach (87BGAP). Subsequently, its performance and practicality for field implementation have been showcased.

3.1 Introduction

Busbar, in particular, is one of the vital parts of the power system as tripping of it causes disconnection of all associated transmission lines. On the contrary, any compromise in sensitivity can cause high replacement costs and forced alterations in system operations. As discussed in the previous section, reliability in the case of busbar faults is of utmost priority while designing the substation protection system. Increased short-circuit level in an interconnected power system network and state-of-the-art smart grid infrastructure needs higher protection requirements. Therefore, it is highly desirable

to achieve minimum fault clearance time. In fact, utilities have started mandating one-and-half cycle fault clearance time. The aforementioned reasons demand a faster and reliable operation of the relay [3, 4, 19, 68]. In this study, a new generalized alpha plane (GAP) based digital differential protection scheme for the busbar is presented. The operating and restraining currents are computed by calculating the vector and scalar sum of current phasors of each bay. Afterwards, these currents are converted into equivalent incoming and outgoing currents using the GAP approach. Finally, after calculating the ratio of equivalent outgoing and incoming current for each phase, they are mapped into the alpha plane.

3.1.1 State-of-the-art

Low-impedance percentage differential protection [16, 33, 37] is the long-established method used for the protection of power apparatus including the busbar. However, uncertain power system disturbances and close-in external faults with CT saturation may initiate false tripping of the above scheme. Moreover, it is unable to detect high resistance in-zone faults due to insignificant magnitude of operating current [71]. Superimposed-impedance based directional protection schemes [20, 21, 23] provide better stability against substantial CT saturation. However, due to the requirement of voltage signals along with current signals, the cost and complexity increase. In addition, the reliability of these schemes reduces in case multiple transmission lines connected to the busbar.

Schemes based on TW [43, 44, 77, 78] provide high-speed protection and remain less prone to CT saturation errors. However, production of insufficient incident wave during faults with small inception angle, appearance of the incident and reflected waves at the same instant during close-in fault and requirement of dedicated CTs are the several limitations of the above scheme. Protection schemes based on WT [46–48] extract useful information from post-fault current samples and provide localisation in both time and frequency domains. However, these schemes do not provide good accuracy when the fault signal contains channel noise or DC offset. Though AI-based techniques such as fuzzy logic and neural network [52] provide better fault zone identification accuracy, they require a large number of neurons and tedious training procedure. Hence, the application of AI-based techniques in busbar protection is still in black boxes and lacks

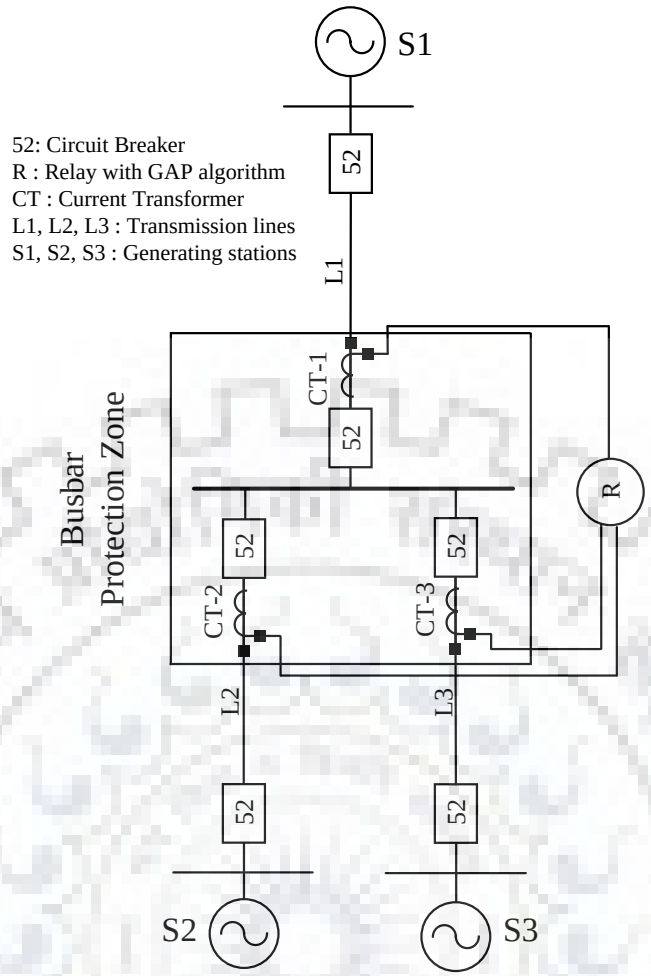

Fig. 3.1: Single line diagram of the 400-kV Indian power system.

transparency. Busbar protection schemes based on sophisticated machine learning algorithms like SVM and RVM provide good classification accuracy with diversified system parameters [55, 59]. However, probabilistic predictions are not feasible because of the abrupt behaviour of kernel functions. Moreover, on-chip implementation of the above schemes involves enormous complexity.

3.2 Proposed Protection Scheme (87BGAP)

3.2.1 System Study

Fig. 3.1 shows the single line diagram of an existing 400-kV Indian power generating system (Wanakbori, Kheda, Gujurat). Three generating stations (S1, S2, and S3) are connected to the substation busbar through transmission lines (L1, L2, and L3), each with a physical length of 100 km. The simulation model is developed using

PSCAD/EMTDC software package [79] and the transmission lines are modelled using Beregron model. The line and system parameters are given in Appendix-III.

3.2.2 Alpha Plane Characteristics

The concept of the alpha plane for differential protection of multi-terminal transmission lines was developed by Roberts *et al.* [80]. Primarily, the ratio of remote-end current and local-end current is calculated. In the case of normal operating conditions/external faults, the ratio lies inside the restraining region whereas it moves outside of the restraining region during internal faults [81].

The concept of the alpha plane is understood by a two-terminal line section as shown in Fig. 3.2 (a). Disregarding all possible errors, system non-uniformity, power angle, and impedance non-homogeneity, the ideal alpha plane characteristics are shown in Fig. 3.2 (b). As per equation 3.1, the alpha plane is defined as the ratio of remote-end current (I_R) and local end current (I_L).

$$\overrightarrow{\alpha} = \frac{\overrightarrow{I_R}}{\overrightarrow{I_L}} = a + jb = Ae^{j\theta} \tag{3.1}$$

As shown in Fig. 3.2 (b), $\overrightarrow{\alpha}$ lies on the real axis under ideal system operating conditions. In the case of external faults/normal operating conditions, $\overrightarrow{\alpha}$ stays close to the point (-1, 0). Conversely, in the case of an internal fault $\overrightarrow{\alpha}$ moves from the point (-1, 0) to the right half of the plane.

During outfeed conditions at the terminal L and R, $\overrightarrow{\alpha}$ moves to the left and right of (-1, 0), respectively. Taking cognizance of system non-uniformities like CT saturation error, line charging current, current alignment errors, channel asymmetry, and adaptive switch over, etc., the new alpha plane characteristic is shown in Fig. 3.2 (c). With reference to Fig. 3.2 (c), the radius of the bigger arc (R_1) is typically set in the range of 6 to 10 whereas the radius of inner arc (R_2) is taken as the reciprocal of the bigger arc. The above two settings modify the sensitivity without affecting the security from CT saturation and current ratio errors. The arc angle is set in the range of 160 to 210 degrees. This angular setting is decided in such a way that it can accommodate the points that arise because of CT saturation or current ratio errors without affecting the sensitivity. In the present work, the radius setting and the angle extended by the

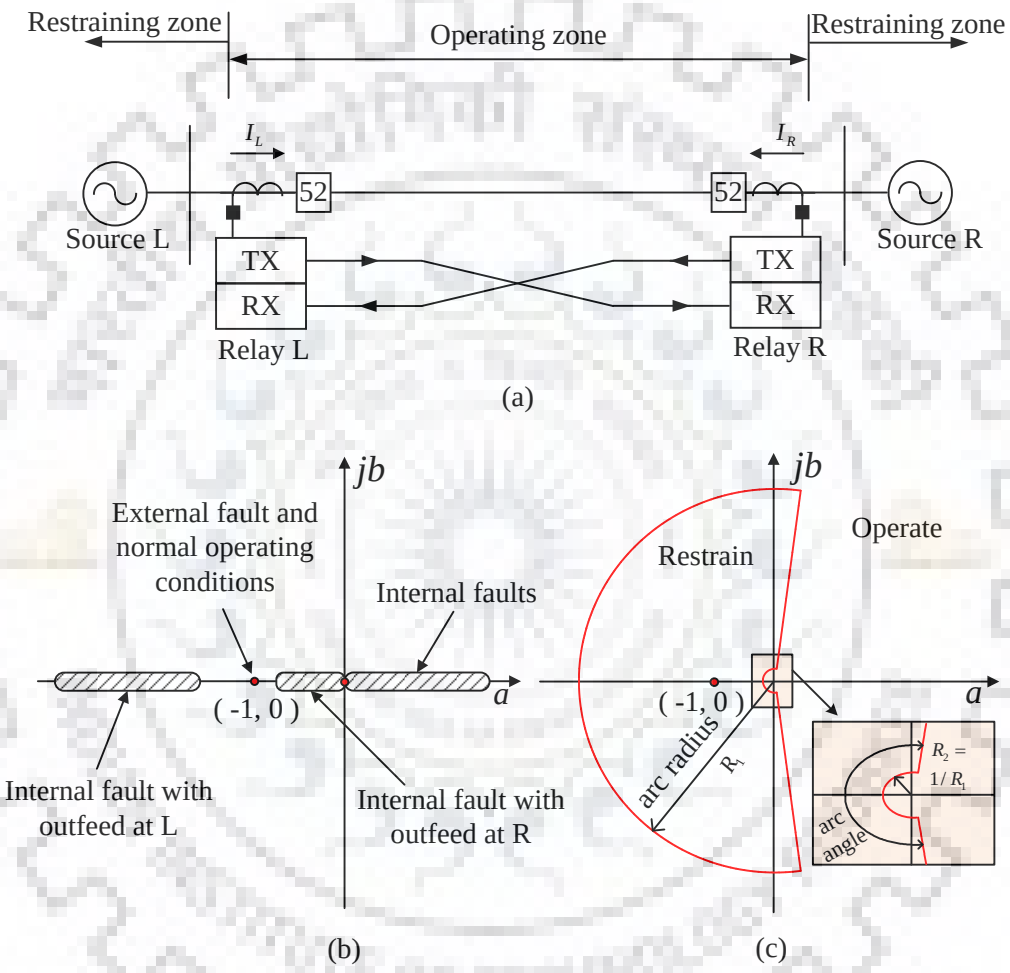

Fig. 3.2: Alpha plane characteristics: (a) Two-terminal transmission line, (b) In case of ideal conditions, (c) Considering system non-uniformity.

arc is taken as 6 and 195 degrees, respectively.

3.3 Generalized Alpha Plane (GAP) Customized for Busbar Protection

The developed GAP algorithm for busbar protection is explained in the following subsections.

3.3.1 Calculation of Operating and restraining current

The flowchart of the proposed algorithm is illustrated in Fig. 3.3. One cycle CT secondary current signals from each bay are acquired by the data acquisition system. Here, a sampling frequency of 4 kHz for a fundamental frequency of 50 Hz (80 samples/cycle) has been used to incorporate IEC 61850-9-2 communication protocols. The phasor computation of the acquired current signals is carried out using a full cycle Modified Discrete Fourier Transform (MDFT) algorithm. It is to be noted that the MDFT algorithm is capable of removing the decaying DC component, present in the fault current signal, efficiently compared to the conventional Discrete Fourier Transform (DFT) algorithm. Utilizing the calculated phasor values of current, the operating and restraining currents are calculated as per equations 3.2 and 3.3, respectively, for each phase (87LA, 87LB, and 87LC).

$$\overrightarrow{I}_{DIF(P)} = \sum_{i=1}^{N} \overrightarrow{I}_{i(P)} = I_{DIF(P),re} + jI_{DIF(P),im} \tag{3.2}$$

$$I_{RST(P)} = \sum_{i=1}^{N} \left| \overrightarrow{I}_{i(P)} \right| = I_{RST(P),re} \tag{3.3}$$

3.3.2 Calculation of two-current equivalents

Fig. 3.4 shows the transformation of the N-terminal busbar into an equivalent 2-terminal busbar. With reference to Fig. 3.4 (a) and as per equations 3.4 and 3.5, the resulting incoming equivalent current and outgoing equivalent current of the 2-terminal busbar should result in the same differential and restraining current as that of the N-terminal busbar.

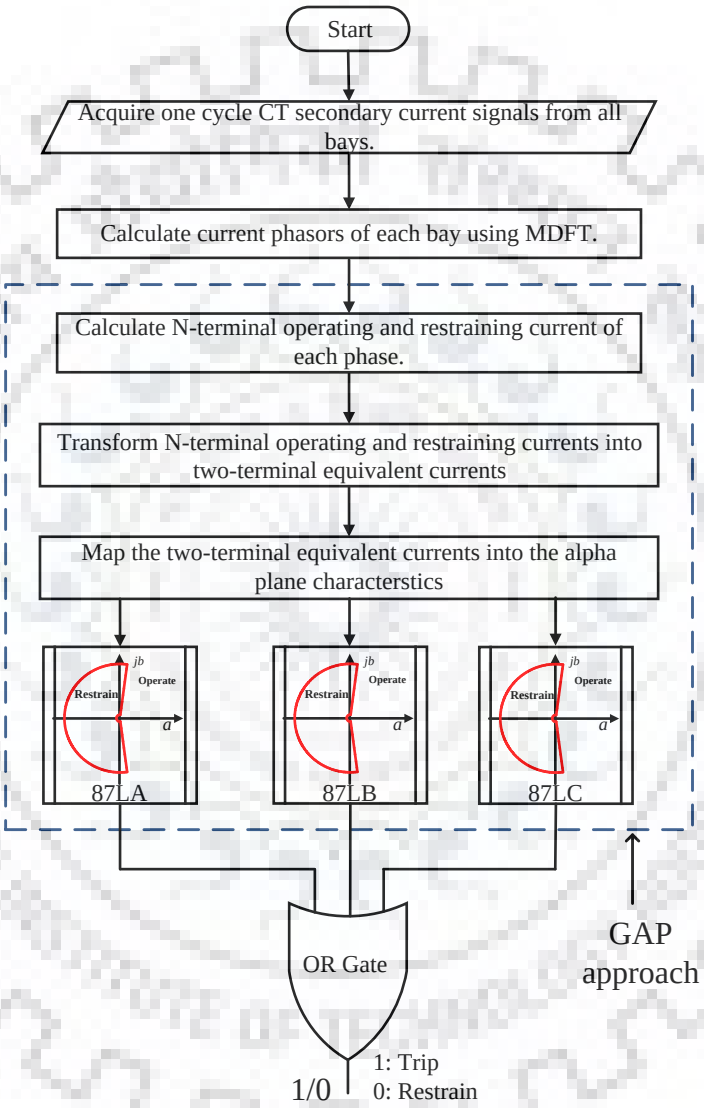

Fig. 3.3: Flowchart of Generalized Alpha Plane based busbar protection scheme.

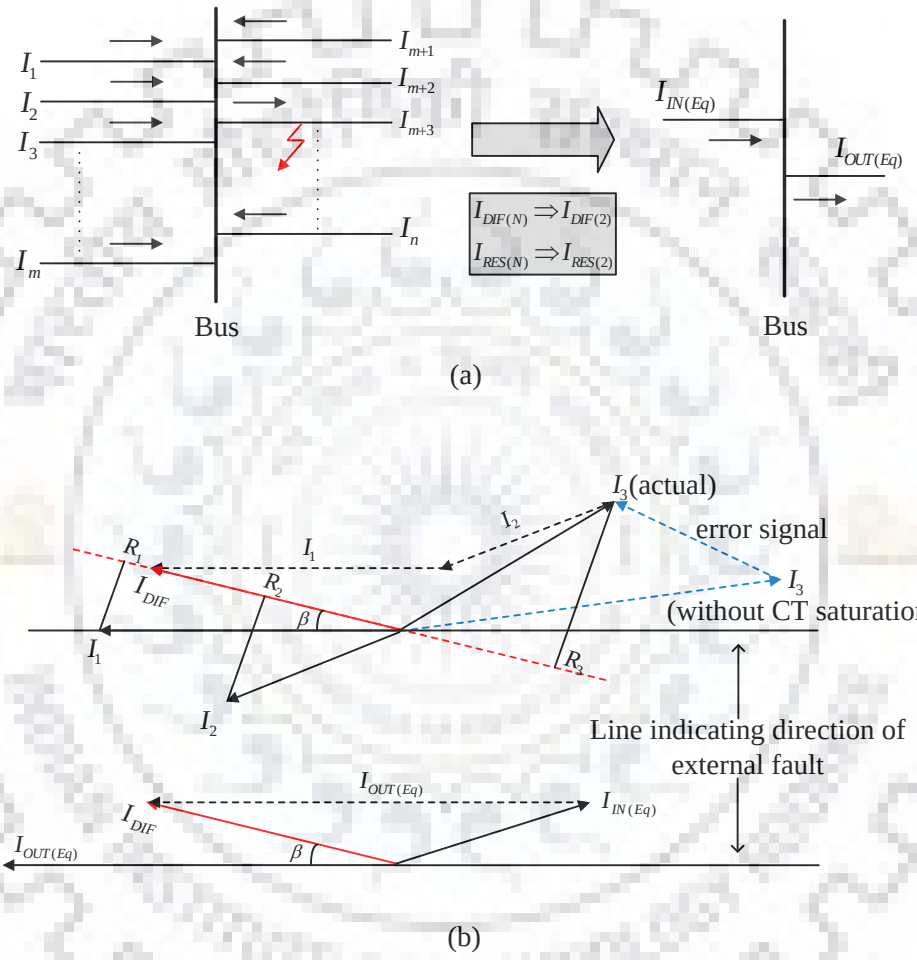

Fig. 3.4: Transformation of N-terminal busbar into equivalent two-terminal busbar. (a) Circuit diagram, (b) Phasor diagram.

$$\overrightarrow{I}_{DIF(N)} = \overrightarrow{I}_{DIF(2)} = \overrightarrow{I}_{IN(Eq)} + \overrightarrow{I}_{OUT(Eq)} \tag{3.4}$$

$$I_{RST(N)} = I_{RST(2)} = \left|\overrightarrow{I}_{IN(Eq)}\right| + \left|\overrightarrow{I}_{OUT(Eq)}\right| \tag{3.5}$$

where, the incoming and outgoing equivalent currents are given by equations 3.6 and 3.7, respectively.

$$\overrightarrow{I}_{IN(Eq)} = I_{IN(Eq),re} + jI_{IN(Eq),im} \tag{3.6}$$

$$\overrightarrow{I}_{OUT(Eq)} = I_{OUT(Eq),re} + jI_{OUT(Eq),im} \tag{3.7}$$

It can be observed from equations 3.4-3.7 that the transformation from N-terminal to 2-terminal busbar requires calculation of four unknowns in the form of real and imaginary parts of the incoming and outgoing equivalent currents. However, as described in 3.2 and 3.3, the differential current is a phasor quantity (both real and imaginary terms) whereas the restraining current is a scalar quantity (pure real). Therefore, the above transformation is constrained by three equations. Four unknown variables with a set of three equations result in an underdetermined system. This problem can be solved by aligning the angular position of one of the equivalent currents along an actual specific line current. The specific line current should be the one that has the highest projection on the differential current. The reason being, during an external fault, if a fictitious differential current arises then it is primarily because of the error signal arising from CT saturation. Hence, it is preferable to select one of the currents flowing out of the bus zone as the equivalent current.

Fig. 3.4 (b) shows the conversion of phasor diagram of a 3-terminal busbar currents (I_1, I_2, I_3) to equivalent 2-terminal busbar currents $I_{IN(Eq)}$ and $I_{OUT(Eq)}$. It is observed from Fig. 3.4 (b) that the bay current I_3 has been affected by CT saturation hence its magnitude is reduced and the phase angle has been advanced (maximum up to 90 degrees for extreme CT saturation). It can also be seen from Fig. 3.4 (b) that the phasor of differential current is in similar alignment with the error signal. Therefore, by selecting the phase of I_1 that is closer to the differential signal $I_{DIF(N)}$ as the reference signal, the outgoing equivalent current $I_{OUT(Eq)}$ is aligned in the direction of external fault current. In order to get the specific line current (reference current), the

projections R_i are drawn on, and the line current with the highest value of projection, obtained as per equation 3.8, is closest to the N-terminal differential current.

$$R_i = \left| re\left(\overrightarrow{I}_i \times conj\left(\overrightarrow{I}_{DIF(N)}\right)\right)\right| \tag{3.8}$$

The phase angle of the reference current (β) is selected as the phase angle of the outgoing equivalent current. Now, for the convenience of further calculations, an auxiliary signal is calculated as per equations 3.9-3.10.

$$\beta = angle\left(\overrightarrow{I}_{ref}\right) \tag{3.9}$$

$$\overrightarrow{I}_X = \overrightarrow{I}_{DIF(N)} \times 1\angle -\beta \tag{3.10}$$

Replacing $I_{DIF(N)}$ as I_X in equations 3.4-3.7, the equivalent currents can be calculated as per equations 3.11 and 3.12 [82]

$$\overrightarrow{I}_{OUT(Eq)} = \left(\frac{im\left(\overrightarrow{I_X}\right)^2 - \left(I_{RST(N)} - re\left(\overrightarrow{I_X}\right)\right)^2}{2\left(I_{RST(N)} - re\left(\overrightarrow{I_X}\right)\right)} + j\,im\left(\overrightarrow{I_X}\right)\right) \times 1\angle\beta \tag{3.11}$$

$$\overrightarrow{I}_{IN(Eq)} = \left(I_{RST(N)} - \left|\overrightarrow{I}_{IN(Eq)}\right|\right) \times 1\angle\beta \tag{3.12}$$

These two equivalent currents are then mapped into the alpha plane by calculating the $\overrightarrow{\alpha}$ as per equation 3.13 for each phase.

$$\overrightarrow{\alpha} = \frac{\overrightarrow{I}_{OUT(Eq)}}{\overrightarrow{I}_{IN(Eq)}} \tag{3.13}$$

When the calculated $\overrightarrow{\alpha}$ for any of the phases moves outside the restraining region, a tripping command is initiated.

3.4 Results and discussions

The performance of 87BGAP has been evaluated on different types of internal and external faults which is discussed in the upcoming sub-sections.

3.4.1 Internal faults

Fig. 3.5 (a) shows the response of 87BGAP during a single line to ground internal fault (L-G) on the busbar with fault resistance (R_F) = 15 Ω. It is observed from Fig. 3.5 (a) that the locus of operating points of all three phases remains close to the point (-1, 0) during the pre-fault condition. However, after the inception of the fault, the locus of operating points of the faulted phase (phase-A) traverses and resolves into the operating region. It has been observed from the literature that the conventional current based differential protection scheme may not be able to detect high resistance internal bus fault due to the lower value of the differential current. Fig. 3.5 (b) shows the response of the proposed scheme during a double line to ground fault (AB-G) with R_F = 100 Ω. It is to be noted from Fig. 3.5 (b) that the proposed scheme detects the said fault as the locus of operating points of faulted phases (A and B) moves and resolves into the operating region. The presented scheme operates correctly since it has considered the ratio of equivalent currents instead of the magnitude of differential currents as in case of the conventional current based differential protection scheme. Fig. 3.5 (c) and 3.5 (d) show the responses of the proposed scheme during a triple line to ground (ABC-G) and a double line (BC) internal fault on the busbar, respectively, with FIA = 0 degrees. It has been observed from both the figures that 87BGAP operates properly as the locus of operating points of the faulted phase(s) moves into the operating region.

3.4.2 External faults

Transient frequency-based busbar protection schemes may maloperate for faults with small inception angle. Hence, to validate 87BGAP for external faults with small inception angles, A-G and AB-G faults with FIA 0 and 5 degrees are simulated on line-3. Fig. 3.6 (a) and (b) show the responses during the aforementioned two faults. It is to be observed that all the operating points lie close to the stable point (-1, 0).

Furthermore, in order to test the robustness of the scheme for close-in external faults, AB-G and ABC-G faults are simulated on line-3 at a distance of 100 m and 5 m from the busbar. As seen from the responses shown in Fig. 3.6 (c) and (d), the operating points lie very close to the point (-1,0). Hence, it can be proved that the proposed GAP based scheme remains stable in case of close-in external faults.

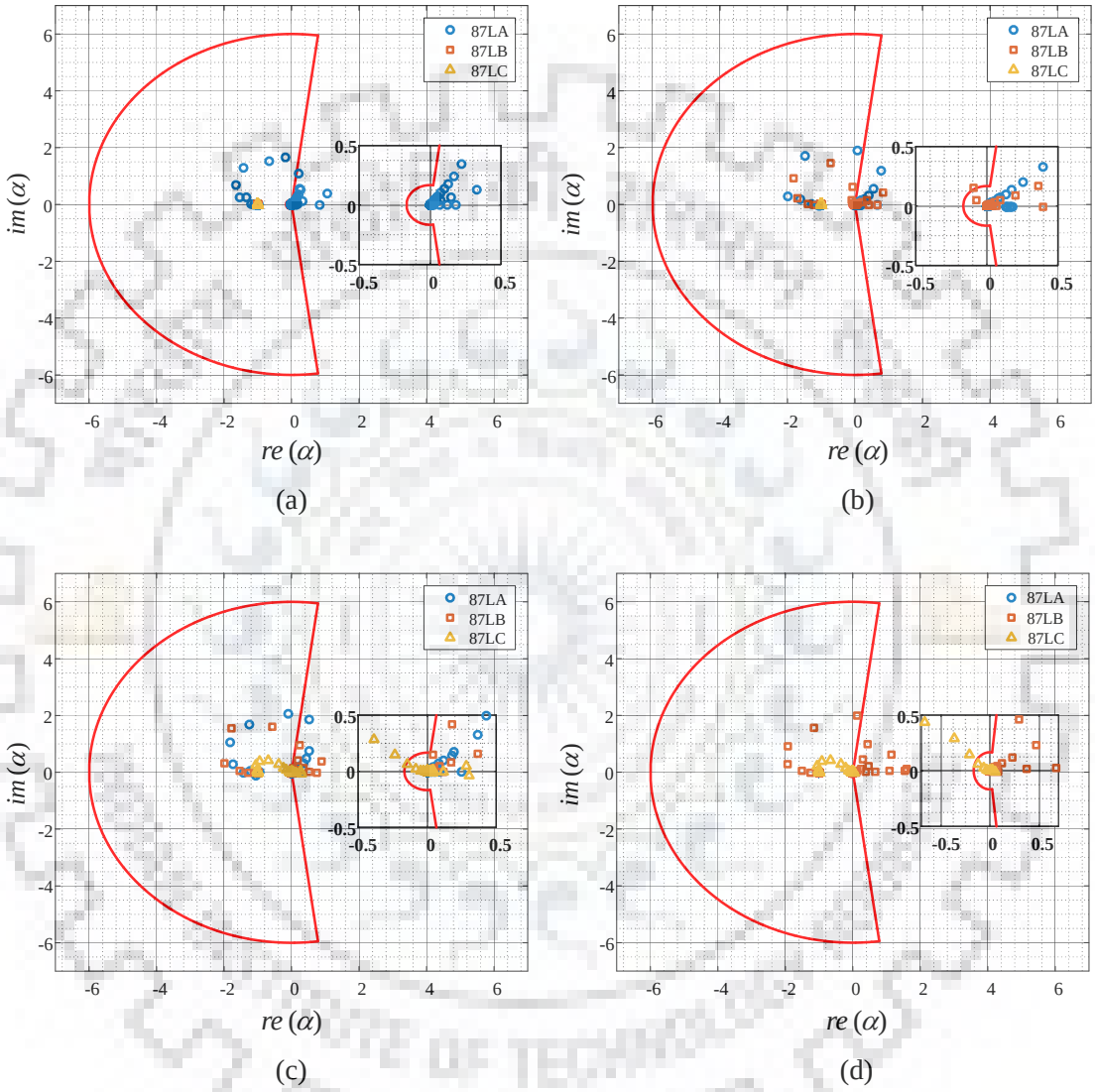

Fig. 3.5: Proposed GAP based relay responses for: (a) L-G (A-G) internal fault with R_F=15 Ω, (b) LL-G (AB-G) internal fault with R_F=100 Ω, (c) LLL-G (ABC-G) internal fault with FIA=0°, (d) LL (BC) internal fault with FIA=0°.

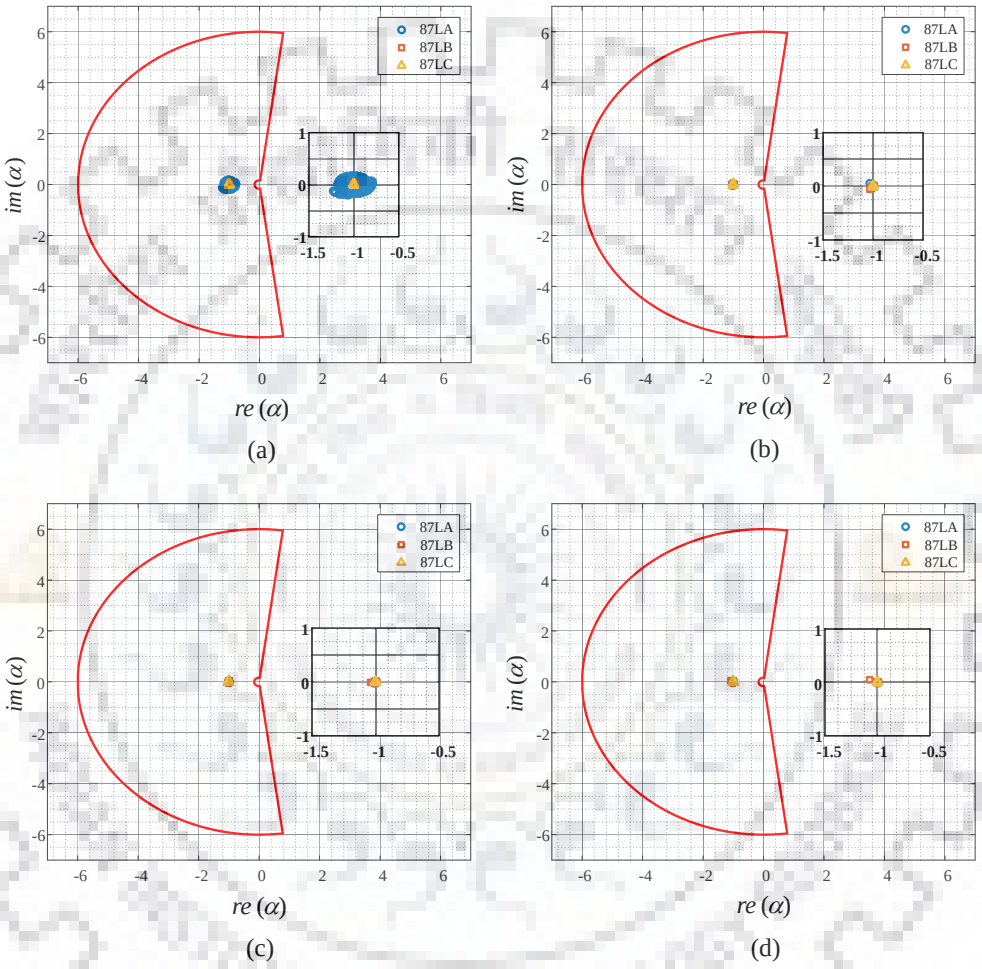

Fig. 3.6: Proposed GAP based relay responses for (a) L-G (A-G) external fault with FIA=0°(b) LL (AB) external fault with FIA=5°(c) LL-G (AB-G) external fault at a distance of 100 m from busbar (d) LLL-G (ABC-G) external fault at a distance of 5 m from busbar.

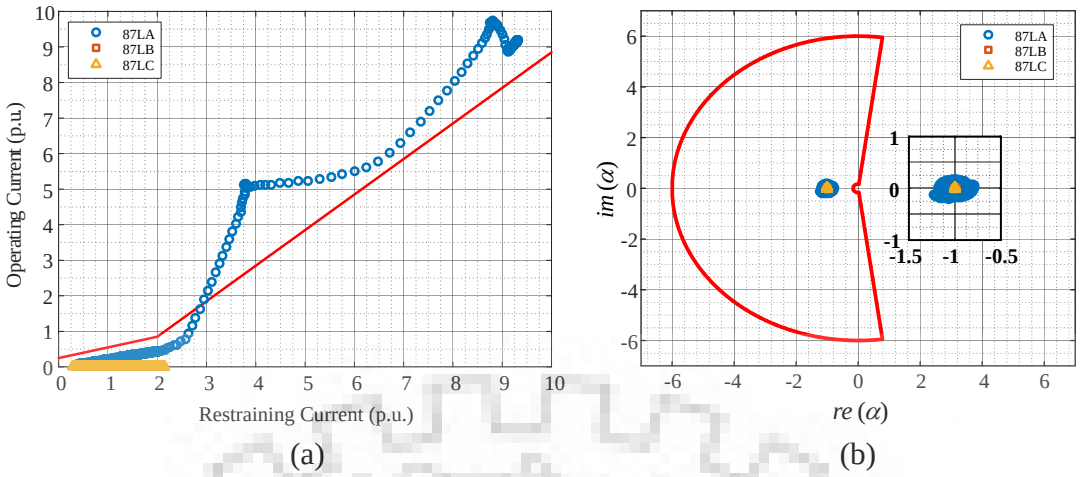

Fig. 3.7: Response in case of the CT saturation condition: (a) Conventional dual-slope differential protection scheme, (b) Proposed GAP-based protection scheme.

3.4.3 Comparison with conventional differential protection

As most of the current-based differential protection schemes are prone to mal-operation in the case of CT saturation, stability against extreme cases of CT saturation is of paramount importance. In order to compare the performance of the traditional busbar differential protection scheme with the proposed GAP-based scheme, an LG (AG) fault is simulated on line 3. In order to replicate the CT saturation condition, the secondary burden resistance of the CT has been increased from its nominal value of 0.5 to 10 Ω. The response of the conventional dual-slope differential protection scheme and the proposed GAP-based scheme for the above-mentioned condition has been illustrated in Fig. 3.7. It is to be observed from Fig. 3.7 that the locus of the operating points of the faulted phase (87LA) moves into the operating region for the convention dual-slope differential protection scheme. However, they remain within the restraining region for the proposed GAP-based scheme. Furthermore, it is to be noted that the margin of safety is very high and 87BGAP may not maloperate for a higher degrees of saturation. The presented scheme remains immune to the effects of CT saturation as the phasor of the output equivalent current has been aligned with the direction of external fault without CT saturation.

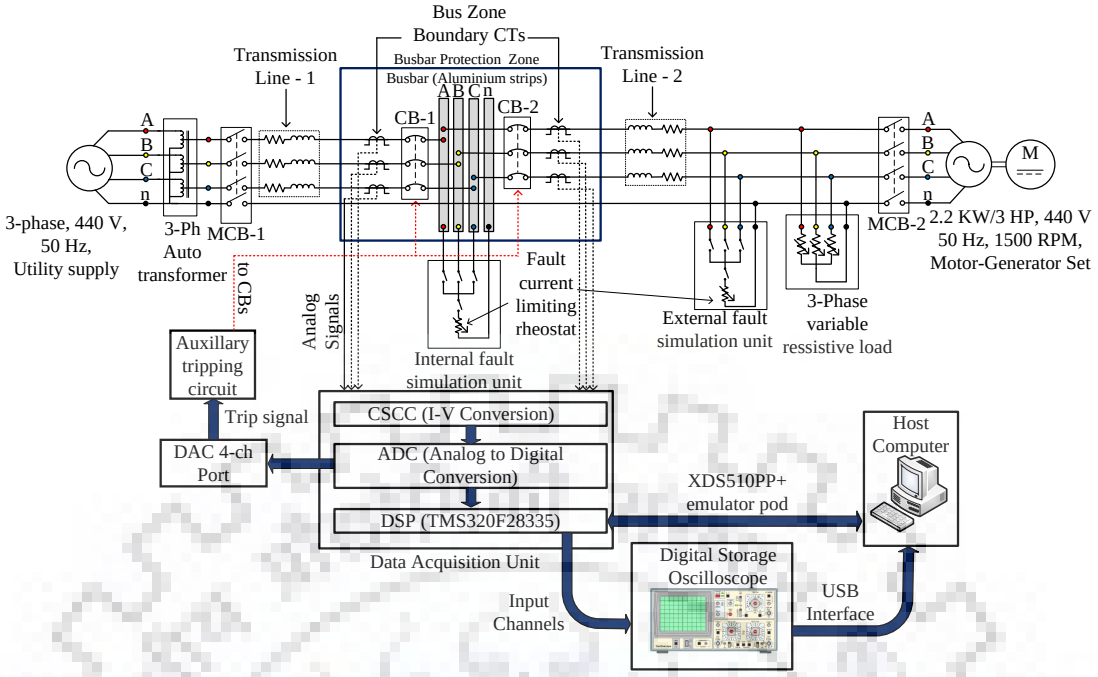

Fig. 3.8: Developed laboratory prototype.

3.5 Hardware implementation

3.5.1 Development of laboratory experimental setup

In order to authenticate the validity of 87BGAP, a prototype of the busbar protection scheme, as shown in Fig. 3.8, has been developed in the laboratory. In this prototype, the utility supply (440 V, three-phase, 50 Hz) and a motor-generator set (2.2 kW/3 hp, 440 V, 50 Hz) have been used to energize the circuit. These two supplies are synchronized using the auto-synchronizing device and phase sequence meter. The busbar and CBs have been replicated by aluminum strips and contactors, respectively. A three-phase auto-transformer has been utilized to control the utility supply. In order to simulate internal and external faults, toggle switches with current limiting resistors are used. The value of fault resistance has been varied between 25 Ω to 45 Ω. Due to practical limitations, solid faults ($R_F = 0$ Ω) have not been simulated using the developed laboratory prototype. Six CTs (10/5 A, 25 VA) have been used to reduce the current level and also to isolate the power circuit from the control circuit.

As shown in Fig. 3.8, CT secondary signals are acquired by the 12-bit ADC of the DSP processor (TMS320F28335) through the Current Sensor Signal Conditioning Circuit (CSSCC). These signals are acquired with a sampling frequency of 4 kHz for the

fundamental frequency of 50 Hz. As the ADC receives only voltage signals, the CSSCC unit converts the current signals into equivalent voltage signals. Moreover, it also scales down and isolates the level of signal prior to the ADC. Using this unit, CT secondary signal is converted into an equivalent 3V peak-to-peak voltage signal. The DSP unit is interfaced with a host computer (Intel Core i7 processor 4 GHz clock frequency, 16 GB RAM) through a bidirectional XDS510PP+ emulator pod. The host computer is supported with Code Composer Studio (CCS v5.1), which interfaces the DSP with MATLAB for execution of the code. The proposed GAP algorithm has been written in MATLAB 2014b and compiled/executed with CCS v5.1. A trip signal, generated by the proposed GAP algorithm during an internal fault, is given to the DAC port (5V). This port generates the final tripping command to the contactors through an auxiliary circuit.

3.5.2 experimental setup results

The authenticity of the proposed algorithm has been tested by simulating various types of internal and external faults on the developed laboratory prototype. A single line to ground fault on busbar (A-G) has been simulated with $R_F = 25\ \Omega$. In this situation, waveforms of CT secondary currents (converted into an equivalent voltage signal by CSSCC unit) are recorded in the host computer through a high resolution (12-bit vertical resolution with sampling rate of 1 GS/sec) DSO and the same are also shown in Fig. 3.9 (a). For the above mentioned internal fault, the response of 87BGAP is shown in Fig. 3.9 (b). It is to be noted from Fig. 3.9 (b) that, initially during the pre-fault condition, the locus of the operating point is very close to the stable point (-1, 0). However, with the inception of an internal fault on the busbar, it moves away from the point (-1, 0) and enters the operating region.

Furthermore, an external fault (A-G) is simulated on an outgoing transmission line. At the same time, the burden of the CT of A-phase of the outgoing transmission line has been increased to replicate the CT saturation condition. Fig. 3.9 (c) shows the recorded waveforms of CT secondary currents of A-phase of incoming and outgoing transmission lines. It has been observed from Fig. 3.9 (c) that the waveform of CT secondary current of phase A of outgoing transmission line has been distorted due to saturation of CT, whereas the waveform of CT secondary current of phase A of the

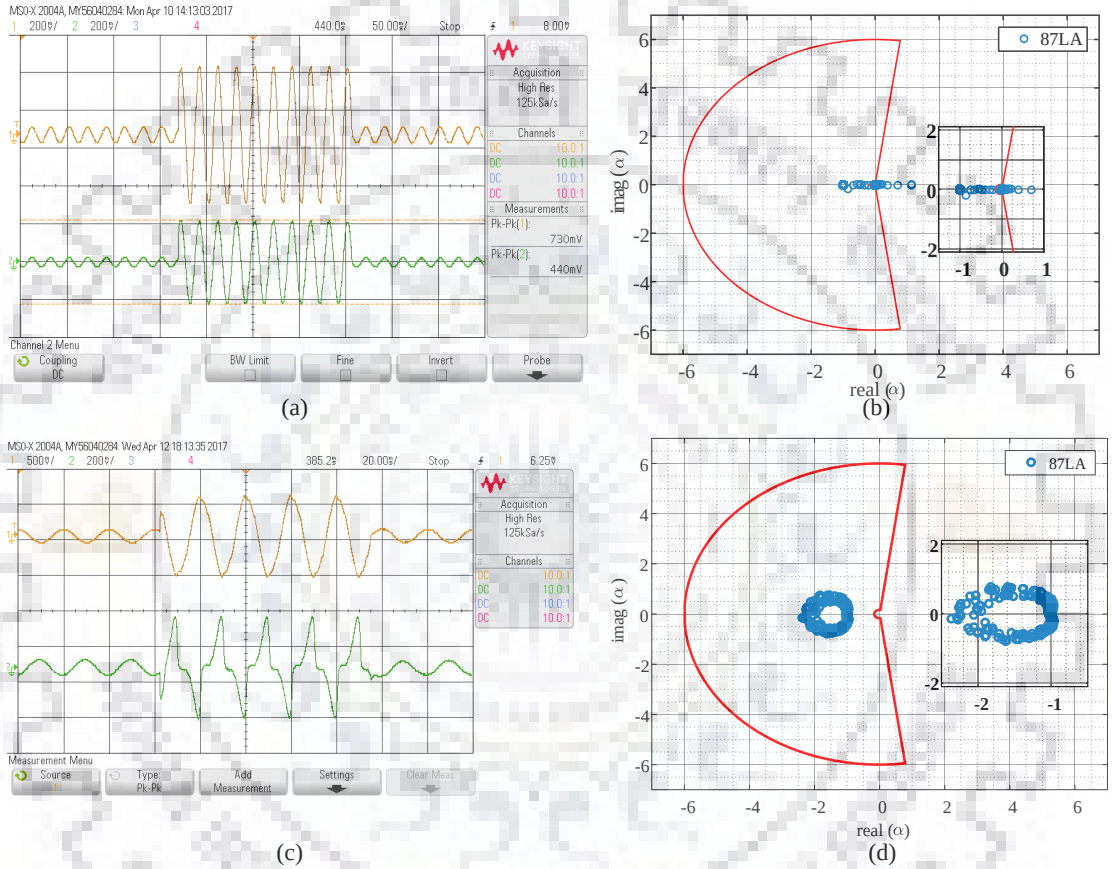

Fig. 3.9: experimental setup results for L-G faults: (a) Current waveforms seen on DSO for an internal A-G fault, (b) GAP based relay response for the internal A-G fault, (c) Current waveforms seen on DSO for an external A-G fault with CT saturation, (d) GAP based Relay response for the external A-G fault with CT saturation.

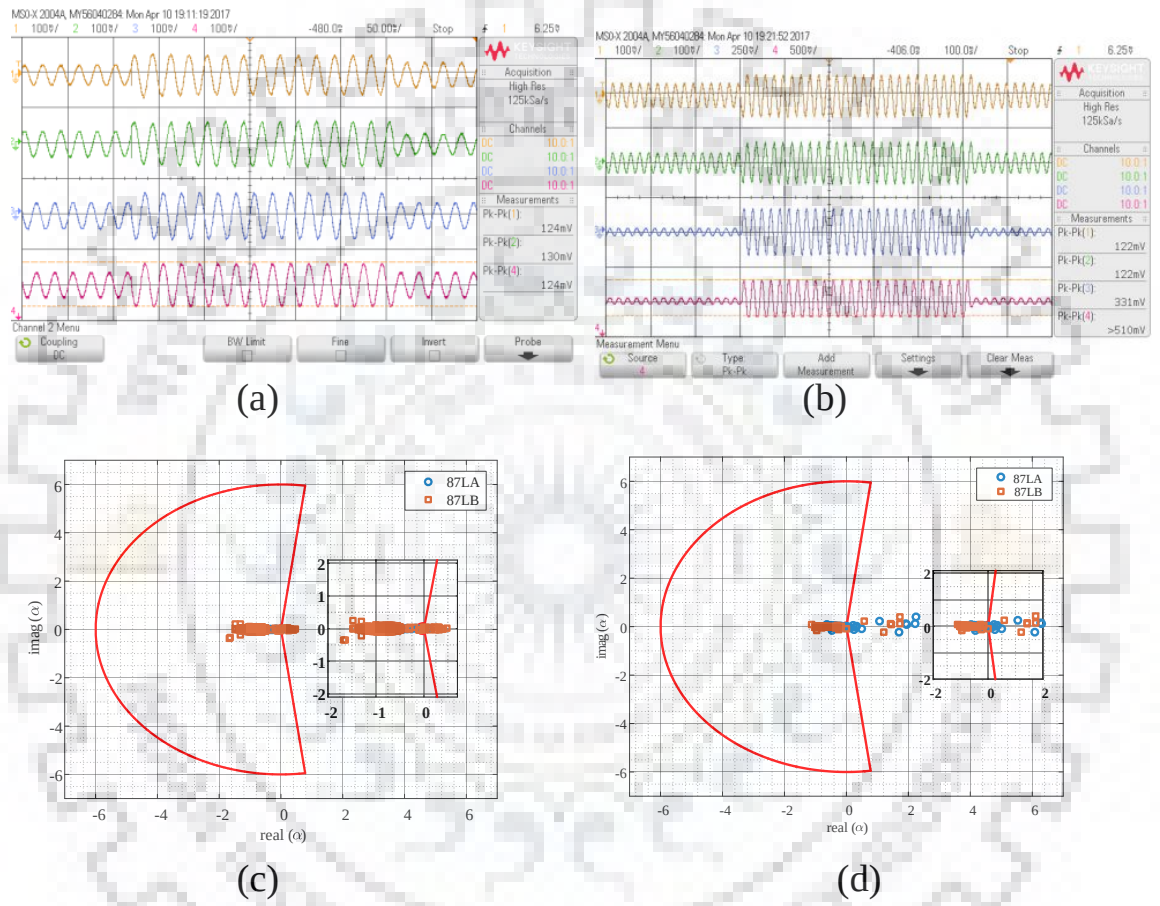

Fig. 3.10: experimental setup results for LL and LL-G faults: (a) Current waveforms obtained on the DSO for AB internal fault, (b) Current waveforms obtained on the DSO for AB-G internal fault, (c) GAP based Relay response for the internal AB fault, (d) GAP based Relay response for the internal AB-G fault.

incoming transmission line is almost sinusoidal in nature. The response of the proposed algorithm during the said situation is shown in Fig. 3.9 (d). It is observed from Fig. 3.9 (d) that the locus of operating point deviates from the stable point (-1, 0). However, it remains within the restraining region. Hence, the proposed algorithm is found to be stable during external fault with CT saturation condition. Likewise, two different types of internal faults (AB and AB-G) have been simulated on the busbar by the internal fault simulation unit. The CT secondary current waveforms of both the phases (A and B) of incoming and outgoing transmission lines for the aforementioned fault scenarios are shown in Figs. 3.10 (a) and (b), respectively. The response of 87BGAP in the case of AB and AB-G internal busbar faults is shown in Figs. 3.10 (c) and (d), respectively. It is to be observed from both figures that the locus of operating points of the faulted phase remains close to the point (-1, 0) during pre-fault conditions. However, with the inception of fault, it moves into the operating region.

3.6 Fault detection time

The fault detection time of 87BGAP depends on the following parameters:

3.6.1 Phasor computation time

The full cycle MDFT algorithm has been used by 87BGAP for the phasor computation of current signals. This requires $(N + 3)$ samples where N is the number of samples/cycle. Therefore, considering 4 kHz as the sampling frequency, the phasor computation time is of the order of 20.75 ms (20 ms + 0.75 ms).

3.6.2 Relay response time

The response time of 87BGAP depends on the number of samples between the instance of fault inception and the instance when the relay response moves from the restraining region to the operating region. These numbers of samples are then multiplied by the sampling period (0.25 ms).

In order to calculate the response time of 87BGAP, AG internal fault on busbar with $R_F = 30\ \Omega$ has been simulated on the laboratory prototype as well as in PSCAD

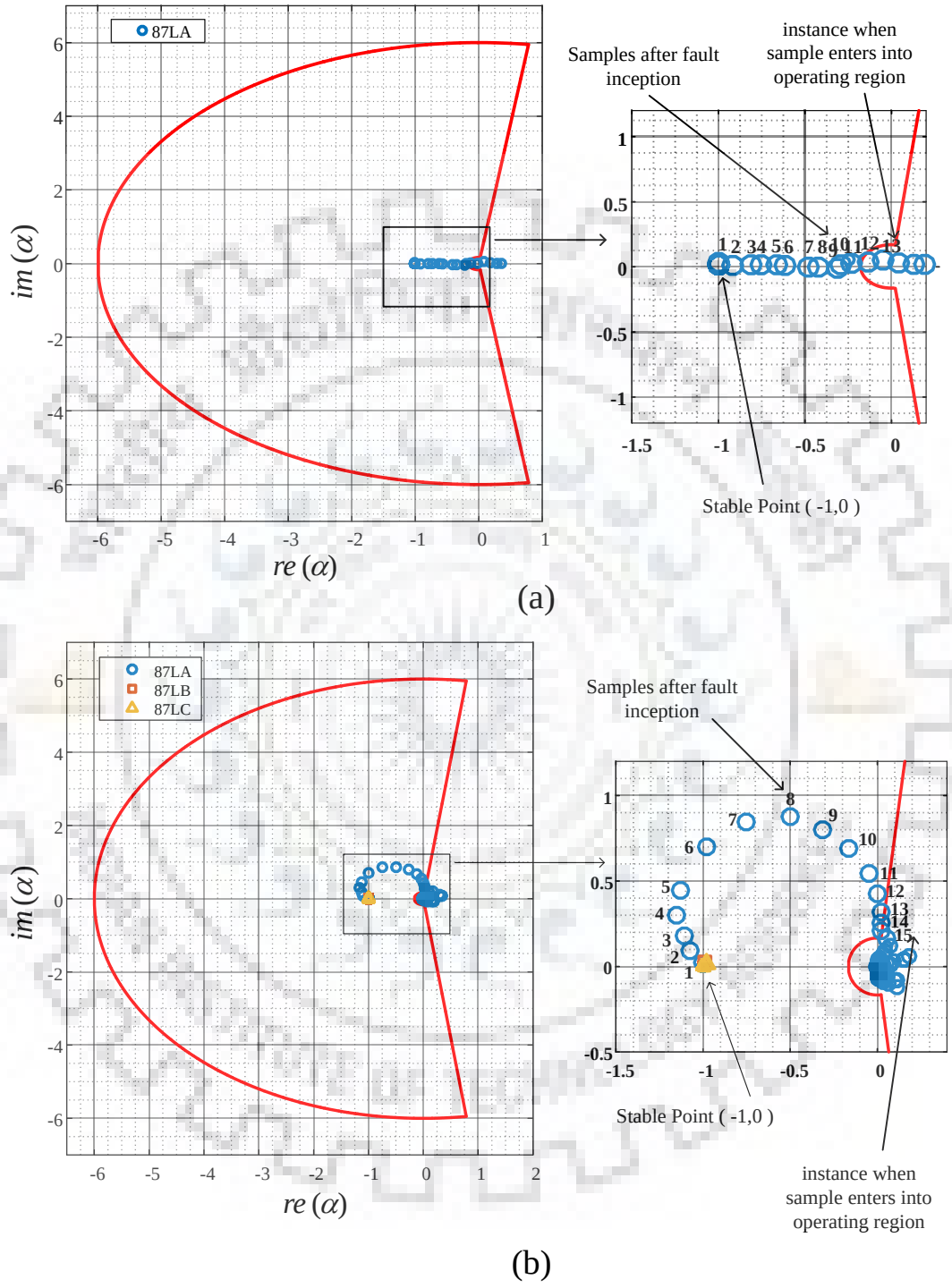

Fig. 3.11: Results obtained from: (a) The laboratory experimental setup, (b) PSCAD simulations.

software. The response of 87BGAP based on data obtained from the laboratory prototype and the PSCAD software is shown in Figs. 3.11 (a) and (b), respectively. It can be observed from both the figures that the locus of operating point lies on the stable point (-1, 0) during pre-fault condition and moves into the operating region consequently after the inception of the fault. However, it is to be noted from Fig. 3.11 (a) that the locus of operating point moves along with the real axis for the data obtained from the laboratory prototype. Conversely, as observed in Fig. 3.11 (b), the locus of operating point moves from the stable point (-1, 0) towards the operating region in a curved path for the data obtained from the PSCAD software. This is due to the fact that the three-phase resistive load has been utilised in case of laboratory prototype, whereas three-phase resistive-inductive load is used for simulation data obtained from PSCAD software.

3.6.3 Program execution time

The processing speed of the host computer is 0.25 μs (1/4 GHz) and the size of the set of instructions is 5 kb. Hence, the program execution time is in the order of 1.25 ms (0.25 μs $\times$ 5 kb).

3.6.4 Propagation delay

Propagation delay due to the data acquisition unit (due to current sensing, current to voltage conversion, ADC, etc.) is of the order of 0.5 ms. Hence, the fault detection time is calculated as per the followings:

$$\begin{aligned} \text{fault detection time} &= \text{phasor computation time (20.75 ms)} \\ &\quad + \text{relay response time (5 ms)} + \text{propagation delay (0.5 ms)} \\ &\quad + \text{program execution time (1.25 ms)} \\ &\quad = 27.5 \text{ ms} \end{aligned} \tag{3.14}$$

Therefore, the total fault detection time (27.5 ms) remains within one-and-half cycle, i.e. $<$ 30 ms which is a mandatory requirement as demanded by some of the

utilities.

3.7 Conclusion

In this chapter, a busbar protection scheme based on GAP has been presented. The proposed algorithm uses one cycle CT secondary current signals of the bays connected to the busbar to map them into the alpha plane. The proposed scheme has been tested on a large number of fault scenarios and the operating points on the alpha plane is found to be close to the stable point (-1, 0) in the case of normal/through-fault conditions. Conversely, it moves out of the stable point (-1, 0) and enters the operating region in case of internal busbar faults. The proposed algorithm has also been validated on data obtained from the laboratory prototype of the busbar protection scheme. It has been observed that the presented scheme yields higher sensitivity during internal busbar faults and better stability in case of external fault with CT saturation condition. Moreover, it is found that the proposed GAP based busbar protection scheme is on par with conventional protection schemes in terms of operating time.

Chapter 4

Initial Travelling Wavefront based Bus Zone Protection Scheme

The previous chapter presents an improved approach to busbar differential protection with Generalised Alpha Plane concept. The scheme shows improved characteristics particularly in case of CT saturation scenarios. It possesses very high potential of on-chip implementation because of simpler numerical calculations with existing hardware. However, the operating time is relatively higher because of the phasor requirement of each phase currents. In the current chapter, development of a high-speed busbar protection scheme (87BITW) based on the appearance of initial travelling waves has been discussed. The performance and responsiveness with communication and computational requirements are showcased.

4.1 Introduction

Due to the connection point of several sub-station devices, busbar is one of the most critical elements in a power system network. Occurrence of a fault on the busbar may cause disconnection of all incoming and outgoing lines connected to the busbar. In large substations, busbar protection zone is usually divided into multiple zones [3, 37]. Therefore, implementing busbar protection has been one of the difficult aspects in power system protection. In order to achieve reliable protection of the busbar, it is necessary to consider several aspects such as tripping time, stability and sensitivity. High-speed tripping during bus fault is one of the most important requirements of

busbar protection as it limits the widespread damage. In order to speed up fault clearance, the present practice is to reduce tripping time of the relay rather than developing new arc extinction methods for CBs [68–70].

This chapter presents a new busbar protection scheme based on the appearance of initial travelling wavefronts at the CT locations in all lines connected to the busbar. The proposed algorithm clearly distinguishes between internal and external faults by comparing the polarity and magnitude of initial WTMMs appearing after fault inception. Therefore, instead of comparing the voluminous instantaneous current data, only the initial WTMMs need to be compared, which significantly reduces the computational burden on the protection unit. As the proposed scheme requires only current data, the issue of high sampling limitations in CCVTs can be avoided. Close-in faults are effectively identified by the proposed scheme due to the high magnitude of current TWs rather than small magnitude of voltage TWs as observed in the case of previously proposed schemes [44, 47]. HIFs are also effectively localized by the proposed scheme.

4.2 State-of-the-art

Based on the frequency components used in relay algorithms, busbar protection schemes can be broadly classified into two categories. The first category comprises schemes based on power frequency components. Since conventional busbar protection schemes are prone to CT saturation, most of the practical busbar schemes need phasor computation, which adds significant time delay in fault clearance. Directional protection schemes [20–22] are based on superimposed impedance and hence, require both acquisition and synchronization of current and voltage data as per IEC-61850 protocol. This, in turn, increases financial burden and decreases reliability. Moreover, synchronization of current and voltage data is a major challenge as high-speed sampling is not feasible with CCVTs. Furthermore, the reliability of these schemes is further marginalized if the number of lines connected to the busbar is very high. Generally, 87B is the widely adopted busbar protection scheme for EHV/UHV substations [16, 33]. However, these schemes are not fully immune to CT saturation problems. In such scenarios, the magnitude of secondary current of the saturated CT is reduced and phase angle is advanced. This develops a fictitious differential current subsequently leading to mal-operation. A

busbar protection scheme using partial differential current has been presented in [83]. Though it effectively counters CT saturation effect, it significantly reduces the sensitivity during high-impedance faults.

The second category of protection schemes are based on transient frequency components. As these schemes are based on instantaneous voltage/current, their tripping speed is significantly higher. The scheme reported in [43] provides a reliable solution by utilizing the polarities of superimposed current at the relay location of all the lines connected to the busbar. As the magnitude of fault current is very small in case of HIFs, it is difficult to identify the fault based on superimposed current. Hybrid approaches such as ANN-fuzzy [52] and wavelet-ANN [54] have been presented for busbar protection. Though they produce very high classification accuracy, a large number of neurons are required for a tedious training process. Moreover, any change in busbar architecture requires retraining of the algorithms. In the past, machine learning-based schemes for busbar protection [55, 57–60] have been presented. Though these schemes provide high classification accuracy for diversified fault scenarios, it would be difficult to achieve probabilistic predictions because of the abrupt behaviour of the kernel or cost functions. Moreover, on-chip implementation of the complex algorithms introduces enormous difficulties. Busbar protection schemes based on alienation coefficients have been proposed in [61, 62]. As these schemes work on the static equivalent model of the busbar, any dynamic changes in busbar configuration make them infeasible.

The TW-based scheme presented in [44] provides real-time high-speed protection. As the fault is identified before the starting of CT saturation, the mal-operation in these cases can be avoided. However, faults occurring at a close-in distance from busbar could not be detected as it practically results in zero voltage across the faulted phase(s). WT-based schemes [36, 46–49] have been presented by researchers, which extracts a great deal of information about the fault characteristics from the transient components. However, these schemes are vulnerable to noise present in the high frequency sampled data. Moreover, the computational burden on the communication channel is very high as they require instantaneous data to be communicated with a very high frequency. A centralized busbar and line protection scheme has been presented in [84]. It requires both synchronized voltage and current measurements. Hence, the reliability decreases whereas computational requirements increase.

4.3 Basic Principles

4.3.1 Initial TWs in Busbar Protection

A fault in the power system is equivalent to the addition of a superimposed voltage source at the fault point [85]. Due to this additional voltage source, TWs are generated from the fault point and propagate towards the line ends. The pre-fault voltage at the fault point $v_{pf}(t)$ can be written as:

$$v_{pf}(t) = V_{pf} \sin(\omega t + \phi) \tag{4.1}$$

where, V_{pf} is the amplitude and ϕ is the initial phase shift. Then, the voltage of the additional source at the fault instance (v_f) is given as,

$$v_f(t) = -v_{pf}(t) = -V_{pf} \sin(\omega t + \phi + \varphi) \tag{4.2}$$

where φ is the fault inception angle. It is worth mentioning that the polarity of the additional voltage source depends on the fault inception instant. If the fault occurs during the positive half cycle (0° to 180°), then the additional voltage source is of negative polarity. On the contrary, if the fault occurs during the negative half cycle (180° to 360°), the additional voltage source is of positive polarity. Due to the additional voltage source, a superimposed current (ΔI_f) is induced in the lines in the form of current TWs.

Fig. 4.1 (a) depicts the single phase representation of a substation network whereas Figs. 4.1 (b) and (c) show the superimposed circuits in case of internal and external faults, respectively. The current direction, from the busbar towards the lines, has been considered as the reference direction in all CTs. With reference to the Fig. 4.1 (b), in case of an internal busbar fault, the initial TWs at the CT location of all connected lines ($l_1 \sim l_n$) are given by,

$$\Delta I_{fi}(t) = \frac{-v_{pf}(t)}{Z_i} = \frac{-V_{pf} \sin(\omega t + \phi + \varphi)}{Z_i} \tag{4.3}$$

where, Z_i is the impedance of the transmission line l_i ($i = 1 \ldots n$) seen from the CT position. Hence, it can be concluded from equation (4.3) that the initial TWs appearing at the CT locations are of same polarity for an internal busbar fault.

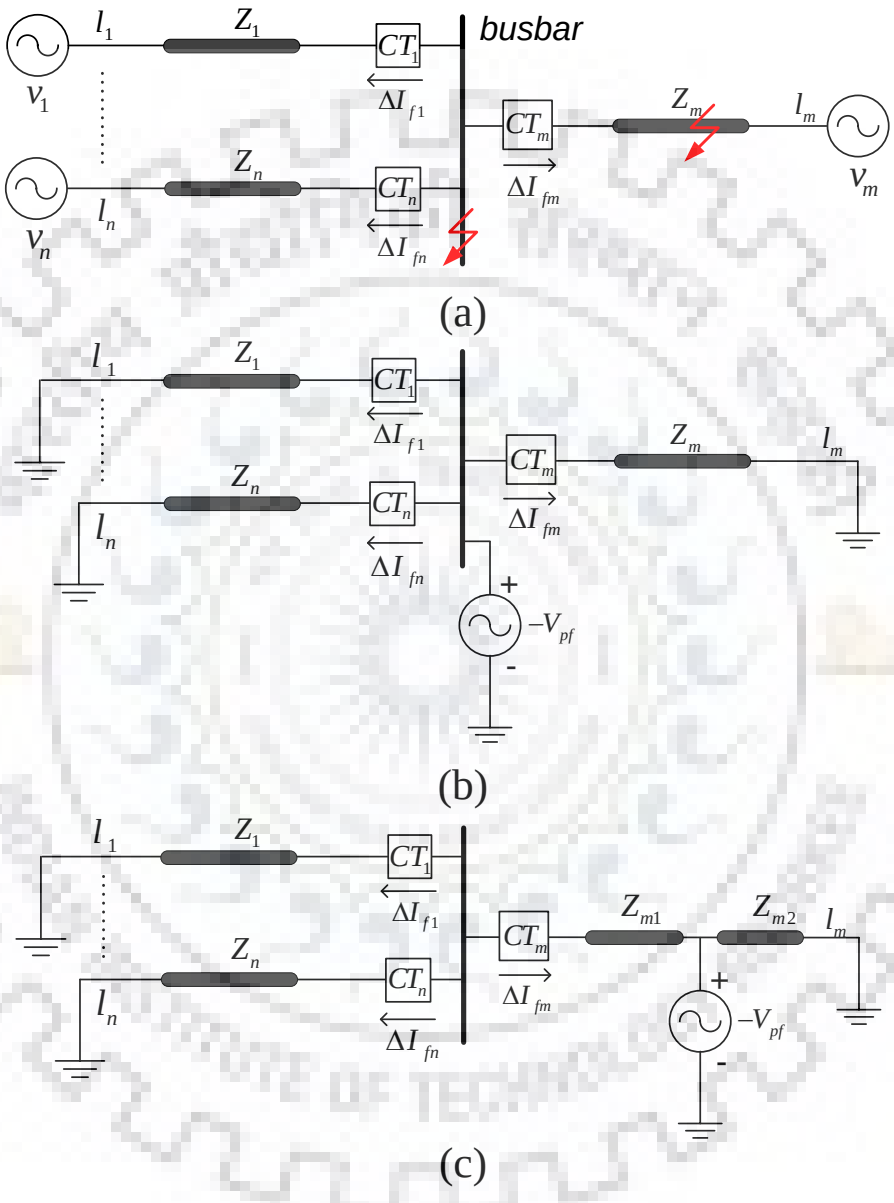

Fig. 4.1: (a) Single line diagram of a power system network. Superimposed circuits during (b) internal fault, (c) external fault.

The superimposed circuit for an external fault on line l_m is shown in Fig. 4.1 (c). Let Z_{m1} be the impedance between the fault point and busbar and Z_{m2} is that of rest of the line. The initial TW observed at the CT location of line l_m is given by,

$$\Delta I_{fm}(t) = -\left(\frac{-v_{pf}(t)}{Z_{t(m)} + Z_{m1}}\right) = \frac{V_{pf}\sin(\omega t + \phi + \varphi)}{Z_{t(m)} + Z_{m1}} \tag{4.4}$$

where,

$$Z_t(m) = Z_1//Z_2//\ldots Z_k\ldots//Z_n; k \neq m \tag{4.5}$$

The symbol // denotes the parallel combination of impedances. The negative sign implies that the direction of ΔI_{fm} is opposite to the reference direction as shown in Fig. 4.1 (c).

The initial TWs in all other lines can be written as per following equation:

$$\begin{aligned}\Delta I_{fi;i\neq m}(t) =& \frac{-v_{pf}(t)}{Z_{t(m)} + Z_{m1}} \times \frac{Z_{t(m,j)}}{Z_{t(m)}} \\ =& \frac{-V_{pf}\sin(\omega t + \phi + \varphi)}{Z_{t(m)} + Z_{m1}} \times \frac{Z_{t(m,j)}}{Z_{t(m)}}\end{aligned} \tag{4.6}$$

Hence, it is evident from equations (4.4) and (4.6) that polarity of the initial TW of the faulted line (l_m) is opposite to that of all other lines ($l_1 \sim l_n$) connected to the busbar.

4.3.2 Karenbauer Phase-Modal Transformation

The discussions in the previous sub-section are based on single phase analysis. However, because of the mutual inductance effect in transmission lines, a fault on any of the phases influences the measurements of healthy phases which in turn negatively affects the faulted phase identification logic. Hence, in order to decouple the phase values, Karenbauer phase-modal transformation, as given in equation (4.7), has been used in this work. This transformation treats each mode as an independent single phase

system [86] .

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_\gamma \\ i_0 \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{4.7}$$

where i_α, i_β, i_γ, and i_0 are the α, β, γ, and 0 modal currents, respectively. i_a, i_b, and i_c are the instantaneous current values of phase a, b, and c, respectively. The coefficients of the transformation matrix are real numbers and the phase-modal transformation is based on instantaneous values of current. This suits the ideal requirement of TW-based relays as necessity of phasor computation of line currents can be eluded.

4.3.3 Wavelet Transform Modulus Maxima

As TWs generated because of faults are the superimposed components hidden in the post fault signals, these high-frequency components can effectively be extracted both in time and frequency domain with good localization characteristics. The requirement of high operating speed rules out the use of continues wavelet transform (CWT) in protection equipment because of higher computational requirements. On the contrary, because of the dyadic nature, discrete wavelet transform (DWT) is better suited for discontinuity detection such as TWs. Due to the multi-resolution analysis, the signal is divided into multiple frequency bands and the components are matched to their scale [87, 88]. However, as the signal is decimated by a factor 2 in every scale [89], the real-time application of DWT for fault analysis is scarcely affected. For example, when WT is applied to current signals of multiple lines, wavelet coefficients must be compared with each other without any time shift. Hence, a time-invariant WT is more suitable for fault analysis. The Maximum Overlap Discrete Wavelet Transform (MODWT) is a modified version of DWT which is time-invariant and does not require downsampling by a factor 2. This facilitates the real-time analysis of fault components with faster computations [90]. Hence, MODWT has been utilized in the present work to calculate the WTMMs. In order to detect the singularity or discontinuity points, the wavelet coefficients are preferred over the scaling coefficients as variations are faster in the high-frequency part when compared to the low-frequency part.

The wavelet coefficients (w) of a current signal i_p at k^{th} sample for the scale j can

be calculated as follows:

$$w_j(k) = \sum_{l=1}^{L_j} \widetilde{h_j}(l) i_p(k - L_j + l) \tag{4.8}$$

where, $\widetilde{h_j}(l) = h_j(l)/2^{j/2}$ are the rescaled coefficients of low and high pass filter at scale j; L_j is the number of filter coefficients at scale j, calculated as follows:

$$L_j = (2^j - 1)(L - 1) + 1 \tag{4.9}$$

where, L is the number of filter coefficients of the mother wavelet.

WTMMs are defined as the local maximas or minimas at a particular scale. In order to calculate the WTMMs, first the difference in wavelet coefficients has been calculated as follows:

$$\Delta w_j(k) = |w_j(k)| - |w_j(k-1)| \tag{4.10}$$

then, $wtmm_j$ is calculated as per the following conditions:

$$wtmm_j(k) = \begin{cases} w_j(k), & \text{if } \Delta w_j(k) > 0 \ \& \ \Delta w_j(k+1) < 0 \\ 0, & \text{otherwise} \end{cases}$$

As WTMMs appear exactly at the same moment when sharp variation in signal magnitude occurs, the time of arrival of wavefronts can effectively be represented. The use of WTMMs instead of the high-frequency current signals significantly reduces the computation and communication burden on the relays.

4.3.4 Selection of mother wavelet and scale of decomposition

One of the major aspects regarding the application of WT is the selection of mother wavelet. This is indeed application-specific and requires prior knowledge of the signal to be analyzed. The followings are the important aspects to be considered when selecting the mother wavelet: a) visual similarity with the original signal b) number of vanishing moments present c) computational requirements d) filter characteristics. The literature on wavelet is rich with the concept that the best results are obtained when the original test signal has the closest visual similarity with the mother wavelet. As discussed

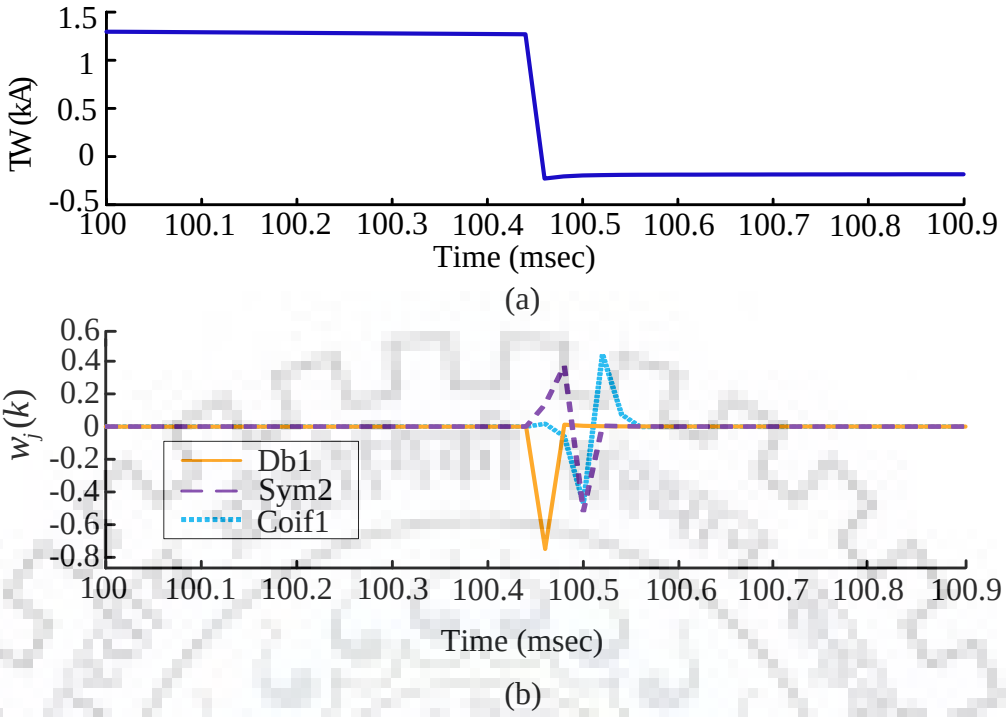

Fig. 4.2: (a) A fault induced TW, (b) corresponding scale-1 coefficients for different mother wavelet.

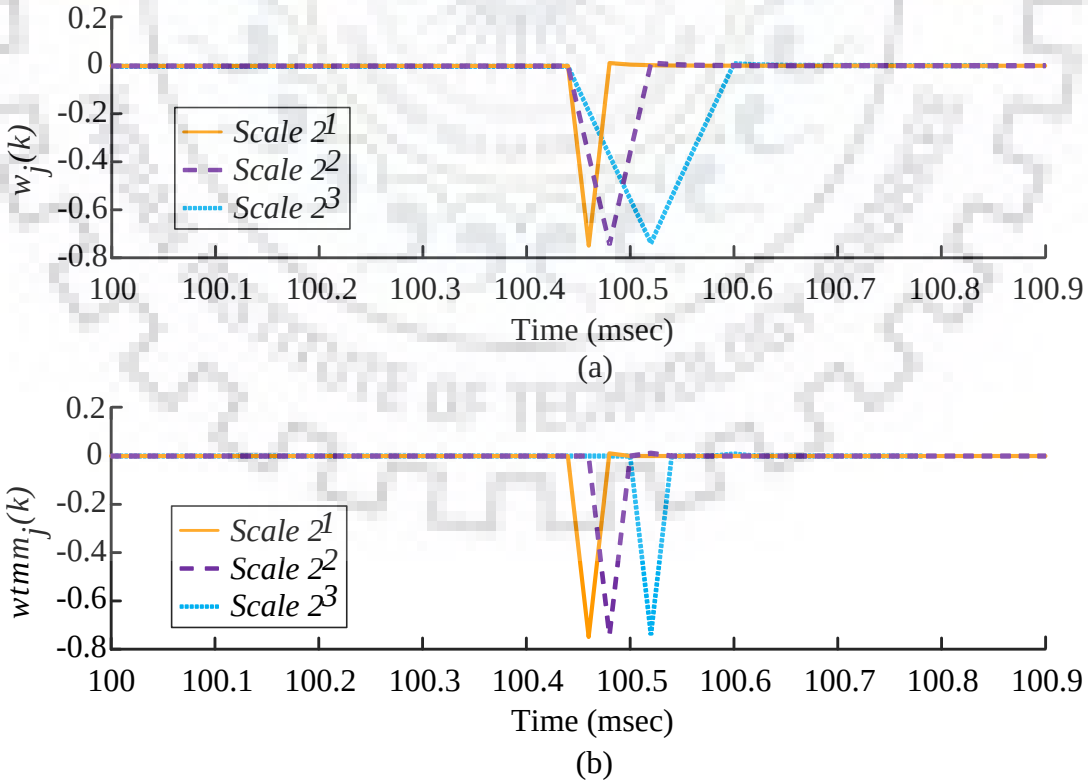

Fig. 4.3: (a) Wavelet coefficients up to scale 2^3 (b) corresponding WTMMs.

previously, fault induced TWs are generated because of a superimposed source at the fault instance. Hence, in HV systems, the current TWs can be regarded as first-order step functions. However, the CTs connected to the lines act as a second-order linear system and damped oscillations are observed at the arrival instant of initial wavefronts. As the polarity of initial wavefronts remains unchanged and steep [91], the correct representation of TWs through WTMMs can be achieved. A visual inspection of different mother wavelets may lead to the conclusion that Db1 (Haar) is the closest representation of a step signal (TW).

It is worth mentioning that in order to detect a discontinuity of order-n, the mother wavelet should have at least $n-1$ vanishing moments. Hence, to detect the initial TWs at the CT secondary, the mother wavelet should have at least one vanishing moments. This also ensures a minimum computational requirement. In order to compare the abilities of different mother wavelets to extract WTMMs, scale-1 wavelet coefficients are calculated with different mother wavelets such as Daubechies(Db), Symlets(Sym), and Coiflets(Coif) with minimum vanishing moments. A fault induced TW along with corresponding scale-1 wavelet coefficients using the aforementioned mother wavelets are shown in Fig. 4.2. It can be observed that out of all the wavelets, Daubechies(Db) is best suited for representing sudden changes such as TWs.

Further, to study the reconstruction abilities of the aforementioned mother wavelets, a typical TW as shown in Fig. 4.2 (a), is reconstructed after scale-3 decomposition. The error signal $e[n]$ is calculated as the difference between the original and reconstructed signal. Then, the L^2-norm of the error signal is expressed as per the following:

$$||e||_2 = \left[\sum_{i=1}^{n} e_i^2\right]^{1/2} \tag{4.11}$$

The error in reconstruction, in the case of different mother wavelets calculated as per the above formula, is given in Table. 4.1. As observed from Table.4.1, Db1 gives the minimum error while reconstructing the signal. Due to the aforementioned advantages, Db1 has been selected as the mother wavelet in this study.

Furthermore, it is to be noted that the wavelet coefficients become smoother as the number of filter coefficients increases. In higher scales, the wavelet becomes less localized in time. Hence, low scale analysis is suitable for detecting wavefronts. In

Table 4.1: Error in reconstruction for different wavelet families

Wavelet family	Order	L^2-norm of error signal
Daubechies (Db)	1	0.1972
	2	1.8050
	3	2.8640
	4	5.3325
Coiflet (Coif)	1	2.7551
	2	3.8803
	3	5.8370
	4	7.7529
Symlets (Sym)	2	0.8258
	3	1.8628
	4	2.8087

this regard, Fig. 4.3 (a) shows the wavelet coefficients up to scale 2^3 using Db1 as the mother wavelet for the TW shown in Fig. 4.2 (a). It can be observed that, as the scale of decomposition increases, the wavelet coefficients become less localized in time (time base increases). This can be visualized from Fig. 4.3 (b) where a WTMM corresponding to scale 2^1 is observed first when compared to scale 2^2 and 2^3. Hence, level-1 decomposition (scale-2^1) has been considered in this study, which saves computational requirements with faster extraction of WTMMs.

4.4 Proposed Busbar Protection Scheme (87BITW)

4.4.1 Simulation Model

The simulation model of an existing 750-kV Indian substation, as shown in Fig. 4.4, has been developed in PSCAD/EMTDC software package [79]. Three generating substations G_1, G_2, and G_3 have been connected to the busbar by transmission lines l_1, l_2, and l_3 each with a physical length of 100 km. The system parameters are given in Appendix-IV.

4.4.2 Selection of sampling frequency

Fig. 4.5 shows the representation of two consecutive wavefronts arriving at instances k_1 and k_2, respectively. MODWT uses a data window of L_j (number of filter coefficients at 2^j scale) for the calculation of wavelet coefficients. In Fig. 4.5, Data window (1)

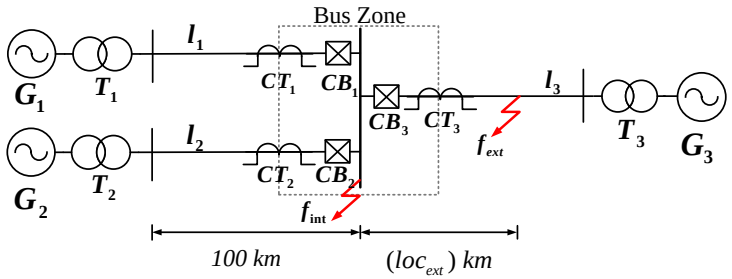

Fig. 4.4: Single line diagram of an existing 750-kV Indian substation.

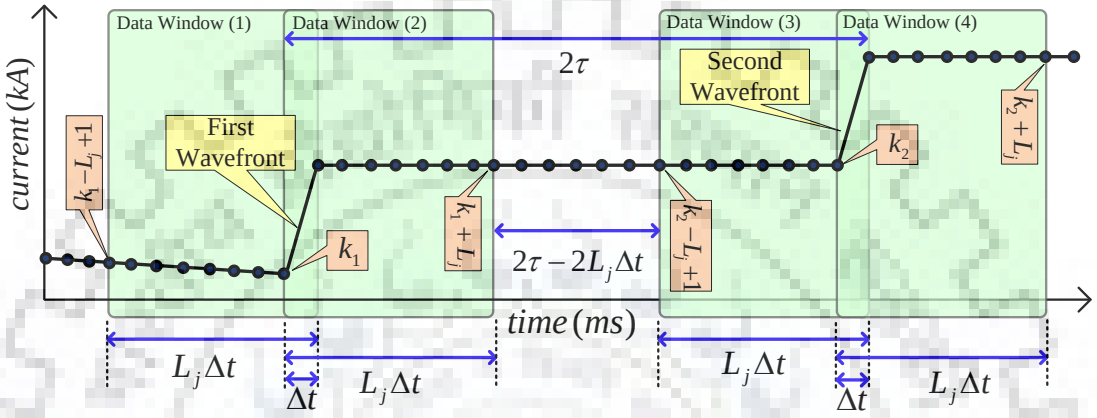

Fig. 4.5: Representation of two consecutive wavefronts and wavelet data windows.

and (2) are the first and last data windows containing the initial wavefront. Likewise, Data window (3) and (4) are the first and last data windows containing the second wavefront. If the propagation time of the smallest line connected to the busbar is τ sec, then the second wavefront appears after 2τ sec. It can be observed from Fig. 4.5 that to avoid the miscalculation in wavelet coefficients, the Data window(2) and (3) should not overlap. Therefore:

$$\begin{aligned} 2\tau - 2L_j\Delta t > 0; \implies 2\tau > 2L_j\Delta t \\ \implies \frac{1}{\Delta t} > \frac{L_j}{\tau}; f_s > \frac{L_j}{\tau} \end{aligned} \tag{4.12}$$

In this study, the smallest line connected to the busbar is 100 km long ($\tau = 0.33$ msec). Hence, as per equation (4.12), the minimum sampling frequency is 6 kHz. Considering a safety margin, a sampling frequency of 8 kHz has been considered.

4.4.3 Fault zone identification

In the case of normal operating conditions, WTMMs are not observed in any of the lines. However, when the magnitudes of WTMMs are greater than a small tolerance value, the polarities of the WTMMs are compared individually for each of the modes (α, β, γ, and 0). Then the fault zone identification is carried out according to the following subroutine:

if $S(wtmm_{1m}) = \cdots = S(wtmm_{nm})$ **then**

The fault is on the busbar.

else if $S(wtmm_{1m}) = \cdots = S(wtmm_{nm}) = -S(wtmm_{fm})$ **then**

The fault is on the line m.

else

No fault condition.

end if

where S represents the polarity of WTMM, n is the total number of lines connected to the busbar, m represents α, β, γ, and 0 modes and f indicates the faulted line. To improve the reliability and nullify the effects of noise, the aforementioned conditions have been checked for all the four modes α, β, γ, and 0. In case, when either of the equations is satisfied for all the modes, the fault location is identified accordingly.

4.4.4 faulted phase identification

4.4.4.1 Motivations from previous literature

While the time localization using WT helps in the detection of a fault, the high-frequency components contain a lot of information about the type of fault. Whenever a fault occurs, high-frequency components are superimposed on fundamental frequency components generating additional information about the type of fault. The transient energy in the current signals produced due to faults can be extracted in the form of Maximum Wavelet Singular Values (MWSV) [92] and Power Spectral Density (PSD) [93]. The greatest energy components in a signal are contained by the MWSV of the wavelet matrix (WM) defined as follows:

$$WM = \begin{bmatrix} w_1(1) & \dots & w_1(n) \\ \vdots & \ddots & \\ w_{L_j}(1) & \dots & w_{L_j}(n) \end{bmatrix} \tag{4.13}$$

where i-th row corresponds to the wavelet coefficients of level-i decomposition.

In [92], the authors have extracted the highest frequency components in the form of MWSV. Each of the faults is reflected in terms of singular values in the respective faulted phase. Thereafter, Euclidean norms have been utilized to find out the threshold values for different types of fault.

Similarly, in [93], PSD values corresponding to the energy components are utilized. They are calculated from the diagonal elements of the covariance matrix as follows:

$$PSD = diag\big[WM \times WM^T\big] \tag{4.14}$$

In a phase-segregated manner, similarities between the probability distribution of the normalized PSD values are compared to that of a reference signal. The threshold for different types of fault in terms of Hellinger distance [94] is based on the general rule that, for a single-phase fault the majority of energy is stored in a particular phase current signal while in case of double or triple phase faults, it is divided between the faulted phases.

As the highest frequency components are most susceptible to any changes in the signal, the faulted phases can be the most efficiently represented by the lower scale detailed coefficients [95]. Hence, a lower scale should be chosen as most of the energy is trapped in the highest frequency band (lowest scale). Analogous to the MWSV in [92] and, PSD in [93], the magnitude of WTMMs can represent the energy contained in the signal time-dilated to the instant of fault inception. This encourages the use of *magnitude* of WTMMs derived from the scale-1 detailed coefficients for fault classification along with *polarity* of WTMMs for fault zone identification as discussed in earlier sections. In this regard, each fault type is reflected in one or more aerial mode WTMMs (α, β, γ). As an additional criterion, a ground fault is reflected in 0-mode WTMMs. While the PSD and MWSV are reflected in terms of phase components, the WTMMs are reflected in terms of aerial mode currents. Hence, to extract the phase information from areal mode WTMMs, boundary conditions for different types

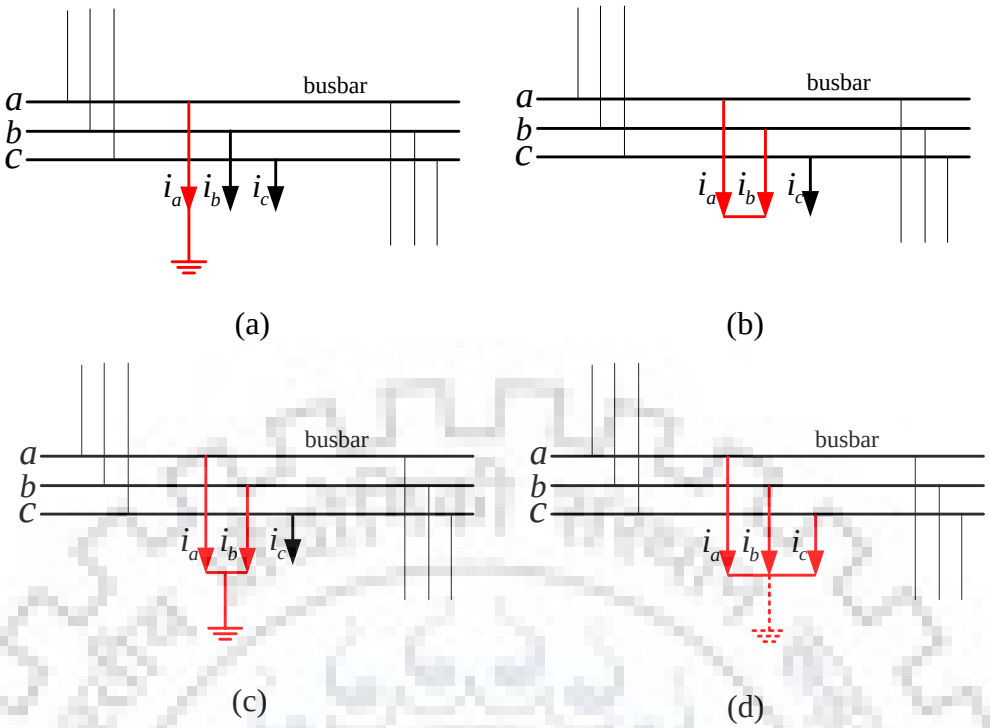

Fig. 4.6: Busbar faults: (a) single line to ground (b) double line (c) double line to ground (d) triple line-(ground)

of fault considering ideal conditions (zero fault resistance) have been derived from the phase-modal transformation.

Fig. 4.6 shows the structural representation of different types of fault on the busbar. The fault classification criteria, as a part of the proposed bus zone fault identification scheme, have been developed based on the boundary conditions in terms of magnitudes of α, β, γ and 0 mode WTMMs.

4.4.4.2 Single line to ground faults

Out of generality, a single line to ground (A-g) fault on busbar has been shown in Fig. 4.6 (a). The boundary condition in terms of instantaneous phase currents is written as:

$$i_b = i_c = 0 \tag{4.15}$$

Then, applying Karenbauers transformation, α, β, γ and 0 mode currents are calculated:

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_\gamma \\ i_0 \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_a \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} i_a \\ i_a \\ 0 \\ i_a \end{bmatrix} \tag{4.16}$$

Similarly, the instantaneous modal boundary conditions for B-g and C-g faults can be calculated.

4.4.4.3 Double line faults

Fig. 4.6 (b) shows a double line (AB) fault on busbar. In this case, the boundary conditions in terms of instantaneous phase currents can be written as:

$$i_a = -i_b; \quad i_c = 0 \tag{4.17}$$

Then, applying Karenbauers transformation, α, β, γ and 0 mode currents can be calculated as:

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_\gamma \\ i_0 \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_a \\ -i_a \\ 0 \end{bmatrix} = \begin{bmatrix} 2i_a \\ i_a \\ -i_a \\ 0 \end{bmatrix} \tag{4.18}$$

Similar analysis can be performed to obtain the instantaneous modal boundary conditions for BC and CA faults.

4.4.4.4 Double line to ground faults

Fig. 4.6 (c) shows a double line to ground (AB-g) fault on busbar. In this case, the boundary condition in terms of instantaneous phase currents is written as:

$$i_c = 0 \tag{4.19}$$

Then, applying Karenbauers transformation, α, β, γ and 0 mode currents can be calculated as:

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_\gamma \\ i_0 \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ 0 \end{bmatrix} = \begin{bmatrix} i_a - i_b \\ i_a \\ i_b \\ i_a + i_b \end{bmatrix} \tag{4.20}$$

Similar analysis can be performed to obtain the instantaneous modal boundary conditions for BC-g and CA-g faults.

4.4.4.5 Triple line-(ground) fault

Practically, triple line and triple line to ground faults are analyzed similarly as both require all three phases to be isolated (supply interruption). To this end, ABC fault has been shown in Fig. 4.6 (d). Neglecting fault resistance, the boundary condition in terms of instantaneous phase currents can be written as:

$$i_a + i_b + i_c = 0 \tag{4.21}$$

Then, applying Karenbauers transformation, the α, β, γ and 0 mode boundary conditions can be written as:

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_\gamma \\ i_0 \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} -(i_b + i_c) \\ -(i_a + i_c) \\ -(i_a + i_b) \end{bmatrix} = \begin{bmatrix} i_a - i_b \\ i_a - i_c \\ i_b - i_c \\ i_a - i_b \end{bmatrix} \tag{4.22}$$

The boundary conditions corresponding to each fault in terms of both phase and modal components are summarized in Table 4.2.

It has been explained in the previous sections that the magnitude of modal currents can be represented by the magnitude of WTMMs. Hence, the criterion corresponding to each fault type has been derived based on the magnitude of WTMMs.

Table 4.2: Boundary conditions in terms of phase and modal currents

Fault type	Boundary conditions	i_α	i_β	i_γ	i_0
Ag	$i_b = i_c = 0$	i_a	i_a	0	i_a
Bg	$i_a = i_c = 0$	-i_b	0	i_b	i_b
Cg	$i_a = i_b = 0$	0	-i_c	-i_c	i_c
AB	i_a=-i_b; $i_c = 0$	$2i_a$	i_a	-i_a	0
BC	i_b=-i_c; $i_a = 0$	-i_b	i_b	$2i_b$	0
AC	i_a=-i_c; $i_b = 0$	-i_c	-$2i_c$	-i_c	0
ABg	i_c=0	i_a-i_b	i_a	i_b	i_a+i_b
BCg	$i_a = 0$	-i_b	i_c	i_b-i_c	i_b+i_c
ACg	$i_b = 0$	i_a	i_a-i_c	-i_c	i_a+i_c
ABC(g)	i_a+i_b+i_c=0	i_a-i_b	i_a-i_c	i_b-i_c	0

4.4.4.6 Detection of grounded faults

As evident from Table 4.2, the involvement of ground in a fault can be effectively identified by the magnitude of 0-mode WTMMs ($wtmm_0$).

$$|wtmm_0| = \begin{cases} 0, & \text{for non-grounded faults} \\ > 0, & \text{for grounded faults} \end{cases}$$

4.4.4.7 Detection of single line to ground faults

It can be verified from Table 4.2 that, in addition to 0-mode, A-g fault is reflected in α and β modes. Then, the criterion can be set as follows:

$$|wtmm_\alpha| - |wtmm_\beta| = 0 \quad \& \quad |wtmm_0| = 0 \tag{4.23}$$

The aforementioned condition is true for the assumption of zero fault resistance. The same has been considered for the derivation of criteria for different faults described in the previous subsection. Considering non-ideal conditions, a tolerance value (ε) is to be set. It is set in terms of the minimum value of WTMM based on a single line to ground faults on the busbar with significant values of fault resistance [92]. The value of ε is set based on both analytic and empirical analysis.

As stated in the previous section, Karenbauer phase-modal transformation decouples the three phase system so that each of three modes can be considered as an independent single phase. In the case of a single line to ground fault on the busbar,

Table 4.3: Selection of tolerance value among different fault scenarios

Case no.	SLG fault scenario R_f (Ω)	FIA ($^\circ$)	Tolerance value (ε) Analytically	simulations
1	50	0.5	0.0617	0.0632
2	100	1	0.0617	0.0652
3	200	2	0.0604	0.0641
4	300	3	0.0692	0.0714
5	400	4	0.0617	0.0632
6	500	5	0.0616	0.0654

the magnitude of WTMM observed at the busbar $wtmm_{b(m)}$ as:

$$wtmm_{b(m)} = \Delta i_f = i_f - 0 = \frac{V_{p(m)} \sin(\omega t + \varphi)}{R_f} \tag{4.24}$$

where, m represents α, β, γ, and 0 modes, $V_{p(m)}$ is the maximum value of voltage of the m-mode, R_f is the fault resistance, and φ is the fault inception angle. As $wtmm_{b(m)}$ is contributed by WTMM of all the lines, ε can be set as per equation (4.25).

$$\varepsilon \leq \frac{1}{n} \cdot \frac{V_{p(m)} \sin(\omega t + \varphi)}{R_f} \tag{4.25}$$

where n is number transmission lines connected to the busbar.

In this chapter, different internal fault scenarios with high fault resistance and low fault inception angle have been simulated. The lowest values of WTMM among all lines for the aforementioned fault scenarios have been considered for the selection of ε. Moreover, ε has also been calculated analytically by equation (4.25) for each of these fault scenarios. Different values of ε obtained from both analytic calculations and simulations are shown in Table 4.3. It is observed from Table 4.3 that the values of WTMMs in lines for the aforementioned fault scenarios remain close to 0.06. Moreover, these results are confirmed by both analytic calculations and simulations. Hence, $\varepsilon = 0.05$ has been set in this study.

Now, the criterion (4.23) is modified as:

$$|wtmm_\alpha| - |wtmm_\beta| < \varepsilon \quad \& \quad |wtmm_0| > \varepsilon \tag{4.26}$$

Similarly, the criteria for B-g and C-g faults are derived.

Table 4.4: Criterion for classification of faults

Fault	Criterion
Ag	$\lvert wtmm_\alpha\rvert - \lvert wtmm_\beta\rvert < \varepsilon$ & $\lvert wtmm_0\rvert > \varepsilon$
Bg	$\lvert wtmm_\alpha\rvert - \lvert wtmm_\gamma\rvert < \varepsilon$ & $\lvert wtmm_0\rvert > \varepsilon$
Cg	$\lvert wtmm_\beta\rvert - \lvert wtmm_\gamma\rvert < \varepsilon$ & $\lvert wtmm_0\rvert > \varepsilon$
AB	$\lvert wtmm_\beta\rvert + \lvert wtmm_\gamma\rvert - \lvert wtmm_\alpha\rvert < \varepsilon$ & $\lvert wtmm_0\rvert < \varepsilon$
BC	$\lvert wtmm_\alpha\rvert + \lvert wtmm_\beta\rvert - \lvert wtmm_\gamma\rvert < \varepsilon$ & $\lvert wtmm_0\rvert < \varepsilon$
AC	$\lvert wtmm_\alpha\rvert + \lvert wtmm_\gamma\rvert - \lvert wtmm_\beta\rvert < \varepsilon$ & $\lvert wtmm_0\rvert < \varepsilon$
ABg	$\lvert wtmm_\beta + wtmm_\gamma\rvert - \lvert wtmm_0\rvert < \varepsilon$ & $\lvert wtmm_0\rvert > \varepsilon$
BCg	$\lvert wtmm_\alpha + wtmm_\gamma\rvert - \lvert wtmm_\beta\rvert < \varepsilon$ & $\lvert wtmm_0\rvert > \varepsilon$
ACg	$\lvert wtmm_\alpha - wtmm_\gamma\rvert - \lvert wtmm_0\rvert < \varepsilon$ & $\lvert wtmm_0\rvert > \varepsilon$
(ABC)g	*Others*

4.4.4.8 Detection of double line faults

As observed form Table 4.2, AB fault is reflected in α, β and γ modes. As ground is not involved, the magnitude of $wtmm_0$ should be 0 in case of ideal or less than the tolerance value (ε) for non-ideal boundary conditions. Considering the magnitude of α, β and γ mode WTMMs, the following criterion is set:

$$|wtmm_\beta| + |wtmm_\gamma| - |wtmm_\alpha| < \varepsilon \quad \& \quad |wtmm_0| < \varepsilon \tag{4.27}$$

Similarly, the criteria for BC and CA faults are established.

4.4.4.9 Detection of Double line to ground faults

Likewise, observing Table 4.2, the criterion for AB-g fault can be derived as follows:

$$|wtmm_\beta + wtmm_\gamma| - |wtmm_0| < \varepsilon \quad \& \quad |wtmm_0| > \varepsilon \tag{4.28}$$

Criteria for BC-g and AC-g faults can be derived in a similar manner. The fault that does not satisfy any of the above criteria is involved with all three phases and (or) ground. Finally, the criterion for each of the faults has been summarized in Table 4.4.

4.4.5 Computational Burden

Fig. 4.7 shows the flow chart of the systematic computation processes in 87BITW. The locations of CTs define the bus zone boundary in both static and dynamic config-

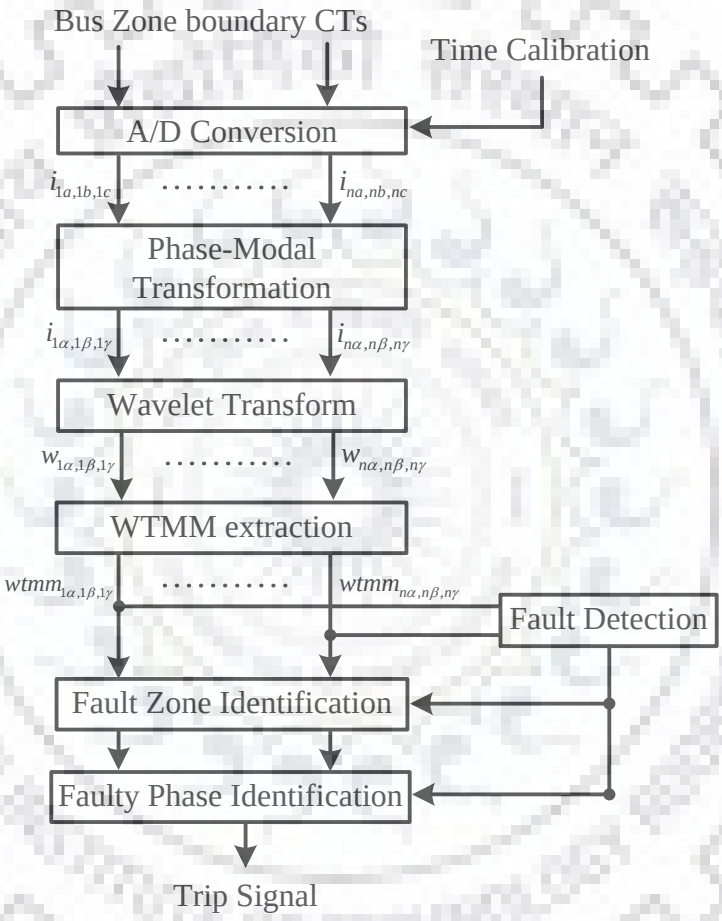

Fig. 4.7: Computational flowchart of the proposed scheme.

urations. MUs present at the bay level acquire CT secondary currents corresponding to individual bus zones. The proposed scheme requires ADC with a moderate sampling frequency of 8 kHz for a fundamental frequency of 50 Hz (160 samples per cycle). Keeping the transient nature of TWs in mind, previously reported TW based protection schemes [44,85] require sampling frequencies in the range of 100-250 kHz. Whereas, the sampling requirement is significantly lower (8 kHz) in the 87BITW. In simpler terms, lower sampling frequency corresponds to fewer current samples and lesser post-fault computational requirements. Here, it is noteworthy to add that conventional CTs used in substations do not posse a very high-frequency response.

The extraction of aerial mode TWs requires phase-modal transformation on the instantaneous current samples. Hence, the requirement of phasor computation (magnitude and phase) with sliding buffers has been eliminated. Moreover, the areal mode current components are calculated with minimal computation as the coefficients of the transformation matrix contains all real numbers. Thereafter, MODWT has been utilized in the current work to compute the wavelet detailed coefficients. The MODWT is a shift-invariant and does not require downsampling. Moreover, scale-1 detailed coefficients for Db1 mother wavelet with two coefficients have been utilized. This is the lowest computational requirement among the WT based busbar protection schemes [36,46–49]. Further, the extraction of WTMMs necessitates three consecutive wavelet coefficients with simpler *smaller than* and *greater than* logic. In case of disturbances due to a fault, the fault detection unit senses concurrent WTMMs across all lines connected with a magnitude greater than a pre-set tolerance value. After detection of a fault, the polarities of the WTMMs are checked for detection of the fault zone. Subsequently, the fault type is classified based on the boundary conditions defined in terms of the magnitude of the same WTMMs. When an internal bus zone fault is detected, a trip signal is sent to corresponding CBs. Further, the computational burden in 87BITW is quantified in the following summaries:

- It is to be noted from equation (4.7) that, computation of each aerial mode TW at a particular instant requires one equation in terms of multiplication of current samples and Karenbauer matrix coefficients. Considering a signal length of N samples, N numbers of computations are required for the calculation of each aerial mode TW.

- As evident from equations (4.8) and (4.9), calculation of detailed wavelet coefficients in MODWT require convolution between the aerial mode TW current samples and the wavelet filter coefficients. As down-sampling is not performed at each scale, a total number of NL_j multiplications are required at each scale. In the proposed scheme, Db1 mother wavelet with 2 filter coefficients at scale-1 ($L_j = 1$) has been used. Hence, $2N$ number of multiplications are required to calculate the scale-1 detailed coefficients (w_1). As the proposed scheme works on scale-1 detailed coefficients, it does not require storage of previous scale wavelet coefficients. On the contrary, DWT performs down-sampling at each scale which requires $NL\sum_{m=0}^{m=j-1} 2^{-m}$ calculations to arrive at scale-j [96]. Afterwards, it requires $NL2^{-j}$ numbers of calculations to find the wavelet detailed coefficients of scale-j (w_j) [92].

- It is to be noted from equation (4.10) and subsequent conditions that calculation of WTMM at each instant require one subtraction and one comparison with *greater than* and *smaller than* logic. Hence, a total number of N subtractions and N comparisons are required for a signal with length N.

- The fault zone identification logic requires monitoring of WTMM polarities at each instant. Hence, N numbers of comparisons are required in this regard. Similarly, the fault classification module calculates the criteria corresponding to each of the 10 fault types. Hence, $10N$ numbers of calculations are required in this regard. It is worth mentioning that the proposed scheme does not involve in any complex calculations at any of the aforementioned stages. It requires basic mathematical operations like subtraction, addition or comparisons that lead to fewer complexities.

4.5 Results and Discussion

The robustness of the presented scheme should be tested for a wide range of fault scenarios. To this end, extensive simulations have been performed by varying parameters such as fault type, fault inception angle (FIA), and fault resistance (R_f). The effect of CT saturation on 87BITW has also been studied in this section. At the end, a comparative analysis of the proposed scheme with the existing busbar protection schemes

has also been presented.

4.5.1 Internal faults

In order to test the sensitivity of 87BITW, SLG fault (A-g) with $FIA = 90°$ and $R_f = 10\ \Omega$ has been simulated on the busbar. Fig. 4.8 shows the simulation results in terms of different aerial mode TWs and corresponding WTMMs for lines l_1, l_2, and l_3. It has been observed from Fig. 4.8 that the polarity of initial WTMMs for α, β, and 0 modes across all the lines are identical which confirms the occurrence of an internal fault on the busbar. Moreover, WTMMs appear exactly at the same instant across all the lines. As only A-phase and ground are involved with this fault, γ-mode WTMMs are not seen in any of the lines. Furthermore, the magnitude of initial WTMMs for α, β, and 0 modes as indicated in Fig. 4.8, satisfy the criterion against A-g fault given in Table 4.4. This confirms the occurrence of SLG (A-g) fault on the busbar.

4.5.2 External faults

In order to test the stability of 87BITW during external faults, a double line fault (A-B) has been simulated on line l_3 at a distance of 10 km from the busbar. Fig. 4.9 shows the simulation results in terms of different aerial mode TWs and corresponding WTMMs for lines l_1, l_2, and l_3. It is observed from Fig. 4.9 that the polarity of initial WTMMs for α, β, and γ mode TWs for l_1 and l_2 are opposite with respect to l_3. This signifies the occurrence of a fault on line l_3.

4.5.3 Different types of fault

Performance of 87BITW has been evaluated for different types of internal fault on the busbar and simulation results are depicted in Table 4.5. It is to be noted that the polarity of initial WTMMs of the respective modes are same for lines l_1, l_2, and l_3. This clearly indicates incidence of an internal fault on the busbar. Furthermore, classification of fault is carried out according to the criterion given in Table 4.4.

Furthermore, Table 4.6 shows the simulation results obtained from 87BITW during various types of external faults on line l_3 at a distance of 10 km from the busbar. It has been observed from Table 4.6 that the polarity of initial WTMMs of the faulted

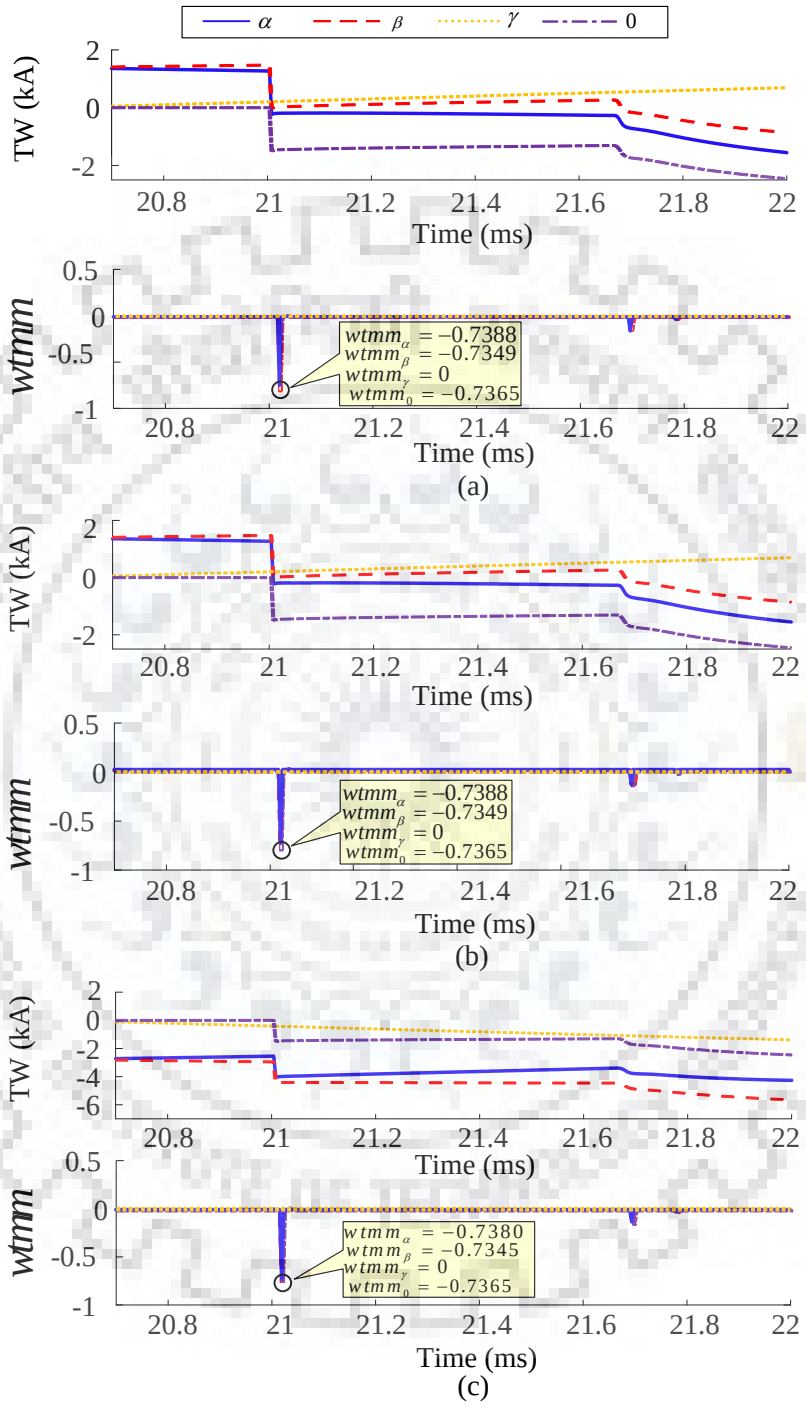

Fig. 4.8: Aerial mode TWs and corresponding WTMMs for an internal fault (A-g) (a) l_1 (b) l_2 (c) l_3

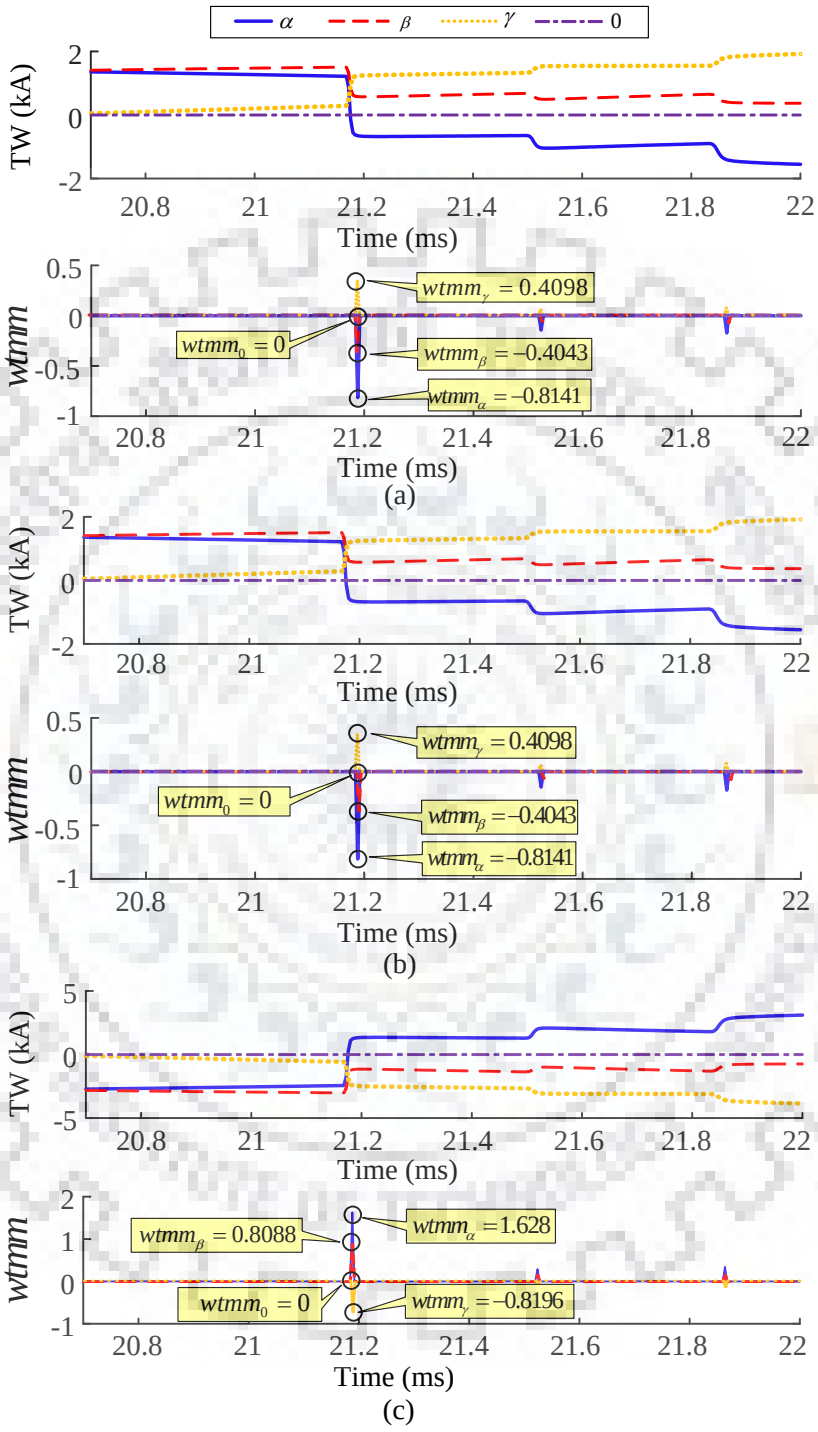

Fig. 4.9: Aerial mode TWs and corresponding WTMMs for an external fault (A-B) (a) l_1 (b) l_2 (c) l_3

Table 4.5: Results for different types of internal faults

case no.	line	Initial $wtmm_m$ α	β	γ	0	Results Fault zone	Fault type
1	l_1	-0.33	0	0.33	0.33	Internal	B-g
	l_2	-0.33	0	0.33	0.33		
	l_3	-0.32	0	0.32	0.33		
2	l_1	-1.37	-0.68	0.69	0	Internal	AB
	l_2	-1.37	-0.68	0.69	0		
	l_3	-1.36	-0.69	0.68	0		
3	l_1	-1.22	-0.79	0.44	-0.35	Internal	AB-g
	l_2	-1.22	-0.79	0.44	-0.35		
	l_3	-1.22	-0.79	0.43	-0.35		
4	l_1	-1.43	-1.52	0.09	0	Internal	ABC
	l_2	-1.43	-1.52	0.09	0		
	l_3	-1.42	-1.53	0.09	0		

Table 4.6: Results for different types of external faults

case no.	line	Initial $wtmm_m$ α	β	γ	0	Results Fault zone
1 (C-g)	l_1	0	0.75	0.74	-0.33	External
	l_2	0	0.75	0.74	-0.33	
	l_3	0	-1.50	-1.48	0.67	
2 (BC)	l_1	-0.35	0.36	0.71	0	External
	l_2	-0.35	0.36	0.71	0	
	l_3	0.70	-0.72	-1.42	0	
3 (BC-g)	l_1	0.43	0.69	0.25	-0.49	External
	l_2	0.43	0.69	0.25	-0.49	
	l_3	-0.87	-1.38	-0.50	0.99	
4 (ABC-g)	l_1	2.12	2.37	0.29	0	External
	l_2	2.12	2.37	0.29	0	
	l_3	-4.24	-4.75	-0.50	0	

line (l_3) is opposite to that of the healthy lines (l_1 and l_2) for the respective modes.

4.5.4 Different fault inception angle

Performance of 87BITW has been evaluated for internal and external faults with wide variation in inception angle and the results are shown in Table 4.7 . It can be concluded from Table 4.7 that 87BITW is able to localize the fault zone with wide range variation in fault inception angle.

Table 4.7: Results for different fault inception angles

$FIA(^\circ)$	fault location	line	Initial $wtmm_m$ α	β	γ	0	Results Fault zone
5	busbar	l_1	-0.25	-0.25	0	-0.23	Internal
		l_2	-0.24	-0.24	0	-0.22	
		l_3	-0.24	-0.24	0	-0.23	
45	busbar	l_1	-1.12	-1.12	0	-1.12	Internal
		l_2	-1.12	-1.12	0	-1.11	
		l_3	-1.11	-1.12	0	-1.11	
135	busbar	l_1	-1.39	-1.39	0	-1.38	Internal
		l_2	-1.39	-1.39	0	-1.38	
		l_3	-1.36	-1.37	0	-1.38	
6	line l_3	l_1	0.11	0.11	0	0.13	External
		l_2	0.11	0.12	0	0.13	
		l_3	-0.22	-0.23	0	-0.26	
45	line l_3	l_1	0.62	0.62	0	0.66	External
		l_2	0.62	0.63	0	0.67	
		l_3	-1.24	-1.25	0	-1.33	
135	line l_3	l_1	0.82	0.82	0	0.36	External
		l_2	0.82	0.82	0	0.36	
		l_3	-1.65	-1.64	0	-0.72	

Table 4.8: Results for internal faults with varying fault resistance

$R_f(\Omega)$	fault location	line	Initial $wtmm_m$ α	β	γ	0	Results Fault zone
10	busbar	l_1	-2.48	-2.45	0	-2.46	Internal
		l_2	-2.48	-2.45	0	-2.46	
		l_3	-2.48	-2.47	0	-2.46	
100	busbar	l_1	-1.36	-1.35	0	-1.35	Internal
		l_2	-1.37	-1.36	0	-1.35	
		l_3	-1.35	-1.36	0	-1.36	
150	busbar	l_1	-0.92	-0.90	0	-0.89	Internal
		l_2	-0.92	-0.90	0	-0.89	
		l_3	-0.90	-0.91	0	-0.90	

Table 4.9: Results for external faults with varying fault resistance

$R_f(\Omega)$	fault location	line	Initial $wtmm_m$				Results
			α	β	γ	0	Fault zone
10	line l_3	l_1	-1.22	-1.19	0	-0.53	External
		l_2	-1.22	-1.19	0	-0.53	
		l_3	2.44	2.38	0	1.06	
100	line l_3	l_1	-0.91	-0.90	0	-0.39	External
		l_2	-0.91	-0.88	0	-0.39	
		l_3	1.82	1.75	0	0.79	
150	line l_3	l_1	-0.65	-0.63	0	-0.28	External
		l_2	-0.65	-0.63	0	-0.28	
		l_3	1.31	1.25	0	0.56	

4.5.5 Different fault resistance

One of the major limitations of 87B is its insensitivity/less sensitivity towards high resistance internal faults. This is due to the reduction in the magnitude of fault current which produces a small operating current. Though the probability of high resistance faults on the busbar is less, a reliable busbar protection scheme should be prepared for the worst possible cases. The performance of 87BITW has been evaluated for internal faults on the busbar with varying fault resistance and the results are shown in Table 4.8. It is to be noted from Table 4.8 that the polarity of initial WTMMs of all three lines is the same. Hence, the faults have been identified as internal busbar faults by 87BITW. Conversely, various external faults have also been simulated on line l_3 with different fault resistance and the simulation results are shown in Table 4.9. It has been observed from Table 4.9 that the polarity of initial WTMMs of individual modes for line l_3 is opposite to that of lines l_1 and l_2. Hence, an external fault on line l_3 has been identified by 87BITW. It can be concluded from Table 4.8 and 4.9 that the proposed scheme is able to identify the fault zone with varying fault resistance. Moreover, the proposed scheme has also been able to locate the fault in case of high resistance faults for which 87B fails.

4.5.6 Effect of CT saturation

A heavy external fault near the fault zone boundary of CTs results in very high current which may saturate the CT core [97]. Significant amount of CT saturation during heavy external fault conditions may lead to mal-operation of 87B. In order to study

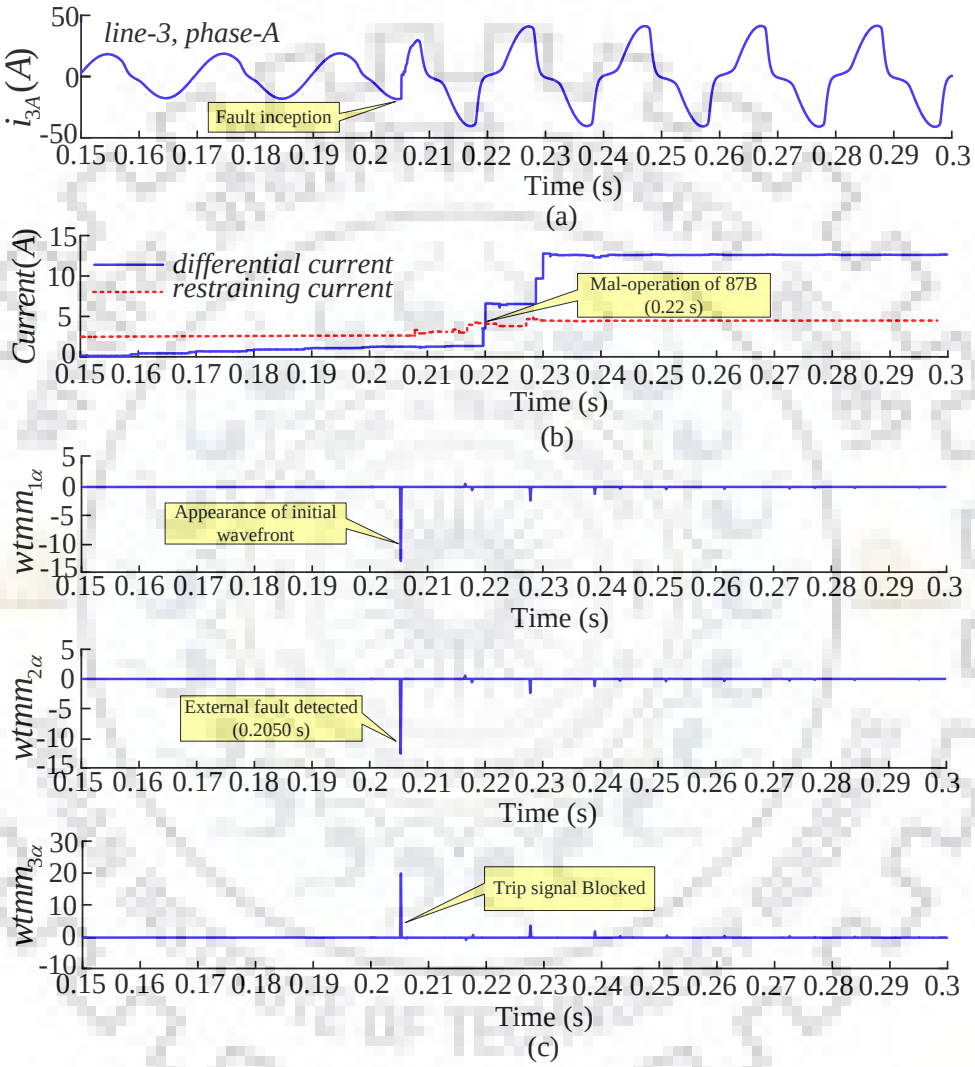

Fig. 4.10: (a) CT secondary waveform of phase-A of line l_3. (b) Differential and restraining currents of 87B. (c) α-mode WTMMs for line l_1, l_2, and l_3.

the influence of CT saturation on 87BITW, an external A-g fault has been simulated at a distance of 1 km from the busbar on line l_3. In order to replicate the CT saturation phenomenon, the secondary burden of the corresponding CT has been increased ten times [73]. The saturated CT secondary waveform of phase-A of line l_3 has been shown in Fig. 4.10 (a). Moreover, differential and restraining currents of 87B are shown in Fig. 4.10 (b). These two values are calculated as per (4.29). The percentage bias has been set at 100 % in these calculations.

$$i_{diff(A)} = \left| \sum_{i=1}^{3} i_{iA} \right| ; i_{res(A)} = \sum_{i=1}^{3} |i_{iA}| \tag{4.29}$$

where, i_{diff} and i_{res} are the differential and restraining currents (for 87B-A), respectively. i_{1A}, i_{2A}, and i_{3A} are phasor values of instantaneous A-phase currents of line l_1, l_2, and l_3, respectively.

It is observed in Fig. 4.10 (b) that the scheme (87B) mal-operates as the differential current exceeds restraining current at 0.22 s. Further, the results obtained from 87BITW is shown in Fig. 4.10 (c). It is to be observed from Fig. 4.10 (c) that α-mode WTMMs appear across all lines before the mal-operation of 87B. Moreover, polarity of α-mode WTMMs for line l_3 is opposite to that of l_1 and l_2. Hence, an external fault is identified. As the fault has been identified before the development of differential current, 87BITW remains stable in this situation.

4.5.7 Comparison with existing TW based scheme

The TW-based busbar protection scheme, reported in [44], is based on the amplitude integral of voltage TWs from the instant of first incident to first reflected-TW observed at the busbar location. In this context, Fig. 4.11 (a) shows the voltage waveforms when a solid three-phase through fault is simulated at 500 m from the busbar. It results in zero voltage TWs in all phases leading to the mal-operation of the scheme reported in [44]. Conversely, Fig. 4.11 (b) shows the simulation results obtained from 87BITW in terms of α-mode WTMMs for current TWs of line l_1, l_2, and l_3 for the aforementioned fault scenario. It is observed from Fig. 4.11 (b) that the polarity of WTMMs of line l_3 is opposite to that of lines l_1 and l_2 which confirms an external fault. In these scenarios, current TWs of high magnitude are observed in contrary to voltage TWs of

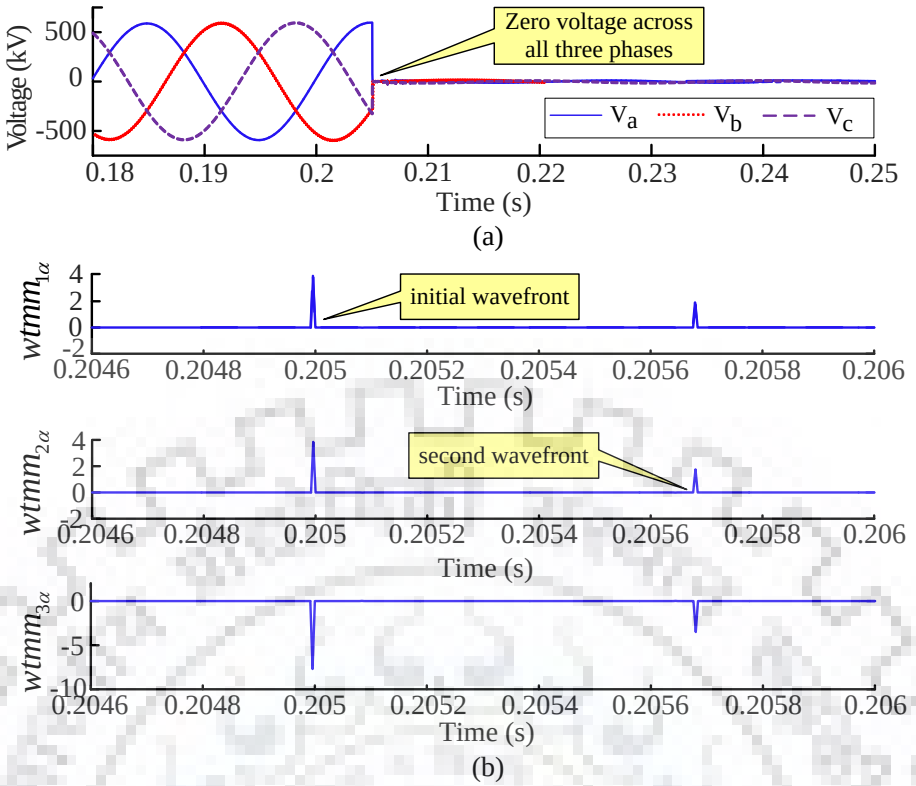

Fig. 4.11: (a) Voltage waveforms during a 3-ph fault at 500 m from busbar. (b) Initial WTMMs of α-mode current TWs for line l_1, l_2, and l_3.

small magnitude. Moreover, CCVTs cannot transform transient voltage signals with a sampling frequency in the range of kHz. Hence, CTs are more preferable than CCVTs.

4.5.8 Comparison with existing Wavelet based scheme

The wavelet-based protection scheme (87BW), reported in [49], works on the principle of energy available in the differential and restraining waveforms. However, when the fault path consists of a high impedance element, the fault current is minimal. The available energy in the differential element in these scenarios may not be sufficient to detect the fault.

In order to evaluate the performance of 87BITW in comparison to the wavelet-based scheme (87BW), an A-g fault with fault resistance 200 Ω is simulated on the busbar. The differential energy for 87BW is calculated from the wavelet coefficients derived from the mother wavelet Db4 using MODWT through sliding windows [49]. To stabilize the restraining current which oscillates in every half cycle, a smoothed version of restraining current, as reported in [98], has been used. A moderate and

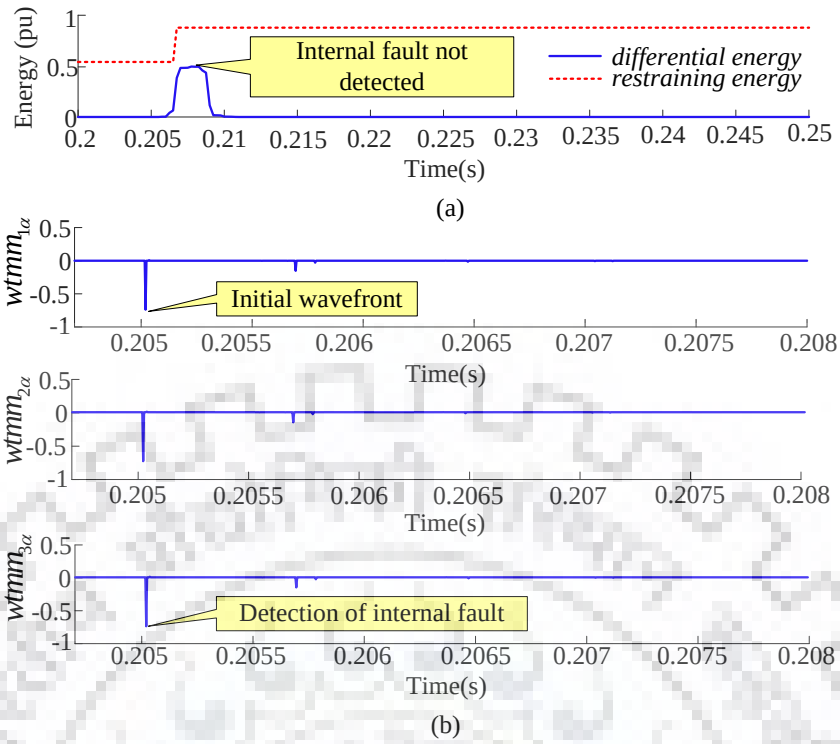

Fig. 4.12: (a) Differential and restraining energy obtained for an internal fault 200 Ω. (b) Initial WTMMs of α-mode current TWs for line l_1, l_2, and l_3.

widely adopted value of 0.6 has been set for the percentage bias setting [99].

Performances of the wavelet-based scheme (87BW) and the proposed scheme in the aforementioned scenarios are shown in Fig. 4.12 (a) and (b), respectively. It is to be observed from Fig. 4.12 (a) that the differential energy is not sufficient to overcome the restraining energy in order to issue the trip signal. On the contrary, as shown in Fig. 4.12 (b), the alpha mode initial WTMMs appearing across all lines (l_1, l_2, and l_3) are of same polarity. Hence, an internal fault is detected by 87BITW. This proves the effectiveness of the proposed scheme in comparison to the wavelet-based scheme in detecting faults with high impedance.

4.5.9 Comparison of computational and communication requirements

Several wavelet-based busbar protection schemes [36, 46–49] have been proposed in the past. However, the computational and communication requirements of these schemes have been a major concern for their on-field implementation. To this end, Table 4.10 provides a comparative evaluation of these schemes in terms of computational and

communication requirements. The followings points are summarized from Table 4.10:

- Different versions of WT such as Discrete Wavelet Transform (DWT), CWT, WPT and MODWT have been used for busbar protection. While CWT offers the best time-frequency localization among all, the computational requirements are the highest. Busbar protection, in particular, requires high-speed protection and signal transmission. Hence, the use of CWT for high-speed protection applications would be unsuitable. On the contrary, DWT provides faster calculation with less number of coefficients. However, it requires decimation at every scale of decomposition. Hence, time localization is not very accurate with DWT, which is another important aspect of transient-based protection applications. WPT is another variant of DWT where in addition to the approximate coefficients the detailed coefficients are also decomposed into smaller window packets. In comparison to DWT, it doubles the computational requirements. On the contrary, MODWT is the shift-invariant version of DWT and hence, time localization is accurate. As it does not require down-sampling, its computational requirements are lesser than DWT and least among all.

- The choice of mother wavelet is application specific and depends on the type of signal to be analyzed. However, with more number of filter coefficients, the computational burden increases at each scale. Moreover, as the scale of decomposition increases, both computation requirements and time increases. Reconstruction of the signal from the wavelet coefficients adds more computation. With these observations from Table 4.10, it is to be concluded that 87BITW with Db1 mother wavelet and 2 filter coefficients at scale-1 detailed coefficients requires the least computation.

- After the calculations of wavelet coefficients, 87BITW calculates the maximas with every three consecutive samples with simple greater than or less than logic. On the contrary, all other schemes, as mentioned in Table 4.10, require either computation in the form of power, differential, restraining, energy coefficients or combination of them. In this aspect, 87BITW requires minimal computation.

- In [36,46–49], the coefficients (power, differential, restraining or energy) are to be calculated separately for each phase. Hence, three phase segregated relays with

inter relay communication are required. On the other hand, the is based on aerial mode TWs (alpha, beta, and gamma) derived from phase-modal transformation. Fault in any of the phases reflects in more than one of the aerial modes and hence, separate calculation for each phase is not required. A single relay which compares the magnitude and polarity of the WTMMs can identify both the fault zone and faulted phase. On this account, it is to be concluded that 87BITW does not require three phase segregated relays with inter-relay communication which is a necessity in all other schemes for faulted phase identification.

Table 4.10: Computational and communication requirements in various schemes

	Scheme [47]	Scheme [48]	Scheme [36]	Scheme [46]	Scheme [49]	Proposed Scheme (87BITW)
Version of WT	DWT	DWT	CWT	WPT	MODWT	MODWT
Down-sampling	Yes	Yes	NA	Yes	No	No
Mother Wavelet	Db3	Bio6.8	Morlet	D2	Db4	Db1
Filter coefficients	6	17	-	2	8	2
Scale	1	1	46 (Scaling factor)	3	2	1
Reconstruction Requirement	Yes	No	No	No	No	No
Post-WT computation	Power Coefficients	Differential Coefficients, Fault index	Differential, Restraining Coefficients	Differential Coefficients	Differential, Smoothed restraining, Energy Coefficients	WTMMs
Required signals	Voltage, Current	Current	Current	Current	Current	Current
Required relays	3	3	3	3	3	1
Inter-relay communication	Required	Required	Required	Required	Required	Not Required

4.6 Real Field Implementation Feasibility

4.6.1 Proposed Architecture

Fig. 4.13 shows the proposed architecture for real field application of the reported scheme based on IEC-61850-9-2 [24] process bus applications. The physical wiring from CT secondary analog signals to the microprocessor-based relay in conventional substations is replaced by MUs, Ethernet based process bus (IEC-61850-9-2) and Intelligent Electronic Devices (IEDs). The CT secondary terminals are wired physically with the MUs at each bay. The information on breaker status (ON/OFF) is also acquired in breaker IEDs in binary form (1/0) through bidirectional GOOSE (Generic Object Oriented Substation Event) messages [100]. The MUs covert the analog CT secondary current signals to digital time-stamped sample values (SVs). Timestamping with accuracy $< 1\mu s$ is achieved through the synchronization unit connected to the GPS station clock. Analog and digital delays due to the filtering circuits and timers are calibrated for synchronization of SVs collected from all bays. The digital output of MU is connected to an Ethernet hub utilizing optical fibres. In large substations, several Ethernet hubs are inter-connected collectively forming a process bus. The SVs are MULTICAST from the MUs to IEDs through the 100 Mbps Ethernet based IEC 61850 process bus in a PUBLISHER-SUBSCRIBER mode.

The proposed three subroutines (i) *Fault detection* (ii) *Fault zone identification*, and (iii) *Fault Classification* are implemented as three separate nodes in IEDs. The inter-node communication between these IEDs is achieved through GOOSE messages. Node-1 detects a fault when the magnitude of WTMMs observed in the SVs, acquired across all MUs, is greater than a pre-set threshold. Upon detecting a fault, it activates Node-2 through GOOSE message to IED-2. Based on the polarity of the WTMMs, IED-2 decides if the fault lies in the bus zone and subsequently activates IED-3 upon detection of a bus fault. Thereafter, Node-3 classifies the fault type and corresponding bus zone CBs in a dynamic configuration or, all of the CBs in case of static configuration are tripped through GOOSE messages to breaker IEDs. All the activities are controlled and monitored in the control centre through an Ethernet based station bus.

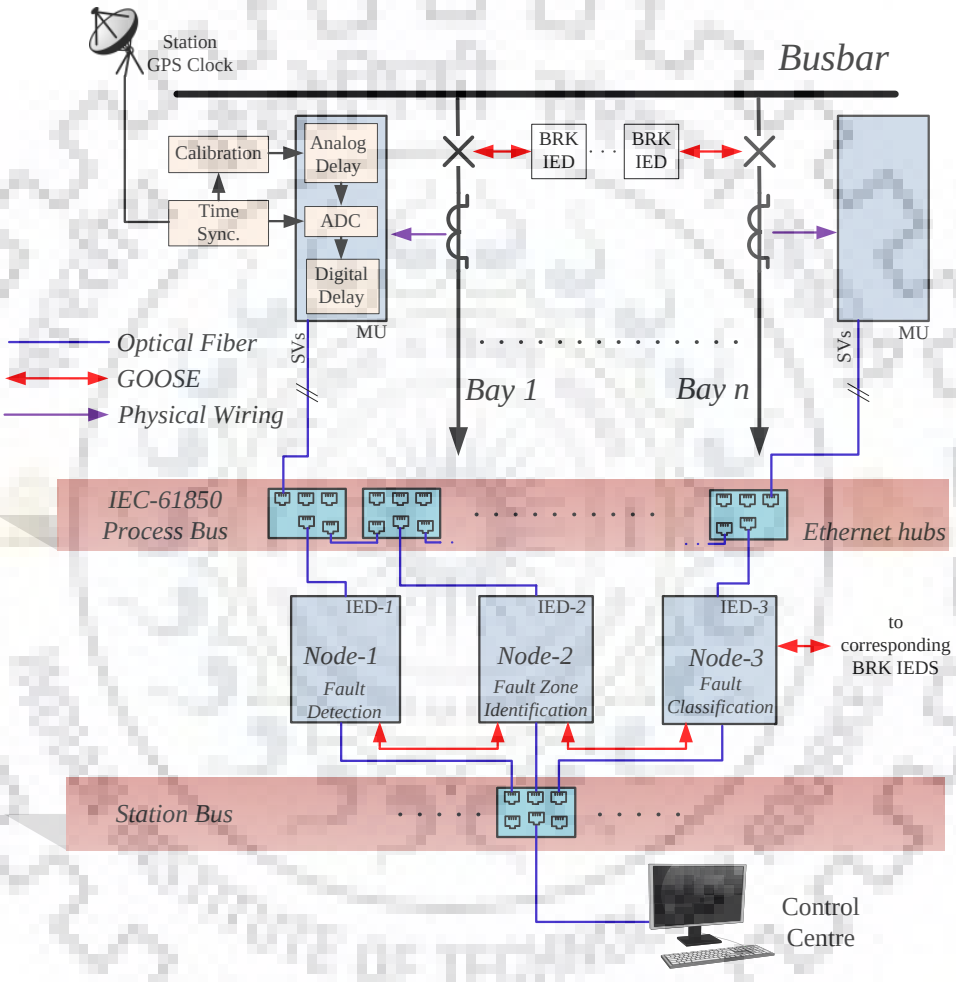

Fig. 4.13: Proposed architecture for real field application.

4.6.2 Response time

The total response time of 87BITW depends on the following factors: (i) path delay, (ii) traffic delay, and (iii) node delay. Out of these factors, (i) and (ii) are because of the latency in communication due to IEC 61850 implementation. The latency in the system is variable which depends upon the size and complexity of the network architecture. The path delay in optical fibres does not exceed 5 μs for 1000 m length in a 1000 Mbps Ethernet framework [101]. The traffic delay depends on the availability of communication channels for the nodes (IEDs). With fewer nodes simultaneously accessing the data, channel availability is high and traffic delay is less. It is worthwhile to note that latency due to (i) and (ii) is tolerable up to 125 μs (time step between two consecutive samples) in 87BITW. As the proposed schemes work only with three nodes, the expected traffic delay is substantially below this tolerance limit. Lastly, the node delay is due to the implementation of the proposed algorithm and the inherent delay due to the electronic circuits inside IEDs. The proposed algorithm requires 625 μs (125 $\mu s/sample$ $\times$ 5 samples) for extraction of WTMMs. It involves two samples window for calculation of wavelet coefficients and three samples window for computation of WTMMs. All other calculations are real time based. The inherent delay in manufacture specific and varies in the ranges of ($5 \sim 10\mu s$). Accounting all these considerations, it is implied that the response time of 87BITW is below 2 ms. Modern state-of-the-art instantaneous busbar differential relays have a response time of around 1/4th cycle (5 ms). In this regard, 87BITW provides reliable protection with faster response time than modern protection schemes.

4.7 Conclusion

This chapter presents a high-speed busbar protection scheme based on the polarity of initial WTMMs appearing after fault inception. The WTMMs are extracted from the current TWs and their polarities are compared individually for each mode which in turn improves the reliability of the scheme. After extensive testing, the following conclusions are drawn about the advantages of 87BITW:

- It provides higher sensitivity during internal faults on the busbar and better stability in case of external faults.

- 87BITW overcomes the problem of CT saturation during external faults as it detects these faults based on the instant of initial WTMMs which appear before the starting of CT saturation.

- 87BITW offers improved stability against close-in external faults and higher sensitivity in case of internal faults with high fault resistance.

- In comparison to the existing schemes, the computational requirements are largely reduced. Moreover, the requirement of three phase-segregated relays with inter-relay communications can be avoided.

- 87BITW also marginalizes the computational burden on the busbar protection unit as it does not involve complex processing of post-fault data. The time delay due to phasor computation and filtering processes can be avoided by implementing the proposed scheme.

Chapter 5

Sampled Value-based Bus Zone Protection with *dq*-components

Previously discussed busbar protection schemes show improvements in more than one aspects of busbar protection. The advancement in terms of process bus applications in this regard has opened the window for high speed protection using instantaneous sampled value data. The processing speed and data management have improved in case complex substation configurations using dynamic bus zone selection. This chapter discusses development of a sampled value based bus bar protection scheme based on direct axis component of current (87BD). The advantages of using d-axis component of current along with the feasibility of process bus implementation have been discussed in the subsequent sections.

5.1 Introduction

Though bus zone faults account for only 6-7% of the total faults in a power system, the severity and operational consequences are enormous. A bus fault may result in a costly affair in terms of repair of damaged equipment and forced alterations in power supply. The present practice is to reduce the fault clearance time of the relay rather than developing new arc extinction methods for the CBs [68]. Stability is another prime aspect while designing a bus zone relay as its mal-operation causes power outage to a large portion of the power system. Hence, bus protection is challenging in terms of reliability and speed. Enhanced numerical data processing units provide greater

flexibility and possible on-chip implementation of smart solutions. Hence, selection of excellent mathematical analysis tools and algorithms has the utmost significance [69, 102]. Security of the protection unit can be improved by appropriate substation design and dividing the bus zone into multiple zones [3]. An internal bus fault, in this case, will disturb only a smaller part of the substation and fewer components will be affected.

This chapter presents a novel algorithm based on dq-components which has been effectively used for bus zone protection. The analog CT secondary signals are acquired and converted into SVs. Then, fundamentals of instantaneous current-based differential protection scheme (87B) have been considered to establish the trip logic of 87BD. Its performance has been validated by simulating faults on an existing 400-kV substation with double-bus-single-breaker configuration. Moreover, a laboratory experimental setup has been developed to test the authenticity of 87BD for various fault scenarios. The obtained results from the simulation model and laboratory prototype testify the claims of higher sensitivity during internal faults and better stability during external faults with CT saturation. 87BD has been able to provide high-speed busbar protection against a wide range of internal faults. Comparative evaluation with contemporary busbar protection schemes indicates its superiority.

5.2 State-of-the-art

Directional comparison based busbar protection schemes [20, 21, 23] use superimposed components of impedance. However, higher cost and increased complexity due to the requirement of voltage signals along with current signals limits its application. Two of the widely adopted busbar protection schemes are in the form of low and high-impedance current differential schemes. The high-impedance protection scheme works on the principle of voltage comparison across the differential element and hence, provides better stability in case of CT saturation. However, its application is restricted as it requires dedicated CTs and surge protective equipment. Predominantly, the fault clearance time of these schemes is high because of the slow sampling of voltage signals. Quite the contrary, low-impedance based protection schemes [16, 33, 83] can be implemented with measurement CTs and compensate CT ratio errors. However,

these schemes mal-operate in case of substantial CT saturation. Moreover, HIFs do not produce sufficient operating current for proper detection [103]. Hence, the current research trend shifts towards developing modern numerical low-impedance differential protection algorithms with better security against CT saturation and high sensitivity towards HIFs.

The aforementioned schemes have the common requirement of voltage and current phasor calculations which rule out the possibility of sub-cycle tripping. In addition, the filtering process adds significant delay. On the contrary, busbar differential protection schemes based on instantaneous values provide fast tripping in the range of quarter cycle [99]. TW-based schemes [44, 77] provide ultra-high-speed protection. However, faults with a small inception angle may not be detected due to insignificant TWs. Similarly, WT-based schemes [46–48,84] are prone to noise. Furthermore, the burden on the communication channel increases as a large volume of data needs to be transferred at a very high speed. A hybrid neuro-fuzzy approach has been presented in [52]. Though it produces a very high classification accuracy, a large number of neurons are required for a tedious training process. Machine learning techniques such as SVM and RVM [55, 58, 59] report high accuracy. However, because of the abrupt behaviour of the Kernel functions, probabilistic predictions are not feasible. Moreover, on-chip implementation of these schemes introduces enormous complexity.

In order to overcome these limitations, this chapter introduces a new bus zone protection scheme based on *dq* components of current. The fundamentals of 87B are established in terms of *d*-axis components. A simpler approach to bus zone protection is proposed which performs more efficiently with low data requirement as only *dq* components of current are monitored instead of all the three phase current data. 87BITW has an edge over TW or wavelet-based schemes as it does not require extraction and complex post-processing of fault data.

5.3 Parks Transformation

5.3.1 Basic fundamental concepts

Parks (*dq*) transformation is widely adopted for research analysis in the field of salient pole synchronous generators, where varying inductances in a static frame are converted

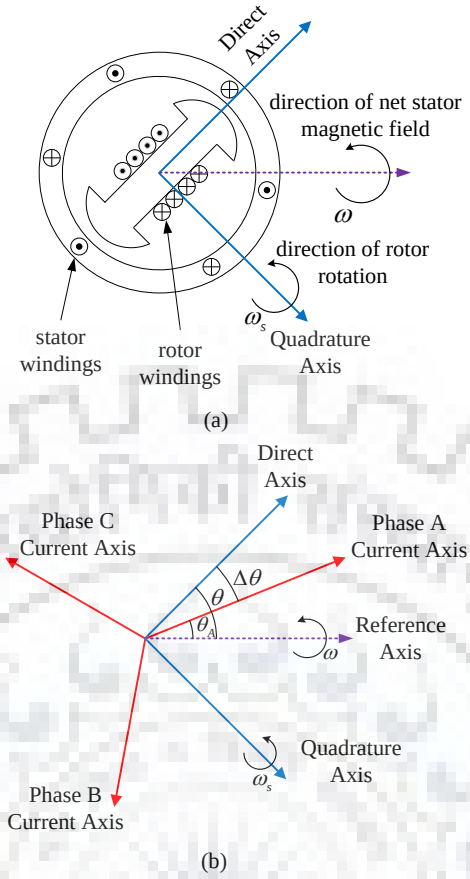

Fig. 5.1: Representation of (a) dq axes in a synchronous generator (b) abc current axes with respect to dq axes

into static inductances in a varying rotating frame. To this end, two rotating axes: direct (d) and quadrature (q), as shown in Fig. 5.1, are defined. These two axes rotate along the direction of rotor rotation with angular synchronous speed ω_s rad/sec. A reference axis is defined in the direction of net magnetic field of the three phase stator windings which are 120 ° space-separated. The net magnetic field rotates at the speed of three phase current phasor rotation ω rad/sec. Due to the magnetic locking between the stator and rotor magnetic field, $\omega_s = \omega$. Hence, the reference axis rotates in synchronization with the dq axes. An observer on the reference axes sees the balanced three phase current signals as constant DC magnitudes.

The direct and quadrature axes components of current (I_{dq}) can be calculated from the three phase current (I_{abc}) as per the following equations:

$$\begin{bmatrix} I_d(k) \\ I_q(k) \end{bmatrix} = T_{dq} \cdot \begin{bmatrix} I_a(k) \\ I_b(k) \\ I_c(k) \end{bmatrix} \tag{5.1}$$

where,

$$T_{dq} = \frac{2}{3}\begin{bmatrix} \cos(\phi) & \cos(\phi - \frac{2\pi}{3}) & \cos(\phi + \frac{2\pi}{3}) \\ -\sin(\phi) & -\sin(\phi - \frac{2\pi}{3}) & -\sin(\phi + \frac{2\pi}{3}) \end{bmatrix} \tag{5.2}$$

I_d and I_q are the direct and quadrature axis components of current, respectively, $\phi = k\omega\Delta t + \theta$, Δt is the sampling interval, θ is the angle between the direct axis and reference axis. As three phase signals can be monitored with either d or q components, the computational requirements are significantly reduced.

5.3.2 Fault analysis using Parks (dq) transformation

The three phase currents of a balanced system are given by:

$$\begin{aligned} I_a &= I_{am}\sin(\omega t + \theta_A) \\ I_b &= I_{bm}\sin(\omega t + \theta_A - 2\pi/3) \\ I_c &= I_{cm}\sin(\omega t + \theta_A + 2\pi/3) \end{aligned} \tag{5.3}$$

where I_{am}, I_{bm}, and I_{cm} are the maximum values of phase currents I_a, I_b, and I_c, respectively. θ_A is the initial phase shift of phase-A axis. Applying equation (5.3) and basic trigonometric operations on equation (5.2), the direct (d) and quadrature (q) axes components of current are calculated as followings:

$$\begin{aligned} I_d = \frac{1}{3}\Big\{ &- \big[I_{am} + I_{bm} + I_{cm}\big]\sin(\theta - \theta_A) \\ &+ \big[I_{am} - 1/2(I_{bm} + I_{cm})\big]\sin(2\omega t + \theta + \theta_A) \\ &+ \big[\sqrt{3}/2(-I_{bm} + I_{cm})\big]\cos(2\omega t + \theta + \theta_A)\Big\} \end{aligned} \tag{5.4}$$

$$\begin{aligned} I_q = \frac{1}{3}\Big\{ &- \big[I_{am} + I_{bm} + I_{cm}\big]\cos(\theta - \theta_A) \\ &+ \big[I_{am} - 1/2(I_{bm} + I_{cm})\big]\cos(2\omega t + \theta + \theta_A) \\ &+ \big[\sqrt{3}/2(-I_{bm} + I_{cm})\big]\sin(2\omega t + \theta + \theta_A)\Big\} \end{aligned} \tag{5.5}$$

In case of balanced steady-state conditions, $I_{am} = I_{bm} = I_{cm} = I_m$. Then,

$$I_d = -I_m\sin(\theta - \theta_A) \tag{5.6}$$

$$I_q = -I_m\cos(\theta - \theta_A) \tag{5.7}$$

and,

$$\theta_A = \theta - \tan^{-1}\left[\frac{I_d}{I_q}\right] \tag{5.8}$$

θ_A can be calculated using any random value of θ. By assuming $\theta = \theta_A$, the dq components can be made zero during steady state conditions. Otherwise, they are constant DC values.

In case of fault conditions, $I_{am} \neq I_{bm} \neq I_{cm}$. As per equations (5.4) and (5.5), oscillations in I_d and I_q are observed with a frequency of 2ω. Hence, dq components can be effectively used in place of abc components for fault analysis.

5.4 Proposed Protection Scheme (87BD)

5.4.1 Algorithm development

The direct axis current (I_d) for each line associated with a particular bus zone (z) is calculated as per equations (5.1)-(5.8). Thereafter, the differential and restraining current coefficients C_{diff} and C_{res}, respectively, for each zone are calculated as follows:

$$C_{diff}(k)^z = \left|\sum_{p=1}^{n} I_{d,p}(k)\right|; \quad C_{res}(k)^z = \sum_{p=1}^{n} |I_{d,p}(k)| \tag{5.9}$$

where, n is the number of lines associated with bus zone (z) and $I_{(d,p)}$ is the direct axis current of the p^{th} line. The bus zone z is decided based on the status of breaker and isolators as described in the next section.

The fault induced transients are of different amplitudes for different fault scenarios. For example, HIFs or faults with small inception angle do not produce sufficient amount of differential current. Moreover, noise present in the fault data may adversely affect the instantaneous current based scheme. Hence, a cumulative approach is more suitable as it produces smoother and fast response [104]. In this regard, the operating and restraining current for the instant (k) may be calculated as the moving average (A)

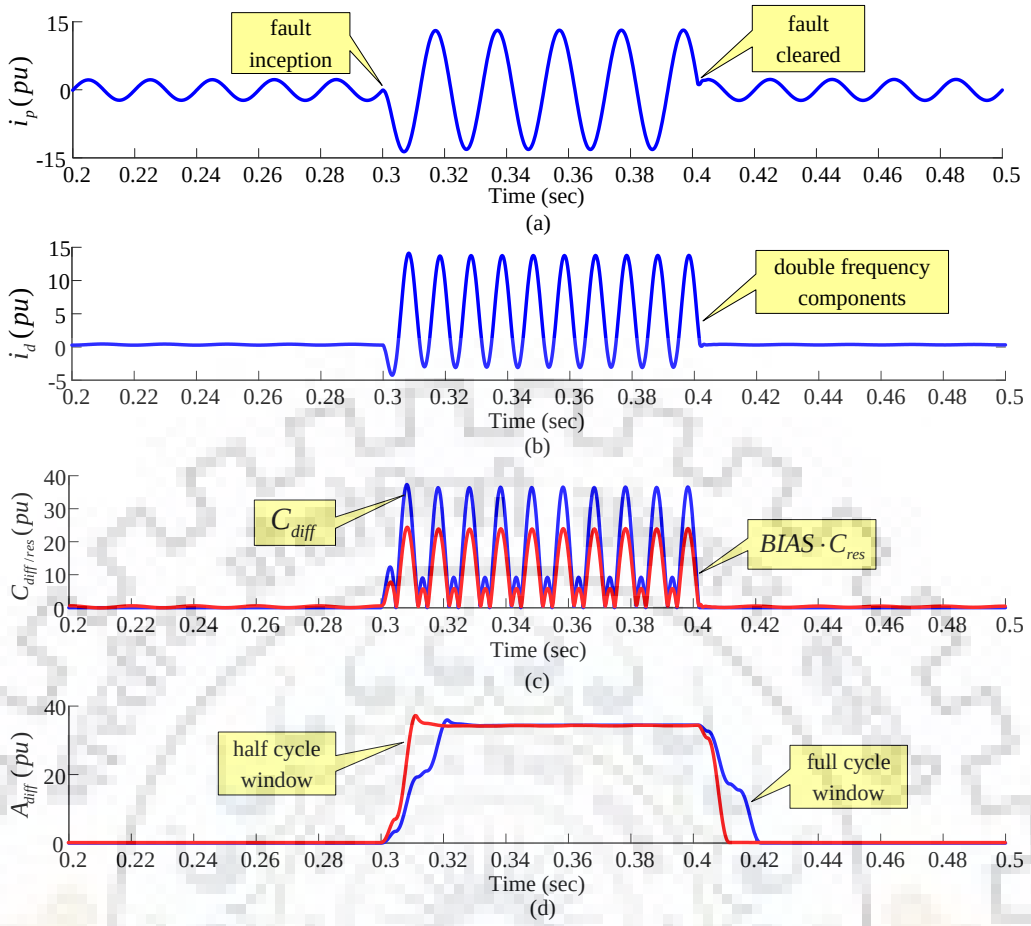

Fig. 5.2: Waveforms of (a) instantaneous current (b) direct-axis current (c) differential and restraining current coefficients (d) differential current.

over data window length (M).

$$A_{diff}(k)^z = \sum_{m=k-M+1}^{k} C_{diff}(m)^z \Big/ M;$$
$$A_{res}(k)^z = \sum_{m=k-M+1}^{k} C_{res}(m)^z \Big/ M \tag{5.10}$$

The selection of the data window length (M) has been decided based on the behaviour of differential and restraining currents. An example of instantaneous and direct axis current components in case of a single line to ground fault which extinguishes after 5 cycles is shown in Fig. 5.2. It is to be noted from Fig. 5.2 (a) and (b) that the fault induced transients in terms of direct axis current oscillate with a double frequency component. As evident from Fig. 5.2 (c), the differential and restraining components show similar patterns in every half power cycle (0.01 sec). It is evident from Fig. 5.2 (d) that the half cycle data window produces a smoother and fast response than the

full cycle window.

Any disturbance in the system can be identified by monitoring the incremental restraining quantity (A_{res}) with respect to time. To this end, a disturbance detection coefficient $dd(k)$ is defined as per equation (5.11).

$$dd(k)^z = \frac{A_{res}(k)^z - A_{res}(k-1)^z}{\Delta t} > 0 \tag{5.11}$$

The tripping logic of the relay is set in terms of equation (5.12).

$$A_{diff}(k)^z > BIAS \cdot A_{res}(k)^z \tag{5.12}$$

In 87BD, equations (5.11) and (5.12) are monitored simultaneously for fault zone identification. The value of BIAS is set in terms of sensitivity of the relay against external faults with CT saturation. Its value normally varies between 0.25-0.8 [26]. 87BD has been tested with the minimum value of 0.25 which ensures security for higher settings.

5.4.2 System study

Fig. 5.3 shows the single line diagram of 400-kV double-bus-single-breaker configuration modelled in PSCAD/EMTDC software package [79]. The transmission lines L1, L2, L3, and L4, each with a physical length of 100 km, are connected to either of the two buses (Bus 1 and Bus 2) through series of breakers (BK) and isolators (IS). Five isolators are connected to each of the lines among which three (IS3, IS4, and IS5) are used in case of breaker maintenance. The remaining two (IS1 and IS2) are used to connect the transmission line to either of the buses. The status of each of the isolators has been represented as either Normally Closed (NC) or Normally Open (NO). The buses are connected through a Bus Coupler (BC) which is NC during normal operating conditions. It is used to transfer the load to the healthy bus in the event of system abnormalities. The rest of the power system connected after the transformer in each line has been represented by the Thevenin's equivalent sources (S1, S2, S3, and S4). The system parameters are depicted in Appendix-V. A sampling frequency of 4 kHz (250 μs/sample or 80 samples/cycle) for a fundamental frequency of 50 Hz has been utilized to acquire current signals.

The transmission lines L1 and L2 are connected to Bus 1 through L1IS1 and L2IS1.

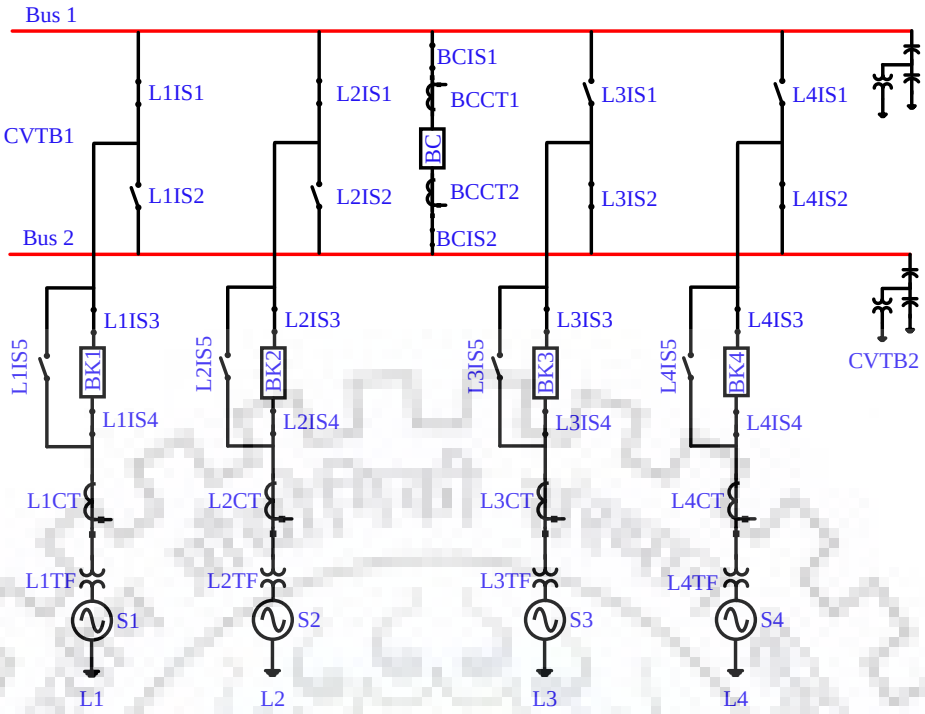

Fig. 5.3: 400-kV substation with double bus single breaker configuration.

Table 5.1: Zone selection for different transmission lines.

Line	Zone 1 ($z1$)	Zone 2 ($z2$)
L1	L1IS1 *AND* (BK1 *OR* L1IS5)	L1IS2 *AND* (BK1 *OR* L1IS5)
L2	L2IS1 *AND* (BK2 *OR* L2IS5)	L2IS2 *AND* (BK2 *OR* L2IS5)
L3	L3IS1 *AND* (BK3 *OR* L3IS5)	L3IS2 *AND* (BK3 *OR* L3IS5)
L4	L4IS1 *AND* (BK4 *OR* L4IS5)	L4IS2 *AND* (BK4 *OR* L4IS5)

Similarly, L3 and L4 are connected to Bus 2 through L3IS2 and L4IS2. Under these settings, zone 1 ($z1$) boundaries have been defined by the CT locations L1CT, L2CT, and BCCT2. Likewise, zone 2 ($z2$) boundaries have been defined by the position of L3CT, L4CT, and BCCT1. It should be noted that this arrangement overlaps the bus zones and hence, the blind spots between the bus coupler (BC) and CTs (BCCT1/BCCT2) are avoided. The transmission lines and network elements are dynamically allocated the bus zones as per the logic laid out in Table. 5.1.

5.5 Architecture of 87BD based on IEC 61850

5.5.1 System Architecture

Fig. 5.4 shows the proposed architecture of the 87BD scheme based on SVs (IEC-61850). The physical wiring of CT secondary analog signals to the microprocessor-based relay in conventional substations is replaced by MUs, Ethernet based process bus (IEC-61850-9-2) and Intelligent Electronic Devices (IEDs) [24]. The analog current signals of CT secondary outputs are hardwired to the individual bay MUs. The information of three phase breaker and isolator statuses are acquired by the breaker IEDs. Time synchronization of each of the units is achieved by the GPS clock. The digital output of MUs is connected to an Ethernet hub by optical fibres. In a large substation, the number of Ethernet hubs are increased with the number of MUs. The proposed 87BD scheme and zone selection logic are implemented in different IEDs. The IEDs coordinate between themselves and send TRIP signals to breaker IEDs through *GOOSE* (Generic Object Oriented Substation Event) messages.

5.5.2 Algorithm Implementation

The detailed data flow for 87BD is shown in Fig. 5.5. The analog CT secondary current signals are converted to SVs by the MUs. Timestamping with accuracy $< 1\mu$ sec is achieved through the synchronization unit connected to the station clock. Required additional analog delay is provided for time calibration between all units. The SVs are MULTICAST from the MUs (publisher) to IEDs (subscriber) through the 100 Mbps Ethernet based IEC 61850-9-2 process bus [105, 106]. The data transfer is carried out at a fixed 80 SVs per cycle in a buffer structure with digital delay as defined in IEC-61850-7-3. The proposed 87BD scheme is implemented in different IEDs. The differential and restraining quantities ($A_{diff}(k)$, $A_{res}(k)$) along with the disturbance detection index ($dd(k)$) for each of the zones connected to the busbar are calculated. The zone selection logic based on the status of breaker and isolators is implemented in a separate IED. A positive output from disturbance detection and trip logic units detects an internal fault in the respective bus zone. The trip decision is sent by the IEDs to corresponding zone CBs through *GOOSE* messages.

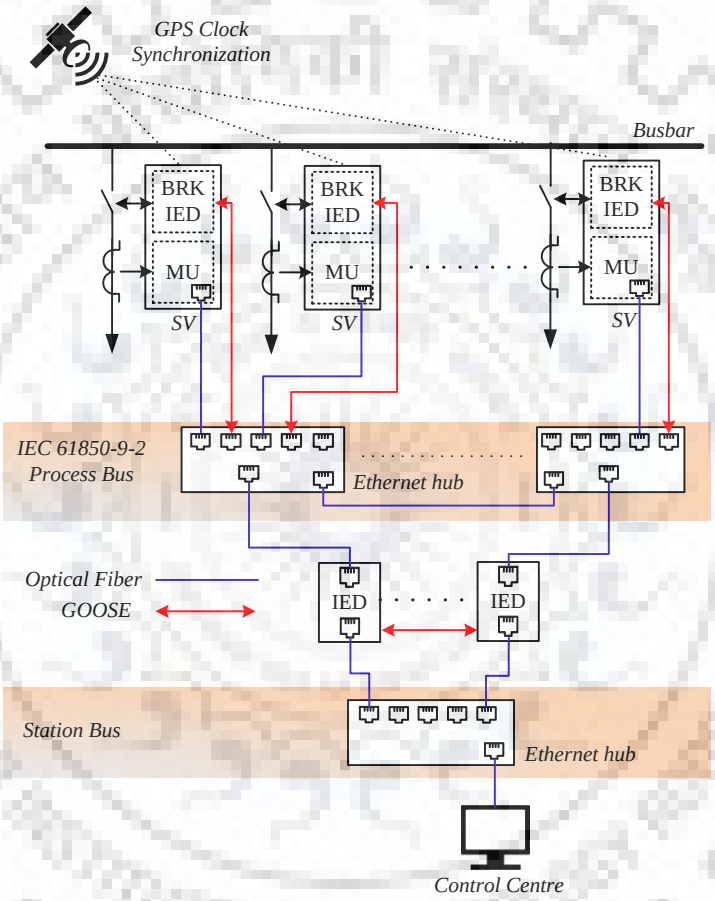

Fig. 5.4: Proposed architecture of 87BD based on IEC-61850

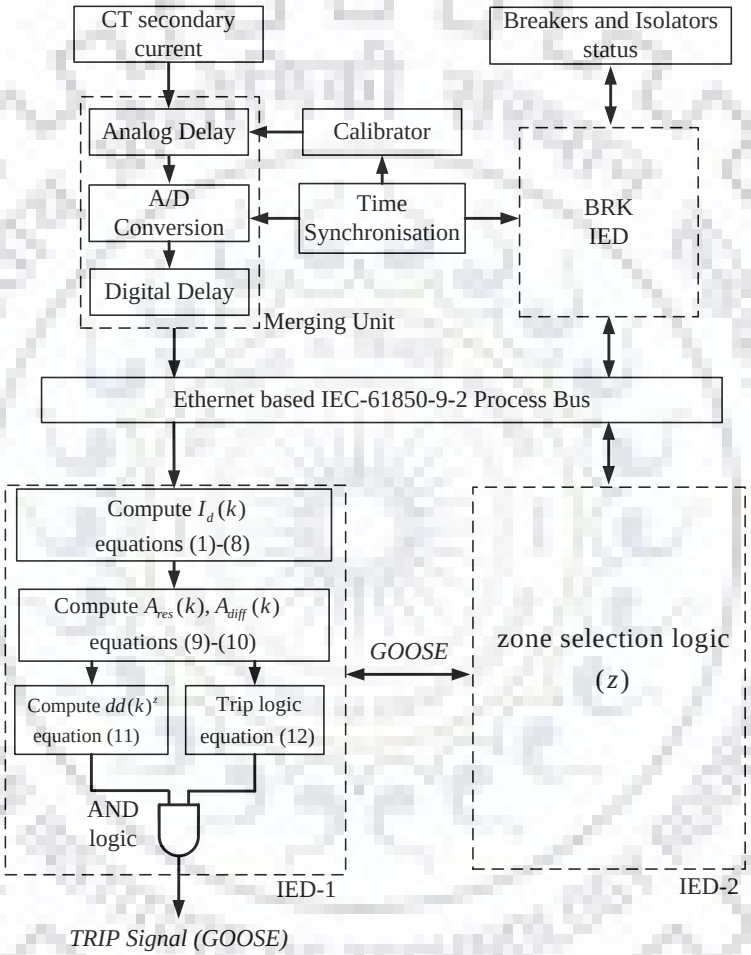

Fig. 5.5: Data flow for the proposed scheme.

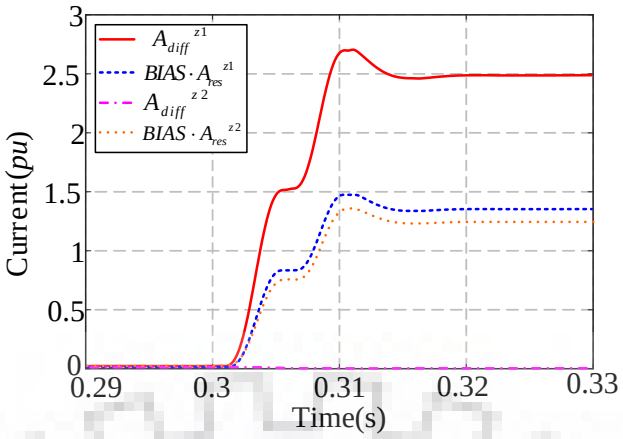

Fig. 5.6: Performance of 87BD for case 1.

5.6 Results and Discussions

In order to test the effectiveness of the proposed busbar protection scheme (87BD), a set of fault scenarios with wide variation in system and fault parameters such as fault type, fault resistance, fault inception angle, etc. have been simulated on the PSCAD model. The performance of 87BD has also been tested with various scenarios where the conventional and contemporary busbar protection schemes are most likely to malopearte.

5.6.1 Internal fault

Out of generality, a phase to ground (AG) fault is carried out on bus 1 (case 1). The performance of 87BD, in this case, is shown in Fig. 5.6. It can be observed that, after the fault inception, zone 1 trips and zone 2 restrains as ${A_{diff}}^{z1}$ remains greater than $(BIAS \cdot {A_{res}}^{z1})$ whereas there is no change in ${A_{diff}}^{z2}$ when compared to $(BIAS \cdot {A_{res}}^{z2})$. Moreover, the differential quantity crosses the restraining quantity within the first half cycle after fault inception. Hence, 87BD can provide fast and reliable response in case of internal faults.

5.6.2 External fault

Robustness of 87BD has been tested by simulating a three phase (ABC) fault on L2 at a distance of 1 km from Bus 1 (case 2). The response of 87BD (87BD) in this case is shown in Fig. 5.7. As observed in Fig. 5.7, the differential quantities $({A_{diff}}^{z1}$

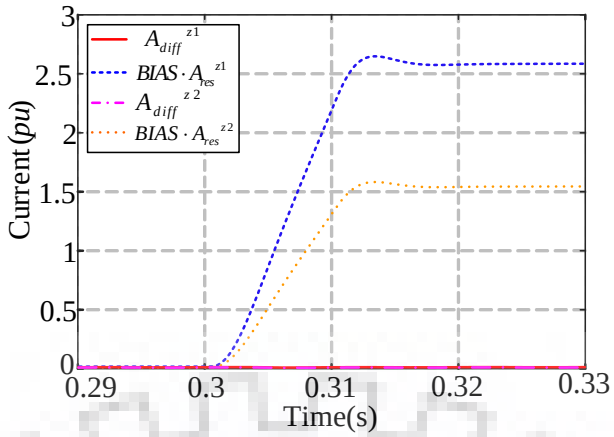

Fig. 5.7: Performance of 87BD for case 2.

and $A_{diff}{}^{z2}$) stay substantially below the restraining quantities ($BIAS \cdot A_{res}{}^{z1}$ and $BIAS \cdot A_{res}{}^{z2}$). Hence, 87BD provides high degrees of stability during external faults.

5.6.3 Performance in case of CT saturation

In case of SV based protection schemes, the lead resistance of the short physical wires connected between the CT secondary and MU input is less when compared to long wires connected between CT secondary and microprocessor based relays in conventional schemes. Though the chances are less, the effect of CT saturation can not be fully ignored in SV based protection schemes. In order to test the effect of CT saturation on the performance of the (87BD) and 87B, a three phase to ground (ABCG) fault is performed on line L2 at a distance of 1 km from bus 1 (case 3). To effectively replicate the CT saturation conditions, secondary burden of the CT has been increased 10 times.

The performance of 87BD for the aforementioned scenario is shown in Fig. 5.8 (a). It is to be noticed that though the value of differential quantity $A_{diff}{}^{z1}$ increases, it remains substantially below restraining quantity ($BIAS \cdot A_{res}{}^{z1}$). Hence, zone 1 relay restrains from tripping.

Fig. 5.8 (b) shows the response of phase-A relay of 87B. To stabilize the restraining current which oscillates in every half cycle, a smoothed version of restraining current ($\hat{I}_{res}^{z1}$) has been used. A moderate value of 0.6 has been set for $BIAS$ [99]. It is to be observed that, the value of I_{diff}^{z1} crosses the value of $BIAS \cdot \hat{I}_{res}^{z1}$ after the saturation free period of $1/8^{th}$ cycle [62] which blocks the fast mode (1-out-of-1) operation for a period of 150 ms. However, the slow mode (2-out-of-2) detects two counts in two

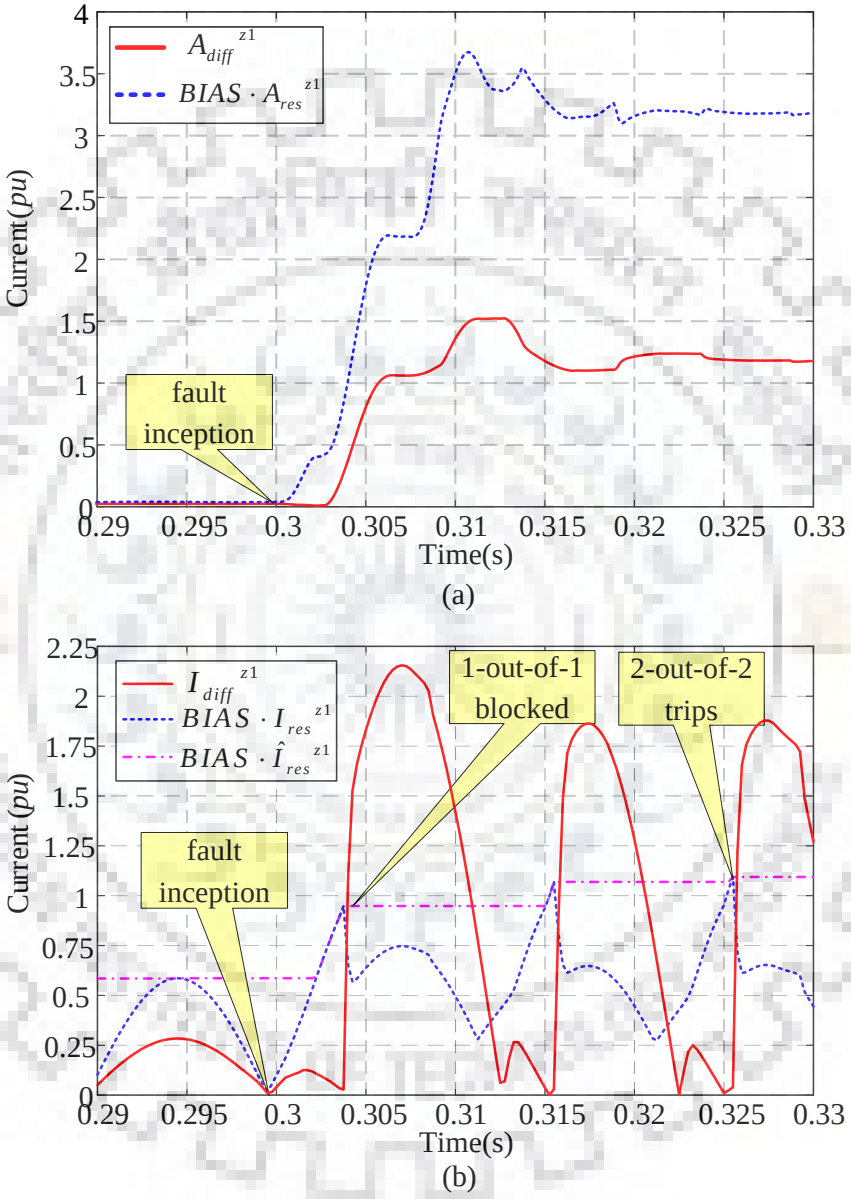

Fig. 5.8: Performance of (a) 87BD (b) 87B for case 3.

successive quarter cycles as I_{diff}^{z1} crosses the value of $BIAS \cdot \hat{I}_{res}^{z1}$. Hence, 87B eventually mal-operates.

5.6.4 Performance in case of high impedance faults

A high impedance fault (HIF) normally occurs when an overhead power line physically breaks and falls to the ground. Such faults are difficult to detect because they often draw small currents which cannot be detected by conventional differential protection. Furthermore, an electric arc accompanies HIFs, resulting in fire hazard, damage to electrical devices, and risk with human life. HIF detection and localization in electrical power systems has been traditionally a challenge for protection engineers. This is due to the nature of this kind of faults, basically their variability and relatively low-current levels compared to substation load currents. Power system disturbances like HIFs create underdamped oscillations. As the magnitude of distortion is small, transient frequency based schemes perform poorly in this situation [107].

To assess the comparative performances between 87BD, 87B, and wavelet-based differential protection scheme (87BW) [49] in the case of HIFs, a single phase to ground (AG) fault is simulated on bus 1 with a fault resistance of 200 ohms (case 4). The differential and restraining energy coefficients (ε_{diff}^{z1}, ε_{res}^{z1}) are calculated from the scale-1 detailed wavelet coefficients derived from the Db4 mother wavelet [108]. To test the sensitivity, $BIAS$ value has been kept the same (0.6) for all schemes. Performances of 87BD, 87B and 87BW schemes for this scenario are shown in Fig. 5.9 (a), (b), and (c), respectively. As observed in Fig. 5.9, the proposed 87BD scheme has been able to issue a trip signal as the differential quantity crosses the restraining quantity. On the contrary, both 87B and 87BW are unable to detect the fault as the differential quantities remain low when compared to the restraining quantities. Hence, 87BD is found to be more sensitive than 87B and 87BW for high impedance internal faults.

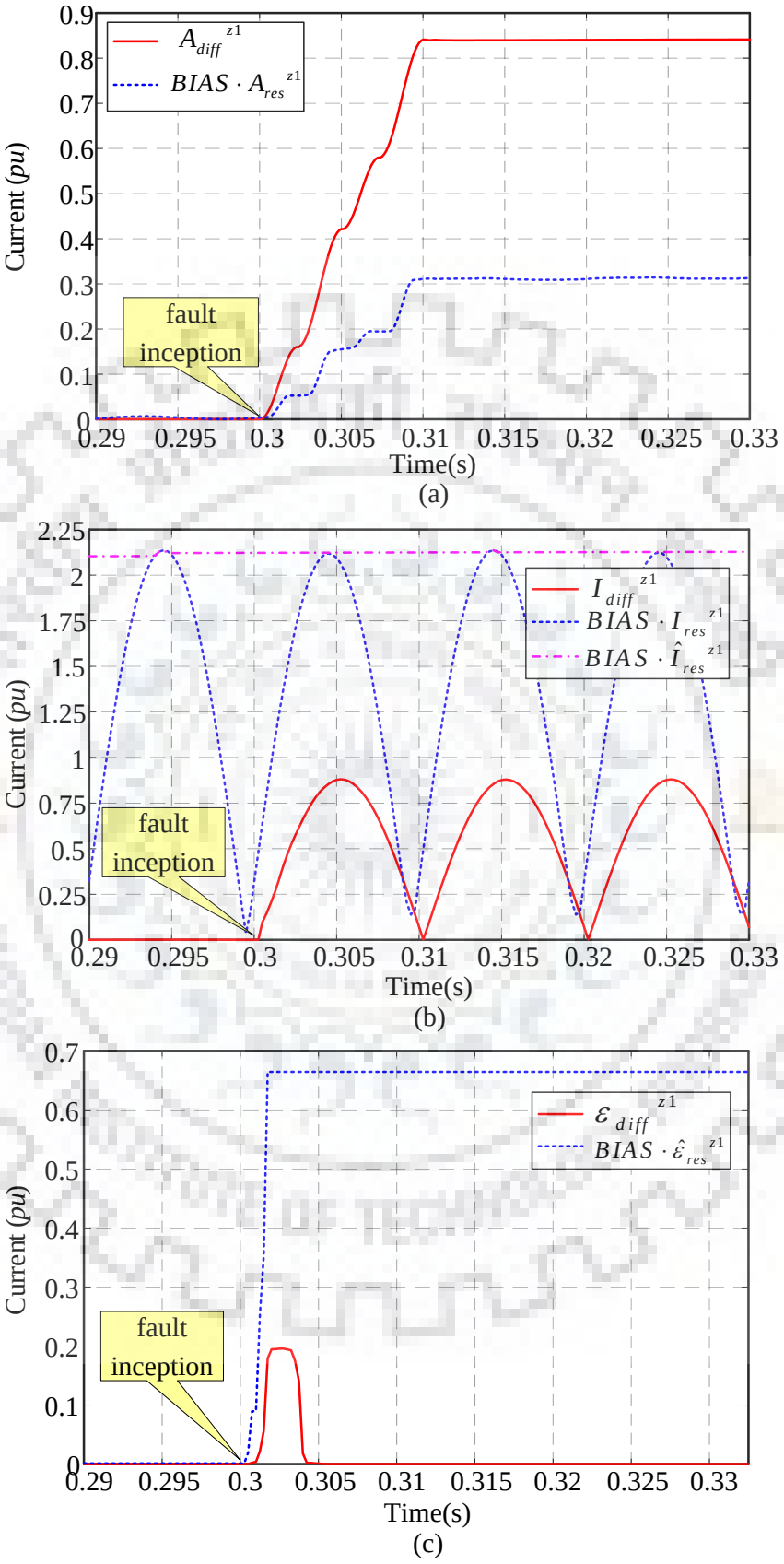

Fig. 5.9: Performance of (a) 87BD (b) 87B (c) 87BW during case 4.

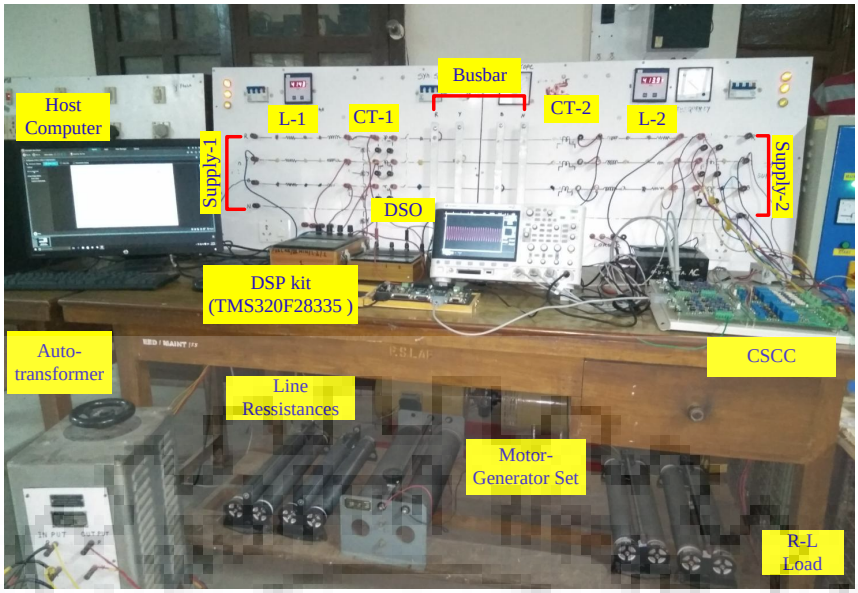

Fig. 5.10: Developed laboratory experimental setup.

5.7 Testing of 87BD on laboratory test-bench

5.7.1 Development of the laboratory test-bench

In order to validate 87BD, a laboratory test-bench, as shown in Fig. 5.10, has been developed. The available power supply (440 V, 3-ϕ, 50 Hz) and a motor-generator set (440 V, 2.2 kW/ 3-hp, 50 Hz) have been utilized as two supply sources. CTs (10/5 A, 25 VA) have been installed on each of the phases to acquire current signals. The Current Signal Conditioning Circuit (CSCC) acquires the current signals from each of these CTs and converts into equivalent voltage signals (3V peak-to-peak). These signals are sampled at 4 kHz sampling frequency by the ADC in the TMS320F28335 DSP processor. The DSP processor has also been interfaced with a host computer via the XDS510PP+ emulator pod. The proposed algorithm has been composed in Code Composer Studio (CCS 5.1) with MATLAB interface.

5.7.2 Test-bench results

An internal AG fault with a fault resistance of 25 Ω has been performed on the busbar (case 5). The phase-A CT secondary current waveforms of the incoming (L-1) and outgoing (L-2) lines, captured by the DSO, are depicted in Fig. 5.11 (a). Fig. 5.11 (b) shows the response of the proposed scheme (87BD) for the aforementioned scenario. It is evident from Fig. 5.11 (b) that a trip signal has been generated as the value of A_{diff}

becomes more than $(BIAS \cdot A_{res})$ after the inception of fault.

An A-G external fault is simulated on line L-2 with a fault resistance of 30 Ω (case 6). To replicate saturation conditions, an extra resistance of 10 Ω has been added to the CT secondary circuit. The phase-A current waveforms of L-1 and L-2 under the aforementioned scenario are shown in Fig. 5.12 (a). As observed in Fig. 5.12 (a), the current waveform of the L2 has been distorted due to saturation. The results obtained from 87BD in this case is shown in Fig. 5.12 (b). It is evident from Fig. 5.12 (b) that 87BD restrains from tripping as the differential component remains substantially below the restraining component.

5.7.3 Response time

Table 5.2 shows the responses of 87BD in terms of tripping time for different faults performed on the laboratory test-bench by varying the fault type and fault resistance. It is to be noted from Table 5.2 that the average tripping time of 87BD is of the order of 3 ms. Delays due to the implementation of IEC-61850 are because of: (1) the introduced latency for the transfer of SVs in frames, and, (2) path delay due to the optical fibres in the Ethernet framework. The introduced latency can be extended up to a maximum of 250 μs (4 kHz sampling frequency). The path delay would not be exceeding $5\mu s$ for 1000 m length in a 1000 Mbps Ethernet framework [101]. Taking the delay due to the inter IED communications into account the maximum delay would not be more than 1 ms. Hence, 87BD has a response time in the order of 4 ms. Modern state-of-the-art instantaneous busbar differential relays have response time in the order of $1/4^{th}$ cycle (5 ms). Though transient based schemes have reported 1 ms tripping time, these schemes may fail during several fault scenarios with overdamped oscillations. So, these schemes are implemented in supplement to the main protection scheme. In this regard, 87BD provides reliable protection with faster response time than the modern protection schemes.

5.7.4 Advantages of the proposed scheme

The proposed scheme is tested through a wide range of fault scenarios and the results signify the following advantages:

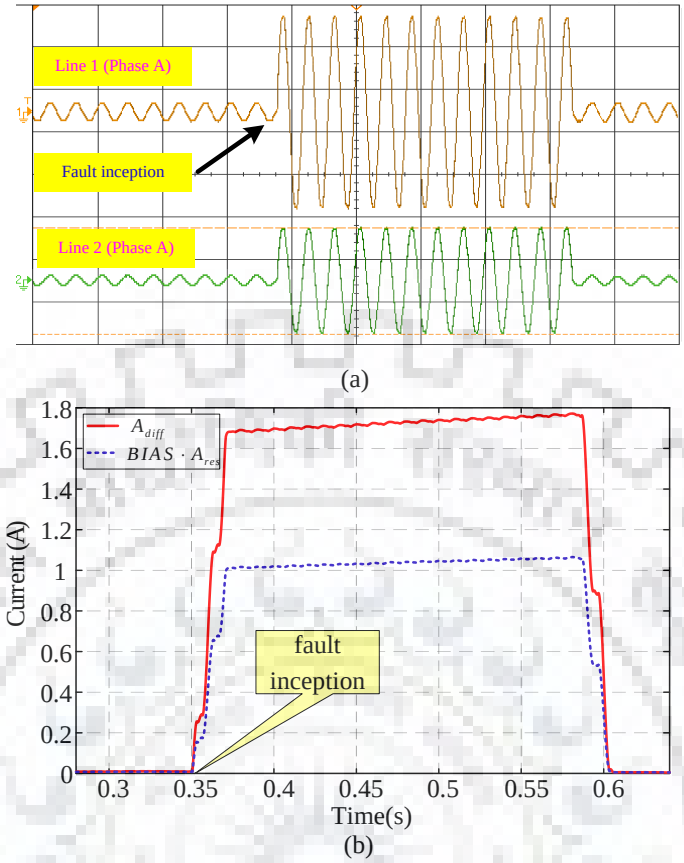

Fig. 5.11: Results obtained from laboratory prototype in case 5 : (a) Current waveforms (b) Response of 87BD.

Table 5.2: Response of 87BD for faults performed on the test-bench

Fault Parameters			87BD Response	Tripping Time
Zone	Type	Resistance		
Internal	LG	25 Ω	Trip	2.5 ms
		30 Ω	Trip	3.25 ms
		40 Ω	Trip	3.5 ms
		45 Ω	Trip	3.5 ms
Internal	LL	0.1 Ω	Trip	4 ms
Internal	LLG	25 Ω	Trip	2.75 ms
External	LG	25 Ω	Restrain	–
		30 Ω	Restrain	–
		40 Ω	Restrain	–
		45 Ω	Restrain	–
External	LL	0.1 Ω	Restrain	–
External	LLG	25 Ω	Restrain	–

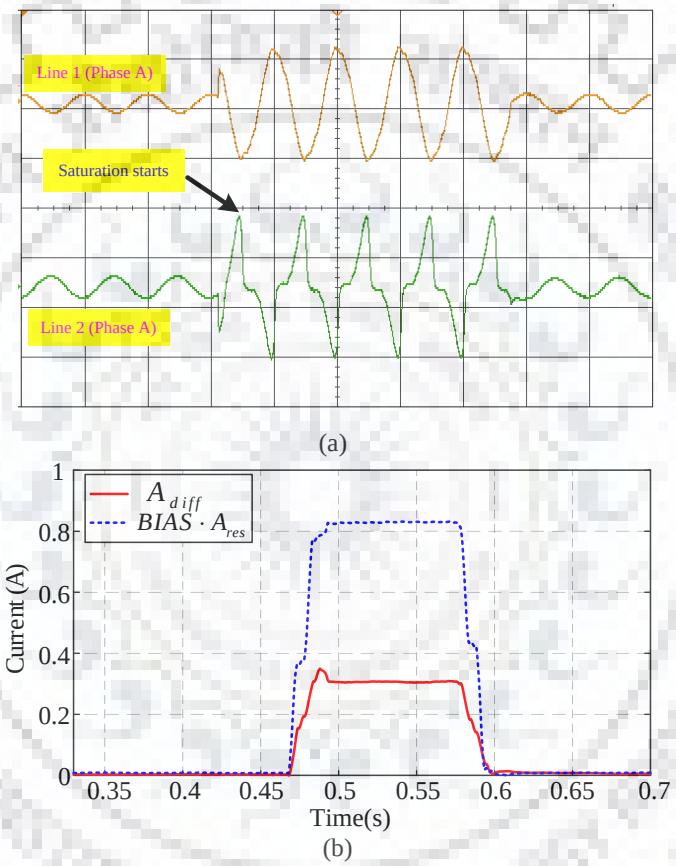

Fig. 5.12: Results obtained from laboratory prototype in case 6 : (a) Current waveforms (b) Response of 87BD.

- The proposed scheme requires only one relay in terms of d-axis current components whereas 87B require three phase segregated relays (a, b, and c). Hence, 87BD is more reliable and cost-effective.

- TW and wavelet-based schemes require a very high sampling frequency to extract transient frequency components. In some cases, the conventional CT or CCVTs do not produce appropriate frequency response in high frequency ranges. Moreover, high frequency signals are prone to noise interference. On the contrary, derivation of d-axis current depends upon components in terms of power frequency, and hence, high sampling frequency is not essentially required. It marginalizes the computational requirements and the possibility of noise interference.

- Performances of wavelet-based schemes are affected by the choice of mother wavelet function and the level of decomposition. On the contrary, 87BD introduces a simpler approach with less computational burden. It does not require downsampling of the signal as in the case of wavelet-based schemes. The improved comprehensibility creates the possibility of on-chip implementation.

- The results shown in the previous subsection suggest that the 87BD outperforms 87B and a wavelet-based differential scheme (87BW) in detecting HIFs and maintaining stability against severe CT saturation scenarios. The fault detection time is also improved as it does not require phasor computation or complex post-processing.

5.8 Conclusion

In this chapter, a new busbar protection scheme based on the direct-axis components of current has been discussed. The CT secondary current signals are mapped into the differential and restraining components. The performance of the proposed scheme has been tested on a set of diversified fault scenarios. 87BD has been compared with 87B and wavelet-based differential scheme (87BW) where it shows better sensitivity in detecting HIFs and higher stability in case of CT saturation scenarios. The authenticity of 87BD has also been validated on a laboratory test-bench. The proposed

scheme provides better performance with less computational complexity and data requirements. The feasibility of the proposed scheme for SV based IEC-61850 process bus implementation has been discussed. As the number of relay requirements are less, the proposed scheme can be implemented in large substations with more number of bay units. In terms of operating times, the proposed scheme is on par with the modern state-of-the-art relays.

Chapter 6

Improved Breaker-failure protection based on Numeric Analysis

The previous chapters see developments of improved busbar protection algorithms in terms of speed, reliability, stability and feasibility for practical implementation. In the last chapter, a sampled value based busbar protection scheme with the feasibility of dynamic zone selection has been presented. Noteworthily, the statuses of isolator and circuit breaker used for dynamic zone selection can be utilized for breaker failure protection (BFP) function. This encourages development of breaker-failure function inside the busbar relay. It will eliminate the common functionality and minimize the wiring requirements. In this regard, this chapter discusses development of a new breaker-failure protection function (BFPN) to prevent the mal-operation arising because of subsidence current. The algorithm development using numerical analysis, results and comparative analysis with existing schemes has been discussed showcased.

6.1 Introduction

As a part of local backup strategy, BFP is called upon when the CB fails to clear a fault. In this situation, the BFP isolates the fault by opening the adjacent CBs. The same can be achieved by opening the remote end CBs as a part of remote backup strategy. However, it results in forced curtailment of some of the loads and adds significant delay to fault clearance time because of the involvement of direct transfer trip command through communication channel [63]. Hence, as a local solution, integration

of BFP function inside commercial relays in substation protection applications has gained momentum in the recent past [9, 64, 65, 109].

Duplication of CBs in substations is not realistic due to economic and operational constraints. In the event of failure of a breaker, adjacent breakers need to be called in to isolate the fault. Typically, a BFP function is integrated within commercial relays to monitor such situations. However, these functions are prone to mal-operation because of subsidence in CT resulting from faults with significant decaying DC components. To this end, a reliable reset algorithm for the BFP function is presented in this chapter. After measuring the decaying DC component within a one-cycle moving window, the proposed algorithm accurately distinguishes between the alternating pattern of fault current and exponential decaying pattern in subsidence current. Its performance remains unaffected during the change in fault current level, decaying dc component, CT saturation, level of subsidence and random noise. Results from simulation as well as laboratory setup indicate that the proposed algorithm can prevent the mal-operation of an existing BFP scheme in the conventional relay with safety margin in the range of 20-40%. A comparative evaluation with available techniques testifies its superiority.

6.2 State-of-the-art

Keeping the stability and operational consequences of a fault in EHV substations in mind, the narrower margin for fault clearance is always preferred. Some of the utilities mandate further reduction of this margin. Hence, it has become more difficult to accommodate the BFP trip time. The selection of excellent mathematical tools to provide reliable BFP has the utmost priority in this regard. Traditionally, BFP is achieved either by physically monitoring the auxiliary contacts or by checking current flow in the CB. The former method is typically troublesome and has been historically proved to be incorrect. The latter one checks two inputs: (i) the trip signal from the protective relay (BFI), (ii) an overcurrent element (50BF) with threshold set at a fraction of CT nominal current. A delay timer (62) is set at the duration of the normal clearing time of the breaker plus a safety margin. If both inputs remain high for this predefined duration, the BFP issues trip signal to the adjacent breakers [10]. Any false tripping inside the relay may lead to large scale power outage or possible

blackouts [11, 105, 110].

Subsidence current in CT secondary presents the main challenge to the BFP function. Momentary interruption of current by the breaker following an offset decaying fault current results in subsidence current in the CT secondary. It energizes the overcurrent element which may lead to subsequent mal-operation of the BFP function. It is a peculiar situation as BFP trips the adjacent breakers when the fault has been cleared by the breaker itself. This can lead to unnecessary power outages or possible blackout of the system. To this end, a reset algorithm by analyzing the CT secondary current passed through a pair of orthogonal sine and cosine filters is proposed in [66]. Subsequently, a BFP reset scheme by identifying the crossing points of CT secondary current and its derivative signals was proposed in [67]. Though these schemes provide reliable reset signals to prevent the mal-operation of BFP function, they may not provide desirable results particularly when the fault current consists of a higher degree of DC decaying component followed by longer subsidence current.

6.3 Issues in Breaker Failure Protection

When the fault current is successfully interrupted by a CB, the primary current in the line CT instantaneously becomes zero. However, flux in the core of the CT is not momentarily neutralized. Moreover, if the fault current consists of significant DC components, then, the flux decay introduces unidirectional current in the CT secondary. In case of saturation of the CT, significant subsidence current flows in the CT secondary [73].

The magnitude estimators such as DFT or RMS see part of the unidirectional subsidence current as legitimate fundamental frequency magnitude. In order to understand this phenomenon, a typical timeline diagram of a fault current waveform interrupted by the CB is shown in Fig. 6.1. The primary relay based on the RMS magnitude of the current takes about one cycle for the trip decision. An additional half-cycle delay incurs in the auxiliary relay tripping circuits and communication process. Hence, the BFI element is activated after 1.5 cycles of fault inception. Upon receiving the trip signal, the CB normally clears the fault within 3 cycles [10]. In the meantime, the breaker failure threshold element (50BF) picks up after a short delay

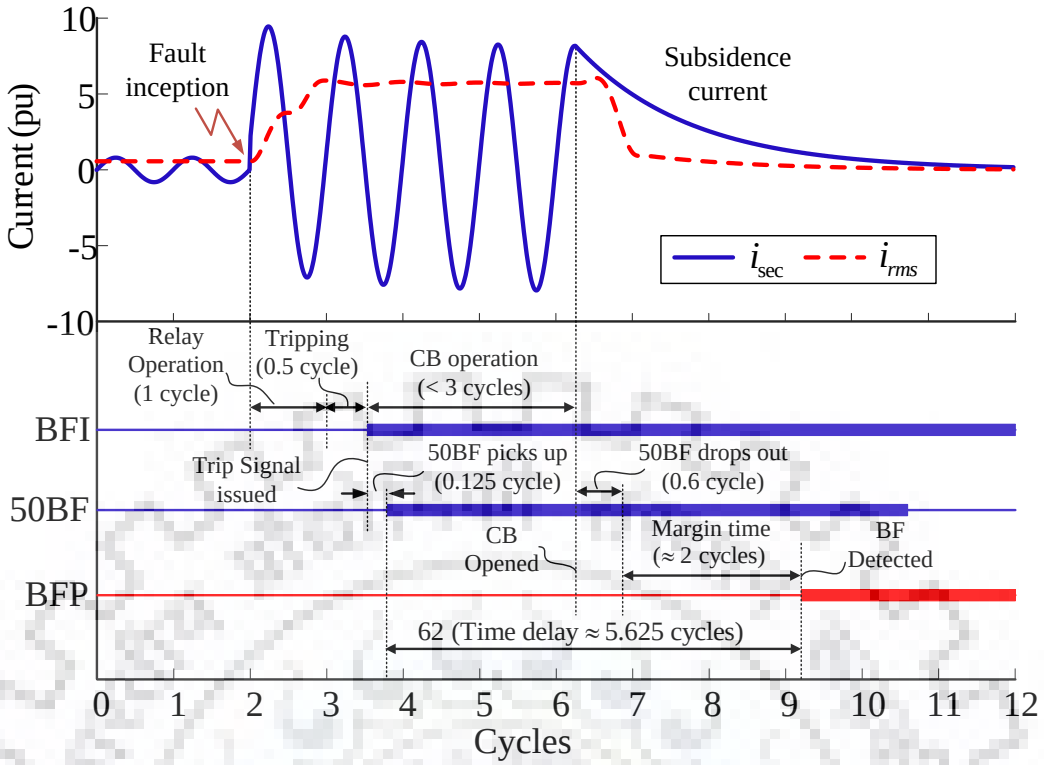

Fig. 6.1: Time line of a fault interrupted by CB and following BF operation.

(0.125 cycle). After the opening of the auxiliary contacts of the CB (52a), the current magnitude (RMS) decreases. The expected time limit for it to drop out below the preset 50BF threshold is 0.6 cycles. As observed in Fig. 6.1, the subsidence current in the CT secondary does not allow the current magnitude to drop out immediately. If this delay crosses a predefined margin (≈ 2 cycles), the BFP issues a trip signal and subsequently, adjacent breakers are unnecessarily tripped. In similar terms, if both BFI and 50BF function remain energized for critical fault clearance duration (≈ 5.625 cycles), the BFP function is activated. Historically, subsidence currents with longer duration have played the main culprit in mal-operation of BFP [111]. This situation can initiate cascade tripping situations and possible large-scale blackout scenario [112].

6.4 Proposed Algorithm

A fault current waveform, as shown in Fig. 6.1, can be realized in two parts. The first part is the sinusoidal fault current with decaying DC component and the second part is the subsidence current in CT secondary with exponential decaying components. The main objective of the proposed BFP (namely, BFPN) scheme is to differentiate

between the alternating and decaying waveform patterns during the fault period and decaying pattern after the fault is cleared.

6.4.1 During Fault Period

Assuming that the fault current consists of a fundamental frequency component, harmonics up to order N_h and a decaying DC component, the current in the CT secondary can be expressed as:

$$\begin{aligned} i(t_n) &= i_s(t_n) + i_{dc}(t_n) \\ &= \sum_{k=1}^{N_h} I_k \sin(nk\omega\Delta T + \phi_k) + I_0 e^{-n\Delta T/\tau_1} \end{aligned} \tag{6.1}$$

where, $i_s(t_n)$ and $i_{dc}(t_n)$ are the sinusoidal and decaying DC components of n-th sample discretized current and $t_n = n\Delta T$ in which ΔT is the time interval between two consecutive samples. I_k and ϕ_k are the magnitude and phase of kth harmonic current and $\omega = 2\pi 50$ rad/s. I_0 and τ_1 are the initial magnitude and time constant of $i_{dc}(t_n)$.

By calculating the summation of fault current over one cycle, the summation value (s) at nth sample *i.e.* $s(t_n)$ can be obtained as:

$$\begin{aligned} s(t_n) &= \sum_{z=n-N+1}^{n} i_s(z\Delta T) + i_{dc}(z\Delta T) \\ &= \sum_{z=n-N+1}^{n} i_{dc}(z\Delta T) \end{aligned} \tag{6.2}$$

where, N is the number of samples in a cycle.

Equation (6.2) holds true as the summation of sinusoidal components over one cycle is zero. Further, by applying integration, equation (6.2) can be written as:

$$\begin{aligned} s(t_n) &= \sum_{z=n-N+1}^{n} I_0 e^{-z\Delta T/\tau_1} \\ &= -I_0(\tau_1/\Delta T)\left[e^{-n\Delta T/\tau_1} - e^{-(n-N+1)\Delta T/\tau_1}\right] \\ &= -I_0(\tau_1/\Delta T)e^{-n\Delta T/\tau_1}\left[1 - e^{(N-1)\Delta T/\tau_1}\right] \end{aligned} \tag{6.3}$$

Likewise, the summation value for $(n-1)$th sample *i.e.* $s(t_{n-1})$ is calculated as:

$$\begin{aligned} s(t_{n-1}) &= \sum_{z=(n-1)-N+1}^{n-1} I_0 e^{-z\Delta T/\tau_1} \\ &= -I_0(\tau_1/\Delta T)\left[e^{-(n-1)\Delta T/\tau_1} - e^{-((n-1)-N+1)\Delta T/\tau_1}\right] \\ &= -I_0(\tau_1/\Delta T)\left[e^{-n\Delta T/\tau_1} - e^{-(n-N+1)\Delta T/\tau_1}\right]e^{\Delta T/\tau_1} \\ &= s(t_n)e^{\Delta T/\tau_1} \end{aligned} \tag{6.4}$$

Applying Taylor series expansion, the ratio between $s(t_n)$ and $s(t_{n-1})$ is calculated as:

$$\frac{s(t_n)}{s(t_{n-1})} = e^{-\Delta T/\tau_1} = 1 - (\Delta T/\tau_1) + \frac{(-\Delta T/\tau_1)^2}{2!} + \dots \tag{6.5}$$

The higher order terms can be neglected due to small value of ΔT. Hence, equation (6.5) can be written as,

$$\frac{s(t_n)}{s(t_{n-1})} = 1 - (\Delta T/\tau_1); \text{and,} \tau_1 = \frac{\Delta T}{1 - \left[s(t_n)/s(t_{n-1})\right]} \tag{6.6}$$

It is to be noted from equation (6.6) that the decaying time constant can be calculated with any two consecutive samples of summation values *i.e* $s(t_n)$ and $s(t_{n-1})$.

As observed from equations (6.1)-(6.4), values of both $i_{dc}(t_n)$ and $s(t_n)$ decrease with the same decaying rate $e^{-\Delta T/\tau_1}$. In this case, if the fault current is passed through a moving average filter, it calculates a part of the decaying DC current $i_{dc}^{MA}(t_n)$.

$$i(t_n) \xrightarrow{h_{MA}} i_{dc}^{MA}(t_n); \quad h_{MA} = \frac{1}{N} \tag{6.7}$$

where, h_{MA} are the filter coefficients. Then, $i_{dc}^{MA}(t_n)$ is calculated as:

$$i_{dc}^{MA}(t_n) = \sum_{z=n-N+1}^{n} \frac{1}{N} \cdot i(t_z) = \frac{1}{N} \sum_{z=n-N+1}^{n} i_{dc}(t_z) \tag{6.8}$$

The percentage error (ϵ) between $i_{dc}(t_n)$ and $i_{dc}^{MA}(t_n)$ is calculated in the following

equations:

$$\begin{aligned}\epsilon(t_n) &= \frac{i_{dc}(t_n) - i_{dc}^{MA}(t_n)}{i_{dc}(t_n)} \\ &= \frac{I_0 e^{-n\Delta T/\tau_1} - \frac{1}{N}\sum_{z=n-N+1}^{n} I_0 e^{-z\Delta T/\tau_1}}{I_0 e^{-n\Delta T/\tau_1}} \\ &= \frac{I_0 e^{-n\Delta T/\tau_1} + \frac{I_0}{N}\frac{\tau_1}{\Delta T} e^{-n\Delta T/\tau_1}\left[1 - e^{(N-1)\Delta T/\tau_1}\right]}{I_0 e^{-n\Delta T/\tau_1}} \\ &= 1 + \frac{\tau_1}{N\Delta T}\left[1 - e^{(N-1)\Delta T/\tau_1}\right]\end{aligned} \tag{6.9}$$

It is observed from equation (6.9), that $\epsilon(t_n)$ is a constant term and all the terms (τ_1, N, and ΔT) are known. It also signifies that the fault current has a uniform error value which depends on the sampling frequency, moving window length and time constant of decaying DC. After the calculation of $\epsilon(t_n)$, the actual value of DC component $i_{dc}(t_n)$ can be calculated by multiplying a correction factor (CF) to the output of the moving average filter $i_{dc}^{MA}(t_n)$ as defined in the following equation:

$$i_{dc}(t_n) = CF(t_n) \cdot i_{dc}^{MA}(t_n); \quad CF(t_n) = \frac{1}{1 - \epsilon(t_n)} \tag{6.10}$$

After the calculation of the DC component, the sinusoidal component is calculated as follows:

$$i_s(t_n) = i(t_n) - i_{dc}(t_n) \tag{6.11}$$

6.4.2 After Fault Clearance

After opening the contacts of the CB, the subsidence current present in the secondary of the CT can be represented in the form of an exponential function as follows:

$$i(t_n) = I_1 e^{-n\Delta T/\tau_2} \tag{6.12}$$

where I_1 is the magnitude of CT secondary current when the fault is cleared and τ_2 is the decaying time constant. Depending upon the CT secondary inductance and resistance values, the subsidence current may extend for a longer duration.

It is worthwhile to note that a fault cleared in the positive half of the cycle results in subsidence current with negative derivative and vice versa. However, equation (6.12) holds good for both the cases. Moreover, equations (6.3)-(6.9) are true when applied

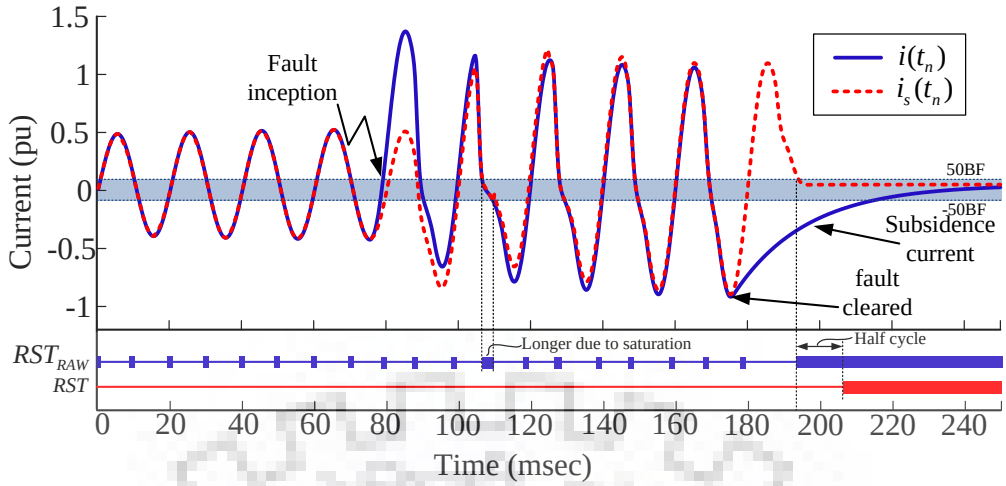

Fig. 6.2: Generation of RST_{RAW} and RST signal in case of CT saturation.

for equation (6.12). The sinusoidal component of current $i_s(t_n)$ would be zero in case of pure decaying subsidence current. Considering, the 50BF threshold is set at a value of 10% of CT secondary nominal current, a reset signal RST_{RAW} is asserted if the instantaneous value of $i_s(t_n)$ lies within the range of -50BF to 50BF which is given by,

$$RST_{RAW}(n) = \begin{cases} 1, & if\ i_s(t_n) \in [-50BF, 50BF] \\ 0, & otherwise \end{cases} \tag{6.13}$$

Fig. 6.2 shows the generation of RST_{RAW} signal for a saturated CT secondary current signal. It can be observed that during the normal operating conditions, the RST_{RAW} signal is asserted for short duration in every cycle when the sinusoidal component of current $i_s(t_n)$ stays below $0.1 \times I_{NOM}$. It stays for a longer duration because of the phase advancement in CT saturation conditions. Moreover, any random noise in the signal may reset the existing BFP function. Hence, the RST_{RAW} signal is monitored for $N/2$ samples, the rationale being that the phase angle advancement may extend up to 90° in case of heavy CT saturation. Then, the RST is asserted as per the following condition:

$$RST(n) = \begin{cases} 1, & if\ \sum_{k=n-N/2+1}^{n} RST_{RAW}(k) = N/2 \\ 0, & otherwise \end{cases} \tag{6.14}$$

6.4.3 Neutralization of Random Noise

Real-time signals from CTs may be contaminated with noise because of communication channels or other signal processing devices. It may adversely affect the proposed scheme as the RST signal is based on the instantaneous value of the sinusoidal component of current. In order to neutralize the effect of random noise when the value of $i_s(t_n)$ lies in the 50BF to -50BF bracket, a de-noised signal ($i_s^{dn}(t_n)$) has been generated by utilizing the routine described in Algorithm 1. At first, the samples within the bracket

Algorithm 1: Denoising of $i_s(t_n)$; $i_s(t_n) \rightarrow i_s^{dn}(t_n)$

Data: $i_s(t_n)$, $50BF$
Result: $i_s^{dn}(t_n)$
if $i_s(t_n) \leq 50BF$ **and** $i_s(t_n) \geq -50BF$ **then**
  $i_s^{dn}(t_n) = 0$;
else if $i_s(t_n) > 50BF$ **then**
  $i_s^{dn}(t_n) = i_s(t_n) - 50BF$;
else
  $i_s^{dn}(t_n) = -(-50BF - i_s(t_n))$;
end
$i_s^{dn}(t_n) \leftarrow 0.5\left[i_s^{dn}(t_n) + i_s^{dn}(t_{n-1})\right]$

are assigned 0 and then the difference between the 50BF boundaries and samples is shrunk. As a result, the samples at a proximity of the boundaries are now positioned within the bracket. Then a moving average between every two consecutive samples further softens the waveform. The denoising process adds only one sample delay in the moving average process and does not affect the overall performance of the scheme. The results of the denoising process are discussed in section 6.5.5.

6.5 Performance Evaluation

The performance of the proposed algorithm has been evaluated by developing an existing substation model with two incoming lines and one outgoing line, as shown in Fig. 6.3, using PSCAD/EMTDC software [79]. The system parameters are given in Appendix-VI. The test waveforms have been acquired from the CT secondary of the outgoing line (CT-3). An extensive range of test waveforms has been simulated reflecting variability in system and fault parameters such as fault current level, decaying dc component, CT saturation, level of subsidence and random noise. A sampling fre-

quency of 4 kHz with the system nominal frequency of 50 Hz has been utilized to acquire the CT secondary waveforms.

Output of the ADC, as discretized CT secondary current samples, is exported to MATLAB environment where the control logic of BFPN has been developed. The conventional DFT algorithm has been used to estimate the RMS magnitude of the current signal (i_{rms}). The fault detection unit sends the TRIP signal to CB-3 when the overcurrent element picks up. Subsequently, the breaker failure initiation (BFI) and breaker failure threshold (50BF) signals are activated. Upon positive output from the signals, BFI and 50BF for a continuous duration (62) of 5.625 cycles, the breaker failure protection element (BFP) is asserted. To generate the RST signal, the CT secondary current samples, with one cycle buffers, calculate the periodic summation signal (s) and the output of moving average filter (i_{dc}^{MA}). Subsequently, the time constant (τ), percentage error value (ϵ), and correction factor are calculated based on equations (6.5)-(6.10). Then, by multiplying the correction factor to the output of moving average filter (i_{dc}^{MA}), the exact DC component of current (i_{dc}) is calculated. The sinusoidal component of current (i_s) is obtained by extracting the DC component of current from the instantaneous current value (i). Finally, with the help of equations (6.13) and (6.14), RST signal is generated. In the case of subsidence current, the proposed scheme asserts the RST signal that resets the BFP signal and produces a new BFP signal (BFPN). Hence, mal-operation of nearby CBs and possible outage is prevented. Results obtained from the proposed algorithm are discussed in the following subsections.

6.5.1 Fault Current Level (Case 1)

The protective class CTs can faithfully transform the fault current up to 20 times the rated current within the specified error limit [113]. On the contrary, the breaker failure threshold (50BF) is typically set at 10% of the CT nominal current. Hence, in case of heavy fault scenarios, the fault current may reach up to 200 times the breaker failure threshold (50BF). Clearance of a fault at such a high magnitude usually creates longer subsidence, which may exceed the critical fault clearance time (62). To test the performance of BFPN in such scenarios, a solid single phase to ground (A-G) fault is simulated on the test system and the results given by BFPN are shown in Fig. 6.4. It is to be noted from Fig. 6.4 that due to the high fault current and following subsidence,

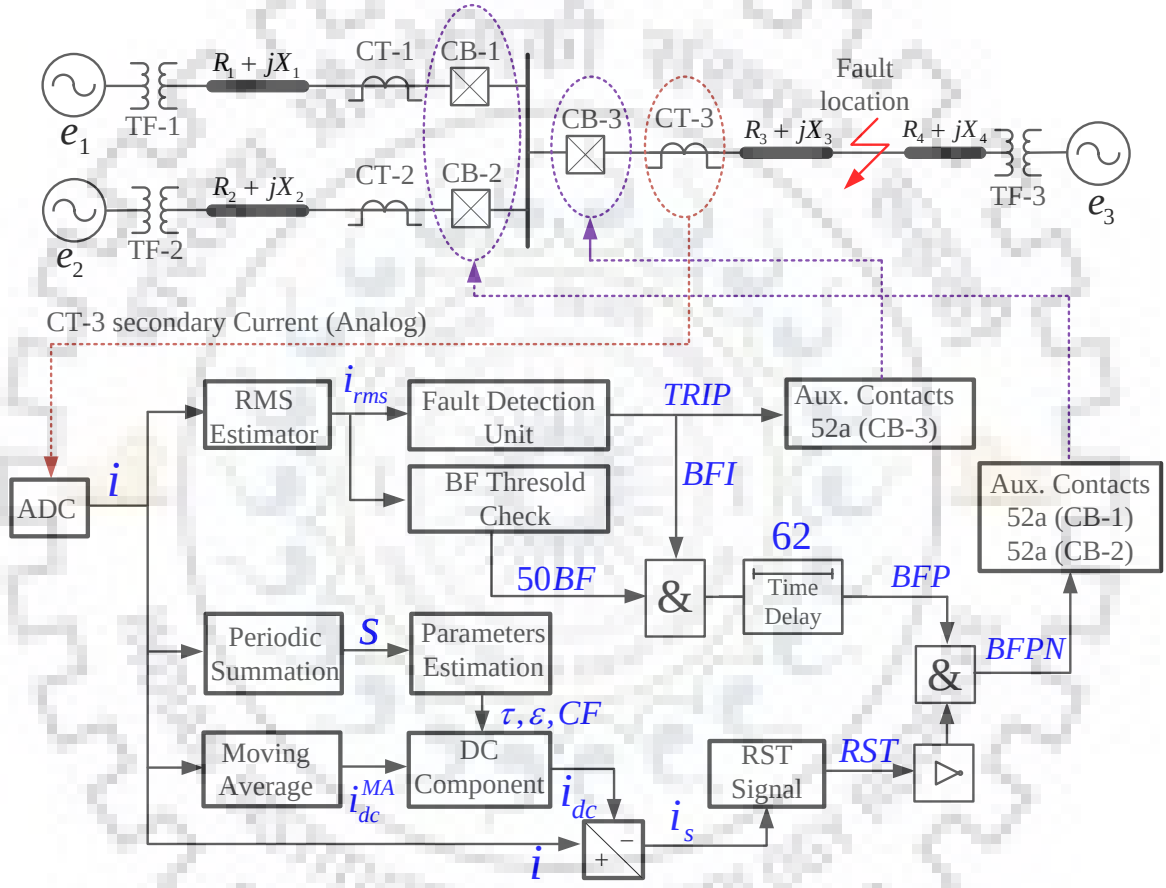

Fig. 6.3: simulation model and control logic of the proposed scheme (BFPN).

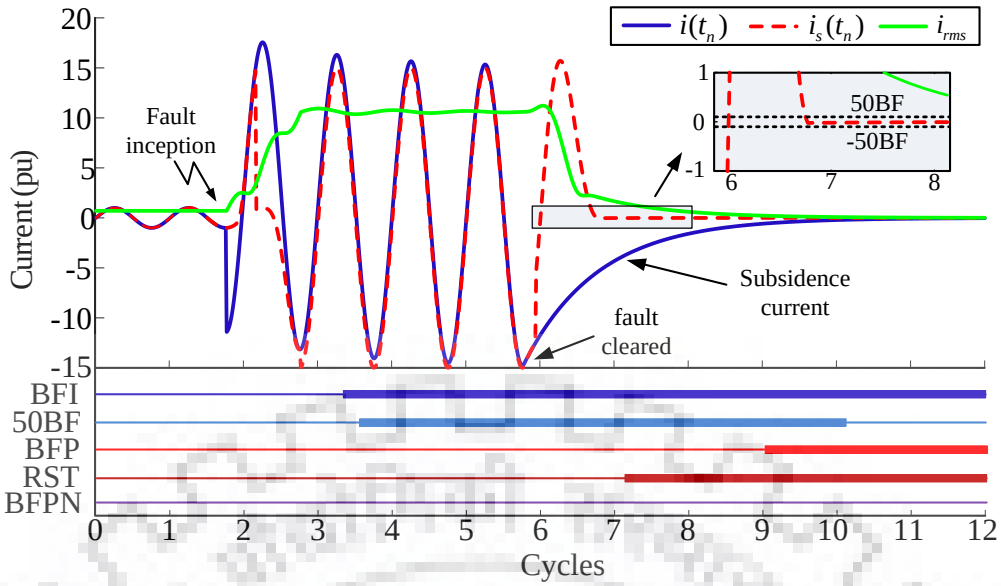

Fig. 6.4: Results obtained in Case 1.

the 50BF element takes a longer duration to drop down, which falsely activates the existing BFP function. Conversely, the proposed scheme executes a prior reset signal (RST) as the sinusoidal current component $i_s(t_n)$ drops down into the bracket of 50BF and -50BF for more than $N/2$ samples. Hence, the BFPN function shows no activity and a mal-operation is prevented.

6.5.2 Decaying DC Component (Case 2)

The decaying component of current consists of a large range of system frequencies. Hence, the conventional phasor estimation algorithms fail to calculate the exact RMS magnitude in most of the cases. The decaying component in fault current depends on the X/R ratio of the transmission line between the fault location and the CT. The RMS estimator, in case of substantial offset current, usually takes longer duration to drop down, which eventually expires the timer (62) duration. The performance of the proposed algorithm has been evaluated by increasing X/R ratio of the line under consideration to 10 times its existing value. The results obtained in this scenario are shown in Fig. 6.5. It can be observed from Fig. 6.5 that the fault current consists of a significant decaying component. Both the BFI and 50BF elements remain high for a duration more than pre-set time duration (62) and the existing BFP function trips. However, a prior RST signal has been executed by BFPN and a probable mal-operation is averted.

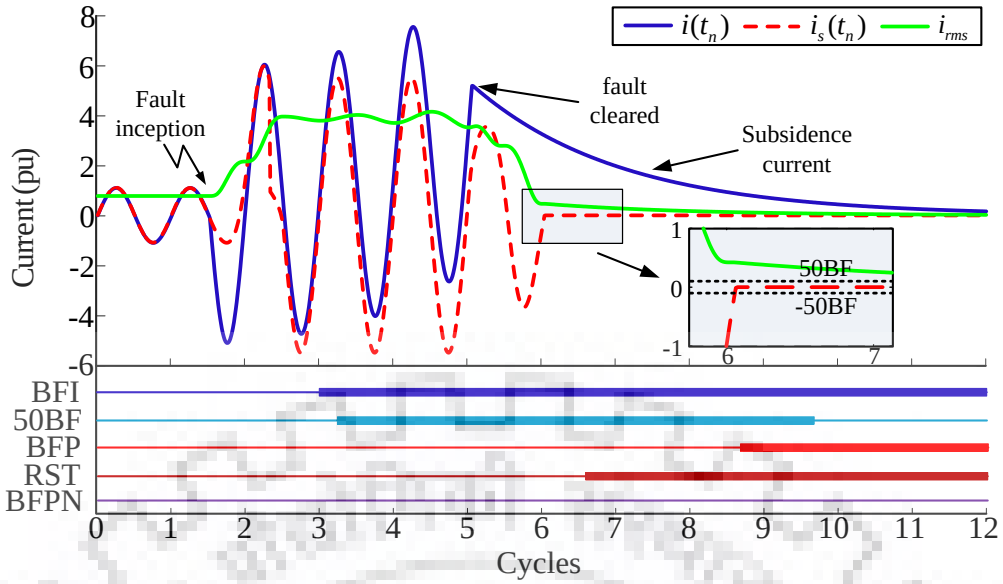

Fig. 6.5: Results obtained in Case 2.

6.5.3 CT Saturation (Case 3)

When the magnetic core of a CT saturates, the secondary current falls too low and flat value [26]. As a result, the magnitude estimator may confuse the 50BF element. As both subsidence current and periodic CT saturation bring similar decaying pattern in magnitude estimators, the existing BFP function may mal-operate. In order to test the performance of BFPN under such conditions, the burden resistance of the CT under consideration (CT-3) has been increased to 10 times its nominal value [114]. Results from BFPN and the exiting BFP scheme in the aforementioned conditions are given in Fig. 6.6. It is to be noted from Fig. 6.6 that the secondary current ($i(t_n)$) falls flat and the phase angle is advanced when compared to the calculated CT secondary current ($i_{primary}(t_n)/CT \quad ratio$) after the saturation point. In this situation, the existing BFP function is asserted as the time element (62) expires. On the other hand, a prior RST signal has been executed by BFPN as the new breaker failure function (BFPN) shows no tripping.

6.5.4 Level of Subsidence (Case 4)

Depending on the CT secondary parameters, the subsidence current may exist from few milliseconds to several seconds. Due to the longer duration of subsidence current, the breaker failure timer (62) eventually expires and BFP function is asserted. In order

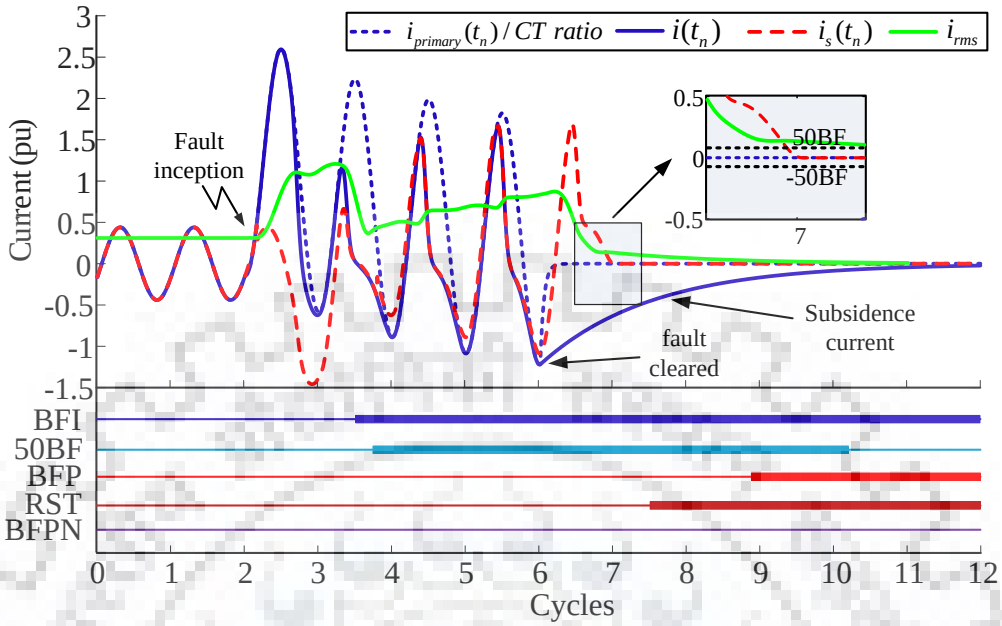

Fig. 6.6: Results obtained in case 3.

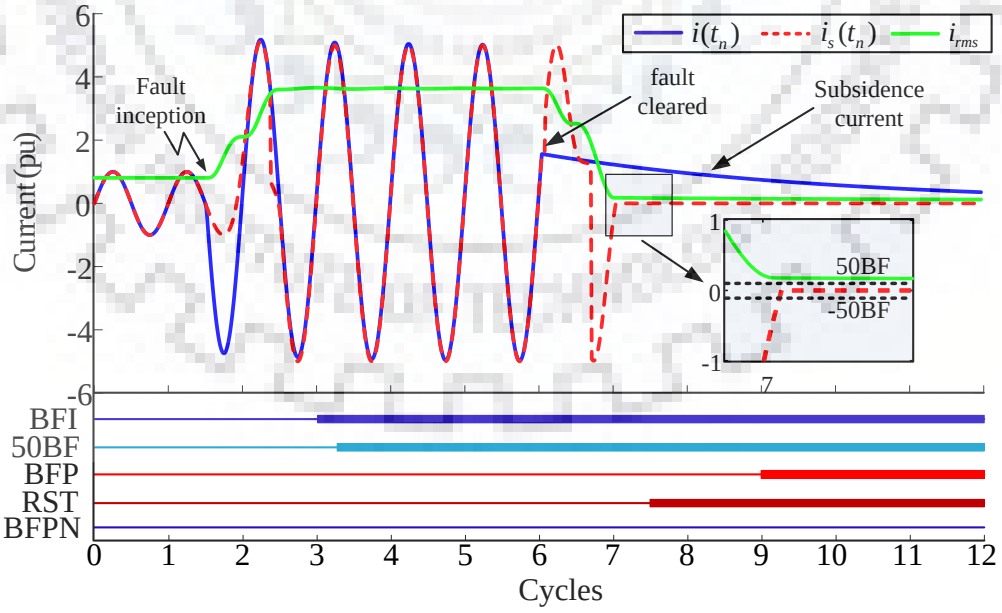

Fig. 6.7: Results obtained in case 4.

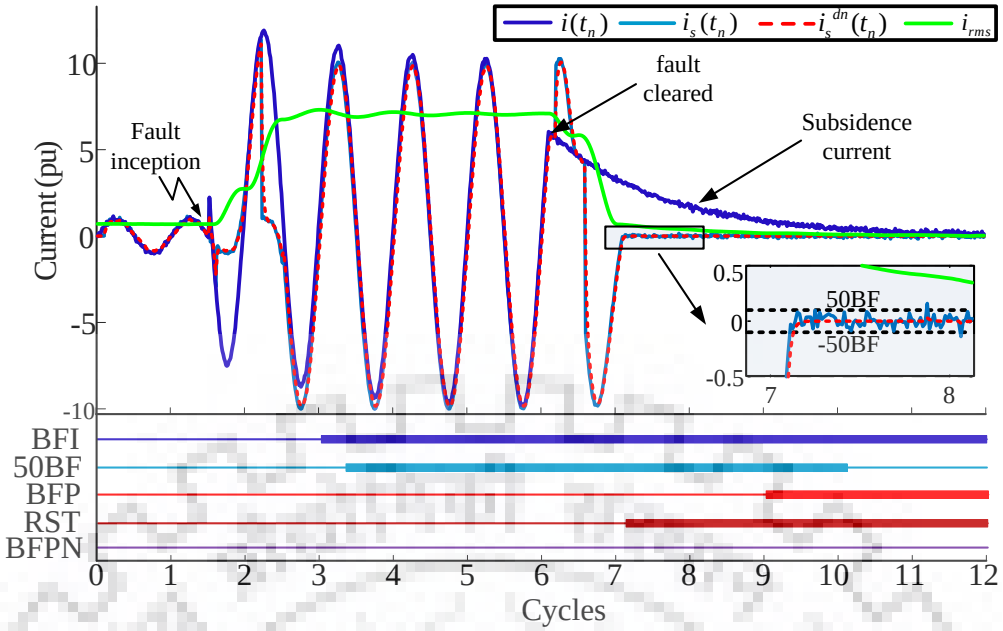

Fig. 6.8: Results obtained in case 5.

to generate subsidence current of longer duration, the CT secondary parameters have been modified. The performance of BFPN for this scenario is shown in Fig. 6.7. It is observed from Fig. 6.7 that the existing BFP function trips as the RMS magnitude estimator remains above 50BF for a significant duration. However, BFPN executes a prior RST signal based on the instantaneous value of the sinusoidal component of current $i_s(t_n)$. Therefore, the mal-operation of the existing BFP function is avoided.

6.5.5 Random Noise

Protection algorithms based on instantaneous current samples such as TW or WT are affected by random noise in the current samples [107, 115]. The RMS magnitude estimators such as DFT need noise-canceling filters for pre-processing of the signal, which adds significant delay in decision making. In order to study the effect of noise on the performance of BFPN, a white Gaussian noise of signal-to-noise ratio (SNR) of 20 dB per sample has been added (Case 5). Results given by BFPN in the aforementioned scenario are depicted in Fig. 6.8. Due to the contamination, the sinusoidal constituent $i_s(t_n)$ holds noise components even after its entry in to -50BF and 50BF bracket. The RST signal has been generated based on the de-noised current signal $i_s^{dn}(t_n)$, which introduces only one sample delay. As evident from the status of BFPN signal, the RST signal restrains the operation of the existing BFP signal even in the presence of

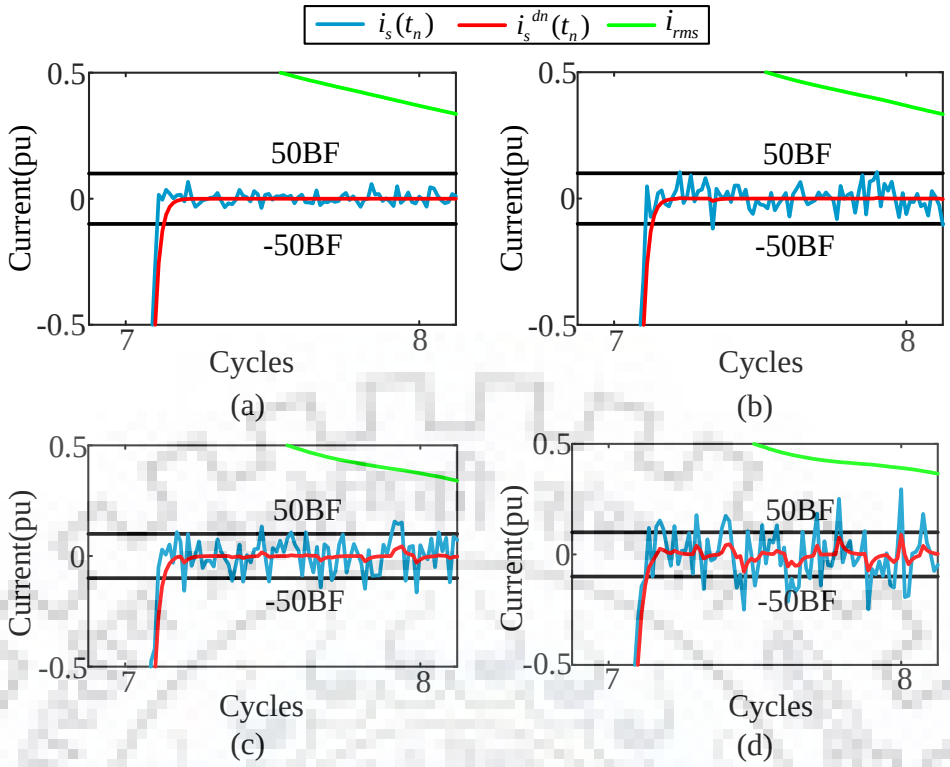

Fig. 6.9: Generation of RST signals at SNR (a) 30 (b) 25 (c) 15 (d) 10 dB

significant noise components.

The typical value of SNR is larger than 27 dB for power system signal analysis [116]. However, to test the effect of noise in more challenging scenarios, white gaussian noises at SNR 30, 25, 15 and 10 dB have been added to the signal. The generated RST signals in the aforementioned scenarios are shown in Fig. 6.9. It can be observed from Fig. 6.9 that the performance of BFPN remains unaffected even with very high noise interference. The denoising process produces favorable results for SNR as low as 10 dB with only one sample delay in the moving average process. A longer moving window may be chosen for signals with lower SNR levels.

6.5.6 Large Scale Analysis

The proposed algorithm has been subjected to a total of 135 diversified test waveforms generated by varying system and fault parameters. Results obtained in terms of average percentage time difference between the 50BF drop out and RST assertion, as defined below, are summarized in Table 6.1.

Table 6.1: Test Results for different combination of scenarios

Scenario	System and fault Parameters			Cases	avg.
	I_f (pu)	X/R	SNR (dB)		t_d (%)
moderate faults	0-10	10	40-50	6	34.6
heavy faults	10-20	10-30	40-50	18	31.6
high DC decay	10-20	50-100	40-50	36	35.3
high subsidence	10-20	10-30	40-50	18	38.2
CT saturation	0-20	10-30	40-50	30	30.3
heavy CT sat.	10-20	10-30	40-50	18	39.8
high noise	0-10	10-30	10-30	9	32.2

$$t_d(\%) = \frac{t_{\text{50BF drop out}} - t_{\text{RST(BFP) pick up}}}{t_{\text{50BF drop out}}} \times 100 \tag{6.15}$$

Alternatively, $t_d(\%)$ signifies the safety margin provided by the proposed algorithm to prevent the mal-operation of the BFP signal. It is observed from Table 6.1 that BFPN has been successful in asserting the reset signal in all possible cases of BFP mal-operation with average safety margin in the range of 30-40%. The results demonstrate significant accomplishments in preventing the mal-operation of the BFP function.

6.5.7 Comparative Evaluation

The magnitude estimators in commercial relays use well-established techniques like DFT or least error squares (LES) [117]. Sustained developments in the field of numerical phasor estimation have lead to recently published sophisticated algorithms such as MDFT [118]. In order to provide a comparative evaluation between these schemes in case of potential breaker-failure situation, a test case with moderate decaying dc presence and high subsidence current (Case 6) has been generated.

Fig. 6.10 shows responses of different magnitude estimators for the aforementioned scenario. It is to be observed from Fig. 6.10 that the RMS magnitudes of current obtained from DFT, LES, and MDFT are not able to neutralize the effect of subsidence current. Each of these algorithms continue to show legitimate RMS current even after 3$\sim$4 cycles after fault clearance. Hence, the commercial relays using any of these RMS estimators would mal-operate the breaker-failure function.

On the contrary, BFPN has been able to completely neutralize the effect of subsidence current. It is evident from Fig. 6.10 that the sinusoidal component of current

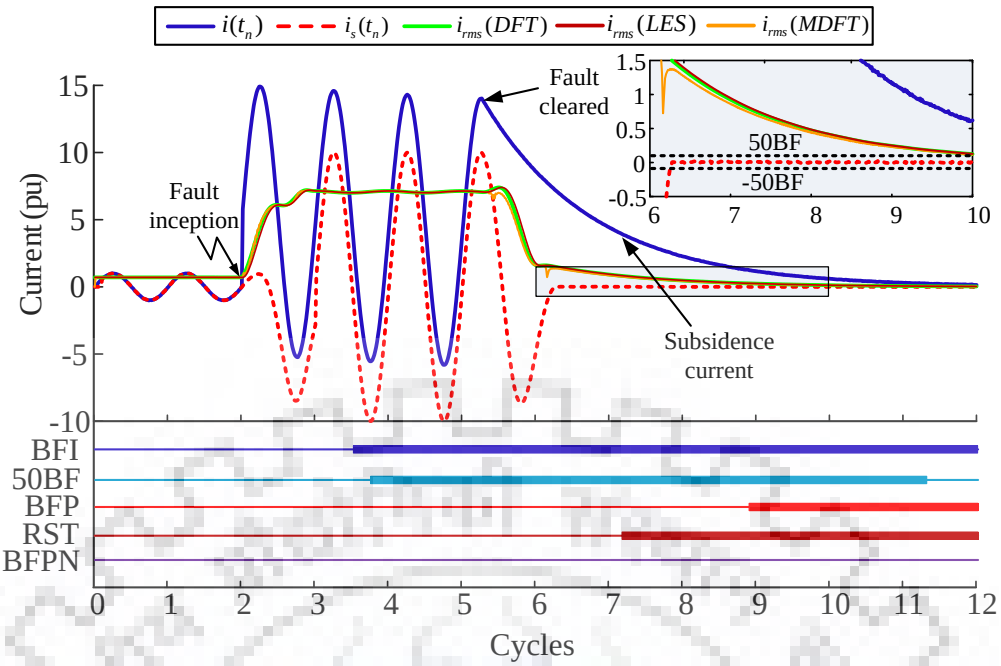

Fig. 6.10: Results obtained in Case 6.

estimated from the proposed algorithm falls within the -50BF and 50BF bracket much before the mal-operation of the BFP signal. The reset (RST) signal is asserted after the fault clearance and the proposed breaker-failure function (BFPN) shows no sign of mal-operation. It is noteworthy to mention that time taken to generate the RST signal is not of much significance as long as it arrives before the assertion of breaker-failure function (BFP) based on the magnitude of RMS estimators. Hence, the results show better reliability of BFPN than the breaker-failure schemes based on conventional and modern RMS magnitude estimators.

6.6 Testing of the proposed algorithm on Laboratory prototype

6.6.1 Prototype Development

In order to test the authenticity of BFPN on realistic waveforms, a laboratory setup, as shown in Fig. 6.11, has been developed. Utility supply and an autotransformer are utilized as a source. The line parameters (R and X) are represented by variable rheostat and inductors. A protective class CT (50/5 A), which scales down the current level for relay operation is connected in series with the line. The BFP module, as given

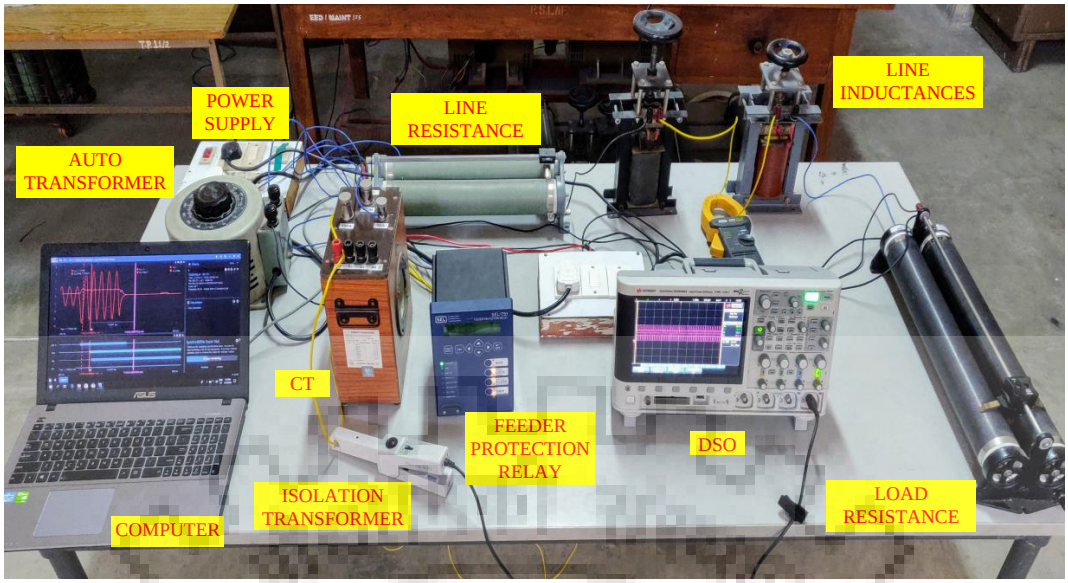

Fig. 6.11: Developed laboratory setup

in the conventional feeder protection relay, is activated for testing in case of different scenarios of subsidence current [119]. The relay is connected to a computer (Intel Core i7 processor at 4 GHz clock frequency, 8 GB RAM) via Ethernet cable to monitor and diagnose the fault scenarios. The CT secondary current is acquired and monitored on a four-channel DSO through an isolation transformer. The events recorded under different test scenarios are exported to evaluate BFPN.

6.6.2 Test results

A solid single-line-to-ground fault with line X/R ratio 10 was applied to the laboratory setup. The results given by the conventional feeder protection relay (event record) and the proposed algorithm for the afore-mentioned scenario are shown in Fig. 6.12. It is observed from Fig. 6.12 (a) that the feeder protection relay trips when the magnitude of fault current exceeds a pre-defined threshold. Subsequently, both BFI and 50BF functions pick-up. It is also to be noted that the BFP function is asserted after both 50BF and BFI remain active for the critical fault clearance duration (5.625 cycles). At the same time, the response of BFPN for the aforementioned event is presented in Fig. 6.12 (b). Upon inspection, it is observed that BFPN can generate the reset signal (RST) before the assertion of the BFP function. Hence, the proposed new breaker-failure scheme (BFPN) prevents a probable mal-operation. This demonstrates the effectiveness of the proposed scheme (BFPN) in practical scenarios where

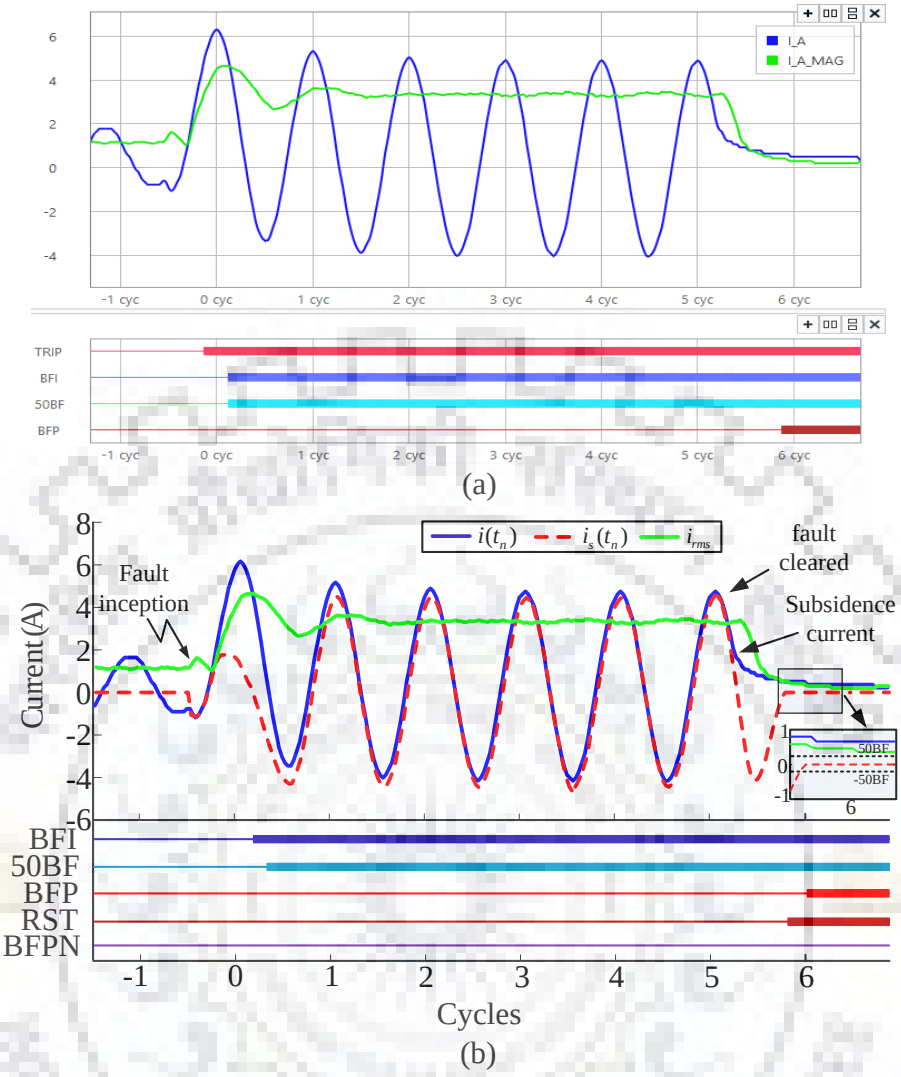

Fig. 6.12: (a) Relay event record (b) response of proposed scheme.

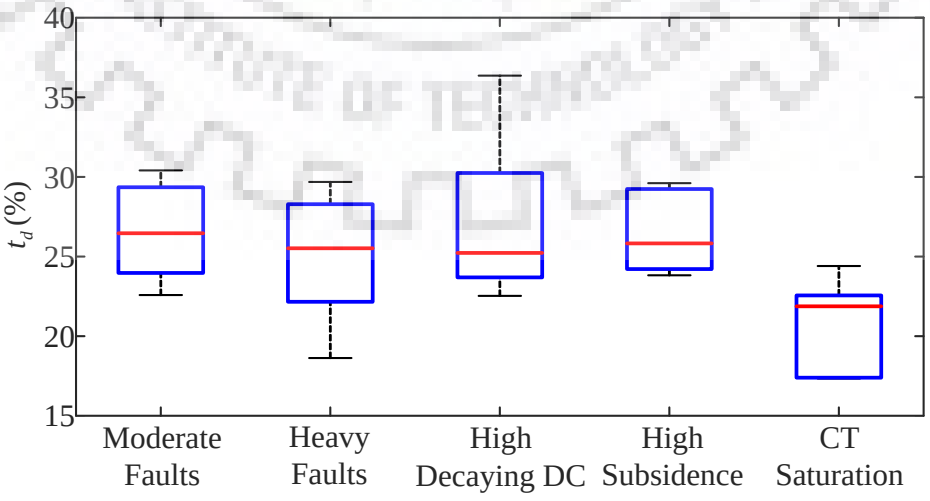

Fig. 6.13: Test results from laboratory setup in % safety margin distribution.

the conventional relay mal-operates.

The performance of the proposed algorithm was further verified by generating 25 different fault scenarios with 5 in each of the categories: moderate faults, heavy faults, high decaying dc, high subsidence, and CT saturation. The results in terms of average percentage safety margin distributions, as defined in equation (6.15), are shown in Fig. 6.13. It is observed from Fig. 6.13 that the proposed scheme was successful in preventing the mal-operation of the existing BFP scheme in the conventional relay with safety margin in the range of 20-30%.

6.7 Conclusion

A reliable breaker failure protection reset scheme, which prevents mal-operation of CBs due to the presence of subsidence current, is presented in this chapter. The proposed scheme differentiates between the alternating pattern of fault current and decaying pattern in subsidence current. The exact decaying component in the current waveform is calculated through numerical analysis and subsequently, the sinusoidal component is extracted. A reset signal is asserted when the sinusoidal component in current lies within the thresholds for a specified duration. The results obtained are consistent and robust in preventing mal-operation of BFP function with significant safety margins in the range of 20-30%. Studies show that wide variation in fault current level, decaying dc component, CT saturation, level of subsidence and noise do not affect the performance of the suggested technique. Additionally, its structure is simple and well defined that can be easily fine-tuned with the existing commercial relays. Also, a comparison of the proposed scheme with the existing technique affirms its supremacy especially during the instances of longer subsidence current following high decaying DC component in the fault current.

Chapter 7

Conclusions and Scope of Future Work

7.1 Summaries

The broader challenging aspects attract researchers to develop sophisticated busbar protection schemes. With higher voltage levels at extra/ultra-high-voltage (EHV/ UHV) substations, the speed of protection has become more critical. Furthermore, dynamic system configurations and load transfers add challenges to reliable busbar protection. Hence, a vast void remains to be filled up in achieving an all-round universal busbar protection. In this regard, A new fault zone identification scheme for busbar using Logistic Regression (LR) binary classifier by utilizing one cycle post-fault current signals of all the bays connected to the busbar has been developed. Practicability of the presented scheme has been verified by modeling an existing 400-kV Indian power generating station in PSCAD/EMTDC software package. The presented scheme has been tested on enormous cases (38,400) which were generated by varying system and fault parameters. The proposed scheme provides active discrimination between internal and external faults with a very high (99.69%) overall accuracy. Moreover, it remains stable in case of heavy through fault conditions, particularly with CT saturation during which the conventional differential protection scheme mal-operates. Furthermore, it provides equally compatible accuracy for unknown system/unseen data set as well as for double/one-and-half breaker busbar arrangement. Besides, the performance of the proposed scheme has been verified on the laboratory prototype. The average tripping

time is of the order of 23 ms in case of internal faults. A comparative evaluation of the proposed scheme with recently presented schemes in the literature indicates its superiority.

After that, to overcome the challenges of 87B, a digital differential busbar protection scheme based on Generalized Alpha Plane (GAP) approach, which combines the benefits of percentage differential approach and two-restrain alpha plane approach has been proposed. The proposed scheme utilizes one cycle CT secondary current signals of all the bays connected to the busbar to map the operating points on a complex alpha plane. The proposed scheme has been evaluated by modeling an existing 400-kV Indian power generating station in PSCAD/EMTDC software package. The performance of the proposed scheme has been evaluated on large numbers of cases with wide variation in system and fault parameters. A laboratory prototype of the proposed busbar protection scheme has been developed to verify the authenticity. From the developed prototype, CT secondary current signals are captured during internal faults and external fault with CT saturation condition. Comparison between the simulation and prototype results clearly shows the effectiveness of the proposed scheme in terms of higher sensitivity during internal faults and better stability in case of external faults. The proposed protection scheme has a high response speed (around 5 ms) and hence, can be considered on par with modern busbar protection schemes.

High-speed tripping is necessary to limit the damage caused by busbar fault, which becomes more significant in case of high voltage substations because of large fault currents. In this regard, a busbar protection scheme based on initial travelling wavefronts is presented. The aerial mode current Travelling Waves (TWs) across all lines connected to the busbar are calculated using Karenbauer transformation. Thereafter, the polarity and magnitude of Wavelet Transform Modulus Maximas (WTMMs) of line current appearing after fault inception are analysed for fault zone and faulted phase identification. Its performance has been evaluated by modelling an existing 750-kV Indian substation in PSCAD/EMTDC software package. The simulation results reveal that the proposed scheme provides better stability for external faults and higher reliability in case of internal faults in comparison with 87B. Moreover, it remains immune to the CT saturation problems. In the end, comparative evaluation of the proposed scheme with the existing busbar protection schemes proves its superiority in terms of

stability against external faults, sensitivity for internal faults, computational obligations, and communication requirements.

Security of the protection unit can be improved by appropriate substation design and dividing the bus zone into multiple zones. An internal busbar fault, in this case, affects only a smaller part of the substation and fewer components are affected. In this regard, a novel algorithm based on *dq*-components has been developed for bus zone protection. The analog CT secondary signals are acquired and converted into sampled values (SVs). Then, the fundamentals of instantaneous current-based differential protection scheme (87B) have been considered to establish the trip logic of the proposed scheme. Its performance has been validated by simulating faults on an existing 400-kV substation with double-bus-single-breaker configuration. Moreover, a laboratory experimental setup has been developed to test the authenticity of the proposed scheme for various fault scenarios. The obtained results from the simulation model and laboratory prototype testify the claims of higher sensitivity during internal faults and better stability during external faults with CT saturation. The proposed scheme has been able to provide high-speed busbar protection against a wide range of internal faults. Comparative evaluation with contemporary busbar protection schemes indicates its superiority.

At the end, a reliable breaker failure protection reset scheme, which prevents mal-operation of CBs due to the presence of subsidence current, is presented. The proposed scheme differentiates between the alternating pattern of fault current and decaying pattern in subsidence current. The exact decaying component in the current waveform is calculated through numerical analysis, and subsequently, the sinusoidal component is extracted. A reset signal is asserted when the sinusoidal component in current lies within the thresholds for a specified duration. The results obtained are consistent and robust in preventing mal-operation of BFP function with significant safety margins in the range of 20-30%. Studies show that wide variation in fault current level, decaying dc component, CT saturation, level of subsidence, and noise do not affect the performance of the suggested technique. Additionally, its structure is simple and well defined that can be easily fine-tuned with the existing commercial relays. Also, comparison of the proposed scheme with the existing technique affirms its supremacy, especially during the instances of longer subsidence current following high decaying DC component in

the fault current.

7.2 Contributions

A busbar acts as a hub of connection point for multiple transmission lines and substation equipment. Though the occurrence of a bus fault is rare, the severity of its consequences is catastrophic. It may result in the loss of multiple transmission lines, equipment, and probable blackout situation. Hence, reliable busbar protection is the most important aspect of substation protection. A busbar fault should be identified and the corresponding fault zone should be isolated from the rest of the network with minimum time delay. On the contrary, the mal-operation of a busbar relay creates unnecessary power outage to a large part of the power system. Hence, it is highly desirable to develop busbar protection schemes with improved characteristics. To this end, the thesis concentrated upon the development of improved state-of-the-art busbar protection schemes with both statistical and numeric analysis. In addition, the thesis also proposes an integrated breaker-failure technique to prevent the mal-operation from subsidence current in CT secondary.
The following major contributions are drawn out of this thesis work:

- Initially, a statistical learning-based approach to busbar protection based on the instantaneous current sample values has been proposed. It has been observed that the fault zones can be classified with a very high accuracy with minimum training required. The proposed scheme can be easily fine-tuned for different busbar configurations with equal compatible results. The decision boundary, in this case, is well defined based on the optimization of the cost function. The performance of the proposed scheme has remained consistent while tested through a large data set comprising a wide variety of fault scenarios. Comparative evaluation among contemporary schemes such as ANN and SVM shows its superiority.

- Thereafter, an improved differential protection for busbar based on the concept of GAP has been presented. The benefits of 87B and the two-restrain alpha plane approach have been combined to develop an improved busbar differential protection scheme. The n-terminal line currents at a busbar has been converted into two-terminal equivalent in a phase-segregated manner. The results obtained

from the testing of a large set of fault scenarios show its responsiveness in internal faults and stability against external faults specifically in severe CT saturation scenarios. The results obtained from the hardware setup show encouraging results for on-field implementation. The response time of the proposed scheme is less than 5 ms which is on par with modern state-of-the-art relays.

- In order to achieve high-speed busbar protection, a protection scheme based on the polarity of initial TWs has been presented. WTMMs have been effectively utilized for the extraction of the initial TWs. The magnitude of the WTMMs has been used for the classification of busbar faults. The results show the high reliability and responsiveness of the proposed scheme in detection and faulted phase identification in busbar faults. The computational and communication burden of the proposed scheme remains the least minimum when compared to other wavelet-based schemes. The practicability of the proposed architecture for real-field application of the scheme has been discussed in detail. Considering factors like system delays and latency in communication, the proposed scheme posses response time below 2 ms. Overall, an improved protection scheme with high-speed response and minimal computation requirements has been developed.

- A sampled value (IEC 61850) based busbar protection scheme using dq-components has been proposed. It has been observed that both d and q components remain constant during normal operating conditions. However, after the inception of fault, they oscillate with double frequency components. This property has been utilized to develop a reliable high-speed busbar differential protection scheme. The fundamentals of 87B has been utilized in terms of d-axis components. The results obtained show that the proposed scheme posses better sensitivity specifically in case of HIFs and higher stability against potential mal-operation due to CT saturation conditions. The results obtained from the laboratory prototype validate its high degrees of reliability and responsiveness. The feasibility of the proposed scheme for IEC 61850 based process bus applications has also been discussed. In terms of operating speed, the proposed scheme provides better responsiveness.

- In the end, a reset algorithm to prevent the mal-operation of the breaker-failure

Table 7.1: Comparative Judgment of Proposed Busbar Protection Schemes

	87BLR	87BGAP	87BITW	87BD
Operating Speed (Cycles)	<1.25	< 1.5	< 0.25	< 0.25
Responsiveness	Very high	high	Ultra high	Ultra high
Reliability	Moderate	Very high	High	Very high
Stability	Moderate	Very high	Moderate	High
Effect of CT saturation	Less	Very less	No effect	Less
Phasor Requirement	No	Yes	No	No
Post fault calculations	High	Moderate	Very less	less
Complexity	High	Less	Very Less	Less
On-Chip feasibility	Moderate	Very high	High	High
Phase-segregated relays	Yes	Yes	Yes	No
Sampling Requirement	Very low	Low	Very high	Moderate

function has been presented. The proposed scheme has been able to generate a reset signal in a wide variation of fault scenarios where a longer subsidence current is present after the fault clearance. It clearly distinguishes between the alternating pattern of true fault current and decaying pattern in subsidence current. Its performance has remained consistent against wide variation in fault current level, decaying dc component, CT saturation, level of subsidence and noisy scenarios. It has been able to prevent potential mal-operation of breaker-failure function with safety margins in the range of 20-30%. Moreover, the structure is simple and well-defined to be fine-tuned with existing commercial relays.

7.3 Comparative Judgement of Proposed Schemes

In this section, different busbar protection schemes presented in this thesis have been compared in terms of their relative performance. Table 7.1 presents the comparative judgement of each of the proposed schemes.

It is to be observed from Table. 7.1 that each of the proposed schemes has their own merits and limitations over others. The logistic regression based classification scheme (87BLR) possesses high responsiveness and does not involve in phasor computation but the on-chip implementation possibilities is relatively difficult with respect to other schemes. On the contrary, the Generalized Alpha Plane based scheme (87GAP) possesses very high potential of on-chip implementation because of simpler numerical calculations with existing hardware. However, the operating time is relatively higher

because of the phasor requirement of each phase currents. The initial travelling wave based scheme (87BITW) is able to provide ultra-high speed protection in the range of <5 ms and also free from the effect of CT saturation mal-operation. However, the sampling requirements are higher when compared to other schemes. The scheme based on the d-component of current (87BD) has high operating speed with lesser complexities. Moreover, the requirement of three separate phase-segregated relays is replaced with a single relay in terms of d-axis component of current. Hence, 87BD possess relative advantages over all other schemes. The evolution of the developed schemes shows the requirement of better solutions with minimum compromise on other aspects.

7.4 Scope of Future Work

After years of steady development, achieving perfection in every aspect of busbar protection remains challenging. This thesis is concentrated on achieving improved busbar and breaker failure techniques. Followings are some of the areas which can be further explored in the pursuit of overall all-round busbar protection:

- Several pragmatic issues such as faults in blind spot (between CT and CB), improper fault zone selection due to positioning of the tie-breaker CB and neighboring CTs can be explored with real-field data and event records.
- Hybrid approach with statistical theories and deep-learning techniques can be approached for massive data analysis of busbar and breaker failure fault scenarios. This analysis can be extended to develop sophisticated yet practical fault zone classification schemes.
- Busbar protection in changing grid scenarios such as HVDC, AC-DC, DC-DC microgrids may be more challenging because of faults on DC sides. A centralized approach for such multi-terminal busbar protection may be developed to address such issues.
- While ultra-high-speed protection for busbar can be achieved through TW-based relays, faults with small inception angles remain undetected. Furthermore, TW based relays rely on inductive CTs and capacitive VTs which do not apply to

DC systems. These aspects should be looked into while developing TW based schemes.

- Prevention of Mal-operation in breaker-failure schemes is one of the uncharted territories that has not gained much attention from researchers. This area can be explored with real-field data and sophisticated mathematical tools can be utilized to achieve improved solutions. The challenges in integrating reliable solutions for both busbar and BFP using the commonly available data with minimum computation and high responsiveness can be investigated.

Appendices

Appendix-I

Parameters used for 400-kV power system network

Source Impedance Values:

Positive-sequence impedance for all sources: $Z_1 = 0.871 + j9.96\ \Omega$

Zero-sequence impedance of all sources: $Z_0 = 1.743 + j19.92\ \Omega$

Transmission-line data:

Length: 100 km

Voltage: 400 kV

Positive-sequence impedance: $0.0297 + j0.332\ \Omega/km$

Zero-sequence impedance: $0.162 + j1.24\ \Omega/km$

Positive-sequence capacitance: $9.23\ nF/km$

Zero-sequence capacitance: $6.72\ nF/km$

Appendix-II

Parameters used for 220-kV power system network

Source Data:

Positive-sequence impedance of $G1$: $0.0174 + j0.199\ \Omega$

Positive-sequence impedance of $G2$: $1.307 + j14.942\ \Omega$

Zero-sequence impedance of $G1$: $0.00435 + j0.0498\ \Omega$

Zero-sequence impedance of $G2$: $0.817 + j9.961\ \Omega$

System Frequency = 50 Hz

Transmission-line data:

Line lengths: $L1 = 100\ km$, $L2 = 100\ km$, $L3 = 80\ km$, $L4 = 70\ km$, and $L5 = 70\ km$

Positive-sequence impedance: $0.0297 + j0.332\ \Omega/km$

Zero-sequence impedance: $0.162 + j1.24\ \Omega/km$

Positive-sequence capacitance: $12.99\ nF/km$

Zero-sequence capacitance: $8.5\ nF/km$

Transformer data:

GT: 300 MVA, 11 kV/220-kV, Delta-Wye neutral grounded (DYng), $Z_l = 10\ \%$

ICT: 150 MVA, 11 kV/6.6 kV, Delta-Wye neutral grounded (DYng), $Z_l = 12\ \%$

UAT: 5 MVA, 11 kV/6.6 kV, Delta-Wye neutral grounded (DYng), $Z_l = 10\ \%$

Reactor data:

Line reactor: 20 MVAR, 220-kV, 50 Hz, Y Connected.

Bus reactor: 50 MVAR, 220-kV, 50 Hz, Y Connected.

Appendix-III

Parameters used for modelling of the 400-kV power system network

Source impedance values of generator $S1, S2$ and $S3$:

Positive-sequence impedance for all sources: $Z_1 = 0.871 + j9.96\ \Omega$

Zero-sequence impedance of all sources: $Z_0 = 1.743 + j19.92\ \Omega$

Transmission-lines $L1, L2$ and $L3$: data:

Length: 100 km

Voltage: 400 kV

Positive-sequence impedance: $0.0297 + j0.332\ \Omega/km$

Zero-sequence impedance: $0.162 + j1.24\ \Omega/km$

Positive-sequence capacitance: $9.23\ nF/km$

Zero-sequence capacitance: 6.72 nF/km

Current Transformers $CT1, CT2$ and $CT3$ data:

CT ratio: 400/5 A

secondary resistance: 0.5 Ω

secondary inductance: 0.8 mH

Burden resistance: 0.5 Ω

Appendix-IV

Parameters of the 750-kV power system network

Generators (G_1, G_2, G_3) Parameters:

Source	Voltage (kV)	$Z_0(\Omega)$	$Z_1(\Omega)$
G_1, G_2	$750 \angle 0°$	$1.743 + j19.92$	$0.871 + j9.96$
G_3	$750 \angle$ -5°	$1.743 + j19.92$	$0.871 + j9.96$

Transmission line (l_1, l_2, l_3) Parameters:

Z_0 (Ω/km)	Z_1 (Ω/km)	C_0 (nF/km)	C_1 (nF/km)
$0.162 + j1.24$	$0.0297 + j0.332$	6.72	9.23

Power Transformer (T_1, T_2, T_3) Parameters:

S (MVA)	X_1 (pu)	Primary (kV)	Secondary (kV)
250	0.145	13.8 (Y)	750 (Δ)

Appendix-V

400-kV double-bus single-breaker substation parameters

Equivalent sources:

$E_{S1,S3} = 400\angle 0$; $E_{S2,S4} = 400\angle -5$

$Z_0 = 1.743 + j19.92\ \Omega$; $Z_1 = 0.871 + j9.96\ \Omega$

Transmission lines:

$Z_0 = 0.162 + j1.24\ \Omega/km$; $Z_1 = 0.0297 + j0.332\ \Omega/km$

$C_0 = 6.72\ nF/km$; $C_1 = 9.23\ nF/km$

Power Transformers:

$V_{ratio} = 13.8/400$ kV $(Y - \Delta)$; $S = 250\ MVA$

Appendix-VI

Simulation Model Parameters

Equivalent sources:

$E_{S1,S2} = 400\angle 0\ kV$; $E_{S3} = 400\angle -5\ kV$

$Z_0 = 1.743 + j19.92\ \Omega$; $Z_1 = 0.871 + j9.96\ \Omega$

Transmission lines:

$Z_0 = 0.162 + j1.24\ \Omega/km$; $Z_1 = 0.0297 + j0.332\ \Omega/km$

$C_0 = 6.72\ nF/km$; $C_1 = 9.23\ nF/km$; length $= 100\ km$

Power Transformers:

$V_{ratio} = 13.8/400$ kV $(Y - \Delta)$; $S = 250\ MVA$;

$X_l = 0.145\ p.u.$

Current Transformers:

Current Transformers:

Ratio $= 400/5$; $R_2 = 0.5\Omega$;$X_2 = 0.25\ \Omega$; Burden $= 0.5\Omega$

List of Publications

SCI Journals:

1. S. Jena and B. R. Bhalja, "Development of a new fault zone identification scheme for busbar using logistic regression classifier," in *IET Generation, Transmission & Distribution*, vol. 11, no. 1, pp. 174-184, January 2017.
2. S. Jena, and B. R. Bhalja, "Numerical Busbar Differential Protection using Generalized Alpha Plane," in *IET Generation, Transmission & Distribution*, vol. 12, no. 1, pp. 227-234, January 2018.
3. S. Jena, and B. R. Bhalja, "A New Differential Protection Scheme for Busbar Using dq0 Transformation," in *Electric Power Components and Systems*, vol. 47, no. 4-5, pp. 382-395, May 2019.
4. S. Jena, and B. R. Bhalja, "Initial travelling wavefront-based bus zone protection scheme," in *IET Generation, Transmission & Distribution*, vol. 13, no. 15, pp. 3216-3229, August 2019.
5. S. Jena, and B. R. Bhalja, "A New Sampled Value-based Bus Zone Protection Scheme with dq-components," in *IET Generation, Transmission & Distribution*, (Under Review).
6. S. Jena, and B. R. Bhalja, and O. P. Malik "An Improved Breaker-failure Reset Algorithm based on Numeric Analysis," in *IEEE Transactions on Industrial Informatics*, (Under Review).

Patents:

1. S. Jena, and B. R. Bhalja, "Add-on device and its method to prvent breaker-failure mal-operation" in *Indian Patents, Application No: 201911053612*, December 2019 (Application filed)

Conference Proceedings:

1. S. Jena and B. R. Bhalja, "A new numeric busbar protection scheme using Bayes point machine," in proceedings *2017 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC), Bangalore*, November 2017, pp. 1-6.

2. S. Jena, B. R. Bhalja, and S. R. Samantray "A Fault Zone Identification Scheme for Busbar using Correlation Coefficients Analysis," in proceedings *2019 IEEE PES General Meeting (PESGM), Atlanta*, August 2019, pp. 1-5.

3. S. Jena, and B. R. Bhalja, "Application of Wavelet Transform for IEC-61850 Based Busbar Protection," in proceedings *IEEE India Council International Conference (INDICON 2019)*, December 2019.

4. S. Jena, and B. R. Bhalja, " A New Differential Protection Scheme for Busbar using Teager Energy Operator," in proceedings *International Conference on Power Systems (ICPS 2019), Jaipur, India*, December 2019.

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