POWER CONVERTER FOR BATTERY CHARGER IN PLUG-IN HYBRID AND ELECTRIC VEHICLES

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree

of

MASTER OF TECHNOLOGY

in

ELECTRICAL ENGINEERING
(With Specialization in Electric Drives and Power Electronics)

By

NITISH SHARMA

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE-247667(INDIA)
May 2019

CANDIDATE'S DECLARATION

I hereby declare that the work which is presented in this project, entitled, **"POWER CONVERTER FOR BATTERY CHARGER IN PLUG-IN HYBRID AND ELECTRIC VEHICLES"**,submitted in partial fulfillment of the requirement for the award of the degree of **Master of Technology** in **"Electrical Drives & Power Electronics"** in Electrical Engineering, Indian Institute of Technology Roorkee, is an authentic record of my own work carried out during the period from January 2018 to November 2018 under the supervision and guidance of **Dr.M.K.Pathak**, Associate professor Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee (India).

Date: May 17,2019

Place: Roorkee,India **(NITISH SHARMA)**

CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Dr.M.K.PATHAK,
Associate Professor,
Electrical Engineering,
Indian Institute of Technology,
Roorkee-247667

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I extend my thanks to all classmates who have given their full cooperation and valuable suggestions for my seminar work.

Thank you,

Date: May 17,2019

Place: Roorkee,India **(NITISH SHARMA)**

ABSTRACT

Plug-in Hybrid Electric Vehicles(PHEV) and Electric Vehicles are rolled out for the consumer,and become popular in a short period of time.With the advent of Battery chargers for PHEVs there is a big opportunity for the power supply Industries to deploy large number of charging stations ,affordable and easy to use,home charging station . Overall charging efficiency advancement is a important factor for the approval of these technologies,when the performance increase the charging hour and service charge decrease. Power factor correction is important to achieve regulatory standards for the AC supply mains.

Chargers with smaller size which could render more power are needed as minimal space is available in vehicle and power consumption is increasing with time,Important part of a charging system is the AC-DC converter connected in front end, which should attain high power density and high efficiency . Different front end AC-DC conventional plug in hybrid electric vehicle charger converter topologies are examined and to enhance the efficiency and performance a new bridgeless interleaved and a phase shifted semi-bridgeless power factor corrected converter are proposed , which is remarkable to optimize the charger size, charging time, and the amount and cost of electricity drawn from the utility. A comprehensive analytical model for these topologies is developed,with the help of which power losses and efficiency are calculated . Experimental and simulation results of prototype Bridgeless interleaved boost converter which convert the universal AC input voltage to 400 V DC at 3.4 kW are provided to authenticate the proof of concept, and analytical work discribed in this thesis. The results show a power factor greater than 0.99 from 750 W to 3.6 kW, THD less than 5% from half load to full load and a peak efficiency of 98 % at 264 V input and 1000 W load.

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List of Symbols

C_O	Output Capacitor
δ_D	Boost Diode Duty Cycle
δ_Q	Boost Main Switch Duty Cycle
I_{ms}	Total Line Current
I_{Irms}	Fundamental Component
K_d	Distortion Factor
K_θ	Displacement Factor
T_S	One Switching Period
θ_I	Angle between Current Fundamental and Sinusoidal
	Line Voltage
V_S	Maximum Input Voltage
V_{ref}	Reference Voltage

Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
ASIC	Application Specific Integrated Circuits
BJT	Bipolar Junction Transistor
BL	Bridgeless
BLIL	Bridgeless Inte leaved
CCM	Continuous Conduction Mode
CRM	Critical Conduction Mode
D	Duty Cycle
DC	Direct Current
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processors
FL	Full Load
FPGA	Field Programmable Gate Array
IC	Integrated Circuits
IGBT	Insulated Gate Bipolar Transistor
IL	Interleaved
EMI	Electrical Magnetic Interference
EV	Electric Vehicle

MOSFET	Metal Oxide Silicon Field Effect Transistor
NL	No Load
PID	Proportional Integral Derivative
PF	Power Factor
PFC	Power Factor Correction
PHEV	Plug in Hybrid Electric Vehicle
PSFB	Phase Shift Full-Bridge
PWM	Pulse Width Modulation
RLC	Resistance Inductor Capacitor
RMS	Root Mean Square
SR	Synchronous Rectifier

Chapter 1

Introduction

In the present era the energy demand increase abruptly and for the main source of energy we depend on fossil fuels as it easy to extract and cost effective. although,there is disadvantage cause by them for example air pollution which as a result effect our atmosphere,other with the price of the fossil fuel which increasing day by day.which pressurizing the Industries and Government to replacement of the fossil fuels. As a result our interest is increasing in the mean of transportation for example Plug in Hybrid Electric Vehicles (PHEV) and Electric Vehicles (EV).

In the early 19th century we were aware of the EV and PHEV technology.however,In comparison with oil the EV have high price and less energy output and the cost of storing battery was high.Now the scenario is different ,with the advent of Lithium-ion batteries and there is a hike in the price of fossil fuels and the pollution arise by them ,convince the organisation to concentrate on EV and PHEV.

when more number of EV and PHEV comes in the market and on the road ,this will impact the utility grid when the demand of charging it is at the peak level [1].As a result in order to reduce the load on grid and decrease the charging hour there is a requirement of efficient and high power factor chargers.To keep the input current harmonics in limit drawn by these charger power factor of the charger must comply with the standards as IEC 61000-3-2 [2]

Chapter 2

Background

2.1 Background

A hybrid vehicle with a capacity battery that could be energized by connecting a plug to an outside electricity supply coming from power source. Outlet for charging with the AC supply certainly require an on-board AC/DC charger having a power factor adjustment. An on-board 3.5 kW charger can charge an fully empty battery package in PHEVs to 95% charge within four hours by the 240 V supply [3].
efficient Chargers are additionally characterized with the dimension of power they can Make accessible to the battery package [4]:

- Level 1:typical family unit circuit, evaluated to 15 amperes and 120 volts AC . These chargers utilize the standard three-prong family unit association, and they are, for the most part thought to be convenient hardware.

- Level 2: For all time wired connected electric vehicle supply equipment utilized particularly for electric vehicle charging; evaluated up to limit of voltage 240 volts AC and current up to 60 amps, and power up to 14.4 kilowatts.

- Level 3:For all time wired electric vehicle supply gear utilized primarily for electric vehicle charging; evaluated for rating more than 14.4 kW. Quick chargers are appraised as Level 3, however not all Level 3 chargers are quick chargers. This

assignment relies upon the span of the battery package to be charged and how much time is required to charge the battery pack. A charger can be viewed as a quick charger on the off chance that it can charge a normal electric vehicle battery pack in 30 minutes or less.

The front-end AC/DC converter is a significant part of the charging system. The reason of this record is to examine how this examination will be led on the elite single-stage answers for AC/DC power factor remedied converters for PHEV battery chargers. An alternate circuit topologies and control techniques have been produced for the PFC application [5–7]. The single-stage active PFC methods can be separated into two classes: the single-stage approach and the two-stage approach. The single-stage approach is appropriate for low power applications. What's more, because of vast low frequency ripple in the output current, just lead-corrosive batteries are chargeable. Accordingly, the two-stage approach is the best possible contender for PHEV battery chargers [8], where the power rating is relatively high, and lithium-particle batteries are utilized as the fundamental energy storage system. The front end PFC area is then trailed by a DC/DC section to complete the charging system.

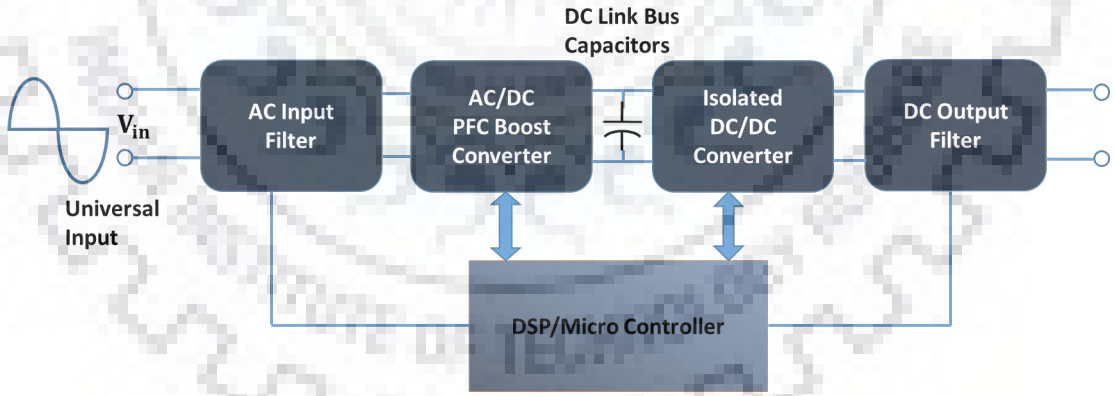


Figure 2.1: block diagram of a universa two-stage battery charger

The PFC level rectify the enter AC voltage and switch it right into a regulated intermediate DC hyperlink bus. At the equal time, power factor component correction characteristic is executed. The following DC/DC stage then converts the DC bus voltage into a regulated output DC voltage for charging batteries, which is required to fulfill the law and brief requirements.

2.1.1 Power Factor general background

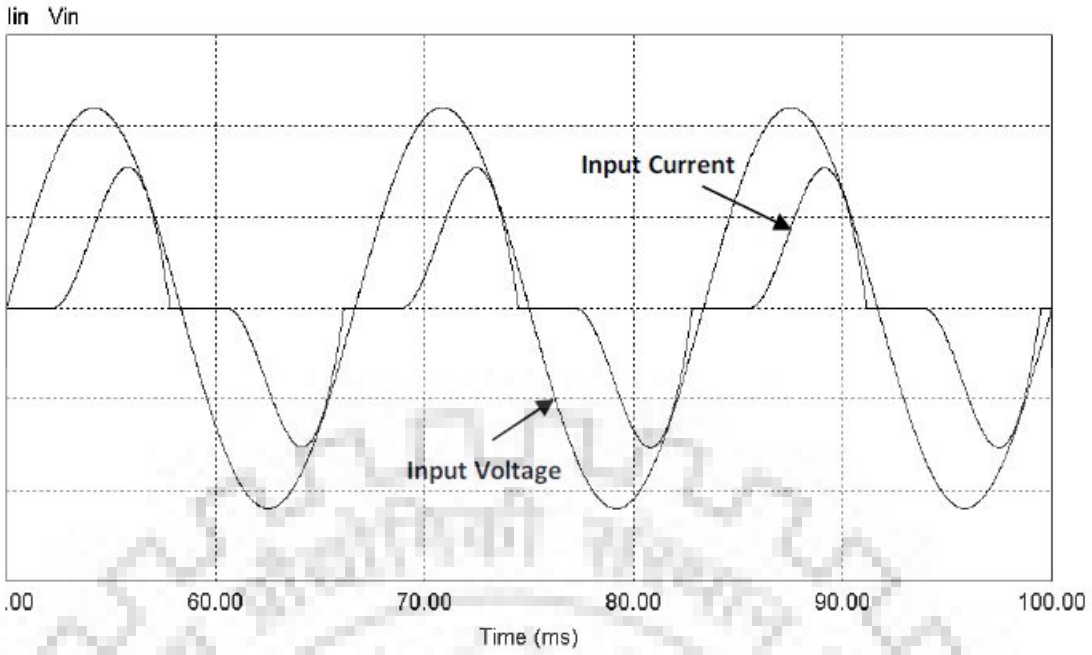
As per the requirements of input current harmonics [9] and output voltage regulation, a front-end converter is regularly actualized by a power factor correction (PFC) stage. Conventionally, a large portion of the power transformation hardware utilizes either a diode rectifier or a thyristor rectifier with a mass capacitor to converter AC voltage to DC voltage before preparing it [10]. Such rectifiers generate harmonic in the input current , which contaminates the power system and the utility lines. Power quality is turning into a noteworthy worry for some electrical users.The most straightforward type of PFC is Passive (Passive PFC).A passive PFC utilize a filter at the AC input to rectify poor power factor. The passive PFC circuitry utilize just passive components - an inductor and some capacitors. despite the fact that it is simple and robust, a passive PFC rarely achieves low Total Harmonic Distortion (THD). Also, since the circuit works at the low line power frequency of 50Hz or 60Hz, the passive elements are generally large and heavy. Figure 1-2 shows input voltage and current for a passive PFC, and the harmonic spectrum of input current.The input power factor (PF) is defined as the ratio of the real power divided by apparent power as:

$$\text{Power Factor}(PF) = \frac{\text{Real Power } (W)}{\text{Apparent Power } (VA)} \tag{2.1}$$

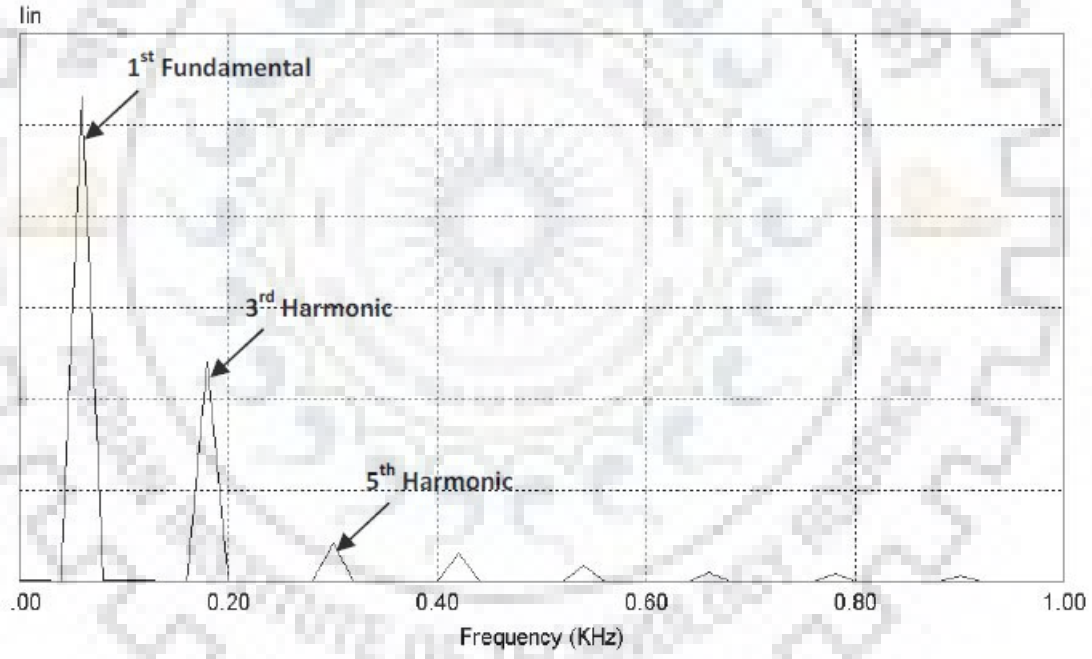
Assuming an ideal sinusoidal input voltage source, the power factor can be expressed as the multiplication of two factors, the distortion factor and the displacement factor, as given:

$$PF = K_d K_\theta \tag{2.2}$$

The distortion factor K_d is the ratio of the fundamental RMS current to the total RMS current.



(a) Input voltage and current waveform



(b) Input Current Harmonic Spectrum

Figure 2.2: Passive power factor correction AC main voltage and current waveforms

The displacement factor,K_θ, is the cosine of the displacement angle between the fundamental input current and the input voltage fundamental RMS current.

$$K_d = \frac{I_1 rms}{I_{rms}} \tag{2.3}$$

$$K_\theta = \cos\theta_1 \tag{2.4}$$

where, line current have I_{Irms} as the fundamental component, I_{rms} as the total line current, and θ_1 is the phase shift of the current fundamental relative to the sinusoidal line voltage. waveform in which distortion can be notice those also have the distortion factor nearly equal to one.so it is not very useful for measuring the distortion practically. but Total harmonic distortion is directly related to distortion factor.

$$THD = \sqrt{\frac{I_{rms}^2 - I_{1rms}^2}{I_1 rms^2}} \tag{2.5}$$

$$K_d = \sqrt{\frac{1}{1 + THD^2}} \tag{2.6}$$

K_d is regulated IEC 1000-3-2 [2] for lower power levels and by IEEE Std 519-1992 [11] for higher power levels, where K_{theta} is regulated by utility companies [12]

By using only the pulse width modulated (PWM) switching technique in the rectification of single phase AC supply we can diminish the current harmonics in the circuits.These converter can resemble like a resistive load and allow very little distortion in the current. these converter by using these modulation technique draw current close to sinusoidal shape with little distortion and higher PF ,this method calledas power factor correction(PFC) .By this research, the already exist based boost converter topology PFC technology with average current-mode control was noticeably improved,which increase the operating range of converter .

Chapter 3

LITERATURE REVIEW

3.1 CLASSIFICATION

B. Singh et al. [5] Discuss a whole analysis of improved power quality converters (IPQCs) configurations, control of applications,components selection,design attributes, other related considerations, and their suitability and selection for precise applications. It is examined to provide a broader overview on the repute of IPQC technology . A categorized listing of more than 450 research guides on the kingdom of art of IPQC is also given for a fast reference. And also includes the sequential development and the reputation of the IPQC era, explained four essential classes namely boost, buck, buck–boost, and multilevel converters which provide higher level of power quality at the input ac source and at dc output

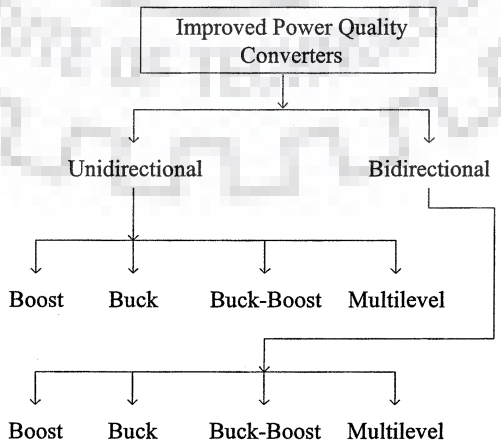


Figure 3.1: Topology-framework based characterization of improved power quality converters

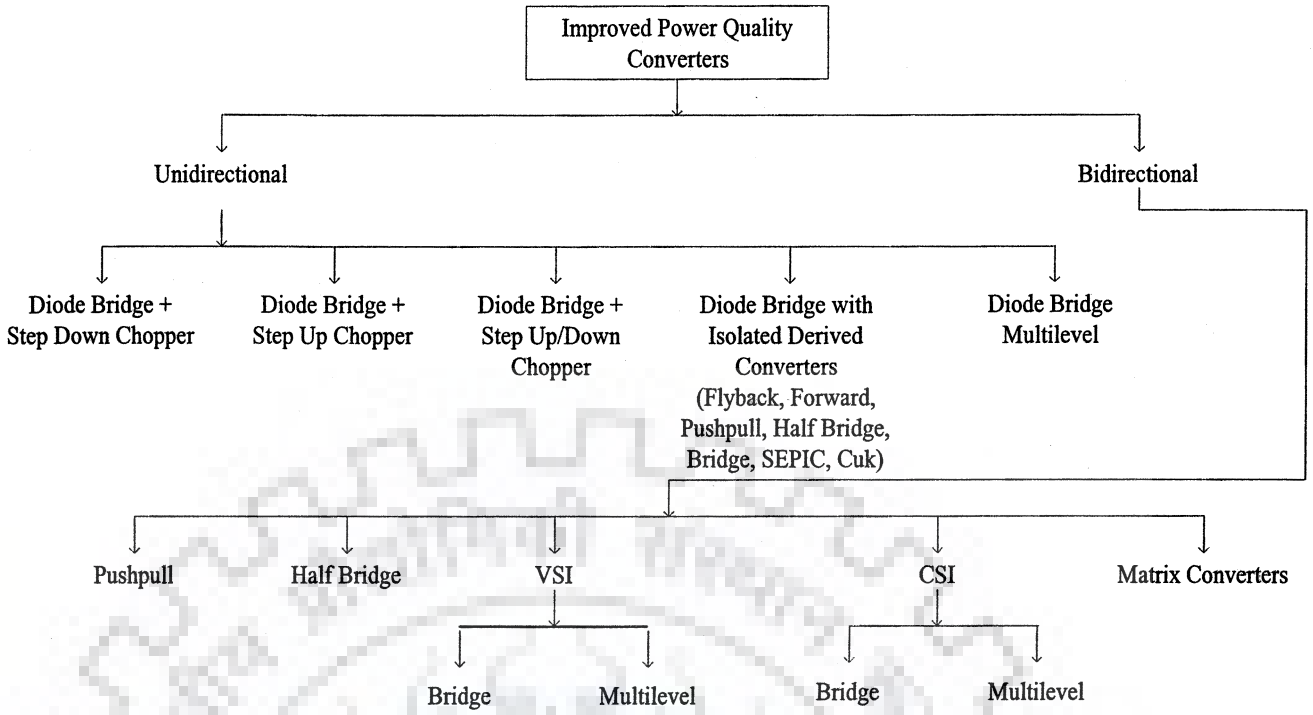


Figure 3.2: Converter-based arrangement of improved power quality converters

3.2 Component stress

L. Petersen et al. [8] In this paper,single organize topology is contrasted and the two phase topology PFC converter which utilized for the most recent decade and still proceeds. The objective of this paper is to draw the consideration on the quantitative investigation of power transferred. To think about the part stress, the after-effects of fundamental DC-DC topologies has been investigated. get the information to discover the elective arrangement of PFC converter and set against the normal two-stage solution.

With the assistance of the component load factors(CLF) looked at different converter topologies [13].other parameter Like cost,size and productivity in a roundabout way rely upon segment stress,so it is determined for fundamental topologies and considering segment stress change under various conditions .a framework of suitable arrangement are accomplished with and the investigation of what ought not to do. Bizarre segment stress is inspected with the data got from the utilization of CFL.

3.3 Investigate Current ripple in output capacitor

Dehong Xu et al. [14]Investigated output capacitor current ripple for Boost converte ,3-level converter with switch in a require range, two lower switches converter and totem pole converter with switch in a require range. Its effect on output voltage ripple and capacitor voltage stress is examined. In output capacitors Filter current ripples for these four topologies are contrasted and the method to select output capacitor according to current ripple capability of capacitor is enumerated.

3.4 Solution for the Issues such as Voltage and current sensing, EMI noise

Bing Lu at el. [15]completed the exploration to illuminate the voltage detecting, current detecting and EMI noise by one cycle control method. Ordinary boost PFC experiences the high conduction loss in the input rectifier bridge connected in frontend. High conversion efficiency can be accomplished by utilizing the bridgeless boost topology. This new circuit has issues, for example, voltage detecting, current detecting, and EMI noise. In this paper, one cycle control procedure is utilized to unravel the issues of the voltage detecting and current detecting. Exploratory outcomes show efficiency improvement and EMI execution

3.5 Current Distortion Problem at low Power

Costel Petrea at el. [16]The ordinary boost power factor remedy converter has high conduction loss as a result of the input rectifier bridge. The utilization of a bridgeless PFC circuit offers high efficiency. For high powers, the bridgeless circuit will be intended to work in persistent conduction mode (CCM), utilizing a normal current mode control. The switches have parasitic capacitances that in CCM lead to switch losses, without impacting the waveform of the converters. For low loads, the intermittent conduction mode Ml D3 M2 D4 (DCM) shows up, yet the parasitic capacitances lead to the input current distortion. This paper centers around the simulation and examination of bridgeless PFC converter working at higher load and lower load and potential answers for wipe out the distortion of the current working at low power.

3.6 Bridgeless P.F.C. Configuration

Ugo Moriconi et al. [17]portrays an inventive topology devoted to a medium to high power PFC organize. The innovation of this topology is the nonappearance of the bridge that generally is put between the EMC filter and the PFC stage. The upsides of this topology can be found as far as increased efficiency and improved thermal management.

3.7 Survey of basic AC– DC PFC topology

The conventional, bridgeless and interleaved boost converters are analyzed to use in front-end of ac– dc change in charging of battery in PHEV in the accompanying sub-section.

3.7.1 Conventional Boost Converter

The conventioal boost topology is the most renowned topology for PFC working. In PFC working, diode bridge is utilized to rectify the AC input voltage to DC , and after this the boost converter, as appeared in Figure. The output ripple current is high in this topology and is the contrast between the DC output current and the diode current. At high power level in the diode connect ,losses become essentially expansive and decline the

effectiveness, so worried with the heat dissemination in a restricted area progresses toward becoming issue. considering above limitations, this topology is works useful for a low to medium power extend, up to about 1 kW. Above 1KW power level, architects inclines toward parallel semiconductors so as to give more output power. Size of inductor likewise turned out to be big issue at high power in view of the restricted core size accessible for the power level and the overwhelming wire check required for winding.

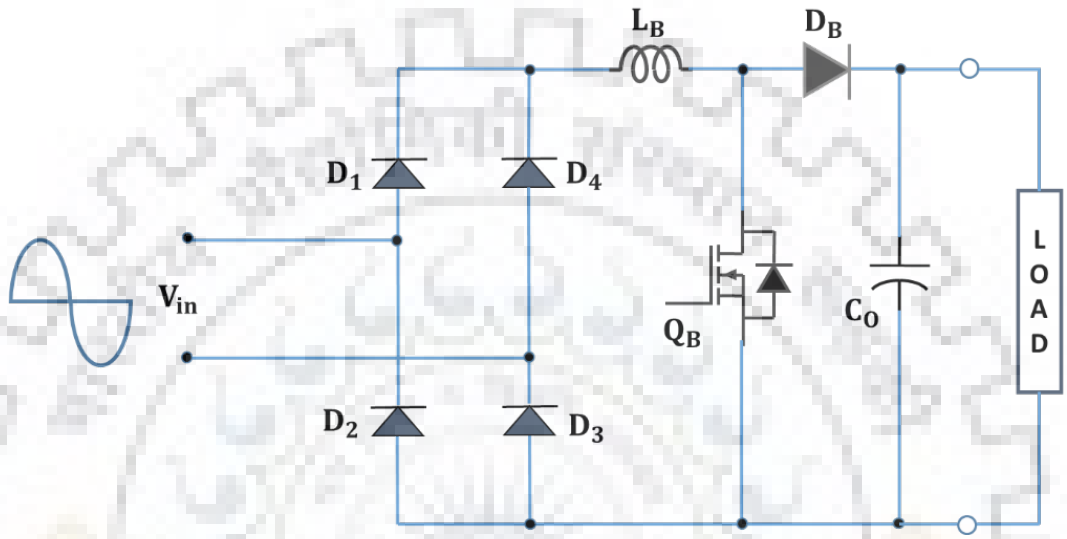


Figure 3.3: Conventional PFC boost converter

3.7.2 Bridgeless Boost Converter

Information connect rectifier isn't required in the bridgeless boost PFC topology in contrast with the Boost AC-DC PFC converter, still, it keeps up the great boost topology. [15–21], as shown in Fig.3.4. It is useful for applications at power levels more prominent than 1 kW, where efficiency and power density are critical. This topology evacuate the issue of heat management in the input rectifier diode bridge, yet the drawback is that expanded EMI present in the circuit [22–24]. skimming input line as for the PFC organize ground is the Another bad mark of this topology, therefore without a low an optical coupler or frequency transformer it unfit to detect the input voltage. Additionally, there is a need of complex hardware so as to detect the input current, current in the MOSFET and diode ways independently, in light of the fact that every half-line cycle current path does not have a similar ground [17, 25]

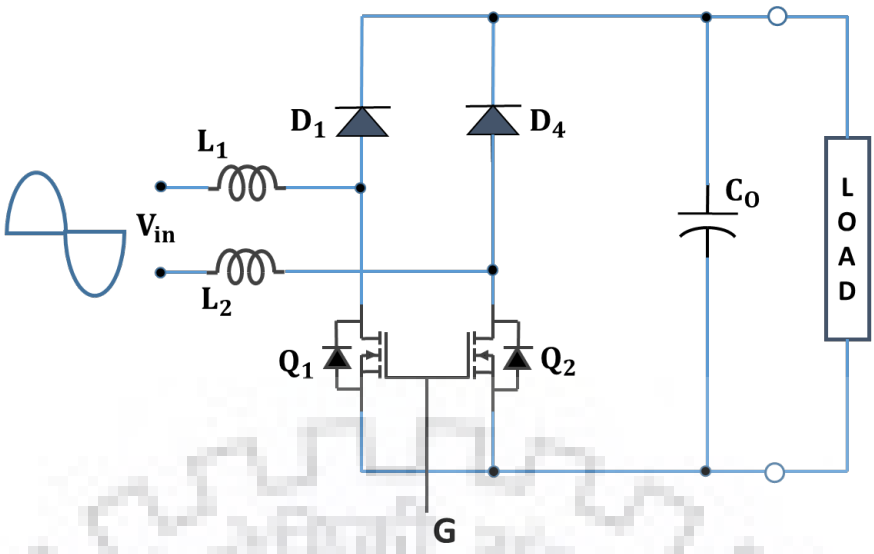


Figure 3.4: without rectifying Bridge PFC boost converter

3.7.3 Interleaved Boost Converter

The interleaved boost converter, shown in Figure.3.5, compose of parallelly connected two boost converter , working 180° out of phase with the help of switching pulses [19, 26, 27]. The input current is the summation of the two inductors currents in L_{B1} and L_{B2}. parallel-ling of boost converter result into many merits. The ripple currents flows in these inductors are out of phase, subsequently they counteract one another, and thusly decrease the high frequency input ripple current delivered by the boost switching action, so the measure of input EMI filter is diminished [28–30].

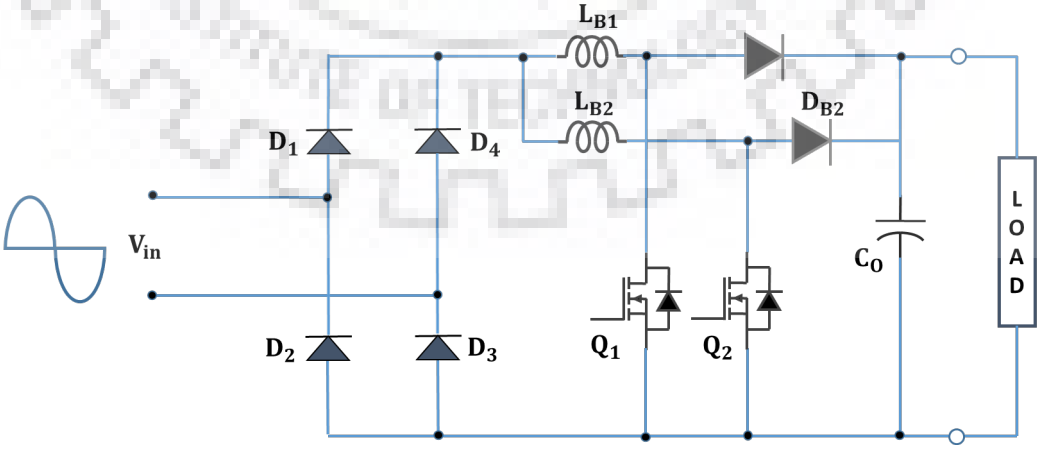


Figure 3.5: Interleaved PFC boost converter

further, the favorable position of this topology is to decrease conduction losses as semiconductors are associated parallelly. hence, high frequency ripple in the output capacitor is additionally diminished. One important inconvenience of the interleaved boost PFC converter is the heat management the executives in the input diode bridge similar as was in the boost PFC converter.

In the resulting area, another BLIL boost PFC converter is prescribed. The boost diode rectifier bridge is dispensed with this high efficiency at power levels over 3 kW is accomplished in proposed topology and its attributes of low EMI due to interleaving, which is an innate advantageous nature of the boost and interleaved boost PFC topologies.

Chapter 4

PROPOSED BLIL BOOST TOPOLOGY

To address the issues as talked about in chapter3 the BLIL PFC converter topology as appeared in Fig.4.1 . The number of semiconductor device used in this converter is similar as in interleaved boost PFC converter.In contrast with interleaved help PFC converter ,it required two more MOSFETs and two quick diodes rather than four moderate diodes utilized in the input bridge of interleaved boost PFC converter . Proposed Converter operation and steady-state analysis is done in the upcoming section. Table 4.1 summarizes the merits and demerits of the proposed topology and the three topologies reviewed in chapter 3

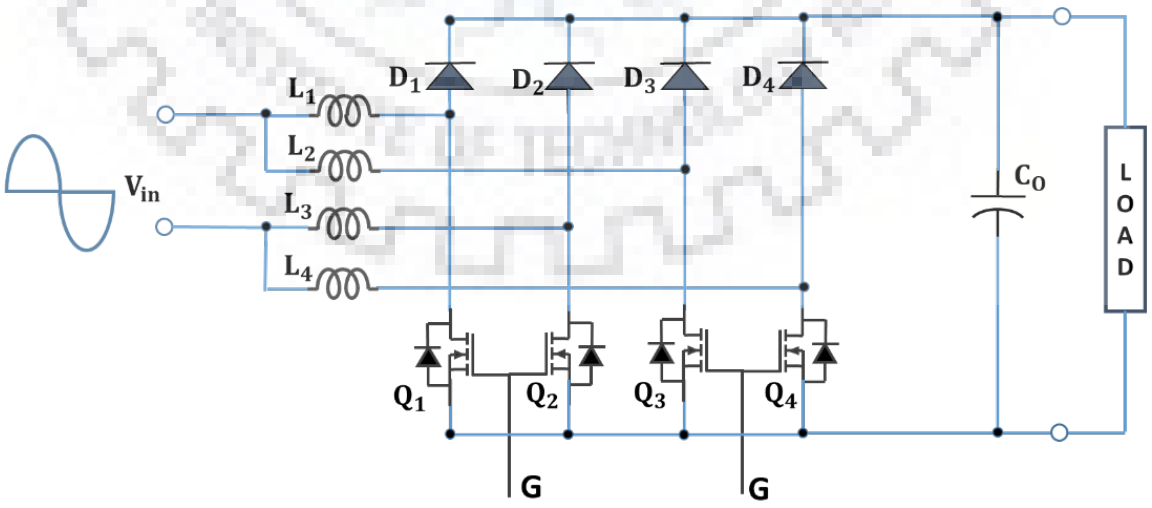


Figure 4.1: Proposed BLIL PFC boost converter

Table 4.1: COMPARISON OF AC-DC PFC TOPOLOGIES FOR PHEV BATTERY CHARGING

Topology	Conventional PFC	Bridgeless PFC	Interleaved PFC	BLIL PFC
Power Rating	< 1000 W	< 2000 W	< 3000 W	> 3000 W
EMI/Noise	Fair	Poor	Best	Fair
Capacitor Ripple	High	High	Low	Low
Input Main Ripple	High	High	Low	Low
Magnetic Size	Large	Medium	Small	Small
Efficiency	Poor	Fair	Fair	Best
Cost	Low	Medium	Medium	High

Chapter 5

OPERATIONAL ANALYSIS

5.1 CIRCUIT WORKING AND STEADY-STATE EXAMINATION

To eliminate the short coming of the topologies described in Chapter 3 for the conventional boost, bridgeless boost, and interleaved boost topologies, The bridgeless interleaved (BLIL) PFC converter [31] is proposed as shown in Figure 4.1 .Instead of four moderate diodes as utilized in the information extension of the standard interleaved boost PFC converter , BLIL converter presents two more MOSFETs and two all the more quick diodes.To comprehend the circuit task , the input supply cycle has been partitioned into the positive and negative half cycles, as portrayed in sub-segments that pursue.What's more, depending on the duty cycle the detailed circuit operation is additionally portrayed, thusly positive half cycle task investigation is accommodated for D $>$ 0.5 and D $<$ 0.5.

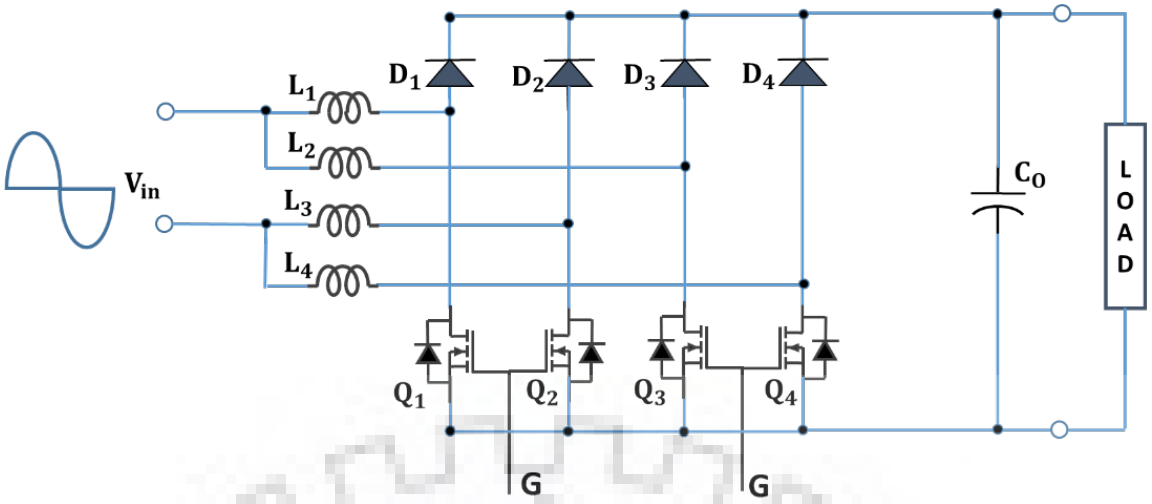


Figure 5.1: BLIL PFC boost converter

5.1.1 Positive Half Cycle working

Refers to Figure 5.2,In the positive half cycle of AC input voltage, PAIR-1 switches (Q1&Q2) switch on and current moves through L1 and Q1 and proceeds through Q2 (and in part its body diode) and afterward L2, come back to the supply line with putting away energy in L1 and L2. When Q1 and Q2 switch off, energy put in L1 and L2 is put away as current moves through D1, through the load and come back through the body diode of Q2 back to the input mains supply.

With interleaving, the similar thing happens for Q3 and Q4, but with a 180° phase delay. The working for this mode is PIAR-2 switches (Q3 and Q4) on putting energy in SET-2 (L3 and L4) inductors by the path L3-Q3-Q4-L4 back to the input. When Q3 and Q4 switch off, energy is given away through D3 to the load and coming back by the body diode of Q4 back to the input mains.

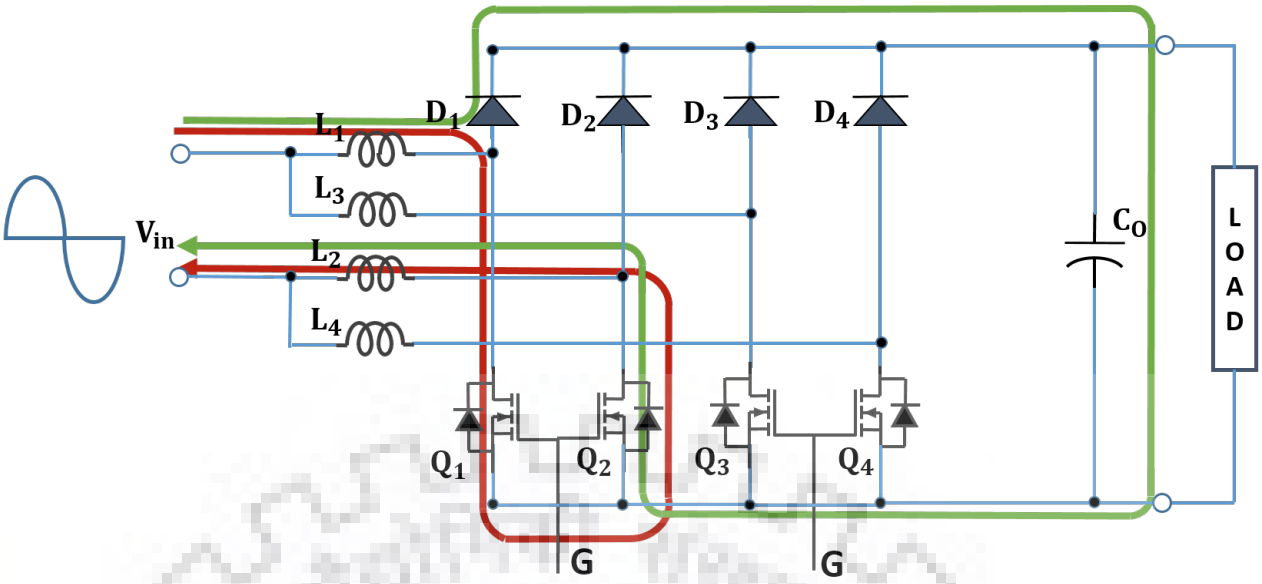


Figure 5.2: Positive Half Cycle working

5.2 Negative Half Cycle working

Refers to Fig. 4-1, In the negative half cycle, During negative ac input supply voltage , Q1*and*Q2 switch on and current moves through L2 and Q2 and proceeds through Q1 (and part of its by body diode) and then L1, coming back to the line while putting energy in L2 and L1. When Q1 and Q2 switch off, energy put in L2 and L1 is given as current moves through D2, through the load and comes back by the body diode of Q1 back to the input mains.

With interleaving, the similar mode occurs for Q3 and Q4, but with a 180° phase delay. The working for this mode has Q3 and Q4 on, putting energy in L3 and L4 by the path L4-Q4-Q3-L3 back to the input.

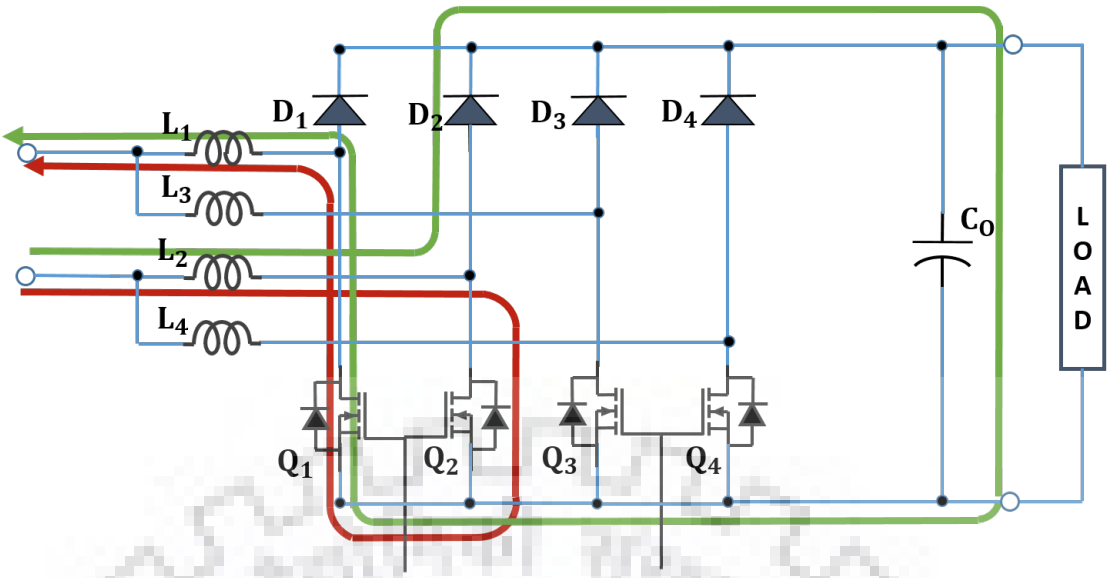


Figure 5.3: Negative Half Cycle working

5.2.1 Point by point Positive Half Cycle working and study for D > 0.5

The total working of the proposed BLIL PFC converter relies on the duty cycle. During any half cycle, the converter duty cycle is either more than 0.5 (when the input voltage is smaller than half of output voltage) or less than 0.5 (when the input voltage is more than half of output voltage).

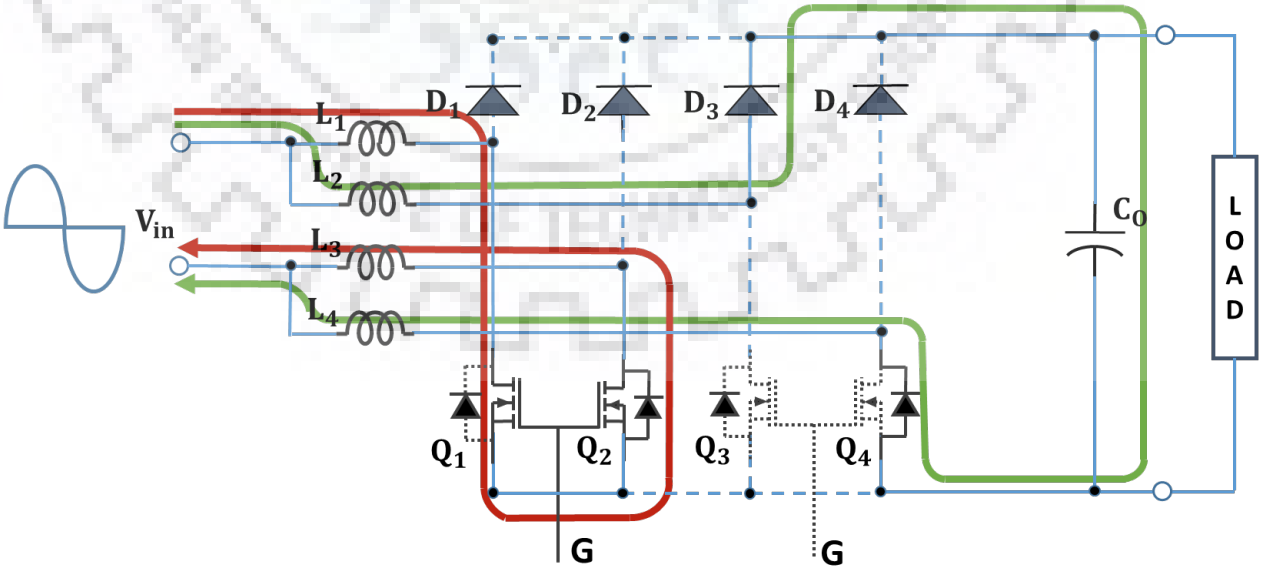


Figure 5.4: During Interval 1 when PAIR-1 switches are high and body diode of Q4 working

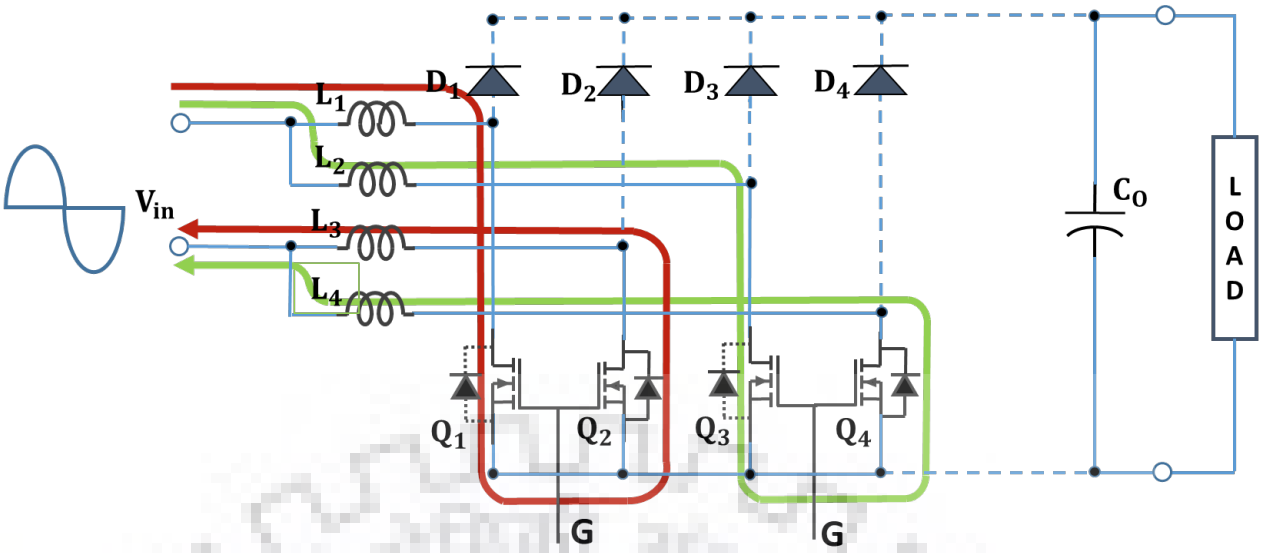


Figure 5.5: During Interval 2 and 4,when all switches are high

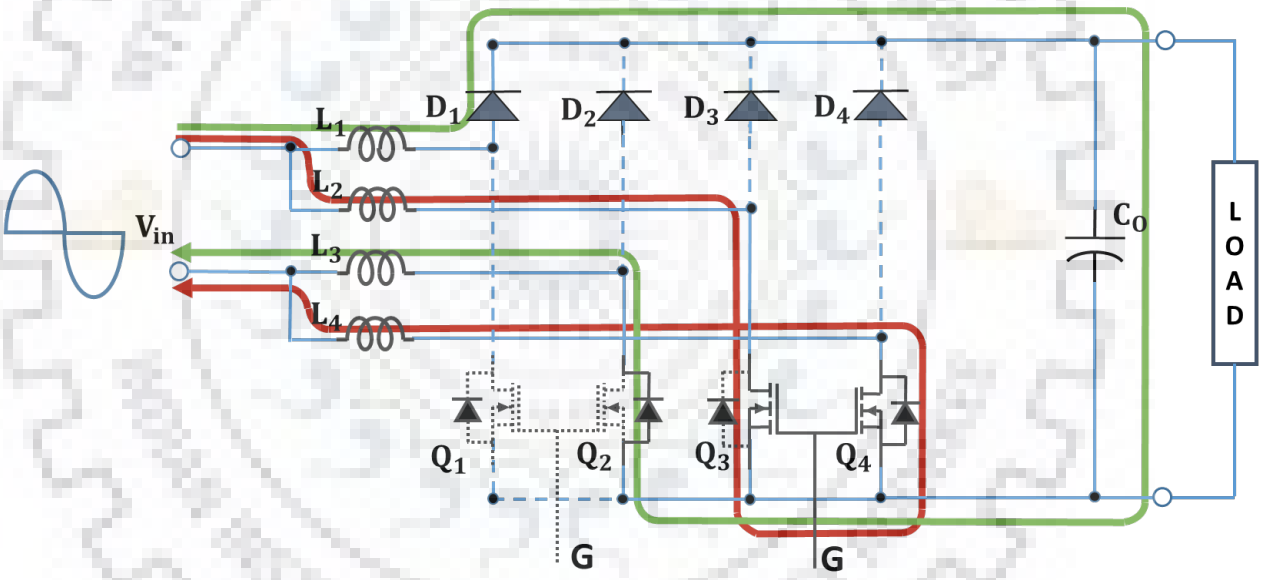


Figure 5.6: During Interval 3 PAIR-2 switches are high,and body diode of Q2 working

Figures 5.4 to 5.6 demonstrate the three one of a kind working interval circuits of the proposed converter for duty cycles more than 0.5 in a positive half cycle operation. Waveforms of the proposed converter in these conditions are illustrated in Figure **??** and Figure**??**.

Because the switching frequency of proposed converter is quite higher than the frequency of input line voltage, the input voltage V2 is taken into consideration constant

for the duration of one switching period T4. The input voltage is given by:

$$v_i = \sqrt{2} V_s \sin(\theta) \tag{5.1}$$

During positive half cycle of the input voltage, the duty ratio of the BLIL converter decides the following voltage relation:

$$\frac{V_o}{v_i} = \frac{1}{1-D} \tag{5.2}$$

The time periods of operation are mentioned as follows. In addition, the ripple current components are derived, helped in calculation of the input ripple current, which give designing information to satisfy the required input current ripple standard.

Interval 1 $(t_0 - t_1)$

At a point t_0,when G1 is high while G2 is low,as shown in Figure.5.4. Throughout this interval the current in the SET-1(L1&L2) inductors rise gradually and putting energy in these inductors. The ripple currents of PAIR-1(Q1&Q2) switches are same as of SET-1 inductors.,its equation given by,

$$\Delta i_{L1} = \frac{1}{L_1 + L_2} v_i (1-D) T_s \tag{5.3}$$

The input ripple current is the addition of SET-1 and SET-2 inductors:

$$\Delta I_{in} = \frac{1}{L_1 + L_2} V_O (1-D) T_S \tag{5.4}$$

Interval 2 $(t_1 - t_2)$

At a point t_1,when G2 is high while G1 is already high,as shown in Figure.5.5. Throughout this interval the current in the all the inductors rise gradually and putting energy in these inductors. The ripple currents of PAIR-1(Q1&Q2) switches are same as of

SET-1(L1&L2) inductors

$$\Delta i_{L1} = \frac{1}{L_1 + L_2} v_i \left(D - \frac{1}{2} \right) T_S \tag{5.5}$$

likewise, the ripple currents of Pair two switches which contain Q3&Q4 (PAIR-2) are same as in set of series inductor, which contain L3&L4(SET-2)

$$\Delta i_{L3} = \frac{1}{L_3 + L_4} v_i \left(D - \frac{1}{2} \right) T_S \tag{5.6}$$

The input ripple current is the addition of SET-1 and SET-2 inductors:

$$\Delta I_{in} = \frac{2}{L_1 + L_2} v_i \left(D - \frac{1}{2} \right) T_S \tag{5.7}$$

Interval 3 $(t_2 - t_3)$

At a point t_2,when G1 is low while G2 is already high,as shown in Figure.5.6. Throughout this interval the current in the SET-2(L3&L4) inductors rise gradually and putting energy in these inductors. The ripple currents of PAIR-2(Q3&Q4) switches are same as of SET-2 inductors.

$$\Delta i_{L3} = \frac{1}{L_3 + L_4} v_i (1 - D) T_S \tag{5.8}$$

The current in SET-1(L1&L2) gradually reduce through D1,Co and body diode of Q2 and transfer the energy to the load .The ripple current in the SET-1 series inductors, which contain L1&L2 is given by

$$\Delta i_{L1} = \frac{1}{L_1 + L_2} \left(V_o - v_i \right) (1 - D) T_S \tag{5.9}$$

The input ripple current is the addition of SET-1(L1&L2) and SET-2 (L1&L2) inductors

$$\Delta I_{in} = \frac{1}{L_1 + L_2} V_o (1 - D) T_s \tag{5.10}$$

Interval 4 $(t_3 - t_4)$

At a point t_3,when G2 is high while G1 is already high,as shown in Figure.5.5. Throughout this interval the current in the all inductors rise gradually and putting energy in all the inductors. The ripple currents of Q1&Q2 are same as of L1&L2 :

$$\Delta i_{L1} = \frac{1}{L_1 + L_2} v_i \left(D - \frac{1}{2} \right) T_s \tag{5.11}$$

likewise, the ripple currents of Pair two switches which contain Q3&Q4 (PAIR-2) are same as in set of series inductor, which contain L3&L4(SET-2)

$$\Delta i_{L3} = \frac{1}{L_3 + L_4} v_i \left(D - \frac{1}{2} \right) T_s \tag{5.12}$$

The input ripple current is the addition of SET-1 and SET-2 inductors:

$$\Delta I_{in} = \frac{2}{L_1 + L_2} v_i \left(D - \frac{1}{2} \right) T_S \tag{5.13}$$

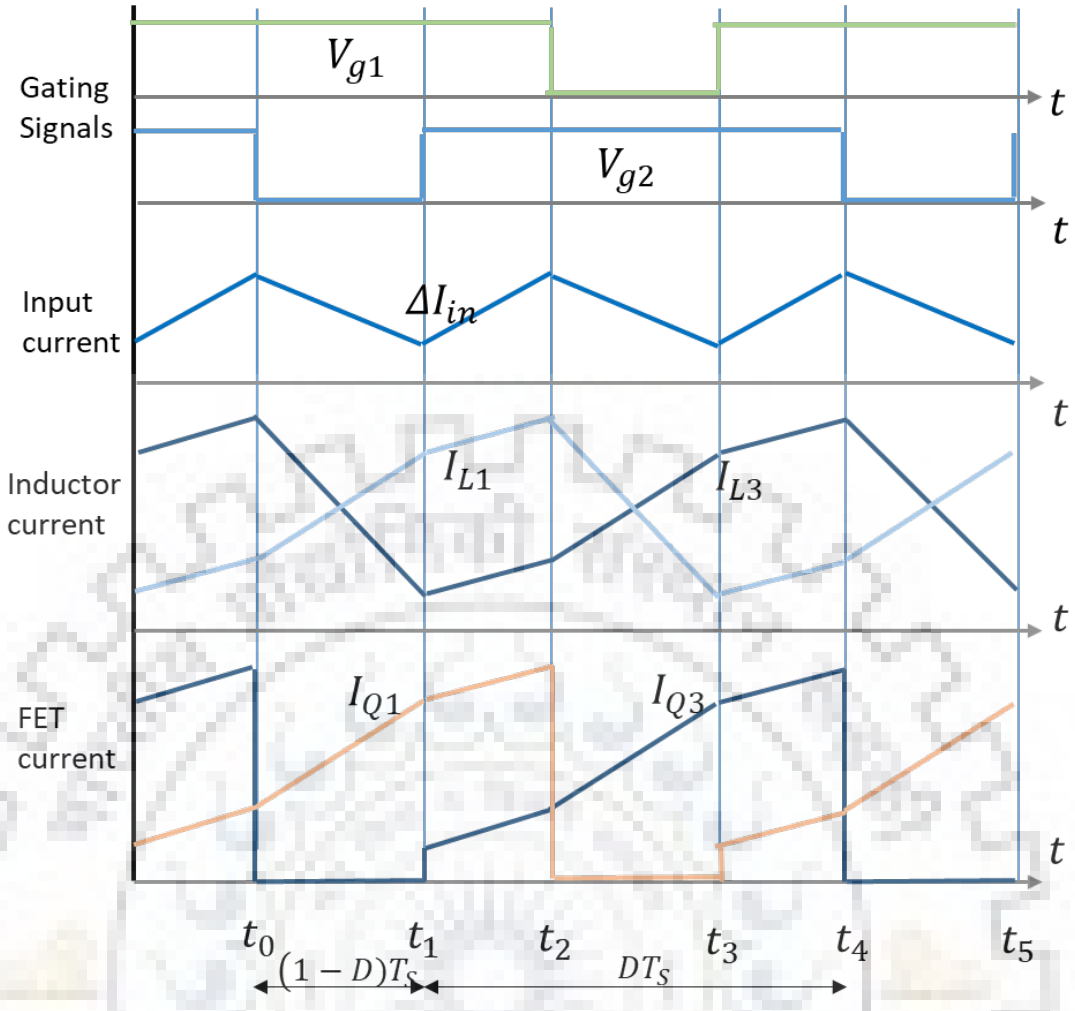


Figure 5.7: for D > 0.5,steady-state Waveforms of BLIL PFC boost converter.

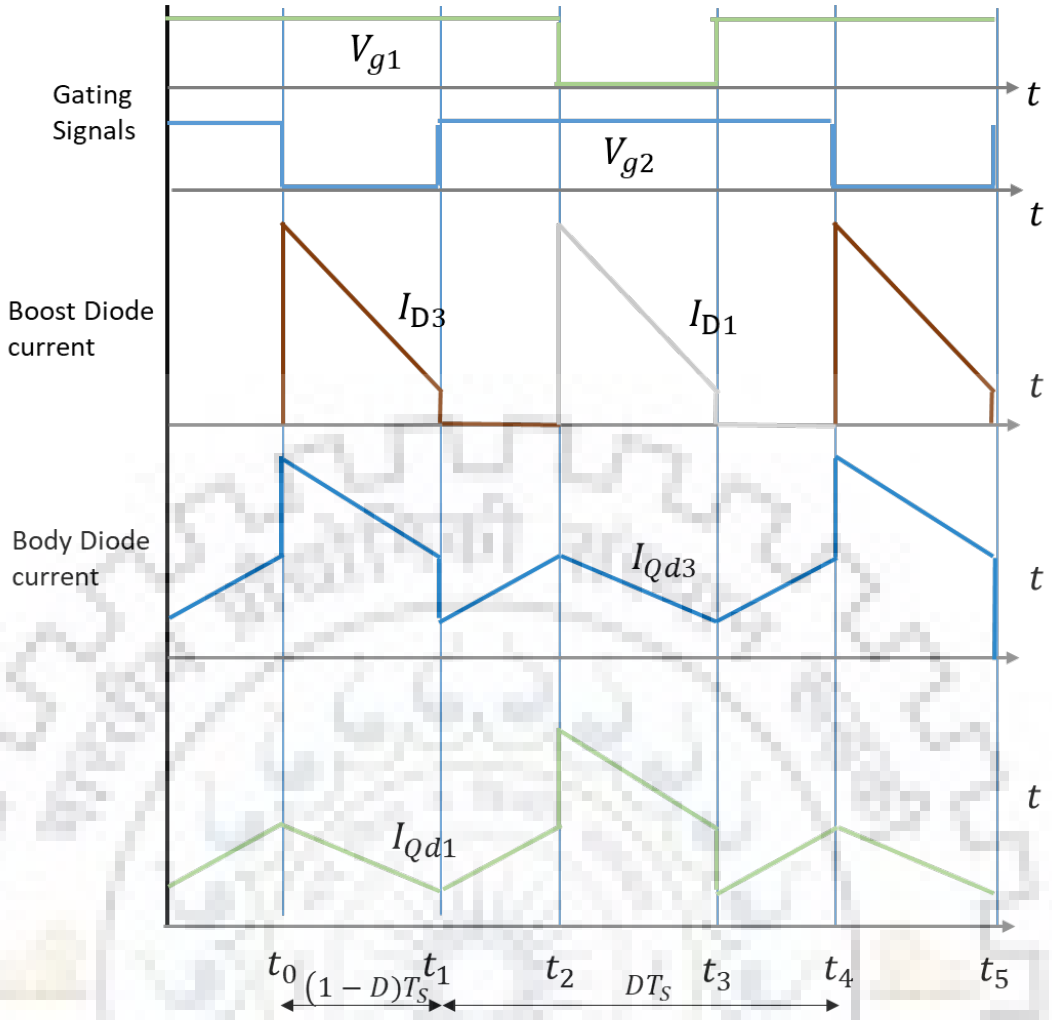


Figure 5.8: for D > 0.5,steady-state Waveforms of BLIL PFC boost converter

5.2.2 Point by point Positive Half Cycle working and study for D < 0.5

Figure5.9 to Figure 5.11 illustrate the working interval circuits of the proposed converter for duty cycles less than 0.5 in the positive half cycle. The waveforms of the proposed converter in these state are illustrated in Figure . The working of intervals are discribed as follows:

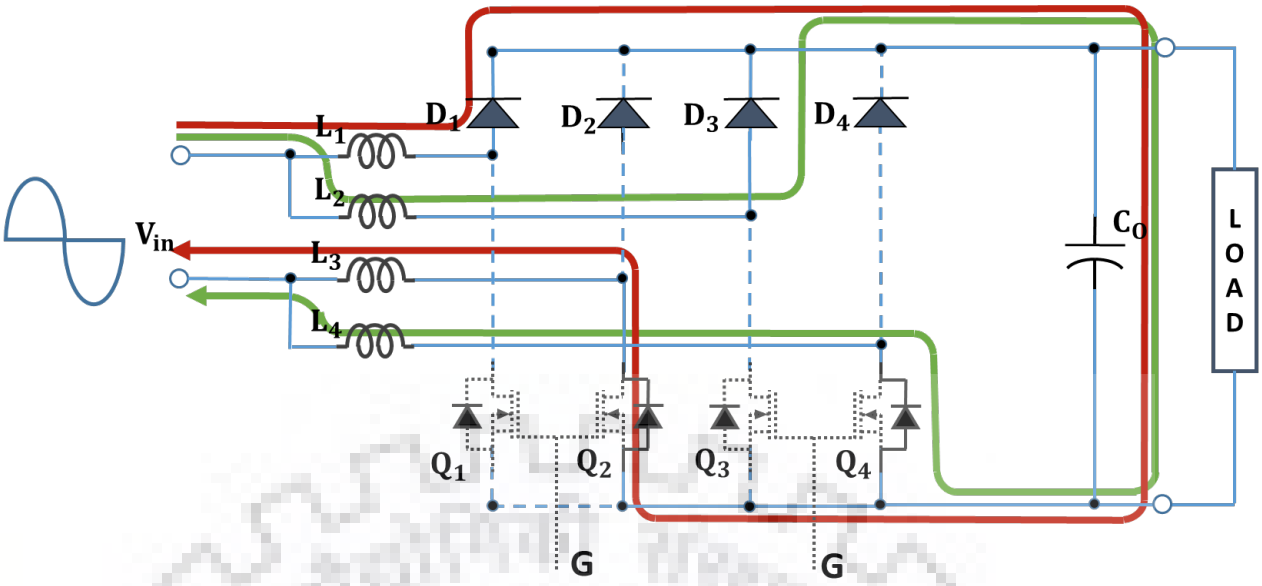


Figure 5.9: Body diodes of Q2 and Q4 conducts in Interval1 and 3

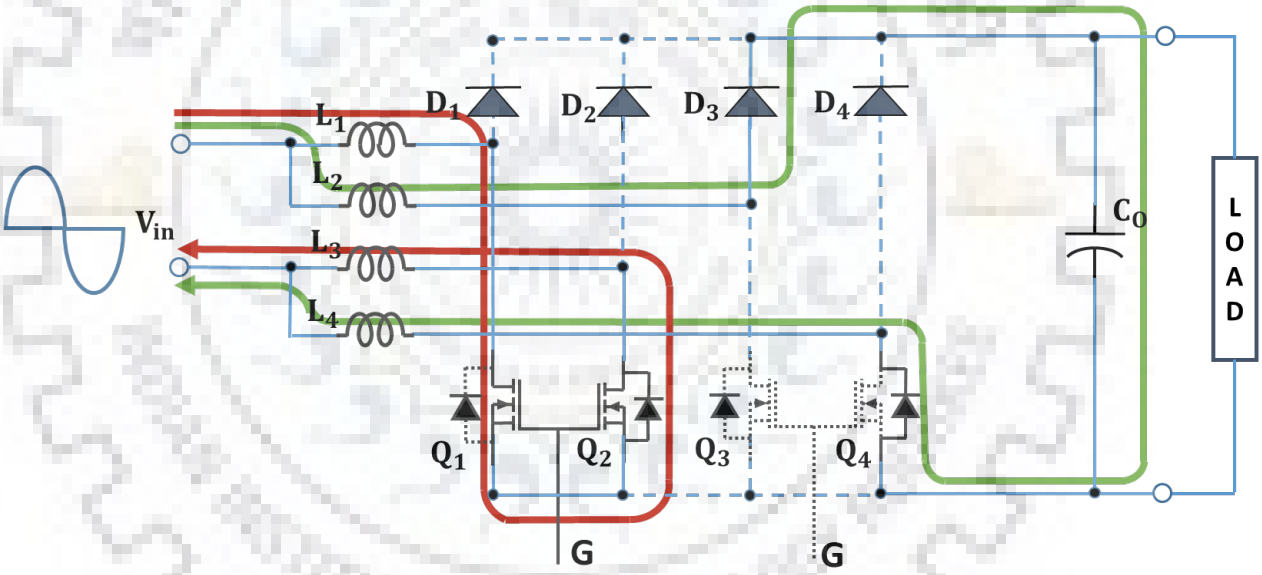


Figure 5.10: PAIR-1 switches are switch ON,and body diode of Q4 conducts in Interval 2

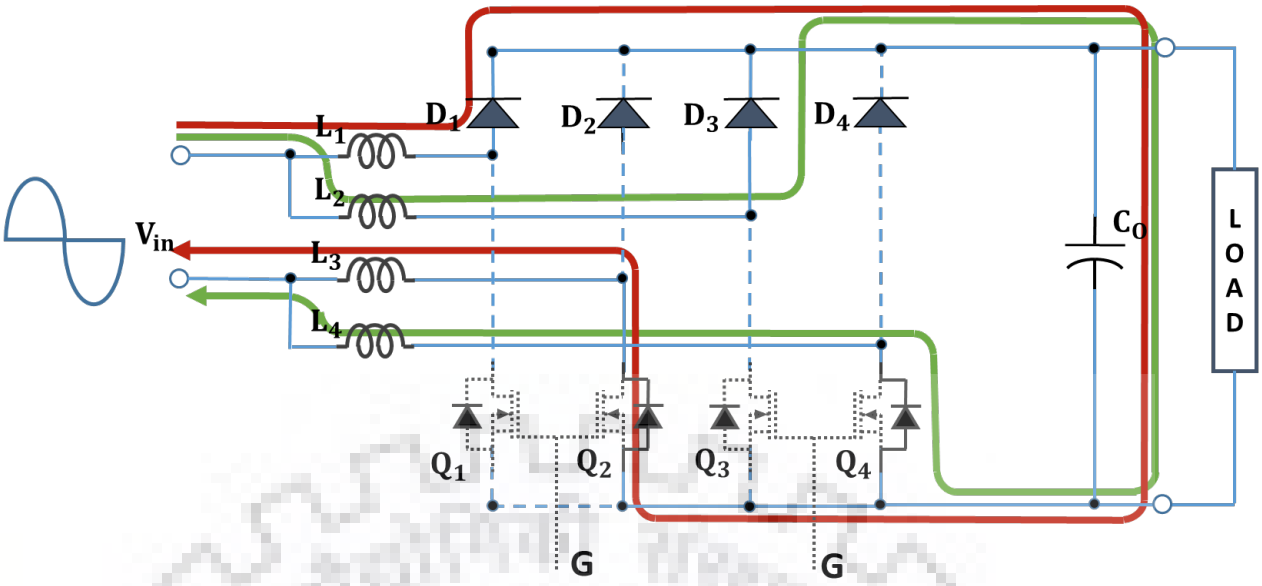


Figure 5.11: PAIR-2 switches are switch ON,and body diode of Q2 conducts in Interval 4

Interval 1 $(t_0 - t_1)$

At a point t_0,when G1 is low while G2 is already high ,as shown in Figure.5.9. Throughout this interval the current in the SET-1(L1&L2) inductors rise gradually and putting energy in the load by the path following D1,Co, and body diode of Q2. The ripple currents of of SET-1 inductors.,its equation given by,

$$\Delta i_{L1} = \frac{1}{L_1 + L_2} (V_o - v_i) \left(\frac{1}{2} - D \right) T_S \tag{5.14}$$

Apart from this, the current through the SET-2 inductor also decreases gradually, transfer the energy to the load by D3, Co and body diode of Q4. The ripple current in i the SET-2 inductor is:

$$\Delta i_{L3} = \frac{1}{L_3 + L_4} (V_O - v_i) \left(\frac{1}{2} - D \right) T_S \tag{5.15}$$

The input current is the addition of currents in L1/L2 and L3/L4:

$$\Delta I_{in} = \frac{2}{L_1 + L_2} (V_O - v_i) \left(\frac{1}{2} - D \right) T_S \tag{5.16}$$

Interval 2 $(t_1 - t_2)$

At a point t_1,when G1 is high while G2 is low,as shown in Figure.5.10. Throughout this interval the current in the SET-1(L1&L2) inductors rise gradually and putting energy in these inductors. The ripple currents of PAIR-1(Q1&Q2) switches are same as of SET-1 inductors.,its equation given by,

$$\Delta i_{L1} = \frac{1}{L_1 + L_2} v_i D T_S \tag{5.17}$$

The current in SET-2 inductor decreases gradually and transfer the energy to the load by D3, Co and body diode of Q4. The ripple current in L3 and L4 is:

$$\Delta i_{L3} = \frac{1}{L_3 + L_4} (V_o - v_i) D T_S \tag{5.18}$$

The input ripple current is the addition of the currents in SET-1 and SET-2 inductors:

$$\Delta I_{in} = \frac{1}{L_1 + L_2} V_o D T_S \tag{5.19}$$

Interval 3 $(t_2 - t_3)$

At a point t_2,when G1 is low while G2 is already low,as shown in Figure.5.9. Throughout this interval the current in the SET-1(L1&L2) inductors reduce gradually and tranfer energy to the load by D1,Co and body diode of Q2. The ripple currents of SET-1 inductors,its equation given by,

$$\Delta i_{L1} = \frac{1}{L_1 + L_2} (V_o - v_i) \left(\frac{1}{2} - D \right) T_S \tag{5.20}$$

likewise, the current in the SET-2(L3&L4) inductors reduce gradually and tranfer energy to the load by D3,Co and body diode of Q4. The ripple currents of SET-2 inductors,its equation given by,

$$\Delta i_{L3} = \frac{1}{L_3 + L_4} (V_o - v_i) \left(\frac{1}{2} - D \right) T_s \tag{5.21}$$

The input current is the addition of currents in SET-1 and SET-2 inductors:

$$\Delta I_{in} = \frac{2}{L_1 + L_2} (V_o - v_i) \left(\frac{1}{2} - D \right) T_S \tag{5.22}$$

Interval 4 $(t_3 - t_4)$

At a point t_3,when G2 is high while G1 is already low ,as shown in Figure.5.11. Throughout this interval the current in the SET-2(L3&L4) inductors rise gradually and putting energy in these inductors. The ripple currents of PAIR-2(Q3&Q4) switches are same as of SET-2 inductors.its equatio given by

$$\Delta i_{L3} = \frac{1}{L_3 + L_4} v_i D T_S \tag{5.23}$$

The current in SET-1 inductors gradually reduce and transfer the energy to the load by D2, Co and body diode of Q4. The ripple current in SET-1 inductors is:

$$\Delta i_{L1} = \frac{1}{L_1 + L_2} (V_o - v_i) D T_s \tag{5.24}$$

The input current is the addition of currents in SET-1 and SET-2 inductors:

$$\Delta I_{in} = \frac{1}{L_1 + L_2} V_o D T_s \tag{5.25}$$

The working of converter in the negative half cycle of input voltage is identical to the working of converter in the positive half cycle of input voltage.

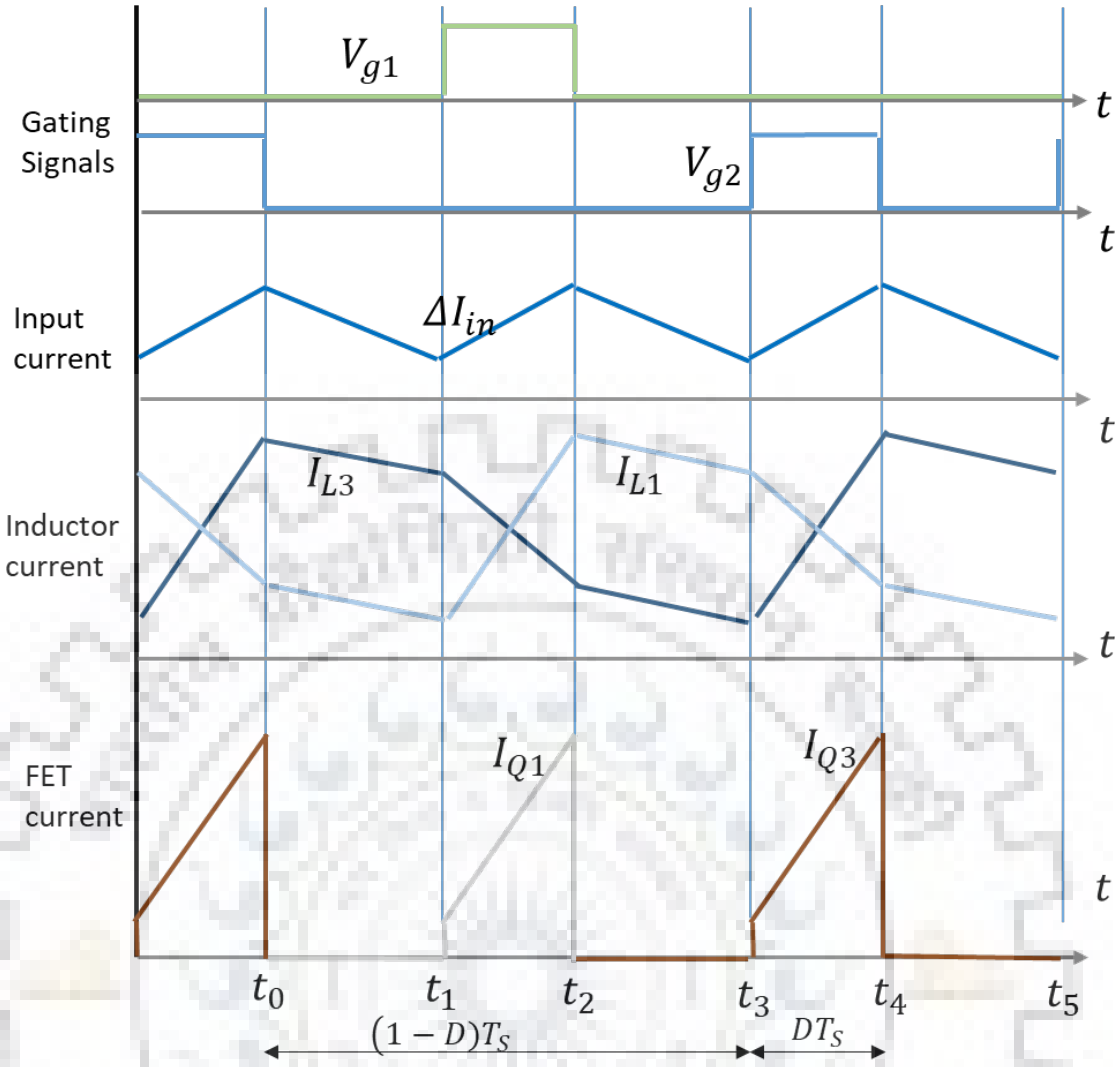


Figure 5.12: for D > 0.5,steady-state Waveforms of BLIL PFC boost converter

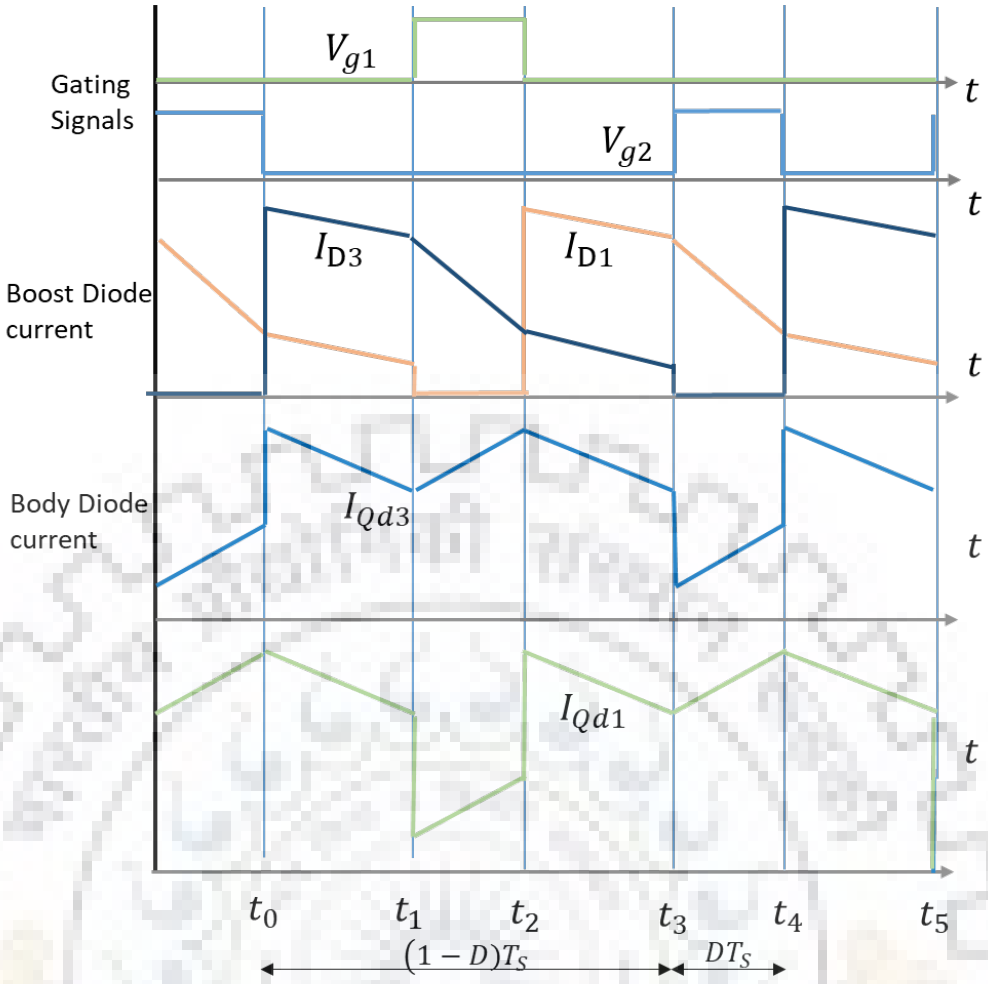


Figure 5.13: for D > 0.5,steady-state Waveforms of BLIL PFC boost converter

Chapter 6

ANALYTICAL MODELING

In order to properly select the power stage components of a converter and calculate the associated power losses, it is necessary to perform a current stress analysis. To do so, analytical expressions are required; including RMS switch and inductor current stresses and average diode current stress. In a typical boost converter, the MOSFET and diode current waveforms are pulsed-width modulated, with both the duty cycle and peak amplitude varying with the ac input, so analytical modeling is challenging, and is most often performed using circuit simulation. However, without an effective mathematical method for determining these RMS and average values, the design and selection of power stage components can be flawed. Therefore, this sub-section proposes an analytical model that can be used for all boost derived PWM PFC regulators. The following assumptions were made in order to analyse the converters and to derive the stress equations:

a) continuous conduction mode (CCM) working is assumed;

b)assumed as unity power factor. i.e., the line current is in phase and shape with the input line voltage as a sinusoidal waveform;

c) the PFC output voltage is dc with no voltage ripple.

In a typical boost converter, the converter MOSFET duty cycle is given by

$$\delta_Q(\theta) = 1 - \frac{|V_{IN}(\theta)|}{V_O} = 1 - \frac{V_{PK}|\sin(\theta)|}{V_o} \tag{6.1}$$

Assuming the inductor current is a sinusoidal waveform

$$i_L(\theta) = I_{PK}|\sin(\theta)| \tag{6.2}$$

The instantaneous MOSFET current and its RMS current can be derived respectively:

$$i_Q(\theta) = I_{PK}|\sin(\theta)|.i_L(\theta) \tag{6.3}$$

The converter MOSFET duty cycle RMS and its RMS current can be derived, respectively

$$\delta_{Q-mns}(\theta) = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left(1 - \frac{V_{PK}|\sin(\theta)|}{V_o}\right)^2 d\theta} \tag{6.4}$$

$$I_{Q-rms}(\theta) = \sqrt{\frac{1}{\pi}\int_0^{x}\left[I_{PK}|\sin(\theta)|\left(\delta_Q(\theta)\right)\right]^2 d\theta} \tag{6.5}$$

The high frequency inductor current ripple is assumed to be half of peak inductor current in each channel for an interleaved boost converter

$$\Delta I_{RP} = \frac{1}{2}\frac{I_{PK}}{2} \tag{6.6}$$

The high frequency ripple component of the inductor current is assumed to be a triangular waveform with a fixed duty cycle, so the RMS current in each inductor is defined by

$$I_{L-rms}(\theta) = \sqrt{\left(\frac{1}{\sqrt{2}}\frac{I_{PK}}{2}\right)^2 + \left(\frac{1}{2\sqrt{3}}\Delta I_{RP}\right)^2} = \frac{5}{4\sqrt{3}}\frac{P_{in}}{V_{PK}} \tag{6.7}$$

The boost diode duty cycle is given by

$$\delta_D(\theta) = 1 - \delta_Q(\theta) = \frac{V_{PK}|\sin(\theta)|}{V_O} \tag{6.8}$$

Therefore, the instantaneous boost diode current and its average current can be derived, respectively

$$I_D(\theta) = I_{PK}|\sin(\theta)|\frac{V_{PK}|\sin(\theta)|}{V_o} \tag{6.9}$$

$$I_{D-\sigma ve} = \frac{1}{\pi}\int_0^{\pi} I_{PK}|\sin(\theta)|\left(\frac{V_{PK}|\sin(\theta)|}{V_o}\right)d\theta \tag{6.10}$$

The output capacitor current has high frequency and low frequency components. The low frequency component is simply given by

$$I_{C-ms(\mathrm{LF})} = \frac{I_o}{\sqrt{2}} = \frac{1}{2}\frac{P_o}{V_o} \tag{6.11}$$

And the high frequency RMS ripple current component is [32]

$$I_{C-ms(\mathrm{HF})} = \frac{P_{in}}{V_o} = \sqrt{\frac{16V_o}{6\pi V_{PK}} - \frac{P_o^2}{P_{in}^2}} \tag{6.12}$$

The same method was used to derive RMS current in different topologies. Table 6.1shows a summary of component RMS current stress for conventional boost converter and bridgeless boost converter. Table 6.2 provides the same summary for interleaved boost converter and bridgeless interleaved boost converter.

Table 6.1: Brief description of the component current stresses for the conventional boost,Bridgeless

Topology	Conventional PFC	Bridgeless PFC
Inductor RMS current	$\sqrt{\frac{97}{48}\frac{P_{in}}{V_{PK}}}$	$\sqrt{\frac{97}{48}\frac{P_{in}}{V_{PK}}}$
Input Bridge Diode Average Current	$\frac{2}{\pi}\frac{P_{in}}{V_{PK}}$	NA
Fast Diode Average Current	$\frac{P_{in}}{V_o}$	$\frac{1}{2}\frac{P_{in}}{V_o}$
MOSFET RMS Current	$\frac{P_{in}}{\sqrt{6}V_0V_{PK}}\sqrt{\left(\frac{3\pi(4V_0^2+3V_{PK}^2)-64V_{PK}V_0}{\pi}\right)}$	$\frac{P_{in}}{\sqrt{6}V_0V_{PK}}\sqrt{\left(\frac{3\pi(4V_0^2+3V_{PK}^2)-64V_{PK}V_0}{\pi}\right)}$
MOSFET Intrinsic Body Diode Average Current	NA	$\frac{1}{2}\frac{P_{in}}{V_o}$
Output Capacitor RMS Ripple Current (Low Frequency)	$\frac{\sqrt{2}}{2}\frac{P_o}{V_o}$	$\frac{\sqrt{2}}{2}\frac{P_o}{V_o}$
Output Capacitor RMS Ripple Current (High Frequency)	$\frac{\sqrt{2}}{2V_o}\sqrt{3P_{in}^2-2P_o^2}$	$\frac{\sqrt{2}}{2V_o}\sqrt{3P_{in}^2-2P_o^2}$

Table 6.2: Brief description of the component current stresses for the interleaved boost,and BLIL PFC topology

Topology	Interleaved PFC	BLIL PFC
Inductor RMS current	$\frac{5}{4\sqrt{3}}\frac{P_{in}}{V_{PK}}$	$\frac{5}{4\sqrt{3}}\frac{P_{in}}{V_{PK}}$
Input Bridge Diode Average Current	$\frac{2}{\pi}\frac{P_{in}}{V_{PK}}$	NA
Fast Diode Average Current	$\frac{1}{2}\frac{P_{in}}{V_o}$	$\frac{1}{2}\frac{P_{in}}{V_o}$
MOSFET RMS Current	$\frac{P_{in}}{2\sqrt{6}V_0V_{PK}}\sqrt{\left(\frac{3\pi(4V_0^2+3V_{PK}^2)-64V_{PK}V_0}{\pi}\right)}$	$\frac{P_{in}}{2\sqrt{6}V_0V_{PK}}\sqrt{\left(\frac{3\pi(4V_0^2+3V_{PK}^2)-64V_{PK}V_0}{\pi}\right)}$
MOSFET Intrinsic Body Diode Average Current	NA	$\frac{1}{2}\frac{P_{in}}{V_o}$
Output Capacitor RMS Ripple Current (Low Frequency)	$\frac{\sqrt{2}}{2}\frac{P_o}{V_o}$	$\frac{\sqrt{2}}{2}\frac{P_o}{V_o}$
Output Capacitor RMS Ripple Current (High Frequency)	$\frac{P_{in}}{V_o}\sqrt{\frac{V_o}{V_{PK}}\frac{16}{6\pi}-\frac{P_o^2}{P_{in}^2}}$	$\frac{P_{in}}{V_o}\sqrt{\frac{V_o}{V_{PK}}\frac{4}{3\pi}-\frac{P_o^2}{P_{in}^2}}$

Chapter 7

CALCULATION

Component current stresses are evaluated for Bridgeless interleaved PFC topology

7.1 Inductor RMS current

from equation 6.7,we have

$$I_{L-rms}(\theta) = \sqrt{\left(\frac{1}{\sqrt{2}}\frac{I_{PK}}{2}\right)^2 + \left(\frac{1}{2\sqrt{3}}\Delta I_{RP}\right)^2} \tag{7.1}$$

substituting peak current from equation 6.6,we have

$$= \sqrt{\left(\frac{1}{\sqrt{2}}\frac{I_{PK}}{2}\right)^2 + \left(\frac{1}{2\sqrt{3}}\left(\frac{1}{2}\frac{I_{PK}}{2}\right)\right)^2} \tag{7.2}$$

$$= I_{PK}\sqrt{\frac{1}{8} + \frac{1}{12}\frac{1}{16}} = I_{PK}\sqrt{\frac{25}{12\times 16}} = I_{PK}\frac{5}{8\sqrt{3}} \tag{7.3}$$

$$= \frac{5}{4\sqrt{3}}\frac{P_{in}}{V_{PK}} \quad \because I_{PK} = \frac{2P_{in}}{V_{PK}} \tag{7.4}$$

7.2 Input Bridge Diode Average Current

As there is no Input bridge rectifier in BLIL PFC converter .So calculation of Input Bridge Diode Average Current is not applicable .

7.3 Fast Diode Average Current

from equation 6.10,we have

$$I_{D-\sigma ve} = \frac{1}{\pi}\int_0^{\pi} \frac{I_{PK}}{2}|\sin(\theta)\left(\frac{V_{PK}|\sin(\theta)|}{V_o}\right)d\theta \tag{7.5}$$

$$= \frac{V_{PK}}{V_O}\frac{I_{PK}}{2\pi}\int_0^{\pi}|\sin(\theta)|^2 d\theta \tag{7.6}$$

$$= \frac{V_{PK}I_{PK}}{2V_O}\frac{2}{\pi}\int_0^{\frac{\pi}{2}}|\sin(\theta)|^2 d\theta \quad \because \int_0^{\pi} f(\theta)d\theta = \int_0^{\pi} f(\pi-\theta)d\theta = 2\int_0^{\frac{\pi}{2}} f(\theta)d\theta \tag{7.7}$$

$$= \frac{V_{PK}I_{PK}}{2V_O}\frac{2}{\pi}\left(\frac{1}{2}\frac{\pi}{2}\right) \quad \because \int_0^{\frac{\pi}{2}} \cos^n(\theta)d\theta = \int_0^{\frac{\pi}{2}} \sin^n(\theta)d\theta = \frac{(\mathrm{n}-1)\cdots 5\cdot 3\cdot 1}{\mathrm{n}\cdots 6\cdot 4\cdot 2}\frac{\pi}{2} \tag{7.8}$$

If n is even

$$= \frac{V_{PK}I_{PK}}{2V_O}\frac{1}{2} = \frac{P_{in}}{2V_O} \quad \because \frac{I_{PK}V_{PK}}{2} = P_{in} \tag{7.9}$$

7.4 MOSFET RMS Current

from equation 6.5,we have

$$I_{Q-rms}(\theta) = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{I_{PK}}{2}|\sin(\theta)|\left(\delta_Q(\theta)\right)\right]^2 d\theta} \tag{7.10}$$

substituting duty cycle from equation 6.1,we have

$$= \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{I_{PK}}{2}|\sin(\theta)|\left(1-\frac{V_{PK}|\sin(\theta)|}{V_o}\right)\right]^2 d\theta} \tag{7.11}$$

$$= \sqrt{\frac{2}{\pi}\int_0^{\frac{\pi}{2}}\left[\frac{I_{PK}}{2}|\sin(\theta)\|\left(1-\frac{V_{PK}|\sin(\theta)|}{V_o}\right)\right]^2 d\theta} \tag{7.12}$$

$\because \int_0^{\pi} \mathrm{f}(\theta)d\theta = \int_0^{\pi} \mathrm{f}(\pi-\theta)d\theta = 2\int_0^{\frac{\pi}{2}} \mathrm{f}(\theta)d\theta$

$$= \frac{I_{PK}}{2}\sqrt{\frac{2}{\pi}\int_0^{\frac{\pi}{2}} \sin\left(\theta\right)|^2 \left(1 - \frac{V_{PK}|\sin(\theta)|}{V_o}\right)^2 d\theta} \tag{7.13}$$

$$= \frac{I_{PK}}{2}\sqrt{\frac{2}{\pi}\int_0^{\frac{\pi}{2}} |\sin(\theta)|^2 \left(1 + \left(\frac{V_{PK}}{V_o}\right)^2 |\sin(\theta)|^2 - 2\frac{V_{PK}}{V_O}|\sin(\theta)|\right) d\theta} \tag{7.14}$$

$$= \frac{I_{PK}}{2}\sqrt{\frac{2}{\pi}\left(\int_0^{\frac{\pi}{2}} |\sin(\theta)|^2 d\theta + \left(\frac{V_{PK}}{V_O}\right)^2 \int_0^{\frac{\pi}{2}} |\sin(\theta)|^4 d\theta - 2\frac{V_{PK}}{V_O}\int_0^{\frac{\pi}{2}} |\sin(\theta)|^3 d\theta\right)} \tag{7.15}$$

$$= \frac{I_{PK}}{2}\sqrt{\frac{2}{\pi}\left(\frac{1}{2}\frac{\pi}{2} + \left(\frac{V_{PK}}{V_O}\right)^2 \frac{3\cdot 1}{4\cdot 2}\frac{\pi}{2} - 2\frac{V_{PK}}{V_O}\frac{2}{3\cdot 1}\right)} \tag{7.16}$$

$\because \int_0^{\frac{\pi}{2}} \cos^n(\theta)d\theta = \int_0^{\frac{\pi}{2}} \sin^n(\theta)d\theta$

$= \frac{(\mathrm{n}-1)\cdots 5\cdot 3\cdot 1}{\mathrm{n}\cdots 6\cdot 4\cdot 2}\frac{\pi}{2}$ If n is even

$= \frac{(\mathrm{n}-1)\cdots 6\cdot 4\cdot 2}{\mathrm{n}\cdots\cdot 5\cdot 3\cdot 1}$ If n is odd

$$= \frac{I_{PK}}{2}\sqrt{\left(\frac{1}{2} + \left(\frac{V_{PK}}{V_O}\right)^2 \frac{3}{8} - \frac{V_{PK}}{V_O}\frac{8}{3\pi}\right)} \tag{7.17}$$

$$= \frac{I_{PK}}{2}\sqrt{\left(\frac{3\pi\left(4V_o^2 + 3V_{PK}^2\right) - 64V_{PK}V_O}{24\pi V_o^2}\right)} \tag{7.18}$$

$$= \frac{I_{PK}}{4\sqrt{6}V_o}\sqrt{\left(\frac{3\pi\left(4V_o^2 + 3V_{PK}^2\right) - 64V_{PK}V_O}{\pi}\right)} \tag{7.19}$$

$$= \frac{P_{in}}{2\sqrt{6}V_oV_{PK}}\sqrt{\left(\frac{3\pi\left(4V_o^2 + 3V_{PK}^2\right) - 64V_{PK}V_O}{\pi}\right)} \tag{7.20}$$

$\because \frac{I_{PK}V_{PK}}{2} = P_{in} \Rightarrow I_{PK} = \frac{2P_{in}}{V_{PK}}$

for BLIL PFC converter

7.5 MOSFET Intrinsic Body Diode Average Current

from equation 6.10,we have

$$I_{D\text{ int-ave}} = \frac{1}{\pi}\int_0^{\pi}\frac{I_{PK}}{2}|\sin(\theta)|\left(\frac{V_{PK}|\sin(\theta)|}{V_o}\right)d\theta \tag{7.21}$$

$$= \frac{V_{PK}}{V_O}\frac{I_{PK}}{2\pi}\int_0^{\pi}|\sin(\theta)|^2 d\theta \tag{7.22}$$

$$= \frac{V_{PK}I_{PK}}{2V_O}\frac{2}{\pi}\int_0^{\frac{\pi}{2}}|\sin(\theta)|^2 d\theta \tag{7.23}$$

$$\because \int_0^{\pi}\mathrm{f}(\theta)d\theta = \int_0^{\pi}\mathrm{f}(\pi-\theta)d\theta = 2\int_0^{\frac{\pi}{2}}\mathrm{f}(\theta)d\theta$$

$$= \frac{V_{PK}I_{PK}}{2V_O}\frac{2}{\pi}\left(\frac{1}{2}\frac{\pi}{2}\right) \tag{7.24}$$

$$\because \int_0^{\frac{\pi}{2}}\cos^n(\theta)d\theta = \int_0^{\frac{\pi}{2}}\sin^n(\theta)d\theta$$

$$= \frac{(\mathrm{n}-1)\cdots 5\cdot 3\cdot 1}{\mathrm{n}\cdots 6\cdot 4\cdot 2}\frac{\pi}{2} \quad \text{If n is even}$$

$$= \frac{V_{PK}I_{PK}}{2V_O}\frac{1}{2} = \frac{P_{in}}{2V_O} \quad \because \frac{I_{PK}V_{PK}}{2} = P_m \tag{7.25}$$

,

7.6 Output Capacitor RMS Ripple Current (Low Frequency)

$$\Delta I_{\text{cap-ripple}} = I_{\text{output-ac}} = \sqrt{(I_{\text{output}-rms})^2 - (I_o)^2} \tag{7.26}$$

At low frequency,

$$\Delta I_{\text{cap-ripple}} = \frac{I_o}{\sqrt{2}} = \frac{\sqrt{2}}{2}\frac{P_o}{V_o} \tag{7.27}$$

7.7 Output Capacitor RMS Ripple Current (High Frequency)

$$\Delta I_{\text{cap-ripple}} = I_{\text{outrput}-ac} = \sqrt{(I_{\text{output}-rms})^2 - (I_o)^2} \tag{7.28}$$

At high frequency,

$$I_{\text{outtput}-rms} = I_{D-rms}(\theta) = i_L(\theta)\sqrt{\delta_D(\theta)} \tag{7.29}$$

$$I_{\text{outtput}ms}(\theta) = \sqrt{\frac{1}{\pi}\int_0^{\pi} \left[I_{\text{output-rms}}\right]^2 d\theta} \tag{7.30}$$

$$= \sqrt{\frac{1}{\pi}\int_0^{\pi} \left[i_L(\theta)\sqrt{\delta_D(\theta)}\right]^2 d\theta} \tag{7.31}$$

$$\because I_{\text{output}-ms} = I_{D-rms}(\theta) = i_L(\theta)\sqrt{\delta_D(\theta)}$$

$$= \sqrt{\frac{1}{\pi}\int_0^{\pi} I_{PK}^2 |\sin(\theta)|^2 \frac{V_{PK}|\sin(\theta)|}{V_O} d\theta} \tag{7.32}$$

Substituting equation 6.2,6.8

$$= I_{PK}\sqrt{\frac{V_{PK}}{V_o}}\sqrt{\frac{1}{\pi}\int_0^{\pi} |\sin(\theta)|^3 d\theta} \tag{7.33}$$

$$= I_{PK}\sqrt{\frac{V_{PK}}{V_o}}\sqrt{\frac{2}{\pi}\int_0^{\frac{\pi}{2}} |\sin(\theta)|^3 d\theta} \tag{7.34}$$

$$\because \int_0^{\pi} \mathrm{f}(\theta)d\theta = \int_0^{\pi} \mathrm{f}(\pi-\theta)d\theta = 2\int_0^{\frac{\pi}{2}} \mathrm{f}(\theta)d\theta$$

$$= I_{PK}\sqrt{\frac{V_{PK}}{V_o}}\sqrt{\frac{2}{\pi}\frac{2}{3\cdot 1}} \tag{7.35}$$

$$\because \int_0^{\frac{\pi}{2}} \cos^n(\theta)d\theta = \int_0^{\frac{\pi}{2}} \sin^n(\theta)d\theta$$

$$= \tfrac{(\mathrm{n}-1)\cdots 6\cdot 4\cdot 2}{\mathrm{n}\cdots 5\cdot 3\cdot 1} \text{ If n is odd}$$

$$= \frac{P_{in}}{V_{PK}}\sqrt{\frac{V_{PK}}{V_o}}\sqrt{\frac{4}{3\pi}} \tag{7.36}$$

$$\because 2\left(\tfrac{I_{PK}V_{PK}}{2}\right) = P_{in} \Rightarrow I_{PK} = \tfrac{P_{in}}{V_{PK}} \text{ Now,}$$

$$\Delta_{\text{ cap-ripple}} = I_{\text{output-ac}} = \sqrt{\left(I_{\text{output}-rms}\right)^2 - \left(I_o\right)^2} \tag{7.37}$$

$$= \sqrt{\left(\frac{P_{in}}{V_{PK}}\sqrt{\frac{V_{PK}}{V_o}}\sqrt{\frac{4}{3\pi}}\right)^2 - \left(I_o\right)^2} \tag{7.38}$$

$$= \sqrt{\left(\frac{P_{in}}{V_{PK}}\sqrt{\frac{V_{PK}}{V_o}}\sqrt{\frac{4}{3\pi}}\right)^2 - \left(\frac{P_o}{V_o}\right)^2} \quad \because I_o = \frac{P_o}{V_o} \tag{7.39}$$

$$= \frac{P_{in}}{V_o}\sqrt{\frac{V_o}{V_{PK}}\frac{4}{3\pi} - \frac{P_o^2}{P_{in}^2}} \tag{7.40}$$

Chapter 8

EXPERIMENTAL RESULTS

8.1 Simulation Result

Simulation of the prototype model has been done to verify the operation of the topology taken.Diagram of the prototype is given in figure. simulation results waveform of are shown in figure

Table 8.1: Value of Parameters taken for Simulation

PARAMETERS	BLIL PFC
Input voltage	325V peak
supply frequency	50Hz
Output voltage	400V
Load	160 ohm
Switching frequency	10KHz
Inductance	$90\mu H$
capacitance	$220\mu F$

from the input voltage and current waveform shown in figure8.6,8.5 we can see that both are in phase and their shape is nearly sinusoidal. Component information is provided in Table 8.1 for the semiconductors and powering components of the proposed BLIL PFC converter.

. The converter power factor is calculated from in Fig.8.5 and8.6 for the load of 400V and 160 ohm.with this topology . The converter power factor is calculated from in Fig. 8-3 and 8-4 for the load of 400V and 160 ohm.

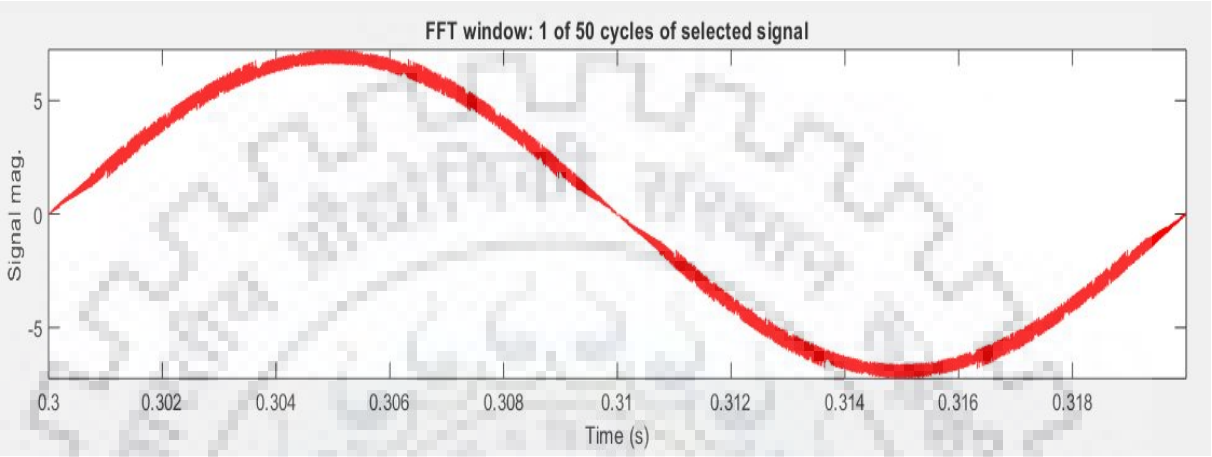


Figure 8.1: Input current signal

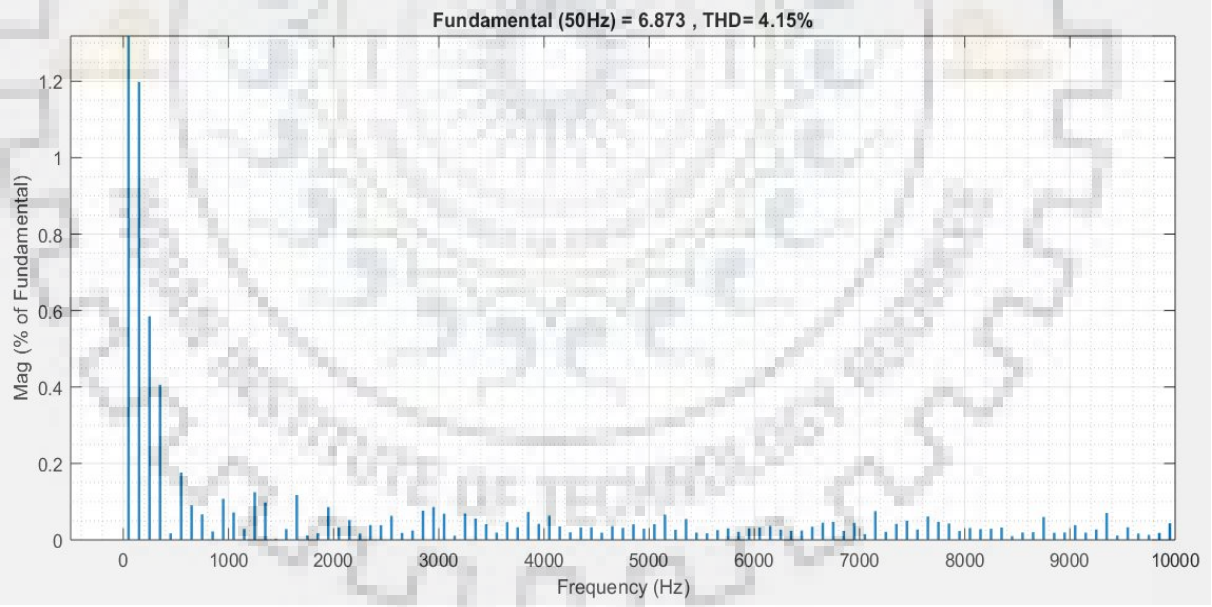


Figure 8.2: Total Harmonic Distortion

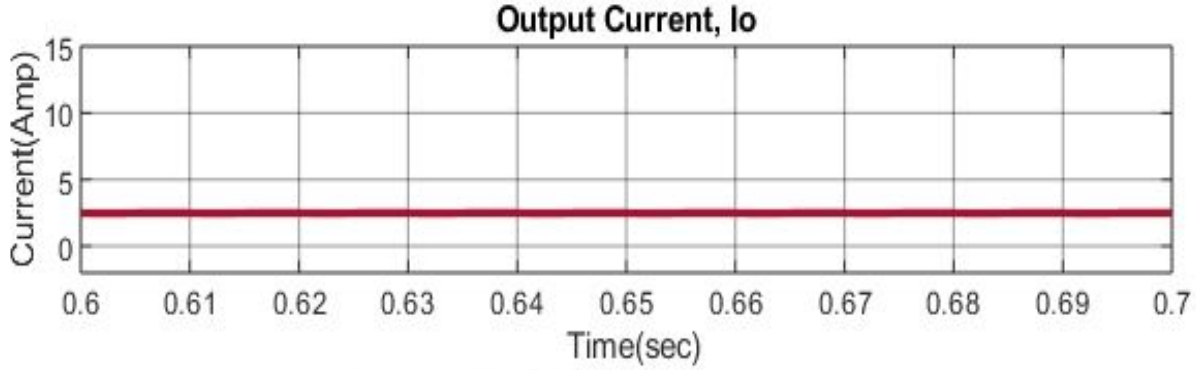


Figure 8.3: Output current

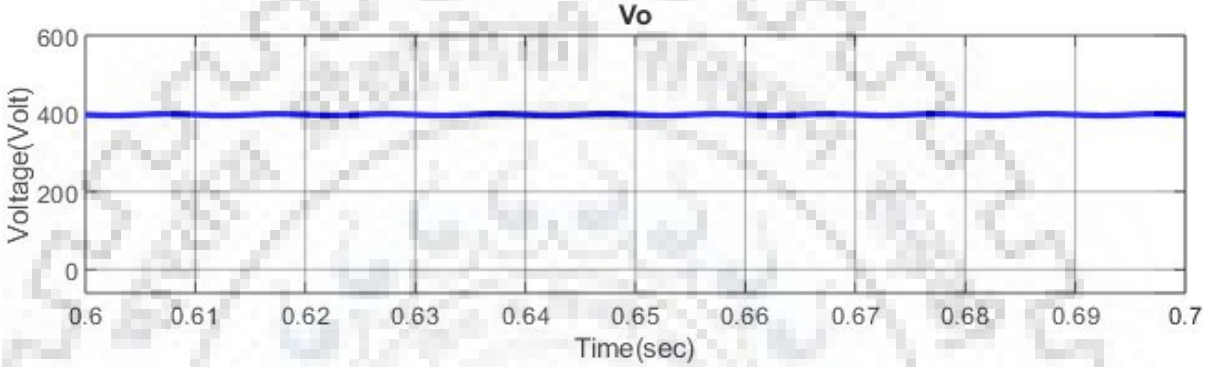


Figure 8.4: Output Voltage

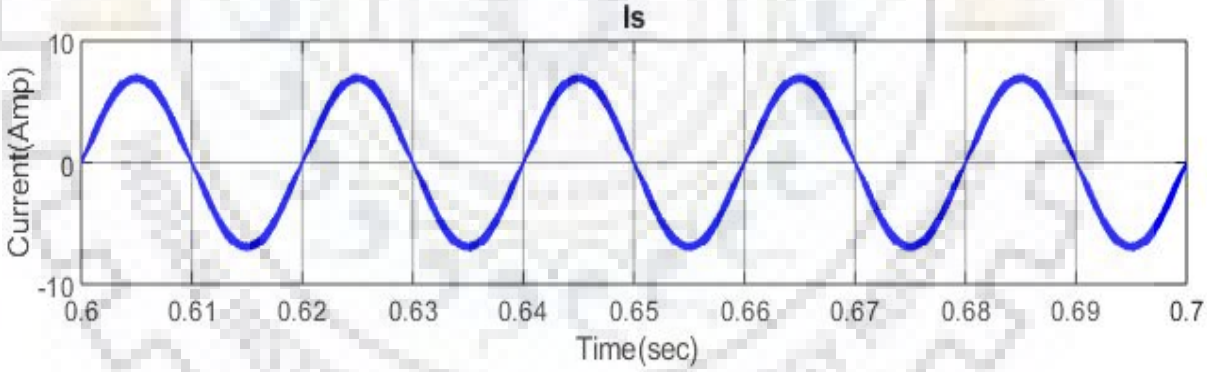


Figure 8.5: Input current

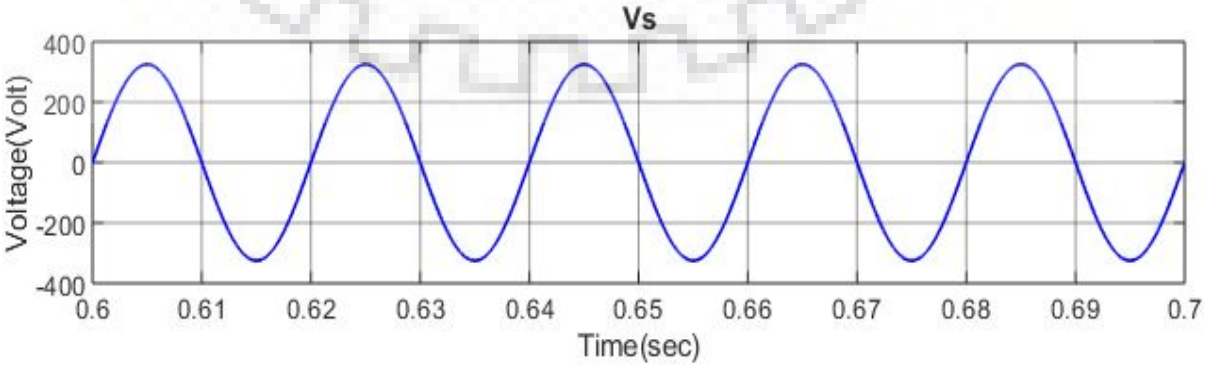


Figure 8.6: Input Voltage

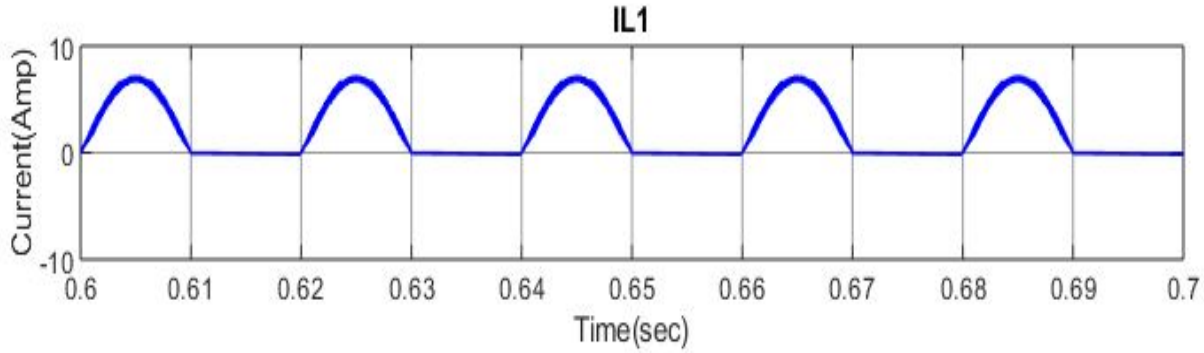


Figure 8.7: Inductor current of L1

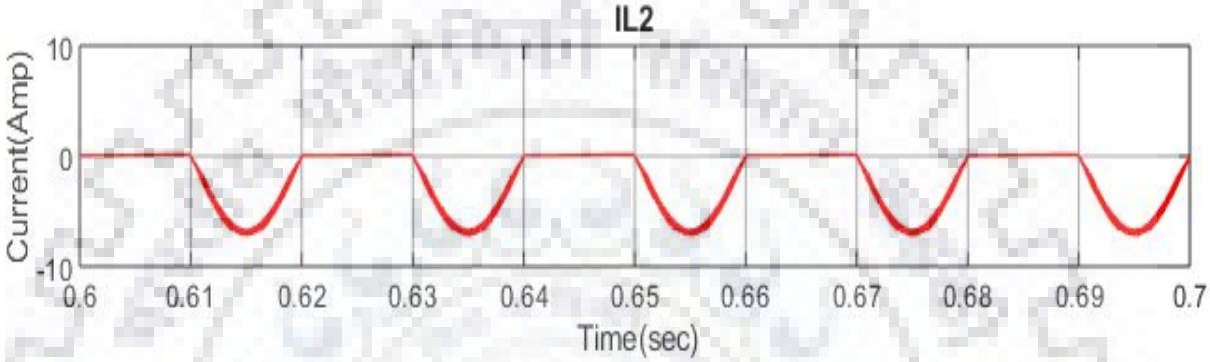


Figure 8.8: Inductor current of L2

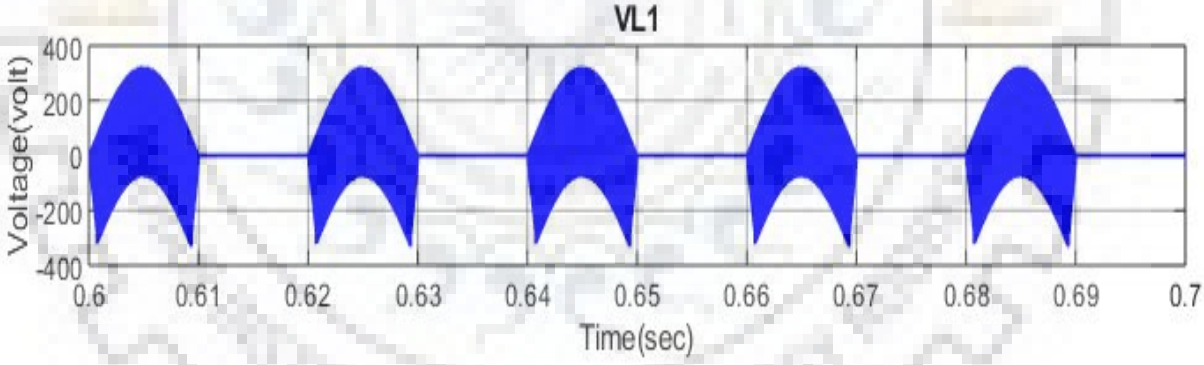


Figure 8.9: Inductor voltage of L1

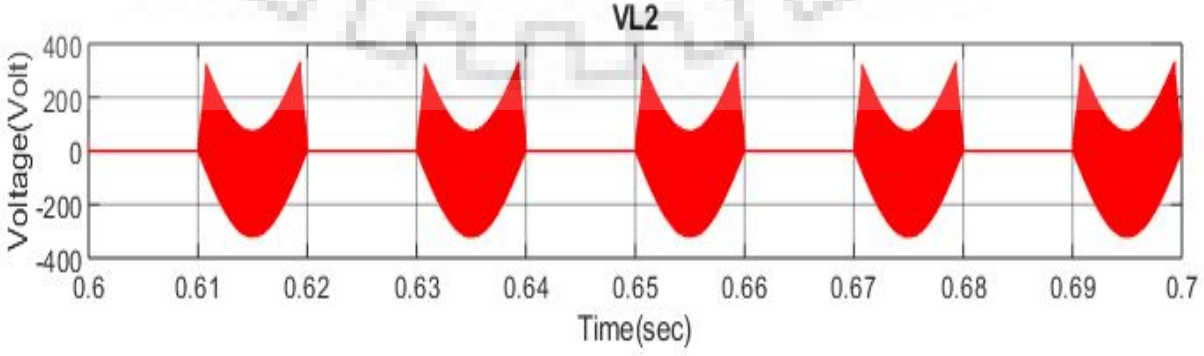


Figure 8.10: Inductor voltage of L2

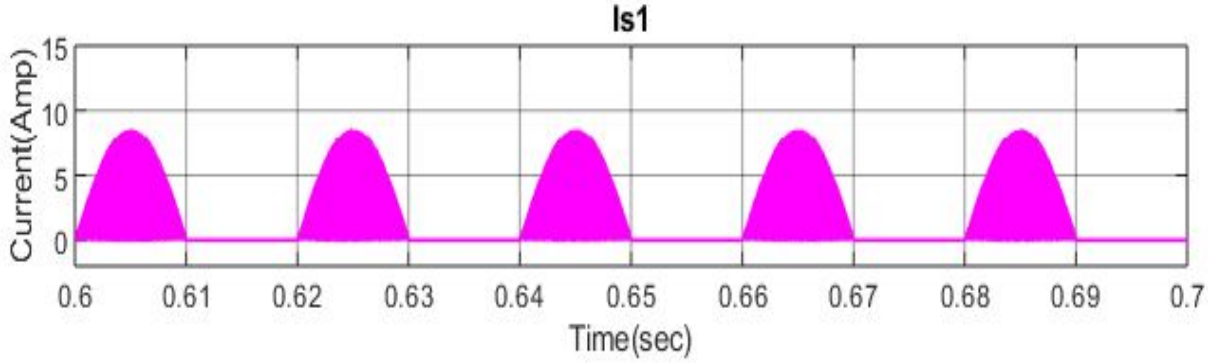


Figure 8.11: MOSFET-1 current

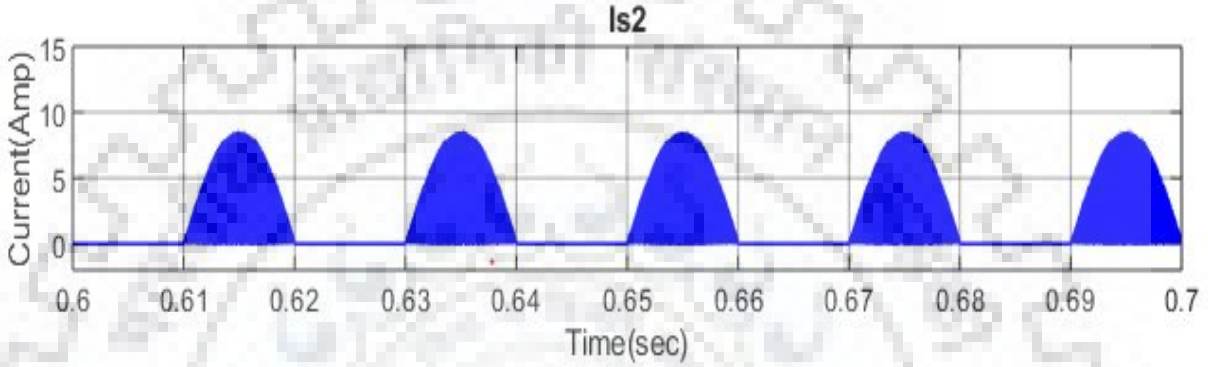


Figure 8.12: MOSFET-2 current

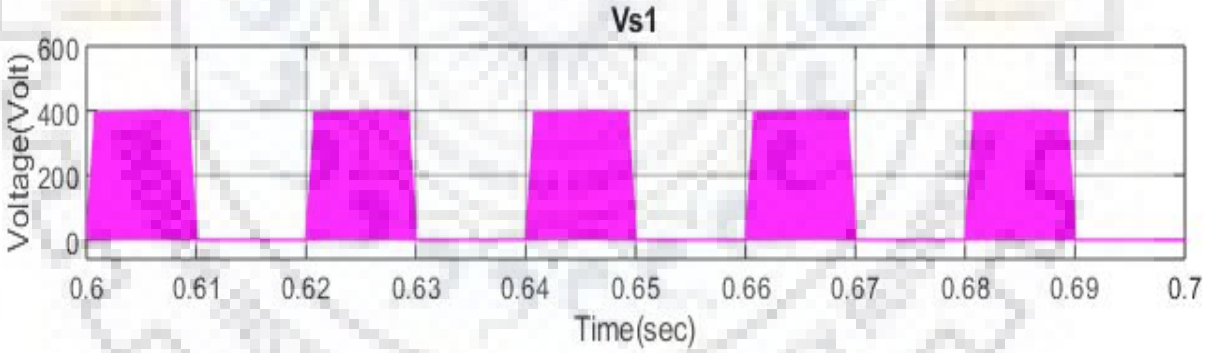


Figure 8.13: MOSFET-1 voltage

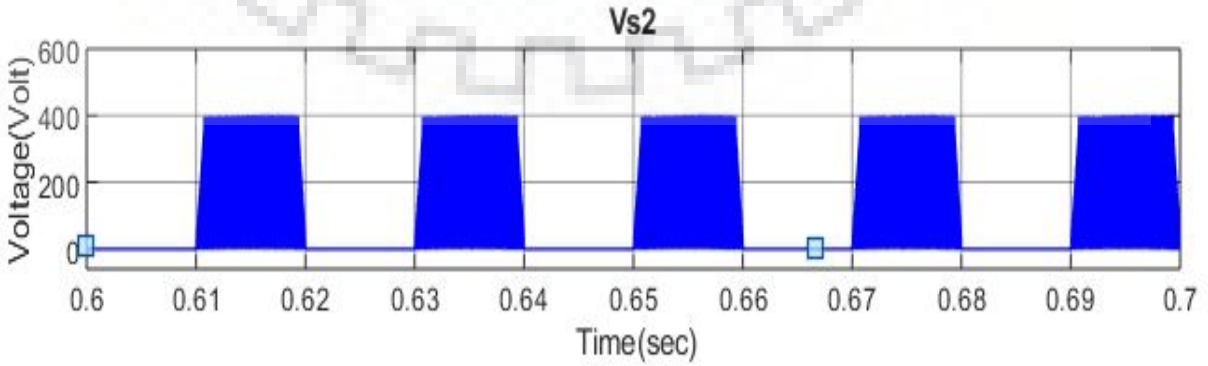


Figure 8.14: MOSFET-2 voltage

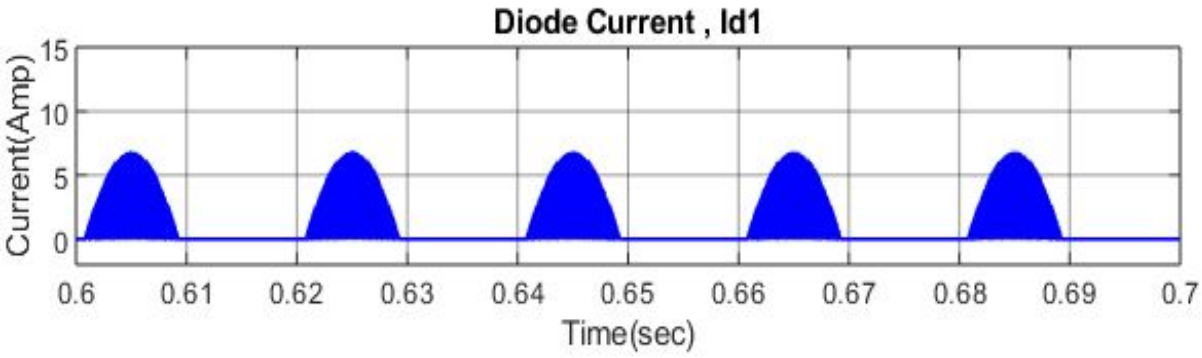


Figure 8.15: Diode-1 current

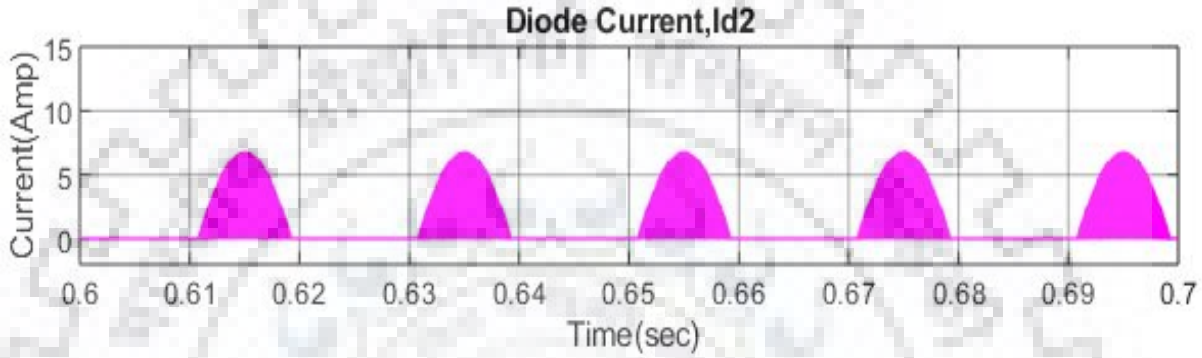


Figure 8.16: Diode-2 current

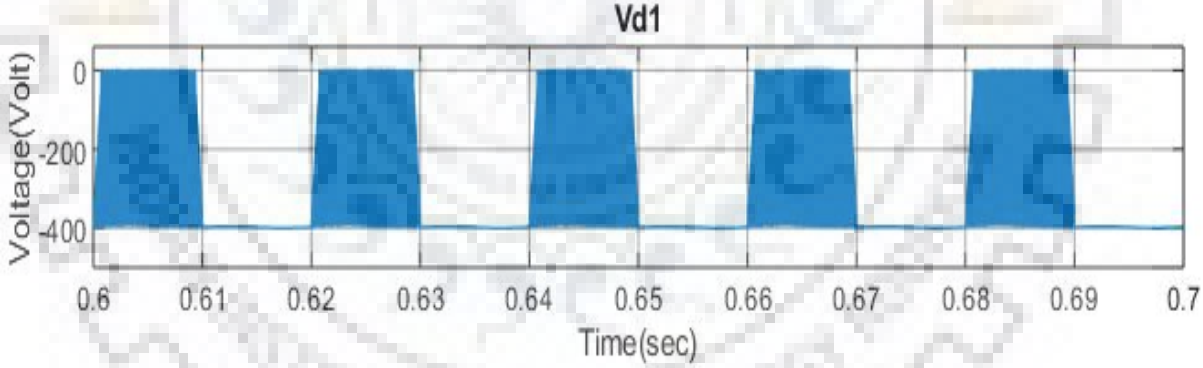


Figure 8.17: Diode-1 voltage

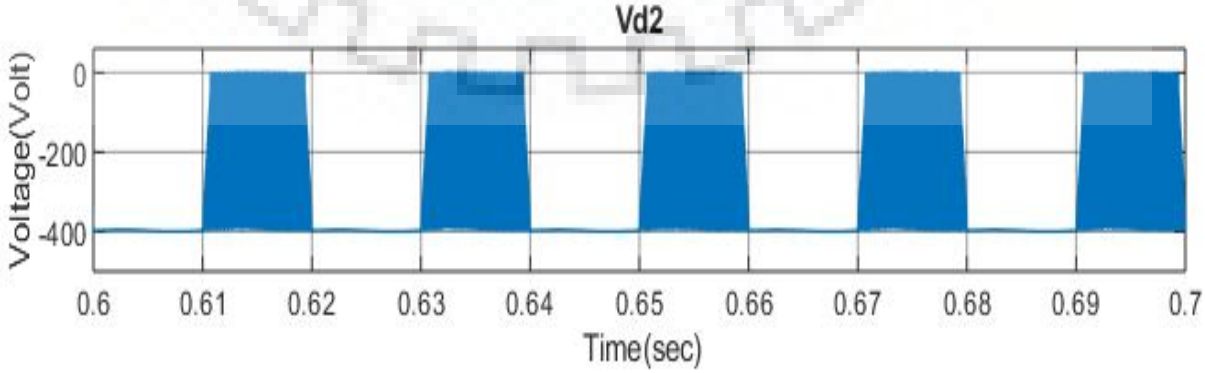


Figure 8.18: Diode-2 voltage

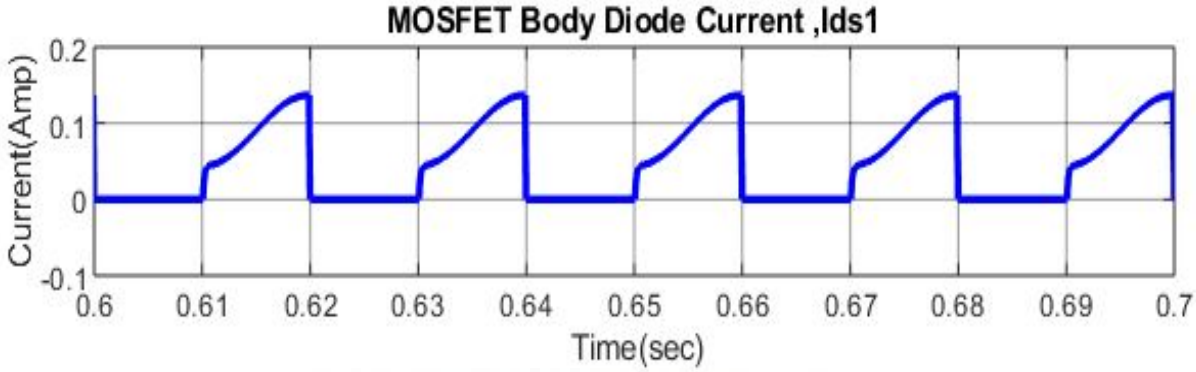


Figure 8.19: MOSFET-1 Body Diode current

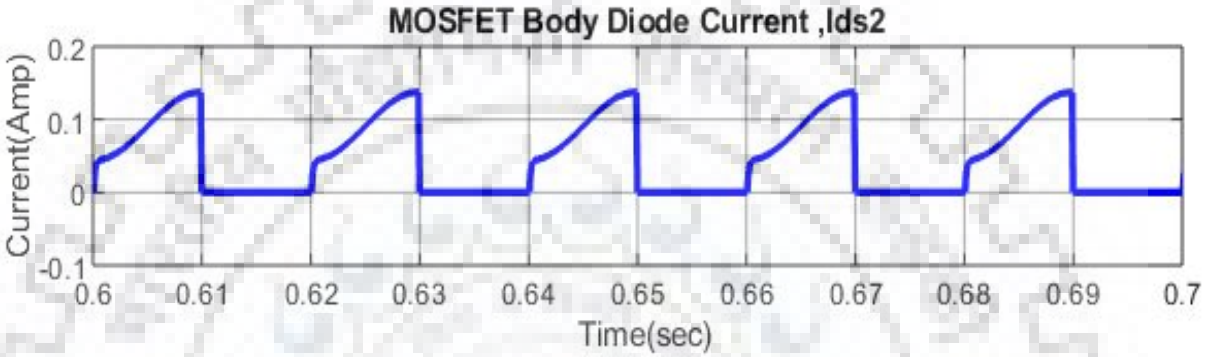


Figure 8.20: MOSFET-2 Body Diode current

Chapter 9

conclusion

A Bridgeless Interleaved topology discussed in this dissertation ,which deploy as the front part of AC-DC converter in plug-in hybrid Electric vehicle battery charger.which is studied and its characteristics presented.

Experiment results shows the efficiency ,graphs and input current harmonics. Harmonic data of input current is compared with the EN 61000-3-2 standard limits,which should be less than 5% from half load to full load and converter is follow with the EN 61000-3-2 standard .The proposed converter achieved a peak efficiency of 98.9 % at 10 kHz switching frequency, 230 V input and 1kW output power.

As the studied topology shows high power factor over wide range of load and less input current harmonics,it has the caliber for the PFC in high power level II battery charging application.

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