DESIGN AND VERIFICATION OF THREE PHASE SEQUENCE DETECTOR

A DISSERTATION

Submitted in fulfillement of the
requirements for the award of the degree
of
MASTER OF TECHNOLOGY
in
ELECTRICAL ENGINEERING
(With the specialization in System and Control Engineering)

Submitted by

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MAY-2019

CANDIDATE'S DECLARATION

I hereby declare that the work which is being presented in this report entitled **"DESIGN AND VERIFICATION OF THREE PHASE SEQUENCE DETECTOR"** submitted in the fulfillment of the requirement for award of the Degree of **Master of Technology** in **Electrical Engineering** with specialization in **System and Control,** from Indian Institute of Technology, Roorkee under the supervision of **Dr. Vishal Kumar**, Professor of Department of Electrical Engineering, Indian Institute of Technology, Roorkee. The matter presented in the dissertation has not been submitted by me for the award of any other degree of this institute or any other institute.

Date :

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CERTIFICATE

This to certify that the above statement made by the candidate is correct to best of my knowledge and belief.

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ACKNOWLEDGEMENT

It is my great pleasure to express my most sincere gratitude and thankfulness to **Dr. Vishal Kumar**, Professor of the Department of Electrical Engineering, Indian Institute of Technology, Roorkee for his dedicated guidance, generous help and the precious time he gave in supervising this dissertaion Report.

I would also sincerely thank all of my fellow friends and the staff of Department of Electrical Engineering Department IIT Roorkee, who have helped me in every possible way in the successful completion of my dissertaion report.

I also take this occasion to thank my family for their help and encouragement in preparing this dissertaion report.

PRABHAT SHRIVASTAVA

ABSTRACT

The work proposes a three-phase sequence detector which will be capable of extracting the three phase sequences of a balanced or unbalanced power system which can be the result of any faults in the phases and or ground, unbalanced loading and open phases. The extraced sequences are the positive, negative and zero sequences components. Digital simulation is used here to process the three-phase input signal which can be balanced or unbalanced. To process the three-phase signal, the conventional symmetrical component transform method in implemented here. Finally, a Field Programmable Gate Array (FPGA) implementation is used here to verify the theoritical results.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

1.1 Overview

An abnormal system can be viewed as there are negative or zero sequence components of currents or voltages in the system. These symmetrical components can be used to determine the operating conditions of the power system and also in the detection and localization of faults. Because of this functionality, filters having the capability to extract out the symmetrical components from the three phase signals are getting popular in applications such as in protecting relays and in control as well as measuring devices.

For the analog control systems and RL or RC circuits based filters are used, whereas, for digital systems, symmetrical component technique is more appropriate to process discrete signals. Following are the fundamental requirements for the digital filters of symmetrical components:

- ✓ Accuracy for large range of input signals . If the signal is distorted because of components of other than fundamental frequency, only a slight change in accuracy is allowed.
- ✓ In the event of change of inputs, output should be produced with short delay.
- ✓ Digital efficiency is required. In other words, algorithm should be less complex in order to reduce the computational complexity [1].

For the fault detection and the analysis of the power system operation, the three phase signals are decomposed into the positive, negative and the zero sequence components. The extracted positive sequence component, which is an essential piece of information, is used for controlling and operating the grid connected devices that may be active power filters or the power systems that are employed in the industries while the extracted negative and zero sequence components are used for the protection control or for the determination of appeared fault type and fault location in the power system. These sequence components are the fundamental tools used in power systems and industrial applications to allow appropriate examination and analysis of the three phase power network under both balanced and unbalanced operating conditions.

The unbalances usually are those prompted by the faults between phases or ground , open phases and unbalanced loading. These symmetrical components provide notable insight into the behavior of the three phase power networks and are widely used in fault analysis of the power system and relay protection.

In a three phase power system, out of the three sets of phasors, one set has same sequence of phases as the system under the study, which is positive sequence (say ABC), second set of phasors has reverse sequence of phases, which is negative sequence (say ACB) and the third set in which all the three phasors are in phase with each other, which is the zero sequence. Figure 1 below depicts the block diagram of the objective of this project [2].

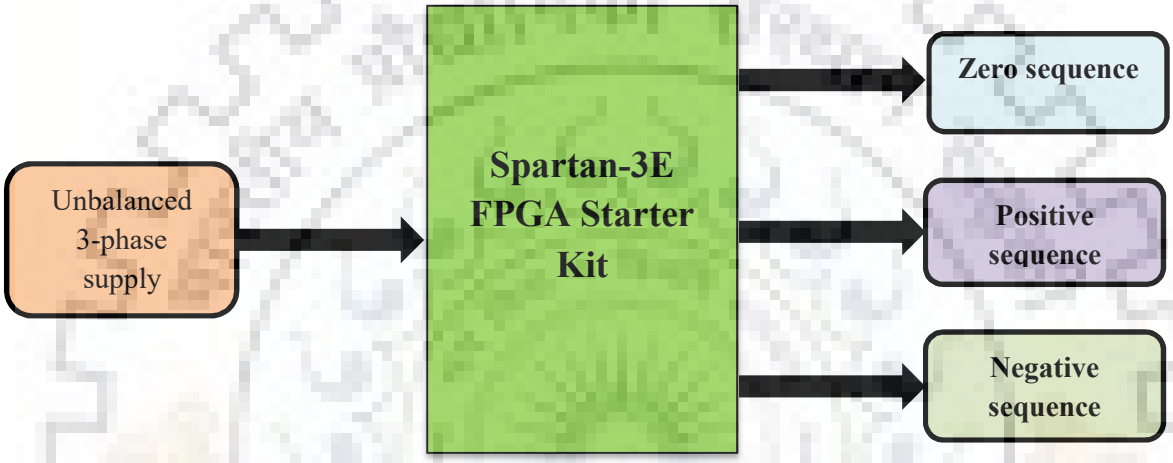


Figure 1: Block diagram of sequence detector

1.2 Why Sequence components

A symmetrical power system is a system with three identical phases. Phasor quantities like voltage and current of different sequences in this power system do not react to each other. Voltage drop in one sequence will be induced by the current in that respective sequence only.

Current in any sequence flows in an associated independent network only, since there in no interaction between quantities of different sequences in a symmetrical power system. We can say that for the positive , negative and the zero sequences, we will get different sequences networks. As an example, positive sequence network have positive sequence current only. Sequence network for a particular sequence network is a single phase equivalent circuit with associated impedances in it.

Therefore, in case of unbalanced fault, system performance and interconnection between voltage and current quantities of different sequences can be analyzed by interconnecting the positive , negative and zero sequence networks at the fault location.

The main advantage of using the method of Sequence components is isolating voltage and current quantities into positive, negative and zero components that help in better criteria for controlling factors for various applications:

- ✓ In Stability analysis, synchronizing force between machines is affected by the Positive sequence components
- ✓ The heating effect due to unbalanced currents depends upon the negative sequence component. Heating effect is observed due to unbalanced currents, which depicts the presence of negative sequence component current flowing in the system. The heating effect and the negative sequence component can be reduced by reducing unbalanced currents.
- ✓ Zero sequence current flows through the system in case of Earth faults. Thus, all earth or ground relay operates on determining the zero sequential components [3].

1.3 Symmetrical and Unsymmetrical faults

Normally, our power system operates under balanced condition. A short-circuit or fault occurs in a line when our system becomes unbalanced due to failure in insulations or contact of live-wires.

There are number of reasons that attributes to fault in the power system such as natural disturbances like lightening, high-speed winds or earthquakes, insulation breakdown, tree falling, bird shorting, etc.

There are two types of faults that occur in our transmission lines:

- ✓ Symmetrical faults
- ✓ Unsymmetrical faults

1.3.1 Symmetrical faults

Symmetrical faults are said to have occurred when all the three phases get short-circuited to each other or to earth as shown in Figure 2. Such faults are said to be balanced since the system remains symmetrical, in other words, we can say that the three phase lines are displaced by an angle of 120° to each other. This type of fault occurs rarely, but it is the most severe fault as it involves largest current. Balanced short circuit calculations are performed for determining these large currents.

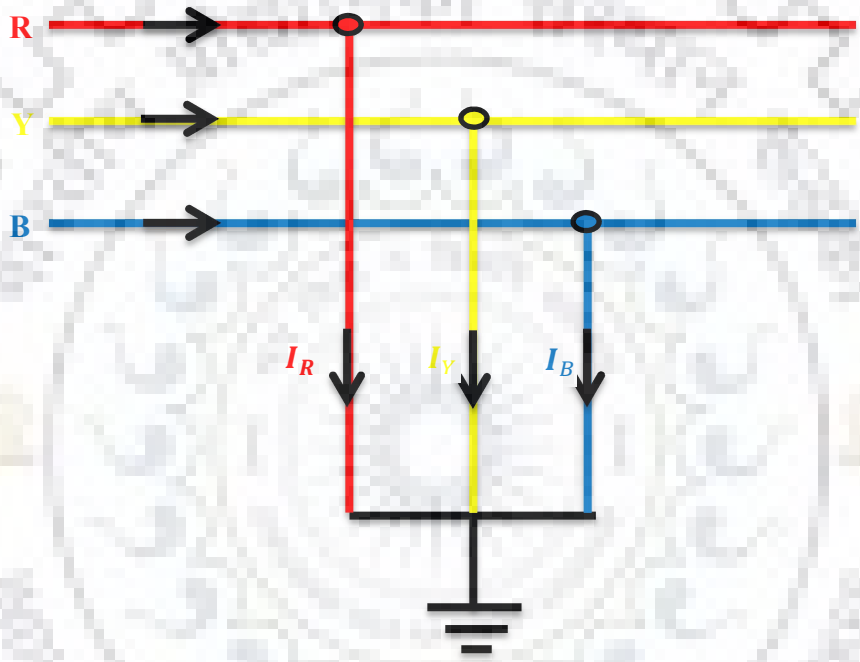


Figure 2: Symmetrical Fault

1.3.2 Unsymmetrical fault

Only one or two phases" are involved in the unsymmetrical faults. In this case, the three-phase lines become unbalanced . These types of faults occur between the lines or between line-to-ground. The unsymmetrical series faults occur between phases or between phase-to-ground , while the unsymmetrical shunt fault is unbalance in the line impedances. The three-phase shunt faults are given below:

- ✓ **Single line-to-ground fault (L.G.):** here a conductor comes in contact with the ground or the neutral conductor.
- ✓ **Line-to-line fault (LL):** this occurs when two conductors are short-circuited
- ✓ **Double line-to-ground fault (L.L.G.):** this occurs when the two conductors fall on the ground or come in contact with the neutral conductor
- ✓ **Three-phase short-circuit fault (L.L.L.)**
- ✓ **Three-phase-to-ground fault (L.L.L.G.)**

LG, LL and LLG faults are unsymmetrical faults shown in Figure 3, whereas LLL and LLLG faults are symmetrical faults.

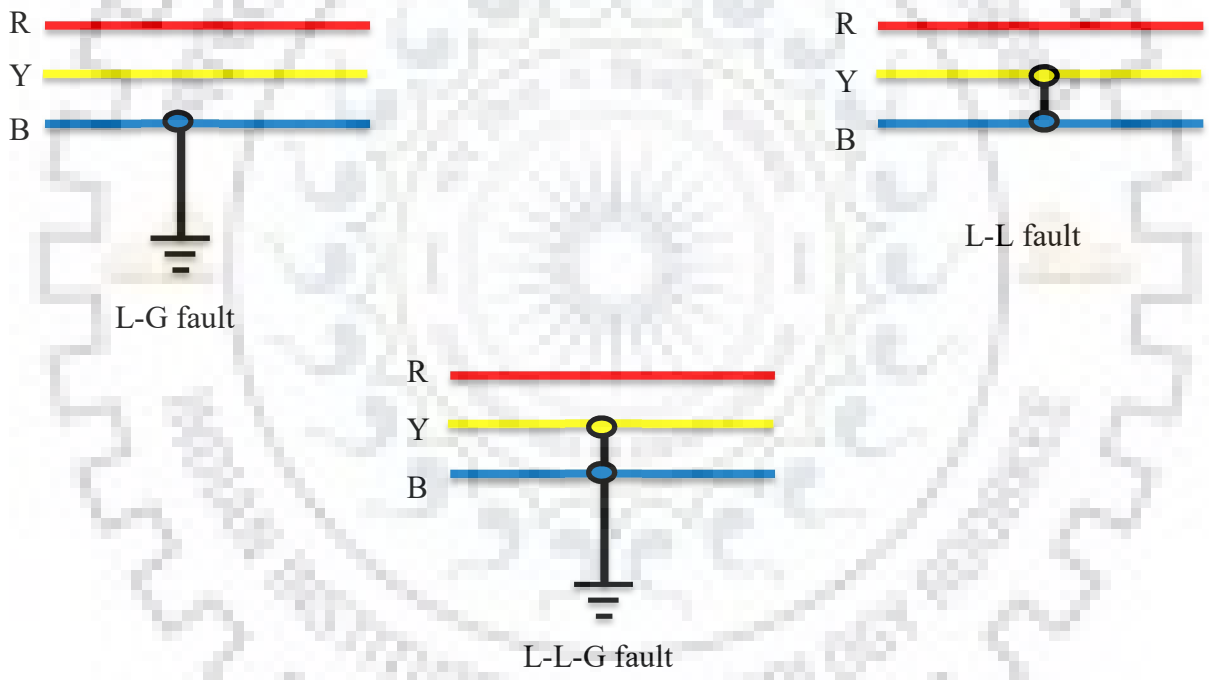


Figure 3: Unsymmetrical faults

1.3.3 Effects of faults on Transmission line

Power system can be damaged and disrupted in several ways because of the faults. Faults result in the increase of the voltages and the currents at certain points on the system. Because of the large

voltages and currents, insulation got damaged and the equipment life reduces. These faults can cause instability in the system, thereby the three-phase system operates improperly.

Therefore, it is necessary to disconnect the fault system, on the occurrence of the fault. Thereby, the rest of the system will not be affected in case of faults [4].

2. SOFTWARE AND HARDWARE DESCRIPTION

Within high integrity and safety critical systems, FPGAs are experiencing their increased popularity. Field Programmable Gate Arrays have hundreds of thousands of programmable logic cells. These logic cells are configurable for a wide range tasks. They also offer many benefits over traditional microprocessors, like very predictable performance and also efficient parallel processing.

Advantages of FPGAs over conventional hardware-implementations:

- ✓ Simpler assembly
- ✓ Lesser component count
- ✓ Lower real-estate requirements

2.1 Coding language used

VHSIC (Very High Speed Integrated Circuit) Hardware Description Language (VHDL) is one commonly used coding language for configuring these FPGAs. VHDL is used for Hardware description. In spite of a hardware description language, it is developed in similarity to traditional software language.

This language was developed for documentation of the behavior of electronic circuits. US Department of Defense was the one who initiated the development of VHDL. They found out that the hardware documentation was not adequate and that it was difficult to reproduce or replace the components. Since then the language is being used as a design tool, with synthesis and simulation tools being developed.

VHDL supports parallel processing as compared to typical software programming languages which makes it a simple, strongly typed language with fast processing. It includes time/ clock processing and low-level circuit description in contrast to the traditional software programming languages. It supports simulation, instead of execution, to provide different simulation results to actual implementations in case VHDL is constructed poorly. Hardware description in the form of VHDL is then converted into a configuration file. This file is then uploaded to the device. [5].

2.2 Programming Technology

As we know that Field Programmable Gate Arrays (FPGAs) are programmable hardwares, it is necessary for us to program them to make them ready for use as per our requirement. VHSIC (Very High Speed Integrated Circuit) Hardware Description Language (VHDL) is used here to program the FPGA board. VHDL is similar to other software languages in terms of structure and development. Rather than execution, it offers simulation which may give different implemented results if in case they are poorly constructed [6].

We basically have two competing methods for programming the FPGAs. The first one is SRAM programming and second uses Anti-fuses. The first one involves small static random memory bits (RAM bits) for each programming element. The second one consists of very small microscopic structures that do not make connection. The connection between the two sides of anti-fuse is made by flowing a certain amount of current while programming the device. A third technology is also in the market, which uses Flash bits as programming elements.

First technology has some advantages that it is easier to improve the technology to make faster and lower power FPGAs with the help of standard fabrication process. These FPGAs can be reprogrammed a number of times, as SRAMs are reprogrammable, even while in the system operation. These devices easily use the internal SRAMs as the small memories in the design.

Comparatively, from Table 1, anti-fuse based FPGAs are faster in theory as they are non-volatile and the delays due to routing are minimal. In practice, because SRAM technology is mature and well understood the speed of SRAM-based and anti-fuse FPGAs are very close. Anti-fuse technology tends to require lower power. They also keep the design information secure since they do not require an external device to program them at power-up .

Table 1: Programming Technologies

	SRAM technology	**Flash technology**	**Anti-fuse technology**
Speed	Fast	Slow	Fast
Density	Slightly dense	In-between	Highly dense
Volatile property	Volatile	Non-volatile	Non-volatile
Re-programmable	Yes	Yes	No
Security	Low	High	High
Power consumption	High	Low	Low

The third technology offers advantages of both the first and second technologies. Flash-based devices use a standard semiconductor process like the SRAM devices. These are non-volatile and therefore use less power and the intellectual property of the design is secure. Also, we can reprogram the Flash-based devices multiple times while operating in the system. A drawback is that they are slower than either SRAM or anti-fuse devices [7].

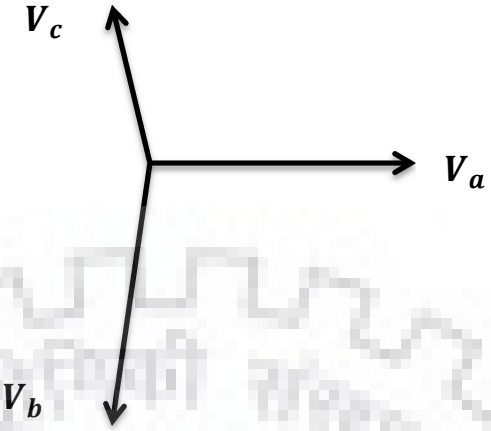
3. SYMMETRICAL COMPONENT METHOD

C.L. Fortescue gave this method in 1913. With the help of this method, a set of three unbalanced phasors are resolved into following three sets of balanced phasors:

- Zero sequence
- Positive sequence
- Negative sequence

The positive sequence here is a set of three balanced phasors with the phases having the original phase sequence, the negative sequence here is a set of three balanced phasors with the phase sequence opposite to that of the original sequence, while the zero sequence is set three phasors which are equal in magnitude as well as phase.

Figure 4 shows an unbalanced phase network is resolved into a three sets of phase networks which are the three sequence components that are mentioned above. It has an unbalanced phase network with three phasors denoted by 'V_a', 'V_b' and 'V_c', and it also has the positive, negative and the zero sequence components which are here denoted with subscripts of '1', '2' and '0'. By this it means that the positive, negative and zero sequence components are represented by respective voltages V_{a1}, V_{a2} and V_{a0}. The figure here shows the resolution of the three unbalanced voltage phasors, and the three unbalanced 'current' phasors can be resolved into the positive, negative or zero sequence components [2].



(i)

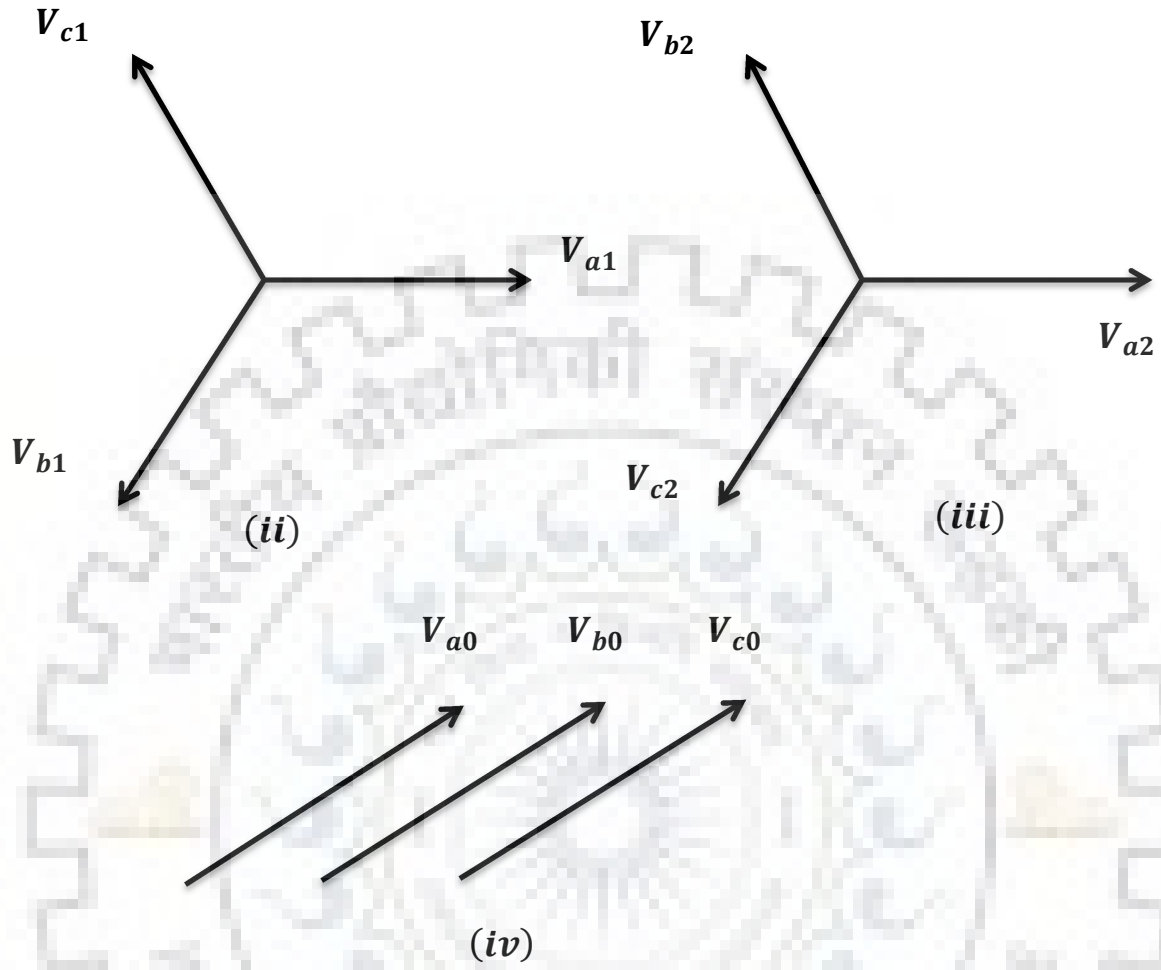


Figure 4: (i) Unbalanced network, (ii) Positive sequence, (iii) Negative sequence and (iv) Zero sequence

Here it can be seen that the positive sequence component has phase sequence of a-b-c and will always be present within the system. The negative sequence component has phasors equal in magnitude and 120^o apart from each other with opposite phase sequence of a-c-b. And the zero sequence component has phasors equal in magnitude with all three phasors in same phase.

The symmetrical component method can be used to resolve the unbalanced set of three phase voltages (or currents) as follows:-

$$V_a = V_{a0} + V_{a1} + V_{a2} \quad (1)$$

$$V_b = V_{b0} + V_{b1} + V_{b2} \quad (2)$$

$$V_c = V_{c0} + V_{c1} + V_{c2} \quad (3)$$

Here the $\propto$-operator is used. Its property is that it rotates a phasor 120^o in anti-clockwise direction, which is the assumed positive direction of rotation. So we can say that phase-b lags phase-a by 120^o.

$$\propto = 1\angle 120^o = \cos 120^o + j \sin 120^o = 0.5 + j\, 0.866 \quad (4)$$

$$\propto^2 = 1\angle 240^o = \cos 240^o + j \sin 240^o = 0.5 - j\, 0.866 \quad (5)$$

$$\propto^3 = 1\angle 360^o = \cos 360^o + j \sin 360^o = 1 \quad (6)$$

Also, since $\propto^3 = 1$, so that $\propto^{-1} = \propto^2$.

So summing equations (4), (5) and (6),

$$1 + \propto + \propto^2 = 0 \quad (7)$$

Hence, interestingly, we can note that 1, $\propto$ and $\propto^2$ are the three cube roots of unity.

Using this $\propto$-operator, we can represent the zero, positive and negative sequence respectively as:

$$V_0 = V_{a0} = V_{b0} = V_{c0} \quad (8)$$

$$V_1 = V_{a1} = \propto V_{b1} = \propto^2 V_{c1} \quad (9)$$

$$V_2 = V_{a2} = \propto^2 V_{b2} = \propto V_{c2} \quad (10)$$

Therefore, using equations (1), (2), (3), (8), (9) and (10), we can write,

$$V_a = V_0 + V_1 + V_2 \quad (111)$$

$$V_b = V_0 + \propto^2 V_1 + \propto V_2 \quad (112)$$

$$V_c = V_0 + \propto V_1 + \propto^2 V_2 \quad (113)$$

As we have written the a-b-c phase quantities in terms of 0-1-2 sequence components in equations form, we can write them in matrix form as,

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \propto^2 & \propto \\ 1 & \propto & \propto^2 \end{bmatrix} \begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} \quad (14)$$

Now we define,

$$A = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \propto^2 & \propto \\ 1 & \propto & \propto^2 \end{bmatrix} \quad (15)$$

$$V_p = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (16)$$

And

$$V_s = \begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} \quad (17)$$

Where, A is the symmetrical component transformation matrix,

V_p represents the actual phase voltages, and

V_s represents the sequence components.

On inversing,

$$A^{-1} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & \propto & \propto^2 \\ 1 & \propto^2 & \propto \end{bmatrix} \quad (18)$$

Therefore,

$$\begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & \propto & \propto^2 \\ 1 & \propto^2 & \propto \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (19)$$

Hence, the sequence components of the above 3-phase unbalanced set of voltages are determined using following equations:-

Zero-sequence component,

$$V_0 = (V_a + V_b + V_c)/3 \tag{20}$$

Positive-sequence component,

$$V_1 = (V_a + \propto V_b + \propto^2 V_c)/3 \tag{21}$$

Negative-sequence component,

$$V_2 = (V_a + \propto^2 V_2 + \propto V_0)/3 \tag{22}$$

4. WORKING PROCEDURE

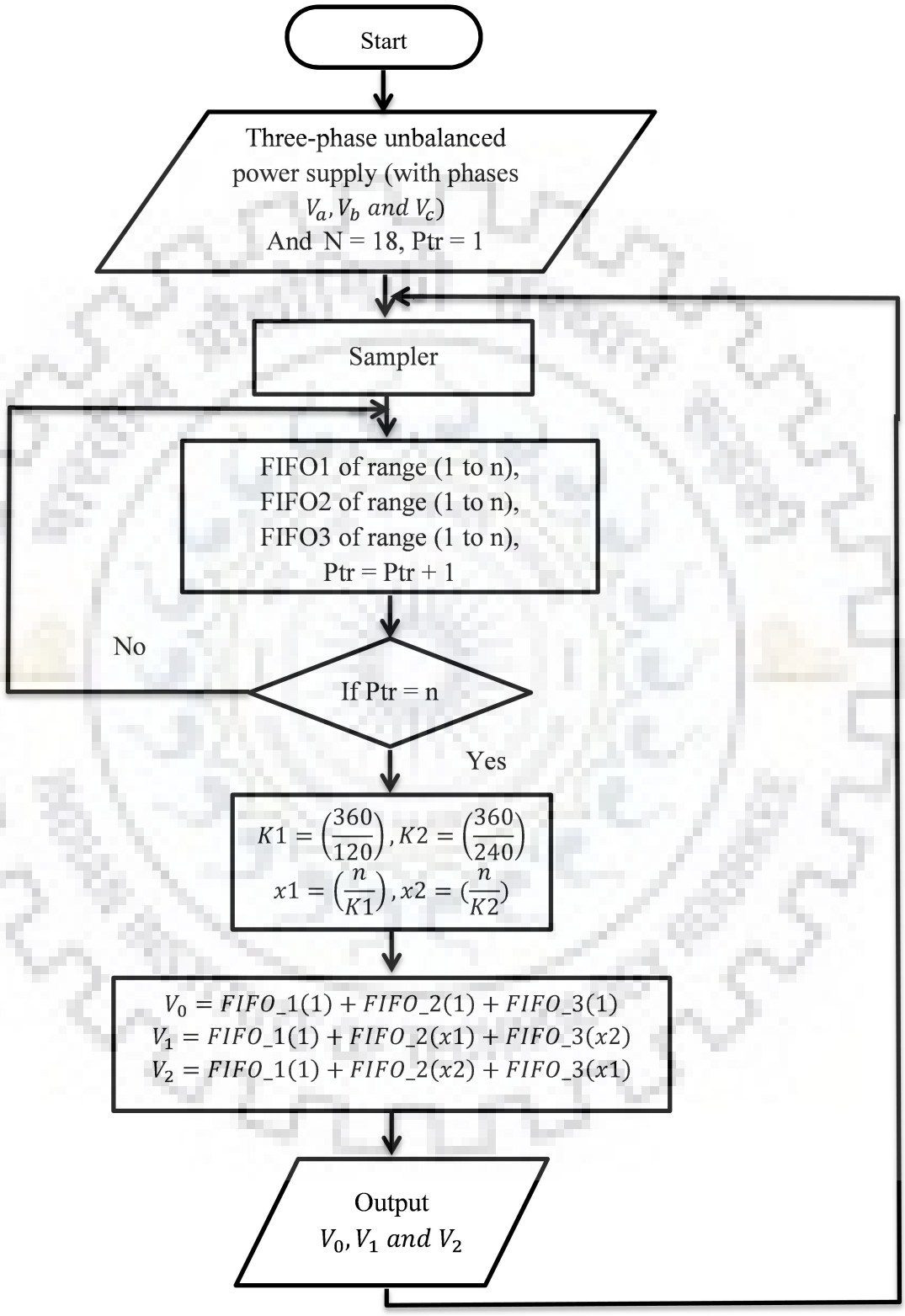


Figure 5: Schematic flowchart of the working

Figure 5 shows the schematic flowchart which comprises of all the steps that an input signal needs to pass through. The input signal frequency used is $f_i = 50\ Hz$ and the sampling frequency is $f_s = 900\ Hz$. So the numbers of samples taken are determined as follows:

$$N = \left(\frac{f_s}{f_i}\right) = \left(\frac{900}{50}\right) = 18$$

The phases are introduced to the sampler with sampling frequency of f_s. The samples of all three phases are then recorded in First In First Out memories (FIFO) with the word length of N.

As the pointer Ptr becomes equal to the number of samples N, the sequences, V_0, V_1 and V_2 are determined using the conventional symmetrical component method. If the pointer Ptr is less than the number of samples N, the design keeps on filling the FIFO memories.

These results are recorded for different types of inputs that include balanced and unbalanced three-phase systems to verify the working of the system.

5. SPARTAN-3E FPGA STARTER KIT

The FPGA device we are using here is Spartan-3E FPGA Starter Kit. To have most functionality for Spartan-3E Starter Kit board, some system level design trade-offs are necessary. It has three different memory configuration sources for demonstrating new Spartan-3E FPGA capabilities

On-board the Starter Kit has Texas Instrument's triple-regulator (TPS75003) for powering the FPGAs. Contrary to this, a separate high-current supply is required for the on-board DDR SDRAM.

5.1 Switches, Buttons and Knobs

5.1.1 Slide switches

It has four slide-switches which are in lower right corner of the board with labeled SW3 to SW0, with SW3 as left-most while SW0 as right-most switch as shown in Figure 6.

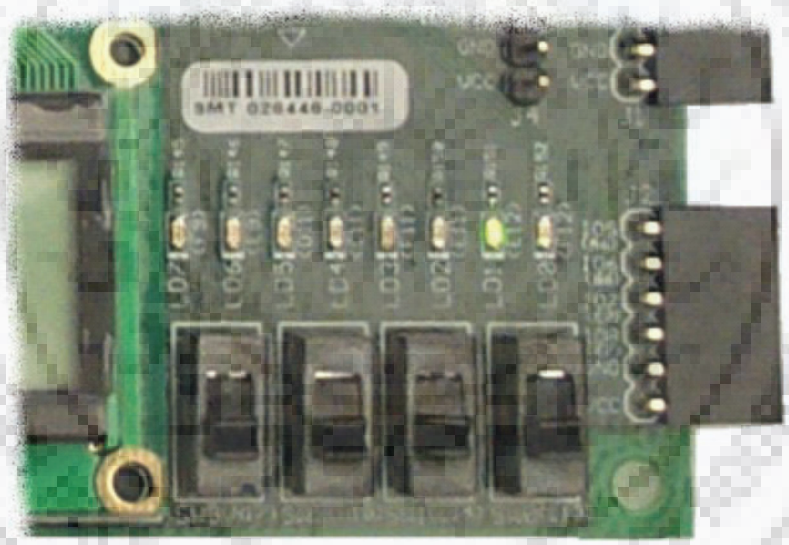


Figure 6: Slide Switches

When in UP (ON) position, the switch connects the FPGA pin to 3.3 V (logic HIGH), while in DOWN (OFF) position, it connects the pin to ground (logic LOW).

5.1.2 Push-button switches

It has four push-button switches in lower left corner of the kit with labeled as BTN_EAST, BTN_WEST BTN_NORTH, BTN_SOUTH as shown in Figure 7.

Pressing them connects associated pin to 3.3V.

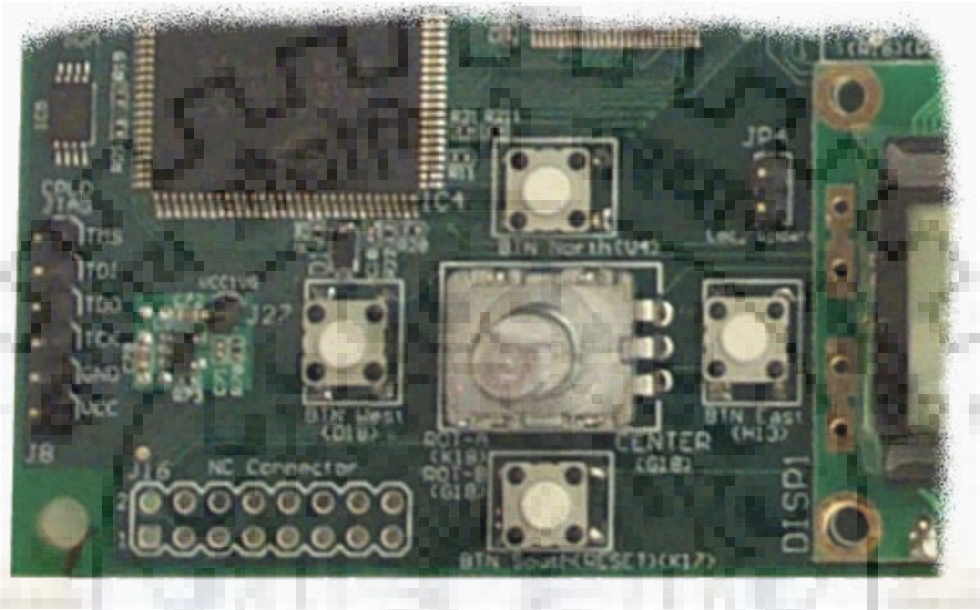


Figure 7: Push-button switches around the Rotary switch

5.1.3 Rotary Push-button switch

It is at the center of the Push-button switches as shown in Figure 7. This switch has three outputs, where ROT_A and ROT_B are two shaft encoder outputs and ROT_CENTER is the center push-button.

Rotating the shaft operates two push-buttons. Switches open and close depending on the way the shaft is rotated. Both switches are closed, when shaft is stationary. It is called *detent* position.

5.1.4 Discrete LEDs

It has eight LEDs located above the slide switches with labels LD7 through LD0, having LD7 left-most and LD0 right-most as shown in Figure 8.

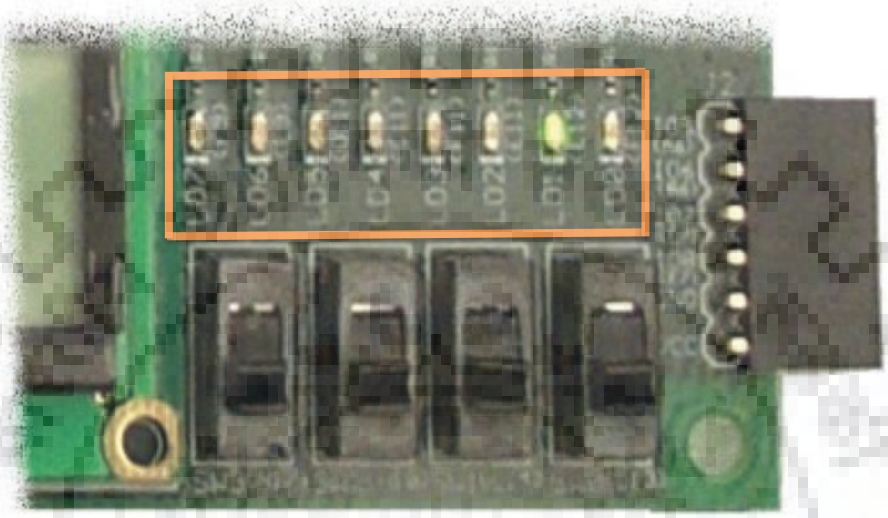


Figure 8: Discrete LEDs

5.2 Clock sources

Figure 9 shows three clock sources just below the “Xilinx” logo.

- ✓ It has an on-board 50 MHz clock oscillator.
- ✓ Clocks can be supplied off-board via SMA-style connector.
- ✓ A separate 8-pin DIP-style clock oscillator can be installed in supplied socket.

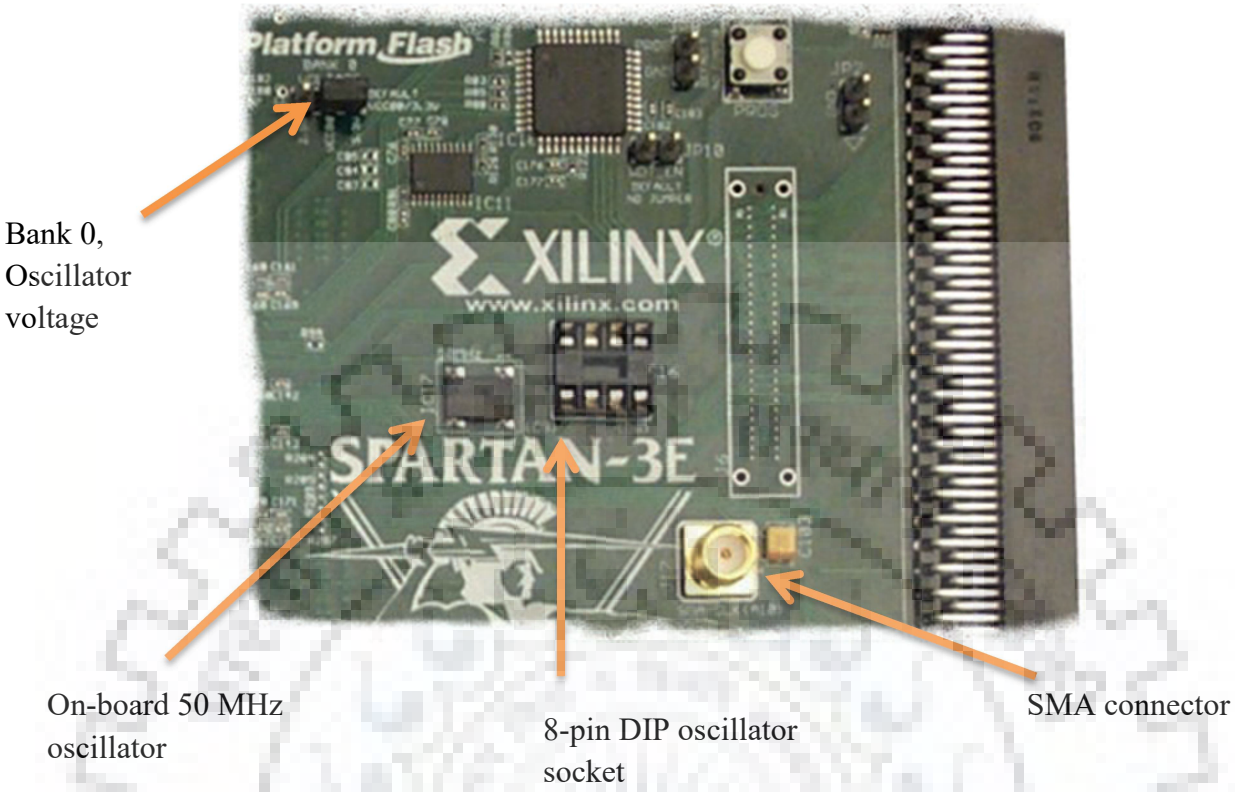


Figure 9: Available clock inputs

I/O Bank 0 has each clock input connected directly to global buffer input. Voltage for all I/O pins in I/O Bank 0 is controlled by jumper JP9.

On-board oscillator is a 3.3V device, which might not perform as expected if JP9 is set to 2.5V. On-board 50 MHz oscillator has 40% - 60% duty-cycle.

8-pin DIP footprint fitted with clock oscillator is accommodated in 8-pin socket. This is used when we require frequency other than 50 Mega-Hz or FPGA's Digital Clock Manager (DCM) can be used to generate other frequencies from on-board 50 MHz oscillator.

SMA connector is used when external clock source is used.

5.3 Character LCD screen

We have a 2-line by 16-character Liquid Crystal Display (LCD) on-board this FPGA Starter Kit. LCD supports 8-bit data interface, but the Starter Kit uses 4-bit data interface to remain compatible with other Xilinx development boards and to minimize total pin count. Compared with 50 MHz on-board clock, the display is slow. The LCD is powered by +5V. Since, the FPGA I/O signals are powered by 3.3 V, FPGA's output levels are recognized as valid LOW/ HIGH by the LCD. LCD controller is compatible for 5V TTL and 3.3V LVCMOS outputs.

5.4 VGA Display Port

We have a VGA display port on-board our Spartan-3E Starter Kit vie a DB15 connector in left most corner at top shown in Figure 10. This port can be connected directly to the PC monitors or LCDs using a standard monitor cable.

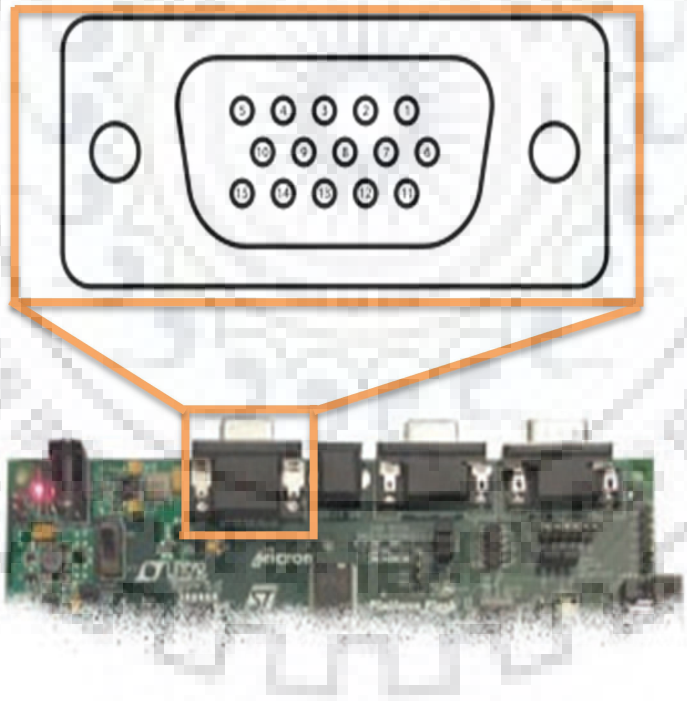


Figure 10: DB15 VGA connector

5.5 RS-232 Serial port

We have on-board two RS-232 serial ports, a female DB9 DCE connector and a male DTE connector as shown in Figure 11 a standard serial cable connects the DCE port directly to the serial port connector on PC. The DTE connector controls other RS-232 peripherals such as modems/ printers or performs simple loopback testing with DCE connector.

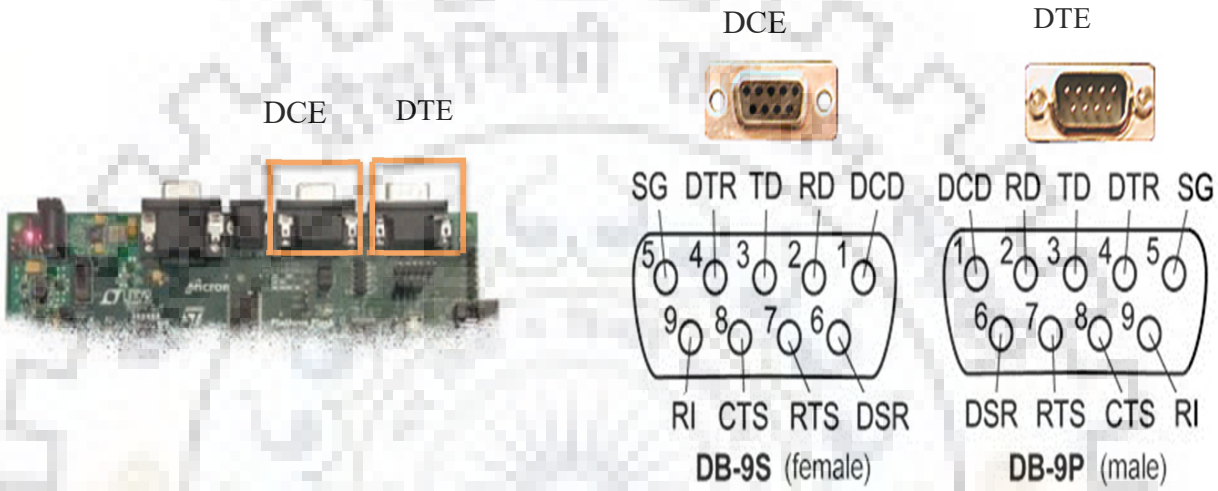


Figure 11: RS-232 Serial ports

A Maxim device is used to convert the LVTTL or LVCMOS levels serial outputs from FPGA to appropriate RS-232 voltage levels and vice-versa.

5.6 PS/2 Mouse/ Keyboard port

We have a PS/2 mouse/ keyboard port and a standard 6-pin mini-DIP connector (labeled J14) on board our Starter Kit. Only pins 1 and 5 of the connector attach to the FPGA. The PS/2 mouse/ keyboard location is shown in Figure 12.

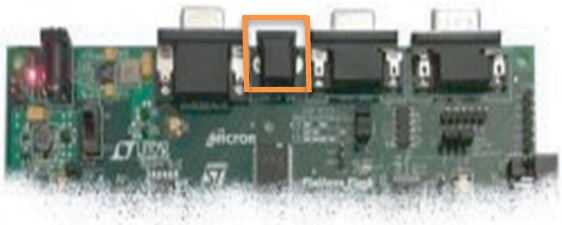


Figure 12: PS/2 connector location

5.7 Digital-to-Analog Convertor (DAC)

It has a SPI-compatible, serial, 4-channel, DAC (LTC2624) with 12-bit resolution present just above RJ-45 connector for Ethernet on-board. The four outputs from DAC appear on J5 as shown in Figure 13.

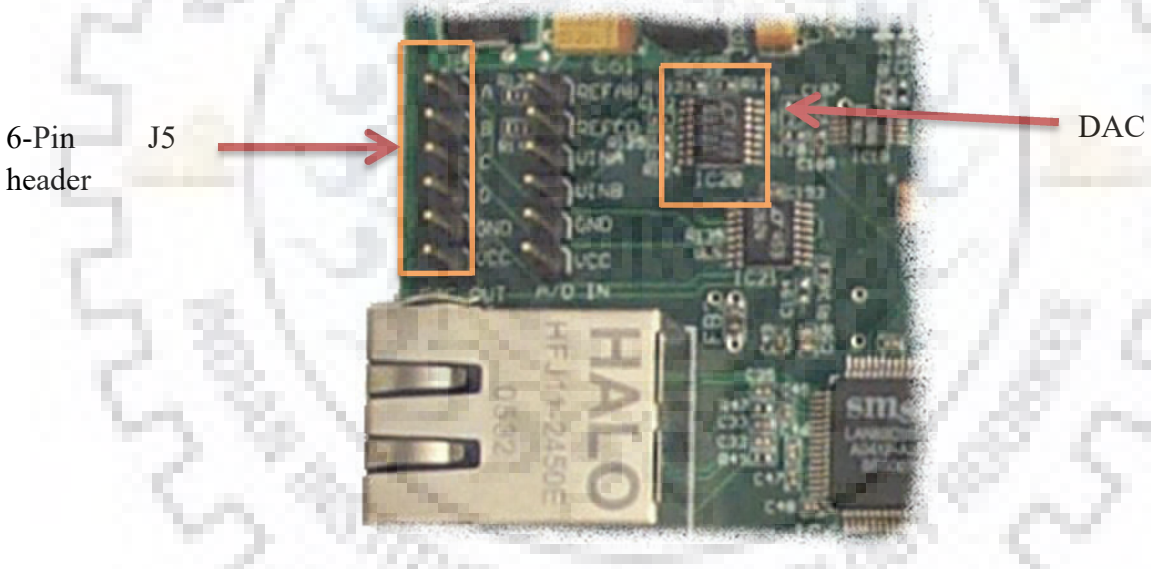


Figure 13: DAC and associated header

5.8 Analog Capture circuit

As shown in Figure 14, we have on-board a 2-channel analog capture circuit, having a programmable pre-amplifier (LTC6912-1) and an Analog-to-Digital-convertor (ADC). Analog inputs are supplied on J7 header. Output of pre-amplifier connects to the ADC (LTC1407A-1). FPGA programs serially and controls both the ADC and the pre-amplifier.

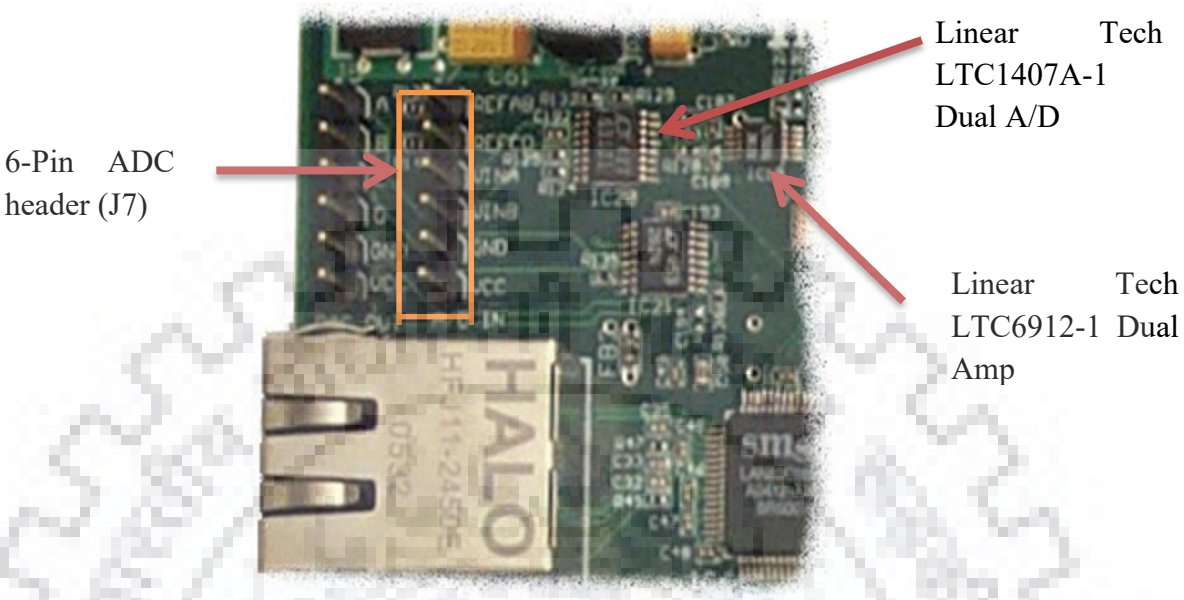


Figure 14: Two-channel Analog capture circuit

5.9 SPI Serial Flash

We have a STMicroelectronics M25P16 16 Mega-bit SPI serial Flash on-board the Starter Kit which provides alternative means to configure the FPGA.

- ✓ Simple non-volatile data storage
- ✓ Storage for identifier codes, serial numbers, IP addresses, etc.
- ✓ Storage of MicroBlaze processor code that can be shadowed into DDR SDRAM.

5.10 Ethernet Physical Layer Interface

As shown in Figure 15, it has an Ethernet physical layer (PHY) (LAN83C185) interface and a RJ-45 type connector. On-board 25 MHz crystal oscillator controls all the timings.

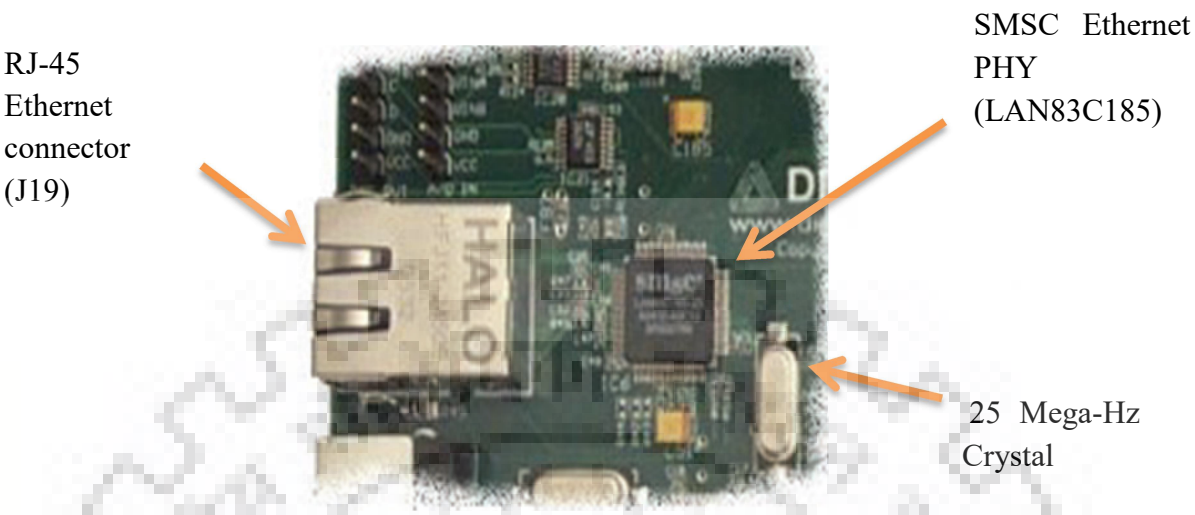


Figure 15: RJ-45 connector and Ethernet PHY Interface

6. DIGITAL SIMULATION RESULTS

Table 2, 3,4 and 5 present the samples input thee phase signals with $V_a, V_b \; and \; V_c$ denoting the three-phase balanced or unbalanced phases and $V_0, V_1 \; and \; V_2$ denoting the zero, positive and negative sequence components respectively. The samples are taken with the help of MATLAB. Some of the following simulation results are recorded while checking the initial working of the proposed work:-

a) Input data:

$$V_a = 10 \sin \theta$$
$$V_b = 10 \sin(\theta - 120^o)$$
$$V_c = 10 \sin(\theta + 120^o)$$

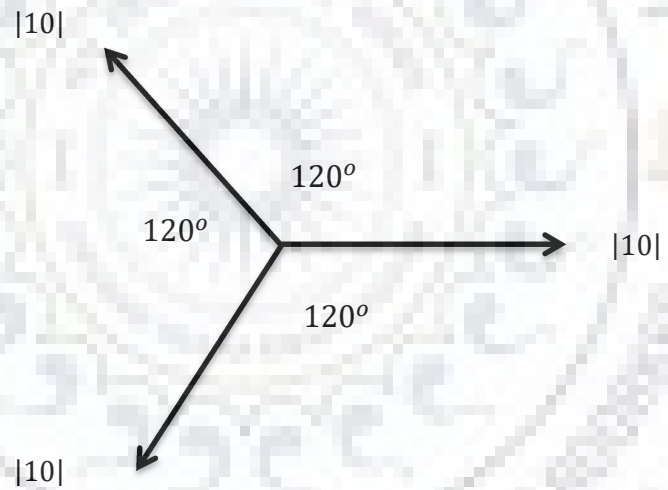


Figure 16: Input 1

Sampled data:

Table 2: Sampled data 1

	V_a	V_b	V_c
1	0	-5	5
2	3	-2	8
3	6	0	9
4	8	4	10
5	9	7	9
6	9	9	7
7	8	10	4
8	6	9	0
9	3	8	-2
10	0	5	-5
11	-3	2	-8
12	-6	0	-9
13	-8	-4	-10
14	-9	-7	-9
15	-9	-9	-7
16	-8	-10	-4
17	-6	-9	0
18	-3	-8	2

Simulation result:

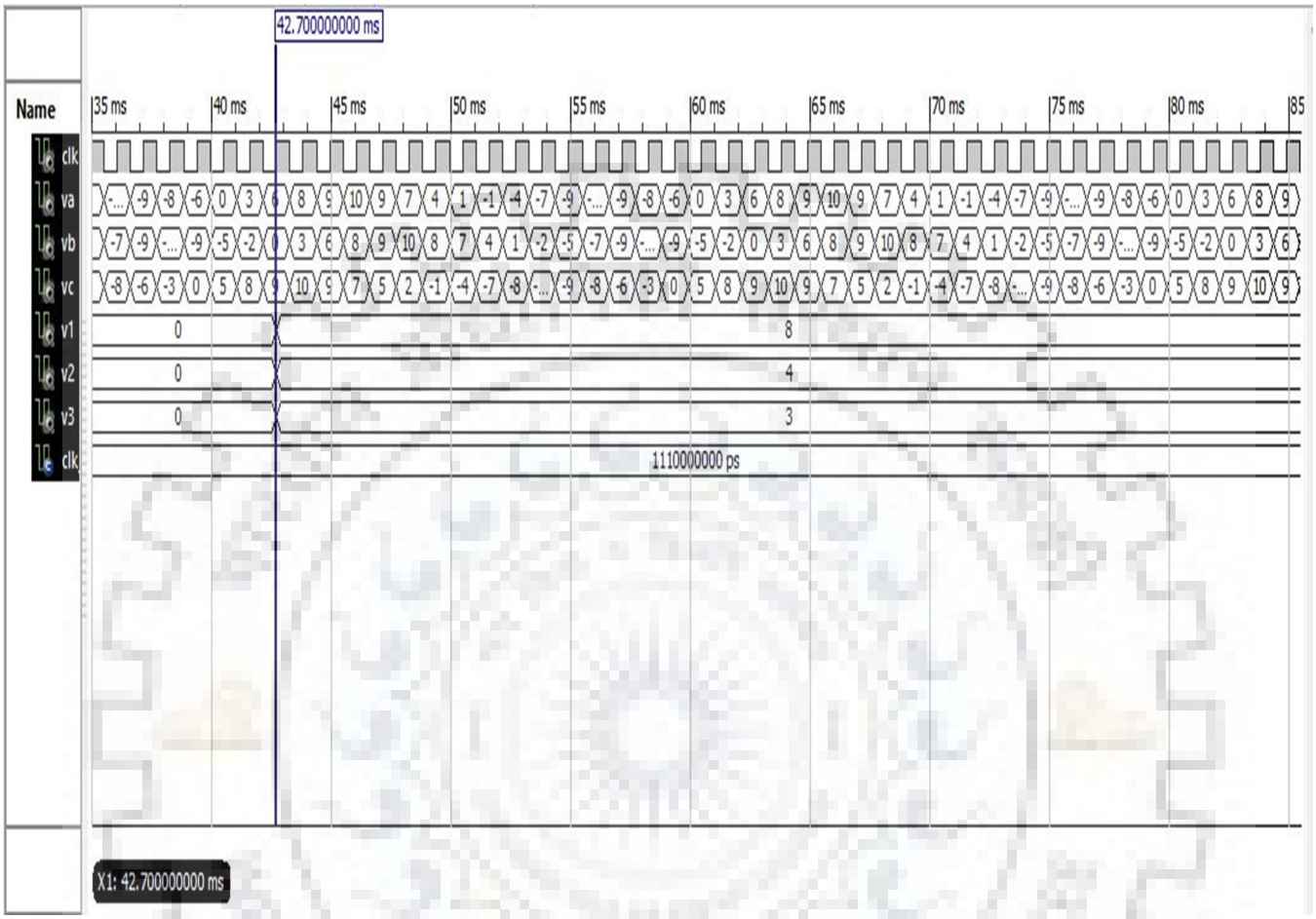


Figure 17: Simulation result 1

Output data:

$V_0 = 8\ V$
$V_1 = 4\ V$
$V_2 = 3\ V$

b) Input data: $V_a = 10\sin\theta$

$V_b = 10\sin(\theta + 50^o)$

$V_c = 10\sin(\theta + 250^o)$

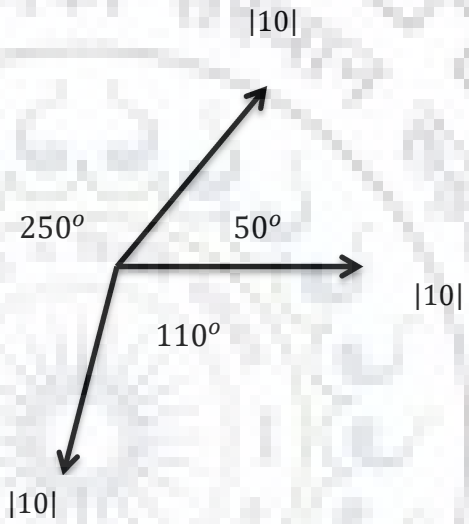


Figure 18: Input 2

Sampled data:

Table 3: Sampled data 2

	V_a	V_b	V_c
1	0	-2	-9
2	3	0	-8
3	6	4	-5
4	8	7	-2
5	9	9	0
6	9	9	4
7	8	9	6
8	6	8	8
9	3	5	9
10	0	2	9
11	-3	0	8
12	-6	-4	5
13	-8	-7	2
14	-9	-9	0
15	-9	-9	-4
16	-8	-9	-6
17	-6	-8	-8
18	-3	-5	-9

Simulation result:

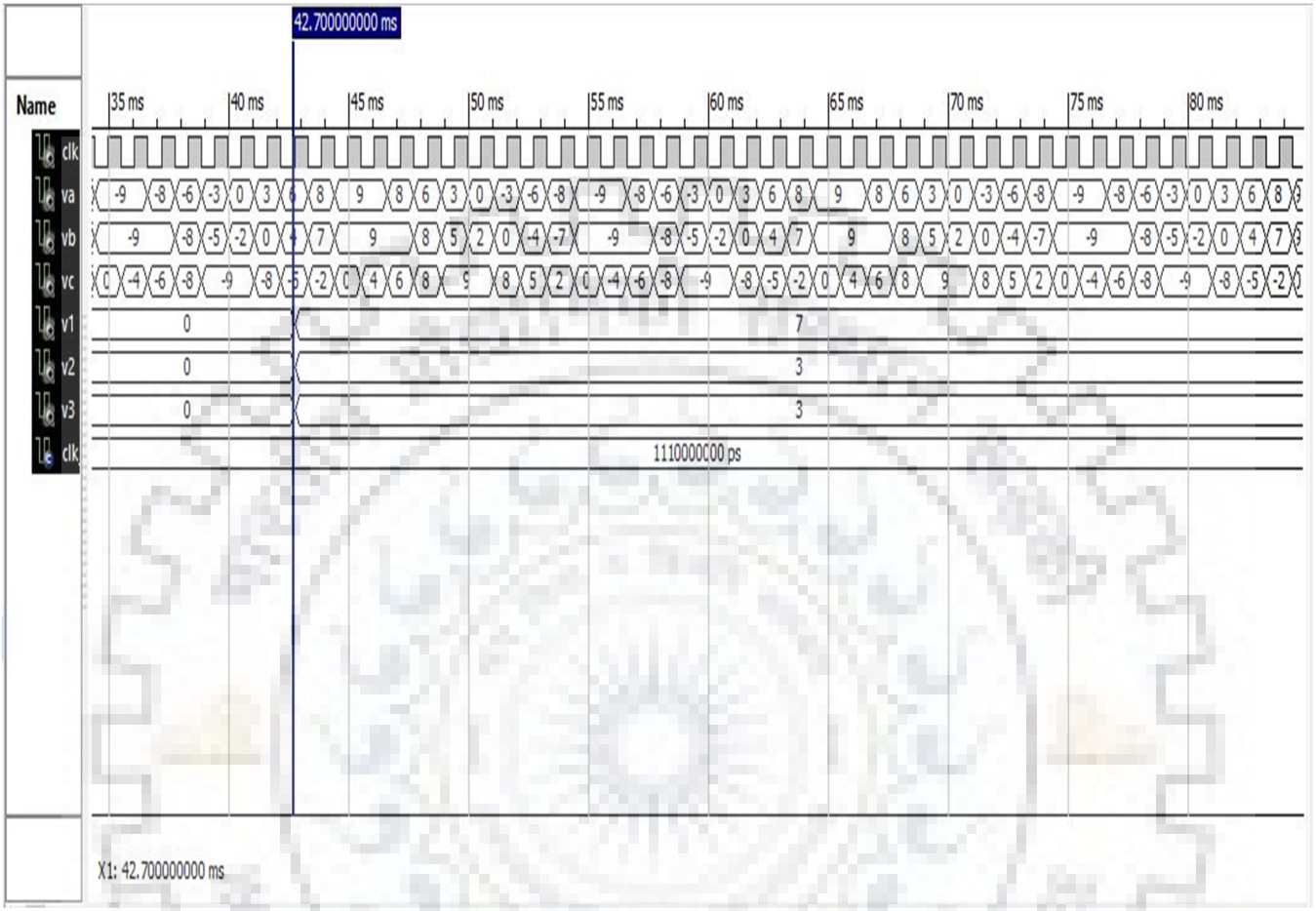


Figure 19: Simulation result 2

Output data:

$$V_0 = 7\ V$$
$$V_1 = 3\ V$$
$$V_2 = 3\ V$$

c) Input data: $V_a = 20\sin\theta$

$V_b = 50\sin(\theta - 120^o)$

$V_c = 75\sin(\theta + 120^o)$

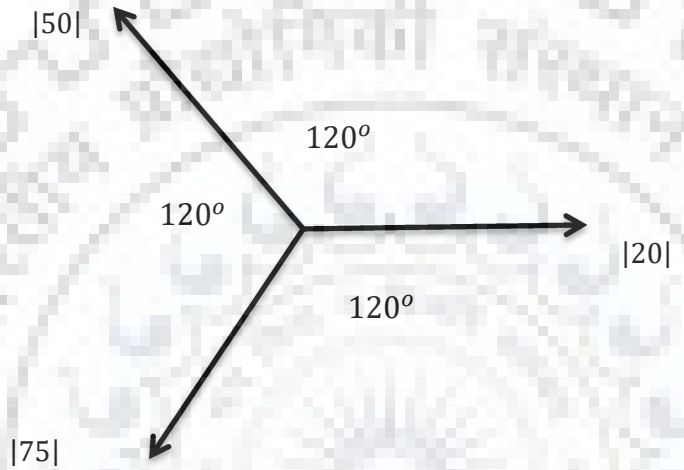


Figure 20: Input 3

Sampled data:

Table 4: Sampled data 3

	V_a	V_b	V_c
1	0	-29	43
2	6	-13	61
3	12	3	72
4	17	20	74
5	19	35	67
6	19	45	52
7	17	49	31
8	12	48	5
9	6	41	-20
10	0	29	-43
11	-6	13	-61
12	-12	-3	-72
13	-17	-20	-74
14	-19	-35	-67
15	-19	-45	-52
16	-17	-49	-31
17	-12	-48	-5
18	-6	-41	20

Simulation result:

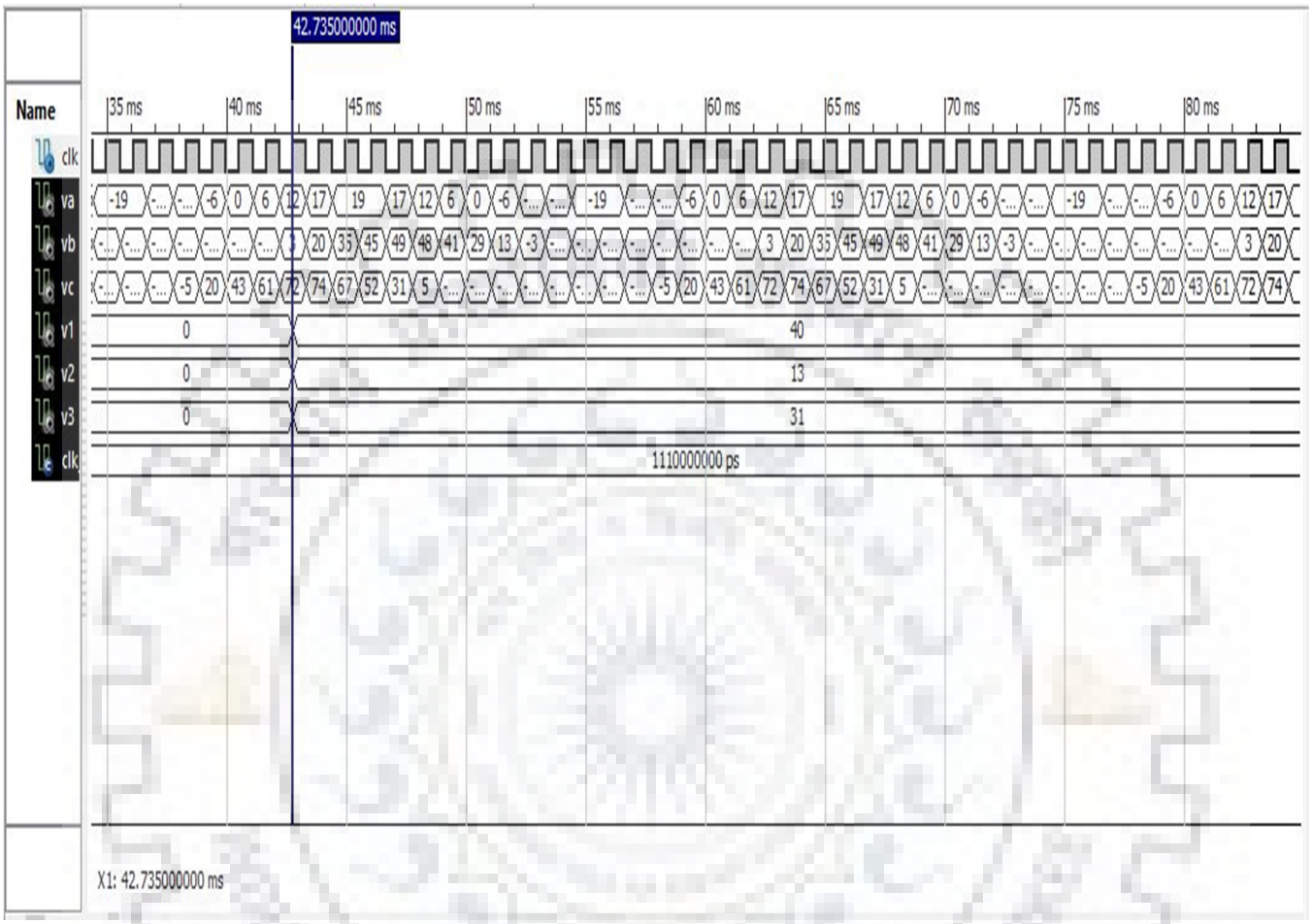


Figure 21: Simulation result 3

Output data:

$$V_0 = 40\ V$$
$$V_1 = 13\ V$$
$$V_2 = 31\ V$$

d) Input data: $V_a = 20\sin\theta$

$V_b = 60\sin(\theta + 60^o)$

$V_c = 15\sin(\theta + 250^o)$

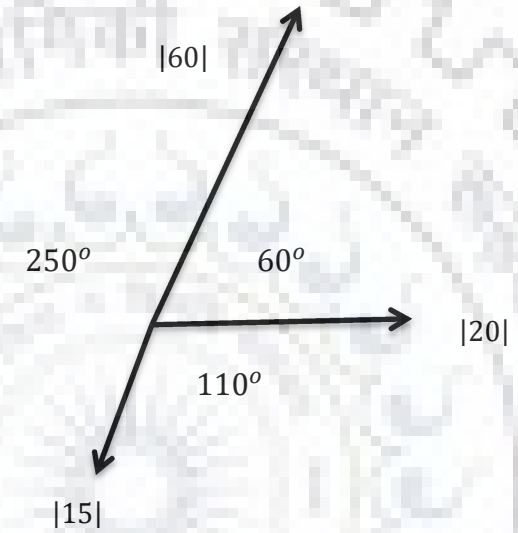


Figure 22: Input 4

Sampled data:

Table 5: Sampled data 4

	V_a	V_b	V_c
1	0	-18	-14
2	6	-36	-12
3	12	-50	-8
4	17	-58	-4
5	19	-59	1
6	19	-53	6
7	17	-40	10
8	12	-22	13
9	6	-2	15
10	0	18	14
11	-6	36	12
12	-12	50	8
13	-17	58	4
14	-19	59	-1
15	-19	53	-6
16	-17	40	-10
17	-12	22	-13
18	-6	2	-15

Simulation result:

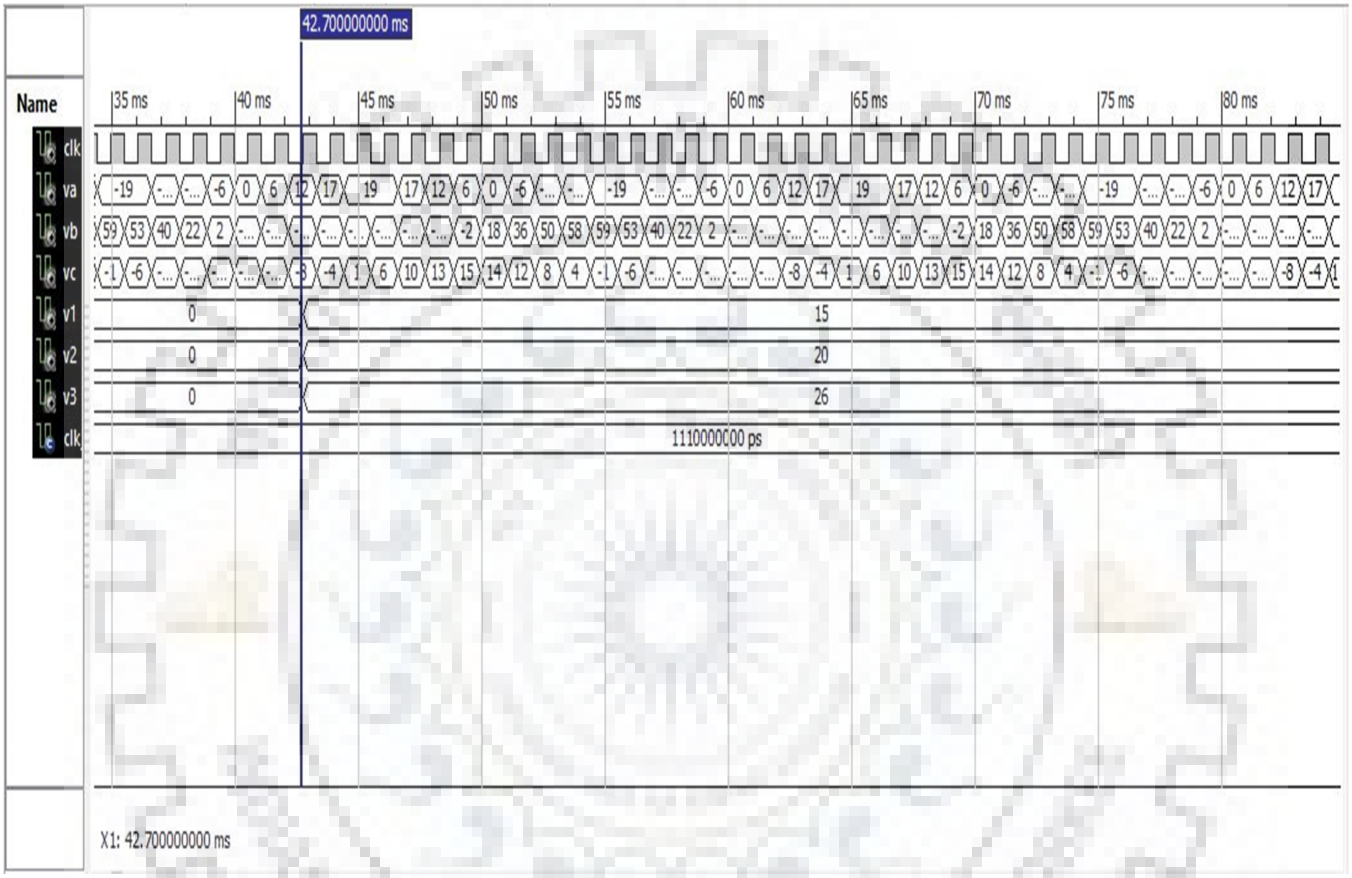


Figure 23: Simulation result 4

Output data:

$V_0 = 15\ V$

$V_1 = 20\ V$

$V_2 = 26\ V$

7. FUTURE ASPECTS

The proposed work can be taken further to be used for following applications:-

1) The method can be used for analyzing the rotating machinery's performance for single phase or unbalanced polyphase operations. It has also been considered for designing machinery on single phase railway systems.
2) With the help of instrument transformer connections and also the groups of external impedances, the zero, positive and negative phase sequence currents and voltages can be used directly for energizing the relays and regulating devices.
3) The positive sequence voltage is being used more and more for regulation of voltages because of its good voltage regulation, mostly because of its stability during faults.
4) There are some advanced schemes being considered for positive and negative sequences with the objective of involving the consumers to balance their loads. They can also be used in determining whether a particular machine is acting as a phase balance.

CONCLUSION

The work here provides a brief overview of the implementation of the three phase sequence detector using the FPGA design approach. The used design technique can reduce the developmental time as well as costs. Under the no-fault condition, the considered system is nothing but a symmetrical balanced system, hence only the positive sequence voltages and currents exist. While during a fault condition, because of which the power system become unbalanced, we can say that positive, negative and zero sequence voltages or currents exist. On using the real-time phase voltages or currents, with the help of symmetrical component method, the positive, negative and the zero sequence voltages or currents can be extracted from the balanced or unbalanced power system.

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