Performance Analysis of Non-volatile Memories Based Logic Gates

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Submitted by

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CANIDATE'S DECLARATION

I hereby declare that the work, which is being presented in this dissertation on entitled, "**Performance Analysis of Non-volatile Memories Based Logic Gates**", being submitted in the partial fulfilment of the requirements for the award of the degree of Master of Technology, in Microelectronics & VLSI, and submitted to the Department Electronics and Communication, Indian Institute of Technology Roorkee, India, is a summary of the study and authentic work carried out by me during the period June 2018 to June 2019, under the guidance of **Dr. B. K. Kaushik**, Associate Professor, Department of Electronics and Communication, Indian Institute of Technology Roorkee, India.

The matter presented here is my understanding of literature in this field and is written in my own words.

Piyush Tankwal — Place: Roorkee

Enrolment No. -17534006 — Date: 06-06-19

CERTIFICATE

This is to certify that the above statement made by the candidate is true to the best of my knowledge and belief.

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ABSTRACT

Rapid development in the technology of memories has grown the interest in spintronic field in the last few years. The main reason of this is Moore's law reaching towards its physical limit below 45nm. The static power dissipation in complementary metal oxide semiconductor (CMOS) technology become a bottleneck for further scaling. The spintronics is the best substitute to replace the CMOS technology in future because of its property of zero stand by power and non-volatility. The magnetic tunnel junction (MTJ) is the fundamental device to store the logics. The MTJs have two types (i) in-plane MTJ (IMTJ) (ii) perpendicular MTJ (PMTJ). The PMTJ is more efficient than IMTJ because it requires less write current and high scalability. Spintronics based memories such as spin transfer torque magnetic random access memory (STT-MRAM) uses spin property of an electron to differentiate between logic '0' and logic '1'. In the last few decades, the leading memories are dynamic random access memory (DRAM), static random access memory (SRAM) and flash memory. These memories have some drawbacks such as SRAM has high standby leakage power, large on chip area. DRAM manufacturing process is complex and it is required refreshing current periodically. Flash memory (non-volatile) requires excess write power. There is a requirement for single memory that can overcome the limitation of the existing memory technologies.

The aim of this dissertation is to explain performance analysis of non-volatile memories based logic gates at the depth. I mainly focused on spin valve, magnetic tunnel junction (MTJ), STT-MRAM, read/write operation, and spin orbit torque (SOT), read/write operation of SOT, differential spin Hall effect (DSH) based MRAM, read write operation of DSH-MRAM, logic gates based on STT/DSH-MRAM and the analysis of the STT and DSH switching techniques. Spintronics based memories are the capable candidate for the future universal memories has properties such as low power consumption, small access time, high endurance, high density, low cost per bit, non-volatility and small on chip area.

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CHAPTER1

INTRODUCTION

1.1 Evolution of Memory Technology

In last few eras, Complementary Metal Oxide Semiconductor (CMOS) technology has played a pivotal part in the electronic field to keep pace with Moore's Law. Memory technologies witnessed a rapid change in terms of performance [1]. In conventional memory data is stored as of charge, according to the charge stored at a node data is recognized as logic '0' or logic '1'. Metal oxide field effect transistor (MOSFET) technology is approaching towards its physical limits due to large static power dissipation, short channel effects (SCE), and other effects [2] - [4]. These effects degraded the performance of the CMOS device below 45-nm technology nodes.

Memories are mainly two types: volatile and non-volatile memory depending upon the data retention with power supply. Volatile memories will retain the data only in the presence of power supply while non-volatile memories retain the data even power supply is off. In 1968 with one transistor and one capacitor per cell, DRAM cell was invented at IBM Thomas J. Watson research centre. Intel releases its first 64-bit static read only memory (SRAM) in 1969 [5]. The evolution of memories is shown in the Figure 1.1.

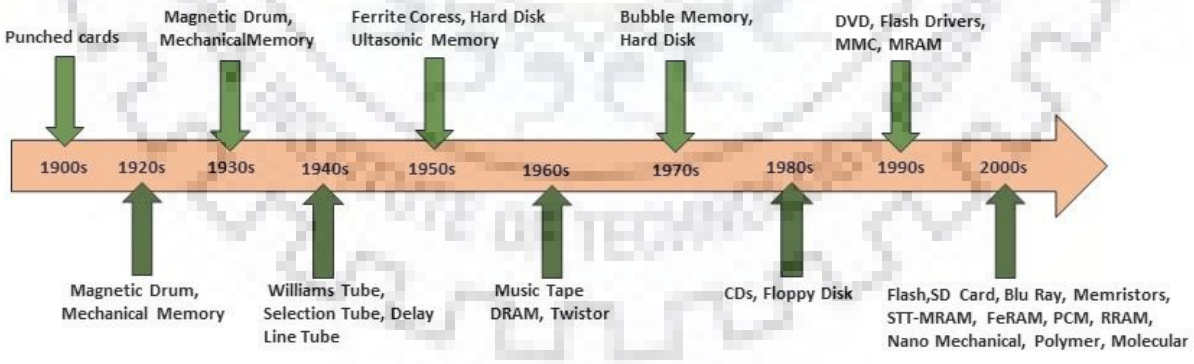


Figure 1.1 Evolution in memories technology

These memories have some drawbacks such as SRAM has the constraints of high standby leakage power and large area. DRAM manufacturing process is complex and it requires

refreshing current periodically. Flash memory (non-volatile) requires excess write power and large access time.

Because of these issues researchers are looking for the new technology that can fulfil all the necessities such as high speed, low static power dissipation, and non-volatlity. Emerging non-volatile memories such as resistive random access memory (RRAM), Spintronics based memories such as magnetoresistance read only memory(MRAM), spin transfer torque MRAM (STT-MRAM) and ferroelectric RAM (FeRAM) are the promising candidates for future storage applications. Among these non-volatile memories alternatives, STT-MRAM and DSH-MRAM are the most suitable due to its unlimited endurance, reliability, small size, non-volatility and ease of fabrication with CMOS [6] - [9].

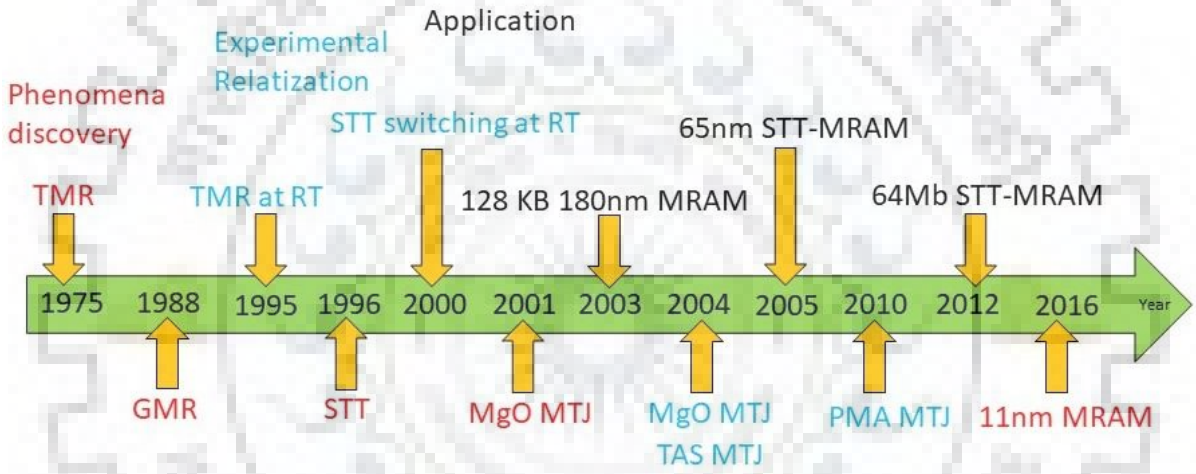


Figure 1.2 Evolution in spintronics memories technology

1.2 Thrust for Non-volatile Memories

With continuous scaling, the CMOS technology moving towards its physical limit, below 45-nm technology node due to SCE (e.g., drain induced barrier lowering (DIBL), gate induced drain leakage (GIDL), mobile degradation, hot carrier effects, quantum mechanical tunneling) and increase in static leakage power. Intel has suggested that transistors will stop shrinking by 2021 and Moore' law was scrapped in 2016. Now transistors on the chip will double in 2.5 to 3 years [10]. Hence, researchers are looking for an alternative to charge based memories. Spintronics is an efficient alternative to CMOS technology. In spintronics, spin of an electron is used as a state variable. Spin transfer torque (STT) and giant magnetoresistance (GMR) are the key phenomenon that are used in spintronics.

GMR effect introduced by Albert Fert and Peter Grunberg [11]. For that they get Nobel prize in 2007 and STT effect was introduce in 1996 [12] - [13]. These effects GMR, STT, SHE are used in most of magnetic memory. In STT-MRAM STT effect used to write the data and tunnel magnetoresistance (TMR) effect is used to read the data from the MTJs cell and in DSH-MRAM Rashba and spin Hall effect are used [14].

Normally in non-volatile device with the non-volatile computing system users no need to reboot their system every time because of its non-volatility. It diminishes the static power and delay time to ON of system. The NV devices having features high speed, high endurance and low power consumption is important to attain low power computing. The memory hierarchy of conventional system have both volatile and non-volatile memory to store the data in order to achieve enhanced performance and low cost of a system as represent in Figure 1.3(a). The top level of memory hierarchy of conventional system composed of CMOS based register and volatile flip-flop (FF) in direction of achieving high speed. But they are very expensive and takes large on-chip area. The cache level of memory hierarchy has SRAM and the main memory consists DRAM. The SRAM and DRAM both are in volatile in nature as well as both are dissipate large static power. In order minimize the static power dissipation the volatile memories in computational system are replaced by the non-volatile memory as represent in Figure 1.3(b) [15].

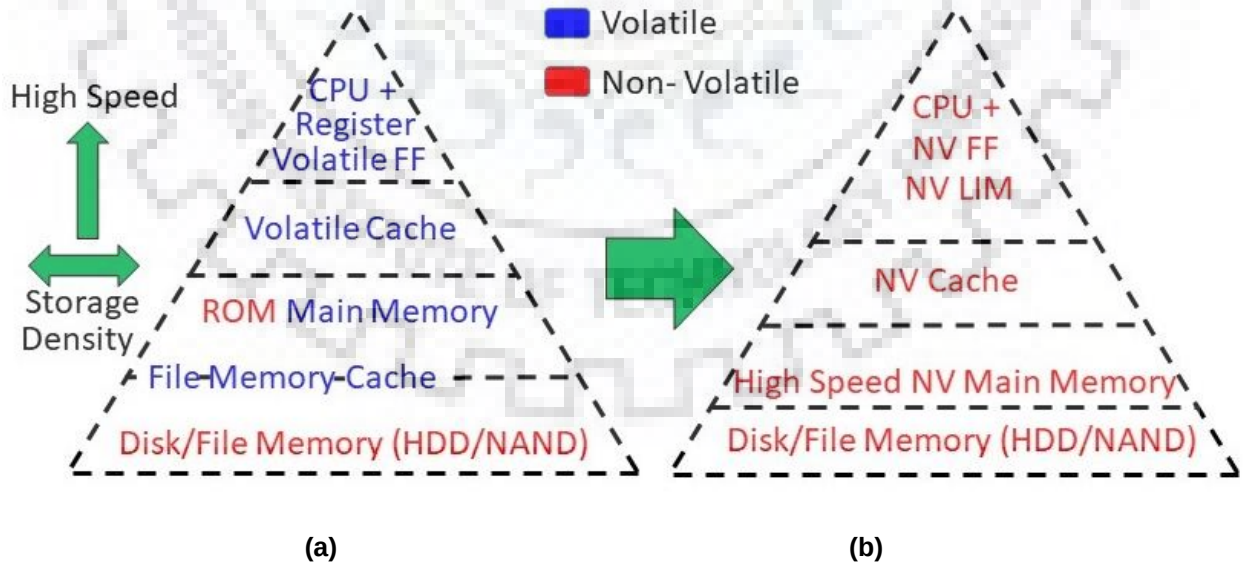


Figure 1.3: (a) Memory hierarchy of conventional system, (b) Non-volatile memory based system [15].

The Von-Neumann architecture of a computing system having separate memory and data at the computing level because of that it is facing some serious issues such as limited memory

bandwidth, huge loss of power as static power dissipation. The in-memory computation and the non-volatile memory technology is the best solution to minimize these kind of effects. It is more power efficient but it takes large on-chip area [15].

CHAPTER2

SPINTRONICS

2.1 Basics of Spintronics

As CMOS technology (charge based) comes to their end due to large statics power dissipation, short channel effect (SCE) and other effects. To overcome these effects researchers are putting lot of efforts from device to circuit level. Spintronics is an efficient alternative to CMOS due to small size and negligible static power dissipation. Spin of a single electron or group of electrons is used to store information. Electron spin produce a magnetic moment which is opposite in the direction of the spin angular momentum of an electron as represent in Figure 2.1.

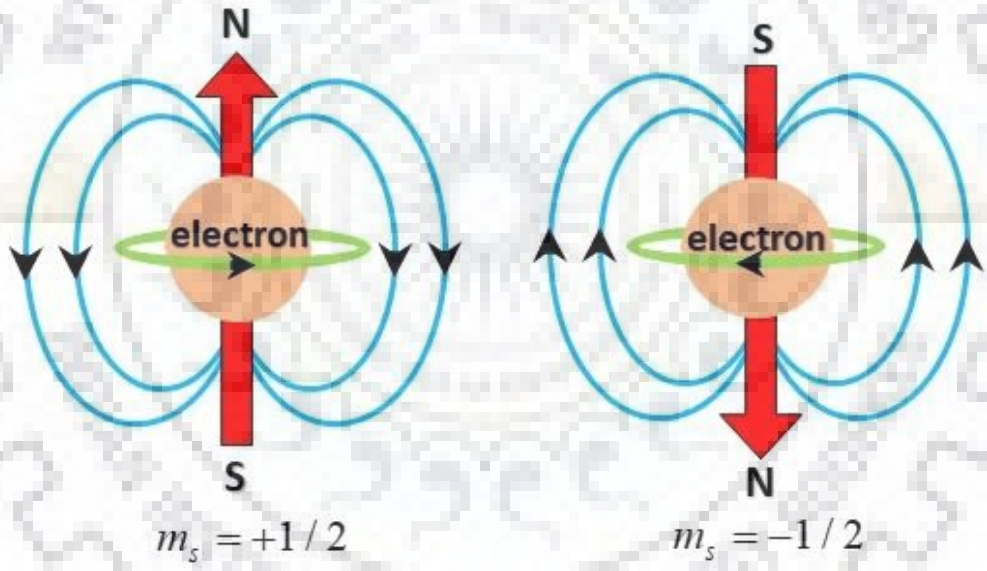


Figure 2.1 Magnetic moment of electron

If we see electrons as a charge particle which is rotating about their axis which have the angular moment L then its magnetic dipole moment is

$$\mu = -\frac{e}{2m_e}L$$

Here, m_e is the rest mass of the electron.

L is spin angular moment.

Using spin property of an electron with the charge provides different effects, enhanced capabilities, and others functionalities for the nanoscale devices. The electron spin is a vector quantity that acts like a magnetic moment with magnitude and direction.

The spin polarization of an electron has only two orientations one is parallel to the field and another is anti-parallel to the field in presence of magnetic field. We can utilize these orientations in our applications as consider the parallel and anti-parallel to logic '1' and logic '0'. Sometimes majority spin sees as up and minority spin seen as down spin electron [11].

2.2 Spin Injection

Under non-equilibrium condition the change in the electron spin known as spin accumulation. The electrically electron spin injection from ferromagnet (FM) to nonmagnetic (NM) is main step in the spintronics devices [16]. This concept was proposed in 1976 by Aronov [16]. It is internal property of FM material layer that when we pass electrical charge current through the FM layer it generates the spin polarized current. In the ferromagnetic metal, such as Fe, difference in the up and down-spin densities of electrons under equilibrium is exists. This difference is known as a spin polarization. A nonmagnetic material exhibits equal up-spin and down-spin channels under equilibrium condition as shown in Figure 2.2(a). A ferromagnet under equilibrium have a spin polarization represent in Figure 2.2(b).

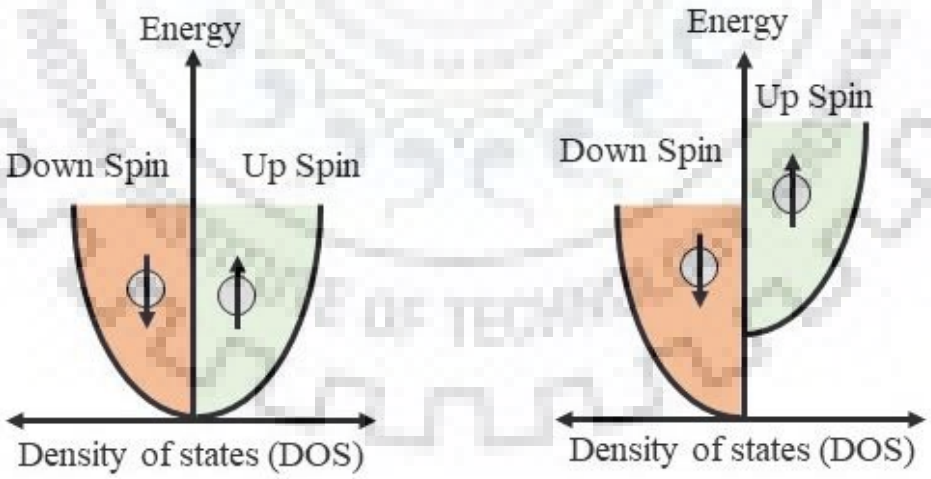


Figure 2.2 Energy v/s DOS diagrams of (a) NM (non-magnetic material) (b)FM (ferromagnetic material)

Due to difference in the densities the non-equilibrium spin polarization. The injected spin polarization travelling due to an electric field as represent in Figure 2.3(a). The non-

equilibrium spin developed can travel diffusively due to a concentration gradient called as spin diffusion as represent in Figure 2.3(b) [17].

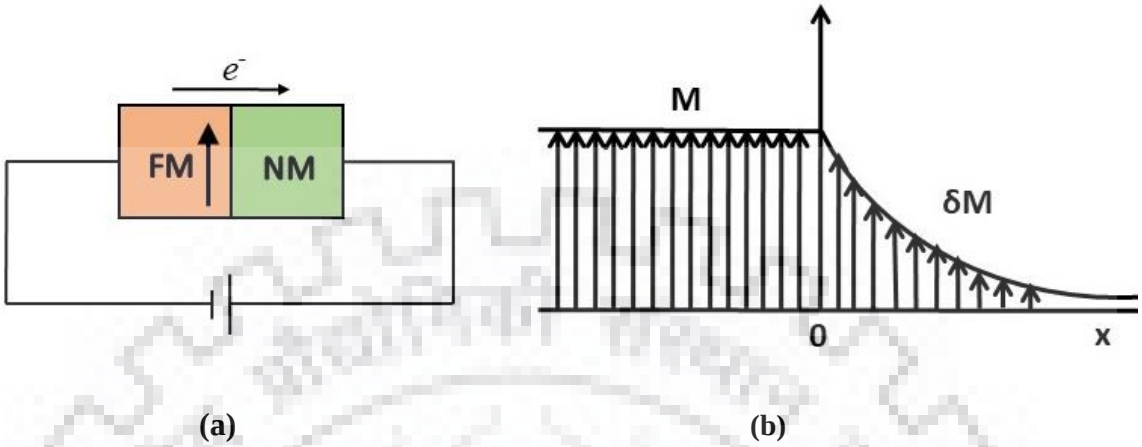


Figure 2.3 (a) An FM-NM interface (b) Spin-Diffusion(diffusively)

2.3 Direction of STT and the Landau–Lifshitz–Gilbert(LLGS) equation

Detection of spin current is the moment exchange between the flux of electrons and magnetization of the ferromagnetic layer (FM), generally, called as the STT effect [18-19]. The behavior of Magnetization ($\overrightarrow{M}$) in a FM layer can be transcribed in the mathematical form as represent in equation (1).

$$\frac{\partial \vec{m}}{\partial t} = \underbrace{-|\gamma|\left(\vec{m} \times \overrightarrow{H_{eff}}\right)}_{Precession} + \underbrace{\alpha \vec{m} \times \frac{\partial \vec{m}}{\partial t}}_{Damping} \quad (1)$$

γ is the gyro-magnetic ratio, $\gamma = \frac{2\mu_s}{\hbar}$, α is the damping constant and $\vec{H}_{eff}$ is the effective magnetic field.

The first part in the equation (1) indicates a precession torque which responsible for the rotational movement of an electron around $\vec{H}_{eff}$ the as shown in Figure 2.4 and a force exerted on the electron due to $\vec{H}_{eff}$ is known as damping torque, it is second term in the equation (1) and it is shown in Figure 2.4.

Under the influence of the flux of electrons a net moment will be generated that will produce an additional spin torque to modify the equation (1) written below and shown in Figure 2.4.

$$\frac{\partial \vec{m}}{\partial t} = \underbrace{-|\gamma|\left(\vec{m} \times \overrightarrow{H_{eff}}\right)}_{Precession} + \underbrace{\alpha \vec{m} \times \frac{\partial \vec{m}}{\partial t}}_{Damping} + \overrightarrow{STT} \quad (2)$$

$$\overrightarrow{STT} = |\gamma|\beta\left(\underbrace{\hat{m} \times \varepsilon \hat{m} \times \widehat{m_p}}_{1} + \underbrace{\acute{\varepsilon} \hat{m} \times \widehat{m_p}}_{2}\right) \quad (3)$$

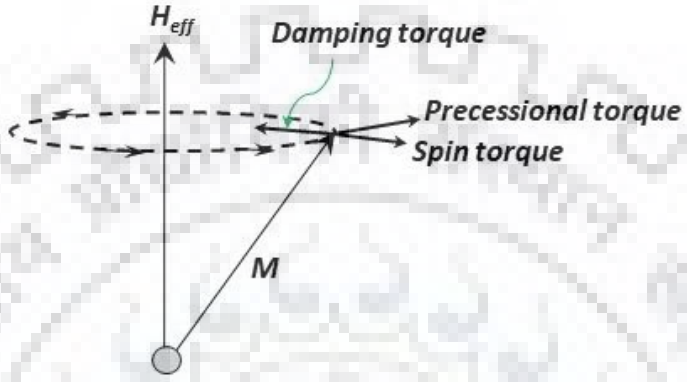


Figure 2.4 Precession, Spin, and Damping torque of magnetic moment (*M*) around a magnetic field (H_{eff})

The first term in equation (3) is in-plane spin torque that is similar to the damping torque. This torque is due to the interaction of injected spin-polarized electrons and bounded electrons in the ferromagnetic layer. The second term denotes the exchange interaction between ferromagnetic layers termed as 'field-like' spin torque. It is perpendicular to both the layers. In most of the cases, the value of field like torque is neglected [16]. The magnitude of the spin torque in comparison with a threshold value decides the change in the magnetization of the target layer.

2.4 Spin Valves

It is a simplest device that has used the spin property of an electron. It basically has three layers in the stack form. Two of them are ferromagnetic (FM) and one is sandwiched between them i.e. (non-magnetic) NM layer as shown in Figure 2.5. Two FM layers are not having the same kind of property. One of them is the free layer (FL) and other is called pinned layer (PL). The FL magnetization moment can be easily changed because it has low coercivity. While the PL magnetization moment can't be changed due to high coercivity [16]. It is pinned by using the stack of anti-ferromagnetic layers like FeMn or IrMn and ferromagnetic layer. The spin orientation in these layers expresses about the logic '0' and logic '1'. If the relative magnetization moment of the MTJs ferromagnetic layers is in parallel, in this case

spin valve have low resistance and conversely, in the case of anti-parallel spin valve have high resistance. The magnetization moment of the MTJs free layer can be changed with the effect of STT. This property utilizes to implements the hybrid logic circuits.

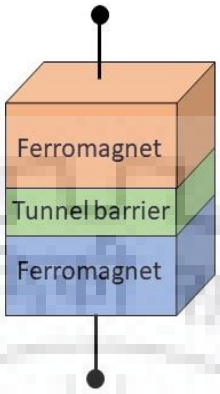


Figure 2.5 Spin Valve

2.5 Giant Magnetoresistance (GMR)

GMR is the phenomenon of variation in relative resistance due to magnetization of ferromagnetic layers detached by a spacer. The resistance depends upon the magnetization orientation in FM layer when the magnetization orientation in FM layer is parallel then we can say the resistance is low it is not depending on spin up channel or spin down channel in both the cases resistance value is low for parallel orientation as represent in Figure 2.6.

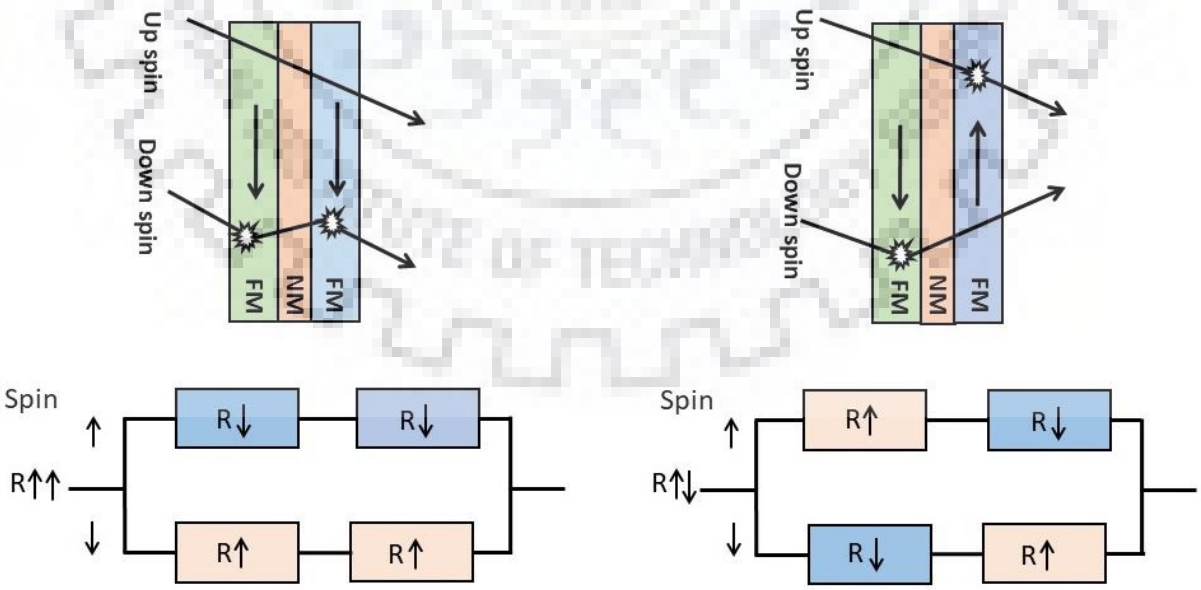


Figure 2.6 GMR effect and two channel Mott Model of spin valve

For parallel magnetization, resistance is low because tunneling probability is high as both FM layers have an equal density of states (DOS) for the up spin and down spin of the electrons. On the other hand, anti-parallel magnetization resistance is high because tunneling probability is low for the up spin and down spin electrons in FM layers.

$$GMR = \frac{R_{AP} - R_P}{R_P}$$

$$R_p = \frac{R_{up} + R_{down}}{R_{up} \times R_{down}}$$

$$R_{AP} = \frac{R_{up} + R_{down}}{2}$$

Here, R_{up}, R_{down} are the resistance offered to spin-up/down electrons flowing through the spin valve, when the magnetization orientation in FM layer is anti-parallel then we can say the resistance is high because it scattered both spin up and spin down as shown in Figure 2.6.
GMR divide in major two parts: i. Current in plane (CIP) GMR ii. Current perpendicular to the plane (CPP) GMR [11]. In CIP GMR, the magnetization in ferromagnetic layers (FM) are not aligned in absence of magnetic field. The flow of current is in the plane of multi layers and in CPP GMR, the direction of current is perpendicular to the surface of ferromagnetic layers. When the magnetic moments are aligned, electrons can easily pass through one of the spin channels.

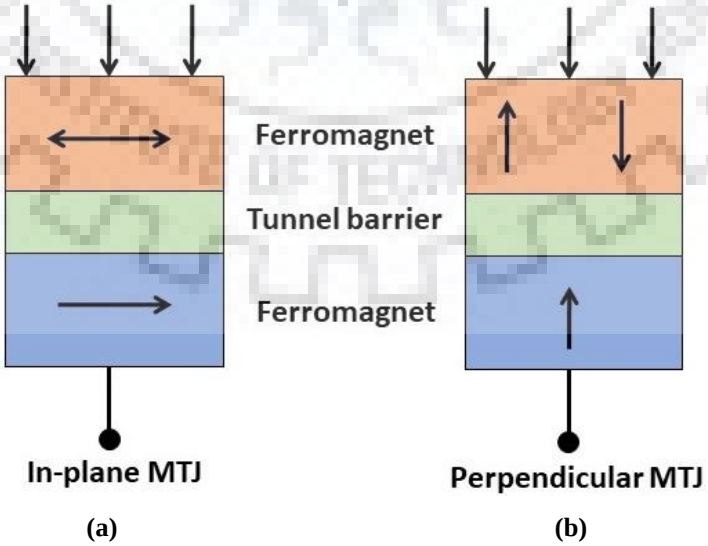


Figure 2.7 (a) Current in plane GMR (b) Current in perpendicular to the plane GMR

CHAPTER3

STT- MRAM

3.1 Magnetic Tunnel Junction (MTJ)

Magnetic Tunnel Junction (MTJ) is a most fundamental spin-based device that utilizes the quantum mechanical spin property of the charge carrier for storing the information [20]. It is hetero-junction use spin dependent quantum-mechanical tunneling. They also have the important magneto-resistance property. The low magneto-resistance ratios (MR) and low resistance shown in Table 3.1 [23].

Table 3.1 The low magneto-resistance ratios(MR) and low resistance.

	GMR	**TMR**
Resistance	10ohm	>100ohm
MR Ratio	<100%	>100%

If spin valves use the insulator spacer in between the two ferromagnetic layers that gives the tunneling magneto-resistance (TMR) which is introduce by the julliere in 1975 [19] but if spin valve using a non-magnetic metal spacer layer, then it gives GMR i.e introduce by Fert and Grunberg [21] - [22]. A non-magnetic tunnel barrier in MTJs is made up of oxides such as MgO, AlOx, TiOx. Due to addition of a layer between the two ferromagnetic layer i.e. tunnel barrier (TB), MTJs provided a tremendous boost up of magneto-resistance ratio. The high value of TMR provides better distinguished between the parallel (P) and anti-parallel (AP) orientation of ferromagnetic layer magnetization. In FM/I/FM layer MTJ, the magnetization orientation of one of the FM layers is fixed which is called the fixed or pinned layer (FL or PL) and the other FM layer whose magnetization orientation can be altered is called free layer (FL). The resistance value of the MTJs is low/high while, the FM electrodes have parallel/antiparallel magnetization orientation shown in Figure 3.1. We can represent the TMR mathematically as describe:

$$TMR = \frac{R_{AP} - R_P}{R_P}$$

Here, the R_{AP} and R_P are the resistances of MTJ in AP and P configurations.

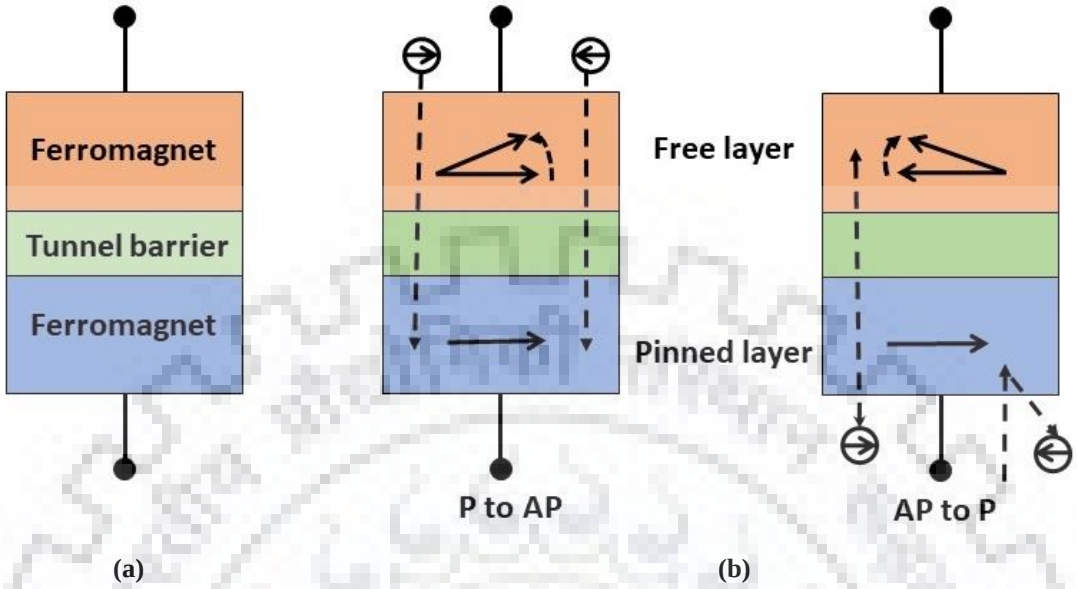


Figure 3.1 (a) MTJ Cell (b) Switching P-AP or AP-P

In 2001, Butler *et al.* [24], Mathon and Umerski [25] theoretically predicted the chance of achieving a remarkably high TMR ratio for Fe/MgO/Fe in fully crystallized (001) MTJ structure. Thereafter, several research groups started focusing on MTJs with MgO tunnel barrier and reported fabulous upgrading in TMR ratios obtained at room temperature (300K), i.e. 230% and an incredible 604% in [26]. TMR mainly determined by the type of the FM electrodes, TB material, fabrication method and the quality of the interfaces.

3.2 STT-MRAM

STT MRAMs is the main contestant for universal memory technology because it consists all the property like high density, high speed, low power memories, high endurance, and non-volatility. STT-MRAM use the spin-transfer torque (STT) effect for write operation and TMR effect for read operation. The MTJ is the most fundamental device to store the data in STT-MRAMs. They are also known with name non-volatile RAM (NVRAM). STT-MRAMs are compatible with CMOS fabrication as shown in Figure 3.2. However, STT-MRAM consumes high write energy and takes the large on-chip area due to large driver transistor sizes [27]. Thus, limits the wide use of STT-MRAM for logic applications. In spite of this STT-MRAM is requires the high write current because of that there is a chance of the oxide breakdown and undesirable switching in MTJ device.

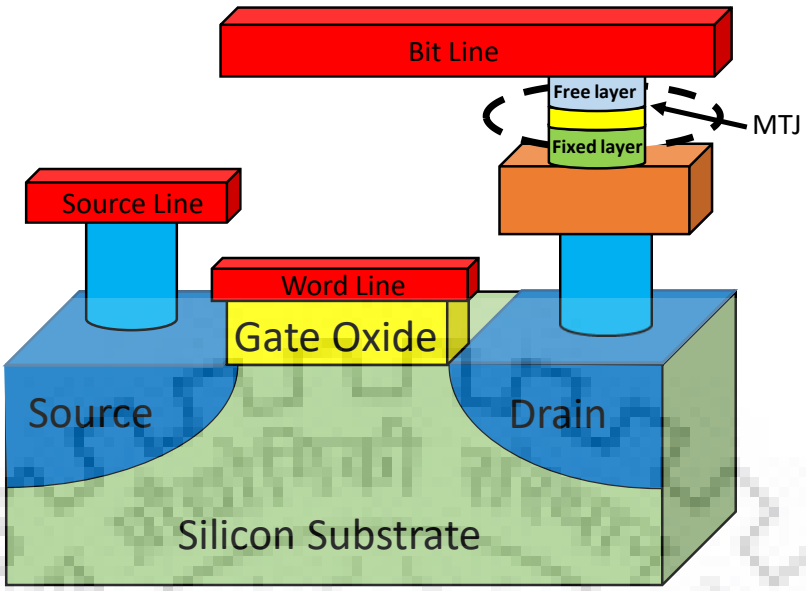


Figure 3.2 Schematic of 1T STT-MRAM cell

3.2.1 STT-MRAM Cell

To overcome the SCE and power consumption issues, STT-MRAM is introduced. Each STT-MRAM cell consists a MTJ as a storage device and a *n*MOS transistor as a select/access device [16]. The *n*MOS transistor provides cell selection through a gate word line (WL) and the bit line (BL) is connected to the free layer of MTJ and the select line (SL) is attached to the source terminal of *n*MOS transistor [28] as represent in Figure 3.3.

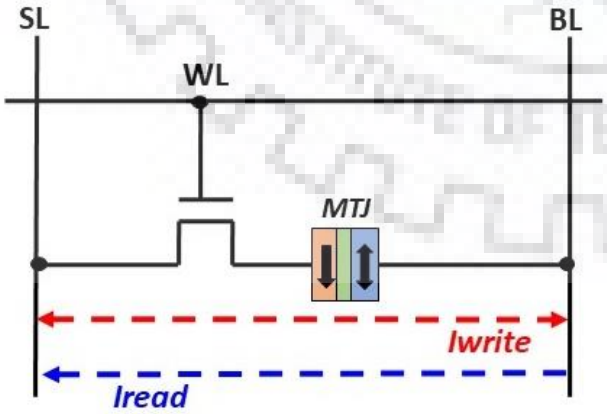


Table 3.2 Read/Write operation of STT-MRAM

	WRITE '1'('0')	READ
Word Line (WL)	V_{DD}	V_{DD}
Bit Line (BL)	$0(V_{DD})$	V_{DD}
Select Line (SL)	$V_{DD}(0)$	0

Figure 3.3 Read / Write operation of a STT-MRAM cell

3.2.2 Write Mechanism

MTJ device of STT-MRAM cell have two switching resistive state on the basis of orientation of magnetization i.e. parallel and anti-parallel. The write operation is based on the STT mechanism; where, spin-polarized electrons interact with the free layer electrons. The spin-polarized electrons convey STT by the exchange of spin angular momentum with the magnetization of the FL. For anti-parallel (AP) to parallel (P) switching, a current is flowing from bit line (BL) to select line (SL) through *n*MOS represent in Figure 3.4.

The electron is moving in the direction of SL to BL because the BL line connected to the higher voltage in comparison to the SL. The pinned layer act as spin filter because it generates majority spin. STT is exerting on the magnetization of free layer by the electrons which passed through the tunnel barrier. Now the state of free layer is same as the pinned layer or else we can also say that anti-parallel changes into the parallel.

During this operation, the electron is moving from BL to SL because the BL line connected to the lower voltage in comparison to the SL, after passing through TB electrons are attain the magnetic moment in the direction of free FL of MTJ. After getting to the pinned layer, the electron only pass which have spin-polarization in the direction of pinned layer magnetization is able to pass whereas, other electrons are returned back to the free layer (FL). Now final magnetization state depends on returned electrons, these electrons are applying spin transfer torque (STT) on the magnetization moment of free layer.

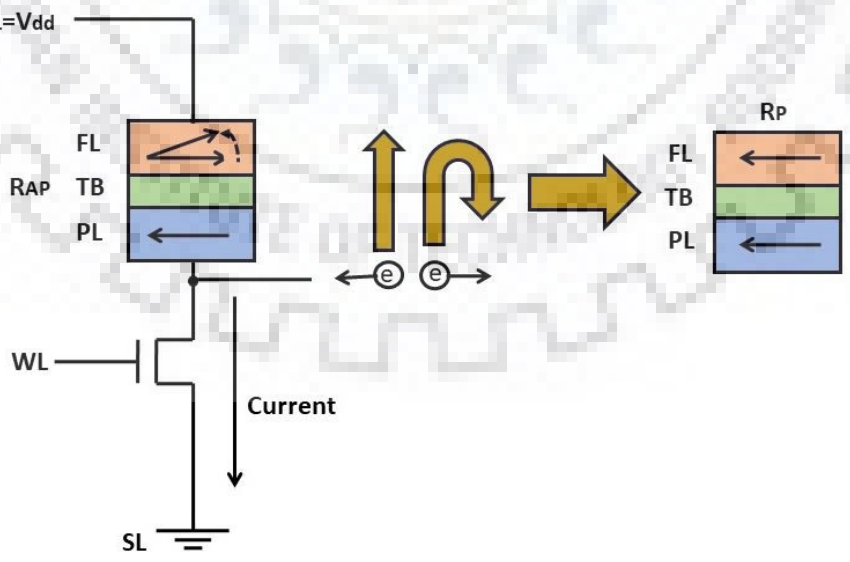


Figure 3.4 A write operation (AP to P switching) in a STT-MRAM cell.

Due to the lesser number of reflected electrons during P to AP switching, MTJ exhibits an asymmetric behaviour of the threshold switching current density as the AP to P switching current is smaller than the P to AP current requirement.

For Parallel to Anti Parallel transition of magnetization, current is traversed from select line (SL) to bit line (BL) as shown in Figure 3.5. In this case the electron is flowing in the direction of FL to PL of MTJ.

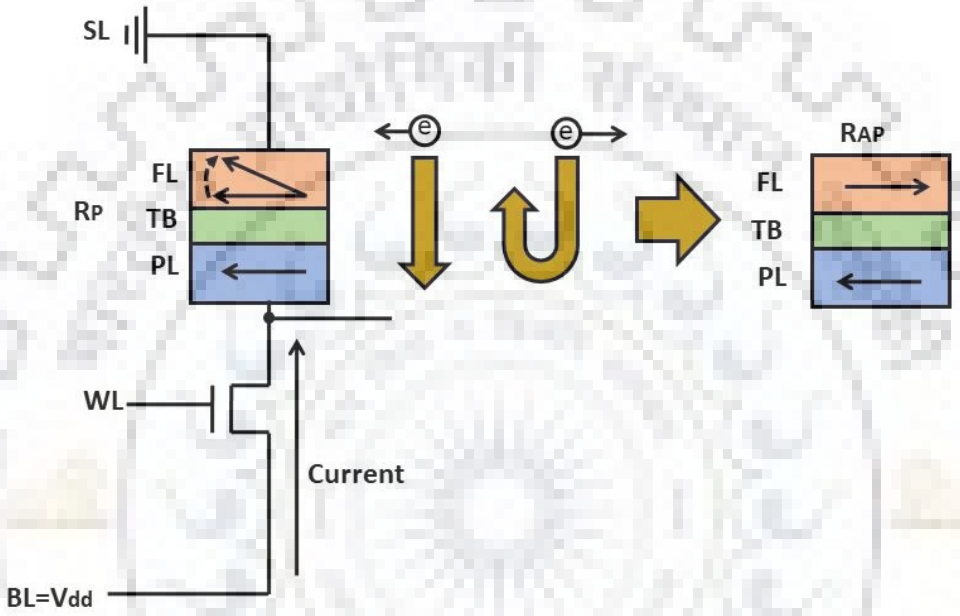


Figure 3.5 A Write operation (P to AP switching) of a STT MRAM cell.

3.2.3 Read Mechanism

The bit stored in the STT MRAM cell can be read by applying a read voltage (V_R) between BL and SL, while, the desired cell is selected using WL=V_{DD}. The parallelizing read scheme connects the BL=V_R and SL=0 in the read operation whereas, the anti-parallelizing read is performed with SL=V_R and BL=0.

An optimum value of V_R is obtained by considering the deprivation in *TMR* along with the MTJ bias voltage and the difference in the read current value for the P and AP states. To read the information read current is compared with reference current, the margin of the difference of the cell current representing logic '0' and logic '1' should be large enough to be distinguished.

Figure 3.6 (c) shows the basic schematic of a simple read circuitry. During the read operation, a small current, I_{read}, carefully chosen to avoid read-disturbance, is fed through the cell. The

voltage (V_x) that develops across the device is compared against a reference voltage (V_{ref}) that is ideally midway between the two-possible level of the input voltages. A sense amplifier (SA) is required to read the voltage difference [29].

The procedure of parallel and anti-parallel read operation is done by calibrate the voltage difference between the R_{ref} and R_{MTJ} by SA (sense amplifier) represent in Figure 3.5(a) and (b), (c).

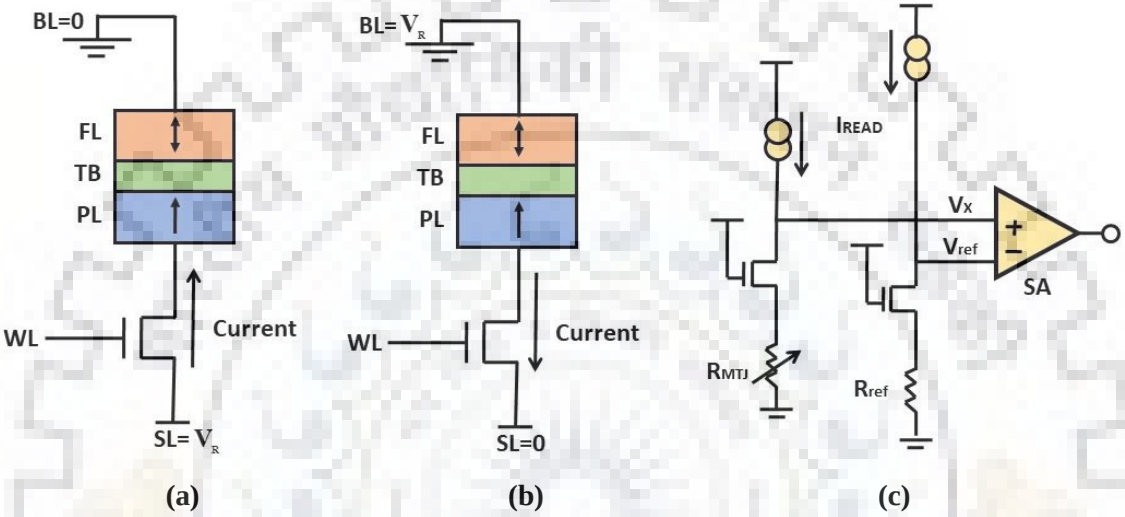


Figure 3.6: (a) STT-MRAM cell with (a) parallel (b) anti-parallel read operations (c) Schematic of a conventional read scheme.

CHAPTER4

DIFFERENTIAL SPIN HALL MRAM

4.1 Spin Orbit Torque(SOT)

MTJs a best contender to proficiently implement a hybrid MTJ/CMOS technology. Two terminal MTJs based on STT switching have many attractive properties for the circuit designer. Despite the attractive properties of the STT devices, there are main two issues 1. writing/reading path is common so that there is a chance of oxide breakdown, 2. reliability. So in order to achieve high speed for both write and read is challenging task with STT based MTJ.

A three-terminal MTJ based on the spin-orbit torque (SOT) switching mechanism is a best way for sorting out the reading and the writing paths. The STT-MRAM consumes large energy and takes large on-chip area due large driver transistors [30]. STT-MRAM required high write current that reduce the reliability and increase the chances of tunnel barrier breakdown in MTJs. In STT-MRAM for reading and writing the logic a common path through oxide is follow. To deteriorate these issues, the new switching technique SHE is used. In this switching technique the read and write path is decoupled [31]. SHE is induced the spin current in the heavy metal (HM). It provides the more than 100% spin injection efficiency and low resistance track [14] because of that SOT-MRAM provides fast and efficient switching.

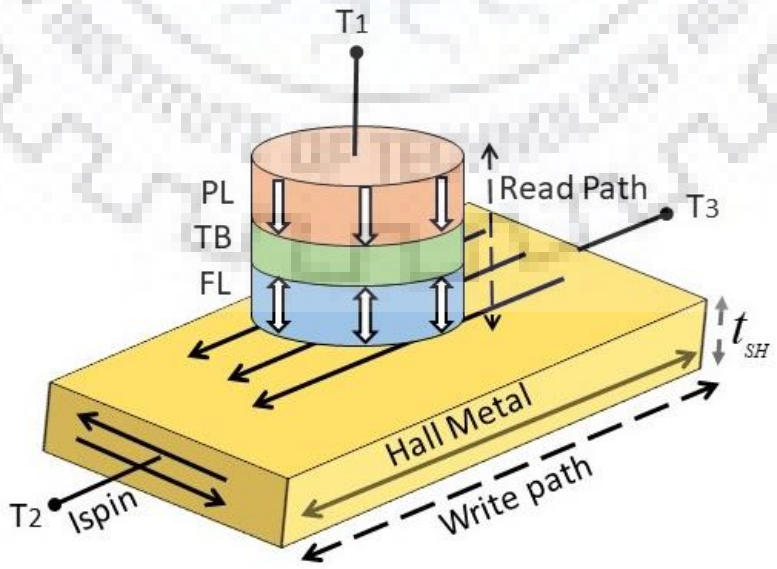


Figure 4.1 SHE-MRAM

In SHE-MRAM device the MTJ's free layer is mounted on the surface of non-magnetic Hall metal (HM) such as tantalum (Ta) as shown in Figure 4.1. Due to SHE or Rashba effect spin current is generates in the perpendicular direction of the electrical charge current when the electrical charge current is flowing through the HM [30]. The spin current start applying the STT on the magnetization of FL of MTJ i.e. mounted on the HM surface in order to change the magnetization state of MTJ.

The spin injection efficiency (i.e. I_{spin} / I_{charge}) of HM in SHE-MRAM is high due to this it requires small switching current [32], [33] in compared to STT-MRAM.

4.1.1 Read Mechanism

The 2T SOT-MRAM bit cell as shown in Figure 4.2 have only two access *n*MOS transistor. The control signals of bit cell are Read Word-Line (*RWL*), Write Word-Line (*WWL*), Read Bit-Line (*RBL*), Write Bit-Line (*WBL*), and the shared Source Line (*SL*) [34].

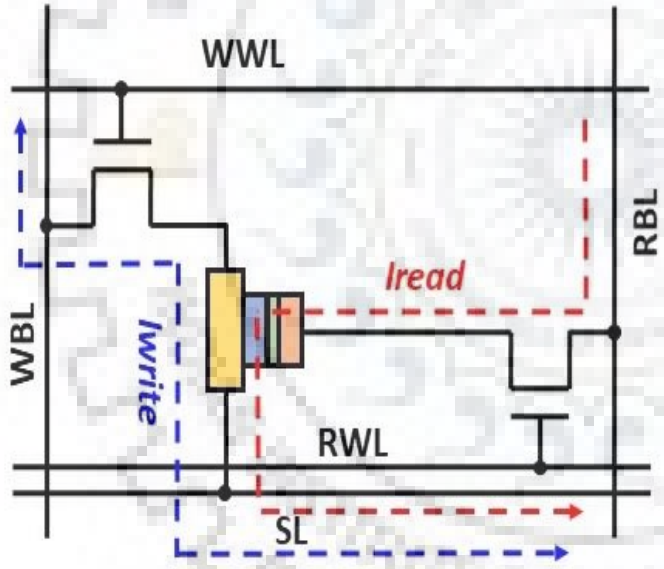


Table 4.1 Read/Write operation of SHE-MRAM

	WRITE '1'('0')	**READ**
WWL	V_{DD}	0
RWL	0	V_{DD}
RBL	0	I_{READ}
WBL	V_+ / V_-	0
SL	0	0

Figure 4.2 Read / Write operation of a SHE-MRAM cell

For reading the data from SOT-MRAM RWL signal kept at high (V_{DD}) voltage in order to ON the read access *n*MOS transistor. The I_{READ} current start flowing through SOT-MTJ and access transistor because of this current a voltage generates across the *RBL* line i.e. called

VREAD. This voltage is varying according to variation in SOT-MTJ resistance i.e. sense by sense amplifier.

4.1.2 Write Mechanism

For writing a logic in SOT-MRAM *WWL* control signal kept at high (V_{DD}) voltage in order to turn ON the write access *n*MOS transistor. After that according to the condition of write logic '1' or logic '0' the *WBL* connected to positive (V_+) or negative(V-) voltage and *SL* line connected to ground.

4.2 Differential Spin Hall MRAM

The STT-based circuits consume high energy while writing the logic and acquire large on chip area due to large driver transistors. The DSHE-MRAM offers simultaneous switching of two MTJs using spin Hall effect and generate complementary logic output. It consists of two MTJs and a spin HM like in SOT-MRAM as shown in Figure 4.1. The FLs layers of the MTJ contact with spin hall metal and SHM has very low resistivity because of that DSHE assisted MTJ requires lesser write current.

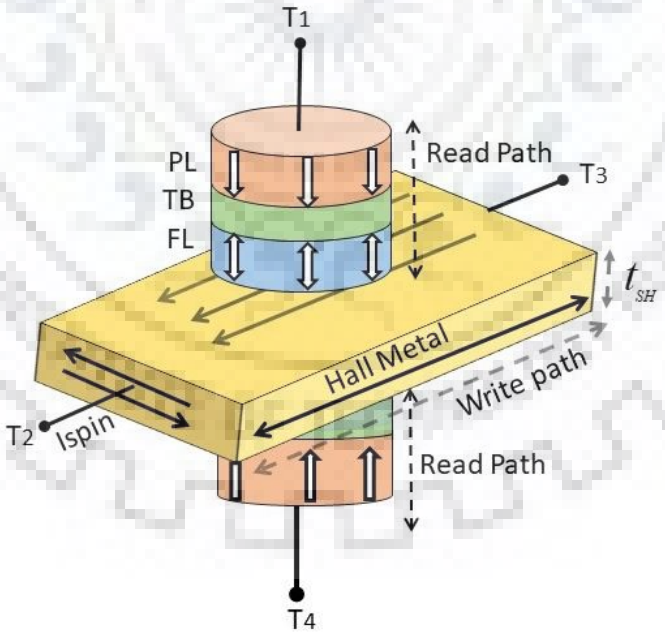


Figure 4.3 DSH-MRAM

The magnetization of FLs layer represents the stored information. The pinned layer magnetization is fixed. The spin coupling between spin orbit and electron spin interaction in

SHM deflects the spins of FLs to +z or -z direction. In DSH-MRAM writing both logic '1' and logic '0' bits at the same instant of time because of that we can say that writing energy required previously to write the logic '1' or logic '0' is same in DSH case to write both logic '1' and logic '0'. In case of read operation, we get the read value which actually depends on the state of magnetization (i.e. parallel and antiparallel).

4.2.1 Read Mechanism

In case of DSH-MRAM requires three access transistors for reading/writing the cell [35]. For reading the data from DSH-MRAM *RWL* signal kept at high (V_{DD}) voltage in order to ON the read access *n*MOS transistor. The I_{READ1} or I_{READ2} current start flowing through MTJs of DSH and access transistor because of these currents a voltage generates across the *RBL* line i.e. called V_{READ}. This voltage is varying according to variation in resistance of MTJs of DSH i.e. sense by sense amplifier.

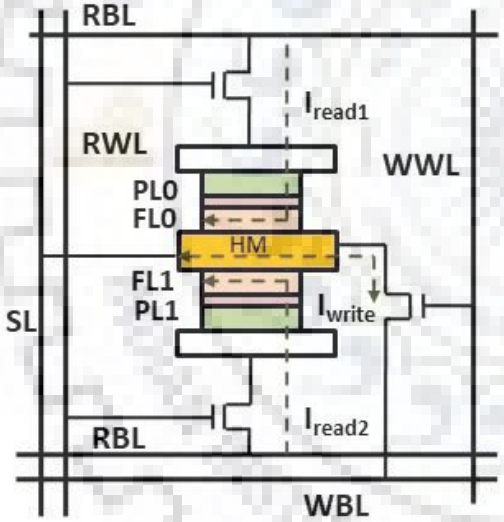


Table 4.2 Read/Write operation of DSH-MRAM

	WRITE '1'('0')	**READ**
WWL	V_{DD}	0
RWL	0	V_{DD}
RBL	0	I_{READ1}/I_{READ1}
SL	0	0
WBL	V_+/V_-	0

Figure 4.4 Read / Write operation of DSH-MRAM cell

4.2.2 Write Mechanism

For writing a logic in DSH-MRAM *WWL* control signal kept at high (V_{DD}) voltage in order to turn ON the write access *n*MOS transistor. Then according to the write logic '1' or logic '0' *WBL* connected to positive (V_+) or negative(V_-) voltage and *SL* line connected to ground.

4.3 STT versus SHE switching technique

Spintronics technology is used as an alternative to CMOS technology as it is having comparatively low amount of power dissipation, non-volatility, high density and high endurance. MTJ is the basic fundamental spin based device that stores data in form of spin instead of charge. Two mechanisms i.e. spin transfer torque (STT) and spin Hall effect (SHE) are used to alter the magnetization moment of MTJ. STT is most suitable technique to replace MOSFET technology in future but due to common path for reading and writing its reliability is low. In order to achieve high reliability, SHE switching technique is used as in SHE read and write path is decoupled.

Table 4.2 Comparison of STT MRAM and SHE PMTJ

STT MRAM	**SHE PMTJ**
Same read and write path.	Separate read and write path.
Low power consumption.	Reduce write energy.
Higher write energy then SRAM.	Avoid barrier breakdown.
Fast in read but slow write operation.	Enhance the endurance and reliability.
High endurance.	Writing scheme is faster.

CHAPTER 5

SIMULATION RESULTS OF STT-MRAM AND DSHE-MRAM

5.1 Simulation Set up and Model parameter

The simulations are done with HSPICE using 45-nm standard CMOS design kit at 1.2 supply voltage and Verilog-A models of STT-MRAM [36] and DSHE-MRAM [14]. Device parameters for STT and DSHE are represent in Table 5.1 and 5.2.

Table 5.1 STT-MRAM device parameters

Parameters	Value
MTJ surface area (nm^2)	40x40
Oxide barrier thickness (nm)	0.85
Write voltage (V)	1.5
MTJ resistance (KΩ)	3.9(P), 7.9(AP)
Free layer thickness (nm)	1.3
CMOS Technology	45nm

Table 5.2 DSHE-MRAM device parameters

Parameters	Value
Heavy metal volume (nm^3)	50x40x3
Heavy metal resistance (Ω)	833
MTJ surface area (nm^2)	40x40
Oxide barrier thickness (nm)	0.85
Write voltage (V)	0.4
MTJ resistance (KΩ)	6.14(P), 14.1(AP)
Free layer thickness (nm)	1.3
CMOS Technology	45nm

Spin orbital torque (SOT) device is a popular among the researchers and in industries because it is fast and dissipates low energy in comparison to two terminal STT based MTJs. The read and write path is decoupled in the SOT device because of that it is more reliable as the write current is not flow through TB. So chances of barrier breakdown are reduced. The internal

structure is used in Verilog-A model of SOT-MRAM [37] shown in Figure 5.1. Here, R_{SHM} is resistance of heavy metal (Ta) and R_{MTJ} is resistance of MTJs.

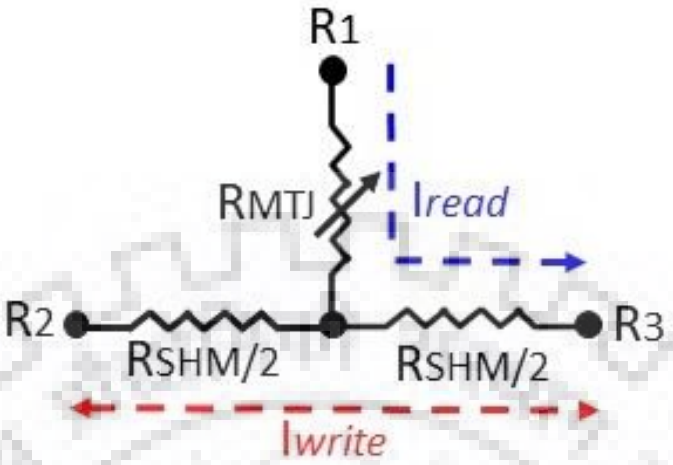


Figure 5.1 Internal structure of SOT-MRAM used in modelling

The differential spin Hall effect (DSHE)-MRAM is extended version of SOT-MRAM. The DSH-MRAM is store complimentary bits simultaneously by using same power, SOT able to stores only one bit. The internal structure is used in Verilog-A model of DSH-MRAM represent in Figure 5.2.

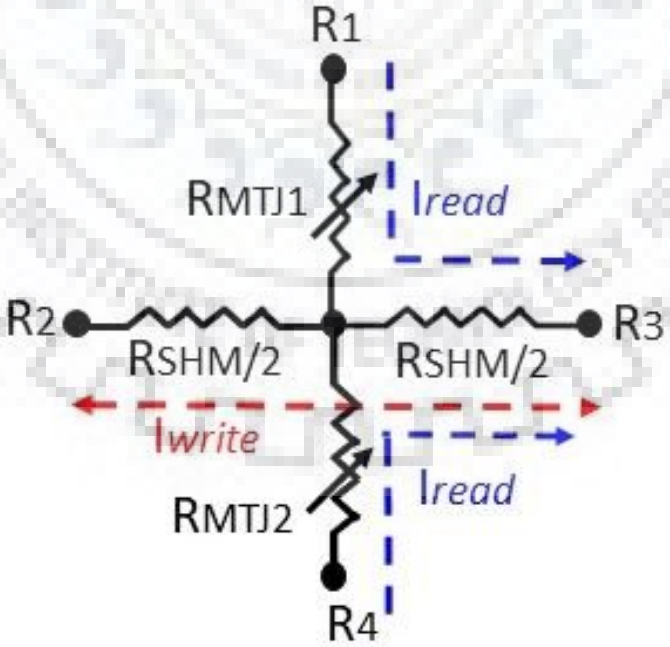


Figure 5.2 Internal structure of DSH-MRAM used in modelling

5.2 Analysis of STT-MRAM

In STT-MRAM the MTJ is a storing device. The resistance value of the MTJs depends upon the relative alignment of the magnetization moment of FM layers of the MTJ. If the magnetization orientation is in parallel direction, then the resistance of MTJ is low. Conversely, if the magnetization orientation is in anti-parallel direction then the resistance of MTJ high. In order to observe the resistance variation of the MTJ. The voltage source (Vmtj) is applied as shown in Figure 5.3. If the Vmtj is positive the electrons are flowing from PL to FL. If the current is greater the critical current, then electrons applied the STT to orient the magnetization in parallel direction. However, if the Vmtj is negative the electrons are flowing from FL to PL. In case of if the critical current is lower than the current flowing through circuit due to Vmtj source, then electrons applied the STT to orient the magnetization in anti-parallel direction.

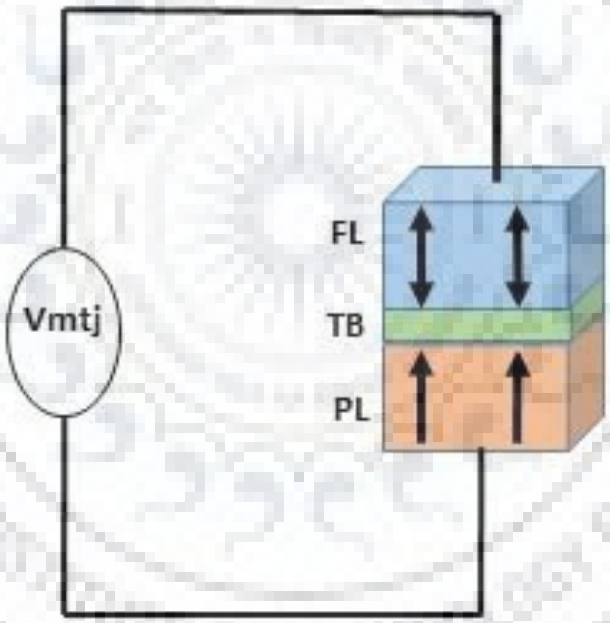


Figure 5.3 MTJ with applied voltage

In simulation the applied voltage (Vmtj) is vary from -1V to 1V as shown in Figure 5.4. It shows that when applied voltage is positive (above the critical voltage) then orientation of magnetization changes from P to AP. Conversely, when applied voltage is negative (above the critical voltage) then orientation change from Antiparallel to parallel. The value of resistance varies in between the 3.9K (P) to 7.9K (AP). So it is easy to distinguish the two state of resistance.

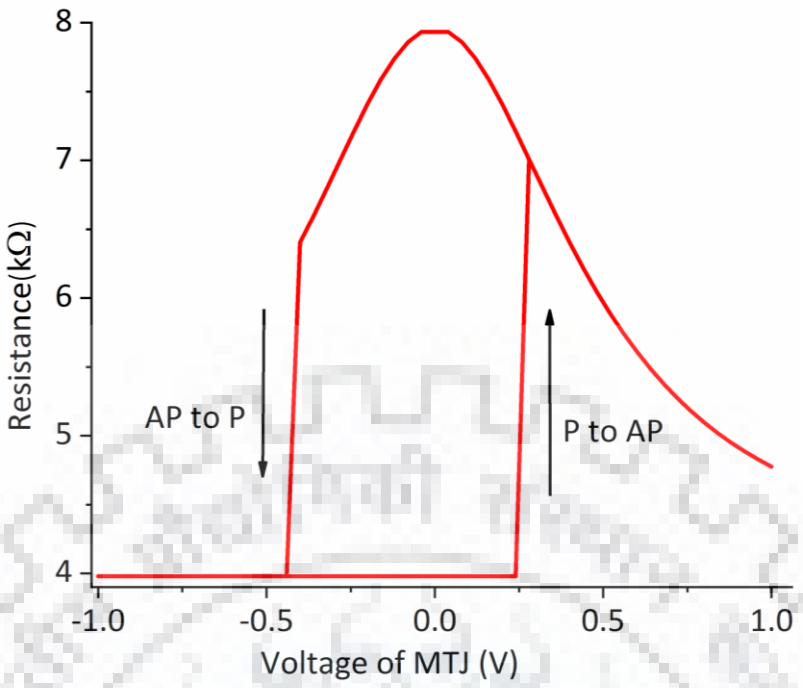


Figure 5.4 Simulated R-V hysteresis loop of a MTJ

The critical switching voltage (above of that state change) for anti-parallel critical switching voltage is 360mV and for the parallel 200mV as represent in Figure 5.5.

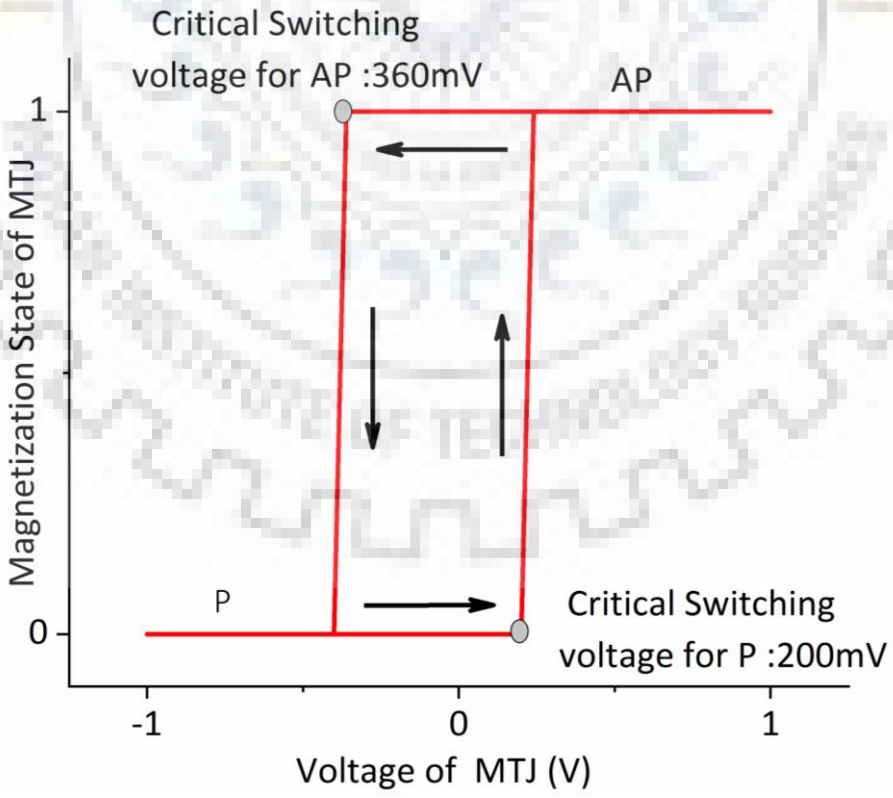


Figure 5.5 Magnetization states of a MTJ for STT-MRAM

The main sources of process variations in STT-MRAM is cross-sectional area of MTJs and tunneling oxide thickness (t_{ox}) [38]. The read and write failure can be happen because of these process variation. The resistance of MTJs is varies inversely proportional to the cross-sectional area of MTJs and the resistance of MTJs varies exponentially with tunnel oxide thickness of the MTJs as shown in Figure 5.6, 5.7.

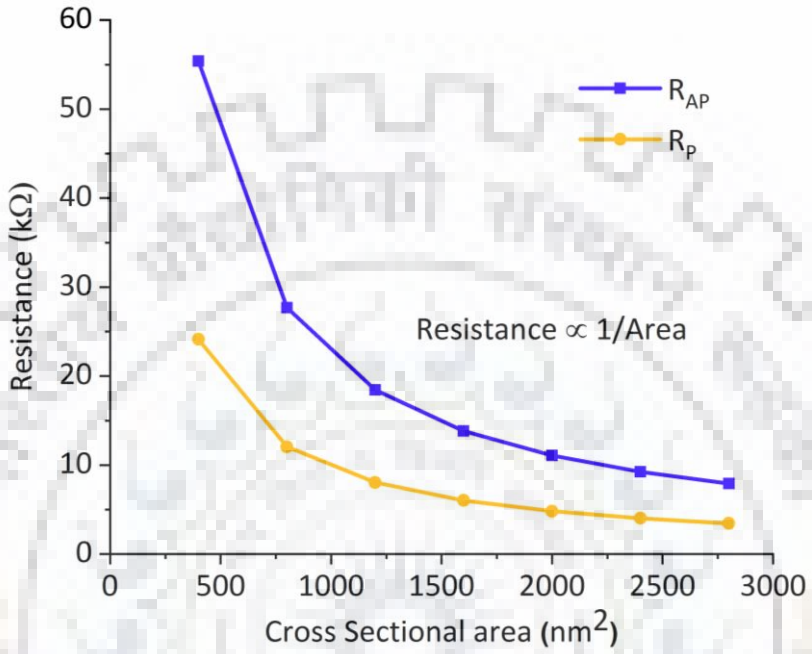


Figure 5.6 Resistance variation with cross sectional area of DSHE-MRAM

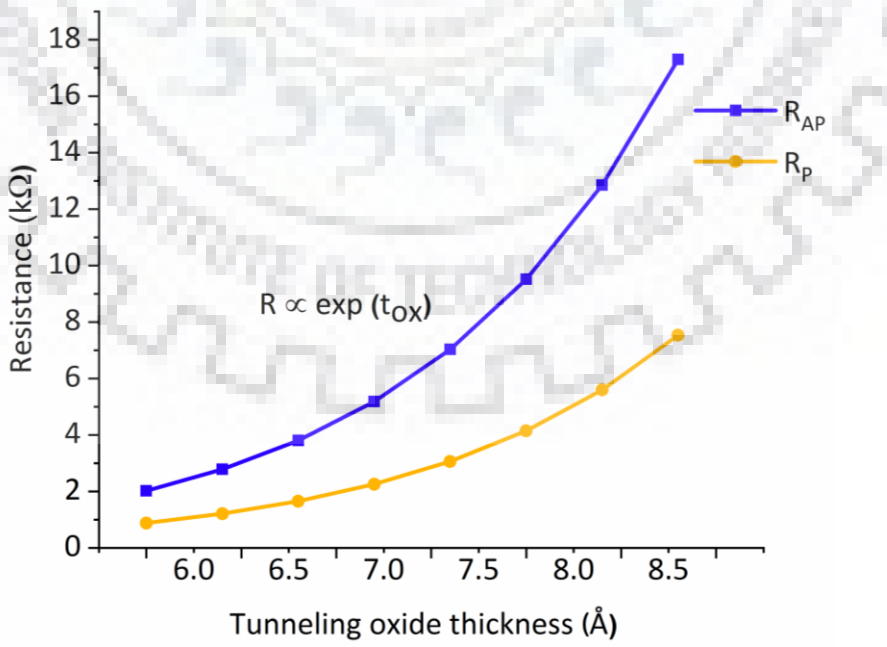


Figure 5.7 Resistance variation with tunneling oxide thickness of DSHE-MRAM

5.2.1 STT-MRAM Write Circuit

The STT-MRAM based circuits utilize four *n*MOS transistors for writing the MTJs [36] as shown in Figure 5.8. While, the DSHE circuits uses only two *n*MOS transistors as shown in Figure 6(b). In STT write circuit, when $In1$ is high the current is flowing in the direction of MTJ0 to MTJ1 as result of that logic '0' write in MTJ0 and logic '1' in MTJ1. Conversely, when $\overline{In1}$ is high current start flowing in opposite direction and as a result logic '1' write in MTJ0 and logic '0' write in MTJ1

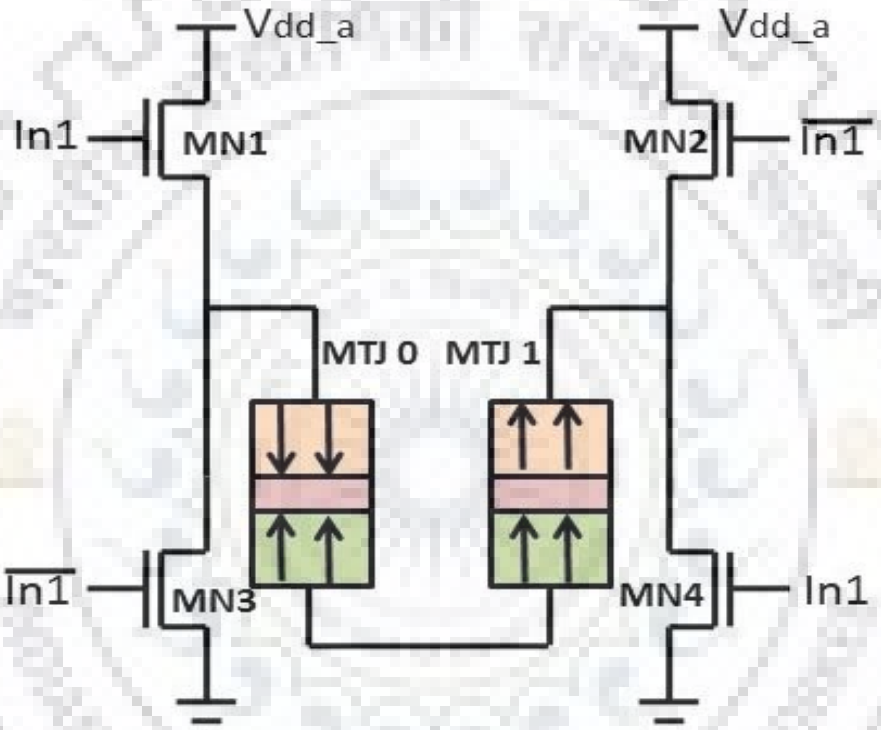


Figure 5.8 Write circuit for STT-MRAM

The writing of logic in MTJ cell can be done in consecutive cock pulse. In case of STT-MRAM power supply for write circuit (Vdd_a) is 1.5 V and $In1$, $\overline{In1}$ requires 20 ns pulse width for writing the MTJs as represent in Figure 5.9. The STT-MRAM write circuit power consumption gives significant value in overall power calculation of a logic circuit. The energy consumed per bit by the write circuit of STT-MRAM is 115.7 fJ.

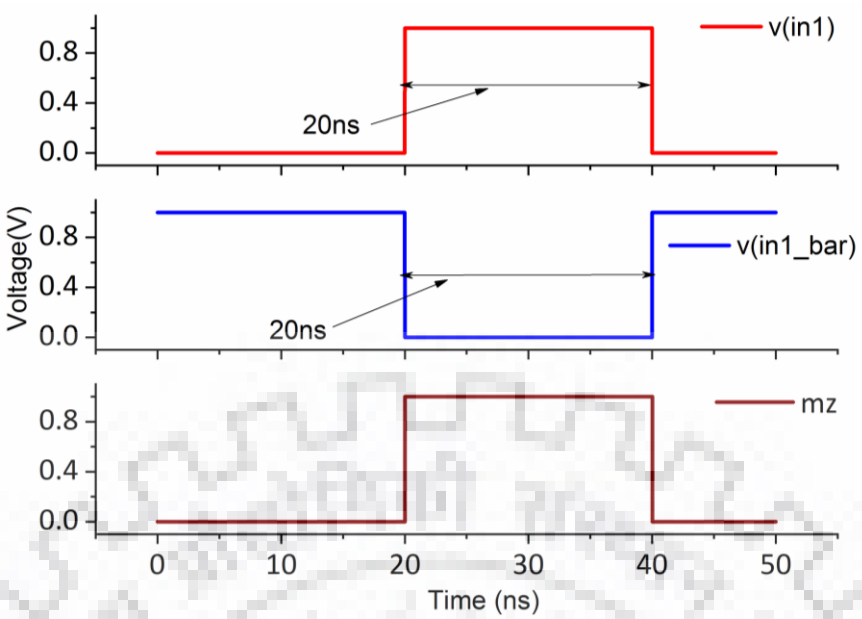


Figure 5.9 Switching for STT-MRAM

5.2.2 STT-MRAM Read Circuit

Pre charge sense amplifier (PCSA) is used to read the logic stored in MTJs cell [36]. The PCSA circuit contributes seven transistors (four *p*MOS, three *n*MOS) and two MTJs as shown in Figure 5.10.

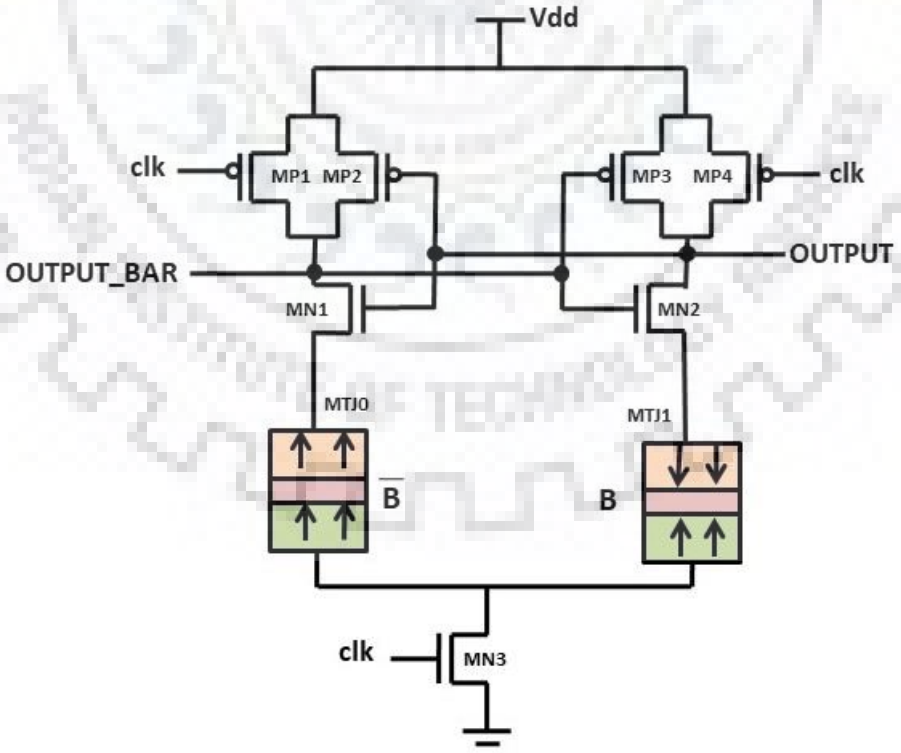


Figure 5.10 STT-MRAM based PCSA

PCSA perform in two phase: 1. Precharge Phase 2. Evalution Phase. In precharge phase when clk=0 the output and output_bar both charge up to Vdd through MP4, MP1 transistor respectively. The MP2, MP3, MN1 and MN2 are the two inverter connected in the form of feedback. In evalution phase when clk=1, the pull down transistor MN3 is ON. This transistor gives the discharging path to the minimum resistance path. If the MTJ0 is at lower resistance, then the OUTPUT_BAR is discharge to zero. Likewise, if the MTJ1 is at lower resistance then the OUTPUT is discharged to ground as shown in Figure 5.11. The sensing delay for STT-MRAM is 68.7 ps

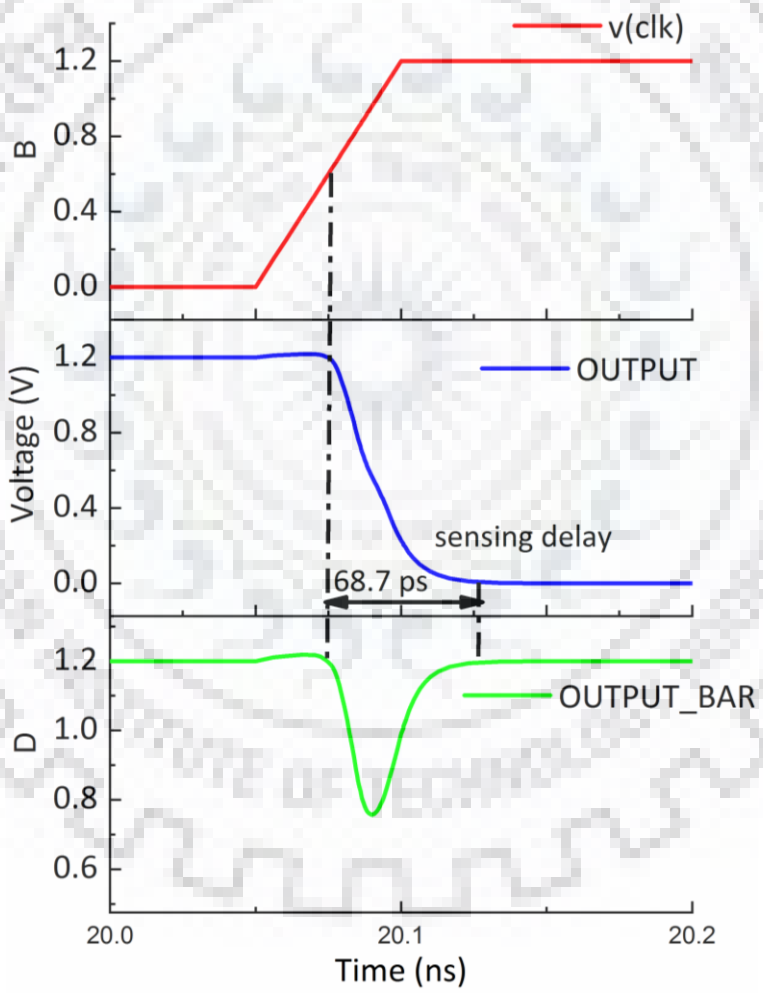


Figure 5.11 Simulation Result of STT-MRAM based PCSA

5.2.3 Magnetization of STT-MRAM

The switching time is the time taken to change the state from AP to P (P to AP) by altering the magnetization orientation of the MTJs layer. If it is sufficiently low, it means that device is fast. The switching time (t_{sw}) for STT-MRAM is 3 ns as represent in Figure 5.12.

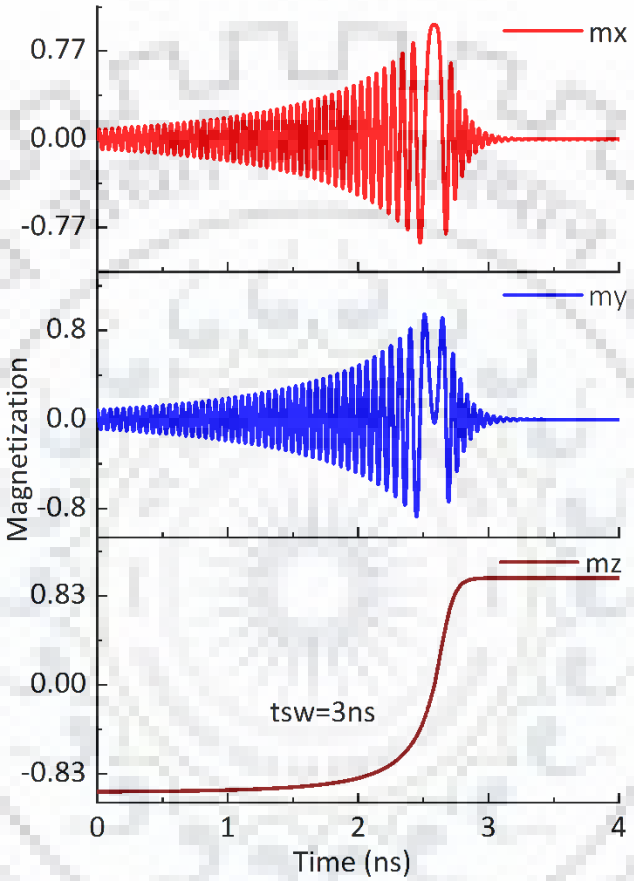


Figure 5.12 Magnetization timing diagram of STT-MRAM

5.3 Analysis of DSH-MRAM

The four terminal device DSH consists of HM layered in between two PMTJs as shown in Figure 5.13. DSH store two complimentary bits simultaneously at very low voltage. It decreases the resistance of write path [14].

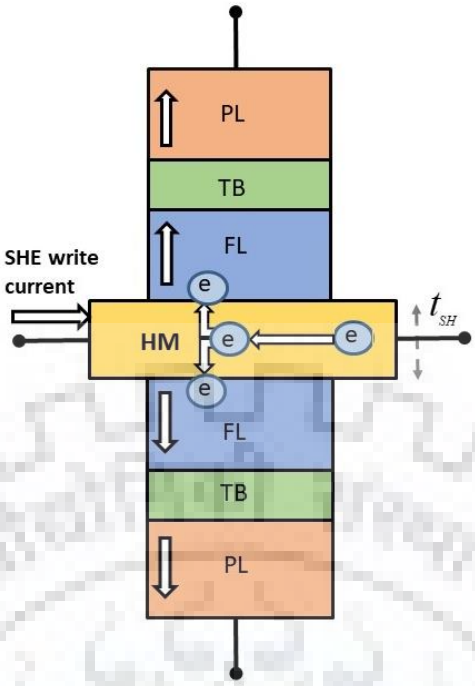


Figure 5.13 DSH-MRAM structure

5.3.1 DSH-MRAM Write Circuit

The DSH-MRAM write circuit consists only two *n*MOS transistors as shown in Figure 5.14. In DSH-MRAM, WL_b is always high for both reading and writing operations, while WL_a is set high for the period of a writing operation. A write voltage (V_{BL} or V_{SL}) of 0.4 V with 300 ps pulse width is used to change the free layer magnetization of MTJ0 and MTJ1 as shown in Figure 5.15. The logic state of MTJs is governs by the voltage on *SL* and *BL* terminal.

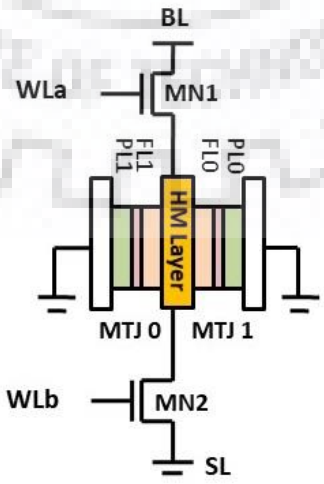


Figure 5.14 Write circuit for DSH-MRAM

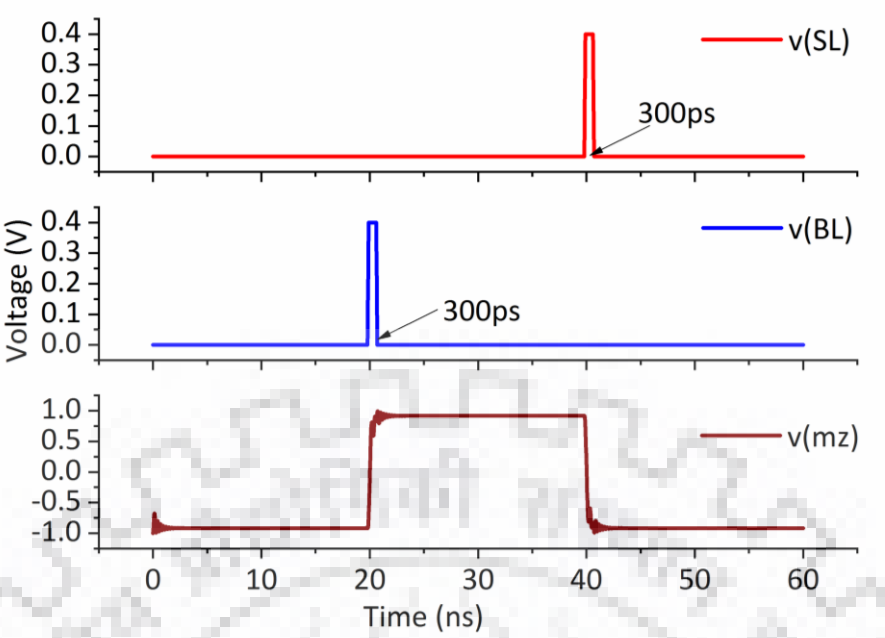


Figure 5.15 Switching for DSH-MRAM

5.3.2 DSH-MRAM Read Circuit

Pre charge sense amplifier (PCSA) is used to read the logic stored in MTJs cell of DSH-MRAM. The DSH-MRAM based PCSA circuit contributes transistors (four *p*MOS, three *n*MOS) and two MTJs as shown in Figure 5.16.

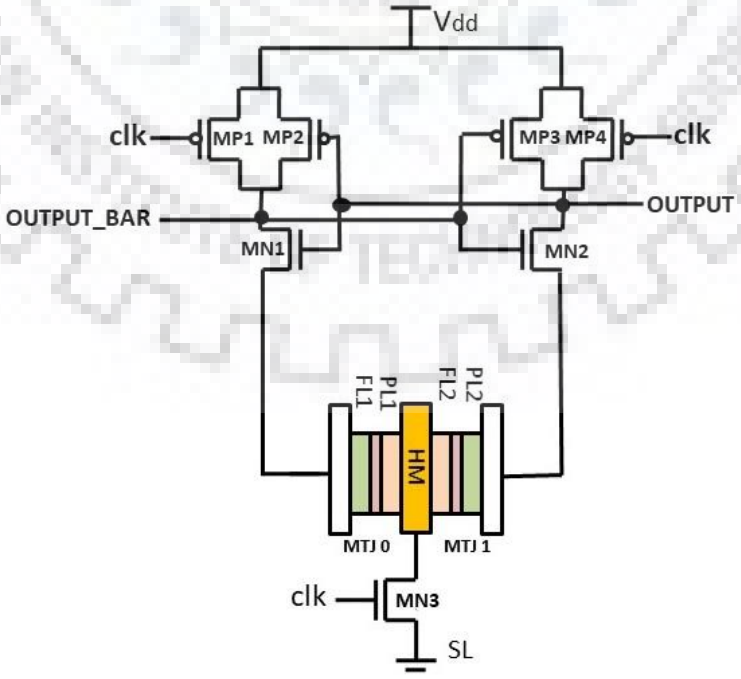


Figure 5.16 DSHE-MRAM based PCSA

PCSA works in two phase: 1. Precharge Phase 2. Evalution Phase. In precharge phase when clk=0 the output and output_bar both charge up to Vdd through MP4, MP1 transistor respectively. The MP2, MP3, MN1 and MN2 are the two inverter connected in the form of feedback. In evalution phase when clk=1, the pull down transistor MN3 is ON. This transistor gives the discharging path to the minimum resistance path. If the MTJ1 is at lower resistance, then the OUTPUT_BAR is discharge to zero. Likewise, if the MTJ2 is at lower resistance then the OUTPUT is discharged to ground as shown in Figure 5.17. The sensing delay for DSH-MRAM-MRAM is 34.9 ps.

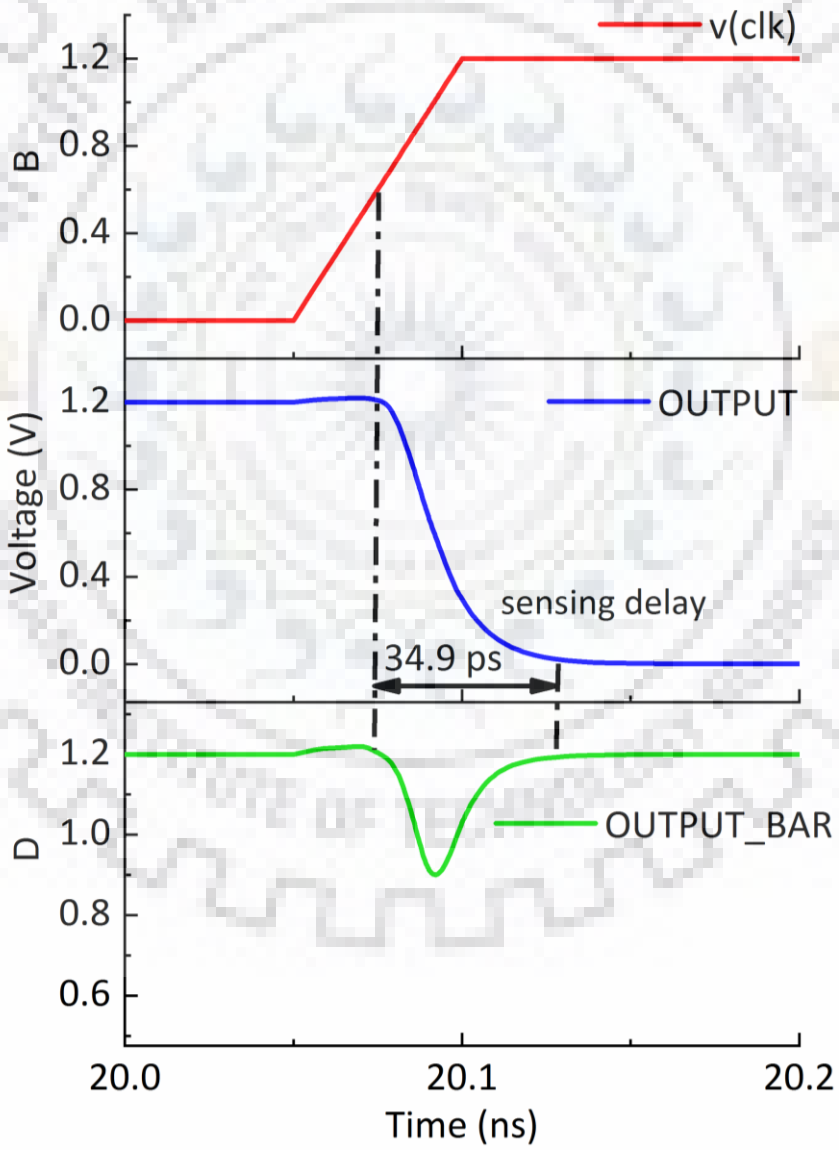


Figure 5.17 Simulation Result of DSHE-MRAM based PCSA

5.3.3 Magnetization of DSHE-MRAM

The switching time (tsw) is the time taken to change the state from AP to P (P to AP) by changing the magnetization orientation of the MTJs layer. If it is sufficiently low, it means that device is fast. The switching time (t_{sw}) for STT-MRAM is 3 ns as represent in Figure 5.18.

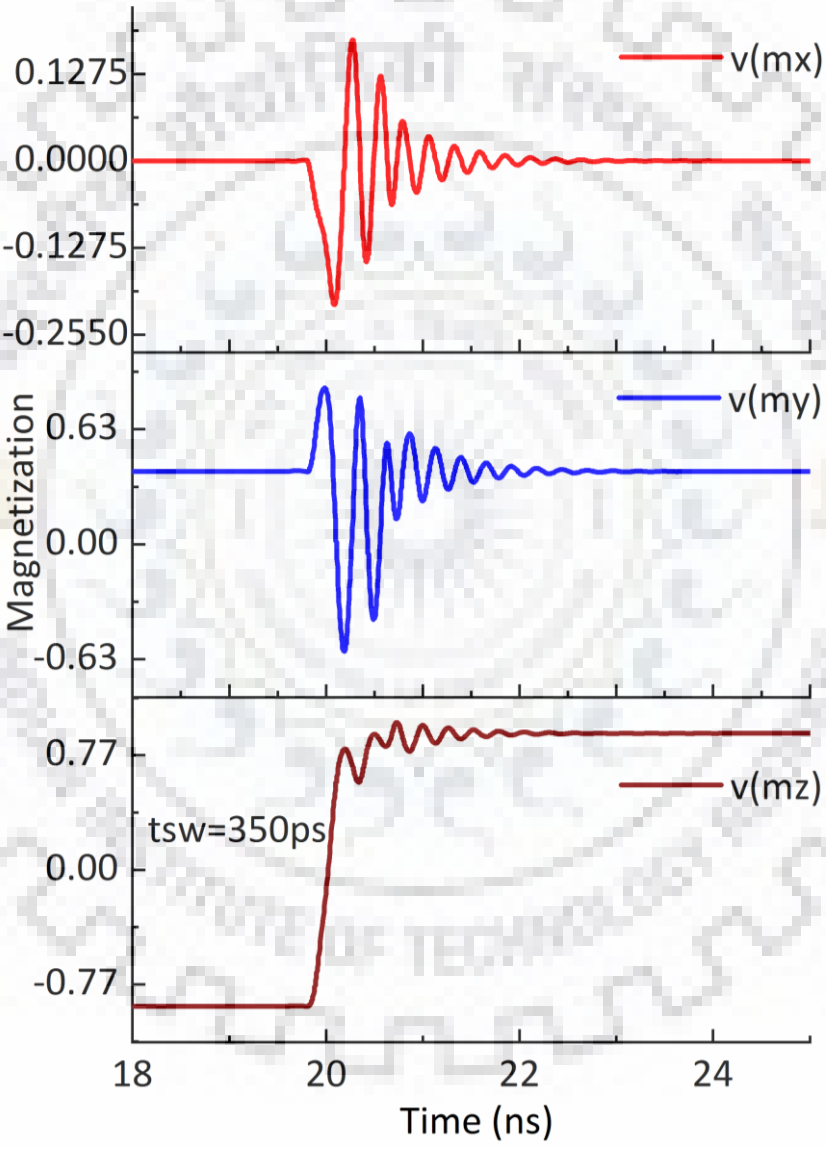


Figure 5.18 Magnetization timing diagram of DSH-MRAM

CHAPTER6

LOGIC CIRCUIT BASED ON STT-MRAM AND DSH-MRAM

6.1 Hybrid CMOS/MTJ circuits

The hybrid CMOS/MTJ circuits have four parts as shown in Figure 6.1. The pre-charge sense amplifier (PCSA) for evaluating the complementary outputs [36]. The combination of *n*MOS transistors used to get the desired output. Write circuit is used to write a particular bit among the pair of MTJs. The MTJs are used to store the complementary bits i.e. non-volatile. The read and write current works in an alternate clock cycles.

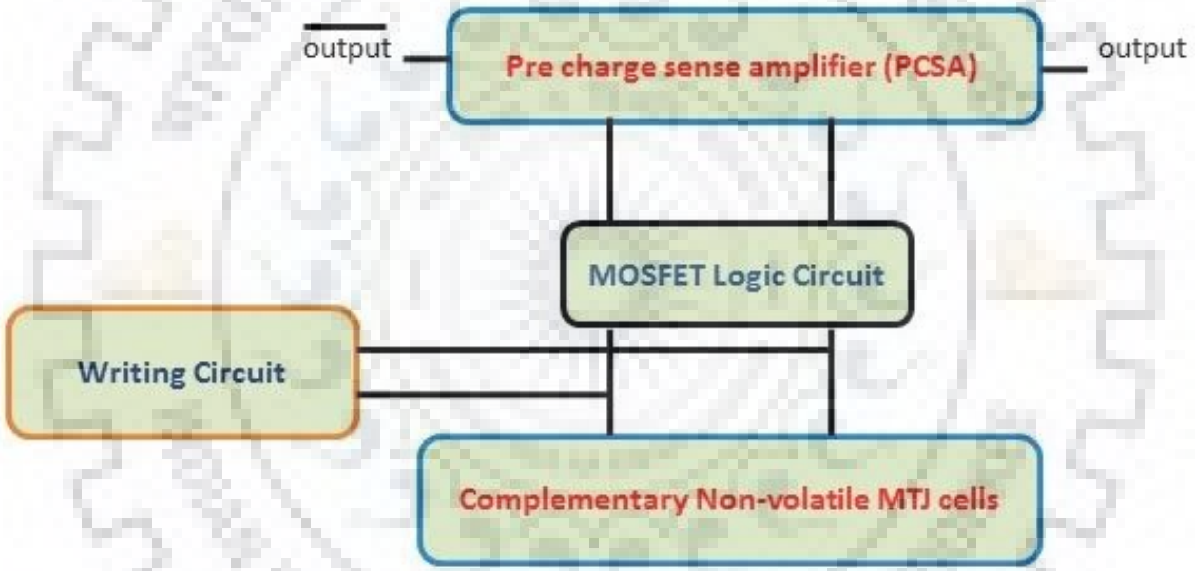
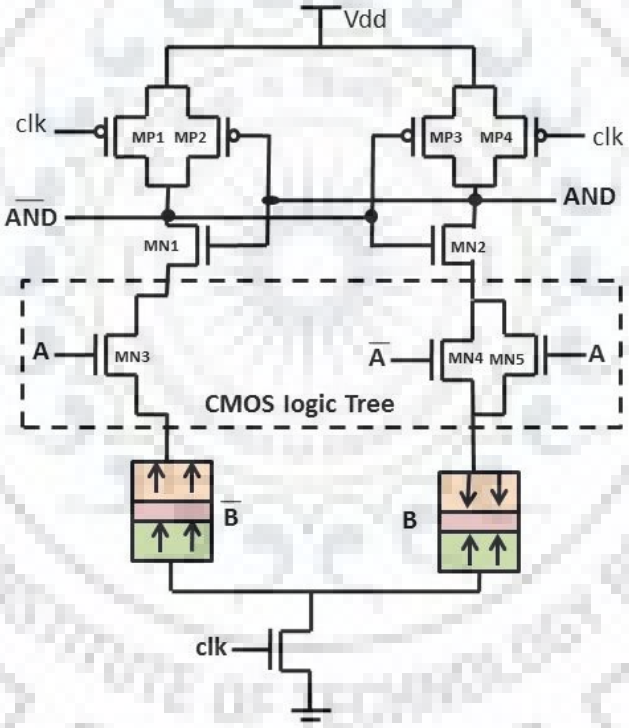


Figure 6.1 Hybrid CMOS/MTJ Circuit

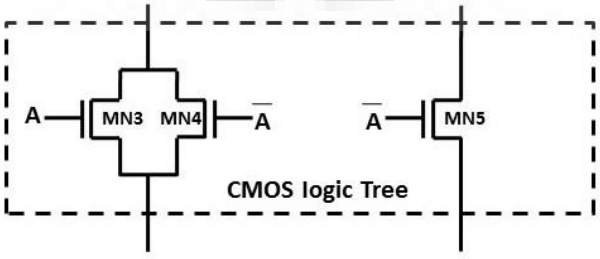
6.2 STT-MRAM Based Logic Gates

The circuit configuration of hybrid MTJ/CMOS for AND/NAND gate is represent in Figure 6.2(a) [39]. It works in two phases: precharge and evaluation phase. B and $\overline{B}$ are the nonvolatile inputs realized using complementary MTJs. In the duration of the precharge phase (clk = 0), both the outputs values will remain at the high logic level. Outputs are evaluated in the evaluation phase (clk = 1) based on the inputs. In MTJ device high resistance state *(*R_{AP}*)* of MTJs is considered as logic '0' (antiparallel state of magnetization) and low resistance state *(*R_P*)* as logic '1' (parallel state of magnetization).

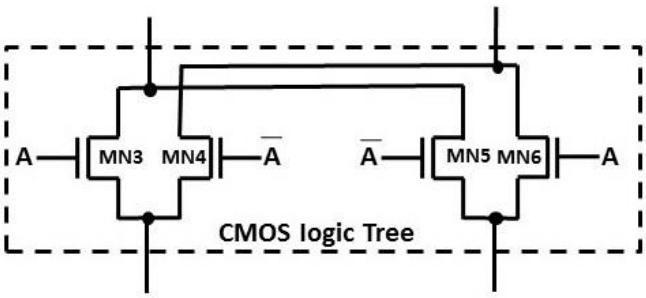
When volatile input A is at logic low '0', *n*MOS transistors MN3 and MN5 will be in OFF mode. Hence, the left branch will be an open circuit resulting in no discharge path through the left branch. Therefore, the output AND will be pulled down through MN2 and MN4 transistors to ground. For input combinations '10' and '11', outputs will depend on the resistance state of nonvolatile inputs through MTJ. For input combination 10 current will pass through both the branches as MN3 and MN5 both are ON. The resistance value of the right side branch is lesser value than that of the left side branch. Hence, the output value of AND node will be discharged to ground and output $\overline{AND}$ will remain at a high logic level. Similarly, during 11 input state resistance value of the right side branch will be higher than the left side one. Hence, the output node AND will remain at a high logic level while $\overline{AND}$ node will be discharged through MN1 and MN3 transistors to ground.



(a)



(b)

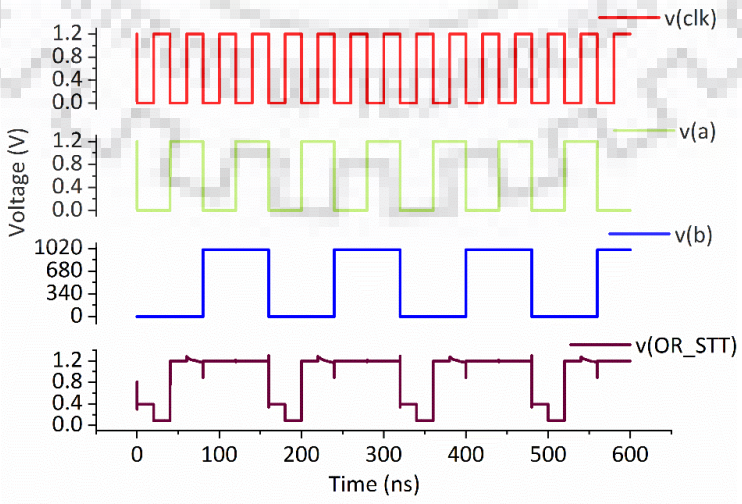


(c)

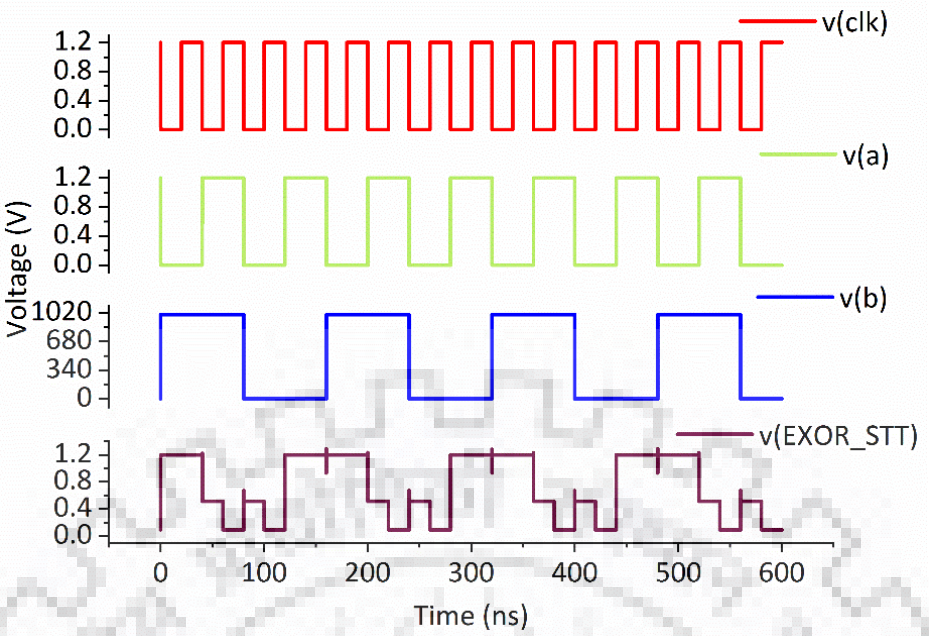
Figure 6.2: STT-MRAM based logic circuits (a) AND gate (b) OR gate (c) EXOR gate

OR/NOR circuit realized using hybrid MTJ/CMOS is shown in Figure 6.2(b). For the input state, 00 resistance value of the left branch is greater than the right side branch. Hence, output node $\overline{OR}$ remains at a high logic level while the output OR is discharged through MN2 and MN5 *n*MOS transistor. In the case of 01, the resistance value of the right side branch is higher than the left branch so the output node OR remains at a high logic level while $\overline{OR}$ is discharged through MN1 and MN3 *n*MOS transistor. During 10 and 11 input state *n*MOS transistor, MN5 will be in OFF mode and the hence right branch will open circuit So Output OR will remain at the high logic level.

EXOR/EXNOR circuit realized using hybrid MTJ/CMOS is shown in Figure 6.2(c). *n*MOS transistor MN4 and MN6 constitute the left branch while the right branch consists of MN5 and MN3 transistors. For the duration of the evaluation phase (clk = 1), the output EXOR will be discharged as the resistance value of the right side branch is smaller than the left side branch for 00 and 11 state.



(a)



(b)

Figure 6.3 Timing waveform of (a) STT-MRAM based OR gate (b) EXOR gate

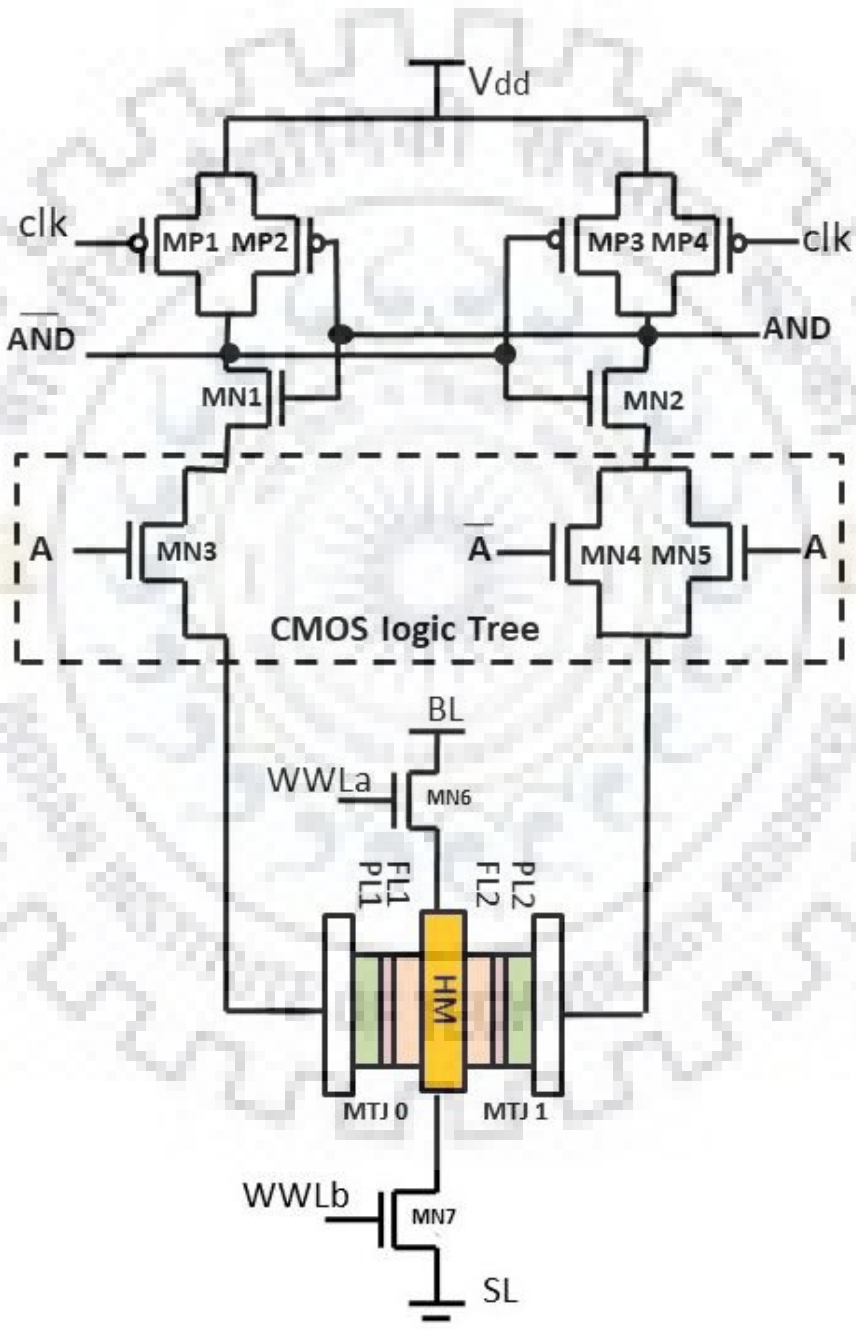
Similarly, for input combinations, 01 and 10 output $\overline{EXOR}$ will be discharged because the resistance value of the left side branch is smaller than a right branch. The timings waveforms for OR and EXOR logic gate is shown in Figure 6.3(a), (b).

6.3 DSH-MRAM Based Logic Gates

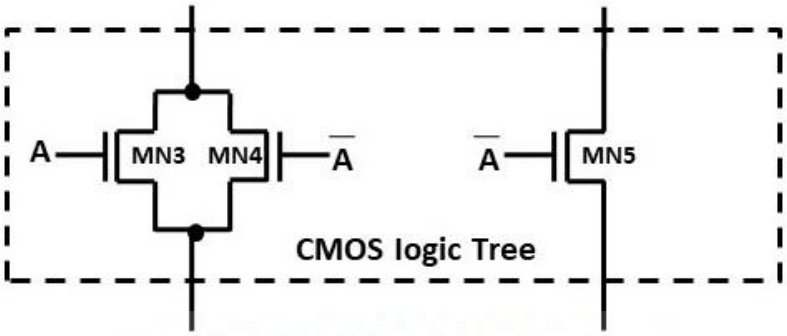
Circuit configuration of hybrid MTJ/CMOS for AND/NAND gate is represent in Figure 6.4(a). It works in two phases: precharge and evaluation phase. B and $\overline{B}$ are the nonvolatile inputs realized using complementary MTJs. In the duration of the precharge phase (clk = 0), both the outputs will remain at the high logic level. Outputs are evaluated during the evaluation phase (clk = 1) based on the inputs. In MTJ device high resistance state (R_{AP}) of MTJs is considered as logic '0' (antiparallel state of magnetization) and low resistance state (R_P) as logic '1' (parallel state of magnetization).

When volatile input A is at logic low '0', *n*MOS transistors MN3 and MN5 will be in OFF mode. Hence, the left branch will be an open circuit resulting in no discharge path through the left branch. Therefore, the output AND node will be discharged to ground through MN2 and MN4 transistors. For input combinations '10' and '11', outputs will depend on the resistance state of non-volatile inputs through MTJ. For input combination 10 current will pass through both the branches as MN3 and MN5 both are ON. The resistance value of the

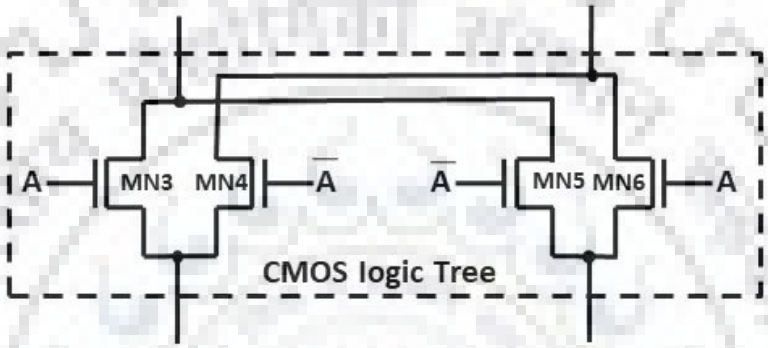
right side branch is lesser than that of the left side branch. Hence, the output AND node will be discharged to ground and output $\overline{AND}$ node will remain at a high logic level. Similarly, during 11 input state resistance value of the right side branch will be greater than that of the left side one. Hence, the output value of AND will remain at a high logic level while $\overline{AND}$ will be discharged through MN1 and MN3 transistors to ground.



(a)



(b)

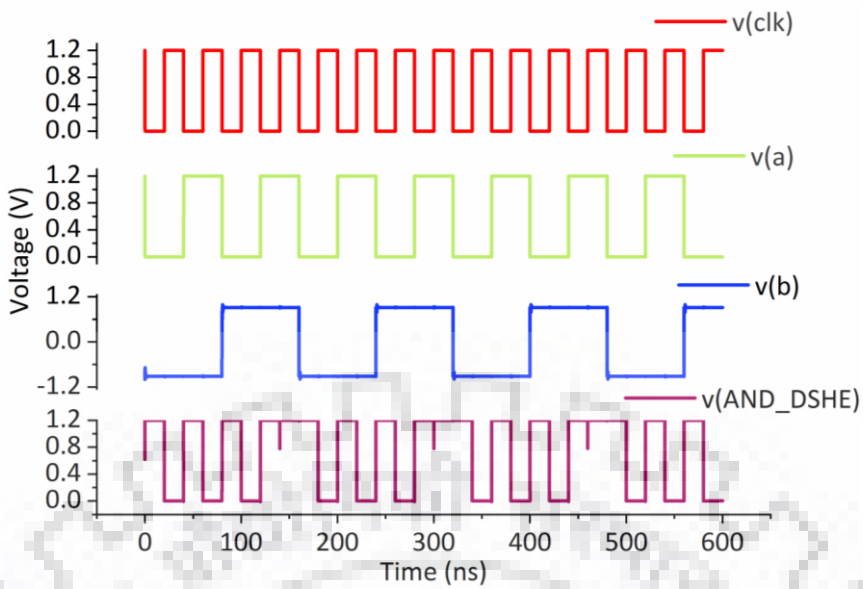


(c)

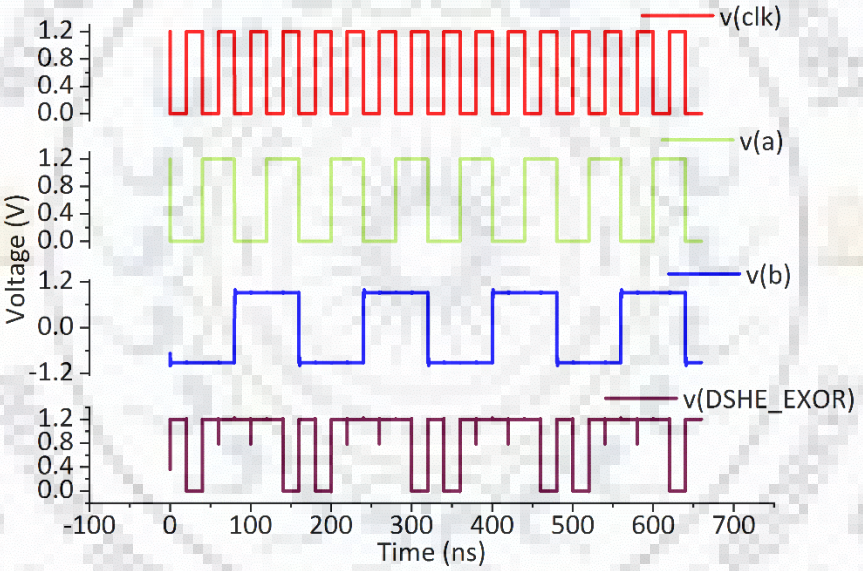
Figure 6.4 DSH-MRAM based logic circuits (a) AND gate (b) OR gate (c) EXOR gate

OR/NOR circuit realized using hybrid MTJ/CMOS is shown in Figure 6.4(b). For the input state, 00 resistance of the left branch is higher than the right branch. Hence, output $\overline{OR}$ remains at a high logic level while the output OR is discharged through MN2 and MN5 *n*MOS transistor. In the case of 01, the resistance value of the right side branch is higher than the left side branch so the output value of OR remains at a high logic level while $\overline{OR}$ is discharged through MN1 and MN3 *n*MOS transistor. During 10 and 11 input state *n*MOS transistor, MN5 will be in OFF mode and the hence right branch will open circuit So Output OR will remain at the high logic level.

EXOR/EXNOR circuit realized using hybrid MTJ/CMOS is shown in Figure 6.4(c). *n*MOS transistor MN4 and MN6 constitute the left branch while the right branch consists of MN5 and MN3 transistors. During the evaluation phase (clk = 1), the output EXOR will be discharged as the resistance value of the right side branch is smaller than the left side branch for 00 and 11 state.



(a)



(b)

Figure 6.5 Timing waveform of DSH-MRAM based (a) AND gate (b) EXOR gate

Similarly, for input combinations, 01 and 10 output $\overline{EXOR}$ will be discharged because the resistance value of the left branch is lesser than a right branch. The timings waveforms for OR and $\overline{EXOR}$ logic gate is shown in Figure 6.5(a), (b).

6.4 Comparison of Power consumption of STT and DSH-MRAM Based Logic Gates

The power consumption of hybrid CMOS/MTJ logic gates based on DSH-MRAM is relatively very low as comparison to logic gates based on STT-MRAM as shown in Table

6.1. It is due to narrow pulse width (300 ps) and low write voltage (0.4 V) for writing the MTJs in case of DSH-MRAM.

Table 6.1 Comparison of power consumption of STT-MRAM and DSH-MRAM based logic gates at 1.2 V.

Basic Logic Gates	Based on STT-MRAM	Based on DSH-MRAM
AND/NAND gate	2.06µW	0.09µW
OR/NOR gate	2.22µW	0.1µW
EXOR/EXNOR gate	2.69µW	0.11µW

6.5 Process Variation

The main sources of process variations in DSH-MRAM is cross-sectional area of MTJs and tunneling oxide thickness (t_{ox}) [38]. The read and write failure can be happen because of these process variation. The resistance of MTJs is varies inversely proportional to the cross-sectional area of MTJs and the resistance of MTJs varies exponentially with tunnel oxide thickness of the MTJs

The variation of TMR with different width of *n*MOS transistor at different applied voltage for STT-MRAM cell is shown in Figure 18. The variation in TMR is according to equation (5).

$$TMR = \frac{TMR(0)}{1+(V_b \times V_b)/(V_h \times V_h)} \tag{5}$$

Here, $TMR(0)$ is TMR at zero bias voltage, V_b is potential drop across MTJ, V_h bias voltage when $TMR = \frac{TMR(0)}{2}$ [36]. When we increase the width of *n*MOS transistor the resistance of transistor start decreasing because of that voltage drop across MTJ increase i.e. V_b. TMR is inversely proportional to V_b according to equation (5), same we observed shown in Figure 6.6.

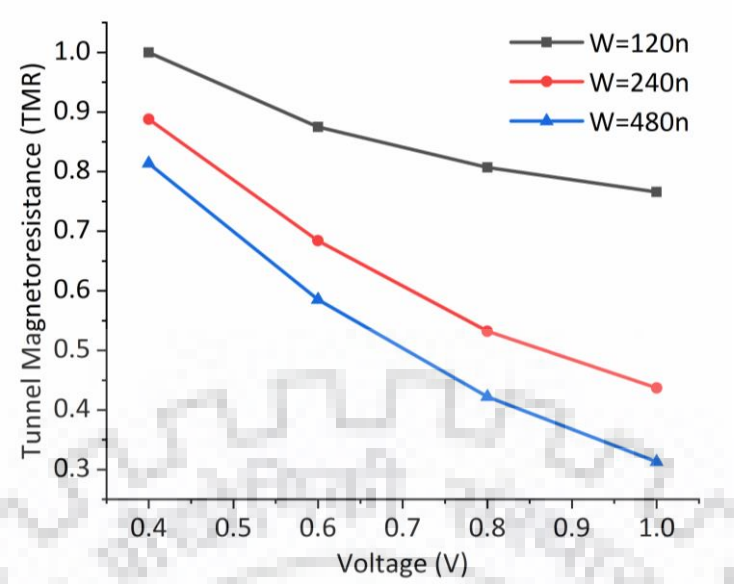


Figure 6.6 TMR variation with applied voltage at different width of *n*MOS for STT-MRAM cell

The simulations are done by varying the power supply (V_{dd}) from 0.6V to 1.4V of pre-charge sense amplifier (PCSA) implemented by using STT and DSH-MRAM. We see that the power dissipation is proportional and the delay is inversely proportional to V_{dd}. The power dissipation and delay both are more in case of STT in comparison of DSH-MRAM as represent in Figure 6.7.

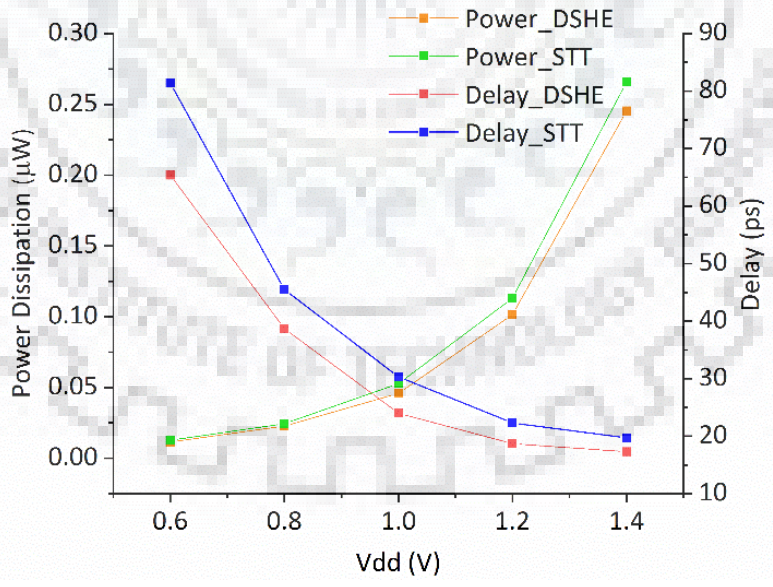


Figure 6.7 Power dissipation and delay variation of DSH-MRAM and STT-MRAM based PCSA with power supply (V_{dd}).

The Monte Carlo statistical simulations are performed for 4000 samples with Gaussian distribution (3σ) to evaluate the impacts of the variation. In practical cases, the variation

during fabrication is random. we cannot predict them directly so in this paper we take approximate variation of 10% in power supply (Vdd), 5% in threshold voltage of MOSFETs, 2% in oxide barrier thickness, 2 % in free layer thickness, 5% in cross-sectional area of MTJ [14], [40], [41]. The Monte Carlo statistical simulations results for MTJ resistance are represent in Figure 6.8 and Figure 6.9.

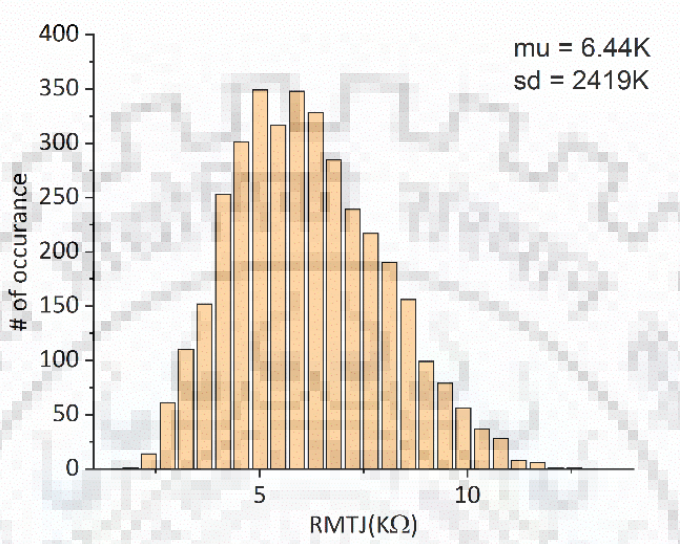


Figure 6.8 Parallel Resistance statics of DSH-MRAM.

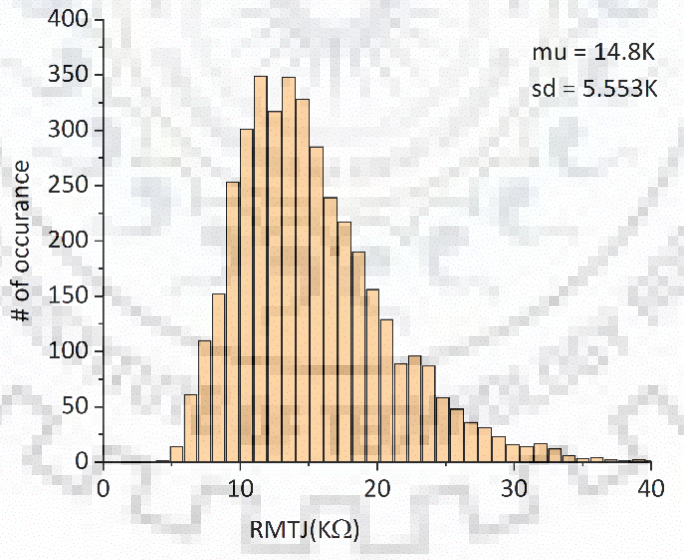
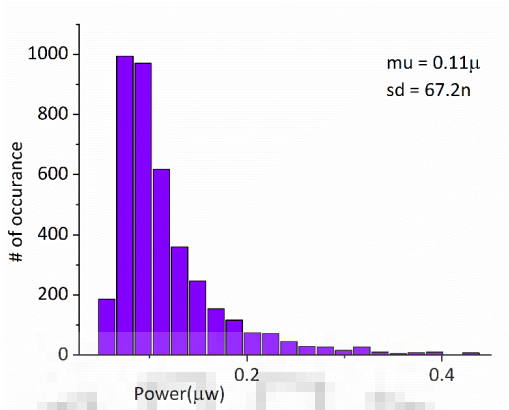
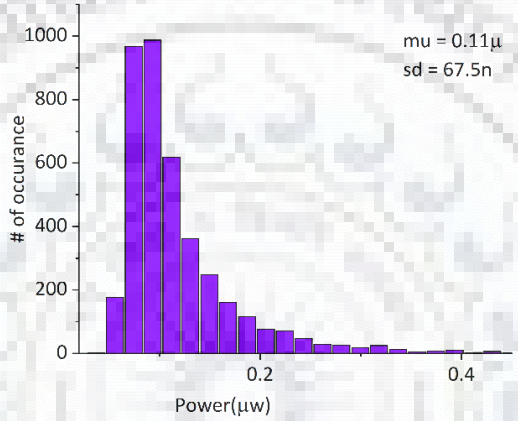


Figure 6.9 Anti-Parallel Resistance statics of DSH-MRAM.

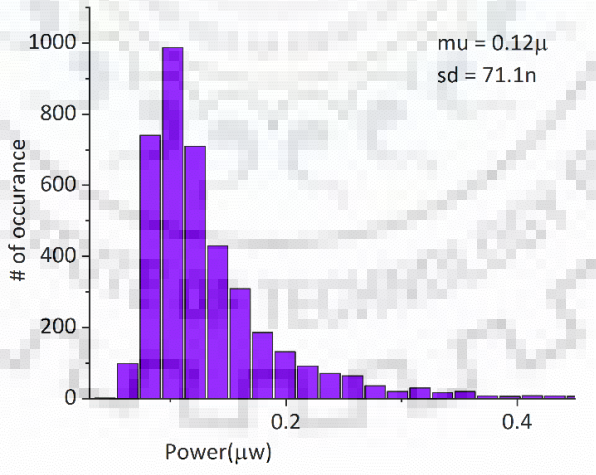
Monte Carlo simulation for power dissipation in DSH-MRAM based logic gates are shown in Figure 6.10. In results of Monte Carlo simulation distribution for power dissipation of DSH-MRAM based logic gates only 2.2% samples are beyond the 6σ yield.



(a)



(b)



(c)

Figure 6.10 Power dissipation statics of DSH-MRAM based (a) AND gate (b) OR gate (c) EXOR gate

CONCLUSION

It seems that in upcoming era's the spintronics technology replace the charge based technology because charge based technology has many drawbacks which deteriorates the performance of the device. The required constraints in a good quality of device is low power consumption, low static power loss, memory should be non-volatile in nature, high density, speed, access time, high endurance, cost per bit, occupied area on chip is less and these are not full-fill by existing MOSFET technology. Main leading memories in present are dynamic read only memory (DRAM), static read only memory (SRAM), flash memory (non-volatile). But they are not full-fill all the requirement which are mention above like SRAM it is high static leakage power and capacity of storage is low, DRAM manufacturing process is complex and it required refreshing current periodically. In Flash (non-volatile) memory requires excess write power.

So, we need a technology which full-fill these all constraints. for that analysis says the spintronics based technology fit into best. In STT/SHE/DSHE-MRAM the static power loss is almost zero other than that it requires less chip area etc. STT/SHE/DSHE-MRAM is far better than the most of the present leading memory technologies (SRAM, DRAM, and FLASH).

Table 6.2 Comparison Between different memories technologies [18]

	SRAM	**FeRAM**	**STT-MRAM**	**SHE-MRAM**	**DSHE-MRAM**
Non-volatility	No	Yes	Yes	Yes	Yes
Endurance	$>10^{15}$	$<10^{12}$	$>10^{15}$	$>10^{15}$	$>10^{15}$
Density	Medium	High	High	High	High
Scalability	Good	Limited	Very Good	Very Good	Very Good
Storage bits	True and Complementary bit	True bit	True bit	True bit	True and Complementary bit
Speed	Fastest	Medium	Fast	Very Fast	Very Fast
Standby current	Low/high	Zero	Zero	Zero	Zero
Technology	Product	Product	Advanced development	Development	Early development

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