STUDIES ON LANDSLIDE MOVEMENTS IN PARTS OF HIMALAYA IN UTTARAKHAND USING DINSAR TECHNIQUES

SYNOPSIS

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1. Introduction

The thermionic injection of electrons over the barrier in the metal-oxide-semiconductor Field Effect Transistors imposes a fundamental limitation to the steep transition. Thus electro-statically, a new device to provide steep slope and high drive current is the need of the time in order to improve the energy efficiency of the circuits [1], [2]. Over the last decade, the journey of Tunneling FETs (TFETs) for improving the drive capability and the subthreshold slope (SS) has directed to the proposal of many new device architecture. An optimization of device architecture and source/channel/drain material and doping is being strongly pursued [3]. The two main tunneling mechanism are as follows: one is lateral (point) tunneling, whereby the tunneling takes place between in parallel to the gate. Other one is line (vertical) tunneling, whereby the tunneling is perpendicular to the gate [4]. In later case the area of cross section for tunneling is increased which improves the drive current and SS. The analog and digital application of TFETs are extensively being explored due to its unique saturation characteristics [5], [6]. Recently, tunnel FETs for internet-of-things applications have been successfully demonstrated experimentally [7]. The focus of research on TFETs is mostly concentrated on the drive currents and steep slopes. The role of interface traps and quantum confinements have also been well addressed [8], [9].

The main concern of TFET based analog circuits is to identify the drain current saturation voltage (V_{DSAT}) of the device to bias the circuits properly. The architecture of the point and line tunneling devices are different in nature and hence the associated physics behind the drain current saturation is also different. The saturation in both the point and line TFETs occur at a constant difference between the gate and drain bias. Till now, the estimation of V_{DSAT} for TFETs are being made as the voltage required to reach 90-95% of the maximum drain current [10], [11]. These methods are merely rough estimation of V_{DSAT} and are not physics based. The correct estimation of V_{DSAT} also provides the trends of analog performance parameters in saturation regimes. A few researchers have discussed the saturation in point TFETs but the saturation of drain current in line TFETs have not been addressed. Moreover, the device design parameters strongly affects the saturation characteristics, especially the value of V_{DSAT}. So there is a need of device/circuit design guidelines using TFETs. The influence of saturation voltages on the analog circuit performance is also yet to be discussed analytically.

The impact of body bias on the drain current modulation has been addressed for point TFETs [12], [13], but its implication to drain current saturation and analog performance need to analyzed. Further the modulation of drain current in case of line TFETs is also required to be evaluated, due to its different gate capacitances and tunneling mechanism. The value of body bias to attain maximum drain current should also be modeled for TFET devices. Although a large number of analytical models and SPICE level models have been demonstrated for group IV and III-V based hetero and homo junction TFETs [14]. However, a compact analytical model for epitaxial layer based line TFET [15] device is also not presented comprehensively. Lastly there is a great need of small signal model for TFETs, so that the values of vital analog performance parameters can be predicted for different device design parameters.

2. Problem Statement

In light of the extensive literature survey, this thesis work reports the physics behind the drain current saturation in point and line TFETs and their implications to analog circuit design. Presently, the TFETs based analog circuits are either arbitrarily biased or a rough approximation is being used. For instance, the drain voltage at which the drain current attains 90-95% of its maximum values, is being used as the saturation voltage. Therefore, we present the extraction method for V_{DSAT} for TFETs, so that biasing of analog circuit can be done properly. The device/circuit performance in soft and deep saturation regimes is also discussed in our work. Since, the Line TFETs exhibit high drive current as compared to their point TFET counterparts, thus most of our work is targeted for line TFETs. The impact of body bias on the epitaxial layer based line TFETs are also presented comprehensively. Lastly, the influence of gate-source overlap length on the vital small signal parameter is reported. Specific objective to provide systematic design methodology for TFETs based analog circuits are as under:

- The drain current of the point TFETs saturates for a constant difference between the gate (V_{GS}) and drain (V_{DS}) bias. Initially, with the increasing drain bias, the conduction band energy difference between the channel and drain remains constant. After certain V_{DS}, this difference starts to increase [16]. Further, the difference between the valance band energy of source and conduction band energy of channel saturates at a specific drain voltage. We have address this issue and also proposed a phenomenological approach to extract the V_{DSAT} of point TFETs.

- The drain current saturation with V_{DS} for epitaxial layer based line TFET has not been addressed. The impact of drain bias on tunneling is different when compared to point TFET. This is because of different band-to-band tunneling mechanism in both the devices, therefore the gate capacitances are also different [17]. The saturation voltage are strongly influenced by the device design parameters, thus a device/circuit design guideline is presented in this work. The variation of vital analog device/circuit parameters of line TFETs also need to be evaluated.
- The critical role body bias in analog circuits have been addressed in literature. In conventional MOSFET the body bias modulates the threshold voltage. For point TFETs, the body bias modulates the drain current [12] due to change in the electric field at the tunneling junction. The availability of states for tunneling plays a critical role in determining the drain current. This issues is addressed in our work. Further, the role of various device design parameters on the drain current modulation and model for V_{BSAT} are also required to be addressed systematically.
- Theoretically, the drain current should increased linearly with the increasing gate-source overlap length in line TFETs [18]. However, a sub-linear increase is observed in the drain current [15]. The physics behind the above said effect is not explained properly. Further, a gate-source overlap length aware small signal model for line TFET is required for analog circuit analysis, so that, the prediction of small signal model parameters can be made easily. This issue is also addressed in our work for saturation regime operation.

3. Thesis Organization

This thesis is based on the objectives discussed above. This thesis is consisted of total seven chapters. Each chapter begin with the introduction, problem statement and motivation behind the respective study. Thereafter, the simulation framework is discussed in details. This is followed by the analysis and interpretation of results. The novelty of the work is also drawn in the conclusion section.

Chapter 1 provides the need of steep slope devices for low power application. This chapter outlines the basic working principal of Tunnel FETs and potential application area. Thereafter, a summary of each chapter is also presented at last.

Chapter 2 presents an extensive literature review of the TFETs, starting from its origin to the recent advancement. This also discuss that how the junction and material engineering are the major driving force behind obtaining the steep slope. The potential applications and limitation of TFETs are also discussed in this chapter.

Chapter 3 deals with a thorough explanation of the physics behind the drain current saturation in point tunneling based TFETs. A well calibrated simulation deck is used to carry out numerical simulation using Sentaurus TCAD tool of Synopsys Inc.. An approach to define the soft and deep saturation condition is also presented for the first time. We propose a systematic methodology to identify the soft and deep saturation voltages of the device, hence a method to extract the V_{DSAT} is also presented. This in turn facilitates the analog designer, to bias the analog circuit in the appropriate regime. A common source amplifier biased in the soft and deep saturation regime is also demonstrated. Further, the impact of source/drain doping and gate length on V_{DSAT} is also presented with the reasoning. The validation of proposed method is done against the experimental data.

Chapter 4 explains the saturation in drain current for a line tunneling based TFETs. The device under consideration is an epitaxial layer TFET, whereby the tunneling occurs normal to the gate. The physics of saturation is different from the point tunneling devices as the tunneling mechanism is different and hence the gate capacitances are also different. As compared to point TFET, the area of cross section for tunneling is effectively increased in line TFETs. The saturation of drain current is explained for the first time. Then, a method to extract the V_{DSAT} for line tunneling TFETs is also proposed for the first time. We also propose the guidelines for line TFETs based device/circuit design. The variation of V_{DSAT} with vital device design parameters like overlap length, doping and thickness of epitaxial layer is also presented with appropriate physics based reasoning. The behavior of vital analog performance parameter with the device design parameters are also explained.

Chapter 5 presents a comprehensive study about the impact of reverse and forward body biasing on the epitaxial layer based line TFETs. The modulation of drain current with body bias is mainly due to the modulation of the available states for tunneling. A physics based explanation of the above said effect is also validated by a mathematical model based on the potential balance equation. The variation in V_{BSAT} (the voltage at which the drain current maximize) with gate and drain bias is also explained with our model. The behavior of vital analog performance parameter with the reverse and forward body bias is also examined in detail. Further, the impact of body biasing on the V_{DSAT} is also examined from the perspective of analog circuit design.

Chapter 6 explains the behavior of drain current with change in the gate-source overlap length in line TFETs. Thereafter, the impact of gate-source overlap length on the vital small signal parameters are discussed. An empirical model to predict the trends of small signal parameter with overlap length in saturation regime, is also presented. The main cause behind the sub-linear increase in drain current with the gate -source overlap length is the lateral electric field induced by the drain. This causes the drain current to exhibit a sub-linear change.

Chapter 7 presents the major finding of the thesis. The conclusions are drawn on the basis of results obtained through TCAD simulations and physics based models. The future scope of the current study is also proposed for the perspective readers.

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