GALLIUM NITRIDE BASED CLASS-D SWITCH MODE POWER AMPLIFIER

A DISSERTATION

Submitted in partial fulfilment of the

requirements for the award of the degree

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INTEGRATED DUAL DEGREE

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ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Wireless Communication)

by

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CANDIDATE'S DECLARATION

I hereby declare that the work presented in this dissertation with the title, "**Gallium Nitride Based Class-D Switch Mode Power Ampliifer**" towards the fulfilment of the requirement for the award of the degree of **Integrated Dual Degree in Electronics and Communication Engineering** submitted in the **Department of Electronics and Communication Engineering, Indian Institute of Technology,** Roorkee, India is an authentic record of my own work carried out during the period from May 2016 to May 2017 under the supervision of **Dr. Karun Rawat,** Assistant Professor, Dept. of ECE, IIT Roorkee.

The content of this dissertation has not been submitted by me for the award of any other degree of this or any other institute.

DATE: ……... **SIGNED:** ……..……

(Jai Datt Poonia)

PLACE: ……...

CERTIFICATE

This is to certify that the statement made by the candidate is correct to the best of my knowledge and belief.

DATE: ……... **SIGNED:** ……..……

(Dr. Karun Rawat)

PALCE: ……...

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DEDICATION

This work is dedicated to my parents.

ABSTRACT

Power Amplifiers (PAs) are the essential components of any communication system. PAs are generally used in the communication system to amplify modulated signal at Radio Frequency (RF). It has been observed that there is rapid growth of advanced wireless communication in last decade and it sets new areas for RF circuit designers. Wide bandwidth, high linearity and high efficiency are the essential requirements of any wireless communication system. In general, to reduce the power consumption in any circuit the efficiency has to be improved. PAs are the most power consuming component of any communication system so if the efficiency of PA is less then, the overall efficiency of any system will also reduce. High power consumption in any system will directly reduce the lifetime of batteries in portable devices. To increase the efficiency of PA, it should drive in saturation but linearity of PA reduces.

Design of high efficiency switch mode Class-D PA has been discussed in this thesis. In Class-D operation of PA the active device is operated as a switch and this will increase the efficiency of PA. Load-pull technique is used to calculate the load impedances at fundamental frequency and its harmonics. A proper harmonic termination is used to reduce the power loss and increase the efficiency of PAs. At intrinsic plane of device, voltage and current waveform corresponding to Class-D behavior are maintained during the entire PA design. In order to validate the analysis, a current mode Class-D PA in push-pull configuration at 2 GHz frequency has been designed and fabricated. The fabricated PA has a drain efficiency of 71.5%, power added efficiency of 65.5%, gain of 11.1 dB and output power of 42.54 dBm.

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CHAPTER 1: INTRODUCTION

1.1 Introduction

Power Amplifiers (PAs) are the essential element of any communication systems. The main purpose of these amplifiers is to amplify modulated signal to radio frequency output which is given to the antenna. Hence efficiency of these amplifiers plays a major role in the overall efficiency of whole communication system. Linear amplifiers like Class-A, Class-B, and Class-AB are being widely used in wireless communication system but have very poor efficiency. The low efficiency in practical circuits is mainly due to losses associated with it at RF operation like switching, conduction, gate drive losses etc. Switch mode PAs have replaced these linear amplifiers to get high efficiency. Theoretically, efficiency of Switch mode PAs is 100% [1]. Due to the switching nature of Class-D PA, it can achieve maximum efficiency of 80 % in the input power range of 10 to 100 W. Theoretical efficiency of Class-D PA is 100%. The advantage of this improvement in efficiency subsequently reduce the power consumption at base station applications and make system thermally stable [2]-[4]. In switch mode PA the transistor acts as a switch. However in practical scenario transistors operating in switch mode does not behave as ideal switches. This is because of the finite ON resistance (R_{ON}), parasitic reactance and limitation in gain [4]. The impedances provided by the output load network at each harmonic frequency at intrinsic terminals of transistors in a Class-D PA operation are very important. To get maximum efficiency it have to be ensured that there is no power loss at harmonic frequencies in the circuit by making it open circuited or short circuited at harmonic frequencies according to the design.

During the switching from OFF state to ON state of transistor, the losses in output parasitic inductor and capacitor depends upon frequency in Voltage Mode Class-D (VMCD)

PAs as it decreases the efficiency rapidly with operating frequency. While in Current Mode Class-D (CMCD) this degradation reduces. When there is a transition from OFF to ON states in CMCD PAs, the output voltage across the device is zero, this is called Zero Voltage Switching (ZVS) [6]. Because of ZVS the CMCD have better performance over VMCD at radio frequencies [5]. Regardless of Class-D PA type, there are difficulties in designing lumped tank and wideband baluns (BALanced to UNbalanced) at such high frequencies for these Classes of PAs. In this design instead of using lumped tank for harmonic termination a distributed matching network using transmission lines has been used to provide required impedances at fundamental and harmonic frequencies at intrinsic terminals of transistor regardless of performance of balun and lumped tank.

1.2 Problem Definition and Targeted Goal

In modern wireless communication system, it is required that PA should be highly efficient and linear. Switched mode PAs (SMPAs) like Class-D, E, F, J and S are used to get high efficiency to fulfill this requirement [7-10]. Among various SMPAs, Class-D PA is one of the solution which can deliver high efficiency by minimizing power dissipation. Power dissipation in transistor is minimized by reducing the power loss at harmonics frequencies by making the transistor open circuit (zero current) and short circuit (zero voltage). Also at fundamental frequency by ensuring the ZVS or ZCS condition, the power loss is minimized. A CMCD PA in push-pull configuration design is discussed in this thesis.

1.3 Different Classes of PAs

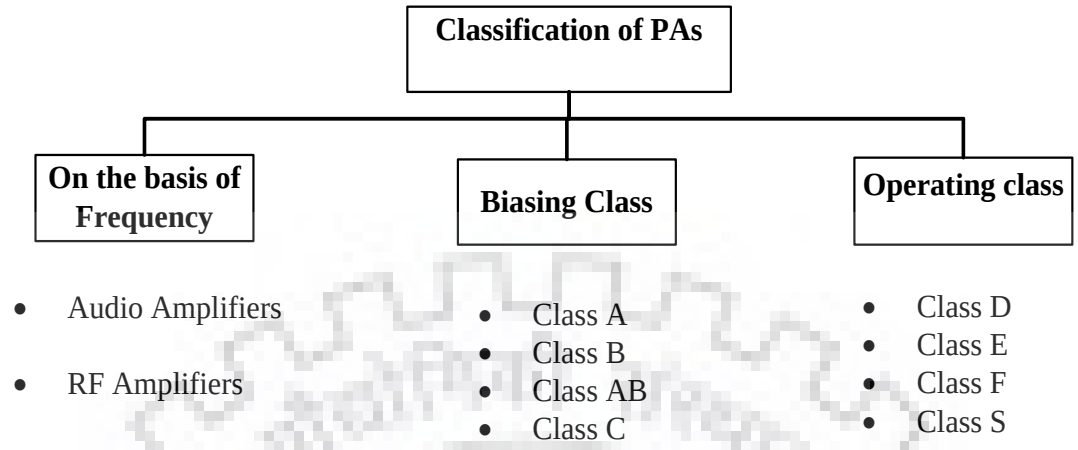

Figure 1 Classification of PAs.

Apart from the classification on the basis of biasing point of active device, further classification of PA is also done on the basis of mode of operation of active device during one cycle of input signal. In these categories, it is assumed that the active device acts as a current source and when it behaves as a switch resulting amplifiers are defined as current mode and switch mode PAs respectively. In switching mode PAs different Classes are defined according to the harmonic control in the device, like Class-D, E, F (inverse F). A detailed discussion of Switch Mode Class-D PA is briefly described in this thesis.

1.3.1 Biasing Class

a) Class-A

This is the most linear Class of PA. The operating point of transistor (active device) in Class-A is approximately in the middle of saturation and pinch off region of transistor or one can say that the device will operate in active region all the time during the 360^0 angle of conduction as shown in Figure 2. Due to this, the output waveforms varies linearly with

the input waveforms and hence it called linear Class of PA. This is also the main advantage of Class-A PA.

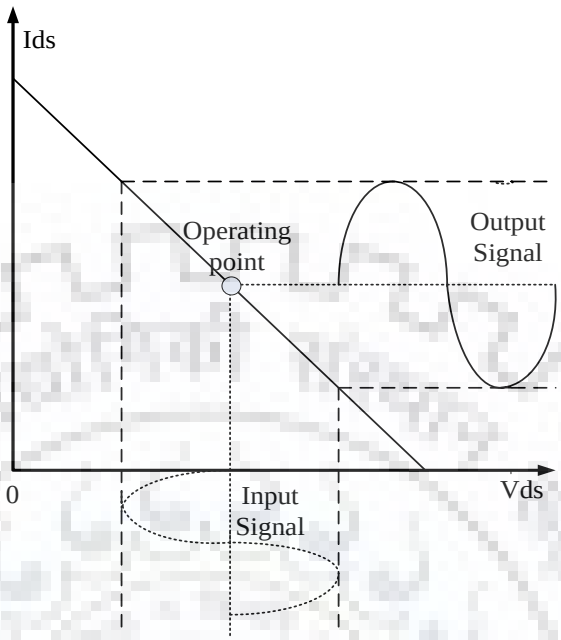

Figure 2 Biasing point of Class-A PA.

Advantage: It produces least distortion in the output among all PAs.

Drawback: In this PA quiescent power dissipation is very large which means transistor dissipates large power although when no AC input is applied.

Application: It is mostly used as a Voltage Amplifier and not preferred as PA due to large quiescent power dissipation.

b) Class-B

In Class-B, the biasing point of transistor is at the pinch off point as can be seen in Figure 3. Hence it has the conduction angle of 180^0. To get the sinusoidal output two transistor are needed to connect in push-pull configuration. Only one transistor is ON at a time. First transistor will operate in the first half cycle and the other one for the second half cycle. So no transistor will operates for more than half cycle of input signal. The linearity

of Class-B PAs are less than that of Class-A but efficiency is higher than the Class-A. In switching mode PAs Class-B is used for biasing of the device.

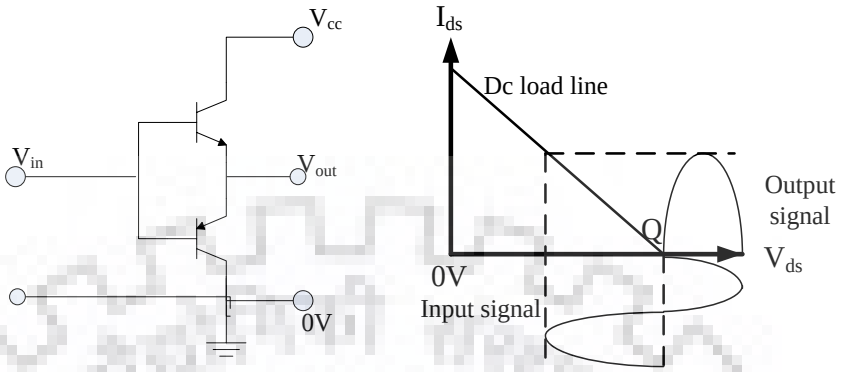

Figure 3 Class-B PA circuit and operating curve.

Advantage :

1. The efficiency is much higher than that of Class-A.
2. No power dissipation when there is no RF input signal is applied.
3. No possibility of DC saturation of core.

Disadvantage :

1. Linearity is less than that of Class-A.
2. There is cross-over distortion in the output waveforms of Class-B push-pull amplifiers.
3. The frequency response is poor.

c) Class-AB

As the name suggests this Class is combination of Class-A and Class-B and the bias point of the transistor is chosen in between Class-A and Class-B as shown in Figure 4. Hence the current conduction angle for this Class of PAs is slightly more than 180^0 but less than 360^0. This Class is basically introduced to eliminate the cross-over distortion problem in the

output waveforms of the Class-B PAs. In this class the linearity is more than Class-B and less than Class-A. The efficiency is more than that of Class-A PAs.

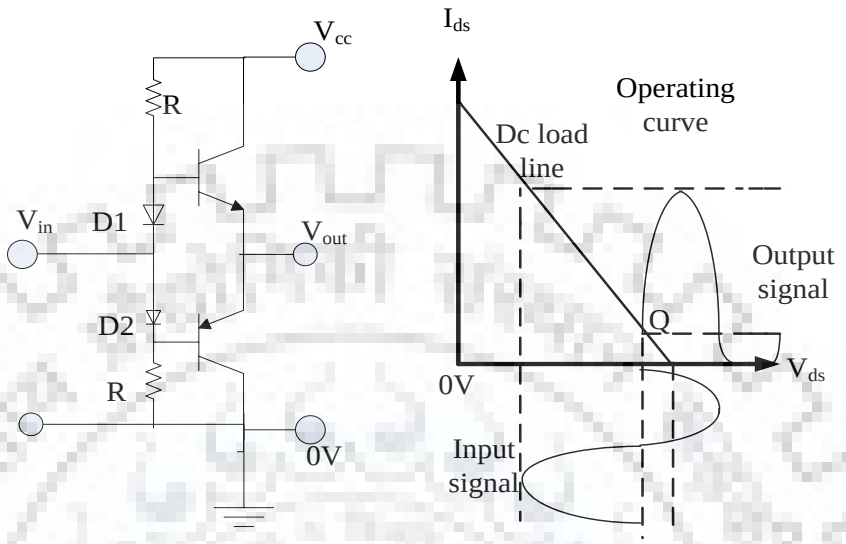

Figure 4 Class-AB PA circuit and operating curve.

d) Class-C

In Class-C PAs, biasing point of transistor is below the pinch off voltage and it has current conduction angle less than 180^0 as can be seen in Figure 5. This means that the transistor will be in OFF state during its operating cycle. Efficiency of Class-C is also very high compare to above discussed Classes but linearity is less. As this Class of amplifiers have high distortion in output waveforms these are generally used in high frequency oscillators and specific type of radio frequency amplifiers. An LC resonator circuit is used at the output of amplifier to convert the current pulses to a full sinusoidal wave of particular frequency.

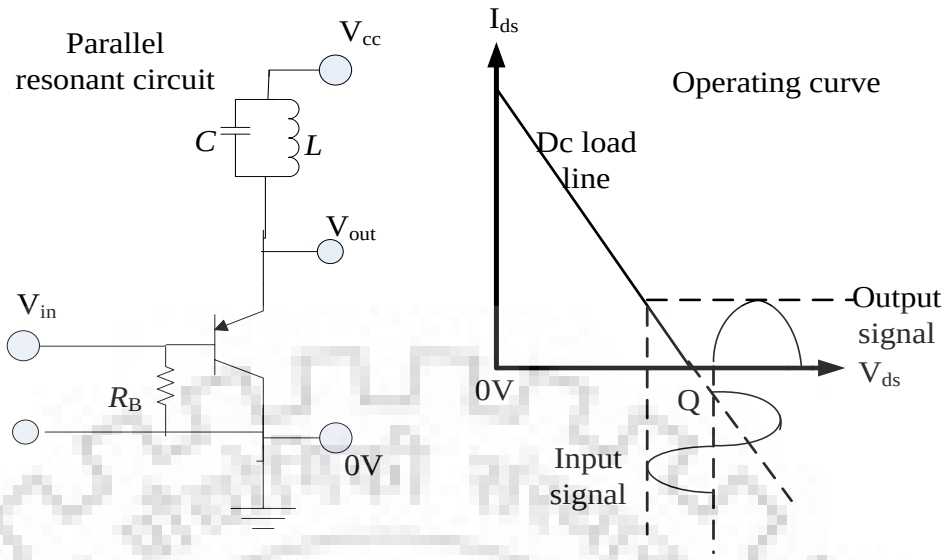

Figure 5 Class-C PA circuit and operating curve.

1.3.2 Operating Class

a) Class-D

Class-D PA was first discussed by Baxandall [7]. In Class-D PAs active device is operated as a switch i.e. either in saturation region or pinch off region but not in linear region. The biasing point of transistor in Class-D PAs is in deep Class-AB or Class-B region. In Class-D PA two transistor are connected in push-pull configuration and driven 180^0 out of phase. It means that only one transistor will be ON for half cycle and another one will ON at one time. There are two type of Class-D PAs, one is voltage switching and another one is current switching. In voltage switching Class-D PAs the waveforms at intrinsic plane are square voltage and half sinusoidal current wave. Similarly in current switching Class-D PAs square current and half sinusoidal voltage waveforms are observed at intrinsic plane of the active devices. By making the harmonics open or short the current and voltage waveforms at intrinsic plane does not overlap hence the power losses are minimized and overall efficiency of PA increases [11]. Theoretically Class-D PAs have efficiency of 100%,

but in practically due to parasitic reactance and finite switching time efficiency degrades. A typical circuit diagram of single ended Class-D PA is shown in figure 7 [12]. The detail discussion on Class-D PA is done in next chapter of this thesis.

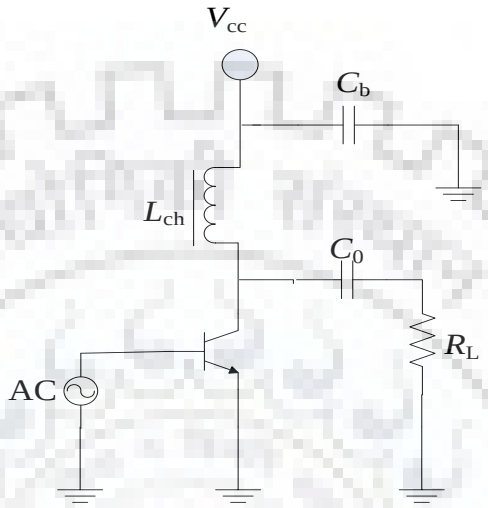

Figure 6 Single ended Class-D PA.

b) Class-E

The Class-E PA was introduced and defined by Sokals [10], [13], and Kazimierczuk, Raab discussed it in more accurate manner [14-16]. Like Class-D, Class-E is also a non-linear PA where the transistor operates as a switch. The Class-E PAs are also capable of achieving 100% theoretical drain efficiency. By minimizing the overlap between drain current and drain voltage of device, power dissipation can be reduced and hence the efficiency of Class-E PA increases [17]. In Figure 7, a typical Class-E PA circuit is shown [10], [14]. A shunt capacitor C_s is used to flatten not only the current but also the voltage waveforms. The harmonic reactance in Class-E is assumed to be negative and comparable in magnitude with fundamental frequency load resistance.

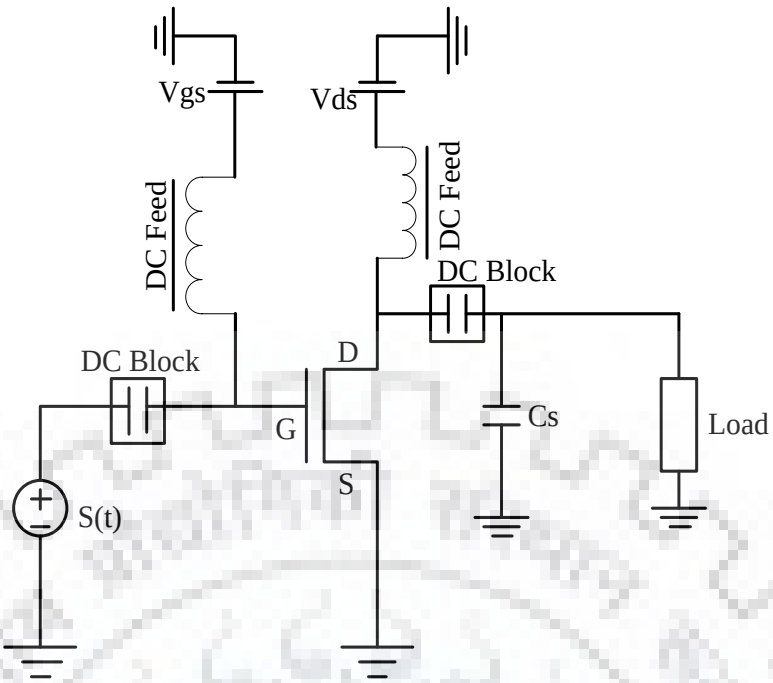

Figure 7 Class-E PA circuit diagram.

c) Class-F

Class-F PAs are slightly different from Class-D and Class-E PAs although biasing in Class-F is also selected in Class-B or Class-C region similar to switch mode PAs [18]. This PA is also non-linear, but the harmonic control (impedances at harmonic frequencies on intrinsic plane of the active device) is different from Class-E. The controlled harmonic termination will give the square current and truncated voltage waveforms. More the number of harmonics controlled, more idealistic waveforms can be obtained. The approximation of square wave current is realized by tuning the load network at even harmonics and the voltage waveforms by tuning the load at odd harmonics. Due to the square waveforms of current and truncated voltage waveforms, Class-F satisfy the ZVS or ZCS conditions [19-20]. This reduces the power dissipation and a high theoretical efficiency of 100% is achieved. In Class-F operation, the square current waveforms are observed which can be applied for the devices in which the current limitation is very critical. In the practical circuits only the finite

harmonics can be controlled so there will be ripples in waveforms. For Class-F, a fast switching device is needed. In addition to this more the odd harmonics are controlled, more the steepness of graph [19-21]. In Figure 8, the typical Class-F circuit diagram is shown [16].

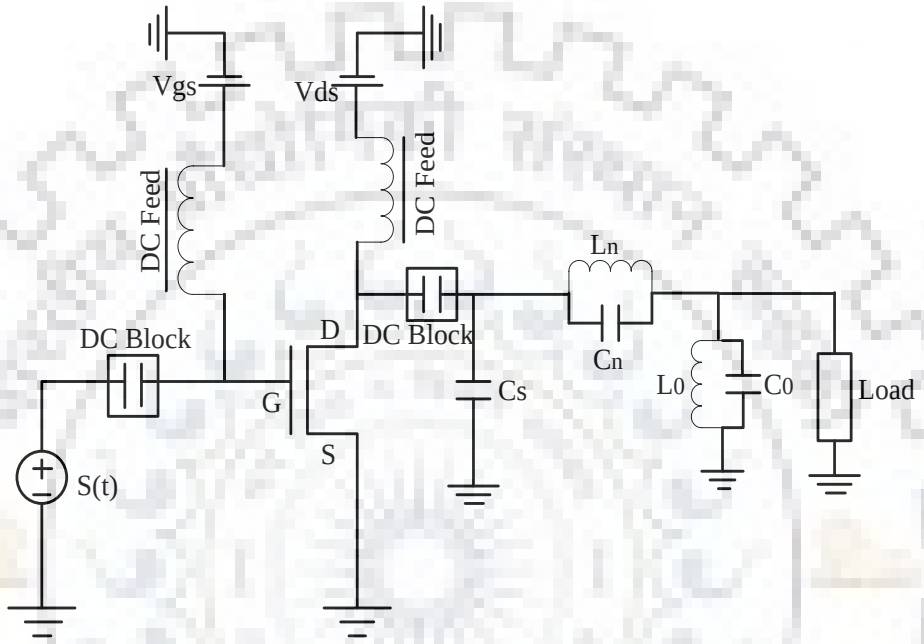

Figure 8 Class-F PA circuit diagram.

According to drain current and voltage waveforms, Class-F can't be considered as Class-D operation, because theoretical backgrounds and assumptions are different [16].

d) Class-S

Class-S is also the switch mode PA based on Class-D structure. In Class-S circuit a switching signal (which can be generated by delta sigma modulation of a simple sinusoidal signal) is given at the input side of Class-D PA and a band pass filter is used at output side

of Class-D to regain the original signal back. The Class-D mode of operation can be considered as ancestor of Class-S operation. Class-S mode includes the most advanced group of PAs. Class-S PA is assumed to be operated on Digital-RF signal of two states. The determination of advanced operation mode which is the most important characteristics of fully switch mode PAs is possible by the switching input signal. The Class-S is operated by switching signal of variable pulse duration, resulting in an inability of operation with ZVS or ZCS conditions. This is the main operational difference between Class-D and Class-S. The typical architecture of Class-S is shown in Figure 9 [23].

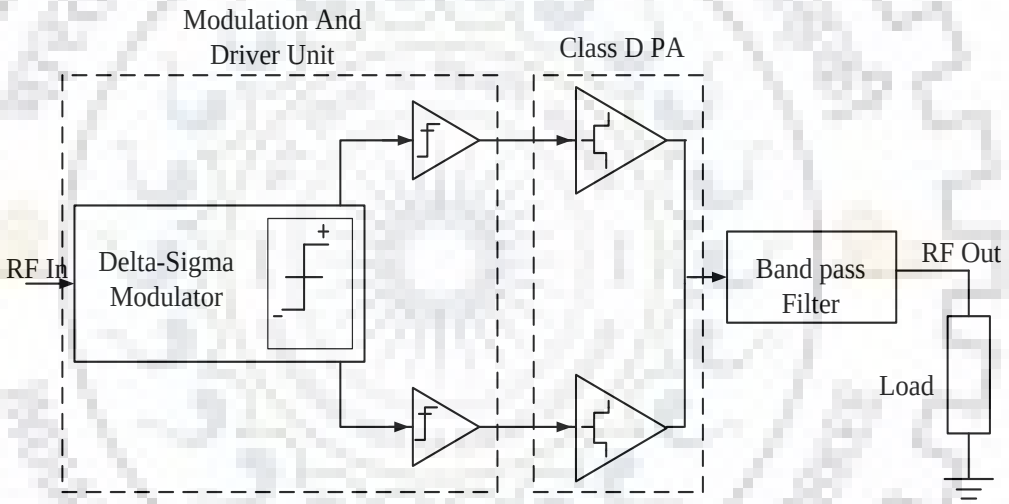

Figure 9 Simplified architecture of Class-S PA.

1.4 Statement of Objective

- Study of explicit derivations of basic theory, drain voltage and drain current waveforms equations of CMCD switch mode PA.
- Design and fabrication of Push-Pull CMCD PA at 2 GHz frequency of operation using a Wolfspeed 10W GaN HEMT ‘CGH40010F’ transistor.

1.5 Thesis Outline

This thesis mainly describes the design of a high efficiency CMCD RF PA. First chapter contains the fundamentals of PAs, their advantages and importance in communication systems. The basic classification of PAs on the basis of biasing point of transistor and mode of operation of transistors. Also a brief discussion about each Class of PAs has been described.

Second chapter is discusses the theoretical background of Class-D PA and different modes of operation of Class-D PA. Brief discussion about two different modes of Class-D PA, Current Mode and Voltage Mode is presented. The operating point and ideal condition of Class-D PA with some basic equations of waveforms are discussed here.

Third chapter explains practical CMCD PA design. Theory of harmonic conditions for CMCD PA and input-output balun used in push-pull configuration are discussed in this chapter. Along with this, evaluation of circuit architecture used so far to design a CMCD PAs are also discussed.

In Chapter four, the design procedure used for this CMCD PA is explained. Steps followed to design and fabricate a CMCD PA at 2 GHz frequency like selecting biasing point, stabilization of device, load calculation for harmonics and input and output matching network design are explained. Design and characteristics of a balun is also described here.

Chapter five contains the results and implementation of designed CMCD PA. Simulated and observed results of drain efficiency, power added efficiency, gain and output power are shown.

Chapter six is the conclusion of so far discussed and explained theory, procedure to design a CMCD PA and results. Future scope of designed CMCD PA is discussed in chapter seven.

CHAPTER 2: THEORY OF CLASS-D OPERATION

2.1 Class-D Operation

The Class-D is a PA in which active device (transistor) is operated as a switch. It means the active device will be operated in saturation region or cut off region. The biasing point of transistor in Class-D PAs is in deep Class-AB or Class-B region. In Class-D PA, two transistors are connected in push-pull configuration and are driven by 180^0 out of phase between the input signals. It means that only one transistor will be ON at a time. There are two type of Class-D PAs one is voltage switching and another is current switching. In voltage switching Class-D PAs the waveforms at intrinsic plane are square voltage and half sinusoidal current wave as shown in Figure 11.

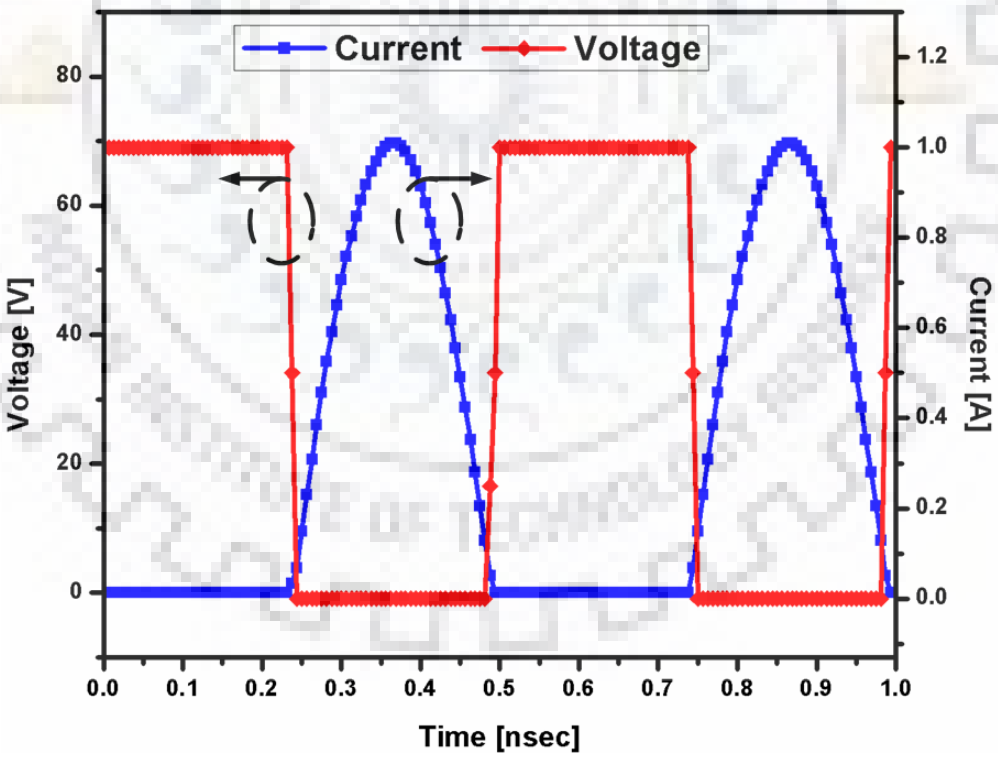

Figure 10 Ideal waveforms of VMCD PA.

Similarly in current switching Class-D PAs square current and half sinusoidal voltage waveforms are observed at intrinsic plane of active devices. By providing the harmonic impedances either open or short circuit the current and voltage waveforms at intrinsic plane dose not overlap and hence the power losses are minimized and overall efficiency of PA increases. Theoretically Class-D PAs have the efficiency of 100%, but in practical circuit due to parasitic reactance and finite switching time, efficiency degrades. The Class-D PA is popular due to relatively simple and easy design relationships equations.

The basic architecture of single ended Class-D PA circuit is shown in Figure 11 and simplified equivalent circuit in Figure 12 [12]. In Figure 11, active device is acting as a switch, L_{ch} is the RF choke to isolate DC power from RF circuit, C_b is the bypass capacitor required to bypass the AC signals present in drain biasing network, and C_0 is the blocking capacitor which blocks the DC power from mixing with RF power and a series load. The current i_R represents the load current which is assumed to be sinusoidal. For operating device in switched mode, it is essential to offer idealized optimum conditions for a zero-power loss in the transistor.

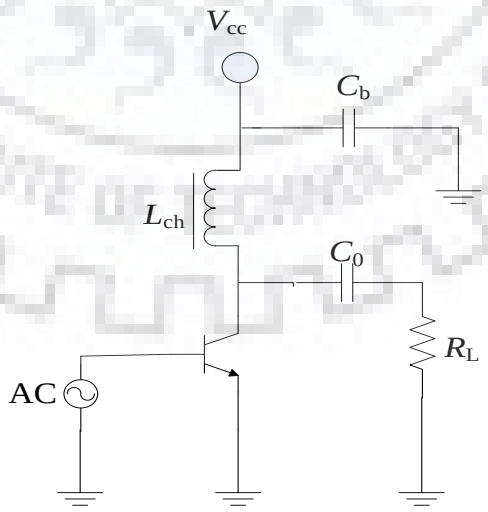

Figure 11 Single ended Class-D circuit.

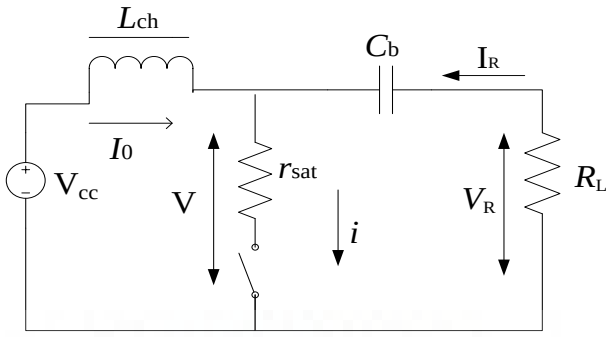

Figure 12 Simplified equivalent circuit of single ended Class-D PA.

Based on this equivalent circuit, theoretical analysis of operation condition for single ended switch mode Class-D PA can be carried out. In this circuit the active device is operating as a switch, with the saturation resistance between drain and source as r_{sat}. The device is driven in such a way that it will switch between its saturation (ON) and cut off (OFF) condition with an assumption of 50% duty cycle.

When switch is ON for $0 \leq \omega t \leq \pi$ [12],

$$i(\omega t) = I_{\max} = \frac{V_{cc} + R_L I_0}{R_L + I_0} \tag{2.1}$$

$$v(\omega t) = V_{sat} = r_{sat} I_{\max} \tag{2.2}$$

$$i_R(\omega t) = I_0 \tag{2.3}$$

$$v_R(\omega t) = R_L I_0 \tag{2.4}$$

Where V_{sat} is the saturated drain voltage, I_0 is the DC current, R_L is the load resistance and I_{max} is peak drain current.

When device is OFF for $\pi \leq \omega t \leq 2\pi$ [12],

$$i(\omega t) = 0 \tag{2.5}$$

$$v(\omega t) = V_{\max} = V_{cc} + R_L I_0 \tag{2.6}$$

$$i_R(\omega t) = -I_0 \tag{2.7}$$

$$v_R(\omega t) = -R_L I_0 \tag{2.8}$$

Where V_{max} is peak drain voltage.

Drain voltage, drain current and load current are rectangular waveforms as shown in Figure 13. It shows that when there is maximum drain voltage then drain current will be minimum (ideally zero) and when drain current is maximum then drain voltage is minimum. The drain voltage can only attain the minimum value of V_{sat} and can't be zero like drain current, this is because the active device is not a perfect switch and there will be some voltage drop across its drain and source terminals. In other words there will be some saturation resistance (r_{sat}) between drain and source of active device when operating in saturation region.

Figure 13 is showing the switch mode operation of active device which is the basic requirement for Class-D operation.

By taking the Fourier transform of equation (2.1) DC current I_0 can be obtained from

$$I_0 = \frac{1}{2\pi}\int_0^{\pi} i(\omega t) d(\omega t) = \frac{V_{cc}}{R_L + r_{sat}}\left(1 + \frac{r_{sat}}{R_L + r_{sat}}\right)^{-1} \tag{2.9}$$

The fundamental drain current component I can be obtained using

$$I = \frac{1}{\pi}\int_0^{\pi} i(\omega t)\sin(\omega t) d(\omega t) = \frac{4}{\pi} I_0 \tag{2.10}$$

We considered as $I_{max} = 2I_0$, the output power for fundamental-frequency can be calculated by

$$P = \frac{1}{2} I^2 R_L = \frac{8}{\pi^2} \frac{R_L}{\left(R_L + r_{sat}\right)^2} \frac{V_{cc}^2}{\left(1 + \frac{r_{sat}}{R_L + r_{sat}}\right)^2} \tag{2.11}$$

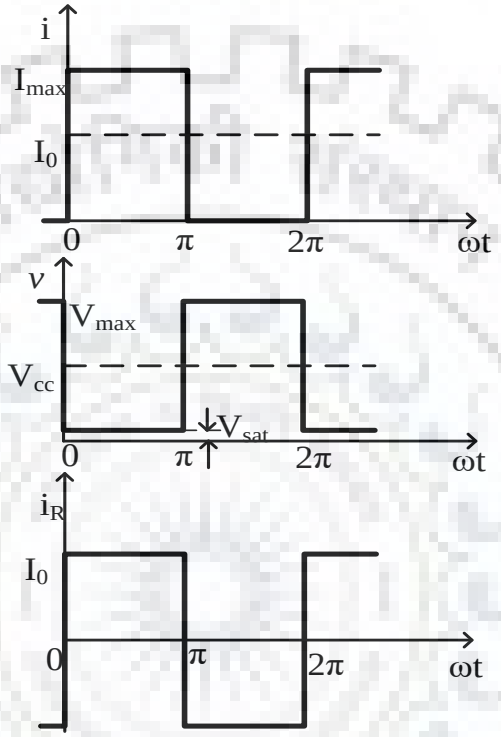

Figure 13 V-I waveforms of single ended Class-D PA.

2.1.1 VMCD PA

In VMCD PA circuit, two active devices should be connected in push-pull configuration [24-29]. It is a common emitter connection of two transistors. Both the transistors are driven 180^0 out of phase by inverting the secondary winding of input transformer. A balun can also be used to give 180^0 phase shift between two input signals. By giving two out of phase inputs it is ensured that only one transistor is operating for half cycle and another one for the next half cycle. If transistors are true complementary (one is P-Type and another is N-Type) then there is no need of reversing the secondary winding of

input transformer. Figure 14 [12] shows simplified architecture of circuit of a VMCD PA, where C_b is bypass capacitor used to bypass AC signals to ground in biasing circuit of the PA. C_0 is blocking capacitor used to block the DC power from mixing with RF power and R_L is a load resistance.

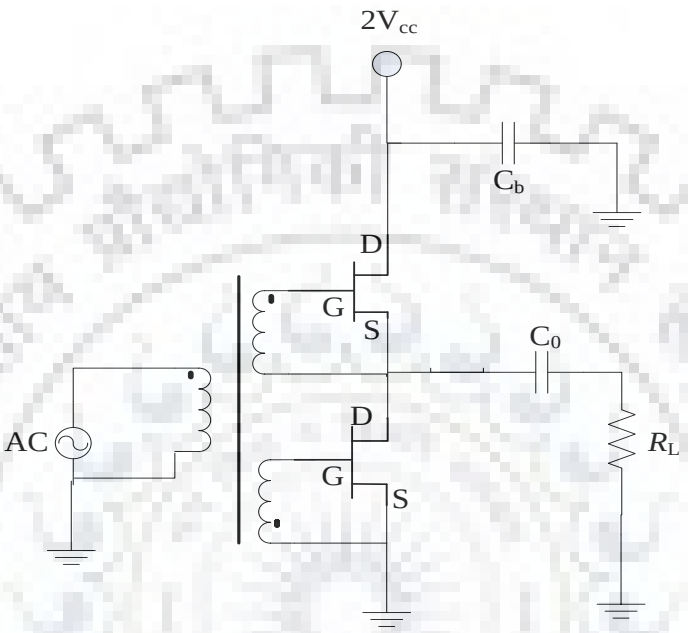

Figure 14 VMCD PA circuit diagram.

In Figure 15 equivalent circuit of VMCD PA of Figure 14 is shown where each transistor is replaced with a switch and have a saturation resistance (r_{sat}).

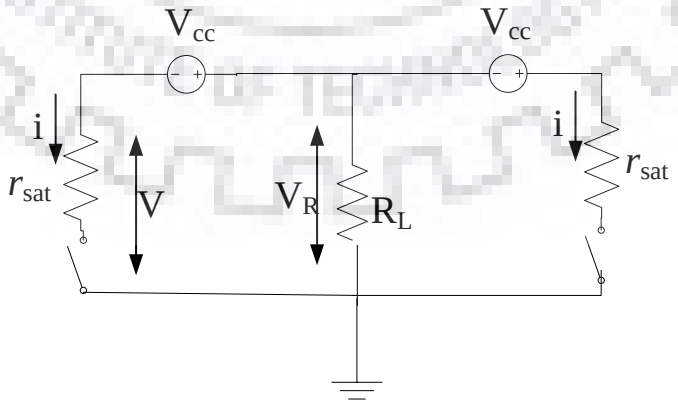

Figure 15 Equivalent circuit of VMCD PA.

Load voltage, device drain current and voltage across device drain and source terminal is shown in Figure 16. It can be observed that load voltage is a square wave, proving VMCD operation.

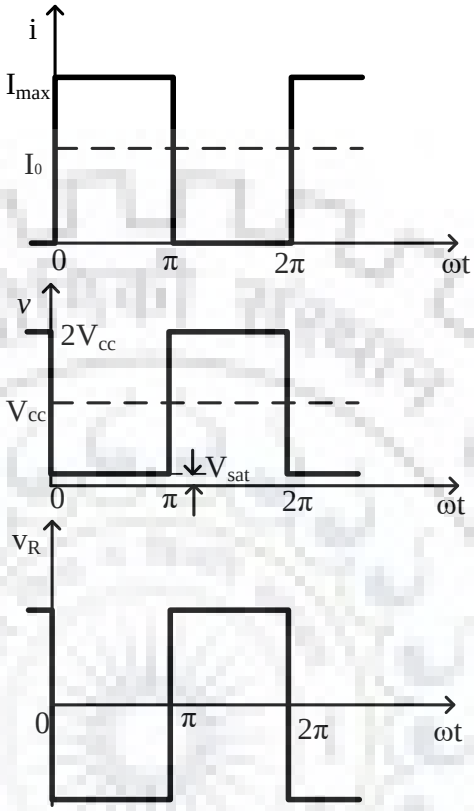

Figure 16 V-I waveforms of VMCD PA.

For theoretical analysis of VMCD PA a simplified equivalent circuit is considered as shown in Figure 16. The transistors here are driven in such a way that they will switch between ON and OFF condition alternatively with an assumption of 50% duty cycle. Here the important point to notice is that for VMCD only the duty cycle of less than or equal to 50% is acceptable. If duty cycle is greater than 50% then both the devices will be in ON state for small period of time, and a large amount of current will flow. This is because of a very low saturation resistance ($2r_{sat}$) between drain and source terminals of transistor in saturation. This will cause large power dissipation and eventually the efficiency of PA will decrease.

Now let us consider the small signal equivalent circuit of VMCD PA of Figure 16.

When the left side device is ON for $0 \le \omega t \le \pi$ [12]

$$i(\omega t) = I_{\max} = \frac{V_{cc}}{R_L + r_{sat}} \tag{2.12}$$

$$v(\omega t) = V_{sat} = r_{sat} I_{\max} \tag{2.13}$$

$$v_R(\omega t) = -R_L I_{\max} \tag{2.14}$$

When the left side device is OFF for $\pi \le \omega t \le 2\pi$

$$i(\omega t) = 0 \tag{2.15}$$

$$v(\omega t) = V_{\max} = V_{cc}\left(2 - \frac{r_{sat}}{R_L + r_{sat}}\right) \tag{2.16}$$

$$v_R(\omega t) = V_R = R_L I_{\max} \tag{2.17}$$

Now again taking Fourier transform of Eq. (2.12) to obtained the dc current I_0

$$I_0 = \frac{1}{2}\frac{V_{cc}}{R_L + r_{sat}} \tag{2.18}$$

The fundamental output power using (2.12) and (2.17) can be calculated as

$$P = \frac{8}{\pi^2}\frac{V_R^2}{R_L} = \frac{8}{\pi^2}\frac{R_L}{(R_L + r_{sat})}V_{cc}^2 \tag{2.19}$$

In Figure 16 drain current, drain voltage and load voltage waveforms are shown. It demonstrates that when there is maximum drain voltage, drain current will be minimum (ideally zero) and when drain current is maximum, drain voltage is minimum. The voltage drop across load resistance is square wave switching between positive and negative values, hence it confirms the VMCD operation of PA.

2.1.2 Current Mode Class-D (CMCD) PA

In CMCD PA circuit, both the devices should be connected in push-pull configuration [30-31]. In CMCD PA, source terminal of both the transistors are tied together to the ground and two drain supplies are needed. In CMCD both the transistors are driven in 180^0 phase shift by inverting the secondary winding of input transformer. A balun can also be used to produce 180^0 phase shift in two input signals. By giving two out of phase inputs it is ensured that only one transistor is operating for half cycle and another one for next half cycle. If transistors are true complementary (one is P-Type and another is N-Type) then there is no need of reversing the secondary winding of input transformer. Figure 17 [12] shows simplified circuit architecture of a CMCD Push-Pull PA, where C_b is bypass capacitor used to bypass the AC signals to ground in biasing circuit of the PA, C_0 is blocking capacitor used to block DC power from mixing with RF power and R_L is a load resistance.

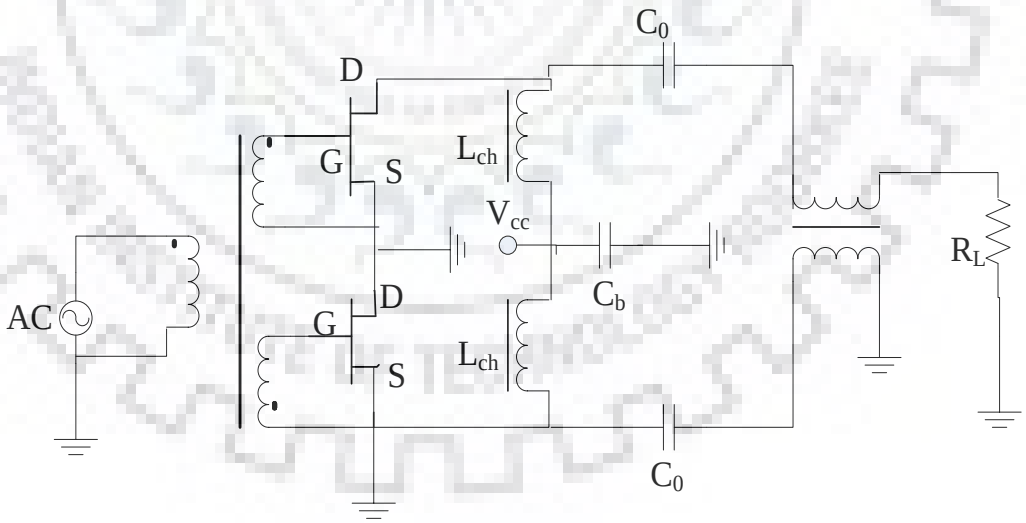

Figure 17 CMCD PA circuit diagram.

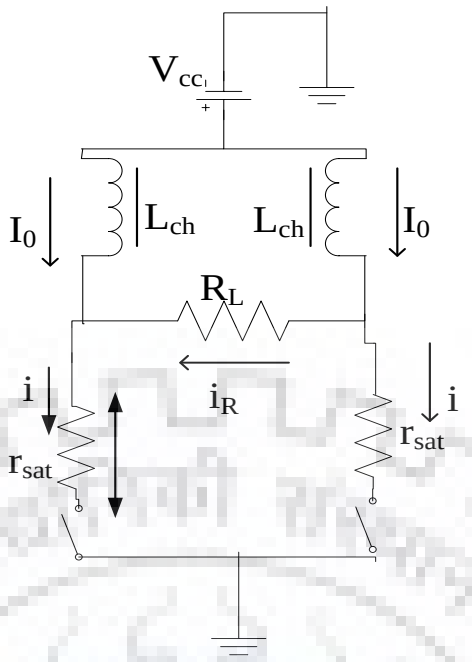

Figure 18 Equivalent circuit of CMCD PA.

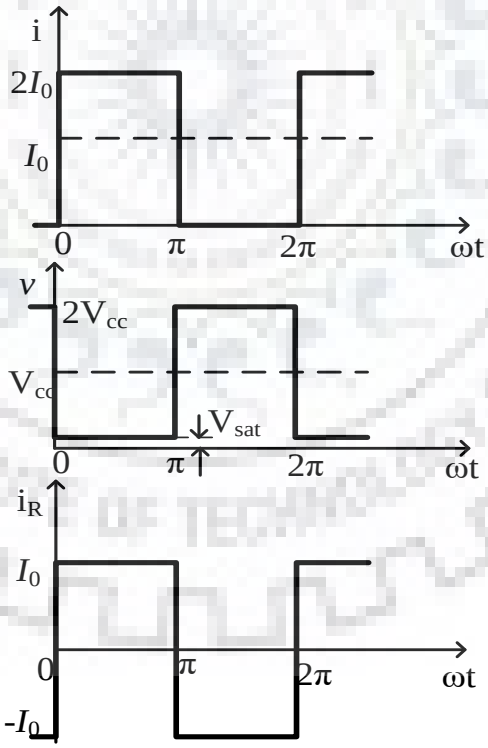

Figure 19 V-I waveforms of CMCD PA.

For theoretical analysis of CMCD PA the equivalent circuit is considered as shown in Figure 18. Where each transistor is replaced with a switch and a saturation resistance (r_{sat}). The transistors here are driven in such a way that they will switch between ON and OFF condition alternatively with an assumption of 50% duty cycle. It is important to notice that for CMCD only the duty cycle of greater than or equal to 50% is acceptable. If duty cycle is less than 50% than both the devices will be in OFF state for small period of time and due to the choke current a large voltage drop across drain and source terminal of transistor will be produced which may cause to the device breakdown. Now let us consider the small signal equivalent circuit of CMCD PA shown in Figure 18.

When the left side device is ON for $0 \le \omega t \le \pi$ [12]

$$i(\omega t) = I_{\max} = 2I_0 \tag{2.20}$$

$$v(\omega t) = V_{sat} = r_{sat} I_{\max} \tag{2.21}$$

$$i_R(\omega t) = I_R = I_0 \tag{2.22}$$

When the left side device is OFF for $\pi \le \omega t \le 2\pi$

$$i(\omega t) = 0 \tag{2.23}$$

$$v(\omega t) = V_{\max} = (R_L + 2r_{sat})I_0 \tag{2.24}$$

$$i_R(\omega t) = -I_0 \tag{2.25}$$

Applying Fourier transform to (2.21) and (2.24) DC supply voltage can be obtained using

$$V_{cc} = \frac{1}{2\pi}\int_0^{2\pi} v(\omega t) d(\omega t) = \frac{V_{\max} + V_{sat}}{2} \tag{2.26}$$

And DC current I_0 can be calculated from

$$I_0 = \left(\frac{1}{2} + 2\frac{r_{sat}}{R_L}\right)^{-1} \frac{V_{cc}}{R_L} \tag{2.27}$$

Now the output power of fundamental frequency can be written using (2.22) and (2.27) as

$$P = \frac{8}{\pi^2} I_R^2 R_L = \frac{8}{\pi^2}\left(\frac{1}{2} + 2\frac{r_{sat}}{R_L}\right)^{-2} \frac{V_{cc}^2}{R_L} \tag{2.28}$$

Drain efficiency will be maximum when saturation resistance (r_{sat}) becomes zero and can be calculated from (2.9), (2.11), (2.18), (2.19), (2.27), and (2.28).

$$\eta = \frac{P}{P_0} = \frac{8}{\pi^2} \cong 0.81 \tag{2.29}$$

From equation (2.29) it can be observed that 19% of total output power is the harmonic power.

CHAPTER 3: PRACTICAL CURRENT MODE CLASS-D PA

3.1 Basics of CMCD PA operation:

Figure 20 shows the basic circuit diagram of CMCD PA. It can be observed that the output network of push-pull RF Class-D PA consists of two active devices (transistors), a parallel *RLC* harmonic shunt tank and RF chokes (*RFC*s). The two transistors act as a switching device with either square voltage wave (VMCD) or square current wave (CMCD). Ideally, the Class-D PA can attain a drain efficiency of 100%, but the parasitic components of the device like, C_{ds} and inductance L, can cause the losses as $0.5C_{ds}V^2$ and $0.5LI^2$ respectively. This is because of their charging and discharging processes [1-5] and [32]. The efficiency also degrades due to other device related parameters. For example the ON-resistor of the device (R_{ON}) and saturation voltage of transistor (V_{sat}) also should have low values.

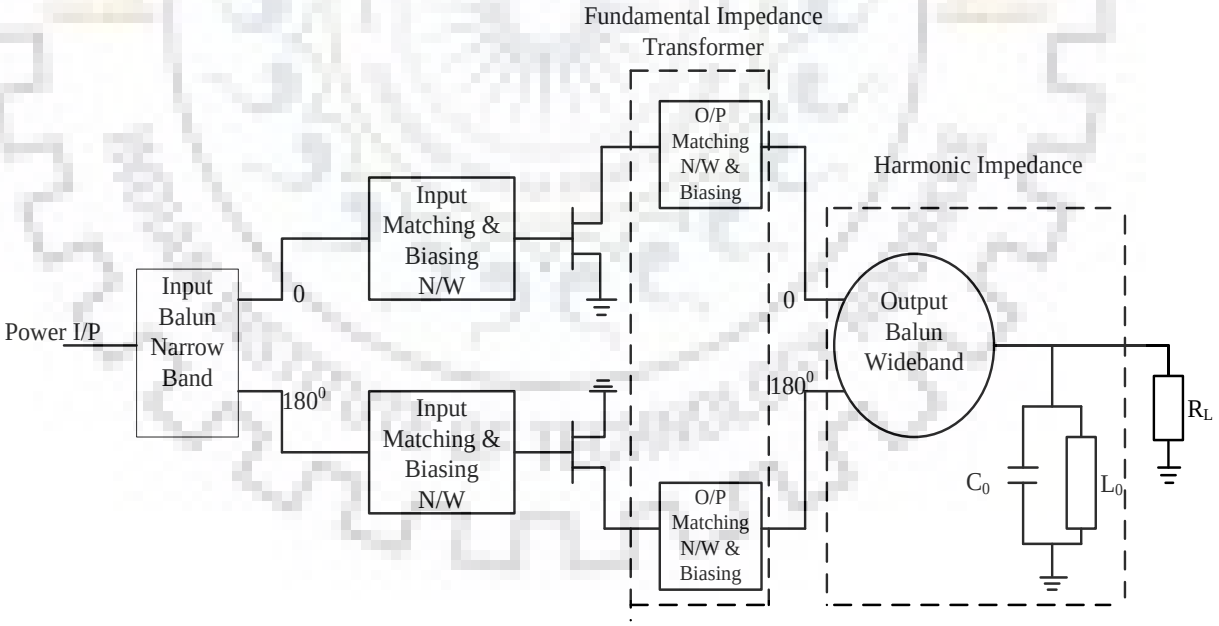

Figure 20 Typical circuit diagram of practical CMCD PA.

To operate transistor as a switch and to produce the square waveforms, its switching frequency should be at least 10 times lower than its gain cut-off frequency (f_T) to allow its spectrum to generate higher order harmonics. The wideband balun provides the infinite impedance at even harmonics at output and the parallel *RLC* shunt tank provides a short-circuit at output of two transistors at odd harmonic frequencies as it is tuned to the fundamental frequency. By providing open circuit at second harmonic and short circuit at third harmonic the drain current is shaped as square and drain voltage is shaped as half sinusoidal waveforms [33-34]. For one of the transistors, the time domain current and voltage waveforms of CMCD PA are as shown in Figure 21. There will be 180^0 phase shift in waveforms of another transistor since both the transistors are driven 180^0 out of phase input by means of a balun at input terminal.

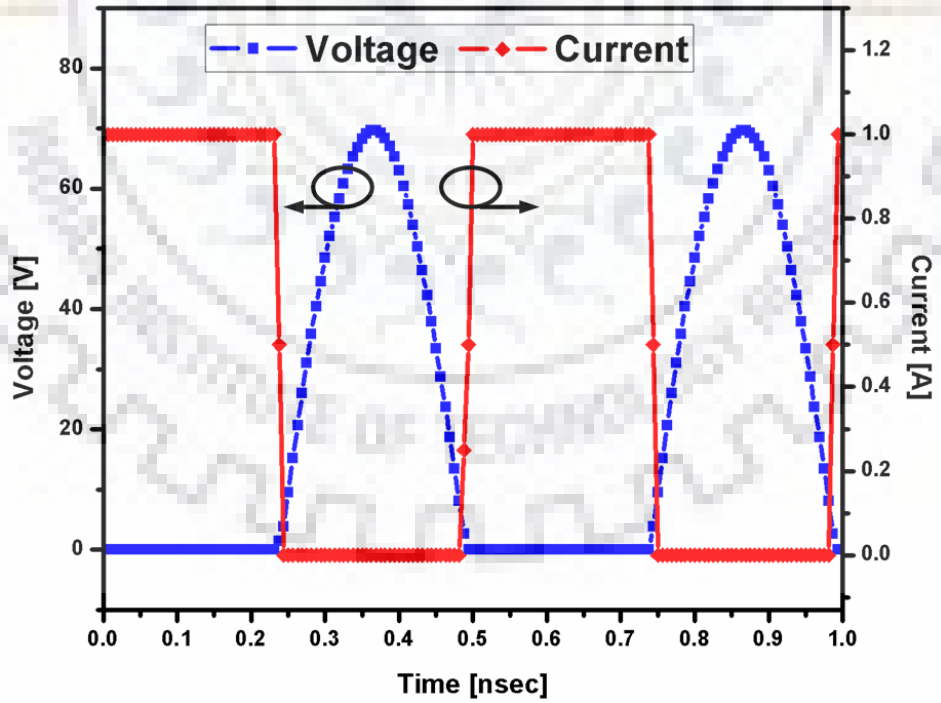

Figure 21 Ideal waveforms of CMCD PA.

By using another balun at output, both the amplified out of phase signals are combined and higher frequency component are filtered using shunt RLC resonator and only fundamental component will be allowed to pass through. As balun provides open circuit at even harmonics these harmonic components will also suppressed. Although by using a wideband balun and a shunt harmonic tank one can ensure that proper impedance has been provided to the output terminals of two active devices (transistors). But for maximum efficiency, a load matching network should transforms a 50Ω load to required fundamental load impedance of transistors. A wideband balun provides the required 180^0 phase shift between its output terminals up to at least 3^{rd} harmonic. This topology is mostly used at low frequency operation as it is easier to design wideband transformers at low frequencies. The problem of designing a wideband balun can be solved by moving the shunt tank to the balanced ports from the unbalanced port of balun [6] and [35-38]. This new design is shown in Figure 22. A parallel *LC* shunt resonator in this structure short circuits the third harmonic component. Because of this, the bandwidth required for balun is reduced. The shunt resonator used here can be realized either by using a chip inductor [37], an air-wound inductor [39] or high impedance transmission lines [40-41] along with a chip capacitor. Capacitor C_0 partially absorbs the output capacitances, this is another advantage of this topology at microwave frequencies. Firstly, this minimizes the capacitance losses of VMCD PA which are frequency dependent, also it makes design less affected by the component tolerance.

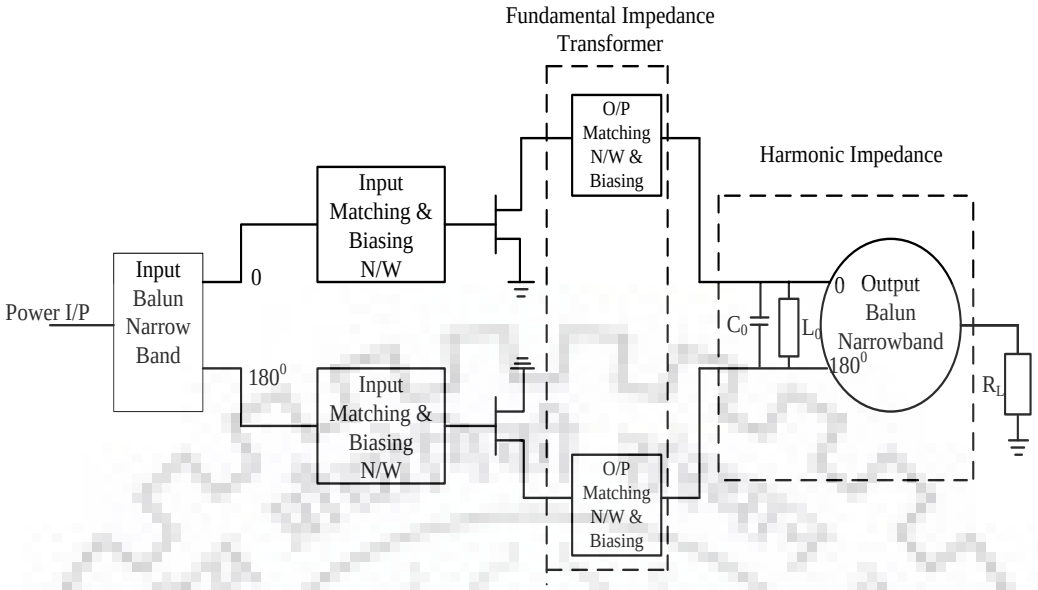

Figure 22 Architecture of CMCD PA using a narrow band balun.

The main problem in implementing the shunt tuned tank using lumped elements is that, its self-resonant frequency (f_{res}) which is higher than third harmonic component. These uncontrolled impedances degrades the efficiency of PA. To overcome this problem, an enhanced CMCD architecture is used which is appropriate for design at high frequencies of operation. In this architecture, a multi-impedance distributed output load matching network has been used (Figure 23) which makes the performance of CMCD PA independent of shunt tuned tank and balun at higher harmonic frequencies.

To obtain the rectangular drain current and sinusoidal drain voltage waveforms as shown in Figure 21, the impedances provided by multi-harmonic load matching network ideally should be Z_{opt} (optimum impedance for maximum efficiency) at fundamental frequency, $Z = \infty$ at even harmonics and $Z = 0$ at odd harmonics.

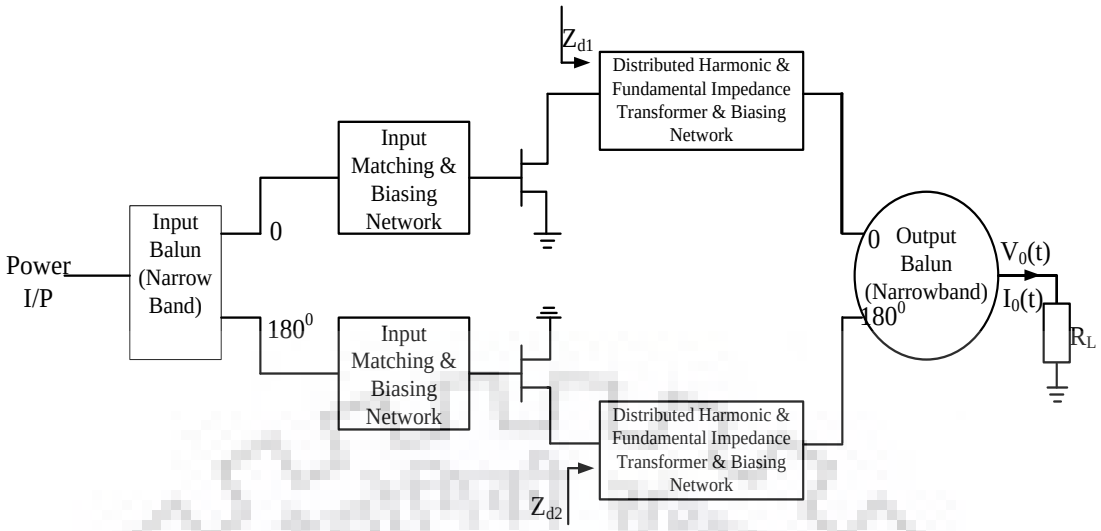

Figure 23 Enhanced architecture of CMCD PA.

Based on the harmonic conditions of CMCD PA [33].

$$I_{ds}(\theta) = I_{dc} + I_{1m}\sin\theta - I_{3m}\sin 3\theta ... \tag{3.1}$$

$$V_{ds}(\theta) = V_{dc} - V_{1m}\sin\theta - V_{2m}\sin 2\theta ... \tag{3.2}$$

The ideal waveforms of CMCD PA after providing the proper harmonics impedances are shown in the Figure 21. The current waveforms will be a square and voltage will be a half sinusoidal.

3.2 Balun design

As shown in the circuit diagram of enhanced structure of practical CMCD PA, a balun is required at input and output sides of the PA. Many times in microwave circuits it is required to convert the unbalanced signal to balanced differential signals. In such situations, baluns are very important components. For example in push-pull PAs, balanced antennas, balanced mixers, microwave leaky-wave antennas baluns are widely used. It is easy to

implement planer baluns and also they exhibit good performance. Over the coupled line baluns [42] and Wilkinson power divider [43] the baluns designed with transmission line sections [44-47] are more in use because of its simpler design [42].

In the design of CMCD PA, the balun used is a rat-race coupler [47] as shown in the Figure 24.

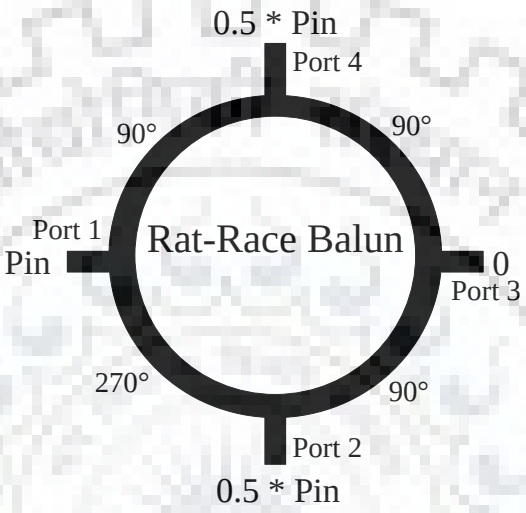

Figure 24 Rat-race coupler.

All the ports have been terminated with the characteristic impedance Z_0 (= 50Ω). Six quarter wave length transmission line having the characteristic impedances $Z = Z_0\sqrt{2}$ have been used to design this coupler. Port 1 is used as input port and coupled with port 2 and port 4. Output power level at port 2 and port 4 of this coupler is half of the input power level at port one. Also this coupler gives the phase difference of 180^0 between the coupled ports (2 and 4) which is a required characteristic of a balun.

The simulated S-parameters of designed balun are shown below. Insertion loss (S_{21} and S_{31}) and isolation between port 2 and 4 (S_{42}) of the balun as shown in Figure 25 at 2 GHz was about -3 dB and -35 dB respectively. Return loss at all 4 ports of balun as shown

in Figure 26 is less than 40 dB at 2 GHz frequency. The phase difference of output signals between port 2 and 4 as shown in Figure 28 is almost 180^0 at 2 GHz frequency.

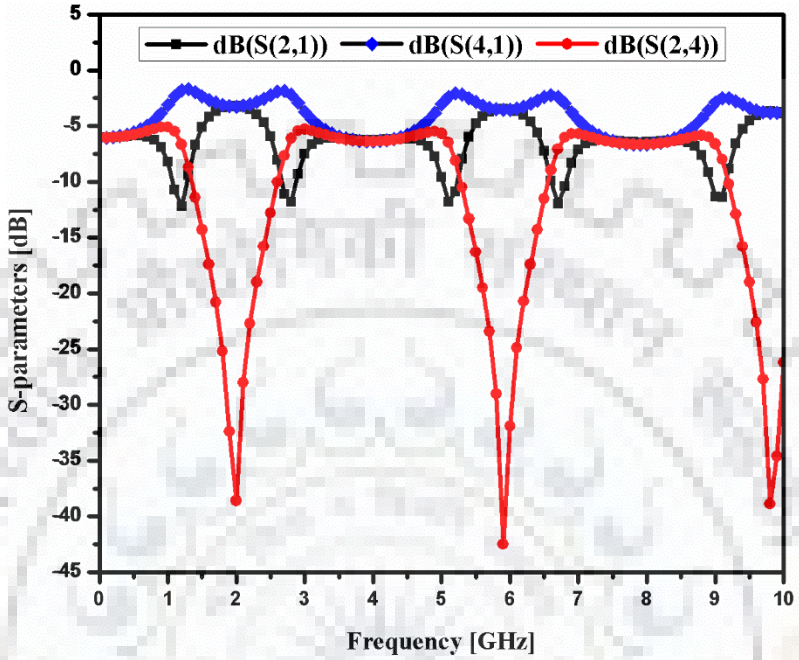

Figure 25 S-parameters (S_{21}, S_{41} and S_{24}) of designed balun.

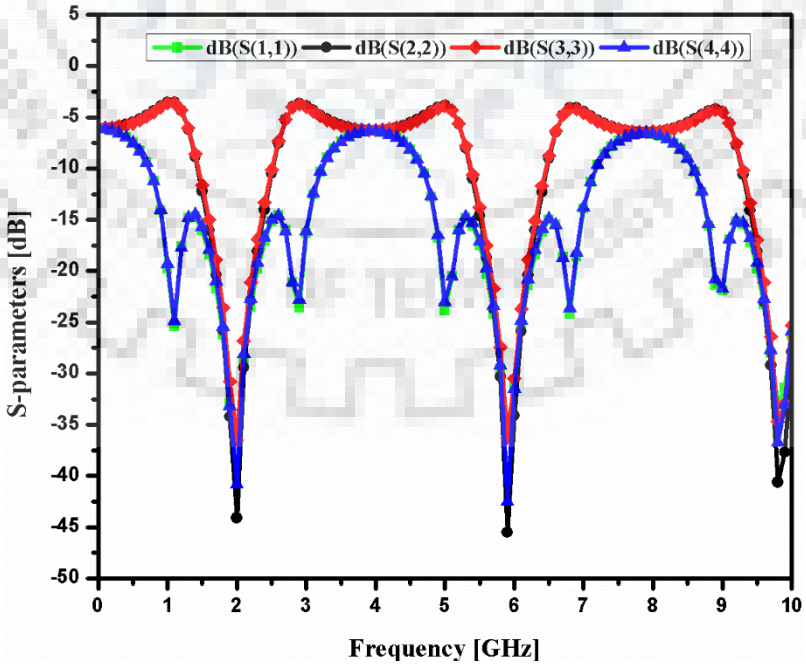

Figure 26 S-parameters (S_{11}, S_{22}, S_{33} and S_{44}) of designed balun.

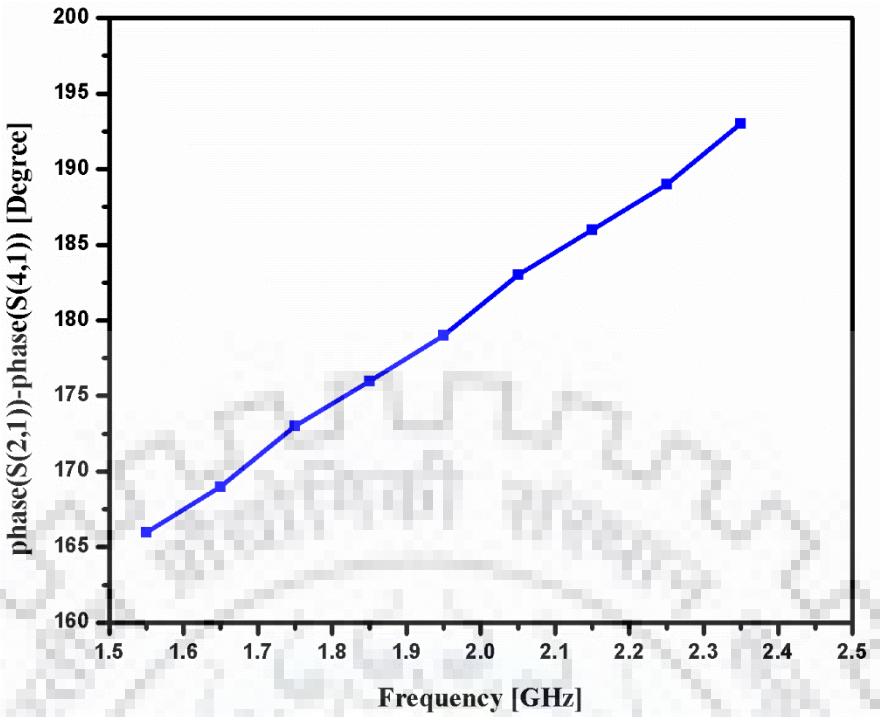

Figure 27 Phase difference between port 2 and 4 of designed balun.

CHAPTER 4: DESIGN OF CMCD PA

After analyzing and understanding the basic theory of CMCD PA, the design procedure has been done. Steps followed during the design are illustrated in this chapter. All the simulations for this design has been done on Keysight's Advanced Design system (ADS).

4.1 Device Selection

Because of low efficiency at high RF, Class-D PA was scarcely designed for long time. This degradation is due to large output capacitance of the transistor. This problem can be solved by using GaN-HEMTs which has low output shunt capacitance. Basic characteristics of GaN HEMTs are low parasitic capacitances, high break-down voltage and high power density. These characteristics are the main requirements of high frequency and high power designs of PAs. Also the ON-state resistance (R_{ON}) of GaN HEMTs is very low which significantly reduces the power loss when it is operated as a switch. For designing the CMCD PA of high efficiency at 2 GHz frequency, device used was CGH40010F from Wolfspeed. It is a 10 W Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT). The CGH40010F, operating at a 28 V. The CGH40010F is ideal for linear and compressed RF PA circuits.

4.2 The biasing and stabilization of device

After selecting the device for implementation next thing to do is to set the biasing point of the device for PA. As defined earlier, the Class-D PA is a switched mode PA in which device is operated as a switch so the biasing point should be close to pinch-off region. Also keeping in mind that for CMCD PA, the duty cycle for each device should be greater

than or equal to 50%. Considering all these facts the biasing point is selected using DC-IV characteristics. The design parameters of CMCD PA is listed in Table 1.

Table 1 Different parameters and their values for designed PA.

S.No.	Parameter	Value
1.	V_{ds}	28 V
2.	V_{gs}	-3.0 V
3.	I_{ds}	65 mA
4.	P_{out}	10 W
5.	Pinch off	-3.4 V
6.	Frequency	2 GHz

Stabilization of the device is very essential in PA designing. After biasing, it is necessary to check the stability of device. If device is not stable that means the load and source stability circles are present inside the smith chart so, a stability circuit has to be used to stabilize the device at designed frequency. In this design, a parallel RC circuit is used at input side of the PA to stabilize the device.

4.3 Calculation of Load Impedances

The device has been selected and biasing point has been set, now it is required to obtain the fundamental and harmonic loads at output of the device to maximize the efficiency and maintain the proper waveforms shapes at intrinsic plane of the device. Using Load-Pull simulations in ADS the optimum load impedances at fundamental frequency was

found for optimum efficiency of single-ended PA. Then for maximum efficiency, phase of reflection coefficient up to third harmonic was set. Starting from the basic theoretical conditions of short circuit at third harmonic frequency ($3f_0$) and open circuit at second harmonic frequency ($2f_0$). To operate in Class-D, the phases of harmonics impedances at output of transistor can only vary near the theoretical value. After few iterations, the measured impedances of multi-harmonic load-pull measurement setup are listed in Table 2.

Table 2 Impedances at harmonic frequencies at output side of PA.

S. No.	Frequency (GHz)	Load Impedances (Ω)
1.	2	30.4 +j23.3
2.	4	0 + j17.75
3.	6	0 – j60

The obtained multi-harmonic impedance termination using load-pull measurement has been verified and optimized by a switch based large signal device model at intrinsic terminals of transistors and thus the waveforms at intrinsic plane of transistor. For this all the parasitic effects was considered for optimal Class-D operation. From these impedances at the output of the PA, impedances at the intrinsic plane of device are as shown in Figure 28.

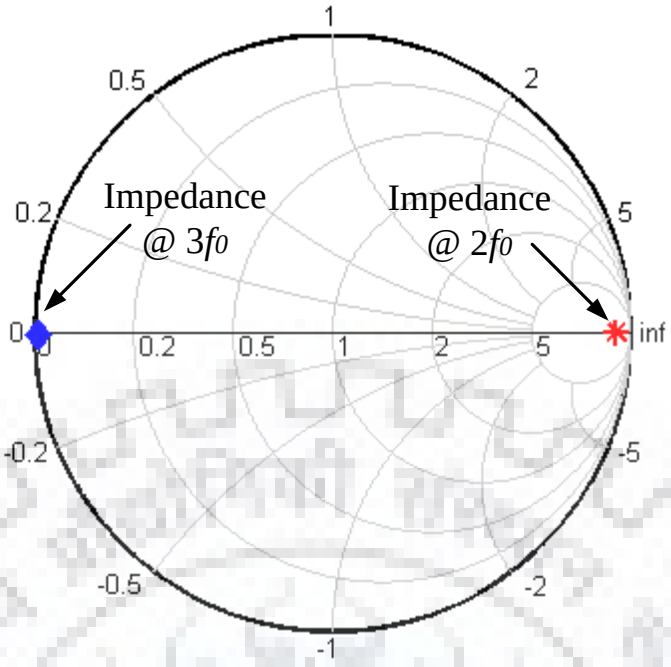

Figure 28 Impedances at intrinsic plane of the device.

4.4 Output Matching Network

Output matching has notable effect on output power of amplifier. For the required harmonic control at intrinsic plane of the device and for optimum efficiency impedances at output terminal has been calculated using load–pull technique in ADS. A matching network is required to provide these impedances to the device at output side. As discussed earlier, this design of CMCD PA is based on enhanced structure. To provide these different impedances at different frequencies, a multiband matching network was designed at output side of the PA [48]. In multiband matching network, different impedances can be matched at different frequencies. Second harmonic impedance was first matched and then third harmonic. The fundamental impedance was matched at last to a 50Ω load. In Figure 29 block diagram of multiband matching network at output side of PA has been shown. The transmission line TL1 and a short circuited stub line TL2 was used to match the second harmonic. Third harmonic was matched using TL3 and an open circuit stub line TL4. At

last transmission line TL5 and TL6 was used to match the fundamental impedance to a load of 50Ω.

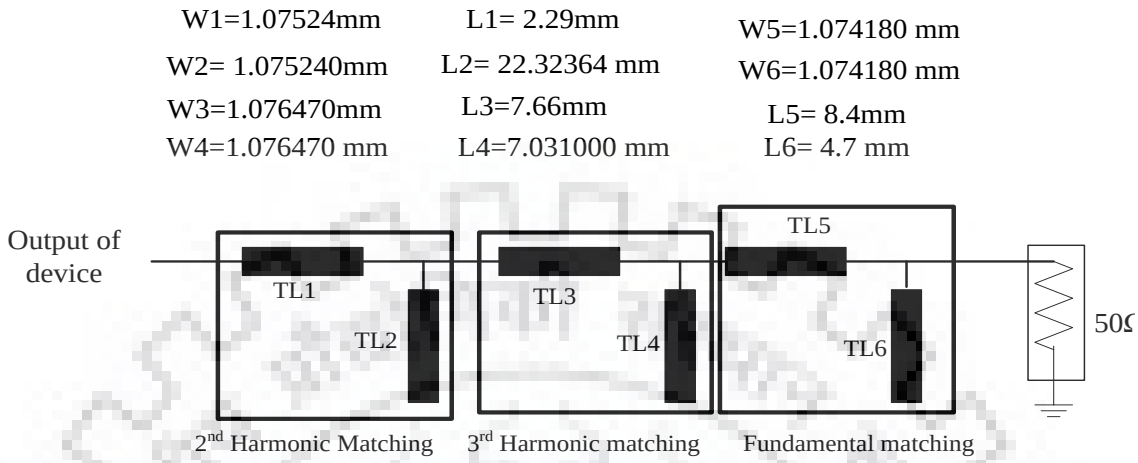

Figure 29 Output matching network for designed PA.

Change in biasing network design according to requirement, an open for second harmonic and a short for fundamental load are provided as shown in Figure 30. The radial stub is constructed from a series of straight micro strip section of various width that are cascade together, number of sections depend upon frequency.

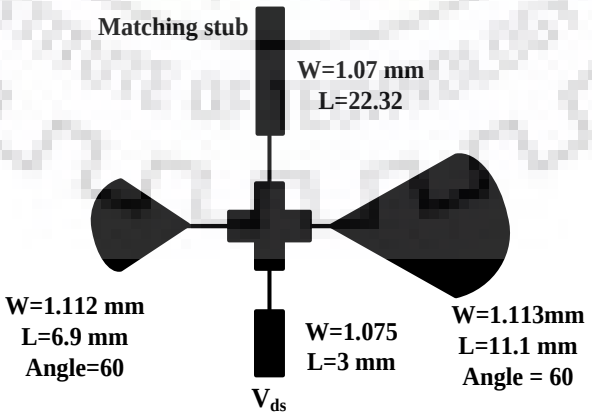

Figure 30 Modified drain biasing circuit for designed PA.

4.5 Input Matching Network:

The input impedance matching has significant effect on gain and efficiency of PA. For no reflection of power at input port of device conjugate matching have to be done. Input impedance is calculated by load pull simulation corresponding to fundamental which is calculated in above section and tuned such that the efficiency and gain can be boosted. Finally, input impedance is matched with 50Ω such that the gate of the transistor sees the required impedance. In Figure 31, the block diagram of input matching network design has been shown using single stub matching technique and converted ideal stub by real line.

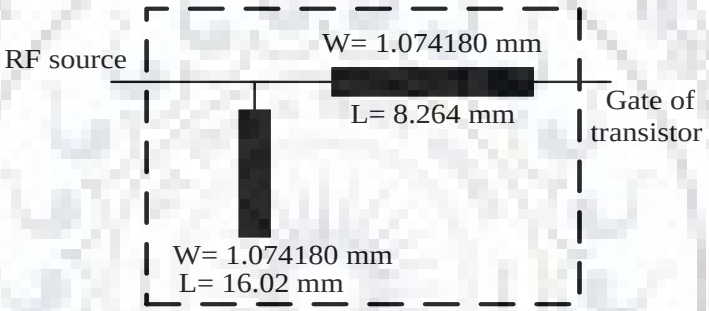

Figure 31 Input matching network for designed PA.

4.6 Complete Circuit Diagram

High efficiency CMCD PA in push-pull configuration has been designed using 10 W GaN HEMT transistor CGH40010F from Wolfspeed. The transistor is biased in deep Class-AB region with drain voltage V_{ds} and drain current I_{ds} of 28 V and 65 mA respectively. The proposed switch mode Class-D PA was fabricated using Rogers RO4350 substrate with dielectric constant (ε_r) equal to 3.66 and 20 mil height. Packaged device is stabilized by connecting parallel *RC* circuit. Input matching network is based on single stub matching at fundamental frequency. Output matching network consists of multiband matching sections

as shown in Figure 32. The impedance for fundamental and harmonic frequencies at output terminal of transistor was obtained by using load-pull technique in ADS.

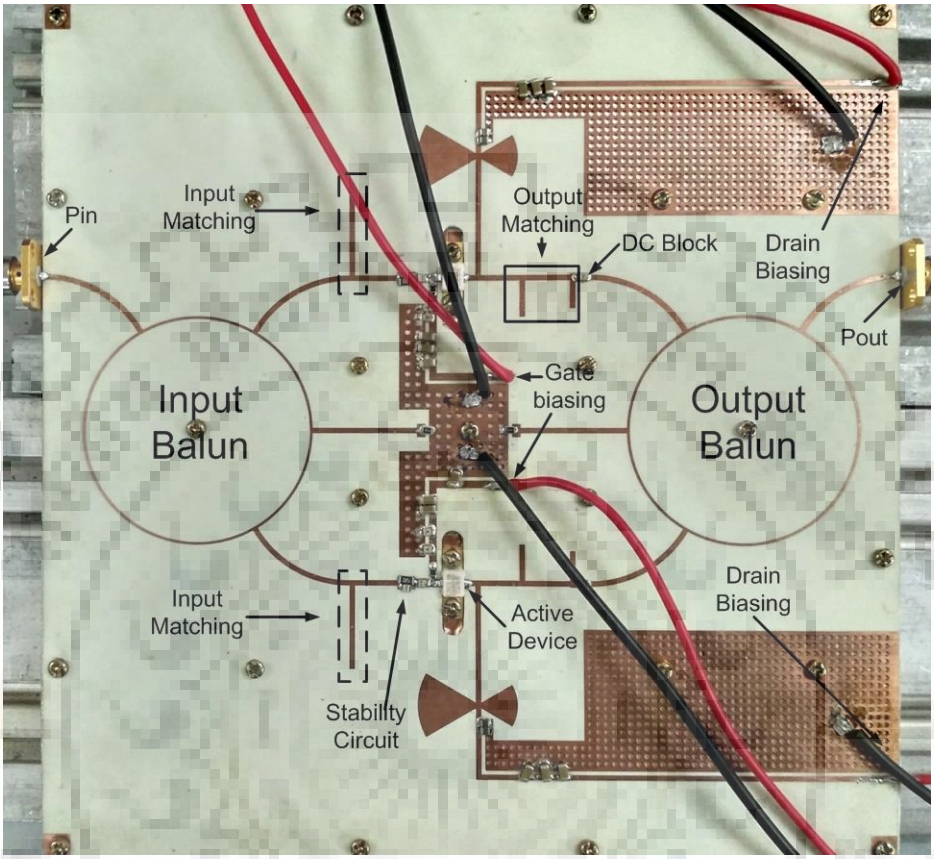

Figure 32 Photograph of complete fabricated PA.

Two single ended Class-D PAs are combined to make a push-pull configured CMCD PA. A rat race coupler is used as balun at input side of the PA to provide half power division with 180^0 phase shift between two inputs of push pull PA. At the output side of the circuit, balun is used for combine two out of phase signals to generate complete waveforms. Also the power of two outputs are combined by output balun.

CHAPTER 5: IMPLIMENTATION AND RESULTS

After the fabrication of designed CMCD PA, it was tested with single tone continuous wave signal from 1.9 GHz to 2.1 GHz. The simulated waveforms at intrinsic plane of device are shown in Figure 33. It is observed that these waveforms are slightly distorted from ideal waveforms as only up to 3rd harmonic was considered for design. These are very much similar to ideal waveforms and thus validate the Class-D mode of operation. In Figure 34 measured and simulated PAE, DE and Gain vs. input power are shown. The simulated results show the maximum DE of 72% and PAE of 67%. The corresponding measured DE and PAE are 71.5% and 65.5% respectively. These efficiencies are measured at saturation where the gain compression is 3 dB at saturation, the simulated and measured gain are 11.6 dB and 11.1 dB respectively. Figure 35 shows the simulated and measured results over the 100 MHz band around center frequency of 2 GHz.

Table 3 Results of fabricated PA.

Parameter	Simulated Results	Measured Results
Frequency	2 GHz	2 GHz
Gain	11.7 dB	11.1 dB
Drain Efficiency	72%	71.5%
PAE	66.5%	65.5%
P_{out}	42.7 dBm	42.54 dBm

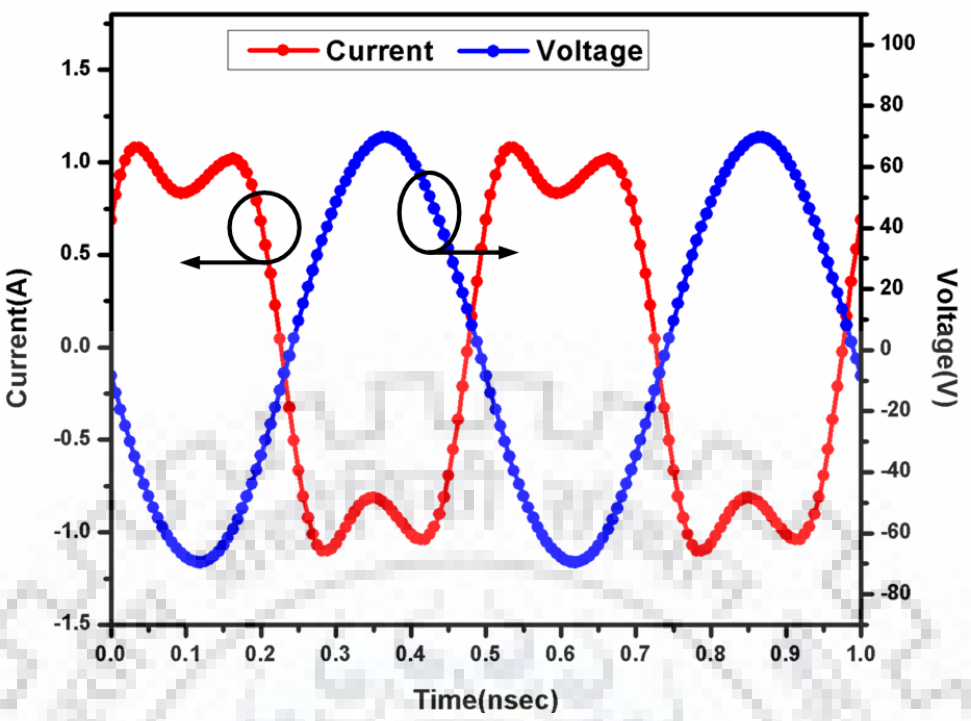

Figure 33 Simulated current and voltage waveforms at intrinsic plane of device.

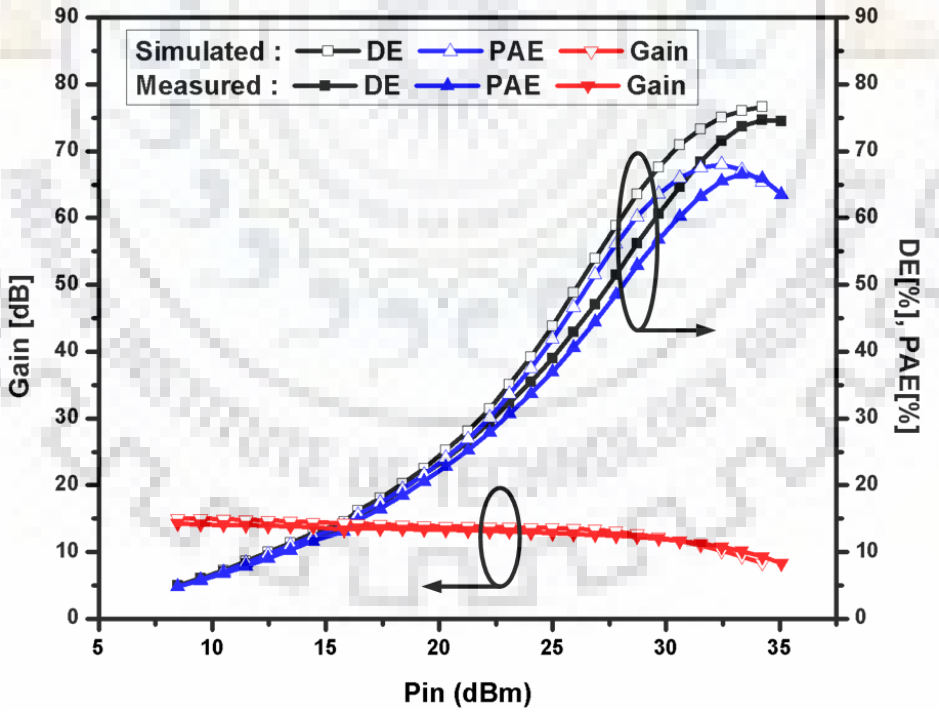

Figure 34 Simulated and measured DE, PAE and Gain of designed PA.

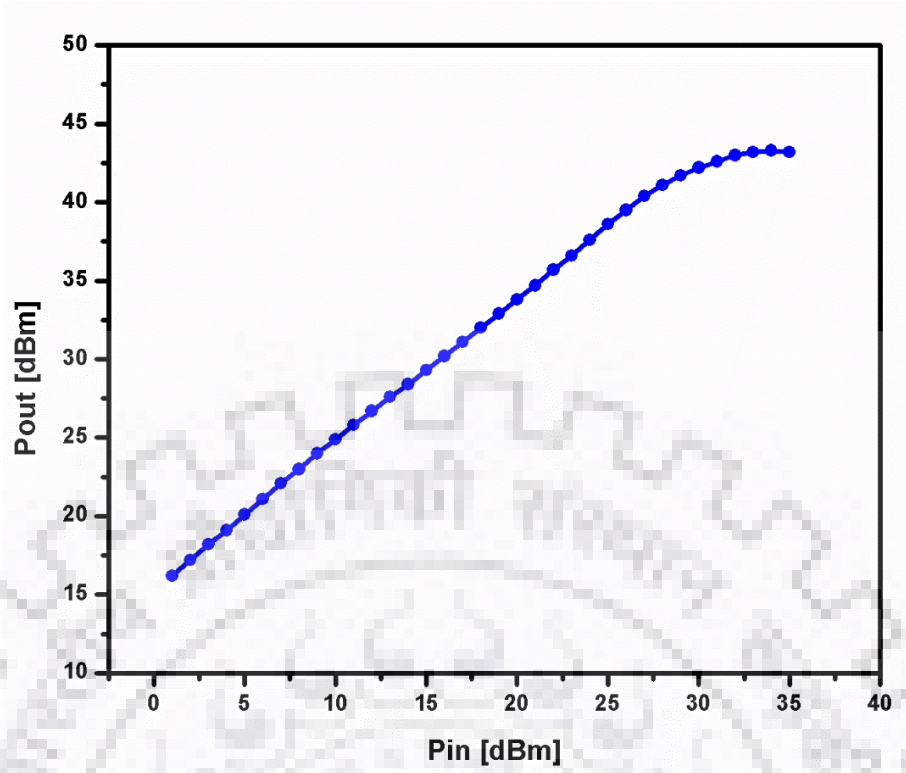

Figure 35 Measured output power of designed PA.

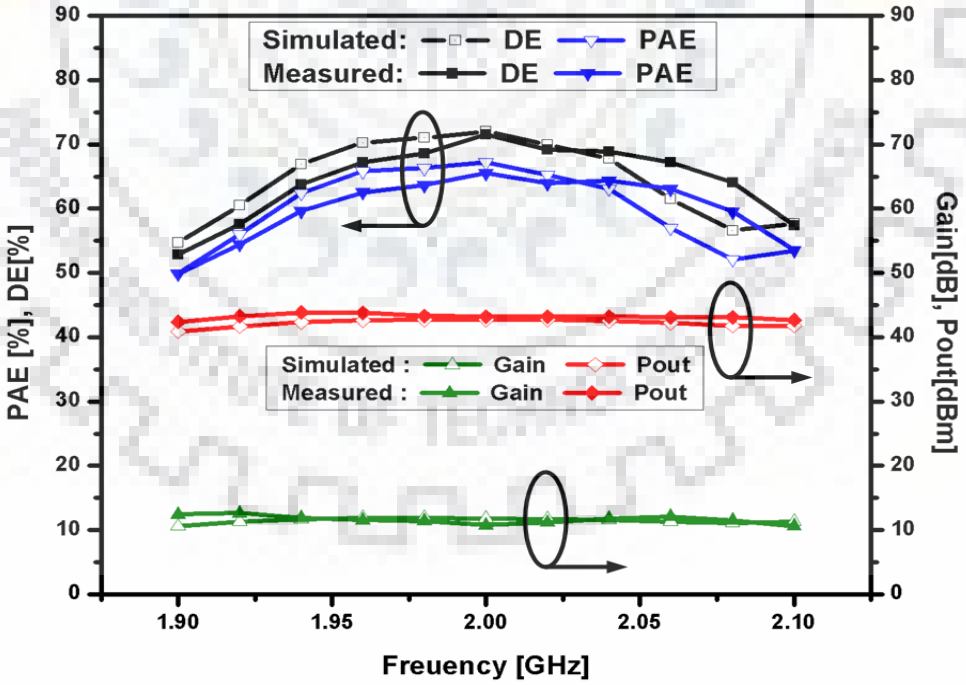

Figure 36 Results of fabricated PA over 100 MHz band.

5.1 Third-Order Intermodulation Distortion Measurement

A two tone measurement is done to measure the carrier to third-order intermodulation distortion (C/IMD3) for nonlinearity test. This distortion product is generally close to the carrier so it is practically impossible to filter out and can cause interference between multichannel communications equipment. But this product can be reduced by properly designing the output matching network. Measured C/IMD3 suppression is better than – 14 dBc in the operating rage as shown in Figure 37.

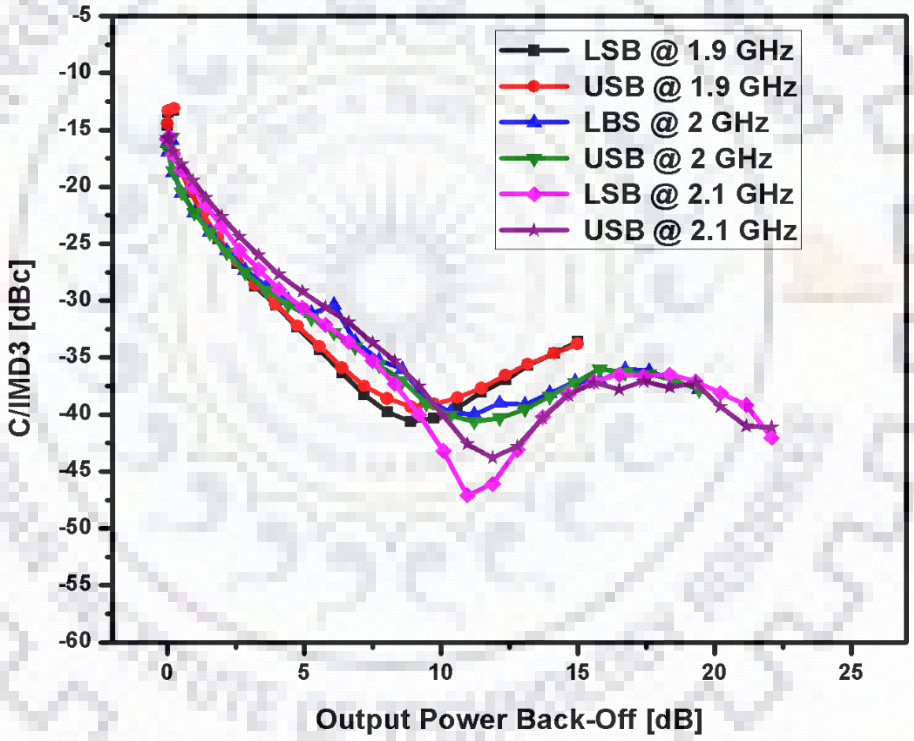

Figure 37 Third order inter modulation distortion of fabricated PA.

CHAPTER 6: CONCLUSION

Theoretical analysis of Class-D operation, derivation for ideal waveforms of voltage and current and load network parameters to ensure ZVS and ZCS conditions for 100% efficiency has been done. A push-pull CMCD PA has been designed at 2 GHz frequency of operation. Waveforms are studied at intrinsic plane of device to maintain the proper Class of operation throughout the design process. This thesis was mainly focused on designing the high efficiency PA operating the device as a switch keeping the proper waveform shape at intrinsic plane of the device. In ideal Class-D operation it has been found that at high frequencies switching time available for the device is very less, further it restricts ideal switching. The load network is tuned at second and third harmonic load to get the proper waveform shaping at intrinsic plane of the device and for maximum power transfer to the load fundamental impedance was matched to the load impedance. The PA is design and fabricated using Wolfspeed GaN HEMT CGH40010F device at 2 GHz. As a result DE of 71.5%, PAE of 65.5% and power delivered to load 42.54 dBm with 11.1 dB gain has been achieved.

CHAPTER 7: FUTURE SCOPE

A high efficiency CMCD PA operating at 2 GHz frequency was designed and fabricated. Further scope in this design is to improve the efficiency more if can (already designed at maximum efficiency by tuning).

Next thing is that this CMCD PA can be operated in Class-S mode by giving a delta sigma modulated signal and putting a band pass filter at output side to regain the original RF signal.

CHAPTER 8: REFERENCES

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