AN ADAPTIVE POWER LINE INTERFERENCE CANCELLER FOR ELECTROCARDIOGRAPHY

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ELECTRICAL ENGINEERING

(With Specialization in Instrumentation and Signal Processing)

By

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Candidate's Declaration

I hereby declare that this thesis report entitled **AN ADAPTIVE POWER LINE INTERFERENCE CANCELLER FOR ELECTROCARDIOGRAPHY**, submitted to the Department of Electrical Engineering, Indian Institute of Technology, Roorkee, India, in partial fulfillment of the requirements for the award of the Degree of Master of Technology in Electrical Engineering with specialization in Instrumentation and Signal Processing is an authentic record of the work carried out by me during the period from September 2012 to June 2013 under the supervision of **Dr. P SUMATHI, Department of Electrical Engineering, Indian Institute of Technology, Roorkee.** The matter presented in this thesis report has not been submitted by me for the award of any other degree of this institute or any other institute.

Date: 14/06/2013
Place: Roorkee

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CERTIFICATE

This is to certify that the above statement made by the candidate is true to the best of my knowledge and belief.

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Abstract

A Goertzel based all digital phase locked loop for removing power line interference from the ECG signal is proposed. A power line interference is artificially introduced in ECG signal and this proposed scheme tracks the amplitude and phase of all the interference components for power line frequency deviations from input signal frequency (i.e. 50 Hz). The output sampling frequency is adjusted with the help of all digital phase locked loop (ADPLL) to correct the phase errors introduced by the SG filter whenever variations in frequency occur. Main building blocks of proposed method are discussed. MATLAB simulation results are discussed and future work is to make this scheme adaptive for large variation in input frequency.

Acknowledgements

I would like to express my sincere gratitude to my guide Dr. P. Sumathi for her valuable guidence and consistent encouragement I, recieved throughout my dissertation work. I consider it as a great opportunity to do my dissertation under her guidence and to learn a lot from her research expertise. She always inspire me and bring me to a higher level of thinking.

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All above, I owe it all to almighty god for granting me the wisdom,health and strength to undertake this research task and enabling me to its complition.

Sarita Mishra

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Abbreviations

ADPLL	**A**ll **D**igital **P**hase **L**ocked **L**oop
DPLL	**D**igital **P**hase **L**ocked **L**oop
PFD	**P**hase **F**requency **D**etector
PD	**P**hase **D**etector
DCO	**D**igitally **C**ontrolled **O**scillator
SG	**S**liding **G**oertzel

Chapter 1

Introduction

"We cannot solve our problems with the same thinking we used when, we created them."

-Albert Einstein

1.1 Background

ECG signal has been a major diagnostic tool for the cardiologists. It is an interpretation of electrical activity of heart over a period of time and is detected by electrode attached to the surface of skin and recorded by a device external to the body. An ECG measures the rate and regularity of heartbeats. After diagnosis cardiologist readily interprets the ECG waveform and classifies them into normal and abnormal patterns. During acquisition there are different types of artifacts and interferences occurs, due to which an ECG signal gets corrupted. These noise sources can be power line interference, motion artifacts, electrode contact noise, motion artifacts, muscle contraction noise, base line drift muscle contraction, noise generated by instrumentation used, electronic devices and electrosurgical noises.

Power line interference is a common source of noise during measurements of bio-potentials and usually seen as horizontal bands on monitor. This type of interference may occur due to stray effect of the ac fields due to loops in patients cables or due to lose contacts on the patients cables as well as dirty electrodes or if the machine or patient is not properly grounded. It overwhelms tiny features and degrades the signal quality that may be critical for clinical diagnosis and monitoring[1]. Cables which are carrying ECG signals are susceptible to electromagnetic interference of power frequency (50Hz or 60 Hz) but sometimes the ECG signal is totally masked by this type of noise[2]. So its necessary that care should be taken while doing the ECG filtering, such that the desired information is not altered or distorted. Filtering of such type of noisy ECG signal is a very challenging problem for researchers. This problem was the first to attract researchers towards adaptive filtering, although; many methods have been suggested by researchers to reduce the power line interference noise in ECG signal[2–6]. There are some classical adaptive filtering method which provides a partial solution to this problem but, the problem is still considered open for researchers to continue their research to find an ultimate solution in this area [7]. Previously analog filtering help in dealing with these problems; however they may introduce non linear phase shifts or skewing the signal. In recent technology digital filters are widely used because these are capable and precise of being implemented and offer more advantages over the analog one.

1.2 Objective of Study

Adaptive filtering is a topic of deep theoretical challenges and immense practical relevance that persist even to this date. The main objective of this dissertation to develope an adaptive canceller for removing power line interferences fron ECG signal.This adaptive canceller is a Goertzel filter based all digital phase locked loop (ADPLL). The objectives of this work include:

1. Study of different components of all digital phase locked loop.

2. To propose a novel Goertzel based all digital phase locked loop.

3. Apply the proposed scheme on ECG signal.

1.3 Organisation of Thesis

The outline of the thesis is as follows: In Chapter 2 the related work done in this area of research is discussed briefly, Chapter 3 presents a theoretical description of ADPLL components type available, such as phase detector, loop filter and DCO.Chapter 4 presents the detailed description of proposed technique. Chapter 5 elaborates the simulation work and results obtained. The conclusion and future work is presented in Chapter 6.

Chapter 2

Literature Survey

A people without the knowledge of their past history, origin and culture is like a tree without roots.

-Marcus Garvey

2.1 Literature Background

Filtering is one of the most general term which is used in signal processing. Now a days adaptive filtering is a very popular topic of practical relevance. Adaptive filter is defined as a filter that adjust its transfer function according to the algorithm that is driven by an error signal. Phase locked loop is also an adaptive filter because it adjusts the output sampling frequency to correct the phase and frequency error whenever, there is a variation in input sampling frequency occur. There are number of adaptive filters which are developed by researchers and the research is still in progress. Most of the adaptive filters are digital filters.The digital PLL (DPLL) is not fully analog so, it is known as semi-analog circuit. Parasitic capacitors used in DPLL chip influence the center frequency of a DPLL and these large variation on center frequency introduce trimming and this become necessary

in critical applications. Many parameters are also subject to temperature drift and aging. To overcome these problems a phase locked loop (PLL) category introduced later than DPLL is an all digital phase locked loop (ADPLL). There are many applications of adaptive filtering in biomedical signal processing and communication signal processing to improve and enhance the quality of the signal. In biomedical signal processing power line interference removal from an ECG signal is a very challenging problem and adaptive filtering is introduced by researchers to solve this problem.

2.2 Related Work

In 1960s analog PLL ICs started appearing first time. This allowed for an incredible growth in PLL usage. Towards the end of the 1960s researchers turned their interest to the implementation and design of DPLLs. The first digital PLL appeared around 1970s. In 1960 Westlake was the first person to give document in this direction[8]. He presented an analysis of partially digitized phase locked loop using z-transform sampled theory. The first all digital loop was reported in 1967 by Dorgin [9]. Greco et al. presented experimental work done on first order DPLL in1972 [10, 11]. After that Garodnick et al. extended the previous work done by Greco et al. and reported first, second and third order DPLL in 1974 and tested using a computer simulation of a noise spike and verified experimentally. In later 1972, first and higher order both types of zero crossing (ZC) DPLLs in absence of noise are systematically analyzed by Gupta and Gill [12, 13]. In 1981 William C. Lindsey and C. M. Chie present a systematic survey of theoretical and practical work which is accomplished in the area of DPLLs [14] during 1960 to 1980. An ADPLL consist three major components: digital phase detector, digital loop filter and digital controlled oscillator (DCO). In 1989 B. Giebel, J. Lutz and P. L. Oleary presents [15] a digitally controlled oscillator which operates from a single 5V supply and fabricated in a standard CMOS process. Various types of all digital phase detectors, loop filters and digitally controlled oscillators (DCOs) are

discussed in [16] by Roland E. Best. A new architecture for a digitally controlled oscillator is presented by Giuliano Donzellini et al. in 1989 [17]. This is based on a controlled phase shifting principle and shows phase and frequency characteristics. This oscillator is especially suitable for applications involving synchronization of different systems. In 1995 a frequency synthesizing, all digital phase locked loop is presented by Dunning, J. et al. [18] which is fully integrated with a CMOS microprocessor. A new design of ADPLL for good phase and frequency tracking performance is proposed by K.T. Ibrahim et al. in 2002. In this ADPLL they reconfigured the commercially available ADPLL 74HC297 [19] with a newly developed DCO to achieve good frequency and phase error detection [20], which is not possible with 74HC297. An ADPLL for high speed clock generation is presented by C.C. Chung et al. in 2003. In this ADPLL control mechanism and a ring oscillator both are used so that it can work with standard cells. This architecture can reduce the design time and design complexity which make it very suitable for designing system on-chip applications [21]. In 2004 Thomas Olsson and Peter Nilsson proposed a new digitally controlled oscillator which is fully integrated and used as a clock multiplying circuit, is designed and fabricated for SoC applications, and also suggested an improved digitally controlled oscillator [22]. Staszewski et al. proposed a phase domain ADPLL [23] in 2005 and this ADPLL shows more advantageousness over conventional PLLs based on charge pump. This proposed model of ADPLL have good signal processing capabilities and it avoids relaying on volatage resolution of analog circuits. In 2007 Kratyuk, V. et al. presented a design procedure [24] which gives an analogy between ADPLL and type-II second order analog phase locked loop. The proposed ADPLL design inherits the frequency response and stability characteristics of analog prototype PLL. In 2008 Yordanov, A., G. Mihov et al. describe the experimental and simulation results of the basic types of digital PDs and their phase-voltage response is also obtained which represents the output voltage of the phase detector as a function of phase error between the input sequences and comparison of simulation results and experimental results is obtained [25, 26] . Qiang Zhang analyzed gradually the digital

PDs, loop filter and DCO and the feasibility of this proposed ADPLL structure is proved by simulation results. This proposed structure simplifies the control system structure and the reliability is also improved [27]. Efstathiou, D. describes a novel D-PLL architecture and presents an analysis of the digital loop filter [28]. FPGA implementation of ADPLL in ripple reduction technique [29] is discussed by Manoj Kumar and Kusum Lata . There are many adaptive filtering techniques which are used in biomedical signal processing to remove power line interferences from biomedical signal such as from electrocardiography. In 2006 Zhao, Z. D. and Chen, Y.Q. has given a new adaptive filtering method to remove base line wander and power line noise from ECG signal. In this proposed method, a 50 Hz notch filter is designed which filters the intrinsic mode function of an ECG signal which is corrupted by power line interference and the pure ECG signal is reconstructed by selecting proper value of intrinsic mode function (IMFs) [30, 31]. Noise cancellation and arrhythmia detection can be done by using adaptive filtering [32]. Santpal Singh Dhillon et al. proposed lattice structure based adaptive IIR notch filter for removing power line noise from ECG signal and also compared its performance with second order IIR notch filter for real time data of an ECG signal[33]. Mohammed Bahoura et al. presents a technique for removing power line noise from electrocardiography and this technique is based on wavelet and its real time implementation on FPGA[34]. Md. Maniruzzaman et al. presents a new adaptive method for removing power line noise from ECG signal which is based on least mean square algorithm [35]. Adaptive filtering has become one of the most popular and effective solution of signal processing and research work on this field is continuously in progress to achieve better results than the previous exsisting work.

Chapter 3

Components of All Digital Phase Locked Loop

To know that we know what we know, and to know that we do not know what we do not know, that is true knowledge.

-Nicolaus Copernicus

Main building blocks of an ADPLL are digital loop filter, digital phase detector and DCO. Basic block structure of an ADPLL is as follows in Figure3.1. In this chapter various types of phase detectors, loop fiters and DCOs are discussed briefly with the help of block diagrams.

3.1 Digital Phase Detector

A phase detector (PD) is a circuit capable of delivering an output signal that is proportional to the phase difference between its two input signals. In digital territory digital phase detectors become popular, such as the EXOR type, the edge triggered JK flip flop and so called phase-frequency detector (PFD). When

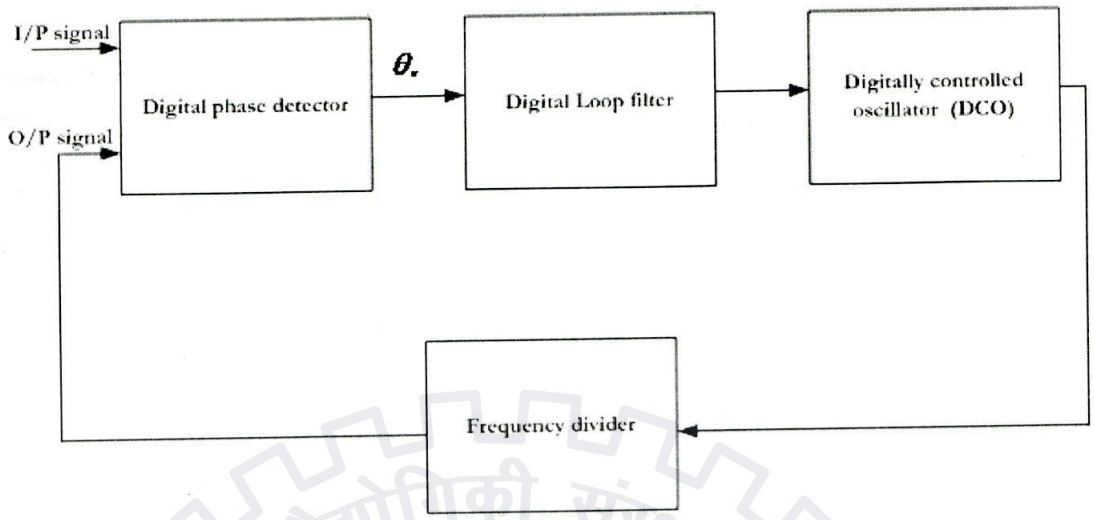


FIGURE 3.1: ALL Digital Phase Locked Loop (ADPLL).

digital word signal instead of bit signals are used, a number of additional phase detector circuits become available. According to the mechanism of PD, DPLL can be categorized mainly into four parts- (i) Flip-Flop DPLL : Positive zero crossing of input signal triggers the flip flop and the clock and,the phase error is computed from the duration between setting and resetting period of flip-flop. (ii) NR-DPLL: In Nyquist rate DPLL the input signal is sampled at the nyquist rate. (iii) ZC-DPLL: In Zero Crossing DPLL incoming signal is sampled at the zero crossing. (iv) LL-DPLL: In Lag-Lead DPLL phase detector determines whether input signal is leading or lagging to clock pulse. Type (i), (iii) and (iv) measure phase of incoming signal with the reconstructed signal while in type (ii) it is done against reference signal so the former is called as non uniform sampling while latter is called as uniform sampling. Block diagram of different PDs are as follows:

3.1.1 EXOR Phase Detector

Figure 3.2shows EXOR phase detector. The nominal lock range with this PD is 90^0 static phase shift. The EXOR phase detector is sensitive to input duty cycle

and if the input duty cycles are not 50% then this PD will lock with a phase error. This PD gives same width for both leading and lagging phase difference.

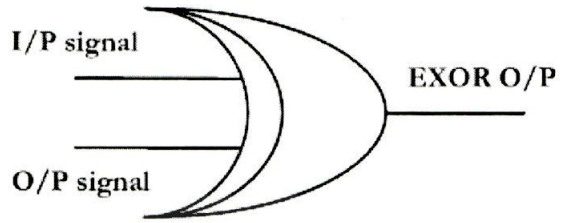


FIGURE 3.2: EXOR Phase Detector.

3.1.2 J K Flip Flop Phase Detector

Figure 3.3 shows block diagram of JK flip flop phase detector. The operation of this phase detector is similar to EXOR phase detector but the only difference is that it overcomes the symmetrical condition which is the drawback of EXOR type PD. The nominal lock point with this type of PD is a 180^0 static phase shift. This PD is not sensitive to input duty cycle. There is a potential to lock to harmonics of the reference clock.

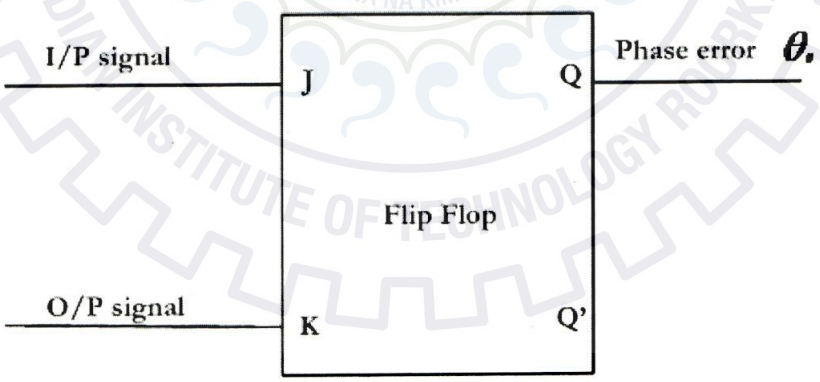


FIGURE 3.3: J K Flip Flop Phase Detector.

3.1.3 N-R Sampling Based Phase Detector

The N-R (Nyquist Rate) sampling PD is shown in Figure 3.4 According to the Nyquist sampling theorem,the input signal is reconstructed if the sampling rate of the analog to digital converter is chosen to be high. To produce the required phase error samples, the digital samples are then multiplied digitally with the local reference samples.

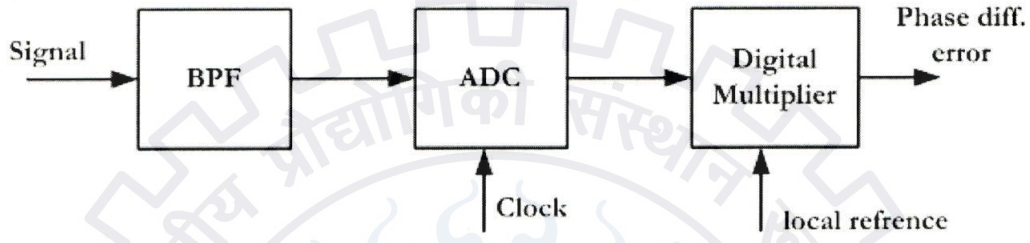


FIGURE 3.4: N-R Sampling Based Phase Detector.

3.1.4 F-F Based Sampling Phase Detector

Figure 3.5 shows block diagram of flip flop based sampling phase detector. When a zero crossing at positive edge of the input signal is detected then the output of the flip flop (SC) is set to 1. When a zero crossing at the local estimate is detected then, flip flop will clear or reset to 1. The phase detector generate a waveform having binary value with a duration of 1 sampling interval and this is related to the phase error between two inputs of this phase detector. This error signal is approximated by using loop filter and this integrated output is used to control a high rate clock counter. The content of the counter is digital representation of phase error within a range of $\pm\frac{\pi}{2^M}$ where, 2^M is the number of level of quantization for the phase error state over 2π.

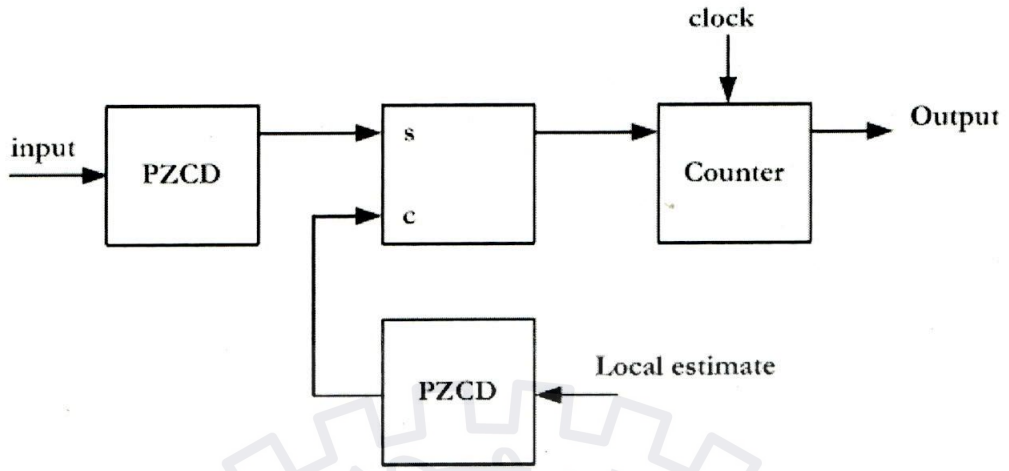


FIGURE 3.5: F-F Based Sampling Phase Detector.

3.1.5 Phase/Frequency Phase Detector

Figure 3.6 shows block diagram of phase frequency detector (PFD). Phase Frequency Detector allows for wide frequency locking range, potentially entire DCO tuning range. There is 3-stage operation with UP and DOWN outputs. Edge-triggering circuits are used to eliminate dependency of Gain to input duty cycle.

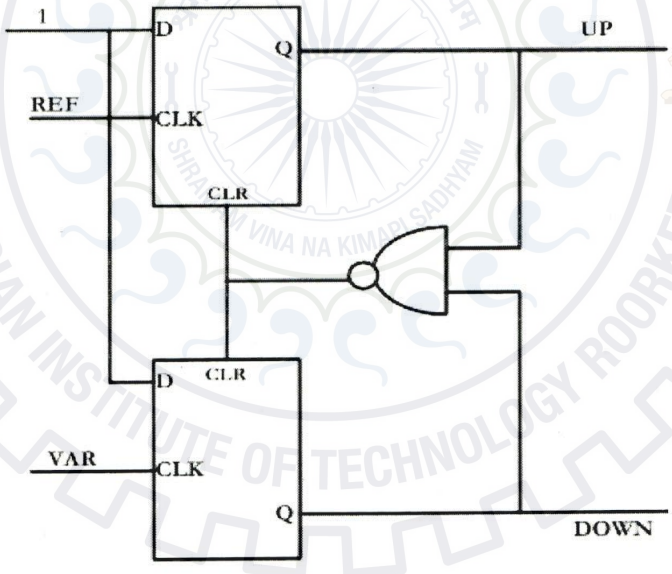


FIGURE 3.6: Phase/Frequency Phase Detector.

Dead Zone condition arises when phase error is too small and PFD cannot compare and output becomes zero. To remove this dead zone condition, a delay is introduced in reset path which sets minimum pulse width and, generates pulses for both UP and Down (DN).

3.1.6 Lead Lag Phase Detector

Figure 3.7 shows block diagram of lead-lag type phase detector. The output of this phase detector simply gives binary pulse to indicate that whether, the local reference signal is leading or lagging to input signal.

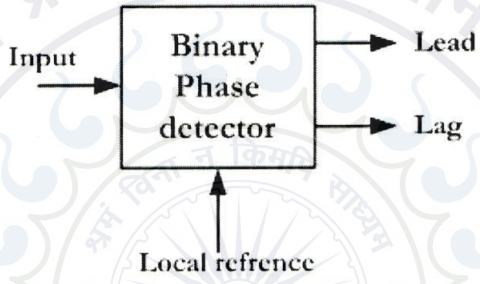


FIGURE 3.7: Lead Lag Phase Detector.

3.1.7 A Positive and Negative Zero Crossing Sampling Phase Detector

Figure 3.8 shows block diagram of this phase detector. Positive zero crossing and negative zero crossing type of phase detectors are two different type of phase detectors. First type samples on positive zero crossing and this type of phase detector is a very simple type of phase detector which is implemented among all type of DPLLs. In second type of phase detector the signal is samples on every zero crossing. The sign of samples is changed by transition sample selector to provide the correct polarity to the phase error by which transition can be detected whether it is negative going or positive going.

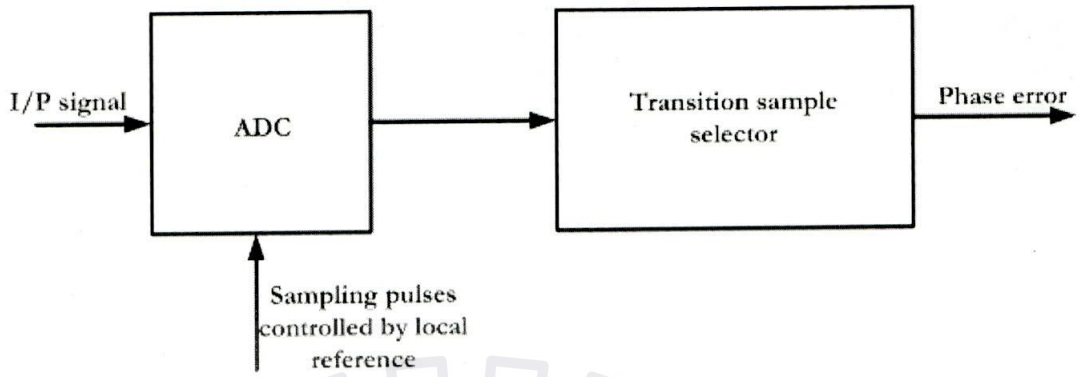


FIGURE 3.8: A Positive and Negative Zero Crossing Sampling Phase Detector.

3.2 Digital Loop Filter

Different types of output signals are generated by different type of phase detectors. Some PDs produces N-bit digital output signals, whereas simpler types, such as the EXOR or the PFD detector deliver one or two binary valued output signals (or tristate signal). It becomes evident that not every all digital loop filter is compatible with all types of all digital PDs. We have to consider which types of loop filters can be matched to the various PDs discussed previously. Several type of digital loop filters are available. Some of them are briefly discussed below.

3.2.1 Up/Down Counter Loop Filter

This loop filter preferably operates with a PD that delivers UP or Down (DN) pulses, such as the phase/frequency detector. This is accommodated easily because this loop filter is easily operated with the EXOR or JK flip flop type of PD and with others also. To convert the incoming UP and DN pulses into a direction ($\overline{Up}/Dn$) signal and a counting clock a pulse forming network is required. Figure 3.9 shows the block diagram of this type of digital loop filter. If the phase detector generate UP pulse then the content N of the counter is incremented by 1 and if DN will present at input end then the content N is decremented by 1. The content

N is given by n-bit parallel output signal of the loop filter. The weighted sum of the UP and DN pulses gives the value of content N, i.e. the UP pulses have an assigned weight of +1, the DN pulses have -1. This filter can be considered as an integrator having transfer function $H(s) = \frac{1}{ST_a}$

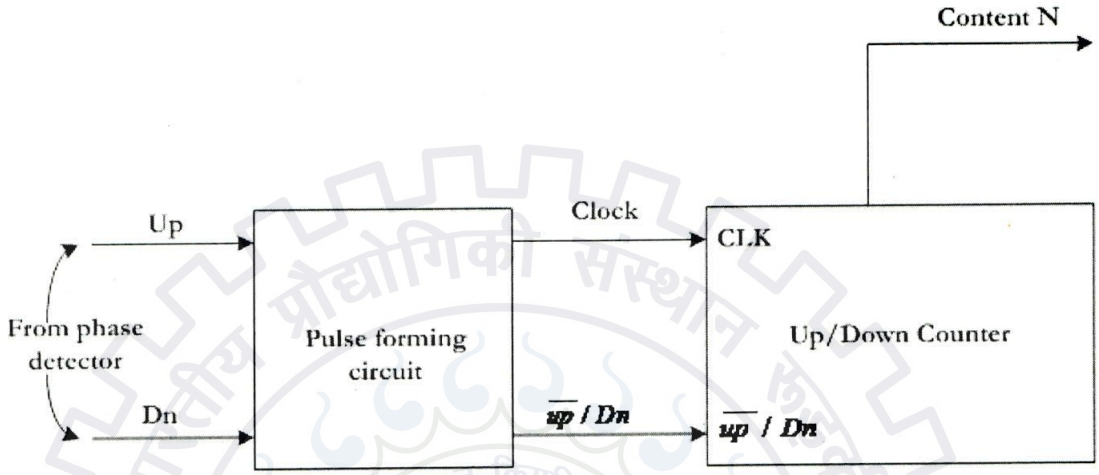


FIGURE 3.9: Up/Down Counter Loop Filter.

Where, T_a is the integrator time constant. This is however a very crude approximation because UP and DN pulses do not carry any information about the actual size of the phase error; they only tell whether the phase of input signal is leading or lagging to output signal.

3.2.2 K Counter Loop Filter

This is one of the most important digital loop filter. This loop filter works together with JK flip flop or the EXOR phase detector. As the Figure 3.10 shows, the K counter made up of two independent counters, which are usually named as up counter and down counter. In reality, both counters are up counter. K is defined as modulo of both the counters; which means, the counters will count the content N in range from 0 to K-1. The K modulus controls the value of maximum count of counter which is always in an integer power of 2. The frequency of the K clock

signal is M times the center frequency f_a of the all digital phase locked loop, where M can be 8, 16, 32. The $\overline{UP}/Dn$ signal controls the operation of K counter. At high value of input signal, the down counter will count, at that time the up counter contents will remain still. In other case, when up counter counts then the content of down counter will remain still. When the content will overflow from the maximum count then both counter recycle to 0. One carry pulse will generate if the count value of the up counter are $\geq K/2$, and the borrow pulse will go high when the count value of down counter are $\geq K/2$. The frequency of DCO is controlled by positive going edges of borrow and carry signals .

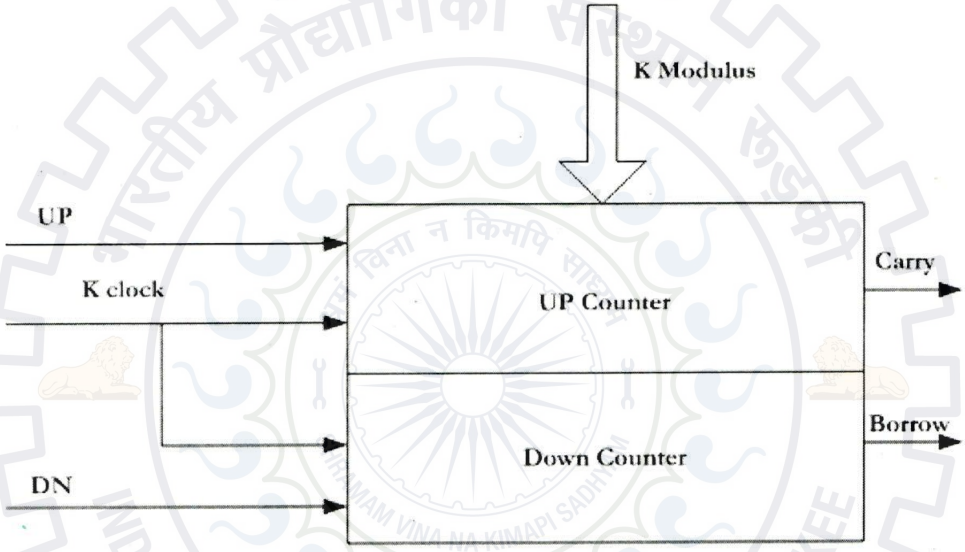


FIGURE 3.10: K Counter Loop Filter.

3.2.3 N Before M Filter

This is another type of digital loop filter and its performance is very non linear. Figure 3.11 shows the block diagram of N before M filter. This type of filter operates in conjunction with PDs, generating UP and DN pulses, same as in case of phase/frequency detector (PFD). In this filter two frequency counters are used to scale down the input signal by a factor N and one other counter is to scale down by M, where $M > N$ always. The divide by M counter counts the incoming UP

and DN pulses. When the upper counter receives N, UP pulses it will produce one carry only when, M counter does not receive M pulses otherwise the down counter would have been reset. The same statement can be make for the lower counter as well. The output of this filter can be used in similar way to control digitally controlled oscillator as it was indicated for K counter loop filter.

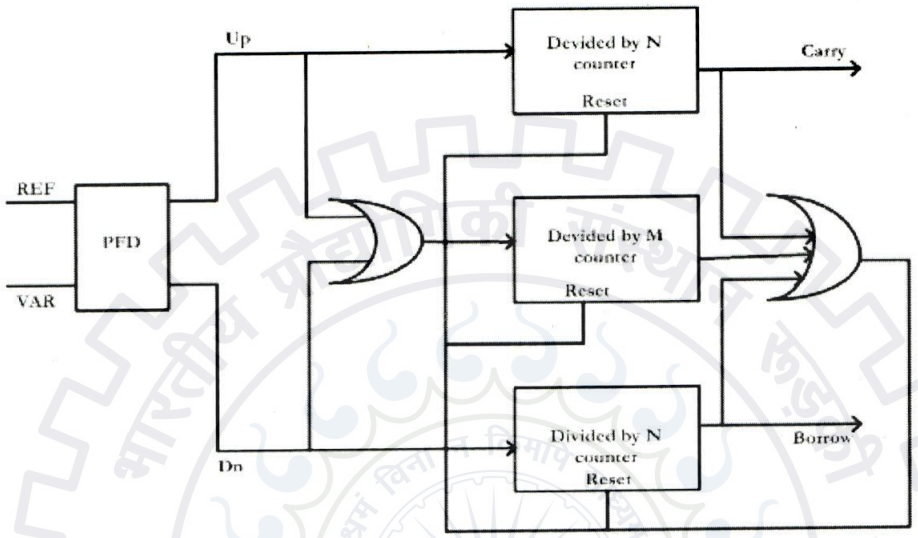


FIGURE 3.11: N Before M Loop Filter.

3.3 Digitally Controlled Oscillator (DCO)

A DCO is a hybrid electronic oscillator which is used in frequency synthesizers. DCOs are designed for tuning stability in phase locked loop and frequency synthesizers. There are varieties of DCOs design which are implemented in hardware or in software.

3.3.1 Divided By N Counter DCO

This is the simplest DCO among all available DCOs. This DCO scales down the frequency of the signal which is generated by high frequency oscillator. The scaling

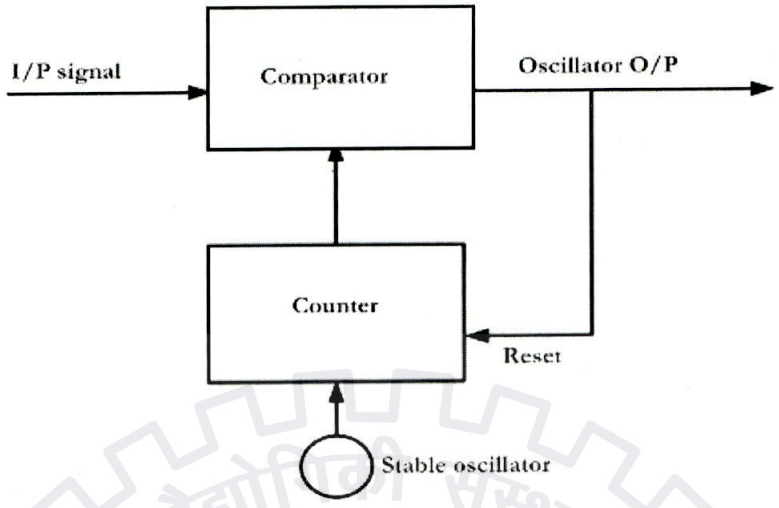


FIGURE 3.12: Divided By N Counter DCO.

factor N of this counter is controlled by the output of digital loop filter. Figure 3.12 shows the block diagram of this DCO.

3.3.2 Increment Decrement (ID) Couter DCO

This DCO operate with K counter loop filter or N before M loop filter that generates borrow and carry pulses. This DCO has three inputs, an ID clock, an

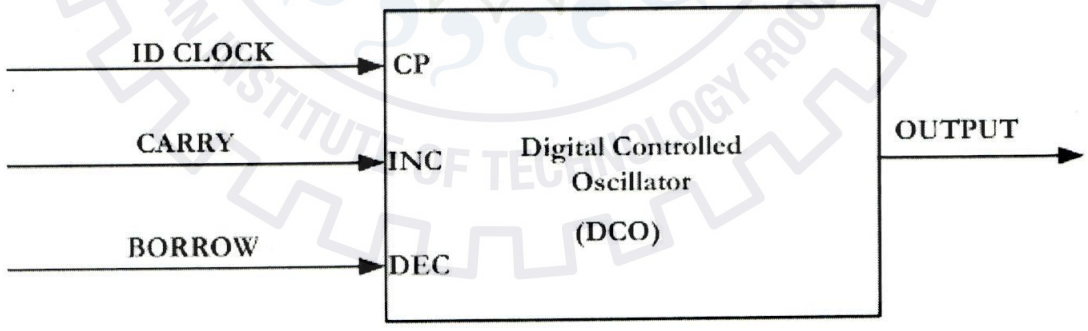


FIGURE 3.13: Increment Decrement Counter DCO.

increment input and a decrement input as shown in Figure 3.13.The carry pulses

generated by loop filter are fed to INC input and borrow pulses are fed to DEC input. ID counter is sensitive to positive going edge of borrow and carry inputs. If there is no borrow and carry input will present at the input end of DCO then this ID counter DCO will act as simply divided by 2 Counter. If there is a carry pulse is present at INC input of DCO then ID out pulse will be advanced by one ID clock period and if borrow pulse will be there at DEC input of DCO then the ID out will be delayed by one pulse of ID clock.The frequency of ID counter should be less than the frequency of the ID clock, but not $\geq \frac{2}{3}$ of that value and this controls the hold range of the ADPLL. If more carry and more borrow will be deliverd by loop filter then ID counter won't be able to process all carries and borrows and a condition of "overslept" will arise. So to prevent this problem the maximum frequency of carry and borrow pulse must not be higher than one-third the frequency of the ID clock.The data sheet of 74HC/HCT297 conclude the exact operation of the ID counter[19].

Chapter 4

Proposed Technique

"Good ideas are not adopted automatically. They must be driven into practice with courageous patience."

-Hyman Rickover

4.1 Proposed Structure of Goertzel Based Adaptive Canceller and Its Working

Proposed structure of Goertzel based ADPLL is shown in Figure 4.1. In this proposed technique corrupted ECG signal (ECG+Noise) is fed to one input end of Goertzel filter which accurately estimates the fourier coefficients of multifrequency sinusoidal signal buried in noise and the other input of goertzel is DCO output. The real frequency coefficients of Goertzel filter is given to phase detector as one input and this phase detector gives phase error i.e. θ_e between the corrupted ECG signal and the Goertzel filter's output.This θ_e is given to the input end of digital loop filter which approximates the error and according to the output of this loop filter, DCO generate pulses (add or delete pulses) to adjust the sampling

frequency of the Goertzel filter. Finally the output of Goertzel filter is subtracted from corrupted ECG signal to get pure or clean ECG signal.

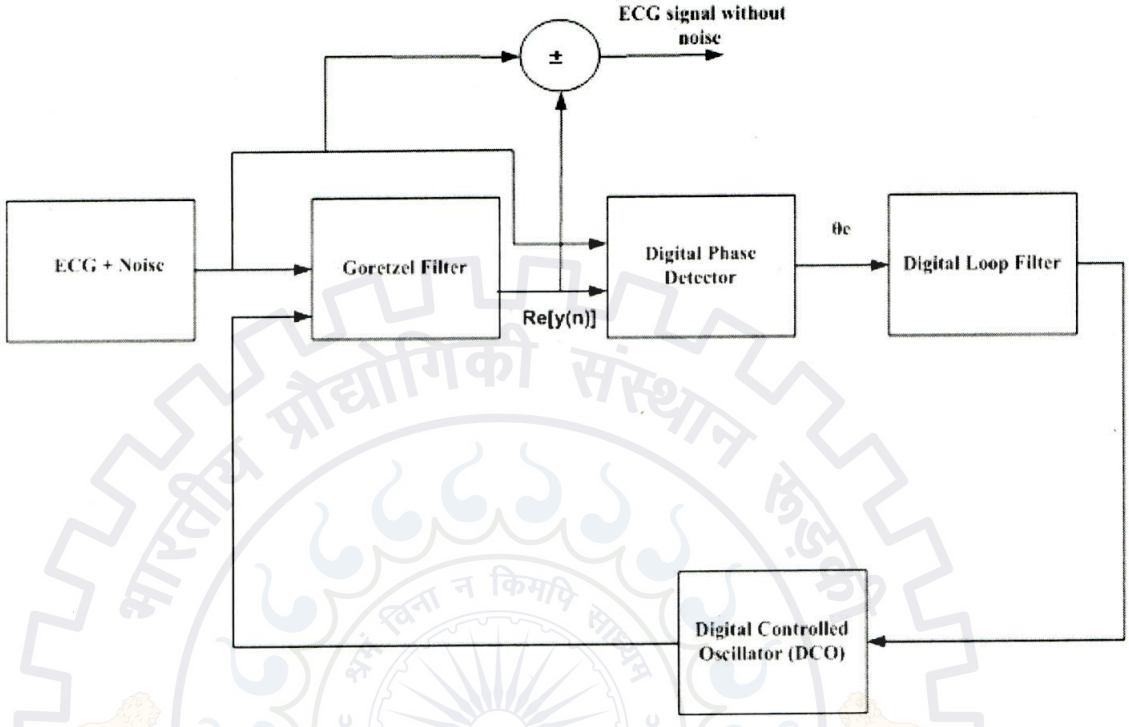


FIGURE 4.1: Proposed Structure of Goertzel Based Adaptive Canceller .

4.2 Description of Basic Building Blocks of Proposed Technique

This Proposed Technique is a Goertzel based All Digital Phase Locked Loop (ADPLL) which is an adaptive noise canceller. All digital means that the system consists of logic devices only. The word digital also signifies that the signal within the system must be digital too. So the signal within the ADPLL can be a bit signal or a binary signal. The basic blocks of this proposed Goertzel based ADPLL are Sliding Goertzel (SG) filter, phase/frequency detector,K counter loop filter and ID counter DCO which are going to be discussed briefly in this section.

4.2.1 Sliding Goertzel Filter

This filter analyizes a selectable frequency component from a discrete signal. Real time processing requires spectral updates on sample by sample basis so, this filter reduces the number of multiplies by which it also reduces computational complexities .

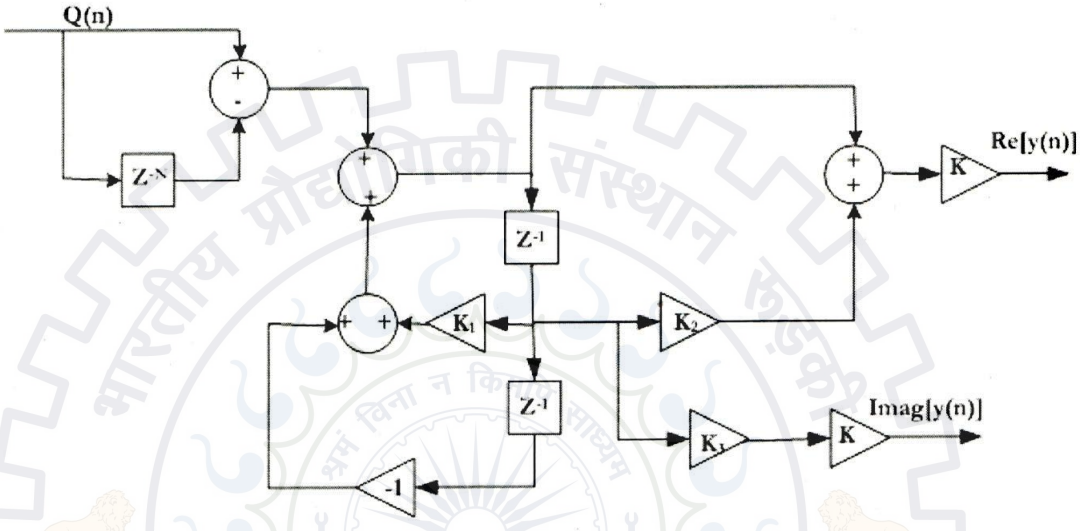


FIGURE 4.2: Block Diagram of Goertzel Filter.

Where, $K1 = 2cos\theta, K2 = -cos\theta, K3 = sin\theta$ *and* $K = 2/N, \theta = (2\pi)/N$
This is applies on a single real valued coefficents at each iteration,using real valued arithmatic for real valued input sequences. Transfer Function of SG filter [36, 37] is given in eq 4.3

$$H_{sg}(z) = \frac{(1 - e^{-j2\pi k/N} Z^{-1})(1 - Z^{-N})}{(1 - 2cos(2\pi k/N)Z^{-1} + Z^{-2}} \tag{4.1}$$

eq 4.3 can also be written as:

$$H_{sg}(z) = \frac{(1 - e^{-j2\pi k/N} Z^{-1})(1 - Z^{-N})}{(1 - e^{-j2\pi k/N} Z^{-1})(1 - e^{2j\pi k/N} Z^{-1})} \tag{4.2}$$

the above eq 4.2 shows that there are N number of zeros are equally spaced over a unity circle of Z-domain , one conjugate pole pair is at $Z = e^{\pm j2\pi k/N}$ and one zero is located at $Z = e^{-j2\pi k/N}$. The pole-zero pair at $Z = e^{-j2\pi k/N}$ will cancel each other and there is one uncanceled pole at $Z = e^{+j2\pi k/N}$ will remain . So the uncanceled pole and N eqally spaced zeros will define asymmetrical frequency response of the filter.

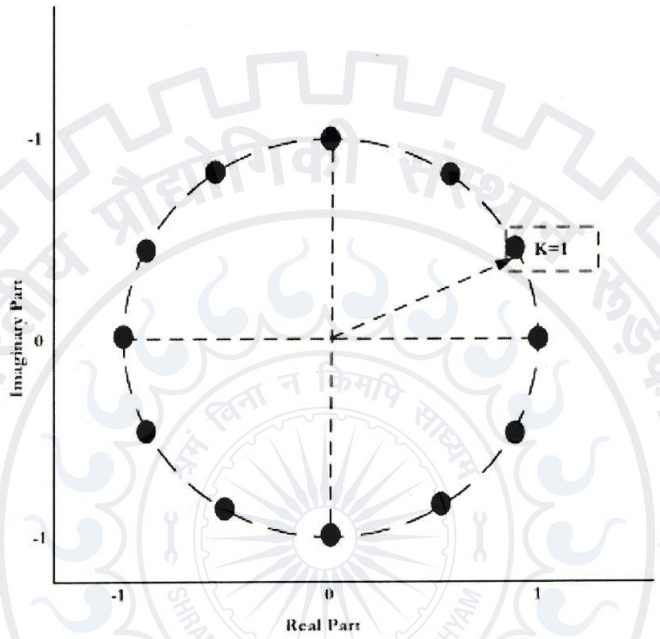


FIGURE 4.3: Pole Zero Location in Z-domain for N=12 and K=1.

Figure 4.3 shows the Z-domain pole zero location for N=12 (shows N equally spaced zeros) and k=1 (shows location of uncancanceled pole in Z-domain). k can be calculated as $k = Nf_0/f_s$ where, f_0 andf_s are central frequency and sampling frequency respectively.

we can write eq 4.3 as

$$H_{sg}(z) = \frac{[1 - [cos(2\pi k/N) - jsin(2\pi k/N)](1 - Z^{-N})}{(1 - 2cos(2\pi k/N)Z^{-1} + Z^{-2}} \tag{4.3}$$

by separating real and imaginary part of the above equation

$$Re[H_{sg}(z)] = \frac{[1 - cos(2\pi k/N)Z^{-1}](1 - Z^{-N})}{(1 - 2cos(2\pi k/N)Z^{-1} + Z^{-2}} \tag{4.4}$$

$$Img[H_{sg}(z)] = \frac{[-sin(2\pi k/N)Z^{-1}](1 - Z^{-N})}{(1 - 2cos(2\pi k/N)Z^{-1} + Z^{-2}} \tag{4.5}$$

by using eq 4.4 and eq 4.5 filter structure can be constructed as shown in Figure 4.2

4.2.2 Phase Detector used in Proposed Technique

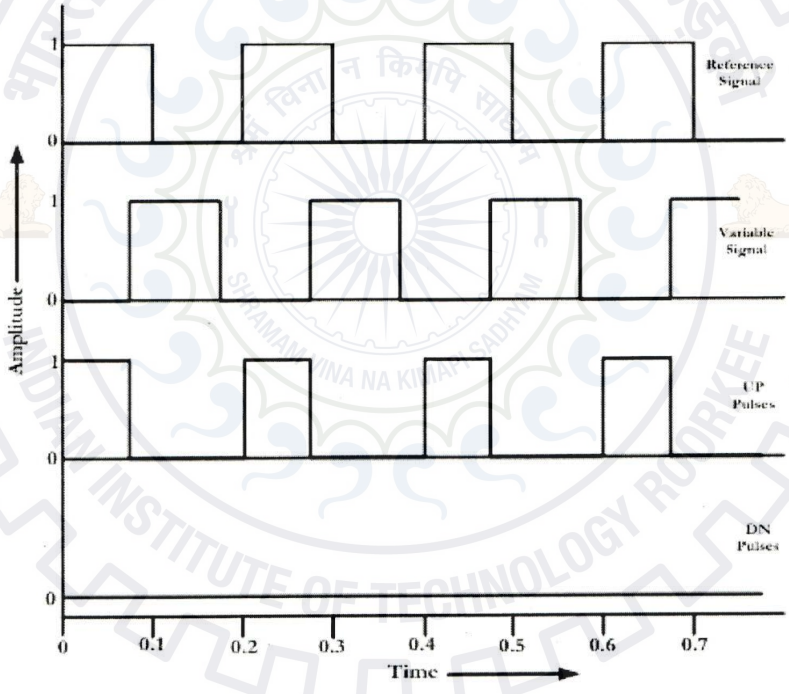


FIGURE 4.4: Waveform of PFD (when Reference signal is leading).

The phase detector which is used in this proposed technique is phase/frequency detector (PFD) shown in Figure 3.6. This phase detector detects phase error as well as frequency error. Figure 4.4 and Figure 4.5 are showing the input and

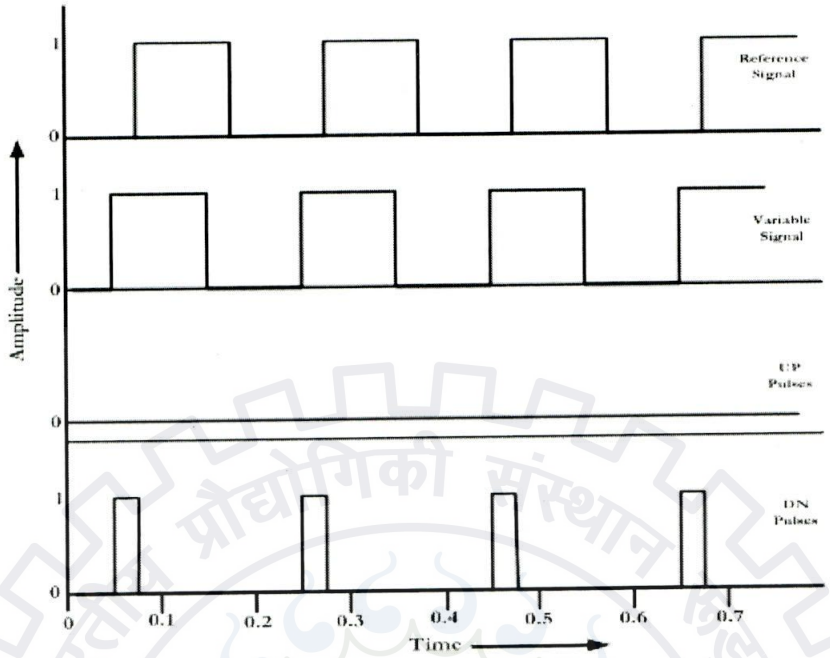


FIGURE 4.5: Waveform of PFD (when Reference signal is lagging).

corrosponding output waveforms of PFD. If there is no error then PFD will not generate any UP pulse or Down(DN) pulse. But when the two inputs of PFD are unequal in phase and/or frequency, the differential UP and DN outputs will provide pulse streams. If reference signal is leading the only UP pulses will be received at the output end of PFD(Figure 4.4) and if reference signal is lagging than DN pulses will be received as shown in Figure 4.5.

4.2.3 Digital Loop Filter used in Proposed Technique

K counter loop filter is used in this technique which is shown in Figure 3.10.The output waveforms of K counter loop filter are shown in Figure 4.6. Whenever UP pulse is present at the input of loop filter then up counter of K counter loop filter will start counting from 0 to maximum count $K-1$ and when the content will exceed from maximum count then it will reset to its initial value, in this design it is taken as 0. When the content of up counter will reach greater than or equal to

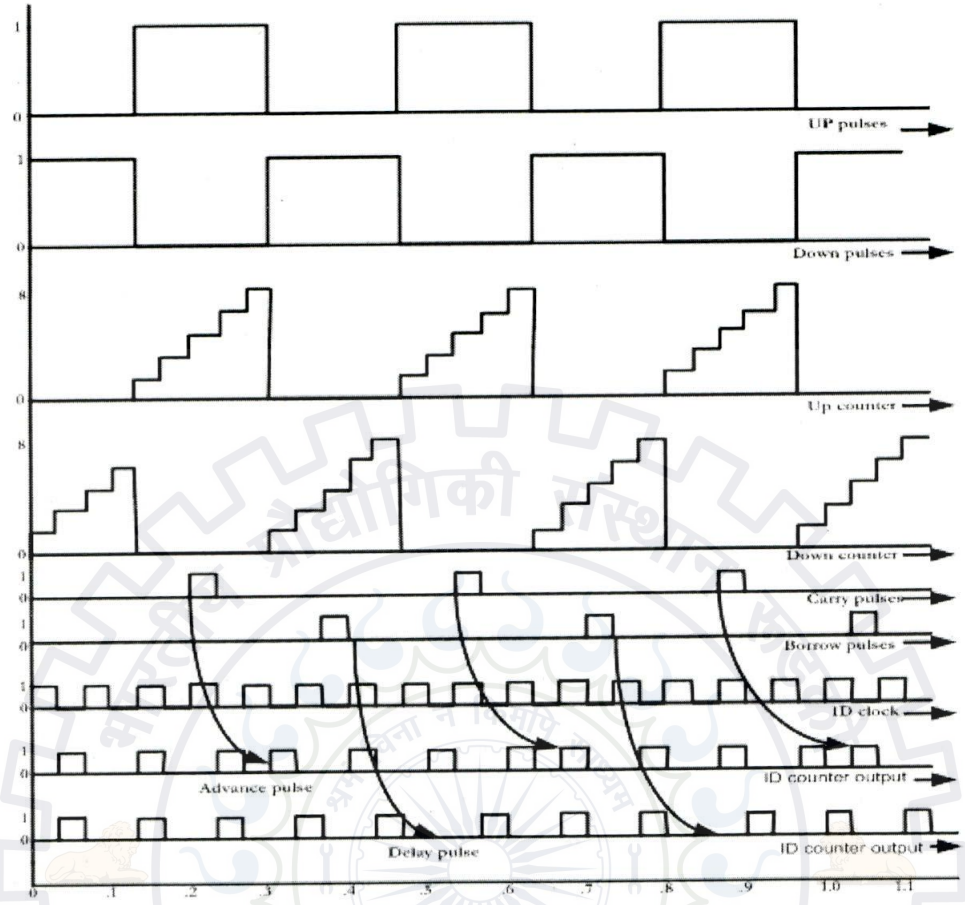


FIGURE 4.6: Output waveform of K counter loop filter and ID counter.

the value of $K/2$ then one carry pulse will generate at output and this time down counter will stay frozen. Similarly, if DN pulse will present at input end of loop filter than down counter will start counting up to its maximum count and when the content of this down counter will exceeds from maximum count $K-1$ it will reset to its initial value i.e. 0, same time up counter will stay frozen. When the content of down counter will reach greater than or equal to the value of $K/2$ then one borrow pulse will produced by loop filter at its output end. These carry pulses and borrow pulses control the operation of DCO.

4.2.4 DCO Used in Proposed Technique

In this techcnique ID counter type DCO is used (Figure 3.13).This ID counter is made up of eight D flip flop and one toggle flip flop as shown in appendix A.6. Output frequency of the ID counter is controlled by carry and borrow pulses. If carry pulse is present at the input of this DCO than it will advance the ID out by one ID clock pulse and if borrow pulse is present than ID out will be delayed by one ID clock pulse as shown in Figure 4.6. This DCO output pulses will fruther used to adjust the sampling frequency of Goertzel filter to get locked with input.

Chapter 5

Simulation Results and Discussion

"Infinite patience produces immediate results."

5.1 Program for ECG Generation

$x2 = 3.5 * ecg(9100);$

$y2 = sgolayfilt(kron(ones(1, 60), x2), 0, 9);$

$n = 1 : 200000$

$del = round(9100 * rand(1));$

$fhb = y2(n + del);$

$t = 0.00025 : .00025 : 50$

$plot(t, fhb);$

$axis([0\ 3\ -4\ 4]);$

$grid;$

$x = [t; fhb];$

The above program is to generate an artificial ECG signal of maternal heart beat. The artificially generated ECG signal is shown in Figure 5.1. The ECG signal is corrupted artificially by adding sinusoidal noise (which is considered as power line interference in proposed scheme) as shown in Figure 5.2. Enlarged form of corrupted ECG signal is shown in Figure 5.3 .

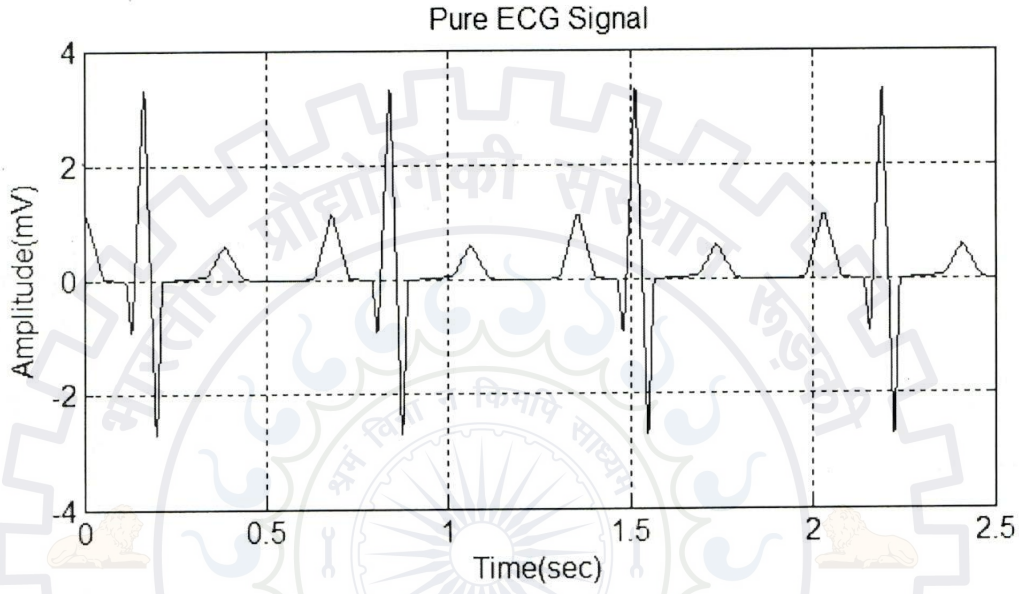


FIGURE 5.1: Plot of Pure ECG Signal.

The proposed technique is being tested with sinusoidal signal and then implemented on ECG signal for removing power line interference. In this simulation work center frequency is taken as 50Hz. Simulation results are showing the locking performance of proposed Goertzel based ADPLL with sinusoidal input and also shows the performance when, it is implemented in ECG signal for removing power line interference from it. Appendix A shows the simulink models of proposed Goertzel based ADPLL and all of its components.

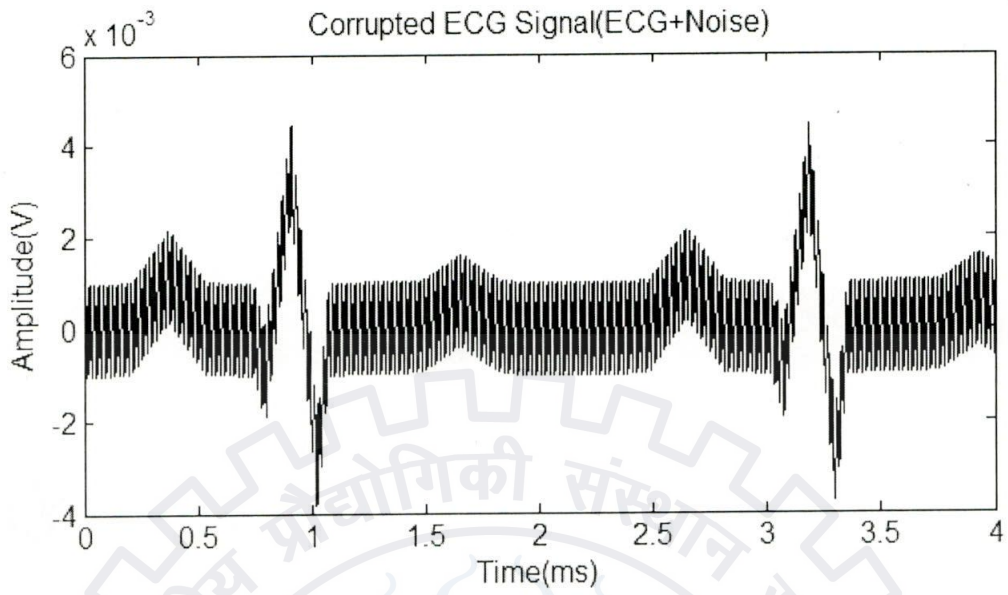


FIGURE 5.2: Plot of Corrupted ECG Signal.

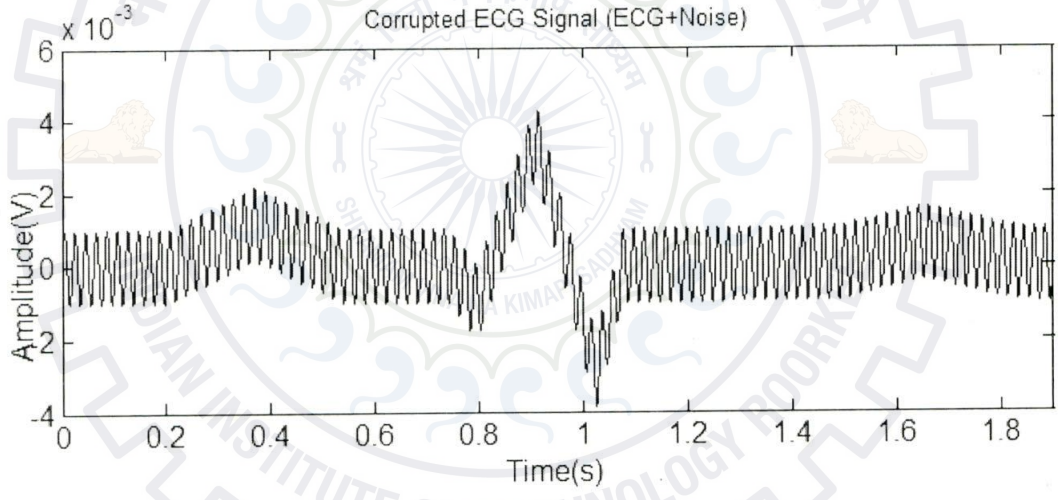


FIGURE 5.3: Plot of Corrupted ECG Signal (Enlarged).

5.2 Results of Proposed Scheme with Sinusoidal Signal

Figure 5.4 showing the locking performance of Goertzel based ADPLL at 50Hz (i.e. center frequency). This simulation results shows that input signal and output

signal both are locking perfectly within one cycle.

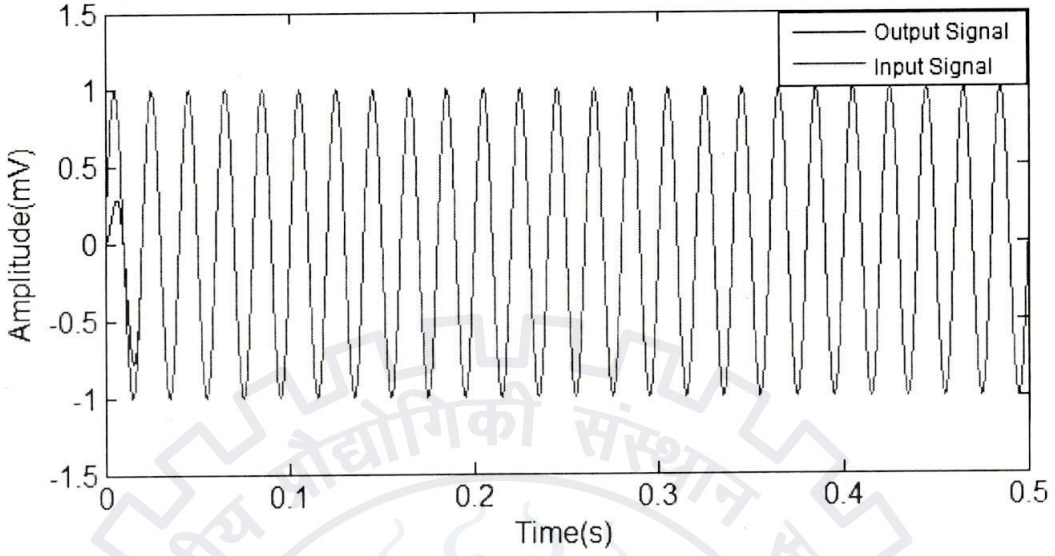


FIGURE 5.4: Locking performance of Goertzel based ADPLL at 50Hz with sinusoidal signal.

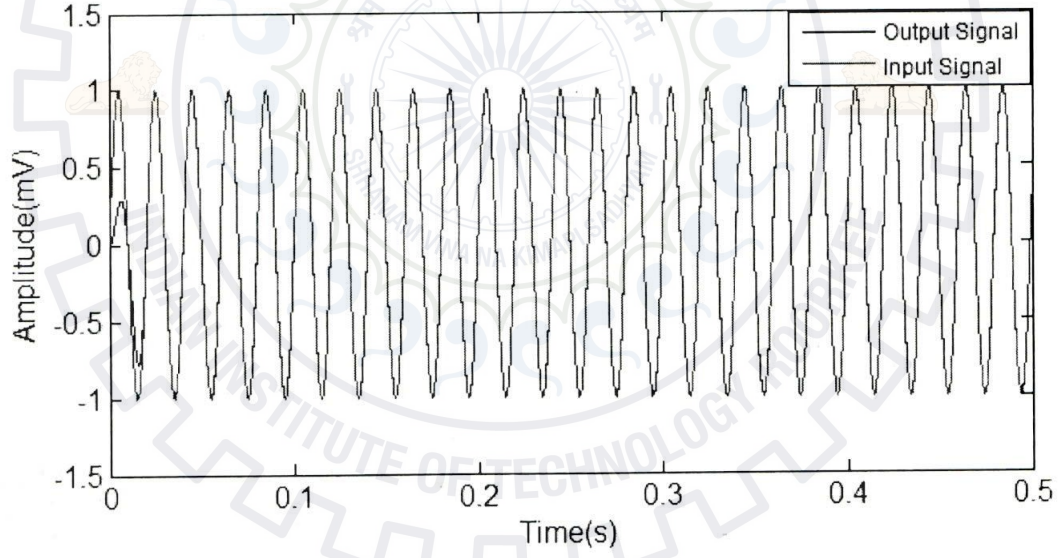


FIGURE 5.5: Locking performance of Goertzel based ADPLL at 50.1Hz with sinusoidal signal.

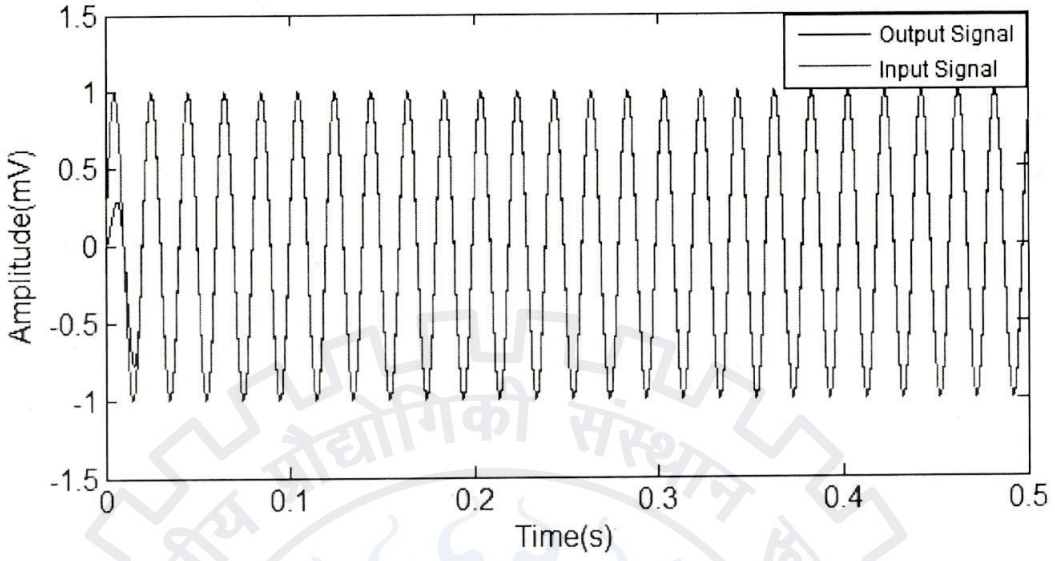


FIGURE 5.6: Locking performance of Goertzel based ADPLL at 50.3Hz with sinusoidal signal.

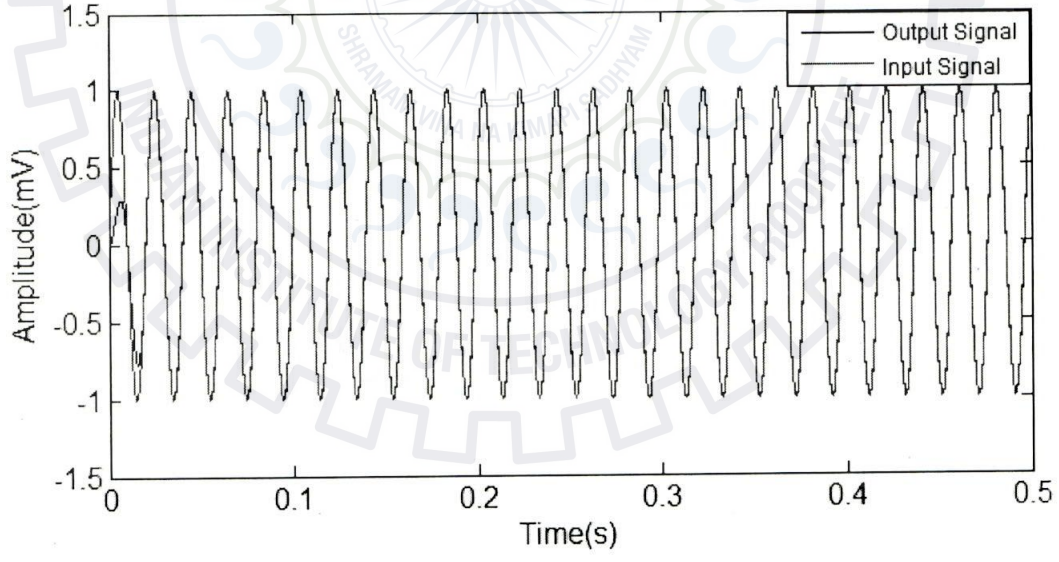


FIGURE 5.7: Locking performance of Goertzel based ADPLL at 50.4Hz with sinusoidal signal.

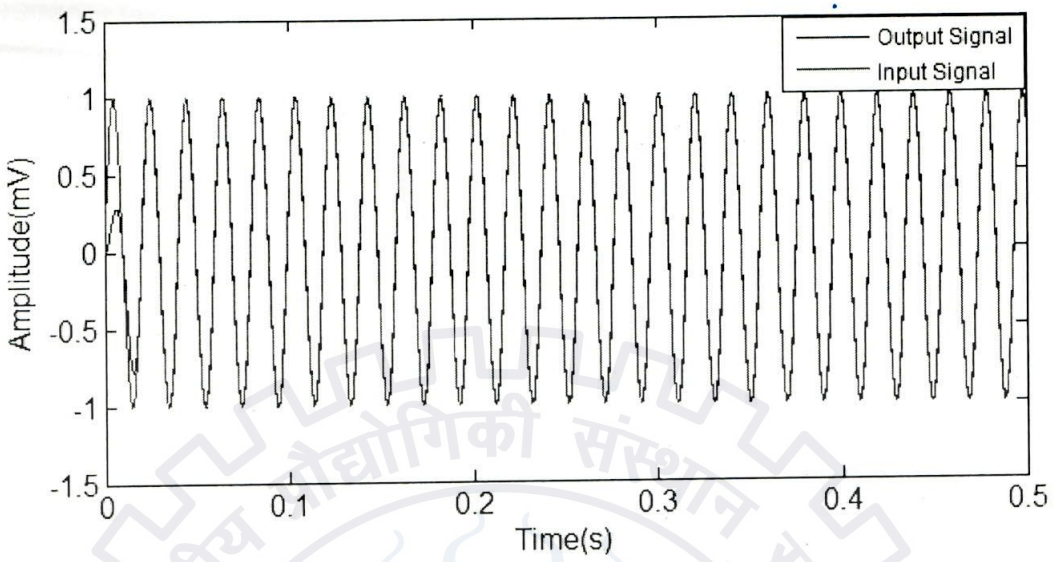


FIGURE 5.8: Locking performance of Goertzel based ADPLL at 50.7Hz with sinusoidal signal.

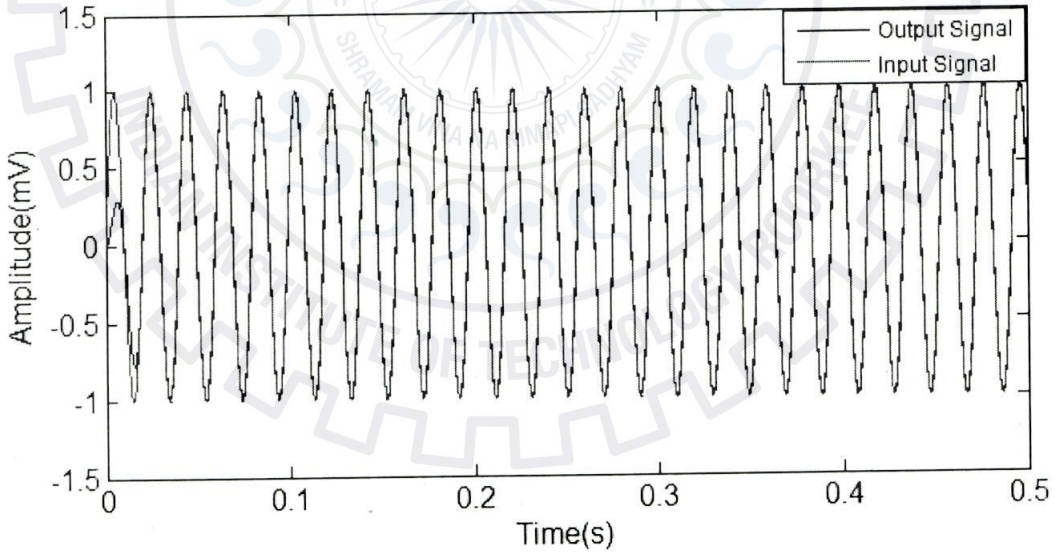


FIGURE 5.9: Locking performance of Goertzel based ADPLL at 50.9Hz with sinusoidal signal.

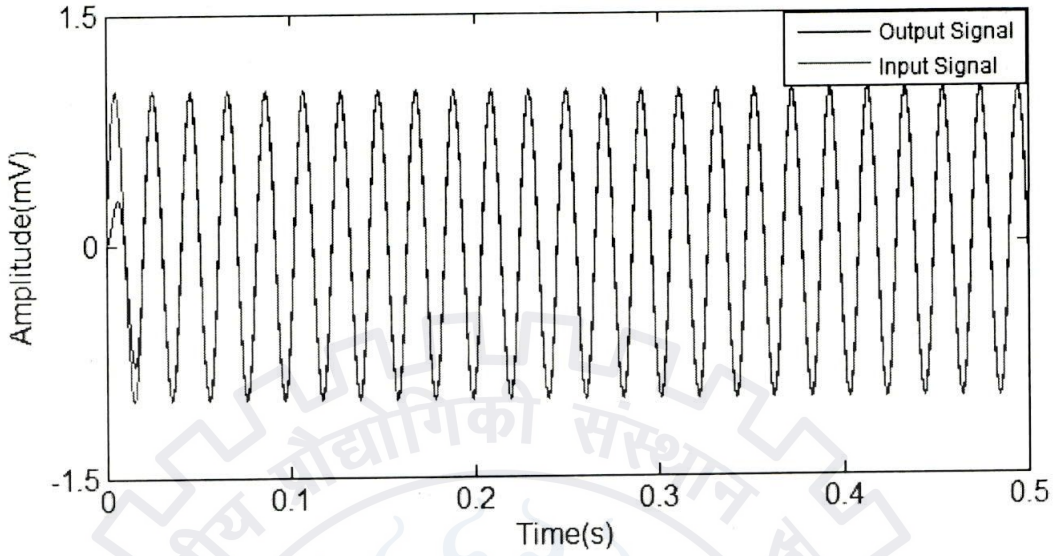


FIGURE 5.10: Locking performance of Goertzel based ADPLL at 51Hz with sinusoidal signal.

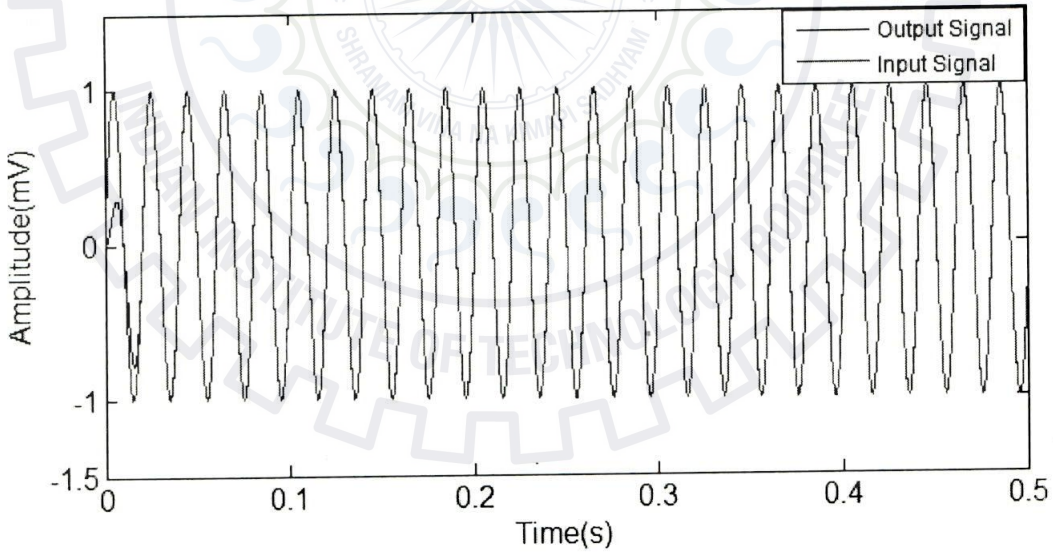


FIGURE 5.11: Locking performance of Goertzel based ADPLL at 49.9Hz with sinusoidal signal.

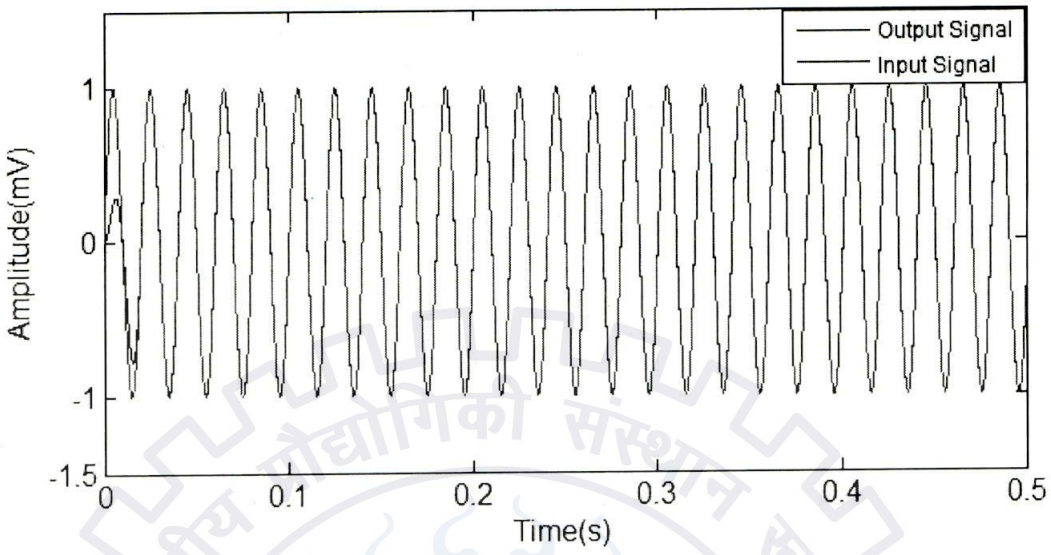


FIGURE 5.12: Locking performance of Goertzel based ADPLL at 49.7Hz with sinusoidal signal.

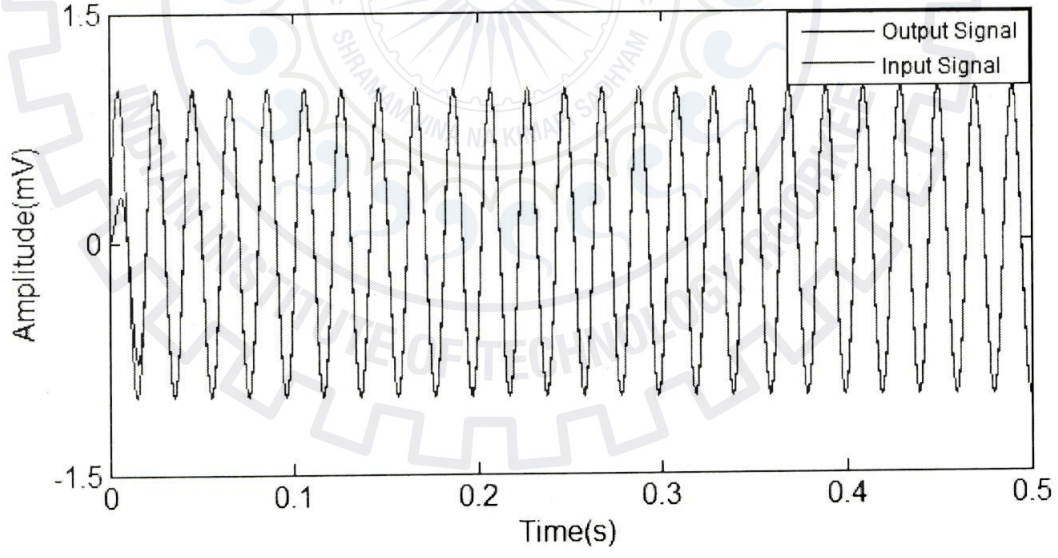


FIGURE 5.13: Locking performance of Goertzel based ADPLL at 49.5Hz with sinusoidal signal.

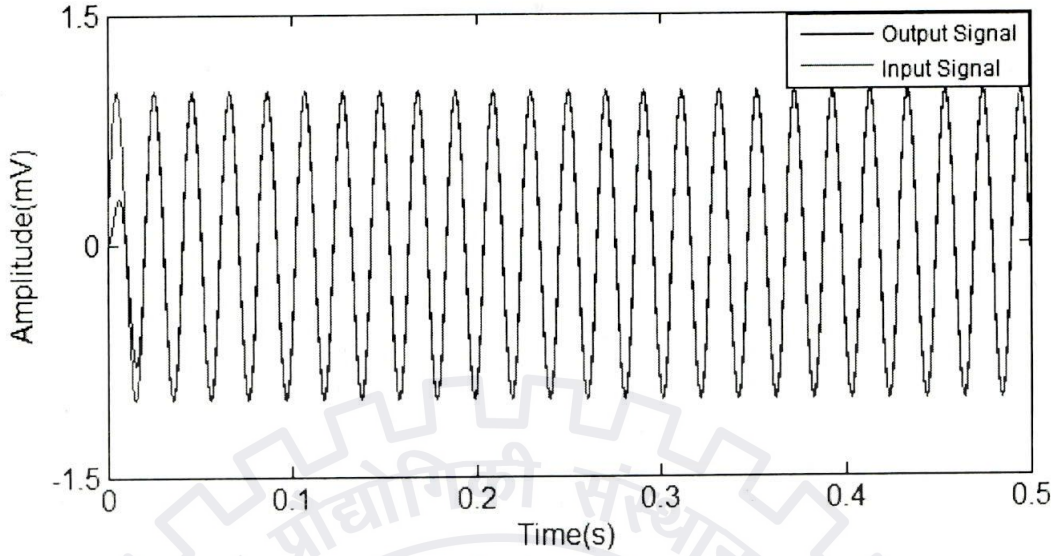


FIGURE 5.14: Locking performance of Goertzel based ADPLL at 49Hz with sinusoidal signal.

This scheme is tested for varying input frequency of sinusoidal signal such as 50.1Hz to 51Hz and also for 49.9Hz to 49Hz as shown above. Simulation results from Figure 5.5 to Figure 5.14 shows that, this proposed ADPLL gives accurate phase, amplitude and frequency locking for the above tested range for sinusoidal signal.It is noticeable that for every tested frequency the output is locking within one cycle of input signal.

5.3 Results of Proposed Scheme with ECG Signal

This scheme is implemented in ECG signal for removing power line noise which is artificially introduced in pure ECG signal. Since ECG signal is a non-stationary sinusoidal signal and filtration of this type of signal is very difficult task. The working of this adaptive canceller is discussed briefly in chapter 4. The ECG signal is 3.5mV signal and noise of 1mV is added, which is a very high value of noise. By simulation results we can conclude that this scheme extracting the pure ECG from a corrupted ECG signal. Figure 5.15 shows the performance result at center frequency i.e. 50Hz. At center frequency pure ECG signal is accurately extracted from corrupted ECG. In Figure 5.15 both signals seems like same or like one signal. Figure 5.15 shows the enlarged form of ADPLL performance at 50Hz.

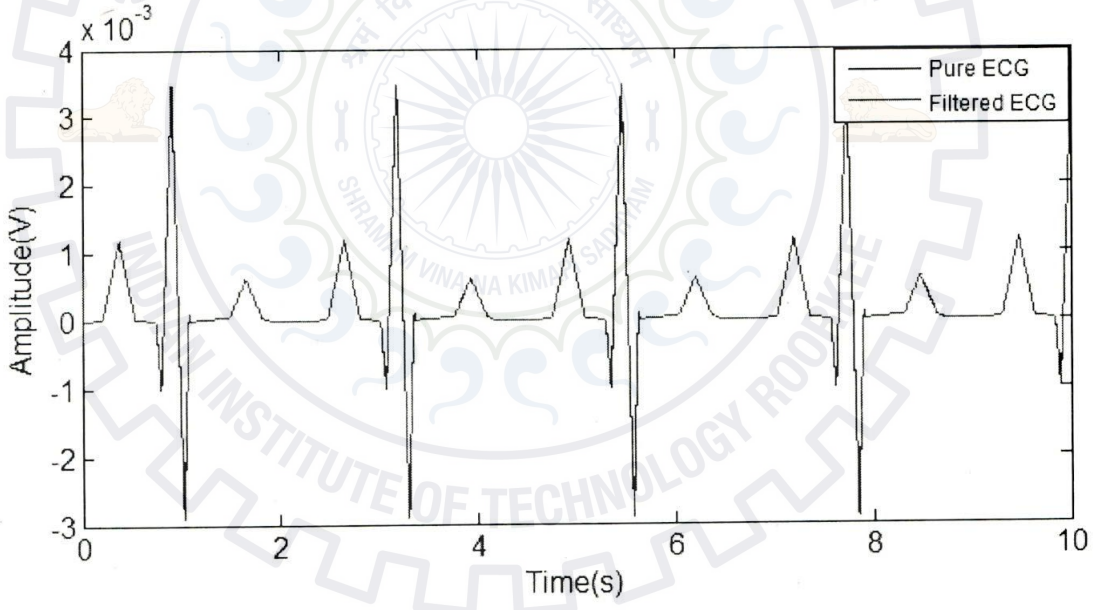


FIGURE 5.15: Performance of Goertzel based ADPLL at 50Hz with ECG signal.

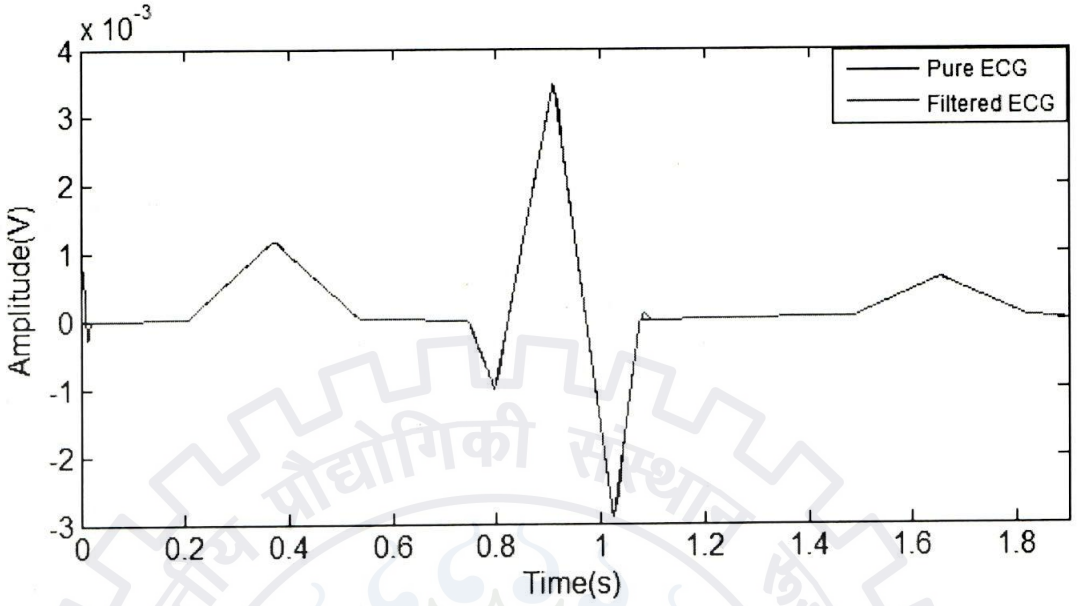


FIGURE 5.16: Performance of Goertzel based ADPLL at 50Hz with ECG signal(Enlarged).

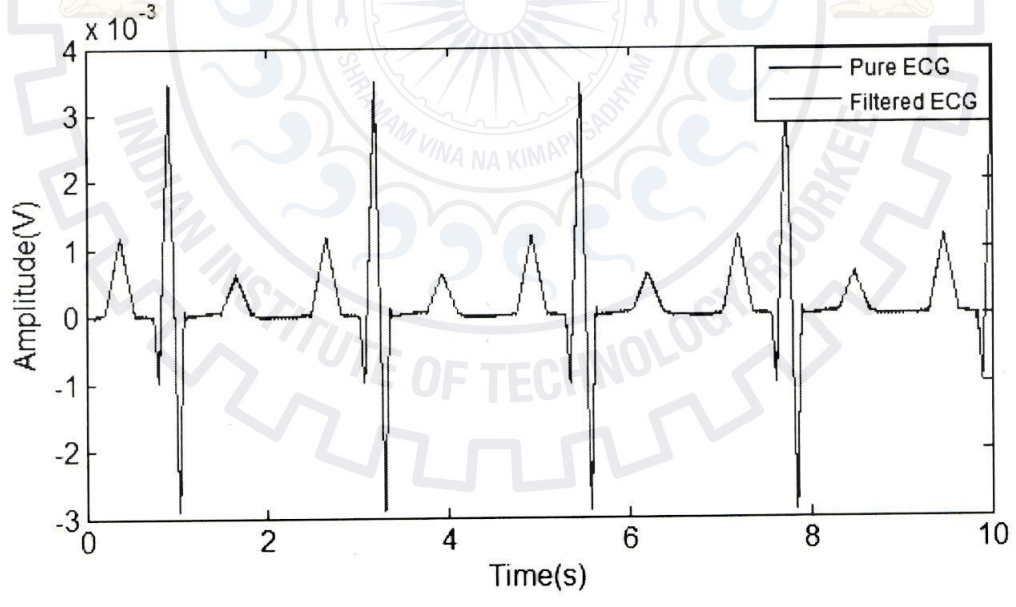


FIGURE 5.17: Performance of Goertzel based ADPLL at 50.2Hz with ECG signal.

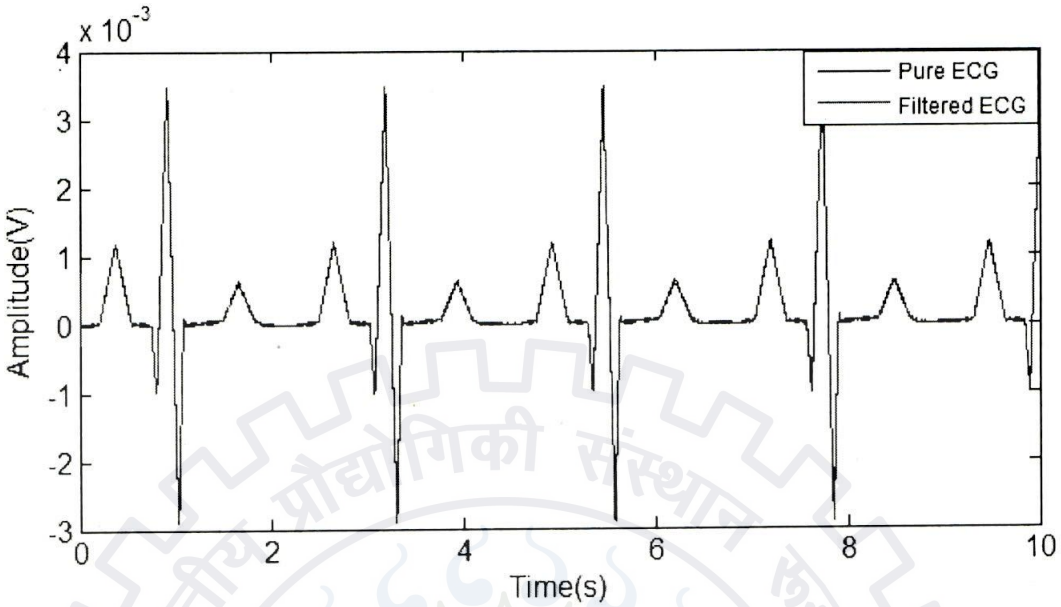


FIGURE 5.18: Performance of Goertzel based ADPLL at 50.3Hz with ECG signal.

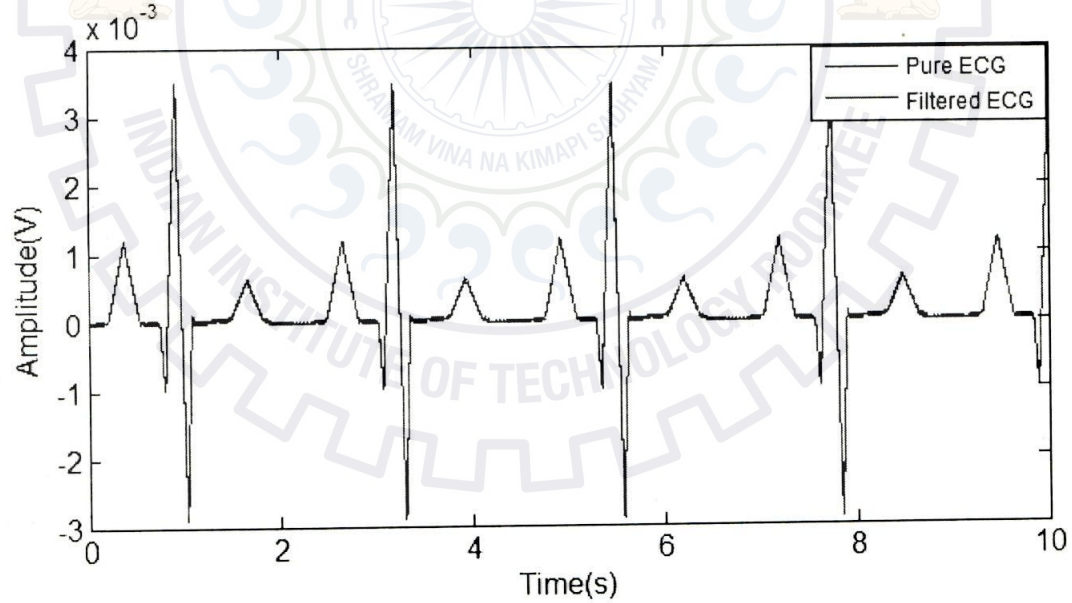


FIGURE 5.19: Performance of Goertzel based ADPLL at 50.4Hz with ECG signal.

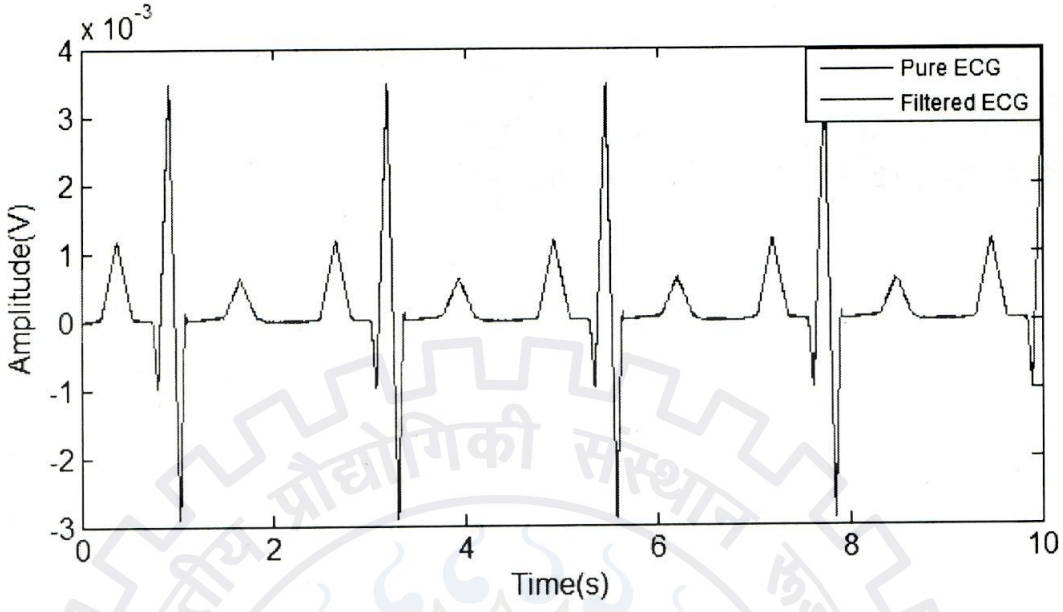


FIGURE 5.20: Performance of Goertzel based ADPLL at 49.9Hz with ECG signal.

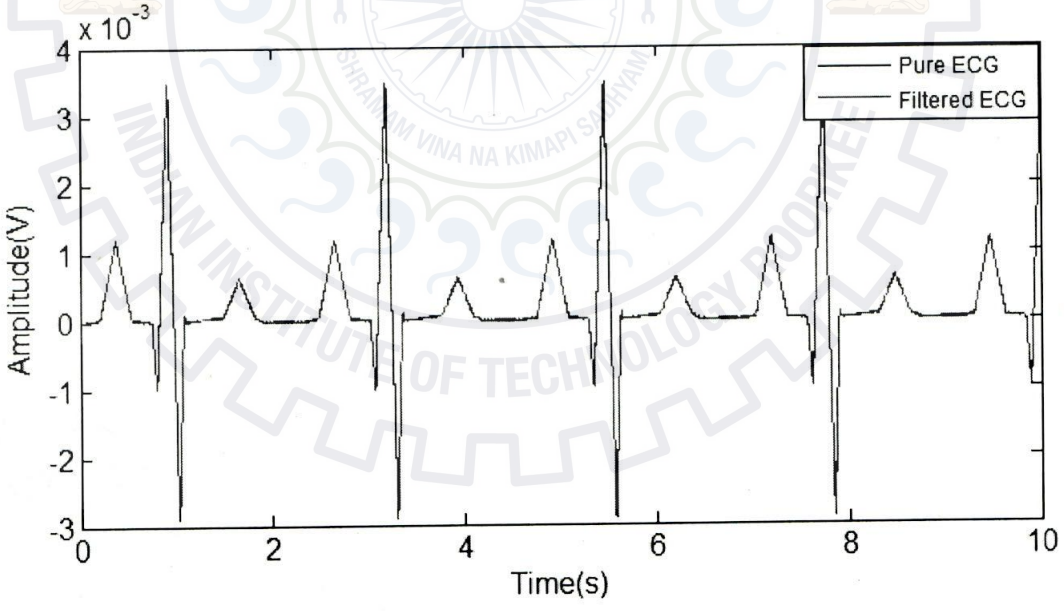


FIGURE 5.21: Performance of Goertzel based ADPLL at 49.8Hz with ECG signal.

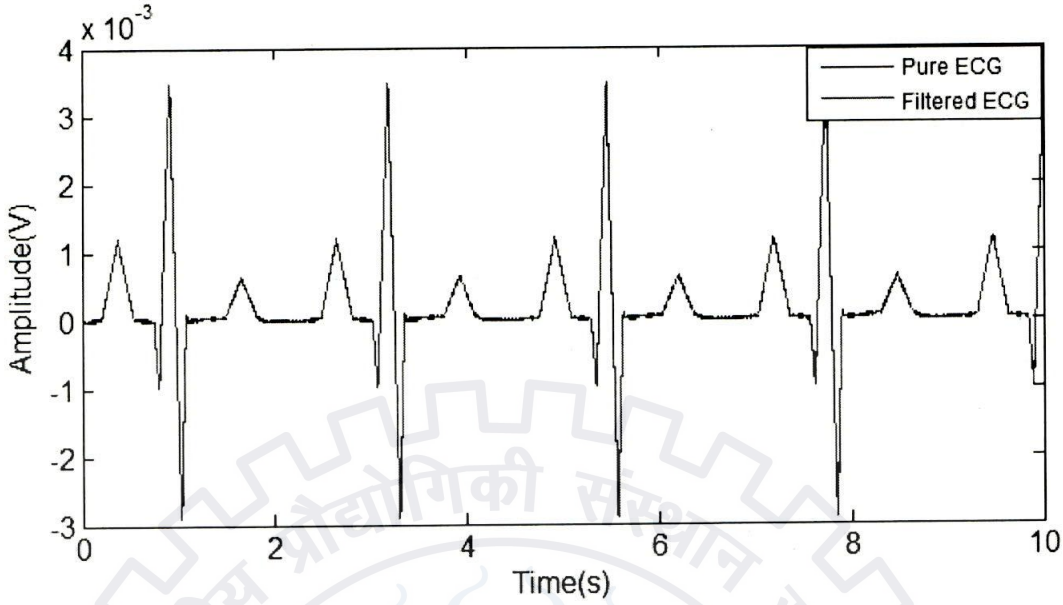


FIGURE 5.22: Performance of Goertzel based ADPLL at 49.7Hz with ECG signal.

Simulation results of proposed adaptive canceller with ECG signal is shown. Performance is checked by varying frequency range of power line interference from 50Hz to 50.4Hz and from 50Hz to 49.6Hz as shown in Figure 5.15 to Figure 5.22. Results show that at 50.4Hz and 49.6 scheme is giving some phase error but its value is very less i.e. approximately .0001mV. Future work can be done to remove this error completely.

Chapter 6

Summary

"When you concentrate your energy purposely on the future possibility that you aspire to realize, your energy is passed on to it and makes it attracted to you with a force stronger than the one you directed towards it."

-Stephen Richards

6.1 Conclusion

A Goertzel based all digital phase locked loop for removing power line interference from the ECG signal is proposed. The methodology is being executed by designing the blocks like Goertzel filter, phase detector, loop filter and DCO. The scheme is tested for simple sinusoidal signal for frequency range of 49.5 Hz to 51 Hz and simulation shows good results are obtained. This scheme is implemented on ECG signal for removing power line interference of the range of 49.6Hz to 50.4Hz. For the mentioned tested frequency range this scheme is satisfactorily removing power line interference from corrupted ECG signal and extraction of pure ECG signal

is done as a result. These features render the proposed ADPLL favorable for biomedical engineering applications and in noise cancellation.

6.2 Future Work

Proposed work deals with the phase locking of noise signal (in this proposed scheme it was power line interference of 50 Hz). The proposed technique can be extended to achieve the following points.

1. To get more accurate phase locking at given frequency.
2. To check the response of proposed technique for power line frequency deviations i.e. about ±3% of 50Hz.
3. To design the proposed scheme in Verilog.
4. To check the proposed technique with real time data as well.

Appendix A

Simulink Models

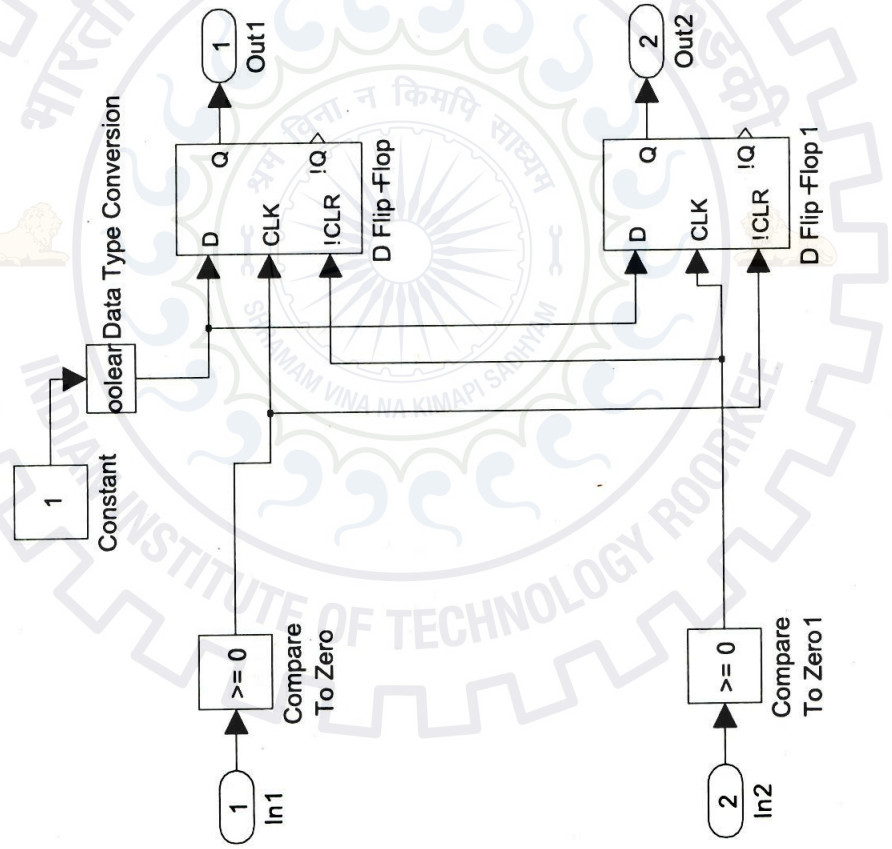


FIGURE A.1: Simulink Model of Phase Detector.

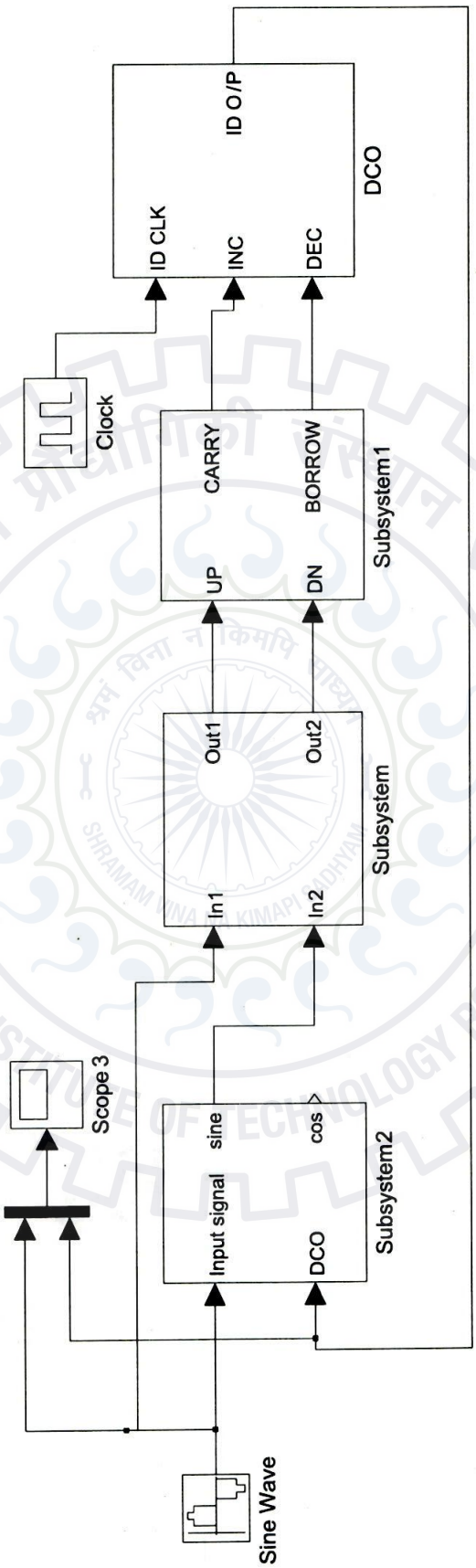
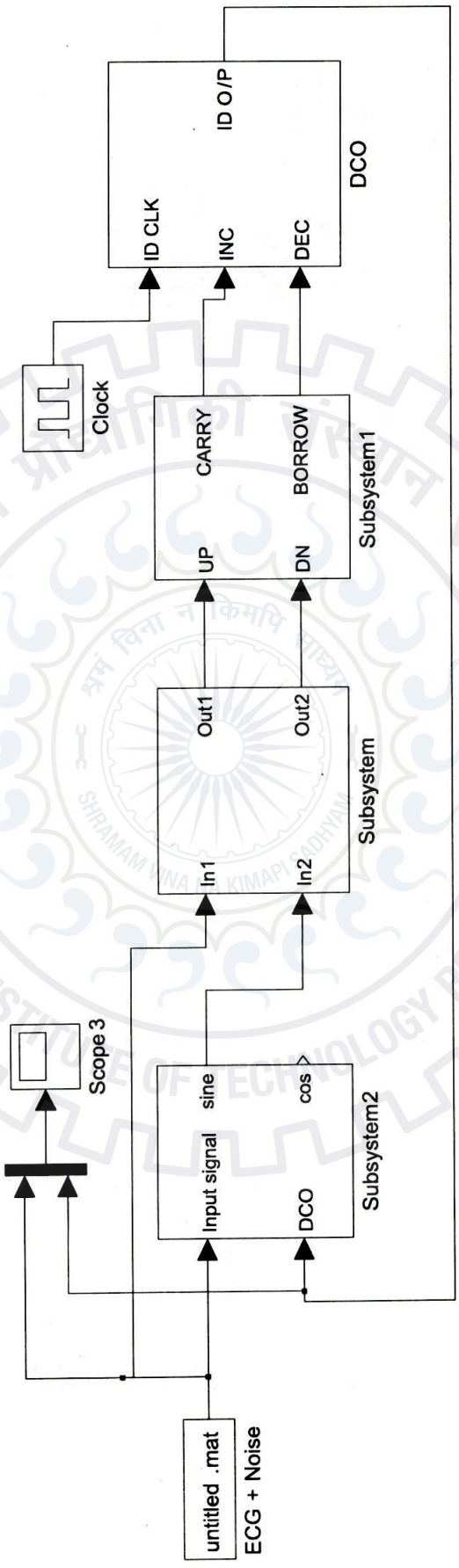


FIGURE A.2: Simulink Model of Proposed Scheme(with sinusoidal input).


ID O/P
DCO
ID CLK
INC
DEC
Clock
CARRY
BORROW
Subsystem1
UP
DN
Out1
Out2
Subsystem
In1
In2
Scope3
sine
cos
Input signal
DCO
Subsystem2
untitled .mat
ECG + Noise

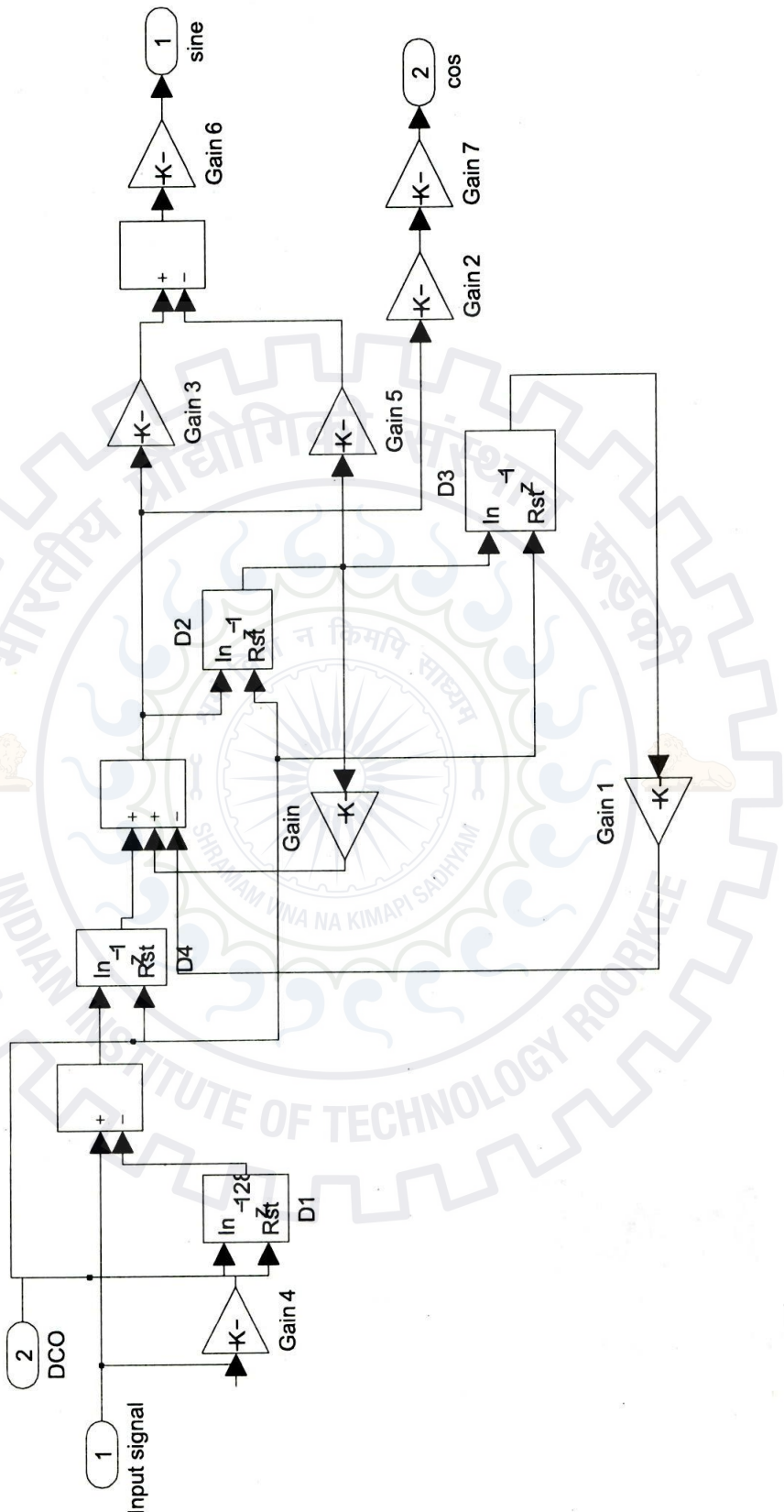


FIGURE A.4: Simulink Model of Goertzel Filter.

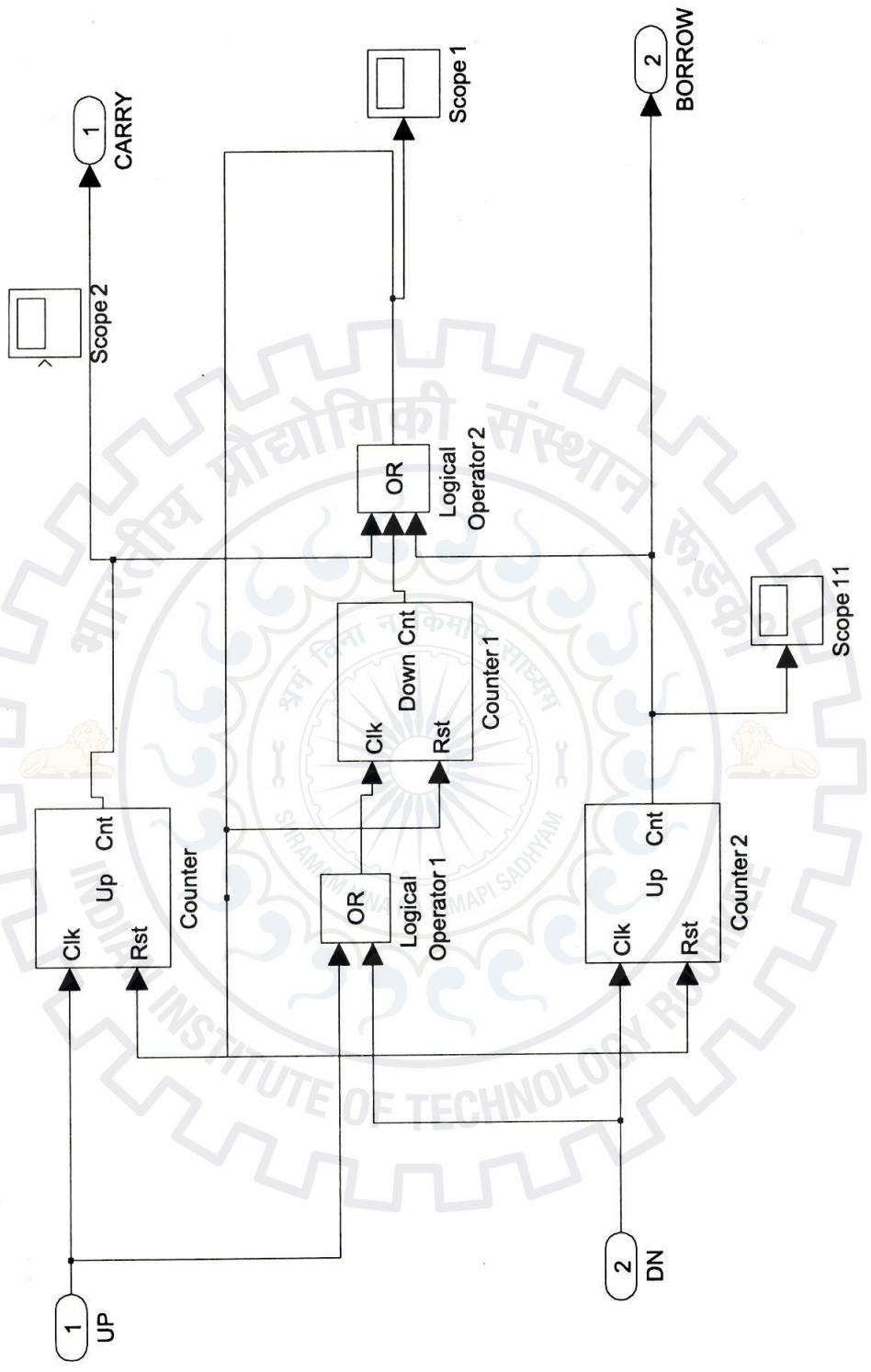


FIGURE A.5: Simulink Model of Loop Filter.

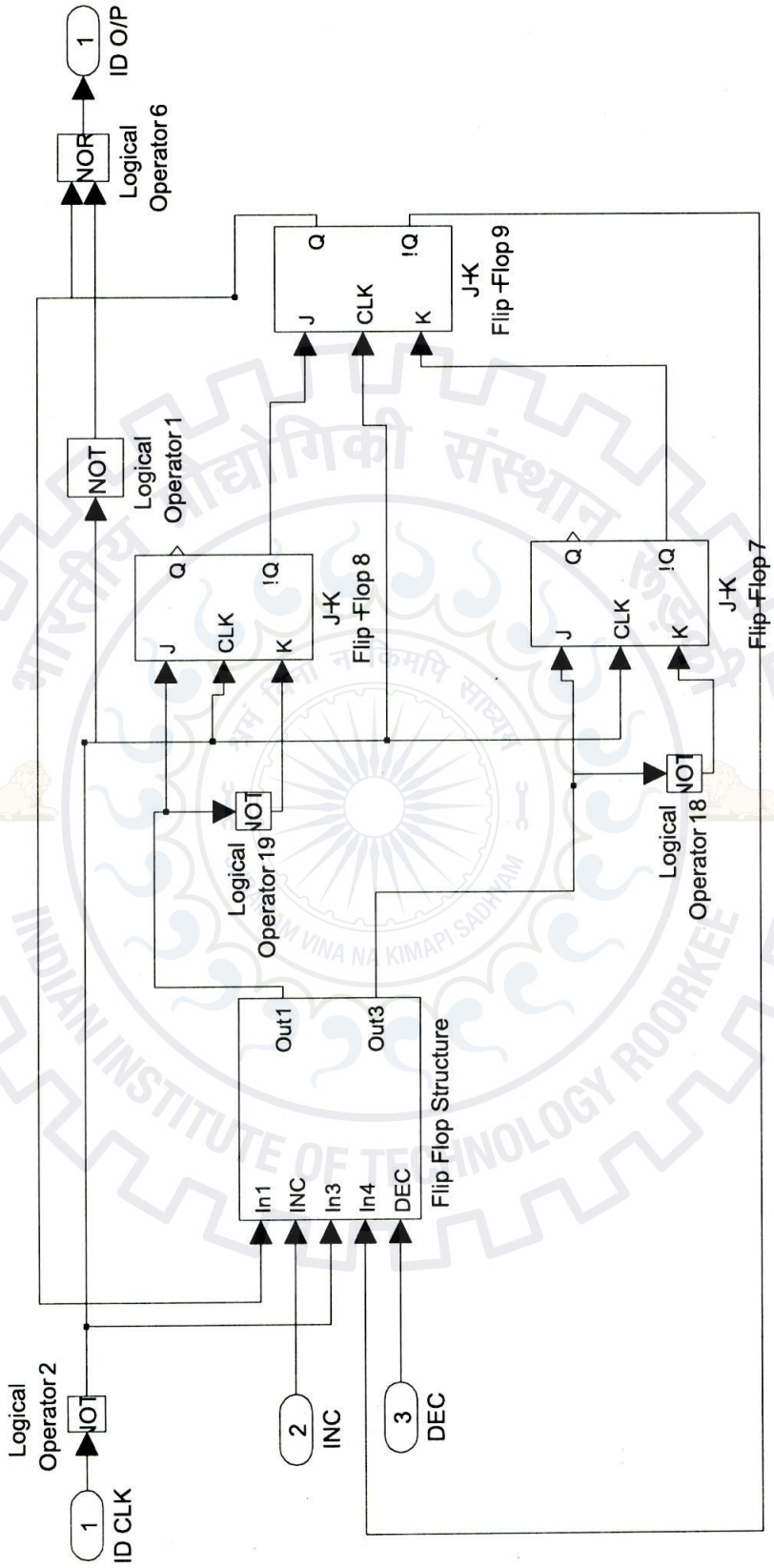


FIGURE A.6: Simulink Model of ID Counter DCO.

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