SLIDING MODE CONTROL OF PUSH-PULL CONVERTER

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ELECTRICAL ENGINEERING

(With Specialization in Electric Drives and Power Electronics)

By

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INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

CANDIDATE'S DECLARATION

I hereby declare that the work that is being presented in this dissertation entitled, **"SLIDING MODE CONTROL OF PUSH-PULL CONVERTER"** in partial fulfilment of the requirements for the award of degree in **Master of Technology** in **Electrical Engineering** With Specialization in **"Electric Drives & Power Electronics"** submitted to the **Department of Electrical Engineering, Indian Institute of Technology, Roorkee, INDIA** is an authentic record of my own work carried under the guidance of **Dr. S. P.Singh, Professor,** Department of Electrical Engineering, Indian Institute of Technology, Roorkee.

The matter embodied in this dissertation report has not been submitted by me for the award of any other degree or diploma.

Date: 19 June 2013
Place: IIT Roorkee

KUNAL SHIVAJI NARAD
(M.TECH. EDPE)

CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge and belief.

13/6/13

Date: 19 June 2013
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ABSTRACT

State space averaging method is used for obtaining the transfer function of Push-Pull converter. Using SISOTOOL in MATLAB tuning of PI controller is obtained. Performance of sliding mode controller for Push-Pull converter is investigated by PSIM software. The PI controller simulation results compared with sliding mode controller. From simulation results it can be observed that sliding mode controller provides better control strategy than PI controller.

With the help of 'Simcoupler Module' which is used for co-simulation of PSIM software and MATLAB, Push Pull converter circuit in open loop configuration as well as with sliding mode controller in closed loop is simulated using Xilinx tool box. Using FPGA (Field programmable gate array) SPARTAN 3 kit, pulses required for converter operation are generated. Prototype model of Push-Pull converter is tested in open loop configuration.

ACKNOWLEDGEMENT

The euphoria and joy, accompanying the successful completion of my task would be incomplete without the special mention of those people whose guidance and encouragement made my effort successful.

I am deeply indebted to my guide Prof. S.P.Singh in department of Department of Electrical Engineering and K.P.Guruswamy, research scholar of Indian Institute of Technology, Roorkee, whose help, stimulating suggestions and encouragement helped me in all the time to make my effort successful.

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Switched mode power converters (SMPS) are efficient for dc-to-dc power conversion. It consists of reactive elements and switches. DC/DC converters are basically classified as non-isolated converters and isolated converters. Buck, Boost, Buck-Boost converters are few examples of non-isolated converters. While Forward, Push-pull, Flyback converters are some examples of isolated converters. An isolated converter has many advantages over non-isolated converters. Push-Pull converter is isolated type of Buck converter. In which transformer is used to isolate load circuit from the line circuit. Push-Pull topology is similar as Forward converter with only difference is Push-Pull converter has two primaries where as Forward converter has only one primary winding. The primary switches alternately power their respective windings. In order to avoid shorting out of power supply small interval provided between turning on of the two switches. The secondary is arranged in a centre tapped configuration. The maximum power capability of a Push-Pull transformer to be twice that of a Forward transformer.

DC/DC converters are non-linear in nature. Any disturbance in line side or load side as well as if there is any situations which causes the parameter variations causes performance behaviour of the converter operation. In order to overcome this problems various kinds of controllers are used. PI controller is widely used controller for converter control operations. Sliding mode control strategy leads to large signal stability compared to the state space average method. Sliding Mode approach for Variable Structure Systems (VSS) offers an alternative way to implement a control action which exploits the inherent variable structure nature of DC-DC converters. In particular, the converter switches are driven as a function of the instantaneous values of the state variables in such a way so as to force the system trajectory to stay on a suitable selected surface on the phase space called the sliding surface. Sliding mode controller provides very robust control system.

As compared to analogue controller digital controller has many advantages like simplicity, accuracy, compactness. Digital signal processor (DSP), Microprocessors (μP), Field programmable gate array (FPGA) are widely used as controller techniques for dc-dc converter applications. But FPGA technique has an edge over DSP and μP like low power consumption, high efficiency, able to operate on higher frequencies and its simplicity of implementation.

1.1 Various dc-to-dc Power Converters

- Buck Converter
- Boost Converter
- Buck-Boost Converter
- Forward Converter
- Single Ended Primary Inductor Converter
- Push-pull converter

1.1.1 Buck converter

✓ Voltage step down only

- ✓ Single output only
- ✓ Very high efficiency
- ✓ Low input ripple current
- ✓ High output ripple current

1.1.2 Boost converter

- ✓ Voltage step up only
- ✓ Single output only
- ✓ Very high efficiency

1.1.3 Forward converter

- ✓ Buck type converter with an added isolation transformer
- ✓ Step up or step down voltage level
- ✓ Multiple outputs are possible

1.1.4 Push-Pull converter

Circuit Diagram:

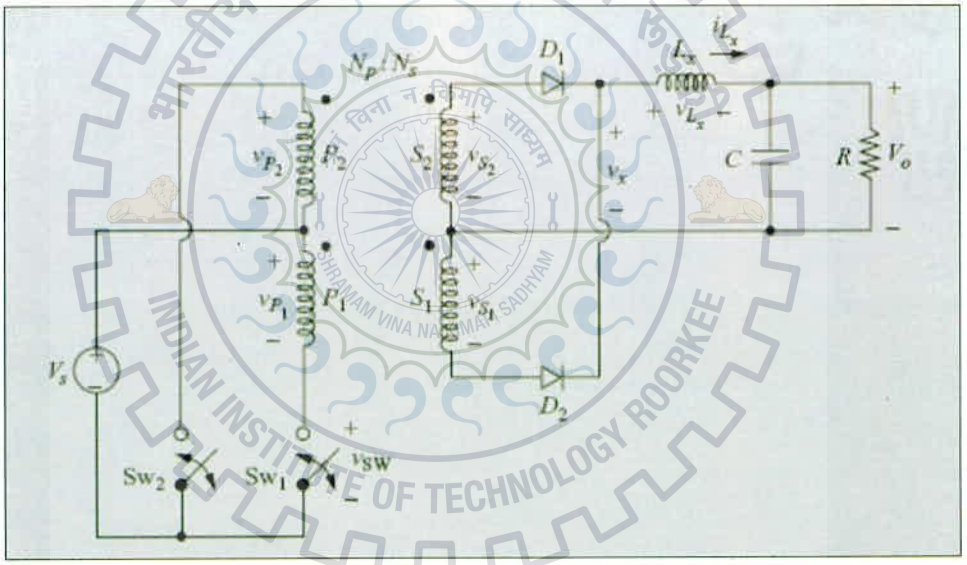


Figure 1.1 Circuit of Push-Pull converter

- ✓ Push-pull converter is similar to a forward converter except Push-Pull converter having two primaries.
- ✓ Two primary winding are alternately switched by two different primary switches.
- ✓ In order to avoid shorting out of power supply small interval provided between turnings on of the two switches.
- ✓ Primary winding as well secondary winding are arranged in a centre-tapped configuration.
- ✓ When Sw1 is turned on current starts flowing through diode D1. When switch Sw2 tuned on current starts flowing through diode D2.

- ✓ The Forward converter operates in a single quadrant of the BH curve, moving up the curve when the switch is active and resetting during the OFF time.
- ✓ The Push-Pull converter operates in two quadrants of the BH curve. Due to which the maximum power capability of a Push-Pull transformer to be twice that of a Forward transformer.

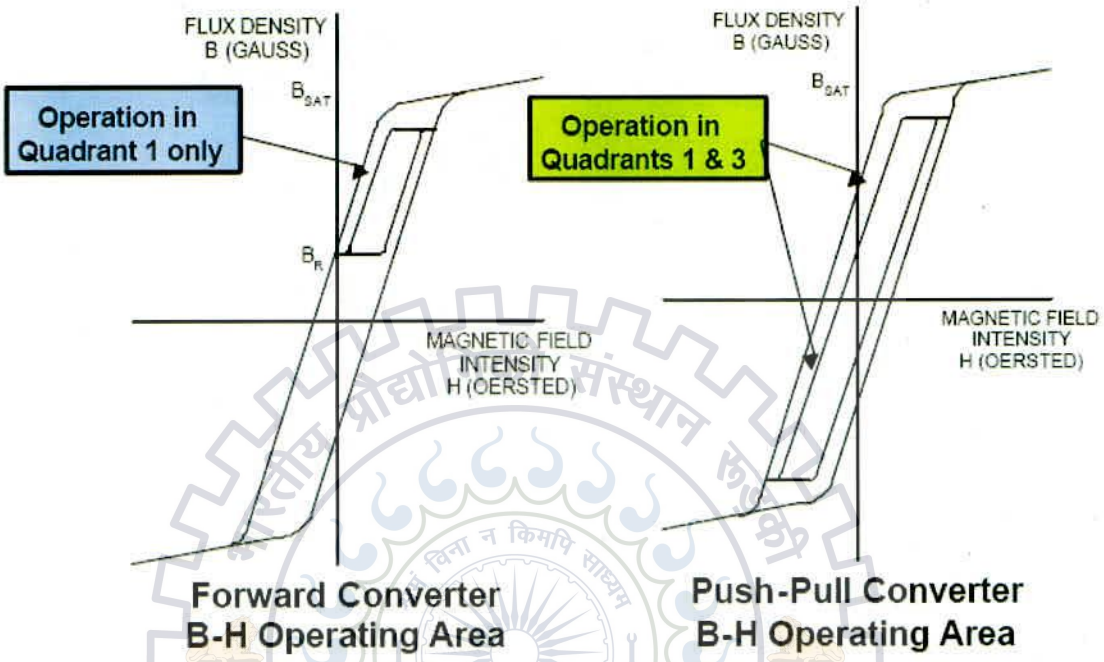


Figure 1.2 B-H characteristics of Forward and Push-Pull converter

- ✓ Step up or step down voltage level
- ✓ Multiple outputs are possible
- ✓ Large Achievable Duty Cycle Range.

Switching pulses:

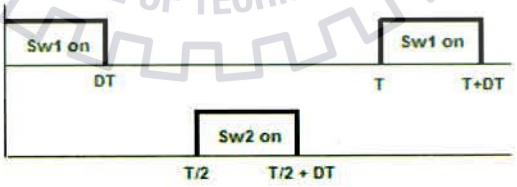


Figure 1.3 Switching pulses for Push-Pull converter

Working:

Push-Pull converter operated in four modes. In first mode ($0 < t < DT$) switch one (Sw_1) is closed and switch two (Sw_2) remains open, which makes upper secondary winding of transformer forward biased and lower secondary winding reverse biased. Hence diode D1 becomes forward biased and diode D2 becomes reverse biased. Current starts flowing through diode D1. In second mode ($DT < t < \frac{T}{2}$) both the switches remains open. The current through inductor must maintain continuity, resulting in both diodes D1 and D2 becoming forward biased. In third

mode $\frac{T}{2} < t < \frac{T}{2} + DT$ switch two (Sw_2) is closed and switch one (Sw_1) is open which makes lower secondary winding of transformer become forward biased. Due to this diode D2 become forward biased and diode D1 become reversed biased and current starts flowing through D2. And in fourth mode $\frac{T}{2} + DT < t < T$ again both the switches are remain open similar as in mode two.

O/P Voltage equation of Push-Pull converter:

$$V_o = 2V_s D\left(\frac{N_s}{N_p}\right)$$

In the past, the method of state space averaging had been successfully applied to characterize DC/DC converters. The variable structure system (VSS) of the DC/DC converters is an alternative method of characterizing the dc-to-dc converters in the time domain. State space averaging method essentially develops a linear, small signal, frequency domain model of nonlinear power converters. One of the widely used methods of controlling the output voltage of DC/DC converters is by means of close loop control of the duty ratio. In order to design such close loop controllers, it is necessary to obtain a dynamic model of duty ratio controlled converters The choice of average modeling method to study both large and small signal characteristics of modern power converters has become widely accepted due to its adaptability to computer simulation. When an average model is simulated, it requires with less computation time than the switched circuit model.

Circuit diagram:

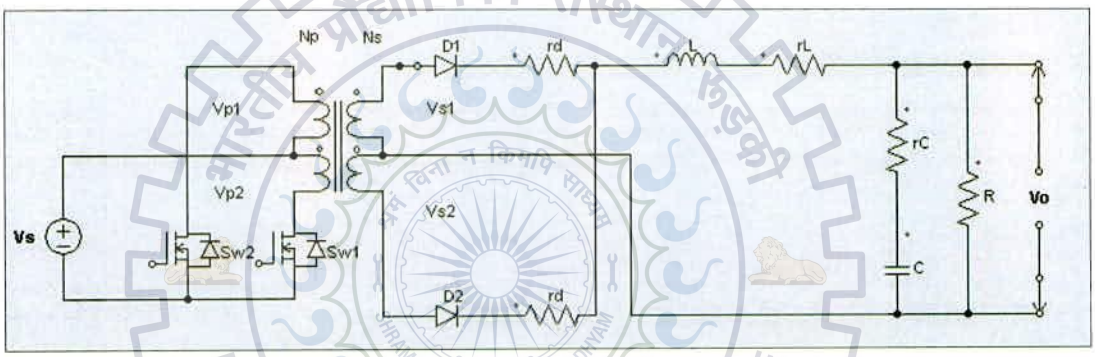


Figure 2.1 Schematic of Push-Pull converter

Firing pulses for switches:

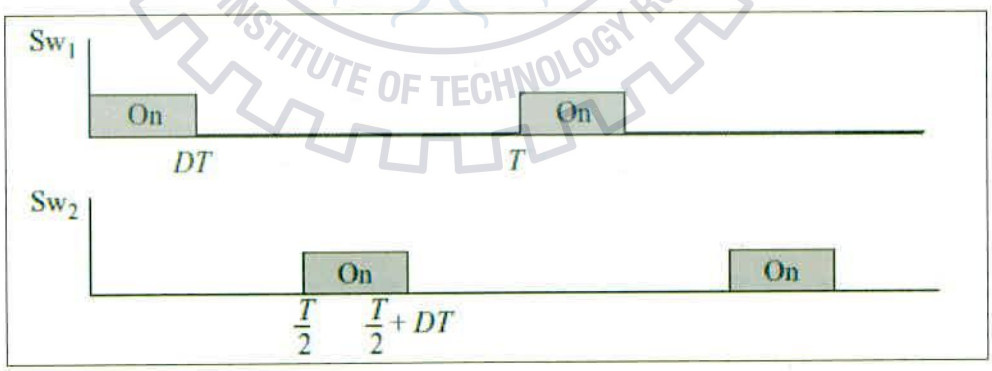


Figure 2.2 Pulses for switches

For deriving averaged model and modelling of Pull-Pull converter following assumptions are made:

1) Both the switches (S_{w1}, S_{w2}) and diodes (D_1, D_2) are identical.
2) Both the diodes (D_1, D_2) having on resistance r_d.

3) Inductor and capacitor have parasitic resistance rL and rC respectively.
4) Converter is assumed to be operates in continuous conduction mode (CCM).
5) Since there are two energy storing elements inductor and capacitor, so there are two state variables including inductor current and capacitor voltage.

In each half cycle Push Pull converter has two modes of operation:

Mode 1: 0 < t < DT

In Mode 1, switch Sw1 is on which causes diode D_1 forward bias. Current stars flowing through upper secondary winding. Circuit model for this mode is shown,

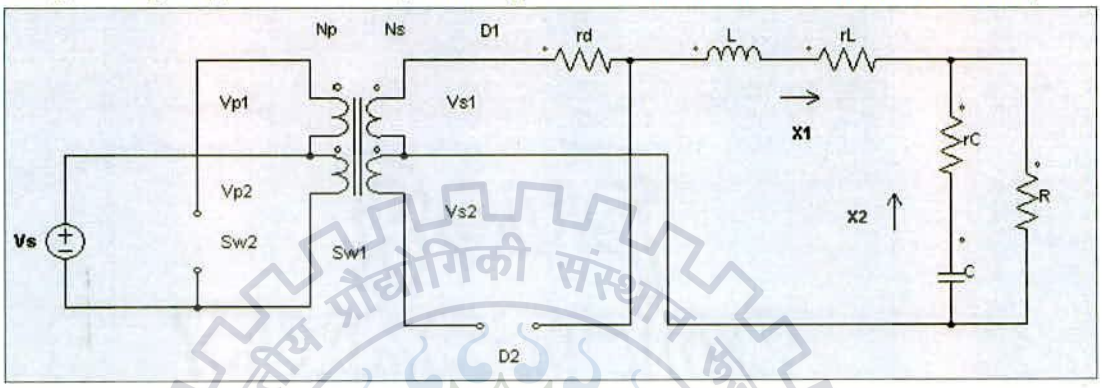


Figure 2.3 Mode 1 operation

State equations of the circuit are obtained by applying KVL and KCL. State variable for inductor current and capacitor is voltage is X_1 and X_2respectively.

$$\dot{X_1} = -X_1\frac{1}{L}\left(rd + rL + \frac{R * rC}{R + rC}\right) - X_2\left(\frac{R}{R + rC}\right) + V_s\left(\frac{N_s}{N_p}\right)$$

$$\dot{X_2} = X_1\left(\frac{R}{R + rC}\right) - X_2\frac{1}{C}\left(\frac{1}{rC + R}\right)$$

$$V_o = X_1R\left(\frac{rC}{R + rC}\right) + X_2R\left(\frac{1}{R + rC}\right)$$

Therefore the matrices in the interval DT are:

$$\dot{X} = A_1X + B_1V_s$$

$$V_o = C_1X$$

$$A_1 = \begin{bmatrix} \frac{1}{L}\left(rd + rL + \frac{R * rC}{R + rC}\right) & \left(\frac{R}{R + rC}\right) \\ \left(\frac{R}{R + rC}\right) & \frac{1}{C}\left(\frac{1}{rC + R}\right) \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{L}\left(\frac{N_s}{N_p}\right) \\ 0 \end{bmatrix}$$

$$C_1 = \begin{bmatrix} R\left(\frac{rC}{R + rC}\right) & R\left(\frac{1}{R + rC}\right) \end{bmatrix}$$

Mode 2: $\frac{T}{2} < t < \frac{T}{2} + DT$

In Mode 2, both the switches (S_{w1}, S_{w2}) are open and load current starts flowing through both the diodes (D_1, D_2).

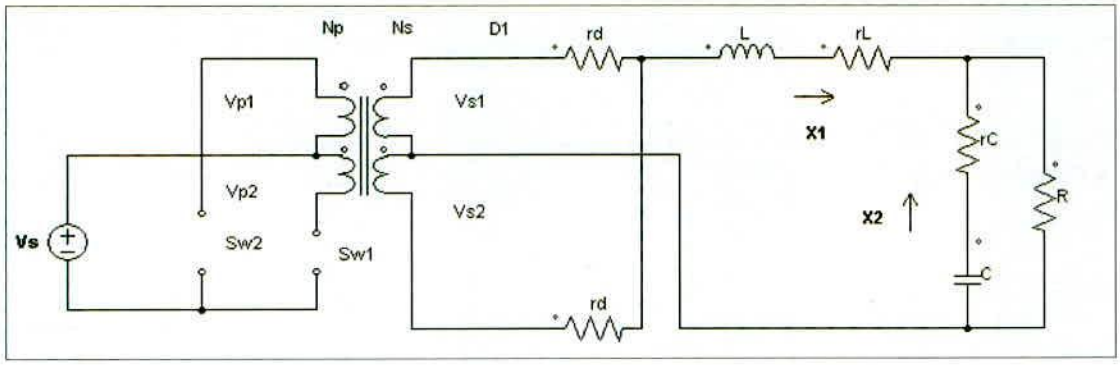


Figure 2.4 Mode 2 operation

Again there are following equations:

$$\dot{X_1} = -X_1 \frac{1}{L}\left(\frac{rd}{2} + rL + \frac{R * rC}{R + rC}\right) - X_2\left(\frac{R}{R + rC}\right)$$

$$\dot{X_2} = X_1\left(\frac{R}{R + rC}\right) - X_2 \frac{1}{C}\left(\frac{1}{rC + R}\right)$$

$$V_o = X_1 R\left(\frac{rC}{R + rC}\right) + X_2 R\left(\frac{1}{R + rC}\right)$$

In this mode state matrices are:

$$A_2 = \begin{bmatrix} -\frac{1}{L}\left(\frac{rd}{2} + rL + \frac{R * rC}{R + rC}\right) & -\left(\frac{R}{R + rC}\right) \\ \left(\frac{R}{R + rC}\right) & \frac{1}{C}\left(\frac{1}{rC + R}\right) \end{bmatrix}$$

$$B_2 = 0$$

$$C_2 = \begin{bmatrix} R\left(\frac{rC}{R + rC}\right) & R\left(\frac{1}{R + rC}\right) \end{bmatrix} = C_1$$

Finally, based on averaged model concept and because the half cycle model of this converter in $\frac{T}{2}$ as:

$$\dot{X} = AX + BV_s\ , \qquad V_o = CX$$

$$A = A_1 2d + A_2(1 - 2d) \qquad \text{(a)}$$

$$B = B_1 2d \qquad \text{(b)}$$

$$C = C_1 \qquad \text{(c)}$$

2.1 Steady state analysis

With the model of state space equation and matrices A, B and C we can consider small perturbation (represented by ~) and dc steady state (in upper case letters) quantities for model parameter as:

$$x = X + \tilde{x}$$

$$v_0 = V_0 + \widetilde{v_0}$$

$$d = D + \tilde{d}$$

$$v_s = V_s + \widetilde{v_s}$$

Substitution of this parameter into state equations (a), (b) and (c) yield:

$$\dot{\tilde{x}} = AX + BV_s + (A\tilde{x} + B\widetilde{v_s}) + [(A_1 - A_2)X + (B_1 - B_2)V_s]2\tilde{d} \quad \text{(d)}$$

+ terms with product of $\tilde{x}, \tilde{d}, \widetilde{v_s}$ (negligible)

$$V_o + \widetilde{v_o} = CX + C\tilde{X} + [(C_1 - C_2)X]2\tilde{d} \quad \text{(e)}$$

+ terms with product of $\tilde{d}, \widetilde{v_s}$ (negligible)

The steady state equation can be obtained from equations (d) and (e) by setting all ac components to zero. Therefore the steady state equation is,

$$AX + BV_s = 0$$

And for output: $V_0 = CX$

From the equations (d) and (e),

$$\dot{\tilde{x}} = A\tilde{x} + B\widetilde{v_s} + [(A_1 - A_2)X + (B_1 - B_2)V_s]2\tilde{d} \quad \text{(f)}$$

$$\widetilde{v_0} = C\tilde{x} + [(C_1 - C_2)X]2\tilde{d} \quad \text{(g)}$$

2.2 Small signal analysis

From equations (f) and (g) that consists of ac perturbation and using Laplace transform:

$$\tilde{x}(s) = (SI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_d]2\tilde{d}(s) + (SI - A)^{-1} + B\widetilde{V_s}(s)$$

(h)

$$\widetilde{V_0}(s) = C\tilde{x}(s) + [(C_1 - C_2)X]2\tilde{d}(s) \quad \text{(i)}$$

From equations (h) and (i) we get the Laplace transform output voltage in term of duty cycle and input voltage:

$$\widetilde{v_0}(s) = \{C(SI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_s] + (C_1 - C_2)X\}2\tilde{d}(s) + C(SI - A)^{-1}B\widetilde{V_s}(s)$$

The perturbation of input voltage is assumed to be zero and for obtaining transfer function of output voltage to duty cycle and hence,

$$\frac{\widetilde{v_0}(s)}{\tilde{d}(s)} = 2C(SI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_s] + 2(C_1 - C_2)X$$

After substituting the matrix values we get the transfer function as:

Converter transfer function:

$$\frac{\widetilde{v_0}(s)}{\tilde{d}(s)} = \frac{1.876e05\ s\ +\ 5.717e09}{s\text{^}2\ +\ 3.602e04\ s\ +\ 1.691e08}$$

The push-pull switching converter is considered a transformer-isolated variation of the buck converter, and probably the most widely used type of power conversion circuit. In this design, the primary of the transformer can be connected in several ways: push-pull, half bridge or full bridge depending upon how one drives the transformer. The push-pull converter is, in fact, an arrangement of two forward converters on a single core. Push-pull converters reduce output voltage ripple by doubling the ripple current frequency to the output filter. A further advantage of push-pull operation is that magnetization is applied to the transformer core in both directions. The push-pull converter transformer, when subjected to small amounts of dc imbalance, can lead to core saturation.

Design Specifications:

Input voltage (V_s)= 100v

Output voltage (V_o)= 24v

Output current (I_o)= 15A

Operating frequency= f= 100 kHz

Regulation (α)= 0.5

Efficiency (η)= 0.95

Total dwell time (t_{dw})= 1μs

Operating flux density (B_m) = 0.11T

MOSFET on resistance (R_Q) = 0.1Ω

Diode voltage drop=1V

3.1 Transformer design

1) Maximum apparent secondary power= $P_{ts} = I_o(V_o + V_s)\sqrt{2} = 530.33W$
2) Apparent power = $P_t = P_{ts}\left(\frac{\sqrt{2}}{\eta} + 1\right)$= 1319.8W
3) Electrical co-efficient = $K_e = 0.145(f)^2(k_f)^2(B_m)^2 10^{-4}$

   $k_f = \text{waveform co} - \text{efficeint} = 4(\text{square wave})$

   $\therefore K_e = 28072$

4) Core geometry = $K_g = \frac{P_t}{2K_e\alpha} = 0.047cm^5$

(When designing with bobbin ferrite or other small bobbin cores, the core geometry is multiplied by 1.25)

$$K_g = 1.25 * 0.047 = 0.0587 cm^5$$

5) From core table RM core with core number KM-42819 is selected. (refer Appendix A)
6) Time period= T= $\frac{1}{f}$=10μs
7) Maximum on time= t= $\frac{T}{2}$μs

$$t_{on}(max) = t - t_{dw} = 4\mu s$$

8) Maximum duty ratio= $D_{max} = \frac{t_{on}(max)}{t} = 0.4$
9) Current density= J= $\frac{P_t * 10^4}{K_f K_u B_m f A_p} = 1597.71\ A/cm^2$

$$K_u = \text{window utilization} = 0.3$$

10) Secondary load power=$P_{to} = I_o(V_o + V_s) = 375W$
11) Average primary current=$I_{in} = \frac{P_{to}}{\eta V_s} = 3.94\ A$
12) Peak primary current= $I_p = \frac{I_{in}}{2D_{max}} = 4.93\ A$
13) Average primary voltage=$V_p = V_s 2D_{max} I_p R_Q = 39.44v$
14) Primary turns= $N_p = \frac{V_p * 10^4}{K_f B_m f A_c} = 9.146 \cong 10$ turns

$$A_c = \text{Iron area}$$

15) Secondary turns=$N_s = \frac{N_p(V_o + V_d)}{V_p} = 6.34 \cong 6\ turns$
16) Skin depth= γ= $\frac{6.62}{\sqrt{f}} = 0.0209cm$
17) Wire area= $\pi * r^2$=0.00137cm^2
From wire table AWG#26 wire is selected. (refer Appendix B)

3.2 Converter design

$$V_o = V_s \left(\frac{N_s}{N_p}\right) 2D$$

Duty ratio=D=0.2

Load resistance= R= $\frac{V_o}{I_o} = 1.6\Omega$

Assume the ripple in inductor current is 20% (=ΔI_{Lx})

$$\Delta I_{Lx} = \frac{V_o(1/2 - D)T}{L}$$

Inductor= L= 24μH

Assume ripple in output voltage is 1%

0.01=$\frac{1-2D}{32f^2LC}$

Capacitor= C= 7.81μF

Parasitic resistance of capacitor and inductor assume approximately 0.08Ω and 0.05Ω.

Design summary:

Core= RM core (KM-42819)

Magnetic material= Ferrite core

Wire type= Litz wire

Frequency= 100kHz

Wire = AWG#26

Primary turns= 10

Secondary turns= 6

L= 24μH

C= 7.81μF

R= 1.6Ω

4.1 Basic structure of controller

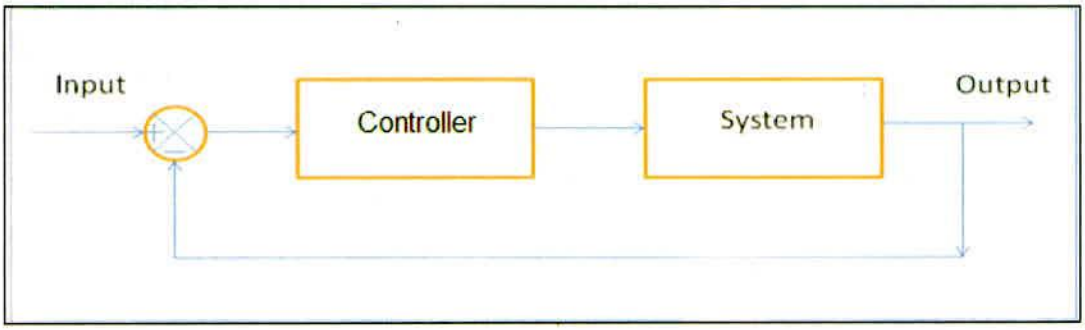


Figure 4.1 Controller structure

A proportional–integral–derivative controller (PID controller) is most widely used in controller for converter applications. Input to the controller is 'error' which is difference between a measured value and desired value. The controller reduces the error by adjusting the controller parameters.

The PID controller consists of three different controller parameters, namely, proportional, integral and derivative denoted P, I, and D respectively. And depending upon the required desired response, proportional and integral term of the PI controller is tuned. By tuning the proportional term rise time of the response can be reduced and by tuning the integral term steady state can be reduced to zero and with tuning of derivative term transients can be reduced.

Tuning of PI controller using SISOTOOL

In order to get desired response of the controller it is necessary to have the controller parameters should be tuned properly. There are various methods like Manual tuning, Ziegler- Nichols method, Software tools adopted for calculation of controller gain parameters. 'SISOTOOL' which is inbuilt function in MATLAB uses converter transfer function to obtain the controller parameters. This tool enables to plot various responses like step, impulse, bode, nyquist for various controller structures, which helps to understand and select appropriate controller for converter.

Converter transfer function of converter

$$\frac{\widetilde{v_0}(s)}{\tilde{d}(s)} = \frac{1.876e05\ s\ +\ 5.717e09}{s\text{^}2\ +\ 3.602e04\ s\ +\ 1.691e08}$$

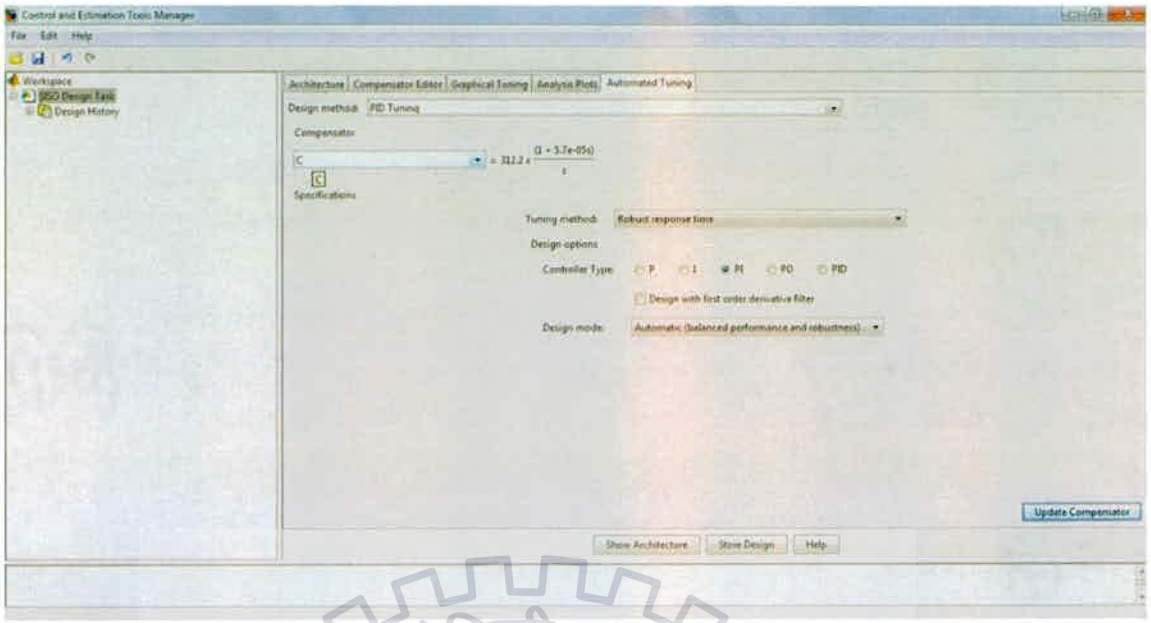


Figure 4.2 Command window of SISOTOOL

Command window of SISOTOOL is shown in Fig. 4.2. This can be obtained from the converter transfer function. SISOTOOL enables to select the type of design method, type of tuning method, the architecture of the controller as well the controller type. By selecting desired controller and the tuning method various responses can be ploted easily.

4.1.1 Step response of the converter without controller

Figure 4.3 shows the step response of the converter without controller. This gives the amplitude of 34 with settling time of around 1ms. To reduce the settling time as well as to reduce the large steady state error, controller is required to get desired response.

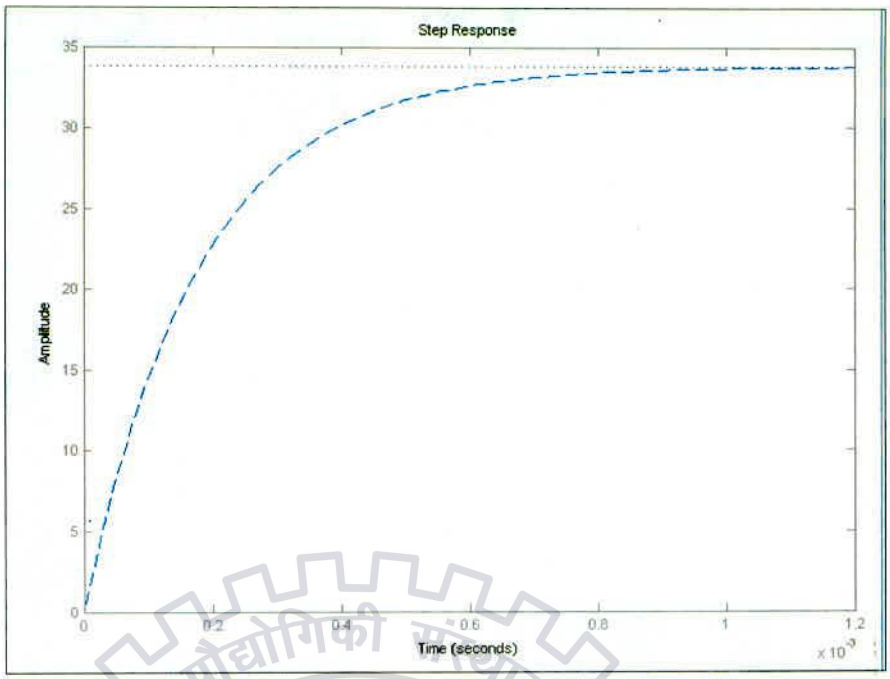


Figure 4.3 Step response of the converter without controller

4.1.2 Step responses of different type controllers

4.1.2.1 Proportional (P) Controller

Figure 4.4 shows the step response of the converter with the proportional (P) controller. As compared to the step response without controller the settling time as well as the steady state reduces.

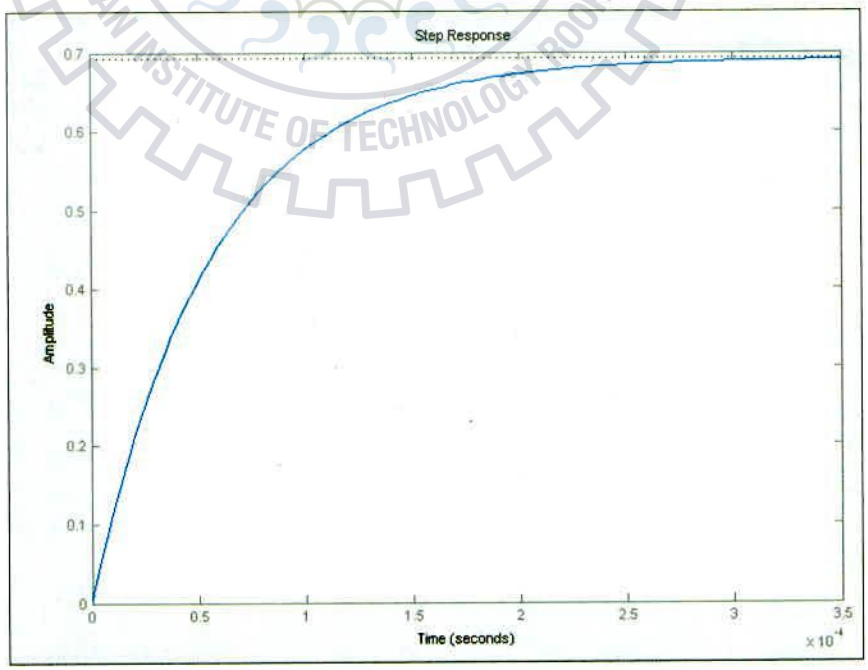


Figure 4.4 Proportional controller step response

4.1.2.2 Integral (I) Controller

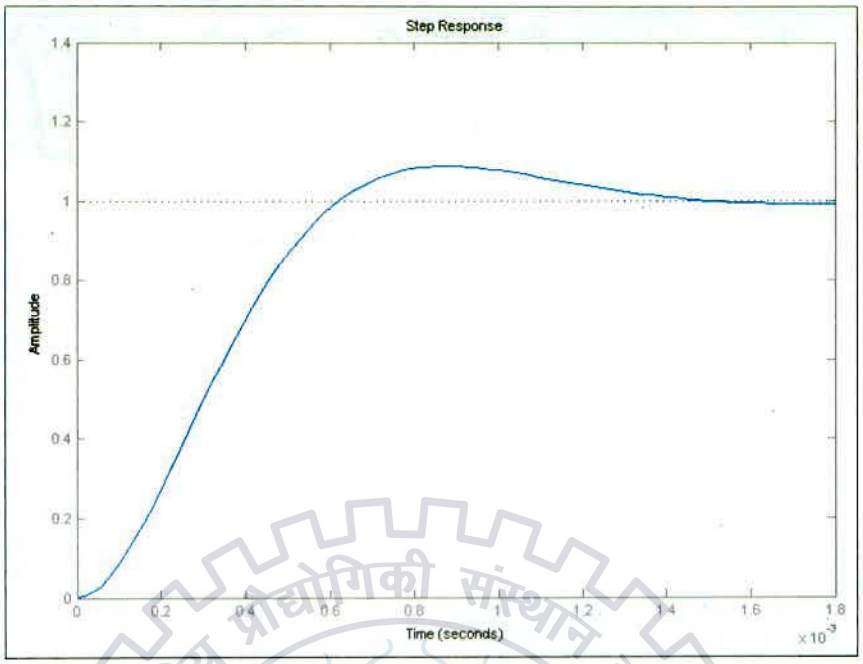


Figure 4.5 Integral controller step response

As compared to P controller Integral (I) controller reduces the steady state error which can be seen in Fig. 4.5. But Integral control gives settling time of response more than the proportional controller.

4.1.2.3 Proportional-Derivative (PD) Controller

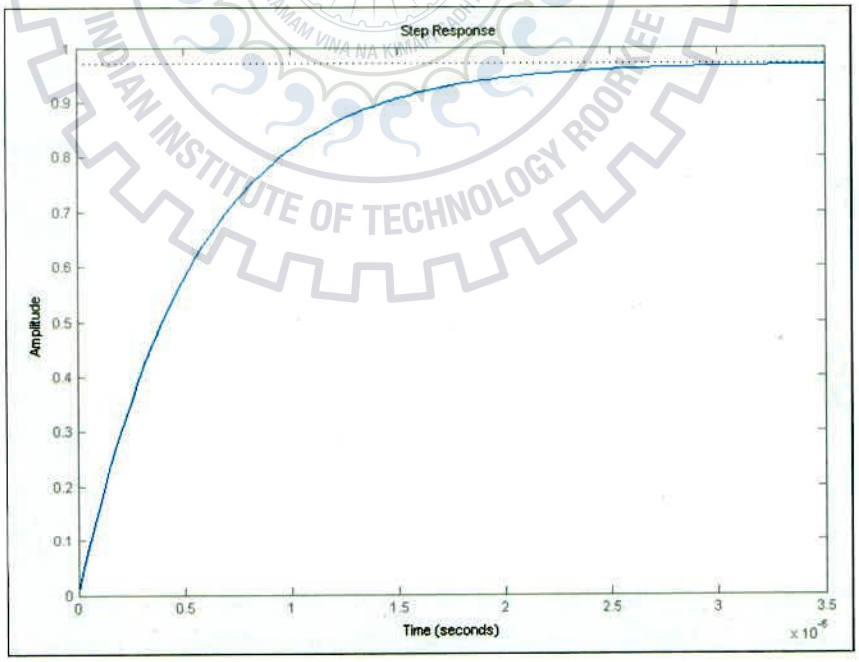
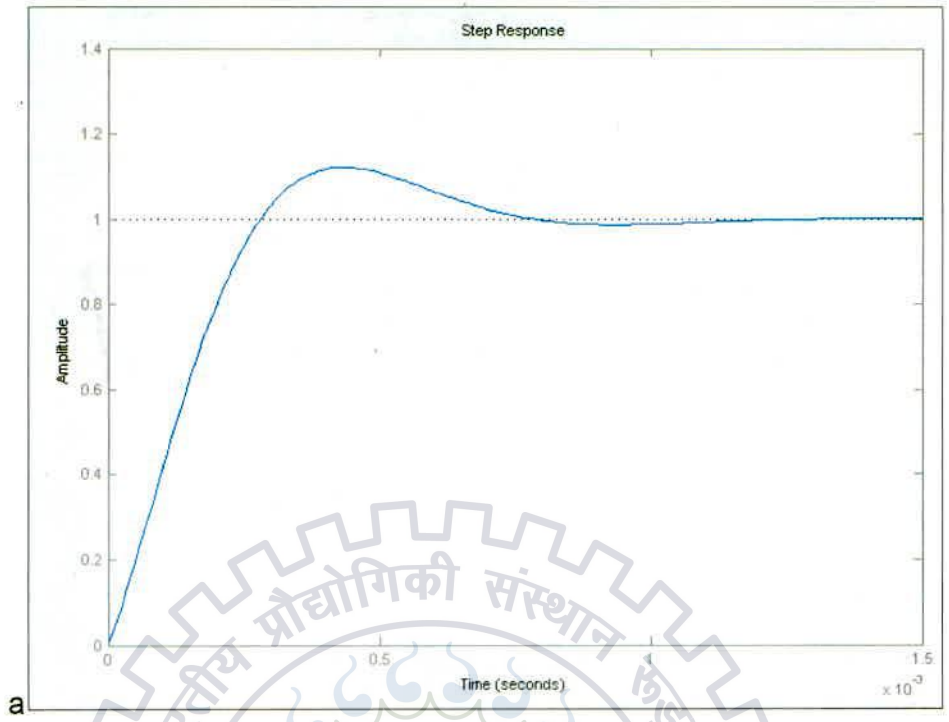


Figure 4.6 PD controller step response

4.1.2.4 PI and PID Controller



a

Figure 4.7 PI and PID controller step response

From the Fig. 4.7 it is clear that PI and PID controller response having zero steady state error with less settling time.

PI Controller transfer function:

G(s) = K* (1 + sT) / (sT)
Where,
K= Gain of the PI controller
T=Time constant T of the PI controller, in seconds.

After tuning in SISOTOOL PI controller parameters as obtained as follows,

Kp= 0.0178
T= 5.7e-05

4.2 Sliding Mode Controller

Nonlinear system model imprecision may come from actual uncertainty about the plant (e.g., unknown plant parameters), or from the purposeful choice of a simplified representation of the system's dynamics. Modeling inaccuracies can be classified into two major kinds: structured (or parametric) uncertainties and unstructured uncertainties (or unmodeled dynamics). The first kind corresponds to inaccuracies on the terms actually included in the model, while the second kind corresponds to inaccuracies on the system order. Inaccuracies in modeling can have strong adverse effects on nonlinear control systems.

One of the most important approaches to dealing with model uncertainty is robust control. The typical structure of a robust controller is composed of a nominal

part, similar to a feedback control law, and additional terms aimed at dealing with model uncertainty. Sliding mode controller design provides a systematic approach to the problem of maintaining stability and consistent performance in the face of modelling imprecision. The Sliding mode control (SMC) is a powerful and excellent robust nonlinear control method. SMC can ensure DC-DC converter to hold stability and good dynamic performance.

Basic structure of Sliding Mode Controller:

Sliding mode controller for Buck converter is shown in Fig. 4.8. Output of the converter is step down with the help of voltage divider circuit. Which compares with reference value (V_{ref}). Error (X_1) after comparison is multiplied with fixed gain parameter(K_p). Capacitor current is multiplied with gain of value minus one. Both the signals are added which further given to PWM circuit. The switching pulses required for the switches are generated by the PWM circuit.

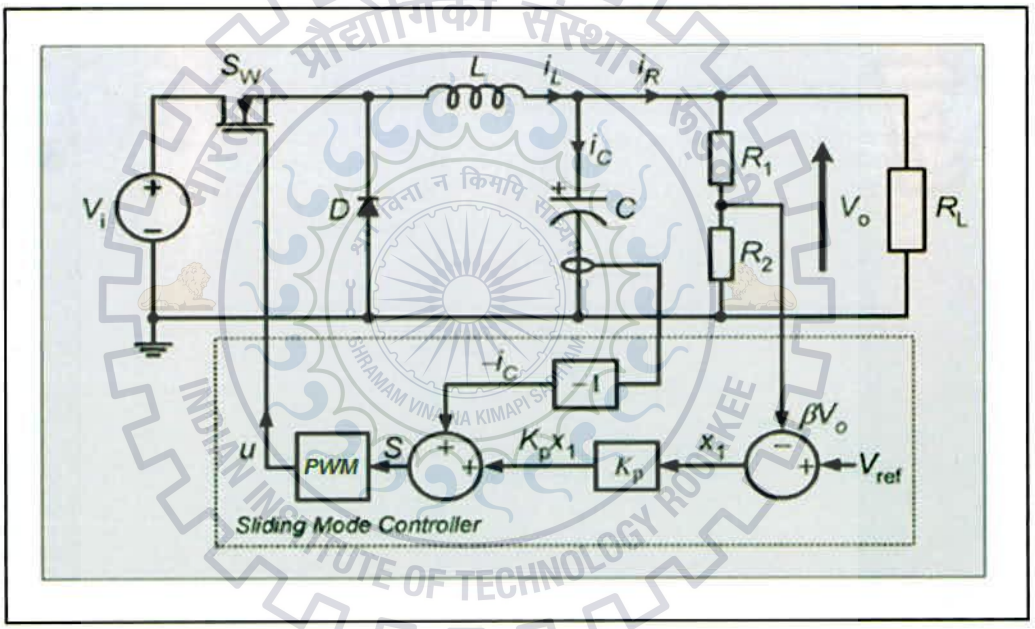


Figure 4.8 Slinding mode controller for Buck Converter

Where,

u= switching state

$\beta = \frac{R2}{R1+R2}$

V_o = Output voltage

V_{ref} = Reference voltage

$K_p = 1/\beta R_L$ = fix gain parameter

$S = K_p(V_{ref} - \beta V_o) - i_c$ = sliding mode controller equation

Converter specifications:

Parameters	Values
Input voltage (V_s)	100 V
Number of primary turns of transformer (N_p)	10
Number of secondary turns of transformer (N_s)	6
Inductance (L)	24μH
Capacitance (C)	7.81μF
Load resistance (R)	1.6Ω
Diode parasitic resistance (r_{d1}, r_{d2})	0.01Ω
Inductor parasitic resistance (r_L)	0.05Ω
Capacitor parasitic resistance (r_C)	0.08Ω
Fix gain parameter (K_p)	0.625
Gain multiplier (K)	-1

5.1 PI controller for Push-Pull Converter

Figure 5.1 shows the simulation circuit of Push-Pull converter with PI controller. Parasitic resistance of diodes, inductor, capacitor is considered for the simulation. In which the output voltage is sensed through voltage sensor which further compares with the reference voltage(V_{ref}). PI controller receives the error generated from the comparison. Sawtooth wave generated from pulse generator and control signal are compared by comparator. Switching pulse generated after comparison is given to switch one (S_{w1}), which is further delayed by 180° for switch two (S_{w2}) by delay circuit.

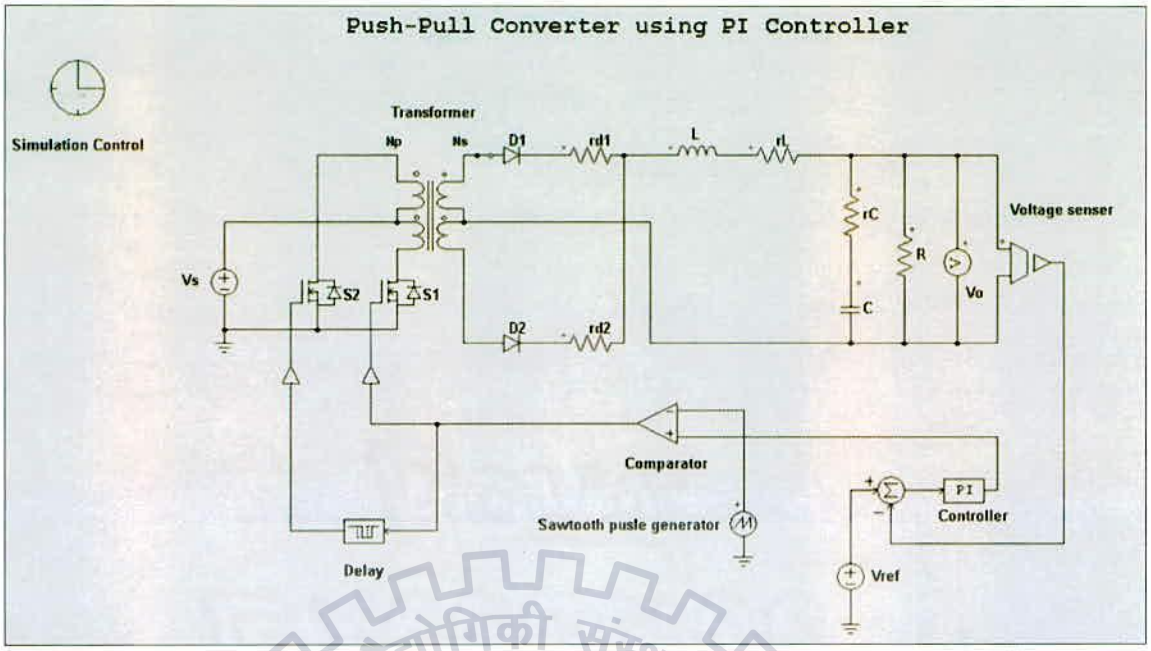


Figure 5.1 Simulation circuit of PI controller for Push-Pull Converter

Result:

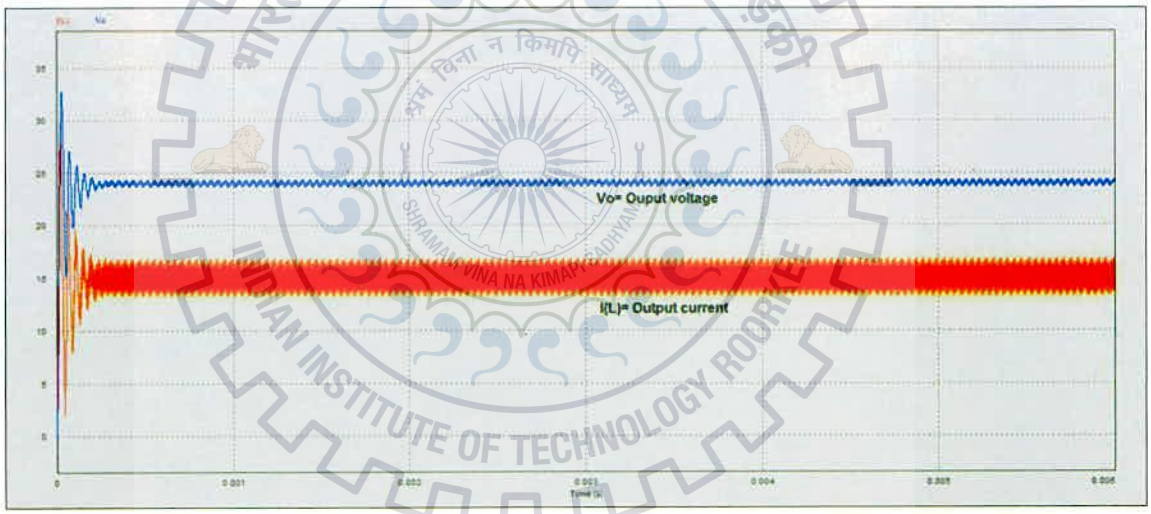


Figure 5.2 Response of PI controller for Push-Pull Converter

5.2 Sliding Mode Controller of Push-Pull Converter

Simulation for sliding mode control of Push-Pull converter is shown in Fig. 5.3. Output voltage (V_o) of the converter is sensed by voltage sensor which compares with the reference value (V_{ref}). The error after comparison is multiplied with the fix gain parameter (K_p). This further added with the capacitor current which multiplied with the gain (K). The controller signal is given to PWM control block. Pulses required for the switches are generated by PWM control block.

Behaviour of sliding mode controller is verified under line variation as shown in Fig. 5.4. At 100 V input the output voltage is equal to 24 V and inductor current is 15 A. At 2 ms input voltage is reduced from 100 V to 90 V and at 4 ms input voltage

increased from 90 V to 110 V. Even though there is disturbance in input voltage just within short interval of time output voltage settle downs its desired value.

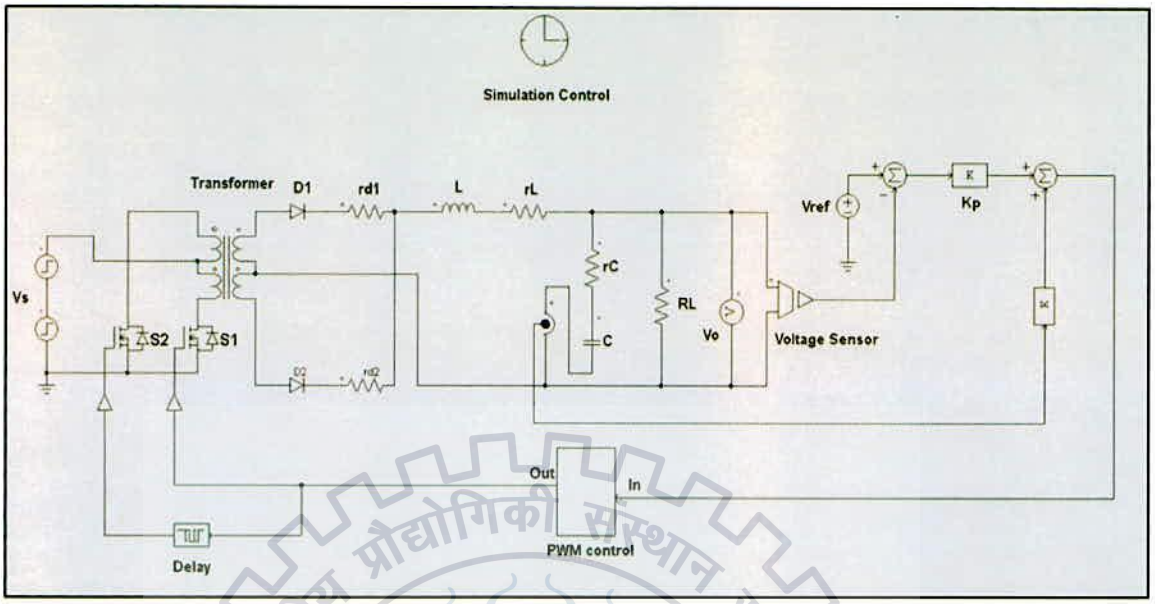


Figure 5.3 Simulation circuit of sliding Mode Controller of Push-Pull Converter

Result:

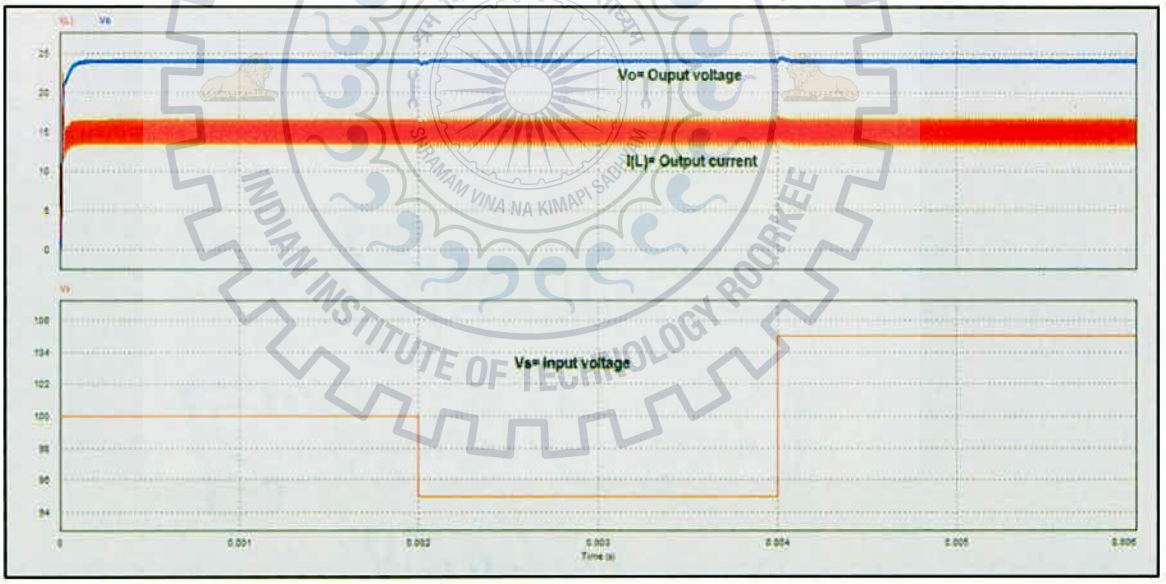


Figure 5.4 Response of sliding Mode Controller of Push-Pull Converter

5.3 Comparison of sliding mode controller with PI controller

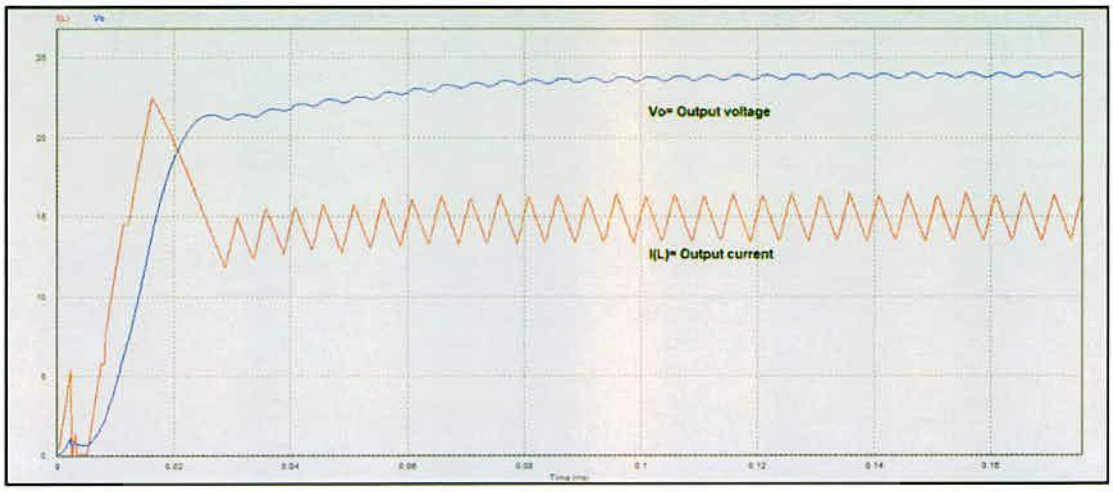


Figure 5.5 Sliding mode controller response

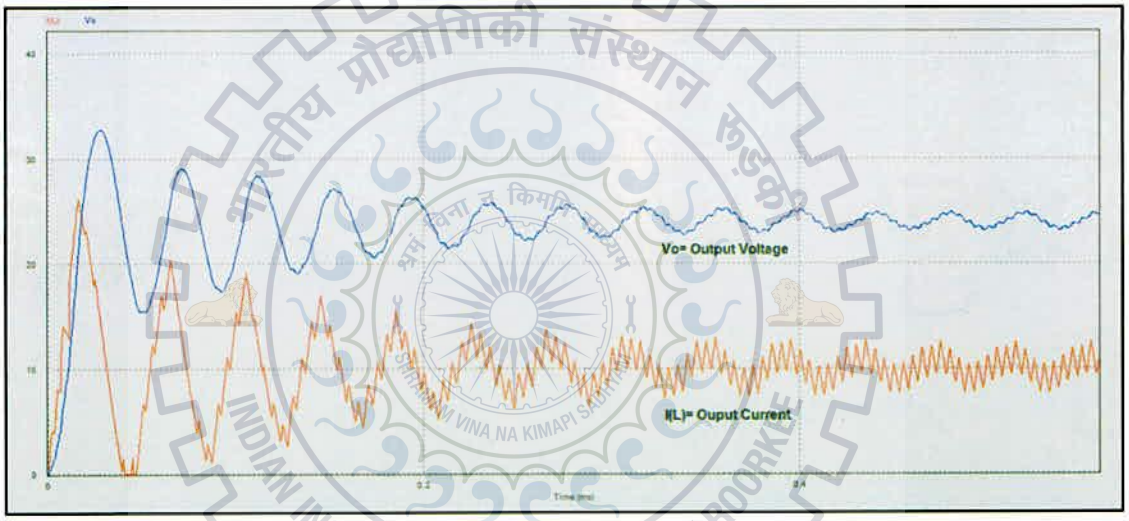


Figure 5.6 PI Controller response

From Fig. 5.5 and Fig. 5.6 it is seen that as compared to PI controller, sliding mode controller reduces overshoot in output voltage and also reduces the settling time. The settling time with sliding mode controller is just 0.1ms where as the settling time with PI controller is 0.4ms.

5.4 FPGA based Push-Pull Converter (Open loop)

Simulation of FPGA based Push-Pull in open loop configuration is show in Fig. 5.7. Power circuit of converter is simulated in PSIM. Pulse generation circuit is simulated in MATLAB with XILINX tool box shown in Fig. 5.8. With the help of SimCoupler Module in MATLAB the co-simulation of PSIM and MATLAB is obtained. IN_1 and IN_2 are input signals from the pulse generation circuit.

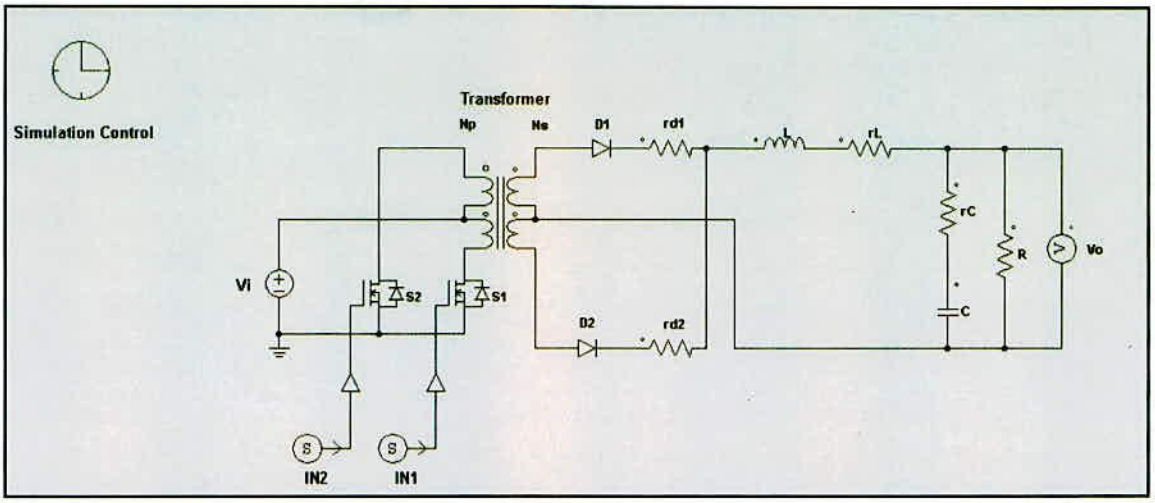


Figure 5.7 Power circuit in PSIM

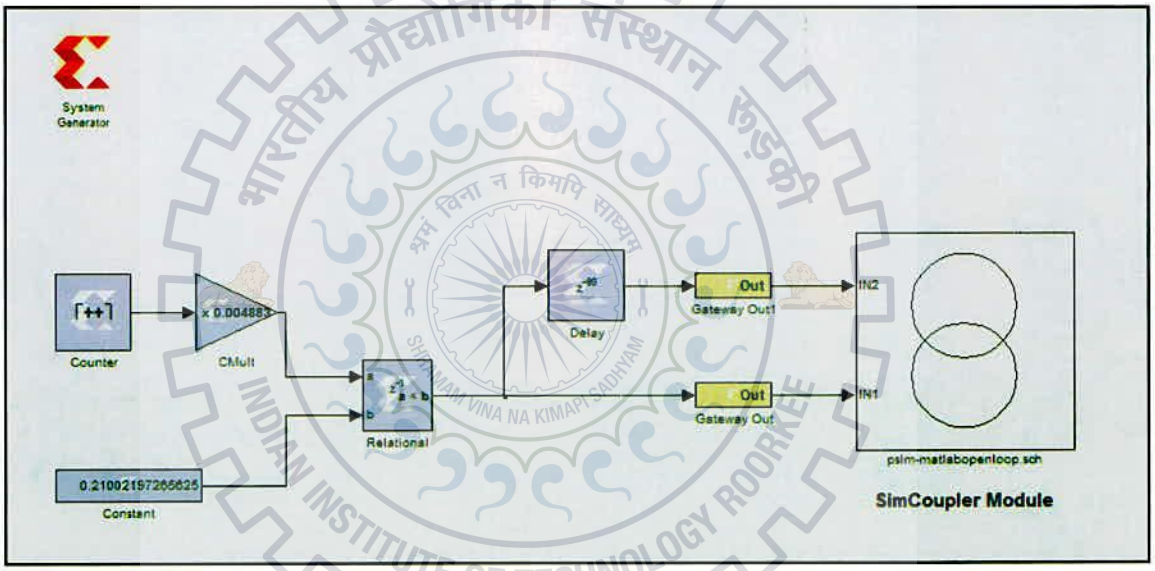


Figure 5.8 Pulse generation circuit in MATLAB

Results:

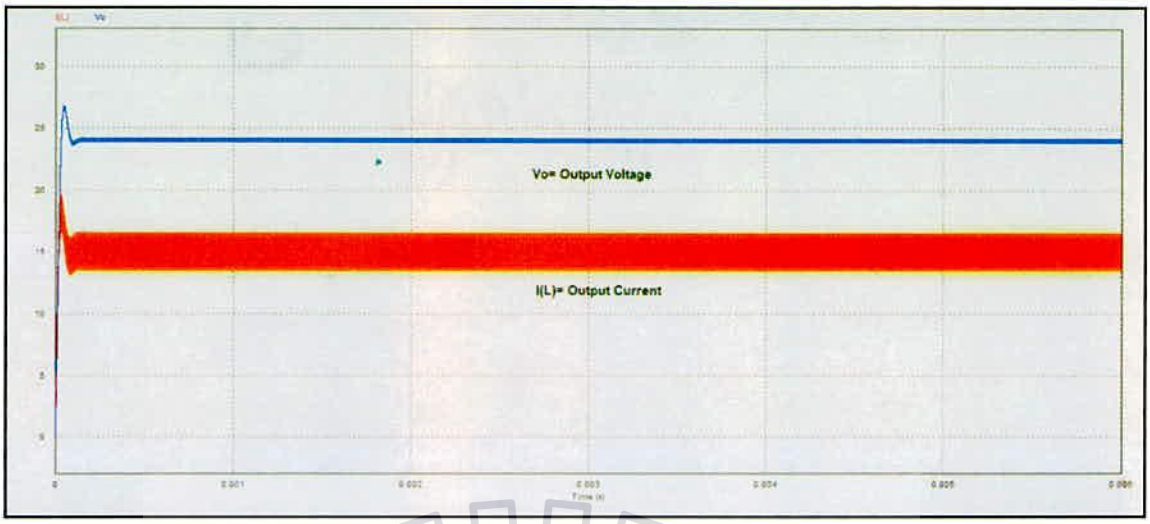


Figure 5.9 Response of FPGA based Push-Pull Converter in open loop

5.5 FPGA based sliding mode controller for Push-Pull Converter

Simulation of FPGA based sliding mode controller for Push-Pull Converter is show in Fig and Fig. 5.10. Power circuit of converter is shown in Fig and controller circuit is shown in Fig. 5.11. Output voltage is sensed by voltage sensor and capacitor current is sensed by current sensor. Pulses generated by PWM control circuit is fed back to switches. Simulation results are shown in Fig which gives the output voltage (V_o) equal to 24 V and inductor current (I_L) equal to 15 A.

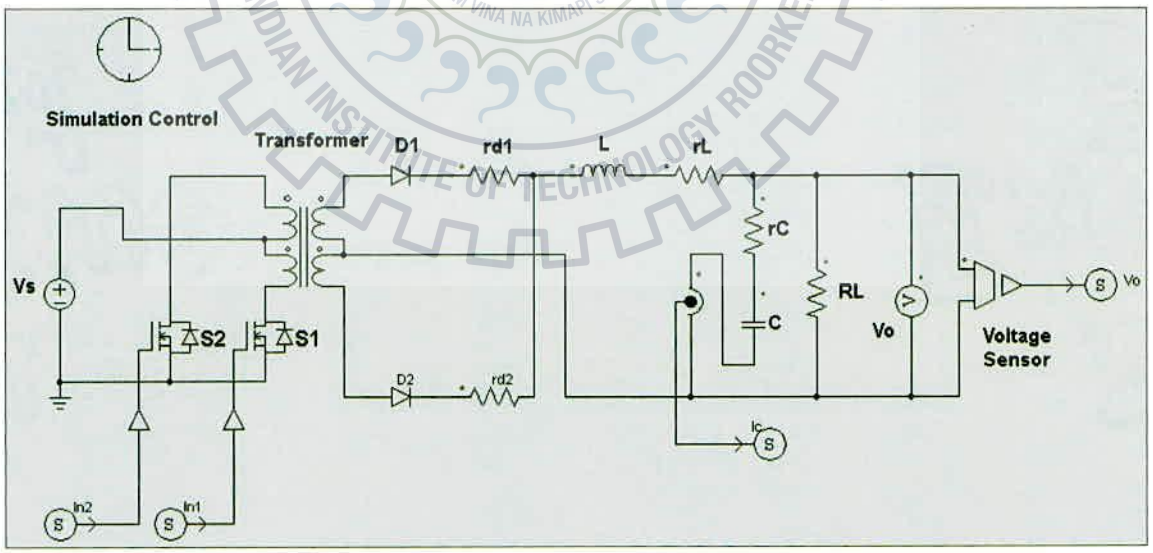


Figure 5.10 Power circuit of converter in PSIM

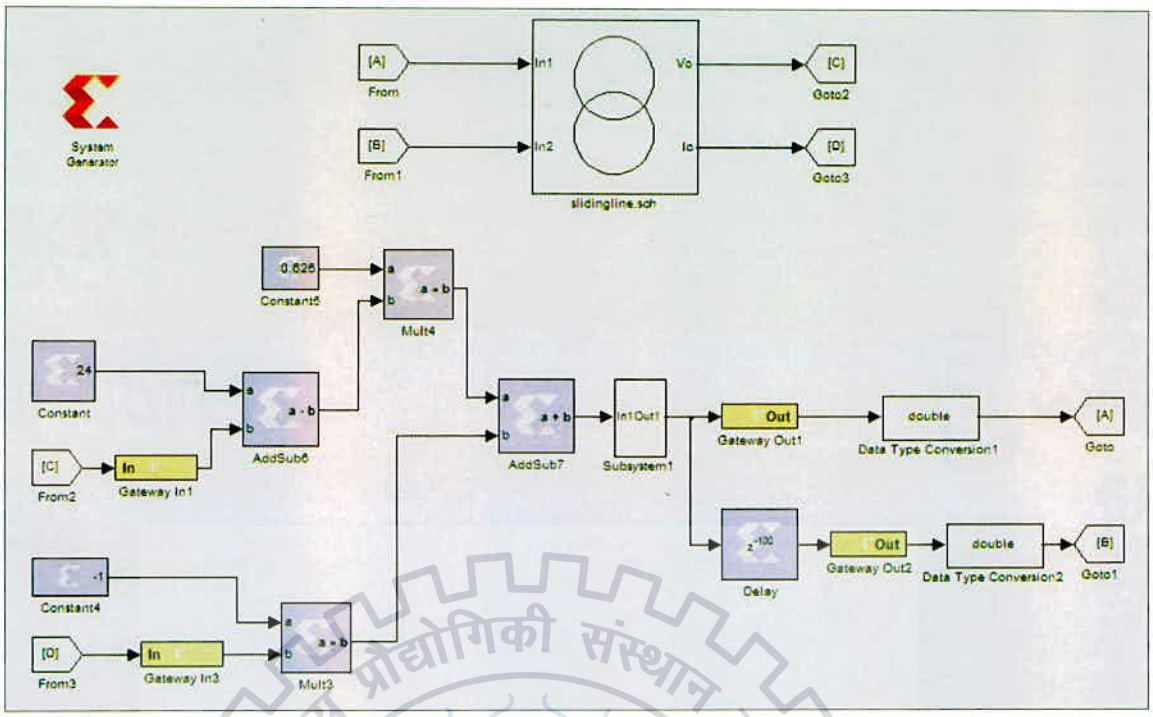


Figure 5.11 Controller circuit in MATLAB with XILINX tool box

Result:

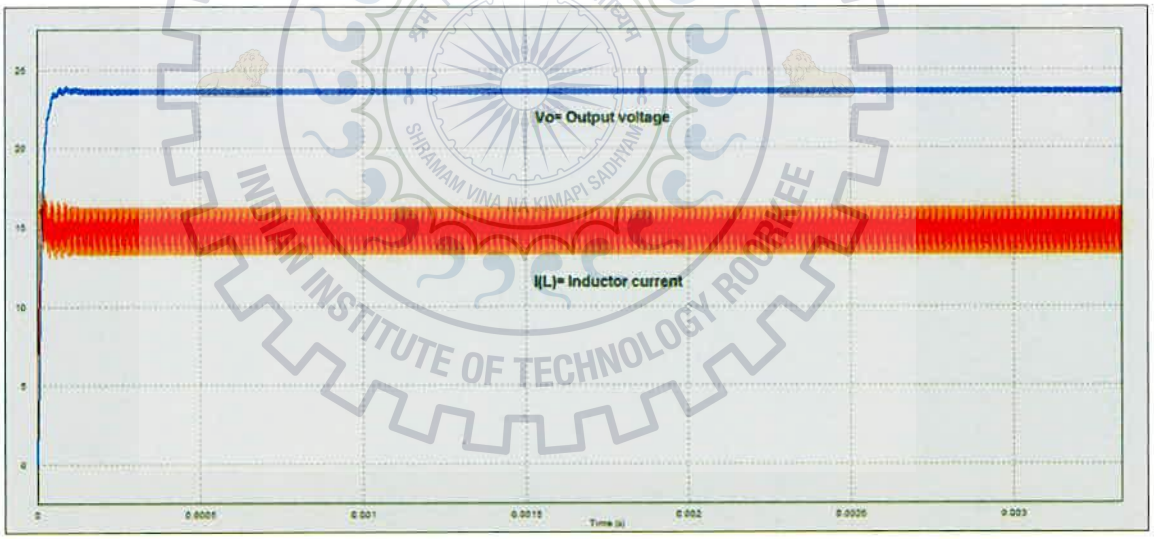


Figure 5.12 Output voltage and output current of converter

With load variation:

Performance behaviour of FPGA based sliding mode controller is verified for load variation as shown in Fig. 5.13. As load resistance reduces or increases the inductor current increases or decreases where as the output voltage of converter remains its desired value.

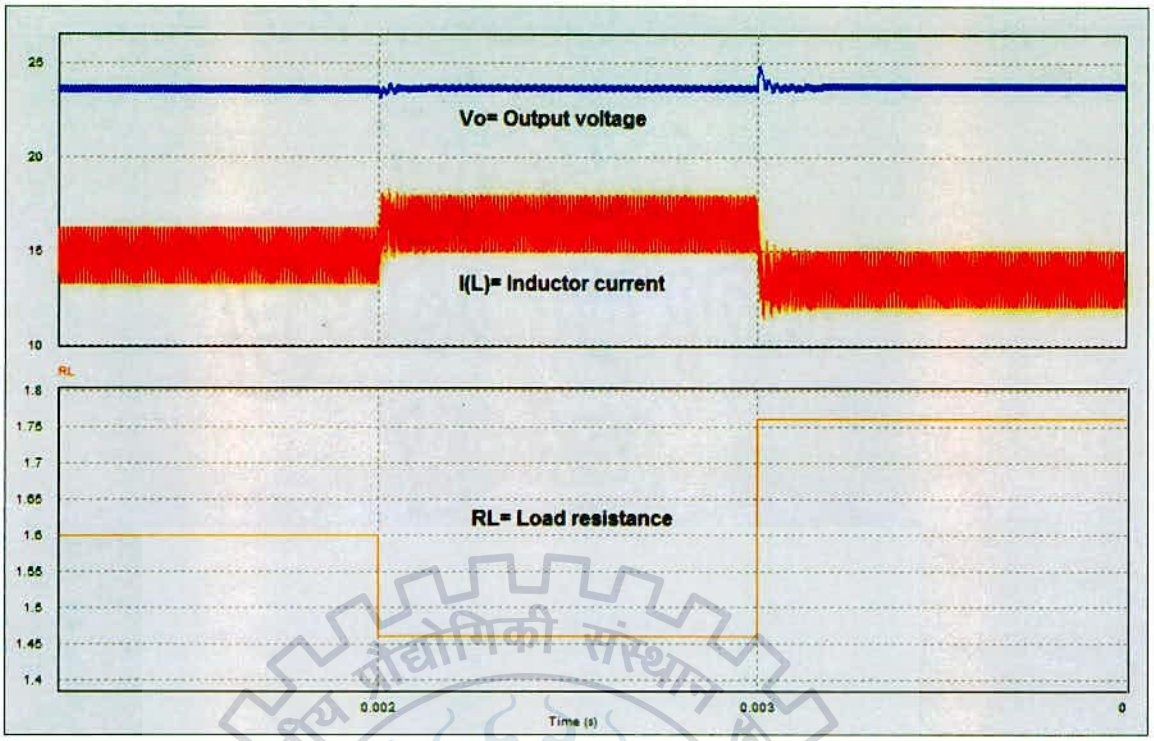


Figure 5.13 Response of controller with load variation

Prototype model of Push-Pull converter is implemented using power circuit, MOSFET driver circuit, FPGA kit. Switching frequency and input dc voltage level are scale down from 100 kHz to 10 kHz and 100 V to V respectively.

Parameters:

Input voltage: 45 V
Switching frequency: 10 kHz
Load resistance: 8Ω
Output voltage: 10 V

6.1 Pulse generation using FPGA SPARTAN 3-kit

6.1.1 Steps for pulse generation

- ✓ MATLAB simulation: Pulse generation circuit is simulated in MATLAB with XILINX tool box.
- ✓ Code generation using SysGen: Using System generator (SysGen) codes are generated.
- ✓ Program files using Xilinx design suit: Once codes are generated, using Xilinx design suit program files are generated.
- ✓ Pin configuration using floor plan ahead: Using floor plan ahead the pin configuration is decided.
- ✓ Generation of bits: Once pin configuration is done bits required for FPGA kit are generated.
- ✓ Download bits into FPGA using Impact: Using IMPACT tool generated bits are dumped into FPGA kit.

6.2 Simulation result and FPGA kit output

Figure 6.1 shows the simulation results and Fig. 6.2 shows that the output obtain from FPGA kit is similar to the output obtain from the simulation. Frequency of the pulses is 100 kHz with 180° phase shift.

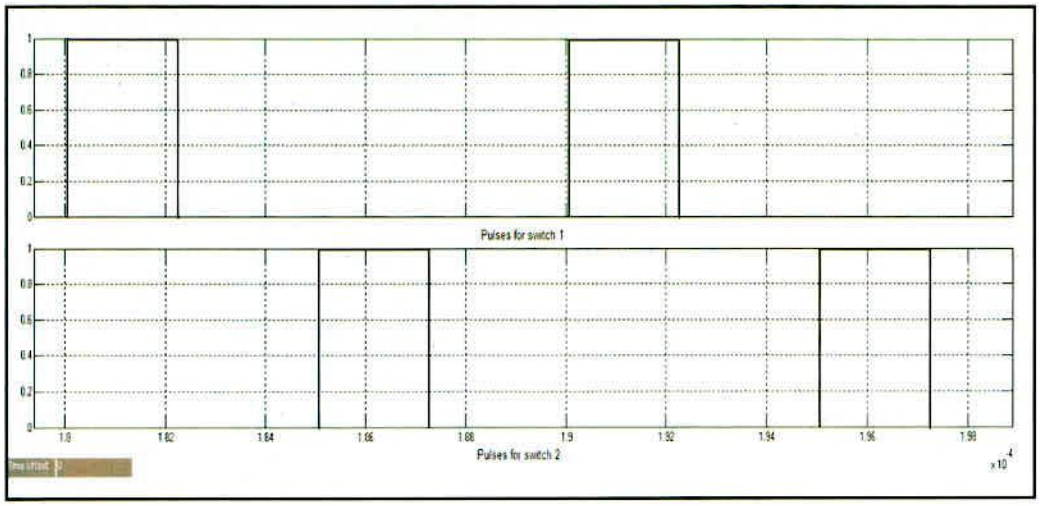


Figure 6.1 Simulation result

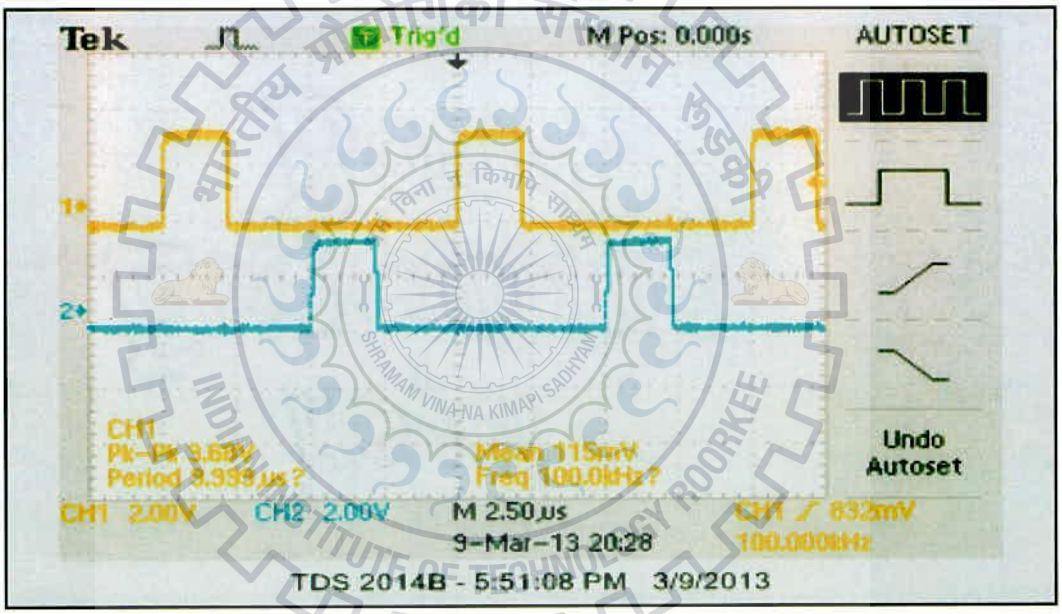


Figure 6.2 FPGA kit output

6.3 Driver circuit for MOSFET

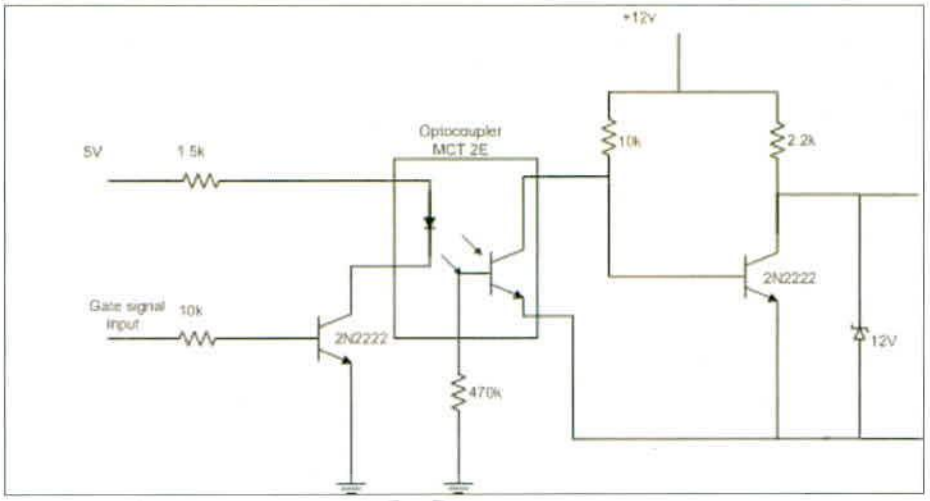


Figure 6.3 MOSFET driver circuit

MOSFET driver circuit is shown in Fig. 6.3. This requires on 5 V and 12 V power supply for working. Opto-coupler is used for the isolation of low voltage circuit with high voltage power circuit. When input gate signal is high first transistor gets turned on. Due to which LED starts conducting. Light energy falls into the base of the phototransistor. Because of which second transistor remains in off position and hence 12 V appears at the output of the circuit. 12 V zener diode is connected at the output of the circuit which maintains the ouput voltage to 12 V. Similarly when the gate input signal is low both transistor number one and phototransistor remains in off position. Which makes transistor number two on. And hence output of the circuit remains in low state.

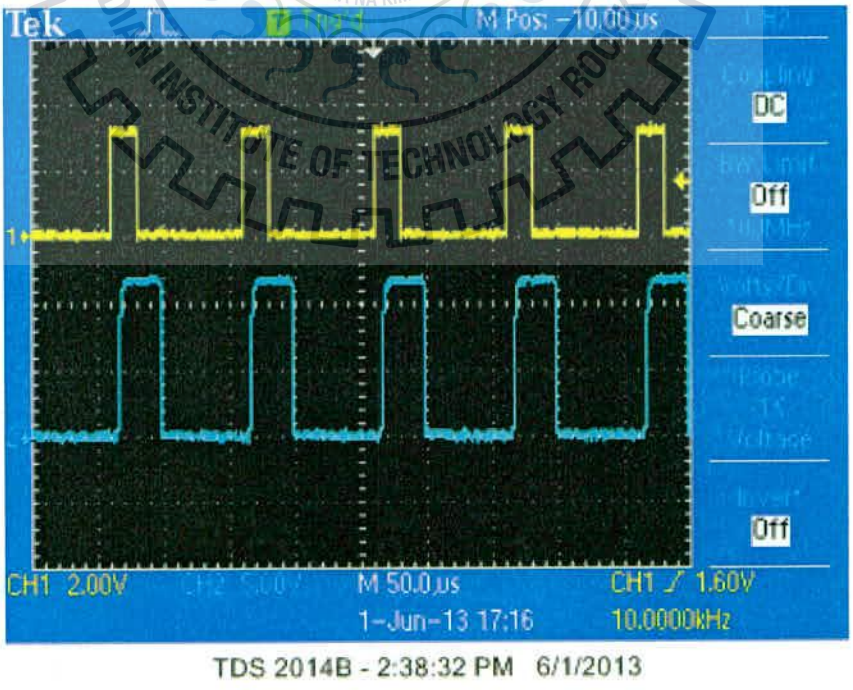


Figure 6.4 Output of driver circuit for switch 1

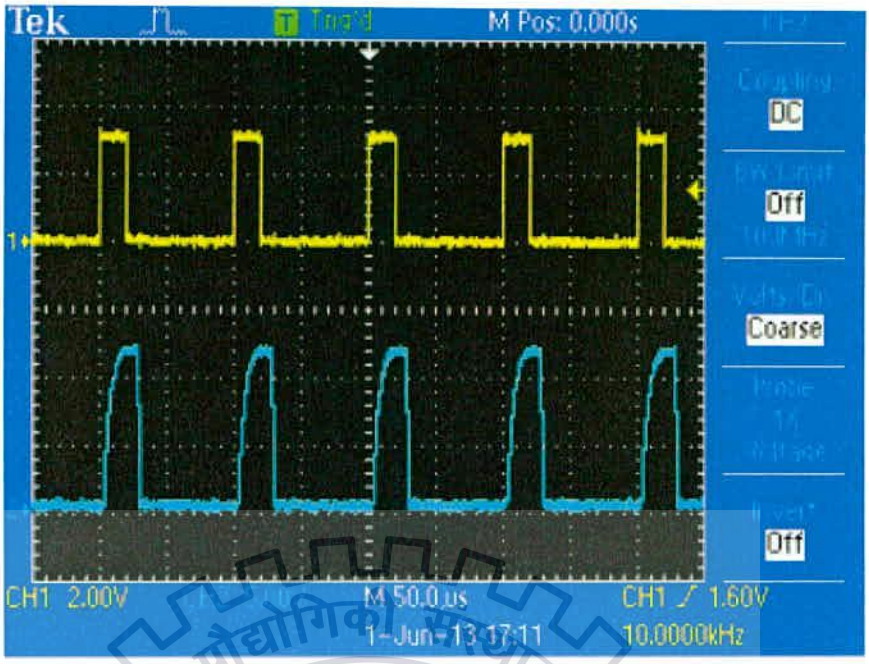


Figure 6.5 Output of driver circuit for switch 2

Figure 6.1 and Fig 6.2 shows the output of the driver circuits for MOSFET. Input the driver circuit is from the FPGA kit. The voltage levels of pulses obtained from FPGA kit are incapable to drive MOSFET. Hence in order to raise the voltage level driver circuits are used. Input to driver circuit is just of 3.5 V but the output of driver circuit is increased to around 12 V which is sufficient to drive switches.

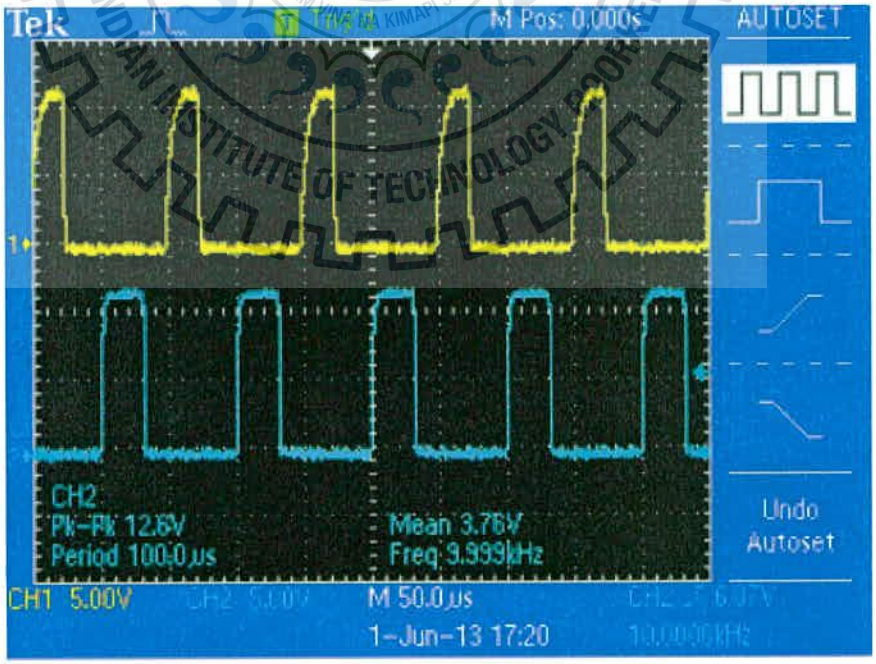


Figure 6.6 Switching pulses from driver circuits

6.4 Experimental setup

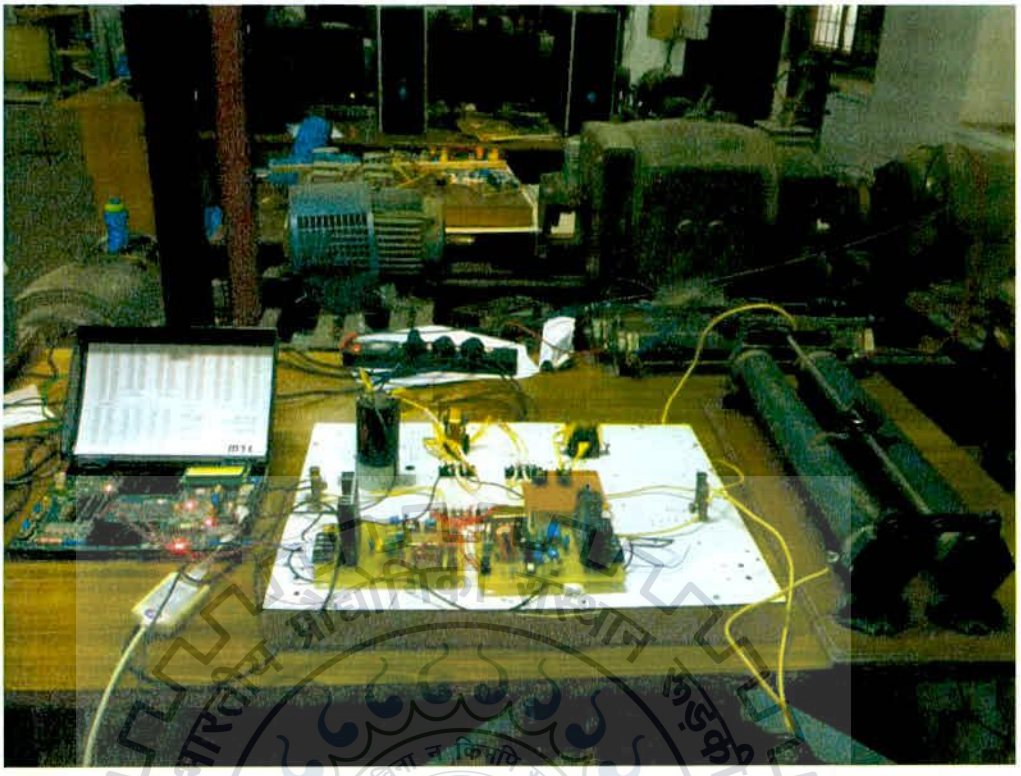


Figure 6.7 Experimental setup of Push-Pull converter

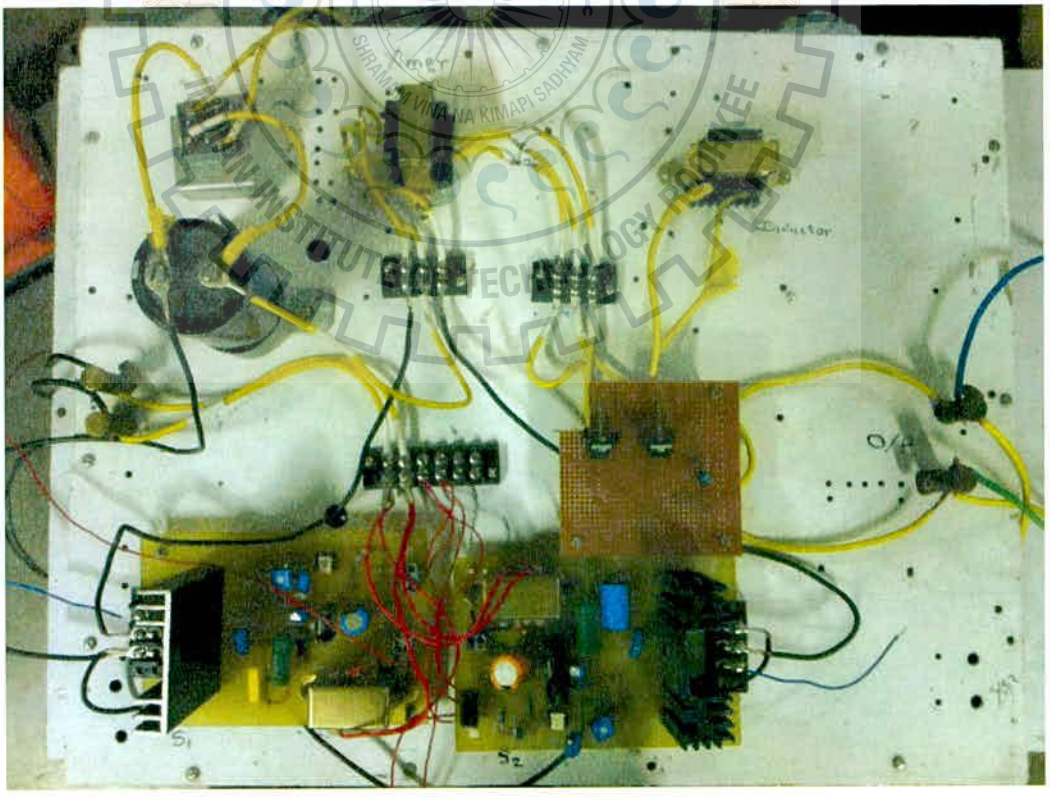


Figure 6.8 Close view of converter circuit

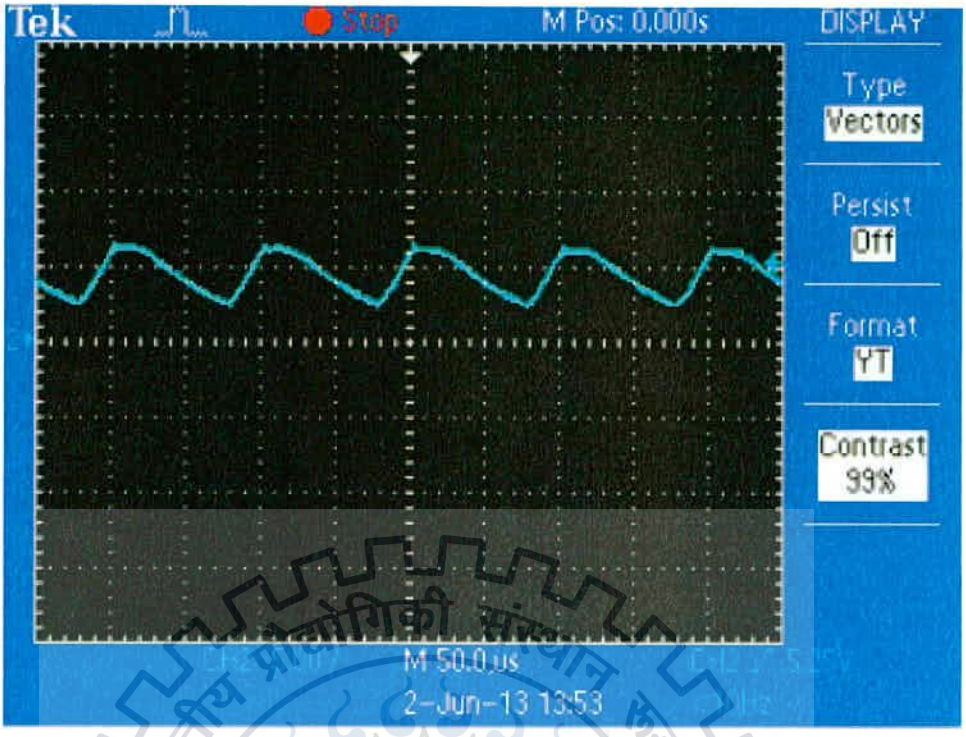


Figure 6.9 Converter output voltage

Figure 6.7 shows the complete experimental setup of Push-Pull converter and Fig. 6.8 shows the close view of the converter circuit. Input to the MOSFET driver circuit is from FPGA kit is given. This increases the voltage level that is required for turning on for MOSFET. DC input voltage for converter working is obtained from the bridge rectifier. Using auto-transformer variable ac input is applied to the bridge rectifier. Output of the bridge rectifier dc link capacitor is connected to reduce the ripple in dc voltage. Fig. 6.9 shows the output obtained from the experiment recorded on DSO. Output voltage is nearly equal to 10 V with ripple content in it.

Using state space averaging method is transfer function of the Push-Pull converter is obtained. With the help of SISOTOOL in MATLAB the tuning of PI controller is achieved using converter transfer function. Step responses of the converter with and without controllers are studied from which PI controller is selected since it gives better settling time with less overshoot. Transformer as well as Push-Pull converter for particular specifications is designed.

The steady state performance of PI controller Push-Pull converter as well as for sliding mode controller for Push-Pull converter is investigated using PSIM software. A comparison sliding mode controller and PI controller for Push-Pull converter is highlighted. Simulation result shows that basic PI controller has maximum settling time as well as maximum overshoot compared to sliding mode controller. Hence using sliding mode controller stability of converter can be improved. FPGA based Push-Pull converter in open loop and using sliding mode controller is also simulated using PSIM, MATLAB and Xilinx tool box.

Prototype model of Push-Pull converter is experimentally tested for scaled down version in open loop configuration. Switching pulses for switches are generated using FPGA kit. Voltage level of pulses increases using MOSFET driver circuit.

FUTURE SCOPE OF WORK:

The prototype model of Push-Pull converter using sliding mode controller has to be developed using switching frequency of 100 kHz.

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[15] Xilinx SPARTAN 3 kit user manual, www.xilinx.com

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LIST OF PUBLICATIONS

International conferences

[1] **K.S.Narad, K.P.Guruswamy, S.P.Singh,** "FPGA-Based PID Controller for Push-Pull Converter" International Conference on Electrical Engineering & Computer Science, EECS-2013/ISBN:978-93-82208-79-2, Nagpur, 19th May 2013, pp 38-42.

[2] **K.S.Narad, K.P.Guruswamy, S.P.Singh,** "Design and Modeling of a Voltage fed Push-Pull DC/DC Converter", International Conference on Electrical, Electronics and Computer Science Engineering, EECS-2013/ISBN:978-93-82208-94-5, New Delhi, 26th May 2013, pp 24-28.

National conferences

[3] **K.S.Narad, S.P.Singh,** "PID Controller for Multiple-Output Push-Pull DC/DC Converter", Proceedings of the National Conference on Electrical Systems and Renewable Energy (NESR), Tiruchirappalli, 3rd May 2013, pp 11-15.

RM Ferrite Cores
Manufacturer **Magnetics** Inc.

Part No.	MPL Cm	G cm	'tfe grams	'tcu grams	MLT cm	A_c cm^2	W_a cm^2	A_p cm^4	% cm^5	A_t cm^2	Penn	'L
RM-41110	2.06	0.700	1.60	1.02	2.02	0.108	0.142	0.0153	0.000327	5.88	2500	750
RM-4151O	2.14	0.630	3.00	1.50	2.53	0.210	0.167	0.0351	0.001160	8.01	2500	1409
RM-41812	2.17	0.798	5.40	2.65	3.11	0.380	0.239	0.0910	0.004440	11.40	2500	1950
KM-42316	3.80	1.074	13.00	6.73	4.17	0.640	0.454	0.2900	0.017820	20.20	2500	2200
KM-42819	4.40	1.240	23.00	11.81	5.20	0.980	0.639	0.6258	0.047180	29.60	2500	3300
RM-43723	5.69	1.680	42.00	22.21	6.10	1.400	1.025	1.4347	0.131820	44.50	2500	3750

Wire Table

AWG	Bare Wire Area		$\mu\Omega$ / cm	Heavy Insulation		
	cm^2	CIR-MIL		cm^2	Turns/cm	Turns/cm
10	0.05260	10384SX)	32.70	0.05590	3.87	10.73
11	0.04168	8226.00	41.37	0.04450	4.36	13.48
12	0.03308	6529.00	52.09	0.03564	4.85	16.81
13	0.02626	5184.00	65.64	0.02836	5.47	21.15
14	0.02082	4109.00	82.80	0.02295	6.04	26.14
15	0.01615	3260.00	104.3	0.01837	6.77	32.66
16	0s)1307	2581.00	131.8	0.01473	7.32	40.73
17	0.01039	2052.00	165.8	0.01168	8.18	51.36
18	0.008228	1624.00	209.5	0.009326	9.13	64.33
19	0.006531	1289.00	263.9	0.007539	10.19	79.85
20	0.005188	1024.00	332.3	0.006065	11.37	98.93
21	0.004116	812.30	418.9	0.024837	12.75	124.0
22	0.003243	640.10	531.4	0.003857	14.25	155.5
23	0.002588	510.80	666.0	0.003135	15.82	191.3
24	0.002047	404.00	842.1	0.002514	17.63	238.6
25	0.001623	320.40	1062.0	0.002002	19.8	299.7
26	0.001280	252.80	1345.9	0.001603	22.12	374.2
27	0.001021	201.60	1687.6	0.001313	24.44	456.9
28	0.0008048	158.80	2142.7	0.0310515	27.32	570.6
29	0.0006470	127.70	2664.3	0.0008548	30.27	701.9
30	0.0005067	100.0	3402.2	0.0006785	33.93	884.4
31	0.0004013	79.21	4294.6	0.0005596	37.48	1072
32	0.0003242	64.00	5314.9	0.0004559	41.45	1316
33	0.0002554	50.41	6748.6	0.0003662	46.33	1638
34	0.0002011	39.69	8572.8	0.0302863	52.48	2095
35	0.0001589	31.36	10849	0.0002268	58.77	2645
36	0.0001266	25.00	13608	0.0001813	65.62	3309
37	0.00010.26	20.25	16801	0.0001538	71.57	3901
38	0.00008107	16.00	21266	0.0001207	80.35	4971
39	0.00006207	12.25	27775	0.0000932	91.57	6437
40	0.00004869	9.61	35400	0.0000723	103.6	8298
41	0.00003972	7.84	43405	0.0000584	115.7	10273
42	0.00003166	6.25	54429	0.0300456	131.2	13163
43	0.00002452	4.84	70308	0.0000368	145.8	16291
44	0.00002020	4.00	85072	0.0000317	157.4	18957