IMPACT OF MECHANICAL STRESS ON MOBILITY & DEVICE CURRENT OF PLANAR MOSFET

A DISSERTATION

Submitted in Partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ELECTRONICS & COMMUNICATION ENGINEERING

(With Specialization in Microelectronics and VLSI)

By

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CANDIDATE'S DECLARATION

I hereby declare that the work, which is being reported in this dissertation entitled, "**Impact of Mechanical Stress on Mobility & Device Current of Planar MOSFET** ", which is being submitted in the partial fulfilment of the requirements for the award of degree **Master of Technology** in **Microelectronics & VLSI**, submitted in the Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee (India), is an authentic record of my own work carried out from June 2012 to May 2013 under the guidance and supervision of **Dr. Anand Bulusu**, Assistant Professor and **Dr. Sudeb Dasgupta**, Associate Professor, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter embodied in the dissertation report to the best of my knowledge has not been submitted for the award of any other degree elsewhere.

Dated: 27-06-2013

Place: Roorkee

(Jayakrushna Mohapatra)

CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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Dedicated to my parents and loving brothers for their unconditional love and support.

ABSTRACT

Strain engineering is used to enhance device performance commensurately with the physical scaling in contemporary technology. Therefore, strain engineering is an integral part of a state-of-the-art CMOS technology flow. Strain engineering is used to introduce favourable mechanical stress in the channel to enhance CMOS performance. In the era of nano-technology devices are working in the near ballistic regime. In this regime of operation performance of device depends on the injection velocity (V_{inj}) and backscattering ratio (r), so here we analyze how these parameters depends on stress. It is observed that uniaxial tensile stress reduces the backscattering ratio due to modulation in KT-layer thickness and carrier mean free path for backscattering. Tensile stress also splits the valley degeneracy, which change the probability of occupancy of carrier in different valley. It also improve injection velocity near the virtual source end by reducing the carrier effective mass. Impact of drive current under uniaxial strain is analyzed in term of mean-free-path, KT-layer thickness, ballistic efficiency and injection velocity.

CONTENTS

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List of Abbreviations and Acronyms

CMOS	Complementary MOS
DIBL	Drain-induced barrier lowering
nMOS	n-type MOS
pMOS	p-type MOS
SGOI	Sige on Insulator
SMT	Stress Memorization Technique
SOI	Si on Insulator
SDOI	Strained Si Directly on Insulator
SSGOI	Strained Si on SiGe on Insulator
SSOS	Strained Si on Si
TCAD	Technology Computer-Aided Design
VLSI	Very Large Scale Integration
SCE	Short-Channel Effect
CESL	Contact Etch Stop Liner
SEG	Selective Epitaxial Growth
DCS	Device Co-ordinate System
CCS	Crystal Co-ordinate System
HH	Heavy Hole
LH	Light Hole
S/D	Source and Drain
BSR	Back Scattering Ratio
MFP	Mean Free Path
OPE	Optical Phonon Emission
BJT	Bipolar Junction Transistor

Chapter-1

Introduction

1.1 Motivation

For the past four decades, down scaling of MOSFETs has resulted into new technology generations every two to three years with doubled logic device density, lowered cost per logic function, and increased chip performance. However, as device dimension enters into the deep sub micrometer regime, many physical phenomena such as short-channel effect (SCE), velocity saturation, high leakage current, and dielectric breakdown limit the benefits of conventional scaling [1,18] . For improving device performance continuously, new device structures, new materials, and strain engineering have been proposed and investigated also. Out of all these new technologies, strain engineering during the past decade has been the dominant one. This technique is a low-cost and low-risk technique by maintaining the traditional metal oxide- semiconductor field-effect transistor (MOSFET) fabrication process. It has been observed by experimentally and theoretically that strain has ability to enhancement of drive current by ~4.5× in Si pMOSFETs and ~2× in nMOSFETs without a significant increase in leakage current [2,17] . With the fourth generation of strained-Si technology now in commercial production, strain-enhanced performance and power saving are present in nearly all VLSI logic chips manufactured today.

There are broadly two types of strain/ stress that is used to enhance the MOSFET performance: (a) Biaxial stress and (b) Uniaxial stress. These two type of stress can enhance the mobility and hence current of the short channel device. Even though the predominant focus of the industry in the 1980s and 1990s was on biaxially stressed devices, the current focus has shifted to uniaxial stress. Uniaxial strain has more benefits than biaxial strain, such as larger mobility enhancements, smaller shift in threshold voltage, integration process is somewhat less complicated. In this dissertation work we give more emphasis to uniaxial stress.

From 90nm technology onwards strain engineering has been consider as the most promising technique for enhancement of nano-scale MOSFET performances. As technology goes beyond 45nm regime transport of the carrier goes to near ballistic or quasi-ballistic region [1,2]. In this regime of operation device performance depends on the injection velocity (V_{inj}), ballistic efficiency (B_{sat}) and backscattering ratio (r) [1]. Stress enhances the effective carrier mobility, but that will not help fully to analyzing the performances enhancement in quasi-ballistic region. So we carried out device simulation here by using sentaurus TCAD for analyzing the effect of stress on above three parameters. The models what we use for simulation are pseudo potential and piezoresistive model. Pseudo potential model is use for calculation of band shifting in EK-space and piezo model use for mobility enhancement calculation.

1.2 Assumption

These are few assumptions we consider throughout the discussion

[1] Stress has very less effect on the threshold voltage, so for this timing we are assuming no variation of threshold voltage with stress.

[2] Device and crystal co-ordinate systems are align with each other.

[3] There is no shear strain component in strain tensor matrix.

[4] Only elastic scattering are there near virtual source.

1.3 Problem Statement

These are the problem statement for this dissertation work

[1] Effect of uniaxial stress on carrier backscattering.

[2] Injection velocity modulation with uniaxial stress.

[3] Effect of stress on carrier mobility.

[4] Carrier mean free path modulation with stress.

1.4 Dissertation Organization

The dissertation is organized as follows

Chapter2 describes the different techniques of introducing stress into the channel of the MOSFET. We discussed here process-induced stress and substrate induced stress.

Chapter3 describe the theory of elasticity. Stress strain relationships. Change of co-ordinate system between device and crystal. Effect of stress on conduction and valence band structure of Si crystal structure. Modulation of carrier concentration in different valleys of conduction band because of stress. Effect of stress on conductivity effective mass and carrier mobility.

Chapter4 describes the effects of stress on device current. In addition to this, we describe how stress affects to different carrier transport mode.

Chapter 5 dedicated to simulation result. The effects of stress on carrier backscattering, mean free path for backscattering and injection velocity are analysing over here.

Chapter-2

Strained Si Technology

The effect of strain on the intrinsic mobility of Si was first investigated in the early 1950's. While this effect was not taking into consider initially, people were recreated in the early 1990's [3]. In 1992 it was first demonstrated that n-channel MOSFETs on a strained Si substrate exhibits higher effective mobility (μ_{eff}) than those on unstrained substrates. After that semiconductor industry has implemented several different technologies to introduce strain in the channel of a MOSFET.

Strain technologies are basically meant to various ways of mechanical stretching and/or compressing the Si crystal lattice. Innovative techniques are used to introduce stress into the MOSFET channel, which required only slight modification of some process steps, thus the additional cost requirement is very small.

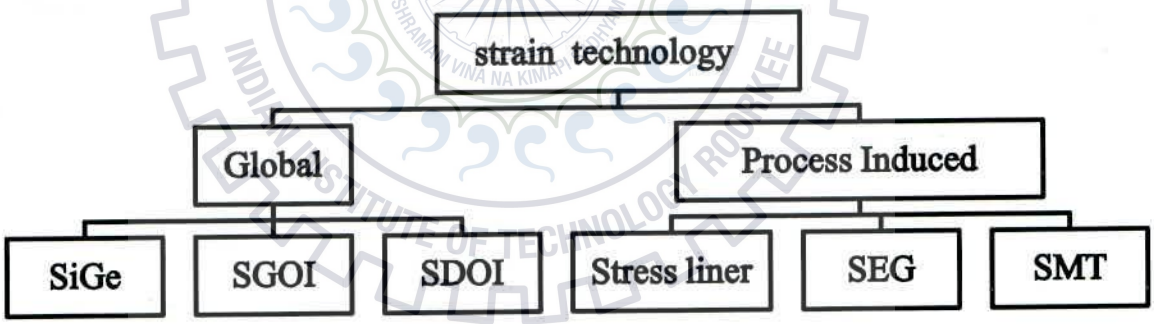


Figure 2.1: summary of the different technology of introducing stress into the MOSFET channel.

This chapter gives an overview of the different techniques of introducing stress into the channel of the MOSFET. These methods are broadly classified into two different categories. These are **(a)** substrate-induced strain which is also called global strain

introducing stress over the entire substrate, **(b)** local strain also called process induced strain. The different stress-induced technologies are summarized in Fig. 2.1.

2.1 Global Strain Techniques

From the name itself, it is very clear that strain is induced in the channel through substrate. It is one of the most effective ways to introduce high tensile strain to the channel of the MOSFET by growing silicon on a relaxed SiGe (Si_{1-y} Ge_y) where 'y' is the mole fraction of Ge in the SiGe alloy. Si and Ge having a lattice mismatch of about 4.2% if we combined together to form a SiGe alloy, the lattice constant of the alloy lies between those of Si and Ge. If a thin layer of Si is grown on a relaxed Si_{1-y} Ge_y layer, the Si layer is forced to assume the larger lattice constant of the underlying Si_{1-y} Ge_y substrate. The Si layer is thus said to be under biaxial tensile strain where the amount of strain is depend on the Ge content (denoted as 'y') in the substrate. Figure 2.2 shows the atomic level representation of the strained and unstrained Si on relaxed SiGe layer. The strain in the plane of the interface between the strained Si layer and the substrate is roughly given by the lattice mismatch,

$$\varepsilon\| = \frac{a_{SiGe} - a_{Si}}{a_{Si}} \quad [7] \tag{2.1}$$

Here, a_{SiGe} and a_{Si} represent the unstrained lattice constant of Si and SiGe respectively, the value of a_{Si} is $5.43A^0$ and the value of a_{SiGe} depends on the mole fraction of the Ge in the alloy and lattice constant of Ge also as given by equation (2.2).

$$a_{Si_{1-x}Ge_x} = 0.5431 + 0.01992x + 0.0002733x^2 \quad [27] \tag{2.2}$$

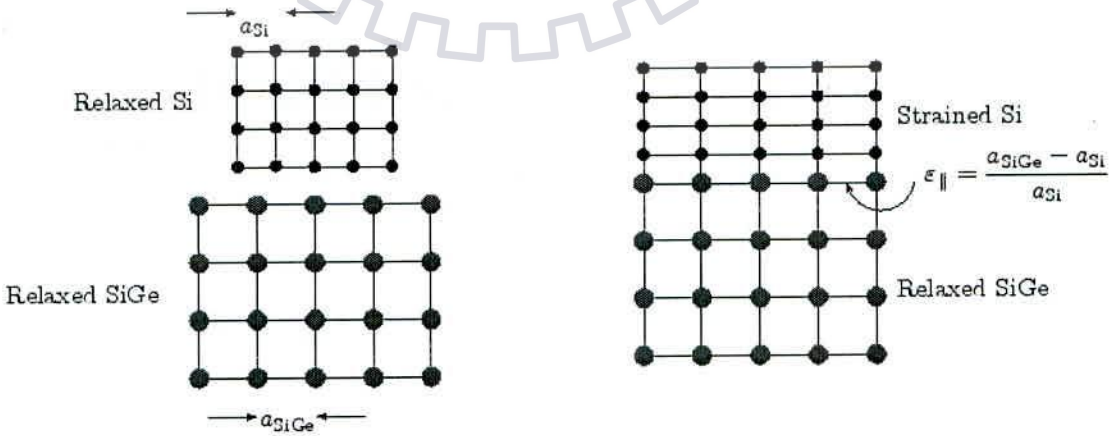


Figure 2.2: Atomic level representation of strain Si over relaxed SiGe

Second way of induced biaxial strain in the channel of the MOSFET is strained Si on SiGe on insulator (SGOI) (see Fig 2.3b). Another technique to introduce biaxial strain in the channel has been proposed by Rim [21]. Rim shows that transistors using ultrathin strained silicon directly on insulator (SDOI) structures (see Fig .2.3c) also behave as a strained silicon device. In that case SiGe layer should be eliminate before transistor fabrication, ultra-thin silicon layer which was there above the SiGe layer providing higher mobility while extenuating the SiGe-induced material through process integration. A SDOI MOSFET structure is fabricated by using a layer-transfer or "wafer-bonding" technique [21]. First, an ultra-thin layer of strained silicon is grown epitaxially on a relaxed silicon germanium (SiGe) layer, than an oxide layer is formed on top of the silicon layer. After finishing of the fabrication step the MOSFET it does not contain any SiGe layer but the strained will be memorized there it's also one type of SMT we can say but the fabrication step of both are completely different. After the complete device fabrication step both electron and hole mobility enhancement have been observed which indicate that strain is retained over there in the channel of the MOSFET [21,22].

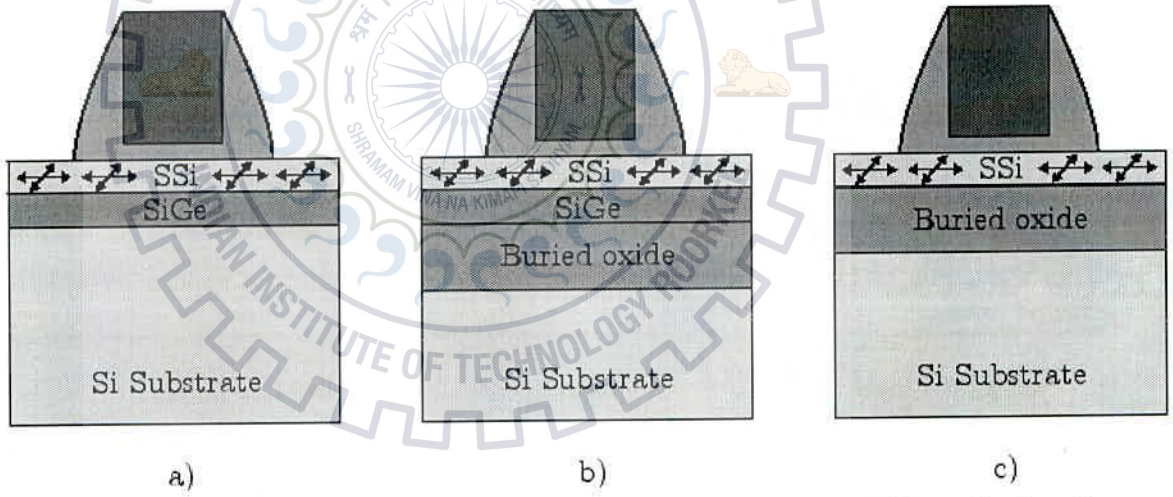


Figure 2.3: MOSFETs showing global (Biaxial) strain:(a) strained Si on SiGe on bulk wafer, (b) strained Si on SiGe on insulator (SGOI), (c) strained Si directly on insulator (SDOI).

Arrow in **Figure 2.3** shows how biaxial stress is there in the channel of the MOSFETs. Biaxial means here stress is there in both longitudinal and lateral direction of the channel of the MOSFETs as shown by the arrows. Biaxial stress advantageous for both n- and p-type MOSFETs but till now not yet introduced into a CMOS logic technology for microprocessors due to the following reason

1) Process integration challenges;

2) Most work showing near zero (very less) hole mobility improvement at the typical operating region of the nanoscale MOSFETs (large vertical electric fields regions). The near zero hole enhancement at the operating region causes the a) advantage to the net logic technology will be small; b) it also increases the p/n MOSFET width ratio beyond the typical range of 2–2.4, which is highly undesirable from fabrication and area constraint point of view, since p-type transistors are already drawn at twice the n-type transistor width;

2.2 Process Induced Strain Techniques

The process induced strain technique overcomes the problem associated with substrate induced strain technique. By this technique we can enhances the performances of both nMOS and pMOS devices independently. Semiconductor industry used this method to include strain in the channel of the MOSFET.

In conventional CMOS fabrication process flows, the stress patterns can arises because of different reason such as variation in processing temperature, variation in coefficient of thermal expansion, variation in growth condition and mechanism, and different dopant implantation. From distribution point of view the process-induced stresses are highly non-uniform in nature it means some part of the device has larger value of stress and some part has small value of stress. Thus by this way it is possible to apply beneficial uniaxial stress in channel region of the MOSFET only instead of applying whole region. For example if we apply uniaxial stress in substrate and in channel region everywhere the substrate leakage current increases which is not desired for MOSFET performances point of view. This technique also called as local strain techniques as we can apply strain locally anywhere in the MOSFET. Initially local strain technique was not able to provide large strain as that of the global strain but this technique enjoy three main advantage as shown below

(i) Strain can be independently applied for enhancement of performance to both n-channel and p-channel MOSFETs.

(ii) Threshold voltage shift is smaller in uniaxially stressed MOSFETs [2].

(iii) Local stress techniques are cheaper and more compatible with standard CMOS technology [21].

The main challenge is to optimize fabrication modules so that stressor will give maximum beneficial effect and minimizing the negative side effect. Three important process-induced strain transfer technique will be discussed in the following section

a) The contact etch stop liner technique (CESL)

b) Selective epitaxy growth (SEG)

c) Stress memorization technique (SMT)

2.2.1 Contact Etch Stop Liner (CESL)

In CESL technique, Local strain is introduced into the Si MOSFET channel via the use of capping layers on the top of the MOSFET. The material used in the capping layers usually of Si nitride (Si_3N_4) which can be grown using CVD techniques after the completion of salicide formation, and these capping layer produce compressive and tensile as per the different deposition condition like ambient temperature. Different stress has different impact on hole and electron, it has been showed that tensile stress is favourable for electron and compressive for hole. So by using this technique we can avoid the problem associated with biaxial stress that is same type of stress i.e. tensile it induced for both n- and p- MOSFETs. Fabrication of CMOS transistor and getting the advantage from stress point of view is easy here and equal for both [23].

In CMOS transistor architectures case we have to apply both tensile and compressive stress liner to the single wafer. Basically this method is called dual stress liner (DSL) technique it means both type of stress liner will be there. In this DSL technology, first a tensile nitride (Si_3N_4) layer is deposited over the entire wafer (on both p- and n- MOSFET), the very next step we have to patterning and etching that tensile layer from pMOS transistor . Afterwards, a compressive nitride film is deposited over the entire wafer and is etched off from the nMOS transistors (see fig 2.4). By this way we can improve the performance of both nMOS and pMOS simultaneously. CESL technique improve both linear and saturation drive current [24]. It has already been reported that nitride layer gives 2.0GPa tensile and 2.1GPa compressive stress in the channel of the MOSFETs [24].

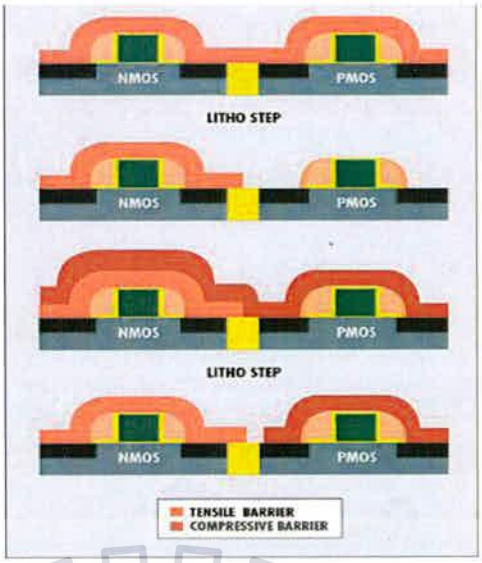


Figure 2.4: Process Integration Step For DSL.

2.2.2 Selective Epitaxial Growth Technique (SEG)

It is a direct way to provide strain to the channel of p- and n-MOSFETs by filling source/drain with SiGe and SiC respectively. SiGe and SiC grown epitaxially in the source drain region of the MOSFET and in the extended region also. Lattice constant of SiGe is greater than Si so it gives uniaxial compressive stress (see Fig 2.5) in the channel region of the MOSFET which is required stress for p-MOS. Similarly lattice spacing of SiC is less than Si so it gives uniaxial tensile stress (see Fig 2.5) in channel region which is required stress for n-MOS. Few extra fabrication steps are required after spacer formation, such as selective Si etched out from the Source/Drain region, growth of SiGe/ SiC (p/n) in that etched region and in-situ doped Source/Drain. Simultaneously both DSL and SEG technique can be used for performances enhancement.

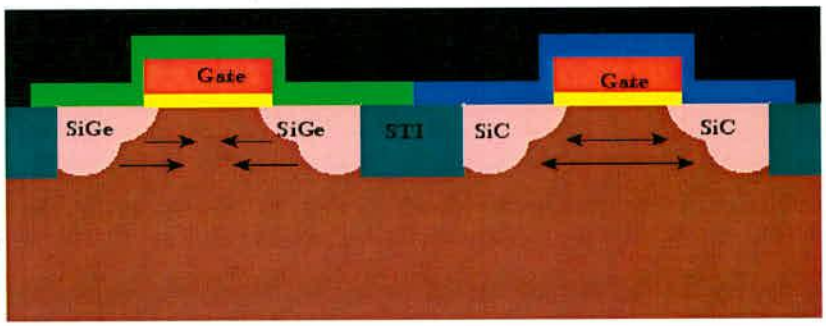


Figure 2.5: CMOS transistor with SEG and DSL

2.2.3 Stress Memorization Technique (SMT)

This technique is used for enhancement of performance of n-MOS only. It degrades the performances of p-MOS. p-MOS should be perfectly masked while doing the SMT fabrication for n-MOS. Fabrication point of view it is somewhat easy but protecting p-MOS from SMT i.e. the masking should be very good quality one. Actually stress is induced in the channel here after the high temperature annealing process. At the time of SMT process, polysilicon gate is surrounded by nitride/oxide layer from all sides except the beneath of the gate (SiO_2/Si interface). When RTA is performed, all materials are expanding as per theirs thermal properties. Polysilicon expands more as compared to the enclosing nitride layer, so it exerts a stress outward to the material enclosing it (see Fig 2.6). Hardness point of view nitride is stronger than polysilicon, so nitride will resist the expansion of polysilicon. Now the only way for polysilicon is to expand towards the Si/SiO_2 interface, which results lateral tensile stress and perpendicular (vertical) compressive stress in the channel region of the MOSFET. The annealing temperature in the SMT state is very high, so that the polysilicon goes from elastic state to the plastic state. After cooling also the poly silicon will remain in its expands state.

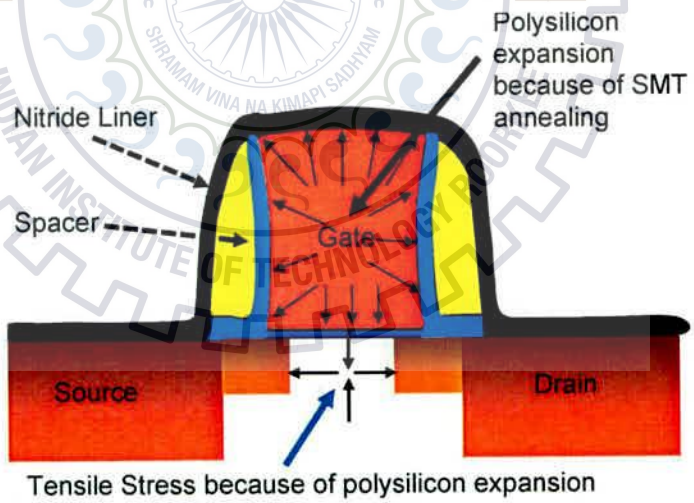


Figure 2.6: Stress transfer by SMT process in to the MOSFET channel [25].

Chapter-3

Effect of Strain on Band Structure

Theory of elasticity basically describes the concept of stress and strain. Both stress and strain are tensorial quantity and they are dependent through Hooke's law. Here we will discuss the definition of stress-strain and how these are related to the silicon crystal structure. We have to do each analysis of Si band structure based on its crystal co-ordinate system. Stress co-ordinate system is nothing but device co-ordinate system. So we propose here a simple formula based on the co-ordinate transformation, so that we can easily convert one co-ordinate system to other co-ordinate system.

3.1 Theory of Elasticity

Elasticity is a property of solid materials, it defines how a certain material changing its shape when external force is applied on it and how it regains its original shape after the removal of external force.

3.1.1 Stress

Stress is defined as force per unit area. Force may be external or may be internal one. It categorized in to two types based on the direction of applied force. If the applied force is perpendicular to the plane it is called normal stress, direction of the applied force in this case is parallel to the direction ratios. Second one is shear stress in which case direction of applied force is parallel to plane of surface.

3.1 shows the visual image of the stress component acting on the faces of an infinitesimal cube of solid. In particular, stress applied on each face of the cube contains one axial component (normal stress component) and two shear stress component. For example consider the front plane which is orthogonal to the x-axis has T_{xx}-normal stress component and T_{xy},T_{xz}- are two shear stress component. Let's assume the total force acting in the small area be 'ΔF' which has three component as shown below.

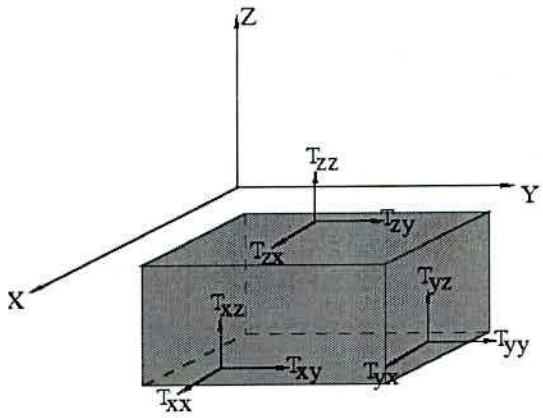


Figure 3.1: stress tensor component visualization.

$$\Delta F = \Delta F_x . i + \Delta F_y . j + \Delta F_z . k \tag{3.1}$$

ΔF_i =force acting in the i^{th} axial direction.

T_{ij} = Stress acting on a plane where subscript i and j are plane direction and force direction respectively.

$$T_{xx} = \lim_{\Delta A_x \to 0} \frac{\Delta F_x}{\Delta A_x}, \quad T_{xy} = \lim_{\Delta A_x \to 0} \frac{\Delta F_y}{\Delta A_x}, \quad T_{xz} = \lim_{\Delta A_x \to 0} \frac{\Delta F_z}{\Delta A_x} \tag{3.2}$$

Other stress components can calculated by using equation 3.2 with few changes as per subscript. Total stress component can write in a matrix format

$$T_{3\times3} = \begin{pmatrix} T_{xx} & T_{xy} & T_{xz} \\ T_{yx} & T_{yy} & T_{yz} \\ T_{zx} & T_{zy} & T_{zz} \end{pmatrix} \quad [7,31] \tag{3.3}$$

Actually our solid cube is in static equilibrium, so the condition for static equilibrium is

$$T_{ij} = T_{ji} \tag{3.4}$$

By applying this condition, we can reduce this 12-stress component in to six components. Then we can write it in a column vector

$$T_6 = \begin{pmatrix} T_{xx} \\ T_{yy} \\ T_{zz} \\ T_{yz} \\ T_{zx} \\ T_{xy} \end{pmatrix} \quad [31] \tag{3.5}$$

3.1.2 Strain

It gives the amount of deformation in shape and size of an elastic and plastic material under the applied force. Mathematically it represent as the change in length divide by original length (For one-dimensional strain case). Strain also categorized into two-type shear strain and normal strain based on applied force. Normal stress causes normal strain and shear stress causes shear strain. Like stress tensor matrix strain tensor also has a (3×3) matrix and it will finally reduce to a column matrix as shown below

$$\epsilon_{3\times3} = \begin{pmatrix} \epsilon_{xx} & \epsilon_{xy} & \epsilon_{xz} \\ \epsilon_{yx} & \epsilon_{yy} & \epsilon_{yz} \\ \epsilon_{zx} & \epsilon_{zy} & \epsilon_{zz} \end{pmatrix} \quad [7,31] \tag{3.6}$$

$$\epsilon_6 = \begin{pmatrix} \epsilon_{xx} \\ \epsilon_{yy} \\ \epsilon_{zz} \\ \epsilon_{yz} \\ \epsilon_{zx} \\ \epsilon_{xy} \end{pmatrix} \quad [31] \tag{3.7}$$

We can write equation 3.6 in form of equation 3.7 under the stable equilibrium case, where (3×3) matrix is a symmetric matrix one.

3.1.3 Stress, Strain Relationship

For band structure calculation purpose we need each stress and strain component is in crystal co-ordinate system. In the next section we will discuss how we transform these parameters from one co-ordinate system to other. For the timing we assume that all stress and strain components are in crystal co-ordinate system. Stress and strain related through the elastic stiffness and elastic compliance constant.

For semiconductor like Si, Ge or GaAs the elastic compliance matrix contain only 3 independent components S_{11},S_{12} and S_{44} and strain to stress relation reads [31]

$$\epsilon_6 = \begin{pmatrix} M1_{3\times3} & M2_{3\times3} \\ M3_{3\times3} & M4_{3\times3} \end{pmatrix} T_6. \text{ [31]} \tag{3.8}$$

$$M1_{3\times3} = \begin{pmatrix} S_{11} & S_{12} & S_{12} \\ S_{12} & S_{11} & S_{12} \\ S_{12} & S_{12} & S_{11} \end{pmatrix} \tag{3.9}$$

$$M2_{3\times3} = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \tag{3.10}$$

$$M3_{3\times3} = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \tag{3.11}$$

$$M4_{3\times3} = \begin{pmatrix} S_{44}/2 & 0 & 0 \\ 0 & S_{44}/2 & 0 \\ 0 & 0 & S_{44}/2 \end{pmatrix} \tag{3.12}$$

Inverse of equation 3.8 will give the relationship between stress and strain

$$T_6 = \begin{pmatrix} M1'_{3\times3} & M2'_{3\times3} \\ M3'_{3\times3} & M4'_{3\times3} \end{pmatrix} . \epsilon_6 \text{ [31]} \tag{3.13}$$

$$M1'_{3\times3} = \begin{pmatrix} C_{11} & C_{12} & C_{12} \\ C_{12} & C_{11} & C_{12} \\ C_{12} & C_{12} & C_{11} \end{pmatrix} \tag{3.14}$$

$$M2'_{3\times3} = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \tag{3.15}$$

$$M3'_{3\times3} = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \tag{3.16}$$

$$M4'_{3\times3} = \begin{pmatrix} 2C_{44} & 0 & 0 \\ 0 & 2C_{44} & 0 \\ 0 & 0 & 2C_{44} \end{pmatrix} \tag{3.17}$$

The values of elastic stiffness and elastic compliance constants are addressed in table 3.1

Table 3.1: Elastic compliance and elastic stiffness constant for Si. [31]

Elastic constants	Value for Si	Unit
C_{11}	1.66×10^{11}	Pa
C_{12}	6.4×10^{10}	Pa
C_{44}	7.96×10^{10}	Pa
S_{11}	8.31×10^{-11}	$(Pa)^{-1}$
S_{12}	-2.56×10^{-11}	$(Pa)^{-1}$
S_{44}	1.256×10^{-10}	$(Pa)^{-1}$

3.1.4 Change of Co-ordinate System for Strain and Stress

We have to change the co-ordinate system from device to crystal. When we apply the stress, we known the stress value in the form of DCS but for calculation of shifting in valley we have to get this stress in CCS. At the time of simulation, we have to fix our co-ordinate system as per requirement. In industries, people are using (001) wafer (industries standard wafer) with [110] channel direction. For this crystal the y and z direction of device coincide with [-110] and [001] direction of CCS. We have to generate a rotational matrix based on this Co-ordinate system. Generalized expression for rotational matrix (R_{rot}) reads as below

Table 3.2: DCS and CCS alignment.

DCS	CCS
x-Axis	$[a_1\ b_1\ c_1]$
y-Axis	$[a_2\ b_2\ c_2]$
z-Axis	$[a_3\ b_3\ c_3]$

$$R_{rot} = \begin{pmatrix} \frac{a_1}{\sqrt{a_1^2+b_1^2+c_1^2}} & \frac{a_2}{\sqrt{a_2^2+b_2^2+c_2^2}} & \frac{a_3}{\sqrt{a_3^2+b_3^2+c_3^2}} \\ \frac{b_1}{\sqrt{a_1^2+b_1^2+c_1^2}} & \frac{b_2}{\sqrt{a_2^2+b_2^2+c_2^2}} & \frac{b_3}{\sqrt{a_3^2+b_3^2+c_3^2}} \\ \frac{c_1}{\sqrt{a_1^2+b_1^2+c_1^2}} & \frac{c_2}{\sqrt{a_2^2+b_2^2+c_2^2}} & \frac{c_3}{\sqrt{a_3^2+b_3^2+c_3^2}} \end{pmatrix} = \begin{pmatrix} p_1 & q_1 & r_1 \\ p_2 & q_2 & r_2 \\ p_3 & q_3 & r_3 \end{pmatrix} \quad 3.18$$

$$R_{D\to C} = \begin{pmatrix} p_1^2 & q_1^2 & r_1^2 & 2q_1r_1 & 2p_1r_1 & 2p_1q_1 \\ p_2^2 & q_2^2 & r_2^2 & 2q_1r_1 & 2p_2r_2 & 2p_2q_2 \\ p_3^2 & q_3^2 & r_3^2 & 2q_3r_3 & 2p_3r_3 & 2p_3q_3 \\ p_2p_3 & q_2q_3 & n_2n_3 & q_2r_3 + q_3r_2 & p_2r_3 + p_3r_2 & p_2q_3 + p_3q_2 \\ p_1p_3 & q_1q_3 & n_1n_3 & q_1r_3 + q_3r_1 & p_1r_3 + p_3r_1 & p_1q_3 + p_3q_1 \\ p_2p_1 & q_2q_1 & n_2n_1 & q_1r_2 + q_2r_1 & p_1r_2 + p_2r_1 & p_1q_2 + p_2q_1 \end{pmatrix} \quad 3.19$$

In equation-3.19, $R_{D\to C}$ represent the transformation matrix, which is derived from the rotational matrix. For convert stress and/or strain from DCS to CCS we use $R_{D\to C}$.

$$\epsilon_{c,6} = R_{D\to C,6} \times \epsilon_6 \quad [31,7] \quad 3.20$$

$$T_{c,6} = R_{D\to C,6} \times T_6 \quad [31,7] \quad 3.21$$

Where subscript 'c' in above equation represent that parameter is in CCS, without 'c' represent in DCS. Now by using the above equations we can happily get all stress, strain in CCS, which is our first and foremost requirement.

3.2 Effect of Stress on Valence and Conduction Band

Effect of enhancement of device current of MOSFET can easily be interpreted through band gap and band structure engineering. Strain has so many interesting feature like it decreases the band gap of the semiconductor, it breaks crystal symmetry, symmetry of conduction band also destroy, band splitting occurs in valence band and carrier repopulation and many more affect. However, these effects give a new light to the semiconductor field. Stress will enhance the drive current by enhancing the mobility of the carrier, also carrier can move faster in the presence of stress. Faster movement is because of changes of lattice spacing, as tensile stress is applied to channel of MOSFETs inter atomic distance increases that will provide a better corridor for electron movement.

3.2.1 Effect on Conduction Band

Conduction band of unstrained Si/Ge have a six ellipsoidal valleys, which are degenerate in EK-space. Figure 3.2 shows this unstrained degeneracy. Energy minimum of all six ellipsoidal valleys are same in unstrained. Δ6-degeneracy split to Δ2 and Δ4 degeneracy state. Here our all discussion based on uniaxial stress which applied in the <110> direction, this analysis is valid for biaxial stress in <100> and <010> too. When we apply uniaxial stress

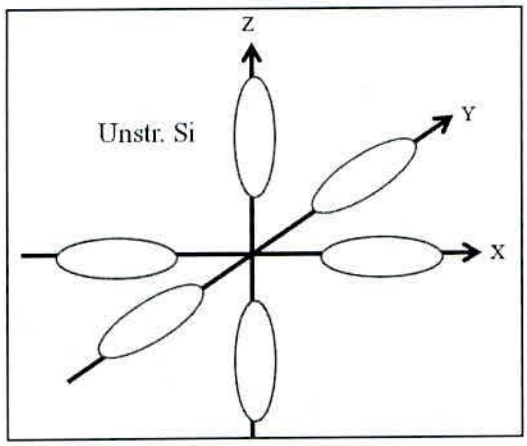
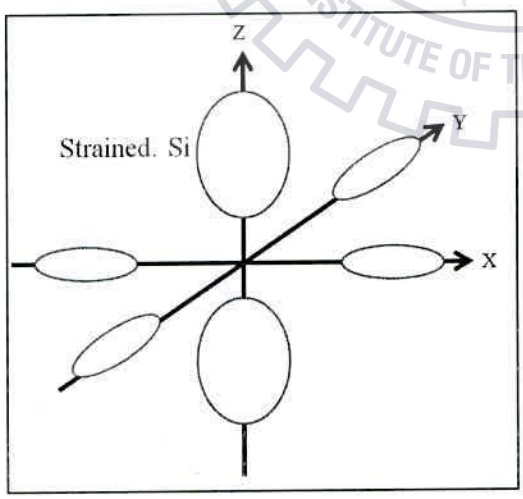


Figure 3.2: Conduction Band Valley of Unstrained Si.

along <110> direction x- and y- valleys (Δ4 valleys) are move away from the original energy position (see fig 3.3). Now the minimum of all valleys are different, Δ2 and Δ4 valleys have some energy gap between them. This energy gap increases with increases in stress. For this case, Δ4 valleys have higher energy than Δ2 valleys, it is for tensile stress case and if it is compressive things will be reverse. So now, electrons preferentially try to stay in the Δ2 valleys, because it is minimum energy state (see fig 3.4), which results lowering in plane effective transport mass as our transport happens in the <110> direction. The splitting of valley degeneracy also affect on the scattering rate, which will discusses in later section of this chapter.



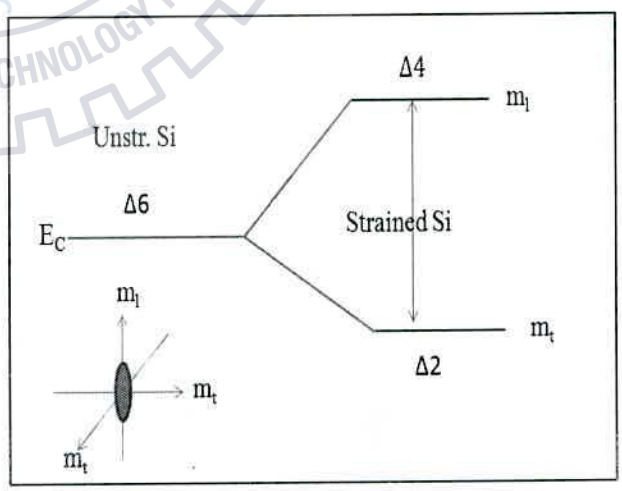


Figure 3.3: Conduction Band Valley for Strained Si, **Figure 3.4**: Δ2 and Δ4 valley location.

As the shifting of valleys is asymmetric, so different valley shift different amount of energy level along E-axis. Deformation potential theory gives the details about the shifting of valley (we use this as a model for simulation). By using this model, we can numerically calculate the position of valleys along different axial direction.

$$\Delta E^{i}_{c,tot} = \Delta E^{i}_{axial} + \Delta E^{i}_{shear} \quad [6\text{-}9] \qquad 3.22$$

Here superscript 'i' represent for x,y, and z axis valleys.

ΔE^{i}_{axial} = Amount of shifting of i^{th} valley along E-axis because of normal (axial) strain.

ΔE^{i}_{shear}= Amount of shifting of i^{th} valley along E-axis because of shear strain.

For our case there is no shear strain components ($\epsilon_{xy}=\epsilon_{yz}=\epsilon_{xz}= 0$) otherwise things are more complicated like the shape of the ellipsoid changes, from prolate to scalene. This changes of ellipsoidal shape have effect on effective masses so indirectly effective mass depend on the shear strain.

$$\Delta E^{i}_{c,tot} = \Delta E^{i}_{axial} = \Xi_d(\epsilon_{c,xx}+\epsilon_{c,yy}+\epsilon_{c,zz}) + \Xi_u(\epsilon_{c,ii}) \qquad 3.23$$

Ξ_d=Dilation deformation potential constant = 1.1eV [7,8]

Ξ_u = Shear deformation potential constant = 9.29eV [7,8]

3.2.2 Effect on Valence Band

Stress has similar effect on the valence band on Si lattice. It split the 2-fold degeneracy of the valence band. Si has two parabolic type band structures in its valence band. These are named as light hole band and heavy hole band as per there effective mass of hole. In HH case, the effective mass of hole is more as compare to the LH band. These effective masses are derived from curvature of the band. Both HH and LH band are degenerate at the 'Γ' point of the first Brillouin zone as shown in the figure 3.5. The 'Γ' point actually the origin of the K-space co-ordinate system. As we are analysing the case of valence band means we are trying to explain how stress effect on the hole mobility case, for hole mobility to enhance we have to apply uniaxial compressive stress. Figure 3.5 shows the valence band of Si in unstrained case and the next one is the strained Si. In case of strained the band at the 'Γ' point Split away, the heavy hole band goes up and its shape also changes after changing its shape it behave as a light hole band, because the curvature of band increases which results decreases

in effective mass of hole. Other interesting thing happens here is as the HH band goes up with respect to energy axis but the hole energy decreases in the positive direction of E-axis, so now more number of holes are trying to stay in that band which results decreases in plane effective mass of hole. As the effective mass decreases mobility increases, movement will be faster one and drive current increases and so on. Here in this dissertation we discuss more about electron, so the above just a overview what happen to the valence band in presence of stress.

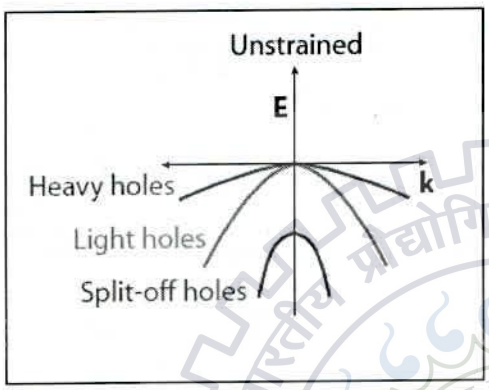


Figure 3.5: Valence Band of Si

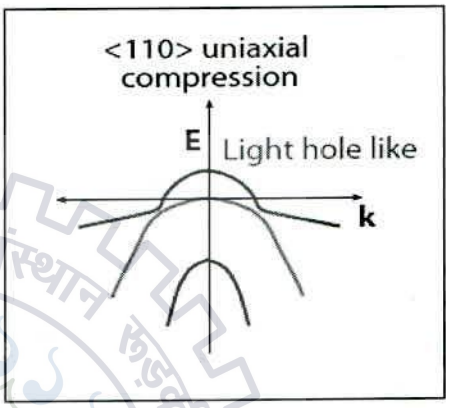


Figure 3.6: Valence Band of Si strained Case

3.3 Effect of Stress on Carrier Concentration

Current conduction in n-type semiconductor is taking place mostly because of the carrier (free electron), which are present at the conduction band. In figure 3.2 it is shown that the ellipsoids, which are present in conduction band are of equal size, but this is the case for unstrained Si. Size represents the number carrier in it. In case of strained Si the sizes of the valleys are different, from which we clear that different valleys contain different number of carrier. The 6-ellipsoid we divided in to 3 groups of valley, 2-valley on the same axis represent as a single group. These groups are named as per the axis where they present. The expression for concentration of electron in conduction band is well known by the formula given below.

$$n_0 = N_C e^{[-(\frac{E_C - E_F}{KT})]} \quad [10] \qquad 3.24$$

Each group of ellipsoid contain one third of the total number of electron present in the conduction band. So we can write equation for the electron present in X-valleys as read below.

$$n_{unstr}^{X} = \frac{N_C}{3} e^{[-(\frac{E_{C,unstr}^{X} - E_F}{KT})]} = \frac{n_0}{3} \quad 3.25$$

Here the subscript 'unstr' represent unstrained Si case.

$$n_{str}^{X} = \frac{N_C}{3} e^{[-(\frac{E_{C,str}^{X} - E_F}{KT})]} \quad 3.26$$

Subscript 'str' represents strained Si.

Ratio between the equation 3.25 and 3.26 gives

$$\frac{n_{str}^{X}}{n_{unstr}^{X}} = e^{[\frac{E_{C,unstr}^{X} - E_{C,str}^{X}}{KT}]} = e^{[\frac{-\Delta E_C^X}{KT}]} \quad 3.27$$

By using equation 3.25 we can write 3.27 as

$$n_{str}^{X} = \frac{n_0}{3} \times e^{[-\frac{\Delta E_C^X}{KT}]} \quad 3.28$$

Where ΔE_C^X - represents shifting of X-valleys along E-axis because of stress. This value can calculate by using equation 3.23. For Y and Z- valleys we have to follow the same rule only superscript 'X' replace by Y and Z. For our case we apply uniaxial stress along <110> direction we get the value of $\Delta E_C^X, \Delta E_C^Y$ and ΔE_C^Z are positive, positive and negative respectively. From this, roughly we clear that after stress application carriers are populated in Z-valley, which satisfy the figure 3.3.

3.4 Effect of Stress on conductivity Effective Mass

In silicon, there exist six equivalent conduction bands along the [100], [010], and [001] direction, the shape of these bands are ellipsoidal in shape. Ellipsoid has two minor axes and one major axis. Two minor axis lengths are equal and which are less than that of the length of major axis. Along the minor and major axis, ellipsoid has different curvature and different radius of curvature, which results different effective masses in different direction as shown in figure below.

We have to use transverse or longitudinal effective mass as per the direction of movement of carrier, for example if the movement is along X-direction then we have to take m_l- for X-valleys and m_t- for Y and Z- valleys.

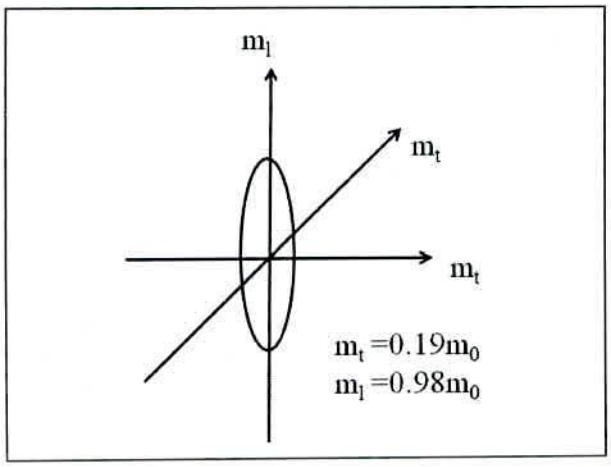


Figure 3.7: Illustration of one conduction band valley of Si.

Another important parameter we have to taking care here is probability of occupancy of valleys. For unstrained Si case each ellipsoid have equal number of electron, so the probability of each valley pair is 1/3, but for strained Si it is not the same one. Probability of occupancy of valleys calculation is shown below.

$$P^i = \frac{n^i_{str}}{n^X_{str}+n^Y_{str}+n^Z_{str}} \qquad 3.29$$

Where P^i = probability of 'i' valley, where 'i' is either X or Y or Z.

For unstrained Si case

$$P^X = P^Y = P^Z = 1/3 \qquad 3.30$$

Now we have to include probability occupancy in to the conductive effective mass calculation equation as shown below.

$$\frac{1}{m_c} = \frac{P^X}{m_l} + \frac{P^Y}{m_t} + \frac{P^Z}{m_t} \qquad 3.31$$

The above equation valid when transmission is along X-direction and the DCS and CCS are aligns each other. Similarly if the transmission along Y-direction we have to take 'm_l ' for Y-valleys and transverse effective mass for X and Z- valleys.

When biaxial stress is applied along <100> and <010> direction (or uniaxial along <110> direction) the value of P^Z will be greater than 1/3, where as the value of P^X and P^Y will

be less than 1/3, because the carriers are populated in the Z-valleys. From above formula, we can easily conclude that effective conductive mass decreases because of the applied stress.

3.5 Effect of Stress on Carrier Mobility

Figure 3.8 shows types of scattering are there in conduction band of Si.

τ_g = Acoustic intra valley scattering and inter valley scattering between equivalent valleys, also called g-type scattering or momentum relaxation scattering.

τ_f = Inter valley scattering between non-equivalent scattering between non-equivalent valleys, also called f-type scattering or energy relaxation time.

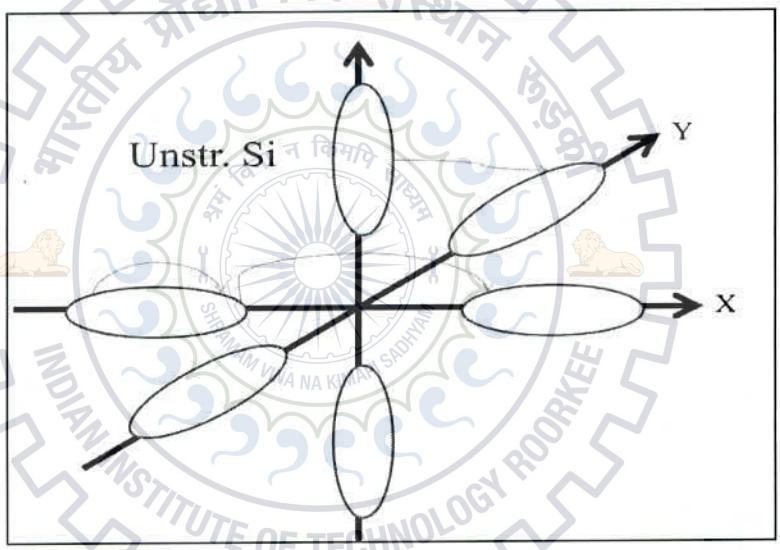


Figure 3.8: Inter and intra valley scattering process in Si.

In case of unstrained Si, all six ellipsoids are in degenerate state. In degenerate state carrier can happily move from one valley to the other because they are in the same energy level no extra energy is required for them. In case of strained Si valleys are not in the same energy level, so here hopping of carrier from one valley to the other are not as frequent as that of earlier one. So the average time between scattering increases, as the equation

Chapter-4

Effect of Strain on Device Current

In this chapter, we will discuss about MOSFET current equation in different carrier transport condition like diffusive, quasi-ballistic and ballistic region of operation. We will also discuss here how these current is dependent on stress directly or indirectly which we apply in the channel of the MOSFETs. The device what we simulate over here is of 32nm technology node (Gate length=32nm) but the distance between two contact is around 18nm which is the major part to concern. As we discussed in the previous chapter that mobility is increase with stress, so if any current equation dependent on mobility it's very simple to prove that current increases with stress, but if the current equation not dependent on mobility directly than we have to figure out which parameter dependent on stress and how?

4.1 Carrier Transport in MOSFETs

Carrier transport in MOSFETs devices is basically depending on its relative dimension i.e. the distance between the two contacts (Source/Drain). For my device the distance between two contacts is in between 16nm to 18nm. Mean free path (MFP) and the distance between contacts will determine in which region my device is working. Figure 4.1 shows the necessary criteria for different carrier transport in nano MOSFETs. The MFP for my device is around 6nm, so we can say distance between contacts is nearly equal to the MFP (L ≈MFP). From this we can clear that my little nano device working in the quasi ballistic region of operation. In the next section we will write more a couple of line about different transport mode and current equation in that mode but the major concern for us is quasi ballistic region of operation, so we have to discuss detail about that and see how strain will affect on performances.

In quasi ballistic region very less number of scattering is face by the carrier throughout his journey. The scattering potential may be ionize impurity, lattice vibration, surface roughness, etc. In this case also few carrier reach to the second contact without any scattering, but the number of such carrier is very less. For present day fabricated MOSFETs

the distance between contact (between 45nm to 10nm range) and MFP are comparable to each other.

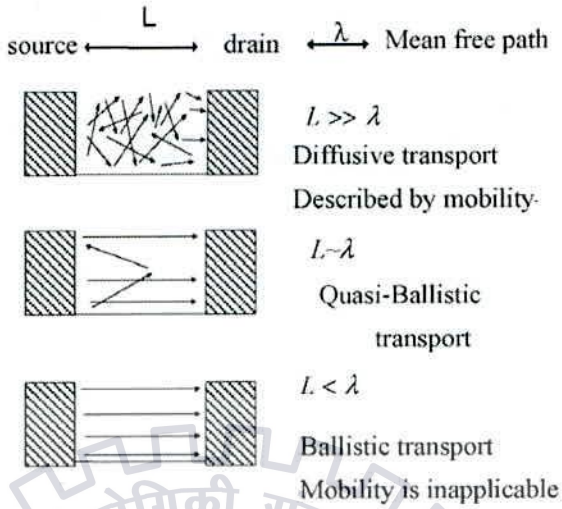


Figure 4.1: Necessary condition for different carrier transport [1].

The transport is said to be diffused when the distance between the contact is many more times of the MFP (see Fig 4.1), and it is well characterized by mobility theory. In this type of transport case the carrier suffers so many scattering throughout his journey, but the number of scattering is different in different region also. For example in MOSFET case in diffusive mode carrier suffer more scattering at the drain side as compared to source side because on the drain side the electric field is very high and also the kinetic energy of the carrier which causes more scattering. The carrier at the beginning is biased towards the second contact by applying some voltage to that contact, after suffering huge number of scattering also the carrier is bound to reach the second contact anyhow.

The transport is said to be ballistic when the distance between the contact is less than that of the MFP (see Fig 4.1), and it cannot characterize by mobility theory because the general mobility equation is not applicable here, if we apply also we will get mobility value infinite which is unacceptable value. In this type of transport movement of the carrier is like a rocket. No scattering is there throughout the journey between the contacts. In ballistic case the device current completely described by carrier injection from the source to the channel of the MOSFET. For current equation in the quasi ballistic region first we have to see the current equation in the ballistic region where no scattering is there, transport is fully ideal one. For quasi ballistic case we have to simply multiply an efficiency type of constant to

taking into account the scattering over there, which we will discuss in the next section of this chapter.

4.2 Current Expression in Different Transport Mode

In this section we will discuss device current in different transport mode like diffusive, quasi ballistic and in ballistic mode. We will also discuss how these current will be affected by applying stress in to the channel of the MOSFETs.

4.2.1 Diffusive Transport

In this case conventional mobility theory used to derive the drain current. Basically level-1 equation of MOSFET is nothing but diffusive transport equation (see Eqn. 4.1). Equation below shows the current equation in both linear and saturation region of operation for long channel device (Diffusive Transport).

$$I_{D\,lin} = \mu_{eff}\, C_{ox} \frac{w}{L} \left[\left(v_{gs} - v_{T,lin} \right) \times v_{ds} - \frac{v_{ds}^2}{2} \right] \quad 4.1$$

$$I_{D\,sat} = \frac{1}{2} \mu_{eff}\, C_{ox} \frac{w}{L} \left[\left(v_{gs} - v_{th,sat} \right)^2 \right] \quad 4.2$$

Here we can see that the only term which will be modulated by the stress is effective mobility. We already discussed how the favourable strain increases the mobility through band splitting and carrier redistribution. Linear and saturation threshold voltage also depends on stress (decreases) for the timing we are assuming that this parameter is invariable with respect to stress for making analysis to be easier and simple one.

4.2.2 Ballistic Transport

This type of transport happens when the distance between the contact (source and drain) sufficiently smaller than the MFP and probability of scattering of carrier in the channel region sufficiently small /or negligible. In ballistic transport case current from source to drain is completely dependent on the injection of the carrier from the source into the channel of the MOSFET. Ballistic transistor basically ideal devices where we are assuming no scattering throughout the journey which is an idealistic assumption, which cannot be achieve in real life fabrication process. People ranked ballistic MOSFETs as a scaling limit, we cannot go

beyond this dimension limit. The advantage of studying the characteristics of this type of MOSFETs is that it will help to analyse the quasi ballistic MOSFETs, where the state-of-the-art of CMOS technology flow is. Second merit of this analysis is we can judge how the contemporary technology close to the ballistic limits one. The current in this region is just product of carrier density, which is dependent &/or controlled by the MOS cap, and the carrier velocity, which is yielded from the carrier transport phenomena. Equation below shows the current expression in the ballistic region.

$$I_{D\,sat} = w\, v_{inj}\, C_{ox} \left(v_{gs} - v_{th}\right) \quad [15\text{-}17] \qquad 4.3$$

We are writing here $I_{D\,sat}$ because as it is ballistic one if we apply small voltage also the velocity in the channel region goes above the saturation velocity of the carrier. Each and every point along the channel region velocity of the carrier is more than its saturation velocity we will discuss more about this in the later part of this dissertation. But for the timing we should keep in mind that the saturation is due to velocity saturation. In equation 4.3 the only parameter to be discussed is injection (v_{inj}). Here we will discuss only what exactly the injection velocity is and in later chapter we will discuss what will be the effect of the stress on injection velocity. For this we have to go for barrier model of the MOSFETs which is also a way to analyses all the characteristics of little nano devices.

4.2.2.1 Barrier Model for MOSFETs

It describes how the carriers face barrier or obstacle when they move from one contact to the other contact. Here we discuss only the flow of electron (For nMOS only) between the contacts, for hole everything is same only the difference is sign in every aspects. Figure below shows the barrier face by the electron at the left contact and also in the right contact when there is no bias is applied between them.

Electron of certain energy when they are trying to moves from the left contact to the right they will face some barrier as shown in the Fig 4.2. But few electron (very less number) will moves from left to right as per the transmission probability of the contact but here we are not applying any voltage between the contact so the transmission probability of right and left contact is equal, so total number of flow of electron from left to right is equal to the number of electron from right to left therefore net flow of carrier is zero, which is the actual case i.e. when zero bias is applied drain current is zero [32]. Our main objective why we apply bias in the contact is to decrease the so that the flow of carrier will be possible. The barrier can

decrease by applying gate voltage and also by applying drain voltage. Here we give only one special case as shown in figure below.

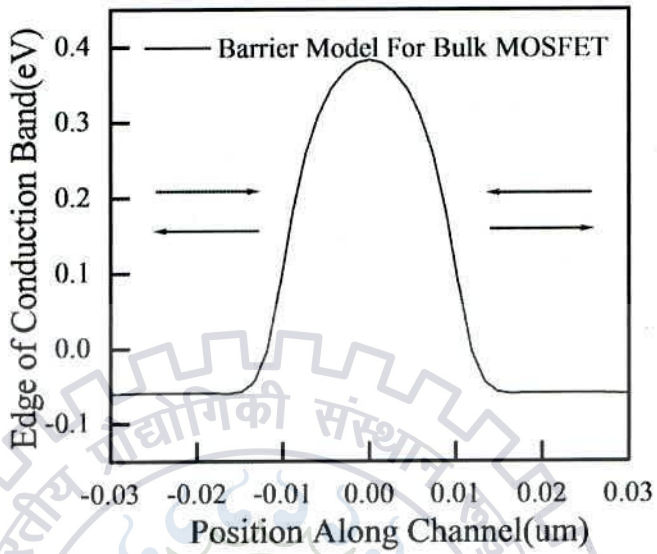


Figure 4.2: Barrier Model for MOSFETs.

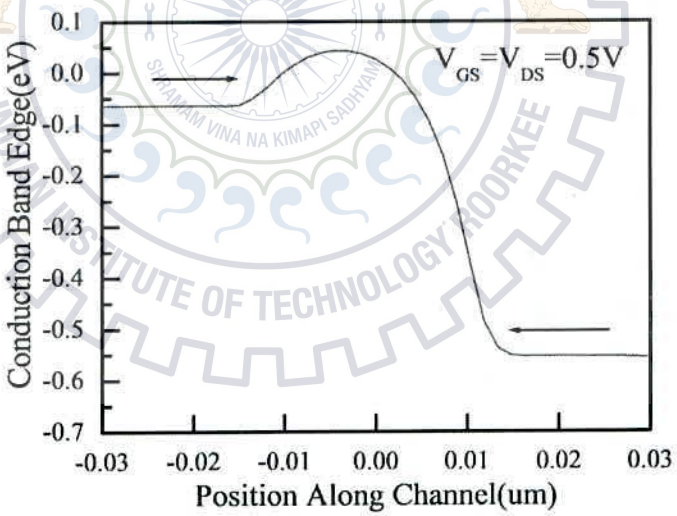


Figure 4.3: Conduction Band Edge vs Position from S/D (Bias Voltage 0.5V).

Figure 4.3 shows how barrier for electron decreases because of the applied voltage and also here we see the electron at the right and left contact face different amount of barrier. Carrier (electron) at the left contact face less barrier so they can easily move from left to right where as carrier at the right contact face huge amount of barrier so it is not possible for them to moves from right to left. The electron which comes from the left contact when they reach

at the right contact the kinetic energy of that electron increases, so the number of scattering face by them at the left side is very less but at the right side is more. Net flow of carrier here from left to right (positive direction of x-axis as per convention) and flow of current is negative direction of x-axis.

4.2.2.2 Injection Velocity (v_{inj})

From fig 4.3 we can see that for a carrier to move from the left contact to the right first it goes to the top of the barrier and then towards the second contact. The left contact is actually behave as the thermal equilibrium reservoir. The top of the barrier also called the virtual source for the nano devices [15-17]. The velocity of the carrier at this top of the barrier is called injection velocity (see fig 4.4). This velocity is a major factor in the current equation of ballistic and quasi-ballistic MOSFETs. In the later section of this dissertation we will see how injection velocity depends on applied stress in the channel of the MOSFETs. Uni-directional thermal (V_T) velocity is the upper limit for V_{inj}, because the carrier injected from the source which is in thermal equilibrium state [18].

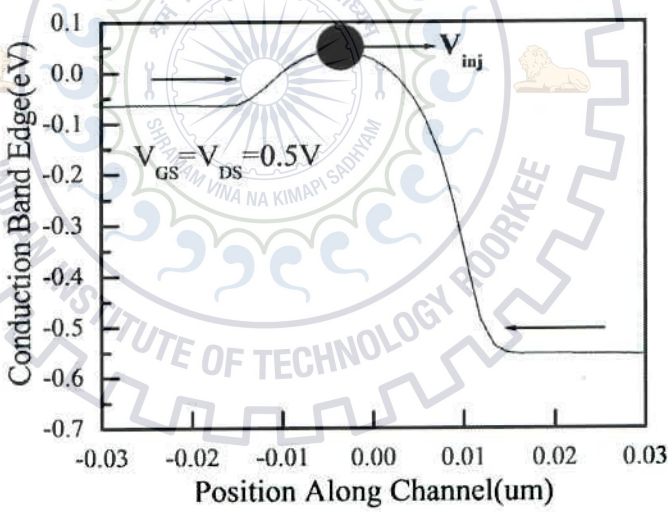


Figure 4.4: Conduction Band Edge vs Position from S/D showing the Location of injection velocity (V_{inj}).

4.2.3 Quasi-Ballistic Transport

In Quasi-ballistic transport case small number of scattering is suffered by the carrier when they move from left contact to the right contact. In nano scale MOSFETs off-equilibrium (velocity overshoot) and qusi-ballistic transport are actually dominant. For

modern MOSFETs i.e. for long channel devices inversion layer mobility is important parameter to be concern but for nano scale region dependency of drain current on mobility is less clear. The analysis of quasi-ballistic MOSFETs based on the backscattering ratio and ballistic efficiency. Equation 4.4 shows the current equation in quasi ballistic region of operation. We have to discuss details about the backscattering ratio and ballistic efficiency to analyse how quasi ballistic device current depends on stress.

$$I_{Dlin} = w\, C_{ox} \frac{v_T}{2k_B T/q} (1 - r_{lin})(v_{gs} - v_{th})V_{ds} \quad [15\text{-}17] \qquad 4.4$$

$$I_{dsat} = w\, v_{inj} \left(\frac{1-r_{sat}}{1+r_{sat}}\right) C_{ox} \left(v_g - v_{th,sat}\right) \quad [15\text{-}17] \qquad 4.5$$

$$B_{sat} = \left(\frac{1-r_{sat}}{1+r_{sat}}\right) \quad [18] \qquad 4.6$$

r_{sat}= Saturation Back scattering ratio.

B_{sat}=Ballistic Efficiency.

4.2.3.1 Carrier Backscattering in a Nano-MOSFETs

In quasi-ballistic region of operation carriers are injected from the thermally equilibrium reservoir (source) into the channel of the MOSFET. They suffer elastic and in elastic scattering in the channel region, because of this scattering few electrons also return back towards the source, so they are not taking part the current conduction. In these scattering process carriers are lose their energy. If the losses happens to be some multiple of KT-by the optical phonon emission (OPE) or by any other scattering potential than that electron have very less chance to get back the energy and exit through the source. So present day MOSFET upper limit current will be determine by the number of carrier backscatter from the channel. The backscatter carriers are not taking part in the current conduction. Out all backscatter carriers more than 80% of the carriers come from the first (KT/q) potential drop region, this region also called KT-layer. Figure 4.4 below shows the thickness of the KT-Layer (ℓ) representation [15-18]. At the edge of this layer the carrier only losses its energy by KT-eV (0.025eV).

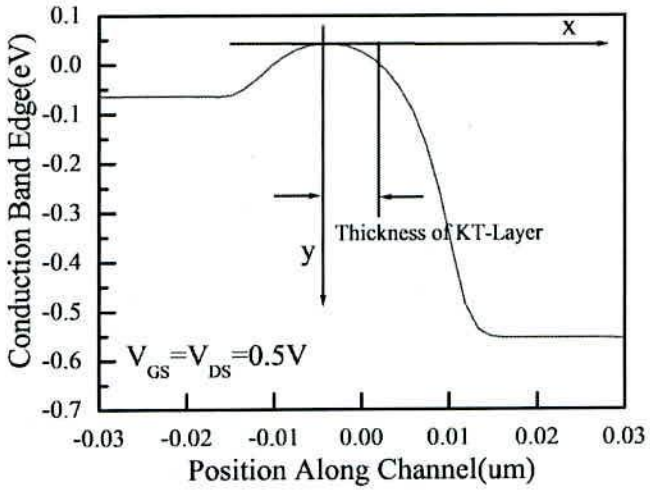


Figure 4.5: KT-Layer Thickness from Barrier Model.

From transmission point of view this KT-layer is the bottleneck region, if any how carrier moves beyond this region it will definitely exit through the drain end. This transmission mechanism is also same as that of BJT carrier transmission, figure 4.5 shows the similarity of region between BJT and MOSFETs.

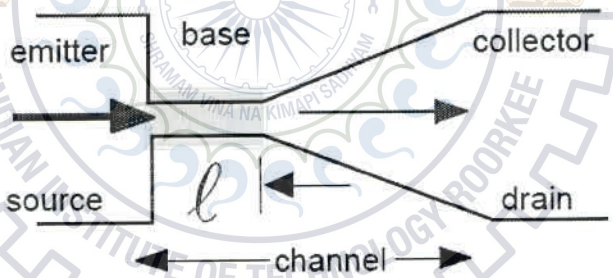


Figure 4.6: Similarity between BJT and MOSFET [16].

From figure 4.5 we can conclude that the total channel region of the MOSFTEs divided into two parts

[1] The region nearer to the bottleneck point is low field region. In these regions, longitudinal electric field is less compare to drain side.

[2] Remaining portion of the conducting channel excluding bottleneck region. Also called high field region as longitudinal electric field strength comparatively more.

The backscatter of carrier makes serious degradation in the characteristics of MOSFETs. So our focus here only in the bottle neck region, because DC-drive current basically depends on how first the carrier can move in this low field region of MOSFETs. At the drain side carrier are in off-equilibrium mode i.e. in velocity overshoot region, movement is very fast, so we should take care about the low field region only.

Back scattering ratio (r) depends on potential profile along the channel and on the scattering physics. BSR depends on the thickness of the KT-Layer. For a well fabricated MOSFETs with proper biasing condition gives KT-Layer thickness is about one MFP, from the above statement it's very clear that the transmission is quasi ballistic one around the bottleneck point.

The BSR for linear region, low applied longitudinal electric field

$$r = \frac{L}{L+\lambda_0} \quad [16] \qquad 4.7$$

The BSR for saturation region, high applied longitudinal electric field

$$r = \frac{\ell}{\ell+\lambda_0} \quad [16] \qquad 4.8$$

L = Length of Channel Region.

ℓ = KT-Layer Thickness.

λ_0 = Near Equilibrium MFP.

Only KT-Layer thickness and near equilibrium mean free path are dependent on the stress. In the later chapter of this dissertation we will discuss how these parameters are modulated by applied stress and what will be the impact on the drive current of this modulation.

Chapter-5

Result and Discussion

5.1 Device Simulation

For analysis of stress effect on the performances of planar MOSFET, we use 32nm planar MOSFET as a vehicle. The technology node of our analysis is of 32nm, it means gate length is 32nm but the effective channel length is around 18nm. Figure 5.2 shows the sentaurus simulator schematic of the NMOS with doping profile in different region.

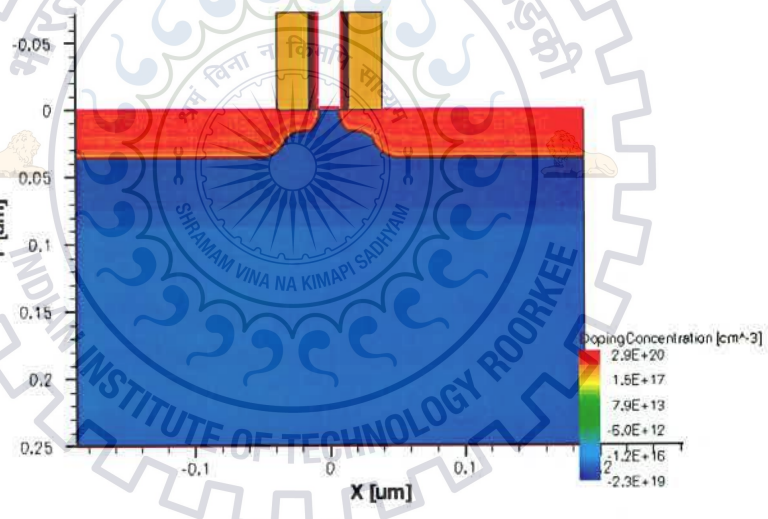


Figure 5.1: schematic cross-section of NMOS with doping concentration.

The model we use here is piezoresistive model, which helps to give details about how mobility will increases with respect to increases in stress. Piezo model includes quantum effect in the inversion layer on MOSFETs, it also explain how carrier repopulation happens in the conduction band because of non-degeneracy, which is created by the applied of stress. Another model we used here is "Deformation potential model" which is taking care about how band splitting occur at both conduction and valence band. Structural dimensions, doping profile and species are given below in a tabular format.

Table 5.1: nMOS-parameter1

PARAMETER	VALUE
Gate length	18nm
Oxide thickness	1nm

Table 5.2: nMOS-parameter2

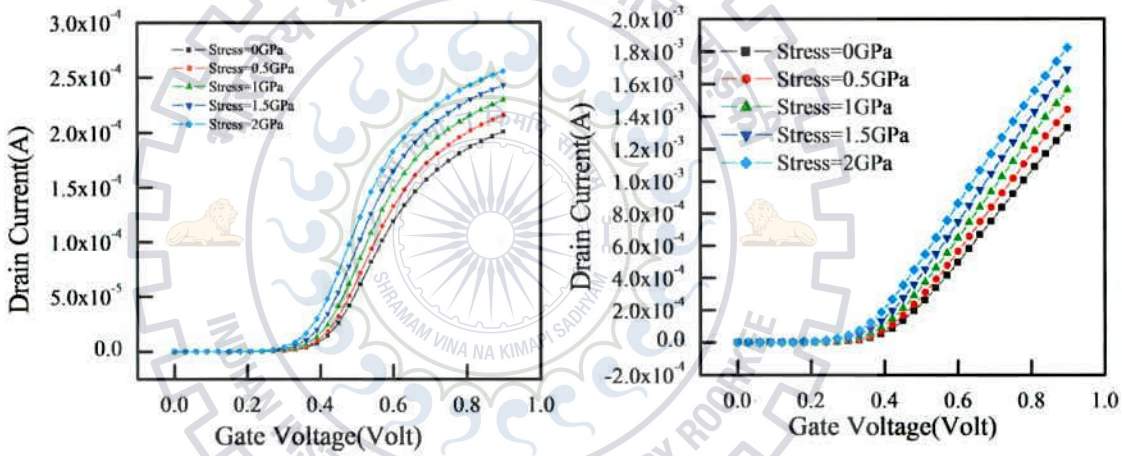
PARAMETER	VALUE
SDE Junction depth	45nm
Deep S/D Junction depth	85nm
Spacer Length	30nm
Substrate Thickness	0.25um
S/D Length	0.15um

Table 5.3: Doping Concentration and Species selection for nMOS.

PARAMETER	TYPE OF DOPING	DOPING CONCENTRATION(cm^{-3})	DOPANT
Channel doping along depth.	Retrograde well.	8e18	Indium (In)
SDE doping	Gaussian (peak at surface, factor=0.4)	1e20	Arsenic (As)
Deep S/D doping	Gaussian (peak at surface, factor=0.6)	2e20	Arsenic (As)

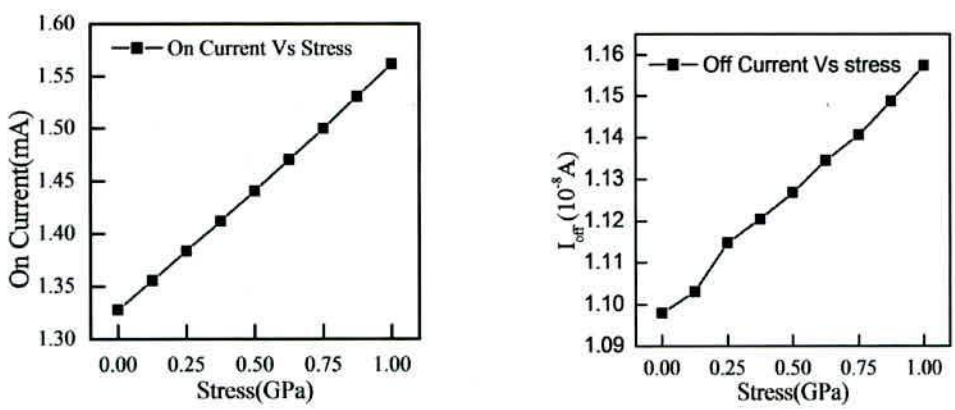
5.2 Current Voltage Characteristics

Figure 5.2 shows the current voltage characteristics of my device. From figure, it is conclude that as applied stress increases device current also increases. The effect of stress on "on current" and "off current" also observed here. "On current" and "off current" both increases with stress but the rate of increment of "on current" is more as compared to "off current" (see figure 5.3c). The reason is very simple, that "off current" is diffusion-dominated transport. As it is diffusion dominated transport increment of mobility has less effect on enhancement of transport in that region. However, the "on current" is purely drift dominated one so enhancement of mobility is fully affect on its performances. Threshold voltage changes are also observe here but the change is very less, so we can assume as it a constant one for our analysis purpose.

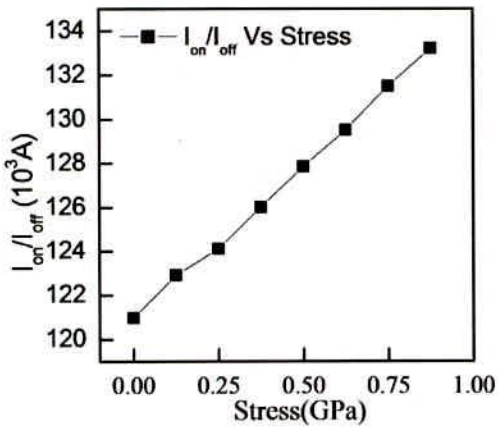


(a) Linear characteristics. (b) Saturation Characteristics

Figure 5.2: Current Voltage Characteristics in Linear and Saturation Region.



(a) On current Vs Stress. (b) off current Vs Stress.

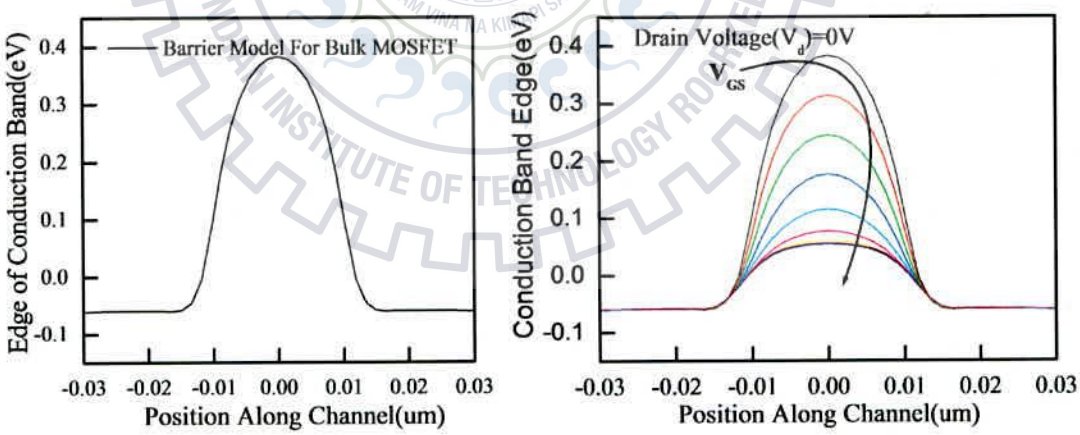


(c) I_{on}/I_{off} Vs Stress.

Figure 5.3: on current, off current and their ratios variation with respect to stress.

5.3 Barrier Modulation process

Previous chapter we already discuss what exactly the barrier for electron when it move from left contact to the right. Here we show some simulation result how these barriers can be modulate by applying different voltages and by applying stress also.



(a) (b)

Figure 5.4: (a) Barrier faced by Carrier when no Bias is applied. (b) Modulation of barrier with variation of gate voltage.

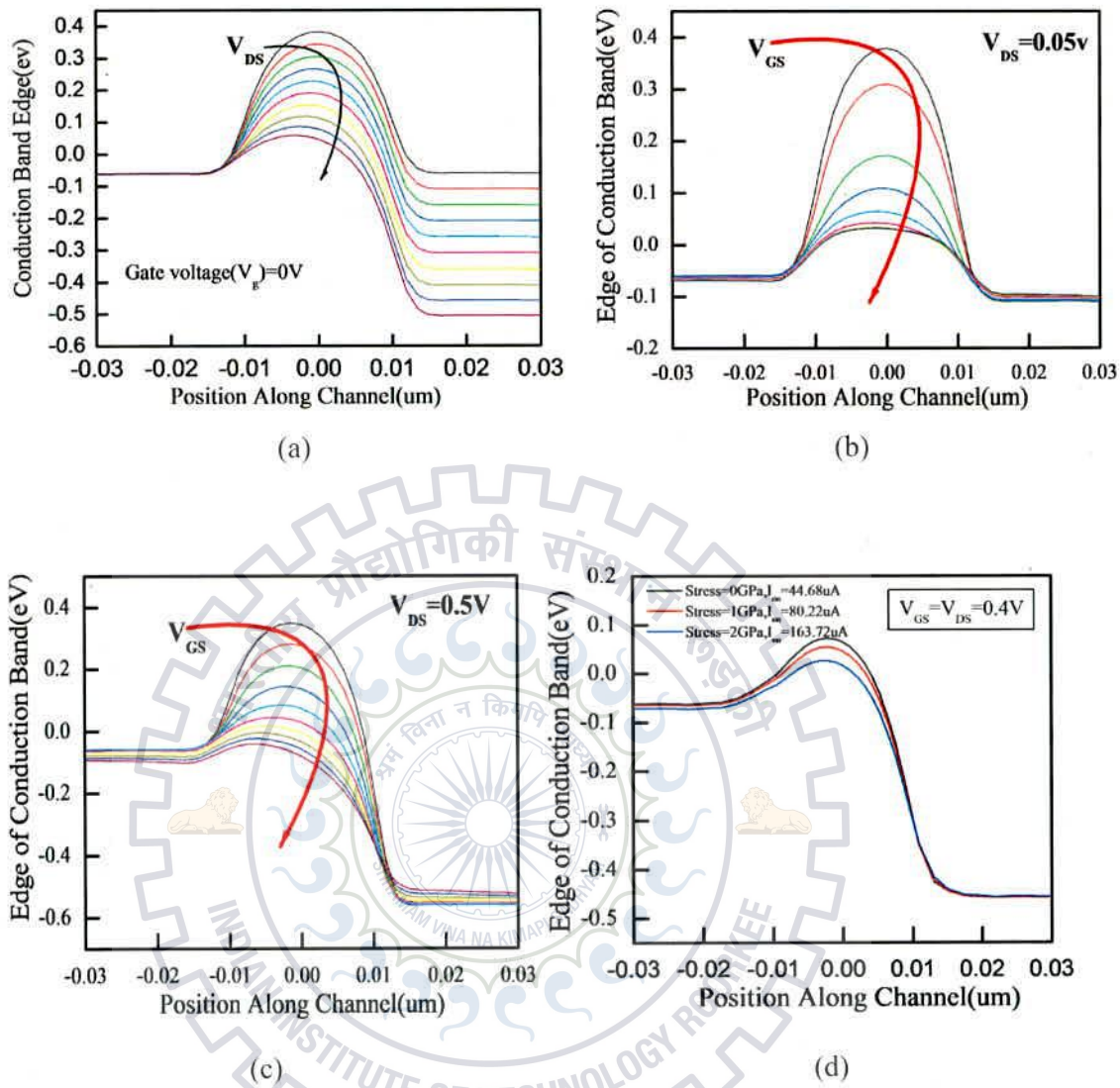
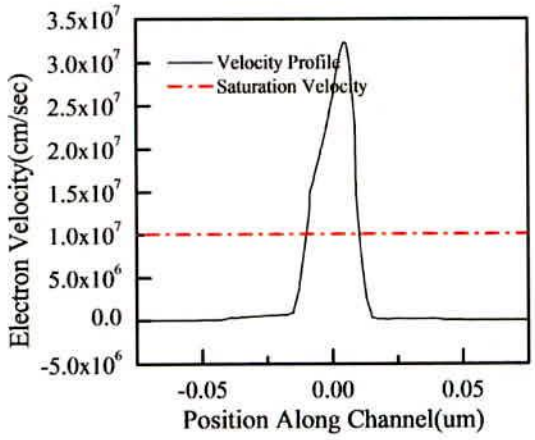


Figure 5.5: Barrier modulation in different condition. (a) V_{GS}=0V (fixed), V_{DS} changes from 0V to 0.45V. (b) V_{DS}=50mv (fixed), V_{GS} changes from 0V to 0.9V. (c) V_{DS}=0.5v (fixed), V_{GS} changes from 0V to 0.9V. (d) V_{GS}=V_{DS}=0.4V (fixed), applied stress changes from 0GPa to 2GPa.

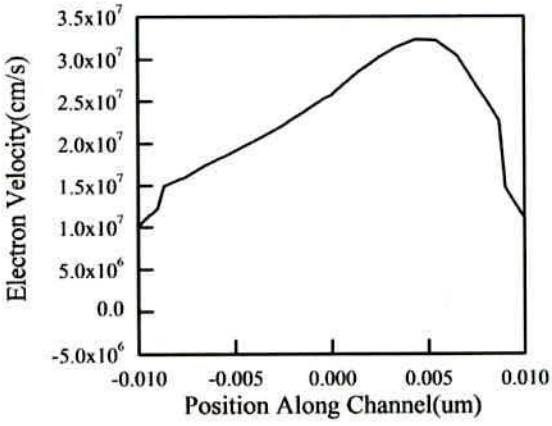
Figure 5.5d shows clearly that the conduction band comes down along the E-axis because of the applied tensile stress. As previously we discussed valence band goes up if tensile stress is apply to it. Therefore, from these above two statements we get that the band gap of Si reduced because of uniaxial tensile stress.

5.4 Carrier Velocity Profile Modulation

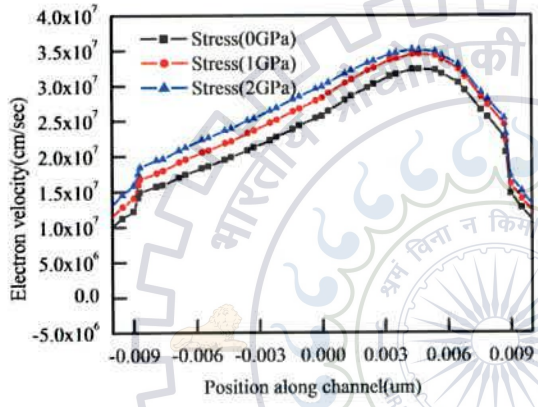
Carrier velocity (injection velocity) in channel region is an important parameter to be analysing from ballistic transport point of view. Here in figure 5.6a shows the average velocity of carrier at different point from source to drain. Near source and drain carrier



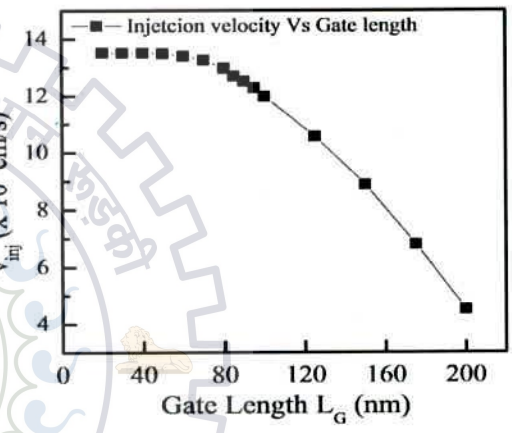
(a)



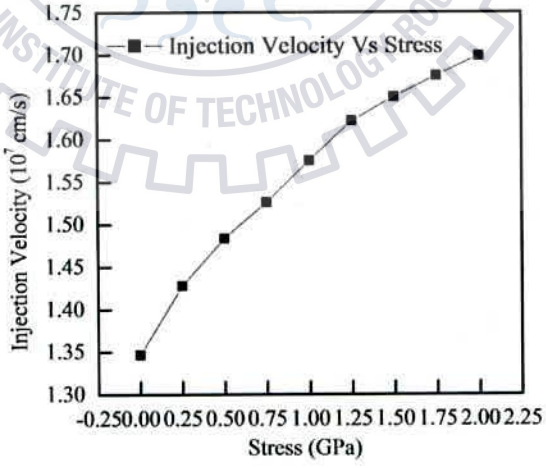
(b)



(c)



(d)



(e).

Figure 5.6: (a) Velocity Profile of Carrier, (b) Magnified portion of the Velocity overshoot region, (c) Velocity Profile Modulation with Stress, (d) Injection Velocity Changes with Gate Length, (e) Injection Velocity Changes With Stress for 32nm Gate Length.

velocity is very low because the doping concentration in that region is very high(order of $10^{20}cm^3$). In the channel region, velocity is very high and close to the drain region, velocity of carrier goes to overshoot region, which mean the velocity is more than that of the saturation velocity.

Figure 5.6b shows the magnified portion of the velocity overshoot region. Figure 5.6c shows how velocity of carrier in channel region modulates because of applied stress, here we apply uniaxial tensile stress. We also simulate device of different gate length and take the result for injection velocity for different case (see figure 5.6d). From the simulated results it is very clear that injection velocity of carrier increases with decrease in gate length. As we go down below 45nm technology, node it goes to saturate at some value around $1.38*10^6$cm/S, which is equal to the unidirectional thermal velocity (see equation 5.1).

Figure 5.6e shows the modulation of injection velocity with variation of uniaxial tensile stress. My device is operating in the velocity saturate region and its injection velocity is equal to the unidirectional thermal velocity. Injection velocity is inversely proportional to the square root of the conductive effective mass. As we already, discuss in chapter 3 how conductive effective mass variation happens with uniaxial stress. We prove there theoretically that the effective mass decreases with increases in stress, this result clear about that theoretical proof. But for exact proof of increment of conductive effective mass with respect to the stress we have to go for more complicated simulation like Monte carlo simulation.

$$V_{inj} = \sqrt{\frac{2k_B T}{\pi m^*}} = V_T \text{ [31]} \qquad 5.1$$

5.5 Mobility Variation with Stress

Figure 5.7a shows the mobility profile from source to drain and the variation of the profile with variation of uniaxial tensile stress along the channel. Mobility of carrier near the source and drain is very low (see figure 5.7a) and in the channel region its value is more than that of the source drain region. Basically our major concern is the mobility along the channel region of the MOSFET, because this region contains limited number of channel for transmission of the carrier. Number of transmission channel in the inversion region of MOSFETs is thousand times less (approximately) than that of the channel presents in the source drain region. For the above said reason we basically focus more on the channel mobility instead of total mobility throughout its journey. So we calculate the average mobility

in the channel region for different gate to source and drain to source voltage and simulate for its variation with uniaxial tensile stress.

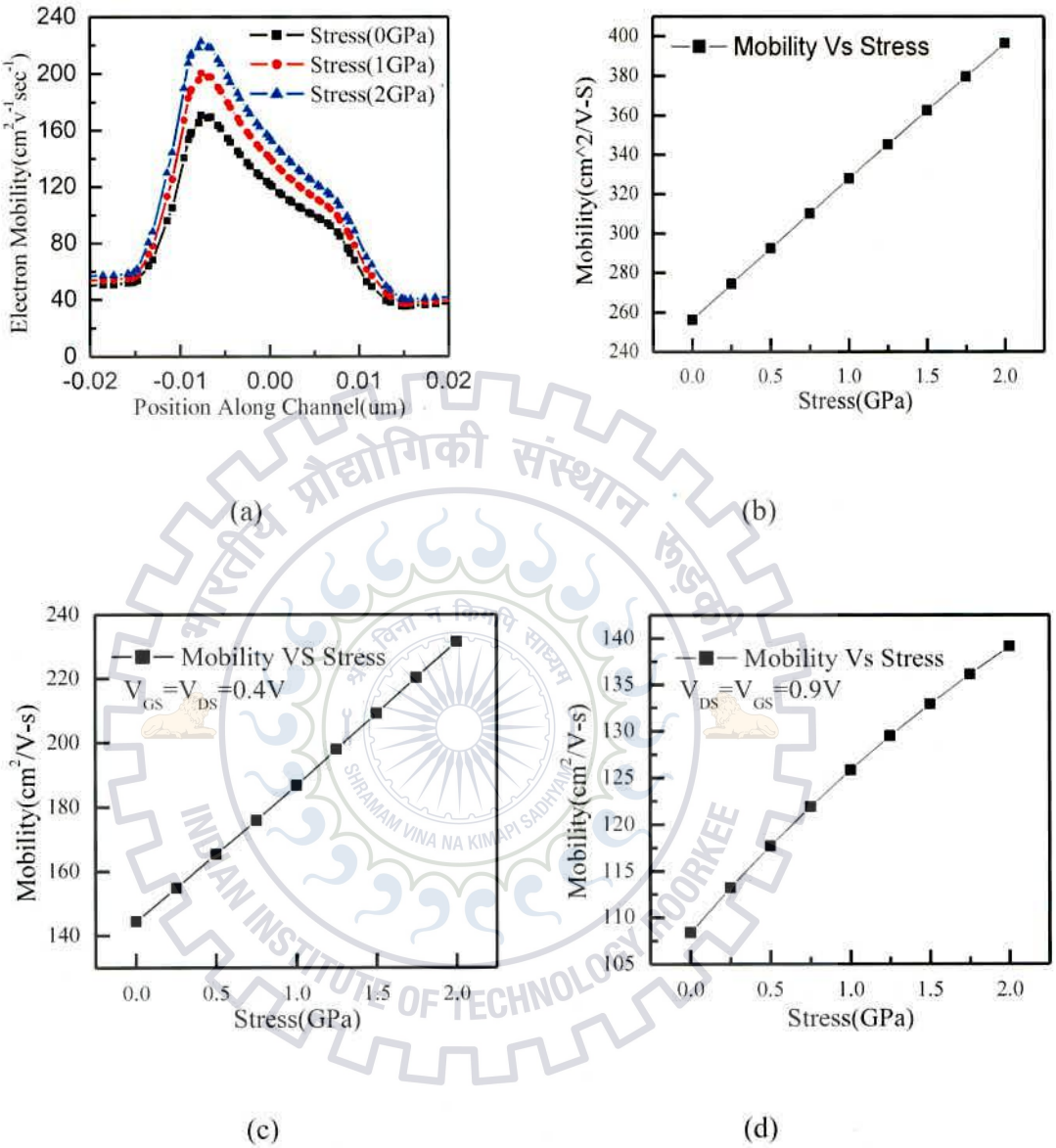


Figure 5.7: (a) Mobility profile from source to drain and its variation with respect to stress. (b) Average channel mobility variation wrt stress (V_{DS}=50mv). (c) Average channel mobility variation wrt stress (V_{DS}=0.4v). (d) Average channel mobility variation wrt stress (V_{DS}=0.9v).

Figure 5.7b,c,d shows the variation of average carrier mobility with stress for different applied voltages.

5.6 Carrier Back Scattering Effect

Here we are considering only the carriers which are backscatter from channel to source of MOSFETs and neglecting the effect of backscatter from drain to source. Expression for carrier backscattering from channel is given in equation 4.8, we can rearrange that equation and write as shown below.

$$r = \frac{1}{1+{}^{\lambda_0}/_{\ell}} \qquad 5.2$$

ℓ = KT-Layer Thickness.

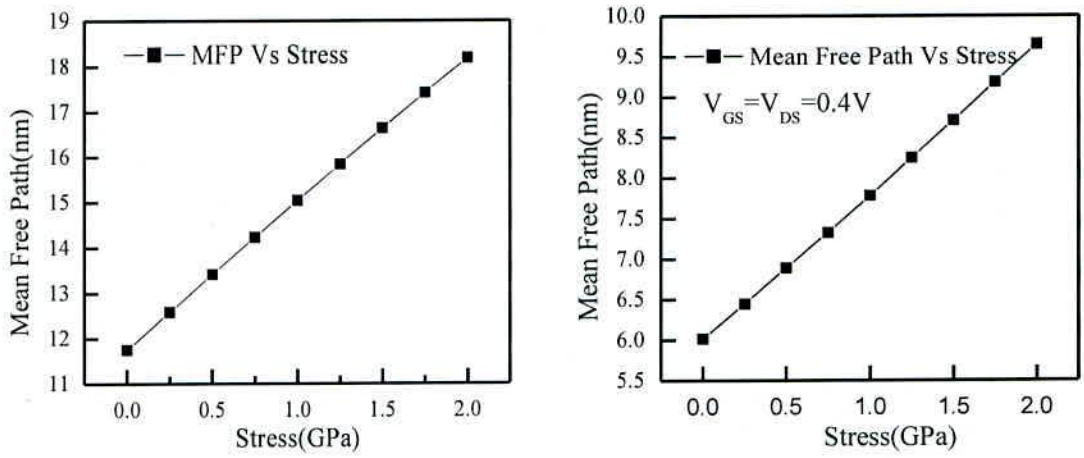
λ_0 = Near Equilibrium MFP.

For analysing the effect of stress on carrier backscattering first of all we have to analyse, how these above two parameter changes with stress. The expression for mean free path is given in equation 5.3.

$$\lambda_0 = \frac{2D_n}{V_T} = \frac{2\mu_n({}^{kT}/_{q})}{V_T}. \quad [31] \qquad 5.3$$

Where V_T= Unidirectional thermal velocity (see equation 5.1)

From equation 5.3 it is very clear that two parameter dependent on stress, these are mobility of electron and unidirectional thermal velocity. For the timing we are assuming that the unidirectional thermal velocity as constant because its variation with stress is small as compare to the mobility. Mobility of carrier increases with stress so mean free path too. Figure 5.8 shows the stress versus mobility characteristics. The mean free path of carrier is around 5 to 6 nm, where the channel region length is approximately 18nm, which clear that my device is working in quasi-ballistic region.



(a) (b)

Figure 5.8: (a) Mean free path versus stress ($V_{GS}=V_{DS}=50mv$). (b) Mean free path versus stress ($V_{GS}=V_{DS}=0.4v$).

Previously we discussed how barrier is modulated with stress, as barrier height is modulated so the KT- layer also modulates with stress. Figure 5.10 shows the simulation results for KT-layer variation with respect to stress.

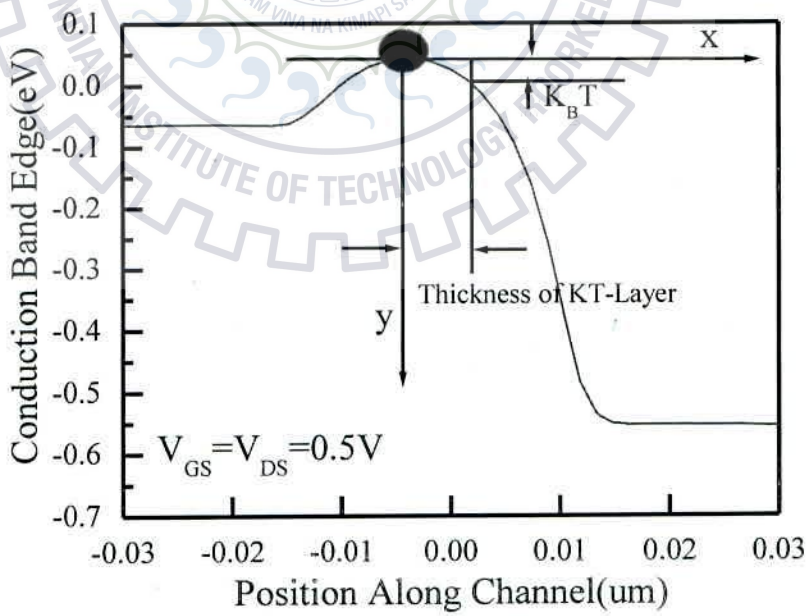


Figure 5.9: KT- Layer thickness representation.

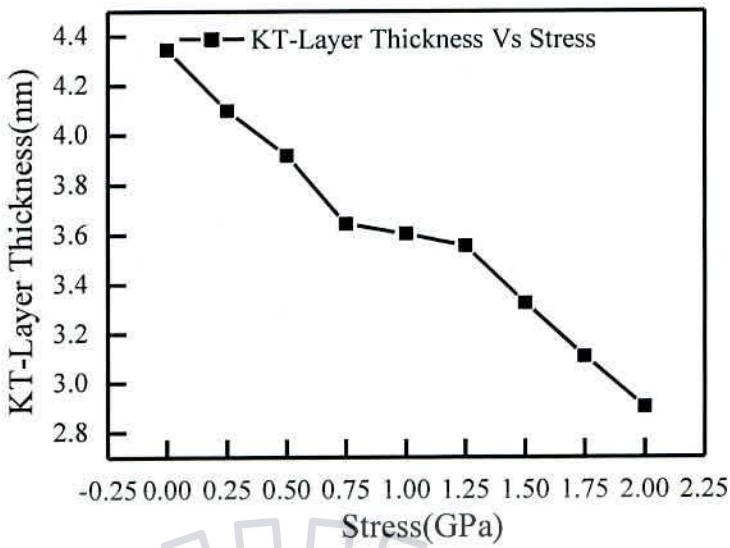
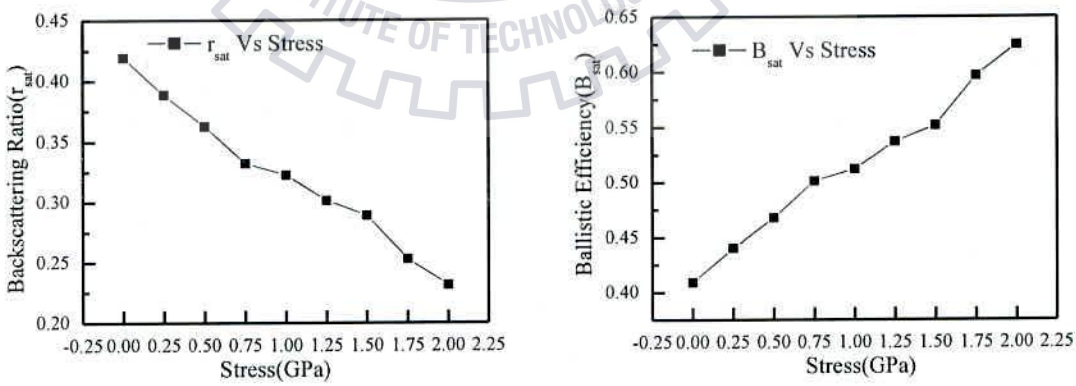


Figure 5.10: KT-layer Thickness Variation wrt Stress.

From above results we concluded that mean free path of backscattering increases with stress and KT-layer thickness decreases with stress, so the ratio (λ_0/ℓ) is increases with stress. Backscattering ratio is inversely related to the ($1+\lambda_0/\ell$), so it decreases with increases with uniaxial tensile stress (see figure 5.11). Backscattering actually represent the fraction of carrier come back from channel region to source because of scattering in that region.



(a) (b)

Figure 5.11: (a) Backscattering Ratio Vs Stress (b) Ballistic Efficiency Vs Stress.

Chapter-6

Summary and Conclusion

Strained Si (SSi) technology is essential to achieve performance related task for the state-of-the-art of the CMOS technology flow. This technology is use as a vector to satisfy the Moore's prediction starting from 90nm technology node. Strain will continue to scale well into future logic technology generations as the MOSFET enters the ballistic regime. My device is operating in quasi-ballistic region, which we demonstrate here, as the mean free path of carrier is comparable to the distance between the contacts. The empirical mobility model, which was there, related to stress, we prove here theoretically and physically, our simulation suit with it.

In quasi-ballistic region device current is depends on channel backscattering ratio, ballistic efficiency and injection velocity. We have shown here how these parameters are modulated with stress, basically uniaxial tensile stress. The impact of uniaxial stress on channel backscattering is demonstrated here and we outlined that it is decreases with increases in stress which conclude that the number of carrier reflect back from channel to source due to scattering decreases with stress, which ultimately increases the device current.

We have shown here the injection velocity of the carrier for different gate length keeping all other parameter remains constant. As the gate length decreases injection velocity increases and it will saturate to unidirectional thermal velocity at around 45nm technology node. Stress has also modulate to unidirectional thermal velocity as it is depends on conductivity effective mass, which decrease with stress, so injection velocity increases with stress. The theoretical background behind the conductive effective mass increment with stress was discussed. Therefore, strain engineering is a novel technique to enhance the device performance for state-of-the-art of CMOS technology flow.

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