STUDY AND PHYSICS BASED MODELLING OF TFET

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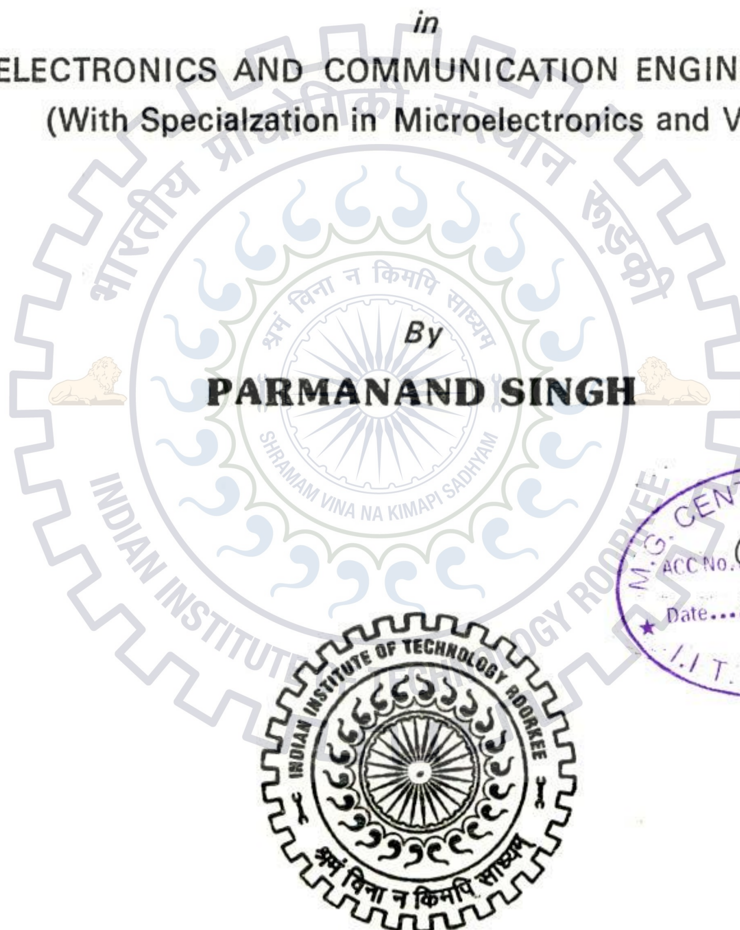

By

PARMANAND SINGH

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE - 247 667 (INDIA)

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ABSTRACT:

Demand for low power operating devices imposed by the mobile, portable electronics and the current chip market has been the motivational source for the researchers for many years. Although circuit and system engineers have put their efforts to reduce the power, but still the fundamental limit in the overall energy efficiency of a system is still rooted in the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) physics i.e. an injection of thermally distributed carriers which does not allow the switching characteristics better than 60 mV/dec at room temperature which puts a constraint over the scaling of supply voltage Vdd and lowest energy consumed per digital operation with current CMOS technology.

In this work, Tunnel-Field-Effect-Transistor (TFET) based on gate induced band-to-band tunneling is studied as an alternative device to overcome the physical limit of the subthreshold slope in MOSFETs which permit the scaling of supply voltage (VDD) and lower threshold (VTH) operation. Following introducing the working principle of the TFET, the calibrated Technology Computer Aided Design (TCAD) simulations are used to study the behavior of the carriers inside the channel to get an overview of the deep physics associated with it. After filtering the existing analytical models for TFET on-current, various areas are explored which required to be improved. As similar to subthreshold current in MOSFETs, the study of leakage current called "*sub onset current*" (sub onset is the point where the overlapping of valence and conduction bands starts) in TFET is also important from the digital application point of view. Keeping this in mind, a SRH generation and recombination based model is proposed for the physical modeling of sub onset current.

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1 INTRODUCTION OF TUNNEL FIELD EFFECT TRANSISTOR:

1.1 Introduction:

As MOSFETS reach nanometer regime, power consumption becomes a major challenge for further scaling. The continued reduction of the MOSFET size is leading to an increased leakage current due to short channel effects, such as Drain Induced Barrier Lowering (DIBL), and the power supply voltage cannot be reduced any further because of the subthreshold slope being limited to 60 mV/decade at room temperature. The latest progress of integrated circuit (IC) technology and continued miniaturization of transistor dimensions yield greater circuit density and functionality at lower cost per function over previously unimaginable capabilities and computing power [1].

As transistor scaling has provided for enhanced performance, it has also resulted in increased in power density of the chip. The fundamental reason for the rapid increase in the power per unit area is that the operating supply voltage (VDD) which is used to drive the transistors has not scaled proportionately with transistor dimensions [2]. The main cause for the reduction in VDD scaling is due to the non-scalability of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) threshold voltage (V_{TH}, the voltage which is applied at the gate terminal to turns the transistor on and off). Also the leakage current in off state (I_{OFF}) of the MOSFET is non-zero because the MOSFET is not an ideal switch and hence it dissipates some power even when it is supposed to be off.

Parallel computing also has been employed in microprocessor design to achieve the improvements in system performance without increasing operating speed of the transistor [6]. By operating multiple cores in parallel at reduced clock speed, parallelism allows the reduction in energy per operation while maintaining the system performance which is otherwise limited when each device is operated at an energy level which is defined by its device-level constraints [7].

For a significant reduction in V_{TH} and V_{DD}, a new device with steeper switching characteristics is required. Hence at a significantly lower voltage, the new device can required I_{ON} current for a given I_{OFF} specification which would result in reduced dynamic energy as compared to MOSFET. Also this new device could achieve much lower I_{OFF} and steeper

switching which would yield a required reduction in leakage power. This leads to an overall improvement in in the energy efficiency.

In this view, the exploration of alternative devices which possibly outperform the MOSFET at these nanometer dimensions and energy limits is required. A promising alternative for the MOSFET, which does not suffer from these limitations, is the tunneling field-effect transistor (TFET). Tunnel Field Effect Transistor (TFET) is an emerging ultra-low power transistor that can, in principle, exhibit <60mV/dec slope. TFETs with a subthreshold slope lower than 60 mV/decade have already been demonstrated [2] and due to their built in tunnel barrier, Si TFETs are expected to exhibit low off currents for channel lengths down to 10 nm [3].

1.2 Literature Survey:

Stuetzer [4] in 1952 was the first who make investigation of transistors which contain the basic elements of the TFET also describing the Esaki's discovery of interband tunneling in p^+–n^+ junction [5]. He showed the ambipolar behavior of current–voltage characteristics, in the lateral gate field of a Ge semiconductor based p–n junction. He also showed the dependence of the tunneling in the transistor characteristic on the placement of gate with respect to the p–n junction. The gated p-i-n structure, consisting of a p^+- and an n^+-doped semiconducting region on each side of a gated intrinsic channel region, was first proposed by Quinn *et al.* in 1978 [6]. The proposed device geometry, the structure of the lateral Tunnel FET, was capable for measurement of splitting of subband effects and the transport properties of tunneling among the highly doped bulk source and channel surface. Later Banerjee *et al.* [7] had studied the behavior and physics of three-terminal silicon Tunnel Field Effect Transistor, and Takeda *et al.* [8] had explored the various aspects which are specifically related to the scaling down of the TFET structure.

Leburton et al. [9] proposed the first vertical TFET aiming to create a high-speed tunnel transistor in which he used the gate field to control the negative differential resistance (NDR) of the transistor. Later in 1992, Baba [10] proposed a lateral Tunnel FET device structure of Quinn and also to use the field of gate to control the NDR. Baba [24] also fabricated the TFETs called surface tunnel transistors using group III–V semiconducting materials and observed the room temperature NDR in STT with Uemura in GaAs [11] in 1994. In 1995, researchers Reddick and

Amaratunga [25] reported their experiments on silicon based surface tunnel field effect transistors. One year later in 1996, a 'forward-biased' three-terminal silicon tunneling field effect transistor device as a post-CMOS switch candidate for the future was proposed by Koga and Toriumi [12]. In 2000, Hansch *et al.* [27] published his experimental data based on reverse-biased vertical silicon based Tunnel FET which was having a highly doped boron as a delta-layer which was fabricated by MBE. In 2004 Wang [4], Bhuwalka [5], and Appenzeller [6] discussed the low subthreshold swing in TFET. Zhang [34] had derived an analytic expression to show how the gate controls both the internal field at the tunnel junction and the band-to-band overlapping, explaining the room temperature swing less than 60-mV/decade. Aydin *et al.* in 2004 [28] processed that the lateral Tunnel Field Effect Transistors with silicon-on-insulator (SOI), which in principle was closer to TFET devices without an intrinsic channel region. To increase the speed there is a requirement of reduction in gate capacitance which is supported by gate over a p–n junction structure. Interest in Tunnel FETs has been raised continuously over the last few years. Recently, TFETs are fabricated in various semi conducting material systems (carbon, silicon, SiGe and group III–V materials) [29–33] which has emerged experimentally as the most promising candidates for the switching devices with very low standby leakage power and less than 0.5 V logic operating supply voltage.

Wang [13] has explained that the TFET current is composed of two components consisting the carriers which are tunneling from the source region to the channel at the source-channel interface while the other component consists of the carriers which are tunneling in the source itself from the bulk region to the region very near to the gate oxide and source interface. The Gate-over-source TFET structure (also known as line TFET [14]) where the carriers are tunneling from source to the region overlapped by the gate, has higher tunneling junction cross section area as well as it shows a better subthreshold slope than a conventional TFET was introduced by Vandenberghe and G. Groeseneken in 2008. They use the Kene generation rate as the generation term which is integrated over the entire volume at the junction but also neglected the leakage current. They have also modeled the tunnel current for the conventional TFET structure.

1.3 Dissertation Outline:

This dissertation aims to address the physical study and challenges in modeling associated with Si based TFET technology in achieving overall view related to OFF current. Results based on simulation shows the carrier's behavior dependency on biasing and various mechanisms for the conduction of the current in tunnel transistor. The calibrated BTBT and recombination models are employed in Technology Computer Aided Design (TCAD) to gain deep understanding of the device physics at the device level. An analytical model based on recombination and generation of carriers in the reversed biased junction is also presented to explain the sub onset (off) current in the TFET.

Chapter 2 introduces the structural and simulation environment information related to TFET. The differences in the device structure and the carrier injection mechanism with respect to a MOSFET will be explained along with an overview of the BTBT model used in TCAD analysis is provided. The basic difference between physics of BTBT based on Kane's generation rate and WKB method of probability is summarized, followed by discussion on point vs. line tunneling.

Chapter 3 presents the study of the tunnel transistor based on the physics related to the carriers behavior and their dependency on the gate and drain voltages. The importance of SRH generation and recombination is presented in this chapter. The saturation of the current is also demonstrated on the basis of carrier's enhancement in the channel region at different biasing conditions. A voltage is also defined called onset voltage at which the current dominating component switches from SRH generation and recombination to tunneling component.

Chapter 4 addresses the limitations associated with the present reported analytical models and how these limitations can be improved is also shown. The impact of inversion width is explained and a method is proposed to include it in the present tunneling models. The importance of off current i.e. sub onset current and an analytical expression also formulated to complete the study of the sub onset current. Modeled and simulated results are presented and discussed and also the closeness of this model with the experimental results is also shown.

Chapter 5 summarizes the contributions to this work and includes the future research directions.

2 TUNNEL FIELD EFFECT TRANSISTOR DESIGN AND OPERATION:

2.1 Introduction to TFET structures:

The TFET is generalized as a gated reverse biased *p-i-n* diode. Figure 2.1 (a) illustrates the structure of gate over source Si TFET. The simulated devices has a total length of 125 nm, composed of a *p*+ source (50 nm), an intrinsic channel (50 nm), and *n*+ drain (50 nm) contact along with a gate length of 25 nm. The acceptor (donor) concentration in the source (drain) extension amounts to 1e20 cm^{-3} (1e18 cm^{-3}). It also consist a dielectric layer of thickness 2.5 nm (material having a dielectric constant 25). The doping concentration is larger in the source than in the drain to create large electric fields at the source-channel interface and increase the tunneling probability while maintaining a lower field and tunneling probability at drain-channel junction.

The same structure is also employed for the analysis of point (conventional) TFET figure 2.1 (b). The only difference in the structure is that the gate is now completely lying over the channel region without any overlap of drain and source. Also the gate length is 50nm.

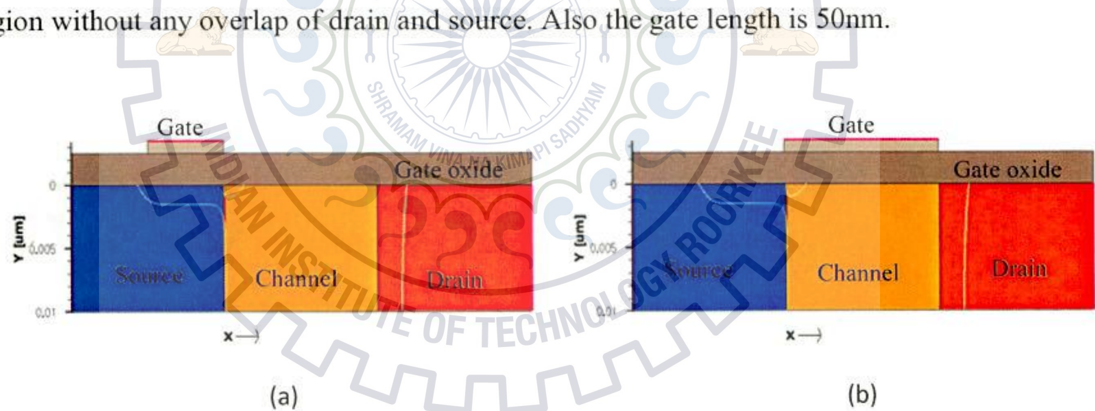

Figure 2.1 Structure and doping concentration of (a) Line TFET and (b) point TFET.

There are two different tunneling modes in designing of a TFET based on BTBT that can be employed depending on the device structure. One is lateral tunneling in which the electrons are injected (tunneled) from the source to the channel region majorly in a direction parallel to the Semiconductor-gate oxide interface (referred to as "point" tunneling in [15]). This is the basic mode of operation for a conventional TFET (Fig. 2.2(a) and (c)). The source region should be

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heavily doped to achieve high tunneling rate so that the energy band bending of the source to channel junction is steep (Fig. 2.2(c)). The source region and gate edge should be aligned so that no reduction in the abruptness of the energy band profile would result in degraded BTBT although gate to source underlap would also result in a degraded tunneling rate.

When compared to the standard CMOS process flow, the point TFET offers an advantage in terms of device fabrication i.e. only an additional step is required for opposite-dopant ion implantation in source and drain regions. Also in order to attain large energy band bending, the doping gradient from the source to the channel should be reduced. Another basic limitation in the point TFET is that the tunneling area is fundamentally small, since it is localized by the inversion layer thickness which is typically 2~3 nm in the *on*-state.

Other type of BTBT transistor can be employed as vertical tunneling devices in which the electrons can tunnel from source region largely in the direction perpendicular to the semiconductor/gate-oxide interface with in the source (Fig. 2.2(b) and (d)) (called as "line" tunneling in [15]). The existence of a sufficient overlap between gate and source region (LOV), allows the electrons to tunnel from within the source to the region inverted below the gate in the source itself (Fig. 2.2 (d)). The doping of the source region should be moderate enough to allow the sufficient band bending within the source region and also the thickness of the source should be large than the depletion width (*i.e.* ~15 nm for moderately doped Ge). The on current in case of vertical TFET is large as compared to the conventional TFET as the tunneling area can be determined by the gate to source overlap region (LOV) [23]. Also subthreshold swing is very less sensitive to the doping gradient across the source to channel junction [14] since the tunneling is taking place within the source region.

2.2 TFET vs. MOSFET:

Fig. 2.1(a) and (b) show the cross-sectional schematics view of an n-channel MOSFET and TFET, respectively. The only difference associated with the structure of TFET is the oppositely doped source and drain regions (p^+-i-n^+) while symmetrically doped source and drain regions (n^+-p-n^+) in a MOSFET [16].

The nomenclatures for the terminal voltages (source, drain, and gate) and the corresponding biasing scheme to define *on* ($V_{GS} = V_{DS} = V_{DD}$) and *off*-state (V_{GS} = 0 V, $V_{DS} = V_{DD}$) remain

identical for both the devices. This difference in terms of the structure associated with the two devices results in a quantitative difference in terms of the carrier injection mechanism and its operating physics.

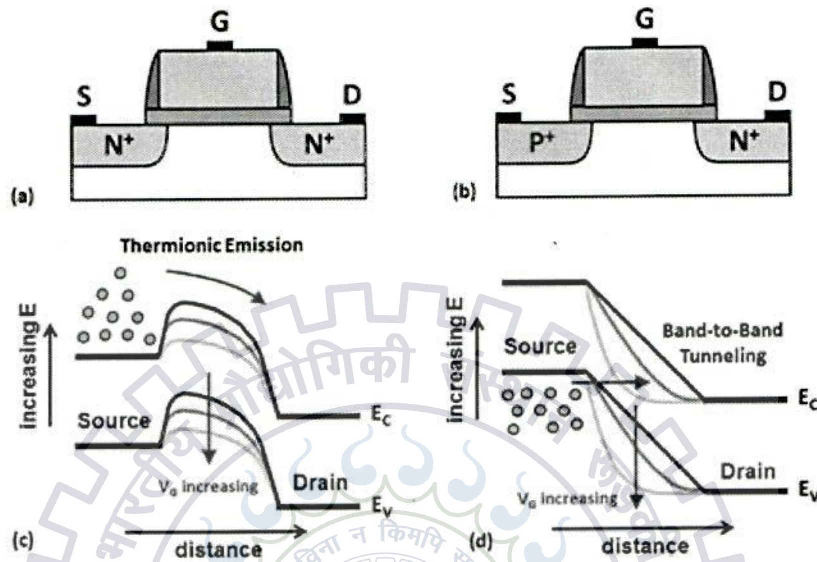

Figure 2.2 Schematic cross-sections for n-channel (a) MOSFET and (b) TFET. (c) The operation of a MOSFET depends on gate-voltage (VG) modulation of the channel potential for the injection of carriers over the barrier height from the source into the channel region through a process called thermionic emission. (d) The operation of a TFET is also based on gate-voltage modulation of the channel potential, but the carriers are injected into the channel through the potential barrier via band-to-band tunneling or Zener tunneling.

The operation of a MOSFET is based on gate-voltage modulation of the channel potential for the injection of carriers from the source region into the channel region through a process called thermionic emission (Fig. 2.2 (c)). These carriers (electrons for an n-channel and holes for a p-channel MOSFET) are thermally distributed in the source region of the device according to the Boltzmann distribution and the resulting current can be expressed as:

$$I_{Thermionic} \approx exp\left[\frac{V_{GS}}{nV_T}\right] \tag{2.1}$$

In the *off*-state, the potential barrier seen by the carriers to be injected from the source region is large, and the resulting current (*off*-state leakage, I_{OFF}) is small (Fig. 2.2 (c)). Note that this current is not zero (in contrast to an ideal switch), since the thermal (Boltzmann or exponential) distribution of carriers still permit a finite number of carriers to be injected over the large potential barrier.

In the *on*-state, the gate voltage lowers channel potential barrier, and results in an exponential carrier injection from the source region into the channel (hence exponential current modulation) (Fig. 2.2 (c)). The thermal (Boltzmann) distribution of mobile charge carriers in the source region will ultimately defines how steeply a MOSFET can switch from *on* to *off*-state which is limited to 60 mV/dec at room temperature i.e. subthreshold slope (S):

$$S = \left[\frac{\partial logI_D}{\partial logV_G}\right]^{-1} = \frac{\partial V_G}{\partial \varphi_s}\frac{\partial \varphi_s}{\partial logI_D} = \left(1 + \frac{C_{DEP}}{C_{OX}}\right)\left(\frac{kT}{q}ln10\right) \geq \left(\frac{kT}{q}ln10\right) \qquad (2.2)$$

The subthreshold swing is expected to degrade with advance in technology nodes due to associated problems (*i.e.* short channel effect) with scaling down the transistors to extremely small dimensions which further prevent the reduction of the threshold and supply voltages.

The operation of a TFET also relies on gate-voltage modulation of the channel potential for the injection of carriers (electrons for an n-channel and holes for a p-channel MOSFET) from the source region into the channel region. However, in contrast to an injection *over* the potential barrier (*i.e.* thermionic emission) in a MOSFET, TFET uses the gate voltage to modulate the width of tunnel barrier instead of height of the potential barrier and hence carriers are injected into the channel *through* the potential barrier via a process called band-to-band tunneling (BTBT) or Zener tunneling (Fig. 2.2 (d)) [17]. The main advantage associated with BTBT is that the energy band gap (of magnitude E_g) cuts off the Boltzmann "tail" of the electrons in the p-type source region (holes for the n-type source region) (Fig. 2.2 (d)) [11-12] and it behaves as if there is a band pass filter which allows the carriers to tunnel across the barrier. Also the indirect tunneling is based on electron-phonon interaction for the change in momentum from Γ-valley maximum to X-valley minimum. Although phonon occupation is determined by Bose-Einstein statistics and the number of phonons is temperature sensitive but indirect tunneling can also

occur even the phonon occupation is zero due to phonon emission by tunneling particle and for this reason indirect tunneling is independent of temperature. This lack of thermal ('kT') dependence permits sharper than 60 mV/dec turn-on characteristics at room temperature, when the conduction band of the channel overlaps with the valence band of the source region. The resulting tunneling current can be expressed as (Kane's expression) [17]:

$$I_{BTBT} \approx A\varepsilon^2 exp\left(-\frac{B}{\varepsilon}\right) \tag{2.3}$$

where A and B are material dependent parameters. When a TFET is in the *off*-state, the p-i-n structure of a TFET is reverse-biased and hence the diode leakage current comprises the dominant source of I_{OFF}, which is significantly smaller than the MOSFET I_{OFF}.

2.3 TCAD Tools Overview

An overview of the Sentaurus TCAD [18] tool suite:-

I. Sentaurus Workbench

Sentaurus Workbench is the primary graphical front end that integrates Sentaurus simulation programs into one environment. Its intuitive graphical user interface is used to design, organize, and run simulations for semiconductor research and manufacturing. Simulations are comprehensively organized into projects. A simulation flow typically consists of several tools, such as the process simulator Sentaurus Process, the meshing tool Mesh, the device simulator Sentaurus Device, and the plotting and analysis tool Inspect. Sentaurus Workbench automatically manages the information flow from one tool to another. This includes preprocessing of user input files, parameterizing projects, setting up and executing tool instances, and visualizing the results. Sentaurus Workbench allows users to define parameters and variables to run comprehensive parametric analyses. The use of mathematical and logical expressions serves to pre-process the simulation input dynamically. The resulting data can be used with statistical and spreadsheet software.

II. Sentaurus Structure Editor

Sentaurus Structure Editor is a 2D and 3D device editor, and 3D process emulator. It has three distinct operational modes: 2D structure editing, 3D structure editing, and 3D process emulation. Geometric and process emulation operations can be mixed freely. From the graphical user interface (GUI), 2D and 3D device models are created geometrically using 2D or 3D primitives such as rectangles, polygons, cuboids, cylinders, and spheres. Three-dimensional regions can also be created by simple extrusion of 2D objects or by sweeping 2D objects along a path. In process emulation mode (Procem), Sentaurus Structure Editor translates processing steps, such as etching and deposition, into geometric operations. Sentaurus Structure Editor offers state-of-the-art visualization. Structures are displayed as they are created and powerful view filters make it possible to select only a subset of regions or make certain regions transparent. Doping profiles and meshing strategies are defined interactively. Placements are visualized as semitransparent boxes for easy verification. All doping and meshing options of the mesh generation tools Mesh and Noffset3D are supported. The GUI features a command-line window, in which Sentaurus Structure Editor prints script commands corresponding to the GUI operations. Script commands can also be entered directly at the command-line window.

III. Mesh and Noffset3D

Synopsys provides two state-of-the-art approaches for the automatic generation of meshes. The quadtree/octree-based method Mesh creates meshes with an axis-aligned structure that is fitted to the boundary. The mesh generator Noffset3D is fully unstructured and pays special attention to mesh elements near material interfaces. Both create meshes that can be used for the discretization methods used in process and device simulators. The meshes are adapted not only to the geometry, but also to the doping concentration in order to capture steep gradients.

IV. Sentaurus Device

Sentaurus Device simulates the electrical, thermal, and optical characteristics of semiconductor devices. It is the leading device simulator and handles 1D, 2D, and 3D geometries, mixed-mode circuit simulation with compact models, and numeric devices. It contains a comprehensive set of physical models that can be applied to all relevant

semiconductor devices and operation conditions. Sentaurus Device is used to evaluate and understand how a device works, to optimize devices, and to extract SPICE models and statistical data early in the development cycle. Applications of Sentaurus Device include VDSM silicon, where Sentaurus Device has proven accuracy to well below 100 nm technology; silicon-on-insulator (SOI) devices, where Sentaurus Device is known for its robust convergence and accuracy; double-gate and FinFET devices, where quantum transport is a reality; SiGe; thin-film transistors; optoelectronics; heterojunction HEMTs and HBTs; and power and RF semiconductor devices.

V. Tecplot SV

Synopsys has integrated and customized Tecplot, dedicated software for scientific visualization. Tecplot, Inc. is a company with a long history of providing high-quality engineering and scientific visualization tools. Tecplot SV is plotting software with extensive 2D and 3D capabilities for visualizing data from simulations and experiments. It represents state-of-the-art scientific visualization. In addition, it is used to explore and analyze data, to produce informative 2D and 3D views, to create presentation-quality plots and animations and to share results on the Web.

VI. Inspect

Inspect is a plotting and analysis tool for x-y data, such as doping profiles and electrical characteristics of semiconductor devices. The graphical user interface allows for quick access to the appropriate curve data. A script language and a library of mathematical functions allow users to compute with curves, and to manipulate and extract data from simulations. The extracted values can be returned to Sentaurus Workbench for further applications.

Following files and programmes are required for SENTAURUS simulation

- Parameter file

  In SENTAURUS device, physical models are defined in physics section. The model parameters, if different from the default, are defined and loaded using the optional parameter file specified in the file section.

- Device structure file

Sentaurus structure editor is a structure editor for 2d and 3d device structures. From the graphical user interface (GUI), 2d and 3d device models are created geometrically. The GUI of Sentaurus structure editor features a command line window, in which Sentaurus structure editor prints script commands corresponding to the GUI operations.

- Sdevice tool

  To obtain electrical-characteristics Sdevice tool is used. For this tool to work, requires following section to be include in command file.

- File section

  Sentaurus Device expects one essential file of input to define the device structure and the field values, for example, the doping, on the structure. In addition, an optional parameter file can be specified.

- Electrode section

  The electrical (or thermal) contacts of the device, together with their initial bias conditions, are defined in the Electrode section. If there is a special boundary condition for a contact, it can be defined here.

- Physics section

  In the Physics section, physical models to be used in the simulation are declared. Example models include the carrier mobility model, the band-gap narrowing model, the carrier generation and recombination model, the impact ionization model, and the gate leakage model.

- Plot section

  This includes the different device parametric values which are to be saved during simulation such as Current Density, (e or h) Density, Mobility, Velocity, Electrostatic Potential, Electric Field, Conduction Band, Valence Band, Quasifermi Potential, Quasifermi Energy and Generation Recombination Rate etc.

- Math section

  It includes the different mathematical algorithms which are to be used for successful simulation. It is used to control the numeric solver in the simulation.

- Solve section

It consists of statements for solving coupled Poisson electron hole equantum, hquantum equations and the quasi-stationary blocks. These quasi-stationary blocks are used to bias and sweep a terminal with voltage or current value.

2.4 Tool Flow:

In a typical device simulation tool flow, the Sentaurus Structure Editor generates a tdr file, which is then used in the Sentaurus Device along with other input files viz. command file (.cmd) and a parameter file to simulate the electrical characteristics of the device. The parameter file(.par) is used for changing the default values. The tdr file can be generated using the Sentaurus Structure Editor alone or it can also be created in an alternate manner: the generation of a device structure by process simulation (using Sentaurus Process), followed by re-meshing using Sentaurus Structure Editor. In this scheme, control of mesh refinement is handled automatically through the command file. The log files contain step-by-step information of the commands executed.

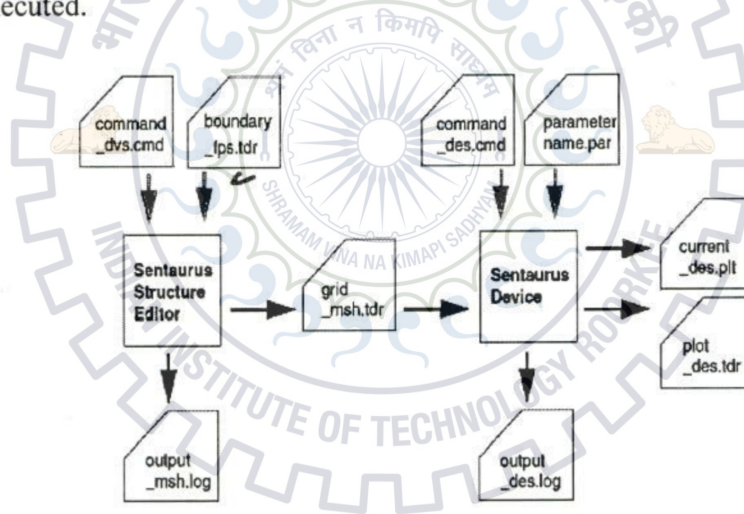

Figure 2.3: Typical tool flow for device simulation using Sentaurus Device

Synopsis Sentaurus is equipped to self consistently compute Band-to-Band-Tunneling (BTBT) current in TFETs. A specified TFET structure is overlapped with a meshing specification so as to create numerous grid points within the entire structure. When calculating BTBT current, the simulator dynamically searches for overlap between valence and conduction bands and then computes the generation rate along various tunneling paths. The model used in

the device simulator Sentaurus has the form of Kane's tunneling model. The parameters $A._{BTBT}$, $B._{BTBT}$ and $C._{BTBT}$ can be defined by the user. The set of default values are 3.5×10^{21} $eV^{1/2}/cm\cdot s\cdot V^2$, 22.5×10^6 $V/cm\cdot eV^{1/2}$ and 2.0 respectively. Also dynamic Non Local path method is used to compute the tunneling components in line and point TFET.

2.5 Kane vs. WKB Approximation:

Kane derive an expression for the rate of electrons tunneling from valence band to conduction band in the paper titled "Zener Tunneling in Semiconductors" [17]. He uses time dependent perturbation theory and Fermi's Golden Rule to calculate the transition rate of carriers tunneling from the valence band to conduction band. The end results of his detailed calculation is-

$$G_{btbt} = \frac{q^2\sqrt{m^*}E^2}{18\pi\hbar^2\sqrt{E_G}} exp\left(-\frac{\pi\sqrt{m^*}{E_G}^{3/2}}{2\sqrt{2}q\hbar E}\right) \tag{2.4}$$

The above equation signifies that band-to-band tunneling (BTBT) rate has an exponential dependence on electric field. It is suitable for direct as well as indirect band gap materials since it calculated the tunneling rate for single as well as many bands existing between the valence and conduction band. The applicability over uniform fields is the only limitation of this approach.

For the explicit calculation of the tunneling probability another intuitive approach is WKB approximation [19]. This involves the integration of all valance band states with momentum directed towards the tunnel barrier and accordingly weighted by a transmission probability. Using various approximations and simplifications, the final expression for tunneling probability is-

$$T \approx exp\left(-2\int_{x1}^{x2} k(x)dx\right) \tag{2.5}$$

where x1 and x2 are classical turning points and shows the locations where electrons enters and exits the potential barrier. For a triangular potential barrier the calculated tunneling rate is identical to the rate shown by Kane's formulation with the exception of slight difference in

numerical pre-factor. Also this gives best results only for direct band gap semiconductors where maxima of valence and minima of conduction band lies along the same Γ momentum. It can only calculate the tunneling rate for the single band existing between two bands. It also fails where the phonon assisted tunneling dominates over direct tunneling. But it is suitable for non-uniform fields with slowly varying potential across the tunneling junction.

3. PHYSICAL UNDERSTANDING OF THE DEVICE:

3.1 Point TFET:

To understand the physics behind the working of the device, different experiments has been performed which relates the various characteristics of the TFET such as band diagram, biasing effects, tunneling current, threshold (onset) voltage etc. Various issues appear into picture while understanding the operation of the tunnel transistor.

3.1.1 Inversion Layer Formation:

Taking into account an n channel point TFET, when a positive bias is applied at the gate terminal, an inversion (conducting) layer of electrons form near channel and oxide interface and completes the conducting path between source and drain. This appearance of the inversion layer as a conducting path can be understood with the help of band diagrams as shown.

Using the above band diagrams it can be seen that the device is operated for the different constant drain biasing with varying gate voltage. When gate voltage is applied at the gate terminal for the different drain biasing a continuous bend in conduction and valence bands can be seen till it reaches to the Fermi level of the drain. Exceeding the gate voltage beyond this level will not bring any effect. Now the question arises, from where these carriers have been generated to invert the channel? The generation of these carriers can be justified by thermal generation, electron coming from drain and electron which tunnel from source to the channel.

The above diagrams are simulated results using quasi-stationary analysis on Sentaurus device simulator. The gate voltage has been varied from 0 to 1volts with steps of 0.1 volts each time. From figure 3.1.1(a) it is clear that the electrons are coming either from thermal generation or from the drain side but since there is no band overlapping between source and the channel hence there will not be any tunneling possible. But as we move to figure 3.1.1(b) and 3.1.1(c) it shows that till 0.3 volts, the source of carrier generation in the channel is again either thermal or drain side and beyond 0.3 volts a tunneling contribution will also be there for the inversion carriers. Also another contribution can be seen that for the different values of the drain voltages the overlapping of the two bands will be different and the corresponding tunneling will be affected.

Now to understand the behavior of carriers to form the conduction channel, their bias dependency should be study. When we increase the drain biasing without applying any bias at the gate terminal, channel region of point TFET gets depleted of carriers and electrons of channel are swept by drain. With the further increase in drain bias more carriers are swept out of the reverse biased drain-channel junction and according to SRH (Shockley-Read-Hall) recombination there will start the generation of electron-hole pairs in the reverse biased space charge region. This can be justified by the negative values of SRH recombination in diagrams shown in figure 3.1.2.

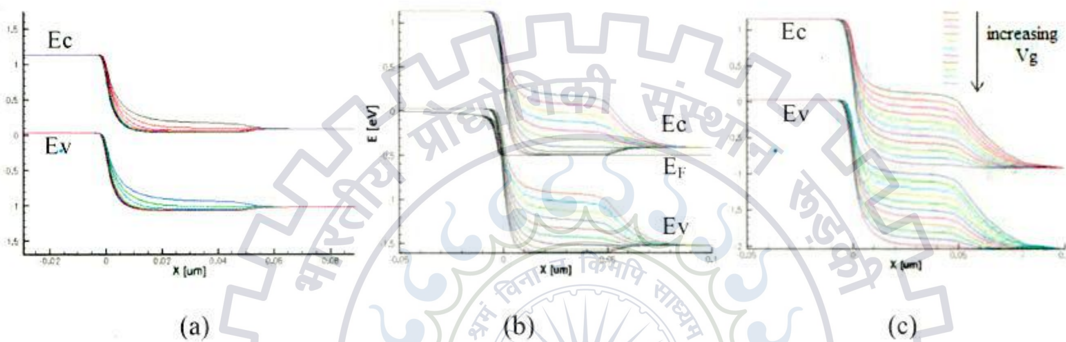

Figure 3.1.1 Point TFET Band diagram (eV) under various bias conditions. (a) with drain at 0 V and gate sweeping from 0-1 V. (b) with gate sweeping from 0-1 V and drain at 0.5 V. (c) with gate sweeping from 0-1 V and drain at 1V. (d) Structure of point TFET taken for observations.

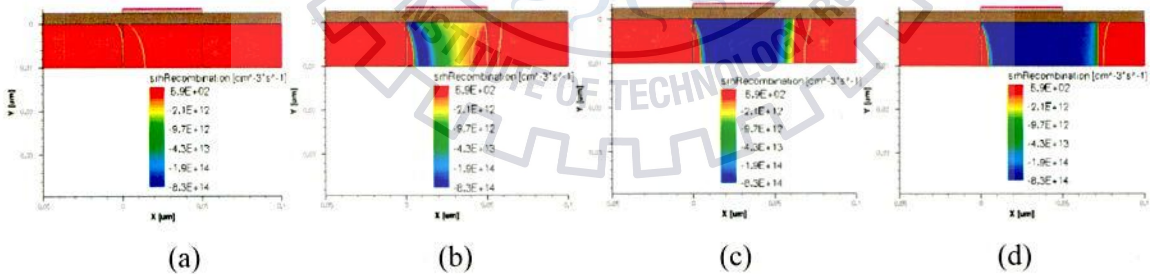

Figure 3.1.2 SRH generation and recombination in point TFET at (a) Vg=Vd=0V, (b) Vg=0, Vd=0.4V (c) Vg=0, Vd=0.8V (d) Vg=0, Vd=1V.

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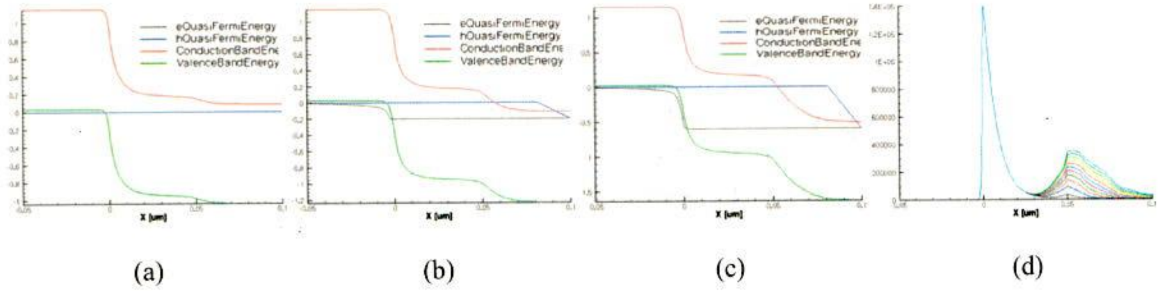
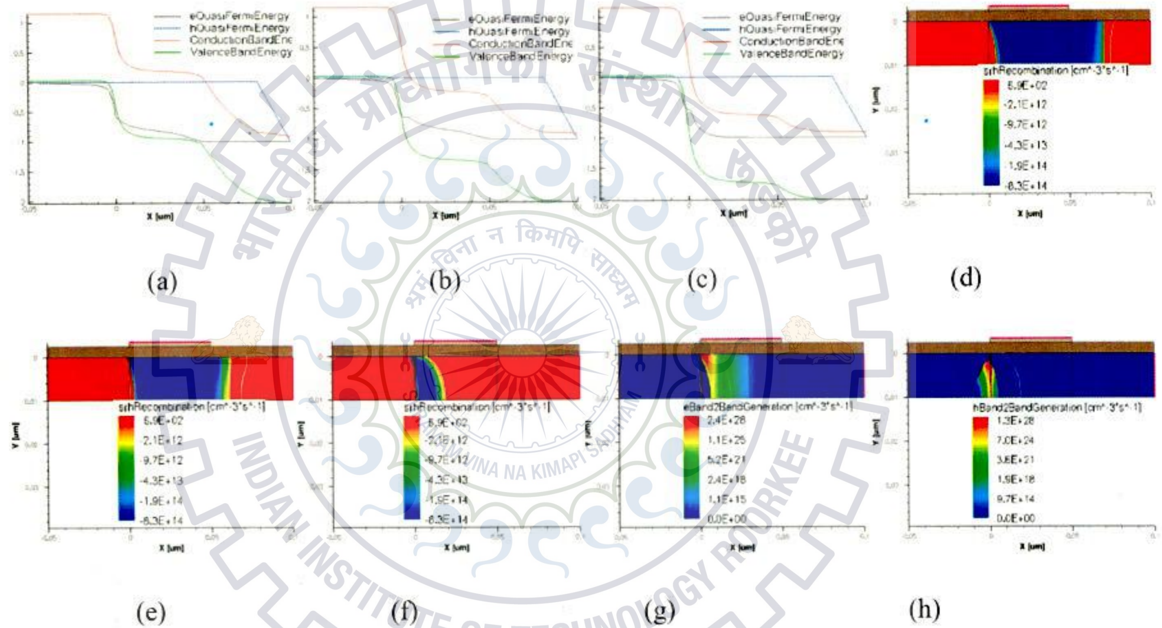


(a) (b) (c) (d)

Figure 3.1.3 (a),(b),(c) shows band diagrams (eV) at Vg=0 and Vd=0,0.5,1V respectively and (d) shows the variation in electric field (V/cm) at the two junctions for Vg=0 and Vd changing from 0 to 1V.



(a) (b) (c) (d)

(e) (f) (g) (h)

Figure 3.1.4 (a),(b),(c) shows the band diagram (eV) at Vd=1V and Vg=0,0.5,1V respectively, (d),(e),(f) shows the SRH generation and recombination at Vd=1V and Vg=0,0.5,1V respectively and (g),(h) shows band to band tunneling of electrons and holes respectively at Vg=Vd=1V.

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These excess carriers (generated electrons and holes) are swept out in opposite direction to each other through the applied drain to source bias and gets recombine with electrons in source region and with holes in drain region (in case of p^{+}-i-n^{+} TFET) to reestablish the thermal equilibrium and continuity of current. The flow of carriers is in the direction of reverse-bias current. This reverse-bias generation current, caused by the generation of electrons and holes in

the space charge region, is the dominating current and constitutes the subthreshold (sub onset) current in TFET until we bias gate terminal.

Also the corresponding band diagrams and electric field, shown in figure 3.1.3 for the above case, suggests that most of the drain to source bias is dropped across the depletion region near drain-channel junction. But the built in electric field (figure 3.1.3(d)) at source-channel interface is much larger than the electric field at the drain-channel junction. Hence the SRH carriers generated at the source-channel depletion region will dominates over the carriers generated at the drain-channel junction.

Now applying gate biases will attracts some SRH generated carries towards the channel oxide interface and increase the electron concentration in the region just below the interface. This increase in electron concentration in channel will cause the conduction band close to the Fermi level and around 0.3V (onset voltage (voltage at which two bands starts overlapping each other or onset of band to band tunneling)) electrons starts tunneling from valence band of source region to the conduction band of channel as shown in figure 3.1.4(b) and (c). Now at this point the increase in electron concentration in the channel region is because of two sources i.e. electrons coming due to electron-hole pair generation in reverse biased space charge region (SRH recombination) and electrons which are tunneling from source side to channel region.

As gate voltage keeps on increasing, the overlapping of two bands keeps on increasing (change in band diagram from figure 3.1.4 (b) to (c)) and more electrons are coming from source side to the channel region. This increase in the tunneling carriers can be clearly seen from the rise in eBand-to-Band generation and hBand-to-Band generation on two sides of the source channel junction (see figure 3.1.4 (g) and (h)). But if we see the change in energy band diagram, one can find that the tunneling of electrons first start at the farthest point in the channel region where the overlapping first occurs and as we increases the gate bias the point of overlapping comes closer to the interface of channel and source and hence the tunneling increases due to reduction in tunnel path length. Also looking at the SRH generation and recombination, we find that as the gate voltage increases there is a decrease in generation over the depleted channel region (figure 3.1.4 (d) (e) and (f)) which is due to the decrease in depletion width in the channel since reverse bias is decreased at the region near to drain. This suggests that at this point the Band-to-Band tunneling is dominating over SRH generation and recombination.

3.1.2 Electron Density:

By increasing the gate voltage when drain is biased at a particular (1V) voltage, the effective reverse bias at the source channel junction will rise and at drain channel junction decreases. This rise in reverse bias will increase the rate of SRH generation at source channel junction and effective e density in this region will increase more as compared to the drain channel junction. As gate voltage reaches to the onset voltage of band-to-band tunneling there is a sudden rise in the electron concentration which shows the starting of tunneling of electron from source to channel. But initially at this point, the rate at which carriers are drifting at drain channel junction is larger than the rate of tunneling of carriers since drain channel junction is maintained at more reverse biased due to low gate voltage. Further increasing the gate voltage increases the region of tunneling across the source channel junction and also it decreases the rate at which carriers are drifting at drain-channel junction due to decrease in reverse bias at this junction, hence the electron concentration also increases in the region away from the source in the channel which can be clearly seen in figure 3.1.5.

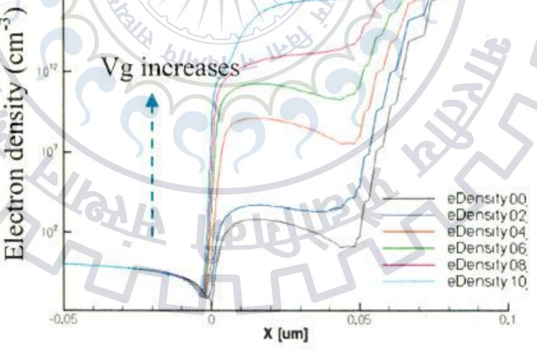


Figure 3.1.5 Change in electron density at different gate bias and Vd=1V.

3.1.3 Dependency on Drain at Constant Gate Voltage:

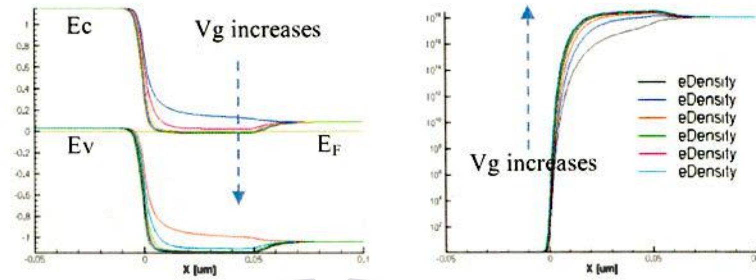
As gate voltage increases without applying any drain voltage, source channel region gets reverse biased and depletion region increases in source as channel region is already depleted of carriers. But as we increase the gate voltage, drain-channel region gets forward biased and more electrons will diffuse from drain side to the channel region. Due to vertical electric field in gated channel region, the electron concentration will increase in the region near to the interface. Since concentration of electron increases in the channel region figure 3.1.6(b), hence depletion region in channel reduces with biasing.

Since the carriers are coming from drain side as same as in case of MOSFET where carriers come from source side, hence surface potential will saturates and conduction band will not go beyond further below the Fermi level of drain side figure 3.1.6(a). Increasing the gate bias will increase the vertical electric field in the channel and hence can be clearly seen from the figure 3.1.6(c) that across the whole channel region the rise in electric field is same at the two junction and channel region. But the built in electric field is at source-channel region is much larger than the at the drain-channel region so the SRH generation of carriers will only takes place at source-channel depletion region only not across the whole channel as shown in figure 3.1.6(d).

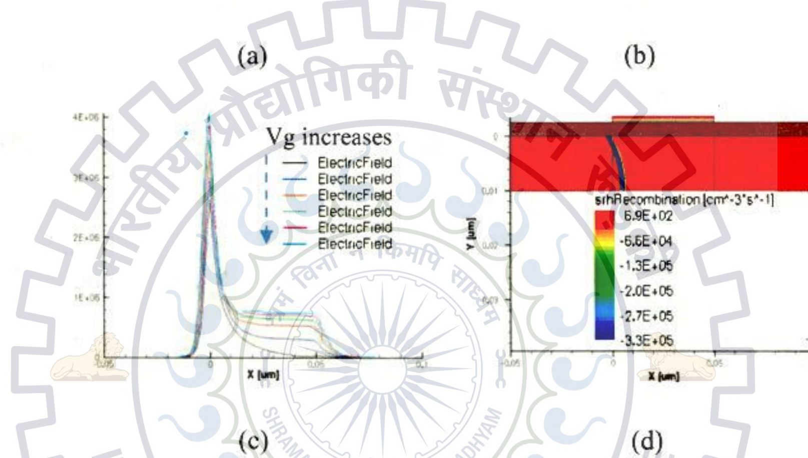
As the gate bias has made a layer just below the gate oxide–channel interface having electron concentration approximately equal to the drain region then this layer behaves as if the drain region gets extended towards the source side. Applying the drain voltage makes the extended drain and source interface region reverse biased and hence initially electrons are swept from this source-channel interface. This can be justified by the change in valence and conduction band energy bands at channel-source interface figure 3.1.7(a). As continuously increasing the drain bias making the drain-channel junction less forward bias because of decrease in bias across this interface (previously which was surface potential only).

As we look at the SRH recombination, applying drain bias will make the extended drain-source interface reverse bias with a high electric field which enables the SRH generation in the depletion region and it increases with drain bias figure 3.1.7(b). Around 0.15 to 0.2 V (onset voltage), we find that the increase in drop across source-channel interface makes the two bands (conduction band at channel side and valence band at source side) to overlap each other and hence this overlapping is the point of start of band to band tunneling of electron from source side

to channel region. As the drain bias increases, the overlapping of two bands increases and the corresponding tunneling also increases figure 3.1.7(a).

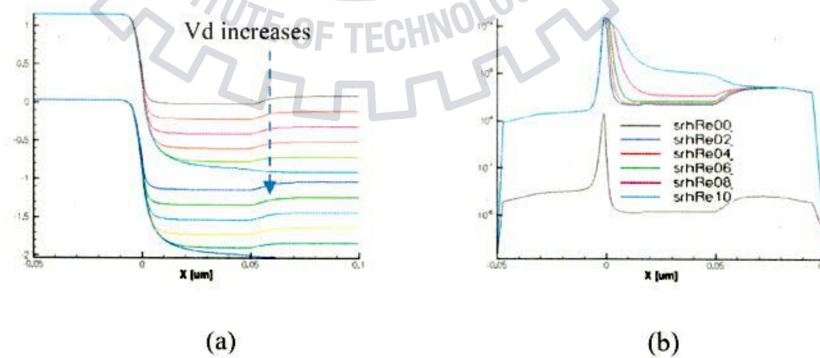


(a) (b)



(c) (d)

Figure 3.1.6 Shows change in (a) Energy Band diagram (eV), (b) electron density (cm^{-3}), (c) electric field (V/cm) at two junctions when Vg changing from 0 to 1V at Vd=0V and (d) SRH recombination at Vd=0, Vg=1V.



(a) (b)

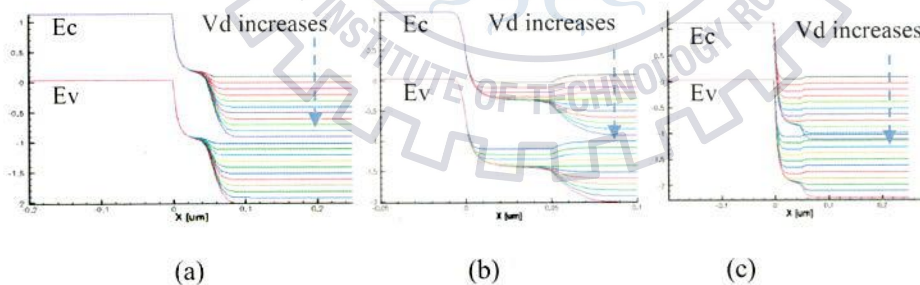
Figure 3.1.7 (a) Band diagram (eV) and (b) SRH recombination ($cm^{-3}s^{-1}$) at Vg=1V and Vd varying from 0 to 1V.

But this overlapping stops after a certain bias which makes the channel-drain region reverse bias and hence afterwards the drain bias starts dropping at the channel drain junction only, figure 3.1.7(a). This dropping of drain voltage at the drain-channel interface brings high field at this junction which increases the SRH generation in the depletion region near to this junction figure 3.1.7(b).

3.1.4 Saturation of IdVd:

As the impact of gate voltage have been studied in the MOS Transistor, similarly drain current in tunnel field effect transistor also gets affected by gate voltage. Different experiments have been performed with various gate voltages and varying drain bias. The gate voltage is varied from 0 V to 0.5 V then to 1 V in three steps but drain voltage is varied in quasi stationary way from 0 V to 1 V using a step size of 0.1 V.

Similar analysis can also be done for the variation in gate voltages. By keeping the gate voltage constant when drain voltage is varied, the drain current increases and gets saturated after a particular value. The reason for this saturation can be explained as-



(a) (b) (c)

Figure3.1.8 Point TFET Band diagram (eV) under various gate voltages (a) with gate at 0 V and drain sweeping from 0-1 V. (b) with gate at 0.5 V and drain sweeping from 0-1 V. (c) with gate at 1 V and drains sweeping from 0-1 V.

The carriers which are forming the channel for conduction, emerges either from drain, thermal generation and tunneling of carriers. By fixing the gate voltage the carriers which are

emerging from the thermal generation are now fixed and not going to increase by varying drain voltage. Also the carriers coming from the drain side decrease as the drain voltage increases hence the only source which contributes the carriers is now tunneling. The overlapping of the two bands decides the tunneling and the rate of tunnel current which is now controlled by gate voltage. The overlapping and the drain current increases with the increase in drain voltage and it saturates after a fixed value. Increasing the drain voltage after this value will not bring any increase in the tunnel current but the extra voltage starts dropping at the channel drain junction.

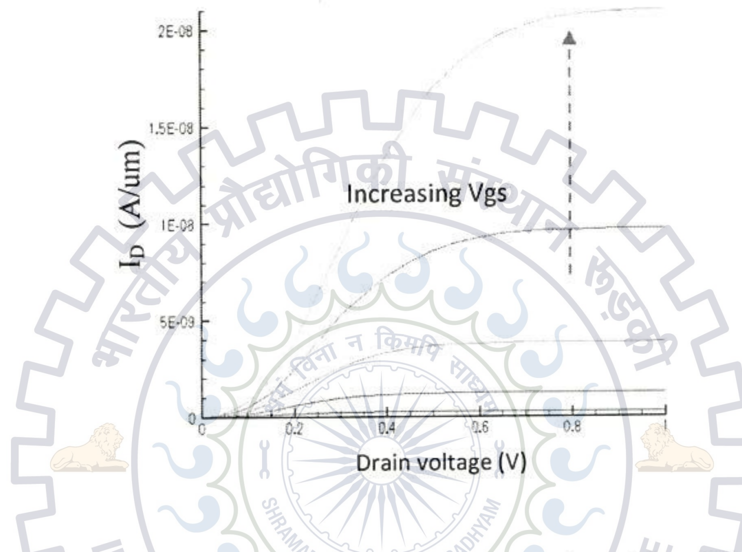


Figure 3.1.9 IdVd curve for Vg varying from 0.5 to 1 V.

The carriers which are coming after tunneling get swept continuously by the drain voltage and hence this limited amount of channel carriers will brings the saturation in the drain current. So the dependency of the tunnel current on the gate voltage and drain voltage cannot be studied independently. It is the gate voltage which decides the onset of saturation of drain current for a fixed value of drain voltage see figure 3.1.9.

Here we can say that a unique characteristic of the Tunnel FET operation is that tunneling of the carriers requires a minimum amount of voltage applied at the drain terminal to turn the device in on state, whatever the applied gate voltage. This is true because the energy barrier narrowing or the tunneling of carriers for the on-current is a function of both gate and drain voltages which critically controls them. Unlike conventional MOS transistors, a second threshold voltage can also be defined for TFET which depends on the drain voltage.

3.2 Line TFET:

A similar study can also be done with the structure of line TFET. In this structure since the gate is overlapping the source completely, see figure 2.1(a) and an inversion layer appears in the source itself under the gate hence the area over which the tunneling taken place will be large as compared to the point TFET structure figure 3.2 (b). The gate biasing will decides the thickness of inversion layer and the concentration of the carriers in the layer which can be clearly seen from the figure 3.2 (a) suggesting the bending of band diagram below the gate region in the source. As the gate voltage increases, the overlapping of two bands occurs at a particular voltage (onset voltage) and electrons starts tunneling from the source region to the inversion layer just below the gate terminal in the source itself shown by the indicated direction.

In this structure as the gate voltage increases more inverted carriers will be enhanced in the region of source and gate dielectric interface. These carriers are supposed to emerging from thermal generation and tunneling both. As can be seen till a particular value of the gate voltage, the carriers are coming from the thermal generation and SRH generation both but when the two bands starts overlapping then an another source of carriers comes as the tunneling of carriers starts and it also participates in the increase in inversion carriers concentration.

The SRH generation (figure 3.2 (c)) and tunneling mechanisms can also be explained in the similar way as done in the study of point TFET. But the increase in the final current is only due to the fact that the area over which the carriers were tunneling in point TFET is smaller than the area in case of line TFET.

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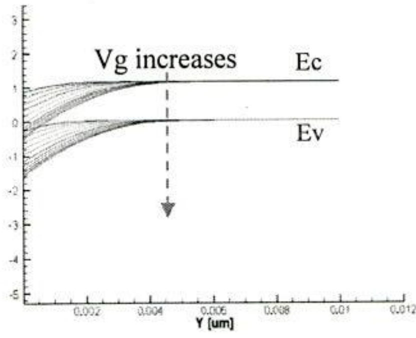
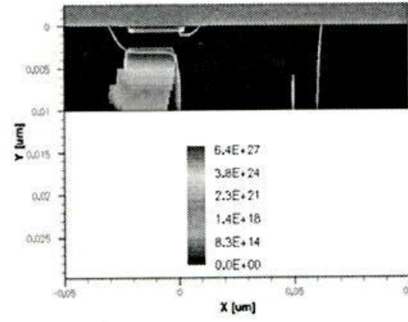


(a)



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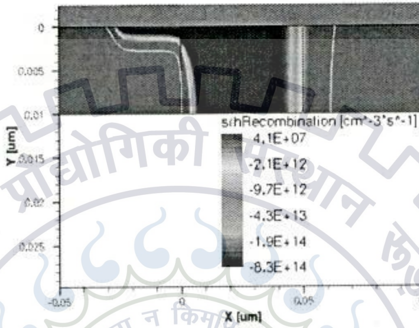

(c)

Figure 3.2 Line TFET (a) Band diagram (eV) along the X direction below gate showing bands overlapping, (b) and (c) showing band to band tunneling and SRH generation and recombination respectively.

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4. ANALYTICAL MODELLING:

Zener tunneling (Band-to-Band tunneling), which defines that the electrons passing from one energy band to another, was first introduced by Clarence Zener in 1934 who explain the dielectric breakdown as a precipitous rise in current with the rise in the field strength. Specifically, in a reverse biased heavily doped semiconducting p^+-n^+ junction where electrons from the region of p^+ valence band can tunnel into the region of n^+ conduction band, the primary transport mechanism was Zener tunneling now called as Band-to-Band tunneling and forms the operational principle for tunnel field effect transistors.

An analytical model of TFET on-current has been proposed by William Vandenberghe et al. [14] where the tunneling current is a function of gate biasing effect only. Later Guido Groeseneken et al. [20] included the effect of drain voltage. Since many of 1-dimensional analytical modeling work already have been published till now, but the influence of inversion channel width on the behavior of tunnel transistor I-V characteristics is not included. Here in this work, we present a study and modeling of a new current component in Gate-over-source Tunnel FET.

The key steps of their model for line TFET structure are-

- Electrostatic potential of the semiconductor is strictly controls by the gate,
- In the region under the gate, the effect of drain voltage is not taken into account,
- One dimensional potential profile is considered by neglecting its variation in the direction parallel to the gate,
- The influence of inversion layer is neglected.

The model in [14] has restricted the current formulation to nTFET only, i.e. the location of the gate is on the top of the *p*-type source. By neglecting the effect of drain voltage, the potential profile is considered one-dimensional. Kane's model [17] is most popular in calculating the generation term for a semiconductor lying in uniform electric field which is given by:

$$G(E) = A\frac{E^D}{\sqrt{E_g}}exp(-BE_g^{\frac{3}{2}}/E) \quad (4.1)$$

where E_g is the semiconductor band gap, E is assume to be the electric field at the tunneling junction and *A,B* are constants which depend on the band gap and effective mass. The above generation term, the tunneling current can be determined by integrating the generation rate over the tunneling volume as shown in the following equation:

$$|I| = q \int GdV = qWL \int Gdz \tag{4.2}$$

The tunneling current in terms of tunnel path and other physical and material parameters of the device is given as (referring eq. 16 of [15]):

$$I \approx -\frac{WLAE_g^{D-1}}{2Bq^D}\left(\frac{1}{l_2^D} - \frac{2E_g\epsilon_s}{q^2N_a}\frac{1}{l_2^{D+2}}\right) e^{-Bq\sqrt{E_g l_2}} \tag{4.3}$$

Now the assumptions made for the above tunnel current calculation are acceptable except the effect of inversion layer as it can be clearly seen in the simulations that the width of inversion layer is quite appreciable when compared to the thickness of the device.

4.1 Inversion width Effect:

The band diagram along the indicated direction 1 is shown in the figure 4.1 (a). The length l_2 described in the above equation indicates the path of the electrons which are tunneling in the direction perpendicular to the gate from the bottom of source to the inversion layer. But as we can see in figure 4.1 (b) the overlapping of the two bands along the direction parallel to the gate suggests that some electrons are also tunneling in this direction.

The way in which we include the current component provided by the additional carriers tunneling in the lateral direction is in tems of modification in the length(L). The total length now includes the length of the gate and the width of the inversion layer($L+W_{inv}$).

The width of inversion layer is calculated using Poisson equation which can be written as:

$$\frac{d^2\varphi}{dy^2} = \frac{qN_a}{\epsilon_0\epsilon_s}\left[1 + e^{(\varphi_x - 2\varphi_b - V_{cb})/V_T} + e^{-2\varphi_b/V_T} - e^{-\varphi_x/V_T}\right] \tag{4.4}$$

where φ_x is the potential at any point along x direction in inversion layer, φ_b is the bulk fermi potential, V_T is thermal voltage and V_{cb} is channel to bulk voltage difference which is zero in our case.

Now integrating equation (4.4) with the boundary conditions at y=0, $\varphi = \varphi_s$, at y=$Winv$, $\varphi = \varphi_b$ and at y=X_d (depletion width), φ=0, the inversion width is given by:

$$W_{inv}{}^2 + 2X_d W_{inv} + \frac{2\varepsilon_o\varepsilon_s}{qN_aK}(\varphi_s - \varphi_b) = 0 \tag{4.5}$$

where φ_s is the surface potential and K represents:

$$K = [1 + e^{(\varphi_x - 2\varphi_b - V_{cb})/V_T} + e^{-2\varphi_b/V_T} - e^{-\varphi_x/V_T}]$$

also the depletion width is:

$$X_d = \sqrt{\frac{2\varepsilon_o\varepsilon_s\varphi_s}{qN_a}}$$

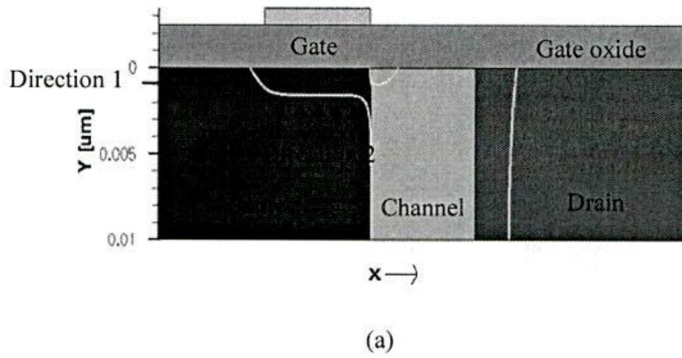
Then by obtaining $Winv$ from eqn. 4.5, the modified tunnel current equation will be:

$$I \approx -\frac{W(L+W_{inv})AE_g^{D-1}}{2Bq^D}\left(\frac{1}{l_2^D} - \frac{2E_g\epsilon_s}{q^2N_a}\frac{1}{l_2^{D+2}}\right)e^{-Bq\sqrt{E_g l_2}} \tag{4.6}$$

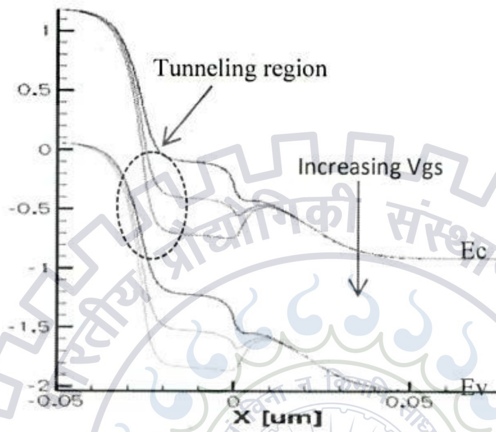
4.2 Comparison with Simulated Results:

When a line TFET is simulated with the parameters given in section [15] using Sentaurus TCAD simulator and compared with the formula derived analytically equation (3) we get the on-current curves as shown in fig.4.2.

The results show that there is an appreciable difference between the simulated result and the modeled formula. This difference can be reduced by including the width of inversion layer also and modifying the length as given in the total current equation (eqn.4.6).



(a)



(b)

Figure 4.1 (a) TFET Structure and directions of electron tunneling. (b) Band diagram along the direction 1.

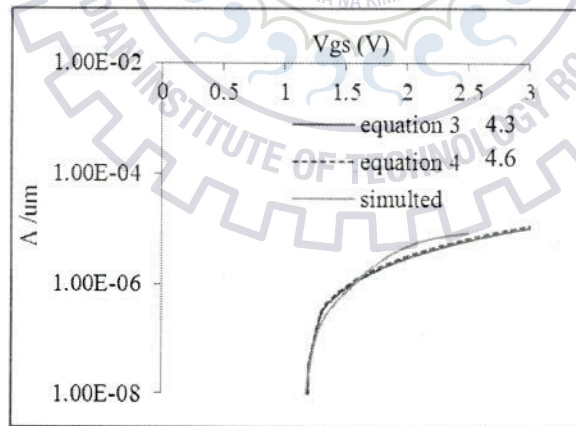


Figure 4.2 Log Id with various gate voltages showing comparison of simulated data and equation 4.3 and equation 4.6.

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When this component is studied exclusively using "Non Local Mesh Band To band Tunneling" models, it is found that its contribution is around 8-9% of the tunneling current in the perpendicular direction to gate terminal. When this component is added to the tunneling current already proposed, and then the total current is closer to the simulated current values.

5. SUB ONSET CURRENT MODELLING

From the discussed physics section we can say that there are two components which constitute the on current in the TFET. One because of the SRH generation in the depletion region near to the source-channel interface when it gets reverse biased and goes on increasing with the reverse electric field and another which enables only when the overlapping of two bands (valence band of the source side and conduction band at channel side of the device) starts i.e. after onset voltage and contains the carriers which are tunneling from source side to the channel region.

In last few years there are some analytical models have already been proposed for tunnel field effect transistor (TFET). G. Groeseneken et al have proposed a complete model for TFET which includes two components for tunneling current, one which occurs at source/channel interface and located in a small area (point tunneling) while the another component is located in the portion of source region which is overlapped by gate terminal (line tunneling) [14-15]. Later they modify the model by including the effect of drain voltage [20]. These works were based on 1-D solution of Poisson's equation along the tunneling path. A pseudo-2-D approach also has been proposed which more accurately explains the electrostatics of the tunnel FET by considering the junction depletion regions [21], [22]. All these models describe the tunnel current based on band-to-band tunneling of carriers from valence band at source side to conduction band at channel side but it is dominated only after the onset of overlapping of two bands i.e. after onset voltage.

5.1 Introduction to SRH:

Before applying proper gate bias so that the two bands (valence band and conduction band) starts overlapping to each other, the contribution of band to band tunneling (so called Zener tunneling) to the conduction current is very less as compared to the SRH recombination current in the channel. SRH is the dominant form of recombination mechanism where an additional energy level is introduced in the forbidden band gap of the semiconductor by the impurities. This energy level leads to recombination by acting as a trap and captures electrons and holes. As in down scaled devices where the doping concentration in the different regions across the junction

reaches to the order of $10^{18}cm^{-3}$ or more, there occurs tunneling via impurity states or traps along with conventional SRH recombination [23]. Trap-Assisted tunneling and SRH recombination are same mechanisms i.e. recombination via impurity states but the difference lies from where the electron makes a transition to the trap state. Hurkx also explain the importance of inclusion Trap-Assisted-Tunneling (TAT) along with band-to-band-tunneling (BTBT) in reverse biased p-i-n diode structure [23]. It shows that at strong field it is necessary to take the effect of carriers tunneling through the band gap (directly from band to band (Zener)) and transitions via trap (TAT) together to explain the complete conduction across the tunnel junction.

Hence before onset of BTBT it is the TAT (modified SRH) which dominates in the conduction current and can be termed as "sub onset current" (current before onset of BTBT). Now for the modeling of TAT as a recombination process, Hurkx has derived a recombination rate which accounts for the carriers tunneling via traps and it gets converted to the conventional SRH at low fields across the junction.

The conventional SRH is determined by the carrier density captured per unit of time along with the probability of emitting a free carrier per unit of time from a trap which is given by:

$$R_{trap} = N_T \frac{C_n C_p np - e_{n0} e_{p0}}{C_n n + C_p p + e_{n0} + e_{p0}} \tag{5.1}$$

where N_T is density of the traps, along with n, p are the density of electron and holes, C_n, C_p are the capture rate of electron and holes and e_{n0}, e_{p0} corresponds for the probabilities of the emission of electron and hole per unit of time.

But at high field this recombination rate gets modified which also include the effect of tunneling of carriers across the band gap via traps and hence density of carriers and the emission probability will change and also include the effect of tunneling of carriers [23]. Both the carrier concentration and emission probability get enhanced by the same factor when a linear potential is applied, i.e.

$$\frac{e_n}{e_{n0}} = \frac{n_t}{n} \equiv \Gamma_n + 1 \tag{5.2a}$$

$$\frac{e_p}{e_{p0}} = \frac{p_t}{p} \equiv \Gamma_p + 1 \quad (5.2b)$$

where field effect is introduced using field effect factor Γ_n and Γ_p.

Now following the same steps of derivation as used to derive the conventional SRH expression, the modified recombination term is achieved as:

$$R_{trap} = \frac{pn - n_{ie}^2}{\frac{\tau_p}{1+\Gamma_p}[n + n_{ie}\exp(E/KT)] + \frac{\tau_n}{1+\Gamma_n}[p + n_{ie}\exp(-E/KT)]} \quad (5.3)$$

where E is the difference between the trap energy level and intrinsic level i.e. $(E_T\text{-}E_i)$, τ_n and τ_p are the recombination lifetimes of electron and holes respectively and n_{ie} is the intrinsic carrier concentration. $\Gamma_{n,p} << 1$ for the weak fields and above equation 3 reduces to conventional SRH recombination formula. Also the field effect factor is same for electron and holes and is given by $\Gamma_n=\Gamma_p=\Gamma$:

$$\Gamma = 2\sqrt{3\pi}\frac{|F|}{F_\Gamma}exp\left[\left(\frac{F}{F_\Gamma}\right)^2\right] \quad (5.4)$$

with

$$F_\Gamma = \frac{\sqrt{24m^*(KT)^3}}{q\hbar} \quad (5.5)$$

where signifies the local field in the depletion region, m* is the effective mass of the electron and other symbols have their usual meaning.

Now the current due to this recombination rate is given by the volume integral of the total charge associated with this recombination rate.

$$I_{sub} = \int qR_{trap}dV \quad A \quad (5.6)$$

$$I_{sub} = qt_{si}W\int R_{trap}\,dy \quad A \quad (5.7)$$

where t_{si} is the thickness, W is width of the device and dy is the elementary width of depletion layer. One assumption have been made to include the thickness of the device in the above

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formula is that the rate of recombination is same in the hole region of the depletion width along the thickness of the device which is approximately correct for the small thickness devices i.e. around 10 nm.

Assuming the recombination at a trap level of mid gap states i.e. $E_t \approx E_i$ gives E=0 and equal recombination lifetimes for electron and holes brings $\tau_n = \tau_p = \tau$. Also in presence of only drain bias the p-i-n diode is reverse biased and under reverse bias the mobile carriers have essentially been swept out of the space charge region (p=n=0).
Hence putting recombination rate in the above equation yields:

$$I_{sub} = -\frac{q t_{si} n_{ie} W}{2\tau} \int 1 + 2\sqrt{3\pi}\left(\frac{F}{F_\Gamma}\right) exp\left[\left(\frac{F}{F_\Gamma}\right)^2\right]\ dy \qquad (5.8)$$

In the above equation F signifies the local field in the depletion region. As the device contains two depletion regions at the two junctions i.e. at source-channel interface (p+-n junction) and another at the drain-channel interface ($n\text{-}n^+$ junction). To calculate the width of the depletion region there is a requirement of channel carrier concentration which changes from doping concentration of the channel due to the structure of the device.

Let initial doping concentration inside the channel is N_d (n type donor impurities) then the corresponding Fermi potential is Φ_f. For silicon the metal semiconductor work function difference is $\Phi_{ms} = V_{fb} = \Phi_m - (4.05 + Eg/2 - \Phi f)$, where V_{fb} is flat band voltage, Φ_m is metal work function and E_g is the band gap of silicon. Gate voltage Vgs can be written as the sum of electrostatic potential at the interface (Ψ_{max}) and the potential difference over the oxide,

$$V_{gs} - V_{fb} = \Psi_{max} + t_{ox}E_{ox} \qquad (5.9)$$

For the small thickness device we can assume that the effect of gate metal brings the surface potential which is same across the whole thickness *($\Psi_{max} \approx \Psi_s$)*. Also considering the change in one direction in electric field only, then using boundary condition at oxide-semiconductor interface as $\epsilon_{ox}E_{ox} = \epsilon_s E_s$. Solving 1-D Poisson equation in the channel to get electric field in terms of surface potential and putting in above equation gives:

$$V_{gs} - V_{fb} = \Psi_s + 2t_{ox}\frac{\epsilon_s}{\epsilon_{ox}}\sqrt{\frac{qN_d\Psi_s}{2\epsilon_s}} \tag{5.10}$$

Surface potential can be calculated using above equation as:

$$\Psi_s = \left\{-t_{ox}\frac{\epsilon_s}{\epsilon_{ox}}\sqrt{\frac{qN_d}{2\epsilon_s}} + \sqrt{\frac{{t_{ox}}^2\epsilon_s}{{\epsilon_{ox}}^2}\frac{qN_d}{2} + \left(V_{gs} - V_{fb}\right)}\right\}^2 \tag{5.11}$$

The improvement in the channel concentration due to this gate material can be accounted by taking the shift in the initial Fermi potential (Φ_f) due to the above surface potential ($\Phi_F=\Phi_f+\Psi_s$). And the new improved concentration due to gate metal only can be calculated using,

$$N_D = n_{ie}exp\left(\frac{\Phi_F}{V_T}\right) \tag{5.12}$$

where N_D is the improved channel concentration due to metal gate and V_T is the thermal voltage at room temperature given by V_T=KT/q.

Now this MOS structure can be supposed to be sandwiched between highly p type doped source and n type doped drain region. Under equilibrium the holes will be injected from p+ source to the channel region as same what we have across a p-n junction and similarly some electron will be injected from channel region to the p^+ source to maintain that equilibrium. The concentration of minority holes in the channel region near to the interface or at the edge of the depletion region is given by:

$$\bar{p}_n = \bar{p}_p exp(-qV_{Bsc}/KT) \tag{5.13}$$

where $\bar{p}_n$ is minority concentration in the channel, $\bar{p}_p$ is the concentration of majority in the source (N_A for p type source) and V_{Bsc} is the built in potential at the source-channel junction. Hence electron concentration in the channel can be calculated as

$$N_{new} = \bar{n}_n \approx \frac{n_{ie}^2}{\bar{p}_p} = \frac{n_{ie}^2}{N_A} exp(qV_{Bsc}/KT) \tag{5.14}$$

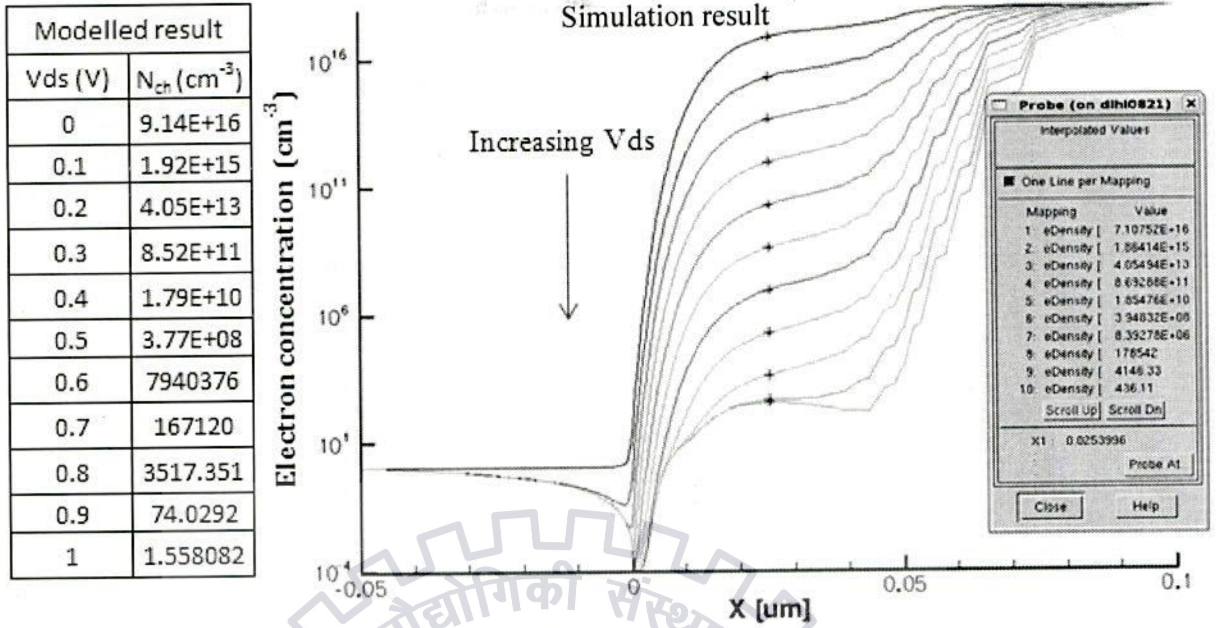
where N_{new} is the new electron concentration in the channel which is same as the majority concentration $\bar{n}_n$ in the channel near to the depletion region edge. Also when we consider the lightly doped channel region connected to the heavily doped drain then there will be diffusion of carriers from a higher concentration region to the lower one. This electron flow from n+ region to the n channel region will be affected when drain bias is applied. When drain is biased with a positive supply then the n+ drain-n channel junction will be reversed biased and the equilibrium flow of electrons form drain to the channel will be dominated by the drift of electrons from channel to the drain region. Then under reverse biased the new electron concentration in the channel near to the drain-channel junction depletion region (N_{ch}) can be given in terms of improved channel concentration (N_{new}) as:

$$N_{ch} = N_{new} exp(-qV_{ds}/KT) \tag{5.15}$$

where V_{ds} is the applied reverse biased drain voltage. Putting equation (5.12), (5.13) and (5.14), the above equation can be rewritten as:

$$N_{ch} = n_{ie} exp\left(\frac{\Phi_f + \Psi_s - V_{ds}}{V_T}\right) \tag{5.16}$$

For the channel length (≈ 50nm), the effect of source and drain are not separated but they merges together to maintain the equilibrium concentration in the channel, given by the above formula. The validity of the above equation can be seen through the simulations.



Modelled result	
Vds (V)	N_{ch} (cm^{-3})
0	9.14E+16
0.1	1.92E+15
0.2	4.05E+13
0.3	8.52E+11
0.4	1.79E+10
0.5	3.77E+08
0.6	7940376
0.7	167120
0.8	3517.351
0.9	74.0292
1	1.558082

Figure 5.1 Shows closeness of electron density at gate zero bias and drain biasing from 0 to 1 V.

Now we can calculate the depletion width at the two junctions using the net channel concentration. Considering the field at any point in the deletion region includes both the built in field and surface potential at that point near to source-channel interface *($F=E(y)+\Psi_s/W_{sc}$)*, where W_{sc} is the depletion width of the source-channel interface junction. To calculate $E(y)$, 1-D Poisson equation can be solved to give:

$E(y) = -\frac{qN_{ch}}{\epsilon_s}(y - y_{ch})$ where y_{ch} is the width of depletion region in the channel. Putting the field in equation (5.8) with proper limits of integration, we have

$$I_{sub} = -\frac{qt_{si}n_{ie}W}{2\tau}\int_0^{W_{sc}} 1 + 2\sqrt{3\pi}\left(\frac{|E(y)|+\frac{\Psi_s}{W_{sc}}}{F_\Gamma}\right) exp\left[\left(\frac{E(y)+\frac{\Psi_s}{W_{sc}}}{F_\Gamma}\right)^2\right] dy \qquad (5.17)$$

Solving by substitution method of integration, above equation can be written as:

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$$I_{sub} = -\frac{q t_{si} n_{ie} W}{2\tau}\left[W_{sc} + 2\sqrt{3\pi}\, X\right] \qquad A \qquad (5.18)$$

where

$$X = \frac{F_{\Gamma}\epsilon_s}{2qN_{ch}}\left\{exp\left[\left(\frac{\Psi_s}{W_{sc}F_{\Gamma}}\right)^2\right] - exp\left[\left(\frac{\frac{qN_{ch}W_{sc}}{\epsilon_s}+\frac{\Psi_s}{W_{sc}}}{F_{\Gamma}}\right)^2\right]\right\} \quad cm \qquad (5.19)$$

Similarly the current due to SRH generation and recombination at drain-channel interface junction can also be calculated by looking at the physics associated with the n-n$^+$ junction. As one can find that the channel is fully depleted of carriers after applying drain bias and also most of the drain region gets depleted due to this. Now with initially gate at zero bias most of the drain voltage will gets dropped at the region associated with the drain depletion. This can also be justified with the help of band diagrams at Vg=0 and changing the drain voltage continuously given in figure 5.2.

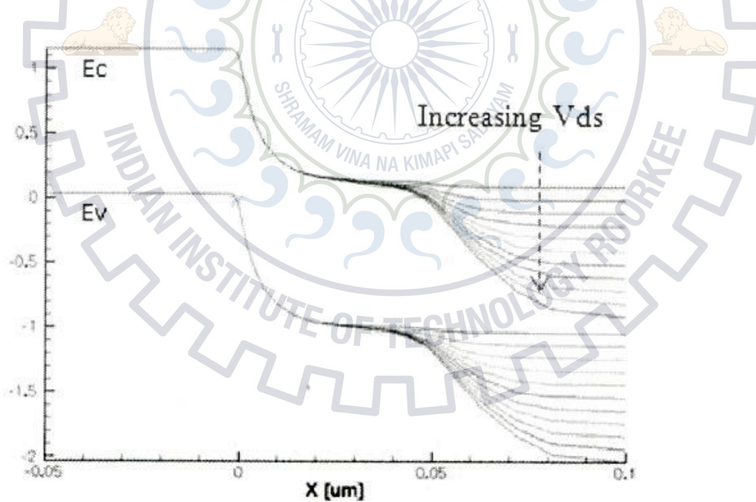

Figure 5.2 Energy band diagram (eV) at gate zero bias and drain changing from 0 to 1 V.

From the above figure it is clear that without any gate bias, all the drain voltage will gets dropped at the drain-channel junction and wii affect the field associated with the drain depletion

region. For calculating depletion width in n-n$^+$ junction we can simply put the hole concentration of n type region given by $n_{ie}{}^2/N_d$. Here the n type region signifies the channel region and n+ region is denoted by drain. So the depletion width in the drain region is given by:

$$W_d = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{n_{ie}{}^2}{n_{ie}{}^2 N_d^+ + N_d^{+2} N_{ch}}\right)(V_{Bcd} + V_{ds} - \Psi_s)} \tag{5.20}$$

where N_d^+ is drain doping concentration. Also when we calculate the electric field in drain depletion region using Poisson equation it is given by:

$E(y) = -\frac{qN_d^+}{\epsilon_s}(y - W_d)$ with W_d as the width of drain depletion region. Following the same steps as followed to obtain equation (5.18), SRH generation and recombination current is given as

$$I_{sub} = -\frac{qt_{si}n_{ie}W}{2\tau}\left[W_d + 2\sqrt{3\pi}\, Z\right] \quad A \tag{5.21}$$

where

$$Z = \frac{F_\Gamma \epsilon_s}{2qN_d^+}\left\{exp\left[\left(\frac{\Psi_s}{W_d F_\Gamma}\right)^2\right] - exp\left[\left(\frac{\frac{qN_d^+ W_d}{\epsilon_s} + \frac{\Psi_s}{W_d}}{F_\Gamma}\right)^2\right]\right\} \text{ cm} \tag{5.22}$$

The total sub onset current is the summation of equation (5.18) and (5.21).

5.2 Comparison with Simulation:

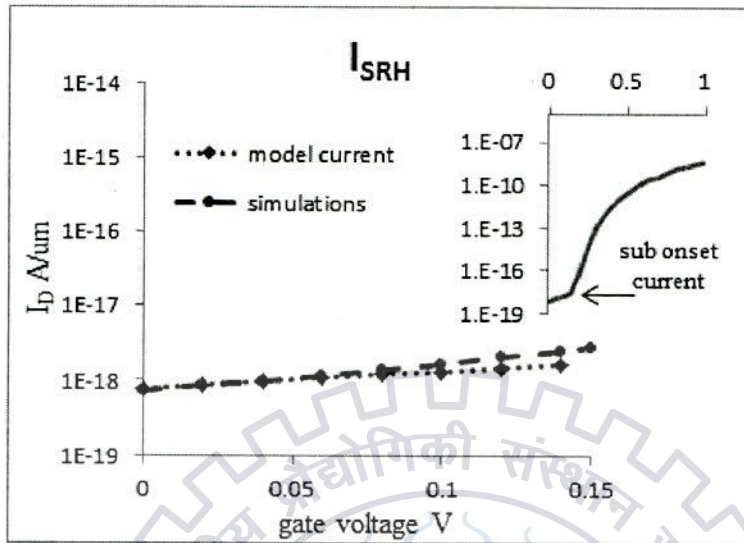

Figure 5.3 Sub onset current given by simulations and modeling by SRH generation and recombination.

We can understand the importance of SRH generation and recombination current in TFET through the closeness with simulation results. Here in the above figure 5.3, inset shows the complete log Id Vs gate voltage characteristics of the tunnel field effect transistor where sub onset voltage point is also shown by the arrow. As already explained we have assumed this (sub onset) point as the point of voltage where the tunnel current dominates over the SRH generation current in the tunnel FET. So up to this point the current nature can be explained by the SRH generation and recombination current across the depletion region in the channel.

6. CONCLUSION:

6.1 Summary of Work

By splitting TFET structure into gate over source (line TFET) and conventional structure (point TFET), it is much easier to understand the physics behind the working principle of the tunnel FET. Both (Kane's model and WKB approximation) the models, for the calculation of carrier generation rate, are quite similar in expression but they differ in their basic approach of application. After studying the different models present in the Sentaurus, a calibrated simulation environment is used to study the SRH generation and recombination along with Band-to-Band tunneling.

A detailed carrier behavior based on different terminal biasing is presented to study the physics behind the TFET operation. How the carriers are changing their behavior based on th different terminal biasing and how is the conducting path is establishing the thermal equilibrium is taken into consideration for both the structures i.e. line and point tunnel. By keeping the biasing of a terminal constant and changing the other changes the nature of the carriers to form the conducting channel. Then to include the inversion width effect in the current modeling of the line TFET we have included an additional component of carriers which are tunneling in the lateral direction along the width of inversion layer to modify the reported on-current expression. In this way the effect of inversion layer is included which was neglected in previous works. The resulting current is now closer to the simulated data, hence increasing confidence in the analytical model.

Detailed analysis of the present models predict that they are quite satisfactory when Band-to-Band Tunneling is considered but when their low voltage behavior is studied then is appears that they are lacking in the inclusion of sub onset current or SRH current which must also be taken into consideration for the complete on-off behavior modeling of the TFET. Hence finally based on the SRH generation and recombination, a sub onset current model is presented which shows a good agreement with the simulations.

6.2 Further Scope for the Research

Still there are certain areas where the study has not been done to include the effect physical dependency of the threshold voltage on the two terminal voltages of the TFET. The threshold voltage depends on both the drain as well as gate voltage and it varies if any one of the voltage gets changed. So the relation between the two voltages and the threshold is required to be finding out in order to know the exact physics in the case of tunnel transistor. The study of parasitic parameters such as resistance and the capacitance is also required to analyses the application part of the tunnel transistor.

The effect of two dimensional electric field and inversion width is still missing in the modeling of the point TFET.

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1. Parmanand Singh, Radhakrishnan Sithanandam, Vivek Asthana, Anand Bulusu and Sudeb Dasgupta,"Improved Analytical Modeling of on-current of Gate-over-source Tunnel FET," *VLSI Design and Test*, 2013, (communicated).
2. Parmanand Singh, Vivek Asthana, Anand Bulusu and Sudeb Dasgupta,"Analytical Modeling of Sub-Onset Current of Tunnel FET," (targeted for TED).