3-DIMENSIONAL SIMULATION OF SINGLE EVENT UPSET OF 6T-SOI BASED 24 nm –FINFET SRAM CELL

A DISSERTATION

Submitted in Partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

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ELECTRONICS & COMMUNICATION ENGINEERING

(With Specialization in Microelectronics and VLSI)

By

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CANDIDATE'S DECLARATION

I hereby declare that the work, which is being reported in this dissertation entitled, "**3-Dimensional Simulation of Single Event Upset of 6T- SOI Based 24nm-FinFET SRAM cell** ", which is being submitted in the partial fulfilment of the requirements for the award of degree **Master of Technology** in **Microelectronics & VLSI**, submitted in the Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee (India), is an authentic record of my own work carried out from June 2012 to May 2013 under the guidance and supervision of **Dr. Sudeb Dasgupta**, Associated Professor and, **Dr. Anand Bulusu** Assistant Professor, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter embodied in the dissertation report to the best of my knowledge has not been submitted for the award of any other degree elsewhere.

Dated: 27/6/2013

Place: Roorkee

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CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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Namani Jayaram

M.Tech(MEV)

Dedicated to my parents and loving brothers for their unconditional love and support.

ABSTRACT

Recent years the radiation effects on modern electronic devices are considered to be an important task, due to continues technology scaling and minimal nodal capacitances. Heavy ion impacts on electronic devices causes the large amount of electron-hole pair generation along it's track. The generated charge under the established electric fields would create the electrical disruptions and changes in node voltages. This became worse for the current technologies due to reduced feature sizes and supply voltages. In this report, we present radiation particle interactions, effects on FinFET SRAM cell. The main objective of this report is to benchmark the FinFET to get the required performance followed by 3-dimensional numerical simulation of 6T-SRAM cell as a contiguous block of silicon and to study the impact of heavy ions on the data states of the cell. We studied the critical charge (Q_{crit}) characterization of the designed SRAM cell and found the SEU threshold Linear Energy Transfer (LET).

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1. INTRODUCTION

Radiation induced effects caused by heavy ion strikes present a continual reliability challenge to the operation of the electronic devices used in radiation harsh environments. The fast-growing scaling and reduced supply voltages have diminished the stored charges at the circuit nodes. This made the designs more vulnerable to ionizing particle strikes. The increased density of the chip and reduced on-chip capacitances enhanced the damage probability due to ion strikes. Thus a low energy particles can also have greater probabilities to cause an upset. The outcomes caused by heavy ion strikes at the sensitive part of an integrated circuit can be complicated, and depend on several factors related to the ion (Linear Transfer Energy (LET), energy, incident angle) and to the characteristics of sensitive devices. The heavy ion impact at a particular of the circuit can cause a wide variety of effects, ranging from simple bit flips to permanent device failure. Here are the two kinds of errors called soft error and hard error. A bit error is called soft error that means the data at a node is damaged but the device is not damaged. However, the complete device failure is called hard error. Non-destructive phenomena have been observed in Static Random Access Memory (SRAM) cells, charge leakage from the flash memory floating gate, micro dose effects, stuck bits. The Soft Error Rate (SER) is the frequency of the soft errors that do not result in permanent device damage. This was the main concern in Dynamic Random Access Memory (DRAM) cells in a few years back. But the reduced node capacitances because of the improved lithographic techniques raised the SER concern in SRAM cells and in other logic designs as well. When an ion passes through the sensitive part of a circuit results in a large amount of charge generation. The generated charge may discharge the stored nodes leading to bit upsets. These upsets are either Single Bit Upsets (SBU) or Multiple Bit Upsets (MBU). The SBU take place when the ion affects only the impact node. The MBU takes place when the ion strike also influences the neighboring nodes. These difficulties made the electronic designs more complicated in order to produce best quality products. This became worse with the reduced feature sizes and reduced supply voltages. All these consequences put the researchers in the direction of radiation hardened circuit design. This concern has risen about its need to produce the components immune to radiation especially in space and military applications. But there is a technology gap between the radiation hardened circuit design and commercial electronics.

1.1 Material behavior due to Radiation:

Here I want to discuss the behavior of the target materials and the effects caused by the radiation. The radiation particles in a radiation environment can have a wide range of energies associated with them. So there are two types of damage mechanisms that can be caused by the energy particles. One is Ionizing damage and the other one is Lattice damage.

1.1.1 Lattice Damage:

Lattice damage is also called displacement damage. High energy particle can displace the lattice atoms during elastic or inelastic nuclear collisions. That means a particle with sufficient energy can knock the lattice atoms from its actual lattice positions. This creates voids and extra interstitial atoms in the target materials. Creating disorder in the atomic arrangement, increasing recombination centers and permanent damage to the material. This causes poor properties of the material and differ in original characteristics of the devices which had been made with the affected materials. The displacement damage mechanism can be demonstrated by the metric called Non Ionizing Energy Loss (NIEL). NIEL gives the energy transfer to the lattice atoms as the ion passes through the material.

1.1.2 Ionization Damage:

This is due to the impact of charged particles. When a charged particle strikes the semiconductor material, it loses energy through the columbic scattering with the lattice atoms. This energy is then transferred to the valence electrons. Some of the electrons will get sufficient energy and ionized to the conduction band. This creates a plasma of electron-hole pairs along the particle track. The generated charge collected as an excess charge at the circuit nodes under previously established electric fields. The rate of energy loss with the material is well demonstrated by Linear Energy Transfer (LET). The collection of generated excess charge is first dominated by drift and then followed by diffusion. This can be explained properly by Funneling effect.

1.1.3 *Funneling effect:*

The soft errors in semiconductor memory chips were first identified by May and Woods [1]. From that point onwards this concern has heightened its effect because the technology scaling made the situation worse that the integrated circuits more vulnerable to soft errors. These errors considered as serious problems by the observation of enhanced charge gathering by rapid drift currents, which was named as funneling effect.

The funneling effect was first explained by McLean and Oldham [2]. When a heavy ion strikes the reverse biased P-N junction, it creates plasma of electron-hole pairs (EHP) along the path by the columbic scattering with the atoms. The plasma of EHP's forms a conductive cylindrical column throughout the path. The plasma lasts in times of orders of picoseconds within the cylindrical column. At this time the plasma density is very much higher than the substrate doping concentration. So the depletion region in the vicinity of column neutralized shown in figure 1.1b. Before the ion strike, the depletion region is a highly resistant region and consist high electric fields. After the plasma collapses the depletion region, that area becomes conductive. So the initial electric fields associated with the depletion region now reduced in magnitude and extend into the substrate.

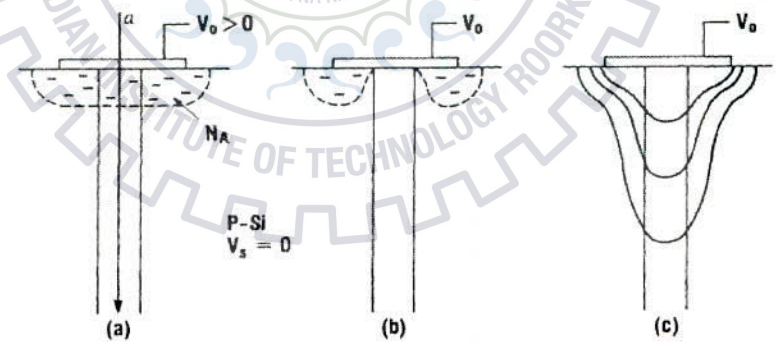


Fig. 1.1: Schematic of charge funneling mechanism indicating in (a) an a-particle strike through an n^+-p junction and associated depletion well, in (b) depletion layer being neutralized by the plasma column, and in (c) equipotential lines extended down from original junction along particle track.

Figure 1.1c shows the distortion of equipotential lines along the particle track associated with the collapsed depletion region. The depletion region is further collapsed until the plasma reaches its maximum. Till then the equipotential lines pushed down into the substrate.

Now the charge separation takes place at the outer edges of the column, The holes driven out of the column and diffused into the neutral substrate. The electrons drifted towards the electrode due to the high electric fields. After some time (orders of picoseconds) the depletion region recovers back and the equipotential lines gets to its original position. So the charge collection is very fast (drift) immediately after the ion strike due to high electric fields, As the time proceeds the fields along the plasma column decrease rapidly, and drift collection of charge gets weaker and weaker.

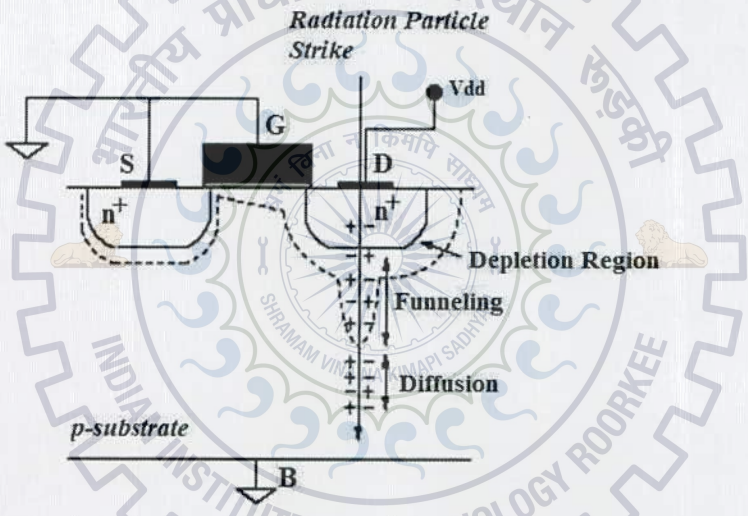


Fig 1.2: Charge deposition and collection by a radiation particle strike.

Figure 1.2 shows the schematic view of charge collection. The carriers under funnel region drifts towards the electrode and the carriers outside the funnel diffused into the substrate. Finally the junction recovers back to the previous condition. The charge collected during this process may lead to various Single Event Effects (SEE) in digital circuits. These are the main reason for data errors in SRAM cells, flip-flops and other memory units. In analog circuits this collected charge may lead to transient current pulses that flows through the circuit as noise.

1.2 Radiation effects in integrated circuits:

These are categorized into two, *(i)* Total Ionizing Dose Effects (TID) *(ii)* Single Event Effects (SEE).

1.2.1 Total Ionizing Dose Effects:

These effects create long term reliability issues to the MOS based devices. TID is the damage mechanism caused by radiation over the certain period of exposition time. TID mainly affects the insulating layers such as oxides. When an ion strikes the oxides in the wafer, it may trap charges, fixed oxide charges, interface charges etc.

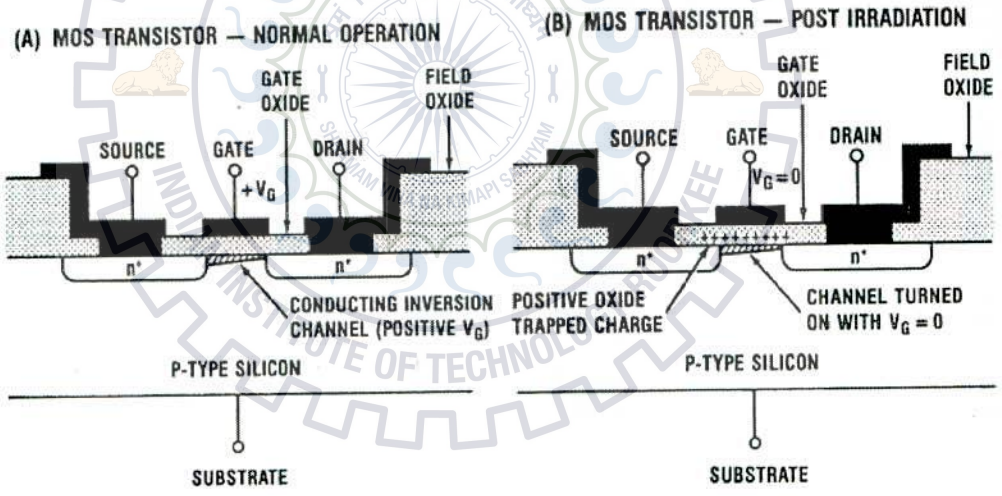


Fig 1.3: Schematic illustrating the charge trapping inside the oxide (A) Pre Radiation (B) Post Radiation.

Figure 1.3 shows the schematic of N-MOS device, with charge trapping inside the oxide after radiation. This may create permanent damage to the devices even failure. Use of high quality, ultra thin oxides minimize the charge trapping problems because of the low volume in which the charge trapped is expected to be minimized. Even if the charge is trapped, it can easily

tunnel from the oxide due to the thin width. High k-dielectric oxides are using currently to get acceptable outcomes.

The Radiation effects in the oxides first explained by [3], Figure 1.4(a) illustrates the damage mechanism caused by the radiation particle strike. The energetic particle impact on oxides, causes electron-hole pairs in SiO_2. The electrons tunnel from the oxide due to gate bias, but the holes move in the same energy level (called Hopping transport of holes) towards the interface. There the holes trapped as positive interface charges.

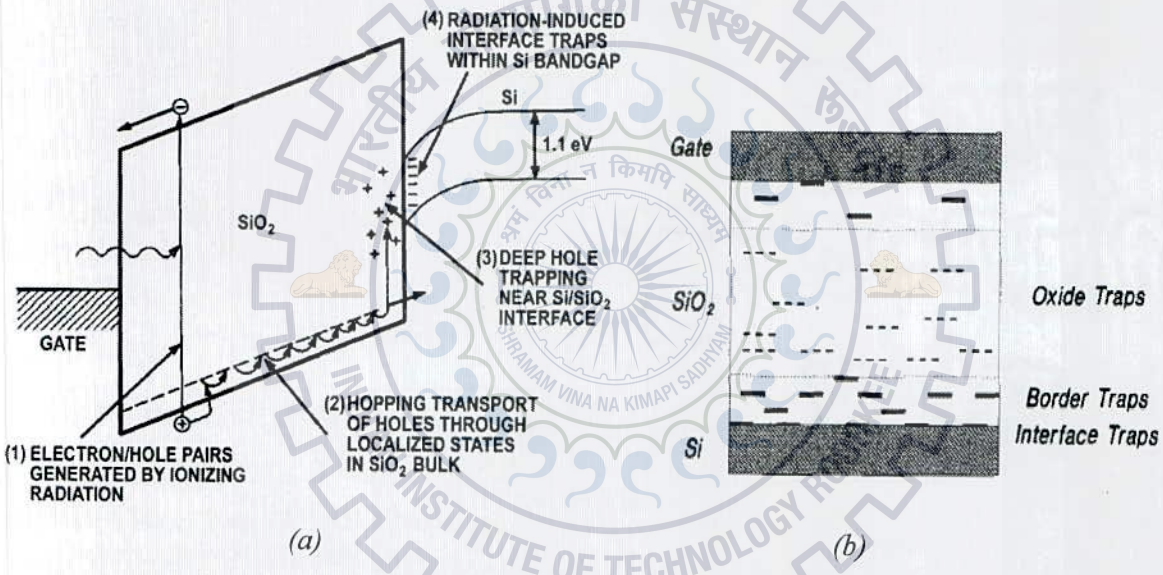


Fig 1.4: (a) Basic Radiation damage phenomenon in oxides, (b) Possible oxide trap charges.

Figure 1.4 (b) shows the various oxide traps, that can be trapped inside the oxide. Oxide traps are normal voids or recombination centers in the oxide, these are due to atomic displacement, defects in materials. Interface traps are generally caused by the work function difference between contact materials and hopping transport and silicon dangling bond defects. These traps can communicate with the channel and can affect the inversion charge. Border traps are normal oxide charges, behaves either oxide traps or interface traps depending upon the bias applied at the gate. The contact interface between border traps and interface traps can move up

and down, if the bias at the gate is changed [4]. For large values of gate voltage leads to a large amount of interface trap charge.

Overall the TID effects cause oxide traps. The consequences due to TID effects are Threshold voltage shifts, permanent change in I-V characteristics of the devices, oxide breakdown, etc. The TID effects are more serious in SOI devices, because of increased volume of oxide due to Buried Oxide (BOX). The difficulties with SOI devices are formation of back channel and large shifts in threshold voltages.

1.2.2 Single event effects:

These are the transient responses caused by the ionizing particle impact. These do not cause permanent damage to the circuit, infact causes short-time electrical disruptions in the electrical behavior of the circuit. These effects are also called as soft errors [5][6]. In recent technologies these effects are primarily due to secondary collisions of the generated carriers prier to ionizing particle impact. The generated charge can lead to a wide variety of effects, including Single Event Upset (SEU), Single Event Gate Rupture (SEGR), Single Event Functional Interrupt (SEFI), Single Event Transient (SET), Single Event Burn-out (SEB), Single Event Latch-up (SEL) etc.

- Single Event Upset (SEU) may occur in Memory units like SRAM, Flip-Flops etc. The deposited charge may flip the memory or register bits, which can not be recovered thereafter. The single ion impact may also cause Multiple Bit Upset (MBU), in dense packages.
- Single Event Gate Rupture (SEGR) occurs in power MOSFETs. The impact of heavy ion at the high voltage gate region, immediately causes the local oxide breakdown. This may lead to overheating and destruction of the gate.
- Single Event Functional Interrupt (SEFI) may occur when the ion hits the control circuitry like state machines etc. This may place the system in indefinite state, or false state so that the system cannot be brought back or even system failure.
- Single Event Transient (SET) causes problems in analog circuits. The current signal generated due to ionizing particle strike can travel through the circuit as a noise signal. This may create power issues in the design.

- Single Event Burn-out (SEB) also observed in power MOSFETs. Here the particle impact somehow forward biases the drain-substrate junction. Result in large amount of current flow and overheating at the junction.
- Single Event Latch-up (SEL) occurs in PNPN structures. The particle strike causes the latch-up condition and the circuit draws large currents.

Since the Single Event Effects (SEE) are due to the charge collection, so these are severe in bulk devices because of large volume of substrate allowing more collection of charge. SOI devices are somewhat immune to the SEE effects. People were employed the Error Correcting Codes (ECC) to detect and correct the SEE's. However, ECC circuits consume significant area on the chip and need to dealt with performance and power issues.

1.3 SEU mechanism in SRAM cell:

The charge collection due to ionizing particle impact at a sensitive location (Reverse biased P-N junction of off-state MOSFET) of the SRAM device results in a transient response in the struck node and may cause data flip by discharging that node. Figure 1.5 shows a typical static RAM cell in an on-chip memory. The cell holds the data by using the back to back inverter configuration, when the Word Line (WL) is low. That means the access transistors are off and the BL and BLBAR are decoupled from the SRAM cell. The particle strike at a node force the date transition, the disturbance may cause transition at the other node through the inverter back to back action. The transient at the second node, in turn, drives the first node toward the false state. This chain action causes both nodes to flip. Finally the cell stores the wrong value, and it can not recovered until rewriting the the cell. If the particle influences the adjascent SRAM cell of the memory chip, then Multiple Bit Upset's may occur, this is the case in real applications.
Soft errors are also caused by the impact on bitlines. During the read operation, a bitline is discharged by a small current from a memory cell. The data bit is read as a "0" or "1" based on the voltage differential developed on the bitline during the cell access period. This voltage differential is disturbed if a particle strikes close to a diode of an access transistor of any of the cells on that bitline.

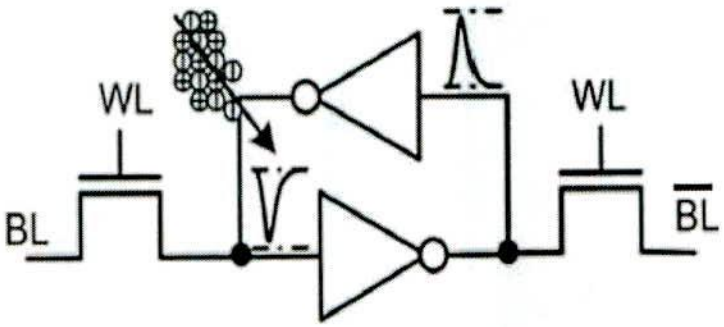


Fig 1.5: SRAM cell with voltage flipping due to charge collection [7].

The amount of charge collected depends on many parameters such as LET (Linear Energy Transfer), strike location, angle and range of the incident particle, charge of the particle, atomic and mass numbers of the particle etc. This study deals with the radiation sensitivity of SRAM cell for different LET's. The term linear energy transfer (LET) is frequently used to describe the energy loss per unit path length of a particle as it passes through a material. As a high-energy ion passes through a material, it loses energy by excitation and ionization of atoms. The amount of energy that an ion deposits per unit depth in a material is given by its stopping power. The mass-stopping power is defined as the linear energy transfer, LET, and is given by

$$LET = -\frac{1}{\rho}\frac{dE}{dx}$$

where ρ is the density of the material and dE/dx is the rate of energy loss in the material. LET has the units $MeV\text{-}cm^2/mg$. The integral of LET over path length gives the total deposited energy. LET threshold is defined as the minimum LET at which the charge collected by the circuit can flip the actual stored voltage into wrong state.

Critical charge (Q_{crit}) is generally described as the least amount of charge that must be collected at the circuit node, due to ionizing particle srike at the sensitive parts of the memory units, in order to change the voltage value of the circuit [8]. It can be calculated by integrating the current at the struck node over flip time. In recent technologies the critical charge is the metric for obtaining the radiation sensitivity of the microelectronic devices and also useful parameter in Radiation hardening circuit design.

1.4 Sources of Radiation:

The vulnerability of microelectronic devices to radiation particle strikes largely depends on Radiation harsh atmosphere and operating surroundings. Especially in military and satellite applications, the radiation intensity is unbearable. Due to the aggressive current technology scaling, terrestrial electronic components are also facing severe degradation in its characteristics. During chip packaging or fabrication process, the components may face ionizing particle strikes. This is due to presence of alpha particles in the chip volume. Solar particle events and mass coronal ejection and solar flares result in large amount of ionizing particle which may cause severe degradation to the devices.

The sources of ionizing particles are as follows.

- Atmosphere largely abundant of Cosmic rays [9], those contains wide range of ionizing particles like, proton contribution 85%, alpha particles contribution14% and 1% heavy ions, along with ultraviolet and X-ray radiation.
- Solar particle events consist of a large flux of ionizing particles such as heavy ions and high-energy protons are main contenders in the flux produced by solar particle events. And those are the main radiation damage particles in modern electronic devices when accompanied with ultraviolet radiation and X-rays.
- The geomagnetic field of Van Allen belts consist protons and electrons. The radiation particle flux density at the outer atmosphere of earth is largely depends on weather conditions and magnetosphere conditions.
- Due increased density of chip and even electronic system, the particle strikes at other components also would be a problem.
- Nuclear reactors eject significant amount of gamma and neutron particle flux to the surroundings.
- The dangerous impulse, short range shock waves from nuclear explosions may contain intense pulses of entire electromagnetic spectrum.
- Nuclear explosions produce a short, extremely intense surge of the entire spectrum of electromagnetic radiation.
- Ionizing particles and solar flares from atmosphere, even the fabrication and defect causing

emitted by radioactive impurities that are present in the integrated circuit (IC) package and in the IC itself.

1.5 Problem Desription:

My work of inerest is to examine the radiation sensitivity of multigate devices like FinFET's. The aggressive technology scaling made the electronic designs volnurable to ionizing particle events, so there is need for the radiation hardened circuit design. For this the study of radiation affects like TID or SEE is more important. We analyzed the Single Event Effects of both bulk and multigate devices.

The whole work has been divided into teo parts

1. Making of bulk SRAM cell using visualTCAD tool and Study of SEE in bulk SRAM cell and finding the critical charge.
2. Design of FinFET devices and it's performance followed by SRAM cell creation. And radiation study of the cell to characterize the critical charge.

1.6 Thesis Organisation:

Chapter 1: First chapter is introduction gives the background of the radiation. Radition damage mechanisms, radiation affects like TID and SEE, sources of radiation.

Chapter 2: The software used for the simulations, models used device and radiation. And working of the tools.

Chapter 3: 24nm-FinFET device making and bench marking followed by FinFET SRAM cell creation.

Chapter 4: Radiation affects on FinFET device and SRAM cell. Characterisation of critical charge (Q_{crit}).

Chapter 5: 90nm-Bulk SRAM cell creation and then irradiation of cell to analyze the behavior.

Chapter 6: Conclusion and future scope.

2. SIMULATION SETUP

2.1 Setup for Device Design:

The software we have used is VisualTCAD. It contains veriety of tools for device making. GDS2MESH for 3D structures, VisualParticle for radiation effects, Klayout for layout drawing, VisualFab etc. And it uses the GENIUS device simulator. User defined card file is taken as input in the GENIUS code. Each line is distinguished from other lines by the keyword at the beginning, and represents a particular statement. In card description the letters are case sensitive, so we can use upper or lower cases for keywards, parameters, enumerate strings, parameters, keywards. Flexibility with GENIUS code is, we do not need to type the full name of keyward. We can use sufficient unequaled charecters for the identification. But the input strings defined by user are case sensitive.

The simulations are carried out by GENIUS device simulator. The fundamental solver used by GENIIUS is Level 1 Drift-Diffusion (DDML1). The principal objective of DDML1 is to solve the electron and hole continuity equations and primarily Possion's equation. However it runs with approximations like

- Elastic nature of all internal collisions.
- During collision, there is no change in band gap.
- Throughout simulation the lattice and Carrier temperatures are same and maintained in equilibrium.
- The driving force gradient should be as small as possible.
- Carrier speed is very much less than light speed.
- No consideration of carrier degenerate.

The advantage of DDML1 is simple, runs pretty fast and robust. However, DDML 1 can't describe some physical phenomenons like quantum effects and velocity overshoot etc. The complex mechanisms and newer degradation characteristics can be included by the comprehensive mobility models.

GENIUS supports many mobility models including low field and high field behaviors. The carriers are almost in equilibrium in low field behavior with the lattice. The primary parameters are impurity scattering and phonon scattering for the low field mobility. Both allows the mobility to decrease. These scattering phenomenons in turn depends on lattice temperature, the low-field mobility is function of lattice temaperature also.

Instead of increasing, the carrier mobility decreases with high electric fields. At high electric fields, the increase in carrier energy result in large number of scattering phenomenons. At some point the drift velocity of carriers doesn't increase linearly with increase in electric field. But it climb up slowly. So the drift velocity reaches it's saturation, there after it remains in same value even with oncrease in electric field. It is named as saturation velocity.

GENIUS uses a wide variety of mobility models such as Masetti analytic model, Philips Mobility Model, Lombardi Surface Mobility model, Lucent High Field Mobility model and Hewlett-Packard High Field Mobility model. Out of all, the Lucent High Field Mobility Model has been used. It is a comprehensive model includes almost all effects in MOS simulations. It considers carrier-carrier scattering, donor-acceptor scattering and carrier screening. It uses an empirical model for MOS device inversion layer mobility to incorporate surface scattering properties. The mobility parameters used by this model are

$\mu_{Lattice,n}$, is lattice scattering electron mobilities.

μ_{D+A+P}, is the carrier mobilitiy to consider acceptor (A), donor (D) and carrier scattering and screening (P) effects.

μ_b, mainly to incorporate ionized impurity scattering. It depends on the body doping concentration, named as bulk doping dependent mobility.

μ_{ac}, It is the inversion layer mobility to consider acoustic phonon scattering. This mobility strongly depends on lateral electric fields in the inversion layer. This is due to quantum confinement in the potential well at the interface.

μ_{sr}, Accounts for surface roughness degradation mobility in the inversion layer. This component also show strong dependence on lateral electric field.

The final carrier mobility obtained by combining all the components using Matthiessen's rule. And for velocity saturation calculations, this model uses the Caughey-Thomas model. This Lucent mobility model is complex and accurate compared to other models, best suited for MOS device simulations. However, it requires more computation time. At the same time, it is less numerically stable. The genius code also uses the models like Band Structure model, Energy Balance equation, Schenk's Bandgao Narrowing model and the recombination mechanisms considered in GENIUS are Shockley-Read-Hall (SRH), Auger, and direct recombinations. The total recombination is considered as the sum of all.

2.2 Setup for Radiation Environment:

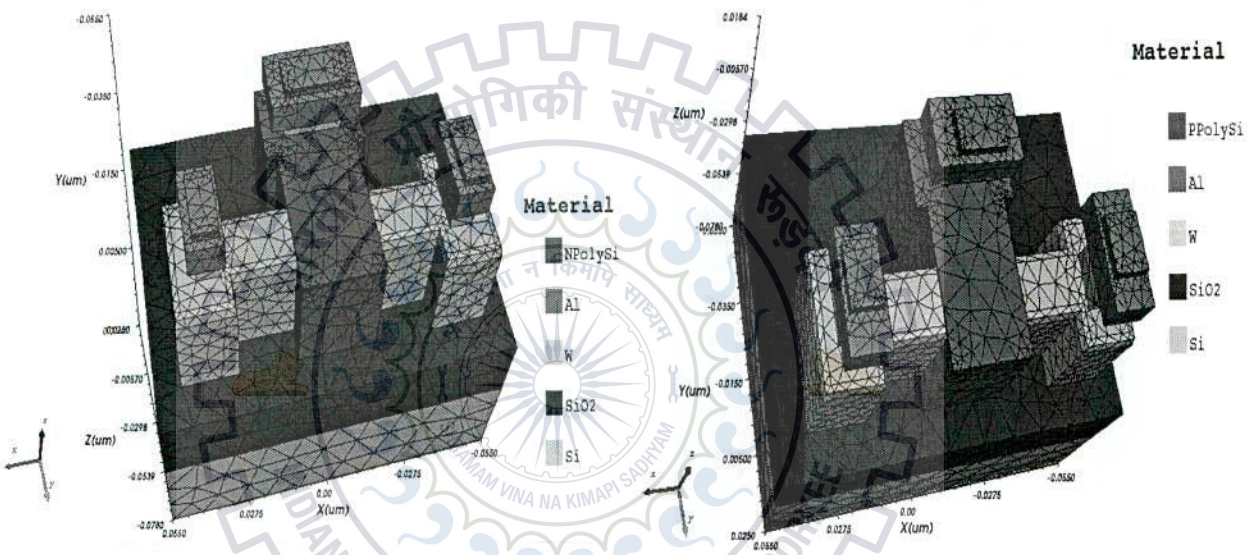
The tool used here is VisualParticle. It creates the radiation environment to irradiate the structure. It is a GUI based tool offers wide range of radiation particles that covers entire periodic table. The Radiation simulation is carried out by GSEAT tool, similar to GENIUS in device simulations.

For the single event effect (SEE) study, we have used the tool GSEAT (Geant-Based Single Event Analysis Tool). It uses a computer code based on Geant4 gudelines and Monte carlo code for the transmission of particles through objects. It takes the 3D device generated by GDS2MESH tool in other format suitable for radiation environment effects. This format is named as GDML file (Geometry Description Markup Language). This file contains all the information about type of particle, it's energy and direction of track and some other parameter. It also includes the device information like material used and geometry etc. GSEAT supports various particle events such as alpha, gamma, X-rays, neutron, proton and heavy ion impacts with wide range of energies. The GSEAT simulates the radiation particle impact interms of how much energy deposited through the matter, and information can be saved in simple text file and xml file (spread sheed). The event files can be used by GENIUS, for the complete simulation of device including with radiation. And GSEAT also use best guess for the appropriate radiation physics. It uses Boson physics, Lepton physics, Hadron physics, Neutron physics Decay physics and Ion physics.

3. DEVICE MAKING AND SIMULATION

In this chapter we illustrated the FinFET device, SRAM making and simulated to obtain the normal operation.

3.1 FinFET Device Simulations:



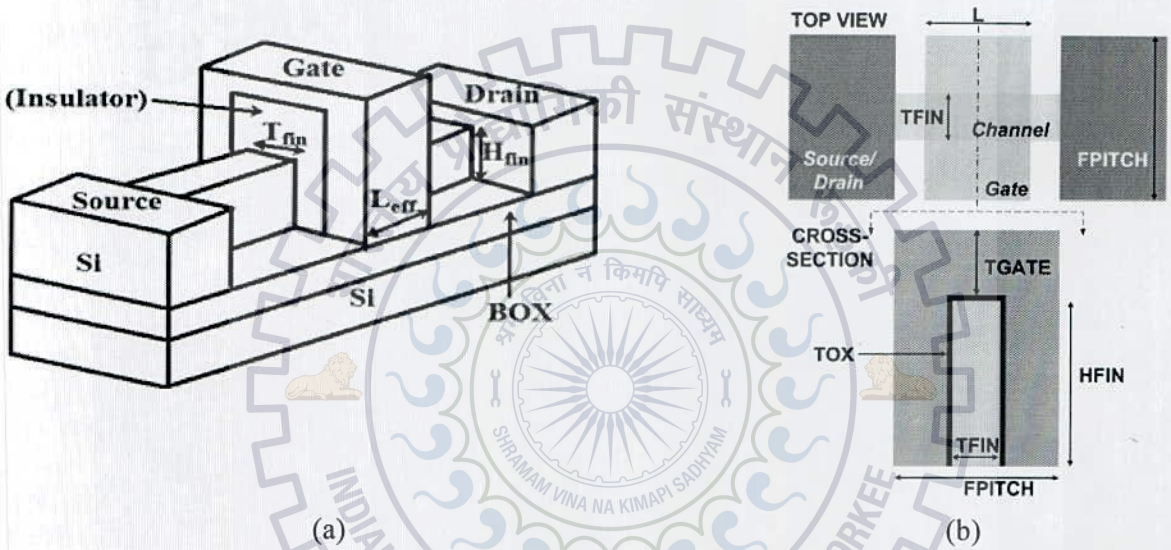
(a) (b)

Fig 3.1: 3D structure of FinFET's with meshing (a) N-FinFET (b) P-FinFET

Figure 3.1 shows the 3D view of the made FinFET's using tool GDS2MESH. The parameters used for the device are tabulated in the table 3.1. We designed 24nm technology SOI-FinFET [10][11] with fin height 30nm, fin thickness 15nm and oxide thickness 1.1nm. Here we have used p-poly and n-poly as pfet and nfet gates respectively. The work function of p-poly is 4.85 and that of n-poly is 4.4.

Table 3.1: FinFET parameters.

Gate length	24nm
Fin thickness(TFIN)	15nm
Fin height(HFIN)	30nm
Fin pitch	60nm
Oxide thickness	1.1nm
Body doping	$1 \times 10^{16}\ cm^{-3}$
S/D doping	$1 \times 10^{20}\ cm^{-3}$



(a) (b)

Fig 3.2: (a) 3D view of FinFET (b) Top and cross sectional view.

Table 3.2: Simulated Device Results.

	S sat (mV/dec)	V_t lin	V_t sat	I_{off} (nA)
P	88	-0.25V	-0.22V	-1.42
N	83	0.28V	0.24V	1.87

Table 3.2 shows the fet parameters extracted from figure 3.3. From the table the sub threshold slope and I_{off} are acceptable for the device operation. NFET threshold voltage for linear region operation is 0.28 and for saturation is 0.24 and those values for PFET is -0.25 and -0.22

respectively. Figure 3.4 shows the I_d-V_{ds} characteristics of both the devices. Both the devices have same range of I_{on}. NFET has I_{on} around 70μA and PFET -50μA.

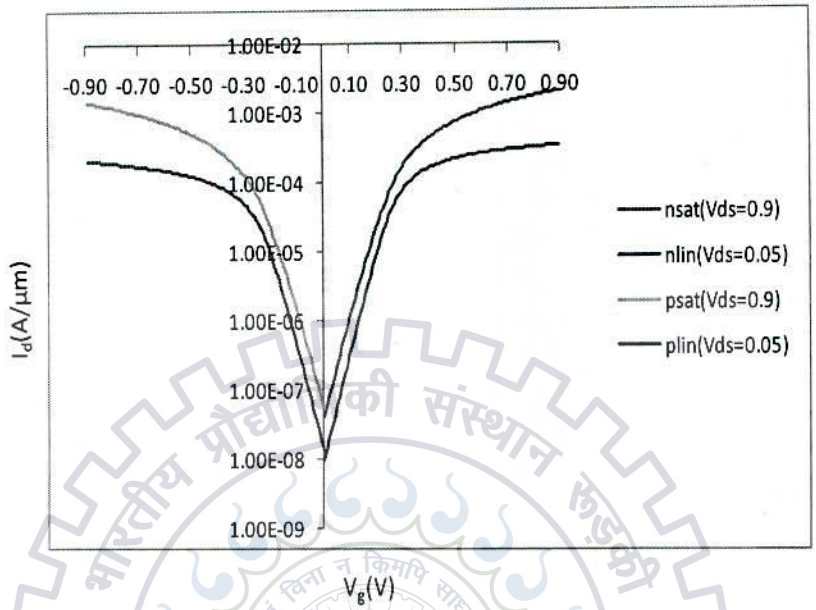


Fig 3.3: I_d-V_g characteristics of N and P FinFETs.

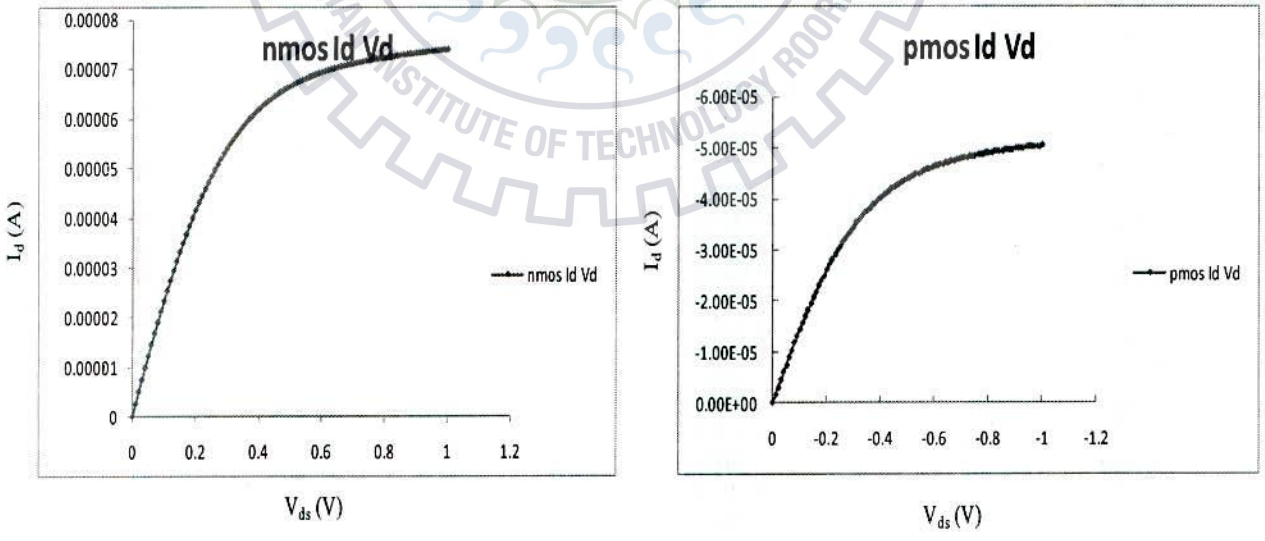


Fig 3.4: I_d-V_{ds} characteristics of N and P FinFETs.

3.2 Cell Creation:

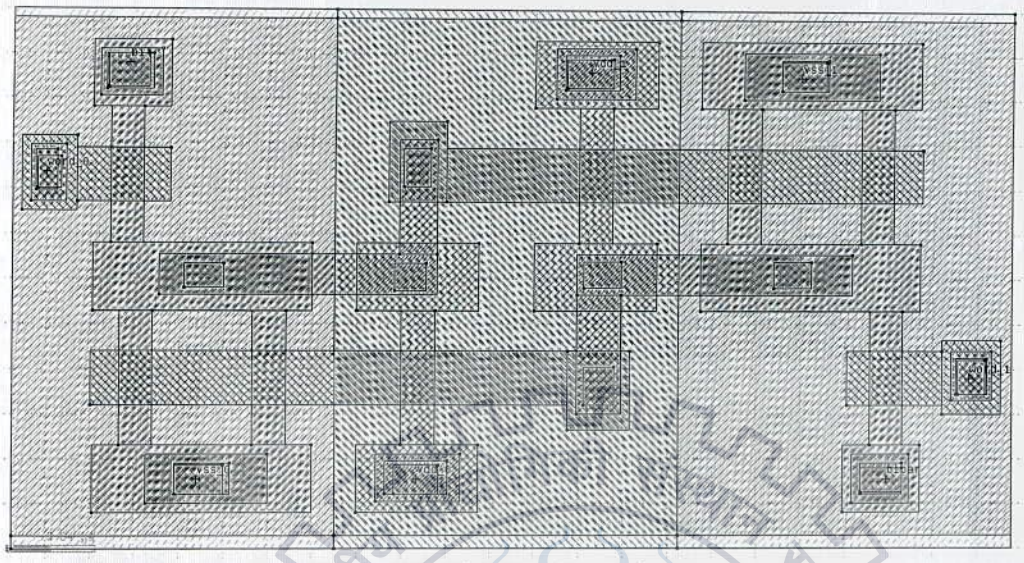


Fig 3.5: FinFET SRAM layout.

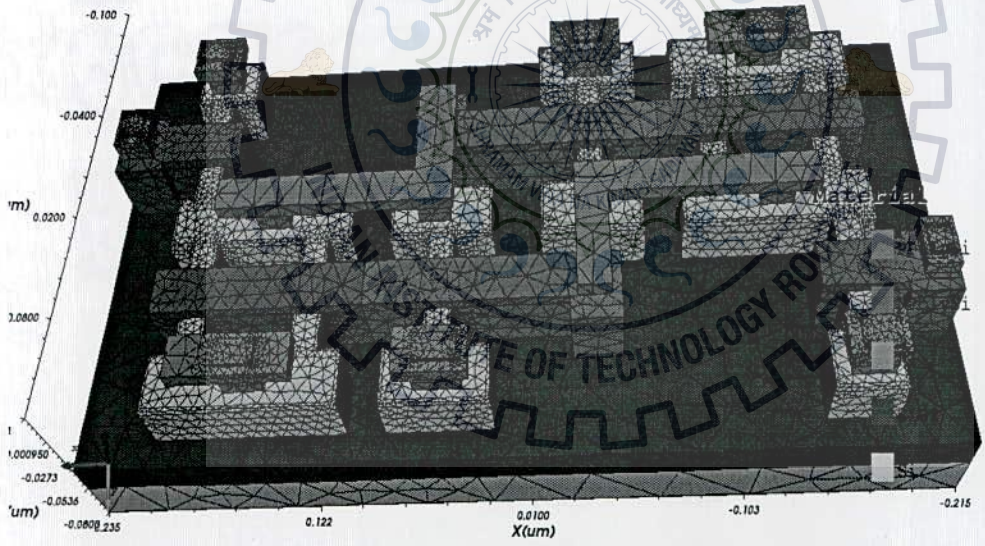


Fig 3.6: 3D view of 6T-FinFET SRAM cell.

The 6T-FinFet SRAM cell has been made and observed the results. Figure 3.5 shows the SRAM layout made by the tool klayout. This layout can be used as a mask file for 3D device making. Si substrate of 30nm thickness with P-type doping of $1 \times 10^{15}\ cm^{-3}$ is used. The source/drain dopings N and P-FETs is $1 \times 10^{20}\ cm^{-3}$ with channel doping $1 \times 10^{16}\ cm^{-3}$ is

used. Gate oxide thickness of 1.1nm is used. The SRAM cell has been sized with, the *cell ratio (CR),* equal to $\frac{W_1}{W_5}$ (fig 3.7), of 2 for appropriate read operation and the *pull-up ratio (PR),* equal to $\frac{W_4}{W_6}$, of 1 for appropriate write operation.

First the working of SRAM cell has been verified by writing data into the cell. The results are shown in figure 3.8. So the Figure 3.8 verifies that constructed SRAM cell works as per the requirement.

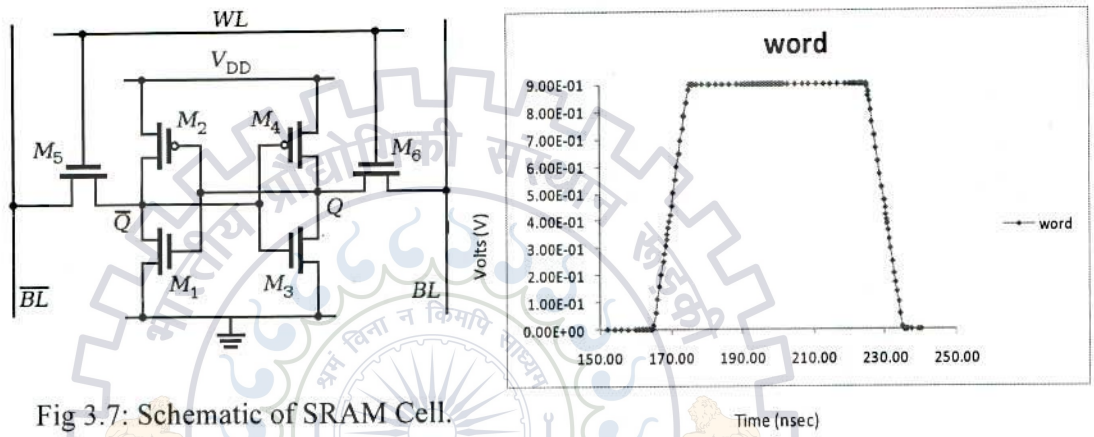


Fig 3.7: Schematic of SRAM Cell.

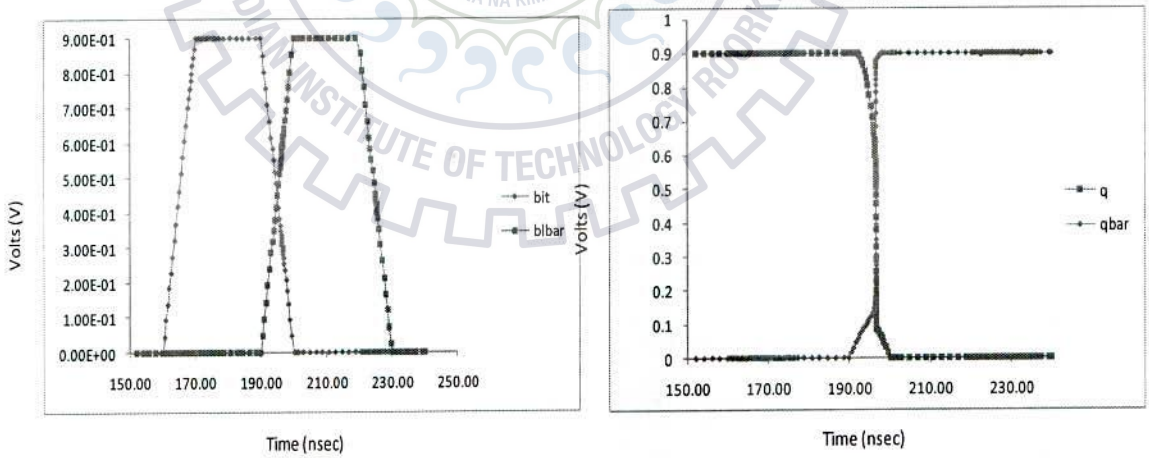


Fig 3.8: Wave forms showing operation of SRAM cell.

4. RADIATION EFFECTS ON FINFET SRAM CELL

In this chapter we discuss the radiation behavior of FinFET device followed by SEU sensitivity of FinFET SRAM cell. For this we have used various energy particles with different LET's.

4.1 Radiation behavior of FinFET device:

The designed 24nm technology FinFET is irradiated with different ions and the response is studied. Here the N-FinFET device is irradiated at the drain side and figure 4.2 shows the observed current pulses due to heavy ion impact. Figure 4.1 shows the irradiated n-FinFET device. The red lines indicate the secondary carriers and the blue line indicates the heavy ion track. During irradiation the drain and gate terminals connected to fixed voltages and source is connected to ground. Figure 4.2 shows that the drain current increases sharply with in the small instant of time due to large amount deposition and then decreases as the time proceeds. The behavior of the drain current can be explained in two ways [12]. First one is the case where the heavy ion crosses the drain substrate junction. Here the charge collection is through funneling effect, in which initially the charge collection is very fast (drift) due to high electric field, followed by diffusion. The track conductivity is the key parameter in funneling. Second one corresponds to heavy ion track not crossing the drain substrate junction. Here the charge collection is due to the charge gradient and can be explained by simple diffusion collection laws. In second case the current pulse is retarded and expanded due to diffusion collection. Many reporters have modeled the current behavior and the best model used by many simulators is

$$I = \frac{Q}{\tau_f - \tau_r} \times \left(\exp\left(-\frac{t}{\tau_f}\right) - \exp\left(-\frac{t}{\tau_r}\right) \right)$$

The above equation is the modeled current equation famously known as double exponential equation with rise and fall times. Where τ_f is fall time and τ_r is rise time.

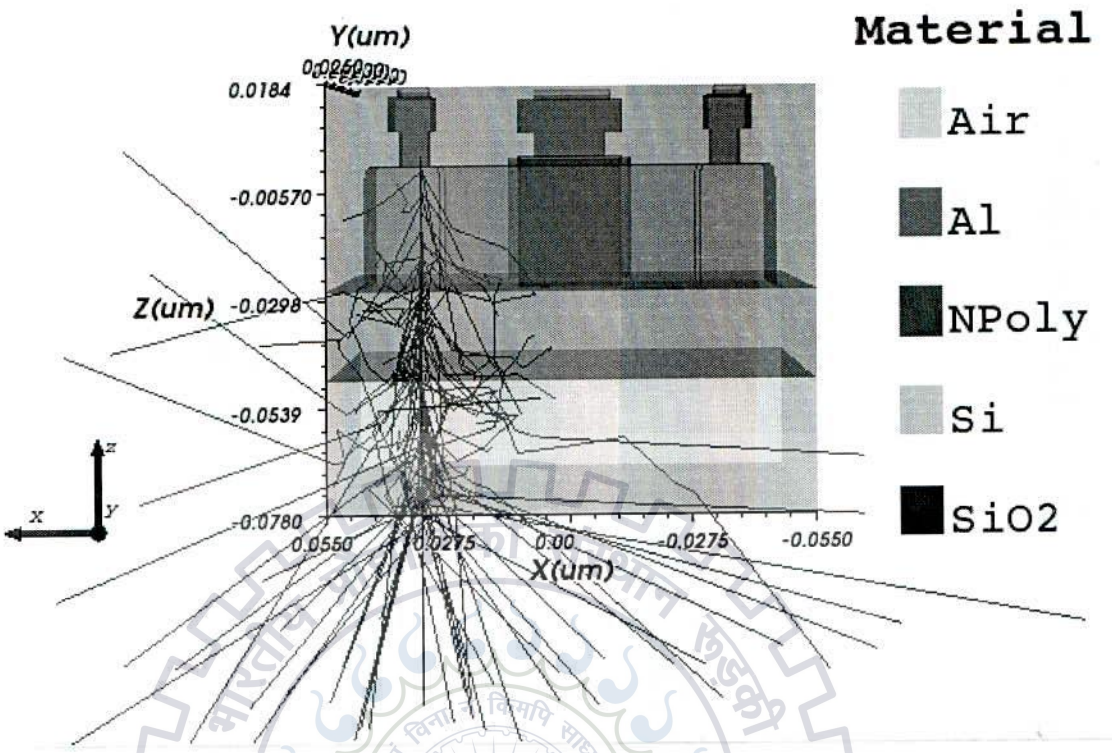


Fig 4.1: Heavy ion track upon irradiating the N-FinFET.

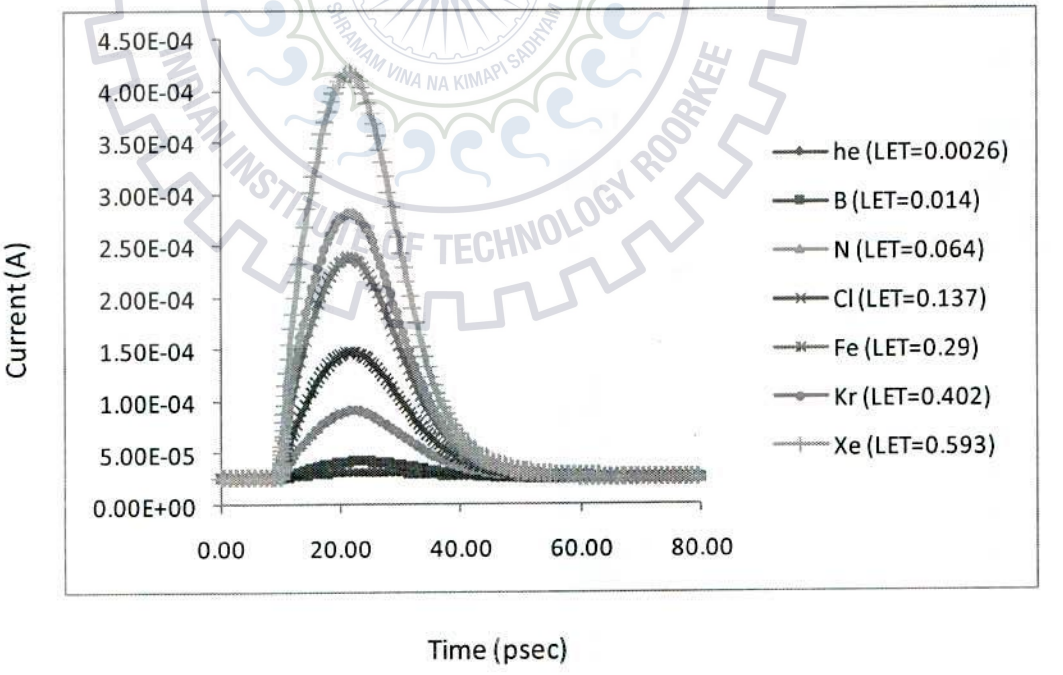


Fig 4.2: The current pulses in the device due to heavy ion impact.

4.2 SEU Simulation of FinFET SRAM cell:

The cell is irradiated with heavy ions of different energies at the drain region of off state NFET (node Q) [13][14]. The heavy ion hit at the location (X=-0.04, Y=0.02 and Z=0.018 μm) with different angles along with normal incidence. First the data is written into the cell, so the cell is in data hold state, holding 1 at node Q and 0 at Q_{bar}. Fig 4.3 shows the schematic of the SRAM cell and strike location. The ion strike at node Q results in discharging of that node due to large amount of charge collection. Fig 4.4 shows the transparent structure of 3D SRAM cell and the red lines indicate the secondary electron-hole pair generations [15] due to heavy ion strike. Since the Q holds high value, the M_1 and M_4 are on, M_2 and M_3 are off with access transistors turned off.

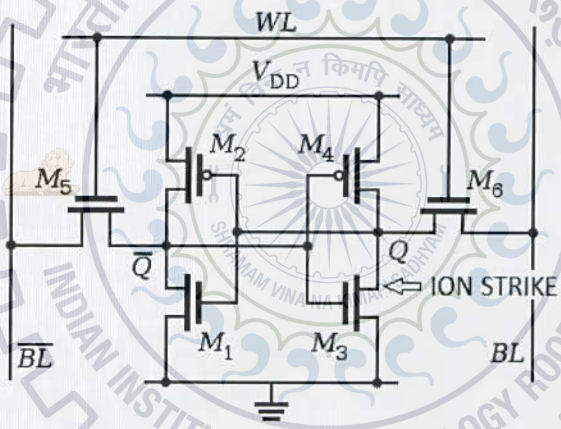


Fig 4.3: Schematic of SRAM cell showing ion strike.

Now the problem here is on which basis the SRAM can be characterized. That means when the cell gets flipped and when it won't. Researchers proposed that, the LET can be solely used to describe the upset probability of the SRAM cell for the technologies above 180nm.Due to higher density of cells for the technologies below 180nm and reduced on-chip capacitances, the Soft Error Rates (SER) in the memory units have risen accordingly. The storage nodes are too close, that the ion strike at a particular node can affect the adjacent nodes. The adjacent nodes can also draw sufficient charge to induce data flips. So the better criteria would be critical

charge (Q_{crit}) [16]. So the SRAM is irradiated with different ions and the charge collected at the sensitive nodes is estimated. We also analyzed SEU response for angled incidences. If the ion hits with an angle, then the charge collection is more due to barrier lowering [17].

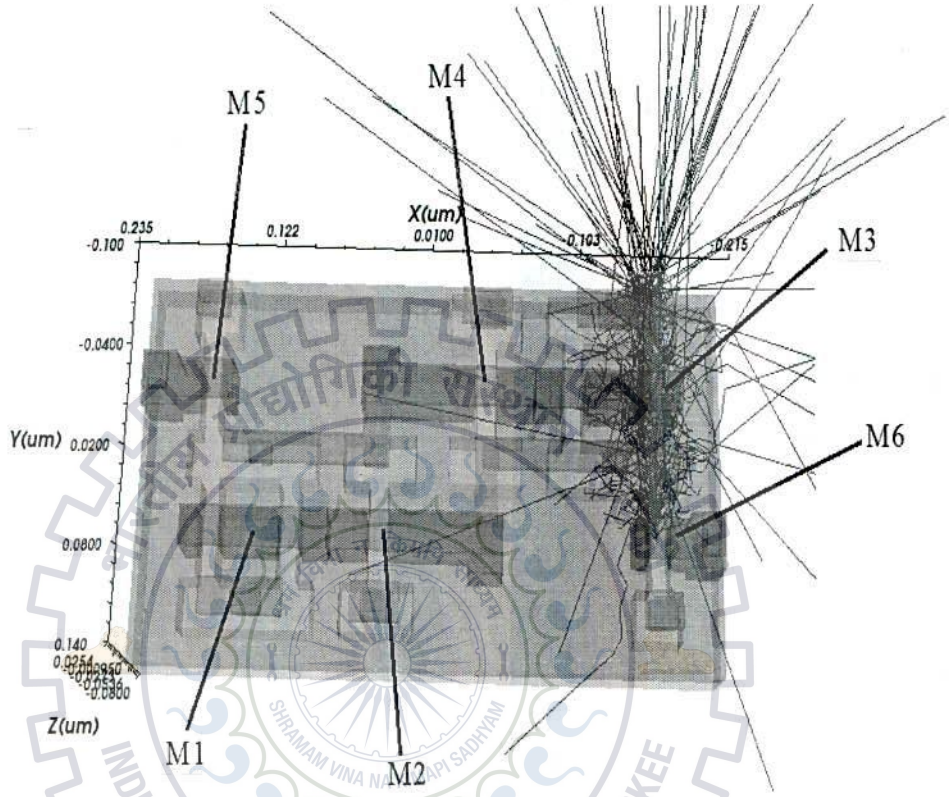
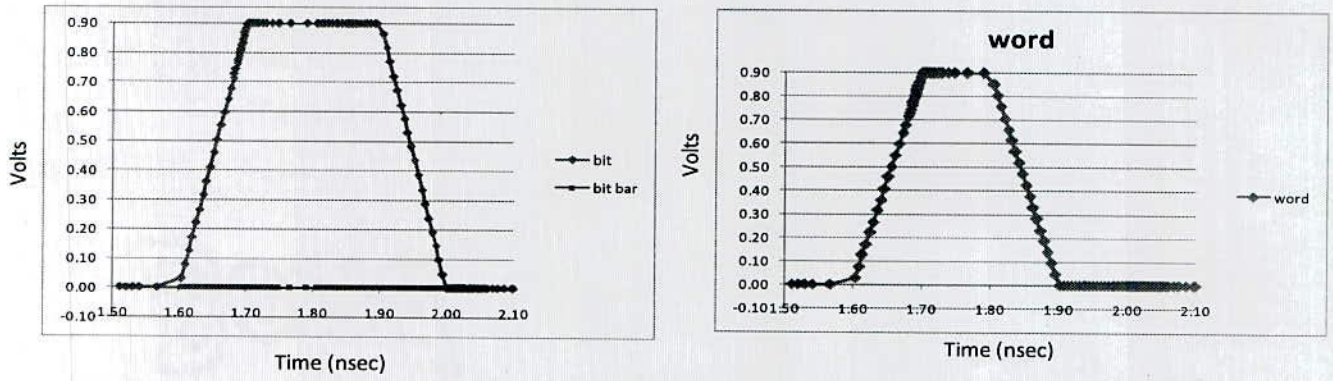


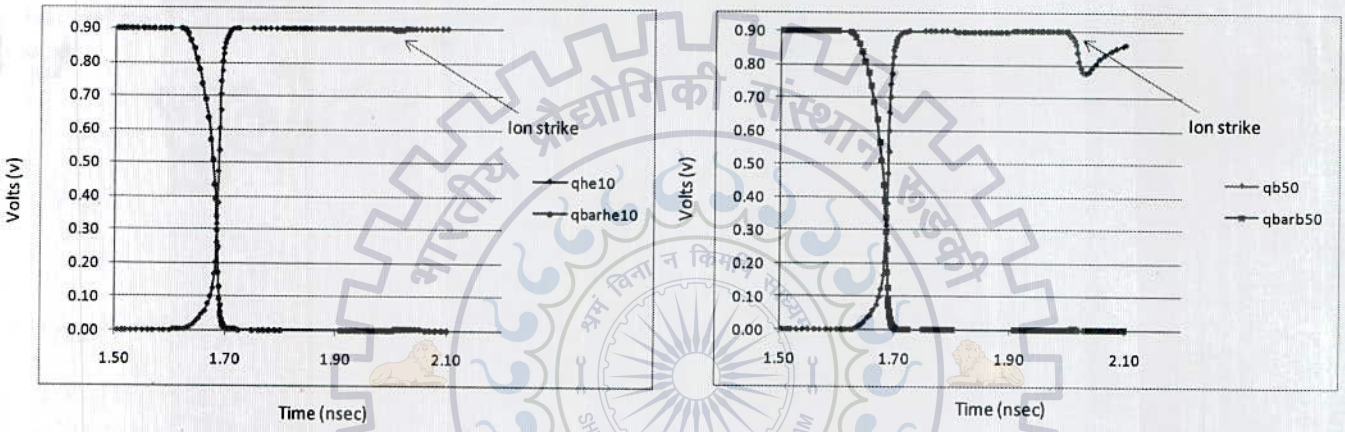
Fig 4.4: Electron-hole pair generation along the ion track.

4.3 Node voltage response with normal incidence:

The cell is irradiated with different ions such as $^{4}He_{2}$, $^{11}B_{5}$, $^{14}N_{7}$, $^{35}Cl_{17}$, $^{56}Fe_{26}$, $^{84}Kr_{36}$, $^{131}Xe_{54}$, $^{197}Au_{79}$ etc. The direction of track is normal at the location (X=-0.04, Y=0.02 and Z=0.018 μm). Since the cell is SOI substrate, the charge collection is due to diffusion only. Because, in normal incidence the ion does not meet the junction throughout its track, since there is no junction underneath the drain due to BOX layer. So the current curve obtained is a time dispersed curve with less magnitude. Figure 4.5 shows the inputs and output responses due to heavy ion impact. The word line is activated at 1.6 nsec to write the data into the cell and turned off at 1.9 nsec. The ion hit the cell at 2 nsec.

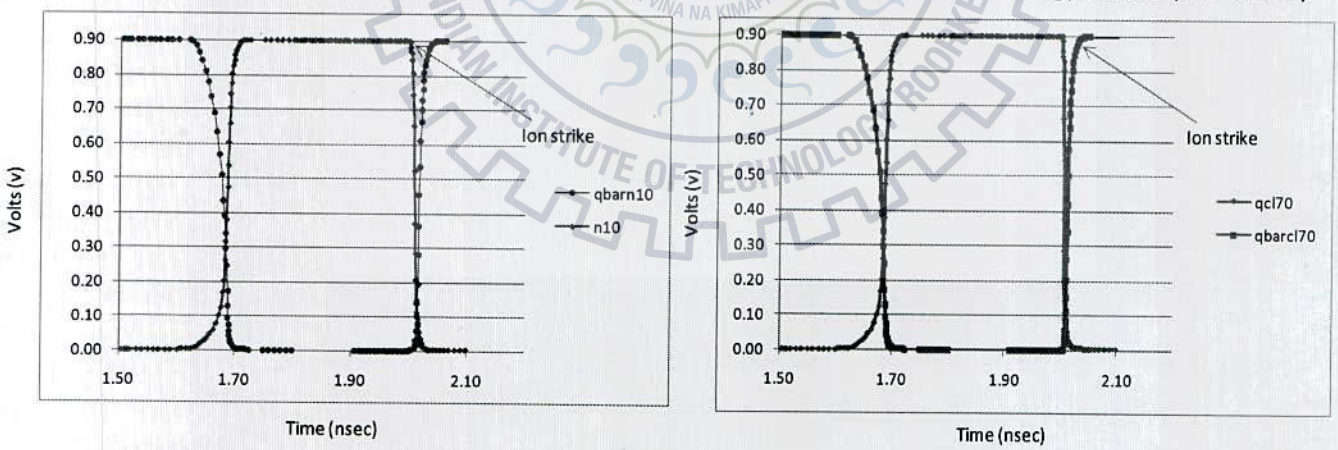


INPUTS



Helium ion strike with energy 10MeV (LET=0.0026)

Boron ion strike with energy 50MeV (LET=0.014)



Nitrogen ion strike with energy 10MeV (LET=0.065)

Chlorine ion strike with energy 70MeV (LET=0.137)

Fig 4.5: Node voltage responses after heavy ion impact.

4.4 Transient Current Response in the Cell:

Figure 4.6 shows the simulated results of the SRAM node voltage response. From the figure the node flips when the LET crosses 0.065. The flip time is the duration data flipping. We can see that the flip time decreases as the LET increases. From figure 4.6, for xenon ion impact the flip time is low compared to other ion impacts. And the LET increases the flip time increases. So the ions with more LET can flip the storage nodes easily. For the data to flip the collected charge must compensate with the actual charge present at the struck node, plus the charge supplied through the pull-up (P-FET) device during flip time. To achieve this, the electron-hole pair generation must be very high to boost the diffusion and also near to the drain contact. If the carriers are generated far from the drain contact, it will take more time and more distance to travel. Meantime, the carriers may diffuse into the substrate or the pull-up device pulls the node to its original value. So the SEU response depends on so many parameters like energy of ion, LET, charge of ion, atomic number, mass number, carrier collection time, strike location, strike angle, supply voltages etc. So the simulation of SEU is difficult that, we need to consider each parameter carefully to get exact outcomes. And these SEU events become worse for the current technology trends.

From the figure 4.7, the width of current pulse is broad for the ions with less LET and the peak value is also less compared to the more LET ion strikes. This is because the gradient of charge is less for low LET ion impacts, so the generated charges diffuse slowly compared with the high LET ion impacts, Results in slow discharge of the struck node. This cause the flip time to increase and thereby increase in power dissipation. One more thing observed is, at the peak the width is narrow and become broad afterwards. This also due to charge gradient, initially the charge is more and gradually decreases as the time proceeds. So the width of the current curve less means lesser probability of data flipping. From figure 4.7, the xenon ion impact produced more charge and the curve is steeper at the peak and reduces gradually. For other ion impacts also the curve is steep but not as steep as the xenon curve. For boron and helium ion impacts, the current curve has no falling, since the peak charge is very less to create sufficient charge gradient and took more time to diffuse.

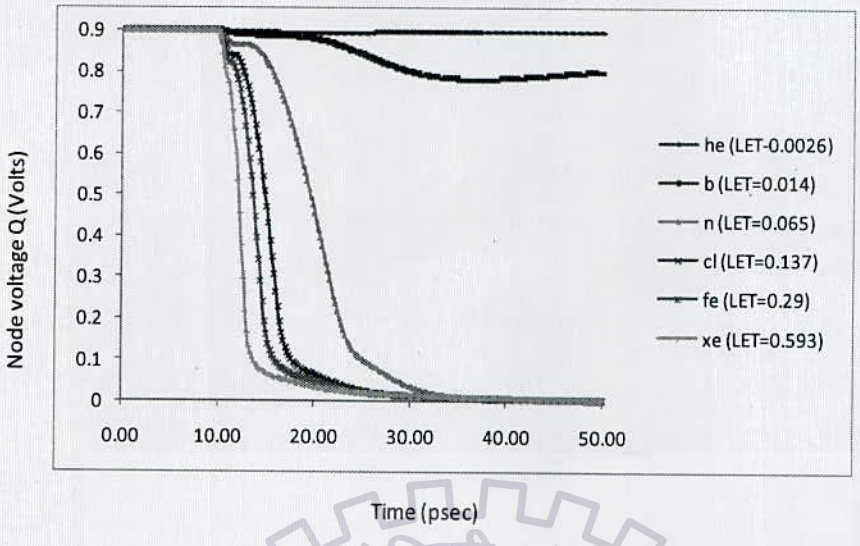


Fig 4.6: Node voltage response.

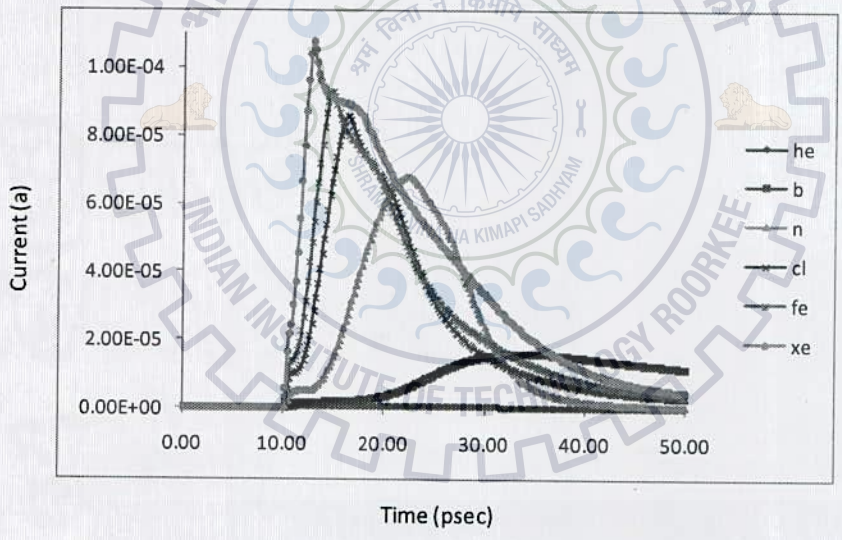


Fig 4.7: Transient current pulses at the struck node.

Now the calculation of critical charge involves the integration of the current pulse over flip time. Finding the flip time is tricky. It is exactly defined as the time between the starting of charge generation and the time at which the secondary carrier density equal to the body doping density. It is usually in the orders of 1psec.

The charge collected can be calculated by

$$Q = \int_0^{T_f} I_d(t)\, dt$$

where $I_d(t)$ is the time-dependent drain transient current and T_f is the flip time.

Table 4.1: SEU response of the cell with different ion impacts.

ION	Energy (*MeV*)	LET *(MeV-cm²/mg)*	Charge collected *(coulombs)*	Effect
$^{4}He_{2}$	10	0.0026	-0.013f	No Upset
$^{11}B_{5}$	50	0.014	-0.27f	No Upset
$^{14}N_{7}$	10	0.065	-0.84f	Upset
$^{35}Cl_{17}$	70	0.137	-0.97f	Upset
$^{56}Fe_{26}$	70	0.29	-1.09f	Upset
$^{84}Kr_{36}$	100	0.402	-1.2f	Upset
$^{131}Xe_{54}$	200	0.593	-1.49f	Upset
$^{197}Au_{79}$	300	0.811	-1.75f	Upset

The SEU response of the cell with different ion impacts are analyzed and tabulated in table 4.1. The table shows the ions of energies and LET's that those ions can deliver and the collected charge which causes upset or not. The cell gets flipped when the LET crosses 0.065 *(MeV-cm²/mg)*. The critical charge is found to be -0.84fC.

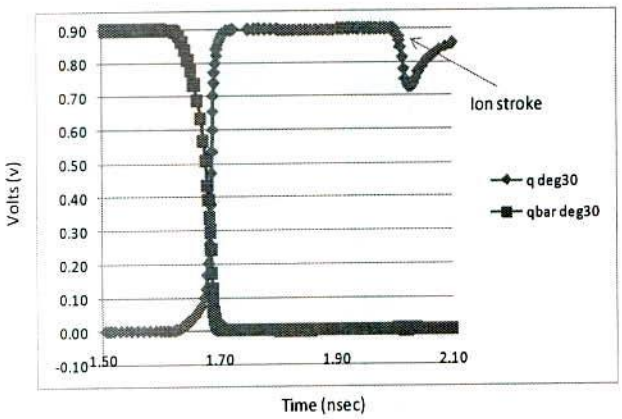
4.5 Heavy Ion Impact with Different Angle of Incidences:

The angled heavy ion strike is a different mechanism here in SOI substrates. The ion strike away from the source region doesn't cause many problems. If the ion strikes towards the source region, the charge collection will be more at the drain contact. This is due to barrier lowering. Since the ion impact yields large amount of hole concentration in the body. So the body potential gets slightly increased, allowing the source and body junction to forward bias. Comparatively some charge from source can be collected at the drain contact. If the ion strike is more towards the source region more will be the collected charge at the drain region. Talking about the different mechanism in SOI substrates, the charge collection is due to funneling effect. Since the ion crossed the drain substrate junction.

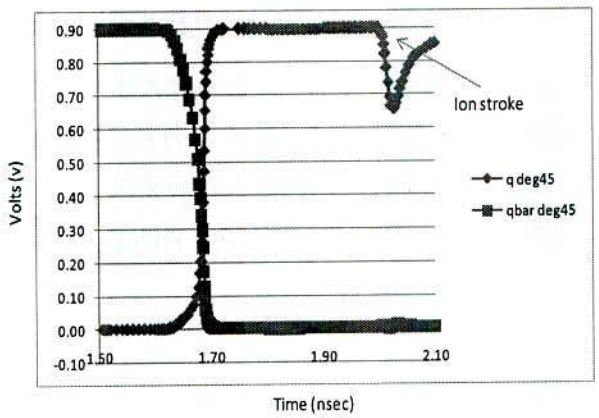
We have taken the boron ion with energy 50 *MeV* , which can produce LET equal to 0.014 causing no upset with normal incidence. Now the cell is irradiated with boron ion with different angles. The results are simulated and tabulated in the table 4.2. From the table, the collected charge is increasing with the increasing angle towards source. The upset occurred at the angle 80^{o} towards source region.

Table 4.2: SEU response of the cell for angled incidences.

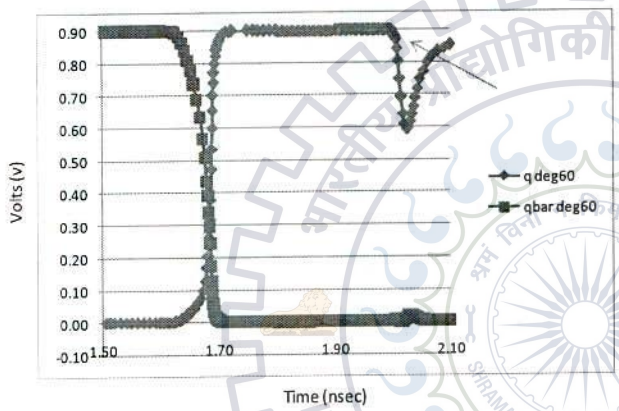
Angle	Charge collected *(coulombs)*	Effect
30^{o}	-0.37f	No Upset
45^{o}	-0.5f	No Upset
60^{o}	-0.604f	No Upset
70^{o}	-0.67f	No Upset
80^{o}	-0.93f	Upset



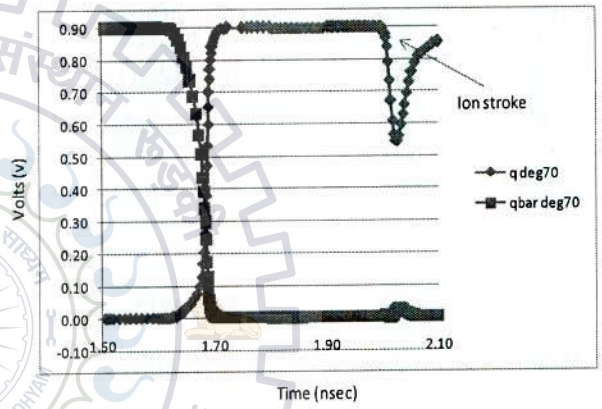
30° towards source



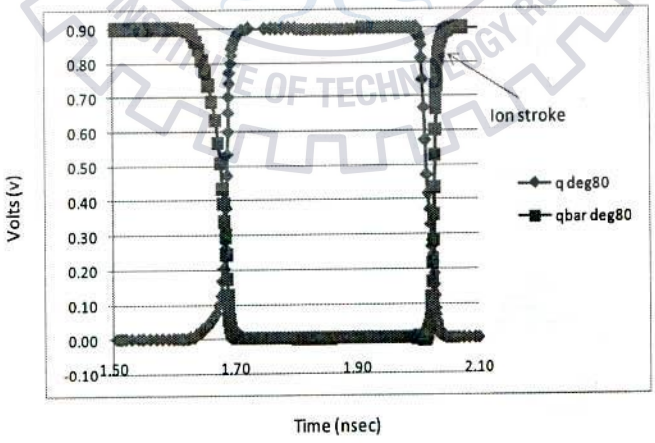
45° towards source



60° towards source

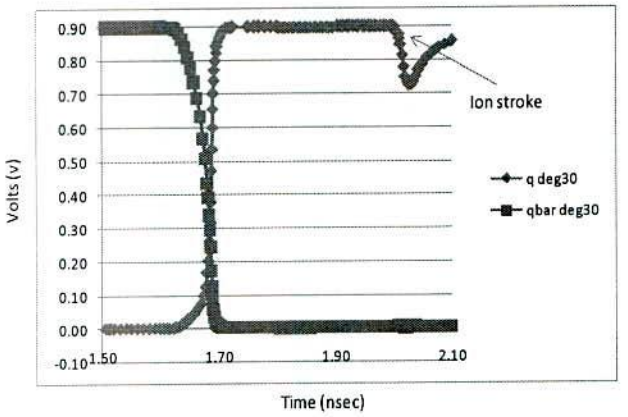


70° towards source

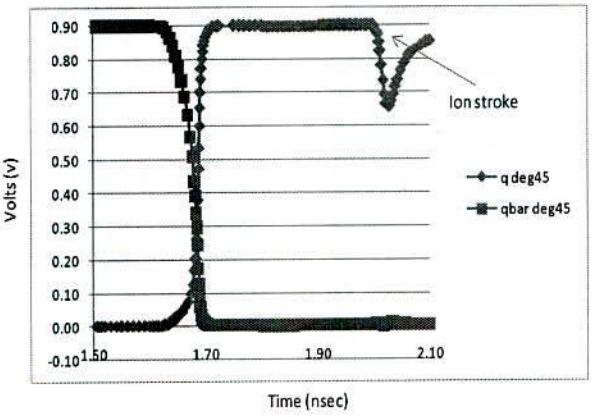


80° towards source

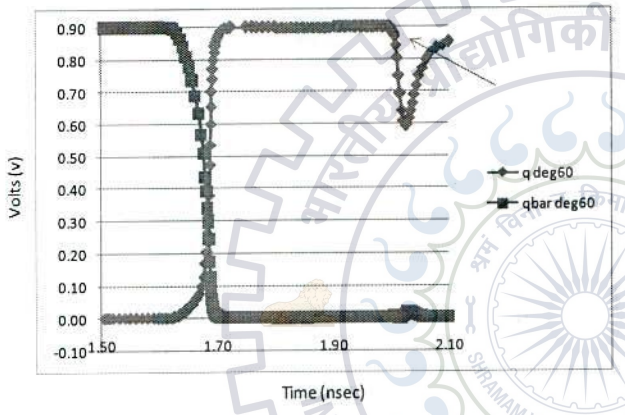
Fig 4.8: Boron ion strike with different angles of incidence.



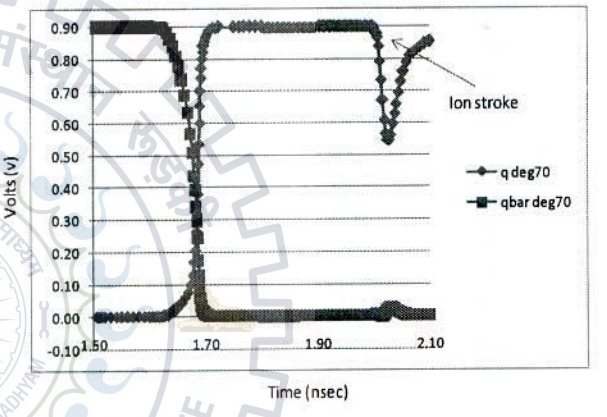
30° towards source



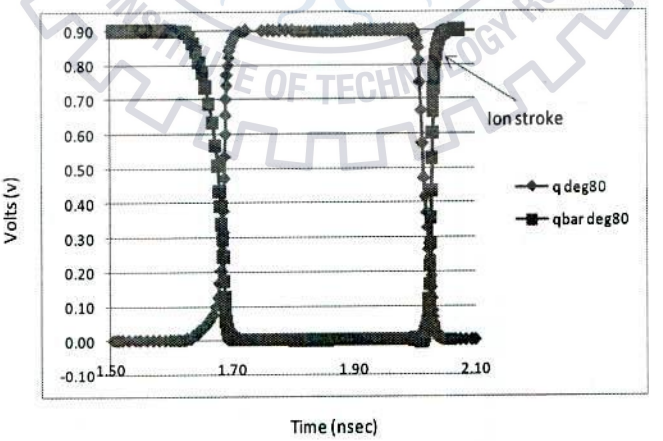
45° towards source



60° towards source



70° towards source



80° towards source

Fig 4.8: Boron ion strike with different angles of incidence.

Figure 4.8 shows the node voltage responses for different angles of incidence. We can see from the figure, the node Q pulls more down as the angle of incidence increases. This is due to the more amount of collected charge as explained above. At 80^{o} of angle, the node changes to wrong value since the collected charge crosses critical charge.

4.6 Results and Discussion:

The 3D 24nm-FinFET SRAM cell is designed and simulated the SEU behavior. The simulations carried out with different ion LET's and also the SEU response for angled incidences. The critical charge (Q_{crit}) of the designed 24nm FinEFT SRAM cell is found to be -0.84fC. And the LET threshold is 0.065 *(MeV-cm^2/mg).*

5. RADIATION EFFECTS ON BULK SRAM CELL

In this chapter we present the radiation effects on bulk SRAM cell. The SEU phenomenon of the bulk structures has been widely studied. In bulk Single Gate MOSFET's, funneling effect is the main damage causing phenomenon due to the presence of reverse biased P-N junction of Drain and Substrate junction. Here we discuss the making of 3D bilk SRAM cell followed by the radiation behavior of the cell.

5.1 3D Bulk SRAM Cell Creation:

90nm 3D contiguous block of 6T-SRAM cell is created by using Visual TCAD tool GDS2MESH which uses 90nm CMOS process with MosisCMOS design rules, as shown in figure 5.1. Si substrate of 1.2 μm thickness with P-type doping of $1 \times 10^{16}\ cm^{-3}$ is used. For NMOS device, Boron Gaussian implant with peak value of $1 \times 10^{20}\ cm^{-3}$ while for PMOS device Phosphorus Gaussian implant with peak value of $1 \times 10^{20}\ cm^{-3}$ is used for threshold voltage adjustments. Gate oxide thickness of 0.0032 μm, P-well doping of $2 \times 10^{18}\ cm^{-3}$, N-well doping of $2 \times 10^{18}\ cm^{-3}$ has been used. The created final structure with graded meshing is shown in figure 5.2. The cell has been sized with, the *cell ratio (CR)*, equal to $\frac{W_1}{W_5}$, of 2 for appropriate read operation and the *pull-up ratio (PR)*, equal to $\frac{W_4}{W_6}$, of 1 for appropriate write operation. So the widths of the transistors M1, M2, M3, M4, M5 and M6 are 0.22 µm, 0.11 µm, 0.22 µm, 0.11 µm, 0.11 µm and 0.11 µm respectively.

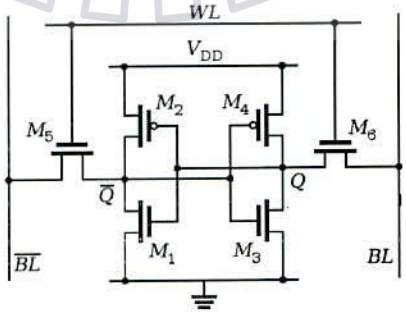


Fig 5.1: Schematic of SRAM cell.

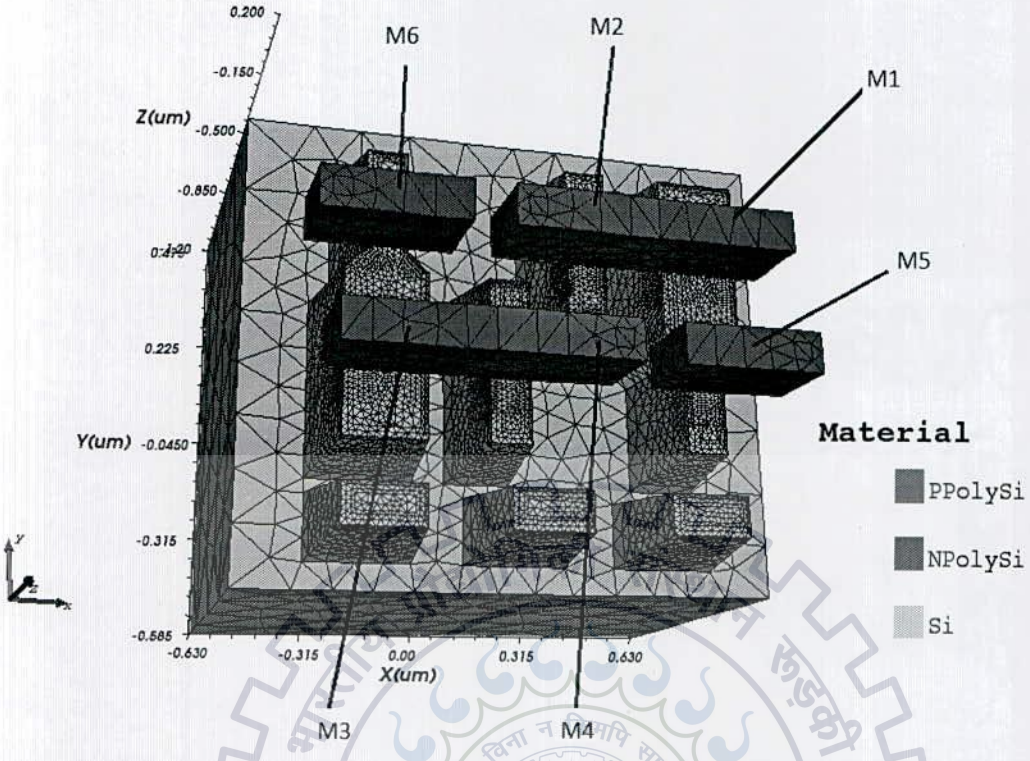


Fig 5.2: 3D view of 6T-SRAM cell.

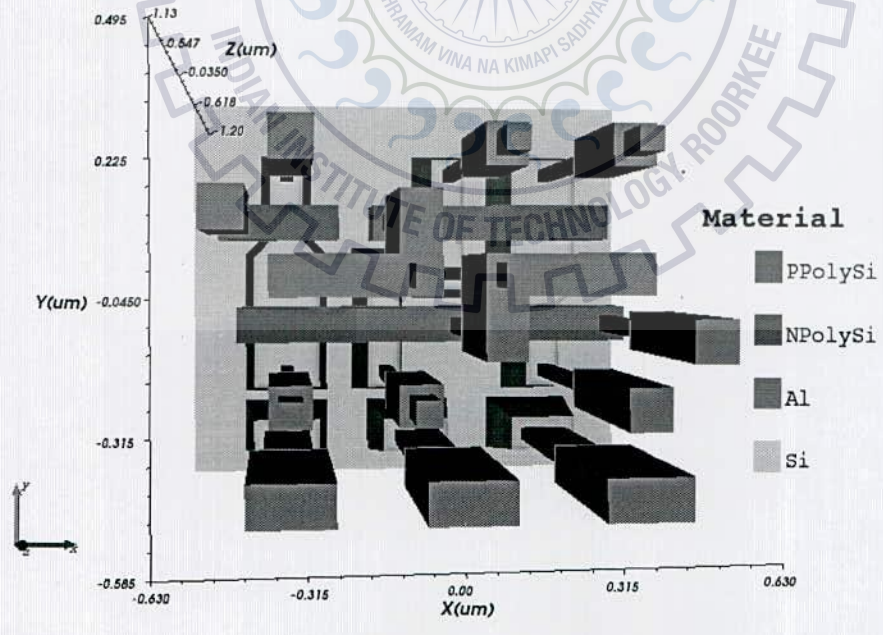


Fig 5.3: Top view of SRAM cell with aluminum contacts.

5.2 Device Simulation:

Device simulations have been carried out to simulate the time evolution of the voltages at different circuit nodes. Circuit and contact equations are solved, along with the Poisson, electron and hole continuity equations in self consistent manner. First the working of SRAM cell has been verified by writing data into the cell. Voltages of 'WL' and 'BLBAR' are pulses with rise and fall times 10 nsec each, with periods 30 nsec, 20 nsec respectively, ramped up at 165 nsec and 160 nsec respectively, to the final desired voltage of 1.2V as shown in figure 5.4. The node Q charged to 1.2V after the pass transistors ON, and holds till 190 nsec, where it discharged due to the changes in BL and BLBAR.

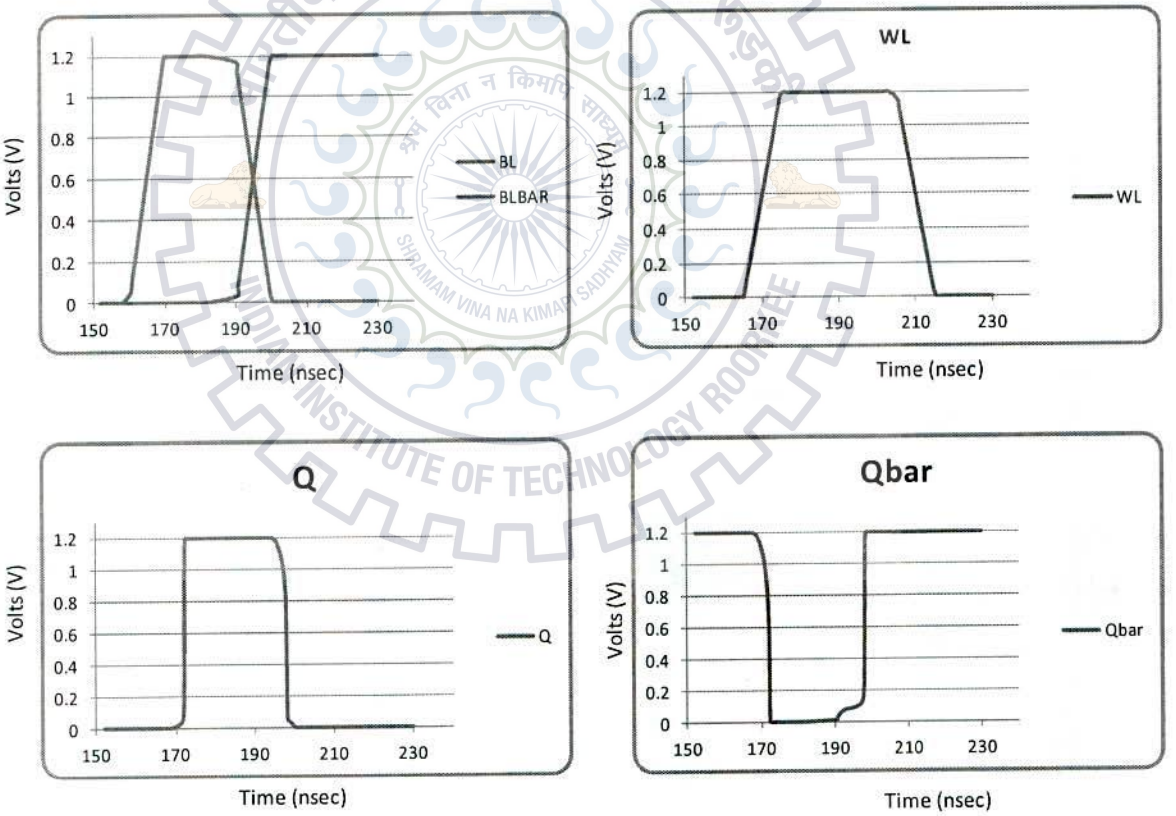


Fig 5.4: Node voltages for Normal Operation of SRAM cell.

So the Figure 5.4 verifies that constructed SRAM cell works as per the requirement. Now at 205 nsec the access transistors are switched off and the cell is in the data hold state with M3 and M2 are in off state.

5.3 SEU Effects on the SRAM cell:

The SRAM cell is now irradiated with the heavy ion gold $197_{AU_{93}}$ with different LET's, using the tool VisualPartilcle as shown in fig 3.2. The heavy ion strikes at location (X=0.35, Y=0.05 and Z=0.05) with direction of motion of ions from top to bottom along vertical Z-axis at time of 230 nsec as shown in figure. That means the ion strikes the cell at the Drain region of the off-state N-MOS (M3) device.

The Geant-based Single Event Analysis Tool (GSEAT) is a computer code, used to study the single event effect (SEE) of the designed SRAM cell. GSEAT is based on Geant4, a Monte Carlo code for the passage of particles through matter. For SEE simulation the detailed 3D structure of microelectronic device is required. GSEAT can load the SRAM structure generated by GDS2MESH tool in the Geometry Description Markup Language (GDML) format. GSEAT support simulation of SEE caused by various particles including alpha, heavy ion, proton and neutron in a wide range energies with realistic physical models.

Figure 5.5 shows the electron-hole pair generation along the length of heavy ion track. This electron-hole pair generation follows Gaussian distribution in the perpendicular direction of track i.e., the spatial distribution of the carrier density away from the track is Gaussian. And figure 5.6 shows the carrier density before radiation and after radiation with X-cut of the device.

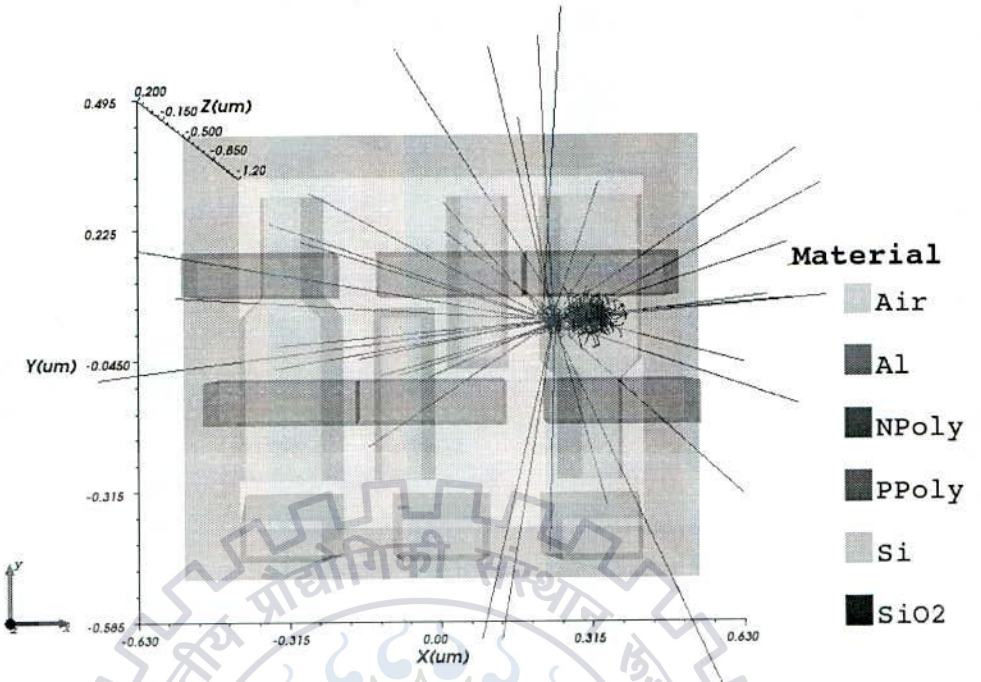
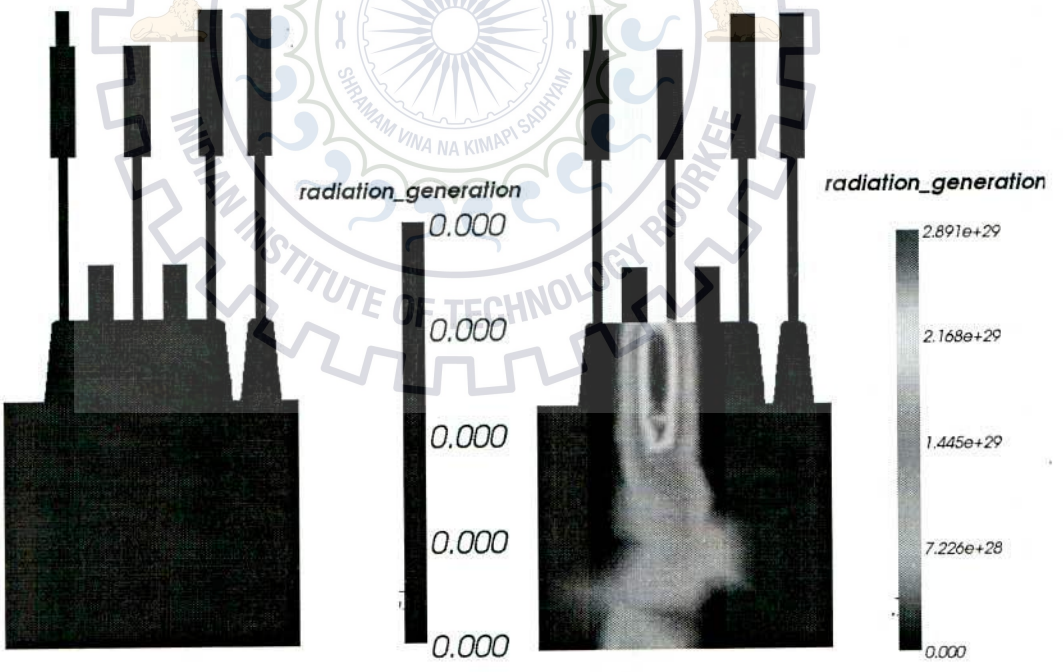


Fig 5.5: Heavy ion induced carrier generation.



(a) (b)

Fig 5.6: Radiation carrier density (a) before radiation (b) after radiation.

5.4 Node Voltage Response:

Analysis of the SRAM cell under both unirradiated (PRERAD) and irradiation (POSTRAD) condition due to heavy ion ($197_{AU_{93}}$) impact with respect to the relevant parameters by changing the LET values from 65.76, 76.63, 77.32 and 78.28 MeV- cm^2/mg is discussed as follows, by giving the shown voltage levels to BL, BLBAR and WL, in figure 5.7. From the figure the heavy ion strikes the cell at 230 nsec, at which the cell holds 1.2 volts and 0 volts at the nodes Q and QBAR respectively. The carrier generation is time dependent Gaussian distribution reaches maximum at 240 nsec with the variance of 3 nsec (set by simulation code). So the time evolution of carrier distribution lasts upto 15 nsec, and then the cell reforms back.

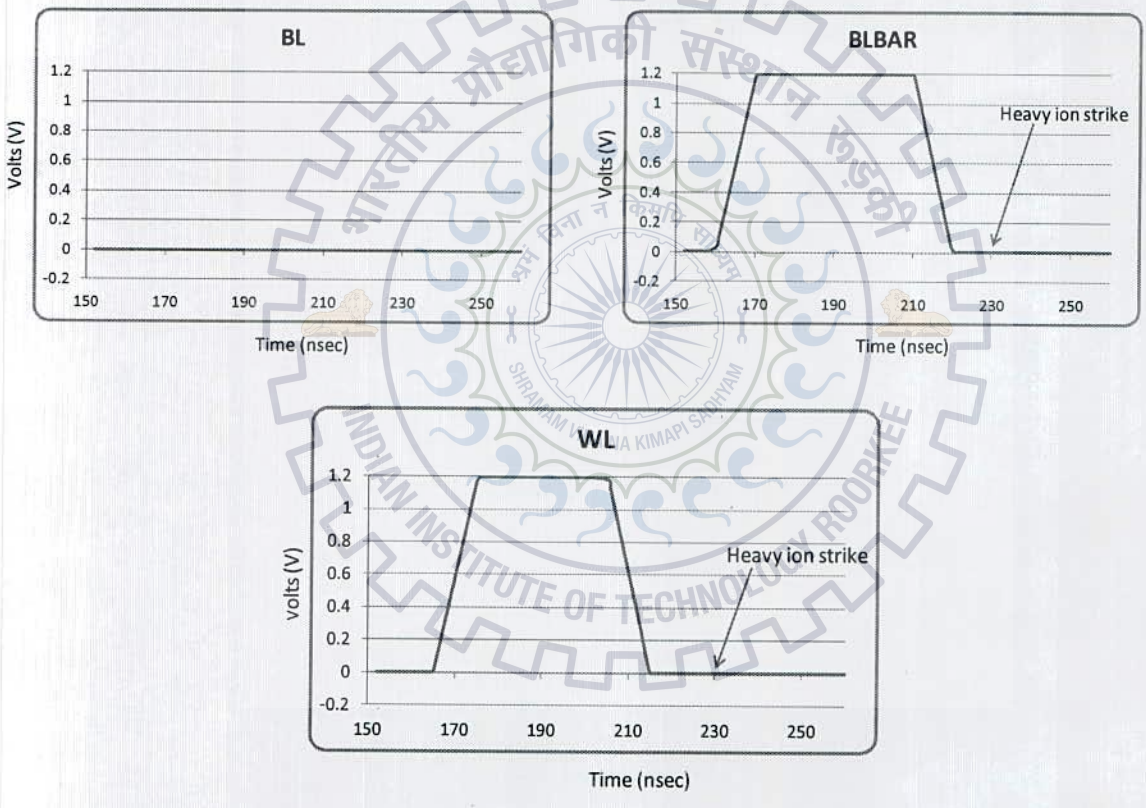


Fig 5.7: Input voltage levels for SRAM cell.

From the simulation results shown in figure 5.8, it is clear that the cell does not upset for LET's 65.76 and 76.63 MeV- cm^2/mg. This is because of insufficient charge collection, and for 77.32

5.6 Radiation Generation:

Figure 5.10 shows the heavy ion generation rate used in the simulation. It follows almost Gaussian distribution along the track. Various curves in the figure represent time dependent radiation profile. This electron-hole pair generation also follows Gaussian distribution with time, reaches maximum at 240 nsec and then falls back.

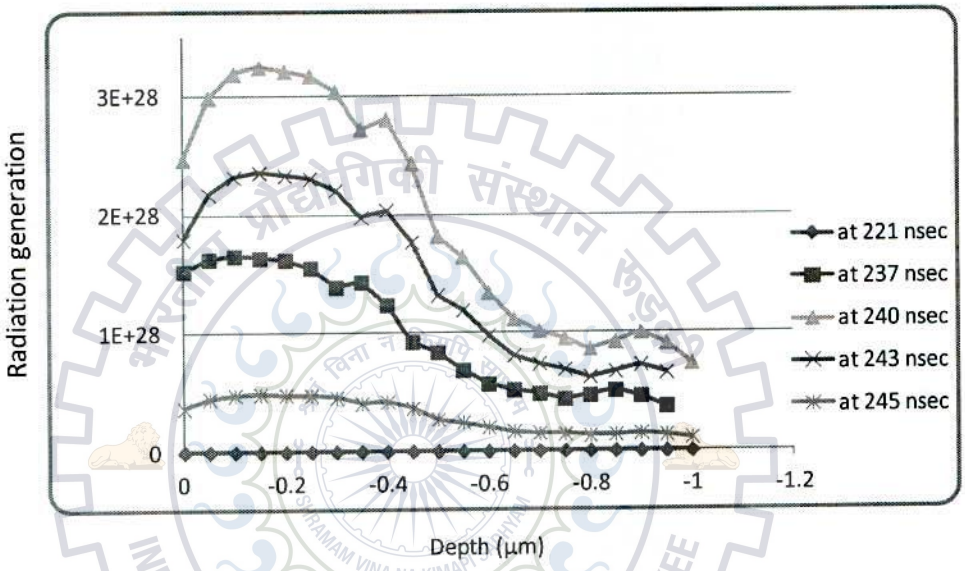


Fig 5.10: Electron-hole pair generation (cm^{-3}/sec) at different time frames.

6. CONCLUSION AND FUTURE WORK

We have performed the Single Event Upset study on multi gate devices. We have made 24nm-FinFET device and benchmarked. The FinFET SRAM cell is created and simulated the heavy ion radiation effects. The key parameter for the radiation sensitivity of the SRAM cell is critical charge. The value of critical is found to be -0.84fC for the designed SRAM cell. We also designed 90nm-bulk SRAM cell in the initial phase of research to observe the radiation sensitivity.

This work can be continued further to analyze the Total Ionizing Dose Effects (TID) of the created FinFET SRAM cell. But the software, I have used doesn't support the TID simulations. We need to move to the advanced tools.

Other way is to proceed in radiation hardened circuit design. Multi gate device are the current technology trends, so the radiation hardening of multi gate memory units would be a better future research scope.

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