CRITICAL EVALUATION OF FRINGE CAPACITANCE IN MULTI FIN FINFET AND ITS PROCESS PARAMETER EVALUATION

A DISSERTATION

Submitted in partial fulfilment of the requirements for the award of the degree

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in

ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Microelectronics & VLSI)

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CANDIDATE'S DECLARATION

I hereby declare that the work, which is being reported in this dissertation on, "**Critical evaluation of fringe capacitance in multi fin FinFET and its process parameter evaluation"**, being submitted in the partial fulfilment of the requirements for the award of the degree of **Master of Technology** in **Microelectronics & VLSI**, submitted in the Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee, India, is an authentic record of my own work carried out from May 2016 to May 2017 under the supervision of **Dr. Sudeb Dasgupta**, Associate Professor, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter embodied in the dissertation to the best of my knowledge has not been submitted for the award of any other degree elsewhere.

Dated:

Place: Roorkee

_____

(Ravi Shankar Pal)

CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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Acknowledgement

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Ravi Shankar Pal

M. Tech (Microelectronics and VLSI)

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABSTRACT

FinFET has emerged as a prominent device which can substitute the bulk MOSFET, as we tend towards the Sub-45nm technology. In FinFET there is a less short channel effects due to better controllability of gate over the channel. In this dissertation report, I have discussed why we need an alternative devices for MOSFET, advantages of scaling, disadvantages of scaling, different short channel effects arises from scaling of device such as Drain Induced Barrier Lowering, Velocity saturation, hot carrier effects, channel length modulation, punch through etc. Then I have discussed the principle of operation of MOSFET as the working of FinFET devices is same as working principle of MOSFET. Then I have described a brief history of multi-gate MOSFET. I have also described the FinFET structure of both double gate and triple gate FinFET, variation of doping in the FinFET, basic approach for the fabrication of FinFET, silicidation, and different architecture of gate and source/drain geometry. Finally, I have derived analytic modelling of fringing capacitances of faceted FinFET using conformal mapping technique and plotted the dependence of fringing capacitance on different parameters such as fin spacing and compare it with the non-faceted FinFET.

CHAPTER 1

INTRODUCTION

1.1 Overview

In this fast-moving world, the human requires a medium to communicate with each other and this requirement is completely fulfilled by the semiconductor industry. Today every aspect of human life is dependent on the outcome of semiconductor industry but there are certain guidelines that semiconductor industry must follow for example devices must be economical, faster and smaller in size. Since the advent of IC by J. Kilby in 1965 at BELL Laboratories, Semiconductor industry has seen a rapid growth in term of technology advancement.

In 1965, Gordon Moore published a paper to predict that no of transistors per chip increases by a factor of 2 after every two years, and this prediction is later known as Moore's law (figure 1.1) [1]. This law is being followed for the last five decades. But now, here comes a limitation imposed by Moore's law as described earlier channel length reduced by half every two years so as semiconductor industry moves towards 20nm technology reduction in channel length further becomes a limitation so semiconductor industry moves towards a new technology called SOI (silicon on insulator) in which silicon film lies over SIO2 layer. SOI technology increases both speed and power limitation significantly and one of the main advantages of SOI technology is reduced parasitic capacitance and enhanced current derive which is not familiar with planar CMOS technology. In planar CMOS technology as transistor channel length reduced the proximity of source and drain increases due to which the Gate lost the control over the potential distribution and flow of charge through the channel thus creating short channel effects (SCE) so taking in account all these disadvantages it looks impossible to further decreases the channel length of bulk MOSFET below 20nm ,so in order to increases the controllability of Gate over channel semiconductor industry turns towards multiple Gate MOSFET (MG).

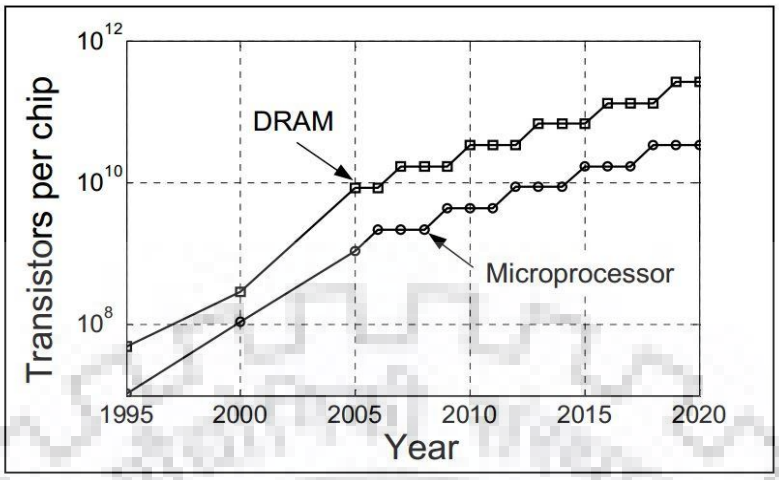


Figure 1.1: Comparison of the number of transistors estimated by the ITRS 2005 for DRAM and high-performance microprocessors (Moore's law) [1]

1.2 Thesis motivation

In FinFET we want to increase the on current and to increase the on current we increase the number of fins which in turns increases the capacitance of the device. So the motivation here is to reduce the fringing field by giving an alternative structure to FinFET and thus reducing the fringing capacitance of the device which in turn increase the speed of the device. So In order to reduce the capacitance of device we have taken a Finfet structure which has its fins cut at an angle due to which the area of coupling between two surfaces is reduced and thereby reduced the fringing field which in turn reduce the fringing capacitance.

1.3 Thesis organization

Rest of the thesis is as follows:

Chapter 2 deals with the advantages and disadvantages of scaling of devices, different short channel effects, MOSFET working principle and a brief history of multigate MOSFET, FinFET device structure, and fabrication.

Chapter 3 deals with the evaluation of fringing capacitance of multi-fin faceted FinFET and comparison of the fringing capacitance of faceted FinFET with the non-faceted FinFET using Matlab tools.

Chapter 4 deals with the conclusion drawn on the basis of this work.

CHAPTER 2

LITERATURE REVIEW

2.1 Advantage of scaling

The scaling of MOSFET has several advantages, as several smaller MOSFET can be integrated or packaged on to a single chip thus increasing the density of MOSFET'S making the chip concise and economic and the silicon area. The reduction in the size of chip allows the manufacturer to produce more chip at the low cost thus reducing the cost per chip.

Besides cost, a very important merit of scaling of MOSFET is increased in speed of operation and increased the frequency of digital circuits. This property is due to the two-basic reason. Firstly, the carriers have to traverse through the smaller channel length and second is smaller Gate capacitance. This reduced capacitance is attributed to the scaling of all the dimension of Gate and Gate capacitance is given by the equation

$$C_{gate} = \frac{\varepsilon_{ox} A_{gate}}{t_{ox}} \tag{2.1}$$

Where A_{gate} and t_{ox} are the Gate area and thickness of oxide layer under the Gate terminal. The scaling of Gate capacitance is done by keeping the Gate resistance constant. Thus, scaling the time constant according to the scaling of the physical dimension.

2.2 Disadvantage of scaling

The level of devices scaling that is prevalent in the industry today, it is downgraded due to the interconnect delay, so one of the primary purposes for which scaling is done is not fulfilled. Also, as the devices are scaled in atomic level, normal operation of MOSFET's is disturbed due to physical limits and some quantum phenomenon such as drain induced barrier lowering, quantum tunneling etc.

As the device is scaled, it starts enduring short channel effects (SCE) due to reduced channel length and some of these short channel effects is channel length modulation, Hot carrier effects, carrier velocity saturation etc. A short explanation of each of these effects is given below:

2.2.1 Drain Induced Barrier Lowering (DIBL)

In MOSFET's in weak inversion region due to applied Gate voltage there exists a small barrier voltage which carriers have to overcome to travel from source to drain terminal. If due to

application of a potential applied to the drain terminal the height of the barrier is lowered due to increase in the electric field lines from the drain terminal then this effect is known as Drain Induced Barrier Lowering (DIBL) [2] as shown in figure (2.1)

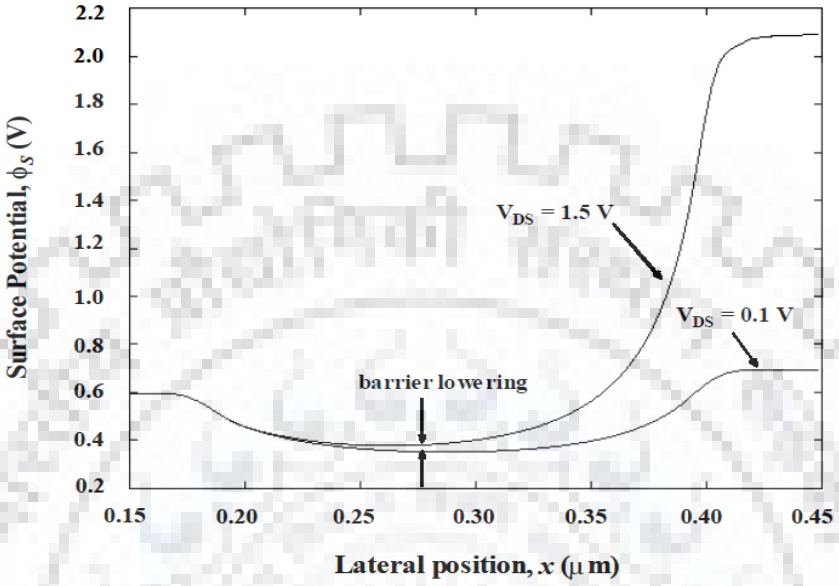


Figure 2.1: Changes in surface potential along the channel [2].

Besides this DIBL effect, another type of DIBL effects are also present in the device due to the scaling of the device e.g. (I) amassing of holes near the drain terminal creates the impact ionization which creates the positive biasing of the drain terminal. (II) For the holes at the source terminal, the height of the barrier is lowered as is shown in Figure (2.2)

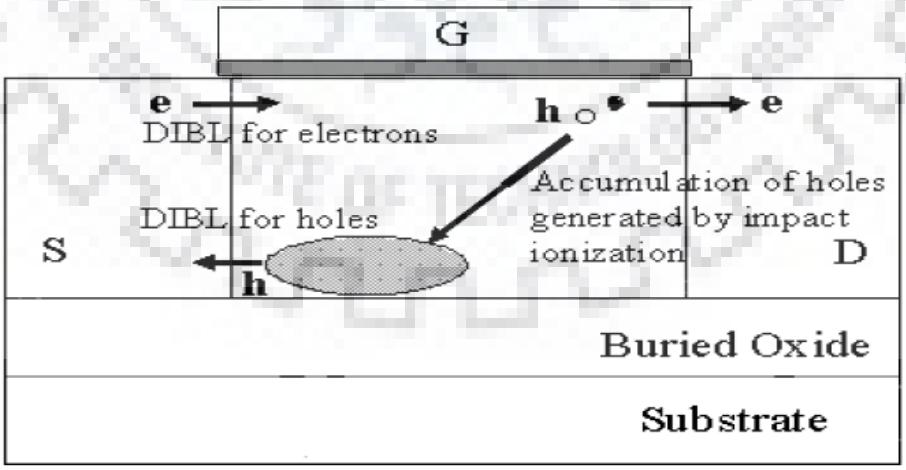


Figure 2.2.: DIBL effects in MOSFET's [2].

Due to ionization, the accumulated hole near the drain area makes the body positive biased which reduces the threshold voltage. The rate of generation of holes depends upon the reduction in channel length. Due to DIBL, the reduction in height of barrier decreases, due to which more number of holes are able to cross the barrier and contribute to lowering the threshold voltage and potential at the drain terminal is lowered. Figure (2.3) shows how the threshold voltage varies for short and long channel device.

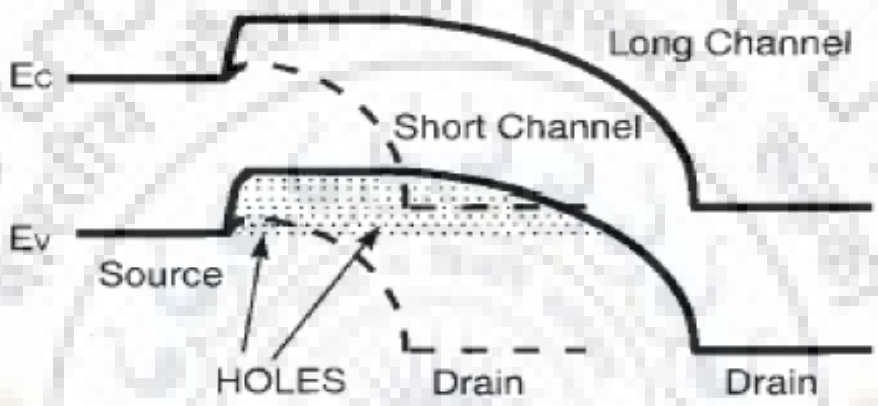


Figure 2.3: Comparison of the energy band in long and short channel MOSFET [2].

2.2.2 Velocity Saturation

In MOSFET for a smaller value of electric field drift velocity is directly proportional to the electric field but after a certain value of an electric field called critical field the velocity of carriers gets saturated so the relation $I= nEAV_d$ is not applied above the critical field. Above the critical field, velocity is given by

$$V_{sat} = (V_{gs} - V_{th}) \frac{v_{sat}}{\frac{\mu_{eff}}{2L}\left(V_{gs} - V_{th}\right) + v_{sat}} \tag{2.2}$$

Effective mobility depends upon channel length which in turn depends on the scaling of devices. Effective mobility is given by

$$\mu = \frac{\mu_{eff}}{\left(1 + \frac{\mu_{eff} V_{sat}}{v_{sat}(L - \Delta L)}\right)} \tag{2.3}$$

Saturation of carrier velocity [3-4] with increasing Gate velocity is shown in figure (2.4).

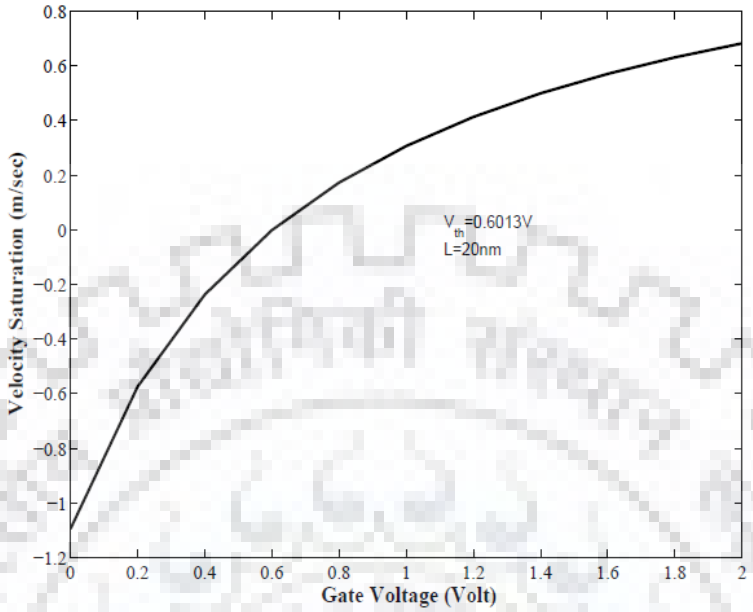


Figure 2.4: Variation of the carrier velocity with the voltage applied to the MOSFET Gate terminal [4].

2.2.3 Hot Carrier Effect or Carrier Heating Effect

For short channel device, the field is maximum at the junction and carriers acquire higher energy and moves in a random manner due to which some of the carriers can create impact ionization are known as hot-carriers. The energy associated with these hot carriers can be clearly studied with temperature. Actually, these energized carriers don't recombine but certainly, crosses the oxide layer and constitute the leakage current explained by E. Takeda et.al [5].

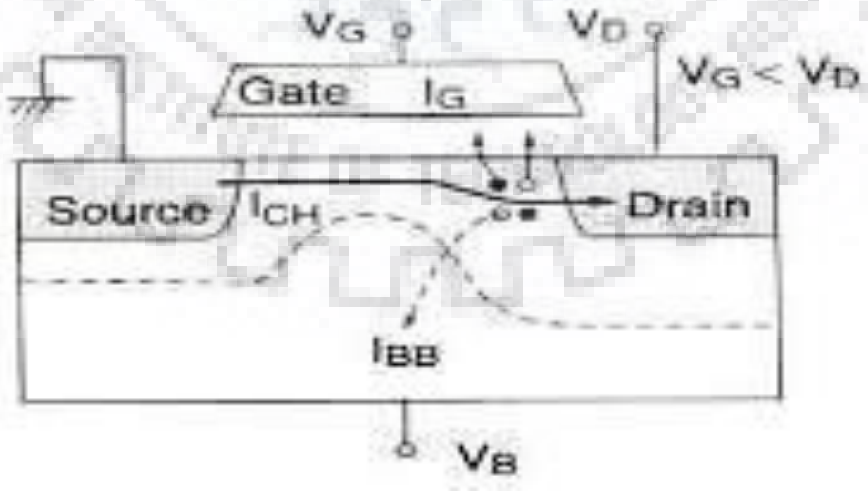


Figure 2.5: Creation the hot carrier due to the increase in electric field in the device [5].

2.2.4 Distance between source and drain gets reduced

The scaling of channel length arises several characteristics in MOS devices. Some of them are explained below.

2.2.4.1 Channel Length Modulation

In the short channel device where the physical thickness between source and drain is less, the depletion region of the drain side extends into the channel region with an increase in the drain supply voltage. This extension of the depletion region reduces the effective channel length. The effective channel length is the difference of metallurgical channel length and the width of the depletion region. The effect of this channel length modulation effect is shown in Figure 1.9, where the conductance of the output side is defined with the non-zero slope. This shortcoming of the device can be overcome by increasing the doping density of the drain according to the reduction in the channel length.

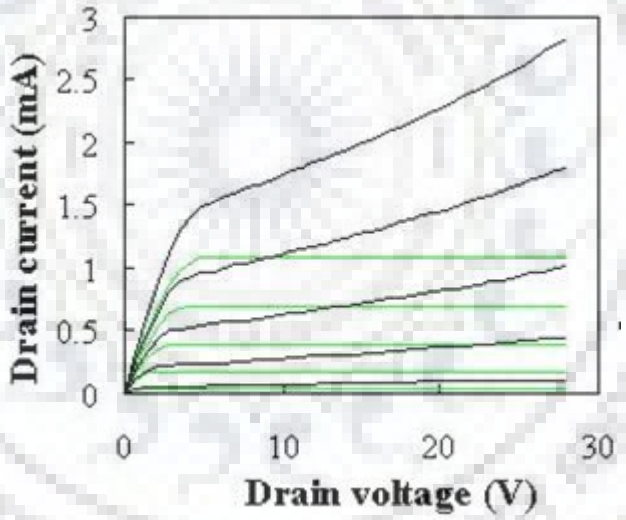


Figure 2.6: Variation of drain current with channel length modulation.

2.2.4.2 Punch Through Condition

As we go on increasing the drain voltage, the depletion region at the source and drain side gets increased and after a certain drain voltage, these two depletion regions touches each other. This results in effective Gate length reduced to zero and the region under the Gates acts as a function of drain voltage resulting in rapid increase in the drain current, and this extreme case of

channel length modulation is called punch through condition and is not desirable for the normal functioning of the device.

2.3 MOSFET working principle

MOSFET is a semiconductor device, consisting of four terminals namely source, drain, Gate, and the substrate. Out of these four terminals, the substrate is optional. In MOS transistor Gate is the controlling terminal having low-resistivity formed on the top of silicon dioxide and is made up of poly-crystalline silicon (polysilicon is heavily doped n or p region). In MOSFET source and drain terminal are of same type either n-type or p-type. While the type of doping of channel is opposite to the doping of source and drain region. Depending upon the magnitude of potential applied at the Gate different regions or conditions such as accumulation, inversion, and depletion region is formed. The simplified structure of n- channel MOSFET is shown in figure 2.7.

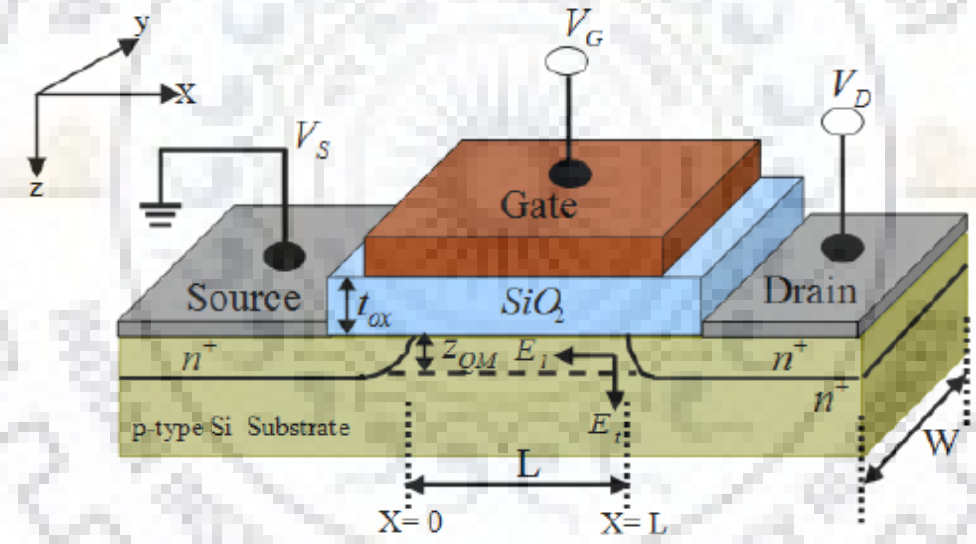


Figure 2.7: Typical MOSFET structure

Depending upon the type of doping in the channel, MOSFET can be MOSFET can be categorized in two types. (i). n-channel MOSFET (ii) p-channel MOSFET in n-channel MOSFET, the carrier responsible for the conduction of current through the channel are electrons while in P-MOSFET the carrier responsible for the conduction are holes. In n-MOSFET a positive voltage at the Gate will repel the holes in the channel leaving a region depleted of holes when Vgs is further increased this depletion region acts as negatively charged acceptor ions and attracts electrons from

source or drain region. Thus, a positive Gate voltage in n-MOSFET is decreasing the potential barrier for the electron and provide a low resistance path to the electrons. The minimum Gate voltage required to create the inversion layer is called threshold voltage whereas the region before the formation the formation of inversion layer is known as sub-threshold voltage as shown in figure 2.8.

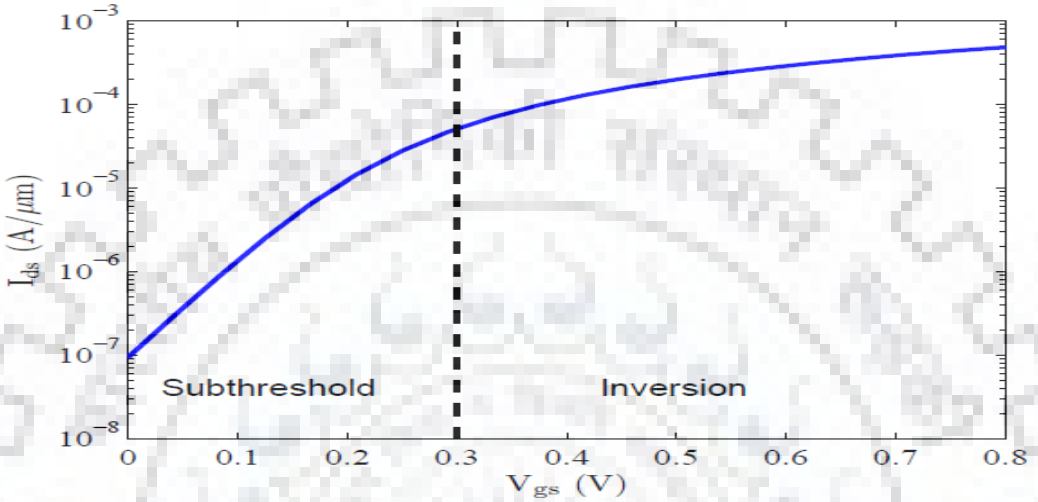


Figure 2.8: Variation of inversion voltage and the sub-threshold current for n-MOS

2.4 Gate Geometry and Short Channel Effects (SCE)

Short channel effects arise when due to source and drain electric field lines in channel get disturbed due to a reduction in channel dimension. These electric field lines are shown in figure 2.9. In bulk semiconductor devices, these field lines pass from source to drain through depletion region, but in short channel devices as doping in the channel increases percentage increase of doping increases which halts the proper device operation.

In fully depleted SOI, most field lines pass through the buried oxide layer (BOX) before reaching the channel as shown in figure 2.9.B. SCE in fully depleted SOI depends on SOI thickness, the thickness of buried oxide layer, doping in the channel. Since in FDSOI most of the field lines pass through the BOX layer gets terminated in that BOX layer itself instead of reaching channel region but this advantage comes at a cost of increases in junction capacitances and body effects.

A convenient method to solve this issue is the use of double Gate transistor. Double Gate transistor structure was firstly proposed by sekigawa and hayasi in 1984 [6]. In DG MOSFET both

Gates are connected together, the electric field lines below the channel get terminated on the bottom Gate and thus restricted to reach the channel and thus reduced the short channel effects as shown in figure 2.9.D [7].

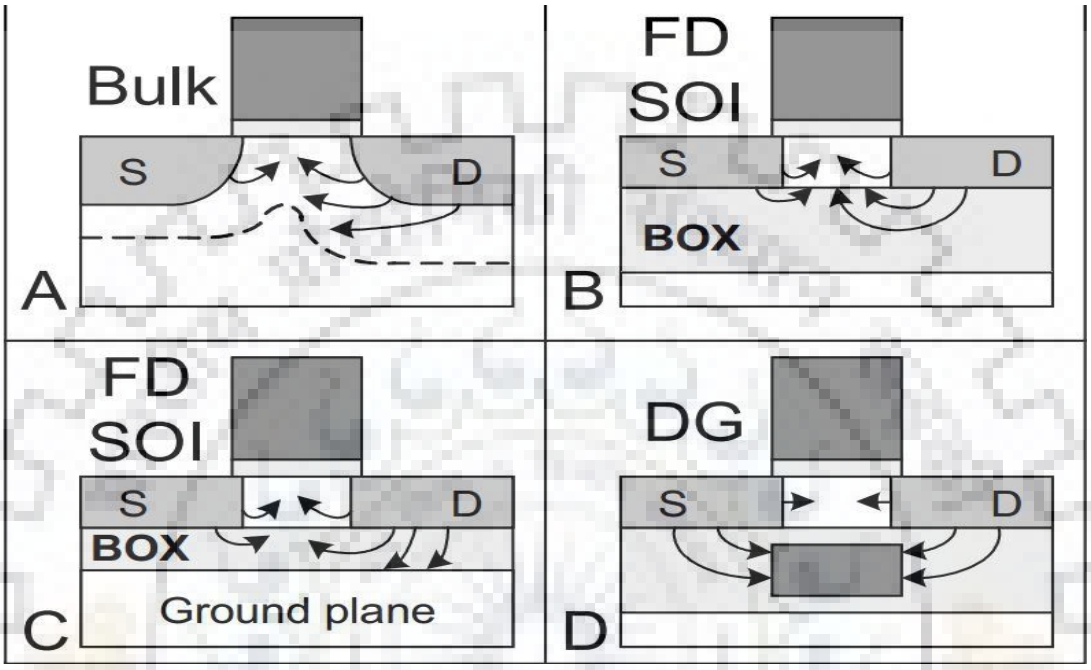


Figure 2.9: Field lines from source and drain on the channel in (A). BULK MOSFET (B). FDSOI (c).FDSOI WITH BOX,(D).DOUBLE GATE MOSFET [7].

2.5 Brief history of multiple GATE MOSFET

In order to get the better current drive and better control of Gate over channel SOI devices evolve from planar devices to three-dimensional devices with multiple structures (single Gate, double Gate, triple Gate).

2.5.1 SINGLE GATE SOI MOSFET

Figure 2.10 shows the evolution of multiple Gate devices from SOI to single Gate, single Gate to multiple Gate, and multiple Gate to fully depleted devices. PDSOI MOSFET was firstly used for high-temperature electronics but afterward used as a technique to improve sub-threshold slope, current drive and increases linearity. Fully depleted SOI has better characteristics in comparison to PDSOI and used as a low power to integrated RF circuits.

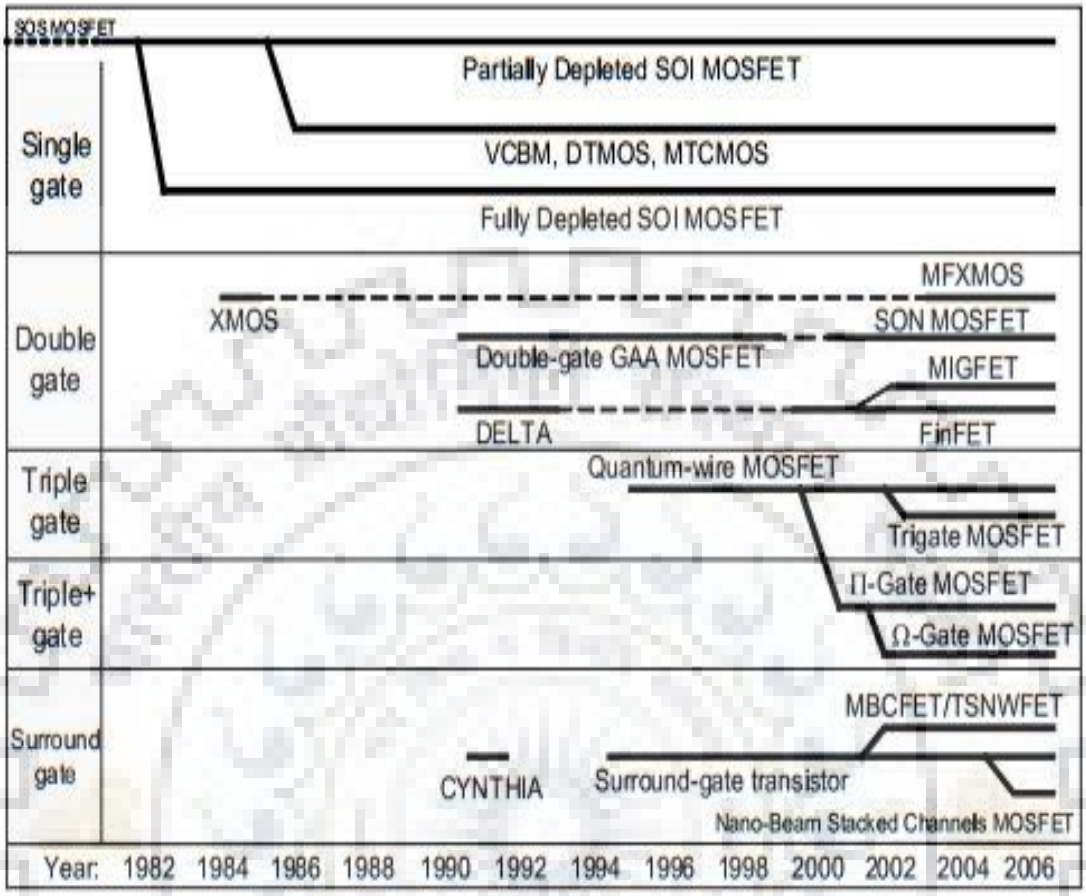


Figure 2.10. Evolution of Multi-Gate MOSFETs [7].

2.5.2 Double GATE SOI MOSFET

The first article published for DG MOSFET was proposed by T. sekigawa and Y. hayashi. They proposed that one can get reduced short channel effects by putting a FDSOI layer between two Gate electrodes. This device was XMOS. In this device, the influence of drain and source electric field over channel reduced due to which SCE decreased. The first fabricated DGSOI MOSFET was DELTA (FULLY DEPLETED LEAN CHANNEL TRANSISTOR) which has tall and thin fins or fingers like structure. The structure of FINFET is same as delta except for the hard mask on the top of the fin as shown in figure 2.11.

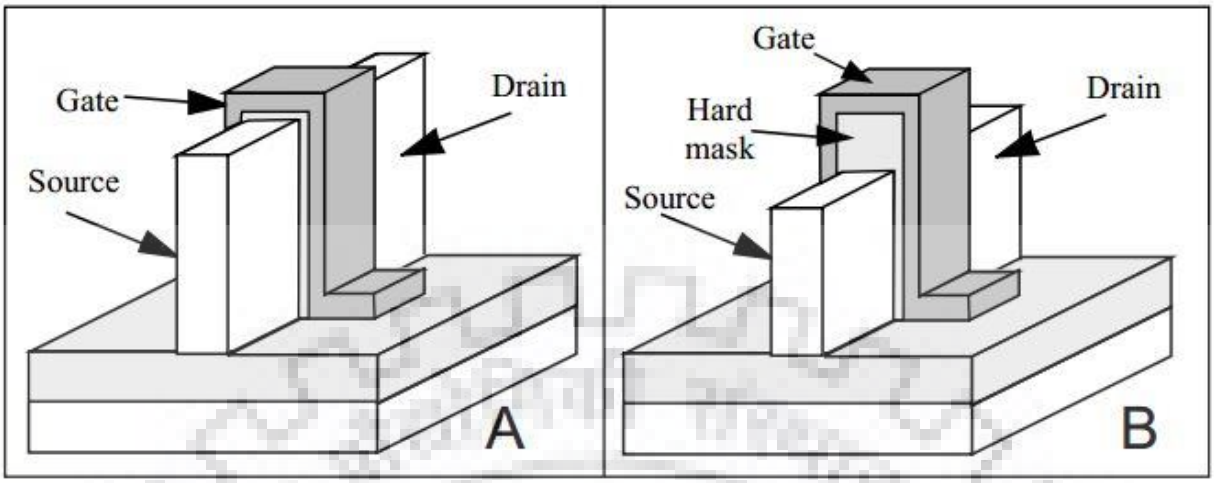


Figure 2.11: Double Gate MOSFET structure. (A)DELTA MOSFET (B) FINFET [7]

2.6 FinFET Structure

Among all the multi-Gate structure available to us, FinFET has shown us as an alternative option to replace the bulk-MOSFET as the fabrication is similar and compatible with the conventional CMOS technology trend. In a FinFET device, there is a vertical silicon structure that forms the channel and it is known as the fin (due to its similarity to the tail fin of the fish). Due to the presence of this vertical silicon structure (fin), the FinFET is called the semi-planner device. However, the direction of the flow of the carrier is parallel to the plane of the silicon wafer. The basic structure of FinFET is of two types:

(1) Double Gate structure (DG) (2) Triple Gate (TG).

In Triple Gate FinFET, the Gate is present on all the three sides of vertical fin structure i.e on top, side wall and thickness of oxide is uniform and same. In double Gate (DG) the thickness of oxide layer is very large on top of Gate in comparison to the thickness of oxide layer on the side wall or the presence of top Gate is avoided. In this work, I have considered only the Triple Gate FinFET.

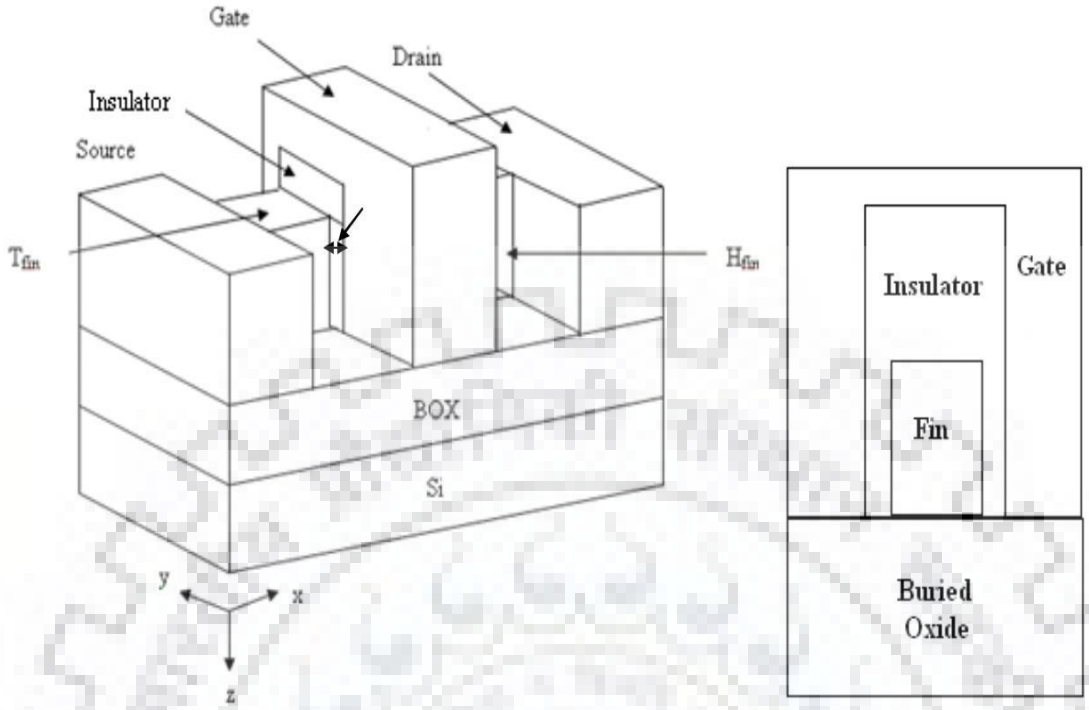
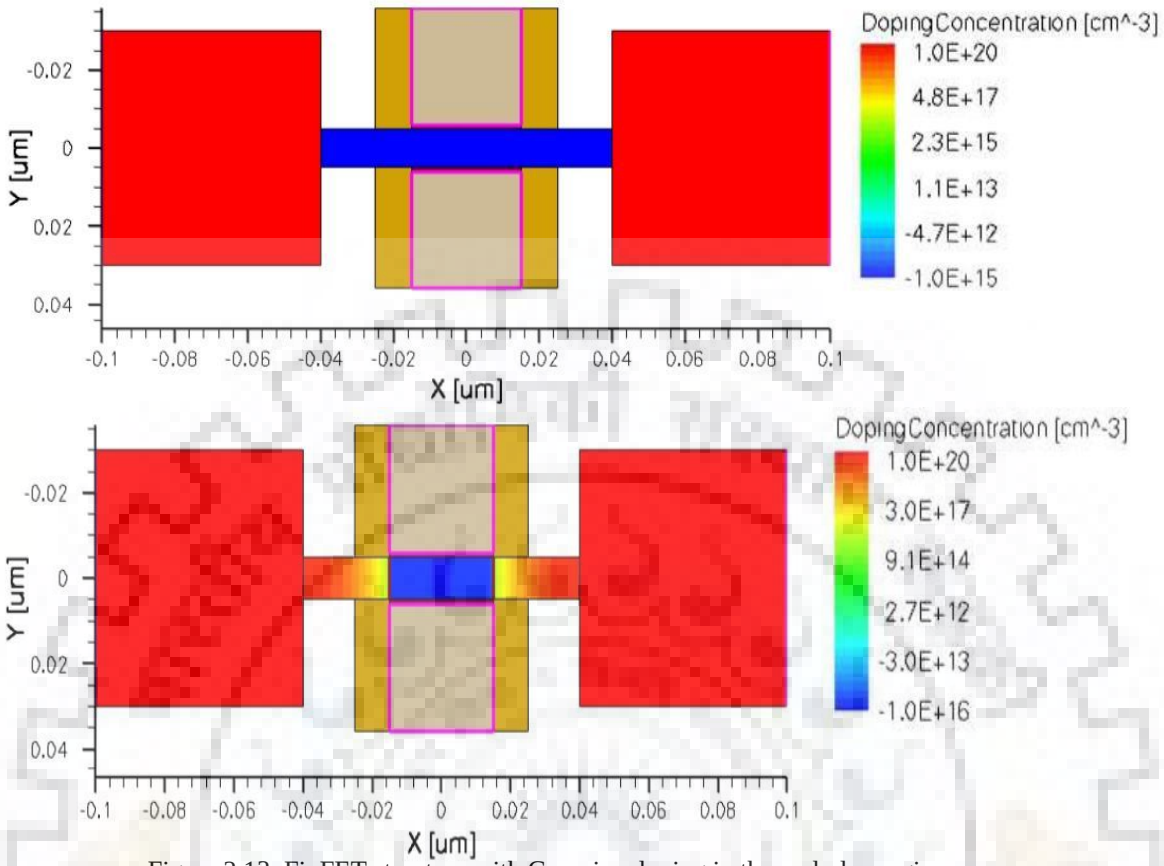


Figure 2.12: (a) 3D structure of a FinFET (b) Cross-sectional view of the Gate region [8]

Figure 2.12 shows the three-dimensional structure of double Gate FinFET and correctional view of Gate region. Fin thickness and fin height are represented by T_{fin} and H_{fin}. The thickness of oxide layer present between side Gate and vertical fin is T_{ox}. Balancing the height of fin, width, and thickness of oxide layer, channel length plays a crucial role in reducing the I_{off} and increasing the I_{on} thereby increasing Ion by Ioff ratio. For a Double Gate FinFET, the width of the fin is a function of the height of fin given by $W_{fin} = 2\ H_{fin}$.For a Triple Gate FinFET due to the additional control of Gate from the top side effective width of Fin is given by $W_{fin} = 2H_{fin} + T_{fin}$.

2.7 Doping Densities

As in conventional MOS devices the channel is lightly doped whereas source and drain region are lightly doped similarly in FinFET devices the fin which acts as the channel is lightly doped whereas the source and drain region are highly doped and the extension to the source and drain region may be undoped or uniformly doped or Gaussian doped.



. Figure 2.13: FinFET structure with Gaussian doping in the underlap region

2.8 FinFET Fabrication

There are two basic methodologies to fabricate FinFET structure:

(i) Gate Last approach: In this process, the source and drain region are fabricated before the formation of Gate. [8,9]

(ii) Gate first approach: Here the source and drain are fabricated after the fabrication of Gate stack. [10]

In the fabrication process of FinFET devices first, the patterning and etching of fin are done on SOI using a hard mask which needs to be retained throughout the whole Process of fabrication. For patterning of fin, the thickness of fin needs to smaller than Gate length for this we can use either optical lithography or electron beam lithography to pattern the fin.

For the Gate first approach, the steps involved in the fabrication of fin is similar to conventional bulk MOSFET. The Gate polysilicon is grown after the Gate oxide is deposited and the spacer is grown next to the source and drain and extension to the Source and drain are implanted using angle implant.

For Gate last approach, the drain and source are formed first then polysilicon is deposited on the fin, lithography is done on the source and drain pads. The effective Gate is the distance between source and drain. The Gate is further decreased by introducing a side wall spacer. Then Gate oxide is deposited and patterning is done. Overall the Gate last approach is subtle where metal Gate and high-K dielectric are used.

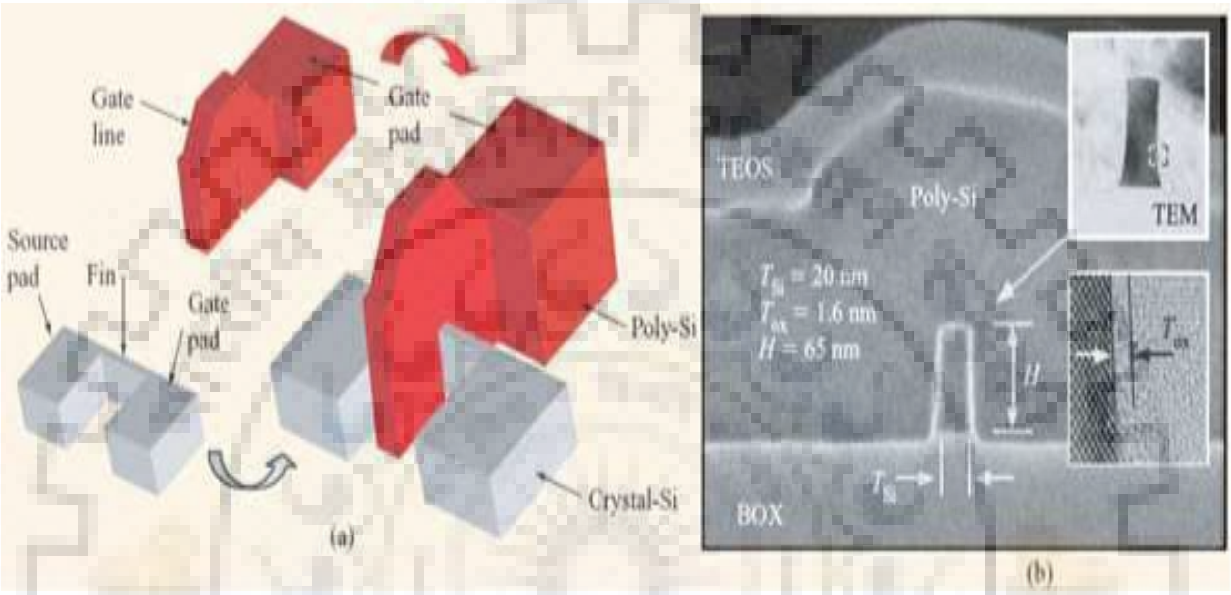


Figure 2.14: (a) Gate-First Process (b) Cross-sectional SEM and TEM images across the device width, demonstrating the fin cross-sectional sizes and the thin (1.6-nm) Gate oxide grown on the sidewall of the fin [11].

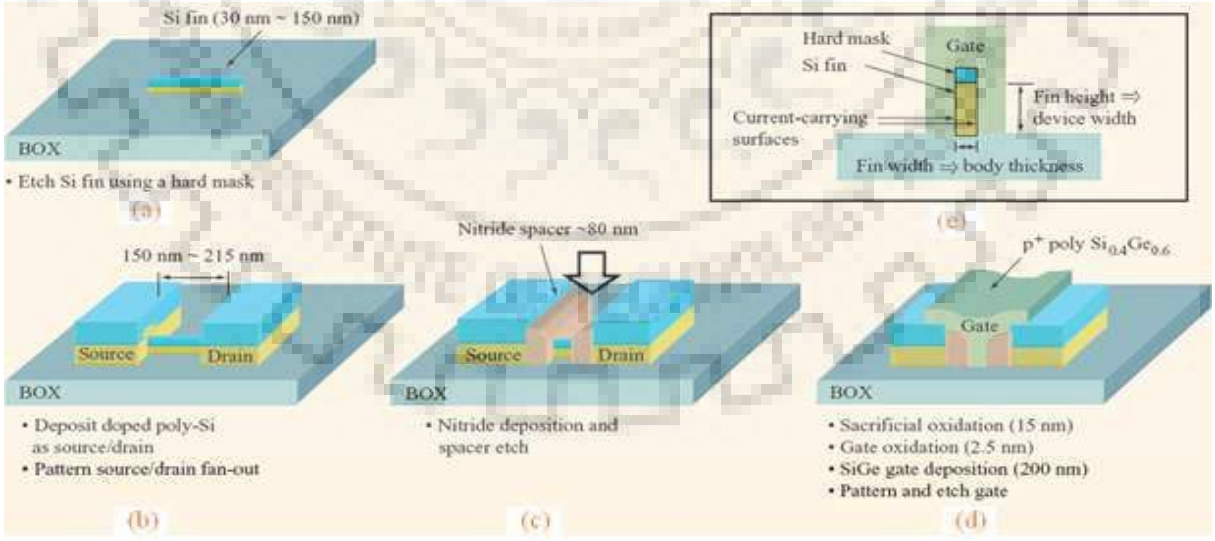


Figure 2.15: (a) – (d) Fabrication process of a Gate-Last Double Gate FinFET process. (e) Cross section of the silicon fin presenting the current-carrying plane. The current flow direction is in the plane of the diagram [11].

2.9 Silicidation

Silicidation is a process in which we use metal Silicon alloy to form a contact e.g Ti is deposited on Si to form Tis_2 alloy. Another example includes Ni-Si etc. The advantage of silicided Gate-devices over the non silicided Gate is tuning of work function can be easily done through adding appropriate impurity at silicide Gate oxide- interface.

Also, the C-V curves of silicide FinFET has a higher capacitance in the inversion region due to the absence of polysilicon Gate. Reduced Gate leakage- with silicided Gate leakage is similar as compared to the non-silicided Gate FinFET. Channel mobility- there is no effect of silicidation on channel mobility.

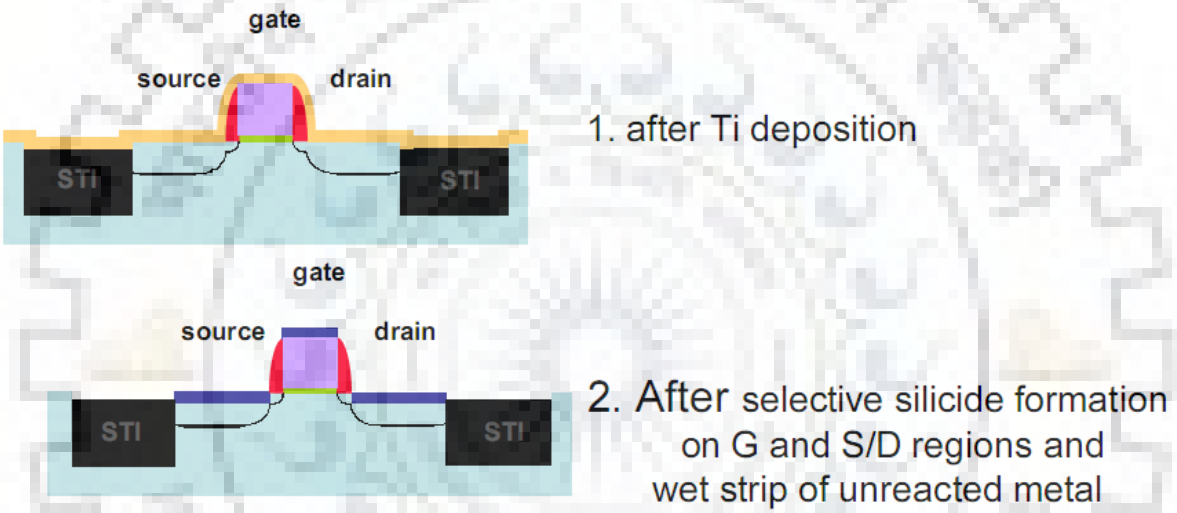


Figure 2.16: Typical Silicidation process [12].

2.10 Source and drain extension geometry:

There are two types of source and drain extension in respect of geometry:

(1) Rectangular

(2) Faceted

In faceted Source and Drain the fin is rectangular whereas the portion of source drain extension beyond the underlap is trigonal and one of the advantages is this geometry is reduced fringing capacitance when compared to with the rectangular source drain.

2.11 Gate architecture

There are two types of Gate architecture used in the FinFET devices:

(1) Raised Gate architecture

(2) Unraised Gate architecture

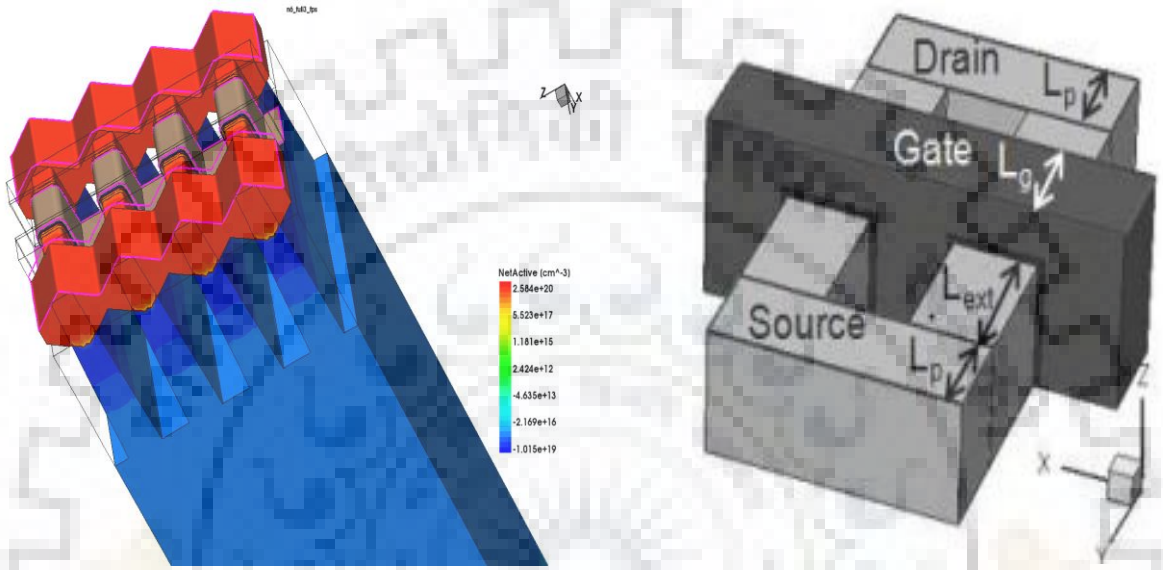


Figure 2.17: (a) Unraised Gate architecture, (b) Raised Gate architecture [17]

In Raised Gate the metal or Polysilicon Gate is present among all the fins with same height throughout whole structure whereas in unraised Gate architecture the Gate is also present between all fins but with reduced height in between the fins due to which there is reduced coupling between metal Gates and sides of source drain extension so in unraised Gate architecture there is reduced capacitance between the Gate and source and drain extension.

CHAPTER 3

EVALUATION OF FRINGING CAPITANCES

In order to make the devices more immune to Short Channel Effects (SCE), Drain Induced Barrier Lowering (DIBL), and decreased controllability of gate over the channel charge and increase the leakage current, the various non-planar structure has been proposed by the semiconductor engineers. In all those proposed structures FinFET is best suited to overcome the above-mentioned effects [13]. Below 90nm technology node, as we further go on decreasing the length of the channel, the total capacitance for the non-planar is increased due to the increase in the fringing field associated with the gate [14]. For a non-planar structure like FinFET, calculation of capacitances using traditional method cannot be applied [15]. Lacord et.al [16] has derived a model that can be applied to 2D and 3D structures. If we follow the guidelines provided by the ITRS then the fringing field will affect the total gate capacitance. So we need an improved device structure which has both the non-planar structure and the property of reduced fringing field. In this chapter, we use conformal mapping technique to find the parasitic fringing capacitance of faceted multi-fin FinFET.

3.1 Evaluation of Fringing Capacitances

Methodology to find the capacitance between the two surfaces [17]:

(1) Firstly, we will use conformal mapping and use boundary conditions we can transform the perpendicular plate system.

(2) Now, solving the Poisson's Integral equation with the above solved transformation we will be able to get the potential distribution in the transformed plane.

(3) Now substitute the potential distribution into the X and Y plane.

(4) Now we can find charge Q using the gauss law.

$$Q = \varepsilon \int -\frac{d\phi}{dx} dy \tag{3.1}$$

(5) Since charge is direct measure of capacitance we can find the capacitance as

$$C = \frac{Q}{V} \tag{3.2}$$

3.2. DEVICE GEOMETRY AND CAPACITANCES ASSOCIATED WITH THE GEOMETRY

Figure 3.1 shows the schematic diagrams of conventional FinFET [19] and faceted FinFET. Where L_g is the gate length, (2Lext+Lg) is the length of fin and L_p is the length of source and drain terminal. W_{fin} and H_{fin} are the width and height of the fin respectively. The thickness of the gate oxide layer is Tox, and number of fins is represented by N_{fin}. The distance between two neighboring fins is S_{fin}. The thickness of gate which is grown over the gate oxide is represented by $T_{poly.}$

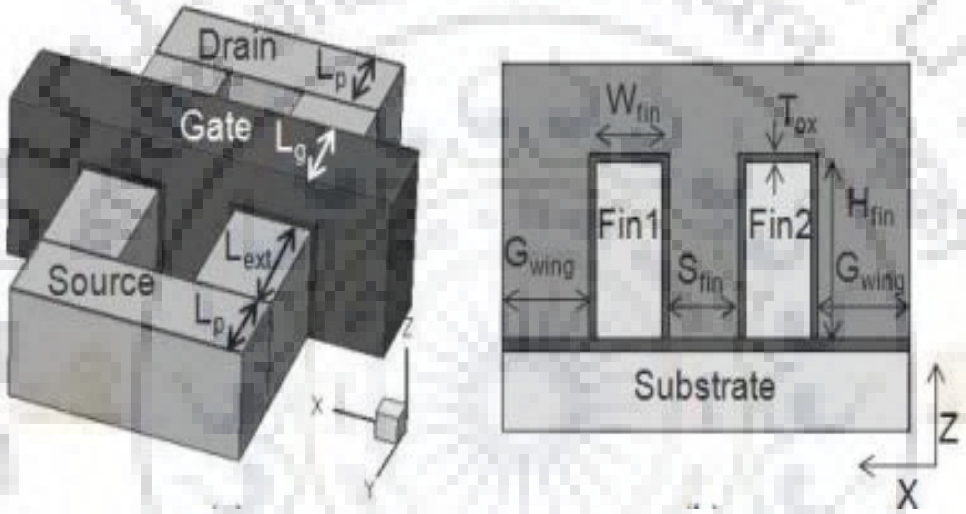
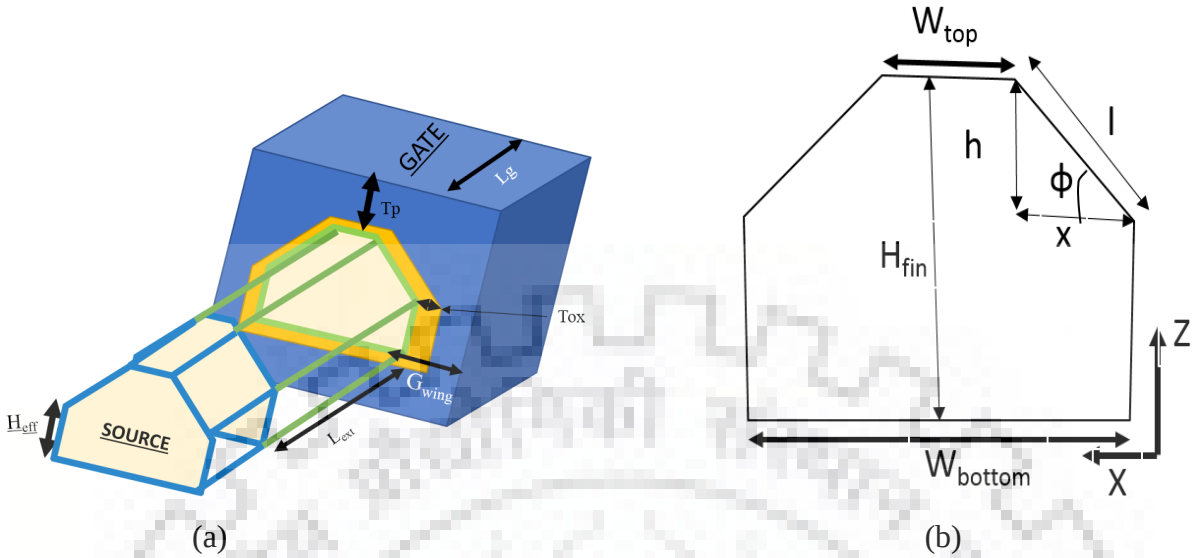


Figure 3.1: Three-dimensional view of FinFET and side view of FinFET [19]

There are two types of capacitance sin FinFET devices, overlap capacitance C_{ov} [18] and fringing capacitance C_{fr}. Overlap capacitance C_{ov} can be derived in the same way as derived as in conventional MOSFET. The fringe capacitance is due to two fringing field: (i) inner fringing field (2) outer fringe field. So, fringing field contributes namely inner capacitance and outer fringing capacitance. The strong inversion field screen the inner fringing capacitance due to this screening the inner fringing capacitance is nearly zero. Therefore we give significance to the outer fringe capacitance only and derive an analytic model for tri-gate faceted Multi-FIN FinFET structure.

In our structure, there are seven capacitance namely C_1, C_2,, C_3, C_4, C_5, C_6,C_7 .C_1 is due to the electric field emerging from the top of gate to the top of the fin and top of the gate to top of



(a) (b)

Figure 3.2: Three-dimensional view of faceted FinFET and side view of faceted FinFET

the inclined fin. C_2 is due to the electric field emerging from the side of the gate to the top of the fin and side of the gate to top of the inclined fin. C_3 is due to the electric field emerging from the side wall of the gate to the side wall of the fin and side wall of the gate to the inclined fin.C_4 is due to the electric field emerging from the end wall of the gate to side wall of the source and drain pad. C_5 is due to the electric field emerging from the side wall of the gate to the end of the source and drain pad. C_6 is due to the electric field emerging from the inner side wall of the gate to the side wall of the fin.C_7 is due to the electric field emerging from the side wall of the gate to the side wall of source-drain pad presents in between the two fins. Figure 3.2 Shows the 3-dimensional view of faceted FinFET with single fin however while calculating the capacitance we have calculated for two fin structures. Figure 3.3 shows the side view of faceted FinFET. Figure 3.3 shows the side view, top view and capacitance associated with the non -faceted FinFET [19] and we have calculated the corresponding capacitances for the faceted FinFET. Figure 3.4 show the top view of a single fin and Double fin FinFET.

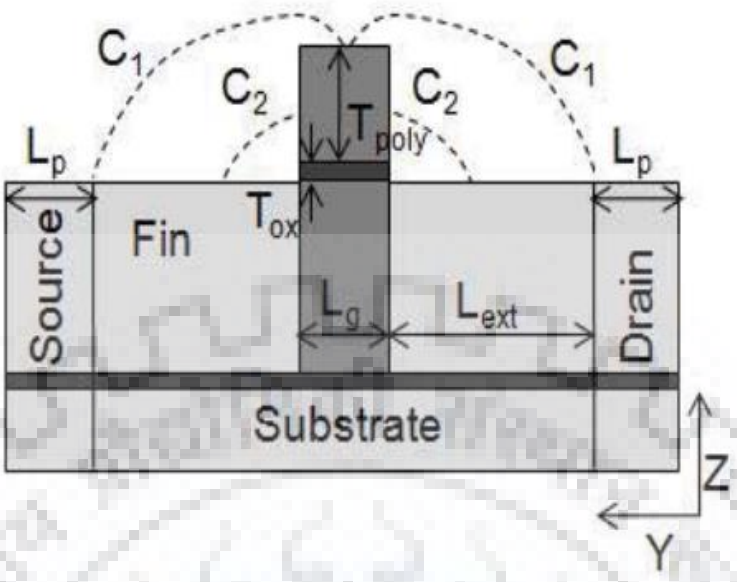


Figure 3.3: Fringing capacitance in Y and Z plane [19]

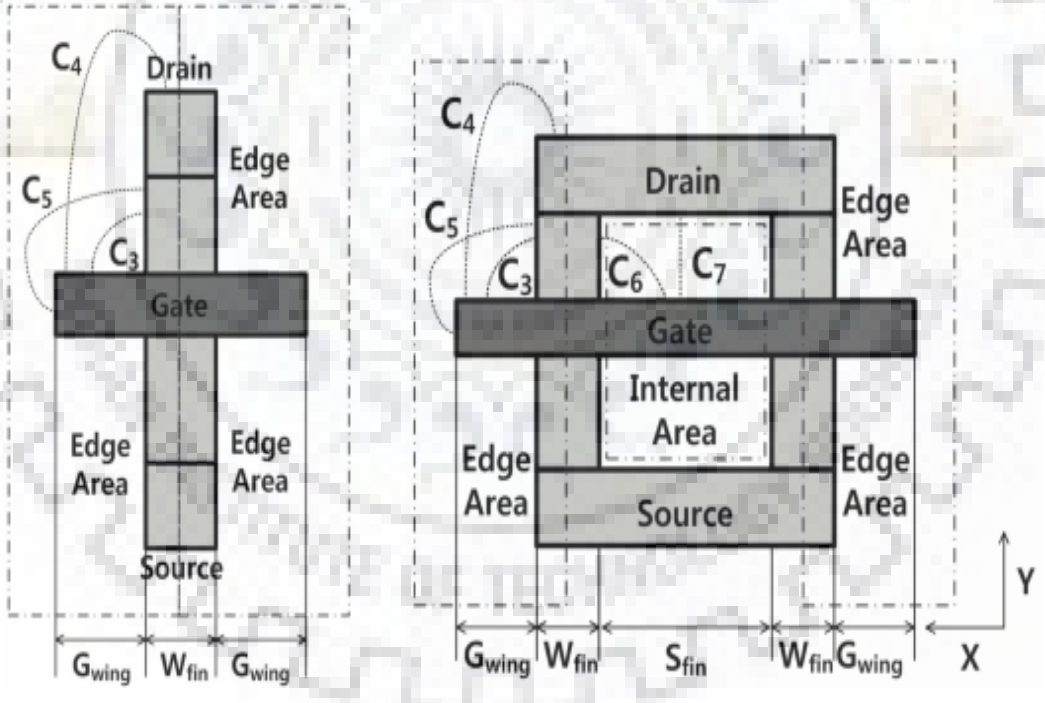


Figure 3.4: Fringing capacitance in X and Y plane for single fin and two fin structure [19].

For modeling of capacitances following device parameters are taken from the device geometry and is shown in Table 1. And some of the parameter used in deriving the capacitances are given below:

$$W_{Top} = W_{fin} - 2x$$

$$H_{eff} = H_{fin} - h$$

$$\tan \Phi = \left(\frac{h}{x}\right)$$

Table 3.1: list of parameter associated with geometry of device

Parameters	Values
L_g	22nm
H_{Fin}	30nm
W_{bottom}	20nm
T_{ox}	1.5nm
T_{poly}	10nm
L_{ext}	30nm
L_p	20nm
h	5nm
x	5nm

3.3 ANALYTICAL MODELING OF FACETED FINFET

Capacitance C_1 and C_2 for the non-faceted FinFET is derived in [19], similarly, for the faceted FinFET C_1 and C_2 is given by

$$C_1 = \frac{2\varepsilon(W_{Top} + S_{fin})}{\pi} ln\left[1 + \frac{L_g}{T_{ox} + T_{poly}}\right] + \frac{4\varepsilon l cos\phi}{\pi} ln\left[1 + \frac{L_g}{T_{ox}+T_{poly}}\right] \quad (3.3)$$

$$C_2 = \frac{2\varepsilon W_{Top}}{\pi} ln\left[1 + \frac{T_{poly}+\sqrt{{T_{poly}}^2+2T_{ox}*T_{poly}}}{T_{ox}}\right] + \frac{\varepsilon W_{Top} e^{-1}}{\pi} ln\left(\frac{\pi W_{Top}}{T_{ox}}\right) + \frac{2\varepsilon(lsin\phi)}{\pi} ln\left[1 + \frac{T_{poly}+\sqrt{{T_{poly}}^2+2T_{ox}*T_{poly}}}{T_{ox}}\right] + \frac{2\varepsilon(lsin\phi)e^{-1}}{\pi} ln\left(\frac{\pi(lsin\phi)}{T_{ox}}\right) \quad (3.4)$$

Where η_2 is given by

$$\eta_2 = exp\left[\frac{L_{ext}+L_p-\sqrt{{T_{poly}}^2+2T_{poly}.T_{ox}}}{L_{ext}+L_P}\right] \quad (3.5)$$

Using conformal mapping [20], the C_3 and C_6 is given as

$$C_{3,6} = \frac{2\varepsilon H_{eff}}{\pi} ln\left[1+\frac{\eta_{3,6}W_{3,6}+\sqrt{{\eta_{3,6}}^2{W_{3,6}}^2+2\eta_{3,6}ToxW_{3,6}}}{T_{ox}}\right] + \frac{\varepsilon H_{eff}e^{-1}}{\pi} ln\left(\frac{2\pi H_{eff}}{T_{ox}}\right) + \left(\frac{\varepsilon lcos\phi}{\pi} ln\left[1+\frac{\eta_{3,6}W_{3,6}+\sqrt{{\eta_{3,6}}^2{W_{3,6}}^2+2\eta_{3,6}ToxW_{3,6}}}{T_{ox}}\right] + \frac{\varepsilon lcos\phi e^{-1}}{\pi} ln\left(\frac{2\pi lcos\phi}{T_{ox}}\right)\right) \quad (3.6)$$

Where $\eta_{3,6}$ is given by

$$\eta_{3,6} = \exp\left[\left\{1-\sqrt{\left(\frac{W_{3,6}+T_{ox}}{L_{3,6}}\right)^2-\left(\frac{T_{ox}}{L_{3,6}}\right)^2}\right\}^2\right] \quad (3.7)$$

Where

$W_3=G_{wing}=\frac{S_{fin}}{2}$

$L_3=L_{ext}+L_p$

For C_6

$W_6=\frac{S_{fin}}{2}$

$L_6=L_{ext}$

C_4 compromises of Cpi, Cpar, and Ccorner. Cpar is connected in series with the parallel combinations of Cpi and C_{corner} and C_4 is given by

$$C_4=\frac{C_{4par}\left(C_{4cor}+C_{4pi}\right)}{C_{4cor}+C_{4pi}+C_{par}} \quad (3.8)$$

Where all these capacitances mentioned above are given by

$$C_{4par} = \frac{\varepsilon H_{eff}W_4}{L_4}+\frac{\varepsilon hW_4}{L_4} \quad (3.9)$$

$$C_{4pi} = \frac{\varepsilon H_{eff}}{\pi} ln\left[1+\frac{2W_4}{T_{ox}}\right]+\frac{\varepsilon h}{\pi} ln\left[1+\frac{2G_{Wing}}{T_{ox}}\right] \quad (3.10)$$

$$C_{4cor}=\frac{\varepsilon H_{eff}}{\pi} exp\left[-\left(\frac{T_{ox}+L_4}{3d_4}\right)\right]+\frac{\varepsilon h}{\pi} exp\left[-\left(\frac{T_{ox}+L_4}{3d_4}\right)\right] \quad (3.11)$$

Where

$W_4=G_{wing}$

$L_4=L_{ext}+L_p$

$d_4=T_{ox}$

C_5 compromises of Cpi, Cpar, and Ccorner. Cpar is connected in series with the parallel combinations of Cpi and C_{corner} and C_5 is given by

$$C_5=\frac{C_{5_{par}}\left(C_{5_{cor}}+C_{5_{pi}}\right)}{C_{5_{cor}}+C_{5_{pi}}+C_{5_{par}}} \quad (3.12)$$

Where all these capacitances mentioned above are given by

$$C_{5_{par}}=\frac{\varepsilon H_{eff}W_5}{L_5}+\frac{\varepsilon l cos\phi W_5}{L_5} \quad (3.13)$$

$$C_{5_{pi}}=\frac{\varepsilon H_{eff}}{\pi} ln\left[1+\frac{2W_5}{T_{ox}}\right]+\frac{\varepsilon l cos\phi}{\pi} ln\left[1+\frac{2G_{Wing}}{T_{ox}}\right] \quad (3.14)$$

$C_{5_{cor}}=0$

Where

$L_5=G_{wing}+T_{ox}$

$W_5=L_{ext}+L_p$

Capacitance C_7 given by

$$C7=\left[\frac{\varepsilon\, hS_{fin}}{L_{ext}}\right] \quad (3.15)$$

Taking into account all the capacitance described above the total capacitance in different planes is given by

$$C_{fr,x\text{-}y}=4(C_3+C_4+C_5+C_6(N_{fin}-1))+2\,C_7(N_{fin}-1) \quad (3.16)$$

$$C_{fr,y\text{-}z}=2N_{fin}(C_1+C_2) \quad (3.17)$$

Total capacitance is given by

$$C_{fr,total}=C_{fr,x\text{-}y}+C_{fr,y\text{-}z} \quad (3.18)$$

3.4 Results and Discussion

In this section, I have plotted different capacitance associated with the geometry of faceted FinFET and compared it with the corresponding capacitances of the non-faceted FinFET using MATLAB tool and results are analyzed.

(i) Variation of C_1 with spacing between the fins.

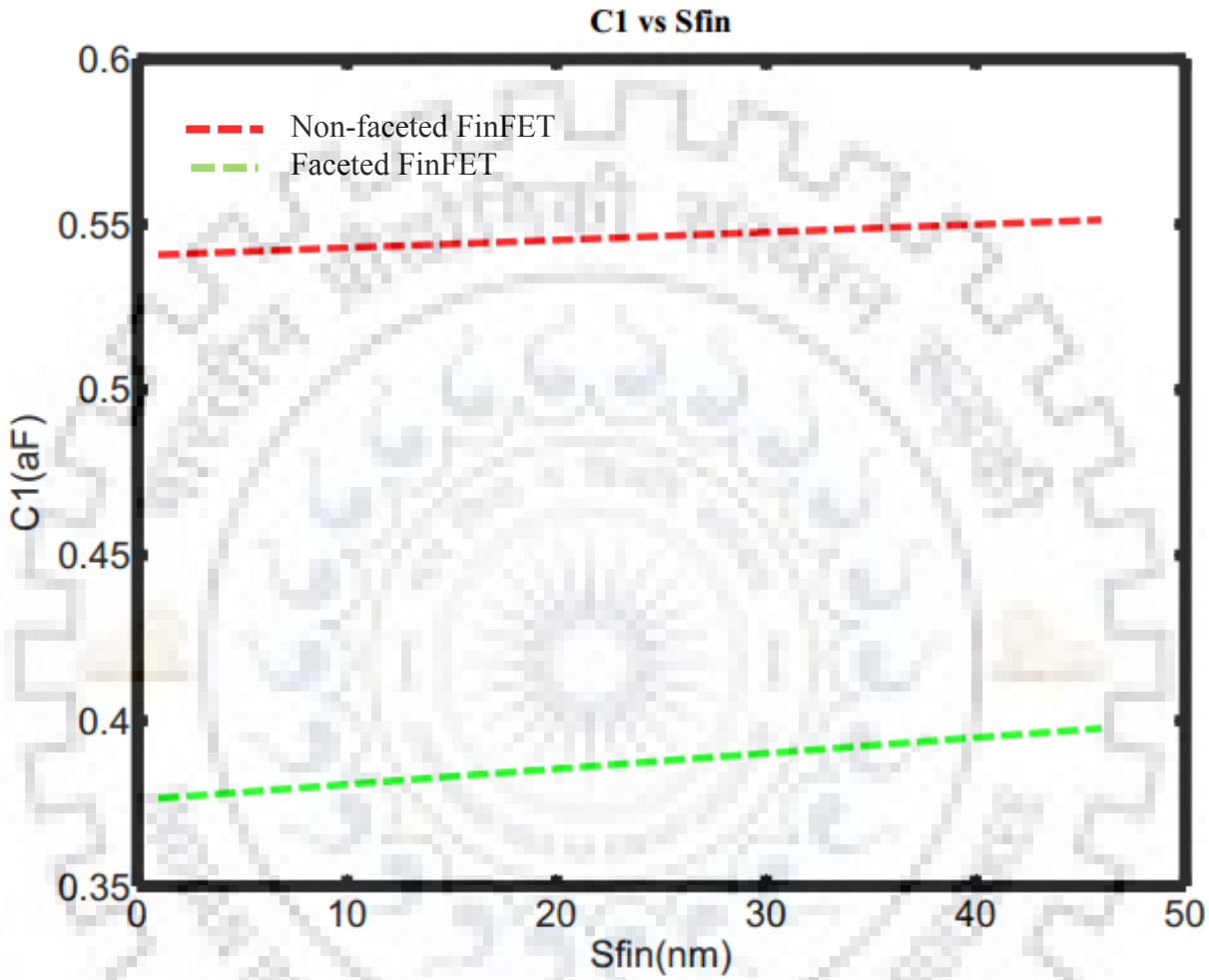


Figure 3.5: Variation of C_1 with spacing between the fins.

Figure 3.5 shows the variation of C_1 with the spacing between the fins. C_1 is the capacitance between the top of the gate and top of the fin along with the top of the inclined surface of the fin. In figure 3.5 red line depicts the non-faceted FinFET and green line depicts the faceted FinFET. As shown in figure 3.5 the C_1 varies linearly with the spacing between the fins. So by faceting the shape of fin C_1 is reduced in comparison to the non-faceted FinFET due to a reduction in effective width of the fin.

(ii) Variation of C_2 with spacing between the fins.

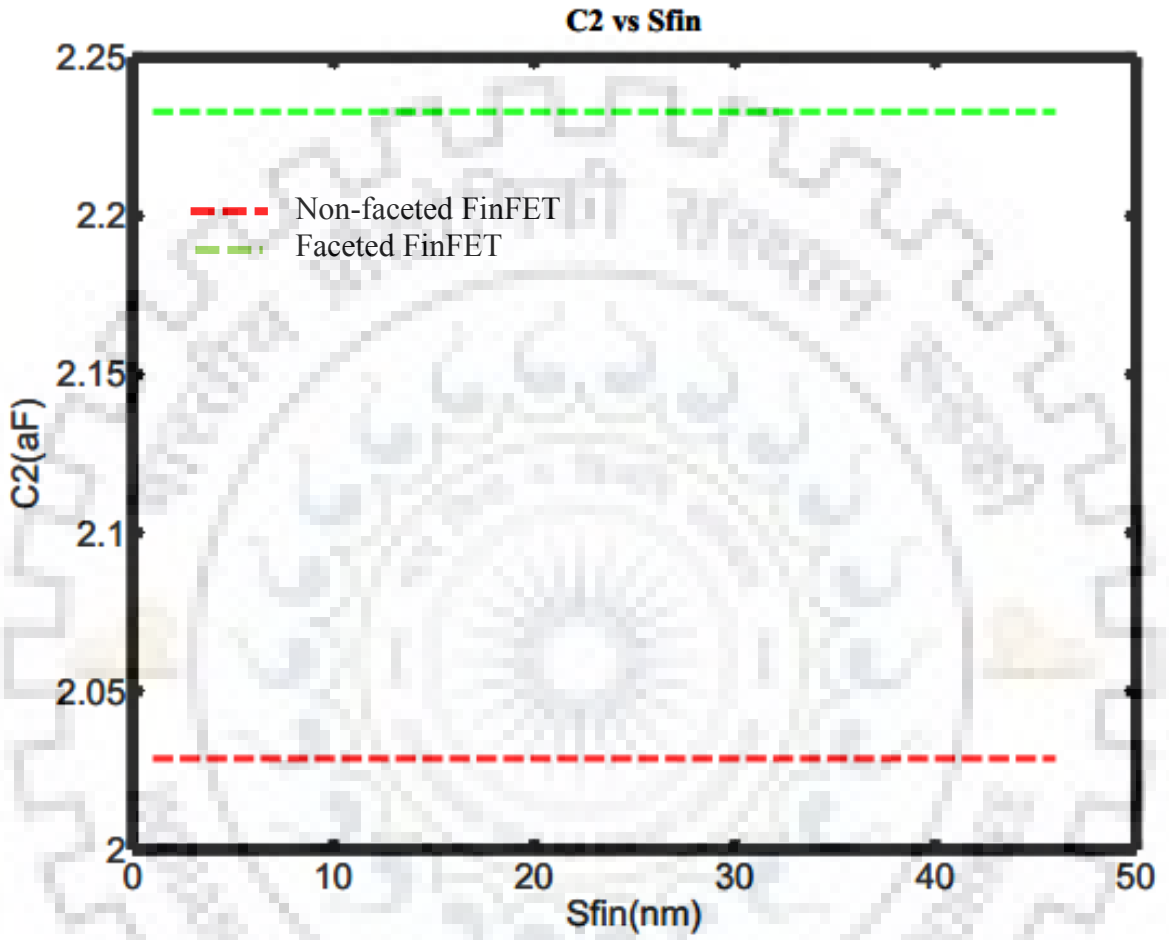


Figure 3.6: Variation of C_2 with spacing between the fins.

Figure 3.6 shows the variation of C_2 with the spacing between the fins. C_2 is the capacitance between the side of the gate and top of the fin along with the top of the inclined surface of the fin. In figure 3.6 red line depicts the non-faceted FinFET and green line depicts the faceted FinFET. As shown in figure 3.6 the C_2 is constant which matches with the results [14] and verifies that it is independent of S_{fin}. From the comparative result of 3 (b) shows that faceted structure offer more capacitance as compared to the non-faceted structure due to additional term in analytical eq. (3.4)

(iii) Variation of C_3 with spacing between the fins.

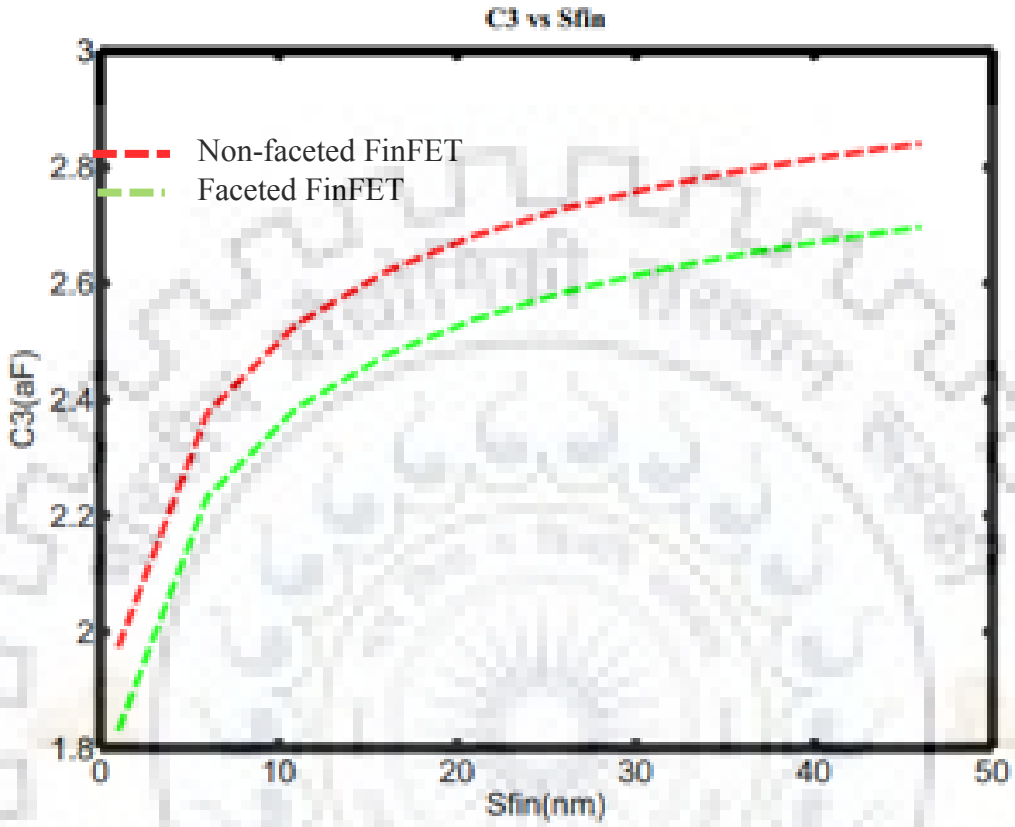


Figure 3.7: Variation of C_3 with spacing between the fins.

Figure 3.7 shows the variation of C_3 with spacing between the fins. C_3 is the capacitance between the side wall of the gate and side of the fin along with the side of inclined surface of fin. As shown in figure 3.7 C_3 of faceted structure is decreased when compared to the non-faceted FinFET and C_3 increases non -linearly with the spacing between the fins. So by faceting the shape of fin C_3 is reduced in comparison to the non-faceted FinFET due to reduction in effective height of fin.

(iv) Variation of C_4 with spacing between the fins.

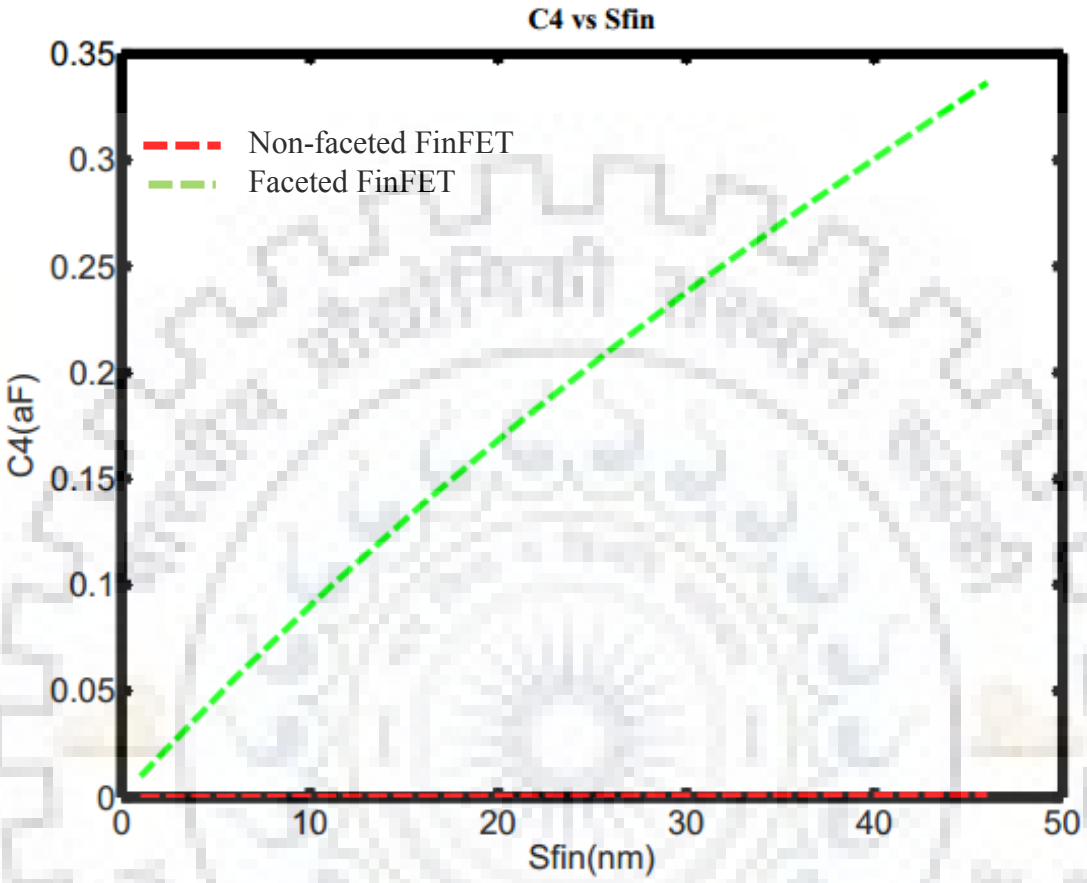


Figure 3.8: Variation of C_4 with spacing between the fins.

Figure 3.8 shows the variation of C_4 with spacing between the fins. C_4 is the capacitance between the side wall of the gate and side wall of the source drain pad. This increase appears due to the tapered face. Since, the slope of this face increases the height of the fin.

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(v) Variation of C_5 with spacing between the fins.

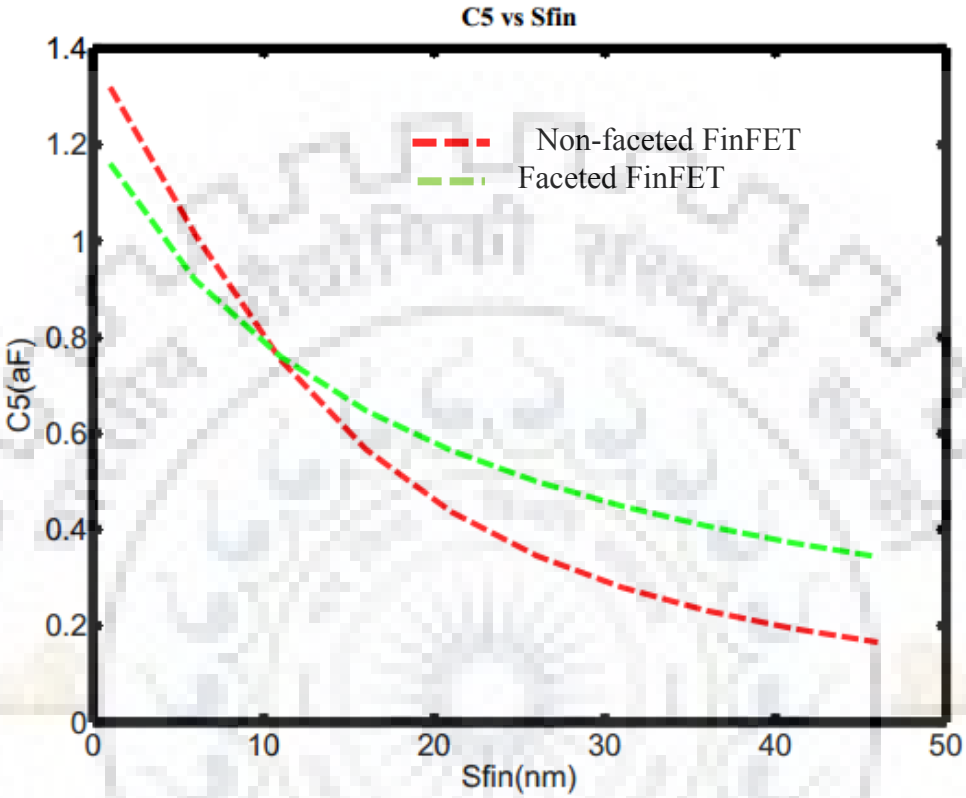

Figure 3.9: Variation of C_5 with spacing between the fins.

Figure 3.9 shows the variation of C_5 with the spacing between the fins. C_5 is the capacitance between the side wall of the fin and end of the gate. In figure 3.9 red line depicts the non-faceted FinFET and green line depicts the faceted FinFET. .From fig. 3.9 we can conclude that for S_{fin} less than 12 nm faceted FinFET offers less capacitance and this decrease can be controlled by taper angle ϕ.

(vi) Variation of C_6 with spacing between the fins.

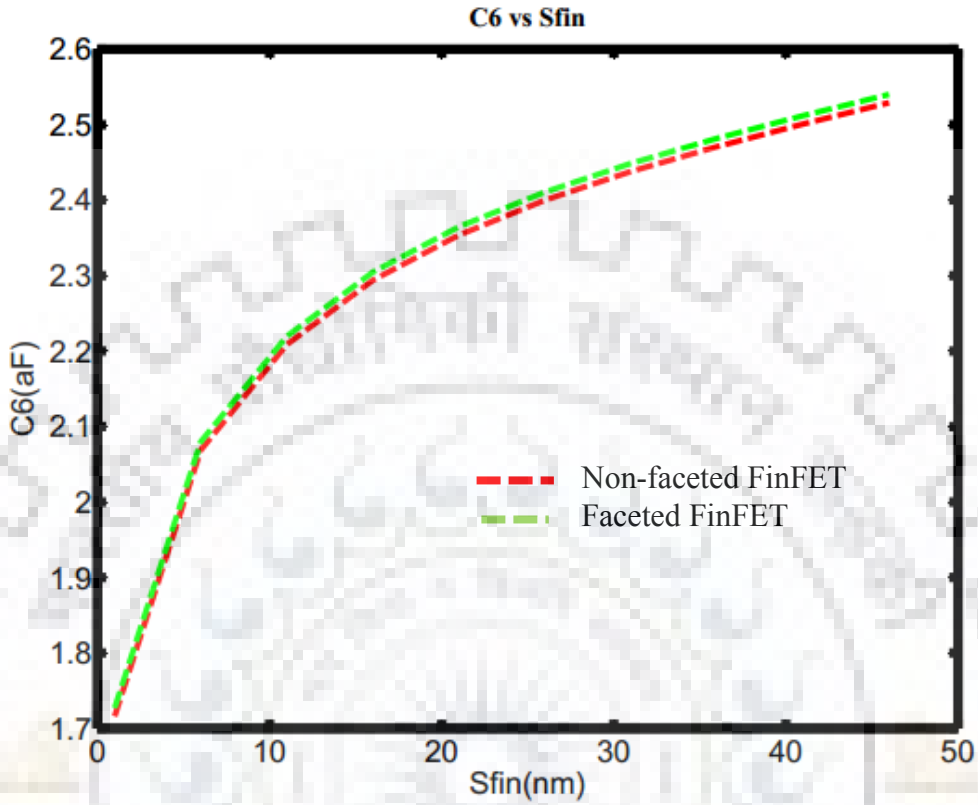

Figure 3.10: Variation of C_6 with spacing between the fins.

Figure 3.10 shows the variation of C_6 with the spacing between the fins. C_6 is the capacitance between the inner side wall of the gate and side of the fin along with the side of the inclined surface of the fin. In figure 3.10 red line depicts the non-faceted FinFET and green line depicts the faceted FinFET. It is clear from the figure that tapered face has no significant effect on capacitance C_6.

(vii) Variation of C_7 with spacing between the fins.

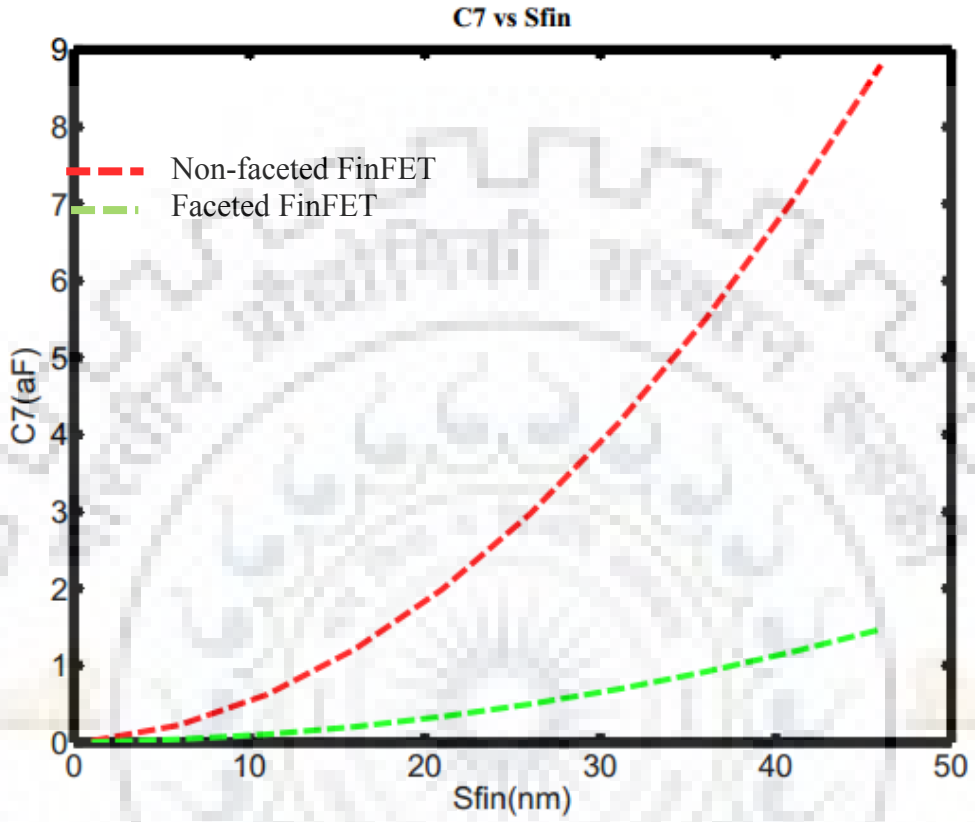

Figure 3.11: Variation of C_7 with spacing between the fins.

Figure 3.11 shows the variation of C_7 with the spacing between the fins. C_7 is the capacitance between the inner side wall of the gate and inner side wall of the source and drain pad. In fig 3.11 we can see that capacitance C_7 is remarkably reduced and this reduction appears here is because of lowering of effective height.

(viii) Variation of C_{total} with spacing between the fins.

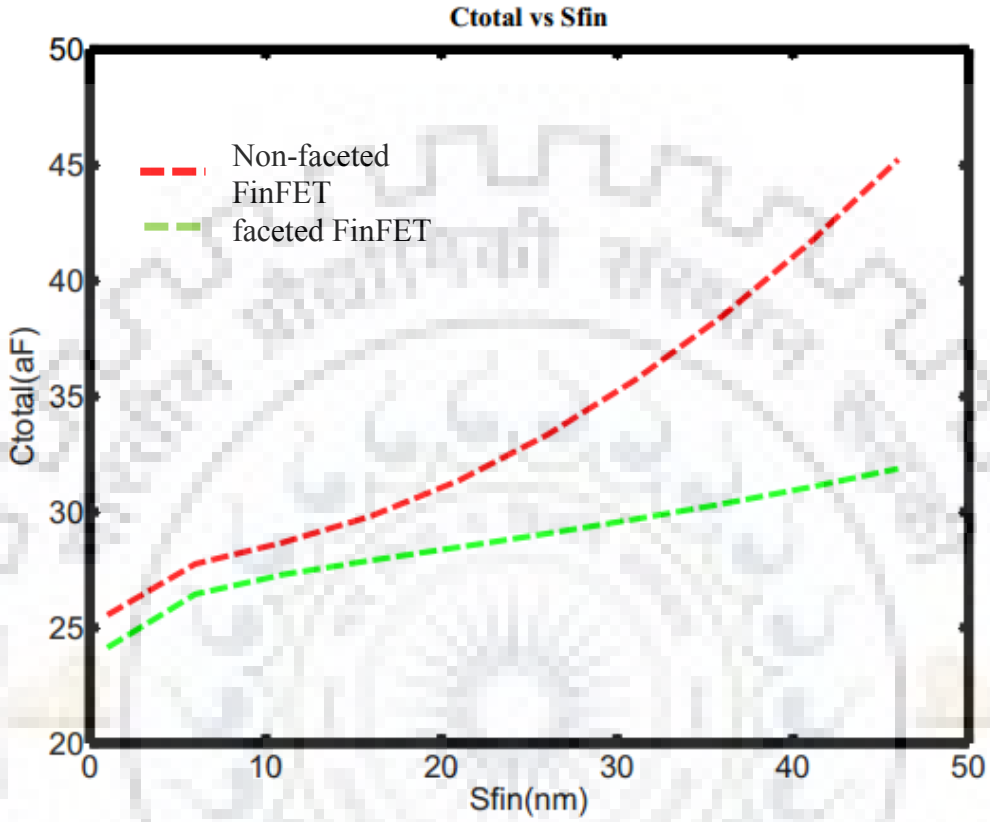

Figure 3.12: Variation of C_{total} with spacing between the fins.

Figure 3.12 shows the variation of C_{total} with the spacing between the fins. C_{total} is the total fringing capacitance of the two fins faceted FinFET. In figure 3.12 red line depicts the non-faceted FinFET and green line depicts the faceted FinFET. From fig 3.12 it is confirmed that faceted FinFET structure offers less capacitance. This improvement is observed because of C_1, C_3, C_7 are dominant in total fringing capacitance which consequently decreases the total fringe capacitances.

CONCLUSION and FUTURE SCOPE

In this dissertation report, an analytic model is derived for the fringing capacitances of faceted FinFET using conformal mapping technique and compared it with the corresponding capacitances of non-faceted FinFET and it is found that by changing the shape of fin i.e. by changing the area of coupling of between two surfaces, total fringing capacitance of increased with the increase in spacing between the fins. While when we compare the total fringing capacitances of the faceted and non-faceted FinFET structure we notice that total fringing capacitance of the faceted FinFET structure is reduced. The reduced fringe capacitance may be advantageous in terms of smaller delay and higher switching speed.

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