SILICON NANOWIRE CMOS CIRCUIT DESIGN AND RELIABILITY

Ph.D. THESIS

by

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **"SILICON NANOWIRE CMOS CIRCUIT DESIGN AND RELIABILITY"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electronics and Communication Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from September, 2013 to April, 2019 under the supervision of Dr. S. K. Manhas, Associate Professor, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(OM PRAKASH)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

(S. K. Manhas)
Supervisor

Date:_________

ABSTRACT

Silicon nanowire (SiNW) FET is one of the most promising candidates at extremely scaled technology nodes due to its superior channel controllability and CMOS compatibility. An accurate physics-based compact model is necessary for process and circuit design engineer to predict the available silicon data for highly scaled dimensions. Moreover, the model can also be used to accelerate the device-circuit co-optimization, which will reduce the fabrication cost and development cycle at the starting phase of future technology. In this study, we develop a unified Verilog-A compact model for lateral SiNW FET circuit design and analysis. The compact model incorporates important nanoscale effects as well as the geometry-dependent parasitic capacitances and resistance models. The parasitic models are scalable and TCAD calibrated. The Verilog-A model is calibrated to accurately match with reported experimental and TCAD based single & multiwire SiNW FET I-V and C-V characteristics.

We have designed SiNW FET based basic core logic gates such as INVERTER, NAND, NOR, Buffer, XOR, XNOR and analyzed their performance. It is seen that the SiNW CMOS based logic gates have better power dissipation (~3-4X), energy-delay product (~2-3X), and power delay product (~3X) compared to corresponding FinFET based designs. Further, we have examined stability metrics (e.g., read, write noise margins and access time), geometrical variability, and layout area optimization of SiNW FET based 6T SRAM employing multiwire sizing technique. The different NW SRAM design configurations (e.g., C_111, C_123, etc., where C_111 denotes the number of wires in pull up (PU), access (ACC), and pull down (PD) transistors respectively) are investigated. Among all design configurations, C_112 is found to be the best configuration considering overall performances such as write stability, speed, layout area, and variability tolerance.

Bias temperature instability (BTI) is one of the major reliability concern at nanoscale nodes and requires an accurate model to predict device and circuit performance. BTI includes negative bias temperature instability (NBTI) and positive bias temperature instability (PBTI), which occurs on p and n-type SiNW FET devices respectively. The stress and recovery BTI model for Si NW FET is obtained from the experimental SiNW FETs using a range of stress voltage, time, and temperature. Thereafter, the developed Verilog-A compact model is integrated with

the BTI model for nanowire (NW) CMOS circuit simulation and design. It is found that NBTI is more pronounced in SiNW FET compared to FinFET and planar MOSFETs. This is attributed to its cylindrical gate structure resulting in enhanced 2-D hydrogen diffusion and stress-induced Si/SiO2 traps. Using the developed model, the impact of NBTI on NW CMOS circuits: inverter, 13-stage ring oscillator (RO), and 6T SRAM performance is analyzed. It is found that initially (for 1 year of a lifetime) due to fast trapping, inverter delay, and RO frequency degrade rapidly and saturates in long-term 10-year lifetime. Further, the combined impact of NBTI and PBTI are analyzed in circuits and a method is proposed to mitigate their impact. We demonstrated that the delay degradation is circuit topology dependent in which series-connected transistors are more prone to degradation due to PBTI (NBTI) in NAND (NOR) gates. Finally, the design of SRAM cell employing multi-wire sizing technique is investigated. It is found that the SRAM cell design margins are configuration dependent in which impact of BTI degrades the RNM by 15 % - 30 % and WNM improves by 5 % - 8 % for 10-year lifetime. We show that the BTI impact on SRAM cells is configuration dependent, which can be reduced by using appropriate design configuration. This study underscores the need for mitigating BTI degradation in NW CMOS, both at the device and circuit level.

Finally, the combined impact of time zero variability and BTI reliability on the core logic gates and read/write stability of the 6T SRAM cell is investigated. We found that the combined impact of time zero variability and BTI reliability degrades the mean and sigma value of circuit delay and SRAM RNM stability. We propose a method to minimize degradation under the influence of variability and reliability by selecting appropriate NW FET design configuration. It is found that overall the C_112 is the best SRAM cell design configuration, having higher read/write reliability and variability tolerance. The comprehensive predictive model framework presented here is a valuable tool for variability and reliability-aware SiNW CMOS circuit design and analysis. The results and developed model of SiNW FET presented in this thesis are important benchmarks for the future studies in SiNW CMOS circuit design.

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ABBREVIATIONS AND SYMBOLS

ACC	Access Transistor
BL/BLB	Bit Lines
BWTV	Bit Line Write Trip Voltage
C_{if}	Inner Fringing Capacitance
CMOS	Complementary MOS
C_{of}	Outer Fringing Capacitance
C_{ov}	Overlap Capacitance
C_{ox}	Oxide Capacitance
CS	Common Source Amplifier
C_{side}	Sidewall Capacitance
D	Diameter
DIBL	Drain Induced Barrier Lowering
E_a	Activation Energy
E_{ox}	Stress Field
$\mathcal{E}_{si}$	Permittivity of Silicon
F	Minimum Feature Size
FO	Fan Out
f_{SCE}	Short Channel Effect factor depends on L_g and λ
H	Height of the cell
HSNM	Hold Static Noise Margin
k	Boltzmann Constant
LEG	Line Edge Roughness
L_{EXT}	Extension Length
L_g	Channel Length
MC	Monte Carlo
MGG	Metal Gate Granularity
NBTI	Negative Bias Temperature Instability
n_i	Intrinsic Carrier Potential
nSiNW	Silicon Nanowire of N-type
NW	Nanowire
PD	Pull Down Transistor

pSiNW	Silicon Nanowire of P-type
PU	Pull Up Transistor
q	Electronic Charge
QMC	Quantum Mechanical Confinements
RAT	Read Access Time
R_{CON}	Contact Resistance
R_{EXT}	Source/Drain extension resistance
RNM	Read Noise Margin
RO	Ring Oscillator
R_{sp}	Spreading Resistance
R_{total}	Total Resistance
SCE	Short Channel Effects
SINM	Static Current Noise Margin
SiNW FET	Silicon Nanowire FET
SRRV	Supply Read Retention Voltage
SS	Sub Threshold Slope
SVNM	Static Voltage Noise Margin
T	Temperature in Kelvin
TCAD	Technology Computer Aided Design
T_{CLK}	Clock Period
t_o	Stress Time
T_{ox}	Gate Oxide Thickness
T_{PHL}	High to Low Propagation Delay
T_{PLH}	Low to High Propagation Delay
V_{read}	Read Voltage
VTC	Voltage Transfer Characteristics
V_{th}	Threshold Voltage
V_{WL}	Word Line Voltage
W	Width of the Cell
WAT	Write Access Time
WM	Write Margin
WNM	Write Noise Margin
WRRV	Word Line Read Retention Voltage
WTI	Write Trip Current

WTV	Write Trip Voltage
WWTV	Word Line Write Trip Voltage
α	Degradation Factor
λ	Feature Size
σV_T	Threshold Voltage Deviation
$\Psi(\rho)$	Channel Potential
ΔV_{it}	Interface Trapped Changes
ΔV_T	Change in V_T
$\Delta V_{thr}(t)$	Degradation at time t
μ	Mean Value of Noise Margin
μ_{deg}	Mobility Degradation Factor
μ_{delay}	Mean Value of Delay
μ_{RNM}	Mean Value of RNM

1 CHAPTER

Introduction

1.1 CMOS Scaling and Advanced MOSFET Structures

The need for higher packaging density, faster switching speed, lower power consumption, and the cheaper cost has been fueling persistent CMOS scaling over the last four decades. Scaling of traditional MOSFETs is achieved by the combination of a reduction in gate dielectric thickness, variation in body doping, and reduction in source/drain junction depth [1]–[3]. A thinner gate oxide enhances the gate control over the channel, but at the same time, it leads to an exponential increase in the gate oxide leakage current due to the tunneling across dielectric [4]. Moreover, high channel doping increases the surface electric field for a given inversion level and thus induces mobility degradation due to surface scattering and Coulomb scattering [5]. In addition, the larger body doping also exhibits random dopant fluctuation, consequently, instigates threshold voltage/current variations in scaled devices.

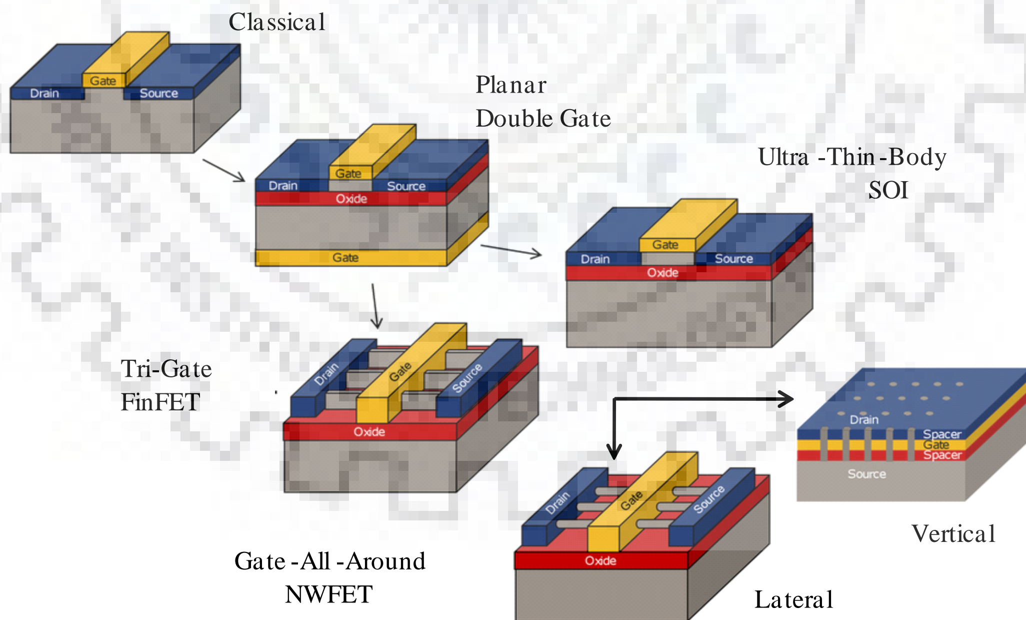


Figure 1.1 Evolution of device structure from single gated to GAA NW FET[1].

With the invention of advanced fabrication techniques, high-k gate dielectric, process induced strain [2], new device materials, the scalability of bulk CMOS is still limited due to extensive short-channel effects (SCEs) [3]. Therefore, the classical bulk MOSFET has been

replaced by silicon-on-insulator MOSFET (SOI) [4], Multi-gate devices such as double gate FinFET[5]–[8] and 3D devices such as tri-gate FinFET[5] and silicon nanowire (SiNW) FET [9]–[11]. Figure 1.1 shows the evolution of MOSFETs from the classical single gate through Multi-gate FinFETs to gate all around (GAA) or silicon nanowire FET for improvement in the electrostatic gate control [1]. Among all these devices, SiNW FET is the leading candidate in nanometer regime due to its extraordinary gate control capability, improved transport properties, short channel immunity, and CMOS compatibility [12], [13]. Moreover, SiNW FET employs a very thin undoped body to suppress surface leakage path, therefore, reduce SCEs. An undoped or lightly doped body eliminates threshold voltage (V_{th}) variation due to random dopant fluctuation [14], enhances carrier transport resulting in higher ON current[15]. Unlike planar MOSFETs, the SiNW FET can be scaled without a proportional reduction in the gate oxide thickness[16]. Therefore, the SiNW FET is the most promising and potential device for the nanoscale regime.

1.2 Lateral Silicon Nanowire Field Effect Transistor

A simplified 3D view of SOI silicon multi nanowire (NW) FET structure is shown in Figure 1.2. The channel, including the extension length is surrounded by the gate oxide. Moreover, the channel region along with the oxide is surrounded by the gate electrode to form a gate of the NW transistor. By applying the appropriate gate bias, the channel conductivity can be modulated and after which the volume inversion is expected to occur in the device [17]. The volume inversion in Si-NW FET renders the channel charge carriers relatively free from the surface scattering [18]. Due to the unique cylindrical structure of NW, it has an advantage of relatively less sensitivity to many more process induced parameter (such as random dopant fluctuation (RDF)) variations compared to other technologies. Moreover, it has been observed that the SiNW FET based 2-inputs NAND gate shows a more than four times less performance variation than its planar MOSFET equivalent and nearly two times less than FinFET devices at the 32 nm and 45 nm technologies node, respectively [19]. In the case of planar MOSFETs and FinFETs, the variation in the oxide thickness strongly affects the strength of drive current and gate capacitance. However, in case of SiNWFET, the gate capacitance has a logarithmic dependence on oxide thickness due to the cylindrical structure which restricts the change in the drive current due to the oxide thickness variation to almost negligible. Further, the variation in channel length causes a lesser impact on the current drive strength of silicon nanowire FET as compared to planar MOSFETs [19]. In conclusion, NW FETs possesses a higher margin for

process parameter variations than planar and FinFET devices. In the planar MOSFETs and FinFETsthe current drive can be modulated by varying channel length, width, Fin thickness and number of parallel fingers in the transistor. Whereas, in nanowire-based devices the current drive strength can be increased by changing the geometrical parameters such as diameter, channel length, extension length and a number of wires [20]. There have been numerous research groups and industries working on the SiNW FET device in the recent years such as IMEC [21], IBM [22], Samsung [23], Institute of Microelectronics Singapore (IME) [24], and Peking University Beijing. The nanowire devices have gained a lot of attention over the past decade due to excellent scalability [25]. This underlines the importance and potential of the multigate or novel devices to extend existing MOSFET scaling limits. Therefore, in order to analyze the multi-gate circuit design, variability, and reliability. Physics-based Verilog-A compact model integrated with the reliability model is needed for timely understanding and fast analysis of NW circuit performance.

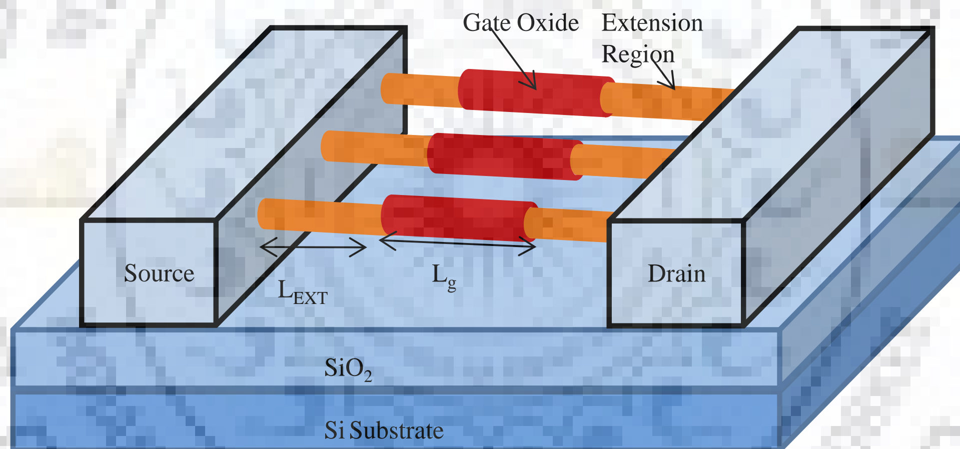


Figure 1.2 3D view of SOI multi-silicon nanowire FET device.

1.3 Compact Modeling of Multi-Gate Devices

A physics-based compact model for Multi-Gate devices expresses in the mathematical form of its complex behavior, and it is implemented in a computer programming language like C or Verilog-A. Moreover, in order to evaluate the capability of such 3D devices in nanoscale regime, a compact model ((I-V), (C-V)), is essential, which can be used to evaluate circuit's performance in a short time. The compact model serves as the bridge between process technology and circuit design. The circuits are always precisely implemented and tested by circuit simulators such as HSPICE, and Cadence, where compact models represent a mathematical form of the complex behavior of device physics in the transistor. It enables the

balance between accuracy and simplicity. An accurate physics-based compact model allows the process and circuit design engineer to make a prediction beyond the available silicon data for highly scaled dimensions, and also enable fast device and circuit co-optimization. Figure 1.3 shows the flow chart for the development of the compact model.

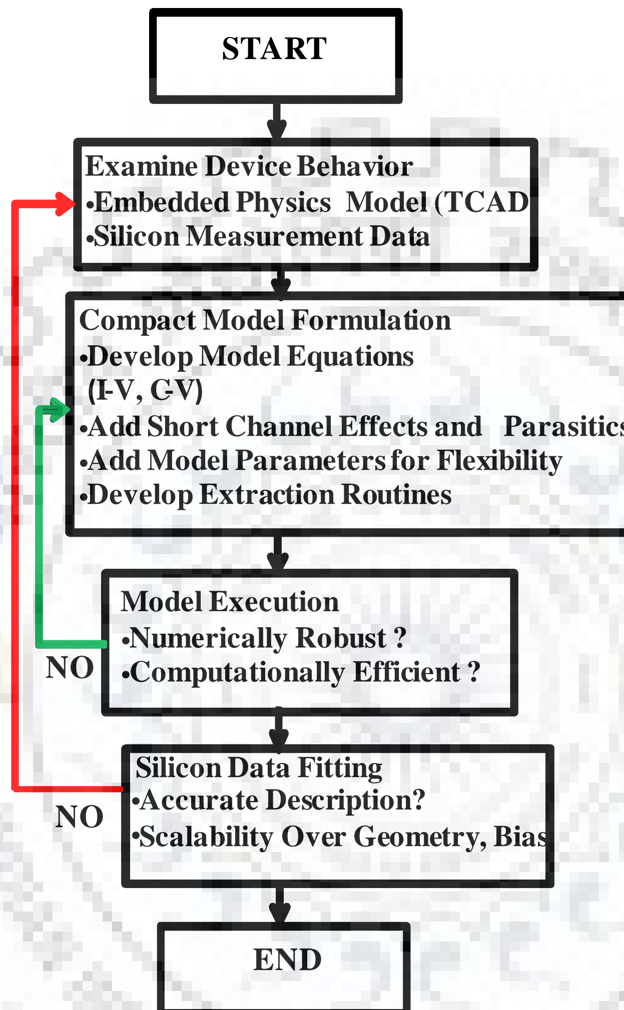


Figure 1.3 Flow chart for the development of compact model [26].

Despite the fact that the implementation might consist thousandsof lines of codes, it takes only a second for computer simulation tools like SPICE [45] to execute the code (for one transistor at a single bias point). One of the major challenges in compact modeling is to address convergence issues. Moreover, the model must be continuous over the entire voltage range (positive to negative voltage). The compact model for nanoscale devices should include all short channel effects like mobility degradation, velocity saturation, and quantum confinement. The model should also comprise scalable geometry dependent parasitic capacitance and resistance, which become highly dominating factors for nanoscale devices.

1.4 Compact Negative/Positive Bias Temperature Instability

NBTI is a physico-chemical mechanism, which occurs in negatively biased ($V_{gs}<0$) p-SiNW FET devices at an elevated temperature, and causes the generationof interface trap charges at Si/oxide interface. Consequently, there is an increase in the threshold voltage with time and hence, a reduction of current strength [27]. NBTI also exhibits a peculiar property of recovery, i.e., when bias is removed (for positive gate voltage) the threshold voltage of p-SiNW FET recovers towards its initial unstressed value. On the other hand, positive bias temperature instability (PBTI) has reemerged as an important reliability concern for n-MOS FET devices in an ultra-scaled transistor which can degrade the threshold voltage and I_{ON}. The shift in V_T due to PBTI in n-MOSFETS FET with stress voltage, temperature and stress time is due to (i) electron tunneling and trapping into the pre-existing oxide traps, (ii) newly generated traps in bulk oxide due to high oxide field [28], (iii) stress-induced defects in gate oxide during the fabrication process causing larger oxide charge trapping. The NBTI/PBTI threshold voltage modeling and the impact on SiNW FET circuits performance arepresentedin more detail in the further chapters.

1.5 Motivation

To overcome the scaling issues in planar MOSFET, novel devices like ultra-thin body FET, FinFET, silicon nanowire (SiNW) FET etc. have been proposed [1]. Among them, SiNW FET is considered as a most promising alternative to address the scaling challenges in 1X and below technology nodes, due to its excellent short channel effect (SCE) immunity, high I_{ON}/I_{OFF} ratio and CMOS compatibility [29].

In order to evaluate the capability of such 3D device in the nanoscale regime, a compact model is required for performance analysis through device circuit simulations. The model included all the nanoscale effect nanoscale effect and more importantly it includes the geometrical parasitic capacitance and resistance model which are highly dominating at the nanoscale regime.

However, in the new device structures and nano-scale technologies, reliability, variability, and circuit design are the big challenges that need to be understood and characterizes. The small device dimensions (e.g. channel length, oxide thickness) causes high lateral/vertical electric fields resulting in hot carrier induced degradation (HCI) [30], time-dependent dielectric breakdown (TDDB) and negative/positive bias temperature instability (N/PBTI). Among these

effects, NBTI and PBTI reliability are the most significant reliability concerns for any CMOS technology in sub-nanoscale nodes. Therefore, the predictive BTI threshold voltage model is necessary to develop for the long term prediction of NW device and circuit performances. In addition, the nanoscale device dimensions have brought a significant device to device random as well as systematic process-induced variation. It may lead to significant uncertainty in the circuit performance, which also needed to consider for circuit design and optimization.

In this thesis, we developed a comprehensive framework in which Verilog-A compact model integrated with a predictive BTI reliability model for NW circuit design and analysis. Our study establishes important benchmarks for NW CMOS circuit design. The presented model has a high potential for incorporation in circuit simulation tools.

1.6 Objectives

In this thesis, an accurate physics based Verilog-A compact model and bias temperature instability (BTI) model of silicon nanowire (SiNW) FET have been developed. Further, the developed BTI model is integratedinto the compact model for NW CMOS circuit design and reliability analysis. The study has the following objectives:

i. The silicon nanowire FET Verilog-A compact model is required which includes all the nanoscale effects and most importantly, it includes parasitic capacitance and resistance model for the accurate circuit simulations.
ii. Analysis of the SiNW FET based 6T SRAM cell in terms of stability metrics (e.g. read, write noise margins and access time), layout area optimization and impact of geometrical variability and find the most suitable cell design for the best performance.
iii. Bias temperature instability (BTI) is an important reliability issue for nanoscale 3D devices such as FinFETs and silicon nanowire FET. Therefore, the extensive device reliability characterization and threshold voltage predictive modeling is needed for reliable NW circuit design.
iv. Develop a comprehensive framework in which Verilog-A compact model is integrated with BTI model for NW CMOS circuit design.
v. The impact of NBTI on NW CMOS circuits: inverter, 13-stage ring oscillator (RO) and 6T SRAM performance. Moreover, the combined impact of BTI (NBTI+PBTI) and

time zero variability on NW CMOS circuits: basic logic gates (Inverter, NAND, and NOR), 6T SRAM cell are required to analyze.

1.7 Outline of the Work

This thesis is based on the objectives discussed in section 1.5. The thesis consists of seven chapters. Each chapter begins with a brief introduction pertaining to the concerned problem and motivation behind the study. Moreover, the results are summarized and discussed at the end of each chapter. The outline of each chapter is as below:

Chapter 1 presents the overview and evolution of novel device structure from single gate to gate all around MOSFET. Further, compact modeling development steps, bias temperature instability reliability, variability and impact of reliability on circuits are presented. The chapter also includes the motivation of taking the specific problem for the purpose of the present and future research work. Furthermore, it presents the outline of the complete thesis work.

Chapter 2 presents an extensive literature review on silicon nanowire I-V, C-V compact modeling, bias temperature instability (BTI), variability and impact of reliability on silicon nanowire based circuit design. This chapter brings forward various technical gaps based on the literature survey.

Chapter 3 presents a unified Verilog-A compact model for lateral silicon nanowire field effect transistor (SiNW FET). The model incorporates all nanoscale effects including short channel effects, velocity saturation, mobility degradation, and quantization. Importantly, the model includes geometry dependent, TCAD calibrated, scalable parasitic capacitances and parasitic resistance models, which are dominant at the highly scaled dimension. The model is well calibrated with published experimental NW devices and the TCAD I-V and C-V characteristics for single and multiwire long, short channel devices. Further using the compact model, the static and dynamic analysis of the CMOS inverter with 10 nm gate length is presented, which match well with TCAD simulations. Using this model the impact of device parasitic on circuit performance is studied by varying device extension length and multiwire.

Chapter 4 presents a core logic gates design for advanced 10 nm lateral SiNW FET technology in super threshold regime. Further, analysis of the stability metrics (e.g. read, write noise margins, and access time), geometrical variability and layout area optimization of silicon

nanowire field effect transistor (SiNW FET) based 6T SRAM with multiwire sizing technique is presented. The SRAM cell analyzed in this chapter is based on the TCAD and experimentally verified SiNW FET Verilog-A compact model with parasitics. The different NW SRAM design configurations (e.g. C_111 and C_123 etc., where C_111 denotes the number of wires in pull up (PU), access (ACC) and pull-down (PD) transistors respectively) are investigated. Finally, the impact of geometrical variability including length, radius and oxide thickness on the read and write stability using N-curve is examined. It is found that the static read and write stability is less susceptible to variability at the nominal supply voltage. However, it is very sensitive to the voltage scaling. Among all design configurations, C_112 is the better configuration for considering overall performances such as write stability, speed, layout area and variability tolerance.

Chapter 5 reports well calibrated predictive and scalable Verilog-A based compact model, integrated with NBTI model for nanowire (NW) CMOS circuit simulation and design. The stress and recovery NBTI model for Si NW FET is obtained from experimental NW pMOSFETs using range of stress voltage, time, and temperature. Further, we have analyzed the impact of PBTI on nSiNW FET and developed a threshold voltage predictive model. Finally, the complete simulation flow chart for the integration of BTI model in Verilog-A model for circuit simulation is presented. This study underscores the need for predictive modeling and mitigation of NBTI/PBTI degradation in NW CMOS, both at the device and circuit level.

Chapter 6 presents the impact of NBTI on NW CMOS circuits: inverter, 13-stage ring oscillator (RO), and 6T SRAM performance is analyzed. Finally, the design of SRAM cell employing multi-wire sizing technique is investigated. We show that the NBTI impact on SRAM cells is configuration dependent, which can be reduced by using appropriate design configuration. Further, the impact of BTI (NBTI+PBTI) on the logic gate delay and SRAM cell read/write static stability has been analyzed. Thereafter, the combined effect of time zero variability and BTI reliability on the core logic gates (INVERTER, NAND, and NOR) delay and read/write stability of the 6T SRAM cell is analyzed. The comprehensive predictive model framework presented in this chapter is a valuable tool for variability and reliability-aware SiNW CMOS circuit design and analysis.

Chapter 7 concludes the thesis. Conclusions are drawn based on the obtained results. The future scope of the work is also presented in this chapter.

The thesis ends with a complete list of references along with our publications based on the research work carried out.

2 CHAPTER

SiNW FET Compact Modeling and BTI Reliability: Literature Review

In the previous chapter, the introduction of this thesis is presented with an emphasis on silicon nanowire (SiNW) FET compact modeling and circuit design. In this chapter, the SiNW FET based compact modeling, the basic mechanism of bias temperature instability, variability, and its impact on circuit design related literature are discussed and research gap which is examined in this thesis are identified. Finally, the chapter is concluded by identifying the research gaps to be addressed through this thesis.

2.1 SiNW FET Compact Modeling

The accurate compact models of SiNW FET devices are necessary for all types of circuit designs such as digital, analog and mixed signal. A compact model is a concise mathematical description of the semiconductor device complex behavior such as current-voltage, terminal charges, and capacitance-voltage characteristics. Initially, *Yijian Chen et al*. [31] modified the analytical model of *Taur* [32] double gate MOSFETs to study the undoped NW MOSFET in strong inversion and accumulation region. Moreover, on the basis of charge analytical solutions obtained, the concentration of inversion charge carrier for double-gate MOSFETs is compared with the NW MOSFETs. It is observed that the NW MOSFETs possess significantly higher inversion charge concentration compared to double-gate MOSFETs under the influence of same surface potential applied, which indicates a potentially higher current drive strength and excellent gate control. Subsequently, *D. Jiménez and B. Iñíguez* group [33], [34] proposed a current-voltage model for NWFET with three distinct assumptions or features as follows: (i) considered channel as undoped (lightly doped), because as expected additional dopants in the ultra thin body MOSFETs would lead to threshold voltage statistical fluctuation, (ii) the current for all the operation regions i.e. linear, saturation and sub-threshold are described by one continuous function, without using nonphysical fitting parameters, (iii) inclusion of the phenomenon of volume inversion. In 2005, *Benjamin Iñíguez et al*. [35] further reported explicit continuous dc I-V model for the long channel NW MOSFET. Unlike the previous

model [33] in which current equation is written as an explicit expression of the applied voltage, the new model for NW MOSFETs is depended upon the unified charge control model. This new model is very accurate and less dependent on empirical fitting parameters. The new model exhibits very smooth transitions throughout all regions of operation, which is very desirable in any circuit simulation. The Quantum Mechanical Effects (QME) were not included in the previously developed compact models due to its insignificant effects for silicon films thickness of more than 10 nm. The QME is considered for the silicon film thickness of less than 10 nm, as it leads to the shift in inversion charge density from the channel surface thus increase in the effective oxide thickness and threshold voltage [36]. All these models discussed so far are for the long channel undoped NW devices and consider a drift-diffusion mechanism for the carrier transportation. Further, *BenjamínIñiguez et al.*[37] presented the compact modeling principles and solution for nanoscale gate all around(GAA) MOSFETs. In this model, they focused on the main challenges of the nanoscale MOSFETs such as quantum mechanical effects due to quantum confinement, quasi-ballistic or ballistic transport, short channel effects (SCE), gate oxide tunneling current, and drain induced barrier lowering (DIBL).

However, for circuit design and analysis only accurate continuous I-V model is not enough. In order to perform the dynamic analysis or ac and transient circuit simulation, terminal charges or capacitances are also required [38]. The model should continuously cover all the regions of operation, without use of any nonphysical fitting parameters. The existing NW MOSFET models are only valid for the undoped or lightly doped body, but due to processing and technology limitations, the practical silicon substrate always contains dopants. To overcome this, *Feng Liu et al.* [39] reported a charge-based model for the long-channel silicon nanowire FETs to illustrate the inversion charge and drain current, which is applicable for a lightly doped to a heavily doped channel.

Jie Yang et al. & S. Venugopalan [40], [41] have proposed a complete long and short channel NW FET physics based compact model for circuit simulation. The model is divided into two parts, first the core model description such as I–V and C–V which are very accurate for a broad range of bias, doping concentrations ranging from 10^{10} cm^{-3} to 10^{19} cm^{-3}[42]. Second, the model included advanced physical effects such as short channel effects and quantum mechanical effects, etc. *Bastien Cousin et al.* [43] and *Jin Xiao-Shi et al.* [44], presented a continuous and explicit model valid in all operating regions, for undoped square and junction less cylindrical GAA MOSFETs. *XingZhau et. al* [45], [46] developed a MOSFET model

(Xsim), for the unification of various types of devices, such as bulk, partially/fully SOI, double gate (DG) FinFETs, and gate all around silicon nanowire (SiNW FET) based on the unified regional modeling (URM) approach. All these silicon nanowire FET compact models are developed without considering the geometrical parasitic capacitance and resistance which are highly dominant in the nanoscale regime.

The extrinsic geometrical parasitic capacitance/resistance has come out as a significant scaling issue in deeply scaled devices, particularly for novel 3D devices such as FinFET and silicon nanowire FETs. For SiNW FET, several authors have reported an analytical intrinsic and extrinsic gate capacitance model in [47]–[49]. The intrinsic device capacitances reduce or relatively less impactful at highly scaled dimensions of the NW FET channel. However, the extrinsic geometrical parasitic capacitance/resistance affects the performance of SiNW FET circuits significantly. The NW FET parasitic gate capacitances are broadly divided into following components (i) outer fringe capacitance from source/drain pad to gate, (ii) inner fringe capacitance from gate to extension region, (iii) sidewall capacitance (iv) overlap capacitance. Out of all these parasitic capacitance, outer fringe from source/drain pad to gate is the most dominating and major contributor to the overall NW gate parasitic capacitance [49]. Moreover, sidewall capacitance manifests itself as a non-negligible parasitic capacitance. On the other hand, for a deeply scaled device below 22 nm regime, parasitic resistance is the dominant part of total device resistance since it does not scale proportionally with the device dimensions. Moreover, due to narrow diameter, the NW device exhibits higher series resistance and hence severely impacts the device and circuit performance. The series parasitic resistance is divided into five components namely extension resistance, spreading resistance, interface resistance, contact and deep source-drain resistance [50]. From the above discussion, we conclude that an accurate NW compact model is required which incorporates geometrical dependent parasitic capacitance and resistance models for real circuit operation.

2.2 Negative Bias Temperature Instability (NBTI)

2.2.1 NBTI Background

Negative bias temperature instability (NBTI) has been known since 1966 [51]. It is a physical and chemical mechanism, which occurs in negatively biased ($V_{gs}<0$) p-MOS devices at elevated temperature, and causes generation of interface trap charges at Si/SiO_2 interface [52]. The generated Si/SiO_2 interface traps causes drift in the threshold voltage (V_{th}) of p-MOSFETs,

thus reducing the channel carrier mobility and degrades the drain current of the device. The NBTI impact has been firstly reported by *Miura et. al* [51], and thereafter characterized by a research group at Bell Laboratories [53], RCA Laboratories [54], and Fairchild Semiconductor [55]. The NBTI is a severe reliability issue that threatens the operational life time of the device and degrades the circuit performance or leads to circuit failure over the life time [56]. At deeply scaled technologies, the thickness of the gate oxide has persistently decreased, and consequently, the threshold voltage V_{th} is also reduced proportionally. Moreover, numerous impacts have been conspired to bring NBTI to the attention of device and circuit designers: first, the operating supply voltage has not scaled at the same pace as the device dimensions, resulting in the enhancement of NBTI degradation due to higher vertical oxide field. Second, there is a large percentage degradation in the current drive strength, as the scaling of device V_{th} has not kept pace with operating supply voltage. Third, during the fabrication process, an addition of nitrogen contents into the gate oxide for the reduction of leakage has the adverse impact of enhancing NBTI.

The NBTI degradation during DC stress voltage primarily results from breaking of Si-H bonds at the Si/SiO_2 interface and resultant hydrogen atom or molecules diffuses away from the interface into the gate oxide and polysilicon gate. Many research groups have used several versions of reaction-diffusion (R-D) model to understand this phenomenon [57]–[60]. Further, with long stress time (t_{stress}>10-100s), threshold voltage shift shows power-law behavior ($\Delta V_{th} \sim t^n$) which is consistent over several decades with time exponent of n ~ 1/6 [61]. The R-D model attributes this robust long-term n ~ 1/6 time exponent to the diffusion of molecular hydrogen (H_2).

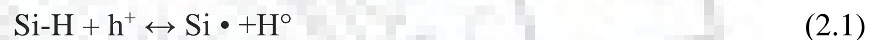
NBTI recovery is one of the peculiar properties which is observed when the device is unstressed, thus the degradation relaxes. This is attributed to the hydrogen annealing or re-passivation of the interface traps by the free hydrogen available in the gate oxide [62]. Many research groups have reported that the impact of NBTI is minor during AC stress (due to recovery) compared to continuous DC stress. Moreover, the ratio of AC to DC NBTI degradation factor is frequency independent for low frequency (<10-100kHz) [63], [64].

2.2.2 NBTI Mechanism

NBTI persists as a crucial reliability issue for deeply scaled p-MOSFETs, since it causes severe long term performance degradation for digital, analog, mixed signal, and memory circuits [65],

[66]. The major cause of NBTI reliability degradation is due to the formation of a silicon (Si)/ (SiO_2) interface and oxide bulk traps under the influence of high oxide field at elevated temperature. When the oxideis grown on top of silicon layer during device fabrication, it leaves dangling bonds at the interface, which act as trap centers. In order to prevent the formation of the dangling bond, the device is annealed in a hydrogen atmosphere, resulting in the passivation of dangling bonds and thus Si-H bond formation takes place. This scheme was quite effective for thicker gate oxides [67]. However, due to miniaturization, we now deal with devices of gate thicknesses in the order of a few nanometers, and hence, the oxide electric field is extremely high. These dangling bonds at Si/SiO_2 interface, however, are weak and under the application of a high electric field (corresponding to a V_g of about - 2 V), combined with a higher operating temperature (due to higher power dissipation), causes the bonds to dissociate, resulting again, in the formation of interface trap centers as shown in Figure 2.1. These interface trap centers act as sites for hole capture which ultimately increases the threshold voltage of the device.

The interface chemical reaction of p-MOSFETs during stress phase is given as [63]



$$\text{Si-H} + h^{+} \leftrightarrow \text{Si} \bullet + H^{\circ} \quad (2.1)$$

where the chemical equation (1) denotes the reaction of a hole h^+ with the Si-H bond results in the formation of donor-like Si/SiO_2 interface trap. The broken free H either diffuses away from the interface towards gate or re-passivates the interface dangling bond at elevated temperature.

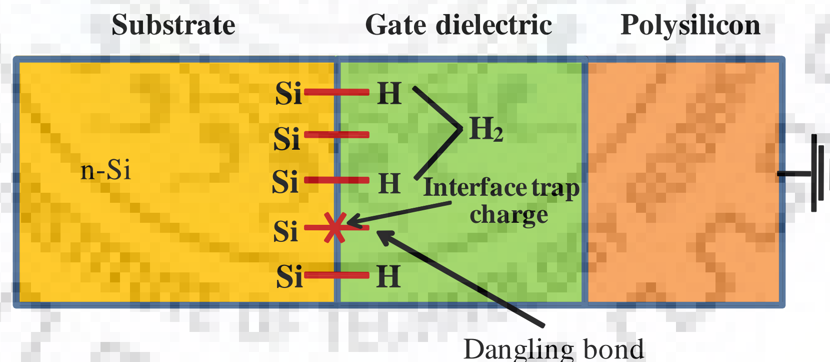


Figure 2.1 Prospective 2D view of silicon nanowire (NW) FET device during stress.

2.2.3 NBTI Recovery Behavior

When stress is removed, the broken hydrogen generated during the stress phase diffuses back towards the interface and reacts with the interface dangling bonds and passivates them as shown in Figure 2.2. The back diffusion takes place in the form of atomic hydrogen, molecular hydrogen or a combination of the both. Thereafter, the threshold voltage of the p-MOSFETs transistor recovers towards its initial unstressed value. This improvement in the threshold

voltage is mainly ascribed to the reduction in number of interface trap density [68]. With the reduction in the gate voltage for the p-MOSFETs, the constants governing the rates of forward and backward reactions in the R-D model are reduced, thus reducing the bond breaking rate, which has an exponential dependence on gate voltage [59]. The overall degradation under AC stress is less than the DC stress due to the recovery effect, which enhances the life time of the circuit operation.

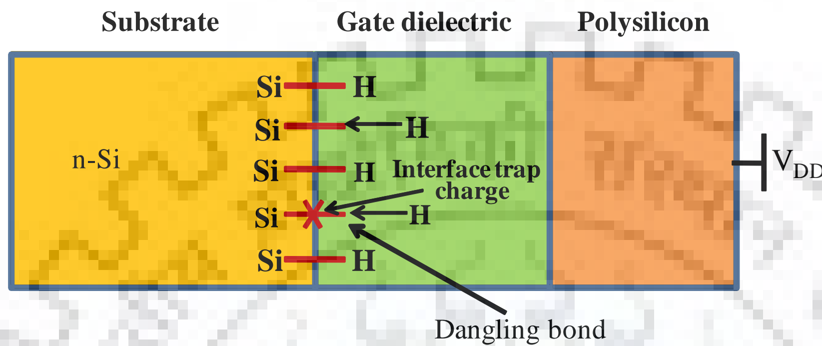


Figure 2.2 Prospective 2D view of silicon nanowire (NW) FET device during recovery.

2.3 Positive Bias Temperature Instability (PBTI) in nMOSFETs

Corresponding to the NBTI, occurs in pMOSFETS as discussed in section 2.2, a PBTI arises in nMOSFETs during positive gate voltage or inversion mode of operation. The impact of PBTI degradation was negligibly small in SiO_2 gate oxide technology but arises with similar even more worse order of degradation magnitude than NBTI in high-k technologies. In high-k stack technology, due to intermediate SiO_2 layer at the substrate insulator interface, PBTI degradation is occur at the certain distance away from the inversion channel. Thus, mainly impacting the threshold voltage with an almost negligible impact on the channel mobility [69]. Unlike NBTI in pMOSFETs in which degradation occur due to the Si/SiO_2 interface trap generation whereas PBTI degradation in nMOSFETis occurred due to charge trapping phenomenon in the high-k dielectric. Therefore, high-k CMOS processing technology especially the gate stack with its specific arrangement of the interface is a very confidential matter for the semiconductor companies. Due to the specific fabrication processing, differing PBTI threshold voltage degradation results are available. It is reported that the PBTI degradation increases as a function of time depending on the stress voltage and temperature [70], [71]. Recent results for HfO_2 based high-k gate dielectric associated with the major part of PBTI degradation is due to electron trapping at oxygen vacancies, preexisting dielectric and stress induced traps [72]. Further, some investigation tried to model the PBTI threshold voltage

degradation with reaction diffusion (RD) phenomenon from NBTI, but neglected the PBTI relaxation mechanism. Furthermore, it is reported that the PBTI recovery is equivalent to NBTI behavior, showing defects recovery occurs for a longerperiod of unstressed time. With high-k dielectric material, the PBTI is also prominent in future 3D device structure such as FinFETs and SiNW FETs due to device structure and high oxide field compared to planar FET.

2.4 The Experimental Signature of BTI and Modeling Approach

The multi-gate and 3D MOSFETs have drawn large attention for deeply scaled CMOS technology. The emerging devices including SOI, double gate MOSFETs, and devices especially below 22 nm are tri-gate bulk/SOI FinFET and silicon GAA nanowire (NW) FETs. Among these various multi-gate transistors, the silicon nanowire FETs (SiNW FET) devices are the most promising candidates for the highly scaled device down to the end of semiconductor roadmap, because of its extraordinary gate controllability and improved carrier transportation properties[9], [24], [73]. However, the bias temperature instability (BTI) reliability is an important issue, which needs to be comprehensively studied and include their effects before SiNW MOSFET goes into circuit applications. The extrapolation of bias temperature instability (BTI) reliability from existing planar MOSFETs to the advance scaled nano technology may lead to inaccurate device lifetime prediction. Since the scaling of device dimensions and the introduction of novel 3D structure, such as NW could vary the Si/SiO_2 interface degradation rate. The unique cylindrical device structure, quasi 1D channel and cylindrical gate of multiple crystallographic interface orientations can result in some special reliability behaviors. *Ru Huang et. al.* characterizedpSiNW FET devices for NBTI reliability and explored the new behavior of degradation with stress time [30]. It is experimentally observed that the initial V_{th} shift (if a device under stress) is very high and later on saturates in about 1000s. Unlike conventional planar MOSFETs in which the broken interface hydrogen (H) under the influence of applied gate bias diffuses in 1-D mode toward the gate, due to the cylindrical gate structure the initial degradation is fast and the broken H diffuses in 2-D mode.

In addition, due to the cylindrical structure of NW, the gate oxide electric field is higher compared to planar MOSFETs, consequently, increasing the rate of reaction at the interface. Moreover, the NBTI is susceptible to the temperature, therefore, high self-heating effects in NW results in even higher degradations due to the NBTI [74]. The elevated temperature near the interface causes large hydrogen diffusion and also leads to faster interface trap generation.

Apart from Si/SiO_2 interface traps, the oxide hole tunneling and trapping in SiNW FET gate oxide is also critical, which may further be increased by the strain in oxide [75] due to the process step called self-limiting oxidation for nanowire shaping. *Liu Change.et. al.* comprehensively investigated that the multiple crystallographic orientations of NW channel surface and gate trimming process induces additional trapping effects [76]. During recovery time or the positive stress voltage applied in p-SiNW FET, the oxide hole de-trapping and interface trap passivation can take place. Subsequently, the threshold voltage shifts toward its initial value. It is reported in the literature that the interface traps recovery due to NBTI is small compared to planar FET, whereas the oxide hole trap relaxation is highly sensitive to the recovery voltage [30].

2.5 Impact of BTI on Circuit Performance

Reliability issues in VLSI circuits have been a growing concern as semiconductor technologies enter into the advanced nanoscale era. NBTI reliability is the most critical issue that restricts the lifetime of device and circuit due to undesirable effects on the device threshold voltage. In 2003 *Anand T. Krishnan et al*. [77] reported for the very first time, the impact of NBTI on the planar device gate-drain capacitance (C_{GD}) degradation. The effects of C_{GD} degradation on circuit performance is measured for both digital and analog circuits. In the case of digital circuits, C_{GD} degradation due to NBTI leads to frequency degradation upto ~90 %. For analog circuit design, the degradation in the C_{gd} due to NBTI causes degradation in the unity current gain frequency response by upto ~70 % in a 2 stage operational amplifier with pMOS inputs. *Bipul C. Paul et al*. [78] proposed an analytical threshold voltage model to predict the delay degradation, which also includes mobility degradation model for a wide range of digital logic circuits such as inverter and ring oscillator, which depends on both worst case and switching activity dependent threshold voltage change due to NBTI. *Rakesh Vattikonda et al*. [79] observed that the circuit performance degradation due to NBTI can be efficiently mitigated by the following approach: (i) supply voltage (V_{DD}) and threshold voltage (V_{th}) tuning, (ii) PMOS transistor sizing, and (iii) duty cycle modulation. Further, *Sanjay V. Kumar et al*. [80] investigated the effect of NBTI on the SRAM cell read stability and proposed a data flipping method to recover the read SNM and the results are simulated on *Berkeley Predictive Technology Model (*BPTM) 70 nm and 100 nm technology node. Moreover, the bit cell flipping technique can recover upto 30 % of the read noise margin degradation caused due to NBTI. *Kunhyuk Kang et al.*[81] proposed an efficient reliability-aware circuit design technique. The

delay guard bending method has been employed to mitigate the NBTI effect. For memory arrays, the read stability in SRAM is mitigated by aggressive design technique such as stand by V_{dd} scaling and adaptive body biasing method.

Yangang Wang et al. [82] in 2008 explained the effect of NBTI on inverter and SRAM cell in 35 nm technology CMOS. The inverter delay degradation increases under the influence of NBTI and power dissipation decreases due to reduction in sub threshold drain current and switching current. For conventional 6T SRAM cell the read noise margin degraded linearly with the NBTI reliability. *R. Femaindezaet. al.* [83] experimentally characterized for NBTI effect on pMOSFETs transistor and CMOS inverters. The results shown are dependent on the following factors: (i) the impact of AC degradation is less than the DC degradation on the transistor performance thus improves the life time, (ii) AC NBTI is independent of frequency in the entire 1 Hz - 2 GHz range, (iii) the NBTI only effects the pMOSFETs or pull up transistor of the inverter and thus degrades the low to high propagation delay (t_{phl}). Further, for a deeply scaled device the reliability and variability are also the major show-stoppers for the circuit performance. *Harwinder Singh et al.* [84] have analyzed single SRAM cell reliability under the influence of NBTI, process and temperature variations in highly scaled CMOS technologies. It is reported that the high V_{th} devices degrade at the lower rate compared to low V_{th} device due to NBTI and degradation become more significant at a higher temperature. As a result, the high V_{th} SRAM memory chip introduces less number of faulty cells over the time as compared to the low V_{th} SRAM cell chip. However, the overall degradation in write margin improves over the time due to NBTI. *RasoulFaraji et al*. [85] have proposed a circuit based on adaptive body bias (ABB) technique to compensate for the aging effect due to BTI circuit performance. This ABB technique is utilized in SRAM cell and found that the static stability i.e. hold margin degradation reduces 6.85 %, read and write margins by 12.24 %, 2.16 %, respectively compared to traditional SRAM cell.

Changze Liu et. al. [76] proposed reaction diffusion (R-D) based SiNW FET NBTI threshold voltage model and investigated the impact on the digital and analog circuit performance. They analyzed the effect of NBTI on the basic logic gates such as basic inverter, inverter chain and 13 stages RO, and degradation is compared with the conventional planar MOSFETs based circuits. Further, the effects of NBTI on the 6T SRAM cell static (read/write margins) and dynamic (read/write access time) performance for 10 years of lifetime is estimated. *S.V Gupta et al*. [86] have considered the impact of NBTI on the access transistor of n-SOI FinFETs based

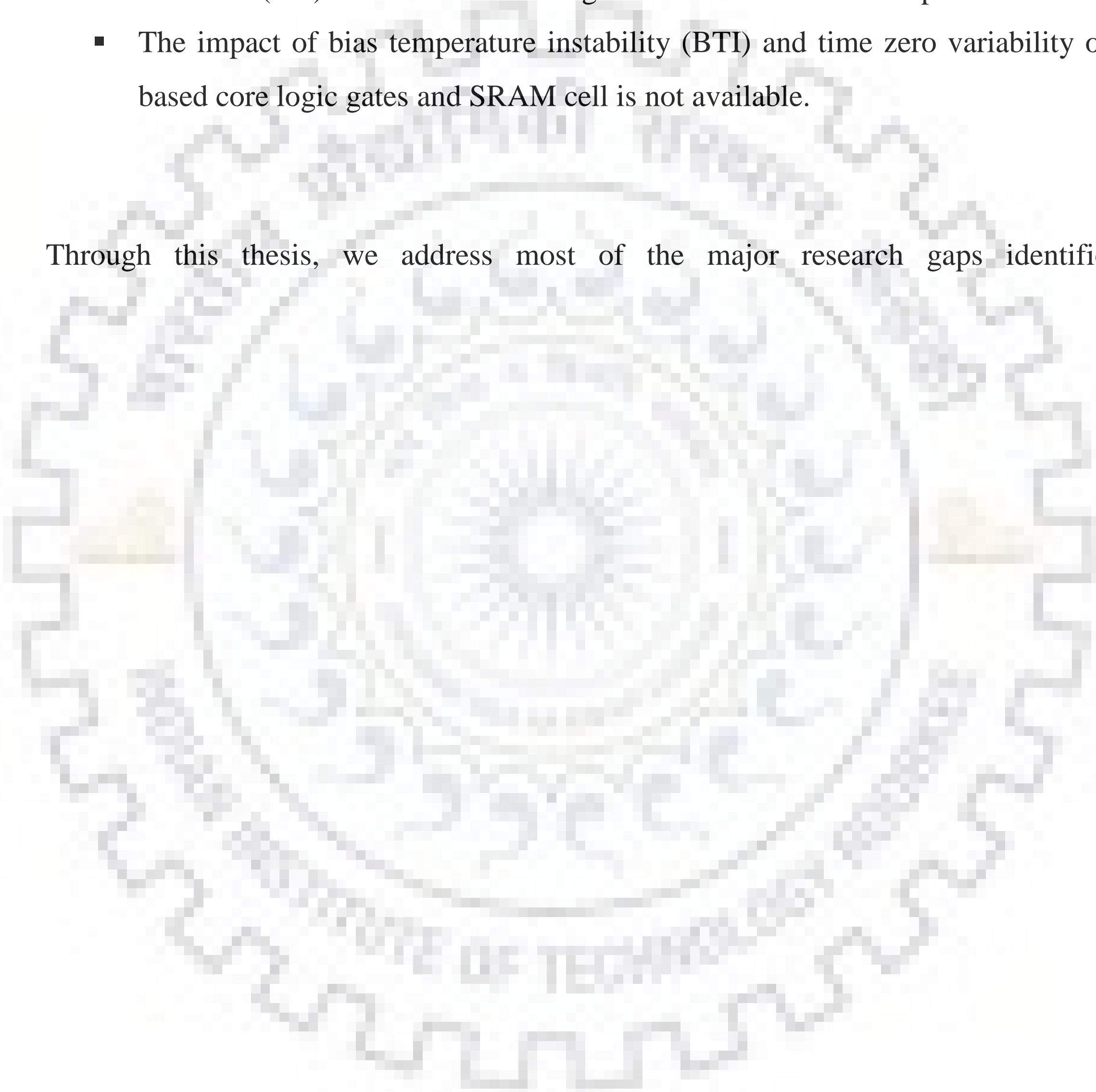
6T SRAM cell. Authors assumed that the access transistor in 6T SRAM cell experiences NBTI degradation during the hold state. Further, the combined impact of NBTI in the access and pull-up SOI FinFETs transistor of 6T SRAM cell has been investigated for the stability and performance and compared with the traditional method of assuming NBTI in only pull-up transistor of 6T SRAM cell. *Seyab Khan et al.* have presented the impact of BTI on basic and complex logic gates. At the transistor level, the impact of NBTI causes 2.30X higher degradation to PMOS transistor than PBTI causes to the NMOS transistors. It is also reported that the impact of NBTI is significant in NOR gate and PBTI brings higher degradation in NAND gates. With these extensive literature surveys, we found that the impact of BTI is only limited to planar MOSFETs and FinFET based circuits. Further, few studies are available to investigate the impact of NBTI on SiNW FET based circuits. Therefore, an accurate BTI predictive model is required to investigate the impact of BTI on SiNW FET based circuit. In this thesis, the complete NW BTI reliability circuit simulation framework has been developed. Finally, the impact of BTI on the NW core logic gates delay and 6T SRAM cell static/dynamic performance have been investigated.

2.6 Technical Gaps

Based on the extensive literature review the following technical gaps are identified which are investigated in this work.

- Modeling of (I-Vs) and (C-Vs) characteristics for long channel and short channel SiNW FET devices have been developed by many researchers [34], [35], [40], [87] for the circuit simulation. Moreover, for short channel SiNW FET devices the compact model including all the short channel effect such as drain induced barrier lowering (DIBL) velocity saturation, mobility degradation. However, for the deeply scaled NW device, geometrical parasitic capacitance and resistance are highly dominating. Therefore it is important & necessary to add the parasitics model in the physics based compact models to analyze the real circuit design performance. It is seen that parasitics induce an additional delay of 30% to50%, hence ignoring these in model can grossly underestimate circuit performance.
- Design and performance of SiNW FET based 6T SRAM and its comparison with the FinFETs or conventional planar technology is necessary for benchmarking and comparison, which is not reported in the literature.

- The threshold voltage and mobility degradation model due to bias temperature instability (BTI) for SiNW FET during stress and recovery time have not been developed. These accurate reliability prediction models are required and need to integrate into physics based Verilog-A compact models for reliability aware circuit design.
- The impact of BTI on the basic logic gates (Inverter, NAND, and NOR gates), ring oscillator (RO) and SRAM cell using NWFET have not been reported.
- The impact of bias temperature instability (BTI) and time zero variability on the NW based core logic gates and SRAM cell is not available.



Through this thesis, we address most of the major research gaps identified above.

भारतीय प्रौद्योगिकी संस्थान रुड़की
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3 CHAPTER

SiNW FET Compact Modeling

3.1 Introduction

In order to evaluate the capability of such 3D devices in the nanoscale regime, a compact model is required for performance analysis through device circuit simulations. In the last decade,a number of core models have been developed by various groups. *Jimenez et al.* proposed an analytic solution for the surface potential, drain current and charge-voltage for an intrinsic long channel transistor [34]. In [88], a long channel I-V model considering analytic charge model for surrounding gate (SG) MOSFETs is presented which is continuous for the entire operating region. *Yang Jieet al.* have proposed a model for long and short channel nanowire (NW) device and also included the impact of low to high doping concentration in the channel [40]. As the device dimensions are scaled parasitic capacitances and series source drain resistances play an increasingly vital role in determining circuit performance [89]. However, in the models reported earlier [41], the parasitic capacitance and resistance have not been included, which renders them inaccurate in predicting performance of real devices and circuits. In order to analyze performance of real/fabricated NW devices, and circuits a compact model is needed, which integrates the core channel model [4], [5], with parasitic resistance and capacitances [50], [9].

In this chapter, a compact model for long and short channel SiNW FET are developed, which include all short channel effects, velocity saturation, mobility degradation, and Quantum confinement effects. The model also includes scalable geometry dependent parasitic capacitance and resistance, which become a very dominating factor for nanoscale devices. The compact model is well calibrated with published experimental and TCAD simulations to ensure the accuracy of device and circuit results. The device model developed uses HSPICE through a Verilog-A interface for circuit simulation. It is seen that the developed compact model is very fast for device and circuit simulation as compared to 3D sentaurus TCAD simulation.

3.2 Core Model Descriptions

Figure 3.1 shows the schematic of lightly doped lateral SiNW FET in which current flow along the Y-direction. The basic formulation of the I-Vs and C-Vs models for long channel SiNW FET are as follows [48].

The electrostatic potential distribution in the silicon channel can be described by Poisson's equation

$$\frac{d^2\psi}{d\rho^2}+\frac{1}{\rho}\frac{d\psi}{d\rho}=\frac{q}{\varepsilon_{si}}(n_i e^{q\frac{(\psi-V)}{kT}}+N_a) \tag{3.1}$$

Where $\psi(\rho)$ is the channel potential, V is the quasi-Fermi potential, n_i is the intrinsic carrier density, q is the electronic charge, ε_{si} is the permittivity of silicon, and N_a is the channel doping concentration.

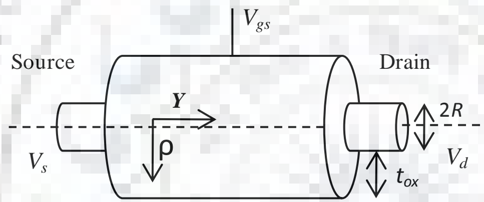


Figure 3.1 Schematic view of lateral SiNW FET.

The Equation (3.1) must satisfy the following boundary conditions:

$$\frac{d\psi}{d\rho}(\rho=0)=0\,,\ \psi(\rho=R)=\psi_s \tag{3.2}$$

Where ψ_s is the surface potential.

Equation (3.1) can be analytically solved with the above boundary condition. The first and second boundary condition can be applied by integrating (3.1). Finally the solution of the equation (3.1) is given as [88].

$$\psi(\rho)=V-\frac{2kT}{q}\ln\left[\frac{R}{2}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT(1-\alpha)}}\left(1-\frac{(1-\alpha)\rho^2}{R^2}\right)\right] \tag{3.3}$$

where α is to be determined by the boundary condition (3.2)

The total mobile charge per unit gate area is

$$Q_i = C_{ox}\left(V_g - V_{th,long} - \psi_s\right) \quad (3.4)$$

Applying gauss's law

$$Q_i = C_{ox}\left(V_g - V_{th,long} - \psi_s\right) = \varepsilon_{si}\frac{d\psi}{d\rho}_{\rho=R} \quad (3.5)$$

Applying equation (3.3) in equation (3.5), this finally converts into following implicit equation

$$\frac{1}{2}\ln\left(1-\alpha\right) - \ln\alpha + s\frac{1-\alpha}{\alpha} = q\frac{\left(V_g - V_{th,long} - V_{s/d}\right)}{2kT} - \ln\left(\frac{2}{R}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}\right) \quad (3.6)$$

here, $s = \varepsilon_{si}\ln(1+(t_{ox}/R))/\varepsilon_{ox}$, R is the radius of nanowire. The equation (3.6) is an implicit function of α and need to be solved for V=0, V=V_d at the source and drain side, respectively. Its solution is discussed in [90], the long channel threshold voltage is expressed as[40]

$$V_{th,long} = \Delta\phi + 2\phi_F + \frac{Q_{dep}}{C_{ox}} - \frac{kT}{q}\ln\left(\frac{2qN_a\varepsilon_{si}}{\frac{KT}{q}\left(C_{ox}\right)^2}\right) \quad (3.7)$$

where $\Delta\phi$ is the work function of gate electrode with respect to silicon, Q_{dep} is the depletion charge per unit gate area and ϕ_f and C_{ox} are the Fermi potential and effective gate capacitance, respectively.

From Gauss' law, the total mobile charge per unit gate area is

$$Q_i = 2\varepsilon_{si}\left(\frac{2kT}{q}\right)\frac{\left(1-\alpha\right)}{\alpha R} \quad (3.8)$$

The current equation is derived using Pao-sha integral can be written as [91].

$$I_{ds} = \mu\frac{2\pi R}{L}\int_{V_s}^{V_d} Q_i\left(V\right)dV = \mu\frac{2\pi R}{L}\int_{\alpha_s}^{\alpha_d} Q_i\left(\alpha\right)\frac{dV}{d\alpha}d\alpha = \mu\frac{8\pi\varepsilon_{si}}{L}\left(\frac{kT}{q}\right)^2\left[f\left(\alpha_d\right) - f\left(\alpha_s\right)\right]$$

(3.9)

Where

$$f\left(\alpha\right) = \left(-\frac{2}{\alpha} - \ln\alpha\right) + s\left(-\frac{1}{\alpha^2} + \frac{2}{\alpha}\right) \quad (3.10)$$

Where μ is the effective mobility, L denotes the channel length, V_d and V_s are the source, and drain voltages respectively, α_s and α_d are the solution of (3.6) relative for V=V_s and V=V_d

respectively. This model is able to produce the I-V characteristic of the long channel device as reported in [88], [40]. In order to calibrate the compact model for long channel silicon nanowire (SiNW) FET with TCAD device data, we have changed the mobility and threshold voltage dependent parameters in the core model. The mobility and work function are tuned to match the I_{ON} and threshold voltage of the device respectively. Fig. 3.2 shows the comparison of the resulting transfer and output characteristic of a long channel SiNW FET between model and TCAD.

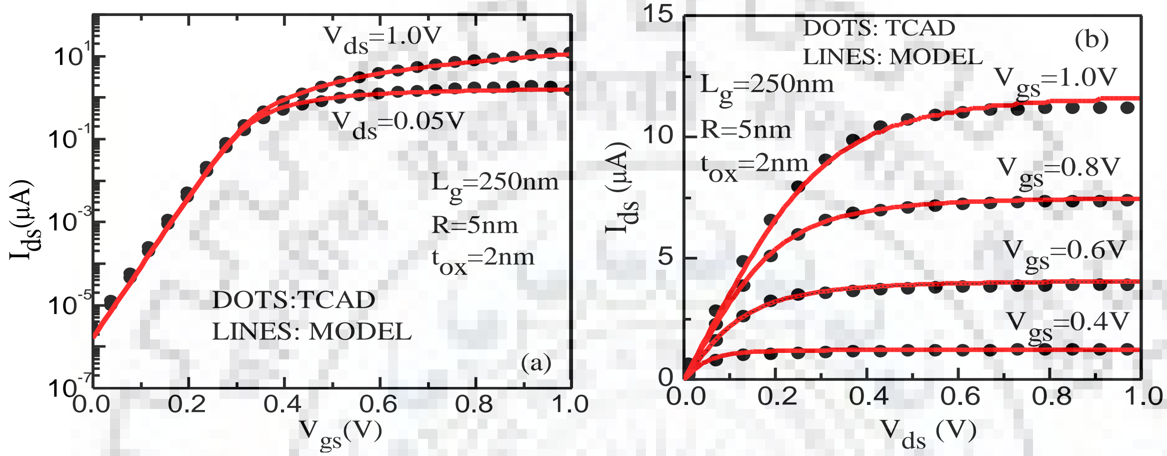


Figure 3.2 Shows the comparison of nSiNW FET device characteristic between model and TCAD (a) I_d-V_g, (b) I_d-V_d.

A. Terminal charges and intrinsic capacitances of SiNW FET

Analytical expressions for terminal charges are required for transient circuit simulation. The quantities Q_g, Q_s, and Q_d are the gate, source and drain terminal charges of SiNW FET respectively and are expressed as [88]:

$$Q_g = 8\pi\varepsilon_{si} L \frac{kT}{q} \frac{g(\alpha_d) - g(\alpha_s)}{f(\alpha_d) - f(\alpha_s)} \tag{3.11}$$

$$Q_d = 8\pi\varepsilon_{si} L \frac{kT}{q} W_{sd} \tag{3.12}$$

$$Q_s = 8\pi\varepsilon_{si} L \frac{kT}{q} W_{ds} \tag{3.13}$$

where W_{sd}, W_{ds} are function of $g(\alpha)$ as given by [88].

The main intrinsic capacitances which are necessary for the circuit simulation are analytically expressed below [88],

$$C_{gg} = C_{gs} + C_{gd} \tag{3.14}$$

$$C_{gs} = 8\pi\varepsilon_{si} L \frac{(1-\alpha_s)\left[\frac{1-\alpha_s}{\alpha_s} + W_{sd} + W_{ds}\right]}{\alpha_s\left(f(\alpha_d) - f(\alpha_s)\right)} \tag{3.15}$$

$$C_{gd} = 8\pi\varepsilon_{si} L \frac{(1-\alpha_d)\left[\frac{1-\alpha_d}{\alpha_d} + W_{sd} + W_{ds}\right]}{\alpha_d\left(f(\alpha_s) - f(\alpha_d)\right)} \tag{3.16}$$

$$C_{dg} = 8\pi\varepsilon_{si} L \left\{ \frac{(1-\alpha_d)\left[\frac{(1-\alpha_d)}{\alpha_d} + W_{sd} + W_{ds}\right]}{\alpha_d\left(f(\alpha_s) - f(\alpha_d)\right)} + \left(W_{ds} - W_{sd}\right)\frac{\frac{1}{\alpha_s} - \frac{1}{\alpha_d}}{\left(f(\alpha_s) - f(\alpha_d)\right)} \right\} \tag{3.17}$$

$$C_{sd} = 8\pi\varepsilon_{si} L \frac{(1-\alpha_d)\left[W_{ds} - W_{sd}\right]}{\alpha_d\left(f(\alpha_d) - f(\alpha_s)\right)} \tag{3.18}$$

Excellent agreement is observed in Figure 3.3 between capacitance model and TCAD simulation for long channel (L_g=250 *nm*) SiNW FET device. The modeled capacitances C_{gg}, C_{gs}, C_{sg}, C_{dg} (Figure 3.3(a)) for nSiNW, as a function of gate voltage for drain-source voltage 1.0 V shows a smooth transition for different operating regimes. Figure 3.3(b) shows the accuracy of intrinsic capacitance's model C_{gg}, C_{gs}, C_{gd} for pSiNW FET as a function of gate-source voltage at the drain voltage −1.0 V.

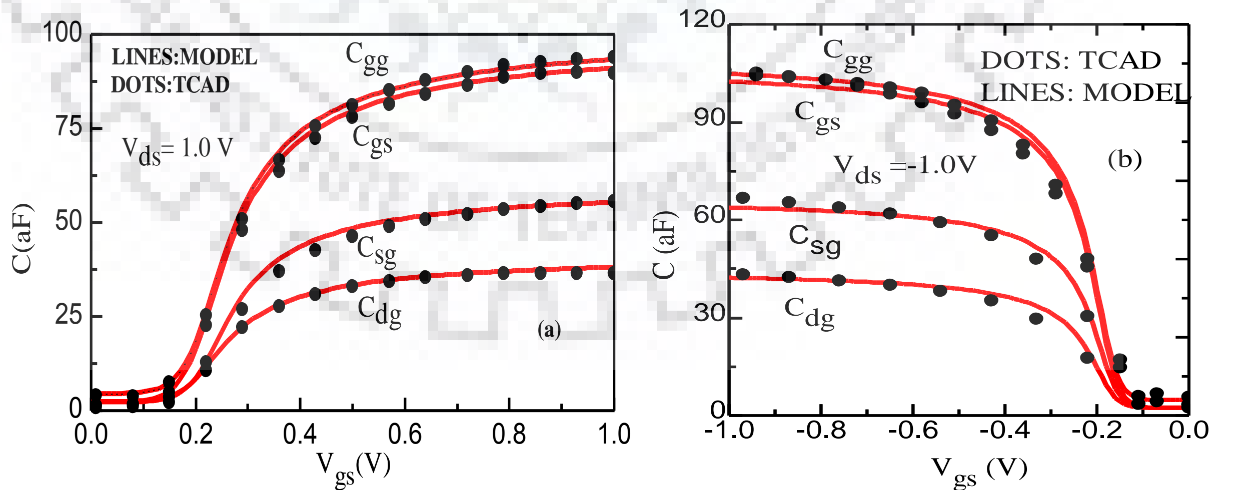


Figure 3.3 (a-b) Capacitance voltage comparison of a n/p-SiNW FET as a function of V_{gs} at V_{ds} =0V obtained from model and TCAD results.

3.3 Advance Physical Effects for Short Channel Devices

For short channel devices, the voltage at drain terminal affects the channel potential or potential barrier which is known as short channel effect (SCE). The SCE induces threshold voltage roll-off, drain induced barrier lowering (DIBL) [92], sub threshold slope (SS). The quantum mechanical (QM) confinement of the carriers is also significant in scaled diameter devices. The SCE and quantum mechanical effect are modeled using [40], while mobility degradation is modeled using [93], and velocity saturation effects are modeled using [41].

The modified implicit equation for short channel devices similar to (3.6) is expressed as

$$\frac{1}{2}\ln(1-\alpha)-\ln\alpha+s\frac{1-\alpha}{\alpha_{SCE}\alpha}=\frac{q\left(V_g-\Delta\phi_{new}\right)}{2kT\alpha_{SCE}}-\frac{qV}{2kT}-\ln\left(\frac{2}{R}\sqrt{\frac{2\varepsilon_{si}kT}{q^2n_i}}\right) \tag{3.19}$$

where

$$\alpha_{SCE}=1+2f_{SCE} \tag{3.20}$$

$$f_{SCE}=\frac{1}{\left[2\cosh\left(\frac{L/2}{\lambda}\right)-2\right]} \tag{3.21}$$

is a SCE factor.

Where $\lambda=\sqrt{t_{oxeff}\left(\frac{R}{2}\right)\left(\frac{\varepsilon_{si}}{\varepsilon_{ox}}\right)+\left(\frac{1}{4}\right)R^2}$ is the natural length of SiNWFET.

$$t_{oxeff}=t_{ox}+\Delta t_{ox} \tag{3 .22}$$

t_{ox} is the oxide thickness and Δt_{ox} is the change in oxide thickness due to the short channel and quantum mechanical effects (QMEs) [40]. The deviation of the location of the peak carrier concentration from the SiO2/Si surface decreases the channel carrier concentration and leads to a decrease in the gate capacitance. In a model, the charge centroid effect is included by the modification in the oxide capacitance as given below [40]

The average inversion charge is given as

$$Q_{iavg}=\frac{Q_{is}+Q_{id}}{2} \tag{3.23}$$

$$E_{avg} = C_{ox} \frac{\left(Q_{dep} + \frac{Q_{iavg}}{3} \right)}{\beta \varepsilon_{si}} \tag{3.24}$$

$$\Delta t_{ox} = a \left(\frac{h^2}{2qm_e E_{avg}} \right)^{\frac{1}{3}} \tag{3.25}$$

$$C_{oxeff} = \varepsilon_{ox} \left[\left(R - \frac{\Delta t_{ox}}{3} \right) \ln \left(\frac{R + t_{ox}}{R - \frac{\Delta t_{ox}}{3}} \right) \right]^{-1} \tag{3.26}$$

Where, m_e is effective mass of electron in lowest electronic sub-band, E_{avg} is average surface field, Q_{is} and Q_{id} are the inversion charge at source and drain side respectively. Other than the electrical confinement (EC), there is strong carrier confinement in nanoscale nanowire even at low electric fields in the channel. It is because the carriers are confined in a rectangular well that is formed by the gate insulator around, which is known as structural confinement (SC). In SC and EC, the conduction band splits into several sub-bands. Since the carriers stay at the sub-band with the lower energy first, the reduction of the amount of carriers can be modeled by widening the effective bandgap.

The modified current equation after the inclusion of SCE is

$$I_{ds} = \mu \frac{8\pi\varepsilon_{si}}{L} \left(\frac{kT}{q} \right)^2 \left[f(\alpha_d) - f(\alpha_s) \right] \tag{3.27}$$

Where $f(\alpha) = \left(\frac{-2}{\alpha} - \ln \alpha \right) + s \left(\frac{-1}{\alpha^2 \alpha_{SCE}} + \frac{2}{\alpha \alpha_{SCE}} \right)$

change in threshold voltage due to SCE is given as [40],

$$\Delta V_{th,SCE} = f_{SCE} \left[2\left(V_{th,long} - Q_{dep} - V_{bi} \right) - V_{ds} \right] \tag{3.28}$$

$$V_{th,short} = \Delta\phi_{new} = V_{th,long} + \Delta V_{th,SCE} \tag{3.29}$$

The threshold voltage of a long channel device is independent of the channel length and the drain voltage. However, as the channel length becomes shorter, the threshold voltage shows a higher dependence on the channel length and the drain voltage. f_{SCE} is the parameter which is takes care of channel length modulation (CLM).

3.3.1 Mobility Degradation

Carrier mobility degradation in the SiNW FET mainly occurs due to following four scattering mechanisms: Coulomb scattering, acoustic phonon scattering, surface roughness scattering, and optical phonon scattering. The first three scattering mechanisms have transverse field dependence and depend upon the FET region of operation. Columbic scattering is dependent upon the weak-inversion region of operation, acoustic phonon scattering at mid-inversion and surface scattering at strong inversion region. All these scattering mechanisms in SiNW FET are very strongly dependent on the low– field electron mobility on the silicon body diameter as well as on the effective field. The last optical phonon scattering is the most dominating scattering at a high lateral field (i.e., at high drain biases and short channel). This high field scattering causes the velocity of the carrier to saturate and it will be discussed in the next section via current saturation submodel. While modeling the long channel, we consider the constant mobility model which actually is not true. This is because of the vertical electric field, which will attract the carrier towards the surface and accounts for surface scattering thus decreasing the mobility. Thus, we need to model the mobility dependence on the gate-source voltage. They are modeled through a submodel called "low-field mobility degradation" and used to get effectivemobility [41] [94].

3.3.2 Velocity Saturation and Drain Saturation Voltage

At high lateral electric field along the channel (e.g. at high drain biases and short channel), optical photon scattering is the dominant mechanism since electron is able to gain enough energy to emit optical photons. This high field scattering induces the velocity of the carriers to saturate and degrades the drain to source current directly. This velocity saturation effect can be model via a submodel called current saturation [41], [94].

Saturation channel E-field is given as

$$Esat1 = 2VSAT1\left(\frac{DMOB2}{ueff}\right) \tag{3.30}$$

Where VSAT1 is the saturation velocity and DMOB2 is the mobility degradation factor.

Velocity saturation factor in the linear region is modeled as

$$DVSAT = \frac{1+\left(delvsat+\left(\frac{delqi}{Esat1\times L}\right)^{EXSAT}\right)^{\frac{1}{EXSAT}}}{1+\left(delvsat\right)^{\frac{1}{EXSAT}}} \tag{3. 31}$$

Where delvsat is velocity saturation parameter in the linear region, EXSAT is the field exponent for velocity saturation and delqi is the average inversion charge.

$$I_{ds} = \frac{I_{ds}}{DVSAT} \tag{3. 32}$$

Drain saturation voltage can be modeled as

$$V_{dsat} = \frac{Esat\times L\times KSAT\left(V_{gsteff}+2V_T\right)}{Esat\times L\times KSAT+V_{gsteff}+2V_T} \tag{3. 33}$$

$$V_{gsteff} = 2V_T \log\left(1+\exp\left(\frac{V_{gs}-V_{th}}{2V_T}\right)\right) \tag{3. 34}$$

$$V_{dseff} = \frac{V_{ds}}{\left(1+\left(\frac{V_{ds}}{V_{dsat}}\right)^{MSAT}\right)^{1/MSAT}} \tag{3. 35}$$

Where V_T is the thermal voltage and V_{th} is the threshold voltage. *KSAT and MSAT* are the fitting parametersused at high and low drain voltage respectively.

3.4 Geometry Dependent Parasitic Capacitance Model

As the channel length is scaled down to nanometer range parasitic becomes dominant factor, which cannot be neglected in circuit simulation [95]. The 2-D cross-sectional view of SiNW FET and parasitic capacitance components are shown in Figure 3.4. Its components are divided into four parts: 1) outer fringing capacitance $C_{of\text{-}gsd/gex}$, 2) the inner fringing capacitance C_{if}, 3) overlap capacitance C_{ov}, and 4) sidewall capacitance C_{side}. The physical capacitance models for these components are given below [49].

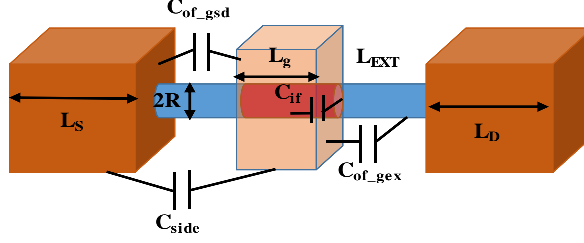


Figure 3.4 3D schematic view of SINW FET with parasitic capacitance. The parasitic components are divided into four parts C_{side}, C_{of}, and C_{if}, where C_{of} is further divided into C_{ofgsd} and $C_{of\text{-}gex}$.

I) *Sidewall Capacitance: C_{side}*

The sidewall capacitance is as follows,

$$C_{side} = \frac{4\varepsilon_{ox}(H_g - \eta W_g)}{\pi} \ln\left(\frac{b}{a}\right) \tag{3. 36}$$

$$\frac{b}{a} = \frac{2\sqrt{L_{S/d}L(L_{S/d}+L_{EXT})(L+L_{EXT})} + 2L_{S/d}L}{L_{EXT}(L+L_{S/d}+L_{EXT})} + 1 \tag{3.37}$$

where n is the number of channels in parallel for multiwireSiNW FET, H_g and W_g are the height and width of a metal gate, L_{EXT} and $L_{s/d}$ are the extension and source drain pad length, respectively.

II) *Outer Fringe Capacitance: C_{of}*

The outer fringe capacitance (C_{of}) consist of the capacitance between gate to source/drain ($C_{of\text{-}gsd}$) and gate to source/drain extension region ($C_{of\text{-}gex}$) gate as shown in Figure 3.4. This capacitance varies with the extension length and can be expressed as

(a) For a long extension region in SiNW FET

$$L_{EXT} \geq \sqrt{H_g^2 + W_g^2}$$

$$C_{of} = C_{of-gex} = \frac{8}{\pi}\varepsilon_{ox}\eta\left[\left(H_g - R - t_{ox}\right)\left(2\frac{W_g}{H_g} + 1 - \frac{H_g}{\sqrt{H_g^2 + W_g^2}}\right)\right] + \frac{8}{\pi}\varepsilon_{ox}\eta\left[\left(W_g - R - t_{ox}\right)\left(2\frac{H_g}{W_g} + 1 - \frac{W_g}{\sqrt{H_g^2 + W_g^2}}\right)\right] \tag{3.38}$$

where R is the radius of SiNW FET.

(b)When the extension regions is small

$$L_{EXT} \le \sqrt{H_g^2 + W_g^2}$$

$$C_{of} = C_{of-gsd} + C_{of-gex}$$

$$C_{of-gsd} = \varepsilon_{ox} \frac{(4H_g W_g - \pi (R - t_{ox})^2)}{L_{EXT}} \tag{3.39}$$

$$C_{of-gex} = 4\varepsilon_{ox} \left(L_{EXT} - t_{ox} + R \ln\left(\frac{L_{EXT}}{t_{ox}} \right) \right) \times \sqrt{\frac{2R}{L_{EXT} + 2R + t_{ox}}} \tag{3.40}$$

III) *Inner fringe capacitance:* C_{if}

$$C_{if} = 4\varepsilon_{si} (R + t_{ox}) \ln\left(\frac{2t_{ox} + R}{2t_{ox}} \right) \tag{3.41}$$

3.5 Geometry Dependent Parasitic Resistance Model

Parasitic series resistance became an important issue due to narrow width extension region, which plays a critical role in SiNW FET based device and circuit performance[96]. Here we have added the TCAD calibrated geometry dependant parasitic resistance models as reported in [50] to the core model. The parasitic series resistance is divided into spreading resistance *(R_{SP})*, extension resistance *(R_{EXT})*, interface resistance *(R_{INT})*, deep source/drain resistance *(R_{DP})* and contact resistance *(R_{CO})* as shown in Figure 3.5. Spreading, contact and extension resistance are the most dominating resistances in nanoscale regions, which are expressed as

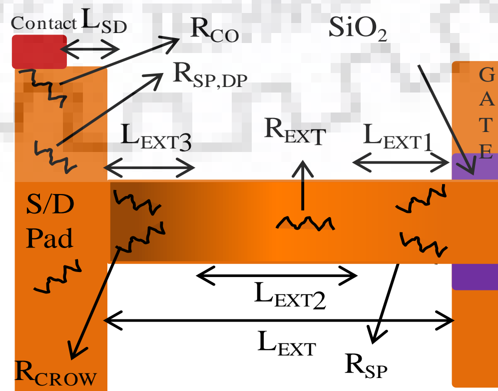


Figure 3.5 2D cross section view of SiNW FET device showing equivalent resistance network to calculate the total resistance.

(a) Spreading Resistance: R_{sp}

The spreading resistance of SiNWcan be expressed as [7]

$$R_{sp} = \int_{L_{EXT}-L_{EXT1}}^{L_{EXT}} \frac{\rho_{EXT1}(y)dy}{W_{EFF}\left[(L_{EXT}-y)\tan\alpha + T_C\right]} \quad (3.42)$$

where W_{EFF} is circumference of wire, α spreading angle at which current diverges, T_C is accumulation layer thickness, and ρ_{EXT1} is the resistivity in extension regions.

(b) Source/drain extension resistance: R_{EXT} is given by

$$R_{EXT} = \frac{\rho_{EXT2} L_{EXT2}}{A} \quad (3.43)$$

where A is the area of nanowire.

(c) Contact resistance: R_{CON}

The contact resistance of SiNW FET can be expressed as [7]

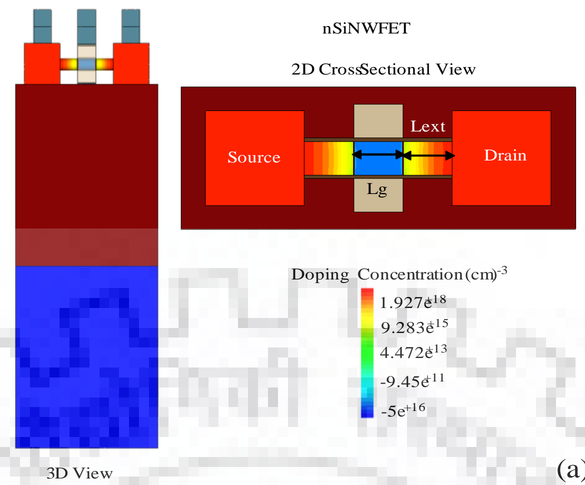
$$R_{CON} = \frac{\rho_c}{l_T W} \coth\frac{l_c}{l_T} \quad (3.44)$$

where $l_T = \sqrt{\frac{\rho_c}{\rho_{HDD}}}$, l_c and W is the length and width of the contact window, ρ_c and ρ_{HDD} are the contact and highly doped drain (HDD) resistivity respectively. The extension length *(L_{EXT})* is divided into L_{EXT1}, L_{EXT2} and L_{EXT3} as shown in Figure 3.5 and it has varying conductance along the extension because the doping concentration difference from source/drain to channel is the range of 2x10^{20} cm^{-3}to 5x10^{15} cm^{-3}. These well calibrated models are included in our core model for device and circuit simulation.

3.6 Asymetric SiNW FET Device

The device asymmetry employs the different source/drain extension length. The I_{ON} can be increased or decreased by changing the length of extension region of SiNW FET device. Larger the extension region, lesser the current due to higher extension resistance vice-versus. Therefore, our compact model is able to predict any kind of asymmetrical extension length by geometrical parasitic capacitance and resistance model. Although, we have not done any device asymmetry analysis but in the future, this model can be used to analyze the impact of asymmetricity on the device performance and propose new circuit design guidelines.

3.7 TCAD SETUP and SiNW FET Device Structure



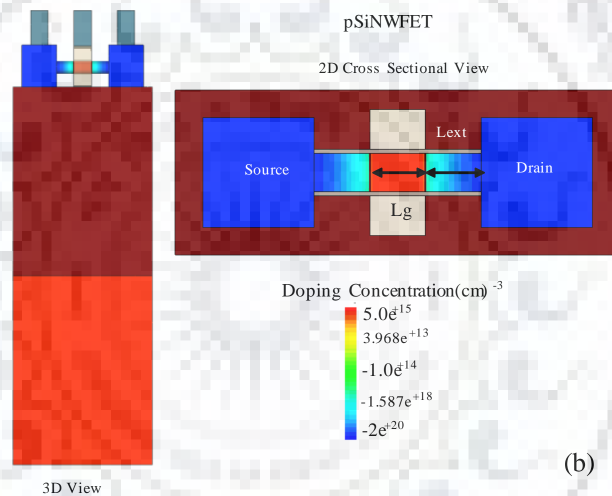


Figure 3.6 (a-b) shows the 3D and 2D cross sectional view of n/p SiNW FET respectively.

A simplified 3D and 2D view of TCAD silicon nanowire FET device structure are shown in Fig. 3.6. The 2D crossection view show the doping concentration along the channel for both n and p SiNW FET. In this section, we further explain about the important models used in the TCAD device simulation.

Transport model:

The density gradient quantization model is used which is most suitable model to calculate the quantization effects such as shift of the threshold voltage, carrier concentration, reduction of gate capacitance due to shift of the carrier distribution from the silicon-oxide interface [97].

Bandgap Narrowing:

At high impurity concentration, the density of energy states depends on the impurity of concentration, no longer has a parabolic distribution. The reduced bandgap is due to the formation of band tails and the broadening of the impurity band on the edge of valance and conduction band. The effective band gap (E_{geff}) results from the band gap reduced by band gap narrowing (E_{bgn}) can be written as

$$E_{geff}(T) = E_g(T) - E_{bng} \tag{3.45}$$

Where $E_g(T)$ is the band gap energy at temperature T can be written as

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} \tag{3.46}$$

Where $E_g(0)$ is the band gap energy at 0K, and α and β are the material dependent parameter.

E_{bgn} is the bandgap narrowing is given by

$$E_{bgn} = \Delta E_g^{\circ} + \Delta E_g^{Fermi} \tag{3.47}$$

Where ΔE_g^{Fermi} is an optional correction and ΔE_g° is determined by the bandgap narrowing slotboom model [98]

Mobility Model:

Different mobility models such as temperature dependent, doping dependent, field saturation dependent, carrier-carrier scattering dependent have been reported to estimate the device performance. For more than one mobility model, the mobility can be combined for different bulk (μb1, μb2, …) and surface (μs1, μs2, …) mobility contributions following the Mathiessen"s rule as

$$\frac{1}{\mu} = \frac{1}{\mu_{b1}} + \frac{1}{\mu_{b1}} + \ldots\ldots\ldots + \frac{1}{\mu_{b1}} + \frac{1}{\mu_{b1}} + \ldots. \tag{3.48}$$

In the simplest case, the mobility is a function of the lattice temperature. Hence, by default the constant mobility model is used in the device simulation to accounts for phonon scattering depending on the lattice temperature as

$$\mu_{cons} = \mu_L \left(\frac{T}{300K}\right)^{-\zeta} \tag{3.49}$$

Where μ_L is the mobility due to phonon scattering.

In addition to temperature dependent, to account for the mobility degradation due to impurity scattering and carrier-carrier scattering the Philips unified model [99] is used. High field saturation model encapsulates three submodels: the low-field mobility model, the velocity saturation model, and the driving force model. Starting from the Caughey-Thomas model, the Canali model proposed [97] the high field mobility as

$$\mu(f) = \frac{(1+\alpha)\mu_{low}}{\alpha + \left[1 + \left[\frac{(1+\alpha)F_{hfs}\mu_{low}}{v_{sat}}\right]^{\beta}\right]^{1/\beta}} \tag{3.50}$$

Where μ_{low} is the low-field mobility calculated by Mathiessen"s rule, β is exponentially dependent on temperature expressed as $\beta=\beta_0(T/300K)^{\beta exp}$, v_{sat} and F_{hfs} are saturation velocity and driving force electric field, calculated using

$$v_{sat} = v_{sat,0}\left(\frac{300K}{T}\right) v_{sat,exp} \ , F_{hfs} = |\nabla \phi_{n/p}| \tag{3.51}$$

Low-field ballistic mobility model is adopted to include quasiballistic effects. The electric field normal to the closest semiconductor-insulator interface is used in mobility model using the "Enormal" model.

Generation-Recombination:

Generation-recombination process exchange carriers between the conduction band and valance band. Recombination rate through deep defect in the band gap is obtained by Shockley-Read-Hall (SRH) model

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n+n_1) + \tau_n(p+p_1)} \tag{3.52}$$

with $n_1=n_{i,eff}\exp(\frac{E_{Trap}}{kT})$, $p_1=n_{i,eff}\exp(-\frac{E_{Trap}}{kT})$, n and p are electron and hole concentrations, $n_{i,eff}$ is the effective intrinsic concentration, E_{trap} is the difference

between the defect level and intrinsic level with a default value of zero. The minority carrier life time τ_n and τ_p models consider the effects of doping, electric field, and temperature. The doping dependence of the SRH lifetime is modeled with the Scharfetter relation [97].

3.8 Calibration of Compact Model with TCAD and Fabricated Data

3.8.1 Single wire TCAD calibration

In order to validate the compact model, we have calibrated it with sentaurus TCAD and published experimental device data. The device calibration is divided into three parts, threshold voltage (V_T), transition regions (from linear to saturation), and I_{on} region matching. The threshold voltage matching has been done by modifying the work function (wf) of metal and transition region matching by modifying the short channel f_{SCE} parameter in expression (3.20) and mobility parameter for current.

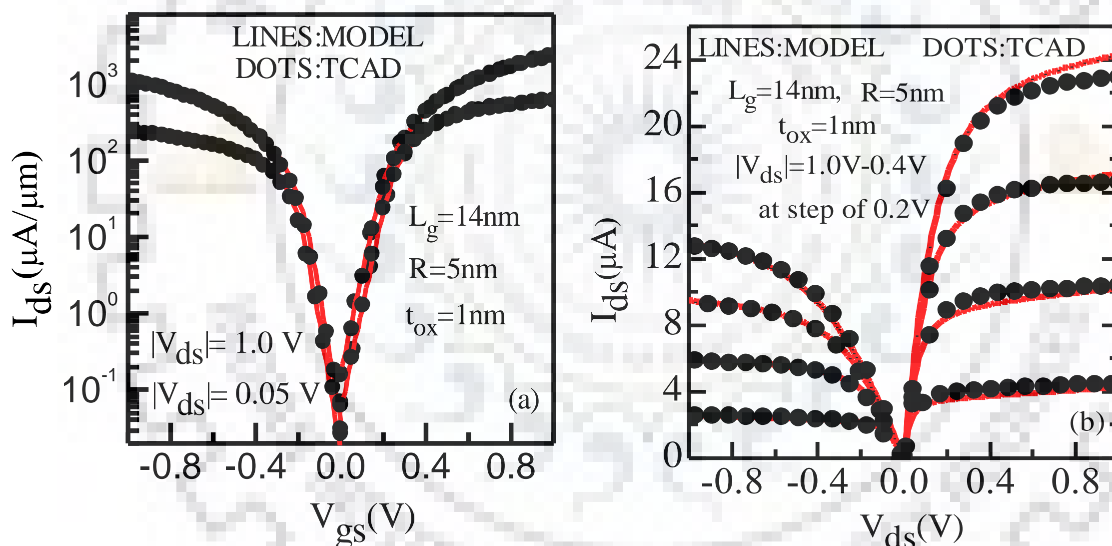


Figure 3.7 Comparison of (a) I_d-V_g,(b) I_d-$V_d$characteristics of a n/p SiNW FET between model prediction and TCAD

Moreover, MEXP and KSAT are the very sensitive parameters at low and high drain voltage in the saturation region respectively. These velocity saturation model parameters such as MEXP has a minimum value of 2.0 for circuit convergence and KSAT value is lies between 0.1 to 2. Figure 3.7 shows the excellent I_d-V_g and I_d-V_d matching of 10 nm single wire nSiNW and pSiNWFET devices between model and TCAD simulation data. Further, Figure 3.8 illustrates the excellent agreements of experimentaldevicecharactrestics (I-V) of the short channel length (L_g=30 nm) data [23], to our compact model.

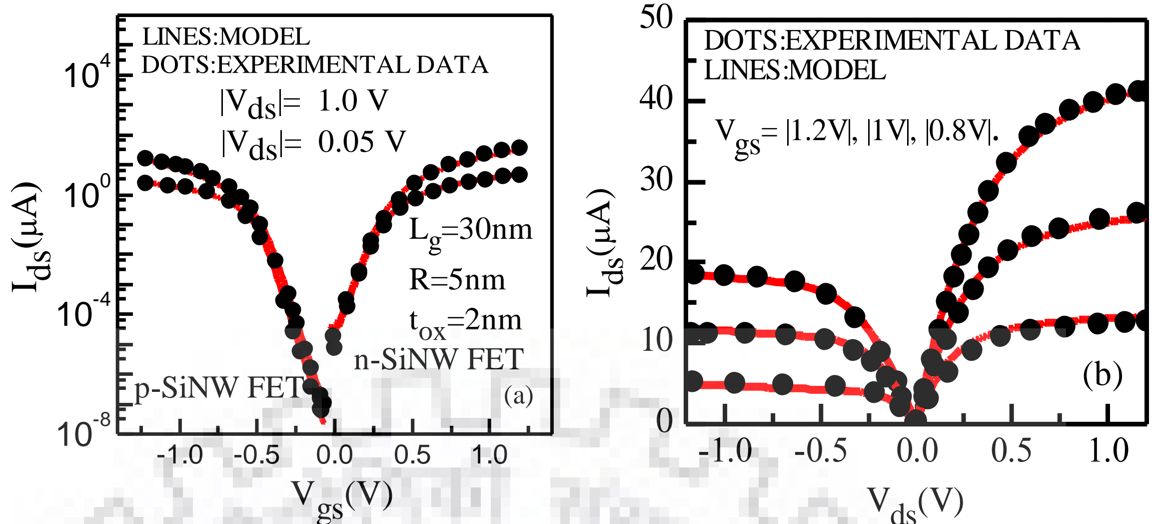


Figure 3.8 Comparison of fabricated data with model (a) shows the good agreement of I_d-V_g with different V_d, (b) I_d-V_d for different V_g.

3.8.2 Multi Wire I-V and C-V Calibration

Unlike MOSFET in which the drive strength of the device can be increase by increasing the width of transistors, but in the case of SiNW FET, it would be different. The drive strength of SiNW FET can be tuned by three geometrical parameters: diameter, extension length and number of wires in parallel. To change the diameter and extension length of each device become a fabrication issue and complexity as compared to increase in the number of wires in parallel for drive strength. In our work, the multiwire sizing technique is utilized for nanowire circuit design. Therefore, the developed compact model is also calibrated with the single and multiwire NW devices. Figure 3.9 shows the calibration of two and three wires nSiNW FET TCAD simulated I_d-V_g data with the model. It shows the current strength for SiNW increases more than the twice and thrice for 2 and 3 wire SiNW FET as compared to single wire. This is attributed to an important parameter for the high performance circuit design.

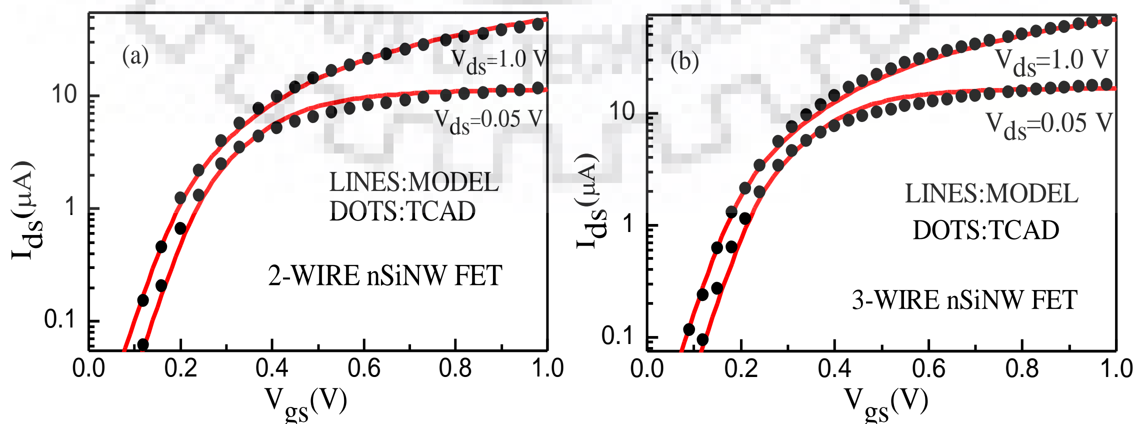


Figure 3. 9 Matching of model with TCAD for 2 and 3 wire SiNW (a) I_d-V_g for 2 wire, (b) I_d-V_g for 3 wire of channel SiNW FET.

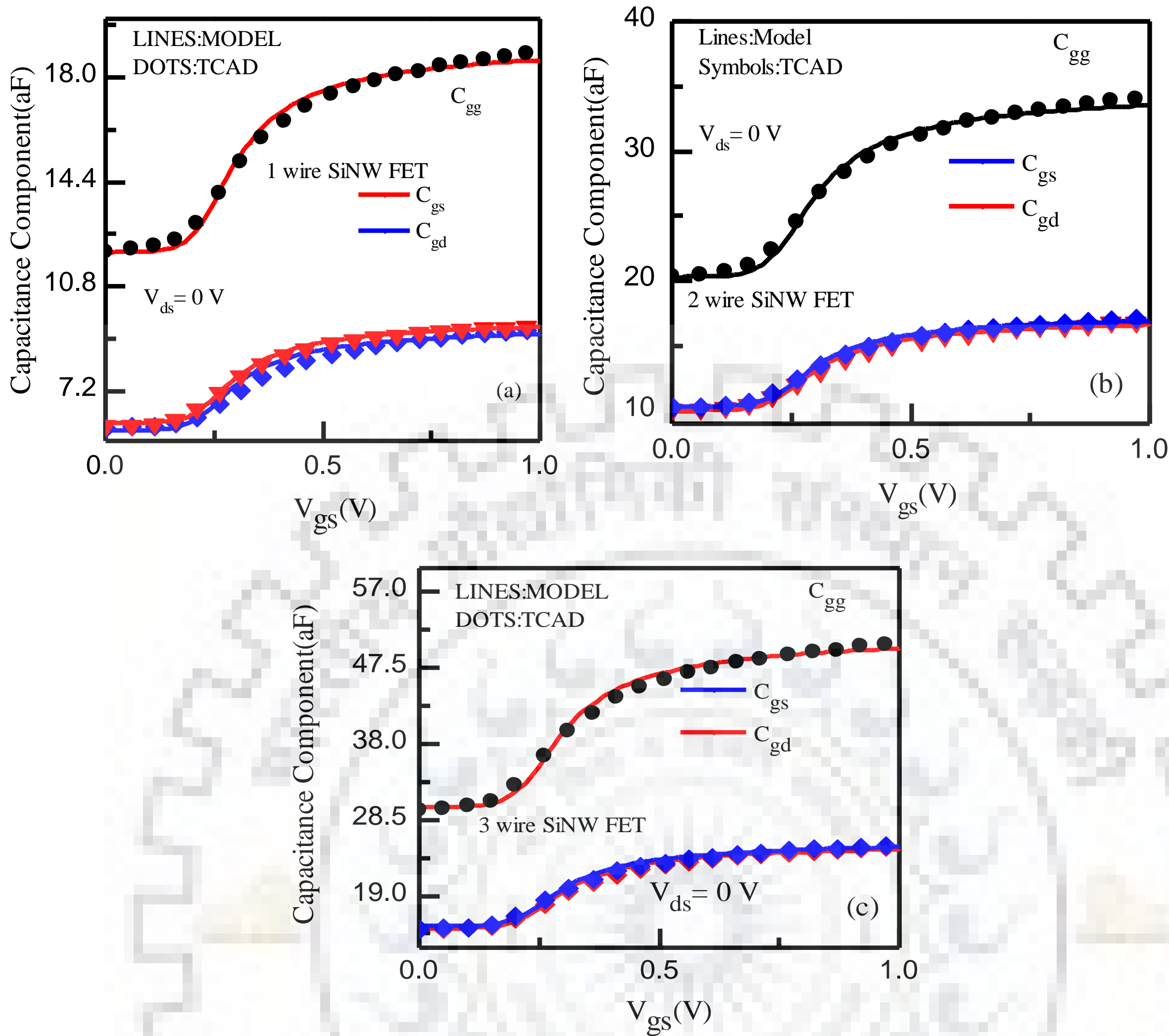


Figure 3. 10 Capacitance components of nSiNW FET as a function of V_{gs} at V_{ds}= 0 V obtain from model in comparison with TCAD (a) 1wire, (b) 2 wire, and (c) 3 wire capacitance.

The compact developed model applies equally-well and accurate to pSiNW FET for single and multiple wire devices. Figure 3.10 (a-c) shows the comparison of model and TCAD of the multiwire capacitance component, e.g. intrinsic capacitance and geometrical dependence parasitic capacitance as a function of V_{gs} at V_{ds}=0 V. These excellent matching of I-Vs & C-Vs of multiwire TCAD data show the validity of our model. The high accuracy of the model with TCAD and experimental data shows the accuracy of circuit simulation.

3.9 Implementation of Model for Circuit Simulation

The developed compact model which is well calibrated with TCAD and fabricated devices is employed in the nanowire circuit simulation. Figure 3.11 (a) shows the schematic diagram of SiNW FET inverter. The static voltage transfer characteristic (VTC) of the SiNW FET inverter is shown in Figure 3.11(b).

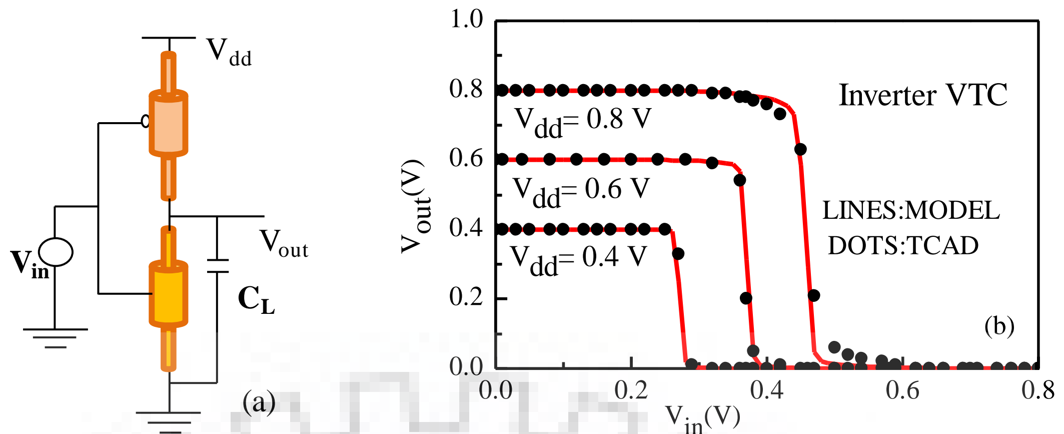


Figure 3.11 (a) Schematic of SiNW FET inverter, (b) Inverter VTC matched with TCAD for different V_{dd}.

The VTC of inverter shows the good agreement between compact model and TCAD (obtained by mixed mode simulation) simulation for different range of supply voltages (from 0.8 V to 0.4 V).

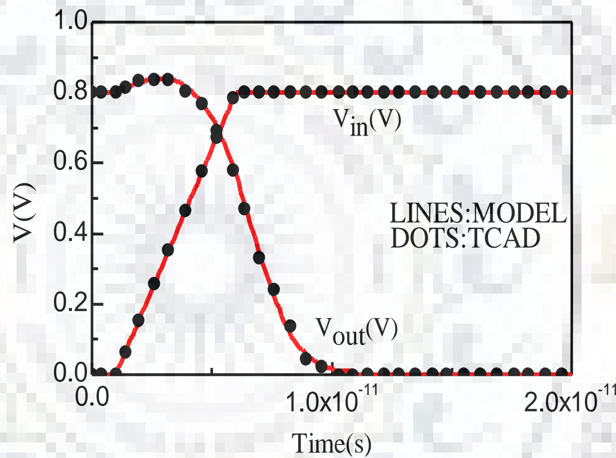


Figure 3.12 Transient characteristic of inverter matched to TCAD result.

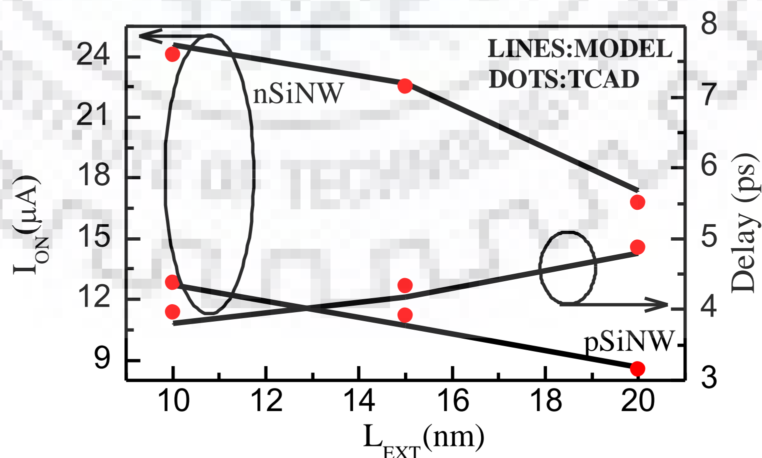


Figure 3.13 Model calculated I_{ON} of the device and inverter delay compared to TCAD to change in extension length for SiNW FET.

Further, Figure 3.12 demonstrates the dynamic characteristics of inverter with FO1 load (53aF), illustrating excellent matching with TCAD. Thereafter, the impact of geometrical parasitic (by

varying extension length) on the device (I_{ON}) current and CMOS inverter delay are illustrated in Figure 3.13 along with TCAD predicted results. The good agreement between compact model and TCAD highlights the accuracy of the model, including parasitic incorporated in the compact model, and its importance in understanding circuit performance. This model can be utilized to design and analyze NW based CMOS logic circuits and SRAM memory cell.

3.10 Summary

The chapter can be summarized as:

1. This chapter presents an accurate, unified compact Verilog-A model for lateral nSiNW and pSiNW FETs, considering all the advanced physical effects. The model integrates scalable parasitic resistance and capacitance. The model accurately predicts device characteristics obtained from TCAD as well as reported fabricated device.
2. Further model validated for single and multiwire devices characteristics which is very important in circuit design.
3. Finally, we simulate NW CMOS inverter circuit and performed the static and transient analysis by varying extension length, the model results are in good agreement with TCAD simulations. The results of circuit simulation demonstrate the value and importance of NW CMOS circuit simulation using HSPICE and Verilog-A framework.
4. This developed compact model is very fast, taking few seconds for the circuit simulation on other hand TCAD takes a much longer time (upto a day) for circuit simulation. Using this model, simulation and design of full range of NWCMOS based digital circuit like SRAM memory and NW based CMOS logic circuits such as AND, OR, NAND and cell library etc. can be easily done. This circumvents the need for performing lengthy, complex, and time consuming TCAD based simulation.

4 CHAPTER

Silicon Nanowire FET based Circuit Design and Analysis

4.1 Introduction

In literature, SiNW FET based circuit design and analysis via TCAD mixed-mode simulation has been investigated [100], [101] which is very time consuming (which can take up to 24 hours). In order to overcome the time consuming TCAD based SiNW FET based circuit simulation, an accurate compact model is reported in chapter 3 developed, which includes the important nanoscale effects and device parasitics.

In this chapter, a unified Verilog-A compact model developed in chapter 3 has been employed for SiNW FET based circuit simulation and analysis. The calibrated model card has been employed todesign the basic logic gates such as INVERTER, NAND, NOR, buffer, XOR and XNOR for performance analysis. Further, the SRAM design and analysis has been done with multi-wire sizing technique. For SRAM cell design, certain current drive strength ratio between the pull-up (PU), access (ACC) and pull-down (PD) transistor are required. Therefore, depending upon the strength of transistors, SRAM cell design is characterized in various configurations. The different configurations e.g. 'C_111', 'C_112', 'C_113', and 'C_123' ('C_111' denote the number of wires in PU, ACC, and PD transistor respectively) are investigated in terms of performance (static and dynamic), layout area and variability to find the most suitable configuration for SiNW based SRAM cell.

The nanoscale device dimensions have brought a significant device to device random as well as systematic process-induced variation[102]. It may lead to significant uncertainty in the circuit performance. The random variations in SiNW FET includes random dopant fluctuation (negligible in SiNW due to undoped channel) [103], Metal Gate Granularity (MGG) [104], Line edge roughness (LER)[105]. The systematic process induced variation, which includes geometric dependent parameters such as effective channel length, radius and oxide thickness [106]–[108]. We investigate the effect of geometric dependent process variation through Verilog-A compact model on SiNW FET based 6T SRAM cell. The N-curve method has been employed to investigate the effect of geometrical variability on the static read and write stability of SiNW FET SRAM Cell in different design configurations (e.g. C_111, C_112,

C_113, and C_123). Finally, the effects of voltage scaling (0.8V to 0.4V) on the read/write voltage and current noise variability of SRAM cell have been investigated.

4.2 Logic Gates Design

In this section, we describe the generation of 10 nm SiNW based logic gates design and examine a different figure of merits. We discuss the sizing of SiNW based inverter, NAND, NOR, buffer, XOR and XNOR gates for the minimum delay. Other performance parameters such as propagation delay, power consumption, energy, energy delay product (EDP), and power delay products (PDP) are also evaluated, for a wide range of input slew and fan-out [109], [110]. The important thing that has to be taken care of while designing the logic gates is that the rise and fall time at the output should be the same. Unlike MOSFET in which drive strength can be tuned by changing the width of the transistor, in case of SiNW FET drive strength depends on the following factors: no of parallel wires, extension length, and diameter of the nanowire. Changing the extension length and diameter of a nanowire becomes fabrication complexity and results in variability, therefore; we are considering a multiwire sizing technique to match the drive strengths.

4.2.1 Sizing of Logic Gates

First, we investigate the number of wires used to pull up and pull down transistor to achieve an equal rise and fall time. For sizinginverter (INV) 1X cell shown in Figure 4.1(a), 1 wire in pull up p-SiNW FET and 1 wire in Pull down n-SiNW FET is used to match the rise-fall delay. For the design of multiple drive strength logic gates, such as INV 2X, INV 3X, and INV 4X an extra transistor in parallel to the existing INV1X transistors are used to rise-fall delay matching. Finding the number of transistors required to pull up and pull down the network for equal fall and rise time is done using Hspice simulations.

NAND/NOR gates are designed such that the fall/rise delay matched to the template inverter. To achieve the same, we need to size the stack transistors correctly. In the case of super threshold stacking, this problem can be solved by selecting the appropriate number of wires in stack transistor so that the current flowing throught the pull down in case of NAND and pull up in case of NOR has a same current driving strength as that of INV 1X. Figure 4.1(b) shows the sizing of NAND gate in which digits ‘1’ or ‘2’ denotes the number of wires used for the smallest NAND gate based on the HSPICE simulation. Similarly, the sizing of other gates such

as OR, buffer, XOR, and XNOR is performed in the same way and discussed in the next section. Tabel 4.1 shows the device dimentions used in the logic gate analysis.

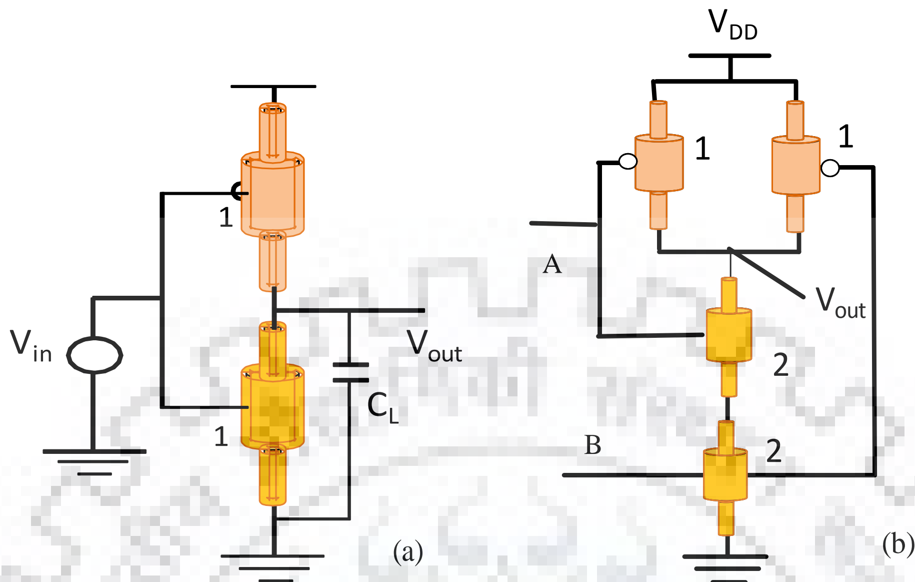


Figure 4.1(a) Shows the schematic of an inverter (b) illustrates the schematic of NAND gates, digit numbering indicates the number of wires in parallel.

Table 4.1 Device dimentions used in the logic gate analysis

Parameters	Values		
	nSiNW FET	pSiNW FET	PTM 16nm FinFET
Channel Length L_G (nm)	16	14	16
Radius R (nm)	10	8	-
Fin Height (nm)	-	-	26
Fin Width (nm)	-	-	12
t_{ox} (nm)	1	1	0.8
V_{DD} (V)	1	1	1

4.2.2 Propagation Delay, Input Output Characteristic of Inverter and Input Capacitance of Logic Gates

The timing parameter of the logic gate includes the propagation delay of the circuit and transition time of the applied pulse that output takes while input change. Propagation delay shown in the Fig. 4.2, is defined as the time interval when the input signal crosses 50 % of V_{DD} to the time when output crosses 50 % of V_{DD}. The propagation delay is an average the high to

low (t_{phl}) and low to high delay (t_{plh}) of an inverter as shown in Fig. 4.2. The propagation delay high to low (t_{phl}) is the delay when output switches from high-to-low, after input switches from low-to-high. The propagation delay low to high (t_{plh}) is the delay when output switches from low-to-high, after input switches from high-to-low. The delay is usually calculated at a 50% point of input-output switching, as shown in the Fig. 4.2. In order to calculate the propagation delay, we use single input switching assumption, which states that only one input will make a transition at a time while keeping the other inputs at a constant voltage.The time taken by the input signal to rise from 10% to 90% of the V_{DD} as defined as input slew in this work. Further, the static voltage transfer characteristic (VTC) of the SiNW FET inverter is shown in Fig 4.3.

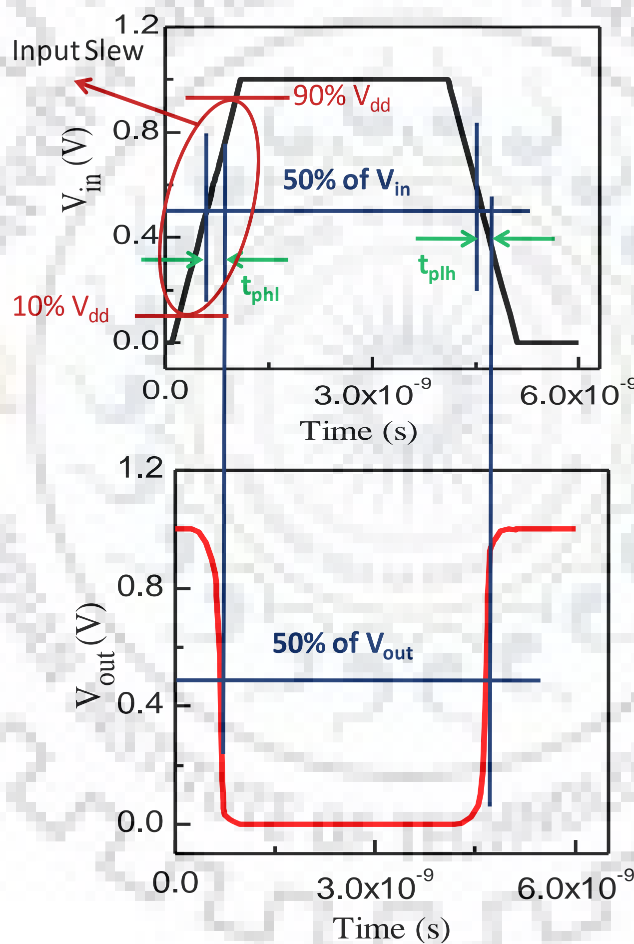


Figure 4.2 Shows the propagation delay and input slew.

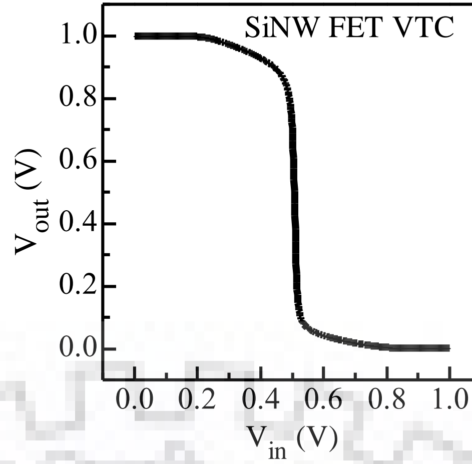


Figure 4.3 Shows the input and output characteristic of the inverter.

Further, input capacitance for the particular input pin is calculated by integrating the input current over the time that input signal switches divided by change in supply voltage during the switching period. The input capacitance of INV1X, INV2X will not be same as later will include number of transistors so more parasitic. The input capacitance of the inverter is expressed as

$$C_{in} = \frac{\Delta Q_{in}}{\Delta V_{in}} = \frac{\int_{t,0.2V_{in}}^{t,0.8,V_{in}} I_{in}\, dt}{\Delta V_{in}} \tag{4.1}$$

whereas ΔQ_{in} is change in charge with change in the input voltage (ΔV_{in}) of the inverter.

4.2.3 Power Dissipation

The power dissipation in a circuit consists of leakage power, switching power, and short circuit power. Switching power consumption occurs when there is charging or discharging of the load capacitance. Here we considered only dynamic power consumption over a period. For dynamic power first, we calculated the energy from charge through average current integration then divide by a period of input pulse. The dynamic power consumption of basic logic gates by considering different fanout and input slew has been analyzed.

Total Power Dissipation (per cycle) = Static Power Dissipation + Dynamic Power Dissipation

$$= \int_0^t V_{DD}\, I_{leak}\, dt + \int_0^t C_L V^2{}_{DD}\, f\, dt \tag{4.2}$$

whereas V_{DD} and I_{leak} are the supply voltage and leakage current. C_L and f are the load capacitance and the frequency of transition.

4.3 Logic Gates Performance Analysis

In this section, we demonstrate the energy and power efficient 10 nm SiNW CMOS based core logic gates design and comparison with the 16 nm predictive technology model (PTM) MG FinFETtechnology [111]. The core logic gatesconsist of INVERTER, NAND, NOR, Buffer, XOR and XNOR are analysze for wide range of input slew and load capacitance (FO1 and FO4).

4.3.1 Inverter, NAND, and NOR Gate Performance Analysis

The output capacitance of the inverter is estimated from the current integral method as discussed earlier, values of fanout capacitance FO1, FO2, and FO4 are calculated as 58aF, 116aF, and 232aF respectively. Figure 4.4 (a-b) shows the propagation delay [(t_{phl} +t_{plh})/2] and energy consumption per cycle of INV1X for FO1 and FO4. It is shows that the delay of SiNW FET based inverter is nearly the same as FinFET for both the load capacitance. Whereas the energy consumption per cycle of SiNW FET based inverter is significantly lower (more than 2X) than FinFET. The lower energy consumptions illustrate that the NW based circuit is more energy efficient and can be operated to the lower supply voltage to save more dynamic energy. Further, the different drive strength inverter can be design such as INV2X, INV3X etc., by simply increase in the number of wires in the pull up and pull down transistor of INV1X. Figure 4.5 (a-b) shows the large advantage in energy delay product (EDP) and power delay product (PDP) of the SiNW FET inverter at V_{DD} = 1 V compared to FinFET.

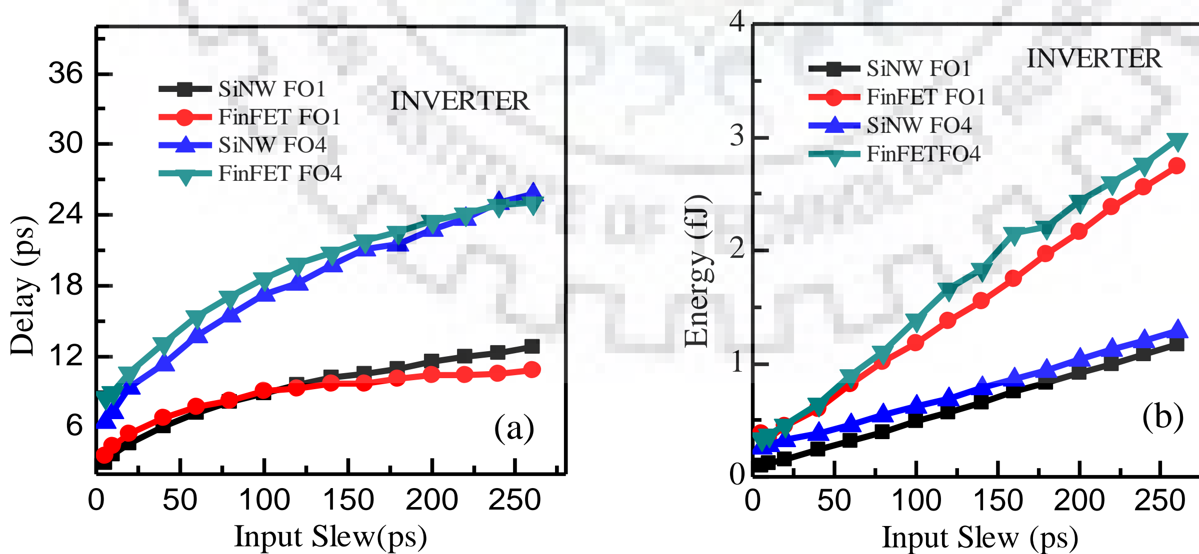


Figure 4.4 (a-b) Average delay, energy consumption comparison between SiNW and FinFET based INV 1X for different input slew and load capacitance.

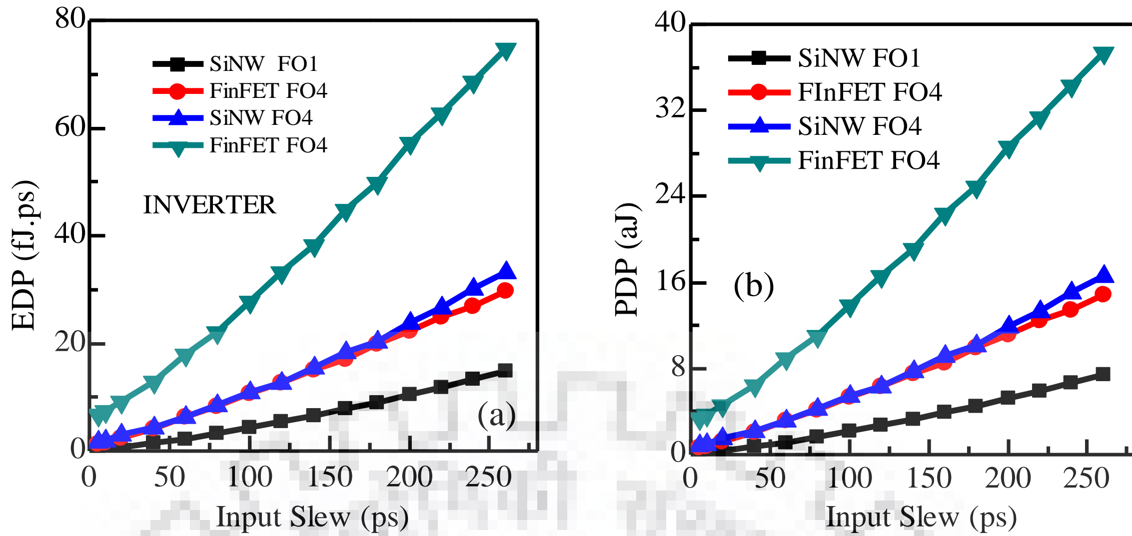


Figure 4.5 (a-b) Energy delay product (EDP), power delay product (PDP) comparisons between SiNW and FinFET based INV 1X for different input slew and load capacitance.

Figure 4.6-4.7 compares the propagation delay and dynamic power dissipation of SiNW FET and FinFET based NAND and NOR gate for a wide range of input slew from 10ps to 260ps at FO1 load. The propagation delay of SiNW FET based NAND and NOR gates is almost equal to FinFETs but the dynamic power is significantly lower for Si NW CMOS. The SiNW CMOS NAND/NOR gate has a ~3X less power consumption as compared to 16 nm FinFET. Table 4.2 compares the energy delay product (EDP) between SiNW and FinFET based 2 input NAND and NOR gates for FO1 load. One can observe from the table that SiNW FET NAND and NOR gate are more energy efficient, showing ~2-3X advantage compare to FinFET due to smaller gate capacitance, better gate control, and short channel immunity. The performance metric of the circuits can be evaluated by the power delay product (PDP), which is the multiplication of average power consumptions and the maximum delay.

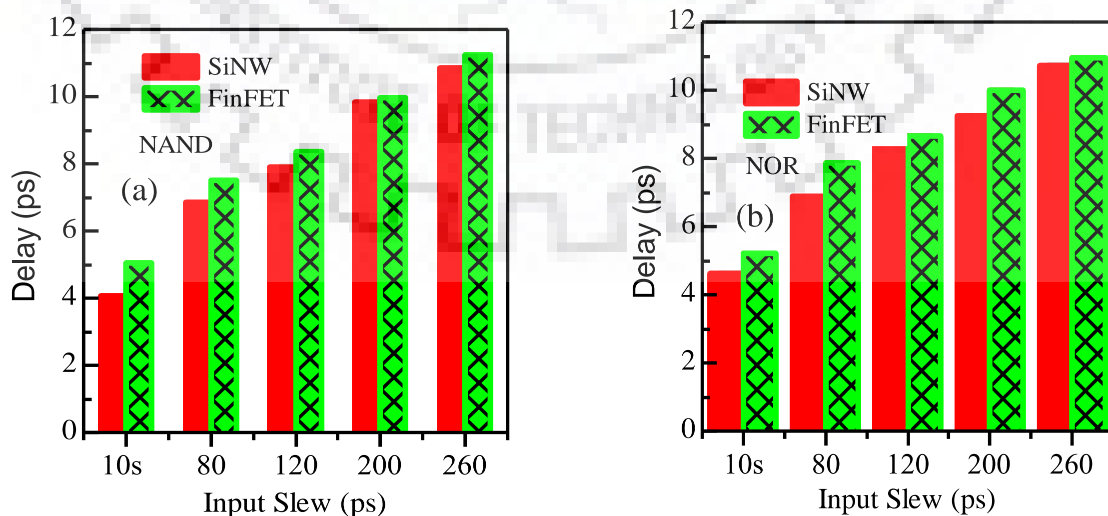


Figure 4.6 (a-b) Delay comparisons between SiNW and FinFET based NAND and NOR 1X for different input slew and load capacitance.

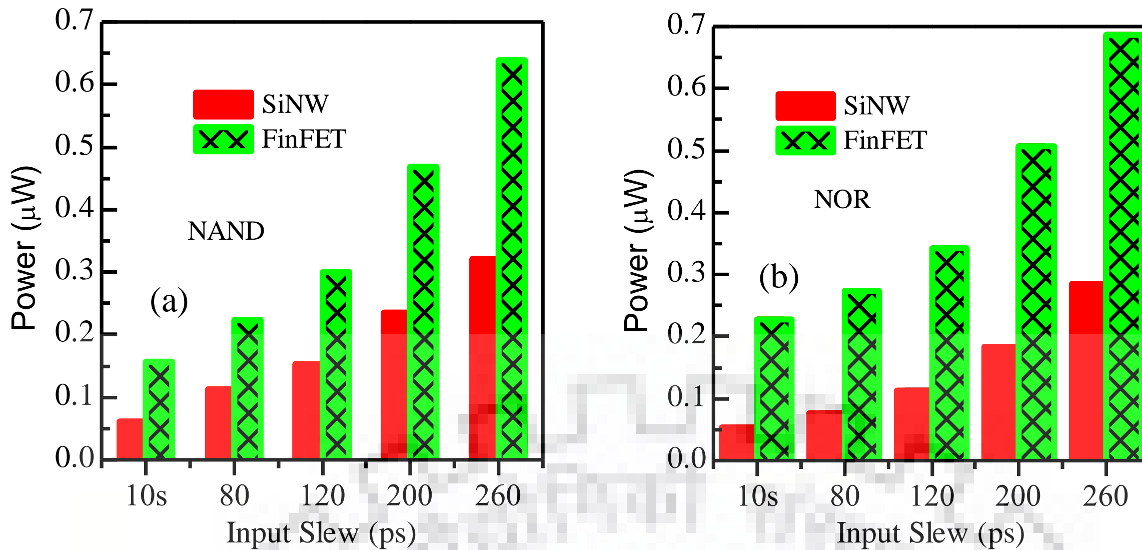


Figure 4.7 (a-b) **Dynamic powerconsumption comparisons between SiNW and FinFET based NAND, NOR 1X for different input slew and load capacitance.**

Table 4.3 shows the performance comparison in terms of PDP between SiNW and FinFET based NAND/NOR gates in super threshold regime. The SiNW FET NAND gate has a ~3X better PDP, the NOR gate has ~4X better PDP at low input slew and ~3X at high input slew compared to 16 nm FinFET. These comparisons of delay, power, energy, PDP, and EDP results showcase the benefits of choosing Si NW CMOS logic gate for power and energy efficient application.

Table 4.2 Energy delay product of NAND and NOR gate.

	SiNW 10 nm Energy-Delay Product (fJ.ps)			
	NAND FO1		NOR FO1	
Rise/Fall time (ps)	SiNW FET	FinFET	SiNW FET	FinFET
10	0.495	1.737	0.628	2.564
40	1.554	4.506	1.562	5.398
80	3.395	9.261	3.393	9.495
120	5.71	13.88	5.74	14.81
160	8.209	19.56	8.144	19.82
200	11.25	24.07	11.08	25.18
240	14.08	30.42	14.07	31.56
260	15.51	33.83	15.69	34.44

Table 4.3 Power delay product of NAND and NOR gate.

	SiNW 10 nm Power-Delay Product (µ.W)			
	NAND FO_1		NOR FO_1	
Rise/Fall time (ps)	SiNW FET	FinFET	SiNW FET	FinFET
10	0.2479	0.8685	0.3145	1.282
40	0.3949	1.39	0.4176	1.715
80	0.7769	2.253	0.7809	2.699
120	1.215	3.166	1.333	3.697
160	1.698	4.631	1.696	4.747
200	2.308	5.559	2.287	6.045
240	2.855	6.94	2.87	7.403
260	3.478	8.316	3.518	8.41

4.3.2 Buffer, XOR, and XNOR Gates Performance Analysis

Figure 4.8 (a-b) compares the propagation delay and dynamic power dissipation of SiNW FET and FinFET based 2 stage buffer for a wide range of input slew from 5 ps to 220ps at FO1, FO4 loads. The 2 stage buffer can be used as a delay element and to drive a larger fanout load. The 1:1 number of wires in a pull up and pull down is used to design a minimum size a SiNW FET buffer. It shows that the propagation delay of SiNW FET based buffer for FO1 and FO4 loads is almost equal to FinFETs. Whereas, the dynamic power dissipation in SiNW FET buffer is ~3X lower than FinFETs based buffer. The high driving capability, power efficient buffers can also be design by increasing the number of wires in pull up and pull down transistors such as 2:2, 3:3 etc. Figure 4.9 (a-b) shows the energy consumption per cycle and energy delay product comparison between SiNW FET and FinFET based 2 stage buffer. It is observed that the SiNW FET buffer is highly energy efficient, which is ~ 3X lower in energy consumption compared to FinFET technology. Further, we show the power delay product (PDP) comparison and from Figure 4.10, one can observe that the 10nm SiNW FET technology achieves much better PDP, which is ~ 3X the lower value against the FinFET technology.

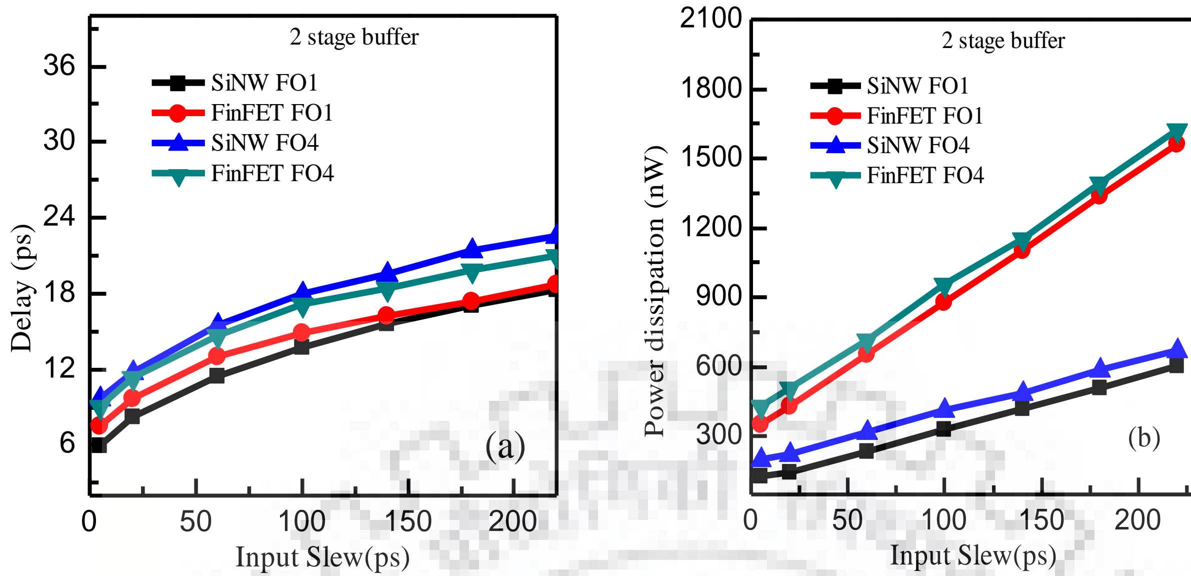


Figure 4.8 (a-b) Delay and power dissipation comparison between SiNW and FinFET based 2 stage buffer for different input slew and load capacitance.

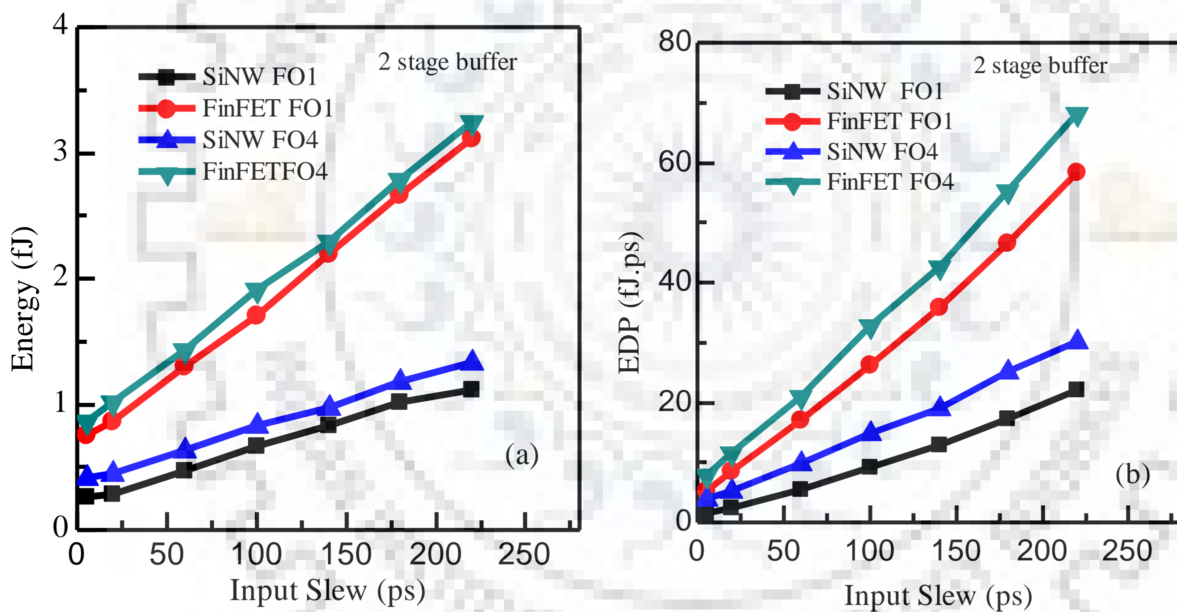


Figure 4.9 (a-b) Energy consumption per cycle and energy delay product (EDP) comparison between SiNW and FinFET based 2 stage buffer for different input slew and load capacitance.

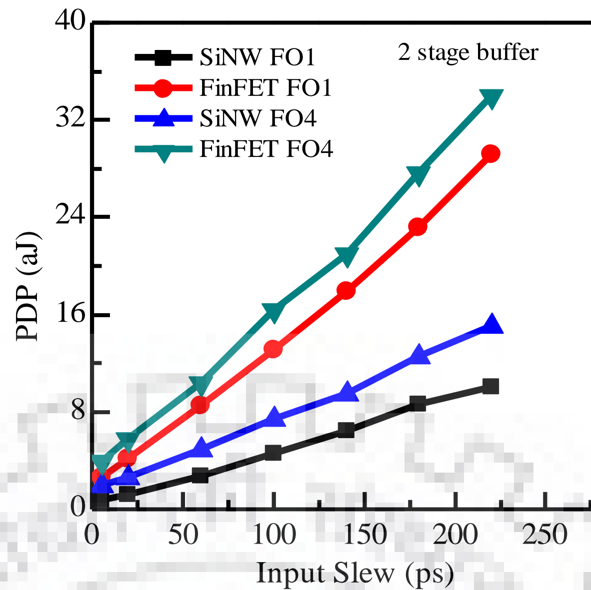
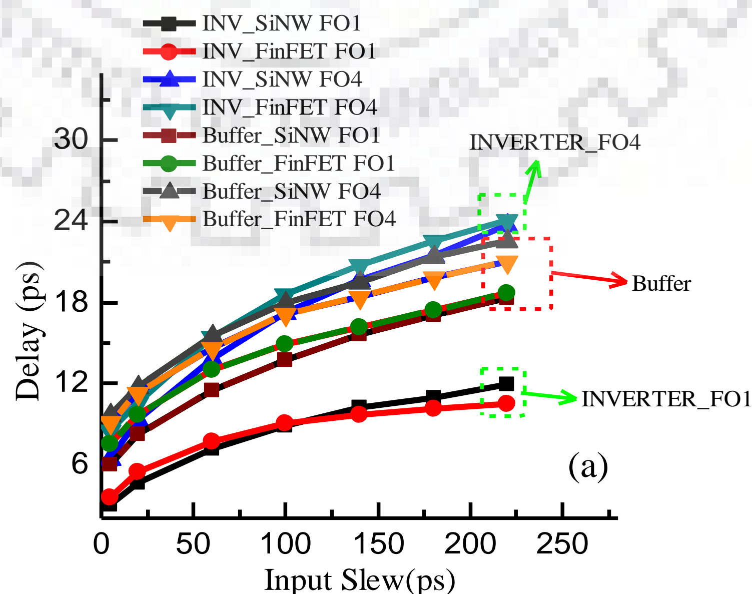


Figure 4.10 Power delay product (PDP) comparison between SiNW and FinFET based 2 stage buffer for different input slew and load capacitance.

Figure 4.11(a) shows the comparison of the delay between an inverter and 2-stage buffer for FO1 and FO4 load. The buffer FO1 shows a higher delay compared to an inverter FO1 delay. The buffer has higher delay due to one extra stage, which addsan extra delay between input to output as compared to the inverter delay. In the case of FO4 load, the buffer has lower delay compared to the inverter with FO4 load; this is because the first stage in the buffer is having FO1 load (as shown in the Figure 4.11(b)), therefore, at the intermediate node 'X' transition is very fast which is the input to the second stage. The fast transition at intermediate node leads to decrease the delay of buffer FO4 load. However, the inverter is directly driving the FO4 load.Therefore, overall delay is higher for the inverter with FO4 load compared to 2-stage buffer.



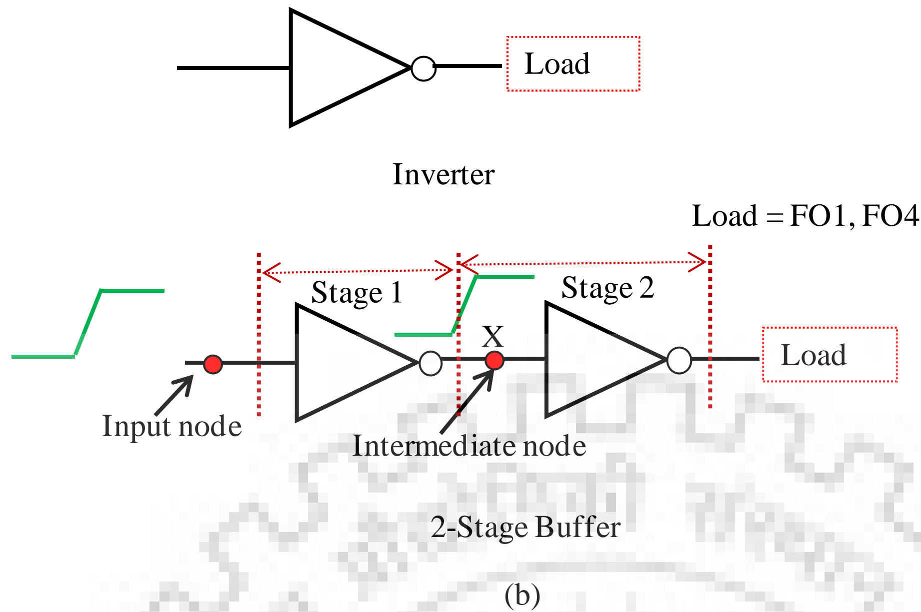


Figure 4.11 Shows the delay comparision between Inveter and buffer at FO1 and FO4 load.

Figure 4.12 (a-b) compares the propagation delay and dynamic power dissipation of SiNW FET and FinFET based XOR gate for a wide range of input slew from 5 ps to 220 ps at FO1, FO4 loads. The multiwire sizing technique is employed to design 2 input XOR gate. It is found that the propagation delay of SiNW FET based XOR gate for FO1 and FO4 loadsis almost equal to FinFETs technology. Whereas the dynamic power dissipation in SiNW FET XOR gate is lower than 4X to than the FinFETs technology. The multidrive strength and power efficient XOR gate can be design such as XOR 2X, XOR 3X by increases the number of wires in pull up and pull down transistor of XOR gate.

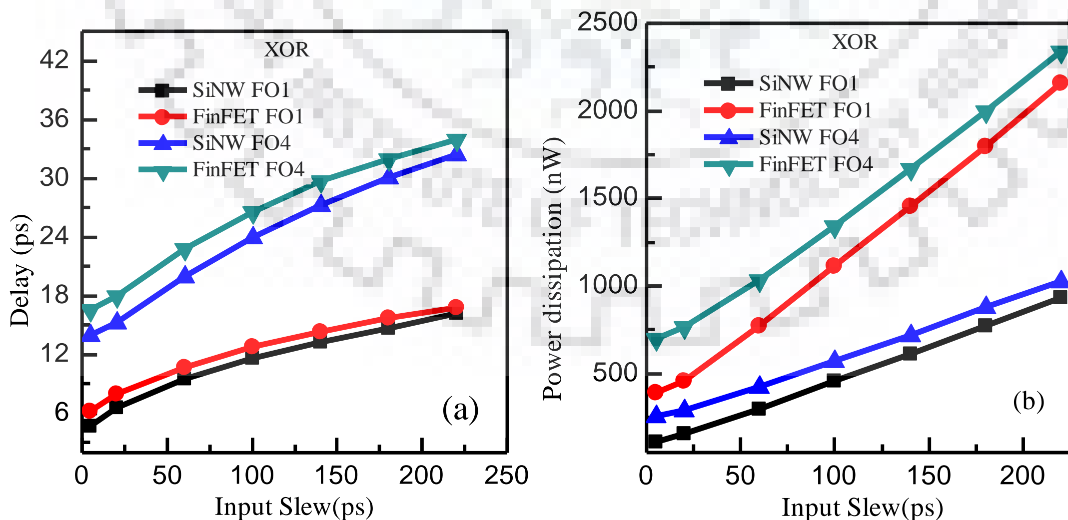


Figure 4.12 (a-b) Delay and power dissipation comparison between SiNW and FinFET based XOR gate for different input slew and load capacitance.

Further, Figure 4.13 (a-b) shows the energy consumption per cycle and energy delay product (EDP) comparison between SiNW FET and FinFET based XOR gate. It is observed that the significant amount of energy reduction, up to ~3X is achieved by operating 10nm SiNW FET XOR gate in the super threshold regime against the 16nm FinFETs technology. Further, we show the power delay product (PDP) comparison and from Figure 4.14, one can observe that the 10nm SiNW FET technology achieves much better PDP, which ~ 4X lower value against the FinFET technology.

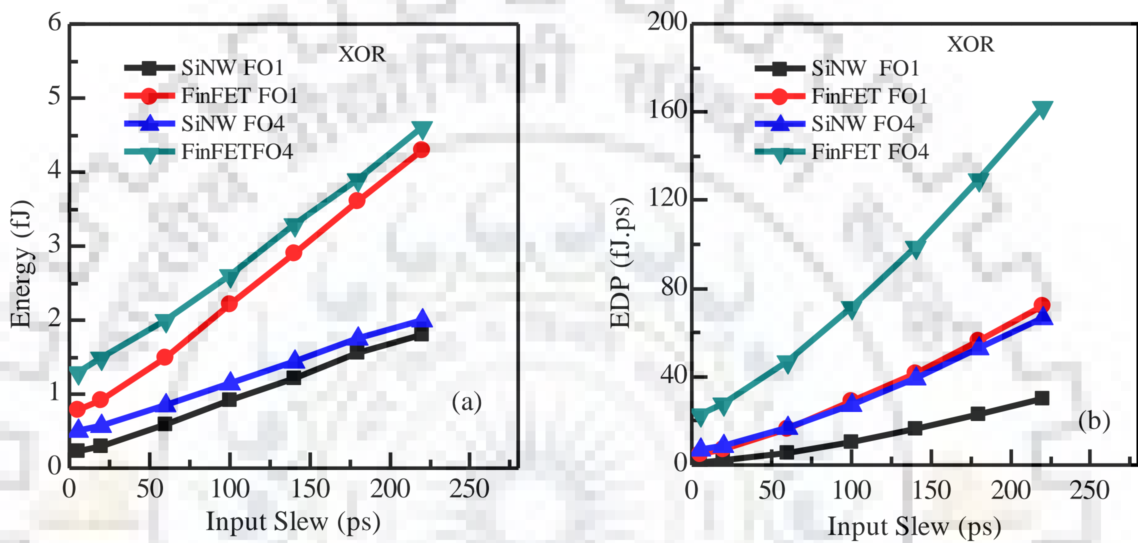


Figure 4.13 (a-b) Energy consumption per cycle and energy delay product (EDP) comparison between SiNW and FinFET based XOR for different input slew and load capacitance.

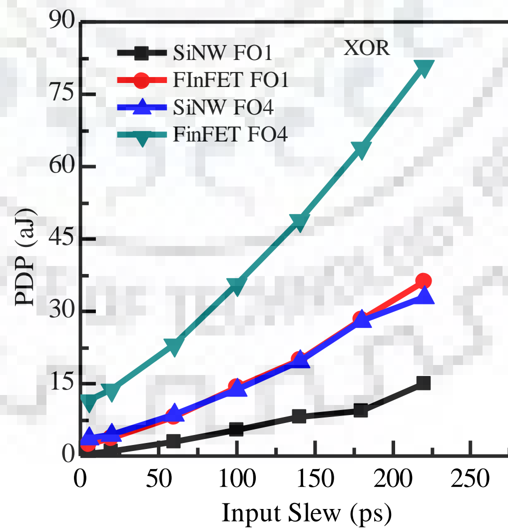


Figure 4.14 Power delay product (PDP) comparison between SiNW and FinFET based XOR for different input slew and load capacitance.

Figure 4.15 (a-b) compares the propagation delay and dynamic power dissipation of SiNW FET and FinFET based XNOR gate for a wide range of input slew from 5 ps to 220ps at FO1, FO4 loads.The propagation delay of SiNW FET based XNOR gate for FO1 and FO4 loadsis almost

equal to FinFETs. Whereas, the dynamic power dissipation in SiNW FET XNOR gate is lower than 3X to that of FinFETs technology. The multidrive strength and power efficient XOR gate can be design such as XOR 2X, XOR 3X by the increase in the number of wire in a pull up and pull down transistor.

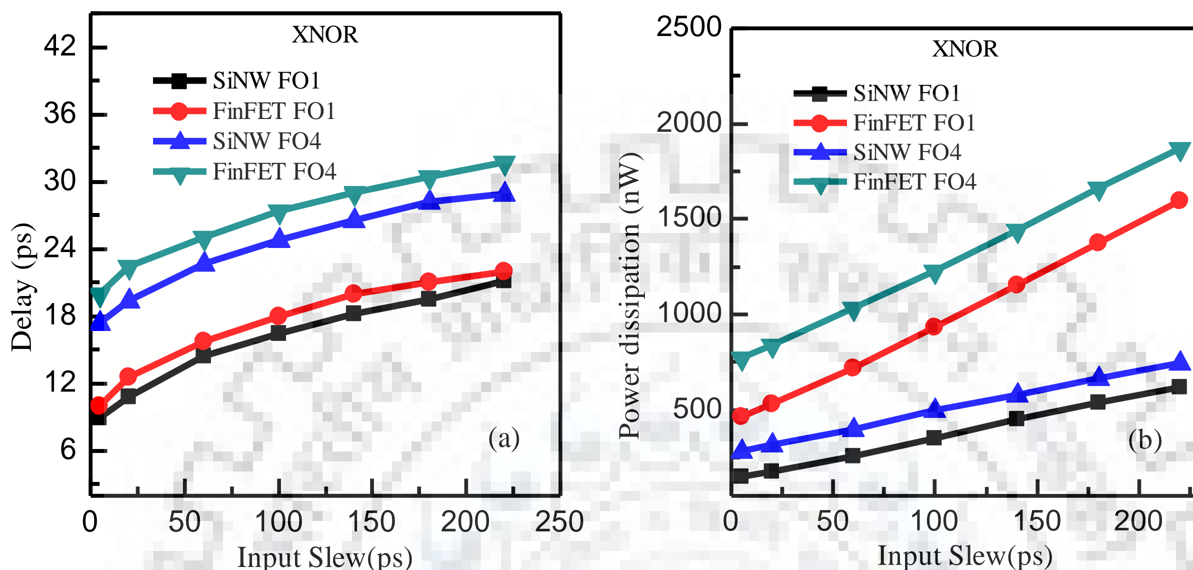


Figure 4.15 (a-b) Delay and power dissipation comparison between SiNW and FinFET based XNOR buffer for different input slew and load capacitance.

Further, Figure 4.16 (a-b) shows the energy consumption per cycle and energy delay product comparison between SiNW FET and FinFET based XNOR gate. It is observed that the significant amount of energy reduction, up to ~3X is achieved by operating 10nm SiNW FET XNOR gate in the super threshold regime against the 16nm FinFETs technology. Further, Figure 4.17 shows the power delay product (PDP) comparison and one can observe that the 10nm SiNW FET technology achieve much better PDP, which is ~ 4X lower value against the FinFET technology.

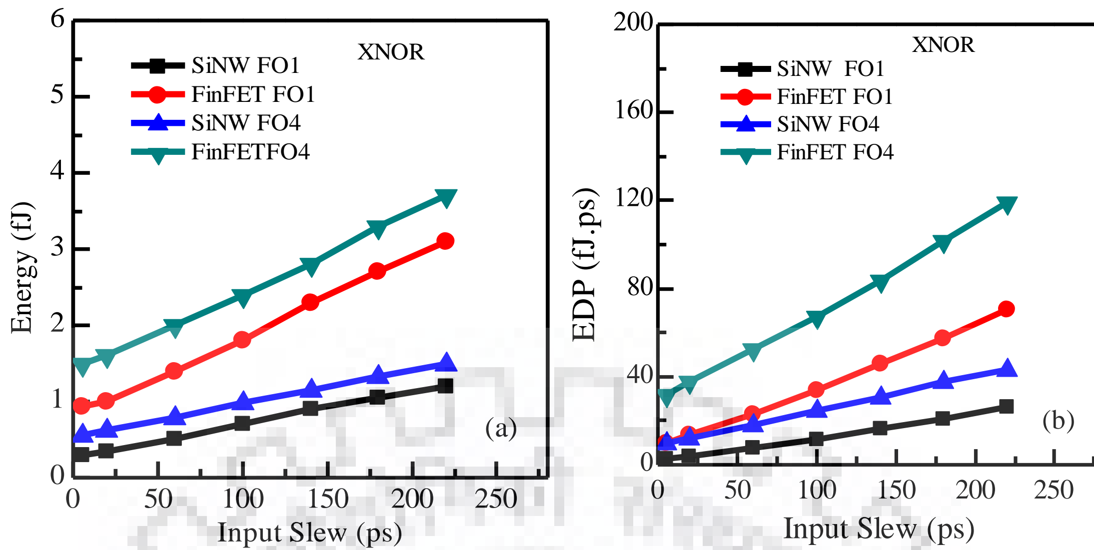


Figure 4.16 (a-b) Energy consumption per cycle and energy delay product (EDP) comparison between SiNW and FinFET based XNOR for different input slew and load capacitance.

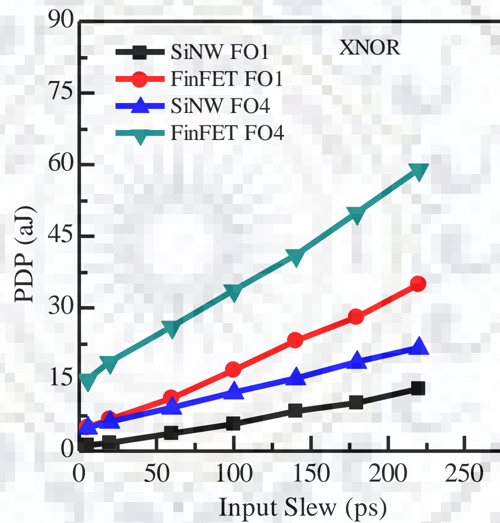


Figure 4.17 Power delay product (PDP) comparison between SiNW and FinFET based XNOR for different input slew and load capacitance.

4.3.3 Impact of Vdd scaling on the delay, energy, EDP and PDP on Inverter

Fig. 18 (a-b) shows the delay and energy consumption of an inverter with the V_{dd} scaling. The delay increases with the V_{dd} scaling due to decrease in the drive current of the transistor. Operating a circuit at near threshold regime, results in reduced energy consumption at the cost of circuit speed degradation. Fig. 18 (b) shows significant energy saving (~15 time) at V_{dd} 0.3V compared to V_{dd} at 1V. Moreover, the energy delay product (EDP) and power delay product (PDP) are also decreases with the V_{dd} scaling as shown in Fig. 18(b-c).

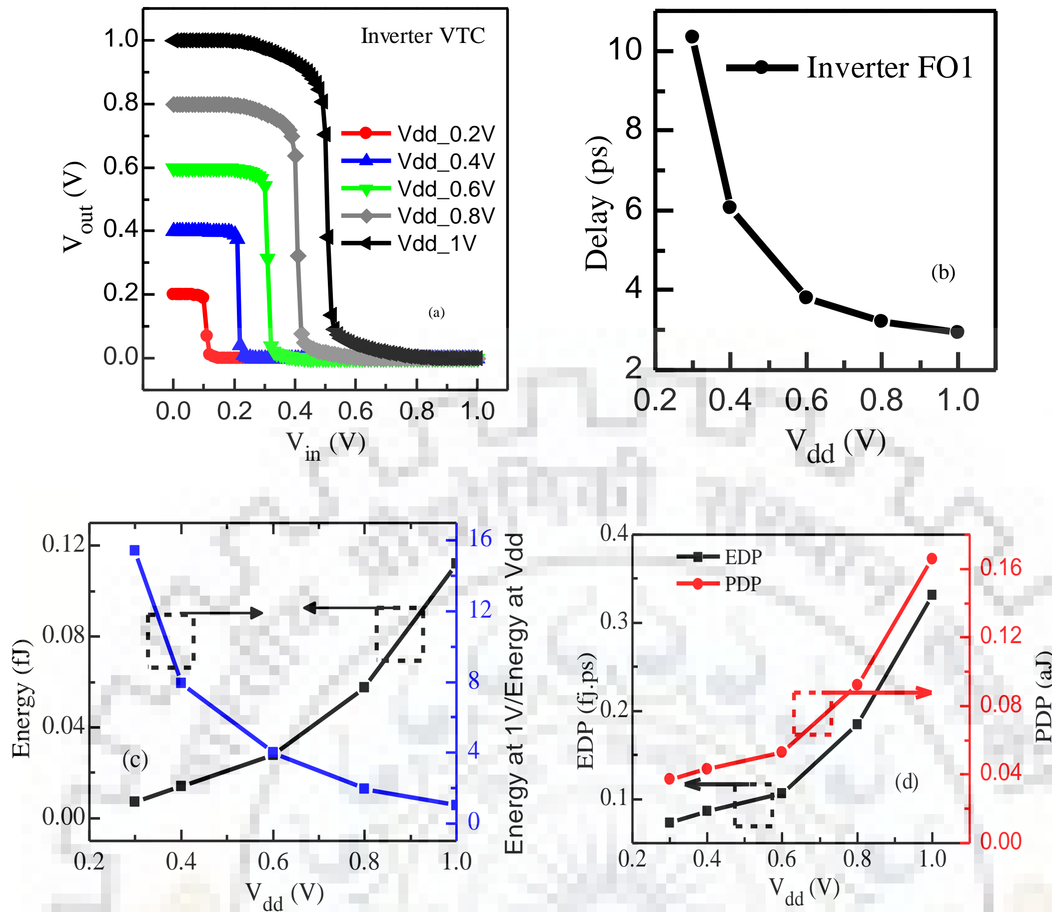


Figure 4.18 Shows the inverter delay, energy, energy delay product and power delay product with the supply voltage scaling.

In summary, the SiNW FET core logic gates such as Inverter, NAND, NOR, buffer, XOR and XNOR performance are analyzed for a wide range of input slew and fanout load. The performance of SiNW FET based logic gates is compared with FinFET based logic gates. It is found that the propagation delay of the SiNW FET logic gates is nearly same as of FinFET based logic gates. Whereas, the power dissipation and energy consumption of SiNW FET based logic gates is ~3X lower than the FinFET based gates. In addition, we have compared the important figure of merit such as energy delay product (EDP) and propagation delay product (PDP). It is found that the SiNW FET logic gates achieved much better EDP and PDP, which are ~4X lower against the FinFET technology. Therefore, the SiNW FET based circuit design and analysis is highly preferable for high speed, energy efficient and low power application. Moreover, from the above results a circuit designer can opt for an appropriate combination of input slew and load capacitance to build the SiNW FET based energy and power efficient large circuit design such as ISCAS'85 benchmarked circuits, standard cell library.

4.4 SRAM Cell Design and Analysis

In this section, SiNW FET SRAM cell read and write stability are investigated for various design configurations. The computational effort and time is taken for circuit simulation using our compact model are significantly smaller when compared to TCAD simulations (1 to 2 days).

Figure 4.19 (a) shows the schematic of SiNW FET based 6T static RAM (SRAM) cell in C_112 configuration. The notation C_112 denotes the number of wires in pullup (PU), access (ACC) and pulldown (PD) transistor respectively. Unlike MOSFET in which current strength depends upon the width of the transistor, SiNW FET has wire as channel and its driving strength is increased by increasing the number of wires. A 6T SRAM cell has $W_{PD}/W_{ACC} \geq 1$ and $W_{PU}/W_{ACC} \leq 1$ for acceptable Hold, Read and Write SNM, respectively [112].

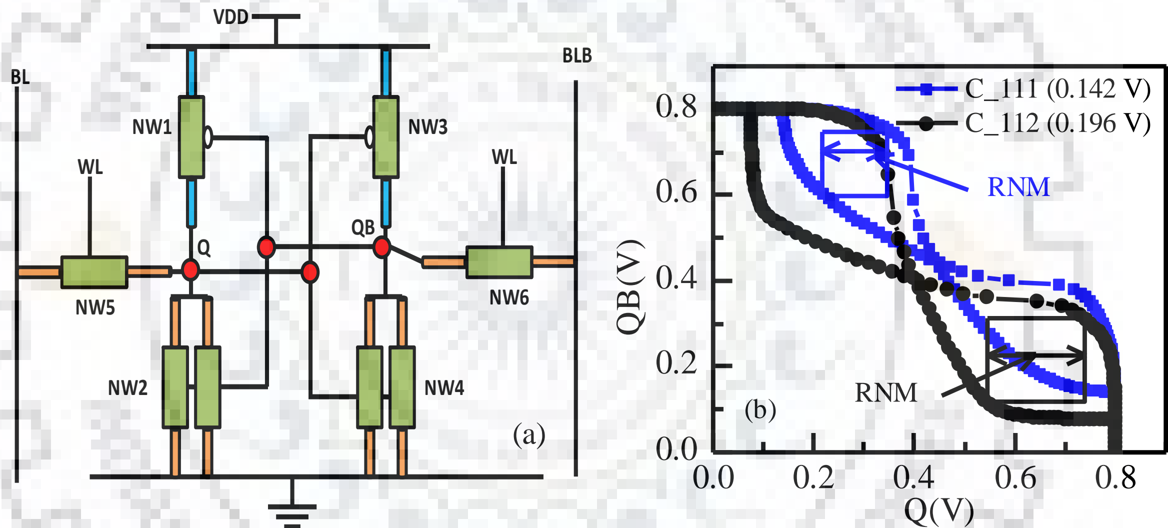


Figure 4.19 (a) 6T SRAM cell schematic based on SiNW FET (C_112 configuration), (b) Butterfly curve for RNM in C_111, C_112 configuration.

4.4.1 Read Stability

The read stability of the SRAM cell is characterized by the read static noise margin (RNM). During the read operation mode the bit cell node Q stores '0' and QB node stores '1' keeping BL, BLB, and WL '1' respectively as shown in Figure 4.19(a). The RNM is computed from the side of maximum square embedded into the butterfly curve formed by the DC sweep of input of the cross coupled inverters as shown in Figure 4.19(b). For the successful read operation, the voltage at the bit cell node Q should not exceed the threshold voltage of the pull down (PD) transistor $NW4$ in Figure 4.19(a) [113], [114]. However, read stability of SRAM cell can be achieved by using proper drive strengths of pull-up (PU), access (ACC), and pull-down (PD) transistors. We have considered various design configurations (such as C_111, C_112, C_113

etc.) for SRAM cell analysis. Figure 4.19 (b), the butterfly curve shows the RNM value of 142 mV, 196 mV in high density C_111 and C_112 configurations. Further, we have analyzed other different configurations to get high RNM value. Figure 4.20 (a) shows the RNM of SiNW SRAM cell in different configurations C_111, C_112, C_113, C_124, and C_123. It is found from the configurations that, with increase in the number of wires in the PD transistor while keeping ACC transistor wire constant. The RNM value increases due to a decrease in the resistance of PD transistor compared to ACC transistors (e.g. in C_113 PD has 3 wires and resistance is equal to $R_{total}/3$). Therefore, lower the node voltage $V\ (Q)$ at Q owing to voltage division of the series resistance combination of the ACC and PD transistor.

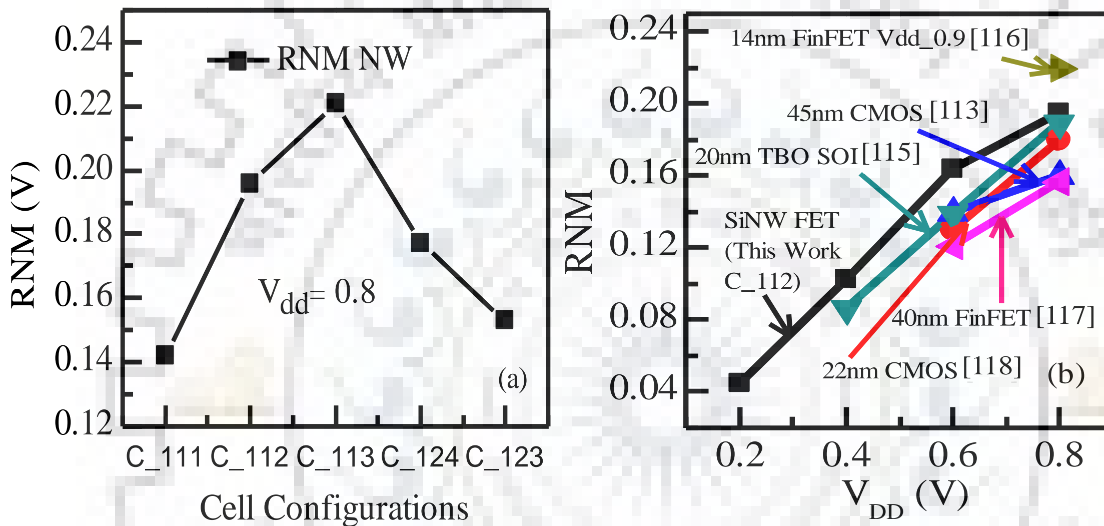


Figure 4.20 (a) READ SNM of SiNW FET 6T SRAM cell in different configurations, (b) RNM comparison with voltage scaling between SiNW and published experimental FinFET, planar devices.

The RNM decreases with an increase in the number of wires in ACC transistor relative to PD transistors such as configuration C_124 (0.177V) to C_123 (0.153V). This is due to reduction in the resistance of ACC transistor causing higher $V\ (Q)$ which may lead to flip the storage node. Therefore, from this analysis, we can select the appropriate number of wires in the ACC and PD transistor for higher read stability (high SNM). Out of all configurations, C_112 and C_113 are the best configurations for higher RNM value. Figure 4.20(b) shows the RNM stability with voltage scaling upto 0.2V for 10 nmSiNW FET in 'C_112' configuration. Further, it is compared with other technology nodes such as fabricated data of 45 nm bulk CMOS [113], 20nmthin-buried-oxide SOI (TBO-SOI) [115], 14 nm technology node FinFET at V_{dd} 0.9 [116], 40 nm FinFET [117] and 22 nm CMOS [118]. It is the most stable configuration for low power applications.

4.4.2 Write Stability

The write stability of SRAM cell can be measured by the write noise margin (WNM). The WNM of SRAM is estimated using the butterfly curve formed by the combination of write and read VTC [119]. The write VTC is extracted by DC sweeping the storage node voltage Q, with BL and WL operated at '1' and BLB biased at '0' while monitoring storage node voltage QB. The WNM is quantified by the side length of smallest square inscribed in the butterfly curve formed by the read and the write VTC of same configuration SRAM cell at the lower half of the curve. The single crossover point in the WNM butterfly curve shown in Figure 4.21(a) indicates the successful write '0' operation. This is due to the voltage V(QB) pulled below the trip point of the inverter formed by $NW1 - NW2$, otherwise, it is difficult to write. The writability totally depends upon the ratio of access to pullup transistors. Therefore, we have investigated the various configurations to get high WNM by varying the number of wires of access transistors. The WNM in C_111, C_112 configurations are 355mV, 320mV and decreases in C_113 configuration to 280mV, with increases wires in PD transistor. However, WNM increases with increasing the number of wires in access transistor compared to pull up transistor from C_123 (330mV) to C_233 (355mV) configurations. Hence, it is concluded that C_111, C_112, and C_233 are the best configurations for better WNM stability. Further, Figure 4.21(b) shows the comparison of SiNW FET SRAM cell WNM with FinFET [116] and UTB SOI [120] data.

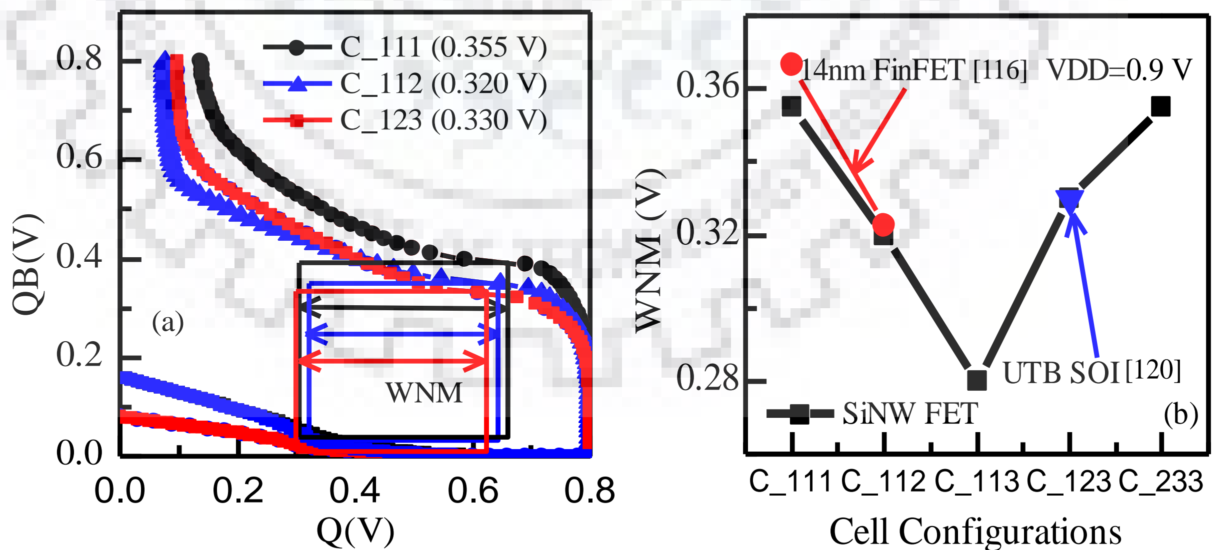


Figure 4.21(a) Butterfly curve for write '0' operation, (b) WRITE SNM of SiNW FET 6T SRAM cell in various configurations.

4.5 Dynamic Analysis of SiNW SRAM Cell

In this section, dynamic performance of SiNW FET 6T SRAM cell, that includes read access time (RAT) and write access time (RAT) are discussed. The number of wires is considered as a design parameter for tuning the current drives to improve the read and write access time.

4.5.1 Read Access Time

The read operation voltage waveform is shown in Figure 4.22(a) as a function of time for 'C_111' configuration. The capacitance associated with bit lines is due to source/drain capacitance ($C_{GD/D,}$ $C_{GD/S}$) of an access transistor. The capacitance associated with word line is two time the C_{GG} of access transistor. Hence, the effective load capacitances considered are 256 times of $C_{GD/D,S}$ and $2\times C_{GG}$ are applied on BL/BLB and word line respectively for RAT [121]. The read access time (RAT) is the time difference between the point when the BL/BLB voltage decreases by 50mV from V_{DD} and 50 % of the WL voltage value [122]. Initially in Figure 4.22(a), before WL rises to the $V_{DD,}$ the node voltages BL, Q, BLB, QB are set at V_{DD}, 0, V_{DD}, and V_{DD}respectively. As the WL begins to increase from 0 to V_{DD}, the ACC (NW5) transistor turns on as shown in Figure 4.22(a), consequently, the BL node starts to discharge from its initial value of V_{DD}through NW5 and NW2 transistor and help to charge the storage node Q. As the WL reaches V_{DD}, the ACC transistor fall in saturation mode and PD transistor is in linear mode. The ACC transistor in saturation mode act as a constant current source that provide constant current to the PD transistor and keeping node voltage Q nearly constant, even though the BL decreases as shown in Figure 4.22(a). The read access time of SiNW FET in C_111 configuration is found to be as 23.84ps. Figure 4.22(b) shows the RAT in various configurations from C_111 to C_233 and comparisons with the published experimental data such as UTB SOI[120], planar CMOS and CNT FET [123], 14 nmFinFET[116], 22 nm SOI FinFET[124].The reason for lower access time (delay=CV/I) in SiNW FET based SRAM cell compared to FinFET is due to high current drive strength in SiNW FET (The drive strength can be further increased with increase in a number of wires and hence lower the access time). The current drive in SiNW FET (from the compact model) is 34 % higher than SOI FinFETs [34]. The RAT decreases with increasing the drive strength of ACC and PD transistor which help to quick charge and discharge the storage node. The configuration C_111 has a highest access time of value 23.84ps and decreases with increase in the number of wires as C_112, C_123, C_233 of value 20.11ps, 10.94ps, and 8.37ps (high speed SRAM cell) at the cost ofmore cell

area. From Figure 4.22(b), it is concluded that the RAT is better for a design considering wires in PD $> ACC > PU$ and PD/ACC ≥ 1.

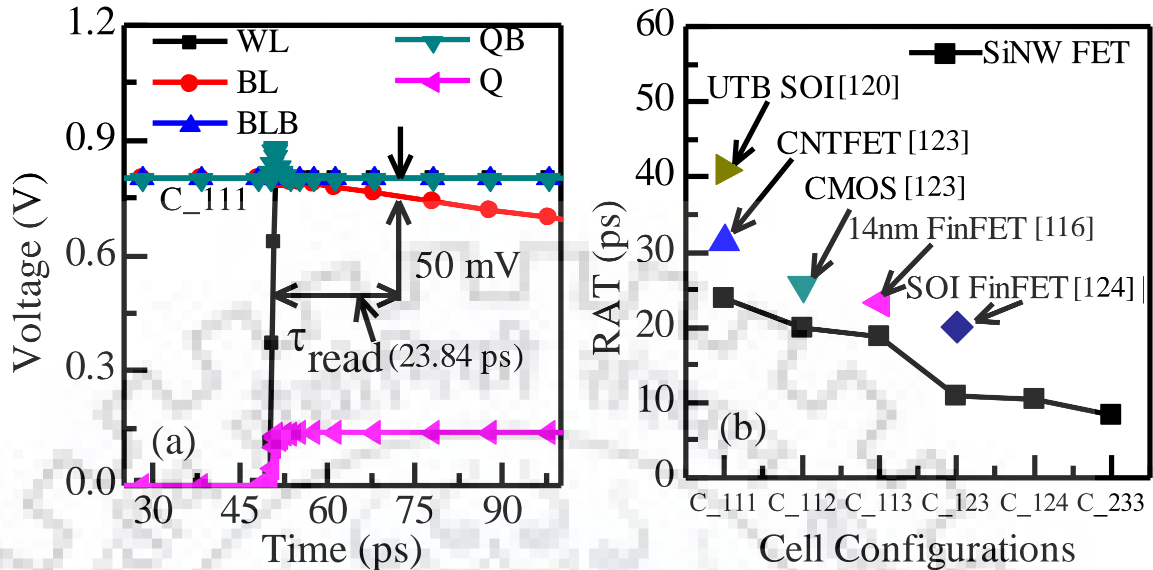


Figure 4.22 (a) Transient analysis during read operation in C_111 configuration, (b) Read access time (RAT) calculation for different configurations and comparison with the published experimental data.

4.5.2 Write Access Time

Write access time (WAT) is the time required to change the stored bit cell logic (Q, QB). The transient analysis is performed for 10 nm SiNW in C_111configuration for WAT as shown in Figure 4.23 (a) by forcing suitable node voltages. Initially, the node voltages at BL, Q, BLB, QB, and WL in write mode are 0, V_{DD}, V_{DD}, 0, and 0, respectively. The effective load capacitance applied on BL, BLB is the same as that is used in the case of RAT. As the word line (WL) begins to increase from '0' to V_{DD} at the same time the node voltages Q, QB begin to start discharging/charging from V_{DD} to 0 and 0 to V_{DD} through the BL and BLB as shown in Figure 4.19 (a). The WAT ($\tau_{(0,write)}$) is the time difference when storage node voltage Q decreases from the $V_{(85\,\%)}$ to $V_{(15\,\%)}$ as shown in Figure 4.23(a).

The WAT ($\tau_{1,write}$) for writing V_{DD} at the bit cell node QB is defined as the time difference when QB node voltage increases from $V_{15\,\%}$ to $V_{85\,\%}$. The average of $\tau_{1,write}$, $\tau_{0,write}$ is defined as the effective WAT. Figure 4.23(b) shows the WAT in various configurations from minimum area SRAM cell C_111 to C_233. As we increase the number of wires in PD transistor, the WAT increases C_111 (1.8 ps) to C_113 (3.01 ps). Whereas, WAT decreases with increasing the number of wires in ACC transistor from C_124 (2.6 ps) to C_233 (1.7 ps) as shown in Figure 4.23(b). It is concluded that the WAT mainly depends upon the number of wires in ACC transistor compared to PU transistor. Moreover, for smaller area SRAM cell designs C_111 and

C_112 are the best configurations with low WAT. Although C_233 showing better WAT compared to C_111, with the additional penalty of more layout area.

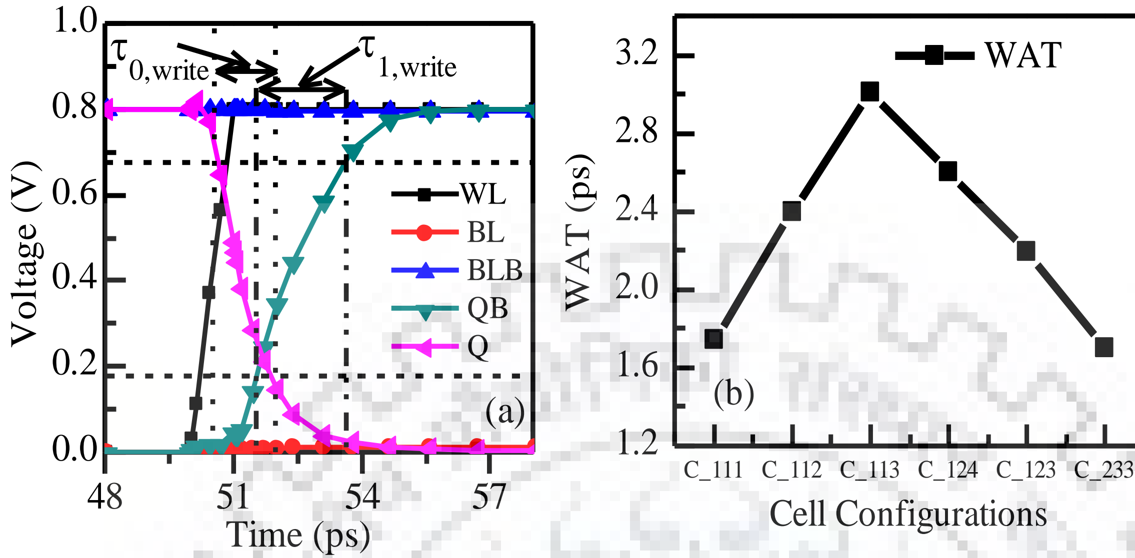
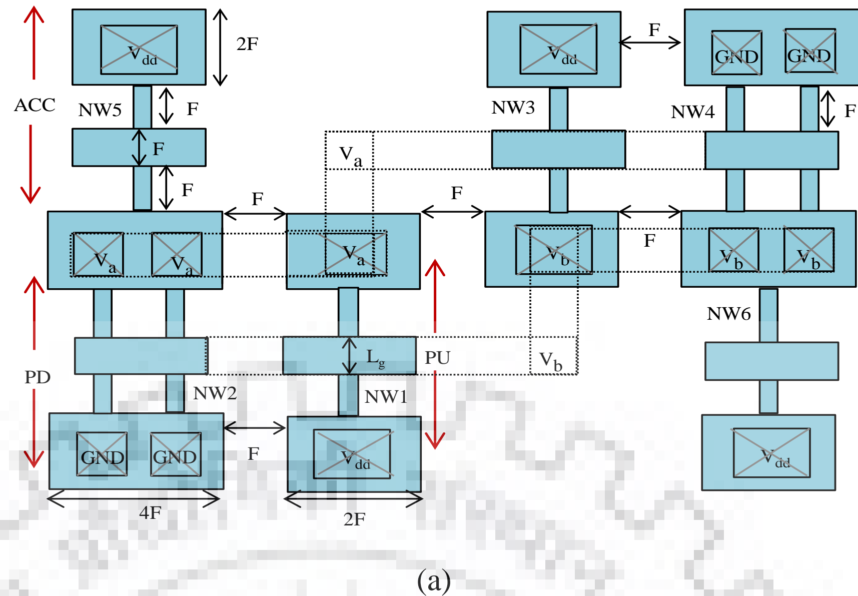


Figure 4.23 (a) Node voltages of WAT for '0' and '1' in C_111 configuration, (b) Write access time (WAT) of SiNW FET 6T SRAM cell in different configurations.

4.6 SRAM Cell Area Optimization

A top view of SiNW FET 6T SRAM cell layout area with 'F' as a minimum feature size (layout parameter) is shown in Figure 4.24(a). The height (H) of the cell is kept constant and width (W) is varied according to the number of wires used in PU, ACC, and PD transistor. Figure 4.24(a) shows the layout in C_112 configuration with a area of 12F×15F=180F^2 (Area = Length×Width). In Figure 4.24(b), 10 nm SRAM cell shows various design configurations such as C_111, C_112, C_113, C_123, C_124, and C_233. Out of all these configurations C_111is considered as a minimum size SRAM cell configuration with single wire used in PU, ACC and PD transistor. The C_111 configuration shows area saving of ~36 %, ~73 %, ~146 % and~109 %as compared to configuration C_112 , C_113 , C_123 , and C_233 respectively. Hence,SiNWFET multiwire sizing technique is employed to realize SRAM cells with better performance parameters (SNM, RNM, WNM etc.) and low area by using an appropriate number of wires in PU, ACC, and PD transistor as a design configuration.



(a)

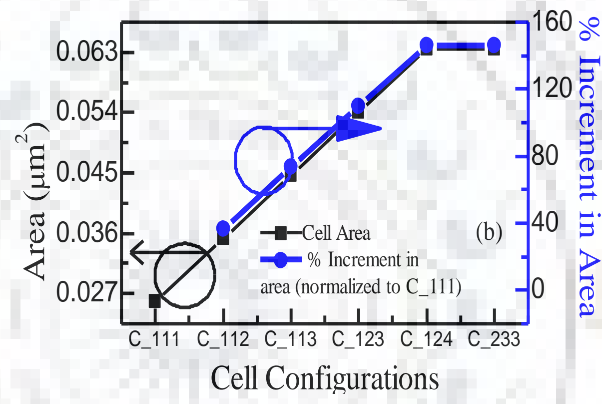


Figure 4.24 (a) Layout of 6T SRAM cell in C_112 configuration corresponding to, (b) layout area and comparison in various configurations.

4.7 SiNW SRAM Variability Analysis

We demonstrate the applicability of unified Verilog-A compact model described in chapter 3 to investigate the effect of device geometry dependent process variability on the stability of 6T SRAM cell. The compact model is calibrated for the variability analysis by TCAD simulations of SiNW FET with ±15 % variation in the channel length, radius and oxide thickness. One thousand Monte Carlo (MC) simulation by HSPICE has been performed to investigate the impact of geometry dependent process variation on the stability of the 6T SRAM cell. We assume that the device parameters such as radius, channel length, and oxide thickness of a nanowire for MC simulations vary by ±15 % in the range of 3σ spread [125], [19].

In the short channel SiNW FET device, the channel length becomes a significant source of variation which induces a change in threshold voltage due to drain induce barrier lowering

(DIBL)[126]. Unlike, planar and FinFET devices in which oxide thickness (t_{ox}) is strongly controls on drive current and capacitance. In the case of SiNW FET the oxide thickness is the logarithmic dependence of oxide capacitance due to the cylindrical structure, hence causes a negligible change in drive current due to oxide thickness variation [19]. Further, the variation in the radius of a SiNW FET becomes a critical issue and its impact on the drive current is strong compared to the other parameters. Equation (4.3) shows the threshold voltage shift (ΔV_{th}) dependence on the channel length, radius, and oxide thickness to SiNW FET.

The $\Delta V_{th,SCE}$ is a shift in threshold voltage produced due to SCE [40].

$$\Delta V_{th,SCE} = f_{SCE}[2(V_{th,long} - Q_{dep} - V_{bi}) - V_{ds}] \quad (4.3)$$

where f_{SCE} is the SCE factor which depends on the channel length and minimum feature size (λ), $\Delta V_{th,long}$ is the threshold voltage of long channel device, Q_{dep} is the depletion charge, V_{bi} and V_{ds} are built-in and drain/source voltages. The minimum feature size (λ) is dependent on the radius (R) and effective oxide thickness [40].

We employ the N-curve method to investigate the effect of device geometry dependent process induced variability on the static read and write stability of SiNW FET SRAM Cell in different design configurations. The N-curve is the simple method to provide both current and voltage information to characterize the read, write SRAM stability. Figure 4.25 shows the N-curve, which monitors the current to external source applied into Q (or QB) node, while voltage V(Q) is swept keeping BL, BLB, and WL at supply voltage. The three intercept points A, B, and C on N-curve, where current is zero corresponds to the two stable point (A, C) and one metastable (B) point of the butterfly curve (Figure 4.19(b)) of the read SNM. The intercept point A is related to the ACC and PD transistors, while intercept point B relates to the PD and PU relative strength.

The voltage difference between the first two intercept points A and B are interpreted as the maximum tolerable DC noise voltage at the storage node Q of the cell before the stored data of the cell is flipped during the read operation. This voltage difference is defined as a static voltage noise margin (SVNM). The peak current between intercept points A and B, effectively measures the maximum acceptable DC current injected into the storage node of an SRAM cell without disturbing its data, indicated as a static current noise margin (SINM).

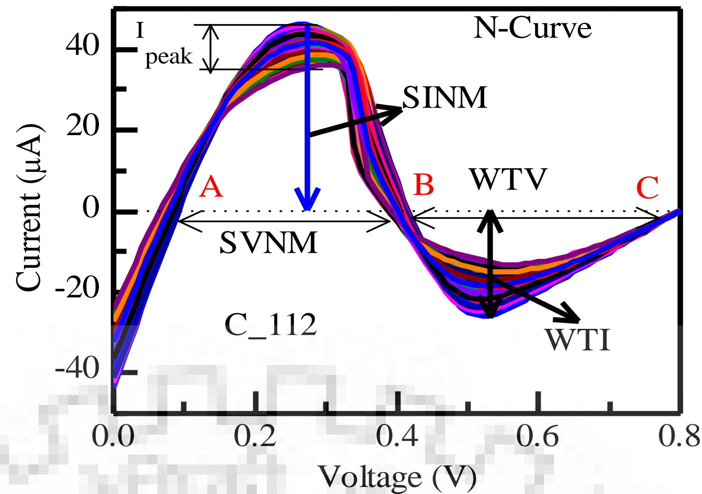


Figure 4.25 The N-curve characteristic in configuration C_112 under geometrical variation.

In addition to these parameters SVNM, SINM, the write trip voltage (WTV), and write trip current (WTI) of the cell need to be measured during the write operation of SRAM characterization. The WTV is the voltage difference (between C and B in N-curve) needed to flip the cell content. Similarly, N-curve also gives the information about the write trip current (negative peak current between C and B) which is required to write the cell, when both the bit lines are kept at supply voltage [119], [127], [128]. Using the above approach we investigate the impact of geometrical process variations on the SRAM cell stability metrics by considering different SRAM configuration, such as C_111, C_112, C_113, and C_123. A variation ±15 % in channel length, radius and oxide thickness of SiNW FET to study the effect of variability on an SRAM cell is considered.

4.7.1 Impact of Variability on Read and Write Stability

Figure 4.26 shows the normality plot to analyze the SVNM, SINM, WTV, and WTI variability at supply voltage 0.8V for four different SRAM design configurations: C_111, C_112, C_113, and C_123. All the stability metrics such as SVNM, SINM etc. are normalized by their mean values. Figure 4.26 (a-b) shows the normality plot of SVNM and SINM in four different configurations. The configurations C_111, C_112, and C_113 show a good normality for SVNM upto ±3σ distribution. However, in case of C_123 there is a good normal distribution at the center, but the lower and upper tails are deviated above and below ±3σ. A measured SVNM shows no significant variation (σ/μ) (~1 % to 1.4 % based on design configuration) from the normal distribution. For SINM, configuration C_113 shows the higher variation ~5 % and C_123 has lower variation of 2.57 % (But the lower tail has deviated from the normal curve). Other configurations such as C_111 and C_112 shows good normality, less

deviation, and variability.

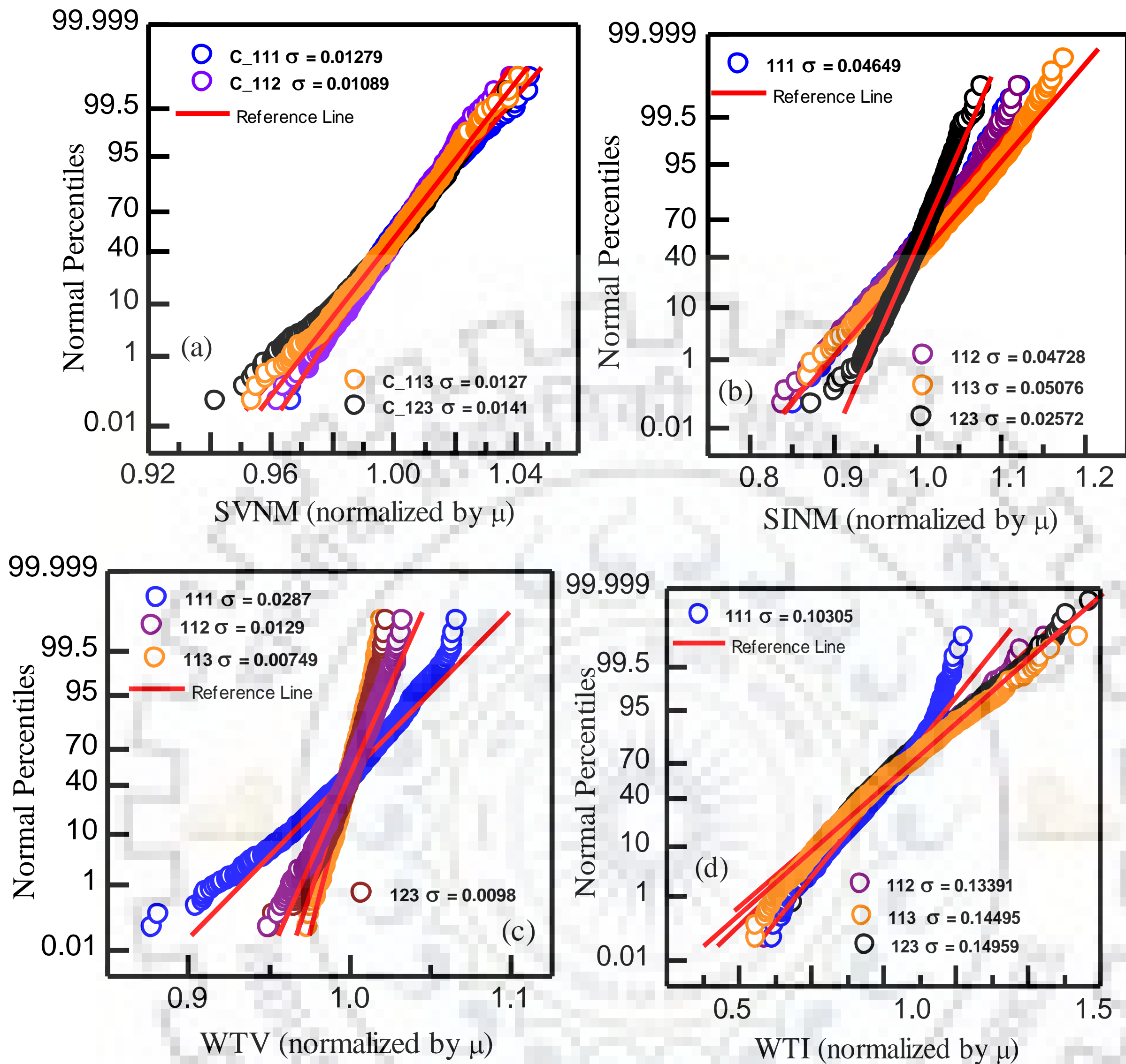


Figure 4.26 Normality plot of (a) SVNM, (b) SINM, (c) WTV, and (d) WTI for different configuration normalized by the mean.

Figure 4.26 (c-d) shows the normal probability plot of the WTV and WTI in various design configurations at supply voltage 0.8V. The configurations C_112, C_113,and C_123 exhibit a good normal distribution for WTV and very less sensitive to variability (σ/μ) of values 1.29 %, 0.749 % and 0.98 %, respectively. However, the minimum area configuration, C_111 shows a slightly larger variation (2.8 %) and longer tail away from the normal distribution in WTV from above and below ±3σ range. This longer lower tail may leads to the write failure. The WTI variability is highly sensitive to design configuration as shown in Figure 4.26(d). The minimum area configuration C_111 possess less variability of 10.8 % and other configuration, such as C_112, C_113 and C_123exhibits 13.39 %, 14.49 % and 14.95 % respectively. Finally, it is concluded that, the read, write voltage margin is less sensitive to variability compare to read

and write current margin in various SRAM cell design configuration. Since, SiNW FET current drive strength is strongly dependent on the diameter and number of wires used (by increase of two and three wires, the current also increase approximately twice and thrice).

4.7.2 Effect of Voltage Scaling on the Variability of SRAM Cell Performance

We analyzed the impact of supply voltage scaling on the read and write variability of the SRAM cell. Figure 4.27 shows the effect of supply voltage scaling from 0.8V to 0.4V on the SVNM, SINM, WTV and WTI stability of an SRAM cells in various configurations. At the nominal supply voltage of 0.8 V, all these metrics are of good normality of ±3σ and nearly linear dependence on the threshold voltage of the pass gate transistor operating in saturation and pull down operating in the linear mode. As the supply voltage drops to 0.4 V variation range increases and the pass gate transistors (NW5, NW6) are no longer in saturation. While pull down transistors (NW2, NW4) enter in saturation mode. Hence, SINM is linearly dependent on the V_{th} of PD and ACC. As shown in Figure 4.27, the voltage noise margins are less susceptible to variability ~2 % for SVNM and ~5 % for WTV depending upon the configuration. On the other hand, read and write static current margin are severely affected by supply voltage scaling. Depending upon the design configuration SINM exhibits ~18 % and WTI shows more than 30 % variability.

The read and write current noise margins vary ~18 % and ~35 % at scaled supply voltage of 0.4 V. Moreover, by employing appropriate SRAM cell design configuration, we can reduce read current variability from ~18 % to ~16 % and write current variability from ~35 % (C_111) to ~30 % (in C_112, C_113, and C_123). Furthermore, by increasing supply voltage, the read and write current noise reduces ~2 % and ~10 % (at a supply voltage of 0.8 V) respectively. The minimum area SRAM cell configuration C_111 shows a significantly larger variation (current and voltage stability) with voltage scaling compared to C_123 (with the penalty of ~80 % more layout area). In conclusion, the SiNW FET based SRAM cell design configurations follow the pelgrom's law of scaling 1/sqrt (W×L) (clearly shown in Figure 4.27).

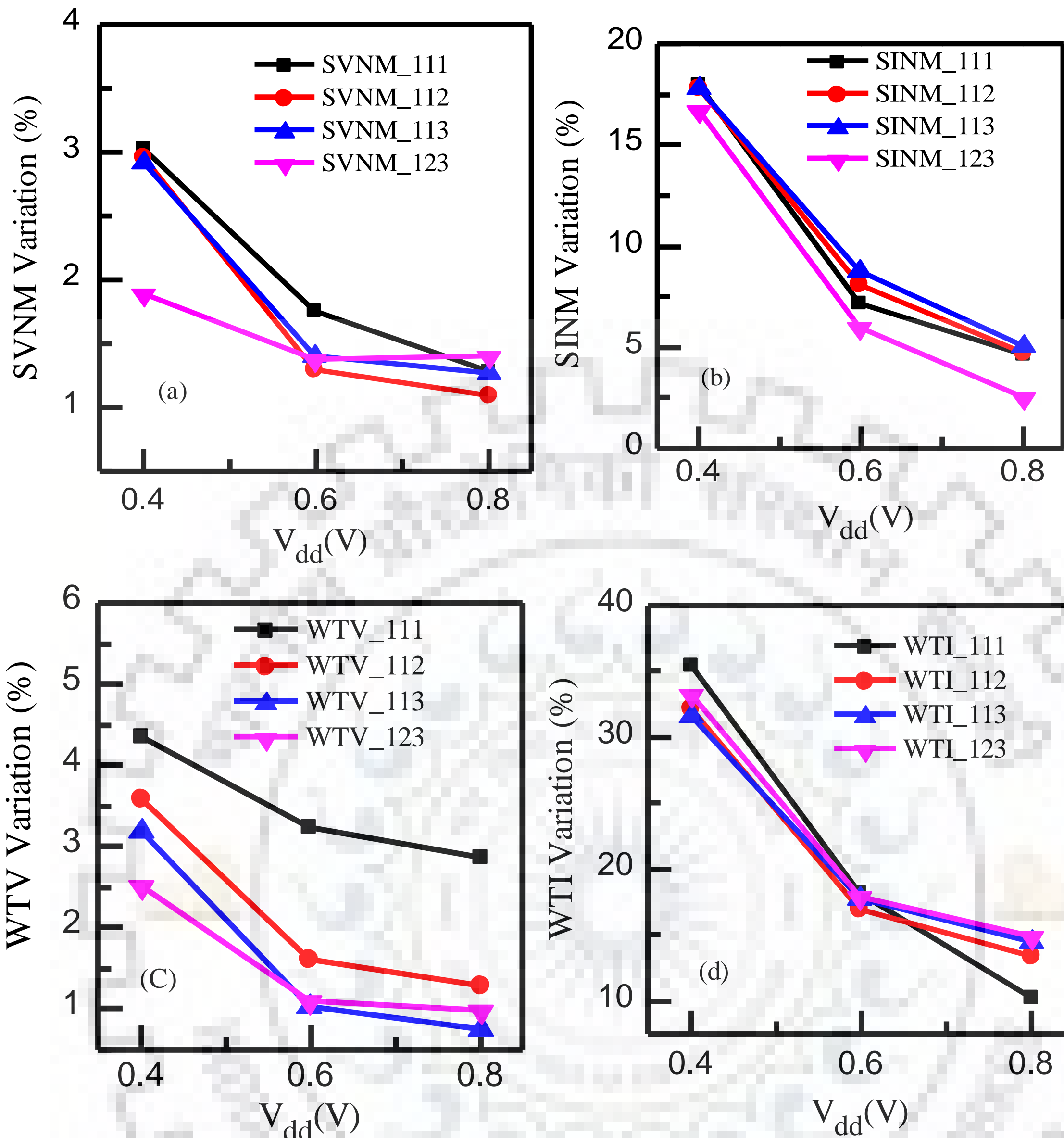


Figure 4.27 Effect of supply voltage scaling on the (a) SVNM, (b) SINM, (c) WTV, and (d) WTI due to geometrical variability.

As expected, the standard deviation in read/write stability is inversely proportional to the cell area. Therefore, C_123 possess a slightly smaller variation compared to other design configurations as shown in Figure 4.27. The variation difference (σ) among the various SiNW FET SRAM cell design configurations is small ~2 to 3 % (Figure 4.26/4.27). However, the mean (μ) value of noise margin is strongly SRAM cell configuration dependent. This can be clearly seen in Figure 4.20 (a) from the absolute value of read noise margin. The C_112 configuration has ~35 % (51mV) higher value of read noise margin compared to C_123 configurations. On other hand, C_113 has slightly better read noise mean values, but there is a large area penalty compared to C_112 configuration. Hence, it is possible to achieve a better SRAM cell design with a high mean value of noise margin and yield compared to large area

design (C_123). Similarly, for write margin (Figure 4.26 (c-d)), the mean of C_123 configuration is slightly better than C_112 configuration but at the penalty of the large layout area. The higher mean value of noise margins gives higher variation tolerance. Therefore, the C_112 configuration has higher process variation tolerance and less area penalty compared to C_113and C_123. The similar trend of variability is also shown in FinFET based SRAM cell design [4]. Moreover, from our analysis, it is also found that the larger area configurations C_123 possess a longer tail (upper and lower), and also the deviation from the mean (As shown in the normality curve Figure 4.26).

4.8 Summary

This chapter can be summarized as:

1. The energy efficient NW FET based core logic gates such as INVERTER, NAND, NOR, XOR and XNOR have been designed using mulwire sizing technique. We found that the SiNW FET based logic gates achieves low (PDP) average (EDP) compared to FinFET based design.
2. The published experimental and TCAD calibrated Verilog-A compact model with parasitics has been utilized to design and investigate the SiNW FET based 6T SRAM cell. The read, write noise margin and access time of SiNW based SRAM cells using themultiwire sizing technique are investigated by considering various configurations such as C_111, C_112, C_113, C_124, C_123, and C_233.
3. In addition, the impact of geometry dependent process induced variability such as channel length, radius and oxide thickness on the read, write stability of SRAM in different design configuration is analyzed. We find that geometrical variability is extremely influenced by read current noise margin by ~5 %, and write trip current ~15 % depending upon the configuration. Whereas, the static read voltage noise margin and write trip voltage are lower affected by variability ~2 % at supply voltage.
4. Further, we have investigated the effect of supply voltage scaling on the variability of the SRAM cell. From our analysis, it is found that among all design configurations, C_112 is the better configuration for considering the overall performance such as RNM, WNM, RAT, WAT, layout area, and variability tolerant.

5 CHAPTER

Silicon Nanowire CMOS BTI Modeling

5.1 Introduction

SiNW FET is a potential candidate in sub-10 nm technology nodes, which prominently overcomes the issues such as short channel effect, poor gate controllability, high leakage current, low I_{ON}/I_{OFF} ratio caused by miniaturization of MOSFETs [23], [129]. However, apart from the issues due to scaling, bias temperature instability (BTI) reliability have become major challenges in 3D devices such as FinFET[130] and SiNW FET [30], [19]. Bias Temperature Instability (BTI) includes negative bias temperature instability (NBTI) and positive bias temperature instability (PBTI) which occurs in p and n type MOS devices respectively [27], [131], [132]. The impact of BTI induces an unwanted shift in the threshold voltage (V_T) of the device, thus, degraded the ON current. In this chapter we measure NBTI/PBTI reliability of NW p-FET/n-FET fabricated using top-down CMOS process [129]. We experimentally characterize NBTI/PBTI on SiNW device having SiO_2 gate oxide for a wide range of stress voltage, temperature, time and extracted model parameters. The experiment were performed under two condition i) in the first case, we kept the oxide field constatnt by keeping constant gate stress voltage and varied the device temperature, ii) in the second case, we kept the temperature constant and varied the gate oxide field for a wide range. Further, we have investigated and developed the SiNW FET BTI stress and recovery threshold voltage predictive model. Finally, we integrated BTI threshold voltage and mobility degradation model in SiNW FET Verilog-A compact model to investigate the impact of BTI on circuit performance.

5.2 Negative Bias Temperature Instability in pSiNW FET

5.2.1 Device Structure and Experimental Setup

The stress experiments are performed on p-SiNW FET devices. The devices used in the study were fabricated using top-down CMOS fabrication process having self-limiting oxidation process for nanowire formation [9]. The devices have p+ poly gate with gate oxide thickness t_{ox} of 3.5 nm, channel length (L_g) of 400 nm$-$750nm and diameter (D)15 nm. Figure 5.1 shows the cross-sectional view of SiNWFET with interface trap charges. The NBTI for p-

SiNW FETs is measured using conventional stress-measure technique employing Keithley 4200 semiconductor characterization system (SCS) which is equipped with self programmed KITE software. KITE software is capable for various types of electrical characterization such as precision DC current-voltage (I-V), AC impedence, and pulse or transisent current-voltage (Ultra fast I-V). The Keithley 4200 SCS is connected through cable with 4 probe station for device under test. In 4 probe station, three probes are connected to source, drain, gate and 4th probe kept common dring measurement. The time varying stress experiments are performed at a different temperature and gate stress voltages through self programmed KITE. The model parameters are extracted from long time stress values.

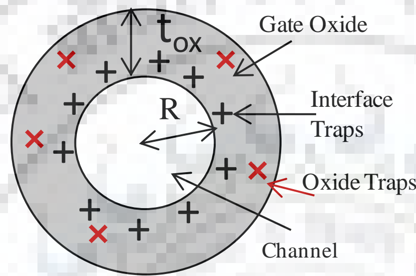


Figure 5.1 Cross sectional view of SiNW FET channel showing interface traps.

5.2.2 Model Description during Stress Phase

The NBTI threshold voltage model depends on conditions such as stress time, operating temperature and applied vertical gate electric field at which devices are stressed. Figure 5.2(a) shows variation of the threshold voltage with stress time at different gate bias.

The degradation in threshold voltage due to the interface trapped charges (ΔN_{it}) can be expressed as

$$\Delta V_T = C_1 t^n \tag{5.1}$$

where C_1 is a constant, t is the stress time and exponent "n" is the signature of diffusing species in Reaction-Diffusion model [59]. Initially, there is a significant degradation, which can be attributed to larger electric field due to cylindrical gate structure resulting in enhanced H_2 and diffuse away from interface, and more trapping in stress induced defects in gate insulator [76]. The slope indicated in Figure 5.2(a) gives the value of time exponent n≈0.168.

The oxide electric field is an important factor contributing to enhancement of NBTI in SiNW FET. The curvature of concentric cylindrical structure leads to accelerated large interface trap generation in 2D mode. The field dependence of NBTI arises due to the electro-chemical nature of the NBTI reaction [133]. As the diffusing elements H/H_2 are charge neutral, thus the effect

of electric field will appear only near Si/SiO_2 interface region. Figure 5.2(b) shows measured data of exponential relation between stress field (E_{ox}) [134] and ΔV_T. The field dependent shift in threshold voltage is modelled as:

$$\Delta V_T = C_2 e^{\beta E_{ox}} \tag{5.2}$$

$$E_{ox} = \frac{(V_g - V_{th})}{R \ln\left(1 + \frac{t_{ox}}{R}\right)} \tag{5.3}$$

where C_2 ans $\beta$are a constant, V_g and V_{th} are the applied gate voltage and threshold voltage during strong inversion, R and t_{ox} are the NW radius and oxide thickness of a device, respectively.The threshold voltage shift $\Delta V_T$is a good approximation (β is a constant and E_{ox} is oxide field at the Si-SiO_2 interface) [58]-[135] for modelling field dependence of NBTI.

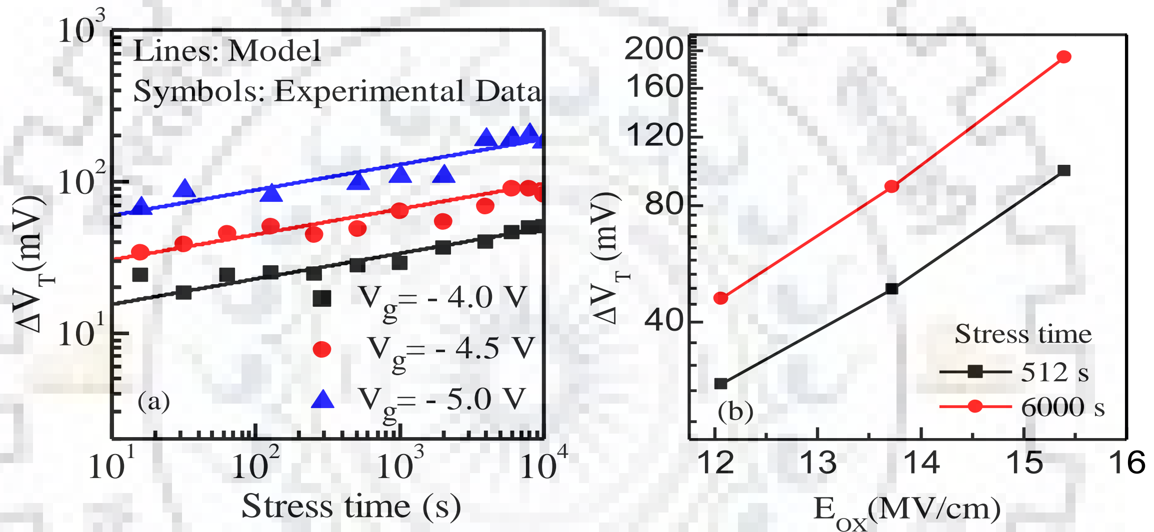


Figure 5.2(a) NBTI induced ΔV_T comparison between experimental and model equation, (b) ΔV_T versus oxide electric field at different stress time.

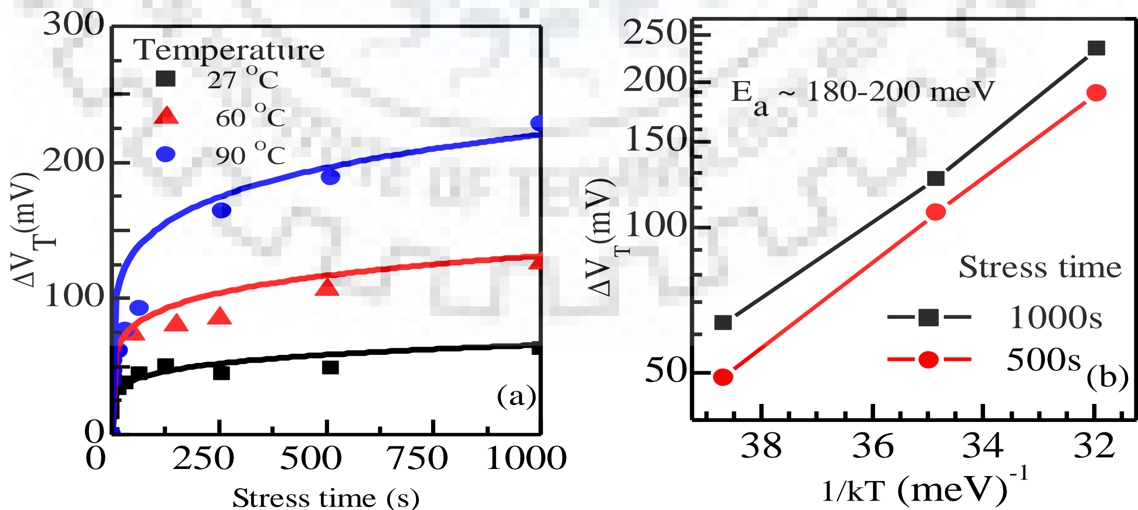


Figure 5.3 (a) NBTI induced ΔV_T comparison between experimental and model equation at different temperatures (for constant gate stress voltage of (Vgs=-4.5V), (b) shows the $E_a$value from the slope of ΔV_T and (1/kT).

In addition to the stress time and field dependence, the temperature also plays a key role in NBTI activation energy. Figure 5.3(a) shows the impact of temperature on the threshold voltage degradation. Figure 5.3(b) shows the Arrhenius T activation nature of NBTI. For Arrhenius T activation the temperature dependence of a shift in threshold voltage can be modeled as:

$$\Delta V_T = C_3 e^{-E_a/kT} \tag{5.4}$$

Where C_3 is a constant, E_a the activation energy, k is the Boltzmann constant and T is the temperature in Kelvin. The value of E_a is determined from the slope of curve shown in Figure 5.3(b) and extracted values are in the range of 180meV-200meV. The extracted values of E_a are consistent with experimentally reported values in literature [13].

The complete threshold voltage degradation model combing (5.1)-(5.4) is expressed as

$$\Delta V_T = A e^{\beta E_{ox}} e^{-E_a/kT} t^n \tag{5.5}$$

where A is a constant, it is expected that the parameters β and A include technology dependent effects such as gate dielectric, gate metal and other related processes. Figure 5.4(a) compares NBTI degradation of p-SiNW FET along with experimental bulk FinFETs and conventional planar MOSFETs [136]. To get fair comparison of different technologies, change in V_T is for plotted for oxide field as shown in Figure 5.4(b) for 500s and 1000s of stress. We see from Figure 5.4(b) that for same oxide field, planar MOSFETs has a lower degradation followed by FinFET, with SiNW FET being the highest. This can be attributed to: (i) lower vertical electric field (due to planar structure), (ii) lesser initial 1-D diffusion of hydrogen and lesser traps. Further, FinFETs show less threshold voltage degradation compared to SiNW FET at same the temperature (100°C) and oxide thickness due to the structural difference.

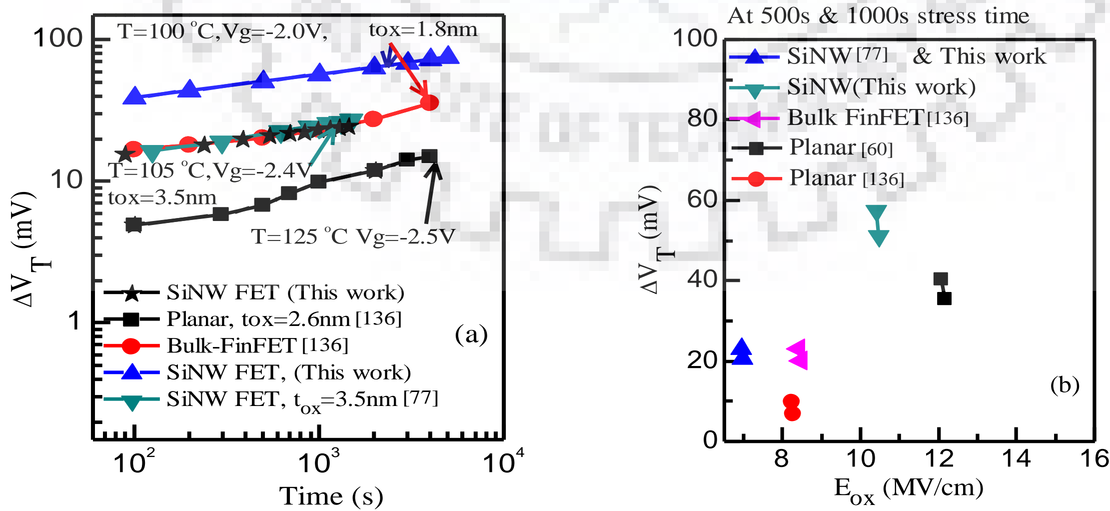


Figure 5.4 (a) NBTI benchmarking and comparison among different technologies: planar, FinFET and NW MOSFETs, (b) Oxide field comparisons of different technologies.

Table 5.1 NBTI model parameter values.

A	β (V/m)$^{-1}$	E_a(meV)	n
83.5	4.05x10^{-9}	180	0.168

Cylindrical structure NW FETs are more susceptible to NBTI reliability due to its cylindrical structure leading to: i) increased 2D hydrogen diffusion during NBTI stress compared to 1D diffusion in traditional planar devices, ii) significant enhancement of gate electric field due to the larger curvature, resulting in larger trap generation in gate dielectric, iii) stress induced defects in cylindrical gate oxide during the fabrication process causing larger oxide charge trapping during NBTI stress [75]-[30]. The NBTI degradation obtained from our model with a same oxide thickness (field) and temperature, as earlier published SiNW FET threshold voltage data [76] compares well, which demonstrate the accuracy and scalability of our model. The model parameters obtained from the stress experiments are listed in Table 5.1.

5.3 SiNW FET NBTI Recovery Modeling

The threshold voltage degradation due to NBTI starts to recover after stress is removed [137]. Therefore, neglecting stress recovery would result in underestimation of a device lifetime. During stress period threshold voltage increases due to degradation and decreases during a recovery period because hydrogen atoms diffuse back to the interface again [138]. The recovery response to stress is an important aspect of NBTI as continuous DC stress is rarely seen in real applications. Figure 5.5 shows temperature dependent NBTI recovery behavior for devices used in this work. In [139], [137] authors presented a stress recovery model which is given as

$$\Delta V_{thr}(t) = \Delta V_{tho} \times (1 - \alpha(t - t_o)^n) \tag{5.6}$$

where, $\Delta V_{thr}(t)$ is the degradation at time t, ΔV_{th_o} is the degradation at the end of stress period or at the beginning of recovery period, t_o is stress period, α is the proportionality constant (dependent on temperature), and n is the time exponent expressed in (5.1). Figure 5.5 shows the threshold voltage shift during stress and recovery time at constant voltage and different temperature. The value of α is determined by substituting all other parameters in the recovery threshold voltage model equation (5.6). The all other parameters value such as ΔV_{thr}(t), ΔV_{tho} and n are extracted from the experiments.

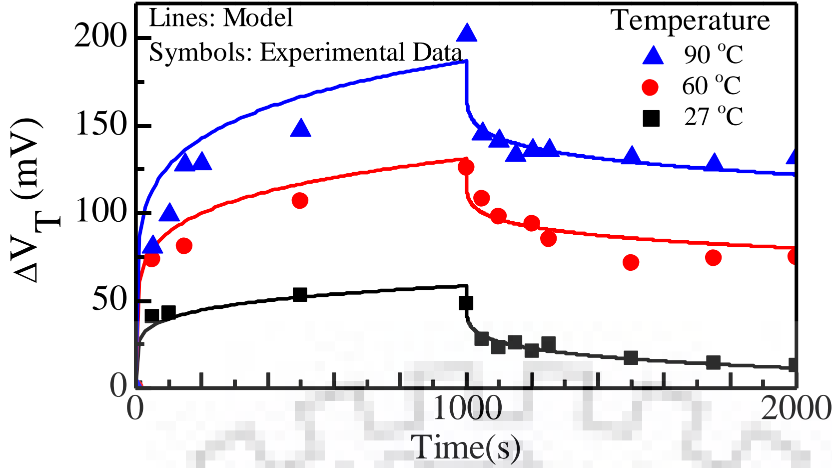


Figure 5.5 Shows the threshold voltage degradation for dynamic NBTI (Stress VoltageVgs=-4.5V) at various temperature, and comparison between experimental data and model.

Figure 5.5 also shows the comparison of experimental, and predicted model using (5.5) and (5.6) for stress and recovery for p-SiNW FET in which DC stress is applied for 1000 *s* and then V_g positive value is applied for next 1000 *s* at three different temperatures.

5.4 Integrated NBTI Model for NW Circuit Simulation

In the previous section, we presented separate stress and recovery models. However, in practical circuit operations, long term degradation model, which include both stress and recovery according to the input signal (e.g. duty cycle) is required. Figure 5.6 shows the stress and recovery cycle for N number of periods of digital signal. During the 1st stress phase ΔV_T increases with time and is modeled as $\Delta V_{ths} = Kt^n$ (obtained from DC stress), where K includes the field and temperature dependent parameters, whereas in recovery phase, ΔV_T decreases and is modeled as $\Delta V_{thr} = \Delta V_{ths,t_o}(1 - \alpha(t - t_o)^n$ from recovery model, where $\Delta V_{ths,t_o}$ is the threshold voltage degradation at the end of stress phase and t_o represent the stress time period. The shift in the threshold voltage after cycle, which includes both stress and recovery depends upon the previous cycle threshold voltage [64]. Hence, the iterative method for stress and recovery is used to predict threshold voltage for long duration, which is clock period and duty cycle dependent. The threshold voltage degradation at the end of stress phase of the Nth cycle can be expressed as

$$\Delta V_{ths}(N) = K\left[\left(\frac{\Delta V_{th}^{N-1}}{K}\right)^{1/n} + gT_{CLK}\right]^n \tag{5.7}$$

where K is the stress voltage and temperature dependent parameter, g is the duty cycle, and T_{CLK} is the clock period.

Threshold voltage after recovery in N^{th} cycle can be expressed as

$$\Delta V_{thr}(N) = \Delta V_{ths}(N)[1 - \alpha[(1 - g)T_{CLK}]^n] \tag{5.8}$$

Where $\Delta V_{ths}(N)$ is the net threshold voltage degradation at the end of the stress phase of Nth cycle and α is the recovery factor. Therefore, employing an iterative process of stress and recovery in Eq. (5.7-5.8), we can predict the net degradation in threshold voltage for any number of cycles with any duty cycle. The result of DC vs AC prediction using the above approach is shown in Figure 5.7(a) for different duty cycles. We observe that after a large number of cycles AC stress tend to asymptotically follow the same power law (n=1/6) with time as DC stress.

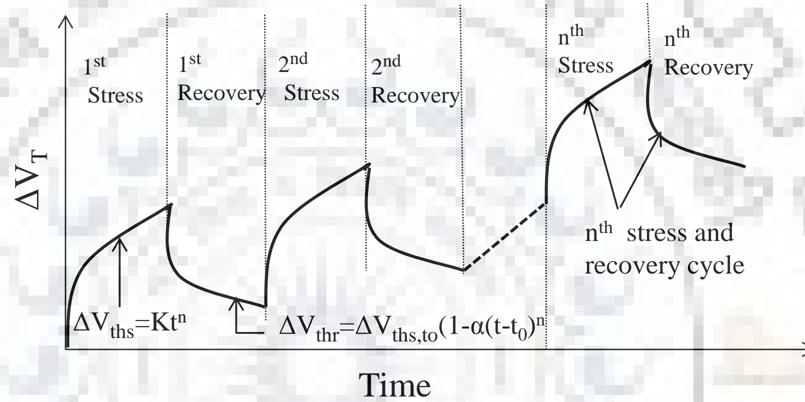


Figure 5.6 Schematic diagram for an estimation of ΔV_T during AC Stress.

Due to extremely large number of computations, it is impractical to run cycle to cycle simulation for long time prediction (e.g. 3 to 10 years) of circuit performance. We use method investigated in [140], in which NBTI degradation can be represented as being asymptotically equal to the γ times DC NBTI degradation.The degradation ratio is denoted by γ shown in Figure 5.7(b),

$$\Delta V_T(AC) = \gamma \Delta V_T(DC) \tag{5.9}$$

where γ is the scaling factor, which depends on the duty cycle of the signal. Figure 5.7(b) shows the value of γ, which is independent of frequency as verified for a wide range of frequency range (1 kHz to 10GHz).

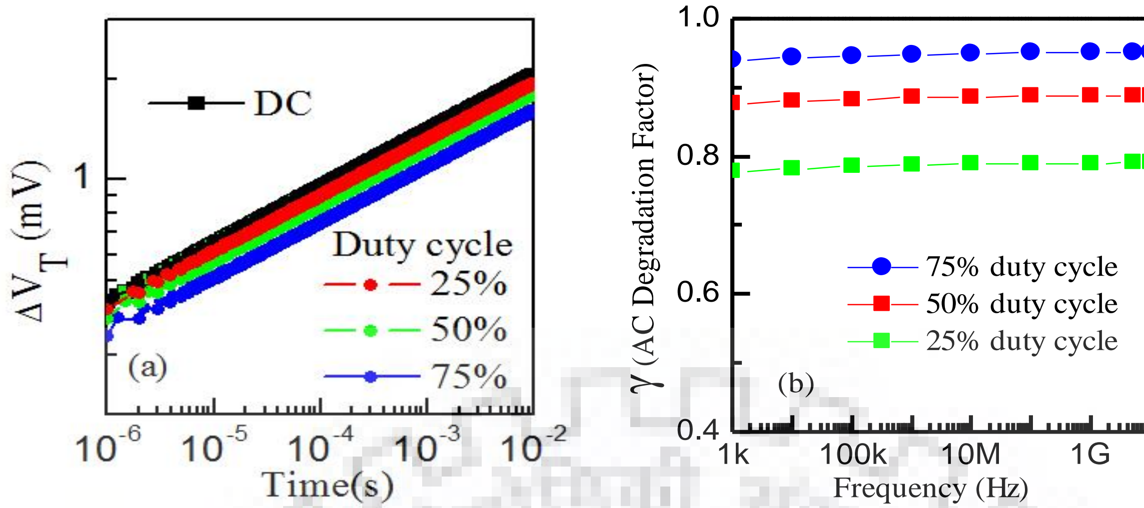


Figure 5.7 (a) NBTI degradation for DC and AC stress under different duty cycles, (b) Show the asymptotic ratio of AC to DC (γ) degradation with frequency.

5.5 Positive Bias Temperature Instability (PBTI) in nSiNW FET

Positive bias temperature instability (PBTI) has an important reliability concern for n-MOS FET devices in an ultra scaled transistor which degraded the threshold voltage and reduced current strength. The shift in V_T due to PBTI in n-MOSFETS FET with stress voltage, temperature and stress time is due to (i) electron tunneling and trapping into the pre-existing oxide traps, (ii) newly generated traps in bulk oxide due to high oxide field [28], (iii) stress induced defects in gate oxide during the fabrication process causing larger oxide charge trapping.

5.5.1 Model Description of n-SiNW FET during Stress Phase

The n-SiNW FET devices have been characterized for a wide range of stress voltage, temperature and stress time. In our measurement, we have first stressed the nSiNW FET at different gate voltages +4.0 V, +4.0 V, and +5.0 V at room temperature for longer stress time (~10000 sec) and measured the threshold voltage. Fig. 5.8 shows the shift in threshold voltage with stress time at different stress voltages. The shift in threshold voltage has been measured from the shift in the slop of the transfer characteristic due to the applied stress voltage. The shift in the threshold voltage is attributed to (i) electron tunneling and trapping into the pre-existing oxide traps, (ii) newly generated traps in bulk oxide due to high oxide field, (iii) generation of acceptor type traps causing positive V_T shift [28]. Since due to the cylindrical gate structure of SiNW FET, it possess a larger gate area and multiple crystallographic orientations (100, 110, 111 etc.) of gate oxide causes more traps formation and electron trapping [76].

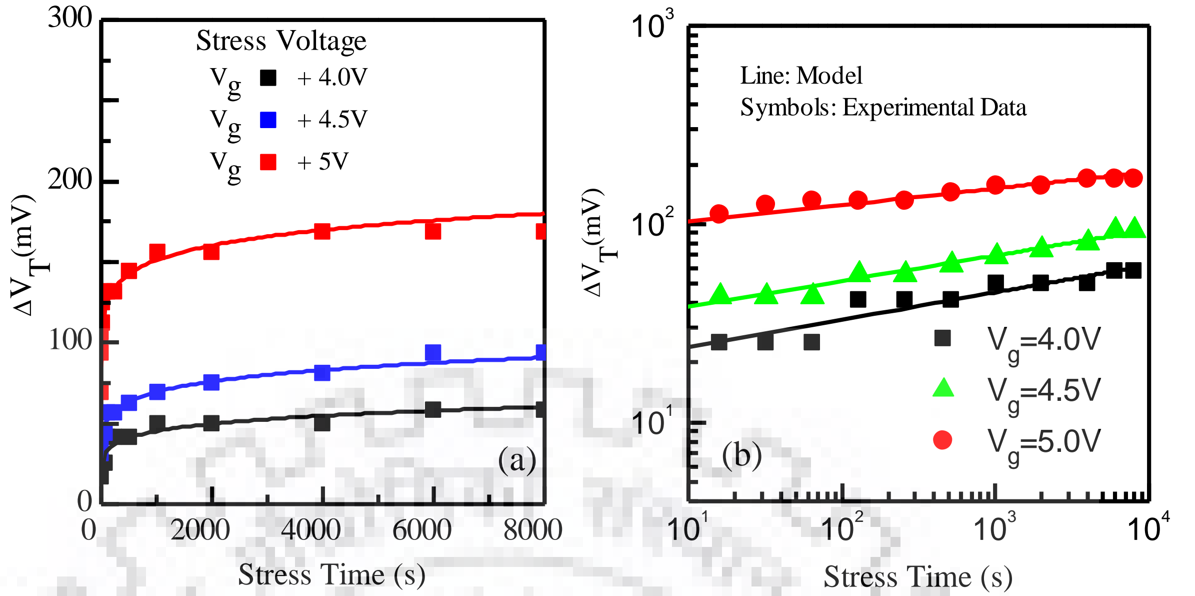


Figure 5.8 Threshold voltage shift under the influence of positive gate stress (n-SiNW FET) in (a) Linear, (b) log plot.

A generic NW V_T model PBTI under the DC stress is described by the power law framework [62] modeled by

$$\Delta V_T = C e^{\beta E_{ox}} e^{-E_a/kT} t^n \tag{5.10}$$

where C and β are dependent on process parameters such as gate dielectric, gate metal, and other process associated parameters. The parameters E_a, k and T denote the activation energy, Boltzmann constant and temperature respectively. These, threshold voltage model parameters, due to PBTI are extracted in similar ways as NBTI (In section 5.2). Figure 5.8(a-b) shows the good agreement between model and characterized data for PBTI.

Figure 5.9 compares the NW V_T degradation due to PBTI/NBTI with the published experimental planar MOSFETs [141], [136] and FinFET[142], [136] data. Figure 5.9 shows that the NW PBTI degradation is higher than the planar MOSFET due to high oxide field. Further, the lower degradation in NW FET is attributed to SiO_2 gate oxide of fewer traps, consequently less trapping compared to FinFET with high-k gate dielectric. Table 5.2 shows the NBTI/PBTI model parameters extracted from the stress experiments. These extracted parameters are consistent with experimentally reported values in [135], [141].

Table 5.2 NBTI/PBTI model parameters value.

	$\beta (V/m)^{-1}$	**E_a(meV)**	**n**
NBTI	4.05e-9	180	0.168
PBTI	3.5e-9	246	0.12

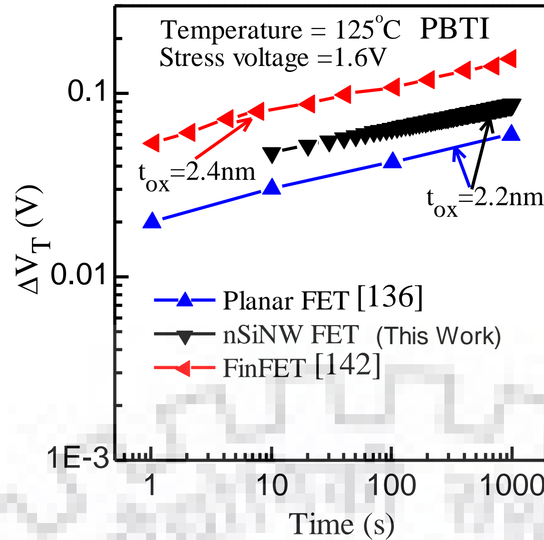


Figure 5.9 Shows the comparison of threshold voltage shift due to PBTI among nSiNW FET, planar MOSFETs and FinFET technology.

5.6 Compact Model Incorporating BTI for Circuit Simulation

5.6.1 NBTI Model Incorporation for 10 nmSiNW FET Circuit Simulation

The BTI model found from fabricated devices in section 5.2 and 5.5, is scaled to nanoscale NW FET using model scalable parameters [143], [138]. In order to utilize threshold voltage degradation model for lower technology node, we modify electric field E_{ox} (which depends upon oxide thickness and radius of the device), gate voltage V_g and temperature T, whereas other model parameters given in Table 5.2 are kept constants.

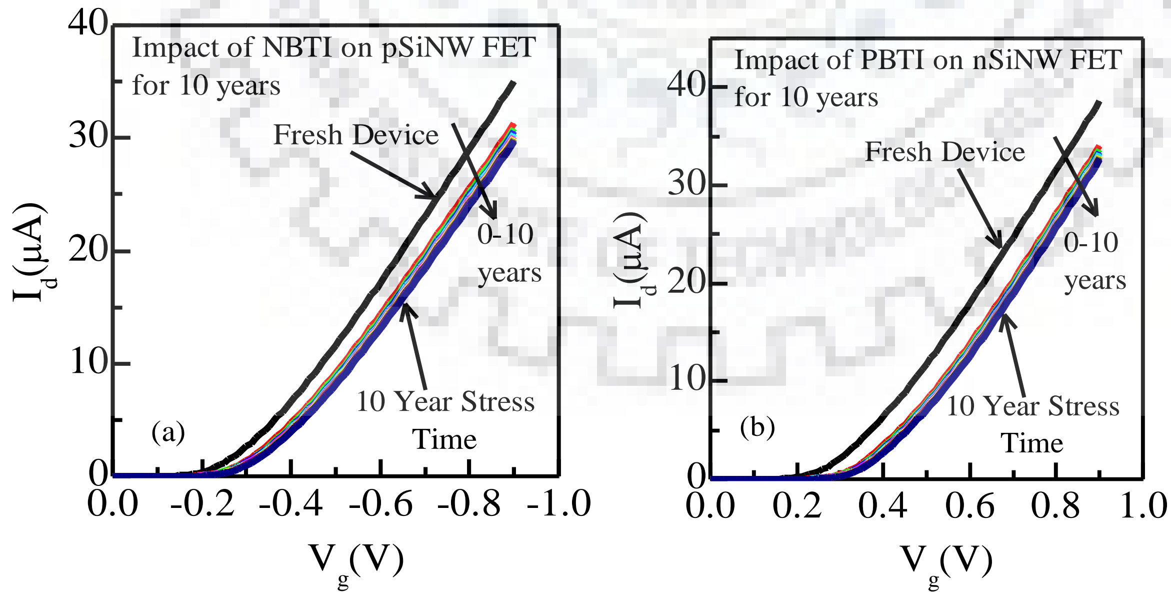


Figure 5.10 (a-b) Shows the shift in the I_d-V_g characteristics on NW device under the influence of NBTI and PBTI respectively.

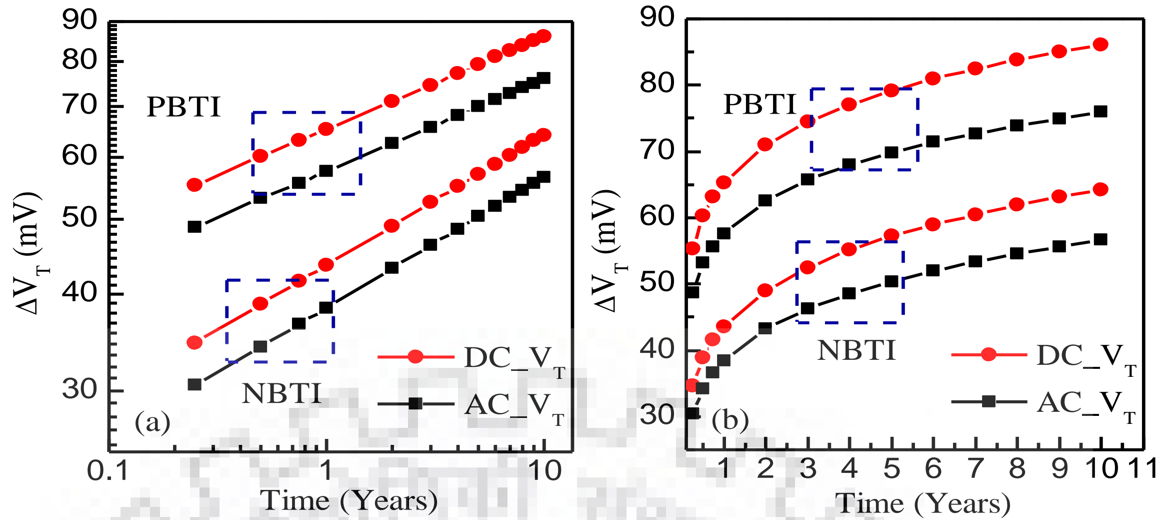


Figure 5.11 Shows the DC and AC V_T degradation due to NBTI/PBTI in (a) log, (b) linear scale for 10 year of life time.

Figure 5.10 (a-b) shows the device I_d-V_g characteristic before and after the stress due to NBTI and PBTI on 10 nmpSiNW FET and nSiNW FET devices respectively. This device characteristic prediction, demonstrating the model capability for NW based circuit design and analysis. Further, Figure 5.11 (a-b) show model predicted threshold voltage shift (in log and linear plot) due to DC and AC NBTI/PBTI model for 10 year lifetime for 10 nm NW PMOSFET, with channel length L_g=14 nm, radius R =5 nm, and oxide thickness t_{ox}=1 nm. In addition to the degradation in threshold voltage, the increase in interface trap charges also results in the degradation of carrier mobility. The mobility degradation factor can be express empirically as a function of interface trap density as [144]:

$$\mu_{deg} = \frac{\mu_{eff}}{1+\alpha_1 N_{it}} \tag{5.11}$$

where,

$$N_{it} = \frac{(\Delta V_T C_{ox})}{q} \tag{5.12}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{(R\ln(1+t_{ox}/R))} \tag{5.13}$$

α_1, is the degradation factor and its value from measurement is calculated as $0.1(10^{-11}\text{cm}^2)$, ΔV_T is the threshold voltage degradation, C_{ox} oxide capacitance and q is the electronic charge. The integrated NBTI model also incorporates mobility degradation as modeled by Eq. 5.11.

Figure 5.12 (a-b) shows the hierarchical framework and equivalent circuit schematic to integrate NBTI model for the circuit performance prediction. We begin with the calibrated current – voltage $(I - V)$ data of a fresh device at time t=0 s to prepare the nominal model card. Further, extract the threshold voltage for fresh and stressed device using the constant current

method. We extract the shift in V_T and mobility degradation factor (μ_{deg}) value for time $t > 0\ s$ from the developed threshold voltage and mobility degradation model of SiNW FET. Further the aged model card is generated using the combination of fresh and degraded threshold voltage and mobility model. With the help of aged model card and compact Verilog-A model, we write circuit netlist in HSPICE and simulate the circuit performance at any time. The complete BTI simulation flow is used to analyze the impact of BTI (NBTI+PBTI) on NW based circuits in the next chapter.

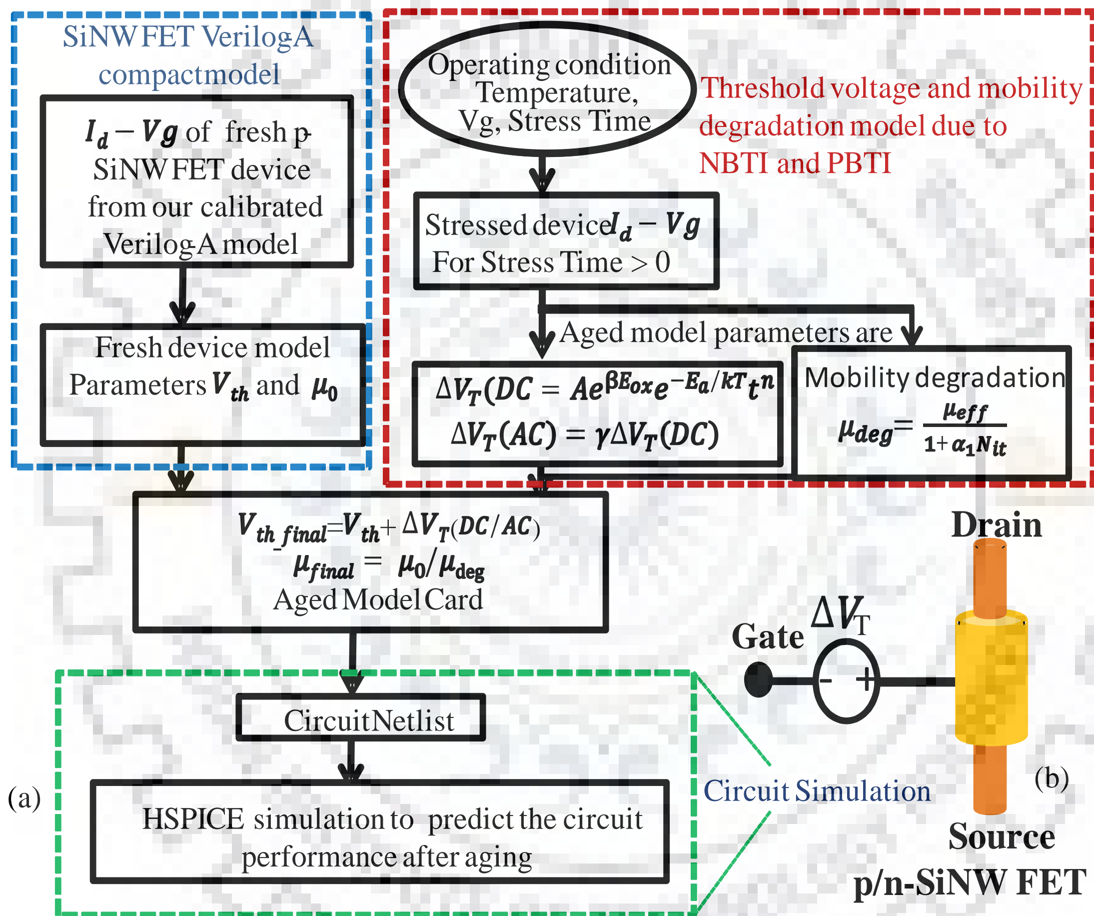


Figure 5.12 (a) Overview of the simulation flow for the prediction of circuit performance degradation due to BTI, (b) p/n-SiNW FET BTI equivalent circuit.

5.7 Summary

This chapter can be summarized as:

1. The p-SiNW FET threshold voltage NBTI model during stress and recovery phase has been obtained from the experimentally measured data.
2. The n-SiNW FET threshold voltage PBTI model during stress phase has been obtained from the experimentally measured data.
3. Presented a flow chart to incorporate the BTI (NBTI+PBTI) reliability model in Verilog-A compact model for NW CMOS circuit design and analysis.

6 CHAPTER

Impact of BTI Reliability on NW Circuits

6.1 Introduction

In the previous chapter, we have developed a comprehensive framework in which a NW BTI reliability model is integrated intoVerilog-A compact model for circuit analysis. In this chapter, we analyze the impact of BTI (NBTI+PBTI) reliability and time zero variability on the basic logic gates and 6T SRAM cell. First, the impact of NBTI on SiNW FET based inverter delay degradation and 13-stage ring oscillator (RO) frequency degradation for 10 year lifetime is investigated. Further, we have designed a SiNW FET based SRAM cell and discussed NBTI impact on SRAM cell performance. The multiwire sizing technique has been employed to design a NW based 6T SRAM cell in different design configurations. We have investigated the impact of NBTI on the static and dynamic stability of SRAM cell by considering various design configurations such as C_111, C_112, C_113, C_123, and C_122 (e.g. configuration C_112 denotes the number of wires in pull up, access and pull down transistor respectively). Thereafter, we investigate the impact of BTI (NBTI+PBTI) on propagation the delay of logic gates such as Inverter, NAND, NOR, and SRAM cell read/write stability. Further, SRAM cells read stability under the combined effect of BTI and time zero variability in three different cell design configuration such as C_111, C_112, C_123 is studied. Finally, it is shown that with suitable SRAM cell design configuration the reliability and variability tolerable circuits can be designed.

6.2 Impact of NBTI on NW Circuit Performance

In this section, we investigate the impact of NBTI on the circuit performance using NBTI integrated compact Verilog-A model for 10 nm NW CMOS. We analyze the impact of NBTI on the inverter, ring oscillator and 6T SRAM cell crucial performance parameters. The NBTI effects on circuits are simulated at 105 ℃ temperature, and 0.9 V supply voltage for a 10 year lifetime.

6.2.1 Inverter and Ring Oscillator Performance under NBTI

Figure 6.1(a) shows the percentage delay degradation of a FO4 load (232 aF) inverter at 25 %, 50 %, and 75 % of input duty cycle for 10 year lifetime. The delay degradation of inverter during the initial phase of a life time (say before 1 st year) is very high and increases with duty cycle value. The large degradation during 1 st year can be attributed to the large initial stage V_T degradation (as seen in Figure 5.11, chapter 5). This occurs due to the higher oxide field and larger stress induced defects in the cylindrical structure of NW gate insulator. The 25 % duty cycle of inverter exhibiting less degradation compared to 50 % and 75 % duty cycle due to the higher recovery effect (due to more off time). Figure 6.1 (b) shows the frequency degradation of a 13 stage ring oscillator (RO). The result shows that the overall RO operating frequency is degraded by ~7.5 % for 10 year lifetime. Figure 6.2(a) shows the benchmark comparison of SiNW FET inverter delay degradation with planar [78] and FinFET[145] technologies. We note that the initial delay degradation of SiNW FET is very high due to high oxide field compared to planar and FinFET. Further, Figure 6.2(b) shows the 11 stage SiNW FET RO degradation compared to the planar CMOS [146], we note that NW CMOS has higher degradation due to trapping and large interface state degeneration in gate oxide due to cylindrical structure with respect to planar RO.

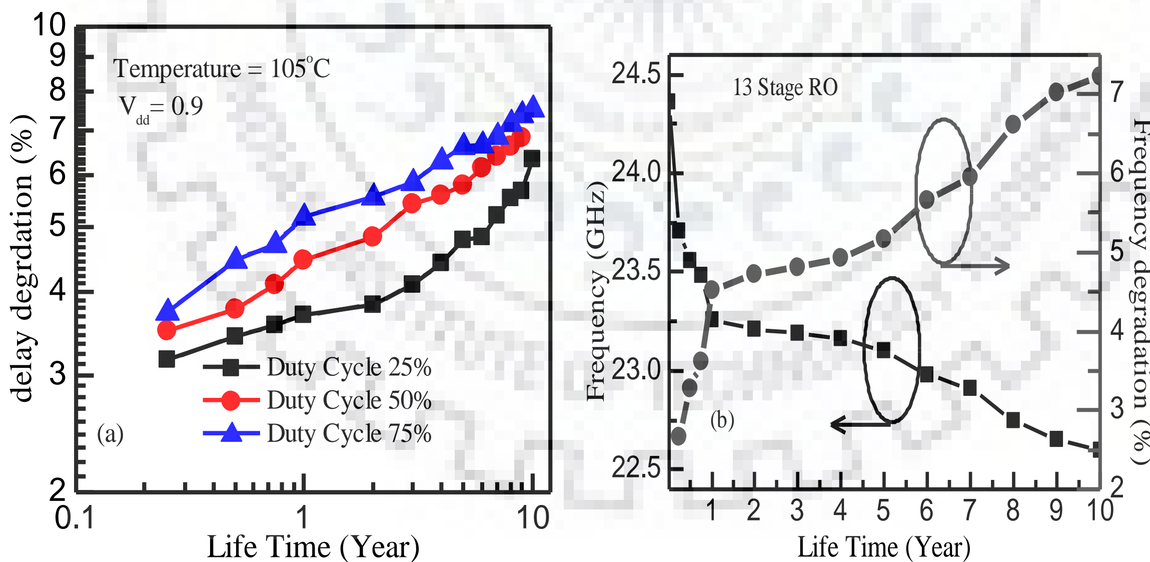


Figure 6.1 (a) Delay degradation of inverter at different duty cycle, (b) Absolute and percentage frequency degradation of the 13-satge SINW FET based ring oscillator due to NBTI.

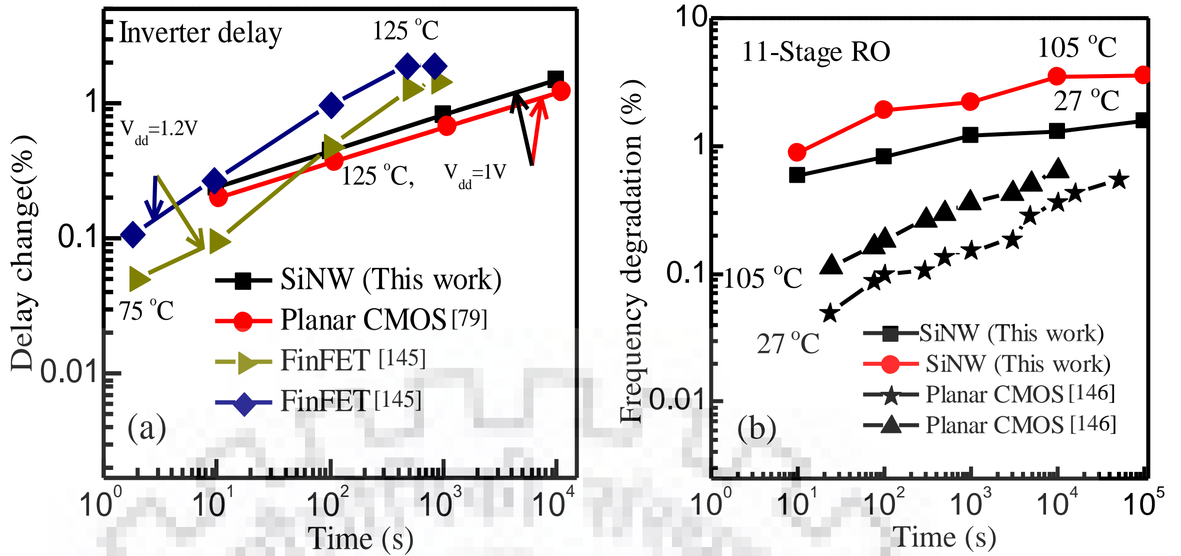


Figure 6.2 (a) The comparison of the relative delay degradation among SiNW, FinFET and planar CMOS inverters, (b) A comparison of 11-stage RO Frequency degradation between SiNW FET and planar CMOS technology at temperature 27 °C and 105°C.

6.2.2 SRAM Cell Stability

The multiwire sizing technique have been employed (as discussed in chapter 4) to design the NW 6T CMOS SRAM cell. Figure 6.3(a) shows the schematic of a SiNW based 6T SRAM cell in C_111 configuration. The configuration C_111 denotes the number of wires in pull up (PU), access (ACC) and pull-down (PD) NW transistor respectively. The SRAM cell stability is measured by the static noise margin (SNM), which quantifies the amount of noise voltage required at the internal bit cell node to flip the cell's contents, when the SRAM cell is in hold, read and write modes [147].

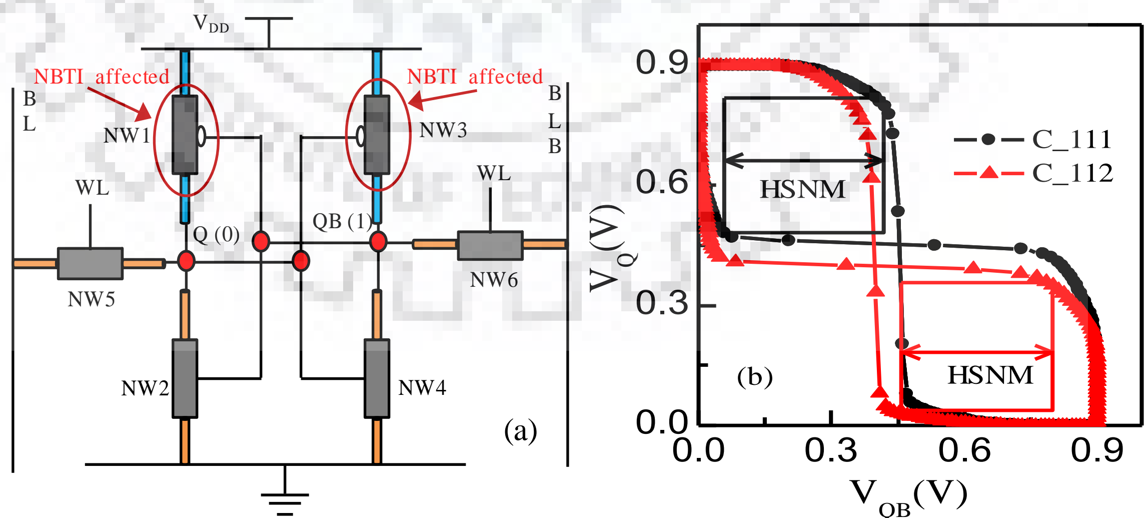


Figure 6.3(a) Schematic of SiNW FET based 6T SRAM cell in the C_111 configuration with the NBTI affected transistors. (C_111 denotes the number of wires in pull up, access and pull down transistor respectively), (b) shows butterfly curve for HSNM in C_111 and C_112 configurations.

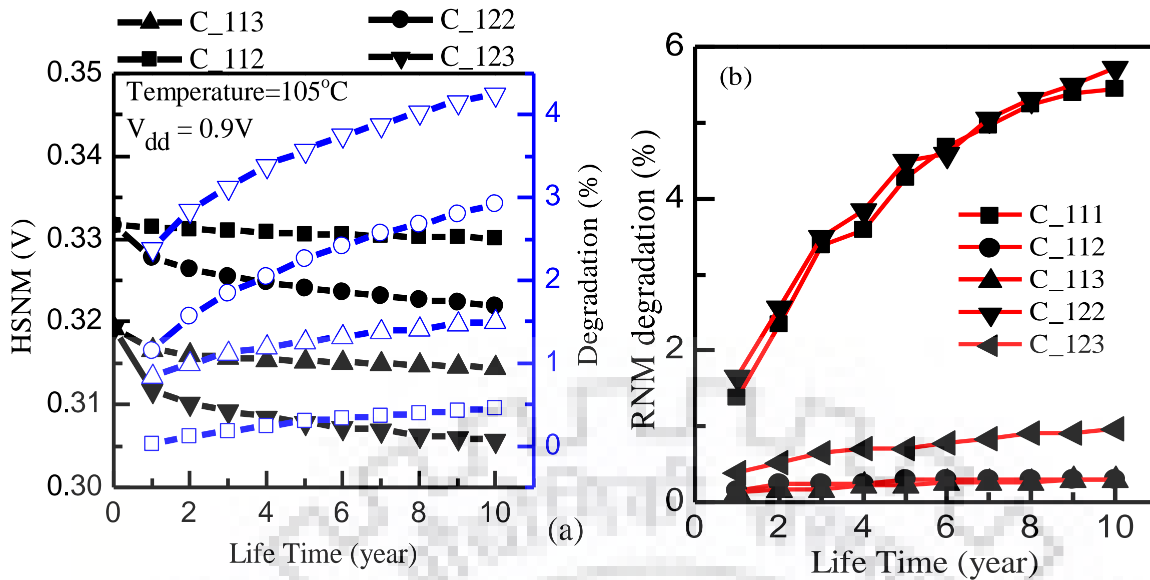


Figure 6.4(a-b) Show the HSNM and RNM degradation due to NBTI for the 10 year lifetime considering different configuration (open symbol shows the % degradation).

We have already discussed the basic read/write static and dynamic analysis of 6T SRAM cell in chapter 4. With the basic understanding of HOLD, READ, and WRITE operation, we investigate the effect of NBTI on the stability and performance of SiNW 6T SRAM cell. As shown in Figure 6.3(a) NBTI effects occur in PMOS devices. For SRAM cell the HOLD and READ stability are characterized by their static noise margin (SNMs), therefore larger the SNM, the higher is the stability. Figure 6.4(a) shows up to 4.5 % degradation in the HSNM stability due to NBTI for 10 year lifetime depending upon the design configurations. The degradation in hold static noise margin (HSNM) is mainly due to the NBTI impact on pull up NW1 and NW3 transistors. The SRAM HSNM with C_112 (0.5 %) configuration is least affected for the 10 year lifetime compared to the maximum inC_123 (4.5 %). The HSNM degradation in C_112 and C_123 configurations is due to the asymmetric strength of inverter (two and three wires in PD) formed by NW1, NW2, and weakening of PU (NW1) transistor due to NBTI cause squeezing of the upper lobe of butterfly curve.

NBTI degradation in PU transistors (NW1,3) leads to a significant effect on the RNM stability due to the reduction of the logic threshold voltage of an inverter formed by NW3,4 transistors. Figure 6.4(b) shows the impact of NBTI on the RNM of 6T SRAM cell in different design configuration. In C_111 configuration the RNM value degrades from 145 mV to 136 mV, around 6 % for the 10 year lifetime, whereas only ~ 1 % degradation is observed for C_112, C_113 and C_123 configuration as shown in Figure 6.4(b). This lower degradation of RNM in C_112, C_113 and C_123 is due to increase in the number of wires in PD transistors. Because of that, more reduction in the V_{read} (V(Q)) voltage compared to the reduction of trip voltage

V(QB) due to NBTI on NW3. Therefore, the SRAM cell with C_111 and C_122 have higher chances of failure due to NBTI as compared to C_112, C_113, C_123 configuration as shown in Figure 6.4(b). Out of all these configurations,C_112 is the best configuration in the terms of lower HSNM and RNM NBTI degradation.

In contrast to HOLD and READ stability, WRITE stability improves with NBTI. This is because NBTI degrades the driving capability of p-SiNW FET NW1 and NW3 is resulting in a less effort (easy to pull down of QB node below the trip point of the inverter formed by NW1,2 transistor) to write the data at V (Q) or V (QB) node. Figure 6.5 shows the write margin improvement in different SRAM cell configurations. The WM is calculated employing WL sweep methodology. WM is primarily depended upon the access and pull up transistors. The absolute value of WM in C_122, and C_123 configuration is large due to the high driving capability of access transistor. However, the percentage improvement in WM due to NBTI is less because of node voltages V(Q) and V(QB) counter balance each other resulting in less impact of NBTI on WM. In other configurations such as C_111, C_112, and C_113, the absolute WM is lower. For these configurations, high drive strength of the PD (NW2) transistor leads to decrement in the V(Q) node voltage, at the same time due to NBTI in PU (NW3) the node voltage V(QB) decreases. Hence, due to this combined effect (decreasing the node voltages simultaneously), there is a larger improvement in the C_111, C_112 and C_113 configuration NBTI degradation. It is seen that the WM improves ~3.5 %, depending upon the SRAM cell configurations.

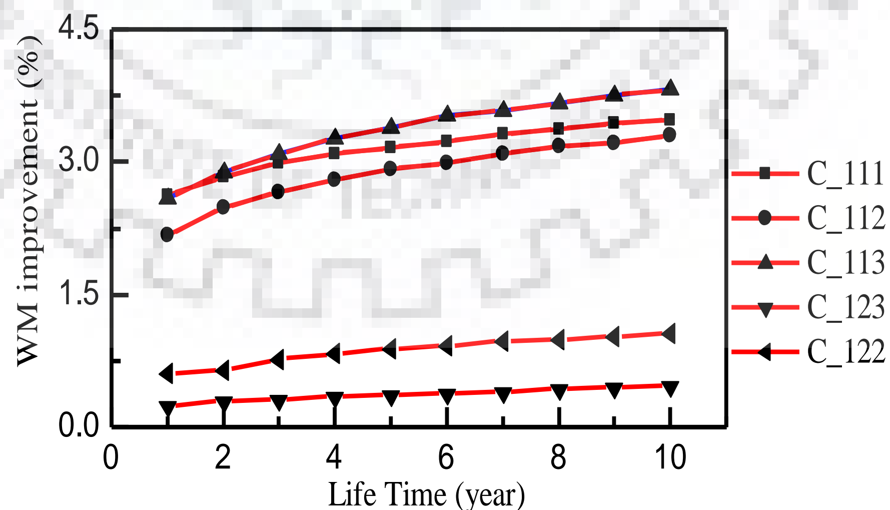


Figure 6.5 Shows write margin (WM) improvement over a 10 year lifetime.

Apart from static stability degradation, NBTI also affects the read/write access time of a SRAM cell significantly. The READ access time (RAT) is the time taken to discharge the bit-line BL

through ACC (NW5) and PD (NW2) transistors. The RAT is inversely proportional to the read current I_{READ}, which passes through NW5 to NW2 transistor as shown in Figure 6.3(a). Figure 6.6 (a) shows the READ current in different SRAM configurations, which is not affected by NBTI because of n-SiNW FET (NW5 and NW2) operates during read phase. On the other hand, write access time as shown in Figure 6.6(b), (improves) with NBTI due to the weakening of PU (NW3) p-transistor leading to the faster discharge of node V(QB). We found that due to the NBTI WAT improves ~3-7 %, depending on the configuration used for SRAM design, this can be observed in the Figure 6.6(b). Considering all SRAM cell metrics such as HSNM, RNM, WNM, RAT, WAT, C_112configuration is the best configuration.

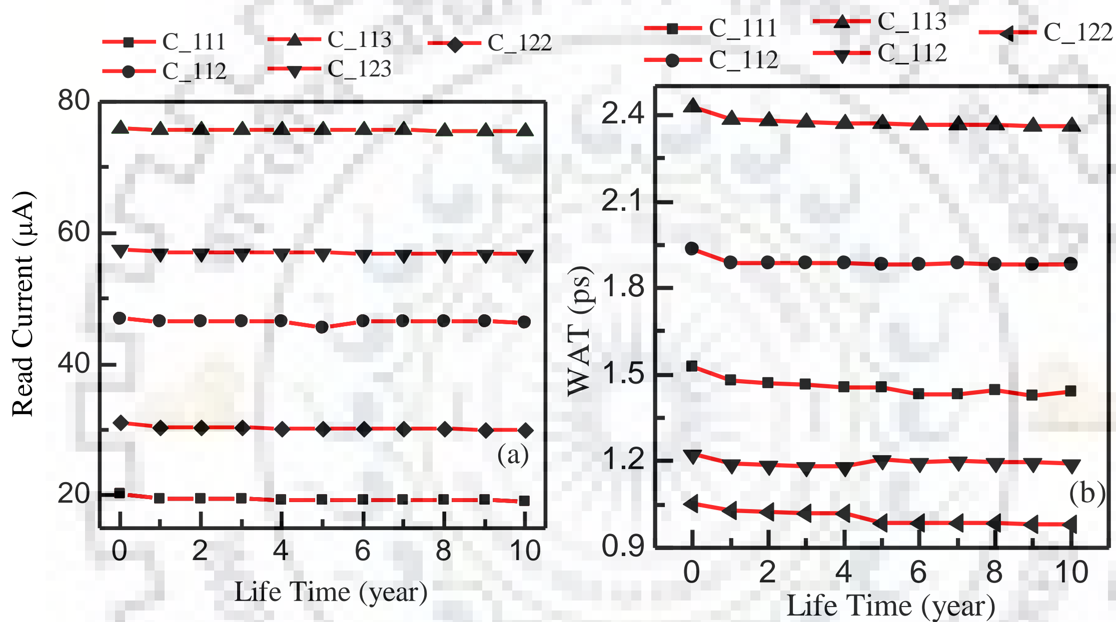


Figure 6.6 (a) Shows insignificant impact of NBTI on the read current for 10 year life time, (b) Absolute value of write access time improvement over a 10 year lifetime.

6.3 Effect of BTI (NBTI+PBTI) on NW Circuits Performance

In this section the calibrated physics based Verilog-A compact model with integrated BTI (NBTI+PBTI) predictive reliability model is used to investigate the NW FET based core logic gate delay, and SRAM cell read/write stability performance. The device and reliability models developed employ HSPICE through Verilog-A interface for circuit analysis.

6.3.1 Impact of BTI on Logic Gates

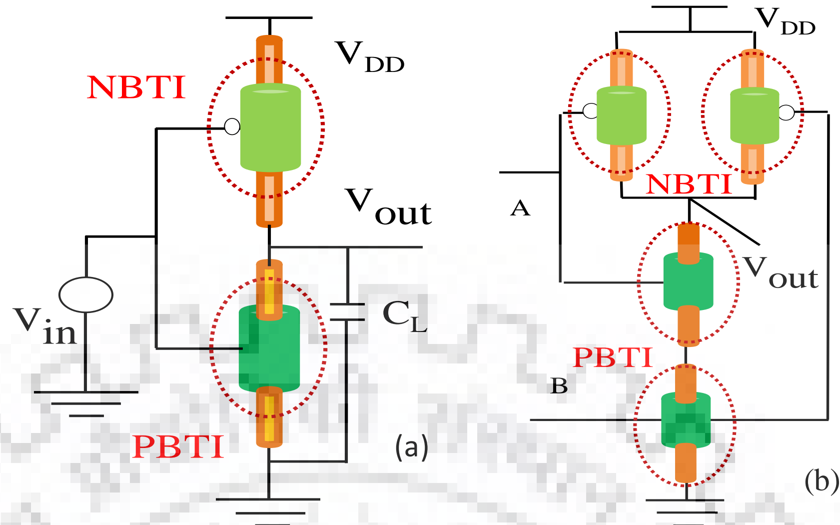


Figure 6.7 Shows the schematic with NBTI/PBTI affected transistors of (a) Inverter, (b) NAND gate.

Figure 6.7(a-b) shows the schematic of SiNW FET-based CMOS inverter circuit and NAND gate with NBTI and PBTI affected transistors. Since, NBTI and PBTI degrade the threshold voltage of PMOS and NMOS device respectively, for a logic gate, the delay from low to high (T_{PLH}) and high to low (T_{PHL}) is accordingly degraded due NBTI and PBTI. Figure 6.8(a) shows the separate and combined impact of NBTI/PBTI on propagation delay (T_{PLH}/T_{PHL}) of FO4 load inverter with a size ratio of 1:1 (pull-up: pull-down) wires. The T_{PHL} show the higher degradation due to PBTI (~30 %) compared to T_{PLH} caused by NBTI (~24 %). However, the impact of BTI (NBTI+PBTI) on propagation delay is the average delay degradation due to BTI. Moreover, it is observed that the initial delay degradation (1st year) is high, which is attributed to the larger V_T degradation due to large interface traps generation and high electron trapping in gate oxide during stress time as seen in Figure 5.10 (chapter 5). Further, it saturates for longer period of time (10 years). Figure 6.8(b) shows the comparison of inverter delay degradation due to NBTI/PBTI between 10 nm SiNW and planar MOSFET [148]. The NW based inverter show higher PBTI delay degradation compared NBTI. The higher impact of PBTI is due to more stress induced defects formation and electron tunneling in the gate oxide. Overall, the impact of NBTI/PBTI is higher on NW inverter delay comparedtoplanar FET due to high oxide field and larger V_T degradation.

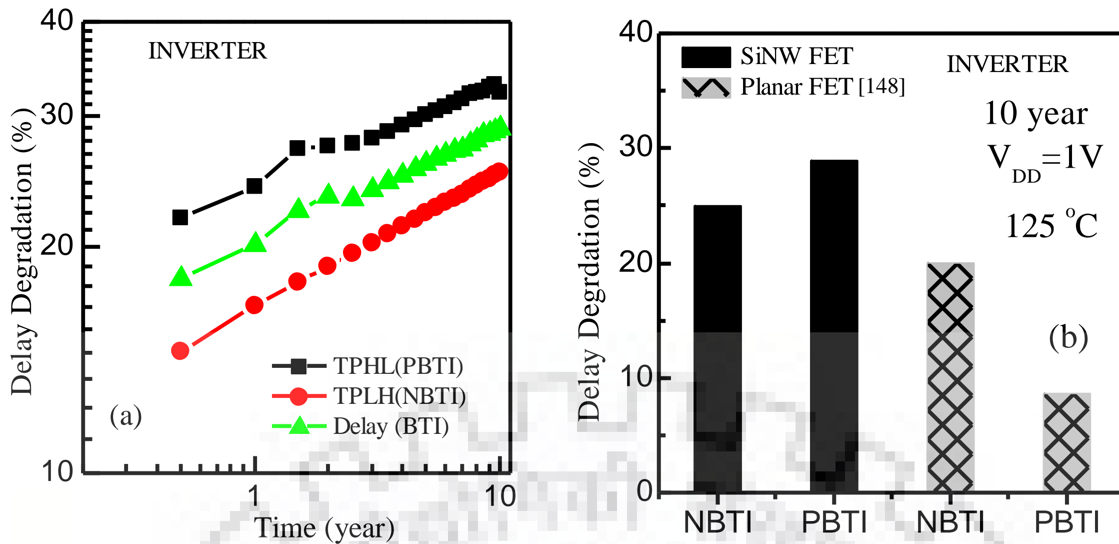


Figure 6.8 (a) Shows the effect of NBTI/PBTI on inverter delay degradation, (b) Comparison of delay between SiNW FET and planar MOSFET based inverter.

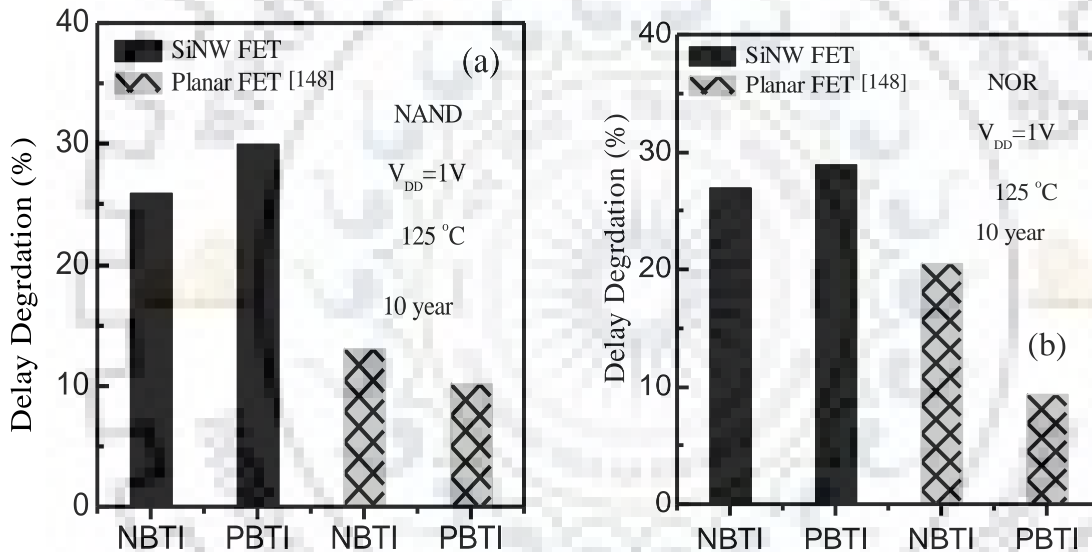


Figure 6.9 (a-b) Shows the effect of NBTI/PBTI on delay degradation of NAND/ NOR and comparison between SiNW FET and planar MOSFET.

Figure 6.9 (a-b) shows the higher impact of NBTI/PBTI on the delay degradation of SiNW FET based NAND/NOR gates compared to reported planar MOSFET [148]. The higher delay degradation in NW as discussed above is due to high oxide field, more stress induced oxide and interface traps. Further, we find that the BTI degradation is strongly circuit topology dependent. For NAND (NOR) gate shown in Figure 6.9 (a-b), the PBTI (NBTI) degradation is more significant due to the transistors connected in series i.e. in a stack. The pull down and pull up transistor of NAND/NOR gate are connected in series. Therefore, the threshold voltage degradation in series transistors takes more time to charge and discharge the output node capacitance, and hence increase the delay with time.

6.3.2 Impact of BTI on ISCAS 85 C17 Circuit

The ISCAS 85 C17 benchmarked circuit as shown in Figure 6.10 (a) is used to investigate the impact of BTI on a delay of each gate. We demonstrate the effect of BTI on each NAND gate delay from G0-G5 of the C17 circuit for the 10 year lifetime as shown in Figure 6.10 (b). The NAND gate G0 shows the least degradation ~7 %, whereas G3 shows the highest degradation of ~ 37 %. G0 and G2 are the primary gates, while G0 is followed by G1 and suffers 7.15 % delay. On the other hand, G2 is succeeded by G3, and G1, which increases its delay to 29.13 % approximately ~4X more than the G0. We find that the BTI induced delay of the gate depends on the degradation of succeeding gates. Moreover, the delay of a gate is also influenced by the degradation of the preceding gates in the circuit. The preceding gates of G1 (i. e. G0, G3) are less degraded and results in only 27.27 % delay increment for G1 gate. However, the gate preceding G5 (i.e. G3&G4) have higher delay increment, as a result, G5 approaches 30.6 % degradation. It is concluded that the difference in the gate delays is due to the different levels of degradation in the succeeding and preceding gates.

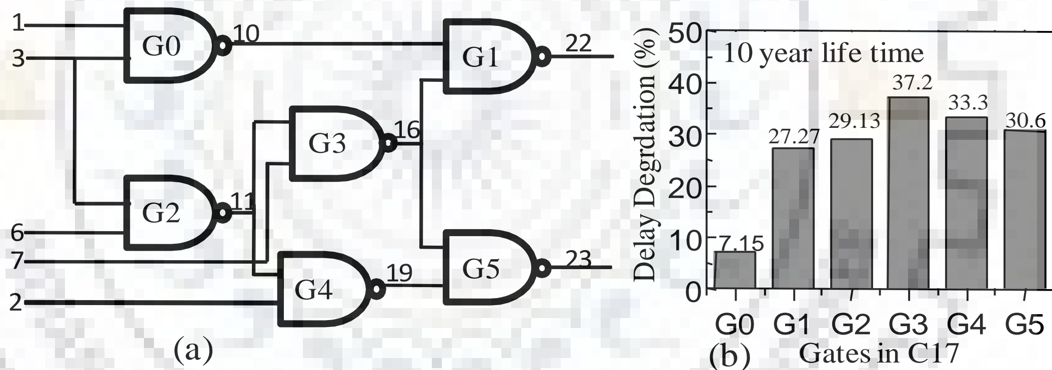


Figure 6.10 (a) schematic of ISCAS85 C17 benchmark circuit, (b) propagation delay of each gate in benchmarked circuit.

6.3.3 Impact of BTI on the Read Stability of SRAM Cell

Figure 6.11(a) shows the schematic of SRAM cell in C_111 configuration indicating NBTI/PBTI affected transistors. When the data is stored in the SRAM cell (assume 0 at Q and 1 at QB node during read/write operation), one of the nSiNW FET (NW2) and pSiNW FET (NW3) transistor are always under the positive and negative stress, respectively. We separately analyzed the effect of NBTI on NW3, and PBTI on NW2 and then combined effect of BTI (NBTI+PBTI) on SRAM cell. Figure 6.11(b) shows the traditional SRAM cell butterfly curve formed using two internal node voltages (Q and QB) before and after stress [149]. Moreover, PBTI in NW2 causes an increase in the V_{read} voltage at V(Q) node, which may cause cell to flip causing read failure. First of all, the impact of PBTI is considered in PD nSiNW FET (NW2) to

investigate the RNM stability. The PBTI in NW2 causes a reduction in the threshold voltage with time due to which the lower envelope of VTC curve formed by NW1 and NW2 shifts toward right causing a reduction in RNM as shown in Figure 6.11(b). Moreover, with PBTI in NW2 causing an increase in the V_{read} voltage at V(Q) node which may causeacell to flip and read failure.

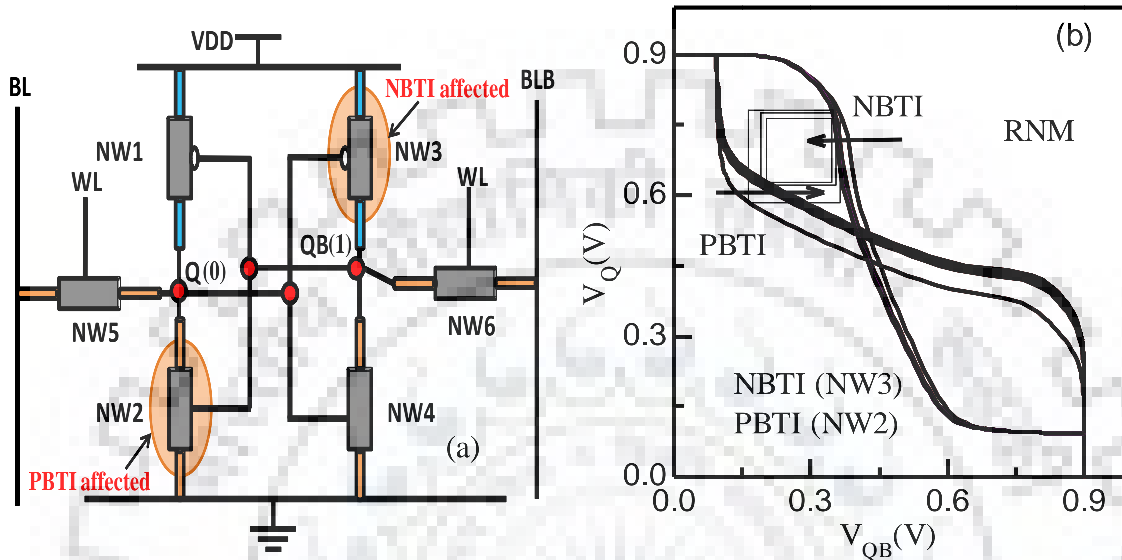


Figure 6.11 (a) shows the schematic of SiNW FET 6T SRAM cell in C_111 configuration with NBTI/PBTI affected transistor, (b) read butterfly curve.

Figure 6.12(a) shows the impact of PBTI on the RNM of SRAM cell in different design configurations such as C_111, C_112, and C_123. The C_111 shows a higher degradation ~25 % compared to C_123 (~20 %) and C_112 (~15 %) configuration for a 10 year lifetime. This lower degradation in C_112 and C_123 configuration is due to the increase in the number of wires in PD (NW2,4) transistor with respect to ACC (NW5,6) transistor. Due to which, there is larger reduction in the V_{read} voltage compared to the trip point of the inverter formed by NW3,4. Therefore, C_111 has higher chances of failure due to PBTI compared to C_112 and C_123.

Figure 6.12 (b) shows the impact of BTI on the RNM of SRAM cell in different design configurations. The NBTI in PU (NW3) reduces the trip voltage of inverter formed by NW3,4 and PBTI in PD increases the read voltage (V_{read}) at Q storage node. Therefore, the overall combined impact will degrade the RNM of SRAM cell. The C_111 configuration shows a higher degradation of ~30 % due to BTI compared to C_112 (~15 %) and C_123 (~22 %) for a 10 year lifetime. We see that the NW based SRAM cell read stability is strongly configuration dependent. With an appropriate design configuration, we can reduce the impact of BTI on

RNM degradation. We find that C_112 is the better configuration with a higher RNM value and reliability tolerant.

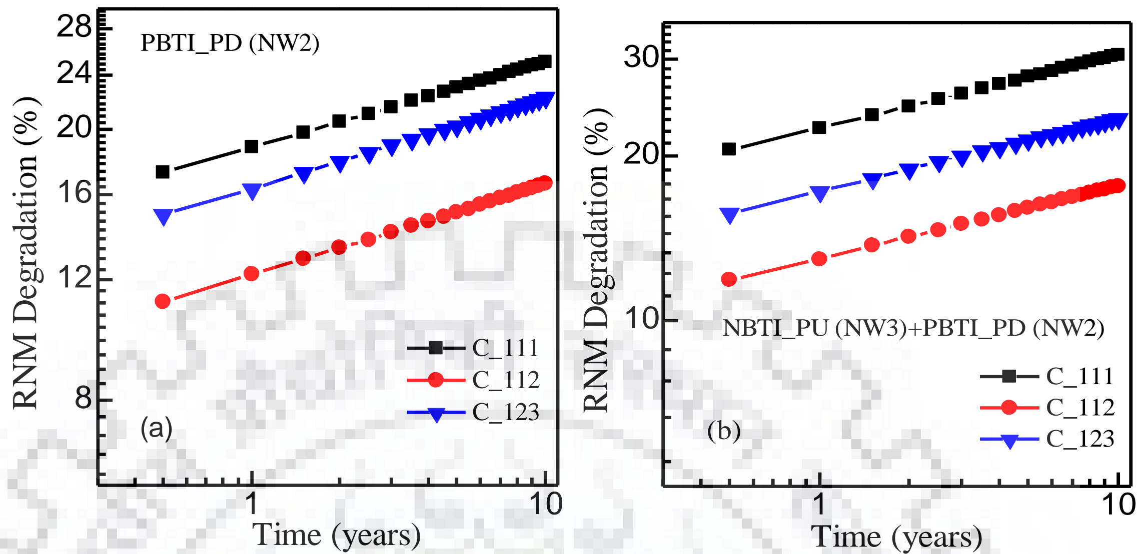


Figure 6.12 (a) Effect of PBTI on PD (NW2) transistor, (b) Combined impact of NBTI and PBTI on PU (NW3) and PD (NW2) transistor on read stability.

6.3.4 Effect of BTI on the Word Trip Voltage of SRAM Cell

Word trip voltage (WTV) quantifies the write stability of SRAM cell [128]. In the WTV method, the node voltage (here, V_{QB}) is monitored, while the word line voltage (V_{WL}) is swept from zero to V_{DD}. It is defined as the voltage difference between power supply (V_{DD}) and V_{WL} when voltage of V(QB) storage node flips. Moreover, the write noise margin of the SRAM cell depends upon the strength of ACC (NW6) and PU (NW3) transistors. However, PBTI in PD (NW2) transistor causes the lower drive, as a result the V (Q) node voltage increases and become more than the trip voltage of inverter form by NW3/NW4 transistors. Hence, it is easy to flip the storage node data. The configuration C_111 exhibits the higher improvement upto ~3.5 % in the WTV compared to C_112 (~2.8 %) and C_123 (~2 %) configuration as shown in Figure 6.13(a). In C_111 configuration, due to PBTI in PD (NW2), the storage node voltage V (Q) increase, thus it is easy to flip the states during a write operation. Whereas, in C_112 and C_123 configurations the storage node voltage (V (Q)) decreases due to increase in the number of wires in PD transistor and become more dominant than PBTI effect. Therefore, it is difficult to flip the state of a storage node. So as seen in Figure 6. 13(a) C_112 and C_123 exhibits average and lower improvement respectively.

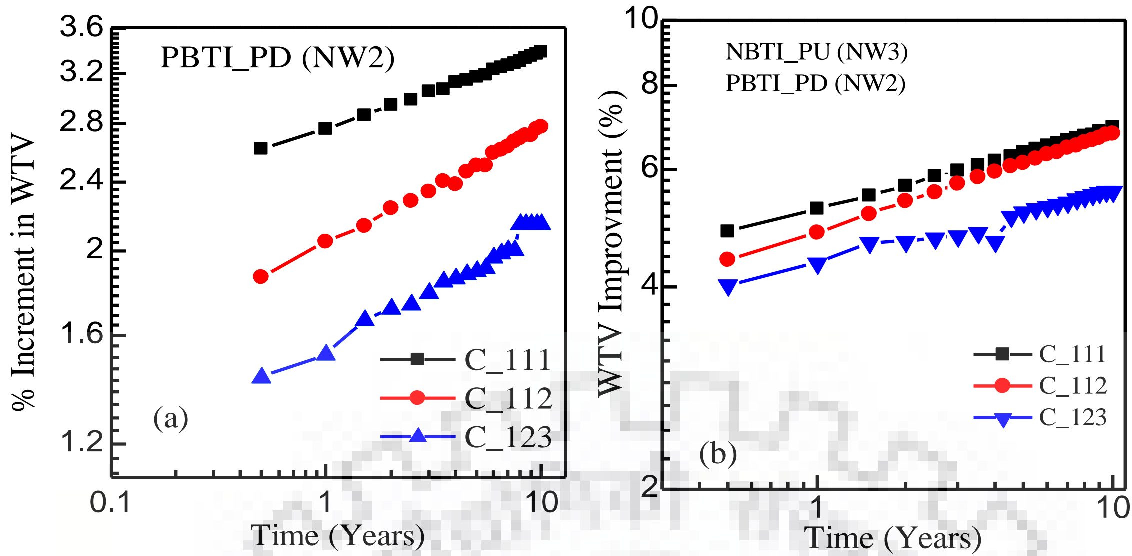


Figure 6.13 (a) The effect of PBTI on the WTV, (b) Effect of BTI (NBTI+PBTI) on the WTV in various SRAM cell configurations.

Figure 6.13(b) shows the improvement in WTV due to the impact of NBTI on PU (NW3) transistor in different cell design configurations. Since, NBTI degrades the driving capability of p-SiNW FETs, NW3, resulting in a less effort (easy to pull down of QB node below the trip point of the inverter formed by NW1,2 transistor) to write the data at V(Q)or V(QB)node. The C_111 configuration shows the higher improvement of ~5 % and C_112 & C_123 exhibits medium (~4 %) and lower (~3.5 %) respectively for a 10 year lifetime. The lower improvement in C_112 and C_123 configuration is due to decrease in V (Q) node voltage because of an increase in the number of wires in PD (NW2). Further, the effect of BTI on WTV is examined, it is found that the combined effect of NBTI and PBTI resulting in the improvement in the range of ~5-8 % for different SRAM cell design configurations. From the above analysis, it is concluded that the BTI reliability improves the write noise margin and C_112 configuration has better reliability tolerance for read/write operation.

Table 6.1 shows the comparison of the impact of NBTI, PBTI and BTI on RNM of SRAM cell for different technologies: 14 nmFinFET[150], 22 nm planar MOSFET [150] and 10 nmSiNW FET at a nominal supply voltage of 0.9 V for 3 years. We find that the FinFET, planar MOSFET and NW FET (C_111) based SRAM cells RNM degrades due to NBTI to nearly same (~6 %) extent. However, NW FET RNM degradation can reduce ~2 %,depending upon the appropriate design configuration such as C_112 and C_123 (as shown in Table 6.1).

In case of PBTI, FinFET based SRAM cell RNM degrades upto 10 % and planar MOSFET has a negligibly small impact. However, NW FET RNM degrades in the range of 14.0% to 20.0%, depending upon the cell design configurations (C_111, C_112, and C_123). Higher degradation

in NW Cell can be attributed to larger V_T degradation due to more electron trapping and formation of new oxide traps in cylindrical structure. Further, the impact of BTI on RNM is compared, in which FinFET and planar degraded by 14.8 % and 6.5 %. Whereas, NW FET SRAM cell RNM degradation due to BTI is the range of 15 % to 25 %. It is concluded from the TABLE 6.1 that NW SRAM cell RNM can be mitigated by choosing an appropriate design configuration. Finally, C_112 is the best configuration in the term of RNM degradation due to BTI and it is comparable to FinFET degradation data.

Table 6.1 Read Noise Margin (Supply Voltage 0.9V)

	Fin FET [150]	**MOSFET** [150]	**SiNW FET (This work)**		
	Initial Degradation	**Initial Degradation**	**Initial**	**Degradation**	**Degradation**
	(mV) (%)	**(mV) (%)**	**(C_111,C_112, C_123)**	**(mV)**	**(%)**
NBTI	**0.143 0.135 (5.98)**	**0.172 0.162 (5.99)**	**(0.145, 0.205, 0.155)**	**(0.137, 0.200, 0.151)**	**(4.82, 2.4, 2.4)**
PBTI	**0.143 0.126 (10.1)**	**0.173 0.173 (0.112)**	**(0.145, 0.205, 0.155)**	**(0.115, 0.176, 0.125)**	**(20.0, 14.0, 19.0)**
BTI	**0.143 0.121 (14.8)**	**0.174 0.162 (6.50)**	**(0.145, 0.205, 0.155)**	**(0.108, 0.174, 0.123)**	**(25.0, 15.0, 20.0)**

6.4 Impact of Time Zero Variability and BTI Reliability

In this section, we investigate the impact of geometrical variability (channel length (L_g), oxide thickness (t_{ox}) and radius(R)), which is superimposed on BTI for finding combined effect on core logic gate delay (INVERTER, NAND, and NOR) and SRAM cell performance. However, due to the lack of the NW experimental BTI variability characterization, which requires large number of devices we have used model based variability as a substitute. It has been experimentally demonstrated by the different research groups that the BTI variability mainly causes a shift in the mean values of the device/circuits threshold voltage, while the standard deviation (σ) does not vary significantly with stress time [151]–[153]and is dominated by the σ of time zero variability. PieterWeckx et al. [154] have also demonstrated that the total variance after BTI stress can be approximated as a sum of the time zero variance and the average V_T shift due to NBTI.For geometrical variability, we assume that the device parameters vary by ±15 % in 1000 Monte Carlo (MC) simulation within 3σ value (σ is the standard deviation).

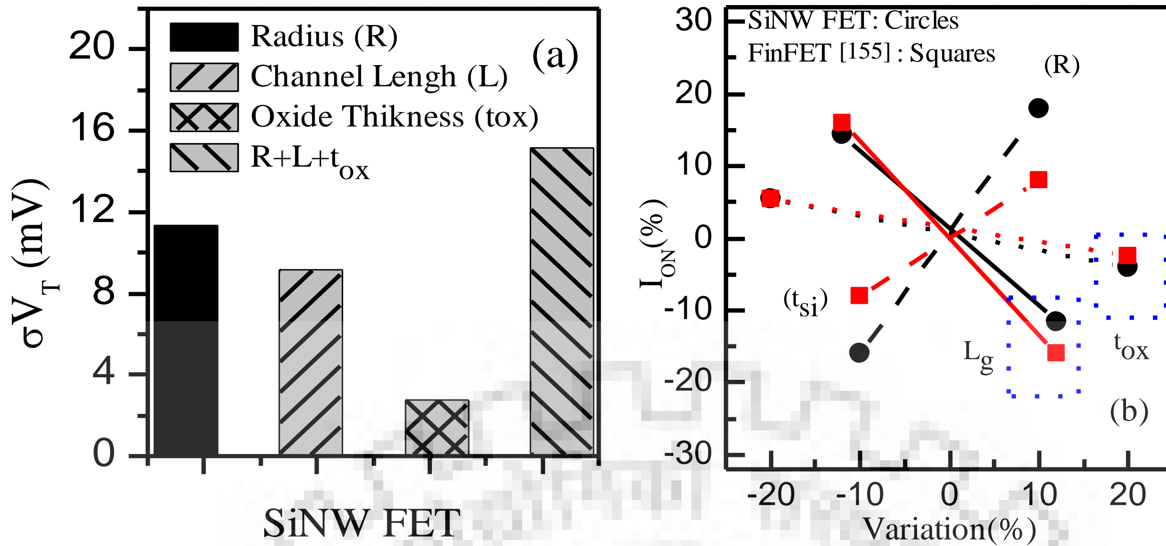


Figure 6.14 (a) V_T deviation (σV_T) due to NW geometry variation (R, L and t_{ox}), (b) Impact of geometrical variation and comparison with FinFET on the I_{ON}.

Figure 6.14 (a) shows the impact of geometrical variation on the threshold voltage deviation (σV_T) and ON current of the device. We see that the V_T variation shows a strong dependence on the radius of SiNW FET compared to the channel length and oxide thickness. Further, the sensitivity of I_{ON} due to geometrical variation is compared between SiNW FET and FinFET[155] in Figure 6.14 (b) It is found that the variation of L_g and t_{ox} for NW and FinFET causes nearly same shift in the I_{ON}. Whereas I_{ON} is quite sensitive to the diameter of NW variability compared to FinFET body thickness (t_{si}).

It is reported by Intel [156], IMEC [157]–[159] and Global Foundries [153], that, as CMOS scaling continues into the deca-nanometer range, the degradation is defectscentric, and induces time dependent variability. It is also reported that the impact of BTI variability $\sigma\Delta V_T$ in the NW is relatively lower compared to planar and FinFETs devices. In order to quantify the combined impact of BTI degradation (V_T shift), time zero variability and BTI variability on circuits, we use a hybrid approach. We use shift in V_T due to BTI using our model obtained from experimentally measured data in our study (chapter 5), and the time zero variability as obtained from TCAD and experimentally calibrated accurate Verilog-A model. However given a lack of experimental data on BTI variability, we have used data reported in the reportsmentioned above IMEC[158], [159]. It is reported that the $\sigma\Delta V_T$varies from ~4mV to ~13mV for 50mV mean ΔV_T shift due to the NW BTI variability corresponding to the 10mV to ~25mV σV_{T0} value for time zero variability [158], [159]. The BTI model in our study predicts a ~50mV ΔV_T shift in 3 years and ~35-40mV shift in 1 year for 10 nm node. Therefore, in order to the estimate impact of BTI variability, we use the literature data on NW. We have considered

~6mV (ΔV_Tshift 35mV) and ~10mV (ΔV_Tshift 50mV) $\sigma\Delta V_T$values for 1 and 3 year, respectively, due to BTI variability (corresponding to ~16mV σV_{T0} as shown in Figure 6.14 (a)) in NW circuit simulation. Furthermore, we have taken time zero variability σV_{T0} value from our TCAD calibrated compact model which is ~16 mV, this value is also consistent with the reported data [158], [159]. The total standard deviation due to the combined impact of time zero and BTI variability can be statistically expressed as [76]

$$\sigma V_{Total} = \sqrt{(\sigma V_{To})^2 + (\sigma \Delta V_T)^2} \quad (6.1)$$

where σV_{T0} is the threshold voltage deviation in the fresh devices, and $\sigma\Delta V_T$, is the additional shift in the threshold voltage induced by the BTI degradation.

Using the above approach, we have done the NW circuit level simulation under the combined impact of time zero and BTI variability. Figure 6.15 (a) shows the inverter delay normality curve under the influence of time zero and BTI variability for 1 and 3 years. The BTI variability causes the inverter delay normality curve to shift to higher value with change in the mean delay by ~0.4ps caused by BTI, and about ~0.2ps shift in the σ delay value due to BTI variability for a 3 year lifetime. Moreover, due to BTI variability, the lower and upper tails of the inverter delay normality curve are seen to deviate from the mean. Further, the impact of BTI variability on σ delay can be minimized by increasing the number of wires in pull up and pull down of the inverter.

Figure 6.15 (b-c) shows the impact of BTI and time zero variability on the NAND and NOR gates after 1 and 3 years. It is seen that NAND and NOR gates show higher initial shift in the mean delay of ~0.8ps due to BTI, and change in σ delay value of ~0.12ps due to BTI variability for 3 years of lifetime. The higher initial shift in the mean delay degradation in NAND/NOR circuit is attributed to the presence of stack (series connected) transistors. The stack transistors consist of the nSiNW FET in the pull down transistor of NAND, and sinew FET in pull up transistor of NOR gate. The series connected transistors (NAND/NOR) have higher degradation due to an increase in the series resistance and hence leads to higher shift in the delay mean value due to BTI for 3 years. Whereas, the inverter shows a lower delay meanvalue shift compared to NAND/NOR due to single wire in pull up and pull down transistor which induces lower degradation. Furthermore, the inverter shows the higher σ delay value shift after stress due to BTI variability compared to NAND and NOR gate. The lower impact on σ delay value due to BTI variability on the NAND and NOR gates can be explained by the plegrom's law of scaling (σ=1/sqrt(W_xL) in which variability is dependent upon the area of the circuit or

the number of transistors in the circuit. The NAND/NOR gates have larger area due to four transistors compared to two in inverter explaining lower σ delay shift compare to the inverter circuit. Figure 6.15 also shows the high initial shift in the delay distribution due to BTI for the first year and saturates for longer time. These delay distributions follow the same saturation behavior as seen in V_T degradation due to BTI (as discussed in Figure 5.10, chapter 5). Finally, BTI variability also causes the extremes of the normality curve to deviate from their delay mean values, which is also consistent with the reported data [160].

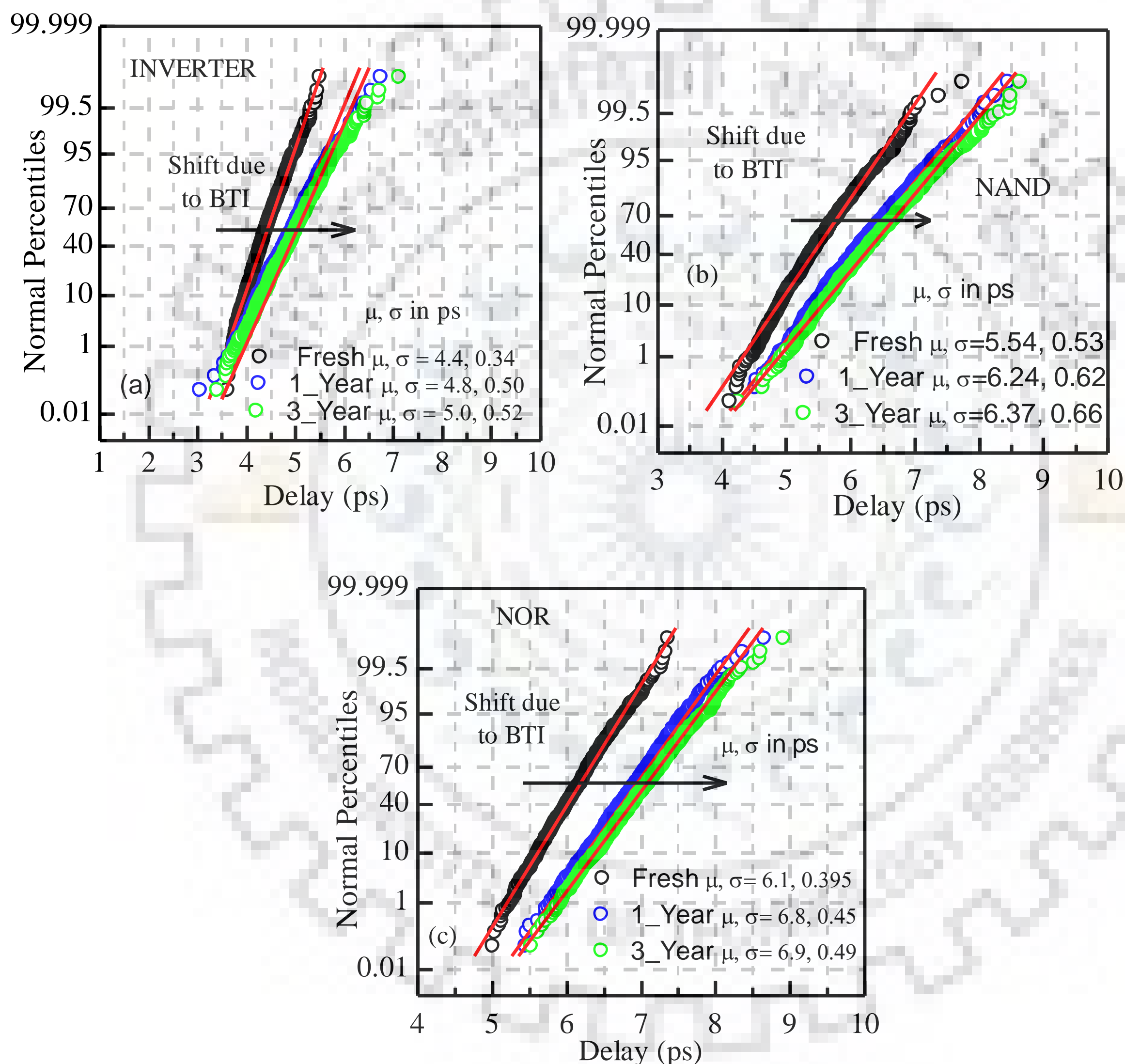


Figure 6.15 (a-c) shows the normality curve for INVERTER, NAND, and NOR delay under time zero variability and BTI reliability.

Figure 6.16 (a-c) shows the time zero (t=0s) and BTI variability on the read noise margin (RNM) of the SRAM cell in different cell design configurations C_111, C_112, and C_123.Under the influence of BTI, the mean RNM value for C_111, C_112, and C_123 configurations degrades, and shifts towards the lower value by ~28 % for the 3 year lifetime as shown in Figure 6.16 (a-c). Whereas, σ RNM shift due to BTI variability is configuration

dependent in which C_112 and C_123 shift by 8-10 %, and C_111 has an insignificant impact due to BTI variability. We observe that the BTI variability in RNM for C_111 configuration is lower compared to the C_112 and C_123 configurations. The RNM stability of SRAM cell is dependent upon the cell (current drive) ratio (PD/ACC), in which higher the cell ratio better us the stability. Moreover, the better cell ratio can be achieved by increasing the PD transistor strength relative to ACC transistor. In the SRAM cell ACC transistor is not affected due to BTI variability (as it is on for a very small period of time), whereas PD transistor is degraded due to BTI. Therefore, as we increase the number of wires in PD such as 2 and 3 wires (C_112 and C_123 configuration in Figure 6.16(a-c)), the overall impact of BTI variability on PD is higher relative to ACC due to reduced current drive, which increases the σ RNM of SRAM cell after 1 and 3 year lifetime.

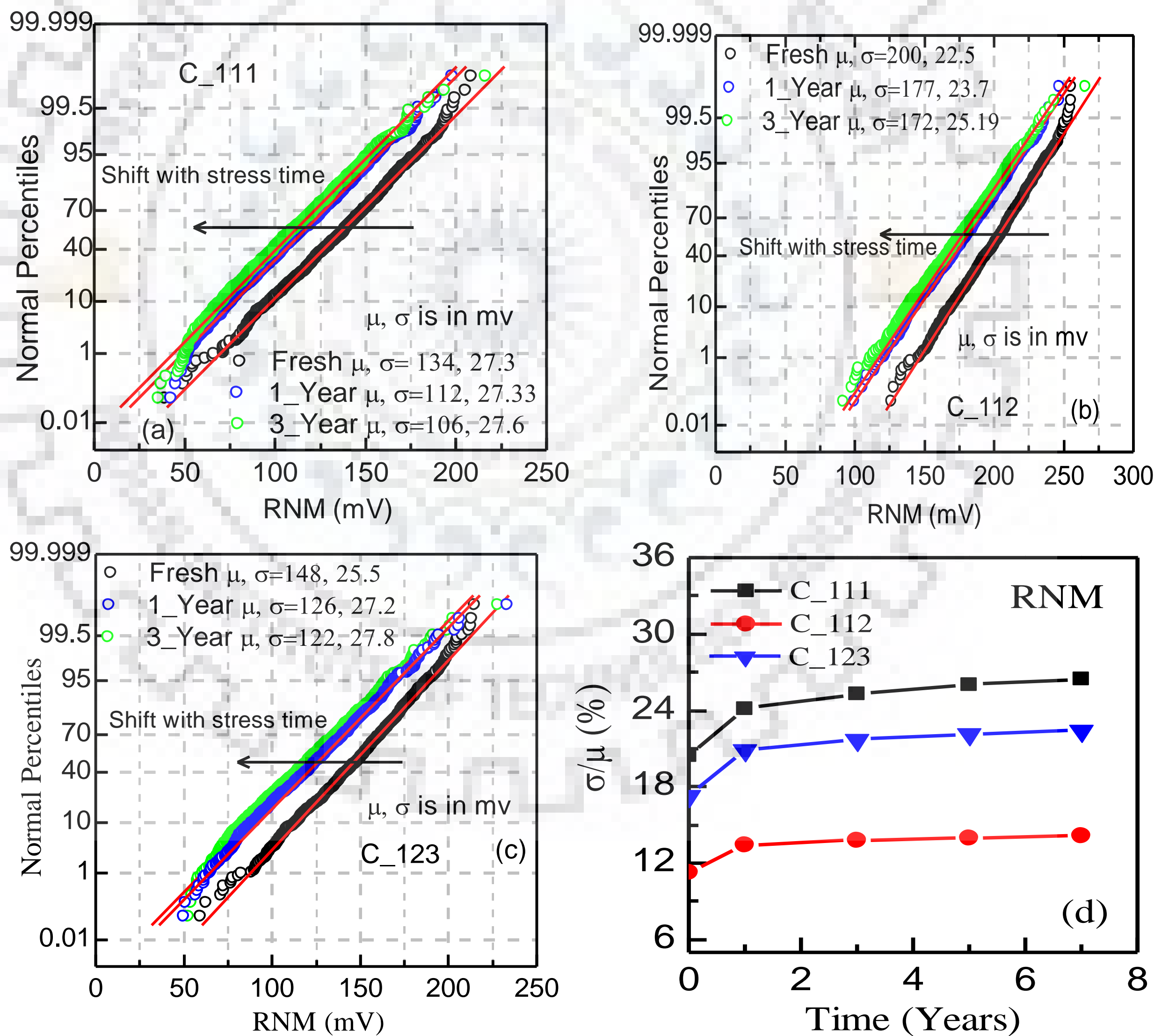


Figure 6.16 (a-c) RNM distribution under time zero and BTI variability, (d) shows the RNM variability (σ/μ) in different cell configurations.

In addition, due to BTI variability, the extremes of normality curves (e.g. C_111 configuration) deviate from the RNM mean value as shown in Figure 6.16. These end tails deviations are attributed to BTI variability and can be mitigated using an appropriate cell design configuration such as C_112, and C_123 as shown in Figure 6.16 (b-c).The normality curves clearly show that the initial shift (for 1 year) is very high and saturates for 3 years. These RNM distributions follow the same behavior as V_T degradation due to BTI (as discussed in Figure 5.10, chapter 5). The behavior of NW SRAM cell under the influence of time zero variability and BTI reliability is consistent with the FinFET based SRAM cell data and it is reported in [161]. Figure 6.16 (d) shows the RNM variability (σ/μ) under the influence of geometrical variation and BTI reliability in different SRAM design configurations. The C_111 configuration shows high variability (~25 % for 7 year of life time) due to low mean and high standard deviation. Whereas, C_112 and C_123 configurations possess lower variability (~13 % and ~20 %) due to higher μ_{RNM} and lower σ_{RNM} value. We see that the RNM is strongly configuration dependent, indicating it is possible to achieve better RNM stability with lower variability and reliability in an optimized design. Finally, it is concluded that out of all the SRAM cell design configurations, C_112 is the better configuration with high RNM mean value and less end tail deviation due to BTI variability.

6.5 Summary

This chapter can be summarized as:

1. We find that the logic gates show higher initial delay degradation and later on saturates. This is attributed mainly due to a higher initial V_T shift, which saturates for a longer stress time.
2. It is observed that the impact of BTI on logic gates is configuration dependent in which series connected transistor is degraded more such as in NAND gate (pull down transistor) and NOR (pull up transistor).
3. With these basic gates, the ISCAS85 C17 benchmarked circuit is analyzed for BTI reliability.
4. We study the impact of BTI on the read/write stability of SRAM cell in different cell configurations, and find that the read stability degrades and write stability improves with time. Further, the impact of time zero variability and BTI reliability of logic gates delay and SRAM cell READ stability is studied. It is found that the mean and sigma value of delay (μ_{delay},σ_{delay}) and RNM (μ_{RNM}, σ_{RNM}) is degraded by stress time.
5. Furthermore, we presented that with an appropriate SRAM cell design configuration,

the impact of time zero variability and BTI can be mitigated. From this study it is concluded that SRAM cell with C_112 NW FET is best design configuration, having higher read/write reliability and variability tolerance.

6. This study highlights that a circuit designer should consider these effects for a reliable circuit implementation. Overall, the compact model incorporating reliability presented here provides an excellent framework and with high potential to design reliable digital/analog nanowire CMOS circuits.

7 CHAPTER

Conclusion & Future Scope

In this chapter, we consolidate the major conclusions of this thesis work carried out on silicon nanowire compact modeling, circuit design, and reliability. Moreover, we present future directions that can be undertaken employing silicon nanowire devices.

7.1 Conclusion

In this thesis, the silicon nanowire FET (SiNW FET) based Verilog-A compact model has been developed for NW circuit design and analysis. Further, the compact model is integrated with the Bias Temperature Instability (BTI) reliability model. Its impact on digital circuit performance is comprehensively studied, and major results are concluded in this section.

In the first part of the work, an accurate unified physics based Verilog-A compact model for lateral SiNW FET has been developed by considering all the advanced nanoscale effects. The compact model is well integrated with TCAD calibrated scalable parasitic resistance and capacitance models which are highly dominating at the nanoscale regime. The model accurately predicted device characteristics obtained from TCAD as well as reported experimental devices. The developed compact model is very fast in circuit simulation compared to TCAD simulations without degrading the accuracy. Using this model, simulation and design of NW based CMOS logic circuits such as AND, OR, NAND, and SRAM cell etc. can be easily designed.This circumvents the need for performing lengthy, complex and time consuming TCAD based simulation.

In the second part of the work, the calibrated Verilog-A compact model has been employed to design the energy efficient core logic gatesandthe SiNW FET based 6T SRAM cell performance are investigated.Thecore logic gates such as INVERTER, NAND, NOR, Buffer, XOR and XNOR for a wide range of input slew and fan output load are analyzed for performance analysis.We found that the Si NW CMOS based core logic gates have better performance in the term of power dissipation (~3-4X), energy-delay (~2-3X), and power delay product(~3X) compared to correspondingFinFET based designs. This comparison showcase the benefits of Si NW CMOS logic design for power and energy efficient application.

The read, write noise margin and access time of SiNW based SRAM cells using the multiwire sizing technique are investigated by considering various design configurations such as C_111, C_112, C_113, C_124, C_123, and C_233 (C_111 denotes the number of wires in pull up, access and pull down transistor respectively). We found that with increasing the number of wires in PD transistor while keeping the number of wires in ACC transistor constant which is 1, the RNM value is increased from ~145mV in C_111 to 220mV in C_113 configurations. On the other hand, the RNM value decreases with an increase in the number of wires in ACC transistor relative to PD transistors. Out of all configurations,C_112 and C_113 are found to be the best configuration for higher RNM value. Further, we have investigated the various configurations to get high WNM by varying the wires of access transistors. The WNM in C_111, C_112 configurations are 355mV, 320mV and decreases in C_113 configuration to 280 mV, with increases wires in PD transistor. However, WNM increases with increasing the number of wires in access transistor compared to pull up transistor from C_123 (330mV) to C_233 (355mV) configurations. Hence, it is concluded that C_111, C_112 and,C_233 are the best configurations for better WNM stability.

The dynamic analysis, such as read access time (RAT) and write access time (WAT) are analyzed. The RAT decreases with increasing the drive strength of ACC and PD transistor which help to quick charge and discharge the storage node. The configuration C_111 has a highest access time 23.84ps and decreases with an increase in the number of wires (in ACC and PD) as C_112 (20.11ps), C_123 (10.94ps), C_233 (8.37ps) at the cost of larger area. It is concluded that the RAT is better for a design considering wires in $PD \geq ACC \geq PU$ and $PD/ACC \geq 1$. Finally, the SRAM cell designed for lower WAT and it is found that WAT mainly depends upon the number of wires in ACC transistor compare to PU transistor. It is shown that the smaller area SRAM cell design C_111 and C_112 are the best configurations with low WAT. Although C_233 shows better WAT compare to C_111 but with the penalty of more layout area.

In addition, the impact of device geometry dependent variability on the read and write stability of SRAM stability is investigated. It is also foundthatthe mean (μ) value of noise margin is strongly cell configuration dependent. Hence, it is possible to achieve a better SRAM cell design with a high mean value of noise margin and yield compared to large area design (C_123). The higher mean value of noise margins gives higher variation tolerance. Therefore, the C_112 configuration has higher process variation tolerance and less area penalty compared to C_113 and C_123.

The bias temperature instability power law model used in our study is a physics-based model. The model parameters explicitly described the BTI physical phenomenon. The stress and recovery bias temperature instability (BTI) threshold voltage (V_T) model for Si NW FET is obtained from the experimental NW MOSFETs using a range of stress voltage, time, and temperature. Since the model parameters are extracted from the experiments, therefore it is highly accurate and effective in predicting the device aging and reliability performance of the nanowire circuits. The obtained parameters can be scaled to nanoscale nanowire CMOS. It is found that BTI is more pronounced in SiNW FET compared to FinFET and planar MOSFETs. This is attributed to its cylindrical gate structure resulting in enhanced 2-D hydrogen diffusion and stress induced Si/SiO_2 traps. Further, the recovery model is developed, since the recovery response to stress is an important aspect of NBTI as continuous DC stress is rarely seen in real applications. Thereafter, a model is developed to investigate the long term circuit performance under the influence of BTI reliability.Finally, a comprehensive framework in which NW BTI reliability model is integrated into a Verilog-A compact model for circuit analysis is developed.

In the final chapter, the impact of BTI (NBTI+PBTI) reliability on the NW based basic logic gate and 6T SRAM cell is examined. It is seen that the delay degradation of inverter during the initial phase of a life time (say before 1 st year) is very high, and increases with duty cycle value. The large degradation during 1 st year can be attributed to large initial stage V_T degradation. Further, it is found, that the 25 % duty cycle of inverter exhibits less degradation and quick saturation as compared to 50 % and 75 % duty cycle due to higher recovery effect (due to more off time) and quick saturation (e.g.small oxide area).

We have investigated the impact of NBTI on the static and dynamic stability of the SRAM cell by considering various design configurations. The impact of NBTI on the RNM of SRAM cell is higher in C_111 configuration; whereas only ~ 1 % degradation is observed forC_112, C_113, and C_123 configuration. Further, the impact of NBTI on the write stability is studied and found that it improves upto 3.5 % depending upon the SRAM cell configuration. The RAT is not influenced by NBTI, whereas, WAT improves with NBTI due to the weakening of PU p-transistor leading to the faster discharge of a storage node. We found that due to the NBTI WAT improves ~3-7 % depending on the configuration used for SRAM design.We find that out of all configurations (C_111, C_112, C_113, C_123, and C_122), C_112 is the best configuration with lower read noise margin, read access time degradation and higher improvement in write noise margin and write access time.

In the further studies, the combined impact of NBTI and PBTI on the core logic gates such as an inverter, NAND, NOR, and 6T SRAM cell is examined. We find that the BTI degradation is strongly circuit topology dependent. For NAND (NOR) gate the PBTI (NBTI) degradation ismore significant due to the transistors connected in series, i.e. in a stack. The pull down and pull up transistor of NAND/NOR gate are connected in series. Therefore, the threshold voltage degradation in series transistors takes more time to charge and discharge the output node capacitance and hence increase the delay with time.

The impact of BTI on the RNM of SRAM cell in different design configurations is analyzed. The overall combined impact (NBTI+PBTI) degraded the RNM of SRAM cell. The C_111 configuration shows a higher degradation of ~30 % due to BTI compared to C_112 (~15 %) and C_123 (~22 %) for 10 year lifetime. It is shown that, with an appropriate cell design configuration, the impact of BTI on RNM degradation canbeminimized. Further, the effect of BTI on write trip voltage (WTV) is examined, it is found that the combined effect of NBTI and PBTI resulting in the improvement in the range of ~5-8 % for different SRAM cell design configurations. From the above analysis, it is concluded that the BTI reliability improves the write noise margin and C_112 configuration has better reliability tolerance for read/write operation.

The impact of time zero variability and BTI reliability on logic gates delay and SRAM cell READ stability is studied. The BTI variability causes the inverter delay normality curve to shift to a higher value with change in the mean delay by ~0.4ps caused by BTI and about ~0.2ps shift in the σ delay value due to BTI variability for a 3 years lifetime. The impact of BTI variability on σ delay can be minimized by increasing the number of wires in a pull up and pull down of the inverter. The impact of BTI and time zero variability on the NAND and NOR gates after 1 and 3 years is examined. It is seen that NAND and NOR gates show a higher initial shift in the mean delay with a significant change in the sigma delay due to BTI variability for 3 years of lifetime. The higher initial shift in the mean delay degradation in NAND/NOR circuit is due to the presence of stack (series connected) transistors. Finally, BTI variability also causes the extremes of the normality curve to deviate from their delay mean values which are also consistent with the reported data.

Finally, the time zero (t=0s) and BTI variability on the read noise margin (RNM) of the SRAM cell in different cell design configurations are examined. It is found that under the influence of BTI variability, the mean RNM value for C_111, C_112, and C_123 configurations degrades, and shifts towards the lower value by ~28 % for 3 years lifetime. Whereas, σ RNM shift due to BTI variability is configuration dependent in which C_112 and C_123 shift by 8-10 %, and

C_111 has an insignificant impact due to BTI variability. From the normality curve, it is clearly seen that the initial shift (for 1 year) is very high and saturates for 3 years. These RNM distributions follow the same behavior as V_T degradation due to BTI. Furthermore, we investigated that with appropriate SRAM cell design configuration, the impact of time zero variability and BTI can be mitigated. From this study, it is concluded that SRAM cell with C_112 NW FET is a better design configuration, having higher read/write reliability and variability tolerance. This study highlights that a circuit designer must consider these effects for reliable circuit implementation.Overall, the SiNW FET compact model incorporating reliability presented in this work provides an excellent framework to design reliable digital/analog nanowire CMOS circuits.

7.2 Future Scope

In this section, we concisely present future work that can be carried out based on this thesis.

1. In aggressively scaled geometries with highly confined topologies, the self-heating effect hasbecome a major concern regarding run-time performance and long-term reliability. Therefore, the predictive model on the basis of device performance and reliability due to the self-heating effect is required. Further, the self heating effect model can be integrated into NW Verilog-A compact model to analyze its impact on circuits.
2. For low power application,SiNW CMOS logic circuit and SRAM cell can be carried out in the subthreshold logic.
3. The logarithmic trapping and de-trapping threshold voltage model for bias temperature instability can be developed, which is highly accurate for high-k dielectric based SiNW FET devices. This model can be integrated in the compact model to analyze the impact of BTI variability on NW based circuits.
4. Adetailed analysis of SiNW FET can be carried out with various analog circuits such as a current mirror, differential amplifiers, and other analog circuit blocks.

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PUBLICATIONS

Journal/Transaction Publications

1. **O. Prakash**, S. Swen, S. Maheshwaram, A. Bulusu, N. Singh, and S.K Manhas, "Compact NBTI Reliability Modeling in Si Nanowire MOSFETs and Effects in Circuits," ***IEEE Trans. Device Mater. Reliab***., vol. 17, no. 2, pp. 404–413, 2017.
2. **O. Prakash**, S. Maheshwaram, M. Sharma, A. Bulusu, and S. K. Manhas, "Performance and Variability Analysis of SiNW 6T-SRAM Cell using Compact Model with Parasitics," ***IEEE Trans. Nanotechnol***., vol. 16, no. 6, pp. 965 - 973, 2017.
3. **O. Prakash**, S. Swen, S. Maheshwaram, A. Bulusu, N. Singh, and S.K Manhas, "Impact of Time Zero Variability and BTI Reliability on SiNW FET Based Circuits" ***IEEE Trans. Device Mater. Reliab.****(under review)*
4. **O. Prakash**, S. Maheshwaram, and S.K. Manhas " SiNW FET diameter tuned SRAM cell design and its variability analysis" yet to be communicated.

Conference Publications

5. **O. Prakash**, S. Maheshwaram, M. Sharma, A. Bulusu, A. K. Saxena, and S. K. Manhas, "Lateral Silicon Nanowire Based Standard Cell Design for Higher Performance," *in proc.* ***IEEE APCCAS****, 2016,* vol. 2, pp. 135–138, Jeju, Korea.
6. **O. Prakash**, S. Maheshwaram, M. Sharma, A. Bulusu, A. K. Saxena, and S. K. Manhas, "A Unified Verilog-A Compact Model for Lateral Si Nanowire (NW) FET Incorporating Parasitics for Circuit Simulation," in proc. ***IEEE VDAT***, 2016.
7. M. Sharma, S. Maheshwaram, **O. Prakash**, A. Bulusu, A. K. Saxena, and S. K. Manhas, "Compact Model for Vertical Silicon Nanowire Based Device Simulation and Circuit Design," *Proc.* ***IEEE ISOCC***, pp. 107-108, 2-5 Nov. 2015, Gyungju, South Korea.
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APPENDIX

Lateral silicon nanowire FET Verilog-A code.

```
module lnwRC (d, g, s);
        inout d, g, s;
        electrical d, g, s;
        electrical di, si;

// Parameters for device physics
        parameter real L = 14e-7;                                //cm
        parameter real R = 5e-7;                                 //cm
        parameter real tox = 1e-7;                               //cm
        parameter real NA = 5e17;                                //cm^-3
        parameter real un = 300;                                 //cm^2/V.s
        parameter real wfMet = (4.42-4.75);            // eV
        parameter real T = 300;                                  //K
        parameter real epsilOX = 3.9×8.854e-14;                  // F/cm
        parameter real Eg = 1.12;                                // eV
        parameter real EA = 4.05;                                // eV
        parameter real epsilSi = 11.7×8.854e-14;                 // F/cm

// Parameters for physical constants
        parameter real q = 1.602e-19;                            // coulombs
        parameter real kB = 8.617e-5;                            // eV K^-1
        parameter real ni = 1.48e10;                             // cm^-3
        parameter real pi = 3.1416;

// Parameters for short channel and Quantum Effects
        parameter real hbar = (1/(2×3.1416))×6.626e-34;      // J.s 4.135e-15; // eV.s
        parameter real me = 0.92×9.109e-31;                      // kg;
        parameter real aSi = 5.431e-8;                           // cm

// Parameters for Vdsat
        parameter real KSAT = 0.285/0.56;//n/p SiNW FET
        parameter real NSAT = 1.0;
        parameter real MSAT = 2;

// Parameter for Velocity Saturation & Mobility Degradation
parameter real VSAT1=5e7/2e7;                   //n/p SiNW FET
parameter real EXSAT=2;
parameter real DELTAVSAT1=0.0010/35;//n/p SiNW FET
parameter real chargewf=1;
parameter real ETAMOB4=7/2;        //
parameter real UOMULT=3;
parameter real neta4= `TYPE(0.33,0.33);
//Parasitic Capacitance Parameter
        parameter real Hg =10e-7;
```

parameter real Lsrc = 14e-7;
parameter real Ldrn = 14e-7;
parameter real Wg = 10e-7;

// Parasitic Resistance Parameter
parameter real Lext1 =3e-7;
parameter real Tc = 2e-7;
parameter real uext1=120;
parameter real Next1=1e20;

// Other Parameters Resistances and Capacitances is also defined in the Same Ways.

// Short Channel Parameter
parameter real fcrv1=1.0;//n/p SiNW FET
parameter real fcrv2=2.5/3;//n/p SiNW FET
parameter real fcrv3=1.0;
parameter real aSS1=0.95/1.2;//n/p SiNW FET
parameter real aSS2=0.9/1.29;//n/p SiNW FET
parameter real dIoff=-1.08/-2.399;//n/p SiNW FET
parameter real dDibl=9/10;//n/p SiNW FET

// For Considering Number Of Wires
parameter real NWire =1;

// Real parameters related to charge, capacitance and parasitics are defined below

real del, Cox, betainv, eta, svar, phiF, Qdep, ueff, delPhi, VchL, Vch0, LDi;
real V0, Vt, GL, z1L, z1min, z1max, eta0L, eta1L, eta2L, eta3L, z2L, lam0L, lam1L, lam2L, z3L; // for calculating I, Q
real G0, z10, eta00, eta10, eta20, eta30, z20, lam00, lam10, lam20, z30;
real alpd, alps, falpd, falps, Vds, Vgs, Vgd, Ids, Qg, Qd, Qs, Cgs, Cgd, Cdg, Csd, Csg, Cds, Cgg, Cdd, Css, Qgd, Qgs;
real galpd, galps, halpd1, halpd2, halpd3, halpd, halps1, halps2, halps3, halps, nqg, nqd, nqs, norm1;
real gm ,gds, gmbyIds, nCgg, nCsg, nCdg, nCgs, nCgd, nCsd, nCds, nCdd, nCss, norm2;
real Vges,Vses,Vdes,Vded, lnLDi, delVthVOL, qinavg, Eavg, deltox, toxeff, Coxeff, lamq, E0byq,Vbi, Vtlong, lambda, fSCE, alpSCE, Vgsfbeff, Vgsfbeff1;
real delVthSCE, svar2, Cifs, Cifd, Rdrain, Rsource, Iddi, Issi;

//Invertion charge parameter
real qins, qind, qis, qia, qia2, eta4;
real cdop1,vpolys, z, phiS, epsilRatio,WR;
//The Real mobilityand velocity saturation parameters are also defined
// The real parameters related to parasitic resistance and capacitance is also defined

analog begin

// Obtaining appropriate terminal voltages
Vds = type × V(di, si);
Vgs = type × V(g, si);

```
        Vgd   = Vgs - Vds;
        Vges  = type × V(g, si);
        Vses  = type × V(s, si);
        Vdes  = type × V(d, si);
        Vded  =Vdes - Vds;

        // Assigning value for internal variables related to device physics
        betainv = kB×T;
        Qdep = q×NA×R/2.0;
        del = q×ni/(betainv×epsilSi);  //small del
        Cox = epsilOX/(R×lln(1.0+tox/R));

        eta = 4.0×epsilSi/(Cox×R);
        svar = 2.0×epsilSi×(lln(1.0+tox/R))/epsilOX;
        LDi = sqrt(2.0×epsilSi×betainv/(q×ni));
        lnLDi = lln(2.0×LDi/R);
        phiF = betainv×lln(NA/ni);
        ueff = un;
        delPhi = wfMet - (EA+Eg/2+phiF); // wf difference between gate and Silicon body
        VchL = Vds;
        Vch0 = 0;
        V0 = delPhi + 2×phiF + Qdep/(Cox)-
betainv×ln(2×q×NA×epsilSi/(betainv×Cox×Cox));
        delVthVOL = -betainv×ln((Cox×betainv/(2×Qdep))×(1-exp(-
(Qdep×R/(2×epsilSi×betainv)))));
        Vt = V0 + delVthVOL;                    // Vt definition

// Start of evaluation of device I-V and C-V
// Source side charge calculation (alpha calculation for inversion charge)
begin
          G0 = (0.5×(Vgs-Vt-Vch0)/betainv);
                if(G0 < -10) z10=lexp(2.0×G0);
                else if (G0 > 10) z10 = G0/svar;
                else
                begin
                z10 =
sqrt((1.0/(4.0×svar×svar×svar×svar))+(1.0/(svar×svar))×(lln(1.0+lexp(G0)))×(lln(1.0+lexp(G0)
)))-(1.0/(2.0×svar×svar));       // initial guess
                end
                if (z10 > z1max || z10 < z1min) begin   //
                                if(z10 > z1max) z10  =  z1max;
                                else z10  =  z1min;
                end

                if(G0 < -50) z30 =  z10;
                else begin
                eta00 = 0.5×lln(z10+z10×z10) + svar×z10 - G0;
                   eta10 = 0.5/z10 + 0.5/(1.0+z10) + svar;
                   eta20 = -0.5/(z10×z10) - 0.5/((1.0+z10)×(1.0+z10));
                   eta30 = 1.0/(z10×z10×z10) + 1.0/((1.0+z10)×(1.0+z10)×(1.0+z10));
```

z20 = z10 -
(eta00/eta10)×(1.0+(eta00×eta20/(2×eta10×eta10))+(eta00×eta00×(3.0×eta20×eta20-eta10×eta30)/(6.0×eta10×eta10×eta10×eta10))); // firstiterationapprox
lam00 = 0.5×lln(z20+z20×z20) + svar×z20 - G0;
lam10 = 0.5/z20 + 0.5/(1.0+z20) + svar;
lam20 = -0.5/(z20×z20) - 0.5/((1.0+z20)×(1.0+z20));
z30 = z20 - (lam00/lam10)×(1.0+(lam00×lam20/(2×lam10×lam10)));
// second iteration approximate value of solution
end

alps = 1.0/(z30+1.0);
qins = (2.0×epsilSi×2.0×betainv×(1.0-alps)/(R×alps))/(betainv×Cox);

// Drain side charge calculation
The same steps has followed as discussed above to calculate the inversion charge at drain side
alpd = 1.0/(z3L+1.0);
qind = (2.0×epsilSi×2.0×betainv×(1.0-alpd)/(R×alpd))/(betainv×Cox);

// Calculation of quantum mechanical effect using above solution
qinavg = svar×(((1.0-alpd)/alpd)+((1.0-alps)/alps));
Eavg = Cox×betainv×(Qdep/(Cox×betainv)+qinavg/3.0)/epsilSi;
deltox = aSi×(pow(hbar×hbar/(2.0×q×me×Eavg),1/3));
toxeff = tox+deltox;
Coxeff = epsilOX/((R-deltox/3.0)×(ln((R+tox)/(R-deltox/3.0))));
lamq = 2.0×pi×hbar/(sqrt(2.0×me×Eavg));
E0byq = (lamq×betainv/q)×(hbar×hbar×pi×pi/(4.0×me×R×R));

// Calculation of short channel effect parameters
Vbi = 0;
VchL = Vds+Vbi+E0byq;
V0 = delPhi + 2.0×phiF + Qdep/(Coxeff)-betainv×ln(2.0×q×NA×epsilSi/(betainv×Coxeff×Coxeff));
delVthVOL = -betainv×ln((Coxeff×betainv/(2.0×Qdep))×(1.0-exp(-(Qdep×R/(2.0×epsilSi×betainv)))));
Vtlong = V0 + delVthVOL;

lambda = sqrt(((ln(1.0+toxeff/R))×(R×R/2.0)×(epsilSi/epsilOX))+(R×R/4.0));
fSCE = fcrv1/(fcrv2×((cosh(0.5×L/lambda))-fcrv3));
alpSCE = aSS1+aSS2×fSCE;
delVthSCE = fSCE×(dIoff×(Vtlong-(Qdep/Coxeff)-Vbi)-Vds/dDibl);

Vt = Vtlong + delVthSCE;
svar2=svar/alpSCE;

// Effective vgs for vdsat calculation
Vgsfbeff = Vgs - Vt;
Vgsfbeff1= Vgsfbeff/1.5;

// calculation of device I-V

// Calculation of vdsat and vdseff by BSIM

```
            Vdsat = (EsatL×KSAT(Vgsfbeff1 -
        phiS+2.0×betainv))/(EsatL+KSAT×(Vgsfbeff1 - phiS+2.0×betainv)) ;        // KSAT is
        used to decrease the current by decreasing it.

            Vdseff = Vds/pow((1.0+pow(Vds/Vdsat, MSAT)),1.0/MSAT);          //
MSAT is used to change the slope of curve connecting linear and saturation region
            if(Vdseff>Vds) Vdseff = Vds;
```

//Mobility degradation

```
delqi=qins-qind;
qia=.5×(qins+qind);
          qia2=qia;  // +  0.5×chargewf×(1.0-exp((Vdseff×Vdseff)/6.25e4))×delqi;
          eta4= (neta4)×ETAMOB4;
Eeffa = 1e-8×(Qdep/Cox+eta4×abs(qia2))/(epsilRatio×toxeff);
          DMOB2 =
1.0+UA×pow(abs(Eeffa),EU)+UD/pow(0.5×(1.0+abs(qia2)×Cox/0.01),UCS);
          DMOB2=DMOB2/UOMULT;
          ueff1=ueff/DMOB2;                        // UOMULT is used to normalize the
DMOB2 and ETAMOB4 is used to increase the variation of DMOB4
```

// Velocity saturation

```
          Esat1=2×VSAT1×DMOB2/ueff;
delvsat=DELTAVSAT1;
a11= pow((delqi/Esat1×L),EXSAT);
          P69=(delvsat+pow((delqi/Esat1×L),EXSAT));
Dvsat=1 + pow(P69,1/EXSAT)/(1+ pow(delvsat,(1/EXSAT)));
          q0=4.0×betainv×epsilSi/R;
        powI = 1.4;  // 1.4
            linI = 1.25;  // 1.6  4
            lnI =  1.95;  // 1.95
          c11=   (pow(qins,powI)-pow(qind,powI))/2.0×Cox +linI×betainv×(qins-qind);
          c12= (q0×betainv×lln((q0+lnI×cdop1×qind)/(q0+lnI×cdop1×qins)))/cdop1;
          Ids1=2.0×pi×R×ueff1×(c11+c12)×c13/(L×Dvsat); //BSIM,jimnez Current equation

falpd = (-svar/(alpd×alpd×alpSCE))+(2.0×svar/(alpd×alpSCE))+(-2.0/alpd)-(ln(alpd));
//svar replaced by svar
            falps = (-svar/(alps×alps×alpSCE))+(2.0×svar/(alps×alpSCE))+(-2.0/alps)-
(ln(alps));
            //Ids1 = (ueff1×8.0×pi×epsilSi)×(betainv×betainv)×(falpd-falps)/(L×Dvsat);
if(GEOMOD==0 &&Vds!= 0.0)
            Ids1 = Ids1/(1.0+((Rch×Ids1)/Vds)); //intrinsic current without Source Drain
resistance
```

// Short channel I-V to be used in C-V

```
            falpd = (-svar/(alpd×alpd×alpSCE))+(2.0×svar/(alpd×alpSCE))+(-2.0/alpd)-
(ln(alpd));       //svar replaced by svar
            falps = (-svar/(alps×alps×alpSCE))+(2.0×svar/(alps×alpSCE))+(-2.0/alps)-
(ln(alps));
            Ids = (ueff×8.0×pi×epsilSi)×(betainv×betainv)×(falpd-falps)/L;
if(GEOMOD==0 &&Vds!= 0.0)
        Ids = Ids/(1.0+((Rch×Ids)/Vds));   //intrinsic current without Source Drain resistance
```

// Short channel C-V

```
        // for charge calculation
                galpd = ((-1.0/(alpd×alpd))+(3.0/alpd)+lln(alpd))+(svar/alpSCE)×((-
2.0/(3.0×alpd×alpd×alpd))+(2.0/(alpd×alpd))-(2.0/alpd));
                galps = ((-1.0/(alps×alps))+(3.0/alps)+lln(alps))+(svar/alpSCE)×((-
2.0/(3.0×alps×alps×alps))+(2.0/(alps×alps))-(2.0/alps));

                halpd1 = ((-4.0/(3.0×alpd×alpd×alpd))+(5.0/(2.0×alpd×alpd))+(1.0/alpd)-((1.0-
3.0×alpd)×(lln(alpd))/(alpd×alpd))+((lln(alpd))×(lln(alpd))/2.0));
                halpd2 = ((3.0/(2.0×alpd×alpd×alpd×alpd))-
(43.0/(9.0×alpd×alpd×alpd))+(9.0/(2.0×alpd×alpd))+((2.0-
6.0×alpd+6.0×alpd×alpd)×(lln(alpd))/(3.0×alpd×alpd×alpd)));
                halpd3 = ((2.0/(5.0×alpd×alpd×alpd×alpd×alpd))-
(2.0/(alpd×alpd×alpd×alpd))+(10.0/(3.0×alpd×alpd×alpd))-(2.0/(alpd×alpd)));
                halpd = halpd1-(svar/alpSCE)×halpd2-(svar/alpSCE)×(svar/alpSCE)×halpd3;
                halps1 = ((-4.0/(3.0×alps×alps×alps))+(5.0/(2.0×alps×alps))+(1.0/alps)-((1.0-
3.0×alps)×(lln(alps))/(alps×alps))+((lln(alps))×(lln(alps))/2.0));
                halps2 = ((3.0/(2.0×alps×alps×alps×alps))-
(43.0/(9.0×alps×alps×alps))+(9.0/(2.0×alps×alps))+((2.0-
6.0×alps+6.0×alps×alps)×(lln(alps))/(3.0×alps×alps×alps)));
                halps3 = ((2.0/(5.0×alps×alps×alps×alps×alps))-
(2.0/(alps×alps×alps×alps))+(10.0/(3.0×alps×alps×alps))-(2.0/(alps×alps)));
                halps = halps1-(svar/alpSCE)×halps2-(svar/alpSCE)×(svar/alpSCE)×halps3;

                if (Vds==0)
                begin
                Qg = (8.0×pi×epsilSi×L×betainv)×(1.0-alps)/alps;
                Qd = -(4.0×pi×epsilSi×L×betainv)×(1.0-alps)/alps;
                  Qs = -(4.0×pi×epsilSi×L×betainv)×(1.0-alps)/alps;

                end
                else
                begin
                Qg = (8.0×pi×epsilSi×L×betainv)×(galpd-galps)/(falpd-falps);
                Qd = (8.0×pi×epsilSi×L×betainv)×(falps×(galpd-galps)+(halpd-halps))/((falpd-
falps)×(falpd-falps));
                  Qs = (8.0×pi×epsilSi×L×betainv)×(falpd×(galps-galpd)+(halps-
halpd))/((falpd-falps)×(falpd-falps));
                end
                norm1 = (8.0×pi×epsilSi×L×betainv)×(1.0-alps)/alps;
                nqg = Qg/norm1;
                nqd = -Qd/norm1;
                nqs = -Qs/norm1;

                // for capacitance calculation
                gm = (8.0×pi×ueff×epsilSi×betainv/L)×((alpd-alps)/(alps×alpd));
//ddx(Ids,V(g));//
                gds = (8.0×pi×ueff×epsilSi×betainv/L)×((1.0-alpd)/alpd);    //ddx(Ids,V(d));//
                gmbyIds = gm/Ids;
if (Vds==0)
```

```
		begin
			Cgs = (4.0×pi×epsilSi×L×(1.0-alps)/(2.0×alps-alps×alps+2.0×svar×(1.0-
alps)/alpSCE));
			Cgd = (4.0×pi×epsilSi×L×(1.0-alps)/(2.0×alps-alps×alps+2.0×svar×(1.0-
alps)/alpSCE));
			Cdg = (4.0×pi×epsilSi×L×(1.0-alps)/(2.0×alps-alps×alps+2.0×svar×(1.0-
alps)/alpSCE));
			Csd = ((-8.0/6.0)×pi×epsilSi×L×(1.0-alps)/(2.0×alps-
alps×alps+2.0×svar×(1.0-alps)/alpSCE));
			Csg = (4.0×pi×epsilSi×L×(1.0-alps)/(2.0×alps-alps×alps+2.0×svar×(1.0-
alps)/alpSCE));
			Cds = ((-8.0/6.0)×pi×epsilSi×L×(1.0-alps)/(2.0×alps-
alps×alps+2.0×svar×(1.0-alps)/alpSCE));
			Cgg = (8.0×pi×epsilSi×L×(1.0-alps)/(2.0×alps-alps×alps+2.0×svar×(1.0-
alps)/alpSCE));
			Css = ((8.0/3.0)×pi×epsilSi×L×(1.0-alps)/(2.0×alps-
alps×alps+2.0×svar×(1.0-alps)/alpSCE));
			Cdd = ((8.0/3.0)×pi×epsilSi×L×(1.0-alps)/(2.0×alps-
alps×alps+2.0×svar×(1.0-alps)/alpSCE));
		end
		else
		begin
			Cgs = ((L×L×(gds+gm)×(gds+gm)/(ueff×Ids))-(Qg×(gds+gm)/Ids));
			Cgd = ((-L×L×gds×gds/(ueff×Ids))+(Qg×gds/Ids));
			Cdg = ((-L×L×gds×gds/(ueff×Ids))+(Qg×gds/Ids)-((Qs-Qd)×gm/Ids));
			Csd = ((Qs-Qd)×gds/Ids);
			Csg = ((L×L×(gds+gm)×(gds+gm)/(ueff×Ids))-(Qg×(gds+gm)/Ids))-
((Qd-Qs)×gm/Ids);
			Cds = -Csd;
			Cgg = Cgs+Cgd;
			Css = Csd+Csg;
			Cdd = Csd+Cgd;
		end
		norm2 = (4.0×pi×epsilSi×L/svar2);// for normalising short channel capacitance
```

//Parasitic capacitance

// Outer fringe capacitance calculation Cof

```
		HWsr=sqrt((Hg×Hg) + (Wg×Wg));  //lenghans width sqrt
		etanw1= HWsr - R - tox;
		etanw2= 4.0×Hg×Wg - pi×((R+tox)×(R+tox));
		etanw=sqrt((2×pi×R×etanw1)/etanw2);
	if (Lsrc>= HWsr)
	begin			//Hg and Wg are the hight and width og gate
		Cof_gex1 = Hg - R - tox;
		Cof_gex2 = 2.0×(Wg/Hg) + 1.0 - Hg/HWsr;
		Cof_gex3 = Wg - R - tox;
		Cof_gex4 = 2.0×(Hg/Wg) + 1.0 - Wg/HWsr;
		Cof1=(8.0/pi)×epsilsrc×etanw×(( Cof_gex1×Cof_gex2));
		Cof2=(8.0/pi)×epsilsrc×etanw×((Cof_gex3×Cof_gex4));
		Cofd = Cof1 +Cof2;  // outer fring capacitance calculation
	end		//
```

```
else
begin
                Cof_gds = epsilsrc×(4.0×Hg×Wg - pi×((R+tox)×(R+tox)))/Lsrc;
                Cof_gex5 = 4.0×epsilsrc×(Lsrc - tox + R×lln(Lsrc/tox))×sqrt((2.0×R)/(Lsrc +
2.0×R + tox));
                Cofd = Cof_gds + Cof_gex5;
        End

        // Inner fringe capacitance calculation Cif
        Cifd = 4×epsilSi×(R + tox)×lln((2×tox + R)/(2×tox));

        // Side wall capacitance
        Lsbyd=L/2;
        bbya1 = sqrt((Lsbyd × L) ×(Lsbyd + Ldrn)×( L + Ldrn)) ;
        bbya2 = Ldrn×(L+Ldrn+Lsbyd);
        bbya = (2×bbya1 + 2× Lsbyd×L)/bbya2 +1;
        Csided = (4×epsildrn×(Hg + NWire×Wg)/pi)×lln(bbya);

        // Overlap capacitance
        Cov = (2.0×pi×epsilOX×Lov)/(lln((tox+R)/R));

        Cgdpara=NWire×(Cofd + Cifd + Cov)+Csided;
```

(In the same way, we have also included the source parasitics capacitance)

```
//Parasitic source drain resistance calculations
        // spreding resistance
                rowext1 = 1/(q×uext1×Next1);
                Weff= 2×pi×R;
                tanalpha = (R- Tc)/Lext1;
                Rsp = (rowext1/(Weff×tanalpha)) ×lln((Tc + (Lext1×tanalpha))/Tc);
                Rsp = Rsp;

        // Source drain extenstion resistance
                A = pi×R×R;
                rowext2 = 1/(q×uext2×Next2);
                Lext2 = Ldrn - 6e-7; // /$&×
                Rext = (rowext2×Lext2)/A;
                Rext = Rext;

        //S/D interface resistance
                rowext3 = 1/(q×Next3×uext3);
        //A2 = pi×R×R;
                Rsh = (rowext3×Lext3)/A;
                Rsh = Rsh;

        // Deep S/D resistance
                A1= Hsd×Wsd;
                rowsd = 1/(q×Nsd×unsd);
                tanalpha1=(Hsd-R×0.5)/(2×Lsd);
                Rspdp = rowsd/(Weff×tanalpha1)×lln(2);
```

```
Rshdp = (rowsd×Lsd)/A1 ;
Rdp = Rspdp×Rshdp/(Rspdp + Rshdp);
Rdp = Rdp;
```

// Contact resistance calculation

```
rowhdd = (1/(q×Nc×uncon));
lt = sqrt(rowc/rowhdd);
Rcon = (rowc/(lt×W))×((1 + exp(-2.0×(lc/lt)))/(1 - exp(-2.0×(lc/lt))));
Rcon = Rcon;
RDrainGeo=  (Rsp + Rext + Rsh + Rdp + Rcon)/NWire; (In the same way, we
have also included the source parasitics resistance)
```

// For asymmetric source/drain resistance

```
if(DRIGHT==1.0)begin
    Rdrain=RDrainGeo;
    Rsource=RSourceGeo;
end
else begin
    Rdrain=RSourceGeo;
    Rsource=RDrainGeo;
end
```

// Calculation of impact of parasitic resistance on device I-V or current through resistance

```
Iddi = Vded/ Rdrain;
    Issi = Vses/ Rsource;
```

// Calculation of impact of miller capacitance through Qg

```
Qgd = Cgd×Vgd;
        Qgs = Cgs×Vgs;
```

// Terminal current, voltage, and impacts of parasitic

```
if(GEOMOD==1)
    begin
        I(d, di) <+ type×Iddi;
        I(s, si) <+ type×Issi;
    end
    else
    begin
        V(d, di) <+ 0.0;
        V(s, si) <+ 0.0;
    end
```

//Impact of parasitic capacitance through miller calculation

```
    I(g,d) <+ type×ddt(Qgd);
I(g,s) <+ type×ddt(Qgs);
```

//Device current

```
I(di,si) <+ type×NWire×Ids1;
end
endmodule
```

LIST OF FITTING PARAMETERS

Name	Unit	nSiNW/pSiNWFET (values)	Description
Type	-	1/-1	1 for nSiNW FET -1 for pSiNW FET
Saturation Velocity parameters			
VSAT1	cm/s	5e7/2e7	Saturation Velocity
KSAT	-	0.285/0.56	Parameter for V_{dsat}
NSAT	-	1/1	
MSAT	-	2/2	Smoothing factor for V_{dsat}
EXSAT	-	2/2	Fitting parameter for V_{dsat}
DELTAVSAT1	-	0.0010	
Mobility degradation parameters			
UOMULT	-	3/3	
ETAMOB4	-	70/2	
neta4	-	0.33/0.33	
chargewf	-	1/1	
Short channel effect parameters			
fcrv1	-	1/1	These parameters are used to match the curve in transition region and for subthesholdslope
fcrv2	-	2.5/3	
fcrv3	-	1/1	
aSS1	-	0.95/1.2	
aSS2	-	0.9/1.29	
dIoff	-	-1.08/-2.399	I_{off}
dDibl	-	9/10	DIBL
Linear Region of Operation			
powI	-	1.4/2	These parameters are used to match the curve in linear region
linI	-	1.25/2	
lnI	-	1.95/1	