DESIGN AND ANALYSIS OF NEAR THRESHOLD CMOS STORAGE ELEMENTS CONSIDERING VARIATIONS AND SOFT ERRORS

Ph.D. THESIS

by

CHAUDHRY INDRA KUMAR

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE - 247667, INDIA
JUNE, 2019

DESIGN AND ANALYSIS OF NEAR THRESHOLD CMOS STORAGE ELEMENTS CONSIDERING VARIATIONS AND SOFT ERRORS

A THESIS

Submitted in partial fulfilment of the requirements for the award of the degree

of

DOCTOR OF PHILOSOPHY

in

ELECTRONICS AND COMMUNICATION ENGINEERING

by

CHAUDHRY INDRA KUMAR

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE – 247667 (INDIA)
JUNE, 2019

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **"DESIGN AND ANALYSIS OF NEAR THRESHOLD CMOS STORAGE ELEMENTS CONSIDERING VARIATIONS AND SOFT ERRORS"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electronics and Communication Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from July, 2014 to June, 2019 under the supervision of Dr. Anand Bulusu, Associate Professor, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(CHAUDHRY INDRA KUMAR)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

(Anand Bulusu)
Supervisor

Date:_____

The Ph. D. Viva-Voce Examination of **Mr. CHAUDHRY INDRA KUMAR**, Research Scholar, has been held on 31st August 2019.

Chairman, SRC

Signature of External Examiner

This to certify that the student has made all the corrections in the thesis.

Signature of Supervisors

Head of the Department

ABSTRACT

Energy efficient computation is vital for the success of the next generation very large scale integration (VLSI) applications. Operating circuits in sub/near-threshold voltage (NTV) regime is one of the techniques to design energy efficient circuits. However, NTV computing has created resiliency challenges, including increasing timing faults due to process, voltage and temperature (PVT) variations and data-retention failures due to radiation-induced soft errors in modern digital circuits. To address these issues resilient circuit techniques are used to mitigate the performance degradation and data failures resulting from PVT variations and external transient noise. The work in this thesis proposes a framework to handle timing errors and soft errors issues in the NTV regime employing a resilient approach. First, we proposed a resilient latch that overcomes the timing errors issues in the NTV region. Moreover, a systematic methodology to resolve soft error issues, which are critical for memory elements (latches/SRAM) in the NTV is developed. For the same, first, an accurate model to estimate the critical charge for a static D latch is derived. Using the proposed model, soft error susceptible latches/Flip-Flop's can be identified at an initial design stage (pre-layout) and, subsequently, replaced by the radiation hardened latches. However, the reported radiation hardened latches are implemented with too large cost penalties in terms of delay, power, and area. To overcome the issue, we proposed low cost and highly reliable radiation hardened latches in the NTV regime. In this thesis we also proposed a cost effective radiation hardened SRAM cell since it is similar to a static latch.

In this thesis, first we present an energy efficient and resilient circuit design approach using novel self correcting latches (SCL). The proposed SCL technique corrects the faults due to timing violation caused by variations in data-paths and sequential elements automatically, thereby lowering PVT variation induced performance degradation. Our SCL technique employs inverse narrow width effect (INWE) in designing the self-correcting latches to reduce performance variability. The SCL technique can achieve higher performance when compared to reported resilient techniques with a much smaller area and power overhead. Consequently, most of the traditional design margins due to global and local PVT variations are eliminated which results in significant energy savings.

Further, we propose a physics based semi-analytical model to estimate the critical charge, which is a key to assessing the radiation-induced soft error susceptibility of static D-latch. To develop the model, first, we argue that the value of the critical charge increases with fan-out load of a latch. The proposed model is a function of design parameters such as transistor sizes, supply voltage and fan-out load. Consequently, it enables characterizing the spread of critical charge due to process-induced variations in these parameters. This can help circuit designers to estimate and optimize the critical charge and hence the SER at an initial design stage. The critical charge estimated by the model is in good agreement with SPECTRE simulations. Therefore, the proposed model can serve as a reliable alternative to time-intensive SPICE simulations for estimating the critical charge at design stage.

In order to limit the radiation-induced soft errors further, we propose three novel highly reliable energy efficient radiation hardened latches. The proposed latches provide the soft error tolerance by using restorer circuits (RC) to hold the correct state and Muller C-element to block the fault. The RCs are based on pull-up and pull-down paths, controlled by different susceptible nodes, results in better radiation tolerance. Furthermore, to improve the D-Q and CLK-Q transmission delay, we use INWE at the layout level of the proposed latches. The proposed latches effectively, maintain their soft error tolerance in the presence of PVT variations. We also verify the soft error rubostness of the proposed latches in TCAD mixed mode simulations.

Finally, we extend our analysis to SRAM cells. Scaling of CMOS SRAM have led to a denser packing, however, this makes SRAM cells more susceptible to a single event multiple-node upset (SEMNU). Therefore, to mitigate the effect of SEMNU in SRAM cells, we propose novel energy efficient radiation hardened memory cells in NTV regime. The proposed cells maintain its radiation-induced soft error tolerance in the presence of PVT variations. The TCAD mixed mode simulations show that our memory cells have a better performace as compared to the existing radiation hardened memory cells. Therefore, for NTV and aerospace applications our proposed memory cells would be a better choice.

ACKNOWLEDGEMENT

सरस्वति महाभागे विद्ये कमललोचने।

विद्यारूपे विशालाक्षि विद्यां देहि नमोऽस्तु ते॥

Completing this doctoral program was possible with the support of several people who contributed to shaping this thesis. First of all, I express my profound gratitude to my supervisor, Dr. Anand Bulusu without his guidance, encouragement and continuous moral support this work could not exist. I learned from him how to face challenges, question thoughts, and express ideas. His guidance helped me all the time, not only in research but also in leading a better life. He is not only excellent in his profession, but a gentle human being also. Words are not enough to express my gratitude to him.

I would like to express my sincere thanks to Prof. Sudeb Dasgupta, Head, Department of Electronics & Communication Engineering, Dr. A. Patnaik, Chairman DRC, Prof. D. Singh, Chairman SRC, and Dr. V. Rastogi, Department of Physics, (External expert), for being my research committee members. My sincere thank to Dr. B. K. Kaushik, Dr. B. P. Das, and Dr. B. Kumar for their lectures and discussions, which helped me to deal with the technical problems during the Ph.D. My sincere thanks to Mr. Naveen Kanwar, Microelectronics and VLSI Design Group, and other non-teaching staff of ECE Department for providing the basic lab facilities and support.

I would like to give special thanks to my senior Dr. Arvind Kumar Sharma for all the support and guidance throughout my Ph.D. His consistent motivation, valuable comments and suggestions helped me to finish the research problems efficiently. I am very grateful to my friend Dr. Abhishek Bhattacharjee for his patience and precious time to review my research papers and thesis thoroughly. I would like to sincerely thank senior research scholar of Microelectronics and VLSI group, Dr. Baljit Kaur, Dr. Pankaj Pal, Dr. Manoj Majumdar, Dr. Shivam Verma, Dr. Archana Pandey, Dr. Savitesh, Dr. Ruchi, Dr. Abhishek Acharya and Om Parkash for all the technical discussion, moral support and motivation during Ph.D.

Most Importantly, I would like to thanks my PhD friends Mandeep, Govinda, Lalit, Vikas sir, Anant sir, Sanjay sir, Sourabh, Upendra Bhatt, Satendar, Navjeet, Neeraj, Prabhat, Nitanshu, Sarita, Swati, Sonal, Amit, Rahul, Dinesh for their support, friendship and having important technical discussions related to my research. A special thanks to Priyamvada and Poorvi for all

the fun time we enjoyed together and to make this Ph.D journey memorable and pleasant. I have spent a lot of time with them at IITR and memories that brings smile on my face. I want to thanks my friends, Anuj Tewari, Santosh Gupta, Mohit Maru, Balbir Awana, Puspraj Chauhan, Khaliq Ansari, Shalini and Natwar for motivating me to opt for higher studies.

Finally, I would like to thanks my beloved parents (Shri Jagpal Singh and Smt. Kamlesh Singh), caring brothers (Rajneesh bhaiya, Partap bhaiya, and Krishan bhaiya) and loving sister-in-laws (Priya bhabhi, Anu bhabhi, and Sangeeta bhabhi) for supporting me without any expectations at every juncture of my life. I am lucky to have them in my life. I could not imagine myself at this level without the values they taught me. I offer my sincere gratitude to the Almighty for giving me the right inspiration at right time, blessing me with all the good fortunes and the company of right people who helped me to move toward the aspiration of life.

Date:

Place: (Chaudhry Indra Kumar)

CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABBREVATIONS AND SYMBOLS

6T	Six Transistor
10T	Ten Transistor
12T	Twelve Transistor
13T	Thirteen Transistor
14T	Forteen Transistor
AEDP	Area Energy Delay Product
B	Boron
BL	Bit Line
BLB	Bit Line Bar
BPSG	Borophosphosilicate Glass
Cg	Gate Capacitance
C_L	Load Capacitance
C_{ox}	Oxide Capacitance
C_p	Parasitic Capacitance
CG	Clock Gating
CLCT	Circuit and Layout Combination Technique
CMCE	Clocked Muller C-element
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DIC	Dual Interlocked Cell
DID	Die-to-Die
DIRT	Dual Input Inverter Radiation Tolerant
DNCS	Double Node Charge Sharing
DNU	Double Node upset
DNURL	Double Node Upset Resilient Latch
DSTB	Double Sampling with Time Borrowing
DUT	Device Under Test
ECC	Error Correction Coding
EDC	Error Detecting and Correcting
EDP	Energy Delay Product
EHP	Electron Hole Pair
EMFF	Error Masking Flip-Flop

ERFF	Error resilient Flip-Flop
FBT	Feedback Transistors
FERST	Feedback Redundant Single Event Upset Tolerant
FF	Fast Fast
FS	Fast Slow
FO	Fan-Out
FOM	Figures-of-Merit
GND	Ground
HPST	High Performance SEU Tolerant
HRDNUT	Highly Robust Double Node Upset Tolerant
HSPICE	SPICE Simulator by Synopsis Inc.
I_{DS}	Drain Source Current
I_{dsat}	Drain Saturation Current
i_{Mn}	NMOS Current
i_{Mp}	PMOS Current
I_{out}	Output Current
I_{SEU}	SEU Current due to Soft Error
$I_{SEU,trip}$	Trip SEU Current due to Soft Error
ITD	Inverse Temperature Dependence
INWE	Inverse Narrow Width Effect
k	Boltzman Constant
KCL	Kirchoff's Current Law
λ	Channel Length Modulation Factor
L	Channel Length
LCTNUT	Low Cost and Triple Node Upset Tolerant
LET	Linear Energy Transfer
LSEDUT	Low-Cost Single Event Double-Upset Tolerant
MC	Monte Carlo
MCE	Muller C-Element
MEP	Minimum Energy Point
MIMCAP	Metal-Insulator-Metal Capacitor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MNDT	Multiple Node Disruption Tolerant
MNU	Multiple Node Upset

MSFF	Master Slave Flip-Flop
n	Subthreshold Factor
NTV	Near-Threshold Voltage
PDK	Process Design Kit
PDP	Power Delay Product
PVT	Process, Voltage, and Temperature
$Q_{ciritical}$	Critical Charge
RAT	Read Access Time
RC	Restorer Circuit
RDF	Random Dopant Fluctuations
RFEL	SEU Resilient and SET Filterable Robust Latch
RHBD	Radiation Hardened by Design
RSNM	Read Static Noise Margin
σ	Standard Deviation
SCL	Self-Correcting Latch
SDT	Separated Dual Transistor
SEDU	Single Event Double Upset
SEED	Soft-Edge Error-Detecting
SEF	Soft Edge Flip-Flop
SEMNU	Single Event Multiple Node Upset
SER	Soft Error Rate
SET	Single Event Transient
SEU	Single Event Upset
SF	Slow Fast
SNTU	Single Node Triple Upset
SNU	Single Node Upset
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random Access Memory
SRC	Self Repair Circuit
SRCE	SNU Resilient Cells
SS	Slow Slow
STI	Shallow Trench Isolation
t_f	Fall Time
t_r	Rise Time

TCAD	Technology Computer-Aided Design
TDFF	Time Dilation Flip-Flop
TDTB	Transition Detector with Time Borrowing
TID	Total Ionizing Dose
TF	Transient Fault
TMR	Triple Modular Redundancy
TNU	Triple Node Upset
TNUHL	Triple Node Upset Hardened Latch
TOX	Gate Oxide Thickness
μ	Mean
μ_0	Mobility
V_{DD}	Supply Voltage
V_{DS}	Drain Source Voltage
V_{GS}	Gate Source Voltage
V_T	Thermal Voltage
V_{TH}	Threshold Voltage
VAFF	Variation Aware Flip-Flop
VTC	Voltage Transfer Characteristic
VLSI	Very Large Scale Integration
W	Channel Width
W_n	Width of NMOS
W_P	Width of PMOS
WAT	Write Access Time
WID	Within-Die
WL	Word Line
WSNM	Write Static Noise Margin

1 CHAPTER

Introduction

Scaling of supply voltage (V_{DD}) and CMOS device geometries significantly improves the energy efficiency of digital integrated circuits (IC's). To design modern energy efficient CMOS circuits, one of the necessary criteria is to operate them in sub/near-threshold voltage (NTV) regime [1], [2]. However, the major concern with NTV operation is that it leads to growing challenges in system variability and reliability [3]-[5]. As V_{DD} reduces, setup and hold times increases while, it degrades the data storing capability. Rising process, voltage, and temperature (PVT) variations in NTV regime increases the worst case timing margins, consequently creating more timing errors and data retention failures [6]-[11]. Due to the scaling of CMOS technology and NTV operation, circuit node capacitance also gets scaled as well [12], [13]. Consequently, the signal charge representing a logic state on a node is also reduced, which makes the CMOS circuit more vulnerable to external noise due to the alpha particles and high energy neutrons, which are originated from packaging materials and intergalactic cosmic rays, respectively [14]-[16]. Therefore, resilient circuit techniques/approaches are necessary in alleviating the performance degradation and data retention failures resulting from PVT variations and external transient noise. The advantage of these techniques is that they automatically detect and correct the errors which occur because of variations and external transient noise in sequential circuits [17]. In this thesis we discuss resilient circuit design techniques to improve the tolerance against PVT variations and external transient noise. In this chapter, we briefly explain the concept of NTV operation and the circuit reliability challenges associated with it. This chapter begins with discussing the benefits of NTV operation, focusing on the trade-offs of energy and propagation delay. Thereafter, a detailed discussion is presented on the sources of variations in modern CMOS technologies. Finally, we discuss the soft error issues in NTV operation.

1.1 Sub/near-Threshold Voltage (NTV) Operation

Today's electronic gadgets require ultra-low power and energy efficient circuit operation. One of the most efficient methods to improve the energy efficiency is to reduce the V_{DD} into the sub/near-threshold voltage regime [18]-[21]. With NTV operation, the V_{DD} is reduced to just

below or near to the threshold voltage (V_{TH}) of the transistors (n-MOSFET/ p-MOSFET). Circuits operating in the NTV regime yields an energy reduction on the order of ~10X at the cost of approximately ~10X reduction in operating frequency, as compares to a nominal supply voltage (super threshold regime) as seen in Fig 1.1 [19], [22].

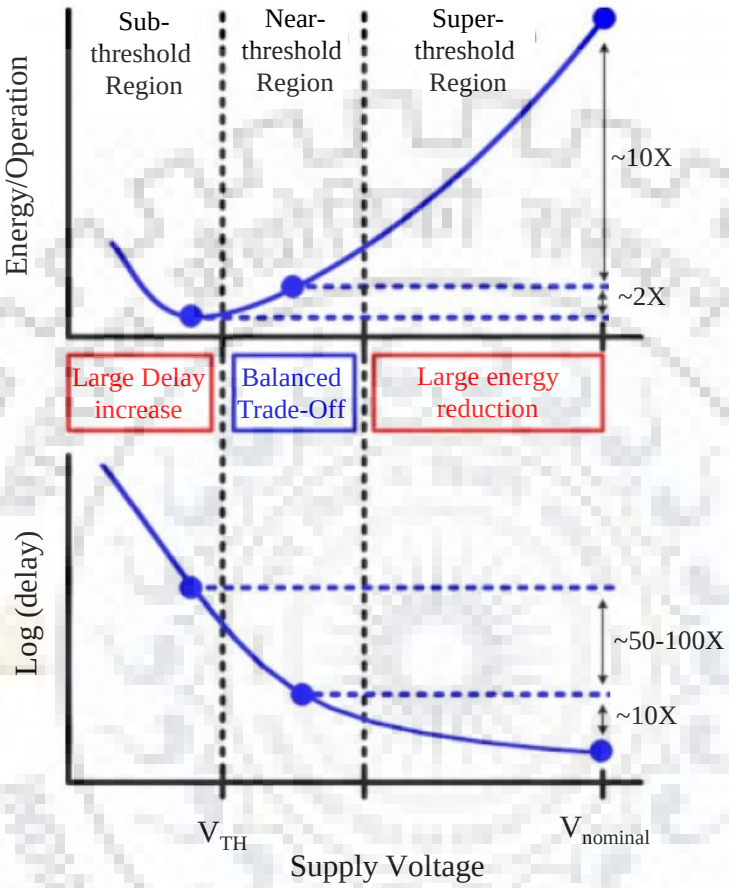


Figure 1.1 Energy and delay in different operating regimes [19].

Sub/near-threshold voltage operation differs from super-threshold operation (nominal supply voltages) mainly because in NTV operation the ON current depends exponentially on V_{DD} and $V_{TH,}$ while at nominal supply voltage this dependence is linear [23]. The variation of the ON current is given in [23].

$$\frac{\sigma_{I_{sub}}}{\mu_{I_{sub}}} = \sqrt{e^{\left(\frac{\sigma V_{TH}}{n V_T}\right)} - 1} \tag{1.1}$$

Where V_T is the thermal voltage, n is the sub-threshold slope factor (directly proportional to V_{DD}), and standard deviation (σ) in the V_{TH} is proportional to (W. L)-1/2. This leads to more variation in the transistor ON current in sub-threshold regime. Therefore, the impact of

variations in sub/near threshold region is more adverse as compared to super-threshold region (nominal supply voltage) [24]-[27]. However, operating circuits at NTV regime is an auspicious technique to optimize the energy efficiency [28], [29]. The design techniques in NTV region would be distinct and challenging from that in the super-threshold region. For reliable operation distinct new circuits/architectures have been proposed at low supply voltages [30]-[36]. In the same direction, more research is required to improve the performance of circuits operating in the NTV regime.

1.2 Near-Threshold Voltage Operation Barriers

Although NTV operation provides excellent energy-delay tradeoffs, it brings its own set of complexities. The NTV operation faces the following major challenges that must be overcome for widespread use; performance variation and reliability issues due to soft errors.

1.2.1 Performance Variations

The first and foremost barrier in NTV operation is variations. In near threshold circuits mainly two types of variations are predominant, which are: Process and Environmental variations [37], [38] as shown in Fig. 1.2. Because of the exponential relationship between transistor current and threshold voltage variations, sub/near-threshold circuit designs are highly sensitive to variations [39].

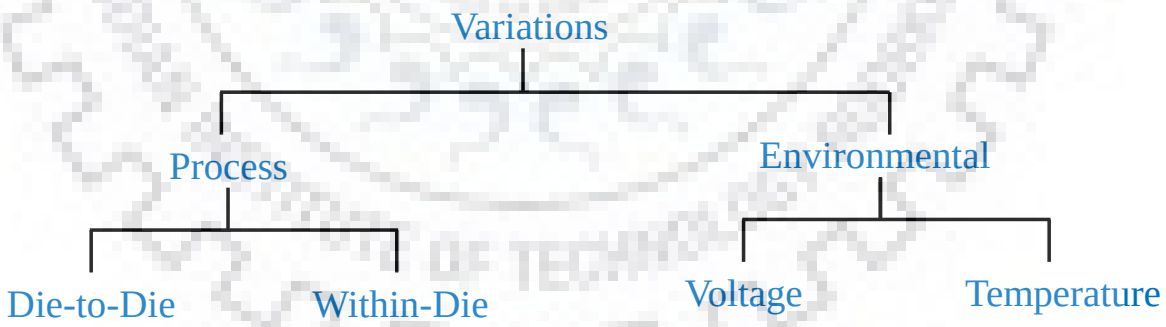


Figure 1.2 Classification of variations.

1.2.1.1 Process Variation

Process variations are occurring due to the imperfect fabrication process. Process variations are spatially correlated and are common to transistors within the same area. This implies that process variations cannot only occur between the wafers, but also between areas within the same wafer. These variations are static in nature, i.e. process variations are fixed after the

fabrication. Random dopant fluctuations (RDF) [40], variations in gate oxide thickness (TOX) [41], and channel length variations [42] are the main sources of process variations that affect the transistor parameters

Process variations are also classified as Die-to-Die (DID) and within-Die (WID) variations. Global or DID variation affects the physical parameter of all transistors equally with in a die. These parameters include layer thickness, channel length (L), channel width (W), body effect, and doping density [43]. Local or WID variation affects the physical parameter of each transistor with in a die differently. RDF is the main source of within-die variation and is caused by the mismatch in the amount of dopants in the channel. As a consequence, identically designed CMOS circuits may have different electrical characteristics. Global variations are only affecting the functionality of the chip but it cannot affect the yield. However, local variations only affect the yield without changing the output of the chip.

The deviation in the physical parameters of the transistor due to variations leads to changes in the electrical characteristics such as the V_{TH} of the transistor. The change in V_{TH} alters the transistor current which leads to variation in the circuit performance and power consumption, due to its exponential dependence [38], [44], [45]. It is shown in [5], [6] that variations in physical parameters of the transistor cause a ~30% variation in the chip frequency and introduce 20 X variation in the chip leakage. Traditionally, analytical models have been used to study the effect of process variations on the circuit performance [46]-[48]. The effect of static process variations at the circuit level can be reduced by changing the threshold voltage of the transistors using body or substrate biasing. Circuit-level techniques such as multiple-V_{TH} [49] and gate sizing [50] have been proposed to minimize the effect of process variations.

1.2.1.2 Environmental Variations

The NTV circuits are also affected by environmental variations, that include supply voltage and temperature variations. These variations are dynamic in nature.

Supply voltage plays an important role in performance and power characteristics of digital circuits. Supply voltage variation is mainly due to IR drop and current derivative noise. Voltage drop or IR drop arises when the current flows on the parasitic resistance of the power grid network [51]. Current derivative noise is caused by time-varying current drawn by the parasitic

inductance of the package leads. Differences in the requirement of active current and leakage current due to IR drop across the chip lead to voltage variations [37].

As the chip density increases dramatically, temperature of the devices also increases and may affect performance dramatically. For every 100^0 C increase in the temperature, failure rate approximately doubles [52] due to the increased interconnect resistance and reduced carrier mobility. An increase in temperature will increase the gate delay at nominal voltages. However, the inverse is observed at low supply voltages. This phenomenon is known as the inverse temperature dependence (ITD). For ultra low voltage designs, an increment in temperature will increase the transistor switching speed. This is because a higher temperature will reduces carrier mobility and threshold voltage of the transistor. In low voltages, the effect of reduction in threshold voltage is dominant as compared to the reduction in carrier mobility. In sub/near-threshold designs, circuit switching speed is directly proportional to temperature. A temperature variation on a die mainly depends on the thermal characteristics of materials, power consumption of blocks, cooling and packaging efficiency.

Summarizing, in the NTV regime, the MOSFET current is exponentially dependent on threshold voltage, power supply, and operating temperature. Consequently, NTV circuit designs display a dramatic increase in performance uncertainty.

1.2.2 Functional Failure due to Soft error

NTV circuits are vulnerable to soft errors such as single node upset (SNU) and single event multiple node upset (SEMNU) [53].The minimum charge required to flip the logic level is lesser in NTV circuits due to the smaller supply voltage (due to NTV operation) and smaller node capacitances (due to an implementation at lower technology node). Consequently, the minimum charge required at a circuit node to change the logic level is getting reduced [12], [13]. Consequently, noise sources, such as electromagnetic interference, radiation-induced voltage transients, chip and board level signal coupling, etc. can easily change the logic state. In a properly designed architecture, voltage transients due to radiations are the major threat to the logic state integrity.

The radiation that influences the electronics architecture mainly consists of alpha particles and high energy neutrons, which are originated from chip packaging materials and intergalactic cosmic rays, respectively [54]. A soft error occurs when these energy particle strike on a

sensitive region of a transistor and generates charge carriers i.e., electron hole pairs (EHP's) in the body [55], [56]. These charge carriers are collected by the drain/source diffusion of the reverse biased drain/source-body junction. This results in the generation of a voltage transient at the node. This transient is known as a single event transient (SET) or transient fault (TF). If the duration of SET is large enough, it can flip the data (from "1" to "0" or from "0" to "1") at the node. When this corrupted logic state is processed by a sequential element (latch/ Flip-flop), it is known as a single event upset (SEU). Consequently, the transistor which is in OFF state starts conducting temporarily and changes the logic level of an affected node. A glitch at the node is thus produced, which results in TF and may result in a system failure or soft error [57]. Moreover, due to the reduction in the magnitude of node capacitance and inter node spacing, striking of a high energy particle may affect multiple nodes, which results in a multiple node upset (MNU) [58], [59].

1.2.2.1 Sources of Soft error

The three main sources of radiation induced soft error in electronics circuits are: i) alpha particles from chip packaging materials, ii) high energy neutrons from intergalactic cosmic rays, and iii) the interaction of thermal neutrons from cosmic ray and ^{10}B in electronic devices containing borophosphosilicate glass (BPSG) [54]. The third soft error source is only be of concern above 180nm technology. In lower process nodes the effect of BPSG has been eliminated during the fabrication process [54].

The first major source of soft error is the alpha particles originated from chip packaging materials. Nucleus of an alpha particle is formed by two protons and two neutrons, and is emitted by radioactive materials like Lead-210 (^{210}Pb) in solder, Uranium-238 (^{238}U), Thorium-232 (^{232}Th), in packaging. Alpha particles are mostly produced by energy less than 10MeV. Consequently, an alpha particle having energy = 1 MeV, can generate approximately 44.5 fC of charge, which is enough to flip the logic state of a memory element [60].

The second major source of radiation induced soft errors is high energy neutrons from cosmic rays. Cosmic rays produce a chain of nuclear interactions with the Earth's atmosphere, and generating neutrons, muons, pions, and protons before reaching sea level. The cosmic neutron flux is directly dependent on neutron energy and the altitude. Consequently, intensity of cosmic rays is different in different cities of the world as shown in Figure 1.3 [61]. As a result, neutron induced soft error rate (SER) of the same electronic circuits will be different in different cities.

A cosmic neutron generates charge through indirect ionization by interacting with silicon nucleus. When a high energy neutron collides with the silicon, it can break the nucleus into multiple fragments, each of which generates charge. The resulting charge density per distance traveled (25-150 fC/μm) is significantly higher than that for alpha particles (16 fC/μm) [54].

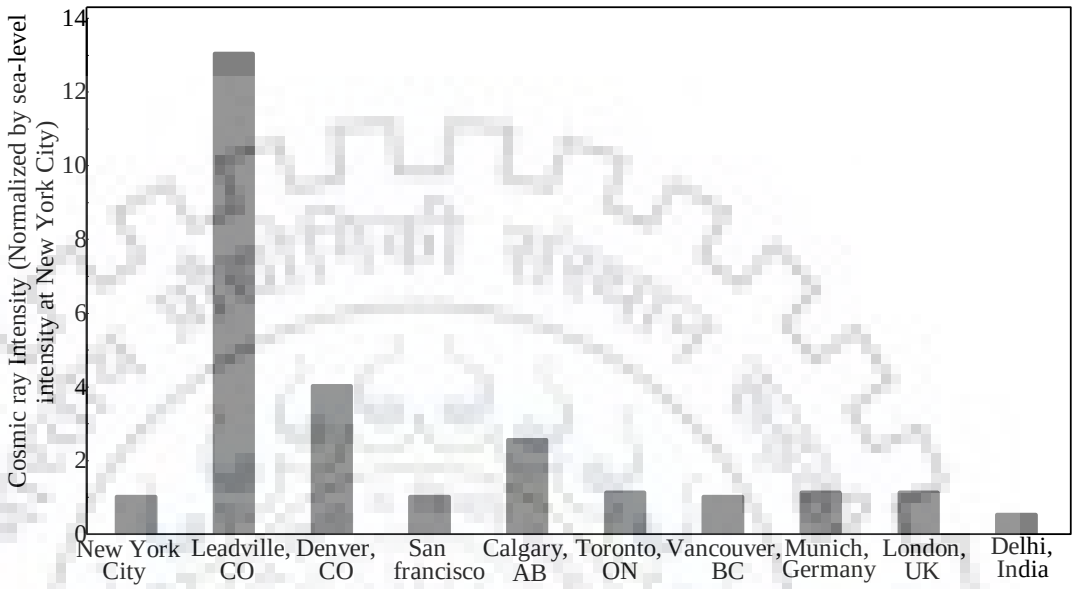


Figure 1.3 Cosmic ray intensity at different cities in the world [61].

1.2.2.2 Basic Mechanism of Soft Error

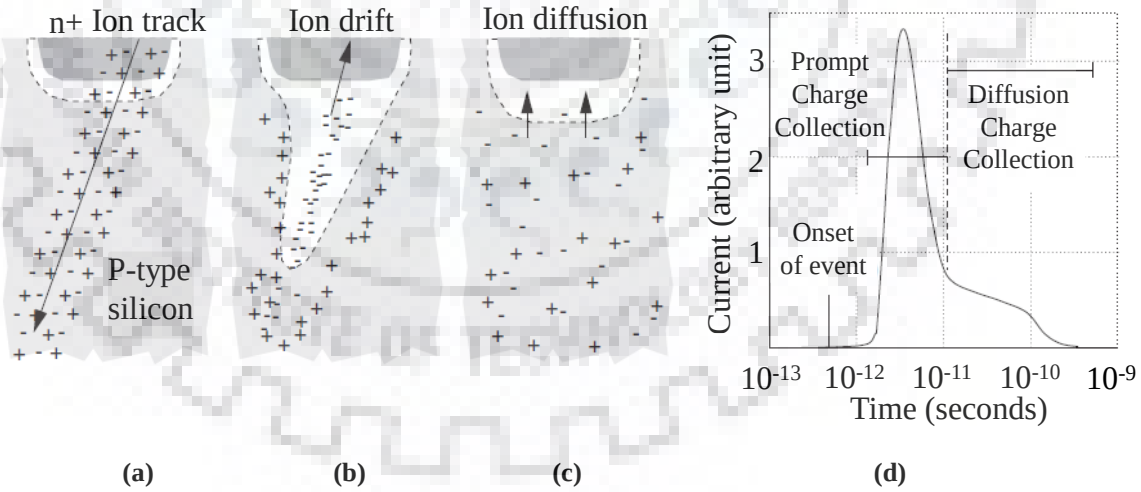


Figure 1.4 Charge generation and collection mechanism from [56].

The most charge sensitive part of the electronic circuits is reverse-biased junction, particularly when the junction is weakly driven or floating. As shown in Fig. 1.4 (a), when a high energy particle strike on the sensitive region of a transistor, a cylindrical charge column with a submicron radius and a high carrier (EHP's) concentration is generated. The quantity of generated charge depends on the linear energy transfer (LET) of the particles, which is a

measure of loss of particle energy per unit length. The generated charge is quickly collected on reverse-biased junction. Due to the electric field EHPs are separated; the electrons (holes) move towards the drain in n-MOSFET (p-MOSFET) and holes (electrons) move towards the substrate of n-MOSFET (p-MOSFET) (please refer Fig. 1.4 (b)). A remarkable feature of this event is the distortion of the depletion region into a funnel shape [62]. This funnel greatly enhances the drift charge collection by extending the depletion region deeper into the substrate as shown in Fig. 1.4 (b). This drift charge collection phase is completed within few tens of picoseconds and is followed by slower diffusion charge collection phase (please refer Fig. 1.4 (c)). Diffusion charge collection process continues until all extra charge carriers have been diffused away from the junction area. These generated and collected charge carriers results in a current pulse (please refer Fig. 1.4 (d)). This current pulse results a SET on the node voltage. The magnitude of the collected charge is depending on the duration and amplitude of the current pulse. If the collected charge is more than a minimum charge, the logic state in a memory element is flipped and SEU or soft error occurs. This minimum charge is called the critical charge ($Q_{ciritical}$).

1.3 Motivation

Due to the PVT variations and soft errors, NTV circuit designers are in a hard dilemma, while achieving reliable designs with maximum energy efficiency. Among different electronic components in every chip, sequential elements (latches/ Flip-Flop/ static random access memory (SRAM)) represent up to 50% of the chip area [63]. Sequential elements, highly affect the chip efficiency, performance and reliability. In addition, the power consumption of the clock network, in latches/Flip-Flop approximately more than half of the total chip power consumption [45]. Therefore, efficient implementation of latches and memory cells is of great importance for energy efficient and reliable integrated circuits design. Conventionally, large design margins are allocated for sub/near-threshold circuits to function in worst-case scenario. However, these worst-case margins severely degrade the performance and increase the power dissipation of a design [64]. Hence, adding these safety margins to handle PVT variations makes the design inefficient for low voltage applications. Several resilient techniques have been presented to address PVT variations [65]-[77]. The advantage of these techniques is to automatically detect and correct the errors that occur because of PVT variations in worst cases. However, these techniques detect error when data transition occurs after the edge of the clock signal, these techniques do not handle the setup time violations.

As discussed earlier, the minimum charge on the sensitive node is called the critical charge ($Q_{ciritical}$). This $Q_{ciritical}$ exhibits an exponential relationship with the soft error rate. Several critical charge models have been presented to address this requirement [78]-[87]. However, these models are derived only for SRAM cells. In particular, modeling and analysis of soft errors due to SEU in sub/near-threshold latches is also vital. Therefore, an accurate model to estimate the $Q_{critical}$ of a static D latches in sub/near-threshold regime is necessary. This $Q_{critical}$ model will enable circuit designers to estimate and optimize the $Q_{critical}$ and hence the SER at the schematic stage. Since the PVT variations can lead to variation in SER across the fabricated chip. This information can help the process designer to fine-tune the process in order to minimize the SER in fabricated chips.

When a static D-latch or 6T SRAM cell is operating in near threshold voltage, it becomes more susceptible to SEUs because of reducing supply voltage, increasing densities, and decreasing critical charge. Therefore, if we want to design ultra-low power memory elements in reliability critical or space applications, techniques to tolerate SEU should be applied. Error Correction Code (ECC) is a traditional approach to solve this problem. However, when multi-bit upset due to SEU occurs, ECC may not be suitable solution because the cost of complicated coding and decoding technique for multi-bit correction is too high. It will bring high power consumption and large overhead, as well as degrade the performance of the circuit. To overcome SEMNU issues, radiation-hardened by-design (RHBD) techniques are explored in [88]-[114]. The advantage of these techniques is increased immunity against soft errors in worst cases. However, the cost in terms of power, speed and area for protecting SRAM cells from a SEU is significant. Therefore, energy efficient, low cost and radiation hardened memory element (latches/ SRAM cell) designs are indispensable in NTV regime.

1.4 Objectives

From the above discussion, it is imminent that innovative NTV sequential circuit design techniques that not only overcome timing errors but also handle soft error issues effectively are essential. These sequential circuit designs which have reasonable area overhead as compared to conventional approaches are in great demand. In this work, the impact of PVT variations and soft errors on sequential elements' functionality/performance is discussed. The twin objectives of this research are to design PVT variation aware sub/near-threshold self correcting

latches/SRAM and address the radiation-induced data retention failure issues. The main objectives of the thesis are:

1. To develop a methodology that corrects the faults due to timing violation caused by variations in data-paths and sequential elements automatically, thereby lowering PVT variation induced performance degradation.

2. To develop a physics-based variability aware methodology to estimate the critical charge of an NTV static D-latch without losing the accuracy for different fan-out loads, power supply voltages, and temperatures. Using this model, we devise a methodology to estimate the critical charge using a few DC simulations and a single transient simulation program with integrated circuit emphasis (SPICE) simulation for a given process design kit (PDK). This is an end to end method to include an accurate estimation of the critical charge for latches in NTV standard cell library characterization.

3. Design a highly reliable, low cost and energy efficient radiation hardened latch design for low voltage applications.

4. Design a novel energy efficient and higher single event multiple node upset tolerant SRAM cell designs for space applications.

1.5 Organization of the Thesis

This thesis is based on the objectives discussed above. The thesis consists of seven chapters. Each chapter begins with a brief introduction to the concerned problem and motivation behind the study. Subsequently, the simulation framework, analysis, and results are discussed in a lucid manner. A brief discussion of each chapter is presented below:

Chapter 1 provides the overall philosophy of the thesis. It provides the motivation and outline behind this research and the agenda for choosing the objectives of the work. Problem statement, objectives of the thesis and the thesis organization is presented in this chapter. It also introduces the CMOS near threshold voltage regime operation which has been considered the operating region in this thesis.

Chapter 2 provides a comprehensive literature review on NTV techniques to incorporate timing errors due to variations in CMOS circuits. Single Event Upset due to transient fault,

Double Node upset (DNU) and triple node upset (TNU) due to charge sharing, modelling of $Q_{critical}$ of a conventional static D-latch are also discussed. Moreover, existing design methodologies to optimize circuit performance considering circuit level variations due to NTV are reviewed.

Chapter 3 presents a novel energy efficient self-correcting latch (SCL). The proposed technique corrects the faults due to timing violation caused by variations in datapaths and sequential elements automatically, thereby lowering PVT variation induced performance degradation. Our technique employs Inverse Narrow Width Effect (INWE) in designing the self-correcting latches to reduce performance variability. We validate the proposed methodology on several ISCAS'89 benchmark circuits and 74X series circuits.

Chapter 4 presents a physics based semi-analytical model to estimate the critical charge $Q_{critical}$ of a static D-latch as a function of its fan-out load and supply voltage. The model describes the critical charge in terms of the supply voltage and transistor level parameters. The model can be used while considering PVT variations. We validate the proposed model on STMicroelectronics 65-nm CMOS technology node for different process corners. Based on this model, we propose a procedure to estimate the critical charge using a few DC simulations and a single transient simulation. This method results in an estimate of the latch's critical charge for different values of fan-out load and supply voltages.

Chapter 5 presents high performance energy efficient radiation hardened latch designs in NTV regime. In the case of a transient fault, the proposed latches, mask the fault by a clocked Muller- C and memory elements based restorer circuit. In the transparent mode data passes through a fast and efficient path. Inverse Narrow Width Effect (INWE) is used to further improve the performance of the proposed latches at the layout level. The proposed radiation hardened latches shows a higher performance and also a better robustness against soft error occurring due to transient faults, without power consumption overhead of the earlier techniques. We validate the better SEU tolerance and improved performance of the proposed latch in STMicroelectronics 65-nm and TCAD calibrated 32-nm CMOS technologies.

Chapter 6 presents two novel energy efficient radiation hardened by design SRAM cell designs. We validate the proposed SRAM cells in STMicroelectronics 65-nm and TCAD calibrated 32-nm CMOS technologies. The proposed SEU hardened memory cell shows better

performance (in terms of read and write access time) and also more robustness against SEU, without power consumption overhead of the earlier techniques.

Chapter 7 concludes the thesis. The conclusions of the thesis are drawn based on the obtained results. The future scope of the work is also presented in this chapter. The thesis ends with a complete bibliography.

2 CHAPTER

Literature Survey

In the Introduction chapter, we discussed the main challenges in near threshold circuit design. This chapter presents a comprehensive literature survey of the present and past research work that is closely related with the work presented in this thesis. The problem statement of this thesis is mainly focused on addressing the timing and soft error issues in the near threshold voltage (NTV) circuit's design, while maintaining their inherent energy-efficiency. Therefore, the works in this thesis can be classified into four parts: NTV error detection and correction (EDC) techniques (Section 2.1), critical charge modeling for static D-latch (Section 2.2), radiation hardened by design (RHBD) techniques for static D-latch (Section 2.3) and mitigation of soft error in static random access memory (SRAM) cells (Section 2.4). Finally, section 2.5 summarizes the chapter by identifying the technical gaps that we addressed in this thesis.

2.1 NTV Timing Error Detection and Correction (EDC) Techniques

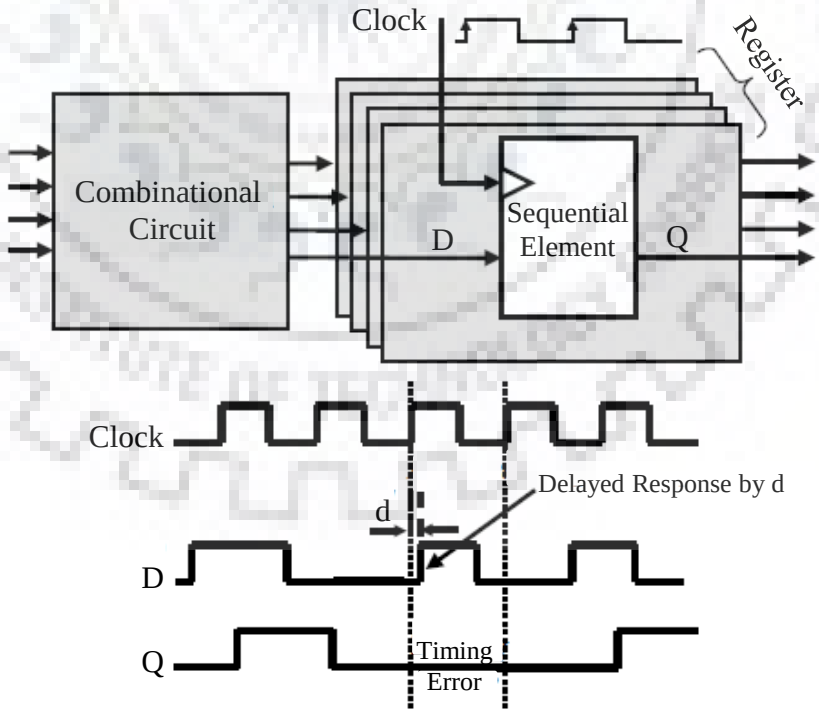


Figure 2.1 Conceptual timing diagrams in worst and nominal conditions [64].

Timing error in combinational circuits leads to delayed responses on its output node. Figure 2.1 shows that, within the presence of variations, the input data (D) arrive after the rising edge of the clock signal. Consequently, the sequential element will capture an incorrect data and a time failure error occurs. Traditionally, large design margins are allocated for NTV circuits so that the circuits can function in worst-case scenario. However, circuit designing with huge design margins results in sub-optimized designs. Therefore, the challenge to achieve a maximum yield without using large timing margins is daunting.

To overcome this issue, error detection, correction and prevention techniques are used. Employing these techniques results in high performance, while the errors encountered due to variations in worst cases are automatically detected and corrected. Various timing error detection techniques have been presented in the open literature [65] – [77]. The advantage of these techniques is to automatically detect and correct the errors which occur because of variations in a data-path in worst cases. Most of the above methodologies cited in literature are aimed to generate a post-silicon warning when process voltage and temperature (PVT) variations cause timing violations**.** The ICs which generate these warnings need external intervention (such as increasing the supply voltage V_{DD}).

Razor I circuit [65] detects errors by using an error detecting latch (shadow latch) and corrects timing errors via architectural replay. However, in Razor I, if there is a setup time violation in the datapath, the error detection may not happen due to metastability of the Flip-Flop. Soft-Edge Flip-Flop (SEF) is presented in [66]. The basic principle of the SEF is to delay the master latch's clock signal so that a transparency window can be made instead of a hard boundary for sampling the data. By creating a transparency window, SEF increase the hold time. The SEF does not require any error correction operation, but it cannot instruct a controller to scale the voltage and frequency of the circuit. Consequently, it will have a very large window of transparency. In Razor II technique [67], a signal transition detector is used to make the Flip-Flop detect timing errors and do corrections. In Bubble Razor technique [68], a cycle prolongation is done in both directions of data propagation in pipeline. The main principle of bubble razor is that when timing violations occur, it broadens the operating clock cycle. However, both Razor II and Bubble Razor techniques require a huge overhead of additional circuitry for changing the clock cycle time dynamically and also increase the circuit area and clock power dissipation.

In [69], a Transition Detector with Time Borrowing (TDTB) and Double Sampling with Time Borrowing (DSTB) methodologies are proposed which are based on the principle of time borrowing. DSTB has the same issues as in the Razor I technique. In TDTB the problem of meta-stability in the main data-path's Flip-Flop was solved, however, meta-stability can occur in the error path's Flip-Flop. In [70], an error masking technique based on generic monitoring is proposed. The main drawback of this is that it is incapable to capture design characteristics, consequently giving a large error in the measurements. Therefore, the delay estimation using generic monitors is less accurate. Variability has been handled by all existing warning circuit techniques by either changing cycle time dynamically or by increasing supply voltage. In [71], a variation aware Flip-Flop (VAFF) is proposed; the VAFF generate an error signal when its input and output logic levels are different after the rising edge of the clock signal. One of the major problems in VAFF is that in case of setup time violation the final output may be erroneously chosen while in case of no setup time violations huge hold time is required. In addition, its comparator results in delay and power consumption overhead. In error resilient Flip-Flop (ERFF) [72], a late detector detects input data transition causing timing violations. The late signal converts the Flip-Flop into a latch thereby increasing the timing window dynamically. One of the major problems in ERFF technique is the possibility of race around condition because of the conversion of the Flip-Flop into a latch whenever there is late signal generated by the late detector. In addition, ERFF cannot handle meta-stability issues resulting from setup time violations.

In [73], an error detecting and correcting technique based on bit flipping concept is proposed. The technique gives the timing error tolerance by using two XOR gate and an additional memory element for timing error correction. Output of XOR gate is stored in a pulsed latch. An error is detected by comparing the input and output of the Flip-Flop, and the output is stored in a metastability detector. The bit flipping Flip-Flop incurs a huge overhead of additional circuitry and also increases the circuit area and power dissipation. The Time Dilation Flip-Flop (TDFF) is presented in [74]. The TDFF employs a XOR gate and a 2:1 multiplexer per system Flip-Flop to monitor the timing errors. In TDFF, the XOR gate compares input data and output data of the main Flip-Flop to generate an error signal. While the 2:1 MUX with the feedback loop forms a shadow latch that captures delayed correct data for error rectification. The large extra logic gates occupy high silicon area and create performance degradation. The main

drawback in TDFF technique is the possibility of system failure when the output signal of the Flip-Flop enters in a metastable state.

In [75], Soft-Edge Error-Detecting (SEED) Flip-Flop is presented. The SEED Flip-Flop observes through monitoring the two floating nodes and generates an error signal when a violation occurs. The SEED Flip-Flop uses a variation tolerant logic, which delays the edge of the clock signal of master latch by a small amount relative to the clock signal of slave latch. This delay creates a transparency window. The SEED Flip-Flop require a huge overhead of additional circuitry for changing the clock cycle time and power supply dynamically and these also increase the circuit area and clock power dissipation. In [76] error masking flip-flop (EMFF) is presented. The EMFF consists of a traditional Flip-Flop with modified input inverter, a correction inverter and a controlling generation circuit. The modified input inverter is an inverter followed by a transmission gate. The controlling generation circuit works as the comparator to compare the input and output signals. Therefore, if the input and the output signals are not same, a timing failure error is generated. This generated error signal would activate the correction inverter to rectify the error. The main drawback of EMFF is the extra controlling signals, which makes the EMFF technique complicated. The iRazor technique is presented in [77] that only take a three transistor overhead as compared to a conventional D Flip-Flop. The iRazor technique utilizes a D-latch with asynchronous reset signal and an error detection circuit. There is a 3-transistor current detector in the error detection circuit, which indicates that after the rising edge of the clock signal the latch is drawing any transistor on-current or not. Therefore, error detection circuit effectively detecting the signal switching at the input of the iRazor. The iRazor technique needed extra signals, such a control signal for the tail transistor and a reset signal for the latch circuitry, which complicates the iRazor technique.

2.2 Critical charge models to predict the circuit SEU tolerance

As mentioned earlier, if the total charge deposited by the striking of high energy particle at the sensitive node, is more than a minimum charge, the stored data is flipped in memory elements. This minimum charge on the sensitive node is called the critical charge ($Q_{ciritical}$), which can be used as a parameter to measure a latch's susceptibility to SEU or soft errors [78]-[80]. $Q_{ciritical}$ have an exponential relationship with the soft error rate (SER) [81]. To design a latch/Flip-Flop's $Q_{ciritical}$ must be high enough to limit the SER. In particular, sub-threshold/ near-

threshold latches/ Flip-Flop are susceptible to SEU as discussed earlier. Therefore, modeling and analysis of soft errors due to SEU in sub-threshold/ near-threshold latches is vital.

Traditionally, $Q_{ciritical}$ is estimated by injecting a noise current pulse at the susceptible node and then integrating the current that is able to flip the stored data. Several critical charge models have been presented to address this requirement [82]-[86]. However, these models are derived only for SRAM cells. All of these models express the same opinion in the qualitative definition of $Q_{ciritical}$, while, they have different opinion in the quantitative explanation. Authors in [83] proposed an analytical technique to estimate $Q_{ciritical}$ in terms of transistor parameters and injected current's pulse amplitude and duration. The most noteworthy characteristic of this model is that it considers the SRAM cell's dynamic stability response when a particle strikes. However, the estimated value of $Q_{ciritical}$ in this model shows 11% maximum error with SPICE simulations as reported in [83]. Authors in [84] proposed an analytical model to calculate the $Q_{ciritical}$ for super-threshold SRAM cells. Despite the accuracy of this model in calculating the $Q_{ciritical}$, this analytical model mainly depends on SPICE simulations and can be used only for super threshold region. Authors in [86] proposed an analytical model to estimate the $Q_{ciritical}$ for sub-threshold SRAM cell, accounting for both local and global variations. This model is further approximated to give more design insights on the impact of PVT variations on the $Q_{ciritical}$. However, this model entails complex mathematical equations that restrict the utility for a circuit designer. However, most of the researchers employed Monte Carlo (MC) analysis to calculate the critical charge [87]. But MC analysis is not a convenient solution to calculate the critical charge because it is very time consuming and also not scalable with CMOS technology [86] and circuit size. For every new CMOS technology node MC analysis has to be carried out to calculate the $Q_{ciritical}$ variability. In literature, models are derived for the estimation of $Q_{ciritical}$ for SRAM cells only. To the best of our knowledge there is no model to estimate the critical charge of a static D-latch in sub/near-threshold regime. The presented models are not used in the estimation of $Q_{ciritical}$ for static D-latch, because in the hold mode there is a transmission gate in the feedback path of a latch.

Therefore, how to estimate the critical charge of a static D-latch in the near threshold regime without losing the accuracy for different fan-out loads, power supply voltages and temperatures ?" is not properly addressed in literature.

2.3 Mitigation of Soft Errors in Static D-Latch

Radiation-hardened-by-design techniques provide best solution to minimize the soft error rate (SER). In the last decade, researchers have mostly focused on the radiation hardening for Flip-Flop's [88] - [90], latches [91] – [114], memory cells [115] – [130], and CMOS RF integrated circuits like oscillators [131] – [134] using RHBD techniques like multiple-modular redundancy, temporal redundancy, and so on. Radiation hardened techniques for static D-latch can be classified into three categories:

(1) Single node upset tolerant technique
(2) Double node upset tolerant technique
(3) Triple node upset tolerant technique

In the following sub-section, we discuss radiation-hardened techniques for static D-latch.

2.3.1 Single node upset tolerant technique

The triple modular redundancy (TMR) latch is used in [91], [92]. One effective solution to enhance radiation tolerance at circuit level is to replace each latch of the system by a set of three latches i.e. TMR-latch. A TMR latch consists of three identical latches and a voting circuit. TMR-latch can tolerate the transient fault if SEU affect one of the three identical latches. Therefore, TMR latch provides complete transient fault immunity. Although this technique is highly reliable and widely used in space applications, but it always incurs huge area overhead and power dissipation. In [93] separated dual transistor (SDT) is proposed. The SDT latch consists of two Muller C-elements (MCE), which are connected by a transmission gate. A MCE is a state holding element and its function is same as an inverter, only if both of its inputs are at same logic level. The SDT latch having two data inputs namely, D1 and D2. Input data D2 is delayed version of input data D1. Input data D1 is not equal to D2 in the case of erroneous inputs causing MCE on output side to disconnect from the supply voltage. The pervious state of the output signal is stored at the output until the both inputs (D1 and D2) are equal. The SDT latch is vulnerable to SEU at the output node. In [94] two radiation hardened latches namely SIN-LC and SIN-HR are presented. In the error free operation of the SIN-LC latch, the data propagates from input node to output node through the MCE. A feedback from the output node to the intermediated nodes N1 and N2 is provided via the two inverters (in positive phase of clock signal). When a transient fault occurs at one of the susceptible nodes,

the output node does not flip; because the MCE retains its previous state. However, the major drawback of the SIN-LC latch is its incapability of tolerating the SEU which occurs at the output of the latch. There is another problem with SIN-LC latch is the electrical contention between the input node and the output node. To avoid electrical contention SIN-HR is design. However, the susceptibility to soft errors remains at the output node.

In [95] Feedback redundant single event upset tolerant (FERST) latch is proposed. To overcome the SEU effects, FERST latch uses a redundant feedback path with MCE. When a transient fault occurs, both the inputs of the MCE's are different; therefore, the outputs of the MCE's remain unchanged. Consequently, the output of latch will not be erroneous. Soft error correction using a duplication technique is proposed in [96]. In this technique, two identical latches are used with MCE. In case of both the inputs have different logic values, the MCE retains the previous logic value at its output. These latches suffer from performance penalty and area overhead. In [97] Dual Interlocked Cell latch (DICE) is proposed. It is a well known latch because of its SEU tolerance ability. The DICE latch consists of two cross- coupled latches, which are used to inter-lock each other to a stable value. When an alpha particle strikes on any internal node, the node can easily be restored the original value by the state stored on the other three internal nodes. However, in DICE latch if the alpha particle energy is high enough, a SEU fault may happen [98]. The radiation hardened latch proposed in [99] consists of two cross-coupled structures. These structures form negative feedback paths. During the transparent mode, feedback paths of the latch are cut off to improve the circuit performance in terms of speed. Negative feedback helps to recovers the flip state caused by transient fault, when the latch works in the hold mode. However, in the latch if the alpha particle energy is high enough, a SEU fault may happen. Moreover, the latch also suffers from area penalty.

In [100] high performance SEU tolerant (HPST) latch is proposed. The HPST Latch consists of two MCE's, and one clocked MCE. In the hold/latch mode clocked MCE blocks the soft error. The HPST latch uses multiple MCE and redundant feedback paths to masks the soft error issues. In [101] DICE latch with feedback transistors (DICE-FBT) latch is proposed. The DICE-FBT Latch improves the SEU tolerance by adding four feedback transistors in the feedback path of the DICE latch. These feedback transistors are enabled during the transparent mode of the latch and OFF during the hold mode. By using the feedback transistors in DICE-FBT latch improves the soft error tolerance by increasing the feedback loop delay in the latch mode. In [102] SEU resilient and SET filterable robust (RFEL) latch is proposed. The RFEL

latch uses a triple mutual feedback CMOS structure to handle single node upset issues due to the high energy particle striking. The RFEL latch consists of the input-split Schmitt trigger, two MCE's, two inverters and four transmission gates. The radiation hardened latch proposed in [103] consists of a static D-latch and an error detection circuit. The Latch in [103] is mitigating the effect of soft error through an error detection circuit. The error detection circuit can detect the corrupted state in the latch and corrects the faulty output state. These latches also suffer from performance penalty. The radiation hardened latch proposed in [104] consists of a static D-latch and multiple MCE's. The latch presented in [104] utilize the 3-input clocked MCE at the out output stage to mitigate the soft errors due to transient fault. The latch also suffers from area overhead and power dissipation due to the use of multiple MCE's.

2.3.2 Double node upset tolerant technique

The multiple node disruption tolerant (MNDT) latch is based on the use of redundant nodes [105]. MNDT latch comprises eight MCE's and these MCE's drives eight internal nodes. If both inputs of a MCE are corrupted due to soft error, the affected output is not propagated as input on any of the MCE's that drives the corrupted nodes. In this way the corrupted nodes are restored, consequently, output of the affected MCE is also restored. However, this approach incurs large area overhead. The double node charge sharing (DNCS) latch [106] consists of a six stage feedback loop, which is composed of 2-input MCE. In this latch a 3-input MCE is used at the output stage to retain the data. If a TF occurs at any two nodes of the feedback loop, at least one of the inputs of the 3-input MCE remains uncorrupted. Consequently, output of the latch retains the correct state. DNCS latch effectively tolerates DNU but requires a large area and increases power dissipation. The circuit and layout combination technique (CLCT) latch is presented in [107]. The CLCT latch is based on the TMR latch. The CLCT latch consists of typical DICE latch and a conventional static D-latch. The output of both latches are connected to a 3-input MCE. Further, using the layout technique, the CLCT latch effectively tolerates DNU at the cost of area and power dissipation overhead. In [108] highly robust double node upset tolerant (HRDNUT) latch is presented. The HRDNUT is based on three cross connected memory cell loops connected to three MCEs. The HRDNUT latch can tolerate DNU but at the cost of performance penalty. The double node upset resilient latch (DNRUL) [109] consists of a set of three transmission gates and three interconnected SNU resilient cells (SRCEs). Each SRC consists of, two clock-gating (CG) based on 2-input MCE's, a normal 2-input MCE, and two inverters. In a case when two nodes are affected by DNU, output will not be affected

because all the three SRCE are SNU resilient. The DNRUL latch incurs a huge area overhead and power dissipation due to SRCE. The dual input inverter radiation tolerant (DIRT) latch is proposed in [110]. The DIRT latch comprises twelve dual input inverters and 6 transmission gates are used to store the data in the latch. The DIRT latch improves DNU tolerance by using a dual-input inverter. The DIRT latch effectively mitigates the DNU but incurs large area due to the multiple dual-input inverters. In [111] Low-cost single event double-upset tolerant (LSEDUT) latch is presented. The LSEDUT latch consists of a set of five transmission gates, a 3-input MCE, and a triple path dual interlocked based storage cell. The storage cell comprises of three CG-based 2-input MCEs pairs. In the case of a DNU, the storage cell holds a source of uncorrupted state that recovers the state at the affected node. The LSEDUT latch suffers from performance penalty and area overhead because of the storage elements.

2.3.3 Triple node upset tolerant technique

In [112] triple node upset hardened latch (TNUHL) is presented. TNUHL latch consists of five inverters, four 5-input MCEs, one 4-input MCE, two 3-input MCEs, and one 2-input MCE to construct interlocked feedback loops. The triple node upset tolerant latch is proposed in [113]. The latch consists of four DICE cells and 5-input clocked-MCE to provide single event double upset (SEDU) tolerance and single node triple upset (SNTU). The latch is based on the TMR configuration, its structure is divided into three parts. All DICEs in the latch are connected together as a circle. One node from each DICE cell is connected to 5-input clocked MCE. The basic principle of this latch is if any of the three DICE cells of the latch are affected due to soft error, in this case corrupted node is blocked by the 5-input clocked MCE because the logic state of forth DICE cell is not corrupted. The Low Cost and triple node upset tolerant (LCTNUT) latch [114] consists of a storage module and three 2-input C-elements. The storage module of the latch consists of four transmission gates, CG based input-split inverters, and input-split inverters to maintain the correct data. These latches [112]-[114] effectively tolerate TNUs but at the high cost penalties in terms of power, performance and area due to the use of multiple input C-elements and DICE cells.

In summary, to remedy SNU/DNU/TNU due to soft error in Latch/ Flip-Flop, researchers have proposed techniques with additional circuitry to hold the data. However, additional circuitry adds a huge overhead to the performance in terms of delay and power dissipation. To solve this problem, novel high performance energy efficient TNU tolerant latch in NTV region needs to be proposed.

2.4 Mitigation of Soft Errors in SRAM cell

To mitigate radiation-induced soft errors in SRAM cells, several approaches have been proposed in literature.

Radiation induced soft error tolerant SRAM cell, for space applications with delayed regenerative action by using Metal-insulator-Metal Capacitor (MIMCAP) is presented in [115]. Authors in [116] found that the total ionizing dose (TID) can be mitigated by using reverse body biasing and two edge transistors in the SRAM cell. But afterwards, authors in [117] advised that the guard rings and edge less transistors are not necessary for low voltage operation to enhance TID Hardness. In [118], the optimized methodology for radiation hardened library appreciated such as use of guard rings to reduce SET, minimization of feedback loop, and use of edge less transistors for leakage currents minimization. Robust layouts with respect to soft errors are selected by comparing the sensitivity maps is another interesting method for radiation hardening. In [119] proposed an optimization methodology to improve the SEU tolerance by introducing miller capacitance between the susceptible nodes of the memory cell. In [97], DICE SRAM cell is presented, which is highly reliable and widely used in space applications, however, at the cost of area overhead and power dissipation. The DICE memory cell has smaller (or negligible) ability to tolerate SEMNU. In [120], a Quatro-10T SRAM cell is proposed to mitigate only a 1 to 0 flipping case by employing a negative feedback. Quatro-10T memory cell cannot tolerate SEMNU. In [121], two memory cells are proposed using a stacked structure (NS-10T and PS-10T), however, these SRAM cells only provide partial SEU tolerance. These memory cells cannot mitigate SEMNU. Radiation tolerant 12T SRAM is proposed in [122], overcomes the need of separate well for PMOS transistor. In [123], an RHBD-12T SRAM is proposed by making a tradeoff with increased area overhead employing the shallow trench isolation technique. This SRAM cell mitigates SEMNU at the cost of larger area. In [124] Low power radiation hardened 13T SRAM cell using a dual driven separated feedback is proposed. A 10T SRAM is presented in [125] improving the SEU tolerance at the cost of read and write access time. Moreover, 10T memory cell cannot recover from SEMNU. In [126], a circuit level RHBD 12T SRAM cell is proposed to improve the SEMNU tolerance. In [127] 12T radiation hardened SRAM cell (RHSC) is proposed. RHSC-12T cell is based on Quatro10T uses two n-MOSFET to prevent logic “0” to logic “1” flipping at output nodes of the cell. In [128] a 14T radiation-hardened with speed and power optimized for space application is proposed. RSP-14T SRAM cell improve the SEU tolerance by using

source isolation technique. These SRAM cells suffer from a performance penalty, area overhead and lower stability.

Therefore, an RHBD CMOS SRAM cell with improved energy-efficiency, higher reliability, and area-efficient properties is necessary to offer appropriate design for reliability systems in the sub/near-threshold regime.

2.5 Technical Gaps

In the light of the literature survey, it is hence noted that circuit designing in NTV regime is recently gaining a high attention. However, NTV circuits have always been sensitive to PVT variations and susceptible to soft error as discussed earlier. To resolve these issues, several resilient circuit techniques have been reported in literature but they have some limitations. In this respect, following are some technical gaps required to be resolved:

- In most of the timing error resilient techniques where error is found to occur, either authors decrease the operating frequency or increase the power supply voltage (V_{DD}). Consequently, it results in either performance degradation or increase in power dissipation. There is no optimal solution for self-detection and correction at fixed voltage and operating frequency is available.
- Soft error rate exhibits an exponential relation with critical charge of a static D-latch. An accurate model to estimate the critical charge of a static D latches in sub/near-threshold regime is necessary. This critical charge model will enable circuit designers to estimate and optimize the critical charge and hence the soft error rate at the schematic stage. This model is an end to end method to include an accurate estimation of the critical charge for latches in NTV standard cell library characterization. This model provides information that can help the circuit designer to fine-tune the process in order to minimize the soft error rate in fabricated chips.
- To remedy soft error issues in storage elements, researchers have proposed techniques with additional circuitry to hold the data. However, additional circuitry adds a huge overhead to the performance in terms of delay and power dissipation. It would be interesting to carry out work in the area of cost effective solution for radiation hardened recovery circuit. This circuit would be helpful in providing fault free outputs of latches in the radiation affected working environment.

- SRAM cells are also vulnerable to soft error due to their high packing density and the relative lack of transient masking mechanisms. A high energy particle strike directly affects a SRAM cell and often the neighbouring cells by changing the stored data in these cells. The changed values remain stored until the cells are rewritten. In literature several SRAM cells are presented those provided radiation hardness at the cost of area, delay and power dissipation overhead. Therefore, an energy-efficiency CMOS SRAM cell with higher reliability against radiation-induced soft error is necessary. Which offer an appropriate design for reliability systems in the sub/near-threshold regime.

Through this thesis we will address above-mentioned technical gaps.

3 CHAPTER

Energy Efficienct Variation Aware Self Correcting latch

3.1 Overview

Power dissipation is a prime concern in sub-nanometer VLSI regime and, therefore, operation at sub/near-threshold regime has gained importance. However, though energy efficient, a system performance/functionality is at stake, because of the increase in the variability in near-threshold (NTV) regime. Reduction in the power supply voltage in modern CMOS technologies, affect circuit's noise margins and reliability [135]. Therefore, the challenge to achieve a maximum yield without using large timing margins is daunting. To overcome these issues, resilient circuit approaches are important in alleviating the performance degradation resulting from process, voltage, and temperature (PVT) variations. All reported techniques detect error when data transition occurs after the edge of the clock, these techniques do not handle the setup time violations. This chapter presents an energy efficient and resilient circuit design approach using a novel self correcting latch. The proposed technique corrects the faults due to timing violation caused by variations in data-paths and sequential elements automatically, thereby lowering PVT variation induced performance degradation. Our technique employs inverse narrow width effect (INWE) [136] in designing the self-correcting latches to reduce performance variability. In this technique INWE is used to realize devices which have equal gate capacitances and different current drives. We validate the proposed methodology on several ISCAS'89 benchmark circuits and 74X series circuits [137]. Simulation results show that by employing the proposed methodology, an average improvement of ~ 20%, 10%, and 4.85% in delay, power delay product, and layout area, respectively, over previous resilient methodologies can be achieved.

The main contribution which is offered by the proposed technique is that it does not require a change in V_{DD} or clock cycle time when timing violations occur. It dynamically changes the latch setup time by using layout techniques exploiting INWE. The technique predicts a setup time violation and dynamically reduces the data to output (D-Q) delay of the latch. This is different from the earlier techniques since they detect an arrival of Flip-Flop's input data after its clock edge.

The chapter is organized as follows: Section 3.2 describes the proposed self correcting latch (SCL) technique. Section 3.3 discusses our simulation setup. The validation of our technique on several ISCAS'89 benchmark circuits is discussed in Section 3.4. Section 3.5 summaries the chapter.

3.2 Proposed Self Correcting Latch

3.2.1 Principle of the proposed Self Correcting Latch

The block diagram, the schematic, and the layout of the proposed self correcting latch (SCL) technique are shown in Fig. 3.1, Fig. 3.2 and Fig. 3.3, respectively. The circuit consists of a conventional data launching latch, a datapath, a data receiving latch, including two transmission gates, and a self repair circuit (SRC). The proposed SCL technique is transparent in the positive phase of the clock cycle. As shown in Fig. 3.4, in the case of timing violations of the delayed signal D, the proposed latch can detect the violation and correct it.

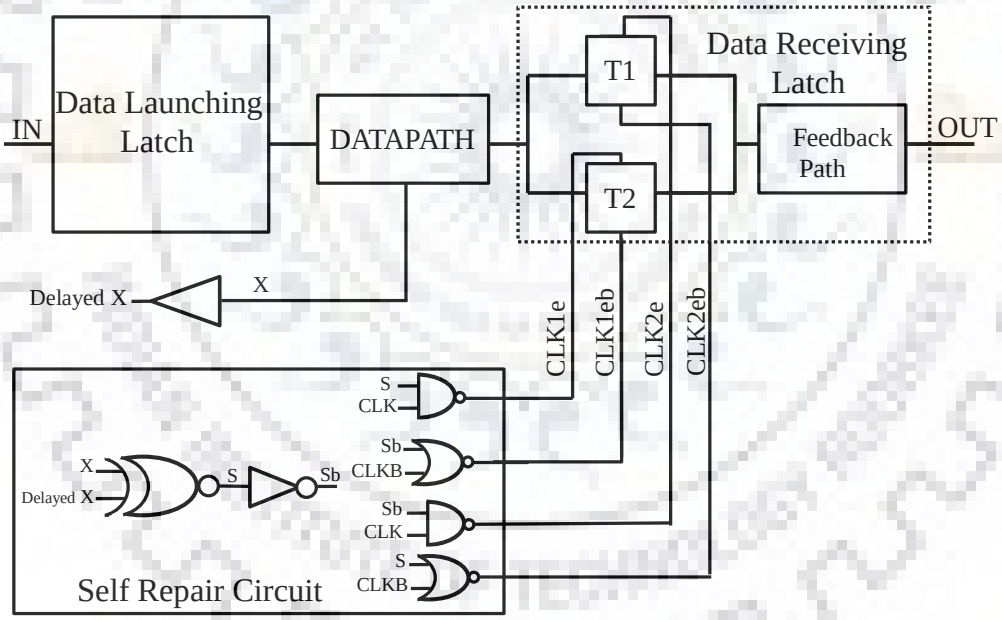


Figure 3.1 Block diagram of proposed SCL technique consists of a conventional data launching latch, a datapath and a data receiving latch.

The basic principle of the proposed SCL technique is as follows: Consider the case in which the total delay of a data launching latch and the following data-path violates the setup time of the data receiving latch (please refer to Fig. 3.2) due to PVT variations; in that case our SCL technique automatically corrects the error by using a delayed version of the input clock signal (i.e. CLK2e and CLK2eb). The advantage of our technique is that the effective clock to Q delay does not increase.

3.2.2 Operation of the proposed Self Correcting Latch

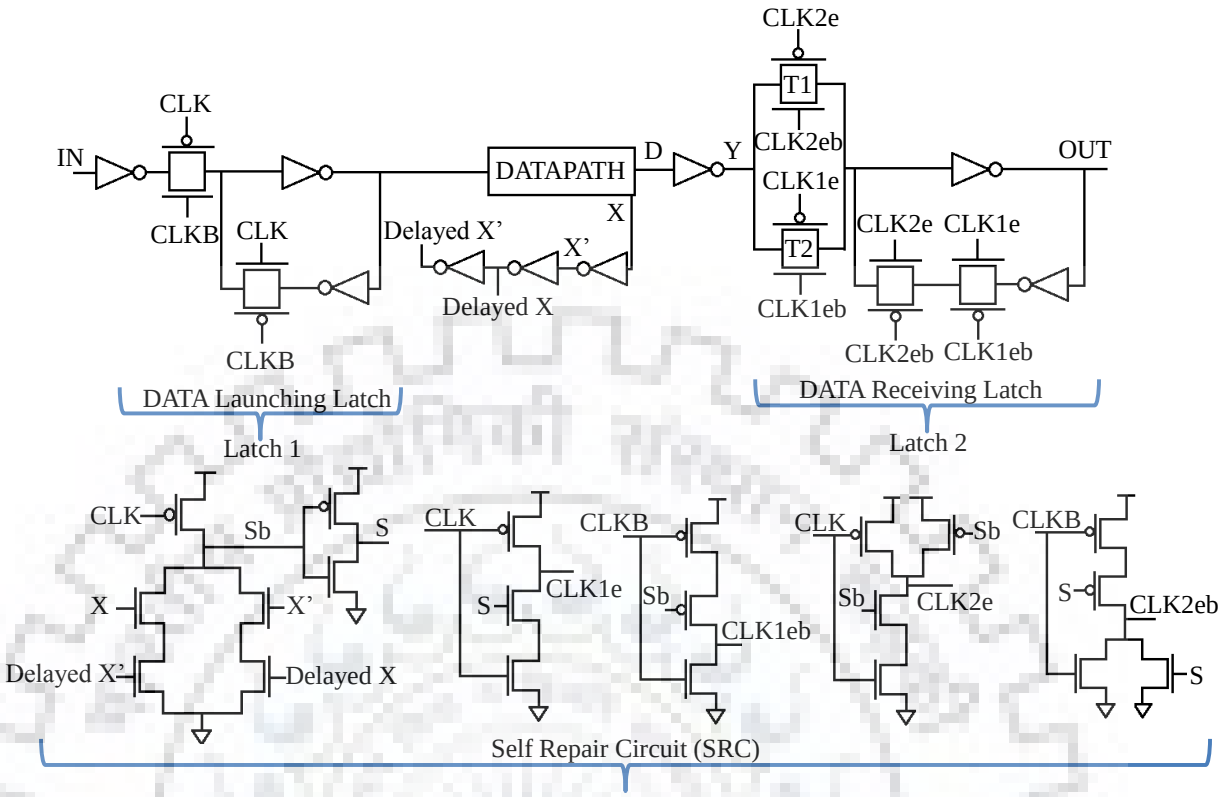


Figure 3.2 Schematic diagram of proposed SCL technique.

The proposed SCL technique is shown in Fig. 3.2, has two parts. The first part is composed of a D-type latch which is based on CMOS transmission gate (Latch 2). Its input inverter is thereby followed by two parallel transmission gates namely T1 and T2. The sizes (W and L) of T1 and T2 are equal; however, their layout implementations are different. A maximum possible number of fingers, while following minimum finger width constraint, are kept in the transmission gate T1 [136]. In any CMOS technology, there is a minimum finger width constraint that would determine maximum number of fingers for a transistor [138]. Consequently, the charging/discharging current of T1 is higher than that of T2 due to INWE. The layout of the proposed architecture is shown in Fig. 3.3. The layouts of T1 and T2, which have a different numbers of fingers, are highlighted in the Fig. 3.3. The proposed self-repair circuit (refer to Fig. 3.2), which is explained next, selects one of the transmission gate T1/T2 based on the latch's input arrival time. If data transitions occur in the high phase of clock signal and there is no setup time violation, then T2 is selected by controlling signals of transmission gate (i.e. CLK1e and CLK1eb). If data switches near the edge of clock signal (i.e. setup time violation) T1 is selected by controlling signals (i.e. CLK2e and CLK2eb). In Fig. 3.2, CLK and CLKB are the clock signal and inverted clock signal respectively.

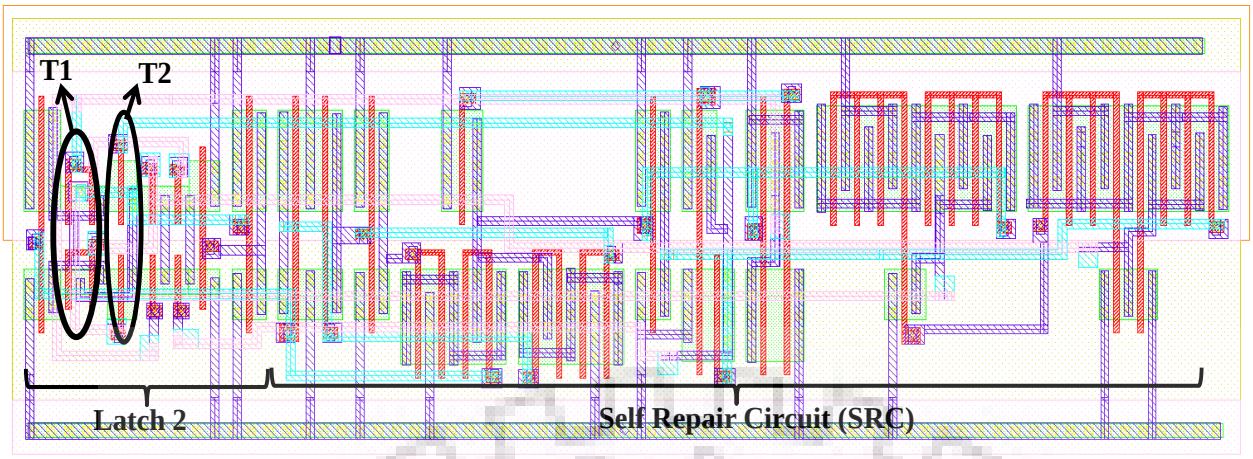


Figure 3.3 Layout of proposed SCL technique.

The second part of SCL is the self-repair circuit which consists of a dynamic NAND, NOR and XOR circuit. If the input data switches in the setup time window of the clock signal, then self-repair signal (S) will not switch thus activating T1, which is faster because of the INWE. Therefore, our self repair circuit generates control signals CLK2e and CLK2eb (please refer to Fig. 3.4), which are the delayed versions of the input clock signal. Consequently, the data at node D gets extra time to reach the output node through T1 path (which is faster than T2) as illustrated in Fig. 3.2.

From the second last stage of the data-path, an input namely X is taken which is then applied to the self repair circuit. For each data switching, the dynamic XOR-gate's first pair of inputs i.e. signal X and X' change their values immediately. Whereas the second pair of inputs i.e. delayed X and delayed X' change their value after a short delay. This short delay should allow for the discharge of node Sb. A pulse is generated at the output node of the XOR gate (S), if the data switches during the high phase of the clock signal (i.e. CLK = 1).

Two 2–input dynamic NOR gates and NAND gates are used in our methodology; these logic gates pass the self-repair signal as the control signal of the transmission gates T1 and T2. The following constraints must be met by appropriate transistor sizing in the self repair circuit: let the delay between the switching of node X and the control signals of transmission gate T1/T2 be D1. D1 should be smaller than the delay between the switching of node X and input Y of transmission gate T1/T2. We used the method of logical effort to size our SRC [139]. In the dynamic gates in the SRC, we use minimum size transistor for the pre-charge transistors. The evaluation transistors are sized according to the method of logical effort [139]. This ensures a minimum possible delay through the self repair cicuit.

The proposed SCL latch is transparent during the high phase of clock signal (CLK = 1), while non-transparent when CLK = 0. In transparent mode, when data arrives before the falling edge of the clock signal (means error free case) input data (D) is propagating to output (OUT) through transmission gate T2. In this case feedback path of the latch is in standby mode. During the low phase of the clock signal (CLK = 0) both transmission gate (T1 and T2) are get in standby mode while in this case feedback is activated. In this case the proposed latch retains the pervious data on output node of the proposed latch.

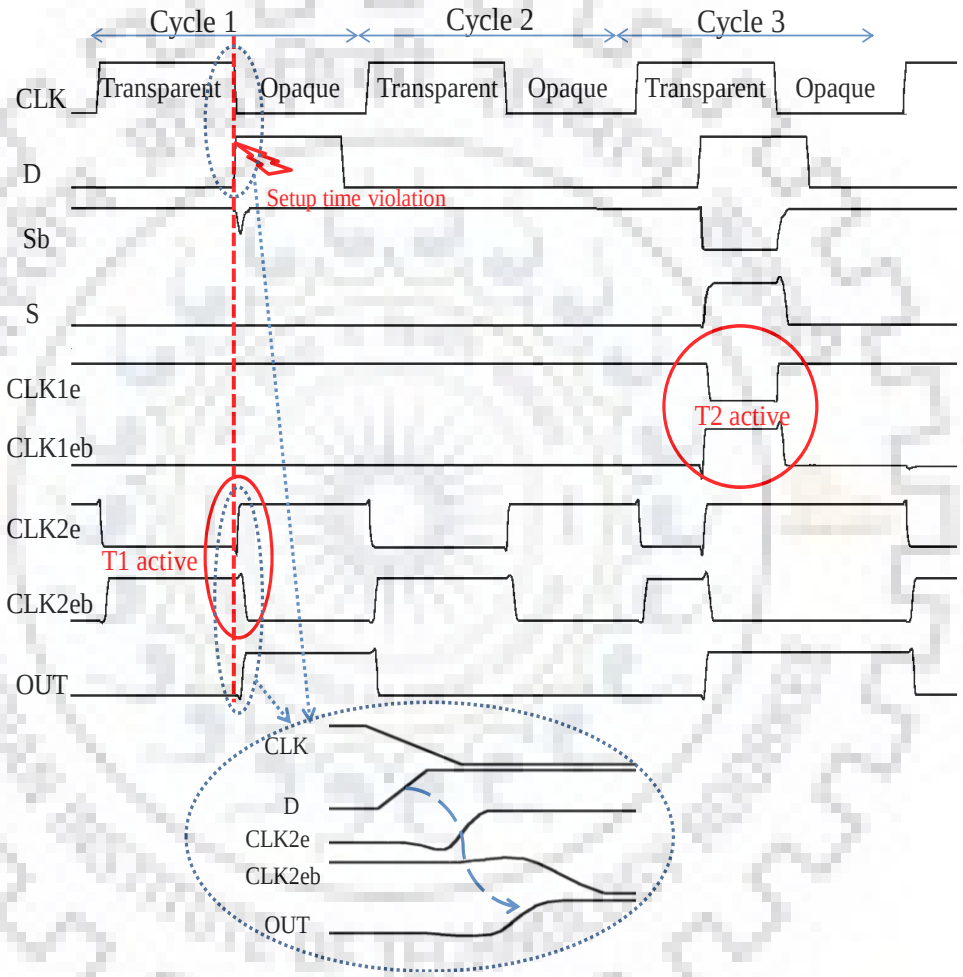


Figure 3.4 Simulated timing diagram of the proposed methodology using S27 as a datapath.

In our proposed SCL technique when timing violation occur the data (D) passes through T1 transmission gate. Therefore, the internal setup time is with respect to CLK2e is T_{si}. Let the delay between CLK2e and CLK be D_{CLK}. Let the setup time of a conventional latch (i.e. Latch1 in Fig. 3.2) be T_s. Then the limit of setup time violation allowed in our SCL technique is T_s-(T_{si}-D_{CLK}), which is equal to inverter FO1 delay. The internal setup time of the proposed latch is with respect to CLK2e while the actual setup time is with respect to CLK signal. So, the negative setup time for our proposed latch is T_s-T_{si}.

In our SCL technique, we employ INWE to optimize the performance; INWE occurs due to the shallow trench isolation (STI) which is the most popular isolation technique in deep sub-micron technologies. Due to the poly overhang over the isolation oxide, as the MOS transistors width reduces, the parasitic corner transistor adds a major portion in the transistor characteristic. Consequently, the threshold voltage (V_{TH}) reduces for a narrow width transistor. This effect is also called INWE. Moreover, the drain current (I_{dsat}) is exponentially dependent on V_{TH} in near/sub threshold regime, which strengthens the impact of INWE [140], [141]. In NTV regime INWE increases the charging/discharging currents exponentially for the MOS transistor and improves the performance of the circuit. Figure 3.5 validates the same and shows that when the input passes through T1 (which is having a large number of fingers for a given total width i.e. a stronger INWE) it takes less time for charging /discharging as compared to T2 and hence improves the latch's performance.

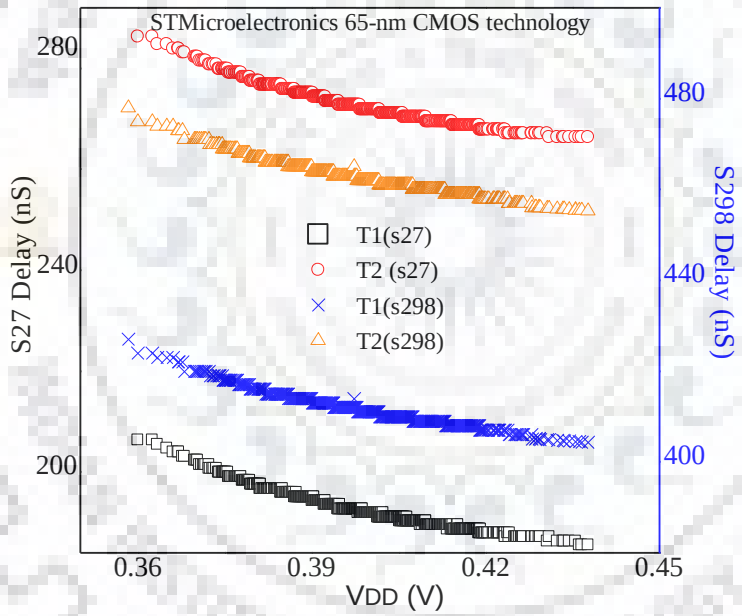


Figure 3.5 In-Out delay (through transistor T1 and T2) vs V_{DD} for S27 ISCAS circuit obtained using HSPICE 1000 MC Simulations.

The reason for using slow and fast paths instead of a single fast path in latch 2 in the proposed technique is as follows: In NTV circuit design due to high variations large design margins are required for a high yield, resulting in a sub-optimal design. Using our technique, we can reduce the design margins without compromising the yield. Though the nominal path is slightly slow the reduced design margins in our SCL technique improves the overall performance. A data receiving latch (conventional latch) using only T1, would have higher failure rate due to large variations. We have done 1000 Monte Carlo (MC) simulations with only fast path (without

slow path and self repair circuit) in latch 2, and then we find 36% more failed simulation as comparison to our technique.

3.3 Simulation Setup

For a fair comparison with existing resilient Flip-Flop's, we implement our self correcting latch technique as a Master Slave Flip-Flop (MSFF). We employed proposed self correcting latch technique as an MSFF on ISCAS'89 benchmark circuits (s27, s298 and s344) and 74X series circuits (74182 and 74283) from benchmark database. All the simulations are carried out on STMicroelectronics 65-nm CMOS process design kit (PDK). We verified the proposed SCL technique at a supply voltage V_{DD} = 0.4V because, using HSPICE simulations, we determine the minimum energy point (MEP) to be at V_{DD} = 0.4V. For calculating the MEP, we simulate an inverter chain shown in Fig. 3.6 (a). Fig. 3.6 (b) shows the simulated energy delay curve for the device under test (DUT) in the inverter chain. From Fig.3.6 (c) we observe that MEP is at V_{DD} = 0.4V.

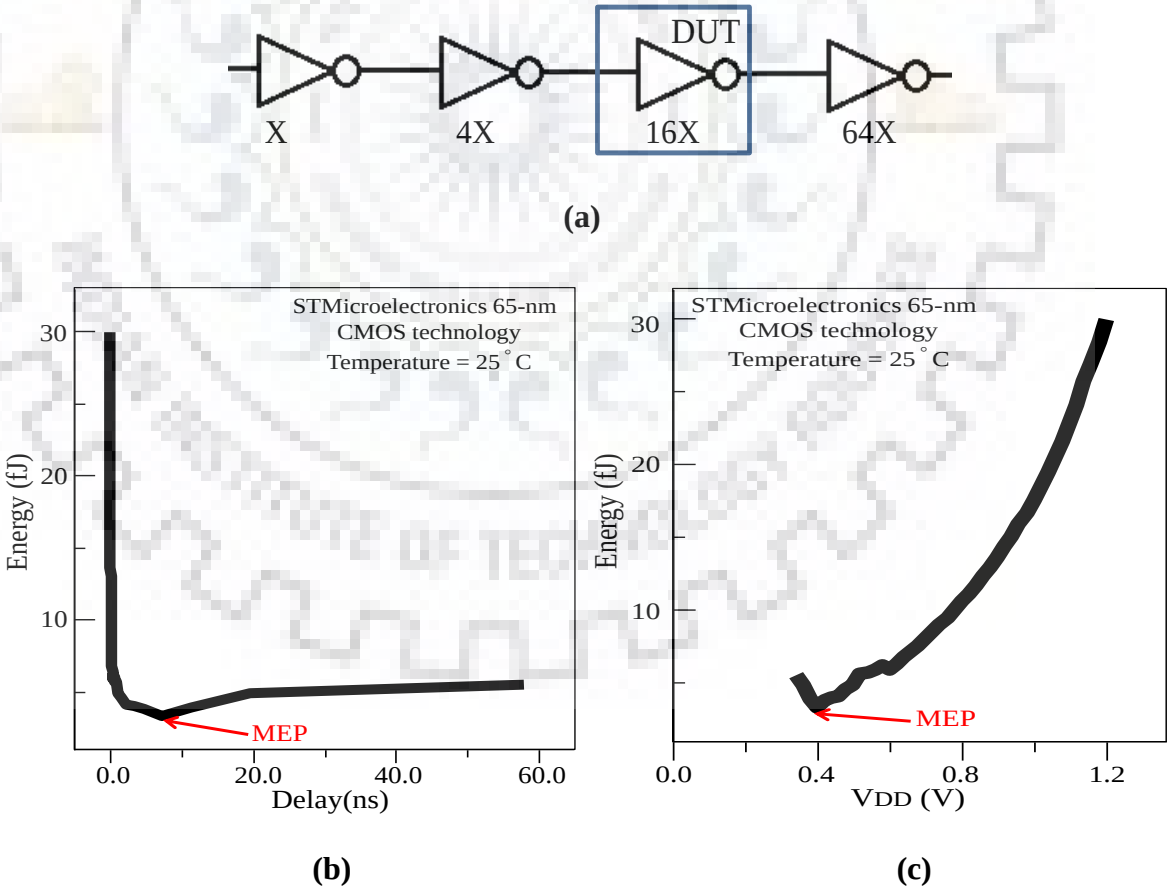


Figure 3.6 (a) Static CMOS inverters (b) Energy Delay curve, (c) Energy v/s power supply (V_{DD}) curve for an inverter.

The transistor sizes in the proposed latch are as follows for the STMicroelectronics 65-nm CMOS technology: (a) For self repair circuit (SRC), sizing of XOR gate of NMOS (PMOS) transistors have W=1.4µm (1.06µm), while the sizing of NAND gate NMOS (PMOS) transistors have W= 1.06µm (1.06µm), and sizing of NOR gate NMOS (PMOS) transistors have W= 0.53µm (2.06µm), (b) For proposed latch the transmission gate (T1) PMOS and NMOS transistors have W=0.53µm, with maximum allowed number of fingers while T2 is single finger with size same as of T1. All others transistors have the smallest allowed W values for the given technologies. We have sized ERFF and VAFF in such a way that the comparison with our SCL technique is for an iso-input (D) load case.

3.4 Simulation Results

In this section, using MC HSPICE simulations, we verify that our SCL technique detects timing violations in data-paths efficiently. We also compare the SCL technique to recently reported ERFF technique [72] and VAFF technique [71]. The work in [71] and [72] is also based on the choice of sequential element through multiplexing in case of timing violation. Our verification flow is as follows: First, we consider each of the ISCAS'89 benchmark circuits (s27, s298, s344, 74182 and74283) in DATAPATH of Fig. 3.2. We next perform 1000 MC simulations to evaluate the circuit performance under PVT variations. A 10% variation is given in transistor threshold (V_{TH}) and power supply (V_{DD}) voltages [75], [142] at three different temperatures (-25°C, 25°C and 125°C).

Figure 3.7 (a), Fig. 3.8 (a), and Fig. 3.9 (a) show the delays of S27 using the proposed SCL, ERFF and VAFF, respectively, at 25°C and V_{DD} = 0.4V. We have also shown the mean and standard deviation of the delays of S27 in these figures. We observe that the proposed SCL technique gives 14.43% (16.62%) and 34.13% (50%) lesser standard deviation (i.e., variations) and mean (i.e., performance) of delay as compared to the ERFF (VAFF) technique at room temperature. This is also illustrated in Table 3.1. Similar results are also observed for S298, S344, 74182 and 74283 ISCAS' 89 benchmark circuits as shown in Fig. 3.7, Fig. 3.8, and Fig. 3.9, respectively. We explain these results as follows: Upon setup time violation, the voltage levels of the inputs of the "late detector" (self-repair circuit) of ERFF do not reach V_{DD}/0 ("n1" and "n2" of Fig.2 of [72]). Whereas, in our approach, T1 reduces the delay by about 10% - 20% in the case of a setup time violations.

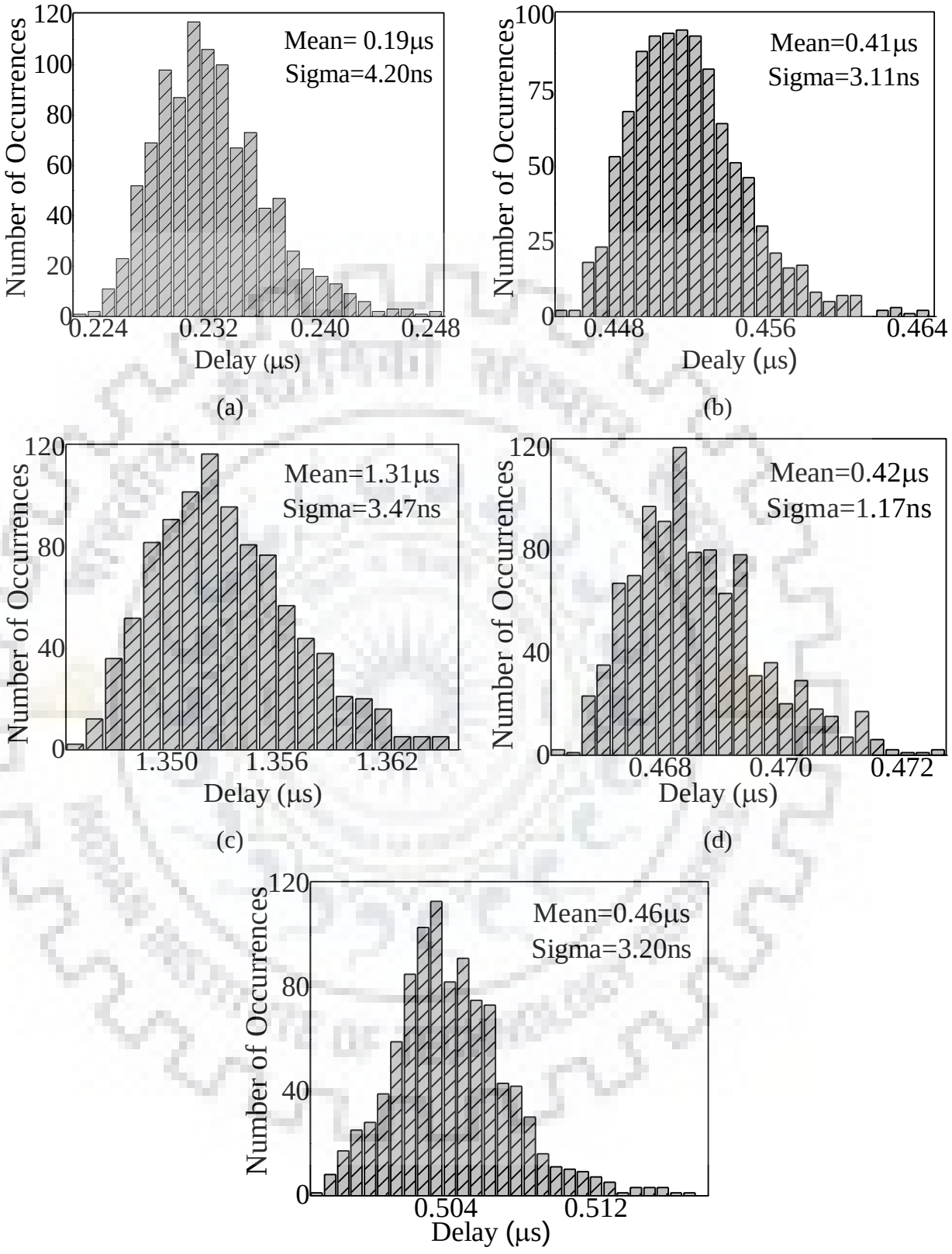


Figure 3.7 Histogram of our SCL technique at 25^0C for (a) S27, (b) S298, (c) S344, (d) 74182 and, (d) 74283.

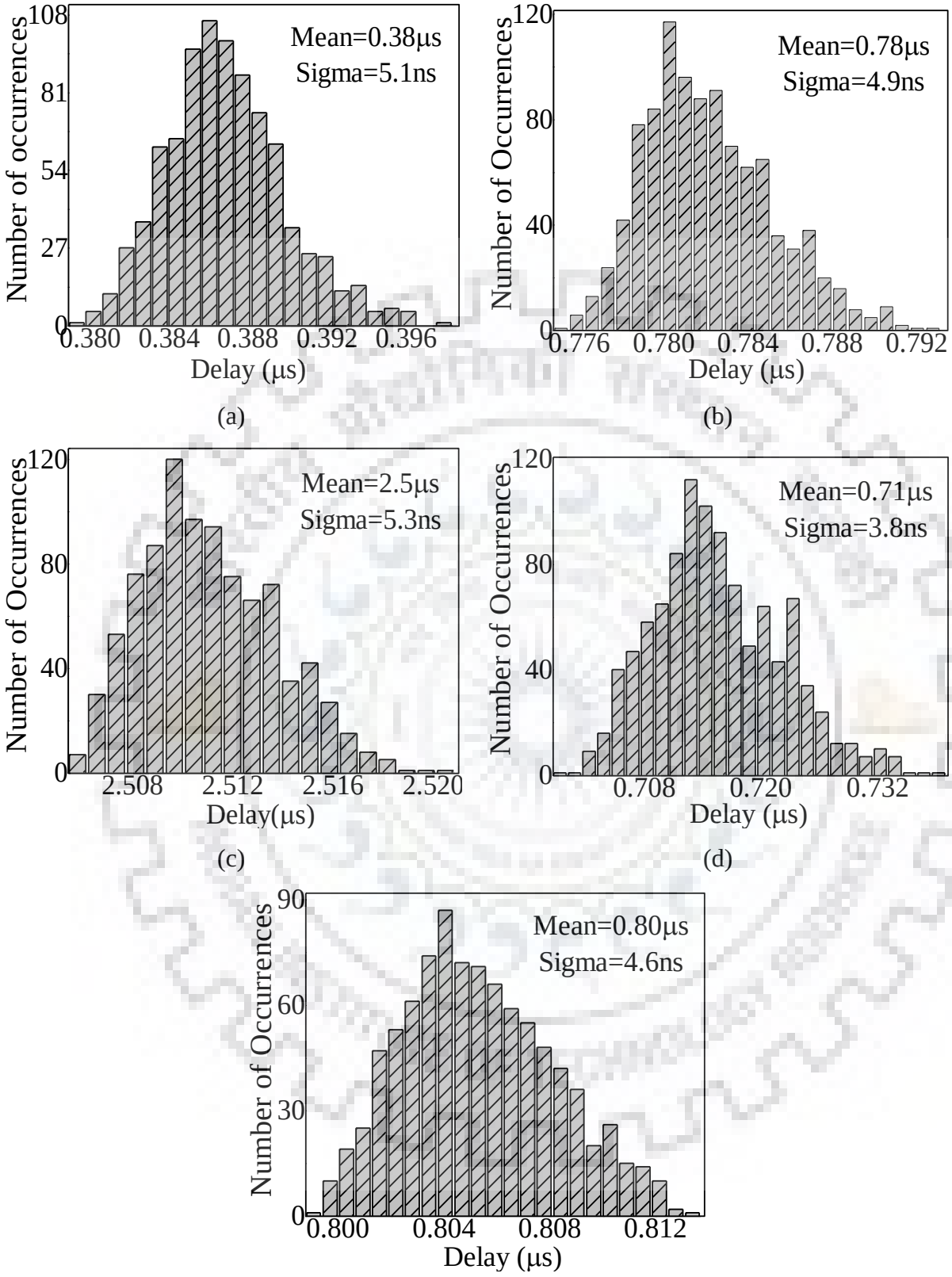


Figure 3.8 Histogram of ERFF technique at 25^{0}C for (a) S27, (b) S298, (c) S344, (d) 74182 and, (d) 74283.

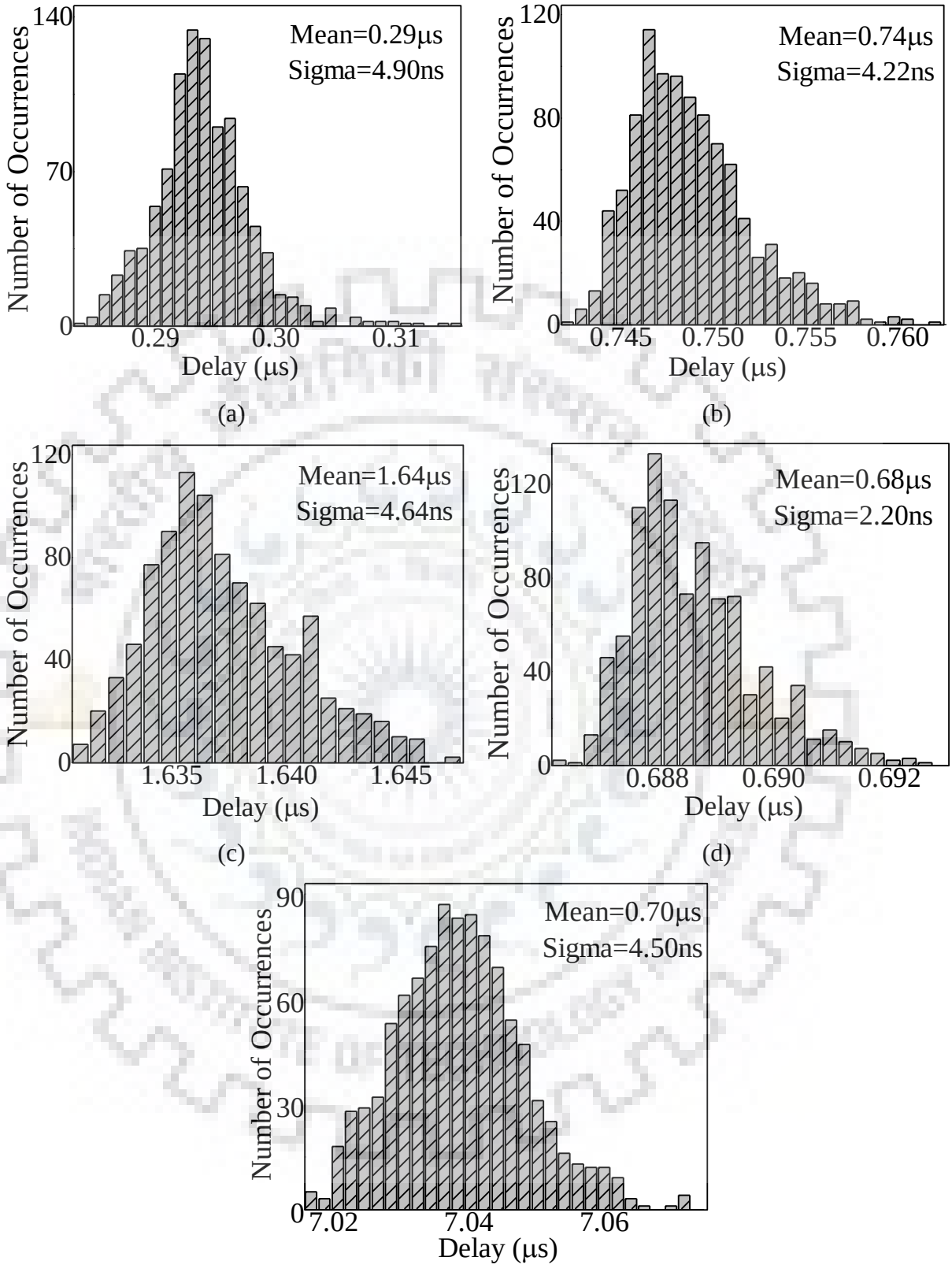


Figure 3.9 Histogram of VAFF technique at 25^{0}C for (a) S27, (b) S298, (c) S344, (d) 74182 and, (d) 74283.

Table 3.1 Comparison summary of various parameters of ERFF and VAFF to proposed SCL technique.

Temperature	ISCAS'89 benchmark circuit	Techniques	Mean (µs)	Sigma (ns)	Maximum Delay(µs)	Avg. Power (nW)	Input Cap of X (fF)
-25°C	S27	SCL Technique	0.21	12.4	0.252	43.10	0.11
		VAFF Technique [71]	0.41	15.01	0.428	48.33	0.23
		ERFF Technique [72]	0.31	13.2	0.350	41.51	0.18
	S298	SCL Technique	0.42	5.42	0.469	114.00	5.81
		VAFF Technique [71]	0.86	8.35	0.939	125.64	9.83
		ERFF Technique [72]	0.81	8.09	0.910	114.70	7.42
	S344	SCL Technique	1.39	5.61	1.43	211.70	7.82
		VAFF Technique [71]	2.73	8.31	2.810	223.50	10.51
		ERFF Technique [72]	1.79	7.53	1.820	197.42	7.96
	74182	SCL Technique	0.47	3.62	0.474	51.37	3.61
		VAFF Technique [71]	0.79	7.83	0.821	64.58	6.01
		ERFF Technique [72]	0.70	5.01	0.721	44.13	4.93
	74283	SCL Technique	0.48	7.83	0.501	62.15	3.72
		VAFF Technique [71]	0.82	8.36	0.841	73.04	6.57
		ERFF Technique [72]	0.72	9.15	0.736	55.53	5.01
25°C	S27	SCL Technique	0.19	4.21	0.214	47.00	0.68
		VAFF Technique [71]	0.38	5.13	0.401	59.14	0.92
		ERFF Technique [72]	0.29	4.91	0.326	45.78	0.72
	S298	SCL Technique	0.41	3.11	0.427	176.00	8.75
		VAFF Technique [71]	0.78	4.91	0.798	193.95	15.36
		ERFF Technique [72]	0.74	4.22	0.765	163.00	11.63
	S344	SCL Technique	1.31	3.47	1.33	283.41	10.31
		VAFF Technique [71]	2.51	5.30	2.521	298.19	16.99
		ERFF Technique [72]	1.64	4.64	1.660	267.53	12.49
	74182	SCL Technique	0.42	1.17	0.434	61.49	6.53
		VAFF Technique [71]	0.71	3.85	0.746	76.89	9.39
		ERFF Technique [72]	0.68	2.19	0.695	52.63	7.81
	74283	SCL Technique	0.46	3.19	0.479	75.95	7.87
		VAFF Technique [71]	0.80	4.68	0.824	89.91	11.01
		ERFF Technique [72]	0.70	4.56	0.708	65.06	8.43
125°C	S27	SCL Technique	0.15	1.20	0.158	255.00	2.52
		VAFF Technique [71]	0.24	1.68	0.246	256.37	5.41
		ERFF Technique [72]	0.18	1.53	0.191	228.70	4.37
	S298	SCL Technique	0.40	0.79	0.404	930.03	19.33
		VAFF Technique [71]	0.47	1.34	0.561	979.27	27.03
		ERFF Technique [72]	0.50	0.97	0.505	924.01	22.05
	S344	SCL Technique	0.70	0.752	0.706	1154.03	21.45
		VAFF Technique [71]	1.47	1.89	1.492	1189.36	31.82
		ERFF Technique [72]	0.90	1.09	0.909	1147.81	27.83
	74182	SCL Technique	0.41	0.29	0.417	317.20	17.12
		VAFF Technique [71]	0.51	1.02	0.539	388.49	24.88
		ERFF Technique [72]	0.52	0.42	0.530	311.2	20.71
	74283	SCL Technique	0.45	0.59	0.458	423.71	19.03
		VAFF Technique [71]	0.61	2.45	0.636	447.86	26.32
		ERFF Technique [72]	0.70	0.74	0.699	388.10	21.66

Table 3.1 also compares the figures-of-merit (FOM) of the SCL technique to the ERFF and VAFF technique, when s27, s298 and s344 ISCAS'89 benchmark circuits and 74182 and 74283 74X series circuits are used as DATAPATH (please refer to Fig. 3.2). Table 3.1 shows the maximum delay, which is the largest propagation delay obtained from the 1000 MC simulations, and is used as a pointer of robustness.

"Input Cap" is the input capacitance seen by the data path warning/self repair signal generator input X; a large value of input cap increases the delay. Our SCL technique shows a smaller input capacitance as compared to technique in [71] and [72]. This is because we implement the self-repair through a dynamic circuit. Due to the same reason, the proposed circuit has less area overhead as compared to the [71] and [72].

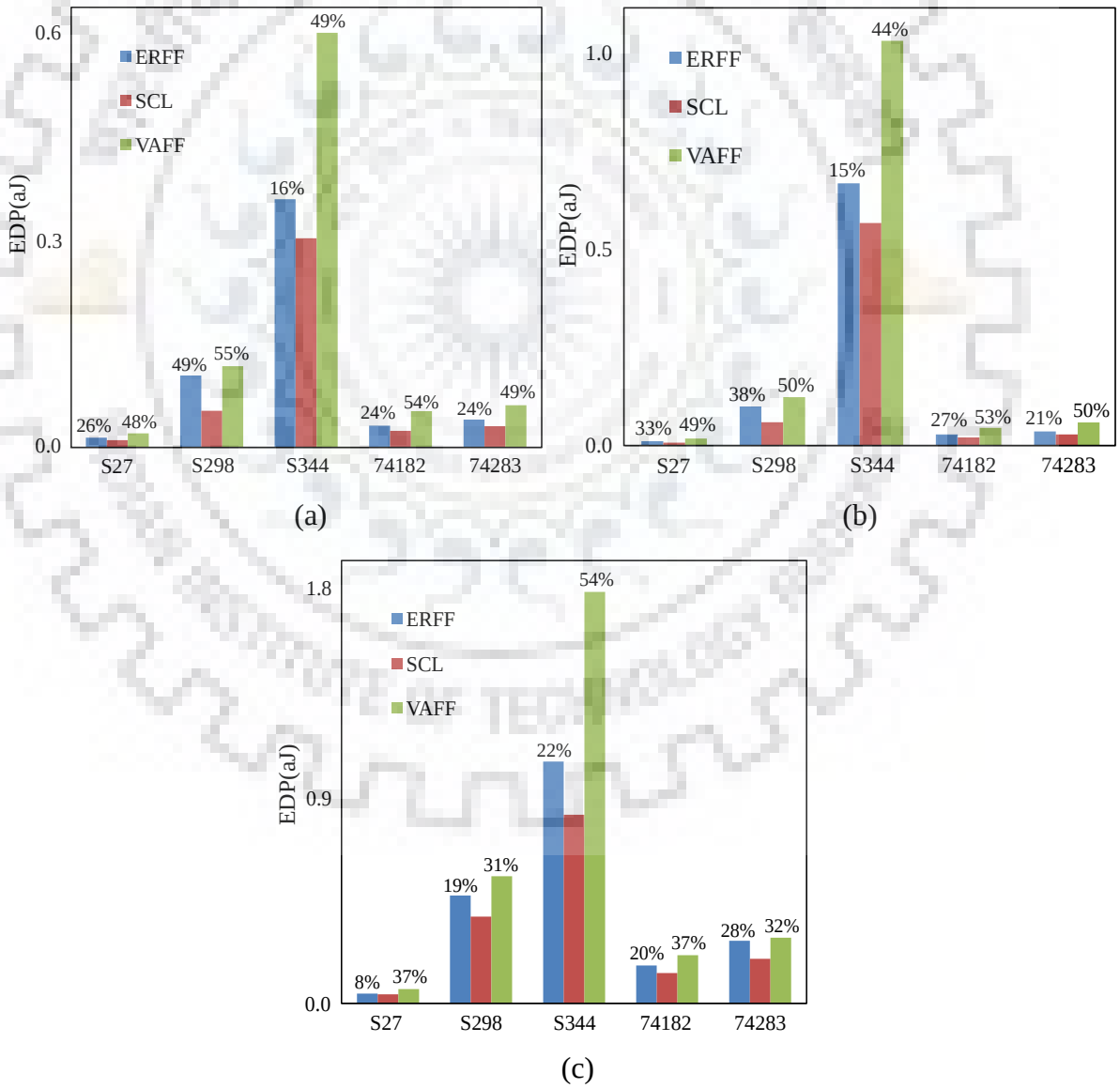


Figure 3.10 Energy Delay Product of our SCL technique, ERFF technique and VAFF technique for ISCAS benchmark circuits (s27, s298, s344, 74182 and 74283) at (a) -25°C, (b) 25°C and (c) 125°C.

Figure 3.10 shows the maximum energy delay product (EDP) of the SCL, ERFF and VAFF technique at 0.4V power supply (please note that maximum propagation delay is taken for these EDP calculations). In Fig. 3.10, the percentage data represents the improvement over ERFF and VAFF technique when s27, s298, s344, 74182 and 74283 ISCAS'89 benchmark circuits are used as the DATAPATH (please refer to Fig. 3.2). Please note that the power consumption mentioned in Table 3.1 is for the entire circuit, which includes the benchmark datapath as well as the SCL/ERFF/VAFF technique. From Fig. 3.10, we observe that proposed SCL technique shows a significant improvement over design techniques discussed in [71] and [72] (Please note that in EDP calculations, the total power dissipation per cycle is used). From above analysis, we find that the SCL technique is robust in mitigating setup time violations due to PVT variations in near/sub threshold regime without changing the V_{DD} and operating clock frequency.

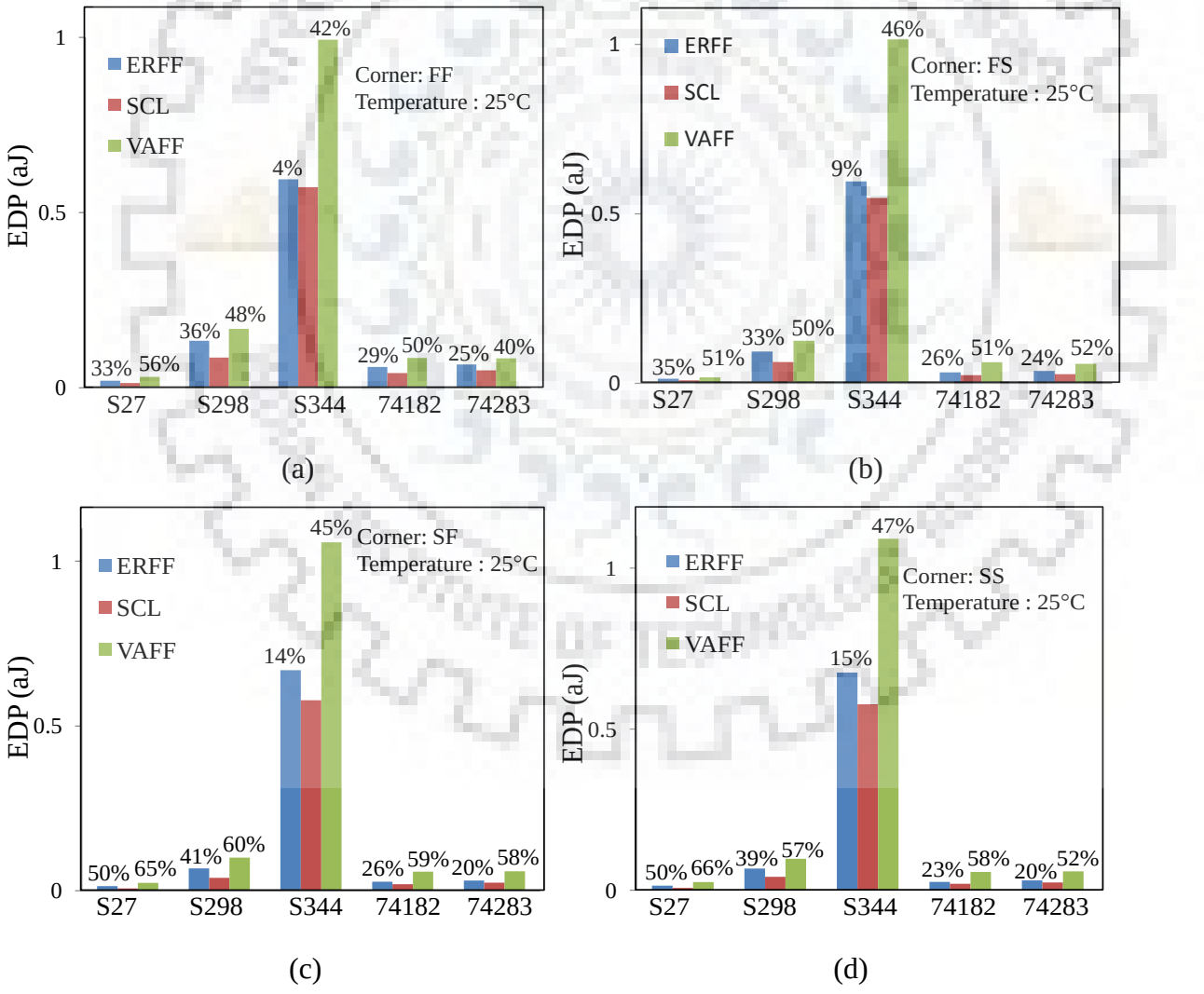


Figure 3. 11 Energy Delay Product of our SCL technique, ERFF technique and VAFF technique for ISCAS benchmark circuits (s27, s298, s344, 74182 and 74283) at power supply 0.4V at room temperature (a) FF corner, (b) FS corner, (c) SF corner, and (d) SS corner.

The comparison of EDP of the proposed SCL technique with ERFF and VAFF at four different process corners namely Fast Fast (FF), Fast Slow (FS), Slow Fast (SF), and Slow Slow (SS) in 65nm CMOS technology is shown in Fig. 3.11 at supply voltage 0.4V at room temperature (25°C). In Fig. 3.11 percentage data represents the improvement over ERFF and VAFF technique when s27, s298, s344, 74182 and 74283 ISCAS'89 benchmark circuits are used as the DATAPATH (please refer to Fig. 3.2). In all process corners the proposed SCL technique shows less EDP as compare to the ERFF and VAFF technique.

Post layout simulation results show that the SCL technique is robust with PVT variations as compared to the [71] and [72] techniques. Further, the SCL technique improves the performance over ERFF technique with nearly same power dissipation. For iso-input data load our proposed latch's clock load is nearly 3.76fF, whereas, for the existing technique VAFF, and ERFF is 4.52fF and 4.31fF respectively. Please note that the clock load is lesser in our SCL case compared to ERFF and VAFF in the iso-input load case.

In Table 3.2, we compare our SCL technique with the most cited Razor Flip-Flop technique [65] and recently reported soft edge error detecting (SEED) Flip-Flop [75] technique. Table 3.2 shows that the percentage of failure rate employing our SCL technique is ~17% and 14% better than the Razor technique and SEED technique, respectively. In Table 3.2 percentage of failure rate means the percentage of failed simulations out of 1000 Monte Carlo simulations means those simulations have lager delay than the (mean + 3σ). We observe that our SCL technique has lesser number of failed simulations over the existing technique. Table 3.2 also shows the comparison of average power dissipation. The proposed SCL technique have less average power dissipation compare with the other two techniques.

Table 3.2 Comparison of percentage of 3σ failure rate and Avg. power dissipation between Razor, SEED and our methodology.

Benchmark circuits	Failure rate percentage			Avg. Power(nW)		
	SCL Technique	Razor Technique [65]	SEED [75]	SCL Technique	Razor Technique [65]	SEED [75]
S27	2.8%	19.2%	15.7%	47.00	49.62	51.14
S298	2.5%	15.3%	12.1%	176.00	195.87	196.95
S344	2.9 %	16.7%	13.8%	283.41	314.64	317.06
74283	3.2%	16.9%	14.0%	75.95	79.85	83.27

We also tested our SCL technique on a small datapath, which was also used in [69], with ERFF, VAFF and SEED. In this small datapath variation is more as compare to large datapath, in sub/near threshold region. Table 3.3 shows the comparison of our SCL technique with ERFF, VAFF and SEED in terms of delay and variance for this datapath. Our SCL technique shows better results as compare to existing technique.

Table 3.3 Comparison summary of VAFF [71], ERFF [72], and SEED [75] to our methodology for the small datapath of [69].

Techniques	Mean(nsec)	Sigma(nsec)
SCL Technique	0.26	1.05
VAFF Technique [71]	0.38	1.57
ERFF Technique [72]	0.33	1.46
SEED Technique [75]	0.37	1.53

3.5 Summary

In this chapter, a low area timing error resilient circuit technique in NTV regime has been proposed. In the case of a timing violation, our technique automatically chooses an appropriate faster path in our novel latch, thereby reducing the setup time. This latch employs a transmission gate based multiplexer in a latch, with the transmission gates differing in their layout implementations. INWE is used to implement the faster path (transmission gate), which is activated in the case of timing violations. The proposed SCL technique shows a higher performance and better robustness against PVT variations without power consumption overhead over earlier resilient circuit techniques. We have shown that under PVT variations the SCL technique implementation on s27, s298, s344, 74182 and 74283 ISCAS'89 benchmark circuits improves the performance in terms of delay up-to 34%, 44%, 25%, 42% and 32% respectively at 0.4V power supply. We observed that our SCL technique is less variant compared to other existing approaches. For iso-delay the SCL technique shows up-to ~ 21% reduction in power dissipation compared to the ERFF technique for S27 ISCAS'89 benchmark circuit. Post-layout simulations show that our technique achieves 4.85%, 7.73% and 5.79% less area compared to the earlier proposed ERFF, VAFF and SEED techniques, respectively. We further present that over ERFF technique our SCL technique leads to a ~ 20% minimization in power delay product for several ISCAS'89 benchmark datapath circuits.

4 CHAPTER

A Physics based Variability Aware Methodology to Estimate Critical Charge for Near-Threshold Voltage Latches

4.1 Overview

Nowadays ultra-low power and energy efficient near threshold voltage (NTV) circuit techniques [4]-[6], [143] are emerging. However, due to the smaller circuit node capacitances (due to an implementation at lower technology node) and smaller supply voltage operation (due to NTV operation), NTV circuits are more prone to single event upsets (SEU) [53]. Consequently, the charge required at a circuit node to change the logic value is getting aggressively reduced [12]-[13]. This signifies that the logic level of a node becomes more easily upset by glitches resulting from radiations due to the high energy neutrons and alpha particles [13]. In memory and sequential elements (Latches/Flip-Flops), this perturbation can result in data flipping ("1" to "0" flip or "0" to "1" flip). An SEU in a latch/Flip-Flop may increase the propagation delay due to glitches and/or the data may be enter a metastable state. Soft errors are serious design issues in latches/Flip-Flops because of another reason: If a transient fault (TF) or a glitch occurs at the output of a latch/Flip-Flop, it may lead to a non-critical path turning into a critical path. A conventional D-latch or Flip-Flop is very sensitive to SEU due to high energy particle strikes. During the low phase of the clock signal, an SEU may upset the logic level of the positive edge triggered Flip-Flop, the corrupt values are not corrected until a new value is stored in the Flip-Flop [144].

For memory elements such as Flip-Flops and latches, if the total charge deposited by the striking of a high energy particle at the sensitive node is more than a minimum charge, the node level is flipped and an SEU occurs. This minimum charge on the sensitive node is called the critical charge ($Q_{ciritical}$), which can be used as a parameter to measure a latch's susceptibility to SEU or soft errors [78]-[80]. The $Q_{ciritical}$ exhibits an exponential relationship with the soft error rate (SER) [81]. To design a latch/ Flip-Flop, $Q_{ciritical}$ must be high enough to limit the SER. In particular, sub-threshold/near-threshold voltage latches/Flip-Flops are susceptible to SEU due to the reason discussed earlier. Therefore, there is a need of modeling and analysis of radiation-induced soft error due to SEU in sub-threshold/ near-threshold voltage static latches.

Recently, researchers have shown interest to determine $Q_{critical}$ on sensitive nodes of a memory and sequential circuits such as latches/ FF's. Work has also been done to handle the impact of process-voltage-temperature (PVT) variations in the critical charge in super-threshold regime (nominal voltages). However, most of the researchers employed Monte Carlo (MC) analysis to calculate the critical charge [87]. But MC analysis is not a convenient solution to calculate the critical charge because it is very time consuming and also not scalable with CMOS technology [86] and circuit size. For every new design and process node, MC analysis has to be carried out to calculate the $Q_{ciritical}$ variability.

In this chapter, an accurate semi-analytical model to estimate the $Q_{critical}$ for a static D-latch operating in the NTV regime is proposed. The proposed model is a function of design parameters such as transistor sizes, supply voltage and fan-out load. The main contribution of this chapter is: For the first time, a physics-based variability aware methodology to estimate the critical charge of an NTV static D-latch is proposed. The derived model can be used to estimate the critical charge as a function of latch's fan-out loads and supply voltages.

The chapter is organized as follows: Section 4.2 presents the proposed physics based semi-analytical model of critical charge for a static D-latch. The validation of the proposed model using Cadence SPECTRE simulations in STMicroelectronics 65-nm process design kit (PDK) and for technology computer-aided design (TCAD) mixed-mode simulations, we use calibrated 32-nm technology setup [145] is presented in section 4.3. Section 4.4 presents the impact of variability on the proposed model. Section 4.5 presents the methodology to estimate $Q_{critical}$. Section 4.6 summarizes the chapter.

4.2 Critical Charge Model for Static D-latch

Figure 4.1 depicts the conventional static D-latch circuit. It consist two paths: First is the main path which consists of an inverter and, second is the feedback path which consists of an inverter followed by a transmission gate. The static D-latch stores two complementary binary values (0 and 1) at intermediated nodes N1 and N2. This conventional latch is more prone to particle strike on intermediated nodes in hold mode (CLK = 0), because the intermediate nodes are disconnected from the input (IN) of the latch. The transmission gate T1 is not included in our analysis because both the transistors are in OFF state during the low phase of the clock signal. In the hold mode (when CLK = 0), let us assumed that node N1 stores logic "1" and N2 stores logic "0". Therefore, only Mn1, and Mp2 transistors and transmission gate T2 are ON.

Traditionally, a double exponential current source is used to emulate the injection of an SEU on internal nodes [146]. This current source represents the electrical impact of a high energy particle strike.

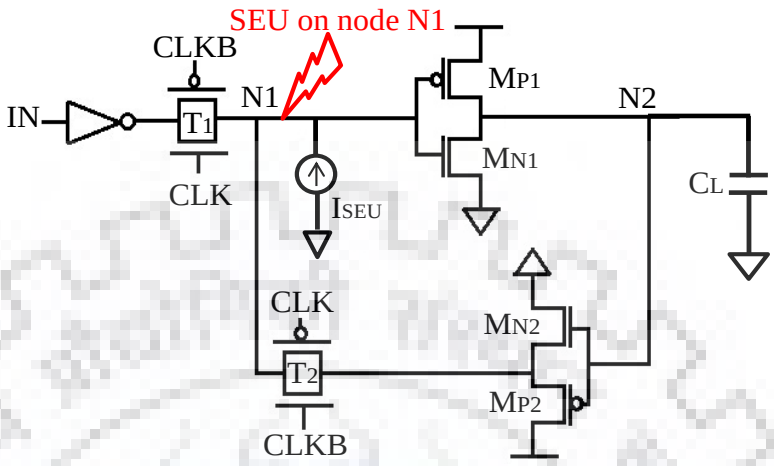


Figure 4.1 The static D-latch, which is most commonly used, is susceptible to SEU due to transient fault at node N1 (equivalently, node N2)

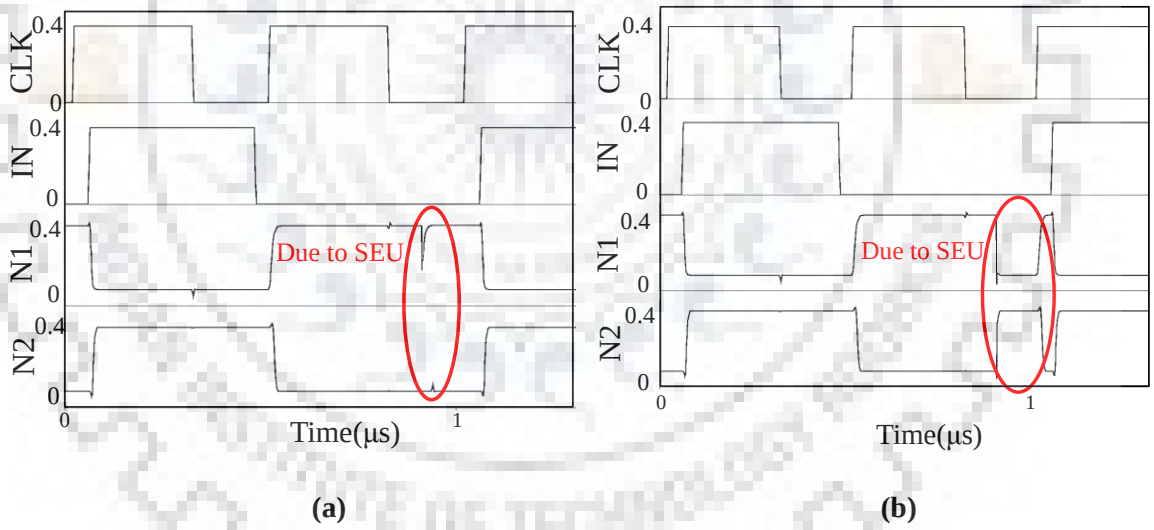


Figure 4.2 Simulated waveforms for Nodes N1 and N2 of the static D-latch for (a) non-flipping (< Qcritical) case, (b) flipping (> Qcritical) case due to SEU

Figure 4.2 shows the simulated waveform of a static D-latch for SEU for both the cases, one, an output glitch and, two, data flipping. In the glitch case, the magnitude of the SEU current pulse is not high enough to change the logic level at node N1. Therefore, voltage level at node N1 temporarily moves away from logic level 1 and finally returns to the same logic level (Fig. 4.2 (a)). On the other hand, if the magnitude of the current pulse is large enough to change the logic level at node N1, flipping the latch output happens (Fig. 4.2(b)). In this work, a high energy/alpha particle strike is modeled as a double exponential current source (applied at node

N1 in Fig. 4.1) and given by [146]

$$I_{SEU} = \frac{Q}{\tau_f - \tau_r}\left[\exp\left(-t/\tau_f\right) - \exp\left(-t/\tau_r\right)\right] \quad (4.1)$$

Where, Q is the total charge deposited by the double exponential current source, τ_f and τ_r are the falling time and the rising time constants, respectively [146]. Typically, for an alpha particle strike generated current pulse, the falling time constant is much larger than the rising time constant [78], [84]. The rising time is short (in the range of 0.1– 10ps) and the falling time is longer (in the range of 5–200ps) [105], [109]. In our simulation setup we use the exponential stimulus with parameters extrapolated for the technology we used i.e. 65nm (τ_r = 100fs and τ_f = 5ps) from the values provided by relevant earlier research [105], [109]. Consequently, we approximate (1) as a single exponential current source:

$$I_{SEU} = \frac{Q}{\tau_f - \tau_r}\left[\exp\left(-t/\tau_f\right)\right] \quad (4.2)$$

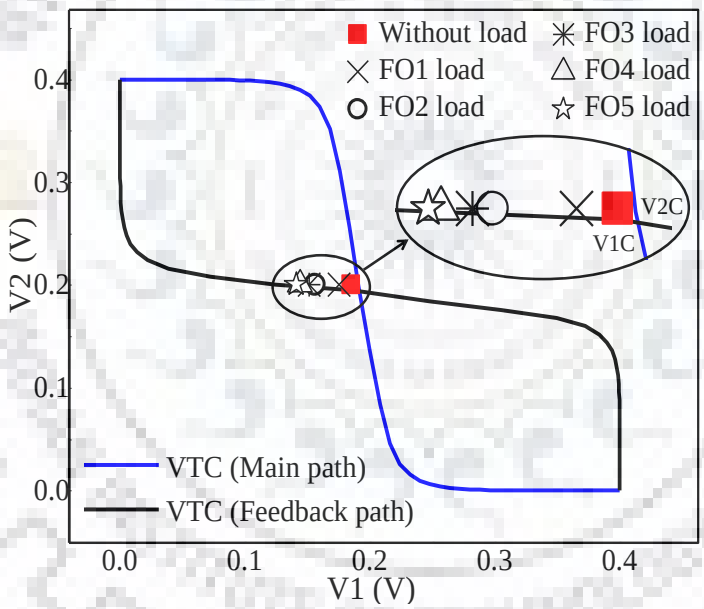


Figure 4.3 Trip points of the static latch lie on the VTC of the feedback-path.

V1 and V2 are voltages at node N1 and N2, respectively. Now we explain the phenomenon of flipping of logic states in the static latch due to SEU, both for externally unloaded and loaded cases. From DC simulations we got the voltage transfer characteristic (VTC) of both paths (main and feedback) of a static D-latch without external load (as shown in Fig. 4.3). Using transient simulations, we observe that the intersecting point of both the VTC's gives the flipping node voltages of node N1 and N2, and this point is known as trip point of a latch. This is also consistent with SRAM cell results reported in [84]. However, in a latch this trip point changes with the change in the load capacitance.

The trip point is calculated by applying the I_{SEU} on node N1 with an appropriate magnitude which high enough to flip the logic levels on nodes N1 and N2. Suppose that the latch is in hold state with N1 at logic 1 and N2 at logic 0. When a smaller value of I_{SEU} is applied at node N1, the current i_{Mn1} is greater than i_{Mp1} and in the feedback path i_{Mp2} is greater than i_{Mn2}. Therefore, in this case there is no flipping of the output node, because the PMOS current (i_{Mp2}) of the feedback path recovers the voltage level at node N1 back to its pervious state (i.e. logic 1). However, if the magnitude of I_{SEU} is increased, the current i_{Mp1} increases the value of voltage at N2. This, in turn, increases (reduces) i_{Mn2} (i_{Mp2}), which results in the voltage at node N1 not getting restored to logic 1. Consequently, the voltage at node N2 flips from its original state (from logic 0 to logic 1). As discussed earlier, at such a value of I_{SEU}, the voltages V1 and V2 fall on the VTC's of the both paths (main and feedback). At this point output currents of the main path and the feedback path are zero ($i_{Mn1} = i_{Mp1}$ and $i_{Mn2} = i_{Mp2}$). Therefore, the potentials of node N1 and N2 don't change any further, resulting in a metastable state at nodes N1 and N2. These tripping point voltages at nodes N1 and N2 are V1C and V2C, respectively. Figure 4.4 shows the waveforms of V1 and V2 at the trip point with no external (FO = 0) load. At the trip point the output currents of the main and the feedback paths are ideally zero valued, which results in V1 and V2 being held at constant values V1C and V2C, respectively, for a long time.

The value of I_{SEU} at which voltage level of node N2 ideally remains at V2C is the $I_{SEU,trip}$. In our simulations, to extract the value of $I_{SEU,trip}$, we measure the smallest value of I_{SEU} for which the latch flips from its original logic state. This is the reason for V1C (red rectangle in the inset of Fig. 4.3) being slightly smaller than its corresponding ideal metastable value.

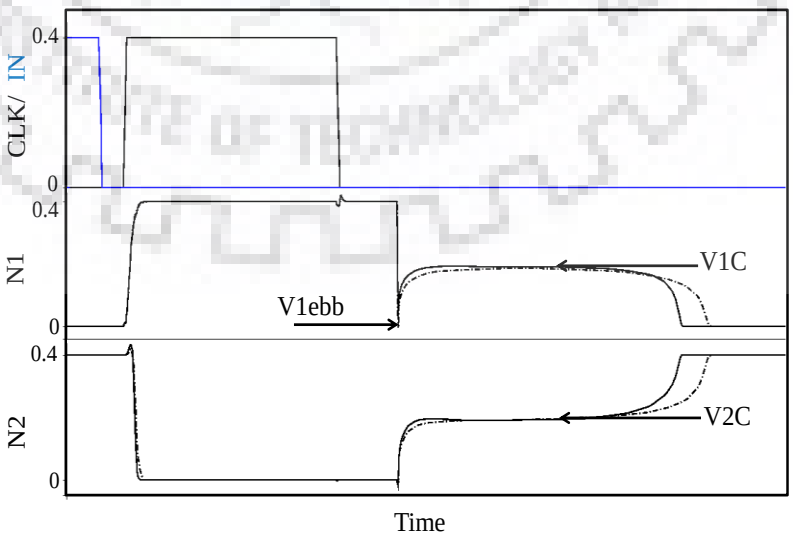


Figure 4.4 The solid (dotted) lines show the voltage transients at node N1 and N2 for a logic flipping for zero FO (FO2) case.

For a non-zero FO load, the logic states at nodes N1 and N2 flip for a larger value of I_{SEU}. To extract the value of $I_{SEU,trip}$, we follow a procedure similar to that of the zero FO case, discussed earlier. Since V1and V2 are held in metastable state, at the value $I_{SEU,trip}$ the output current of the feedback path is zero. The output current of feedback path (I2-T2) is almost fully determined by the value of V2 during SEU. This is because of the low value of V1 due to SEU and the near/sub-threshold operation of the transistors. Therefore, even for a larger FO, the value of V2 at the trip point remains V2C as in the zero external load case (dotted line in the inset of Fig. 4.4).

From simulation we observe that the slope of voltage at node N2 (dV2/dt) is constant for different FO's (as shown in Fig. 4.5) (reason is shown in Appendix A). Therefore, the output (charging) current of inverter I1 must increase linearly with the external load capacitance (FO). The value of minimum voltage at node N1 due to SEU would, therefore, reduce appropriately, as we discuss later in this section.

Due to our procedure for extracting $I_{SEU,trip}$, as the latch load increases the trip point moves slightly towards the left along the VTC of the feedback path. This is because, after V2 reaches a value V2C, to flip the state, a larger PMOS current (in I1) is required to charge the extra FO capacitance. Since the output current of the feedback path is zero, this new (slightly smaller) value of V1C also falls on the VTC of the feedback path. This is shown in Fig. 4.3, trip point moves toward left as fan-out increases.It is important to estimate the critical charge when the latch is in hold mode. We apply an I_{SEU} as a double exponential current source on node N1 (which is held at logic 1) to determine the minimum voltage value at node N1 at which node N2 flips from logic 0 to logic 1. This minimum voltage value of node N1 is termed as V_{1ebb}. In the flipping case (when node N1 flips from 1-0), the PMOS transistor (Mp1) of inverter I1 turns ON and changes the logic level of node N2.

Our critical charge model is based on the fact that the node N2 is charged from 0 to V2C through the transistor Mp1 (current i_{Mp1}). The current through transistor Mn1 (IMn1) can be neglected because of its negative VGS. This is also supported by our simulation result where we find that the value of $i_{Mn1}/ i_{Mp1} = 0.22$ at V1 = V1ebb. Because of the SEU charging of N1, $V_{GS,p1}$ is nearly equal to V_{DD} while $V_{GS,n1}$ is nearly equal to 0. This is because the value of V_{1ebb} varies between from 20mV to -49mV for $0 \leq FO \leq 8$. Now, the KCL at node N2 due to SEU on node N1 is

$$C_{N2}\frac{dV_2}{dt} = I_{MP1} \tag{4.3}$$

Where, C_{N2} is the total capacitance at node N2. In sub-threshold region, the sub-threshold current is modeled as [147]

$$C_{N2}\frac{dV_2}{dt} = I_0 \exp\left(\frac{V_{GS,p} - |V_{TH,p}|}{nV_T}\right)[1 - \exp\frac{V_{DS}}{V_T}] \tag{4.4}$$

Where, $I_0 = \mu_0 C_{ox}\frac{W}{L}(V_T)^2 * \exp(\lambda V_{DS})$. Here, the impact of V_{DS} on i_{Mp1} can be neglected, because $V_{DS} \approx V_{DD}$ when V1 = V_{1ebb}.

V_T is thermal voltage (V_T = 26mV) V_{DS} is much larger than the V_T at room temperature therefore, the term [1-exp ($-V_{DS}/V_T$)] ≈ 1.

$$C_{N2}\frac{dV_2}{dt} = I_0 \exp\left(\frac{V_{GS,p} - |V_{th,p}|}{nV_T}\right) \tag{4.5}$$

$$V_{GS,p} = V_{DD} - V_{1ebb} \tag{4.6}$$

$$C_{N2}\frac{dV_2}{dt} = I_0 \exp\left(\frac{V_{DD} - V_{1ebb} - |V_{th,p}|}{nV_T}\right) \tag{4.7}$$

$$V_{1ebb} = (V_{DD} - |V_{th,p}|) - nV_T * \ln(\frac{C_{N2}(^{dV_2}/_{dt})}{I_0}) \tag{4.8}$$

From (4.8), we observe that V_{1ebb} has a logarithmic relation with FO's of a static D-latch. As we defined earlier, V_{1ebb} is the lowest voltage of node N1 when $I_{SEU,trip}$ is applied. As discussed earlier, dV2/dt is constant irrespective of FO load (Fig. 4.5). This implies that as the value of external load (FO) in Fig. 4.1 increases, the PMOS current (i_{Mp1}) increases linearly. Once voltage at node N1 is equal to V_{1ebb}, the feedback path (inverter followed by transmission gate I2-T2) charges node N1 till V2 = V2C, when it stops charging N1. Therefore, the critical charge $Q_{critical}$ is obtained as follows:

$$Q_{critical} = (V_{DD} - V_{1ebb}) * C_{N1} \tag{4.9}$$

Where, C_{N1} is the total capacitance at node N1. Equations (4.8) and (4.9) constitute the proposed model that will be used to calculate $Q_{critical}$ for a static D-latch. Now we discuss a method to calculate the value of $Q_{critical}$ for different FOs when the latch is operated at a different V_{DD}.

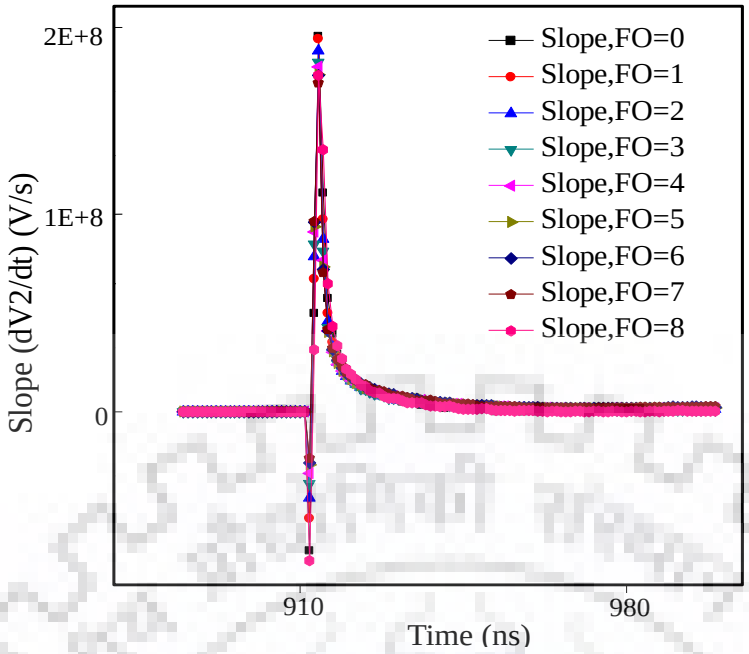


Figure 4.5 Slope (dV2/dt) vs time overlaps at trip point independent of fan-outs.

Now we describe our model to estimate the values of dV2/dt, and thereby $Q_{critical}$, at different values of V_{DD}. We used (4.8) to first estimate the value of parasitic capacitance (Cp) at node N2:

$$C_{N2} = C_p + C_g$$

$$Cp = \frac{I_0 e^{\frac{V1ebb - Vdd + vthp}{nVt}}}{\frac{dV2}{dt}} - Cg \tag{4.10}$$

We observe that the value of Cp obtained from (4.10) is almost constant within a range of suplly volatges important in sub/near-threshold regime as shown in Fig. 4.6.

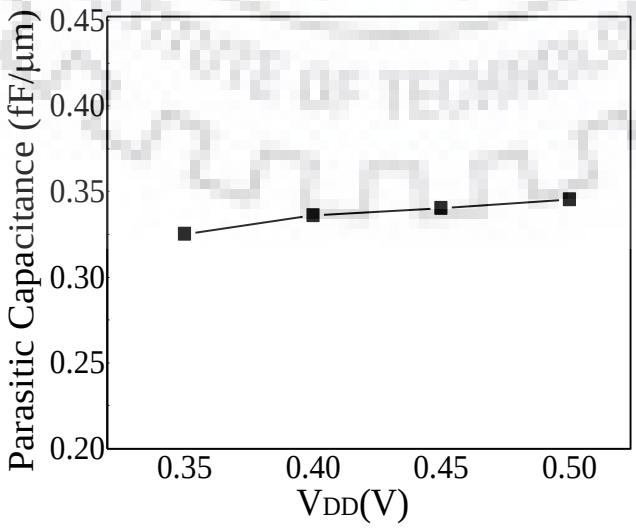


Figure 4.6 Parasitic capacitance vs V_{DD} curve independent of supply voltage at near threshold regime.

For C_L=0, since the values of C_p are equal at V_{DD} = 0.4V and at a different V_{DD}, from (4.3) we obtain,

$$\left(\frac{dV_2}{dt}\right)_{V_{DD}} = \frac{Iout,V_{DD}}{Iout,0.4} * \left(\frac{dV_2}{dt}\right)_{0.4} \tag{4.11}$$

The Main contribution of this section is the consideration of the change in the value of $Q_{critical}$ with external load of the latch. In addition we drive and validate an expression relating $Q_{critical}$ and the FO load which can be used to avoid tedious and repetitive transient simulations. We show applications of this in standard cell characterization and PVT variation aware design in the following sections. The derivation of the model has been made possible due to the following points discussed in this section:

- The value of V_{1ebb} reduces with increasing values of C_L because of the increase in the time in charging the node N2 to the value V2C.
- The values of dV2/dt remain unchanged with increasing values of C_L.
- The value C_p for an SEU flipping should be obtained using (4.10). This value is constant irrespective of V_{DD}.

The same procedure is followed when an SEU occur at node N2. In this case the load capacitance is fixed. A similar model for the value of $Q_{critical}$ for the case of a 0-to-1 flip at node N1 can be developed. However, a 1-to-0 flip at node N1 is the most important SEU event for a static D-latch. This is because, as reported in [148], the value of $Q_{critical}$ is determined only at that susceptible node which has the lowest value of $Q_{critical}$. Such node is referred to as the most susceptible node and can be determined by simulation [149]. The node N1 (please refer Fig. 4.1) has lowest $Q_{critical}$ during the hold mode as compared to the other intermediate nodes [150]. Using simulations, we also verified that for the static D-latch the lowest value of $Q_{critical}$ is indeed at the node N1. It has been reported that node N1 is more vulnerable to soft errors in case of a 1-to-0 flip as compared to 0-to-1 flip case [148]. Using simulations, we observe that the $Q_{critical}$ for a 0-to-1 flip is about 14 X larger than that for a 1-to-0 flip at node N1. This can be explained in the following manner: A high energy particle strike in the drain of a MOSFET creates and an extended depletion region (funnel). Due to the high energy of the particle electron hole pair (EHP) generates with in this funnel. Due to the electric field in the funnel EHPs are separated; the electrons (holes) move towards the drain in n-MOSFET (p-MOSFET). The hole transit (p-MOSFET) towards the drain within the funnel depletion region would be slower than that of the corresponding electron transit (n-MOSFET). This gives rise to a higher

recombination of generated holes and thus a smaller SEU charge in a p-MOSFET for a given amount of heavy ion charge strike.

The following procedure is employed by us to obtain the critical charge data for the Static D-latch, which is used to develop and validate our model:

Step1: Find out the trip point of a latch when there is no external output load (C_L = 0). The trip point is calculated by applying a double exponential current source (I_{SEU}) on susceptible node N1. At the trip point we calculate the value of V_{1ebb}.

Step2: The next step is the determination of the slope (dV2/dt) at the output node (N2) when V1= V_{1ebb} keeping when C_L=0.

Step3: Determine the inputs capacitance of inverters (capacitance/um), as done in [151].

Step4: Now we determine the parasitic capacitance at node N2. By using (4.8) we get the value of parasitic capacitance:

$$C_{N2} = C_p + C_g \tag{4.12}$$

$$Cp = \frac{I_0 e^{\frac{V1ebb - Vdd + vthp}{nVT}}}{\frac{dV2}{dt}} - Cg \tag{4.13}$$

Where, C_p is the parasitic capacitance and, C_g is the gate capacitance, for a given technology node the values of I_0, V_{thp}, n, V_T, are fixed and the value of slope (dV2/dt) is obtained in Step 2.

Step5: Update the value of C_L for FO1 load. Repeat Step 1-4. Now, by using (4.8) varying the FO's of the static latch and calculating the corresponding value of V_{1ebb} at V_{DD} = 0.4V.

Step6: Now using (4.9), we calculate the value of $Q_{critical}$.

Step7: For evaluating V_{1ebb} at other V_{DD}'S. First we draw VTC by using DC simulation for both path (main and feedback) of the static D-latch without FO load at V_{DD}=0.4V. The intersecting point of both VTC's gives the value of V1C and V2C at V_{DD} =0.4V. Same procedure is followed for another V_{DD} for which we next calculate V_{1ebb}.

Step8: Now, from DC simulations calculate the value of $I_{out,VDD}$ (= I_{Mp1}-I_{Mn1}) when V2 = V2C at node N2 for both the voltages.

Step9: Next step is that of obtaining the slope (dV2/dt) using simulations for another V_{DD}.

Step10: Now repeat step 5 to 7 for calculating $Q_{critical}$ at new value of V_{DD}.

4.3 Critical Charge Model Validation

In this section, the proposed critical charge model is validated using SPECTRE and TCAD mixed-mode simulations. For SPECTRE simulations STMicroelectronics 65-nm PDK is used. For TCAD simulations, we used calibrated simulation setup as discussed in our group's earlier work [145].

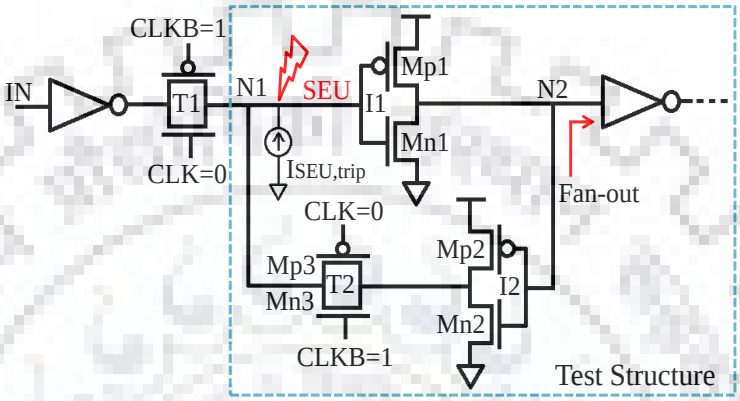


Figure 4.7 Test circuit to emulate soft error at node N1 in the Latch with a fan-out load.

The test structure for validation is shown in Fig. 4.7. The procedure followed for determining for critical charge for different values of C_L, V_{DD} and temperatures. All DC and transient simulations are done using Cadence Virtuoso IC6.1.5-64b. The critical charge model is verified for appropriate ranges of power supply voltages (V_{DD}), FO loads and temperatures. In simulations, for both the inverters (I1 and I2) W_p/W_n ratio is kept at 2, whereas, the channel lengths are kept at allowed minimum values. For the feedback transmission gate (T2), the values of W_{Mn3} and W_{Mp3} are kept equal to the W_{Mn1} (please refer to Fig. 4.7), as discussed in [138]. First we simulate the test structure (please see Fig.4.7) and extracted critical charge at V_{DD}=0.4V for different fan- outs. For this, we follow steps 1-5 describe in the simulation procedure in the previous section. We then estimate the value of dV2/dt at a different V_{DD} using (4.11). Using (4.8) and (4.9), we calculate the values of $Q_{critical}$ for different FOs at this new V_{DD}. We also obtain the values of $Q_{critical}$ at this new V_{DD} following steps 6-10 in the simulation procedure described in section 4.2.

Figure 4.8(a), Figure 4.8(b), Figure 4.8(c), and Figure 4.8(d) shows the comparison of calculated $Q_{critical}$ values using our model and those obtained from simulations with different FOs at V_{DD} = 0.35V, V_{DD} = 0.40V, V_{DD} = 0.45V, and V_{DD} = 0.50V, respectively. The critical

charge is compared for different V_{DD} with a FO range of 1 to 8, which is typical [152] in a critical path. In all the simulations results, the proposed model's calculated values are represented using symbols and the simulated values (from SPECTRE/ TCAD) are shown with lines. Figure 4.8 shows that the critical charge estimated using our model matches well with the simulation results with a maximum error of 3.4%. The model is benchmarked against simulation results only because, to the best of our knowledge, there is no previous model addressing this problem.

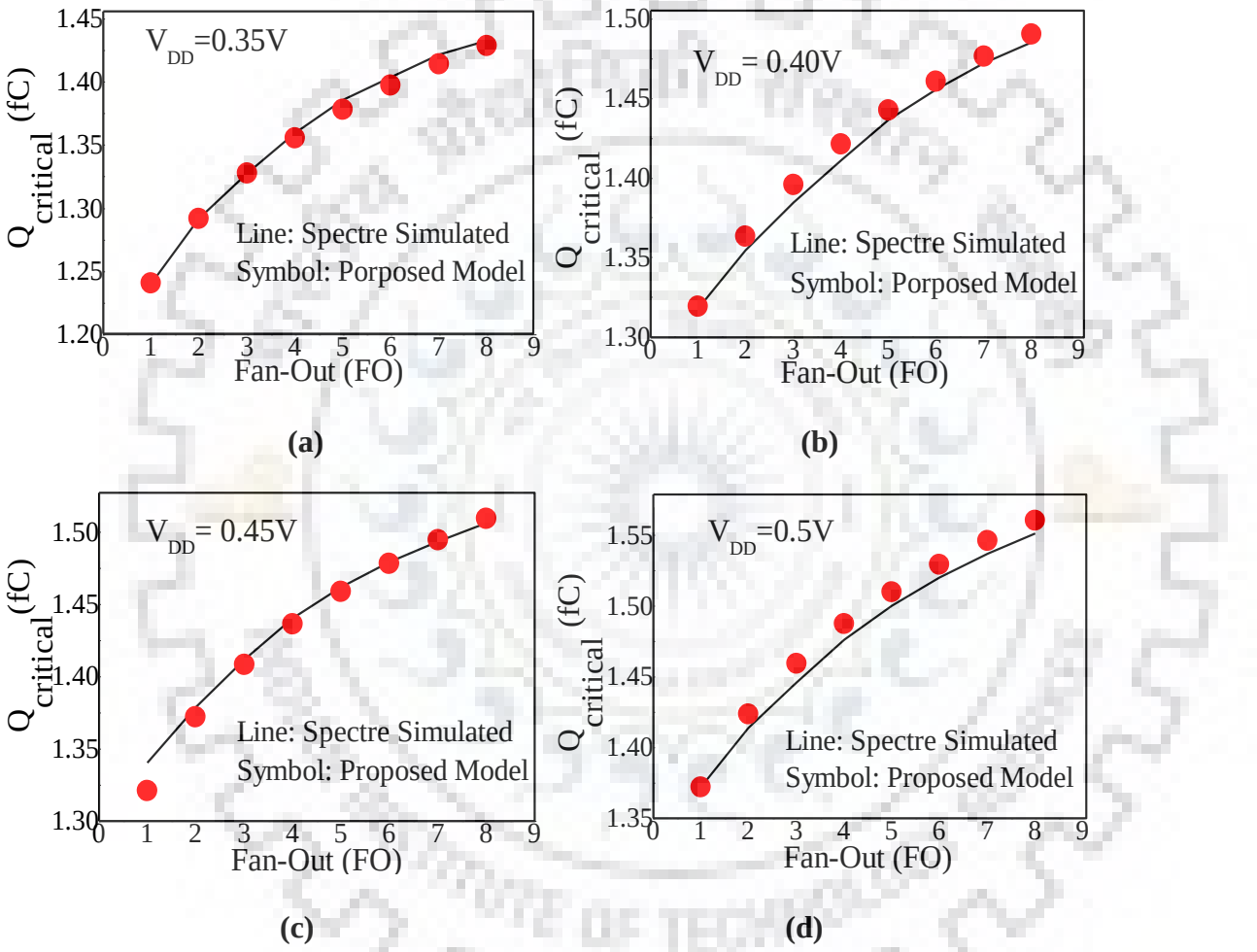


Figure 4.8 Validation of the proposed model with SPECTRE simulation for Qcritical calculation at (a) V_{DD} = 0.35V, (b) V_{DD} = 0.4V, (c) V_{DD} = 0.45, and (d) V_{DD} = 0.5V in STMicroelectronics 65-nm CMOS technology at 25^0 Temperature .

We also validate the proposed model for three important temperature values (-40°C, 25°C, and 125°C) at V_{DD} = 0.4V. In (4.8) we change the value of thermal voltage (V_T) is accordingly updated. Figure 4.9 show that the critical charge estimated using our model matches well with simulations done for different temperatures (-40°C, 25°C, and 125°C) with a maximum error of 1.5%.

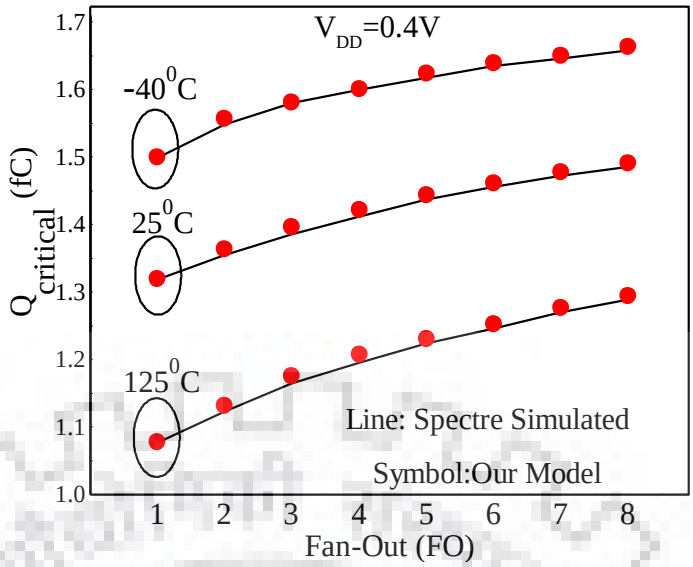


Figure 4.9 Validation of the proposed model with SPECTRE simulation for Qcritical estimation at different temperatures (-40°C, 25°C, and 125°C) at V_{DD}=0.4V in STMicroelectronics 65-nm CMOS technology.

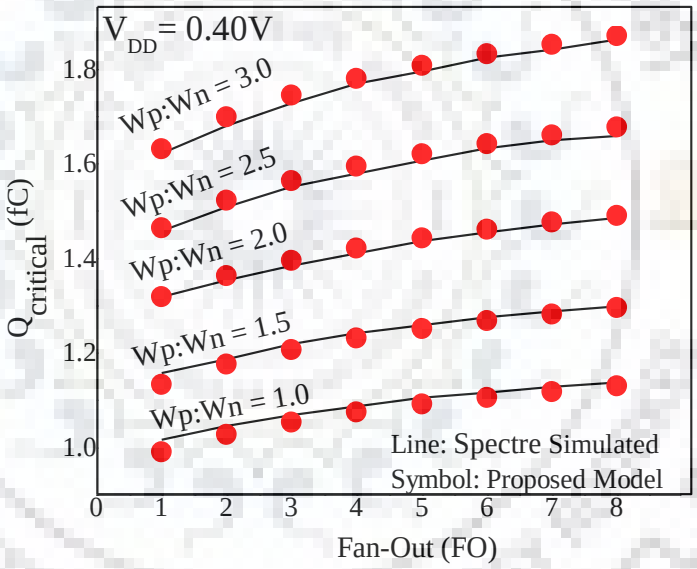


Figure 4.10 Validation of the proposed model with SPECTRE simulation for Qcritical estimation at different beta ratio (1, 1.5, 2, 2.5, and 3) at V_{DD}=0.4V in STMicroelectronics 65-nm CMOS technology at 25^0 Temperature.

We also validate the proposed model for different beta ratio values 1, 1.5, 2.5, and 3 for the evaluation of critical charge of the static D-latch. Figure 4.10 shows that the impact of beta ratio on critical charge of the static D-latch. It can be observed from Fig. 4.10 that the as beta ratio increases, critical charge also increases for a particular FO load. This is because, as the beta ratio increases gate capacitance at node N1 also increases. Consequently, critical charge of the D-latch increases. We can see from the Fig. 4.10 that the proposed model predicts the impact of beta ratio accurately.

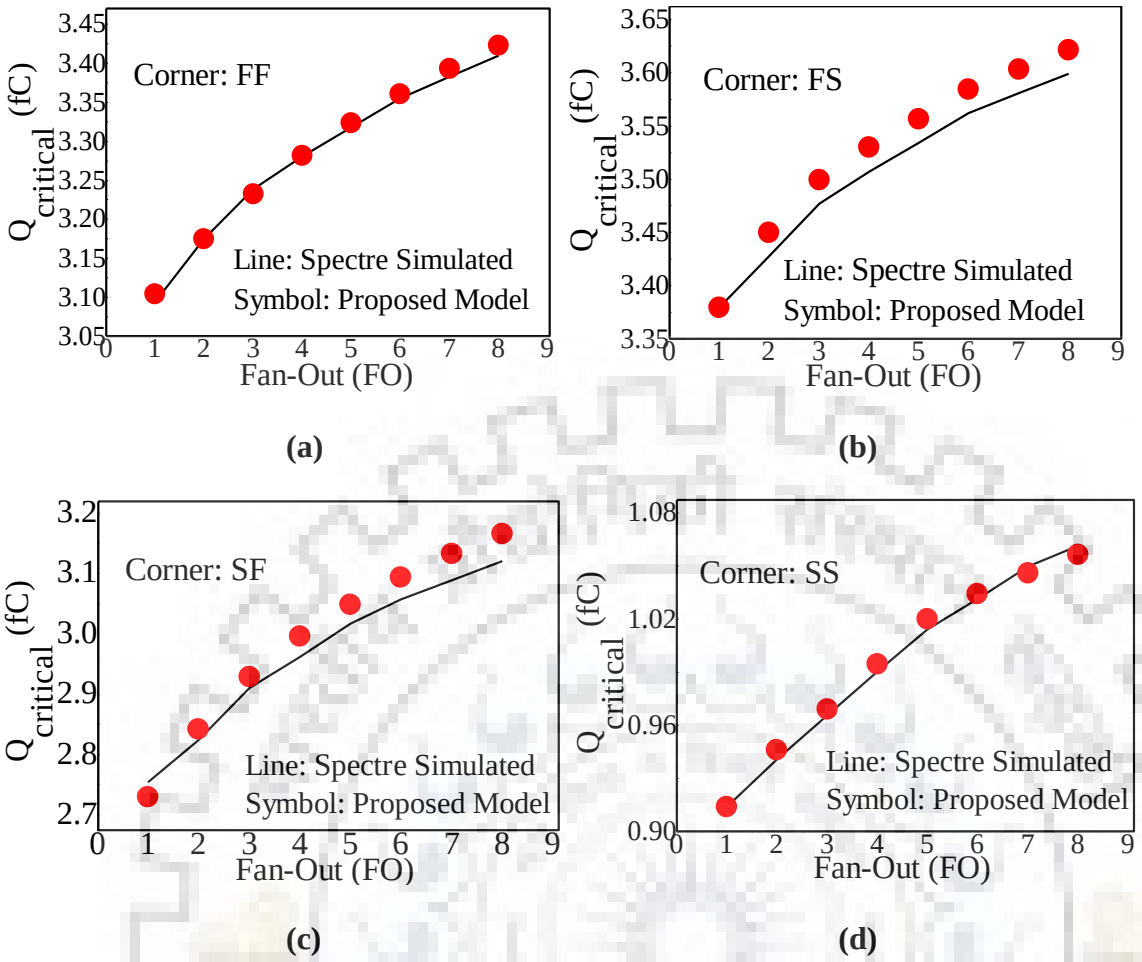


Figure 4.11 Validation of the proposed model with SPECTRE simulation for different corners Qcritical calculation at V_{DD} = 0.40V in (a) FF, (b) FS, (c) SF, and (d) SS in STMicroelectronics 65-nm technology

The comparison of $Q_{critical}$ estimated by the proposed method with $Q_{critical}$ measured from the simulation at four different process corners, namely, Fast Fast (FF), Fast Slow (FS), Slow Fast (SF), and Slow Slow (SS) in STMicroelectronics 65-nm CMOS technology node is shown in Fig. 4.11 at a supply voltage of 0.40V. For estimating $Q_{critical}$ using our model, we first extracted the values of I_0 and $V_{TH,p}$ in (4.8) using DC simulations at FF, FS, SF and SS corners. From this comparison, it is observed that for all the corners, the proposed model is in good agreement with the simulations with a maximum error 8.2% in FS and SF corners.

We also validate the proposed $Q_{critical}$ model in TACD calibrated 32-nm CMOS technology [145]. Figure 4.12 compare the I-V of MOSFETs simulated using our calibrated simulation setup to the experimental results [153]. Figure 4.13 show the comparison of calculated $Q_{critical}$ values using the proposed model and measured using Sentaurus TCAD mixed mode simulations at different fan-outs at V_{DD} = 0.30V, and V_{DD} = 0.40V. The value of dV2/dt was extracted for V_{DD}=0.4V in our model based approach using (4.11), as discussed in Section 4.2.

Figure 4.12 shows that the $Q_{critical}$ calculated employing the proposed model matches well with simulation results with a maximum error of 7.50%. The Heavy-ion models are used in the TCAD mixed mode simulations. The Linear energy transfer (LET) value increases with the FO's of the static D- latch. In our TCAD simulations, the heavy-ion strikes at the center of the drain of the affected transistor.

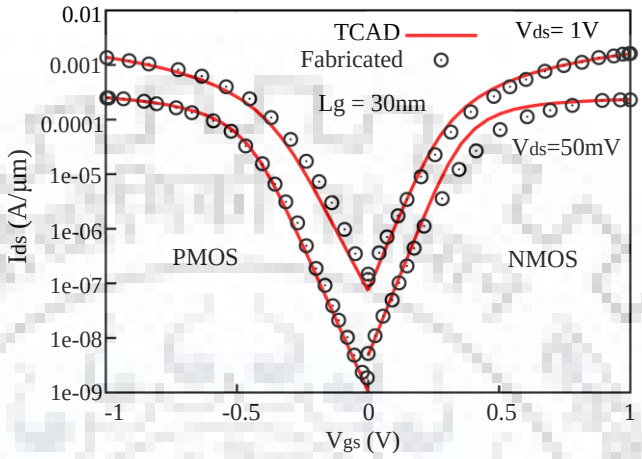


Figure 4.12 Calibration of the TCAD models [145] with data form fabricated devices given in [153] for Lg = 30 nm

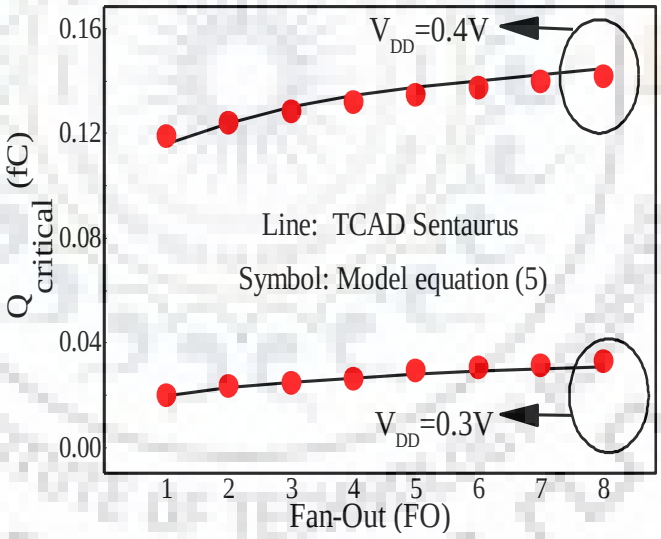


Figure 4.13 Validation of the proposed crtical charge model with TCAD- Sentaurus mixed mode simulations for Qcritical calculation at V_{DD} = 0.30V, and V_{DD} = 0.40V at 25^0 C Temperature in 32-nm CMOS technology node.

The proposed model accurately estimates the value of $Q_{critical}$ at different FOs; therefore, it validates the estimation of the $Q_{critical}$ for latches in NTV standard cell library characterization. Using our model we also calculate the values of $Q_{critical}$ at different V_{DD}s, temperatures and process corners accurately. Therefore, our model can be used to determine $Q_{critical}$ values PVT variations. We discuss this in the following section.

4.4 Variability Analysis of the Proposed Critical Charge Model

In order to investigate the impact of process variations on the critical charge model, we vary supply voltage (V_{DD}), threshold voltage (V_{TH}), temperature, and fan-out load (C_L) in SPECTRE and in the proposed model.

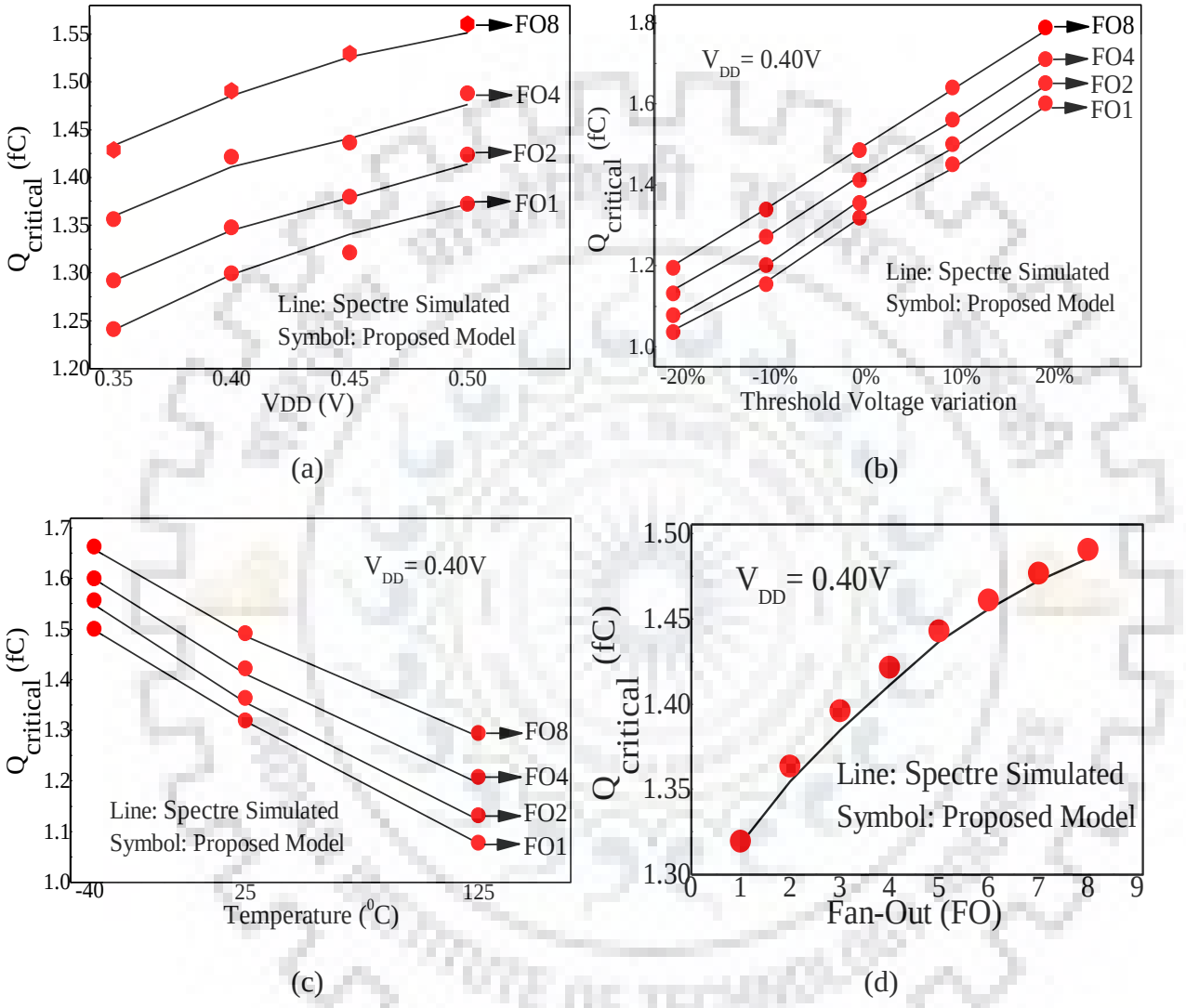


Figure 4.14 Validation of the proposed model with SPECTRE simulation for Qcritical estimation at (a) V_{DD} variations, (b) V_{TH} variations, (c) Temperature variations, and (d) fan-out load variations.

4.4.1 Supply Voltage Variation

From (4.8) and (4.9) we observe that, the critical charge is proportional to the V_{DD} of the static D-latch. Using this we conclude that, decrease in latch supply voltage linearly decreases Qcritical of the susceptible node of the static D-latch. For a given fan-out load Qcritical decreases with reduction in the supply voltage. From Fig. 4.14(a) we also verify our calculations based on (4.8) and (4.9) with simulations.

4.4.2 Threshold Voltage Variation

From (4.8) we observe that, the minimum voltage of node N1 (V1ebb) is directly proportional to threshold voltage (V_{TH}) of the PMOS transistor. As increasing the V_{TH} from the nominal V_{TH}, $Q_{critical}$ on the susceptible node also increases. This is because a higher V_{TH} of PMOS transistor implies a lower V_{1ebb}, consequently, requires a larger value of Qcritical to upset the vulnerable node of the latch. Effects of V_{TH} variation on $Q_{critical}$ is shown in Fig. 4.14(b), where our calculation match with simulations. In this Figure, the 0% shows a point on the x axis corresponds to the nominal values of V_{TH}.

4.4.3 Temperature Variation

Furthermore, the effect of the temperature on the $Q_{critical}$ is obtained by using (4.8). In (4.8) thermal voltage (V_T) changes according to the temperature. As temperature increases $Q_{critical}$ of the vulnerable node is decreases. This is because as temperature increases thermal voltage also increases. From Fig. 4.14(c) we also see that for a given fan-out load $Q_{critical}$ decreases with increment in temperature.

4.4.4 Fan-out load Variation

As fan-out of the gate increases the load capacitance of the driving gate also increases due to the gate capacitance of driven gates. From (4.8), we observe that V_{1ebb} has a logarithmic relation with FO's of a static D-latch. V_{1ebb} is the lowest voltage of node N1 when $I_{SEU,trip}$ is applied. As discussed earlier, dV2/dt is constant irrespective of FO load. This implies that as the value of external load (FO) increases, the PMOS current (I_{Mp1}) increases linearly. As fan-out load increases critical charge of the latch also increases, this is due to the logarithmic dependence of V_{1ebb} on FO's load. From Fig. 4.14 (d) we also see that for a given supply voltage Qcritical increases with the FO load.

4.4.5 Statistical Variability

Transistor parameters are affected due to process variations which results in Qcritical variation of the static D-latch. Random dopant fluctuations (RDF) and channel length variations are the main sources of process variations that affect the transistor parameters. RDF and channel length variations in MOSFET impact directly on transistor threshold voltage [154]. Therefore, to

validate our model against process variations we varied the threshold voltage of transistors in the static D-latch.

To verify the statistical variability of the proposed model in NTV regime, we have done 5,000 Monte Carlo (MC) simulations. To validate the variability, critical charge estimated by the proposed model is compared to the Monte Carlo simulations. In MC simulations 3σ V_{TH} variation is used at 25°C temperature. From MC simulations, the value of the Qcritical is determined. Figure 4.15 shows the critical charge of the static D-latch with FO1 load for 5,000 MC simulations obtained using HSPICE simulation and the proposed model. From Fig. 4.15, we observe that our model estimates the critical charge variation due to the process variability accurately. Therefore, the proposed model is quite accurate to estimate the critical charge variability with the statistical variations.

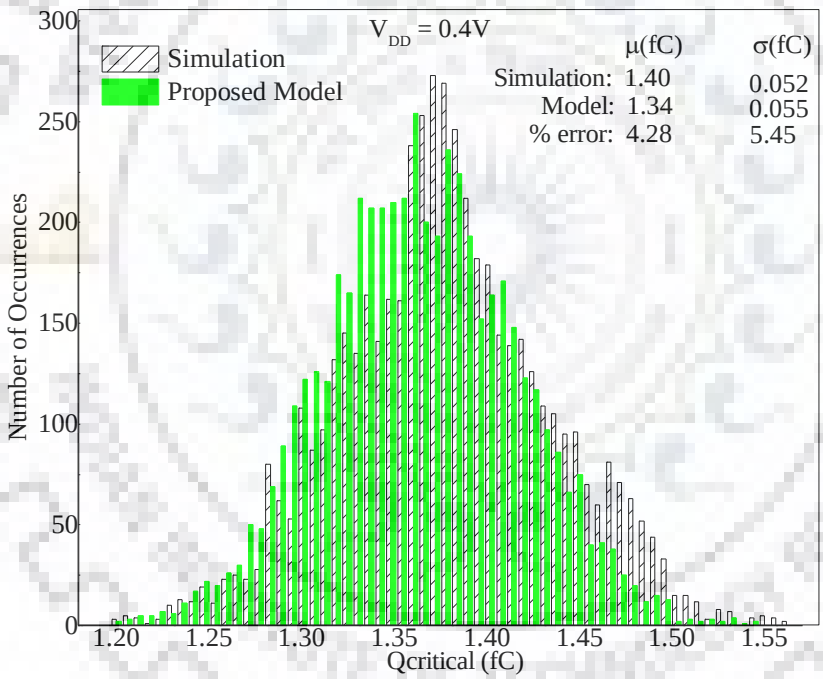


Figure 4.15 Critical charge of static D-latch with FO1 load for 5,000 Monte simulations obtained using HSPICE simulations and the proposed model at V_{DD} = 0.4V and Temperature=25°C.

4.5 Methodology to Estimate Critical Charge

In this section, we proposed a methodology to determine critical charge for a static D-latch based on our models discussed in section 4.2. In this methodology the change in the values of critical charge due to PVT variations is also estimated. For a given PVT corner, the value of critical charge is determined form CL = FO0 to CL = FO8, which covers typical critical path loads. This methodology is discussed in algorithm 1 and the flow chart in Fig. 4.16.

Algorithm 1: Modeling and Analysis of estimating $Q_{critical}$

Input: Model file, SCL_Netlsit.cir, Cgcalc.cir, ioutxcal (V_{DD}), V_{DD} range, load range, Temp. range

Output: $Q_{critical}$ variation with respect to Fan-Out Load, V_{DD}, and Temp.

Tools: Cadence Spectre for simulations, Python for scripting

Procedure BEGIN:

FOR each cell in SCL_Netlsit.cir do

Initial set V_{DD}=0.4V and C_{load}=0, Temp= 25

UNTIL state flips ⟶ Apply I_{SEU} at N1 and Monitor logic state of N2

IF state flips **then**

V_{1ebb} ⟵ minimum voltage at V1

Differentiate V2 to obtain $\frac{dV2}{dt}$ at time (V_{1ebb})

C_g(/um) ⟵ C_{gcal} (Cgcalc.cir)

C_p (/um) ⟵ from equation

$$Cp = \frac{Ie^{\frac{V1ebb-Vdd+vthp}{nVt}}}{\frac{dV2}{dt}} - Cg$$

Iout0.4 ⟵ ioutxcal(V_{DD} = 0.40V)

end if

CALCULATE $Q_{critical}$ for C_L = 0

FOR each Temp < max (Temp. range) **do**

FOR each V_{DD} < max (V_{DD} range) **do**

FOR each FOs < max (load range) **do**

V_{1ebb} ⟵ V_{DD}-V_{thp}- nV_T ln((C_L)*dV2/dt)/I_0)

$Q_{critical}$ = (V_{DD}-V_{1ebb}).C_{N1}

end for

Update V_{1ebb}, $Q_{critical}$ Tables and V_{DD}

Update $I_{out}(V_{DD})$ ⟵ ioutxcal(V_{DD})

Update dV2/dt ⟵ $(dV2/dt)=(I_{out}(V_{DD})/I_{out}(0.4))*(dV2/dt)\_0.4$

end for

end for

end for

PRINT V_{1ebb} and $Q_{critical}$

Procedure END

Compute ioutxcal (V_{DD})

First we draw VTC by using DC simulation for both the paths (main and feedback) of static D-latch with $C_L = 0$ for $V_{DD} = 0.40V$ and other VDD's in the V_{DD} range. The Intersection point of both the VTC's gives the value of V1C and V2C. Using DC simulations, obtain the values of I_{Mp1}-I_{Mn1} (I_{out}) when the voltage of the node N2 is V2C for a given V_{DD}. Ioutxcal (V_{DD}) = Iout.

Set VDD = 0.4V and $C_{load} = 0$

Compute Cgcalc.cir as done in [151].

The time Complexitiy of the proposed model is $O(N^3)$, where, N is number of inputs.

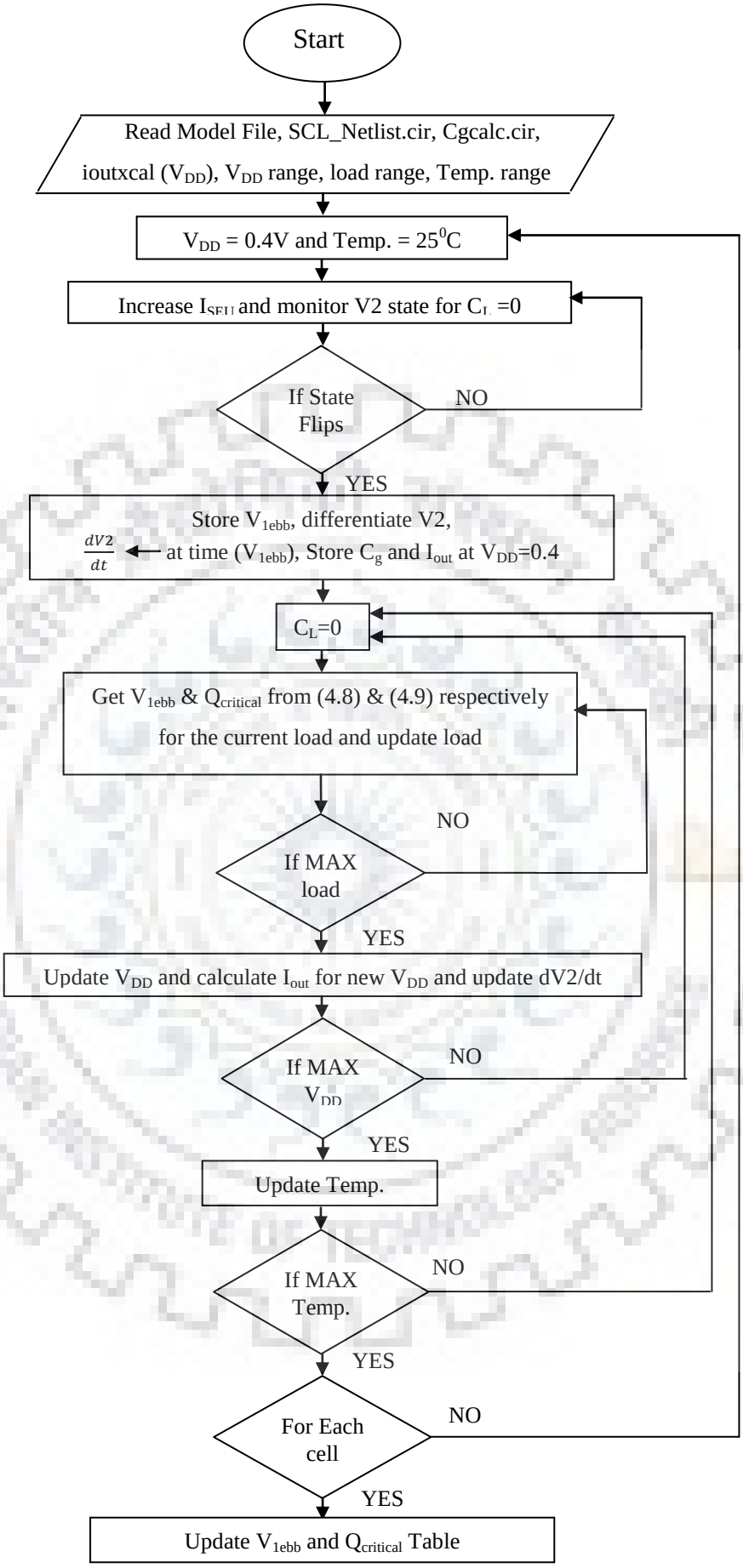


Figure 4.16 Flow chart of the proposed methodology for estimating Qcritical

4.6 Summary

Susceptibility of sequential elements to soft errors due to single event upset is high in the near/sub-threshold voltage regime, due to their low operating voltage and smaller node capacitances. This chapter, presents a physics based semi-analytical model to estimate the critical charge of a static D-latch as a function of its fan-out load, supply voltage, temperature and the transistor level parameters. To develop this model, we first argue that the value of the critical charge is increases with fan-out load. Based on this model, we propose a procedure to estimate the critical charge using a few DC simulations and a single transient SPECTRE simulation for a given PDK. In this methodology, we calculate the critical charge for latches in an NTV standard cell library. This method results in an estimate of the latch's critical charge for different values of fan-out load, supply voltages and temperature. The proposed methodology estimates the critical charge of a static D-latch with a maximum error of 3.4% at different power supply compared with SPECTRE simulations in STMicroelectronics 65nm PDK. The proposed model results in 7.5% error at 32 nm technology node which is verified using our calibrated TCAD simulation setup. Further, the model predicts the changes in the critical charge accurately for different process corners. This methodology also addresses the issue of critical charge due to PVT variations.

5 CHAPTER

Energy Efficient Radiation Hardened Latch Designs

5.1 Overview

In order to overcome the extensive Monte-Carlo circuit simulations, an accurate semi-analytical model to estimate the critical charge for the static D-latch operating in the near-threshold voltage (NTV) regime is reported in the previous chapter. However, the static D-latch is more prone to soft errors because of its lesser critical charge due to technology scaling and NTV operation. Terrestrial soft errors occur in electronic circuits either from alpha particles originated from packaging or neutron particles from cosmic rays. Due to soft error a transistor which is in OFF state starts conducting temporarily and changes the logic level of an affected node. Moreover, due to the reduction in the magnitude of node capacitance and inter node spacing, striking of an energy particle may affect multiple nodes. Due to charge sharing, if two adjacent nodes are affected in a latch, then it is known as a double node upset (DNU). If three adjacent nodes are affected in a latch, then it is known as triple node upset (TNU). Radiation hardened by design (RHBD) techniques provides best solution to tolerate radiation-induced transient faults. From the last decade, vast research in the field of radiation hardened latches against multiple nodes upset (MNU) due to soft errors is carried out. To solve these problems first we have proposed an energy efficient single node upset (SNU) tolerant latch. The proposed SNU tolerant latch consist of a set of three transmission gates, a memory cell and a Muller C- element (MCE) to enhance SNU tolerance to achieve more robustness compared to the recently reported SNU hardened latches [91]-[104]. Further we have proposed an energy efficient DNU hardened latch that is based on our SNU tolerant latch. The proposed DNU tolerant latch improves the D-Q delay and area energy delay product (AEDP) as compared to other existing DNU hardened latches [105]-[111]. This is achieved by employing cross connected pull-up and pull-down memory and multiple MCEs. Finally we have proposed a TNU hardened latch. The proposed TNU hardened latch features a lower susceptibility against soft error, a smaller delay and area compare to the recently reported TNU hardened latches [112] and [114].

The working principle, implementation, and soft error robustness of the proposed SNU, DNU, and TNU hardened latches is presented in section 5.2. The simulation and comparison results in

STMicroelectronics 65-nm CMOS technology is presented in section 5.3. Sentaurus TCAD mixed mode simulations are carried out to validate the soft error robustness of the proposed latches in 32-nm CMOS technology is presented in section 5.4. Section 5.5 summarizes the chapter.

5.2 Proposed Latch Designs

5.2.1 Proposed Single Node Upset Tolerant Latch

The schematic and the layout of the proposed SNU hardened latch are shown in Fig. 5.1 and Fig. 5.2, respectively. The circuit consists of a set of three transmission gates, a memory cell and a clocked Muller C-element (MCE). The proposed latch is transparent in the positive phase of the clock cycle. In the case of transient fault (TF), internal nodes of memory cell retain the correct data. Clocked MCE retains the state during high phase of clock signal. While in fault free case, input data propagates to output through transmission gate T3.

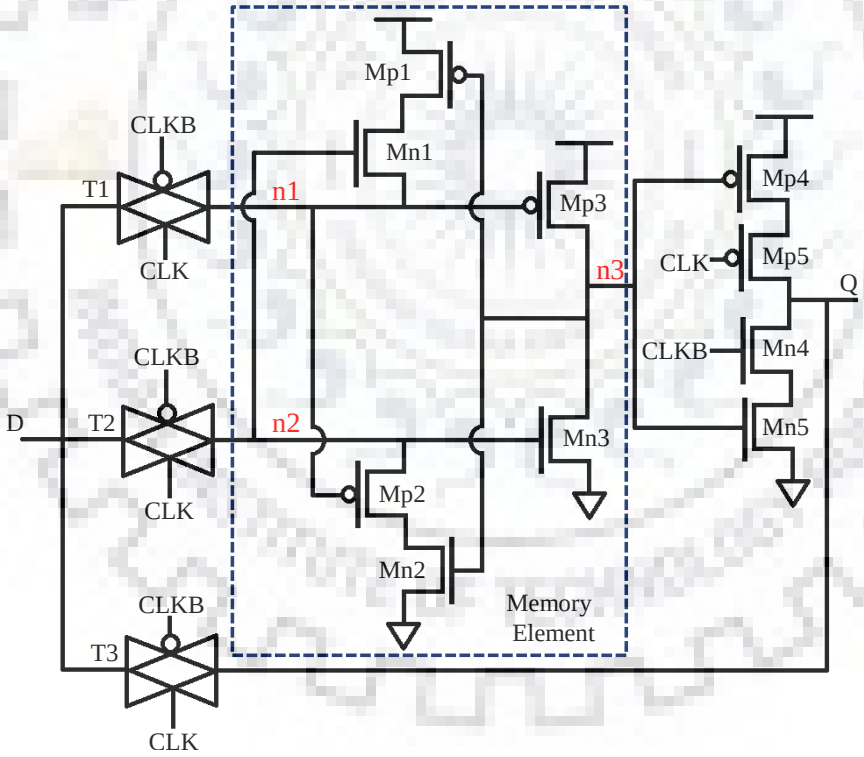


Figure 5.1 Schematic of the proposed high performance, low area and SNU tolerant latch.

The basic principle of SNU hardening of the proposed latch is as follows: Consider the soft error case (when CLK = 0) in which a transient fault occur at one of the intermediate node (n1, n2, or n3) of the latch. This transient fault never switches the output signal because the value on affected node can be restored by the states on the other two nodes. In the presence of single

event upset (SEU), our latch automatically corrects the error by using a memory element. The advantage of our technique is that it improves the performance and area of the latch also.

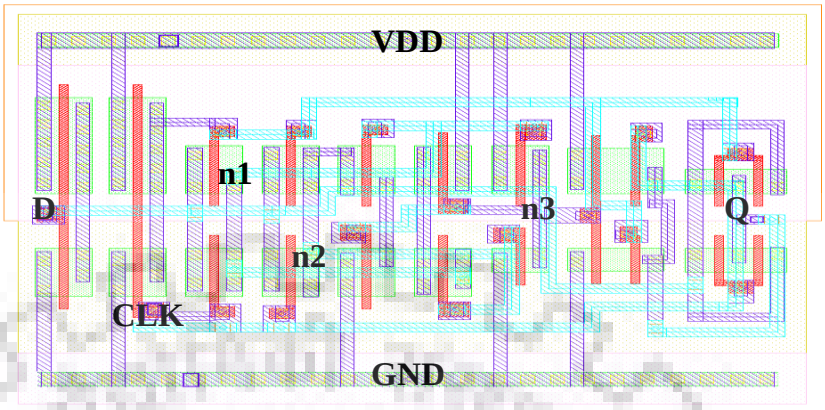


Figure 5.2 Layout of the proposed high performance, low area and SNU tolerant latch

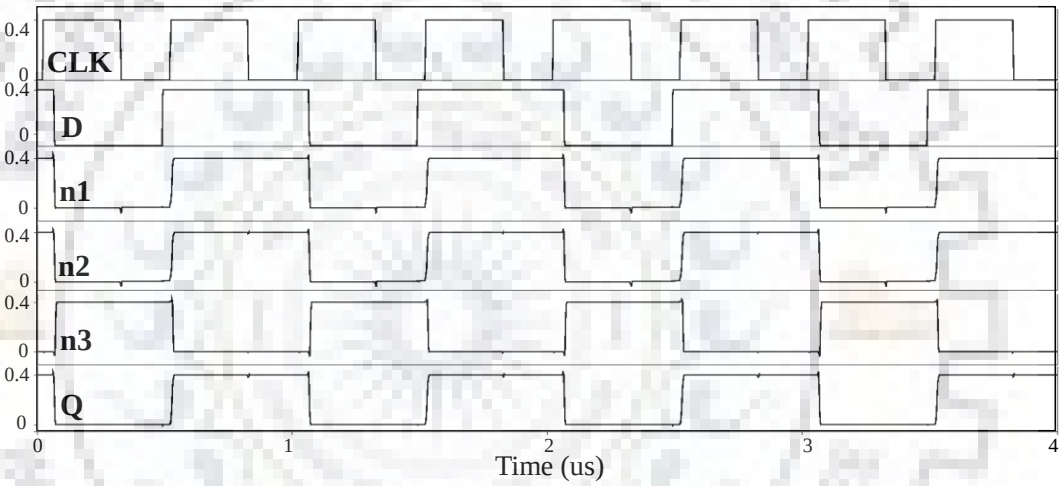


Figure 5.3 Post-layout simulated waveforms of the proposed SNU hardened latch for a fault free case in the STMicroelectronics 65nm CMOS technology at 0.4 V supply voltage.

The schematic of the proposed SEU tolerant latch is shown in Fig. 5.1. When clock is high (CLK = 1), transmission gate T1, T2, and T3 turn ON and the latch operates in transparent mode. The input data (D) is propagating to output (Q) through transmission gate T3. In this case memory cell stores the value of D and node n3 and output signal Q are electrically isolated by clocked MCE. When clock is high MCE is turned OFF to reduce propagation delay and power dissipation. When clock is low (CLK = 0), transmission gate T1, T2, and T3 are turned off and latch is working in hold mode. Clocked MCE turns ON, therefore, the latches are in holding state and the output of the MCE retains the same state. In this case the latch retains the pervious data on output node of the proposed latch. Figure 5.3 shows the simulated waveforms for the proposed radiation hardened latch considering a fault free case.

Further, we discuss the proposed latch's response to TF. Suppose that logic 1 is written at nodes n1 and n2 in the hold mode (i.e. CLK = 0 and CLKB = 1) while logic 0 is stored on node

n3. When a high energy particle destroys the state of one of the intermediate nodes, its state is restored because it is driven by the other two intermediate nodes. Suppose, a TF occurs on the node n1 while the node holds logic 1. This fault is not be propagated to the output node and n1 is restored to logic 1, because the transistors Mp1 and Mn1 are kept ON by the voltages of n3 and n2, respectively. Therefore, the output will not be corrupted by an SEU. Now, we consider a transient fault on node n2 while it holds logic 0. The fault cannot be propagated on output node because in this case Mp2 and Mn2 transistors are ON by logic stored on n2 and n3, respectively. As a result, the correct logic 0 is restored on the internal node n2. Now, we consider an error on node n3. Suppose logic 1 is stored on node n3, in this case a transient fault occurs on node n3 and changes the state of the node to logic 0. This faulty state can be recovered by transistor Mp3 because logic state on node n1 is at logic 0 and turns on transistor Mp3. Consequently, state on node n3 retains its corrected value and hence the fault cannot be propagated to the output node. Figure 5.4 shows the post layout waveforms of the proposed latch when the particle strikes on nodes n1, n2 and n3 inside the memory cell at 1.78ns, 0.41ns and 3.35ns, respectively. Thus, the injected SEU cannot affect the output node Q of the proposed SNU hardened latch.

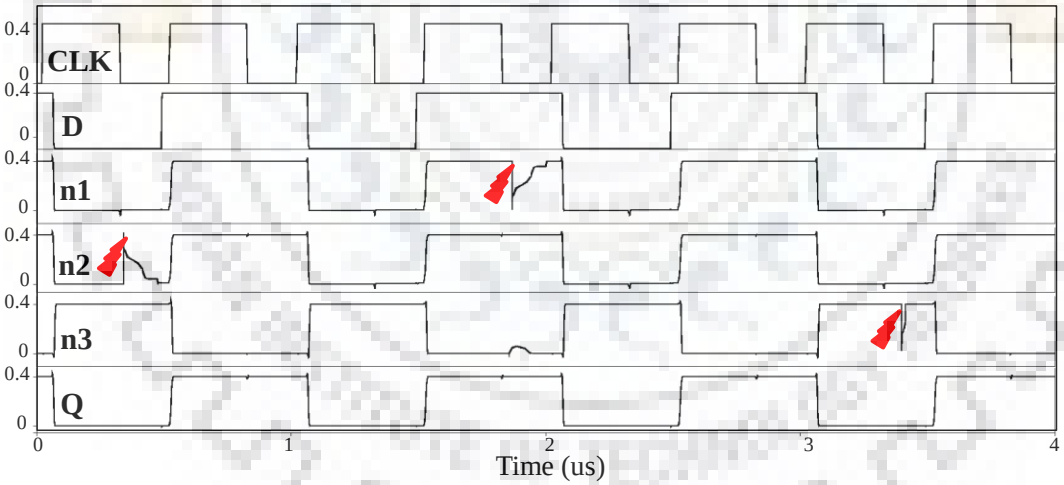


Figure 5.4 Post-layout simulated waveforms of the proposed SNU hardened latch when a particle strikes on nodes n1, n2, and n3.

5.2.2 Proposed Double Node Upset Tolerant Latch

The schematic diagram and the layout of the proposed DNU hardened latch are shown in Fig. 5.5 and Fig. 5.6, respectively. The proposed DNU hardened latch circuit consists of a set of four transmission gates, a memory element, a 3-input MCE and a 3-input clocked MCE. In the proposed DNU hardened latch, CLK is the clock signal, and CLKB is the inverted clock signal. When clock signal is high (CLK = 1), transmission gates T1, T2, T3, and T4 turn ON and the latch operates in transparent mode. The input data (D) propagates to output (Q) through T4.

The input nodes of the memory cell are driven by D through T1 and T2. In the transparent mode the value of D stores at nodes n1, n2, n3, n4 and n5. Node n4 and output signal Q are electrically isolated by 3-input clocked MCE. In this case 3-input clocked MCE is turned OFF to reduce propagation delay and power dissipation.

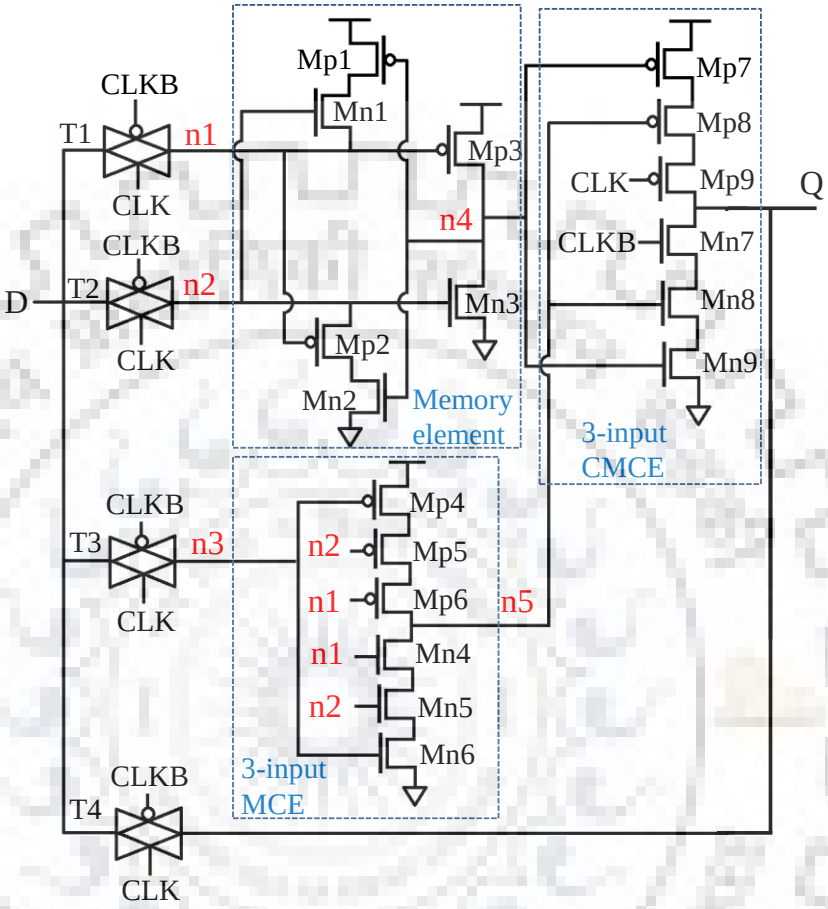


Figure 5.5 Schematic of the proposed high performance, low area and DNU hardened latch.

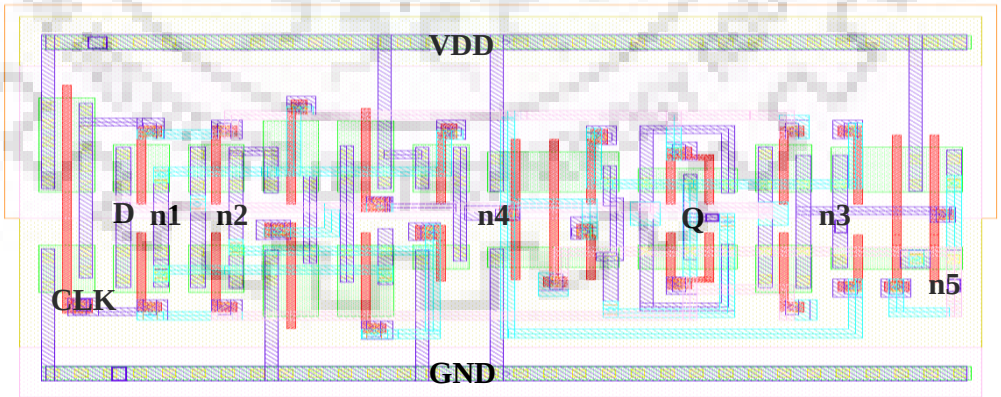


Figure 5.6 Layout of the proposed high performance, low area and DNU tolerant latch

When the clock is low (CLK = 0 and CLKB = 1), transmission gate T1, T2, T3, and T4 are turned OFF and the latch is working in hold mode. The 3-input clocked MCE turns ON, therefore, the latches are in holding state and the output of the clocked MCE retains the same state. In this case the latch retains the pervious data on output node of the proposed DNU

hardened latch. Figure 5.7 shows the post-layout simulated waveforms for the proposed DNU hardened latch in fault free case.

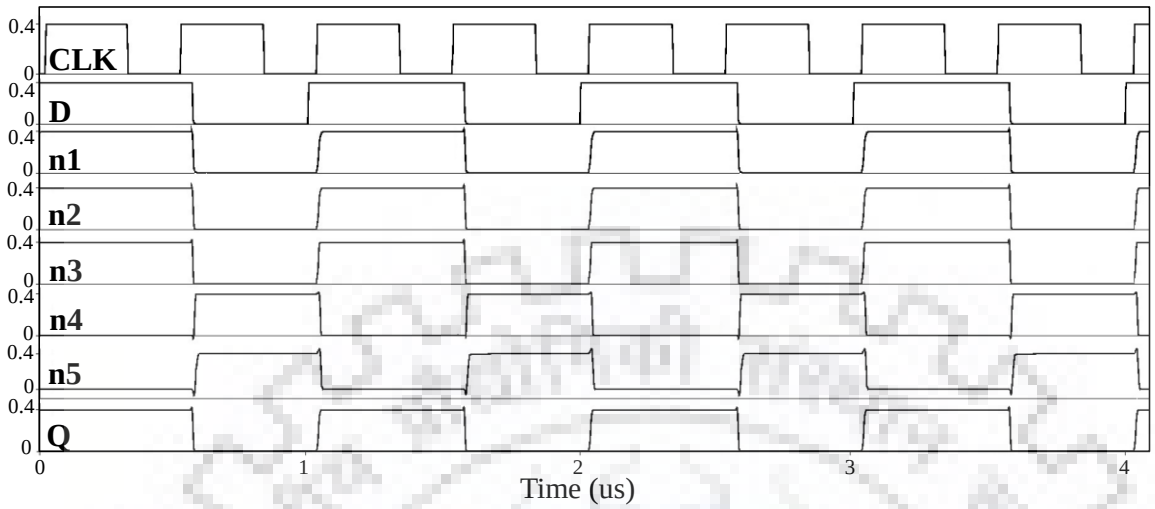


Figure 5.7 Post-layout simulated waveforms of the proposed DNU hardened latch for a fault free case in the STMicroelectronics 65-nm CMOS technology at 0.4 V supply voltage.

Further, we discuss the cases affected by SNU and DNU due to TF. Case 1: An SNU in the proposed latch. In this case two possible scenarios exist. Case 1(a): an SNU is occurs inside the memory cell. In this scenario, nodes at the uncorrupted state restore back the original state on the affected node. Case 1(b): an SNU affect the 3-input MCE. In this scenario, the 3-input clocked MCE mitigate the transient fault. Case 2: we consider a pair of nodes affected by DNU due to soft error. In this case also two possible cases exist. Case 2(a): two intermediated nodes in the memory cell/ 3-input MCE are corrupted due to charge sharing-induced soft error. Case 2 (b): both, an SNU inside the 3- input MCE cell and an SNU inside the memory cell are corrupted. Analysis of these cases (i.e. case1 and case 2) is done when the proposed latch works in the holding/latching mode. Now we explain the reasons of radiation hardness.

Case 1(a): Suppose that D = 1, the nodes n1, n2 and n3 are held at logic 1 state in the hold mode (i.e. CLK = 0 and CLKB = 1) while nodes n4 and n5 are set at low logic state. In this case, say a discharging SEU occurs on the node n1 while the node holds the high logic state. For this case, the transistors Mp1 and Mn1 are kept ON due to the voltages of node n4 and n2, respectively. Therefore, the fault is not propagated to the output node Q and node n1 is restored to high logic state. Further, we consider a charging SEU on node n2 while it is set at a low logic state. The fault cannot be propagated on Q because in this case Mp2 and Mn2 transistors are ON due to the logic stored on node n1 and n4, respectively. As a result, correct logic 0 is restored on the node n2. Furthermore, we consider an SEU on node n4. Suppose high logic state is set on node n4 and due to SEU state of node n4 changes to logic 0. This corrupted state

can be recovered by transistor Mp3 because voltage level of node n1 turns on transistor Mp3. Consequently, state on node n4 restores back to its original state. Therefore, the output will not be corrupted by an SEU in case 1(a).

Case 1(b): Suppose that D = 1, node n3 is set to the high logic state in the hold mode while, node n5 is set at low logic state. In this case, an SEU occurred on the node n3 cannot be propagated to the output node Q, because voltages at node n1 and n2 turns OFF the transistor Mp6 and Mp5, respectively. Now, we consider an SNU at internal node n5, while the node holds logic 0. In this case, state of node n5 is restored back to its original state by the unaffected voltages at node n1, n2, and n3. Consequently, state on node n5 restores back to its original state. Therefore, the output will not be corrupted by an SEU in case 1(b). Figure 5.8 shows the post layout parasitic extracted waveforms of the proposed DNU hardened latch when the particle strikes on nodes n1, n2, n3, n4, and n5. Thus, the injected SEU cannot affect the output node Q of the proposed DNU hardened latch.

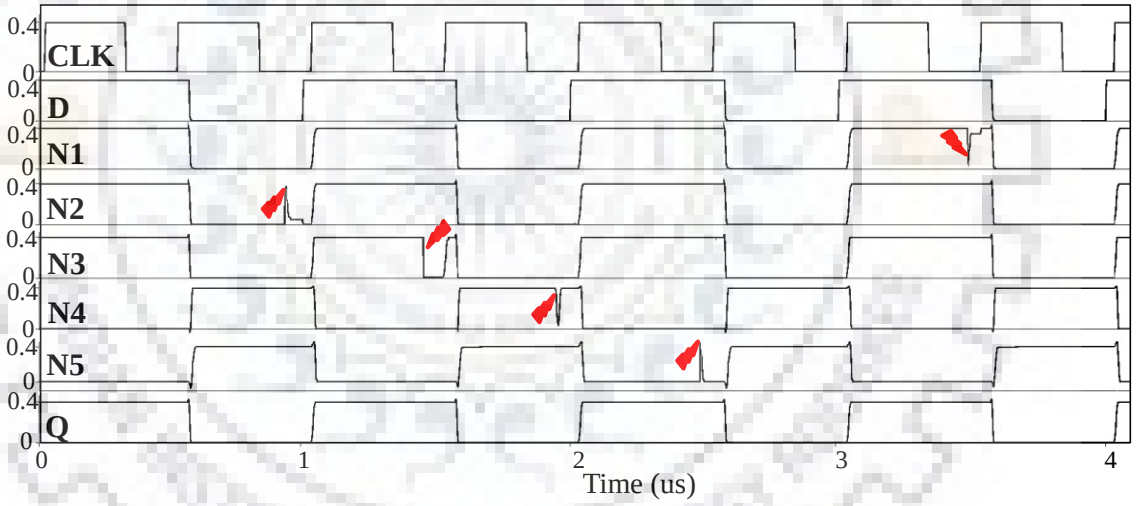


Figure 5.8 Post-layout simulated waveforms of proposed DNU hardened latch for SNU injection cases in STMicroelectronics 65-nm technology at 0.4V supply voltage

Case 2(a): when two nodes are affected inside the memory cell: If node n1 and n2 are affected (i.e. nodes n1and n2 are flipped to logic 0), Mp3, Mp5, and Mp6 are turned ON while Mn3, Mn4, and Mn5 are turned OFF. In this case logic state of node n5 is not affected, because transistors Mp4 and Mn6 are OFF and ON, respectively. In this case soft error cannot be propagated to the output node Q because 3-input clocked MCE blocked the transient fault. Moreover, we consider node n1 and n4 are affected (i.e. node n1 is flipped to logic 0 and node n4 is flipped to logic 1), in this case transistors Mp3, Mp6 and Mn9 are turned ON while, Mn4 and Mp7 are turned OFF. In this case also DNU is blocked by the 3-input clocked MCE because the logic state of node n5 is unaffected. Analysis is similar when the node pair n2 and

n4 is affected by an SEU. If n3 and n5 nodes are affected (i.e. n3 is flipped to logic 0 and n5 is flipped to logic 1), transistors Mp4 and Mn8 are turned ON while Mn6 and Mp8 are turned OFF. In this case fault is blocked is by the 3-input clocked MCE because the logic state of node n4 is unaffected. Therefore, the output of the latch will not be corrupted by DNU in case 2(a).

Case 2(b): Now we consider when radiation affects a node in the 3-input MCE cell and a node in the memory cell. If node n1 and n3 are affected by an SEU (i.e. both are discharge to 0), transistor Mp2, Mp3, Mp4 and Mp6 are turned ON while Mn4 and Mn6 are turns OFF. In this scenario node n1 is restored to high logic state by the uncorrupted node voltages of node n2 and n4. In this case soft error cannot be propagated to the node Q because 3-input MCE and 3-input clocked MCE blocked the fault. Analysis is similar when the node pair n2 and n3 is affected by an SEU. If n1 and n5 nodes are influenced due to DNU (i.e. n1 is flipped to logic 0 and n5 is flipped to logic 1), transistors Mp3, Mp6 and Mn8 are turned ON while, Mn4 and Mp8 are turned OFF. In this scenario node n1 self recovers its logic state by node voltages stored on n2 and n4 nodes. Consequently node n5 also recovers its original state through transistor Mn4. Therefore, the output will not be corrupted by DNU. Analysis is similar when the node pair n2 and n5 is affected by an SEU. If n3 and n4 nodes are affected (i.e. n3 is flipped to logic 0 and n4 is flipped to logic 1), transistors Mp4 and Mn9 are turned ON while Mn6 and Mp7 are turned OFF. In this scenario node n4 self recovers its logic state by node voltages stored on node n1 and n2. Consequently, the fault is blocked by the 3-input clocked MCE and the fault is not propagated to the output node Q. Furthermore, we consider a transient fault occurs on n4 and n5 nodes (i.e. both are discharged to 0). In this case n4 and n5 nodes are restored back to the original state due to the unaffected states of n1, n2 and n3. Therefore, the output will not be corrupted by DNU in case 2(b). Figure 5.9, shows the simulated waveforms for the proposed DNU hardened latch when particle strikes on node pairs inside the latch.

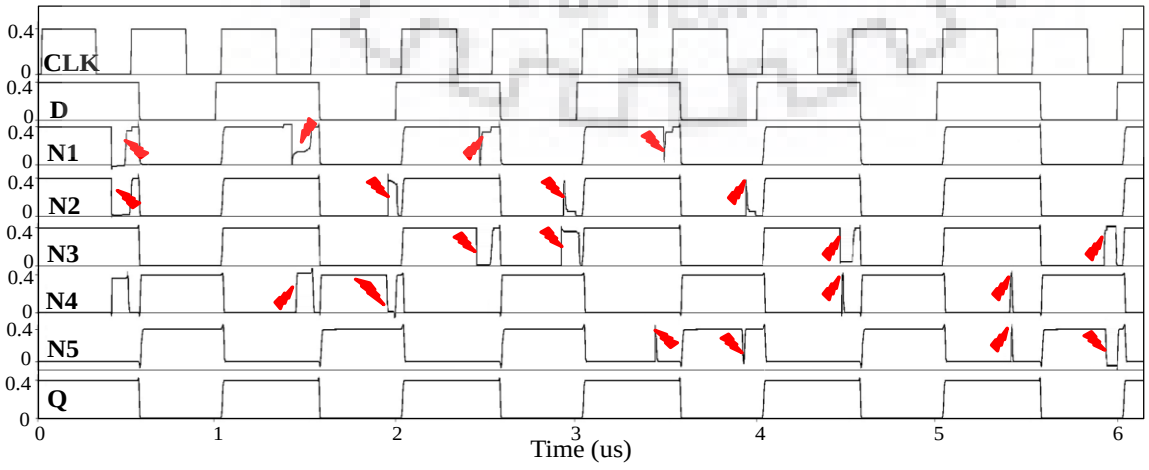


Figure 5.9 Post-layout simulated waveforms of the proposed DNU hardened latch for DNU injection cases in STMicroelectronics 65-nm technology at V_{DD} =0.4V.

5.2.3 Proposed Triple Node Upset Hardened Latch

The schematic and the layout of the proposed TNU tolerate latch are shown in Fig. 5.10 and Fig. 5.11, respectively. The proposed TNU hardened latch circuit consists of a set of five transmission gates, two restorer circuits (RCs), and a 3-input clocked MCE.

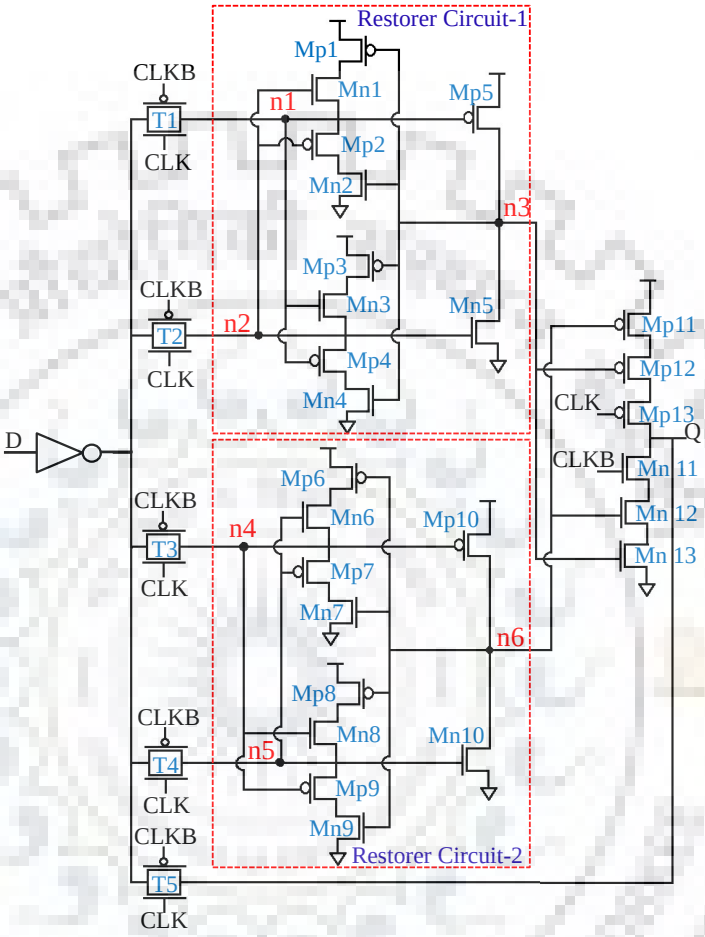


Figure 5.10 Schematic of the proposed TNU hardened latch

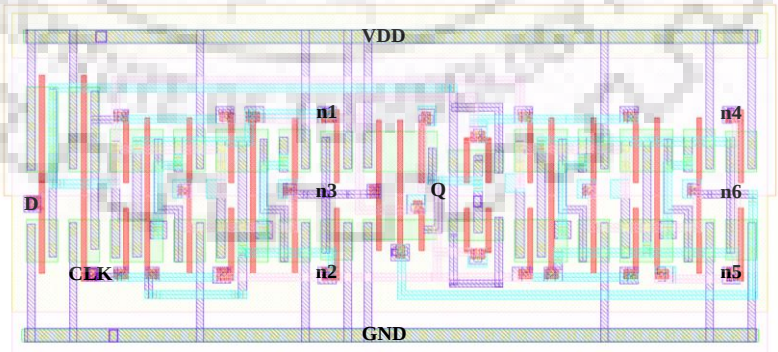


Figure 5.11 Layout of the proposed TNU hardened latch

When CLK = 1 and CLKB = 0, all the transmission gates, namely T1, T2, T3, T4, and T5 are turned ON and the latch operates in transparent mode. The data propagates from the input (D) to the output (Q) through the transmission gate T5. The input nodes of the restorer circuit are driven by D through transmission gates T1, T2, T3 and T4. In the transparent mode the value of

D stored at the intermediate nodes n3 and n6 and its inverse is stored on nodes n1, n2, n4 and n5. The output nodes of the restorer circuits n3 and n6, are electrically isolated from the latch output node Q by a 3-input clocked MCE. In transparent mode 3-input clocked MCE is turned OFF to reduce propagation delay and power dissipation. In the hold mode (i.e. CLK = 0 and CLKB = 1), all transmission gates T1, T2, T3, T4 and T5 are turned OFF. The 3-input clocked MCE turns ON, therefore, the output of the clocked MCE retains the latch state. Subsequently, the logic states at the nodes n3 and n6 feedback to nodes n1, n2, n4, and n5. This way, the feedback loops are constructed in the RC to robustly hold the latch state.

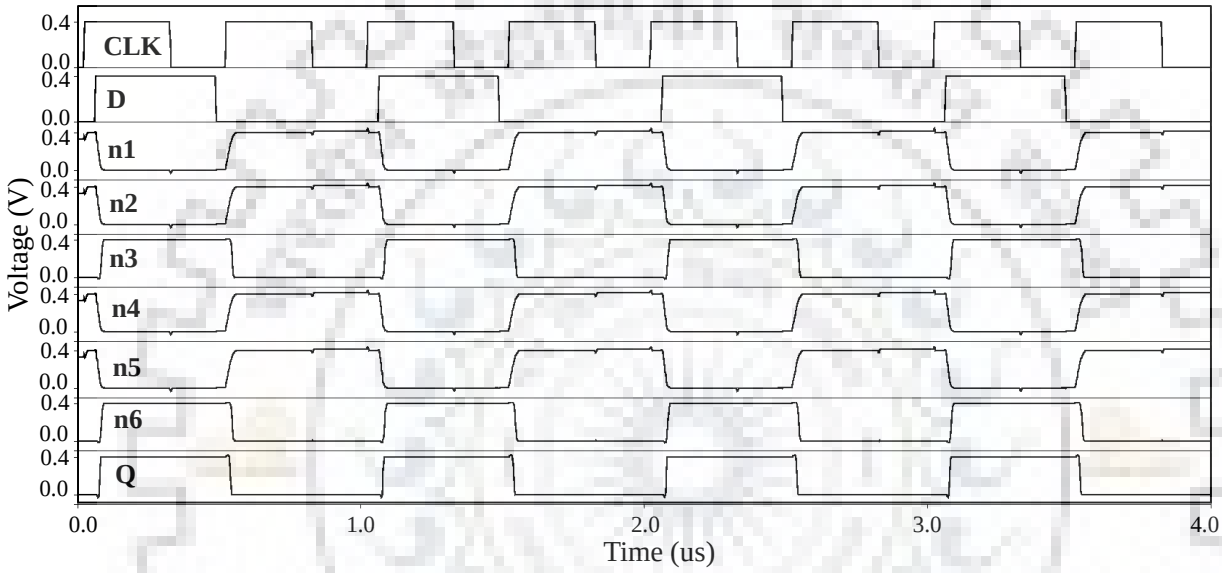


Figure 5.12 Post-layout simulated waveforms of proposed TNU hardened latch in fault free case in STMicroelectronics 65-nm technology at 0.4V supply voltage.

The basic principle of soft error hardening of the proposed TNU hardened latch is explained as follows: Consider the soft error case during the hold mode (i.e. CLK = 0 and CLKB = 1) in which a transient fault occur at one of the internal susceptible nodes (n1, n2, n3, n4, n5, n6) of the restorer circuits. This transient fault never switches the output signal of the latch because the state of the corrupted node can be recovered by the uncorrupted states on the other two nodes. In the presence of SNU/DNU/TNU, our latch retains the correct state on the output node (Q). The advantage of our technique is that it improves the performance and area of the latch also.

Now, we discuss the cases affected by SNU, DNU, and TNU due to transient fault of the proposed TNU hardened latch. We assume D = 0 for all fault-tolerance analysis and at that time nodes Q, n1, n2, n4, and n5 are at high logic state while nodes n3 and n6 are at low logic state in the hold mode (i.e. CLK is at logic 0).

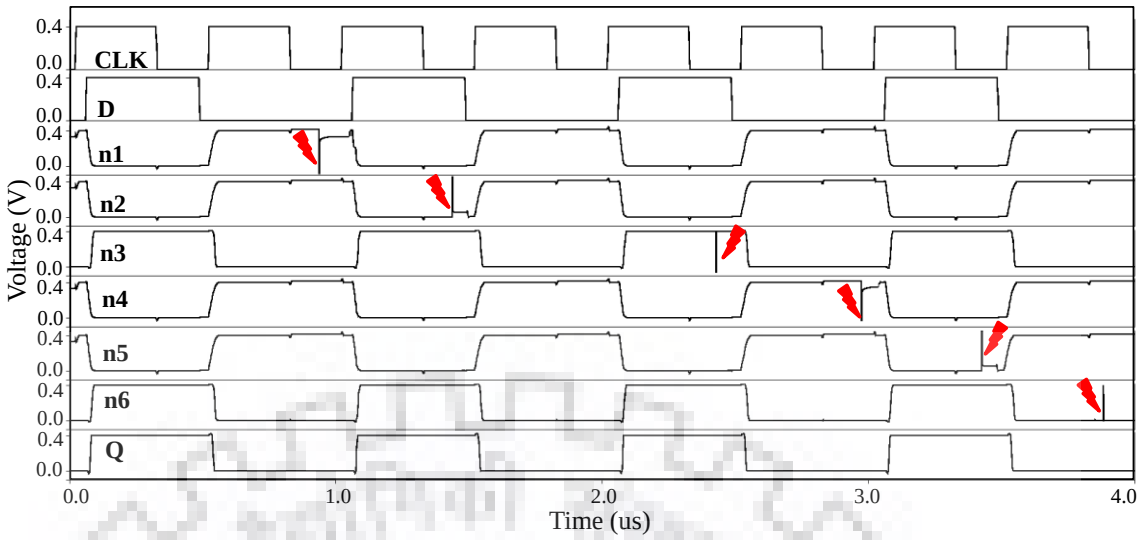


Figure 5.13 Post-layout simulated waveforms of proposed TNU hardened latch for SNU injection cases in STMicroelectronics 65-nm technology at 0.4V supply voltage

Case 1: Suppose, an SEU occurs on the node n1 while the node holds logic 1. This fault is not to be propagated to the output node. Node n1 is recovered to logic 1, because the transistors Mp1 and Mn1 are kept ON by the unaffected node voltages of n3 and n2, respectively. Therefore, the output will not be corrupted by an SEU. Now, we consider an SEU on node n2. The fault cannot be propagated to the output node Q because in this case Mp3 and Mn3 transistors are ON by logic stored on n3 and n1, respectively. As a result, logic state 1 is restored on node n2. Now, we consider an SEU occurs on node n3 and changes the state of the node to logic 1. This faulty state can be recovered by transistor Mn5 because the unaffected logic state on node n2 turns on the transistor Mn5. Consequently, the state on node n3 restores back to its original value. Analysis is similar when an SEU occurs on a single node in restorer circuit-2 (RC-2). Figure 5.13 shows the post layout parasitic extracted waveforms of the proposed TNU hardened latch when the particle strikes on nodes n1, n2, and n3 (n4, n5 and n6) inside the RC-1 (RC-2). Thus, the injected SEU cannot affect the output node Q of the proposed latch.

Case 2: Now, we consider two nodes are affected by DNU. In this scenario, there are total 15 node pairs and these node pairs are classified into two categories: (a) {n1, n2}, {n1, n3}, {n2, n3}, {n4, n5}, {n4, n6}, {n5, n6}; (b) {n1, n4}, {n2, n4}, {n1, n5}, {n2, n5}, {n1, n6}, {n2, n6}, {n4, n3}, {n5, n3}, {n3, n6}.

Case 2(a): If nodes n1 and n2 are affected (i.e. both are discharged from 1 to 0). In this scenario, transistors Mp5 and Mn5 will turn ON and OFF respectively. Consequently, the voltage level of node n3 will be charged to logic 1. However, the state of nodes n4, n5 and n6

will be at their initial states. Therefore, in this case soft error is blocked by the 3-input MCE because the logic state of node n6 is unaffected. The same analysis is done in node pairs {n1, n3} and {n2, n3}. If the nodes n4 and n5 are affected by DNU (i.e. both are discharged from logic 1 to logic 0), transistors Mp10 and Mn10 will turn ON and OFF, respectively. Consequently, the voltage level of node n6 will be charged to logic 1. However, the states of nodes n1, n2 and n3 would be maintained at their uncorrupted values. Therefore, in this case soft error is blocked is by the 3- input MCE because the data stored on node n3 is unaffected. The same analysis is done in node pairs {n4, n6} and {n5, n6}.

Case 2(b): When the intermediated nodes n1 and n4 are flipped from logic 1 to logic 0 due to DNU, transistors Mp4, Mp5, Mp9, and Mp10 are temporarily turned ON while Mn3 and Mn8 are temporarily turned OFF. However, the state of nodes n3 and n2 will be at their initial states (i.e. logic 0 and logic 1, respectively). Consequently, the transistors Mp1 and Mn1 will be always ON. Therefore, the state of node n1 will be recovered to its original state (i.e. logic 1). Similarly, node n4 is flipped to its initial state by the uncorrupted node voltages of nodes n5 and n6. Therefore, nodes n1 and n4 can restore back to their initial state from the DNU through node voltages of (n2, n3) and (n5, n6), respectively. The same analysis is done when a DNU occurs on the node pairs {n2, n4}, {n1, n5}, and {n2, n5}. Further, we consider if node pair {n1, n6} is affected (i.e. n1 is flipped from logic 1 to logic 0 while n6 is flipped from logic 0 to logic 1), transistors Mp4, Mp5, Mn7, and Mn9 are temporarily turned ON while Mn3, Mp6, and Mp8 are temporarily turned OFF. However, the state of nodes n4 and n5 will be at their initial states (i.e. both are held at logic 1). Consequently, the transistors Mp10 and Mn10 will always be OFF and ON respectively. Therefore, the state of node n6 will be recovered to its original state (i.e. logic 0). In this case node n1 also self recover to its logic state by the unaffected node voltages of node n3 and n2. Similar analysis is done when a DNU occurs on the node pairs {n2, n6}, {n4, n3}, and {n5, n3}. Therefore, the node pairs {n1, n6}, {n2, n6}, {n4, n3}, and {n5, n3} are able to self-recover from DNU. Furthermore, we consider we consider if a TF occur on node pair {n3, n6}. In this scenario, transistors Mn2, Mn4, Mn7, and Mn9 are temporarily turned ON while Mp1, Mp3, Mp6, and Mp8 are temporarily turned OFF. However, the state of nodes n1, n2, n4, and n5 will be at their initial state (i.e. logic 1). Consequently, the transistors Mn5 and Mn10 will be always ON. Therefore, the state of both nodes n3 and n6 will be recovered to their original state (i.e. logic 0). In this case also the proposed TNU hadrened latch is able to self-recover from DNU. Figure 5.14, shows the simulated waveforms for the proposed TNU hardened latch when particle strikes on node pairs inside the latch.

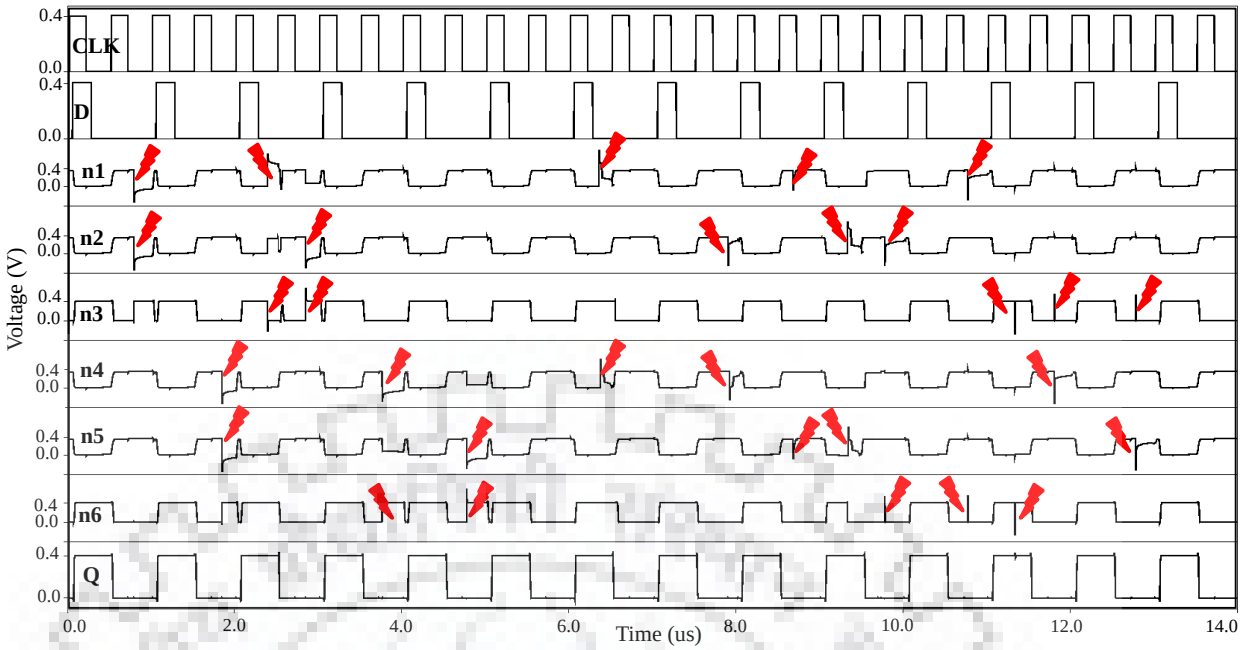


Figure 5.14 Post-layout simulated waveforms of the proposed TNU hardened latch for DNU cases in STMicroelectronics 65-nm technology at 0.4V supply voltage.

Case 3: Next we consider when triple nodes are affected by a TNU due to soft error. There are total 20 possible cases where triple nodes are affected and these are classified into three categories: (a) {n1, n2, n3}, {n4, n5, n6}; (b) {n1, n2, n4}, {n1, n2, n6}, {n1, n2, n5}, {n1, n3, n4}, {n1, n3, n6}, {n2, n3, n4}, {n2, n3, n5}, {n1, n3, n5}, {n2, n3, n6}; (c) {n1, n4, n5}, {n2, n4, n5}, {n3, n4, n5}, {n1, n4, n6}, {n2, n4, n6}, {n3, n4, n6}, {n2, n5, n6}, {n1, n5, n6}, {n3, n5, n6}.

Case 3(a): If nodes n1, n2 and n3 are affected (i.e. n1 and n2 are discharged to 0 while n3 is charged to 1). In this case logic state of nodes n4, n5 and n6 are not affected. Therefore, in this scenario soft error is blocked by the 3-input MCE. Consequently, output node (Q) will remains at high logic state. Similar explanation is applicable when a TF occurs at a same time on nodes n4, n5 and n6.

Case 3(b): Now, we consider the case when nodes n1, n2, and n4 are affected (i.e. all affected nodes are flipped to logic 0). In this case, transistor Mn5 turns ON. Consequently, the voltage level of node n3 will be charged to logic 1. Therefore, nodes n1 and n2 are not capable to recover their initial states. However, the state of nodes n6 and n5 will be at their initial state (i.e. logic 0 and logic 1, respectively). Consequently, the transistors Mp6 and Mn6 will be always ON. In this case node n4 will be recovered to its original state (i.e. logic 1). Therefore, soft error is blocked by the 3-input MCE and Q remains at high logic state. The same analysis is done for {n1, n3, n4}, {n1, n2, n5}, {n1, n3, n5}, {n2, n3, n4}, and {n2, n3, n5} TNU combinations. Further, we consider if nodes n1, n2 and n6 are flipped due to TNU (i.e. n1 and

n2 are discharged to 0 while n6 is charged to 1). In this case also nodes n1 and n2 are unable to self recover as explained above. However, the state of node n6 is recovered by the unaffected node voltages of nodes n4 and n5. In this case also TNU is blocked by the 3-input MCE because the logic state of node n6 is restored. The same analysis is done for {n1, n3, n6} and {n2, n3, n6} TNU combinations.

Case 3(c): Now, we consider the case when SNU occurs simultaneously at nodes n1, n4, and n5 (i.e. all affected nodes are flipped to logic 0). This is same as the case 3(b) discussed above. In this case, nodes n4 and n5 are not capable to recover its original state. However, node n1 will be recovered to its original state (i.e. logic 1). Therefore, soft error is blocked by the 3-input MCE and Q remains at high logic state. The same reason hold for other TNU combinations that fall under case 3.

From the above discussion, the following conclusions can be drawn.

- All the proposed radiation hardened latches are able to self-restore from any SNU, demonstrating that the memory cell/ restorer circuit are completely self-restorable with any flipping, even if any state (0 or 1) is stored
- The proposed DNU and TNU hardened latches can provide complete hardness against DNU though the memory element/ restorer circuits and Muller C-element.
- The proposed TNU hardened latch can completely tolerate any TNU though the restorer circuits and block the fault though Muller C-element.

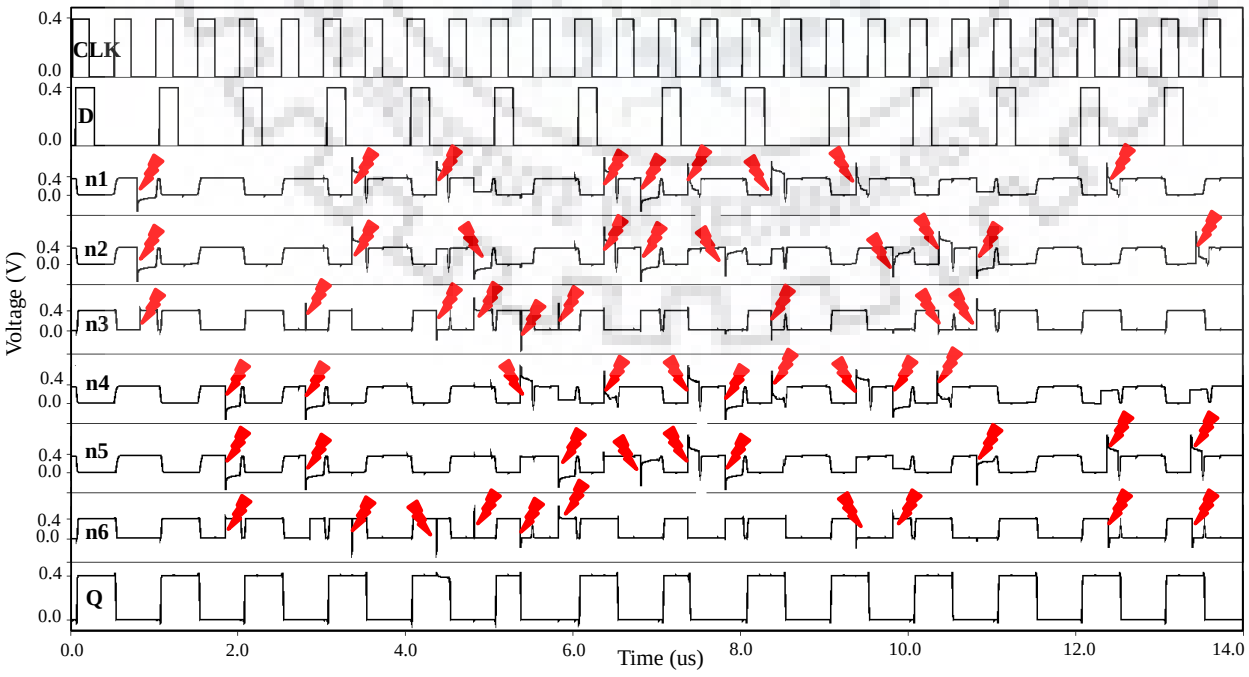


Figure 5.15 Post-layout simulated waveforms of the proposed TNU hardened latch for TNU injection cases in STMicroelectronics 65-nm technology at 0.4V supply voltage

Now we discuss a layout method to improve the timing performance of our radiation hardened latch designs. In our techniques we employ inverse narrow width effect (INWE) in T3 (proposed SNU hardened latch)/ T4 (proposed DNU hardened latch)/ T5 (proposed TNU hardened latch) to improve the performance. By using INWE (minimum allowed finger width in T4) in the proposed latch D-Q delay reduces by 12.19% when compared with the case where fingered layout is not used for T4 (at V_{DD} = 0.4 in STMicroelectronics 65nm technology).

5.3 Simulation Results

5.3.1 Simulation Setup

Cadence Virtuoso, HSPICE and Synopsys Sentaurus TCAD are used for circuit performance analysis and validation. We have used Cadence Virtuoso for layout and parasitic extraction. Subsequently, HSPICE simulator is used for circuit simulation on the extracted net-list. In cadence and HSPICE simulations, we have used physical design kit (PDK) of STMicroelectronics 65-nm CMOS technology. For Sentaurus TCAD 2-D mixed mode simulations, we used calibrated [145] 32-nm CMOS technology. We verified all the proposed radiation hardened latches in the NTV regime. In this chapter, we verify the proposed latches at power supply (V_{DD}) near to the threshold voltage (V_{TH}) of transistors (PMOS/NMOS) i.e. NTV regime. The V_{TH} of NMOS and PMOS transistors are 0.41 V and 0.5 V in STMicroelectronics 65nm CMOS technology, respectively. However, the V_{TH} of NMOS and PMOS transistors are 0.25 V and 0.31 V for 32-nm CMOS technology, respectively.

5.3.2 Performance, Power and Area Comparison

A high soft error tolerance is realized in radiation hardened latches by using redundancy at the expense of area, power and performance. Therefore, in this section we compare the cost of the proposed latches to reported SNU, DNU and TNU tolerant latches [91]-[114].

The results of this comparison in the STMicroelectronics 65nm technology are shown Table 5.1. Table 5.1 shows that the proposed radiation hardened latches has lower power dissipation than the reported latches in [91]-[114]. The D-Q delay is the average of the time difference between from 50% of input (D) voltage to 50% of output (Q) voltage for input rise and fall transitions. Table 5.1 shows that the proposed radiation hardened latches takes less D-Q delay as compared to TMR, FERST, DICE, HPST, DICE-FBT, RFEL, Latch [103], CLCT, DNCS, DNURL, DIRT, LSEDUT, TNUHL, and LCTNUT latches. We explain these results as follows: When the proposed latch is transparent, the data is passes through faster and narrow

transmission gate T3 (proposed SNU hardened latch)/T4 (proposed DNU hardened latch)/ T5 (proposed TNU hardened latch) due to INWE, while the other radiation hardened latches the input data passes through multiple MCEs, which increases the propagation delay. Due to the same reason, Table 5.1 indicates that our latch has a minimum clock to output (C-Q) delay than the TMR, FERST, DICE, HPST, DICE-FBT, RFEL, Latch [103], CLCT, DNCS, DNURL, DIRT, LSEDUT, TNUHL, and LCTNUT latches. Table 5.1 shows that the area of the proposed TNU hardened latch is 39.39%, 4.12%, 36.54%, and 20.54% less as compared to DNURL, LSEDUT, TNUHL, and LCTNUT, respectively. DICE, FERST, CLCT and DNCS latches have less area as compared to the proposed TNU hardened latch; however, DICE, FERST, CLCT and DNCS cannot handle TNU.

Table 5.1 Cost comparison of post layout parasitic extracted performance of SNU, DNU and TNU hardened latches in STMicroelectronics 65-nm CMOS technology

Latch	SNU Tolerant	DNU Tolerant	TNU Tolerant	D-Q Delay (ns)	C-Q Delay (ns)	Avg. Power (nW)	Area (μM^2)
TMR	√	×	×	29.55	129.55	11.22	43.16
FERST	√	×	×	26.21	126.21	8.66	33.20
DICE	√	×	×	21.12	116.17	7.99	30.45
HPST	√	×	×	21.32	121.31	9.79	39.38
DICE-FBT	√	×	×	24.83	124.84	9.58	34.68
RFEL	√	×	×	24.94	124.94	10.47	38.47
Latch [103]	√	×	×	20.99	120.99	16.37	46.23
CLCT	√	√	×	23.65	123.65	8.37	42.01
DNCS	√	√	×	28.55	128.55	10.86	42.81
DNURL	√	√	×	23.98	123.98	15.64	70.90
DIRT	√	√	×	19.63	119.63	20.47	70.14
LSEDUT	√	√	×	22.59	122.59	9.65	44.82
TNUHL	√	√	√	28.11	128.11	28.04	67.72
LCTNUT	√	√	√	21.85	121.85	9.47	54.08
Proposed SNU	√	×	×	18.95	118.95	6.17	29.75
Proposed DNU	√	√	×	15.04	115.04	8.13	41.51
Proposed TNU	√	√	√	18.54	118.54	7.69	42.97

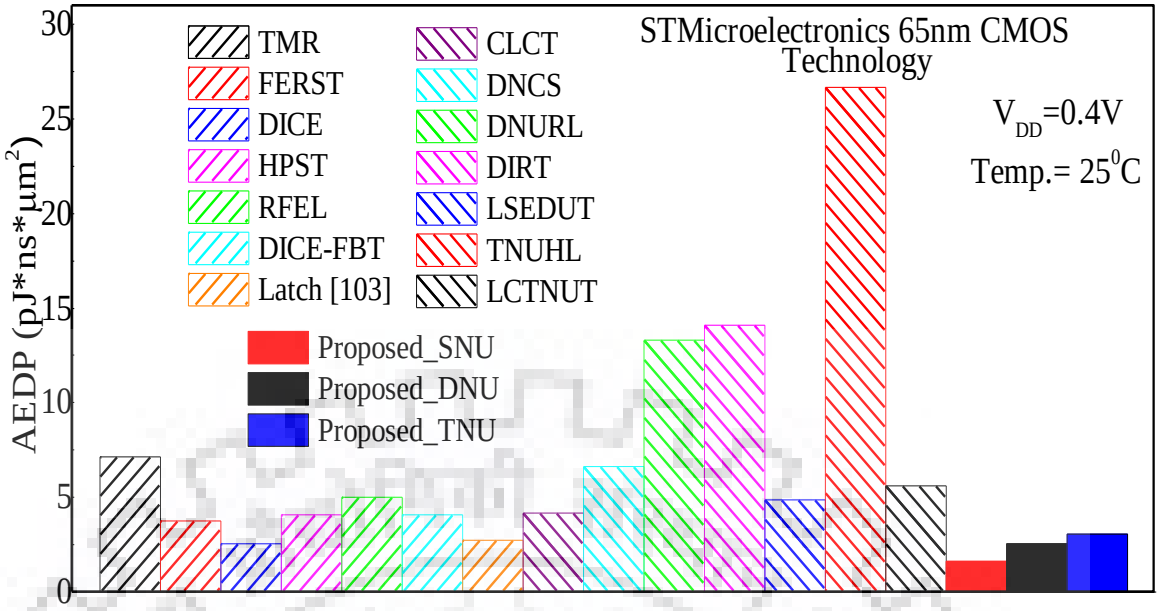


Figure 5.16 Comparison of area-energy-delay-product of the proposed radiation hardened latches with reported SNU/ DNU/ TNU hardened latches in STMicroelectronics 65-nm CMOS technology at V_{DD} = 0.4V

The comparison of area-energy-delay-product (AEDP) of the proposed SNU, DNU, and TNU hardened latches with existing radiation hardened latches [91] - [114] at 0.4V supply voltage in STMicroelectronics 65-nm CMOS technology is shown in Figure 5.16. In AEDP calculations D-Q propagation delay is taken. Figure 5.16 shows that the proposed SNU/DNU/TNU hardened latch have minimum AEDP among SNU/DNU/TNU hardened latches. Figure 5.16 shows that the AEDP of the proposed TNU hardened latch is 88% and 42% less as compared to the recently reported TNUHL [112] and LCTNUT [114] latches.

5.3.3 Variability Analysis

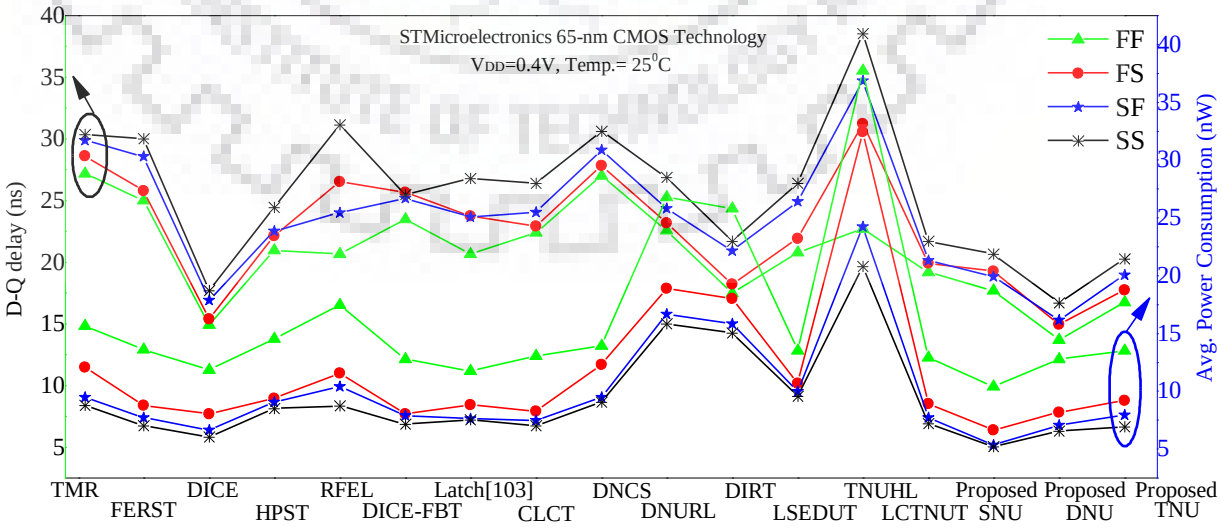


Figure 5.17 Comparison of D-Q delay and average power consumption at different process corners of various latches for STMicroelectronics 65-nm CMOS technology at V_{DD} = 0.4V.

A circuit design must be validated in extreme cases of performance variation due to changes in process parameters. These extreme cases of performance variations are represented by "process corners". Fast Fast (FF), Slow Slow (SS), Fast Slow (FS), and Slow Fast (SF) are these extreme case process corners for MOSFETs (NMOS/PMOS). The comparison of average power consumption and D-Q delay of the radiation hardened latches with reported radiation hardened latches [91]-[114] at FF, FS, SF, and SS is shown in Fig. 5.17 at V_{DD} = 0.4V. From simulations, it is observed that at all process corners the proposed latches shows less D-Q delay and power consumption as compared to the existing radiation hardened latches [91]-[114].

Table 5.2 Standard Deviation (σ) for D-Q delay and Avg. Power dissipation of radiation hardened latches

Latches	D-Q delay (ns)	Avg. Power (nW)
TMR	1.47	0.87
FERST	2.13	0.53
DICE	1.33	0.39
HPST	0.67	0.66
DICE-FBT	1.21	0.41
RFEL	2.62	0.68
Latch [103]	1.87	0.71
CLCT	1.25	0.41
DNCS	1.46	1.09
DNURL	0.97	1.08
DIRT	1.14	1.01
LSEDUT	1.18	0.48
TNUHL	4.05	2.08
LCTNUT	0.95	0.64
Proposed SNU	0.51	0.47
Proposed DNU	0.52	0.58
Proposed TNU	0.80	0.48

To verify the variability of the proposed radiation hardened latches in NTV regime we have done Monte-Carlo (MC) simulations. We have performed 10,000 MC simulations to evaluate performance of the proposed latch under PVT variations. In each of these MC simulations, a

20% variation in V_{DD} and 3σ V_{TH} variation is used at 25°C temperature. From Table 5.2, we can validate that the proposed latches have less sensitivity to the PVT variation for power and D-Q delay as compared to existing radiation hardened latches. The proposed TNU hardened latche shows less Standard deviation (σ) in D-Q delay because of high speed transmission gate (due to INWE) and minimum power consumption (due to less number of transistors) as compared to the existing TNU hardened latches in [112] and [114].

5.4 Soft Error Robustness Simulations using TCAD Tool

For Synopsys Sentaurus technology computer-aided design (TCAD) mixed mode simulations, we used calibrated simulation setup as discussed in our group's earlier work [145]. Figure 4.12 compares the current voltage (I-V) characteristics of MOSFETs (NMOS and PMOS) simulated using our calibrated simulation setup to the experimental results [153]. The Sentaurus TCAD mixed mode simulations are performed using the velocity saturation, process induced mechanical stress, generation-recombination, high field mobility degradation, quantum effects and heavy ion models.

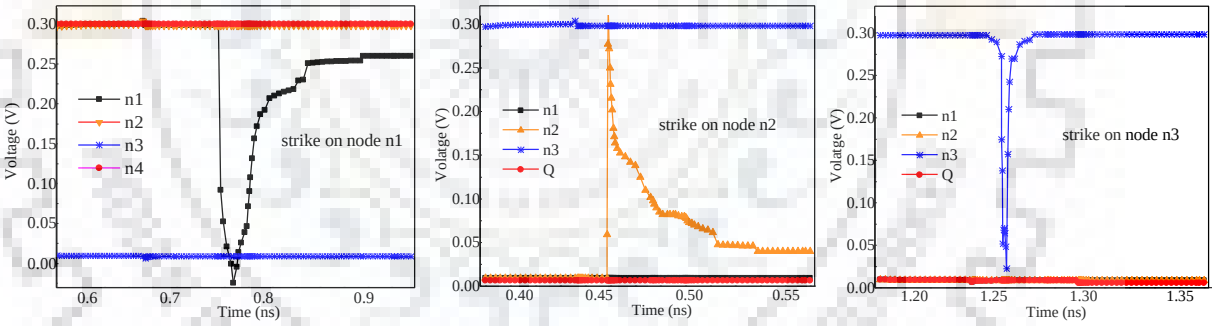
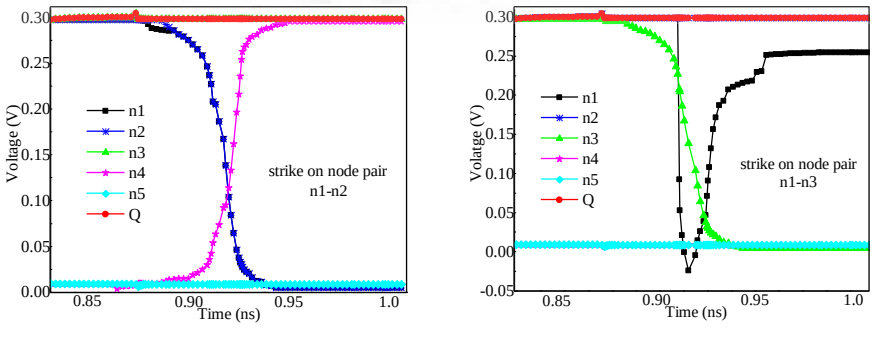
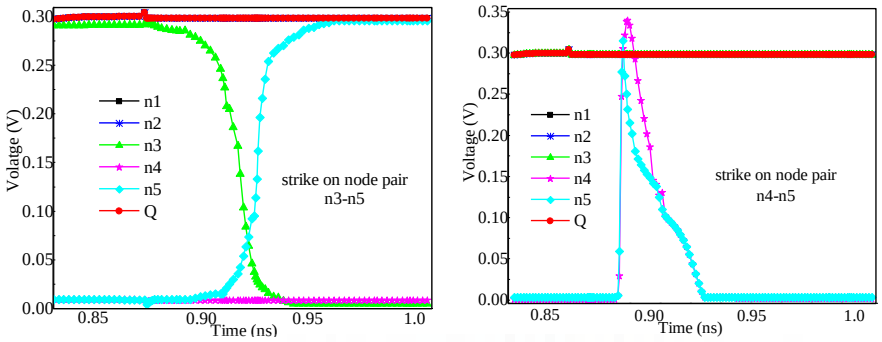


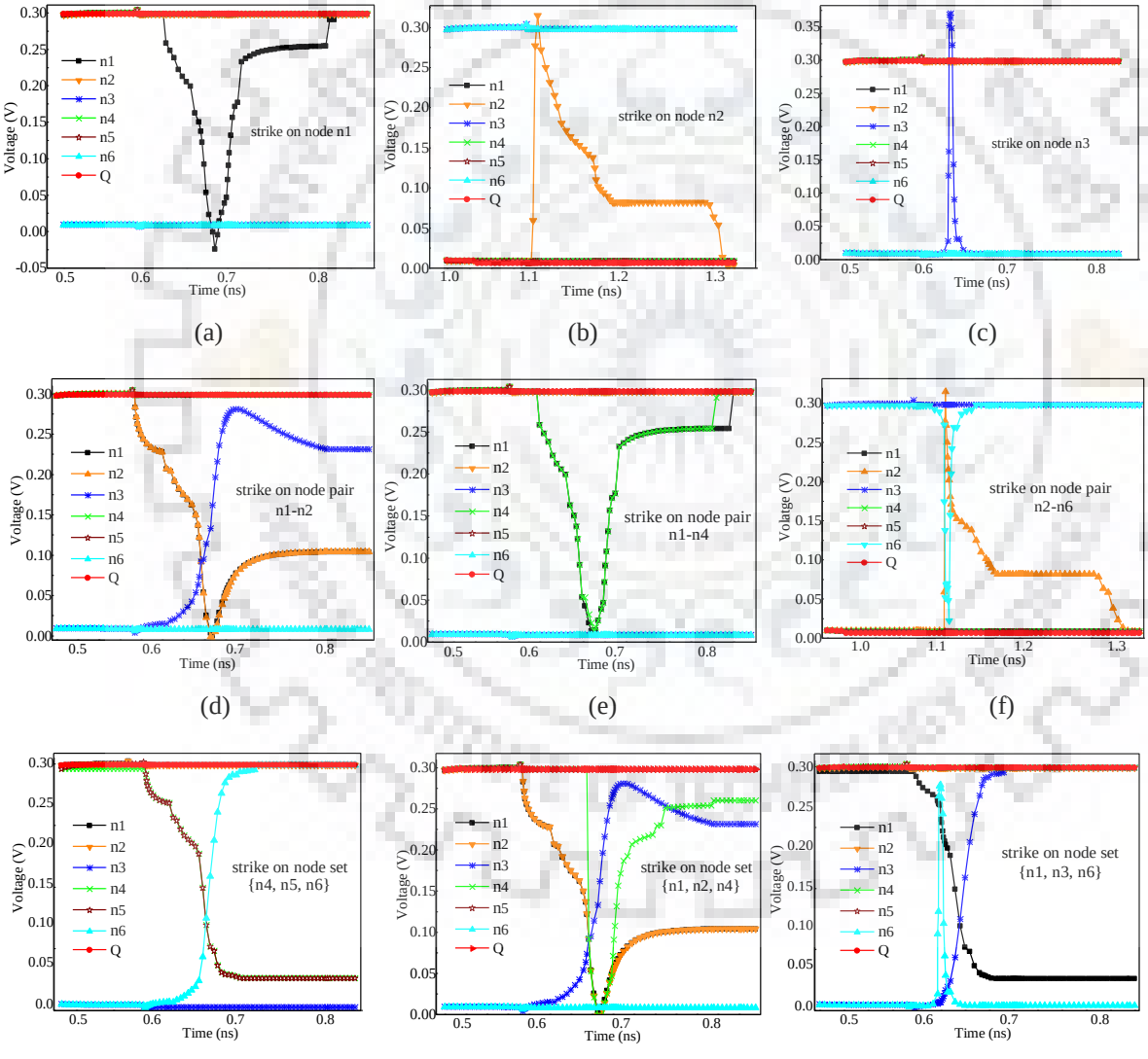
Figure 5.18 Node voltages v/s time for TCAD mixed mode simulation using 32-nm CMOS technology with LET = 170 MeV-cm2/mg strike on (a) node n1, (b) node n2, and (c) node n3 of the proposed SNU hardened latch.





(c) (d)

Figure 5.19 Node voltages v/s time for TCAD mixed mode simulation using 32-nm CMOS technology with LET = 170 MeV-cm2/mg strike at node pairs (a) n1-n2 , (b) n1-n3, (c) n3-n5, and (d) n4-n5 of the proposed DNU hardened latch.



(a) (b) (c)

(d) (e) (f)

(g) (h) (i)

Figure 5.20 Node voltages v/s time for TCAD mixed mode simulation using 32-nm CMOS technology with LET = 170 MeV-cm2/mg strike on (a) node n1, (b) node n2, (c) node n3, (d) node pair n1-n2, (e) node pair n1-n4, (f) node pair n2-n6, (g) node set {n4, n5, n6}, (h) node set {n1, n2, n4}, and (i) node set {n1, n3, n6} of the proposed TNU hardened latch.

Figure 5.18, Figure 5.19, and Figure 5.20 shows Sentaurus TCAD 2-D mixed-mode simulation results for the proposed radiation hardened latches, respectively. From Figure 5.18, Figure 5.19, and Figure 5.20, we can see that the proposed radiation hardened latches can effectively mitigate the impact of heavy ion strike with a linear energy transfer (LET) of 170 MeV-cm2/mg at normal (90^0) strike. Figure 5.18(a), Fig. 5.18(b), and Fig. 5.18(c) show the SNU cases by heavy ion strike at nodes n1, n2, and n3, respectively of the proposed SNU hardened latch. Figure 5.19(a), Fig. 5.19(b), Fig. 5.19(c) and Fig. 5.19(d) show the DNU cases due to heavy ion strikes at node pair {n1-n2}, {n1-n3}, {n3-n5} and {n4-n5}, respectively of the proposed DNU hardened latch . Figure 5.20 shows the heavy ion strikes on the proposed TNU hardened latch strikes. The Heavy-ion models are used in the Sentaurus TCAD mixed mode simulations. The radius and the length of the ion track are kept at 5nm and 10um, respectively, for all of our TCAD simulations. In our TCAD mixed mode simulations, the heavy-ion strikes at the center of the drain of the affected transistor.

From Fig. 5.18, Fig. 5.19, and Fig. 5.20, we validated that the proposed radiation tolerant latches effectively mitigates the heavy ion strike on single node, double node and also triple node. It means that the proposed TNU tolerant latch can hold its original data after a heavy ion strike at LET = 170 MeV-cm2/mg.

5.5 Summary

In this chapter, three novel highly reliable energy efficient radiation hardened latches in the near-threshold voltage regime is presented. The proposed latches provide the soft error tolerance by using memory element/ restorer circuits (RC) to hold the correct state and Muller-C element. The memory element/ RC are based on pull-up and pull-down paths, controlled by different susceptible nodes, results in better radiation hardness. Furthermore, we use inverse narrow width effect at the layout level of the proposed latches to improve the D-Q and C-Q propagation delay. The proposed latches effectively, maintain its soft error tolerance in the presence of process voltage temperature (PVT) variations. Using post-layout simulations, we have shown that the proposed TNU hardened latch improves the performance in terms of D-Q delay (CLK-Q delay) up-to ~ 34% (7%), and 15% (3%) over recently reported TNU hardened latches TNUHL, and LCTNUT, respectively at V_{DD} = 0.4V in an STMicroelectronics 65-nm technology. We also observed that the area-energy-delay-product (AEDP) of the proposed TNU hardened latch is 89% and 42% smaller than that of the TNUHL and LCTNUT latches respectively. Moreover, we also validated the proposed radiation hardened latches in Sentaurus

TCAD using 32-nm calibrated CMOS technology. From TCAD mixed mode simulation we have validated that our latches can provide soft error tolerance up to the value of linear energy transfer (LET) equals to 170 Mev-cm2/mg in 32-nm CMOS technology. Therefore, for NTV and space applications the proposed radiation hardened latches would be a better choice.

6 CHAPTER

Energy Efficient Radiation-Induced Soft Error Tolerant SRAM cell Designs

6.1 Overview

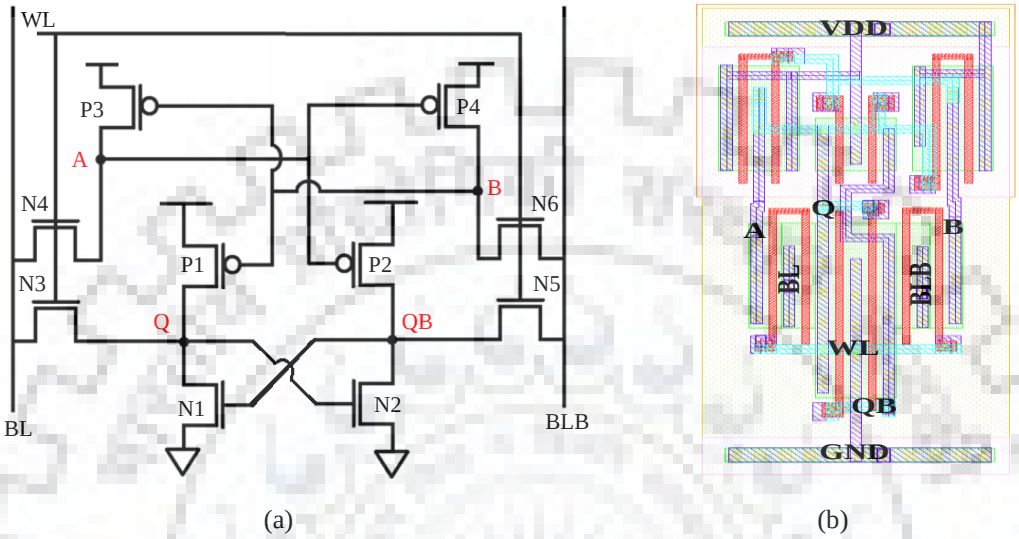
In the previous chapters, we have proposed a critical charge model and resilient radiation hardened design techniques for latches in the near-threshold voltage (NTV) regime. Fundamentally, squentail/storage circuits elements are more or less similar. In particular all versions of static latch and static random access memory (SRAM) cells have a similar core of back to back connected inverter pair. Hence, the issues faced by static latches are similar to those of SRAM cells. Therefore, soft errors also a serious issues in SRAM cells [12]. A conventional 6T SRAM cell is very sensitive to single-event multiple-node upsets (SEMNU) because of high energy particle strikes. During the hold mode, a single event upset (SEU) may upset the stored data of the SRAM cell which would be corrected when a new data is written on the SRAM cell. SEMNU occurs when a high energy particle strikes on a chip and affects multiple susceptible intermediate nodes and causes an upset even in an SEU tolerant SRAM cell. The CMOS SRAM cells are becoming more susceptible to an SEU/SEMNU related reliability challenge because of reducing supply voltage, increasing densities, and decreasing critical charges [3]. To solve these problems first we have proposed an energy efficient single node upset (SNU) tolerant 10T SRAM cell. The proposed 10T SRAM cell consists of six NMOS transistors and four PMOS transistors to enhance SNU tolerance to achieve more robustness compared to the recently reported SRAM cells [124]-[126]. Further we have proposed an energy efficient SEMNU tolerant 12T SRAM cell that is based on our SNU tolerant 10T SRAM cell. The proposed SEMNU tolerant 12T SRAM cell improves the read/ writes noise static margins (RSNM/WSNM), and read/ write access time (RAT/WAT) as compared to the recently reported radiation hardened SRAM cells [124]-[126].

The chapter is organized as follows: Section 6.2 presents the working principle, implementation, and soft error robustness of the proposed 10T and 12T SRAM cells. The experimental and comparison results in STMicroelectronics 65-nm CMOS technology is presented in section 6.3. In section 6.4, we validate the soft error robustness of the proposed

SRAM cells in 32-nm CMOS technology using Sentaurus TCAD mixed mode simulations. Section 6.5 concludes the chapter.

6.2 Proposed SRAM cell Designs

6.2.1 Proposed Single Node Upset Tolerant 10T SRAM cell



(a) (b)

Figure 6.1 (a) The schematic and (b) the layout of the proposed high performance, low area and SEU tolerant 10T SRAM cell

The schematic and the layout of the proposed SEU hardened 10T SRAM cell is shown in Fig. 6.1(a) and Fig. 6.1(b) respectively. The proposed 10T SRAM cell consists of four PMOS transistors (P1-P4) and six NMOS transistors (N1-N6). The access transistors, N3 and N5, are connected to the bit lines (BL and BLB) to the storage nodes Q and QB respectively. Transistor N3, N4, N5, and N6 are controlled by word line (WL). Therefore, when WL cell is in ON mode (WL = 1), these NMOS transistors (N3-N6) are turned ON and read/ write operations can be done. The intermediated nodes Q, QB, A, and B are responsible to maintain the stored data correctly in the proposed memory cell.

In the hold mode, i.e., WL = 0 (namely GND), assuming Q = 1 and QB = 0, transistors P1, P3 and N2, are turned ON, while the rest transistors are turned OFF, from which it is concluded that the proposed 10T SRAM cell maintain its state correctly. In the read operation of the proposed 10T SRAM cell, bit lines BL and BLB are pre-charged to V_{DD} (logic 1), thereafter, as the WL signal is changed from 0 to 1, and then the access transistors N3 and N5 are turned ON immediately. The stored value on node Q and BL maintain its initial value 1, while the BLB is discharged to 0 through transistors N2 and N5. Read operation is completed when the difference between bit lines BL and BLB is identified by a sense amplifier, and the stored value

of the proposed 10T SRAM cell is output. For write operation, the bit lines BL and BLB are pre-charged to 0 and 1 respectively and initially assumed that output nodes Q and QB are at 1 and 0 sate, respectively. When the WL signal is activated, the state stored on the bit lines BL and BLB will charge node QB to 1 and discharge node Q to 0, respectively. Figure 6.2 shows the waveforms for read and write operations in a fault free scenario. Therefore, these simulated waveforms validate the capability of achieving proper operation (write and read) by the proposed RHBD-10T SRAM cell.

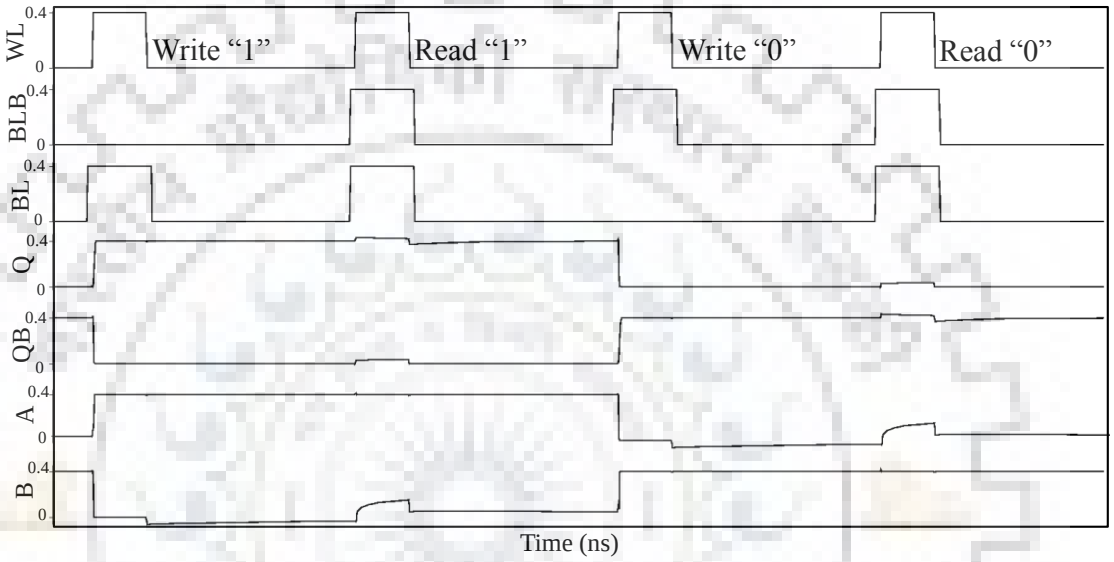


Figure 6.2 Post-layout simulated waveforms for proposed 10T SRAM cell for fault free case in STMicroelectronics 65-nm technology at V_{DD}=0.4 V

The basic principle of SEU hardening of the proposed 10T SRAM cell is as follows: Consider the transient fault (TF) case (when WL = 0) in which a SEU occur at one of the sensitive nodes (Q, QB, A, or B) of the RHBD-10T SRAM cell shown in Fig. 6.1(a). All the four nodes are driven by a PMOS and an NMOS transistor and gate of these transistors are connected to the two different nodes. Consequently, if a soft error/TF pulls up (down) the node voltage level of Q and QB, it can be restored by the 'ON' transistors (NMOS/PMOS) connected to the affected node and driven by an unaffected node. If the voltage level of nodes A and B is pulled down, it would be restored by the unaffected PMOS transistors P3 and P4 respectively. If the voltage level of either of the nodes A and B is pulled up, transistors P2 and P1 would be OFF and the voltage level of Q and QB would remain unaffected. Therefore, in the event of an SEU, our 10T SRAM cell automatically corrects the error. Our technique also improves the performance of the memory cell.

Now, we discuss the SEU recovery mechanism for the proposed 10T SRAM cell. We assume QB = 0, Q = 1, A = 1, B = 0 for the analysis.

1) If the output node ‘Q’ is discharge to 0 by an SEU, transistor N2 will be temporarily OFF. However, the voltage of node B will be in its initial state (logic 0). Consequently, the transistor P1 will be always ON. Finally, the voltage of node Q will be flipped to the initial voltage (logic 1).

2) When the sensitive node QB is flipped due to an SEU, transistor N1 will be temporarily be ON and then the voltage of node Q will be discharged to 0. Hence, transistor N2 will be temporarily turned OFF. Transistor P1 remains in ON state because the node B still holds its initial voltage level (logiv 0). Therefore, the node Q will be pulled up to logic level 1 and then transistor N2 will be turned ON again, and node QB will be pulled down to logic level 0. Consequently, the intermediate node will not be corrupted by SEU.

3) Further, we consider a transient fault at node A while it holds logic 1. The fault can not affect the node QB because in this case transistor N2 remains in ON state due to the initial state stored on node Q. Also, the transistor P3 is in ON state due to the initial state stored on node B. As a result, the correct logic 1 is restored at the affected node A.

4) Finally, we consider a transient fault which occurs at node B which changes the state of the node to logic 1. The fault cannot be affecting the output node Q because in this case transistor N1 remains in OFF state by logic stored on node QB. Therefore, the output nodes (Q and QB) will not be corrupted by transient fault due to SEU. Figure 6.3 shows the post layout parasitic extracted waveforms of the proposed 10T radiation hardened SRAM cell when the particle strikes on nodes Q, QB, A, and B.

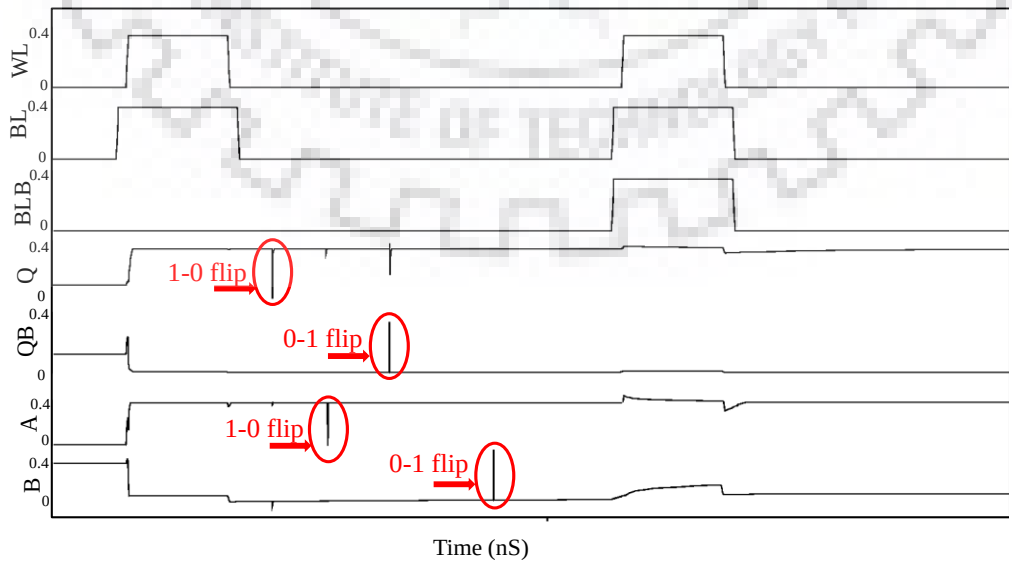
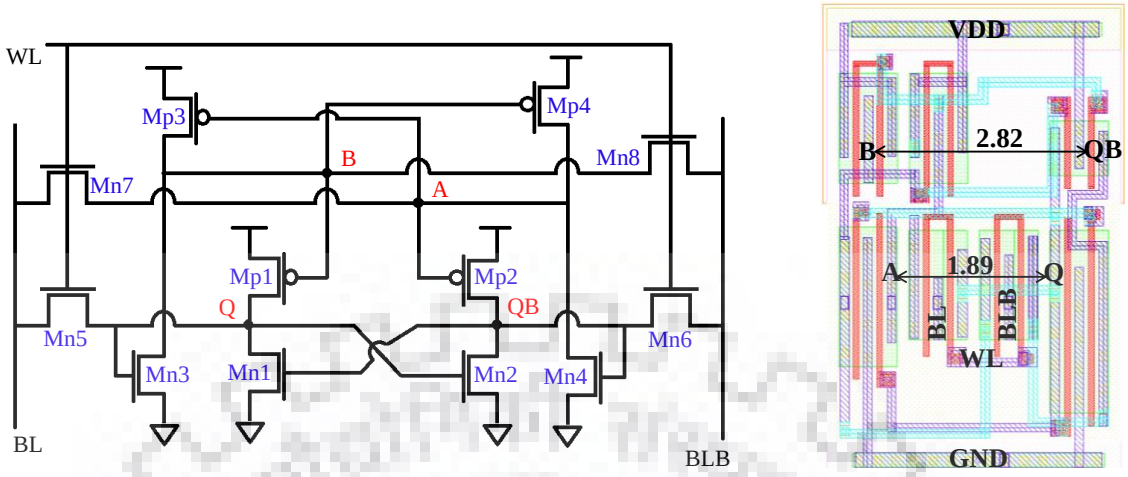


Figure 6.3 Simulated waveforms for proposed 10T SRAM when a particle strikes on nodes Q, QB, A, and B for a STMicroelectronics 65-nm technology at 0.4 V supply voltage.

6.2.2 Proposed Single Event Multiple Node Upset Hardened 12T SRAM cell



(a) (b)

Figure 6.4 (a) The schematic and (b) the layout of the proposed high performance, low area and SEMNU tolerant 12T SRAM cell

The schematic and the layout of the proposed SEMNU hardened 12T SRAM cell is shown in Fig. 6.4(a) and Fig. 6.4(b), respectively. The memory cell consists of eight NMOS transistors (Mn1-Mn8) and four PMOS transistors (Mp1-Mp4). The access transistors, Mn5 and Mn6, are connected to the bit lines (BL and BLB) and to the storage nodes Q and QB respectively. Transistors Mn5, Mn6, Mn7, and Mn8 are controlled by WL. Therefore, when WL cell is in ON mode (WL = 1), these transistors (Mn5-Mn8) are turned ON, and read/write operations can be done. The intermediate nodes Q, QB, A, and B are responsible to maintain the stored data correctly in the proposed memory cell. In the hold mode, i.e., WL = 0, assuming Q = 1, QB = 0, A = 1, and B = 0 transistors Mp1, Mp4, Mn2, and Mn3 are turned ON, while the rest transistors are turned OFF. So, it can be concluded that the proposed 12T memory cell maintain its state correctly. In the read operation of the proposed 12T memory cell, bit lines BL and BLB are pre-charged to V_{DD} (logic 1), thereafter, as the WL signal is changed from 0 to 1, and then the access transistors Mn5 and Mn6 are turned ON immediately. The stored value on node Q and BL maintain its initial value logic 1, while the BLB is discharged to 0 through transistors Mn2 and Mn6. Read operation is completed when the difference between bit lines BL and BLB is identified by a sense amplifier, and the stored value of the memory cell is output. For write operation, the bit lines BL and BLB are pre-charged to 0 and 1, respectively and initially assumed that output nodes Q and QB are at 1 and 0 sate, respectively. When the WL signal is activated, the state stored on the bit lines BL and BLB will charge node QB to 1 and discharge node Q to 0 respectively. Figure 6.5 shows the waveforms for read and write operations in a fault free scenario. Therefore, these simulated waveforms validate the capability of achieving a proper operation (write and read) by the proposed 12T memory cell.

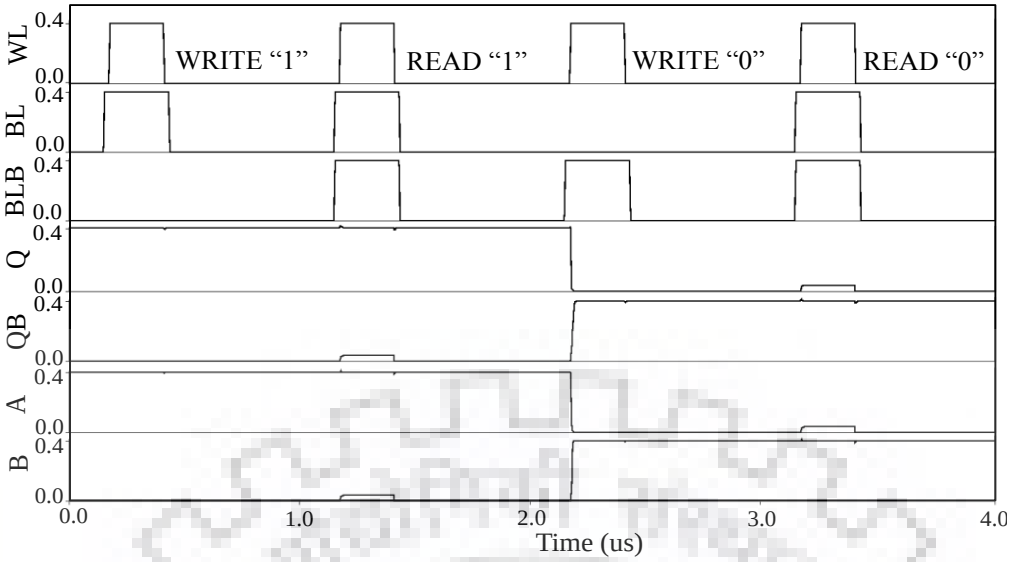


Figure 6.5 Post-layout simulated waveforms of proposed 12T memory cell for fault free case in STMicroelectronics 65-nm technology at V_{DD}=0.4V

The basic principle of SEU hardening of the proposed RHD-12T memory cell is explained as follows: Consider the TF case (when WL = 0) in which an SEU occurs at one of the sensitive nodes (Q, QB, A, or B) of the proposed 12T SRAM cell shown in Fig. 6.4 (a). All the four nodes are driven by a PMOS and an NMOS transistor and gate of these transistors are connected to the two different nodes. Consequently, if a soft error/TF pulls up (down) the node voltage level of Q and QB, it can be restored by the 'ON' transistors (NMOS/PMOS) connected to the node and driven by an unaffected node. If the voltage level of node A (B) is pulled down, it would be restored by the unaffected transistor Mp4 (Mp3). If the voltage level of either of the nodes A (B) is pulled up, it would be restored by the unaffected transistor Mn4 (Mn3). Therefore, in the event of an SEU, our memory cell automatically corrects the error.

Now, we discuss the SEU and SEMNU recovery mechanism for the proposed memory cell. We assume Q = 1, QB = 0, A = 1, and B = 0 for the entire analysis. For the proposed 12T memory cell, according to the single event upset physical mechanism, the nodes A, B, Q, and QB are the susceptible nodes.

1) If the node Q is discharged to 0 by an SEU, transistor Mn2 will be temporarily OFF. However, the voltage of node B will be in its initial state (logic "0"). Consequently, the transistor Mp1 will be always ON. Therefore, the state of node 'Q' will be flipped to its initial state (i.e. logic 1).

2) When the intermediate node QB is flipped due to an SEU, transistors Mn1 and Mn4 will be temporarily ON and then the voltage of node Q will be discharged to 0. Hence, transistor Mn2 will be temporarily turned OFF. However, the state of node A will be at its initial state, because

the size of transistor Mp4 is larger than that of Mn4 (1.7 X larger). Consequently, the state of node B is unchanged. Therefore, the output node Q and node A will be charged up to logic level 1, and then transistor Mn2 will be turned ON again, and node QB will be pulled down to logic level 0. Consequently, the intermediate nodes will not be corrupted by an SEU.

3) Further, we consider an SEU at node A while it holds logic 1. The logic state at node A is recovered by the state stored at node B. The fault can not affect the node QB because in this case transistor Mn2 remains in ON state due to the initial state stored at node Q. Also, the transistor Mp4 is in ON state by the initial state stored at node B. Consequently, the correct logic 1 is restored at the affected node A.

4) Furthermore, we consider a TF occurs at node B which changes the state of the node to logic 1. The fault cannot affect the node Q because in this case transistor Mn1 remains in OFF state by logic stored on node QB. The logic state at node B is recovered by the state stored at node Q. Transistor Mn3 is in ON state by the initial state stored on node Q.

5) Due to the charge sharing effect in an SRAM cell, multiple nodes may be affected by an SEU. Now, we consider that the node pair A-B is upset, transistor Mp1 and Mp3 will be temporarily turned OFF. In this case logic state at node B is recovered by transistor Mn3 which is in ON state by the initial state stored on node Q. Further, the discussion is similar as in the case 3.

6) Now, we consider that the node pair Q-QB is affected by SEU. In this scenario, transistors Mn1 and Mn4 turned ON while Mn2 and Mn3 turns OFF. Output node Q is recovered to its initial state by Mp1 due to the unaffected state of node B. Consequently, the transistor Mn2 will be turned ON and the state of QB restored.

7) When node pairs A–Q/QB or B–Q/QB is upset due to charge sharing effect by an SEU. In this case, the stored state cannot be restored. However, when the spacing of nodes A/B and node pair Q–QB is large enough, the probability of the charge sharing-induced multiple nodes upset can be minimized. Fig. 6.4(b) shows the layout of the proposed RHBD-12T memory cell in which the transistor–transistor spacing of node pairs A-Q/QB and B-Q/QB is greater than the effective range of charge sharing (about 1.5 μm [155], [156]). Therefore, in this work, we focus only on the Q-QB and A-B node pairs.

Figure 6.6 shows the post layout parasitic extracted waveforms of the proposed 12T radiation hardened SRAM cell when the particle strikes on nodes Q, QB, A, and B. It can be concluded

that if a TF occurs due to SEU on susceptible nodes Q, QB, A, B or even node pairs Q-QB and A-B, our memory cell is able to hold its original state.

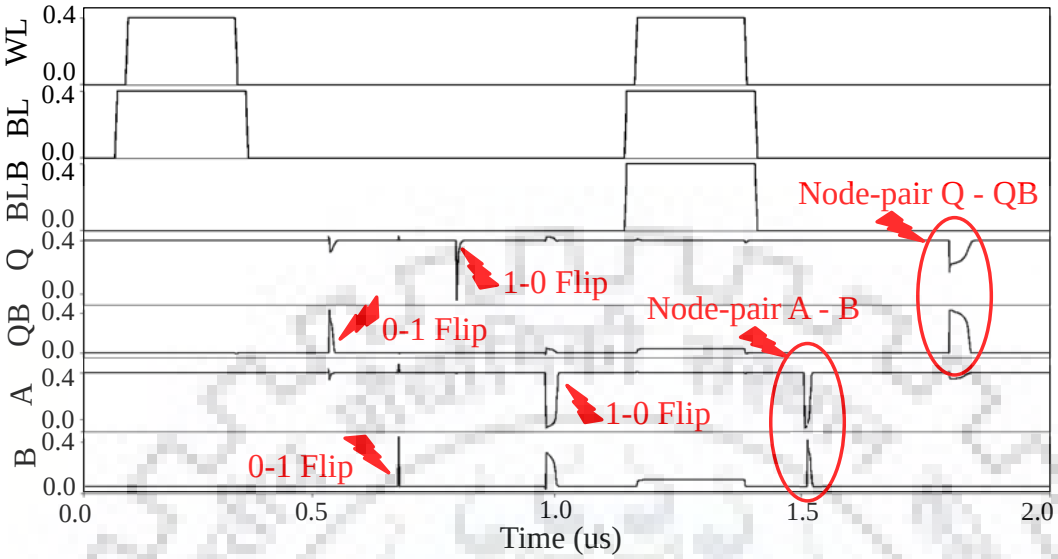


Figure 6.6 Simulated waveforms for proposed 12T SARM cell when a particle strikes on nodes Q, QB, A, and B for an STMicroelectronics 65-nm technology at 0.4 V supply voltage.

6.3 Simulation Results

For performance comparison, we have borrowed same simulation set up as discussed in chapter 5. A high SEU tolerance is realized in radiation hardened SRAM cells by using redundancy at the expense of performance, power and area overhead. Therefore, in this section we compare the performance overhead of the proposed memory cell to reported radiation hardened memory cells namely, 10T, NS10T, PS10T, Quatro10T, DICE, 12T and RHBD-12T cells.

Table 6.1 compare the figures-of-merit (FOM) of power, area, read/write noise static margins (RSNM/WSNM), and read/write access time (RAT/WAT). The FOM's of the parasitic extracted net-lists of the proposed memory cell with 10T, NS10T, PS10T, Quatro10T, DICE, 12T and RHBD-12T cells, all implemented in the STMicroelectronics 65nm technology. Table 6.1 shows that the area of the proposed memory cell is 20%, 3%, 22%, 42% and 16% less as compared to 10T, Quatro-10T, DICE, 12T and RHBD 12T, respectively. The 6T SRAM cell has less area as compared to the proposed memory cell; however, 6T SRAM cannot handle SEU/SEMNU. The proposed SRAM cell has lower power dissipation than PS10T, DICE, 12T and RHBD12T SRAM cells, and nearly the same power dissipation compared to Quatro-10T and NS10T. However, Quarto-10T and NS10T memory cells only provide partial soft error immunity (only mitigate 1-0 flip). RAT is calculated as the time difference between from the moment when the bit lines (BL/BLB) voltages discharged by 50mV from V_{DD} to the word line

(WL) crossing 50% of VDD, which is done as in [122], [157]. In order to calculate a high fan-out (FO), a 0.2 pF capacitance is connected to the BL/BLB, which is according to [122]. Table 6.1 shows that the proposed memory cell takes less time for completing read operation compared to 10T, NS10T, PS10T, Quatro10T, 12T and RHBD-12T cells. The proposed memory cells has nearly the same read access time as 6T SRAM cell, this is because both the memory cells have the same pull-down transistor and access transistor. Whereas, in other memory cells the capacitive load is increased due to an addition of the redundant transistors which degrades the performance.

Table 6.1 Cost comparison of post layout parasitic extracted performance of proposed 10T SRAM and 12T SRAM cells in STMicroelectronics 65-nm CMOS technology

FOM / SRAM cells	WSNM (mV)	RSNM (mV)	WAT (pS)	RAT (pS)	Avg. Power (nW)	area	% of Failure
6T	198	50	135.60	418.80	2.46	9.76	100%
10T	102	24	145.30	465.90	2.93	18.34	85%
NS-10T	217.62	74.95	139.92	499.04	3.07	14.52	100%
PS-10T	240.01	43.65	142.48	492.73	3.35	15.36	100%
Quatro-10T	239	58	147.48	495.73	3.26	14.99	96%
DICE	210	37	129.40	263.20	4.50	18.73	100%
12T	198	52	151.70	503.45	3.97	25.11	100%
RHBD-12T	218	51.80	207.30	491.20	3.83	17.26	0%
Proposed 10T	212.78	55	138	419.01	3.30	13.02	0%
Proposed 12T	213.99	55.05	138.50	419.70	3.30	14.52	0%

Table 6.1 also shows that the write access time of the proposed SRAM cell is 33.18% less as compared to RHBD-12T. The proposed memory cell requires less time for the write operation, because of the parallel paths from BL (BLB) to Mp1-Mn2 (Mp2-Mn1). Static noise margin metrics (SNM) are generally used as the benchmark of stability. In this chapter, we also

compare RSNM and WSNM of the proposed SRAM cell to the other memory cells. From Table 6.1 it can be seen that the RSNM of the proposed SRAM cells is larger than the 10T, PS10T, DICE, 12T, 6T and RHBD-12T memory cells, which shows that our SRAM cells has better read stability. In addition, Table 6.1 indicates that our SRAM cells has a larger WSNM than the 10T, 12T, and DICE memory cells.

6.4 Soft Error Robustness Simulations using TCAD Tool

For Synopsys Sentaurus technology computer-aided design (TCAD) mixed mode simulations, we have borrowed same simulation set up as discussed in chapter 5. Figure 6.7 shows Sentaurus TCAD mixed-mode simulation results for the SEU cases. Figure 6.7(a) show the NMOS-hit by heavy ion while Fig. 6.7 (b), (c), and (d) shows the PMOS-hit by heavy ion. The proposed memory cell can tolerate the impact of heavy ion strike with a linear energy transfer (LET) of 30 MeV-cm2/mg at normal (90◦) strike.

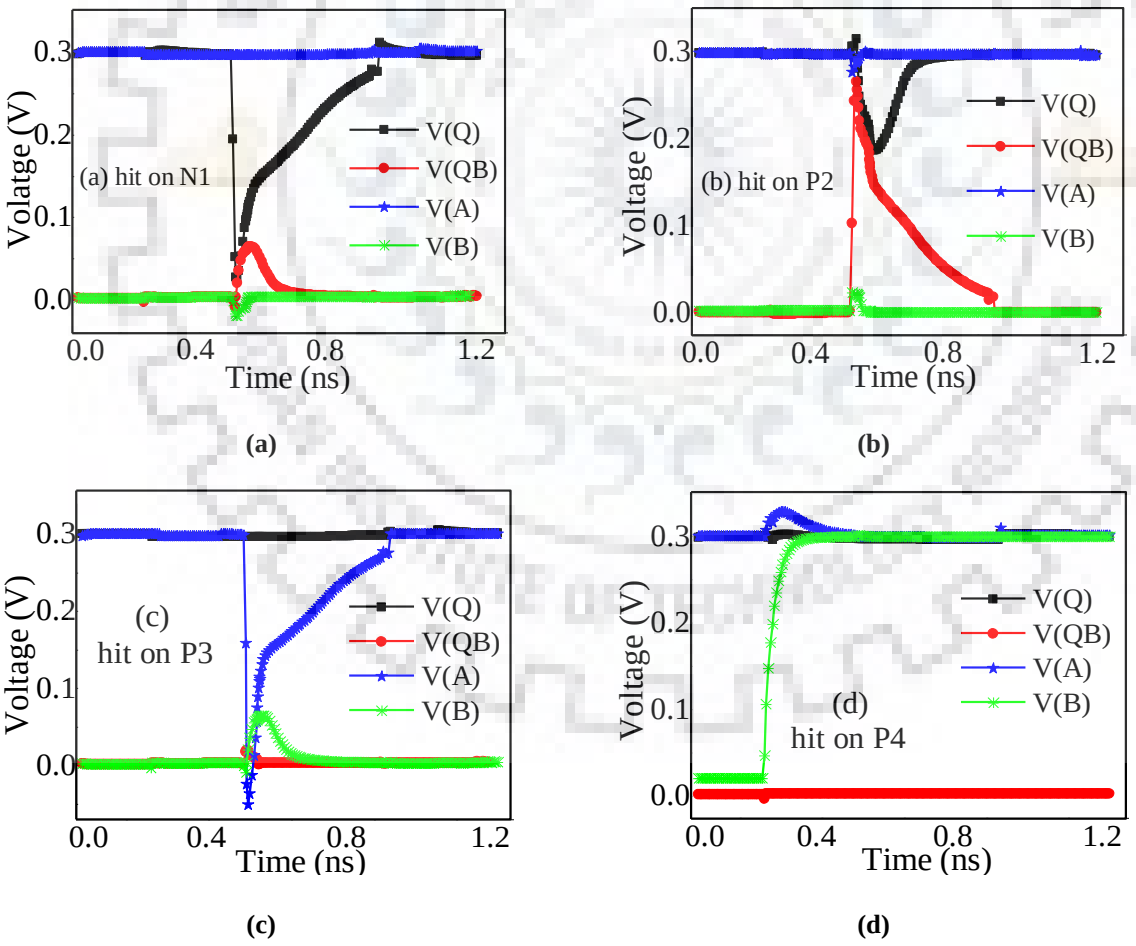


Figure 6.7 Node voltages v/s time for TCAD mixed mode simulation using 32-nm CMOS technology with LET = 30 MeV-cm2/mg strike on (a) node Q, (b) node QB, (c) node A, (d) node B for proposed 10T SRAM cell.

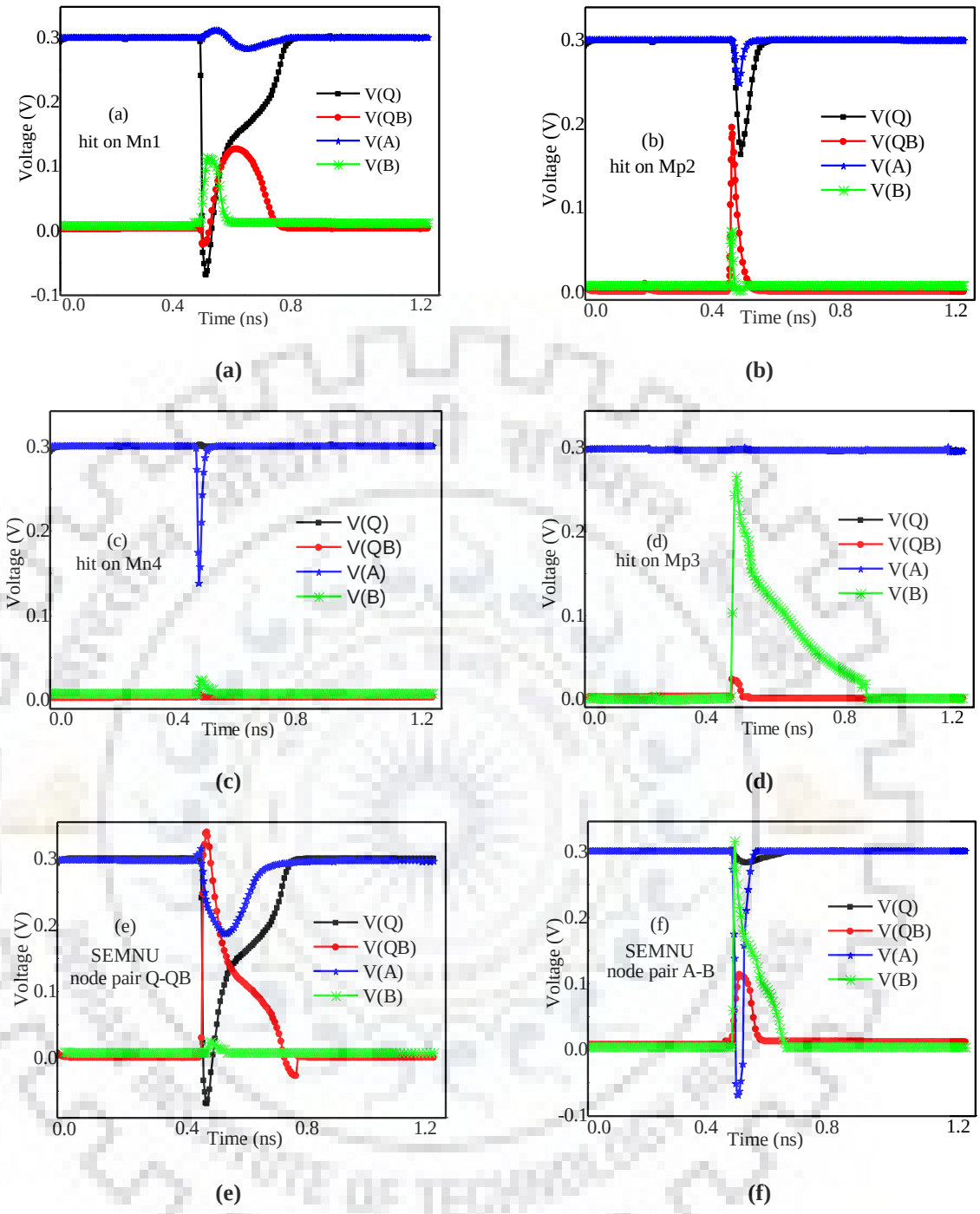


Figure 6.8 Node voltages v/s time for TCAD mixed mode simulation using 32-nm CMOS technology with LET = 30 MeV-cm2/mg strike on (a) node Q, (b) node QB, (c) node A, (d) node B, (e) node pair Q-QB, and (f) nodepair A-B for proposed 12T SRAM cell.

Figure 6.8 shows Sentaurus TCAD mixed-mode simulation results for the SEU/ SEMNU casesof the proposed 12T SRAM cell. From Fig. 6.8 we can see that the proposed memory cell can mitigate the impact of heavy ion strike with a linear energy transfer (LET) of 30 MeV-cm2/mg for a normal (90◦) strike angle. Fig. 6.8(a) and (c) shows the NMOS-strike by heavy ion cases while Fig. 6.8(b) and (d) show the PMOS-strike by heavy ion cases.

Fig. 6.8 also shows the single event multiple-node upset cases due to the charge sharing effect. Fig. 6.8 (e) and (f) shows cases when SEMNU occurs at node pair Q-QB and A-B, respectively. From Fig. 6.8, we validate that the proposed 12T memory cell also mitigates the heavy ion strike on node pair Q-QB. It means that the proposed RHD-12T SRAM cell can tolerate the impact of heavy ion strike with a LET of 30 MeV-cm2/mg at normal (90◦) strike.

Table 6.2 show the comparison of FOM's of the proposed memory cells with 10T, NS10T, PS10T, Quatro10T, DICE, 12T and RHBD-12T cells, all memory cell are implemented in 32nm technology mixed mode simulation using Synopsys TCAD tool. In 32nm technology the proposed memory cell shows higher performance (in terms of RAT and WAT) and also better robustness against SEU without a power consumption overhead. In the 32nm technology the proposed SRAM cell has lower power dissipation than the 10T, PS-10T, DICE, 12T and RHBD12T memory cells, and nearly the equal power dissipation compared to Quatro-10T and NS10T. However, Quarto-10T and NS10T memory cells only provide partial SEU immunity.

Table 6.2 Cost comparison of performance of proposed 10T SRAM and 12T SRAM cells in 32-nm CMOS technology

FOM / SRAM cells	WSNM (mV)	RSNM (mV)	WAT (pS)	RAT (pS)	Avg. Power (nW)
6T	96.41	32.96	44.25	31.59	7.41
10T	86.88	16.17	54.90	36.36	8.73
NS-10T	118.94	41.24	47.95	43.14	8.48
PS-10T	125.81	30.06	51.84	38.74	8.88
Quatro-10T	127.00	40.56	53.08	39.61	6.64
DICE	112.00	25.13	23.54	17.59	8.97
12T	108	34.08	52.77	34.94	10.05
RHBD-12T	115.75	34.82	56.54	36.81	9.53
Proposed 10T	124	36	25	33	8.18
Proposed 12T	119.99	36.96	22.92	31.61	8.50

6.5 Summary

In this chapter, two novel highly reliable energy efficient radiation hardened SRAM cells in the near-threshold voltage regime are presented. The proposed memory cells maintain their SEU tolerance in the presence of PVT variations. Using post-layout parasitic extraction, we have shown that the proposed memory cell improves the performance in terms of RAT/WAT (WSNM/RSNM) up-to 4%/10% (52%/56%), 17%/9% (7%/6%), and 14%/33% (-2%/6%) over recently reported 10T, 12T, and RHBD12T, respectively at 0.4V power supply in an STMicroelectronics 65nm technology. The proposed 10T SRAM cell is robust for SNU while the proposed 12T SRAM cell also mitigates the effect of SEMNU. We have also validated the proposed memory cell in 32nm CMOS technology calibrated with TCAD. In 32nm technology our memory cells can tolerate the impact of heavy ion strike with a linear energy transfer (LET) of 30 MeV-cm2/mg at normal (90◦) strike. TCAD mixed mode simulations show that our memory cells has better results as compared to the reported memory cells.

7 CHAPTER

Conclusion & Future Scope

7.1 Conclusion

Energy and power-efficient designs have become attractive for today's electronic systems. Today's processors require a system that not only consumes less power, but also function at the desired performance [1]. Near-threshold voltage (NTV) operation of the circuit has become more important in internet of things (IoT), biomedical, wearable devices and sensor node applications. Operating circuits in NTV regime is one of the most efficient techniques to design power efficient systems [2]. However, though energy efficient, system performance/functionality is at stake, because of the increase in the variability and reliability issues in NTV regime. Process, voltage, and temperature (PVT) variations and radiation-induced soft errors are the main causes of performance degradation and functional failures in NTV circuits. Traditionally, circuit designers used safety margins for a reliable circuit operation in the worst operating conditions. The use of safety margins ensures reliable circuit operations but these margins degrade the performance and increase the power dissipation. Therefore, resilient circuit approaches are necessary in alleviating the performance degradation and data retention failures resulting from PVT variations and radiation induced soft errors. The advantage of resilient techniques is that they self correct the errors which occur because of variations and external transient noise in sequential circuits [17].

In this thesis, a framework is proposed to handle timing errors and soft errors issues using resilient apporoches in the NTV regime. First we proposed a resilient latch to handle the timing errors due to PVT variations in the NTV region. In addition to this, since radiation-induced soft error are a major issue in the NTV regime, this work also explores these issues. We proposed a model to estimate the critical charge for a static D latches in NTV regime is proposed. Using the proposed model, the soft error susceptible latches/Flip-Flop's can be easily identified and these latches/Flip- Flop's can be replaced by reported radiation hardened latches at the desgin stage. However, the reported radiation hardened latches are implemented with too large cost penalties in terms of delay, power and area. To overcome this issue, we proposed low cost and highly reliable radiation hardened latches in the NTV regime. Conceptually, data storage cells, i.e., SRAM cells, and static D-latches are similar because both circuits have two stable

operating points. Hence, the radiation-induced soft error challages faced by static latches are similar to those of SRAM cells. Therefore, we have proposed radiation hardened SRAM cells in the final part of this work .

To address the above-mentioned issues, first, we proposed a low area timing error resilient circuit technique in sub/near-threshold regime. In the case of timing violation due to PVT variations in the datapath, the proposed self-correcting latch (SCL) technique automatically chooses an appropriate faster path, thereby reducing the setup time. Our technique automatically corrects the set-up time error by generating an equivalently delayed version of the input clock signal. The advantage of our technique is that the effective clock to Q delay increases only marginally. The proposed SCL technique employs a transmission gate based multiplexer in a latch, with the transmission gates differing in their layout implementations. Inverse Narrow Width Effect (INWE) is used to implement the faster path (transmission gate), which is activated in the cases of timing violations. The proposed SCL technique shows a higher performance and better robustness against PVT variations without power consumption overhead over earlier resilient circuit techniques. We have shown that under PVT variations the SCL technique implementation on several ISCAS'89 benchmark circuits improves the performance in terms of delay approximately 30% as compared to existing methodologies. We also observed that our SCL technique is less variant compared to other existing approaches. Post-layout simulations show that our technique achieves 4.85% and 7.73% less area compared to the earlier proposed techniques.

We presented a comprehensive physics based model to estimate the critical charge for NTV latches for the first time. Which is a key to assessing the soft error susceptibility of static D-latches. In literature, models are derived for the estimation of critical charge for SRAM cells only. The models for SRAM cells presented in the literature are time consuming iterative SPICE simulations for estimating the critical charge. Whereas, the proposed model is less time consuming than SPICE simulations. Accordingly, it will enable fast but accurate estimation of the soft error vulnerability of static D-latches at an initial design stage. To develop the proposed model, we first argue that the value of the critical charge increases with fan-out load. Based on this model, we devise a methodology to estimate the critical charge using a few DC simulations and a single transient SPECTRE simulation for a given process design kit (PDK). This is an end to end method to include an accurate estimation of the critical charge for latches in NTV standard cell library characterization. This method results in an estimate of the latch's critical charge for different values of fan-out load, supply voltages and temperature. The proposed

methodology estimates the critical charge of a static D-latch with a maximum error of 3.4% at different power supply compared with SPECTRE simulations. Further, the model predicts the changes in the critical charge accurately for different process corners. This methodology also addresses the issue of critical charge due to PVT variations.

The major drawback of most reported techniques is that their cost is too high and also they provide limited level of reliability. To address this issue, we proposed three low cost highly reliable energy efficient radiation hardened latches in the NTV regime. The proposed latches provide the soft error tolerance by using memory element/restorer circuits (RC) to hold the correct state and Muller C-elements. The memory element/ RC are based on pull-up and pull-down paths, controlled by different susceptible nodes, results in better radiation-induced soft error tolerance. Furthermore, we use INWE at the layout level of the proposed latches to improve the D-Q and CLK-Q transmission delays. The proposed latches effectively, maintain its radiation-induced soft error tolerance in the presence of PVT variations. We also observed that the area energy delay product (AEDP) of our TNU hardened latch is 89% and 42% smaller than that of the recently reported TNUHL and LCTNUT latches. Moreover, we also validated the proposed radiation hardened latches in Sentaurus TCAD using 32nm calibrated CMOS technology. From TCAD mixed mode simulation we have validated that our latches can provide radiation tolerance up to the value of linear energy transfer (LET) equals to 170 Mev-cm2/mg in 32nm technology.

The final part of this work analyzes the impact of radiation-induced soft error in SRAM cells operating in the NTV regime. In sub/near-threshold region, existing radiation hardened SRAM cells are too expensive. Therefore, two highly reliable energy-efficient radiation hardened by design (RHBD) SRAM cells in the NTV regime have been proposed. The proposed cells maintain its radiation-induced soft error tolerance in the presence of PVT variations. Using post-layout parasitic extraction, we have shown that the proposed memory cells improve the performance in terms of RAT/WAT up-to 14%/6% over recently reported SRAM cells. TCAD mixed mode simulations show that our memory cells have better results as compared to the existing memory cells. Therefore, for NTV and aerospace applications our proposed memory cell would be a better a choice.

7.2 Future Scope

Based on the research work presented in this thesis, a number of directions for future work have been identified.

- A resilient circuit has been designed to handle hold time violation and metastability issues. Since hold time and metastability have become major concerns for low-power design, it will be necessary to have a hold time or metastability monitor to prevent such failure occurrence.
- The proposed critical charge model for soft error rate (SER) estimation can be used to develop an automated SER prediction tool. A computer program in python or pearl could be used in this purpose. This tool will be able to estimate the change in the SER performance when the circuit under test is designed by varying different transistor parameters. The tool can be used to estimates the SER variation due to the process variability accurately, and thus it can be very useful for radiation hardened circuit designers.
- The proposed critical charge estimation methodology for static D-latch can be extended to different type of latches/flip-flops can be developed.
- It would be interesting to check the validity/applicability of the proposed techniques for circuit design methodologies using novel devices (FinFET, NCFET etc.).

APPENDIX A

In this appendix we present the reason behind the slope of voltage at node N2 (dV2/dt) is constant for different fan-out load (FO) (assumption in chapter 4).

Suppose a high energy/ alpha particle strike at node N1 of Fig. 4.7, KCL at node N2

$$C_{N2}\frac{dV_2}{dt} = I_{MP1} \tag{A1}$$

Where, C_{N2} is the total capacitance at node N2. In subthreshold region, the subthreshold current is modelled as [147]

$$C_{N2}\frac{dV_2}{dt} = I_0 \exp\left(\frac{V_{GS,Mp1} - |V_{th,p}|}{nV_T}\right)\left[1 - \exp\frac{V_{DS,Mp1}}{V_T}\right][1 + \lambda(V_{Ds,Mp1})]$$

V_{DS} ($V_{DS} \approx V_{DD}$) is much larger than the V_T (26mV) at room temperature therefore, the term in above equation [1-exp ($-V_{DS}/V_T$)] ≈ 1.

$$V_{GS,Mp1} = V_{DD} - V_1 \; and \; V_{Ds,Mp1} = V_{DD} - V_2$$

V_1 and V_2 are the voltages at node N1 and N2, respectively.

$$I_0 \exp\left(\frac{V_{DD} - V_1 - |V_{th,p}|}{nV_T}\right)[1 + \lambda\,(V_{DD} - V_2) = C_{N2}\frac{dV_2}{dt}$$

The value of V_1 adjusts (reduces) as C_{N2} changes (increases). Let us suppose C_{N2} increases by a factor of α.

Let the time at which the energy particle strikes be t = 0

For a given time $t = t_k$, voltage at node N1 ($V_1(t_k)$) reduces by a small value ΔV_1 because Mp1 needs supply a larger charge for this case

i.e., $V_{1new} = V_1 - \Delta V_1$

where, V_{1new} = voltage at node N1 at time $t = t_k$ for α *CN2

V_1 = voltage at node at time t = tk for CN2

ΔV_1 = change in voltage at node N1 for increasing in load capacitance from CN2 to α *CN2

Suppose dV_2/dt also changes,

Suppose C_{N2} increases by a factor α, V1 changes by a factor ά (ά << α).

$$I_{0P}\exp\left(\frac{V_{DD}-V_1+\Delta V_1-|V_{th,p}|}{nV_T}\right)[1+\lambda\,(V_{DD}-V_2-\Delta V_2)\;=\alpha*C_{N2}\left[\frac{dV_2}{dt}+\;\Delta\;\frac{dV_2}{dt}\right]$$

$$I_{0P}\exp\left(\frac{V_{DD}-V_1-|V_{th,p}|}{nV_T}\right)\exp\left(\frac{\Delta V_1}{nV_T}\right)[1+\lambda\,(V_{DD}-V_2-\Delta V_2)\;=\alpha*C_{N2}\left[\frac{dV_2}{dt}+\;\Delta\;\frac{dV_2}{dt}\right] \qquad \text{(A2)}$$

At time t = tk

Suppose, voltage V2 changes (reduces) as CN2 changes (increase) with factor alpha.

From (A2), we can see that the change in V1 voltage is very small, this because ΔV_1 is comes under the exponential function.

So, from above discussion/(A2) we can say that there is very small change in V1 voltage if V2 changes (reduces) as CN2 changes (increase)

Now we apply KCL at node N1,

$$C_{N1}\frac{dV_1}{dt}=\;I_{0P}\exp\left(\frac{V_{GS,p}-|V_{th,p}|}{nV_T}\right)\left[1-\exp\frac{V_{DS,p}}{nV_T}\right][1+\lambda(V_{Ds,p})]$$
$$+\,I_{0N}\exp\left(\frac{V_{GS,n}-|V_{th,n}|}{nV_T}\right)\left[1-\exp\frac{V_{DS,n}}{nV_T}\right][1+\lambda(V_{Ds,n})]$$

$$V_{GS,p}=\;V_{DD}-V_2\;and\;V_{DS,p}=\;V_{DD}-V_1$$

$$V_{GS,n}=\;V_2\;and\;V_{DS,n}=\;-V_1$$

$V_{DS,p}$ is much larger than the V_T at room temperature therefore, the term in above equation $[1-\exp(-V_{DS,p}/V_T)] \approx 1$.

$V_{DS,n}$ is very small therefore, the term $[1+\lambda V_{DS,n})] \approx 1$.

$$C_{N1}\frac{dV_1}{dt}=\;I_{0P}\exp\left(\frac{V_{DD}-V_2-|V_{th,p}|}{nV_T}\right)[1+\lambda(V_{DD}-V_1)]$$
$$+\,I_{0N}\exp\left(\frac{V_2-|V_{th,n}|}{nV_T}\right)\left[1-\exp\frac{-V_1}{nV_T}\right]$$

Suppose CN2 increases by a factor α and dV1/dt is also increases by a factor ά (<< α)

$$\acute{\alpha} * C_{N1}\frac{dV_1}{dt} = I_{0P}\exp\left(\frac{V_{DD}-V_2+\Delta V_2-\left|V_{th,p}\right|}{nV_T}\right)[1+\lambda(V_{DD}-V_1+\Delta V_1)] + I_{0N}\exp\left(\frac{V_2-\Delta V_2-\left|V_{th,n}\right|}{nV_T}\right)\left[1-\exp\frac{-V_1+\Delta V_1}{nV_T}\right] \quad \text{(A3)}$$

At time t = tk

From (A3), we can see that the change in V2 voltage has a large impact on V1 voltage

Both equation (A2) and (A3) are not inconsistent it means there is a very small change in V2 this argument is fit for the validation/ consistent of both equations.

All terms of ΔV2 are linear in (A2) while exponential in (A3), it implies that V_2 remains almost constantly varying with time as C_{N2} (fan-out load) changes.

<u>We have also shown below the mathematical argument for the reason why dv2/dt is constant with FO's load.</u>

Applying KCL at node N_2 in Fig. 4.7

$$I_{MP1} = C_{N2}\frac{dV_2}{dt} \quad \text{(A4)}$$

$$I_0\exp\left(\frac{V_{GS,p}-\left|V_{th,p}\right|}{nV_T}\right)[1-\exp\frac{V_{DS}}{V_T}]\ [1+\lambda\,(V_{DS})] = C_{N2}\frac{dV_2}{dt} \quad \text{(A5)}$$

V_{DS} is much larger than the V_T at room temperature therefore, the term [1-exp ($-V_{DS}/V_T$)] ≈ 1.

$$I_0\exp\left(\frac{V_{DD}-V_1-\left|V_{th,p}\right|}{nV_T}\right)[1+\lambda\,(V_{DD}-V_2) = C_{N2}\frac{dV_2}{dt} \quad \text{(A6)}$$

$$I_0\exp\left(\frac{V_{DD}-V_1-\left|V_{th,p}\right|}{nV_T}\right) = f_1(V_1)$$

$$f_1(V_1)[1+\lambda\,(V_{DD}-V_2) = C_{N2}\frac{dV_2}{dt}$$

$$\int_0^{V_2}\frac{dV_2}{[1+\lambda\,(V_{DD}-V_2)]} = \frac{1}{C_{N2}}\int_0^t f_1(V_1)dt$$

$$\int_0^{V_2} \frac{dV_2}{[1+\lambda\,(V_{DD}-V_2)]} = \frac{1}{C_{N2}}\, f_{11}(V_1(t), t) \qquad \text{(A7)}$$

From above equation we see that the node voltage (V_2) at N_2 is not a function of C_{N2}. The same values of V_2 can be obtained for several values of C_{N2}. However, V_2 is a function of both V_1 and C_{N2}.

Let value of V_2 at a time $t = t_n$ be V_n,

Therefore, from above equation,

$$f_{11}(V_1(tn), tn) = V_n * C_{N2}$$

$$f_{11}(V_1(t_{n-1}), t_{n-1}) = V_{n-1} * C_{N2}$$

.

.

.

$$f_{11}(V_1(0), 0) = 0$$

Above equations shows that $V_1(t)$ is an implicit function w.r.t. C_{N2}. Therefore, from above discussion we can see that, $V_1(t) = f(C_{N2})$.

It implies that $\frac{dV_1(t)}{dt}$ is also a function of C_{N2}.

$$f(C_{N2}) = \frac{dV_1(t)}{dt}$$

the charging current on the node N1 due to the feedback path is a function of V1 and V2

Let at time $t = t_K$

$$\left.\frac{C_{N1}dV_1}{dt}\right|_{t=t_K} = f_2(V_1(t), V_2(t)\big|_{t=t_K} \qquad \text{(E8)}$$

Function of C_{N2}

$V_2(t)$ is either constant or a function of C_{N2}

From (E7), and (E8) we observe the for different values of C_{N2}, $V_2(t)$ would have the same value (it means V_1 changes according to C_{N2}). It implies that $\frac{dV_2}{dt}$ is constant with C_{N2} (fan-out load).

From above discussion we can say that $\frac{dV_2}{dt}$ is constant with fan-out load.

BIBLIOGRAPHY

[1] D. Markovic, C. C. Wang, L. P. Alarcon, T. Liu and J. M. Rabaey, "Ultralow-Power Design in Near-Threshold Region," in *Proceedings of the IEEE*, vol. 98, no. 2, pp. 237-252, Feb. 2010.

[2] V. Stojanovic, D. Markovic, B. Nikolic, M. A. Horowitz and R. W. Brodersen, "Energy-delay tradeoffs in combinational logic using gate sizing and supply voltage optimization," *Proceedings IEEE European Solid-State Circuits Conference*, Florence, Italy, 2002, pp. 211-214.

[3] H. Kaul, M. Anders, S. Hsu, A. Agarwal, R. Krishnamurthy and S. Borkar, "Near-threshold voltage (NTV) design — Opportunities and challenges," *DAC Design Automation Conference*, San Francisco, CA, 2012, pp. 1149-1154.

[4] S. Hsu, A. Agarwal, M. Anders, S. Mathew, H. Kaul, F. Sheikh, and R. Krishnamurthy, "A 280mV-to-1.1V 256b reconfigurable SIMD vector permutation engine with 2-dimensional shuffle in 22nm CMOS," *IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2012, pp. 178-180.

[5] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi and V. De, "Parameter variations and impact on circuits and microarchitecture," *Proceedings IEEE Design Automation Conference*, Anaheim, CA, 2003, pp. 338-342.

[6] S. Borkar, T. Karnik and Vivek De, "Design and reliability challenges in nanometer technologies," *Proceedings IEEE Design Automation Conference*, San Diego, CA, USA, 2004, pp. 75-75.

[7] S. P. Mohanty and A. Srivastava, "Nano-CMOS and post-CMOS electronics: circuits and design," vol. 2, The Institute of Engineering and Technology, 2016.

[8] S. Burman, A. Palchaudhuri, R. S. Chakraborty, D. Mukhopadhyay and P. V. Singh, "Effect of Malicious Hardware Logic on Circuit Reliability," in *Proc. Springer VDAT*, Shibpur, India, 2012, pp. 190-197.

[9] R. A. Thakker, C. Sathe, M. S. Baghini and M. B. Patil, "A Table-Based Approach to Study the Impact of Process Variations on FinFET Circuit Performance," in *IEEE Trans. Computer Aided Design of Integrated Circuits and Systems*, vol. 29, no. 4, pp. 627-631, April 2010.

[10] S. Narasimhan, S. Paul, R. S. Chakraborty, F. Wol, C. Papachristou, D. Weyer and S. Bhunia, “System level self-healing for parametric yield and reliability improvement under power bound," in *Proc. NASA/ESA Conference on Adaptive Hardware and Systems*, Anaheim, CA Jun. 2010, pp. 52-58.

[11] R. A. Thakker, C. Sathe, A. B. Sachid, M. S. Baghini, V. R. Rao and M. B. Patil, “A Novel Table-Based Approach for Design of Fin-FET Circuits," in *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 28, no. 7, pp. 1061-1070, July 2009.

[12] V. Ferlet-Cavrois, L. W. Massengill, and G. Pascale, “Single event transients in digital CMOS—A review,” in *IEEE Trans. Nuclear Science*, vol. 60, no. 3, pp. 1767-1790, June 2013

[13] A. K. Pudi N S and M. S. Baghini, "Robust Soft Error Tolerant CMOS Latch Configurations," in *IEEE Transactions on Computers*, vol. 65, no. 9, pp. 2820-2834, 1 Sept. 2016.

[14] P. Hazucha and C. Svensson, “Impact of CMOS technology scaling on the atmospheric neutron soft error rate," in *IEEE Trans. on Nuclear Science*, vol. 47, no. 6, pp. 2586-2594, Dec. 2000.

[15] Y. Komatsu, Y. Arima, T. Fujimoto, T. Yamashita, and K. Ishibashi, “A soft error hardened latch scheme for SoC in a 90 nm technology and beyond," in *IEEE CICC*, Orlando, FL, USA, Oct. 2004, pp. 329-332.

[16] N. Cohen, T.S. Sriram, N. Leland, D. Moyer, S. Butler, and R. Flatley, “Soft error considerations for deep-submicron CMOS circuit applications,” in *IEEE IEDM*, Washington, DC, USA, 1999, pp. 315-318.

[17] C.I. Kumar, A. K. Sharma, R. Partap, and A. Bulusu, “An energy-efficient variation aware self-correcting latch” in *Elsevier Microelectronics Journal*, vol. 84, pp. 67-78, 2019.

[18] D. Markovic, V. Stojanovic, B. Nikolic, M. A. Horowitz and R. W. Brodersen “Methods for true energy-performance optimization,” in *IEEE Journal Solid-State Circuits*, vol. 39, no. 8, pp. 1282–1293, Aug. 2004.

[19] R. Dreslinski, M. Wiekowski, D. Blaauw, D. Sylvester, and T. Mudge, “Near-threshold computing: reclaiming Moore's law through energy efficient integrated circuits,” in *Proc. of the IEEE*, vol. 98, no. 2, pp. 253 – 256, Feb. 2010.

[20] E. A. Vittoz, "Weak inversion for ultimate low-power logic," in Low-Power Electronics Design, C. Piguet, Ed. Boca Raton, FL: CRC, 2005.

[21] B. Calhoun, A. Wang, and A. Chandrakasan, "Modeling and sizing for minimum energy operation in subthreshold circuits," in *IEEE Journal Solid-State Circuits*, vol. 40, no. 9, pp. 1778–1786, Sept. 2005.

[22] B. Zhai, D. Blaauw, D. Sylvester, K. Flautner, "Theoretical and practical limits of dynamic voltage scaling," In *Proc. of the IEEE DAC* , San Diego, CA, USA, Jul. 2004, pp. 868-873.

[23] J. Kwong and A. Chandrakasan, "Variation-driven device sizing for minimum energy sub-threshold circuits," in *Proc. of the IEEE ISLPED*, Tegernsee, 2006, pp. 8–13.

[24] C. T. Chuang, S. Mukhopadhyay, J. J. Kim, K. Kim, and R. Rao. "High-performance SRAM in nanoscale CMOS: Design challenges and techniques," in *IEEE IWMTDT*, Taipei, Dec. 2007, pp. 4-12.

[25] H. Kaul, M. Andres, S. K. Mathew, S.K. Hsu, A. Agarwal, R. Krishnamurthy, and S. Borkar, "A 320 mV 56μW 411 GOPS/Watt Ultra-Low voltage motion estimation accelerator in 65 nm CMOS," in *IEEE Journal Solid-State Circuits*, vol. 44, no, 1, pp. 107-114, Jan. 2009.

[26] O. Hirabayashi, A. Kawasumi, A. Suzuki, Y. Takeyama, K. Kushida, and K. Sasaki, "A process-variation-tolerant dual-power-supply SRAM with 0.179m2 cell in 40nm CMOS using level-programmable wordline driver," in *IEEE ISSCC*, San Francisco, CA, Feb. 2009, pp. 458-459.

[27] C. H. Chen, K. Bowman, C. Augustine, Z. Zhang, and J. Tschanz, "Minimum supply voltage for sequential logic circuits in a 22nm technology," in *IEEE ISLPED*, Beijing, Sept. 2013, pp. 181-186.

[28] V. K. Rajanna and B. Amrutur, "Energy efficient memory decoder design for ultra-low voltage systems," in *proc. of the IEEE VLSID*, Mumbai, India, Jan. 2014, pp. 145-149.

[29] V. K. Rajanna and B. Amrutur, "A Variation-Tolerant Replica-Based Reference-Generation Technique for Single-Ended Sensing in Wide Voltage-Range SRAMs," in *IEEE Transactions on VLSI*, vol. 24, no. 5, pp. 1663-1674, May 2016.

[30] C. B. Kushwah, S. K. Vishvakarma and D. Dwivedi, "A 20nm Robust Single-Ended Boost-Less 7T FinFET Sub-threshold SRAM Cell under Process-Voltage-Temperature Variation," in *Elsevier Microelectronics Journal*, vol. 51, no. 5, pp. 75-88, 2016.

[31] C. B. Kushwah and S. K. Vishvakarma, "A Single-Ended with Dynamic Feedback Control 8T Sub-Threshold SRAM Cell," in *IEEE Transactions on VLSI*, vol. 24, no. 1, pp. 373-377, 2016.

[32] N. A. Gilda, V. G. Hande, D. K. Sharma, V. Ramgopal Rao, and M. S. Baghini, "Low power, area efficient, and temperature-variation tolerant bidirectional current source for sensor applications," *Elsevier Microelectronics Journal*, vol. 49, no. 3, pp. 29-35, 2016.

[33] H. V. Gopal, P. Gupta, and M. S. Baghini, "Ultra low-supply voltage reference generator with low sensitivity to PVT variations," in *proc. IEEE ASQED*, Penang, 2013, pp. 18-21.

[34] S. Mukhopadhyay, K. Kang, H. Mahmoodi, and K. Roy, "Reliable and self-repairing SRAM in nano-scale technologies using leakage and delay monitoring," in *IEEE International Conference on Test*, Austin, TX, Jun. 2005, pp. 1-10.

[35] S. Dutt, A. Chauhan, R. Bhadoriya, S. Nandi, and G. Trivedi, "A high-performance energy-efficient hybrid redundant MAC for error-resilient applications," in *IEEE VLSID*, Bangalore, India, 2015, pp. 351-356.

[36] S. Dutt, H. Patel, S. Nandi, and G. Trivedi, "Exploring approximate computing for yield improvement via re-design of adders for error-resilient applications," in *IEEE VLSID*, Kolkata, India, 2016, pp. 134-139.

[37] O. S. Unsal, J. W. Tschanz, K. Bowman, V. De, X. Vera, A. Gonzalez, and O. Ergin, "Impact of Parameter Variations on Circuits and Microarchitecture," in *IEEE Micro*, vol. 26, no. 6, pp. 30-39, 2006.

[38] S. P. Mohanty, E. Kougianos, D. Ghai, and P. Patra, "Interdependency study of process and design parameter scaling for power optimization of nano-CMOS circuits under process variation," in *Proc. ACM/IEEE IWLS*, 2007, pp. 207-213.

[39] C. H. Kim, H. Soeleman, and K. Roy, "Ultra-low-power DLMS adaptive filter for hearing aid applications," in *IEEE Trans. on VLSI*, vol. 11, no. 6, pp. 1058-1067, 2003.

[40] H. Mahmoodi, S. Mukhopadhyay, and K. Roy, "Estimation of delay variations due to random-dopant fluctuations in nano-scale CMOS circuits," in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1787-1796, 2005.

[41] A. Asenov, S. Kaya, and J.H. Davies, "Intrinsic threshold voltage fluctuations in decanano MOSFETs due to local oxide thickness variations," in *IEEE Trans. on Electron Devices*, vol. 49, no. 1, pp. 112-119, 2002.

[42] S. Ghosh and K. Roy, "Parameter variation tolerance and error resiliency: New design paradigm for the nano-scale era," in *Proc. of the IEEE*, vol. 98, no. 10, pp. 1718-1751, 2010.

[43] S. K. Saha, "Modeling Process Variability in Scaled CMOS Technology" in *IEEE Design & Test of Computers*, vol. 27, no. 2, pp. 8-16, 2010.

[44] N. Mehta, and B. Amrutur, "Dynamic supply and threshold voltage scaling for CMOS digital circuits using in-situ power monitor," in *IEEE Trans. on VLSI*, vol. 20, no. 5, pp. 892-901, 2012.

[45] M. Alioto, E. Consoli, G. Palumbo, "Variations in nanometer CMOS ip-ops: part Iimpact of process variations on timing," in *IEEE Trans. Circuits and System-I*, vol. 62, no. 8, pp. 2035-2043, 2015.

[46] B.P. Harish, N. Bhat, M. B. Patil, "Analytical modeling of CMOS circuit delay distribution due to concurrent variations in multiple processes," in *Elsevier Solid-State Electronics*, vol. 50 no. 7/8, pp. 1252-1260, 2006.

[47] A. Datta, S. Bhunia, S. Mukhopadhyay and K. Roy, "Delay modeling and statistical design of pipelined circuit under process variation," in *IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems*, vol. 25, no. 11, pp. 2427-2436, 2006.

[48] B. P. Harish, M. B. Patil and N. Bhat, "Modelling of the Effects of Process Variations on Circuit Delay at 65nm," in *Proc. IEEE Conference on Electron Devices and Solid-State Circuits*, Dec. 2005, pp. 761-764.

[49] A. Agarwal, K. Kang, S. Bhunia and K. Roy, "Device-aware yield-centric dual-Vt design under parameter variations in nano-scale technologies," in *IEEE Trans. on VLSI*, vol. 15, no. 6, pp. 660-671, 2007.

[50] N. Reynders and W. Dehaene, "Variation-resilient building blocks for ultra-low-energy sub-threshold design," in *IEEE Trans. Circuits and System II*, vol. 59, no. 12, pp. 898-902, 2012.

[51] M. Wirnshofer, Variation-Aware Adaptive Voltage Scaling for Digital CMOS Circuits, vol. 41, Dordrecht, The Netherlands: Springer, 2013.

[52] J. M. Chang and M. Pedram, Low power design. In Power optimization and synthesis at behavioral and system levels using formal methods, chapter 1. Springer Science & Business Media, 2012.

[53] H. Li, J. Mundy, W. Patterson, D. Kazazis, A. Zaslavsky, and R. I. Bahar, "A model for soft errors in the sub-threshold CMOS inverter," in *Proc. SELSE2*, 2006.

[54] R. C. Baumann, "Soft errors in advanced semiconductor devices - part I: the three radiation sources," in *IEEE Trans. Nuclear Science*, vol. 1, no. 1, pp. 17–22, 2001.

[55] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modelling of single-event upset in digital microelectronics," in *IEEE Trans. Device Material Reliability*, vol. 50, no. 3, pp. 583–602, 2003.

[56] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," in *IEEE Trans. Device Material Reliability*, vol. 5, no. 3, pp. 305–316, 2005.

[57] G.C. Messenger, "Collection of Charge on Junction Nodes from Ion Tracks", in *IEEE Trans. Nuclear Science*, vol. 29, no. 6, pp. 2024-2031, 1982.

[58] J. D. Black, P. E. Dodd, and K. M. Warren, "Physics of multiple-node charge collection and impacts on single-event characterization and soft error rate prediction," in *IEEE Trans. Nuclear Science*, vol. 60, no. 3, pp. 1836–1851, 2013.

[59] K. Zhang and K. Kobayashi, "Contributions of charge sharing and bipolar effects to cause or suppress MCUs on redundant latches," in *IEEE IRPS*, 2013, pp. SE.5.1–SE.5.4.

[60] L. Lantz, "Soft errors induced by alpha particles," in *IEEE Trans. on Reliability*, vol. 45, no. 2, pp. 174–179, 1996.

[61] S. M. Jahinuzzaman, "Modeling and mitigation of soft errors in nanoscale SRAMs," *Ph.D. Thesis*, University of Waterloo, Ontario, Canada, 2008.

[62] C. M. Hsieh, P. C. Murley, and R. Brien, "A field-funnelling effect on the collection of alpha-particle-generated carriers in silicon devices," in *IEEE Trans. Electron Device Letter*, vol. 2, no. 4, pp. 686–693, 1981.

[63] W. M. Elsharkasy, "Low Power Reliable Design using Pulsed Latch Circuits," Ph.D. Thesis, University of California, Irvine, 2017.

[64] A. Floros, Y. Tsiatouhas, and X. Kavousianos, "Timing Error Detection and Correction by Time Dilation," in *IFIP/IEEE International Conference on Very Large Scale Integration-System on a Chip*, 2008, pp. 271-285..

[65] D. Ernst, N. S. Kim, S. Das, S. Pant, R. Rao, T. Pham, C. Ziesler, D. Blaauw, T. Austin, K Flautner, and T. Mudge, "Razor: A low-power pipeline based on circuit-level timing speculation," in *Proc. IEEE/ACM Int. Symp. Microarchitecture*, 2003, pp. 7–18.

[66] V. Joshi, D. Blaauw, and D. Sylvester, "Soft-edge flip-flops for improved timing yield: design and optimization," in *Proc. of the IEEE ICCAD*, 2007, pp. 667-673.

[67] S. Das, C. Tokunaga, S. pant, W. Ma, S. Kalaiselvan, K. Lai, D. Bull, and D. Blaauw, "RazorII: In situ error detection and correction for PVT and SER tolerance," in *IEEE Journal of Solid-State Circuits*, vol. 44, no. 1, pp. 32-48, 2009.

[68] M. Fojtik, D. Fick, Y. Kim, N. Pinckney, D. Harris, D. Blaauw, and D. Sylvester, "Bubble Razor: An architecture-independent approach to timing-error detection and correction," in *IEEE ISSCC*, 2012, pp. 488-489.

[69] K. Bowman, J. W. Tschanz, N. S. Kim, J. C. Lee, C. B. Wilkerson, S. L. Lu, T. Karnik, and V. K. De, "Energy-efficient and meta stability immune resilient circuits for dynamic variation tolerance," in *IEEE Journal of Solid-State Circuits*, vol. 44, no. 1, pp. 49-63, 2009.

[70] K. Kang, S. P. Park, K. Kim, and K. Roy, "On-chip variability sensor using phase-locked loop for detecting and correcting parametric timing failures," in *IEEE Trans. on VLSI*, vol. 18, no. 2, pp. 270–280, 2010.

[71] Y. Jang, Y. Changnoh, K. Jinsang, and W. Cho, "Low-power variation-aware flip flop", in *IEEE ISCAS*, May 2012, pp. 488-491.

[72] C. M. Huang, T. Liu, and T. Chiueh, "An energy-efficient resilient flip-flop circuit with built-in timing-error detection and correction," in *IEEE VLSI-DAT*, Apr. 2015, pp. 1-4.

[73] S. Valadimas, Y. Tsiatouhas, and A. Arapoyanni, "Timing Error Tolerance in Small Core Designs for SoC Applications," in *IEEE Trans. on Computers*, vol. 65, no. 2, pp. 654-663, 2016.

[74] S. Valadimas, A. Floros, Y. Tsiatouhas, A. Arapoyanni, and X. Kavousianos, "The time dilation technique for timing error tolerance," in *IEEE Trans. on Computers*, vol. 63, no. 5, pp. 1277-1286, 2014.

[75] S. Lei, X. Li, and Y. Liu, "Soft-Edge error-detecting flip-flop for lowering error-correction-rate under ultra-low voltage." *in IEEE EDSSC*, 2017, pp. 1-2.

[76] Z. Yong, X. Xiang, C. Chen, and J. Meng, "A new error masking flip-flop with one cycle correction penalty" in *IEEE ASICON*, 2017, pp. 72-75.

[77] Y. Zhang, M. Khayatzadeh, K. Yang, M. Saligane, N. Pinckney, M. Alioto, D. Blaauw, and D. Sylveste, " iRazor: current-based error detection and correction scheme for PVT variation in 40-nm ARM Cortex-R4 processor," in *IEEE Journal of Solid-State Circuits*, vol. 53, no. 2, pp.619-631, 2018.

[78] T. Heijmen, D. Giot, and P. Roche, "Factors that impact the critical charge of memory elements," in *Proc. IEEE IOLTS*, 2006, pp. 57–62.

[79] T. P. Ma and P. V. Dressendorfer, Inonizing Radiation Effects in MOS Devices and Circuits. New York: Wiley, 1989.

[80] T. Nakamura, M. Baba, E. Ibe, Y. Yahag, and H. Kameyama, Terrestrial Neutron-Induced Soft Errors in Advanced Memory Devices. Singapore: World Scientific Publishing, 2008.

[81] P. Hazucha and C. Svensson, "Impact of CMOS technology scaling on the atmospheric neutron soft error rate," in *IEEE Trans. Nuclear Science*, vol. 47, no. 6, pp. 2586-2594, 2000.

[82] J. M. Palau, G. Hubert, K. Coulie, B. Sagnes, M. C. Calvet, and S. Fourtine, "Device simulation study of the SEU sensitivity of SRAMs to internal ion tracks generated by nuclear reactions," in *IEEE Trans. Nuclear Science*, vol. 48, no. 2, pp. 225–231, 2001.

[83] B. Zhang, A. Arapostathis, S. Nassif, and M. Orshansky, "Analytical modeling of SRAM dynamic stability," in *Proc. IEEE/ACM ICCAD*, 2006, pp. 315–322.

[84] S. M. Jahinuzzaman, M. Sharifkhani, and M. Sachdev, "Investigationof process impact on soft error susceptibility of nanometric SRAMs using a compact critical charge model," in *Proc. IEEE ISQED*, 2008, pp. 207–212.

[85] S. M. Jahinuzzaman, M. Sharifkhani, and M. Sachdev, "An analytical model for soft error critical charge of nanometric SRAMs," in *IEEE Trans. on VLSI*, vol. 17, no. 9, pp. 1187-1195, 2009.

[86] H. Mostafa, M. H. Anis, and M. Elmasry, "Analytical soft error models accounting for die-to-die and within-die variations in sub-threshold SRAM cells," in *IEEE Trans. on VLSI*, vol. 19, no. 2, pp. 182-195, 2011

[87] Q. Ding, R. Luo, H. Wang, H. Yang, and Y. Xie, "Modeling the impact of process variation on critical charge distribution," *in Proc. IEEE SOC*, 2006, pp. 243–246.

[88] R. Bishnoi, F. Oboril and M. Tahoori, "Design of Defect and Fault-Tolerant Nonvolatile Spintronic Flip-Flops," in *IEEE Trans. on VLSI*, vol. 25, no. 4, pp. 1421-1432, 2017.

[89] M. Glorieux, S. Clerc, G. Gasiot, J. Autran and P. Roche, "New D-Flip-Flop Design in 65 nm CMOS for Improved SNU and Low Power Overhead at System Level," in *IEEE Trans. Nuclear Science*, vol. 60, no. 6, pp. 4381-4386, 2013.

[90] A. J. Drake, A. K. Osowski, A. K. Martin, "A Self- Correcting Soft Error Tolerant Flop-Flop," in *NASA Symposium on VLSI Design*, Oct. 2005, pp. 4-5.

[91] M. Favalli and C. Metra, "TMR voting in the presence of crosstalk faults at the voter inputs," in *IEEE Trans. on Reliability*, vol. 53, no. 3, pp. 342 – 348, 2004.

[92] L. Sterpone and M. Violante, "Analysis of the robustness of the TMR architecture in SRAM-based FPGAs," in *IEEE Trans. on Nuclear Science*, vol. 52, no. 5, pp. 1545-1549, 2005.

[93] Y. Zhao and S. Dey, "Separate dual-transistor registers: A circuit solution for online testing of transient error in UDSM-IC," in *Proc. IEEE Int. On-line Test Symp.*, 2003, pp. 7-11.

[94] M. Omana, D. Rossi and C. Metra, "Novel Transient Fault Hardened Static Latch," in *Proc. of IEEE Int. Test Conference*, 2003, pp. 886-892.

[95] M. Fazeli, A. Patooghy, S. G. Miremadi, and A. Ejlali, "Feedback redundancy: A power efficient SEU-tolerant latch design for deep sub-micron technologies," in *Proc. IEEE DSN*, Jun. 2007, pp. 276–285.

[96] S. Mitra, M. Zhang, S.Waqas, N. Seifert, B. Gill, and K. S. Kim, "Combinational logic soft error correction," in *Proc. IEEE Int. Test Conf.*, 2006, pp. 1-9.

[97] T. Calin, M. Nicolaids, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," in *IEEE Trans. on Nuclear Science*, vol. 43, no. 6, pp. 2874-2878, 1996.

[98] I. C. Wey, Y. S. Yang, B. C. Wu and C. C. Peng, "A low power-delay-product and robust Isolated-DICE based SEU-tolerant latch circuit design" in *Elsevier Microelectronics Journal*, vol. 45, no.1, pp. 1-13, 2014.

[99] P. Liu, T. Zhao, F. Liang, J. Zhao, and P. Jiang, "A power-delay-product efficient and SEU-tolerant latch design," in *IEICE Electronics Express 14*, no. 23, pp. 20170972-20170972, 2017.

[100] Z. Huang, "A high performance SEU-tolerant latch for nanoscale CMOS technology," in *Proc. IEEE DATE*, 2014, pp 1-5.

[101] H. B. Wang, Y. Q. Li, L. Chen, L. X. Li, R. Liu, S. Baeg, N. Mahatme, B. L. Bhuva, S. J. Wen, R. Wong, and R. Fung, "An SEU-tolerant DICE latch design with feedback transistors," in *IEEE Trans. Nuclear Science*, vol. 62, no. 2, pp. 548–554, 2015.

[102] A. Yan, H. Liang, Z. Huang, C. Jiang, Y. Ouyang and X. Li, "An SEU resilient, SET filterable and cost effective latch in presence of PVT variations," in *Elsevier Microelectronics Reliability*, vol. 63, pp. 239- 250, 2016.

[103] H. Xu, J. Zhu, X. Lu, and J. Li, "An advanced SEU tolerant latch based on error detection," in *Journal of Semiconductors*, vol. 39, no. 5, 2018.

[104] F. S. Alghareb, R. Zand, and R. F. DeMara, "Non-Volatile Spintronic Flip-Flop Design for Energy-Efficient SEU and DNU Resilience," in *IEEE Trans. on Magnetics*, vol. 55, no. 3, pp. 1-11, 2019.

[105] D. R. Blum and J. G. Delgado-Frias, "Hardened by design techniques for implementing multiple-bit upset tolerant static memories," in *IEEE International Symposium on Circuits* and *Systems*, May 2007, pp. 2786-2789.

[106] K. Katsarou and Y. Tsiatouhas, "Soft error interception latch: Double node charge sharing SEU tolerant design," in *IET Electronics Letter*, vol. 51, no. 4, pp. 330–332, 2015.

[107] X. Hui and Z. Yun, "Circuit and layout combination technique to enhance multiple nodes upset tolerance in latches," in *IEICE Electron. Exp.*, vol. 12, no. 9, pp. 1–7, 2015.

[108] A. Watkins and S. Tragouodas, "A highly robust double node upset tolerant latch," in *IEEE DFT*, Sept. 2016, pp. 15–20.

[109] A. Yan, Z. Huang, M. Yi, X. Xu, Y. Ouyang, and H. Liang, "Double-node-upset-resilient latch design for nanoscale CMOS technology," in *IEEE Trans. on VLSI*, vol. 25, no. 6, pp.1978-1982, 2017.

[110] N. Eftaxiopoulos, N. Axelos, and K. Pekmestzi, "DIRT latch: A novel low cost double node upset tolerant latch," in *Elsevier Microelectronics Reliability*, vol. 68, pp. 57-68, 2017.

[111] J. Jiang, Y. Xu, J. Ren, W. Zhu, D. Lin, J. Xiao, W. Kong, W. and S. Zou, "Low-cost single event double-upset tolerant latch design," in *IET Electronics Letters*, vol. 54, no. 9, pp.554-556, 2018.

[112] A. Watkins, and S. Tragoudas, "Radiation Hardened Latch Designs for Double and Triple Node Upsets," in *IEEE Trans. on Emerging Topics in Computing*, in press.

[113] D. Lin, Y. Xu, X. Li, X. Xie, J. Jiang, J. Ren, H. Zhu, Z. Zhang, and S. Zou. "A novel self-recoverable and triple nodes upset resilience DICE latch," in *IEICE Electronics Express 15*, no. 19, pp. 20180753-20180753, 2018.

[114] A. Yan, C. Lai, Y. Zhang, J. Cui, Z. Huang, J. Song, J. Guo, and X. Wen, "Novel Low Cost, Double-and-Triple-Node-Upset-Tolerant Latch Designs for Nano-scale CMOS," in *IEEE Trans. on Emerging Topics in Computing*, in press.

[115] T. Hoang, J. Ross, S. Doyle, D. Rea, E. Chan, W. Neiderer, and A. Bumgarner, "A radiation hardened 16-Mb SRAM for space applications," in *IEEE Aerospace Conference*, Mar. 2007, pp. 1-6.

[116] L. T. Clark, K. C. Mohr, K. E. Holbert, X. Yao, J. Knudsen, and H. Shah, "Optimizing radiation hard by design SRAM cells," in *IEEE Trans. Nuclear Science*, vol. 54, no. 6, pp. 2028-2036, 2007

[117] T. H. Chen, J. Chen, L. T. Clark, J. E. Knudsen, and G. Samson, "Ultra-low power radiation hardened by design memory circuits," in *IEEE Trans. Nuclear Science*, vol. 54, no. 6, pp. 2004-2011, 2007.

[118] A. Stabile, V. Liberali, and C. Calligaro, "Design of a rad-hard library of digital cells for space applications," in *IEEE International Conference on Electronics, Circuits and Systems*, Aug. 2008, pp. 149-152.

[119] E. Do, V. Liberali, A. Stabile, and C. Calligaro, "Layout-oriented simulation of non-destructive single event effects in CMOS IC blocks," in *IEEE European Conference on Radiation and Its Effects on Components and Systems*, Sept. 2009, pp. 217-224.

[120] S. M. Jahinuzzaman, D. J. Rennie, and M. Sachdev, "A soft error tolerant 10T SRAM bit-cell with differential read capability," in *IEEE Trans. Nuclear Science*, vol. 56, no. 6, pp. 3768–3773, 2009.

[121] I. S. Jung, Y. B. Kim, and F. Lombardi, "A novel sort error hardened 10T SRAM cells for low voltage operation," in *Proc. IEEE MWSCAS*, Aug. 2012, pp. 714–717.

[122] M. Shayan, V. Singh, A. D. Singh, and M. Fujita, "SEU tolerant robust memory cell design," in *IEEE IOLTS*, Jun. 2012, pp. 13-18.

[123] C. Qi, L. Xiao, T. Wang, J. Li, and L. Li, "A highly reliable memory cell design combined with layout-level approach to tolerant single-event upsets," in *IEEE Trans. Device Materials Reliability*, vol. 16, no. 3, pp. 388–395, 2016.

[124] L. Atias, A. Teman, R. Giterman, P. Meinerzhagen, and A. Fish, "A low-voltage radiation-hardened 13T SRAM bitcell for ultralow power space applications," in *IEEE Trans. on VLSI*, vol. 24, no. 8, pp. 2622-2633, 2016

[125] J. Guo, L. Zhu, Y. Sun, H. Cao, H. Huang, T. Wang, C. Qi, R. Zhang, X. Cao, L. Xiao, and Z. Mao, "Design of Area-Efficient and Highly Reliable RHBD 10T Memory Cell for Aerospace Applications," in *IEEE Trans. on VLSI*, vol. 26, no.5, pp. 991-994, 2018.

[126] J. Guo, L. Zhu, W. Liu, H. Huang, S. Liu, T. Wang, L. Xiao, and Z. Mao, "Novel radiation-hardened-by-design (RHBD) 12T memory cell for aerospace applications in nanoscale CMOS technology," in *IEEE Trans. on VLSI*, vol. 25, no. 5, pp. 1593–1600, 2017.

[127] D. Lin, Y. Xu, X. Liu, W. Zhu, L. Dai, M. Zhang, X. Li, X. Xie, J, Jiang, H. Zhu, and Z. Zhang, "A novel highly reliable and low-power radiation hardened SRAM bit-cell design," in *IEICE Electronics Express*, vol. 15, no. 3, pp. 20171129-20171129, 2018.

[128] C. Peng, J. Huang, C. Liu, Q. Zhao, S. Xiao, X. Wu, Z. Lin, J. Chen, and X. Zeng, "Radiation-Hardened 14T SRAM Bitcell With Speed and Power Optimized for Space Application," in *IEEE Trans. on VLSI*, vol. 27, no. 2, pp. 407-415, 2019.

[129] A. Sudipta, V. Singh, K. Saluja, and M. Fujita, "SEU tolerant SRAM cell," in *Proc. IEEE ISQED*, Santa Clara, CA, 2011, pp. 1–6.

[130] S. Sarkar, A. Adak, V. Singh, K. Saluja, and M. Fujita. "SEU tolerant SRAM for FPGA applications," in *IEEE International Conference on Field-Programmable Technology*, Beijing, 2010, pp. 491-494.

[131] W. Chen, V. Pouget, G.K. Gentry, H.J. Barnaby, B. Vermeire, B. Bakkaloglu, S. Kiaei, K.E. Holbert, and P. Fouillat, "Radiation hardened by design RF circuits implemented in 0.13 μm CMOS technology," in *IEEE Trans. Nuclear Science*, vol. 53, no. 6, pp. 3449-3454, 2006.

[132] S. Jagtap, R. Sivaramakrishna, and S. Gupta, "Design of Radiation Hardened Wide Tuning Range CMOS Oscillators," in *IEEE ISQED*, Mar. 2014, pp. 224-229 .

[133] S. Jagtap, D. Sharma, and S. Gupta, "Design of SET tolerant LC oscillators using distributed bias circuitry," in *Elsevier Microelectronics Reliability*, vol. 55, no. 9, pp. 1537-1541, 2015.

[134] S. Jagtap, D. Sharma, and S. Gupta, "Design of SET tolerant LC oscillators using distributed bias circuitry," in *European Symposium on Reliability of Electron Devices, Failure Physics and Analysis*, Oct. 2015, pp. 1537-1541.

[135] S. Matakias, Y. Tsiatouhas, A. Arapoyanni, and Th. Haniotakis, "A Circuit for Concurrent Detection of Soft and Timing Errors in Digital CMOS ICs," in *Journal of Electronic Testing: Theory and Applications*, vol. 20, no. 5, pp. 523-531, 2004.

[136] K. K. L. Hsueh, J. L. Sanchez, T. A. Demassa, and L. A. Akers, "Inverse-narrow-width effects and small-geometry MOSFET threshold voltage model," in *IEEE Trans. on Electron Devices*, vol. 35, no. 3, pp. 325-338, March 1988.

[137] ISCAS'89 benchmarks, June. 2018, [online] Available: http://www.pld.ttu.ee/maksim/benchmarks/iscas89/verilog/.

[138] B. Razavi, Design of Analog CMOS Integrated Circuits, New York, NY, USA: McGraw-Hill, 2001.

[139] I. Sutherland, B. Sproull, and D. Harris, Logical Effort: Designing Fast CMOS Circuits. San Mateo, CA, USA: Morgan Kaufmann, 1999.

[140] C. Pacha, B. Martin, K. Arnim, R. Brederlow, D. Landsiedel, P. Seegebrecht , J. Berthold, and R. Thewes, "Impact of STI-induced stress, inverse narrow width effect, and statistical V_{TH} variations on leakage currents in 120 nm CMOS," in *IEEE ESSDERC*, Leuven, Belgium, 2004, pp. 397-400.

[141] L.Xinfu, L. Kheeyong, W. Zhihua, X. Zhibin, D. Yongping, N. Hao, W. Yanping, S. Yanping, T. Bin, L. Louis, C. Sally, Y. Xing, H. Feng, and S. Yang, "A study of inverse

narrow width effect of 65nm low power CMOS technology," in *IEEE ICSICT*, Beijing, 2008, pp.1138-1141.

[142] S. Kim and M. Seok, "Variation-tolerant, ultra-low-voltage microprocessor with a low overhead, within-a-cycle in-situ timing-error detection and correction technique," in *IEEE Journal of Solid-State Circuits*, vol 50, no. 6, pp. 1478-1490, June 2015.

[143] A. Wang, B. H. Calhoun, and A. P. Chandrakasan, Sub-Threshold Design for Ultra Low-Power Systems. New York: Springer, 2006.

[144] R.W. Keyes, "Fundamental limits of silicon technology", in *Proc. of the IEEE*, vol. 89, no. 3, pp. 227–339, Mar. 2001.

[145] A. Sharma, N. Alam, and A. Bulusu, "Effective current model for inverter-transmission gate structure and its application in circuit design," in *IEEE Trans. Electron Devices*, vol. 64, no. 10, pp. 4002-4010, Oct. 2017.

[146] G. R. Srinivasan, P. C. Murley, and H. K. Tang, "Accurate, predictive modeling of soft error rate due to cosmic rays and chip alpha radiation," in *Proc. IEEE Int. Reliab. Phys. Symp.*, San Jose, CA, USA, 1994, pp. 12–16.

[147] Y. Taur, T. H. Ning, "Fundamentals of modern VLSI devices: volume 2," Cambridge University Press Cambridge, 1998.

[148] R. Ramanarayanan, V. Degalahal, N.Vijaykrishnan, M. J. Irwin, and D. Duarte, "Analysis of soft error rate in flip-flops and scannable latches," *IEEE International Systems-on-Chip Conference*, Sept. 2003, pp. 231–234.

[149] S. Lin, Y. B. Kim, and F. Lombardi, "Analysis and design of nanoscale CMOS storage elements for single-event hardening with multiple-node upset," in *IEEE Trans. on Device and Materials Reliability*, vol. 12, no. 1, pp. 68-77, March 2012.

[150] Y. Choi, Y. B. Kim, and F. Lombardi, "Soft error masking latch for sub-threshold voltage operation," in *IEEE MWSCAS*, Boise, ID, 2012, pp. 25-28.

[151] Neil H.E. Weste, and David Harris, "CMOS VLSI design: a circuits and systems perspective," Pearson Education India, 2015.

[152] K. V. Arnim, C. Pacha, K. Hofmann, T. Schulz, K. Schrufer, J. Berthold, "An effective switching current methodology to predict the performance of complex digital circuits," in *IEEE* IEDM, Washington, DC, 2007, pp. 483–486.

[153] P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, and W. Han, "High performance 32nm logic technology featuring 2nd generation high-k+ metal gate transistors," in *IEEE IEDM*, Baltimore, MD, 2009, pp.659-662.

[154] H. Mostafa, M. Anis, and M. Elmasry, "A design-oriented soft error rate variation model accounting for both die-to-die and within-die variations in submicrometer CMOS SRAM cells," in IEEE Trans. on Circuits and Systems I: Regular Papers, vol. 57, no. 6, pp. 1298-1311, June 2010

[155] J. Chen, S. Chen, B. Liang, B. Liu, and F. Liu, "Radiation hardened by design techniques to reduce single event transient pulse width based on the physical mechanism," in *Elsevier Microelectronics Reliability*, vol. 52, no. 6, pp. 1227–1232, June 2012.

[156] J. R. Ahlbin, M. J. Gadlage, N. M. Atkinson, B. Narasimham, B. L. Bhuva, A. F. Witulski, W. T. Holman, P. H. Eaton, and L. W. Massengill, "Effect of multiple-transistor charge collection on single-event transient pulse widths," in *IEEE Trans. Device Materials Reliability*, vol. 11, no. 3, pp. 401–406, Sept. 2011.

[157] V. Sharma, M. Gopal, P. Singh, S. K. Vishvakarma, and S. S. Chouhan "A robust, ultra low-power, data-dependent-power-supplied 11T SRAM cell with expanded read/write stabilities for internet-of-things applications" in *Analog Integrated Circuits and Signal Processing*, vol. 98, no. 2, pp. 331-346, 2019.

PUBLICATIONS

Journal/Transaction Publications

1. **C. I. Kumar** and B. Anand, "A Highly Reliable and Energy Efficient Triple-Node-Upset Tolerant Latch Design", in ***IEEE Transactions on Nuclear Science***, 2019 **(Accepted).**
2. **C. I. Kumar**, I. Bhatia, A. K. Sharma, D. Sehgal, H. S. Jatana, and A. Bulusu, "A Physics-Based Variability-Aware Methodology to Estimate Critical Charge for Near-Threshold Voltage Latches," in ***IEEE Transactions on Very Large Scale Integration Systems***, vol. 27, no. 9, pp. 2170-2179, 2019.
3. **C. I. Kumar**, and B. Anand, "High Performance Energy Efficient Radiation Hardened Latch for Low Voltage Applications", **in *Elsevier Integration: The VLSI Journal,*** vol. 66, pp. 119-127, 2019.
4. **C. I. Kumar**, A. K. Sharma, R. Pratap and B. Anand, "An energy-efficient variation aware self-correcting latch", **in *Elsevier Microelectronics Journal,*** vol. 45, pp. 67-78, 2019.
5. **C. I. Kumar** and B. Anand, "Design of highly reliable energy-efficient SEU tolerant 10T SRAM cell", **in *IET Electronics Letters,*** vol. 54, no. 25, pp.1423-1424, 2018.
6. **C. I. Kumar** and B. Anand, "A Highly Reliable and Energy Efficient Radiation Hardened 12T SRAM Cell Design", in ***IEEE Transactions on Device and Material Reliability***, 2019 (Revision submitted).
7. **C. I. Kumar** and B. Anand, "A Highly Reliable Energy Efficient Double Node Upset Tolerant Latch ", in ***IEEE Transactions on Device and Material Reliability***, 2019 (Under review).

Conference Publications

1. **C. I. Kumar** and B. Anand, "Design and Analysis of Energy Efficient Self Correcting Latches considering Metastability," in *IEEE conference on Ph. D. Research in Microelectronics and Electronics (PRIME), Prague, Czech Republic*, 2018, pp. 101-104.

2. **C. I. Kumar**, A. K. Sharma, S. Miryala, and B. Anand, "A novel energy-efficient self-correcting methodology employing INWE," in *IEEE 13th International Conference on Synthesis Modeling Analysis and Circuit Design, Lisbon*, 2016, pp. 1-4.