CHARACTERIZATION AND MITIGATION OF LINEAR AND NON-LINEAR DISTORTIONS IN SIX-PORT MODULATORS

by

CHETAN PATHAK

Submitted in partial fulfillment of

the requirements of the degree of

Doctor of Philosophy

to the

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

ENGINEERINGINDIAN INSTITUTE OF

TECHNOLOGY,ROORKEE

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Certificate

This is to certify that the thesis entitled, **"Characterization & Mitigation of Linear & Non-linear Distortions in Six-Port Modulator",** being submitted by **Chetan Pathak** for the award of the degree of **Doctor of Philosophy** to the Department of Electronics and Communication Engineering, Indian Institute of Technology, Roorkee is a record of bonafide research work carried out by hisunder our guidance and supervision.

Chetan Pathak has fulfilled the requirements for the submission of this thesis, which to our knowledge has reached the requisite standard. The results contained in this thesis have not been submitted in part or in full to any other university or institute for the award of any degree or diploma.

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Chetan Pathak

Abstract

There is an increasing demand of lowering the complexity and power consumption in the design of the wireless terminals. Further, wideband, compact size, and low-cost digital transceivers are required to meet the demands of upcoming mobile and wireless communications. With the advent of 5G wireless communication, the expected data rate is going to exceed to an order of Gbps. This is possible with high spectral efficient modulation scheme or multiplexing techniques, where, maximum data can be transmitted within limited bandwidth. These schemes such as higher order quadrature amplitude modulation and orthogonal frequency division multiplexing result into envelope varying signals with high crest factor; which generates several linear and non-linear distortions in radio frequency modulators. The crest factor of any envelope varying signal is defined as the ratio of peak amplitude divided by r.m.s value of the signal. Moreover, the bandwidth requirement is still high to handle high data rate expected for 5G communication. Therefore, based on the availability of spectrum and the spectral efficiency of modulation scheme, both sub-6 GHz band and millimetre-wave band are recently opened for 5G communication. The power amplifiers an inevitable component of radio frequency chain which produces most of the distortion in transmitter. Therefore, one must restrict preceding stages such as RF modulator to add any distortion which may be further amplified with the PA. The conventional quadrature modulator uses mixers which are inherently non-linear components and can generate non-linear distortion. This will further reduce spectral efficiency. However, six-port reflectometer based modulator which does not use mixer is inherently linear and can be a good choice for upcoming wireless

transmitters, where, spectral efficiency requirement is quite high. Moreover, the architecture of Six-Port Modulator is simple which uses conventional passive components and schottky diodes and therefore, can easily be scaled to millimetre wave frequency. Although, these modulators are inherently linear in practice, there are several linear and non-linear distortions which appear in case of envelope varying signals with high crest factor. This thesis presents an experimental methodology to characterize these distortions using an instrument based test-bed. A hardware prototype of six-port modulator was developed to modulate in-phase (*I*) and quadrature-phase (*Q*) components of baseband signal to RF carrier of 2 GHz. Later, appropriate digital pre-compensation schemes are implemented to mitigate the distortions generated in SPM. With the implementation of proposed scheme, the SPM hardware prototype presents an excellent performance in terms of reduced error vector magnitude and adjacent channel leakage ratio.

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List of Abbreviations

Abbreviations	Definition
ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADS	Advanced Design System
ATC	American Technical Ceramics
BLC	Branch Line Coupler
BPSK	Binary Phase Shift Keying
CAD	Computer Aided design
DAC	Digital to Analog Converter
DC	Direct Current
DPD	Digital Predistortion
DSP	Digital Signal Processing
EM	Electromagnetic
EVM	Error Vector Magnitude
FPGA	Field Programmable Gate Array
GPIB	General Purpose Interfacing Bus
HCs	Hybrid Couplers
ILA	Indirect Learning Architecture
IF	Intermediate Frequency
LTE	Long Term Evolution
LO	Local Oscillator

NMSE	Normalized Mean Square Error
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PCB	Printed Circuit Board
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QIMP	Quadrature-Interface Memory Polynomial
QPSK	Quadrature Phase Shift Keying
QRQIMP	Quasi Recursive Quadrature - Interface Memory Polynomial
RMS	Root Mean Square
RF	Radio Frequency
SPC	Six-Port Correlator
SPM	Six-Port Modulator
VNA	Vector Network Analyzer
VSA	Vector Signal Analyzer
VSG	Vector Signal Generator
WPD	Wilkinson Power Divider

Chapter One: INTRODUCTION

1.1 **Motivation**

The radio frequency (RF) six-port network which was originally proposed as reflectometer, now finds several applications including modulators, demodulators, network analyzers as well as beam forming and direction-finding network [1]-[85]. In each application, six-port network is comprised of passive six-port correlator (SPC) and loads terminating the SPC. The passive SPC correlates the reflected waves from its multiple ports to provide various applications. RF quadrature modulator is one such application which is an important element of wireless transmitter in modern wireless communication. This plays an important role in modulating baseband data in the form of in-phase (*I*) and quadrature phase (*Q*) components. The conventional quadrature modulator is based on mixers and quadrature hybrid couplers (HCs) [22],[51]. There is an alternative architecture based on six-port network which was proposed as modulator for wireless transmission [17],[21]-[22],[24]-[26],[28]-[36],[38]-[43].In case of six-port based modulator, the four out of six ports of SPC are terminated by either variable loads realized using schottky diodes or switches [17]-[35]. The SPC is realized using three HCs and one wilkinson power divider (WPD) as presented in [17]-[35], [46]-[47], [55]. Due to its simplified structure, low-cost and low power consumption feature along with passive nature, six-port modulator (SPM) is a good candidate for high frequency applications. For example, the passive SPC can be easily scaled to millimeter wave (mm-wave)

frequencies making SPM a potential candidate for 5G applications [66]-[72].The schottky diode based architecture [17]-[20],[24]-[26],[28]-[32] can modulate high speed data and handle higher order quadrature amplitude modulation (QAM) with reduced complexity as compared to PIN diode or switch based architecture [21]-[22],[34],[65].However, the non-linearity of schottky diodes limits the performance of the modulator. This limitation is more visible in the case of high crest factor signals such as high order QAM. The crest factor of any envelope varying signal is defined as the ratio of peak amplitude and root mean square (RMS) value of the signal. In addition, the SPC is comprised of low-cost passive printed circuit board (PCB) components and their s-parameter performance can easily deviate from ideal values while implementing SPC. This is perhaps due to losses as well as imperfect realization of phase shifts by transmission line components. The error in the SPC realization results into linear distortion, which, along with non-linear distortion, can severely affect the performance of six-port modulator (SPM). Therefore, a suitable digital correction scheme is required to correct these distortions. This is important in order to qualify spectral mask and error vector magnitude (EVM) specifications for latest wireless standards.

This thesis presents identification and characterization of linear and non-linear distortions along with their sources in SPM. A suitable digital correction scheme is proposed to correct for the hardware impairments resulting into various distortions in SPM.

1.2 **Background and Existing Methodologies**

As discussed in previous section, the topologies of SPMs are broadly classified under two categories. One, utilizing switchable load configuration, whereas the other operating on variable load configuration. Figure 1.1 shows the generic topology for switchable load configuration, where, a switching matrix is used to choose among various loads for terminating four different ports of SPC.

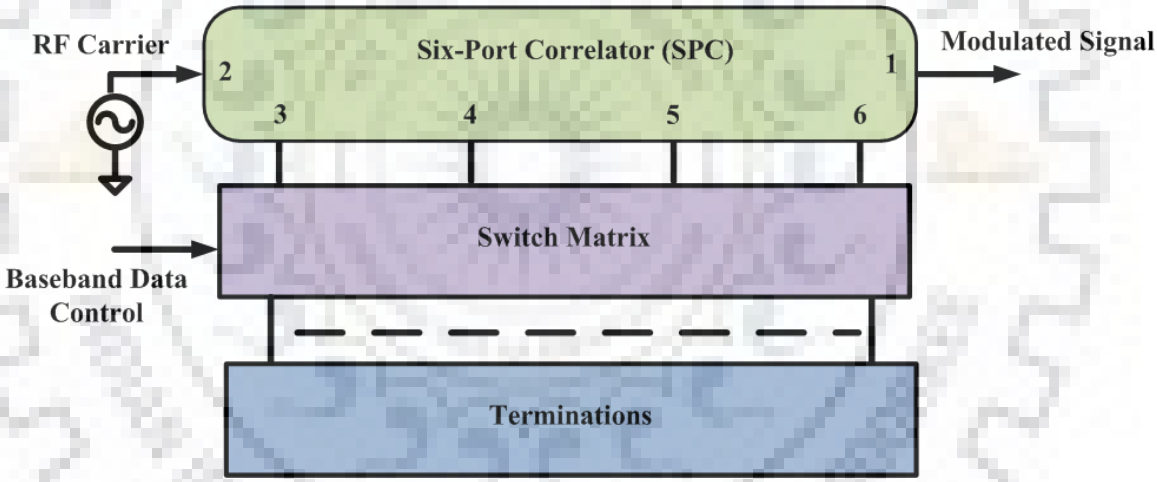

Figure 1.1: Architecture of SPM using switchable loads.

The selections of different loads are therefore controlled by switches available in switch matrix and the switching action is controlled by baseband data which is being modulated. The other two ports of six-port network are used for injection of RF carrier and obtaining modulated RF carrier as an output as shown in Figure1.1.The implementations of this topology are given in [21]-[22],[33]-[39], [46], [50],[52]-

[53],[58],[83]. Most of these earlier works demonstrate the performance with hardware prototype of SPM using various switching configurations. The [83] presents two different configurations of switching based SPM. The primary difference is in terms of SPC topology, where, parallel modulator configuration uses two quadrature HCs connected in parallel [83]. The same topology has been used in several SPM based on switched loads as well as variable loads [17]-[20],[24]-[26],[28]-[32]. Figure 1.2 shows the most common topology of SPC widely used in literature.

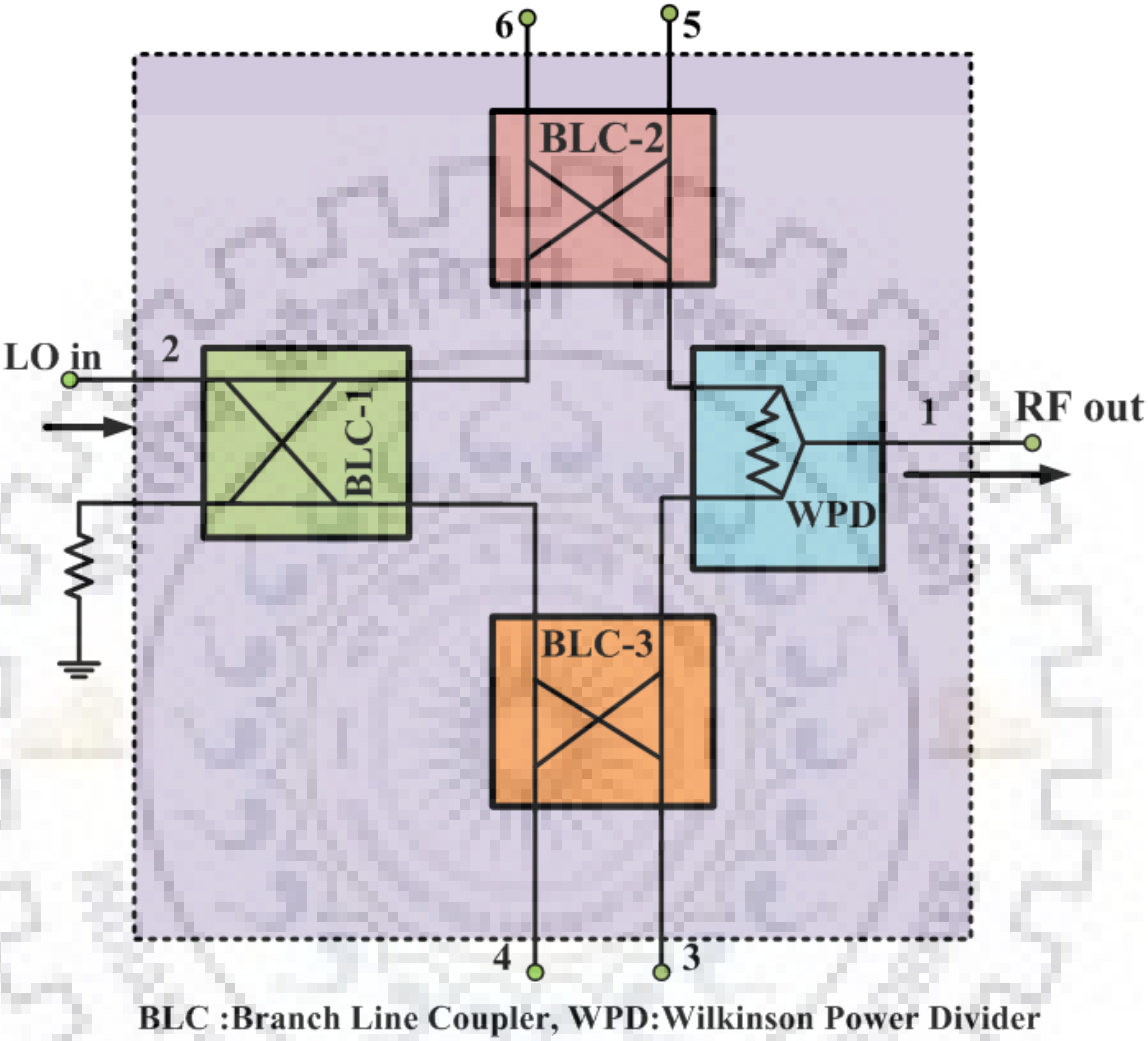

Figure 1.2: Topology of SPC widely used in literature.

This topology comprises of three quadrature HCs realized using branch line couplers (BLCs), where, two of them are connected in parallel. In case of SPM architecture as presented in [17]-[20],[24]-[26],[28]-[32], the RF carrier is applied to port 2 using BLC-1. The modulated output is available at port 1, which is internally connected to the combiner port of Wilkinson power divider (WPD) as shown in Fig. 1.2. The ports 3-6 are

used for connecting loads (switched or variable) based on the architecture of SPM.

The series configuration comprises of two BLCs connected in series [83]. The parallel modulator has better bit error probability with low conversion efficiency as compared to the serial modulator [83]. The conversion efficiency of series modulator drops fast as compared to the efficiency of parallel modulator with change in load [83].

Different configurations of SPCs are presented to scale the frequency of operation to mm-wave in case of SPM [37],[39]-[41]. The quadrature phase shift keying (QPSK) modulation is demonstrated at 62 GHz and 86 GHz for different data rates such as 100 Mbps, 500 Mbps and 1 Gbps [40]. The [37] demonstrates 16-phase shift keying (PSK) modulation at 77 GHz with 500 Mbps data rate. In addition, [34] and [42] present frequency scalability of most common SPC as shown in Fig. 1.2, where, QPSK modulation is demonstrated. The [34] demonstrates QPSK modulation at data rate of 250 Mega-baud/sec at 24 GHz. whereas, [42] demonstrates QPSK modulation at data rate of 120 Mega-baud/sec at 19 GHz. The [51] presents an SPC architecture comprising of WPD only.

The [21] presents hardware prototype capable of 16 QAM modulation upto 200 Mbps data rate at RF carrier frequency of 4.2 GHz. The modulation is performed with an EVM of 6.99%. A direct QPSK modulation is demonstrated with similar data rate in hardware at RF carrier frequency of 4.0 GHz in [22]. Similarly, [80] demonstrates hardware for QPSK modulation at 5 Mbps, 10 Mbps and 15 Mbps data rates over RF carrier frequency of 2.4 GHz.

Anultra-wideband performance of SPM is presented in [36]. The work presents

QPSK modulation at 400 Mega-Symbol/s across octave RF carrier frequency range from 4.5 GHz to 9 GHz. The [36] also analyzes various configurations of SPC to get performance over wide range of frequency. Similarly, [50] utilizes microstrip slot technique in conventional SPC architecture as shown in Figure 1.2 to enhance the bandwidth. In such case QPSK based modulation is performed over the frequency range from 4.5 GHz to 10.6 GHz [50]. The [52] uses broadside couplers in SPC configuration to achieve wide bandwidth. The binary phase shift keying (BPSK) modulation with 4Gbps data rate is demonstrated at 60 GHz using the SPM based transmitter in [52].

The [30] presents SPM hardware capable of modulating baseband data to 64 QAM with EVM of 7-7.5% at RF carrier frequency of 2.475 GHz. A higher order modulation such as 256-QAM is also demonstrated in [46], [29] at data rate of 50 M symbol/s, however, no EVM performance is reported.

Figure 1.3 shows the other topology of SPM based on variable loads. This topology utilizes the voltage controlled loads connected to four ports of SPC. The other two ports are used for injecting RF carrier frequency and modulated output as shown in Figure 1.3.Unlike the switching load configuration, there is no requirement of any switching matrix or mechanism and a direct output of digital-to- analog converter (DAC)

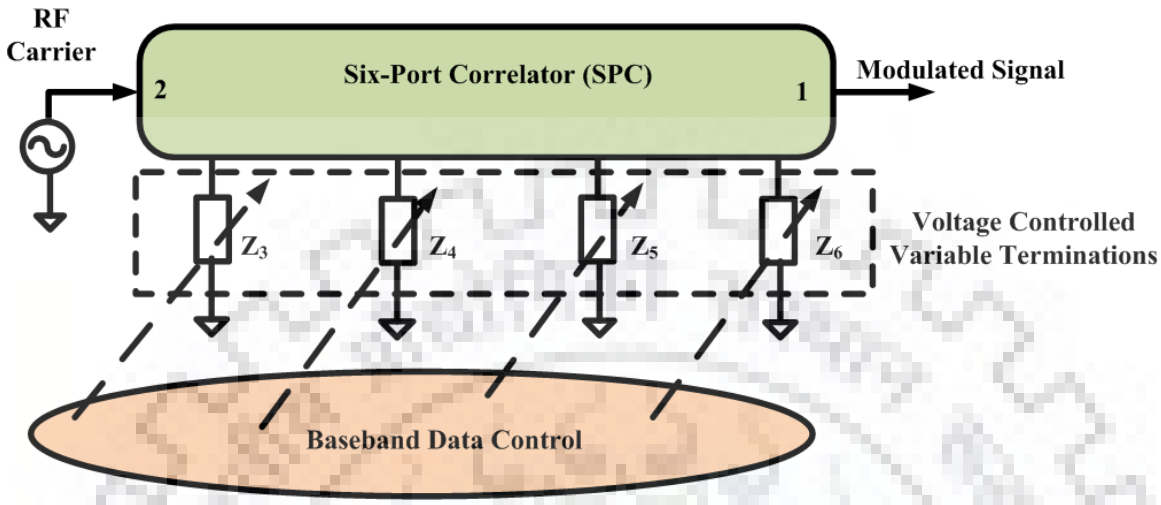

Figure 1.3: Architecture of SPM using voltage variable loads.

can drive the voltage controlling the load impedances. The common strategy is to use schottky diodes, where, the impedance presented by the diode depends on bias voltage [24]-[26], [28]-[32], [47], [53], [55], the bias voltages of these diodes can be varied as per baseband signals obtained after DAC. The performance of this configuration is severely limited due to non-linearity of diode. The diode impedance varies non-linearly with the bias voltage, limiting the dynamic range of this type of SPM [28], [29], [32], [55]. Moreover, this non-linearity further exemplify due to hardware imperfections in passive SPC. Therefore, for higher order QAM modulation, the performance in terms of EVM is severely limited [24]-[26], [28]-[32], [47], [53], [55]. However, due to availability of digital access, a suitable pre-compensation technique can be implemented for correcting this non-linear effect as well as compensating for the hardware imperfections in SPC.

Apart from these generic configurations as shown in Figure 1.1 and Figure 1.2,

the polyphase networks along with power dividers/combiners are also used in implementing SPM [65]. This modulator demonstrates QPSK modulation with 3% EVM with data rate upto 20 Mbps.

1.3 **Problem Statements and Targeted Goals**

Problem Statement #1

The switchable architecture of SPM utilizes complex switching matrix to realize high order QAM. In such case most of the work in literature are focused on QPSK and 16 QAM modulationsas discussed in previous section. The variable load architecture however is comparatively simple and can be used for handling higher order QAM. However this scheme has limitations in terms of diode non-linearity which is being used as variable loads. The diode non-linearity restricts the dynamic range as well as further deteriorates the effect of hardware imperfection over successful modulation in this architecture. This problem must be mitigated in order to use the variable load architecture of SPM for handling the higher order QAM.[28], [30], [32], [55].

Targeted Goal #1

In order to compensate for non-linearity introduced by the diodes and linear distortions introduced by passive SPC, a nonlinear characterization setup is required to characterize these distortions in SPM. This setup should be capable of capturing linear and non-linear distortions in SPM. In addition, the setup should be able to generate in-

phase (*I*) and quadrature phase (*Q*) data corresponding to the baseband signal which will control the variable loads terminating the ports of SPC. The schottky diodes can be used for implementing variable loads.

Problem Statement #2

In the case, where, schottky diodes are used as variable loads in SPM, the performance is restricted due to the non-linearity introduced by the diode. In addition, any hardware imperfection in passive SPC will further enhance the effect of this non-linear distortion. Therefore, an appropriate compensation is required to obtain required performance in terms of EVM.

Targeted Goal #2

The non-linear characterization scheme as discussed in problem statement 1 provides access to the digital baseband signals. This will give an opportunity to apply digital predistortion (DPD) to compensate for the linear and non-linear distortions in the SPM due to hardware imperfection in SPC as well as diode non-linearity. A suitable algorithm will be identified for developing behavioral model for SPM. Later, an inverse model will be developed to apply DPD for compensating distortions in SPM.

Problem Statement #3

The DPD scheme proposed for compensating distortions in SPM may not always be feasible to be applied in digital signal processing (DSP) / field programmable gate array (FPGA) platform. In such case, low complexity models are required for modelling and DPD application in SPM.

Targeted Goal #3

The target is to search for new low complexity model which can be easily implemented in DSP/FPGA platform with low resource consumption.

1.4 Scope and Objective of Work

The overall aim of the research in this thesis is to propose digitally assisted SPM which can modulate modern wireless communication signals with minimum distortion. The thesis primarily targets three key objectives, where the summary of work under these objectives are listed as follows:

1. Development of Hardware prototype & characterization test-bed for digital base-band signal generation and modulation with digital correction.
    - A SPM modulator is developed with passive SPC designed at 2 GHz. The schottky diode HSMS2820 by Broadcom technologies is used as variable load.

- An instrument based test-bed is developed to generate baseband data and modulate it using SPM. This comprises of vector signal generator (VSG) by Keysight (model no. MXG N5182B), which play-back the baseband *I* and *Q* data stored in its memory. The differential DAC outputs at the rear panel of VSG provide the analog signals corresponding to the *I* and *Q* data which is modulated by the SPM hardware. The vector signal analyzer (VSA) by Keysight (model no. MXA N9020B) is used to capture modulated RF carrier and extract corresponding baseband *I* and *Q* data. This output *I* and *Q* data is compared with input baseband *I* and *Q* data originally sent to VSG to retrieve gain and phase characteristic of SPM. These gain and phase characteristics are then used for behavioural modelling and DPD application.

2. Characterization of Linear and Non-linear distortion of SPM & digital pre-compensation.
    - The imperfections in SPM are characterized using instrument test-bed developed under objective 1.
    - A behavioural modelling of linear and non-linear distortions is performed based on neural network.
    - A DPD scheme is implemented to pre-compensate and mitigate these distortions.
3. Low-complexity solution for Linear and Non-linear distortion mitigation in SPM.

- A polynomial based low-complexity model is proposed which will be implemented digitally using less resources as compared to Neural Network based model.
- The model is used to apply DPD for distortion mitigation in SPM.
- The SPM is tested with high order QAM signals as well as orthogonal frequency division multiplexing (OFDM) signals complying long term evolution (LTE) standard.

1.5 **Thesis Outline**

The thesis is organised into five chapters including introduction and conclusion. The following discussion presents the content of each chapter in brief.

The first chapter states the literature review on SPM and their performance. Various configurations based on switching or variable loads are discussed including their advantages and disadvantages. The configurations using transistors or diodes realizing the variable loads are also discussed in this chapter. The chapter also discusses the problem statements and targeted goals. The objectives of the thesis are also presented in this chapter based on these problem statements. This chapter also summarizes the contribution as well as thesis organisation.

Second chapter discusses the design of SPM using passive SPC and schottky diode as variable loads. A hardware prototype is developed using RO4350B substrate with dielectric constant of 3.66, height of 20 mil and loss tangent of 0.0037. The schottky

diode HSMS2820 by Broadcom technologies is used as variable load. The hardware prototype is designed to operate at centre frequency of 2 GHz. An instrument based test-bed is also developed which can provide baseband *I* and *Q* data to the SPM for modulation of RF carrier frequency at 2 GHz. These basebands *I* and *Q* data correspond to digital modulation such as QAM which is generated in MATLB and later uploaded to the memory of VSG (Keysight MXG N5182B). The DACs inside VSG convert these baseband *I* and *Q* data to analog signals which are available in differential form at the rear panel of VSG. The SPM modulates the RF carrier with respect to these signals. Similarly, the test-bed also has VSA which captures the modulated RF carrier and saves the *I* and *Q* baseband data modulating the RF carrier. These baseband *I* and *Q* data are then used generate behavioural model of SPM so that DPD can be applied to compensate for the distortions.

The third chapter focuses on the identifying the linear and non-linear distortion components and their sources in SPM. The hardware imperfections in SPC primarily contributes to linear distortions which further add-up to the nonlinear distortions produced by the diodes. A behavioural model is developed based on real-valued focused time delay neural network to model these linear and non-linear distortions. The SPM is characterized in terms of gain and phase distortions which are captured from the test-bed developed in chapter 2. Later these distortions are modelled and inverse of this model is applied in digital domain. The *I* and *Q* baseband data when passes through this model get pre-distorted such that after modulation from SPM the output of SPM is effectively distortion free. This digital pre-compensation technique is validated with the modulation

of QAM and LTE signals and the modulated signals qualify the requirements of LTE standard in terms of EVM and adjacent channel leakage ratio (ACLR).

The fourth chapter presents low-complexity quadrature interference memory polynomial (QIMP) Model and its variant. This model has better performance as compared to the state-of-art polynomial based models. In comparison to neural network based behavioural modelling of chapter 3, this model offers low resource consumption in terms of signal processing. The performance of the model is validated in hardware prototype and test-bed developed in chapter 2. The QAM as well as the LTE signals are modulated using the SPM after applying the digital predistorters based on the proposed model. The EVM and ACLR are well below the required range as specified by the standards.

The fifth chapter concludes the thesis by summarizing the research outcomes against various objectives defined in chapter 1. The chapter also discusses future work related to the thesis.

1.6 **Summary of Contributions**

Journal Publication:

[1] C. Pathak, K. Rawat, “Nonlinear Characterization & Distortion Mitigation in Six-Port Modulator", *IEEE Transactions on Instrumentation and Measurement*, vol.68,no.4,pp.1178-1188,Apr.2019

[2] C. Pathak, K. Rawat, “Characterization and Modelling of Hardware Imperfections in Schottky Diode Based Six-Port Modulator", *Wiley International Journal of RF and Microwave Computer-Aided Engineering*,vol.29,no.6, pp.1-10,Jun.2019

Conference Proceedings:

[3] C. Pathak, K. Rawat, “Quadrature modulation using radio frequency wave correlation in multiport network,” 5th IEEE International Conference on Signal Processing and Integrated Networks (SPIN), New Delhi, India, Feb 2018, pp.1-3.

Chapter Two: Six-Port Modulator Design and Development of Its Characterization Test-Bed

2.1 **Introduction**

This chapter discusses the architecture of SPM based on the architecture shown in Fig. 1.3. The modulation performed by the presented architecture is also discussed along with assumptions that will lead to ideal operation in terms of modulation. Later, a hardware prototype is developed based on this architecture to modulate the signals at RF carrier frequency of 2 GHz. The performance of this hardware prototype is validated in terms of s-parameters in simulation as well as measurement. The chapter also presents an instrument based test-bed developed to characterize and measure the performance of SPM hardware prototype in terms of LTE signals using 64-QAM modulation.

2.2 **Six-Port Modulator Architecture and Operation**

The modulator architecture based on multiport network. This comprises of passive multi-port wave correlator which correlates and combines the reflected wave from its various ports. SPM comprises of passive SPC with its four ports terminated with high speed variable impedances schottky diodes [17]-[20],[24]-[26],[28]-[32],[55]. The SPC combines these waves reflected from the ports terminated by these schottky diodes. Figure 2.1 shows the architecture of SPM, where, the RF carrier signal of frequency f_c is

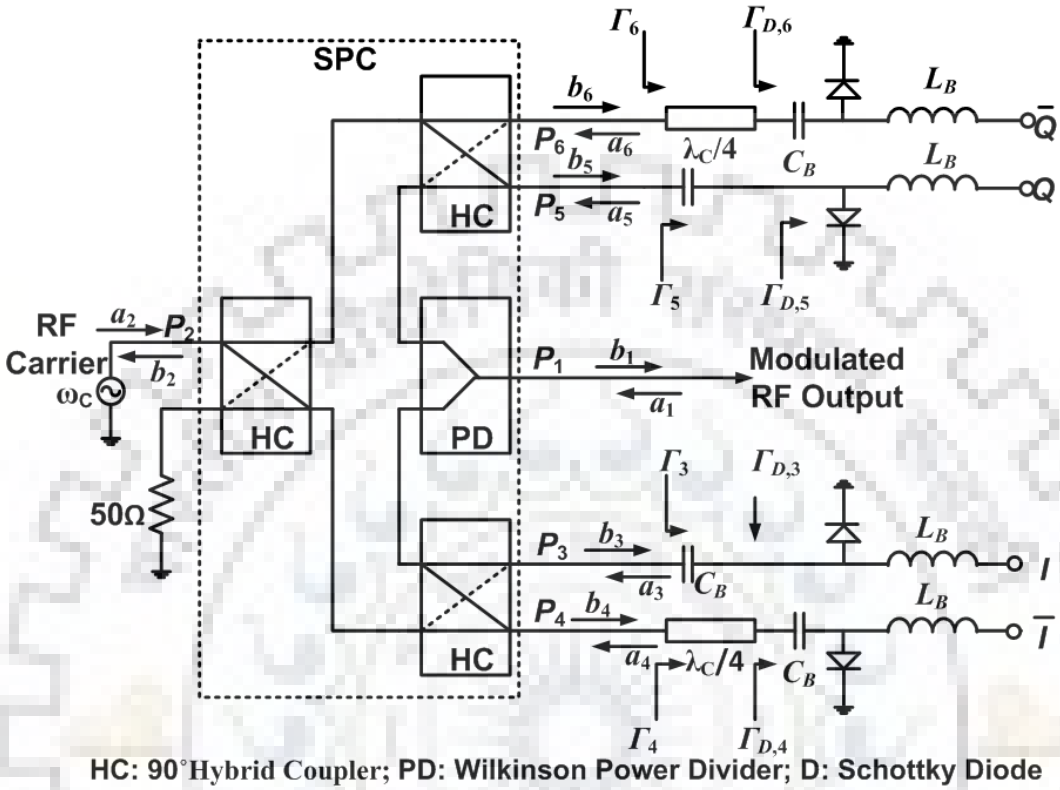

Figure 2.1: Architecture of SPM with SPC, diodes, and biasing circuits.

fed from port P_2, which is reflected from ports P_3 to P_6 with reflection coefficients Γ_3 to Γ_6. Ports P_3 to P_6 are terminated using schottky diodes with quarter-wave transmission lines and their bias circuitry is shown in Figure 2.1.

SPC combines these reflected waves using its s-parameter matrix and gives output modulated signal at Port 1. The reflection coefficients Γ_3, Γ_4, Γ_5 and Γ_6 depend on diodes reflection coefficients $\Gamma_{D,3}$, $\Gamma_{D,4}$, $\Gamma_{D,5}$ and $\Gamma_{D,6}$ which varies with the control signals $I = -\bar{I}, Q = -\bar{Q}$ as shown in Figure 2.1. These control signals can be *I*, *Q* of any digital

modulation schemes such as QAM produced after DAC conversion. In such case, the baseband information is modulates the RF carrier by changing reflection coefficients of the diodes according to *I* and *Q* data. The quarter-wave transmission lines of length $\lambda_C/4$ and the injection of *I* and *Q* in differential form helps in carrier leakage suppression at output port P_1 which is described in [24]-[26],[28]-[32],[55]. The diodes are biased by the baseband inputs as common-mode signal and the bias circuitry comprises of RF chokes L_B and blocking capacitors C_B as shown in Figure 2.1. The RF chokes L_B blocks the leakage of RF carrier to the baseband input side from where baseband data and direct current (DC) bias is injected. The blocking capacitors C_B in Figure 2.1 blocks DC bias to leak towards RF path connecting to passive SPC.

The s-parameter matrix of SPC is given in (2.1).

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \\ b_5 \\ b_6 \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 0 & 0 & -1 & j & -1 & j \\ 0 & 0 & 1 & j & j & -1 \\ -1 & 1 & 0 & 0 & 0 & 0 \\ j & j & 0 & 0 & 0 & 0 \\ -1 & j & 0 & 0 & 0 & 0 \\ j & -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ a_5 \\ a_6 \end{bmatrix} \tag{2.1}$$

The output signal b_1 at port P_1 in Figure 2.1 is the function of incident RF carrier signal a_2, its reflected components from various ports and s-parameters of passive SPC. Assuming L_B and C_B as ideal components, the modulated RF carrier at port P_1 is given in (2.2).

$$b_1 = a_2 \sum_{m=3}^{6} S_{m2}\Gamma_m S_{1m} \qquad (2.2)$$
$$a_2\left(S_{32}\Gamma_3 S_{13}+S_{42}\Gamma_4 S_{14}+S_{52}\Gamma_5 S_{15}+S_{62}\Gamma_6 S_{16}\right)$$

where, b_1 is modulated carrier output from port P_1 and S_{m2} is the s-parameter defined as ratio of voltage wave measured at m^{th} port and the voltage wave incident at port P_2, when all the other ports are terminated with matched loads. Similarly, S_{1m} is the s-parameter between port P_1 and m^{th} port, which is obtained as the ratio of voltage wave measured at Port P_1 and the voltage wave incident at m^{th} Port, with all the ports terminated with matched loads. Γ_m is the reflection coefficient at m^{th} port of SPC. Using the s-parameter matrix of ideal SPC as given in (2.1), one can write,

$$b_1 = -\frac{a_2}{4}\left[\left(\Gamma_3+\Gamma_4\right)+j\left(\Gamma_5+\Gamma_6\right)\right] \qquad (2.3)$$

Thus, modulated carrier b_1 depends upon reflection coefficients Γ_3,Γ_4,Γ_5 and Γ_6. In order to obtain b_1 as modulated carrier, Γ_3 and Γ_4 should replace baseband component *I*. Similarly, Γ_5 and Γ_6 should be function of input baseband component *Q*. This is possible since reflection coefficient Γ_m, at m^{th} port where, m=3,4,5,6 depends on diode reflection coefficient, which can vary with *I* and *Q* signals provided as control voltages of schottky

diodes. Expanding the reflection coefficient by Taylor series at the DC bias voltage V_{CM} of the diode, one can obtain

$$\Gamma_{D,m}(V) = \Gamma_{D,m}(V_{CM}) + k_0(V - V_{CM}) + k_1(V - V_{CM})^2 + ... + k_{n-1}(V - V_{CM})^{n-1} \quad (2.4)$$

where,

$$k_{n-1} = \frac{1}{n!}\Gamma_{D,m}^{(n)}(V_{CM}) = \frac{1}{n!}\frac{\partial^n \Gamma_{D,m}(V)}{\partial V^n}\bigg|_{V=V_{CM}} ; n = 1, 2, ... \quad (2.5)$$

Assuming diode operation is restricted to linear region only, one can truncate (2.5) to first order term

$$\Gamma_{D,m}(V) \approx \Gamma_{D,m}(V_{CM}) + k(V - V_{CM}) = \Gamma_0 + k_0 \Delta v \quad (2.6)$$

where, m represents port numbers 3 to 6 of SPC which are connected to diodes. $\Gamma_{D,m}$ (V_{CM}) or Γ_0 is the reflection coefficient due to common mode voltage applied to each diode such as DC bias. Parameter k_0 governs the rate of change of reflection coefficient Γ with change in voltage. If the reflection coefficient as described in (2.4) is controlled by the baseband I and Q data which is in voltage form, then using (2.6) in (2.3), results into carrier signal b_1 modulated with I and Q data. However, the component Γ_0 of reflection

coefficient will reflect carrier only and hence produce carrier leakage in addition to the modulated signal. To avoid the carrier leakage at port 1, the *I* and *Q* data are applied in differential form along with quarter wave transmission line of length $\lambda_c/4$ between diodes and ports of SPC as shown in Figure 2.1.These transmission lines give 180˚ phase shifts to the reflection coefficients $\Gamma_{D,4}(V)$ and $\Gamma_{D,6}(V)$. The diode reflection coefficients $\Gamma_{D,m}(V)$ and the reflection coefficients at SPC ports as shown in Figure 2.1are related as:

$$\Gamma_3(V) = \Gamma_{D,3}(V) = \Gamma_0 + k_0 I \tag{2.7}$$

$$\Gamma_5(V) = \Gamma_{D,5}(V) = \Gamma_0 + k_0 Q \tag{2.8}$$

$$\Gamma_4(V) = e^{-j\pi}\Gamma_{D,4}(V) = -\Gamma_{D,4}(V) = -\Gamma_0 - k_0 \bar{I} \tag{2.9}$$

$$\Gamma_6(V) = e^{-j\pi}\Gamma_{D,6}(V) = -\Gamma_{D,6}(V) = -\Gamma_0 - k_0 \bar{Q} \tag{2.10}$$

where, factor $e^{-j\pi}$ appears in (2.9) and (2.10) due to quarter wave transmission line of length $\lambda_c/4$ as shown in Figure 2.1. Using (2.7) - (2.10) in (2.4), one can write

$$b_1 = -\frac{a_2}{4}\left[\left(\Gamma_0 + k.I\right) + \left(-\Gamma_0 - k.\bar{I}\right) + j\left\{\left(\Gamma_0 + k.Q\right) + \left(-\Gamma_0 - k.\bar{Q}\right)\right\}\right] \tag{2.11}$$

If $\bar{I}$ and $\bar{Q}$ represents inverted replica of baseband *I* and *Q* signals i.e. *I*= -$\bar{I}$, *Q*= -$\bar{Q}$, one can write (2.11) as:

$$b_1 = -\frac{|a_2|k}{2}\left[I + jQ\right]e^{j\omega_C t} \tag{2.12}$$

Therefore, differential *I* and *Q*, along with quarter-wave transmission line, remove the component Γ_0 which would have contributed for carrier leakage at output if not cancelled [24],[26],[65]. Equation (2.12) represents successful modulation with following assumptions:

1. The diodes reflection coefficient should change symmetrically around Γ_0 as described in (2.7)-(2.10).

2. The diodes reflection coefficient should be linear function of control voltages as described in (2.7)-(2.10).

3. $\bar{I}$ and $\bar{Q}$ should be inverted replica of baseband *I* and *Q* signals,

4. The s-parameters of SPC hardware should be same as s-parameters of ideal SPC, as shown in Figure 2.1.

Any deviation from the above four assumptions will result into poor performance of SPM and hence produce distortions in the output. The distortions occurring due to non-ideal s-parameters and errors in relation between $I, \bar{I}, Q, \bar{Q}$ are linear distortions. The non-linear relation between reflection coefficient of diode and its baseband control voltage will result into non-linear distortion. This also disturbs the first assumption, and

the reflection coefficient variation will be no more symmetric around Γ_0 resulting into carrier leakage. No matter, how carefully the design is developed and simulated; some of these imperfections are inevitable. These imperfections are due to fabrication errors, use of low cost components, inaccurate diode models and non-ideal paths between DACs and SPM. Therefore, one must use digital corrections with SPM to obtain up-to mark performance. Fortunately, the SPM is directly connected to the baseband unit. Therefore, it is feasible to implement a system which can characterize the imperfections and apply suitable correction algorithm for accurate modulation. Following sections describe a hardware prototype developed based on the architecture of Figure 2.1. Later, an instrument based test-bed is described which is capable of capturing the linear and non-linear distortions and applying appropriate digital corrections to digital-baseband *I*, *Q* signals for compensating distortions.

2.3 **Hardware Prototype Implementation of Six-Port Modulator**

Based on the architecture of Figure 2.1, a hardware prototype is fabricated on Rogers RO4350B substrate. The Rogers RO4350 substrate has dielectric constant 3.66, height of 20 mil and loss tangent of 0.0037. Figure 2.2 shows the photograph of the hardware prototype which uses schottky diode HSMS2820 by Broadcom technologies as variable load. The diode has nominal junction capacitance C_{j0}=0.649pF and saturation current I_s=0.48nA. Table 2.2 shows the spice parameters of the diode. The diode is biased using an inductor realized by a transmission line terminated with butterfly stubs as shown in

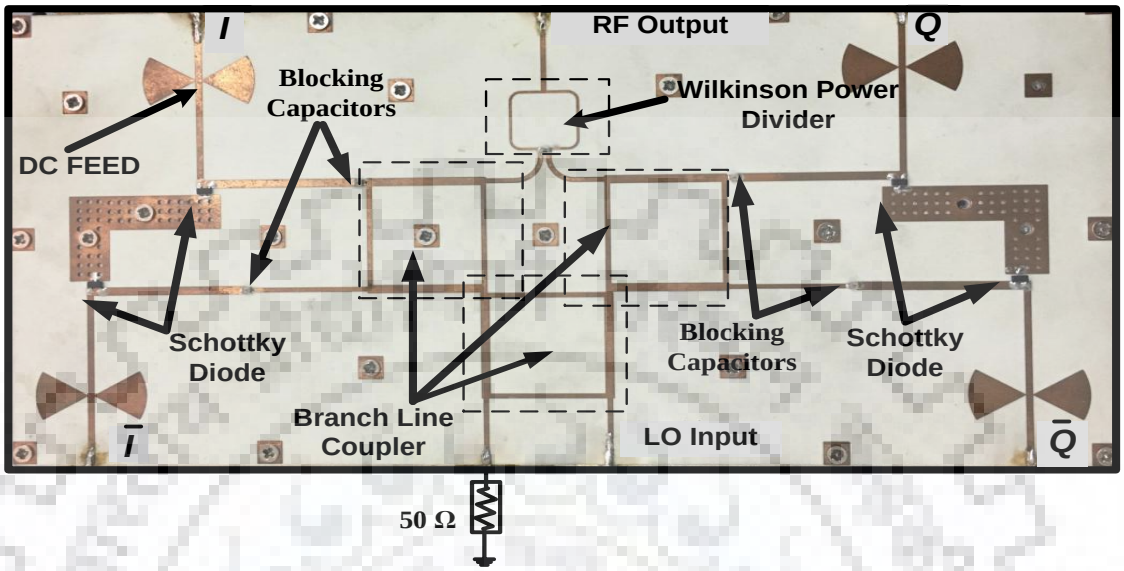

Figure 2.2: Photograph of SPM fabricated hardware.

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Table 2.2: Spice parameters of schottky diode [87]

Parameter Type	Values
Saturation current, I_s	0.48nA
Ohmic resistance, R_s	7.8
Emission coefficient, N	1.067
Junction capacitance at zero bias, C_{jo}	0.0649pF
Junction potential, V_j	0.65 V
Grading Coefficient, M	0.5
Energy gap, Eg	0.69eV
Breakdown Voltage, Bv	26.7
Low Level Reverse breakdown knee current, Ibv	100µA

Figure 2.2.The capacitors by American Technical Ceramics (ATC) are used as DC blocks to avoid leakage of DC bias to SPC. The bias can be supplied as common-mode voltage from differential *I* , *Q* ports.

Figure 2.3 shows diode reflection coefficient with different bias voltages for RF carrier power of 0 dBm in simulation. One can see from Figure 2.3 that for carrier power of 0 dBm, the diode can operate in quasi-linear region with peak-to-peak voltage of 180 mV around the common mode bias voltage of 360 mV. While extending this region, the diode non-linearity will play an important role restricting the dynamic range of the diode and therefore modulator. In addition, a hardware imperfection will enhances this small non-linearity further in real scenario.

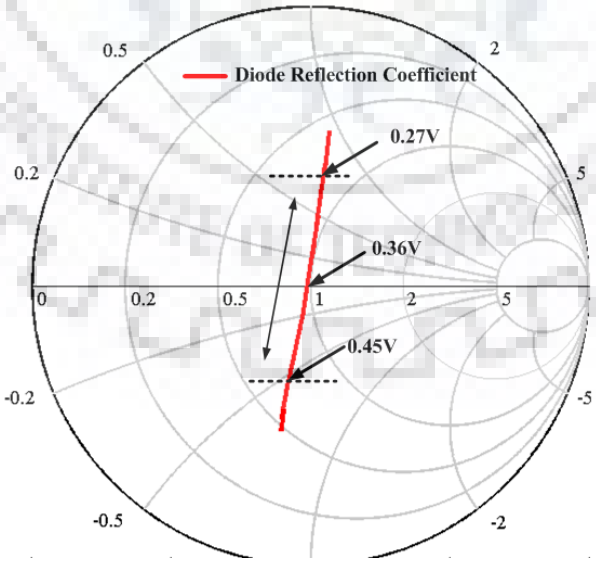

Figure 2.3: Variation of reflection coefficient of diode as variable load with bias.

Therefore, a digital correction scheme is required in SPM which are described in later chapters.

2.3.1 S-Parameters of Six-Port Modulator

The s-parmeters of passive SPC used in SPM is seperately fabricated for measuring its s-parameters. This is shown in Figure 2.4. This SPC comprises of three BLCs and one WPD and similar to the archeitecture as described in Figure 1.2 in chapter 1. The s-parameter of this SPC is validated using electromagnetic (EM) simulation as well as in measurement using vector network anlyzer (VNA).

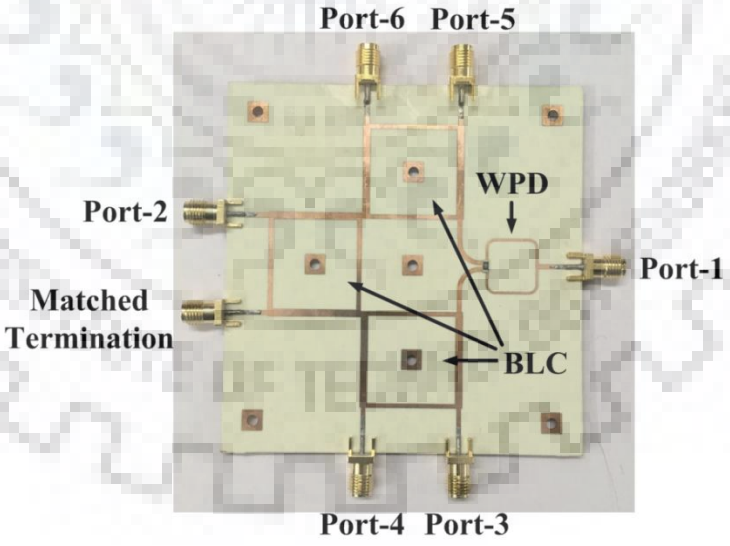

Figure 2.4: Photograph of SPC used in SPM.

Figure 2.5 shows s-parameters S_{11}, S_{22}, S_{33}, S_{44}, S_{55} and S_{66} expressed at each port. One can see from this figure that return loss is greater than 27 dB at center frequency of 2 GHz at each port. This corresponds to the S-parameter values below 0.044 which is close to ideal value of zero as given in s-parameter matrix of (2.1). Figure 2.6 shows magnitude of s-parameters S_{32}, S_{42}, S_{52} and S_{62} in dB scale.

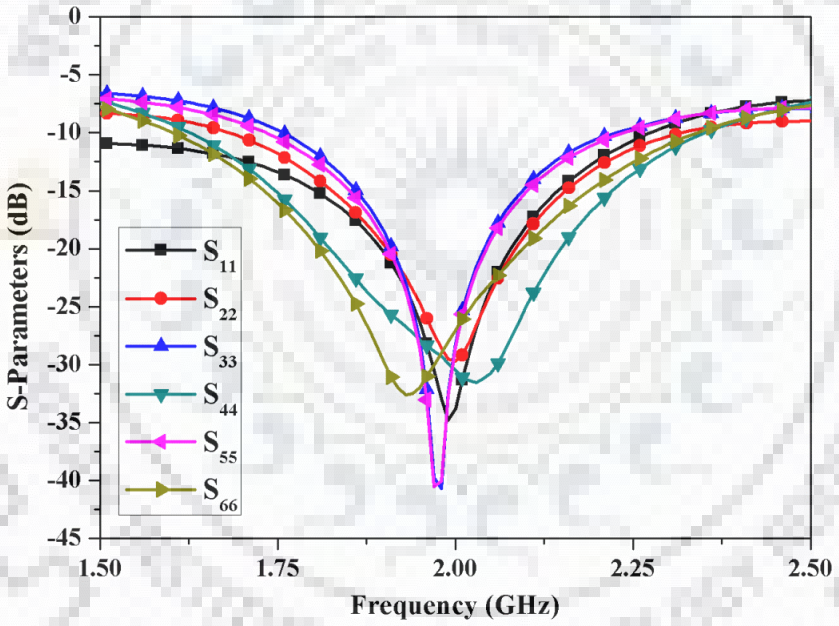

Figure.2.5: Magnitude of various s-parameters (in dB) at each port.

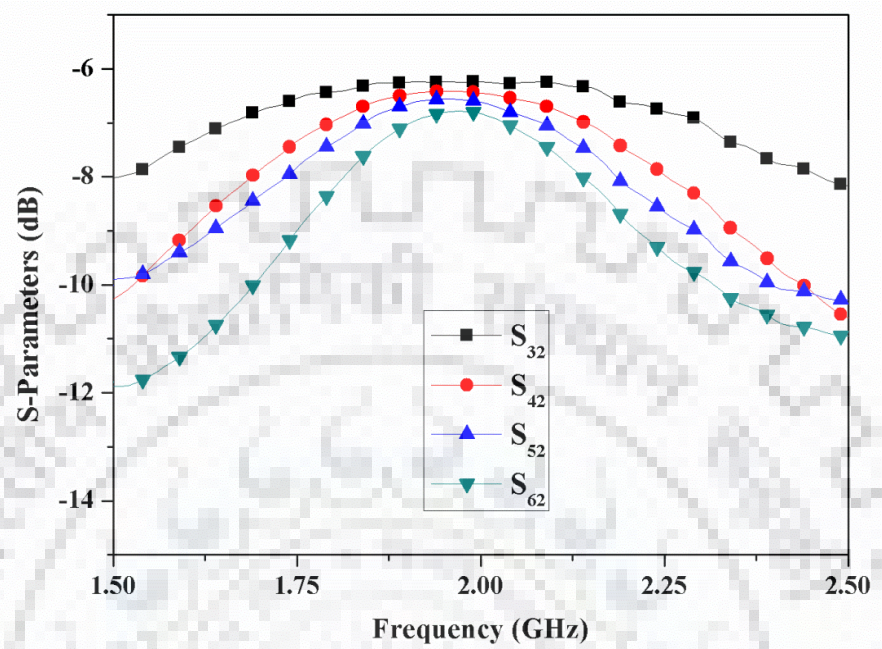

Figure 2.6: Magnitude of s-parameters (dB): S_{32}, S_{42}, S_{52} and S_{62}.

One can verify from Figure 2.6 that the magnitude of these s-parameters is between -6.2 dB -6.8 dB. This corresponds to the values of magnitude between 0.46 to 0.49 in the linear scale which is close to the ideal value of 0.5 as given in s-parameter matrix of (2.1).

Figure 2.7 shows the measured magnitude of s-parameters S_{13}, S_{14}, S_{15} and S_{16} in dB scale. One can see that the values are s-parameters is between -6.2 dB to -6.5 dB. This corresponds to the values of magnitude between 0.47 to 0.49 in the linear scale which is close to the ideal value of 0.5 as given in s-parameter matrix of (2.1). Figure 2.8 represents measured phase of s-parameters S_{32}, S_{42}, S_{52} and S_{62}.

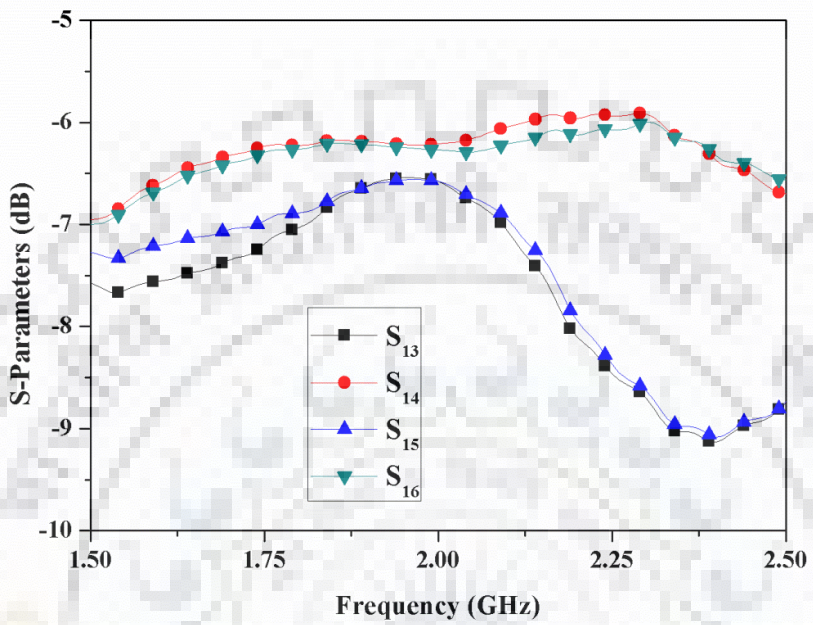

Figure 2.7: Magnitude of s-parameters (dB): S_{13}, S_{14}, S_{15} and S_{16}.

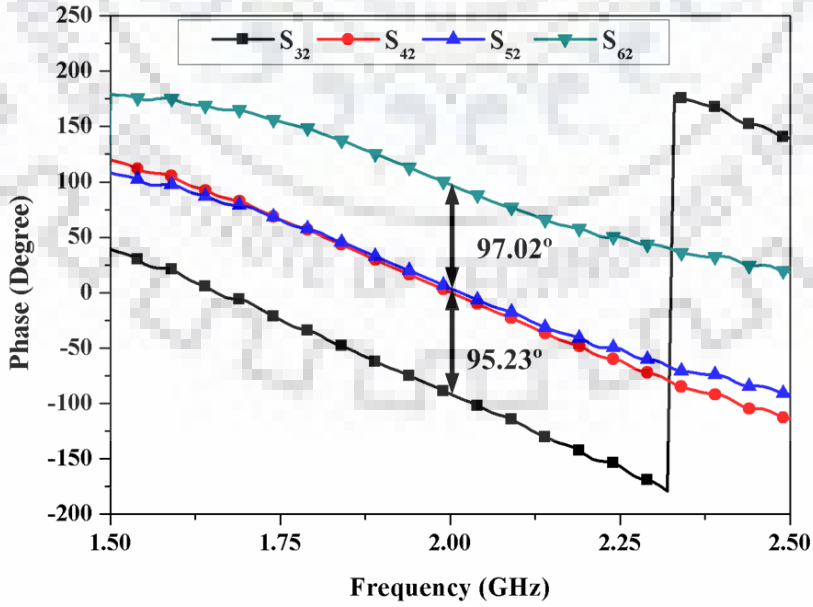

Figure 2.8: Phase of s-parameters (Degree): S_{32}, S_{42}, S_{52} and S_{62}.

Assuming, initial phase due to feed lines and interconnections to be approximately-88˚ to -91˚ for de-embedding, the value of angle of s-parameters S_{32}, S_{42}, S_{52} and S_{62} are slightly deviated within 6˚ from the ideal phase as described in s-parameter matrix of (2.1).

Figure 2.9 shows the phase of s-parameters: S_{13}, S_{14}, S_{15} and S_{16}. De-embedding, constant offset between-144˚and -147˚ due to feedline and interconnections, the phases are close to the values as listed in (2.1) within an error of 9˚.

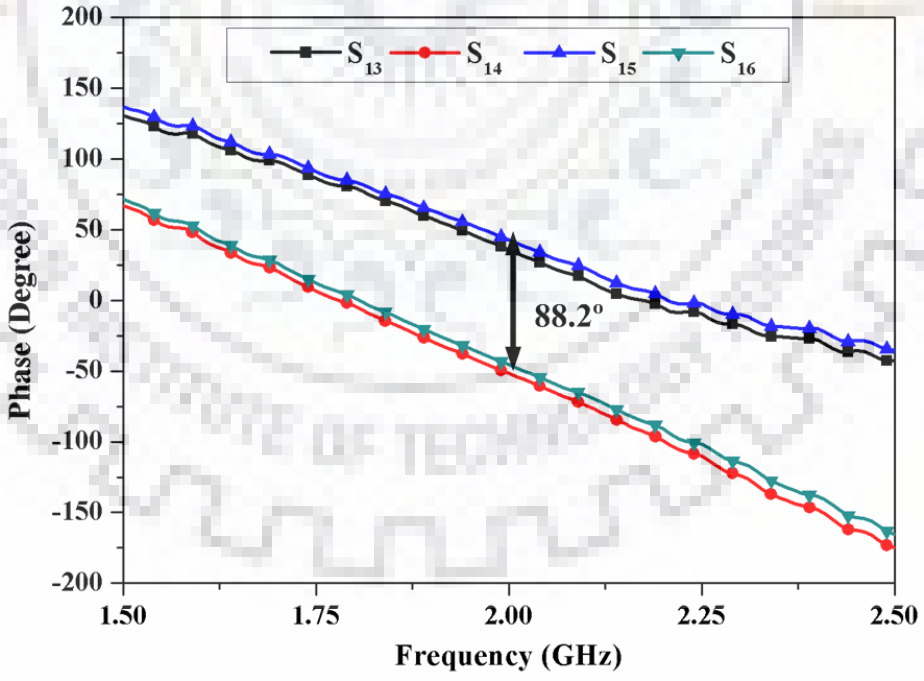

Figure 2.9: Phase of s-parameters (Degree): S_{13}, S_{14}, S_{15} and S_{16}.

2.3.2 Modulated Results in ADS/MATLAB Co-simulation

The modulating capability of SPM designed in this chapter is first validated in simulation by using Keysight advanced design system (ADS) computer aided design (CAD) tool. In such case, cosine and sine signals of 5 MHz frequency are used as *I* and *Q* data representing an intermediate frequency (IF) signal. They are applied differentially as shown in Figure 2.1. Here, the RF carrier is represented as local oscillator (LO) of frequency 2 GHz which is applied at port P_2. The power of this LO signal is set to2 dBm and the diodes are biased at 0.2 V. Figure 2.10 shows the spectral response of the modulated output at port P_1 in Figure 2.1. The RF power is obtained as -6 dBm, whereas, LO leakage is -46 dBm. The image suppression is around 55 dBc. The other products are intermodulation products of f_{IF} and f_{LO} due to inherent diode non-linearity. Figure 2.10 validates the SPM performance in simulation, where, the spurious components such as image, LO and intermodulation products are suppressed to some extent. However, this suppression is limited due to hardware imperfections resulting into non ideal s-parameter of passive SPC. In addition, a non-linear effect may also combine with these hardware imperfections results into distortions which degrade the performance of SPM. This can be corrected digitally in baseband before DACs which is explained in the subsequent chapters.

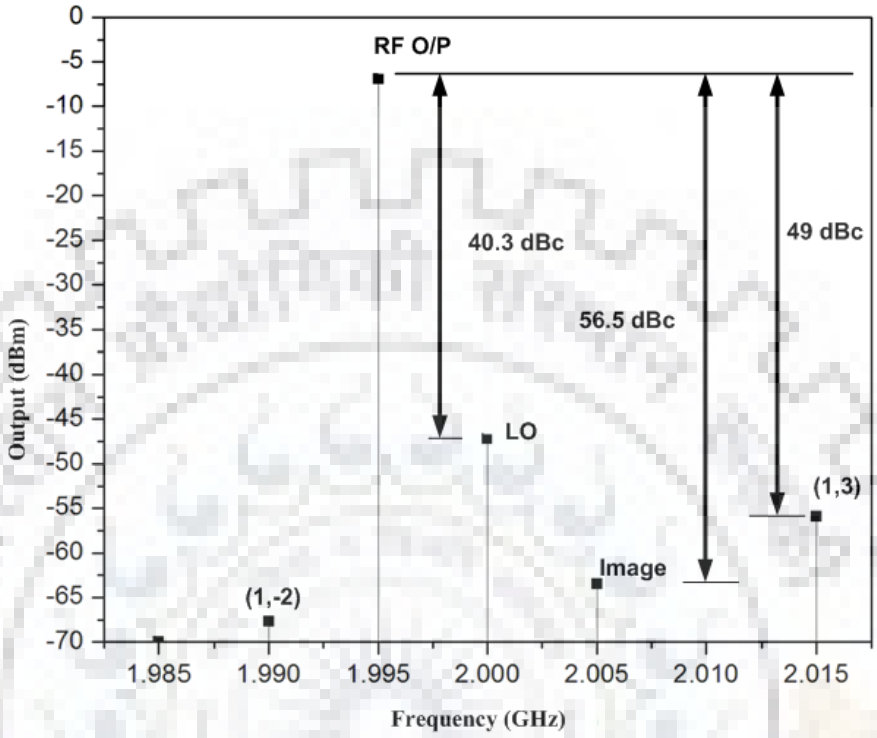

Figure 2.10: Simulated output of six-port network.

2.4 **Measurement and Characterization Test-bed for SPM**

The characterization and distortion mitigation setup of SPM has digital baseband generation unit and a bank of DACs for converting baseband digital data into analog *I, Q* signals in differential form i.e. $I = -\bar{I}, Q = -\bar{Q}$. Figure 2.11 shows this instrument based test-bed, where, baseband generation and DAC are realized by VSG from Keysight (model no. MXG N5182B). The computer as shown in Figure 2.11 uses MATLAB to generate different signals using different modulation schemes and data rates. The corresponding baseband data in *I* and *Q* format is uploaded in the memory of VSG using general purpose interface bus (GPIB) interface. The GPIB is common terminology for IEEE 488 short-range digital communications which uses 8-bit parallel multi-master interface bus specification. The VSG plays the baseband data stored in its internal memory and its internal DACs convert this digital baseband data into analog signals which are available $I, -\bar{I}, Q, -\bar{Q}$ in differential form at the rear panel of VSG as shown in Figure 2.11.

These signals are then fed to six-port quadrature modulator at its respective inputs as shown in Figure 2.10.The six-port quadrature modulator is an in-house developed PCB as shown in Figure 2.2. The bias is supplied as common-mode voltage from differential *I-Q* ports in the rear panel of VSG. The RF modulated carrier is captured using vector signal analyzer (VSA) by Keysight (model no. MXA N9020B) as shown in Figure 2.11.The captured signal can be displayed in the form of spectrum in VSA. The VSA also has the

feature to demodulate captured signal and extract the baseband *I* and *Q* data using its internal quadrature-demodulator and analog to digital converters (ADCs).

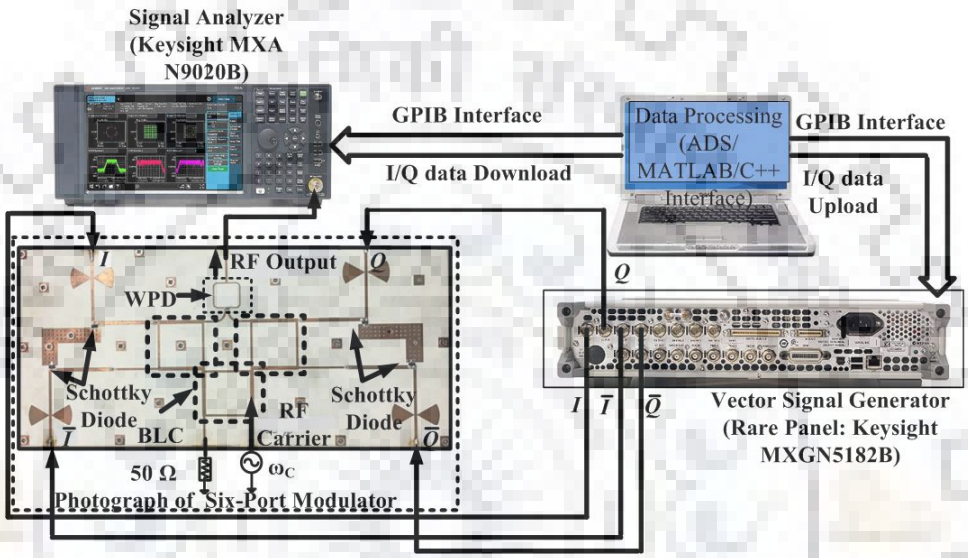

Figure 2.11: Characterization setup for SPM.

This baseband data is sent back to computer using GPIB interface where the MATLAB is used for further processing. Once, the corresponding baseband *I* and *Q* data at the input as well as output is known, the complex gain of the system can be identified by comparing the two. An appropriate behavioral modeling is then employed to model the complex gain in terms of gain and phase compression characteristics of the system. Once, the model is complete, an inverse model can be employed in digital domain to predistort the input baseband *I* and *Q* data such that linear as well as non-linear distortion can be cancelled at the output. In order to evaluate the performance of six-port based modulator, a 20 MHz LTE signal with 100 Mbps data rate using 64-QAM modulation

scheme is modulated using the SPM as shown in Figure 2.11.The characterization setup of Figure 2.11is also used to capture the modulated output to measure the performance in terms of ACLR and EVM.

2.5 **Measurement Results**

The measured output spectrum of RF carrier modulated by SPM and captured by VSA is shown in Figure 2.12. Ideally, the spectrum should not have adjacent channel leakage.

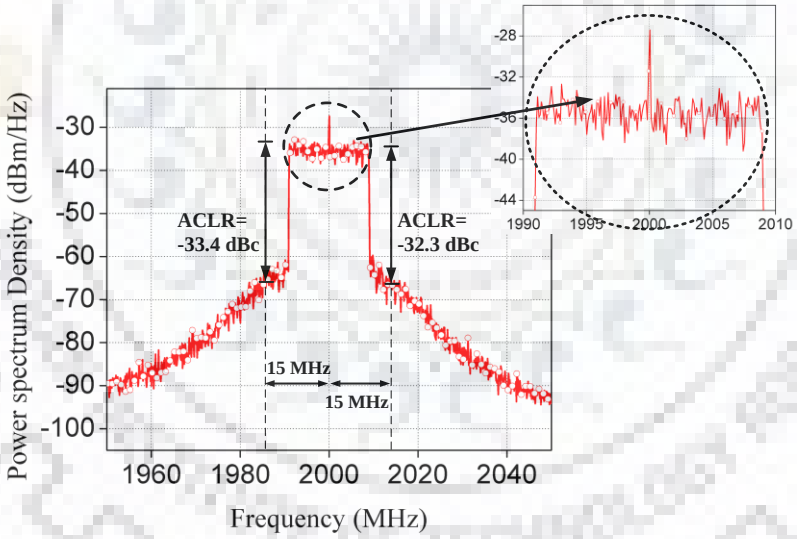

Figure 2.12: Measured distorted spectrum of RF carrier modulated with 20 MHz LTE captured at the output of SPM characterization setup.

One can see from Figure 2.12, a spectral leakage in adjacent band is appearing due to several distortions such as diode non-linearity and imperfections in passive SPC hardware. The ACLR is the measure of spectral leakage in the adjacent channel. The

ACLR is calculated as ratio of power measured in adjacent channel at certain frequency offset to the power measured within the channel. Figure 2.12 shows an ACLR of -33.4 dBc and -32.2 dBc measured at 15 MHz offset in lower and upper side of center frequency, respectively. These ACLR values do not comply with the industry requirements as described in RF physical layer specification of 3GPP TS36.141 6.2 document [88]-[89]. A carrier leakage is also appearing in the signal as shown in zoomed version of measured spectrum in Figure 2.12. This will result into an in-band distortion in this case.

Figure 2.13 shows the constellation of 64-QAM signal after demodulation of LTE carrier captured by VSA in Figure 2.11. From Figure 2.13 one can see the symbol spreading due to distortion, as compared to the actual symbols locations. This spread is measured in terms of EVM which is a measure of the error between the predefined industry-approved constellation symbol location and the actual measured symbol after equalization [90]. The EVM of 20.14% is calculated in the present case for the modulated signal with no correction. This does not qualify the 8% requirements of LTE signal with 64-QAM modulation as described in RF physical layer specification as mentioned in 3GPP TS36.104 document [90]-[91]. Therefore, it is important to capture and model the distortion of SPM such that a suitable digital correction scheme can be employed to mitigate them.

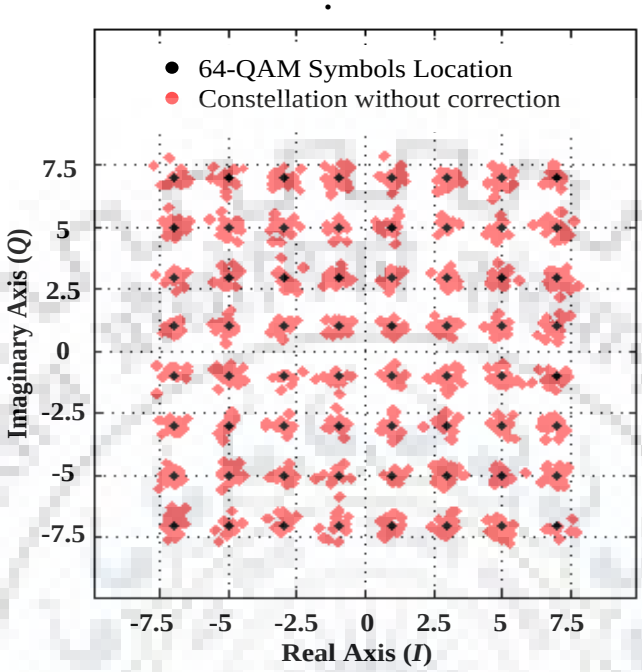

Figure 2.13: Measured constellation diagram of 64-QAM used in LTE signal modulated by SPM.

2.6 **Conclusion**

This chapter discusses the basic architecture of SPM and its operating principle for modulating *I* and *Q* signals of any digital modulation schemes such as QAM produced after DAC conversion. A hardware prototype based on this architecture is designed and developed to demonstrate the modulation feature of SPM. An RF instrument based characterization setup is also developed to upload *I* and *Q* signals of any digital modulation scheme and convert them to analog signals using DACs for driving six-port based modulator hardware prototype. A successful modulation of LTE signal using 64 QAM is demonstrated using the hardware prototype SPM and its characterization setup.

However, due to several distortions and hardware imperfections, the quality of modulation in terms of measured EVM is not up to mark and does not qualify the requirement set by LTE standard. Therefore, a suitable distortion mitigation scheme must be studied to utilize six-port based modulators to be used in commercial LTE transmission.

Chapter Three: Characterization of Linear and Non-linear Distortions of Six-Port Modulator and Digital Pre-Compensation.

3.1 **Introduction**

This Chapter focuses on the characterization of various distortions (linear as well as non-linear) in SPM. The diode is the major source of non-linear distortion in SPM design, as discussed in section 2.1 of chapter 2. In addition, small hardware imperfections in implementing the correct s-parameters of passive SPC in hardware prototype further enhances these distortions. This chapter analyze the effect of these hardware imperfections in generating extra cross-modulation terms due to even weak non-linearity of diode operation. In order to digitally compensate these linear and non-linear distortions, a behavioural model is developed based on real-valued focused time delay neural network. This model is based on the characterization of the SPM prototype developed in chapter 2 using the gain and phase distortions captured from the test-bed developed in previous chapter. Later, these distortions are modelled and inverse of this model is applied in digital domain for pre-compensation. The *I* and *Q* baseband data when passes through this model get predistorted such that after modulation from SPM, the output of SPM is effectively distortion free. This digital pre-compensation technique is established with the successful modulation of QAM and LTE signals over the RF carrier at 2 GHz. The modulated carrier qualifies the requirement by LTE standard in terms of EVM and ACLR.

3.2 **Six-Port Modulator Architecture in Presence of hardware Imperfections**

SPM architecture using schottky diodes as variable load is described in section 2.1 of chapter 2. The ideal s-parameters of SPC are given in (2.1). In case of hardware imperfections, the elements of this s-parameter matrix changes. If a small error (δ) is assumed in every s-parameters in terms of phase and amplitude, the modified s-parameter matrix with hardware imperfection can be given by

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \\ b_5 \\ b_6 \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 0 & 0 & -(1+\delta_1)+j\delta_2 \\ 0 & 0 & (1+\delta_9)+j\delta_{10} \\ -(1+\delta_1)+j\delta_2 & (1+\delta_9)+j\delta_{10} & 0 \\ \delta_3+j(1+\delta_4) & \delta_{11}+j(1+\delta_{12}) & 0 \\ -(1+\delta_5)+j\delta_6 & \delta_{13}+j(1+\delta_{14}) & 0 \\ \delta_7+j(1+\delta_8) & -(1+\delta_{15})+j\delta_{16} & 0 \end{bmatrix} \begin{bmatrix} \delta_3+j(1+\delta_4) & -(1+\delta_5)+j\delta_6 & \delta_7+j(1+\delta_8) \\ \delta_{11}+j(1+\delta_{12}) & \delta_{13}+j(1+\delta_{14}) & -(1+\delta_{15})+j\delta_{16} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ a_5 \\ a_6 \end{bmatrix} \quad (3.1)$$

In order to simplify the case, the isolation and reflection coefficient of each element of SPC are assumed 0. The reciprocity i.e. $S_{ij}=S_{ji}$, is also considered in (3.1) as the travelling wave faces same transmission while moving from i^{th} port to j^{th} port and vice versa. In order to further simplify the analyses, all error terms are assumed to be very small and

hence same i.e. $\delta_1 = \delta_2 = \delta_3 = \delta_4 = \ldots. \delta_{16} = \delta$. For ideal case, without the above imperfections, where $\delta_1 = \delta_2 = \delta_3 = \delta_4 = \ldots. \delta_{16} = \delta = 0$, (3.1) reduces to (2.2). Using the imperfect s-parameter matrix of SPC as given by (3.1) in (2.2), one can obtain the output wave b_1 as given in (3.2).

$$b_1 = -\frac{a_2}{4}\Big[\left\{\Gamma_3\left(1+2\delta+2\delta^2\right)+\Gamma_4\left(1+2\delta\right)+2\delta\left(1+\delta\right)\left(\Gamma_5+\Gamma_6\right)\right\} + j\left\{\left(1+2\delta\right)\left(\Gamma_5+\Gamma_6\right)-\Gamma_4 2\delta\left(\delta+1\right)\right\}\Big] \tag{3.2}$$

Assuming, the diode is operating in non-linear region, one can now truncate (2.4) to third-order non-linear approximation as

$$\Gamma_{D,m}\left(V\right) \approx \Gamma_0 + k_0.\Delta v + k_1.\left(\Delta v\right)^2 + k_2.\left(\Delta v\right)^3 \tag{3.3}$$

If the reflection coefficient $\Gamma_{D,m}(V)$ as described in (3.3) is controlled by the baseband I and Q data which are in voltage form, then one can write

$$\Gamma_3\left(V\right) = \Gamma_{D,3}\left(V\right) = \Gamma_0 + kI + k_1 I^2 + k_2 I^3 \tag{3.4}$$

$$\Gamma_5\left(V\right) = \Gamma_{D,5}\left(V\right) = \Gamma_0 + kQ + k_1 Q^2 + k_2 Q^3 \tag{3.5}$$

$$\Gamma_4\left(V\right) = e^{-j\pi}\Gamma_{D,4}\left(V\right) = -\Gamma_{D,4}\left(V\right) = -\Gamma_0 - k\bar{I} - k_1\left(\bar{I}\right)^2 - k_2\left(\bar{I}\right)^3 \tag{3.6}$$

$$\Gamma_6(V) = e^{-j\pi}\Gamma_{D,6}(V) = -\Gamma_{D,6}(V) = -\Gamma_0 - k\bar{Q} - k_1(\bar{Q})^2 - k_2(\bar{Q})^3 \tag{3.7}$$

Using (3.4) to (3.7) in (3.2), the modulator output can be represented as (3.8) with various modulator imperfections. This expression is obtained assuming $\bar{I}$ and $\bar{Q}$ representing exact inverted replica of baseband *I* and *Q* signals i.e. *I*= - $\bar{I}$, *Q*= - $\bar{Q}$.

$$\begin{aligned} b_1 = -\frac{a_2}{4}\Bigg[\Bigg\{ & \underbrace{2k(1+\delta)^2 I}_{I\,Component} + \underbrace{4k\delta(1+\delta)Q}_{Crosstalk/Leakage\,of\,Q} + \underbrace{2\delta^2\Gamma_0}_{DC\,offset} \\ & + \underbrace{2k_1\delta^2 I^2 + 2k_2(1+\delta)^2 I^3}_{Nonlinear\,Terms\,of\,I} + \underbrace{4k_2\delta(1+\delta)Q^3}_{Nonlinear\,Term\,of\,Q}\Bigg\} \\ & + j\Bigg\{\underbrace{2k(1+2\delta)Q}_{Q\,Component} - \underbrace{2k\delta(1+\delta)I}_{Crosstalk/Leakage\,of\,I} + \underbrace{2\delta(1+\delta)\Gamma_0}_{DC\,offset} \\ & + \underbrace{2k_2(1+2\delta)Q^3}_{Nonlinear\,Terms\,of\,Q} + \underbrace{2k_1\delta(1+\delta)I^2 - 2k_2\delta(1+\delta)I^3}_{Nonlinear\,Terms\,of\,I}\Bigg\}\Bigg] \end{aligned} \tag{3.8}$$

One can clearly see from (3.8) that due to imperfect realization of s-parameters of passive SPC along with non-linearity of diode, there is a crosstalk between real and imaginary part depending upon all the reflection coefficients. In addition, the common mode voltage which should cancel in ideal situation is present at the output as DC offset at both in-phase and quadrature component of output wave b_1. This DC-offset can be ignored in in-phase component considering δ is small, however, its effect cannot be

neglected in quadrature component. One can also see that slight tuning in terms of amplitude of *I* and *Q* can correct for some imbalances as discussed in [24], but cannot mitigate the DC offset. The non-linearity will further expand with small error in the s-parameter matrix as shown in (3.8) and will contribute to further cross talk. Therefore, the strategy of using differential *I* and *Q* along with quarter-wave transmission line [18]-[33],[55] cannot completely remove the component Γ_0 contributing for carrier leakage, if SPC is realized with imperfect s-parameters.

3.3 **Non-linearity in Schottky Diode**

Figure 3.1 shows the variation of real and imaginary parts of complex reflection coefficient Γ_m of diode with bias voltage. Figure 3.1 also shows this variation for different local oscillator (LO) power. The LO power here represents the RF carrier power during modulation. A non-linear model of diode in simulation has been used to estimate diode non-linearity in Figure 3.1. One can see from Figure 3.1, that for LO power of 0 dBm, the diode varies over quasi-linear region of 270 mV to 450 mV. Therefore, the diode bias can be set at 360 mV with maximum peak-to-peak voltage varying 180 mV around the common mode bias voltage of 360 mV.

Accordingly, the *I* and *Q* signal voltages are also falling within this range. In real scenario the hardware imperfections and small diode non-linearity is inevitable. Therefore, a digital correction scheme is required in SPM to keep the errors due to above imperfection under check. Like any other quadrature modulator, SPM is connected

directly to baseband digital unit. Therefore, a suitable digital predistortion scheme can correct its linear as well as non-linear distortions. Even with careful design, some of these imperfections are inevitable.

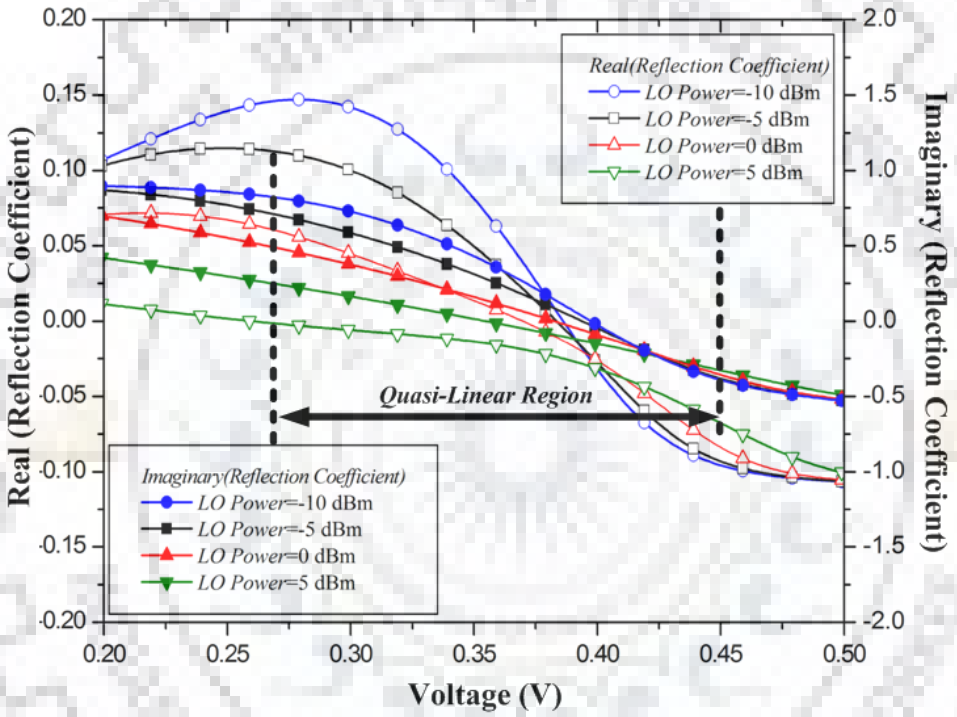

Figure 3.1: Diode non-linearity in simulation and quasi-linear region for operation with different LO power.

A setup sown in Figure 2.11 is capable of capturing the linear and non-linear distortions and applying an appropriate digital correction to digital-baseband *I*, *Q* signals for hardware compensation.

3.4 **Behavioral Modeling of Distortion in Six-Port Modulator**

In the absence of any distortion, the impairment free modulator output should be linearly scaled version of the baseband data modulated over RF carrier [88]-[89]. If the output of modulator is captured and de-modulated, the demodulated output and the baseband inputs are related as

$$V_{out} = g\left(V_{in}\right) \tag{3.9}$$

where, the baseband input voltage is $V_{in}= I+jQ$, and V_{out} is the demodulated baseband output voltage. The gain represented by function g ( ) is a complex valued non-linear function representing the amplitude as well as phase change in the modulated signals with the input signal amplitude. In ideal situation, this gain and phase change is constant. However, in practice, the gain and phase change produced by the modulator can be non-linear due to diode non-linearity and other impairments, such *I*/*Q* imbalances, cross-talks etc. occurring due to imperfect SPC as given in (3.8).

Figure 3.2 and 3.3 show distortion in gain and phase with respect to input signal power. This is obtained by comparing baseband *I, Q* data demodulated from the output of modulator and the input baseband *I, Q* data fed to the modulator after proper time delay adjustment. The output baseband data is obtained from VSA by down-converting and demodulating captured modulated RF carrier at the output of modulator. One can see

from Figure 3.2 that the non-linear gain response represents amplitude modulation to amplitude modulation (AM/AM) distortion. The large scattering of gain in Figure 3.2 is due to DC offset and *I*/*Q* imperfections in the modulators as established in literature [88]-[90].

Similarly, Figure 3.3 shows the non-linear phase difference between output and input signals of the modulator which represents amplitude modulation to phase modulation (AM/PM) distortion.

Moreover, the bias circuitry uses energy storing elements such as capacitors and inductors with finite charging and discharging time. Thus, in the presence of the modulated signals with broadband envelope, memory effect is also exhibited by the modulator, which contributes to the scattering of its gain and phase response even in the absence of DC offset, non-linearity and I/Q imbalances etc.

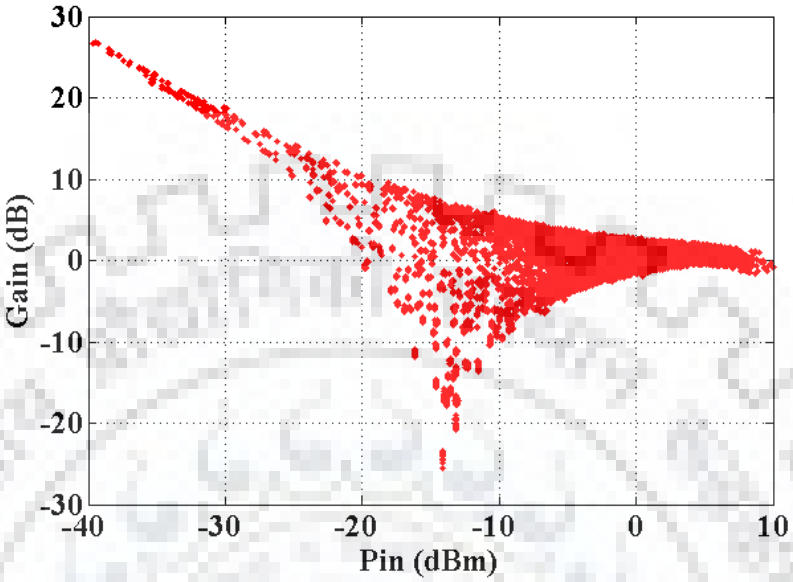

Figure 3.2: Measured gain distortion with input signal power.

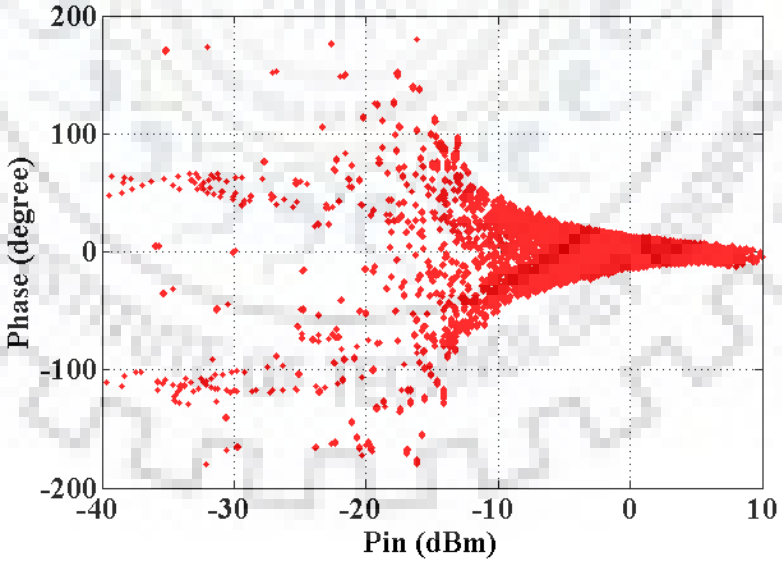

Figure 3.3: Measured phase distortion with input signal power.

3.4.1 Indirect Learning Architecture Predistortion Scheme

The distortion characterization and mitigation setup of Figure 2.11 provides an option of utilizing a very powerful digital correction scheme called predistortion which can correct any type of the hardware distortion. Predistortion scheme requires a behavioral model of hardware capturing all its distortion, and the inverse of this model is implemented in the digital domain. There are two architectures generally used for model extraction i.e. direct learning architecture and indirect learning architecture. The difference between direct and indirect learning architecture has been investigated in [101]. The indirect learning architecture can be run in an open-loop fashion. While direct learning architecture is usually used in closed-loop systems. Therefore, the stability of the system is required to be maintained. The closed-loop estimation is shown in Figure 3.4, where the predistorter coefficients are updated based on linearized system input and output.

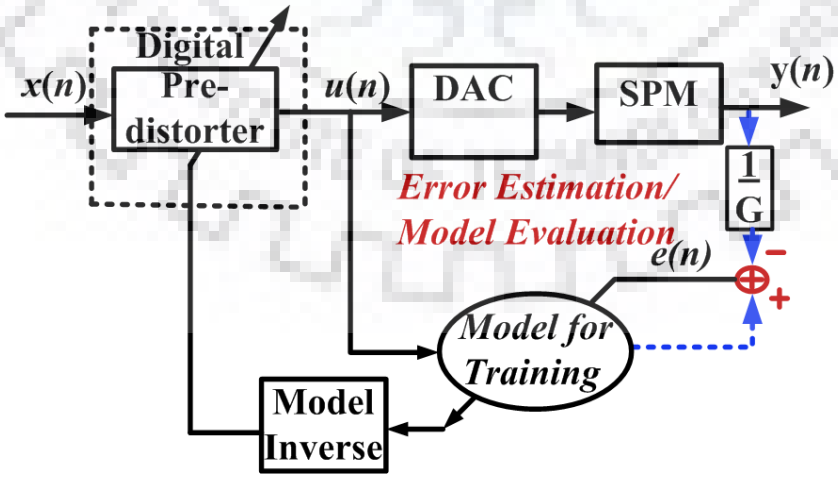

Figure 3.4: Direct Learning Architecture of predistorters scheme

The indirect learning approach is a well-established method for the Digital Predistortion. Figure 3.5 shows the indirect learning architecture (ILA) of predistorter [100],-[103],[113]-[114]. $x(n)$ is input signal to predistorter, $u(n)$ is predistorter output and input to modulator and y(n) is the output of modulator after application of predistorted signal $u(n)$. ILA principle is based on the observation that if the $\tilde{u}$ (n) is the output of predistorter when ($y(n)$ /G) is input to predistorter model, then if one imposes u (n) = $\tilde{u}$ (n), then it leads to x (n) = (y (n) /G), where G represents small signal gain of modulator.

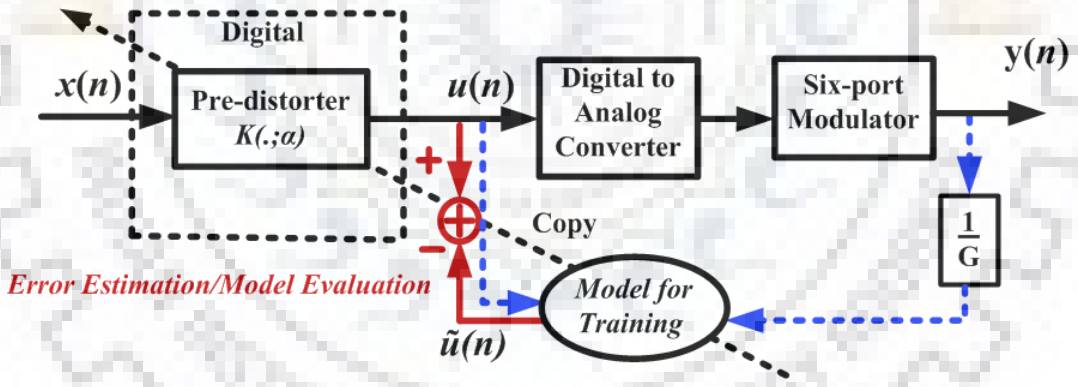

Figure 3.5: Indirect Learning Architecture of predistorters scheme.

In other words, one can also perceive that once required conditions are imposed, the output is linear amplified version of input given as

$$\tilde{u}(n) = \psi(y(n)/G) \tag{3.10}$$

if one imposes condition of $u(n) = \tilde{u}(n)$, predistorter coefficients estimation condition for the first iteration, predistorter has no action and input to SPM is $u(n) = x(n)$. Now

$$x(n) = \psi(y(n)/G) \tag{3.11}$$

As $x(n)$ and $y(n)$ are available from the measurement data, non-linear predistortion model coefficients and subsequently ψ can be calculated using adaptive signal processing schemes. The main advantage of ILA is that predistorters can be any non-linear model ψ that maps normalized output to input available in baseband form. In this thesis, the feed forward neural network (NN) is used to represent non-linear function ψ. Once coefficients (weights/bias) for the model are extracted based on input and output data of modulator, they are digitally copied in predistorters in the digital domain before the analog hardware in the line-up shown in Figure 3.5. One can also observe from Figure 3.5 that for the first iteration, this mapping maps a relation which is inverse of normalized SPM characteristics given as $y(n)/G = \Psi(x(n))$.

3.4.2 Neural Network for Modelling: Real Valued Focused Time Delay Neural Network for Modelling

The real valued focused time-delay neural network (RVFTDNN) topology is shown in Figure 3.6. This NN topology is used to model the function, relating the pair of input *I*, *Q*

data and the pair of output *I, Q* data as shown in Figure 3.6.The motivation of using NN based model becomes evident from linear and non-linear distortion behaviour of six-port based modulator setup. There are linear as well as non-linear distortion in *I* and *Q*.

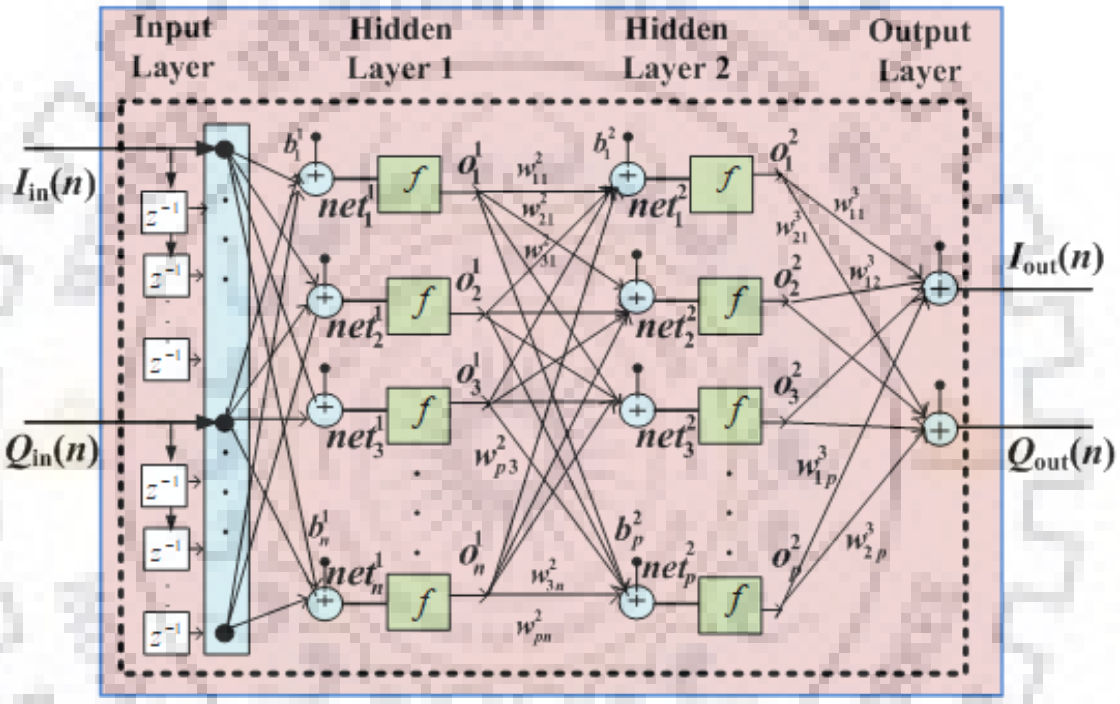

Figure 3.6: Architecture of real-valued focused time delay neural network.

In addition, there is a possible cross-talk between *I* and *Q* due to imperfect s-parameter of SPC as described in (3.8). In such case, NN based model is very useful as it can map all these possible combinations of cross-talks, non-linearity and dc bias which is expected from its topology as shown in Figure 3.6. The feed-forward neural network (FFNN) is a popular modelling tool, which is presented with input vectors of order $1\times2(m+1)$, including the real values of present and past inputs.

$$X(n) = [I_{in}(n), I_{in}(n-1).....I_{in}(n-m), Q_{in}(n), Q_{in}(n-1).....Q_{in}(n-m)] \quad (3.12)$$

where *n* denotes the present training sample and *m* is the memory length of the modulator system. The targeted output vector is

$$Y(n) = [I_{out}(n), Q_{out}(n)] \quad (3.13)$$

where, I_{out} (*n*) and Q_{out} (*n*) represents pair of output *I*, *Q* data.

3.4.2.1. Forward Computation

The hidden layers are fully connected, as shown in Figure 3.6. During the forward computation, data from neurons of a lower layer (i.e., k^{th} layer) is multiplied with weight and propagated forward to neurons in the upper layer i.e., $(k+1)^{th}$ layer. The net input to any neuron, *i*, in any layer (*k*+1) is given by

$$\text{net}_i^{k+1} = \sum_{j=1}^{p} w_{ij}^{k+1} o_j^k + b_i^{k+1} \quad (3.14)$$

If w_{ij} denotes the synaptic weight connecting the j^{th} input from the previous layer to the i^{th} neuron of the present layer, where, P denotes the total number of neurons in the previous layers, b_i^k denotes bias of the i^{th} neuron in the k^{th} layer. It is worth mentioning that the SPM output is the function of four variables $I, \bar{I}, Q, \bar{Q}$. The $\bar{I}$ and $\bar{Q}$ represents an inverted replica of baseband I and Q signals which are automatically adjusted in the bias value of neurons inherently present in the NN. The output of any layer represents an input to the next layer. The output of i^{th} neuron at any k^{th} layer is calculated as

$$o_i^k = f(\text{net}_i^k) \tag{3.15}$$

where, f is a non-linear activation function, which maps non-linearity between –1 and 1. The hyperbolic tangent, also known as the "tansig" function, is a popular choice if the input signal contains both positive and negative values. Therefore, hidden layers have 'tansig' function to introduce non-linear filtering. Initial weights are chosen randomly in the interval of [–0.8,0.8] which converge iteratively towards their optimal values as the training progress. The output layer has a linear activation function, which adds the outputs of hidden neurons and linearly maps them to the output.

3.4.2.2.Backward Computation

The error calculation at the output of each layer is handled by backward computation.

This error originates at the output of *NN* by calculating error between desired output and computed output of *NN* in previous section.

$$\xi = \frac{1}{2N}\sum_{n=1}^{N}\{[I_{\text{out}}(n)-\hat{I}_{\text{out}}(n)]^2+[Q_{\text{out}}(n)-\hat{Q}_{\text{out}}(n)]^2\} \quad (3.16)$$

where ξ is total error, $I_{out}(n)$ and $Q_{out}(n)$ are the desired outputs, and $\hat{I}_{out}(n)$ and $\hat{Q}_{out}(n)$ are the outputs from output- layer neurons. If δ_i^{k+1} is the local gradient for the i^{th} neuron in the $(k+1)^{\text{th}}$ layer given by

$$\delta_i^k = \varepsilon_i^k f'(\text{net}_i^k) \qquad k = \text{Present Layer} \quad (3.17)$$

$$\varepsilon_i^k = \begin{cases} t_i - o_i^k & k = \text{Output Layer} \\ \sum_{j=1}^{N_{k+1}} w_{ij}^{k+1}\delta_j^{k+1} & k = \text{Hidden Layer} \end{cases} \quad (3.18)$$

where ε_i^k is the error term for the i^{th} neuron in k^{th} layer, and $f'(\text{net}_i^k)$ is the derivative of the activation function. With the aim of minimizing the error energy given in (3.16), the backward computation is done in batch mode to adjust the synaptic weights and biases of the network. Several numerical optimization techniques can be used for weight adaptation at each layer. Figure 3.7 shows the convergence of prominent algorithms implemented for the given problem.

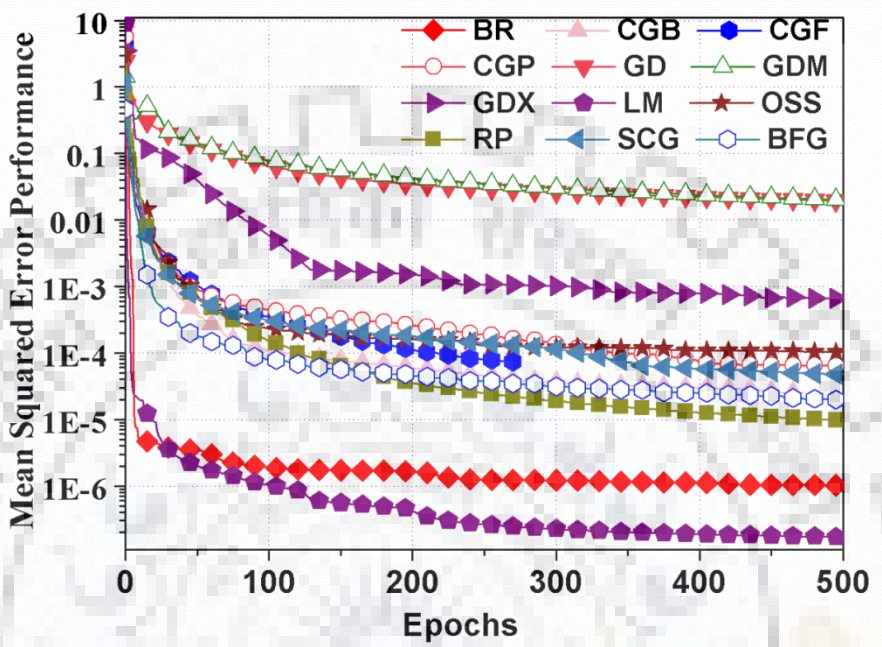

Figure 3.7: Convergence of various NN optimization algorithms for inverse modeling of distortion in SPM.

Gradient Descent (GD) method updates the weights in the direction of negative gradient, i.e. $\Delta \mathbf{X} = -\mu J(\mathbf{X})$, where $J(\mathbf{X})$ is the Jacobian matrix of performance calculated with respect to $\mathbf{X}$, where

$$\mathbf{X} = [w\ w \ldots\ldots\ldots w\ b \ldots\ldots b \ldots\ldots w\ w \ldots\ldots w\ b \ldots\ldots b\ ] \tag{3.19}$$

Gradient descent with momentum (GDM) is a modification over GD to avoid falling into local minima given by $\Delta \mathbf{X} = \eta \Delta \mathbf{X}_{prev} + \mu(1-\eta)\mathrm{J}(\mathbf{X})$. Another modification of GD is variable learning rate gradient descent (GDX), which utilizes different learning rates at

each iteration for faster convergence. Resilient propagation method (RP) uses only the sign of the derivative to determine the direction of the weight update. The updated value for each weight and bias is increased by a factor whenever the derivative of the performance function with respect to that weight has the same sign for two successive iterations.

Another class of optimization is based on conjugate gradient method $\Delta\mathbf{X} = -\eta d(\mathbf{X})$, where $d(\mathbf{X}) = -J(\mathbf{X}) + d(\mathbf{X})_{old} Z$ is the direction of search. Fletcher-reeves version of conjugate gradient (CGF) uses line search method to calculate $d(\mathbf{X})$. In Polak-Ribiére variation (CGP), *Z* for direction search is calculated as [123].

$$Z = \frac{-\Delta \mathrm{J}_{old}{}^{T}(\mathbf{X})\mathrm{J}^{T}(\mathbf{X})}{\mathrm{J}_{old}{}^{T}(\mathbf{X})\mathrm{J}_{old}{}^{T}(\mathbf{X})} \quad (3.20)$$

Another variation based on Powell-Beale Algorithm (CGB) avoids saturation and early stopping of CG methods, which is imposed by checking $\left| J_{old}{}^{Tb}(\mathbf{X}) J(\mathbf{X}) \right| \geq 0.2 \left| J^{T}(\mathbf{X})\ J(\mathbf{X}) \right|$ for each term in Jacobian matrix. Scaled Conjugate gradient (SCG) method uses second order optimization, instead of line-search method, along with a regularization factor for stopping Hessian Matrix from becoming indefinite [130]. Another method relies on approximating Hessian matrix H(**X**) to achieve Newton's solution $\Delta\mathbf{X} = -H^{-1}(\mathbf{X})\ J(\mathbf{X})$ for fast convergence. Broyden, Fletcher, Goldfarb, and Shanno (BFGS) is most popular implementation [123]. To reduce complexity of BFGS method, one step secant method (OSS) has been proposed as a bridge between

Conjugate gradient and Newton's method, where search direction is defined as $d(\mathbf{X})=-J(\mathbf{X}) + a\Delta\mathbf{X}+ b\Delta d(\mathbf{X})$ [124].

Levenberg-Marquardt algorithm is a numerical optimization of the Gauss-Newton method [132]. The very high value of μ provides steepest descent solution where a small value of μ leads to a Gauss-Newton solution, which avoids falling into local minima. For any iteration, the change in the neurons weights and biases from previous iteration is calculated as

$$\Delta\mathbf{X} = [\mathrm{J}^T(\mathbf{X})\mathrm{J}(\mathbf{X}) + \mu\mathrm{I}]^{-1}\mathrm{J}^T(\mathbf{X})\mathrm{e}(\mathbf{X}) \tag{3.21}$$

$$\mathrm{e}(\mathbf{X}) = [\varepsilon_I(I)\varepsilon_Q(I)\varepsilon_I(2)\varepsilon_Q(2).....\varepsilon_I(N)\varepsilon_Q(N)] \tag{3.22}$$

where, N denotes the total number of training samples, h denotes the outermost layer, and ε_I and ε_Q are local gradients according to (3.18), calculated for I and Q, respectively. Bayesian regularization (BR) method is modification over LM technique for better generalization qualities [133]. Based on the convergence curves, LM had been chosen as selected optimization algorithm. The procedure is repeated for each layer in backward direction. The training is provided in several iterations till the desired performance is achieved as shown in Figure 3.8.

3.4.3 Inverse Modeling Performance

The distortion mitigation capability of DPD depends on the accuracy of the model that is trained to learn the inverse characteristics ψ given in (3.11). The *NN* must be exposed to the training dataset containing the entire possible range of input voltage level for best learning. The performance of any modeling can be validated, in terms of the normalized-mean-square error (NMSE) given by

$$\mathrm{NMSE} = 10\log_{10}\left(\frac{\sum_{\mathrm{i=1}}^{\mathrm{N}}(I - I_{\mathrm{desired}})^2 + (Q - Q_{\mathrm{desired}})^2}{\sum_{i=1}^{N} {I_{\mathrm{desired}}}^2 + {Q_{\mathrm{desired}}}^2}\right) \tag{3.23}$$

where I and Q are the model outputs, which are compared with the desired output $I_{desired}$ and $Q_{desired}$. Figure 3.7 shows the effects of increasing number of neurons on inverse modeling performance and it can be observed that beyond 8 neurons in hidden layer, the improvement is not drastic. In this modeling, 15 neurons in the hidden layer have been chosen. One can note that each neuron of the proposed *NN*, (shown in Figure 3.7) contains a non-linear function, a bias and weighted outputs of each neuron is interconnected with other neurons from previous layer.

Therefore, proposed *NN* is well suited to model non-linearity of diodes, dc offset and cross-interference terms.

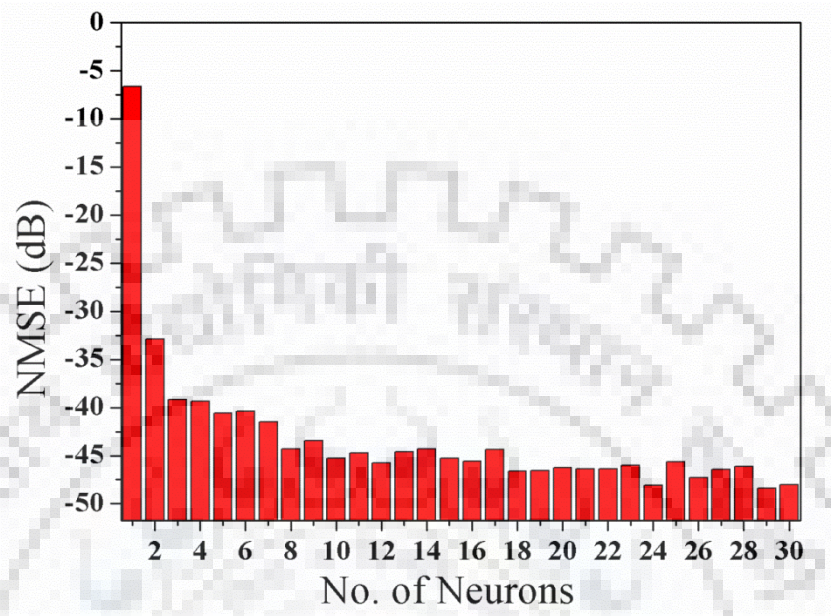

Figure 3.8: Convergence of model with respect to number of neurons.

To showcase suitability and superiority of the proposed model in terms of inverse modeling of SPC based modulator, it is compared with the state-of-art non-linear models proposed in the literature. Memory polynomial model (MP) ([114], eq.6) is an established popular model for non-linear DUTs, such as power amplifiers, however it does not have provision for *I*/*Q* imbalance and interference. The Parallel Hammerstein model (PH) [134] is a modification over MP model to include effects of *I*/*Q* imbalance in a quadrature modulator, however there is no provision for interference between *I* and *Q* streams. A modified Cartesian Memory Polynomial (MCMP) model is proposed in [30], which is adaptation of MP model for SPM application and includes provision for non-linearity as well as interference terms.

Table 3-1 shows the modeling performance of the proposed and existing models in terms of NMSE.

Table 3.1: Performance comparison of various models.

S. No.	References No.	Model Type	NMSE (dB)
1	[114]	Memory Polynomial ([114], eq. (6))	-16.3
2	[134]	Parallel Hammerstein (PH) model	-27.1
3	[30]	Modified Cartesian Memory Polynomial (MCMP)	-43.6
4	This Work	Proposed Neural Network Based Model	-47.1

As expected, PH model has better performance over MP model, however both the models are not able to provide sufficient NMSE performance for DPD application. MCMP model is able to provide good modeling performance, however proposed model has almost 3.5 dB better NMSE performance over MCMP model. It may be due to the fact that the proposed NN model is inherently capable of mapping interference terms such as $I(n\text{-}M_{\mathrm{p}})*Q(n\text{-}M_{\mathrm{Q}})$, where M_{P} and M_{Q} represent different memory terms. Whereas, MCMP model is rigid to model only $I(n\text{-}M_{\mathrm{P}})*Q(n\text{-}M_{\mathrm{P}})$ terms due to selected polynomial topology.

3.5 **Corrections of Linear and Non-linear Distortions in Six-Port Modulator**

After the extraction of the weights for *NN* based predistorter, the original baseband *I* and *Q* signals are processed through the predistorter before sending to the SPM. As the predistorted signal is synthesized to compensate for interference as well as non-linear distortion, the output signal should theoretically be free from distortion. In practice, the level of suppression of distortion at the output of modulator depends on the accuracy of model which can be judged by NMSE. Since the NMSE obtained in this case is quite good in the context of the existing literature, one can expect good performance. The performance in terms of 64 QAM @100 Mbps LTE transmissions can be judged by ACLR and EVM as described before. The measurement is done in the same hardware setup of Figure 2.11 with the predistortion applied in digital domain.

Figures 3.9 and 3.10 show the distortion mitigation in terms of gain and phase compression characteristic after applying proposed DPD scheme. Figure 3.9 shows that AM/AM distortion is minimized with the proposed distortion mitigation scheme in comparison to the case where no DPD is applied. Figure 3.10 shows phase compression characteristic in presence and absence of DPD. One can see that in the absence of DPD, the modulator exhibits severe AM/PM distortion which is minimized after applying DPD. Figure 3.11 shows the measured modulated spectrum of 64-QAM data @100 Mbps complying LTE standard. It also shows the case with various memory effects under consideration.

One can see that as memory depth increases from *M*=0 to 2, the ACLR improves. The zoomed versions of sidebands also show that the side bands have different shapes and ACLR values for *M*=0 and *M*=1, which indicates memory effect is not well compensated. However, in case of *M*=2, the spectrum at both side bands are similar and ACLR values are also similar indicating well compensation of memory effect. These ACLR values are measured at 15 MHz offset in lower and upper side of center frequency, respectively. One can see an improvement of more than 16 dB in ACLR with respect to the spectrum of Figure 2.12 where no digital correction is employed. These ACLR value for the case of *M*=2 easily qualify the industry requirement of -44.2 dBc as described in [88]. One can also see that carrier leakage at the modulated output has been reduced after employing this digital correction.

Figure 3.12 shows constellation diagram of demodulated RF carrier captured from the output of SPM after and before digital correction. The EVM measured from the constellation after DPD is 1.37%, which is quite below the requirements of LTE transmission as given in [89].

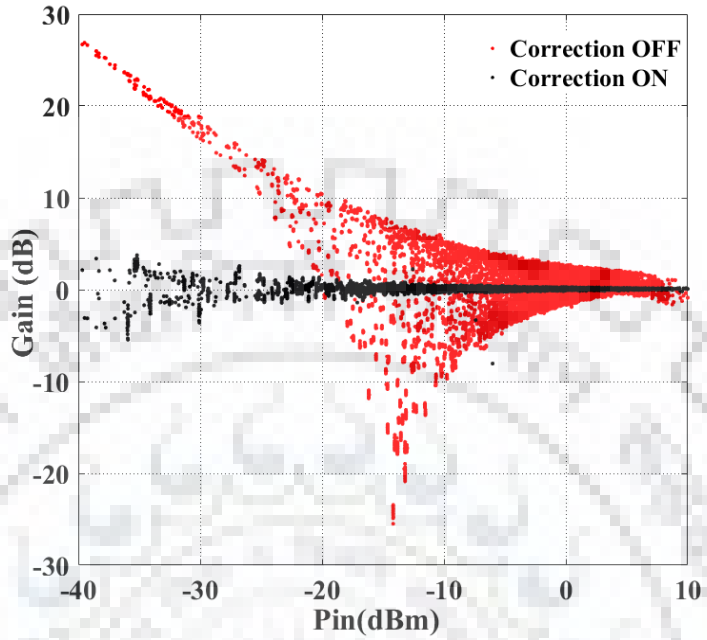

Figure 3.9: Measured response of modulator with and without DPD correction: AM/AM distortion.

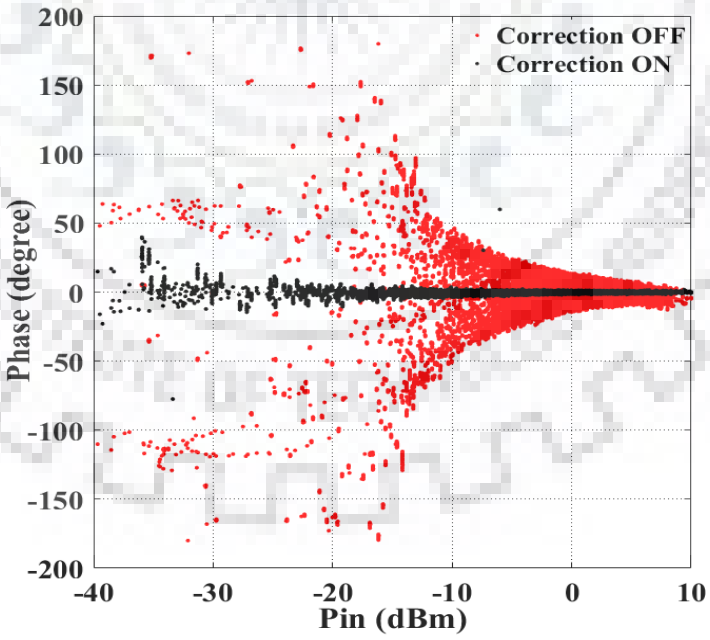

Figure 3.10: Measured response of modulator with and without DPD correction: AM/PM distortion.

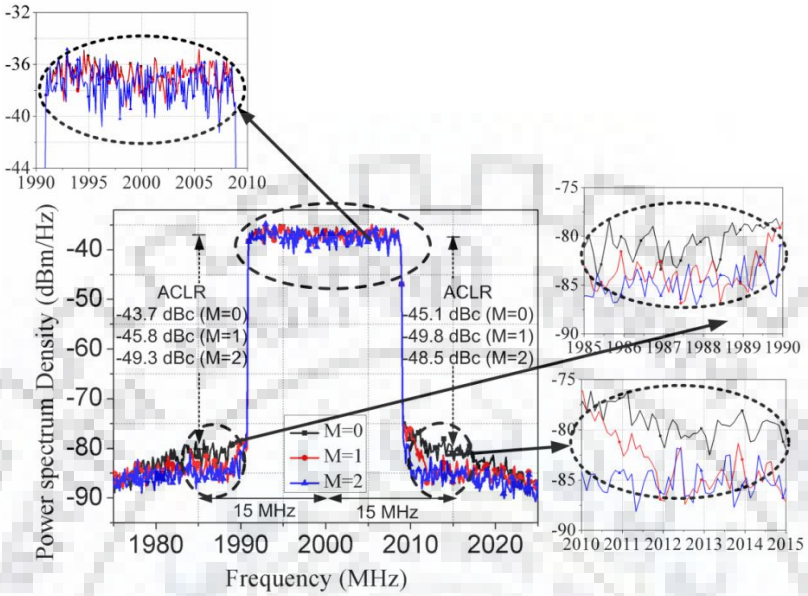

Figure 3.11: Measured modulated spectrum of SPM with 64 QAM @ 100 Mbps with proposed scheme incorporating various memory depth.

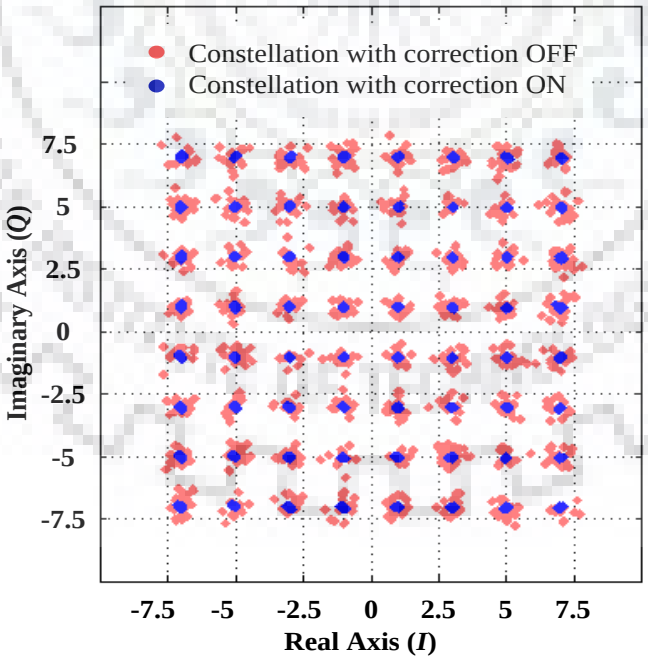

Figure 3.12: Measured constellation diagram of modulated output of SPM with 64 QAM @ 100 Mbps in presence and absence of digital correction.

The proposed scheme is also tested with high speed as well as higher order QAM data. Figure 3.13 shows the modulated spectrum of 256-QAM data of 400 Mbps speed modulated with SPM using setup of Figure 2.11.

One can see from Figure 3.13 that without any digital correction, the ACLR of -34.3 dBc and -36.5 dBc are measured at 50 MHz offset in lower and upper side of center frequency, respectively. Whereas, after digital correction, the ACLR of -47 dBc and -48 dBc are measured at the same frequency offset in lower and upper side of center frequency respectively. This corresponds to an improvement of 12.3 dB and 10.8 dB at 50 MHz offset in lower and upper side of center frequency, respectively.

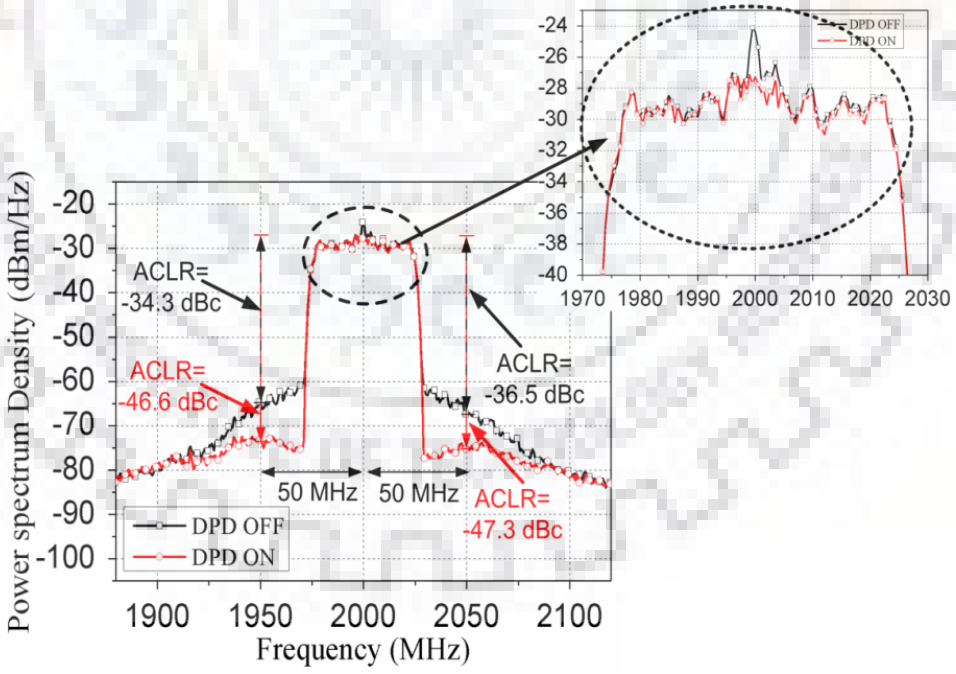

Figure 3.13: Measured modulated spectrum of SPM with 256 QAM @ 400 Mbps. in presence and absence of digital correction.

Figure 3.14 shows the constellation diagram of 256-QAM data of 400 Mbps speed modulated with SPM using setup of Figure 2.11. Figure 3.14 shows that without digital correction, the data in constellation diagram is scattered resulting into 19.1% EVM. However, after digital correction, the EVM reduces to 2.15%.

Table 3-2 reports the measured EVM for the proposed SPM setup and compare it with prior arts. One can see from the Table 3-2 that even for higher order QAM and high speed data, the proposed setup has better EVM as compared to the state of art.

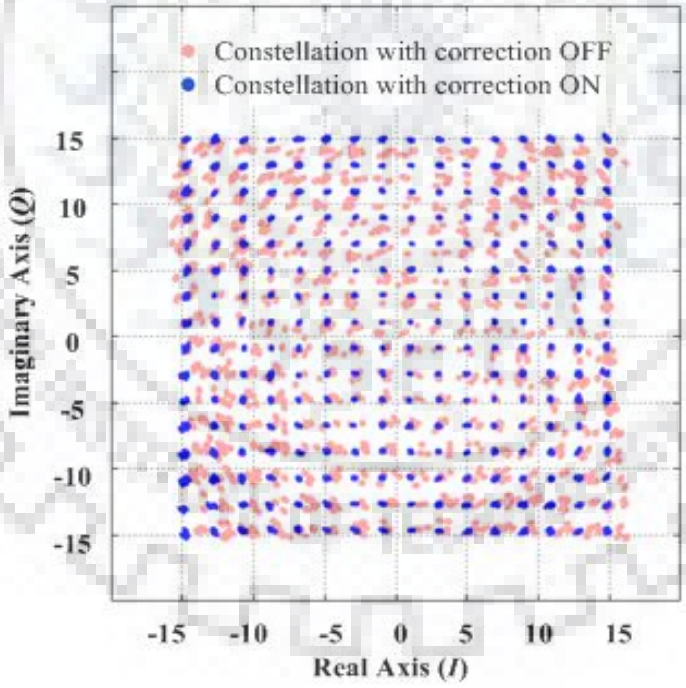

Figure 3.14: Measured constellation diagram of SPM with 256 QAM @ 400 Mbps. in presence and absence of digital correction.

Table 3.2: Performance comparison with state-of-the-art.

S. No.	References No.	Mod. Scheme	Data Rate (Mbps)	BW (MHz)	Carrier Freq. (GHz)	EVM (%)	ACLR (L/U) (dBc)	Output Power (dBm)
1	[21]	16-QAM	200	10	4.2	6.99	NA	NA
2	[24]	16-QAM	400	100	7.5	7.15	NA	NA
3	[30]	16 - QAM	NA	4	2.6	2.7	~ -43.0/-44.0**	NA
		64-QAM	NA	10	2.6	2.9	~ -46.0/-47.0*	
4	[65]	QPSK	20	50	2.4	3.0	NA	NA
5	This work	64 - QAM	100	20	2	1.37	-49.3/-48.5	-11.2
		256-QAM	400	55	2	2.15	-46.6/-47.3	-10.5

NA: Not available, L: Lower, U: Upper *Offset@10 MHz, **Offset@4 MHz

3.6 **Conclusion**

The Chapter presents linear/non-linear distortion characterization and correction setup for SPM. A *NN* based model is trained with *I, Q* data to model the captured distortion of the SPM. An ILA of DPD is employed to correct the linear and non-linear distortion in low cost analog SPM. Therefore, with a proper distortion characterization and mitigation setup, one can use low-cost, low-power, simplified six-port based modulator for high end applications such as 5G wireless communication.

Chapter Four: Low Complexity Polynomial Based Model for Linear and Non-linear Distortion Mitigation in Six-Port Modulator

4.1 **Introduction**

This chapter presents low-complexity QIMP model and its variant for distortion mitigation in SPM. This model has better performance as compared to the state-of-art polynomial based model. In comparison to neural network based behavioural modelling of chapter 3, this model offers low resource consumption in terms of signal processing. The performance of the model is validated with hardware prototype as shown in Figure 2.2. The test-bed developed in chapter 2 and as shown in Figure 2.11 is used for generating *I* and *Q* data corresponding QAM as well as LTE signals which are later fed to SPM. The same set-up will be used to characterize hardware imperfections in passive SPC as well as diode non-linearity. The QIMP model and its variant will be used for behavioral modelling and DPD application [135]-[161]. The resource consumption by applying DPD using the QIMP model and its variant is also analyzed in this chapter. The performance is compared with the state of art in terms of EVM and ACLR which are well below the specified range.

4.2 **Behavioral Modeling and DPD of Six-Port Modulator Using Polynomial Based Model**

In case of imperfect SPC realization, the modulator output comprises of cross-talks between *I* and *Q* data. When the system has no *I,Q* imbalance and only non-linearity is a concern, following memory polynomial (MP) model is a popular choice [146].

$$y_{MP}(n) = \sum_{j=0}^{K} \sum_{m=0}^{M} c_{k,j} x(n-m) \left| x(n-m) \right|^{j} \tag{4.1}$$

where y_{MP} is the output of the predistorter, *K* is the highest non-linearity order and *M* is the memory order. In the presence of DC offset, phase and amplitude imbalance in a quadrature modulator, the modified polynomial model, named Parallel Hammerstein (PH) model is given as [134], *x* is baseband complex data (*I*+*jQ*).

$$y_{PH}(n) = a + \sum_{j=0}^{K} \sum_{m=0}^{M} b_{k,m} x(n-m) \left| x(n-m) \right|^{j} + \sum_{j=0}^{K} \sum_{m=0}^{M} c_{k,m} x^{*}(n-m) \left| x(n-m) \right|^{j} \tag{4.2}$$

However, in case of SPM, the imperfection in realizing SPC may result in cross-talk, which may not be directly related to quadrature imbalances. Therefore, model given by (4.2) is not sufficient, where only gain and phase between *I* and *Q* need to be maintained.

4.2.1 FIR Approach to Six-Port Modulator

It is to be noted that (4.1) and (4.2) impose condition of quadrature relation between *I* and *Q*, i.e. models are dependent on *x*. Moreover, there is no provision of cross-interference between *I* and *Q* data streams. Above conditions are true for quadrature modulators. However, as discussed in chapter 2, in case of imperfect SPC realization, the modulator output comprises of cross-talks between *I* and *Q* data. Focusing on this requirement, a QIMP model is proposed for SPM modeling as,

$$y_{QIMP}(n) = y_I(n) + jy_Q(n) \tag{4.3}$$

where, $y_I(n)$ and $y_Q(n)$ are given by

$$\begin{aligned} y_I(n) &= \sum_{k=0}^{K}\sum_{j=0}^{k}\sum_{m=0}^{M} b_{k,j}^{m}\, x_I^{\,k-j}(n-m)\, x_Q^{\,j}(n-m) \\ y_Q(n) &= \sum_{k=0}^{K}\sum_{j=0}^{k}\sum_{m=0}^{M} c_{k,j}^{m}\, x_Q^{\,k-j}(n-m)\, x_I^{\,j}(n-m) \end{aligned} \tag{4.4}$$

x_I and x_Q are input baseband signal in in-phase and quadrature-phase components. $b_{k,j}^{m}$ and $c_{k,j}^{m}$ are the coefficients to be identified for the in-phase and quadrature-Phase model outputs respectively. It is to be noted that the above model utilizes real-valued model identification as opposed to (4.1) and (4.2), which allows the modeling of cross-terms. *K*

is the non-linearity order and *M* is memory length of the QIMP model. Each output in Equation (4.4) can also be represented as a Matrix equation Y=AX, where Y is output baseband signal vector, A is coefficient vector and X is the input matrix. The coefficients can be evaluated using least squares (LS) solution as follows:

$$\mathrm{A} = (\mathrm{X}^{H}\mathrm{X})^{-1}\mathrm{X}^{H}\mathrm{Y} \tag{4.5}$$

Each output model in (4.4) is a function of present and previous instances of input signal only and therefore can be considered (FIR) presentation of the model.

4.2.2 IIR (Recursive) Approach to Six-Port Modulator

Infinite impulse response (IIR) filters are known to provide better modeling performance and IIR representation of (4.3) can be given as following recursive model

$$y_{QRQIMP}(n) = y_I^R(n) + jy_Q^R(n) \tag{4.6}$$

where,

$$y_I^R(n) = \sum_{e=0}^{E}\sum_{d=0}^{e}\sum_{g=0}^{G} b_{e,d}^{g}\ f_{e,d}^{g}\left(n-g\right) - y_I(n)\sum_{k=0}^{K}\sum_{j=0}^{k}\sum_{m=0}^{M} d_{k,j}^{m}\ \ f_{k,j}^{m}\left(n-m\right) \tag{4.7}$$

$$y_Q^R(n)=\sum_{e=0}^{E}\sum_{d=0}^{e}\sum_{g=0}^{G}c_{e,d}^{g}\ f_{e,d}^{g}\left(n-g\right)-y_Q(n)\sum_{k=0}^{K}\sum_{j=0}^{k}\sum_{m=0}^{M}d_{k,j}^{m}\ \ f_{k,j}^{m}\left(n-m\right) \tag{4.8}$$

and

$$f_{V,W}^{u}\left(n-u\right)=x_Q{}^{V-W}\left(n-u\right)x_I{}^{W}\left(n-u\right) \tag{4.9}$$

K and *E* denote the non-linearity orders, *M* and *G* denote the memory depths for the FIR and IIR terms, respectively. It can be observed from (4.7) and (4.8) that for a captured input-output measurement data set, the model is linear with respect to coefficients. Therefore, the coefficients can be calculated using LS solution implemented as show in (4.5).

To provide a robust model in the ideal recursive topology, using the stored values of $x(n)$ and $y(n)$, the coefficients are extracted. However, for practical applications of behavioral model, $y(n)$ at the present instance cannot be known beforehand, which is a limitation when applying such recursive mode. To utilize recursive property for better modeling performance, this paper further proposes the use of a two- step method, where the QIMP model is extracted in a first step and the modeled output of QIMP model, is used as input to the recursive QIMP model in the second step, where $y_{QRQIMP}(n)$ denotes quasi recursive quadrature interface memory polynomial (QRQIMP) implementation.

4.2.3 Flow Chart Implementation

Figure 4.1 shows the flow-chart of the implementation. In the $y_{QRQIMP}(n)$ model, the first step provides a crude modeling while the second step offers fine- tuning of the coefficients. It is to be noted that the final stage of proposed model is directly dependent on input data as well as output of previous stage (error in previous step can be adjusted due to the presence of the input data in the final stage).

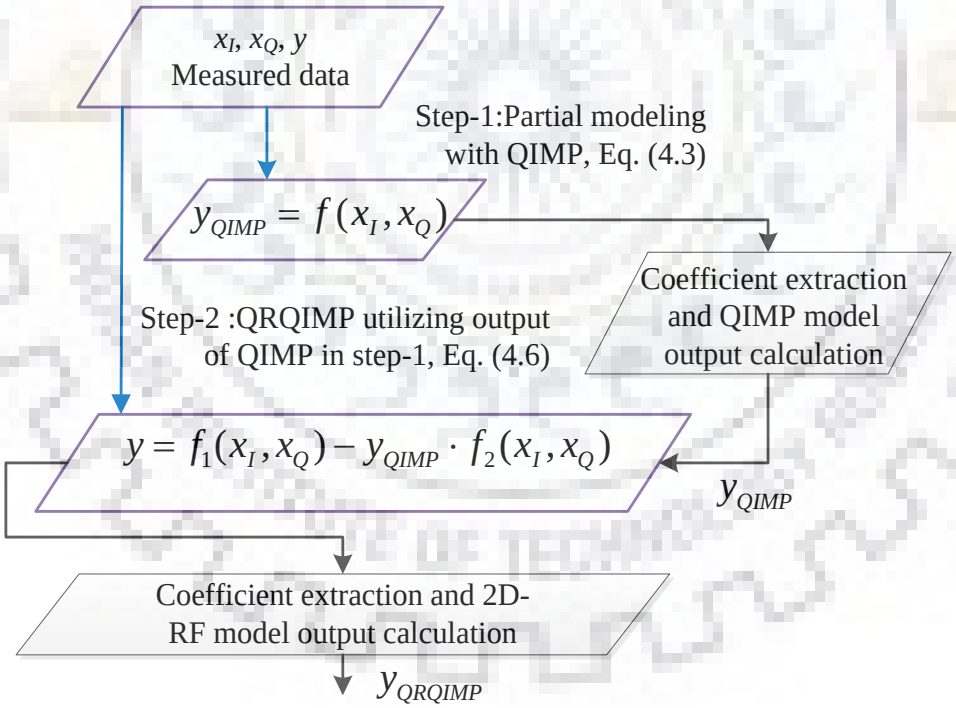

Figure 4.1: Model extraction scheme for QRQIMP model

The proposed model is evaluated in terms of NMSE. The NMSE is defined as mean square error between measured and modeled output normalized with respect to the sum of squared measured output.

The comparison between the QIMP and QRIMP model in terms of NMSE and number of coefficient is plotted in Figure 4.2 and 4.3.

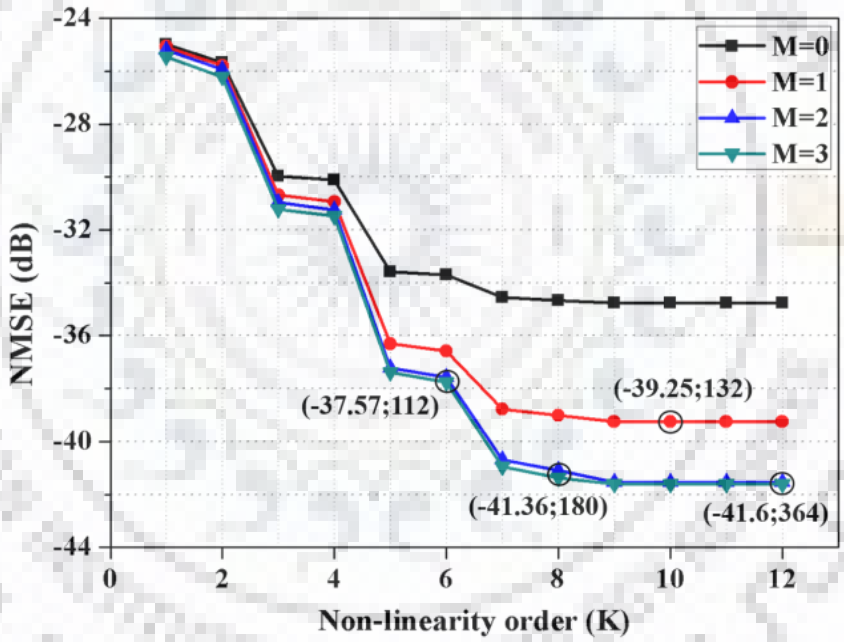

Figure 4.2: Variation of NMSE with respect to *K* for QIMP Model.

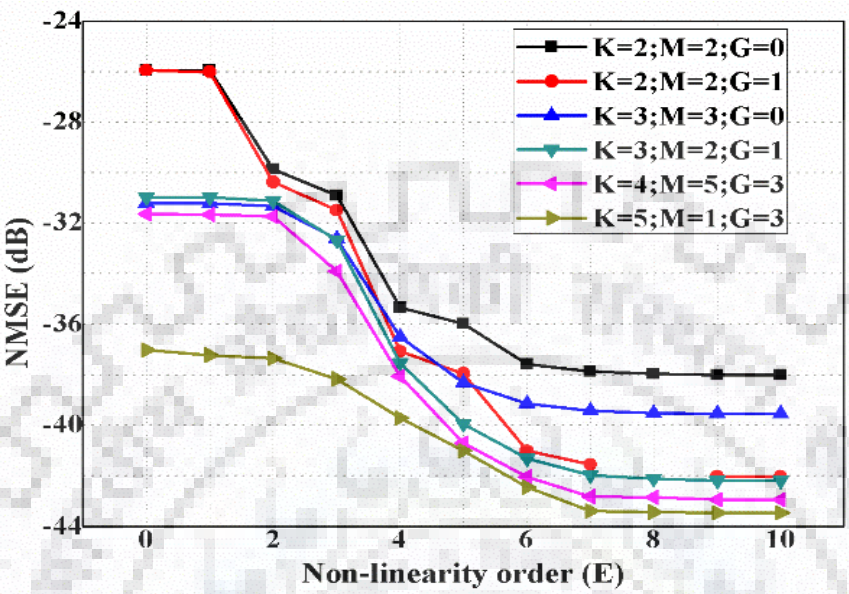

Figure 4.3: Variation of NMSE with respect to *E* for QRQIMP Model.

Although a thorough analysis of the model has been done for different combinations of *K*, *M*, *E* and *G*, a few of them have been incorporated in the Figure 4.2 and 4.3 for proof-of-concept.

It is evident from the Figure that the QRQIMP model requires less number of co-efficient as compared to the QIMP model for a given value of NMSE. In addition to that, the NMSE saturates after *M*=2 in case of QIMP with a best result of -41.6 dB. Whereas, in case of QRQIMP NMSE as high as -43.4 dB has been achieved with relatively less number of coefficients.

4.2.4 Computational Calculations

This clearly indicates the advantage of the proposed QRQIMP model over the previously

proposed models. The memory of the model for QIMP and QRQIMP model can be calculated by using the relation,

$$\text{Memory of the model} = \text{Matrix size} \times \text{Bit Resolution} \tag{4.11}$$

where,

$$\text{Matrix Size} = \text{No. of Samples} \times \text{No. of Coefficient.} \tag{4.12}$$

Table 4-1 shows the modeling performance of the proposed and existing models in terms of NMSE for the same number of coefficients. QIMP model uses K=9 and M=4 (no. of coefficients 275, performance is similar for higher no. of coefficients) where its convergence curve saturates, while QRQIMP model uses K=3 and M=1 in first step and E=8 and G=2 (no. of coefficients 290) in second step with an improved NMSE value. These values of NMSE are obtained for 20 MHz LTE signal using 64 QAM. One can see from Table 4-1 that the proposed QIMP& QRQIMP models have superior performance over the state-of-the art. One can see the NMSE of the proposed QIMP and QRQIMP is below -40 dB which is quite good in comparison to the other popular model.

Table 4.1: Performance comparison of various models

S. No.	Model Type	NMSE (dB)
1	Memory Polynomial	-16.31
2	Quadrature-Interference memory Polynomial (QIMP)	-41.7
3	Quasi Recursive Quadrature-Interference Memory Polynomial (QRQIMP)	-43.1
4	Parallel Hammerstein (PH) Model	-27.17

Table 4-2 shows the Memory of the models for different models QIMP, QRQIMP in Mega Bits and comparison for different parameters like its matrix size, no. of coefficients, bit resolution and memory of the model.

Table 4.2: Memory of the models for different models

S. No.	Name of the Models	Matrix Size	No. of Coefficients	Bit Resolution	Memory of the Model
1	QIMP	156672	275	64	344.68MB
2	QRQIMP	156672	290	64	363.48MB

4.3 **Measurement Results**

The QRQIMP model is implemented in digital domain to predistort baseband *I* and *Q* data. This predistorted data is then sent to SPM using setup shown in Figure 2.11. The measured results of 16 QAM modulated data using SPM shown in Figure 4.4.Figure 4.4

shows measured spectrum of modulated carrier, where one can see an improvement of at least 10 dB in terms of ACLR when DPD is ON. Figure 4.5 shows the scattering of *I*/*Q* data without DPD. This corresponds to an EVM of 5.7%, which reduces to 1.1% when DPD is ON.

Figures 4.6 and 4.7 show performance of SPM for modulating 64 QAM data complying LTE standard. One can see from Figure 4.6 that without DPD, the ACLR performance of SPM is poor and does not qualify the industry requirement of -44.2 dBc for LTE transmission as described in [88]. After applying DPD, the ACLR of -48.10 dBc and -48.43 dBc are measured at 20 MHz offset in lower and upper side of center frequency respectively as shown in Figure 4.6. Therefore, after applying the proposed DPD technique, the SPM qualifies spectral mask requirement for LTE standard.

Figure 4.7 shows the scattering of *I/Q* data without DPD. The EVM of modulated data without DPD is 7.4%. However, it reduces to 1.2% when DPD is applied. This is quite less then the requirement of 8% EVM for 64-QAM in LTE transmission as described in [90]. However, this requirement of 8% is set for the entire transmitter, the EVM of modulator must be kept as low as possible [90]. Typically, if the EVM degradation of the modulator and the DACs is limited to around 1%, it will provide sufficient headroom to non-linear PA in subsequent stage which will add significant distortion further [90].

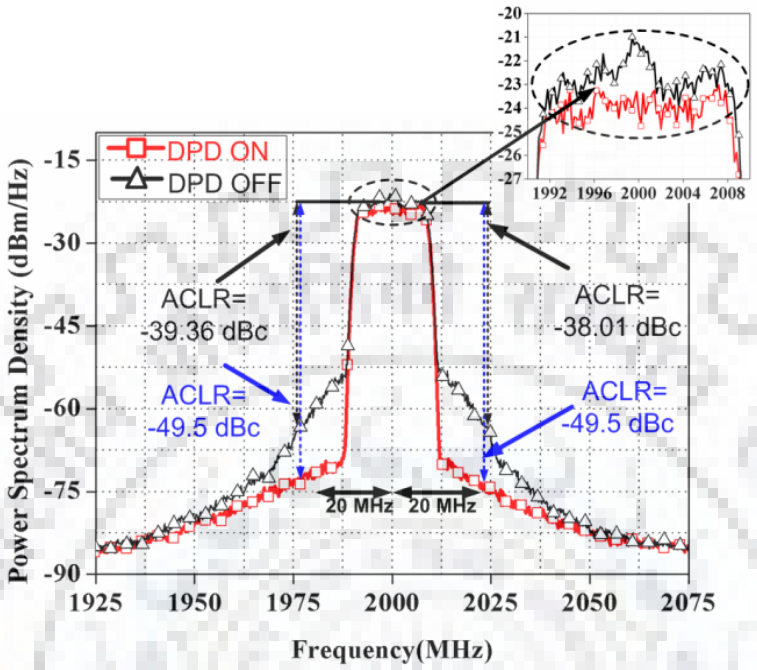

Figure 4.4: Measured modulated spectrum of SPM with 16 QAM.

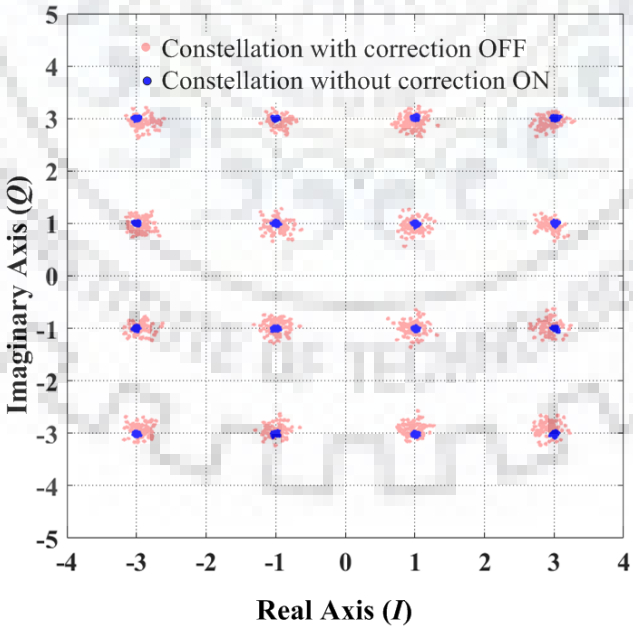

Figure 4.5: Measured performance of SPM with 16 QAM in terms of constellation diagram.

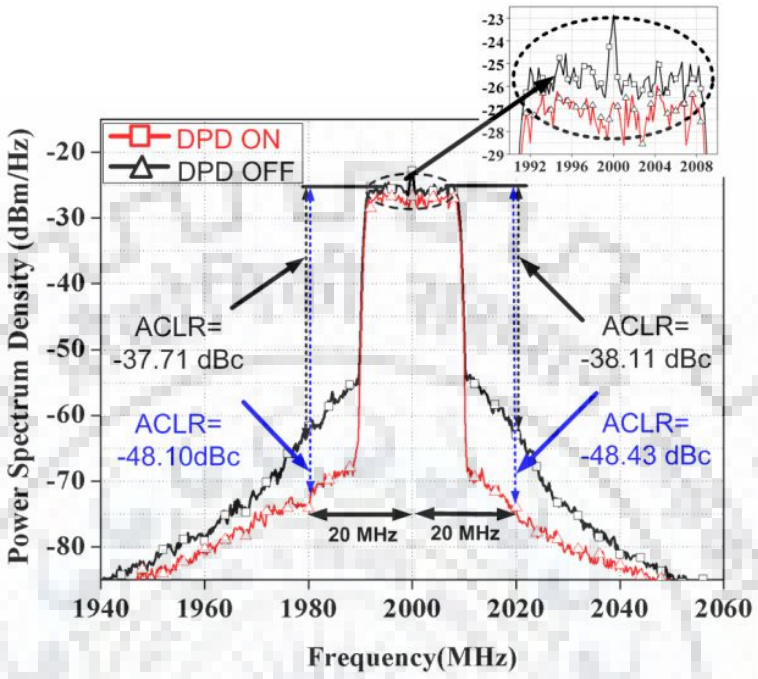

Figure 4.6: Measured modulated spectrum of SPM with 64 QAM.

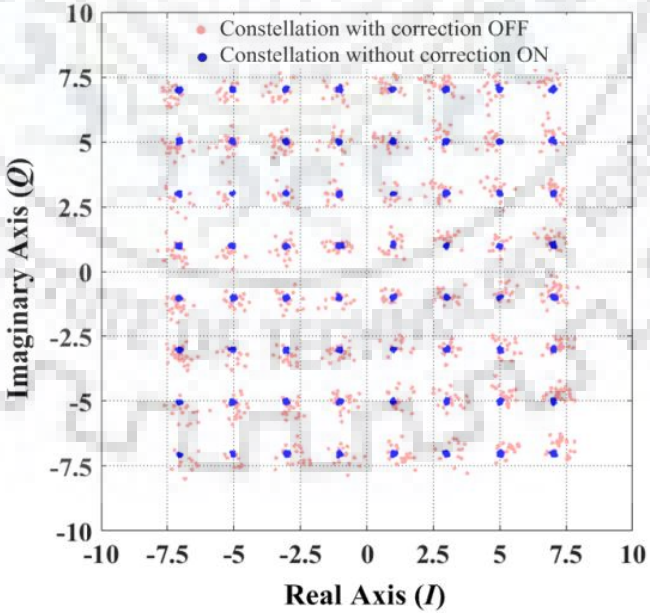

Figure 4.7: Measured performance of SPM with 64 QAM in terms of constellation diagram.

Table 4-3 shows the Comparison of Neural Network with Proposed Polynomial Models.

Table 4.3: Comparison of neural network with polynomial model

S. No.	Model Type	Mod. Scheme	Data Rate (Mbps)	BW (MHz)	Carrier Freq. (GHz)	EVM (%)	ACLR (L/U) (dBc)	Complexity
1.	Neural Network	64 –QAM 256-QAM	100 400	20 55	2 2	1.3 2.15	- 49.3/- 48.5 - 46.0/- 47.0	More complex to implement on FPGA
2.	QRQIMP MODEL	16 -QAM 64 -QAM	67.2 100	20 20	2 20	1.1 1.2	- 49.5 /- 49.5 - 48.1 /-48.4	Less complex to implement on FPGA

Table 4-4 shows the performance of proposed scheme in comparison to the state of art. One can see from Table 4-4 that proposed scheme presents good performance in terms of EVM as compared to the state of art.

Table 4.4: Performance comparison with state-of-the-art

S. No.	Reference No.	Mod. Scheme	Load Type	BW (MHz)	Carrier Freq. (GHz)	EVM (%)	ACLR (L/U) (dBc)
1	[21]	16- QAM	Switch	10	4.2	6.99	NA
2	[22]	QPSK	Switch	10	4.2	4.0	NA
3	[24]	16-QAM	Diode	100	7.5	7.15	NA
4	[30]	16 -QAM 64- QAM	Diode Diode	4 10	2.6 2.6	2.7 2.9	~ - 43.0/- 44.0** ~ - 46.0/- 47.0*
5	[31]	16- QAM	Transistor	NA	2.5	10	NA
6	[33]	QPSK 256-QAM	Transistor	100 50	7-8	<18	- 42.0
7	[35]	64-QAM	Transistor	NA	2.5	7.0	NA
8	[65]	QPSK	Transistor	10	2.4	3.0	NA
9	This work	16 -QAM 64 -QAM	Diode Diode	20 20	2.0 2.0	1.1 1.2	- 49.5 /- 49.5 - 48.1 /-48.4

NA: Not available, L: Lower, U: Upper *Offset@10 MHz, **Offset@4 MHz

4.4 **Conclusion**

The Chapter presents a novel behavioral model for correcting the linear and non-linear distortion in SPM using DPD. The chapter identifies the sources of distortion in SPM, which can provide an understanding of correct modeling requirements for DPD. The

measured performance of proposed model and DPD scheme for various type of modulation has been demonstrated in support of the theory.

Chapter Five: Conclusion and Future Scope

5.1 **Introduction**

This Chapter presents conclusion of the thesis and future scope of the work presented in the thesis. The thesis is concluded with the discussion over the achievements of the objectives laid on the first chapter. The thesis also compares and benchmark the presented work against the state-of-art.

5.2 **Thesis Conclusion**

The overall objective of this thesis is to characterize the effect of hardware imperfections, linear and non-linear distortions associated with the conventional topology of SPM. Specifically, the topology where schottky diodes are used as variable loads is investigated in this thesis. In order to perform measurement based characterization, the hardware of SPM is developed using off-the-shelf schottky diodes operating as variable loads. The passive SPC is realised using microstrip transmission lines using conventional printed circuit board technology. An instrument based test-bed is developed using VSG and VSA, where, the DACs at the rear end of VSG can directly feed the baseband input signals to SPM hardware. The test-bed is capable of generating modulated signals complying wireless standards such as LTE. The SPM hardware is tested with these modulated signals and the distortions are characterized in terms of AM/AM and AM/PM

conversion data. These AM/AM and AM/PM characteristics representing gain and phase variation with input drive are used to develop behavioural model of SPM. The SPM has several distortions apart from diode non-linearity. These distortions arise due to imperfect differential drive of *I* and *Q* data and imperfect s-parameter matrix realization of passive SPC. Combined effect of these distortions led to carrier leakage, cross talk between *I* and *Q* as well as added non-linearity and DC leakage to *I* and *Q* data. The conventional models used for capturing linear and non-linear distortions do not fit in case of SPM due to its different architecture and mode of operation. Therefore, the source of distortions and their interaction is different in case of SPM. This thesis first uses neural network to model the behaviour of SPM. The model fits well to the characteristics of SPM which can be seen with good NMSE performance. The model is later used for DPD application, which greatly improves the performance of six-port model in terms of EVM as well as ACLR. The neural network based behavioural model and DPD is quite accurate, however it suffers with computational complexity and high resource consumption when implemented in digital signal processing platform. Therefore, a polynomial based model is investigated in later chapter which can be implemented with low resource consumption. This model, when applied in DPD application, still provides good performance in terms of EVM and ACLR qualifying the requirement by modern wireless standards such as LTE. Therefore, the thesis fulfils all the objectives laid in first chapter resulting into well thought of DPD schemes to mitigate the distortions existed inherently in the SPM. These DPD schemes are tested experimentally with a test-bed which

validates the suitability of proposed schemes to enable SPM for modulation complying the wireless communication.

5.3 **Future Scope**

The thesis uses a conventional architecture of SPM. This topology suffers with low bandwidth and therefore new architectures of passive SPC can be investigated to enhance the bandwidth. Moreover, in order to scale the SPM application to mm-wave frequencies, the SPC can be modified in future to have minimum effect of s-parameter imperfections in the performance of SPM. Moreover, in-situ characterization of diode can be more useful in such case to identify the diode non-linearity and isolate its effect from rest of the imperfections of the SPM hardware. This study will help in understanding the effect of diode non-linearity and calibrating it while SPM is in operation.

It is worth mentioning that the SPM architecture based on variable loads suffers with diode non-linearity but can provide higher QAM modulation with simplified architecture. Therefore, switch based SPM architecture seems to be more viable solution for mm-wave frequency, where, low order QAM can be used to modulate very high speed data. Moreover, the bandwidth is not restricted with DAC speed in such architecture and therefore, it can be explored as new solution for upcoming 5G communication. Studying the effects of imperfections of SPC in case of such architecture can also be future scope of this work.

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