FPGA PROTOTYPING FOR MICROGRID PROTECTION

Ph.D. THESIS

by

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STUDENT'S DECLARATION

I hereby certify that the work presented in the thesis entitled "**FPGA PROTOTYPING FOR MICROGRID PROTECTION"** is my own work carried out during a period from July, 2014 to June, 2019 under the supervision of Dr. Vishal Kumar, Associate Professor and Dr. Rajendra Pratap Adjunct Faculty Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in the thesis has not been submitted for the award of any other degree of this or any other Institute.

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Dated: **June 06, 2019**

SUPERVISOR'S DECLARATION

This is to certify that the above mentioned work is carried out under my supervision.

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ABSTRACT

The recent advancement of digital technology is the re-configurable hardware i.e. field programmable gate array (FPGA), programmed by Hardware Description Language (HDL) is used for high-speed applications. It has credentials for developing intelligent electronic devices, which are used in the power system components, and smart grid applications i.e. fast relay for the protection of the microgrid (MG) asking high computational demand, low latencies, reconfigurability, high bandwidth and parallel processing. Some inherent benefit of the FPGA device is the parallelism of hardware that increases the execution speed compared to sequential software architecture based technologies (μP and μC). Due to these predominant features, the FPGA based digital relays are being considered for the protection of MGs.

MGs provides a platform for integration of various distributed generators (DGs) and renewable energy sources (RESs) like solar PVs and wind generators, loads and storage devices. These DGs and RESs serve multiple purposes viz. reducing the carbon footprint from the environment, reachability to remote demand locations, quick installation and low-cost maintenance etc. The MG is usually connected to the utility grid through a single bus called the point of common coupling (PCC) and hence, is capable of operating both in synchronism with the utility grid known as grid-connected mode and as an autonomous power island i.e. standalone mode. The small-scale MGs provide uninterrupted power supply to the end user during the period of power outages, emergencies and failures of the utility grid due to any abnormality or a fault occurring in the utility grid. There are several challenges for reliable operation of a MG in the field of monitoring, controls, and protection. Among these, the device development for the protection of the MG has been addressed in the present work.

The existing overcurrent protection relays (OCRs) developed for passive distribution networks (radial network) are not applicable for active distribution networks viz. Microgrid (MG). Since the integrated distributed energy resources (DERs) are connected through power electronic interfacing (PEI) having fast dynamics, therefore, the MG is a low-inertial system. To overcome the stated problem, a fast relay is required for the protection of MG that can isolate the faulty section, detect its mode of operation and adapt threshold settings as per the operating mode. Protective hardware is required to be developed that can sense the faster dynamics within MG and also have the feature of parallel processing by which the computation time for decision making is reduced. The FPGA is such an electronic device that is used in the power system

industry and smart grid applications asking for high computational demand, low latencies, reconfigurability and parallel processing. Due to these predominant features, the FPGA based digital relays are being considered for the protection of the MGs. In the present work, the FPGA based prototyping has been used for different block of OCR viz. DC-offset module, anti-aliasing filter, DFT filter module, harmonic detection module and relay emulation module are implemented with a higher degree of accuracy at low cost.

Conventional OCRs are mostly used for the protection of the radial distribution network. However, in case of microgrid protection, OCRs maloperate due to the bidirectional power flow, the need of directional feature of the relay has become necessary. Therefore, the directional feature is added to the developed OCR prototype. Here, a digital phase detection module has been developed for the estimation of direction of current flowing through the power system network using a zero-crossing detector. A parallel architecture for phase and tripping time computation has been used in the proposed design that makes the developed relay faster by reducing the computation time of the algorithm. Here also, performance of the DOCR is tested by creating the faults at different locations with different values of time dial settings and plug-point-multiplier. Hardware-in-loop (HIL) verification of the relay is carried out with the real-time-digital simulator (RTDS) with FPGA prototype. The results are compared with the standard DOCR of the RTDS which verify the successful operation of the designed relay under different fault conditions.

Islanding is the condition, which occurs when a portion of the distribution network (or MG) is disconnected from the utility grid and operates independently with the help of local DGs and RESs. Generally, two types of MG islanding occur i.e. intentional and unintentional. The intentional islanding is mainly performed to carry out some maintenance works within the MG and for the safety of the working personnel; whereas the unintentional islanding occurs due to the utility grid blackout by equipment failure, natural disaster or any abnormality in the power system. As per the suggested standard viz. UL-1741, IEC-62116 and IEEE 1547^{TM} islanding must be detected and the active DGs are isolated from the MG within 2-seconds after detecting the islanding. Hence, it is an essential requirement to develop a fast relay that can detect the islanding (by sensing variation in parameters) within the stipulated time interval as well as take necessary action i.e. either isolate the affected section/DG of the MG (with non-critical loads) by generating the trip signal. In present work, the FPGA prototype for islanding detection based on the islanding discrimination factor (IDF) using the periodic maxima of superimposed voltage components is developed. A modular design approach is used to implement the islanding

detection technique (IDT) algorithm. Verilog HDL has been used to optimize the hardware resources and minimize computational complexity. HIL verification of the IDT has been performed for islanding and non-islanding events with a microgrid test system developed on RTDS. The performance of the prototype has been verified under various test cases viz. for both islanding and non-islanding events.

Now, the magnitude of a fault current depends on the operating mode of the MG as well as number and types of the integrated DGs placed within the MG. The contribution of the fault current by rotating machine-based sources is higher than that of PEI DERs as compared to their respective normal rated current. The magnitude of fault current is 6.0-10.0 p.u in the rotating machine whereas its magnitude is lower i.e. up to 1.0-2.0 p.u in case of PEI interfaced DERs. However, in the grid-connected mode of operation, the magnitude of fault current is greater than the magnitude of the fault current in the islanded mode of operation. Also, the trip time is more in the case of a standalone mode in comparison with the grid-connected mode. Hence, mode-adaptability of the OCR is inevitably required for the reliable operation of MG, which can be performed by changing the threshold setting i.e. pick-up current (*Ip*) setting of the OCR. In this work, a hardcore reconfigurable multifunctional relay is designed, which is used for the detection of operating modes of the MG as well as mode adaptation within the MG. Some additional functional modules viz. voltage unbalance module, rate of change of frequency (ROCOF) module and a soft controller are designed on the FPGA and added in the developed OCR prototype. HIL verification of the developed prototype is performed with the RTDS under various test conditions viz. under different power mismatches.

Lastly, the prototype of a communication assisted adaptive relay (CAAR) is developed by adding a communication feature with the designed OCR to achieve mode adaptability of the relay installed at various DG located remotely. The status of these modes and the working status of the DGs are communicated through the wireless network. Here nRF24L01 wireless modules are used as the transmitter and the receiver of the CAAR. Performances of the CAAR prototype has been verified in HIL on a MG test system under the environment of RTDS. Different test cases i.e. operating modes of the MG, faults at different locations, types of faults and relay coordination are tested to validate the functionality of the developed prototype of CAAR. In the present work, the FPGA based prototype of the overcurrent relay (OCR) with its internal components viz. DC-offset module, anti-aliasing filter, DFT module, harmonic detection module and relay emulation module are developed with a higher degree of accuracy and low cost. Here, Verilog HDL is used to optimize the hardware resources and minimize

computational complexity. Furthermore, the directional feature is added to the developed OCR prototype, which is works as directional-OCR. Here, a digital phase detection module is used for the estimation of the direction of current by a zero-crossing detector. Performance of the relay is tested by creating the faults at different locations with different values of time dial settings and plug-point-multiplier.

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(Praveen Kumar)

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LIST OF SYMBOLS

Symbols	Meaning
A,B,p	Characteristics Constant of the Relay
ADC_in	Input of the FPGA
Clk	Clock
f	Frequency
F_1	Fault at Location 1
F_2	Fault at Location 2
F_3	Fault at Location 3
F_4	Fault at Location 4
F_5	Fault at Location 5
FLT	Fault
F_n	Frequency of the Fundamental Component
F_s	Sampling Frequency
G	Generation Capacity
H	Moment of Inertia
I_F	Fault Current
Ip	Pick-up Current
k	Scaling Factor for ROCOF
N_0	Zero Sequence Component
N_1	Positive Sequence Component
N_2	Negative Sequence Component
N_A, N_B, N_C	Phase A,B,C Voltage
N_T	Target Number
P_b, Z_b, P_c, Z_c	Parameter Constant
$ROCOF_{th}$	Threshold Value of Rate of change of frequency
t	Relay Tripping Time
t_r	Relay Reset Time
TRIP_FPGA	Trip Signal Generated by FPGA Relay Prototype
TRIP_ROCOF	Trip Generated by Rate-of-change of Frequency Module
TRIP_RTDS	Trip Signal Generated by RTDS Relay
TRIP_VU	Trip Generated by Voltage Unbalance Module
t_s	Relay Set Time
VU_{th}	Threshold Value of Voltage Unbalance
X(0)	DC Component of Input Signal

$X(1)$	Fundamental Component of Input Signal
$X(2)$	2nd Harmonic Component of Input Signal
$x(n)$	Input Signal
Z	Accumulator
ΔP	Power Unbalances between Load and Generation

LIST OF ABBREVIATIONS

Abbreviations	Meaning
AAF	Anti-Aliasing Filter
ADC	Analog to Digital Converter
AFD	Active Frequency Drift
ANN	Artificial Neural Network
ASIC	Application Specific Integrated Circuit
BRAM	Block Random Access Memory
CAAR	Communication Assisted Adaptive Relay
CB	Circuit Breaker
CLB	Configurable Logic Block
CORDIC	Coordinate Rotational Digital Computer
CT	Current Transformer
DER	Distributed Energy Resource
DFT	Discrete Fourier Transform
DG	Distributed Generator
DOCR	Directional Overcurrent relay
DSO	Digital Storage Oscilloscope
DSP	Digital Signal processing
DT	Definite Time
DWT	Discrete Wavelet Transform
EI	Extreme Inverse
FPGA	Field Programmable Gate Array
GTAO	Gigabit Transceiver Digital Output Card
GTDI	Gigabit Transceiver Digital Input Card
HD	Harmonic Distortion
HDL	Hardware Description Language
HHT	Hilbert Huyang Transform
HIL	Hardware-in-loop
I/O	Input-output
IT	Inverse Time
ID	Internal Design
IDF	Islanding Discrimination Factor
IDMT	Inverse Definite Minimum Time
IDT	Islanding Detection Technique
IED	Intelligence Electronic Device
IP	Intellectual Property
ISE	Integrated Synthesis Environment
LG	Line-Ground
LL	Line-Line
LLLG	Line-Line-Line-Ground

LUT	Lookup Table
M	Plug Point Setting
MCB	Main Circuit Breaker
MG	Microgrid
MSPS	Mega Sample Per Second
NDZ	Non Detection Zone
NGC	Native Generic Circuit
OCR	Overcurrent Relay
PCC	Point of Common Coupling
PD	Phase Detection
PD	Phase Detection
PEI	Power Electronics Interfacing
PLC	Power Line Communication
PLC	Programmable Logic Controller
PLL	Phase Locked Loop
PMU	Phasor Measurement Unit
PSM	Power System Module
PV	Photovoltaic
RAM	Random Access Memory
REM	Relay Emulating Module
RES	Renewable Energy Sources
RMS	Root Mean Square
ROCOF	Rate of Change of Frequency
ROCOP	Rate of Change of Output Power
RPS	Real Power Shift
RTDS	Real-Time Digital Simulator
RTL	Register Transfer logic
SCADA	Supervisory Control and Data Acquisition
SFS	Sandia Frequency shift
SMS	Slip Mode Frequency Shift
SOPC	System on Programmable Chip
SVS	Sandia Voltage shift
TDS	Time Dial Setting
THD	Total Harmonic Distortion
TT	Transfer Trip
UCF	User Constraint File
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VI	Very Inverse
VT	Voltage Transformer
VU	Voltage Unbalance
ZCD	Zero Crossing Detector

CHAPTER 1: INTRODUCTION

1.1 Overview of Relay Design

An electromagnetic relay is a fundamental relay, which works on the principle of electromagnetic effects of the current flowing through the energised winding. This relay has many limitations such as high power consumption, contact problem, slow response, a high burden on instrument transformer and adaptability. Adaptation of the diodes, transistors, capacitors and inductors in the 1980s, added a new edge in the power system industry by introducing the solid state and static relays. These relays have comparatively low cost, small size and require less maintenance. Programmability and lack of communication features were the main disadvantages of these conventional relays. The microprocessor (μP) and the microcontroller (μC) based digital numerical relays were introduced in the 1990s. These relays facilitate software programmability and support multiple objectives realization on a single controller. However, the requirement of application specific integrated circuits, programmability, memory space, computational burden, limited speed and high cost were the main constraints of these relays.

The recent advancement of digital technology is the re-configurable hardware i.e. field programmable gate array (FPGA), programmed by Hardware Description Language (HDL) is used for high-speed applications. It has credentials for developing intelligent electronic devices, which are used in the power system components, and smart grid applications i.e. fast relay for the protection of the microgrid (MG) asking high computational demand, low latencies, reconfigurability, high bandwidth and parallel processing. Some inherent benefit of the FPGA device is the parallelism of the hardware that increases the execution speed compared to sequential software architecture based technologies (μP and μC).

1.2 Overview of Microgrid

The increased usage of the low-carbon emitting distributed generators (DGs) and renewable energy sources (RESs) like solar PVs and wind generators placed at the distribution level has changed the structure of the conventional power system network [1], [2]. These DGs and RESs serve multiple purposes viz. reducing the carbon footprint from the environment, reachability to remote demand locations, quick installation and low-cost maintenance etc. The term “microgrids” (MGs) was coined around one and a half decade ago, provides a platform for

integration of various diesel generators, RESs, loads and storage devices [3]. These MGs are usually connected to the utility grid through a single bus called the point of common coupling (PCC) and hence, are capable of operating both in synchronism with the utility grid known as grid-connected mode and as an autonomous power island i.e. standalone mode. The small-scale MGs provides uninterrupted power supply to the end users during the period of any power outage, emergencies and failures of the main/utility grid due to any abnormality or when a fault occurs in the utility grid.

Figure 1.1 gives a simple architecture of the MG that consists of different types of generation unit i.e. solar photovoltaic (PV) cells, wind turbine, flywheel, diesel generator, batteries and microturbine. Some of these generations are RESs type i.e. PV cells and wind turbine, which are intermittent in nature and follows different generation characteristics [4], [5]. These RESs are connected to the MG through power electronics interfacing (PEI) inverters and converters, which are used to convert the generated power into different format i.e. DC-to-AC and AC-DC-AC. Different types of loads (L), Isolators and circuit breaker (CB) are also connected to the MG. The isolator is used to connect or disconnect a portion of the MG (to accommodate any change in its configuration). Whereas, the CB is a controlled switch that is used to perform the control and protection activities. The main circuit breaker (MCB) located at PCC is a centralized switch that is responsible for deciding the operating modes of the MG. Now, there are several challenges for reliable operation of the MG system viz. monitoring, controls, and protection. Among these, protection of the MG is of high significance. The work presented in this thesis covers various aspects of MG protection.

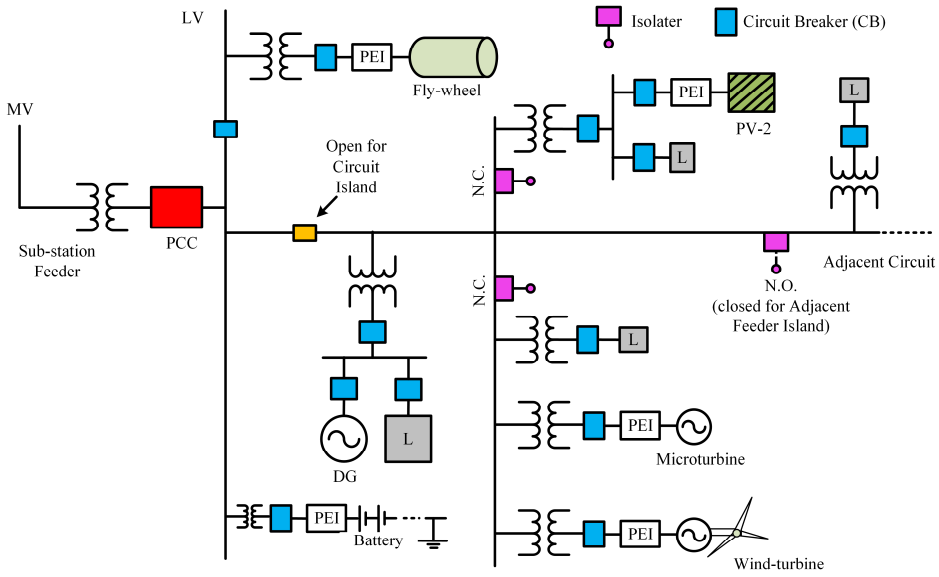

Figure 1.1 Architecture of the Microgrid

1.2.1 Microgrid Protection

Traditional protection schemes used in the conventional power system, are not applicable for the protection of the MG due to the integration of a large number of DERs [6] [7]. The involvement of low inertial interfacing converters, bidirectional power flow within the network and different generation characteristics make the task of MG protection a complex one. Furthermore, the magnitude of the fault current is limited and it depends on the operating mode of the MG as well as number and types of the integrated DGs placed within the MG. The contribution of the fault current by rotating machine based sources are higher than that of inverter-interfaced DERs as compared to their respective normal rated current. The magnitude of fault current is 6.0-10.0 p.u in the rotating machine whereas its magnitude is lower i.e. up to 1.0-2.0 p.u in case of inverter-interfaced DERs [8]–[11] [12]. Moreover, in the grid-connected mode of operation, the magnitude of fault current is greater than the magnitude of fault current in the islanded mode of operation. Therefore, it is important to detect the operating mode of the MG. Identification of the mode of operation of the MG is also essential for the programming of protection devices since the contribution of the fault current depends on the mode of operation of the microgrid and penetration of the DGs, RESs and storage devices that affect the satisfactory working of the traditional protective relays. Quick isolation of the DGs in case of islanding event is considered to be a significant step towards MG protection. However, it is difficult to achieve this goal by using a traditional relay. Several other protection issues of MG viz. identification of its operating mode, islanding detection, isolation of spurious or faulty sections, fault current level, the direction of power flow and blocking of false trips etc. in the presence of a large number of DGs is a challenging task [13], [14]. Out of all these, islanding detection is one of the most crucial aspects for MG protection for safe, secure and uninterrupted power supply.

1.2.2 Importance of IDTs

Islanding is the condition which occurs when a portion of the distribution network (or MG) is disconnected from the utility grid and operates independently with help of local DGs and RESs [15], [16]. Generally, two types of islanding of MG occur i.e. intentional and unintentional [17]. The intentional islanding is mainly performed to carry out some maintenance works within the MG and for the safety of the working personnel [18]; whereas the unintentional islanding occurs due to the utility grid blackout by equipment failure, natural disaster or any abnormality in the power system. System stability and power quality within the MG are adversely affected during the unintentional islanding, which can damage the electrical equipment (critical loads and DGs)

within the working islanded section. Hence, in present studies, more focus is given on the unintentional islanding of the MG [12].

Therefore, when islanding occurs at PCC, it must be detected at the DG terminals which can be disconnected from the MG feeders for the safety of the equipment. As per the suggested standard viz. UL 1741 [19], IEC-62116 [20] and IEEE 1547^{TM} [21] islanding must be detected and the active DGs are isolated from the MG within 2-seconds after detecting the islanding. However, by isolating a DG, the reliability of the MG i.e. maintaining the uninterrupted power supply to critical loads is lost. Therefore, to improve the reliability of MG, another way to act in case of MG islanding is to reduce the output power of the DGs (equivalent to the critical load demand) instead of isolating it. In that case, for the protection of working DGs, the relay settings should be changed i.e. reduced as per the decrease in the power flowing through the network. Now, for the purpose of islanding detection, under/over voltage, under/over frequency, and phasor based techniques are mostly used [22]. Hence, it is an essential requirement to develop a fast relay that can detect the islanding (by sensing variations in these parameters) within the stipulated time interval as well as take necessary action i.e. either isolate the affected section/DG of the MG (with non-critical loads) by generating the trip signal or adapting the relays at the DG terminal i.e. reducing their threshold setting for maintaining reliability of the supply to critical loads.

1.2.3 Requirement of Fast Relays

The existing overcurrent protection relay i.e. OCRs developed for passive distribution networks (radial network) are not applicable for active distribution networks viz. MG. Since MG is a low-inertial system as the integrated DERs are connected through PEI having fast dynamics. Some of the other significant protection issues for using conventional relays with respect to MGs are listed below [6] [23]:

- The level of fault current varies according to their mode of operation i.e. the protection technique developed for one mode of operation would not be applicable for another mode of operation due to the different level of fault current.
- Threshold setting of the relay become invalid because of the unpredictable dynamic characteristics of RESs based generators.
- DERs are connected to the MG using different types of interfacing PEI which limits the amount of fault current.

To overcome the stated problems, a fast relay is required for the protection of a MG that can isolate the faulty section, detect its mode of operation and also, change the setting of the

threshold as per the operating mode. Further, it is important to note that, the MG is a low-inertial system having different types of DG with faster dynamics. To tackle these issues, protective hardware is required to be developed that can sense the faster dynamics within a MG and also have the feature of parallel processing by which the computation time for decision making is reduced. Hence, a faster response is obtained. The Field programmable gate arrays (FPGA) is such an electronic device that is used in the power system industry and smart grid applications asking for high computational demand, low latencies, reconfigurability, high bandwidth and parallel processing [24].

With the help of FPGA, signal processing modules are implemented with a higher degree of accuracy at a low cost. Furthermore, they are easily reprogrammable to accommodate any changes in the design [25]. The performance of the FPGA based system is a lot better than the microcontroller i.e. μC and DSP based relays. Since FPGA works on the principle of parallel processing, its operations are faster [26]. Due to these predominant features, the FPGA based systems are currently being considered to perform power flow monitoring, fault identification and the protection of the distribution systems [27].

1.3 Field Programmable Gate Array

FPGAs are programmable integrated devices capable of implementing the digital design of the protective relays for MGs. Reconfigurability and re-programmability are the important features of the FPGA that provides the flexibility for developing logic circuits at low cost. Low power consumption, high-speed input-output (I/O) capabilities and parallel processing are some of the essential features of FPGA, which are used in the signal processing and found suitable for the practical platform with real-time applications [28], [29] [30]. Hardware description language (HDL) viz. VHDL or Verilog is used to implement the digital-logic on the FPGA. In VHDL, 'V' stands for **V**ery **H**igh-**S**peed **I**ntegrated **C**ircuit (VHSIC) and HDL. Figure 1.2 shows a typical architecture of the FPGA that consists of input-output blocks (IOBs), programmable switches (Ss) and configurable logic blocks (CLBs) [31]. IOBs are the special logic blocks that provide a programmable interface between the CLBs and the external peripherals. Switches provide programmable interconnections between input/output and CLBs. CLBs are the programmable logic blocks also known as slices or logic cells that are used in the digital design of an algorithm or a circuit for performing necessary computation and storage of data. Programmable combinational logic (various gates), flip-flops and look-up tables are the main elements of CLBs.

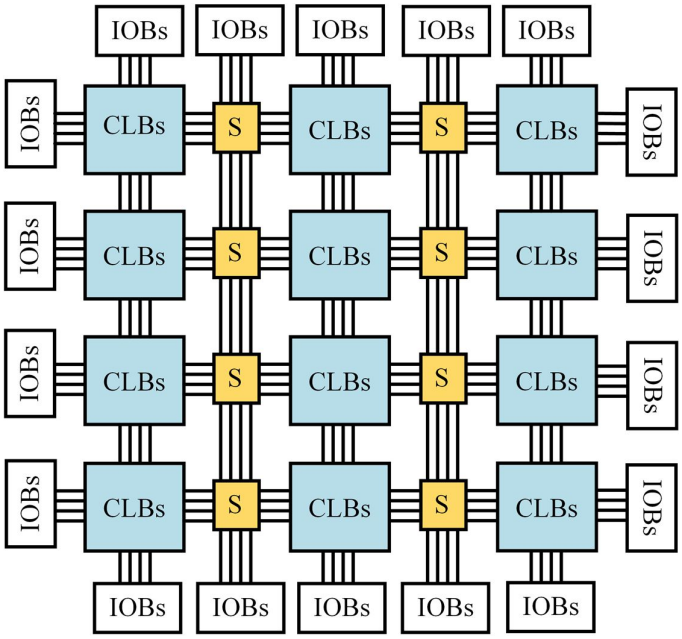

Figure 1.2 Overview of the Field Programmable Gate Array

1.3.1 FPGA Design Flow

Figure 1.3 shows the simplified design flow to program an FPGA. It includes HDL coding, simulation, synthesis, and implementation as discussed below:

Design Entry:

At this stage, functionality and structure of the design plus I/Os of an algorithm are defined. There are different methods of the design entry viz. schematic based, HDL based and a combination of both. Schematic based design entry is easy to read, but, it is not convenient for large project (complex design). HDL based designs are more convenient and fast to implement the sophisticated design. In our work, HDL based design approach is used to implement the relaying algorithm using Verilog HDL. Target FPGA device is also selected during the design entry for the simulation and implemented of the design.

RTL Design and Simulation:

It is also known as register transfer logic (RTL) design and simulation. This simulation is performed to detect any logic error in the functionality implementation of the design. The simulation run time is not very high and it also allows one to change the HDL code if the required functionality is not met.

Synthesis:

In this process, input HDL viz. VHDL or Verilog is translated into a netlist, which describes a list of logical element (logic gates and flip-flops) and their connectivity. For a complex design,

multiple netlists are generated. It has three standard processes i.e. syntax check, optimization and mapping. The resulting output design netlist is in the format of Native Generic Circuit (NGC) file that is used for design implementation.

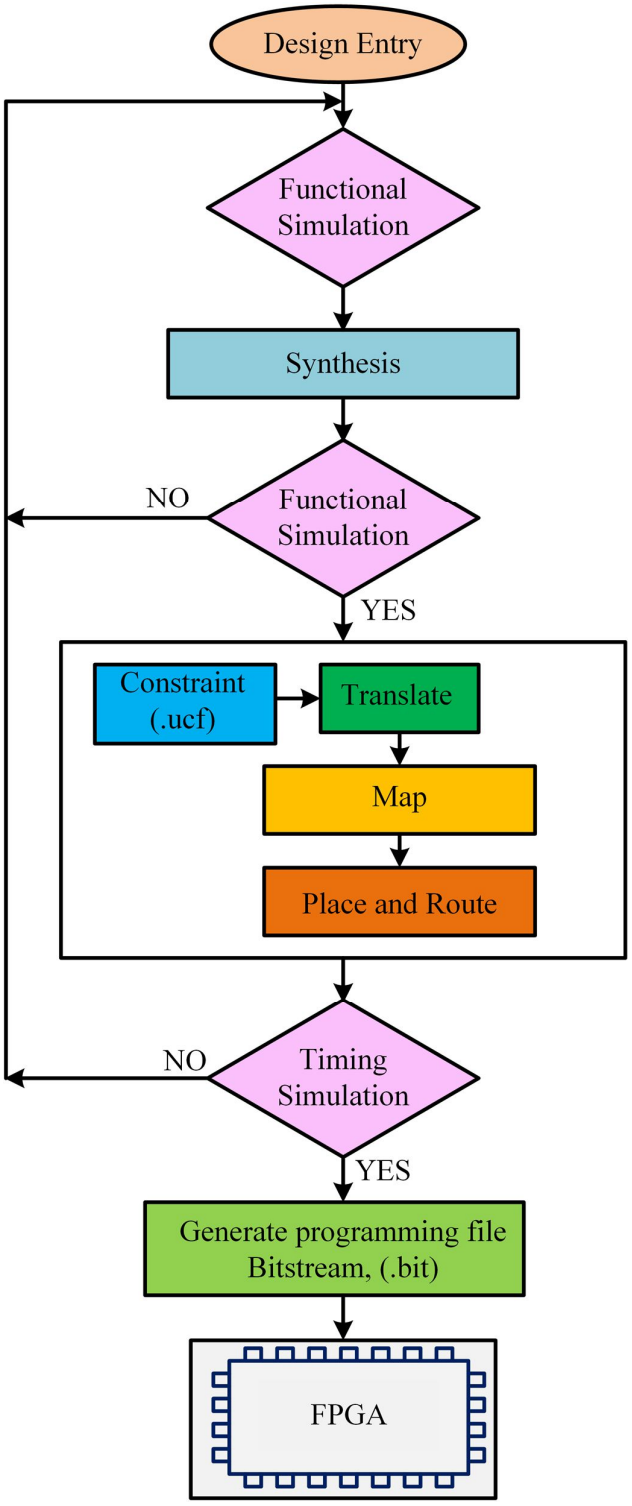

Figure 1.3 FPGA design flow

***Functional Simulation**:*

It is a post-synthesis simulation that gives information about the logic operation of the circuit. The functionality of the design can be tested after completion of the translation process. If the functionality of the design is not met, changes in the code can be done.

Implementation:

This process includes translate, mapping, placement and routing of the logic within the FPGA device. In the translation process, all netlists and constraints are combined into single large netlist (Xilinx format is Native Generic Database (NGD)). Here, constraints are defined through pin assignment and timing requirement viz. input clock period and maximum delay. This information is stored in a User Constraints File (UCF) with extention.ucf.

After that, the specified resources of the input netlist (extention.ngd) are compared with the available resources of the target FPGA during the mapping step. Here, an error message is generated if the resources are specified/defined incorrectly. The whole circuit is divided into sub-blocks to fit into the logic blocks of the target FPGA. Native Circuit Description (NCD) file is generated as an output.

Now, the place and route processes are used to mapped NCD sub-blocks into FPGA logic blocks physically, according to the defined constraints. Also, signals are routed between logic blocks to meet the timing constraints. The output NCD file carries routing information.

Timing Analysis:

Finally, a timing simulation is performed after the place and route step, which evaluates the implemented design with all the timing constraints. The complete information of the time delay of the design is written out in the Post Place and Route timing report.

The routed NCD file is converted to a bitstream (.bit file) using BITGEN that is used to programme the target FPGA for on-chip implementation.

1.4 Literature Review

As this thesis primarily focuses on the fast acting relays and MG protection, the literature review is divided into three parts: relay design, islanding detection and mode adaptability for the MG protection. A comprehensive review of these areas is carried out as follows:

1.4.1 Relay Design

A relay is designed to ensure the protection of an electric power supply network against faults and abnormalities in power system operation. Overcurrent relays (OCRs) are more commonly used relays for power system protection than any other type of relays [32]. These relays operate when the actuating current exceeds from a specified limit, by generating a trip

signal for the CB. These relays have been deployed to protect a wide range of power system components such as generators, sub-transmission and distribution networks, rotating machines and transformers etc. Figure 1.4 and Figure 1.5 represent the inverse characteristics i.e., Very inverse (VI) and Extremely inverse (EI) characteristics of the OCR. In these figures, y-axis represents the relay tripping time in sec whereas x-axis represents the fault current (I_{sc}) in Amp. Each curve shows the fixed values of the I_p settings. For a given I_p, if the magnitude of fault current I_{sc} increases, the trip-time decreases. However, if plug-setting I_p is kept high (for a given fault current), then the relay tripping time would also increases.

An electromagnetic relay is a fundamental relay which works on the principle of electromagnetic effects of the current flowing through the energized winding. This relay has many limitations such as high power consumption, contact problem, slow response, a high burden on instrument transformer and adaptability. A technological transition in relaying is observed after cheap and large-scale manufacturing of the diodes, transistors, capacitors and inductors were made possible in the late 1980s. This added a new edge in the power system industry by introducing the solid state and static relays. These relays have comparatively low-

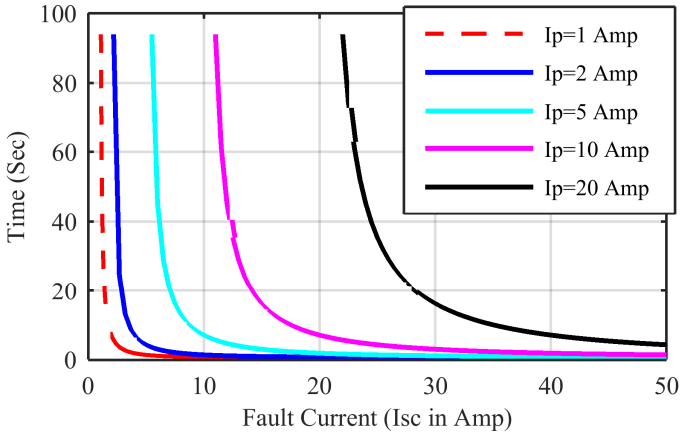

Figure 1.4 Characteristics plot (time vs I_{sc}) for VI

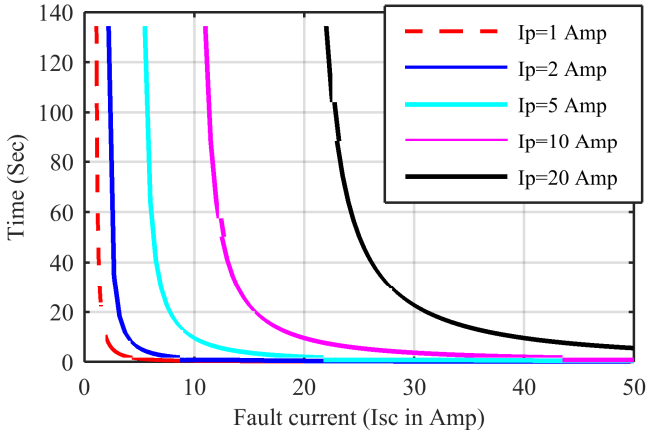

Figure 1.5 Characteristics plot (time vs I_{sc}) for EI

cost, small size and require less maintenance. However, programmability and lack of communication features were the major drawbacks of such conventional relays.

Microprocessor and Microcontroller based digital numerical relays were introduced in the 1990s [33]–[38]. These relays facilitate software programmability and support multiple objective realizations on a single chip. However, the requirement of application specific integrated circuits (ASIC), programmability, memory space, computational burden, limited speed and high cost were the main constraints of these relays. A hybrid passive OCR equipped with an inductor and a capacitor is proposed in [39]. Here, overcurrent function is used for the detection of DC fault, while the frequency of the LC circuit is processed by the discrete wavelet transform (DWT) to detect high resistive faults. However, this relay is meant for small-scale DC grids only. In [40], a new time-current characteristic for numerical OCRs is proposed by using a customized approach having a set of successive straight lines considered as the OCR characteristics. Relay tripping time is computed using the look-up table which contains the relay operating time and magnitude of the fault current. By doing so, it was assumed that each relay should be operated at the lowest possible time. However, the operating time of the OCR is increased when the magnitude of the fault current does not fall into the look-up table. Therefore, the linear characteristic maintains a fixed time interval between the primary and backup protection relays, hence, affects their coordination. Therefore, some researchers are still trying to define better time-current characteristics than the standard ones to be used in the numerical OCRs [41], [42].

Later, OCR is developed on the FPGA hardware, which is a mature technology and used for high-speed applications. It has credentials for developing intelligent electronic devices (IEDs) which are used in power system industry and smart grid applications asking high computational demand, low latencies, reconfigurability, high bandwidth and parallel processing [24]. FPGA based OCR design is reported in [43] which uses a three-stage pipelined architecture which consists of a look-up-table, a counter, and two comparators. Although the design involves the advantages of FPGA, the effects of noise, signal conditioning and inverse characteristics of the OCR are not considered in the design. The FPGA-based wavelet transformation module is proposed in [44]. Here, the dedicated task of detecting various disturbances in power system such as voltage sags, swells, and loss of power has been carried out. This hardware design requires the allocation of huge amount of hardware resources. Another FPGA based inverse definite minimum time (IDMT) OCR is reported in [45]. The design is based upon a look-up table and the trip signal is generated after a certain delay (predefined in the look-up table) when the value of current is greater than the magnitude of stored value. Here, a preloaded lookup

table is used for determination of tripping time with respect to operating current and cannot be used under varying operating current conditions. Also, it does not follow the IEEE Standard inverse characteristics curve. In [46], a system on a programmable chip (SOPC) based OCR design is presented. Altera development board and soft processor intellectual property (IP) core are used in the design. However, this design does not report extraction of the fundamental frequency component and the proposed OCR is not tested in a closeded loop environment such as Hardware-in-Loop (HIL). Another FPGA based digital OCR is presented in [47] [48]. Here, the pipeline architecture has been used for the design, which was implemented on the Xilinx Virtex-II development board. In this design different types of fault is considered for the verification of the inverse characteristics prescribed by IEEE. However, the HIL verification has not been done for the proposed design. Here also, it lacks the verification in the form of FPGA implementation under real-time operating conditions.

In [49], a multi-functional protective relay is presented which is completely based on pre-existing IP cores. The design is based on floating point arithmetic operations which increase both the hardware utilization and the computational burden. Instead of real-time, stored data for fault conditions has been used for testing and HIL verification in closed-loop condition has not been performed. These also fail to cater the requirement of restraint behaviour under inrush current effect which arises due to energization of transformers. Also, in this article, a directional-OCR (DOCR) has also been proposed. Design of the DOCR is based on the delay timer where the trip signal is initiated after a certain time delay. In this design, the inverse characteristics of the OCR have not been included. Directional protection algorithm based on the current sensing module is proposed in [50]. Here, two separate modules have been used for the detection of the magnitude of the fault and its direction. Current is considered as the polarizing quantity in this module and the direction detection module computes the phase angle difference with respect to the normal current. In this paper, inverse characteristics of the OCR is not considered and HIL verification has also not been performed. In [51], a current signal based DOCR is discussed for the transmission line protection. The pre-fault current signal is used as the polarizing quantity. The direction of the fault is detected by a superimposed component of the current signal. The design does not consider the inverse characteristics of the OCR. Also, it is not verified in a real-time environment (HIL).

Certain application of directional relay for coordinated operation is also available in the literature [52]. In [53], a directional inverse time OCR is suggested for meshed distribution systems. Here, continuous relay settings are suggested for the coordination strategy in addition to the conventional pick-up current *Ip* and time-dial settings (*TDS*). By doing so, the operating

time of the OCR is reduced. But, it fails to provide details for computing its directional element. Also, the design and testing of the directional relay in a closed-loop environment have not been discussed. In [54], a new directional element based OCR is proposed. The directional element of the asymmetrical fault is computed using the magnitude and angle of the superimposed negative sequence impedance, whereas for a symmetrical fault the same is computed using the magnitude of the superimposed positive-sequence impedance, positive sequence current and torque angle. Here, the hardware complexity is higher since computation of the sequence component of the impedance is required. Further, the speed of operation of the directional element depends upon the size of the phasor measurement window. Also, the experimental validation of the designed relay was not reported, and only simulation studies are presented. In [55], the direction of the fault is estimated by a current-based algorithm using the sign of the imaginary part of the post-fault current phasor. However, the experiments are performed in off-line mode by considering a data logger.

1.4.2 Islanding Detection Technique for MGs

Islanding detection techniques (IDTs) are broadly classified as local, remote and intelligent IDTs as shown in Figure 1.6 [56]–[60]. Local IDTs are further categorized as active, passive, and hybrid methods. In passive IDTs, local parameters of the target DGs terminal viz. frequency, voltage, current, and phase angle are monitored to detect the islanding [61], [62]. Whereas, in active IDTs, small perturbations are introduced with the local parameter. This results in a significant change in the measured system parameters that are used to detect the islanding. In hybrid IDT, two or more methods of islanding detection from active and passive IDTs are combined. In remote IDT, variations in the electrical parameters due to system disturbance is measured at different locations within the MG and the information is transferred to the central control unit through a communication link. The decision for islanding is taken based upon an assessment of various conditions observed from the information shared. Other important category is the intelligent technique that use advanced signal processing tool viz. wavelet transform, neuro-fuzzy classifier, S-transform, artificial neural networks (ANNs), adaptive ANNs for effectively detecting and classifying islanding conditions [56], [57]. The advantages and limitations of the discussed techniques are tabulated in Table 1.1 [63].

1.4.2.1 Active islanding detection techniques

Active IDTs are based on estimating the response of various local parameters at the DGs terminal which are mostly generated by introducing/injecting small perturbations using an external source. In active islanding detection technique, a small noise signal is intentionally

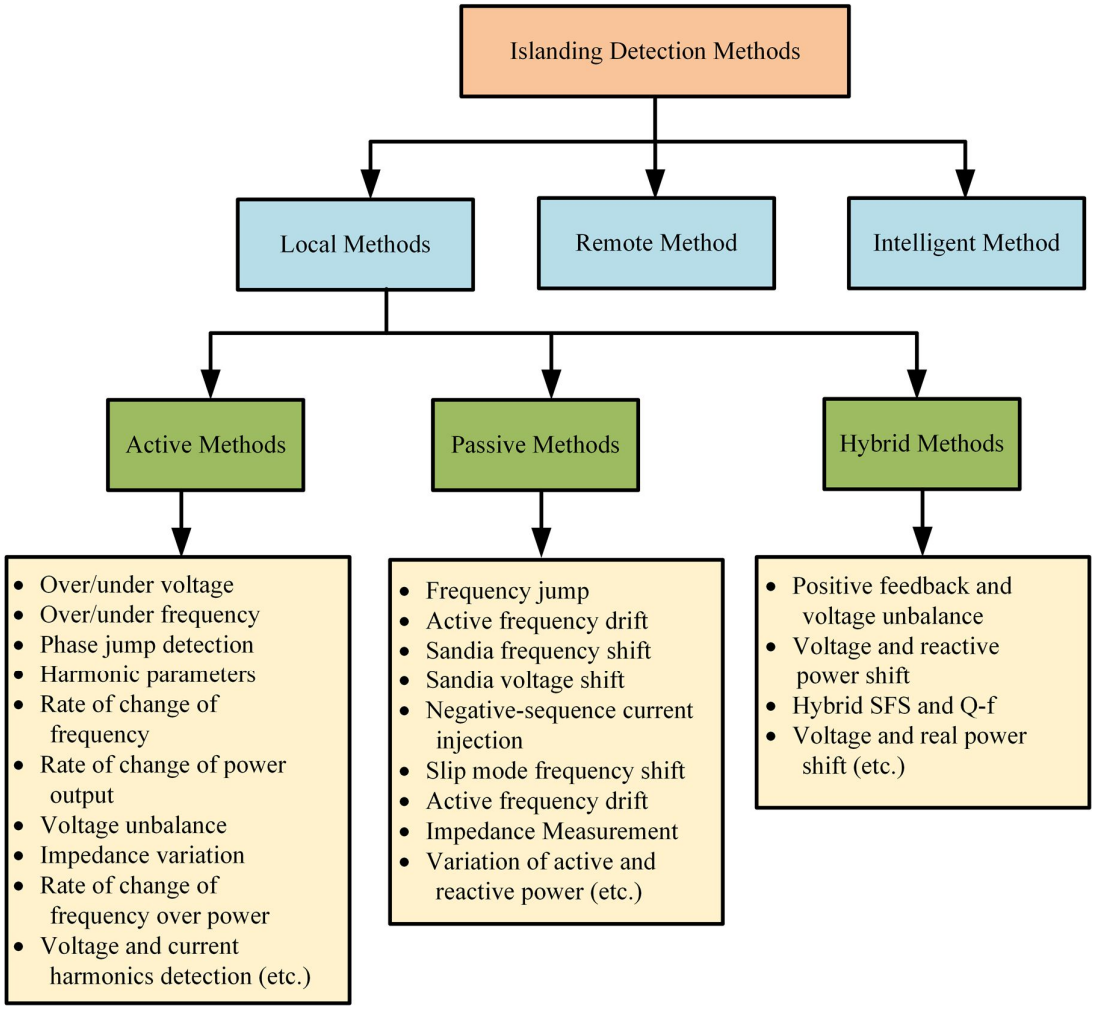

Figure 1.6 Classification of islanding detection techniques

introduced into the system and decision is taken based on the response of the introduced noise signal [64], [65]. Under normal condition this noise signal will not cause large deviation in the system parameters, however, during islanding, this signal gets amplified and thus facilitates islanding detection [66]. Various active IDTs are suggested in the literature, some of those are discussed in following subsection.

In the active frequency drift (AFD) method, a slightly distorted current is injected into the PCC by the inverter. This method is effective only when loads are purely resistive [16], [67]–[69]. Here, the frequency of the output current is varied by using positive feedback. The main advantage of this method is that it is easy to implement and has a small NDZ. Furthermore, NDZ is zero for purely resistive loads [60]. However, it may fail to detect islanding in case of multiple inverters and the power quality of inverters output is degraded more quickly.

In slip mode frequency shift (SMS) method, positive feedback is introduced to the phase angle of the inverter current that causes deviation in frequency at PCC that is used for islanding detection [70]–[72]. When the MG operates in grid-connected mode, the phase angle between

Table 1.1 Comparison of various islanding detection method

Features	Passive	Active	Hybrid	Remote	Intelligent
Operating principal	Monitoring PCC parameters	Injected disturbance	Both active and passive methods	Communication between DG	Features extraction
Non detection zone	Large	Small	Very small	Zero	Negligible
Response time	Short	Very short	Longer than active methods	High	Short
Applicability in MG with DGs	Highly preferable	Not preferable	Not preferable	Preferable	Preferable
Nuisance tripping (%)	High	High	Lower than active and passive	Negligible	Low
Implementation cost	Average cost	Minimum	High cost	Extremely high cost	Average cost
Effect on MG	None	Power quality highly degraded	Degrades power quality	None	None

the inverter current and the PCC voltage is zero or very close to it. However, when it is disconnected from the main grid, the phase angle of load and frequency will vary along with the predefined SMS curve. Islanding is detected when frequency variation crosses the threshold value. The main advantages of this method are easy to implement and smaller NDZ than other active methods.

Sandia frequency shift (SFS) is an advanced version of AFD that includes positive feedback to the frequency at PLL [73], [74]. In the grid-connected mode of operation, a small change in frequency occurs and it does not amplify by the feedback due to the stability of the main grid. However, when the grid is disconnected, frequency of the PCC changes that produce a phase error. The process continues until a threshold limit is crossed and the island is detected. This method has the smallest NDZ, but, it reduces the power quality.

Other feedback-based method is Sandia voltage shift (SVF) in which positive feedback is applied to the amplitude of the PCC voltage [75], [76]. Outputs of the inverter i.e. power and current are varied by the positive feedback. The amplitude of voltage is not affected much in the grid-connected mode of operation but in islanded operation, voltage drift is increased, that is used to detect islanding. This is the most effective detection method over other feedback methods and also with faster detection speed and a smaller NDZ.

In impedance measurement based method, inverter output impedance is considered to detect the islanding. Here, a variation in inverter output impedance is observed due to the loss of utility grid [77]–[79]. In this method, a shunt inductor is connected across the supply voltage from time to time, which is used to compute the source impedance using short circuit current and reduction in supply voltage. It is also very difficult to set the threshold value of the impedance. This method has extremely small NDZ for single DG system. However, detection efficiency decreases in multiple inverter cases unless all the inverter is synchronized.

In negative sequence current injection method, negative sequence current is injected through the three-phase voltage source converter [80]. After that negative sequence voltage is monitored at the PCC to detect islanding. In grid-connected mode, the PCC voltage is not affected by the injected negative-sequence current, because the main grid has low impedance and injected current entirely flow into the grid. However, in islanded MG, injected current flow into the local load due to which voltage unbalances occur at PCC, which is used for islanding detection when the magnitude of voltage unbalance exceeds the threshold value. This method is faster than other active IDTs and also have zero NDZ. A comparison between various active IDTs is tabulated in Table 1.2.

1.4.2.2 Passive islanding detection techniques

Passive detection techniques are also known as universal detection technique because these are applicable for both inverter and synchronous machines DGs. Various traditional passive IDTs exist in the literature, those are discussed as follows:

Some of the important IDTs in literature are voltage and frequency based methods [56], [59], [81]–[85]. In these methods, the allowable range i.e. threshold value of voltage or frequency is predefined. The deviation of the voltage and frequency is mainly due to the power mismatch between DGs output and loads of the MG. The decision for islanding is taken if the

Table 1.2 Comparison of various active islanding method

Methods	Detection Time	NDZ	Advantage	Drawback
IM	0.77s-0.95s	Small for single inverter system	✓ NDZ reduces ✓ Error detection ratio decreases ✓ Increases harmonic distortion	✓ Deteriorate power quality ✓ More effective in multiple inverter system
SMS	~0.4s	Smaller than AFD		
AFD	Within 2s	NDZ increases with 'Q'		
SFS	-	Smallest		
SVS	-	Smallest		
Negative sequence current injection	60ms	Zero		

measured deviation of the voltage or frequency at the PCC is greater than the predefined threshold. The major advantage of these methods is low cost and no impact on power quality. However, large non-detection zone (NDZ) and long detection time are the main shortcomings.

In phase jump detection (PJD) method, a sudden jump in the phase difference between the inverter's terminal voltage and current is used to detect islanding [70], [86]–[89]. In this method, the phase-locked loop (PLL) is used to detect the zero-crossing of the PCC voltage that is synchronized with the inverter current. Sudden 'jump' in voltage in islanded operation is captured due to the phase angle of the load which is used for islanding detection. Although, this method is easy to implement, have fast detection speed and does not affect the power quality. However, difficulty in setting the threshold value is the major concern of this method. Also, this method fails to detect islanding when the generation of power closely matches with the power demand of the local loads.

In harmonic detection (HD) based techniques, total harmonic distortion (THD) of the voltage signal at PCC is monitored to detect the islanding. When the magnitude of THD exceeds its pre-defined threshold value, it is detected as islanding [56], [84], [90], [91][92]. During grid-connected operation, the magnitude of PCC voltage is equal to the grid voltage due to which the magnitude of harmonics is negligible. However, during islanded operation, the current harmonics produced by the inverter are transmitted to the loads that cause HD at PCC. The major advantage of this method is its effectiveness in case of multiple DGs that are connected to the PCC in parallel, and also it is easy to implement. But, it is difficult to select the threshold value for reliable islanding detection. Also, this method fails when the magnitude of the quality factor (Q) is large.

In case of the grid-connected mode of operation of MG under power mismatch condition and it is disconnected and from the main grid, then it causes a power imbalance situation in the MG. This, in turn causes transients in the islanded MG and thus leading to the change in frequency. Therefore, the rate of change of frequency (ROCOF) is computed over a few cycles usually 2-50 cycles for islanding detection [82], [93], [94]. The continuous monitoring of ROCOF and comparing it with the standard threshold value creates a suitable condition of islanding detection. The major drawback of ROCOF based method is is sensitivity to load switching and fluctuation that causes an error in detection.

Rate of change of power output (ROCOP) is an important IDT that is applicable where power imbalances are more. In this method, changes in the output power of the DG is monitored, since, effective load changes due to loss of mains. NDZ is the major shortcoming of this method that

arises in power balance condition, and also the detection time is more. However, this method is more effective in case of the increased amount of power mismatch [59], [93], [95].

Bus voltage variations have been a significant parameter to indicate any discrepancies viz. network faults, topological change and tripping of large generator or load. Hence, taking account of the voltage unbalance (VU) that is computed using negative and positive sequence of voltage at the PCC, can enhance the effectiveness of islanding detection [91], [96]. Although this method is not sensitive to the system disturbance, the negative sequence component of voltage is highly affected by harmonics.

From the above discussion, it is clear that passive IDTs are cost-effective and simple in implementation. However, the major shortcomings of these methods are the large NDZ, and also fails to detect the islanding condition under power balance condition. A comparison between various passive IDTs is tabulated in Table 1.3.

Table 1.3 Comparison of various passive islanding method

Methods	Detection Time	NDZ	Advantage	Drawback
OUV/OUF	4ms-2s	Large	✓ No impact on power quality ✓ Detection speed is fast	✓ Large NDZ ✓ Error detection rate is high
PJD	53ms	Large		
HD	45ms	Large with a large value Q		
ROCOF	24ms	Small		
ROCOP	24ms-26ms	Smaller than OUV/OUV		
VU	53ms	Smaller		

1.4.2.3 Hybrid islanding detection techniques

In the hybrid detection technique, a combination of both active and passive methods are used to detect the islanding and also takes advantage of both the methods. These IDTs have lower NDZ and do not affect the power quality significantly. Some of the important hybrid IDTs are discussed as follows:

In [97], a hybrid IDT based on Positive feedback and voltage unbalance (VU) is used to detect islanding. Here, both active and passive methods i.e. positive feedback and VU respectively are used where the drawback of both the methods are eliminated. A spike in VU is developed when any disturbance is applied to DGs and island is detected if the magnitude of the spike is above the threshold value. The advantage with this methods is that, the load switching is discriminated from islanding condition.

In [98], real power shift (active) and the average rate of voltage change (passive) are simultaneously used to detect islanding. Here, the real power shift (RPS) is used only when the passive method is not able to detect islanding, which rejects the requirement to injecting the disturbances frequently. This method can also be used to detect islanding with multiple DGs system that operates at unity power factor.

Voltage and reactive power shift based hybrid IDT is suggested in [70]. In his method, covariance value is calculated by varying the voltage over time, thereafter, the adaptive reactive power shift algorithm is used for islanding detection. In the case of suspicious islanding, the additional reactive power shift speeds up the phase shift that causes fast frequency shift. In [99], a hybrid IDT based on the combination of the slip mode frequency shift (an active IDT) and ROCOF and over/under frequency relay (a passive IDT) has been proposed. Another hybrid IDT based on the probability of islanding (PoI), which uses a combination of active, passive along with the communication-based technique (a remote IDT) is suggested in [100]. These

Table 1.4 Comparison of various hybrid islanding method

Methods	Detection Time	NDZ	Advantage	Drawback
ROCOV and power variation	~	Small	✓ Applicable for complex systems ✓ Takes the advantages of both the combined methods ✓ Comparative small detection time	✓ Slightly degrade power quality ✓ Effective in multiple- inverter vases
VU and SFS,SVS	~	Very small		
ROCOF and IM	0.216s	Small		
Wavelet & S-transform based)	Very small (less than 1 cycle)	None		
Combination of voltage amplitude and frequency at the PCC	33.3ms	Very small		
Combination of voltage amplitude and frequency	150ms	Very small		
Combination of ROCOV and real power shift	<2s	Small		
Combination of VU and THD	<2s	None		

hybrid IDTs are accurate, reliable and have low NDZ, however, these methods are usually more complex in design and implementation, with high computational costs. A comparison between various hybrid IDTs is tabulated in Table 1.4.

1.4.2.4 Communication-based islanding detection techniques

In remote IDT, variations in the electrical parameters due to system disturbance is measured at different locations within the MG and the information is transferred to the central control unit through a communication link. The decision for islanding is taken based upon an assessment of various conditions observed from the information shared. Remote IDTs such as power line carrier (PLC) signalling scheme [60], [101], [102], transfer trip relaying scheme [103], phasor measurement units [104], and supervisory control and data acquisition (SCADA) [90], are mostly used. In the power line communication (PLC), the power line is used as a communication medium by which a signal is continuously sent from the grid to the DG. The island is detected by checking the status of the receiving signal. The concept of master and slave is used in SCADA system, which consists of a master and a number of distributed remote terminal units (RTUs) connected to the master through communication channels. Transfer-trip (TT) technique is incorporated using the central SCADA system at the substation. When a disconnection is detected at the substation, TT sends trip signals to DGs of identified areas of islanded MG. Although it is a complicated detection technique but it is reliable and insensitive to noise. These remote IDTs are accurate, reliable, do not affect the power quality by destabilizing the system, less NDZ and provide a good solution to the problems occurring in active and passive detection methods. However, these methods are complex and very expensive (additional cost of communication infrastructure) to implement and has comparatively larger detection time. A comparisons between various communication based IDTs is tabulated in Table 1.5.

Table 1.5 Comparison of various communication based islanding method

Methods	Detection Time	NDZ	Advantage	Drawback
PLCC	200ms	None for normal load	✓ NDZ ✓ No impact on power quality and system transient response.	✓ Expensive ✓ Complicated ✓ Implementation cost high ✓ Usually applied in MG with dense DG
SPD	100ms-300ms	None		
Transfer trip	~	Less		
SCADA	speed depends on the system	none		

1.4.2.5 Advanced IDTs based on signal processing tool

IDTs based on advanced signal processing tool (SPT) viz. wavelet transform [105]–[108], S-transform [109], [110], Hilbert Huyang transform (HHT) [111], pattern recognition [66], principal component analysis [112] and rate of change of sequence component of current [113] are also suggested in the literature. In these methods, SPTs are used to extract the features of the signals to detect islanding. However, these techniques fail to discriminate between the islanding events from non-islanding events and do not take reliable action during the zero power imbalance condition. Later, [114] presents an islanding discrimination factor (IDF) based IDT using the superimposed component of voltage. Although it works satisfactorily for zero power imbalances, however, the IDF based method is too complex, have higher computational burden and detection time. Also, when the ratio of positive to negative sequence components is constant during the normal condition, it may lead to maloperation of the IDT. A comparison between various signal processing based IDTs is tabulated in Table 1.6.

1.4.3 Adaptive Protection Schemes of Microgrid

As mentioned in the above literature, a mode adaptability feature is inevitably required for the reliable operation of MG, subsequent to the islanding operation. In this regard, it is observed that, the magnitude of the fault current in grid-connected mode is higher than the stand-alone mode of operation. Also, the trip time is more in the case of a stand-alone mode in comparison to the grid-connected mode. Hence, mode-adaptability of the OCR module is a must, which can be achieve by changing the I_p setting of the OCR located at the targeted terminal of the MG. Adaptive protection is an online activity that modifies the preferred protective response to a change in system conditions automatically. Adaptive relays are those having their own settings, characteristics or logic functions, changed according to the status of the grid on-line by means of externally generated signals or control action [115].

In the literature, many protection strategies i.e. overcurrent and adaptive relay have been proposed for the grid-connected and stand-alone mode of operation of the MG. In [116], a numerical relay is used for the mode adaptation, meant for overcurrent protection of the MG. The threshold settings of the OCRs were computed manually, and these settings were changed as per the mode of operation. However, relay settings were not updated in real-time by using any communication network. In [117], Microprocessor based relays with a communication feature was suggested for MG protection. In this relay, positive sequence impedances are computed by using phasor measurement unit (PMU), which were considered as parameters for updating the setting of the relay, i.e. pickup current (I_p). The main shortcoming of the design is the time synchronization between the installed PMU and the method was not verified in HIL.

Table 1.6 Comparison of various signal processing based islanding method

Methods	Detection Time	Analyzed Signal	Advantage	Drawback
WT	17ms-26ms	Target DG voltage PCC voltage PCC frequency	Coefficients for all scales and transformations is obtained Better low frequency resolutions	High computational burden and design complexity
WPT	200ms	ROCOP at DG	Equal resolution for low and high frequency	Time-frequency localization decreased with increased decomposition levels
ST	26ms	Negative sequence voltage at PCC	Provides simplified multi resolution	Fails in localization of momentary phenomenon
HST	22ms	PCC voltage or negative sequence voltage at PCC	Better time and frequency resolutions for high and low frequency	Window may not incorporate all signals
TTT	25ms	Negative sequence voltage at PCC or PCC voltage	Better understanding of time-local properties of the time series	Inappropriate low-frequency Localization
MM	$\leq$ 40ms	Negative sequence voltage at PCC	Less computational complexity	Reconstruction of the original signal is not possible
HHT	22ms	PCC voltage	Provides physical representation of data	Less suitable for close frequency components signals

In [118], a multifunctional digital relay with a communication feature was suggested for AC MG. In this method, the GPS technology is used for time-stamping and synchronization with the help of NI9647 module. However, it has reliability issues due to the synchronization of data during any communication failure. In [119], a directional current based adaptive protection scheme is developed in which the steady-state component of the fault current is used for relaying criteria. In this method, the relay settings of the current protection scheme are computed online. However, a time delay is introduced in computing the operating zone and setting the relay adaptability for islanding operation, which makes the protection scheme sluggish.

In [120], a digital relay based on the differential current with communication network for the protection of the MG is suggested. It utilizes the concept of synchronized PMU and microprocessor based relay. Here, time synchronization is not considered in the design, which is the major shortcoming and causes a serious impact as the tripping signal is issued using the measured instant of the differential current. Also, here the implementation cost is quite high. A communication based adaptive protection scheme is suggested in [121], where the setting of the relay is adjusted automatically according to the configuration of the grid. To update the

configuration, a programmable logic controller (PLC) is used as a centralized controller, which monitors the status of the CB. However, to update the multiple configurations, the number of required PLC modules is increased, which in turn increases its design cost. In [122] and [123], a multi-agent based adaptive protection scheme was suggested to adopt the relay settings as per the different operating conditions and the ON/OFF status of the DG. Here, every agent viz. the DG agents, Elements and Relay agent are distributed throughout the network using intelligent electronic devices. These devices are capable of collection and delivery of the information, decision making and communication. However, the proposed scheme inevitably imposes a heavy burden on the communication system. Therefore, many of its tasks are time-consuming. In [124], a numerical OCR relay with inverse characteristic was implemented on FPGA. The inverse features of the relay are emulated by using the concept of ANN. However, this design lacks communication capability and also has a high computational burden.

In [125], multi-agent based adaptive relay was suggested for medium voltage smart grid. In this article, the setting of the relay is adapted automatically if any changes occur due to the network configuration. The adaptivity of the suggested scheme was based on distributed intelligence having a high level of fault tolerance. However, the complexity of the system is very high due to the inter-communication between all the used agents. In [126], the effect of high penetration of DGs on protection device coordination and their adaptability for the distribution system was reported. The proposed adaptive scheme is independent of size, number, and placement of DGs in the distribution system and applicable to temporary as well as permanent changes and placement of DGs. The major advantage of this method is that loss of load in the distribution system is reduced in case of permanent faults. However, the method is not applicable to systems having low DG penetration. In [127], adaptive protection of MG using a digital relay with communication features was suggested. Here, protection settings of the relay are updated centrally through the suggested centralized protection method as per the operating condition of the MG. The settings of the relay are updated not only for the operating mode of the MG but also for different states of the MG i.e. topology, generation and load. Here, the major shortcoming are the protection settings of the relay that is computed using offline fault analysis and updated periodically. In [128], adaptive overcurrent protection using local information is suggested to select the tripping characteristics of the relay based on the operating condition (grid-connected or island) of the MG. The islanding detection method is used to modify the OCR settings. One of the major advantage of using local information is that, if any problem occurs in a relay, it will not affect the other relays present in the network. Here, the studies are limited only to three-phase fault and lack communication facility.

1.5 Motivation

From the literature review, it can be concluded that the use of FPGA in relay design is limited and most of the literature lacks HIL verification. A huge gap still exists to meet the overall efficiency of FPGA based OCR in terms of latency, computational burden, resource utilization and trip time for different inverse characteristics as defined in the IEEE standard. In many reported works, instead of real-time analysis, simulation results and predefined IP (intellectual property) core are considered. Furthermore, stored data from fault conditions have been used for testing. Also, HIL verification in the closed-loop condition has not been performed. These also fail to cater to the requirement of restraint behaviour under inrush current effect which arises due to energization of transformers. Moreover, literature for the inclusion of the directional feature of the OCR is very complex, which increases the burden of the hardware resources. Many designs do not consider the inverse characteristics recommended by IEEE for the design of directional-OCR. A huge gap still exists around HIL verification and real-time signal conditioning and relay coordination among the developed DOCRs.

Now, from the discussion on various IDTs in literature, it is clear that the research for implementing the accurate IDTs with negligible NDZ and less detection time is still in early stages. Low computational complexity and accurate discrimination of the islanding and non-islanding events within the permissible detection time is a major challenge. Along with that, the digital design and HIL verification of these methods are also not yet considered on hardware platform.

Furthermore, most of the works are related to isolating the DGs in case of islanding events. These works do not consider the settings of the internal relays present within the active section of the MG. To maintain the supply for any critical load (hospital, fire station etc.), it is required to keep the DGs connected and maintain appropriate generation. Now, with a reduced capacity of the MG, the magnitude of the fault current in the islanded mode of operation is lower than the grid-connected mode. Therefore, to protect the working DGs, the plug-setting of the OCR must be altered. Also, low computational complexity with higher accuracy that too within the permissible detection time is a major challenge, which also decides the cost of implementation. Mode adaptation of the relays within the MG after the islanding condition and HIL verification has also not been studied. Furthermore, to simultaneously achieve mode adaptability of the OCRs installed at various DG locations, it is essential to add a communication feature within the OCR module along with the features of having different threshold setting upon detection of MGs' operation mode. Now,

instead of using expensive wired communication infrastructure, use of economical wireless communication modules could be explored.

1.6 Objectives and Contributions of the Thesis

Considering aforesaid technical challenges for relay prototype and adaptive protection of MG, the main objectives behind the research work carried out are summarised below:

- To design and implement a FPGA based prototype of the OCR using Verilog-HDL that includes standard IEEE characteristics such as extreme inverse (EI) and very inverse (VI), which can also differentiate the inrush current from the fault current to avoid nuisance tripping.
- To develop the OCR prototype with low latency, adjustable characteristic parameters with directional features, computationally efficient, reduced on-chip resource utilisation and having a faster signal pre-conditioning to satisfy the MG protection requirement.
- To design a new IDT algorithm based on the periodic maxima of superimposed voltage components using an islanding discrimination factor (IDF) to distinguish the islanding and non-islanding events accurately even in perfect power balance condition.
- Developing a multifunctional relay on reconfigurable FPGA chip used for both islanding detection (using a hybrid IDT scheme to take advantage of two passive methods) and mode adaptation of OCR settings to accommodate two operating modes of MG.
- Use of low-cost devices i.e. nrf24L01 (support Enhanced ShockBurst protocol) wireless module to achieve simultaneous mode adaptability of the developed intelligent OCRs installed at different DG locations along with maintaining all the prerequisite criteria of standard OCR and MG islanding conditions.
- Developing a testbed MG system with different RESs on the RTDS® platform to perform the HIL testing of the developed FPGA based relay prototype with all the added features like islanding detection, mode adaptability and wireless communication modules.

1.7 Organization of the Thesis

The thesis is organised in seven chapters and the work included in each chapter is presented in the following sequences:

Chapter 1 gives an overview of the microgrid protection and importance of islanding detection. Also, the requirement of fast relays and usage of FPGA are explained. Thereafter, the literature on existing relay design techniques and the features of mode adaptability for the purpose of microgrid protection are presented. Finally, various objectives and contributions of the thesis are discussed.

In **Chapter-2**, a detailed discussion of the OCR prototype developed on FPGA by using Verilog Hardware Description Language is presented. Internal design development of the OCR and various sub-modules, i.e. analog-to-digital converter, discrete Fourier transform, root mean square module, harmonic distortion module are discussed. The experimental setup for HIL testing of the developed prototype is discussed for both the characteristics and the operational verification of the OCR. HIL verification of the developed prototype has been carried out with real-time digital simulator (RTDS).

Chapter-3 describes the development of a Directional-OCR on the reconfigurable FPGA chip. Here, an efficient design for the computation of the directional logic by using a simple zero-crossing detector method is presented. A fixed point integer arithmetic based design algorithm using Verilog HDL has been used for the implementation and verification of the DOCR. Test system, simulation results, hardware set-up for HIL verification of the developed prototype of DOCR are explained.

Chapter-4 presents a novel islanding detection technique (IDT) based on the islanding discrimination factor using the periodic maxima of superimposed voltage components. The proposed IDT is developed on the FPGA chip. Hardware-in-loop verification of the proposed IDT has been performed for islanding and non-islanding events with a microgrid test system developed on Real Time Digital Simulator.

In **Chapter-5**, the prototype of a hardcore multifunctional relay designed on a reconfigurable FPGA is presented, that used for islanding detection and adaptation of OCR settings as per the operating modes of the MG. The proposed protection scheme is a modular based design. The proposed IDT incorporates the advantages of two IDTs viz. ROCOF and VU. HIL verification of the proposed design is performed with RTDS.

In **Chapter-6**, the DOCR developed in chapter 3 using FPGA platform is further aided with communication features for the adaptive setting of the threshold current that is updated as per the operating mode of the MG. Also, the impact of fault current on MG protection due to its operating modes and DGs are discussed. An MG test system is designed in RTDS to verify the operation of the relay. A complete testbed is developed which includes Enhanced ShockBurst protocol based wireless infrastructure for the HIL testing of the relay.

In **Chapter-7**, conclusion of the carried research work is given. Furthermore, a suggestion for the future scope of the work is also presented.

CHAPTER 2: EMULATION OF AN OVERCURRENT RELAY ON RECONFIGURABLE HARDWARE

2.1 Introduction

A relay is designed to ensure the protection of electric power supply network against faults and abnormalities in power system operation. Overcurrent relays (OCRs) are more commonly used for power system protection than any other types of relays. This relay operates when the actuating current exceeds a specified limit of the current, by generating a trip signal for the circuit breaker. These relays have been deployed to protect a wide range of power system components such as generators, sub-transmission and distribution networks, rotating machines and transformers etc. In this chapter, the design and development of FPGA based prototype of an OCR is presented. The OCR-prototype is implemented on the FPGA and its functionality has been verified using hardware-in-loop testing on the real-time digital simulator. Computational efficiency and memory requirement of the OCR is improved by using integer arithmetic Verilog design platform. Extreme inverse (EI) and very inverse (VI) characteristics of the OCR based on IEEE standard C37.112-1996 is used and tested in the proposed design. The hardware design is developed by using Verilog HDL. The Verilog-based design provides low latency as compared with processor-based systems. The performance of the OCR is evaluated for a broad range of characteristic parameters (pick-up current, time-dial-setting) and various operating conditions which validate the operation of the relay in real-time with the power network. The designed relay is capable of differentiating between fault and inrush current to avoid any maloperation during energization of transformers.

2.2 Working Principle and Design Overview of OCR

The OCR operates when the magnitudes of actuating current exceed from its predefined threshold (I_p) value. Based on time-current characteristics OCRs are divided into three main categories i.e. Definite-time (DT) OCR, instantaneous (I) OCR and inverse time (IT) OCR. I-OCR operates immediately when the magnitude of current exceeds from its pre-set value. Therefore the time delay of the I-OCR is zero. A constant time delay is used in the designing of the DT-OCR. When the magnitude of the current exceeds from its set value, the relay operates by generating the trip signal after passing the time delay setting. In IT-OCRs, time dial setting (TDS) is used instead of a fixed time delay setting for generating the trip signal. In these relays, tripping time varies by varying the magnitude of the fault current inversely i.e. the higher

Table 2.1 Parameters for the relay characteristics

Characteristics	A	B	p	t_r
Very inverse	19.61	0.491	2	21.6
Extremely Inverse	28.2	0.1217	2	29.1

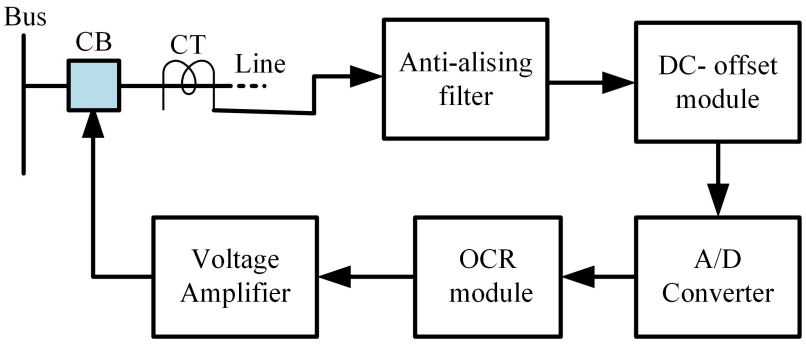

Figure 2.1 Architecture of the proposed protection scheme

the magnitude of fault current, the lower will be the relay tripping time. Different types of standard inverse characteristics i.e. very inverse, moderate inverse and extremely inverse are suggested by the IEEE standard C37.112-1996 [129]. Tripping time of the OCR with inverse time-current characteristics are approximated by (2.1) and (2.2) [129]. The equation (2.1) gives the relay trip time for (M > 1) whereas (2.2) is used for the calculation of relay reset time for (0 < M <1).

$$t = TDS\left(\frac{A}{M^{p}-1}+B\right) \tag{2.1}$$

$$t = TDS\left(\frac{t_r}{M^{2}-1}\right) \tag{2.2}$$

In the above equations, M (plug point setting) represents the multiple of I_p setting which is equal to [I_{rms} / I_p]. A, B, and p are the characteristic (Inverse) constants of the relay. TDS and t_r are the time-dial setting and relay reset time in seconds respectively. The standard relay characteristics constants for VI and EI characteristics are given Table 2.1 [46].

Figure 2.1 shows a brief overview of the protection system. The current measured by the CT at any targeted bus is passed through a set of signal conditioning modules viz. anti-aliasing filter (AAF), dc-offset and analog to digital converter (ADC) module, before it is passed to the OCR module. The internal design (ID) of the OCR module is discussed in the following subsections. The trip signal generated by the relay module is fed to the CB after a fixed amount of amplification (through voltage amplifier block).

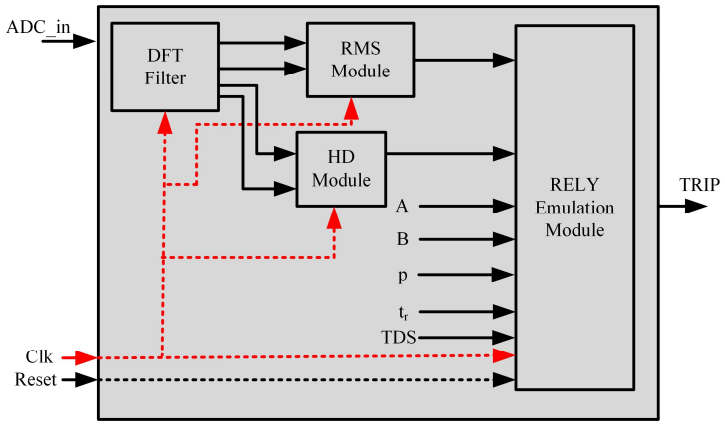

Figure 2.2 Functional block diagram of OCR module

2.3 Internal Design of OCR

Figure 2.2 shows the functional block diagram of the designed OCR. *ADC_in*, *Clk*, *Reset*, *A*, *B*, *p*, T_r and *TDS* are the input signals of the designed OCR whereas *TRIP* is the output signal. The block has four internal sub-module viz. Discrete Fourier Transform (DFT) module, Root-Mean-Square (RMS) module, Harmonic detection (*HD*) module and relay emulation module (REM). These sub-modules are implemented on the FPGA hardware. A detailed discussion on these modules and sub-modules are presented in the subsequent sections.

The ID of OCR is divided into several functional modules and signal flows from one module to another in the following sequence i.e ADC, DFT, RMS and REM. The design and functionality of these modules are discussed as follows:

2.3.1 ADC Module

A 14 bit, two-channel, serial ADC (LTC1407A-1) with programmable pre-amplifier LTC6912-1 is used in the proposed prototype [130]. With the help of a programmable gain amplifier, the range of ADC is varied from 0.4 to 2.9 V. In the design, the gain of the amplifier is fixed at (-) 1. A DC offset of 1.65 V is required and developed for the sampling of 1.25 V (P-P) sinusoidal input signals. 1.5 Mega-samples per second (MSPS) is the maximum sampling frequency of the ADC. The required clock signal of ADC is provided by the designed clock module, which runs at the onboard 100 MHz clock oscillator. Quantization error of the ADC is 153 µV [130], which is insignificant compared to the magnitude of the signal being measured.

2.3.2 DFT Filter and RMS Estimation Module

In this module, the fundamental frequency component (50 Hz) of the input signal is extracted using DFT. RMS of the extracted signal is computed using coordinate rotational digital computer (CORDIC) core [131]. The dc-offset from fundamental frequency component

is removed by subtracting the dc values at each sampling instant [132]. The general expression of the N-point DFT, X(m), m = 0,1,…., N-1 of a sequence x(n) is given by (2.3).

$$X(m) = \sum_{n=0}^{N-1} x(n)\, e^{\frac{-j2\pi mn}{N}} \tag{2.3}$$

X(0), *X(1)* and *X(2)*, are the DC, fundamental and 2nd harmonics components of the input signal x(n) respectively.

A 16 points DFT core is realized in the present work [133]. The sampling frequency of 40 kHz is used in the DFT core to accommodate 16 samples in a single cycle, which reduces the memory requirement and design complexity. The input to this core is provided with real and imaginary data values. The data width of the input and output are in 16 bits 2's complement format. The ADC block outputs 14-bit number, while the DFT module needs a 16-bit input. Therefore the scaling is performed by left shifting and concatenation operations, to manage the data width required by DFT core.

Figure 2.3 shows the timing diagram of the DFT module which gives the data flow from input to output. In this figure, *CLK*, *RESET*, *IN_RE*, and *IN_IM*, are the input signals of the module. *NEXT_IN* is control input and *NEXT_OUT* is the handshaking output of the DFT module which shows from when the output is valid. *O/P_RE* and *O/P_IM* are the data output signals of the DFT module. DFT core starts working after reset signal becomes active high for one clock cycle. *NEXT_IN* triggers the input frame reading by the DFT module. *IN_RE* and *IN_IM* are the 16 bit real and imaginary input data which come from the ADC module and is fed into the DFT module. However, as ADC handles only real numbers (instead of a complex number), the imaginary part of the input is set to zero and by doing so, the compatibility between ADC and DFT modules is maintained. DFT module takes 16 clock cycles to process the data. *O/P_RE* and *O/P_IM* are the real and imaginary output data of 16-bit. *NEXT_OUT* provides the

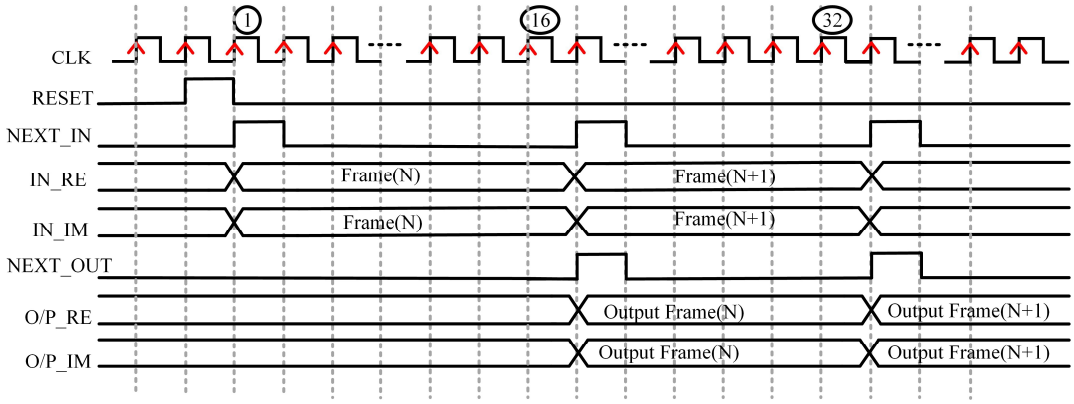

Figure 2.3 Timing diagram of DFT core

handshake to start output data reading which is valid for 16 clock cycles. The output frame of this core consists of coefficients for dc, fundamental and other higher harmonic components of the signal.

The format of the output data of this core is given by equation(2.4). The magnitude of the extracted fundamental component and its RMS is calculated by using equations(2.5), (2.6) and(2.7). Xilinx LogiCORE IP CORDIC v4.0 core is used for the computation of the square root of fundamental component [134] [135].

$$X(1) = x_r + jx_i \tag{2.4}$$

$$|X(1)| = \sqrt{x_{r1}^2 + x_{i1}^2} \tag{2.5}$$

$$|X(2)| = \sqrt{x_{r2}^2 + x_{i2}^2} \tag{2.6}$$

$$X_{rms} = \frac{X(1)}{\sqrt{2}} \tag{2.7}$$

In the above equations, x_r and x_i are the real and imaginary data of the output frames i.e. *O/P_RE* and *O/P_IM*, while *X(1)*, *X(2)* are magnitudes of the fundamental and second harmonic component of the input signal respectively.

2.3.3 Effect of Transformer Inrush Current and Harmonic Distortion Module

A large amount of instantaneous current is drawn by the electrical equipment when it is turned ON. This instantaneous current is known as inrush current or input surge current. The magnitude of this current is several times higher than the rated current. The main source of this inrush effect is the power transformer. The transformer creates a high inrush current during the magnetization of its core. This inrush current includes a high magnitude of decaying dc along with the other harmonic components. The peak value of the dc decaying component may lie within 6 to 20 times of the rated value of the current, during the transformer energization. This causes malfunctioning of the OCR in the presence of the increased values of current and generates a false-trip signal. Therefore, it is necessary to prevent the mal-operation of the relay. To mitigate the effect of inrush current of the OCR, second harmonic distortion (HD) based technique has been used in this work. HD is the percentage change of the 2^{nd} harmonics to the fundamental component of the signal is given by(2.8). During normal and faulty conditions HD is less than 15 %, whereas, in the case of inrush, its value is greater than 15% [136].

$$HD = \frac{X(2)}{X(1)} \times 100\% \tag{2.8}$$

2.3.4 Relay Emulating Module

In this module, one-dimensional numerical integration is performed for emulating the inverse characteristics of the relay represented by (2.9), (2.10) and (2.11) [46].

For $M \leq 1$, $Z_i = Z_r$, and for $M > 1$, $Z_i = Z_s$.

$$\sum_{i=i}^{K} Z_i > N_T \tag{2.9}$$

For M > 1

$$Z_s = \frac{N_T \times \Delta T}{t} \tag{2.10}$$

For 0<M ≤ 1

$$Z_r = \frac{-N_T \times \Delta T}{t} \tag{2.11}$$

In the above equations, 't' is the relay operating time obtained from (2.1) and (2.2) which correspond to the set and reset times as per the value of plug-point-setting (PPS). In the above equation, N_T is the fixed integer (target number) used to emulate the inverse characteristics of the relay [35]. When the sum $\sum Z_i$ exceeds the target number N_T and $HD < HD_{th}$ (threshold value of the HD) the trip signal is generated. The tripping time of the OCR is calculated by (2.12).

$$t_{trip} = K \times \Delta T \tag{2.12}$$

In the above equation, K is the number of operating clock cycle and ΔT is the sampling interval of the REM module.

Figure 2.4 shows the data-path for the logical implementation of REM, which consists of comparators, AND, OR and Inverted-OR (I-OR) gates. An accumulator (Acc), 32- multiplexers (Mux), and an adder block have been used. A 32-bit result block has also been used to emulate the reset characteristics. The signals I_{rms}, rst, clk, Z_r, Z_s and HD are the inputs to the REM. These signals are processed by REM, which takes the necessary decision as per the inputs, and OCR characteristic for the generation of the trip signal.

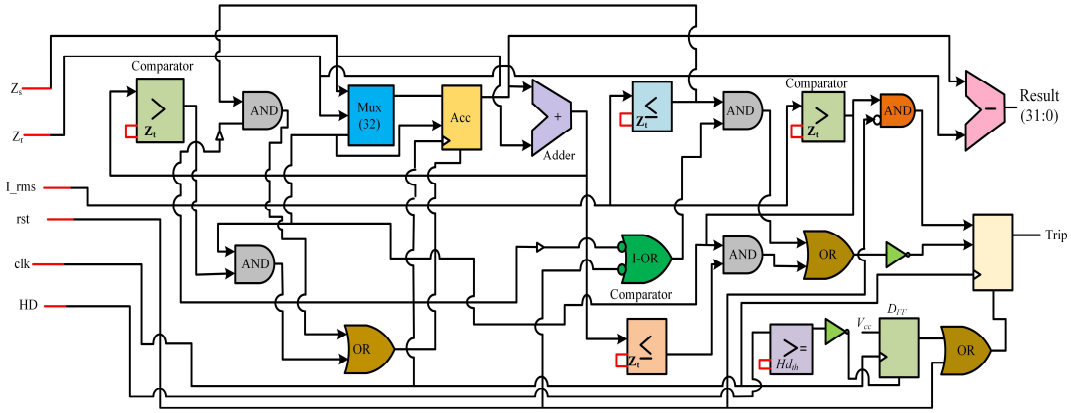

Figure 2.4 Data path for emulating the relay

2.3.5 Operation of Designed OCR

Figure 2.5 shows the algorithmic chart of the proposed algorithm designed on FPGA using hardware description language (HDL). The hardware relaying algorithm is triggered by selecting the parameters of the characteristic curve. In this design, integer arithmetic is used to perform the operation to make calculations simpler. A, B, p and t_r are the standard curve shaping constants of the relay. These are rounded to next integer value for improving the computation time of the relay without affecting its accuracy. The generalized multiplier for A, B, p, and t_r are taken as 4096, 64, 1, and 64. N_T is the target number used by the REM, which is set to a

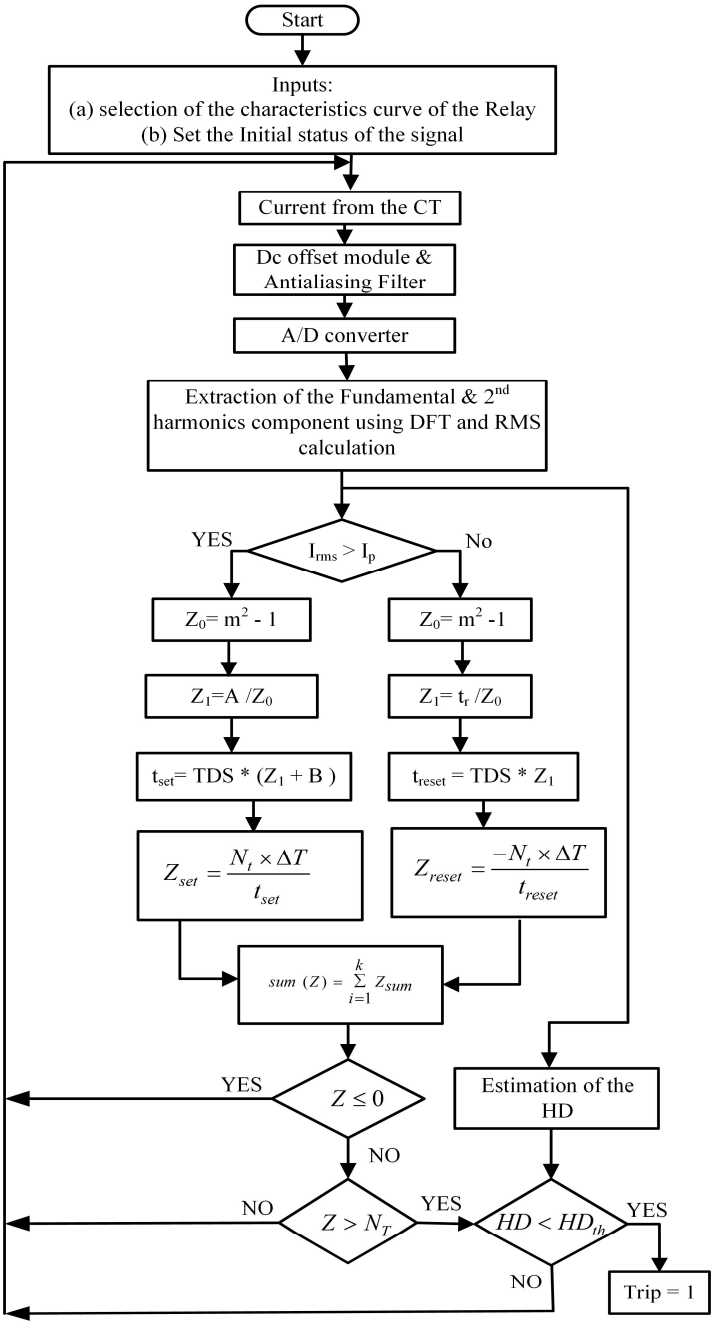

Figure 2.5 Algorithmic chart of overcurrent relay

predefined value of $6.4\times\times10^6$. The setting of I_p depends upon the current flowing through the network under normal condition for e.g. the pickup current may be chosen as 2.5 times of the normal current. After initialization, the RMS value of the signal is calculated and used for the computation of set and reset time of the OCR. At the arrival of the RMS values of current, summation $\sum Z_i$ is increased by the amount Z_s when $I_{RMS} > I_{p,}$ or decreased by Z_r when $I_{RMS} < I_p$. The most significant bit (MSB) of $\sum Z_i$ is checked at every clock event, which runs at 800 Hz. If MSB bit of $\sum Z_i$ is equal to zero and I_{RMS} is less than I_p then the contribution to the $\sum Z_i$ is zero. The updated value of $\sum Z_i$ is compared with N_T at every positive edge of the clock. Simultaneously, HD is also computed and compared with HD_{th}. The *TRIP* signal is generated when $\sum Z_i$ is greater than N_T and $HD < HD_{th}$.

2.4 Emulation Results

The complete hardware design is targeted to the Virtex®5 XC5VLX50T-3FF1136 FPGA chip [25]. The design is implemented using Verilog HDL. Xilinx ISE® 12.4 design suit environment with the "ISim M.81d" has been used to simulate the design. Onboard 100 MHz clock oscillator (clk) has been used to generate 40 kHz and 800 Hz clock using a clock module which is provided as an input to the ADC, DFT core and REM modules. Integer arithmetic based Verilog module is developed for computing average of the input signals. The CORDIC IP core within the RMS module is used to calculate the square root of the input signal received from the DFT core. The proposed relay has the ability to emulate the inverse characteristics of the standard relay. The hardware resource utilization for the implementation of the design is summarized in Table 2.2. It suggests only 9% of the available slice registers are utilized by the prototype. Hence, the space for the inclusion of more functionality is available. The relay operating time of the designed OCR for EI and VI characteristics are obtained from the FPGA. The design has been tested for the fixed amplitude sinusoidal. The sampled sinusoidal is the

Table 2.2 Summary of XC5VLX50T-3FF1136 device resource utilization

	XC5VLX50T-3FF1136 device summary	Used	% Utilization
1	Number of Slice Registers	2819	9
2	Number of Slice LUTs	9889	34
3	Number of used LUT-FF pairs	1527	13
4	Number of Bonded IOBs	80	16
5	Number of BUFG/BUFGCTRLs	4	12
6	Number of DSP48Es	22	45

input to this REM. The results are compared with the relay operating time of the IEEE Std. C37.112-96 for different values of M.

Different test conditions i.e. (5 different values of *M* and 10 different values of *TDS*) have been considered to validate the accuracy of the designed relay shown in Table 2.3 and Table 2.4. The percentage error of the relay trip time of the prototype with respect to IEEE standard inverse relay is shown in Table 2.5 and Table 2.6 for EI and VI characteristics respectively. The minimum and maximum percentage error are found to be 0.003% to 3.09% which is insignificant. The result suggests that the proposed relay meets the trip time requirements of the IEEE standard.

Table 2.3 IEEE standard and emulated operating time for EI time-current characteristic

TDS	IEEE Std. M=2.5	Emulated M=2.5	IEEE Std. M=4	Emulated M=4	IEEE Std. M=7	Emulated M=7	IEEE Std. M=10	Emulated M=10	IEEE Std. M=15	Emulated M=115
1	5.49	5.5022	2.0017	2.0090	0.709	0.7173	0.406	0.4145	0.247	0.2552
2	10.98	10.9871	4.0034	4.0093	1.418	1.4253	0.813	0.8192	0.495	0.5016
3	16.47	16.4766	6.0051	6.0094	2.127	2.1332	1.219	1.2239	0.742	0.7479
4	21.96	21.9662	8.0068	8.0104	2.836	2.8413	1.626	1.6286	0.990	0.9943
5	27.45	27.4644	10.008	10.009	3.546	3.5493	2.032	2.0334	1.238	1.2406
6	32.94	32.9454	12.010	12.009	4.255	4.2574	2.439	2.4381	1.485	1.4869
7	38.43	38.4653	14.011	14.009	4.964	4.9656	2.845	2.8430	1.733	1.7333
8	43.92	43.9243	16.013	16.011	5.673	5.6732	3.252	3.2477	1.980	1.9796
9	49.41	49.4374	18.015	18.010	6.382	6.3811	3.658	3.6522	2.228	2.2260
10	54.9	54.92096	20.017	20.010	7.092	7.0899	4.065	4.0572	2.475	2.4723

Table 2.4 IEEE standard and emulated operating time for VI time-current characteristic

TDS	IEEE Std. M=4	Emulated M=2.5	IEEE Std. M=4	Emulated M=4	IEEE Std. M=7	Emulated M=7	IEEE Std. M=10	Emulated M=10	IEEE Std. M=15	Emulated M=15
1	4.2262	4.2330	1.7983	1.8056	0.8995	0.9074	0.6891	0.6971	0.0077	1.3341
2	8.4525	8.4570	3.5967	3.6020	1.7991	1.8056	1.3782	1.3851	0.0060	0.5220
3	12.6787	12.682	5.3950	5.3985	2.6986	2.7039	2.0672	2.0731	0.0044	0.2572
4	16.905	16.904	7.1933	7.1949	3.5982	3.6020	2.7563	2.7612	0.0027	0.1204
5	21.1312	21.130	8.9917	8.9914	4.4977	4.5003	3.4454	3.4494	0.0013	0.0473
6	25.3574	25.363	10.7900	10.7878	5.3972	5.3985	4.1345	4.1375	0.0004	0.0134
7	29.5837	29.5890	12.5883	12.5865	6.2968	6.2968	4.8236	4.8258	0.0018	0.0445
8	33.8099	33.8000	14.3867	14.3806	7.1963	7.1949	5.5126	5.5135	0.0034	0.0751
9	38.0361	38.0410	16.1850	16.1770	8.0959	8.0931	6.2017	6.2014	0.0052	0.1017
10	42.2624	42.2849	17.9833	17.9735	8.9954	8.9914	6.8908	6.8903	0.0065	0.1132

Table 2.5 (%) error between IEEE standard and emulated relay operating time

TDS	Percentage Error Between the IEEE Standard and Emulated for EI Characteristic				
	M=2.5	M=4	M=7	M=10	M=15
1	0.2231	0.3678	1.1416	1.9686	3.0990
2	0.0654	0.1472	0.4837	0.7532	1.2957
3	0.0405	0.0711	0.2644	0.3563	0.6946
4	0.0283	0.0448	0.1576	0.1517	0.3941
5	0.0527	0.0118	0.0935	0.0339	0.2137
6	0.0162	0.0036	0.0507	0.0487	0.0935
7	0.0918	0.0141	0.0235	0.0983	0.0076
8	0.0100	0.0117	0.0068	0.1437	0.0516
9	0.0555	0.0285	0.0267	0.1810	0.1023
10	0.0381	0.0334	0.0289	0.2028	0.1428

Table 2.6 (%) error between IEEE standard and emulated relay operating time

TDS	Percentage Error Between the IEEE Standard and Emulated for VI Characteristic				
	M=2.5	M=4	M=7	M=10	M=15
1	0.1631	0.4066	0.8847	1.1619	1.3341
2	0.0538	0.1497	0.3620	0.5038	0.5220
3	0.0287	0.0659	0.1974	0.2893	0.2572
4	0.0002	0.0229	0.1079	0.1813	0.1204
5	0.0212	0.0031	0.0582	0.1164	0.0473
6	0.0250	0.0202	0.0251	0.0732	0.0134
7	0.0196	0.0140	0.0011	0.0456	0.0445
8	0.0269	0.0418	0.0187	0.0168	0.0751
9	0.0130	0.0490	0.0335	0.0034	0.1017
10	0.0533	0.0542	0.0442	0.0060	0.1132

2.5 Experiment setup for HIL Testing of FPGA Prototype

2.5.1 Test System

The test system for the verification of the OCR prototype is developed in RSCAD/RTDS [138] as shown in Figure 2.6. It consists of power sources, circuit breakers (CBs), transmission lines, current transformer (CT), and different types of fault. The parameters of this system are summarized in Table A. 1 of the Appendix.

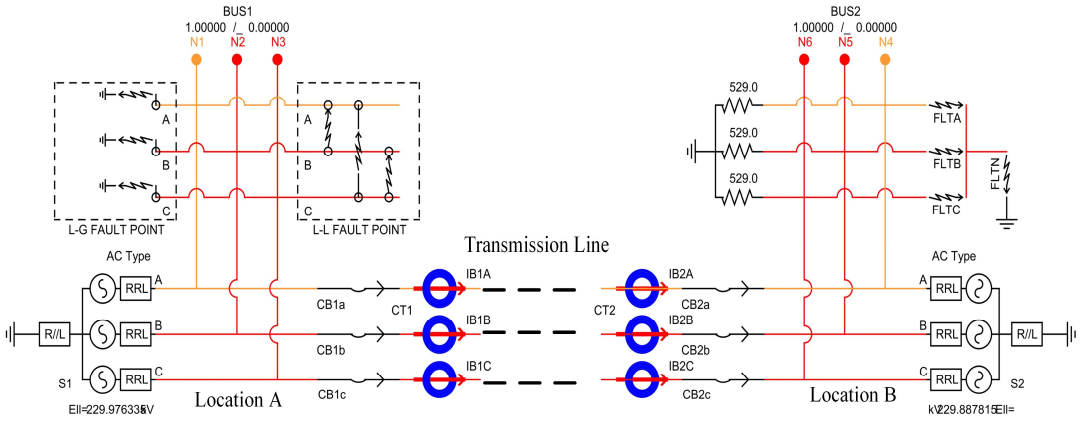

Figure 2.6 Test module of OCR in RTDS

2.5.2 Interfacing between FPGA and RTDS

The hardware set-up for the HIL verification of OCR using the RTDS is shown in Figure 2.7. The real-time current signal received from the current transformer (CT) has been taken out from the analog output port of the RTDS through the Gigabit Transceiver Analogue Output Card (GTAO). The GTAO card has its own current to voltage (C2V) converter with the output range of (±)10 V to communicate with external peripherals. To validate the proposed OCR, the

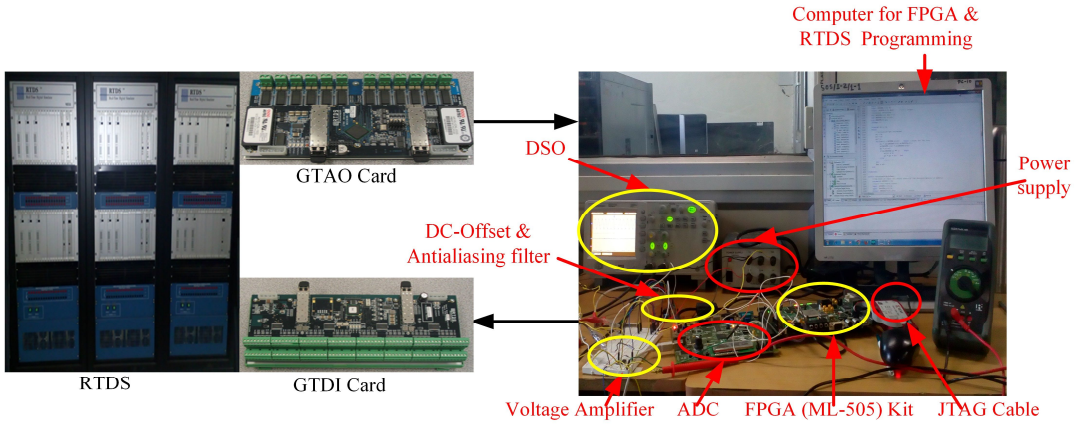

Figure 2.7 Hardware-setup for HIL verification of OCR prototype

output port of the GTAO card is scaled-up to detect the maximum swing of 1.2 V (P-P). The voltage signal is passed through the dc offset module (offset=1.65 V). The output signal of this module is passed through analog low-pass filter (AAF), which is used to block the unwanted high-frequency component present in the signal [139]. The BW of the developed AAF is selected as 250 Hz such that all the required components (fundamental and 2nd harmonics component) of the power frequency are present in the input signal. The filtered signal is fed into ADC which provides 14-bit digital data. The output of the ADC is converted to the 16-bit 2's complement data and passed to the DFT processing core where the magnitude of the fundamental component of signal is extracted. CORDIC core is used to estimate the RMS of the received data and transferred to the REM. After processing the data, if the condition for tripping is satisfied, a trip signal is generated from the developed OCR and is given to the CB of the RTDS through the Gigabit Transceiver Digital Input Card (GTDI). A voltage amplifier is used as an intermediate circuit to amplify the digital trip signal generated by FPGA required by the GTDI card of RTDS. Various test conditions have been considered for the verification of the proposed prototype. Agilent digital storage oscilloscope (DSO)-1012A, 100*MHz*, is used to monitor the output current signal coming from the GTAO card and the trip signal from REM of the OCR. Considering the identical conditions, the tripping time of the developed prototype of the OCR is compared with the trip time of the OCR used within RTDS [140].

Figure 2.8 gives the signal communication latency produced by each of modules i.e. signal conditioning module (SCM), ADC, FPGA (DFT, RMS, and REM) as shown in the figure below. Each module has specific communication latency, which was obtained from datasheet and by experimentation and is mentioned in the figure. The power system test case is simulated in the RTDS and measured current signals are taken out by the GTAO card of RTDS. Here, the maximum communication latency between GPC processor card and GTAO card is 9.203μs [138]. Next, the SCM has AAF and dc-offset modules. Communication latency of this module

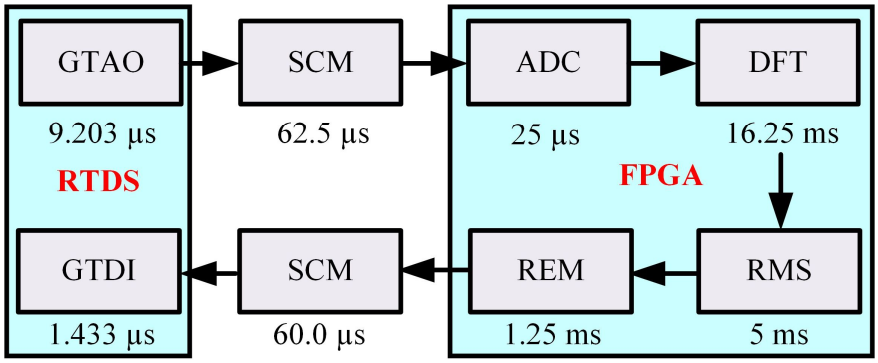

Figure 2.8 Latency involve in HIL verification

is 62.5μs. The latency of the ADC module is ~25 µs. The signal is passed to the FPGA board on which DFT, RMS and REM modules have been designed which is running on the master clock of 100 MHz. The FPGA processing is taking 400 µs. From FPGA *TRIP* signal passes through the SCM to make it compatible with the GTDI card of the RTDS by using the voltage amplifier. The latency of SCM and GTDI [138] card are ~60μs and 1.433μs. Total latency of the complete design is 558μs.

2.6 Hardware-in-Loop Verification of OCR Prototype

In this section, HIL verification of the developed OCR has been discussed by considering its characteristics viz. inverse characteristic and operational performance of the relay.

Inverse characteristics of the OCR i.e. extremely inverse (EI) and very inverse (VI) of the designed relay is verified with different values of I_p and TDS. The operation of the relay is verified by considering under different operating conditions i.e. line to ground (LG) fault, line to line (LL) fault and line-line-line-ground (LLLG) fault. Further, the effect of fault resistance on the relay tripping time is also verified. Along with that, coordination of the relay has been illustrated for primary and backup protection. Also, the performance of the designed OCR has also been evaluated in the presence of inrush current.

2.6.1 Characteristic verification of the designed OCR

Various cases of characteristic conditions for HIL verification have been considered to verify its functional inverse characteristics (EI and VI) and discussed in the following subsections:

Case: 1 *EI characteristic at TDS=1*

A test case for the verification of EI characteristic of the OCR prototype with TDS=1 and I_p = 0.9A has been considered here. The output of CT, representing the line current, which is converted to a voltage signal through the GTAO card is shown in Figure 2.9 as a blue coloured signal. Status of the trip signal generated by the prototype is further passed through an amplifier to act as the digital input in pink colour for the GTDI card as shown in Figure 2.9. In Figure 2.10, Signal *CB1*, *FLT*, *TRIP_FPGA* and *TRIP_RTDS* representing the status of the CB connected to the OCR, status of fault, the trip signal generated by the FPGA and trip signal generated by RTDS respectively. The status of these signals is shown in Figure 2.10 at three different instants of time. The signal *CB1*=1 shows the CB is close whereas *CB1*=0 gives the information about the CB which is in the off state and current does not flow through the CB. FLT=1 represents the occurrence of the fault whereas FLT=0 represents the normal condition. *TRIP_FPGA*=0 and *TRIP_RTDS*=0 are the trip signals in off state and are generated by the

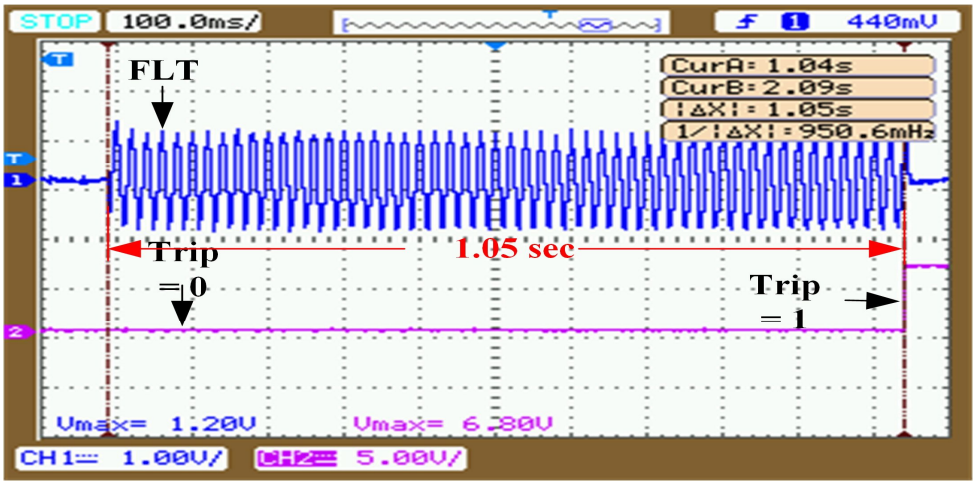

Figure 2.9 Trip signal generated by FPGA at TDS=1 for EI characteristic

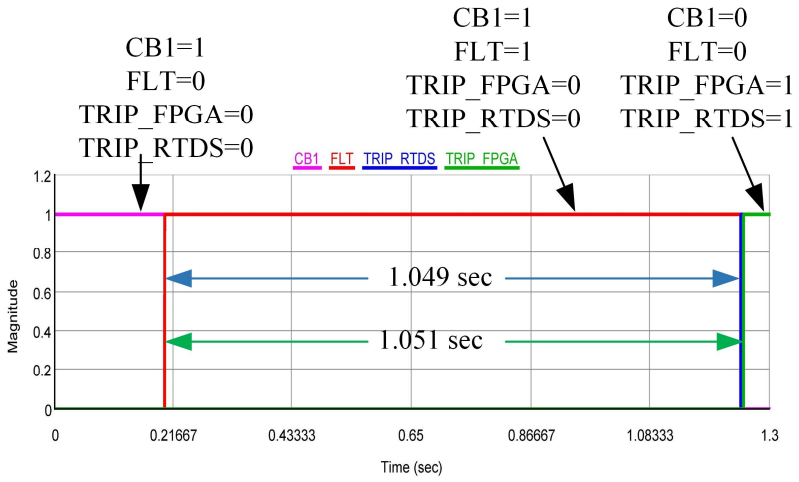

Figure 2.10 EI OCR at TDS = 1

prototype and RTDS respectively. Whereas *TRIP_FPGA*=1 and *TRIP_RTDS*=1 are the trip signal generated by RTDS and FPGA respectively, which are in the active high state. In this condition, CB will be off and current will not be allowed to flow through the CB.

In the case considered, a fault at Location_A occurred at t=0.2002 sec. For this fault (a-g), the maximum fault current of 8.23A, equivalent to 1.20V is observed by the DSO as shown in Figure 2.9. The trip time taken by the prototype to trip the CB is 1.05 seconds, while by the RTDS it is 1.049 seconds as shown in Figure 2.10.

Case: 2 *EI characteristic at TDS=2*

In this case, the performance of the OCR has been tested for EI characteristic with TDS=2 and I_p=0.90A. Figure 2.11 shows the trip signal generated by the FPGA prototype. Here also the input of the prototype is shown by a blue colored signal. Status of *CB*, *FLT* and *TRIP*

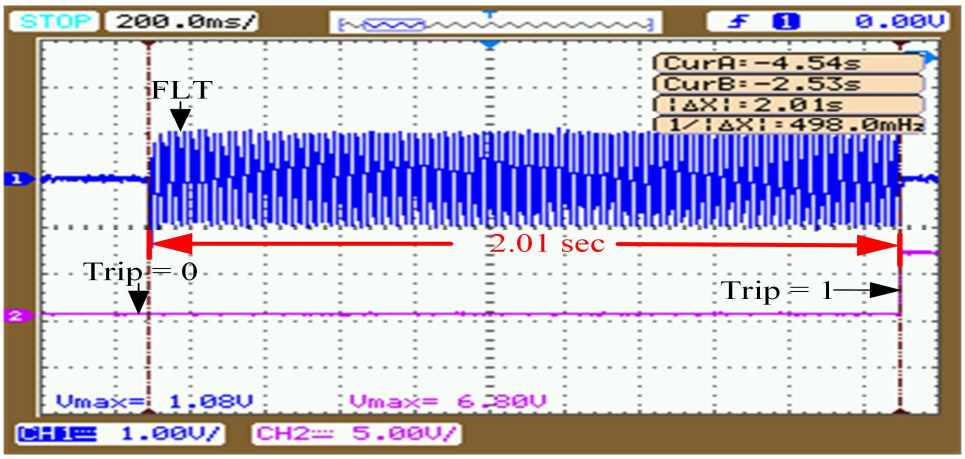

Figure 2.11 Trip signal generated by FPGA for EI OCR at TDS=2

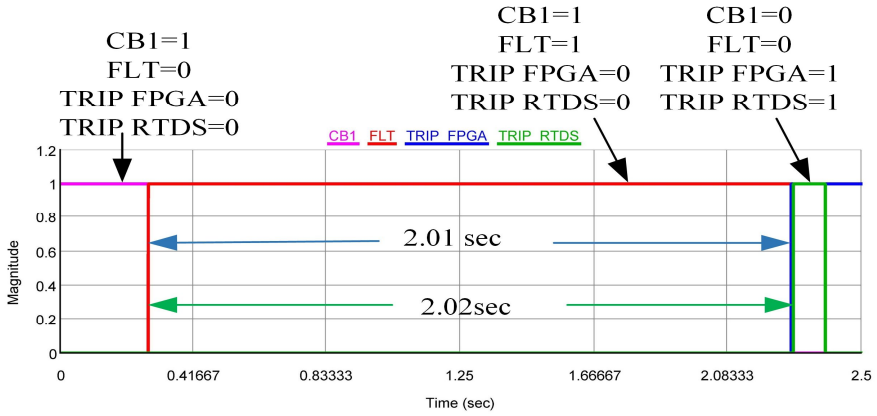

Figure 2.12 EI OCR at TDS=2

signals generated by FPGA and RTDS at different instants of time i.e. before, after the occurrence of the fault and at the tripping condition, are given in Figure 2.12.

In this case, the fault is occurred at t=0.3003 seconds. *TRIP* signals are generated by the prototype and RTDS at t=2.31 seconds and t=2.32 seconds, respectively. Here the tripping time of the prototype is 2.01 seconds while the tripping time of the RTDS relay is 2.02 seconds.

Case: 3 *VI characteristic at TDS=1*

In this section, the test result of the OCR prototype is discussed for the VI characteristic with TDS=1 and I_p=1.05A. Figure 2.13 shows the trip signal generated by FPGA. Status of *CB*, *FLT*, and *TRIP* signal generated by FPGA and RTDS at three different instant of time is given in Figure 2.14. *CB1*=1, *FLT*=0, *TRIP_FPGA*=0 and *TRIP_RTDS*=1 are the status of the signals before the occurrence of the fault. When the fault occurs, the status of the *CB1*, *FLT*, *TRIP_FPGA* and *TRIP_RTDS* signals are 1, 1, 0 and 0 respectively. While, after the occurrence of the trip signal, the status of these signals are *CB1*=0, *FLT*=0, *TRIP_FPGA*=1 and *TRIP_RTDS*=1 shown in Figure 2.14.

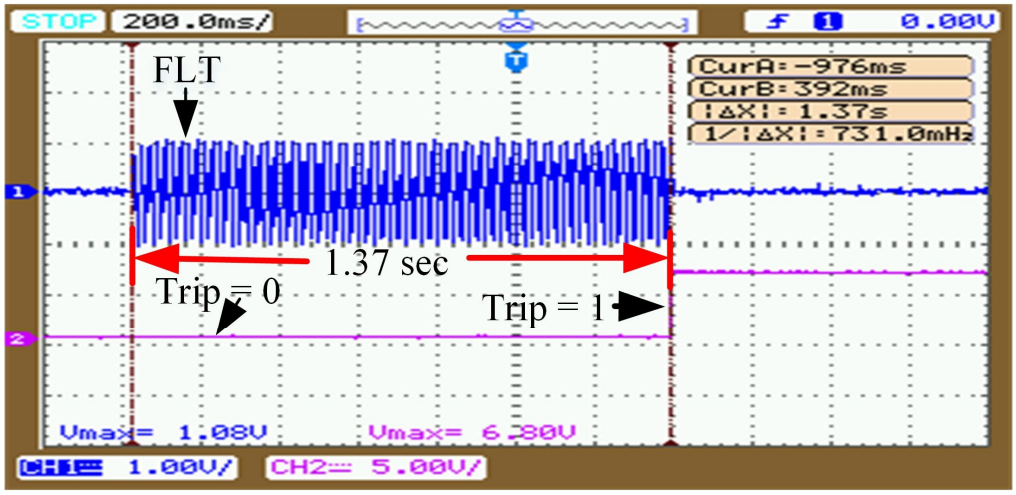

Figure 2.13 Trip signal generated by FPGA at TDS=2 for VI characteristic

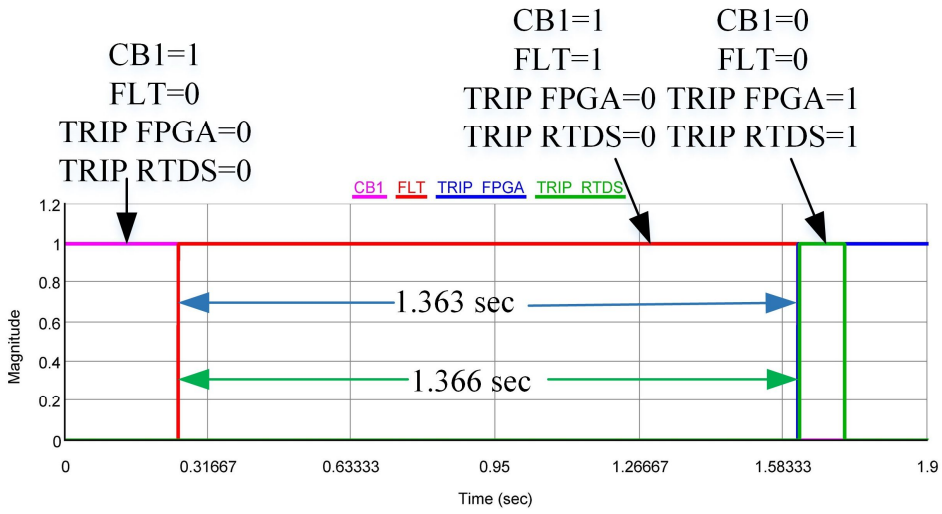

Figure 2.14 Test results for VI characteristic at TDS=2 in close loop condition

In this case, the fault is occurred at t=0.25 seconds and the *TRIP* signals are generated by the prototype and the RTDS relay (after the occurrence of the fault) at 1.613 seconds and 1.6166 seconds respectively. Therefore, relay tripping time of the prototype and RTDS relay is 1.363 seconds and 1.366 seconds, respectively.

Comprehensive testing for relay tripping time between FPGA and RTDS platforms were performed. Many test cases for a different set of characteristics performance are considered to validate the algorithm and its implementation by varying its internal parameters viz. I_P and TDS. The error between FPGA and RTDS relay tripping time is found to be within the acceptable range of 1.06 %. The findings are reported in Table 2.7.

Table 2.7 Characteristics verification of the OCR with different values of Ip and TDS

	TDS	I_p (Amp)	FPGA	RTDS	% error
			Trip time (sec)		
Extremely Inverse (EI)	1	0.905	1.051	1.049	0.214
		1.273	2.014	2.013	0.079
		1.515	2.865	2.873	0.271
		2.1	5.956	5.941	0.250
		2.69	11.091	11.091	0
		3.10	16.956	16.87	0.509
	2	0.886	2.005	2.02	0.722
		1.27	4.014	4.004	0.249
		1.54	5.97	5.946	0.404
Very inverse (VI)	1	0.84	1.046	1.045	0.143
		1.05	1.363	1.366	0.205
		1.35	2	1.987	0.609
		1.98	4.010	4.010	0
		2.565	7.190	7.193	0.044
	2	2.732	17.09	16.91	1.064

2.6.2 Operational Verification of the designed OCR

The different cases of line to ground (LG) fault, line to line (LL) fault, line-line-line-ground (LLLG fault) and fault resistance at different fault inception angle have been considered for operational verification of the designed OCR. These faults were incepted externally at Location_A and Location_B as shown in Figure 2.6.

Case: 1 *EI characteristic at TDS=1 and I_p=1A*

In this case, the performance of the proposed OCR is tested for EI characteristic with TDS= 1 and I_p = 1 A, when a fault is occurred at location B as shown in Figure 2.6. In this case, fault occurs at θ (fault inception angle) = 2π/3 or t= 0.1104 sec. For this line-to-line (LL) fault (a-b), maximum fault current of 13.69 A is observed by the CT on RTDS. The output of the CT is converted to voltage signal through GTDI card and its magnitude is (1.04V) shown in Figure 2.15 as blue coloured signal; whereas, pink coloured signal shows the status of the *TRIP* signal generated by the FPGA. In Figure 2.16, Signal *CB1*, *FLT*, *TRIP_FPGA* and *TRIP_RTDS* representing the status of the CB connected to the OCR, status of fault, the trip signal generated by the FPGA and trip signal generated by RTDS respectively. The trip time taken by the

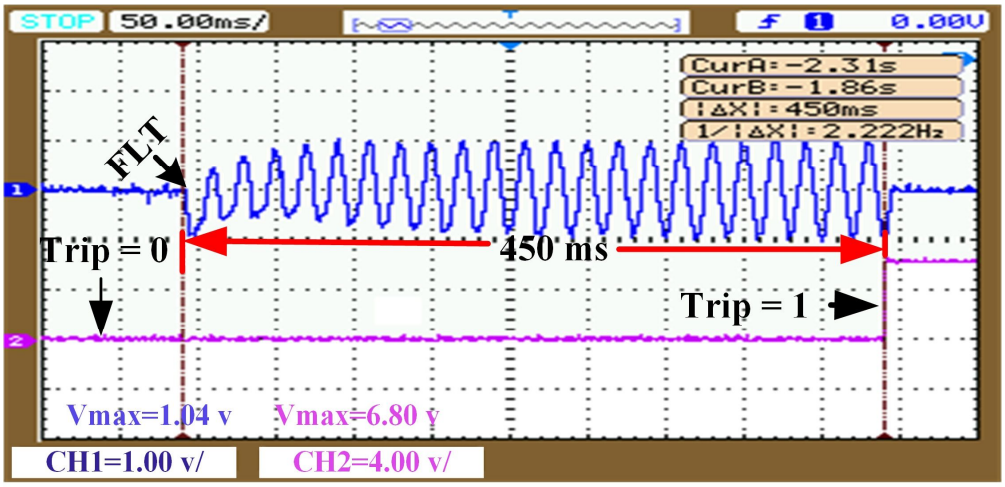

Figure 2.15 Test results for EI characteristic when LL fault occurred at location B

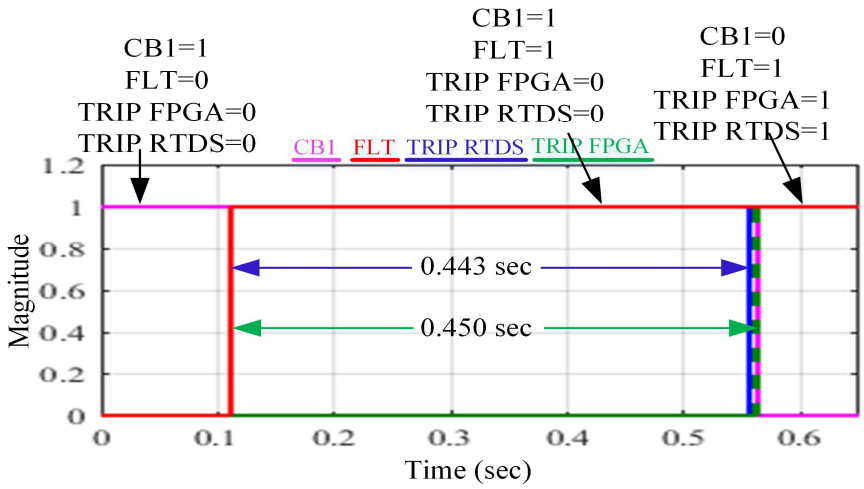

Figure 2.16 Signal generated by FPGA and RTDS for EI OCR at TDS = 1

prototype relay to issue trip signal for CB1 is 0.450 sec, while by the OCR in RTDS it is 0.443 sec for the same.

Case: 2 *VI characteristic at TDS=1 and I_p=0.886A*

In this case, the performance of the proposed OCR is tested for VI characteristic with TDS= 1 and I_p =0.886A, when LL fault occurs at location B as shown in Figure 2.6. Here, also the fault occurs at θ = 2π/3 or t= 0.1104 sec. In this LL fault, the maximum fault current of 13.72 A is observed by the CT in RTDS and the respective voltage signal is 1.20V as shown in Figure 2.17 as a blue colour. Similarly, Figure 2.18 shows the respective signal as discussed in case I. Here, the tripping time of the prototype relay is 0.668s while for RTDS relay it is 0.660s shown in Figure 2.17 and Figure 2.18 respectively.

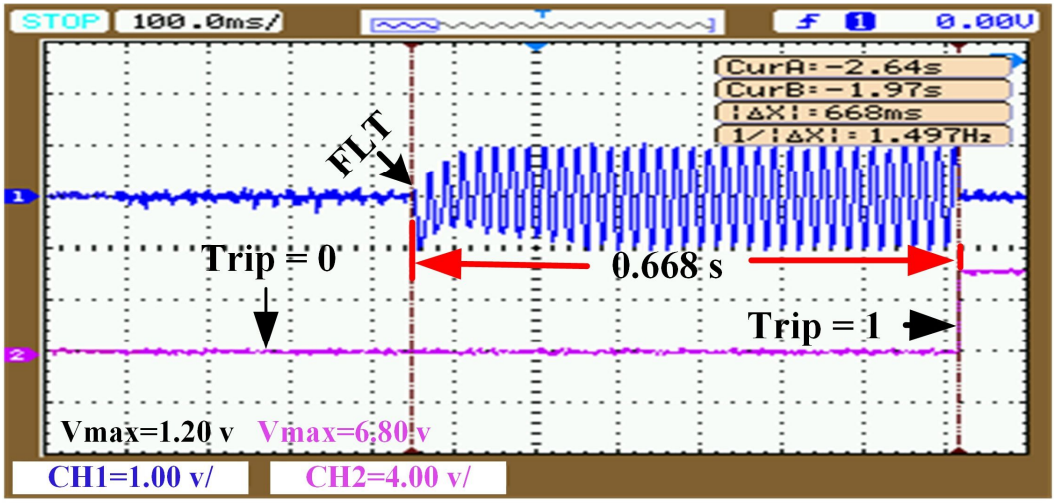

Figure 2.17 Test results for VI characteristic when LL fault occurred at location B

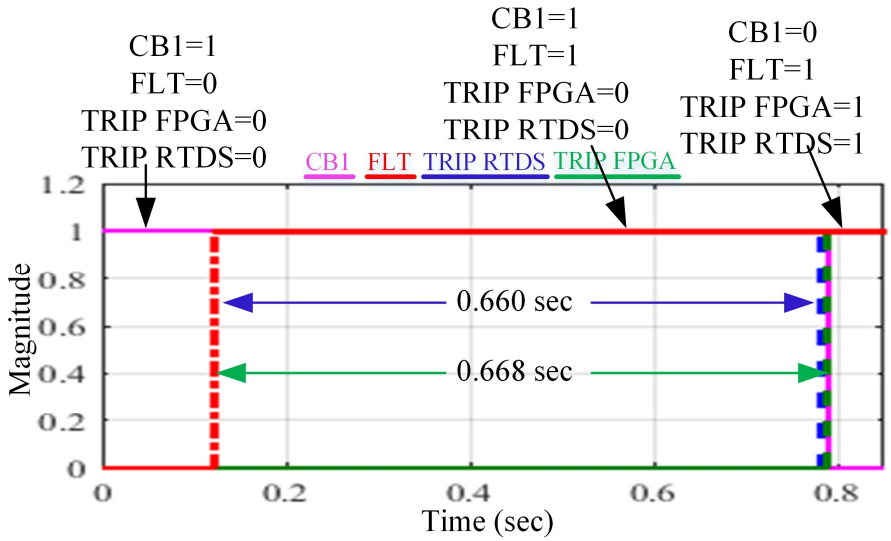

Figure 2.18 Signal generated by FPGA and RTDS for VI OCR at TDS = 1

Case: 3 *EI characteristic at TDS=2*

In this case, performance of the proposed OCR is tested for EI characteristic with TDS = 2 and I_p = 0.886A, for a LLLG fault at location B shown in the Figure 2.6. In this case, fault occurs at θ = π/2 (or t= 0.1406 sec) and the maximum fault current of 14.63A is observed by the CT on RTDS. Output of the CT is converted to voltage signal through GTAO card and its magnitude is (1.12V) shown in Figure 2.19 as a blue coloured signal, whereas, pink coloured signal shows the status of the *TRIP* signal generated by the FPGA. In Figure 2.20, Signal *CB1*, *FLT*, *TRIP_FPGA* and *TRIP_RTDS* representing the status of the CB connected to the OCR, status of fault, the trip signal generated by the FPGA and trip signal generated by RTDS

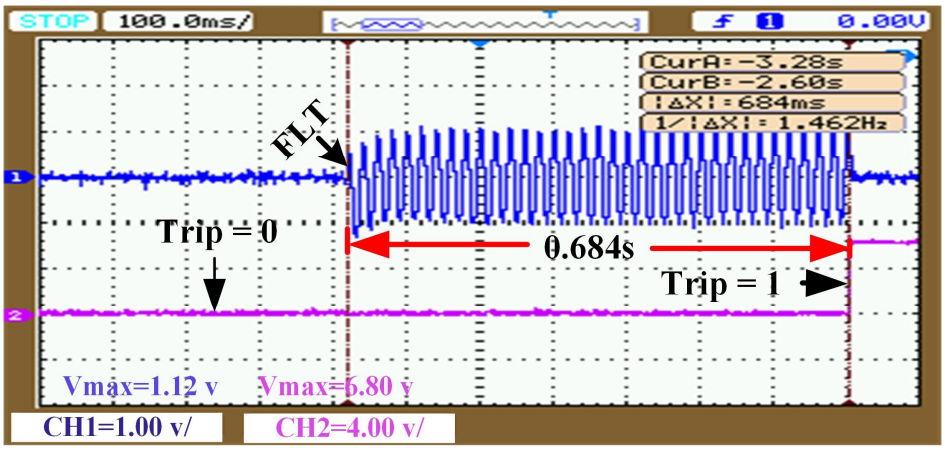

Figure 2.19 Test results for EI characteristic when LLLG fault occurred at location B

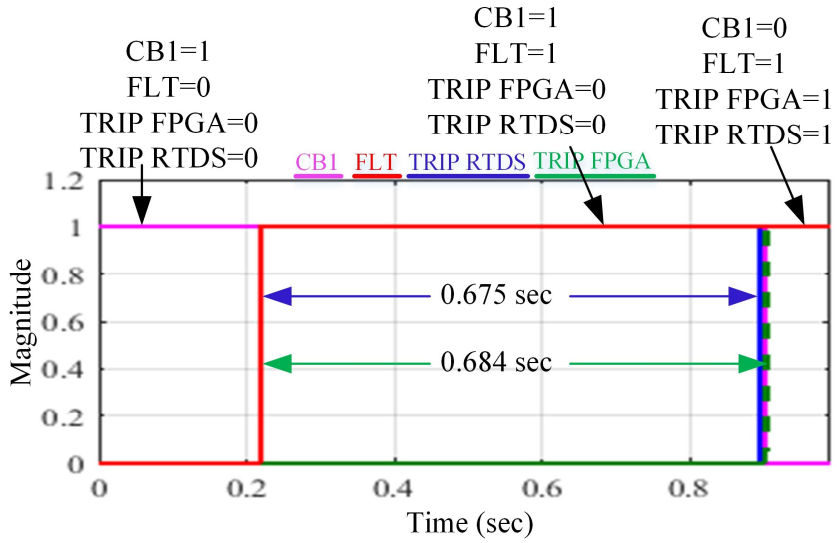

Figure 2.20 EI OCR at TDS = 1

respectively. Here, the tripping time of the prototype OCR is 0.684s while the tripping time of the RTDS relay is 0.675s as shown in Figure 2.19 and Figure 2.20 respectively.

Case: 4 *VI characteristic at TDS=1*

In this case, the performance of the proposed OCR is tested for VI characteristic with TDS= 1 and I_p =0.886, when LLLG fault occurs at location B as shown in Figure 2.6. Here also, a fault is initiated at θ = π/4 (or t= 0.1406 sec) and the magnitude of maximum fault current is observed to be 18.01A by the CT on RTDS, which is equivalent to 1.24 V as shown in Figure 2.21 in blue colour. Similarly, Figure 2.22 shows the status of the various signal as discussed in case I. Now, the relay tripping time of the prototype OCR and RTDS relay is 0.684s and 0.675s respectively, as shown in Figure 2.21 and Figure 2.22. The error between FPGA and RTDS relay tripping time is found to be within the acceptable range of 1.3 %.

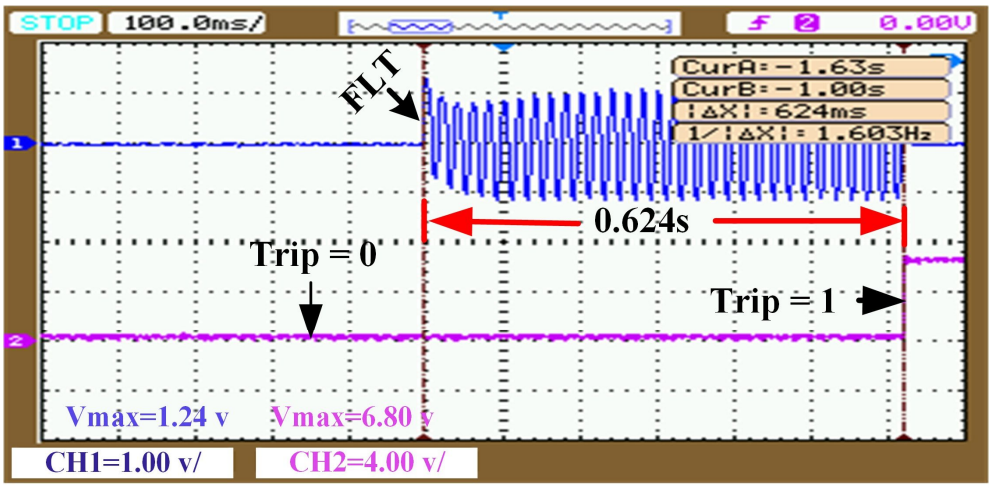

Figure 2.21 Test results for VI characteristic when LLLG fault occurred at location B

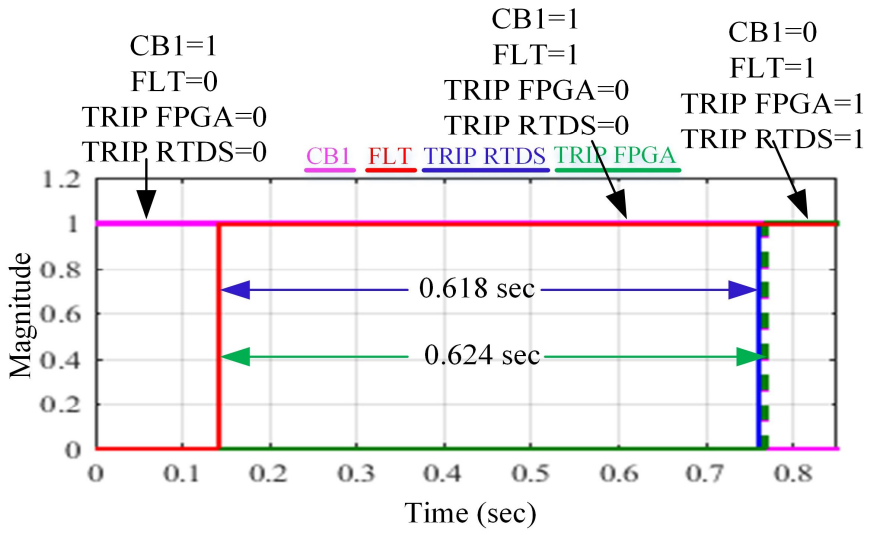

Figure 2.22 Signal generated by FPGA and RTDS relay for EI OCR at TDS=1

2.6.2.1 Performance with different fault resistances and inception angles

The OCR is tested for EI characteristic with TDS=1 and I_p=0.886A, and the value of fault resistance (R_f) is taken as 0.1Ω and 5Ω. The fault is incepted at Location_B given in Figure 2.6. The case with R_f of 0.1Ω, a line-to-ground (A-G) fault occurs at θ = 0° (at t=0.213 sec). A maximum fault current of 13.57 A is observed by the CT on RTDS. The corresponding voltage signal through the GTAO card is shown in Figure 2.23 in blue colour and the generated *TRIP* signal is shown in pink colour. The tripping time taken by FPGA and RTDS relays is 0.792 sec and 0.784s respectively, as shown in Figure 2.23 and Figure 2.24. The error between FPGA and RTDS relay tripping time is found to be within the acceptable range of 1%.

In another case with R_f = 5Ω, the value of the fault current is observed as 6.98A. The equivalent voltage is shown in Figure 2.25. The tripping time taken by FPGA and RTDS relays

are 1.22s and 1.21s respectively, as shown in Figure 2.25 and Figure 2.26. The error between FPGA and RTDS relay tripping time is found to be within an acceptable range of 0.8 %.

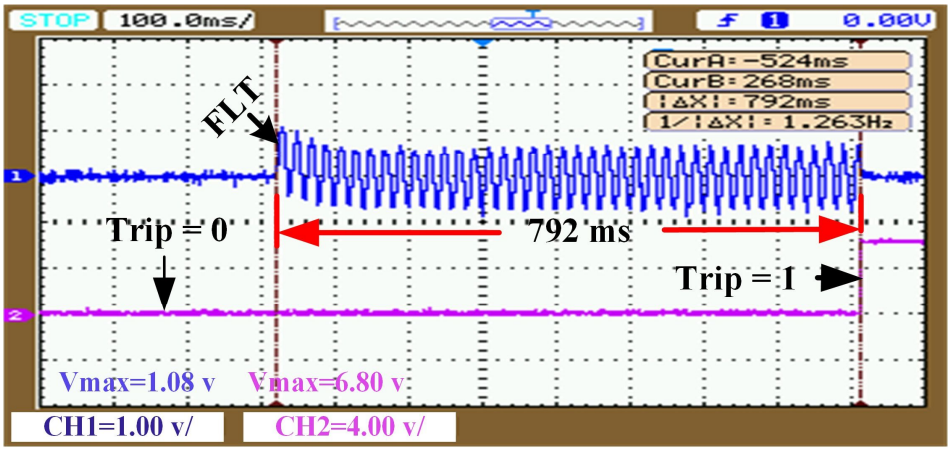

Figure 2.23 Test results for EI characteristic when LG fault incepted

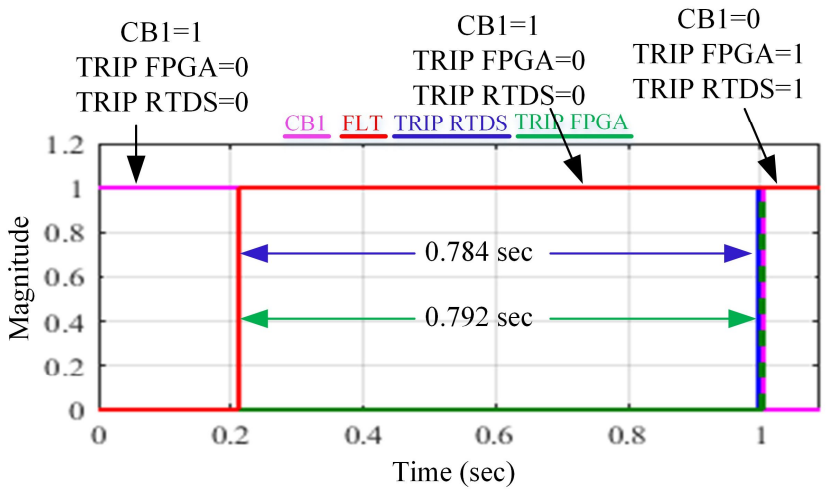

Figure 2.24 EI OCR at TDS = 1, when R_{on}=0.1Ω

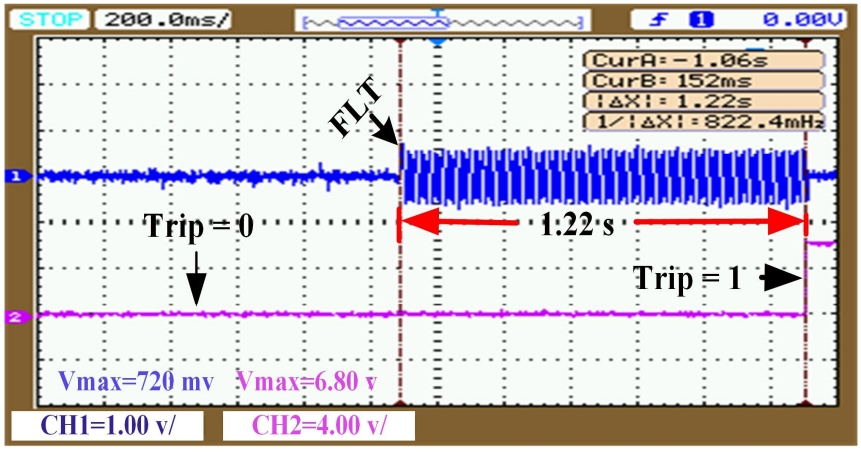

Figure 2.25 When LG (a-g) fault incepted, when R_{on}=5Ω

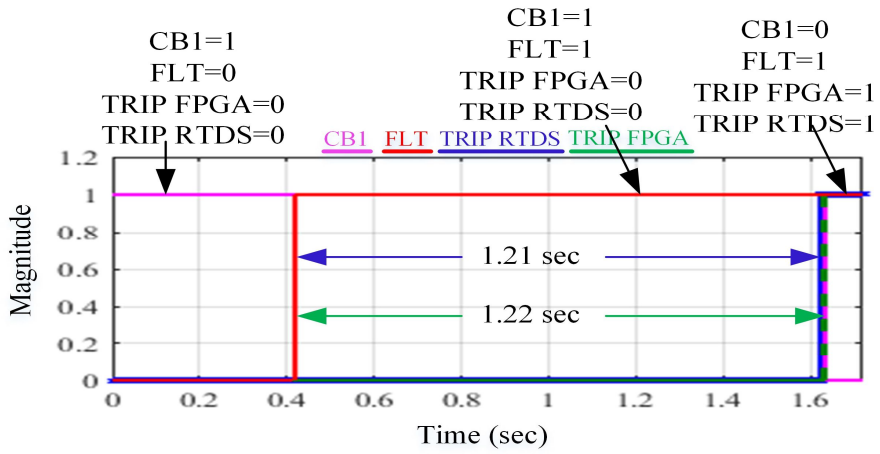

Figure 2.26 VI OCR, when Ron=5Ω

Table 2.8 Operational verification of the OCR with different operating conditions

	Types of Fault	Fault Inception Angle	Fault Resistance (Ω)	I_p	TDS	Trip time in sec		% error
						FPGA	RTDS	
Extremely Inverse (EI)	LG	(0)°	0.1	0.886	1	0.789	0.784	0.63
		(0)°	5			2.226	2.220	0.27
		(π/2)°	0.1			0.781	0.783	0.25
		(π/2)°	5			2.224	2.218	0.27
	LL	(0)°	0.1			0.374	0.369	1.35
		(0)°	5			0.707	0.699	1.14
		(π/2)°	0.1			0.377	0.371	1.61
		(π/2)°	5			0.705	0.699	0.85
	LLLG	(0)°	0.1			0.309	0.303	1.98
		(0)°	5			0.563	0.555	1.44
		(π/2)°	0.1			0.312	0.306	1.96
		(π/2)°	5			0.565	0.561	0.71
Very inverse (VI)	LG	(0)°	0.1			0.942	0.937	0.53
		(0)°	5			1.946	1.941	0.25
		(π/2)°	0.1			0.944	0.934	1.07
		(π/2)°	5			1.961	1.951	0.51
	LL	(0)°	0.1			0.667	0.660	1.06
		(0)°	5			0.889	0.888	0.11
		(π/2)°	0.1			0.669	0.663	0.90
		(π/2)°	5			0.899	0.892	0.78
	LLLG	(0)°	0.1			0.688	0.681	1.02
		(0)°	5			0.801	0.792	1.13
		(π/2)°	**0.1**			**0.684**	**0.675**	**1.33**
		(π/2)°	5			0.807	0.796	1.38

Comprehensive experimental results for different set of inception angle in combination with different fault resistance and types of fault for both the EI and the VI relay characteristics are presented in Table 2.8. The error between FPGA and RTDS trip time is found to be within the acceptable range of 0.11%-1.98%.

2.6.2.2 Coordination of OCRs

The coordination of the designed OCR with other relays in the network has also been verified. For that purpose, two independent relays placed across two ends of the transmission line have been considered as shown in Figure 2.6. These two relays are used to operate the respective circuit breaker CB1 and CB2. If a fault occurs at Location_B, Relay_2 acts as primary protection and Relay_1 acts as secondary or backup protection. Similarly, Relay_1 and

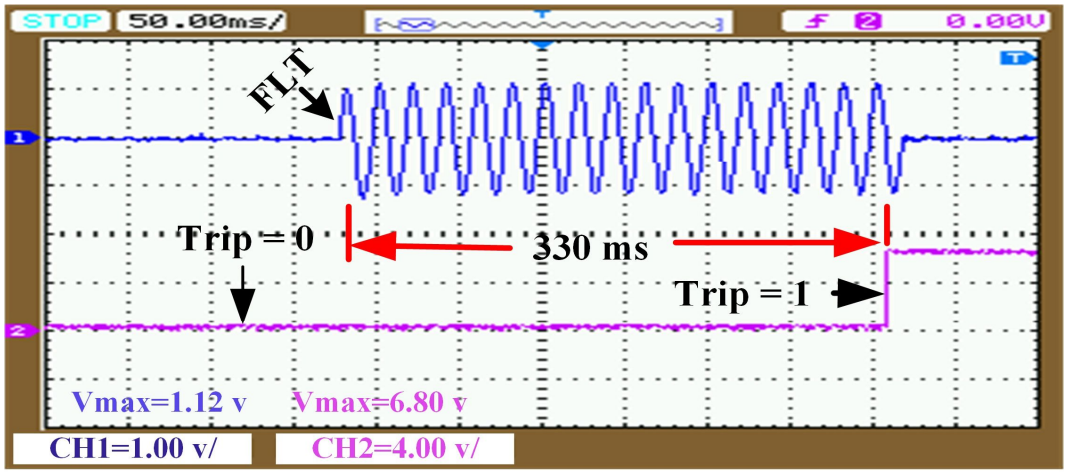

Figure 2.27 Trip signal generated by FPGA for EI OCR at TDS=1

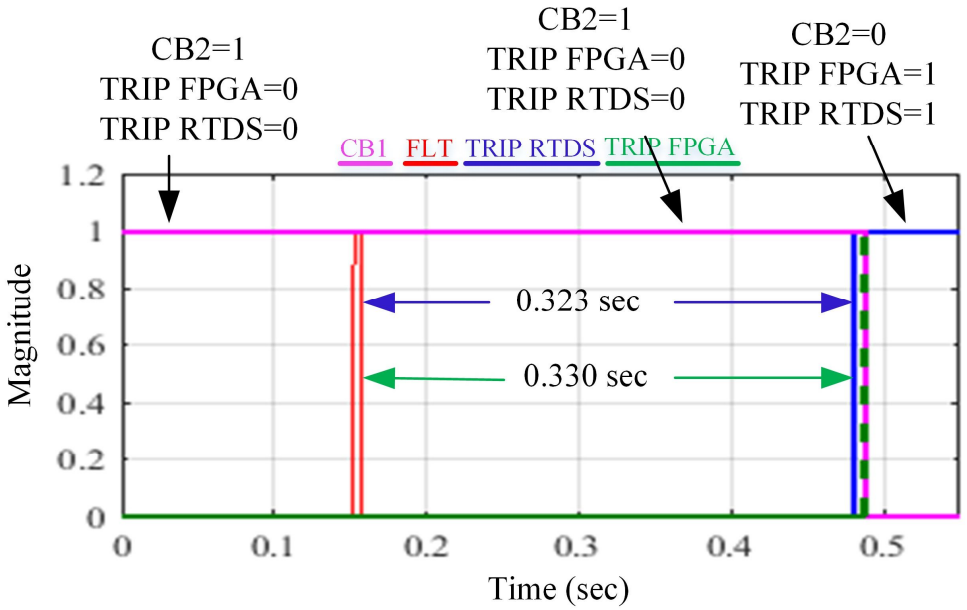

Figure 2.28 Signal generated by FPGA and RTDS relay for EI OCR at TDS=1

Relay_2 act as the primary and secondary protection for a fault occurring at Location_A. In the current study, EI characteristic of OCR have been considered to verify the relay coordination. A line-to-ground (A-G) fault is incepted at Location_B. The values of pick-up settings for both the OCRs are 0.5 Amp and TDS settings of Relay_1 and Relay_2 are 1 and 2 respectively. The fault occurs at t = 0.1104 sec. The fault current of 8.422A is observed by CT2 in RTDS as shown in Figure 2.27. The tripping time of the designed prototype occurs at 0.330 sec, while the tripping time of the RTDS relay is 0.323 sec as shown in Figure 2.28. Similarly, the fault current 8.31A is observed by CT1 on RTDS is shown in Figure 2.29. Here the tripping time of the prototype is 0.664 sec while the tripping time of the RTDS relay is 0.661sec as shown in Figure 2.30. The error between FPGA and RTDS relay tripping time is found to be within the acceptable range of 0.4 %.

From the above discussion, the coordination between the relays across the transmission line has been verified with the designed relay prototype.

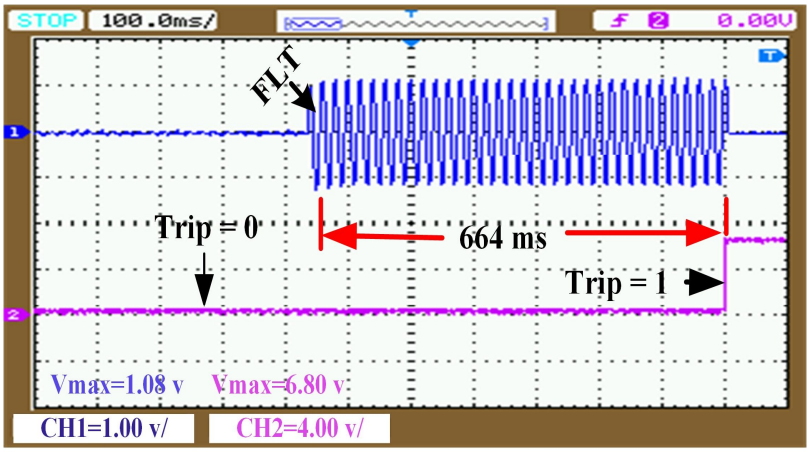

Figure 2.29 Test results for EI characteristic based OCR at TDS=2

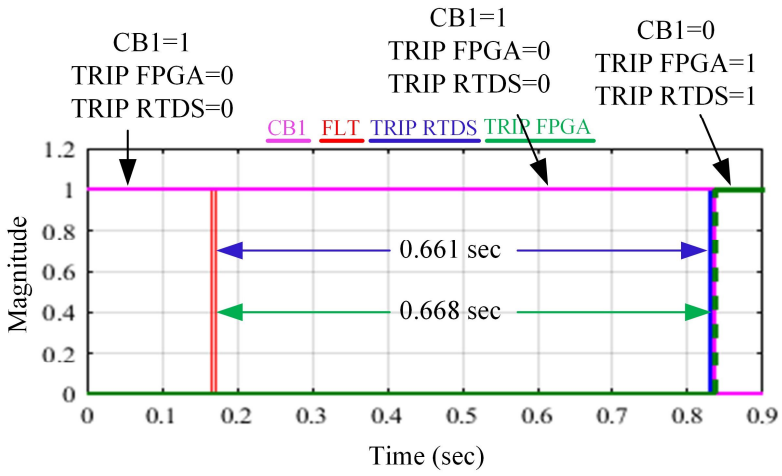

Figure 2.30 Signal generated by FPGA and RTDS relay for VI OCR

2.6.2.3 Performance of the proposed OCR during transformer inrush condition

In this case, the operation of the developed prototype has been verified during transformer inrush condition with EI characteristic. The considered parameters of the relay are TDS=1, I_p=0.05A and HD_{th}=36 %. Figure 2.31*a* shows the current signal obtained from the CT in the presence of transformer inrush and the magnitude of this current is 4.12A. Trip_0 is the output of the FPGA when the effect of inrush is not considered. The transition of this signal occurs as shown in Figure 2.31*b*, because of the condition $I_{rms} > I_p$. Signal *HD* is shown in Figure 2.31*c* and its values reached to 150% due to transformer energization. Figure 2.31*d* shows the status of the signal when HD is greater than HD_{th}. When $HD>HD_{th}$, an intermediate signal is generated as shown by Trip_1=1, which indicates the inrush effect. Also, under the condition $HD<HD_{th}$, the signal Trip_1=0 represents the absence of inrush effect. Here, the effective Trip signal is generated by the prototype when both the conditions Trip_0=1 and Trip_1=0 are met simultaneously.

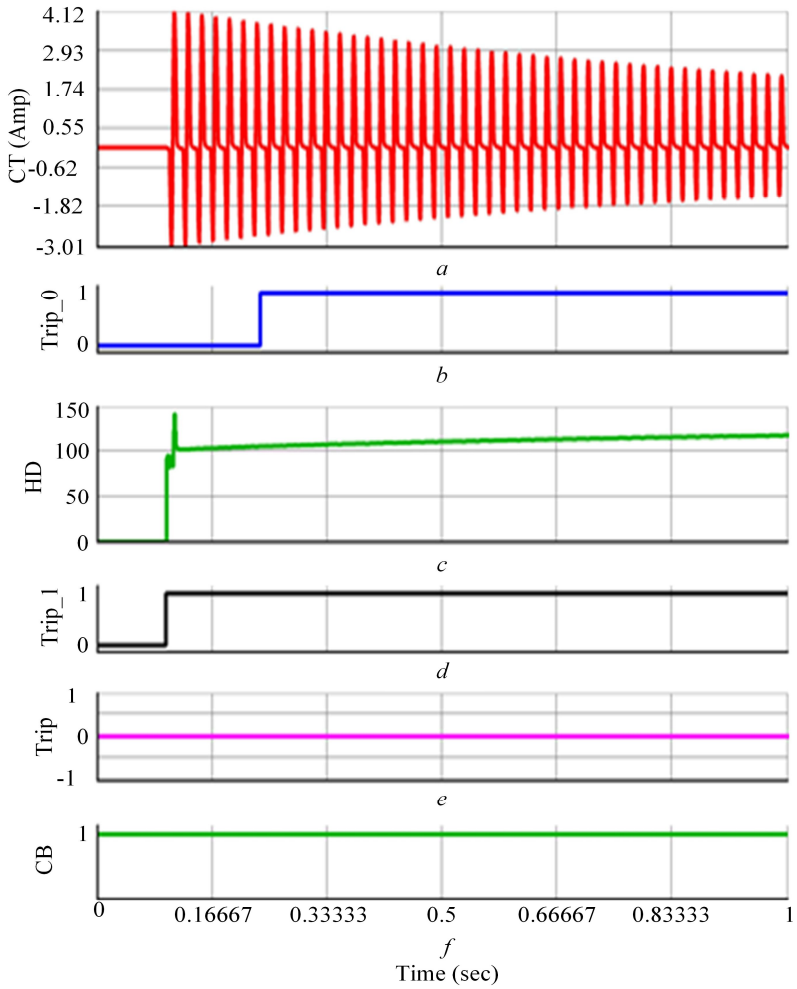

Figure 2.31 Test results under inrush effect (a) CT current under inrush condition (b) Trip signal generated by the FPGA (c) HD of the signal under inrush condition (d) Trip signal (HD > HDth) (e) Effective trip signal generated by the prototype (f) Status of the CB

If the status of the signal i.e. Trip_0=1 and Trip_1= 1 are satisfied, it indicates $I_{rms} > I_p$ occurs due to the presence inrush effect. Here, the mal-tripping of the prototype is prevented as the effective trip signal of the prototype remains zero shown in Figure 2.31*e* and Figure 2.31*f*.

2.7 Summary

In this chapter, FPGA implementation of overcurrent relay in presented. The developed prototype of the relay has been substantially verified for its characteristics and operational performance. The testing has been performed by placing the prototype relay through single wire hardware interface in the network model designed in real time digital simulator (RTDS®) environment in closed loop setup. The performance of the developed prototype has been found to be satisfactory. The design is entirely based on Verilog HDL and integer arithmetic which lowers computational overhead having low resource utilization and communication latency. The developed soft-core can be instantiated to produce multiple relays on the same or different chips. Now, this work is further extended for directional-OCR in the next chapter. Thereafter, the present design shall be enhanced by adding a communication and adaptation feature.

CHAPTER 3: FPGA BASED DESIGN AND HIL VERIFICATION OF DIRECTIONAL OVERCURRENT RELAY

3.1 Introduction:

Directional overcurrent relays (DOCRs) are the most economical and widely used component for protection of an electric power system. This chapter presents the design and development of a DOCR for field-programmable-gate-array (FPGA) implementation. A digital phase detection module has been developed for the estimation of the direction of current flowing through a power line of a power system network. In the proposed design, inverse characteristics viz. extreme inverse and very inverse characteristics of OCR have been considered for the computation of the relay tripping time. The integer arithmetic with Verilog hardware description language platform has been used to optimize the computational burden and the use of hardware resources. The design is implemented on the Xilinx Virtex Ml-505 FPGA development board. The performance of the DOCR is tested under various fault condition at different locations with different values of time dial settings and plug-point-multiplier. Hardware-in-loop, HIL verification of the relay prototype is carried out with the real-time-digital simulator (RTDS®). The results are compared with the standard DOCR of the RTDS which verify the successful operation of the designed relay under different fault conditions.

3.2 Directional Overcurrent Relay

The main feature of the DOCRs over the OCR is the direction based selectivity i.e. control logic computes the current flowing direction (forward or reverse) through the circuit breakers (CBs). A trip signal is generated when the short circuit fault current (I_F) exceeds from the threshold (I_{th}) current and a directional control signal is generated. Three types of inverse characteristics of the OCR have been suggested by IEEE standard C37.112-1996 [129]. Moderately inverse (MI), very inverse (VI) and extremely inverse (EI) is the preferred inverse characteristics used for the relay design. Relay-based on these characteristics operates by sensing the magnitude of the fault current i.e. higher the magnitude of fault current lesser will be the trip time. The functional block diagram of the DOCR shown in Figure 3.1, consists of three sub-modules viz. dc-offset with anti-aliasing filter (AAF) module, ADC module, and relay module. Zero crossing detector (ZCD) and phase detection (PD) module are internally designed

on the FPGA and works within the relay module. Time-current characteristics of the DOCR is explained in Section 2.2 of Chapter 2.

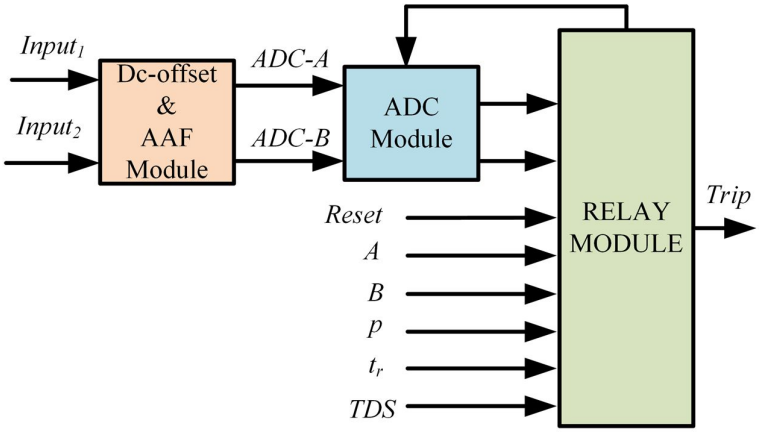

Figure 3.1 Block diagram for the RMS module

3.3 Design Flow of the DOCR

The detail discussion of functional modules of the designed DOCR i.e. ADC, MAF, RMS, ZCD, PD, REM and power system module (PSM) is carried out in the following subsections.

3.3.1 Analog to Digital Converter

A 2-channel 14-bit serial analog to digital converter (ADC) LTC1407A is used in the design. Programmable amplifier LTC6912-1 is associated with the ADC which increases the range of the ADC [141]. The details description of used ADC is given in Section 2.3.1 of Chapter 2.

3.3.2 DFT Filter and Root Mean Square Module

A discrete-time Fourier transform (DFT) filter has been used for the extraction of the fundamental component of the input signal as explained in Section 2.3.2 of Chapter 2.

3.3.3 Zero Crossing Detector Module

The phase angle of the signal has been determined using the zero crossing detector. The digital output of the ADC is input to the ZCD module. In this module, each sample received from the ADC is compared with a fixed value (7112) that is the digital equivalent of the dc-offset used in the design. If the digital value of the sample exceeds the predefined equivalent value of the offset, then output signals of ZCD (*ZCD_A* & *ZCD_B*) toggle to 1, else if the above condition does not satisfy then ZCD module produces 0 as shown in Figure 3.2. Thus, a square wave signal is generated by the ZCD module for every cycle of the input signal (current and

voltage). The phase detection module uses these square wave signals for the estimation of the phase angle between the input signals.

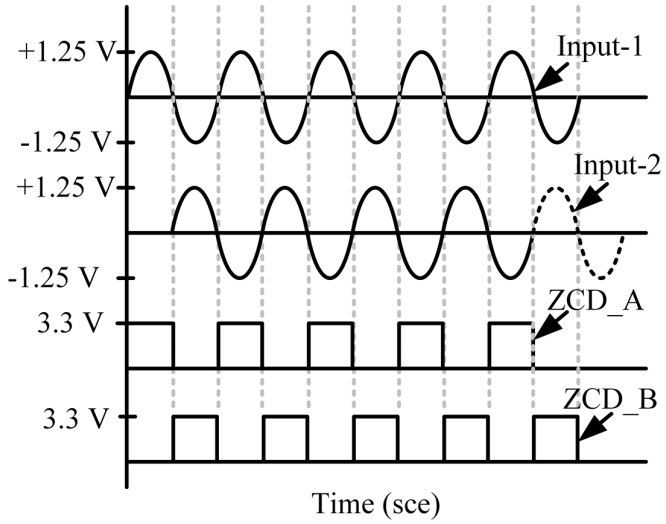

Figure 3.2 Waveforms of the ZCD module

3.3.4 Phase Detection Module

Figure 3.3 shows the state diagram of the conventional PD. *X (ZCD_A)* and *Y (ZCD_B)* are the input signals received from the ZCD module, Q_A and Q_B are the output signals of the PD. *State0, State1* and *State2* are the three states of the PD module. These states updated at every rising edge of the event signals (*X* and *Y*). The *state0* is the initial state of the PD where both the outputs (Q_A & Q_B) are 0. *State1* denotes the status of the output signal Q_A & Q_B as one and zero respectively. In state2, the magnitude of the output signals Q_A & Q_B are zero and one respectively.

Circuit diagram of the PD module has also been shown in Figure 3.4. Two D flip-flop and a logical-and gate are used in the module. Here, *X* and *Y* are the input pulses received from the ZCD module. The *Rst* is an intentional interrupt signal used in the design to reset the output. The phase angle computed by the stored output signals i.e. Q_A and Q_B.

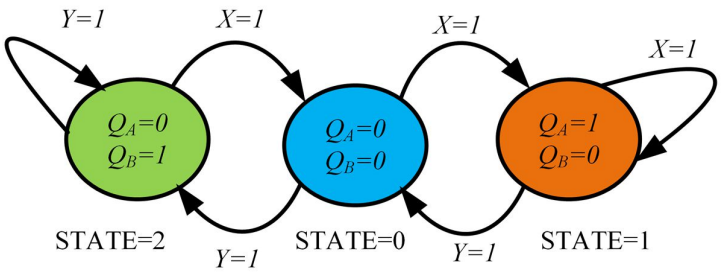

Figure 3.3 State diagram of the PD module

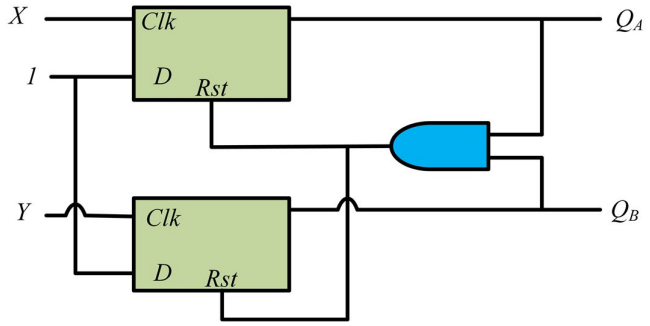

Figure 3.4 Circuit diagram of the PD module

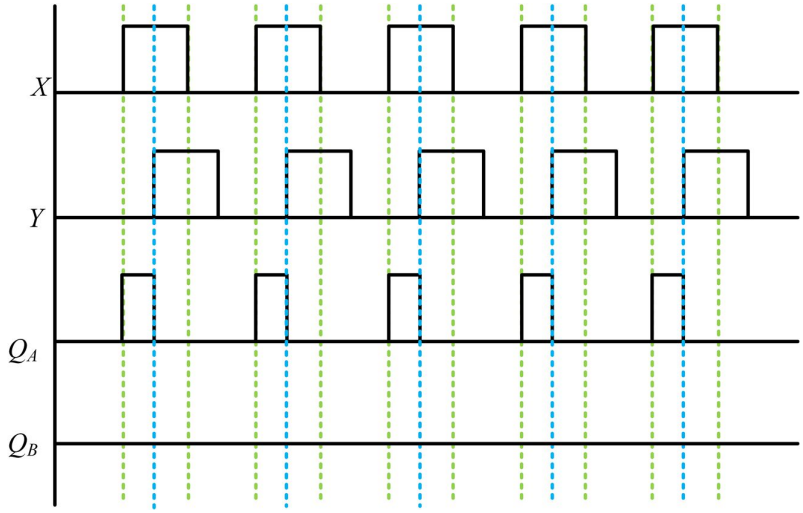

Figure 3.5 Output of PD module when *X* leads *Y*

Figure 3.5 shows the output waveforms (when input *X* leads *Y*) of the PD module. In this figure, waveforms *X* and *Y* are input signals coming from the ZCD module. Initially, both the output Q_A and Q_B are in *state0* with magnitude "0" or in active low state. Here, the present state changes from *state0* to *state1* after receiving the rising edge of the input signal *X* i.e. (*X=1*) and the output becomes Q_A=1 and Q_B=0. Thereafter, input '*Y*' becomes actives high i.e. (*Y=1*), state changes from *state1* to *state0* and output becomes Q_A=0 and Q_B=0. Thus, Q_A gives information about the leading phase of inputs '*X*' with respect to '*Y*'. The magnitude of the leading phase is computed by running an internal counter that is transferred to the REM.

3.3.5 Relay Emulating Module

Two functions get evaluated in the relay emulating module (REM). The 1st process is used to check the status of the *tick* signal generated by the OCR under normal or faulted condition while the 2nd process is accountable for the directional sensitivity of the DOCR. The

trip signal is generated by the logical ANDing of the directional control (of the PD module) and the *tick* signal. The trip time of the OCR is emulated with the help of the characteristics given by (2.1) and (2.2) of Section 2.3 of Chapter 2. Here, REM operates at the positive-edge of the 800 *Hz* input clock signal. The condition of $\sum Z_i$ is updated at every sample and compared with the N_T. "*UP* (Q_A)" is the output signal of the PD module which updates the status of the directional control signal. The status of the "*UP*" signal is updated when the phase difference between the inputs (*V* and *I*) is out of phase. At every clock edge of 800 Hz clock signal, the sum ($\sum Z_i$) is computed and compared with N_T. After that, the tick is updated which reflects the status and direction of the current flowing through CB. *The trip* signal is generated and sent to the CB when both the signals (*tick*, *UP*) are in the active high state.

3.3.6 Power system module

A simple test network for the verification of FPGA based DOCR prototype has been developed in RTDS [140] and shown in Figure A. 1 of the Appendix. The module consists of two ac sources, transmission line, CT, voltage transformer and CB. Different types of the fault have been introduced at a different location for operational verification. Performance of the developed prototype has been compared with a standard multi-functional OCR module available with RTDS. The phase voltage and currents are the inputs for the standard DOCR of RTDS. These signals are the outputs of the VT and CT respectively. Standard and manual settings are two operating modes of operation available on the DOCR. User can select the parameters of the operating mode as per their- requirement. Here, manual mode of operation is selected for the verification of the standard inverse characteristics of the DOCR. The values of parameters selected for the test module are given in Table A. 1 of the Appendix [138].

3.4 Implementation of the Proposed Design

Figure 3.6 shows the flow chart for the implementation of the design on FPGA using Verilog hardware description language (HDL). The implemented algorithm is initialized by setting parameters (*A*, *B*, P, *TDS*, T_r and N_T) of the relay characteristics curve equations. To reduce the computational complexity, the parameters of the implemented design are rounded to the next integer without affecting the accuracy of results. The multiplier of *A* is 4096, *B* is 64, *P* is 1 and T_r is 64 for both the inverse characteristics of DOCR. A large value of N_T=6.4×10^6 is considered to emulate the standard inverse characteristics of the OCR. After initialization of the constant parameter of the REM, ADC starts functioning and conversion of signals from analog to digital takes place. The ADC module converts the fundamental frequency cycle of 50 Hz input signal into packets of digital data of width 2 bytes. These packets are used by the DFT

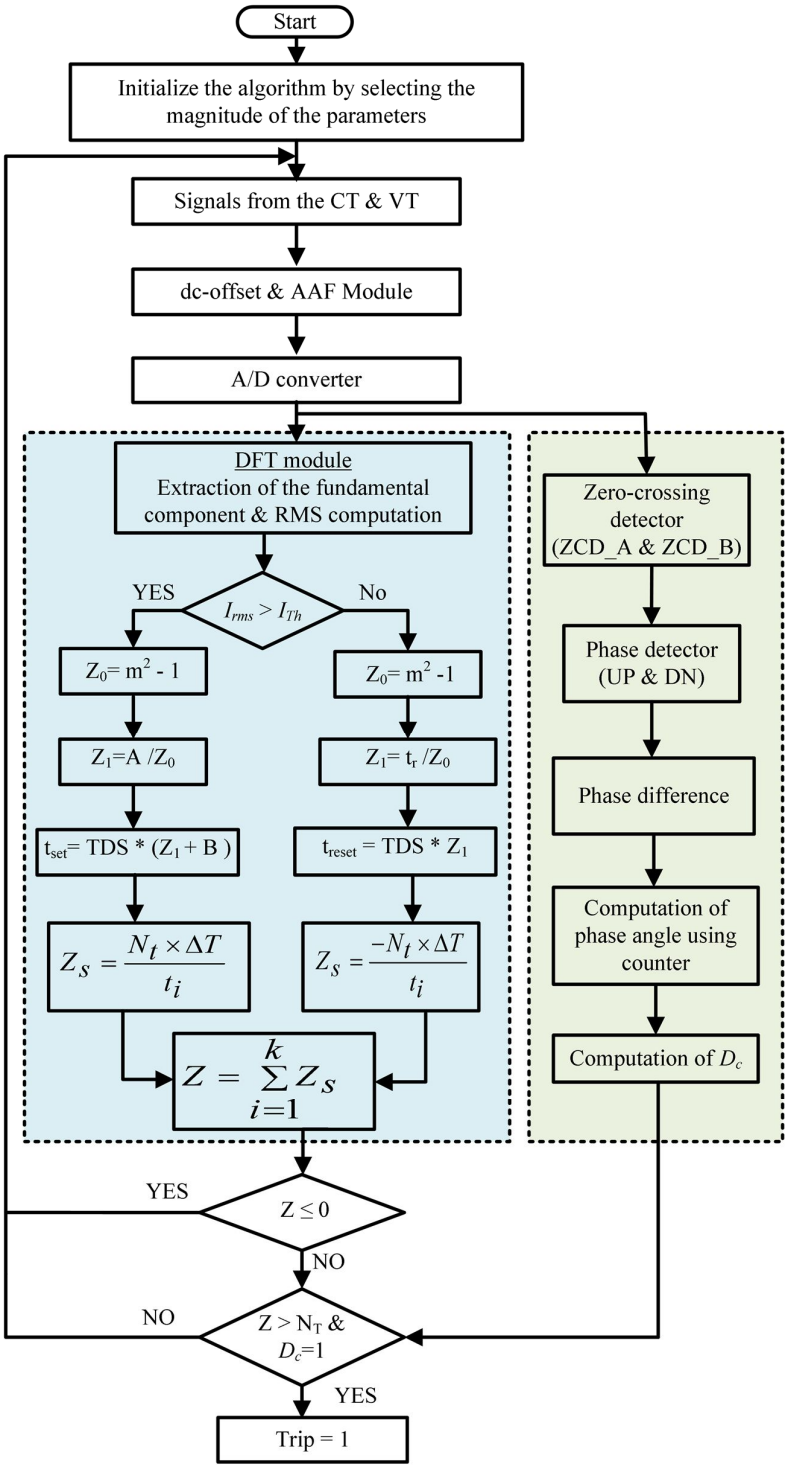

Figure 3.6 Flow chart of the DOCR

filter and the RMS module, which works at 800 Hz clock, the rms of the fundamental component is computed. The RMS value of the current and directional control signal received from the PD module are the inputs to the REM. In this module, the relay set and reset time of the OCR is evaluated. An accumulator is used in the REM to store the updated summation ($\sum Z_i$). If $I_{rms} > I_p$, the accumulator is increased by Z_i else if $I_{rms} < I_p$ it is decreased by Z_r. No

change in the value of accumulator if $\sum Z_i=0$ and $I_{rms} < I_p$. This condition is rectified to prevent the erroneous trip signal being generated. If it is in the active low state and $I_{rms} < I_p$, then the contribution to the accumulator is zero. The stored value of the accumulator is compared with N_T. Status of the trip signal is changed from zero to one when the present value of the accumulator is greater than N_T and directional control of the phase detection module is in the active state.

3.5 Results and Discussion

3.5.1 Characteristics Verification of DOCR

Virtex®-5 XC5VLX50T-1FFG1136 FPGA [137] is used as the target device for implementation of the DOCR. A *TRIP* signal with the directional control signal (*UP*) is generated on this dedicated hardware for the HIL verification. Register Transfer Logic (RTL)-Verilog coding technique has been used for the development of prototype design which includes 32 and 64-bit fixed point operations. Simulation, synthesis and mapping of the developed design have been carried on the Xilinx ISE® 12.4 platform. The verified design has been used for testing and real-time hardware verification of the DOCR. A clock module which operates at 100 MHz, is used to produce 40 kHz and 800 Hz clocks. 40 kHz clock is used by ADC, MAF, ZCD and PD whereas RMS and REM modules use the 800 Hz clock. Simulation and validation have been done for the evaluation of the relay operating time of the developed module as per the IEEE standard C37.112-96 for VI and EI characteristics. Table 3.1 summarises the percentage utilisation of hardware resources of FPGA (XC5VLX50T-1FFG1136). In this design, the limited number of hardware logic resources provided by Xilinx XC5VLX50T-1FFG1136 FPGA chip is used. Multiple relays or additional features can be

Table 3.1 Summary of FPGA Device Resource Utilization for DOCR

	XC5VLX50T-1FFG1136 device summary	Used	% Utilization
1	Number of Slice Registers	707	2
2	Number of Slice LUTs	6737	23
3	Number of occupied Slices	1861	25
4	Number of bonded IOBs	26	5
5	Number of BUFG/BUFGCTRLs	4	12
6	Number of DSP48Es	17	35

added to the proposed prototype due to the availability of the unused hardware resources. The simulation results are compared with the relay tripping time computed by equation 2.1 and 2.2 of chapter 2. Figure 3.7 and Figure 3.8 show that the absolute error of the relay tripping time in seconds between proposed and calculated values is insignificant. These simulations do not consider the dynamic behaviour of fault current. Therefore, RTDS has been used for the real-time testing of the designed relay under a different fault condition.

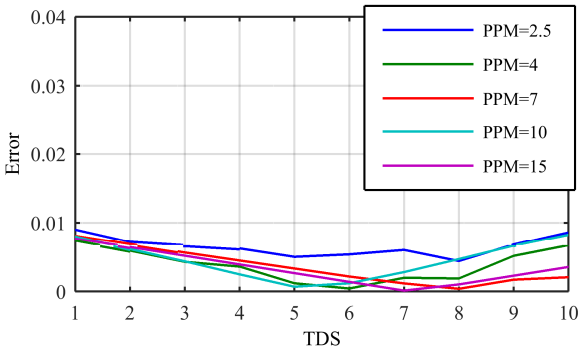

Figure 3.7 Error between emulated and IEEE Std. relay operating

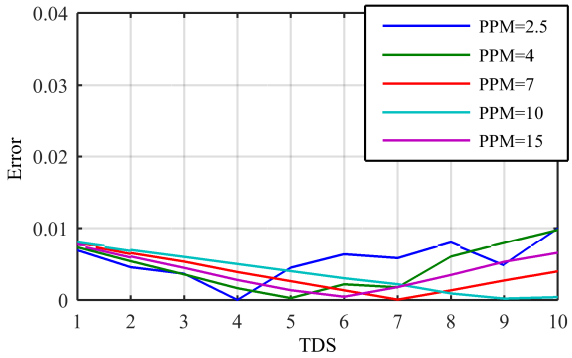

Figure 3.8 Error between emulated and IEEE Std. relay operating time

3.5.2 Hardware setup for HIL Testing

A test network has been developed and used for the HIL testing of the FPGA-based prototype of DOCR on RTDS® as shown in Table A. 1. Various components such as Gigabit Transceiver Analogue Output (GTAO) Card, Gigabit Transceiver Digital Input (GTDI) Card, Digital oscilloscope (DSO), DC offset module, Dual power supply, ADC module, JTAG cable, digital multi-meter, FPGA board and personal computer have been used as tools for the implementation. At the first level of implementation voltage and current signals of the test network are stepped-down using VT and CT respectively. Thereafter the current signal obtained

from CT is passed through the GTAO card which converts the current signal to voltage signal at an appropriate level as required by external devices. To validate the proposed DOCR, scaling factor of the current to voltage (C2V) converter of GTAO card is chosen as 36 for scaling down of the maximum fault current- to 1.2 V (P-P). The output signals from the GTAO card are input to the DC-offset module of the design. Then these signals are connected to 16-bit digital signal using the ADC module. After that these digital signal is input to REM having the designed FPGA prototype of DOCR, as discussed earlier. The trip is an output signal produced by the REM as per the operating conditions.

3.6 Results and Discussion for HIL Testing

In this section, various conditions are considered for the verification of the DOCR. Line-to-ground (LG) and line-to-line (LL) faults have been incepted at location-1 and location-2 for real-time testing of the prototype. Four channel digital storage oscilloscope (DSO)-1012A, 100 MHz, is used to store the control signals of the RTDS and FPGA development board. The result of the PD module and four test cases have been discussed for performance evaluation of the DOCR under the following subsections.

3.6.1 Testing of PD Module under Faults

In this case, the response of the PD module and its working has been discussed. *ZCD_A* and *ZCD_B* are the input signals to the module. Phase information is carried by the signal *Ph-diffn,* that is an internal signal of the PD module, whereas, *Directional-control* is the output of this module. Three different operating conditions have been considered and the signal recorded by DSO are shown in Figure 3.9, Figure 3.10 and Figure 3.11. The internal signal *Ph-diffn* is updated by the positive edge of the input signals whereas *Directional-control* is the output of the phase counter of PD which counts and compares the phase angle. Figure 3.9 shows the responses under the normal condition when the phase difference between the references are 270

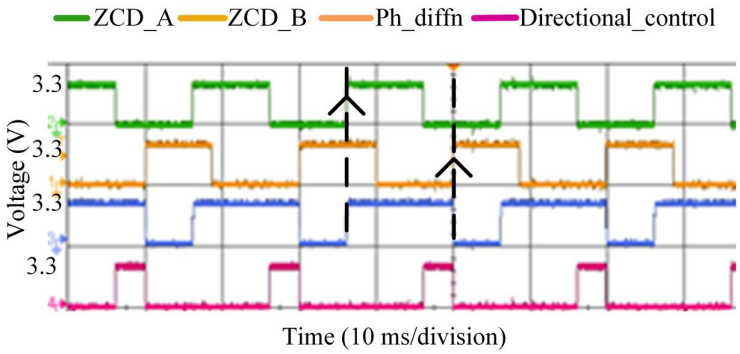

Figure 3.9 HIL testing of PD module under normal condition

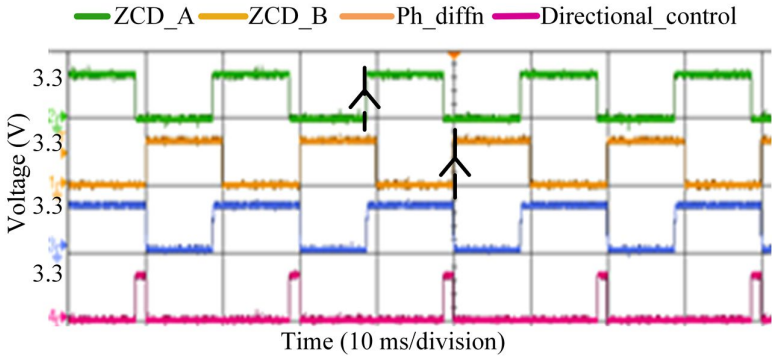

Figure 3.10 HIL testing of PD module when fault incepted at Location-1

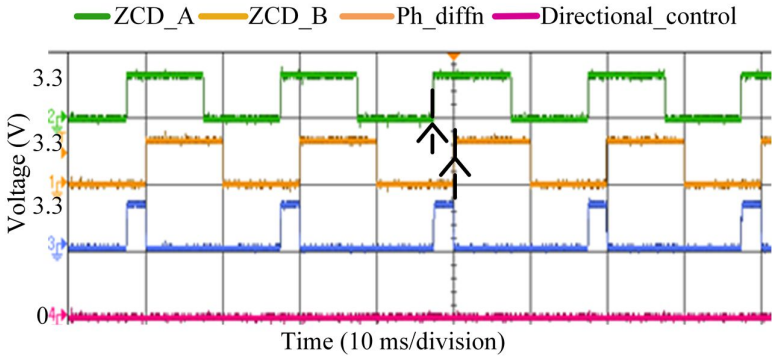

Figure 3.11 HIL testing of PD module when fault incepted at Location_2

degrees as shown by *Ph-diffn* signal. Then the *Ph-diffn* signal is compared with the threshold value of the phase angle (180°), and the result is updated by the *Directional-control*. Figure 3.10 shows the status of these signals when a fault has occurred at location-1. Here voltage and current signals are out-of-phase. Voltage and current are in-phase when the fault is incepted at location-2 as shown in Figure 3.11. In this case, the response of the PD module is in the active low state.

3.6.2 Operational Verification of Designed DOCR

Case: I *EI characteristics at TDS=1*

The developed DOCR for EI characteristics have been tested under the conditions; TDS=1 and I_{th}=1.17 kA. In this case, the fault is incepted at location-1 as shown in Figure A. 1 of the Appendix. Figure 3.12 shows the current signal of the current to voltage (C2V) converter which is received from the CT of the RTDS. The signals *Directional_control* and Trip_*FPGA* are also shown in Figure 3.12. *Directional_control* is the internal signal to the PD module which gives the phasor information between voltage and current signals. Signal *Trip_FPGA* is the output of the prototype (FPGA) and send back to the CB of the RTDS. In Figure 3.12*a*, the transition of the signals, before and after the occurrence of the fault is

highlighted. Whereas Figure 3.12*b* highlights the signal after generation of the trip signal. The status is also reported in Table 3.2. Various digital signals i.e *CB* (status of the circuit breaker), *FLT* (status of fault signal), *TRIP_RTDS* (trip signal generated by the DOCR of RTDS), *TRIP_FPGA* (trip signal generated by the FPGA-based DOCR) are shown in Figure 3.13. Here '0' stands for active low (OFF) whereas '1' represents an active high (ON) signal. These signals are captured in RTDS. When a fault is created, current changes abruptly and the current and voltage are out-of-phase. The maximum fault current I_F observed is 4.87 KA. In this case, the *FLT* signal is incepted at t=0.20sec and *trip* time, produced by the FPGA is 1.46 sec while RTDS is 1.45 sec.

Table 3.2 Status of signals when fault is occurred at location 1

SIGNALS	Status of the Signals		
	Normal condition	At the occurrence of *FLT*	At the occurrence of *TRIP*
FLT	0	1	1
Directional_control	1	1	1
TRIP(FPGA)	0	0	1

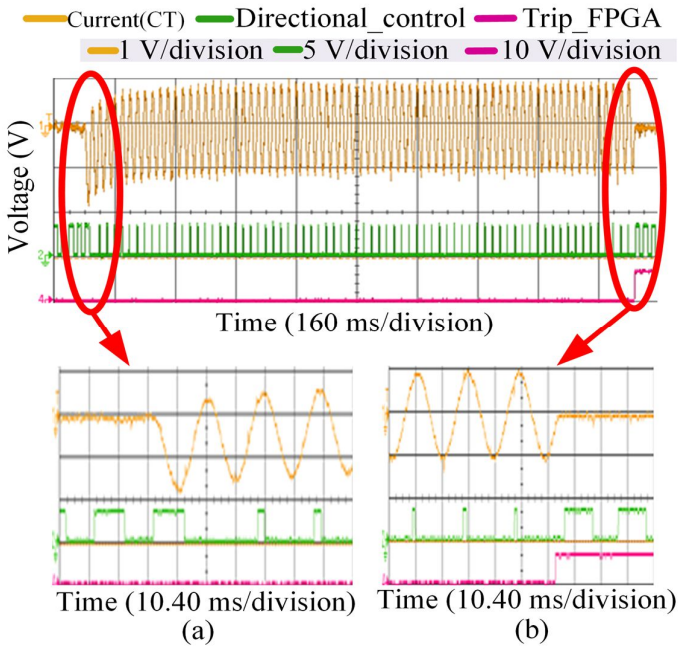

Figure 3.12 HIL result for EI characteristics when LG fault occurred at location1

Case: II *When fault incepted at location-2*

In this case, the fault is incepted at location-2 as shown in Figure A. 1 of Appendix and here the voltage is in-phase with the current. Results have been verified for EI characteristic with the settings; TDS=1 and I_{th}=1.67 kA. After the occurrence of fault, *Directional_control*=0

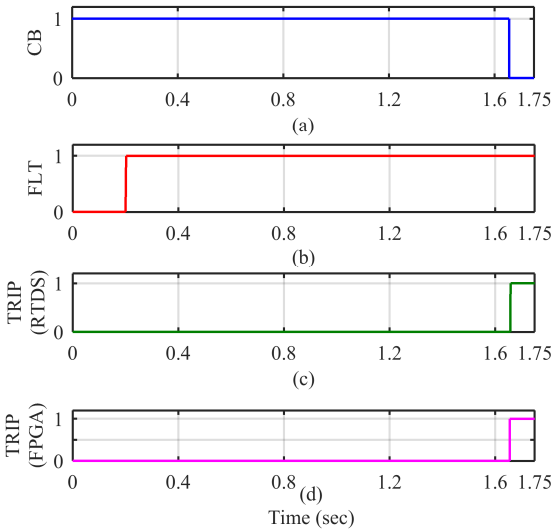

Figure 3.13 Status of control signal when LG fault occurred at location-1

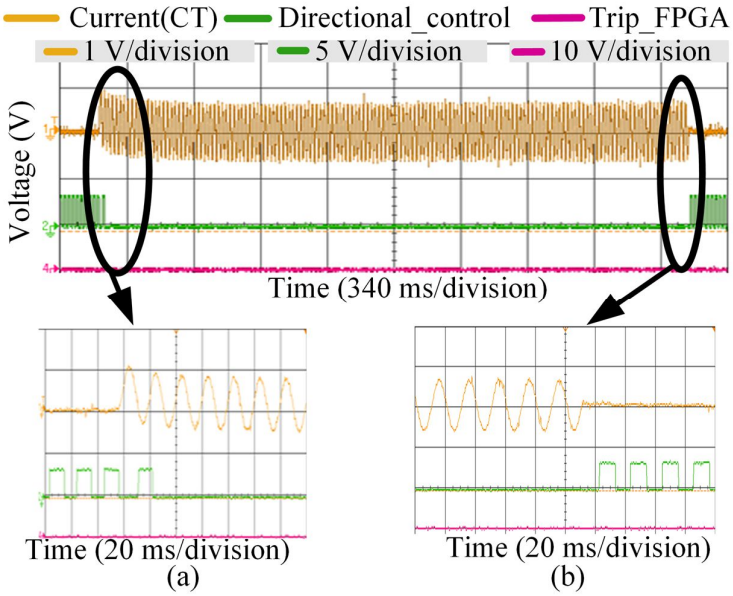

Figure 3.14 HIL result for EI characteristic when LG fault occurred at location 2

Table 3.3 Status of signals when fault is occurred at location 2

SIGNALS	Status of the Signals		
	Normal condition	At the occurrence of *FLT*	After the clearance of FLT
FLT	0	1	1
Directional-control	1	0	1
TRIP(FPGA)	0	0	0

shows that the voltage is in-phase with current as shown in Figure 3.14. In this condition, the maximum fault current observed is 1.67 KA. The status of the control signals observed in DSO and RTDS are shown in Figure 3.14 and Figure 3.15. Table 3.3 reports the status of control

signals as shown in Figure 3.14. In this case, FLT is incepted at t=0.40 sec. The status of the trip signal generated by the FPGA and the RTDS is low irrespective of the magnitude of fault current.

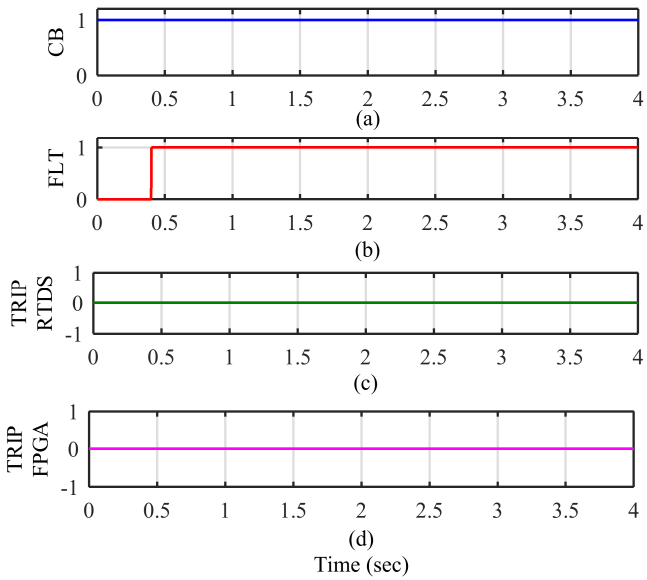

Figure 3.15 Status of control signal when LG fault occurred at location-2

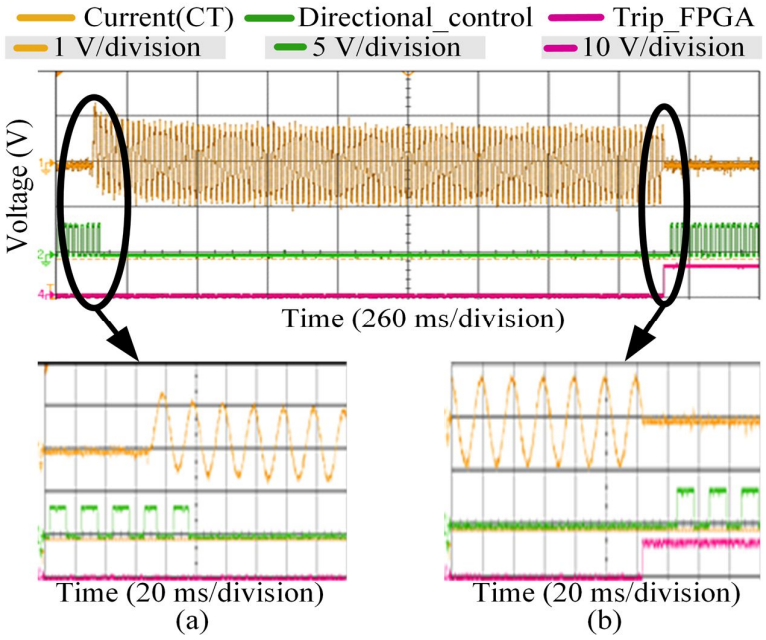

Figure 3.16 HIL result for EI characteristic when LL fault occurred at location 1

Case: III *When LL fault occurred at location-1*

In this case, LL fault is occurred at location-1 as shown in Figure A. 1 of the Appendix. The result has been verified for EI characteristic with the setting; TDS=1 and I_{th}=2.3kA. After the occurrence of fault, *Directional-control*=1 which shows that the voltage is out of phase with

current as shown in Figure 3.16. In this condition, the maximum fault current observed is 10.5 kA. The control signals observed in DSO and RTDS are shown in Figure 3.16 and Figure 3.17. *FLT* is introduced at t=0.51 seconds. Trip time taken by the designed FPGA-relay and the standard RTDS-relay is 2.18 sec and 2.19 sec respectively.

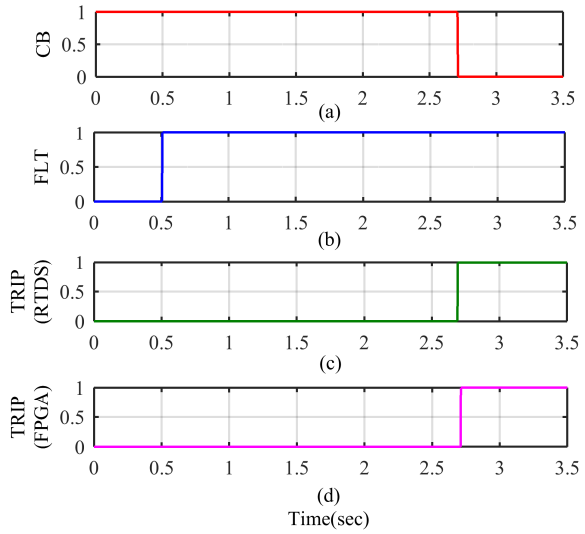

Figure 3.17 Status of control signal when LL fault occurred at location 1

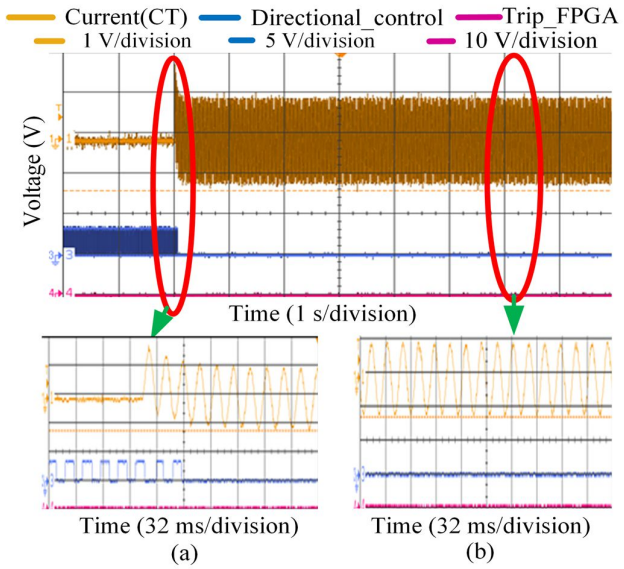

Figure 3.18 HIL result for EI characteristic when LL fault occurred at location 2

***Case: IV** When LL fault incepted at location-2*

In this case, LL fault is incepted at location-2 as shown in Figure A. 1 of the Appendix. The result has been verified for EI characteristic with the setting; TDS=1 and I_{th}=2.3 kA. After the occurrence of fault *Directional-control*=0, which shows that the voltage is in-phase with current as shown in Figure 3.18. In this condition, the maximum fault current observed is 10.6

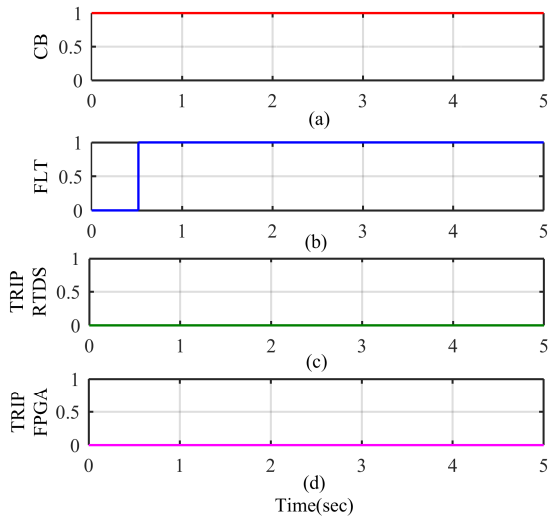

Figure 3.19 Status of control signal, when LL fault occurred at location 2

kA. Control signals observed in DSO and RTDS are shown in Figure 3.18 and Figure 3.19 respectively. *FLT* is incepted at t=0.53 seconds. The status of the *trip* signal generated by the FPGA and the RTDS is low irrespective of the magnitude of fault current.

DOCR has been tested for LG fault and discussed in *case-I* and *case-II*. In *case-I*, relay tripping time of the proposed DOCR is 1.46 sec while standard DOCR of RTDS is 1.45 sec. LL fault is considered in case-III and case-IV. In case-III, the tripping time of the proposed DOCR is 2.19 seconds while standard DOCR of RTDS is 2.18 seconds. The maximum percentage error observed in the above results is 0.69 %. The highlighted portion of Table 3.2 and Table 3.3 showed the ability of the directional sensitivity of DOCR and relay does not trip for the condition discussed in the *case-II* and the *case-IV*. It is also clear from the above results that the error observed is insignificant.

3.7 Summary

In this chapter, an HDL based modular design of DOCR has been developed and implemented on FPGA. The developed DOCR has been substantially verified for its operational performance and inverse characteristics by HIL approach using RTDS and FPGA platform. The design is entirely based on Verilog HDL using fixed-point integer arithmetic which lowers the computational burden and reduced hardware resource utilisation. The results suggest that the developed prototype is capable of distinguishing the direction of the fault current and act accordingly.

The proposed DOCR can be further used to develop a library of power system protection components. This developed module can also be used for relay coordination and protection of the bi-directional distribution networks such as microgrids. Also, the present design has been extended with communication and adaptation feature and shall be discussed in chapter 6.

CHAPTER 4: ISLANDING DETECTION TECHNIQUE BASED ON DISCRIMINATION FACTOR

4.1 Introduction:

After digital design of the protective relay, another objective of this thesis i.e. the protection of microgrid is has been addressed. Islanding detection is one of the most important issues for MG protection for safe, secure and uninterrupted power supply. It is the condition which occurs when the MG is disconnected from the main grid due to any contingency in the grid side. Generally, two types of islanding of the DGs occur i.e. intentional and unintentional. The intentional islanding is mainly performed for some maintenance works within the MG for the safety of the working personnel, while the unintentional islanding occurs due to the utility grid blackout by equipment failure, natural disaster or any abnormality in the power system. Unintentional islanding detection techniques are broadly classified as local and remote IDTs. Local IDTs are further categorized as active, passive, and hybrid techniques. In passive IDTs, local parameters of the target DGs terminal viz. frequency, voltage, current, and phase angle are monitored and compared with the predefined threshold values of the parameters. If the magnitude of the measured parameter is greater than the value of the predefined threshold, then islanding is detected by generating a trip signal to the CB located at the target DG terminal.

In this chapter, a novel passive IDT based on the islanding discrimination factor (IDF) using a periodic maxima of superimposed voltage components is presented. The voltage profile of the target distributed generator (DG) is monitored continuously and its sequence components are extracted using half angle theorem. A modular approach is used to implement the IDT algorithm, which is targeted on the reconfigurable hardware i.e. FPGA. Hardware description language (HDL) Verilog, has been used to optimize the hardware resources and minimize the computational complexity. Hardware-in-loop (HIL) verification of the IDT has been done for islanding and non-islanding events with a microgrid test system developed on Real Time Digital Simulator (RTDS®). Various test cases for both islanding and non-islanding events viz. different types of fault are tested on the standard microgrid test system. The results suggest that the proposed scheme successfully differentiates islanding events from a non-islanding event, and also detects the islanding event accurately even under perfect power balance condition within half cycle.

4.2 System Architecture of Designed IDT Module

Figure 4.1 depicts the outline of the IDT. The voltages from the target DG (DG-2) terminal is extracted from the RTDS through the voltage amplifiers and thereafter, processed by a sequence of pre-conditioning modules viz. DC-offset, an anti-aliasing filter (AAF) and analog to digital converter (ADC), before being fed into the targeted FPGA chip. Then, the ADC output is processed on the FPGA, where the superimposed components of the voltages are calculated, which are used to compute the positive component (ΔV_1) and the negative component (ΔV_2) of the superimposed voltage. Finally, voltage unbalance (*VU*) and islanding discrimination factor (IDF) are estimated by the IDF module which is compared with predefined thresholds i.e. $(IDF_{th})_{max}$ and $(IDF_{th})_{min}$. When the magnitude of the *IDF* falls within $(IDF_{th})_{max}$ and $(IDF_{th})_{min}$ then the islanding event is detected and a *TRIP* signal is generated and transferred to the circuit breaker *CB-2* of the DG-2 terminal of the RTDS.

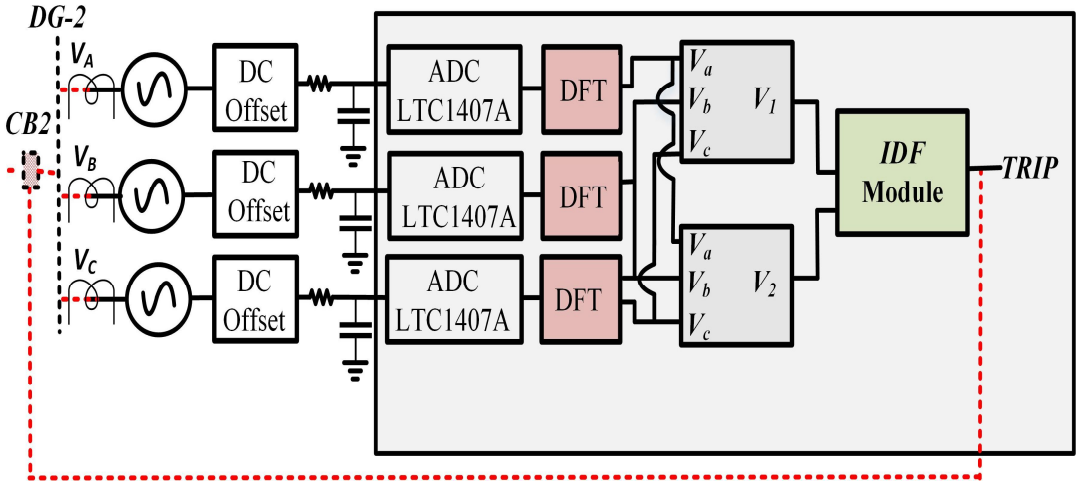

Figure 4.1 Overview and signal-flow of the proposed IDT

4.3 Digital Design of the Proposed IDT Algorithm

Digital design and implementation for the computation of the *IDF* to be used in the developed *IDT* algorithm developed on the reconfigurable hardware is presented in this section.

Node voltages of the *DG-2* terminal are taken as the inputs for the signal-conditioning modules i.e. DC-offset, LPF and ADC. After that, the digital output of the ADC is given as the inputs to the target FPGA development board (XC5VLX50T-3FF1136). Variations in bus voltages of *DG-2* can be considered as a notable parameter to indicate any inconsistency in the MGs i.e. network faults, islanding of the MG from the main grid and tripping of any large

generator or load. Hence, monitoring and estimation of the 3-phase voltage at the terminal of the *DG-2* enhance the effectiveness of islanding detection. This feature is aggregated into the proposed periodic maxima of superimposed voltage components based *IDT* by computing the *IDF*, which arises at the target DG i.e. *DG-2* terminal. The realized *IDF* module converts voltage magnitude to the superimposed components of voltages (ΔV_A, ΔV_B, and ΔV_C) given by equations(4.1), (4.2) and(4.3). These superimposed components are computed using sliding window techniques, in which data of the current window is updated by the data of the previous window [114].

$$\Delta V_A(n) = V_A(n) - V_A(n-N) \tag{4.1}$$

$$\Delta V_B(n) = V_B(n) - V_B(n-N) \tag{4.2}$$

$$\Delta V_C(n) = V_C(n) - V_C(n-N) \tag{4.3}$$

In the above equations V_A, V_B, and V_C are the node voltage of the DG-2 terminal whereas ΔV_A, ΔV_B, and ΔV_C are the superimposed component of the voltage at the same terminal. "N" is the number of samples in the fundamental cycle and "n" is the measuring instant. Thereafter, the sequence components viz. positive and negative of the superimposed voltage are computed by equations (4.4) and (4.5) using half-angle formula [142].

$$3\Delta V_1(n) = V_A(n) + P_b V_B(n) - Z_b V_B(n-1) - P_c V_c(n) + Z_c V_C(n-1) \tag{4.4}$$

$$3\Delta V_1(n) = V_A(n) - P_c V_B(n) + Z_c V_B(n-1) + P_b V_c(n) - Z_b V_C(n-1) \tag{4.5}$$

In the above equations, ΔV_1 and ΔV_2 are the positive, and negative sequence component of the 3-φ superimposed node voltage at the terminal of DG-2. In the above equations, 'n' is the 'n_{th}' number of sample and P_b, Z_b, P_c and Z_c are the constant parameters computed by equations (4.6), (4.7), (4.8) and (4.9).

$$P_b = \left[\tan(30^\circ + \beta) - \cos 30^\circ - \sin 30^\circ\right]^{-1} \tag{4.6}$$

$$Z_b = \left[\sin(30^\circ + \beta) - \cos(30^\circ + \beta)\tan 30^\circ\right]^{-1} \tag{4.7}$$

$$P_c = \left[\sin 30^\circ - \tan(30^\circ - \beta)\cos 30^\circ\right]^{-1} \tag{4.8}$$

$$Z_c = \left[\cos(30^\circ - \beta)\tan 30^\circ - \sin(30^\circ - \beta)\right]^{-1} \tag{4.9}$$

In the above equations, $\beta=[(2\pi F_n)/F_s]$. F_n and F_s are the frequency of the fundamental component and sampling frequency of the design respectively.

Thereafter voltage unbalance is computed using equations (4.4) and (4.5) which is defined as the ratio of the instantaneous negative sequence to the positive sequence of the voltage given by equation (4.10) [142], [60].

$$VU = \frac{\Delta V_2(n)}{\Delta V_1(n)} \times 100 \tag{4.10}$$

Finally, IDF is computed periodically by the equation (4.11) for every half cycle (N/2) using the moving window technique.

$$IDF = \max\left[VU_i\right]_{i=k-\frac{N}{2}\ to\ K} \tag{4.11}$$

In the above equation, '*i*' is the measurement instant and '*K*' is the total number of sample in the measurement window (*N*/2).

4.4 Working Principle and Design of IDT

Figure 4.2 gives the flow chart of the proposed IDT designed on the reconfigurable hardware using Verilog HDL. Fixed point integer arithmetic is used to emulate the IDT algorithm to decrease the computational burden and hardware resources. To initialize the algorithm, parameters of IDT i.e. P_b, Z_b, P_c and Z_c are fixed which depend on the sampling frequency and the frequency of the fundamental cycle. In design, the sampling frequency is 1.92 kHz that provides 32 samples in a power cycle (60 Hz). For this sampling frequency, the values of the parameters are "3.853", "4.439", "4.853" and "4.439" respectively. First, terminal voltages of the DG-2 are scaled down by the voltage transformer and taken out from the RTDS. Then, the output voltage is passed through the DC-offset module and AAF module. The filtered signal is passed to the ADC, where analog data is converted into 14-bit 2's complement digital data [143]. The sampled data is used for the computation of the superimposed components i.e. $\Delta V_A(n)$, $\Delta V_B(n)$, and $\Delta V_C(n)$ given in equations (4.1), (4.2) and(4.3). Now, these signal are processed by the modified Discrete Fourier transform (DFT), where the fundamental component is extracted and the decaying dc-component is eliminated which usually arises during the fault condition [144]. After that, the extracted signal is used for the computation of the $\Delta V_1(n)$, and $\Delta V_2(n)$. Now, the voltage unbalance i.e. ratio of the negative to the positive component is calculated. Subsequently, the 32-bit moving window algorithm is used for the computation of the maximum magnitude of samples within half cycle of the power signal (60 Hz). Finally, IDF given in the equation (4.8) is computed. Later, the magnitude of measured

IDF is compared with the predefined thresholds $(IDF_{th})_{max}$ and $(IDF_{th})_{min}$. And using the pre-defined threshold conditions, a *TRIP* signal is generated if the condition is satisfied and the status of CB2 in updated.

4.5 Test System

In this Section, a standard MG test system [145], modelled in RTDS® [140] has been used for the verification of the proposed technique for islanding detection. The considered MG test

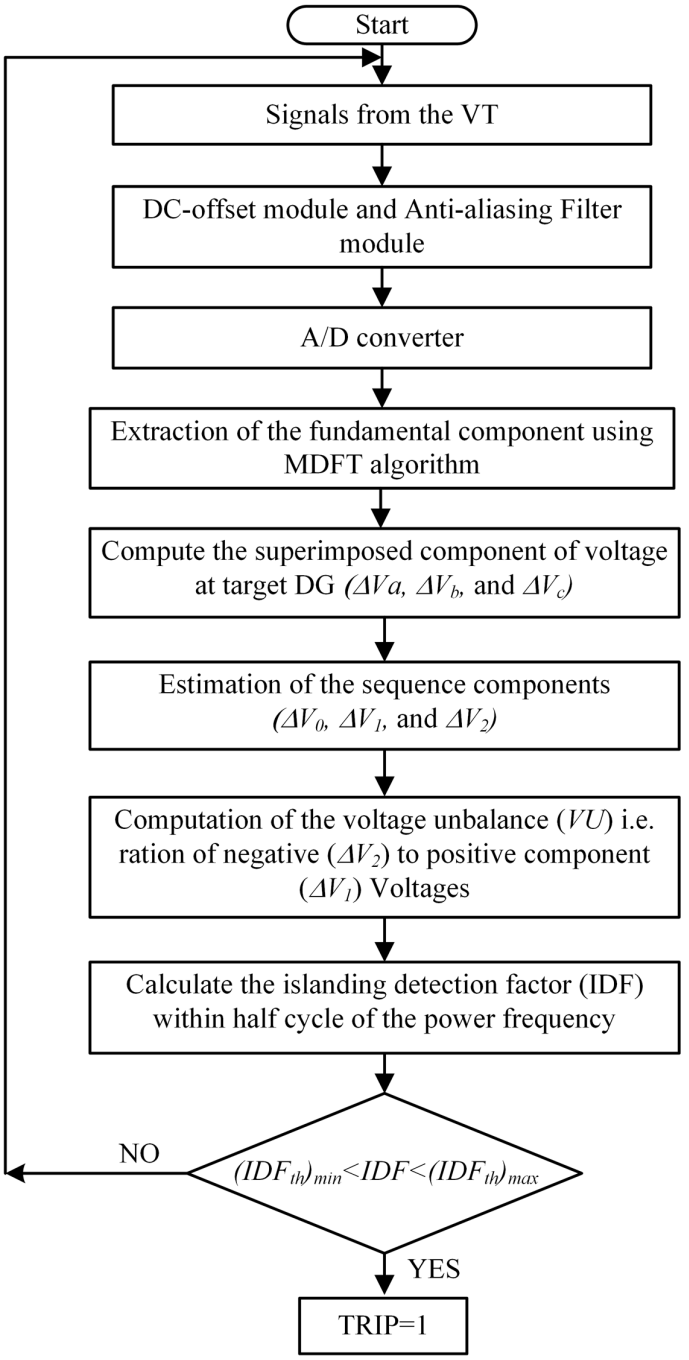

Figure 4.2 Flow-chart of the proposed islanding detection technique

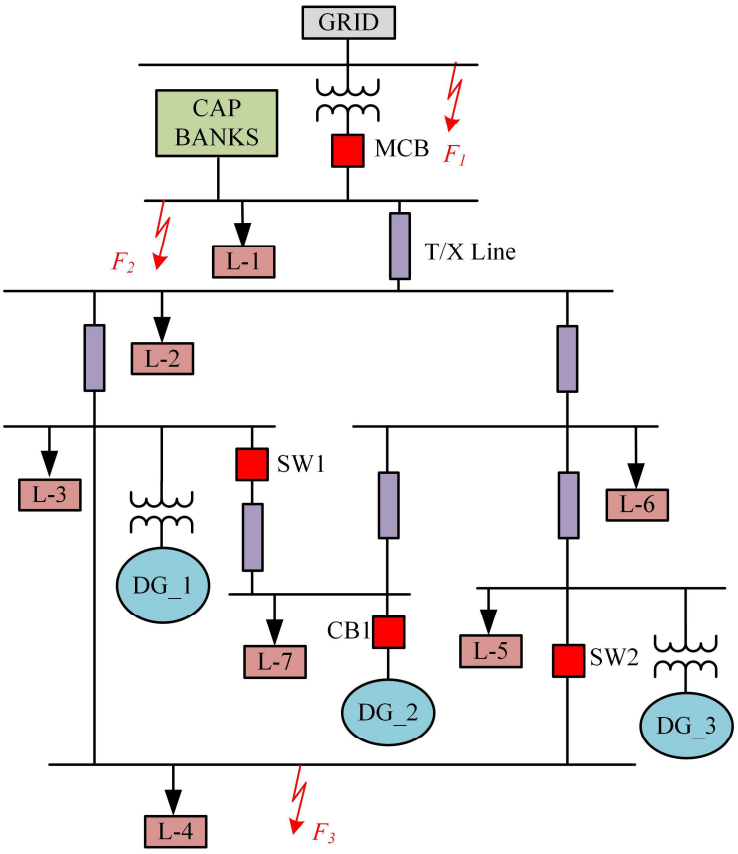

Figure 4.3 Microgrid test system modelled in RTDS

system is shown in Figure 4.3, which consists of a photovoltaic (PV) array (*DG-1*), a diesel generator (*DG-2*), a wind farm (*DG-3*), local loads (L_1, L_2, L_3, L_4, L_5, L_6 and L_7) and transmission lines. MG is connected to the main grid through the main circuit breaker (MCB). Parameters of the main grid, DGs, transmission line and loads are given in Table A. 2. The MG operates at frequency of 60 Hz and voltage of 13.2 kV. The operating modes of the MG is defined by the status of the MCB. When MCB is in active high state, MG works in grid-connected mode and for the active low state, it works in stand-alone mode. The microgrid forms a radial network if the switches SW_1 and SW_2 are open and when these switches are closed it operates as a mesh network. For the verification of the proposed algorithm under different operating conditions different types of faults at different locations (F_1, F_2, and F_3) and islanding of the MG is done when SW_1 and SW_2 are open.

4.6 Experimental Setup for HIL Verification

Hardware set-up for HIL-verification of the proposed IDT is depicted in Figure A. 2. The algorithm of IDT is targeted on Xilinx's virtex®5 development board i.e. XC5VLX50T-3FF1136 FPGA [137]. The MG test case system is modelled and simulated in the RTDS.

Analog output of the RTDS is taken through the Gigabit Transceiver Analogue Output (GTAO) Card whereas a digital input to the RTDS is given by Gigabit Transceiver Digital Input Card (GTDI). These cards are attached with the internal amplifier circuits, which establishes compatibility with the external peripheral devices. The gain of the voltage converter of the GTAO card is fixed at 23 to detect and bring down the voltage levels equivalent to the maximum input range of the ADC i.e. 2.5 V (P-P). Now, the bi-directional sinusoidal input signals are sensed using a dc-offset module which provides a magnitude of 1.65 V. Thereafter, the outputs of these offset modules are made to pass through the anti-aliasing filter to suppress any signals with higher order frequency components. The filtered signals from the offset modules are converted into digital signal by the ADC module and passed to the target FPGA chip. Finally, in FPGA the tripping condition evaluated using the designed algorithm. *TRIP* signal for the *CB2*, installed at the terminal of DG-2 is generated having a magnitude of $3.3V$ and fed into the RTDS through the GTDI card via a voltage amplifier.

4.7 IDF Threshold Settings

It is essential to fix the threshold value of the featured parameter for accurately differentiate between islanding from non-islanding events. Since, if the threshold value is set too low, it may result to false tripping of the target DG and if it is set too high, the islanding event may not be detected. The magnitude of *IDF* is computed by running the test cases under islanding and non-islanding events (different types of faults) for different power imbalance conditions like 0%, 25 % and (-)25% respectively as shown in Figure 4.4, Figure 4.5 and Figure 4.6. Then, the threshold values of *IDF* i.e. $(IDF_{th})_{max}$ and $(IDF_{th})_{min}$ are selected from the computed *IDF* values. During non-islanding events, huge change is observed in the maxima of superimposed

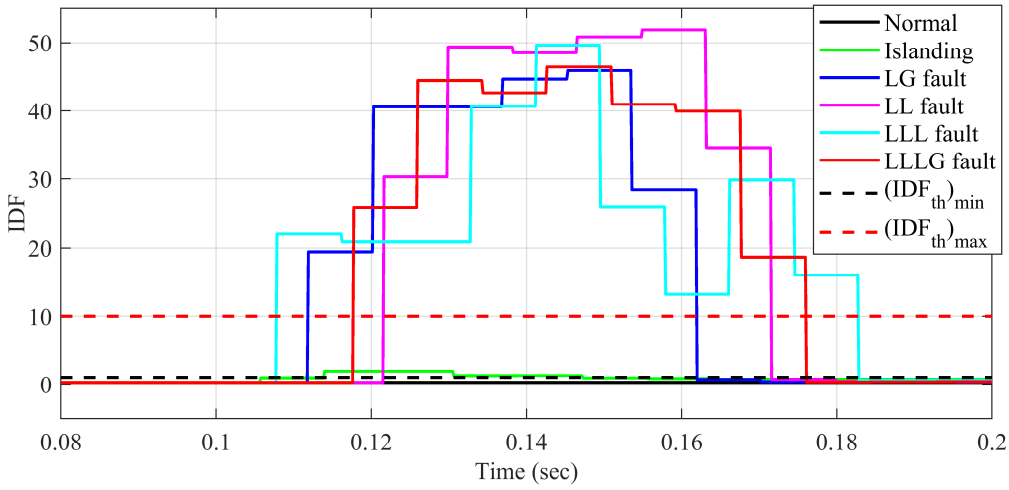

Figure 4.4 IDF magnitude for islanding & non- islanding events with power mismatch 0%

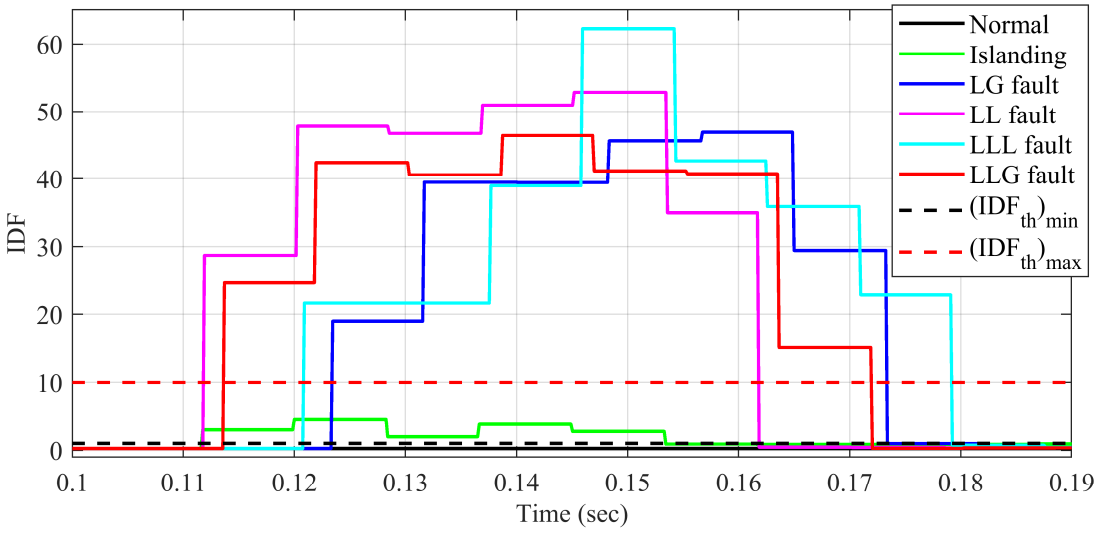

Figure 4.5 IDF magnitude for islanding & non-islanding events for 25% power mismatch

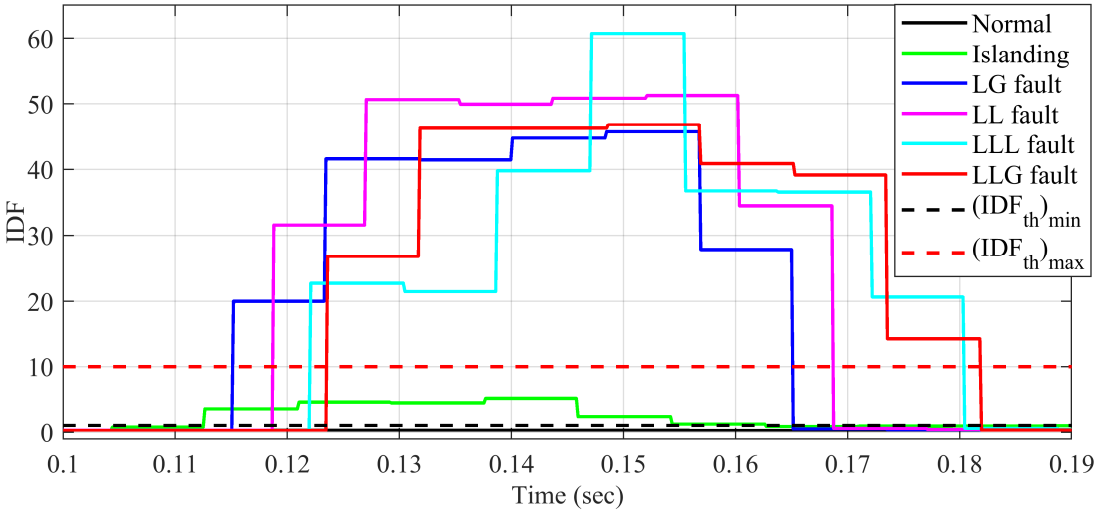

Figure 4.6 Values of IDF for islanding & non- islanding events for -25% power mismatch

voltage component i.e. *IDF* which is beyond the upper threshold level i.e. $(IDF_{th})_{max}$ whereas, in case of islanding event, variations in IDF are within the range between $(IDF_{th})_{min}$ and $(IDF_{th})_{max}$. In Figure 4.4 the magnitude of *IDF* is 0.26 in normal condition whereas its value increases to ~2, ~20, ~30, ~22, ~25 approximately in case of islanding, *LG* (line-ground) fault, *LL* (line-line) fault, LLL (line-line-line) fault, LLLG (line-line-line-ground) fault respectively when simulations are done for 0 % power imbalance. Similarly, the changes in the case of 25 % power mismatch are ~6, ~45, ~55, ~65, ~45 for islanding condition and different types of faults (*LG*, *LL*, *LLL*, and *LLLG*) respectively, depicted in Figure 4.5. Also, when the power unbalance between grid and MG is (-) 25 % (*-ve* sign indicate that the load is less as compared to MG generation), the magnitude of *IDF* for normal condition is 0.26, and the magnitude of *IDF* changes from its normal values to ~5, ~46, ~55, ~60, ~48 approximately for islanding and

non-islanding events (*LG*, *LL*, *LLL*, and *LLLG*) respectively, shown in Figure 4.6. Hence, from the above discussion, the threshold values of *IDF* i.e. $(IDF_{th})_{min}$ and $(IDF_{th})_{max}$ is chosen between the range of 1 and 10 respectively. And if the magnitude of *IDF* falls within these limits then the condition for islanding is satisfied, otherwise, it confirms non-islanding events. The lower limit of the *IDF* is selected as '1' to avoid false detection during normal condition. Therefore, for the selected range of *IDF*, the islanding condition is separated from the non-islanding events accurately even under zero percent power unbalance.

4.8 Results of HIL Verification

In this section, HIL verification of the developed *IDT* for various test cases of islanding and non-islanding events have been discussed. The islanding condition at *DG-2* is verified by opening the MCB at *PCC*, whereas non-islanding events are verified by incepting different types of the fault i.e. *LG, LL* and *LLLG* at different location i.e. F_1, F_2 and F_3, as shown in Figure 4.3.

4.8.1 Operation of IDT Algorithm under Islanding Event for Zero Power Imbalance

In this case, the performance of the proposed IDT is evaluated when the power transfer between the main grid and the microgrid is zero. To study this condition, the magnitude of the loads L_1, L_2, L_3, L_4, L_5, L_6 and L_7 are 0.8 MW, 0.5 MW, 0.5 MW, 0.5 MW, 0.5 MW, 0.5 MW and 3 MW respectively. For these loads, the amount of output power of the main grid, *DG-1*, *DG-2*, and *DG-3* is 0 MW, 1.7 MW, 3 MW and 2.0 MW respectively. To verify the islanding condition, the status of MCB is set to "0" which implies it is in open condition, while performance for non-islanding events is verified by applying different types of fault. Results are discussed in the following sub-sections.

4.8.1.1 Performance verification for islanding condition

In this section, the operation of the proposed technique is verified by opening the MCB at PCC and monitoring the magnitude of node voltage of the target DG i.e. *DG-2*. The signals observed in RTDS is shown in Figure 4.7, while inputs of the signal conditioning module and output of the FPGA chip is shown in Figure 4.8. Figure 4.7*a* shows the magnitude of the terminal voltage of the *DG-2*. Figure 4.7*b* represents the magnitude of the *IDF* in blue coloured signal while its set thresholds $(IDF_{th})_{Max}$ and $(IDF_{th})_{Min}$ are represented in red and pink coloured signal respectively. Signals MCB and *CB2* represent the status of MCB and the CB located at the terminal of the target *DG-2* as shown in Figure 4.7*c* and Figure 4.7*d* respectively. V_A is the phase-A voltage of the *DG-2*, which is output from RTDS and fed into the DC-offset module

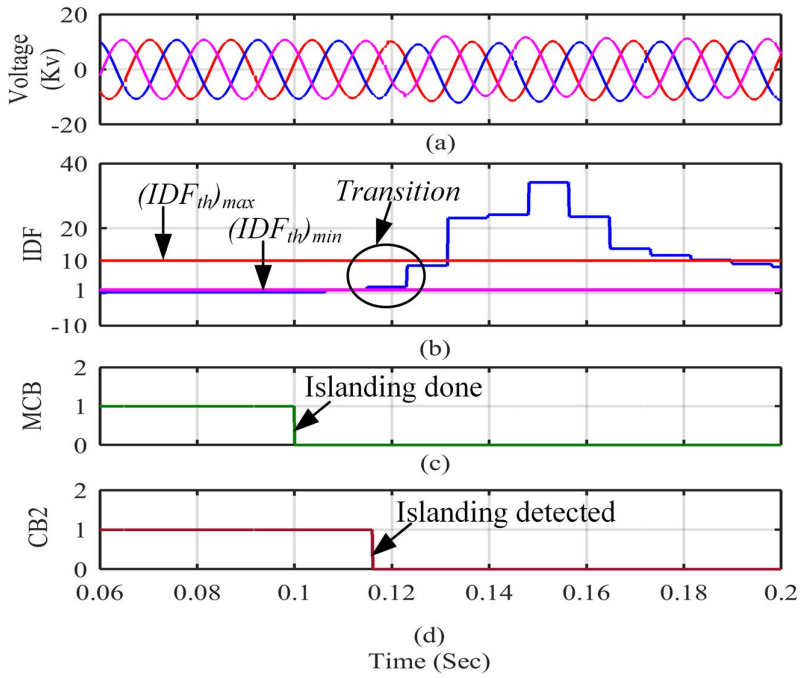

Figure 4.7 Test results for 0% mismatch condition monitored in RTDS

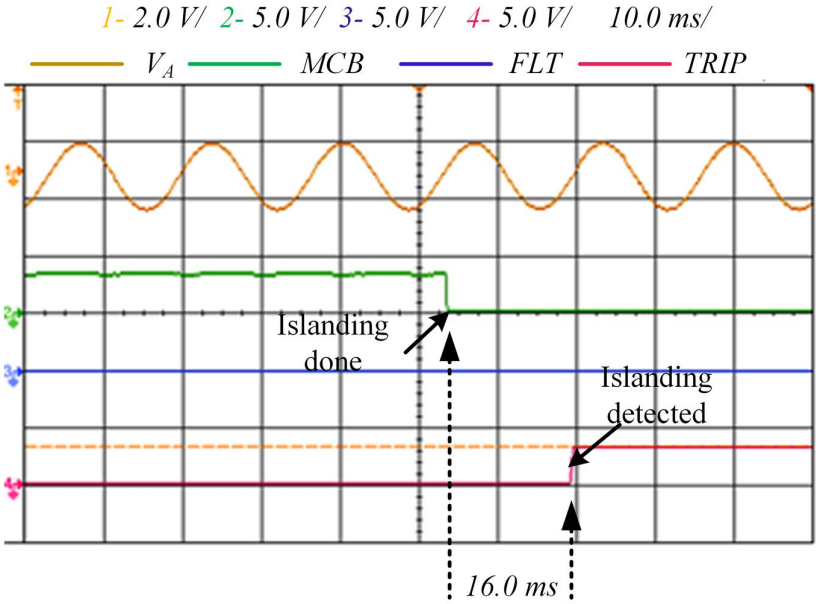

Figure 4.8 Test results for 0% mismatch condition monitored in DSO

shown in yellow colour in Figure 4.8. Here, signals *FLT* and *TRIP* are the output of the RTDS and FPGA in blue and pink colour respectively. Islanding is done at t= 0.099 sec shown in Figure 4.7*c*. After the occurrence of islanding event, the changes in the *IDF* is observed and shown in Figure 4.8*b* in blue coloure. The transition of the *IDF* is within the range of thresholds i.e. between red and pink coloured signals with magnitude 1.8 (blue signal), which ascertains an islanding event. Now, in FPGA the islanding is detected at t= 0.116 sec and a *TRIP* signal (pink coloured in Figure 4.8*b*) is generated and fed to RTDS to open the CB2. To measure the

detection time the reference signal of islanding event (at 0.099 sec) is also inserted into the DSO as shown in the green coloured signal. Hence, the difference between islanding detection and islanding event i.e. detection time is ~16 ms.

4.8.1.2 Performance verification for non-islanding event

In this section, the performance of the proposed *IDT* is verified for critical non-islanding event i.e. fault inception. The magnitude of the terminal voltage of *DG-2*, *IDF*, *CB2*, V_A, MCB, *FLT* and *TRIP* are depicted in Figure 4.9 and Figure 4.10. Figure 4.9*c* represents the duration of the incepted fault. In this case, the duration of fault is kept for half power cycle (~8 ms).

An LG fault (F_1) shown in Figure 4.3 is incepted between phase-*A* to ground at t = 0.1005 sec whose effect starts from t=0.1094 sec (next zero crossing). After this instant, the fluctuations in *DG-2* terminal voltage has been observed as shown in Figure 4.9*a*. Figure 4.9*b* represents the variations of the *IDF* in pink coloured signal. Here, no transitions occurred between the predefined threshold regions which are shown in blue and red coloured signal as the magnitude of *IDF* varies from 0.098 to 19.51 (encircled) in Figure 4.9*d* which confirms the non-islanding events. In Figure 4.10, the blue signal shows the fault incepted and the pink coloured signal shows the status of the *TRIP* signal generated by the FPGA, which remains in active low stage confirming the non-islanding event.

4.8.2 Performance Verification of Prototype under 25% Power Imbalance

Here, the operation of the *IDT* has been verified for 25% power mismatch i.e. power transfer between the main grid and the microgrid is 25%. For this purpose, the magnitude of the loads

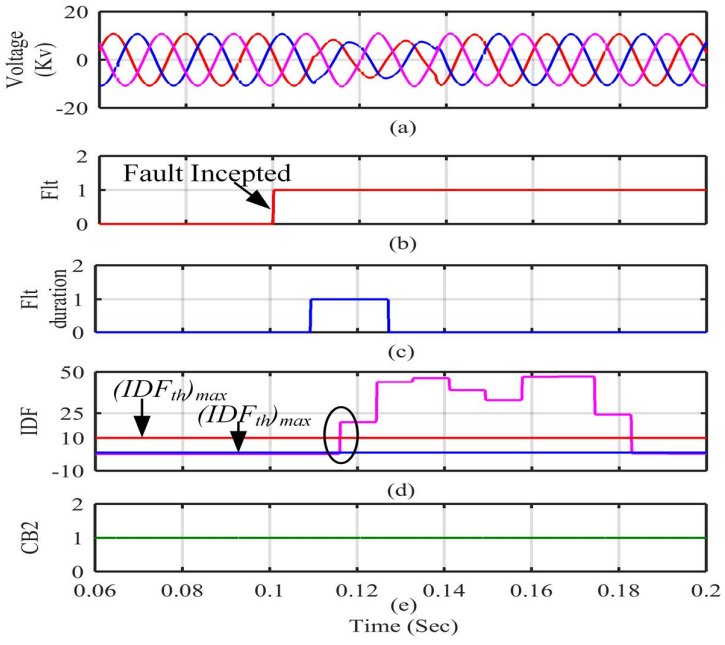

Figure 4.9 Test results monitored in RTDS when mismatch is 25%

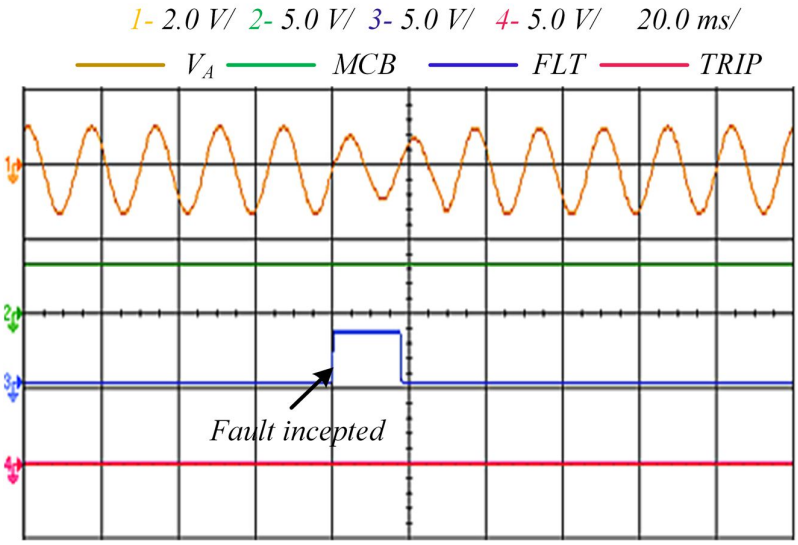

Figure 4.10 Test results monitored in DSO, when mismatch is 25%

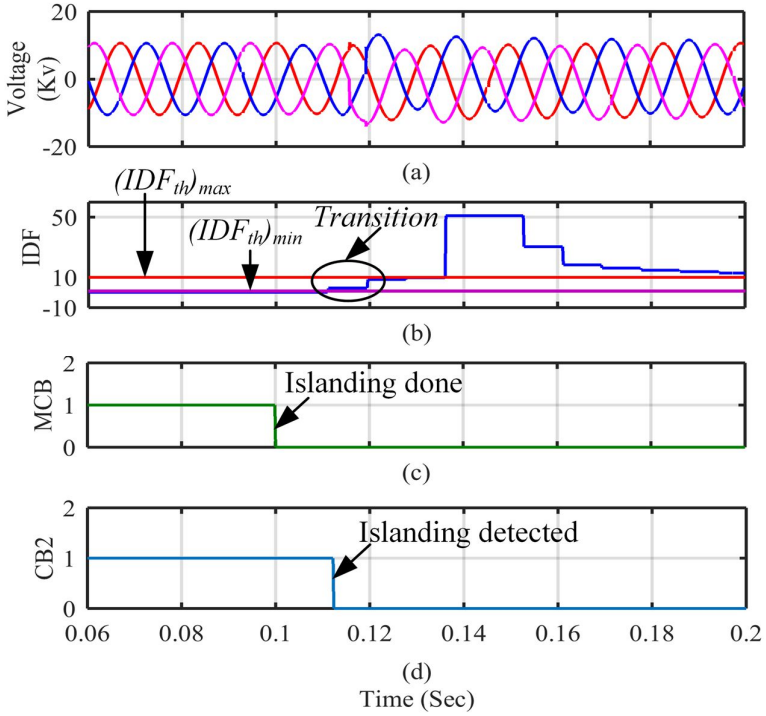

Figure 4.11 Performance Verification of islanding condition when mismatch is 25%

L_1, L_2, L_3, L_4, L_5, L_6 and L_7 are considered as 0.8 MW, 0.5 MW, 0.5 MW, 0.5 MW, 0.5 MW, 0.5 MW and 5.12 MW respectively. For this load, the respective magnitude of output power of the main grid, *DG-1*, *DG-2*, and *DG-3* is 2.06 MW, 1.7 MW, 3 MW and 2 MW.

4.8.2.1 Performance verification for islanding condition

Here, the impact of the islanding event with 25% power imbalance between the main grid and the microgrid is discussed for the *IDT* algorithm. The magnitude of the voltage, *IDF*, MCB and *CB2* are monitored in RTDS and are shown in Figure 4.11. In Figure 4.12, V_A, MCB, *FLT*

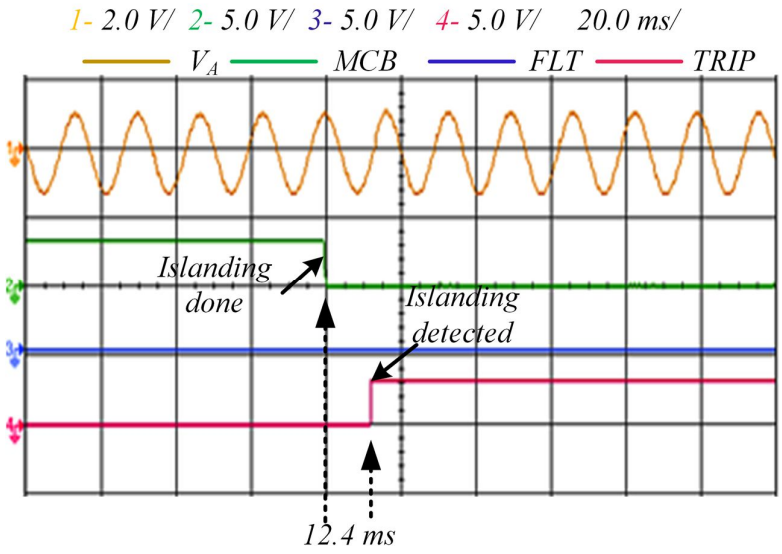

Figure 4.12 Signal monitored in DSO for performance verification when mismatch is 25%

and *TRIP* is the signal measured by DSO. Now, the islanding is done at t=0.099 sec by opening the MCB, shown in Figure 4.11*c*. After changing MCB status, variations in the *IDF* is observed as shown in Figure 4.11*b* in blue coloured signal. The transition of the *IDF* is within the boundaries of thresholds i.e. $(IDF_{th})_{Max}$ and $(IDF_{th})_{Min}$, from 0.25 to 2.97. Under these conditions, islanding is detected at t=0.1122 sec and at this instant *CB2* opens as shown in Figure 4.11*d*. Hence, the total detection time is ~12.4 ms. Also, the *TRIP* signal generated by the FPGA is shown in Figure 4.12 in green coloured signal.

For further performance evaluation of the presented technique has been verified for the islanding event under different active power imbalance conditions. The obtained results are summarized in Table 4.1. Maximum detection time of islanding observed is ~14 ms which is less than that of the suggested technique (~22.5 ms) of [108], [114]. Similarly, the performance of the proposed *IDT* has also been tested for critical non-islanding events i.e. impact of different types of fault. A set of different cases of *LG* fault, *LL* fault, *LLLG* fault with different fault resistance and different fault inception angle have been considered. These faults were triggered

Table 4.1 Testing of the designed prototype under different power mismatch conditions

Power mismatch (%)	*Islanding done*	*Islanding detected*	*Detection time*
0	at, t=0.100 sec	at, t=0.111 sec	11 msec
25	at, t=0.100 sec	at, t=0.114 sec	14 msec
50	at, t=0.100 sec	at, t=0.110 sec	10 msec
75	at, t=0.100 sec	at, t=0.111 sec	11 msec
100	at, t=0.100 sec	at, t=0.110 sec	10 msec

Table 4.2 Testing of the designed prototype under different power mismatch conditions

Power mismatch	*Events*	*Events incepted (at* t=0.100 sec *)*	*Islanding detected*	*Detection time*
0%	*LG, LL,* LLL, and LLG fault	F_1	Non-islanding events	Not applicable
		F_2		
		F_3		
25%	*LG, LL,* LLL, and LLG fault	F_1	Non-islanding events	Not applicable
		F_2		
		F_3		
50%	*LG, LL,* LLL, and LLG fault	F_1	Non-islanding events	Not applicable
		F_2		
		F_3		
75%	*LG, LL,* LLL, and LLG fault	F_1	Non-islanding events	Not applicable
		F_2		
		F_3		

externally at Location F_1, F_2 and F_3 as shown in Figure 4.3. The results are reported in Table 4.2. Here, the proposed *IDT* method successfully identifies the non-islanding even and doesn't generate *TRIP* signal for DG-2.

4.8.3 Performance Verification under other Non-Islanding Scenario

In this section, performance of the proposed IDT is tested under the sudden change in load, switching of inductive or capacitive load and sustained voltage sag/swell condition.

4.8.3.1 Sudden change in load:

The performance of the proposed IDT during the sudden change in load is studied by increasing the load (10% to 50% from their reference magnitude) at the target DG when MG is operating under 25% power mismatch condition. Figure 4.13*A* shows the waveform of the IDF for the sudden increase in the load (10%, 20%, 30%, and 40%) and Figure 4.13*B* shows the waveform of the control signal when 50% change in load is introduced. From Figure 4.13*A*, it is clear that the magnitudes of the IDF are beyond the threshold values of IDF (IDF_{min}=1 & IDF_{max}=10). In fact, it remains well below the lower limit of the threshold value i.e. IDF_{min}=1. Also, in Figure 4.13*B* the magnitude of the IDF does not fall between its threshold values of the IDF nor does any transition in the IDF occurs within the threshold band. Therefore, the proposed algorithm works satisfactorily in the case of sudden change in load condition and does not initiate the *TRIP* signal.

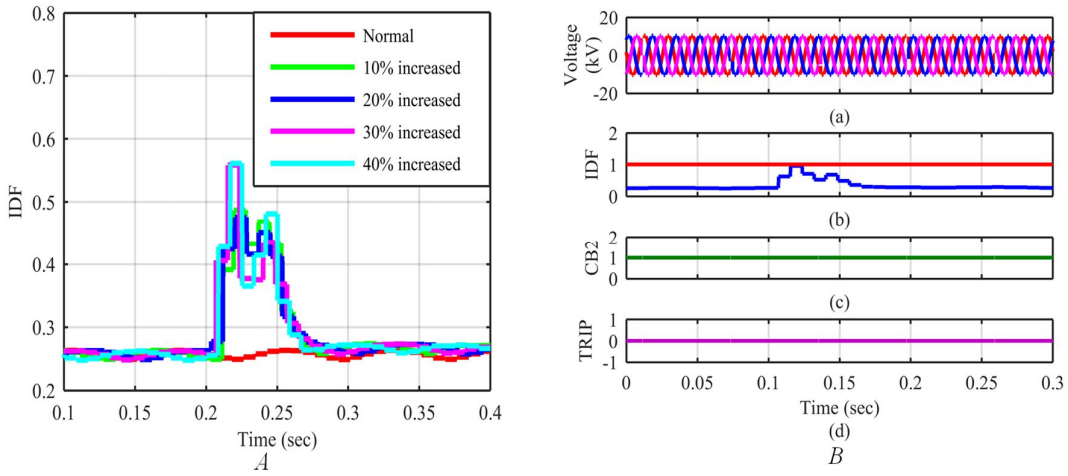

Figure 4.13 Variation of load at target DG (a) Magnitude of IDF (b) Under 25% power mismatch for 50%

4.8.3.2 Sudden change in Inductive or capacitive load:

In this case, the performance of the proposed IDT is tested when sudden change in inductive and capacitive load at the target DG is applied by varying these loads by 10% to 50%. Figure 4.14 and Figure 4.15 represent the waveforms of the IDF, status of the *CB2* (Circuit breaker located at the target DG terminal) and signal '*TRIP*' generated by the algorithm for change in inductive and capacitive loads respectively. For both the cases (inductive and capacitive load increases from 10% to 40%), the magnitudes of the IDF are below the lower limit of the threshold value i.e. (IDF_{th}=1) as shown in Figure 4.14*A* and Figure 4.15*A*. Figure 4.14*B* and Figure 4.15*B* show the waveform when loads are increased 50%, here also, for both the cases the magnitude of the IDF is not crossed beyond the lower threshold limit of the IDF_{th} (IDF_{th}=1). Therefore it does not generate the *TRIP* signal as shown in Figure 4.14*B*(d) and Figure 4.15*B*(d). Hence, the proposed IDT remains stable during sudden change in inductive and capacitive load.

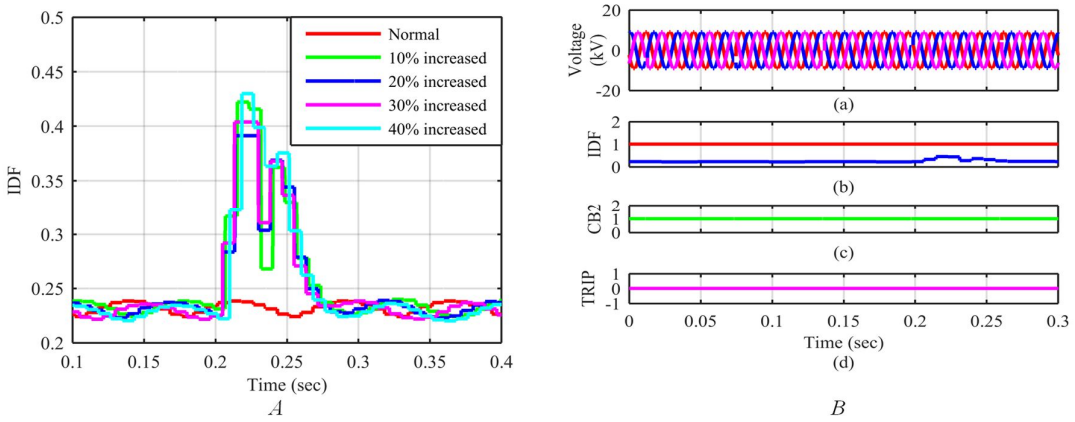

Figure 4.14 Variation in inductive load at target DG (a) Magnitude of IDF (b) For 50% change in inductive

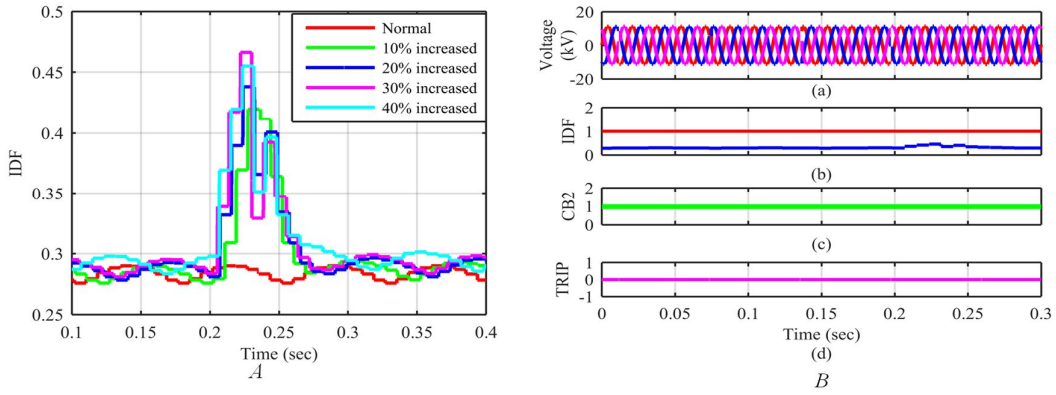

Figure 4.15 Variation of capacitive load at target DG (a) Magnitude of IDF (b) response for 50% variation in capacitive load

4.8.3.3 Sustained voltage Sag/Swell:

The performance of the proposed IDT is tested under the condition of voltage sag and swell. Figure 4.16*A* and Figure 4.16*B* represent the waveforms of the voltage at the target terminal, IDF, status of the *CB2* and status of the *TRIP* signal for voltage sag and swell respectively. ~20% voltage drop is introduced by varying the load at the target DG terminal shown in Figure 4.16 (a). The transition in IDF magnitude does not fall within the threshold of the IDF i.e. IDF_{min}=1 & IDF_{max}=10, shown in Figure 4.16*A*(b), due to which *TRIP* signal is not generated that confirm the case of the non-islanding event. Similarly, to verify the performance under voltage swell condition, ~20% voltage is increased from its nominal voltage as shown in Figure 4.16*B*(a). Here also, the transition in IDF magnitude does not fall within the threshold value of the IDF, shown in Figure 4.16*B*(b). This confirm the non-islanding event since the status of the *TRIP* signal is not changed. From the above discussion, it is clear that the proposed IDT algorithm works satisfactorily under sustained voltage sag and swell condition.

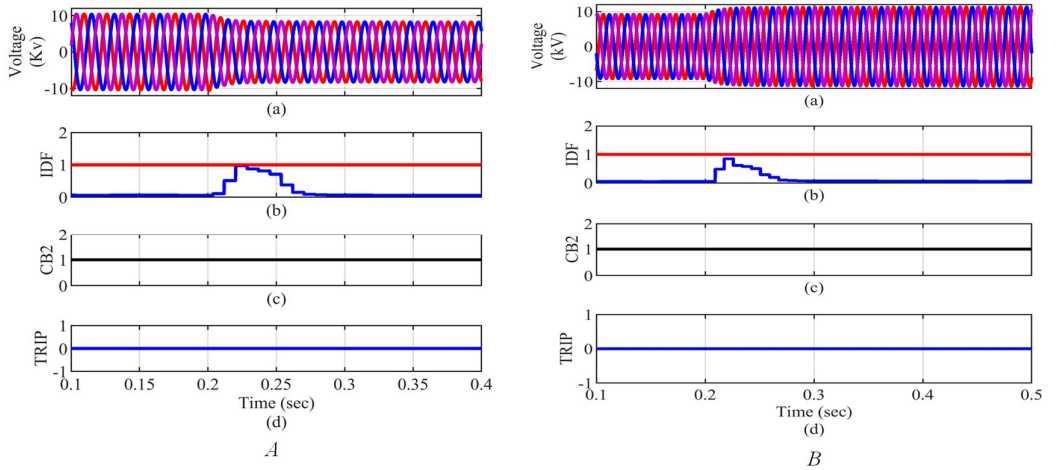

Figure 4.16 Performance under non-islanding events (A) under voltage sag (B) under voltage swell

The performance of the proposed algorithm has been tested for two different network configuration, which is done by changing the status of the network switches i.e. SW1 and SW2 as shown in Figure 4.3. The magnitude of the IDF is tested for different configuration under various islanding and non-islanding events viz. switching of the MCB, switching of inductive or capacitive loads, sudden change in load, voltage swag/swell, change in DG rating and different type of fault conditions. In all the above test cases, magnitude of the IDF lies between the threshold values of IDF i.e. (IDF_{min}=1 & IDF_{max}=10) only for islanding condition and for non-islanding events its magnitude are beyond the threshold levels. Therefore, for this condition (non-islanding events) TRIP signal is not generated. From the above discussion, it is clear that the performance of the proposed IDT does not affected by changing of the network configuration and types of the target DG.

4.9 Comparative Study of the Proposed IDT

The proposed IDT algorithm is compared with the oscillatory frequency (f_o) based detection method [146] and superimposed voltage based method [114]. The results of these methods are shown in Figure 4.17. In [146], frequency deviation based method is suggested and the

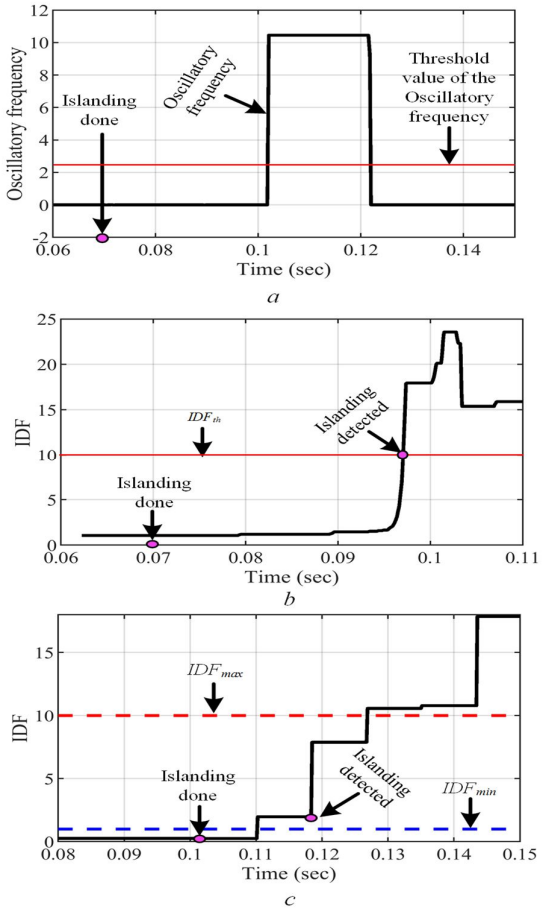

Figure 4.17 Comparison between published and proposed IDT

magnitude of f_o is used to discriminate the islanding event from non-islanding events. The threshold value of $(f_o)_{th}$ is 2.5 Hz. The magnitude of "f_o" for islanding condition is lower than the threshold value ($(f_o)_{th}$=2), however, for non-islanding condition, the magnitude of f_o is above the threshold value $(f_o)_{th}$. The performance is verified for islanding condition under 0% power mismatch case and waveforms are shown in Figure 4.17*a*. Here, the magnitude of f_o crosses the $(f_o)_{th}$ as shown in the figure that is a non-islanding condition. Hence, this islanding detection method fails. In second method, super imposed component of voltage is presented [114] that detect islanding for perfectly power balanced condition in 27ms shown in Figure 4.17*b*.

The response of the proposed IDT under similar condition is tested and results are shown in Figure 4.17*c*. Islanding is done at 0.101 sec and detected at t=0.112 sec. Since, the transition in the IDF magnitude occurs between the predefined thresholds of the IDF i.e. IDF_{min}=1 & IDF_{max}=10. Therefore, islanding detection time is 11 ms (0.112 sec - 0.101 sec) that is less than 27ms of [114], as presented in Table 4.1. From the above discussion, it is clear that the proposed IDT works satisfactorily under perfect power balance condition. The IDT has no NDZ and also less detection time. Therefore, the proposed IDT method is found to be superior to the existing techniques.

4.10 Summary

In this chapter, the design and implementation of a new *IDT* based on an *IDF* parameter is presented. The *IDF* is determined from periodic maxima of superimposed voltage components of the target DG. The *IDT* algorithm is emulated on the reconfigurable hardware i.e. FPGA. The HIL testing of the developed *IDT* is performed using hardwired interfacing with the MG test model designed in RTDS®. Verilog HDL is used for the hardware development which lowers the computational burden and also the utilization of the available on-chip resources. The *IDT* is accurate and detection time is observed to be lesser than other existing techniques and works satisfactorily for zero power mismatch condition between the main grid and MG. Its performance is also tested for non-islanding events i.e. different types of faults, and the given *IDT* algorithm satisfies the restraining attributes. The maximum detection time of the developed *IDT* is 14ms when power mismatch is 25 %.

Now, after being discussed regarding the islanding detection of microgrid, the next chapter presents a multifunctional relay for islanding detection and mode adaptation.

CHAPTER 5: MODE ADAPTATION SUBSEQUENT TO ISLANDING OPERATION

5.1 Introduction

Islanding detection is an important factor of the microgrid (MG) protection. Since a MG can work in two different modes, i.e., grid-connected or stand-alone/islanded mode, during any abnormality appearing in the upstream grid, the MG must be decoupled at the point of common coupling and made to operate in the islanded mode to sustain the critical loads. Because of this mode switching, it is necessary to change the pick-up current settings of the overcurrent relays (OCRs) at the distributed generators (DGs) to accommodate the changes in the current levels. In this chapter, the prototype of a hardcore multifunctional relay is designed on a reconfigurable FPGA, which is not only used for islanding detection but also caters further protection issues i.e., mode adaptation. The proposed IDT incorporates the advantages of two IDTs viz ROCOF and VU. Along with it, an overcurrent module (OCM) is also incorporated to facilitate the mode adaptation feature. Various parameters such as 3-phase voltage and current were monitored and estimation of other parameters such as frequency and 3-phase sequence components have been carried out on the FPGA. Another feature of the proposed design is the mode adaptability that updates the settings of the OCR placed at the active DGs terminal when the islanding is done. A modular approach is used to implement the design, which is targeted on FPGA. HDL, Verilog, is used to develop the optimized design of the hardware. HIL verification for various test cases under different power mismatches is performed with the Real Time Digital Simulator (RTDS) with FPGA prototype of the relay.

5.2 Architecture of Microgrid

Figure 5.1 shows the microgrid test system modeled in the RTDS, which consists of four DG units (two synchronous generators, a solar array and a wind farm), five local loads which are modelled as constant power type (with fixed MW or MVar) and two transmission lines [147] [148]. The MG is connected to the utility grid through the point of common coupling (PCC). Parameters of the grid components are given in Table A. 3 of the Appendix. Operating voltage of the MG is 25 kV and 50 Hz frequency. Operating modes of the MG is defined by the status of the circuit breaker (CB). When *CB1* (CB placed at PCC) is in active high state, MG works in grid-connected mode and is in synchronous with the utility grid, otherwise, it operates in standalone mode. For the whole MG system, a multifunctional relay is designed on FPGA

for monitoring of the local parameters viz. voltage, current along with their sequence components i.e. positive and negative components. The multifunctional relay is placed at PCC, which is used for islanding detection and six OCRs are placed at locations *CB2*, *CB3*, *CB2.1*, *CB2.2*, *CB3* and *CB3.1*. These OCRs have different sets of pick-up current (I_p) settings for two different operating zones i.e. setting for grid-connected and standalone mode.

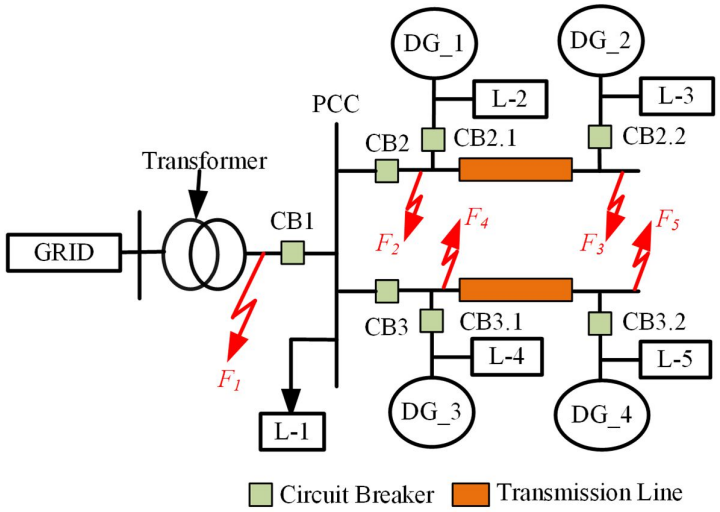

Figure 5.1 Microgrid test system modelled in RTDS

5.3 Internal Architecture of Multifunctional Relay

There are various signal pre-conditioning blocks i.e. DC-Offset, AAF (Anti-aliasing filter), ADC (Analog to digital converter) along with the developed *IDT* modules viz. Sequence detector module (SDM), Voltage unbalance (VU) module, Rate-of-change of frequency (ROCOF) module and MUX (Multiplexer) of the proposed design as shown in Figure 5.2. These blocks are used to explain the complete architecture of the multi-functional relay. The dc-offset module is used to make the measured sinusoidal signals compatible with the ADC. Its offset is taken as 1.65 V for the sampling of 2.5 V (P-P) sinusoidal input signals. Thereafter, the signal is passed through the AAF, which is used to remove all the higher frequency transient components above 200 Hz. A 14-bit programmable pre-amplifier, two-channel, serial ADC (LTC1407A-1) is used in the proposed design. The output of ADC is processed by the Discrete Fourier Transform (DFT) module where the fundamental component of the signal is extracted. The emulation of the OCR is presented under the OCM module. Here, the magnitude of the root-mean-square of the incoming signal and emulation of the inverse characteristics is performed. A detail discussion on the above is given in Section 2.3 of Chapter 2. Thereafter, in the SDM module, symmetrical positive-negative-zero sequence components of the 3-phase

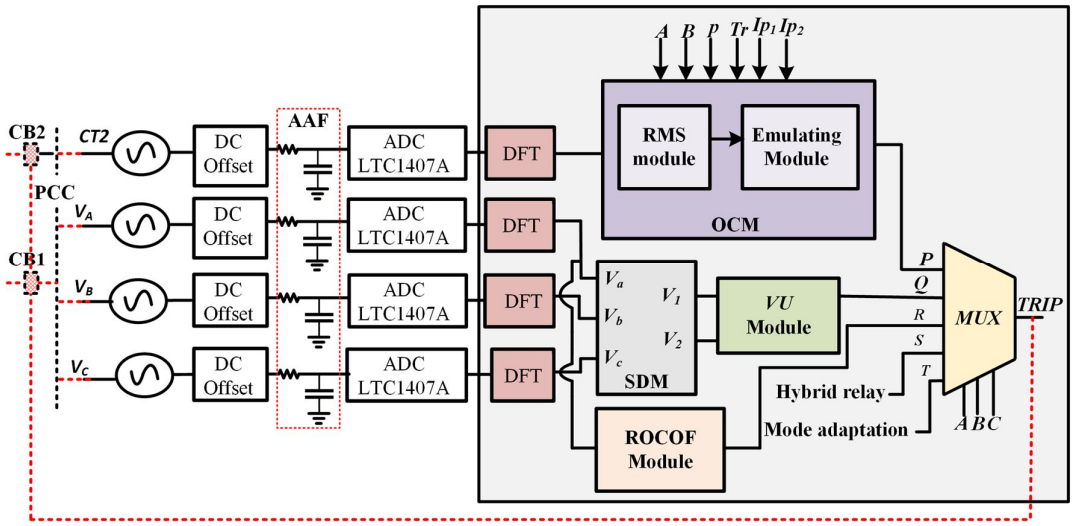

Figure 5.2 Design-flow of the proposed design

input voltages are extracted using a phase-shifting algorithm. Its output is fed into the *VU* module, where the computation of the voltage unbalances is carried out. In the ROCOF module, computation of the magnitude of the frequency and ROCOF have been performed using backward difference algorithm [149]. A *MUX* is designed to route the output of the OCM, SDM and ROCOF modules by the control signals i.e. *A*, *B* and *C*. Finally, the output of the multifunctional relay is fed to the CBs i.e. *CB1* and *CB2* of the RTDS to act accordingly for islanding detection and mode adaptation. The magnitude of the measured parameter at PCC is continuously compared with the pre-defined thresholds. When the parameter value goes beyond the pre-set threshold values, *a TRIP* signal is generated and the status of *CB* in updated.

5.3.1 Design of Over-current Module

The variation in current magnitude flowing through the microgrid is observed when it works under grid connected and islanded modes during any network contingency. Hence, taking account of 3-phase current at PCC enhances the effectiveness of DGs operation during islanding condition. The magnitude of the fault current is also different for the two modes of operation. The realized OCM has two different sets of threshold settings. Working principle of this module is based on the magnitude of the fault current i.e. when the measured current is greater than the pre-defined threshold (I_{th}) due to abnormal operation of the MG along with the mode of operation; a trip signal is generated and transferred to the CB. A detail discussion on the design of the OCR is given in Section 2.2 and Section 2.3 of Chapter 2.

5.3.2 Design of Voltage Unbalance Module

Bus voltage variations is a significant parameter that indicates any discrepancies viz. network faults, topological change and tripping of large generator or load. Hence, the 3-phase

voltage at the PCC is taken into account to enhance the effectiveness of islanding detection. This attribute is aggregated into the proposed hybrid islanding detection scheme by using the voltage unbalances (*VU*) arising at the PCC. The realized *VU* detection module considers both voltage magnitude and phase unbalances by converting the 3-phase voltages into symmetrical positive-negative-zero sequence components given by equation(5.1). Thereafter, the *VU* is defined as the ratio of the instantaneous negative sequence to the positive sequence of the bus voltage given by the equation (5.2) [91], [150].

$$\begin{bmatrix} N_0 \\ N_1 \\ N_2 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}\begin{bmatrix} N_A \\ N_B \\ N_C \end{bmatrix} \tag{5.1}$$

$$VU = \frac{N_2}{N_1} \times 100 \tag{5.2}$$

In the above equations N_0, N_1, and N_2 are the positive, negative, zero sequences whereas N_A, N_B, and N_C, are the 3-φ voltage at PCC.

The *VU* module is implemented on FPGA that is used to extract the sequence components. The data fed into this module is pre-processed by the ADC module and the DFT. The output of the ADC is passed through the DFT, where the fundamental components are extracted. Phase shifting algorithm is used for the estimation of sequence components. An expression representing the sequence components are given by the equations (5.3), (5.4) and (5.5) [151].

$$3N_{0(n)} = N_{A(n)} + N_{B(n)} + N_{C(n)} \tag{5.3}$$

$$3N_{1(n)} = N_{A(n)} + N_{B\left(n-\frac{2m}{3}\right)} + N_{C\left(n-\frac{m}{3}\right)} \tag{5.4}$$

$$3N_{2(n)} = N_{A(n)} + N_{B\left(n-\frac{m}{3}\right)} + N_{C\left(n-\frac{2m}{3}\right)} \tag{5.5}$$

In the above equations, 'n' is the "n_{th}" number of sample, 'm' represents the total number of samples in one fundamental cycle. 0.750 *kHz* is the sampling frequency used to accommodate the '15' samples in a fundamental cycle. Equations (5.4) and (5.5) are used for the computation of the *VU*.

5.3.3 Design of the Rate of Change of Frequency Module

Power imbalances in distribution network cause variation in frequency (a global parameter). When the microgrid is disconnected from main grid with a power mismatch, the frequency will

change. With the value of df/dt measured over a few cycles, the islanding can be detected and inverters shut down, if it exceeds a setting threshold. The magnitude of frequency variation w.r.t time i.e. ROCOF is directly proportional to the power imbalances (difference between generation and demand, ΔP) and inversely proportional to the moment of inertia (H) and generation capacity (G) as given by the equation (5.6) [60].

$$ROCOF, \left(\frac{df}{dt} \right) = \frac{\Delta P}{2HG} \tag{5.6}$$

Any fault conditions or tripping of large generators may cause the loss of mains (LOM) scenario. An effective method for islanding detection can be implemented by continuous monitoring of the voltage waveforms at the PCC. Thereafter, a trip signal is generated, if the magnitude of ROCOF increases beyond the predefined threshold for a certain time duration. This technique avoids maloperation, which arises due to the non-islanding switching operations within the MG. Equations(5.7), (5.8) and (5.9) are used to compute the frequency of the analog signal [149].

$$X(t) = A\sin(\omega t + \varphi) \tag{5.7}$$

$$X(t) = \underbrace{A\sin(\omega t + \varphi)}_{In-phase\{x_1(t)\}} + \underbrace{A\cos(\omega t + \varphi)}_{quardrature\{x_2(t)\}} \tag{5.8}$$

$$f = \frac{x_2(t)\dot{x}_1(t) - x_1(t)\dot{x}_2(t)}{2\pi\left[x_1^2(t) + x_2^2(t) \right]} \tag{5.9}$$

Now, a brief discussion of the frequency measurement module (FMM) developed on FPGA hardware is discussed below.

The sinusoidal signal output from the CT is input to the ADC module where the analog signal is converted to the digital signal. This signal is processed by the DFT filter, where digital signal $\{x(n)\}$ is decomposed into two components i.e. in-phase $\{x_1(n)\}$ and quadrature component$\{x_2(n)\}$. Backward difference algorithm is used for the calculation of time derivative viz. $\{\dot{x}_1(n)\}$ and $\{\dot{x}_2(n)\}$ of the in-phase component $\{x_1(n)\}$ and quadrature component $\{x_2(n)\}$ respectively. Mathematical expression for the backward difference algorithm is given by (5.10).

$$\dot{x}(n) = \frac{x(n) - x(n-1)}{\Delta T} \tag{5.10}$$

$$f \approx \frac{\{x_2(n) + x_2(n-1)\}\dot{x}_1(n) - \{x_1(n) + x_1(n-1)\}\dot{x}_2(n)}{\left\{ \{x_1(n) + x_1(n-1)\}^2 + \{x_2(n) + x_2(n-1)\}^2 \right\} \times \pi T} \tag{5.11}$$

In the above equation, ΔT is the sampling period. Expression of frequency determination is given by equation(5.11). The effective ROCOF is computed by using equations (5.12) and (5.13). In the equation(5.13), k is the scaling factor of ROCOF and its magnitude is considered as constant i.e. k=10.

$$\dot{f}(n) = \frac{x(n)(n) - x(n-1)}{\Delta T} \tag{5.12}$$

$$ROCOF = k \times \left[\sum_{1}^{n} \dot{f}(n) \right] \tag{5.13}$$

5.4 Experimental Setup for HIL Verification

Figure A. 2 of the appendix shows the experimental setup for HIL-verification of the proposed multifunctional relay. The proposed algorithm is targeted on virtex®5 (XC5VLX50T-3FF1136) FPGA [137]. RTDS is used to simulate the power system network and closed-loop verification of the developed relay [140]. Phasor information of the positive, negative, and zero sequences (voltage and current) are monitored at PCC. These signals are further processed on RTDS and FPGA for the emulation of the different conditions discussed in Section II. Gigabit Transceiver Analogue Output Card (GTAO) and Gigabit Transceiver Digital Input Card (GTDI) card are the interfacing card of the RTDS that are used to communicate the internal signal of network to the external device (FPGA). These cards are associated with the internal amplifier, which is used to bring the peripheral devices at the compatible level. Monitored signals are processed on the RTDS and taken out from the GTAO card. The gain of the voltage converter is fixed at 36 to detect and bring the maximum fault current to the equivalent level with maximum range of 2.5 V (P-P) of the ADC. A dc-offset module of 1.65 V is required to sense the bi-directional sinusoidal input signals. Outputs of this offset module are passed through an AAF. The filtered signals are further processed by the ADC module before passing it to the FPGA chip. Now, in FPGA tripping condition is checked by the designed internal hardware, and if it is satisfied, *TRIP* signal is generated for the CBs installed in the MG of RTDS through the GTDI card. Digital storage oscilloscope (DSO), is used to monitor the output signal coming from the GTAO card and the trip signal of the designed module of the prototype. A detailed list of the settings of the used components for HIL testing is provided in Table 5.1. Also, the communication latency between RTDS and FPGA board during the HIL-implementation and effects of dead-zone have also been considered.

The impact of dead-zone on the developed FPGA prototype is removed by the use of high-speed analog to digital converter (ADC) with high resolution. In the proposed prototype, the resolution of the used ADC is 152.59 μV. If any change occurs within this limit, the dead-zone

Table 5.1 Components settings for HIL-Verification of the proposed prototype

Sl. No.	List of Components	Maximum Range	Set values
1	ADC(LTC1407A-1of Spartan 3E-development board)	0.4v-2.9v	2.5 V (P-P)
2	Gain of the amplifier settings	(-1)-(-100)	-1
3	GTAO CARD (o/p voltage)	±10v	±1.25 v
4	GTAO CARD (o/p scaling)	(-1e6)- (+1e6)	36
5	Sampling frequency of ADC	1.5 mega-samples per second	37.5 kHz
6	Offset value	(0v-5v)	1.65 v
7	Cut-off frequency of AAF	-	200
8	CT turn ratio	-	380
9	DFT CLOCK	-	0.750 kHz

conflict occurs. However, this magnitude is very less (i.e. in μV), which is considered insignificant as compared to the magnitude of the signals being measured (~mV). The communication latency during HIL-implementation was obtained from the datasheets and by experimentation. During HIL verification, signals are taken out from the GTAO card through GPC processor of RTDS. The latency between GPC processor card and GTAO card is 9.203 μs [143]. The communication latency of the signal conditioning module i.e. AAF and dc-offset modules is 62.5 μs. Whereas, the latency of the ADC module is ~25 μs. Further, the signal is processed through the implemented multifunctional relay on FPGA where different computations are performed in the DFT, OCM, SDM, ROCOF and VU modules which are runs on the master clock of 100 MHz. The latency of these computations is commutated determined as 525 μs. Hence, the total latency of the complete design is approximately 621 μs.

5.5 Results and Discussion

Various test conditions have been considered for the HIL verification of the proposed relay. A (5:1) multiplexer is designed to select the operating mode of the multifunctional relay which is controlled externally by the input signals i.e. *A*, *B*, and *C*. The output of the proposed prototype is given by (5.14).

$$TRIP = \bar{A}\bar{B}\bar{C}P + A\bar{B}\bar{C}Q + \bar{A}B\bar{C}R + AB\bar{C}S + \bar{A}\bar{B}CT \tag{5.14}$$

In the above equation *P, Q, R, S* and *T* are the internal output of the sub-modules viz. overcurrent, *VU, ROCOF,* hybrid relay and mode adaptive respectively. Implementation technique for selecting a different operating mode of the designed relay using the control inputs *A, B* and *C* are given in Table 5.2.

Table 5.2 Functional modules of the relay

Control signal			TRIP (o/p)	Relay functionality
A	**B**	**C**		
0	0	0	$\overline{ABC}P$	Overcurrent module
0	0	1	$\overline{AB}CQ$	VU module
0	1	0	$\overline{A}B\overline{C}R$	ROCOF module
0	1	1	$AB\overline{C}S$	Hybrid
1	0	0	$\overline{AB}CT$	Mode adaptation

Now, the performance of the designed hardcore relay has been evaluated under various conditions as discussed in the subsequent sections.

5.5.1 Perfectly Matched Load and Generation

In this case, the performance of the relay is verified for the different mode of operations as discussed in Table 5.2. Different conditions for IDTs and operation of the OCM has been verified when the power transfer between the utility grid and the microgrid is zero. To study this condition, the dynamic load at PCC is fixed at 2 MW. The amount of power supplied by grid, DG1, DG2, PV and wind are considered as 0 MW, 4 MW, 5 MW, 1.7 MW and 1.93 MW respectively. The obtained results are discussed in the following sub-sections.

5.5.1.1 Verification of OCM for control input ABC=000

Performance of the OCM is verified for both the operating modes of the MG i.e. grid connected and standalone mode and results are discussed as *case-1* and *case-2*.

CASE:-1

A test case for the verification of EI characteristic with TDS=1 and *Ip*=0.9A is conidered. The output of CT represents the line current as shown in Figure 5.3*a* with colour signal. The current signal is converted to the voltage signal through GTAO card and given as input to the ADC module. Status of the trip signal "*TRIP2"* generated by the prototype, is further passed through an amplifier to act as the digital input for the GTDI card as shown in Figure 5.3*e*. In Figure 5.3, signals *MODE*, *FLT, CB2,* and *TRIP2* represent the operating mode of the MG, the status of CB2, the status of the fault and the trip signal generated by the multifunctional relay prototype respectively. The status of the signal *MODE*=1 shows the operation of the MG in grid-connected mode and *MODE*=2 represents the standalone mode of operation. *CB2*=1 shows the CB is closed whereas *CB2*=0 gives its opened status. *FLT*=1 represents the occurrence of the fault whereas *FLT*=0 represents the normal condition. The trip signal generated by FPGA

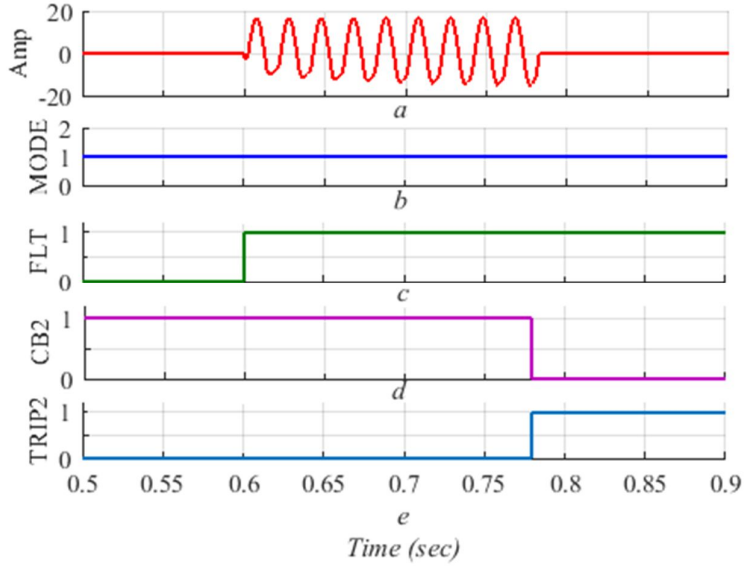

Figure 5.3 Results of the OCM for grid-connected mode

as *TRIP2*=0 for normal operations and *TRIP2* =1 for faults which in turns opens the CB2 to isolate the upper section of the MG.

In this case, fault F_2 shown in Figure 5.1 is incepted at t=0.602 sec. For this fault, a maximum fault current of 19.23A is observed as shown in Figure 5.3*a*. The trip time taken by the prototype to trip the CB2 is 0.1763 seconds shown in Figure 5.3*e*. The trip generation time is verified with a standard OCR of the RTDS under identical test condition. Tripping time of the RTDS relay is monitored by a counter which is approximately 0.1752 seconds. Hence, the performance of the designed OCM is as par with the standard library OCR of the RTDS.

CASE-II

Here, the impact of the fault current during the standalone mode of operation of MG is observed. The settings of the OCR for the verification of EI characteristic are kept as TDS=1 and *Ip*=0.9A. The signals shown in Figure 5.4 are discussed in the previous case. In this case, fault F_2 shown in Figure 5.1 is incepted at t=0.599 sec. For this fault, the maximum fault current is 2.1 A, as shown in Figure 5.4*a*. The trip time taken by the prototype to trip the CB2 is 1.536 sec shown in Figure 5.4*e*. Whereas, the tripping time of the RTDS OCR is ~1.529 sec, which is monitored by the inbuilt counter of the RTDS.

Therefore, from the above results, it is observed that the magnitude of a fault current in grid-connected mode is more than the standalone mode. Also, it is important to note that the trip time is more in case of a grid-connected mode in comparison to the standalone mode. Hence, as mentioned in the introduction section a mode-adaptability of the OCR module is required to be enforced as presented in the later part of this section.

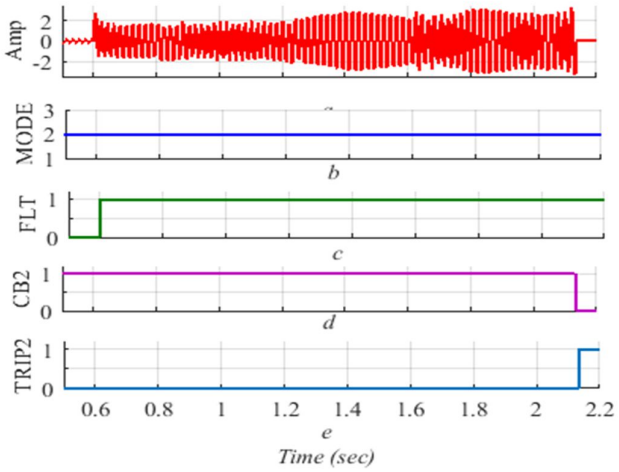

Figure 5.4 Results of the OCM for standalone mode

5.5.1.2 Verification of VU module for control input ABC= 001

Now, the impact of the VU for IDT has been discussed for the control signal *ABC=001*. The magnitude of the node voltage at PCC, status signal |VU|, *CB1* and *TRIP1* are shown in Figure 5.5. The signals *CB1* and *TRIP1* are same as described in the previous case. An LG fault between phase "A" to the ground is incepted at t= 0.7004 sec for verifying the impact of VU on the IDT. The magnitude of VU before the fault inception is zero as shown by the status signal |VU|=0 in Figure 5.5*b*. The magnitude of VU is ~2 after fault inception. Since, the measured variation is greater than the threshold value of the VU_{th}=1, and |VU|=1 which initiates a trip signal to opens CB1 and making the MG work in the standalone mode of operation. In this case, *TRIP1* signal is generated at the time instant t= 0.7109 sec and islanding detection time is about 10 ms.

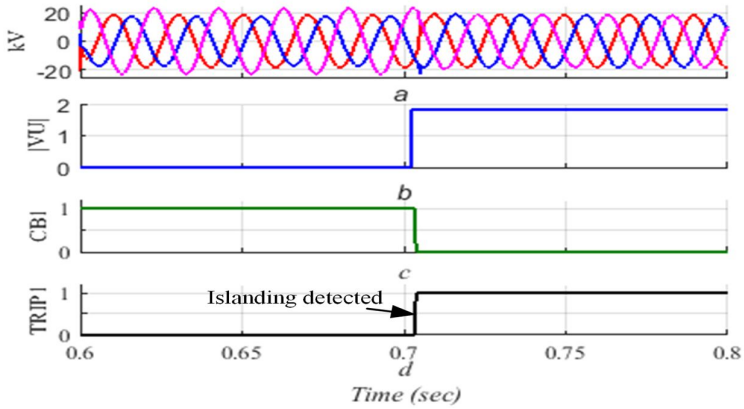

Figure 5.5 Status of the signal for HIL- verification of VU module

5.5.1.3 Verification of ROCOF module for control input ABC=010

Now, IDT based on ROCOF module has been discussed. The magnitude of the node voltage at PCC, frequency, and ROCOF are shown in Figure 5.6. Signal *CB1* shows the status of the circuit breaker at PCC and gives the information about operating mode of the MG, when CB1=1, MG works in the grid-connected mode and when CB1=0, MG works in the islanded mode shown in Figure 5.6. *TRIP1* is the signal generated by the FPGA, which gives the instant of islanding detection after the islanding occurred and monitored in RTDS through GTAO card of the RTDS. Before islanding, the system frequency is 50 Hz and ROCOF=0 as shown in Figure 5.6*b* and Figure 5.6*c*. In this case, islanding occurs at t=0.606 sec. After the islanding event, variation in the measured parameters viz. f>~50.5 Hz and |ROCOF|>~5 Hz/s are observed. Here, *TRIP1* signal is generated by the FPGA at instant t = 0.625 sec. Hence, here the islanding detection time is 19 msec.

5.5.1.4 Hybrid mode of operation for control input ABC= 011

In this case, the impact of the hybrid IDT is discussed for the control signal *ABC=011*. The effect of |VU| and ROCOF are simultaneously considered for islanding detection. The magnitude of the PCC voltage, FLT, |ROCOF|, |VU|, TRIP and *CB1* are shown in Figure 5.7. These signals are discussed in the previous sections. When the measured variations are greater than the threshold value of $|VU_{th}|$ and $|ROCOF_{th}|$, which are set to 1 and 5 respectively, a trip signal is initiated which opens the CB1 and the MG works independently in stand-alone mode.

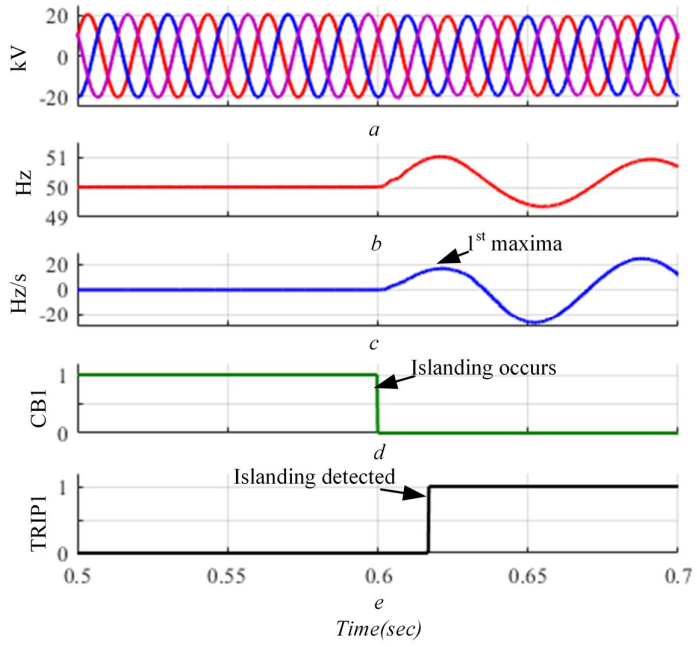

Figure 5.6 HIL-verification of the ROCOF module for constant power load

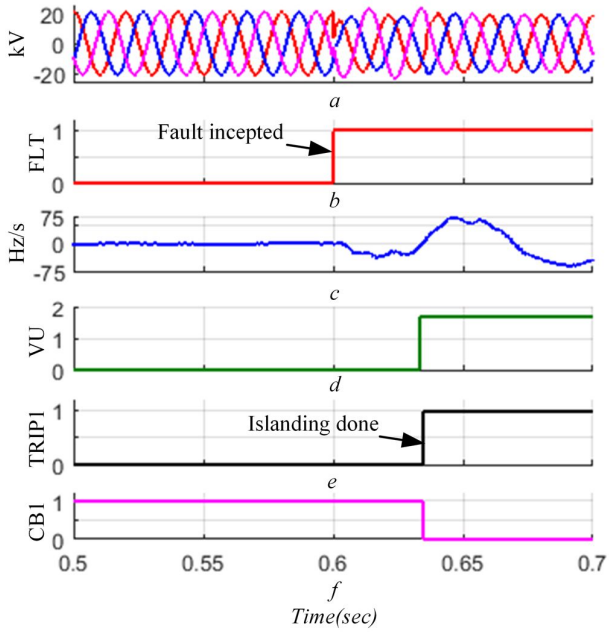

Figure 5.7 Operation of the hardcore relay in hybrid mode

A fault F_1 (LG) is incepted at t=0.5984 sec for verifying the hybrid operation of the hardcore relay with VU and *ROCOF* modules. The magnitude of the |*ROCOF*| and |VU| before fault inception is "0" as shown in Figure 5.7*c* and Figure 5.7*d*. Whereas, the magnitude of |*ROCOF*| and |VU| after fault inception is ~75 and ~2 respectively. Since the measured variation is greater than the threshold values, a trip signal is generated which opens the CB1. Here, TRIP1 signal is generated at the time instant t= 0.644 sec and islanding detection time is 46 ms.

5.5.1.5 Verification for adaptation of relay

From the above discussion, it is clear that the magnitude of the fault current in grid-connected mode is higher than the fault current for the standalone mode of operation. If the I_p settings for both the modes are kept constant then as per the inverse characteristics of the OCR, relay tripping time is more in standalone mode as compared to grid-connected mode [152]. Due to this, components of the MG network are adversely affected that might lead to equipment failure. To avoid such damage, the proposed hardcore based multifunctional relay is integrated with mode adaptive features. In which, two sets of I_p setting can be predefined for the OCR, one for grid-connected and other for the islanded mode. These predefined values are digitally controlled by the signal MODE. Figure 5.8 shows the status of the control signals i.e. *FLT, CB1, CB2, ROCOF, VU, TRIP1, MODE* and *TRIP2* generated by the FPGA hardware. Signals i.e. *FLT, CB1, CB2, TRIP1, MODE and TRIP2* are defined in the previous sections. In Figure 5.8, ROCOF and VU are the control signal generated by the FPGA. These signal have two sets of values i.e. 0 and 1 signifying that the measured value is less than or greater than the

predefined threshold values respectively. The magnitude of the CT current measured at *CB2* terminal is shown in Figure 5.8*a*. Control signals CB1 and CB2 represent the status of the CB located at PCC and the upper section of the MG, shown in Figure 5.8*c* and Figure 5.8*d*. For the verification of mode adaptation, the threshold values for VU, ROCOF, I_{p1} and I_{p2} are taken as 1, 5, 1 and 0.5 respectively. I_{p1} and I_{p2} are the settings of the OCR in the grid-connected and standalone mode of operation respectively.

In this case, fault F_2 is incepted at t=0.6006 sec as shown in Figure 5.8*b*. Control signal for the ROCOF and VU changed their state at t= 0.642857 and 0.6519 sec as shown in Figure 5.8*e* and Figure 5.8*f* respectively and islanding is detected at t=0.6519 sec as shown in Figure 5.8*g* and at this instant MG is disconnected from the utility grid and control signal MODE is updated from 1 to 2 as shown in Figure 5.8*h*. Finally, CB2 is opened at t= 2.32092 sec shown in Figure 5.8*i* signifying that the OCM is operating for I_{p2} which is meant for the islanded mode. Hence,

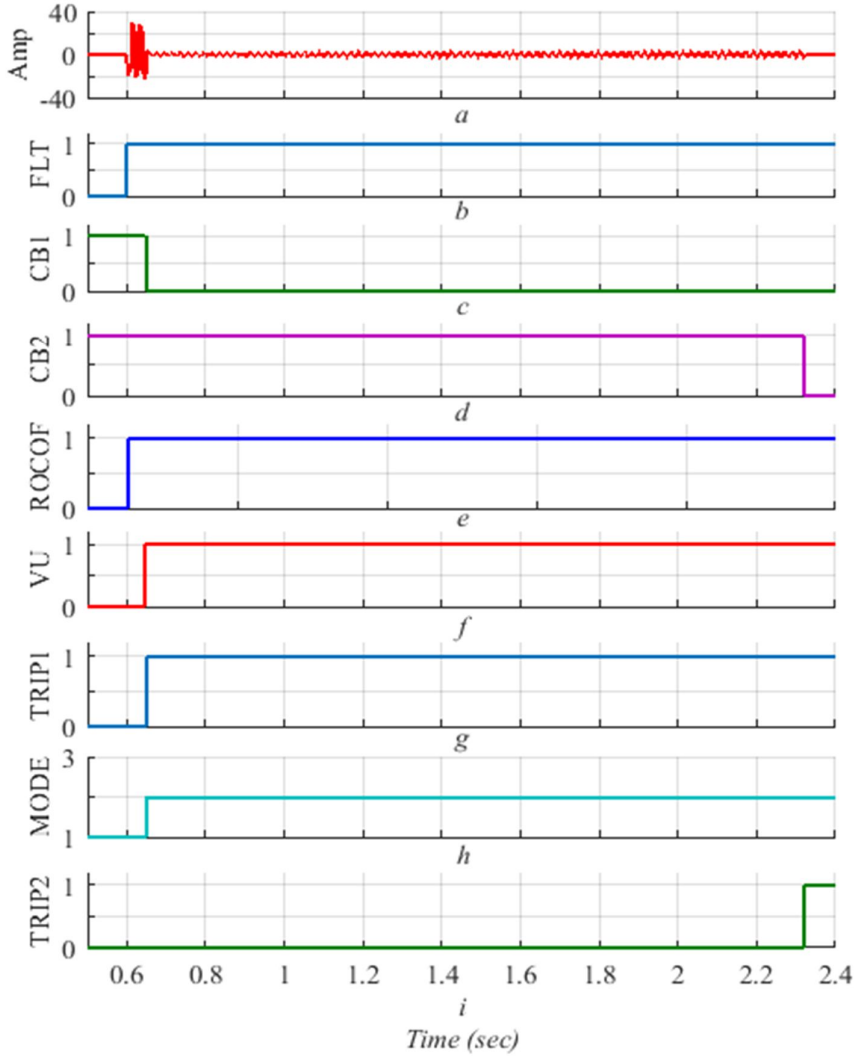

Figure 5.8 Performance of the relay under mode adaptation

from this discussion, it is clear that the mode adaptation for the OCM achieved, once the islanding is detected.

5.5.2 Power Mismatch between Load and Generation is 25%

The performance of OCM, ROCOF and VU modules, along with the hybrid IDT and mode adaptation is verified for an extensive set of test conditions i.e. at different fault location F_1, F_2, F_3, F_4 and F_5, for LG and LLLG faults. The dynamic load at PCC is fixed at 3 MW to verify the working of the relay under these conditions. At this dynamic load, the amount of output power of the grid source, DG1, DG2, PV and wind is -1.6 MW, 4 MW, 5 MW, 1.7 MW and 1.94 MW respectively. The performance of the OCM in the grid-connected and stand-alone mode of operation, VU module and ROCOF module for control inputs 000, 001 and 010 respectively are verified and results are shown in Table 5.3.

Now, one of the cases (Case-I) for control inputs (000) is discussed here. A line-to-ground fault (*FLT*) is incepted at location F_2 at t=599 ms. The magnitude of the fault current is observed to be 16.96 A. The OCR is operated in grid-connected mode when the status signal *MODE=1*. Here, the tripping time of OCM prototype on FPGA is found to be 179ms. A similar case study has been done for the islanded mode of operation in case-II representing the stand-alone mode

Table 5.3 Verification of the designed module of the proposed relay

When control inputs are "000"					
	I_F (Amp)	***MODE***	***FLT***	***TRIP2***	***CB2***
CASE-I (F_2,a-g)	**16.96**	**1**	**t=0.59945 s**	**t=0.7784 s**	**0, 0.1790 s**
CASE-II (F_2,a-g)	3.24	2	t=0.77874 s	t=2.1413 s	0, 1.5391 s
When control inputs are "001"					
	V_{PCC} (kV)	***|VU|***	***FLT***	***TRIP1***	***CB1***
F_1 (a-g)	15.78	1.83	t=0.5984 s	1, at t=0.6589s	ID at t=0.0605s
F_2 (a-g)	18.03	1.60	t=0.6061 s	1, at t=0.6763s	ID at t=0.0701s
F_3 (a-g)	**20.00**	**0.29**	**t=0.6061 s**	**0**	**Not affected**
F_4 (a-g)	17.92	1.40	t=0.6061 s	1, at t=0.6329s	ID at t=0.0268s
When control input is "010"					
Power unbalance (%)	***ROCOF (Hz/s)***	***CB1 (Islanding Done)***	***TRIP1 (Islanding Detected)***		
			By Prototype	***By RTDS***	***By COM-relay (SEL-751)***
0	~19.8	0, at t=606ms	19ms	18.8ms	19.2ms
25	**~25.17**	**0,at t=599ms**	**9ms**	**8.7ms**	**8.9ms**
50	~28	0,at t=599ms	~8.7ms	~8.5ms	8.8ms
75	~30	0,at t=599ms	~8.4ms	~8.2ms	9ms

of operation. In this case, the magnitude of fault current is observed as 3.24A and tripping time of the OCM prototype on FPGA is 1.362s.

For control signal 001, the performance of the VU module of the prototype is verified for different types of faults applied at the different locations as shown in Figure 5.1. When the measured value is greater than the threshold ($VU_{th}=1$), the trip signal is generated and sent to CB1 otherwise CB1 remains in its previous state. A case for the control signal "001", highlighted in Table 5.3, is discussed here. A line to ground fault (F_3) is incepted at t=606ms, for this fault, the magnitude of VU, observed as 0.29, is less than $VU_{th.}$ Therefore, in this condition, the status of the CB1 is not affected and it still works in the grid-connected mode of operation.

Performance of the ROCOF module of the prototype is verified and results are presented in Table 5.3 for the control input "010". The performance of the developed relay prototype is validated with the standard relay of RTDS and a commercial relay (COM-relay) (SEL-751) [153] in a closed loop environment, also given in Table 5.3. Here, the percentage of power imbalance, instant of islanding i.e. opening of CB1, tripping time of the prototype, RTDS and COM-relay are presented. A test case for control inputs "010" (highlighted) is discussed here for 25% power imbalance condition. Islanding occurs at t=599ms by opening the CB1. The amount of ROCOF in this condition is greater than $ROCOF_{th}$ and the trip signal is initiated by the prototype. The comparative tripping time for the developed prototype, RTDS, and COM-relay are found to be 9, 8.7 and 8.9ms respectively. This signifies that the islanding is detected within half time of the power cycle.

In Table 5.4, the operation of hybrid IDT for 25 % power mismatch is presented. The instants at which status of various signals (FLT, $TRIP_{ROCOF}$, $TRIP_{VU}$, $TRIP1$, $CB1$) showing changes from initial to final state considered are defined in section 5. LG and LLG faults are incepted to measure the parameter variation. If the variation is greater than the predefined threshold, i.e. $ROCOF_{th}$=5 and VU_{th}=1 simultaneously, then the signal $TRIP1$ is updated and islanding of the MG is performed by opening the CB1. One of the cases of Table 5.4 (Highlighted) is discussed here. An LLLG fault, F_5 (shown in Figure 5.1) is incepted at t=800ms. For this fault, the magnitude of the $ROCOF$ is greater than set $ROCOF_{th}$, and trip signal $TRIP_{ROCOF}$ is generated by the designed ROCOF module. The magnitude of $|VU|$ is less than the magnitude of VU_{th}, therefore, the status of the $TRIP_{VU}$ is not changed. Here, the criterion for islanding is not satisfied. Hence, the status of TRIP1 and CB1 is not changed.

Mode adaptation feature of the designed relay for different fault locations in the case of 25% power mismatch condition is presented in Table 5.5. The magnitude of measured current, fault

Table 5.4 Operation in hybrid IDT for 25 % power mismatch ("011")

	V_{PCC} (kV)	*FLT*	$TRIP_{ROCOF}$	$TRIP_{VU}$	*TRIP1*	*CB1*
F_1 *(a-g)*	0	t= 0.304 s	1, at t=0.332s	1, at t=0.320s	1, at t=0.332s	0, at t=0.332s
F_2 *(a-g)*	0	t=0.400s	1, at t=0.406s	1, at t=0.466s	1, at t=0.466s	0, at t=0.466s
F_3 *(a-g)*	20	t=1.21s	0, $Measured_{ROCOF}$=4.21	0, $Measured_{VU}$=0.14	0	0
F_4 *(a-g)*	0	t=0.402s	1, at t=0.407s	1, at t=0.494s	1, at t=0.494s	0, at t=0.494s
F_5 *(a-g)*	20	t=1.006s	1, at t=1.298s	0	0	1
F_1*(abc-g)*	0	t=0.801s	1, at t=0.943s	1, at t=0.820s	1, at t=0.943s	0, at t=0.943s
F_2 *(abc-g)*	0	t=0.812s	1, at t=0.934s	0	0	1
F_3 *(abc-g)*	20	t=0.812s	1, at t=0.842s	0	0	1
F_4 *(abc-g)*	0	t=0.812s	1, at t=0.934s	0	0	1
F_5 (abc-g)	**20**	**t=0.800s**	**1, at t=0.842s**	**0**	**0**	**1**

inception instant, the status of CB1, and CB2, the trip signal generated by ROCOF and VU modules, the instant of ID, mode adaptation, and trip generation by OCM are given in the figure. Ip_1 and Ip_2 of OCM are set at 1 and 0.5 for *MODE1* and *MODE2* respectively. Signals are discussed in the initial part of the current section. An LG fault (F_1), is incepted at t=304ms, as shown in Figure 5.1. The magnitude of the measured current in grid-connected mode is 13.62A. For this fault, the trip signals are generated by ROCOF and VU module at t=332ms and 320ms respectively. Here, islanding is detected at t=332ms and at this instant MG is disconnected from the utility grid by opening the CB1 and control signal MODE is updated from 1 to 2. Here, CB2 remains in same state i.e. closed as the magnitude of the fault current in the islanded mode of operation is less than $I_{p2,}$ signifying that the OCM is operating for I_{p2} which is meant for standalone mode.

A large number of test conditions have been created in the RTDS to extensive testing of the performance of the designed prototype of hybrid IDT. The various operating conditions namely Line to ground (LG), line to line (LL), line to line to line (LLL), line to line to line to ground (LLLG) and islanding of the MG with different amount of power exchange have been created as shown in Table 5.3, Table 5.4 and Table 5.5. The islanding detection and mode adaptation function for the multi-functional relay have been successfully verified.

It is important to note that, in all the above test cases, constant power type loads are considered. However, a constant impedance load has also been used to verify the performance of the prototype. For this purpose, a test scenario for 0% power mismatch case of the ROCOF module is considered and the results are shown in Figure 5.9. From the Figure 5.6 and Figure

Table 5.5 Adaptive operation of the proposed design

	I_{CT2}	*FLT*	*CB1*	*CB2*	$TRIP_{ROCOF}$	$TRIP_{VU}$	*TRIP1*	*MODE*	*TRIP2*
F_1 (a-g)	**13.62 A**	**t= 0.304s**	**0, at t=0.332s**	**1, after ID I_{F1}=0.299A**	**1, at t=0.332s**	**1, at t=0.320s**	**1, at t=0.332s**	**2, at t=0.332s**	**0**
F_2 (a-g)	33.69 A	t=0.400s	0, at t=0.466s	0, at t=0.466 s	1, at t=0.406s	1, at t=0.466s	1, at t=0.466s	2, at t=0.466s	1, at t=0.466 s
F_3 (a-g)	2.87 A	t=2.002s	1	t ≥ 8s	0	0	0	1	t ≥ 8s
F_4 (a-g)	9.47 A	t=0.402s	0, at t=0.494s	0, at t=0.494s	1, at t=0.407s	1, at t=0.494s	1, at t=0.494s	2, at t=0.494s	1, at t=0.494s
F_5 (a-g)	0.78 A	t=1.006s	1	1	1, at t=1.298s	0	0	1	0

5.9, it is observed that the variation in the magnitude of the measured parameter (1st maxima of the ROCOF) is ~19.8 Hz/sec and ~10 Hz/sec when test system is modelled using constant power and constant impedance type loads respectively. Both these variations in ROCOF value are greater than the preset threshold, and islanding is detected in 19ms and 20ms as shown in Figure 5.6*e* and Figure 5.9*e*.

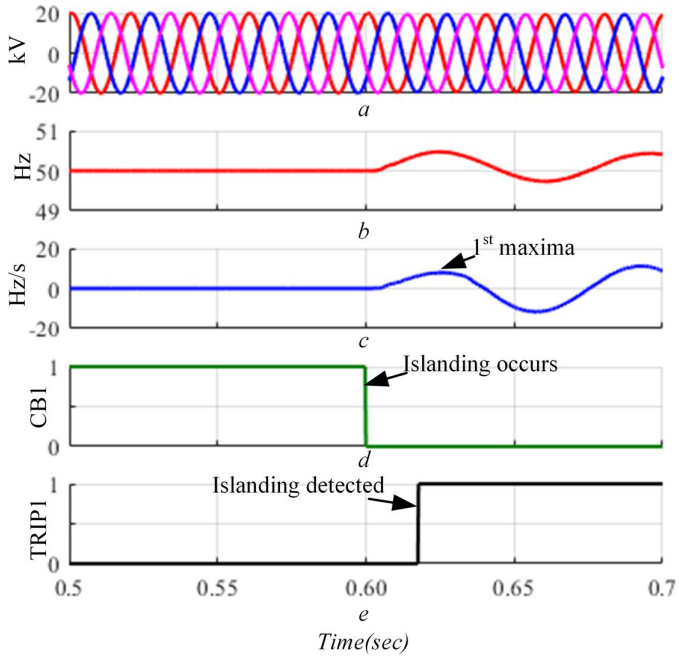

Figure 5.9 HIL-verification of the ROCOF module for constant impedance load

From the above analysis, it is clear that the islanding detecting time is slightly more when loads are considered as constant impedance type than that of the constant power type loads. However, the difference in detection time is insignificant.

5.6 Result Discussion

As mentioned in the introduction section, a mode adaptability feature is inevitably required for the reliable operation of MG, subsequent to the islanding operation. In this regard, it is observed from Figure 5.3 and Figure 5.4 that in the similar condition the magnitude of the fault current in grid-connected mode is higher than the standalone mode. Also, the trip time is more in the case of a standalone mode in comparison to the grid-connected mode. Figure 5.9 verifies the successful mode adaptation between the two modes of operations. From the figure, it can be concluded that when islanding is detected MG changes its mode of operation by changing the I_p setting of the OCR located at the target DG terminal. Rigorous testing has been done for the performance verification of the proposed prototype, by creating different combinations of test conditions which are presented in Table 5.5.

The developed prototype is capable to detect an islanding event with zero NDZ, within the permissible time limits even in the critical power mismatch condition i.e. 0% mismatch. For an LG fault inception, the MG changes its status at t=0.71098 sec from grid-connected to stand-alone mode of operation. The response of the VU module is shown in Figure 5.5. Here, the trip

time of the main CB is 10ms. Similarly, Figure 5.6 and Figure 5.7 represent the operability of the ROCOF module under critical condition i.e. 0 % power mismatch between load and generation. Under this condition tripping time of the ROCOF is 19ms, which implies that the islanding detected for the critical case within a cycle. Figure 5.8 confirms the hybrid operation of the proposed IDT. Here, the trip time is taken 46ms, which is less than that of trip time required by ROCOF and higher than the VU module independently. This signifies that a trade-off between the accuracy and detection time is achieved. Therefore, it can be concluded that the proposed prototype is accurate, having very less detection time and is able to subsequently adapt its mode effectively.

5.7 Summary

In this chapter, design of hardcore multifunctional relay on Virtex®5 XC5VLX50T-3FF1136 FPGA chip is presented. The developed relay has been substantially verified for islanding detection and mode adaptation. Hybrid islanding detection technique based on ROCOF and VU is implemented on the reconfigurable hardware for islanding detection purpose along with an OCM to incorporate the mode adaptation application. The HIL testing has been done by placing the proposed relay through the hardwired interface in the network model designed in RTDS®. The performance of the developed relay prototype is found to be satisfactory.

The design is entirely based on Verilog HDL which lowers the computational burden having minimum resource utilization. The proposed hybrid islanding detection technique is accurate and detection time is observed to be very less. Also, the proposed technique has zero NDZ for a small mismatch between DG and load powers.

CHAPTER 6: COMMUNICATION BASED ADAPTIVE PROTECTION

6.1 Introduction

Microgrids (MGs) are low to medium voltage networks consist of local loads, distributed generators (DGs), renewables (REs) and storage elements. It operates either in stand-alone mode or grid-connected mode when connected to the utility grid. The amount of the fault current in grid-connected mode is higher than that of the autonomous mode of operation. To mitigate the effect of fault current for the protection of the MG, the threshold setting of the overcurrent relay (OCR) as per the operating mode is an important issue. In this chapter, the prototype of a communication assisted adaptive relay (CAAR) is developed on FPGA. It has the ability to adapt the settings of the OCR as per the operating modes of the MG. The status of these modes and the working status of the DGs are communicated through the wireless network using wireless radio transceiver that supports Enhanced ShockBurst protocol. Performances of the prototype have been verified as hardware-in-loop on a developed MG test system with the real-time digital simulator (RTDS). Different test cases i.e. operating modes of the MG, various fault locations, types of faults and relay coordination are rigorously tested to validate the developed CAAR in ensuring accurate operation and protection of the MG.

6.2 Architecture and Internal Design of Developed Relay

Figure 6.1 represents the generalized block schematic of the developed CAAR. Line voltage and current are measured by the current transformer (CT) and voltage transformer (VT) respectively at any specified bus. At these locations, the current and voltage signals are processed by the DC-offset module to meet the requirement of the subsequent analog to digital converter (ADC). A low-pass filter (LPF) is used to mitigate any higher order spurious noise present within the signal. The analog input is converted to 10-bit digital data which is given to the wireless fidelity (Wi-Fi) modules. This Wi-Fi is placed at each CT, VT, circuit breaker (CB) and centralized control unit (CCU) of the proposed protection scheme. These modules have the capability of transmitting and receiving the data from ADC and CCU. At CCU, data received from the wireless channels is processed and various computations viz. extraction of the fundamental and harmonics components, computation of the phase differences (between voltage and current signals) and calculation of the relay tripping time are performed. In CCU, different control action viz. updating of the CB status, identification of the operating mode and updation of the magnitude of relay settings (I_p) have been performed. Finally, trip signal is

generated in the CCU if the required conditions are satisfied. The trip signal is transferred to the CB through the communication channel.

Now, a brief discussion of the working of developed CAAR and its sub-modules viz. signal conditioning module (DC-Offset & LPF), ADC, Wi-Fi (transmitter & receiver) module and CCU is discussed in the following subsections.

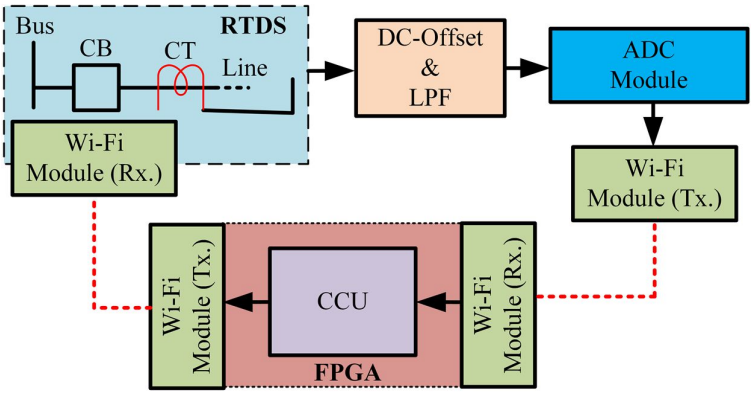

Figure 6.1 Overview of the developed overcurrent relay

6.2.1 Working of Developed Relay Module

In CAAR, inverse characteristics i.e. very inverse (*VI*) and extremely inverse (*EI*) characteristics of the OCR are emulated. Figure 1.4 Characteristics plot (time vs I_{sc}) for VIFigure 1.4 and Figure 1.5 shown in chapter 1, represent the inverse characteristics of VI and EI. In these figures, y-axis represents the relay tripping time in sec whereas x-axis represents the fault current (I_{sc}) in Amp. Each curve shows the fixed values of the I_p settings. For a given I_p, if the magnitude of fault current I_{sc} increases, the trip-time decreases.

Therefore, the I_p setting of the OCR within the MG is an important parameter for the faithful operation of the MGs. Since, there are two modes of operation viz. grid-connected and islanded mode, during any abnormality the maximum fault current in grid-connected mode is higher than that of the islanded mode of operation. Also, MG consists of inverter-interfaced DGs viz. solar and wind. During any abnormality, the contribution of the fault current in power electronics based DGs is ~1.5-2 times lower than that of rotating machine based DGs [154]. The detail discussion for the computation of the relay tripping time is given in Section 2.2 of Chapter 2.

Figure 6.2 shows the adaptive relaying feature of the developed CAAR. In this figure, y-axis represents the relay operating time whereas x-axis represents the threshold current *Ip*. The *Ip1* and *Ip2* are the settings of the CAAR for grid-connected and standalone mode of operation respectively. The threshold current settings are changed within the CAAR, when the MG start working in standalone mode after being disconnected from the utility grid. The magnitude of the pick-up current changes between *Ip1 to Ip2* as per the operating modes of the MG.

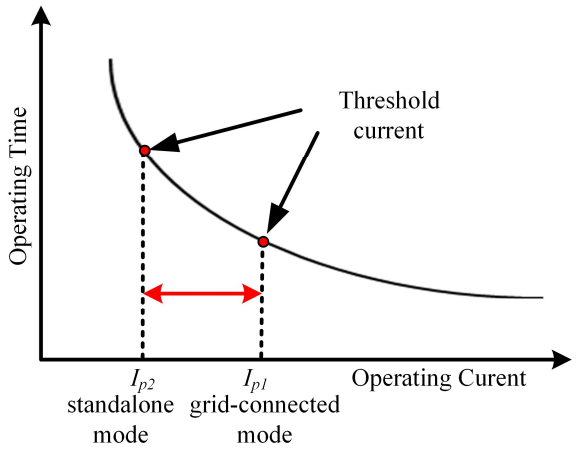

Figure 6.2 Adaptive relaying principal

6.2.2 Signal Conditioning Module

In this module, the output of CT and VT are processed and the output of this module is given to the ADC. The bipolar output of the CT and VT are made compatible with the unipolar ADC having input range 0-5V with the help of the dc-offset module. The dc-offset module is developed using various active and passive components viz. operational amplifier (op-amp) and resistors. The magnitude of the offset is fixed at 2.5 V for the sampling of the sinusoidal input signals having peak-to-peak value 5V. A passive LPF with cut-off frequency of 200 Hz is also designed with the dc-offset module that is used to remove the higher frequency components beyond 3^{rd} harmonic and any spurious noise present in the input signal.

6.2.3 Analog to Digital Converter

In developed CAAR, analog signal is converted to digital data (10-bits) using on-board microcontroller (µC), ATmega-328 of Arduino board [155]. ATmega-328 is a 8-bit AVR family µC having reduced instruction set computer (RISC) processor core [156]. The detectable input range of on-board ADC is from 0 to 5.0 V. A 2.5 V dc-offset is used to sense the bi-directional input having the maximum swing of 5V (P-P) received from the CT/VT. Resolution and the maximum possible sampling frequency of the ADC are 4.9 mV and 9.615 kHz respectively. The output data of the ADC is transmitted through the wireless channel that is received by another Wi-Fi module of the CCU.

6.2.4 Wi-Fi Module

The output data (10-bit) of the ADC is transmitted through the nRF24L01 wireless module [157]. The data is received by CCU of the FPGA development board through a level shifter with the help of Rx of the Wi-Fi module. After processing the data, the trip signal is transmitted

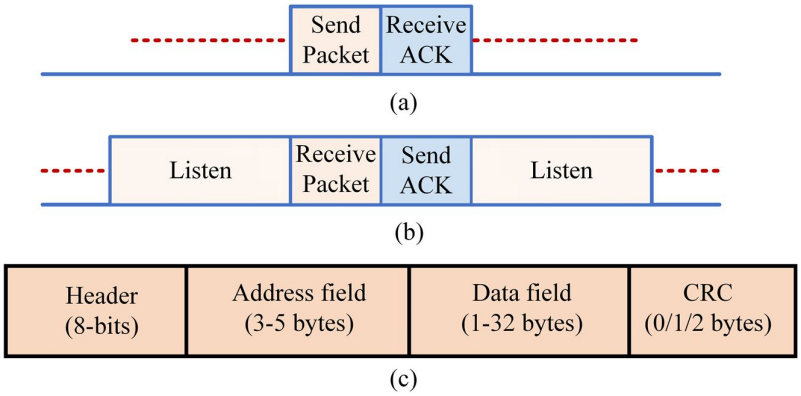

Figure 6.3 Enhanced ShockBurst protocol engine

(a) Operation in PTx (b) Operation in PRx (c) Data Packet

to the CB using Tx of the Wi-Fi module. The nRF24L01 is a low-cost system-on-chip (SoC) wireless transceiver/Wi-Fi module, which is operated in the Industrial, Scientific and Medical (ISM) band with operating frequency of 2.4GHz. The Wi-Fi module is programmed by using the Arduino Integrated Development Environment (IDE) through Serial Peripheral Interface (SPI). A printed circuit board (PCB) antenna is mounted on it, which is used to communicate (transmitting and receiving) the data between different channels of the Wi-Fi module. The data is communicated effectively between two modules under 100 meters (~300 feet). These Wi-Fi modules are operated at 3.3 V which makes it compatible for FPGA interfacing. The module is designed to operate for very high-speed communications (up to 2Mbit/s). The Wi-Fi module consists of a power amplifier, a frequency synthesizer, crystal oscillator, modulator, demodulator and Enhanced ShockBurst (ESB) protocol engine. One Wi-Fi nodule can communicate with six other communicating modules and each module has 125 different address/channels.

The Wi-Fi module is configured and operated by using the SPI interface. The module support embedded ESB baseband protocol, which is used for two way data communication that includes buffering, acknowledgement and automatic retransmission of lost data packets. Communication of the data packet between two modules takes place by considering one transceiver as the Primary Transmitter (PTx) and the other transceiver as the Primary Receiver (PRx) [158]. The operation of the PTx and PRx are shown in Figure 6.3*a* and Figure 6.3*b*. The transmission of the data packets is initiated from PTx and successfully completed after receiving an acknowledgement (ACK) packet from PRx. Figure 6.3*c* represent the data packet of the ESB protocol that consists of a header, address field, data fields and cyclic redundancy check (CRC) for error correction.

6.2.5 Control Unit Developed on FPGA Hardware

Here, at first, fundamental and second harmonic components of the input signals are extracted using a Discrete Fourier Transform (DFT). After that RMS of the extracted fundamental component and harmonic component are computed using Xilinx IP-LogiCORE (V4.0 IP core), which are further used by the relay emulating module (REM). Thereafter, the computation of the harmonic distortion (HD) is performed that is an essential feature of the OCR, as it makes the relay immune to inrush or input surge current. Details of the design of DFT, REM and HD modules are explained in Section 2.3 of Chapter 2.

Later, directional feature is introduced by using the zero crossing detector (ZCD) module, where the phase angle between voltage and current is computed [159]. The ZCD module operates once for every packet (10-bit digital data) of incoming data. In this module, each sample received from the ADC is compared with the fixed value (512), which is the digital equivalent of the dc-offset used in the design. If the digital value of the sample exceeds the predefined equivalent value of the offset, the output signal of ZCD toggles to 1. When the above condition does not satisfy then ZCD module produces 0. Thus, a square wave signal is generated by the ZCD module for every cycle of the input signal (current and voltage). The difference between each cycle of the two square waves is used to identify the direction of fault by the phase detector (PD) module. A detail discussion of the design of ZCD and PD modules is given in Section 3.3 of Chapter 3

6.3 Flow Chart of the Developed Protection Scheme

The structure of the design flow is shown in Figure 6.4. At the beginning of the algorithm, various parameters viz. A, B, p, TDS, T_r, and N_T, are initialized with the pre-set values 4096, 64, 1, 64, 6.4×10^6, 1, 1, 5, and 50 respectively. Voltage and current through the CT and PT are measured at the terminal of the PCC, DGs and RESs. The analog current and voltage signals are taken out from the GTAO card of the RTDS. Thereafter, these signal are processed by the DC-Offset and low-pass filter modules. The filtered signal is converted to 10-bit data and given to the FPGA using ADC. The digital data are transmitted to the control unit (developed on FPGA) through the Wi-Fi module installed at the terminal of the PCC, DGs and RESs. The computation for I_{RMS}, *HD*, *ZCD*, phase, and relay tripping time has been performed in the control unit of the FPGA. A DFT is used for the extraction of the fundamental and second harmonic component of the input signal. Status of the CB1 (at PCC) is transmitted through the Wi-Fi module. When CB1=0, MG operates in the grid-connected mode and the I_p setting of the OCR is updated as $I_p = I_{p1}$. Else for CB1=1, MG operates in standalone/islanded mode and the

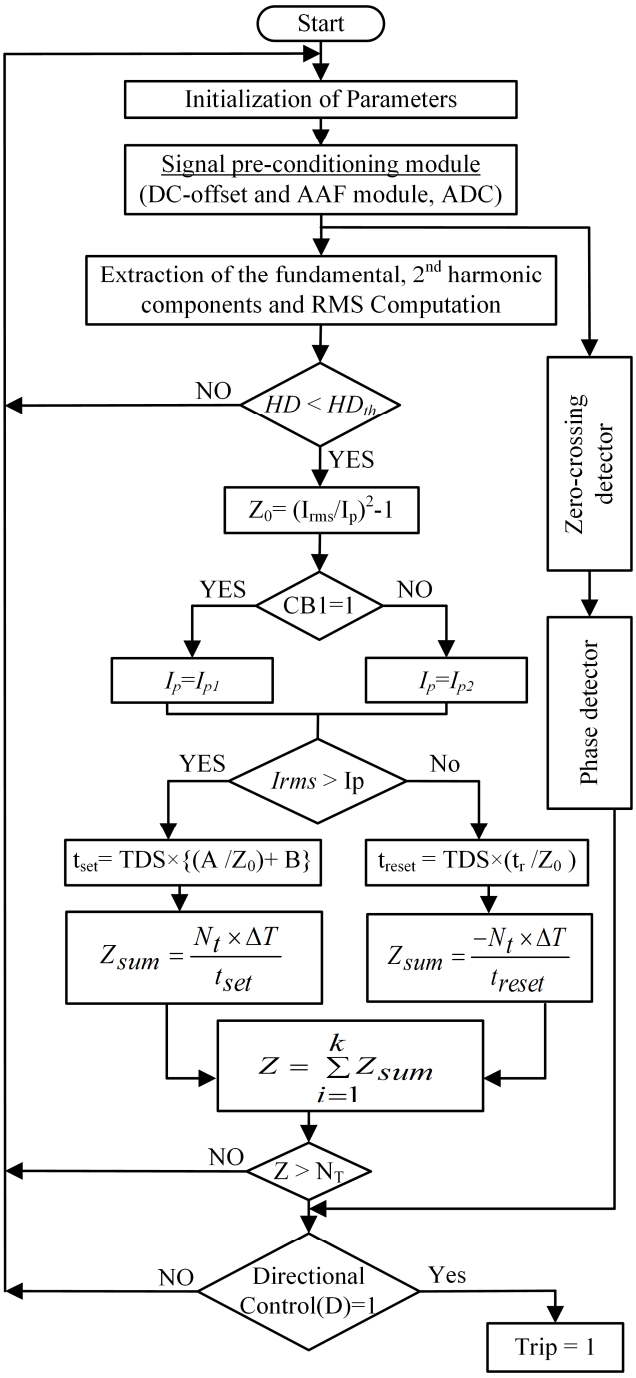

Figure 6.4 Flow-chart of the proposed relay prototype

I_p setting of the OCR is updated as $I_p = I_{p2}$. Zero crossings of the voltage and current signal are computed using the ZCD module, which is used for the computation of the phase between voltage and current. The Directional control signal (D) is generated by the phase detector module which represents the forward and reverse direction of the current flowing through the network. D=1 represents forward, whereas D=0 indicates the reverse direction of current flow. After the initialization, RMS value of the current is calculated and used for the computation of

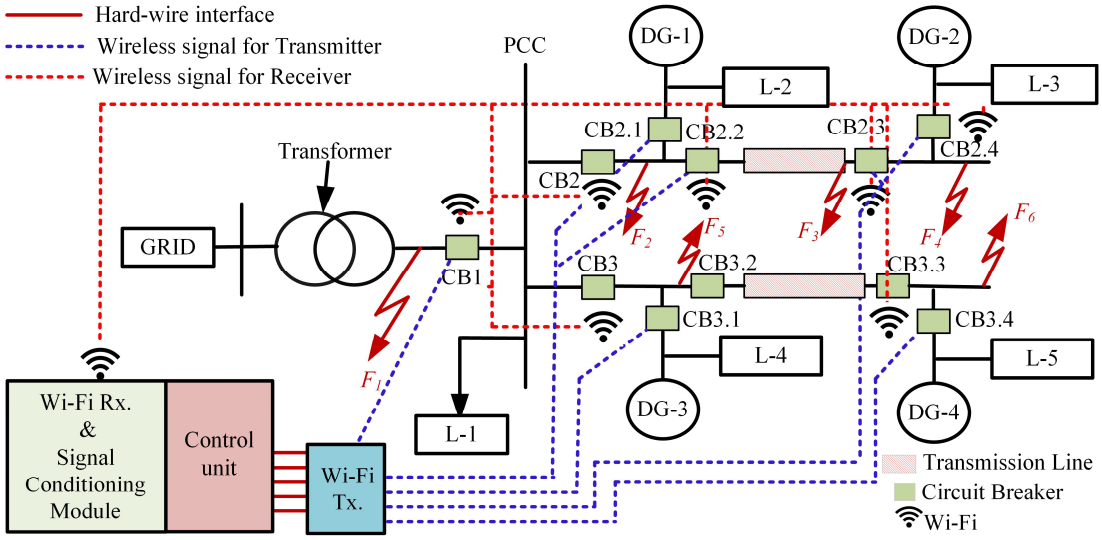

Figure 6.5 Layout of the Microgrid test system with control strategy

set and reset time of the OCR. At the arrival of the RMS values of current, summation $\sum(Zsum)_i$ is increased or decreased by the amount Z_{sum} when $i_{rms} > I_p$ or $i_{rms} < I_p$ respectively. The updated value of $\sum Z_i$ is compared with N_T at every positive edge of the clock. The *trip* signal is generated when $\sum Z_i$ is greater than N_T *and* $D=1$. The status of the *TRIP* signal is transmitted from the control unit through the Wi-Fi module and opens the respective CB.

6.4 Test System and Hardware-in-loop Verification

6.4.1 Microgrid Test System Developed in RTDS

A MG test system consists of DGs and RESs is modelled in the RTDS as shown by Figure 6.5 [140]. This MG includes two synchronous generators, a solar farm, a wind farm, five local loads and two transmission lines. The MG is connected to the main grid through PCC. The operating mode of the MG is defined by the status of the circuit breaker *CB1* placed at PCC. When the status of the *CB1*=1, MG works in standalone/islanded mode and for *CB1*=0 it operates in grid-connected mode. Wi-Fi modules (nRF24L01) are placed at *CB1*, *CB2*, *CB3*, *CB2.2, CB2.3, CB2.4* and *CB3.2,* which are used to transmit and receive the control signal from the control unit over the wireless network. The output of the CT, PT and status of the CB are transferred to the control unit through a wireless network shown in Figure 6.5 as red and blue colored dotted lines. These OCRs have two I_p settings, one for grid-connected and another for the islanded mode. The *TRIP* signal generated at the control unit is transferred to the specific CB through the transmitter of the Wi-Fi Module located at the control unit. The value of parameters of the MG test system is given in [154].

6.4.2 Experimental Setup

An experimental setup for HIL testing of communication assisted adaptive relay is illustrated by Figure 6.6. RTDS, DC-offset module, LPF, ADC and FPGA are the main components of the setup. The MG shown in Figure 6.5 is modelled and simulated in RTDS while the proposed algorithm of the adaptive relay is targeted on the VIRTEX®5 (XC5VLX50T-3FF1136) FPGA. Implementation of the algorithm has been done on the targeted FPGA hardware by Verilog HDL with the help of the Xilinx Integrated Synthesis Environment (ISE) 12.4 and ISE simulator (Isim) design tool. A centralized control unit designed on the FPGA internally updates the settings of the pick-up current as per the operating mode of the MG. The current and voltage output signals of the CT and PT respectively are taken out from GTAO card of the RTDS. These signals are scaled down to 5 V (P-P) by the GTAO card to communicate with developed FPGA chip. The output of the GTAO card is given to the DC-Offset module (offset value= 2.5V) which makes the input signal compatible to the ADC of Aurdino-uno. A LPF is placed between DC-Offset and ADC module to cancel any noise introduced during the processing of the analog signal. The ADC outputs 10-bit data, which is further provided to the Wi-Fi modules (ESP-01, ESP 8266) as shown in Figure 6.5. These modules are used to transmit 10-bit output and also receive 1-bit data. After receiving the packet of 10-bit data from the Wi-Fi module, various computations are performed on the FPGA. After processing the data, status of *CB1* is checked, if *CB1*=0, I_p is updated as I_{P1} otherwise it is updated as I_{p2}. Also, if conditions for tripping of the developed relay are satisfied, a *TRIP* signal is generated and is taken out from the FPGA and transmitted through the Wi-Fi module. Thereafter, this signal is received by the Wi-Fi receiver placed at the GTDI card and is given to the targeted CB of the RTDS.

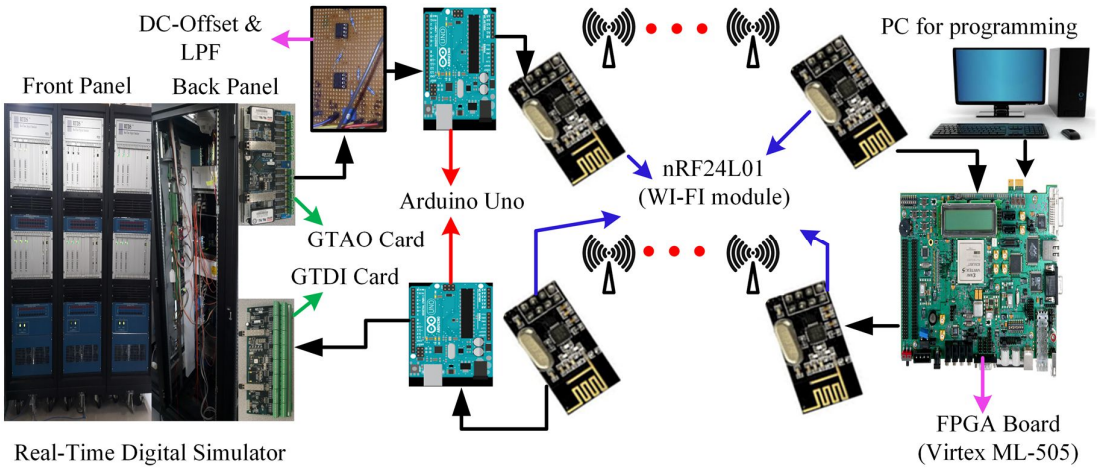

Figure 6.6 Hardware set-up for HIL verification

6.5 Results and Discussion

In this section, various test conditions for verification of the designed CAAR are discussed. Different types of faults i.e. line-to-ground (LG) fault, line-to-line (LL) fault and line-line-line-ground (LLLG) fault are incepted at different locations i.e. F_1, F_2, F_3, F_4, F_5 and F_6, as shown in Figure 6.5, for real-time hardware in loop testing of the designed relay.

6.5.1 Effect of Operating Mode of MG on Relay

Here, the effect of the fault current on the designed CAAR under different operating modes of the MG is discussed.

Case-I: Grid-connected mode of operation

In this case, the performance of the relay is tested for CB2 under EI characteristics. Here, the settings of the relay are 1 and 0.5 A respectively for TDS and I_p. The obtained results are shown in Figure 6.7. The currents flowing through the breaker and the output terminal of the CT are shown in Figure 6.7*a* and Figure 6.7*b* respectively. The operating mode of the MG is represented by signal *MODE* in blue color as shown in Figure 6.7*c*. If *MODE*=1, then MG operates in the grid-connected mode of operation, else if *MODE*=2 it operates in the standalone mode. Here, *MODE=1*, the MG operates in the grid-connected mode. The status of the CB, incepted fault and generated trip signal is shown in Figure 6.7*d,* Figure 6.7e and Figure 6.7f

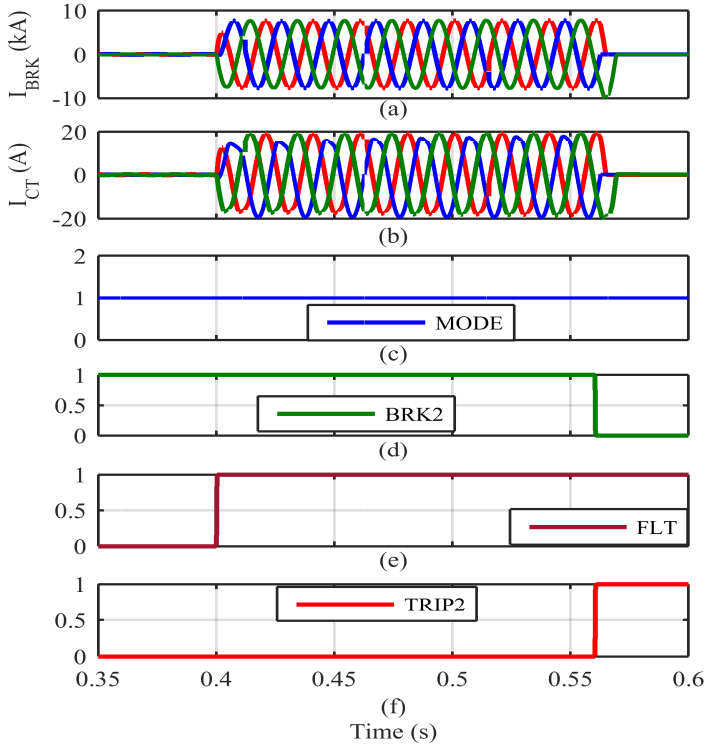

Figure 6.7 Test results for grid-connected MG when fault is incepted at F_2

respectively. The status of BRK i.e. BRK2=1, represent the status of CB2 in 'CLOSE' state whereas for BRK2=0, the CB2 'OPEN' state. *FLT*=1 shows the fault is incepted whereas *FLT*=0 represents the normal operating condition.

A LLLG fault is incepted at location F_2 at t=0.4003 sec. The magnitude of the fault current through the CB is observed as 7.84 kA after the inception of the *FLT* as shown in Figure 6.7*a*. After passing this current through the CT, its magnitude at the output terminal becomes 19.56 A as shown in Figure 6.7*b,* which is given to the ADC of the Arduino through the GTAO cards of the RTDS. Here, this signal is converted to 10-bit digital data fed to FPGA (CCU) through the Wi-Fi modules. Now, various pre-defined conditions are checked for generating the trip signal. Here, the status of the CB2 is updated through *TRIP2* signal. The status of the *TRIP2* signal becomes '1' from '0' at t= 0.5606 sec as shown in Figure 6.7*f*. At the same instant, CB2 opens and shown in Figure 6.7*d*. Hence, the relay tripping time is 0.1603 sec (interval between fault inception and opening of CB2).

Case-II Islanded mode of operation

In this case, the operation of the relay under the islanded mode of MG is tested and the observed results are shown in Figure 6.8. The signals monitored are *MODE*, *BRK2*, *FLT* and *TRIP2* which are defined in the above sub-section. Here also, the EI-characteristics of the relay is considered and a LLLG fault is incepted at location F_2 at t=0.4003 sec as shown in Figure 6.8*e*. The threshold settings I_{p2} is 0.25 A, which is relay settings for islanded mode of operation and is confirmed by the continuously monitored the signal *MODE* i.e. *MODE*=2 as shown in

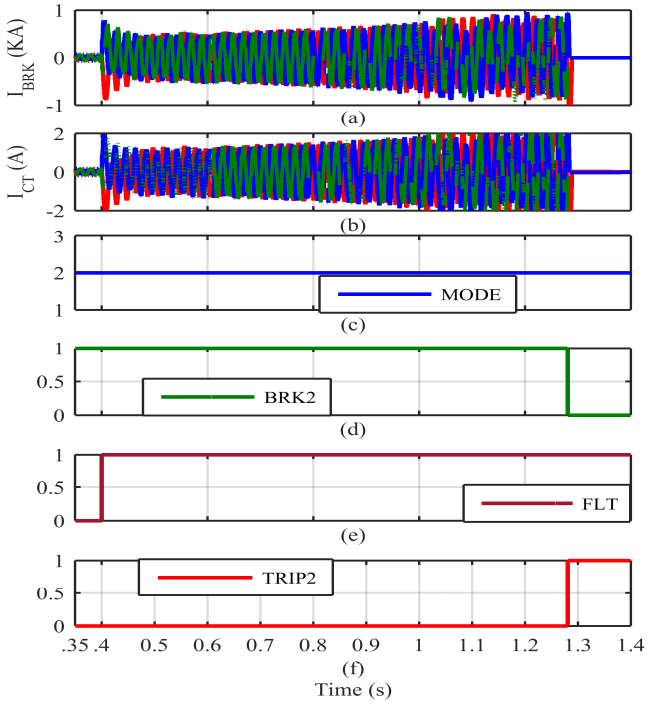

Figure 6.8 Results for islanded MG when fault incepted at F_2

Figure 6.8*c*. Here, after fault inception, it is observed that the magnitude of fault current is decreased drastically with respect to grid-connected mode i.e. from 7.84 kA to 0.955 kA shown in Figure 6.7*a* and Figure 6.8*a* respectively. Thereafter, the current is scaled down by CT to 2.37 A as shown in Figure 6.8*b*. Due to this decreased amount of fault current, signal *TRIP2* is generated at t=1.281 sec that is sent to open CB2 and change its status from '1' to '0'. The observed trip time is 0.8807 sec.

6.5.2 Mode Adaptability of Developed Relay

In this case, the performance of the developed relay in terms of adaptive feature is tested. Threshold settings of the relay are predefined i.e. I_p= 0.50 A for grid-connected mode and I_p= 0.25 A for standalone operation. The status of the signal *MODE* is updated by CB1 that is placed at the PCC through the transmitter and receiver Wi-Fi modules. Once the CB1 opens, the status of the signal *MODE* changes from '1' to '2', which signifies the working mode of the MG. Here, a LLLG fault F_2 is incepted at t=0.4001 sec as shown in Figure 6.9*e*. The magnitude of the current flowing through the CB1 is 17.87 kA and the CT1 is 19.63 A given in Figure 6.9*a* and Figure 6.9*b* respectively. Here, *TRIP1* signal is generated at t=0.5592 and at the same instant the status of mode is changed from '1' to '2' as shown in Figure 6.9*f* and Figure 6.9*c* respectively. Now, at this instant, CB1 is opened due to which the MG shifts from grid-connected to the standalone mode of operation.

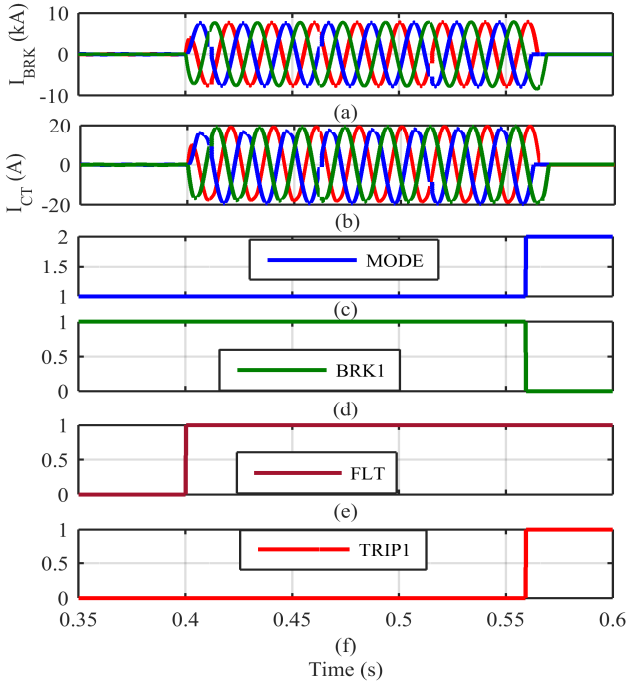

Figure 6.9 Operation of the OCR for mode adaptation

6.5.3 Testing for Relay Coordination

In this case, the coordination between relays i.e. R-1 and R-2 placed at *CB2.2* and *CB2.3* on both ends of the transmission line as shown in Figure 6.5 and results are shown in Figure 6.10. Here, EI characteristics of developed OCR has been considered to verify the relay coordination by incepting a LLLG fault at location F_3 at time t=0.4003 sec as shown in Figure 6.10*c*. The threshold (I_p) setting for R-1 and R-2 are 0.5*A* and 0.15*A* respectively for the grid-connected operation. The magnitude of the measured fault current through the BRK2.2 and BRK2.3 are 1.47 kA and 0.1479 kA given by Figure 6.10*a* and Figure 6.10*b* respectively. For both the CTs, output current exceeds their Ip settings. However, only for CB 2.2, the condition for direction i.e. *D=1* is met. Hence, a trip signal *TRIP8* is generated at t=0.9806 sec shown in Figure 6.10*e* for CB 2.2 by the breaker signal *BRK8* shown in Figure 6.10*d*. The tripping time of the OCR is 0.5803 sec. The status of signals *BRK9* and *TRIP9* are not changed since the condition of tripping i.e. direction *D=0* is not satisfied.

In addition to this, a comprehensive set of test cases i.e. different types of fault at different locations as discussed in this section have also been considered to evaluate the performance of the developed relay and the results are reported in Table 6.1. These results suggest the effectiveness of the developed OCR for protection of MGs for different modes of operation.

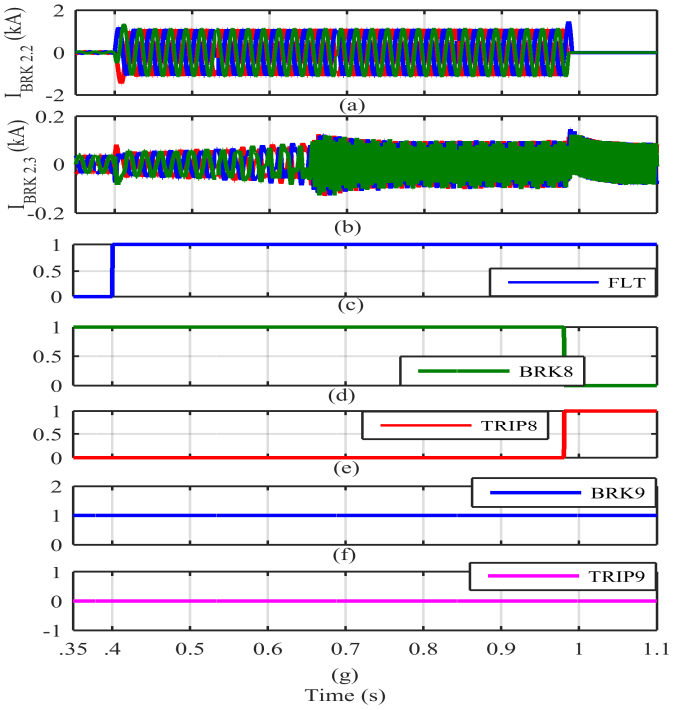

Figure 6.10 Results for relay coordination for fault at F_3

Table 6.1 Testing of the relay performance under different fault conditions

Flt		*MODE*	*FLT (incepted)*	I_F*(Max) In Amp*	*TRIP signal (generated)*
Type	*Location*				
LG	F_1	Grid-connected	at, t=0.401s	7.538A I_p=0.50A	CB1, opens at=0.802s
	F_2	islanded	at, t=0.405s	2.339A I_p=0.25A	CB2, opens at=1.385s
	F_2	Grid-connected	at, t=0.406s	16.97 A I_p=0.50A	CB2, opens at=0.575s
	F_4	islanded	at, t=0.405s	2.65 A I_p=0.25A	CB2, opens at=1.110s
LLG	F_2	Islanded	at, t=0.402s	2.62A I_p=0.25A	CB2, opens at=1.103s
	F_1	Grid-connected	at, t=0.408s	7.870A I_p=0.50A	CB1, opens at=0.767s
	F_5	Islanded	at, t=0.402s	2.47A I_p=0.50A	CB2, opens at=1.825s
	F_4	Grid-connected	at, t=0.000s	3.139A I_p=0.50A	CB2, opens at t>2s
LLLG	F_1	Grid-connected	at, t=0.405s	1.21A I_p=0.50A	CB1, opens at t>2s
	F_2	Grid-connected	at, t=0.4001s	7.878A I_p=0.50A	CB1, opens at=0.559s
	F_2	Islanded	at, t=0.4001s	0.955A I_p=0.25A	CB2, opens at=1.281s
	F_3	Grid-connected	at, t=0.4003s	3.65A I_p=0.50A	CB2.2,opens at t=0.980s

6.6 Summary

In this chapter, a communication assisted adaptive relay is discussed for the protection of the MG having different types of DGs. The relay is implemented on the FPGA (XC5VLX50T-3FF1136) using Verilog HDL that reduces the computational burden and onboard resource utilization. This helps to achieve faster operation. Here, the status of the CB is updated at the central controller through the transmitter and receiver of the Wi-Fi module. The mode adaptability feature of the relay settings is also introduced to effectively use the same relay under two operating mode of the MG. This provides an edge over the existing conventional overcurrent relays to be used with MGs. The operation of the proposed relaying technique has been verified using hardware-in-the-loop with RTDS, FPGA board and wireless communication (Enhanced ShockBurst protocol) nRF24L01 modules. A comprehensive test cases for fault current under different operating modes of MG, adaptability in pick-up setting and relay coordination are performed. The results obtained suggest the developed relay is capable to work satisfactorily under different operating modes of MG.

CHAPTER 7: CONCLUSION AND FUTURE WORK

7.1 Conclusion

The work reported in the present thesis covers the design of a protection relay with multiple features i.e. islanding detection and communication feature for mode adaptation using Verilog HDL. The integer arithmetic calculations of the relay are performed using HDL that improves the overall computational efficiency and on-chip resource utilization. The FPGA based OCR prototype has the features of re-configurability i.e. modifications can be accommodated by re-programming. The proposed relays are developed on Virtex ML-505 FPGA development board and tested in real-time simulation environment viz. HIL with RTDS.

In **Chapter-2,** a detailed discussion of the OCR prototype developed on FPGA is presented. The internal design of the OCR and various sub-modules, i.e. analog-to-digital converter (ADC), discrete Fourier transform (DFT), root mean square (RMS) module, harmonic distortion (HD) module are discussed. Signal pre-conditioning has been carried out to mitigate any potential noise present in the input (actuating current) signal. The experimental setup for HIL testing of the prototype has been discussed for both the characteristics and operational verification of the OCR. This OCR prototype can differentiate the inrush current from the fault current, due to which nuisance tripping of the relay can be avoided.

In **Chapter 3**, prototype of a DOCR which includes both directional and inverse characteristics of an OCR has been discussed, with the addition of the directional feature. An efficient design for the directional logic is also introduced with the OCR by using a simple zero-crossing detector module. The proposed DOCR is flexible for variable I_P and TDS. Signal conditioning module has been developed to mitigate various spurious noise present in the actuating signal. This DOCR are suitable for protection of MGs where bidirectional power flow occurs.

In **chapter 4**, an IDT algorithm based on the periodic maxima of superimposed voltage components has been proposed. In this method, an IDF is computed to distinguish the islanding and non-islanding events accurately. Also, it is able to identify the MGs' normal operation as a lower bound of IDF is selected that prevents any maloperation. Various test conditions viz. different active power unbalance and critical non-islanding events have been considering for the performance verification of the proposed method. The proposed design can detect the islanding condition even in perfect power balance condition.

In **chapter 5**, the prototype of a hardcore multifunctional relay is designed on a reconfigurable FPGA, which is not only used for islanding detection but also caters further protection issues i.e. mode adaptation. The proposed IDT incorporates the advantages of IDTs viz. ROCOF and VU. Along with it, an OCM is also incorporated to facilitate the mode adaptation feature that updates the settings of the OCR placed at the active DGs terminal, when the islanding is done.

In **chapter 6**, a DOCR is developed in FPGA platform aided with directional and communication features for the adaptive setting of the threshold current that is updated as per the operating mode of the MG. The impact of the fault current on the MG protection due to DGs and the operating modes of the MG is presented. An MG test system is designed in RTDS to verify the operation of the relay. A complete testbed is developed which includes Enhanced ShockBurst protocol based wireless infrastructure for HIL testing of the relay.

7.2 Future Scope of the Research Work

- The present modular design of relays using HDL gives the direction to develop a library of power system protection components in the form of HDL modules. This developed module can be used for producing a tailor-made solution for customized problems.
- Although the proposed prototype has been experimentally validated in the power system laboratory, further tuning on the hardware and software sides may be required for future design. In addition, the design algorithm and methodology can be implemented in the actual industrial power system in the future.
- Utilization of hardware resources can be reduced by optimizing the algorithm by using the concept of pipelining.
- Furthermore, the proposed relay prototype can also be tested for reconfigurable MGs i.e. interchanging network connections viz. radial, ring and meshed type. Here, the mode adaptability in the presence of different types of DGs can also be considered.
- Reverse power flow analysis can also be studied for the developed relay prototype.
- Timing analysis and the communication delays associated with the proposed relay can be studied.
- The present thesis primarily focused on the relaying and adaptive protection of MG. The work can be extended for other possible application in the power system.

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LIST OF PUBLICATIONS

International Journals:

1. **Praveen Kumar**, Vishal Kumar and Rajendra Pratap, "Prototyping and Hardware-in-loop Verification of OCR", *IET Generation, Transmission & Distribution*, Vol. 12, no. 12, pp. 2837-2845, Mar.2018.
2. **Praveen Kumar**, Vishal Kumar and Rajendra Pratap, "Design and Verification of Hardcore Reconfigurable Relay for Islanding Detection and Subsequent Mode Adaptation of Microgrid", *Int. Trans. Electr. Energ. Syst*., 2019;e2807.
3. **Praveen Kumar**, Vishal Kumar and Rajendra Pratap, "FPGA Based Design and HIL Verification of a Soft-core Directional-OCR", *in Electric Power Components and Systems*. (**Accepted on July 30, 2019**)

International Conferences:

4. **Praveen Kumar**, Vishal Kumar, Rajendra Pratap, "Digital Design and Implementation of an Overcurrent Relay on FPGA", In 14th IEEE India Council International Conference (INDICON), pp. 1-5, Dec. 2017.
5. **Praveen Kumar**, Vishal Kumar, Rajendra Pratap, "Design and Implementation of Phase Detector on FPGA", In 6th IEEE International Conference on Computer Applications in Elect. Eng. Recent Advances (CERA), pp. 108-110, Oct. 2017.
6. **Praveen Kumar**, Vishal Kumar, Rajendra Pratap, "Rate of Change of Frequency Deviation Based Unintentional Islanding Detection for Microgrids", In IEEE Inter. Con. on Control, Power, Communication and Computing Tech. (ICCPCCT), Mar. 2018.
7. **Praveen Kumar**, Aishwarya Mittal, Kakarla U.K Reddy, Shubham Chowdhary, Vishal Kumar, Rajendra Pratap, "Design and Verification of Three Phase Sequence Decomposer on Re-configurable Hardware", In 10th IEEE Inter. Conf. on Computing, Communication and Networking Technologies (ICCCNT), Kanpur.

APPENDIX

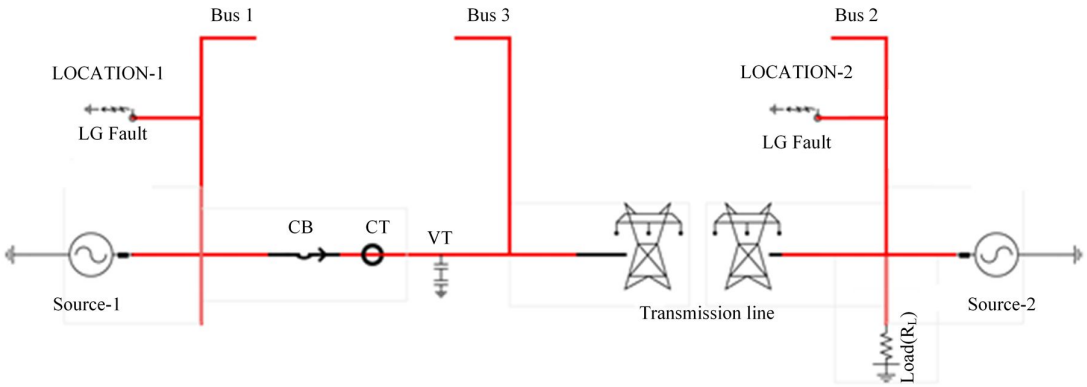

Figure A. 1 Parameters of the test module

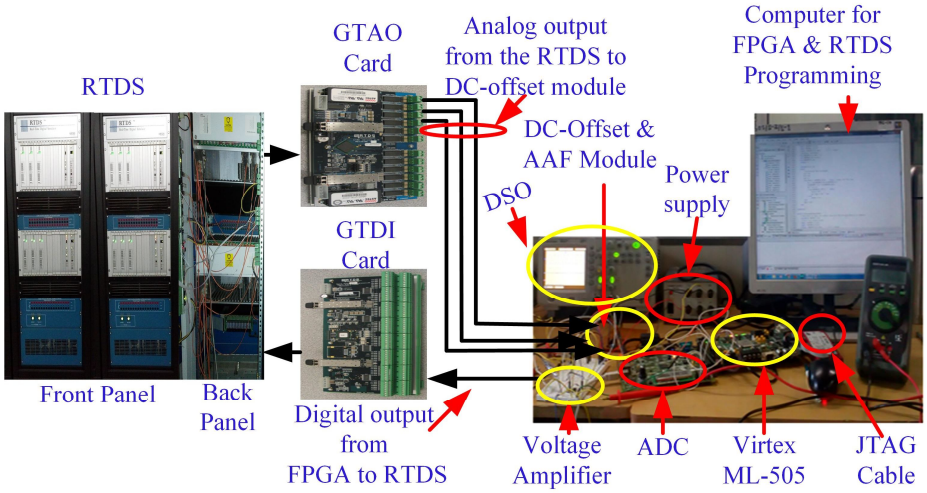

Figure A. 2 Hardware set-up for HIL-verification

Table A. 1 Parameters of the test module

Source parameters
Z_1=0.5278 ∠87.18 Ω, Z_2=5.27884 ∠87.18 Ω, Frequency=50 Hz
Distribution line parameters
Positive sequence parameters: Series resistance (R_s)= 0.018747 Ω/km, Series inductive reactance (X_{Ls})= 0.37661 Ω/km, Shunt capacitive reactance (X_{Cs})= 0.22789 MΩ-km Zero sequence parameters: R_s =0.3618376 Ω/km, X_{Ls}=1.227747 Ω/km, X_{Cs}=0.34513 MΩ-km
CT parameters
Burden series resistance=1.5 Ω, Burden series inductance=35 mH, Secondary side resistance = 0.5 Ω, Secondary side inductance=0.8 mH, Turn ratio=380:1
Impedance=529 Ω

Table A. 2 Parameters of the test module

Grid Parameter
Rated line-to-line voltage (RMS) = 138 kV, and
Transmission line parameters: PI section , Rated frequency = 60 Hz.
Positive sequence parameters: Series resistance (R_p) =0.0173 Ω/km, Series inductive reactance (X_p) =0.4317 Ω/km, Shunt capacitive reactance (X_{cp}) =0.005036 MΩ-km. Zero sequence parameters: Series resistance (R_z)=0.350 Ω/km, Series inductive reactance (X_z)=1.7986 Ω/km, Shunt capacitive reactance(X_{cz})=0.012285 MΩ-km
Solar energy
Rated solar (PV) power = 1.75 *MW*, No. of cells in series/module = 36, No. of cells string in parallel = 1, Open circuit voltage = 21.7 *V*, Short circuit current = 3.35 *A,* Voltage at maximum power = 17.4 *V*, Current at maximum power = 3.05 *A*, No. of modules in series = 115, No. of modules in parallel = 285, Nominal temperature = 25 ^oC, Rated solar intensity = 1000 W/m^2.
Wind Turbine
Rated power = 2.2 *MVA*, Rotor/Stator turn ratio = 2.6377, Inertial constant (H) = 1.5 *MWs/MVA*, Air density (kg/m^3)= 1.2 kg/m^3, Rated wind speed= 13 *m/s*, Rated frequency=60 Hz.
First cage rotor resistance = 0.006, Stator resistance = 0.00462, Unsaturated magnetizing reactance = 4.384, Stator leakage reactance = 0.102, First cage rotor leakage reactance = 0.08596 (all values are in per unit).
Diesel generator parameters
Rated line-to-line voltage = 4 kV, Base angular frequency = 60 rad/sec, ,Rated MVA= 5 No. of q-axis rotor winding=2 Machine electrical data: Xa= 0.130 p.u, Xd=1.79 p.u, Xd'=0.169 p.u, Xd''=0.135 p.u, Xq=1.71 p.u, Xq'=0.228 p.u, Xq''=0.2 p.u, Ra= 0.002 p.u, Tdo'=4.3 sec, Tdo''=0.032 sec, Tqo'= 0.85s, Tdo''=0.05s. Machine zero sequence impedances: Mrzo = 0.002 p.u, Mxzro = 0.132 p.u, Rneut = 1.0 × 105 p.u, Xneut = 0 p.u

Table A. 3 Parameters of the test module

Grid Parameter
Rated line-to-line voltage (RMS) = 230 kV, and Frequency = 50 Hz,
Transmission line parameters: PI section , 10 km each, rated voltage= 25 kV
R_p=0.018747 Ω/km, X_p=0.37661 Ω/km, X_{cp}=0.22789 MΩ-km, R_{pz}=0.1153 Ω/km, X_{pZ}=0.3298 Ω/km, X_{cZ} Shunt=2809.4 MΩ-km.
Solar energy
Rated solar (PV) power = 1.75 MW, No. of cells in series/module = 36, No. of cells string in parallel = 1, Open circuit voltage = 21.7 V, Short circuit current = 3.35 A, Voltage at maximum power = 17.4 V, Current at maximum power = 3.05 A, No. of modules in series = 115, No. of modules in parallel = 285, Nominal temperature = 25 ^oC, Rated solar intensity = 1000 W/m^2.
Wind Turbine
Rated power = 2 MW, Rotor/Stator turn ratio = 2.6377, Inertial constant (H) = 1.5 MWs/MVA, Air density (kg/m^3)= 1.2 kg/m^3, Rated wind speed= 13 m/s.
Rotor resistance = 0.006, Stator resistance = 0.00462, Magnetizing reactance = 4.384, Stator reactance = 0.102, Rotor reactance = 0.08596 (all values are in per unit).
Synchronous generator parameters
Rated line-to- line voltage (Gen_1) = 0.575 kV, Rated line-to- line voltage (Gen_2) =0.400 KV, Base angular frequency = 50 rad/sec, H = 4.7 MWs/MVA, ,Rated MVA= 5. Machine electrical data: X_a= 0.2327 p.u, X_d=1.7134 p.u, $X_{d'}$=0.4345 p.u, $X_{d''}$=0.3253 p.u, Xq=1.6424 p.u, Xq'=0.6168 p.u, Xq''=0.3253 p.u, R_a= 0.002 p.u, Tdo'=6.174 sec, Tdo''=0.032 sec, Tqo'= 0.388s, Tdo''=0.047s. Machine zero sequence impedances: Mrzo = 0.002 p.u, Mxzro = 0.2327 p.u, R_{neut} = 1.0 × 10^5 p.u, X_{neut} = 0 p.u Exciter parameters: Voltage regulator time constant (Ta)= 0.02 sec, AVR lag time constant(Tb)= 20 sec, AVR lead time constant(Tc)= 1 sec, voltage regulator gain= 200, Regulation factor of excitation system= 0.175.
Constant Loads (L_2, L_3,L_4 and L_5) = 8MW & 3 Mvar