MODELING, ANALYSIS AND CONTROL OF NON-ISOLATED DC-DC CONVERTERS

Ph. D. Thesis

by

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled "**MODELING, ANALYSIS AND CONTROL OF NON-ISOLATED DC-DC CONVERTERS"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electrical Engineering of the Indian Institute of Technology Roorkee, Roorkee, is an authentic record of my own work carried out during a period from July, 2014 to May, 2019 under the supervision of Dr. Yogesh Vijay Hote, Associate Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institution.

(VISHWANATHA SIDDHARTHA)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

(Yogesh Vijay Hote)
Supervisor

Date:

ABSTRACT

The switched mode converters grow to be popular, because of its vast applications in different fields. These are having applications mainly in micro-grid, renewable energy power generation, battery charging, power supplies, LED drivers, aero-space equipment, drives applications etc. Different applications require their individual set point voltage levels according to the requirement. Depending on the applications, various DC-DC converters have been utilized to step up/down the regulated DC voltage from the unregulated DC voltage. In practice, buck, boost and buck-boost converters are the most commonly used DC-DC converters for step down/up applications. Here, the accurate design analysis of these converter systems is very important. This is main motive to work on detailed analysis, accurate modelling and control of non-isolated DC-DC converters.

Overall, DC-DC converters can be classified as buck and boost type. In this work, the basic non-isolated DC-DC converters such as boost, buck-boost and NIBB (Non-inverting buck-boost) are mainly considered for analysis in different aspects. All major non-idealities of the converter system are considered such as equivalent series resistances (ESR) of filter elements (inductor, capacitor), resistances of input supply, semiconductor switches and diode forward drop voltage. Overall, thesis can be viewed as two parts, first part concentrates on design, modelling analysis of DC-DC converters and second part focuses on their controller design.

The first part mainly concentrates on power electronic related issues like design, modelling and analysis. This includes improved or accurate expressions of duty cycle, inductor and capacitor for non-ideal boost, buck-boost and NIBB converter. Here, the important discussions of maximum achievable duty cycle, voltage of converter system with the given parameters and minimum input voltage needed for the desired output are explained in detail. The exact utilization of these expressions for power and control engineers also explained. Further, OVR (Output Voltage Ripple) and ESR are analysed and also the effect of ICR (Inductor Current Ripple), OVR on capacitor design discussed in detail. Moreover, the maximum permissible ESR for specified OVR is derived. Along with this, a complete non-ideal mathematical

model is developed, which gives similar response of practical system in dynamic and steady-state behaviour wise. The state-space average approach is used to develop the accurate non-ideal models. These non-ideal models are compared with the ideal models. Desired practical results are obtained by the non-ideal model with minimum tolerance. In addition, a hybrid converter namely non-inverting buck-boost derived hybrid converter (NIBBDHC) is proposed based on the knowledge of basic converter topologies. The proposed topology has a feature, which can provide both DC and AC outputs, simultaneously. Functionally as similar as conventional VSI (Voltage Source Inverter), however, shoot through is well utilized in proposed converter. Complete mathematical analysis is presented and are verified through simulation and practical implementation.

The second part of thesis is related to designing a controller for DC-DC converters. Here, IMC (Internal Model Control) is used to design the PID controller. The λ tuning is proposed for DC-DC converters. The main focus is to design a general PID controller for all types of converters and there is no need for trial and error method to choose PID parameters. Along with this, the designed PID can achieve desired bandwidth of the system, which is very important for the DC-DC converters. Further, when there exist parametric uncertainties, a PID controller is designed. The best part of this work is that, single PID controller can handle the parametric uncertainties (interval type of uncertainties). For this, Kharitonov theorem and stability boundary locus techniques are used. Here, a reduced polynomial approach is proposed for DC-DC converters. Finally, all these control techniques are implemented on considered DC-DC converters through simulations and practical experiments. The controller is implemented on DSPACE-1104 through Hardware in loop.

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(Vishwanatha Siddhartha)

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LIST OF ACRONYMS

ac, AC	Alternating Current
dc, DC	Direct Current
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
DSO	Digital Storage Oscilloscope
ESR	Equivalent Series Resistance
GCF	Gain Crossover Frequency
GM	Gain Margin
ICR	Inductor Current Ripple
IMC	Internal Model Control
MOSFET	Metal Oxide Semiconductor Field-effect Transistor
MPM	Model Plant Mismatch
NIBB	Non-Inverting Buck-Boost
NIBBDHC	Non-Inverting Buck-Boost Derived Hybrid Converter
OVR	Output Voltage Ripple
PM	Phase Margin
PI	Proportional and Integral
PID	Proportional-Derivative-Integral
PWM	Pulse Width Modulation
SMPS	Switch Mode Power Supply
SSA	State-Space Averaging
SBL	Stability Boundary Locus
VSI	Voltage Source Inverter
ZSI	Z-Source Inverter

LIST OF SYMBOLS

L	Inductor
C	Capacitor
R	Load resistance
r_g	Source or Input resistance
r_L	Inductor equivalent series resistance
r_c	Capacitor equivalent series resistance
r_d	Diode resistance
r_{on}	Switch or MOSFET ON time resistance
V_g	Steady state input supply voltage
$v_g(t)$	Instantaneous input voltage
V_o, V_{dco}	Steady state output voltage
$v_o(t)$	Instantaneous output voltage
V_{aco}	AC output voltage
V_L	Steady state voltage across inductor
$v_L(t)$	Instantaneous voltage across inductor
V_c	Steady state voltage across capacitor
$v_c(t)$	Instantaneous voltage across capacitor
V_{fd}	Diode forward drop voltage
I_g	Steady state input current
$i_g(t)$	Instantaneous input current
I_L	Steady state inductor current
$i_L(t)$	Instantaneous inductor current
I_o	Steady state output current
$i_o(t)$	Instantaneous output current
I_c	Steady state capacitor current
$i_c(t)$	Instantaneous capacitor current

Δi_L	Inductor current ripple
Δv_o	Output voltage ripple
Δv_{rC}	Voltage ripple due to ESR
Δvc	Voltage ripple due to capacitor
D, D_1, D_2	Duty cycle
D_{st1}, D_{st2}	Shoot through period
M_a	Modulation index
T	Total time period
f	Switching frequency
Q	Quality factor
ω_{LHPz}	Left Half Plane Zero
ω_{RHPz}	Right Half Plane Zero
ω_P	Pole frequency
ω_{pc}	Phase crossover frequency
ωgc	Gain crossover frequency
λ	Lambda
K_p	Proportional gain
K_i	Integral gain
K_d	Derivative gain

CHAPTER 1

INTRODUCTION

This chapter introduces the work carried out in this thesis. Beginning with fundamentals of power converters and categorization of DC-DC Converters. The basic theme and objectives of current research work have also been outlined.

1.1 Revisit to Fundamentals

A power converter is the generic name for any device which converts power (presumably electrical charge) from one mode to another. A power converter is used to take power input from a source in one form and output it into another form, more useful at the user loads. The power conversion is converting electric energy from one form to another, converting between AC and DC, or just changing the voltage or frequency, or some combination of these. Based on this and from literature [1]- [4], power converters can be classified as

1. AC to DC converters (Rectifiers)
2. AC to AC converters (AC voltage regulators or Cyclo converters)
3. DC to DC converters (Choppers)
4. DC to AC converters (Inverters)

The present thesis is completely about DC to DC converters and explained in further sections and chapters.

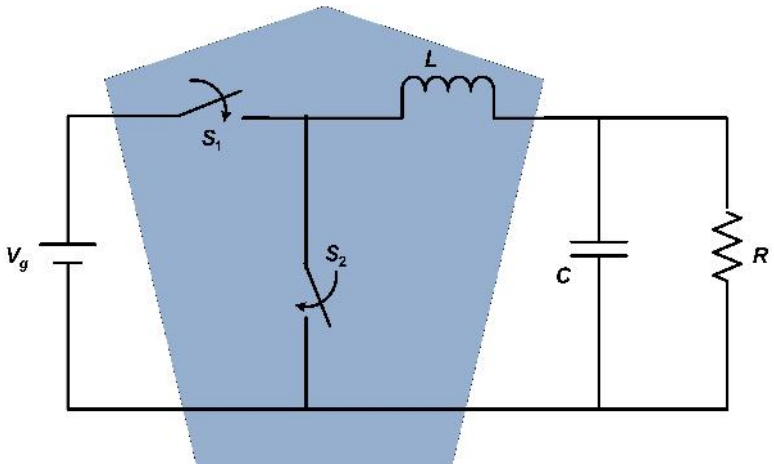
1.2 DC-DC Converters: Background

DC to DC converter is a class of power converter, which converts one level of dc voltage into higher or lower level. DC-DC conversion is important for various systems in which power supply required from battery. Such system often contains several sub-systems, each with its own voltage level requirement, different from voltage level supplied by the battery. Additionally, the battery voltage diminishes as it's stored

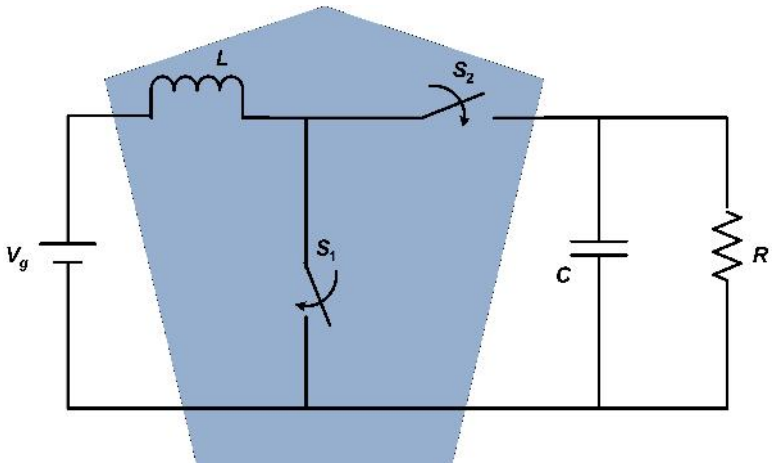
energy discharged. DC-DC conversion provided to increase voltage from a partially lowered battery voltage thereby saving the space instead of using multiple batteries.

In earlier days, linear regulators are in use for DC-DC conversion. However, linear regulators suffer from low efficiency and high amount of power wastage. In view of this research started in the direction of switched mode power conversion [5]. Advent of solid state power electronics, prone to reliable and efficient power conversion. The vital asset of switched mode converter is power conversion and voltage regulation at high efficiency is achievable, if switches are ideal in nature. Further, semi-conductor switches can be operated at high frequencies, which in turn effect the filter component selection [6, 7]. The features of switched mode converters are low weight, losses, higher efficiency and will take less space. Switched mode power converters have applications in low, medium and high power range. Low power applications are computers, mobile chargers, implant devices, energy harvesting, telecommunication, LED lighting etc. Medium range power applications are Plasma research, X-ray, PV, wire less power transfer, street lighting, auto mobile head light, Radar, DC Micro-grid, Motor drive, aerospace instruments, UPS, SMPS, power factor correction etc. High power applications will be HVDC, hybrid EV, FC-EV, Plug-in EV, V2G, Electric train, Elevator/Escalator, Air craft, Tramway etc. [8]- [30].

DC-DC converters mainly consist semi-conductor switches and filter elements (inductor and capacitor). Interconnection of these elements in different combinations will lead to different switched mode power converter topologies [31]. For interconnection of switches & energy storage elements, two conditions must be considered. First, never interrupt current through inductors. Second, never short circuit the capacitor voltages. So, by using switch inductor cell, possible topologies are shown in Figure 1.1. They are known as buck, boost & buck-boost respectively. Figure 1.1(a), shows the buck topology, which gives output voltage less than the input. It's features are, continuous output current, discontinuous input current and less OVR (Output Voltage Ripple) which requires less value of capacitance. Figure 1.1(b), shows the boost topology, which provides higher voltages than the input. Its features are, continuous input current, discontinuous output current and more OVR which requires



(a)



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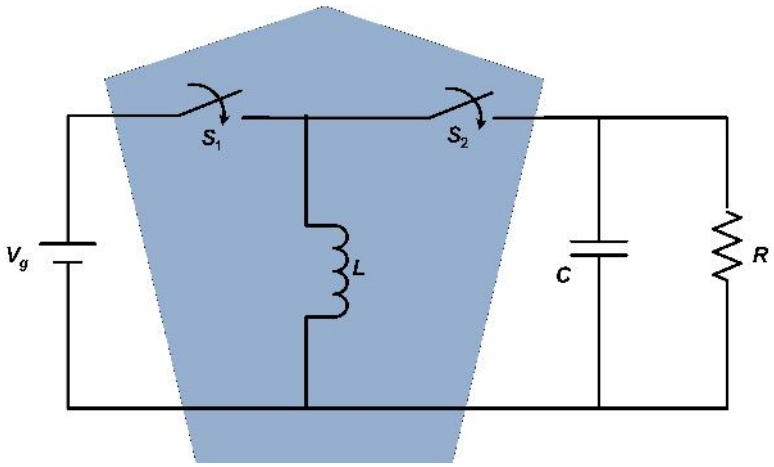


(c)

Figure 1.1: Schematic of (a)DC-DC Buck converter (b)DC-DC Boost converter (c)DC-DC Buck-boost converter.

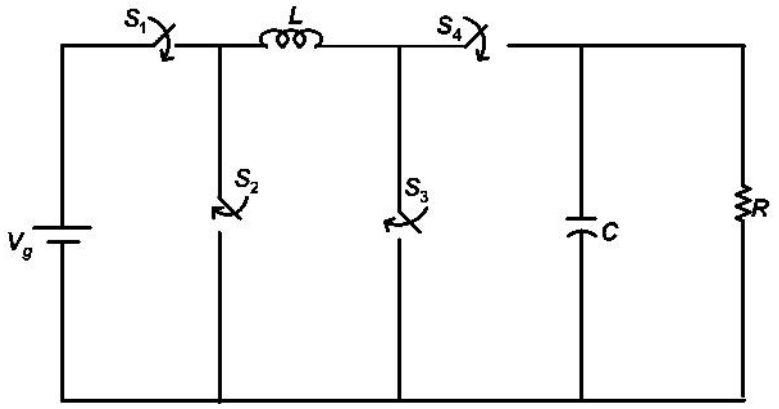


Figure 1.2: Schematic of non-inverting buck-boost converter.

high value of capacitance. Figure 1.1(c), shows the buck-boost topology, which can give both higher and lower values of output voltage than the input. Its features are, both input, output currents are discontinuous and output voltage polarity is opposite to input. These are the basic topologies of DC-DC converters, which are of second-order systems.

Further, inductor with four switch cell will be used to get different type of topologies. Using this, it is possible to get all three basic converters operation in one converter and there is no opposite polarity of output. This is also called as non-inverting buck-boost (NIBB) converter. Another way it can deduced by cascade connection of buck with boost. This is shown in Figure 1.2. NIBB converter also has single inductor, capacitor and of second order. This converter is best suited for low power portable applications [32].

Moreover, many other DC-DC converters are reported in literature [33]- [35]. Each and every topology has its own advantages, disadvantages and useful for specific applications. So, classification of these topologies available in literature [4, 31] many different ways. However, some important classifications are discussed here. Based on input and output magnitudes, DC-DC converters can be classified as step-down and step-up type. In power electronics point of view, the switched mode DC-DC converters can be classified as

- Non-isolated DC-DC Converters: There is no electrical isolation between input

and output. The basic advantages with these type of converters are simple structure, light weight, low cost and suitable for low to medium power applications. Eg: Buck, Boost, Buck-Boost, NIBB, Cuk, SEPIC, etc.

- Isolated DC-DC Converters: There is a electrical isolation between input and output by means of high frequency transformer. The basic advantages with these type of converters are less noise, less EMI problems, suitable for multi output topologies and high power applications. Anyway, magnetic elements design should be precise and size of converters is more compared to non-isolated converters. Eg: Half bridge, Full bridge, Push-pull,Forward converter etc.

Based on the power flow directions, DC-DC converters can be classified as,

- Unidirectional: Simple to control and less complex in comparison to bidirectional DC-DC converters.

- Bidirectional: Suitable for regenerating applications and complex control.

Further, DC-DC converters can be chosen for application based on current flow through the inductor. If inductor current is continuous, then it is called as CCM (Continuous Current Mode) operation otherwise DCM (Discontinuous Current Mode) operation. Generally, CCM operation is preferred in most of the applications. Whereas, in specific applications such as PFC [36], DCM operation of DC-DC converter is preferred.

1.3 Literature and Research Plan

DC-DC converters have wider applications in different fields and easy to understand, which makes most of the researchers to work in this area, around the globe. One can visualize the major research topics in this area are, design or analysis of converters, mathematical modeling of converters, new topologies for specific applications and controller design.

1.3.1 Design or Analysis of converters

The design and analysis of the DC-DC converters is an important topic of interest for power electronics researchers [37]- [45]. In the literature [46]- [48], design and analysis are carried out by considering the ideal nature of the elements mostly. However, the elements of DC-DC converters are not ideal in practice and have certain parasitic or non-idealities [4], [49] such as equivalent series resistances (ESRs) of inductors and capacitors, the parasitic resistances of diode and metaloxidesemiconductor field-effect transistor (MOSFET) during conduction and also the forward voltage drop of the diode. The design and performance of DC-DC converters are affected by these non-idealities. Inductor current ripple (ICR) and output voltage ripple (OVR) are the two important parameters to observe with the effect of non-idealities. Ripple or ESR analysis for some DC-DC converters have been reported in [2], [43]- [52]. In [43] & [44], the design analysis of non-ideal DC-DC converters (Buck and Cuk converters) presented, but input resistance is neglected. Actually, internal resistance of supply or source is also an important parameter, for example batteries have internal resistance [53], [54].

1.3.2 Modeling of converters

The modeling of the converters is an important and interesting area of research in the field of power electronics. Modelling is an important tool to know the insight of a system and also for detailed analysis of the system. Two types of models can be obtained such as large signal model and small signal model. A large signal modeling tool is necessary to study the global dynamic behaviour of switching converters and to design robust systems. Small signal models used to predict the small signal stability of system. In the literature, many modeling techniques have been reported to get the mathematical model of DC-DC converter such as circuit averaging technique, state space averaged method (SSA) [4], [33], [55, 56], current injected equivalent circuit approach (CIECA) [57, 58], switching flow graph method (SFG) [59], averaged switch models [60, 61], bond graph technique [62]- [64], energy factor approach [65]- [67], fractional order modeling [68, 69], relay feedback method [70] etc. All these

techniques or methods are needed to get mathematical model of DC-DC converter. Most of the research work in literature is found that the converter models are generally procured by considering ideal nature of elements or neglecting non-idealities of elements. Nevertheless, consideration of non-idealities or parasitic is essential to get accurate mathematical models. Therefore, in present work SSA method is used to get the complete non-ideal or accurate models of the DC-DC converters.

1.3.3 New topologies for specific applications

In addition, DC-DC converter topological research majorly moves around application point of view. In present scenario DC micro grids, smart grids and nano grids reflect the fast growth of technology. These advanced systems insisting further hybrid technology from power electronic converters point of view. Many sophisticated power electronic converters are available, in order to feed both DC and AC loads independently from grid or renewable source [71,72]. But no converter can give both AC and DC simultaneously. This has been shown in Figure 1.3(a), whereas Figure 1.3(b) presents hybrid architecture to feed both AC and DC simultaneously. These hybrid topologies are more reliable and capable (capability of using shoot through issue effectively). The hybrid converter topologies presented in literature [73]- [76]. By studying carefully, a new hybrid converter topology is proposed in this work.

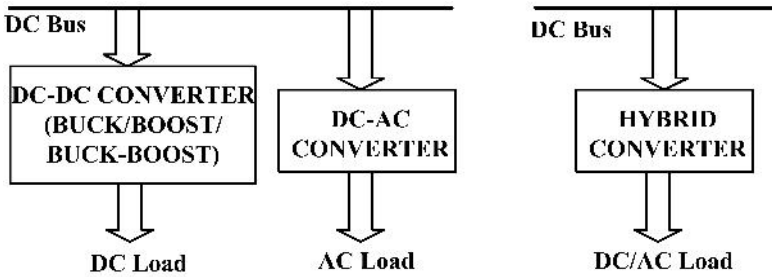


Figure 1.3: Hybrid architecture.

1.3.4 Control of DC-DC converters

Finally, another interesting and important topic of DC-DC converters is controller design based on their mathematical models. Generally, in control theory, it may

be observed that one way of classifying systems is linear and non-linear. Further, linear systems can be classified as minimum and non-minimum phase. Here, DC-DC converters are classified in many ways as discussed before. It is important to know the dynamic behaviour of the system, before designing a controller. So, in control point of view, DC-DC converters (based on their transfer function models) can be classified as

- Minimum phase (MP) converters (Eg: Buck,Forward converter etc.)
- Non-minimum phase (NMP) converters (Eg: Boost, Buck-boost converter etc.)

Many researchers have given their contribution towards the control of DC-DC converters in the literature. In various control techniques, PID controller design is very important aspect. Available methods to design PID controller are K-factor approach [78], frequency response method [79], Z-N method [80], stability boundary locus (SBL) method [81], PID design by internal model control (IMC) [82], PID design by fractional order control [83], PID formulation based on capacitor current [84] etc., presented in the literature. As some of DC-DC converters are NMP type, specifically for these also control designs are reported in literature [85]- [90]. Further, in the literature, optimal control like LQR-LQG [91], predictive control [92]- [94], Smith-predictor control [125]- [127], one-cycle control [95] [96], H-infinity control [97], sliding mode control [98]- [103], fractional order control [104], fuzzy control [105]- [107], type-2 fuzzy logic control [108], neural network controller [109]- [110], neuro-fuzzy control [111]- [112], adaptive control [113, 114] evolutionary techniques [115]- [116] and cascaded control schemes like PI-SMC [117]- [120], IMC-SMC [121], etc., are reported.

All these control methods have its own advantages and disadvantages depending upon requirement. However, there is always a scope in every method to improve performance of the DC-DC converters. Though there are many control methodologies, classical PID control always been a better option [122, 123] over other controllers for the following reasons.

- These are not involving complex calculations.

- Many industries are still using PID for different applications.
- Simple to understand.

From the reported work, it is observed that tuning of PI/PID is an always interesting topic of area for researchers. To the best of author's knowledge, there is no generalized PI/PID design for DC-DC converters without trial and error of any parameter. This idea has motivated to design generalized PI/PID design for DC-DC converters without trial and error of any parameter. For this purpose, IMC (Internal Model Control) has been used.

1.3.4.1 IMC literature

IMC design scheme was proposed by Garcia and Morari [124]. Similar to Smith predictor control scheme [125], IMC does require model and other summing blocks for its design and thereby making it complex for implementation. The ease of implementing IMC controller comes into picture when it is treated through the conventional feedback control structure [128, 129]. There are some alternate representation of IMC structure in the form of two- or three-degree of freedom control where number of degree corresponds to different number of attributes (tracking, disturbance rejection, robustness) independently by individual controller [130]- [132]. Recently, the concepts of active disturbance rejection and iterative learning have opened a new gate way to utilize IMC framework to obtain advanced control schemes [133, 134]. The power of IMC theory flashes out when it is utilized for the implementation and tuning of PID controller [135]. In literature [136]- [138], concept of IMC has been used in different applications. Through IMC theory, all the tuning parameters of PID controller can be evaluated by a single parameter (generally represented by λ and therefore also known as lambda tuning in some research articles [139]).

1.3.4.2 Literature on lambda tuning

Generally, lambda selected such as less than the closed-loop bandwidth over which the process model is valid [135]. Later on, Brosilow and Joseph [140] recommended that filter parameter (*i.e.,*lambda) should be chosen such that the high frequency gain

of the controller does not exceed 20 times of its low frequency gain. Horn et al. [141] proposed new arrangements of filter and recommended that lambda should be less than largest time constant in the system. Liu et al. proposed that lambda is evaluated by minimizing a weighted function of integral square error (ISE) and the maximum of the complementary sensitivity function [142]. Whereas, Chen et al. extracted tuning principles based on specification of maximum closed-loop amplitude ratio of +2 dB [143]. Further, Chen and Seborg [144] presented a direct synthesis design method to improve disturbance rejection. Kaya [145] also suggested tuning methods based on desired gain and phase margin specifications .

Overall, it is clear that the single tuning parameter lambda is related to the cross over frequency of the system. Similarly, DC-DC converters speed of response is also related to bandwidth (bandwidth should be one tenth to one fifth of switching frequency of DC-DC converter). So, by choosing λ in relation to bandwidth, it will be better for DC-DC Converters. Therefore, in the present work, λ tuning of PID design for DC-DC converters without trial and error of any parameter is proposed.

1.3.4.3 Literature on robust PID design

Another basic requirement of controller is to make the whole system robust or in other words is to make the system insensitive to disturbances and parametric variations. Therefore, stability analysis and robust controller design are extremely important. Robust controller design process requires a model with uncertainties. Robust analysis and design of controller for interval systems or systems with parametric uncertainties is available in literature [146, 147]. Specifically, most of the robust controller design for DC-DC converters has been done using H^{∞} technique [97], QFT technique [148] etc. Even though, these control techniques function fairly, as mentioned before heavy mathematics, complex analysis and most of industries choice is PID type controller. Especially, for uncertain cases, Kharitonov's theorem [149] is simple and useful to design PID.

In control literature, there exist Kharitonov's theorem which is useful for stability analysis of interval systems [149]. Recently, various simple techniques are reported

for stability analysis of DC-DC converters based on Kharitonov's theorem [150]-[152]. In [153], design of classical controllers (P, PI, PID) based on Kharitonov's theorem are shown. In [81, 155], a new design technique based on Kharitonov's theorem reported for stabilization of an interval plant based on the specific stability margin, hence robust controller can be designed. In [156, 157], robust controller design for uncertain systems using Kharitonov's theorem has been presented. From the literature survey, it is found that as the order of uncertain plant increases, then the number of interval plant transfer functions will be more. Hence, it will increase the complexity for designing of robust PID controller by using Kharitonov's theorem. Further, with the existing work, it is difficult to choose the PID parameters exactly. So, this motivates authors to design robust PID controller for DC-DC converters. This is an another contribution of this work.

1.4 Main Contributions

Based on literature survey and research plan, the important objective of this thesis is to present the accurate design and transfer function models of non-isolated DC-DC converters for controller design, which focus on following points: importance of including non-idealities, control oriented analysis, obtaining PID parameters directly from model. The main research contributions are as given below:

- The non-isolated DC-DC converter topologies such as buck, boost, buck-boost and NIBB are designed and modelled by including all major non-idealities such as equivalent series resistances (ESR) of inductor, capacitor, source resistance, MOSFET resistance, diode resistance and diode forward voltage drop to obtain the almost equivalent model of practical converter system. Here, some important expressions like maximum achievable duty cycles, voltage and maximum permissible ESR are discussed in detail.

- The state space models of complete non-ideal models are presented. Effects of parasitics or non-idealities on the performance of converter system are evaluated. The obtained steady-state and small signal models are to be analysed in control point of view and need to deduce some important conclusions for

closed loop operation and controller design.

- From the knowledge of basic converter topologies, with some modifications a new converter topology is proposed. The proposed converter can give both AC and DC outputs, simultaneously.

- Finally, from the transfer functions of modelled DC-DC converters, it is clear that some of them are minimum phase systems (eg: buck converter) and some of them are non-minimum phase systems (eg: boost, buck-boost converters). A general PID design method is proposed for DC-DC converters. Along with this, a robust PID controller is designed for DC-DC converters, when there are parametric variations.

- The simulation results of theoretical analysis validation performed. For this, a laboratory prototype is developed. Controller implementation has been done on dSPACE-1104 controller board.

1.5 Overview of Thesis

The thesis is organized in six chapters, Chapter 1 explores the scope of the present research, theoretical background of DC-DC converters, literature survey on the proposed work and research objectives of the present study. This chapter will highlight why the area under investigation in this thesis is of high and rising relevance. The remaining part of the thesis is structured as follows:

Chapter 2 presents a non-ideal DC-DC boost converter design and modeling by considering all major non-idealities, which gives an accurately designed model. Duty cycle and filter elements expressions are modified. Important specifications such as maximum possible voltage and duty cycle, minimum input voltage to get a particular output voltage are presented. Further, detailed analysis of ICR, OVR and ESR are discussed in detail. Effect of parasitics on plant model is analysed. It also includes detail steady state and control oriented analysis using small signal model. Finally, the importance of complete non-ideal is verified by comparing it with other semi non-ideal converters. All theoretical studies are validated through experiments.

Chapter 3 presents design and modeling of a non-ideal DC-DC buck-boost converter by considering all major non-idealities. Modified formulae for duty cycle and filter elements are derived. Important specifications such as maximum possible voltage and duty cycle, minimum input voltage to get a particular output voltage are presented. Further, detailed analysis of ICR, OVR and ESR are discussed in detail. Effect of parasitics on plant model is analysed. It also includes detail steady state and control oriented analysis using small signal model. Finally, the importance of complete non-ideal is verified by comparing it with other semi non-ideal converters. All theoretical studies are validated through experiments.

Chapter 4 presents design analysis of two switch buck-boost converter or non-inverting buck-boost (NIBB) converter by considering all major non-idealities. It can be viewed as generalised converter, as it can be operated in buck, boost and buck-boost modes. The expressions for output voltage, duty cycles, filter elements are derived. These are generalised expressions, since it is shown that from these expressions, remaining basic converter (buck, boost and buck-boost) expressions are obtainable. As there are two duty cycles, modeling and analysis are little bit different as compared to single switch converters. Effect of parasitics on plant model or practical system is presented. It also includes detail steady state and control oriented analysis using small signal model. Further, NIBB derived Hybrid converter is proposed and analysed. All theoretical studies are validated through experiments.

Chapter 5 presents the controller design of DC-DC converters. DC-DC converters are classified based on their transfer function models and gain cross over frequency selection is discussed in detail. Further in this chapter, main focus is to get PID values using models obtained in previous chapters. For this, model based controller IMC (Internal Model Control) is explored and proposed a generalised PID design for DC-DC converters. Along with this, robust PID controller is also designed, when all plant parameters are varying. For this Kharitonov theorem, stability boundary locus are utilized. All theoretical studies are validated through experiments.

Chapter 6 summarizes the conclusions drawn from the exhaustive experimentation carried out in the present research work on “Modeling, Analysis and Control of

Non-isolated DC-DC Converters". This chapter also presents the limitations of the present work and emphasizing the scope for future work in this field.

CHAPTER 2

NON-IDEAL PWM DC-DC BOOST CONVERTER

This chapter presents different design issues and accurate mathematical modeling of non-ideal boost converter in detail. The steady-state and dynamic analysis of non-ideal boost converter are explained. Various transfer functions are derived and analyzed the effect of non-idealities.

2.1 Background and Motivation

A PWM DC-DC boost converter is a basic step-up voltage circuit having many features, which make it suitable for variety of applications extending from low-power portable devices to high-power stationary applications. Some of them will be in a cellular phone (to provide proper bias to the RF amplifier) or locally to provide adequate high-side bias to a dedicated circuitry, in battery-powered systems (e.g., a 12 V battery supplying an audio amplifier), solar, micro-grid, aerospace and power supplies. The extensive application of PWM DC-DC boost converters has been attracted by its less count of elements, which makes it more advantageous in terms of simple design implementation, manufacturing [8].

In view of these applications or as everyone needs an accurate and optimal design, analysis of boost converter. Most of the research articles and information about design analysis of boost converter presented by considering the ideal nature of elements [1]- [4]. Nevertheless, the converter elements are not ideal in nature and have non-idealities [43], [44] [49], [158]- [160]. The effect of these non-idealities or parasitics on element design and analysis is not negligible. Specifically in aerospace applications or power supplies, where accurate design is necessary and compact size is required. In general, the dc output voltage is proportional to the duty cycle for DC-DC converters [161, 162]. Therefore, in order to get the desired output voltage, the duty cycle of the switch should be estimated properly.

The duty cycle of an ideal boost converter operating in continuous conduction

mode (CCM) is given by

$$D_{ideal} = \frac{V_o - V_g}{V_o} \tag{2.1}$$

where, V_g is input voltage and V_o is output voltage. This equation is well known and is derived by considering the ideal behaviour of elements [1]- [4]. However, in practical case, duty cycle given in Eq. (2.1) does not provide exact output voltage V_o for a input voltage V_g. This is due to the power loss across the non-ideal components. Further, the knowledge of maximum achievable output voltage V_o with the boost converter is necessary before operating it in a closed-loop. Moreover, accurate design of converter elements is also important to achieve desired performance. This can be done by rigorous analysis of converter circuit and its operation. So, this chapter includes the exhaustive analysis of non-ideal DC-DC Boost converter carried out to obtain the accurate expressions for duty cycle, maximum achievable duty cycle, maximum achievable voltage and modified equations for design of inductor and capacitor.

The proper estimation of output voltage ripple (OVR) is also an important issue for DC-DC converters, especially for high performance applications such as aerospace, military and distribution generation [8, 43, 44]. In boost converter, the equivalent series resistance of output capacitor plays an important role. The low ESR capacitor results in lesser output voltage ripple. On the other hand, large ESR increases the output voltage ripple, hence arising the need to have a large capacitance value. Moreover, ESR may also affect the stability of the converter. Therefore, in this chapter, a nearly accurate formula of maximum permissible ESR for specified OVR and ICR is derived. It is shown by the simulation and experimental results that if the ESR is chosen beyond this limit, the output voltage will have more ripples than the specified.

Once design analysis is completed, then the next most important for the converters is mathematical modeling. With which, one can get transfer function to design controller. Most of the work in literature about boost converter modeling [4, 163, 164] presented by considering ideal nature of elements, since it is easy to understand. Some researchers [49, 165, 166] shown interest in non-ideal modeling, but not considered all non-idealities. In this chapter, DC-DC boost converter is modelled by

considering all non-idealities using well-known SSA (State Space Averaging) approach. Further, effect of these parameters on poles, zeros and stability of converter is analysed. Moreover, the RHP (Right Half Plane) zero of boost converter explained in practical way and important discussions for controller design are concluded.

The following sections discusses the detailed design issues and modeling analysis of non-ideal dc-dc boost converter.

2.2 Fundamental Analysis

The preliminary equations of complete non-ideal DC-DC boost converter is presented. The schematic representation is shown in Figure 2.1(a). The circuit consists of switch (S), diode (D_d), inductor (L), capacitor (C) and load resistance (R). For obtaining nearly accurate model of boost converter, all parasitic resistances are considered such as source resistance (r_g), inductor resistance (r_L), switch resistance (r_{on}), diode resistance (r_d), diode forward voltage drop (v_{fd}), capacitor ESR (r_c). Further, V_g is input supply, v_o is output voltage, v_c is voltage across capacitor, v_L is voltage across inductor, D is duty cycle and T is total period. In comparison to load resistance R, the parasitics values are very small. The duty cycle D is ratio of switch ON time (t_{on}) to the total time period ($T = t_{on} + t_{off}$). Mathematically [3],

$$D = \frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}}{T} = t_{on} f_s \tag{2.2}$$

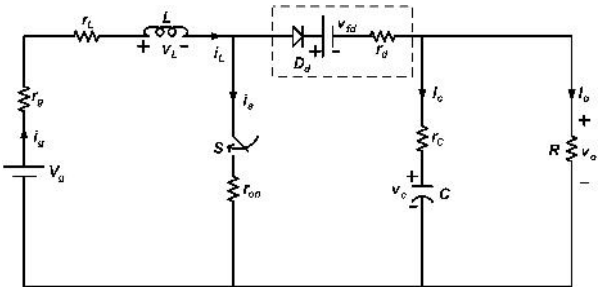
Here, we have made few assumptions [4] for analysing the PWM DC-DC boost converter.

Assumption 1: PWM DC-DC boost converter is operating in continuous conduction mode (CCM). In CCM operation, converter works in two switching intervals: (a) ON time interval, *i.e.*, $0 < t \leq DT$ and (b) OFF time interval, *i.e.*, $DT < t \leq T$.

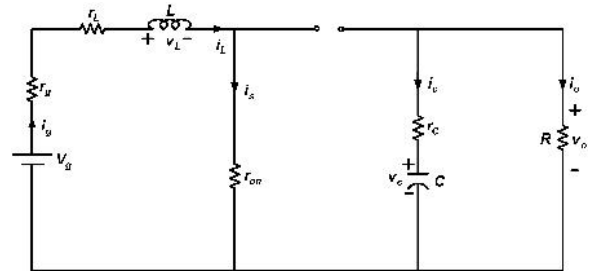
Assumption 2: Initial charging current through inductor is zero, *i.e.,* $i_L(0) = 0$ and initial voltage across the capacitor is zero, *i.e.,* $v_c(0) = 0$.

2.2.1 Energy storing phase ($0 < t \leq DT$)

The equivalent circuit for boost converter during interval $0 < t \leq DT$ *i.e.,* ON period is shown in Figure 2.1(b). In this interval, the diode (D_d) is OFF and switch is replaced



(a)



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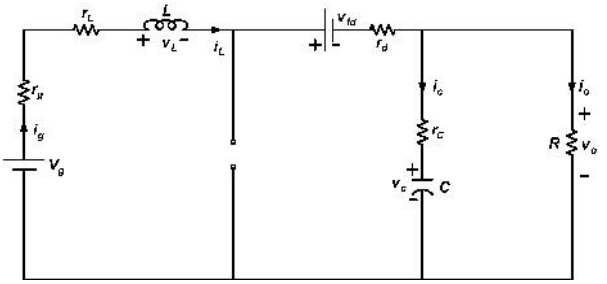
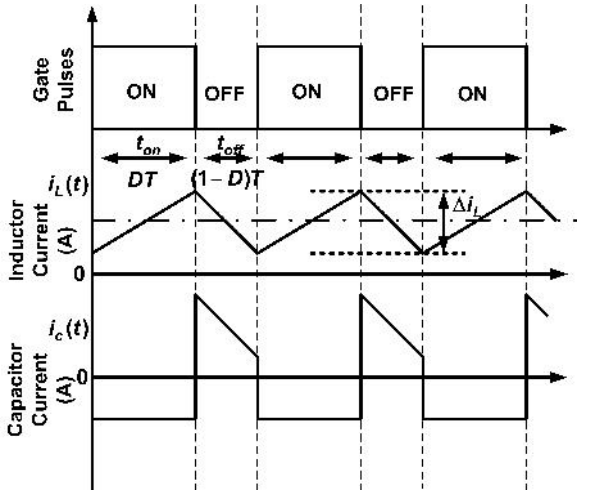


(c)



(d)

Figure 2.1: Schematic of (a)non-ideal DC-DC boost converter (b)during ON time (c)during OFF time (d) related waveforms.

by its ON time resistance (r_{on}). Here, the switch current (i_s) is same as inductor current (i_L) and input current (i_g). Diode current (i_d) is zero. During this period, the inductor stores energy, and the output capacitor alone powers the load. The wave forms corresponding to this interval are also shown in Figure 2.1(d).

Using Kirchhoffs voltage law (KVL) and Kirchhoffs current law (KCL), the fundamental equations for the circuit shown in Figure 2.1(b) are obtained as follows:

$$(v_L(t))_{ON} = L\frac{di_L(t)}{dt} = -\left[r_g + r_{on} + r_L\right] i_L(t) + v_g(t) \tag{2.3}$$

$$(i_c(t))_{ON} = C\frac{dv_c(t)}{dt} = -\frac{v_o(t)}{R} \tag{2.4}$$

$$(v_o(t))_{ON} = v_c(t) + r_c i_c(t) \tag{2.5}$$

2.2.2 Energy releasing phase ($DT < t \leq T$)

The equivalent circuit for boost converter during interval $DT < t \leq T$ *i.e.,* OFF period is shown in Figure 2.1(c). In this interval, the switch (S) is OFF and diode (D_d) is ON. Here, the diode (D_d) is replaced by its equivalent model, *i.e.,* resistance (r_d) in series with forward voltage (v_{fd}). The input current (i_g) is same as inductor current (i_L) and switch current (i_s) is zero. In this interval, the stored inductive energy appears in series with the input source and contributes to supply the output. The capacitor charges by inductor and supply, then discharges through load. The wave forms corresponding to this interval are also shown in Figure 2.1(d).

Using KVL and KCL, the fundamental equations for the circuit shown in Figure 2.1(c) are obtained as follows:

$$(v_L(t))_{OFF} = L\frac{di_L(t)}{dt} = -\left[r_g + r_L + r_d + \frac{Rr_c}{R+r_c}\right] i_L(t) - \frac{R}{R+r_c}v_c(t) - V_{fd} + v_g(t) \tag{2.6}$$

$$(i_c(t))_{OFF} = C\frac{dv_c(t)}{dt} = i_L(t) - \frac{v_o(t)}{R} \tag{2.7}$$

$$(v_o(t))_{OFF} = v_c(t) + r_c i_c(t) \tag{2.8}$$

2.3 Steady-State Analysis

For the steady state analysis of PWM DC-DC boost converter, the following assumptions are made.

Assumption 1: Voltages and currents are assumed constant over one switching cycle.

Assumption 2: Voltages and currents are represented by their average (steady state) values as follows:

$$i_L(t) = I_L, v_g(t) = V_g, v_C(t) = V_C$$

In general, the average value X of a variable $x(t)$ over a period T is given as:

$$X = \frac{1}{T}\int_0^T x(t)dt = Dx_{on}(t) + D'x_{off}(t) \tag{2.9}$$

where, $x(t)$ is voltage across or current through an element of the boost converter, $D' = 1 - D$. The terms $x_{on}(t)$ and $x_{off}(t)$ represent the variable $x(t)$ during switch ON and switch OFF, respectively.

According to volt-sec balance [4], in steady state, the average inductor voltage must be equal to zero.

$$V_L = \tfrac{1}{T}\int_0^T v_L(t)dt = \tfrac{1}{T}\left(\int_0^{t_{on}=DT}(v_L(t))_{ON}dt + \int_{t_{on}=DT}^{t_{off}=(1-D)T}(v_L(t))_{OFF}dt\right) = 0 \tag{2.10}$$

Similarly, in steady state, according to charge balance [4] through the capacitor, the average capacitor current must be equal to zero.

$$I_C = \tfrac{1}{T}\int_0^T i_C(t)dt = \tfrac{1}{T}\left(\int_0^{t_{on}=DT}(i_C(t))_{ON}dt + \int_{t_{on}=DT}^{t_{off}=(1-D)T}(i_C(t))_{OFF}dt\right) = 0 \tag{2.11}$$

The average output voltage is determined as follows:

$$V_o = \tfrac{1}{T}\int_0^T v_o(t)dt = \tfrac{1}{T}\left(\int_0^{t_{on}=DT}(v_o(t))_{ON}dt + \int_{t_{on}=DT}^{t_{off}=(1-D)T}(v_o(t))_{OFF}dt\right) = 0 \tag{2.12}$$

Substitute (2.3) and (2.6) in (2.10), we get,

$$V_L = D\left(V_g - (r_g + r_{on} + r_L)I_L\right) + (1-D)\begin{pmatrix} V_g - V_{fd} - \frac{R}{R+r_C}V_C \\ -\left(r_g + r_L + r_d + \frac{Rr_C}{R+r_C}\right)I_L \end{pmatrix} = 0$$

$$\Rightarrow \tfrac{V_C R}{R+r_C} = \tfrac{V_g}{(1-D)} - V_{fd} - \tfrac{\left(r_g + r_L + Dr_{on} + (1-D)\left(r_d + \frac{Rr_C}{R+r_C}\right)\right)I_L}{(1-D)} \tag{2.13}$$

Substitute (2.4), (2.7) in (2.11), we get,

$$\begin{aligned} &I_C = D\left(-\tfrac{V_o}{R}\right) + (1-D)\left(I_L - \tfrac{V_o}{R}\right) = 0 \\ &\Rightarrow I_L = \tfrac{V_o}{(1-D)R} = \tfrac{I_o}{(1-D)} \end{aligned} \tag{2.14}$$

Here, I_o is the steady-state value of load current. Substitute (2.5) and (2.6) in (2.12), we get,

$$\begin{aligned} &V_o = D\left(V_C + I_C r_C\right) + (1-D)\left(V_C + I_C r_C\right) \\ &\Rightarrow V_o = V_C \end{aligned} \tag{2.15}$$

2.3.1 Output voltage expression

Substitute (2.14) and (2.15) into (2.13), we get,

$$\frac{V_o R}{R + r_C} = \frac{V_g}{(1-D)} - V_{fd} - \frac{\left(r_g + r_L + D r_{on} + (1-D)\left(r_d + \frac{R r_C}{R + r_C}\right)\right) V_o}{R(1-D)^2} \tag{2.16}$$

$$\Rightarrow V_o \left(\frac{\left(r_g + r_L + D r_{on} + D^{'} r_d\right)(R + r_C) + D^{'}\left(D^{'} R + r_C\right)}{D^{'} R\left(R + r_C\right)} \right) = V_g - D^{'} V_{fd}$$

Finally, we get output voltage expression as

$$\Rightarrow V_o = \frac{[V_g - D' V_{fd}] D' R (R + r_c)}{[(r_g + r_L + D r_{on} + D' r_d)(R + r_c)] + [D' R (D' R + r_c)]} \tag{2.17}$$

Further, we can write,

$$\Rightarrow V_o = \frac{M V_g}{\frac{V_{fd}}{V_o} + \frac{1}{R}\left[M^2\left(r_g + r_L + r_{on}\right) + M\left(r_d - r_{on}\right)\right] + \frac{1 + \frac{M r_C}{R}}{1 + \frac{r_C}{R}}} \tag{2.18}$$

Here, $M = \frac{1}{D'}$.

If all non-idealities are zero, then the ideal output voltage of boost converter is

$$V_o = \frac{V_g}{D'}. \tag{2.19}$$

In an ideal PWM DC-DC boost converter, the output voltage is a function of duty cycle and input voltage only. However, by including non-idealities, the output voltage V_o of PWM DC-DC boost converter is not only function of duty cycle D and input voltage V_g but also the load resistance R and other parasitic elements, which is shown in Eq. (2.17).

Table 2.1: Parameters of DC-DC boost converter

Parameters	Value
Input voltage (V_g)	5V
Output voltage (V_o)	8.33V
Source resistance (r_g)	0.2 Ω
Inductor (L/r_L)	250 μH/ 0.24Ω
Capacitor (C/r_c)	200 μF/ 0.12Ω
Diode forward drop (V_{fd})	0.5V
Diode resistance (r_d)	0.03 Ω
Switch resistance (r_{on})	0.05 Ω
Switching frequency (f)	20KHz
Load resistance (R)	22Ω/100 W

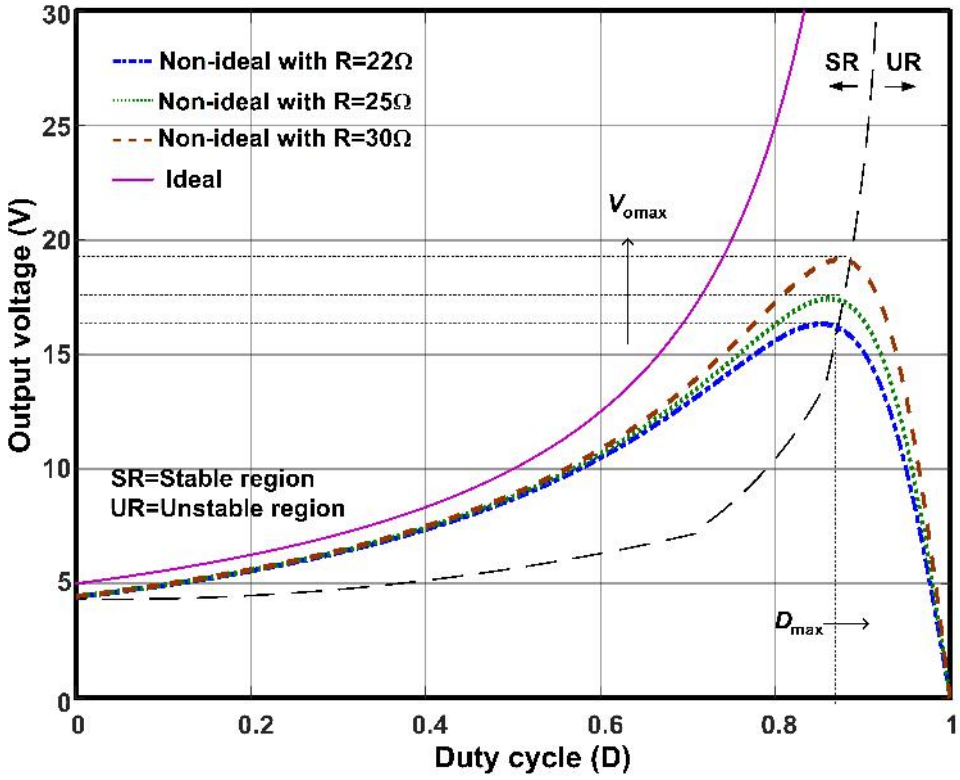


Figure 2.2: Output voltage versus duty cycle for different load resistances.

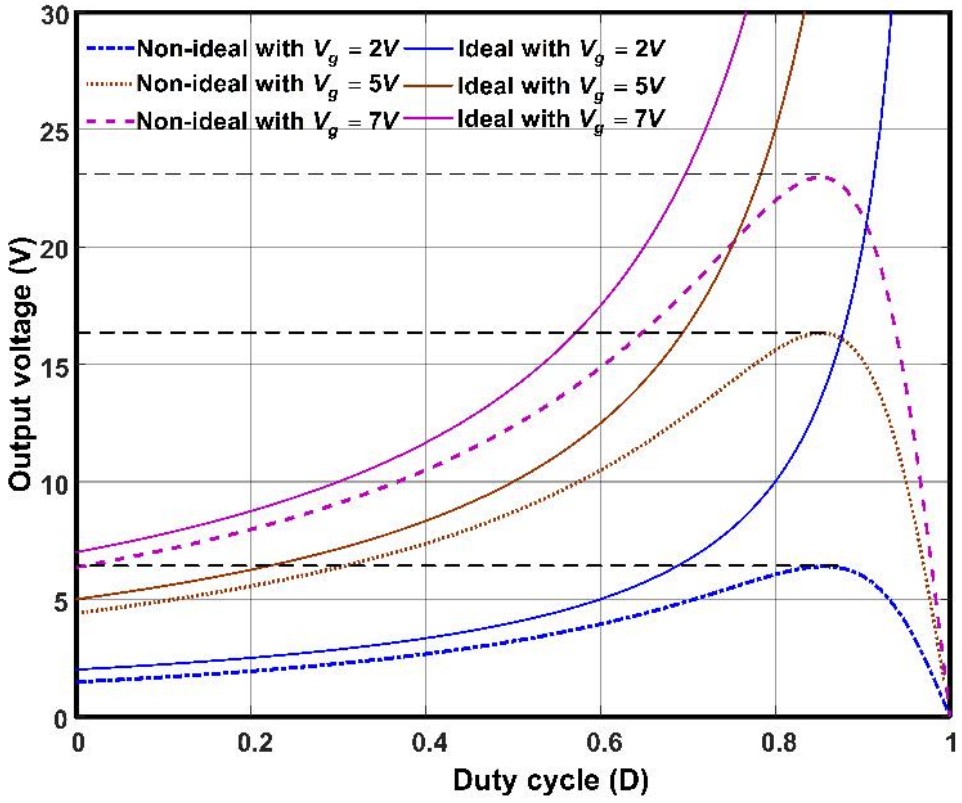


Figure 2.3: Output voltage versus duty cycle for different input voltages.

The plot of output voltage V_o as a function of duty cycle D is shown in Figure 2.2 for ideal and non-ideal cases at different load resistances (R) and other parameters are constant. For an ideal case, the converter output voltage increases with duty cycle. On the other hand, for the non-ideal case, the output voltage first increases with duty cycle, reaches its maximum value, and then decreases to zero at duty cycle close to unity. The output voltage is dependent on load resistance also. At a particular value of duty cycle, as the load resistance decreases, the output voltage also drops significantly. For any fixed duty cycle, the difference between ideal dc output voltage and non-ideal dc output voltage increases with decrease in load resistance. This is because of the increased voltage drop across the non-idealities in practical boost converter at lower load resistance (or higher load current). As the load resistance increasing, the V_{omax} and D_{max} are also increasing.

Reason for unstable region: DC-DC boost converter is one of the indirect energy transfer converter. It means, energy stores first (*i.e.,* during ON time) and releases in

next phase (*i.e.,* during OFF time). Moreover, reason for boost operation is that the voltage across inductor during ON time is positive (equal to supply or input voltage) and during OFF time must be negative (equal to input voltage minus output voltage). This employs output voltage or capacitor stored voltage is more than the input. For higher duty cycles ($\geq D_{max}$) also the explanation is same, but the stored energy is comparatively less. This is the reason that the output voltage decreases instead of increasing after D_{max}.

The plot of output voltage V_o as a function of duty cycle D is shown in Figure 2.3 for ideal case and non-ideal case at different input voltages (V_g) and other parameters are constant. For a particular duty cycle, the difference between the output voltage of an ideal and non-ideal boost converter becomes larger as input voltage increases. So, in the presence of parasitics, switch should kept ON for long time to get the same output voltage. As the input voltage decreases, V_{omax} also decreasing in non-ideal case. This V_{omax} is decreases because of input voltage variation. From this, we get the information of minimum input voltage (V_{gmin}) to be applied for converter at fixed output voltage (in regulator problems).

Therefore, it is clear that the output voltage of a practical boost converter is always less than the ideal boost converter, if the MOSFET switch of practical boost converter is operated at a duty cycle which satisfies the relation in Eq. (2.19). It is because, this relation is for ideal boost converter which neglects the non-idealities present in practical boost converter. Therefore, to achieve the desired output voltage from a practical boost converter, duty cycle should be obtained by satisfying the input-output voltage relationship in Eq. (2.17). This will be the practical duty cycle and greater than the ideal one as given in (2.1).

2.3.2 Modified duty cycle expression

From previous discussion, we conclude that there is a need to develop an improved or modified expression for duty cycle in presence of parasitics or non-idealities. The derivation as follows:

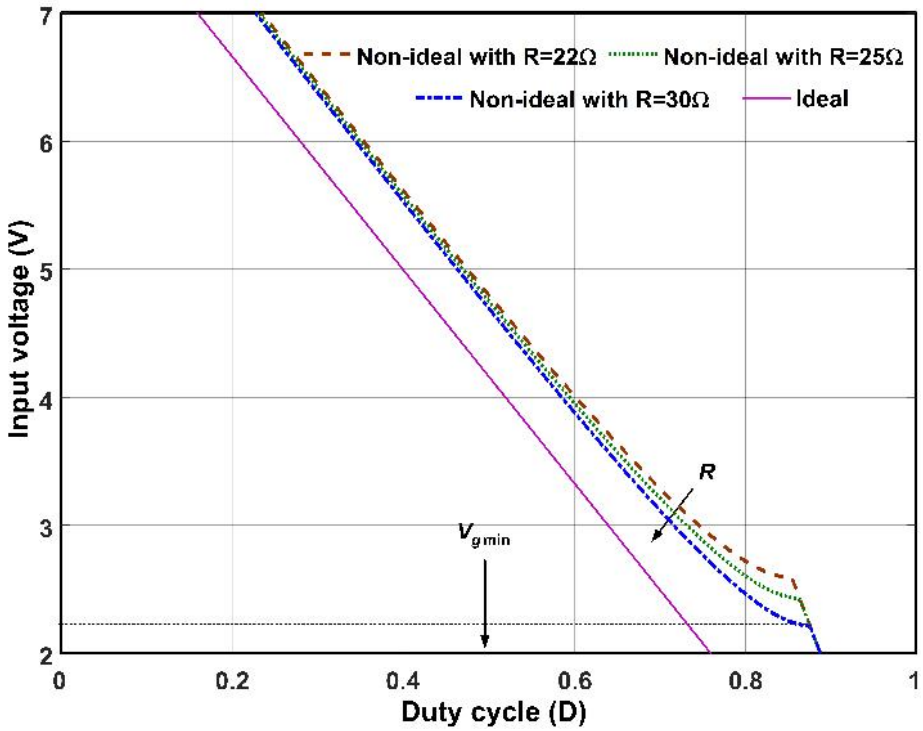


Figure 2.4: Output voltage of boost converter as a function of duty cycle for a fixed output voltage when both input voltage and load resistance are varying.

Rewriting (2.18) as,

$$V_{fd} + \frac{V_o}{R}\left(\left[\frac{1}{(D')^2}\left(r_g + r_L + r_{on}\right) + \frac{1}{D'}\left(r_d - r_{on}\right)\right] + \frac{1 + \frac{r_C}{D'R}}{1 + \frac{r_C}{R}}\right) = \frac{V_g}{D'}$$

Further simplifying, we get a quadratic expression in terms of D' as,

$$\underbrace{\left(V_o R^2 + V_{fd} R\left(R + r_C\right)\right)}_{a}\left(D'\right)^2 + \underbrace{\left(-V_o\left(\left(r_{on} - r_d\right)\left(R + r_C\right) - R r_C\right) - V_g R\left(R + r_C\right)\right)}_{b}\left(D'\right) + \underbrace{V_o\left(r_g + r_L + r_{on}\right)\left(R + r_C\right)}_{c} = 0 \tag{2.20}$$

The solution of above quadratic equation will be,

$$D' = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{2.21}$$

The practicable or realizable duty cycle falls under positive sign. Therefore, the improved expression for duty cycle of a practical DC-DC boost converter is obtained as

given in Eq. (2.22).

$$D^{'} = D^{'}_{ideal} \frac{\left[1 + \frac{V_o}{V_g}\left(\frac{r_{on} - r_d - R\|r_c}{R}\right)\right] + \sqrt{\left[1 + \frac{V_o}{V_g}\left(\frac{r_{on} - r_d - R\|r_c}{R}\right)\right]^2 - 4\left[\frac{V_o}{V_g}\right]^2 \left[\frac{R}{R+r_c} + \frac{V_{fd}}{V_o}\right]\left[\frac{r_g + r_L + r_{on}}{R}\right]}}{2\left[\frac{R}{R+r_c} + \frac{V_{fd}}{V_o}\right]} \tag{2.22}$$

Whereas, from (2.19), the ideal formula for DC-DC boost converter is

$$D^{'}_{ideal} = \frac{V_g}{V_o} \tag{2.23}$$

This expression (2.22) confirms that the actual duty cycle is not only dependent on output voltage and input voltage as in ideal case but also depends on load resistance and other non-ideal elements of boost converter. The duty cycle calculated using Eq. (2.22) results in exact value of output voltage V_o which we desire.

The plot of input voltage V_g as a function of duty cycle D for different load resistances at a particular output voltage is shown in Figure 2.4. In this, other parasitics are considered as constant. It shows that the actual duty cycle is dependent on load resistance and at a particular value of input voltage, as the load resistance decreases, the required duty cycle increases. In an ideal case, it is possible to achieve desired output voltage for any value of input, but in non-ideal case, it is not possible. Moreover, there is a limit on minimum value of input voltage. As the load resistance increases, the minimum value of input voltage (V_{gmin}) to be applied decreases.

2.3.3 Maximum achievable duty cycle and output voltage

Figures 2.2-2.4 and previous section analysis explains the importance to derive the maximum value of duty cycle. The derivation as follows:
Rewriting (2.17),

$$V_o = \frac{[V_g - D'V_{fd}]D'R(R + r_c)}{[(r_g + r_L + Dr_{on} + D'r_d)(R + r_c)] + [D'R(D'R + r_c)]}$$

From above expression, it is observed that V_o is a function of D. Now, maximum value of this expression (2.17) can be found as follows:

$$\frac{\partial V_o}{\partial D} = 0 \tag{2.24}$$

Therefore, by differentiating V_o with respect to D and equating to zero, we get the expression of maximum permissible duty cycle (D_{max}) as follows:

$$D_{\max} = \frac{[V_g R^2 + V_{fd} r_1] - \sqrt{r_2 \left[(V_g R)^2 + V_g V_{fd} r_3 + V_{fd}^2 r_2 \right]}}{V_g R^2 + V_{fd} r_3} \tag{2.25}$$

where,

$r_1 = (r_L + r_d + r_g)(R + r_c) + Rr_c$, $r_2 = (r_L + r_{on} + r_g)(R + r_c)$, $r_3 = (r_d - r_{on})(R + r_c) + Rr_c$.

By substituting Eq. (2.25) in Eq. (2.17), the maximum achievable voltage (V_{omax}) with the given converter can be determined as,

$$V_{o\max} = \frac{\left[V_g - D'_{\max} V_{fd}\right] D'_{\max} R (R + r_C)}{[(r_g + r_L + D_{\max} r_{on} + D'_{\max} r_d)(R + r_C)] + [D'_{\max} R (D'_{\max} R + r_C)]} \tag{2.26}$$

2.3.4 Effect of parasitics

Even though the parasitics of the converter are almost constant during operation,

Table 2.2: Effect of parasitics on steady state performance

Parasitic element (If it increases)	D_{max}	V_{omax}
Source resistance (r_g)	Decreases	Decreases
Inductor ESR (r_L)	Decreases	Decreases
Diode resistance (r_d)	No effect	No effect
Capacitor ESR (r_c)	Negligible effect	Slightly decreases
Switch resistance (r_{on})	Slightly decreases	Slightly decreases
Diode forward drop voltage (V_{fd})	No effect	No effect

they may change when there is temperature changes because of long term operation of converter or external means. However, Figure 2.5 shows the effect of parasitics on duty cycle versus output voltage characteristics while keeping input voltage and load resistances as constant. These observations have been tabulated in Table 2.2.

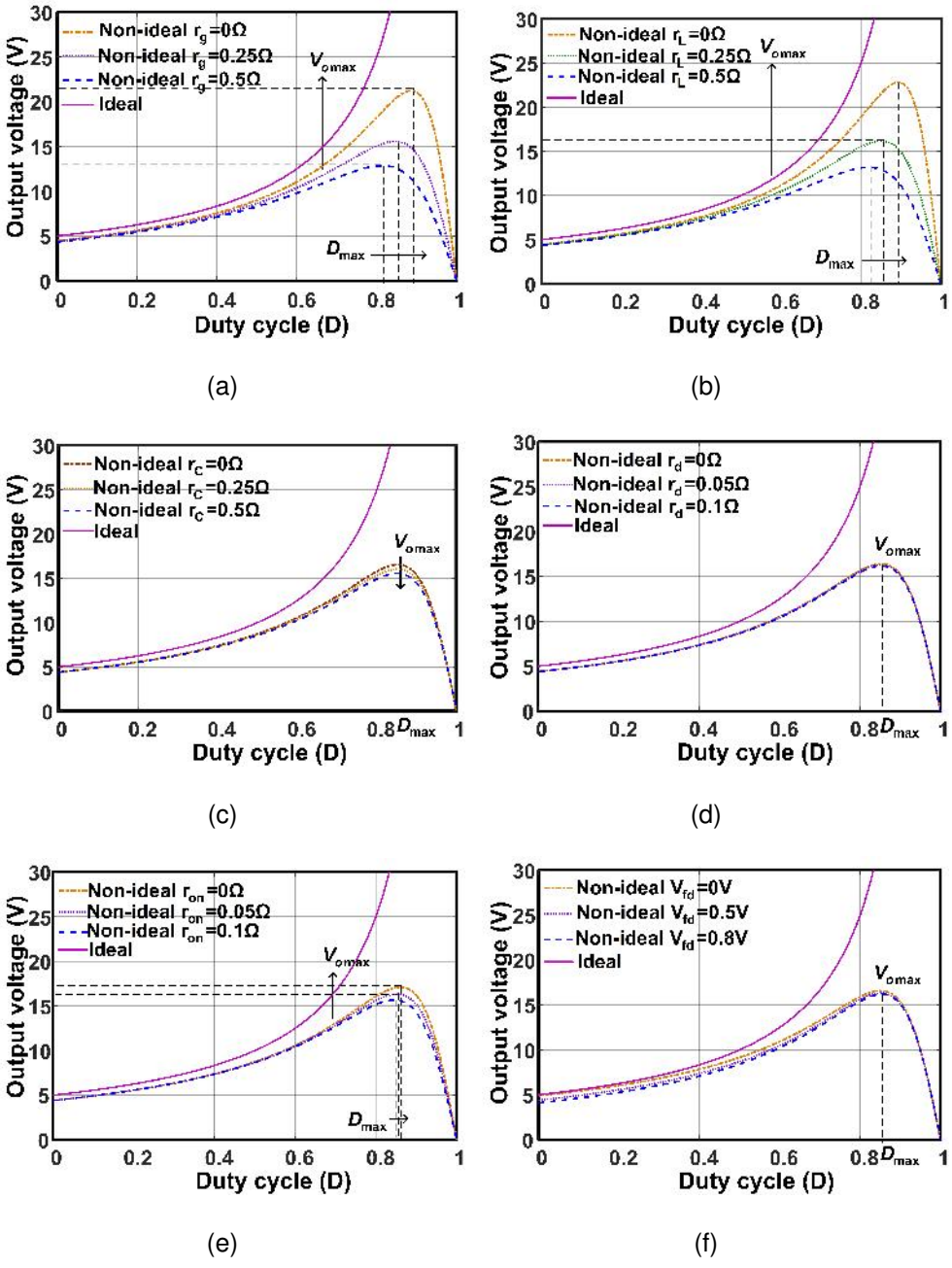


Figure 2.5: Output voltage of boost converter as a function of duty cycle (a) for variation in source resistance (b) for variation in inductor resistance (c) for variation in ESR of capacitor (d) for variation in diode resistance (e) for variation in switch on resistance (f) for different diode forward drop voltages.

2.4 Outcomes for Closed-loop Control

Finally from steady-state analysis, we obtain some important conclusions for closed-loop operation of converter as follows:

1. Output voltage of a practical converter is always less than the ideal. So, to get the exact value in both theoretical and practical cases, the improved duty cycle expression is very important.

2. If the design parameters are known, then with this analysis we can find the values of V_{omax} and D_{max} with the converter, which plays pivotal role in closed-loop operation.

3. Usually in closed-loop operation, the duty cycle of a boost converter will be adjusted to increase, if the output voltage decreases with the change in load or input voltage. When this change is large, then the converter may operate in unstable region as shown in Figure 2.2, which leads to output voltage collapse. So to avoid this, limit the controller output to some finite value K as shown in Figure 2.6.

$$K = D_{max} \tag{2.27}$$

where, $D_{max} < 1$ and the accurate expression for D_{max} is given in (2.25).

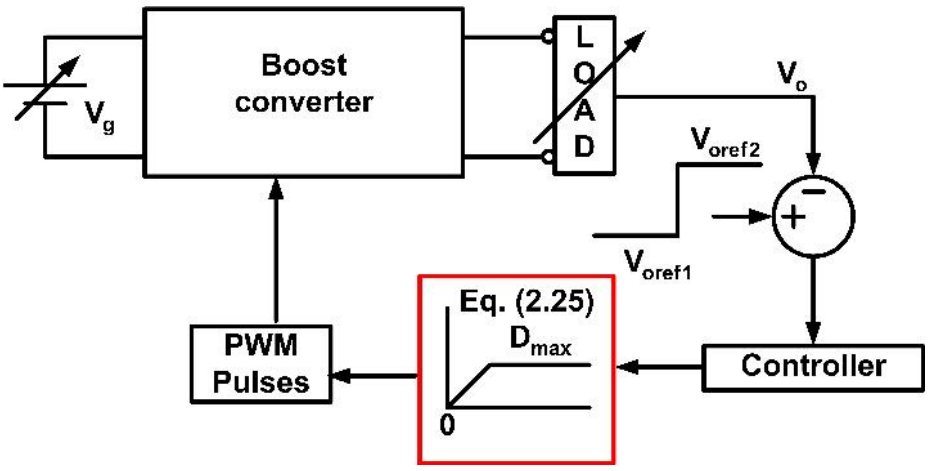


Figure 2.6: Output voltage of boost converter as a function of duty cycle for a fixed output voltage when both input voltage and load resistance are varying.

4. By this analysis, the key information of input voltage range specification V_{gmin} of the converter is observed at a constant output voltage.

5. From Table 2.2 and Figure 2.5, it is clear that the input and inductor resistances are effecting characteristics significantly as compare to other parasitics. From this, we can conclude that while designing converter, these parameters values should be low.

The following illustrative examples will explain the details of above discussed outcomes:

Example 1: Consider the closed-loop operation of boost converter to achieve steady state output value of 25V. Here we analyse the importance of ideal and non-ideal operation. Consider the parameters as given in Table 2.1.

First consider the ideal operation. Since the elements are ideal, parasitics are neglected. Now, we check whether the duty cycle is in the range or not. From (2.19), duty cycle is calculated as $D_{ideal} = 0.8$. So, by operating converter in closed-loop with proper controller values, steady state output is achievable. Now consider the non-ideal operation, since parasitics are present in the elements practically. From (2.22), duty cycle obtained as imaginary value, which shows that the given steady state output is not achievable with this converter. Also from Figure 2.2, it is clear that the maximum achievable voltage is around 16.3 V. So, even if we operate in closed-loop we cannot achieve the steady state output as 25 V, which is contradictory result from the ideal operation. So, this critical information of maximum achievable voltage (V_{omax}) with the converter is necessary before operating it in a closed-loop.

Example 2: Consider the closed-loop operation of boost converter to achieve steady state output value of 8.3V. Suppose input voltage or reference voltage is varying, then how to design closed-loop control? Consider the parameters as given in Table 2.1.

As we have seen in example 1, $V_{omax} = 16.3$V, so the output value mentioned in the problem is achievable. For this converter, $D_{max} = 0.85$ for $R = 22\Omega$ and $V_g = 5$V. To achieve $V_o = 8.33$V in open loop $D_{req} = 0.475$ required, which shows $D_{req} <$

D_{max}. Suppose in first case, the input voltage started decreasing gradually, then accordingly duty cycle of the boost converter will increase (up to D_{max}) to achieve the steady state output. In second case, input voltage or reference voltage changes suddenly, then error is large. So to minimize this error, the duty cycle may increase to unity for instant. This will collapse the output voltage. To avoid this, the duty cycle should be limited to D_{max}. Here in both cases, the input voltage is allowed to decrease up to $V_{gmin} = 2.6$V only, which is clearly observable from Figure 2.4. This will show the importance of analysis (*i.e.,* knowledge of D_{max}, V_{gmin}) for the closed-loop operation, when sudden changes occur.

2.5 Design of Filter Elements

2.5.1 Inductor current ripple (ICR) and Inductor design

Design of inductor is an another important issue for boost converter. Generally, inductance value mostly depends on the ICR (Δi_L) and switching frequency. So, in this section, the effect of non-idealities is analysed on inductors design and inductor ripple current. Let x_L be inductor current ripple factor (ICRF) for inductor L, such that

$$x_L = \frac{\Delta i_L}{I_L}. \tag{2.28}$$

Here, I_L is average current through inductor L.

From (2.3), the rate of change of inductor current i_L can be assumed constant over one cycle in steady-state *i.e.,*

$$\frac{\Delta i_L}{\Delta t} = \frac{V_g - I_L(r_g + r_L + r_{on})}{L} \tag{2.29}$$

For ON-period $\Delta t = DT$, the steady state magnitude of ripple current Δi_L can be written as

$$\Delta i_L = \frac{V_g - I_L(r_g + r_L + r_{on})}{L} DT \tag{2.30}$$

Substituting value of I_L from (2.14) and simplifying,

$$\Delta i_L = \frac{DV_o}{Lf}\left[\frac{V_g}{V_o} - \frac{r_g + r_L + r_{on}}{RD'}\right] \tag{2.31}$$

Here $f = \frac{1}{T}$ is the switching frequency of boost converter. Equation (2.18) can be written as,

$$\frac{V_g}{V_o} = D' \left[\frac{V_{fd}}{V_o} + \frac{1}{R} \left[\frac{1}{(D')^2} (r_g + r_L + r_{on}) + \frac{1}{D'} (r_d - r_{on}) \right] + \frac{1 + \frac{r_C}{D'R}}{1 + \frac{r_C}{R}} \right] \tag{2.32}$$

Substitute (2.32) in (2.31), we get,

$$\Delta i_L = \frac{DD'V_o}{Lf} \left[\begin{array}{l} \frac{V_{fd}}{V_o} + \frac{1}{R} \left[\begin{array}{l} \frac{1}{(D')^2}(r_g + r_L + r_{on}) \\ + \frac{1}{D'}(r_d - r_{on}) \end{array} \right] + \frac{1 + \frac{r_c}{RD'}}{1 + \frac{r_c}{R}} - \frac{r_g + r_L + r_{on}}{R(D')^2} \end{array} \right] \tag{2.33}$$

Further simplifying, we get ICR expression as

$$\Rightarrow \Delta i_L = \frac{DD'V_o}{Lf} \left(\frac{V_{fd}}{V_o} + \frac{r_d - r_{on}}{RD'} + \frac{1 + \frac{r_c}{RD'}}{1 + \frac{r_c}{R}} \right) \tag{2.34}$$

or

$$\Delta i_L = \Delta i_{Lideal} \left(\frac{V_{fd}}{V_o} + \frac{r_d - r_{on}}{RD'} + \frac{1 + \frac{r_c}{RD'}}{1 + \frac{r_c}{R}} \right) \tag{2.35}$$

Substituting $\Delta i_L = x_L I_L = x_L \frac{V_o}{RD'}$ into Eq. (2.34), we get the expression for inductor L as

$$L = \frac{DR\left(D'\right)^2}{x_L f} \left(\frac{V_{fd}}{V_o} + \frac{r_d - r_{on}}{RD'} + \frac{1 + \frac{r_c}{RD'}}{1 + \frac{r_c}{R}} \right) \tag{2.36}$$

or

$$L = L_{ideal} \left(\frac{V_{fd}}{V_o} + \frac{r_d - r_{on}}{RD'} + \frac{1 + \frac{r_c}{RD'}}{1 + \frac{r_c}{R}} \right) \tag{2.37}$$

Putting the values of all non-ideal elements to zero in Eq. (2.34) and (2.36), these expressions become

$$\Delta i_{Lideal} = \frac{DD'V_o}{Lf} \tag{2.38}$$

$$L_{ideal} = \frac{DR\left(D'\right)^2}{x_L f} \tag{2.39}$$

From Eq. (2.38) and (2.39), we can observe that these are same as given in various textbooks to calculate the inductor current ripples and inductance value. However, Eq. (2.36) and (2.34) provide the actual value of inductance L and ripple expression to limit the current ripples within specified range in presence of non-idealities.

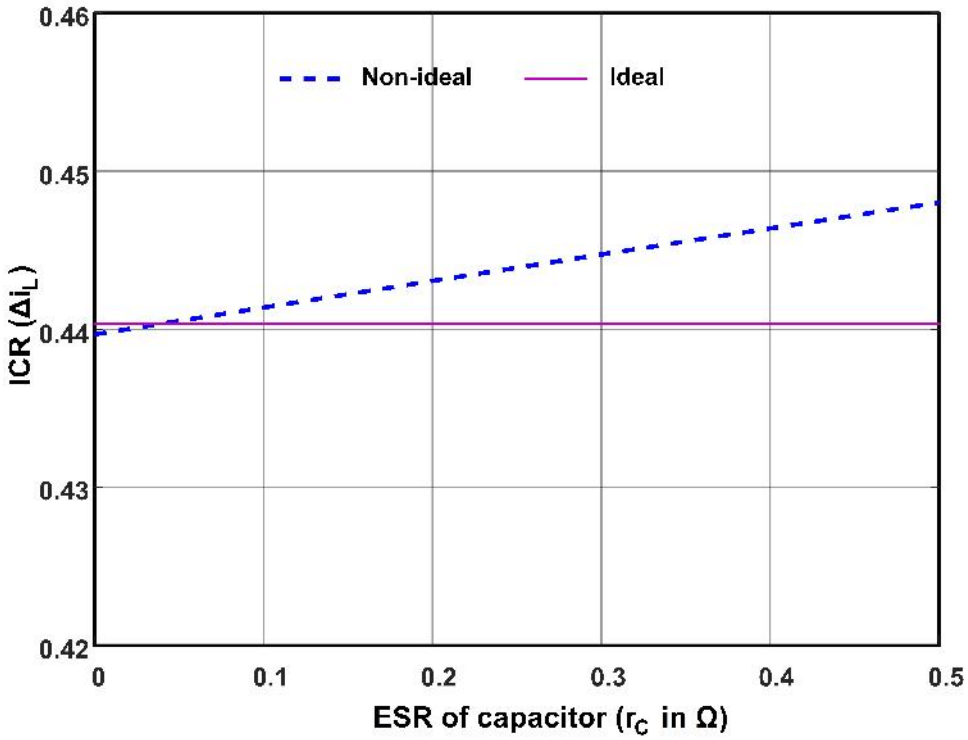


Figure 2.7: ESR of capacitor effect on ICR.

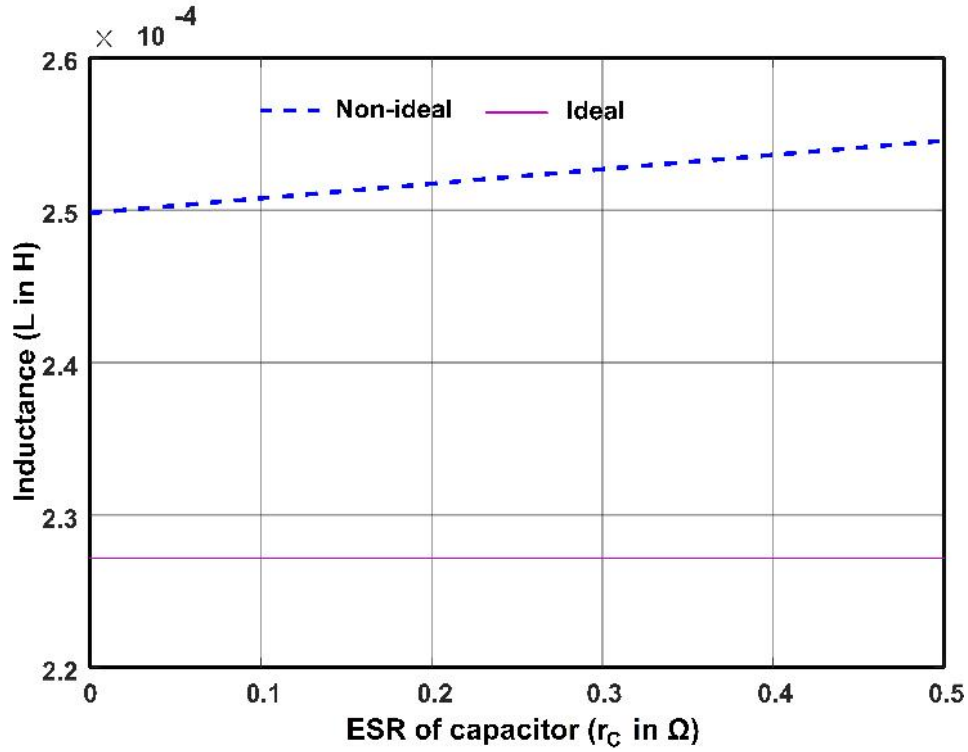


Figure 2.8: ESR of capacitor effect on Inductance.

2.5.1.1 Effect of parasitics on ICR and inductance

The expressions (2.37) and (2.35) shows that there is a additional multiplying factor to the ideal expressions. Here, an important observation from non-ideal design is that the value of inductance and ICR are mainly effected by the ESR of the capacitor though there are other parasitics also present. The plots between ESR of the capacitor versus ICR and inductance are shown in Figures. 2.7 and 2.8. From these figures, it is observed that as the capacitor ESR increases, the ICR increases and the inductance required also increases.

2.5.2 Design of Capacitor

Capacitor design is also the very important as inductor design for a boost converter. The voltage across the capacitor will be taken as output voltage in boost converter. Therefore, the capacitor design depends on the allowable OVR and switching frequency. The equivalent series resistance (ESR) of a capacitor plays an important role in design. A capacitor is modelled by its capacitance value and ESR value. In order to design capacitance, the OVR analysis of capacitor is needed.

2.5.2.1 OVR analysis

In any DC-DC converter, the total voltage ripple (Δv_o) of a capacitor is sum of

- Voltage ripples due to its own capacitance (Δv_C)
- Voltage ripples due to its ESR (Δv_{rC}).

Therefore, for proper capacitor design, it becomes necessary to consider the effect of ESR. The capacitor C is used as filter capacitor at output stage. The voltage ripples across this capacitor directly affect the quality of output voltage. Therefore, its design is carried out more carefully to limit the output voltage ripples within permissible range.

The capacitor current and different components of voltage ripples in steady state are shown in Figure 2.9. In this figure, it can be observed that the maximum ripple occurs during OFF time. This is because, during ON time of converter, capacitor supplies power to load or discharges and during OFF time capacitor charges for

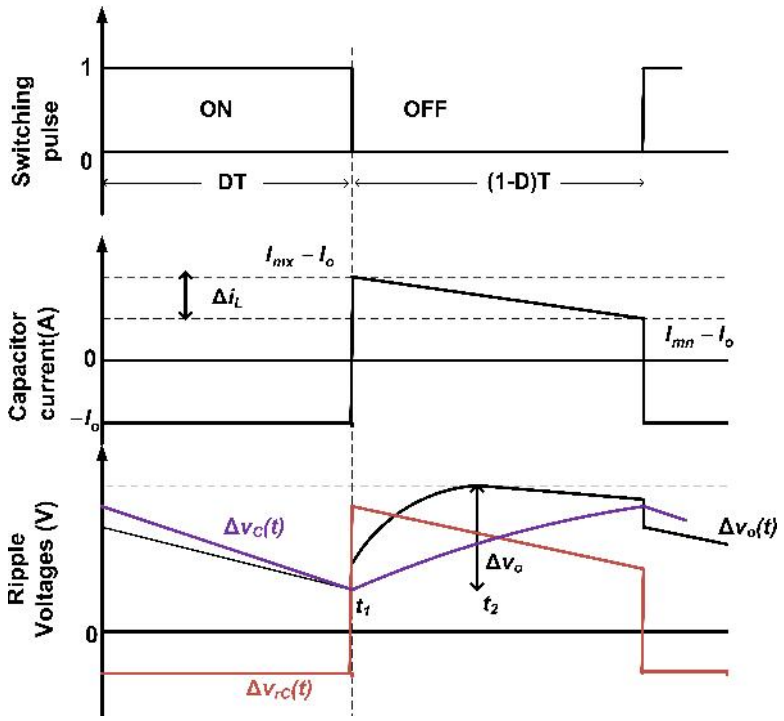


Figure 2.9: Current and ripple voltage waveforms associated with capacitor C.

some time period, reaches maximum and starts discharges (*i.e.,* after some time period $I_L < I_o$, which means capacitor supplies power to load). As discussed earlier, output voltage ripple $\Delta v_o(t)$ is made up of two components as

$$\Delta v_o(t) \simeq \Delta v_C(t) + \Delta v_{rC}(t) \tag{2.40}$$

Voltage ripples due to ESR, $\Delta v_{rC}(t)$, expressed as

$$\Delta v_{rC}\,(t) = r_c i_C\,(t) \tag{2.41}$$

Voltage ripples due to capacitor, $\Delta v_C(t)$ expressed as

$$\Delta v_C\,(t) = \frac{1}{C}\int_0^t i_C\,(t)dt + \Delta v_C\,(t_0) \tag{2.42}$$

$\Delta v_C(t_0)$ is initial voltage across capacitor at $t = t_0$.

The detailed analysis is carried out as follows:

2.5.2.2 Analysis during ON time

The current through capacitor C is

$$i_c(t) = -I_o \tag{2.43}$$

Therefore, the voltage ripple contribution due to capacitor ESR is

$$\Delta v_{rC}(t) = r_c i_C(t) = -I_o r_c \tag{2.44}$$

The voltage ripple contribution due to capacitor itself is

$$\Delta v_C(t) = \frac{1}{C}\int_0^t i_C(t)dt + \Delta v_C(0) = -\frac{I_o}{C}t + \Delta v_C(0) \tag{2.45}$$

$\Delta v_C(0)$ is initial voltage across capacitor at $t = 0$. Therefore, total output voltage ripple during switch ON is

$$\Delta v_o(t) = \Delta v_C(t) + \Delta v_{rC}(t) = -\frac{I_o}{C}[t + Cr_c] + \Delta v_C(0) \tag{2.46}$$

From Eq. (2.46), it is clear that $\Delta v_o(t)$ is a line equation which is shown in Figure 2.9 also. It has a minimum value at $t_1 = DT$. At $t = t_1$, the voltage ripples obtained as

$$\Delta v_{rc}(t_1) = -I_o r_c \tag{2.47}$$

$$\Delta v_C(t_1) = -\frac{I_o DT}{C} + \Delta v_C(0) \tag{2.48}$$

$$\Delta v_{o,\min} = \Delta v_o(t_1) = -\frac{I_o}{C}[Cr_c + DT] + \Delta v_C(0) \tag{2.49}$$

2.5.2.3 Analysis during OFF time

In this duration, the capacitor current dynamics is

$$i_C(t) = \frac{-\Delta i_L(t - DT)}{D'T} + I_{mx} - I_o \tag{2.50}$$

Therefore, the voltage ripple contribution due to capacitor ESR is

$$\Delta v_{rC}(t) = r_c i_C(t) = -\frac{\Delta i_L r_c}{D'T}(t - DT) + (I_{mx} - I_o) r_c \tag{2.51}$$

The voltage ripple contribution due to capacitor itself is

$$\Delta v_C(t) = \frac{1}{C}\int_{DT}^t i_C(t)dt + \Delta v_C(DT) = -\frac{\Delta i_L (t-DT)^2}{2CD'T} + \frac{(I_{mx}-I_o)(t-DT)}{C} + \Delta v_C(DT) \tag{2.52}$$

$\Delta v_C(DT)$ is initial voltage across capacitor at $t = DT$.

Therefore, total output voltage ripple during switch-off is

$$\Delta v_o\left(t\right) = \Delta v_C\left(t\right) + \Delta v_{rC}\left(t\right) = -\frac{\Delta i_L}{D'T}\left[\frac{(t-DT)^2}{2C} + r_c\left(t - DT\right)\right] + \frac{(I_{mx}-I_o)}{C}\left(Cr_c + (t - DT)\right) + \Delta v_C\left(DT\right) \tag{2.53}$$

The time t_2 at which value of $\Delta v_o(t)$ occurs maximum during switch-off is obtained by differentiating (2.53) w.r.t time and equating it to zero as,

$$\frac{\partial \Delta v_o}{\partial t} = 0 \tag{2.54}$$

Further simplifying, we get,

$$t_2 = DT - Cr_c + \frac{(I_{mx} - I_o)}{\Delta i_L} D'T \tag{2.55}$$

Now, by substituting (2.55) in (2.51), we get,

$$\Delta v_{rc}(t_2) = \frac{\Delta i_L\left(Cr_c^2\right)}{CD'T} \tag{2.56}$$

By substituting (2.55) in (2.52), we get,

$$\Delta v_C(t_2) = \frac{(I_{mx} - I_o)^2 D'T}{2C\Delta i_L} - \frac{\Delta i_L\left(Cr_c^2\right)}{2CD'T} + \Delta v_C(DT) \tag{2.57}$$

and the maximum value of output voltage ripples are obtained by substituting (2.55) in (2.53), we get,

$$\Delta v_{o,\max} = \Delta v_o\left(t_2\right) = \frac{\Delta i_L}{2CD'T}\left(\left(\left(I_{mx} - I_o\right)\frac{D'T}{\Delta i_L}\right)^2 + \left(Cr_c\right)^2\right) + \Delta v_C\left(DT\right) \tag{2.58}$$

Therefore, the total peak-to-peak voltage ripple will be

$$\Delta v_o = \Delta v_o\left(t_2\right) - \Delta v_o\left(t_1\right) \tag{2.59}$$

Substituting from (2.49), (2.58), we get,

$$\Delta v_o = \frac{\Delta i_L f}{2CD'}\left(\left(\left(I_{mx} - I_o\right)\frac{D'}{\Delta i_L f}\right)^2 + \left(Cr_c\right)^2\right) + I_o r_c \tag{2.60}$$

If non-idealities are zero, then Eq. (2.60) becomes:

$$\Delta v_o = \frac{V_o DT}{RC} \tag{2.61}$$

The above simplification in detail given in *Appendix B*.

2.5.3 Effect of ESR on OVR

The voltage ripple contribution of ESR and capacitor in peak-peak OVR can be obtained as follows:
The OVR due to ESR is

$$\Delta v_{rC} = \Delta v_{rC}\left(t_2\right) - \Delta v_{rC}\left(t_1\right) \tag{2.62}$$

Substituting Equations (2.47) and (2.56) in (2.62), we get,

$$\Delta v_{rc} = \frac{\Delta i_L\left(Cr_c^2\right)}{CD'T} + I_o r_c \tag{2.63}$$

Similarly, the OVR due to capacitor is

$$\Delta v_C = \Delta v_C\left(t_2\right) - \Delta v_C\left(t_1\right) \tag{2.64}$$

Substituting Equations (2.48) and (2.57) in (2.64), we get,

$$\Delta v_C(t_2) = \frac{(I_{mx}-I_o)^2 D'T}{2C\Delta i_L} - \frac{\Delta i_L\left(Cr_c^2\right)}{2CD'T} \tag{2.65}$$

The expressions (2.63) and (2.65) shows that OVR is the sum of two individual OVR's. The voltage ripple obtained by the expressions Equation (2.60), Equation (2.63) and Equation (2.65) are plotted in Figure 2.10 with the variation of ESR (r_c). From this Figure, with an increase in ESR, Δv_{rc} increases at a faster rate than Δv_C decreases, thereby causing a net increase in Δv_o. However, as the value of r_c increases beyond $r_{c,\max}$, Δv_{rc} becomes higher than Δv_o, which is practically impossible. This result implies that the capacitor is no longer able to keep OVR within the specified limit for $r_c > r_{c,\max}$. So from Figure 2.10, ripple provided by capacitor is obtained as negative (for $r_c > r_{c,\max}$), which can be observed from (2.65).

2.5.4 Output capacitor design

Let the maximum specified output voltage ripple be Δv_{om}. Therefore, the value of capacitor C should be chosen such that

$$\Delta v_o \leq \Delta v_{om} \tag{2.66}$$

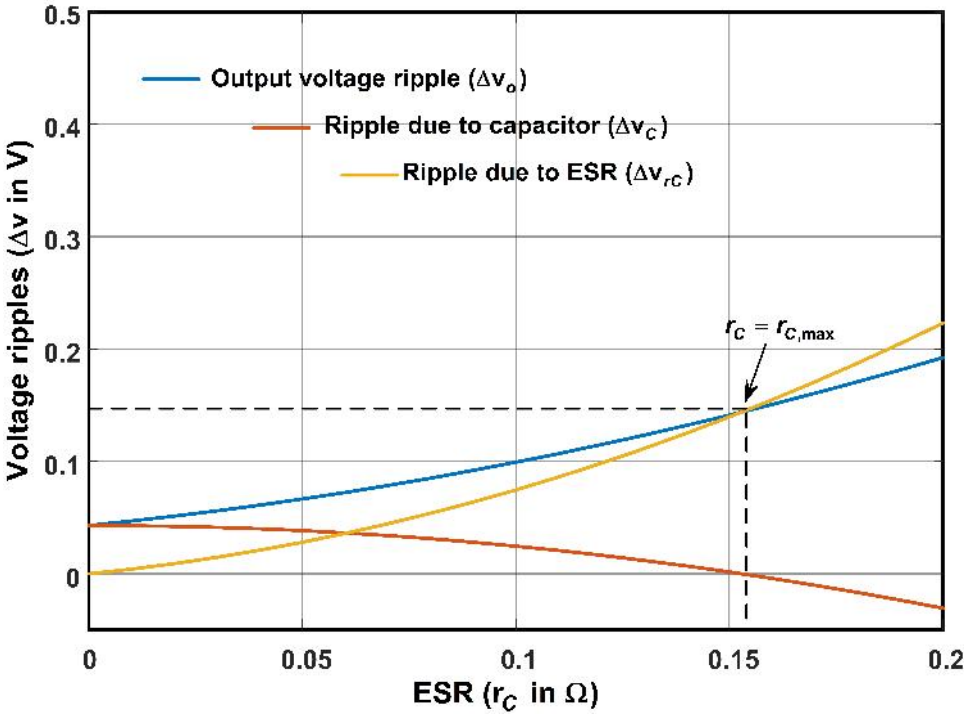


Figure 2.10: Different voltage ripple variation with ESR.

Substitute value of Δv_o from (2.60), we get,

$$\frac{(I_{\max}-I_o)^2\left(D'T\right)^2+(\Delta i_L C r_C)^2+2I_o\Delta i_L C r_C D'T}{2\Delta i_L C D'T}\leq \Delta v_{om} \tag{2.67}$$

By solving the above inequality, we get,

$$C^2r_C^2-C\left[\frac{2D'}{f}\left(\frac{\Delta v_{om}-I_o r_C}{\Delta i_L}\right)\right]+\frac{(I_{\max}-I_o)^2\left(D'T\right)^2}{(\Delta i_L)^2}\leq 0 \tag{2.68}$$

The above expression is quadratic in C and solution is the minimum value of filter capacitor C for given OVR and ICR can be obtained as follows:

$$C_{mn}=\frac{D'}{fr_c^2}\left[\frac{\Delta v_{om}-I_o r_c}{\Delta i_L}\pm\sqrt{\left(\frac{\Delta v_{om}-I_o r_c}{\Delta i_L}\right)^2-\left(\frac{I_{mx}-I_o}{\Delta i_L}\right)^2 r_c^2}\right] \tag{2.69}$$

This expression is valid for $r_C \leq r_{C,max}$. The variation in minimum value of capacitance as a function of ESR is drawn in Figure 2.11.From this figure, it is evident that the required capacitor value increases with increase in ESR and after $r_c = r_{c,\max}$, it is not possible to maintain the output voltage ripple constraint as shown in (2.66).

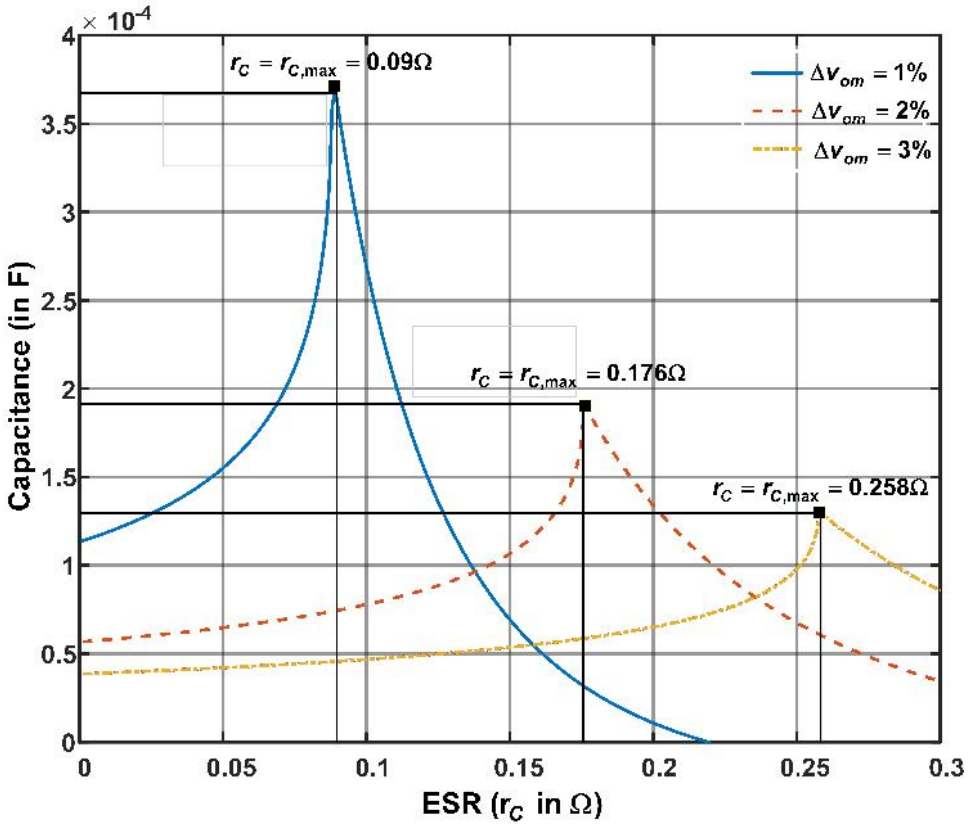


Figure 2.11: Capacitance variation with ESR.

2.5.5 Maximum permissible ESR ($r_{C,max}$) and ICR effect

As discussed in previous section, the ESR of output capacitor C plays an important role in OVR of boost converter. As the value of ESR increases, more ripples appear in output voltage, degrading the output voltage quality. Therefore, it is necessary to find out the maximum permissible value of ESR for maximum specified OVR.

In Eq. (2.69), Capacitor C will have a real value (practically feasible) only if the terms inside the root is greater than or equal to zero, *i.e.,*

$$\left(\frac{\Delta v_{om} - I_o r_c}{\Delta i_L}\right)^2 - \left(\frac{I_{mx} - I_o}{\Delta i_L}\right)^2 r_c^2 \geq 0 \tag{2.70}$$

On simplification,

$$r_c \leq \frac{\Delta v_{om}}{I_{mx}} \tag{2.71}$$

Therefore, the maximum permissible value of ESR ($r_{c,\max}$) for specified output volt-

age ripple and inductor current ripple can be defined as

$$r_{c,\max} = \frac{\Delta v_{om}}{I_{mx}} \tag{2.72}$$

If the ESR value of the output capacitor is greater than the $r_{c,\max}$, then the output

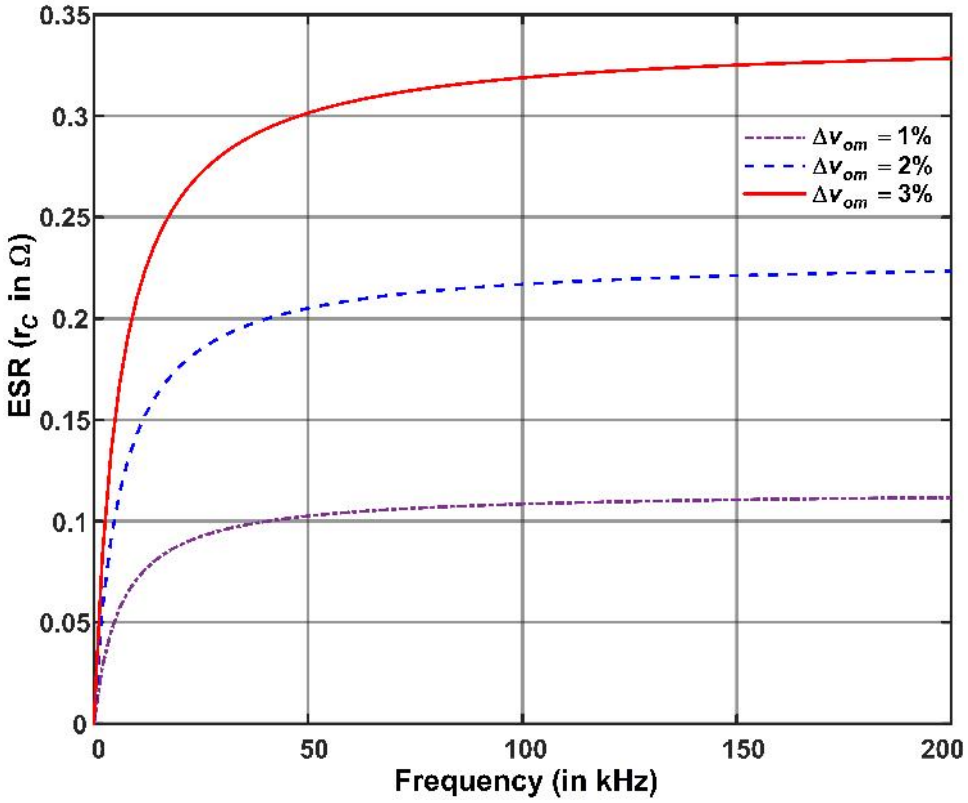


Figure 2.12: ESR vs frequency.

voltage ripple will exceed the maximum defined limit. Further sections, this can be observed by simulation and experimental results.

Further, Eq. (2.72) can be written as,

$$r_{c,\max} = \frac{\Delta v_{om}}{\frac{DV_o}{2Lf}\left[\frac{V_g}{V_o} - \frac{r_g + r_L + r_{on}}{D'R}\right] + I_L} \tag{2.73}$$

This relation (2.73), shows that for specified output voltage ripple, the maximum permissible value of ESR ($r_{c,\max}$) is not proportional to switching frequency. Figure 2.12 shows the variation in $r_{c,\max}$ with switching frequency. From this, it is observed that, as the switching frequency of converter increases, the power supply designer

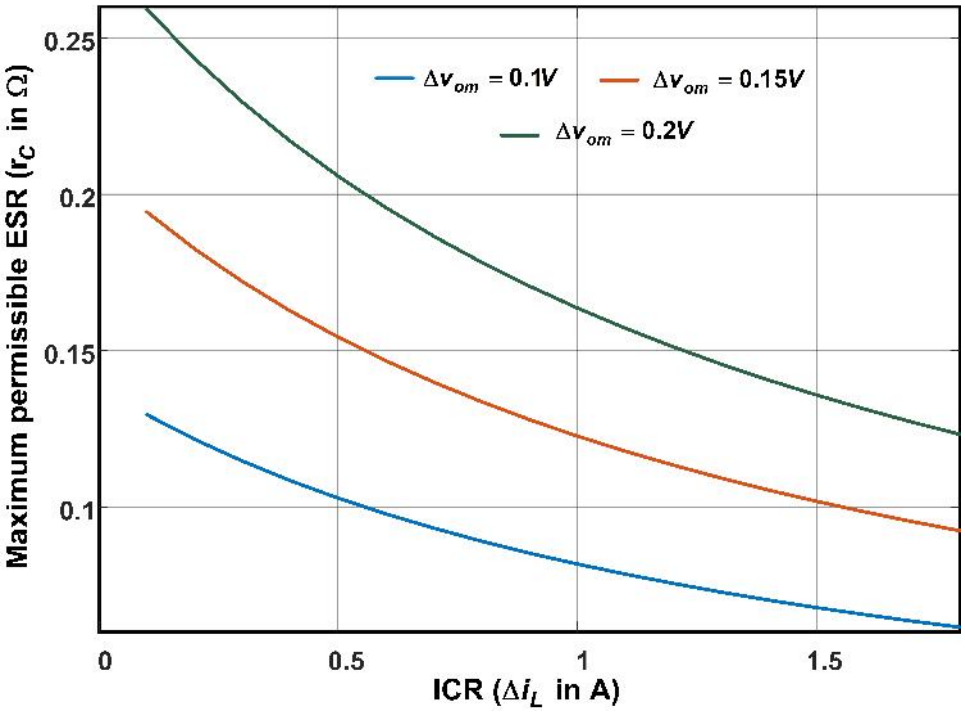


Figure 2.13: Maximum permissible ESR vs ICR.

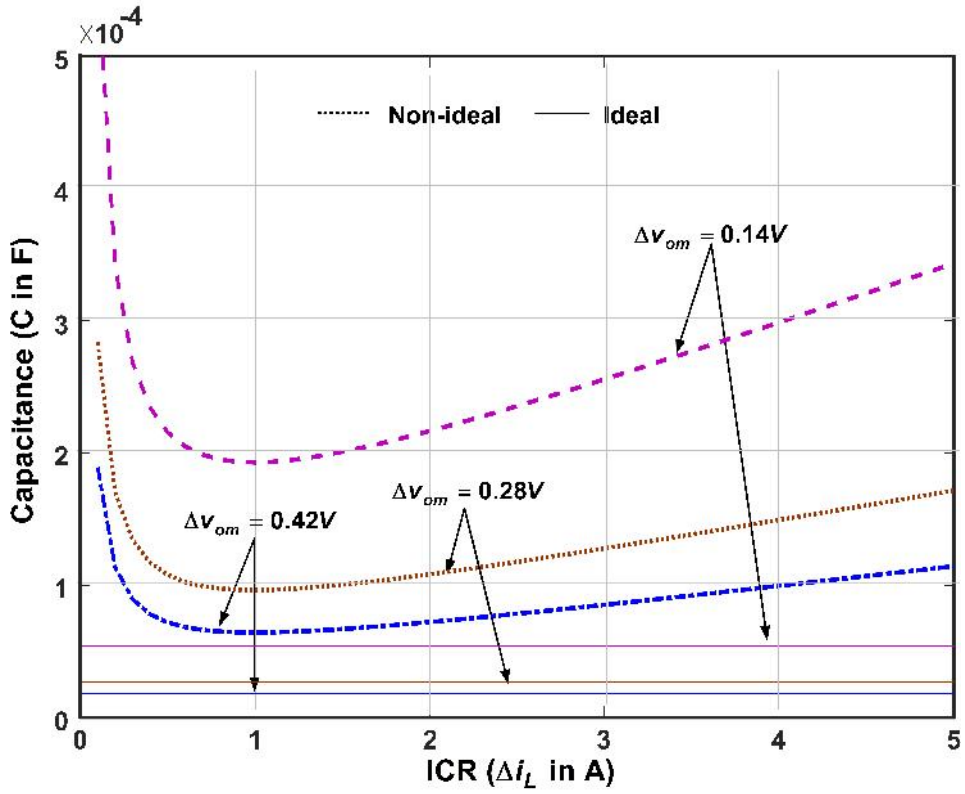


Figure 2.14: Effect of ICR on capacitance.

should use some specific value of ESR capacitor for the mentioned output voltage ripple constraint. It is also to note that as frequency increases, required capacitor value also decreases.

Substituting value of $r_{C,\max}$ from Eq. (2.72) into (2.69), the minimum value of output capacitor in worst case is

$$C_{mn} = \frac{D' I_{mx} \left(I_{mx} - I_o \right)}{\Delta i_L \Delta v_{om} f} \tag{2.74}$$

From Eq. (2.72), it is clear that maximum permissible ESR depends on the ICR. From this relation, we can observe that maximum permissible ESR will increase as the ICR decreases for a prescribed OVR which is shown in Figure 2.13. From Eq. (2.74), it is observed that the capacitance value depends on the ICR. The plot between capacitance required versus ICR for different specified OVR is shown in Figure 2.14. From figure, it is observed that the capacitor design in boost converter actually depends not only on specified OVR but also the ICR. Further, from ideal analysis, it is observed that capacitance is independent of ICR and only depends on OVR.

2.6 Experimental Results and Discussion

The previous sections analytical findings are validated by simulations and experimental results. The simulations are carried out in MATLAB/Simulink software package whereas for the experimental results, a hardware prototype is developed as shown in Figure 2.15.According to the availability, MOSFET IRFP460 and diode MUR1560 are chosen as semiconductor switching devices. The ferrite core inductors and electrolytic capacitors are used as energy storage elements. The values of various parameters used for simulation and prototype design are given in Table 2.1.

For given specifications, using Eq. (2.1), the ideal duty cycle is calculated as 0.4, whereas the actual duty cycle in presence of non-idealities is calculated as 0.475 using proposed relationship in (2.22). This increased duty cycle is necessary to compensate the voltage drop occurring due to non-idealities. The value of inductor L using ideal formula is 227 μH whereas it is 250 μH using the proposed formula in Eq. (2.36). Therefore, the more inductance is required in the presence of non-

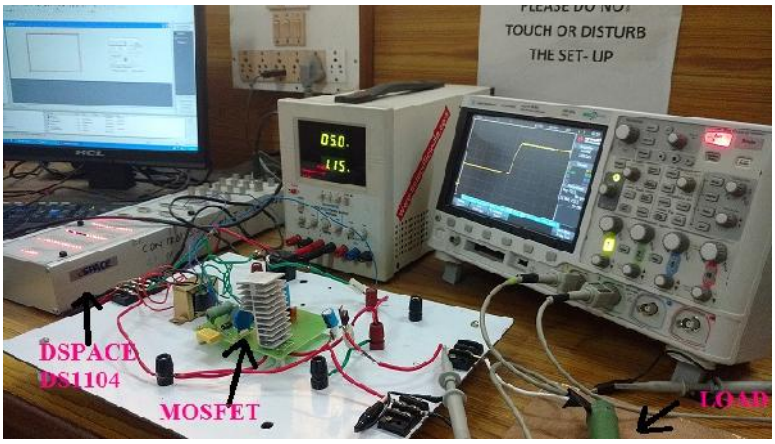


Figure 2.15: Experimental set up of DC-DC boost converter.

idealities. The minimum value of capacitor C is 200μF as calculated by Eq. (2.74). The maximum permissible value of output capacitor ESR ($r_{c,max}$) is calculated as 0.17Ω using Eq. (2.72) to confine the output voltage ripples within 2% of output voltage.

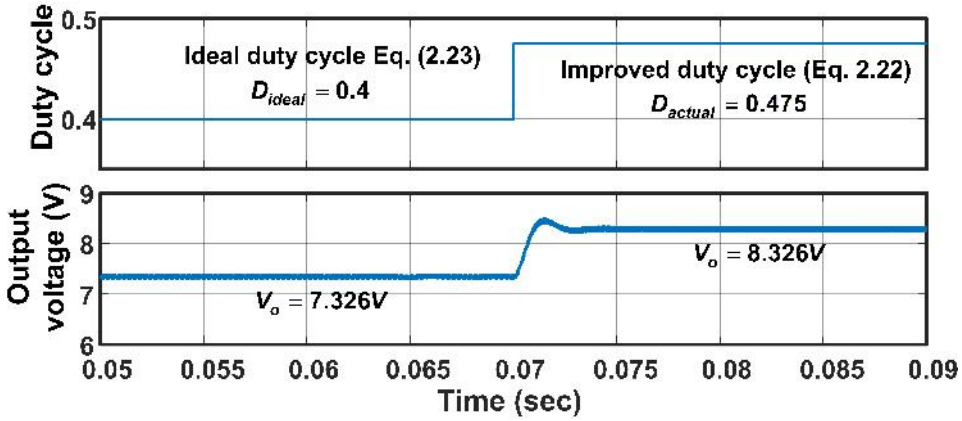


Figure 2.16: Simulation result of output voltage with ideal and modified duty cycle expressions.

The simulated output voltage responses of DC-DC PWM boost converter with ideal duty cycle $D = 0.4$ and actual duty cycle $D = 0.475$ are obtained as shown in Figure 2.16. In steady state, the output voltage magnitude reaches to 7.32V (not 8.33V as desired). On the other hand, it is observed that if the duty cycle is 0.475 as calculated by proposed relationship, the output voltage is 8.33V in steady state. The

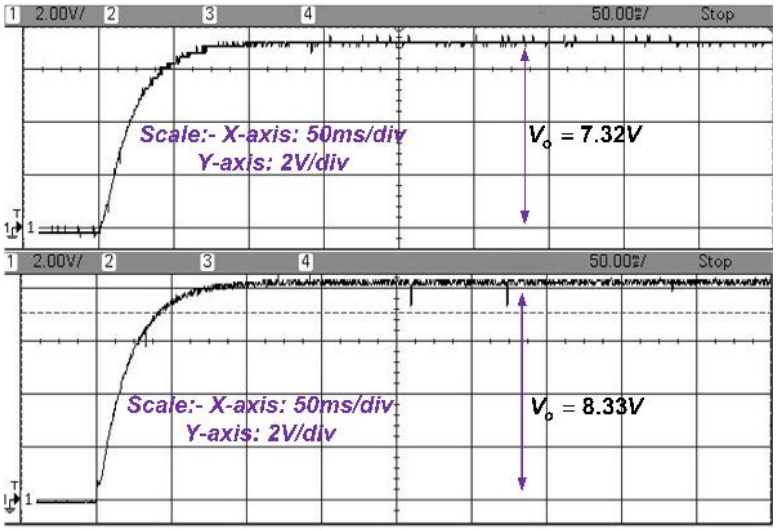


Figure 2.17: Experimental result of output voltage with ideal and modified duty cycle expressions.

corresponding experimental results are shown in Figure 2.17.

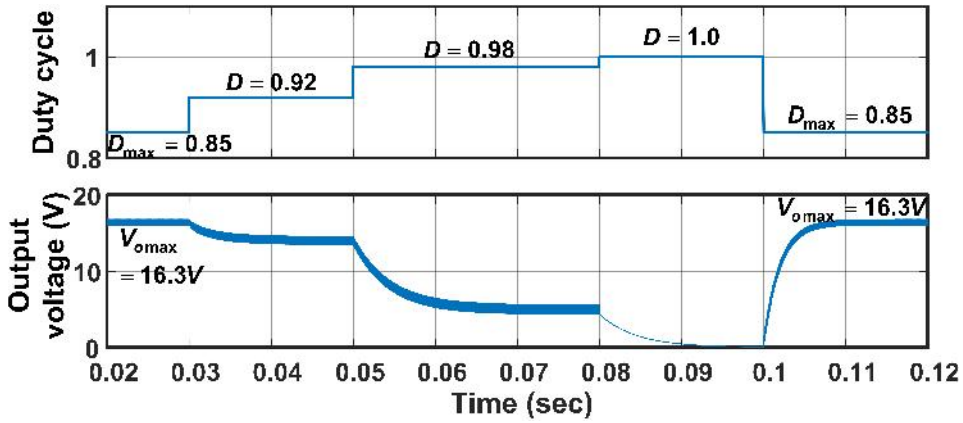


Figure 2.18: Simulation result of output voltage at different duty cycle $D > D_{max}$.

Now, the maximum permissible duty cycle and maximum achievable voltage with the converter are also have been verified by simulation and practically. The maximum possible output voltage (V_{omax}) achieved by the presented converter is 16.3V at $D_{max} = 0.85$, obtained by substituting Eq. (2.25) and (2.26), respectively. The simulation result is shown in Figure 2.18 and experimental result shown in Figure 2.19. Here, as the duty cycle increases above D_{max}, the output voltage start decreasing

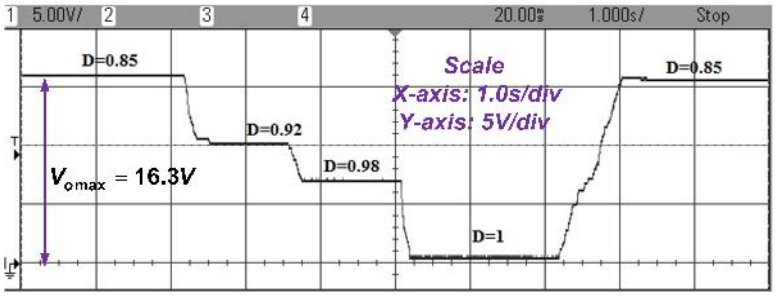


Figure 2.19: Experimental result of output voltage at different duty cycle $D > D_{max}$.

and finally reaches zero at $D = 1$.

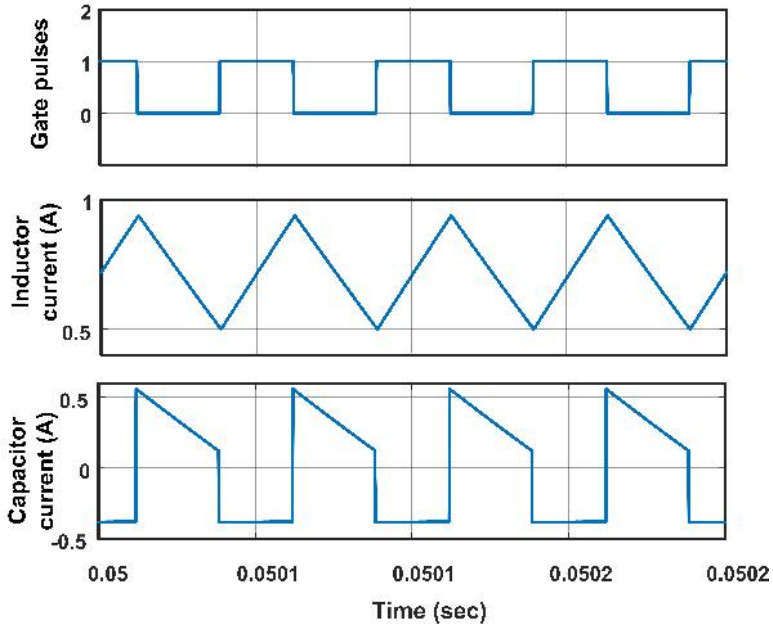


Figure 2.20: Simulation result of Capacitor and inductor current waveforms of converter in open loop operation at duty cycle $D = 0.475$.

The simulation results of inductor current and capacitor current waveforms are shown in Figure 2.20. The experimental results for inductor current and capacitor current are shown in Figure 2.21. The average inductor current (I_L) value is 0.704A and inductor current ripple Δi_L is 0.44A. In experimental results, the current sensor is used for measuring inductor current which has gain of 1.8.

The D_{max} of the converter is calculated from (2.25) as 0.85 and corresponding

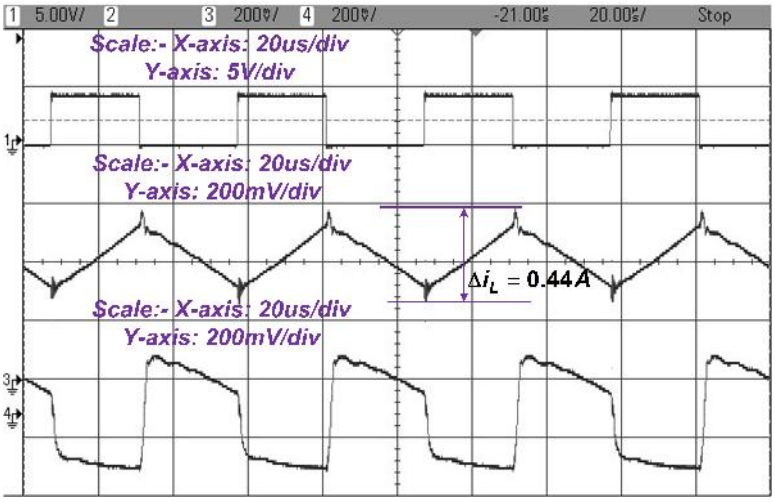
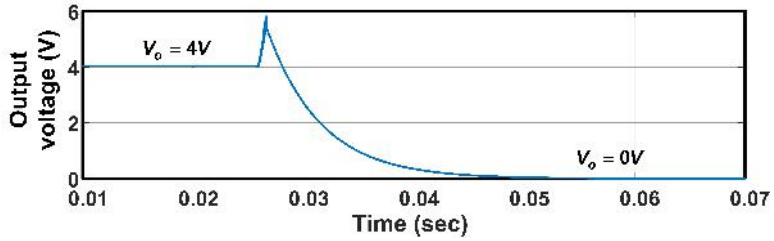
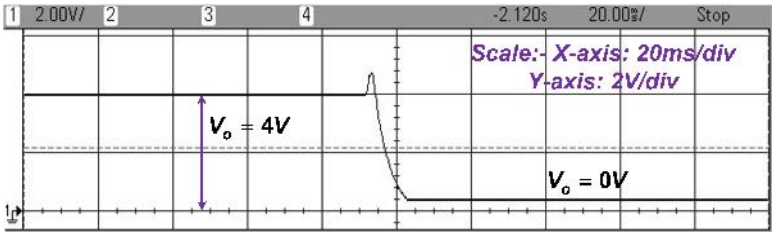


Figure 2.21: Experimental result of Capacitor and inductor current waveforms of converter in open loop operation at duty cycle $D = 0.475$.



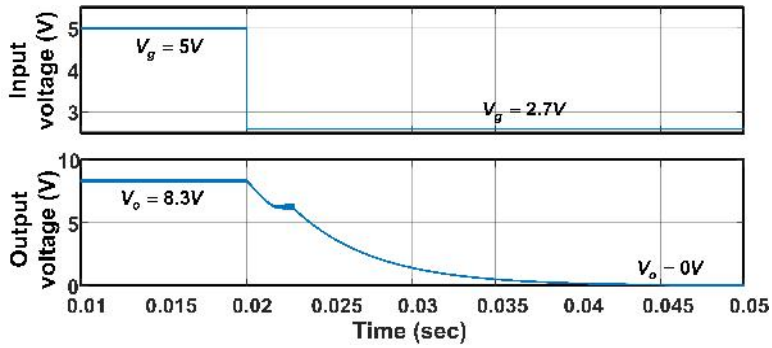
(a)



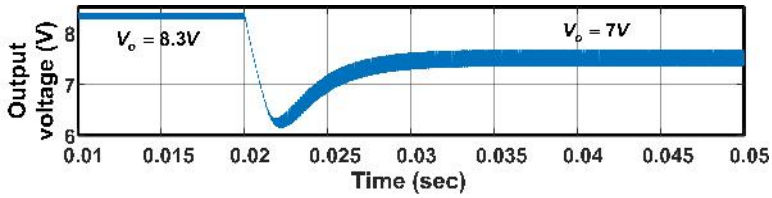
(b)

Figure 2.22: Output voltage in closed-loop operation when $V_{ref} > V_{omax}$ (a)Simulation (b)Experimental.

V_{omax} is 16.3V. From this, we concluded that if $V_{ref} > V_{omax}$, then converter operates in unstable region and output voltage collapse. So, in order to verify this practically, we set $V_{ref} = 17$V, in the closed-loop operation of converter, which resulted in output voltage collapse as shown in Figures 2.22(a) and (b).

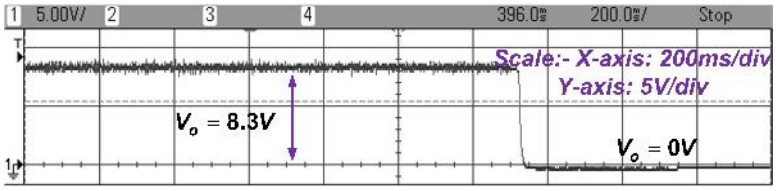


(a)

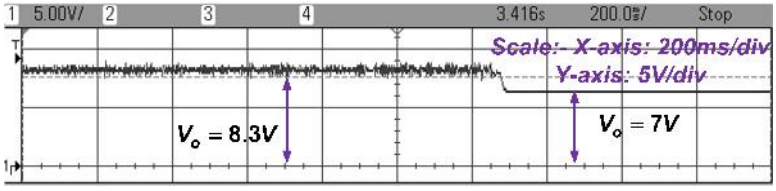


(b)

Figure 2.23: Simulation result of output voltage in closed-loop operation when sudden input voltage change ($V_g < V_{gmin}$) (a)without D_{lim} (b)with D_{lim}.



(a)

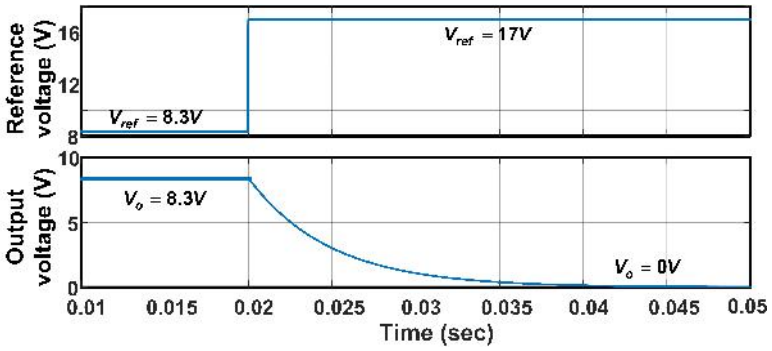


(b)

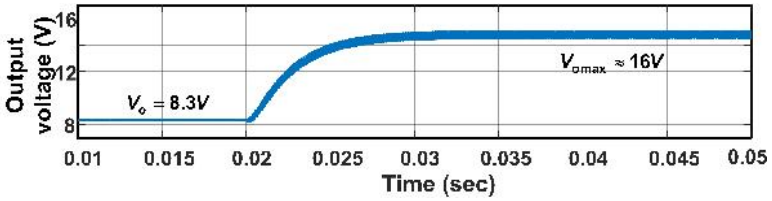
Figure 2.24: Experimental result of output voltage in closed-loop operation when sudden input voltage change ($V_g < V_{gmin}$) (a)without D_{lim} (b)with D_{lim}.

The analysis is also carried out for changes in input voltage and reference voltages. It is suggested that in closed-loop operation, vary the input voltage with in

the range obtained (*i.e.,* $V_g = 2.6$V to 5V) and also to limit the controller output to $D_{max} = 0.85$. In Figure 2.24(a), the output voltage collapses, since input voltage is decreased to $V_g = 2.5$V which is less than the $V_{gmin} = 2.6$V and no limiter is used after the controller. So, $D > D_{max}$ which leads the voltage collapse. In Figure 2.24(b), the output voltage not collapsed, since D_{max} is used as limiter at the controller output. Here the reason is that $D = D_{max}$.



(a)

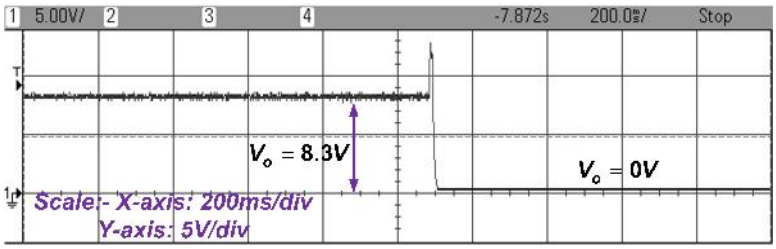


(b)

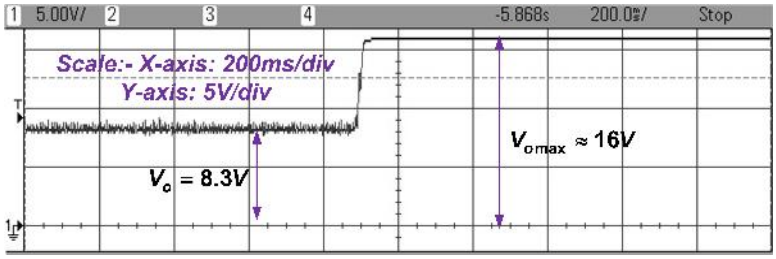
Figure 2.25: Simulation result of output voltage in closed-loop operation when sudden reference voltage change (a)without D_{lim} (b)with D_{lim}.

In Figure 2.25(a) and 2.26(a), the sudden change in reference voltage (*i.e.,* $8V$ *to* $17V$) occurs and limiter has not been used at the controller output, so the output voltage collapsed (*i.e.,*$D > D_{max}$). In Figure 2.25(b) and Figure 2.26(b), the output voltage not collapsed since the controller output is limited to D_{max} (*i.e.,*$D = D_{max}$).

The effect of output capacitor ESR (r_c) on output voltage ripples is also studied. By this study, the importance of determining the maximum permissible ESR ($r_{c,max}$) is highlighted. For this purpose, two different cases ($r_c < r_{c,\max}$ and $r_c > r_{c,\max}$) are



(a)



(b)

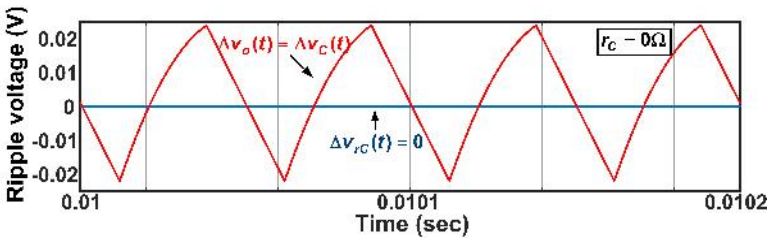
Figure 2.26: Experimental result of output voltage in closed-loop operation when sudden reference voltage change (a)without D_{lim} (b)with D_{lim}.

considered as discussed below-

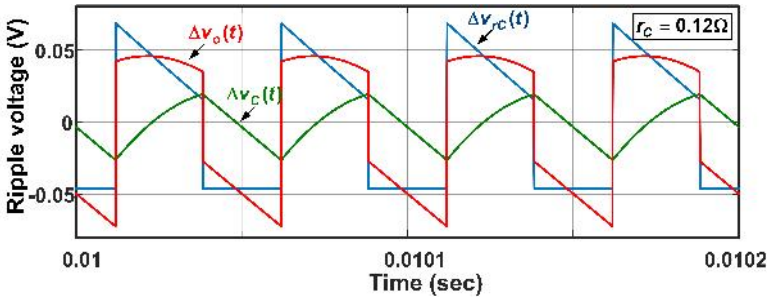
***Case 1 (*$r_c = 0$*)*:** In this case, the ESR of output capacitor (r_c) is 0Ω which is an ideal case. However, this is not possible in practical. The ripple contribution is only because of capacitor itself. The simulated result of output voltage ripples are shown in Figure 2.27(a). These results show that the peak-peak magnitude of output voltage ripple is about 0.04 V.

***Case 2 (*$r_c = 0.12 < r_{c,\max}$*)*:** In this case, the ESR of output capacitor (r_c) is 0.12Ω which is less than the value of maximum permissible ESR. The ripple contribution is not only because of capacitor itself and ESR also. The simulated and experimental waveforms of output voltage ripples are shown in Figure 2.27(b) and 2.28(a), respectively. These results show that the magnitude of output voltage ripple is about 125 mV, which is within desired limit (166 mV).

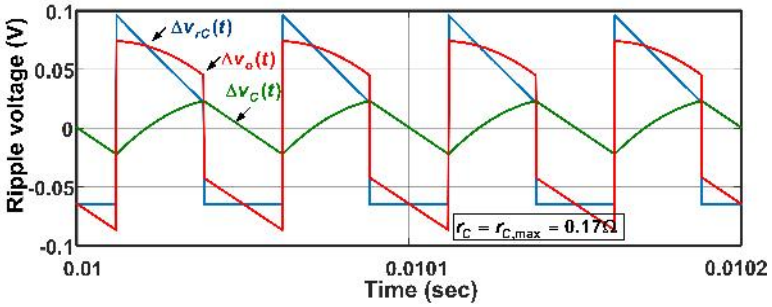
***Case 3 (*$r_c = r_{c,\max} = 0.17$*)*:** In this case, the ESR of output capacitor (r_c) is 0.17Ω which is equal to the value of maximum permissible ESR. The ripple contribution due to ESR increases, resulting to increases OVR. The simulated result of output voltage



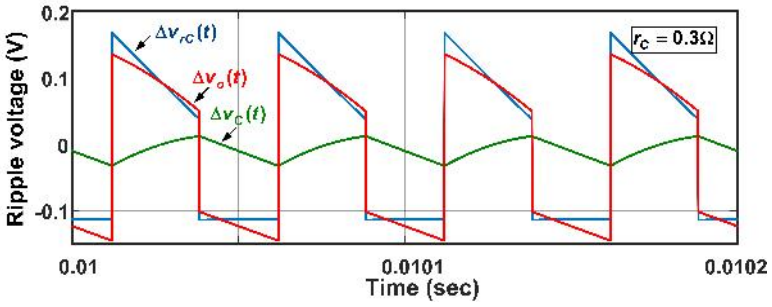
(a)



(b)

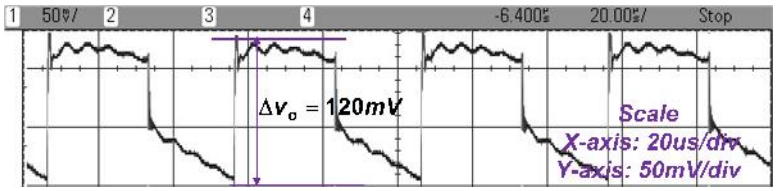


(c)

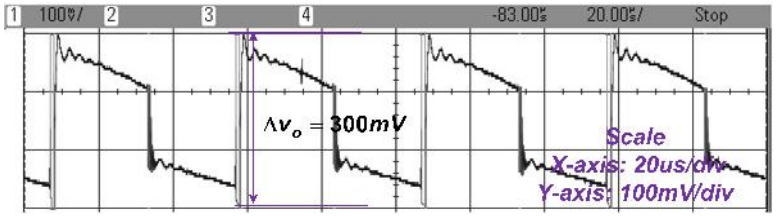


(d)

Figure 2.27: Simulation results of output voltage ripples with aESR (r_c) =0Ω bESR (r_c) =0.12Ω cESR (r_c)= 0.17Ω dESR (r_c) =0.3Ω.



(a)



(b)

Figure 2.28: Experimental result of output voltage ripples with (a)ESR (r_c) =0.12Ω (b)ESR (r_c) =0.3Ω.

ripples are shown in Figure 2.27(c). These results show that the magnitude of output voltage ripple is about 125 mV, which is within desired limit (166 mV).

Case 4 ($r_c = 0.3 > r_{c,\max}$***):*** This case evaluates the output voltage ripples if capacitor ESR (r_c) is greater than the maximum permissible ESR. Therefore, the value of r_c is kept 0.3Ω in simulation as well as in experiment. As shown in Figure 2.27(d) and Figure 2.28(b), respectively, the output voltage ripple is obtained nearly 300 mV, which is beyond the desired limit (166 mV). Therefore, this value of output capacitor ESR is not suitable to have output voltage ripples within 2% range as desired.

2.7 Performance Comparison of Non-ideal Boost Converter With Other Semi-non ideal Boost Converter Models

In most of the existing literature, researchers only considers few of the non-idealities as it makes the calculations simple. In design and control point of view, it makes difference between complete non-ideal model and other models. To analyse the comparative performance of presented non-ideal boost converter, we have considered the semi-non ideal boost converter models (*i.e., models with less parasitic elements*) used in [158–160, 163, 164].

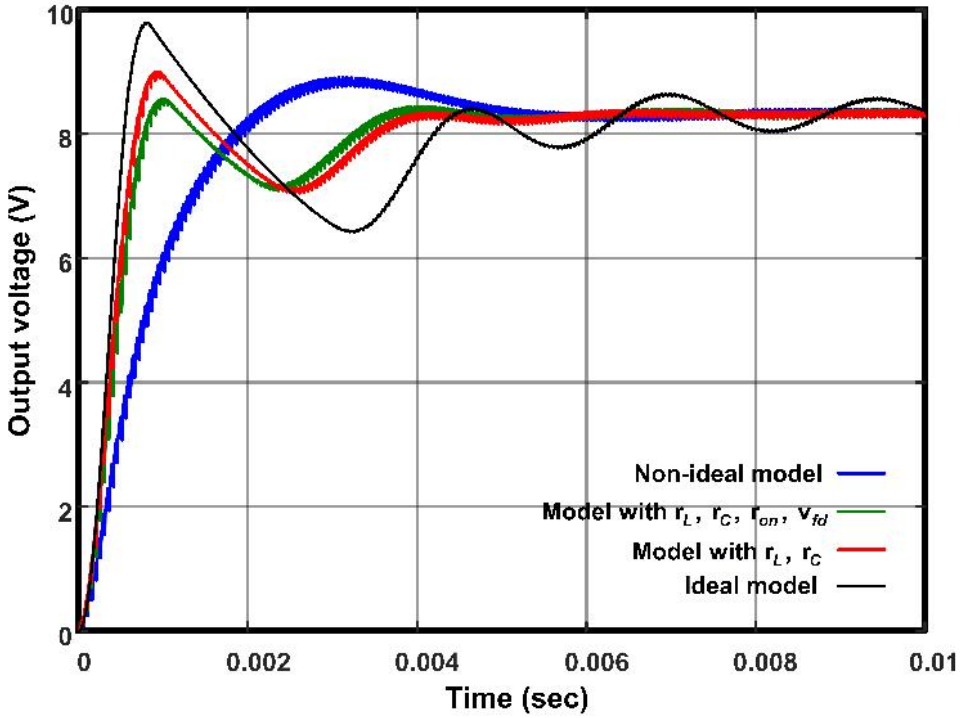
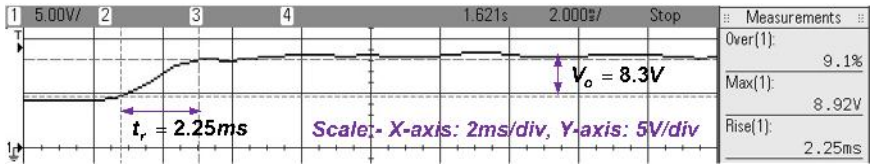


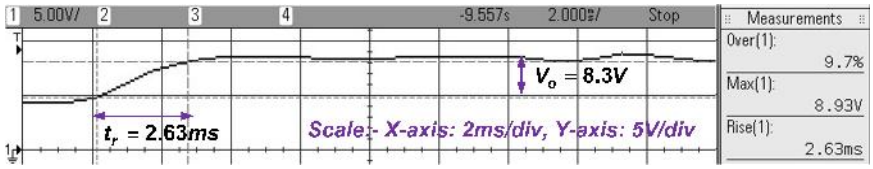
Figure 2.29: Simulation comparison of performance of different converters.

Here, basic internal model control [82] based PID controllers are designed for semi-non ideal and complete non-ideal boost converters. Since the models are non-identical, controller gains will be different. The simulation results of closed-loop performance of the all converter models are shown in Figure 2.29. The corresponding experimental results are shown in Figure 2.30(a) to Figure 2.30(d). In all simulations, we observe that the controller improves the closed-loop performance of the converter. Whereas, in practical system, all non-idealities will present. So when the controller parameters implemented practically, it will not give the same result as it gives in the simulation. Hence, there is a considerable difference between simulations and experimental results.

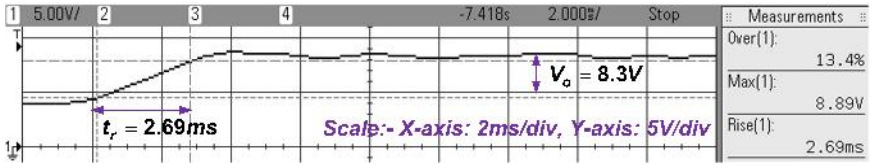
Further, Table 2.3 shows the comparison of all considered converters in terms of various performance specifications. From this comparison, it is clear that the complete non-ideal boost converter simulations are very near to the experimental values. This is duo to the controller designed by using the non-ideal model. This shows that the complete non-ideal model will resembles the practical system.



(a)



(b)



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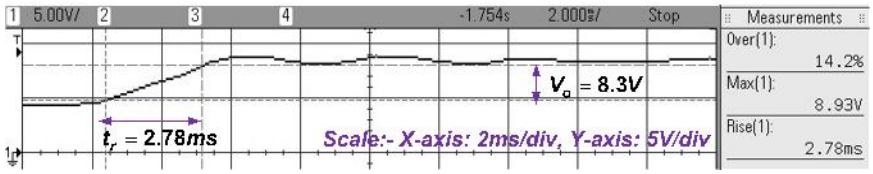


(d)

Figure 2.30: Experimental results of boost converter for PID parameters calculated from (a) complete non-ideal boost converter model (b) boost converter model with r_L, r_C, r_{on} and V_{fd} (c) boost converter model with r_L, r_C (d) ideal boost converter.

Table 2.3: Performance comparison of non-ideal boost converter performance with other semi-non ideal converters

	Non-ideal model of boost converter			Boost converter with r_L,r_C, r_{on} and V_{fd} [158]			Boost converter with r_L and r_C [159, 160]			Ideal boost converter [163, 164]		
	Sim	Exp	**Err**	Sim	Exp	Err	Sim	Exp	Err	Sim	Exp	Err
Reg_{Line} (%)	0.17	0.22	**22%**	0.21	0.34	38.2%	0.24	0.40	40%	0.08	0.48	82%
Reg_{Load}(%)	0.22	0.29	**24%**	0.24	0.44	45.4%	0.25	0.48	47%	0.09	0.5	83%
t_r (in ms)	1.9	2.25	**15.5%**	0.77	2.67	71%	0.67	2.69	75%	0.5	2.78	85%
M_p (in V)	8.9	8.92	**0.2%**	8.56	8.93	4.1%	9.0	8.89	1.2%	8.93	9.78	8.7%
V_{gmin} (in V)	2.6	2.7	**3.7%**	1.99	2.7	26%	1.78	2.7	34%	-	2.7	-
V_{omax} (in V)	16.3	16.32	**0.1%**	21.28	16.32	23%	23.4	16.32	30.1%	-	16.32	-
D_{max}	0.85	0.85	**0.0%**	0.89	0.85	4.4%	0.9	0.85	5.5%	1.0	0.85	15%

Sim-Simulation, Exp-Experimental, Err- Relative error, Reg_{Line}-Line regulation, Reg_{Load}-Load regulation, t_r-Rise time, M_p-Peak value, V_{gmin}-Minimum input voltage in closed-loop,

V_{omax}-Maximum achievable voltage, D_{max}-Maximum possible duty cycle

2.8 Mathematical Modelling

Boost converter with non-idealities to be modelled is shown in Figure 2.31. The state space average approach is used for modeling, which is explained in *Appendix A*. The most important point to be observed is that the modeling done by considering the all non-idealities or parasitics. As depicted in Figure 2.31, which is same as Figure 2.1(a), but a current source ($i_z(t)$) is connected to the output terminals of the converter, which models the loading effect of the load subsystem (besides the resistive load) being fed from this converter. As explained in previous sections, modeling of

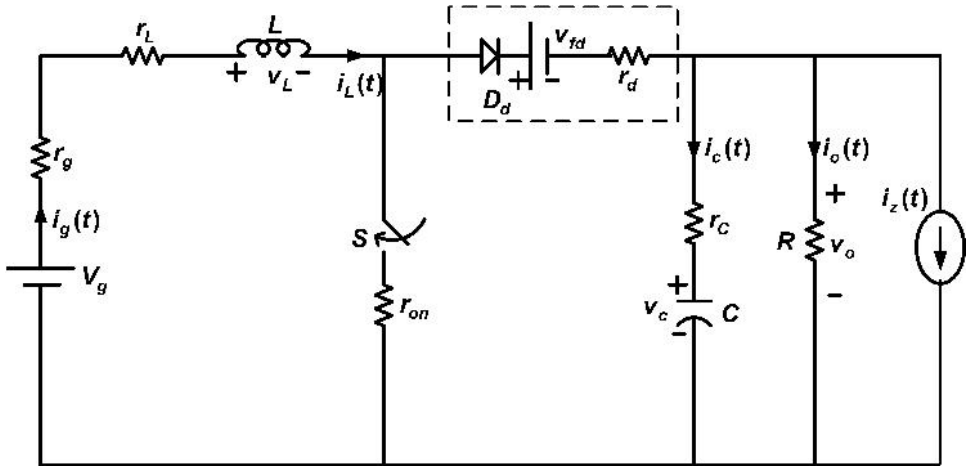


Figure 2.31: Non-ideal boost converter model.

non-ideal DC-DC boost converter is carried out in CCM. In this, as converter consists of only one active switch (S) that can be ON or OFF and thus has only two modes of operation. The equivalent circuits for these modes are already shown in Figures 2.1(b) and (c). So, we need to write state equations for both modes of operation. For this, inductor current and capacitor voltage as considered as states of the system. The mathematical modeling of the non-ideal boost converter is given below:

Step 1: Writing the state equations for two modes of operation

During ON time $(0 < t < DT)$

When switch is ON (S), the equations governing with inductor current (i_L), capacitor

voltage (v_c) and output voltage (v_o) are obtained as:

$$\begin{aligned} v_L(t) = L\frac{di_L(t)}{dt} &= -\left[r_g + r_{on} + r_L\right] i_L(t) + v_g(t) \\ \Rightarrow \dot{i}_L(t) &= -\left(\frac{r_g + r_{on} + r_L}{L}\right) i_L(t) + \left(\frac{1}{L}\right) v_g(t) \end{aligned} \tag{2.75}$$

$$i_c(t) = C\frac{dv_c(t)}{dt} = -\frac{v_o(t)}{R} - i_z(t) \tag{2.76}$$

$$v_o(t) = v_c(t) + r_c i_c(t) \tag{2.77}$$

Substituting (2.76) in (2.77), we get,

$$\begin{aligned} v_o(t) &= v_C(t) + r_C\left(-\frac{v_o(t)}{R} - i_z(t)\right) \\ \Rightarrow v_o(t) &= \left(\frac{R}{R+r_c}\right) v_c(t) - \left(\frac{Rr_c}{R+r_c}\right) i_z(t) \end{aligned} \tag{2.78}$$

Substituting (2.78) in (2.76), we get,

$$\dot{v}_c(t) = -\left(\frac{1}{C(R+r_c)}\right) v_c(t) - \left(\frac{1}{C(R+r_c)}\right) i_z(t) \tag{2.79}$$

$$i_g(t) = i_L(t) \tag{2.80}$$

Equations (2.75), (2.79), (2.78) and (2.80) can be represented in state space form as

$$\underset{\tilde{}}{\dot{x}} \qquad\qquad \underset{}{A_1} \qquad\qquad\qquad\qquad \underset{}{B_1} \qquad\qquad\qquad\qquad \underset{}{J_1}$$

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} -\frac{r_g + r_{on} + r_L}{L} & 0 \\ 0 & -\frac{1}{C(R+r_c)} \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{R}{C(R+r_c)} \end{bmatrix}\begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix}\begin{bmatrix} V_{fd} \end{bmatrix} \tag{2.81}$$

$$\underset{\tilde{}}{y} \qquad\qquad \underset{}{C_1} \qquad\qquad\qquad\qquad \underset{}{E_1} \qquad\qquad\qquad\qquad \underset{}{F_1}$$

$$\begin{bmatrix} v_o(t) \\ i_g(t) \end{bmatrix} = \begin{bmatrix} 0 & \frac{R}{R+r_c} \\ 1 & 0 \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 0 & -\frac{Rr_c}{R+r_c} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix}\begin{bmatrix} V_{fd} \end{bmatrix} \tag{2.82}$$

During OFF time

When switch is OFF (S), the equations governing with inductor current (i_L), capacitor voltage (v_c) and output voltage (v_o) are obtained as:

$$v_L(t) = L\frac{di_L(t)}{dt} = -\left[r_g + r_L + r_d\right] i_L(t) - v_o(t) + v_g(t) - V_{fd} \tag{2.83}$$

$$i_c(t) = C\frac{dv_c(t)}{dt} = i_L(t) - \frac{v_o(t)}{R} - i_z(t) \tag{2.84}$$

$$v_o(t) = v_c(t) + r_c i_c(t) \tag{2.85}$$

$$i_g(t) = i_L(t) \tag{2.86}$$

Substituting (2.84) in (2.85), we get,

$$\begin{aligned} &v_o(t) = v_c(t) + r_c\left(i_L(t) - \tfrac{v_o(t)}{R} - i_z(t)\right) \\ &\Rightarrow v_o(t) = \left(\tfrac{R}{R+r_c}\right)v_c(t) + \left(\tfrac{Rr_c}{R+r_c}\right)i_L(t) - \left(\tfrac{Rr_c}{R+r_c}\right)i_z(t) \end{aligned} \tag{2.87}$$

Substituting (2.87) in (2.84), we get,

$$\dot{v}_c(t) = \left(\frac{R}{C(R+r_c)}\right)i_L(t) - \left(\frac{1}{C(R+r_c)}\right)v_c(t) - \left(\frac{R}{C(R+r_c)}\right)i_z(t) \tag{2.88}$$

Substituting (2.87) in (2.83), we get,

$$\begin{aligned} \dot{i}_L(t) = &-\left(\tfrac{(r_g+r_d+r_L)(R+r_c)+Rr_c}{L(R+r_c)}\right)i_L(t) - \left(\tfrac{R}{L(R+r_c)}\right)v_c(t) + \left(\tfrac{1}{L}\right)v_g(t) + \\ &\left(\tfrac{Rr_c}{L(R+r_c)}\right)i_z(t) - \tfrac{V_{fd}}{L} \end{aligned} \tag{2.89}$$

Equations (2.87), (2.88), (2.89) and (2.86) can be represented in state space form as

$$\underset{\tilde{}}{\dot{x}} \qquad\qquad A_2 \qquad\qquad\qquad\qquad B_2$$

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} -\frac{(r_g+r_d+r_L)(R+r_c)+Rr_c}{L(R+r_c)} & -\frac{R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & -\frac{1}{C(R+r_c)} \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{Rr_c}{L(R+r_c)} \\ 0 & -\frac{R}{C(R+r_c)} \end{bmatrix}\begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix}$$

$$J_2$$

$$+ \begin{bmatrix} -\frac{1}{L} \\ 0 \end{bmatrix}\begin{bmatrix} V_{fd} \end{bmatrix} \tag{2.90}$$

$$\underset{\tilde{}}{y} \qquad\qquad C_2 \qquad\qquad\qquad\qquad E_2 \qquad\qquad\qquad\qquad F_2$$

$$\begin{bmatrix} v_o(t) \\ i_g(t) \end{bmatrix} = \begin{bmatrix} \frac{Rr_c}{R+r_c} & \frac{R}{R+r_c} \\ 1 & 0 \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 0 & -\frac{Rr_c}{R+r_c} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix}\begin{bmatrix} V_{fd} \end{bmatrix} \tag{2.91}$$

Step 2: Obtain the large signal state-space averaged model

The large signal averaged state-space model of non-ideal DC-DC boost converter can be obtained as

$$\tilde{\dot{x}} \qquad \bar{\dot{x}} \qquad\qquad\qquad A$$

$$\frac{d}{dt}\begin{bmatrix}\bar{i}_L(t)\\ \bar{v}_C(t)\end{bmatrix} = \begin{bmatrix}-\frac{\left(\, r_g + r_L + Dr_{on} + (1-D)r_d \,\right)^{(R+r_c)+(1-D)(Rr_c)}}{L} & -\frac{(1-D)R}{L(R+r_c)}\\ \frac{(1-D)R}{C(R+r_c)} & -\frac{1}{C(R+r_c)}\end{bmatrix}\begin{bmatrix}\bar{i}_L(t)\\ \bar{v}_C(t)\end{bmatrix}$$

$$B \qquad\qquad J$$

$$+\begin{bmatrix}\frac{1}{L} & \frac{(1-D)Rr_c}{L(R+r_c)}\\ 0 & -\frac{R}{C(R+r_c)}\end{bmatrix}\begin{bmatrix}\bar{v}_g(t)\\ \bar{i}_z(t)\end{bmatrix} + \begin{bmatrix}-\left(\frac{1-D}{L}\right)\\ 0\end{bmatrix}\begin{bmatrix}V_{fd}\end{bmatrix} \tag{2.92}$$

$$\tilde{\bar{y}} \qquad\qquad C \qquad\qquad E \qquad\qquad F$$

$$\begin{bmatrix}\bar{v}_o(t)\\ \bar{i}_g(t)\end{bmatrix} = \begin{bmatrix}\frac{(1-D)Rr_c}{R+r_c} & \frac{R}{R+r_c}\\ 1 & 0\end{bmatrix}\begin{bmatrix}\bar{i}_L(t)\\ \bar{v}_C(t)\end{bmatrix} + \begin{bmatrix}0 & -\frac{Rr_c}{R+r_c}\\ 0 & 0\end{bmatrix}\begin{bmatrix}\bar{v}_g(t)\\ \bar{i}_z(t)\end{bmatrix} + \begin{bmatrix}0\\ 0\end{bmatrix}\begin{bmatrix}V_{fd}\end{bmatrix} \tag{2.93}$$

Where,

$$\begin{aligned} A &= DA_1 + (1-D)A_2, B = DB_1 + (1-D)B_2\\ C &= DC_1 + (1-D)C_2, E = DE_1 + (1-D)E_2\\ J &= DJ_1 + (1-D)J_2, \mathrm{F} = DF_1 + (1-D)F_2 \end{aligned} \tag{2.94}$$

Step 3: Linearising around a operating point and obtain the ac small signal model

The all available time varying signals can be approximately written as sum of it's steady-state (DC or average) value and it's small variation around a operating point.

$$\begin{aligned} &i_L(t) = I_L + \hat{i}_L(t), i_g(t) = I_g + \hat{i}_g(t), i_o(t) = I_o + \hat{i}_o(t), i_z(t) = I_z + \hat{i}_z(t),\\ &d(t) = D + \hat{d}(t), v_C(t) = V_C + \hat{v}_C(t), v_g(t) = V_g + \hat{v}_g(t), v_o(t) = V_o + \hat{v}_o(t). \end{aligned} \tag{2.95}$$

To get the steady-state (DC) and small signal (ac) models of the non-ideal DC-DC boost converter, substitute (2.95) in (2.92) and (2.93), we get,

Steady-state (DC) model:

$$\begin{bmatrix}I_L\\ V_C\end{bmatrix} = -A^{-1}\left(B\begin{bmatrix}V_g\\ I_z\end{bmatrix} + J\right) \tag{2.96}$$

$$\begin{bmatrix} V_o \\ I_g \end{bmatrix} = C \begin{bmatrix} I_L \\ V_C \end{bmatrix} + E \begin{bmatrix} V_g \\ I_z \end{bmatrix} + F \tag{2.97}$$

Small-signal (ac) model:

$\tilde{\ }$ $\hat{\ }x$ A

$$\frac{d}{dt}\begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_C(t) \end{bmatrix} = \begin{bmatrix} -\frac{\Big(\ r_g + r_L + Dr_{on} + (1-D)r_d\ \Big)(R+r_c)+(1-D)(Rr_c)}{L} & -\frac{(1-D)R}{L(R+r_c)} \\ \frac{(1-D)R}{C(R+r_c)} & -\frac{1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_C(t) \end{bmatrix}$$

B B_d

$$+ \begin{bmatrix} \frac{1}{L} & \frac{(1-D)Rr_c}{L(R+r_c)} \\ 0 & -\frac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \hat{v}_g(t) \\ \hat{i}_z(t) \end{bmatrix} + \begin{bmatrix} \frac{((r_d-r_{on})(R+r_c)+Rr_c)I_L+RV_c-Rr_cI_z+V_{fd}(R+r_c)}{L(R+r_c)} \\ -\frac{RI_L}{C(R+r_c)} \end{bmatrix} \left[\hat{d}(t)\right] \tag{2.98}$$

$\tilde{\ }$ $\hat{y}$ C E E_d

$$\begin{bmatrix} \hat{v}_o(t) \\ \hat{i}_g(t) \end{bmatrix} = \begin{bmatrix} \frac{(1-D)Rr_c}{R+r_c} & \frac{R}{R+r_c} \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_C(t) \end{bmatrix} + \begin{bmatrix} 0 & -\frac{Rr_c}{R+r_c} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_g(t) \\ \hat{i}_z(t) \end{bmatrix} + \begin{bmatrix} -\frac{Rr_cI_L}{R+r_c} \\ 0 \end{bmatrix} \left[\hat{d}(t)\right] \tag{2.99}$$

Step 4: Determination of steady-state values

The steady-state values of output voltage, input current and inductor current can also be found by substituting (2.98), (2.99) in (2.96) and (2.97), respectively. we get,

$$\Rightarrow I_L = \frac{V_o}{R} + I_z \tag{2.100}$$

$$\Rightarrow I_g = \frac{V_o}{R} + I_z \tag{2.101}$$

$$\Rightarrow V_o = \frac{[V_g - D'V_{fd}]D'R(R+r_c)}{[(r_g + r_L + Dr_{on} + D'r_d)(R+r_c)] + [D'R(D'R+r_c)]} \tag{2.102}$$

In order to get the ideal steady-state models of the DC-DC boost converter, replace non-idealities or parasitics with zero in (2.100)-(2.102), we get,

$$\Rightarrow I_{Li} = \frac{V_{oi}}{R} + I_z \tag{2.103}$$

$$\Rightarrow I_{gi} = \frac{V_{oi}}{R} + I_z \tag{2.104}$$

$$\Rightarrow V_{oi} = \frac{V_g}{1-D} \tag{2.105}$$

2.8.1 Comparison of steady-state ideal and non-ideal models

The steady-state models of ideal and non-ideal boost converters are obtained in previous sections. Now, for comparison of these models, parameter values are consider from Table 2.1. These values substituted in relationships obtained for non-ideal and ideal cases given in (2.100)-(2.102) and (2.103)-(2.105), respectively. The values obtained in non-ideal case are always less than the ideal case, this is due to the power loss in non-ideal elements which is clear from Table 2.4. This has been clearly discussed in previous sections, where these steady-state relationships are derived analytically as given in (2.17).

Table 2.4: Steady-state values comparison of ideal and non-ideal cases at $D = 0.475$

Parameter	Ideal case			Non-ideal case		
	Analytical	Experimental	Error	Analytical	Experimental	Error
I_L (A)	0.828	0.71	16.6%	0.72	0.71	1.4%
V_o (V)	9.54	8.32	14.6%	8.33	8.32	0.1%
I_g (A)	0.828	0.71	16.6%	0.72	0.71	1.4%

Step 5: Determination of various transfer functions

As per the considered input variables (v_g, i_z, d), state variables (i_L, v_C) and output variables (v_o, i_g) maximum twelve transfer functions are possible for non-ideal DC-DC boost converter. Nevertheless, some important transfer functions only presented here. In order to get various transfer functions, first need to find $(sI - A)^{-1}$ for boost

converter, which is given below:

$$(sI - A)^{-1} = \frac{Adj\,(sI - A)}{|sI - A|} \tag{2.106}$$

$$\Rightarrow \frac{\begin{bmatrix} s + \frac{1}{C(R+r_c)} & -\frac{D^1 R}{L(R+r_c)} \\ \frac{D^1 R}{C(R+r_c)} & s + \frac{r_L + r_g + Dr_{on} + D^1(r_d + R\|r_c)}{L} \end{bmatrix}}{s^2 + \frac{(R+r_c)\left(L + C\left(r_L + r_g + Dr_{on} + D' r_d\right)(R+r_c) + D' R r_c\right)}{LC(R+r_c)^2} s + \frac{\left(r_g + r_L + Dr_{on} + D' r_d\right)(R+r_c) + D' R\left(D' R + r_c\right)}{LC(R+r_c)^2}} \tag{2.107}$$

Now, some of the important transfer functions of non-ideal DC-DC boost converter are derived, which are useful for controller design and analysis.

(i) Control to output voltage or Control voltage gain:

This transfer function describes the impact of variation in duty cycle ($\hat{d}(t)$) on output voltage ($\hat{v}_o$). This is derived by keeping the input voltage ($\hat{v}_g$) and output current ($\hat{i}_z$) variations to zero. This can be determined as follows:

$$G_{vd}(s)|_{\hat{v}_g, \hat{i}_z = 0} = \frac{\hat{v}_o(s)}{\hat{d}(s)} = C(sI - A)^{-1} B_d + E_d \tag{2.108}$$

By substituting (2.98) and (2.99) in (2.108), we get,

$$G_{vd}(s) = \begin{bmatrix} \frac{(1-D)Rr_c}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix} \frac{Adj(sI - A)^{-1}}{|sI - A|} \begin{bmatrix} \frac{((r_d - r_{on})(R+r_c) + Rr_c) I_L + RV_c - Rr_c I_z + V_{fd}(R+r_c)}{L(R+r_c)} \\ -\frac{RI_L}{C(R+r_c)} \end{bmatrix} + \begin{bmatrix} -\frac{Rr_c I_L}{R+r_c} \\ 0 \end{bmatrix} \tag{2.109}$$

Further simplifying (2.109) and writing in terms of pole-zero form as given in (2.110)

$$G_{vd}(s) = K_{vd} \frac{\left(1 + \frac{s}{\omega_{LHPz}}\right)\left(1 - \frac{s}{\omega_{RHPz}}\right)}{1 + \frac{s}{Q\omega_P} + \left(\frac{s}{\omega_P}\right)^2} \tag{2.110}$$

or in SOPTD

$$G_{vd}(s) = (K_{vd} * \omega_{RHPz}) \frac{\left(1 + \frac{s}{\omega_{LHPz}}\right)}{1 + \frac{s}{Q\omega_P} + \left(\frac{s}{\omega_P}\right)^2} e^{-\frac{s}{\omega_{RHPz}}} \tag{2.111}$$

where,

$$K_{vd} = \frac{R\left(R+r_c\right)\left(\begin{array}{l}\left(V_g - D^{'}V_{fd}\right)\left(-r_g - r_L - r_{on}\right)\left(R+r_c\right) + V_g\left(D^{'}R\right)^2 + \\ D^{'}\left(V_{fd} - I_z\left(R \parallel r_c\right)\right)\left(\begin{array}{l}\left(r_g + r_L + Dr_{on} + D^{'}r_d\right)\left(R+r_c\right) \\ +D^{'}Rr_c\end{array}\right) \\ -I_z\left(R \parallel r_c\right)\left(D^{'}\right)^3 R^2\end{array}\right)}{\left(\left(r_g + r_L + Dr_{on} + D^{'}r_d\right)\left(R+r_c\right) + D^{'}R\left(D^{'}R + r_c\right)\right)^2} \tag{2.112}$$

$$\omega_{RHPz} = \frac{\left(\begin{array}{l}\left(V_g - D^{'}V_{fd}\right)\left(r_g + r_L + r_{on}\right)\left(R+r_c\right) - V_g\left(D^{'}R\right)^2 - \\ D^{'}\left(V_{fd} - I_z\left(R \parallel r_c\right)\right)\left(\left(r_g + r_L + Dr_{on} + D^{'}r_d\right)\left(R+r_c\right) + D^{'}Rr_c\right) \\ +I_z\left(R \parallel r_c\right)\left(D^{'}\right)^3 R^2\end{array}\right)}{L\left(R+r_c\right)\left(-V_g + D^{'}V_{fd}\right)} \tag{2.113}$$

$$\omega_{LHPz} = \frac{1}{Cr_c} \tag{2.114}$$

$$\omega_p = \sqrt{\frac{\left(\left(r_g + r_L + Dr_{on} + D^{'}r_d\right)\left(R+r_c\right) + D^{'}R\left(D^{'}R + r_c\right)\right)}{LC\left(R+r_c\right)^2}} \tag{2.115}$$

$$Q = \frac{\sqrt{LC\left(\left(r_g + r_L + Dr_{on} + D^{'}r_d\right)\left(R+r_c\right) + D^{'}R\left(D^{'}R + r_c\right)\right)}}{L + C\left(\left(r_g + r_L + Dr_{on} + D^{'}r_d\right)\left(R+r_c\right) + D^{'}Rr_c\right)} \tag{2.116}$$

This transfer function mainly used in controller design for regulator problems. Now, by replacing non-idealities or parasitics with zero in (2.110), we get the ideal model as,

$$G_{vdi}(s) = \frac{\widehat{v}_o}{\widehat{d}}(s) = \frac{V_g\left(1 - \frac{L}{R(D^{'})^2}s\right)}{\left(D^{'}\right)^2\left(\frac{LC}{\left(D^{'}\right)^2}s^2 + \frac{L}{R(D^{'})^2}s + 1\right)} \tag{2.117}$$

(ii) Input to output voltage or Audio susceptibility:

This transfer function describes the impact of variation in input or line voltage ($\hat{v}_g$) on output voltage ($\hat{v}_o$). This is derived by keeping the duty cycle ($\hat{d}$) and output current ($\hat{i}_z$) variations to zero. This can be determined as follows:

$$G_{vg}(s)|_{\hat{i}_z, \hat{d}=0} = \frac{\hat{v}_o(s)}{\hat{v}_g(s)} = C(sI - A)^{-1}B_{1^{st}column} + E_{1^{st}column} \tag{2.118}$$

By substituting (2.98) and (2.99) in (2.118), we get,

$$G_{vg}(s) = \begin{bmatrix} \frac{(1-D)Rr_c}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix} \frac{Adj(sI-A)^{-1}}{|sI-A|} \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{2.119}$$

Further simplifying (2.119) and writing in terms of pole-zero form as given in (2.120),

$$G_{vg}(s) = K_{vg} \frac{\left(1+\frac{s}{\omega_{LHPz}}\right)}{1+\frac{s}{Q\omega_P}+\left(\frac{s}{\omega_P}\right)^2} \tag{2.120}$$

where,

$$K_{vg} = \frac{D'R\left(R+r_c\right)}{\left(r_g+r_L+Dr_{on}+D'r_d\right)\left(R+r_c\right)+D'R\left(D'R+r_c\right)} \tag{2.121}$$

$$\omega_{LHPz} = \frac{1}{Cr_c} \tag{2.122}$$

$$\omega_p = \sqrt{\frac{\left(\left(r_g+r_L+Dr_{on}+D'r_d\right)\left(R+r_c\right)+D'R\left(D'R+r_c\right)\right)}{LC\left(R+r_c\right)^2}} \tag{2.123}$$

$$Q = \frac{\sqrt{LC\left(\left(r_g+r_L+Dr_{on}+D'r_d\right)\left(R+r_c\right)+D'R\left(D'R+r_c\right)\right)}}{L+C\left(\left(r_g+r_L+Dr_{on}+D'r_d\right)\left(R+r_c\right)+D'Rr_c\right)} \tag{2.124}$$

This transfer function is very important in designing of regulator. The effect of input harmonics or changes on output can be found. Now, by replacing non-idealities or parasitics with zero in (2.120), we get the ideal model as,

$$G_{vgi}(s) = \frac{\widehat{v_o}}{\widehat{v_g}}(s) = \frac{1}{D'\left(\frac{LC}{\left(D'\right)^2}s^2+\frac{L}{R\left(D'\right)^2}s+1\right)} \tag{2.125}$$

(iii) Output Impedance:

This transfer function describes the impact of variation in output or load current ($\hat{i}_z$) on output voltage ($\hat{v}_o$). This is derived by keeping the duty cycle ($\hat{d}$) and input voltage ($\hat{v}_g$) variations to zero. This can be determined as follows:

$$Z_{out}(s)|_{\hat{v}_g,\hat{d}=0} = \frac{\hat{v}_o(s)}{\hat{i}_z(s)} = C(sI-A)^{-1}B_{2^{nd}column} + E_{2^{nd}column} \tag{2.126}$$

By substituting (2.98), (2.99) in (2.126), we get,

$$Z_{out}(s) = \begin{bmatrix} \frac{(1-D)Rr_c}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix} \frac{Adj(sI-A)^{-1}}{|sI-A|} \begin{bmatrix} \frac{(1-D)Rr_c}{L(R+r_c)} \\ -\frac{R}{C(R+r_c)} \end{bmatrix} + \begin{bmatrix} -\frac{Rr_c}{R+r_c} \\ 0 \end{bmatrix} \tag{2.127}$$

Further simplifying (2.127) and writing in terms of pole-zero form as given in (2.128)

$$Z_{out}(s) = K_{zo}\frac{\left(1+\frac{s}{\omega_{LHPz1}}\right)\left(1+\frac{s}{\omega_{LHPz2}}\right)}{1+\frac{s}{Q\omega_P}+\left(\frac{s}{\omega_P}\right)^2} \tag{2.128}$$

where,

$$K_{zo} = -R\frac{\left(r_g + r_L + Dr_{on} + D^{'}r_d\right)(R + r_c) + DD^{'}Rr_c}{\left(r_g + r_L + Dr_{on} + D^{'}r_d\right)(R + r_c) + D^{'}R\left(D^{'}R + r_c\right)} \tag{2.129}$$

$$\omega_{LHPz1} = \frac{\left(r_g + r_L + Dr_{on} + D^{'}r_d\right)(R + r_c) + DD^{'}Rr_c}{L\left(R + r_c\right)} \tag{2.130}$$

$$\omega_{LHPz2} = \frac{1}{Cr_c} \tag{2.131}$$

$$\omega_p = \sqrt{\frac{\left(\left(r_g + r_L + Dr_{on} + D^{'}r_d\right)(R + r_c) + D^{'}R\left(D^{'}R + r_c\right)\right)}{LC(R + r_c)^2}} \tag{2.132}$$

$$Q = \frac{\sqrt{LC\left(\left(r_g + r_L + Dr_{on} + D^{'}r_d\right)(R + r_c) + D^{'}R\left(D^{'}R + r_c\right)\right)}}{L + C\left(\left(r_g + r_L + Dr_{on} + D^{'}r_d\right)(R + r_c) + D^{'}Rr_c\right)} \tag{2.133}$$

This transfer function also very important quantity in voltage regulator design. Now, by replacing non-idealities or parasitics with zero in (2.128), we get the ideal model as,

$$Z_{outi}(s) = \frac{\hat{v}_o(s)}{\hat{i}_z(s)} = \frac{LC}{(1-D)^2}\frac{-\frac{s}{C}}{\frac{LC}{(1-D)^2}s^2 + \frac{L}{R(1-D)^2}s + 1} \tag{2.134}$$

(iv) Input Impedance:

This transfer function describes the impact of variation in input or line voltage ($\hat{v}_g$) on input current ($\hat{i}_g$). This is derived by keeping the duty cycle ($\hat{d}$) and output current ($\hat{i}_o$) variations to zero. This can be determined as follows:

$$Z_{in}^{-1}(s)\big|_{\hat{i}_z,\hat{d}=0} = \frac{\hat{i}_g(s)}{\hat{v}_g(s)} = C_{2^{nd}row}(sI - A)^{-1}B_{1^{st}column} + E_{1^{st}column} \tag{2.135}$$

By substituting (2.98) and (2.99) in (2.135), we get,

$$Z_{in}^{-1}(s) = \begin{bmatrix}1 & 0\end{bmatrix}\frac{Adj(sI - A)^{-1}}{|sI - A|}\begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix} + \begin{bmatrix}0\\ 0\end{bmatrix} \tag{2.136}$$

Further simplifying (2.136) and writing in terms of pole-zero form as given in (2.137)

$$Z_{in}^{-1} = K_{Zi}\frac{\left(1+\frac{s}{\omega_{LHPz}}\right)}{1+\frac{s}{Q\omega_P}+\left(\frac{s}{\omega_P}\right)^2} \tag{2.137}$$

where,

$$K_{Zi} = \frac{(R+r_c)}{(r_g+r_L+Dr_{on}+D'r_d)(R+r_c)+D'R(D'R+r_c)} \tag{2.138}$$

$$\omega_{LHPz} = \frac{1}{C(R+r_c)} \tag{2.139}$$

$$\omega_p = \sqrt{\frac{((r_g+r_L+Dr_{on}+D'r_d)(R+r_c)+D'R(D'R+r_c))}{LC(R+r_c)^2}} \tag{2.140}$$

$$Q = \frac{\sqrt{LC((r_g+r_L+Dr_{on}+D'r_d)(R+r_c)+D'R(D'R+r_c))}}{L+C((r_g+r_L+Dr_{on}+D'r_d)(R+r_c)+D'Rr_c)} \tag{2.141}$$

This transfer function is useful for cascaded converters and it plays important role when EMI filter is added [4]. Now, by replacing non-idealities or parasitics with zero in (2.128), we get the ideal model as,

$$Z_{ini}^{-1}(s) = \frac{\widehat{i}_g(s)}{\widehat{v}_g(s)} = \frac{CRs+1}{R(D')^2\left(\frac{LC}{(D')^2}s^2+\frac{LC}{R(D')^2}s+1\right)} \tag{2.142}$$

2.8.2 Comparison of small-signal ideal and non-ideal models

Here, we compare the ideal and non-ideal small signals models of the boost converter. In order to compare, the values are consider from Table 2.1. These values substituted in relationships obtained for non-ideal and ideal cases given in (2.110)-(2.142).

The comparison is shown in Table 2.5. From this table, it is observed that the quality factor (Q) is less for non-ideal model (nearly 10 times lesser the ideal value), which tells that there will not be much peak in output. Most of the transfer functions derived from non-idealities are having an extra zeros compared to their ideal models. The steady-state gain of non-ideal models is completely different than ideal models. Therefore, it is clear that non-idealities or parasitics make a lot difference in non-ideal and ideal small signal models.

Table 2.5: Transfer function comparison of ideal and non-ideal cases

Parameter	$G_{vd}(s)$		$G_{vg}(s)$		$Z_o(s)$		$Z_{in}^{-1}(s)$	
	Ideal	Non-ideal	Ideal	Non-ideal	Ideal	Non-ideal	Ideal	Non-ideal
K (dB)	18.138	14.25	5.2	4.68	-22.8	4.68	-15.8	-16.3
ω_{LHPz}	-	37880	-	37880	0	2037,37.8k	206.6	205.5
ω_{RHPz}	24250	23620	-	-	-	-	-	-
ω_P	2238.6	2324.4	2238.6	2324.4	2238.6	2324.4	2238.6	2324.4
Q	10.83	0.979	10.83	0.979	10.83	0.979	10.83	0.979

The non-ideal model transfer functions derived in previous sections are further analysed in control point of view and effect of non-idealities or parasitics also analysed.

2.9 Control Oriented Analysis

This section presents the importance of derived non-ideal transfer functions and crucial observations made through time domain and frequency response analysis. If we observe the considered transfer functions, they are mainly useful for voltage mode control, which is the objective of this thesis. Further, this section reveals the importance of small-signal transfer functions obtained by using state space average approach over the respective ideal models or transfer functions.

2.9.1 Analysis of control to output voltage or control voltage gain

2.9.1.1 Parametric effect on poles and zeros

The small-signal model or control to output transfer function presented in (2.110), shows that it is a common two pole low pass filter with two zeros. Where as, (2.117) is an ideal one, which is also the same but with one zero. Now, the effect of poles, zeros with respect to boost converter parameters are analyzed.

The trajectory of poles and zeros of ideal and non-ideal transfer functions at different values of the duty cycle D is shown in Figure 2.32. In case of non-ideal model, the LHP zero $z_1 = \frac{-1}{\omega_{LHPz}}$ do not alter with the duty cycle as it is free from duty cycle and obtained by the filter capacitor C and its equivalent series resistance r_C, where as, in ideal model there is no LHP zero. The poles locations are severely affected by the duty cycle in both ideal and non-ideal cases. Especially, in non-ideal case, poles are far from imaginary axis compared to the ideal case. The RHP zero $z_2 = \frac{1}{\omega_{RHPz}}$ moves towards origin with increase in the duty cycle in both the cases. At low duty ratios, the zero is located in the right-half of the s-plane. With increase in the duty cycle, the RHP-zero moves towards the origin. In non-ideal case, at one point (Shown as small circle M), the RHP zero is crossing the origin and moving to LHP, where as in ideal case there is no such possibility. This corresponds to a maximum possible value of duty cycle *i.e.,* D_{max}.

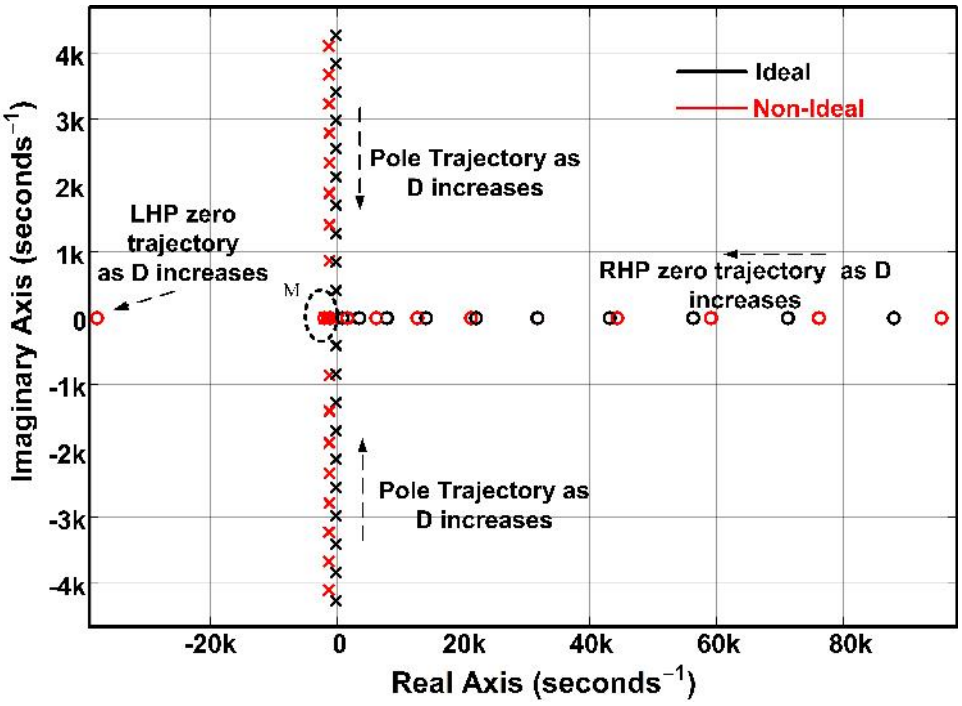


Figure 2.32: Pole zero trajectories with duty cycle variation.

Practical view of RHP zero: From control point of view, delay is introduced because of RHP zero. Practically, this can be seen as it is indirect energy transfer converter, for charging and discharging there is a time constant (approximately $\frac{L}{R}$). Hence, there will be a delay in output voltage. Further, as RHP zero moves towards origin system becomes unstable (RHP zero moves towards origin as duty cycle increases). Practically, this can be observed as duty cycle increases, converter voltage increases up to one point and collapses afterwards.

The trajectory of poles and zeros of ideal and non-ideal transfer functions at different values of the load resistance R is shown in Figure 2.33. In case of non-ideal model, the LHP zero $z_1 = \frac{-1}{\omega_{LHPz}}$ do not alter with the load resistance as it is free from R term and obtained by the filter capacitor C and its equivalent series resistance r_C, where as, in ideal model there is no LHP zero. The poles locations are not affected by the resistance variation in ideal case, where as in non-ideal case its less effected. However, the RHP zero $z_2 = \frac{1}{\omega_{RHPz}}$ moves towards $\inf$ with increase in the load resistance, which means converter is more stable at higher load resistances or low output powers. From this, it is observed that the controller design of plant should be done

for the worst-case condition, which is at minimum load condition.

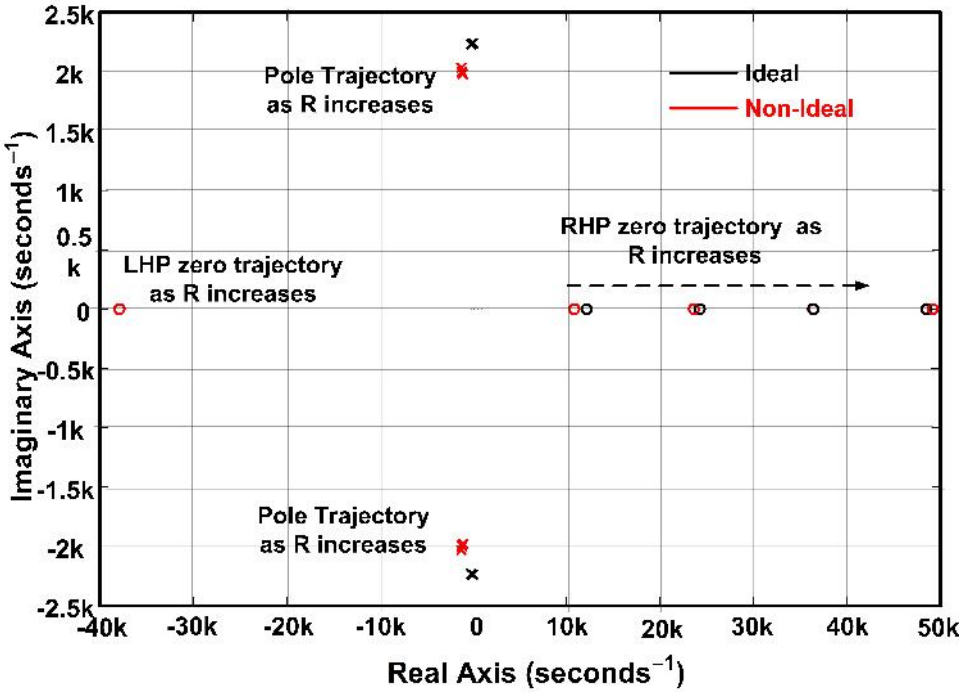


Figure 2.33: Pole zero trajectories with load resistance variation.

The trajectory of poles and zeros of ideal and non-ideal transfer functions at different values of the inductance L is shown in Figure 2.34. In case of non-ideal model, the LHP zero $z_1 = \frac{-1}{\omega_{LHPz}}$ do not alter with the inductance as it is free from L term and obtained by the filter capacitor C and its equivalent series resistance r_C, where as, in ideal model there is no LHP zero. The poles locations are also affected by the inductance variation in both ideal and non-ideal cases. However, the RHP zero $z_2 = \frac{1}{\omega_{RHPz}}$ moves towards origin with increase in the inductance.

The trajectory of poles and zeros of ideal and non-ideal transfer functions at different values of the capacitance C is shown in Figure 2.35. The LHP zero $z_1 = \frac{-1}{\omega_{LHPz}}$ moves towards origin with the increase in capacitance, where as, in ideal model there is no LHP zero. The poles locations are also affected by the inductance variation in both ideal and non-ideal cases. However, the RHP zero $z_2 = \frac{1}{\omega_{RHPz}}$ do not alter, as it is free from C term.

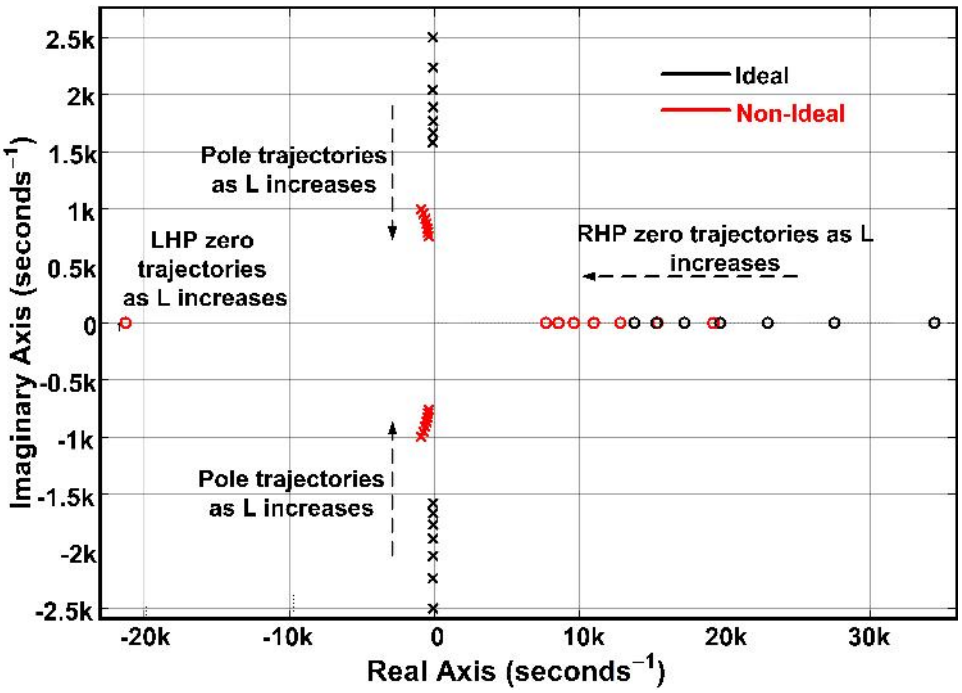


Figure 2.34: Pole zero trajectories with inductance variation.

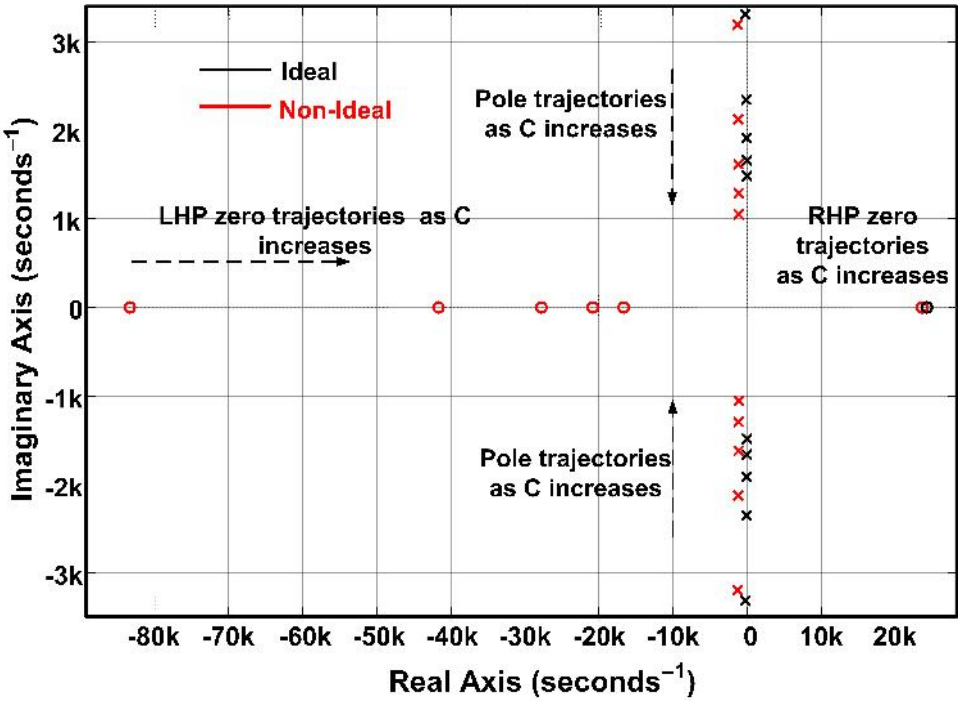


Figure 2.35: Pole zero trajectories with capacitance variation.

2.9.1.2 Time domain and frequency response analysis

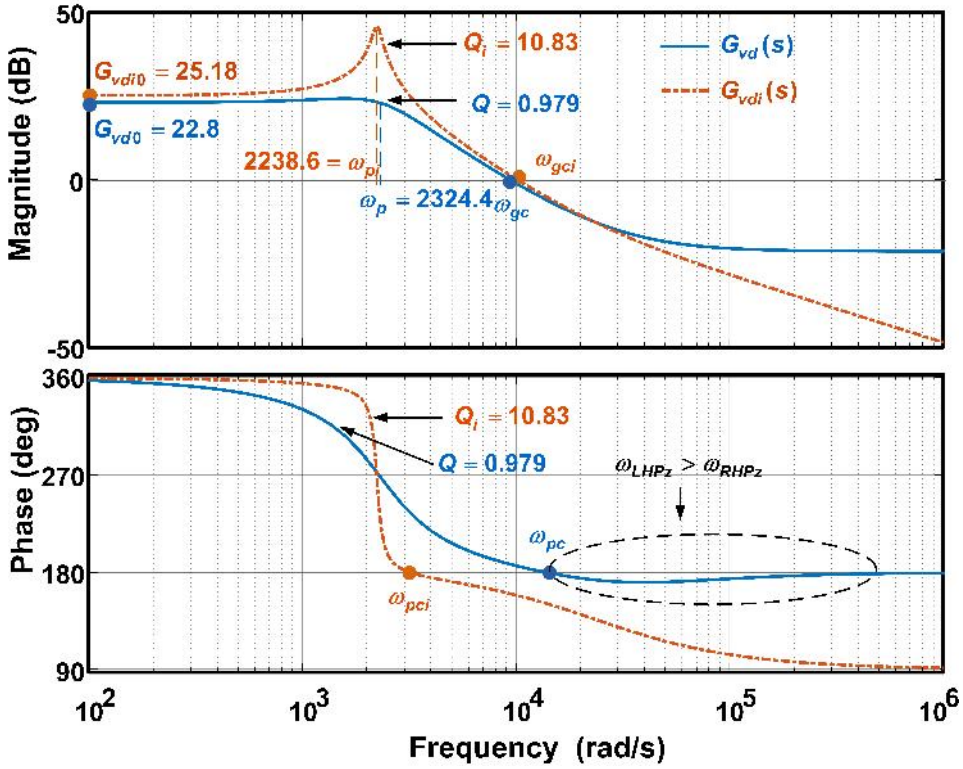


Figure 2.36: Frequency responses of ideal and non-ideal models.

By replacing the parameter values in (2.110) and (2.117), we get the transfer functions of non-ideal and ideal models of DC-DC boost converter as

$$G_{vd}(s) = \frac{14.25\left(\frac{s}{37880}+1\right)\left(-\frac{s}{23620}+1\right)}{\left(\frac{s}{2324.435}\right)^2 + \frac{s}{2275.9}+1} \tag{2.143}$$

or

$$G_{vdi}(s) = \frac{18.138\left(-\frac{s}{24250}+1\right)}{\left(\frac{s}{2238.6}\right)^2 + \frac{s}{24254.598}+1}. \tag{2.144}$$

As we have seen in previous discussion, these transfer functions have RHP zero, which makes system non-minimum phase. Figure 2.36 and 2.37 show the frequency and step responses of control to output transfer functions of ideal and non-ideal models respectively. The dc or low frequency gain of ideal model is $G_{vdio} = 25.18dB = 18.15V/\Delta d$, where as for non-ideal model is $G_{vdo} = 22.8dB = 13.8V/\Delta d$. From results section, Figure 2.16 and 2.17, shows that for a change in duty cycle ($\Delta d = 0.075$),

corresponding output voltage (V_o) changes from $7.32V$ to $8.33V$, *i.e.,* $\Delta v_o = 1.01V$. The gain calculated as $\frac{\Delta v_o}{\Delta d} = 13.47 \simeq G_{vdo}$, which shows the accuracy of non-ideal model. Further from Bode plots, it is clear that bandwidth is limited as it is a case of non-minimum phase system. More discussion on RHP zero can be seen in Chapter 5. It can be clearly observed that crossover frequency obtained using ideal model is very less compared to that of non-ideal model. From step responses also it is observed that non-idealities provides damping and there will not be much oscillations as in the case of ideal.

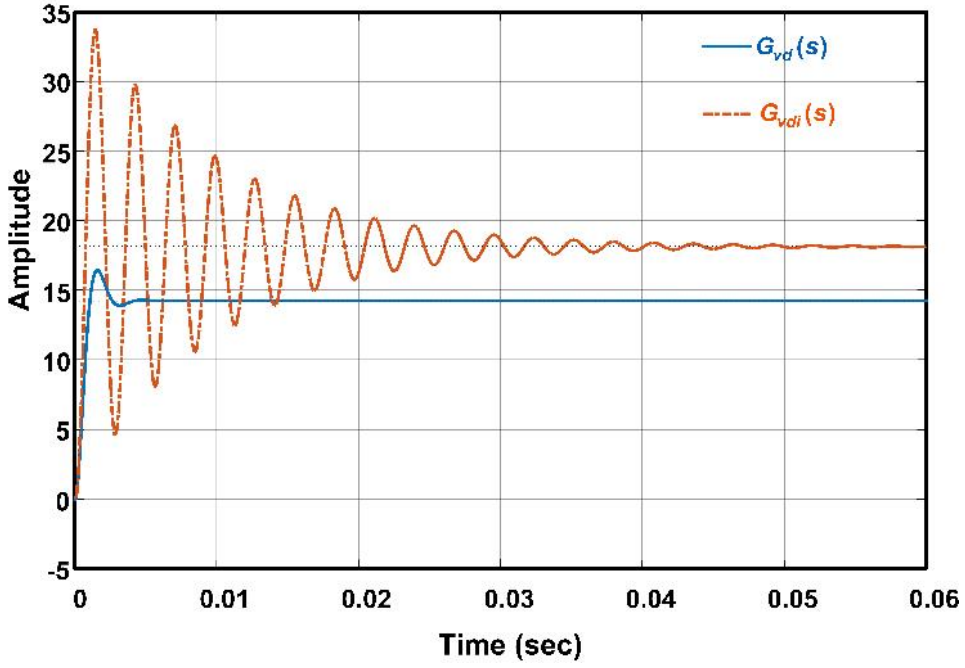


Figure 2.37: Step responses of ideal and non-ideal models.

2.9.1.3 Important observations for controller design

From the previous analysis of the control to output transfer function, the following observations can be drawn for the closed-loop control design:

- For designing robust controller by considering the parametric variations, the linear transfer function model presented in (2.110) is essential, since the model shows the dependency of pole zero frequencies on parasitics.

- From the transfer function, it is observed that the following condition must be satisfied to ensure the closed-loop stability of converter.

$$(f_{LHPz} - f_{RHPz}) < \frac{f_p}{Q} \tag{2.145}$$

  This term mostly effected by inductor and capacitor values.

- The frequency location of RHP zero (ω_{RHPz}) can be calculated exactly and how this depends on parasitics can be analysed with the expression shown (2.110). Since, the RHP zero limits the bandwidth of boost converter, this analysis is important.

- In case of non-ideal analysis, an additional LHP zero is added, which will help for the bandwidth improvement. From the expression of LHP zero frequency ω_{LHPz}, we observe that it depends on capacitor value and its ESR.

- The selection of cross over frequency should be well below the frequency of RHP zero and frequency of LHP zero should be greater than the RHP zero.

- Effect of parasitic elements on closed-loop stability of the converter system is observed from Table 2.6. All parasitics are providing stability in system and improving the closed-loop performance.

2.9.2 Analysis of input to output voltage or audio susceptibility

By replacing the parameter values in (2.120) and (2.125), we get the transfer functions of non-ideal and ideal models of DC-DC boost converter as

$$G_{vg}(s) = \frac{1.75\left(\frac{s}{37880} + 1\right)}{\left(\frac{s}{2234.435}\right)^2 + \frac{s}{2275.9} + 1} \tag{2.146}$$

$$G_{vgi}(s) = \frac{1.98}{\left(\frac{s}{2238.526}\right)^2 + \frac{s}{25254.598} + 1}. \tag{2.147}$$

Figures 2.38 and 2.40, show the frequency and step responses of input voltage to output voltage transfer functions of ideal and non-ideal models respectively. The dc

Table 2.6: Effect of parasitics on stability

Element (As it increases)	L	C	R	r_g	r_l	r_c	r_{on}	r_d	V_{fd}
K_{vd}	×	×	⇑	⇓	⇓	↓	↓	*	×
ω_{LHPz}	×	⇓	×	×	×	⇓	×	×	×
ω_{RHPz}	⇓	×	⇑	⇓	⇓	↓	⇓	×	↑
ω_p	⇓	⇓	↓	⇑	⇑	*	*	*	×
Q	⇑	⇓	↑	⇓	⇓	⇓	↓	↓	×
Over all closed loop stability	⇓	⇑	⇑	⇑	⇑	⇑	*	*	*

⇑Increases, ↑Slightly increases, ⇓Decreases, ↓Slightly decreases, *Negligible effect, ×No effect

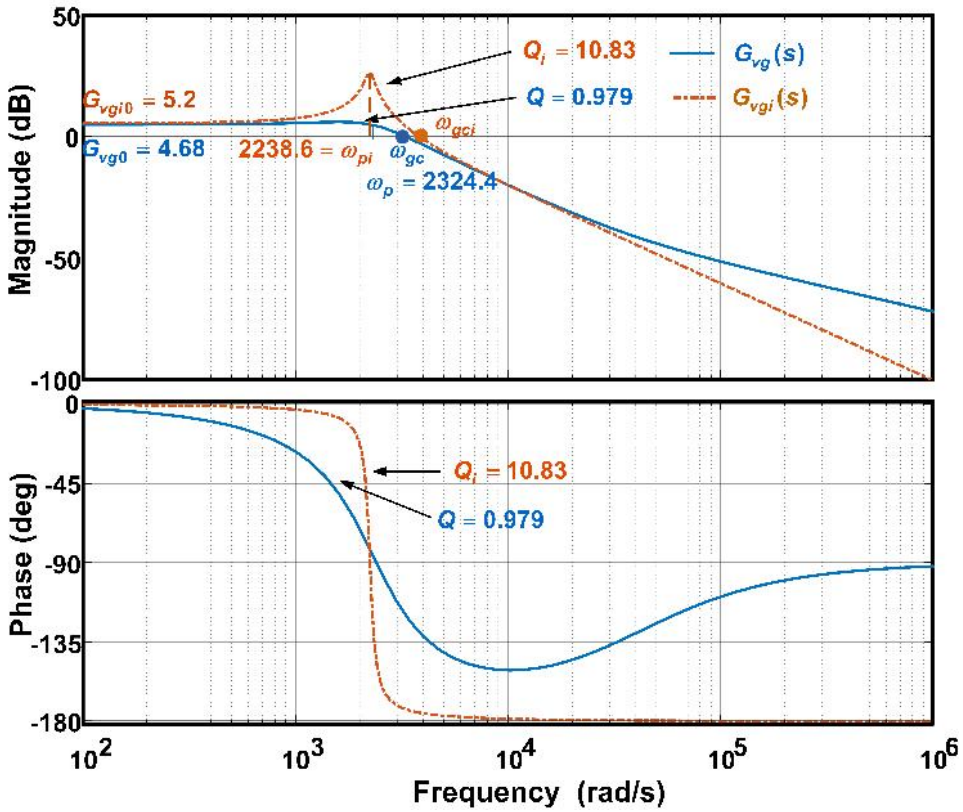


Figure 2.38: Frequency responses of ideal and non-ideal models.

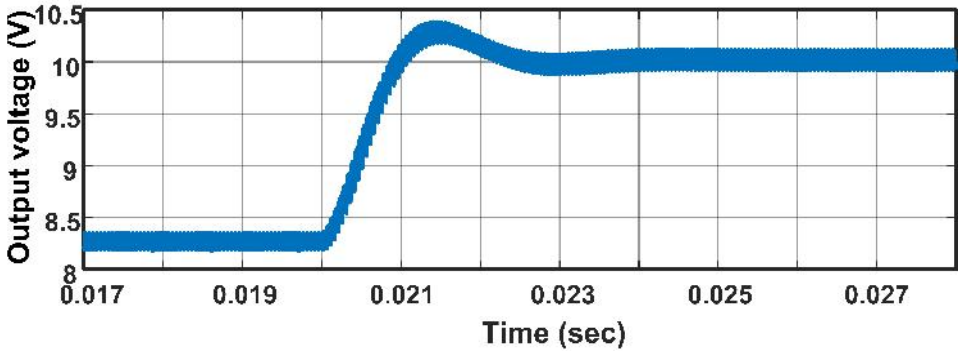


Figure 2.39: Output voltage change for input voltage change of 1V.

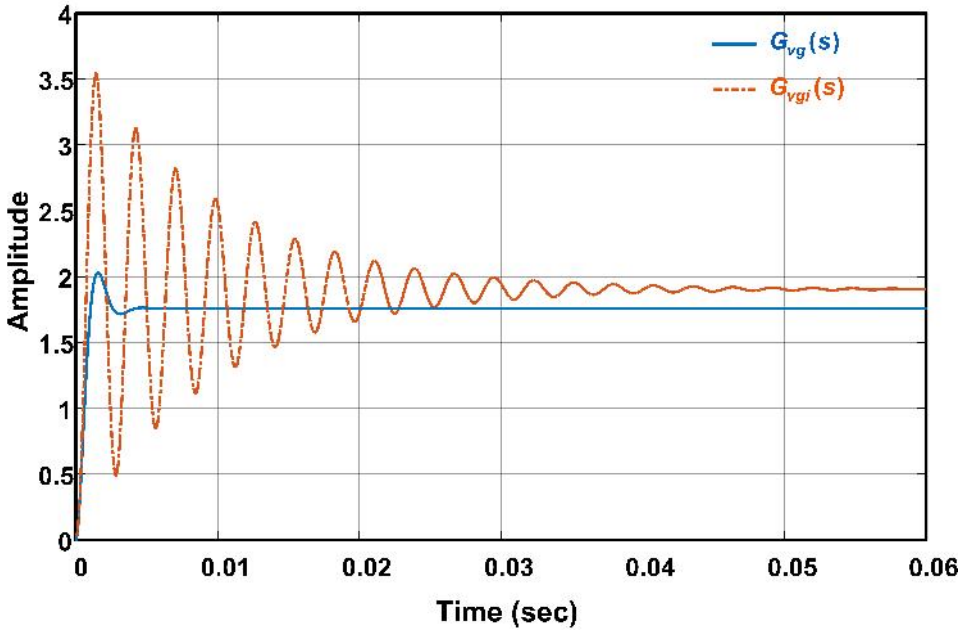


Figure 2.40: Step responses of ideal and non-ideal models.

or low frequency gain of ideal model is $G_{vgio} = 5.2dB = 2V/V$, where as for non-ideal model is $G_{vgo} = 4.68dB = 1.7V/V$. From Figure 2.39, it is observed that for a change in input voltage ($\Delta v_g = 1V$), corresponding output voltage (V_o) changes from $8.32V$ to $10V$, *i.e.,* $\Delta v_o = 1.68V$. The gain calculated as $\frac{\Delta v_o}{\Delta v_g} = 1.7 \simeq G_{vgo}$, which shows the accuracy of non-ideal model. Further Bode plots, it is observed that stability (PM and GM) of non-ideal model is better compared to ideal model. Moreover, step response also confirms that, non-ideal model is less oscillatory compared to ideal model. From this, it is concluded that parasitics or non-idealities are improving

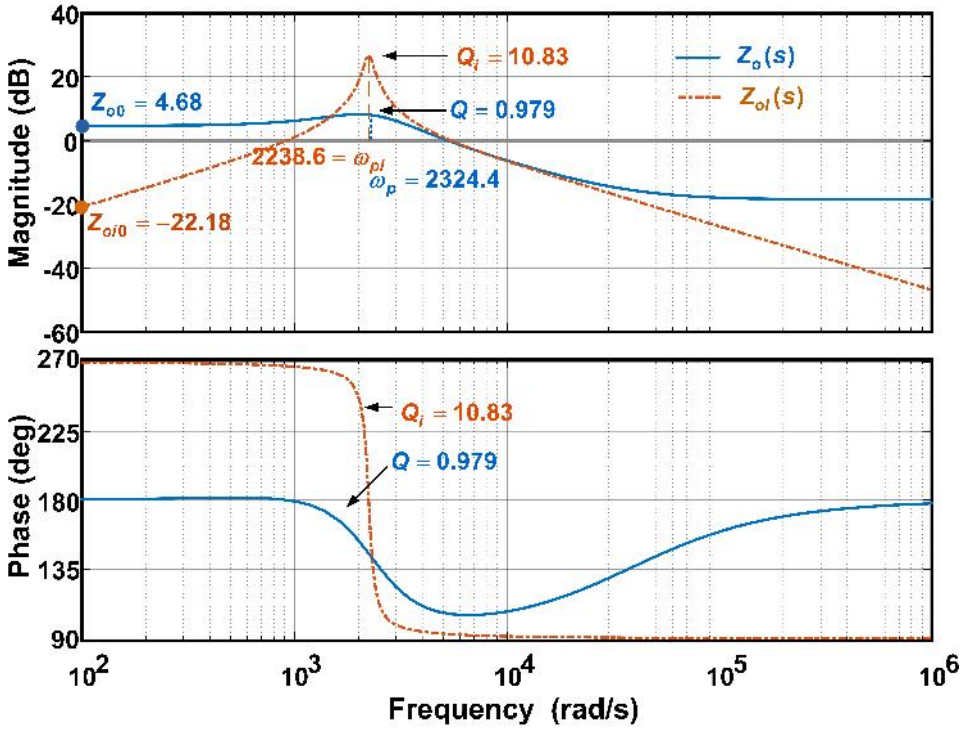


Figure 2.41: Frequency responses comparison of ideal and non-ideal models.

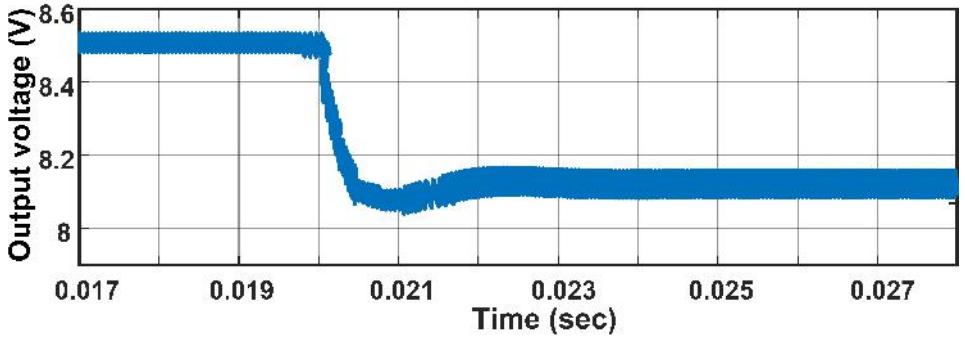


Figure 2.42: Output voltage change for load current change of 0.2A.

the stability of uncompensated boost converter in closed-loop under input voltage disturbances.

2.9.3 Analysis of output impedance

By replacing the parameter values in (2.128) and (2.134), we get the transfer functions of non-ideal and ideal models of DC-DC boost converter as

$$Z_o(s) = -\frac{1.7\left(\frac{s}{2037}+1\right)\left(\frac{s}{37880}+1\right)}{\left(\frac{s}{2234.435}\right)^2+\frac{s}{2275.9}+1} \tag{2.148}$$

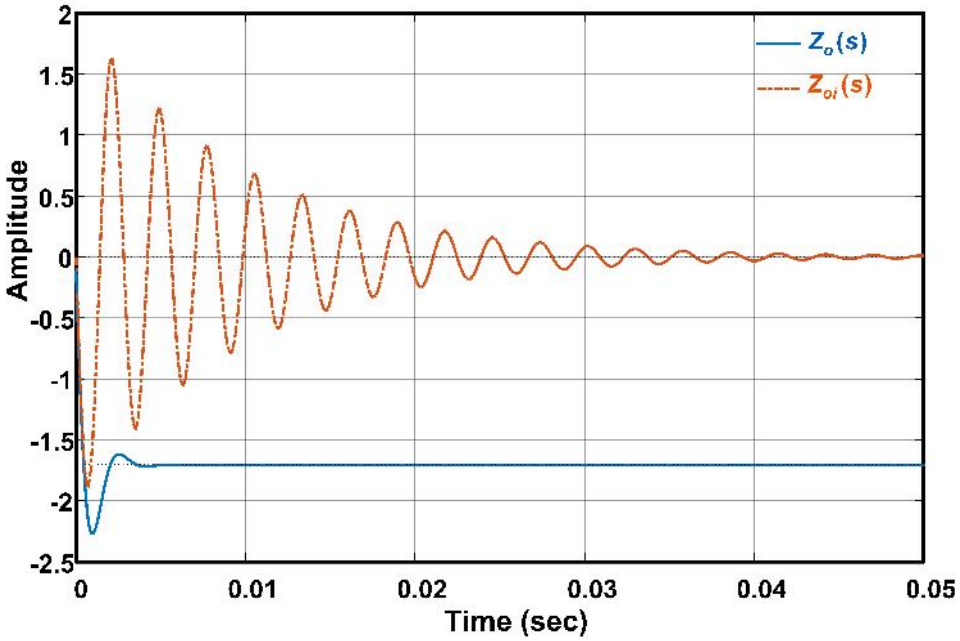


Figure 2.43: Step responses comparison of ideal and non-ideal models.

$$Z_{oi}(s) = \frac{-\frac{s}{1102.41}}{\left(\frac{s}{2238.526}\right)^2 + \frac{s}{25254.598} + 1}. \tag{2.149}$$

Figures 2.41 and 2.43, show the frequency and step responses of load current to output voltage transfer functions or output impedance of ideal and non-ideal models respectively. The dc or low frequency gain of ideal model is $Z_{oi0} = -22.18dB = 0.07\Omega/\Delta i_z$, where as for non-ideal model is $Z_{o0} = 4.68dB = 1.7\Omega/\Delta i_z$. Figure 2.42, shows that for a change in load current ($\Delta i_z = 0.2A$), corresponding output voltage (V_o) changes from $8.15V$ to $8.5V$, *i.e.,* $\Delta v_o = 0.35V$. The gain calculated as $\frac{\Delta v_o}{\Delta i_z} = 1.75\Omega \simeq Z_{o0}$, which shows the accuracy of non-ideal model. At dc and low frequencies, capacitive reactance is more and output impedance is dominated by inductive reactance. As frequency increases, the capacitive reactance dominates and makes impedance zero.

2.9.4 Analysis of input impedance

By replacing the parameter values in (2.137) and (2.142), we get the transfer functions of non-ideal and ideal models of DC-DC boost converter as

$$Z_{in}^{-1}(s) = \frac{0.152\left(\frac{s}{205.5} + 1\right)}{\left(\frac{s}{2234.435}\right)^2 + \frac{s}{2275.9} + 1} \tag{2.150}$$

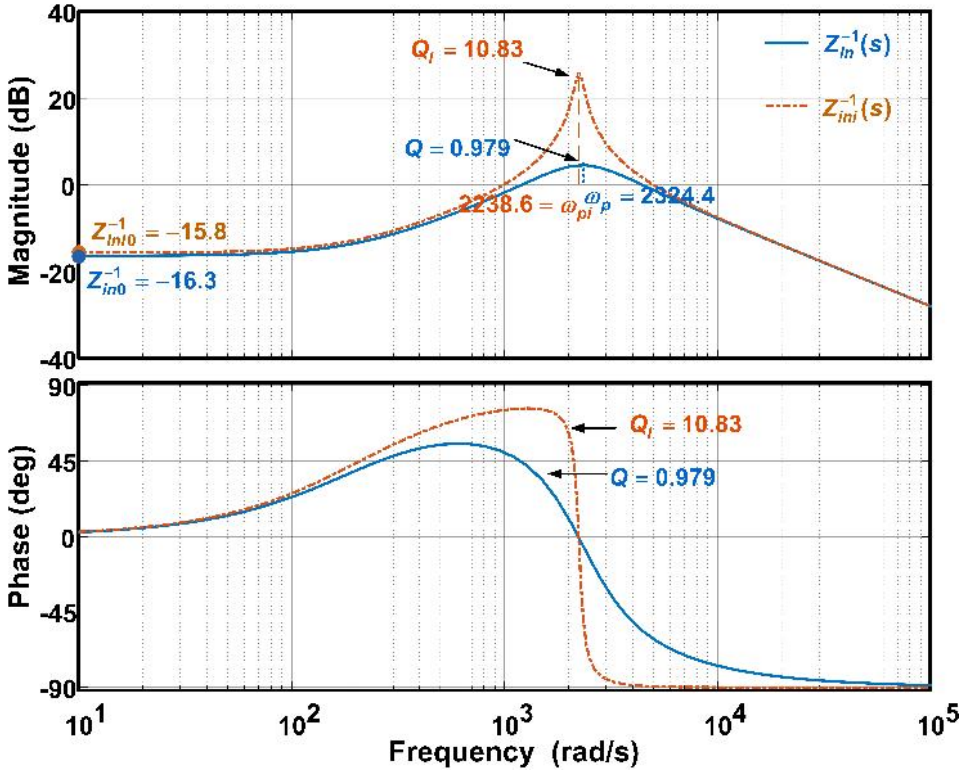


Figure 2.44: Frequency responses comparison of ideal and non-ideal models.

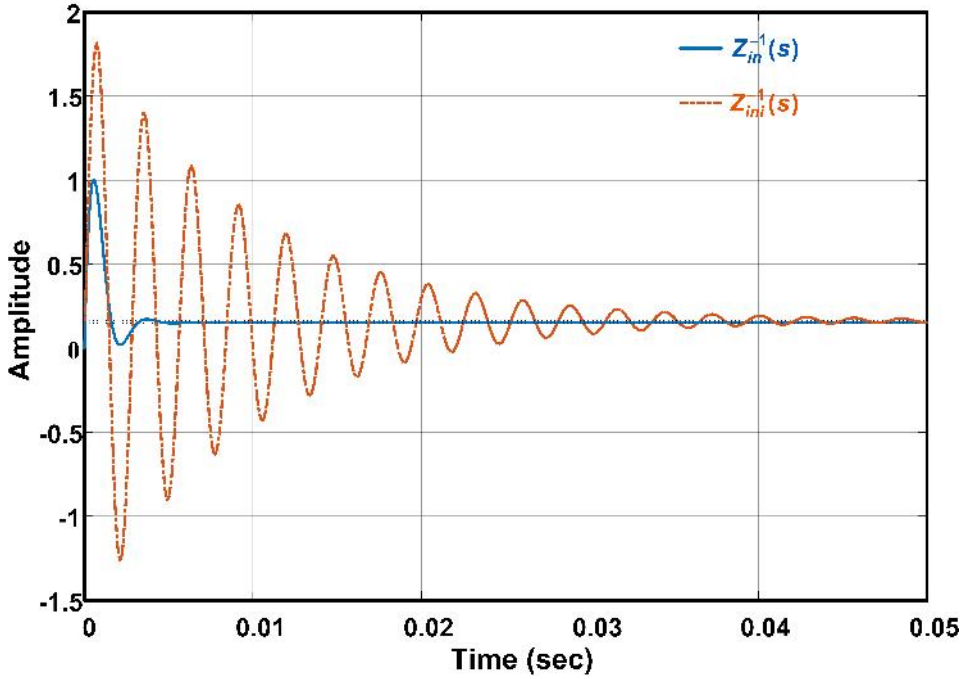


Figure 2.45: Step responses comparison of ideal and non-ideal models.

$$Z_{ini}^{-1}(s) = \frac{0.1649\left(\frac{s}{206.6}+1\right)}{\left(\frac{s}{2238.526}\right)^2 + \frac{s}{25254.598}+1} \tag{2.151}$$

Figures 2.44 and 2.45, show the frequency and step responses of input current to input voltage transfer functions of ideal and non-ideal models respectively. From the Bode plot, it is observed that the input impedance is $Z_{in} = 6.57\Omega$ at low frequencies or dc and it is minimum at corner frequencies. Phase is decreasing from 0 to -90, as frequency increasing. From step responses, it is observed that the steady state error is zero in both cases, but ideal is more oscillatory.

2.10 Conclusions

An improved relationship for calculating the duty cycle of a non-ideal DC-DC PWM boost converter has been developed. It has been shown that the duty cycle calculated using conventional formula results in lesser output voltage than desired. Further, the design equations of inductor and capacitor have been modified based on the non-idealities present in different elements. It is shown that the inductor design, ICR, capacitor design and OVR are the interdependent on each other. So, it is concluded that the ICR of the inductor has significant effect on capacitor design and ESR of the capacitor also effects the inductor design. Moreover, it has been analysed that the ESR of output capacitor plays a significant role in output voltage ripples. Finally, these design formulas are recommended to the power electronic engineers in precise design of boost converter modules.

Even though the most of presented work shows open-loop operation, it will give the crucial information of the maximum achievable output voltage and minimum input voltage specification, which is the base for operating a converter in a closed-loop, which will help control engineers in accurate control design of DC-DC boost converter in applications such as aerospace, military etc. The dynamic performance analysis of the converter concludes that the parasitics are improving the closed-loop stability of the system.

Finally, from experimental results, it is concluded that the complete non-ideal model of the boost converter is essential to evaluate the performances of new control methodologies. Since the non-ideal model is almost as accurate as the practical

system. Therefore, it is advised to use the presented non-ideal transfer function model of the boost converter to design robust controllers.

CHAPTER 3

NON-IDEAL DC-DC BUCK-BOOST CONVERTER

This chapter presents different design issues and accurate mathematical modeling of non-ideal buck-boost converter in detail. The steady-state and dynamic analysis of non-ideal buck-boost converter are explained. Various transfer functions are derived and analyzed the effect of non-idealities.

3.1 Background and Motivation

A PWM DC-DC buck-boost converter is used for step up/down voltage circuit, which is derived of basic topologies of DC-DC converters (Buck and Boost). The variety features of buck-boost converter, which make it suitable option for different kind of applications. Especially in PFC, solar etc., where other basic topologies suffered from some drawbacks [167]- [170].

In view of these applications, similar to previous chapter analysis, buck-boost converter also needs an accurate and optimal design, analysis. As most of the literature [1]- [4] presents the design and analysis of buck-boost converter by considering the ideal nature of elements. Some articles [43], [44], [49], [171]- [173] presented the analysis by including some of the non-idealities. Thus, in present work, the component design and analysis of DC-DC buck-boost converter operating in CCM (continuous conduction mode), performed by considering the all parasitic elements. Here, a little overview of the existing work and explains the presented analysis.

Ideally, the duty cycle expression of buck-boost converter working in CCM is given by [2]- [4]

$$D_{ideal} = \frac{|V_o|}{V_g + |V_o|} \tag{3.1}$$

where, V_g and V_o are the input and output voltages, respectively. Although, this is widely used expression for calculating the duty cycle of buck-boost converter, but it

does not yield the precise output voltage. The reason for this, is the loss of power in parasitics of converter elements. Thus, in present work, a precise expression of the duty cycle for DC-DC buck-boost converter in terms of converter parasitics is derived. From this accurate expression, some vital information like maximum possible duty cycle and achievable output voltage can be obtained. These derivations will be useful to control and power engineers for the design and closed-loop performance evaluation of DC-DC buck-boost converter. Along with this, the commonly used expressions for the design of inductor and capacitor [2]- [4] are also modified, which are more accurate.

Further, the assessment of OVR is an another main concern of DC-DC power converters [47, 51], predominantly in sensitive applications like aerospace, distributed generation and military [8, 22]. Generally, the capacitor's ESR plays a key role in OVR of any DC-DC converter. However, it can be observed that OVR is approximately proportional to ESR of the capacitor. Hence, in present work, the ripple analysis is shown in detail. The maximum allowable ESR for a given OVR and ICR is thrived and shown that beyond a ESR value, OVR is uncontrollable.

Besides this, a small signal analysis of DC-DC buck-boost converter is carried out by considering all the non-idealities. Although a similar analysis is presented in literature [4, 49, 174]. Whereas, in the current work, an extensive analysis is made from control point of view, such as effect of parasitics on the model of DC-DC buck-boost converter. Alongside, the transfer function model of complete non-ideal buck-boost converter is presented.

The following sections discusses the detailed design issues and modeling analysis of non-ideal dc-dc buck-boost converter.

3.2 Fundamental Analysis

This section presents the preliminary equations of non-ideal DC-DC buck-boost converter operating in CCM. Basic non-ideal buck-boost converter system is shown in Figure 3.1(a). In this figure elements are represented as switch (S), diode (D_d), in-

ductor (L), capacitor (C) and load resistance (R). To acquire precise model of buck-boost converter, all parasitic resistances are considered such as source resistance (r_g), inductor resistance (r_L), switch resistance (r_{on}), diode resistance (r_d), diode forward voltage drop (v_{fd}), capacitor ESR (r_c). Further, V_g , v_o, v_c and v_L are input, output, capacitor and inductor voltages, respectively. Alongside, i_L, i_c are inductor and capacitor currents, respectively, and D is duty cycle.

Here, we have made few assumptions [4] for analysing the PWM DC-DC buck-boost converter.

Assumption 1: PWM DC-DC buck-boost converter is operating in continuous conduction mode (CCM). In CCM operation, converter works in two switching intervals: (a) ON time interval, *i.e.*, $0 < t \leq DT$ and (b) OFF time interval, *i.e.*, $DT < t \leq T$.

Assumption 2: Initial charging current through inductor is zero, *i.e.,* $i_L(0) = 0$ and initial voltage across the capacitor is zero, *i.e.,* $v_c(0) = 0$.

3.2.1 Energy storing phase ($0 < t \leq DT$)

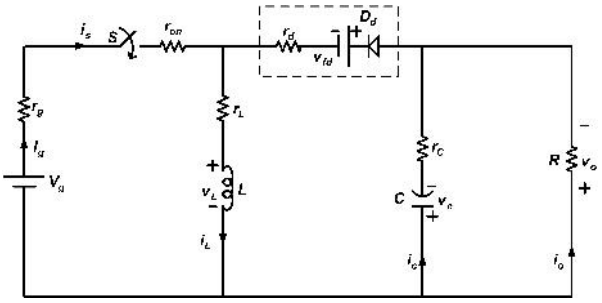
The equivalent circuit for buck-boost converter during interval $0 < t \leq DT$ *i.e.,* ON period is shown in Figure 3.1(b). In this interval, the diode (D_d) is OFF and switch is replaced by its ON time resistance (r_{on}). Here, the input current (i_g) is same as inductor current (i_L). Diode current (i_d) is zero. During this period, the inductor stores energy, and the output capacitor alone powers the load. The wave forms corresponding to this interval are also shown in Figure 3.1(d).

Using Kirchhoffs voltage law (KVL) and Kirchhoffs current law (KCL), the fundamental equations for the circuit shown in Figure 3.1(b) are obtained as follows:

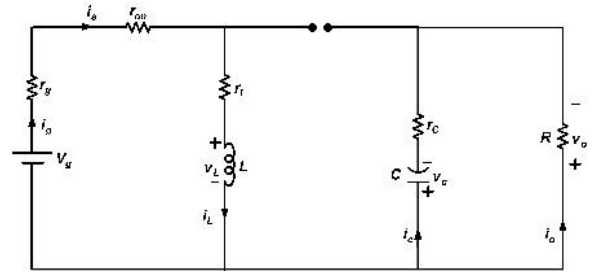
$$(v_L(t))_{ON} = L\frac{di_L(t)}{dt} = -\left[r_g + r_{on} + r_L\right] i_L(t) + v_g(t) \tag{3.2}$$

$$(i_c(t))_{ON} = C\frac{dv_c(t)}{dt} = -\frac{v_o(t)}{R} \tag{3.3}$$

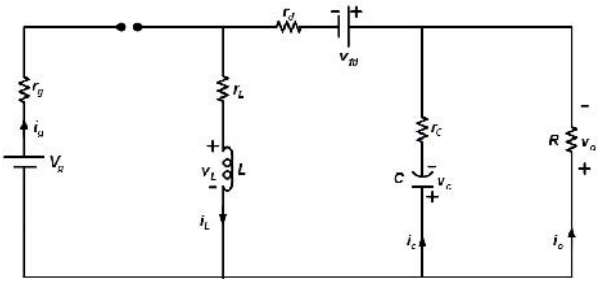
$$(v_o(t))_{ON} = v_c(t) + r_c i_c(t) \tag{3.4}$$



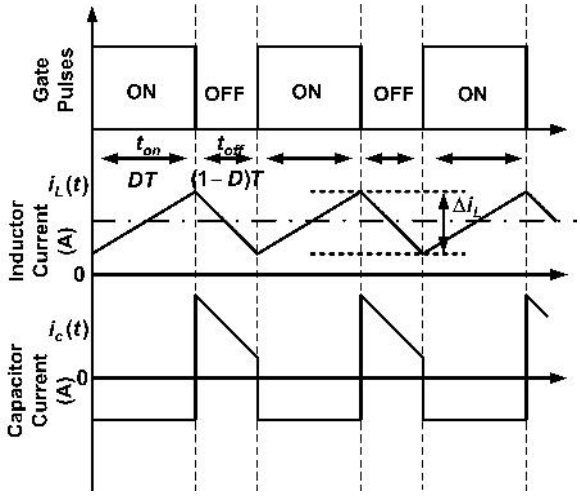
(a)



(b)



(c)



(d)

Figure 3.1: Schematic of (a)non-ideal DC-DC buck-boost converter (b)during ON time (c)during OFF time (d) related waveforms.

3.2.2 Energy releasing phase ($DT < t \leq T$)

The equivalent circuit for buck-boost converter during interval $DT < t \leq T$ *i.e.,* OFF period is shown in Figure 3.1(c). In this interval, the switch (S) is OFF and diode (D_d) is ON. Here, the diode (D_d) is replaced by its equivalent model, *i.e.,* resistance (r_d) in series with forward voltage (v_{fd}). The input current (i_g) is zero. In this interval, the stored inductive energy contributes to supply the output. The capacitor charges by inductor and supply, then discharges through load. The wave forms corresponding to this interval are also shown in Figure 3.1(d).

Using KVL and KCL, the fundamental equations for the circuit shown in Figure 3.1(c) are obtained as follows:

$$(v_L(t))_{OFF} = L\frac{di_L(t)}{dt} = -(r_L + r_d + \frac{Rr_c}{R+r_c})i_L(t) - \frac{R}{R+r_c}v_c(t) - V_{fd} \tag{3.5}$$

$$(i_c(t))_{OFF} = C\frac{dv_c(t)}{dt} = i_L(t) - \frac{v_o(t)}{R} \tag{3.6}$$

$$(v_o(t))_{OFF} = v_c(t) + r_c i_c(t) \tag{3.7}$$

3.3 Steady State Analysis

In this context of analysis, voltages and currents are supposed to be constant over a switching period and are illustrated by equilibrium state values as follows:

$$i_L(t) = I_L, v_g(t) = V_g, v_C(t) = V_C$$

According to volt-sec balance [4], in equilibrium state, the average voltage across inductor equal to zero. Therefore, using (3.2) and (3.5), we write,

$$V_L = \frac{1}{T}\int_0^T v_L(t)dt = \frac{1}{T}\left(\int_0^{t_{on}=DT}(v_L(t))_{ON}dt + \int_{t_{on}=DT}^{t_{off}=(1-D)T}(v_L(t))_{OFF}dt\right) = 0 \tag{3.8}$$

Likewise, in equilibrium state, according to charge balance [4], the average current through capacitor equal to zero. Therefore, using (3.3) and (3.6), we get,

$$I_C = \frac{1}{T}\int_0^T i_C(t)dt = \frac{1}{T}\left(\int_0^{t_{on}=DT}(i_C(t))_{ON}dt + \int_{t_{on}=DT}^{t_{off}=(1-D)T}(i_C(t))_{OFF}dt\right) = 0 \tag{3.9}$$

The equilibrium state output voltage is

$$V_o = \frac{1}{T}\int_0^T v_o(t)dt = \frac{1}{T}\left(\int_0^{t_{on}=DT}(v_o(t))_{ON}dt + \int_{t_{on}=DT}^{t_{off}=(1-D)T}(v_o(t))_{OFF}dt\right) = 0 \tag{3.10}$$

Substitute (3.3) and (3.6) in (3.8), we get,

$$\begin{aligned} V_L &= D\left[-I_L\left(r_g + r_L + r_{on}\right) + V_g\right] + (1-D)\left[\begin{array}{l} -I_L\left(r_L + r_d + \left(\frac{Rr_c}{R+r_c}\right)\right) \\ -V_c\frac{R}{R+r_c} - V_{fd} \end{array}\right] = 0 \\ \Rightarrow \frac{V_C R}{R+r_C} &= \frac{DV_g}{1-D} - V_{fd} - \frac{\left(r_L + D(r_g+r_{on}) + (1-D)\left(r_d + \frac{Rr_C}{R+r_C}\right)\right)I_L}{1-D} \end{aligned} \tag{3.11}$$

Substitute (3.4) and (3.7) in (3.9), we get,

$$\begin{aligned} I_C &= D\left(-\frac{V_o}{R}\right) + (1-D)\left(I_L - \frac{V_o}{R}\right) = 0 \\ \Rightarrow I_L &= \frac{V_o}{(1-D)R} = \frac{I_o}{(1-D)} \end{aligned} \tag{3.12}$$

Here, I_o is the steady-state value of load current. Substitute (3.5) and (3.6) in (3.10), we get,

$$\begin{aligned} V_o &= D\left(V_C + I_C r_C\right) + (1-D)\left(V_C + I_C r_C\right) \\ \Rightarrow V_o &= V_C \end{aligned} \tag{3.13}$$

3.3.1 Output voltage expression

Substitute (3.12) and (3.13) into (3.11), we get,

$$\frac{V_o R}{R+r_C} = \frac{DV_g}{1-D} - V_{fd} - \frac{\left(r_L + D\left(r_g + r_{on}\right) + (1-D)\left(r_d + \frac{Rr_C}{R+r_C}\right)\right)V_o}{R(1-D)^2} \tag{3.14}$$

$$\Rightarrow V_o\left[\frac{\left(r_L + D\left(r_g + r_{on}\right) + D^{'}r_d\right)\left(R + r_C\right) + D^{'}R\left(D^{'}R + r_C\right)}{D^{'}R\left(R + r_C\right)}\right] = DV_g - D^{'}V_{fd}$$

Finally, we get output voltage expression as

$$\Rightarrow V_o = \frac{[DV_g - D^{'}V_{fd}]D^{'}R\left(R + r_c\right)}{[(r_L + D(r_{on} + r_g) + D^{'}r_d)(R + r_c)] + [D^{'}R(D^{'}R + r_c)]} \tag{3.15}$$

Further, we can write

$$V_o = \frac{MV_g}{1 + \frac{V_{fd}}{V_o} + \frac{(1+M)}{R}\left[\ M(r_g + r_L + r_{on}) + r_L + r_d\ \right] + \frac{Mr_c}{R+r_c}}. \tag{3.16}$$

Table 3.1: Parameters of DC-DC buck-boost converter

Parameters	Value
Input voltage (Battery) (V_g)	12V
Source resistance (r_g)	0.3 Ω
Ferrite core inductor (L/r_L)	392 μH/ 0.34Ω
Electrolytic capacitor (C/r_c)	100 μF/ 0.2Ω
Diode (MUR1560) forward drop (V_{fd})	0.5V
Diode resistance (r_d)	0.03 Ω
Switch (IRFP460) resistance (r_{on})	0.05 Ω
Switching frequency (f)	20KHz
Load resistance (R)	22Ω

Where, $M = \frac{D}{1-D}$.

From (3.16), the dc voltage gain of buck-boost converter is

$$\begin{aligned} M_{V_{dc}} &= \frac{V_o}{V_g} \\ &= \frac{M}{1+\frac{V_{fd}}{V_o}+\frac{(1+M)}{R}\Big[\ M(r_g+r_L+r_{on})+r_L+r_d\ \Big]+\frac{Mr_c}{R+r_c}} \end{aligned} \tag{3.17}$$

If all parasitics are zero in (3.17), then we obtain the ideal formula for calculating the output voltage of buck-boost converter as

$$V_o = MV_g = \frac{DV_g}{D'}. \tag{3.18}$$

In an ideal PWM DC-DC buck-boost converter, the output voltage is a function of duty cycle and input voltage only. However, by including non-idealities, the output voltage V_o of PWM DC-DC buck-boost converter is not only function of duty cycle D and input voltage V_g but also the load resistance R and other parasitic elements, which is shown in Eq. (3.15).

The plot of output voltage V_o as a function of duty cycle D is shown in Figure 3.2 for ideal case and non-ideal case at different load resistances (R) and other parameters are constant. For the ideal case, the converter output voltage increases

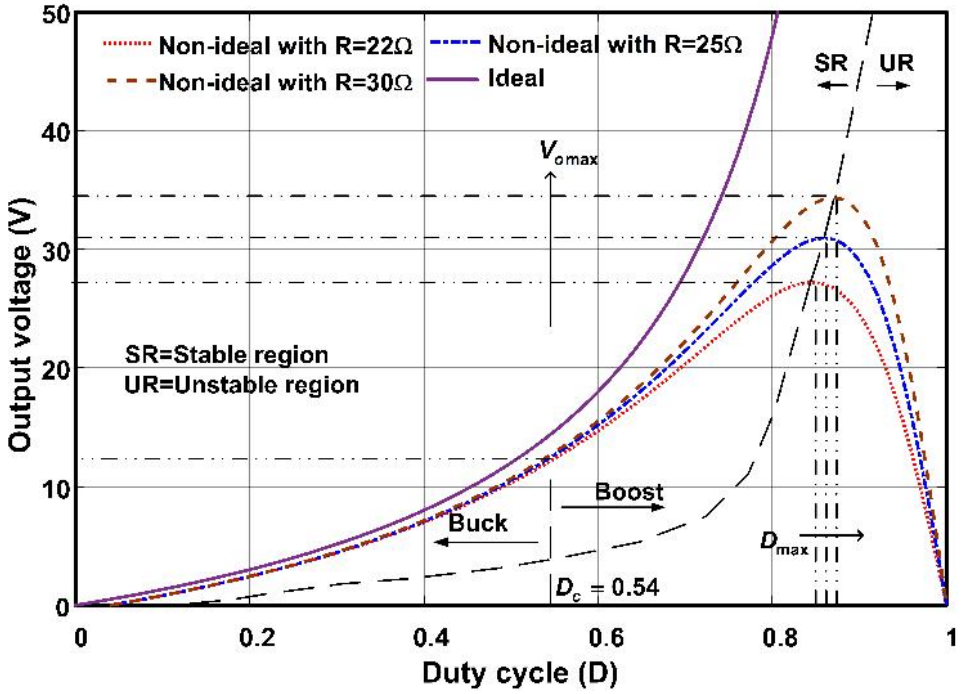


Figure 3.2: Output voltage of buck-boost converter as a function of duty cycle for different load resistances and fixed input voltage.

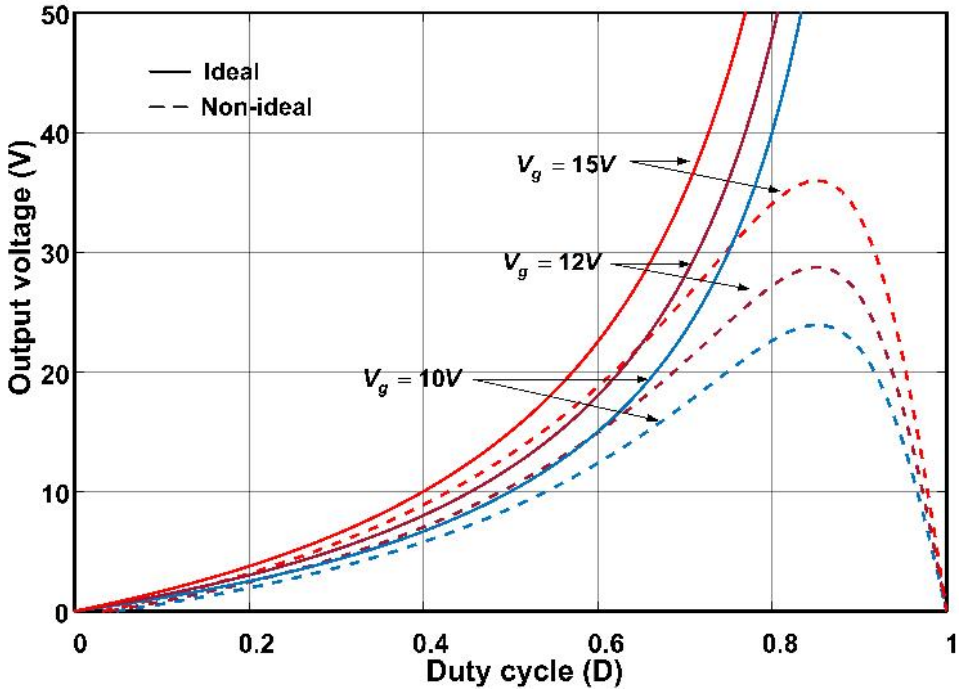


Figure 3.3: Output voltage of buck-boost converter as a function of duty cycle for different input voltages and fixed load resistance.

with duty cycle. On the other hand, for the non-ideal case, the output voltage first increases with duty cycle, reaches its maximum value, and then decreases to zero at duty cycle close to unity. The output voltage is dependent on load resistance. At a particular value of duty cycle, as the load resistance decreases, the output voltage also drops significantly. For any fixed duty cycle, the difference between ideal dc output voltage and non-ideal dc output voltage increases with decrease in load resistance. This is because of the increased voltage drop across the non-idealities in practical buck-boost converter at lower load resistance (or higher load current). As the load resistance increasing, the V_{omax} and D_{max} are also increasing.

The plot of output voltage V_o as a function of duty cycle D is shown in Figure 3.3 for ideal case and non-ideal case at different input voltages (V_g) and other parameters are constant. For a particular duty cycle, the difference between the output voltage of an ideal and non-ideal buck-boost converter becomes larger as input voltage increases. So in the presence of parasitics, switch should kept ON for long time to get the same output voltage. As the input voltage decreases, V_{omax} also decreasing in non-ideal case. This V_{omax} is decreases because of input voltage variation. From this, we get the information of minimum input voltage (V_{gmin}) to be applied for converter at fixed output voltage (in regulator problems).

Therefore, it is clear that the output voltage of a practical buck-boost converter is always less than the ideal buck-boost converter, if the MOSFET switch of practical buck-boost converter is operated at a duty cycle which satisfies the relation in Eq. (3.18). It is because, this relation is for ideal buck-boost converter which neglects the non-idealities present in practical buck-boost converter. Therefore, to achieve the desired output voltage from a practical buck-boost converter, duty cycle should be obtained by satisfying the input-output voltage relationship in Eq. (3.15). This will be the practical duty cycle and greater than the ideal one as given in (3.1).

3.3.2 Modified duty cycle expression

It is easily noticeable that the output voltage of a non-ideal buck-boost converter (*i.e.,* practical) is always less than the ideal buck-boost converter. Since, the relation for an ideal case, which neglects the parasitics present in practical buck-boost converter. So, there is a need to develop the improved expression for duty cycle, which is as follows:

Rewriting (3.16),

$$V_{fd}(R+r_c)+\frac{V_o(R+r_c)}{(1-D)R}\left(\frac{D}{1-D}(r_g+r_{on})+\frac{r_L}{1-D}+r_d\right)+\frac{DV_or_c}{1-D}+V_o(R+r_c)=\frac{DV_g}{1-D}(R+r_c) \tag{3.19}$$

Further, above expression can be expressed as quadratic equation in terms of $D^{'}$ or $1-D$, which is written as follows:

$$(D')^2\underbrace{\left[V_oR^2+R(R+r_c)(V_g+V_{fd})\right]}_{a}+D'\underbrace{\begin{bmatrix}-V_gR(R+r_c)+\\ V_o(r_d-r_g-r_{on})(R+r_c)-Rr_c\end{bmatrix}}_{b}$$
$$+\underbrace{V_o\left(r_g+r_{on}+r_L\right)\left(R+r_c\right)}_{c}=0 \tag{3.20}$$

The solution of quadratic equation will be,

$$D^{'}=\frac{-b\pm\sqrt{b^2-4ac}}{2a} \tag{3.21}$$

The practicable or realizable duty cycle falls under negative sign. Therefore, the improved expression for duty cycle of a practical DC-DC buck-boost converter is obtained as given in Eq. (3.22).

$$D^{'}=D^{'}_{ideal}\frac{a_1-\sqrt{a_1^2-4a_2}}{2a_3}. \tag{3.22}$$

Where,

$$a_1=1+\frac{V_o}{V_g}\left(\frac{-r_d+r_{on}+r_g-R\parallel r_c}{R}\right),$$
$$a_2=\left[\frac{V_o}{V_g}\right]^2\left[\frac{R}{R+r_c}+\frac{V_g+V_{fd}}{V_o}\right]\left[\frac{r_g+r_L+r_{on}}{R}\right],$$

$$a_3 = \left[\left(\frac{R}{R+r_c}\right)\left(\frac{V_o}{V_o+V_g}\right) + \left(\frac{V_{fd}+V_g}{V_o+V_g}\right)\right].$$

The duty cycle calculated using (3.22) results in exact practical value of output volt-

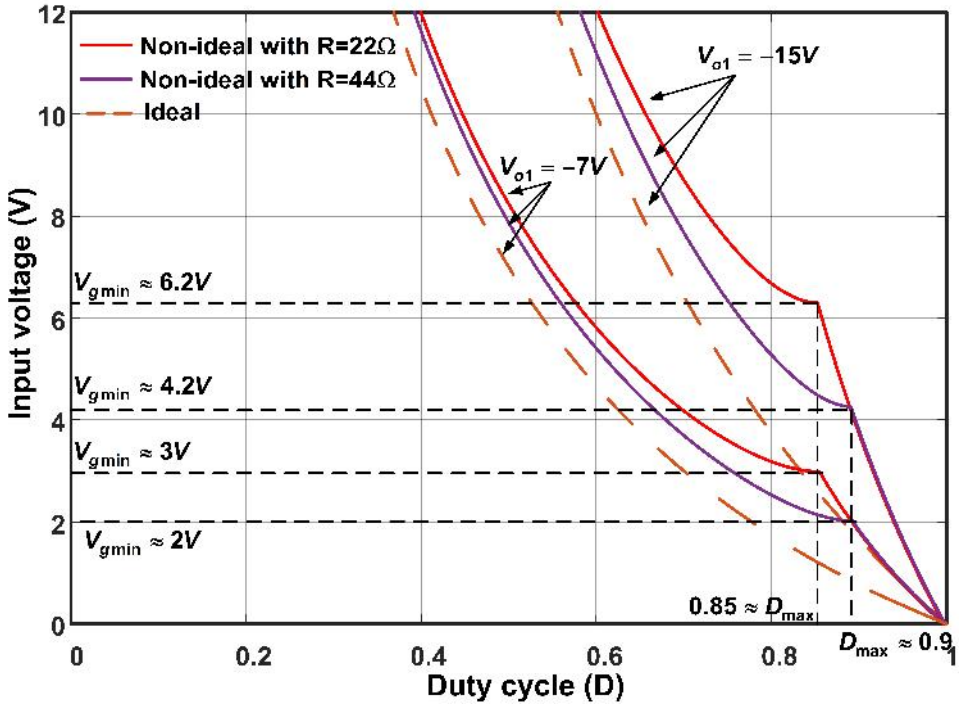


Figure 3.4: Output voltage of buck-boost converter as a function of duty cycle for a fixed output voltage when both input voltage and load resistance are varying.

age V_o. Here, two duty cycles are not able to realize the same output voltage. The realizable value for duty cycle is obtained with minus sign. Let us consider the values from Table 3.1, then we obtain two duty cycle values as $D_1^{'} = 0.004$ and $D_2^{'} = 0.601$. From these values, it is observable that $D_1 = 0.996$ is in unstable operating region of the converter as shown in Figure (3.2), so this is not the desired duty cycle. Whereas, other term gives the desired value $(D_2 = 0.399)$. So, only one duty cycle is considered which is realizable. Further sections, validation of this analysis has been carried out by simulations and experiments.

3.3.3 Maximum achievable duty cycle and output voltage

Figure 3.2 and previous section analysis explains the importance to derive the maximum value of duty cycle. The derivation as follows:

Rewriting (3.15),

$$V_o = \frac{[DV_g - D^{'}V_{fd}]D'R\,(R + r_c)}{[(r_L + D(r_{on} + r_g) + D^{'}r_d)(R + r_c)] + [D^{'}R(D^{'}R + r_c)]}$$

This can be written as given in (3.23),

$$V_o = \frac{R\,(R + r_c)\,(-D^2\,(V_g + V_{fd}) + D\,(V_g + 2V_{fd}) - V_{fd})}{D^2R^2 + D\,((r_{on} + r_g - r_d - R)\,(R + r_c) - R^2) + (R + r_L + r_d)\,(R + r_c)} \quad (3.23)$$

From above expression, it is observed that V_o is function of D. Now, maximum value of this expression can be found as follows:

$$\frac{\partial V_o}{\partial D} = 0 \quad (3.24)$$

Therefore, by differentiating V_o with respect to D and equating to zero, we get the expression of maximum permissible duty cycle (D_{max}) as follows:

$$D_{max1,max2} = \frac{-\,(2\,(a_1b_3 - b_1a_3)) \pm \sqrt{(2\,(a_1b_3 - b_1a_3))^2 - 4\,(a_1b_2 - a_2b_1)\,(a_2b_3 - a_3b_2)}}{2\,(a_1b_2 - a_2b_1)} \quad (3.25)$$

where,

$a_1 = -R\,(R + r_c)\,(V_g + V_{fd})\,;$

$a_2 = R\,(R + r_c)\,(V_g + 2V_{fd})\,;$

$a_3 = -R_L\,(R + r_c)\,V_{fd}; b_1 = R^2;$

$\mathrm{b}_2 = (r_{on} + r_g - r_d - R)\,(R + r_c) - R^2;$

$b_3 = (R + r_L + r_d)\,(R + r_c)\,.$

Here, two values of duty cycles are obtained from (3.25). Two duty cycles are not able to realize the same output voltage. Only one value of the duty cycle *i.e.,* D_{max2} (which is obtained with minus sign) will give the desired or realizable output voltage. Let us consider the values (from Table 3.1), we obtain two duty cycle values as $D_{\max 1} = 1.21, D_{\max 2} = 0.8526$. From these values, it is clear that $D_{\max 1}(= 1.21) > 1$, which is not possible to realize. So ,only one duty cycle is considered which is realizable. Further sections, validation of this analysis done by simulations and experiments.

By substituting Eq. (3.25) in Eq. (3.15), the maximum achievable voltage (V_{omax}) with the given converter can be determined as,

$$V_{omax} = \frac{[D_{max}V_g - D^{'}_{max}V_{fd}]D^{'}_{max}R\,(R + r_c)}{[(r_L + D_{max}(r_{on} + r_g) + D^{'}_{max}r_d)(R + r_c)] + [D^{'}_{max}R(D^{'}_{max}R + r_c)]} \quad (3.26)$$

3.3.4 Effect of parasitics

Even though the parasitics of the converter are almost constant during operation, they may change when there is temperature changes because of long term operation of converter or external means. However, in Figure 3.5 shows the effect of parasitics on duty cycle versus output voltage characteristics while keeping input voltage and load resistances constant. These observations have been tabulated in Table 3.2.

Table 3.2: Parasitic effect on output voltage versus duty cycle characteristics

	D_{max}	V_{omax}
As $r_g \uparrow$	$\downarrow$	$\downarrow$
As $r_L \uparrow$	$\downarrow$	$\downarrow$
As $r_C \uparrow$	negligible effect	Slightly $\downarrow$
As $r_{on} \uparrow$	negligible effect	Slightly $\downarrow$
As $r_d \uparrow$	negligible effect	negligible effect
As $V_{fd} \uparrow$	no effect	no effect

3.4 Outcomes for Closed-loop Control

Here, from this analysis, we summarized some important observations, which are handy in a closed-loop operation, as given below:

1. Practical buck-boost converter system always has lower output voltage compared to ideal case. So, in order to get the similar duty cycle value in practical as well as theory, the derived expression (3.22) is essential.

2. Maximum achievable duty cycle (D_{max}) and maximum output voltage (V_{omax}) are two crucial parameters to know for before the closed-loop operation of converter.

3. From Figure 3.5, it can be observed that each parasitic element effects the D_{max} and V_{omax}. It is also shown in Table 3.2.

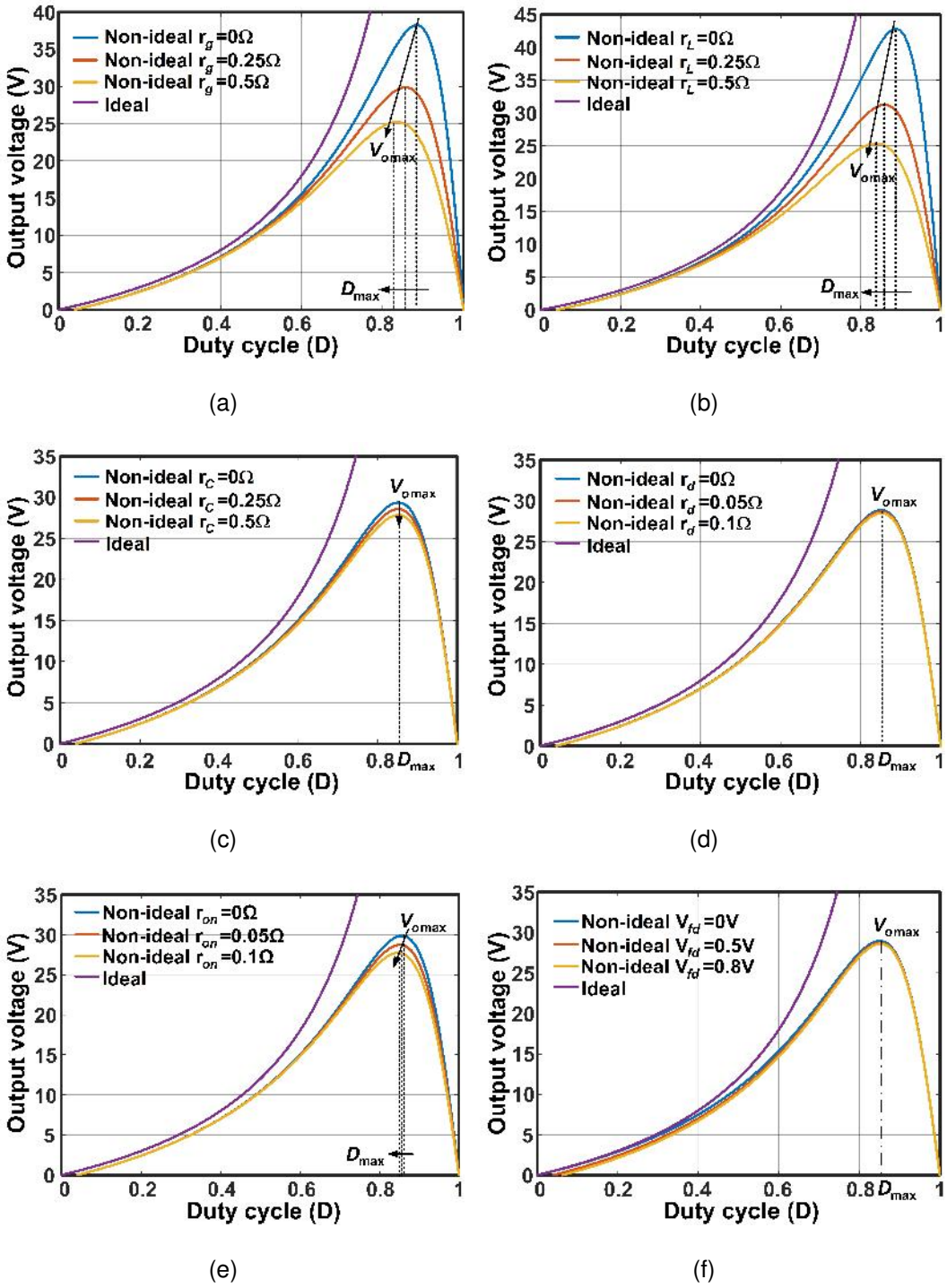


Figure 3.5: Output voltage of buck-boost converter as a function of duty cycle (a) for different source resistance values (b) for different inductor ESR values (c) for different capacitor ESR values (d) for different diode resistance values (e) for different switch resistance values (f) for different diode forward drop voltages.

4. From Figure 3.2, it is clear that converter may operate in unstable region for sudden changes in input or load. In order to avoid this, confine the controller output to D_{max}, which is shown in Figure 3.6.

5. From Figures 3.3 and 3.4, it can be observed that the operating range of input voltage is limited to V_{gmin}, to obtain the specific value of output.

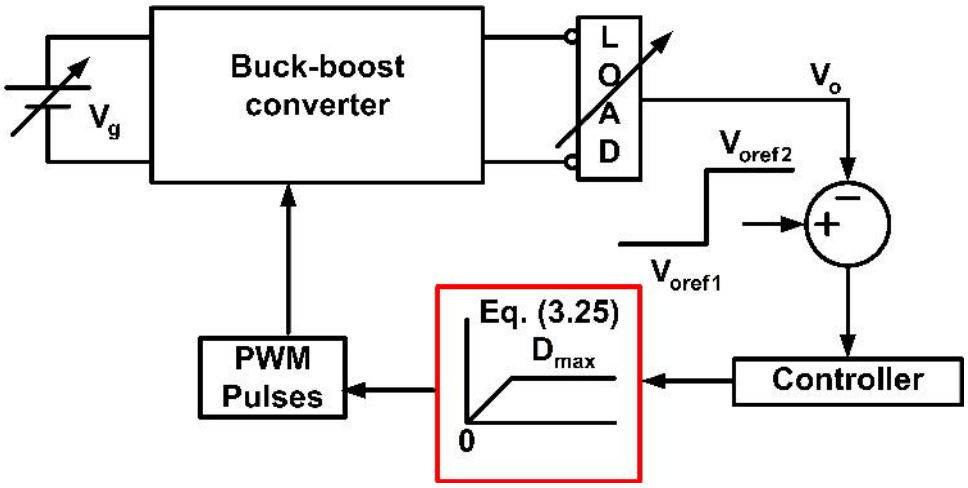


Figure 3.6: Diagramatic representation to use limiter (limits to D_{max}) in closed-loop operation.

The following illustrative example will explain the details of above discussed outcomes:

Illustrative example 1: Suppose, buck-boost converter is operating in closed-loop to get the output value of V_{ref1} at steady-state. If there is sudden change of set-point value from V_{ref1} to V_{ref2}, then how to get the stable operation of converter ?

From observation (2), it is clear that the maximum of V_{omax} can be achieved by the buck-boost converter at D_{max}. Let assume that V_{ref1} can be obtained at $D = D_1$ and $D_1 < D_{max}$. If there is sudden change in the set-point value from V_{ref1} to V_{ref2}, then the duty cycle will be adjusted to achieve V_{ref2}. But, here in two different cases, converter may lead to unstable operation. The first case will be $V_{ref2} > V_{omax}$ and second case is that the change in set point value is very large such that converter

may forced to operate more than D_{max} for an instance. In first case, output may not be reached to set-point value, since it is more than the achievable limit of converter. So, at least to avoid collapse of voltage, put a limiter at the end of controller as shown in Figure 3.6. Therefore, steady state value will be V_{omax} and there is no collapse in voltage.

The second case is an interesting one, even though the set-point value is within the limits, converter may become unstable. This is because, error in sudden change may force duty cycle for an instance to operate at D_2, which will be more than D_{max}. At that instance, voltage will be collapsed. So, if limiter is used, then this condition will be easily handled. This limiter will not allow to enter into unstable region of converter and further it will settle to V_{ref2}.

3.5 Design of Filter Elements

3.5.1 Inductor current ripple (ICR) and Inductor design

Design of inductor is an another important issue for buck-boost converter. Generally, inductance value mostly depends on the ICR and switching frequency. So, in this section, the effect of non-idealities is analysed on inductors design and inductor ripple current. Let x_L be inductor current ripple factor (ICRF) for inductor L, such that

$$x_L = \frac{\Delta i_L}{I_L}. \tag{3.27}$$

Here, I_L is average current through inductor L.

From (3.2), the rate of change of inductor current i_L can be assumed constant over one cycle in steady-state *i.e.,*

$$\frac{\Delta i_L}{\Delta t} = \frac{-I_L(r_g + r_L + r_{on}) + V_g}{L} \tag{3.28}$$

For ON-period $\Delta t = DT_s$, the magnitude of ICR (Δi_L) can be written as

$$\Delta i_L = \frac{V_g - I_L(r_g + r_L + r_{on})}{L} DT \tag{3.29}$$

Substituting value of I_L from (3.12) and simplifying,

$$\Delta i_L = \frac{DV_o}{Lf}\left[\frac{V_g}{V_o} - \frac{r_g + r_L + r_{on}}{RD'}\right] \tag{3.30}$$

Here $f = \frac{1}{T}$ is the switching frequency of buck-boost converter. Equation (3.17) can be written as,

$$\frac{V_g}{V_o} = \frac{D^{'}V_{fd}}{D} + \frac{\left(r_L + D\left(r_g + r_{on}\right) + D^{'}r_d\right)\left(R + r_C\right) + D^{'}R\left(D^{'}R + r_C\right)}{DD^{'}R\left(R + r_C\right)} \tag{3.31}$$

Substitute (3.31) in (3.30), we get,

$$\Delta i_L = \frac{D^{'}V_o}{Lf}\left[\begin{array}{l} 1 + \frac{V_{fd}}{V_o} + \frac{1}{RD^{'}}\left(\begin{array}{l}\frac{D}{D^{'}}(r_g + r_L + r_{on}) + r_d + r_L\end{array}\right) \\ + \frac{Dr_c}{D^{'}(R+r_c)} - \frac{D(r_g+r_L+r_{on})}{R\left(D^{'}\right)^2}\end{array}\right]. \tag{3.32}$$

Further simplifying, we get ICR expression as

$$\Delta i_L = \frac{V_o}{Lf}\left[\frac{D^{'}V_{fd}}{V_o} + \frac{r_d + r_L}{R} + \frac{D^{'}R + r_c}{R + r_c}\right]. \tag{3.33}$$

or

$$\Delta i_L = \Delta i_{Lideal}\left[\frac{V_{fd}}{V_o} + \frac{r_d + r_L}{D^{'}R} + \frac{D^{'}R + r_c}{D^{'}\left(R + r_c\right)}\right]. \tag{3.34}$$

Where,

$$\Delta i_{Lideal} = \frac{D^{'}V_o}{Lf} \tag{3.35}$$

Substituting $\Delta i_L = x_L I_L = -x_L \frac{V_o}{R_L(1-D)}$ into (3.33), we get the inductor (L) expression as,

$$L = \frac{RD^{'}}{x_L f}\left(\frac{D^{'}V_{fd}}{V_o} + \frac{r_d + r_L}{R} + \frac{D^{'}R + r_c}{R + r_c}\right). \tag{3.36}$$

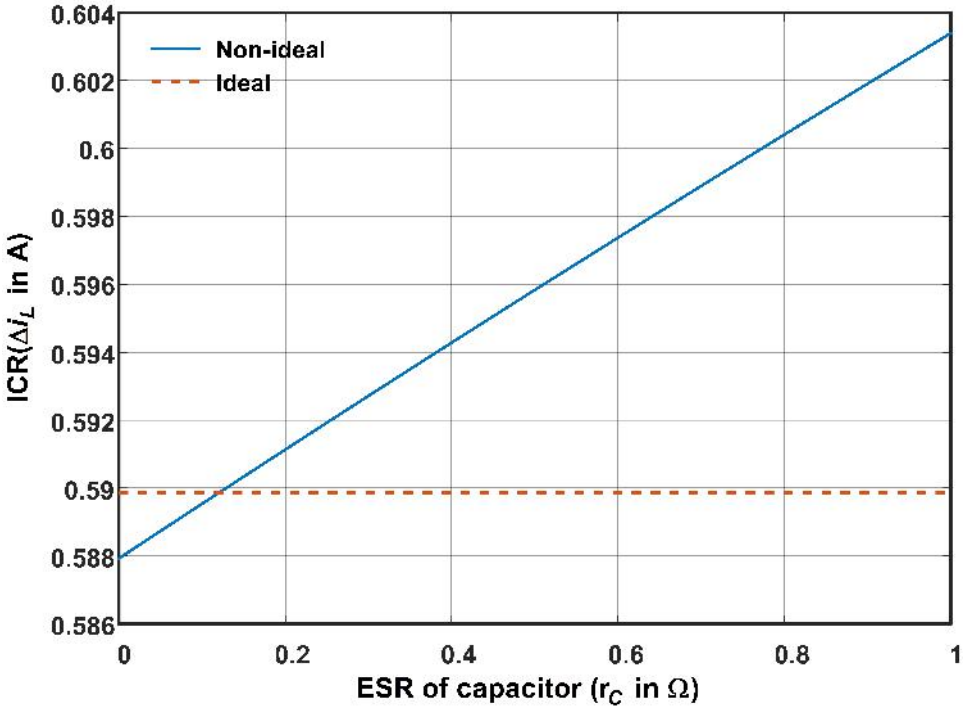
or

$$L = L_{ideal}\left[\frac{V_{fd}}{V_o} + \frac{r_d + r_L}{D^{'}R} + \frac{D^{'}R + r_c}{D^{'}\left(R + r_c\right)}\right]. \tag{3.37}$$

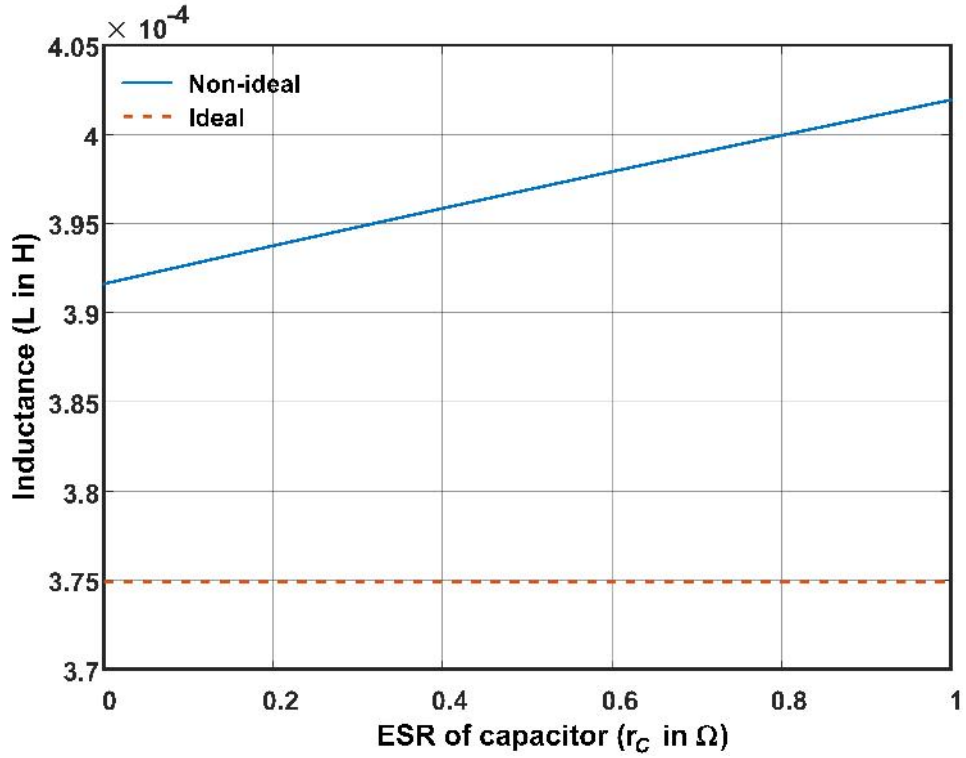
Where,

$$L_{ideal} = \frac{R\left(D^{'}\right)^2}{x_L f}. \tag{3.38}$$

From Eq. (3.35) and (3.38), we can observe that these are same as given in various textbooks to calculate the inductor current ripples and inductance value. However, equations (3.36) and (3.33), gives the actual value of inductance L and ICR in presence of non-idealities.



(a)



(b)

Figure 3.7: Output voltage of buck-boost converter as a function of duty cycle (a) Variation of ICR with respect to capacitor ESR (b) Variation of inductance with respect to capacitor ESR.

3.5.1.1 Effect of parasitics on ICR and inductance

The expressions obtained are analysed and observed that capacitor ESR has noticeable effect on ICR and inductor design, which is shown in Figure 3.7. The expressions (3.34) and (3.37) reveals that there is a additional multiplying factor to the ideal expressions. Here, an important observation from non-ideal design is that the value of inductance and ICR are mainly effected by the ESR of the capacitor though there are other parasitics also present. From Figure 3.7, it is observed that as the capacitor ESR increases, the ICR increases and the inductance required also increases.

3.5.2 Design of Capacitor

Capacitor design is also the very important as inductor design for a buck-boost converter. The voltage across the capacitor will be taken as output voltage in buck-boost converter. Therefore, the capacitor design depends on the allowable OVR and switching frequency. The equivalent series resistance (ESR) of a capacitor plays an important role in design. A capacitor is modelled by its capacitance value and ESR value. In order to design capacitance, the OVR analysis of capacitor is needed.

3.5.2.1 OVR analysis

In any DC-DC converter, the total voltage ripple (Δv_o) of a capacitor is sum of

- Voltage ripples due to its own capacitance (Δv_C)
- Voltage ripples due to its ESR (Δv_{rC}).

Therefore, for proper capacitor design, it becomes necessary to consider the effect of ESR. The capacitor C is used as filter capacitor at output stage. The voltage ripples across this capacitor directly affect the quality of output voltage. Therefore, its design is carried out more carefully to limit the output voltage ripples within permissible range. The capacitor current and different components of voltage ripples in steady state are shown in Figure 3.8. As discussed earlier, output voltage ripple $\Delta v_o(t)$ is

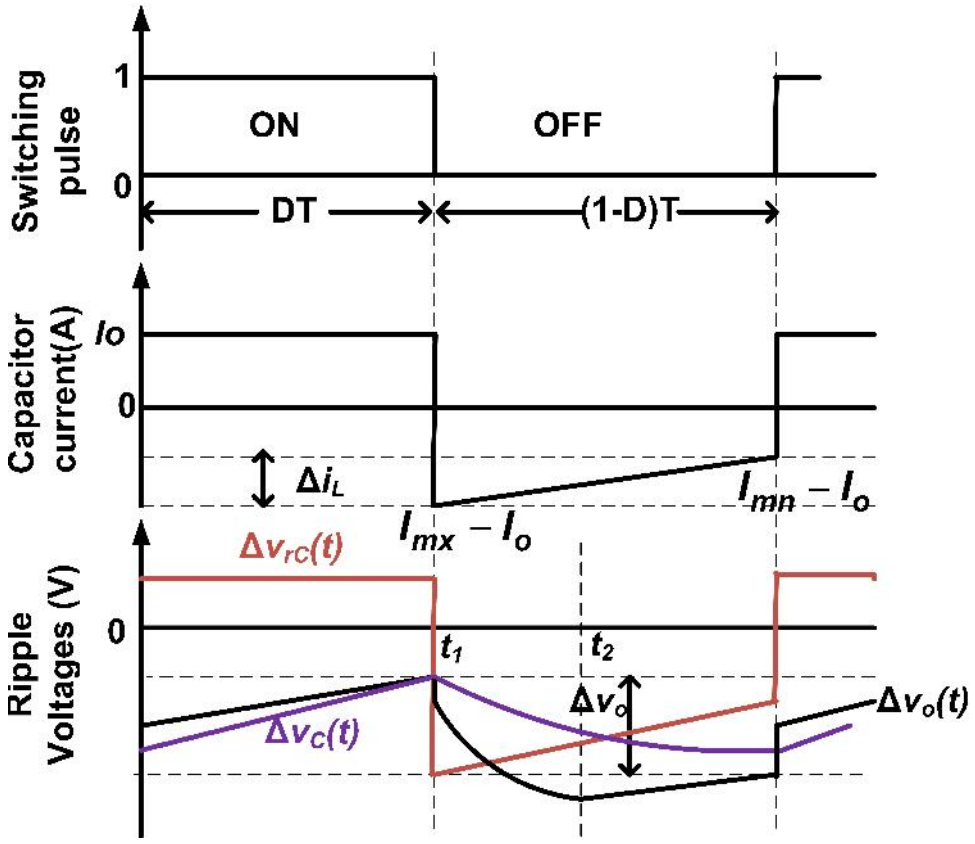


Figure 3.8: Waveforms of switching pulse, capacitor current and ripple voltages.

made up of two components as

$$\Delta v_o(t) \simeq \Delta v_C(t) + \Delta v_{rC}(t) \tag{3.39}$$

Voltage ripples due to ESR, $\Delta v_{rC}(t)$, expressed as

$$\Delta v_{rC}\left(t\right) = r_c i_C\left(t\right) \tag{3.40}$$

Voltage ripples due to capacitor, $\Delta v_C(t)$ expressed as

$$\Delta v_C\left(t\right) = \frac{1}{C}\int_0^t i_C\left(t\right)dt + \Delta v_C\left(t_0\right) \tag{3.41}$$

$\Delta v_C(t_0)$ is initial voltage across capacitor at $t = t_0$.

The detailed analysis is carried out as follows:

3.5.2.2 Analysis during ON time

The current through capacitor C is

$$i_c(t) = I_o. \tag{3.42}$$

Therefore, the voltage ripple contribution due to capacitor ESR is

$$\Delta v_{rC}(t) = r_c i_C(t) = I_o r_c. \tag{3.43}$$

The voltage ripple contribution due to capacitor itself is

$$\Delta v_C(t) = \frac{1}{C}\int_0^t i_C(t)dt + \Delta v_C(0) = \frac{I_o}{C}t + \Delta v_C(0). \tag{3.44}$$

$\Delta v_C(0)$ is initial voltage across capacitor at $t = 0$. Therefore, total OVR during ON time is

$$\Delta v_o(t) = \Delta v_C(t) + \Delta v_{rC}(t) = \frac{I_o}{C}[t + Cr_c] + \Delta v_C(0). \tag{3.45}$$

From (3.45), $\Delta v_o(t)$ represents a line equation. Only minimum value exists for this expression, *i.e.,* at $t_1 = DT$. At $t = t_1$, the voltage ripples obtained as

$$\Delta v_{rc}(t_1) = I_o r_c \tag{3.46}$$

$$\Delta v_C(t_1) = \frac{I_o DT}{C} + \Delta v_C(0) \tag{3.47}$$

$$\Delta v_{o,\min} = \Delta v_o(t_1) = \frac{I_o}{C}[Cr_c + DT] + \Delta v_C(0). \tag{3.48}$$

3.5.2.3 Analysis during OFF time

The capacitor current equation during off time expressed as

$$i_C(t) = \frac{\Delta i_L(t - DT)}{D'T} - (I_{mx} - I_o). \tag{3.49}$$

Therefore, the voltage ripple contribution due to capacitor ESR is

$$\Delta v_{rC}(t) = r_c i_C(t) = \frac{\Delta i_L r_c}{D'T}(t - DT) - (I_{mx} - I_o) r_c. \tag{3.50}$$

The voltage ripple contribution due to capacitor itself is

$$\begin{aligned}\Delta v_C(t) &= \tfrac{1}{C}\int_{DT}^{t} i_C(t)dt + \Delta v_C(DT) \\ &= \tfrac{\Delta i_L (t-DT)^2}{2CD'T} - \tfrac{(I_{mx}-I_o)(t-DT)}{C} + \Delta v_C(DT).\end{aligned} \tag{3.51}$$

$\Delta v_C(DT)$ is initial voltage across capacitor at $t = DT$. Therefore, total OVR during OFF time is

$$\begin{aligned}\Delta v_o(t) &= \Delta v_C(t) + \Delta v_{rC}(t) \\ &= \tfrac{\Delta i_L}{D'T}\left[\tfrac{(t-DT)^2}{2C} + r_c(t-DT)\right] - \tfrac{(I_{mx}-I_o)}{C}\left(Cr_c + (t-DT)\right) + \Delta v_C(DT).\end{aligned} \tag{3.52}$$

The time t_2 at which value of $\Delta v_o(t)$ will become maximum during off time and is given by

$$t_2 = DT - Cr_c + \frac{(I_{mx}-I_o)}{\Delta i_L} D'T, \tag{3.53}$$

and at $t = t_2$, the voltage ripples obtained as

$$\Delta v_{rC}(t_2) = -\frac{\Delta i_L (Cr_C)^2}{CD'T} \tag{3.54}$$

$$\Delta v_C(t_2) = -\frac{(I_{mx}-I_o)^2 D'T}{2C\Delta i_L} + \frac{\Delta i_L (Cr_C)^2}{2CD'T} \tag{3.55}$$

$$\begin{aligned}\Delta v_{o,\max} &= \Delta v_o(t_2) \\ &= -\tfrac{\Delta i_L}{2CD'T}\left(\left((I_{mx}-I_o)\tfrac{D'T}{\Delta i_L}\right)^2 + (Cr_c)^2\right) + \Delta v_C(DT).\end{aligned} \tag{3.56}$$

Therefore, the total peak-to-peak voltage ripple will be

$$\Delta v_o = \Delta v_o(t_2) - \Delta v_o(t_1) \tag{3.57}$$

From (3.48) and (3.56) the total voltage ripple (peak-to-peak) will be

$$\begin{aligned}\Delta v_o &= \Delta v_o(t_2) - \Delta v_o(t_1) \\ &= -\tfrac{\Delta i_L f}{2CD'}\left(\left((I_{mx}-I_o)\tfrac{D'}{\Delta i_L f}\right)^2 + (C_f r_c)^2\right) - I_o r_c\end{aligned}. \tag{3.58}$$

If all parasitics are zero, then (3.58) becomes

$$\Delta v = -\frac{V_o DT}{RC} \tag{3.59}$$

The simplification details to get ideal formula (3.59) mentioned in *Appendix B*.

3.5.3 Effect of ESR on OVR

The voltage ripple contribution of ESR and capacitor in peak-peak OVR can be obtained as follows:
The OVR due to ESR is

$$|\Delta v_{rc}| = \Delta v_{rC}\left(t_2\right) - \Delta v_{rC}\left(t_1\right) \tag{3.60}$$

Substituting Equations (3.46) and (3.54) in (3.60), we get,

$$|\Delta v_{rc}| = \frac{\Delta i_L\left(Cr_c^2\right)}{CD'T} + I_o r_c, \tag{3.61}$$

Similarly, the OVR due to capacitor is

$$|\Delta v_C(t_2)| = \Delta v_C\left(t_2\right) - \Delta v_C\left(t_1\right) \tag{3.62}$$

Substituting Equations (3.47) and (3.55) in (3.62), we get,

$$|\Delta v_C(t_2)| = \frac{(I_{mx}-I_o)^2 D'T}{2C\Delta i_L} - \frac{\Delta i_L\left(Cr_c^2\right)}{2CD'T} \ . \tag{3.63}$$

The total OVR is given by Eq. (3.58). The OVR expressions (3.58), (3.61) and (3.63) versus ESR (r_c) is depicted in Figure 3.9(a). This plot reveals that, Δv_c decreases with an increase in ESR, at a slower rate than Δv_{rC} increases, thereby overall increment in Δv_o. Nevertheless, an impracticable things also occurs in a condition $r_c > r_{c,\max}$. Since, in this condition, the total ripple Δv_o becomes lesser than Δv_{rC}. Conclusively, it can be noted that the capacitor is no longer able to filter the ripples (or) keep OVR within the prescribed limit.

3.5.4 Output capacitor design

Let, Δv_{om} is the specified OVR for capacitor C design. Then, the procedure as follows:

$$|\Delta v_o| \leq |\Delta v_{om}| \, . \tag{3.64}$$

Substituting values from (3.58) ,

$$\frac{\Delta i_L f}{2C(1-D)}\left(\left((I_{mx}-I_o)\,\frac{(1-D)}{\Delta i_L f}\right)^2 + \left(Cr_c\right)^2\right) + I_o r_c \leq \Delta v_{om} \ . \tag{3.65}$$

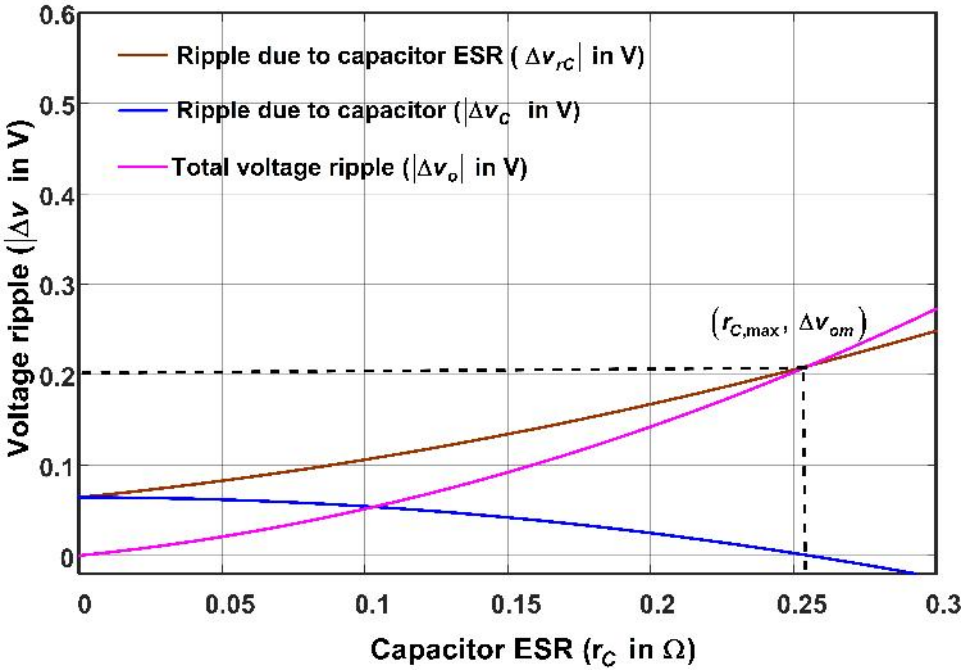


Figure 3.9: Different voltage ripple variation with ESR.

Above inequality can be simplified as,

$$C^2 r_c^2 - C\left(\frac{2(1-D)}{f}\left(\frac{\Delta v_{om} - I_o r_c}{\Delta i_L}\right)\right) + \left((I_{mx} - I_o)\frac{(1-D)}{\Delta i_L f}\right)^2 \leq 0 \tag{3.66}$$

This is quadratic constraint in C_f, which is solved to find the minimum value of output capacitor as

$$C_{mn} = \frac{(1-D)}{f r_c^2}\left[\frac{\frac{\Delta v_{om} - I_o r_c}{\Delta i_L} \pm \sqrt{\left(\frac{\Delta v_{om} - I_o r_c}{\Delta i_L}\right)^2 - \left(\frac{I_{mx} - I_o}{\Delta i_L}\right)^2 r_c^2}}{}\right]. \tag{3.67}$$

This expression gives the minimum value of filter capacitor C_f for specified OVR and ICR.

3.5.5 Maximum permissible ESR ($r_{C,max}$) and ICR effect

In previous section, it is emphasizing that the capacitor ESR takes significant part in OVR of buck-boost converter. More ripples at output means more ESR and degrading the voltage quality. Hence, the calculation of allowable ESR value ($r_{c,\max}$) for given Δv_{om} is important.

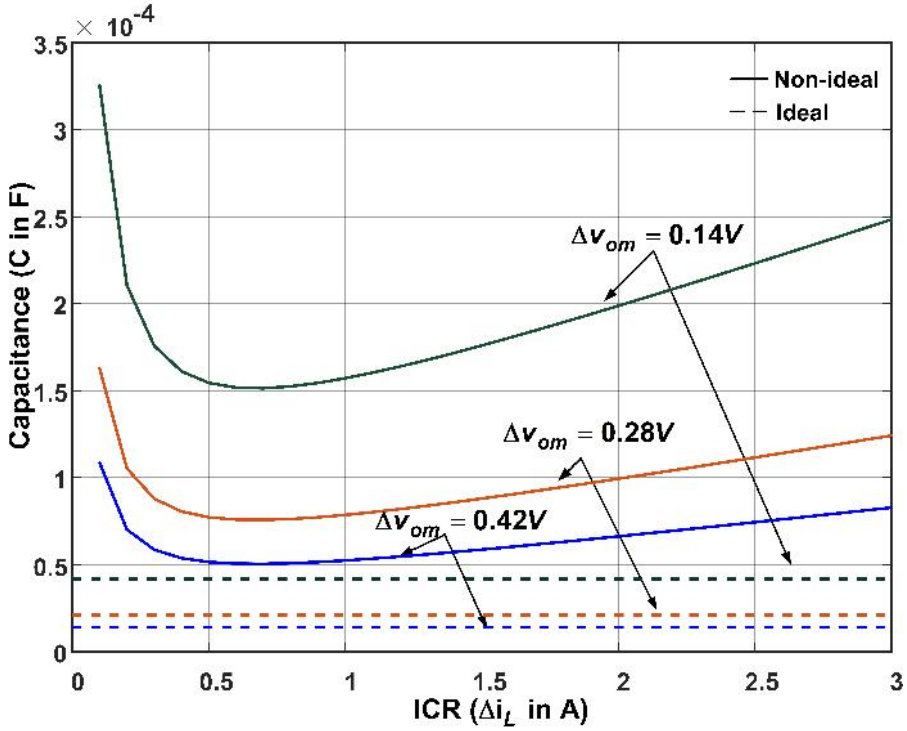


Figure 3.10: Inductance current ripple effect on capacitance value.

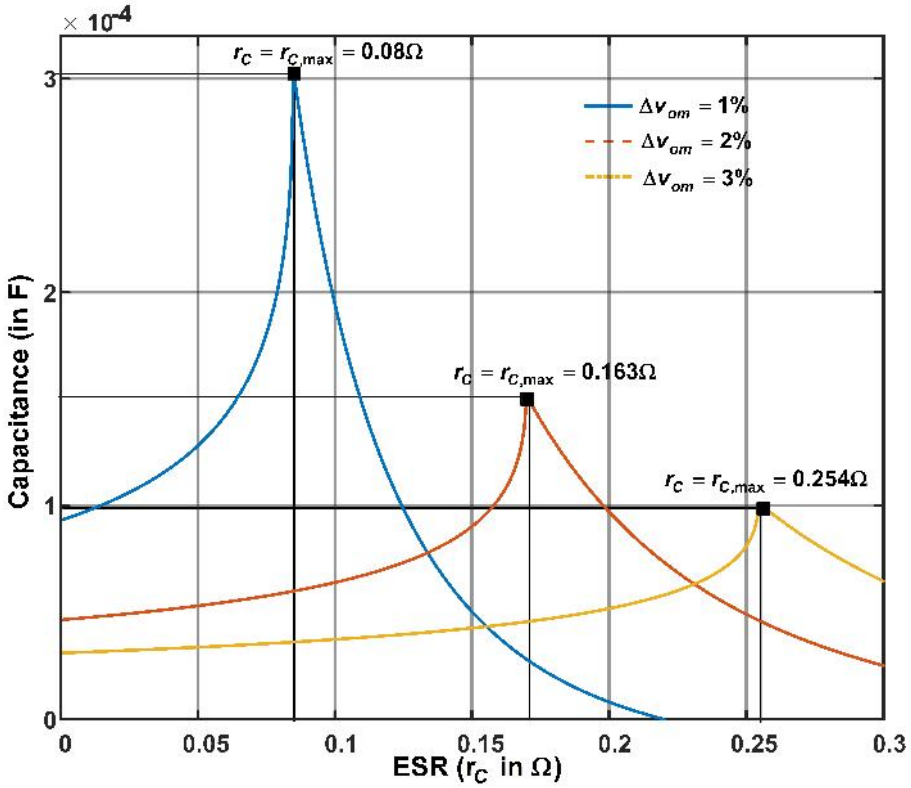


Figure 3.11: Capacitance variation with ESR.

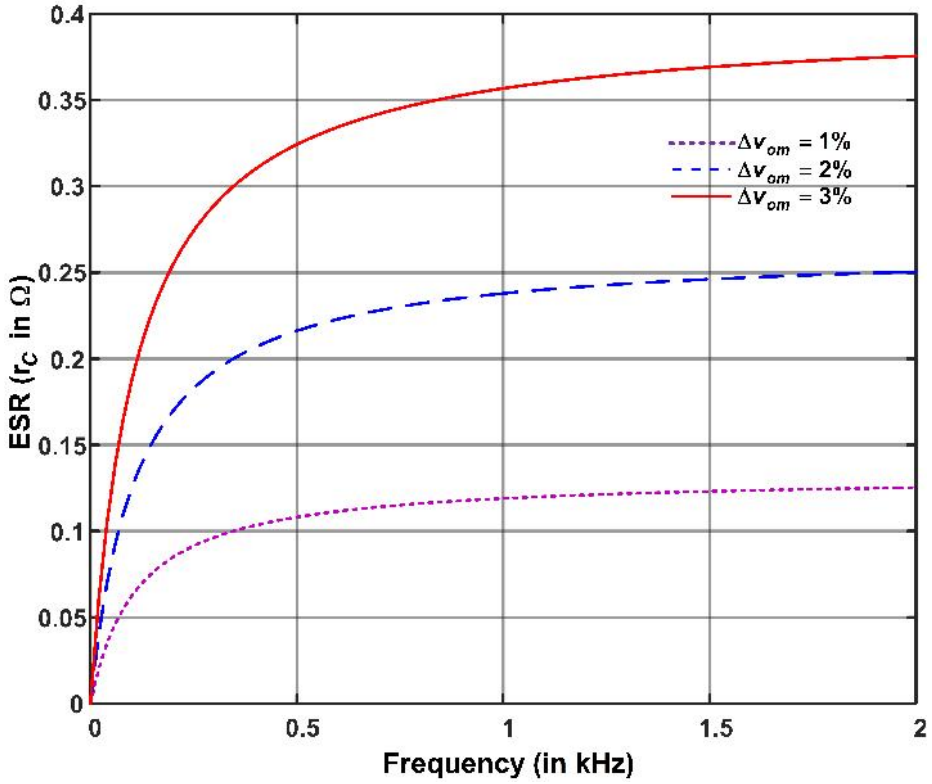


Figure 3.12: ESR vs frequency.

Equation (3.67), gives a real value (since C should be real value) only when parameters inside the square root are greater than or equal to zero, *i.e.,*

$$\left(\frac{\Delta v_{om} - I_o r_c}{\Delta i_L}\right)^2 - \left(\frac{I_{mx} - I_o}{\Delta i_L}\right)^2 r_c^2 \geq 0. \tag{3.68}$$

On simplification,

$$r_c \leq \frac{\Delta v_{om}}{I_{mx}}. \tag{3.69}$$

Hence, $r_{c,\max}$ for prescribed Δv_{om} and Δi_L can be determined as

$$r_{c,\max} = \frac{\Delta v_{om}}{I_{mx}}. \tag{3.70}$$

This analysis can be extended with simulation and practical experiments in further sections. The elaboration of this analysis done in such away that the effect of ESR on OVR in different conditions like $r_C > r_{C,\max}$ and $r_C < r_{C,\max}$.

Further, to obtain the capacitor value in worst case, substitute (3.70) into (3.67),

we get,

$$C_{mn} = \frac{D' I_{mx} \left(I_{mx} - I_o \right)}{\Delta i_L \Delta v_{om} f}. \tag{3.71}$$

Generally, capacitor ideal design (3.59) reveals that there is no effect of ICR, but from (3.71), it is clear that ICR also effects the capacitance design. This phenomenon can be observed from Figure 3.10.

3.6 Experimental Results and Discussion

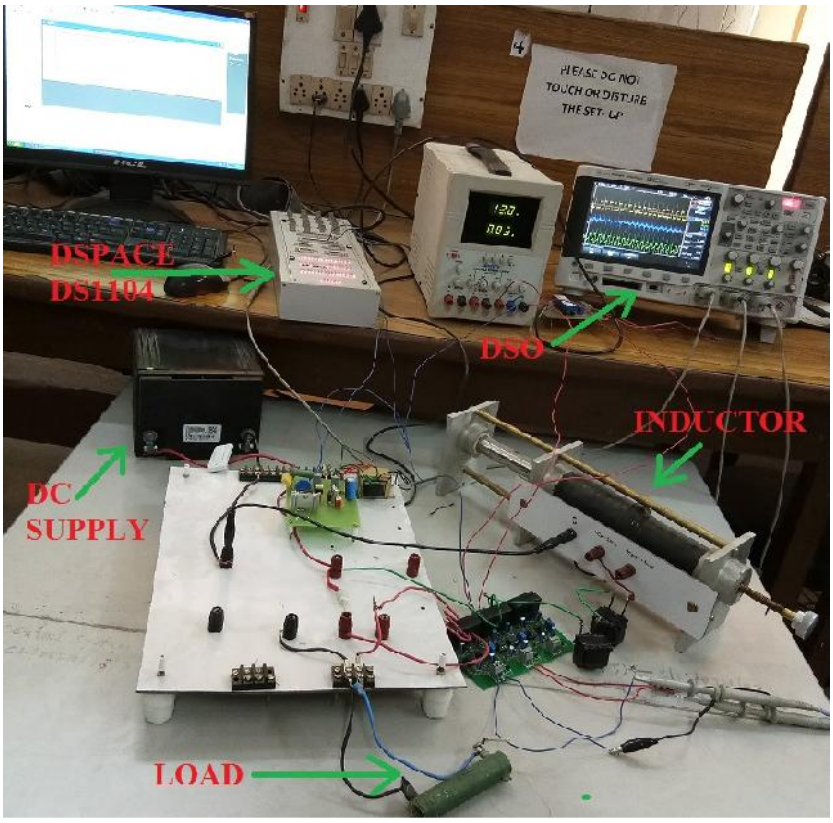


Figure 3.13: Experimental set up of DC-DC buck-boost converter.

In previous sections analytical findings are validated by simulations and experimental results. The simulations are carried out in MATLAB/Simulink software package whereas for the experimental results, a hardware prototype is developed as shown in Figure 3.13.According to the availability, MOSFET IRFP460 and diode MUR1560 are chosen as semiconductor switching devices. The ferrite core inductors and electrolytic capacitors are used as energy storage elements. The values of

various parameters used for simulation and prototype design are given in Table 3.1.

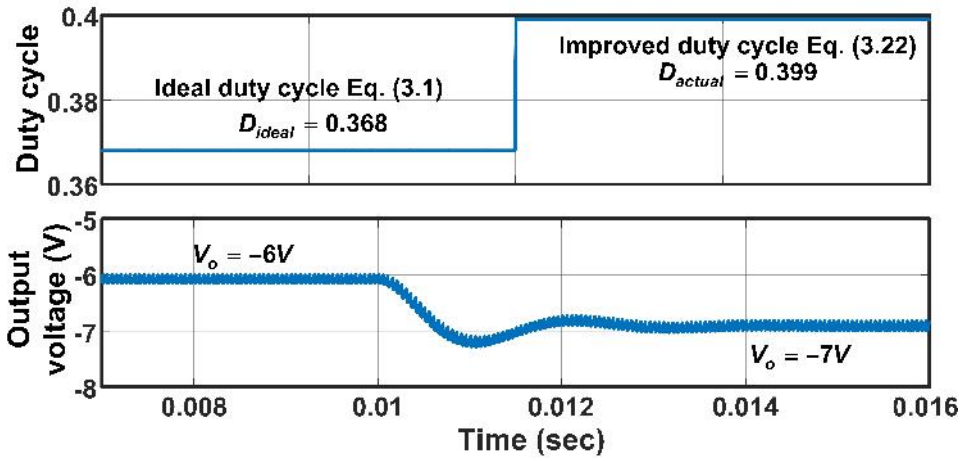


Figure 3.14: Simulation result of output voltage with ideal and modified duty cycle expressions.

Beginning with steady state analysis, from (3.22), the improved expression for duty cycle is calculated as 0.399, where as through ideal calculation (3.1), 0.368 are obtained to get a output of -7V. This has been verified through simulations as shown in Figure 3.14. These simulations are validated through experiment results as shown in Figure 3.15. Here, with ideally calculated value, less output value obtained (*i.e.,*-6V) than expected (*i.e.,*-7V), where as with the proposed duty cycle relation expected value obtained. This increase in duty cycle value is to compensate the voltage drop across parasitics.

Here, the maximum permissible duty cycle and maximum achievable voltage with the converter are also have been verified by simulation and practically. The maximum permissible duty cycle of buck-boost converter in presence of parasitics (as per Table 3.1) is $D_{max} = 0.8526$. The corresponding simulation and experimental results have been shown in Figure 3.16 and Figure 3.17, respectively. From this figure, it is very clear that the converter operates in unstable region when $D > D_{max}$ and reaches to zero at $D = 1$. Alongside, the V_{omax} for this converter is -28.7V. Therefore, this information is crucial for engineers to operate converter in a closed-loop.

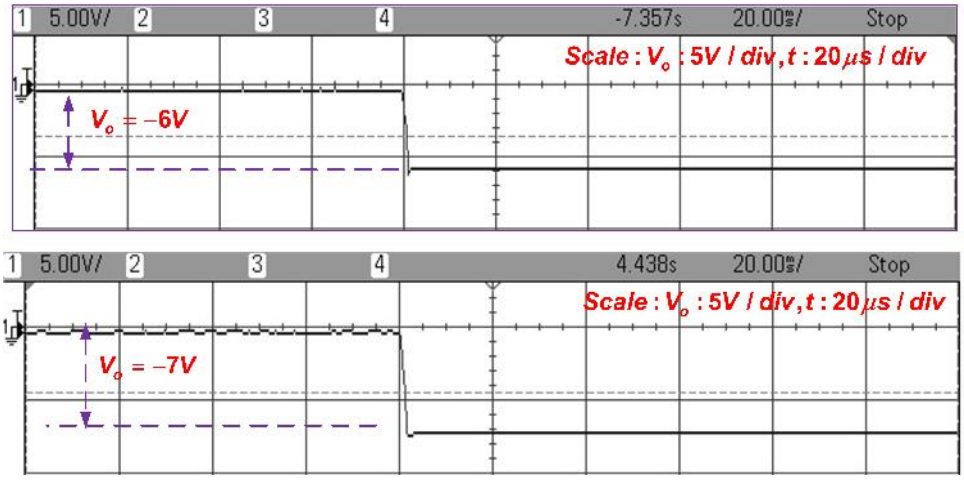


Figure 3.15: Experimental result of output voltage with ideal and modified duty cycle expressions.

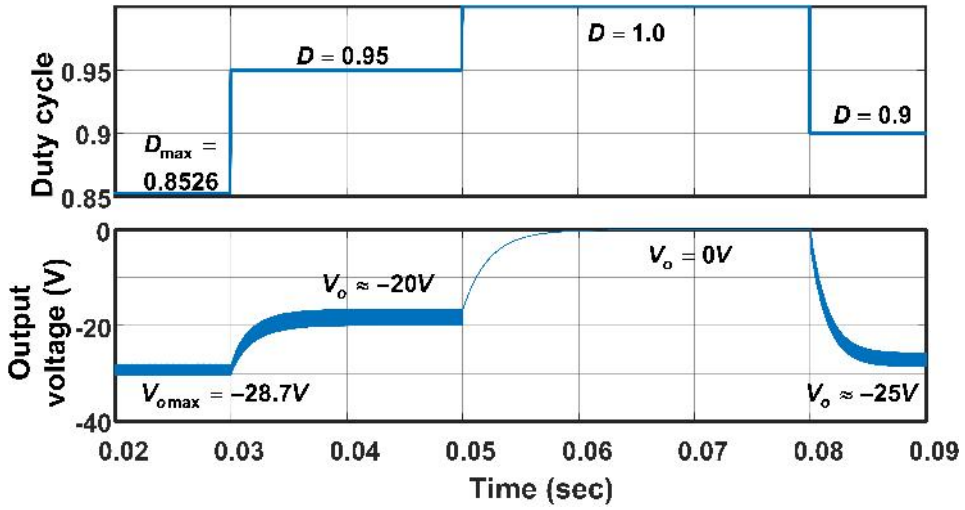


Figure 3.16: Simulation result of output voltage at different duty cycle $D > D_{max}$.

Now, the observations made on steady state analysis for closed-loop operation are tested. Suppose, reference voltage has been set for $V_{oref} = -30$V and then started the operation. The output will reach to zero, which is clearly observed from simulation and experimental results as shown in Figure 3.18. This is because the reference is more than the maximum achievable voltage of the converter.

Next, analysis is also carried out for changes in input voltage, when converter is operating in a closed-loop. Suppose, the step change in input voltage value is

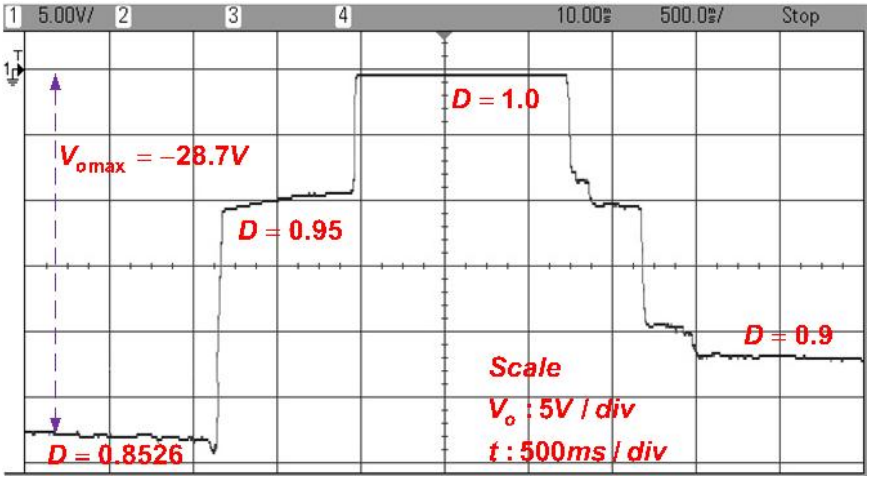
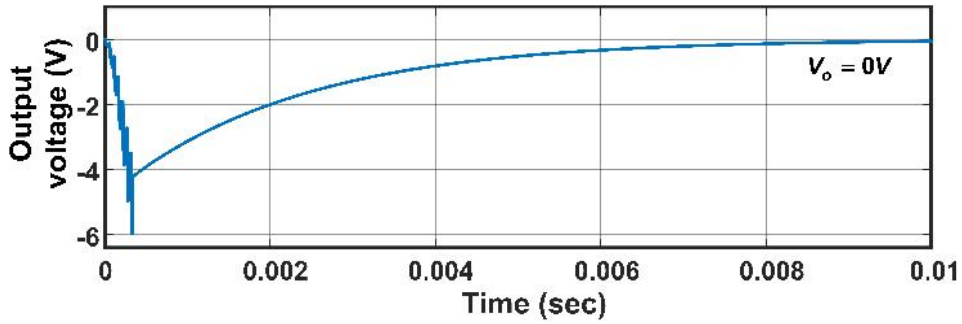
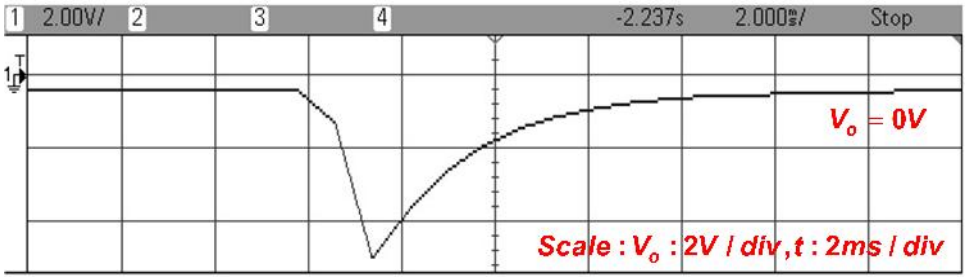


Figure 3.17: Experimental result of output voltage at different duty cycle $D > D_{max}$.



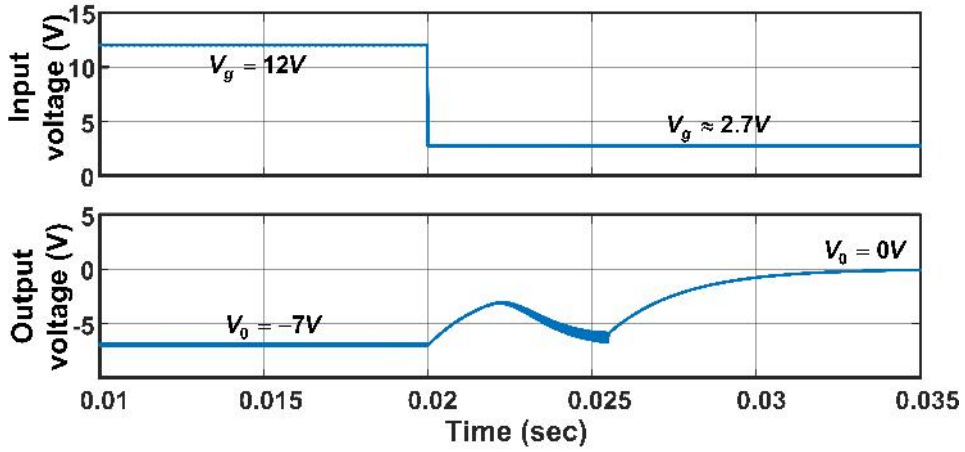
(a)



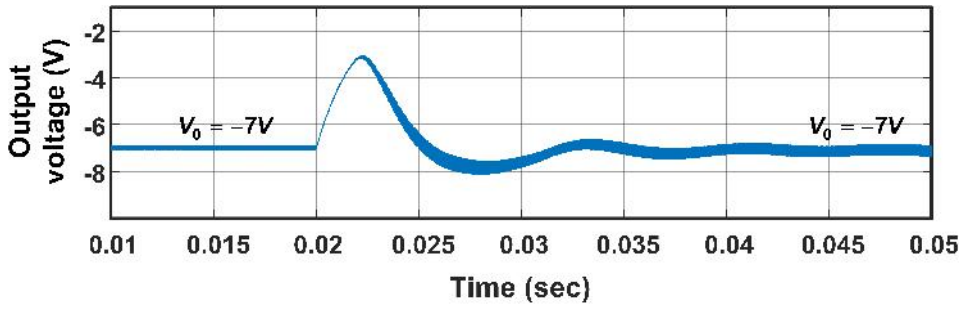
(b)

Figure 3.18: Output voltage in closed-loop operation when $V_{ref} > V_{omax}$ (a)Simulation (b)Experimental.

very large (*i.e.,* $V_g = 12$V to 2.6V), then the output will become zero as shown in Figure 3.19 (a) and corresponding experimental results is shown in Figure 3.19 (b).



(a)

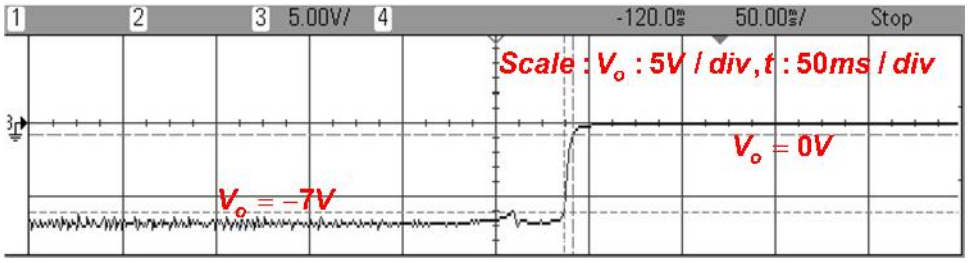


(b)

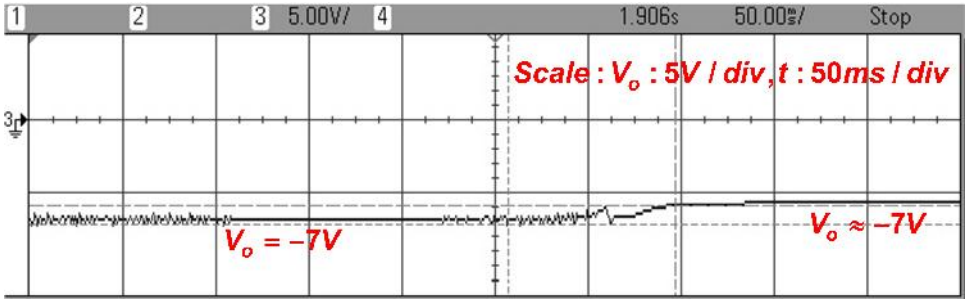
Figure 3.19: Simulation result of output voltage in closed-loop operation when sudden input voltage change ($V_g < V_{gmin}$) (a)without D_{lim} (b)with D_{lim}.

Since, the duty cycle corresponds to the sudden step change is more than D_{max} (sometimes may be $D = 1$). For the same case, now a limiter is added at the controller output and then the same operation has been carried out. Now, the output has not become zero and system is stable, which is shown in Figure 3.19(b) and corresponding experimental results is shown in Figure 3.19 (b). Since, the controller output is limited to D_{max}, which is calculated from (3.25).

In another case, let the converter is operating in a closed-loop. Suppose, the step change in reference voltage value is very large, then the output will become zero as shown in Figure 3.21 (a) and corresponding experimental results is shown in Figure 3.22 (a). Since, the duty cycle corresponds to the sudden step change is more than



(a)



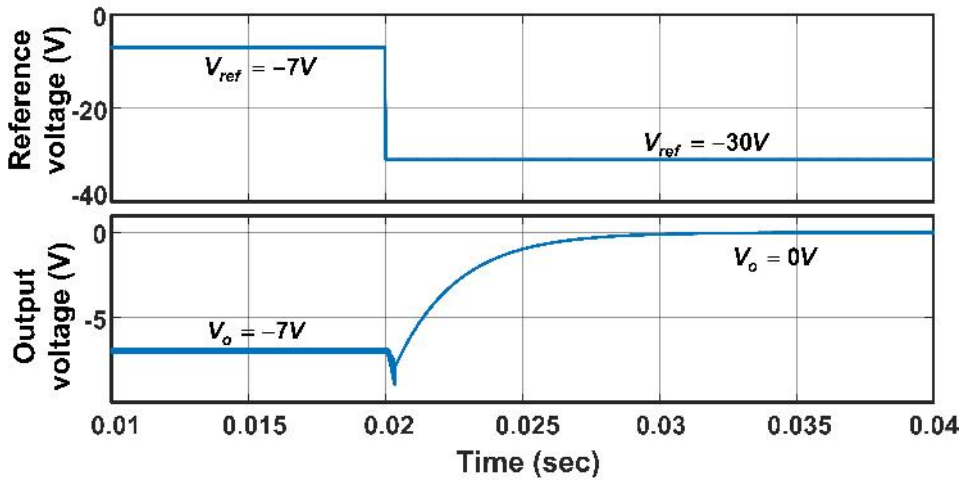
(b)

Figure 3.20: Experimental result of output voltage in closed-loop operation when sudden input voltage change ($V_g < V_{gmin}$) (a)without D_{lim} (b)with D_{lim}.

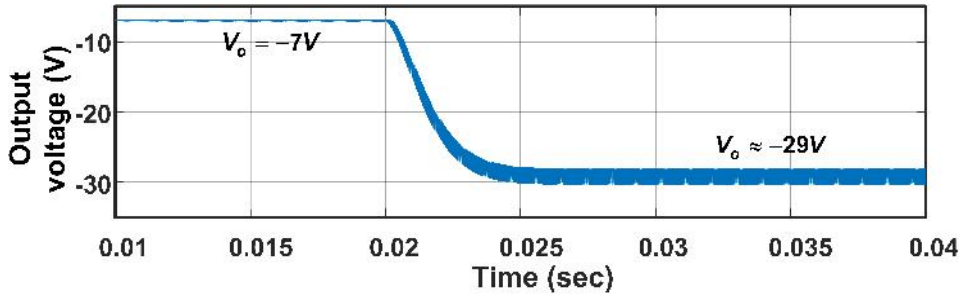
D_{max} (sometimes may be $D = 1$). For the same case, now a limiter is added at the controller output and then the same operation has been carried out. Now, the output has not become zero and system is stable, which is shown in Figure 3.21(b) and corresponding experimental results is shown in Figure 3.22 (b). Since, the controller output is limited to D_{max}, which is calculated from (3.25).

Further, the modified relations for inductor and capacitor are verified. The ideal calculated value of inductor L is 360 μH, whereas through modified expression (3.36) is 392.3 μH. Hence, the inductance required is more in existence of parasitics. The minimum required capacitance C obtained as 100μF from Eq. (3.71). Figure 3.23 and Figure 3.24, depict the simulation and experimental results of inductor and capacitor current wave forms. The steady-state I_L value is 0.549A and Δi_L is 0.59A. In Figure 3.24, the measured current is output of a current sensor having gain as 20 and for capacitor current sensor gain is 2.5.

Now, coming to the ripple analysis, from Eq. (3.70), the $r_{c,max}$ is obtained as 0.256Ω



(a)



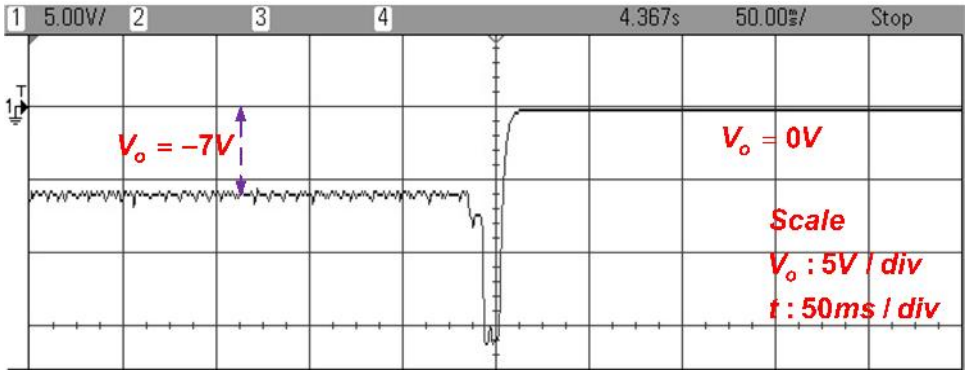
(b)

Figure 3.21: Simulation result of output voltage in closed-loop operation when sudden reference voltage change (a)without D_{lim} (b)with D_{lim}.

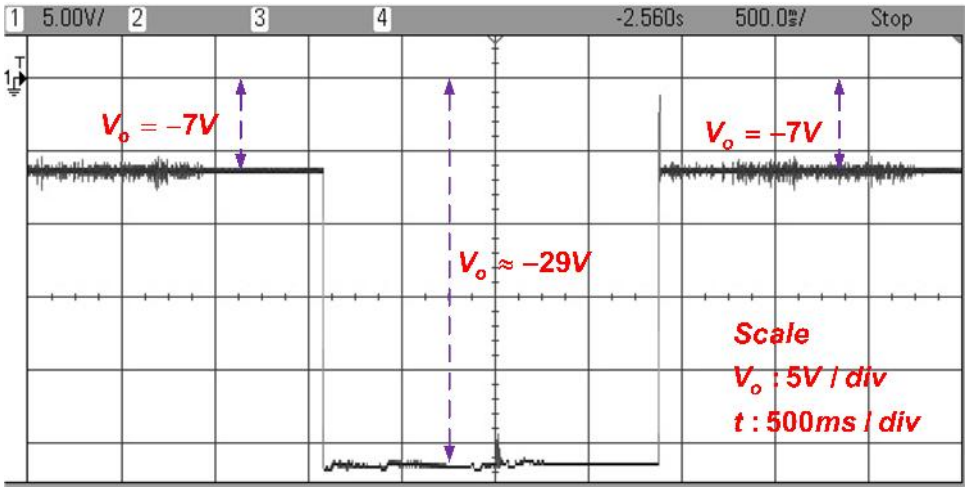
to keep the output voltage ripples within 3% of output voltage. The effect of r_c on OVR is observed and the necessity of maximum permissible ESR ($r_{c,max}$) is highlighted. Two different cases ($r_c < r_{c,\max}$ and $r_c > r_{c,\max}$) are taken for demonstration as discussed below-

***Case 1 ($r_c = 0$)*:** In this case, the ESR of output capacitor (r_c) is 0Ω which is an ideal case. However, this is not possible in practical. The ripple contribution is only because of capacitor itself. The simulated result of output voltage ripples are shown in Figure 3.25(a). These results show that the peak-peak magnitude of output voltage ripple is less than 0.04 V.

***Case 2 ($r_c = 0.2 < r_{c,\max}$)*:** In this case, the ESR of output capacitor (r_c) is 0.2Ω



(a)



(b)

Figure 3.22: Experimental result of output voltage in closed-loop operation when sudden reference voltage change (a)without D_{lim} (b)with D_{lim}.

which is less than the value of maximum permissible ESR. The ripple contribution is not only because of capacitor itself and ESR also. The simulated and experimental wave forms of output voltage ripples are shown in Figure 3.25(b) and Figure 3.26(a), respectively. These results show that the magnitude of output voltage ripple is about 200 mV, which is within desired limit (210 mV).

Case 3 ($r_c = r_{c,\max} = 0.256$***)*:** In this case, the ESR of output capacitor (r_c) is 0.256Ω which is equal to the value of maximum permissible ESR. The ripple contribution due to ESR increases, resulting to increases OVR. The simulated result of output voltage ripples are shown in Figure 3.25(c). These results show that the magnitude of output

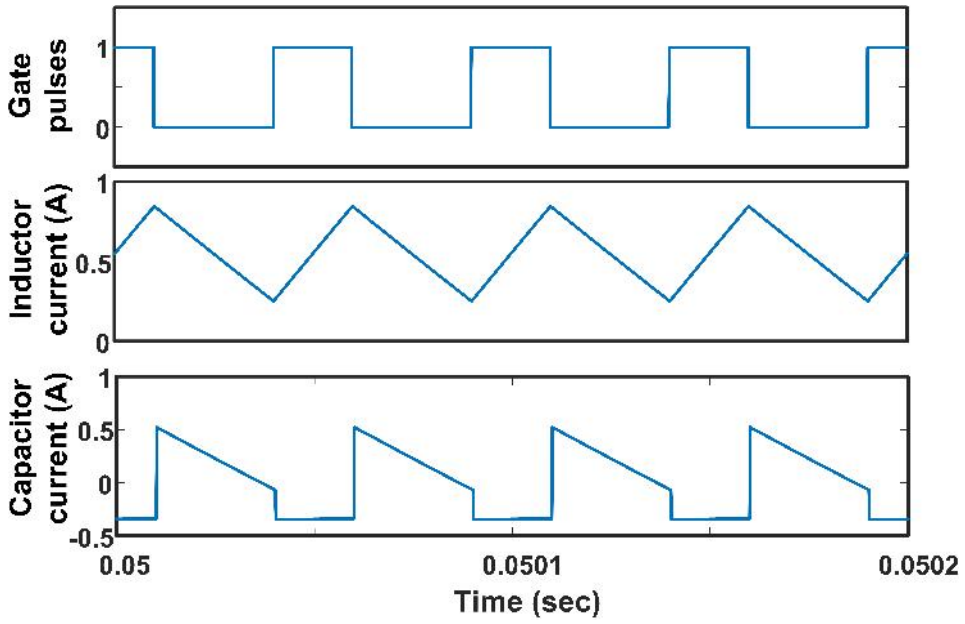


Figure 3.23: Simulation result of Capacitor and inductor current waveforms of converter in open loop operation at duty cycle $D = 0.4$.

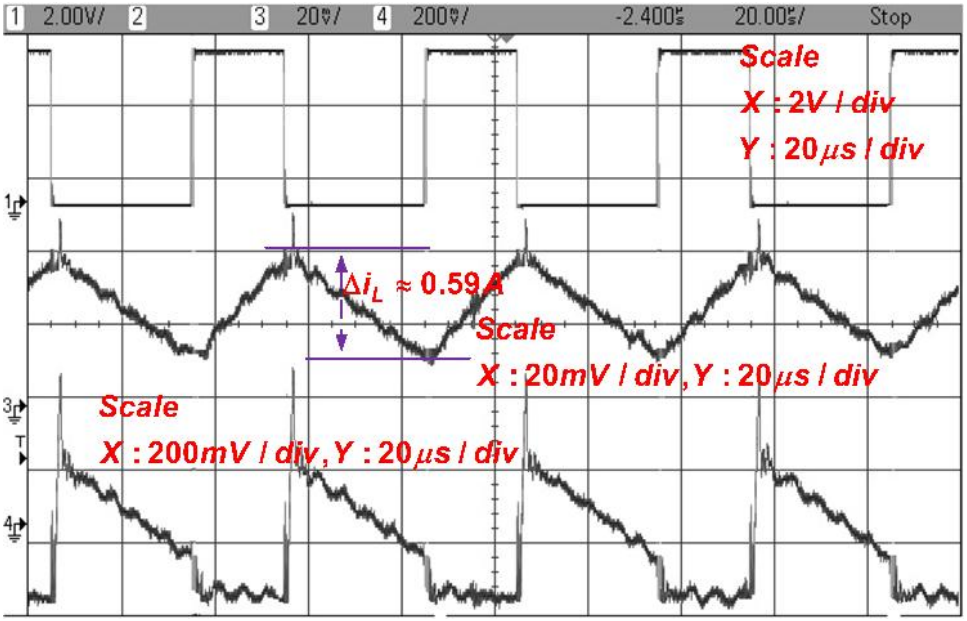
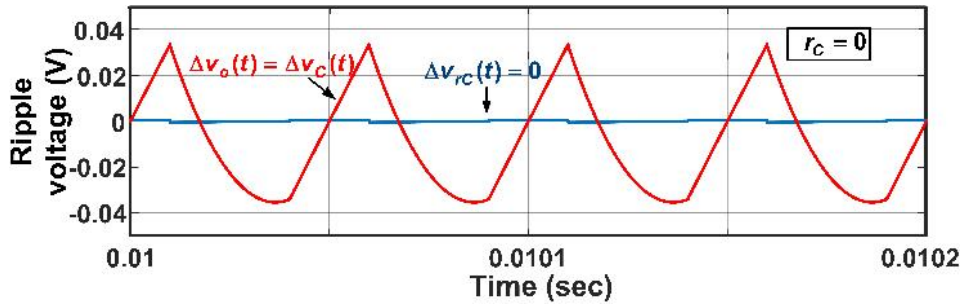


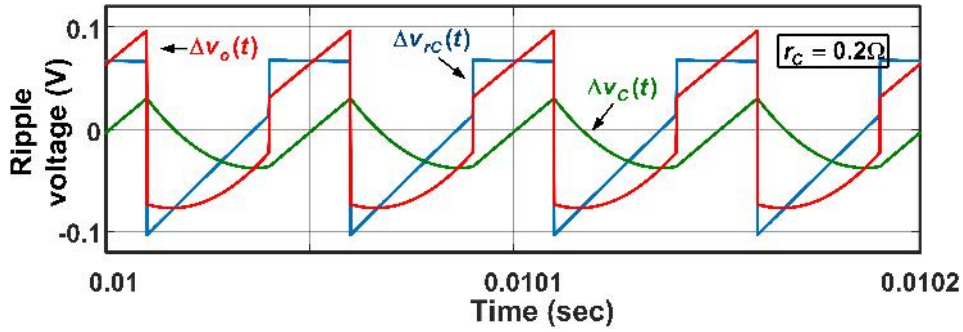
Figure 3.24: Experimental result of Capacitor and inductor current waveforms of converter in open loop operation at duty cycle $D = 0.4$.

voltage ripple is about 210 mV, which is within desired limit (210 mV).

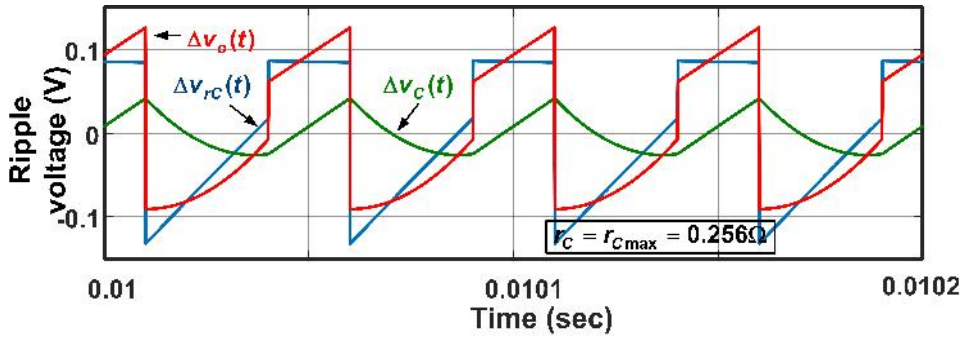
***Case 4 ($r_c = 0.3 > r_{c,\max}$)*:** This case evaluates the output voltage ripples if ca-



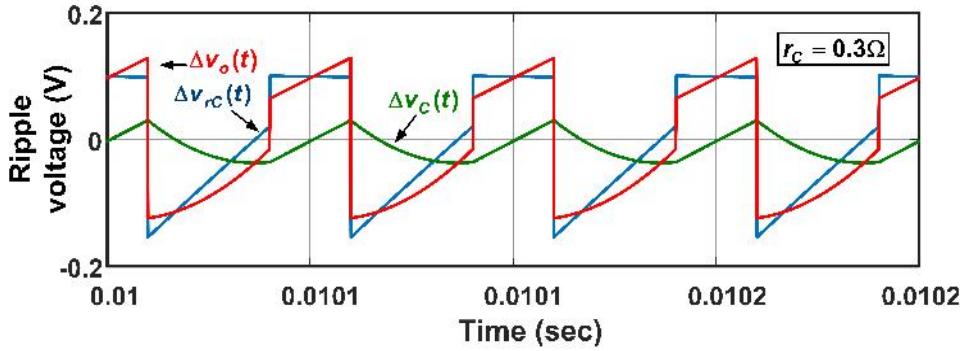
(a)



(b)

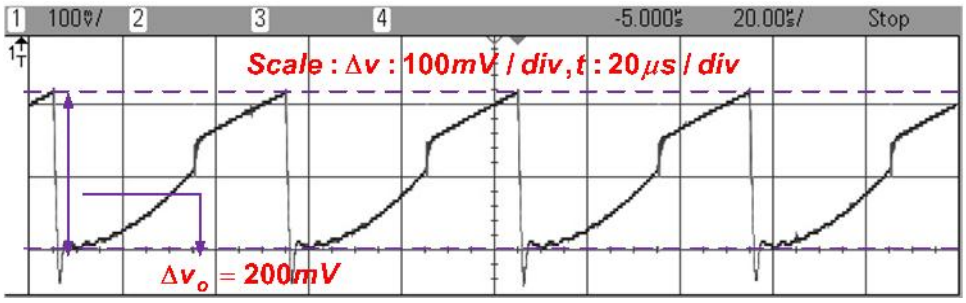


(c)

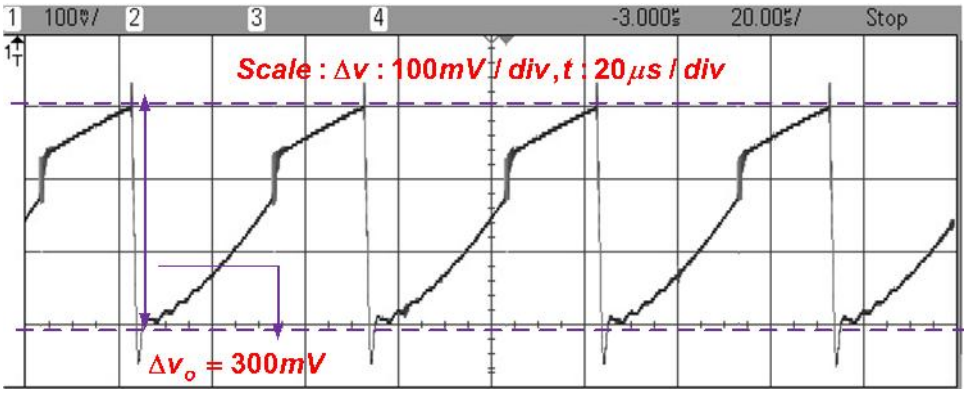


(d)

Figure 3.25: Simulation results of output voltage ripples with (a)ESR (r_c) =0Ω (b)ESR (r_c) =0.2Ω (c)ESR (r_c)= 0.256Ω (d)ESR (r_c) =0.3Ω.



(a)



(b)

Figure 3.26: Experimental result of output voltage ripples with (a)ESR (r_c) =0.2Ω (b)ESR (r_c) =0.3Ω.

pacitor ESR (r_c) is greater than the maximum permissible ESR. Therefore, the value of r_c is kept 0.3Ω in simulation as well as in experiment. As shown in Figure 3.25(d) and Figure 3.26(b), respectively, the output voltage ripple is obtained nearly 300 mV, which is beyond the desired limit (210 mV). Therefore, this value of output capacitor ESR is not suitable to have output voltage ripples within 3% range as desired.

3.7 Experimental Validation of Complete Non-ideal Small Signal Model of Buck-Boost Converter

The comparative performance of complete non-ideal buck-boost converter with other the semi non-ideal buck-boost converter models (*i.e.,* transfer function models with less parasitics) studied experimentally. For this purpose, model based controller such as IMC (Internal Model Control)-PID [82], designed for all models. It is observ-

able that, the transfer functions will differ each other and also PID values. Figure 3.27, demonstrates the closed-loop performance of the all models. Figures 3.28(a)-(d), shows the analogous experimental results.

It is noticeable from simulations that the converter performance has improved by controller designed by respective models. Nevertheless, all parasitics will effect the practical system. The implementation of respective controllers will not produce the similar results as in simulations. Besides, this performance is compared through tabular form as shown in Table 3.3 by considering various specifications. This comparison signifies that, the simulation of complete non-ideal model is almost similar to the experimental values. This is due to the PID parameters are evaluated by considering the complete non-ideal small-signal model of buck-boost converter, which is almost same as the practical system.

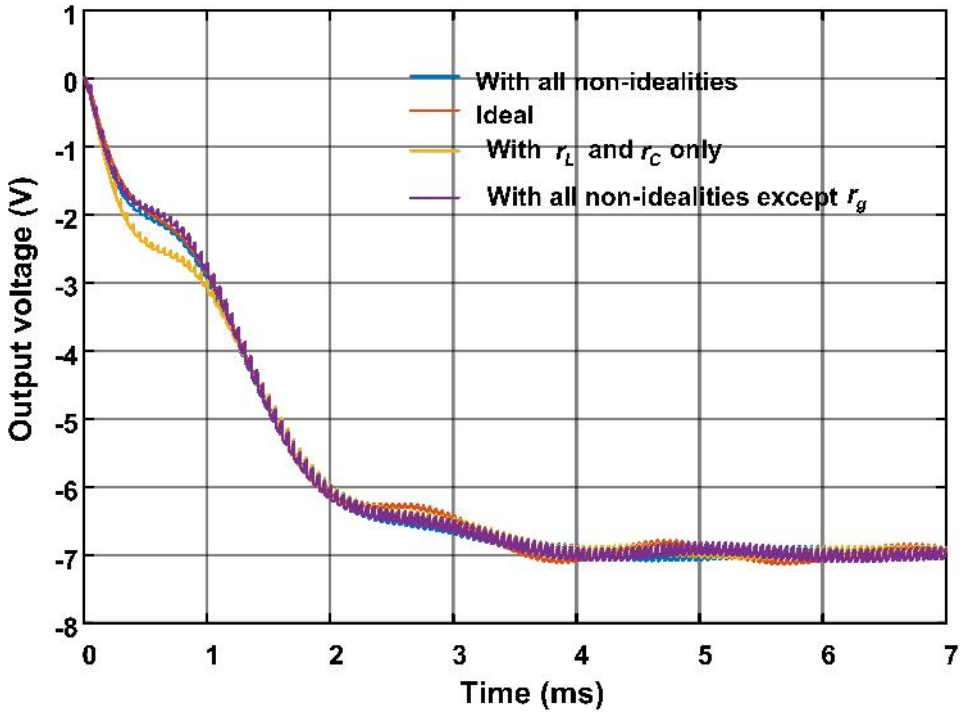
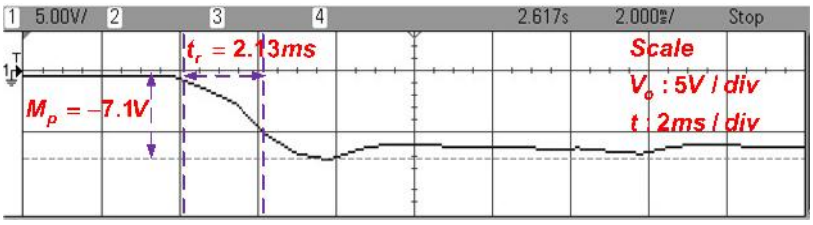
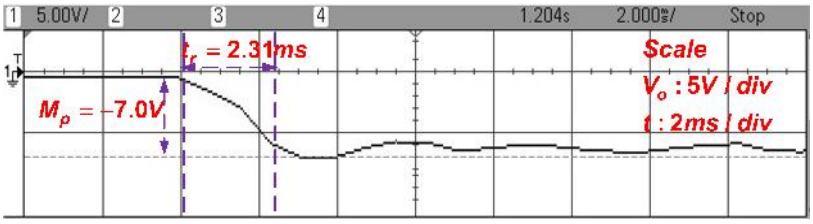


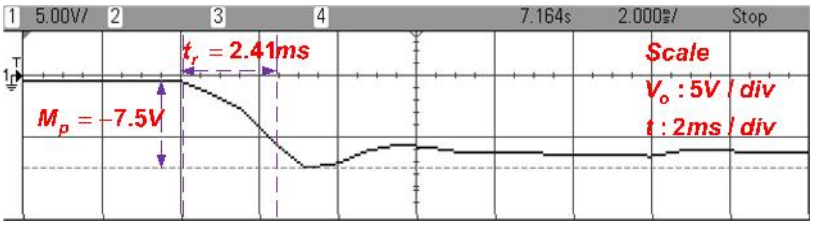
Figure 3.27: Simulation comparison of performance of different converters.



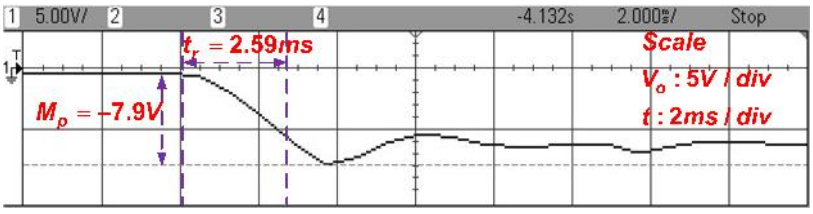
(a)



(b)



(c)



(d)

Figure 3.28: Experimental results of buck-boost converter for PID parameters calculated from (a) complete non-ideal model (b) model with all non-idealities except r_g (c) model with r_L, r_C (d) ideal model.

Table 3.3: Performance of non-ideal buck-boost converter in comparison with other converter models with less non-idealities

	Non-ideal model of buck-boost converter (presented in paper)			Buck-boost converter with r_L,r_c, r_{on} and V_{fd} [173]			Buck-boost converter with r_L and r_c [171]			Ideal buck-boost converter [172]		
	Sim	Exp	**Err**	Sim	Exp	Err	Sim	Exp	Err	Sim	Exp	Err
t_r (in ms)	2.1	2.13	**1.0%**	2.1	2.31	10%	2.1	2.41	14.7%	2.1	2.59	23.3%
M_p (in V)	7.0	7.1	**1.0%**	7.0	7.0	0.0%	7.0	7.5	7.1%	7.0	7.9	12.8%
V_{omax} (in V)	28.7	28.2	**1.7%**	38.2	28.2	26%	41.3	28.2	31.7%	-	28.2	-
D_{max}	0.8526	0.8526	**0.0%**	0.88	0.8526	3.2%	0.89	0.8526	4.3%	1.0	0.8526	17.2%

Sim-Simulation, Exp-Experimental, Err- Relative error, t_r-Rise time, M_p-Peak value, V_{omax}-Maximum obtainable voltage, D_{max}-Maximum duty cycle

3.8 Mathematical Modeling

Buck-boost converter with non-idealities to be modelled is shown in Figure 3.29. The state space average approach is used for modeling, which is explained in *Appendix A*. The most important point to be observed is that the modeling done by considering the all non-idealities or parasitics. As depicted in Figure 3.29, which is same as Figure 3.1(a), but a current source ($i_z(t)$) is connected to the output terminals of the converter, which models the loading effect of the load subsystem (besides the resistive load) being fed from this converter. As explained in previous sections, modeling

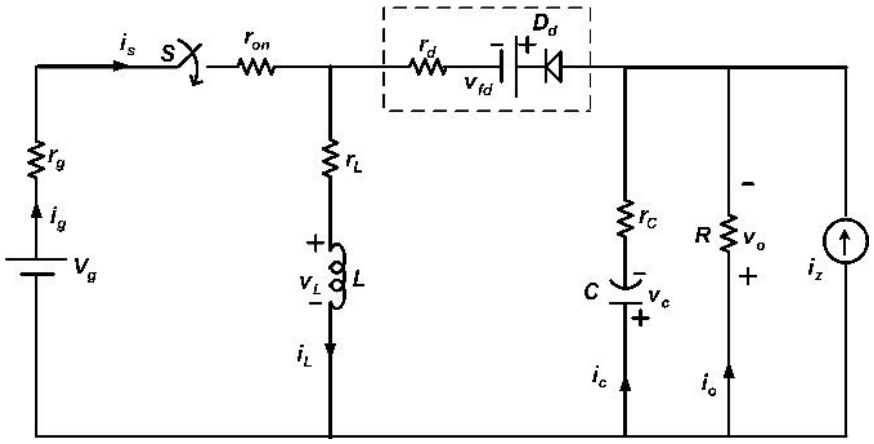


Figure 3.29: Non-ideal buck-boost converter model.

of non-ideal DC-DC buck-boost converter is carried out in CCM. In this, as converter consists of only one active switch (S) that can be ON or OFF and thus has only two modes of operation. So, we need to write state equations for both modes of operation. For this, inductor current and capacitor voltage as considered as states of the system. The modeling as follows:

Step 1: Writing the state equations for two modes of operation

During ON time $(0 < t < DT)$

When switch is ON (S), the equations governing with inductor current (i_L), capacitor voltage (v_c) and output voltage (v_o) are obtained as:

$$\begin{aligned} v_L(t) = L\frac{di_L(t)}{dt} &= -\left[r_g + r_{on} + r_L\right] i_L(t) + v_g(t) \\ \Rightarrow \dot{i}_L(t) &= -\frac{r_g + r_{on} + r_L}{L} i_L(t) + \frac{1}{L} v_g(t) \end{aligned} \tag{3.72}$$

$$i_c(t) = C\frac{dv_c(t)}{dt} = -\frac{v_o(t)}{R} - i_z(t) \tag{3.73}$$

$$v_o(t) = v_c(t) + r_c i_c(t) \tag{3.74}$$

Substituting (3.73) in (3.74), we get,

$$\begin{aligned} v_o(t) &= v_C(t) + r_C\left(-\tfrac{v_o(t)}{R} - i_z(t)\right) \\ \Rightarrow v_o(t) &= \tfrac{R}{R+r_c}v_c(t) - \tfrac{Rr_c}{R+r_c}i_z(t) \end{aligned} \tag{3.75}$$

Substituting (3.75) in (3.73), we get,

$$\dot{v}_c(t) = -\frac{1}{C(R+r_c)}v_c(t) - \frac{1}{C(R+r_c)}i_z(t) \tag{3.76}$$

$$i_g(t) = i_L(t) \tag{3.77}$$

Equations (3.72), (3.76), (3.75) and (3.77) can be represented in state space form as

$$\underset{\tilde{}}{\dot{x}} \qquad\qquad A_1 \qquad\qquad B_1 \qquad\qquad J_1$$

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} -\frac{r_g+r_{on}+r_L}{L} & 0 \\ 0 & -\frac{1}{C(R+r_c)} \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{R}{C(R+r_c)} \end{bmatrix}\begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix}\begin{bmatrix} V_{fd} \end{bmatrix} \tag{3.78}$$

$$\underset{\tilde{}}{y} \qquad\qquad C_1 \qquad\qquad E_1 \qquad\qquad F_1$$

$$\begin{bmatrix} v_o(t) \\ i_g(t) \end{bmatrix} = \begin{bmatrix} 0 & \frac{R}{R+r_c} \\ 1 & 0 \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 0 & -\frac{Rr_c}{R+r_c} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix}\begin{bmatrix} V_{fd} \end{bmatrix} \tag{3.79}$$

During OFF time $(DT < t < T)$

When switch is OFF (S), the equations governing with inductor current (i_L), capacitor voltage (v_c) and output voltage (v_o) are obtained as:

$$v_L(t) = L\tfrac{di_L(t)}{dt} = -\left(r_L + r_d\right)i_L(t) - v_o(t) - V_{fd} \tag{3.80}$$

$$i_c(t) = C\frac{dv_c(t)}{dt} = i_L(t) - \frac{v_o(t)}{R} - i_z(t) \tag{3.81}$$

$$v_o(t) = v_c(t) + r_c i_c(t) \tag{3.82}$$

$$i_g(t) = 0 \tag{3.83}$$

Substituting (3.81) in (3.82), we get,

$$\begin{aligned} & v_o(t) = v_c(t) + r_c \left(i_L(t) - \tfrac{v_o(t)}{R} - i_z(t) \right) \\ & \Rightarrow v_o(t) = \left(\tfrac{R}{R+r_c} \right) v_c(t) + \left(\tfrac{Rr_c}{R+r_c} \right) i_L(t) - \left(\tfrac{Rr_c}{R+r_c} \right) i_z(t) \end{aligned} \tag{3.84}$$

Substituting (3.84) in (3.81), we get,

$$\dot{v}_c(t) = \frac{R}{C(R+r_c)} i_L(t) - \frac{1}{C(R+r_c)} v_c(t) - \frac{R}{C(R+r_c)} i_z(t) \tag{3.85}$$

Substituting (3.84) in (3.80), we get,

$$\dot{i}_L(t) = -\tfrac{(r_d+r_L)(R+r_c)+Rr_c}{L(R+r_c)} i_L(t) - \tfrac{R}{L(R+r_c)} v_c(t) + \tfrac{Rr_c}{L(R+r_c)} i_z(t) - \tfrac{V_{fd}}{L} \tag{3.86}$$

Equations (3.86), (3.85), (3.84) and (3.83) can be represented in state space form as

$\tilde{\dot{x}}$ A_2 B_2

$$\frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} -\frac{(r_d+r_L)(R+r_c)+Rr_c}{L(R+r_c)} & -\frac{R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & -\frac{1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 0 & \frac{Rr_c}{L(R+r_c)} \\ 0 & -\frac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix}$$

J_2

$$+ \begin{bmatrix} -\frac{1}{L} \\ 0 \end{bmatrix} \begin{bmatrix} V_{fd} \end{bmatrix} \tag{3.87}$$

$\tilde{y}$ C_2 E_2 F_2

$$\begin{bmatrix} v_o(t) \\ i_g(t) \end{bmatrix} = \begin{bmatrix} \frac{Rr_c}{R+r_c} & \frac{R}{R+r_c} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 0 & -\frac{Rr_c}{R+r_c} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \begin{bmatrix} V_{fd} \end{bmatrix} \tag{3.88}$$

Step 2: Obtain the large signal state-space averaged model

The large signal averaged state-space model of non-ideal DC-DC buck-boost converter can be obtained as

$$\underset{\tilde{\cdot}}{\dot{\bar{x}}} \qquad\qquad\qquad\qquad A$$

$$\frac{d}{dt}\begin{bmatrix}\bar{i}_L(t)\\ \bar{v}_C(t)\end{bmatrix} = \begin{bmatrix} -\frac{\left[\, r_L + D\left(r_g + r_{on}\right) + (1-D)r_d \,\right]^{(R+r_c)+(1-D)(Rr_c)}}{L} & -\frac{(1-D)R}{L(R+r_c)} \\ \frac{(1-D)R}{C(R+r_c)} & -\frac{1}{C(R+r_c)} \end{bmatrix}\begin{bmatrix}\bar{i}_L(t)\\ \bar{v}_C(t)\end{bmatrix}$$

$$B \qquad\qquad J$$

$$+\begin{bmatrix}\frac{D}{L} & \frac{(1-D)Rr_c}{L(R+r_c)}\\ 0 & -\frac{R}{C(R+r_c)}\end{bmatrix}\begin{bmatrix}\bar{v}_g(t)\\ \bar{i}_z(t)\end{bmatrix} + \begin{bmatrix}-\left(\frac{1-D}{L}\right)\\ 0\end{bmatrix}\begin{bmatrix}V_{fd}\end{bmatrix} \tag{3.89}$$

$$\underset{\tilde{}}{\bar{y}} \qquad\qquad C \qquad\qquad\qquad E \qquad\qquad F$$

$$\begin{bmatrix}\bar{v}_o(t)\\ \bar{i}_g(t)\end{bmatrix} = \begin{bmatrix}\frac{(1-D)Rr_c}{R+r_c} & \frac{R}{R+r_c}\\ D & 0\end{bmatrix}\begin{bmatrix}\bar{i}_L(t)\\ \bar{v}_C(t)\end{bmatrix} + \begin{bmatrix}0 & -\frac{Rr_c}{R+r_c}\\ 0 & 0\end{bmatrix}\begin{bmatrix}\bar{v}_g(t)\\ \bar{i}_z(t)\end{bmatrix} + \begin{bmatrix}0\\ 0\end{bmatrix}\begin{bmatrix}V_{fd}\end{bmatrix} \tag{3.90}$$

Where,

$$\begin{aligned} &A = DA_1 + (1-D)A_2, B = DB_1 + (1-D)B_2 \\ &C = DC_1 + (1-D)C_2, E = DE_1 + (1-D)E_2 \\ &J = DJ_1 + (1-D)J_2, \mathrm{F} = DF_1 + (1-D)F_2 \end{aligned} \tag{3.91}$$

Step 3: Linearising around a operating point and obtain the ac small signal model

The all available time varying signals can be approximately written as sum of it's steady-state (DC or average) value and it's small variation around a operating point.

$$\begin{aligned} &i_L(t) = I_L + \hat{i}_L(t), i_g(t) = I_g + \hat{i}_g(t), i_o(t) = I_o + \hat{i}_o(t), i_z(t) = I_z + \hat{i}_z(t), \\ &d(t) = D + \hat{d}(t), v_C(t) = V_C + \hat{v}_C(t), v_g(t) = V_g + \hat{v}_g(t), v_o(t) = V_o + \hat{v}_o(t). \end{aligned} \tag{3.92}$$

To get the steady-state (DC) and small signal (ac) models of the non-ideal DC-DC buck-boost converter, substitute (3.92) in (3.89), (3.90), we get,

Steady-state (DC) model:

$$\begin{bmatrix}I_L\\ V_C\end{bmatrix} = -A^{-1}\left(B\begin{bmatrix}V_g\\ I_z\end{bmatrix} + J\right) \tag{3.93}$$

$$\begin{bmatrix} V_o \\ I_g \end{bmatrix} = C \begin{bmatrix} I_L \\ V_C \end{bmatrix} + E \begin{bmatrix} V_g \\ I_z \end{bmatrix} + F \tag{3.94}$$

Small-signal (ac) model:

$\tilde{\ }$ $\hat{\ }x$ A

$$\frac{d}{dt}\begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_C(t) \end{bmatrix} = \begin{bmatrix} -\frac{\Big(\ r_L + D\left[r_g + r_{on}\right] + (1-D)r_d\ \Big)(R+r_c)+(1-D)(Rr_c)}{L} & -\frac{(1-D)R}{L(R+r_c)} \\ \frac{(1-D)R}{C(R+r_c)} & -\frac{1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_C(t) \end{bmatrix}$$

B B_d

$$+ \begin{bmatrix} \frac{D}{L} & \frac{(1-D)Rr_c}{L(R+r_c)} \\ 0 & -\frac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \hat{v}_g(t) \\ \hat{i}_z(t) \end{bmatrix} + \begin{bmatrix} \frac{((r_d - r_g - r_{on})(R+r_c)+Rr_c)I_L + RV_c - Rr_cI_z + \left(V_g + V_{fd}\right)(R+r_c)}{L(R+r_c)} \\ -\frac{RI_L}{C(R+r_c)} \end{bmatrix} \left[\hat{d}(t)\right] \tag{3.95}$$

$\tilde{\ }$ $\hat{y}$ C E E_d

$$\begin{bmatrix} \hat{v}_o(t) \\ \hat{i}_g(t) \end{bmatrix} = \begin{bmatrix} \frac{(1-D)Rr_c}{R+r_c} & \frac{R}{R+r_c} \\ D & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_C(t) \end{bmatrix} + \begin{bmatrix} 0 & -\frac{Rr_c}{R+r_c} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_g(t) \\ \hat{i}_z(t) \end{bmatrix} + \begin{bmatrix} -\frac{Rr_cI_L}{R+r_c} \\ I_L \end{bmatrix} \left[\hat{d}(t)\right] \tag{3.96}$$

Step 4: Determination of steady-state values

The steady-state values of output voltage, input current and inductor current can also be found by substituting (3.95), (3.96) in (3.93), (3.94) as follows:

$$\Rightarrow I_L = \frac{V_o}{D'R} + \frac{I_z}{D'} \tag{3.97}$$

$$\Rightarrow I_g = \frac{DV_o}{D'R} + \frac{DI_z}{D'} \tag{3.98}$$

$$\Rightarrow V_o = \frac{[DV_g - D^{'}V_{fd}]D'R\left(R + r_c\right)}{[(r_L + D(r_{on} + r_g) + D^{'}r_d)(R + r_c)] + [D^{'}R(D^{'}R + r_c)]} \tag{3.99}$$

In order to get the ideal steady-state models of the DC-DC buck-boost converter, replace non-idealities or parasitics with zero in (3.97)-(3.99), we get,

$$\Rightarrow I_{Li} = \frac{V_{oi}}{D'R} + \frac{I_z}{D'} \tag{3.100}$$

$$\Rightarrow I_{gi} = \frac{DV_{oi}}{D'R} + \frac{DI_z}{D'} \tag{3.101}$$

$$\Rightarrow V_{oi} = \frac{DV_g}{1-D} \tag{3.102}$$

3.8.1 Comparison of steady-state ideal and non-ideal models

In order to compare the ideal and non-ideal models, converter parameters are consider from Table 3.1. These values substituted in relationships obtained for non-ideal and ideal cases given in (3.97)-(3.99) and (3.100)-(3.102) respectively. The values obtained in non-ideal case are always less than the ideal case, this is due to the power loss in non-ideal elements which is clear from Table 3.4. This has been clearly discussed in previous sections, where these steady-state relationships are derived analytically.

Table 3.4: Steady-state values comparison of ideal and non-ideal cases at $D = 0.399$

Parameter	Ideal case			Non-ideal case		
	Analytical	Experimental	Error	Analytical	Experimental	Error
I_L (A)	0.6	0.5	20%	0.52	0.5	3.8%
V_o (V)	7.96	7	12%	7	7	0%
I_g (A)	0.24	0.2	16.6%	0.2	0.2	0%

Step 5: Determination of various transfer functions

As per the considered input variables (v_g, i_z, d), state variables (i_L, v_C) and output variables (v_o, i_g) maximum twelve transfer functions are possible for non-ideal DC-DC buck-boost converter. Nevertheless, some important transfer functions only presented here. In order to get various transfer functions, first need to find $(sI - A)^{-1}$

for buck-boost converter, which is given below:

$$(sI-A)^{-1}=\frac{Adj(sI-A)}{|sI-A|}$$
$$=\frac{\begin{bmatrix} s+\frac{1}{C(R+r_c)} & -\frac{D^{'}R}{L(R+r_c)} \\ \frac{D^{'}R}{C(R+r_c)} & s+\frac{r_L+D(r_g+r_{on})+D^{'}(r_d+R\|r_c)}{L} \end{bmatrix}}{s^2+\frac{(R+r_c)\left(L+C\left(r_L+D(r_g+r_{on})+D^{'}r_d\right)(R+r_c)+D^{'}Rr_c\right)}{LC(R+r_c)^2}s+\frac{\left(r_L+D(r_g+r_{on})+D^{'}r_d\right)(R+r_c)+D^{'}R\left(D^{'}R+r_c\right)}{LC(R+r_c)^2}} \tag{3.103}$$

Now, some of the important transfer functions of non-ideal DC-DC buck-boost converter are derived, which are useful for controller design and analysis.

(i) Control to output voltage or Control voltage gain:

This transfer function describes the impact of variation in duty cycle ($\hat{d}(t)$) on output voltage ($\hat{v}_o$). This is derived by keeping the input voltage ($\hat{v}_g$) and output current ($\hat{i}_z$) variations to zero. This can be determined as follows:

$$G_{vd}(s)|_{\hat{v}_g,\hat{i}_z=0}=\frac{\hat{v}_o(s)}{\hat{d}(s)}=C(sI-A)^{-1}B_d+E_d \tag{3.104}$$

By substituting (3.95), (3.96) in (3.104) we get,

$$G_{vd}(s)=\begin{bmatrix}\frac{D^{'}Rr_c}{R+r_c} & \frac{R}{R+r_c}\end{bmatrix}\frac{Adj(sI-A)^{-1}}{|sI-A|}\begin{bmatrix}\frac{((r_d-r_g-r_{on})(R+r_c)+Rr_c)I_L+RV_c-Rr_cI_z+\left(V_g+V_{fd}\right)(R+r_c)}{L(R+r_c)} \\ -\frac{RI_L}{C(R+r_c)}\end{bmatrix}+\begin{bmatrix}-\frac{Rr_cI_L}{R+r_c}\end{bmatrix} \tag{3.105}$$

Further simplifying (3.105) and writing in terms of pole-zero form as given in (3.106)

$$G_{vd}(s)=K_{vd}\frac{\left(1+\frac{s}{\omega_{LHPz}}\right)\left(1-\frac{s}{\omega_{RHPz}}\right)}{1+\frac{s}{Q\omega_P}+\left(\frac{s}{\omega_P}\right)^2} \tag{3.106}$$

where,

$$K_{vd}=-\frac{\begin{pmatrix} V_g\left(D^2\left(r_g+r_{on}\right)+(2D-1)\,r_L-\left(D^{'}\right)^2\left(R+r_d\right)\right) \\ -D^{'}V_{fd}\left((1+D)\left(r_g+r_{on}\right)+2r_L+D^{'}\left(r_d+R\parallel r_c\right)\right)\end{pmatrix}}{\left(\left(r_L+D(r_{on}+r_g)+D^{'}r_d\right)\left(R+r_c\right)+D^{'}R\left(D^{'}R+r_c\right)\right)^2} \tag{3.107}$$

$$\omega_{RHPz}=\frac{\begin{matrix} V_g\left(D^2(r_g+r_{on})+(2D-1)r_L-\left(D^{'}\right)^2(R+r_d)\right) \\ -D^{'}V_{fd}\left((1+D)(r_g+r_{on})+2r_L+D^{'}(r_d+(R\parallel r_c))\right)\end{matrix}}{L(DV_g-D^{'}V_{fd})} \tag{3.108}$$

$$\omega_{LHPz} = \frac{1}{Cr_c} \tag{3.109}$$

$$\omega_p = \sqrt{\frac{\left(\left(r_L + D\left(r_{on} + r_g\right) + D'r_d\right)\left(R + r_c\right) + D'R\left(D'R + r_c\right)\right)}{LC(R + r_c)^2}} \tag{3.110}$$

$$Q = \frac{\sqrt{LC\left(\left(r_L + D\left(r_{on} + r_g\right) + D'r_d\right)\left(R + r_c\right) + D'R\left(D'R + r_c\right)\right)}}{L + C\left(\left(r_L + D\left(r_{on} + r_g\right) + D'r_d\right)\left(R + r_c\right) + D'Rr_c\right)} \tag{3.111}$$

This transfer function mainly used in controller design for regulator problems. Now, by replacing non-idealities or parasitics with zero in (3.106), we get the ideal model as,

$$G_{vdi}(s) = \frac{\widehat{v}_o}{\widehat{d}}(s) = \frac{V_g\left(1 - \frac{DL}{R(D')^2}s\right)}{(D')^2\left(\frac{LC}{(D')^2}s^2 + \frac{L}{R(D')^2}s + 1\right)} \tag{3.112}$$

(ii) Input to output voltage or Audio susceptibility:

This transfer function describes the impact of variation in input or line voltage ($\hat{v}_g$) on output voltage ($\hat{v}_o$). This is derived by keeping the duty cycle ($\hat{d}$) and output current ($\hat{i}_z$) variations to zero. This can be determined as follows:

$$G_{vg}(s)|_{\hat{i}_z,\hat{d}=0} = \frac{\hat{v}_o(s)}{\hat{v}_g(s)} = C(sI - A)^{-1}B_{1^{st}column} + E_{1^{st}column} \tag{3.113}$$

By substituting (3.95), (3.96) in (3.113) we get,

$$G_{vg}(s) = \begin{bmatrix} \frac{(1-D)Rr_c}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix} \frac{Adj(sI - A)^{-1}}{|sI - A|} \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{3.114}$$

Further simplifying (3.114) and writing interms of pole-zero form as given in (3.115)

$$G_{vg}(s) = K_{vg}\frac{\left(1 + \frac{s}{\omega_{LHPz}}\right)}{1 + \frac{s}{Q\omega_P} + \left(\frac{s}{\omega_P}\right)^2} \tag{3.115}$$

where,

$$K_{vg} = \frac{DD'R\left(R + r_c\right)}{\left(r_g + r_L + Dr_{on} + D'r_d\right)\left(R + r_c\right) + D'R\left(D'R + r_c\right)} \tag{3.116}$$

$$\omega_{LHPz} = \frac{1}{Cr_c} \tag{3.117}$$

$$\omega_p = \sqrt{\frac{\left(\left(r_L + D\left(r_{on} + r_g\right) + D'r_d\right)\left(R + r_c\right) + D'R\left(D'R + r_c\right)\right)}{LC(R + r_c)^2}} \tag{3.118}$$

$$Q = \frac{\sqrt{LC\left(\left(r_L + D\left(r_{on} + r_g\right) + D'r_d\right)\left(R + r_c\right) + D'R\left(D'R + r_c\right)\right)}}{L + C\left(\left(r_L + D\left(r_{on} + r_g\right) + D'r_d\right)\left(R + r_c\right) + D'Rr_c\right)} \tag{3.119}$$

This transfer function is very important in designing of regulator. The effect of input harmonics or changes in output can be found. Now, by replacing non-idealities or parasitics with zero in (3.115), we get the ideal model as,

$$G_{vgi}(s) = \frac{\widehat{v}_o}{\widehat{v}_g}(s) = \frac{D}{D'\left(\frac{LC}{(D')^2}s^2 + \frac{L}{R(D')^2}s + 1\right)} \tag{3.120}$$

(iii) Output Impedance:

This transfer function describes the impact of variation in output or load current ($\hat{i}_z$) on output voltage ($\hat{v}_o$). This is derived by keeping the duty cycle ($\hat{d}$) and input voltage ($\hat{v}_g$) variations to zero. This can be determined as follows:

$$Z_{out}(s)|_{\hat{v}_g, \hat{d}=0} = \frac{\hat{v}_o(s)}{\hat{i}_z(s)} = C(sI - A)^{-1}B_{2^{nd}column} + E_{2^{nd}column} \tag{3.121}$$

By substituting (3.95) and (3.96) in (3.121), we get,

$$Z_{out}(s) = \begin{bmatrix} \frac{(1-D)Rr_c}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix} \frac{Adj(sI - A)^{-1}}{|sI - A|} \begin{bmatrix} \frac{(1-D)Rr_c}{L(R+r_c)} \\ -\frac{R}{C(R+r_c)} \end{bmatrix} + \begin{bmatrix} -\frac{Rr_c}{R+r_c} \\ 0 \end{bmatrix} \tag{3.122}$$

Further simplifying (3.122) and writing in terms of pole-zero form as given in (3.123)

$$Z_{out}(s) = K_{zo}\frac{\left(1+\frac{s}{\omega_{LHPz1}}\right)\left(1+\frac{s}{\omega_{LHPz2}}\right)}{1+\frac{s}{Q\omega_P}+\left(\frac{s}{\omega_P}\right)^2} \tag{3.123}$$

where,

$$K_{zo} = -\frac{\left(r_L + D\left(r_{on} + r_g\right) + D'r_d\right)\left(R + r_c\right) + DD'Rr_c}{\left(r_L + D\left(r_{on} + r_g\right) + D'r_d\right)\left(R + r_c\right) + D'R\left(D'R + r_c\right)} \tag{3.124}$$

$$\omega_{LHPz1} = \frac{\left(r_L + D\left(r_{on} + r_g\right) + D'r_d\right)\left(R + r_c\right) + DD'Rr_c}{LCr_c\left(R + r_c\right)} \tag{3.125}$$

$$\omega_{LHPz2} = \frac{1}{Cr_c} \tag{3.126}$$

$$\omega_p = \sqrt{\frac{\left(\left(r_L + D\left(r_{on} + r_g\right) + D' r_d\right)\left(R + r_c\right) + D' R\left(D' R + r_c\right)\right)}{LC(R + r_c)^2}} \tag{3.127}$$

$$Q = \frac{\sqrt{LC\left(\left(r_L + D\left(r_{on} + r_g\right) + D' r_d\right)\left(R + r_c\right) + D' R\left(D' R + r_c\right)\right)}}{L + C\left(\left(r_L + D\left(r_{on} + r_g\right) + D' r_d\right)\left(R + r_c\right) + D' R r_c\right)} \tag{3.128}$$

This transfer function also very important quantity in voltage regulator design. Now, by replacing non-idealities or parasitics with zero in (3.123), we get the ideal model as,

$$Z_{outi}(s) = \frac{\hat{v}_o(s)}{\hat{i}_z(s)} = \frac{LC}{(1-D)^2} \frac{-\frac{s}{C}}{\frac{LC}{(1-D)^2} s^2 + \frac{L}{R(1-D)^2} s + 1} \tag{3.129}$$

(iv) Input Impedance:

This transfer function describes the impact of variation in input or line voltage ($\hat{v}_g$) on input current ($\hat{i}_g$). This is derived by keeping the duty cycle ($\hat{d}$) and output current ($\hat{i}_o$) variations to zero. This can be determined as follows:

$$Z_{in}^{-1}(s)\big|_{\hat{i}_z, \hat{d}=0} = \frac{\hat{i}_g(s)}{\hat{v}_g(s)} = C_{2^{nd}row}(sI - A)^{-1} B_{1^{st}column} + E_{1^{st}column} \tag{3.130}$$

By substituting (3.95), (3.96) in (3.130) we get,

$$Z_{in}^{-1}(s) = \begin{bmatrix} D & 0 \end{bmatrix} \frac{Adj(sI - A)^{-1}}{|sI - A|} \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{3.131}$$

Further simplifying (3.131) and writing in terms of pole-zero form as given in (3.132)

$$Z_{in}^{-1}(s) == K_{Zi} \frac{\left(1 + \frac{s}{\omega_{LHPz}}\right)}{1 + \frac{s}{Q\omega_P} + \left(\frac{s}{\omega_P}\right)^2} \tag{3.132}$$

where,

$$K_{Zi} = D^2 \frac{(R + r_c)}{\left(r_L + D\left(r_{on} + r_g\right) + D' r_d\right)\left(R + r_c\right) + D' R\left(D' R + r_c\right)} \tag{3.133}$$

$$\omega_{LHPz} = \frac{1}{C\left(R + r_c\right)} \tag{3.134}$$

$$\omega_p = \sqrt{\frac{\left(\left(r_L + D\left(r_{on} + r_g\right) + D' r_d\right)\left(R + r_c\right) + D' R\left(D' R + r_c\right)\right)}{LC(R + r_c)^2}} \tag{3.135}$$

$$Q = \frac{\sqrt{LC\left(\left(r_L + D\left(r_{on} + r_g\right) + D'r_d\right)\left(R + r_c\right) + D'R\left(D'R + r_c\right)\right)}}{L + C\left(\left(r_L + D\left(r_{on} + r_g\right) + D'r_d\right)\left(R + r_c\right) + D'Rr_c\right)} \tag{3.136}$$

This transfer function is useful for cascaded converters and it plays important role when EMI filter is added [4]. Now, by replacing non-idealities or parasitics with zero in (3.132), we get the ideal model as,

$$Z_{ini}^{-1}(s) = \frac{\widehat{i}_g(s)}{\widehat{v}_g(s)} = \frac{D^2\left(CRs + 1\right)}{R(D')^2\left(\frac{LC}{\left(D'\right)^2}s^2 + \frac{LC}{R\left(D'\right)^2}s + 1\right)} \tag{3.137}$$

3.8.2 Comparison of small-signal ideal and non-ideal models

In order to compare the small signal models of ideal and non-ideal plants, the converter parameters are consider from Table 3.5. These values substituted in relationships obtained for non-ideal and ideal cases given in (3.106)-(3.137).

The comparison is shown in Table 3.5. From this table, it is observed that the quality factor (Q) is less for non-ideal model (nearly 5 times lesser the ideal value), which tells that there will not be much peak in output. Most of the transfer functions derived from non-idealities are having an extra zeros compared to their ideal models. The steady-state gain of non-ideal models is completely different than ideal models. Therefore, it is clear that non-idealities or parasitics make a lot difference in non-ideal and ideal small signal models.

The non-ideal model transfer functions derived in this section will be further analysed from control point of view and effect of non-idealities or parasitics also analysed.

Table 3.5: Transfer function comparison of ideal and non-ideal cases

Parameter	$G_{vd}(s)$		$G_{vg}(s)$		$Z_o(s)$		$Z_{in}^{-1}(s)$	
	Ideal	Non-ideal	Ideal	Non-ideal	Ideal	Non-ideal	Ideal	Non-ideal
K (dB)	30.44	29.34	-3.5	-4.1	-20.18	3	-34	-34.5
ω_{LHPz}	-	50000	-	50000	0	1387,50k	450.5	454.5
ω_{RHPz}	50680	54450	-	-	-	-	-	-
ω_P	3119.7	3031.6	3119.7	3031.6	3119.7	3031.6	3119.7	3031.6
Q	6.67	1.5	6.67	1.5	6.67	1.5	6.67	1.5

3.9 Control Oriented Analysis

This section presents the importance of derived non-ideal transfer functions and crucial observations made through time domain and frequency response analysis. The transfer functions, which are discussed, mainly useful for voltage mode control, which is the objective of this thesis. Further, this section reveals the importance of small-signal transfer functions obtained by using state apace average approach over the respective ideal models or transfer functions.

3.9.1 Analysis of control to output voltage or control voltage gain

3.9.1.1 Parametric effect on poles and zeros

The small-signal model or control to output transfer function presented in (3.106), shows that it is a common two pole low pass filter with two zeros. Where as, (3.112) is an ideal one, which is also the same but with one zero. Now, the effect poles, zeros with respect to buck-boost converter parameters are analysed.

The trajectory of poles and zeros of ideal and non-ideal transfer functions at different values of the duty cycle D is shown in Figure 3.30. In case of non-ideal model, the LHP zero $z_1 = \frac{-1}{\omega_{LHPz}}$ do not alter with the duty cycle as it is free from duty cycle and obtained by the filter capacitor C and its equivalent series resistance r_C, where as, in ideal model there is no LHP zero. The poles locations are severely affected by the duty cycle in both ideal and non-ideal cases. Especially, in non-ideal case, poles are far from imaginary axis compared to the ideal case. The RHP zero $z_2 = \frac{1}{\omega_{RHPz}}$ moves towards origin with increase in the duty cycle in both the cases. At low duty ratios, the zero is located in the right-half of the s-plane. With increase in the duty cycle, the RHP-zero moves towards the origin. In non-ideal case, at one point (Shown as small circle), the RHP zero is crossing the origin and moving to LHP, where as in ideal case there is no such possibility. This corresponds to a maximum possible value of duty cycle *i.e.,* D_{max}.

The trajectory of poles and zeros of ideal and non-ideal transfer functions at dif-

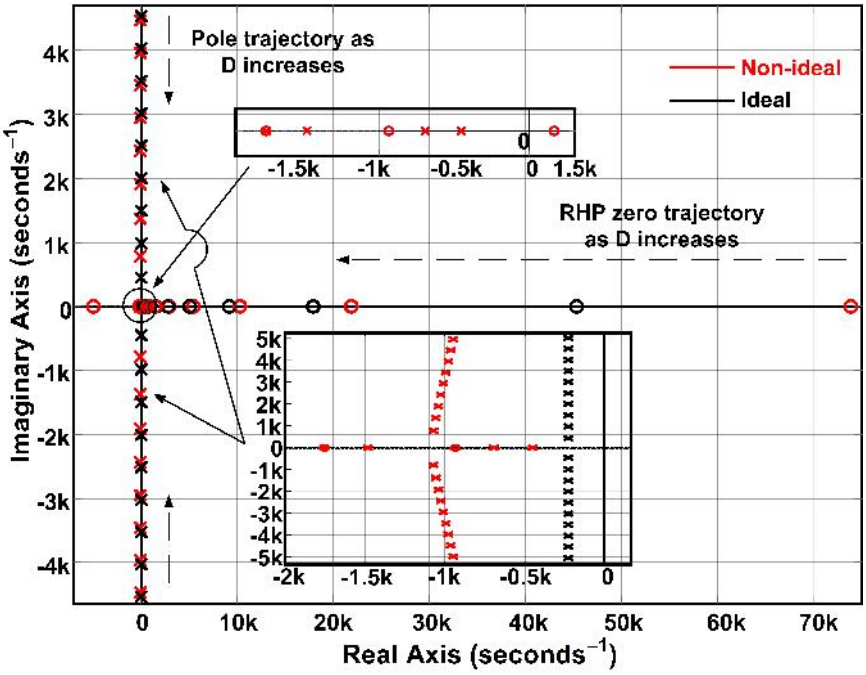


Figure 3.30: Pole zero trajectories with duty cycle variation.

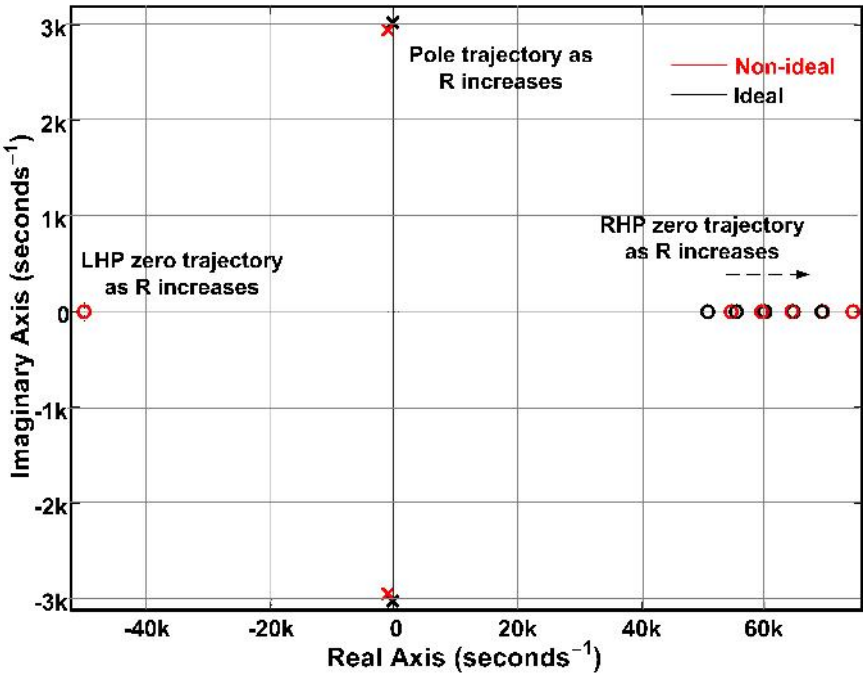


Figure 3.31: Pole zero trajectories with load variation.

ferent values of the load resistance R is shown in Figure 3.31. In case of non-ideal model, the LHP zero $z_1 = \frac{-1}{\omega_{LHPz}}$ do not alter with the load resistance as it is free from

R term and obtained by the filter capacitor C and its equivalent series resistance r_C, where as, in ideal model there is no LHP zero. The poles locations are not affected by the resistance variation in ideal case, where as in non-ideal case its little effected. However, the RHP zero $z_2 = \frac{1}{\omega_{RHPz}}$ moves towards $\inf$ with increase in the load resistance, which means converter is more stable at higher load resistances or low output powers. From this, it can be observed that the controller design of plant should be done for the worst-case condition, which is at minimum load condition.

The trajectory of poles and zeros of ideal and non-ideal transfer functions at different values of the inductance L is shown in Figure 3.32. In case of non-ideal model, the LHP zero $z_1 = \frac{-1}{\omega_{LHPz}}$ do not alter with the inductance as it is free from L term and obtained by the filter capacitor C and its equivalent series resistance r_C, where as, in ideal model there is no LHP zero. The poles locations are also affected by the inductance variation in both ideal and non-ideal cases. However, the RHP zero $z_2 = \frac{1}{\omega_{RHPz}}$ moves towards origin with increase in the inductance.

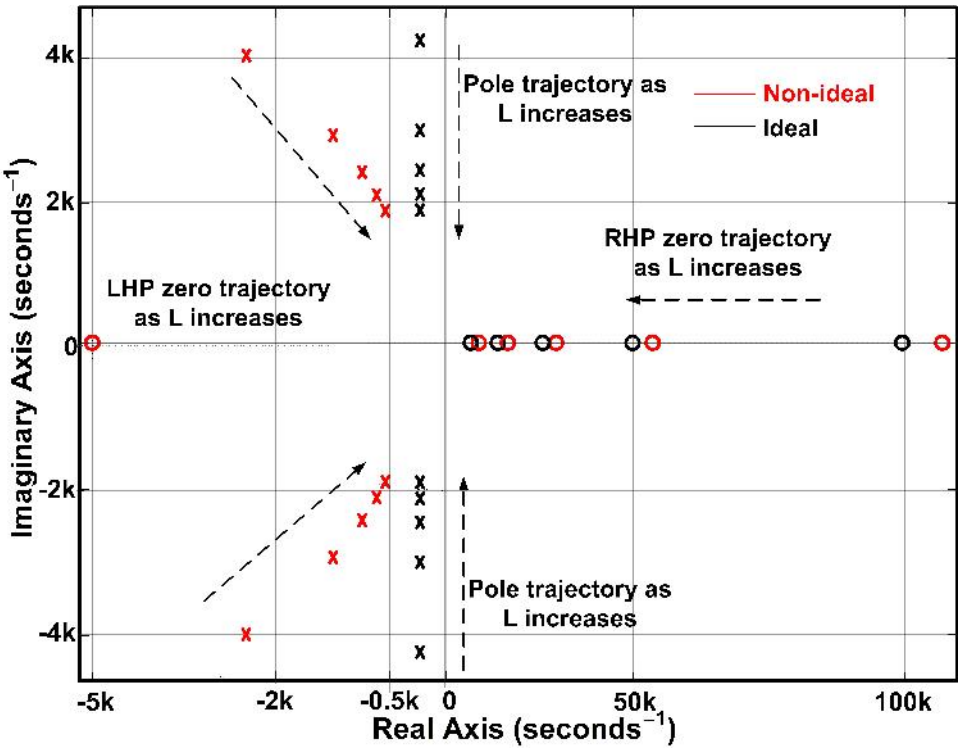


Figure 3.32: Pole zero trajectories with inductance variation.

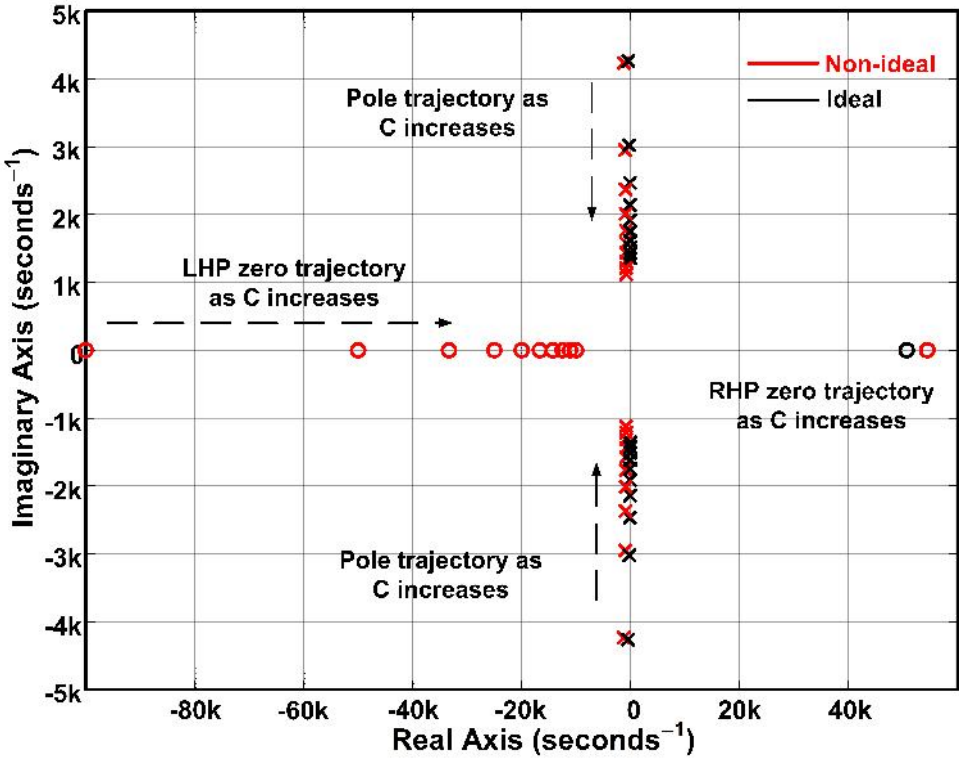


Figure 3.33: Pole zero trajectories with capacitance variation.

The trajectory of poles and zeros of ideal and non-ideal transfer functions at different values of the capacitance C is shown in Figure 3.33. The LHP zero $z_1 = \frac{-1}{\omega_{LHPz}}$ moves towards origin with the increase in capacitance, where as, in ideal model there is no LHP zero. The poles locations are also affected by the inductance variation in both ideal and non-ideal cases. However, the RHP zero $z_2 = \frac{1}{\omega_{RHPz}}$ do not alter, as it is free from C term.

3.9.1.2 Time domain and frequency response analysis

By replacing the parameter values in (3.106) and (3.112), we get the transfer functions of non-ideal and ideal models of DC-DC buck-boost converter as

$$G_{vd}(s) = \frac{29.29\left(\frac{s}{50000}+1\right)\left(-\frac{s}{54450}+1\right)}{\left(\frac{s}{3119.7}\right)^2+\frac{s}{4818.3}+1} \tag{3.138}$$

$$G_{vdi}(s) = \frac{33.22\left(-\frac{s}{50680}+1\right)}{\left(\frac{s}{3031.6}\right)^2+\frac{s}{20222.2}+1}. \tag{3.139}$$

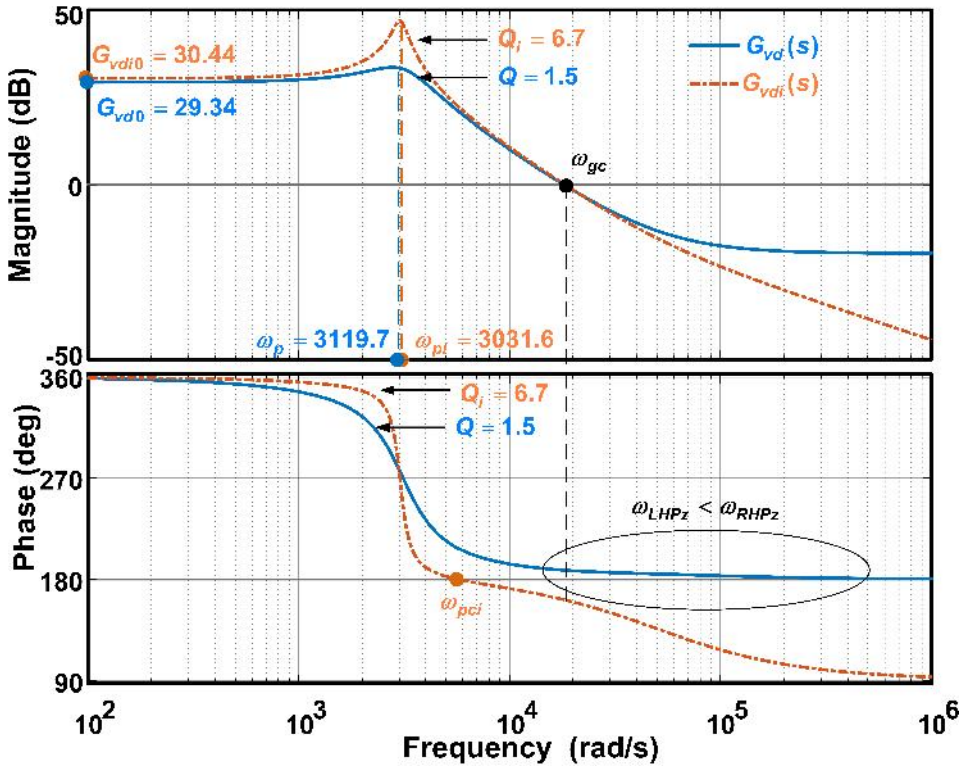


Figure 3.34: Frequency responses of ideal and non-ideal models.

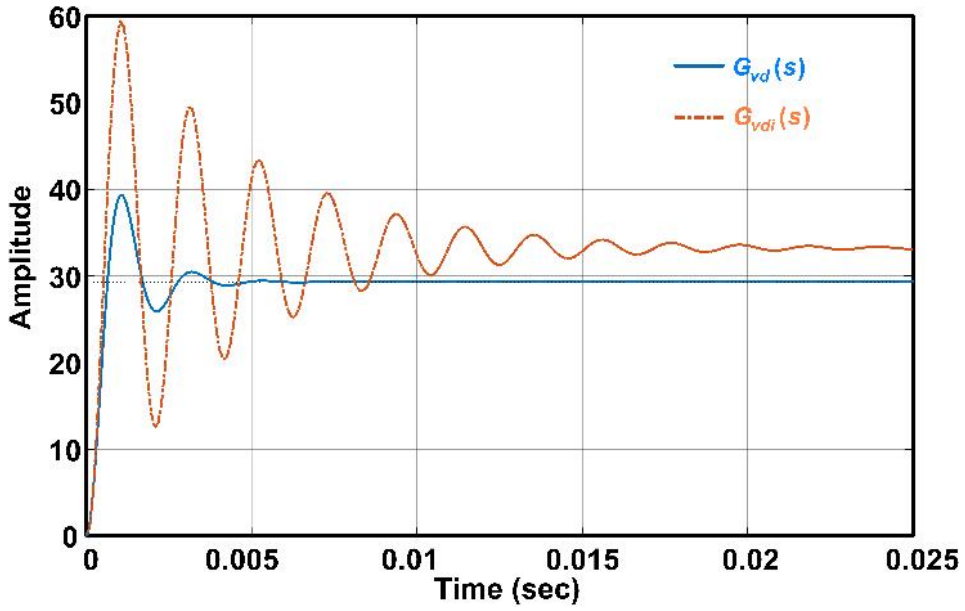


Figure 3.35: Step responses of ideal and non-ideal models.

As we have seen in previous discussion, these transfer functions have RHP zero, which makes system non-minimum phase. Figure 3.34 and Figure 3.35 show the frequency and step responses of control to output transfer functions of ideal and non-ideal models, respectively. The dc or low frequency gain of ideal model is $G_{vdio} = 30.44dB = 33.26V/\Delta d$, where as for non-ideal model is $G_{vdo} = 29.34dB = 29.3V/\Delta d$. From results section, Figure 3.14 and Figure 3.15, shows that for a change in duty cycle ($\Delta d = 0.031$), corresponding output voltage (V_o) changes from $-6V$ to $-7V$, *i.e.,* $\Delta v_o = 1V$. The gain calculated as $\frac{\Delta v_o}{\Delta d} = 30.1 \simeq G_{vdo}$, which shows the accuracy of non-ideal model. Further from Bode plots, it is clear that bandwidth is limited as it is a case of non-minimum phase system. More discussion on RHP zero can be seen in Chapter 5. It can be clearly observed that crossover frequency obtained using ideal model is very less compared to that of non-ideal model. From step responses also it can be observed that non-idealities provides damping and there will not be much oscillations as in the case of ideal.

3.9.1.3 Important observations for controller design

From the previous analysis of the control to output transfer function, the following observations can be drawn for the closed-loop control design:

- For designing robust controller by considering the parametric variations, the linear transfer function model presented in (3.106) is essential, since the model shows the dependency of pole zero frequencies on parasitics.

- From the transfer function, it is observed that the following condition must be satisfied to ensure the closed-loop stability of converter.

$$(f_{LHPz} - f_{RHPz}) < \frac{f_p}{Q} \tag{3.140}$$

  This term mostly effected by inductor and capacitor values.

- The frequency location of RHP zero (ω_{RHPz}) can be calculated exactly and how this depends on parasitics can be analysed with the expression shown (3.106).

Since, the RHP zero limits the bandwidth of buck-boost converter, this analysis is important.

- In case of non-ideal analysis, an additional LHP zero is added, which will help for the bandwidth improvement. From the expression of LHP zero frequency ω_{LHPz}, we observe that it depends on capacitor value and its ESR.
- The selection of cross over frequency should be well below the frequency of RHP zero and frequency of LHP zero should be greater than the RHP zero.
- Effect of parasitic elements on closed-loop stability of the converter system is observed from Table 3.6. All parasitics are providing stability in system and improving the closed-loop performance.

Table 3.6: Effect of parasitics on control to output transfer function

Elements (As it increases)	L	C	R	r_g	r_L	r_c	r_{on}	r_d	V_{fd}
K_{vd}	$\times$	$\times$	$\uparrow$	$\Downarrow$	$\Downarrow$	$\downarrow$	$\downarrow$	*	$\times$
ω_{LHPz}	$\times$	$\Downarrow$	$\times$	$\times$	$\times$	$\Downarrow$	$\times$	$\times$	$\times$
ω_{RHPz}	$\Downarrow$	$\times$	$\Uparrow$	$\Downarrow$	$\Downarrow$	$\downarrow$	$\Downarrow$	$\times$	$\uparrow$
ω_p	$\Downarrow$	$\Downarrow$	$\downarrow$	$\Uparrow$	$\Uparrow$	*	*	*	$\times$
Q	$\Uparrow$	$\Downarrow$	$\uparrow$	$\Downarrow$	$\Downarrow$	$\Downarrow$	$\downarrow$	$\downarrow$	$\times$
Over all closed loop stability	$\Downarrow$	$\Uparrow$	$\Uparrow$	$\Uparrow$	$\Uparrow$	$\Uparrow$	*	*	*

$\Uparrow$Improves, $\uparrow$Slight improvement, $\Downarrow$Decrement, $\downarrow$Slight decrement, *Insignificant, $\times$No effect

3.9.2 Analysis of input to output voltage or audio susceptibility

By replacing the parameter values in (3.115) and (3.120), we get the transfer functions of non-ideal and ideal models of DC-DC buck-boost converter as

$$G_{vg}(s) = \frac{0.62\left(\frac{s}{50000}+1\right)}{\left(\frac{s}{3119.7}\right)^2 + \frac{s}{4818.3} + 1} \tag{3.141}$$

$$G_{vgi}(s) = \frac{0.6634}{\left(\frac{s}{3031.6}\right)^2 + \frac{s}{20222.2} + 1}. \tag{3.142}$$

Figure 3.36 and Figure 3.38 show the frequency and step responses of input voltage

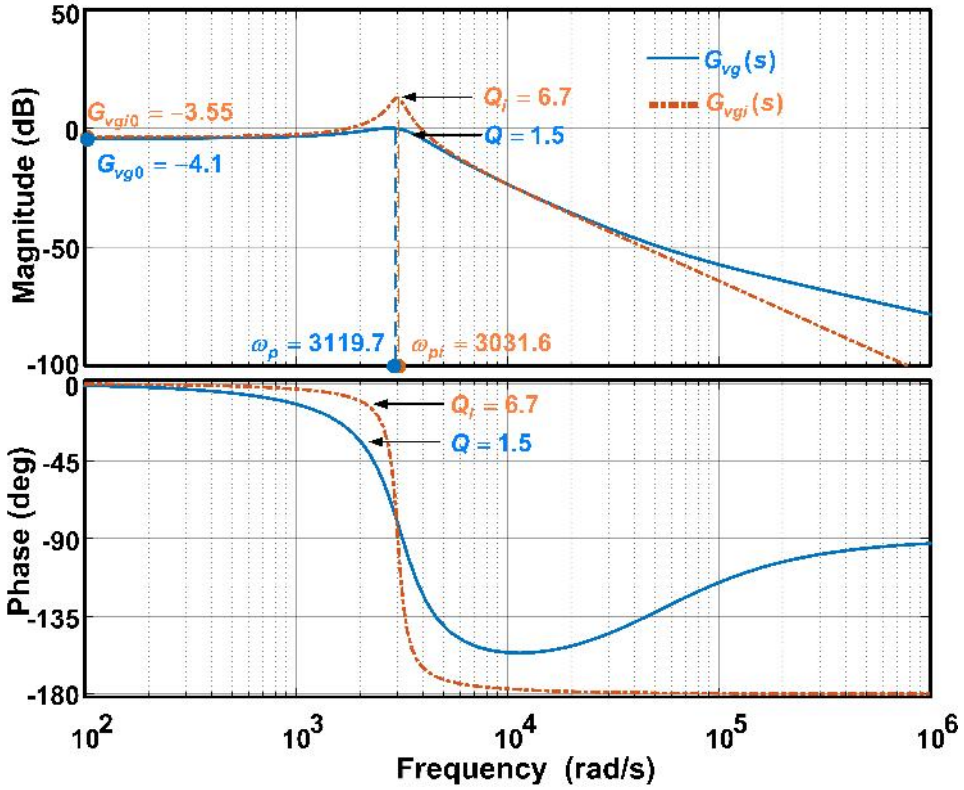


Figure 3.36: Frequency responses of ideal and non-ideal models.

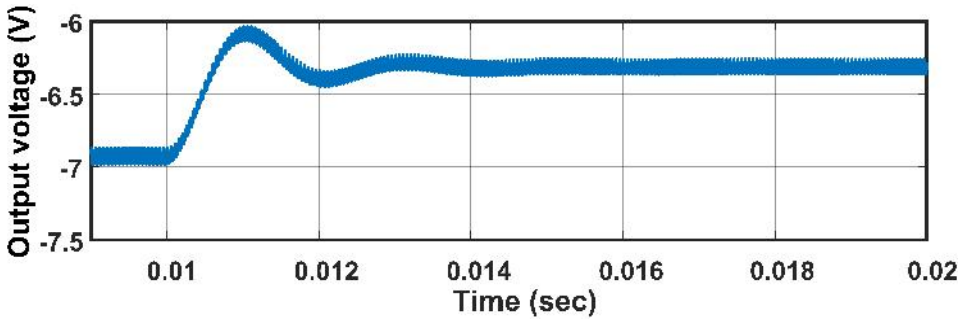


Figure 3.37: Output voltage change for input voltage change of 1V.

to output voltage transfer functions of ideal and non-ideal models, respectively. The

dc or low frequency gain of ideal model is $G_{vgio} = -3.55dB = 0.66V/V$, where as for non-ideal model is $G_{vgo} = -4.1dB = 0.62V/V$. From Figure 3.37, it can be observed that for a change in input voltage ($\Delta v_g = 1V$), corresponding output voltage (V_o) changes from $-7V$ to $-6.4V$, *i.e.,* $\Delta v_o = 0.6V$. The gain calculated

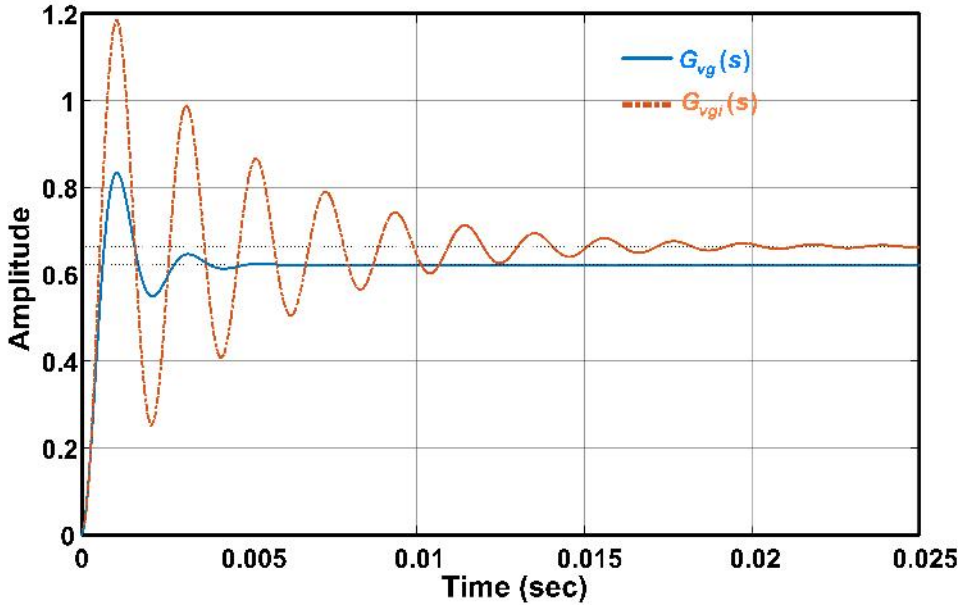


Figure 3.38: Step responses of ideal and non-ideal models.

as $\frac{\Delta v_o}{\Delta v_g} = 0.6 \simeq G_{vgo}$, which shows the accuracy of non-ideal model. Further from Bode plots, it is be observed that stability (PM and GM) of non-ideal model is more compared to ideal model. Moreover, step response also confirms that, non-ideal model is less oscillatory compared to ideal model. From this, it can be concluded that parasitics or non-idealities are improving the stability of uncompensated buck-boost converter in closed-loop under input voltage disturbances.

3.9.3 Analysis of output impedance

By replacing the parameter values in (3.123) and (3.129), we get the transfer functions of non-ideal and ideal models of DC-DC buck-boost converter as

$$Z_o(s) = -\frac{1.414\left(\frac{s}{1387}+1\right)\left(\frac{s}{50000}+1\right)}{\left(\frac{s}{3119.7}\right)^2+\frac{s}{4818.3}+1} \tag{3.143}$$

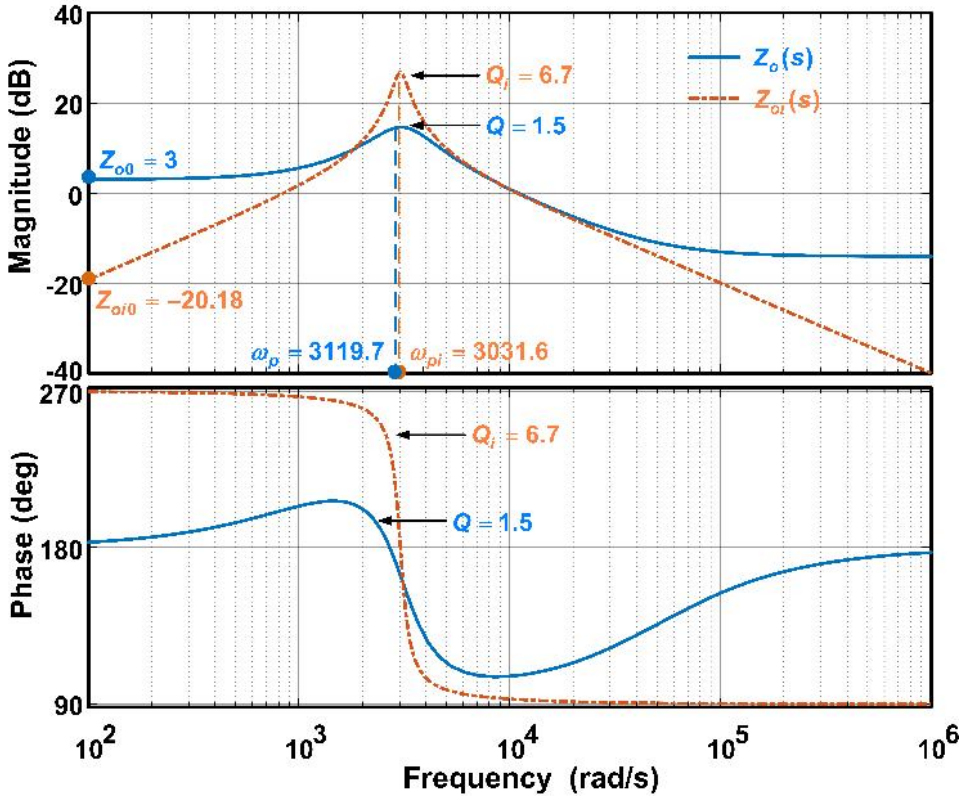


Figure 3.39: Frequency responses comparison of ideal and non-ideal models.

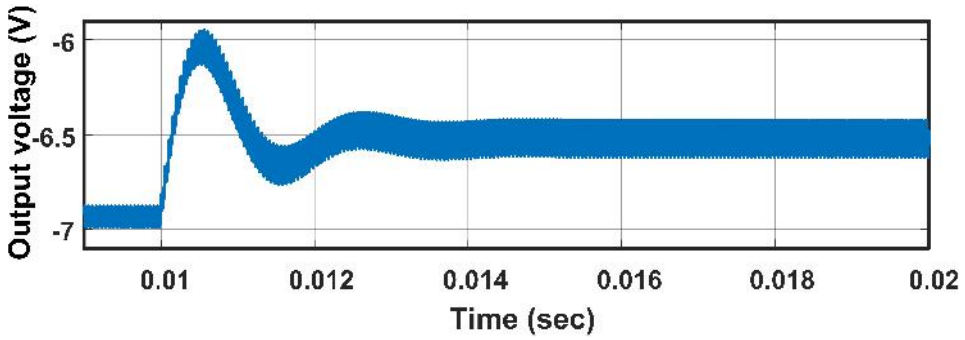


Figure 3.40: Output voltage change for load current change of 0.2A.

$$Z_{oi}(s) = \frac{-\frac{s}{9191}}{\left(\frac{s}{3031.6}\right)^2 + \frac{s}{20222.2} + 1}. \tag{3.144}$$

Figure 3.39 and Figure 3.41 show the frequency and step responses of load current to output voltage transfer functions or output impedance of ideal and non-ideal models, respectively. The dc or low frequency gain of ideal model is $Z_{oi0} = -20.18dB =$

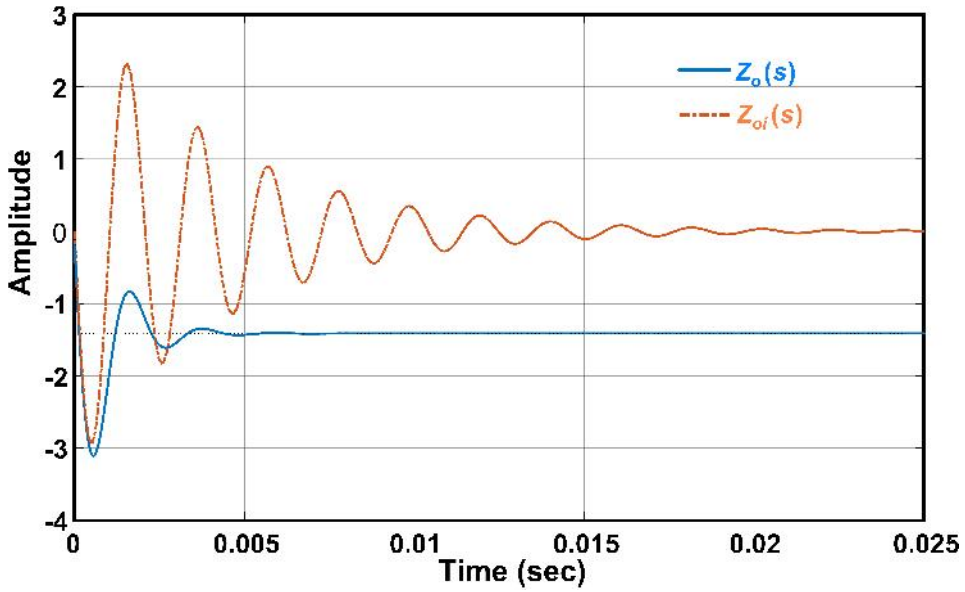


Figure 3.41: Step responses comparison of ideal and non-ideal models.

0.108Ω, where as for non-ideal model is $Z_{o0} = 3dB = 1.41\Omega$. Figure 3.40, shows that for a change in load current ($\Delta i_z = 0.35A$), corresponding output voltage (V_o) changes from $-7V$ to $-6.5V$, *i.e.,* $\Delta v_o = 0.5V$. The gain calculated as $\frac{\Delta v_o}{\Delta i_z} = 1.43\Omega \simeq Z_{o0}$, which shows the accuracy of non-ideal model. At dc and low frequencies, capacitive reactance is more and output impedance is dominated by inductive reactance. As frequency increases, the capacitive reactance dominates and makes impedance zero.

3.9.4 Analysis of input impedance

By replacing the parameter values in (3.132) and (3.137), we get the transfer functions of non-ideal and ideal models of DC-DC buck-boost converter as

$$Z_{in}^{-1}(s) = \frac{0.018\left(\frac{s}{450.5}+1\right)}{\left(\frac{s}{3119.7}\right)^2 + \frac{s}{4818.3} + 1} \tag{3.145}$$

$$Z_{ini}^{-1}(s) = \frac{0.02\left(\frac{s}{454.5}+1\right)}{\left(\frac{s}{3031.6}\right)^2 + \frac{s}{20222.2} + 1} \tag{3.146}$$

Figure 3.42 and Figure 3.43 show the frequency and step responses of input current to input voltage transfer functions of ideal and non-ideal models respectively. From

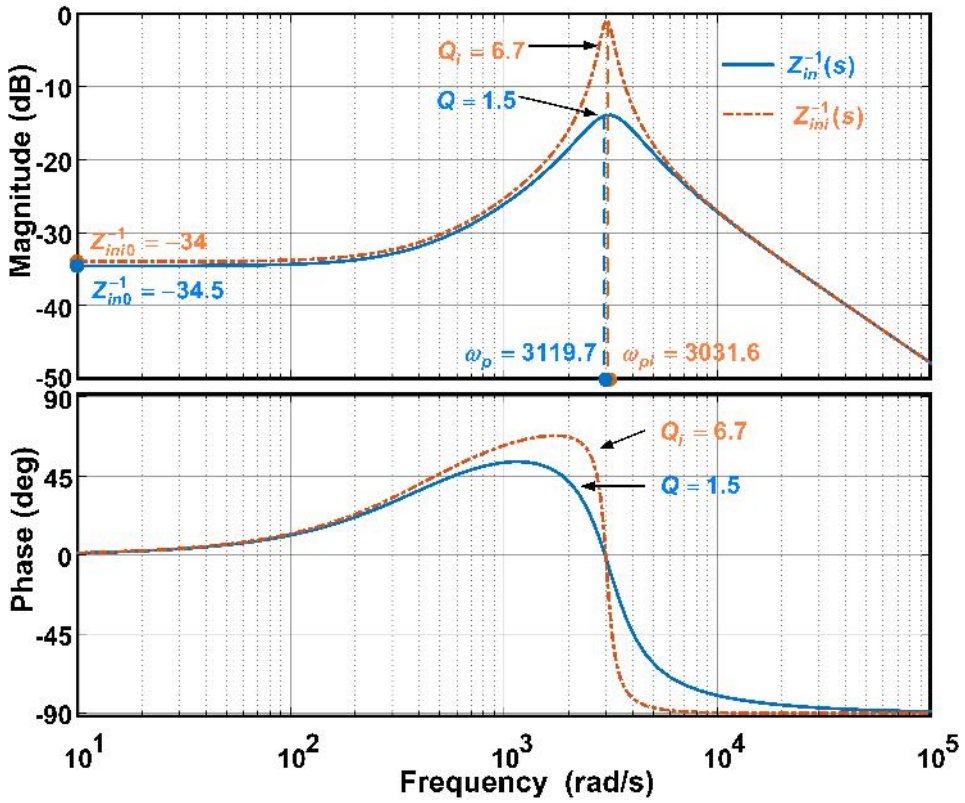


Figure 3.42: Frequency responses comparison of ideal and non-ideal models.

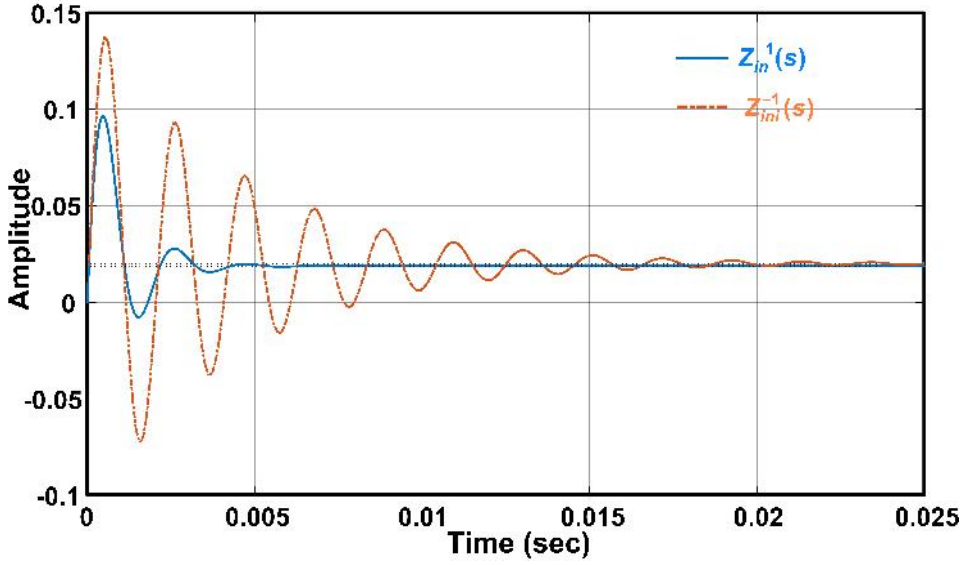


Figure 3.43: Step responses comparison of ideal and non-ideal models.

the Bode plot, it is be observed that the input impedance is $Z_{in} = 55.56\Omega$ at low frequencies or dc and it is minimum at corner frequencies. Phase is decreasing from 0 to -90, as frequency increasing. From step responses, it is be observed that the steady state error is zero in both cases, but ideal is more oscillatory.

3.10 Conclusions

An improved duty cycle relationship for a non-ideal DC-DC PWM buck-boost converter has been derived and also demonstrated that the ideally calculated duty cycle results in lower output voltage than the anticipated value. Further, the modified design equations of inductor and capacitor by considering the all parasitics have been presented. Here, from analysis, it is observed that inductor, capacitor design, ICR and OVR are associated with each other. From this, it is inferred that, ICR has definite role in capacitor design and capacitor ESR also has significant role on inductor design. Alongside, the ripple analysis concludes that the ESR of output filter capacitor effects more on OVR. Conclusively, it is recommended to design engineers to use these modified expressions in accurate design of buck-boost converter modules.

Although, most of the work presents open-loop operation, it gives the critical information about specifications such as the maximum achievable output voltage and duty cycle respectively, which are essential for closed-loop operation and also helpful to engineers in control design of DC-DC buck-boost converter in applications such as military, aerospace etc. Overall, parasitics are enhancing the stability of closed-loop system, this can be negotiated from small-signal analysis.

Eventually, experimental results confirms the importance of non-ideal model of the buck-boost converter to estimate the performances of new control techniques. The non-ideal model is resembling the practical system. The analysis of controller performance is very easy. Since, all parasitic effect is very clear on transfer function model, it is easy to observe the robust performance of the converter under parametric variations.

CHAPTER 4

NON-IDEAL NON-INVERTING DC-DC BUCK-BOOST CONVERTER

This chapter presents different design issues and accurate mathematical modeling of non-ideal non-inverting buck-boost converter (NIBB) in detail. The steady-state and dynamic analysis of non-ideal NIBB converter are explained. Various transfer functions are derived and analyzed the effect of non-idealities. Further, NIBB derived hybrid converter is proposed. The proposed converter design and analysis is presented in detail and compared with other hybrid converter topologies.

4.1 Background and Motivation

A PWM DC-DC NIBB converter is also used for step up/down voltage, similar to basic buck-boost converter, which is derived from basic topologies of DC-DC converters (Buck and Boost). The basic difference is that it does not invert output voltage, where as basic buck-boost or cuk converter invert the output, which results in complicated auxiliary power supply and drive circuit [175]. In comparison to SEPIC, ZETA converters, which are of higher order (fourth order or contain two inductors and capacitors), NIBB is a second order and leading to high power density [176]. In addition, the stress on switches in other (Cuk, SEPIC, ZEta etc.) topologies is more (*i.e.,* the sum of input and output voltages).

In view of these advantages, similar to other converters this also need accurate analysis and optimal design. After going through literature, a very few researchers [32], [177]- [181], worked on this and specifically with ideal nature of elements only. Thus, in present work, the component design and analysis of DC-DC NIBB converter operating in CCM (continuous conduction mode), performed by considering the all parasitic elements.

NIBB converter, which is formed by cascade connection of buck with boost converter and its output voltage expression is similar to buck-boost converter but with positive polarity, which is given in (4.1)

$$V_o = \frac{D_1}{1 - D_2} V_g \tag{4.1}$$

The above expression is obtained by considering ideal nature of elements [179]. From this expression, it is found that it has two duty cycles. This expression also reveals that it can be operated in three different modes as shown Table 4.1.

Table 4.1: Operating modes of NIBB converter

Mode of operation	D_1	D_2
Buck	0 to 1	0
Boost	1	0 to 1
Buck-boost	0 to 1	0 to 1 and always $D_2 < D_1$

The non-ideal analysis and modeling shown in previous chapters are of converters with single switch. Since there is more than one switch, it is a little different from previous chapters. For NIBB also maximum achievable voltage and duty cycles are derived in further sections, which are very important for closed-loop operation.

NIBB converter is similar to buck and boost converters, therefore, design of inductor and capacitor also similar to them. The design for inductor and capacitor along with ripple analysis is given for NIBB converter. Further, another interesting part of this work is that the mathematical modeling of NIBB converter since, it is having two switches. Complete modeling is carried out by including all non-idealities as discussed in the previous chapters.

Alongside, a hybrid converter is proposed based on NIBB converter, which can give both ac and dc outputs simultaneously. The detailed operation of NIBB derived hybrid converter and advantages over the existing hybrid converters presented. The control method to generate pulses for switches also explained.

The following sections discuss the detailed analysis of non-ideal dc-dc NIBB converter and proposed hybrid converter.

4.2 Fundamental Analysis

Similar to previous converters, this section presents the preliminary equations of non-ideal DC-DC NIBB converter operating in CCM. Basic non-ideal non-inverting buck-boost converter system is shown in Figure 4.1(a). In this figure, elements are represented as switches (S_1 and S_2), diodes (D_{d1} and D_{d2}), inductor (L), capacitor (C) and load resistance (R). To acquire precise model of non-inverting buck-boost converter, all parasitic resistances are considered such as source resistance (r_g), inductor resistance (r_L), switch resistances (r_{s1} and r_{s2}), diode resistances (r_{d1} and r_{d2}), diodes forward voltage drop (v_{fd1} and v_{fd2}), capacitor ESR (r_c). Further, V_g , v_o, v_c and v_L are input, output, capacitor and inductor voltages respectively. Alongside, i_L, i_c are inductor and capacitor currents respectively, and D_1, D_2 are duty cycles of switches S_1, S_2. The most important condition for the operation is always $D_2 < D_1$.

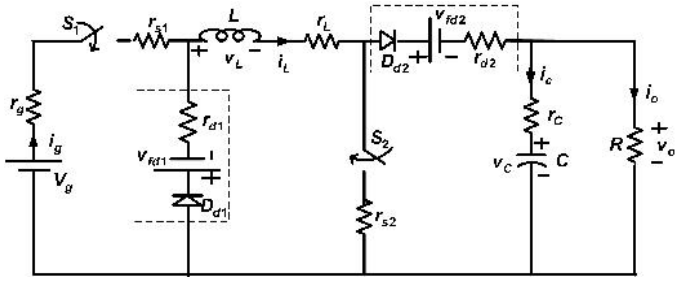
Here, we have made few assumptions for analysing the PWM DC-DC NIBB converter.

Assumption 1: PWM DC-DC NIBB converter is operating in continuous conduction mode (CCM). In CCM operation, converter works in three switching intervals: (a) Mode-I interval, *i.e.*, $0 < t \leq D_2T$, (b) Mode-II interval, *i.e.*, $D_2T < t \leq D_1T$ and (c) Mode-III interval, *i.e.*, $D_1T < t \leq T$ [4].

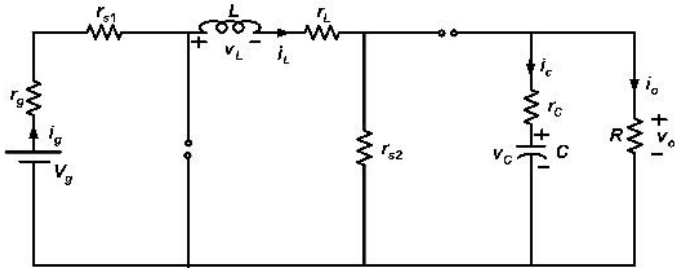
Assumption 2: Initial charging current through inductor is zero, *i.e.,* $i_L(0) = 0$ and initial voltage across the capacitor is zero, *i.e.,* $v_c(0) = 0$.

4.2.1 Mode-I Operation ($0 < t < D_2T$)

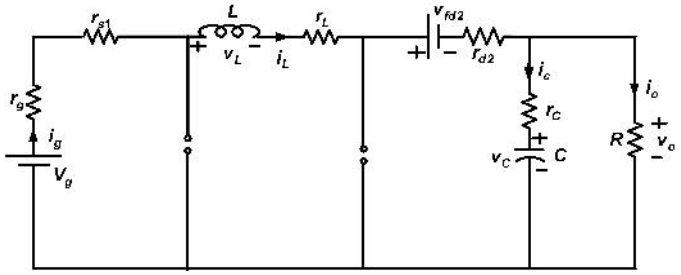
The equivalent circuit for NIBB converter during interval $0 < t \leq D_2T$ *i.e.,* when both switches ON is shown in Figure 4.1(b). In this interval, the diodes (D_{d1} and D_{d2}) are OFF and switches are replaced by their ON time resistances (r_{s1} and r_{s2}). Here, the input current (i_g) is same as inductor current (i_L) and diode current (i_d) is



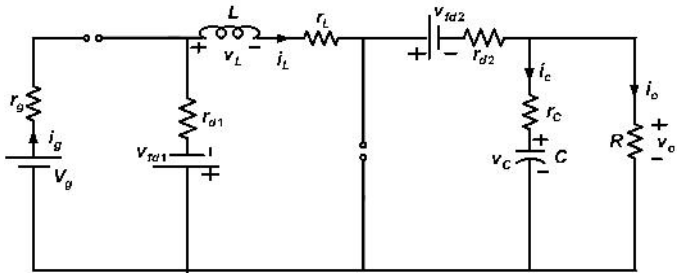
(a)



(b)



(c)



(d)

Figure 4.1: Schematic of (a)non-ideal DC-DC non-inverting buck-boost converter (b)Mode-I operation (S_1-ON, S_2-ON) (c)Mode-II operation (S_1-ON, S_2-OFF) (d)Mode-III operation (S_1-OFF, S_2-OFF).

zero. During this period, the inductor stores energy, and the output capacitor alone delivers power to the load.

Using Kirchhoffs voltage law (KVL) and Kirchhoffs current law (KCL), the fundamental equations for the circuit shown in Figure 4.1(b) are obtained as follows:

$$(v_L(t))_{M1} = L\frac{di_L(t)}{dt} = -\left(r_g + r_{s1} + r_L + r_{s2}\right) i_L(t) + v_g(t) \tag{4.2}$$

$$(i_c(t))_{M1} = C\frac{dv_c(t)}{dt} = -\frac{v_o(t)}{R} \tag{4.3}$$

$$(v_o(t))_{M1} = v_c(t) + r_c i_c(t) \tag{4.4}$$

4.2.2 Mode-II Operation ($D_2T < t < D_1T$)

The equivalent circuit for NIBB converter during interval $D_2T < t \leq D_1T$ *i.e.,* S_1 is ON and S_2 is OFF is shown in Figure 4.1(c). In this interval, the switch (S_2) is OFF and diode (D_{d2}) is ON. Here, the diode (D_{d2}) is replaced by its equivalent model, *i.e.,* resistance (r_{d2}) in series with forward voltage (v_{fd2}). The input current (i_g) is same as inductor current (i_L). The stored inductive energy appears in series with the input source and contributes to supply the output. The capacitor charged by both inductor and input supply, then discharges through load.

Employing Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL) to the Figure 4.1(c), we get,

$$\begin{aligned}(v_L(t))_{M2} = L\tfrac{di_L(t)}{dt} = -\left((r_g + r_{d2} + r_L + r_{s1}) + \tfrac{Rr_c}{(R+r_c)}\right) i_L(t) - \left(\tfrac{R}{(R+r_c)}\right) v_c(t) \\ +v_g(t) - V_{fd2}\end{aligned} \tag{4.5}$$

$$(i_c(t))_{M2} = C\frac{dv_c(t)}{dt} = i_L(t) - \frac{v_o(t)}{R} \tag{4.6}$$

$$(v_o(t))_{M2} = v_c(t) + r_c i_c(t) \tag{4.7}$$

4.2.3 Mode-III Operation ($D_1T < t < T$)

The equivalent circuit for NIBB converter during interval $D_T < t \leq T$ *i.e.,* S_1 and S_2 are OFF as shown in Figure 4.1(d). In this interval, the switches (S_1 and S_2) are OFF and diodes (D_{d1} and D_{d2}) are ON. Here, both diodes are replaced by its equivalent model, *i.e.,* resistance in series with forward voltage. The input current (i_g) is zero. In this interval, the stored inductive energy contributes to supply the output. The capacitor charges by inductor and then discharges through load.

Using KVL and KCL, the fundamental equations for the circuit shown in Figure 4.1(d) are obtained as follows:

$$(v_L(t))_{M3} = L\frac{di_L(t)}{dt} = -\left((r_{d1} + r_{d2} + r_L) + \frac{Rr_c}{(R+r_c)}\right) i_L(t) - \left(\frac{R}{(R+r_c)}\right) v_c(t) \\ -V_{fd1} - V_{fd2} \tag{4.8}$$

$$(i_c(t))_{M3} = C\frac{dv_c(t)}{dt} = i_L(t) - \frac{v_o(t)}{R} \tag{4.9}$$

$$(v_o(t))_{M3} = v_c(t) + r_c i_c(t) \tag{4.10}$$

4.3 Steady State Analysis

In this context of analysis, voltages and currents are supposed to be constant over a switching period and are illustrated by equilibrium state values as follows:

$$i_L\,(t) = I_L, v_g\,(t) = V_g, v_C\,(t) = V_C$$

According to volt-sec balance [4], in equilibrium state, the average voltage across inductor equal to zero. Therefore, using (4.2), (4.5) and (4.8), we write,

$$V_L = D_2(v_L(t))_{M1} + (D_1 - D_2)(v_L(t))_{M2} + (1 - D_1)(v_L(t))_{M3} = 0 \tag{4.11}$$

Likewise, in equilibrium state, according to charge balance [4], the average current through capacitor equal to zero. Therefore, using (4.3), (4.6) and (4.9), we get,

$$I_C = D_2(i_c(t))_{M1} + (D_1 - D_2)(i_c(t))_{M2} + (1 - D_1)(i_c(t))_{M3} = 0 \tag{4.12}$$

The equilibrium state output voltage is

$$V_o = D_2(v_o(t))_{M1} + (D_1 - D_2)(v_o(t))_{M2} + (1 - D_1)(v_o(t))_{M3} \tag{4.13}$$

Substitute (4.2), (4.5) and (4.8) in (4.11), we get,

$$\begin{aligned} V_L &= D_2\left[-I_L\left(r_{M1}\right) + V_g\right] + \left[D_1 - D_2\right]\left[-I_L\left(r_{M2}\right) - \tfrac{RV_C}{R+r_C} - V_{fd2} + Vg\right] \\ &+ \left[1 - D_1\right]\left[-I_L\left(r_{M3}\right) - V_{fd1} - V_{fd2} - \tfrac{RV_C}{R+r_C}\right] = 0 \end{aligned}$$

$$\Rightarrow \frac{RV_C}{R + r_C} = \frac{D_1V_g - D_1^{'}V_{fd1} - D_2^{'}V_{fd2} - I_L\left[D_2r_{M1} + \left(D_1 - D_2\right)r_{M2} + D_1^{'}r_{M3}\right]}{D_2^{'}} \tag{4.14}$$

where,

$r_{M1} = r_g + r_{s1} + r_L + r_{s2}, r_{M2} = r_g + r_{s1} + r_L + r_{d2} + R \parallel r_C, r_{M3} = r_L + r_{d1} + r_{d2} + R \parallel r_C.$

Substitute (4.3), (4.6) and(4.9) in (4.12), we get,

$$I_C = D_2\left[-\frac{V_o}{R}\right] + \left[D_1 - D_2\right]\left[I_L - \frac{V_o}{R}\right] + \left[1 - D_1\right]\left[I_L - \frac{V_o}{R}\right] = 0$$

$$\Rightarrow I_L = \frac{V_o}{RD_2^{'}} = \frac{I_o}{D_2^{'}}. \tag{4.15}$$

Here, I_o is the steady-state value of load current. Substitute (4.4), (4.7), (4.10) in (4.13), we get,

$$\begin{aligned} V_o &= D_2\left[V_C + I_Cr_C\right] + \left[D_1 - D_2\right]\left[V_C + I_Cr_C\right] + \left[1 - D_1\right]\left[V_C + I_Cr_C\right] \\ &\Rightarrow V_o = V_C \end{aligned} \tag{4.16}$$

4.3.1 Output voltage expression

Substitute (4.15) and (4.16) in (4.14), we get,

$$\Rightarrow \frac{RV_o}{R + r_C} = \frac{D_1V_g - D_1^{'}V_{fd1} - D_2^{'}V_{fd2} - \frac{V_o}{RD_2^{'}}\left[D_2r_{M1} + \left(D_1 - D_2\right)r_{M2} + D_1^{'}r_{M3}\right]}{D_2^{'}} \tag{4.17}$$

$$\Rightarrow V_o\left[\frac{\left(RD_2^{'}\right)^2 - D_2r_{M1} - \left(D_1 - D_2\right)r_{M2} - D_1^{'}r_{M3}}{D_2^{'}R\left(R + r_C\right)}\right] = D_2V_g - D_1^{'}V_{fd1} - D_2^{'}V_{fd2}$$

Finally, we get output voltage expression as

$$V_o = \frac{D_2^{'} R \left(R + r_c\right) \left[D_1 V_g - D_1^{'} V_{fd1} - D_2^{'} V_{fd2}\right]}{\left(D_2 \left(r_{M1} - r_{M2}\right) + D_1 \left(r_{M2} - r_{M3}\right) + r_{M3}\right) \left(R + r_c\right) + \left(\left(1 - D_2\right) R\right)^2} \tag{4.18}$$

If we operate converter in buck mode ($D_2 = 0$) of operation, then the output voltage of converter will be

$$V_{obuck} = \frac{R \left(R + r_c\right) \left[D_1 V_g - \left(1 - D_1\right) V_{fd1} - V_{fd2}\right]}{\left[D_1 \left(r_1 - r_3\right) + r_3\right] \left(R + r_c\right) + R^2} \tag{4.19}$$

If we operate converter in boost mode ($D_1 = 1$) of operation, then the output voltage of converter will be

$$V_{oboost} = \frac{\left(1 - D_2\right) R \left(R + r_c\right) \left[V_g - \left(1 - D_2\right) V_{fd2}\right]}{\left(D_2 \left(r_1 - r_2\right) + r_1\right) \left(R + r_c\right) + \left(\left(1 - D_2\right) R\right)^2} \tag{4.20}$$

This is the expression for non-ideal boost converter as given in (2.17). In order to get the single switch buck-boost ($D_1 = D_2 = D$) operation, then the output voltage of converter will be

$$V_{obuck-boost} = \frac{D^{'} R \left(R + r_c\right) \left[D V_g - D^{'} \left(V_{fd1} + V_{fd2}\right)\right]}{\left[D \left(2 r_1 - r_2\right) + D^{'} r_3\right] \left(R + r_c\right) + \left(D^{'} R\right)^2} \tag{4.21}$$

The analysis of output voltage to duty cycle can be done in similar way to previous chapters. Thus, this analysis will be the same, since it can be operated in buck, boost and buck-boost modes.

If all parasitics are zero in (4.18), then we obtain the ideal formula for calculating the output voltage of non-inverting buck-boost converter as given in (4.1). In an ideal PWM DC-DC NIBB converter, the output voltage is a function of duty cycles and input voltage only. However, by including non-idealities, the output voltage V_o of PWM DC-DC NIBB converter is not only function of duty cycles D_1, D_2 and input voltage V_g but also the load resistance R and other parasitic elements, which is shown in Eq. (4.18).

The plot of output voltage V_o as a function of duty cycles D_1, D_2 is shown in Figure 4.2 for non-ideal case at different load resistances (R) and other parameters are constant. In general for ideal case, the converter output voltage increases with duty cycles in boost and buck-boost conditions. On the other hand, for the non-ideal case,

Table 4.2: Parameters of DC-DC NIBB converter

Parameters	Value
Input voltage (V_g)	12V
Output voltage (V_o)	15V
Source resistance (r_g)	0.3 Ω
Inductor (L/r_L)	500 μH/ 0.34Ω
Capacitor (C/r_c)	160 μF/ 0.12Ω
Diode forward drop (V_{fd1}, V_{fd2})	0.5V
Diode resistance (r_{d1}, r_{d2})	0.03 Ω
Switch resistance (r_{s1}, r_{s2})	0.05 Ω
Switching frequency (f)	20KHz
Load resistance (R)	22Ω/100 W

the output voltage first increases with duty cycles, reaches its maximum value, and then decreases to zero at duty cycles close to unity. Here, it is clear that the output voltage depends on load resistance, whereas it is not the case in ideal case. The difference from the ideal to non-ideal is because of the increased voltage drop across the non-idealities in practical NIBB converter at lower load resistance (or higher load current).

The plot of output voltage V_o as a function of duty cycle D is shown in Figure 4.3 for NIBB converter at different input voltages (V_g) and other parameters are constant. For a particular duty cycle, the difference between the output voltage of converter becomes larger as input voltage increases. So in the presence of parasitics, switches should kept ON for long time to get the same output voltage. As the input voltage decreases, V_{omax} also decreasing.

The plot of input voltage V_g as a function of duty cycles D_1 & D_2 is shown in Figure 4.4 for NIBB converter at different output voltages (V_o) and other parameters are constant. As the input voltage decreases, the duty cycles required to keep switch ON also increases and reaches a point where no duty cycle combination will achieve

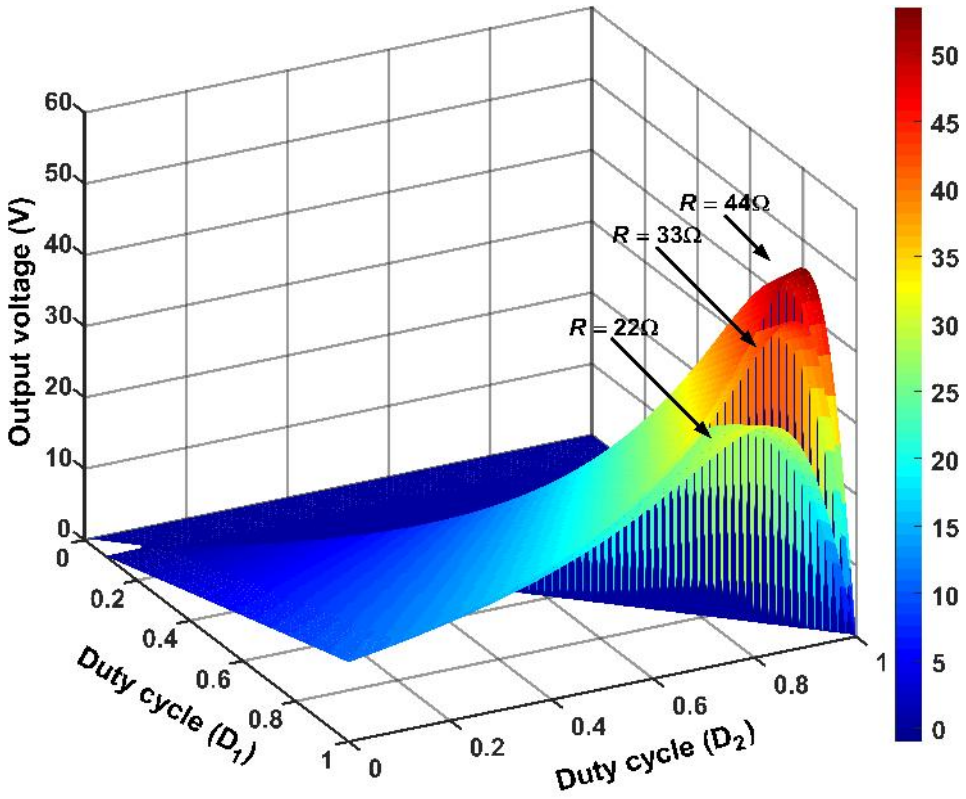


Figure 4.2: Output voltage vs Duty cycle at different load resistances.

the required output voltage value. This input voltage value is considered as the lower limit of the NIBB converter operation for given specifications. From this, we get the information of minimum input voltage (V_{gmin}) to be applied for converter at fixed output voltage (in regulator problems).

4.3.2 Modified duty cycle expression

It is easily noticeable that the output voltage of a non-ideal NIBB converter (*i.e.,* practical) is always less than the ideal NIBB converter. Since, the relation for an ideal case, which neglects the parasitics present in practical buck-boost converter. So, there is a need to develop the improved expression for duty cycles. But, there are two duty cycles for NIBB converter, compared to other basic converters. So, here with different combinations of duty cycles, same voltage can be achieved. So, in order to derive modified expression for duty cycles, first fix one duty cycle and then derive expression for other duty cycle and vice versa.

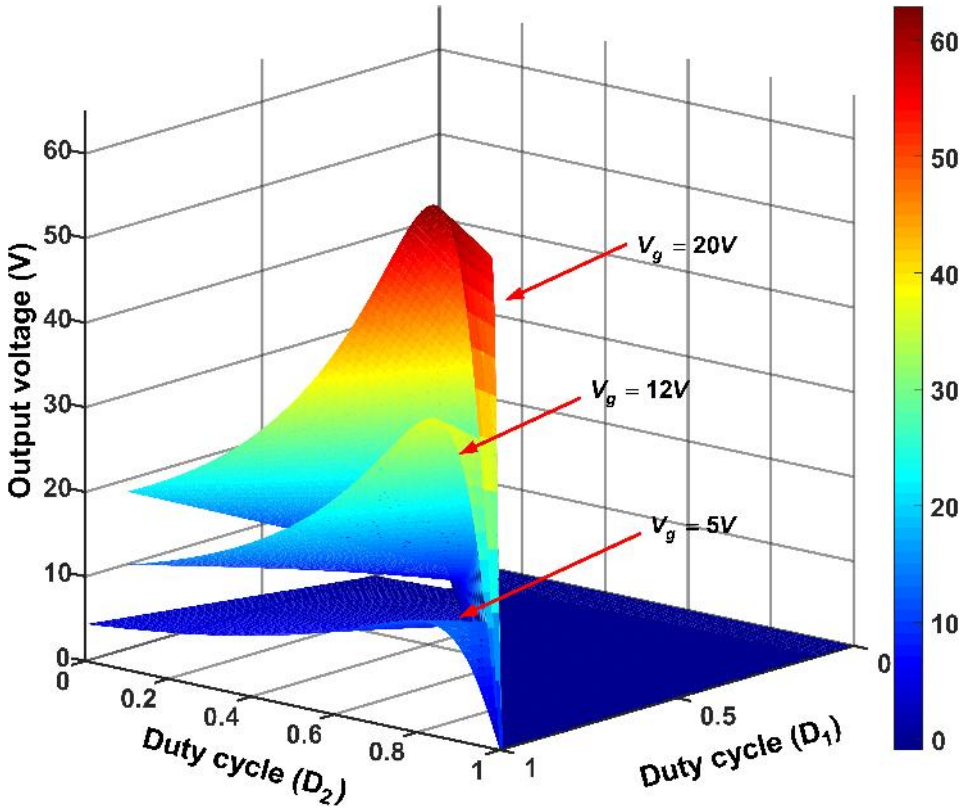


Figure 4.3: Output voltage vs Duty cycle at different input voltages.

Case I:

First, we will fix D_1 as constant and derivation for D_2 as follows:

Rewriting (4.18),

$$\frac{RV_o}{R+r_C} = \frac{D_2' \left[R\left(D_1V_g - D_1'V_{fd1}\right) + V_o\left(r_1 - r_2\right)\right] - \left(D_2'\right)^2 RV_{fd2} - V_o\left[D_1'\left(r_{M3} - r_{M2}\right) + r_{M1}\right]}{R\left(D_2'\right)^2} \tag{4.22}$$

Further, it can be expressed as quadratic equation in terms of (D_2' or $1 - D_2$) written as follows:

$$\left(D_2'\right)^2 \underbrace{\left[R^2V_o + R\left(R + r_C\right)V_{fd2}\right]}_{a} - \left(D_2'\right) \underbrace{\left[R + r_C\right]\left[R\left(D_1V_g - D_1'V_{fd1}\right) + V_o\left(r_{M1} - r_{M2}\right)\right]}_{b}$$
$$+ \underbrace{V_o\left[D_1'\left(r_{M3} - r_{M2}\right) + r_{M1}\right]\left[R + r_C\right]}_{c} = 0 \tag{4.23}$$

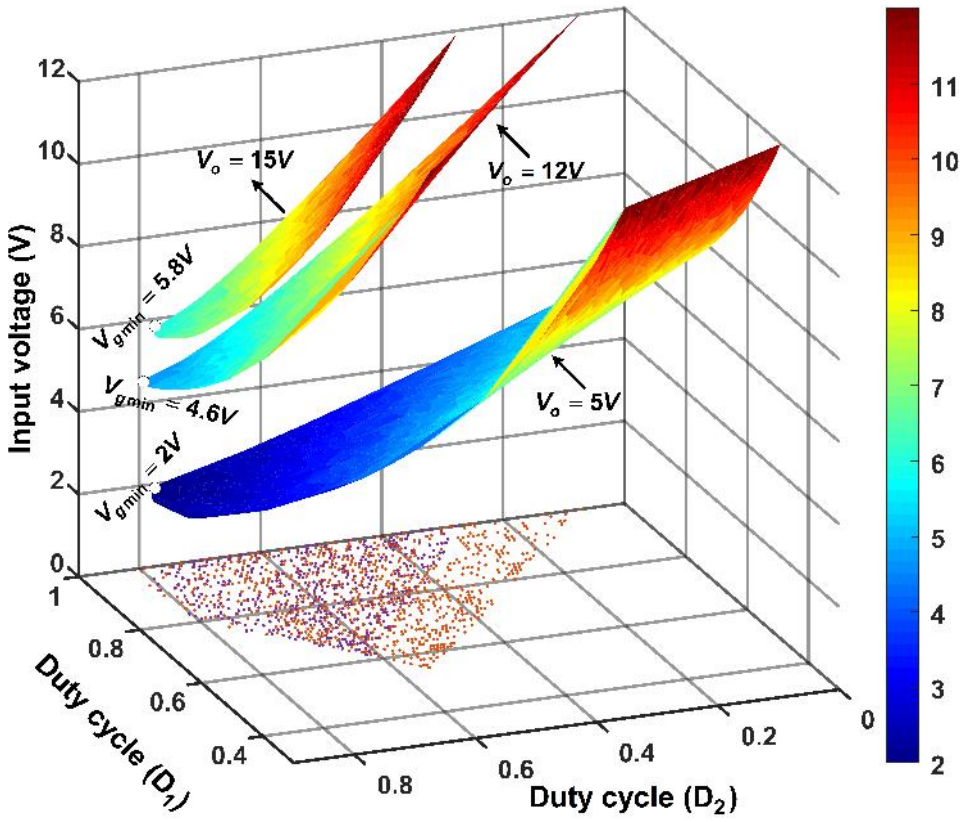


Figure 4.4: Minimum input voltage specification for given parameters.

The solution of above quadratic equation can be determined as,

$$D_2^{'} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{4.24}$$

The practicable or realizable duty cycle falls under positive sign. Here, conditions for operating NIBB converter is that the calculated D_2 cannot be more than the chosen or fixed D_1.

Case II:

Now, we will fix D_2 as constant and derivation for D_1 as follows:

Rewriting (4.18),

$$V_o\left[\left(RD_2^{'}\right)^2 + \left[D_2\left(r_{M1} - r_{M2}\right) + r_{M3}\right]\left(R + r_C\right)\right] + R\left(R + r_C\right)D_2^{'}\left[V_{fd1} + D_2^{'}V_{fd2}\right]$$
$$= D_1\left[R\left(R + r_C\right)D_2^{'}\left(V_g - V_{fd1}\right)\right] - V_o\left(r_{M2} - r_{M3}\right)\left(R + r_C\right) \tag{4.25}$$

Further, it can be written as

$$D_1 = \frac{V_o\left[\left(RD_2^{'}\right)^2 + \left[D_2\left(r_{M1} - r_{M2}\right) + r_{M3}\right]\left(R + r_C\right)\right] + R\left(R + r_C\right)D_2^{'}\left[V_{fd1} + D_2^{'}V_{fd2}\right]}{\left[R\left(R + r_C\right)D_2^{'}\left(V_g + V_{fd1}\right)\right] - V_o\left(r_{M2} - r_{M3}\right)\left(R + r_C\right)} \tag{4.26}$$

Here, conditions for operating NIBB converter is that the calculated D_1 should be more than the chosen or fixed D_2, otherwise increase D_2 and calculate D_1 till we get the condition $D_1 > D_2$.

The possible operating region or feasible duty cycles for the operation of NIBB converter for given specifications (from Table 4.2) is shown in Figure 4.5. This region is obtained by the modified duty cycle expressions given in (4.24) and (4.26). In Figure 4.5, complete triangle ABC refer to ideal case, *i.e.,* all the non-idealities or parasitics set to zero. The shaded part of triangle ABC in Figure 4.5 is feasible duty cycles with the considered parameters. Figure 4.6 shows, the obtainable voltages of NIBB converter. In Figure 4.6, voltage surfaces shown at different load values.

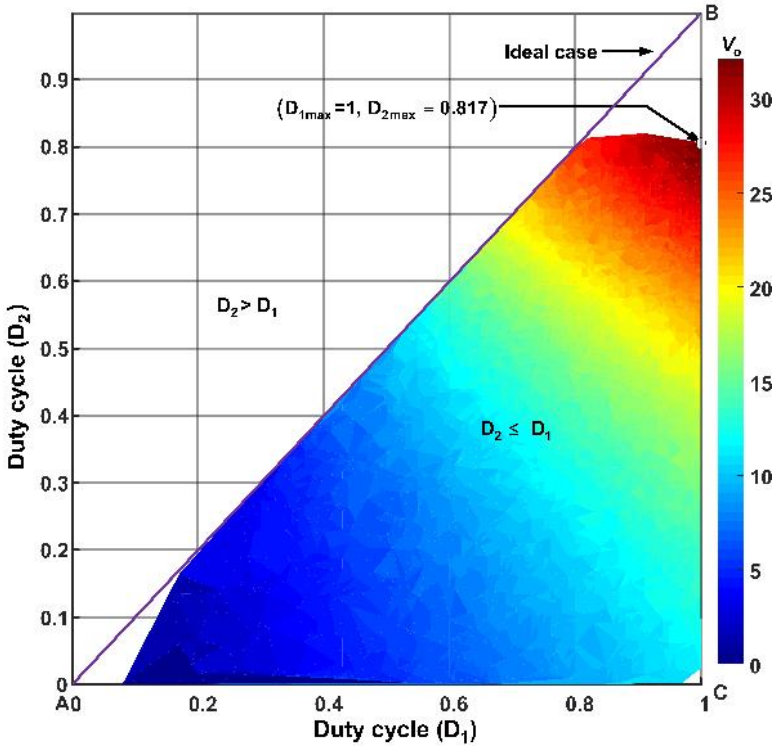


Figure 4.5: Possible operating region of NIBB converter.

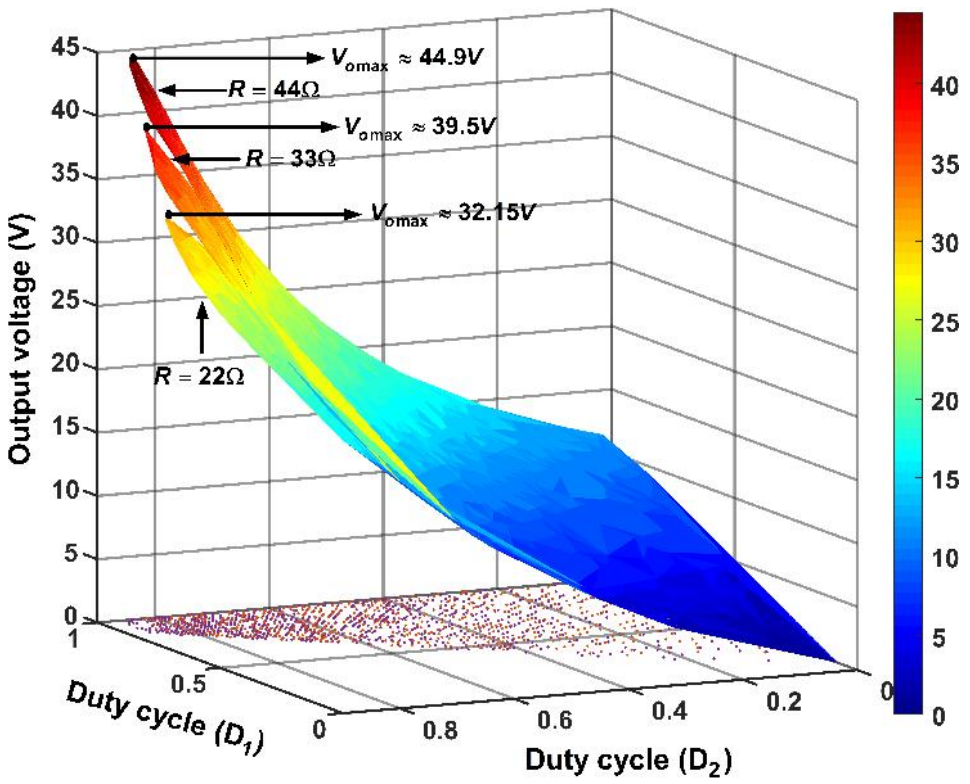


Figure 4.6: Maximum achievable output voltages with the given specifications.

4.3.3 Maximum achievable duty cycle and output voltage

Generally, the buck mode of operation in NIBB converter will not have any limits on duty cycle and output voltage. NIBB converter operation is mainly limited by duty cycle, when it operates in boost and buck-boost modes. The maximum achievable voltage will be at ($D_{1\max}$ & $D_{2\max}$) and depends on mode of operation. This is also clear from Figure 4.2, where it is noticed that, as the load resistance increasing, the maximum value of output voltage V_{omax} is increasing and corresponding duty cycles $D_{1\max}$ & $D_{2\max}$ are also increasing. So, here we obtain the expressions for maximum achievable duty cycle and output voltage of the NIBB converter for the given specifications.

In order to get maximum achievable duty cycle, rewriting eq. (4.18) as,

$$V_o = \frac{D_2^{'} R \left(R + r_c\right) \left[D_1 V_g - D_1^{'} V_{fd1} - D_2^{'} V_{fd2}\right]}{\left(D_2 \left(r_{M1} - r_{M2}\right) + D_1 \left(r_{M2} - r_{M3}\right) + r_{M3}\right) \left(R + r_c\right) + \left(\left(1 - D_2\right) R\right)^2}$$

From this expression and operation of converter ($D_2 < D_1$) suggests that it has

different operational limits or maximum value of duty cycle ($D_{2\max}$) depending on the value of D_1, which means D_2 can be maximum equal to D_1. But, this is true only up to certain value of D_1, thereafter the maximum value of D_2 changes. Hence, here we find the maximum value of duty cycle ($D_{2\max}$) corresponding to the D_1. This will be the maximum achievable output voltage of the NIBB converter operating in boost or buck-boost mode.

Now, maximum value of this expression (4.18) can be found as follows:

$$\frac{\partial V_o}{\partial D_2} = 0 \tag{4.27}$$

Therefore, from (4.27), we get the expression of maximum permissible duty cycle ($D_{2\max}$) as follows:

$$a\left(D_2^{'}\right)^2 + b\left(D_2^{'}\right) + c = 0 \tag{4.28}$$

Finally, we get maximum possible duty cycle expression as

$$D_{2\max}^{'} = \frac{-b + \sqrt{b^2 - 4ac}}{2a} \tag{4.29}$$

where,

$$\begin{aligned} a &= R^2\left[D_1 V_g - D_1^{'} V_{fd1}\right] + V_{fd2}\left[r_2 - r_1\right]\left[R + r_c\right]; \\ b &= 2V_{fd2}\left[r_1 - D_1^{'}\left(r_2 - r_3\right)\right]\left[R + r_c\right]; \\ c &= -\left[D_1 V_g - D_1^{'} V_{fd1}\right]\left[r_1 - D_1^{'}\left(r_2 - r_3\right)\right]\left[R + r_c\right]. \end{aligned} \tag{4.30}$$

From output voltage expression and overall operation of NIBB converter, the maximum voltage occurs at $D_{1\max} = 1$ and $D_2 = D_{2\max}$. The maximum achievable voltage of the converter will be

$$V_{o\max}|_{(D_{1\max}, D_{2\max})} = \frac{\left(1 - D_{2\max}\right) R\left(R + r_c\right)\left(V_g - \left(1 - D_{2\max}\right) V_{fd2}\right)}{\left(D_{2\max}\left(r_1 - r_2\right) + r_1\right)\left(R + r_c\right) + \left(\left(1 - D_{2\max}\right) R\right)^2} \tag{4.31}$$

The operational limits of D_1 and D_2 are shown in Figure 4.5 for given specifications. The maximum achievable duty cycles and corresponding voltages are also mentioned. Further, in Figure 4.6, the maximum achievable voltage at different load values also indicated.

4.4 Outcomes from Steady State Analysis

Here, from this analysis, we summarized some important observations, which are handy in a closed-loop operation, as given below:

1. Practical NIBB converter system always has lower output voltage compared to ideal case. So, in order to get the similar value in practical as well as theory, the derived expression (4.24) and (4.26) are essential.

2. Maximum achievable duty cycles ($D_{1\,\max}$ & $D_{2\,\max}$) and maximum output voltage (V_{omax}) are two crucial parameters to know for before the closed-loop operation of converter. These are the maximum possible values in overall operation.

3. Since the parasitics effect on output voltage, it is not possible to get the full output value in conventional buck converter. Whereas, this is possible through NIBB converter. In boost and buck-boost modes of operation, sudden changes in load or input may lead to collapse of output. This can be avoided by adding limiter ($= D_{1\,\max}$ or $= D_{2\,\max}$) at the controller output as shown in Figure 4.7.

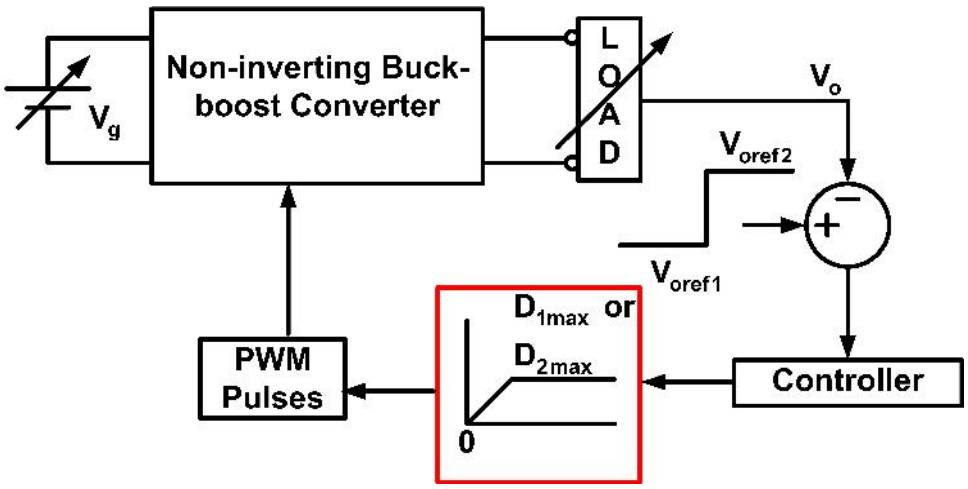


Figure 4.7: Closed loop operation.

4. From the analysis, it can be observed that each parasitic element effects the maximum achievable duty cycles ($D_{1,max}$ & $D_{2,max}$) and V_{omax}.

5. By this analysis, the key information of input voltage range specification V_{gmin} of the converter is observed at a constant output voltage. This can be observed from Figure 4.4.

4.5 Design of Filter Elements

4.5.1 Inductor current ripple (ICR) and Inductor design

Design of inductor is an another important issue for NIBB converter compared to other single switch converter. As NIBB converter operated in three modes, inductance required is calculated in all modes and finally the worst case value is chosen for operation. Generally, inductance value mostly depends on the ICR and switching frequency. In this section, the effect of non-idealities is analysed on inductors design and inductor ripple current. Let x_L be inductor current ripple factor (ICRF) for inductors L, such that $\Delta i_L = x_L I_L$.

For Mode-I of operation, $\Delta t = D_2 T$, the steady state magnitude of ripple current Δi_L can be written as

$$\Delta i_L = \left[\frac{V_g}{L} - \frac{I_L\left(r_g + r_L + r_{s1} + r_{s2}\right)}{L}\right] D_2 T \tag{4.32}$$

Substituting value of I_L from (4.15) and simplifying

$$\Delta i_L = \frac{D_2 V_o}{Lf}\left[\frac{V_g}{V_o} - \frac{r_g + r_L + r_{s1} + r_{s2}}{RD_2'}\right] \tag{4.33}$$

Here $f = \frac{1}{T}$ is the switching frequency.

Eq. (4.18) can be written as

$$\frac{V_g}{V_o} = \frac{\left(D_2\left(r_1 - r_2\right) + D_1\left(r_2 - r_3\right) + r_3\right)\left(R + r_c\right) + \left(D_2' R\right)^2}{D_1 D_2' R\left(R + r_c\right)} + \frac{D_1' V_{fd1} + D_2' V_{fd2}}{D_1 V_o} \tag{4.34}$$

Now using equation (4.34), eq. (4.33) is simplified further and the expression of inductor ripple current Δi_L is obtained in final form as follows:

$$\Delta i_L = \frac{D_2 D_2' V_o}{D_1 L f}\left[\frac{[D_2(r_1-r_2)+D_1(r_2-r_1-r_3)+r_3](R+r_c)+\left[D_2' R\right]^2}{\left(D_2'\right)^2 R(R+r_c)} + \frac{D_1' V_{fd1}+D_2' V_{fd2}}{D_2' V_o}\right] \tag{4.35}$$

or

$$\Delta i_L = \Delta i_{Lideal} \left[\frac{[D_2(r_1-r_2)+D_1(r_2-r_1-r_3)+r_3](R+r_c)+\left[D_2'R\right]^2}{\left(D_2'\right)^2 R(R+r_c)} + \frac{D_1'V_{fd1}+D_2'V_{fd2}}{D_2'V_o} \right] \tag{4.36}$$

From this, the inductance can be calculated as

$$L_{MI} = \frac{D_2 D_2' V_o}{D_1 \Delta i_L f} \left[\frac{[D_2(r_1-r_2)+D_1(r_2-r_1-r_3)+r_3](R+r_c)+\left[D_2'R\right]^2}{\left(D_2'\right)^2 R(R+r_c)} + \frac{D_1'V_{fd1}+D_2'V_{fd2}}{D_2'V_o} \right] \tag{4.37}$$

or

$$L_{MI} = L_{MIideal} \left[\frac{[D_2(r_1-r_2)+D_1(r_2-r_1-r_3)+r_3](R+r_c)+\left[D_2'R\right]^2}{\left(D_2'\right)^2 R(R+r_c)} + \frac{D_1'V_{fd1}+D_2'V_{fd2}}{D_2'V_o} \right] \tag{4.38}$$

For Mode-II of operation, $\Delta t = (D_1 - D_2)\,T$, the steady state magnitude of ripple current Δi_L can be written as

$$\Delta i_L = \left[\frac{V_g - V_{fd2}}{L} - \frac{RV_o}{R+r_C} - \frac{I_L r_2}{L} \right] (D_1 - D_2)\,T \tag{4.39}$$

Substituting value of I_L from (4.15) and simplifying

$$\Delta i_L = \frac{(D_1 - D_2)\,V_o}{Lf} \left[\frac{V_g}{V_o} - \frac{V_{fd2}}{V_o} - \frac{R}{R+r_C} - \frac{r_2}{RD_2'} \right] \tag{4.40}$$

Now using equation (4.34), eq. (4.40) is simplified further and the expression of inductor ripple current Δi_L is obtained in final form as follows:

$$\Delta i_L = \frac{\left(D_1 D_1' - D_2 D_2'\right) V_o}{D_1 L f} \left[\begin{array}{l} \frac{\left[D_2(r_1-r_2)+D_1'r_3\right](R+r_c)+\left(D_2'R\right)^2}{(D_1+D_2)' D_2' R(R+r_c)} \\ +\frac{D_1'V_{fd1}+(D_1+D_2)'V_{fd2}}{(D_1+D_2)'V_o} - \frac{D_1 R}{(D_1+D_2)'(R+r_c)} \end{array} \right] \tag{4.41}$$

or

$$\Delta i_L = \Delta i_{Lideal} \left[\begin{array}{l} \frac{\left[D_2(r_1-r_2)+D_1'r_3\right](R+r_c)+\left(D_2'R\right)^2}{(D_1+D_2)' D_2' R(R+r_c)} \\ +\frac{D_1'V_{fd1}+(D_1+D_2)'V_{fd2}}{(D_1+D_2)'V_o} - \frac{D_1 R}{(D_1+D_2)'(R+r_c)} \end{array} \right] \tag{4.42}$$

From this, the inductance can be calculated as

$$L_{MII} = \frac{\left(D_1 D_1' - D_2 D_2'\right) V_o}{D_1 \Delta i_L f} \left[\begin{array}{l} \frac{\left[D_2(r_1-r_2)+D_1'r_3\right](R+r_c)+\left(D_2'R\right)^2}{(D_1+D_2)' D_2' R(R+r_c)} \\ +\frac{D_1'V_{fd1}+(D_1+D_2)'V_{fd2}}{(D_1+D_2)'V_o} - \frac{D_1 R}{(D_1+D_2)'(R+r_c)} \end{array} \right] \tag{4.43}$$

or

$$L_{MII} = L_{MIIideal} \left[\begin{array}{l} \frac{\left[D_2(r_1-r_2)+D_1'r_3\right](R+r_c)+\left(D_2'R\right)^2}{(D_1+D_2)' D_2' R(R+r_c)} \\ +\frac{D_1'V_{fd1}+(D_1+D_2)'V_{fd2}}{(D_1+D_2)'V_o} - \frac{D_1 R}{(D_1+D_2)'(R+r_c)} \end{array} \right] \tag{4.44}$$

For Mode-III of operation, $\Delta t = (1 - D_1)\,T$, the steady state magnitude of ripple current Δi_L can be written as

$$\Delta i_L = \left[\frac{-V_{fd1} - V_{fd2}}{L} - \frac{RV_o}{L\,(R + r_C)} - \frac{I_L r_3}{L}\right] D_1' T \tag{4.45}$$

Substituting value of I_L from (4.15) and simplifying

$$\Delta i_L = \frac{D_1' V_o}{Lf}\left[-\frac{V_{fd1} + V_{fd2}}{V_o} - \frac{R}{R + r_C} - \frac{r_3}{RD_2'}\right] \tag{4.46}$$

or

$$\Delta i_L = \Delta i_{Lideal}\left[-\frac{V_{fd1} + V_{fd2}}{V_o} - \frac{R}{R + r_C} - \frac{r_3}{RD_2'}\right] \tag{4.47}$$

From this, the inductance can be calculated as

$$L_{MIII} = \frac{D_1' V_o}{\Delta i_L f}\left[-\frac{R}{R + r_C} - \frac{V_{fd1} + V_{fd2}}{V_o} - \frac{r_L + r_{d1} + r_{d2}}{RD_2'}\right] \tag{4.48}$$

or

$$L_{MIII} = L_{MIIIideal}\left[-\frac{R}{R + r_C} - \frac{V_{fd1} + V_{fd2}}{V_o} - \frac{r_L + r_{d1} + r_{d2}}{RD_2'}\right] \tag{4.49}$$

Now, the final inductance for the operation of converter is selected as follows:

$$\mathrm{L} = \mathrm{Max}\left\{\mathrm{L_{MI}}, \mathrm{L_{MII}}, \mathrm{L_{MIII}}\right\} \tag{4.50}$$

The expressions (4.37), (4.43) and (4.48) shows that there is a additional multiplying factor to the ideal expressions. Here, an important observation from non-ideal design is that the value of inductance and ICR are mainly effected by the ESR of the capacitor though there are other parasitics also present. From these expressions, it is observed that as the capacitor ESR increases, the ICR increases and the inductance required also increases.

4.5.2 Design of Capacitor

Capacitor design is also the very important aspect. So, the capacitor design for NIBB converter is derived in this section. The capacitor design depends on the allowable OVR and switching frequency. The equivalent series resistance (ESR) of a capacitor plays an important role in design. A capacitor is modelled by its capacitance and ESR values. In order to design capacitance, the OVR analysis of capacitor is needed.

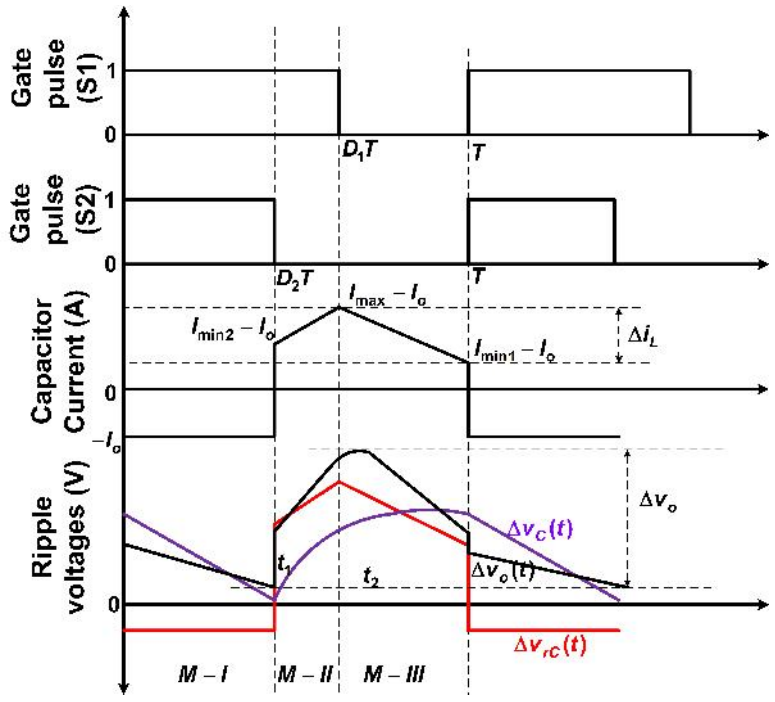


Figure 4.8: Current and ripple voltage waveforms associated with capacitor C in boost and buck-boost modes.

4.5.2.1 OVR analysis

In any DC-DC converter, the total voltage ripple (Δv_o) of a capacitor is sum of

- Voltage ripples due to its own capacitance (Δv_C)
- Voltage ripples due to its ESR (Δv_{rC}).

Therefore, for proper capacitor design, it becomes necessary to consider the effect of ESR. The capacitor C is used as filter capacitor at output stage. The voltage ripples across this capacitor directly affect the quality of output voltage. Therefore, its design is carried out more carefully to limit the output voltage ripples within permissible range.

The capacitor current and different components of voltage ripples in steady state are shown in Figure 4.8. As discussed earlier, output voltage ripple $\Delta v_o(t)$ is made

up of two components as

$$\Delta v_o(t) \simeq \Delta v_C(t) + \Delta v_{rC}(t) \tag{4.51}$$

Voltage ripples due to ESR, $\Delta v_{rC}(t)$, expressed as

$$\Delta v_{rC}\left(t\right) = r_c i_C\left(t\right) \tag{4.52}$$

Voltage ripples due to capacitor, $\Delta v_C(t)$ expressed as

$$\Delta v_C\left(t\right) = \frac{1}{C}\int_0^t i_C\left(t\right)dt + \Delta v_C\left(t_0\right) \tag{4.53}$$

$\Delta v_C(t_0)$ is initial voltage across capacitor at $t = t_0$.
The NIBB converter can be operated in buck, boost and buck-boost modes. Now, we will derive in detail for each mode which is given below:

A. Buck-boost mode:

To operate NIBB converter in buck-boost mode *i.e.,* $D_1 = 0 - 1$ and D_2 varies from 0 to $< D_1$. Most importantly, the condition is $D_2 < D_1$. The detailed analysis is carried out as follows:

4.5.2.2 Analysis during Mode I

The current through capacitor C is

$$i_c(t) = -I_o \tag{4.54}$$

Therefore, the voltage ripple contribution due to capacitor ESR is

$$\Delta v_{rC}\left(t\right) = r_c i_C\left(t\right) = -I_o r_c \tag{4.55}$$

The voltage ripple contribution due to capacitor itself is

$$\Delta v_C\left(t\right) = \frac{1}{C}\int_0^t i_C\left(t\right)dt + \Delta v_C\left(0\right) = -\frac{I_o}{C}t + \Delta v_C\left(0\right) \tag{4.56}$$

$\Delta v_C(0)$ is initial voltage across capacitor at $t = 0$. Therefore, total output voltage ripple during M-I period is

$$\Delta v_o\left(t\right) = \Delta v_C\left(t\right) + \Delta v_{rC}\left(t\right) = -\frac{I_o}{C}\left[t + Cr_c\right] + \Delta v_C\left(0\right) \tag{4.57}$$

From Eq. (4.57), it is clear that $\Delta v_o(t)$ is a line equation which is shown in Figure 4.8 also. It has a minimum value at $t_1 = D_2T$. At $t = t_1$, the voltage ripples obtained as

$$\Delta v_{rc}(t_1) = -I_o r_c \tag{4.58}$$

$$\Delta v_C(t_1) = -\frac{I_o D_2 T}{C} + \Delta v_C(0) \tag{4.59}$$

$$\Delta v_{o,\min} = \Delta v_o\left(t_1\right) = -\frac{I_o}{C}\left[C r_c + D_2 T\right] + \Delta v_C\left(0\right) \tag{4.60}$$

4.5.2.3 Analysis during Mode II

In this duration, the capacitor current dynamics is

$$i_C(t) = \frac{I_{\max} - I_{\min 2}}{\left(D_1 - D_2\right) T}\left[t - D_2 T\right] + I_{\min 2} - I_o \tag{4.61}$$

Therefore, the voltage ripple contribution due to capacitor ESR is

$$\Delta v_{rC}(t) = r_C i_C(t) = \frac{\left(I_{\max} - I_{\min 2}\right) r_C}{\left(D_1 - D_2\right) T}\left[t - D_2 T\right] + \left(I_{\min 2} - I_o\right) r_C \tag{4.62}$$

The voltage ripple contribution due to capacitor itself is

$$\begin{gathered}\Delta v_C(t) = \frac{1}{C}\int_{D_2T}^{t} i_C(t)dt + \Delta v_C(D_2T) = \frac{I_{\max}-I_{\min 2}}{2C(D_1-D_2)T}\left[t - D_2T\right]^2 \\ + \frac{I_{\min 2}-I_o}{C}\left[t - D_2T\right] + \Delta v_C(D_2T)\end{gathered} \tag{4.63}$$

$\Delta v_C(D_2T)$ is initial voltage across capacitor at $t = D_2T$.

Therefore, total output voltage ripple during switch-off is

$$\begin{gathered}\Delta v_o\left(t\right) = \Delta v_C\left(t\right) + \Delta v_{rC}\left(t\right) = \frac{I_{\max}-I_{\min 2}}{(D_1-D_2)T}\left[\frac{(t-D_2T)^2}{2C} + r_c\left(t - D_2T\right)\right] + \\ \frac{(I_{\min 2}-I_o)}{C}\left(Cr_c + (t - D_2T)\right) + \Delta v_C\left(D_2T\right)\end{gathered} \tag{4.64}$$

From Figure 4.8, it is clear that there is no maximum or minimum of the wave form. But Eq. (4.63) can be used to determine the value of $\Delta v_C(D_1T)$.

$$\Delta v_C(D_1T) = \frac{I_{\max} - I_{\min 2}}{2C}\left[D_1 - D_2\right]T + \frac{I_{\min 2} - I_o}{C}\left[D_1 - D_2\right]T + \Delta v_C(D_2T) \tag{4.65}$$

4.5.2.4 Analysis during Mode III

In this duration, the capacitor current dynamics is

$$i_C(t) = \frac{-(I_{\max} - I_{\min 1})(t - D_1 T)}{D_1' T} + I_{max} - I_o \tag{4.66}$$

Therefore, the voltage ripple contribution due to capacitor ESR is

$$\Delta v_{rC}(t) = r_c i_C(t) = -\frac{(I_{\max} - I_{\min 1}) r_c}{D_1' T}(t - D_1 T) + (I_{max} - I_o) r_c \tag{4.67}$$

The voltage ripple contribution due to capacitor itself is

$$\Delta v_C(t) = \frac{1}{C}\int_{D_1 T}^{t} i_C(t)dt + \Delta v_C(D_1 T) = -\frac{(I_{\max} - I_{\min 1})(t - D_1 T)^2}{2CD_1' T} + \frac{(I_{max} - I_o)(t - D_1 T)}{C} + \Delta v_C(D_1 T) \tag{4.68}$$

$\Delta v_C(D_1 T)$ is initial voltage across capacitor at $t = D_1 T$.

Therefore, total output voltage ripple during switch-off is

$$\begin{gathered}\Delta v_o(t) = \Delta v_C(t) + \Delta v_{rC}(t) = -\frac{(I_{\max} - I_{\min 1})}{D_1' T}\left[\frac{(t - D_1 T)^2}{2C} + r_c(t - D_1 T)\right] + \\ \frac{(I_{max} - I_o)}{C}(Cr_c + (t - D_1 T)) + \Delta v_C(D_1 T)\end{gathered} \tag{4.69}$$

The time t_2 at which value of $\Delta v_o(t)$ occurs maximum during switch-off is given by

$$t_2 = D_1 T - Cr_c + \frac{(I_{max} - I_o)}{(I_{\max} - I_{\min 1})} D_1' T \tag{4.70}$$

$$\Delta v_{rc}(t_2) = \frac{(I_{\max} - I_{\min 1})(Cr_c^2)}{CD_1' T} \tag{4.71}$$

$$\Delta v_C(t_2) = \frac{(I_{max} - I_o)^2 D_1' T}{2C(I_{\max} - I_{\min 1})} - \frac{(I_{\max} - I_{\min 1})(Cr_c^2)}{2CD_1' T} + \Delta v_C(D_1 T) \tag{4.72}$$

and the maximum value of output voltage ripples are obtained as

$$\Delta v_{o,\max} = \Delta v_o(t_2) = \frac{(I_{\max} - I_{\min 1})}{2CD_1' T}\left(\left((I_{max} - I_o)\frac{D_1' T}{(I_{\max} - I_{\min 1})}\right)^2 + (Cr_c)^2\right) + \Delta v_C(D_1 T) \tag{4.73}$$

Therefore, the total peak-to-peak voltage ripple will be

$$\Delta v_o = \Delta v_o(t_2) - \Delta v_o(t_1) \tag{4.74}$$

Substituting from (4.60) and (4.73), we get

$$\Delta v_o = \frac{(I_{\max}-I_{\min 1})}{2CD_1'T}\left[\left(\frac{I_{\max}-I_o}{I_{\max}-I_{\min 1}}\right)^2\left(D_1'T\right)^2+(Cr_C)^2\right]+\frac{(I_{\max}+I_{\min 2}-I_o)(D_1-D_2)T}{2C}+I_o r_c \tag{4.75}$$

For buck-boost mode operation, when D_1 is very close to D_2, the later term in (4.75) is very small and observed that it does not effect the value, so this can be written as

$$\Delta v_o = \frac{(I_{\max}-I_{\min 1})}{2CD_1'T}\left[\left(\frac{I_{\max}-I_o}{I_{\max}-I_{\min 1}}\right)^2\left(D_1'T\right)^2+(Cr_C)^2\right]+I_o r_c \tag{4.76}$$

This expression is very similar to buck-boost converter ripple expression in section 3.

B. Boost mode:

To operate NIBB converter in boost mode *i.e.,* $D_1 = 1$ and D_2 varies from 0 to 1. So, the wave forms for this mode will not the same as given in Figure 4.8. The wave form is given in Figure 2.9 and remaining design analysis for this is same as DC-DC boost converter as given in Chapter 2, Section 2.5.2.

C. Buck mode:

To operate NIBB converter in buck mode *i.e.,* $D_2 = 0$ and D_1 varies from 0 to 1. So, the wave forms for this mode will not the same as given in Figure 4.8. The corresponding wave forms for this mode is given in Figure 4.9. Though, this analysis is same as the DC-DC buck converter as given in [44]. This is explained here in brief as follows: From this figure, the operating conditions will be $D_2 = 0$, $I_{\min 1} = I_{\min 2} = I_{\min}$ and $I_o = 0$. So, we have only Mode II and Mode III. The equations for Mode II can be written as

$$i_C(t) = \frac{\Delta i_L}{(D_1)\,T}t - \frac{\Delta i_L}{2} \tag{4.77}$$

$$\Delta v_{rC}(t) = \frac{\Delta i_L r_C}{(D_1)\,T}t - \frac{\Delta i_L r_C}{2} \tag{4.78}$$

$$\Delta v_C(t) = \frac{\Delta i_L t}{2C}\left[\frac{t}{D_1 T}-1\right]+\Delta v_C(0) \tag{4.79}$$

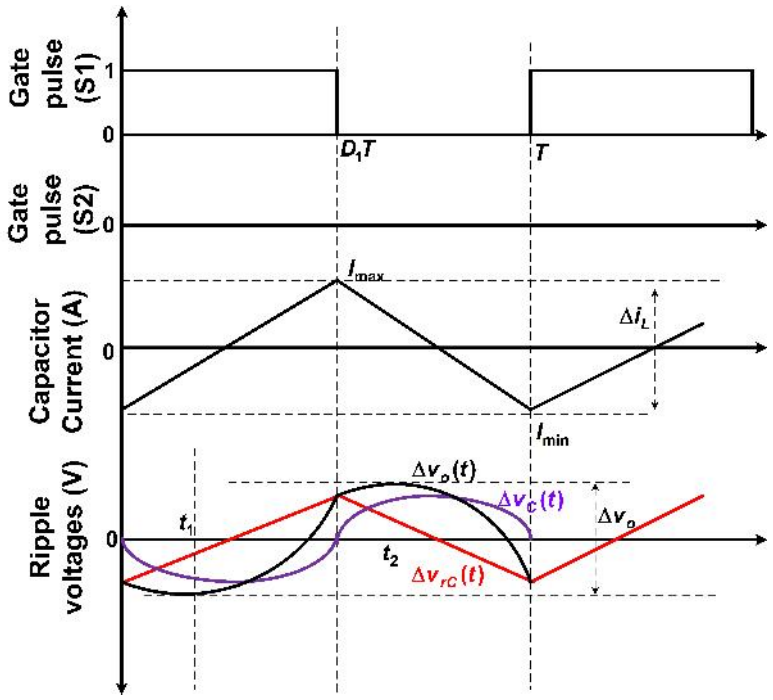


Figure 4.9: Current and ripple voltage waveforms associated with capacitor C in buck mode.

$$\Delta v_o(t) = \Delta i_L r_C \left[\frac{t}{D_1 T} - \frac{1}{2}\right] + \frac{\Delta i_L t}{2C}\left[\frac{t}{D_1 T} - 1\right] + \Delta v_c(0) \tag{4.80}$$

In this period (*i.e.,* Mode II) only, it has minimum ripple value. So, differentiate (4.80) and equate to zero, we get t_1 as

$$t_1 = \frac{D_1 T}{2} - C r_C \tag{4.81}$$

Substituting (4.81) in (4.80) (*i.e.,*$t = t_1$), we get the minimum ripple as

$$\Delta v_{o,\min} = \Delta v_o(t_1) = -\Delta i_L \left[\frac{D_1 T}{8C} + \frac{C r_C^2}{2 D_1 T}\right] + \Delta v_c(0) \tag{4.82}$$

Now, from Figure 4.9, the equations for Mode III can be written as

$$i_C\left(t\right) = \frac{-\Delta i_L \left(t - D_1 T\right)}{D_1' T} + \frac{\Delta i_L}{2} \tag{4.83}$$

$$\Delta v_{rC}\left(t\right) = \frac{-\Delta i_L r_C \left(t - D_1 T\right)}{D_1' T} + \frac{\Delta i_L r_C}{2} \tag{4.84}$$

$$\Delta v_C\left(t\right) = -\frac{\Delta i_L (t-D_1T)^2}{2CD_1'T} + \frac{\Delta i_L (t-D_1T)}{C} + \Delta v_C\left(D_1T\right) \tag{4.85}$$

$$\Delta v_o\left(t\right) = -\frac{\Delta i_L}{D_1'T}\left[\frac{(t-D_1T)^2}{2C} + r_c\left(t-D_1T\right)\right] + \frac{\Delta i_L}{C}\left(Cr_c + (t-D_1T)\right) + \Delta v_C\left(D_1T\right) \tag{4.86}$$

In this period (*i.e.,* Mode III) only, it has maximum ripple value. So, differentiate (4.86) and equate to zero, we get t_2 as

$$t_2 = \frac{(1+D_1)T}{2} - Cr_C \tag{4.87}$$

Substituting (4.81) in (4.80), we get the minimum ripple as

$$\Delta v_{o,\max} = \Delta v_o(t_2) = -\Delta i_L\left[\frac{D_1'T}{8C} + \frac{Cr_C^2}{2D_1'T}\right] + \Delta v_c(D_1T) \tag{4.88}$$

So, finally in buck mode, the total output voltage ripple will be

$$\Delta v_o = \Delta v_o\left(t_2\right) - \Delta v_o\left(t_1\right) = \Delta i_L\left[\frac{1}{8fC} + \frac{Cr_C^2 f}{2D_1D_1'}\right] \tag{4.89}$$

4.5.3 Effect of ESR on OVR

This analysis is same as the sections 2.5.3 and 3.5.3 from chapters 2 and 3 respectively.

4.5.4 Output capacitor design

Let the maximum specified output voltage ripple be Δv_{om}. Therefore, the value of capacitor C should be chosen such that

$$\Delta v_o \leq \Delta v_{om} \tag{4.90}$$

A. Buck-boost mode:

Substitute Δv_o from (4.76) in (4.90), we get,

$$\frac{(I_{\max}-I_{\min 1})}{2CD_1'T}\left[\left(\frac{I_{\max}-I_o}{I_{\max}-I_{\min 1}}\right)^2\left(D_1'T\right)^2 + \left(Cr_C\right)^2\right] + \frac{(I_{\max}+I_{\min 2}-I_o)(D_1-D_2)T}{2C} + I_o r_C \leq \Delta v_{om} \tag{4.91}$$

By solving the above inequality, we get,

$$C^2 r_C^2 - C\left[\frac{2D_1^{'}}{f}\left(\frac{\Delta v_{om}-I_o r_C}{\Delta i_L}\right)\right] + \frac{(I_{\max}-I_o)^2\left(D_1^{'}T\right)^2}{(\Delta i_L)^2} + \frac{(I_{\max}+I_{\min 2}-I_o)(D_1-D_2)D_1^{'}T^2}{\Delta i_L} \leq 0 \tag{4.92}$$

Expression (4.92) is quadratic in C and solution is the minimum value of filter capacitor C for given OVR and ICR, which can be obtained as follows:

$$C_{mn} = \frac{D_1^{'}}{f r_c^2}\left[\frac{\Delta v_{om}-I_o r_c}{\Delta i_L} \pm \sqrt{\left(\frac{\Delta v_{om}-I_o r_c}{\Delta i_L}\right)^2 - \left(\frac{I_{mx}-I_o}{\Delta i_L}\right)^2 r_c^2 - \frac{(I_{\max}+I_{\min 2}-I_o)(D_1-D_2)r_c^2}{\Delta i_L}}\right] \tag{4.93}$$

For buck-boost mode operation, when D_1 is very close to D_2, the later term in (4.93) is very small and hence this eq. (4.93) can be written as

$$C_{mnI} \approx \frac{D_1^{'}}{f r_c^2}\left[\frac{\Delta v_{om}-I_o r_c}{\Delta i_L} \pm \sqrt{\left(\frac{\Delta v_{om}-I_o r_c}{\Delta i_L}\right)^2 - \left(\frac{I_{mx}-I_o}{\Delta i_L}\right)^2 r_c^2}\right] \tag{4.94}$$

This expression is very similar to buck-boost converter ripple expression in section 3. These expressions are valid for $r_C \leq r_{C,max}$.

B. Boost mode:

The boost mode is same as to DC-DC boost converter as given Chapter 2, Section 2.5.4. This can be written as C_{mnII}.

C. Buck mode:

Substitute Δv_o from (4.89) in (4.90), we get,

$$\Delta i_L\left[\frac{1}{8fC} + \frac{C r_C^2 f}{2D_1 D_1^{'}}\right] \leq \Delta v_{om} \tag{4.95}$$

By solving the above inequality, we get,

$$C^2 r_C^2 - \frac{2D_1 D_1^{'}}{f}\left[\frac{\Delta v_{om}}{\Delta i_L}\right] C + \frac{D_1 D_1^{'}}{4f^2} \leq 0 \tag{4.96}$$

The above expression is quadratic in C and solution is the minimum value of filter capacitor C for given OVR and ICR, which can be obtained as follows:

$$C_{mnIII} = \frac{D_1 D_1^{'}}{f r_C^2}\left[\frac{\Delta v_{om}}{\Delta i_L}\right] - \sqrt{\left[\frac{D_1 D_1^{'}}{f r_C^2}\left[\frac{\Delta v_{om}}{\Delta i_L}\right]\right]^2 - \frac{D_1 D_1^{'}}{4f^2}} \tag{4.97}$$

This expression valid for $r_C \leq r_{C,max}$.

Finally, capacitor is chosen from these expressions such as

$$\mathrm{C} = \mathrm{Max}\left\{\mathrm{C_{mnI}}, \mathrm{C_{mnII}}, \mathrm{C_{mnIII}}\right\}. \tag{4.98}$$

4.5.5 Maximum permissible ESR ($r_{C,max}$) and ICR effect

As the value of ESR increases, more ripples appear in output voltage, degrading the output voltage quality. Therefore, it is necessary to find out the maximum permissible value of ESR for maximum specified OVR.

A. Boost and Buck-boost modes:

In Eq. (4.94), Capacitor C will have a real value (practically feasible) only if the terms inside the root is greater than or equal to zero, *i.e.,*

$$\left(\frac{\Delta v_{om} - I_o r_c}{\Delta i_L}\right)^2 - \left(\frac{I_{mx} - I_o}{\Delta i_L}\right)^2 r_c^2 \geq 0 \tag{4.99}$$

On simplification, we get,

$$r_c \leq \frac{\Delta v_{om}}{I_{mx}} \tag{4.100}$$

Therefore, the maximum permissible value of ESR ($r_{c,\max}$) for specified output voltage ripple and inductor current ripple can be defined as

$$r_{c,\max} \approx \frac{\Delta v_{om}}{I_{mx}} \tag{4.101}$$

If the ESR value of the output capacitor is greater than the $r_{c,\max}$, then the output voltage ripple will exceed the maximum defined limit.

Substituting value of $r_{C,\max}$ from Eq. (4.101) into (4.94), the minimum value of output capacitor in worst case is

$$C_{mn} = \frac{D_1' I_{mx}\left(I_{mx} - I_o\right)}{\Delta i_L \Delta v_{om} f} \tag{4.102}$$

From Eq. (4.102), it is clear that maximum permissible ESR depends on the ICR. This complete analysis is same as Chapters 2 and 3.

B. Buck mode:

In Eq. (4.97), capacitor C will have a real value (practically feasible) only if the terms inside the root is greater than or equal to zero, *i.e.,*

$$\left[\frac{D_1 D_1^{'}}{f r_C^2}\left[\frac{\Delta v_{om}}{\Delta i_L}\right]\right]^2 - \frac{D_1 D_1^{'}}{4f^2} \geq 0 \tag{4.103}$$

On simplification,

$$r_C \leq 2\sqrt{D_1 D_1^{'}}\frac{\Delta v_{om}}{\Delta i_L} \tag{4.104}$$

Therefore, the maximum permissible value of ESR ($r_{c,\max}$) for specified output voltage ripple and inductor current ripple can be defined as

$$r_{c,\max} = 2\sqrt{D_1 D_1^{'}}\frac{\Delta v_{om}}{\Delta i_L} \tag{4.105}$$

If the ESR value of the output capacitor is greater than the $r_{c,\max}$, then the output voltage ripple will exceed the maximum defined limit.

Substituting value of $r_{C,\max}$ from Eq. (4.105) into (4.97), the minimum value of output capacitor in worst case is

$$C_{mn} = \frac{1}{4f}\frac{\Delta i_L}{\Delta v_{om}} \tag{4.106}$$

4.6 Experimental Results and Discussion

The previous sections analytical findings are validated by simulations and experimental results. The simulations are carried out in MATLAB/Simulink software package whereas for the experimental results, a hardware prototype is developed as shown in Figure 4.10. According to the availability, MOSFET IRFP460 and diode MUR1560 are chosen as semiconductor switching devices. The ferrite core inductors and electrolytic capacitors are used as energy storage elements. The values of various parameters used for simulation and prototype design are given in Table 4.2.

Beginning with steady state analysis, from (4.24), the improved expression for duty cycle is calculated as 0.53, where as through ideal calculation (4.1), 0.44 are obtained to get a output of 15V. This has been verified through simulations as shown in Figure 4.11. These simulations are validated through experiment results as shown in Figure

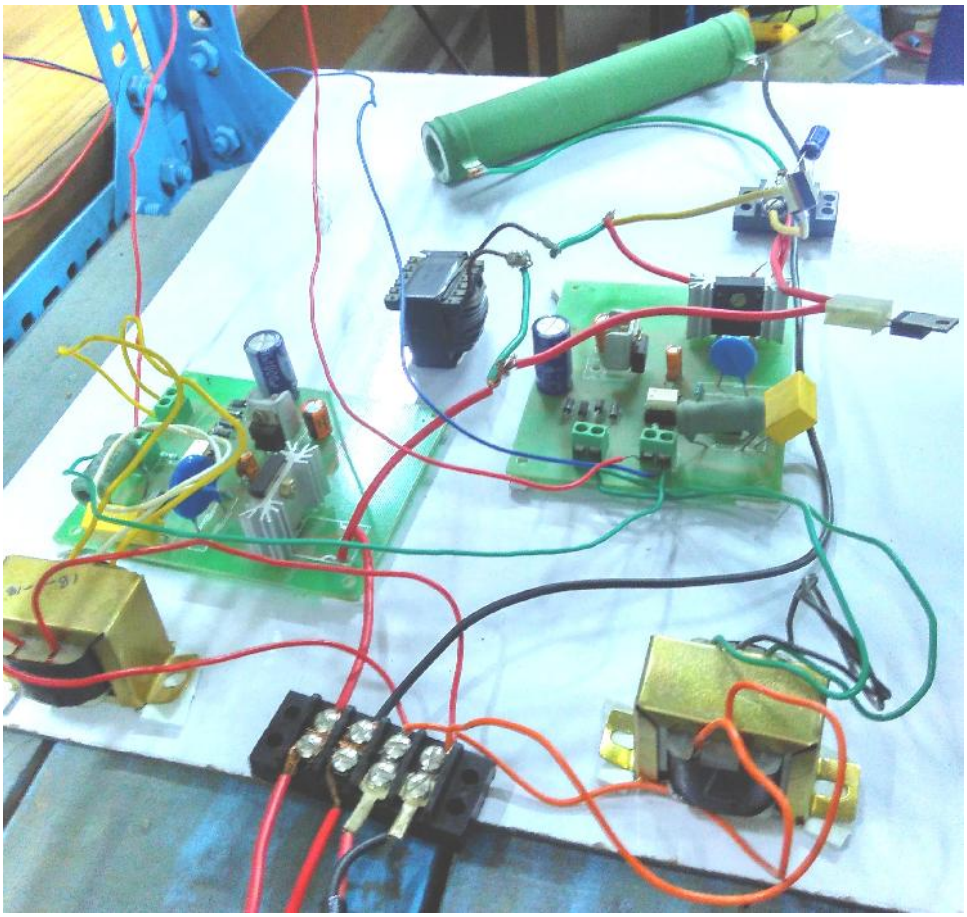


Figure 4.10: Experimental set-up.

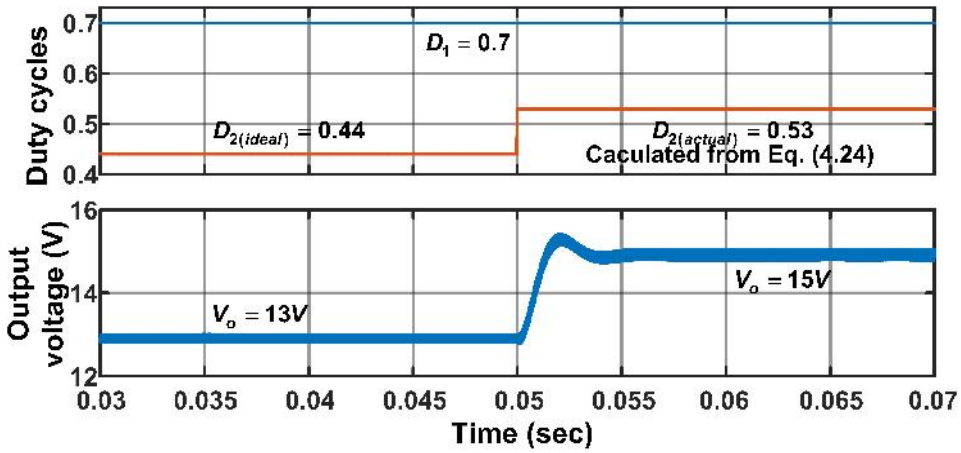


Figure 4.11: Simulation result of output voltage with ideal and modified duty cycle expressions.

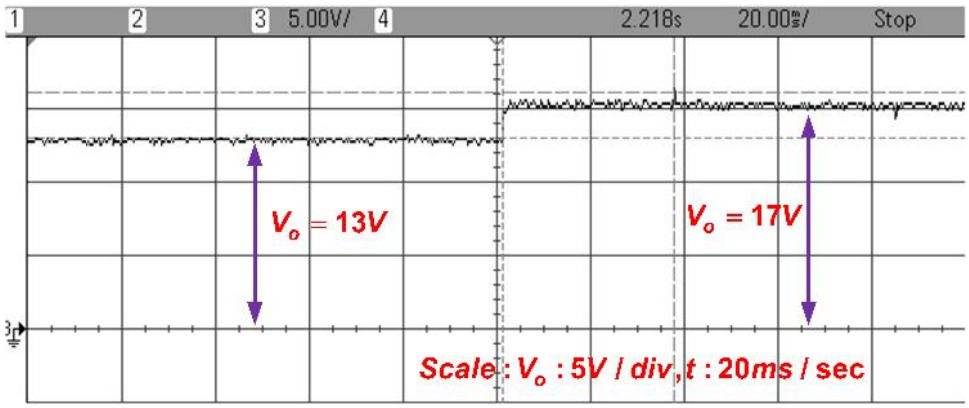


Figure 4.12: Experimental result of output voltage with ideal and modified duty cycle expressions.

3.15. Here, ideally calculated value has given less output value (*i.e.,*13V) than expected (*i.e.,*15V), where as the proposed duty cycle relation given as expected. This increase in duty cycle value is to compensate the voltage drop across parasitics.

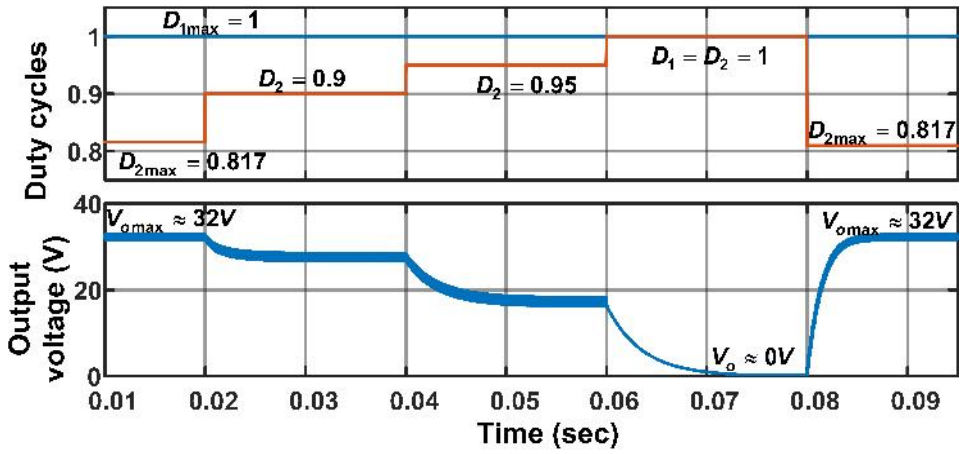


Figure 4.13: Simulation result of output voltage at different duty cycle $D_2 > D_{2\max}$, $D_{1\max} = 1$.

Here, the overall maximum permissible duty cycles and maximum achievable voltage with the NIBB converter are also have been verified by simulation and through experiments. The maximum permissible duty cycles of NIBB converter in presence of parasitics (as per Table 4.2) is $D_{1\max} = 1$, $D_{2\max} = 0.817$. The corresponding simulation and experimental results have been shown in Figure 4.13 and Figure 4.14

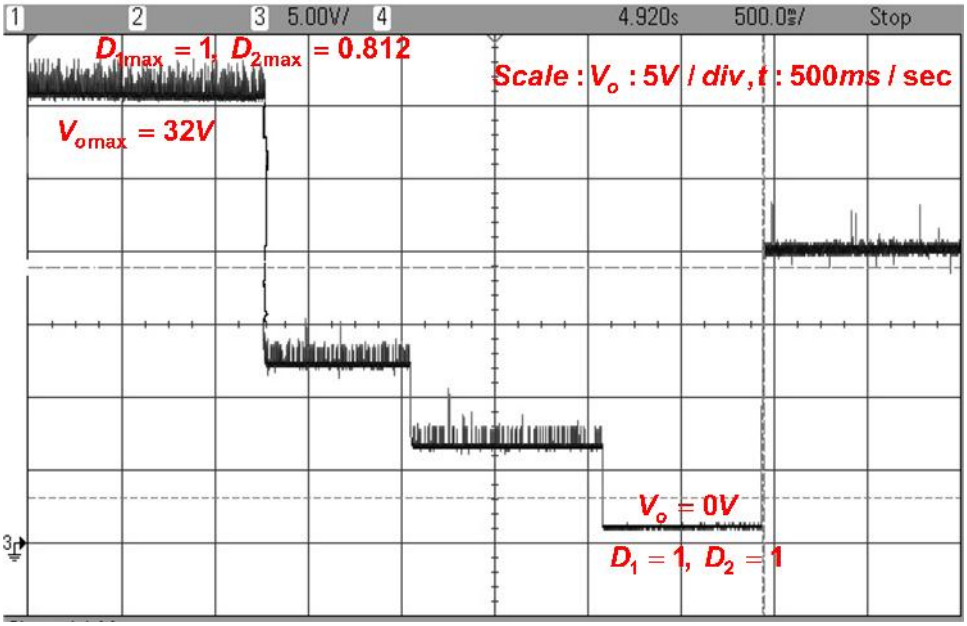


Figure 4.14: Experimental result of output voltage at different duty cycle $D_2 > D_{2\,\max}$, $D_{1\,\max} = 1$.

respectively. From this figure, it is very clear that the converter operates in unstable region when $D_2 > D_{2\,\max}$ to $D_2 = 1$ and $D_{1\,\max} = 1$. Alongside, the V_{omax} for this converter is 32.17 V. Therefore, this information is crucial for engineers to operate converter in a closed-loop.

Operation as a conventional buck-boost converter:

The basic advantage discussed earlier in this chapter is that there is no inversion of output voltage. So, in order to show this, first we will see the similar operation as we have seen in the chapter 3. Alongside, we will discuss the additional benefits of using NIBB converter over the buck-boost converter. In chapter 3, we designed the converter to get the output voltage of 7 V. So, here also if we design NIBB converter to get the same voltage, the parameter obtained are almost same as for buck-boost converter as given in Table 3.1. The simulation results are shown in Figure 4.15. This is same as we got previously with inversion of output voltage.

The same voltage we get in different possible combinations of duty cycles with the NIBB converter, whereas with basic buck-boost converter, this is not possible. Here,

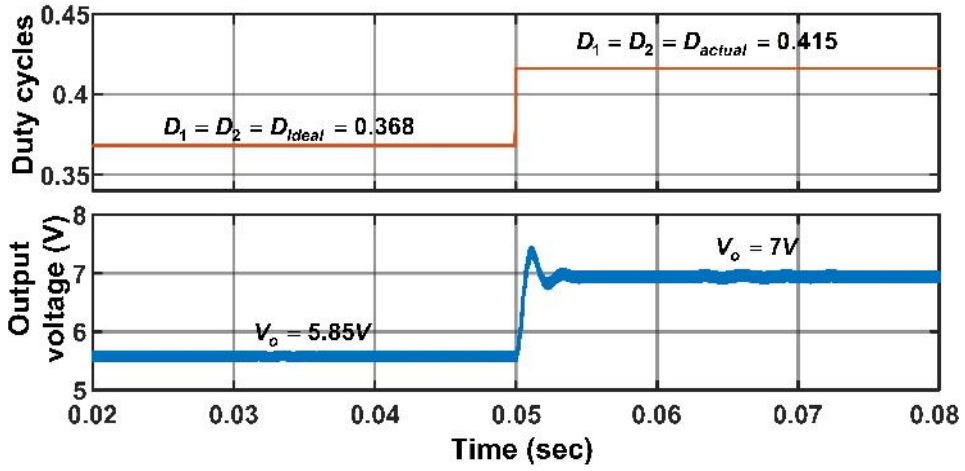


Figure 4.15: Simulation result of output voltage with ideal and modified duty cycle expressions.

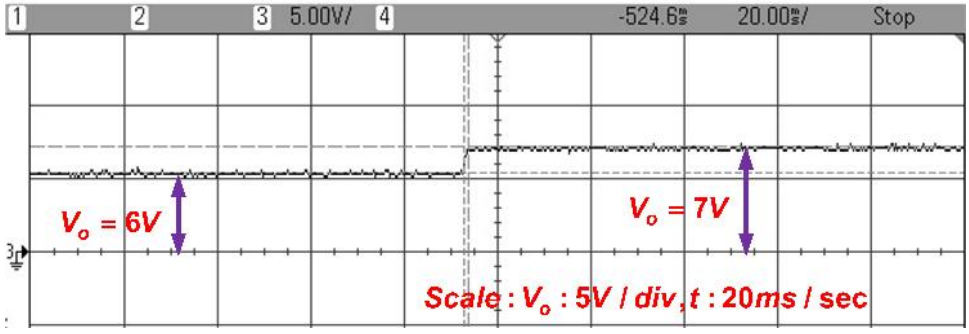


Figure 4.16: Experimental result of output voltage with ideal and modified duty cycle expressions.

we see in detail about this point. Some possible duty cycle combinations are A($D_1 = 0.655$, $D_2 = 0$), B($D_1 = 0.5$, $D_2 = 0.268$) etc. The inductor and capacitor required for first combination are $L = 230mH$, $C = 35uF$ respectively. So, these values are very less in comparison to the buck-boost converter. This is also called pure buck mode of operation. For the next combination, inductor and capacitor required are $L = 350mH$, $C = 60uF$, which are also less. So, with NIBB converter, we have option to choose best possible design.

Operation as a conventional boost converter:

Now, we will see the similar operation as we have seen in the chapter 2. Along-

side, we will discuss the additional benefits of using NIBB converter over the basic boost converter. In chapter 2, we designed the converter to get the output voltage of 8.3 V. So, here also if we design NIBB converter to get the same voltage, the parameter obtained are almost same as for boost converter as given in Table 2.1. The simulation results are shown in Figure 4.17. This is same as we achieved previously with inversion of output voltage.

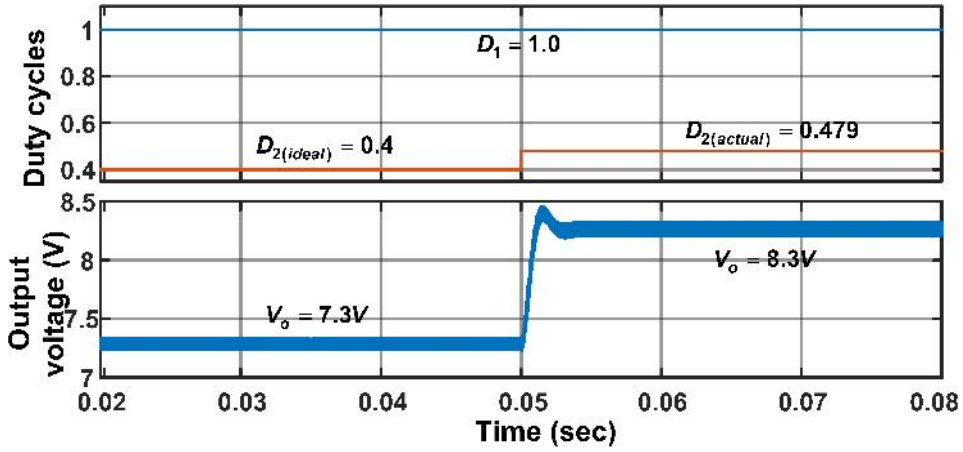


Figure 4.17: Simulation result of output voltage with ideal and modified duty cycle expressions in boost operating mode.

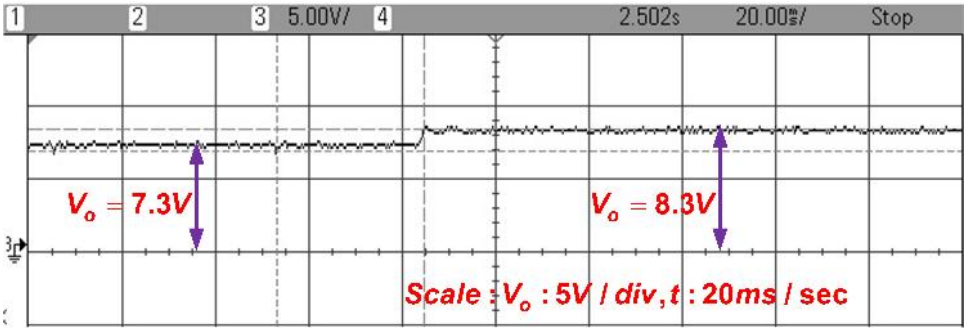


Figure 4.18: Experimental result of output voltage with ideal and modified duty cycle expressions in boost operating mode.

The same voltage we get in different possible combinations of duty cycles with the NIBB converter, whereas with basic boost converter this is not possible. Here, we

see in detail about this point. Some possible duty cycle combinations are A($D_1 = 0.7$, $D_2 = 0.69$), B($D_1 = 0.8$, $D_2 = 0.61$) etc. The inductor and capacitor required for first combination are $L = 330mH$, $C = 311uF$, respectively. So, these values are different in comparison to the boost converter. For the next combination, inductor and capacitor required are $L = 310mH$, $C = 135uF$, which are also different. So, with NIBB converter, we have option to choose best possible design.

4.7 Mathematical Modeling

NIBB converter with non-idealities to be modelled is shown in Figure 4.19. The state space average approach is used for modeling, which is explained in *Appendix A*. The most important point to be observed is that the modeling done by considering the all non-idealities or parasitics. As depicted in Figure 4.19 which is same as Figure 4.1(a), but a current source ($i_z(t)$) is connected to the output terminals of the converter, which models the loading effect of the load subsystem (besides the resistive load) being fed from this converter.

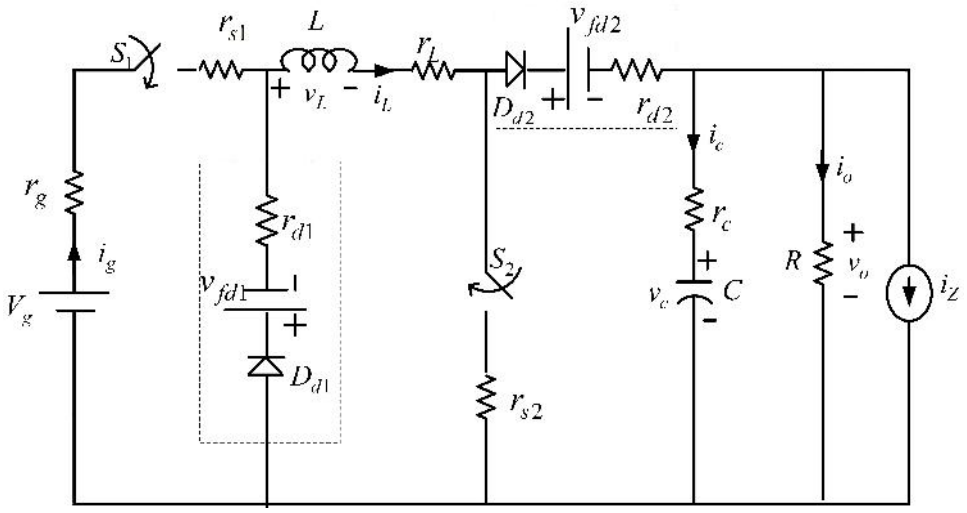


Figure 4.19: Non-ideal NIBB converter model.

As explained in previous sections, modeling of non-ideal DC-DC NIBB converter is carried out in CCM. The converter consists of two active switches (S_1 and S_2) and thus has three modes of operation.The equivalent circuits for these modes are

already shown in Figures 4.1(b)-(d). So, we need to write state equations for all modes of operation. For this, inductor current and capacitor voltage as considered as states of the system. The modeling as follows:

Step 1: Writing the state equations for three modes of operation

Mode-I Operation ($0 < t < D_2T$**)**

When both switches are ON, the equations governing with inductor current (i_L), capacitor voltage (v_c) and output voltage (v_o) are obtained as:

$$\begin{aligned} v_L(t) = L\frac{di_L(t)}{dt} &= -\left(r_g + r_{s1} + r_L + r_{s2}\right) i_L(t) + v_g(t) \\ \Rightarrow \dot{i}_L(t) &= -\frac{(r_g+r_{s1}+r_L+r_{s2})}{L} i_L(t) + \frac{v_i(t)}{L} \end{aligned} \tag{4.107}$$

$$i_c(t) = C\frac{dv_c(t)}{dt} = -\frac{v_o(t)}{R} - i_z(t) \tag{4.108}$$

$$v_o(t) = v_c(t) + r_c i_c(t) \tag{4.109}$$

Substitute (4.108) in (4.109), we get,

$$\begin{aligned} v_o(t) &= v_C(t) + r_C\left(-\frac{v_o(t)}{R} - i_z(t)\right) \\ \Rightarrow v_o(t) &= \frac{R}{(R+r_c)} v_c(t) - \frac{Rr_c}{(R+r_c)} i_z(t) \end{aligned} \tag{4.110}$$

Substitute (4.110) in (4.108), we get,

$$\dot{v}_c(t) = -\frac{1}{(R+r_c)\,C} v_c(t) - \frac{R}{(R+r_c)\,C} i_z(t) \tag{4.111}$$

$$i_g(t) = i_L(t) \tag{4.112}$$

Equations (4.107), (4.111), (4.110) and (4.112) can be represented in state space form as

$$\underset{\tilde{}}{\dot{x}} \qquad\qquad A_1 \qquad\qquad\qquad\qquad B_1 \qquad\qquad J_1$$

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} -\left(\frac{r_g+r_{s1}+r_L+r_{s2}}{L}\right) & 0 \\ 0 & -\frac{1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \begin{bmatrix} V_{fd} \end{bmatrix} \tag{4.113}$$

$$\tilde{\quad} \qquad y \qquad\qquad C_1 \qquad\qquad\qquad E_1 \qquad\qquad\qquad F_1$$

$$\begin{bmatrix} v_o(t) \\ i_g(t) \end{bmatrix} = \begin{bmatrix} 0 & \frac{R}{R+r_c} \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 0 & -\frac{Rr_c}{R+r_c} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \begin{bmatrix} V_{fd} \end{bmatrix} \tag{4.114}$$

Mode-II Operation ($D_2T < t < D_1T$)

When S_2 is OFF and S_1 is ON, the equations governing with inductor current (i_L), capacitor voltage (v_c) and output voltage (v_o) are obtained as:

$$\begin{aligned} v_L(t) = L\tfrac{di_L(t)}{dt} = -\left((r_g + r_{d2} + r_L + r_{s1}) + \tfrac{Rr_c}{(R+r_c)}\right) i_L(t) - \left(\tfrac{R}{(R+r_c)}\right) v_c(t) \\ + v_g(t) - V_{fd2} \end{aligned} \tag{4.115}$$

$$i_c(t) = C\frac{dv_c(t)}{dt} = i_L(t) - \frac{v_o(t)}{R} - i_z(t) \tag{4.116}$$

$$v_o(t) = v_c(t) + r_c i_c(t) \tag{4.117}$$

Substituting (4.116) in (4.117), we get,

$$\begin{aligned} & v_o(t) = v_c(t) + r_c\left(i_L(t) - \tfrac{v_o(t)}{R} - i_z(t)\right) \\ & \Rightarrow v_o(t) = \left(\tfrac{R}{R+r_c}\right) v_c(t) + \left(\tfrac{Rr_c}{R+r_c}\right) i_L(t) - \left(\tfrac{Rr_c}{R+r_c}\right) i_z(t) \end{aligned} \tag{4.118}$$

Substituting (4.118) in (4.116), we get,

$$\dot{v}_c(t) = \left(\frac{R}{C(R+r_c)}\right) i_L(t) - \left(\frac{1}{C(R+r_c)}\right) v_c(t) - \left(\frac{R}{C(R+r_c)}\right) i_z(t) \tag{4.119}$$

Substituting (4.118) in (4.115), we get,

$$\begin{aligned} \dot{i}_L(t) = -\left(\tfrac{(r_g+r_{d2}+r_L+r_{s1})(R+r_c)+Rr_c}{L(R+r_c)}\right) i_L(t) - \left(\tfrac{R}{L(R+r_c)}\right) v_c(t) + \left(\tfrac{1}{L}\right) v_g(t) \\ + \left(\tfrac{Rr_c}{L(R+r_c)}\right) i_z(t) - \tfrac{V_{fd2}}{L} \end{aligned} \tag{4.120}$$

$$i_g(t) = i_L(t) \tag{4.121}$$

Equations (4.120), (4.119), (4.121) and (4.118) can be represented in state space form as

$\tilde{\quad}$ $\dot{x}$ A_2 B_2

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} -\left(\frac{(r_g+r_{d2}+r_L++r_{s1})(R+r_c)+Rr_c}{L(R+r_c)}\right) & -\frac{R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & -\frac{1}{C(R+r_c)} \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{Rr_c}{L(R+r_c)} \\ 0 & -\frac{R}{C(R+r_c)} \end{bmatrix}\begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix}$$

J_2

$$+\begin{bmatrix} -\frac{1}{L} \\ 0 \end{bmatrix}\begin{bmatrix} V_{fd2} \end{bmatrix} \tag{4.122}$$

$\tilde{\quad}$ y C_2 E_2 F_2

$$\begin{bmatrix} v_o(t) \\ i_g(t) \end{bmatrix} = \begin{bmatrix} \frac{Rr_c}{R+r_c} & \frac{R}{R+r_c} \\ 1 & 0 \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 0 & -\frac{Rr_c}{R+r_c} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix}\begin{bmatrix} V_{fd2} \end{bmatrix} \tag{4.123}$$

Mode-III Operation ($D_1T < t < T$)

When both switches are OFF, the equations governing with inductor current (i_L), capacitor voltage (v_c) and output voltage (v_o) are obtained as:

$$\begin{aligned} v_L(t) = L\tfrac{di_L(t)}{dt} = &-\left((r_{d1}+r_{d2}+r_L)+\tfrac{Rr_c}{(R+r_c)}\right)i_L(t) - \left(\tfrac{R}{(R+r_c)}\right)v_c(t) \\ &-V_{fd1}-V_{fd2} \end{aligned} \tag{4.124}$$

$$i_c(t) = C\frac{dv_c(t)}{dt} = i_L(t) - \frac{v_o(t)}{R} - i_z(t) \tag{4.125}$$

$$v_o(t) = v_c(t) + r_c i_c(t) \tag{4.126}$$

Substitute (4.125) in (4.126), we get,

$$\begin{aligned} &v_o(t) = v_c(t) + r_c\left(i_L(t) - \tfrac{v_o(t)}{R} - i_z(t)\right) \\ &\Rightarrow v_o(t) = \left(\tfrac{R}{R+r_c}\right)v_c(t) + \left(\tfrac{Rr_c}{R+r_c}\right)i_L(t) - \left(\tfrac{Rr_c}{R+r_c}\right)i_z(t) \end{aligned} \tag{4.127}$$

Substituting (4.127) in (4.125), we get,

$$\dot{v}_c(t) = \left(\frac{R}{C(R+r_c)}\right)i_L(t) - \left(\frac{1}{C(R+r_c)}\right)v_c(t) - \left(\frac{R}{C(R+r_c)}\right)i_z(t) \tag{4.128}$$

Substituting (4.127) in (4.124), we get,

$$\begin{aligned} \dot{i}_L(t) = &-\left(\tfrac{(r_{d1}+r_{d2}+r_L)(R+r_c)+Rr_c}{L(R+r_c)}\right)i_L(t) - \left(\tfrac{R}{L(R+r_c)}\right)v_c(t) + \left(\tfrac{Rr_c}{L(R+r_c)}\right)i_z(t) \\ &-\tfrac{V_{fd1}}{L} - \tfrac{V_{fd2}}{L} \end{aligned} \tag{4.129}$$

$$i_g(t) = 0 \tag{4.130}$$

Equations (3.86), (3.85), (3.84) and (3.83) can be represented in state space form as

˜ $\dot{x}$ A_3 B_3

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} -\left(\frac{(r_{d1}+r_{d2}+r_L)(R+r_c)+Rr_c}{L(R+r_c)}\right) & -\frac{R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & -\frac{1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 0 & \frac{Rr_c}{L(R+r_c)} \\ 0 & -\frac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix}$$

J_3

$$+ \begin{bmatrix} -\frac{1}{L} \\ 0 \end{bmatrix} \left[V_{fd1} + V_{fd2}\right] \tag{4.131}$$

˜ y C_3 E_3 F_3

$$\begin{bmatrix} v_o(t) \\ i_g(t) \end{bmatrix} = \begin{bmatrix} \frac{Rr_c}{R+r_c} & \frac{R}{R+r_c} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 0 & -\frac{Rr_c}{R+r_c} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \left[V_{fd1} + V_{fd2}\right] \tag{4.132}$$

Step 2: Obtain the large signal state-space averaged model

Since there are two duty cycles, the averaged model can be obtained as follows:

$$\begin{aligned} A &= D_2A_1 + (D_1 - D_2)\,A_2 + (1 - D_1)\,A_3 \\ B &= D_2B_1 + (D_1 - D_2)\,B_2 + (1 - D_1)\,B_3 \\ C &= D_2C_1 + (D_1 - D_2)\,C_2 + (1 - D_1)\,C_3 \\ E &= D_2E_1 + (D_1 - D_2)\,E_2 + (1 - D_1)\,E_3 \\ F &= D_2F_1 + (D_1 - D_2)\,F_2 + (1 - D_1)\,F_3 \\ J &= D_2J_1 + (D_1 - D_2)\,J_2 + (1 - D_1)\,J_3 \end{aligned} \tag{4.133}$$

The large signal state space averaged model of NIBB converter obtained as

~ $\bar{\dot{x}}$ A

$$\frac{d}{dt}\begin{bmatrix}\bar{i}_L(t)\\ \bar{v}_C(t)\end{bmatrix} = \begin{bmatrix}-\left(\frac{(r_{d2}+r_L+D_1(r_g+r_{s1})+D_2(r_{s2}-r_{d2})+(1-D_1)r_{d1})(R+r_c)+(1-D_2)(Rr_c)}{L(R+r_c)}\right) & -\frac{(1-D_2)R}{L(R+r_c)}\\ \frac{(1-D_2)R}{C(R+r_c)} & -\frac{1}{C(R+r_c)}\end{bmatrix}\begin{bmatrix}\bar{i}_L(t)\\ \bar{v}_C(t)\end{bmatrix}$$

B J

$$+\begin{bmatrix}\frac{D_1}{L} & \frac{(1-D_2)Rr_c}{L(R+r_c)}\\ 0 & -\frac{R}{C(R+r_c)}\end{bmatrix}\begin{bmatrix}\bar{v}_g(t)\\ \bar{i}_z(t)\end{bmatrix} + \begin{bmatrix}-\left(\frac{1}{L}\right)\\ 0\end{bmatrix}\left[D_1'V_{fd1}+D_2'V_{fd2}\right] \tag{4.134}$$

~ $\bar{y}$ C E F

$$\begin{bmatrix}\bar{v}_o(t)\\ \bar{i}_g(t)\end{bmatrix} = \begin{bmatrix}\frac{(1-D_2)Rr_c}{R+r_c} & \frac{R}{R+r_c}\\ D_1 & 0\end{bmatrix}\begin{bmatrix}\bar{i}_L(t)\\ \bar{v}_C(t)\end{bmatrix} + \begin{bmatrix}0 & -\frac{Rr_c}{R+r_c}\\ 0 & 0\end{bmatrix}\begin{bmatrix}\bar{v}_g(t)\\ \bar{i}_z(t)\end{bmatrix} + \begin{bmatrix}0\\ 0\end{bmatrix}\left[V_{fd1}+V_{fd2}\right] \tag{4.135}$$

Step 3: Linearising around a operating point and obtain the ac small signal model

All the available time varying signals can be approximately written as sum of it's steady-state (DC or average) value and it's small variation around a operating point.

$$\begin{aligned}&i_L(t) = I_L + \hat{i}_L(t), i_g(t) = I_g + \hat{i}_g(t), i_o(t) = I_o + \hat{i}_o(t), i_z(t) = I_z + \hat{i}_z(t),\\ &d_1(t) = D_1 + \hat{d}_1(t), d_2(t) = D_2 + \hat{d}_2(t), v_C(t) = V_C + \hat{v}_C(t), v_g(t) = V_g + \hat{v}_g(t),\\ &v_o(t) = V_o + \hat{v}_o(t).\end{aligned} \tag{4.136}$$

To get the steady-state (DC) and small signal (ac) models of the non-ideal DC-DC NIBB converter, substitute (4.136) in (4.134) and (4.135), we get,

Steady-state (DC) model:

$$\begin{bmatrix}I_L\\ V_C\end{bmatrix} = -A^{-1}\left(B\begin{bmatrix}V_g\\ I_z\end{bmatrix} + J\right) \tag{4.137}$$

$$\begin{bmatrix}V_o\\ I_g\end{bmatrix} = C\begin{bmatrix}I_L\\ V_C\end{bmatrix} + E\begin{bmatrix}V_g\\ I_z\end{bmatrix} + F \tag{4.138}$$

Small-signal (ac) model:

$$\begin{aligned}\dot{\hat{x}}(t) &= A\hat{x}(t) + B\hat{u}(t) + B_{d1}\hat{d}_1(t) + B_{d2}\hat{d}_2(t)\\ \hat{y}(t) &= C\hat{x}(t) + E\hat{u}(t) + E_{d1}\hat{d}_1(t) + E_{d2}\hat{d}_2(t)\end{aligned} \tag{4.139}$$

Where,

$$\begin{aligned}B_{d2} &= (A_1 - A_2)X + (B_1 - B_2)U\\ B_{d1} &= (A_2 - A_3)X + (B_2 - B_3)U\\ E_{d2} &= (C_1 - C_2)X + (E_1 - E_2)U\\ E_{d1} &= (C_2 - C_3)X + (E_2 - E_3)U\end{aligned} \tag{4.140}$$

$$\begin{aligned}\tilde{\dot{\hat{x}}} \quad & \qquad\qquad\qquad\qquad A\\ \frac{d}{dt}\begin{bmatrix}\hat{i}_L(t)\\ \hat{v}_C(t)\end{bmatrix} &= \begin{bmatrix}-\left(\frac{(r_{d2}+r_L+D_1(r_g+r_{s1})+D_2(r_{s2}-r_{d2})+(1-D_1)r_{d1})(R+r_c)+(1-D_2)(Rr_c)}{L(R+r_c)}\right) & -\frac{(1-D_2)R}{L(R+r_c)}\\ \frac{(1-D_2)R}{C(R+r_c)} & -\frac{1}{C(R+r_c)}\end{bmatrix}\begin{bmatrix}\hat{i}_L(t)\\ \hat{v}_C(t)\end{bmatrix}\\ & \qquad\qquad\qquad\qquad B \qquad\qquad\qquad\qquad B_{d1}\\ & + \begin{bmatrix}\frac{D_1}{L} & \frac{(1-D_2)Rr_c}{L(R+r_c)}\\ 0 & -\frac{R}{C(R+r_c)}\end{bmatrix}\begin{bmatrix}\hat{v}_g(t)\\ \hat{i}_z(t)\end{bmatrix} + \begin{bmatrix}\frac{(-r_g-r_{s1}+r_{d1})I_L+V_g+V_{fd1}}{L}\\ 0\end{bmatrix}\left[\hat{d}_1(t)\right]\\ & \qquad\qquad\qquad\qquad\qquad\qquad B_{d2}\\ & + \begin{bmatrix}\frac{((r_{d2}-r_{s2})(R+r_c)+Rr_c)I_L+RV_c-Rr_cI_z+V_{fd2}(R+r_c)}{L(R+r_c)}\\ -\left(\frac{RI_L}{C(R+r_c)}\right)\end{bmatrix}\left[\hat{d}_2(t)\right]\end{aligned} \tag{4.141}$$

$$\begin{aligned}\tilde{\hat{y}} \quad & \qquad\qquad C \qquad\qquad\qquad E \qquad\qquad E_{d1}\\ \begin{bmatrix}\hat{v}_o(t)\\ \hat{i}_g(t)\end{bmatrix} &= \begin{bmatrix}\frac{(1-D_2)Rr_c}{R+r_c} & \frac{R}{R+r_c}\\ D_1 & 0\end{bmatrix}\begin{bmatrix}\hat{i}_L(t)\\ \hat{v}_C(t)\end{bmatrix} + \begin{bmatrix}0 & -\frac{Rr_c}{R+r_c}\\ 0 & 0\end{bmatrix}\begin{bmatrix}\hat{v}_g(t)\\ \hat{i}_z(t)\end{bmatrix} + \begin{bmatrix}0\\ I_L\end{bmatrix}\left[\hat{d}_1(t)\right]\\ & \qquad\qquad\qquad\qquad E_{d2}\\ & + \begin{bmatrix}-\left(\frac{Rr_cI_L}{R+r_c}\right)\\ 0\end{bmatrix}\left[\hat{d}_2(t)\right]\end{aligned} \tag{4.142}$$

Step 4: Determination of steady-state values

The steady-state values of output voltage, input current and inductor current can also be found by substituting (4.141), (4.142) in (4.137), (4.138) respectively, as follows:

$$\Rightarrow I_L = \frac{V_o}{D_2{}'R} + \frac{I_z}{D_2{}'} \tag{4.143}$$

$$\Rightarrow I_g = \frac{D_1 V_o}{D_2{}' R} + \frac{D_1 I_z}{D_2{}'} \tag{4.144}$$

$$\Rightarrow V_o = \frac{D_2' R \left(R + r_c\right) \left[D_1 V_g - D_1' V_{fd1} - D_2' V_{fd2}\right]}{\left(D_2 \left(r_{M1} - r_{M2}\right) + D_1 \left(r_{M2} - r_{M3}\right) + r_{M3}\right) \left(R + r_c\right) + \left(\left(1 - D_2\right) R\right)^2} \tag{4.145}$$

In order to get the ideal steady-state models of the DC-DC NIBB converter, replace non-idealities or parasitics with zero in (4.143)-(4.145), we get,

$$\Rightarrow I_{Li} = \frac{V_{oi}}{D_2{}' R} + \frac{I_z}{D_2{}'} \tag{4.146}$$

$$\Rightarrow I_{gi} = \frac{D_1 V_{oi}}{D_2{}' R} + \frac{D_1 I_z}{D_2{}'} \tag{4.147}$$

$$\Rightarrow V_{oi} = \frac{D_1 V_g}{1 - D_2} \tag{4.148}$$

4.7.1 Comparison of steady-state ideal and non-ideal models

In order to compare the steady-state ideal and non-ideal models, parameter values considered from Table 4.2. These values substituted in relationships obtained for non-ideal and ideal cases given in (4.143)-(4.145) and (4.146)-(4.148), respectively. The values obtained in non-ideal case are always less than the ideal case, this is due to the power loss in non-ideal elements which is clear from Table 4.3. This has been clearly discussed in previous sections, where these steady-state relationships are derived analytically as given in (4.13).

Step 5: Determination of various transfer functions

As per the considered input variables (v_g, i_z, d_1, d_2), state variables (i_L, v_C) and output variables (v_o, i_g), maximum sixteen transfer functions are possible for non-ideal DC-DC NIBB converter. Nevertheless, some important transfer functions only presented here. In order to get various transfer functions, first need to find $(sI - A)^{-1}$ for NIBB converter, which is given below:

$$[sI - A]^{-1} = \frac{Adj\,(sI - A)}{|sI - A|}$$

Table 4.3: Steady-state values comparison of ideal and non-ideal cases

Parameter	Ideal case			Non-ideal case		
	Analytical	Experimental	Error	Analytical	Experimental	Error
I_L (A)	1.7	1.5	13%	1.45	1.5	3.4%
V_o (V)	17.8	15	18%	15	15	0%
I_g (A)	1.2	1	20%	1.01	1	1%

$$\Rightarrow \frac{\begin{bmatrix} s+\frac{1}{C(R+r_c)} & -\frac{D_2^{'}R}{L(R+r_c)} \\ \frac{D_2^{'}R}{C(R+r_c)} & s+\frac{r_{eq}(R+r_C)+D_2^{'}Rr_C}{L(R+r_C)} \end{bmatrix}}{s^2+\frac{(R+r_c)\left(L+C\left(r_{eq}(R+r_c)+D_2^{'}Rr_c\right)\right)}{LC(R+r_c)^2}s+\frac{r_{eq}(R+r_c)+D_2^{'}R\left(D_2^{'}R+r_c\right)}{LC(R+r_c)^2}} \tag{4.149}$$

where, $r_{eq} = r_L + r_{d2} + D_1(r_g + r_{s1}) + D_2(r_{s2} - r_{d2}) + D_1^{'}r_{d1}$.

Now, some of the important transfer functions of non-ideal DC-DC NIBB converter are derived, which are useful for controller design and analysis.

(i) Control to output voltage or Control voltage gain:

This transfer function describes the impact of variation in duty cycles ($\hat{d}_1(t), \hat{d}_2(t)$) on output voltage ($\hat{v}_o$). This is derived by keeping the input voltage ($\hat{v}_g$) and output current ($\hat{i}_z$) variations to zero. This can be determined as follows:

$$G_{vd2}(s)|_{\hat{v}_g,\hat{i}_z,\hat{d}_1=0} = \frac{\hat{v}_o(s)}{\hat{d}_2(s)} = C(sI-A)^{-1}B_{d2} + E_{d2} \tag{4.150}$$

By substituting (4.141) and (4.142) in (4.150), we get,

$$G_{vd2}(s) = \begin{bmatrix} \frac{D_2^{'}Rr_c}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix} \frac{Adj(sI-A)^{-1}}{|sI-A|} \begin{bmatrix} \frac{((r_{d2}-r_{s2})(R+r_c)+Rr_c)I_L+RV_c-Rr_cI_z+V_{fd2}(R+r_c)}{L(R+r_c)} \\ -\left(\frac{RI_L}{C(R+r_c)}\right) \end{bmatrix} + \left[-\left(\frac{Rr_cI_L}{R+r_c}\right)\right] \tag{4.151}$$

Further simplifying (4.151) and writing in terms of pole-zero form as given in (4.152), we get,

$$G_{vd2} = K_{vd2}\frac{\left(1+\frac{s}{\omega_{LHPz}}\right)\left(1-\frac{s}{\omega_{RHPz}}\right)}{1+\frac{s}{Q\omega_P}+\left(\frac{s}{\omega_P}\right)^2} \tag{4.152}$$

where,

$$K_{vd2} = \frac{R\left(R+r_c\right)\left(\begin{array}{l}\left(D_1V_g - D_1'V_{fd1} - D_2'V_{fd2}\right)r_{v1} + \left(D_1V_g - D_1'V_{fd1}\right)\left(D_2'R\right)^2 \\ +D_2'\left(V_{fd2} - I_z\left(R \parallel r_c\right)\right)r_{v2} - I_z\left(R \parallel r_c\right)\left(D_2'\right)^3R^2\end{array}\right)}{\left(r_{eq}\left(R+r_c\right) + D_2'R\left(D_2'R+r_c\right)\right)^2} \tag{4.153}$$

$$\omega_{RHPz} = \frac{\left(\begin{array}{l}\left(D_1V_g - D_1'V_{fd1} - D_2'V_{fd2}\right)r_{v1} + \left(D_1V_g - D_1'V_{fd1}\right)\left(D_2'R\right)^2 \\ +D_2'\left(V_{fd2} - I_z\left(R \parallel r_c\right)\right)r_{v2} - I_z\left(R \parallel r_c\right)\left(D_2'\right)^3R^2\end{array}\right)}{L\left(R+r_c\right)\left(D_1V_g - D_1'V_{fd1} - D_2'V_{fd2}\right)} \tag{4.154}$$

here,

$$r_{v1} = \left(-D_1\left(r_g + r_{s1}\right) - r_L - r_{s2} - D_1'r_{d1}\right)\left(R+r_c\right)$$
$$r_{v2} = \left(\left(r_L + r_{d2} + D_1\left(r_{s1}+r_g\right) + D_2\left(r_{s2}-r_{d2}\right) + D_1'r_{d1}\right)\left(R+r_c\right) + D_2'Rr_c\right)$$

$$\omega_{LHPz} = \frac{1}{Cr_c} \tag{4.155}$$

$$\omega_p = \sqrt{\frac{\left(r_{eq}\left(R+r_c\right) + D_2'R\left(D_2'R+r_c\right)\right)}{LC\left(R+r_c\right)^2}} \tag{4.156}$$

$$Q = \frac{\sqrt{LC\left(r_{eq}\left(R+r_c\right) + D_2'R\left(D_2'R+r_c\right)\right)}}{L + C\left(r_{eq}\left(R+r_c\right) + D_2'Rr_c\right)} \tag{4.157}$$

Now,

$$G_{vd1}(s)|_{\hat{v}_g,\hat{i}_z,\hat{d}_2=0} = \frac{\hat{v}_o(s)}{\hat{d}_1(s)} = C(sI-A)^{-1}B_{d1} + E_{d1} \tag{4.158}$$

By substituting (4.141) and (4.142) in (4.158) we get,

$$G_{vd1}(s) = \left[\begin{array}{cc}\frac{D_2'Rr_c}{R+r_c} & \frac{R}{R+r_c}\end{array}\right]\frac{Adj(sI-A)^{-1}}{|sI-A|}\left[\begin{array}{c}\frac{(-r_g-r_{s1}+r_{d1})I_L+V_g+V_{fd1}}{L} \\ 0\end{array}\right] + \left[\begin{array}{c}0\end{array}\right] \tag{4.159}$$

Further simplifying (4.159) and writing in terms of pole-zero form as given in (4.160)

$$G_{vd1} = K_{vd1}\frac{\left(1+\frac{s}{\omega_{LHPz}}\right)}{1+\frac{s}{Q\omega_P}+\left(\frac{s}{\omega_P}\right)^2} \tag{4.160}$$

where,

$$K_{vd1} = \frac{D_2' R\left(R+r_c\right)\left(\begin{array}{l} V_g\left(\left(r_L+r_{d1}+D_2 r_{s2}+D_2' r_{d2}\right)\left(R+r_c\right)\right) \\ +V_{fd1}\left(\left(r_g+r_L+r_{s1}+D_2 r_{s2}+D_2' r_{d2}\right)\left(R+r_c\right)\right) \\ +\left(V_g+V_{fd1}\right)\left(D_2' R\left(D_2' R+r_c\right)\right)+V_{fd2}\left(D_2'\left(R+r_c\right)\left(r_g+r_{s1}-r_{d2}\right)\right) \end{array}\right)}{\left(r_{eq}\left(R+r_c\right)+D_2' R\left(D_2' R+r_c\right)\right)^2} \tag{4.161}$$

$$\omega_{LHPz} = \frac{1}{Cr_c} \tag{4.162}$$

$$\omega_p = \sqrt{\frac{\left(r_{eq}\left(R+r_c\right)+D_2' R\left(D_2' R+r_c\right)\right)}{LC(R+r_c)^2}} \tag{4.163}$$

$$Q = \frac{\sqrt{LC\left(r_{eq}\left(R+r_c\right)+D_2' R\left(D_2' R+r_c\right)\right)}}{L+C\left(r_{eq}\left(R+r_c\right)+D_2' R r_c\right)} \tag{4.164}$$

These transfer functions mainly used in controller design for regulator problems. Now, by replacing non-idealities or parasitics with zero in (4.152) and (4.160), we get the ideal model as,

$$G_{vdi1}(s) = \frac{\hat{v}_o}{\hat{d}_1}(s) = \frac{V_g}{D_2'\left(\frac{LC}{\left(D_2'\right)^2}s^2+\frac{L}{R\left(D_2'\right)^2}s+1\right)} \tag{4.165}$$

$$G_{vdi2}(s) = \frac{\hat{v}_o}{\hat{d}_2}(s) = \frac{D_1 V_g\left(1-\frac{L}{R\left(D_2'\right)^2}s\right)}{\left(D_2'\right)^2\left(\frac{LC}{\left(D_2'\right)^2}s^2+\frac{L}{R\left(D_2'\right)^2}s+1\right)} \tag{4.166}$$

(ii) Input to output voltage or Audio susceptibility:

This transfer function describes the impact of variation in input or line voltage ($\hat{v}_g$) on output voltage ($\hat{v}_o$). This is derived by keeping the duty cycles ($\hat{d}_1(t), \hat{d}_2(t)$) and output current ($\hat{i}_z$) variations to zero. This can be determined as follows:

$$G_{vg}(s)|_{\hat{i}_z,\hat{d}_1,\hat{d}_2=0} = \frac{\hat{v}_o(s)}{\hat{v}_g(s)} = C(sI-A)^{-1}B_{1^{st}column} + E_{1^{st}column} \tag{4.167}$$

By substituting (4.141) and (4.142) in (4.167), we get,

$$G_{vg}(s) = \begin{bmatrix} \frac{(1-D_2)Rr_c}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix} \frac{Adj(sI-A)^{-1}}{|sI-A|} \begin{bmatrix} \frac{D_1}{L} \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{4.168}$$

Further simplifying (4.168) and writing in terms of pole-zero form as given in (4.169), we get,

$$G_{vg}(s) = K_{vg}\frac{\left(1+\frac{s}{\omega_{LHPz}}\right)}{1+\frac{s}{Q\omega_P}+\left(\frac{s}{\omega_P}\right)^2} \tag{4.169}$$

where,

$$K_{vg} = \frac{D_1 D_2' R\left(R+r_c\right)}{r_{eq}\left(R+r_c\right)+D_2' R\left(D_2' R+r_c\right)} \tag{4.170}$$

$$\omega_{LHPz} = \frac{1}{Cr_c} \tag{4.171}$$

$$\omega_p = \sqrt{\frac{\left(r_{eq}\left(R+r_c\right)+D_2' R\left(D_2' R+r_c\right)\right)}{LC(R+r_c)^2}} \tag{4.172}$$

$$Q = \frac{\sqrt{LC\left(r_{eq}\left(R+r_c\right)+D_2' R\left(D_2' R+r_c\right)\right)}}{L+C\left(r_{eq}\left(R+r_c\right)+D_2' R r_c\right)} \tag{4.173}$$

This transfer function is very important in designing of regulator. The effect of input harmonics or changes on output can be found. Now, by replacing non-idealities or parasitics with zero in (4.169), we get the ideal model as,

$$G_{vgi}(s) = \frac{\widehat{v_o}}{\widehat{v_g}}(s) = \frac{D_1}{D_2'\left(\frac{LC}{\left(D_2'\right)^2}s^2+\frac{L}{R\left(D_2'\right)^2}s+1\right)} \tag{4.174}$$

(iii) Output Impedance:

This transfer function describes the impact of variation in output or load current ($\hat{i}_z$) on output voltage ($\hat{v}_o$). This is derived by keeping the duty cycles ($\hat{d}_1(t), \hat{d}_2(t)$) and input voltage ($\hat{v}_g$) variations to zero. This can be determined as follows:

$$Z_{out}(s)|_{\hat{v}_g,\hat{d}_1,\hat{d}_2=0} = \frac{\hat{v}_o(s)}{\hat{i}_z(s)} = C(sI-A)^{-1}B_{2^{nd}column} + E_{2^{nd}column} \tag{4.175}$$

By substituting (4.141) and (4.142) in (4.175), we get,

$$Z_{out}(s) = \begin{bmatrix}\frac{(1-D_2)Rr_c}{R+r_c} & \frac{R}{R+r_c}\end{bmatrix}\frac{Adj(sI-A)^{-1}}{|sI-A|}\begin{bmatrix}\frac{(1-D_2)Rr_c}{L(R+r_c)}\\ -\frac{R}{C(R+r_c)}\end{bmatrix} + \begin{bmatrix}-\frac{Rr_c}{R+r_c}\\ 0\end{bmatrix} \tag{4.176}$$

Further simplifying (4.176) and writing in terms of pole-zero form as given in (4.177), we get,

$$Z_{out}(s) = K_{zo}\frac{\left(1+\frac{s}{\omega_{LHPz1}}\right)\left(1+\frac{s}{\omega_{LHPz2}}\right)}{1+\frac{s}{Q\omega_P}+\left(\frac{s}{\omega_P}\right)^2} \tag{4.177}$$

where,

$$K_{zo} = -R\frac{r_{eq}\left(R+r_c\right)+D_2D_2^{'}Rr_c}{r_{eq}\left(R+r_c\right)+D_2^{'}R\left(D_2^{'}R+r_c\right)} \tag{4.178}$$

$$\omega_{LHPz1} = \frac{r_{eq}\left(R+r_c\right)+D_2D_2^{'}Rr_c}{L\left(R+r_c\right)} \tag{4.179}$$

$$\omega_{LHPz2} = \frac{1}{Cr_c} \tag{4.180}$$

$$\omega_p = \sqrt{\frac{\left(r_{eq}\left(R+r_c\right)+D_2^{'}R\left(D_2^{'}R+r_c\right)\right)}{LC(R+r_c)^2}} \tag{4.181}$$

$$Q = \frac{\sqrt{LC\left(r_{eq}\left(R+r_c\right)+D_2^{'}R\left(D_2^{'}R+r_c\right)\right)}}{L+C\left(r_{eq}\left(R+r_c\right)+D_2^{'}Rr_c\right)} \tag{4.182}$$

This transfer function also very important quantity in voltage regulator design. Now, by replacing non-idealities or parasitics with zero in (4.177), we get the ideal model as,

$$Z_{outi}(s) = \frac{\hat{v}_o(s)}{\hat{i}_z(s)} = \frac{LC}{\left(D_2^{'}\right)^2}\frac{-\frac{s}{C}}{\frac{LC}{\left(D_2^{'}\right)^2}s^2+\frac{L}{R\left(D_2^{'}\right)^2}s+1} \tag{4.183}$$

(iv) Input Impedance:

This transfer function describes the impact of variation in input or line voltage ($\hat{v}_g$) on input current ($\hat{i}_g$). This is derived by keeping the duty cycles ($\hat{d}_1(t), \hat{d}_2(t)$) and output current ($\hat{i}_o$) variations to zero. This can be determined as follows:

$$Z_{in}^{-1}(s)\big|_{\hat{i}_z,\hat{d}=0} = \frac{\hat{i}_g(s)}{\hat{v}_g(s)} = C_{2^{nd}row}(sI-A)^{-1}B_{1^{st}column}+E_{1^{st}column} \tag{4.184}$$

By substituting (4.141) and (4.142) in (4.184), we get,

$$Z_{in}^{-1}(s) = \begin{bmatrix} D_1 & 0 \end{bmatrix}\frac{Adj(sI-A)^{-1}}{|sI-A|}\begin{bmatrix}\frac{D_1}{L}\\0\end{bmatrix}+\begin{bmatrix}0\\0\end{bmatrix} \tag{4.185}$$

Further simplifying (4.185) and writing in terms of pole-zero form as given in (4.186), we get,

$$Z_{in}^{-1}(s) == K_{Zi}\frac{\left(1+\frac{s}{\omega_{LHPz}}\right)}{1+\frac{s}{Q\omega_P}+\left(\frac{s}{\omega_P}\right)^2} \tag{4.186}$$

where,

$$K_{Zi} = \frac{D_1^2(R + r_c)}{r_{eq}\left(R + r_c\right) + D_2' R\left(D_2' R + r_c\right)} \tag{4.187}$$

$$\omega_{LHPz} = \frac{1}{C\left(R + r_c\right)} \tag{4.188}$$

$$\omega_p = \sqrt{\frac{\left(r_{eq}\left(R + r_c\right) + D_2' R\left(D_2' R + r_c\right)\right)}{LC(R + r_c)^2}} \tag{4.189}$$

$$Q = \frac{\sqrt{LC\left(r_{eq}\left(R + r_c\right) + D_2' R\left(D_2' R + r_c\right)\right)}}{L + C\left(r_{eq}\left(R + r_c\right) + D_2' R r_c\right)} \tag{4.190}$$

This transfer function is useful for cascaded converters and it plays important role when EMI filter is added [4]. Now, by replacing non-idealities or parasitics with zero in (4.186), we get the ideal model as,

$$Z_{ini}^{-1}(s) = \frac{\widehat{i}_g(s)}{\widehat{v}_g(s)} = \frac{D_1^2\left(CRs + 1\right)}{R\left(D_2'\right)^2\left(\frac{LC}{\left(D_2'\right)^2}s^2 + \frac{LC}{R\left(D_2'\right)^2}s + 1\right)} \tag{4.191}$$

4.7.2 Comparison of small-signal ideal and non-ideal models

In order to compare the small signal ideal and non-ideal models, the parameter values considered from Table 4.2. These values substituted in relationships obtained for non-ideal and ideal cases given in (4.152)-(4.191). These non-ideal model transfer functions derived in this section will be further analysed in control point of view and effect of non-idealities or parasitics also analysed.

Table 4.4: Transfer function comparison of ideal and non-ideal cases

Parameter	$G_{vd1}(s)$		$G_{vd2}(s)$		$G_{vg}(s)$		$Z_o(s)$		$Z_{in}^{-1}(s)$	
	Ideal	Non-ideal	Ideal	Non-ideal	Ideal	Non-ideal	Ideal	Non-ideal	Ideal	Non-ideal
K (dB)	25.53	22.52	38	25.2	1.3	1.5	-2.6	-0.002	0.088	0.09
ω_{LHPz}	-	52080	-	52080	-	52080	0	52080,1.3k	284.1	282.5
ω_{RHPz}	-	-	9720	8703	-	-	-	-	-	-
ω_P	1661.6	1767	1661.6	1767	1661.6	1767	1661.6	1767	1661.6	1767
Q	5.8	1.05	5.8	1.05	5.8	1.05	5.8	1.05	5.8	1.05

4.8 Control Oriented Analysis

This section presents the importance of derived non-ideal transfer functions and crucial observations made through time domain and frequency response analysis. These transfer functions are mainly useful for voltage mode control, which is the objective of this thesis. Further, this section reveals the importance of small-signal transfer functions obtained by using state apace average approach over the respective ideal models or transfer functions.

4.8.1 Analysis of control to output voltage or control voltage gain

4.8.1.1 Parametric effect on poles and zeros

The small-signal model or control to output transfer function presented in (4.152), shows that it is a common two pole low pass filter with two zeros. Where as, (4.165) is an ideal one, which is also the same but with one zero. This is similar to boost or buck-boost transfer function. Another transfer function presented in (4.160), shows that it is a common two pole low pass filter with one zero. Where as, (4.166) is an ideal one, which is also the same but with no zero. This is similar to buck transfer function.

Since these transfer functions are similar to basic buck, boost and buck-boost converters, the pole-zero plots are similar and observations are also same. Please refer chapter 2 and chapter 3.

4.8.1.2 Time domain and frequency response analysis

As explained earlier, this analysis also similar (as in chapter 2 and chapter 3), but some important observations made through the step and Bode plots. The analysis is done at three different conditions, such as $A(\mathrm{D}_1 \neq \mathrm{D}_2, \mathrm{D}_1 > \mathrm{D}_2)$, $B(\mathrm{D}_1 = \mathrm{D}_2)$, $C(\mathrm{D}_1 = 1, \mathrm{D}_2)$.

By replacing the parameter values in (4.160) and (4.165), we get the transfer func-

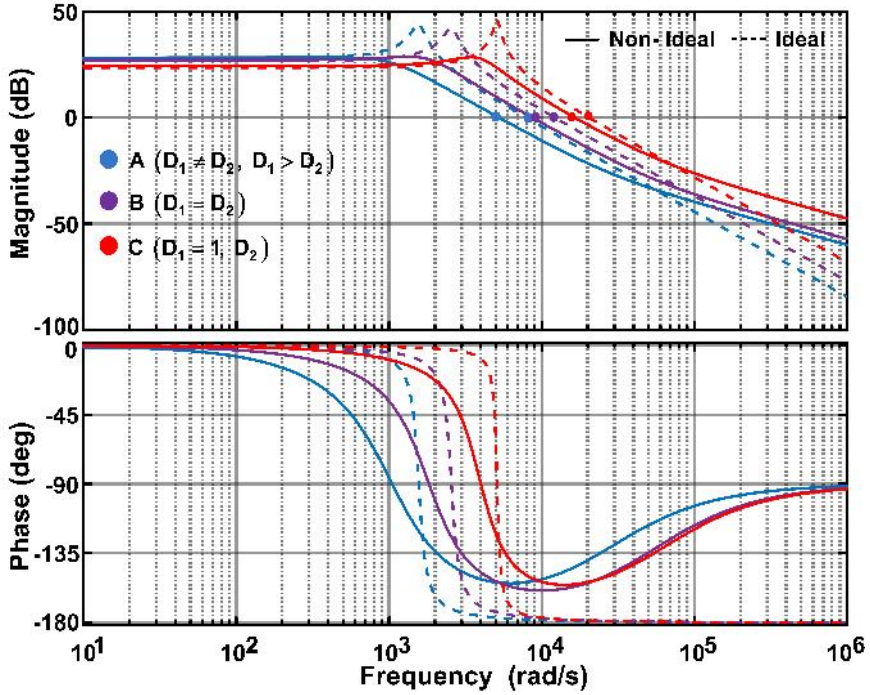


Figure 4.20: Frequency response of ideal and non-ideal models (v/d_1).

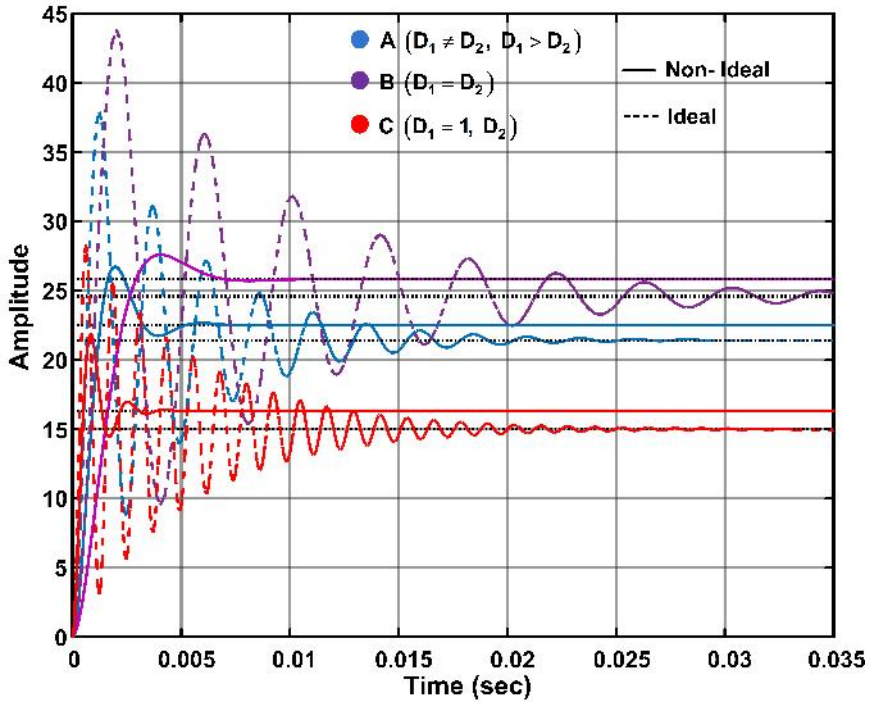


Figure 4.21: Time response of ideal and non-ideal models(v/d_1).

tions of non-ideal and ideal models as

$$G_{vd1}(s) = \frac{22.53\left(\frac{s}{52080}+1\right)}{\left(\frac{s}{1767}\right)^2 + \frac{s}{1876.2}+1} \tag{4.192}$$

$$G_{vd1i}(s) = \frac{25.53}{\left(\frac{s}{1661.6}\right)^2 + \frac{s}{9718.8}+1}. \tag{4.193}$$

These are very similar to buck transfer functions, which are of minimum phase type. Figure 4.22 and Figure 4.23 show the frequency and step responses of control to output transfer functions of ideal and non-ideal models respectively. The dc or low frequency gain of ideal and non-ideal models at all conditions is almost same. The gain crossover frequency is more for condition 'C'.

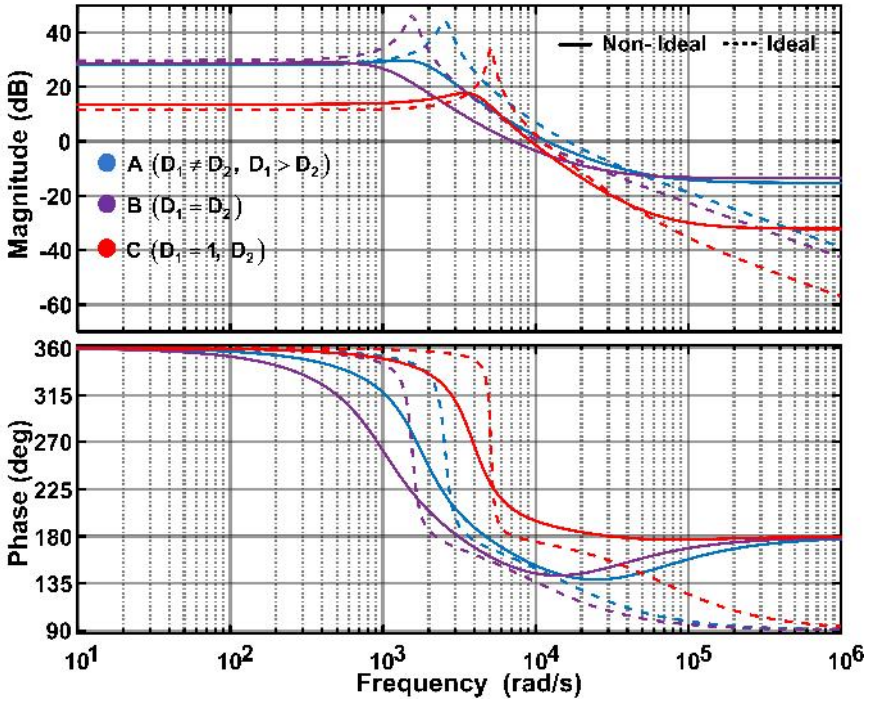


Figure 4.22: Frequency response of ideal and non-ideal models (v/d_2).

By replacing the parameter values in (4.152) and (4.166), we get the transfer functions of non-ideal and ideal models of DC-DC NIBB converter as

$$G_{vd2}(s) = \frac{25.13\left(\frac{s}{52080}+1\right)\left(-\frac{s}{8703}+1\right)}{\left(\frac{s}{1767}\right)^2 + \frac{s}{1876.2}+1} \tag{4.194}$$

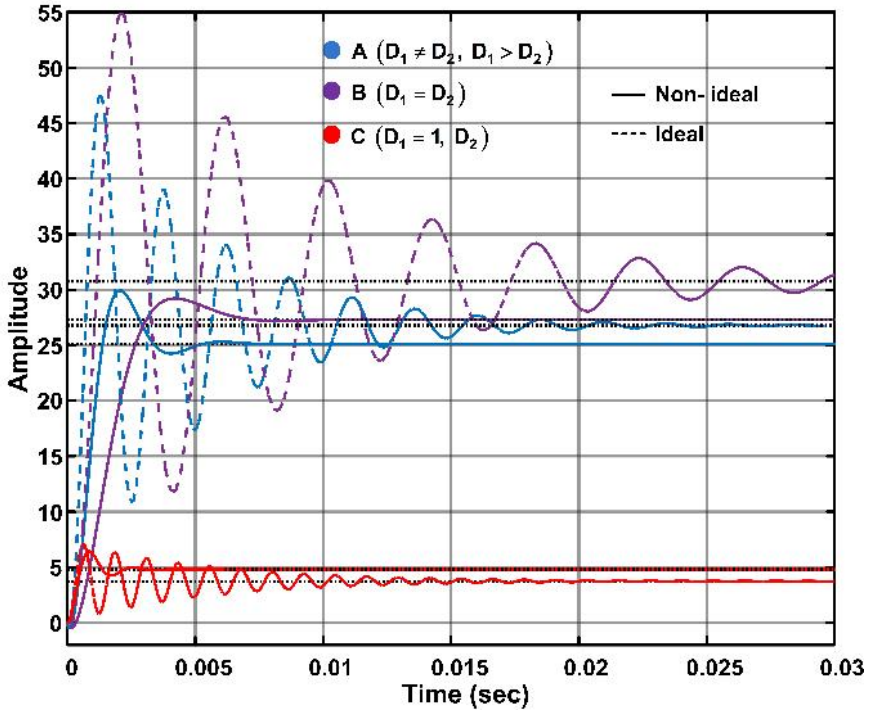


Figure 4.23: Time response of ideal and non-ideal models (v/d_2).

$$G_{vd2i}(s) = \frac{38.03\left(-\frac{s}{9720}+1\right)}{\left(\frac{s}{1661.6}\right)^2+\frac{s}{9718.8}+1}. \tag{4.195}$$

These are very similar to boost or buck-boost transfer functions, which are of non-minimum phase type. Figure 4.20 and Figure 4.21 show the frequency and step responses of control to output transfer functions of ideal and non-ideal models respectively.

The basic advantage of this analysis is that, converter parameters can be designed by observing these plots such that the better performance can be achieved.

4.8.2 Analysis of input to output voltage or audio susceptibility

By replacing the parameter values in (4.169) and (4.174), we get the transfer functions of non-ideal and ideal models of DC-DC NIBB converter as

$$G_{vg}(s) = \frac{1.31\left(\frac{s}{52080}+1\right)}{\left(\frac{s}{1767}\right)^2+\frac{s}{1876.2}+1} \tag{4.196}$$

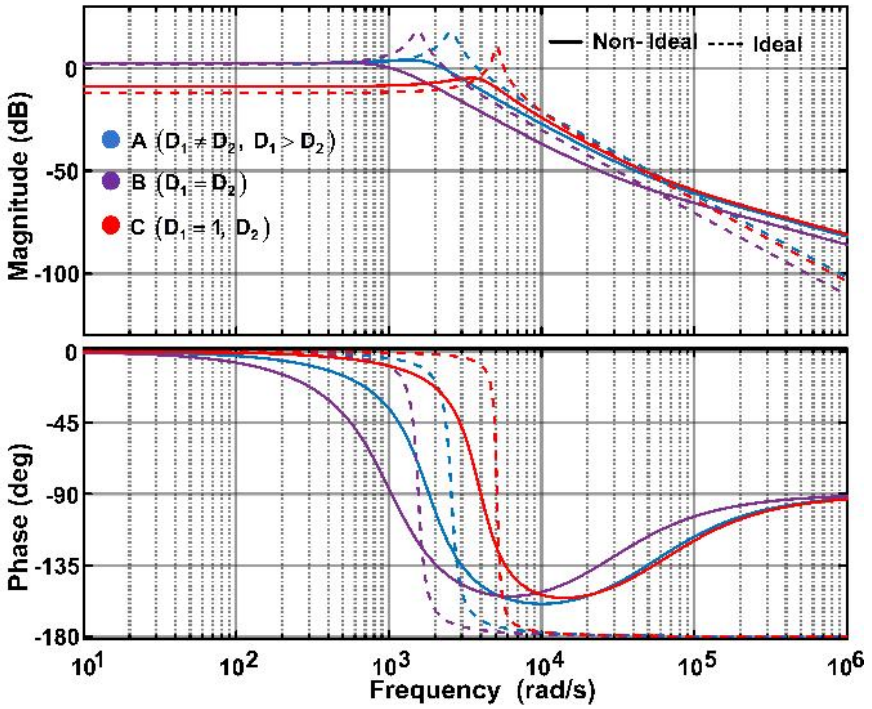


Figure 4.24: Frequency response of ideal and non-ideal models (v/v_g).

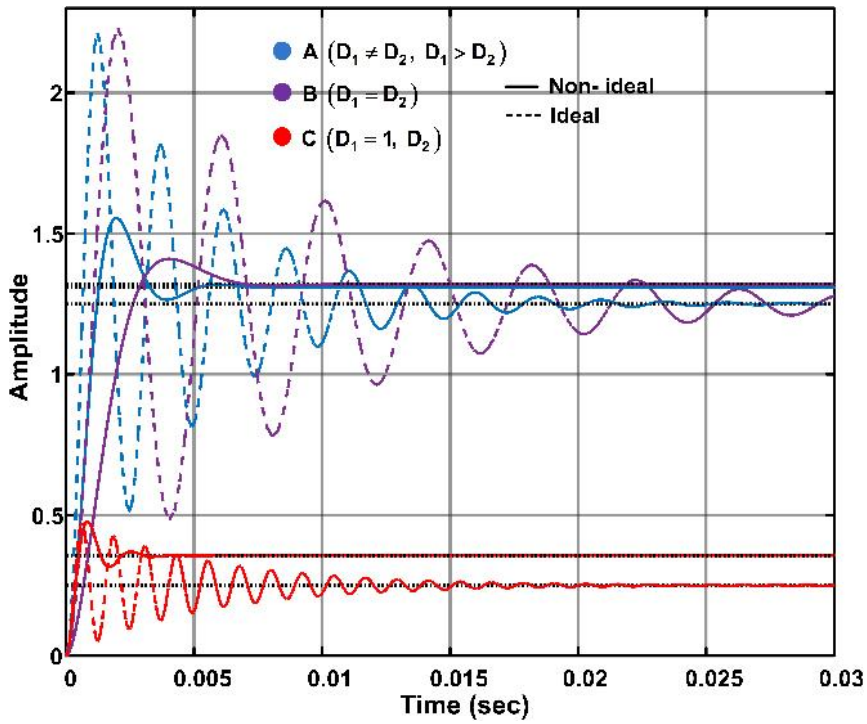


Figure 4.25: Step response of ideal and non-ideal models (v/v_g).

$$G_{vgi}(s) = \frac{1.489}{\left(\frac{s}{1661.6}\right)^2 + \frac{s}{9718.8} + 1}. \tag{4.197}$$

Figure 4.24 and Figure 4.25 show the frequency and step responses of input to output voltage transfer functions of ideal and non-ideal models, respectively.

From plots, it is observed that, dc gain of the system is less for operating point C and better stability. Another way, boost mode of operation is giving better performance compared to other operating points. This option is available with only NIBB converter.

4.8.3 Analysis of output impedance

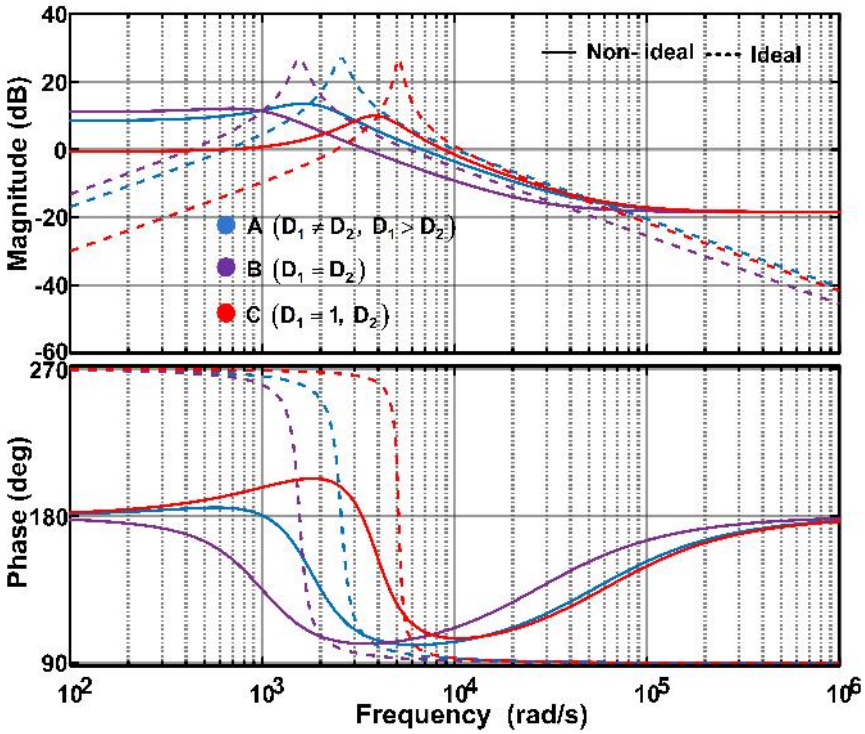


Figure 4.26: Frequency response of ideal and non-ideal models (v/i_z).

By replacing the parameter values in (4.177) and (4.183), we get the transfer functions of non-ideal and ideal models of DC-DC NIBB converter as

$$Z_o(s) = -\frac{2.64\left(\frac{s}{1329} + 1\right)\left(\frac{s}{52080} + 1\right)}{\left(\frac{s}{1767}\right)^2 + \frac{s}{1876.2} + 1} \tag{4.198}$$

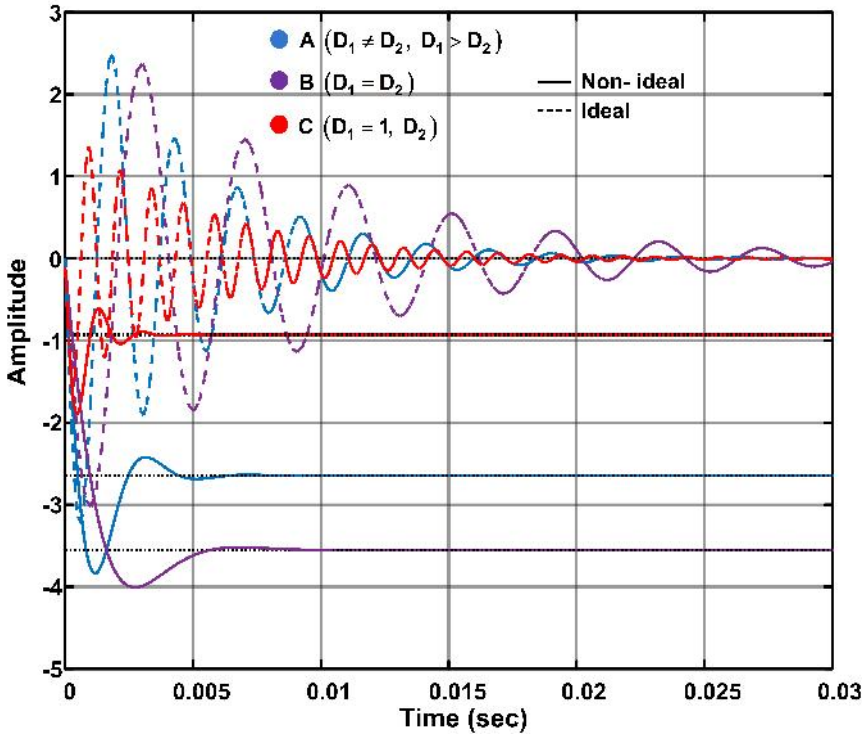


Figure 4.27: Step response of ideal and non-ideal models (v/i_z).

$$Z_{oi}(s) = \frac{-\frac{s}{441.76}}{\left(\frac{s}{1661.6}\right)^2 + \frac{s}{9718.8} + 1}. \tag{4.199}$$

Figure 4.26 and Figure 4.27 show the frequency and step responses of output impedance transfer functions of ideal and non-ideal models, respectively.

From plots, it is observed that, the dc or low frequency gain and stability parameters are better for operating point C. At dc and low frequencies, capacitive reactance is more and output impedance is dominated by inductive reactance. As frequency increases, the capacitive reactance dominates and makes impedance zero.

4.8.4 Analysis of input impedance

By replacing the parameter values in (4.186) and (4.191), we get the transfer functions of non-ideal and ideal models of DC-DC NIBB converter as,

$$Z_{in}^{-1}(s) = \frac{0.088\left(\frac{s}{282.5} + 1\right)}{\left(\frac{s}{1767}\right)^2 + \frac{s}{1876.2} + 1} \tag{4.200}$$

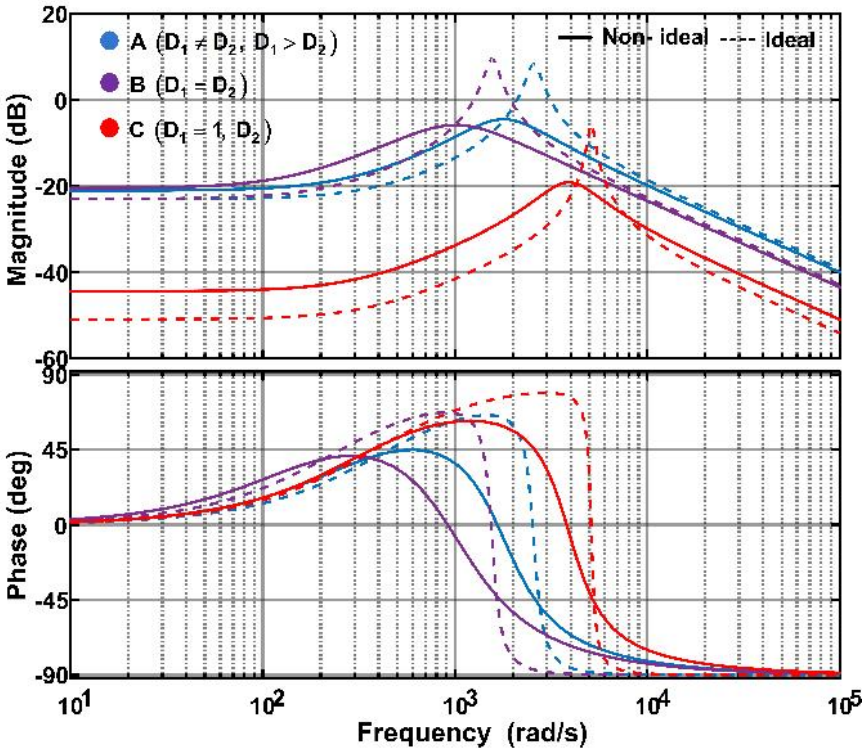


Figure 4.28: Frequency response of ideal and non-ideal models (i_g/v_g).

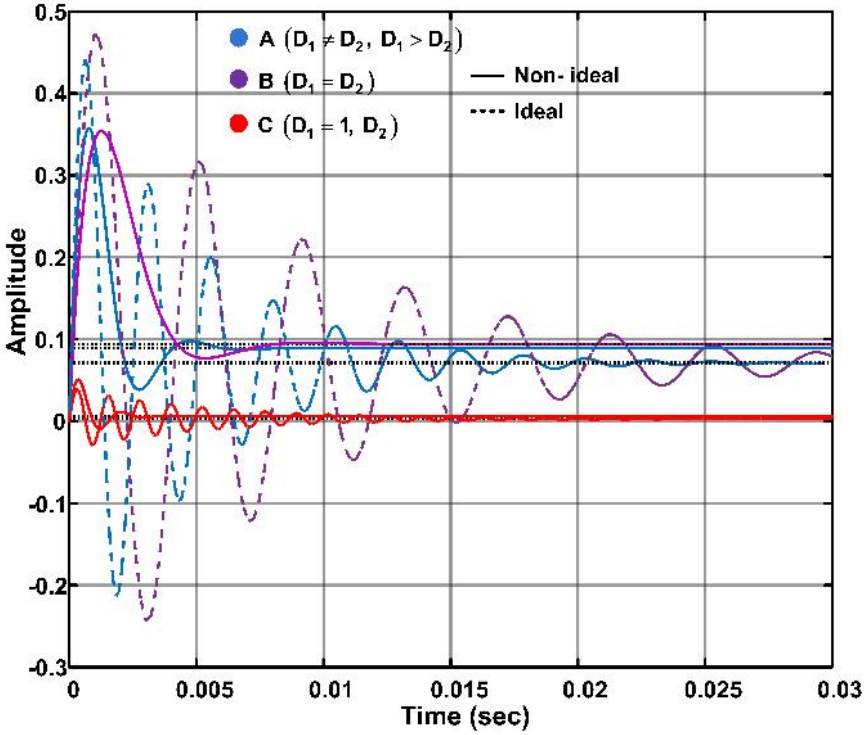


Figure 4.29: Step response of ideal and non-ideal models (i_g/v_g).

$$Z_{ini}^{-1}(s) = \frac{0.1\left(\frac{s}{284.1}+1\right)}{\left(\frac{s}{1661.6}\right)^2 + \frac{s}{9718.8} + 1} \tag{4.201}$$

Figure 4.28 and Figure 4.29, show the frequency and step responses of input impedance transfer functions of ideal and non-ideal models, respectively.

From plots, it is observed that the input impedance is at low frequencies or dc differs a lot for boost mode operation (*i.e.,* operating point C) and it is minimum for all operating points at corner frequency. Phase is decreasing from 0 to -90, as frequency increasing. From step response, it is observed that the steady state error is zero in both cases, but ideal is more oscillatory.

4.9 Proposed NIBB Derived Hybrid Converter (NIBBDHC)

Generating power from natural resources (or non conventional energy sources) is always appreciable for residential systems. Increasing population put main constraints on space utilization, so these sources are confined to give low voltage and power whereas, modern developed grids (such as nano grids, DC micro grid etc) can give high voltages and power. There are two independent converters are available for power conversion, such as dc to dc converter (e.g., buck, boost or buck-boost) and dc to ac converter *i.e.,* voltage source converter (VSC). These two converters are either connected in series or parallel according to the requirement (AC or DC). Grids might be connected to the loads which may require both step-up and step-down operation. For these type of requirements, a non-inverting buck-boost topology [32] is suitable.

The major issue with conventional VSCs is shoot-through. By using dead-time circuitry, this issue can be resolved. But, it is an additional circuitry. EMI (Electro Magnetic Interference) [182] is also another problem for VSCs. For resolving these issues, many topologies investigated in literature. One of such topology is the Z-source inverter (ZSI) [183], which can eliminate the shoot-through problem. Further many topologies such as quasi-ZSI [184] and for achieving high gains [185]- [187] are proposed. All these converter topologies are for mitigating the problem of con-

ventional VSCs and these cannot provide hybrid converter operation *i.e.,* supplying AC and DC loads, simultaneously.

Hybrid converter topologies are also proposed in literature [73]- [76]. Switched boost inverter (SBI) [73], boost derived hybrid converter (BDHC) [74] are some of proposed hybrid converter topologies. But, these converter topologies can only achieve boost operation. Further, cuk-derived hybrid converter (Cuk-DHC) proposed in [75], is a hybrid converter which can achieve both buck and boost operations. But, with inversion of output voltage and it contain more number of passive elements. Current fed switched inverter (CFSI) based hybrid topology proposed in [76], which can

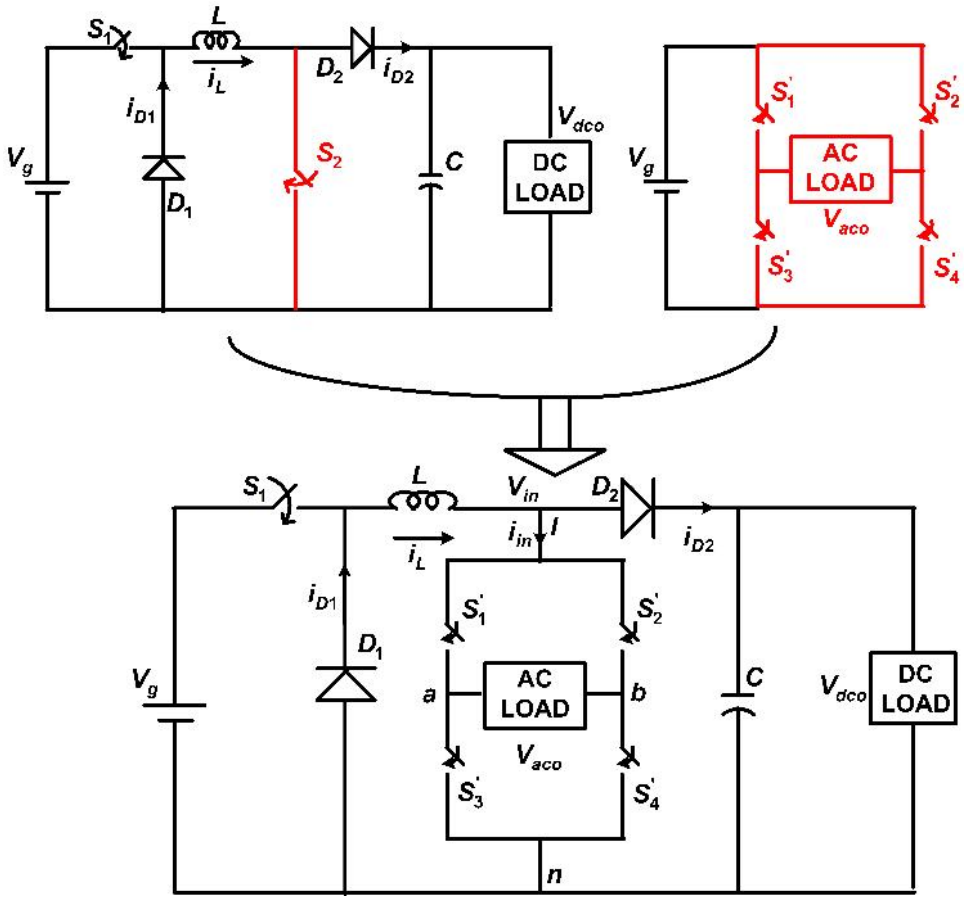


Figure 4.30: Proposed non-inverting buck-boost derived hybrid converter.

be operated in buck and boost modes. But, buck and boost characteristics achieved for AC output and for DC output boost characteristics are only possible. So, this

motivated to propose a hybrid converter which meets the discussed requirements.

4.9.1 Synthesis of NIBBDHC

The conventional two switch non-inverting buck-boost topology is shown in Figure 4.1. The NIBBDHC topology synthesized by replacing the switch S2 by a conventional VSC as shown in Figure 4.30. The switch S_1 used to get different modes of operation. The bridge type VSC having four switches ($S_1^{'}$ to $S_4^{'}$), is realized by MOSFET or IGBTs which are compatible for high switching frequency. This topology will provide non-inverting DC output (V_{dco}) by the buck-boost converter action besides AC output (V_{aco}). Converter can be operated in three different modes namely buck mode, boost mode and buck-boost mode. This operation can be achieved by simultaneous switching of any independent leg of VSC ($S_1^{'} - S_3^{'}$ or $S_2^{'} - S_4^{'}$) along with switch S_1. This is very similar to normal operation of non-inverting buck-boost operation. The AC output from NIBBDHC is obtained by providing the appropriate PWM switching pulses to the switches of inverter leg ($S_1^{'} - S_4^{'}$ or $S_2^{'} - S_3^{'}$). The node voltage ($V_{\ln}$) acts as input to the VSC.

4.9.2 Operation of NIBBDHC

The NIBBDHC operation can be studied in three dissimilar manner *i.e.*, buck, boost and buck-boost operation. The buck operation of NIBBDHC obtained when ON period of switch S_1 is less than the shoot-through interval. The boost operation of NIBBDHC observed when switch S_1 is ON for total duration irrespective of shoot-through interval. The buck-boost operation of NIBBDHC realized in two cases as when the shoot- through interval is equal to the ON period of switch S_1 and ON period of switch S_1 is greater than the shoot-through interval. The continuous conduction operation of NIBBDHC is analysed. The waveforms for NIBBDHC in buck operating conditions are shown in Figure 4.31(a). The waveforms for NIBBDHC in boost and buck-boost operating conditions are shown in Figure 4.31(b). The major difference in boost to buck-boost operating condition switch S_1 duty cycle (D_{st2}), which is unity for boost operating conditions. So, diode D_1 never comes in conduction in boost operating

condition. This can be seen from diode D_1 current waveform (i_{D1}) in Figure 4.31(b), which is zero in boost operating condition and non-zero for buck-boost operating conditions. The waveforms node voltage (V_{in}), inductor current (i_L), VSC output voltage (V_{ab}), diode currents (i_{D1}, i_{D2}), VSC input current ($i_{\ln}$) are shown.

In all operating conditions of NIBBDHC, three different switching modes observed as explained below.

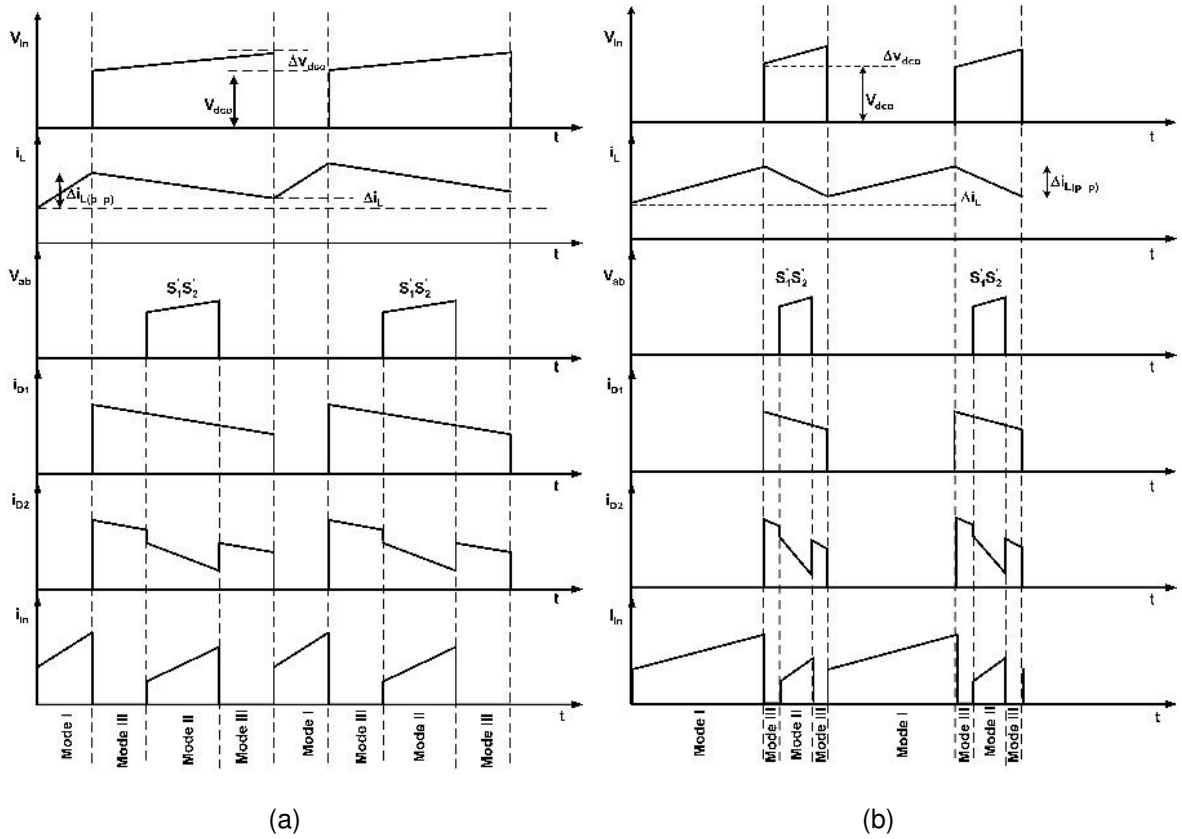


Figure 4.31: Waveforms of NIBBDHC (a) Buck operating conditions (b) Buck-boost operating conditions.

4.9.2.1 Mode-I (Shoot-through)

Shoot-through is nothing but both switches of anyone inverter leg operated at the same instant ($S_1^{'} - S_3^{'}$ or $S_2^{'} - S_4^{'}$). Shoot-through period of NIBBDHC in buck type operating conditions are shown in Figure 4.32(a), (b). Since the switch S_1 duty cycle

(D_{st2}) is less than shoot through duty cycle (D_{st1}), the diode D_1 will come into the conduction as soon as switch S_1 goes to OFF state. Shoot-through period of NIBB-DHC in boost type operating conditions is shown in Figure 4.33(a). Since the switch S_1 duty cycle (D_{st2}) is equal to one (*i.e.,* S_1 always ON), the shoot through duty cycle (D_{st1}) will become the boost converter duty cycle and the diode D_1 will always be in OFF state. Shoot-through period of NIBBDHC in buck-boost type operating conditions is shown in Figure 4.34(a). Since the switch S_1 duty cycle (D_{st2}) is equal or more than the shoot through duty cycle (D_{st1}), both buck and boost operations are possible. In all operating conditions, the diode D_2 will be reverse biased during this period.

4.9.2.2 Mode-II (Power Period)

In this mode, power delivered to the load. The diode D_2 is ON during this period. The voltage input to the inverter ($V_{\ln}$) is equal to the output dc voltage (V_{dco}). In this mode, for all types of operating conditions either $S_1' - S_4'$ or $S_2' - S_3'$ will be ON to deliver power to AC load. The power period of NIBBDHC in buck type operating conditions is shown in Figure 4.32(c). The diode D_1 will be on in buck operating conditions. The power period of NIBBDHC in boost type operating conditions is shown in Figure 4.33(c). The power period of NIBBDHC in buck-boost type operating conditions is shown in Figure 4.34(b) for $D_{st2} = D_{st1}$ and for $D_{st2} > D_{st1}$ is shown in Figure 4.34(c).

4.9.2.3 Mode-III (Zero or null Period)

During zero period, the currents circulates among the switches of bridge network. Current is neither supplied nor absorbed. Zero period of NIBBDHC in buck type operating conditions is shown in Figure 4.32(d). Zero period of NIBBDHC in boost type operating conditions is shown in Figure 4.33(c). Zero period of NIBBDHC in buck-boost type operating conditions is shown in Figure 4.34(d). In all operating conditions, the diode D_2 will be in conduction.

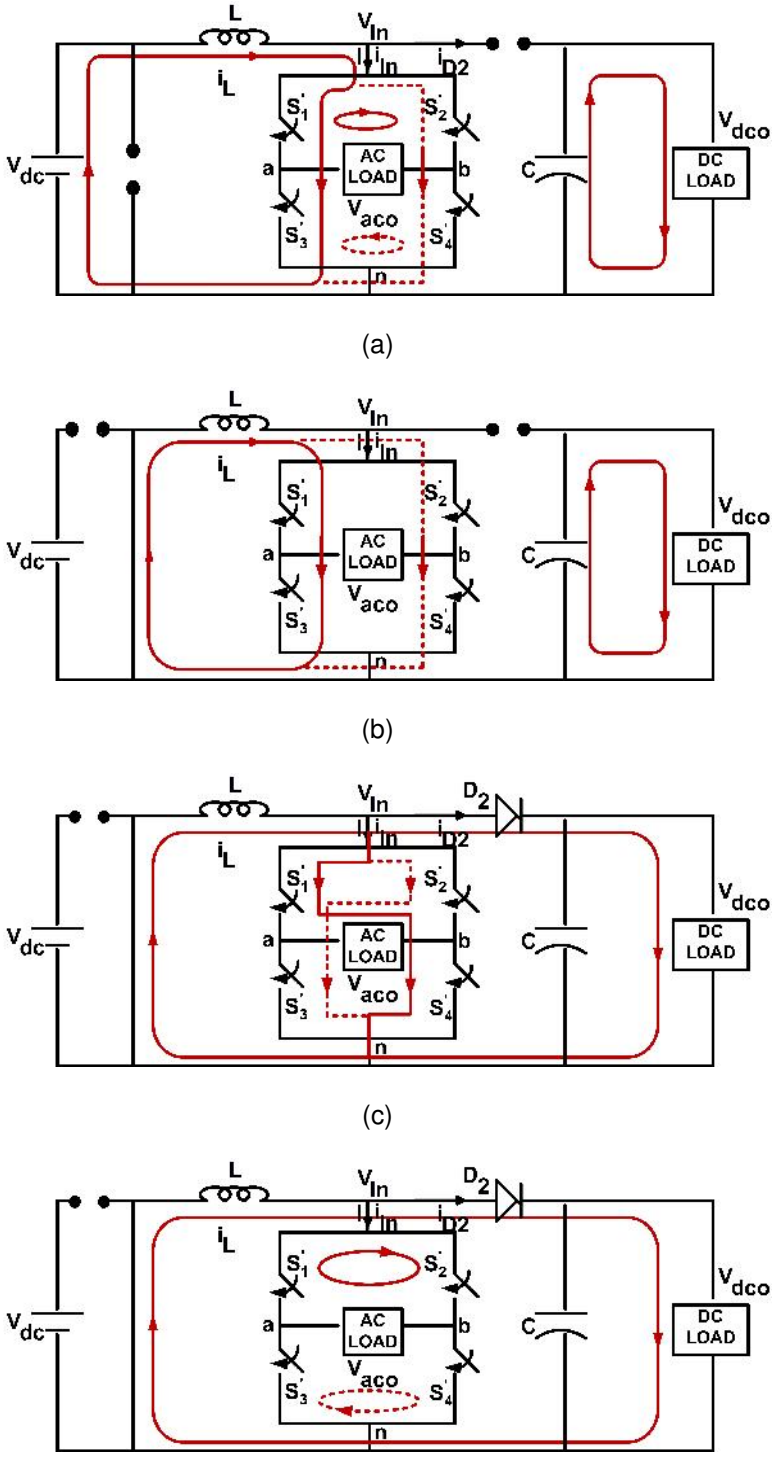


Figure 4.32: Buck operation of NIBBDHC (a) and (b) Shoot-through period (c) Power period (d) Zero period.

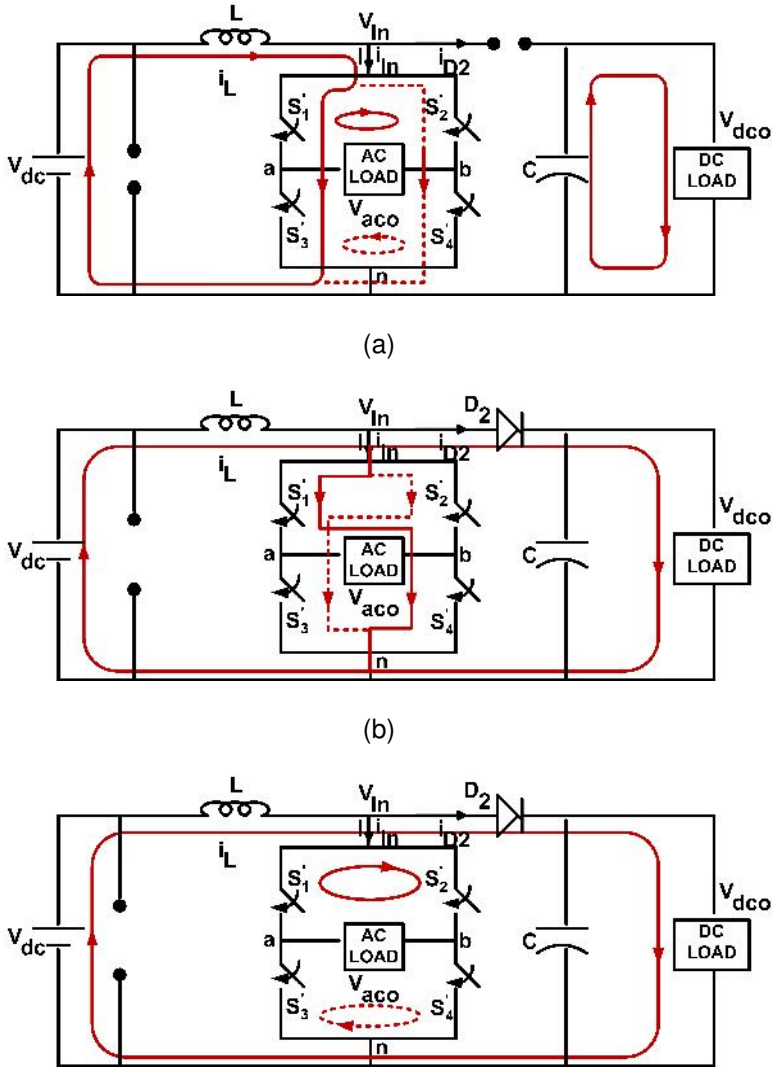


Figure 4.33: Boost operation of NIBBDHC (a) Shoot-through period (b) Power period (c) Zero period.

4.9.3 Steady-state analysis

4.9.3.1 DC and AC output voltage gains

The DC voltage gain of NIBBDHC is analogous to the voltage gain expression of conventional two switch non inverting buck boost converter, which will be expressed in terms of duty cycle of switch S_1 (D_{st2}) and shoot-through period (D_{st1}). Hence, DC voltage gain is given as

$$\frac{V_{dco}}{V_{dc}} = \frac{D_{st2}}{1 - D_{st1}} \tag{4.202}$$

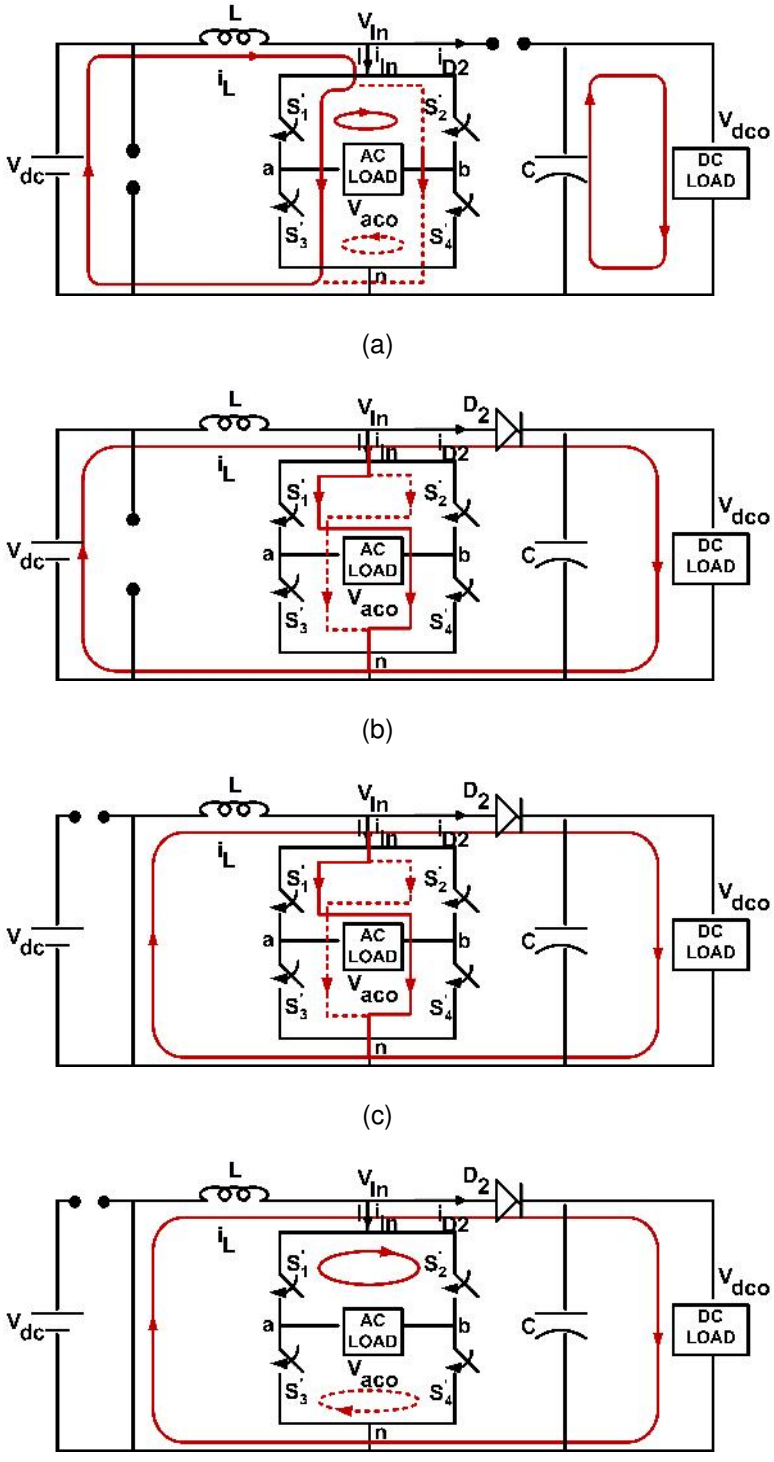


Figure 4.34: Buck operation of NIBBDHC (a) Shoot-through period (b) and (c) Power period (d) Zero period.

The AC voltage gain can be expressed in terms of modulation index (M_a), duty cycle of switch S_1 (D_{st2}) and shoot-through period (D_{st1}). Hence, AC voltage gain is given as

$$\frac{V_{aco(peak)}}{V_{dc}} = \frac{M_a}{1 - D_{st1}} \times D_{st2} \tag{4.203}$$

Here, the operation limit is sum of modulation index (M_a) and shoot-through period (D_{st1}) should not exceed unity, which is given in (4.204). The reason for this, as it exceeds unity, zero period is going to vanish.

$$M_a + D_{st1} \leq 1 \tag{4.204}$$

Some important observations from (4.203) and (4.204) are

1. Maximum value of AC output voltage peak is equal to the input voltage. This is also possible in boost operating conditions only (i.e., $D_{st2} = 1$).
2. There is no limitation on duty cycle of switch S_1.

4.9.3.2 Output power expressions

From (4.202) and (4.203), the output DC power (P_{dc}) and output AC power (P_{ac}) can be written as follows

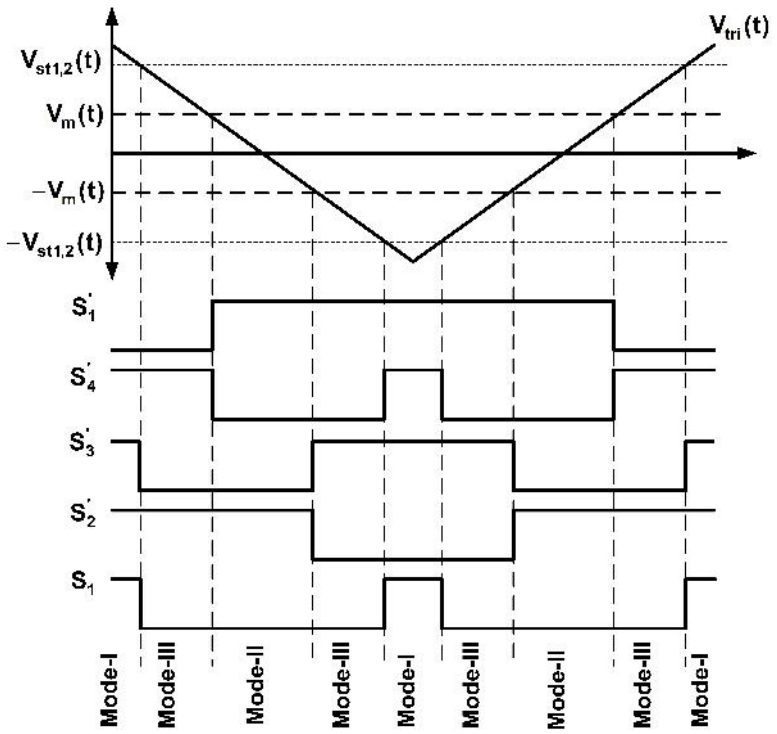
$$P_{dc} = \frac{V_{dc}^2 \times D_{st2}^2}{R_{dc} \times (1 - D_{st1})^2} \tag{4.205}$$

$$P_{ac} = \frac{0.5 \times V_{dc}^2 \times M_a^2 \times D_{st2}^2}{R_{ac} \times (1 - D_{st1})^2} \tag{4.206}$$

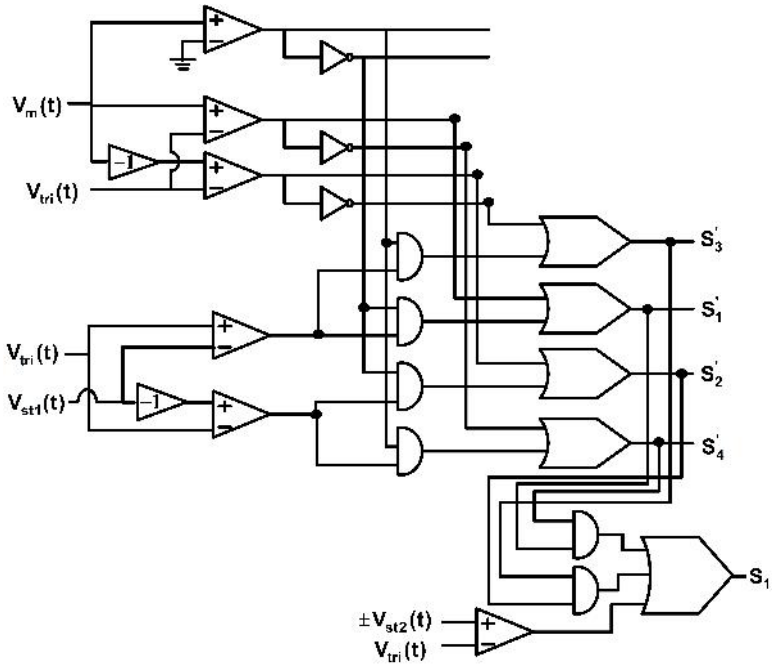
where, R_{ac} and R_{dc} are the AC and DC output resistances, respectively.

4.9.4 Switching pulses generation

The control technique is based on the unipolar sinusoidal PWM technique. The control scheme of NIBBDHC is similar to the PWM scheme proposed in [77]. This PWM scheme will generate pulses for the inverter switches (S_1' to S_4') only. But, NIBBDHC have one more switch S_1 and pulses for this are generated with some appropriate modification.



(a)



(b)

Figure 4.35: (a) PWM pulses for switches (b) Implementation of PWM control scheme.

The control scheme and pulse generation for inverter switches and switch S_1 are shown in Figure 4.35(a). The implementation of this control is shown in Figure 4.35(b). A DC signal ($V_{st1}(t)$) and sine wave($v_m(t)$) are compared with a high frequency carrier signal ($v_{tri}(t)$) to generate PWM pulses for the switches of inverter bridge. The constraint here deduced from the inequality (4.204) as follows:

$$|v_m| \leq |V_{st1}| \tag{4.207}$$

Another DC signal ($V_{st2}(t)$) is compared with carrier signal ($v_{tri}(t)$) to generate PWM pulses for the switch S_1 as given in Figure 4.35(b). There is no constraint for this signal magnitude. Basically, the buck, boost and buck-boost operating conditions are based on magnitude of $V_{st2}(t)$.

4.10 Hardware Implementation

The investigation of proposed NIBBDHC is done by considering the following parameters as shown in Table 4.5. The simulations of presented topology is carried out under open-loop conditions in MATLAB/SIMULINK and experiments are also performed. The results of NIBBDHC is taken under different operating conditions. Hardware prototype of proposed converter is shown in Figure 4.36.

Note: As the proposed converter is of hybrid type, the closed-loop control is out of scope for this thesis. Closed loop control is one of the future work.

Table 4.5: Parameters of proposed NIBBDHC converter

Parameters	Ratings
Inductor (L)	5mH
Capacitor (C)	1000uF
Input DC voltage (V_{dc})	12V
DC load resistance (R_{dc})	20Ω
AC load resistance (R_{ac})	20Ω
Switching frequency (f)	10KHz

Figure 4.36: Experimental set-up.

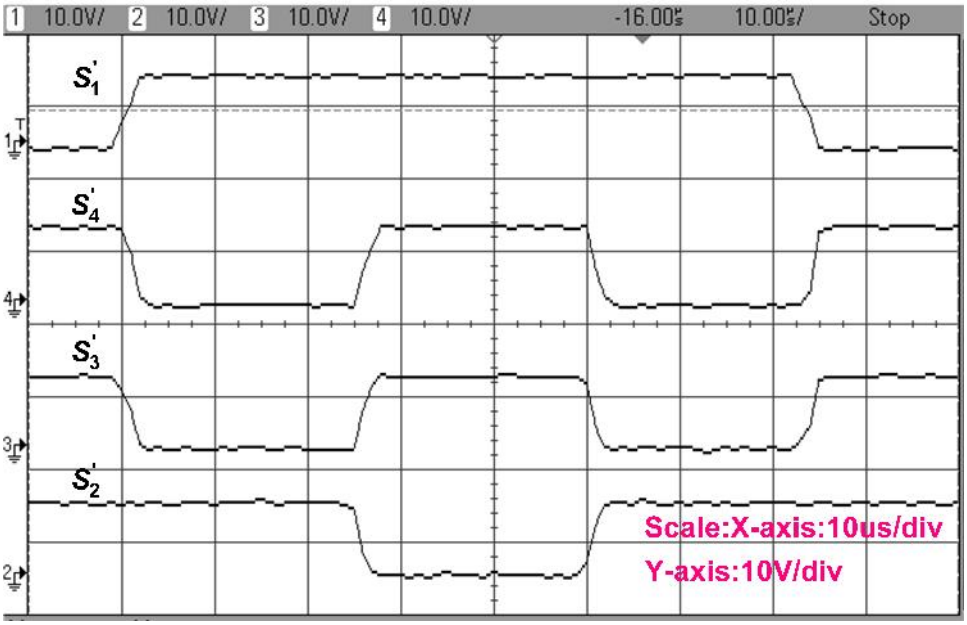
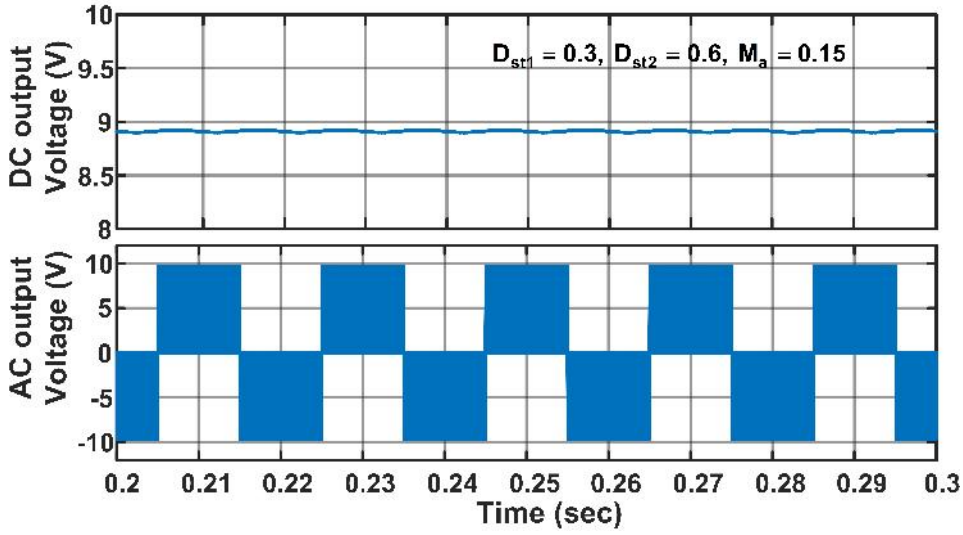
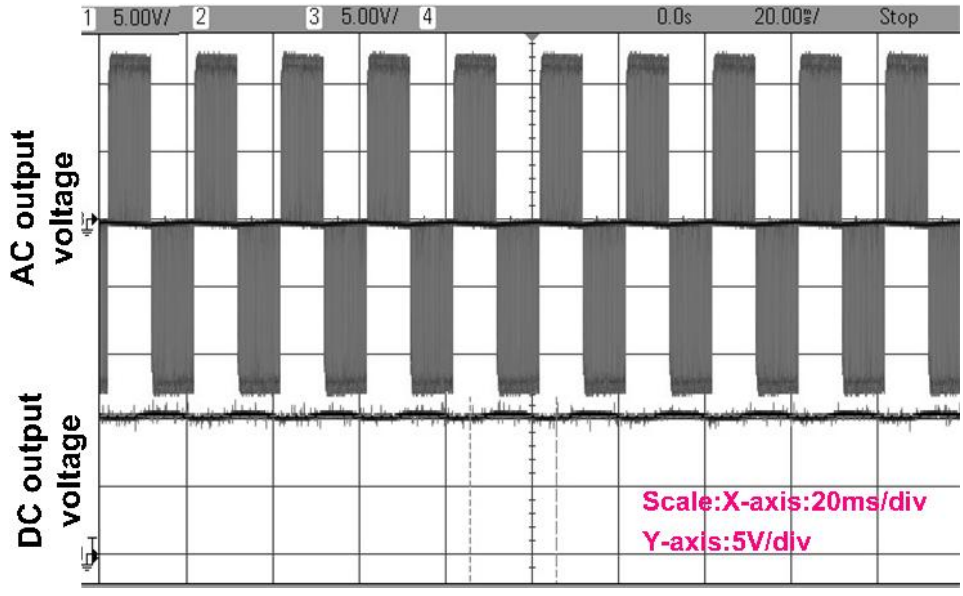


Figure 4.37: Switching pulses.

A. Buck operating conditions: Simulation and experimental results of NIBBDHC, under buck operating condition output DC and AC voltages are shown in Figure 4.38(a) and Figure 4.38(b), respectively. Parameters considered for results shown are $D_{st2} = 0.6$,$D_{st1} = 0.3$, and $M_a = 0.15$.



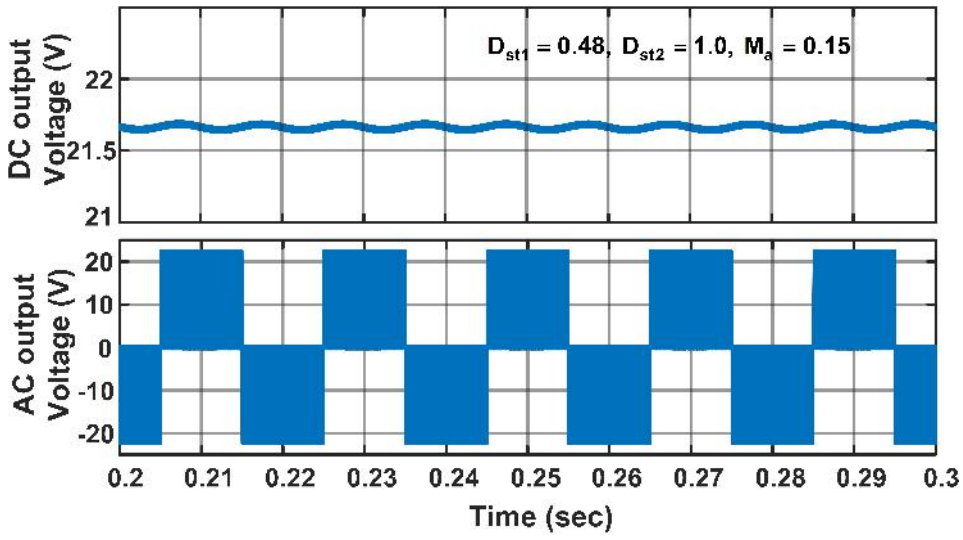
(a)



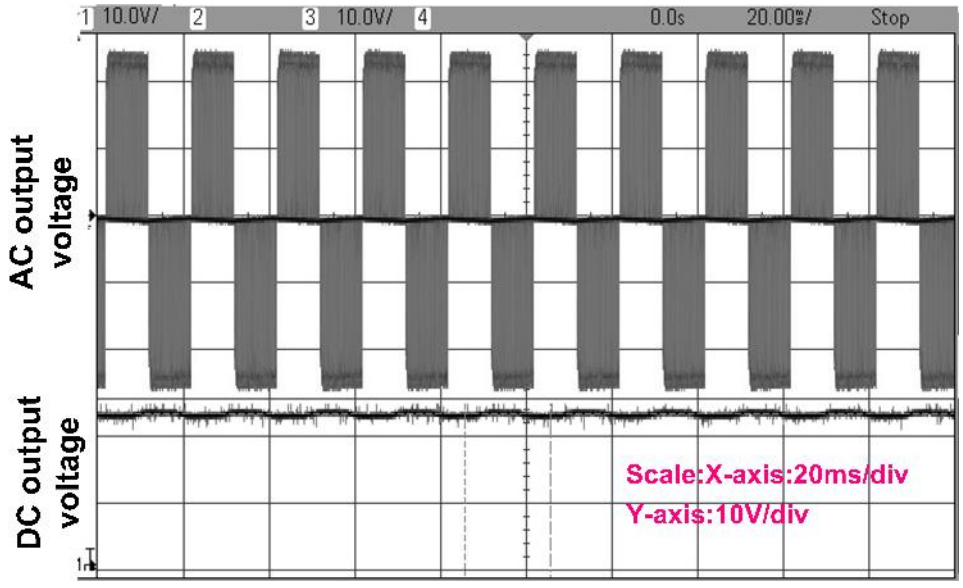
(b)

Figure 4.38: Buck operation of NIBBDHC (a) Simulation (b) Experimental.

B. Boost operating conditions: Simulation and experimental results of NIBB-DHC, under boost operating condition output DC and AC voltages are shown in Figure 4.39(a) and Figure 4.39(b), respectively. Parameters considered for results are $D_{st2} = 0.48$,$D_{st1} = 1.0$, and $M_a = 0.15$.



(a)



(b)

Figure 4.39: Buck operation of NIBBDHC (a) Simulation (b) Experimental.

C. Buck-boost operating conditions: Simulation and experimental results of NIBB-DHC, under buck-boost operating condition output DC and AC voltages are shown in Figure 4.40 and Figure 4.41, respectively. Parameters considered for results shown in Figure 4.40(a) and Figure 4.41(a) are $D_{st2} = D_{st1} = 0.3,$ and $M_a = 0.15$. Parameters considered for results shown in Figure 4.40(b) and Figure 4.41(b) are $D_{st2} = D_{st1} = 0.7,$ and $M_a = 0.15$.

4.10.1 Comparison of proposed NIBBDHC with existing topologies

The proposed NIBBDHC has many advantages compared to conventional converters in terms of number of switches, shoot-through issue etc. Merits of proposed NIBBDHC as follows:

1. Shoot-through issue in normal inverter bridge is utilized for the operation of proposed topology. So, EMI problems are eliminated.

2. Dead time circuits are also not essential as these are required in normal VSC.

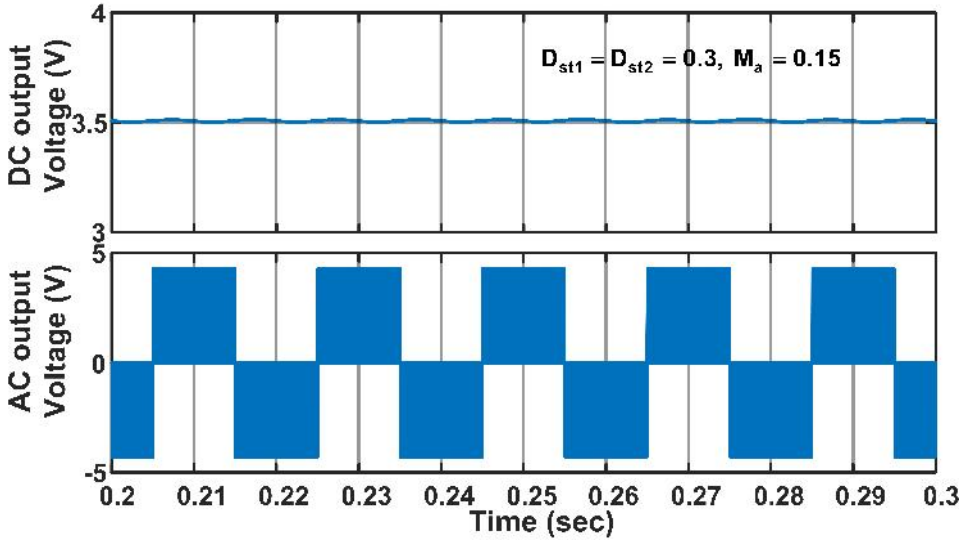
3. The number of semi-conductor switches required are less when compared to a non-inverting buck boost converter topology cascaded with VSC.

4. Here, the maximum duty cycle of converter is not limited by 0.5 as in ZSI. As per the requirement, it can operate only for generating DC.

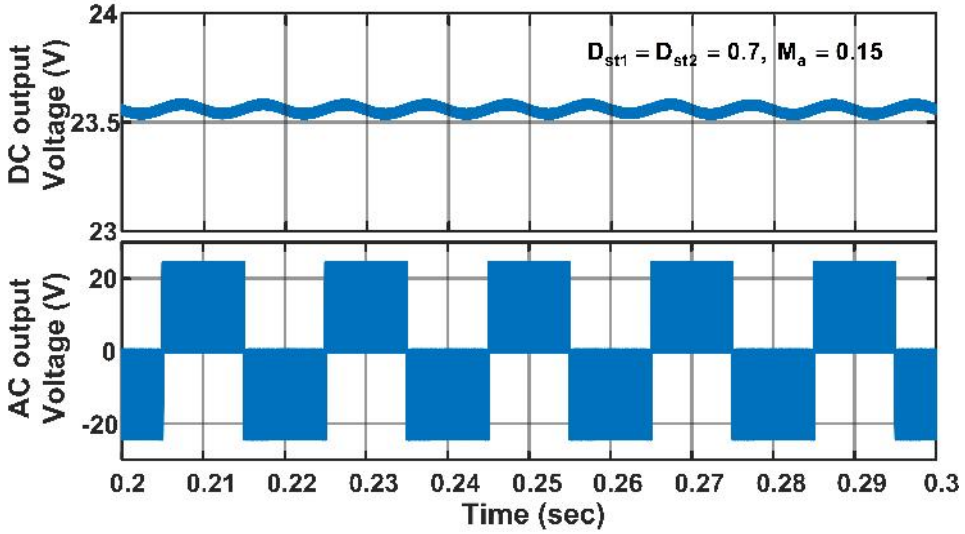
5. The proposed topology is used for generating both AC and DC simultaneously as in BDHC [74]. But, this can also operated in buck and boost operations.

6. Proposed NIBBDHC can provide output without inversion, not as in cuk-DHC [75]. Further, cuk-DHC has four passive elements, whereas proposed NIBB-DHC has only one inductor and capacitor.

7. Proposed NIBBDHC can be operated in buck and boost modes for both DC and AC loads, which is not possible in CFSI [76].



(a)

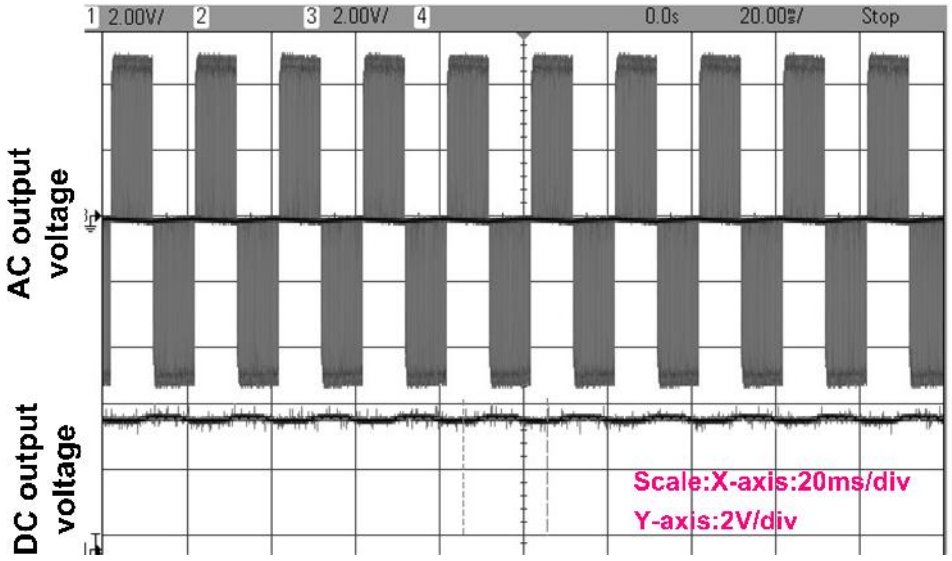


(b)

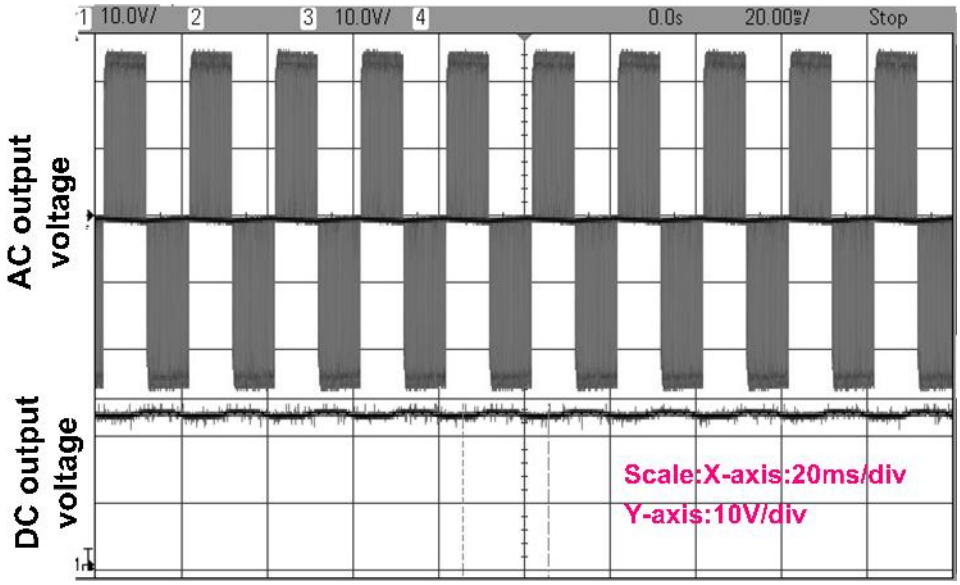
Figure 4.40: Buck-boost operation of NIBBDHC (Simulation) (a) Buck mode (b) Boost mode.

4.11 Conclusions

The analysis of NIBB converter is carried out in a similar way to the boost and buck-boost converters. But, as NIBB converter has two switches and three operating modes, analysis is done in different way. Here also, an improved duty cycle relationships for a non-ideal DC-DC PWM NIBB converter has been derived and also



(a)



(b)

Figure 4.41: Buck-boost operation of NIBBDHC (Experimental) (a) Buck mode (b) Boost mode.

demonstrated that the ideally calculated duty cycle results in lower output voltage than the anticipated value. Both duty cycles expressions are important. Though, the design analysis of inductor and capacitor is very similar to the buck, boost and buck-boost converters, selection is dependent on the mode of operation. The ripple

analysis concludes that the ESR of output filter capacitor effects more on OVR, which is very similar to the previous converter analysis. Conclusively, it is recommended to design engineers to use these modified expressions in accurate design of NIBB converter modules.

Here, we have two duty cycles, so the analysis given to get the overall maximum achievable voltage and duty cycle with the NIBB converter. This information is very crucial for closed-loop operation and also helpful to engineers in control design of DC-DC NIBB converter. Overall, parasitics are enhancing the stability of closed-loop system, which can be negotiated from small-signal analysis. NIBB converter can come under both minimum phase and non-minimum phase type systems.

Eventually, experimental results confirms the importance of non-ideal model of the NIBB converter to estimate the performances of new control techniques. The non-ideal model is resembling the practical system. The analysis of controller performance is very easy. Since all parasitic effect is very clear on transfer function model, it is easy to observe the robust performance of the converter under parametric variations.

Finally, non-inverting buck-boost derived hybrid converter is proposed from the conventional two-switch non-inverting buck-boost converter, which can supply both DC and AC simultaneously. The characteristics and analysis of the proposed converter analyzed through wave forms and equivalent circuit diagrams in different operating conditions. The uniqueness of the proposed converter is shoot-through problem utilization and ability to supply both AC and DC, which makes distinctive from other conventional converters. The validation of converter is carried out by simulation results. From these results, it is clear that the proposed converter able to operate in buck, boost and buck-boost modes. Further, the proposed converter is more flexible to get wider operating range of voltage in comparison to other proposed hybrid converter topologies.

CHAPTER 5

CONTROLLER DESIGN FOR DC-DC CONVERTERS

This chapter presents the controller design for DC-DC Converters. The performance of controllers are validated by simulation and experimental results.

5.1 Background and Motivation

The previous chapters discusses the design and accurate modelling of DC-DC converters. Alongside, the control oriented analysis of models also described. These are the basic steps for any system, before designing the controller. In general, most of the applications require constant or regulated output voltage from DC-DC converters. However, there will be some disturbances in input voltage or loading. So, there may be a chance of fluctuations in output voltage. Hence, a controller is needed to regulate the output voltage. Now the closed-loop controller is to be designed for output voltage regulation of the DC-DC converter.

Some of the problems encountered in the closed-loop operation of converters are as follows or we can say desired features from the closed-loop operation.

- Line rejection or Dynamic line response
- Dynamic load response or Rejection of load disturbances
- Good transient and steady-state response
- Robust stability.

DC-DC converters are typically of minimum and non-minimum phase type. Especially, the problems encountered in DC-DC converters [188]- [190] are

- RHP zero

- Sub-harmonic instability (this exists mainly in current mode control)

- EMI (Electro Magnetic Interference)

As per the transfer function model analysis, the converters considered are non-minimum phase or having RHP zero. The problems with RHP zero explained as follows:

5.1.1 RHP zero

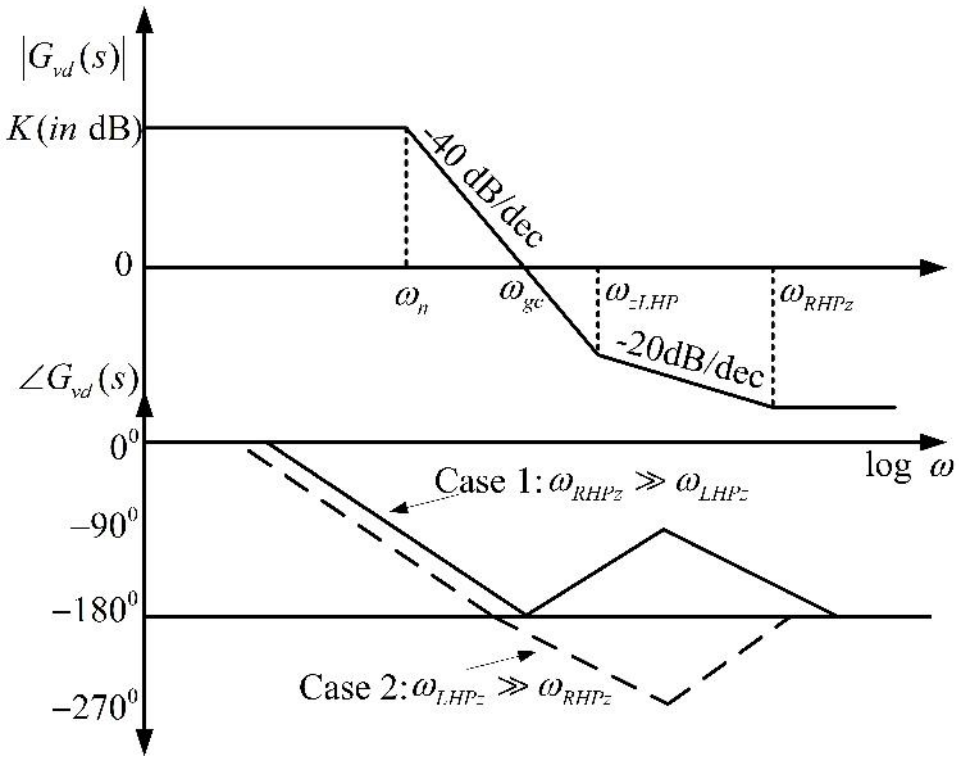


Figure 5.1: Asymptotic frequency response of non-minimum phase systems(boost and buck-boost converters).

The research on problems encountered or effects of RHP zeros on the system is one of the interested topic [190]- [200]. Here, it is explained the challenges with existence of RHP zeros. Consider the complete non-ideal model transfer functions (output voltage to duty cycle) of non-minimum phase type converters in CCM, which

are of the following form.

$$G_{vd}(s) = K_g \frac{\left(1 + \frac{s}{\omega_{LHPz}}\right)\left(1 - \frac{s}{\omega_{RHPz}}\right)}{1 + \left(\frac{s}{\omega_n Q}\right) + \left(\frac{s}{\omega_n}\right)^2}. \tag{5.1}$$

Where, ω_{LHPz} = Frequency of LHP zero due to ESR, ω_{RHPz} = Frequency of RHP zero, ω_n =Pole frequency and Q is quality factor. To analyse Eq. (5.1), the asymptotic frequency response plots are shown in Figure 5.1. This plot shows, two different cases. In both the cases, it is clear that there will be no change in magnitude plot even though RHP zero is present. Where as, change will be observed in phase plot and made the following observations.

Case I: (When $\omega_{LHPz} < \omega_{RHPz}$) The RHP zero $\pi/2$ lag in phase at ω_{RHPz} and force the complete system phase towards π. Hence, controller can be designed to get a crossover frequency well below the RHP zero. So, the maximum achievable bandwidth in this case is

$$\omega_{gc}|_{\max} \leq \omega_{RHPz}. \tag{5.2}$$

Case II: (When $\omega_{LHPz} > \omega_{RHPz}$) This will be the even worst scenario for the system. Since, RHP zero location is ahead of LHP zero, phase of the system will goes to $-3\pi/2$. So bandwidth is restricted more than the previous case and will be less than crossover frequency of the plant without controller (ω_{gco}). So, the maximum achievable bandwidth in this case is

$$\omega_{gc}|_{\max} < \omega_{gco}. \tag{5.3}$$

Generally, selection of gain crossover frequency for switched mode power converters depends on following constraints [195];

- If there is no RHP zero in the system, then the crossover frequency will be one tenth to one fifth of the switching frequency. If it chooses more than this value, then additional problems like noise will be introduced.
- If it is of case I, then the crossover frequency is selected as below 30% of maximum achievable bandwidth of the case.

This analysis will help to design controller for the non-minimum phase plants with desired crossover frequency within achievable limits.

Overall, this section presents the proposed PID controller design for DC-DC converters under following cases:

Case I: When converter parameters are constant.

Case II: When converter parameters are varying within prescribed limits.

In case I, an IMC (Internal Model Control) technique is used to design PID controller. In case II, Kharitonov theorem, stability boundary locus and IMC techniques are used to design robust PID controller for DC-DC converters.

5.2 IMC (Internal Model Control)

The internal model control is a class of control technique which is known to exhibit robustness, sub-optimality, less computational burden, and analytical as well as easily understandable approach. IMC (Internal Model Control), the name itself explains what it is exactly. It means, the controller is derived from the model of the system or plant. This makes IMC standout from the other control techniques. The internal model control (IMC)-based PID controller is widely used in industrial control problems. This scheme provides a good compromise among set-point tracking, disturbance attenuation, and robustness.

5.2.1 IMC structure

The structure of IMC has been evolved from the fundamental feedback control structure; see Figure 5.2(a). On adding and subtracting the plant model in Figure 5.2(a)), as shown in Figure 5.2(b), may lead to an entirely new structure; see Figure 5.2(c). After rearranging and solving the inner loop depicted by dashed line in Figure 5.2(c), the equivalent structure obtained in Figure 5.2(d) is internal model control system. This control structure is so called because the process model is completely an internal part of the controller. It is also sometimes referred as model inverse-based control. Thus, the conversion or synthesis equation of IMC through classical feed-

back form is

$$Q(s) = \frac{C(s)}{1 + G(s)C(s)} \tag{5.4}$$

or

$$C(s) = \frac{Q(s)}{1 - G(s)Q(s)} \tag{5.5}$$

Thus for the LTI systems, the IMC based controller confirms to be an alternate parametrization of a classical controller. The various input/output relations for Figure 5.2(d) are

$$\hat{n} = \left[G(s) - \tilde{G}(s)\right] u(s) + d(s) \tag{5.6}$$

$$u(s) = \left[R(s) - \hat{n}\right] Q(s) \tag{5.7}$$

$$u(s) = \frac{Q(s)}{1 + Q(s)\left(G(s) - \tilde{G}(s)\right)} \left(R(s) - d(s)\right) \tag{5.8}$$

$$Y(s) = d(s) + \frac{G(s)Q(s)}{1 + Q(s)\left(G(s) - \tilde{G}(s)\right)} \left(R(s) - d(s)\right) \tag{5.9}$$

or

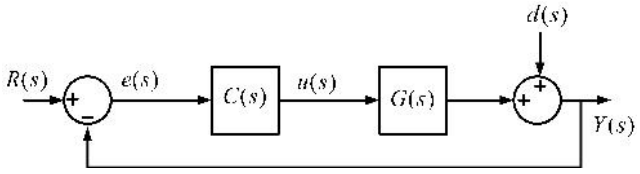
$$Y(s) = \underbrace{\frac{G(s)Q(s)}{1 + Q(s)\left(G(s) - \tilde{G}(s)\right)}}_{S} R(s) + \underbrace{\frac{\left(1 - \tilde{G}(s)Q(s)\right)}{1 + Q(s)\left(G(s) - \tilde{G}(s)\right)}}_{S'} d(s) \tag{5.10}$$

where, S=Sensitivity and S'= Complimentary sensitivity.

5.2.2 IMC properties

The three salient features of IMC structure have evoked the concept of controller design. These properties are as follows [128].

1. **Dual Stability Criterion:**The closed-loop stability of a system is governed by the stability of the plant and controller individually.



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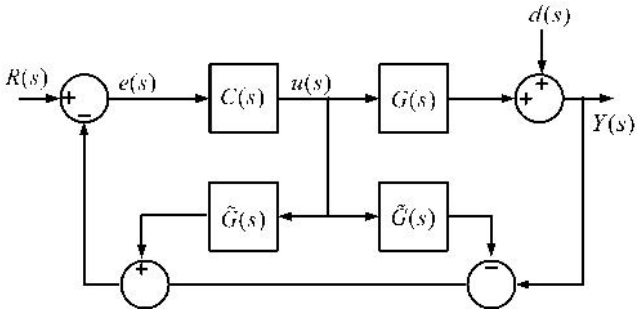

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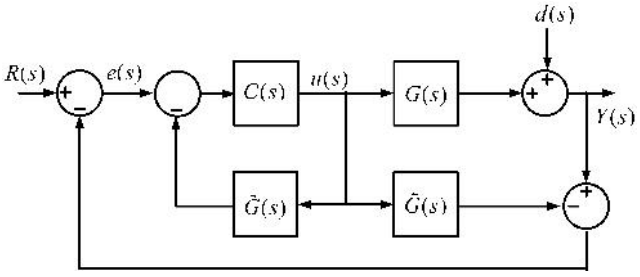

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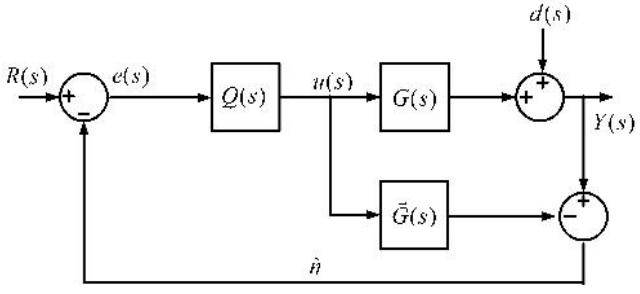


(d)

Figure 5.2: Schematic of (a)Classical feedback structure (b)-(d)IMC evolution.

In the absense of MPM (Model Plant Mismatch) (*i.e.,*$G(s) = \tilde{G}(s)$), the closed-loop transfer function (5.10) reduces to

$$Y(s) = [G(s)Q(s)]\, R(s) + \left[1 - \tilde{G}(s)Q(s)\right] d(s) \tag{5.11}$$

Thus, if the plant is open loop stable, the closed-loop stability is ensured if the controller is chosen to have stable poles.

2. **Perfect Controller:**Ideally, perfect tracking with full disturbance rejection is achieved in IMC structure when the controller is equivalent to inverse of the stable plant.

$$G(s) = \tilde{G}(s); C(s) = G(s)^{-1} \tag{5.12}$$

3. **Zero Offset:** The steady state value of output is free from offset if the following conditions hold.

   As we know, for zero steady state error is $\lim_{s\to 0} se(s) = 0$. Here, $e(s)$ is

$$e(s) = \frac{1 - Q(s)\tilde{G}(s)}{1 + Q(s)\left[G(s) - \tilde{G}(s)\right]} R(s) \tag{5.13}$$

   For step input $R(s) = \frac{1}{s}$, steady state error will be

$$\lim_{s\to 0} e(s) = 0 \Rightarrow \lim_{s\to 0} \frac{1-Q(s)\tilde{G}(s)}{1+Q(s)\left[G(s)-\tilde{G}(s)\right]} = 0 \Rightarrow \lim_{s\to 0} [1 - Q(s)G(s)] = 0 \tag{5.14}$$

   Here, steady-state error will be zero for $Q(0) = \frac{1}{\tilde{G}(0)}$.

   Now, for ramp input $R(s) = \frac{1}{s^2}$, steady state error will be

$$\lim_{s\to 0} \frac{e(s)}{s} = 0 \Rightarrow \lim_{s\to 0} \left[\frac{1 - Q(s)\tilde{G}(s)}{1 + Q(s)\left[G(s) - \tilde{G}(s)\right]}\right] \frac{1}{s} = 0 \tag{5.15}$$

   Here, steady-state error will be zero if $\left.\frac{d\left[1-Q(s)\tilde{G}(s)\right]}{ds}\right|_{s=0} = 0$ and $Q(0) = \frac{1}{\tilde{G}(0)}$.

   Similarly, for generalized input like $R(s) = \frac{1}{s^{k+1}}$, steady-state error will be

$$\lim_{s\to 0} \frac{e(s)}{s^k} = 0 \Rightarrow \lim_{s\to 0} \left[\frac{1 - Q(s)\tilde{G}(s)}{1 + Q(s)\left[G(s) - \tilde{G}(s)\right]}\right] \frac{1}{s^k} = 0 \tag{5.16}$$

Here, steady-state error will be zero if $\left.\frac{d\left[1-Q(s)\tilde{G}(s)\right]}{ds^m}\right|_{s=0} = 0$ for $m = 1, 2...k$ and $Q(0) = \frac{1}{\tilde{G}(0)}$.

5.2.3 Issues with IMC

The designed $Q(s)$ must be stable, proper and casual. Further, it should be realizable. In order to design controller, the following issues may arises.

- From properties 1 and 2, it is clear that controller should be inverse of the plant model. This will be problematic for NMP systems and delayed systems, since for NMP systems, the designed controller will be unstable. To resolve this issue, factorize numerator as MP and NMP parts and use only MP part for controller design.

- In attaining inverse, some cases Q will become improper (*i.e.,* numerator degree will be more than denominator). So, it is difficult to realize the controller practically. To address this issue, an additional filter is to be added, which makes overall system proper.

- In practical implementations, there is always a MPM (Model Plant Mismatch) due to approximate or ideal modelling. Thus, a filter is needed to address this problem.

5.2.4 IMC filter

From the above discussion, it can be concluded that the filter is needed to design a controller. The designed filter is expected to have following properties:

- The controller should become proper or realizable

- It should provide robustness against MPM, disturbance/noise rejection.

- It is very important that, it should not add offset to the system.

So, from this it is clear that the filter should have low pass characteristics and can be selected as follows: From property 3 and Eq.(5.14)-(5.16), it can written as

$$Q(0)\tilde{G}(0) = 1 \Rightarrow \left[G^{-1}(0)F(0)\right]\tilde{G}(0) = 1 \Rightarrow F(0) = 1. \tag{5.17}$$

Therefore a low pass filter, which satisfies relation (5.17), can be chosen as

$$F(s) = \frac{1}{(\lambda s + 1)^n} \tag{5.18}$$

where, λ is tuning parameter and n is order of the filter which makes the whole controller proper.

Sometimes, the filter can be chosen in following form:

$$F(s) = \frac{\alpha_2 s^2 + \alpha_1 s + \alpha_0}{(1 + \lambda s)^n} \tag{5.19}$$

where, $\alpha_0, \alpha_1, \alpha_2$ are parameters that help to suppress noise or input disturbance rejection.

5.2.5 IMC-PID design procedure

Consider a stable proper finite dimensional plant as,

$$G(s) = K\frac{N(s)}{D(s)} \tag{5.20}$$

where $K > 0$, $N(s) = \sum_{i=0}^{n} n_i s^i$, $n_i \in \mathbb{R}$, $D(s) = \sum_{i=0}^{n+1} d_i s^i$, $d_i > 0$, and $n \in \mathbb{N}$.

Step 1: Factorize the plant model given in (5.20) as minimum phase (MP) and non-minimum phase (NMP) parts. So, we can write,

$$G(s) = G^{+}(s)G^{-}(s). \tag{5.21}$$

Where, $G^{+}(s) = K\frac{N^{+}(s)}{D(s)}$ and $G^{-}(s) = K\frac{N^{-}(s)}{D(s)}$ are minimum and non-minimum phase parts of plant model, respectively.

Step 2: The IMC controller is obtained by

$$Q(s) = G^{+}(s)^{-1}F(s) \tag{5.22}$$

Where, $F(s)$ is filter used in IMC controller $Q(s)$ and $F(s) = 1/f(s)$ where $f(s) = (\lambda s + 1)^n$, $n \in \mathbb{N}$, $\lambda > 0$.

Step 3: Obtaining PID parameters

Substituting $Q(s)$ in (5.5), we get

$$C(s) = \frac{G^+(s)^{-1}}{f(s) - 1} \Rightarrow C(s) = \frac{D(s)}{N^+(s)K\lambda s} \tag{5.23}$$

Further, the above equation can be restructured as

$$C(s) = K_p + \frac{K_i}{s} + K_d s \tag{5.24}$$

where, K_p=Proportional gain, K_i= Integral gain, K_d= Derivative gain.

From (5.23)-(5.24), it is clear that the controller gains are function of λ. So, there is need to tune only one parameter (*i.e.,*λ) to get controller gains.

5.2.6 λ selection

Evaluating λ is always an important issue in IMC design because it is the only parameter, which completes the design. It is observed that the smaller values of λ gives the fast speed of response and more bandwidth of the closed-loop system. For larger the value of λ gives the slow response, smaller the action of the manipulated variable and lesser bandwidth of the closed-loop system.

Thus, λ is related to bandwidth. Similarly, DC-DC converters speed of response is also related to bandwidth (bandwidth should be one tenth to one fifth of switching frequency of DC-DC converter). So, by choosing λ in relation to bandwidth, it will be better for DC-DC Converters. Here, we proposes λ for obtaining desired gain crossover frequency for DC-DC converters.

5.2.6.1 Proposed λ for DC-DC converters

The tuning principle follows the concept of Bode's ideal transfer function.

Consider an integrating type system in a feed forward path in classical control loop

with gain k as

$$L(s) = C(s)P(s) = \frac{k}{s} \tag{5.25}$$

then the gain crossover frequency (ω_{gc})

$$\omega_{gc} = k \tag{5.26}$$

and phase margin $\phi = \pi/2$. It means that, ω_{gc} varies with k, however ϕ is insensitive to k. Now, the closed-loop system is given by

$$T(s) = \frac{L(s)}{1 + L(s)} = \frac{1}{1 + {}^{s}/_{k}} \tag{5.27}$$

Thus, the system exhibits infinite gain margin with the constant phase margin.

Lemma 1 [201]: The closed-loop transfer function of controlled system is equivalent to IMC filter when plant and model are same and controller is designed via IMC scheme.

Therefore, using aforementioned lemma, we can state that the closed-loop transfer function is equivalent to the filter. So, it can be treated as a reference model as given in (5.25), *i.e.*,

$$T(s) = F(s) = \frac{1}{1 + \lambda s} \tag{5.28}$$

where $\lambda = \frac{1}{k}$. Now from (5.26), the gain crossover frequency is given by

$$\lambda = \frac{1}{\omega_{gc}} \tag{5.29}$$

5.2.7 IMC-PID design for converters exhibiting minimum phase (MP) behaviour

As discussed in previous sections, DC-DC buck converter is one of the example for minimum phase behaviour.

5.2.7.1 IMC-PID for buck converter

Consider buck converter transfer function, which is the second-order system with one left half plane (LHP) zero as shown in (4.160).

Step 1: Factorizing the plant model, we get only MP part ($G^+(s)$) and no NMP part ($G^-(s)$) as buck transfer function have only one LHP zero. Here,

$$N^+(s) = n_1 s + n_0 \tag{5.30}$$

and

$$D(s) = d_2 s^2 + d_1 s + d_0 \tag{5.31}$$

Step 2: The IMC-PID controller obtained by substituting (5.30) and (5.31) in (5.23), we get,

$$C(s) = \left(k_p + \frac{k_i}{s} + k_d s\right) \frac{1}{N^+(s)} \tag{5.32}$$

where,

$$K_p = \frac{d_1}{K\lambda}, K_i = \frac{d_0}{K\lambda}, K_d = \frac{d_2}{K\lambda} \tag{5.33}$$

Note: Equation (5.33) states that, $C(s)$ acquires PID form followed by a lag term $\frac{1}{N^+(s)}$.

Step 3: The λ will be as given in (5.29), which gives desired gain crossover frequency.

On substituting d_0, d_1 and d_2 from (4.160) in (5.33), we get controller parameters in terms of buck converter parameters as:

$$k_p = \frac{\left(\frac{L}{R} + \frac{Cr_c}{R} + C\left(r_L + D\left(r_g + r_{on}\right) + D' r_d\right)\left(1 + \frac{r_c}{R}\right)\right)}{\omega_{gc}{}^{-1}\left(V_g\left(1 + \frac{r_L}{R} + \frac{r_d}{R}\right) + V_{fd}\left(1 + \frac{r_L}{R} + \frac{r_g}{R} + \frac{r_{on}}{R}\right)\right)} \tag{5.34}$$

$$k_i = \frac{\left(1 + \frac{r_L}{R} + D\left(\frac{r_g}{R} + \frac{r_{on}}{R}\right) + D'\left(\frac{r_d}{R}\right)\right)^2}{\omega_{gc}{}^{-1}\left(V_g\left(1 + \frac{r_L}{R} + \frac{r_d}{R}\right) + V_{fd}\left(1 + \frac{r_L}{R} + \frac{r_g}{R} + \frac{r_{on}}{R}\right)\right)} \tag{5.35}$$

$$k_d = \frac{LC}{\omega_{gc}{}^{-1}} \frac{\left(1 + \frac{r_c}{R}\right)\left(1 + \frac{r_L}{R} + D\left(\frac{r_g}{R} + \frac{r_{on}}{R}\right) + D'\left(\frac{r_d}{R}\right)\right)}{\left(V_g\left(1 + \frac{r_L}{R} + \frac{r_d}{R}\right) + V_{fd}\left(1 + \frac{r_L}{R} + \frac{r_g}{R} + \frac{r_{on}}{R}\right)\right)} \tag{5.36}$$

In case of ideal transfer function, the tuning constants (k_{po}, k_{io}, k_{do}) are as follows:

$$k_{po} = \frac{L}{\omega_{gc}{}^{-1} R V_g},\ k_{io} = \frac{1}{\omega_{gc}{}^{-1} V_g},\ k_{do} = \frac{LC}{\omega_{gc}{}^{-1} V_g}$$

Hence, there is no trial and error to choose λ and desired bandwidth can be obtained. Now, this will be explained by illustrative example through simulation and experimental verification.

Simulation and Experimental validation:

Consider a linear plant transfer function of non-ideal buck converter as given in (5.37),

$$G_{vd}(s) = \frac{2522.8(s + 10^5)}{s^2 + 1816s + 2.086 \times 10^7} \tag{5.37}$$

Here, converter switching frequency is $f = 20$kHz. Main contribution is to get PID parameters for various gain crossover frequencies. So, the PID parameters for buck converter given in (5.37) at any ω_{gc} can be calculated by substituting values from (5.37) in (5.33), we get controller parameters as

$$K_p = \frac{1816}{2522.8\omega_{gc}}, K_i = \frac{2.086 \times 10^7}{2522.8\omega_{gc}}, K_d = \frac{1}{2522.8\omega_{gc}} \tag{5.38}$$

Here in Table (5.1), for different ω_{gc}, the PID values are shown.

Table 5.1: IMC-PID values for buck converter (from non-ideal model)

ω_{gc}	0.5kHz	1kHz	1.5kHz	2kHz	2.5kHz	3kHz	3.5kHz
K_p	2.2614e3	4.522e3	6.784e3	9.0457e3	1.1307e4	1.3568e4	1.583e4
K_i	2.5976e7	5.195e7	7.7929e7	1.039e8	1.2988e8	1.5586e8	1.8183e8
K_d	1.2452	2.49	3.735	4.9811	6.2264	7.4717	8.717

The simulation studies are carried out as following two ways:

I.Linear: The results are obtained by using a linear transfer function model given by (5.37). The corresponding results are shown in Figure 5.3.

II. Non-linear: The results are obtained by a analogous model to practical set-up, which is developed in SIMULINK using Sim-PowerSystems Toolbox. The corresponding results are shown in Figure 5.3.

The validation of controller performance is observed from simulations and experiment results. The simulation results of overall system transient response is shown in

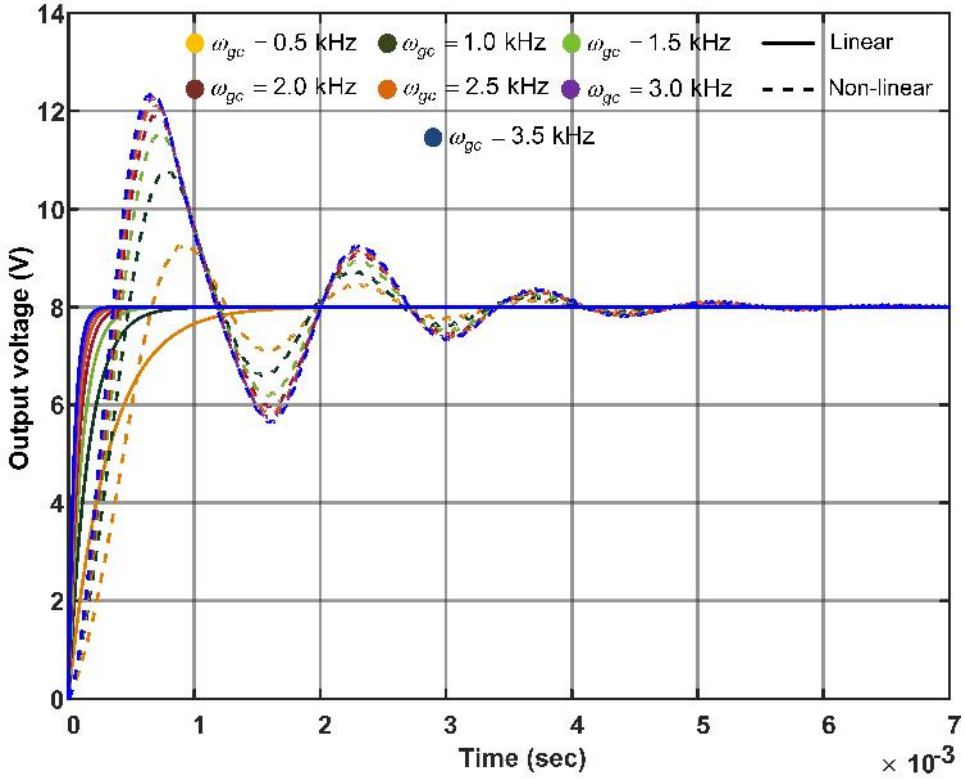


Figure 5.3: Simulation of output voltage at different gain crossover frequencies.

Table 5.2: Performance indices

ω_{gc}	t_r(ms)			t_s(ms)			M_p(%)		
	Sim		Exp	Sim		Exp	Sim		Exp
	L	NL		L	NL		L	NL	
0.5kHz	0.73	0.59	0.66	2.8	4	4	0	15.25	14.6
1.0kHz	0.36	0.43	0.44	1.4	4	4	0	34.3	32.3
1.5kHz	0.24	0.38	0.41	1.1	4	4	0	44	34.8
2.0kHz	0.18	0.36	0.37	0.9	4	6.5	0	48.75	29.8
2.5kHz	0.14	0.34	0.34	0.8	4	4.5	0	51.6	35.8
3.0kHz	0.12	0.33	0.34	0.68	4	6	0	53.5	48.9
3.5kHz	0.1	0.32	0.31	0.39	4	6	0	54.6	50.5

Sim-Simulation, Exp-Experimantal, L-Linear model, NL-Non-linear (Simulink) model

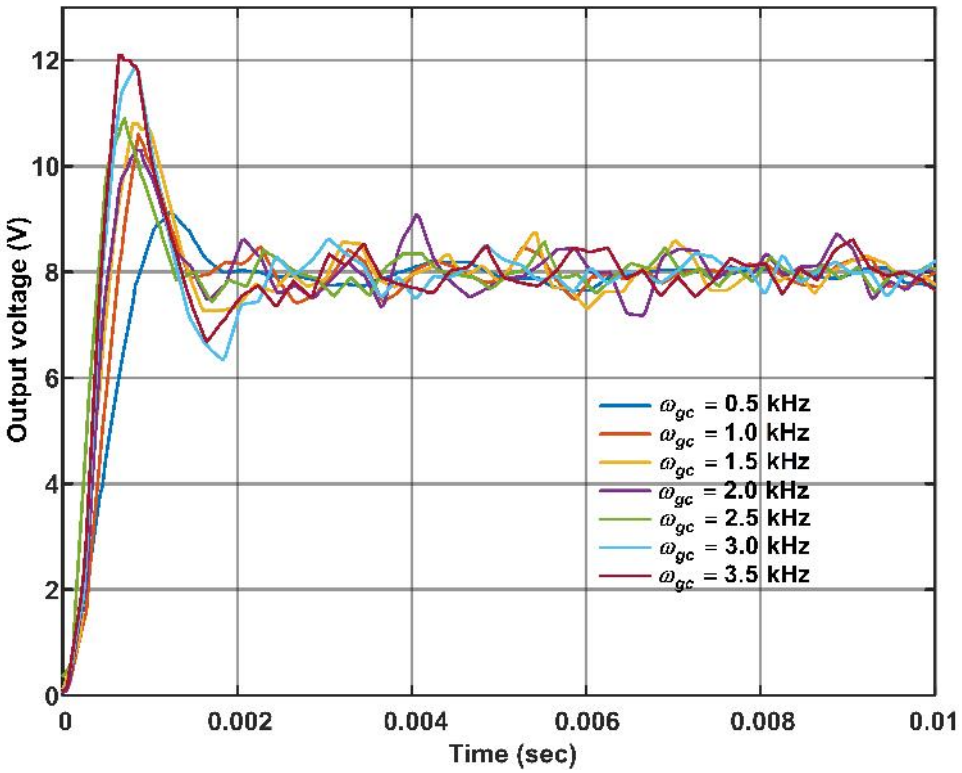


Figure 5.4: Experimental of output voltage at different gain crossover frequencies.

Figure 5.3. There is a peak in results, which are obtained by non-linear model. The reason is that the PID parameters are calculated from linearised model. Further, experimental results are shown in Figure 5.4, which is clearly having overshoot as in non-linear simulation results. The performance comparison also tabulated in Table 5.2. It is well-known that the as gain crossover frequency increases, the speed of response is improved. This can be clearly observed from the results.

Here, the key point or contribution is that there is no trial and error procedure used for tuning and if plant model is known and PID can be designed very easily.

5.2.8 IMC-PID design for converters exhibiting non-minimum phase (NMP) behaviour

As discussed in previous sections, DC-DC boost, buck-boost and NIBB converters are the examples for non-minimum phase behaviour.

From mathematical modelling of DC-DC boost converter, we get RHP zero in the

system transfer function model. Such system has undershoot for step changes in output. Further, with PID controller, the proportional action further enhances undershoot in the simulation. However, the practical boost convert doesn't has undershoot because of reverse biasing of diode. Therefore, to have viability of theory and practice, the undershoot effect can be removed by approximating the RHP zero as a delay in the transfer function of the system. However, while designing IMC controller, the RHP zero will be used. The delay is approximated with a first-order Taylor series approximation as

$$e^{-\omega_{RHPz}s} = -\omega_{RHPz}s + 1 \tag{5.39}$$

The various steps to design controller is given below,

Step 1: Factorizing the plant model, we get MP part ($G^{+}(s)$) and NMP part ($G^{-}(s)$) for each boost, buck-boost and NIBB converters (These are having on LHP and one RHP zeros in transfer functions). In general, we can write,

$$N^{+}(s) = (\omega_{LHPz})^{-1}s + 1 \tag{5.40}$$

$$N^{-}(s) = -(\omega_{RHPz})^{-1}s + 1 \tag{5.41}$$

$$D(s) = (\omega_n)^{-2}s^2 + (\omega_n Q)^{-1}s + 1 \tag{5.42}$$

Step 2: The IMC-PID controller is obtained by substituting (5.40)-(5.42) in (5.23), we get

$$C(s) = \left(K_p + \frac{K_i}{s} + K_d s\right)\frac{1}{f(s) - N^{-}(s)}. \tag{5.43}$$

Step 3: The λ will be as given in (5.29), which gives desired gain crossover frequency.

On substituting d_0, d_1 and d_2 from (5.42) in (5.33), we get controller parameters in terms of converter parameters as:

$$K_p = \frac{(Q\omega_n)^{-1}}{K(\lambda + (\omega_{RHPz})^{-1})}, \tag{5.44}$$

$$K_i = \frac{1}{K(\lambda + (\omega_{RHPz})^{-1})}, \tag{5.45}$$

$$K_d = \frac{(\omega_n)^{-2}}{K(\lambda + (\omega_{RHPz})^{-1})}. \tag{5.46}$$

5.2.8.1 IMC-PID for boost converter

Here, we present the performance of the designed IMC-PID when implemented on a DC-DC boost converter.

Simulation and Experimental validation:

Consider the transfer function of non-ideal boost converter is given in (2.143) as,

$$G_{vd}(s) = \frac{14.25\left(\frac{s}{37880}+1\right)\left(-\frac{s}{23620}+1\right)}{\left(\frac{s}{2324.435}\right)^2 + \frac{s}{2275.9}+1} \tag{5.47}$$

or in terms of SOPTD as,

$$G_{vd}(s) = \frac{14.25\left(\frac{s}{37880}+1\right)\left(e^{-\frac{s}{23620}}\right)}{\left(\frac{s}{2324.435}\right)^2 + \frac{s}{2275.9}+1} \tag{5.48}$$

Here, converter switching frequency is $f = 20$kHz. Main contribution is to get PID parameters for various gain crossover frequencies. But, in this converter, there is a RHP zero, which limits gain crossover frequency. The maximum achievable gain crossover frequency depends on the RHP zero position as discussed in previous sections. As per discussion, the boost converter transfer function given in (5.47) falls under case II (*i.e.,*$\omega_{LHPz} > \omega_{RHPz}$). Hence, crossover frequency should be selected as given in Eq. (5.3) (*i.e.,* less than $\omega_{gco} = 1490kHz$). So, the PID parameters for boost converter at any ω_{gc} can be calculated by substituting values from (5.47) in (5.44-5.46), we get controller parameters as given in Table 5.3.

The simulation studies are carried out as following two ways:

I.Linear: The results are obtained by using a linear transfer function model given by (5.47). The corresponding results are shown in Figure 5.5.

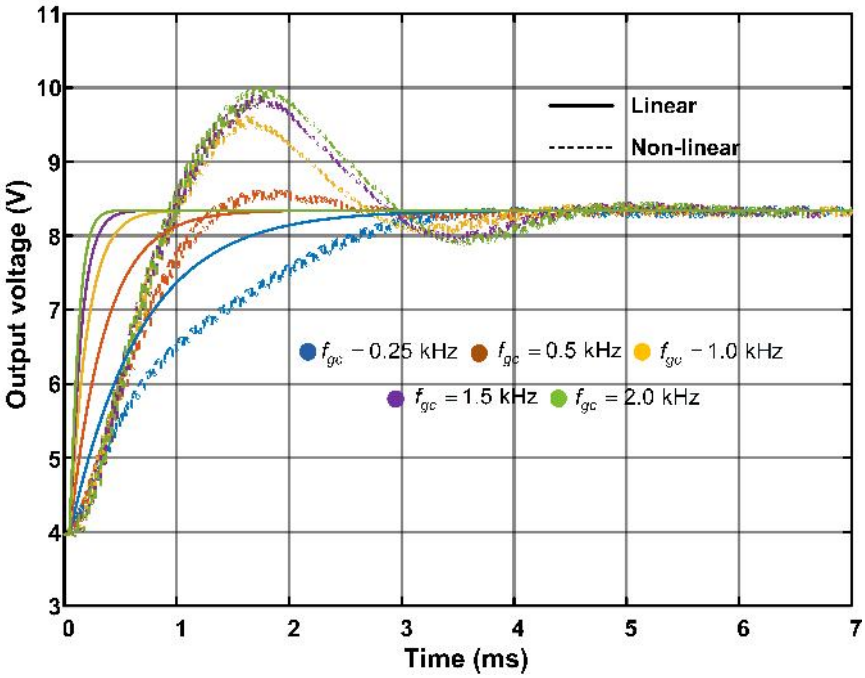


Figure 5.5: Simulation result: output voltage at different gain crossover frequencies.

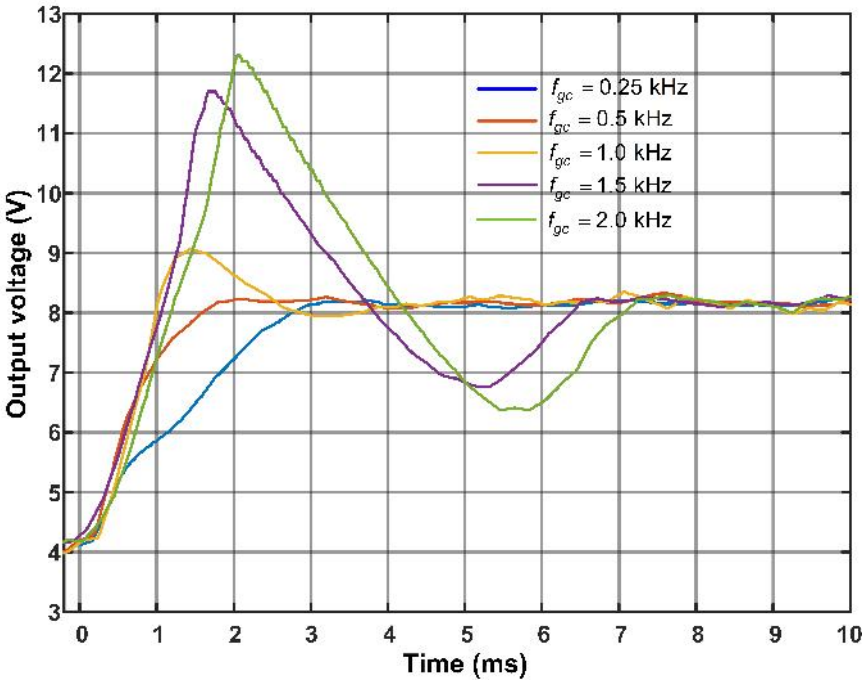


Figure 5.6: Experimental result: output voltage at different gain crossover frequencies.

Table 5.3: IMC-PID values for DC-DC boost converter

f_{gc}	0.25kHz	0.5kHz	1.0kHz	1.5kHz	2.0kHz
K_p	1.721e3	3.239e3	5.798e3	7.871e3	9.583e3
K_i	3.916e6	7.373e6	1.319e7	1.791e7	2.182e7
K_d	0.7249	1.3647	5.4426	3.3156	4.037

II. Non-linear: The results are obtained by a analogous model to practical set-up, which is developed in SIMULINK using Sim-PowerSystems Toolbox. The corresponding results are shown in Figure 5.5.

The validation of controller performance is observed from simulations and experiment results. The simulation results of overall system transient response is shown in Figure 5.5. An overshoot observed from the results, which are obtained by non-linear model. The reason is that the PID parameters are calculated from linearised model. Further, experimental results are shown in Figure 5.6, which is clearly having overshoot as in non-linear simulation results. The performance comparison also tabulated in Table 5.4. It is well-known that the as gain crossover frequency increases, the speed of response is improved. This can be clearly observed from the results.

Here, the key point or contribution is that there is no trial and error procedure used for tuning and if plant model is known and PID can be designed very easily.

5.2.8.2 IMC-PID for buck-boost converter

Here we present the performance of the designed IMC-PID when implemented on buck-boost converter through simulations.

Simulation and Experimental validation:

Consider the transfer function of non-ideal buck-boost converter given in (3.138) as,

$$G_{vd}(s) = \frac{29.29\left(\frac{s}{50000}+1\right)\left(-\frac{s}{54450}+1\right)}{\left(\frac{s}{3119.7}\right)^2+\frac{s}{4818.3}+1} \tag{5.49}$$

Table 5.4: Performance indices

ω_{gc}	t_r(ms)			t_s(ms)			M_p(%)		
	Sim		Exp	Sim		Exp	Sim		Exp
	L	NL		L	NL		L	NL	
0.25kHz	1.0	1.9	2.3	2.0	3.0	2.9	0	0	0
0.5kHz	0.5	0.9	1.1	1.0	2.7	1.9	0	0	0
1.0kHz	0.3	0.78	0.8	0.8	2.7	2.8	0	12	13
1.5kHz	0.2	0.78	0.8	0.5	3.1	6.2	0	25	35
2.0kHz	0.1	0.78	0.8	0.2	3.1	6.5	0	25	48

Sim-Simulation, Exp-Experimantal, L-Linear model, NL-Non-linear (Simulink) model

or in terms of SOPTD as,

$$G_{vd}(s) = \frac{29.29\left(\frac{s}{50000}+1\right)\left(e^{-\frac{s}{54450}}\right)}{\left(\frac{s}{3119.7}\right)^2+\frac{s}{4818.3}+1} \tag{5.50}$$

Here, converter switching frequency is $f = 20$kHz. Main contribution is to get PID parameters for various gain crossover frequencies. But, in this converter there is a RHP zero, which limits gain crossover frequency. The maximum achievable gain crossover frequency depends on the RHP zero position as discussed in previous sections. As per discussion, the buck-boost converter transfer function given in (5.49) falls under case I (*i.e.,*$\omega_{LHPz} < \omega_{RHPz}$). Hence, crossover frequency should be selected as given in Eq. (5.2) (*i.e.,* less than $\omega_{gco} = 1490kHz$). So, the PID parameters for buck-boost converter at any ω_{gc} can be calculated by substituting values from (5.49) in (5.44-5.46), we get controller parameters as given in Table 5.5.

Table 5.5: IMC-PID values for DC-DC buck-boost converter

f_{gc}	0.25kHz	0.5kHz	1.0kHz	1.5kHz	2.0kHz
K_p	569.2	1099	2058	2901	3679
K_i	2.585e6	4.994e6	9.349e6	1.318e7	1.657e7
K_d	0.3378	0.6528	1.22	1.722	2.17

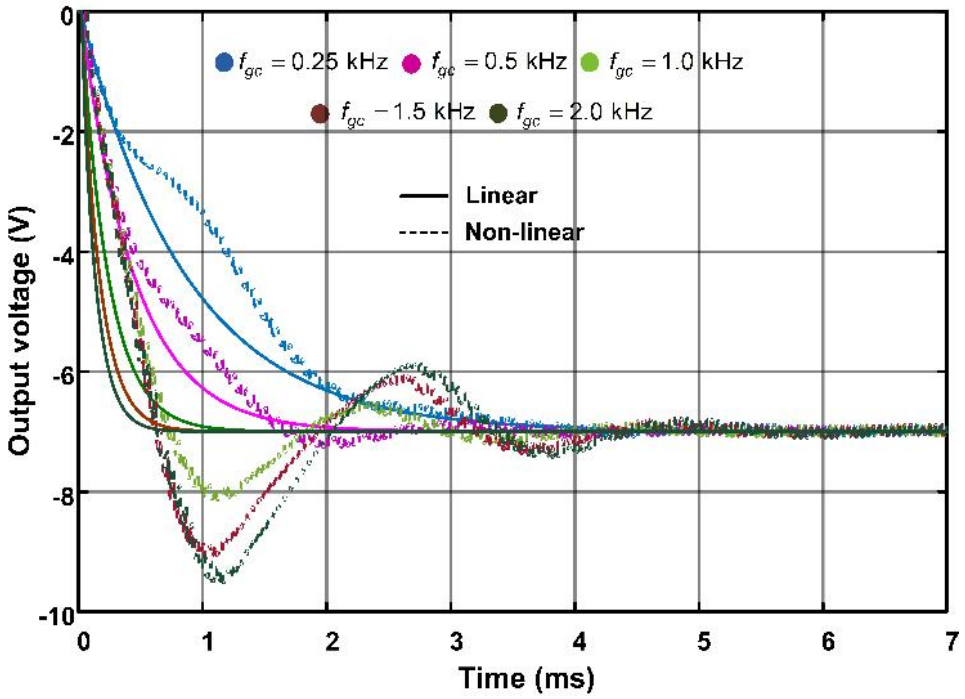


Figure 5.7: Simulation result: output voltage at different gain crossover frequencies.

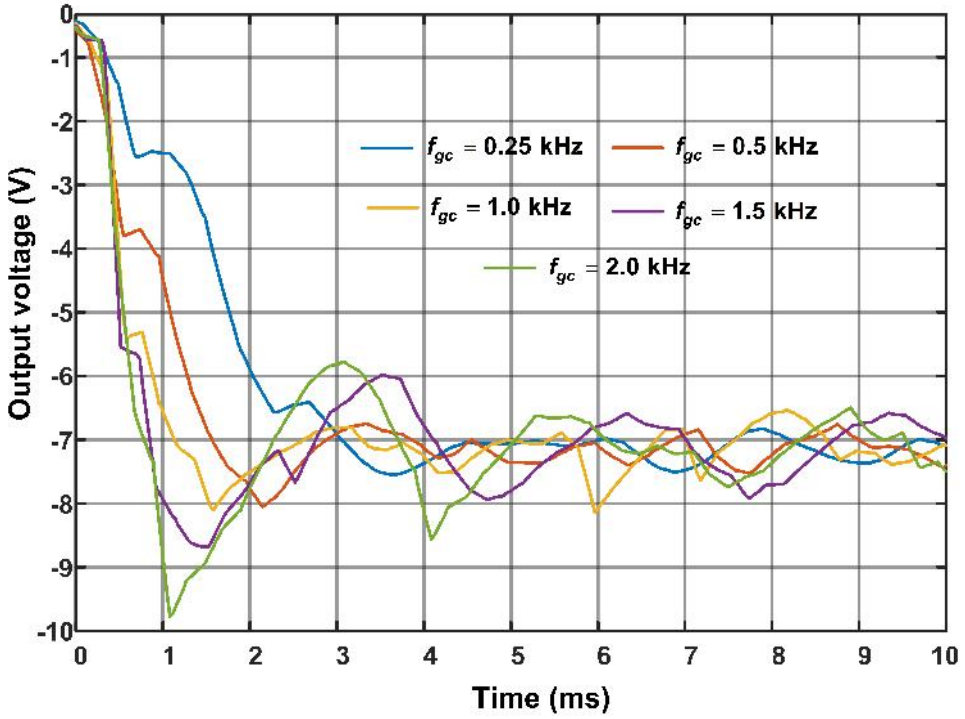


Figure 5.8: Experimental result: output voltage at different gain crossover frequencies.

Table 5.6: Performance indices

ω_{gc}	t_r(ms)			t_s(ms)			M_p(%)		
	Sim		Exp	Sim		Exp	Sim		Exp
	L	NL		L	NL		L	NL	
0.25kHz	2.0	2.0	2.2	3.0	3.0	4	0	0	10
0.5kHz	1.0	1.4	1.3	1.7	2.0	3	0	0	15
1.0kHz	0.5	0.6	0.9	0.7	3.2	3	0	15	15
1.5kHz	0.3	0.6	0.85	0.6	3.2	6	0	27	23
2.0kHz	0.2	0.6	0.85	0.5	3.2	6.5	0	34	42

Sim-Simulation, Exp-Experimantal, L-Linear model, NL-Non-linear (Simulink) model

The simulation studies are carried out as following two ways:

I.Linear: The results are obtained by using a linear transfer function model given by (5.49). The corresponding results are shown in Figure 5.7.

II. Non-linear: The results are obtained by a analogous model to practical set-up, which is developed in SIMULINK using Sim-Power Systems Toolbox. The corresponding results are shown in Figure 5.7.

The validation of controller performance is observed from simulations and experiment results. The simulation results of overall system transient response is shown in Figure 5.7. An overshoot observed from the results, which are obtained by non-linear model. The reason is that the PID parameters are calculated from linearised model. Further, experimental results are shown in Figure 5.8, which is clearly having overshoot as in non-linear simulation results. The performance comparison also tabulated in Table 5.6. It is well-known that the as gain crossover frequency increases, the speed of response is improved. This can be clearly observed from the results.

Here, the key point or contribution is that there is no trial and error procedure used for tuning and if plant model is known and PID can be designed very easily.

5.3 Robust PID Design for DC-DC Converters

Every system is not fully perfect and always shows some perturbed or uncertain characteristics. These can be observed from modeling and analysis, which we have presented in previous chapters. Uncertainties can be classified [202, 203] as,

1. Non-parametric (or) unstructured uncertainty: This type uncertainties may be occurred by imperfect dynamics, truncated high frequency modes, non-linearities, effects of linearisation, time-variation, etc.

2. Parametric (or) structured: This type uncertainties may be occurred by physical parameters that vary within given bounds, interval uncertainty (I1), ellipsoidal uncertainty (I2) and I1 uncertainty.

To compensate these uncertainties, a robust controller is required for regulatory and servomechanism of control system.

In DC-DC converters, the uncertainties caused by temperature change, ageing effect etc. So, the current section presents the design of robust controller for DC-DC converter system having parametric uncertainty (so called interval systems).

5.3.1 Interval analysis [153, 154]

An interval number $[x^-, x^+]$ can be defined by the set of $n \in \Re$ such that $x^- < n < x^+$. The arithmetic operations on intervals are defined as follows:

$$[x^-, x^+] + [y^-, y^+] = [x^- + y^-, x^+ + y^+] \tag{5.51}$$

$$\begin{aligned}[x^-, x^+] \times [y^-, y^+] = [\min(x^- y^-, x^- y^+, x^+ y^-, x^+ y^+ \\ , \max(x^- y^-, x^- y^+, x^+ y^-, x^+ y^+)]\end{aligned} \tag{5.52}$$

$$[x^-, x^+] + [y^-, y^+] = [x^- + y^-, x^+ + y^+] \tag{5.53}$$

$$[x^-, x^+] \div [y^-, y^+] = [x^-, x^+] \times [\tfrac{1}{y^+}, \tfrac{1}{y^-}], 0 \notin [y^-, y^+] \tag{5.54}$$

5.3.2 Kharitonov's theorem

Let the interval polynomials are

$$K_i(s) = \sum_{i=0}^{n} \delta_i s^i, \delta_i \in [x_i, y_i], \tag{5.55}$$

where, δ_i can take any value in closed interval $[x_i, y_i]$ are strictly Hurwitz, if and only if the four polynomials (5.56)-(5.59), are strictly Hurwitz:

$$K_1(s) = x_o + x_1 s + y_2 s^2 + y_3 s^3 + ... \tag{5.56}$$

$$K_2(s) = x_o + y_1 s + y_2 s^2 + x_3 s^3 + ... \tag{5.57}$$

$$K_3(s) = y_o + x_1 s + x_2 s^2 + y_3 s^3 + ... \tag{5.58}$$

$$K_4(s) = y_o + y_1 s + x_2 s^2 + x_3 s^3 + ... \tag{5.59}$$

5.3.2.1 Stability margin of an interval plant using Kharitonov's theorem

Consider an uncertain plant transfer function as

$$G(s) = \frac{\sum_{i=0}^{k_1} n_i s^i}{\sum_{i=0}^{k_2} d_i s^i} \tag{5.60}$$

where $k_1 \leq k_2, n_i \in [n_i^-, n_i^+], d_i \in [d_i^-, d_i^+]$.
Therefore, there are four Kharitonov polynomials for the numerator and four Kharitonov polynomials for the denominator. They are shown in (5.61) and (5.62).

$$\begin{aligned} N_1(s) &= n_0^- + n_1^- s + n_2^+ s^2 + ... \\ N_2(s) &= n_0^- + n_1^+ s + n_2^+ s^2 + ... \\ N_3(s) &= n_0^+ + n_1^- s + n_2^- s^2 + ... \\ N_4(s) &= n_0^+ + n_1^+ s + n_2^- s^2 + ... \end{aligned} \tag{5.61}$$

Similarly, the four denominator polynomials are obtained as

$$\begin{aligned} D_1(s) &= d_0^- + d_1^- s + d_2^+ s^2 + ... \\ D_2(s) &= d_0^- + d_1^+ s + d_2^+ s^2 + ... \\ D_3(s) &= d_0^+ + d_1^- s + d_2^- s^2 + ... \\ D_4(s) &= d_0^+ + d_1^+ s + d_2^- s^2 + ... \end{aligned} \tag{5.62}$$

From (5.61) and (5.62), it is clear that we can get 16 Kharitonov transfer functions as given in (5.63).

$$G(s) = G_{ij}(s) = \frac{N_i(s)}{D_j(s)} \tag{5.63}$$

where, $N_i(s)$ and $D_i(s)$ for $i, j = 1, 2, 3, 4$. We determine gain margin and phase margin for all the 16 Kharitonov plants. From them, the worst-case gain margin and phase margin will be determined, which will be the actual stability margin of an interval plant.

5.3.3 Stability boundary locus

The stability boundary locus method was proposed by N. Tan et.al. in 2006 [81] for the computation of PI controller parameters Kp and Ki. This method gives a family of all stabilizing PI controllers. In this method, a global stability region is obtained in Kp-Ki plane by the intersection of the real root boundary (RRB) and the complex root boundary (CRB) [204, 205]. The real root boundary (RRB) is the boundary line at which a real root of the closed-loop characteristic equation crosses the imaginary axis at $s = 0$. The complex root boundary is the boundary line at which complex roots of the closed-loop characteristic equation crosses over the imaginary axis at $s = j\omega$. The RRB and CRB divide the entire parameter plane (Kp-Ki plane) into stable and unstable regions. The stable boundary region can be found by choosing a test point within each region. Any pair of Kp-Ki value within this stable region would stabilize the closed-loop system. Further, this method was also extended to compute the PI parameters based on desired gain margin and phase margin. The stability region obtained based on the desired phase margin and gain margin is a subset of the global stability region.

5.3.4 PID controller design for interval plant

Consider the interval plant as given in (5.63) and put $s = jw$, we get,

$$G(j\omega) = \frac{N_e(-\omega^2) + j\omega N_o(-\omega^2)}{D_e(-\omega^2) + j\omega D_o(-\omega^2)}. \tag{5.64}$$

Inserting gain-phase compensator $Ae^{-j\phi}$ in the forward path along with controller $C(s)$ and $G(s)$ as shown in Figure 5.9. By determining the closed-loop transfer func-

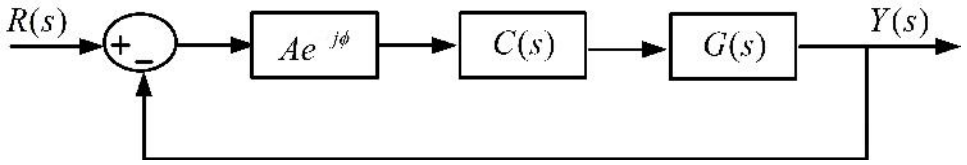


Figure 5.9: Feedback control system with a controller and a gain phase margin tester.

tion and equating real and imaginary parts to zero, we get,

$$k_p = \frac{X(\omega)U(\omega) - Y(\omega)R(\omega)}{Q(\omega)U(\omega) - R(\omega)S(\omega)} \tag{5.65}$$

and

$$k_i = \frac{Y(\omega)Q(\omega) - X(\omega)S(\omega)}{Q(\omega)U(\omega) - R(\omega)S(\omega)} \tag{5.66}$$

where,

$$\begin{aligned}
Q(\omega) &= A(\omega N_e(-\omega^2)\sin(\phi) - \omega^2 N_0(-\omega^2)\cos(\phi)) \\
R(\omega) &= A(N_e(-\omega^2)\cos(\phi) + \omega N_0(-\omega^2)\sin(\phi)) \\
S(\omega) &= A(\omega N_e(-\omega^2)\cos(\phi) + \omega^2 N_0(-\omega^2)\sin(\phi) \\
U(\omega) &= A(\omega N_0(-\omega^2)\cos(\phi) - N_e(-\omega^2)\sin(\phi)) \\
X(\omega) &= \omega^2 D_0(-\omega^2) + Ak_d\omega^2 \begin{pmatrix} N_e(-\omega^2)\cos(\phi) \\ -\omega N_0(-\omega^2)\sin(\phi) \end{pmatrix} \\
Y(\omega) &= -\omega D_e(-\omega^2) + Ak_d\omega^2 \begin{pmatrix} -N_e(-\omega^2)\sin(\phi) \\ +\omega N_0(-\omega^2)\cos(\phi) \end{pmatrix}
\end{aligned} \tag{5.67}$$

To obtain the stability boundary locus (k_p, k_i) plane, for a given value of gain margin A, one needs to set $\phi = 0$ and assume $k_d = k, (k \in \Re^+)$ in (5.65) and (5.66). On

the other hand, setting $A = 1$ and $k_d = k$, in (5.65) and (5.66), one can obtain the stability boundary locus for a given phase margin ϕ. An interval plant $G(s)$ has 16 plants *i.e.*, $G_1(s), G_2(s), ..., G_{16}(s)$.

For $G_1(s)$, when both gain, phase margin and k_d are fixed, the stability region is

$$S\left(G_1(s)\right) = S(G_{1g})_{\phi=0,k_d=k} \cap S(G_{1p})_{A=1,k_d=k} \tag{5.68}$$

where, $S(G_{1g})_{\phi=0,k_d=k}$ shows the stability region for Kharitonov polynomial $G_1(s)$, when we replace A as the actual gain margin required and $\phi = 0, k_d = k$. Similarly, $S(G_{1p})_{A=1,k_d=k}$ shows the stability region for Kharitonov polynomial $G_1(s)$, when we replace ϕ as the actual phase margin required and $A = 1, k_d = k$. $\cap$ indicates the intersection of stability region of $S(G_{1g})_{\phi=0,k_d=k}$ and $S(G_{1p})_{A=1,k_d=k}$.
For $G_2(s)$, we get,

$$S\left(G_2(s)\right) = S(G_{2g})_{\phi=0,k_d=k} \cap S(G_{2p})_{A=1,k_d=k} \tag{5.69}$$

Similarly, for $G_{16}(s)$, we get,

$$S\left(G_{16}(s)\right) = S(G_{16g})_{\phi=0,k_d=k} \cap S(G_{16p})_{A=1,k_d=k} \tag{5.70}$$

Thus, the actual stability region is

$$S\left(G(s)\right) = S\left(G_1(s)\right) \cap S\left(G_2(s)\right) ... \cap S\left(G_{16}(s)\right) \tag{5.71}$$

For various k_d, a family of stability boundaries will be obtained. Select the k_d, such that stability region for the considered plant would be larger.

Remark: If the numerator is constant, then there is a need to determine stability region for only four transfer functions instead of sixteen.

5.3.5 Proposed approach for DC-DC converters

A technique is presented to design PID controller using four transfer functions instead of sixteen transfer functions. This work is continuation of the theory presented in [152]. Let consider a generalized plant transfer function as given in (5.63) and assume it as proper transfer function ($k_1 = k_2$).

The closed-loop characteristic equation of the system is given as

$$\begin{aligned} C(s) &= 1 + G(s) \\ &= (n_0 + d_0) + (n_1 + d_1)\, s + ... + (n_{k_2} + d_{k_2})\, s^{k_2} \end{aligned} \tag{5.72}$$

Applying Kharitonov theorem to interval polynomial (5.72), we get following polynomials:

$$\begin{aligned} \mathrm{p}_1(s) &= \left[n_0^- + d_0^-\right] + \left[n_1^- + d_1^-\right] s + \left[n_2^+ + d_2^+\right] s^2 + ... \\ \mathrm{p}_2(s) &= \left[n_0^- + d_0^-\right] + \left[n_1^+ + d_1^+\right] s + \left[n_2^+ + d_2^+\right] s^2 + ... \\ \mathrm{p}_3(s) &= \left[n_0^+ + d_0^+\right] + \left[n_1^- + d_1^-\right] s + \left[n_2^- + d_2^-\right] s^2 + ... \\ \mathrm{p}_4(s) &= \left[n_0^+ + d_0^+\right] + \left[n_1^+ + d_1^+\right] s + \left[n_2^- + d_2^-\right] s^2 + ... \end{aligned} \tag{5.73}$$

The polynomials (5.73) are in form of $1 + GH(s)$. So, these polynomials can be written in terms of four open loop transfer functions such as

$$\begin{aligned} G'_{K_1}(s) &= \frac{n_0^- + d_0^-}{[n_{k2}^- + d_{k2}^-]s^{k2} + [n_{k2-1}^- + d_{k2-1}^-]s^{k2-1} + [n_{k2-2}^+ + d_{k2-2}^+]s^{k2-2}..}; \\ G'_{K_2}(s) &= \frac{n_0^- + d_0^-}{[n_{k2}^- + d_{k2}^-]s^{k2} + [n_{k2-1}^+ + d_{k2-1}^+]s^{k2-1} + [n_{k2-2}^+ + d_{k2-2}^+]s^{k2-2}..}; \\ G'_{K_3}(s) &= \frac{n_0^+ + d_0^+}{[n_{k2}^+ + d_{k2}^+]s^{k2} + [n_{k2-1}^- + d_{k2-1}^-]s^{k2-1} + [n_{k2-2}^- + d_{k2-2}^-]s^{k2-2}..}; \\ G'_{K_4}(s) &= \frac{n_0^+ + d_0^+}{[n_{k2}^+ + d_{k2}^+]s^{k2} + [n_{k2-1}^+ + d_{k2-1}^+]s^{k2-1} + [n_{k2-2}^- + d_{k2-2}^-]s^{k2-2}..}; . \end{aligned} \tag{5.74}$$

Therefore, there is need to determine stability boundary locus for only four transfer functions. Now, by putting $s = j\omega$ in all these four transfer functions, obtain expressions for k_p, k_i from (5.65) and (5.66), respectively for fixed value of k_d. From stability boundary locus, one can obtain the stability margin as

$$S\left(G'_{K_1}(s)\right) = S\left(G'_{K_{1g}}\right)_{\phi=0, k_d=k} \cap S\left(G'_{K_{1p}}\right)_{A=1, k_d=k} \tag{5.75}$$

Similarly, we get the stability regions for all four transfer functions. Finally, the intersection of all four stability regions gives the actual stability region, which is given as

$$S\left(G(s)\right) = \begin{bmatrix} S\left(G'_{K_1}(s)\right) \cap S\left(G'_{K_2}(s)\right) \\ \cap S\left(G'_{K_3}(s)\right) \cap S\left(G'_{K_4}(s)\right) \end{bmatrix} \tag{5.76}$$

So, here only four transfer functions are sufficient from the family of interval plant transfer functions.

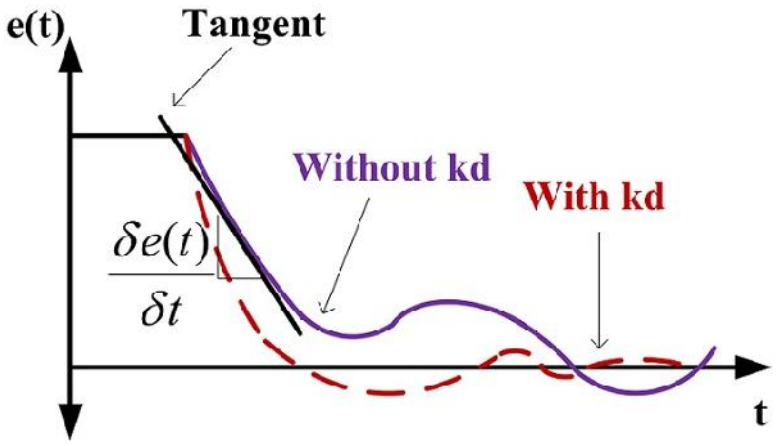


Figure 5.10: Effect of derivative gain k_d.

5.3.6 Selection of derivative gain k_d

Derivative action is generally used for plants having double integrals or second order dynamics [122]. Derivative action profitably used to speed up the transient response. However, drawback with derivative action is that it amplifies or provides high gain for signals with high-frequency. This phenomenon introduces high-frequency noise for large variations of the control signal. So, it is very important to choose proper derivative gain. The PID controller can be expressed as

$$u(t) = k_p e(t) + k_i \int_0^t e(\tau)d\tau + k_d \frac{de(t)}{dt} \tag{5.77}$$

where $u(t)$ =control signal and $e(t)$=error.

From Figure 5.77, it is clear that the derivative term is proportional to the time derivative of the error. Based on this, the following procedure has been given to select the derivative gain constant k_d:

Step 1: Initially, put $k_d = 0$ in (5.65) & (5.66) and we obtain the stability boundary locus in (k_p, k_i) plane.

Step 2: Then, select some point in the plane and find the error function $e(t)$.

Step 3: Derivative is nothing but the rate of change of a function, such as the error function curve shown in Figure 5.10. Measure the slope *i.e.,* $\frac{\delta e(t)}{\delta t}$.

Step 4: Now, select the gain (k_d) such away that changes in error should be eliminated.

5.3.7 Robust PID design for buck converter

The (5.78) shows the analytical expression of the power stage transfer function between output voltage $\tilde{v}_o$ and the duty ratio $\tilde{d}$ in continuous conduction mode (CCM), which is given as,

$$G_{vd}(s) = \frac{\hat{v}_o}{\hat{d}}(s) = \frac{\left(\frac{Rr_c\left(V_g(R+r_L+r_d)+V_{fd}(R+r_L+r_g+r_{on})\right)}{L(R+r_c)(R+r_L+D(r_g+r_{on})+(1-D)r_d)}\right)s + \left(\frac{R\left(V_g(R+r_L+r_d)+V_{fd}(R+r_L+r_g+r_{on})\right)}{LC(R+r_c)(R+r_L+D(r_g+r_{on})+(1-D)r_d)}\right)}{s^2 + \left(\frac{L+C((R+r_c)(r_L+D(r_g+r_{on})+(1-D)r_d)+Rr_c)}{LC(R+r_c)}\right)s + \left(\frac{R+r_L+D(r_g+r_{on})+(1-D)r_d}{LC(R+r_c)}\right)} \tag{5.78}$$

In (5.78), the term in curly brackets of the denominator are of the form $s^2+2\xi w_n s+w_n^2$. Therefore, the transfer function $G_{vd}(s)$ can be written in terms of numerator and denominator as follows:

$$G_{vd}(s) = \frac{\tilde{v}_o}{\tilde{d}} = \frac{w_n^2}{w_z}\frac{s+w_z}{(s^2+2\xi w_n s+w_n^2)} \tag{5.79}$$

This can be further written as

$$= \frac{n_1 s + n_o}{d_2 s^2 + d_1 s + d_o} = \frac{N(s)}{D(s)} \tag{5.80}$$

where,

$$\begin{aligned} d_2 &= 1; \\ d_1 &= \tfrac{L+C((R+r_c)(r_L+D(r_g+r_{on})+(1-D)r_d)+Rr_c)}{LC(R+r_c)}; \\ d_0 &= \tfrac{R+r_L+D(r_g+r_{on})+(1-D)r_d}{LC(R+r_c)}. \end{aligned} \tag{5.81}$$

and

$$\begin{aligned} n_1 &= \tfrac{Rr_c\left(V_g(R+r_L+r_d)+V_{fd}(R+r_L+r_g+r_{on})\right)}{L(R+r_c)(R+r_L+D(r_g+r_{on})+(1-D)r_d)}; \\ n_0 &= \tfrac{R\left(V_g(R+r_L+r_d)+V_{fd}(R+r_L+r_g+r_{on})\right)}{LC(R+r_c)(R+r_L+D(r_g+r_{on})+(1-D)r_d)}. \end{aligned} \tag{5.82}$$

By considering the uncertainties in the system parameters, the (5.80) can be represented in terms of interval polynomial as

$$= \frac{[n_1^-, n_1^+]s + [n_o^-, n_o^+]}{[d_2^-, d_2^+]s^2 + [d_1^-, d_1^+]s + [d_o^-, d_o^+]}, \tag{5.83}$$

Using over-bounding technique, the coefficients of uncertain parameters are expressed as

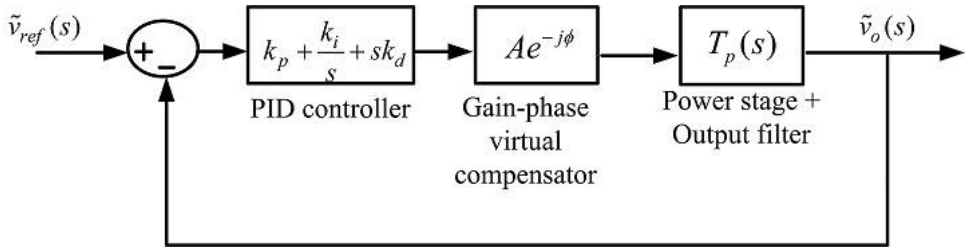


Figure 5.11: Block diagram of closed-loop buck converter with PID controller and gain-phase virtual compensator.

$$\begin{aligned} n_0^- &= \frac{R^-\left(V_g^-\left(R^-+r_L^-+r_d^-\right)+V_{fd}^-\left(R^-+r_L^-+r_g^-+r_{on}^-\right)\right)}{L^+C^+\left(R^++r_c^+\right)\left(R^++r_L^++D\left(r_g^++r_{on}^+\right)+(1-D)r_d^+\right)}, \\ n_0^+ &= \frac{R^+\left(V_g^+\left(R^++r_L^++r_d^+\right)+V_{fd}^+\left(R^++r_L^++r_g^++r_{on}^+\right)\right)}{L^-C^-\left(R^-+r_c^-\right)\left(R^-+r_L^-+D\left(r_g^-+r_{on}^-\right)+(1-D)r_d^-\right)}, \end{aligned} \tag{5.84}$$

$$\begin{aligned} n_1^- &= \frac{R^-r_c^-\left(V_g^-\left(R^-+r_L^-+r_d^-\right)+V_{fd}^-\left(R^-+r_L^-+r_g^-+r_{on}^-\right)\right)}{L^+\left(R^++r_c^+\right)\left(R^++r_L^++D\left(r_g^++r_{on}^+\right)+(1-D)r_d^+\right)}, \\ n_1^+ &= \frac{R^+r_c^+\left(V_g^+\left(R^++r_L^++r_d^+\right)+V_{fd}^+\left(R^++r_L^++r_g^++r_{on}^+\right)\right)}{L^-\left(R^-+r_c^-\right)\left(R^-+r_L^-+D\left(r_g^-+r_{on}^-\right)+(1-D)r_d^-\right)}, \end{aligned} \tag{5.85}$$

$$\begin{aligned} d_0^- &= \frac{R^-+r_L^-+D\left(r_g^-+r_{on}^-\right)+(1-D)r_d^-}{L^+C^+\left(R^++r_c^+\right)}, \\ d_0^+ &= \frac{R^++r_L^++D\left(r_g^++r_{on}^+\right)+(1-D)r_d^+}{L^-C^-\left(R^-+r_c^-\right)}, \end{aligned} \tag{5.86}$$

$$\begin{aligned} d_1^- &= \frac{L^-+C^-\left(\left(R^-+r_c^-\right)\left(r_L^-+D\left(r_g^-+r_{on}^-\right)+(1-D)r_d^-\right)+R^-r_c^-\right)}{L^+C^+\left(R^++r_c^+\right)}, \\ d_1^+ &= \frac{L^++C^+\left(\left(R^++r_c^+\right)\left(r_L^++D\left(r_g^++r_{on}^+\right)+(1-D)r_d^+\right)+R^+r_c^+\right)}{L^-C^-\left(R^-+r_c^-\right)}, \end{aligned} \tag{5.87}$$

$$d_2^- = d_2^+ = 1. \tag{5.88}$$

Now, we determine frequency response of buck converter using Kharitonov's theorem and Bode plots. From these analysis, the worst-case stability margin can be determined. We formulate all possible Kharitonov interval plants and from them the worst-case stability margin is determined. Now, we need to improve the stability margin by designing PID controller, which stabilizes all interval plants and improves the phase margin, since gain margin is infinite. Figure 5.11, shows the block diagram for unity feedback control system for buck converter. A PID controller and a virtual gain-phase compensator are in forward path with the buck converter. According to the proposed design approach, consider the system without PID controller as in

Table 5.7: Parameters for interval buck converter

Parameters	Value
Source voltage (V_g)	12V-15V
Output voltage (V_o)	8V
Input resistance(r_g)	0.1Ω-0.2Ω
Inductor (L)	250 μH-300 μH
Inductor ESR (r_L)	0.3Ω-2Ω
Capacitor (C)	50 μF-100 μF
Capacitor ESR (r_C)	0.1Ω-0.9Ω
Switch ON resistance (r_{on})	0.1Ω-0.2Ω
Diode ON resistance (r_d)	0.05Ω-0.1Ω
Diode forward drop voltage (V_{fd})	0.5V-0.8V
Switching frequency (f)	20KHz
Load resistance (R)	10 Ω-20 Ω

(5.80) and closed-loop formulation is given as

$$G_{cl}(s) = 1 + G_{vd}(s) = d_2 s^2 + (n_1 + d_1)s + n_o + d_o \tag{5.89}$$

Using Kharitonov's theorem, four Kharitonov polynomials are

$$k_1(s) = s^2 + \left[n_1^- + d_1^-\right] s + \left[n_o^- + d_o^-\right] \tag{5.90}$$

$$k_2(s) = s^2 + \left[n_1^- + d_1^-\right] s + \left[n_o^+ + d_o^+\right] \tag{5.91}$$

$$k_3(s) = s^2 + \left[n_1^+ + d_1^+\right] s + \left[n_o^- + d_o^-\right] \tag{5.92}$$

$$k_4(s) = s^2 + \left[n_1^+ + d_1^+\right] s + \left[n_o^+ + d_o^+\right] \tag{5.93}$$

Now we need a controller which stabilizes all four Kharitonov polynomials. First of all, consider Kharitonov polynomial $k_1(s)$ as an open loop transfer function

$$G'_{vdoc1}(s) = \frac{n_o^- + d_o^-}{s^2 + \left[n_1^- + d_1^-\right] s} \tag{5.94}$$

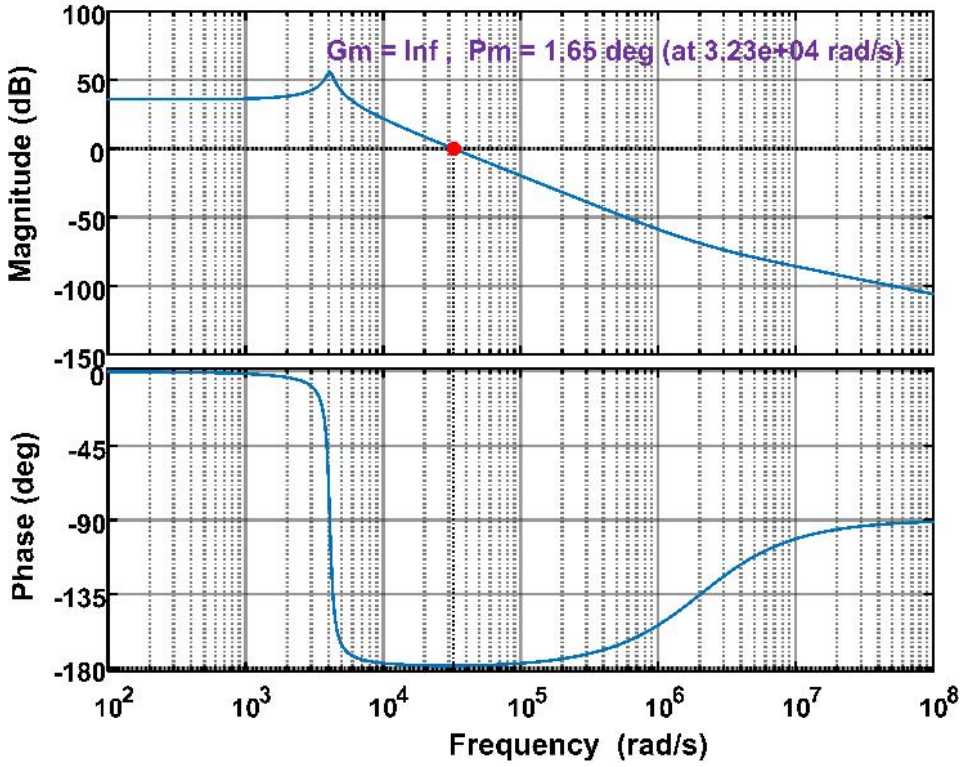


Figure 5.12: Worst case stability margin of the buck converter without controller.

Similarly from remaining three Kharitonov polynomials ($k_2(s)$, $k_3(s)$, $k_4(s)$) as given in (5.91)-(5.93), we can get three more open loop transfer functions $G'_{vdoc2}(s)$, $G'_{vdoc3}(s)$ and $G'_{vdoc3}(s)$, respectively.

Important note: Here, if interval analysis is neglected then step response of $G_{vd}(s)$ and $G'_{vdoc1}(s)$ should be approximately equal. This will be true in cases where transfer functions having placement of LHP zeros far from the origin. For DC-DC buck converter, it is shown in Figure 5.14.

Compare (5.94) with (5.64), we get,

$$N_e(-w^2) = n_o^- + d_o^-, N_o(-w^2) = 0, \tag{5.95}$$

$$D_e(-w^2) = -w^2, D_o(-w^2) = n_1^- + d_1^-. \tag{5.96}$$

Substitute (5.95) and (5.96) in (5.68)-(5.70), we get,

$$k_p = \frac{w\left(D_o(-w^2)\sin\phi + w\cos\phi + k_d N_e(-w^2)\sin\phi\cos\phi(1-w)\right)}{N_e(-w^2)} \tag{5.97}$$

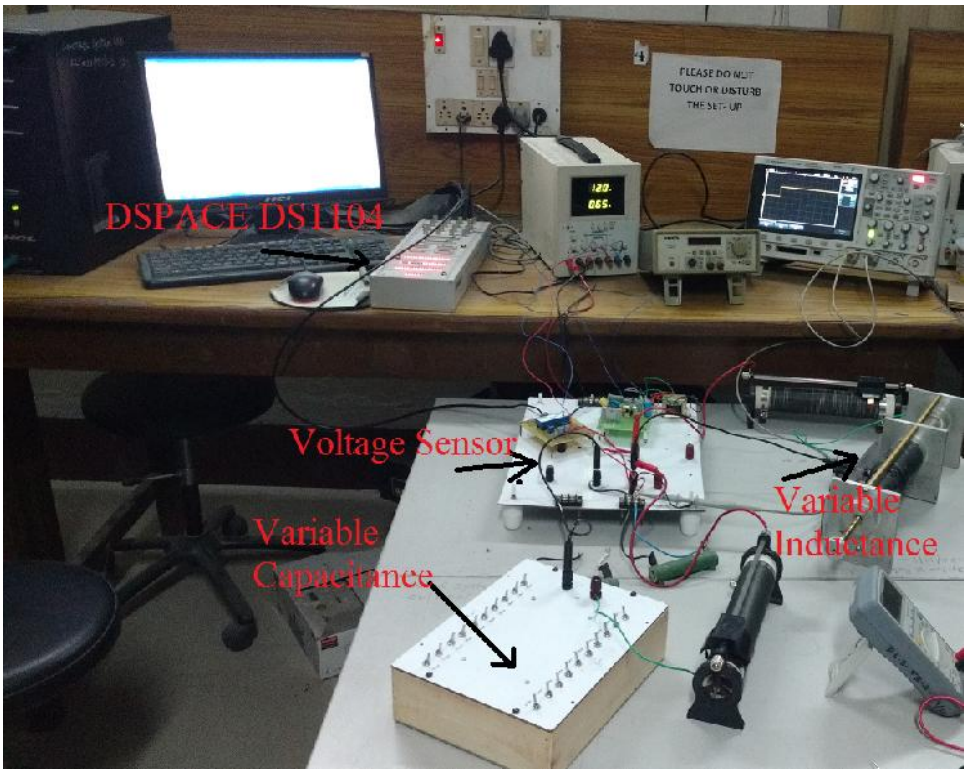


Figure 5.13: Experimental set-up for uncertain DC-DC buck converter.

$$k_i = \frac{w^2\left(D_o(-w^2)\cos\phi - w\sin\phi + k_d N_e(-w^2)\right)}{N_e(-w^2)} \tag{5.98}$$

The PID controller region can be obtained for the required phase margin ϕ. Hence, using (5.97) and (5.98), we can calculate the stability region for ${G_{vdoc1}}'(s)$, in (k_p, k_i) plane for fixed k_d. Similarly, we can obtain the stability region for the remaining three open loop transfer functions derived from Kharitonov polynomials. The intersection of all four regions gives the possible control parameters values. Select anyone value from intersection, then the open loop transfer functions ${G_{vdoc1}}'(s)$ of (5.94) of the buck converter with PID controller becomes

$${G_{vdc1}}'(s) = \frac{n_o^- + d_o^-}{s^2 + \left[n_1^- + d_1^-\right]s}(k_p + \frac{k_i}{s} + sk_d) \tag{5.99}$$

Similarly, we get ${G_{vdc2}}'(s)$, ${G_{vdc3}}'(s)$ and ${G_{vdc4}}'(s)$, where, ${G_{vdc1}}'(s)$, ${G_{vdc2}}'(s)$, ${G_{vdc3}}'(s)$, ${G_{vdc4}}'(s)$ are the Kharitonov compensated open loop transfer functions.

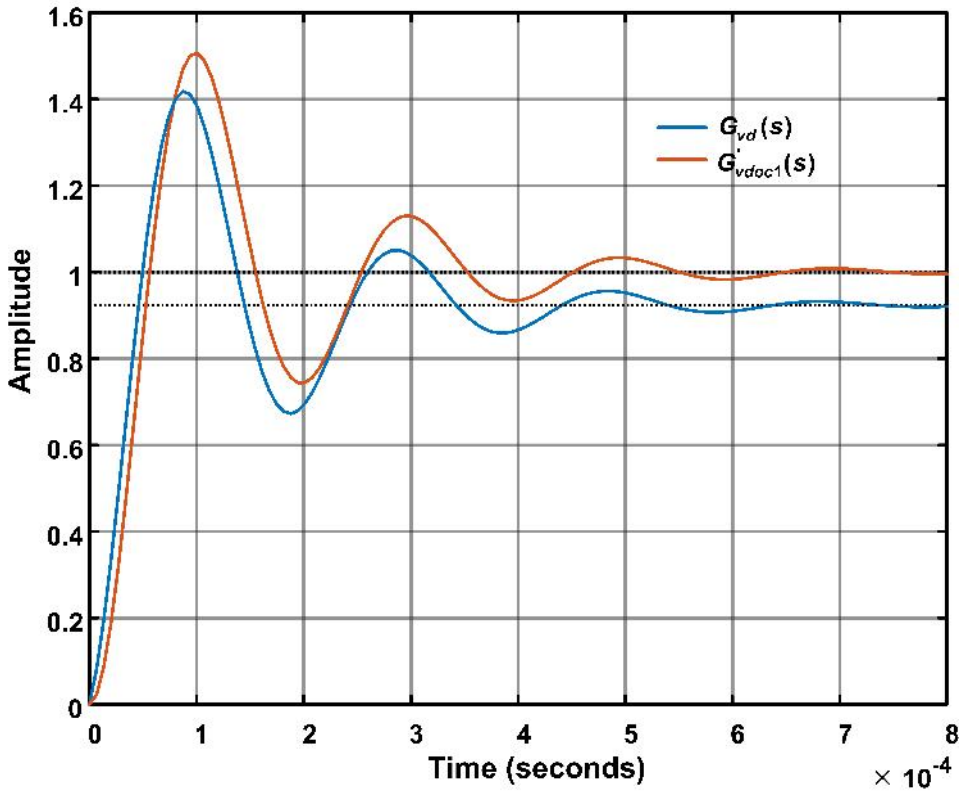


Figure 5.14: Step responses of $G_{vd}(s)$ and $G^{'}_{vdoc1}(s)$.

5.4 Simulation and Experimental Results

The proposed robust control scheme is implemented on the buck converter and validated through simulations and hardware implementations. The hardware prototype set up for uncertain buck converter is shown in Figure 5.13. DSPACE DS1104 digital controller board is used to implement the proposed robust PID controller. The parameters considered for the simulations and hardware prototype are given in Table 5.7.

According to the proposed scheme, we formulated all possible Kharitonov interval plants *i.e.*, 16 and found the worst case stability margin. The worst case stability margin is 25° and gain margin is infinite, which is shown in Figure 5.12 and Table 5.9. Now as explained in previous section, the PID controller is designed for phase margin 40°. First, we obtained stability region in (k_p, k_i) plane for fixed $k_d = 0$ as shown in Figure 5.15. Then, take any combination of (k_p, k_i). Here, we have considered a

Table 5.8: Practical implementation of Kharitonov polynomials.

Kharitonov Polynomials	Parameters chosen for experimentation
First $K_1(s)$	$v_{i\min}, L_{\max}, C_{\max}, R_{\max \rightleftarrows \min}, r_{C\max \rightleftarrows \min}, r_{L\max \rightleftarrows \min},$ $r_{g\max \rightleftarrows \min}, r_{on\max \rightleftarrows \min}, r_{d\max \rightleftarrows \min}, v_{fd\min}$
Second $K_2(s)$	$v_{i\min \rightleftarrows \max}, L_{\max \rightleftarrows \min}, C_{\max \rightleftarrows \min}, R_{\max \rightleftarrows \min}, r_{C\max \rightleftarrows \min}, r_{L\max \rightleftarrows \min},$ $r_{g\max \rightleftarrows \min}, r_{on\max \rightleftarrows \min}, r_{d\max \rightleftarrows \min}, v_{fd\min \rightleftarrows \max}$
Third $K_3(s)$	$v_{i\min \rightleftarrows \max}, L_{\max \rightleftarrows \min}, C_{\max \rightleftarrows \min}, R_{\max \rightleftarrows \min}, r_{C\max \rightleftarrows \min}, r_{L\max \rightleftarrows \min},$ $r_{g\max \rightleftarrows \min}, r_{on\max \rightleftarrows \min}, r_{d\max \rightleftarrows \min}, v_{fd\min \rightleftarrows \max}$
Fourth $K_4(s)$	$v_{i\max}, L_{\max \rightleftarrows \min}, C_{\max \rightleftarrows \min}, R_{\max \rightleftarrows \min}, r_{C\max \rightleftarrows \min}, r_{L\max \rightleftarrows \min},$ $r_{g\max \rightleftarrows \min}, r_{on\max \rightleftarrows \min}, r_{d\max \rightleftarrows \min}, v_{fd\max}$

point $A(0, 50)$ as an example. Then, executed the closed-loop operation and error function obtained as shown in Figure 5.16. As explained in procedure, the slope of the curve $\frac{de(t)}{dt}$ is calculated (In this we obtained $\frac{de}{dt} = 2500$). Now, K_d is selected such that the error is minimised. So, here we chosen $K_d = 0.0001$.

Then, using (5.97)-(5.98), we calculated stability region in (k_p, k_i) plane for fixed $k_d = 0.0001$ for all four Kharitonov polynomials obtained from (5.90) to (5.93). The stability region is shown in Figure 5.17(a)-(d). From (5.76), actual stability region is obtained in MATLAB environment which is nothing but the intersection of all four regions as shown in Figure 5.17(e). For different values of k_d, various intersection regions are obtained as shown in Figure 5.18. From this, it is observed that, as K_d value increases, the intersection of all four regions is increased. By selecting any point in intersection region, we get the infinite gain margin and the phase margin greater than 40°, which is tabulated in Table 5.9. Here, we have selected value of $k_p = 2.5$, $k_i = 500$ and $k_d = 0.0001$. From Figure 5.16, it can be observed that the error became zero faster than with PI controller. Further, with nominal values the step responses of buck converter with PI and PID controllers is compared as shown in Figure 5.19. Moreover, to present the effectiveness of proposed robust PID controller performance, the closed-loop performance of all sixteen Kharitonov transfer functions is shown in Figure 5.20. This shows, only four transfer functions

Table 5.9: Stability margin of converter

Transfer function	Stability margin (without controller)	Stability margin (with controller)
$G_1(s)$	$42.7°$	inf
$G_2(s)$	$70.3°$	inf
$G_3(s)$	$44.3°$	inf
$G_4(s)$	$67.4°$	inf
$G_5(s)$ [a]	$25°$	inf
$G_6(s)$	$41.8°$	inf
$G_7(s)$	$25.4°$	inf
$G_8(s)$	$41.1°$	inf
$G_9(s)$	$85.7°$	inf
$G_10(s)$	$96.7°$	inf
$G_11(s)$	$85.8°$	inf
$G_12(s)$	$96.6°$	inf
$G_13(s)$	$72.3°$	inf
$G_14(s)$	$82.5°$	inf
$G_15(s)$	$72.5°$	inf
$G_16(s)$	$82.2°$	inf

[a] Shows the worst case stability margin.

are needed to design controller. The simulation results are validated through hardware results. In order to verify the proposed algorithm through experiments, uncertainty in each element is required. Therefore, variable inductance of ferrite core material, variable capacitance of electrolytic material and rheostats for equivalent series resistances of inductor and capacitor are used. In order to get the variation in inductor and capacitor ESR, a rheostat is connected in series respectively. The output voltage of the converter is sensed by a voltage sensor (AD202JN), which is given to ADC channel of DSPACE DS1104. This sensed voltage from ADC is

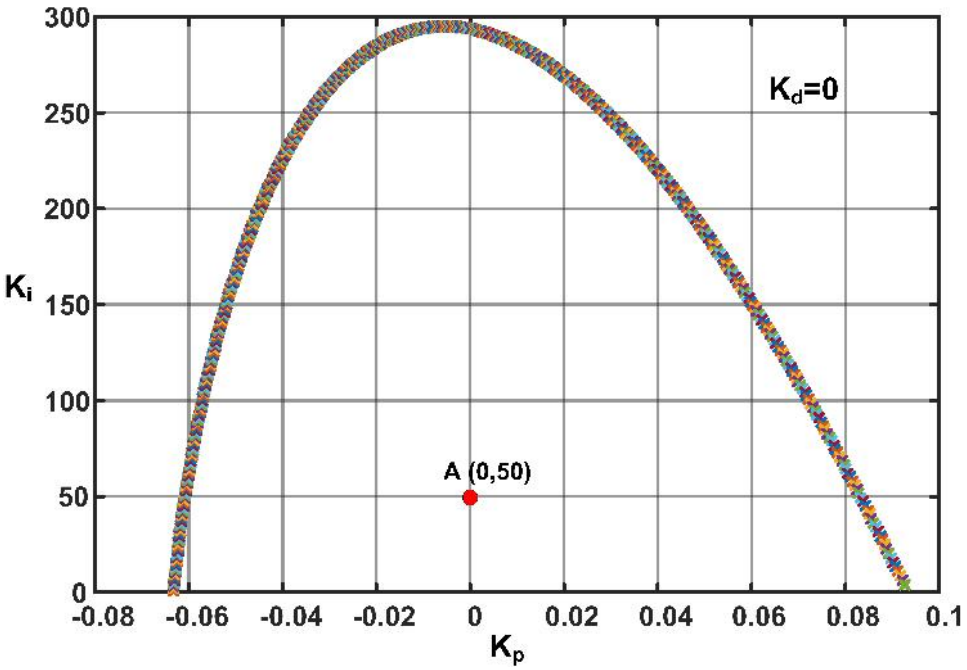


Figure 5.15: Stability region for nominal DC-DC buck converter for K_d=0.

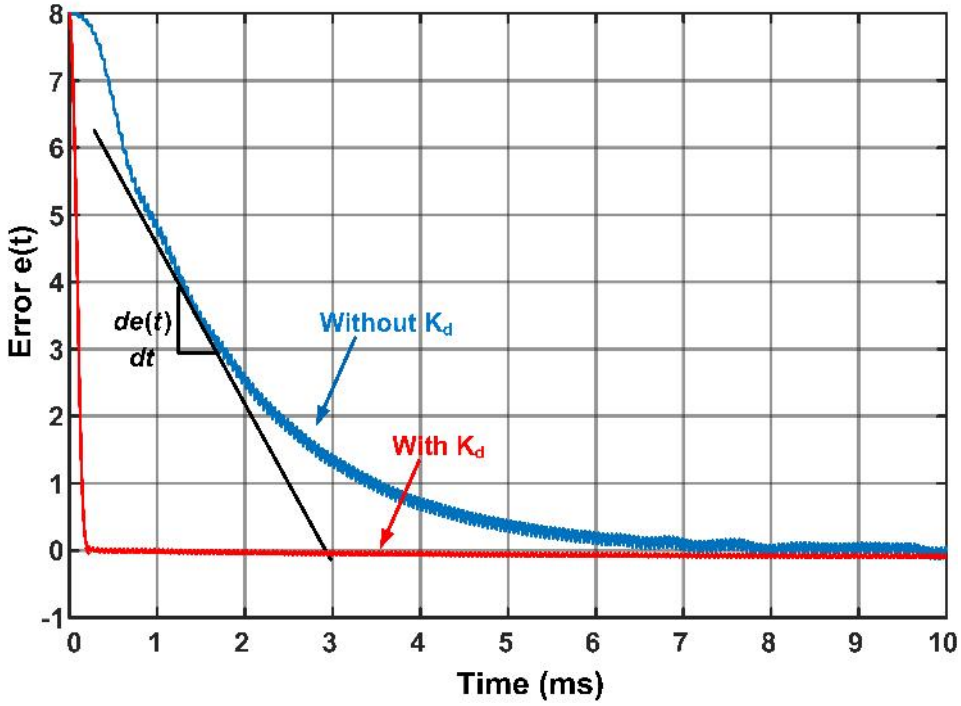
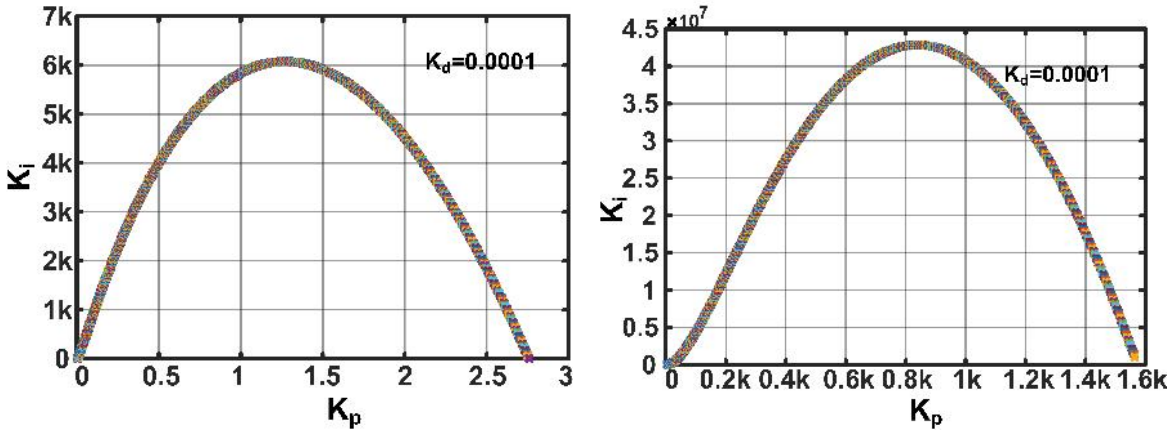
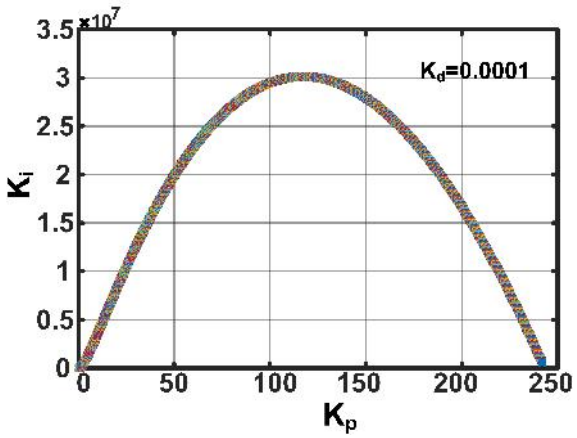


Figure 5.16: Error with derivative and without derivative.

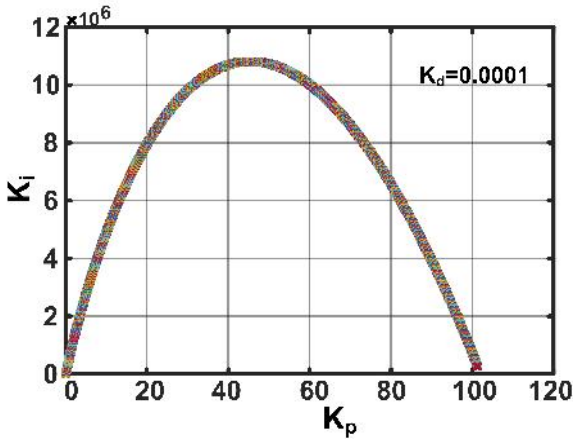


(a)

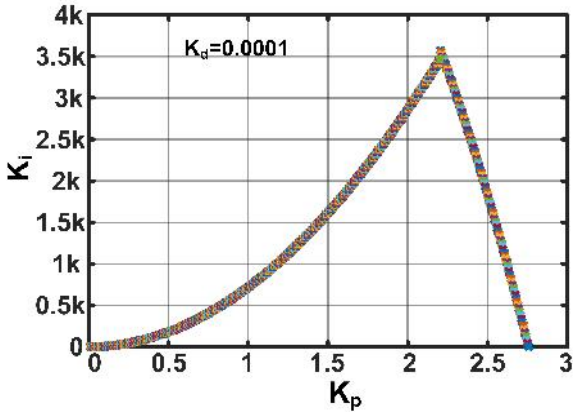
(b)



(c)



(d)



(e)

Figure 5.17: Stability region for all four Kharitonov polynomials for K_d=0.0001 (a)K_1 (b)K_2 (c)K_3 (d)K_4 (e) Common stability region of polynomials.

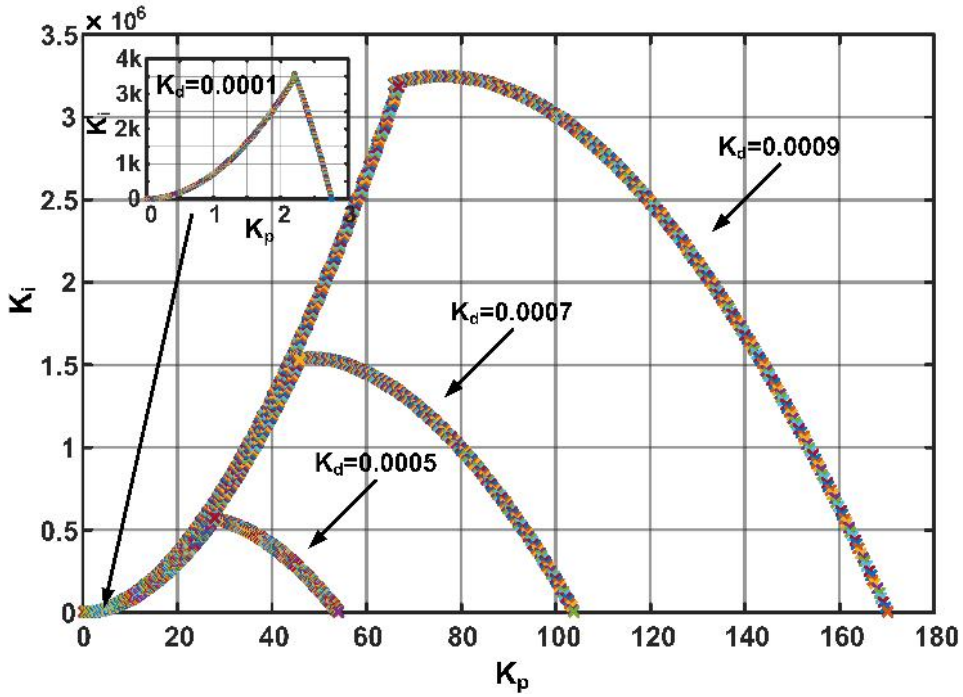


Figure 5.18: Common stability region for DC-DC buck converter for different values of K_d.

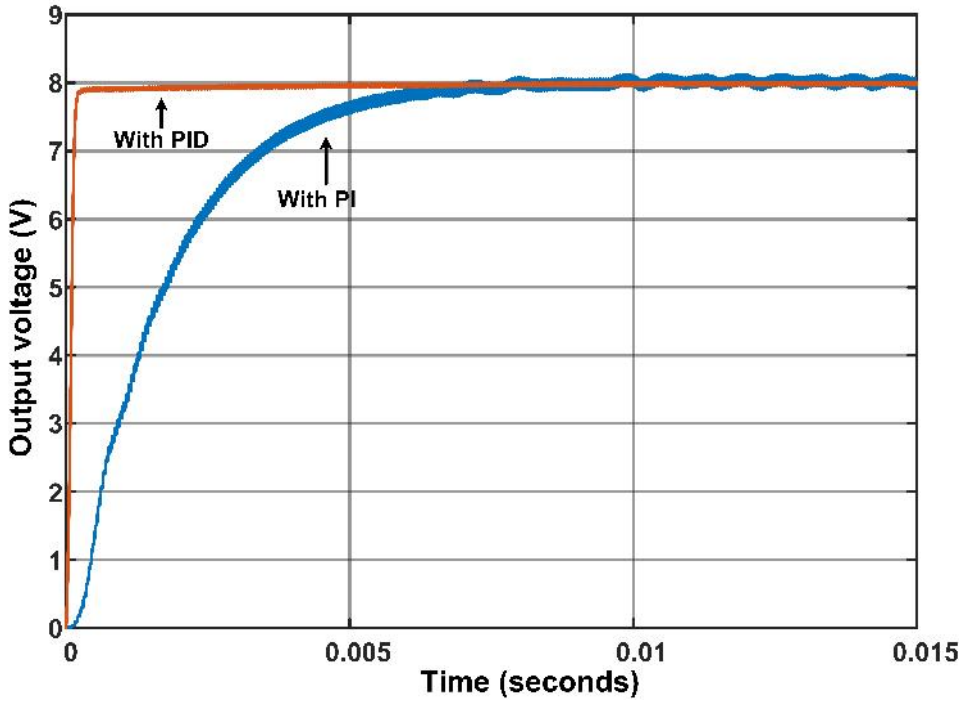


Figure 5.19: Closed loop response of buck converter with PI and PID controllers.

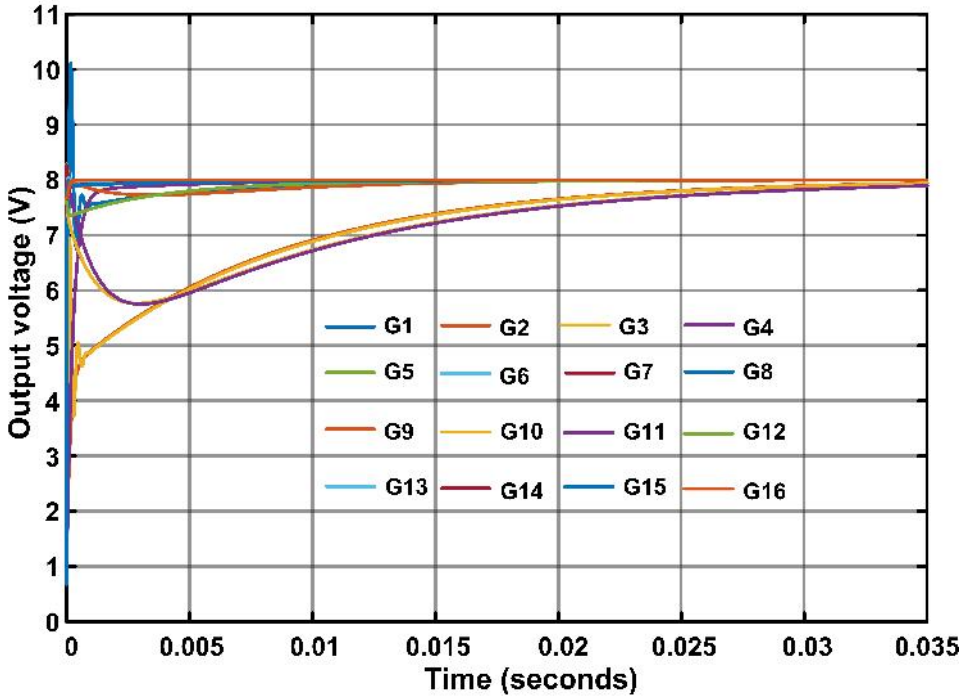
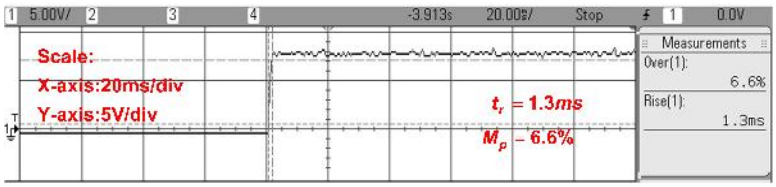


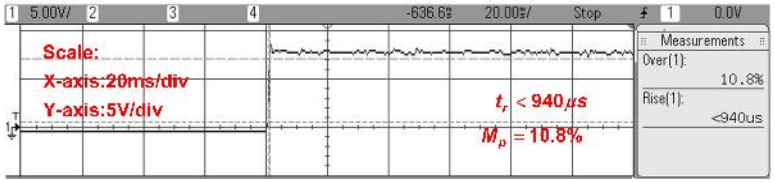
Figure 5.20: Closed loop response of all sixteen transfer functions with proposed PID controller.

compared with the reference voltage and generated error is minimized by designed PID controller. Then, this control voltage from PID output is used as duty cycle of switch. With this PID output pulses generated by using PWM technique. The pulses are taken from the slave PWM of DSPACE DS1104 and given to MOSFET (IRFP460) of buck converter.

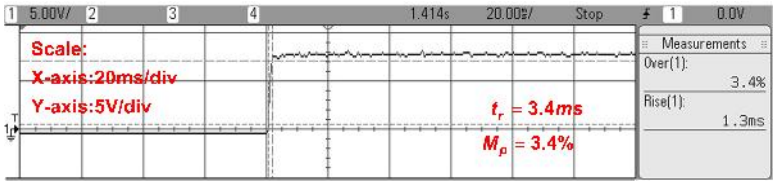
All four Kharitonov polynomials are implemented and which gave the accurate steady state response as shown in Figure 5.21. In order to implement parametric uncertainties practically, experiments are conducted as shown in Table 5.8. The proposed theory is well proved by hardware results, which shows the almost negligible overshoot since phase margin is more than 40° and different speed of responses since gain crossover frequencies are different. In order to test accuracy of the proposed theory, other than four Kharitonov polynomials, we have chosen random parameter values and verified on hardware. This result has been shown in Figure 5.21(e).



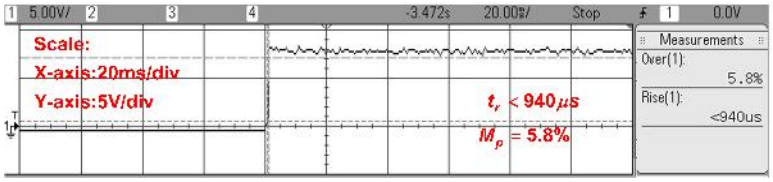
(a)



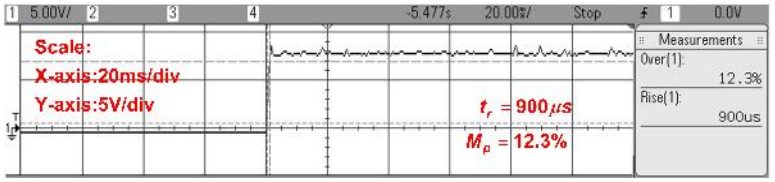
(b)



(c)



(d)



(e)

Figure 5.21: Experimental results for all four Kharitonov polynomials for K_d=0.0001 (a)K_1 (b)K_2 (c)K_3 (d)K_4 (e) For random polynomial.

5.5 Conclusions

This chapter presented the PID controller design for DC-DC converters in two different cases such as when converter parameters are constant and varying within prescribed limits. For converter parameters constant case, a generalised PID based on IMC is proposed for DC-DC converters. The main advantage of proposed controller are

- No need of trial and error method to get PID parameters
- No assumptions to design controller.
- Desired gain crossover frequency is obtained with PID controller (As this is very important for DC-DC converters).
- No need of compensator design.
- If mathematical model is available, then parameters are obtained with straight formulae.

Then, for minimum phase type of systems such as buck is considered and applied proposed technique practically. Further, for non-minimum phase type of systems such as non-ideal DC-DC boost and buck-boost converters are considered. Since these systems shows the non-minimum phase behaviour, the crossover frequency selection and maximum achievable bandwidth is discussed in detail. The simulation results shows the performance of designed controller and it can be observed that as crossover frequency changes, speed of responses are improved. Even in experimental results of boost and buck-boost converters show the performance of proposed controller.

In the next case, a robust PID controller proposed for DC-DC converters, when parameters are varying (Because of heating and ageing effect). Here, a well established Kharitonov theorem and stability boundary locus concepts are utilised. The main contributions in this robust PID design are

- It is shown that only four transfer functions or Kharitonov polynomials are needed to design controller.
- A method is presented to select derivative gain.

Finally, on DC-DC buck converter proposed robust PID controller is implemented. The robust stability region in the (k_p, k_i) plane for different values of k_d, *i.e.*, PID controller region has been determined for uncertain DC-DC buck converter model for desired stability margin and hence the necessary and sufficient condition for robust stability is obtained. The designed controller improved the stability margin of all interval plants. Hence, it is shown that only four transfer functions are sufficient to design controller from the family of interval plant transfer functions. Further, the selection method to chose k_d has been presented.

CHAPTER 6

CONCLUSIONS AND FUTURE SCOPE

The main conclusion of the research work presented in this thesis and the possible future research in this area has been summarized in this chapter

6.1 Conclusion

In this thesis, the design analysis, mathematical modelling and control issues of non-isolated DC-DC converters have been presented. In short, thesis conclusions have been made in two aspects, such as power electronic and control point of view. Boost, buck-boost (Having only single switch) and NIBB (Have two switches) converters have been considered for this work. From power electronics point of view, non-ideal design, analysis of existing converters and a new topology derived from conventional topologies. From control point of view, the non-ideal modelling, transfer function analysis and importantly controller design of converters have been done. For this purpose, two typical type of non-ideal DC-DC converter topologies namely minimum phase converters (NIBB in buck mode) and Non-minimum phase converters (Boost, Buck-boost, NIBB) have been considered. The DC-DC converters have been considered non-ideal while evaluating their design equations and mathematical models. The outcome of this research work on modelling, analysis and control issues can be summarized as follows:

Power electronics point of view:

In the research related to design issues, it was observed that the ideal duty cycle (calculated by considering the converter to be ideal) results in a lesser voltage than the desired. This voltage drop is due to the power loss occurring across the different resistive components of the converter elements. Therefore, the improved expressions for duty cycle of the boost, buck-boost and NIBB converters were de-

rived incorporating the major non-idealities present in the converter elements. Here, analysis of NIBB converter has been special as it has two switches (means two duty cycles). A method to derive improved expression for duty cycle when there are two switches is presented in detail. The critical information such as the maximum achievable output voltage and duty cycle, which are essential for closed-loop operation have been presented. The design equation for inductors and capacitors were also improved considering converters as non-ideal. It is found that the required values of these elements are more in case of non-ideal consideration. Further, the output voltage ripple analysis has been carried out and a formula for maximum possible value of ESR was derived. The ESR of output capacitor less than this maximum value ensures that the output voltage ripple will be within specified limit. The theoretical analysis has been validated by simulation and experimental results.

In continuation of design work, a NIBB derived hybrid converter is proposed from the conventional two-switch non-inverting buck-boost converter, which can supply both DC and AC simultaneously. The uniqueness of the proposed converter is shoot-through problem utilization and ability to supply both AC and DC, which makes distinctive from other conventional converters. Further, the proposed converter is more flexible to get wider operating range of voltage in comparison to other proposed hybrid converter topologies.

Control point of view:

The input voltage to output voltage, load current to output voltage, input current to input voltage and duty cycle to output voltage transfer functions of non-ideal DC-DC boost, buck-boost and NIBB converter were obtained using state-space averaging technique. The ESRs of inductors and capacitors, resistances of switch and diode, and diode forward voltage drop were involved in order to improve the dynamic and steady-state model of the converters. It was found that the non-ideal transfer functions have different steady-state and transient characteristics from the ideal transfer functions. The duty cycle to output voltage transfer function is generally used for control design. It was observed that the duty cycle to output voltage transfer function of

the DC-DC boost, buck-boost and NIBB (in boost or buck-boost modes) converters are non-minimum phase systems having one LHP zero additionally with non-ideal parameters, whereas with the ideal parameter assumptions, it is having only RHP zero. These improved transfer functions were used for the controller design of DC-DC converters.

In order to regulate the output voltage of DC-DC converters in different operating conditions such as when parameters are constant and when parameters are varying, a PID controller is designed. The transfer function models obtained incorporating non-ideal elements of boost, buck-boost and NIBB (in buck mode) converters were used. The IMC based PID controller is designed for both the minimum phase and non-minimum phase converters. The beauty of proposed controller is that, there is no trial and error method used for tuning. The PID parameters are obtained directly from the transfer function model of the converters and with desired bandwidth. Further, the stability boundary locus and Kharitonov's theorem were used to design a robust PID controller. Here, a method is proposed for certain case of systems (for DC-DC buck converters) such that only four kharitonov polynomials are sufficient for designing controller, whereas, in conventional approach sixteen were used. Further, a method is proposed to choose derivative gain.

6.1.1 Future scope

The research work presented in the thesis can further be extended in two aspects as discussed before. Possible future scope of the work are given below:

Power electronics point of view:

1. Though these design, modeling and control issues have been applied for DC-DC boost, buck-boost and NIBB converters in this thesis, but in a similar way with suitable modification, they may be implemented on other type of DC-DC converters.

2. The proposed hybrid converters are very interesting topic. In future, one can work in this area to improve further to eliminate the limitations of proposed converter.

3. As the small-signal averaged model does not reveal the effect of converter

switching frequency on its dynamics. Therefore, the mathematical models of the DC-DC converters can be developed to include the effect of converter switching frequency on its dynamics.

Control point of view:

1. There is a limitation of gain crossover frequency in NMP systems, which creates problem in fast response. So, one can work to resolve this issue in future.

2. The Kharionov's polynomial reduction is presented in the thesis is only for specific case (such as buck converters). So, in future this work can be extended for other type of converters also.

3. In future, presented control design method can be extended to closed loop control of Hybrid converters by proper modifications.

Appendix A

STATE SPACE AVERAGE METHOD

In this appendix, a brief information about the state space average approach is presented.

A.1 Modeling Steps

Step 1: Writing the state equations for each modes of operation

Mode I$(0 < t < t_1)$

$$\dot{x}(t) = \frac{dx\,(t)}{dt} = A_1 x\,(t) + B_1 u\,(t) + J_1 \tag{A.1}$$

$$y\,(t) = C_1 x\,(t) + E_1 u\,(t) + F_1 \tag{A.2}$$

Mode II $(t_1 < t < t_2)$

$$\dot{x}(t) = \frac{dx\,(t)}{dt} = A_2 x\,(t) + B_2 u\,(t) + J_2 \tag{A.3}$$

$$y\,(t) = C_2 x\,(t) + E_2 u\,(t) + F_2 \tag{A.4}$$

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Mode n $(t_{n-1} < t < t_n)$

$$\dot{x}(t) = \frac{dx\,(t)}{dt} = A_n x\,(t) + B_n u\,(t) + J_n \tag{A.5}$$

$$y\,(t) = C_n x\,(t) + E_n u\,(t) + F_n \tag{A.6}$$

Step 2: Obtaining the steady state averaged model

$$\frac{d\bar{x}(t)}{dt} = A(t)\,\bar{x}(t) + B(t)\,\bar{u}(t) + J(t) \tag{A.7}$$

$$\bar{y}(t) = C(t)\,\bar{x}(t) + E(t)\,\bar{u}(t) + F(t) \tag{A.8}$$

where,

$$\begin{aligned}
A(t) &= A_1 d_{n-1}(t) + A_2\left(d_{n-2}(t) - d_{n-1}(t)\right) + ... + A_n\left(1 - d_1(t)\right)\\
B(t) &= B_1 d_{n-1}(t) + B_2\left(d_{n-2}(t) - d_{n-1}(t)\right) + ... + B_n\left(1 - d_1(t)\right)\\
C(t) &= C_1 d_{n-1}(t) + C_2\left(d_{n-2}(t) - d_{n-1}(t)\right) + ... + C_n\left(1 - d_1(t)\right)\\
E(t) &= E_1 d_{n-1}(t) + E_2\left(d_{n-2}(t) - d_{n-1}(t)\right) + ... + E_n\left(1 - d_1(t)\right)\\
F(t) &= F_1 d_{n-1}(t) + F_2\left(d_{n-2}(t) - d_{n-1}(t)\right) + ... + F_n\left(1 - d_1(t)\right)\\
J(t) &= J_1 d_{n-1}(t) + J_2\left(d_{n-2}(t) - d_{n-1}(t)\right) + ... + J_n\left(1 - d_1(t)\right).
\end{aligned}$$

Step 3: Linearising around a operating point and obtain the ac small signal model

$$\begin{aligned}
&\bar{x}(t) = X + \tilde{x}(t), \bar{y}(t) = Y + \tilde{y}(t), \bar{u}(t) = U + \tilde{u}(t)\\
&d_{n-1}(t) = D_{n-1} + \tilde{d}_{n-1}(t), d'_{n-1}(t) = 1 - d_{n-1}(t) = 1 - D_{n-1} - \tilde{d}_{n-1}(t) = D'_{n-1} - \tilde{d}_{n-1}(t)
\end{aligned} \tag{A.9}$$

$$\begin{aligned}
\dot{X} + \dot{\tilde{x}}(t) = &\left[A_1\left(D_{n-1} + \tilde{d}_{n-1}(t)\right) + .. + A_n\left(1 - D_1 - \tilde{d}_1(t)\right)\right](X + \tilde{x}(t)) +\\
&\left[B_1\left(D_{n-1} + \tilde{d}_{n-1}(t)\right) + .. + B_n\left(1 - D_1 - \tilde{d}_1(t)\right)\right](U + \tilde{u}(t)) +\\
&\left[J_1\left(D_{n-1} + \tilde{d}_{n-1}(t)\right) + .. + J_n\left(1 - D_1 - \tilde{d}_1(t)\right)\right]
\end{aligned}$$

$$\begin{aligned}
\Rightarrow\ \dot{X} + \dot{\tilde{x}}(t) = &\left(\sum_{k=n-1}^{1} A_{n-k}D_k\right)X + \left(\sum_{k=n-1}^{1} A_{n-k}D_k\right)\tilde{x}(t) + \sum_{k=n-1}^{1}\left(A_{n-k} - A_{n-k+1}\right)X\tilde{d}_k(t)\\
&+ \sum_{k=n-1}^{1}\left(A_{n-k} - A_{n-k+1}\right)\tilde{d}_k(t)\,\tilde{x}(t) + \left(\sum_{k=n-1}^{1} B_{n-k}D_k\right)U + \left(\sum_{k=n-1}^{1} B_{n-k}D_k\right)\tilde{u}(t) +\\
&\sum_{k=n-1}^{1}\left(B_{n-k} - B_{n-k+1}\right)U\tilde{d}_k(t) + \sum_{k=n-1}^{1}\left(B_{n-k} - B_{n-k+1}\right)\tilde{d}_k(t)\,\tilde{u}(t) +\\
&\left(\sum_{k=n-1}^{1} J_{n-k}D_k\right) + \sum_{k=n-1}^{1}\left(J_{n-k} - J_{n-k+1}\right)\tilde{d}_k(t)
\end{aligned} \tag{A.10}$$

Similarly,

$$\dot{Y}+\dot{\tilde{y}}\left(t\right)=\left[C_1\left(D_{n-1}+\tilde{d}_{n-1}\left(t\right)\right)+..+C_n\left(1-D_1-\tilde{d}_1\left(t\right)\right)\right]\left(X+\tilde{x}\left(t\right)\right)+$$
$$\left[E_1\left(D_{n-1}+\tilde{d}_{n-1}\left(t\right)\right)+..+E_n\left(1-D_1-\tilde{d}_1\left(t\right)\right)\right]\left(U+\tilde{u}\left(t\right)\right)+$$
$$\left[F_1\left(D_{n-1}+\tilde{d}_{n-1}\left(t\right)\right)+..+F_n\left(1-D_1-\tilde{d}_1\left(t\right)\right)\right]$$

$$\begin{aligned}\Rightarrow\ \dot{Y}+\dot{\tilde{y}}\left(t\right)=&\left(\sum_{k=n-1}^{1}C_{n-k}D_k\right)X+\left(\sum_{k=n-1}^{1}C_{n-k}D_k\right)\tilde{x}\left(t\right)+\sum_{k=n-1}^{1}\left(C_{n-k}-C_{n-k+1}\right)X\tilde{d}_k\left(t\right)\\&+\sum_{k=n-1}^{1}\left(C_{n-k}-C_{n-k+1}\right)\tilde{d}_k\left(t\right)\tilde{x}\left(t\right)+\left(\sum_{k=n-1}^{1}E_{n-k}D_k\right)U+\left(\sum_{k=n-1}^{1}E_{n-k}D_k\right)\tilde{u}\left(t\right)+\\&\sum_{k=n-1}^{1}\left(E_{n-k}-E_{n-k+1}\right)U\tilde{d}_k\left(t\right)+\sum_{k=n-1}^{1}\left(E_{n-k}-E_{n-k+1}\right)\tilde{d}_k\left(t\right)\tilde{u}\left(t\right)+\\&\left(\sum_{k=n-1}^{1}F_{n-k}D_k\right)+\sum_{k=n-1}^{1}\left(F_{n-k}-J_{n-k+1}\right)\tilde{d}_k\left(t\right)\end{aligned}\tag{A.11}$$

To obtain the linear model, the second-order non-linear terms (terms having multiplication of two small ac perturbed signals) in (A.10)-(A.11) are neglected and therefore, we get,

$$\begin{aligned}\dot{X}+\dot{\tilde{x}}\left(t\right)=&\left(\sum_{k=n-1}^{1}A_{n-k}D_k\right)X+\left(\sum_{k=n-1}^{1}A_{n-k}D_k\right)\tilde{x}\left(t\right)+\sum_{k=n-1}^{1}\left(A_{n-k}-A_{n-k+1}\right)X\tilde{d}_k\left(t\right)\\&+\left(\sum_{k=n-1}^{1}B_{n-k}D_k\right)U+\left(\sum_{k=n-1}^{1}B_{n-k}D_k\right)\tilde{u}\left(t\right)+\sum_{k=n-1}^{1}\left(B_{n-k}-B_{n-k+1}\right)U\tilde{d}_k\left(t\right)+\\&\left(\sum_{k=n-1}^{1}J_{n-k}D_k\right)+\sum_{k=n-1}^{1}\left(J_{n-k}-J_{n-k+1}\right)\tilde{d}_k\left(t\right)\end{aligned}\tag{A.12}$$

$$\begin{aligned}\dot{Y}+\dot{\tilde{y}}\left(t\right)=&\left(\sum_{k=n-1}^{1}C_{n-k}D_k\right)X+\left(\sum_{k=n-1}^{1}C_{n-k}D_k\right)\tilde{x}\left(t\right)+\sum_{k=n-1}^{1}\left(C_{n-k}-C_{n-k+1}\right)X\tilde{d}_k\left(t\right)\\&+\left(\sum_{k=n-1}^{1}E_{n-k}D_k\right)U+\left(\sum_{k=n-1}^{1}E_{n-k}D_k\right)\tilde{u}\left(t\right)+\sum_{k=n-1}^{1}\left(E_{n-k}-E_{n-k+1}\right)U\tilde{d}_k\left(t\right)+\\&\left(\sum_{k=n-1}^{1}F_{n-k}D_k\right)+\sum_{k=n-1}^{1}\left(F_{n-k}-F_{n-k+1}\right)\tilde{d}_k\left(t\right)\end{aligned}\tag{A.13}$$

These two equations can be further rewritten as

$$\dot{X}+\dot{\tilde{x}}\left(t\right)=\underbrace{AX+BU+J}_{\mathrm{steady-stateterm}}+\underbrace{A\tilde{x}\left(t\right)+B\tilde{u}\left(t\right)+B_d\tilde{d}\left(t\right)}_{\mathrm{smallsignalterm}}\tag{A.14}$$

$$Y + \tilde{y}(t) = \underbrace{CX + EU + F}_{\text{steady-stateterm}} + \underbrace{C\tilde{x}(t) + E\tilde{u}(t) + E_d\tilde{d}(t)}_{\text{smallsignalterm}} \tag{A.15}$$

Where,

$$\begin{aligned} A &= \sum_{k=n-1}^{1} A_{n-k}D_k, B = \sum_{k=n-1}^{1} B_{n-k}D_k, J = \sum_{k=n-1}^{1} J_{n-k}D_k, \\ B_d &= \sum_{k=n-1}^{1} (A_{n-k} - A_{n-k+1})X + \sum_{k=n-1}^{1} (B_{n-k} - B_{n-k+1})U + \sum_{k=n-1}^{1} (J_{n-k} - J_{n-k+1}) \end{aligned} \tag{A.16}$$

and

$$\begin{aligned} C &= \sum_{k=n-1}^{1} C_{n-k}D_k, E = \sum_{k=n-1}^{1} E_{n-k}D_k, F = \sum_{k=n-1}^{1} F_{n-k}D_k, \\ E_d &= \sum_{k=n-1}^{1} (C_{n-k} - C_{n-k+1})X + \sum_{k=n-1}^{1} (E_{n-k} - E_{n-k+1})U + \sum_{k=n-1}^{1} (F_{n-k} - F_{n-k+1}) \end{aligned} \tag{A.17}$$

Equations (A.14)-(A.15) represent the generalized large-signal linear averaged state-space model of a DC-DC converter. It can be separated to obtain steady-state (dc) and small-signal (ac) model as follows:

Steady-state (dc) model

In (A.14)-(A.15), replacing the small-signal terms by zero, we get the steady-state (DC) model as below:

$$\dot{X} = 0 = AX + BU + J \tag{A.18}$$

$$Y = CX + EU + F \tag{A.19}$$

On simplifying (A.18),

$$X = -A^{-1}(BU + J) \tag{A.20}$$

Substituting this value of X into (A.19)

$$Y = -CA^{-1}(BU + J) + EU + F \;\; \Rightarrow \;\; Y = \left(-CA^{-1}B + E\right)U + \left(-CA^{-1}J + F\right) \tag{A.21}$$

Equations (A.20) and (A.21), can be used to obtain the steady-state value of any state variable (inductor current and capacitor voltage) and output variable (output voltage) of DC-DC converter.

Small-signal (ac) model

By replacing the steady-state (DC) terms in (A.14)-(A.15) to zero, we get,

$$\dot{\tilde{x}}(t) = A\tilde{x}(t) + B\tilde{u}(t) + B_d\tilde{d}(t) \tag{A.22}$$

$$\tilde{y}(t) = C\tilde{x}(t) + E\tilde{u}(t) + E_d\tilde{d}(t) \tag{A.23}$$

Step 4: Determining the various transfer functions

Equations (A.22)-(A.23), represent the small-signal state-space averaged model of DC-DC converter. However, to obtain the various transfer functions, the Laplace transform of above state-space model is taken as:

$$s\tilde{x}(s) = A\tilde{x}(s) + B\tilde{u}(s) + B_d\tilde{d}(s) \tag{A.24}$$

$$\tilde{y}(s) = C\tilde{x}(s) + E\tilde{u}(s) + E_d\tilde{d}(s) \tag{A.25}$$

On simplifying,

$$\tilde{x}(s) = (sI - A)^{-1}B\tilde{u}(s) + (sI - A)^{-1}B_d\tilde{d}(s) \tag{A.26}$$

Substituting (A.26) value in (A.25), we get,

$$\tilde{y}(s) = \left[C(sI - A)^{-1}B + E\right]\tilde{u}(s) + \left[C(sI - A)^{-1}B_d + E_d\right]\tilde{d}(s) \tag{A.27}$$

The equations (A.26) and (A.27), can be used to obtain various transfer functions of DC-DC converter.

$$\begin{aligned} \frac{\tilde{x}(s)}{\tilde{u}(s)} &= (sI - A)^{-1}B \\ \frac{\tilde{x}(s)}{\tilde{d}(s)} &= (sI - A)^{-1}B_d \end{aligned} \tag{A.28}$$

$$\begin{aligned} \frac{\tilde{y}(s)}{\tilde{u}(s)} &= C(sI - A)^{-1}B + E \\ \frac{\tilde{y}(s)}{\tilde{d}(s)} &= C(sI - A)^{-1}B_d + E_d \end{aligned} \tag{A.29}$$

Appendix B

SIMPLIFICATION OF EXPRESSIONS

B.1 Ideal Analysis for Output Voltage Ripple

Rewriting Eq. (2.60) and (3.58)

$$\Delta v_o = \frac{\Delta i_L f}{2CD'} \left(\left((I_{mx} - I_o) \frac{D'}{\Delta i_L f} \right)^2 + (Cr_c)^2 \right) + I_o r_c \tag{B.1}$$

As we have consider this as ideal analysis, ESR is zero. So, the ripple will be obtained as

$$\Delta v_o = \frac{D'(I_{mx} - I_o)^2}{2C\Delta i_L f} \tag{B.2}$$

Substitute $I_{mx} = I_L + \frac{\Delta i_L}{2}$,$I_o = D'I_L$, $\Delta i_L = x_L I_L$, where, $x_L = 2x$ (This is only for simplified analysis) in Eq. (B.2) and by simplifying, we get,

$$\Delta v_o = I_L \frac{(D+x)^2 D'T}{4Cx} \tag{B.3}$$

Differentiate Eq. (B.3) with respect to x to get the x value for which Δv_o is minimum. So, we get,

$$x = \pm D \tag{B.4}$$

Substitute Eq. (B.4) in Eq. (B.3) and by simplifying, we get,

$$\Delta v_o = \frac{V_o DT}{RC} \tag{B.5}$$

Substitute Eq. (B.4) in $\Delta i_L = x_L I_L$, we get the relation of ICR in terms of inductor current as

$$\Delta i_L = 2DI_L \left(\frac{L_1}{L_2} \right) \tag{B.6}$$

This relation holds good for a particular value of inductor designed for prescribed duty cycle. If we want to find ICR for all the cases, then the generalized formula is given by

$$\Delta i_L = 2DI_L \left(\frac{L_1}{L_2} \right) \tag{B.7}$$

where, L_1 is inductor value corresponding to operating duty cycle D, L_2 is inductor value designed for operation of converter.

Appendix C

HARDWARE PROTOTYPE DETAILS

In this appendix, a brief information about the implementation of converters experimental setups are presented.

C.1 Simulation and Experimental Setups

The MATLAB/Simulink environment is used for simulation of different converters. Since MATLAB is very well-known tool for modelling, analysis and visualization of proposed or existing systems. As it contains more than 600 mathematical functions and additional toolboxes to make more utilizable. Simulink is a MATLAB add-on software that enables block diagram based modelling and analysis of various systems, which is very useful for power electronic engineers. The power circuits of the converter topologies have been modelled using Sim Power-Systems toolbox of 2015a MATLAB version. The control circuit has been developed using Math Operations, Signal Routing, Sink and Source blocks of Simulink. The simulation sample time has been kept 1e-7 for the execution of power circuit.

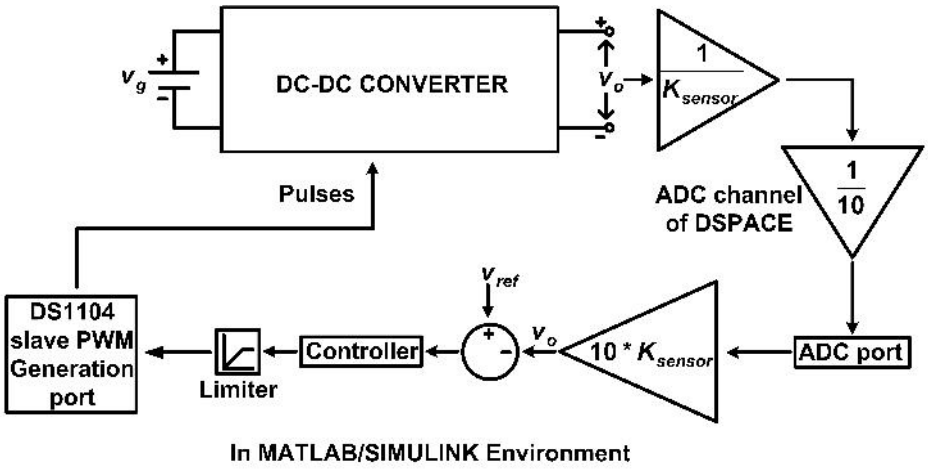
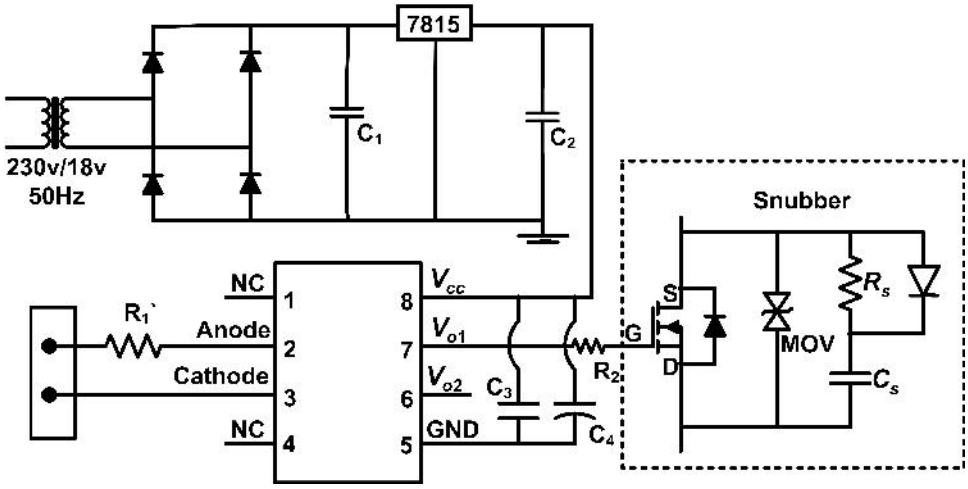


Figure C.1: Schematic complete system.

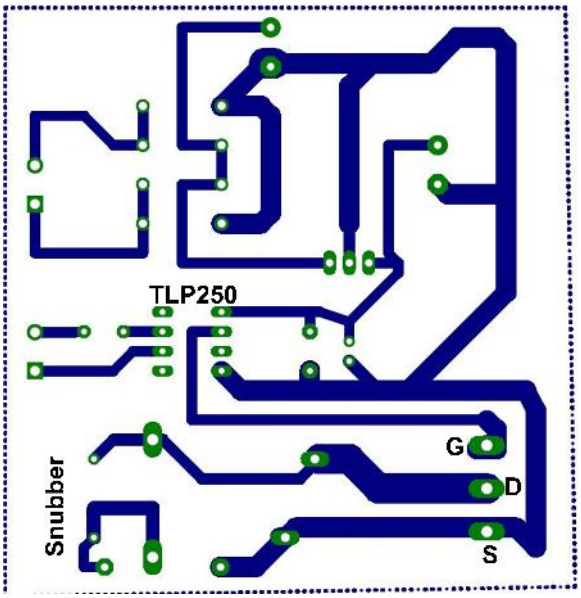
Figure C.1, shows the complete system connection diagram. The experimental

prototype models of boost, buck-boost, NIBB and proposed converters are shown in Figures 2.15, 3.13, 4.10 and 4.36, respectively. The details of components used in the prototypes are as follows:

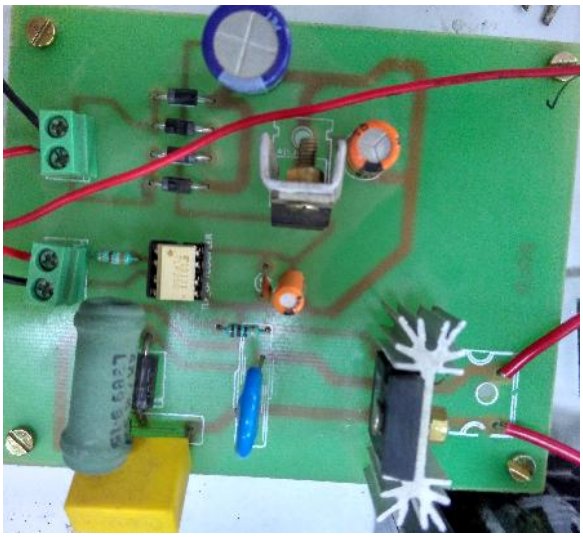
C.1.1 Switch circuit



(a)



(b)



(c)

Figure C.2: Schematic of (a)switch (b)PCB (c)Prototype.

C.1.1.1 Snubber circuit

Switching high current in short time gives rise to voltage transients that could exceed the rating of the MOSFET. Snubbers are therefore needed to protect the switch from transients. Snubber circuit for MOSFET is shown in Figure C.2(a). The diode prevents the discharging of the capacitor via the switching device, which could damage the device due to large discharge current. An additional protective metal oxide varistor (MOV) is used across each device to protect against over voltages across the devices.

C.1.1.2 Pulse amplification and isolation circuit

A circuit diagram the MOSFET driver is made using 8-pin TLP 250 opto-coupler which can be operated upto 25 kHz of switching frequency . However, in this research, the switching frequency was selected as 20 kHz. The driver circuit comprises of +15 V supply, TLP opto-coupler and voltage protection for switch shown in Figure C.2(a). The PWM pulses from the controller are fed between second and third terminals of TLP opto-coupler and magnified PWM pulses are taken at output terminal seven which is connected to gate terminal of the switch. The printed circuit board (PCB) layout and photograph of driver circuit for experimental setup are shown in Figure C.2(b) and (c), respectively.

C.1.2 Sensors

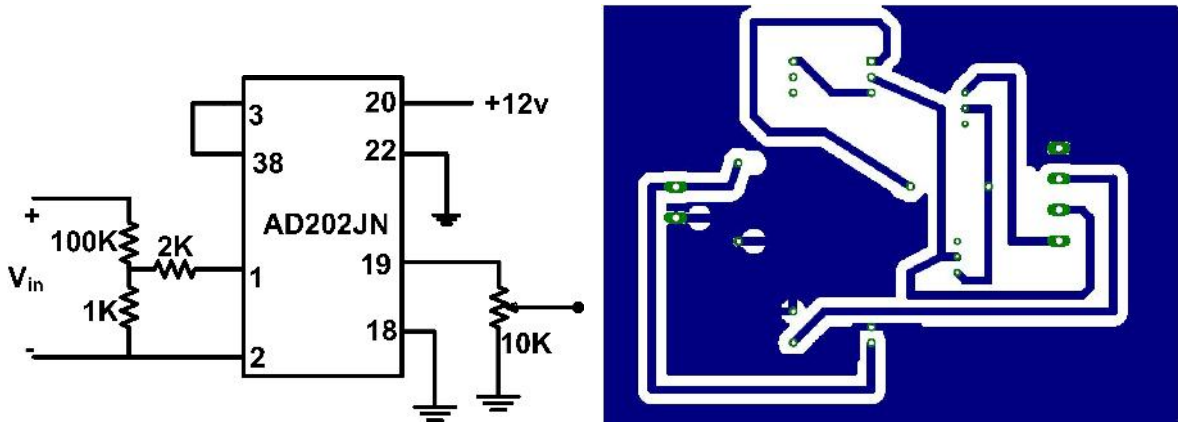
For accurate effective and reliable operation of a system in closed loop measurement of various system parameter and their conditioning is required, which must meet the following requirements:

- high accuracy
- galvanic isolation between high and low voltage side,
- ease of installation
- linearity and fast response, etc.

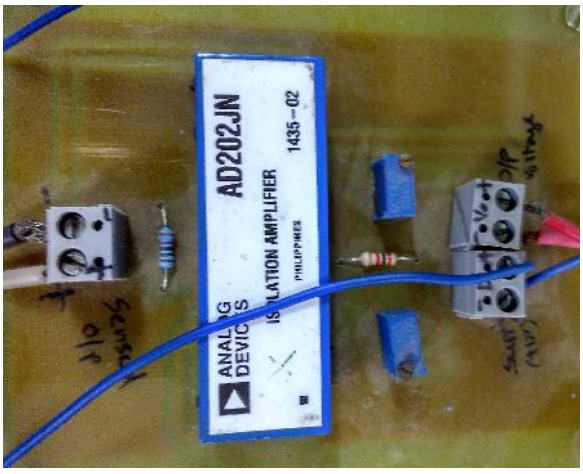
With the availability of Hall Effect current and voltage sensors, these requirements are fulfilled to a great extent. These sensors are now available in variety of range and rating to meet the system requirements. In order to implement the control algorithm following signals are to be sensed

- DC output voltage for controller (PI/PID) processing.
- Inductor and capacitor currents for ripple measurement.

C.1.2.1 Voltage sensor circuit



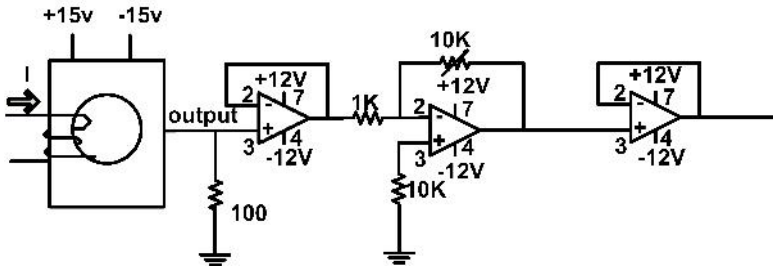
(a) (b)



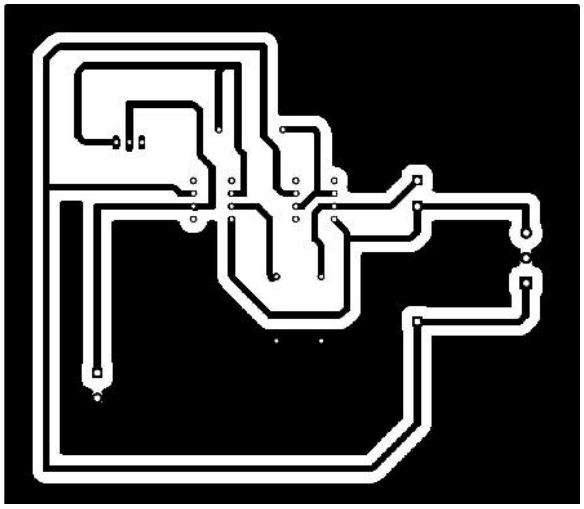
(c)

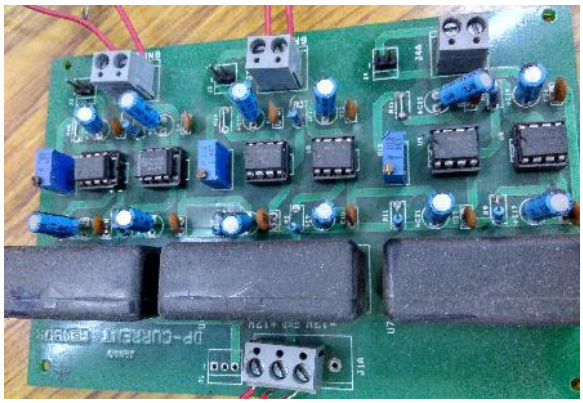
Figure C.3: Schematic of (a)voltage sensor (b)PCB (c)Prototype.

The voltages (ac or dc) are sensed to through AD202JN isolation amplifier which is powered by +15 V supply. In addition, two potentiometers and two resistances are used for the operation of sensing circuit. The main features of AD202JN are: 1) small physical size, 2)High accuracy, 3) Low power consumption and 4) Wide bandwidth. Figure C.3(a) shows a circuit diagram of voltage sensor where sensed voltage is at output terminal 19 of AD202JN.



(a)

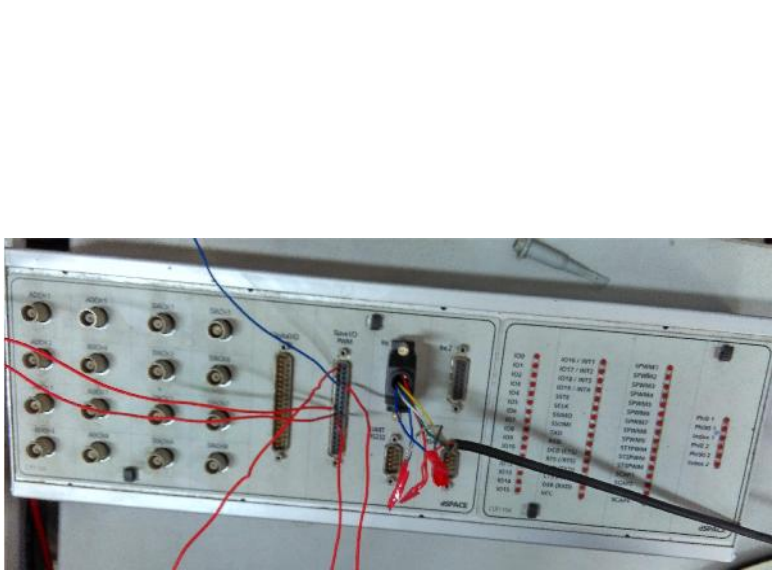




(b) (c)

Figure C.4: Schematic of (a)current sensor (b)PCB (c)Prototype.

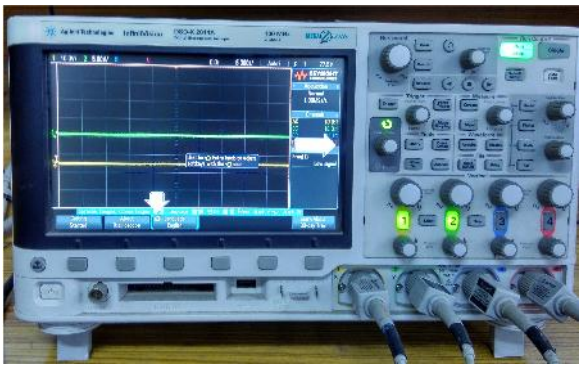
The output of voltage sensor is scaled properly to meet the requirement of the control circuit and is fed to the dSPACE via its ADC channel for further processing. The PCB layout and photograph of voltage sensor for experimental setup are shown in Figure C.3(b) and (c), respectively.



(a)

(b)

(c)



(d)

Figure C.5: Schematic of (a)DSPACE (b)Multiple power supply (PSW 30-36) (c)Multiple power supply (d)DSO.

C.1.2.2 Current sensor circuit

The ac or dc current is sensed using Hall effect sensor (TELCON HTP25). The HTP25 is Hall effect current transformer suitable for measuring current up to 25 A. The current sensors provide the galvanic isolation between the high voltage power circuit and the low voltage control circuit and require a nominal supply voltage of the range -12V to -15V. A dual supply based two operation amplifiers (LF353) is used to convert current signal into voltage signal and scales down the voltage signal at a required magnitude for ADC channel. Figure C.4(a) shows a circuit diagram of current sensor. A PCB layout of current sensor and image of current sensor for experimental setup are shown in Figure C.4(b) and (c), respectively.

C.1.3 DSPACE controller board

The PWM signal for MOSFET (IRFP460) switches is applied through FPGA based controller dSPACE-1104 which has been interfaced with desktop computer. The dSPACE-1104 has 8 ADC/DAC channels, as shown in Figure C.5(a). This has two operating modes, i.e., Master and Slave. For higher switching frequency (5-5 MHz) operation, Slave mode is used, while for low switching frequency range (0-5 kHz), Master mode is used.

For powering the voltage and current sensors, a Scientific multiple power supply PSD 3304 is used, which has three supply terminals as: +30 V/2 A, 5 V/ 5 A and $\pm$15 V/ 1 A, as shown in Figure C.5(c). For input supply, multi range DC power supply PSW 30-36 is used, which can be used for load of 360W, as shown in Figure C.5(b). All experimental waveforms are recorded in Agilent Technology, DSO-X 2014A, as shown in Figure C.5(d).

PUBLICATIONS FROM THE RESEARCH WORK

JOURNALS

1. **Siddhartha Vishwanatha** and Yogesh V. Hote, “Systematic circuit design and analysis of a non-ideal DCDC pulse width modulation boost converter,” *IET Circuits, Devices & Systems*, Vol. 12, Issue 2, pp. 144-156, 2018. (**SCI Indexed, Impact Factor: 1.395**)

2. **Siddhartha Vishwanatha** and Yogesh V. Hote, “A Low Power Non-ideal DC-DC PWM Buck-Boost Converter: Design, Analysis and Experimentation,” *IET Circuits, Devices & Systems*, Vol. 12, Issue 6, pp. 735-745, 2018. (**SCI Indexed, Impact Factor: 1.395**)

3. **Siddhartha Vishwanatha** and Yogesh V. Hote, “Robust PI Controller for Interval Systems With Application to DC-DC Converters,” *International Journal of Control*. (Under review)

4. **Siddhartha Vishwanatha** and Yogesh V. Hote, “Design and Analysis of Two-Switch Buck-Boost (TSBB) Converter with Parasitics,” Submitted to *IEEE Transactions on Circuits and Systems I*.

CONFERENCES

1. **Siddhartha Vishwanatha** and Yogesh V. Hote, “Non-Inverting Buck-Boost Derived Hybrid Converter,” in *Proc. of IEEE International Conference on Emerging Trends in Electrical, Electronics and Sustainable Energy Systems (ICETEES)*, KNIT Sultanpur, India, pp. 1-6, 2016.

2. **Siddhartha Vishwanatha**, Yogesh V. Hote, and Sahaj Saxena, “Non-ideal modelling and IMC based PID Controller Design of PWM DC-DC Buck Converter,” in *Proc. of 3rd IFAC Conference on Advanced PID Control*, Ghent, Belgium, vol. 51, no. 4, pp. 639-644, 2018. [Scopus indexed]

3. **Siddhartha Vishwanatha**, Yogesh V. Hote, “IMC-PID Design of DC-DC Converters Exhibiting Non-minimum phase Characteristics,” in *Proc. of IEEE Power and Energy Conference at Illinois*, Champaign, IL, USA, pp. 1-7, 2019. [*This paper is recommended for possible publications in IEEE Transactions on Industrial Applications*]

4. **Siddhartha Vishwanatha**, Yogesh V. Hote, and J. R. P. Gupta, “Robust PI Controller Design for Perturbed Buck Converter,” *Submitted to INDICON-2019*.

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