INVESTIGATION ON POWER QUALITY IMPROVEMENT USING UPQC

Ph. D. Thesis

by

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in this thesis entitled **"INVESTIGATION ON POWER QUALITY IMPROVEMENT USING UPQC"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electrical Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from January, 2013 to February, 2019 under the supervision of Prof. Pramod Agarwal, Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(**JANARDHANA KOTTURU**)

This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

Date: _____

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The Ph.D. Viva-Voce Examination of ***Mr. Janardhana Kotturu***, Research Scholar, has been held on ……..

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ABSTRACT

The most intensive enlargement industry wise as key equipment for modern power distribution system are the equipments based on power electronic principles. These offers a vast range of advantages for power processing like flexible control, cost reduction, overall size optimization, etc. On the contrary, utilizing these devices gives rise to numerous problems like reactive power shortage and harmonics polluting the power distribution system. The need of excessive reactive power demand leads to poor power factor, bad voltage regulation and a surge in feeder losses with reduced active power flow capabilities of the distribution system. Additionally the situation worsens in the advent of nonlinear loads raising the bar for power quality issues on distribution system. The operation of non-linear equipments on distribution systems like transformers, induction machines, electric arc furnaces, welding equipment, fluorescent lamps (with magnetic ballasts), etc. are also responsible for generation of harmonics in electric power systems. Additionally various perturbations are reported which ranges from sub cycle duration to long term steady state condition leading to distorted waveform. Short disruption, voltage sag, swell, transients of both current and voltage, distorted harmonics and waveforms, voltage fluctuations , flicker, voltage unbalance are few listed interruptions. The severity of the situation lies when there is commence of waveform distortion, flicker, and voltage imbalance at the distribution system regulation of which becomes the prime concern. A slight deviation in magnitude of voltage from its prescribed limit, current and or frequency or waveform impurity results in a potent power quality problem. These power quality problems results into interruption to the normal operation of the electrical equipments that are connected to the distribution system. Modern equipment are highly responsive to the quality of voltage that is being supplied to them. Hence, by improving the power quality takes into account both healthy and efficient distribution system as well as reduced power losses in turn saving upon the cost. To protect the interest of utility, international agencies like IEC, IEEE have been developing various standards (IEC61000, IEEE 519-1992) for harmonic specifications for point of common coupling as well as individual equipment. In addition, these guidelines promote better practices in both power systems and equipment design hence helping to minimize the operational cost.

Conventionally used power quality mitigating devices addresses to a single power quality problem at a single time. This truth lead researchers to develop dynamic and adjustable devices to mitigate multiple power quality problems. A promising approach to it is the Custom Power Devices (CDP's). These devices amends most of the problems of distribution system due to which most of the existing mitigating devices are being replaced by the CDP's reducing the cost as there are less number of overall switches involved. The family of CPDs includes distribution static synchronous compensator (DSTATCOM), dynamic

voltage restorer (DVR) and unified power quality conditioner (UPQC) which is used for compensating the power quality problems in the current and/or voltage waveforms.

The typical custom power device is the distribution static compensator (DSTATCOM) connected in shunt at PCC. Its sole purpose is to diminish the power quality problem related to current on the distribution side. To achieve harmonic filtering, power factor correction and load balancing, the DSTATCOM injects current at the point of common coupling (PCC). An example of custom series compensation device is the dynamic voltage restorer (DVR). Its main motive is to provide protection to sensitive loads from voltage sag/ swell interruptions and harmonics in the supply side. The requisite voltage magnitude and phase angle is injected in series with the distribution feeder utilizing injection transformers and VSI accompanied by the dc-link voltage from the DC storage capacitor. A more modern and relatively versatile approach to the custom power devices is the unified power quality conditioner (UPQC). UPQC comprises of two inverters back to back in conjunction with a common dc-link. It attends to imperfections of both load current and supply voltage making it a substitute of both DSTATCOM and DVR combined.

The present work portraits an extensive and elaborate literature survey of suggested topologies, control strategies of UPQC for the sole purpose of power quality improvement. The adequacy of UPQC with two-level inverter structures has been evaluated for various power quality problems. An extended studies has been performed to multilevel structure of UPQC credits to its unique design which allows a large plethora of high voltage and also reduces the device switching frequency. It is observed that a diode clamed inverter with all the six phases of back to back converter which are sharing a common dc-link is capable of amalgamating desired waveform from several levels of DC voltage. An alluring prospect of investigation would be integration of multilevel diode clamped inverter to UPQC. There are a myriad of features offered by UPQC-ML on deciding the type of control to be used while compensating source voltage (sag, unbalanced voltage, voltage harmonics, current harmonics or reactive power). It also does the same compensating load current playing an important role in the control scheme of back to back inverters. UPQC-3L showcases a much elevated performance in comparison to UPQC-2L as it showcases superior compensating characteristics against distortion in the system. The improvement in the percentage value of THD is also observed for UPQC-3L configuration in comparison to UPQC-2L. Additionally an improved quantity of compensation is seen in with various power quality disturbances for UPQC-3L than UPQC-2L.

A simplified model predictive control for UPQC-2L is proposed, in which predictive voltage control for series converter to maintain a constant value of load voltage during voltage disturbances and predictive current control for shunt converter to maintain source current free from distortions is used without need of multivariable complex mathematical

evaluation. The sensed voltage and current signals of source and load are used to derive the future predicted values of source current and load voltage from the discrete state space model of UPQC. The appropriate switching state is selected and applied to the converters based on the minimization of the cost function, which is selected as the square of the difference between reference and predicted values. Independent generation of reference control signals for both shunt and series converters are performed. The two reference signals are injection voltage by the series transformer into the system, considered for series converter and injectable compensation current by the shunt converter against load distortions, entitled as control reference for shunt converter. In similar way the approach is extended to UPQC-3L configuration with diode clamped multilevel inverter structure. The cost function is modified as the dc-link voltage balancing is mandatory for three-level structure along with series injecting voltage and shunt compensating current signals.

The work also focused on the reducing dc-link voltage rating of UPQC. The thorough literature has been studied on this issue. The requirement of dc-link voltage for shunt and series active filter, for UPQC are different. These fluctuation in values lead to a provocative task to assign a common dc-link of pertinent rating to achieve adequate shunt and series compensation. Conventionally, to achieve legitimate compensation the shunt filter requires higher dc-link voltage in comparison to the series active filter thus to fulfill this criterion, researchers have been left with no preference other than to choose common dc-link voltage on the basis of shunt active filter prerequisites. This leads to over rating of the series active filters as the requisites are less in comparison to shunt active filter. Thus, literature studies have revealed UPQC topologies with elevated dc-link voltage. Hence the voltage source inverters (VSIs) turn out to be bulky due to high value of dc-link capacitor. Additionally, the switch rating has to be chosen with increased value of voltage and current in return the entire cost and size upsurges.

It has been observed in literatures, that few attempts have been initiated to minimize the inverter capacity by lowering the storage capacity of dc-link voltage by introducing hybrid APFs, thus intensifying system reliability. The usage of IGBTs as switching devices in the VSI of active filters cutbacks on the rating of active filter elements in hybrid filters with sensibly elevated rating. As a result it operates at very high frequency contributing to fast response and decrement in size of ripple filter passive elements and size of dc bus capacitor. A combination of shunt passive power filter (PPF) and series APF constitutes the series hybrid APF (SeHAPF). SHAF is gaining popularity due to its reduced capacity and versatile usage. An example to testify the theory would be a hybrid filter as unification of active series filter (5%) and passive series filter (20%) utilizing only 20% rating of load in case of voltage fed loads. Industrial investigation and dedicated research is directed toward series active filters as they are more popular than shunt counterpart due to its simple configuration and

operating procedures. The shunt hybrid active power filters (SHAPFs) are series connection of passive and active filters for ease of operation at a conducive voltage and current in conjunction to high rating of active filter up to 60%-80% of the load. Unified power quality conditioner in comparison to series and shunt active filters receives less attention by the researchers by implementing hybrid structures with passive filters. A hybrid UPQC with a branch of passive filters attached to it, tuned specifically with 3^{rd}, 5^{th}, and 7^{th} order harmonics has been proposed by L.H. Zhou et al. This model reduces the capacity of dc-link of shunt converter compared to conventional UPQC.

The present work proposes an analytic method to control the dc-link voltage of hybrid UPQC. In majority of the UPQC based power quality conditioner, load reactive power compensation is performed by shunt APF. It is so because the utilization factor of the shunt APF is much elevated in comparison to series APF when utilized in steady state operation and is heavily influenced by load reactive power needs. To achieve lower dc-link voltage, the compensation burden on shunt APF rating should be decreased. This can be made possible by adopting phage angle control (PAC). This method enables the sharing of reactive power between series and shunt APFs by introducing a power angle difference between source and load voltage, maintaining the magnitude of voltages for both the APFs equal. The present work makes an attempt to maintain the magnitude of voltage on the dc-link as low as possible by application of PAC to hybrid UPQC which enables to achieve further reduction in dc-link voltage in comparison to conventional UPQC. The algorithm proposed in this work, indirectly identifies the range of minimum possible dc-link voltage for a given load power factor with suitable power angle between source and load voltage. A comparative study is performed for VA loadings and utilization of power electronic converters of the designed hybrid UPQC under different conditions to the traditional UPQC. Additionally, a generalized algorithm is proposed to evaluate optimal dc-link voltage over a percentage range of voltage sag/swell combinations. Thus, the proposed algorithm gives the best fixed minimum dc-link voltage corresponding to within the range fixed by the algorithm based on the compensation level. In this work the maximum dc-link voltages are evaluated for a range of ±10% of system sag/swell index till 50%, at a given phase angle δ varying from 0^0 to 45^0. The analysis of minimum dc-link voltage requirement is simulated in MATLAB Simulink platform for three cases of k: no voltage sag/swell, 20% sag and swell with the combination of load lagging power factor of 0.7 and also validated experimentally.

The feasibility of inclusion of Thyristor Controlled Impedance (TCZ) based PPF in hybrid UPQC is also accessed allowing for a broader range of loading reactive power from lagging to leading power factor. The TCZ-PPF enables to further minimize the dc-link voltage of hybrid UPQC in comparison to the PPF based hybrid UPQC over wide range of compensation. In an Ideal case, the dc-link voltage requirement is zero inside the

compensating angle and vice-versa for outside the range of TCZ-PPF. Additionally, the minimum dc-link voltage is also evaluated for the compensation of current harmonics that are injected by the presence of nonlinear loads apart from the reactive power compensation. Three cases have been accessed to analyse the performance of the proposed topology: border point, inside the TCZ-PPF reactive power compensation range and outside the range. To accomplish minimum requirement of minimum dc-link voltage outside the compensating range, PAC control has been implemented. In addition to that, the influence of voltage sag on the dc-link voltage requirement is also scrutinized for three cases of loading reactive power.

The study focuses on the reduction of cost of UPQC by downsizing the number of components. Due to its easy adaptability, an increase in research interest has taken place in which prime focus has been to improve the performance, efficiency and reduction of size and cost. Numerous topologies have come to lamplight in an effort for reduction of size and cost whilst maintaining its performance and efficiency. A reduction in the number of components can lead to a reduction in the cost of a UPQC. The major component of UPQC is series injection transformer. A Transformer-less series injection (TLSI) UPQC is an example of component reduction of UPQC. The size is so selected that it prevents problems occurring due to magnetization current demand from erratic voltage compensation and possible saturation of transformer due to DC biasing. This Thesis introduces TLSI-UPQC with its construction and explains its mode of operation. The topology integrates UPQC directly with in-coming distribution transformer averting the requirement of series injection transformer. This topology takes advantage of its location, a UPQC places in later to the distribution transformer towards the loads. The leverage provided by the topology is cost reduction and minimizing the requisite of bulky series injection transformers. This design cannot be implemented in single-phase loads due to the absence of physical neutral point. An alternative is to provide an additional forth leg in the shunt converter. Proper control strategy is designed enabling virtual neutral point for transformers on the distribution end and neutral current paths for the unbalanced loads. The proposed topology is simulated in MATLAB Simulink platform and the results are validated through an experimental prototype, which is developed in the laboratory. The experimental results show the validity and effectiveness of the proposed topology in accordance with the simulation results.

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(Janardhana Kotturu**)**

CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS

3P3W	Three-phase, Three-wire
3P4W	Three-phase, Four-wire
ac, AC	Alternating Current
APF	Active Power Filter
CSD	Custom Power Device
CSI	Current Source Inverter
dc, DC	Direct Current
DCMLI	Diode Clamped Multilevel Inverter
DSO	Digital Storage Oscilloscope
DSP	Digital Signal Processor
D-STATCOM	Distribution Static Synchronous Compensator
DVR	Dynamic Voltage Restorer
EMI	Electro Magnetic Interference
FACTS	Flexible AC Transmission System
FCMLI	Flying Capacitor Multilevel Inverter
H-UPQC	Hybrid UPQC
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical & Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
KF	Kalman Filter
LPF	Low Pass Filter
LSPWM	Level-shifted Pulsewidth Modulation
MLI	Multilevel Inverter
MOSFET	Metal Oxide Semiconductor Field-effect Transistor
MPC	Model Predictive Control
PAC	Phase Angle Control
PCC	Point of Common Coupling
pf, PF	Power Factor
PI	Proportional and Integral
PPF	Passive Power Filter
PR	Proportional Resonant
PWM	Pulsewidth Modulation
rms, RMS	Root Mean Square
SVM	Space Vector Modulation
TCR	Thyristor Controlled Reactor
TCZ	Thyristor Controlled Impedance

THD	Total Harmonic Distortion
TLSI-UPQC	Transformer–Less Series Injection UPQC
UPQC	Unified Power Quality Conditioner
UPQC-2L	Two-Level UPQC
UPQC-3L	Three-Level UPQC
UPQC-D	3P3W to 3P4W Distributed UPQC
UPQC-DG	Distributued Generator integrated with UPQC
UPQC-I	Interline UPQC
UPQC-L	Left shunt UPQC
UPQC-MC	Multi-Converter UPQC
UPQC-MD	Modular UPQC
UPQC-ML	Multi-Level UPQC
UPQC-P	UPQC mitigates sag by controlling active power
UPQC-Q	UPQC mitigates sag y controlling reactive power
UPQC-R	Right shunt UPQC
UPQC-S	UPQC mitigates sab by controlling both active and reactive power
UPQC-VA_{min}	Minimum VA loading UPQC
VSI	Voltage Source Inverter

LIST OF SYMBOLS

v_{Sa}, v_{Sb} and v_{Sc}	Three-phase source voltages
i_{Sa}, i_{Sb} and i_{Sc}	Three-phase source currents
i_{La}, i_{Lb} and i_{Lc}	Three-phase load currents
i_{sh_a}, i_{sh_b} and i_{sh_c}	Three-phase shunt compensating currents
m	Number of levels in inverter
f_{cr}	Carrier signal frequency
f_m	Modulating signal frequency
m_a	Amplitude modulation index
m_f	Frequency modulation index
L_s	Source inductance
L_{sh}	Coupling inductor of shunt converter
L_{ac}	Commutation inductance
p, q	Instantaneous real and reactive powers
R_s	Source resistance
V_{dc}	Reference dc-link voltage
k_p, k_i	Proportional and integral gains
i_{Sn}	Source neutral current
i_{Ln}	Load neutral current
S_{UPQC}	VA loading of UPQC
$S_{H\text{-}UPQC}$	VA loading of hybrid UPQC
V_{dcl}	Upper dc-link voltage of UPQC-3L
V_{dcu}	Lower dc-link voltage of UPQC-3L
V_{t_abc}	Three-phase terminal voltages
V_{inj_abc}	Three-phase series injected voltages
Z_s	Source impedance
Z_{PPF}	Impedance of PPF
δ	Phase angle between terminal voltage and load voltage
γ	Angle of series injected voltage wrt terminal voltage
Φ_L	Load power factor angle

CHAPTER 1: INTRODUCTION

This chapter describes introduction to the research work. It will start with some background on foremost power quality problems in distribution systems. Then, the solutions to the problems will be discussed. The power quality problems are discussed in terms of voltage and current profile of various commonly used appliances and also the load profile of the department electrical supply system. After discussion about power quality problems, the detailed possible solutions are presented. The literature survey is conducted on custom power devices. The literature survey is extended to unified power quality conditioner in detail about various topology structures and control strategies as it is considered the research topic of this thesis. Next, scope of work, author's contribution and thesis outlines are explained.

The very inception of interconnected power networks lead to the use of alternating current (AC) circuits as a commonplace. In these power networks, the basic function of generators is to produce a clean sinusoidal voltage waveform, of constant frequency, at their terminals. However, a pure sinusoidal waveform with zero distortion is a hypothetical entity and not a practical one. The voltage waveform, even at the point of generation, contains a small amount of distortion, due to non-uniformity in the excitation magnetic field and discrete spatial distribution of coils around the generator stator slots. The distortion at the point of generation is usually very low, typically less than 1.0%. In past, majority of the loads in power distribution systems were of constant in nature, as regards to power, impedance, current or any of their combination. Such loads include incandescent lighting, heating, AC motors, etc., and are termed as linear loads. However, in recent years, the requirement for more efficient operation of electrical equipment and energy conditioning has led to the advancement in semiconductor technologies and introduction of new power electronic devices. This has significantly changed the nature of load composition because these power electronics based loads are nonlinear in nature. This nonlinearity results in non-sinusoidal load currents, which are periodic in nature and usually reflect Fourier series expansions. Non-sinusoidal periodic waves contain fundamental and higher order frequency components. These higher order frequency components are called harmonics. Harmonics can be defined as the undesirable components of a distorted periodic waveform whose frequencies are the integer multiples of the fundamental frequency [1]–[10].

The injected harmonics are responsible for the distortion of voltage and current wave shapes. A substantial amount of these harmonics are produced by high rating power converters. Other devices responsible for generation of harmonics are static var compensators, adjustable speed drives, power supplies, transformers, arc furnaces, personal computers, cyclo-converters, etc. In future, there may be many more new harmonic sources, such as fuel cells, battery storage devices, photovoltaic cells, etc. Non-sinusoidal currents generated by the nonlinear loads are propagated throughout the network, causing voltage drops across the impedance of transmission lines and transformers. Thus, the voltage at the

point of common coupling (PCC) is no longer sinusoidal, but periodic and also possesses Fourier series expansions. The quantum of voltage distortion depends on the line impedance and the magnitude of current. When several power users share a common power line, the voltage distortion produced due to harmonic current injection by one user can impact the quality of power supplied to others. Due to this, standards have been issued to limit the amount of harmonic currents fed into the source by an individual customer [6].

1.1 Electric Power Quality

Electric power quality is defined in many ways depending on one's frame of reference based on utility, manufacturer and customer view. Power quality is ultimately a consumer driven issue, and the end user's point of reference takes precedence. Therefore, the power quality is defined as "*Any power problem manifested in voltage, current, or frequency deviations that result in the failure or mis-operation of customer equipment*". The definition of power quality given in the IEEE dictionary [63] originates in the IEEE Std 1100 reads as "*Power quality is the concept of powering and grounding sensitive equipment in a matter that is suitable to the operation of that equipment*". The prospective of the customers of electric power is to have an ideal voltage waveform. Thus, the customer interest in power quality is mainly the voltage quality. On the other hand, utilities concern is focused on both voltage and current quality. This classification motivates to mention definitions of voltage and current quality [54].

1.1.1 Power Quality Problems

Power quality has never been an important concern until 1980. This is because from 1960-70, the primary concern revolved around the availability of electrical supply [1]. However, by 1980, reliability of the electrical supply has reached 99.9999% for developed countries and the loads installed during these times were mainly linear loads and introduced little pollutions to the network. They include:

- Motor loads
- Resistive heating loads
- Melting plants

However, from 1970-1980, there was an energy crisis [1]–[3]. This brought about a price hike in oil, which prompted increasing emphasis on the system efficiency. This led to a growth in the usage of power electronic devices or loads that were driven by power electronics [4]–[7]. Although they promise high operational efficiency, they cause distortions, or degrade the power quality in power systems. Some of these devices or loads are:

- Converter loads (e.g., switched-mode power supplies)
- Light dimmers
- Arching loads (e.g., furnaces, smelters)

Furthermore, electrical equipment or processes are interconnected together in the network. Hence, they are exposed to any disturbances that may occur in the network. For example, failure of an equipment or process due to degradation in the power quality can have important consequences on other equipment or processes. This can cause inconvenience and/or financial loses to them. Thus, there is an increasing awareness to improve the power quality in power systems, in addition to maintaining reliable power supply.

The power quality problem is characterized by the following parameters by considering the voltage and current waveform [71].

- Perfectly sinusoidal waveform; no distortion, spikes, dips
- Balance and perfect symmetry of the amplitude and phase phases
- RMS within allowable limits
- Frequency stability
- Power factor within tolerable limits

Disturbances are all internal and external phenomena to the network with a power to amend a transitional or permanent in amplitude and / or shape of the electrical parameters of the network (current, voltage, frequency). These disturbances can be classified according to two criteria: the length of time or the method of allocation is to say, their effects on electrical parameters. There are a number of power quality problems in the present-day fast-changing electrical systems. These may be classified on the basis of events such as transient and steady state, the quantity such as current, voltage, and frequency, or the load and supply systems.

In most of the cases, the voltage takes into account, as the quality of the voltage is the addressed issue for the sake of convenience. The voltage quality is mainly recognised by the three factors as magnitude, wave shape and frequency. The detailed classification and characteristics of the above power quality problems are given in Table 1.1 [1].

Major Power Quality Problems

The important power quality problems at the distribution level are presented in terms of pictorial view in Figure 1.1 and few of them are discussed below [2].

- **Voltage Sag:** It is a decrease in rms value of supply voltage for a short duration. The duration of voltage sag may vary between 5 cycles to a minute. Voltage sags can be caused by the system faults, increased load demand, transitional events such as large motor starting, etc.
- **Voltage Swell:** It is an increase in rms value of supply voltage for a short duration. The duration of voltage swell may vary between 5 cycles to a minute. Voltage swells can be by to system faults, switching off of large rated loads, etc.

- **Voltage Flicker:** A very rapid change in the supply voltage is called as voltage flicker. These are systematic random variations in supply voltages. The arc furnace is one of the most common causes of voltage flicker on utility transmission and distribution systems.

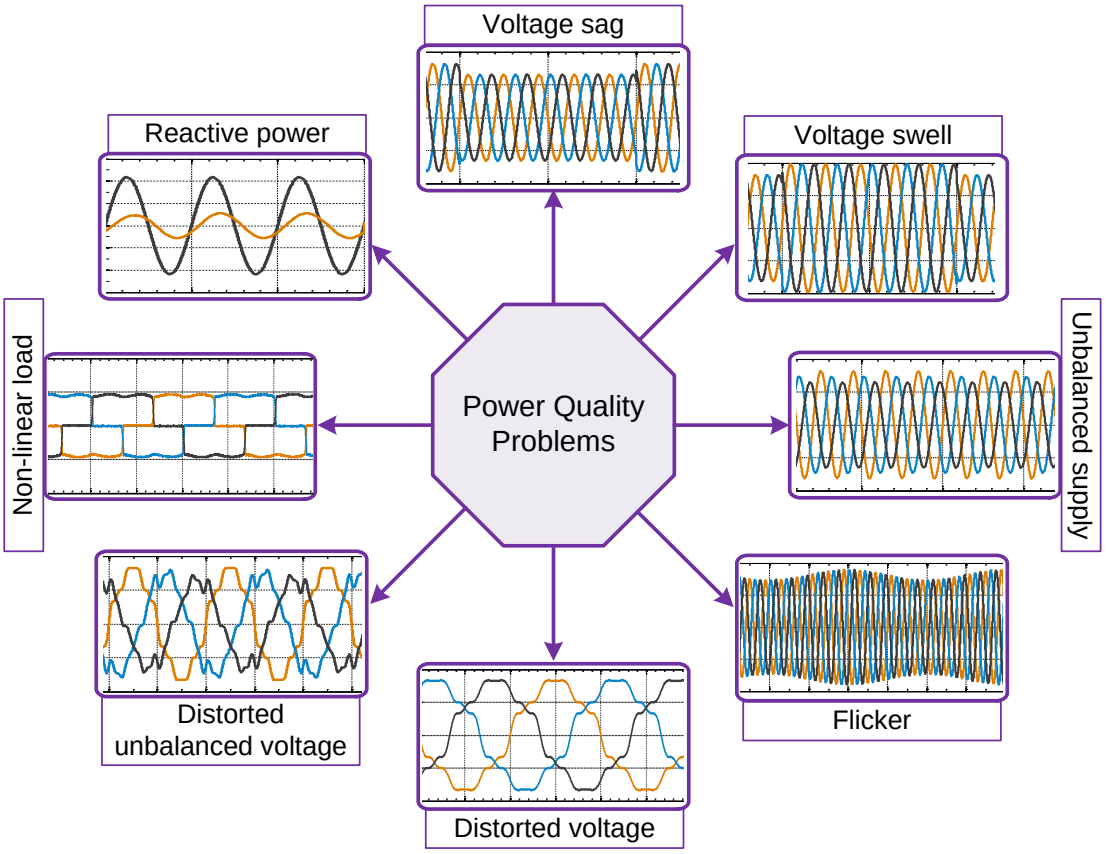


Fig. 1.1: Pictorial view of major power quality problems

- **Waveform Distortion:** It is a steady state deviation in the voltage or current waveform from an ideal sine wave at a fundamental supply frequency, characterized by the spectral content of the deviation. These distortions can be classified as DC offset, harmonics, notching and noise.
- **Harmonics:** Harmonics are sinusoidal voltages or currents having frequencies that are integral multiples of the fundamental supply voltage frequency. Harmonic distortion is caused by the nonlinear characteristics of devices and loads on the power system. The term total harmonics distortion (THD) gives the measure of harmonics content in a signal and is generally used to denote the level of harmonics present in the voltage/current. High harmonic amplitudes may not only cause malfunctions, additional losses and overheating, but also overload the power distribution network and overheat the neutral conductor and cause its burn out. The harmonics can generate additional acoustic noise from motors and other apparatus, reducing the motor efficiency and also can cause interference with neighboring telephone lines.

- **Unbalance:** The voltage/current unbalance is a condition in which the voltages/currents of the three phases of the supply are not equal in magnitude. Furthermore, they may not even be equally displaced in time. The primary cause of voltage/current unbalance is the single-phase load on three-phase circuits. Severe imbalance can result during single phasing conditions when the protection circuit opens up one phase of a three-phase supply.

Table 1.1: Classification and characteristics of power quality problems [1]

Sources of harmonies				
Category		Typical spectrum content	Typical duration	Typical voltage magnitude
Transient	Impulsive			
	Nanosecond	5 ns rise	<50 ns	
	Microsecond	1 μs rise	50 ns-1 ms	
	millisecond	0.1 ms rise	>1 ms	
	Oscillatory			
	Low frequency	<5 kHz	0.3-50 ms	0-4 pu
	Medium frequency	5-500 kHz	20 μs	0-8 pu
	High frequency	0.5-5 MHz	5 μs	0-4 pu
Short duration variation	Instantaneous			
	Interruption		0.5-30 cycles	<0.1 pu
	Sag		0.5-30 cycles	0.1-0.9 pu
	Swell		0.5-30 cycles	1.1-1.8 pu
	Momentary			
	Interruption		0.5 cycle-3 s	<0.1 pu
	Sag		0.5 cycle-3 s	0.1-0.9 pu
	Swell		0.5 cycle-3 s	1.1-1.4 pu
	Temporary			
	Interruption		3 s-1 min	<0.1 pu
	Sag		3 s-1 min	0.1-0.9 pu
	Swell		3 s-1 min	1.1-1.2 pu
Long duration variation	Sustained interruption		>1 min	0.0 pu
	Under voltage		>1 min	0.8-0.9 pu
	Over voltage		>1 min	1.1-1.2 pu
Voltage imbalance			Steady state	0.5-2%
Waveform distortion	DC offset		Steady state	0-0.1%
	Harmonics	0-100th	Steady state	0-20%
	Interharmonics	0-6 kHz	Steady state	0-2%
	Notching		Steady state	
	Noise	Broadband	Steady state	0-1%
Voltage fluctuation		<25 Hz	Intermittent	0.1-7%
Power frequency variations			<10 s	

1.1.2 Power Quality Standards

The Power quality standards are needed in the power quality industry. The power quality industry recognizes that power quality standards are critical to the viability of the industry. Therefore, stakeholders in the power quality industry have developed several power quality standards in recent years. They recognize that the increased interest in power quality has resulted in the need to develop corresponding standards. They realize that the increased use of sensitive electronic equipment, increased application of nonlinear devices to improve energy efficiency, the advent of deregulation, and the increasingly complex and interconnected power system all contribute to the need for power quality standards. Standards set voltage and current limits that sensitive electronic equipment can tolerate from electrical disturbances. Utilities need standards that set limits on the amount of voltage distortion their power systems can tolerate from harmonics produced by their customers with nonlinear loads. End users need standards that set limits not only for electrical disturbances produced by utilities but also for harmonics generated by other end users.

The organizations responsible for developing power quality standards are the following: Institute of Electrical and Electronics Engineers (IEEE), International Electrotechnical Commission (IEC), Computer Business Equipment Manufacturers Association (CBEMA), National Institute of Standards and Technology (NIST), National Fire Protection Association (NFPA), Electric Power Research Institute (EPRI), Information Technology Industry Council (ITIC), Semiconductor Processing Equipment Voltage Sag Immunity (SEMI) etc.

The different standards for different power quality problems are tabulated in the following Table. 1.2.

Table 1.2: Power quality standards [1].

Power quality problem	Standards
Classification of power quality	IEC 61000-2-5: 1995, IEC 61000-2-1:1990, IEEE 1159:1995
Transients	IEC 61000-2-1:1990, IEC 816:1984, IEEE 1159:1995
Voltage sag/swell and interruptions	IEC 61000-2-1:1990, IEEE 1159:1995
Harmonics	IEC 61000-2-1:1990, IEC 61000-4-7:1991, IEEE 519:1992
Voltage flicker	IEC 61000-4-15:1997

Harmonic Standards

The certain indices have developed to provide a measurement on the severity of harmonic distortion in terms of the effective value of a waveform. The most commonly used indices are Total Harmonic Distortion (THD) and Total Demand Distortion (TDD). The current

and voltage harmonics in the system are often expressed by using these indices. THD is defined as the ratio of all harmonic components to the fundamental component.

$$THD_X = \frac{\sqrt{\sum_{h=2}^{\infty} X_h^2}}{X_1} \quad (1.1)$$

Where, X_1 is the rms (root-mean-square) value of fundamental component and X_h is the rms value of h harmonic component of the quantity X. Hence current THD is the ratio of the root-mean-square of the harmonic currents to the fundamental current.

$$THD_I = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \quad (1.2)$$

The IEEE Standard 519-1992 establishes harmonic current distortion limits at the point of common coupling (PCC). THD represents the harmonics content with respect to the actual load current at the time of measurement. It is important to note that a small load current may have a high THD value but may not be significant threat to the system as the magnitude of harmonics is quite low. This is quite common during light load conditions. Some analysts have attempted to avoid this difficulty by referring THD to the fundamental of the peak demand load current rather than the fundamental of the present sample. This is called Total Demand Distortion (TDD) and serves as the basis for the guidelines in IEEE Standard 519-1992, Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems. It is defined as follows:

$$TDD_I = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_L} \quad (1.3)$$

Where, I_L is the peak or maximum load current at the fundamental frequency component over a considerable period of time at PCC. TDD limits are based on the ratio of system's short circuit current to load current (I_{sc}/I_L). This is used to differentiate a system and its impact on voltage distortion of the entire power system. The short circuit capacity is measure of the impedance of the system. Higher the system impedance, lower will be the short circuit capacity and vice versa. The limits, summarized in Table 1.3, are dependent on the customer load in relation to the system short-circuit capacity at the PCC [2]. Furthermore, IEEE also developed similar standard for voltage distortion in IEEE Standard 519-1992, as shown in Table 1.4. The limits on voltage are set 5% for THD and 3% of fundamental for any single harmonic at PCC level. Harmonic levels above this may lead to erratic functioning of equipment. In critical application like hospitals and airports, the limits are more stringent (less

than 3% THD_V) as erroneous operation may have severe consequences. As discussed already, the harmonic voltage will be higher downstream in the system.

Table 1.3: IEEE-519 current harmonic distortion limits [2].

I_{SC}/I_L	h < 11	11 ≤ h < 17	17 ≤ h < 23	23 ≤ h < 35	35 ≤ h	TDD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Where, I_{sc} is the maximum short-circuit current at PCC (can be measured as $MVA/(\%Z * V)$ and I_L is the maximum demand load current (fundamental frequency component) at PCC.

Table 1.4: Harmonic voltage distortion limits in percent of nominal fundamental frequency voltage [2].

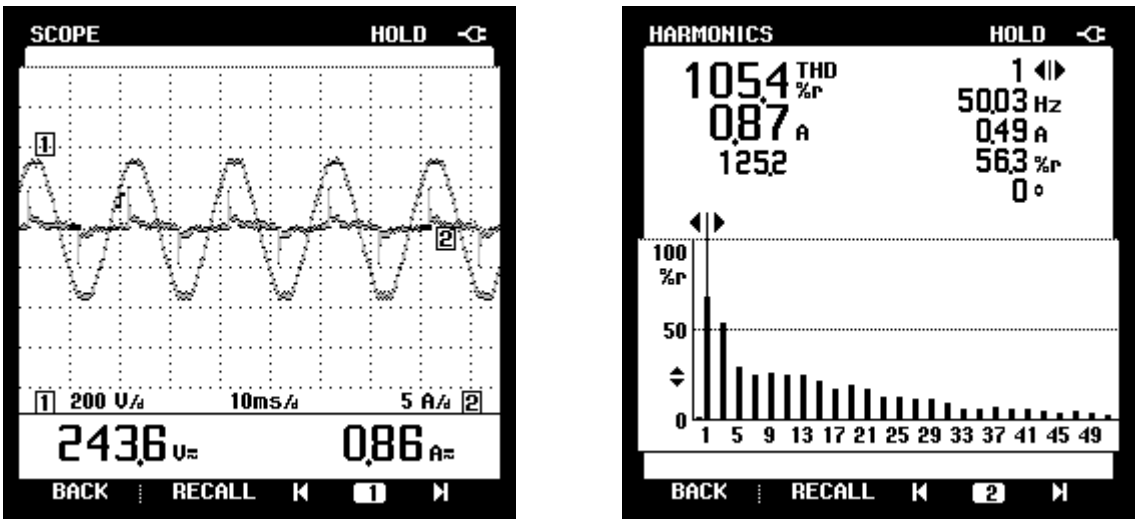
Bus voltage at PCC	Maximum individual harmonic component, %	Maximum THD, %
≤ 1 kV	5.0	8.0
1 kV ≤ V ≤ 69 kV	3.0	5.0
69 kV ≤ V ≤ 161 kV	1.5	2.5
> 161 kV	1.0	1.5

1.2 Survey of Power Quality Problems

The operation of non-linear and unbalanced loads on distribution systems results in low power factor, poor voltage regulation, harmonics currents, load unbalance and excessive neutral current. The increased reactive power, harmonics and unbalance cause an increase in line losses, and voltage distortion in the power system. For completeness, the aforementioned problems are practically analysed with the most common daily use of home appliances and survey related to the electric power usage of the Electrical Engineering department.

(A) Mobile Charger

In today's life, mobiles are the vital part of our life style which is used by everyone. It is the most common type of the single-phase non-linear load, which injects the current harmonics into the supply system. The single-phase Fluke power quality meter is used to capture the waveforms and harmonic spectrum. The current drawn by the mobile charger of Samsung is shown in Figure. 1.2, along with its harmonic spectrum. Form the harmonic spectrum it is clear that the THD of source current is 105.4%.

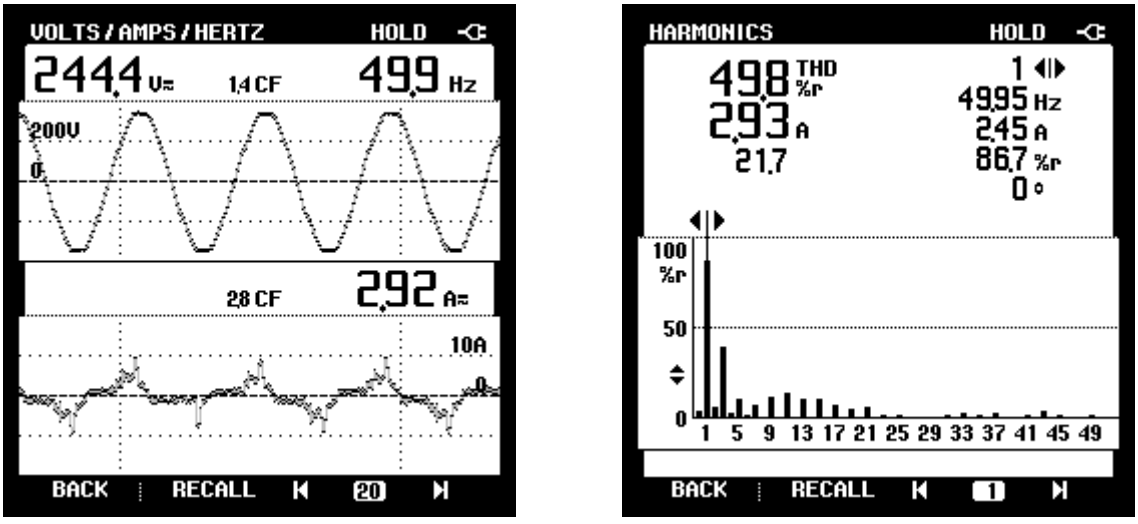


(a) (b)

Fig. 1.2: Mobile charger: (a) Voltage and current waveforms; (b) Harmonic spectrum of current

(B) Personal Computer

Personal computers are also injects the harmonics in the distribution system which is fed via 3P4W system as they use switch mode power supply (SMPS). The typical waveform of the current drawn by the personal computer of HP Desktop Elite 8300 Core i7 processor along with monitor is shown Figure 1.3. Its harmonic spectrum is also shown in which THD of the current is 49.8%. The harmonic spectrum shows that the third harmonic is quite dominant around 40%. The total current drawn by the CPU and monitor is less than 3A, but a typical high-rise building/computer centre can contain several hundred computers. This will show the effect on distribution system, which is not difficult to visualize.

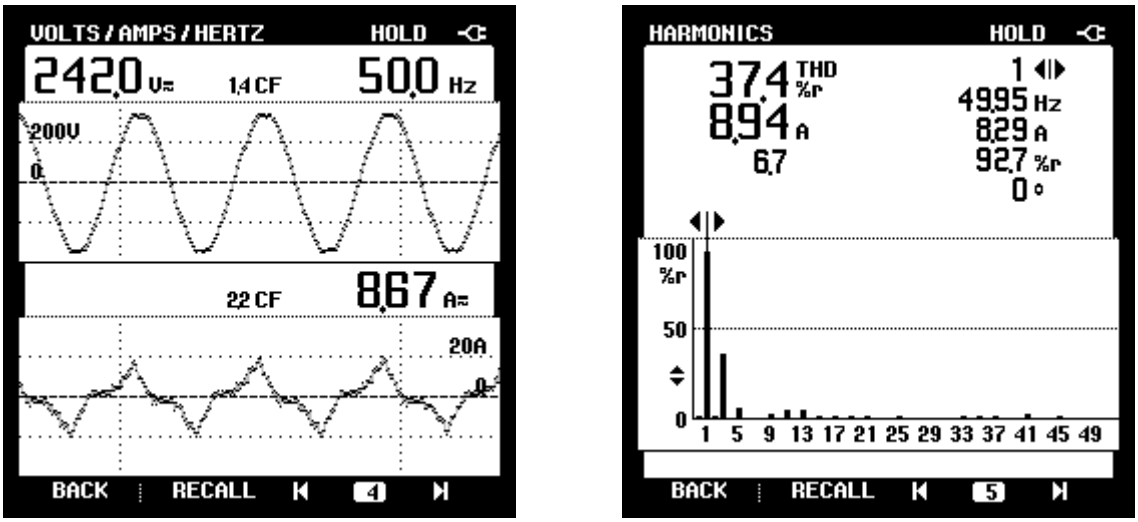


(a) (b)

Fig. 1.3: Personal computer: (a) Voltage and current waveforms; (b) Harmonic spectrum of current

Figure 1.4 shows the voltage and current waveforms along with the harmonic spectrum of input current drawn by the three personal computers fed from uninterruptable power

supply (UPS). UPS provides emergency electrical power to the load when the supply or mains power fails. To analyse the harmonic spectrum a small UPS made by Zebronics is used.

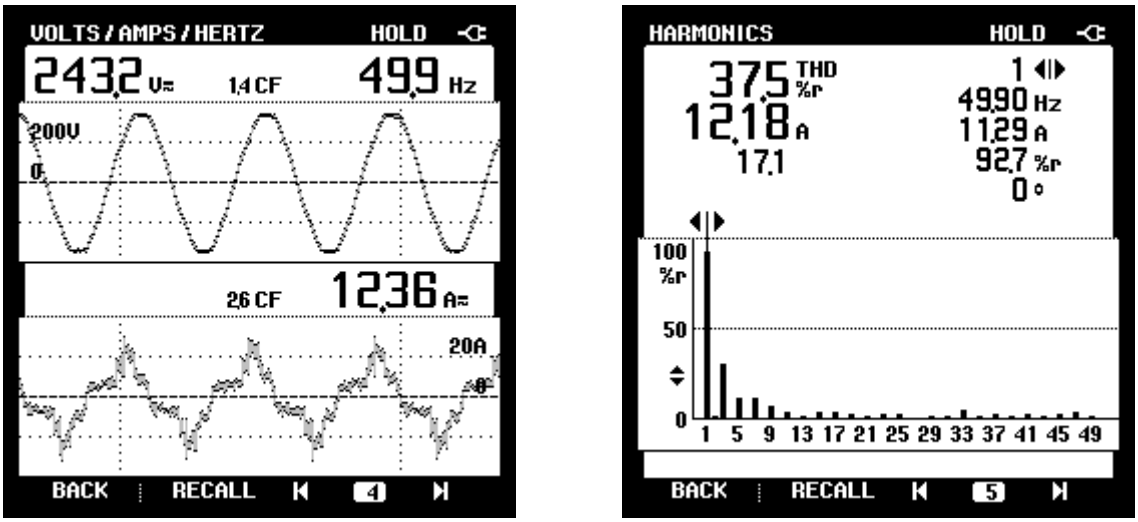


(a) (b)

Fig. 1.4: Uninterruptable power supply: (a) Voltage and current waveforms; (b) Harmonic spectrum of current

(C) Opal-RT Simulator

Similar to personal computers, Opal-RT and RT-Lab simulators are also injects the harmonics into the distribution system. The Opal RT is a real-time simulator which uses programmable power supply for internal mother board operations. The typical waveform voltage and current of the current drawn by the Opal-RT simulator along with personal computer is shown Figure 1.5. The harmonic spectrum of input current is also shown Figure. in which THD of the current is 37.5%. The harmonic spectrum shows that the 3rd, 5th, 7th harmonics are quite dominant.

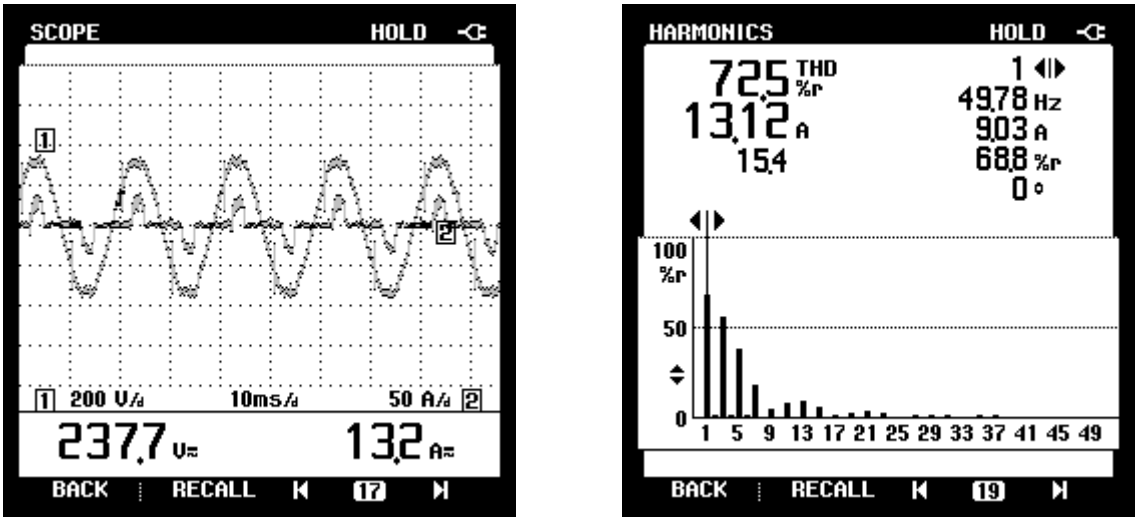


(a) (b)

Fig. 1.5: Opal-RT Simulator: (a) Voltage and current waveforms; (b) Harmonic spectrum of current

(D) Central UPS Supply of Computer Lab

Computer lab is located with many numbers of personal computer, air conditioner, table fan and lighting load. The supply to the all appliances is provided by the uninterruptable power supply (UPS). The profile of input voltage and current waveforms are analysed at the main UPS terminal of the computers lab of Electrical Engineering department. The current drawn by the UPS from the mains is highly distorted with harmonics with the composition of individual harmonic contribution by the various loads. Figure. 1.6 shows the harmonic spectrum of input current at UPS terminals, which is having THD of 72.5% with dominant harmonics of 3rd and 5th of magnitude 52% and 38.5% respectively. The power factor is 0.68 lagging with 2.36kVAR over 3.20kVA load.



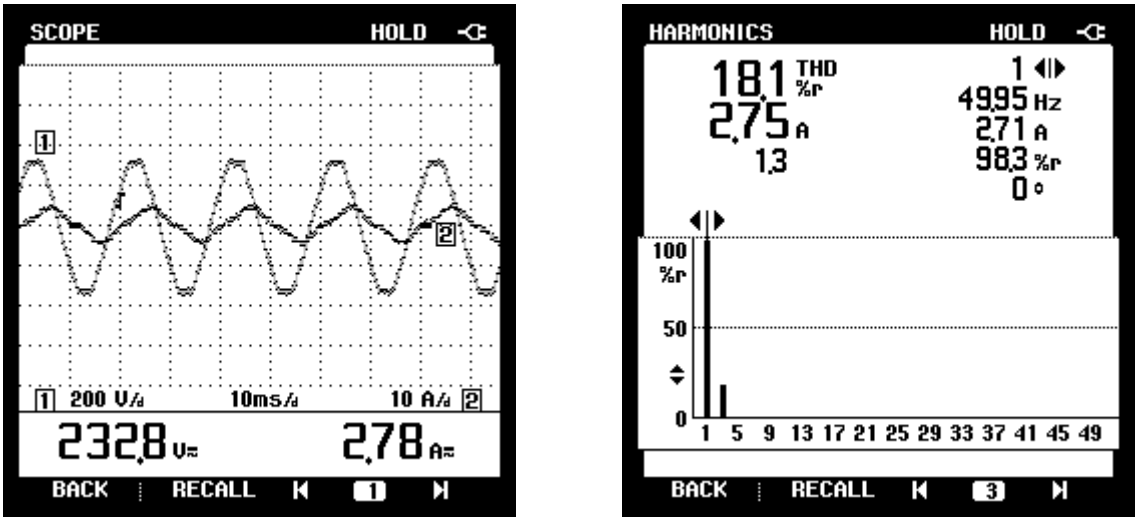
(a) (b)

Fig. 1.6: Central UPS system of computer lab: (a) Voltage and current waveforms; (b) Harmonic spectrum of current

(E) Fluorescent Lighting

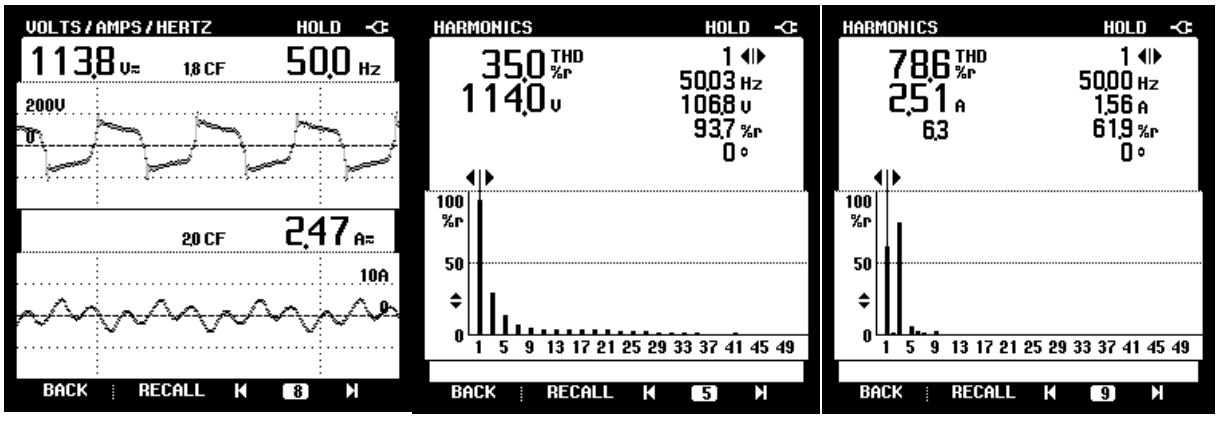
Lighting is considered one of the most important loads in the power system. Due to the advancement in power electronics technology nowadays, fluorescent lamps (FL) and compact fluorescent lamps (CFL) are becoming increasingly more attractive for many reasons. First, the efficiency of FL is four times the efficiency of incandescent lamps (IL) and lifetime of a typical CFL is thousand times that of an IL. The principle of operation of FL is based on magnetic ballast. High voltage up to 1000V is generated with the help of choke which is used to start the production of light. Although the power factor of tube light is as low as 0.6 because of using choke but the current waveform drawn by them is approximately sinusoidal as shown in Figure 1.7(a). Nowadays electronic ballasts are used to establish the high initial voltage across the lamp tube. Ballasts are also important for proper lamp ignition and to limit current once the arc is established. These electronic ballasts uses switch mode power supplies (SMPS), therefore, their current distortion could be increased. Figure 1.7

shows the voltage and current waveforms of single-phase FL connection with magnetic ballast, where the magnitude of current is amplified by 10x. The current drawn by the FL is having THD of 18.1% with the dominant 3rd harmonic component. The current is lagging the supply voltage because of the magnetic ballast present in the circuit such that the power factor becomes 0.62 lag. The harmonic spectrum and neutral current is also studied by using three-phase connection of FLs in 3P4W system. The voltage across the tube terminals and the neutral current is captured and shown in Figure. 1.8. It can be clearly observed that neutral current is having predominant 3rd harmonic component of 78.1%.



(a) (b)

Fig. 1.7: Single fluorescent lamp: (a) Voltage and current waveforms; (b) Harmonic spectrum of current

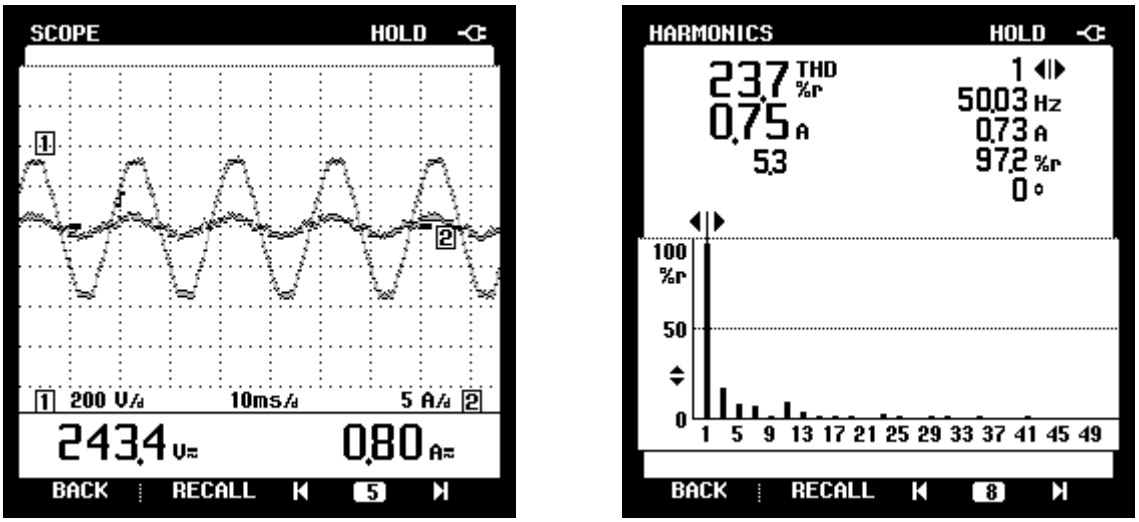


(a) (b) (c)

Fig. 1.8: Three-phase connection of fluorescent lamps: (a) Voltage across tube terminals and neutral current; (b) Harmonic spectrum of tube voltage; (c) Harmonic spectrum of neutral current

Nowadays, compact fluorescent lamp (CFL) is used to replace fluorescent lamp and some types fit into light fixtures designed for incandescent bulbs. The lamps use a tube which is curved or folded to fit into the space of an incandescent bulb, and a compact electronic ballast in the base of the lamp. The principle of operation remains the same as in

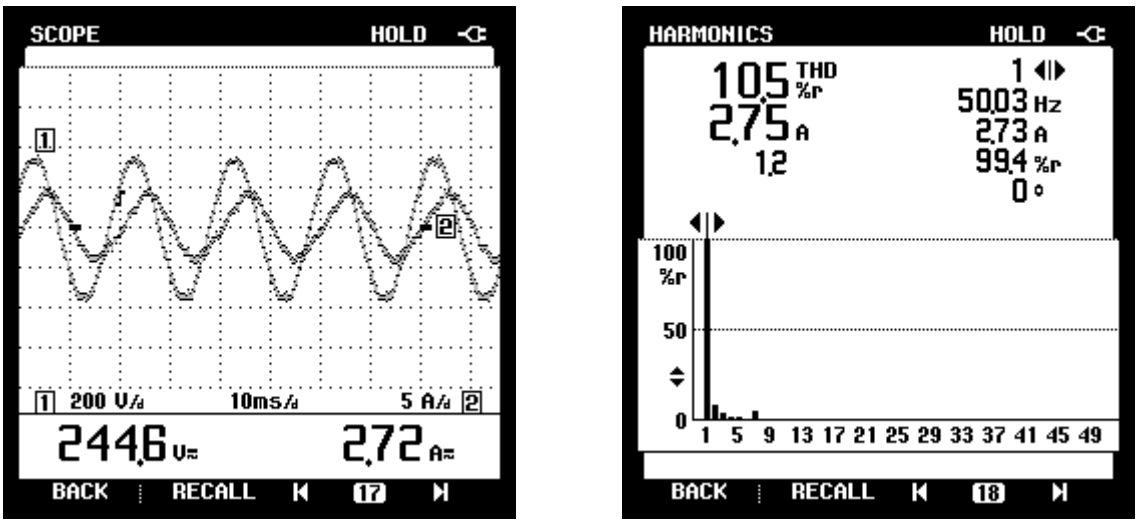
other fluorescent lighting. Because of the use of electronic ballast, CFLs are considered as non-linear loads with significant current waveform distortion and poor power factor. The studies shows that the power factor varies in the range of 0.4 to 0.8 lag [1]. To deal with poor power factor, CFL are manufactured with inclusion of power factor correction (PFC) circuits. However PFC circuit is only available in CFL with higher active power rating having not less than 25W. Figure 1.9. shows the input supply voltage and current waveforms and harmonic structure of input current. Compared to the FL, which is shown in Figure 1.7, CFL possess better power factor because of inclusion PFC circuits inside CFL, where as THD of CFL is more as compared to FL.



(a) (b)

Fig. 1.9: CFL: (a) Voltage and current waveforms; (b) Harmonic spectrum of current

(F) Water Cooler



(a) (b)

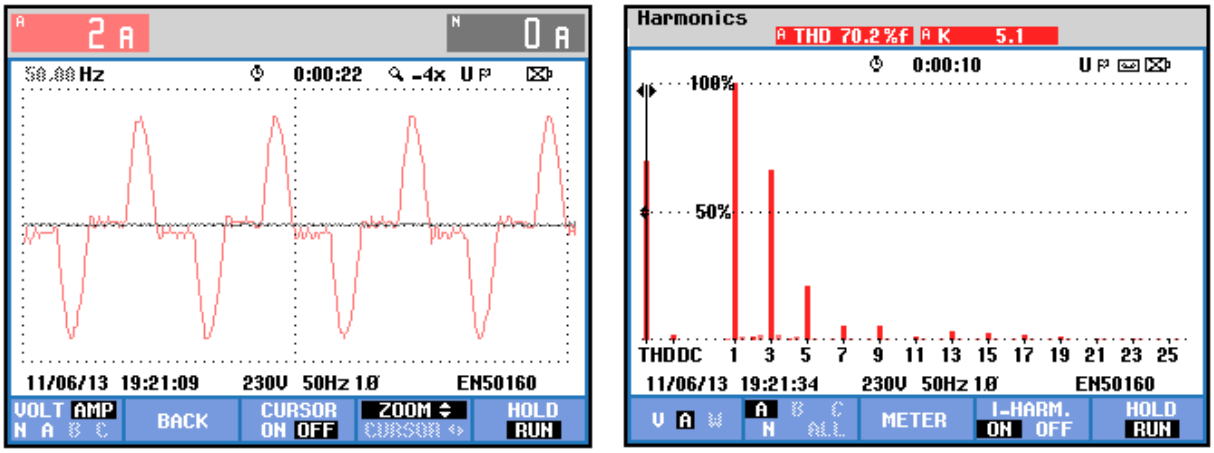
Fig. 1.10: Water cooler: (a) Voltage and current waveforms; (b) Harmonic spectrum of current

The wall-mounted type is connected to the building's water supply for a continuous supply of water and electricity to run a refrigeration unit to cool the incoming water. Wall-mounted water coolers are frequently used in commercial buildings like hospitals, schools,

businesses, and other facilities. The input voltage and current waveforms of water cooler are shown in Figure 1.10. The input source current distortion is 10.5% and draws significant amount of reactive power from the source because of the compressor. The power factor of the water cooler is 0.74 lagging.

(G) Air Conditioner

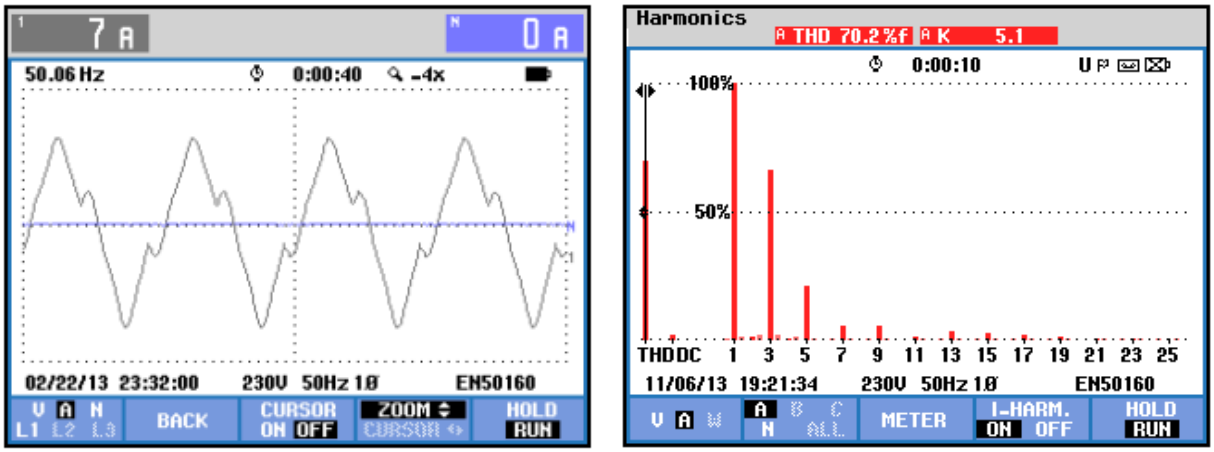
The air conditioners (Aircon) are used generally in the offices, institutions and in household for purpose of cooling, the ac is a most common type of non-linear load which (injects 3rd and 5th harmonics are more dominating, in which 3rd harmonic is around 70%) harmonics in the system. Here the waveform of current drawn by Aircon and its harmonic spectrum of this current is shown Figure 1.11.



(a) (b)

Fig. 1.11: Air conditioner: (a) Input current waveform; (b) Harmonic spectrum

(H) Microwave Oven



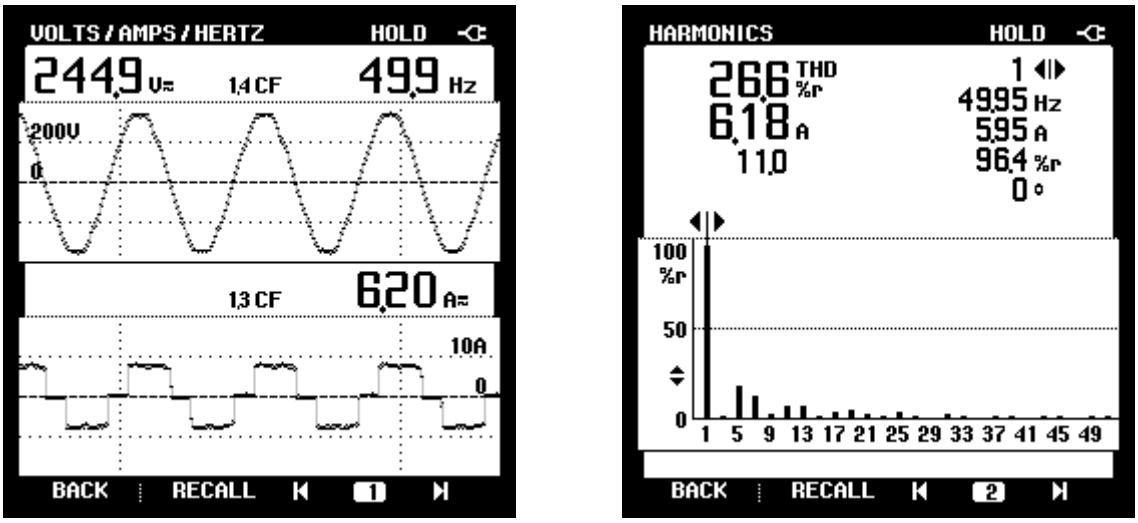
(a) (b)

Fig. 1.12: Microwave oven (a) Input current waveform; (b) Harmonic spectrum

Microwave oven is generally used for the cooking purposes in the households. This microwave oven consists of the transformer as well as voltage doublers circuit, which are used to excite the magnetron producing the microwave energy for cooking purpose. This process results in the high harmonic content from the supply. Figure 1.12 shows the input

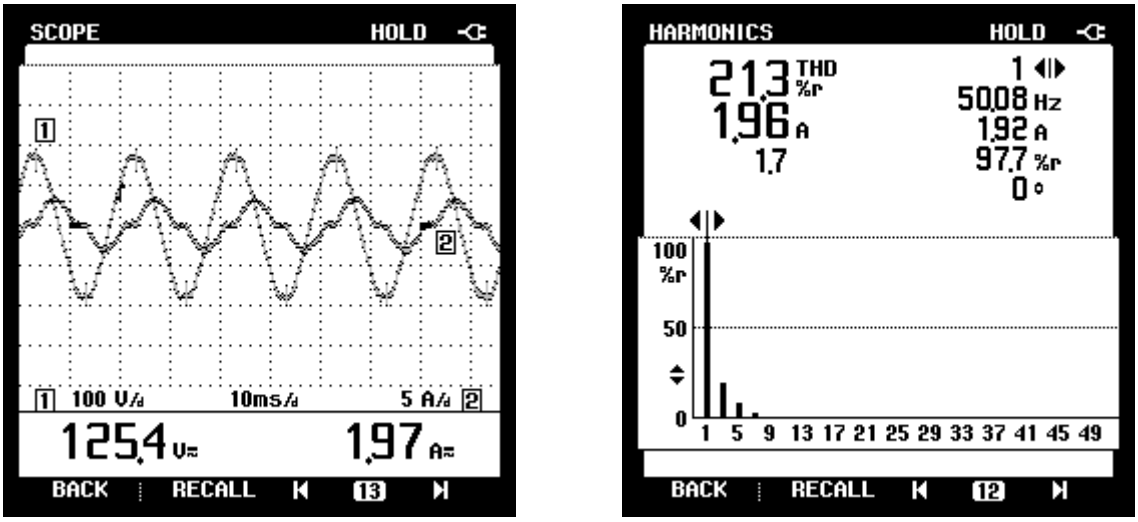
current waveform drawn by the 2100W Microwave, which causes to the source current harmonics with the distortion level of 70.2 % of THD.

(I) Common Power Electronic Circuits



(a) (b)

Fig. 1.13: Three-phase diode bridge rectifier with RL load: (a) Voltage and current waveforms of phase-*a*; (b) Harmonic spectrum of current



(a) (b)

Fig. 1.14: Single-phase voltage regulator with RL load: (a) Voltage and current waveforms of phase-*a*; (b) Harmonic spectrum of current

The AC-DC converter is an example of most commonly used non-linear load. They have a wide range of applications, from small rectifiers to large high voltage direct current (HVDC) transmission systems. Some of the applications such as computers, televisions, mobile phone chargers, kitchen appliances, industrial machinery, medical, military and telecommunications equipments, and other electronic consumer products. Figure 1.13(a) shows the typical phase-*a* current drawn by three-phase diode bridge rectifier fed to RL load. The corresponding harmonic spectrum of source current of phase-*a* shown in Figure 1.13(b).

From Figure 1.13(b), it is observed that the source current contains large amount of lower order harmonics with an observed THD of 26.6%.

The another example of non-linear load under consideration is AC-AC voltage controller, which can be widely used in various applications such as light dimming circuits for street lights, industrial and domestic heating, induction heating, transformer tap changing, speed control of winding machines, fans, etc. Figure 1.14(a) shows the voltage current waveforms of at input supply side of single-phase voltage controller fed to the RL load. The corresponding harmonic structure of input current is shown in Figure. 1.14(b). It can be observed that source current contains mostly the lower order harmonics of 3^{rd}, 5^{th} and 7^{th} with THD of 21.3%.

1.3 Solutions to Power Quality Problems

Various schemes for the mitigation of the power quality issues have evolved in the literature. The sub-section discusses about the solutions to the most common power quality problems such as harmonic distortion, poor power factor and voltage sag/swell.

1.3.1 Solutions to Harmonic Distortion

There are three basic ideas to handle harmonic distortions. They are:

- Providing an alternative path for the harmonic currents so as to minimize the amount of currents injecting into the system.
- Shifting the harmonics to other frequencies (usually at a higher spectrum) away from resonance/problematic region.
- Correcting or modifying the distorted current waveform such that it appears sinusoidal when viewed from the system side.

In view of the above, three techniques are commonly employed. They are:

- Phase multiplication
- Shunt passive filter
- Shunt and series active filters

(A) Phase Multiplication

Phase multiplication deals with the arrangement of converter loads such as PWM-type adjustable speed drives (ASD), DC drives, in a way such that some harmonics can cancel one another [84], [85]. For example, two 6-pulse drives can be phase-shifted from each other by 30^0, resulting in 12-pulse system. This eliminates the 5^{th}, 7^{th}, 17^{th}, 19^{th} harmonics. By connecting some drives through delta-wye transformers, and some through delta-delta transformer, the cancellation can be magnified. Figure 1.15 shows how a 12-pulse system, made up of two 6-pulse ASDs, with delta-wye transformer and delta-delta transformer, are connected. In this way, certain harmonics inherent in the currents drawn by the ASDs are cancelled, so that the harmonic distortion in the supply current is reduced.

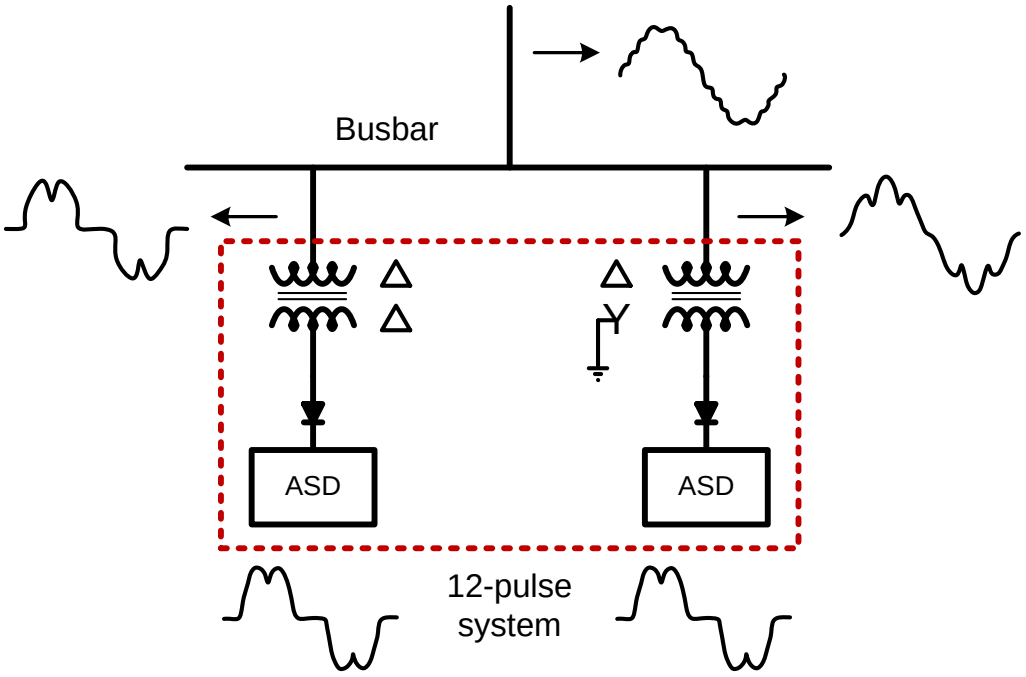


Fig. 1.15: Phase multiplication technique for harmonic compensation in the load [7].

(B) Shunt Passive Filters

The most traditional scheme involves the use of shunt passive filters to reduce the harmonic distortion in the current [7]. The passive filters consist of capacitors and inductors, which are connected in series. However there will be certain resistance inherent in the elements of the shunt passive filter.

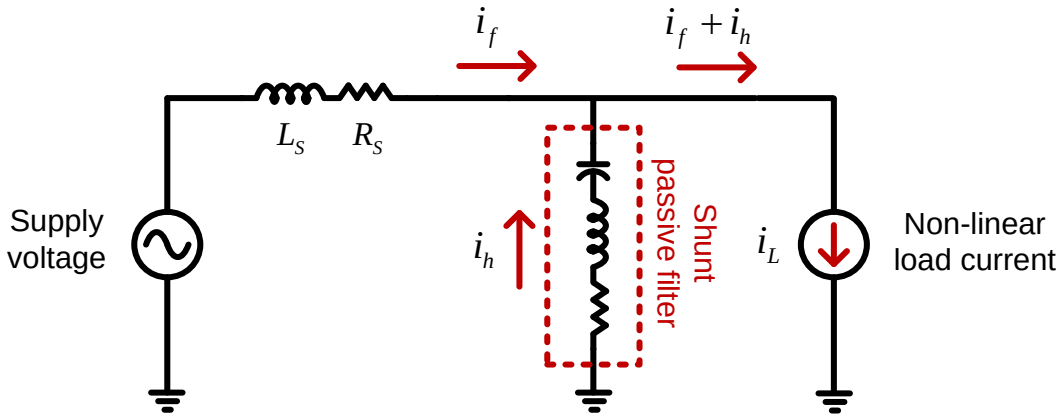


Fig. 1.16: Shunt passive filter installed in the network [7].

Figure 1.16 shows the typical installation site of shunt passive filter in the network. It prevents the load harmonic currents from injecting into the source, or other loads. This is achieved by tuning the resonant frequency (f_r) of the shunt passive filter to match the frequency of the harmonic component to be filtered away. In this way, the shunt passive filter will act as very low impedance at f_r shunting most of the harmonic component at this frequency. Thus, the elimination of multiple frequency requires separate passive filter for each harmonic frequency. In addition, the shunt passive filter is capacitive at low frequency,

e.g., the system frequency. Hence, it can also be used to supply the necessary reactive power demanded by the load. To design the shunt passive filter, the source impedance, R_s and L_s must be known. However, the source impedance is not constant and is dependent on the network configuration directly. This implies that the filtering characteristics are strongly influenced by the source impedance. Other limitations and complications of using shunt passive filters are highlighted in [7]. Although they are simple in operation, they have many limitations such as

- They are not suitable for changing the system condition as these are placed at a particular location in the system
- Each filter unit is sequenced to compensate certain harmonics in the system
- There is a problem with detuning when the operating conditions change
- Chances for occurrence of resonance between distribution transformer reactance and passive filter elements
- At light loads, when one of resonant frequencies between line inductance and shunt capacitors is close to the dominant harmonic frequencies, there will be a propagation of harmonic components throughout the distribution system [3].

(C) Shunt Active Filters

In order to overcome the problems with passive filters and to improve the PQ in the power distribution system, active power filters (APF) are proposed [4]–[7]. The concept of shunt active filter was introduced by L. Gyugyi and E. C. Strycula in 1976 [7]. Though, the basic principles of the active filtering were discussed in 1970's, the technology of those times was unable to support the real time implementation of the same. The rapid advancement of the power semiconductor devices like IGBTs and GTOs in the recent years has enabled the practical realization of these active power filters. Figure 1.17 depicts the operating principles of the shunt active filter.

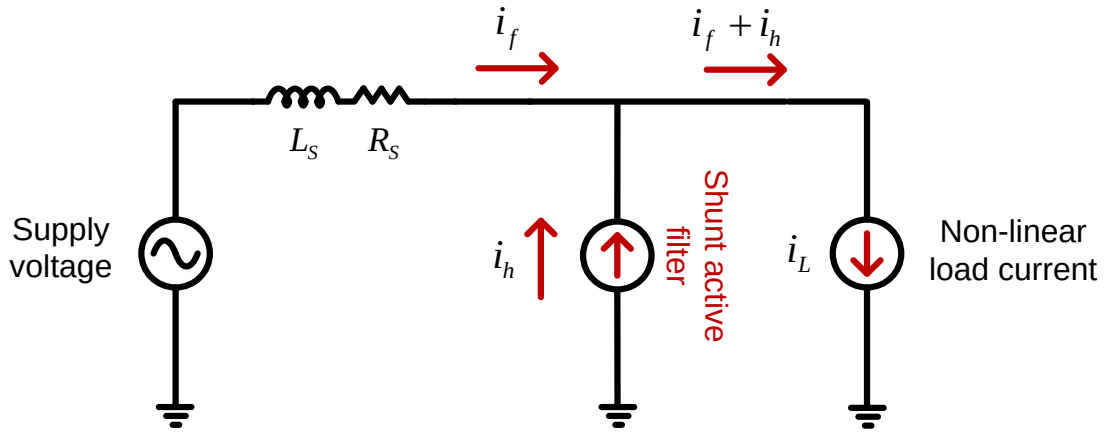


Fig. 1.17: Shunt active filter installed in the network [7].

Here, assume a non-linear load current is drawn from an undistorted supply voltage. Then, a reference based on the harmonic content i_h of the nonlinear load current i_l will be

formed online. Next, the shunt active filter, which is a DC-AC converter, will be tasked to deliver this reference (i.e. i_h) to the load side, so that the supply current consists of only the fundamental components (i_f) of i_l. In this way, the supply side will be undistorted.

As the reference to be delivered by the shunt active filter is formed online based on the load demand, we can see that it is adaptive to changes in the load demand. Thus, the shunt active filter is more superior in performance than the shunt passive filter, due to the fact that it is adaptive to changes in the load demand.

(D) Series Active Filters

A series active filter is a power electronics device that blocks the voltage harmonics in the supply voltage from the load [7]. This device operates as a dual circuit of the shunt active filter as a theoretical situation- the shunt filter to generate a harmonic current to compensate for harmonic distortions in the load current and the series filter to generate a harmonic voltage to compensate for harmonic distortions in the supply voltage. Figure 1.18 depicts the operating principles of the series active filter.

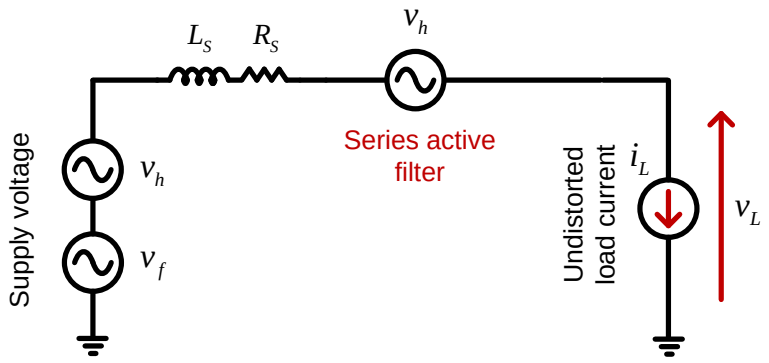


Fig. 1.18: Series active filter installed in the network [7].

Here, assume an undistorted sinusoidal load current is drawn from a distorted supply voltage. Then, a reference based on the harmonic content v_h of the distorted supply v_s will be formed online. Next, the series active filter, which is also a DC-AC converter, will be tasked to generate this reference (i.e. v_h) in series with the network, so that the load voltage consists of only the fundamental components v_f of v_s. In this way, the load voltage will be undistorted.

In reality, the series and shunt active filters are DC-AC converters with low-pass interfacing filters. Thus, it is obvious that the start-up cost of the shunt and series active filters will be more costly than that of the shunt passive filter. Furthermore, it may not be technically feasible to use a large-rating DC-AC converter as active filters with fast current response efficiently [91]. Nonetheless, the superior performance of the shunt and series active filters makes it more favourable than the use of shunt passive filter alone. Otherwise, the use of hybrid filters [101]–[104], that makes use of the advantages of the shunt passive and shunt or series active filters, is an alternative for harmonic compensation. When these active power

filters are employed in power distribution systems, they are referred as custom power devices (CPDs), which are discussed in the later sections.

1.3.2 Solutions to Poor Power Factor

The reactive power is usually very high for loads with poor power factor. Due to the fact that reactive power is not the real actual power used to perform work, it becomes very inefficient to transmit this high reactive power across the transmission line. This constitute to a very high current flow across the transmission line, which causes overloading, overheating and huge energy losses on the transmission lines, as well as the equipment. In addition, the power plants, transmission lines as well as the distribution equipment will have to be oversized to handle this huge capacity. In certain regions, industrial plants with poor power factors can be subjected to additional surcharges. This will mean bigger economical losses to them, which is why power factor is sometimes known as the energy efficiency index of an electric circuit [5]. Thus, if the power factor can be improved, the economical benefits that include lower utility charges due to lower power factor surcharges and lower kVA power demand charges can be enjoyed. It can also lead to the release of the system capacity, so that better utilization of the capacity can be achieved.

To handle loads with poor power factor, power factor correction devices can be installed. In principal, these devices generate and provide reactive power locally at load side so that the power factor at the supply side can be improved. Nowadays, the compensating devices that are available and used widely include:

- Static shunt capacitors
- Synchronous condensers

Often, they are chosen according to the rating requirement. For example, the rating ranges of the static shunt capacitors are from 15kVAr to 10MVAr, while the synchronous condensers are suitable to handle compensating requirement more than 10MVar. Other factors that include reliability, availability, loss management are also crucial in the installation of the devices.

1.3.3 Solutions to Voltage Sag/Swell

Primarily, voltage sag occurs when there is a sudden overloading or a short circuit. Hence, past effort to solve voltage sags usually involve disconnecting some of the loads installed in order to meet the current rating of the supply. Also, on-line/stand-by uninterruptible power supply (UPS) [9] can be installed to provide the additional power so that the supply voltage can be restored to its pre-sag level. However, the use of UPS can be expensive and lossy. In recent years, other ways of mitigating the effects of a sag are being investigated. Series Compensation (SC) voltage injection strategy is one way. In this strategy, energy is supplied by an energy storage device to restore the load voltage to its

pre-sag level. This is achieved by installing a custom power device i.e., the dynamic voltage restorer (DVR) [201], [202] in series with the load voltage to provide for the additional energy demanded by the load. In an event of a swell, the DVR may also be employed to absorb the additional energy in the network.

1.4 Literature Survey of Custom Power Devices

Custom power is formally defined as the concept of employing power electronic (static) controllers in 1kV through 38kV distribution systems for supplying a compatible level of power quality necessary for adequate performance of selected facilities and processes [8]. Custom power devices include power inverters, converters, injection transformers, master-control modules, static switches and energy-storage devices that have the ability to inject currents and voltages or both with in a power distribution system to provide high power quality. Typical custom power devices include distribution static compensator (DSTATCOM), dynamic voltage restorer (DVR), unified power quality conditioner (UPQC) [2]. In this section, a brief description of the important custom power devices are given.

1.4.1 Distribution Static Compensator (DSTATCOM)

The distribution static compensator (DSTATCOM) is typically a shunt connected custom power device [7], [200]. The structure of DSTATCOM is shown in the Figure 1.19. It alleviates the current related power quality problems in the distribution system. DSTATCOM injects current i_{sh} into the system at PCC, which helps in achieving harmonic filtering, power factor correction, neutral current compensation, and load balancing. The shunt injected current makes the source current (i_s) distortion free and balanced irrespective of the load current distortions. The required shunt injected current is realized using a voltage source inverter (VSI). The VSI injects currents at the PCC through the interfacing inductor L_{sh}. The operation of VSI is supported by the dc storage capacitor C_{dc} with dc-link voltage V_{dc} across it. The source with a voltage of v_s supports the linear and nonlinear load current i_l which could be non-sinusoidal, unbalanced and at a low power factor. The source and feeder impedance is represented by the inductor L_s and resistance R_s.

Many DSTATCOM topologies related to three-phase three-wire (3P3W) and three-phase four-wire (3P4W), isolated and non-isolated, and with and without transformers are reported in the literature. DSTATCOM in current control mode injects harmonic and reactive components of load current addressing power quality [5]. In voltage control mode, it regulates load voltage at a constant value protecting loads from voltage disturbances [187,188]. The performance of DSTATCOM depends on the control algorithm used for extraction of reference current components [189] such as instantaneous reactive power (IRP) theory, symmetrical component (SC) theory, synchronous reference frame (SRF) theory, average unit power factor (AUPF) theory, sliding mode control and Adaline based neural

network. [190,191]. The optimal location and sizing of the DSTATCOM which plays an important role in PQ improvement has been employed using firefly algorithm [192] and particle swarm optimization technique [193]. Potential applications of DSTATCOM such as reactive power compensation in single-phase operation of micro-grid [194], voltage support strategy in low voltage (LV) networks [195], a dynamic hybrid VAR compensator along with thyristor switched capacitor (TSC) in distribution system [196], system impact study [197], reduction of photovoltaic power fluctuations [198], enhancement of PV penetration in distribution system [199], and mitigation of voltage sag/swell/flicker [200] are reported in the literature.

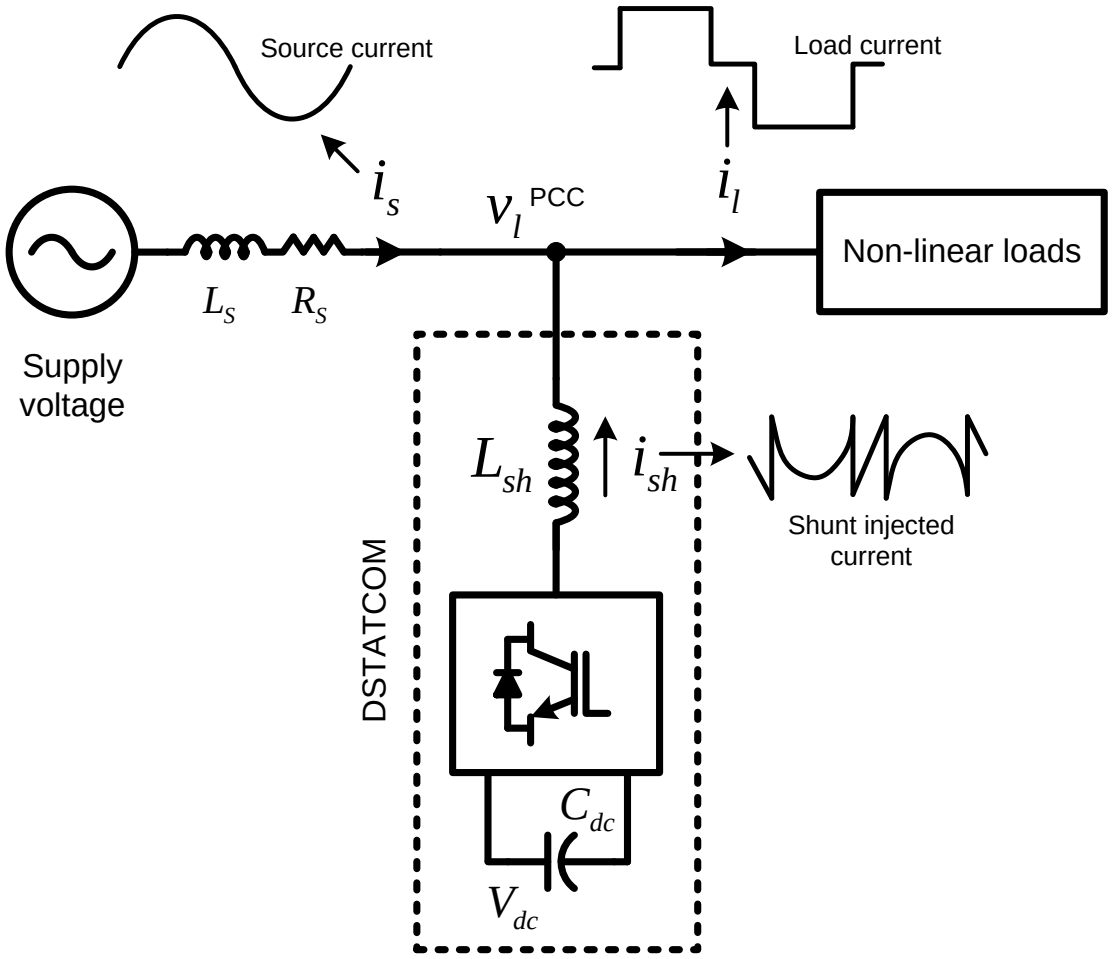


Fig. 1.19: System configuration of DSTATCOM.

1.4.2 Dynamic Voltage Regulator (DVR)

The series compensated custom power device is shown in Figure 1.20, which is referred as dynamic voltage restorer (DVR) [202]. A DVR is a power-electronic converter-based device that has been designed to protect critical loads from supply-side voltage disturbances. It is connected in series with a distribution feeder and is capable of generating or absorbing real and reactive power at its AC terminals [203]. The first DVR built by Westinghouse for EPRI was installed in August 1996 on the Duke Power Company (North

Carolina) 12.47kV system [7]. The main purpose of the DVR is to protect the sensitive loads from voltage sag/swell, interruptions and harmonics in the supply side voltage [2], [16]. It inserts required voltage magnitude and phase angle in series with the distribution feeder using the injection transformers and VSI supported by the dc storage capacitor and dc-link voltage. The series injected voltage v_{inj} makes the load voltage v_l distortion free and balanced with desired magnitude. The interfacing inductance and filter capacitor of the series active filter are represented by L_{se} and C_{se} respectively.

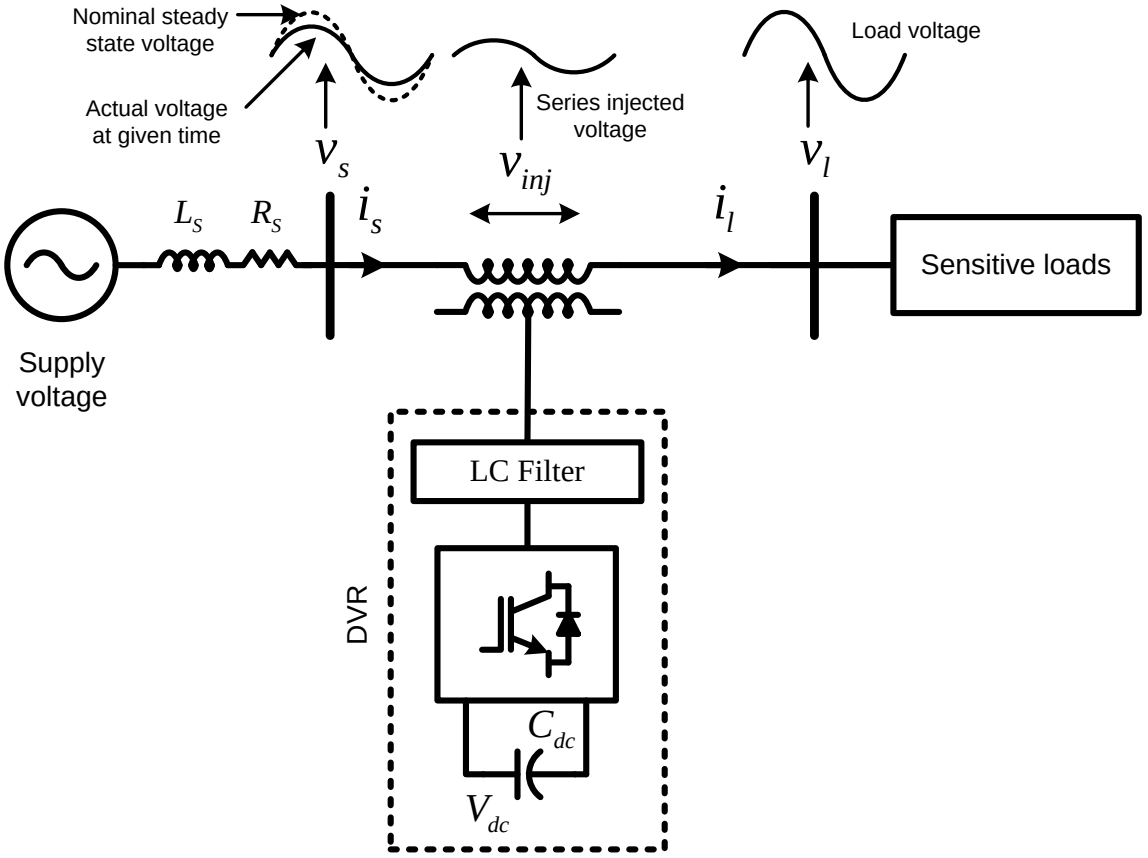


Fig. 1.20: System configuration of DVR.

The main function of a DVR is to compensate for voltage sags/swells. Beside the main function, additional functions such as selective voltage harmonics compensation [201], [202], flicker compensation [201], [204], [203], frequency compensation [205], and reactive power compensation [206] can also be integrated to the DVR design. When there is a fault at the downstream of the DVR installation point, the fault current will also be seen in the DVR and may cause its destruction. Therefore, the DVR should be protected against the downstream fault current [207]. This could be obtained by various bypass switches. However, another approach is to actively contribute to the DVR for fault current limiting. Fault current limiting capability of DVR is addressed in [201], [207]–[211]. When a fault occurs in downstream of the DVR, the DVR injects a negative voltage in series to the grid so that the fault is fed by a very low voltage. Therefore, the fault current is limited considerably. The DVR typically works when there is a voltage disturbance in the grid. In normal condition, DVR is not used and

remains in standby mode. In [213]–[216] DVR based on photovoltaic (PV) is presented. Application of DVR for low-voltage ride-through (LVRT) for distributed energy resources has been addressed in [217]–[223].

1.4.3 Unified Power Quality Conditioner (UPQC)

The thesis work is initiated with the project of feasibility analysis of unified power quality conditioner, popularly known as UPQC, for possible practical applications. The detailed study of UPQC related to the key concepts and operating principles of UPQC is discussed in this section. The reported literature on topology structures and control schemes is also briefly discussed.

UPQC is relatively the latest device in the family of the custom power devices [17]–[21]. UPQC is a versatile custom power device which consists of two inverters connected back-to-back with a common dc-link and deals with both load current and supply voltage imperfections. UPQC can do the work of both DSTATCOM and DVR, simultaneously. It can simultaneously fulfil different objectives like, maintaining a sinusoidal nominal voltage at the bus at which it is connected, maintaining voltage when there are voltage sags and swells in the system, eliminating harmonics in the source currents and load voltages, load balancing, compensating the reactive power, negative sequence current and power factor correction. The single line representation of the UPQC system configuration is shown in Figure 1.21.

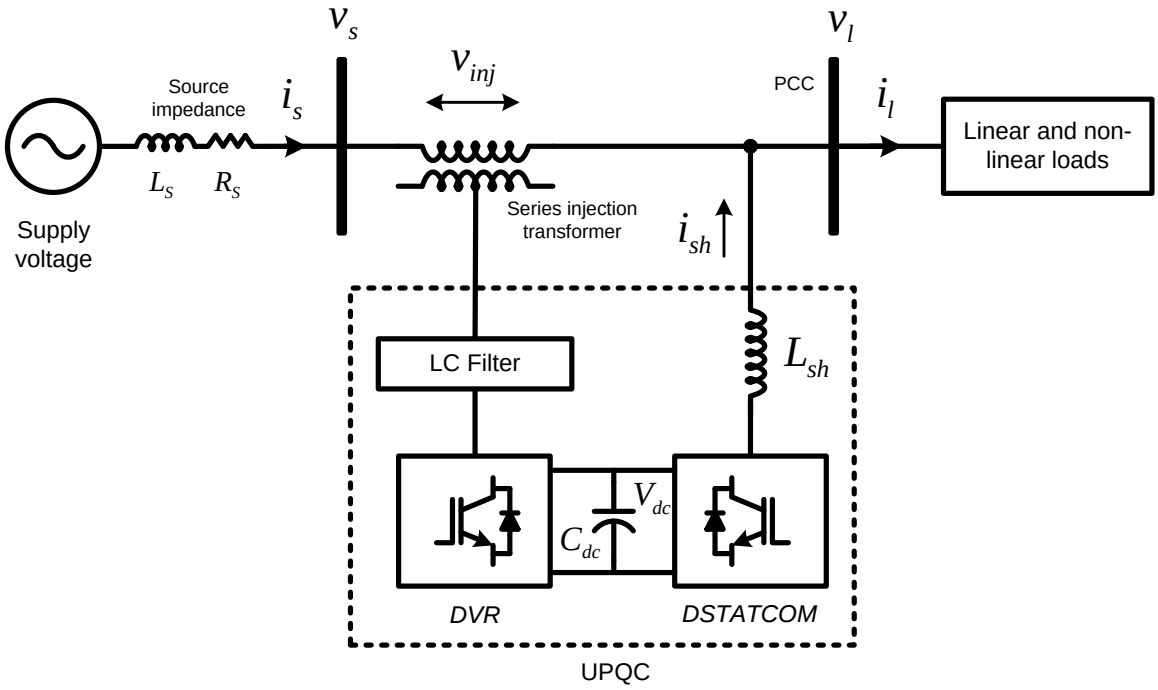


Fig. 1.21: System configuration of UPQC.

The key components of this system are as follows.

- Two inverters—one connected across the load which acts as a shunt APF and other connected in series with the line as that of series APF.

- Shunt coupling inductor L_{sh} is used to interface the shunt inverter to the network. It also helps in smoothing the current wave shape. Sometimes an isolation transformer is utilized to electrically isolate the inverter from the network.
- A common dc-link that can be formed by using a capacitor or an inductor. In Figure 1.21, the dc-link is realized using a capacitor, which interconnects the two inverters and maintains a constant self-supporting dc bus voltage across it.
- An LC filter that serves as a passive low-pass filter (LPF) and helps to eliminate high frequency switching ripples on generated inverter output voltage.
- Series injection transformer that is used to connect the series inverter in the network. A suitable turn ratio is often considered to reduce the current or voltage rating of the series inverter.

In principle, UPQC is an integration of shunt and series APFs with a common self-supporting dc bus. The shunt inverter in UPQC is controlled in current control mode such that it delivers a current, which is equal to the set value of the reference current as governed by the UPQC control algorithm. Additionally, the shunt inverter plays an important role in achieving required performance from a UPQC system by maintaining the dc bus voltage at a set reference value. In order to cancel the harmonics generated by a nonlinear load, the shunt inverter should inject a current as governed by following equation:

$$i_{sh} = i_s^* - i_l \tag{1.4}$$

where i_{sh}, i_s^*, and i_l represent the shunt inverter current, reference source current, and load current, respectively. Similarly, the series inverter of UPQC is controlled in voltage control mode such that it generates a voltage and injects in series with line to achieve a sinusoidal, free from distortion and at the desired magnitude voltage at the load terminal. The basic operation of a series inverter of UPQC can be represented by the following equation:

$$v_{inj} = v_l^* - v_s \tag{1.5}$$

where v_{inj}, v_l^*, and v_s represent the series inverter injected voltage, reference load voltage, and actual source voltage, respectively. In the case of a voltage sag condition, v_{inj} will represent the difference between the reference load voltage and reduced supply voltage, i.e., the injected voltage by the series inverter to maintain voltage at the load terminal at reference value. In all the reference papers on UPQC, the shunt inverter is operated as controlled current source and the series inverter as controlled voltage source except [112] in which the operation of series and shunt inverters is interchanged. In literature the topology with exchanging the functionalities of series and shunt converters is named as dual unified power quality conditioner (iUPQC) [165].

1.4.3.1 Classification of UPQC Topology

The UPQC is classified in two main groups as presented in Figure 1.22: 1) based on the physical structure and 2) on the voltage sag compensation approach used. Former type is considered as voltage sag compensation is one of the important functionalities of UPQC.

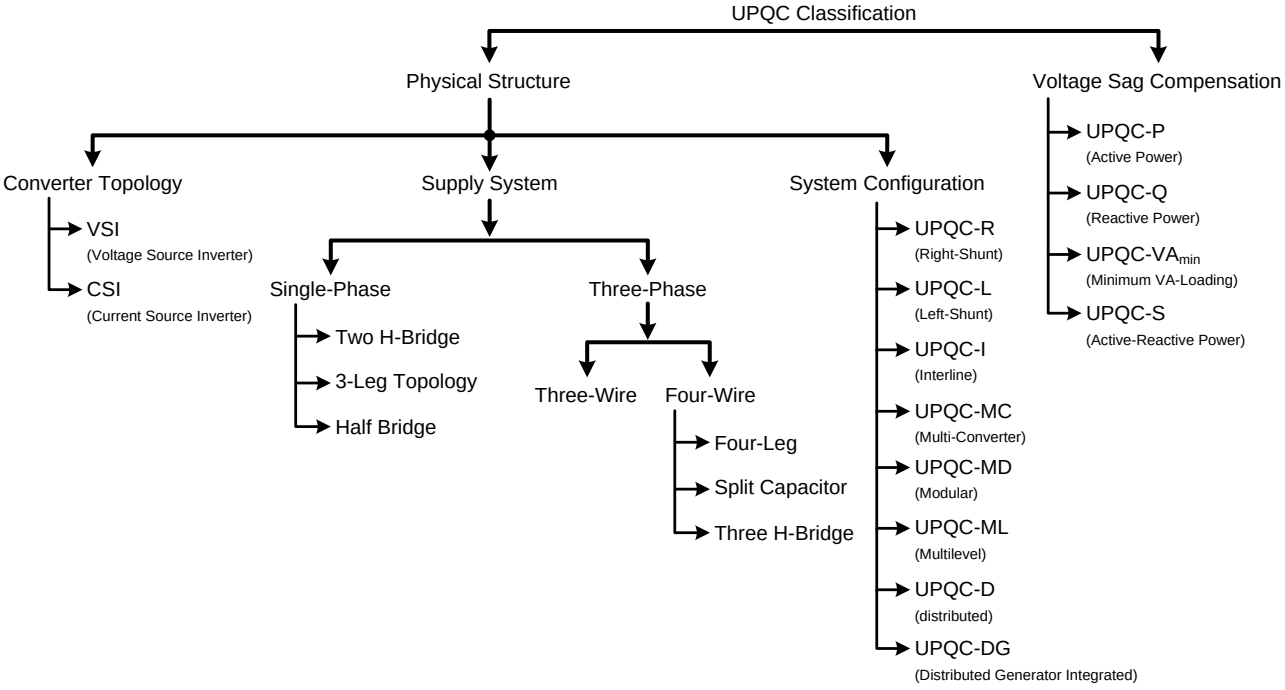


Fig. 1.22: Classification of UPQC topology [231].

A) Physical Structure:

The key parameters that attribute to these classifications are: 1) type of energy storage device used; 2) number of phases; and 3) physical location of shunt and series inverters.

1) Classification Based on the Converter Topology:

The UPQC may be developed using a pulse width modulated (PWM) current source inverter (CSI) [9]–[11], [115] that shares a common energy storage inductor L_{dc} to form the dc-link. The CSI-based UPQC topology is not popular because of higher losses, cost, and the fact that it cannot be used in multilevel configurations. The second topology, a most common and popular converter topology for UPQC, consists of PWM VSI that shares a common energy storage capacitor C_{dc}. The advantages offered by VSI topology over CSI include lighter in weight, no need of blocking diodes, cheaper, capability of multi-level operation, and flexible overall control.

2) Classification Based on the Supply System:

Depending upon the AC loads or equipments on the power system, UPQC can be broadly divided into single-phase and three-phase, supplied by single-phase (two-wire) or three-phase (three-wire or four-wire) source of power. single-phase two-wire (1P2W) supply system consisting of two H-bridge inverters (total eight semiconductor switches) [11]-[23],

[37]–[55]. The half bridge based UPQC system can be found in [57]–[83]. A 3P3W VSI-based UPQC is the most widely studied UPQC system configuration [12]–[15], [84]–[109], [151]–[161]. Apart from the three-phase loads, many industrial plants often consist of combined loads, such as, a variety of single-phase loads and three-phase loads, supplied by 3P4W source. The presence of fourth wire, the neutral conductor, causes an excessive neutral current flow and, thus, demands additional compensation requirement. To mitigate the neutral current in 3P4W system, various shunt inverter configurations have been attempted, namely, two split capacitor (2C) [114]–[118], [166], four-leg (4L) [51], [108], [122], [135] and three H-bridge (3HB) [21], [43], [49], [126]. The 2C topology consists of two split capacitors on the dc side. The midpoint of the capacitor, expected to be at zero potential, is used as connection point for the fourth wire. In 2C topology, it is important to maintain equal voltages across both the capacitors to avoid the flow of circulating current. This requires an additional control loop for dc bus capacitor voltage regulation in 2C topology. The 4L topology may offer better control over neutral current due to the dedicated fourth leg. The 3HB topology uses three units of single-phase H-bridge inverters connected to the same dc bus of the UPQC. In [49], the series inverter is configured as 3HB while the shunt inverter is realized as 2C to compensate the neutral current.

3) Classification Based on the UPQC Configuration:

This section gives an overview on the different UPQC configurations such as UPQC-D, UPQC-DG, UPQC-I, UPQC-L, UPQC-MC, UPQC-MD, UPQC-ML, UPQC-P, UPQC-Q, UPQC-R, UPQC-S, and UPQC-VA_{min}. The brief discussion on these topologies is presented as follows. Based on the placement of shunt inverter with respect to series inverter, the UPQC can be classified as right shunt UPQC (UPQC-R) and left shunt UPQC (UPQC-L). The shunt inverter can be located either on the right (UPQC-R) [99]–[127], [98], [128], [145], [152] side of the series inverter. Among two configurations, the UPQC-R is the most commonly used. The UPQC-L structure is used in special cases to avoid the interference between the shunt inverter and passive filters.

An interesting UPQC system configuration suggested by Jindal et al. is presented in [78], where the two inverters of the UPQC are connected between two distribution feeders named as interline UPQC (UPQC-I). One of the inverters is connected in series with one of the feeders while the other inverter in shunt with second feeder. With such a configuration, the simultaneous regulation of both the feeder voltages can be achieved. Furthermore, the UPQC-I can control and manage the flow of real power between the two feeders. This configuration, however, has certain limitations and can be used for special cases. Researchers have explored the possibilities for improving the system performance by considering additional third converter unit to support the dc bus can be named as multi-converter UPQC (UPQC-MC) [17], [19], [62], [66].

A modular UPQC configuration (named in this paper as UPQC-MD) introduced by Han et al. [147] is realized by using several H-bridge modules similar as connecting several single-phase UPQCs (eight semiconductor switches) in cascade in each phase. In [128] and [147], the H-bridge modules for shunt part of UPQC are connected in series through a multi-winding transformer, while the H-bridges in the series part are directly connected in series and inserted in the distribution line without a series injection transformer.

Rubilar et al. have realized a multilevel UPQC based on a three-level neutral point clamped (NPC) topology [88] and this configuration is addressed as UPQC-ML. Similar to UPQC-MD, the UPQC-ML can be considered as an alternative option to achieve higher power levels. Based on the requirements, the UPQC-ML can be realized in several levels such as 3-level, 5-level, 7-level and so on. A 3P4W distribution system is generally realized by providing a neutral conductor along with the three power lines from substation or by utilizing a delta–star transformer at the distribution level. A new topology for 3P4W UPQC-based distribution system is proposed in [108].

The UPQC can be integrated with one or several distributed generation (DG) systems such as solar and wind energy [39], [63], [86], [98], [152]. The system configuration, thus, achieved is referred as UPQC-DG. The output of DG system is connected to dc bus of the UPQC. The DG power can be regulated and managed through UPQC to supply to the loads connected to the PCC in addition to the voltage and current power quality problem compensation. Additionally, a battery can be connected to the dc bus, such that the excess DG generated power can be stored and used as backup. In the event of voltage interruption, the UPQC-DG system gives additional benefit by providing the power to the load (uninterruptible power supply operation). Furthermore, the DG power can be transferred in an interconnected mode (power to the gird and loads) or islanding mode (power to the specific loads) and so on.

B) Classification Based on the Voltage Sag Compensation Approach:

The voltage sag on a system is considered as one of the important power quality problems. A special attention on using UPQC can be noticed in the literature to mitigate voltage sag on a system. The existing literature suggests four major methods to compensate the voltage sag in UPQC-based applications i.e. UPQC-P, UPQC-Q, UPQC-VA_{min} and UPQC-S.

1) UPQC-P:

The active power is used to mitigate the voltage sag and hence the name UPQC-P (P for active/real power). In principle, to compensate the voltage sag, an in-phase voltage component is injected in the series with line through a series inverter [143]–[156]. This in-phase component is equal to reduced voltage magnitude from the desired load voltage

value. In order to achieve the effective sag compensation, the shunt inverter of UPQC draws the necessary active power required by the series inverter plus the losses associated with UPQC. Due to this, an increased source current magnitude during voltage sag compensation in UPQC-P method can be observed.

2) UPQC-Q:

The voltage sag can also be mitigated by injective reactive power through a series inverter of UPQC [157]–[159], [161], [167]. In such a case, it is called as UPQC-Q (Q for reactive power). The concept is to inject a quadrature voltage through the series inverter of UPQC such that the vector sum of source voltage and the injected voltage equals the required rated voltage at the load bus terminal. The shunt inverter of UPQC necessarily maintains a unity power factor operation at the source side. Therefore, by injecting the series inverter voltage in quadrature with the source voltage, the need of active power to compensate the sag on the system is eliminated. However, the resultant voltage, thus, achieved gives phase angle shift with respect to the source voltage. To compensate an equal percentage of sag, the UPQC-Q requires larger magnitude of series injection voltage than the UPQC-P. This increases the required rating of series inverter in UPQC-Q applications. Furthermore, the UPQC-Q cannot mitigate the swell on the system. Among the aforementioned discussed two approaches, the UPQC-P is the most commonly used method for voltage sag compensation in UPQC applications.

3) UPQC-VA_{min}:

Recently, there has been an attempt to minimize the UPQC VA loading during voltage sag compensation [160]–[167]. Instead of injecting the series voltage in quadrature or in-phase, in this method, it is injected at a certain optimal angle with respect to the source current. This method to compensate the voltage sag using UPQC is abbreviated as UPQC-VA_{min}. Beside the series voltage injection, the current drawn by the shunt inverter (to maintain dc bus and overall power balance) needs to be taken into account while determining the minimum VA loading of UPQC.

4) UPQC-S:

This approach is similar to UPQC-VA_{min}, where the series inverter delivers both active and reactive power. Unlike the UPQC-VA_{min}, in this method, the efforts are made to utilize the available series inverter VA loading to its maximum value. The series inverter of UPQC is controlled to perform simultaneous voltage sag/swell compensation and load reactive power sharing with the shunt inverter. Since, the series inverter of UPQC in this case delivers both active and reactive powers, it is given the name UPQC-S (S for complex power) [168]. The control of UPQC as UPQC-S involves several control loops and, thus, appears relatively complex to employ. However, it can easily be implemented when controlled digitally using a

DSP [168]. Lately discussed two approaches, UPQC-VA_{min} and UPQC-S, suggest the new era for research and development in the subject of power quality enhancement using UPQC where attempts are being made to use the series inverter of UPQC optimally.

1.4.3.2 Control Techniques of UPQC

The UPQC control strategy determines the reference signals (current and voltage) and, thus, decides the switching instants of inverter switches, such that the desired performance can be achieved. There are several control strategies/algorithm/techniques available in the existing literature those have successfully applied to UPQC systems. Frequency domain methods, such as, based on the fast Fourier transformer (FFT), are not popular due to large computation time and delay in calculating the FFT.

Control methods for UPQC in the time domain are based on instantaneous derivation of compensating commands in the form of either voltage or current signals. There are a large number of control methods in the time domain. Two most widely used time-domain control techniques for UPQC are the instantaneous active and reactive power or three-phase p-q theory [170] and synchronous reference frame method or three-phase d-q theory [171]. These methods transfer the voltage and current signals in ABC frame to stationary reference frame (p-q theory) or synchronously rotating frame (d-q theory) to separate the fundamental and harmonic quantities. In p-q theory, instantaneous active and reactive powers are computed, while, the d-q theory deals with the current independent of the supply voltage. The interesting feature of these theories is that the real and reactive powers associated with fundamental components (p-q theory), and the fundamental component in distorted voltage or current (d-q theory), are dc quantities. These quantities can easily be extracted using an LPF or a high-pass filter (HPF). Due to the dc signal extraction, filtering of signals in the α-β reference frame is insensitive to any phase shift errors introduced by LPF. However, the cut-off frequency of these LPF or HPF can affect the dynamic performance of the controller.

The UPQC controller based on three-phase p-q can be found in [14]–[27], [104]–[109], and [126], while d-q method based controller can be found in [33]–[47], [68], [111]–[121] and [167]. The original three-phase p-q theory exhibits limitations when the supply voltages are distorted and/or unbalanced. To overcome these limitations, the original p-q theory has been modified and generally referred as p-q-r theory. The UPQC controller based on this modified p-q-r theory can be found in [49], [70], [82], [116], [131], and [147]. Furthermore, both three-phase p-q and three-phase d-q theories have been modified such that the advantages offered by these methods are widen for single-phase APFs [172], [173] including single-phase UPQC systems [37], [94], [107], [108], [130].

A simple controller scheme for UPQC, called as unit vector template generation (UVTG), is given in [46]. The method uses a phase-locked loop (PLL) to generate unit vector

template(s) for single-/three-phase system. The experimental evaluation of UVTG-based single-phase system is given in [155].

One cycle control (OCC) of switching converters concept based controller is developed for the UPQC in [51] and [76]. The OCC controller generally uses an integrator with reset feature to force the controlled variables to meet the control goal in each switching cycle. The OCC has the advantages of fast response and high precision [51]. Authors in [94] suggest that during normal operating condition, the series inverter of UPQC is not utilized up to its true capacity. In order to maximize the series inverter utilization, a concept named as power angle control (PAC) of UPQC has been developed. The concept of PAC of UPQC proves that with proper control of power angle between the source and load voltages, the load reactive power demand can be shared by both shunt and series inverters without affecting the overall UPQC rating [94]. This indeed helps to reduce the overall rating of the shunt inverter of the UPQC.

A model predictive control (MPC) that takes into account system dynamics, control objectives, and constraints is proposed for UPQC by Zhang et al. [125]. The MPC can handle multivariable control problem and has relatively simple online computations. Li et al. [62] have suggested a H∞-based model matching control to track the inverter output waveforms for effective and robust control of UPQC. Furthermore, Kwan et al. [106] have given a model-based solution via H∞ loop shaping for UPQC. The UPQC is modeled as a multi-input multioutput system to deal with the coupling effect between the series and shunt inverters. Additionally, Kalman filter can be integrated to extract the harmonics in supply voltage/load current [59], [106], [125]. Kamran and Habetler [12] have put forward a technique based on deadbeat control in which the UPQC inverter combination is treated as a single unit [12], [22]. The overall system can be modelled as a single multi-input-multi-output system. This results in improved control performance over the separately controlled converters and/or reduced inter-converter energy storage. The system can have fast dynamic response and high steady-state accuracy.

A nonlinear control law based on linearization via exact feedback theory is described for UPQC in [151] and [141]. A sliding mode controller with a constant frequency scheme is utilized to control the series inverter of UPQC in [162]. Particle swarm optimization technique has also been utilized to develop the controller for UPQC [99], [129], [165]. Furthermore, an ANN technique can also handle the multi-input multioutput control system effectively. Thus, the ANN technique can be utilized to develop the controller for the UPQC to compensate different voltage and/or current related problems [34], [50], [65], [68], [69], [136]. A feedforward ANN scheme is reported by Banaei and Hosseini [68] to separate the harmonics contents in the nonlinear load. In [34] and [69], a Levenberg–Marquardt backpropagation ANN technique is used for UPQC. The time-domain and frequency-domain techniques have

certain drawbacks and limitations. To overcome their problems, a wavelet analysis technique, a tool for fault detection, localization, and classification of different power system transients, is proposed by certain researchers. By using multi-resolution analysis, the wavelet transform can represent a time-varying signal in terms of frequency component. Elnady et al. [24], Forghani et al. [77], and Karthikeyan et al. [133] have applied the wavelet transformation technique to control UPQC.

A symmetrical component theory is generally a choice in the UPQC applications to extract the fundamental positive sequence component when the system supply voltages are unbalanced [25], [31]–[33], [43], [72]. A special attention on compensating the problem of voltage flicker [14], [45], [46], [144], [155] and/or voltage unbalance [81], [117], [144], [166] can be noticed.

1.4.3.3 Concept of UPQC under Compensation

To understand the working concept of UPQC under different operating conditions like voltage sag/swell and reactive power compensation, the fundamental background is developed with active and reactive power flow between source, load and UPQC. This will help to develop the fundamental foundation to understand the compensating performance of the UPQC, which are presented in this thesis work.

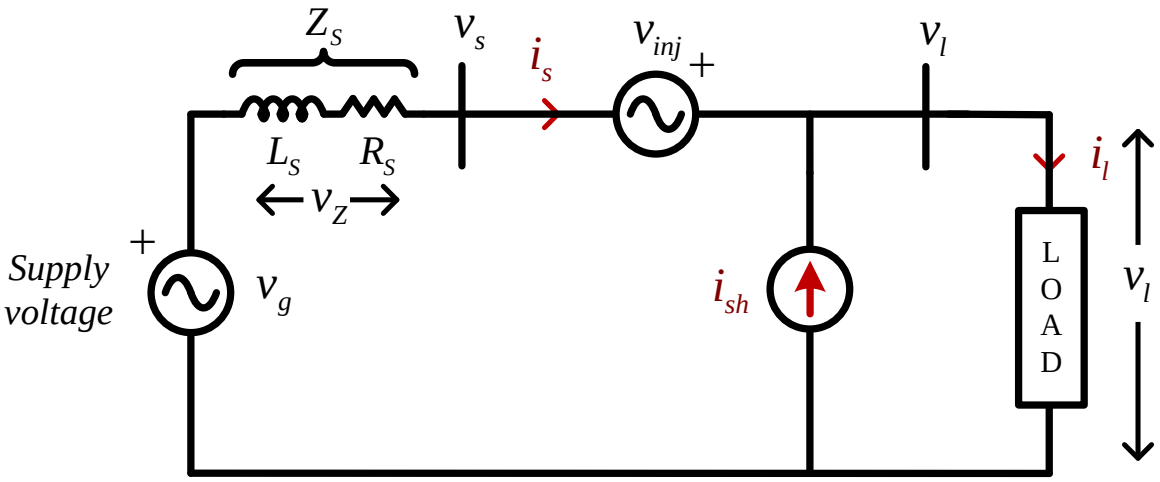


Fig. 1.23: Single-phase equivalent circuit of UPQC [143].

Figure 1.23 shows the equivalent circuit of UPQC. As the three phases of the topology structure are independent and also identical, it is possible to use an equivalent circuit of single-phase for modelling and analysis. The source voltage and source current are denoted by v_s, and i_s respectively. The load voltage and load current are represented by v_l, and i_l while, the voltage and current injected by UPQC are mentioned as v_{inj}, and i_{sh}. R_s and L_s denote the sum of the source and line resistance and inductance such that the resultant impedance can be represented as system impedance, Z_s. From the equivalent circuit, it can be observed that, the supply voltage (v_g) is represented as,

$$v_g = v_z + v_{inj} + v_l \tag{1.6}$$

Where, v_z– is the voltage drop across system impedance, v_{inj}– voltage injected by the series converter, v_l– load voltage at PCC.

The source terminal voltage, v_s is represented as,

$$v_s = v_g - v_z \tag{1.7}$$

If the supply voltage is considered as distorted and non-sinusoidal, then it may consists of fundamental and harmonic components, thus

$$v_g = v_f + v_h \tag{1.8}$$

Where, v_f and v_h are the fundamental and harmonic components of supply voltage respectively.

The load voltage at PCC can be derived as,

$$\begin{aligned} v_l &= v_g - v_z - v_{inj} \\ &= v_f + v_h - v_z - v_{inj} \end{aligned} \tag{1.9}$$

To compensate the distorted voltage at PCC, the series converter of UPQC injects voltage with equal and opposite phase to the supply harmonic component in series the line.

$$v_{inj} = v_h - v_z \tag{1.10}$$

On substituting (1.10) into (1.7), such that the load voltage at PCC will be maintained at fundamental component of supply voltage,

$$\begin{aligned} v_l &= v_f + v_h - v_z - (v_h - v_z) \\ &= v_f \end{aligned} \tag{1.11}$$

If the load is considered as the non-linear, the load current can be expressed as,

$$i_l = i_f + i_h \tag{1.12}$$

Where, i_f and i_h are the fundamental and harmonic components of load current respectively. In absence of UPQC, the source current (i_s) is same as that of load current (i_l), which is not sinusoidal because of the harmonic components.

From Figure 1.23, the shunt compensating current (i_{sh}) injected by the shunt converter of the UPQC can be given as,

$$i_{sh} = i_s - i_l \tag{1.13}$$

According to the operating principle of UPQC, the shunt converter has to inject the current in equal and opposite phase to load harmonic component.

$$i_{sh} = -i_h \tag{1.14}$$

Such that source current (i_s) can be maintained at pure sinusoidal as per (1.15)

$$\begin{aligned} i_s &= i_l + i_{sh} \\ &= (i_f + i_h) + (-i_h) \\ &= i_f \end{aligned} \tag{1.15}$$

The concept of UPQC under compensation can be explained in detail by considering the power flow analysis. This done by considering the following assumptions.

- The powers due to harmonics quantities are negligible as compared to the power at fundamental component, therefore, the harmonic power is neglected.
- Steady state operating analysis is done on the basis of fundamental frequency component only.
- No losses are associated with UPQC.

The UPQC is controlled in such a way that the voltage at load bus is always sinusoidal and at desired magnitude. Therefore, the voltage injected by series converter should be equivalent to a controlled voltage source whose magnitude is equal to the difference between the supply voltage and the ideal load voltage. The function of shunt converter is to maintain the dc-link voltage at constant level. In addition to this, the shunt converter also provides the VAR required by the load such that the input power factor will be unity. Therefore, only fundamental active power will be supplied by the source.

The voltage injected by series inverter can vary from 0° to 360°. Depending on the voltage injected by series inverter, there can be a phase angle difference between the load voltage and the source voltage. In the following analysis, the load voltage is assumed to be in-phase with source voltage irrespective to any variation in supply voltage. This is done by injecting the series voltage in-phase or out of phase w.r.t. the source voltage, during voltage sag and swell conditions, respectively. This suggests the possible real power flow through the UPQC. Depending on the relative magnitude of source voltage over the load voltage, voltage injected by series inverter could be positive or negative, absorbing or supplying the real power. Under these conditions, the series inverter does not handle any reactive power and the shunt inverter alone supplies the load reactive power.

Considering the load voltage, v_l, as a reference phasor and supposing the lagging power factor of the load $\cos\phi_l$, we can write

$$\vec{v}_l = V_l \angle 0^0 \tag{1.16}$$

$$\vec{i}_l = I_l \angle -\phi_l \tag{1.17}$$

$$\vec{v}_s = V_l(1 + k_f)\angle 0^0 \tag{1.18}$$

The small case letters for voltages, currents and powers denote the instantaneous values, while, the capital letters are used to represent the peak values. In (1.18) factor k_f is the ratio of magnitude fluctuation of source voltage, which can be defined as,

$$k_f = \frac{V_s - V_l}{V_l} \tag{1.19}$$

The voltage injected by series inverter should be equal to,

$$\vec{v}_{inj} = \vec{v}_s - \vec{v}_l = -k_f.V_l \angle 0^0 \tag{1.20}$$

The UPQC is assumed to be lossless and therefore, the active power demanded from the load (P_l) is equal to the active power input at PCC (P_s). The UPQC provides a unity power factor source current, therefore, for a given load condition the input active power can be expressed by the following equations,

$$P_s = P_l \tag{1.21}$$

$$V_s.I_s = V_l.I_l.\cos\phi_l \tag{1.22}$$

$$V_l(1+k_f).I_s = V_l.I_l.\cos\phi_l \tag{1.23}$$

$$I_s = \frac{I_l}{1+k_f}.\cos\phi_l \tag{1.24}$$

The above equation suggests that the source current I_s is indirectly proportional to factor k_f, since, ϕ_l and I_l are load characteristics and are constant for a particular type of load. The active (P_{se}) and reactive power (Q_{se}) handled by the series inverter can be expressed as follow:

$$P_{se} = V_{inj}.I_s.\cos\phi_s \tag{1.25}$$

$$P_{se} = -k_f.V_l.I_s.\cos\phi_s \tag{1.26}$$

$$Q_{se} = V_{inj}.I_s.\sin\phi_s \tag{1.27}$$

$\phi_s = 0$, since UPQC is maintaining unity power factor.

$$P_{se} = V_{inj}.I_s = -k_f.V_l.I_s \tag{1.28}$$

$$Q_{se} \cong 0 \tag{1.29}$$

The current provided by the shunt inverter (i_{sh}) is the difference between the input source current (after compensation) and the load current, which includes the load harmonics current and the reactive current.

Therefore, we can write:

$$\vec{i}_{sh} = \vec{i}_s - \vec{i}_l \tag{1.30}$$

$$\vec{i}_{sh} = I_s \angle 0^0 - I_l \angle -\phi_l \tag{1.31}$$

$$\vec{i}_{sh} = I_s - (I_l.\cos\phi_l - jI_l.\sin\phi_l) \tag{1.32}$$

$$\vec{i}_{sh} = (I_s - I_l.\cos\phi_l) + jI_l.\sin\phi_l = I_{sh} \angle \phi_{sh} \tag{1.33}$$

ϕ_{sh} represents the phase angle of shunt current injected w.r.t. the source voltage. The active (P_{sh}) and reactive power (Q_{sh}) handled by the shunt inverter can be expressed as follow:

$$P_{sh} = V_l.I_{sh}.\cos\phi_{sh} = V_l.(I_s - I_l.\cos\phi_l) \tag{1.34}$$

$$Q_{sh} = V_l.I_{sh}.\sin\phi_{sh} = V_l.I_l.\sin\phi_l \tag{1.35}$$

Based on above analytical study the different possible modes of active and reactive power flow between source, load and UPQC are discussed in following subsections.

A) Case-I: Active-Reactive Power Flow during Normal Working Condition:

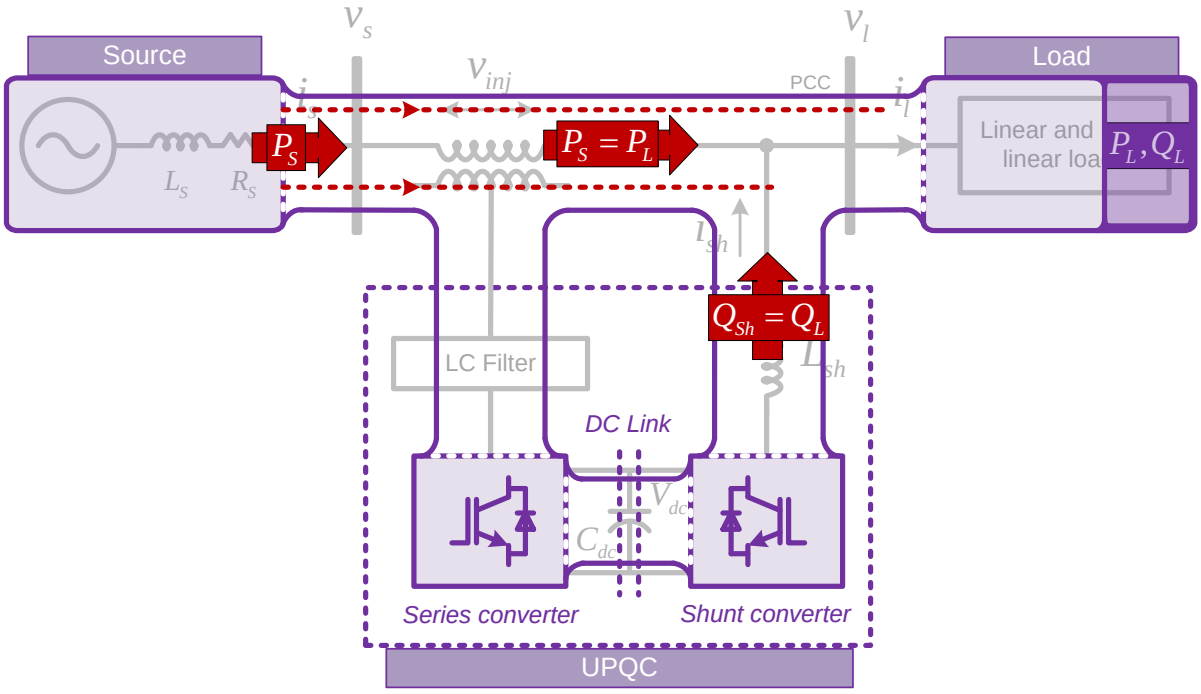


Fig. 1.24: Power flow during normal working condition of UPQC.

Under the normal working condition ($V_s = V_l$), without the voltage sag or swell, the factor k_f from (1.19) will be zero. UPQC does not exchange any active power through UPQC. In this condition, if the UPQC is not connected in the circuit, the reactive power required by the load (Q_l) is completely supplied by the source (Q_s). When the UPQC is connected to the network with the shunt inverter in operation, the shunt inverter alone now provides the reactive power required by the load (Q_{sh}).

Thus, the reactive power burden on the source is handled by shunt inverter ($Q_s = 0$). Therefore, as long as the shunt inverter is ON, it is responsible to supply the load reactive power irrespective to supply voltage distortion and variations. In this case, the series inverter is not taking any active part in supplying the load reactive power. The active and reactive power flow during the normal working condition is shown in Figure 1.24.

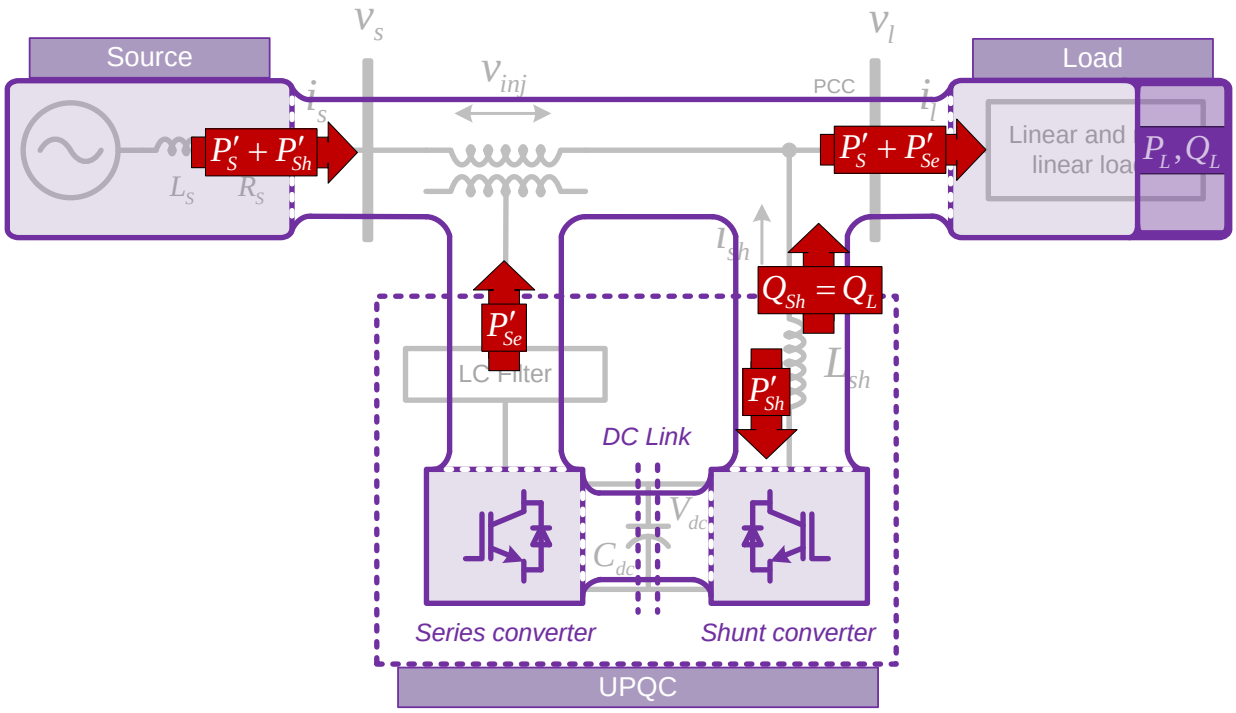


Fig. 1.25: Power flow analysis during sag compensation.

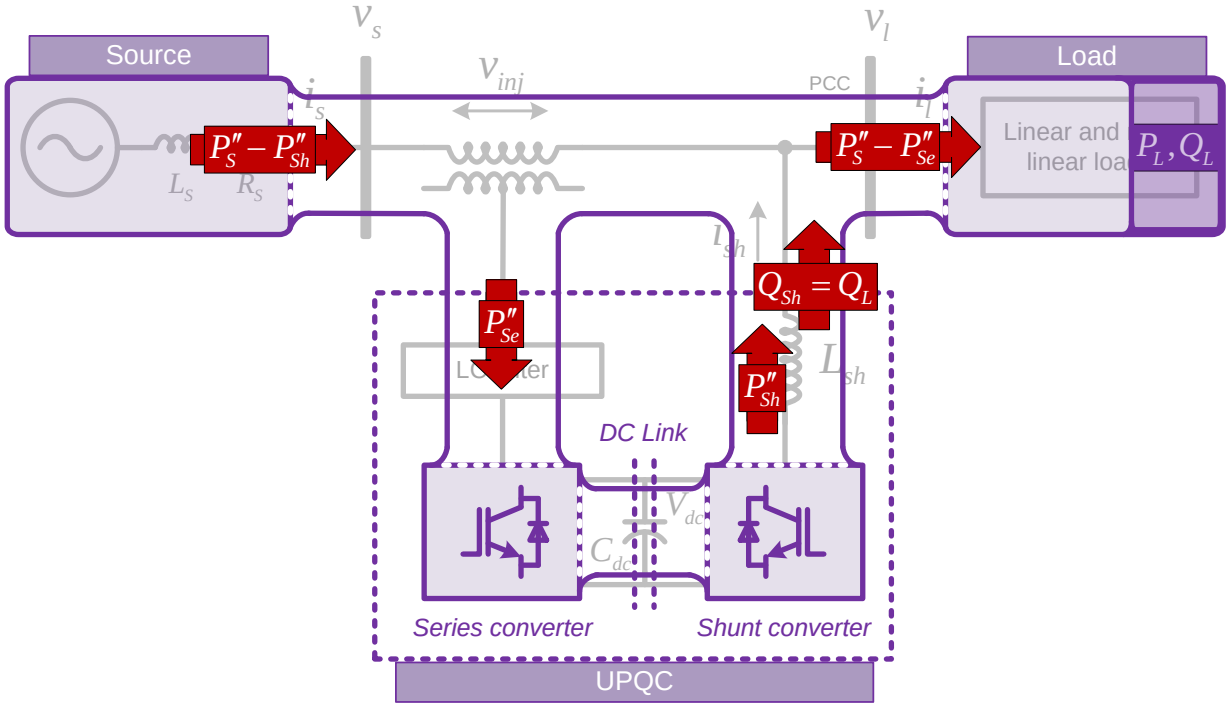


Fig. 1.26: Power analysis during swell compensation.

B) Case-II: Active-Reactive Power Flow during Voltage Sag Condition:

If $k_f < 0$, i.e. $v_s < v_l$, then according (1.19) and (1.28), P_{se} will be positive. It means series inverter supplies the active power to the load. This condition is possible during the utility voltage sag. From (1.24), I_s will be more than the normal rated current. Thus, we can say that the required active power is taken from the utility itself by taking more current to maintain the power balance in the network and to keep the dc-link voltage at desired level. This active power flows from the source to shunt inverter, from the shunt inverter to series inverter via the dc-link, and finally from the series inverter to the load. Thus, the load would get the required rated power even during voltage sag condition. Therefore, in such cases the active power absorbed by the shunt inverter from the source is equal to the active power supplied by the series inverter to the load. As mentioned in Case-I, the load reactive demand is supported by the shunt inverter in addition to the active exchange. The overall active and reactive power flow with the mode of voltage sag compensation is shown in Figure 1.25.

C) Case-III: Active-Reactive Power Flow during Voltage Swell Condition:

If $k_f > 0$, i.e. $v_s > v_l$, then from (1.19) and (1.28), P_{se} will be negative. This means that the series inverter is absorbing the extra real power from the source. This is possible during the voltage swell condition. From (1.24), I_s will be less than the normal rated current. In other words, the UPQC feeds back the extra power to the supply system. The overall active and reactive power flow during voltage swell compensation is shown in Figure 1.26.

D) Case-IV: Active-Reactive Power Flow under Distorted Voltages:

If the voltage at PCC is distorted containing several harmonics, in such cases, the series inverter injects voltage equal to the sum of the harmonics voltage but in opposite direction. Thus, the sum of voltage injected by series inverter and distorted voltage at PCC will get cancelled out. During this voltage harmonic compensation mode of operation the series inverter does not consume any active power from the sources. This is due to the fact that the harmonics quantities contribute to the reactive power.

E) Case-V: Active-Reactive Power Flow under Distorted Load Currents:

If the load is a non-linear producing harmonics, in such cases the shunt inverter injects current equals to the sum of harmonics current but in opposite direction, and thus canceling out current harmonics generated by non-linear load. During this current harmonics compensation mode of operation the shunt inverter does not consume real power from the source since it injects only harmonics current.

1.5 Scope of Work and Author's Contribution

Although the term "power quality" encompasses all disturbances encountered in a power system, it has been found that reactive power burden, harmonic currents, voltage sag,

distorted voltage and unbalanced operation are the most dominant types of power quality problems in modern distribution systems. This thesis exploits this fact and evaluating the solutions based on custom power devices for improving the power quality of the distribution systems. In this thesis, an attempt has been made for improving power quality in 3P3W and 3P4W systems with UPQC.

The main contributions of the author can be summarized as follows:

- A literature survey on available inverter topologies and control strategies for the realisation of UPQC are studied. Based on this study, two-level inverter and three-level inverter based UPQC are selected as the power circuit for the UPQC.
- The comparative performance analysis is carried out between both topologies by applying same control technique for various voltage and current distortion problems. Further, experimental studies have also been carried out to investigate the performance of the both topologies.
- A simplified predictive control is proposed for both the topologies of UPQC-2L and UPQC-3L to address the simple control scheme, as compared to the complicated model predictive control methods. The Extensive simulation have been used for compensating various voltage distortions with nonlinear load currents are conducted to examine the effectiveness of the UPQC with two-level and three-level structures.
- An hybrid UPQC is introduced with the addition of multi functioning capability to the coupling inductor of the shunt converter to reduce the rating of the overall system. A passive power filter (PPF) is added in the place of coupling inductor, such that the reactive burden on shunt converter is reduced by selecting the lower dc-link voltage. In order to further reduce the dc-link voltage, a phase angle control approach is implemented. A suitable algorithm is proposed to wisely select the optimal dc-link voltage to minimize the VA loading of UPQC.
- An alternate solution is proposed to address the fixed compensation by the PPF adopted for UPQC, with the inclusion of thyristor controlled reactor (TCR) to the PPF branch. The dc-link voltage is analyzed with variable compensation provided by the thyristor controlled impedance based PPF (TCZ-PPF). The simulation study is carried out to evaluate the effectiveness of the hybrid UPQC for voltage sag compensation with loading reactive power compensation for within compensation range and also above the range offered by TCZ-PPF is analyzed.
- A new topology is proposed to reduce the size and cost of the UPQC by removing the major component i.e. series injection transformer. Series converter is directly connected to the secondary bottom terminals of the distribution transformer. The advantages and challenges of this proposed topology are explored. The topology is employed for 3P4W systems to verify the effectiveness of the transformerless series

injection based UPQC (TLSI-UPQC). A control strategy is proposed for TLSI-UPQC to handle the neutral point for the distribution transformer and also to connect single-phase loads on PCC.

1.6 Organization of the Thesis

Apart from this chapter, the thesis contains six more chapters and the work included in each chapter is briefly outlined as follows:

CHAPTER 2 describes the comparative performance analysis of unified power quality conditioner related to two-level and three-level inverter structures. It will start with the topology description and control strategy used for the evaluating the performance of both the topologies. The MATLAB simulations are carried out for various voltage distortions along with the nonlinear load. The simulation results are validated with the experimental setup developed in the laboratory.

CHAPTER 3 describes the application of model predictive control approach to unified power quality conditioner. The advantages of model predictive control over exiting control strategies are discussed and then a new approach is proposed to simplify the model predictive control. To verify the effectiveness of the proposed control scheme, it is applied for UPQC with two-level and three-level inverter structures. Next, the comparative performance analysis is presented for both topology structures. The validation of simulations are carried out with experimental work.

CHAPTER 4 describes the hybrid structures incorporating passive power filters in conjunction with custom power devices (CPD) are capable of effectively decreasing the burden of VA loading as well as power semiconductor switch rating. This chapter proposes an analytical method to effectively control the dc-link voltage of Hybrid Unified Power Quality Conditioners (H-UPQC). Phase angle control (PAC) is integrated to H-UPQC to enable sharing of the reactive power burden between both shunt and series filter thereby decreasing the DC-link voltage requirement. Thus, the average switching losses and voltage stress of the semiconductor switches are significantly reduced. A detailed comparison between conventional UPQC and Hybrid UPQC is performed to analyse the DC- link voltage and the VA loading of both the structures.

CHAPTER 5 extends the control of dc-link voltage to minimize further as compared to PPF based UPQC. The PPF provides the fixed reactance to compensate load reactive power. Adopting thyristor controlled reactor (TCR) to PPF, makes the reactance offered by PPF can be controlled over wide range. This concept is adopted for UPQC and named as thyristor controlled shunt reactance PPF (TCZ) based UPQC (TCZ-PPF-UPQC) to analyse the variation in dc-link voltage requirement. The dc-link voltage is also evaluated by applying PAC control approach. The performance is analysed through MATALB Simulink and also validated by the experimental laboratory setup.

CHAPTER 6 describes the structure of the transformer-less series injection (TLSI) based UPQC topology is analysed and compared to a conventional 3P4W UPQC topology. The advantages and challenges of the considered topology are highlighted. The solutions to these challenges are also discussed and a control strategy is proposed and discussed in detail to achieve the desired performance from the TLSI-UPQC topology explained. The Simulink model is developed in the MATLAB/Simulink. The performance is evaluated through simulation study and validated with the laboratory experimental results.

The main conclusions of the presented work and possible future research have been summarized in this CHAPTER 7.

In the end of thesis, the list of references and appendices regarding software and hardware implementations are provided.

CHAPTER 2: PERFORMANCE ANALYSIS OF UNIFIED POWER QUALITY CONDITIONER

This chapter describes the comparative performance analysis of unified power quality conditioner related to two-level and three-level inverter structures. It will start with the topology description and control strategy used for the evaluating the performance of both the topologies. The MATLAB simulations are carried out for various voltage distortions along with the nonlinear load. The simulation results are validated with the experimental setup developed in the laboratory.

2.1 Introduction

In Chapter 1, the structure and the operating principle of the UPQC have been discussed. It also provided the detailed literature survey of the various topologies and control strategies for generation of reference quantities. UPQC are smart devices which improved the service reliability by compensating power quality disturbances like current harmonics, voltage sag/swell in order to protect the process loads. Aside their enormous advantages, these devices fail to guarantee the local distributors differ quality demand levels as it improves the power quality for all supplied the end users making the installation cost quite high to the quality of power obtained [7]. The topology structure with two-level inverters as series and shunt converters is considered as the conventional topology under study. On the counter to two-level inverters, the three-level inverters will give the better performance as seen from the literature. Thus, this chapter contributes the adaption of three-level structure to the UPQC to analyse the performance subjected to the various power quality problems. The unique design of multilevel inverter allows the span of high voltage and to reduce the device switching frequency without the need of transformers. It is seen that a diode clamped inverter, with all six phases of the back-to-back converter sharing a common dc-link, is capable of synthesizing a desired waveform from several levels of DC voltage [5]–[7]. Consequently, an enticing prospect would be to integrate a multilevel diode clamped inverter into a universal power conditioner. The features offered by multilevel universal power conditioner (UPQC-ML) are in-numerous when deciding to what type of control is to be used while compensating source voltage (voltage sag, unbalanced voltages, voltage harmonics, current harmonics or reactive power) and load currents playing an important role in the control of the back-to-back inverters [8], [9]. The system description of UPQC with two-level and three-level inverter structures are presented in detail in the following section.

2.2 System Description

2.2.1 Unified Power Quality Conditioner

The realization of the UPQC is done by using two voltage source inverters (VSI) namely, series converter and shunt converter, which are connected back to back through a common dc-link as shown in Figure 2.1 [6]. The six numbers of IGBTs are required for the

realization of each two-level converter for the three-phase system. The series converter is connected in series with the feeder through low pass LC filter (LPF) and three single-phase series transformers individually on the AC side. On the other hand, the shunt converter is in parallel to the point of common coupling (PCC) through coupling inductor (L_{sh}).

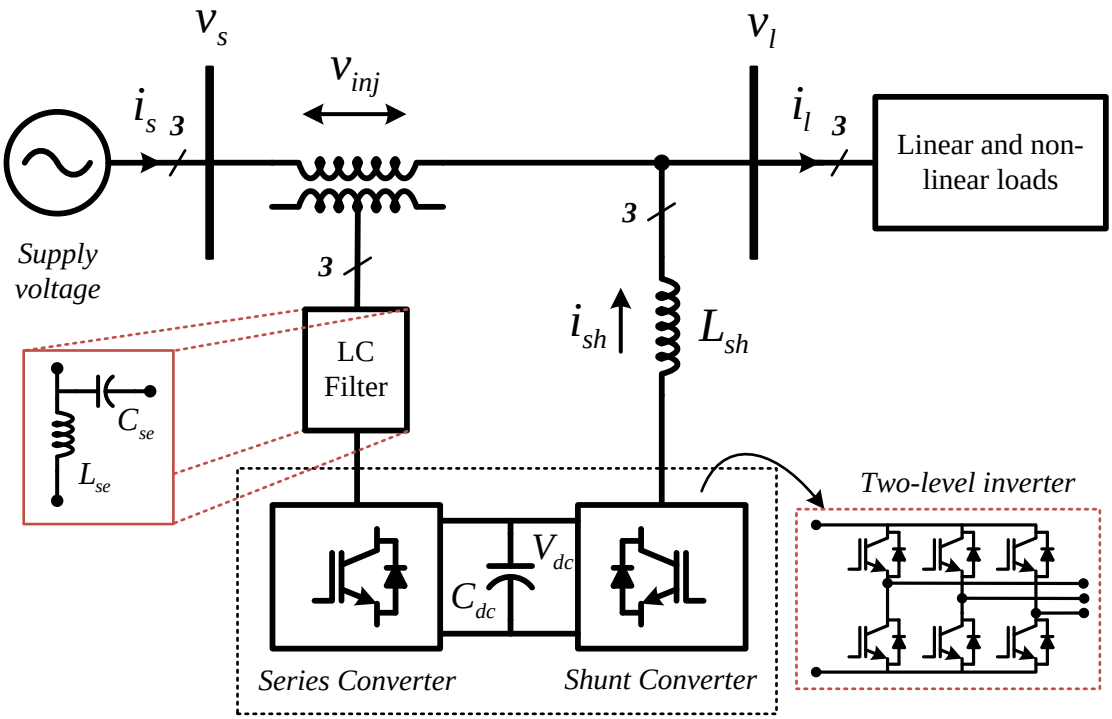


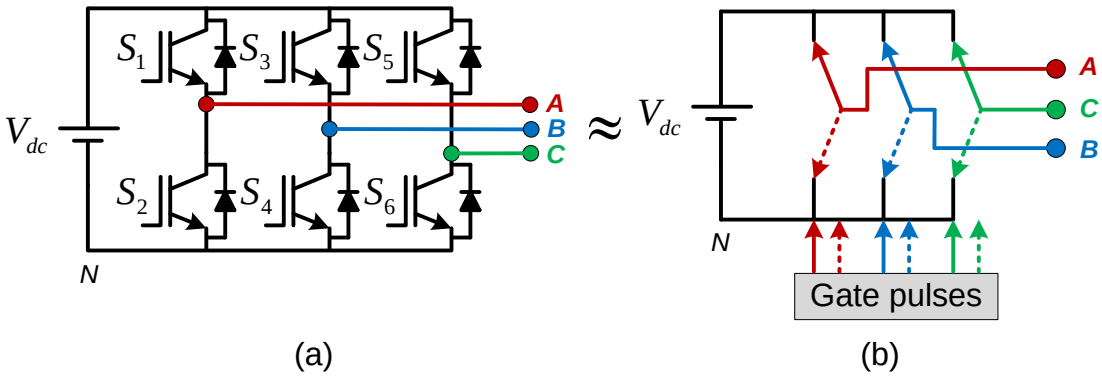
Fig. 2.1: Structure of unified power quality conditioner with two-level inverters

2.2.1.1 Two-level Inverter and Control Schemes

The two-level inverter is composed of six group of active switches, S_1–S_6, with a free-wheeling diode in parallel with each switch as shown in Figure 2.2(a). The typical power stage of three-phase two-level inverter is shown in Figure 2.2(b). The operating status of the switches can be represented by the switching states 1 and 0. The switching state '1' denotes that the upper switch in an inverter leg is on and the inverter terminal voltage (v_{AN}, v_{BN}, or v_{CN}) is positive ($+V_{dc}$) while '0' indicates that the inverter terminal voltage is zero due to the conduction of the lower switch.

There are eight possible combination of switching states represented as V_1 to V_8, which are shown in Figure 2.3. Six out of these eight states (V_1 to V_6) produce a nonzero output voltage and are known as active switching states and the remaining two states (V_0 and V_7) produce zero output voltage and are known as zero switching states.

In this thesis, at various conditions/cases of UPQC, the control sequence of switching states of two-level inverter can be takeover by adopting various pulse width modulation (PWM) techniques such as hysteresis current/voltage control, carrier PWM, space vector modulation (SVM). The brief introduction to these control schemes, which are used in this thesis work are presented in this section.



(a) (b)

Fig. 2.2: Three-phase two-level inverter [258]

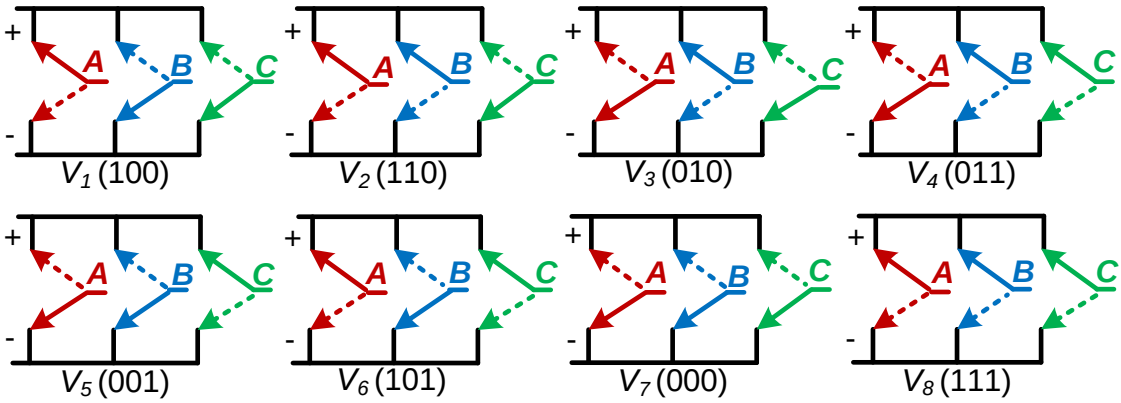


Fig. 2.3: Switching states for two-level inverter

1) Hysteresis Controller

Hysteresis control strategy has proven to be the most suitable solution for applications such as active filters, machine drives and high performance converter and also can be easily implemented in real-time applications [16]. In this chapter, hysteresis controller is adopted for both converters of UPQC by using voltage control for series converter and current control for shunt converter. The adoption of hysteresis controller for the application of UPQC is depicted in Figure 2.4 As in the case of shunt converter; this subsystem of hysteresis current controller was developed to generate the switching pulses to control VSI switches by comparing the actual current signal to the reference current signal. The actual and reference current signals are considered to shunt compensating currents ($i_{sh\_abc}, i^*_{sh\_abc}$) decided by the control strategy, which is adopted for the shunt converter. On the other hand, hysteresis voltage controller generates the switching pulses to VSI switches by comparing the actual voltage signal to the reference voltage signal. These signals are considered to be as series injecting voltages ($v_{inj\_abc}, v^*_{inj\_abc}$). To understand the working of hysteresis controller, the control signals are considered as current signals.

The control scheme gives the switching pattern of active filter switches in order to maintain the actual injected current within a desired hysteresis band (HB) as illustrated in Figure 2.5 [15]–[18]. In the case of positive input current i_{sh}, the current error exceeds the

upper limit of the hysteresis band; thus, inverter output should be set as zero, so current error will be forced to the opposite direction without reaching the other outer limit. If this zero condition does not provide the opposite of current error, it will keep forwarding through inner limit to the other outer hysteresis limit. At this time, a reverse polarity of inverter output will be controlled and therefore current direction will be reversed [14], [15], [17]. The switching frequency of hysteresis current control strategy described and presented above depends mainly on how fast the current changes from upper limit to lower limit of hysteresis band and inversely. Thus, the switching frequency does not remain constant throughout the switching operation but changes along with the current waveform [15], [17], [18].

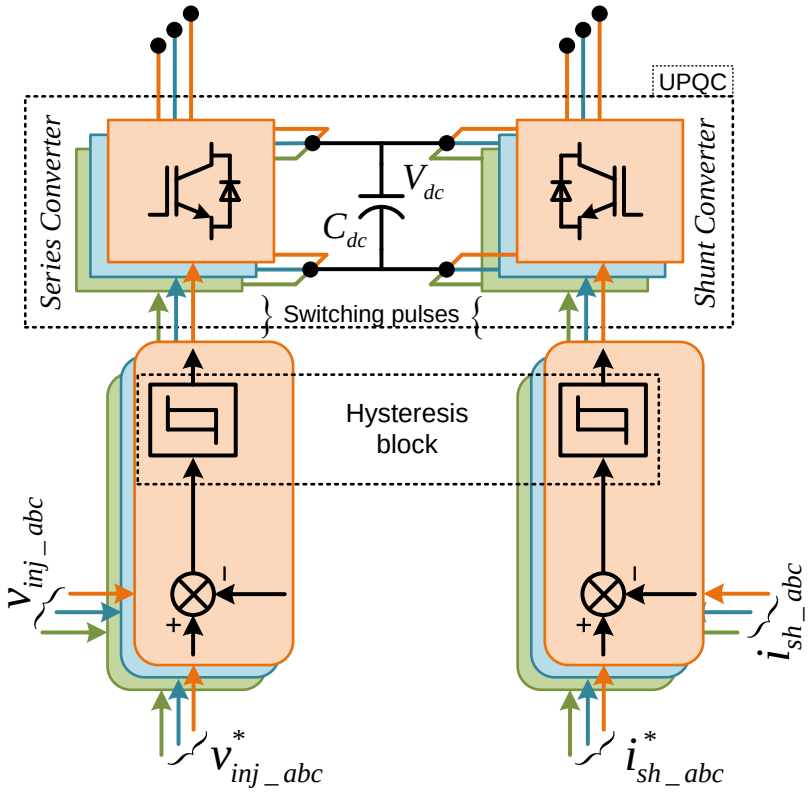


Fig. 2.4: Application of hysteresis controller for two-level inverter in UPQC

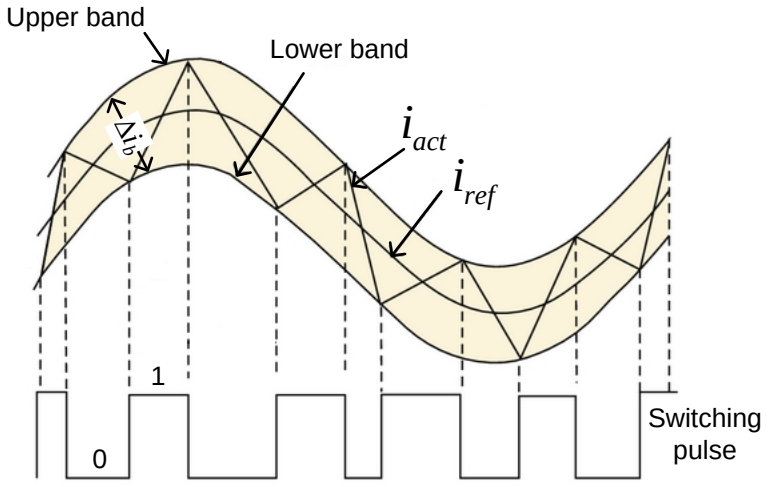


Fig. 2.5: Hysteresis controller

2) PWM Controller

In the Chapter 6, pulse width modulation (PWM) controller is used to generate the switching pulses for series and shunt converters as shown in Figure 2.6.

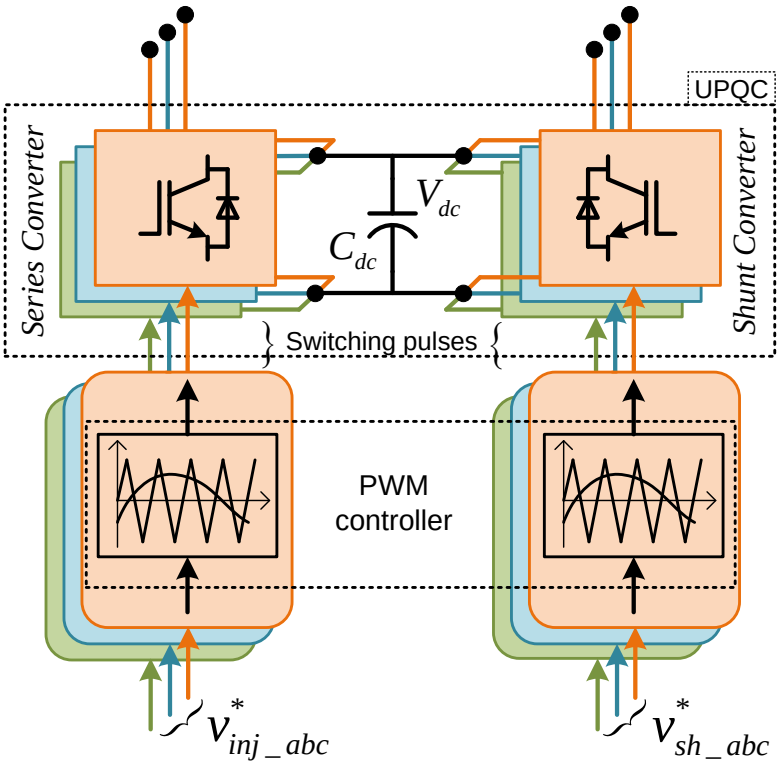


Fig. 2.6: Application of PWM controller for two-level inverter in UPQC

The reference voltage and current signals are generated by the control strategy adopted based on the compensation requirements of UPQC. These reference signals are considered as modulating signals for implementing PWM controller, where triangular carrier signal is compared with the modulating signal to generate the switching commands for converter switches.

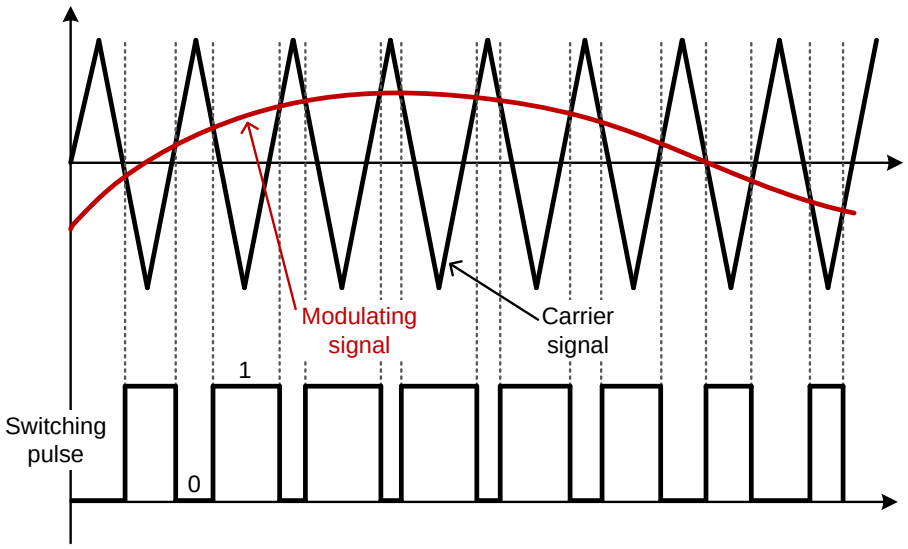


Fig. 2.7: SPWM controller for two-level inverter

Figure 2.7 shows the implementation of PWM controller, where sinusoidal PWM (SPWM) is taken an example to explain the working of PWM controller. The main advantage of carrier based SPWM is that the complexity is very low and the dynamic response. Unlike hysteresis controller, the switching frequency is being decided by the triangular carrier frequency.

3) Space Vector Modulation

The application of space vector modulation (SVM) controller block in the use of MPC controlled UPQC is shown in Figure 2.8. This scheme is implemented in Chapter-3 for UPQC-2L. SVM based generation of switching pulses are used in which, model predictive control (MPC) selects the optimal switching sequence from the available switching states.

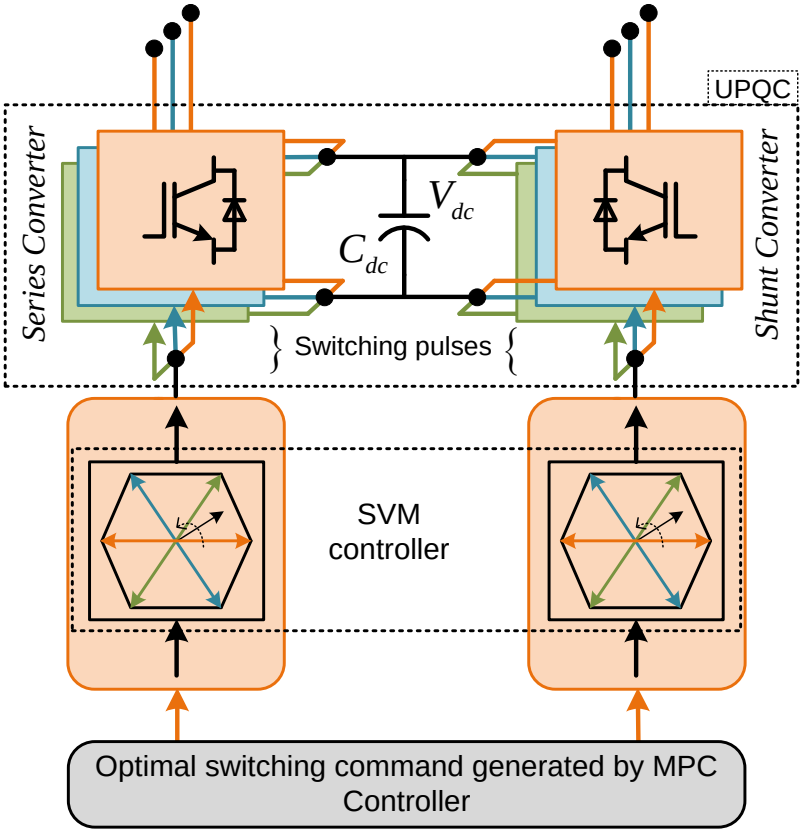


Fig. 2.8: Application of SVM controller for two-level inverter in UPQC

A three-phase two-level inverter is shown in Figure 2.2 (a), which consists of eight switching states as shown in Figure 2.3. The vector representation of these switching states are presented in Figure 2.9(a). Out of eight switching states, two are null states (000 and 111) that produce a zero inverter output voltage (line/phase voltages for the corresponding switching states) as shown in Figure 2.9(a). The other six states (V_1 to V_6) produces a vigorous voltage vector of the same magnitude $0.667V_{dc}$ and have been divided by a constant phase displacement of 60° in a space vector plane as shown in Figure 2.9(a). The tips of these vectors form a regular hexagon. The defined area enclosed by two adjacent

vectors, within the hexagon is known as a sector. Thus there are six sectors numbered 1 to 6 as shown in Fig. 3.5(a). The vectors have zero magnitude are referred to as zero switching state vectors. They assume a position at the origin in the α-β reference plane.

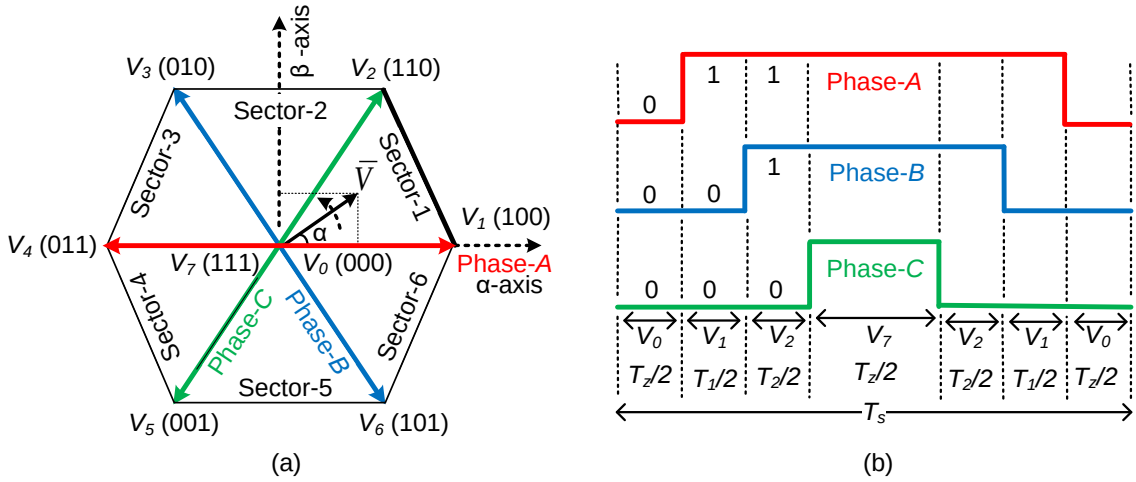


Fig. 2.9: (a) Vector representation for two-level inverter, (b) Pulse pattern of sector-1

The selection of pulse pattern for sector-1 is shown in Figure 2.9(b). The selection of switching states in all the sectors is listed in Table-2.1 [254]. The calculation of switching times (T_1, T_2, and T_z) are described in [268] for two-level SVM.

Table 2.1: Selection of switching sequences for SVM in all sectors

Sector	1st half-sequence	2nd half-sequence
1	$V_0V_1V_2V_7$	$V_7V_2V_1V_0$
2	$V_0V_3V_2V_7$	$V_7V_2V_3V_0$
3	$V_0V_3V_4V_7$	$V_7V_4V_3V_0$
4	$V_0V_5V_4V_7$	$V_7V_4V_5V_0$
5	$V_0V_5V_6V_7$	$V_7V_6V_5V_0$
6	$V_0V_1V_6V_7$	$V_7V_6V_1V_0$

2.2.1.2 Multi-Level Inverter and Control Schemes

In general, the two-level inverters are suitable for low voltage (LV) applications, but not medium voltage (MV) [267]–[268]. The two-level inverter has few limitations such as high switching frequency, more voltage/current stresses on devices, switching losses, overall device cost of the inverter, etc. To overcome the above drawbacks, the multi-level inverter (MLI) is used for medium voltage (MV) applications. To further improve the voltage, current compensation characteristics of UPQC, the two-level voltage source inverter is replaced by three-level diode clamped inverter [267]. In [267], the comparative analysis between two-

level and three-level UPQC is not presented. The author was focused on dc-link balancing of the three-level structure. In this chapter, the UPQC is implemented with both structures of two-level and three-level inverters to compare the performance related to compensation characteristics.

The Multilevel inverter (MLI) concept utilizes a higher number of active semiconductor switches to perform the power conversion in small voltage steps. This approach offers several advantages when compared with traditional two-level inverter, such as the smaller voltage steps leads to the production of high quality output waveforms, reduction of the dv/dt stresses and reduction in the electromagnetic interference. Another important feature of MLI is that the semiconductor switches are connected in series, which eliminates over voltage concerns [267].

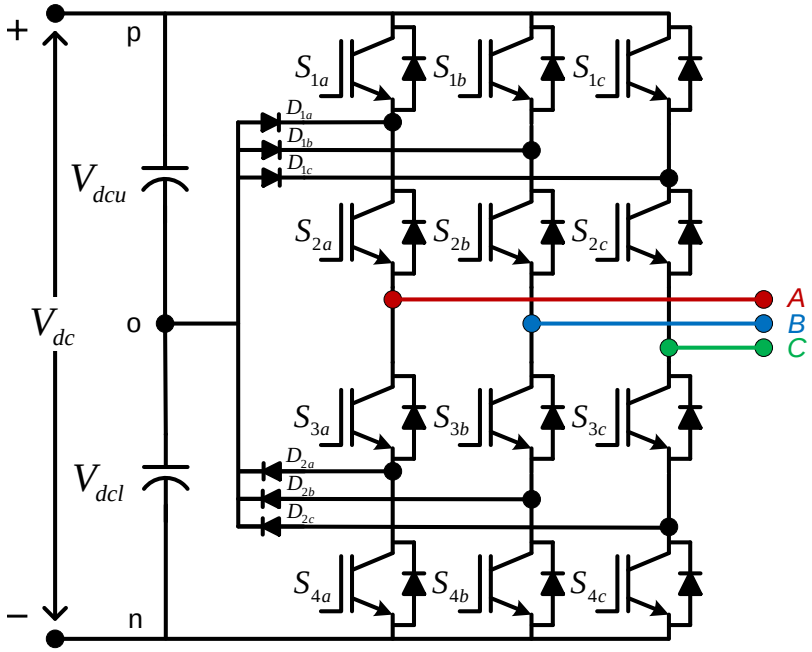


Fig. 2.10: DCMLI structure of three-level inverter

Advancement in power semiconductor technology has led to production of switching devices capable of switching at high speeds and at high power levels. The PWM VSIs are being used extensively instead of CSIs in industrial applications owing to their control, flexibility and acceptable harmonic spectrum. As the power rating of the device goes up, the switching frequency has to be reduced to limit the switching power loss. In such situation, MLI configuration is being suggested for reducing the harmonic content of the inverter output at a low switching frequency for high power applications [267] The three main types of MLIs in use are diode-clamped multilevel inverter (DCMLI), flying-capacitor multilevel inverter (FCMLI) and cascaded H-bridges multilevel inverter (CHBMLI). The circuit diagrams of these MLIs are shown in Figures 2.10, 2.11 and 2.12, respectively [268]. The general concept behind this FCMLI is that the added capacitor is charged to one half of the dc-link voltage and may be inserted in series with the dc-link voltage to form an additional voltage level.

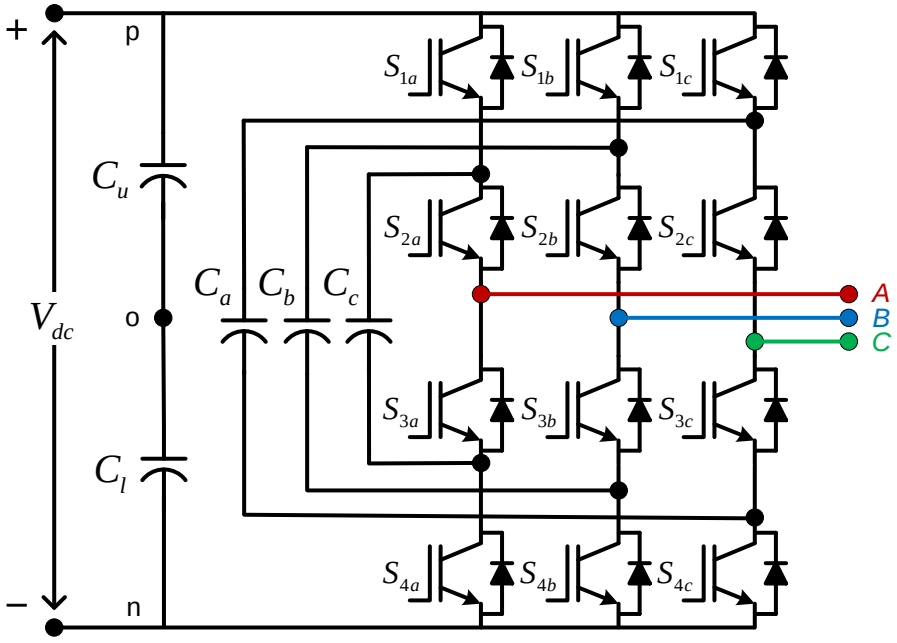


Fig. 2.11: FCMLI structure of three-level inverter

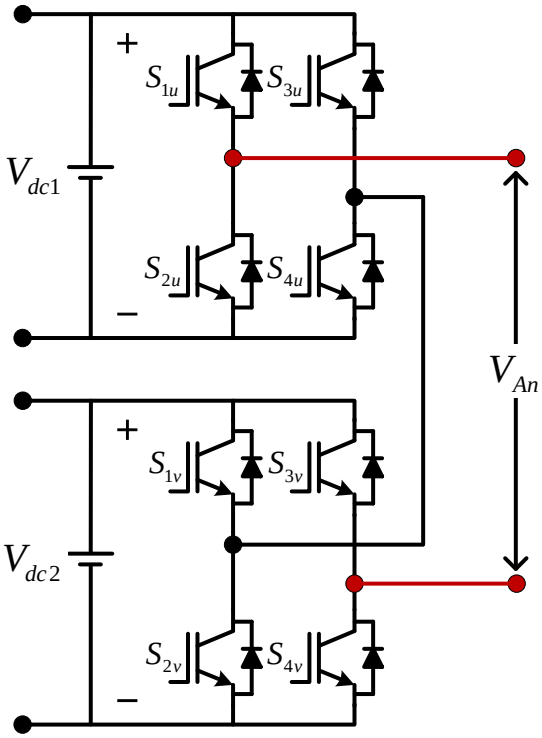


Fig. 2.12: Single-phase of CHBMLI structure with two DC sources

The capacitor voltage may be either added to the converter ground or subtracted from the dc-link voltage. The main drawbacks are: The number of capacitors required is high compared to other topologies, which is important due to the cost of the reactive devices and the inverter control can be very complicated and the switching losses are high for real power transmission. The CHBMLI is simply a series connection of multiple H-bridge inverters. The CHBMLI introduces the idea of using separate DC sources to produce an AC voltage waveform. The major drawback is that, it needs separate DC sources for real power

conversion. Out of the three basic MLI structures, much attention and widely used is the DCMLI because of simplicity of its control [268].

A) Diode-Clamped Multilevel Inverter (DCMLI)

A DCMLI with *m*-level typically consists of (*m*-1) capacitors on DC bus and produces m-voltage levels in the phase voltage output. Figure 2.10 shows a three-level diode clamped multi-level inverter. Comparing this topology with that of a standard two-level inverter shows that there is twice as many power electronics switches as well as added diodes. However, it should be noted that the voltage rating of power electronic switches is half of that of the power electronic switches in the two-level inverter. In three-level inverter, the voltage across each capacitor is $0.5V_{dc}$, and each device voltage stress is limited to capacitor voltage level $0.5V_{dc}$ through clamping diodes. A generalized m-level inverter leg requires (*m*-1) capacitors, 2(*m*-1) switching devices and (*m*-1)*(*m*-2) clamping diodes. For the operation of three-level DCMLI, there are three switching states for each inverter leg; *p*, *o* and *n*. Where '*p*' means that the upper two switches in a leg '*A*' are 'on' and the inverter terminal voltage is $+0.5V_{dc}$; '*n*' means that the lower two switches are 'on' with a terminal voltage of $-0.5V_{dc}$; '*o*' signifies that the inner two switches are 'ON' with a terminal voltage of zero. The corresponding switching states of three-level inverter in one of the phase (*A*) are given in Table 2.2 [268].

Table 2.2: Three-level diode clamped multi-level inverter per phase switching states

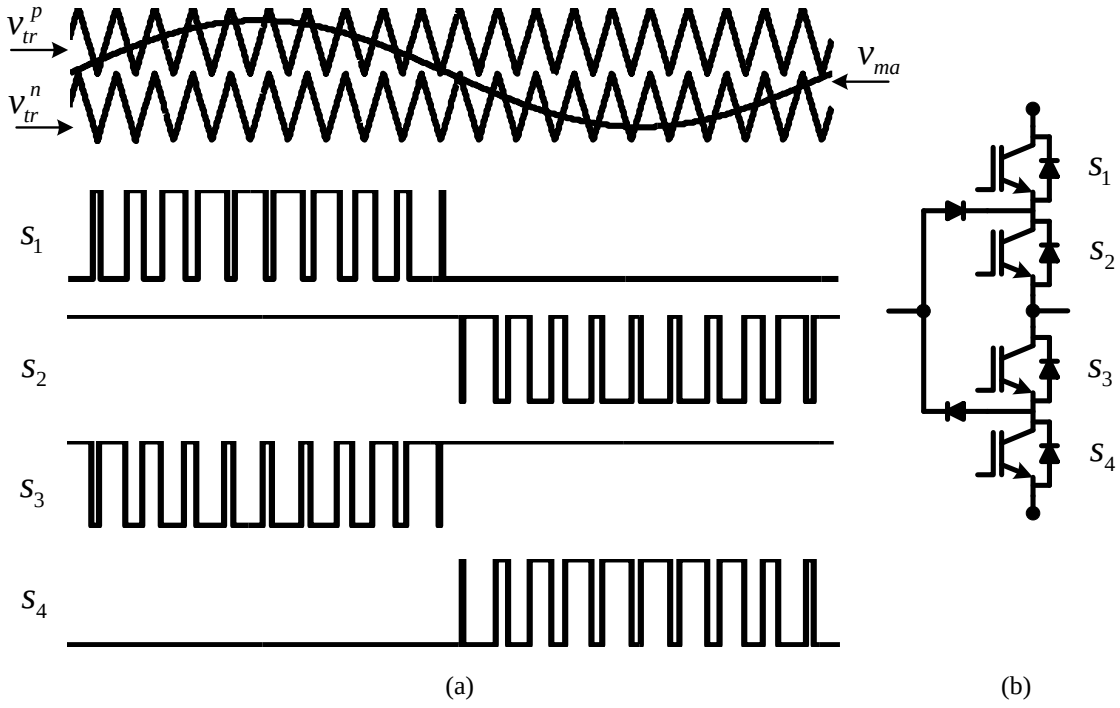
Switching	Switching states				Pole voltage	Line voltage
	S_{1a}	S_{2a}	S_{3a}	S_{4a}		
p	1	1	0	0	$0.5V_{dc}$	V_{dc}
o	0	1	1	0	0	$0.5V_{dc}$
n	0	0	1	1	$-0.5V_{dc}$	0

In this thesis, similar to two-level inverter structure based UPQC, the three-level UPQC is also uses PWM techniques such as multi-carrier PWM, space vector modulation (SVM) to control the sequence of switching states of three-level inverter. The brief introduction to these control schemes are presented in this section.

1) Multi-carrier PWM Controller

In this Chapter, switching pulses for diode clamped multilevel inverter based UPQC are generated by using multi-carrier PWM. The multi-carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. In general, phase-shifted modulation scheme cannot be utilized for diode clamped multi-level inverters [268]. An *m*-level diode clamped inverter using level-shifted multicarrier modulation scheme requires (*m*–1) triangular carriers, all having the same frequency and amplitude. The (*m*–1) triangular carriers are vertically disposed such that the

bands they occupy are contiguous. The level-shifted multicarrier modulation further sub categorised into three schemes. (a) in-phase disposition (IPD), where all carriers are in phase; (b) alternative phase opposite disposition (APOD), where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference. In what follows, only IPD modulation scheme is discussed since it provides the best harmonic profile of all three modulation schemes [268].



(a) (b)

Fig. 2.13: (a). In-phase level shift modulation, (b). Phase leg of three-level diode clamped multilevel inverter [268]

The IPD level shift modulation is considered as multicarrier PWM for three-level DCMLI, which requires two carrier signals, namely upper (v_{tr}^{p}) and lower triangular (v_{tr}^{n}) signals; and three modulating signals which are derived from the voltage controller. Figure 2.13(a), shows the IPD level shift modulation for three-level diode clamped multilevel inverter for phase-*A* [268]. Figure 2.13(b), shows the one phase leg of three-level diode clamped multilevel inverter, where S_1, S_3, and S_2, S_4, are complimented switches. The switching pulses for S_1 and S_3 are generated by the PWM operation of upper triangular (v_{tr}^{p}) and modulating signal, v_{ma} and similarly pulses will be generated for S_2, and S_4 by the PWM operation of lower triangular (v_{tr}^{n}) and modulating signal, v_{ma} as shown in Figure 2.13(a).

2) Space Vector Modulation

In MLIs, the SVM methodologies have the advantage of increased inverter output voltage. In this modulation technique as used in other works [38], [83], the space vector diagram of MLI is divided into different forms of sub-diagrams, in such a manner that the

implementation becomes simpler. However, these works do not reach a generalization of the two-level SVM because either they divide the diagram into triangles or interfere geometrical forms. In this work, a simple and fast method is implemented that divides the space vector diagram of three-level inverter into several small sectors, each sector again divided into four sub-sectors as shown in Figure 2.14. In this manner, three-level space vector modulation (SVM) based generation of switching pulses are used for UPQC-ML in Chapter 3, where model predictive control (MPC) selects the optimal switching sequence from the available switching states.

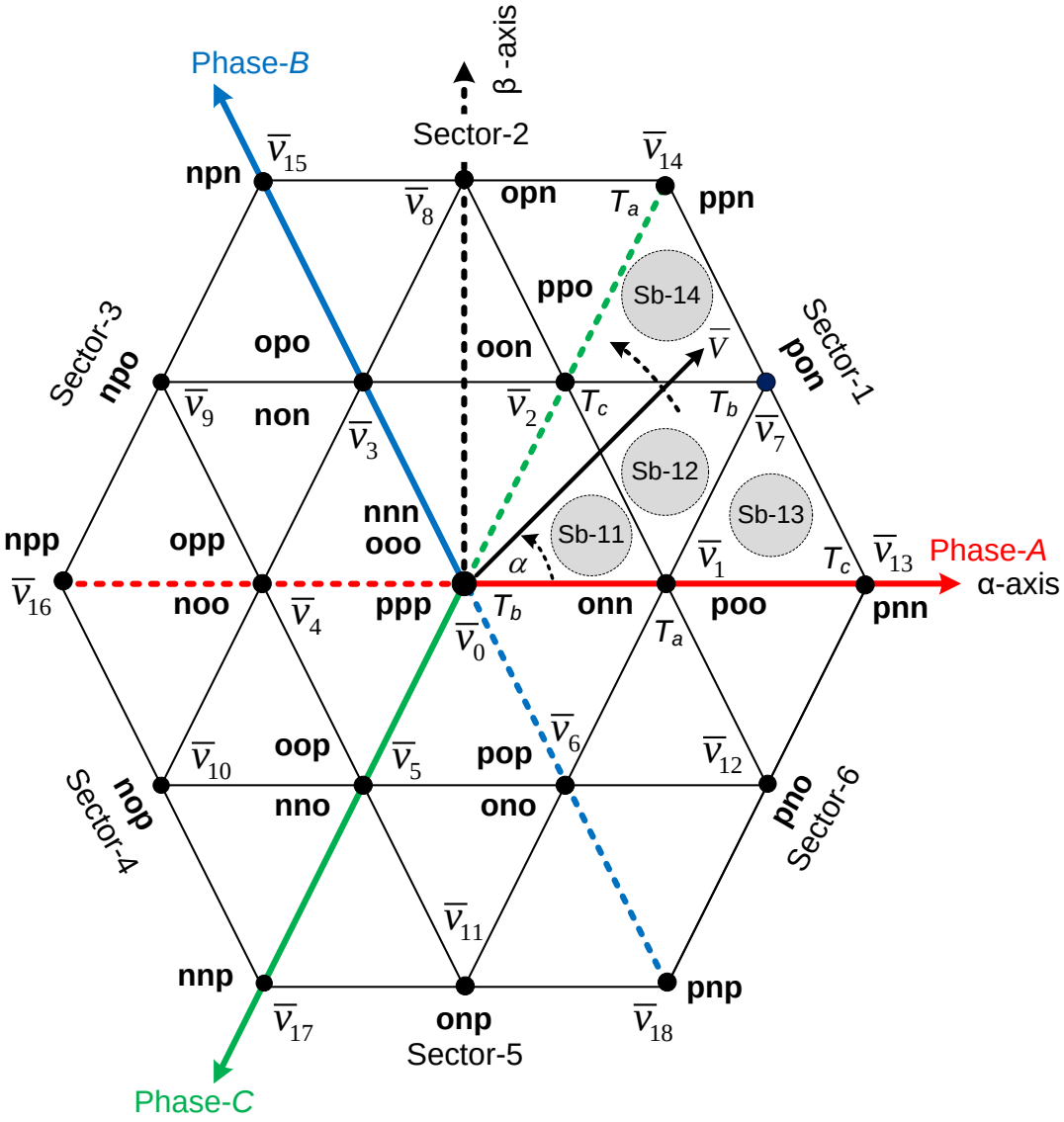


Fig. 2.14: Space vector diagram for three-level inverter [268]

The design of three-level SVM is difficult to understand as compared to two-level inverter. However, the pulses are generated to the inverter as similar to the two-level SVM. The three-level DCMLI is shown in Figure 2.10. It has 27 switching state vectors in which there are three null state vectors and 24 active state vectors as represented in Figure 2.14 [268]. Moreover, these 27 switching state vectors again divided into zero voltage vectors,

small voltage vectors, medium voltage vectors, and large voltage vectors as given in Table 2.3 and the corresponding vector magnitudes are given as below,

The magnitude of three zero voltage vectors are

$$\overline{v}_0 = 0 \tag{2.36}$$

The magnitudes of twelve small voltage vectors are

$$\overline{v}_1 = \overline{v}_2 = \overline{v}_3 = \overline{v}_4 = \overline{v}_5 = \overline{v}_6 = 0.33V_{dc} \tag{2.37}$$

The magnitudes of six medium voltage vectors are

$$\overline{v}_7 = \overline{v}_8 = \overline{v}_9 = \overline{v}_{10} = \overline{v}_{11} = \overline{v}_{12} = 0.5773V_{dc} \tag{2.38}$$

The magnitudes of six large voltage vectors are

$$\overline{v}_{13} = \overline{v}_{14} = \overline{v}_{15} = \overline{v}_{16} = \overline{v}_{17} = \overline{v}_{18} = 0.667V_{dc} \tag{2.39}$$

Three-level inverter has 27 switching state vectors in which three are the zero voltage vectors (v_0) and twenty-four are active state vectors as represented in Figure 2.4.

The 24 active vectors again divided into, small voltage vectors (v_0, v_1, v_2, v_4, v_5, and v_6), medium voltage vectors (v_7, v_8, v_9, v_{10}, v_{11}, and v_{12}), and large voltage vectors (v_{13}, v_{14}, v_{15}, v_{16}, v_{17}, and v_{18}), and their magnitudes are $0.33V_{dc}$, $0.5773V_{dc}$, and $0.667V_{dc}$, respectively [49-50]. Moreover, the active voltage vectors are phase displaced by the same angle, i.e., 60° with respect to their group (small/medium/high) of voltage vectors only as shown in Figure 2.14 [268]. To generalize the three-level SVM into two-level SVM then the three-level SVM has been divided into six sectors i.e. sector-1, sector-2, sector-3, sector-4, sector-5, and sector-6. However, each sector again divided into four sub-sectors. The sector-1 is shown in Figure 2.14, which is divided into four sub-sectors Sb-11, Sb-12, Sb-13, and Sb-14. A three-phase three-level DCMLI is shown in Figure 2.10, in which the nodes '*p*', '*o*', and '*n*' indicate the positive, neutral, and negative positions of the inverter and the corresponding voltages are found when top, middle, and bottom two switches per phase are on, respectively. The corresponding three pole voltages per phase ($V_{A0}/V_{B0}/V_{C0}$) are given as $+0.5V_{dc}$, 0, and $-0.5V_{dc}$ when A, B, and C phases are connected to *p*, *o*, and *n*, respectively [268].

Capacitor Voltage Balance for Three-level DCMLI:

Prior to discussing in Chapter 3, to ensure balanced capacitor voltages at split dc-link of three-level DCMLI based UPQC, the proposed model predictive control (MPC) decides the optimal switching state, implemented through three-level SVM is used. In this sub-section, the general causes of unbalancing capacitor voltages are discussed. The voltage unbalance problem on capacitors (C_1 and C_2) can be improved using SVM algorithm without the need of an extra controller in which, the appropriate switching vector is selected based on the reference vector position without using an extra controller [268]. Figure 2.15 shows the effect of capacitor voltages for different switching vectors involved at sector-1 region.

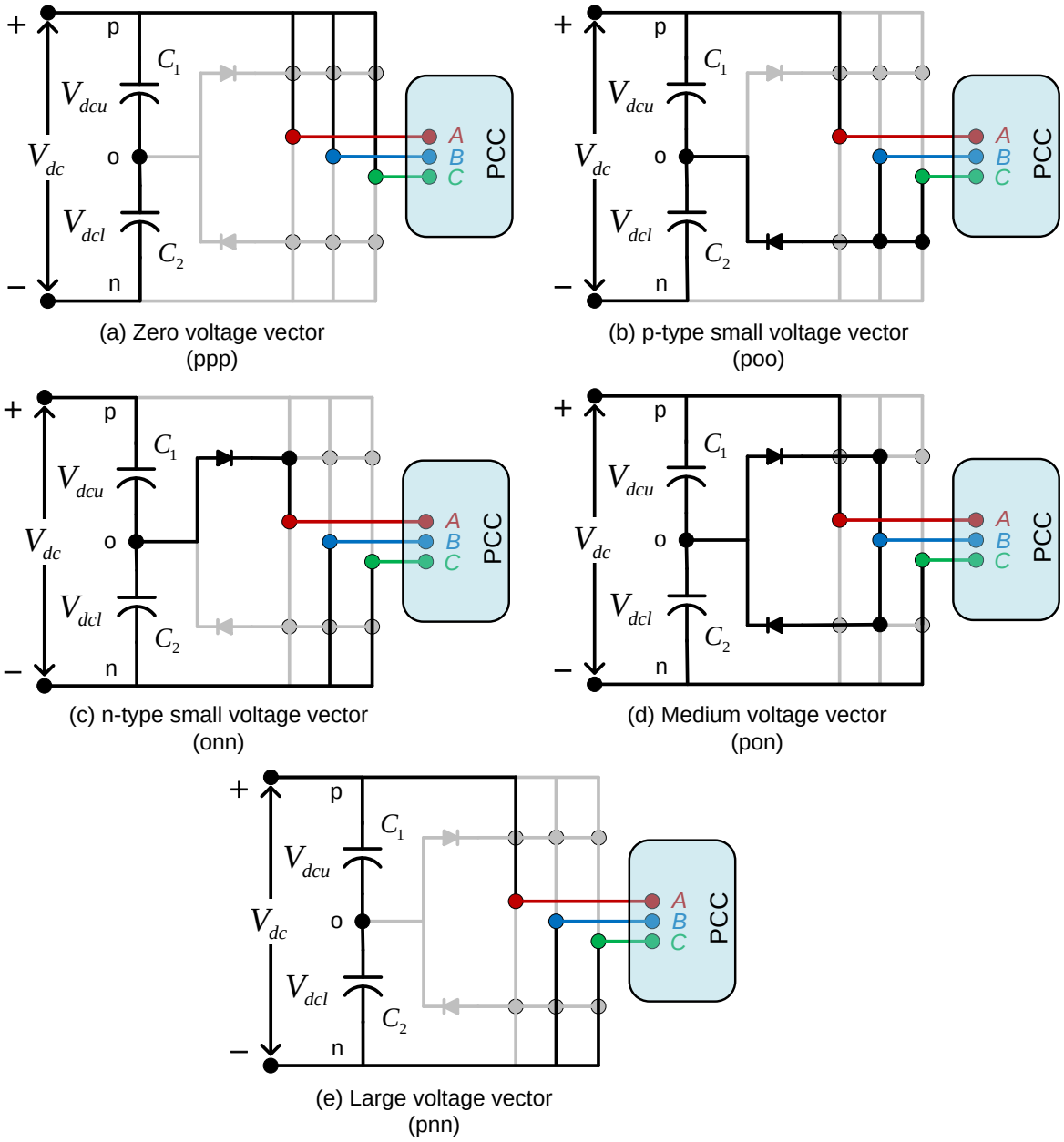
Table 2.3: Three-level switching states with vector classification [268]

Space vector		Switching states		Vector classification	Vector magnitude
$\overline{V}_0$		[ooo, ppp, nnn]		Zero vector	0
		p-type	n-type	Small voltage vector	$0.333V_{dc}$
$\overline{V}_1$	v_{1p}	[poo]			
	v_{1n}		[onn]		
$\overline{V}_2$	v_{2p}	[ppo]			
	v_{2n}		[oon]		
$\overline{V}_3$	v_{3p}	[opo]			
	v_{3n}		[non]		
$\overline{V}_4$	v_{4p}	[opp]			
	v_{4n}		[noo]		
$\overline{V}_5$	v_{5p}	[oop]			
	v_{5n}		[nno]		
$\overline{V}_6$	v_{6p}	[pop]			
	v_{6n}		[ono]		
$\overline{V}_7$		[pon]		Medium vector	$0.5773V_{dc}$
$\overline{V}_8$		[opn]			
$\overline{V}_9$		[npo]			
$\overline{V}_{10}$		[nop]			
$\overline{V}_{11}$		[onp]			
$\overline{V}_{12}$		[pno]			
$\overline{V}_{13}$		[pnn]		Large vector	$0.667V_{dc}$
$\overline{V}_{14}$		[ppn]			
$\overline{V}_{15}$		[npn]			
$\overline{V}_{16}$		[npp]			
$\overline{V}_{17}$		[nnp]			
$\overline{V}_{18}$		[pnp]			

Zero and large voltage vectors: The zero and large voltage vectors are shown in Figure 2.15(a) and (e) in which there is no chance of current flow in capacitors and hence the constant voltage will be maintained in both capacitors.

Small voltage vectors: Figure 2.15(b) and (c) belong to the *p* and *n* type small voltage vectors. The corresponding voltage across dc-link capacitor C_2 (V_{dcl}) increases/decreases based on current flow direction. However, the voltage across the dc-link capacitor C_1 (V_{dcu}) is quite opposite to V_{dcl} as shown in Figure 2.15(b) and (c) [268]. Hence, the average value of

V_{dcu} and V_{dcl} is maintained constant when *p* and *n*-type small voltage vectors are operated once at half of the switching period.



(a) Zero voltage vector (ppp)

(b) p-type small voltage vector (poo)

(c) n-type small voltage vector (onn)

(d) Medium voltage vector (pon)

(e) Large voltage vector (pnn)

Fig. 2.15: Effect of capacitor voltages for the corresponding switching states

Medium voltage vector: The dc-link voltages V_{dcu} and V_{dcl} are kept constant value, while operating medium voltage vector because there is no chance of current flow through the capacitors (C_1 and C_2) and phase-*B* as shown in Figure 2.15(d) [268].

Therefore, the capacitor voltages are well balanced and maintained constant for a given switching period by using zero, medium and large voltage vectors. They can be activated once per half of the switching period. Moreover, the small voltage vectors are operated twice per half of the switching period to maintain the constant voltages across the dc-link capacitors. Similarly, the process remains the same to keep the constant voltage across the dc-link capacitors in another sector region also.

2.2.2 Unified Power Quality Conditioner Using Three-level DCMLI

In case of multilevel unified power quality conditioner (UPQC-ML), multilevel inverters replace the two-level inverters, whereas in the present work, three-level diode clamped multilevel inverters are preferred. So that the topology is named as three-level UPQC (UPQC-3L) in this work. As shown in Figure 2.16, the two diode clamped inverters are connected back to back with a split dc-link with two identical capacitors. The voltages across top and bottom capacitors are indicated as V_{dcu} and V_{dcl} respectively. The mid point of capacitors is taken as a neutral point (*N*) for the generation of three-level output voltage. The three- level diode clamped multilevel inverter consists of twelve numbers of IGBTs and six numbers of clamping diodes [10]. In-detail discussion about the three-level diode clamped inverter and its various control schemes, which are carried out in this thesis work including the present chapter are presented in the previous sub-section.

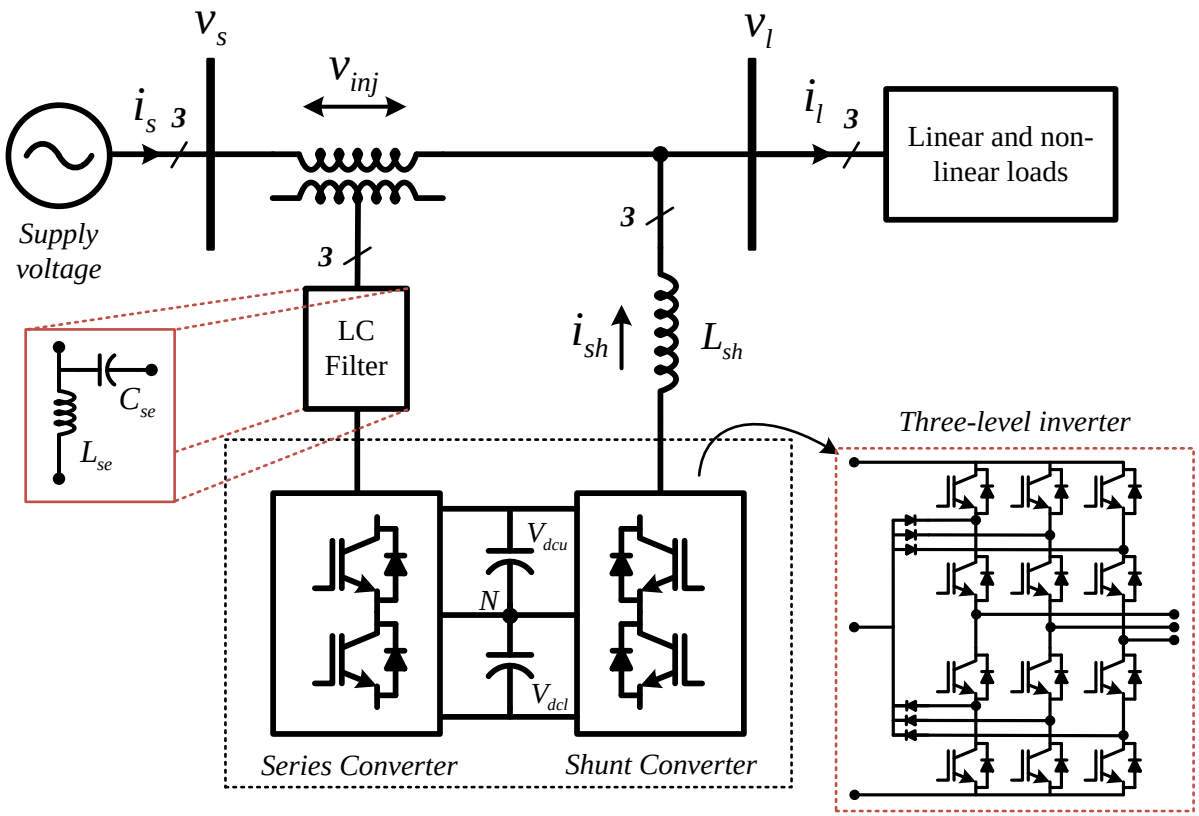


Fig. 2.16: Structure of unified power quality conditioner with three-level inverters

2.3 Parameter Estimation of Unified Power Quality Conditioner

The design of three-phase UPQC includes the design of three-leg series converter and three-leg shunt converter which is shown in Figure 2.1 and Figure 2.16. The parameters of the converters should be designed deliberately for better performance [7]. The critical parameters that should be taken into consideration while designing UPQC are dc-link voltage (V_{dc}), dc-link capacitor (C_{dc}), shunt interfacing inductance (L_{sh}), series interfacing inductance (L_{se}), series capacitor (C_{se}) and the switching frequency (f_{sw}).

2.3.1 Design of Shunt Converter part of UPQC

The shunt converter includes a VSI and interfacing inductors. The design of VSI includes the dc-link voltage level, dc-link capacitance value. The data for three-phase UPQC are as follows:

- Three-phase source line-line voltage: 200V, 50Hz.
- Three-phase balanced linear load: 1380kW, 0.80 lagging power factor

(A) Selection of DC-Link Voltage

The minimum dc-link voltage of the shunt converter should be greater than the twice of the peak phase voltage of the distribution system [134]. The dc-link voltage is calculated as

$$V_{dc} = \frac{2\sqrt{2}V_{L-L}}{\sqrt{3}m} \tag{2.40}$$

where *m* is the modulation index and is considered as 1 and V_{L-L} is the line output voltage of the shunt converter. Thus, V_{dc} is obtained as 326.69V for a V_{L-L} of 200V and it is approximated to 330V. The dc-link voltage across each dc-link capacitor for UPQC-3L is considered as the half the total dc-link as estimated for UPQC-2L.

(B) Selection of DC-Link Capacitor

The value of the DC capacitor (C_{dc}) of the VSI depends on the instantaneous energy available to the shunt converter during transients. The principle of energy conservation is applied as

$$\frac{1}{2}C_{dc}(\mathrm{V}_{dc}^2 - \mathrm{V}_{dc\_min}^2) = 3kV_{ph}(aI_{sh})t \tag{2.41}$$

$$C_{dc} = \frac{6kV_{ph}(aI_{sh})t}{(\mathrm{V}_{dc}^2 - \mathrm{V}_{dc\_min}^2)} \tag{2.42}$$

Where, V_{dc} is the nominal dc-link voltage equal to the reference DC voltage and V_{dc_min} is the minimum voltage level of the dc-link, *a* is the overloading factor, V_{ph} is the phase voltage, I_{sh} is the reactive phase load current, and t is the time by which the dc-link voltage is to be recovered. Considering the minimum voltage level of the dc-link $V_{dc\_min} = 320V$, $V_{dc} = 330V$, $V_{ph} = 115V$, $I_{ph} = 3A$, $t = 30ms$, $a = 1.2$, and variation of energy during dynamics =10% ($k = 0.1$), the calculated value of C_{dc} is 1146.46μF and it is selected as 1500μF for UPQC-2L. For UPQC-3L two capacitors are selected with the same rating as estimated for UPQC-2L.

(C) Selection of Coupling Inductor

The selection of the shunt coupling inductance (L_{sh}) depends on the current ripple, $I_{cr(p-p)}$, switching frequency of the converter f_s, and dc-link voltage (V_{dc}), and it is given as

$$L_{sh} = \frac{\sqrt{3}mV_{dc}}{(12af_sI_{cr})} \tag{2.43}$$

where *m* is the modulation index and a is the overloading factor. The switching frequency of the converter (f_s) depends on the PWM method used for controlling the converter. For carrier based level-shifted PWM technique with carrier signal frequency f_{cr}, fs can be calculated as

$$f_s = 2 f_{cr} \tag{2.44}$$

Considering $I_{cr} = 5\%$, $f_s = 10$kHz, $m = 1$, $V_{dc} = 330V$, and $a = 1.2$, the value of L_{sh} is calculated to be 26.2mH. The round-off value of 25mH is selected in this investigation.

On one hand, for a better harmonic cancellation and reactive power compensation a higher value of inductance is preferable. However, on the other hand, a very high value of inductance will result in slow dynamic response of the shunt compensator and it would not be possible to compensate some of the load harmonics [130]. So, a compromise solution has to be required to further optimize the value of the coupling inductor [229].

2.3.2 Design of Series Converter Part of UPQC

The series converter portion of UPQC consists of three-phase VSI, interfacing inductors with ripple filter and injection transformer.

(A) Selection of Injection Transformer

The injection transformer is selected for connecting the VSI in series with the supply. The voltage rating of the transformer depends on the voltage to be injected and the DC bus voltage of the VSI. For compensating a voltage variation of ±20%, the voltage to be injected is calculated as

$$V_{inj} = xV_S = 0.2 * 115 = 23\text{V} \tag{2.45}$$

The turns ratio of the injection transformer is computed as follows. The dc bus voltage of 330V (decided for 200V for the shunt part of UPQC) can be used to obtain 200V across the line at the output of the VSI using a PWM controller. However, the series converter requires only 23V per phase. Therefore, the maximum value of the turns ratio of the injection transformer is

$$n = V_{VSI} \big/ V_{inj} = 200 \big/ \sqrt{3} * 23 = 5 \tag{2.46}$$

The VA rating of the injection transformer is

$$\begin{aligned} S_{tr} &= 3V_{inj} I_{se(under\,sag)} = 3V_{inj}(P_l \big/ (3(1-x)V_S)) \\ &= 3 * 23 * (1380 \big/ (3 * (115 - 23))) \\ &= 345\,\text{VA} \end{aligned} \tag{2.47}$$

(B) Selection of Series Filter Inductance

The current through the secondary side of the injection transformer is decided by real power of the load. The minimum supply current occurs during voltage swell. The minimum value of supply current is

$$I_{se\,(under\,swell)} = P_l / (3(1+x)V_S) = 1380/(3*(115+23)) = 3.4\,\mathrm{A} \quad (2.48)$$

Considering a 10% ripple in supply current, the value of filter inductance of the series converter is given as

$$L_{se} = (\sqrt{3}/2)nmV_{dc}/6xaf_s\Delta I_{se} \approx 8\ \mathrm{mH} \quad (2.49)$$

(C) Selection of Ripple Filter Capacitance

A high-pass first-order filter tuned at half the switching frequency is used to filter the high-frequency noise from the voltage. Hence, the ripple filter is designed considering the cut-off frequency of 5kHz. The time constant of the filter should be very small compared with the fundamental time period (T), $R_f C_f \ll T/10$, where R_f and C_f are the ripple filter resistance and its capacitance, respectively. Considering a low impedance of 8.1Ω for the harmonic voltage at a frequency of 5kHz, the ripple filter capacitor is designed as $C_f = 5$μF. A series resistance (R_f) of 5Ω is included in series with the capacitor (C_f). The impedance is found to be 637Ω at fundamental frequency, which is sufficiently large, and hence the ripple filter draws negligible fundamental frequency current.

2.4 Control Strategies

In order to evaluate the performance of UPQC with two-level VSI and three-level DCMLI, the both topologies are employed with the same control strategies. The synchronous reference frame theory (*d-q* method) is used for series and for shunt converter of both the topologies [154]. The firing pulses are generated by employing hysteresis controllers for two-level structures and in-phase level shift multicarrier pulse width modulation for the three level diode clamped multilevel inverter structure.

2.4.1 Control Strategy of UPQC-2L

2.4.1.1 Control Strategy of Series Converter

The series converter has to mitigate the distortions from the source voltage in order to maintain distortion free load voltage at PCC. So it has to inject the voltage into the system through series transformer. The control block diagram of series converter is shown in Figure 2.17. In the *d-q* method [14], [155], the distorted source voltages (V_{sa}, V_{sb}, and V_{sc}) are sensed and transformed into the synchronous reference frame using

$$\begin{pmatrix} v_{sd} \\ v_{sq} \end{pmatrix} = T_{abc}^{dq} \begin{pmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{pmatrix} \tag{2.50}$$

Where T_{abc}^{dq} is the transformation matrix, is given in (2.2)

$$T_{abc}^{dq} = \frac{2}{3} \begin{pmatrix} \cos(\omega t) & \cos(\omega t - 120^0) & \cos(\omega t + 120^0) \\ -\sin(\omega t) & -\sin(\omega t - 120^0) & -\sin(\omega t + 120^0) \end{pmatrix} \tag{2.51}$$

The transformation angle (θ) represents the angular position of the reference frame, which is rotating at a constant speed in synchronism with the three-phase AC voltage. The source voltages are passed through the phase locked loop (PLL) block to obtain ωt which is used to transform three-phase quantities into synchronous reference frame coordinates.

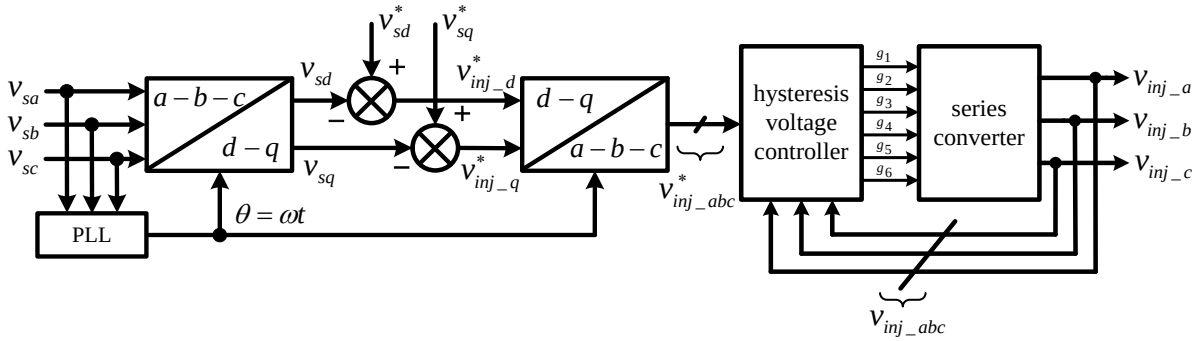


Fig. 2.17: Control strategy of series converter

To maintain the load voltage sinusoidal with a constant desirable magnitude, even if the source voltage is disturbed, the expected source voltage in the synchronous reference frame will have only one component, which is *d*-axis component and *q*-axis component will be zero. The reference compensating voltages in *d-q* reference frame are derived as

$$\begin{pmatrix} v_{inj\_d}^* \\ v_{inj\_q}^* \end{pmatrix} = \begin{pmatrix} v_{sd}^* \\ v_{sq}^* \end{pmatrix} - \begin{pmatrix} v_{sd} \\ v_{sq} \end{pmatrix} \tag{2.52}$$

The reference compensating voltages in (2.17) are transformed back into *a-b-c* reference frame by using transformation matrix T_{dq}^{abc}.

$$\begin{pmatrix} v_{inj\_a}^* \\ v_{inj\_b}^* \\ v_{inj\_c}^* \end{pmatrix} = T_{dq}^{abc} \begin{pmatrix} v_{inj\_d}^* \\ v_{inj\_q}^* \end{pmatrix} \tag{2.53}$$

$$T_{dq}^{abc} = \begin{pmatrix} \cos(\omega t) & -\sin(\omega t) \\ \cos(\omega t - 120^0) & -\sin(\omega t - 120^0) \\ \cos(\omega t + 120^0) & -\sin(\omega t + 120^0) \end{pmatrix} \tag{2.54}$$

The reference compensating voltages ($v^*_{inj\_a}, v^*_{inj\_b}, v^*_{inj\_c}$) and the actual compensating voltages injected by the series converter are processed through hysteresis voltage controller to generate the firing commands to the series converter such that the load voltage at PCC will be maintained at desired levels apart from the voltage sag or swell of supply voltage.

2.4.1.2 Control Strategy of Shunt Converter

The block diagram of control strategy of shunt converter is shown in Figure 2.18. The measured three-phase load currents are converted into synchronous *d-q* reference frame using (2.6)

$$\begin{pmatrix} i_{ld} \\ i_{lq} \end{pmatrix} = T^{dq}_{abc} \begin{pmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{pmatrix} \tag{2.55}$$

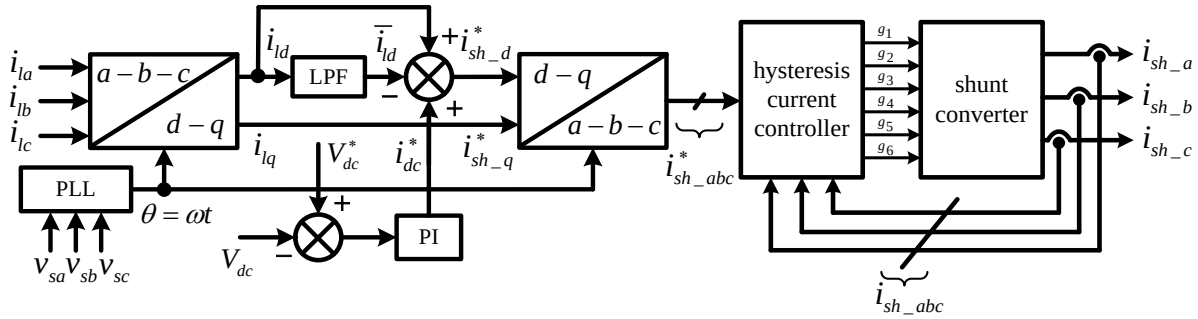


Fig. 2.18: Control strategy of shunt converter

By this transform, the fundamental positive-sequence component and all harmonic components are transformed into corresponding dc and ac quantities with a fundamental frequency shift respectively. Low-pass filters (LPF) can easily extract the fundamental positive-sequence component from the d-axis component of load current.

$$i_{ld} = \bar{i}_{ld} + \tilde{i}_{ld} \tag{2.56}$$

$$i_{lq} = \bar{i}_{lq} + \tilde{i}_{lq} \tag{2.57}$$

Where, $\bar{i}_{ld}$ and $\tilde{i}_{ld}$ are the dc and ac quantities of the active component of the load current (i_{ld}); $\bar{i}_{lq}$ and $\tilde{i}_{lq}$ are the dc and ac quantities of the reactive component of the load current (i_{lq}). If i_s is the source current, then the compensating current injected by the shunt converter (i_{sh}) is given as

$$i_{sh} = i_l - i_s \tag{2.58}$$

Hence *d-q* components of the shunt compensating current should be consists of all harmonic and reactive components

$$i_{sh\_d}^{*} = \tilde{i}_{ld} \tag{2.59}$$

$$i_{sh\_q}^{*} = i_{lq} \tag{2.60}$$

Consequently, the d-q components of the source current becomes,

$$i_{sd} = \overline{i}_{ld} \tag{2.61}$$

$$i_{sq} = 0 \tag{2.62}$$

This means that there are no harmonic and reactive components in the source current. The compensation characteristics of the UPQC depends on the dc-link voltage. The switching losses and other disturbances, such as the sudden variation of load affects the dc-link voltage. In order to regulate the dc-link capacitor voltage against disturbances, a proportional-integral (PI) controller is used, which is shown in Figure 2.18. The actual dc-link voltage (V_{dc}) is sensed and compared with the reference value (V_{dc}^{*}) and error is processed through the PI controller. The output from the PI controller (i_{dc}^{*}) is added to the *d*-axis component of the reference compensating current to generate the new reference current as follows:

$$i_{sh\_d}^{*} = \tilde{i}_{ld} + i_{dc}^{*} \tag{2.63}$$

$$i_{sh\_q}^{*} = i_{lq} \tag{2.64}$$

These reference currents in (2.28 and 2.29) are transformed back into a-b-c reference frame by using transformation matrix T_{dq}^{abc}.

$$\begin{pmatrix} i_{sh\_a}^{*} \\ i_{sh\_b}^{*} \\ i_{sh\_c}^{*} \end{pmatrix} = T_{dq}^{abc} \begin{pmatrix} i_{sh\_d}^{*} \\ i_{sh\_q}^{*} \end{pmatrix} \tag{2.65}$$

The hysteresis current based controller has been used to generate the firing pulses the switches of shunt converter by comparing the sensed actual shunt compensating currents ($i_{sh\_a}, i_{sh\_b}, i_{sh\_c}$) and computed reference source currents ($i_{sh\_a}^{*}, i_{sh\_b}^{*}, i_{sh\_c}^{*}$) as shown in Figure 2.18.

2.4.2 Control Strategy of UPQC-3L

The control strategy that is based on synchronous reference frame theory (*d-q* method) is employed for the UPQC with three-level structure is similar to the UPQC with two-level structure.

2.4.2.1 Control Strategy of Series Converter

The control strategy of series converter of UPQC with three-level structure is shown in Figure 2.19. The reference compensating voltages ($v_{inj\_a}^{*}, v_{inj\_b}^{*}, v_{inj\_c}^{*}$) are generated as

explained in the section 2.4.1.1 using (2.18). These derived reference voltages and the measured compensating voltages ($v_{inj\_a}, v_{inj\_b}, v_{inj\_c}$) are processed through the voltage controller to generate modulating signals ($v_{m\_a}, v_{m\_b}, v_{m\_c}$) for the three-phases of the series converter. The three-level pulse width modulation (PWM) is used to generate the firing commands to the switches of three-level diode clamped multilevel inverter [268]. The three-level PWM is based on IPD level shift modulation. The generation of firing pulses from this modulation technique is discussed in the section 2.2.1 and shown in Figure 2.13.

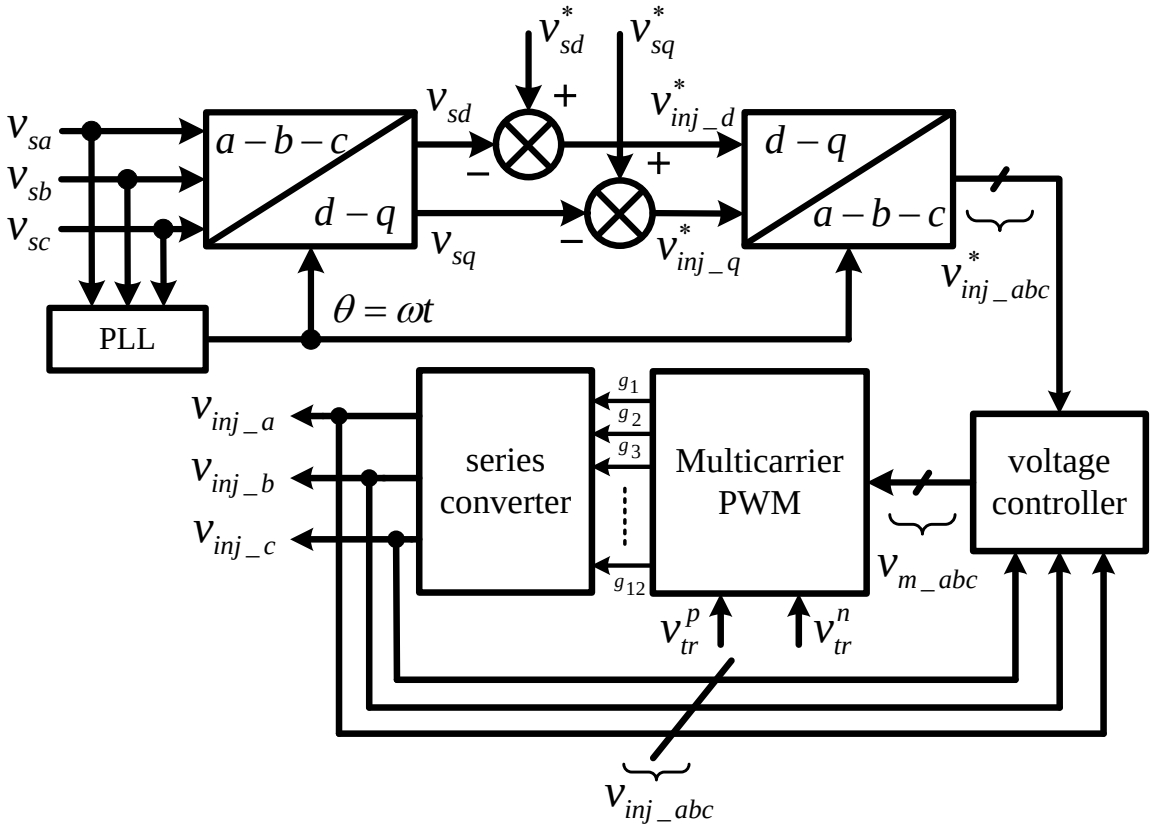


Fig. 2.19: Control strategy of series converter

2.4.2.2 Control Strategy of Shunt Converter

The control block diagram of shunt converter is shown in Figure 2.20. In this control strategy, the three-phase shunt compensating currents ($i^*_{sh\_a}, i^*_{sh\_b}, i^*_{sh\_c}$) are computed from (2.30), where the reference compensating currents in the synchronous reference frame are derived by using the active current component (i^*_{dc}) responsible for regulating split dc-link capacitor voltages. Figure 2.21, shows the block diagram of the dc-link voltage regulator. Despite from the two-level inverter structure, the three-level inverter will have split dc-link consisting of two equal capacitors C_{dcu} and C_{dcl} as shown in Figure 2.21(b). The voltages v_{dcu} and v_{dcl} across both the capacitors are sensed and processed through a summer and subtractor in order to evaluate the error by comparing with the references v^{ref1}_{dc} and v^{ref2}_{dc} respectively as shown in Figure 2.21(a). The error signals are processed through the

proportional-integral (PI) controllers separately and the output of the controllers is added to generate active current component (i_{dc}^{*}).

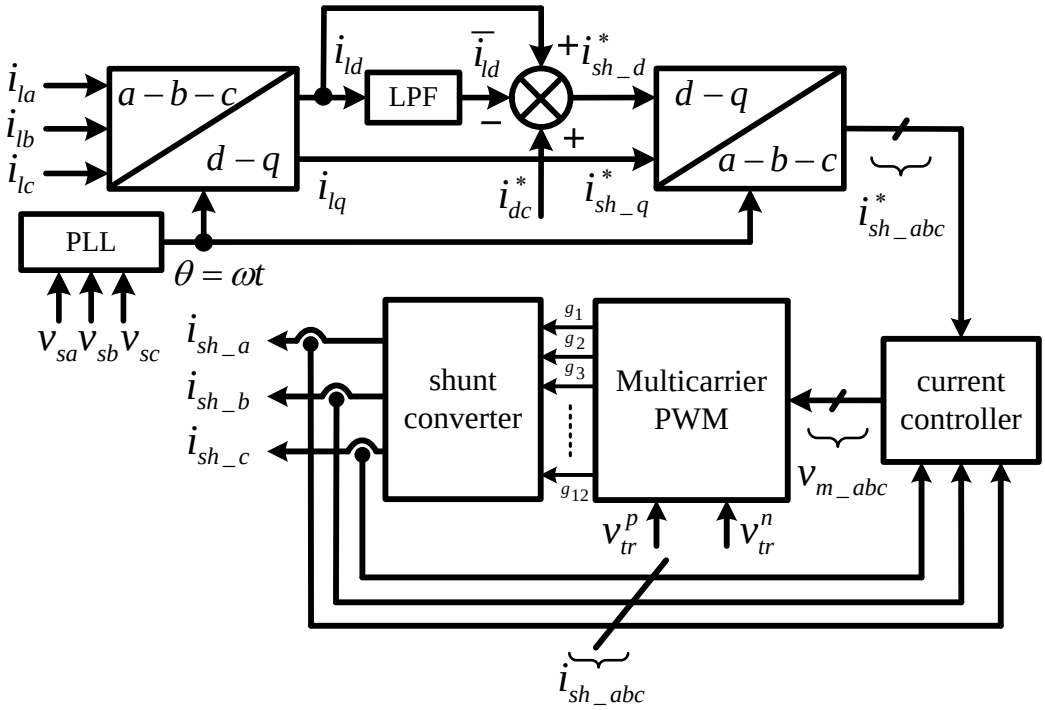


Fig. 2.20: Control strategy of shunt converter

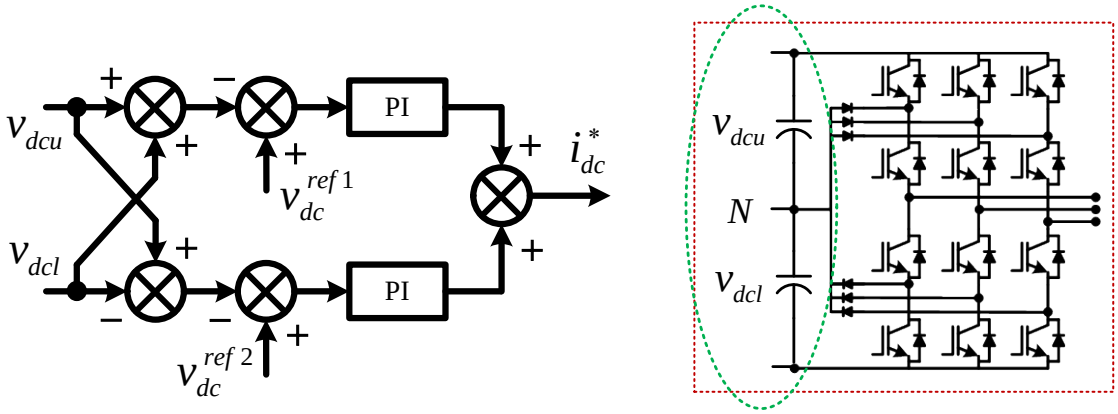


Fig. 2.21: Control strategy of shunt converter

The reference three-phase shunt compensating currents ($i_{sh\_a}^{*}, i_{sh\_b}^{*}, i_{sh\_c}^{*}$) and the sensed actual current signals ($i_{sh\_a}, i_{sh\_b}, i_{sh\_c}$) are processed through the comparator in order to generate the three modulating signals ($v_{m\_a}, v_{m\_b}, v_{m\_c}$) for the implementation of level shift modulation, which is explained in the previous section.

2.5 Simulation and Experimental Results of UPQC-2L and UPQC-3L

The performance of UPQC with two-level voltage source inverter and three-level neutral point multilevel inverter is tested with the load that is made of a combination of linear and nonlinear load. Simulation studies have been made under different utility and load

conditions to verify the performance of these topologies under same scale of parameters selected for topology structure, source and load. The linear load consists of three-phase balanced Y-connected RL load and the nonlinear load consists of three-phase diode rectifier fed RL-load. The parameters for the evaluation of the load and the system for the evaluation of the performance of both the configurations are given in Table 2.4. Both configurations are implemented in the environment of MATLAB Simulink and validated with the experimental setup, which is developed in the laboratory. The performance is evaluated with the balanced distorted source voltage, unbalanced source voltage, unbalanced distorted voltage, nonlinear load, 20% voltage sag and swell on three-phase source voltages and voltage flicker conditions. In order to study the steady-state and transient performance of UPQC-2L and UPQC-3L, the following events have been assumed to occur in the system for all simulation studies:

- At $t = 0.2$s, the voltage disturbance (voltage sag/swell etc.) is introduced into the supply system.
- At $t = 0.3$s, the voltage disturbance (voltage sag/swell etc.) is removed from the source supply system.

The simulation results are presented below for both linear and non-linear loading conditions.

Table 2.4: System parameters under evaluation

Description	Parameter value
Three-phase source voltage	200V (L–L rms)
Supply frequency	50Hz
DC-link voltage	330V
DC-link capacitance (2-level)	1500μF
DC-link capacitance (3-level)	1500*2μF
Shunt resistance, coupling inductance	0.1Ω, 50mH
Series resistance and filter components	0.1Ω, 8mH and 5μF
Three-phase diode rectifier fed RL load	60Ω, 30mH
Three-phase RL load-1 (star connected)	110Ω, 30mH
Three-phase RL load-2 (star connected)	18Ω, 44mH

The simulation studies are carried out at the three-phase line voltage of 200V for both UPQC topologies and to investigate the validity of the simulation results, a prototype of UPQC with two-level and three-level VSI are developed in the laboratory. Though the UPQC-

3L can be tested at higher voltage levels than 200V as multilevel structure can be opted for medium voltage and high power applications, the supply voltage level is chosen as low as 200V due to the limitations of the developed laboratory experimental setup. The system hardware, Opal-RT 5400 interfacing and the development of experimental prototype of UPQC-2L and UPQC-3L are presented in the Appendix-*A*. The experimental setup requires various components such as IGBT switch modules, gate driver circuits, snubber circuits, clamping diodes for three-level NPC, Opal-RT control board, voltage and current transducers, series injection transformer consists of 3 single-phase transformers, coupling inductor, LC filters, pulse isolation and amplification circuits, dead bands, programmable source, dc-link capacitors, dc power supplies etc. The experimental prototype and schematic diagram of experimental setup along with control part is discussed in the Appendix-A. The distorted supply is created by the use of programmable AC voltage source. The details of this source generator is given in the Appendix-A.

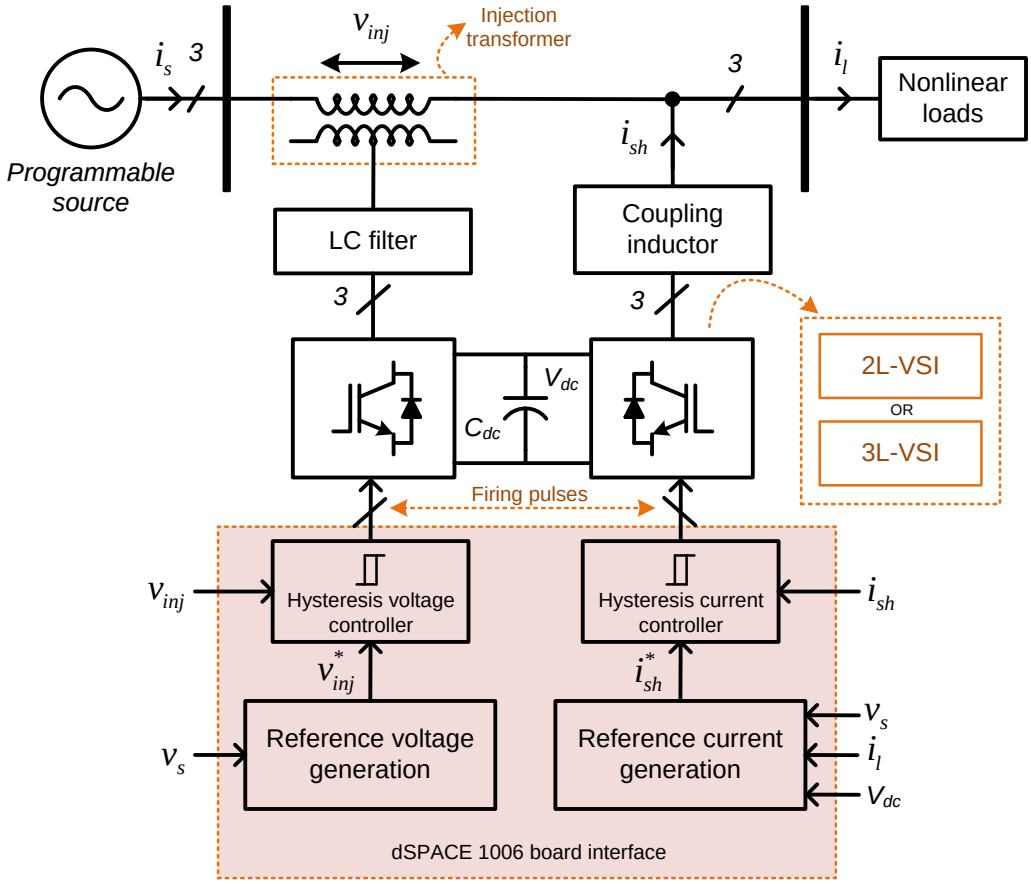


Fig. 2.22: Block diagram of system topology under evaluation

The block diagram of UPQC under evaluation is shown in Figure 2.22, where the sensed voltage and current signals are processed through Opal-RT control board with the help of ADC and DACs. The control strategy, which is explained in the previous sections, is processed in the host computer through MATLAB Simulink to generate the firing commands to the IGBT switch modules of the series and shunt VSIs. The dc link between series and

shunt converters consists of single dc-link capacitor for UPQC-2L, whereas two dc-link capacitors connected in series for UPQC-3L structure. In the experimental work, to record the waveforms a digital storage oscilloscope (DSO) Agilent DSO1014A is used. To analyse the harmonic spectrum and to measure THDs of voltage and current signals, Fluke 434 power quality analyser is used.

2.5.1 Case-1: Distorted Source and Non-linear Load

The uncontrolled diode bridge rectifier with RL elements has been considered as three-phase non-linear load. The parameters of this load are given in Table 2.4. Figure 2.23 shows the circuit configuration of uncontrolled bridge rectifier with RL load.

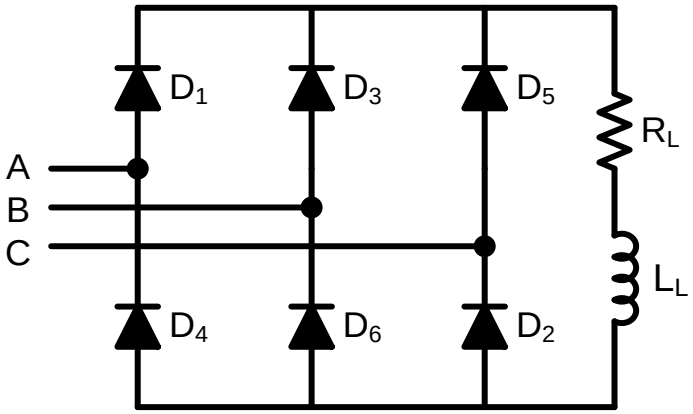


Fig. 2.23: Uncontrolled bridge rectifier with RL load

As discussed in the previous chapter, the shunt converter part of UPQC will be actively participate to compensate the non-linear load current harmonics, while the series converter has no role to support the compensation in this case. In case of distorted supply voltage, the series converters plays main role to compensate the distorted voltage to maintain load voltage at PCC with desired magnitude and sinusoidal. The distorted supply voltage is created with by adding the most dominant harmonic voltages to the fundamental voltage waveform, such as 5th, 7th, 11th, and 13th harmonics with corresponding magnitudes of 1/5th, 1/7th, 1/11th, and 1/13th magnitude of fundamental value. In this thesis, the simulation and experimental results are shown for the shunt and series converter parts separately for both topologies of UPQC-2L and 3L.

(A) UPQC-2L

The simulation results of UPQC-2L compensation characteristics are shown in Figure 2.24 and 2.25, Figure 2.24 shows the simulation results of voltage compensation with UPQC-2L, where, the quantities are shown as follows (from top to bottom): axis-1: three-phase source voltages (v_{s_abc}), axis-2: three-phase series injected voltages (v_{inj_abc}), axis-3: three-phase load voltages at PCC (v_{L_abc}). From Figure 2.24, the following observations can be made:

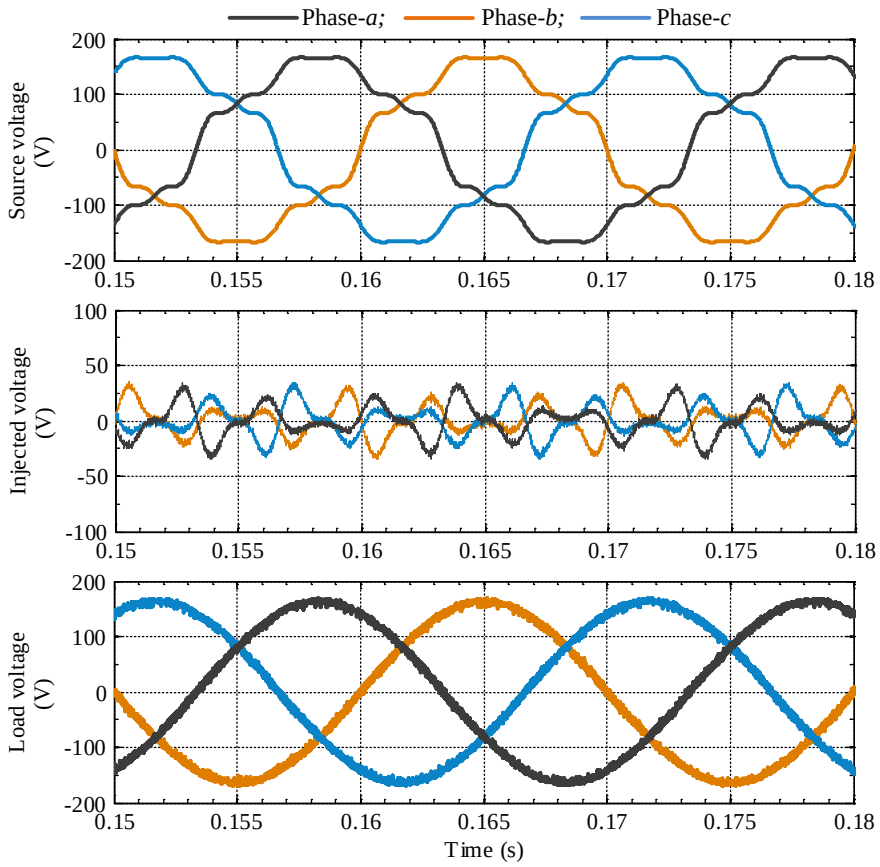


Fig. 2.24: Voltage compensation characteristics by shunt converter of UPQC-2L

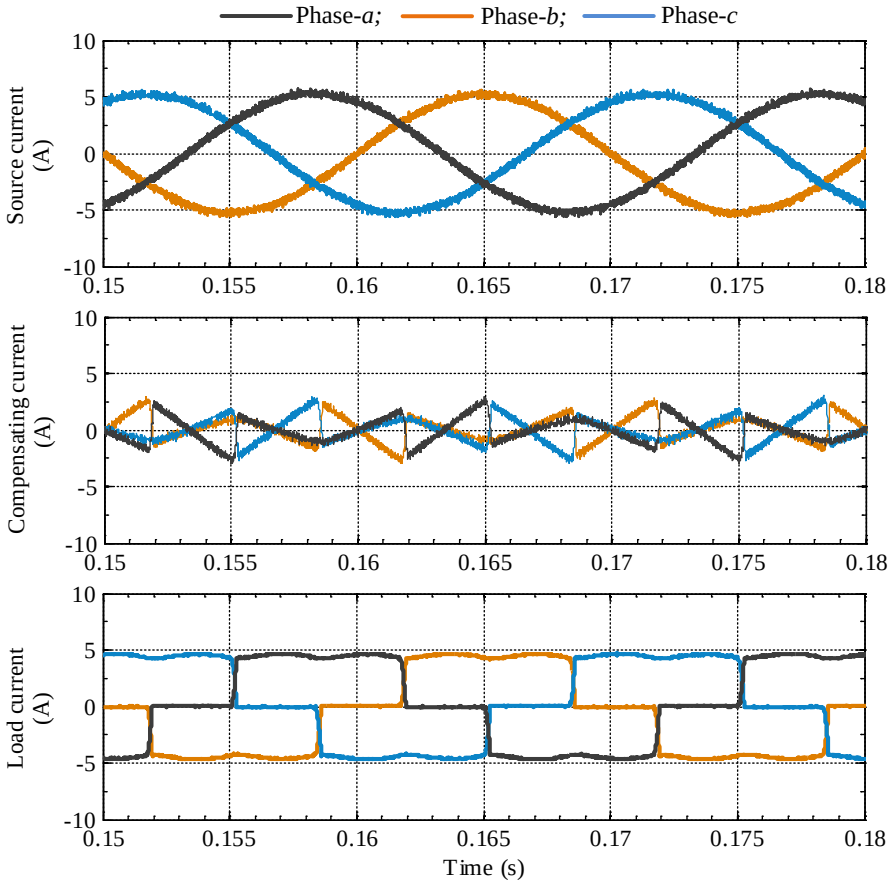
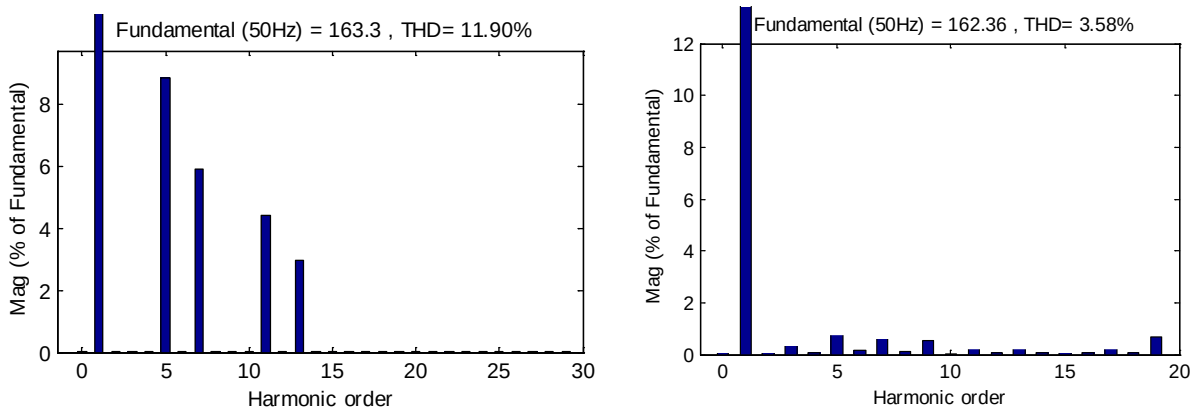
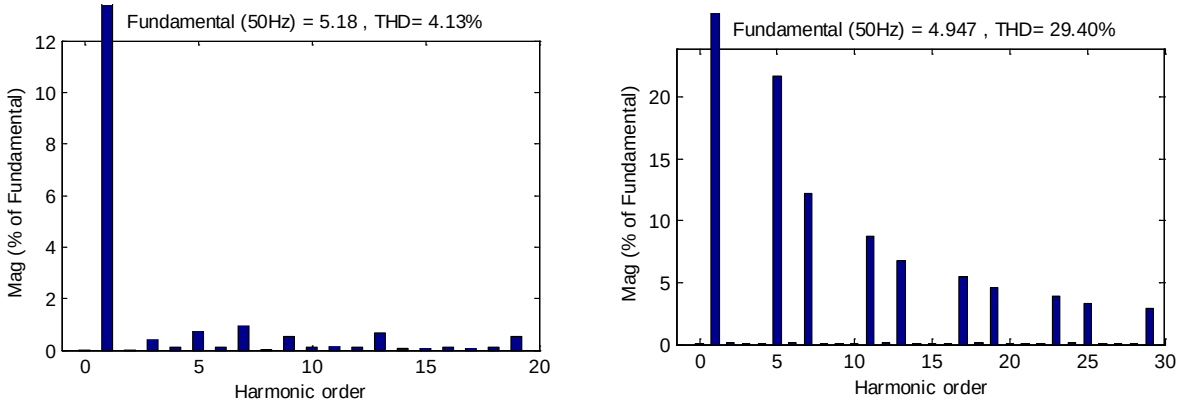


Fig. 2.25: Current compensation characteristics by shunt converter of UPQC-2L



(a) (b)

Fig. 2.26: FFT analysis of phase-*a* of (a) source voltage; (b) load voltage



(a) (b)

Fig. 2.27: FFT analysis of phase-*a* of (a) source current; (b) load current

1. If UPQC is not connected into the system, the load voltage at PCC will be same as that of distorted source voltage, which is not sinusoidal. The THD of the source/load voltage in this case is 12.43%.
2. The UPQC injects the compensating voltages (axis-2) in series with supply voltages to maintain load voltage free from the harmonics induced in the source voltages and maintain the load voltage at desired voltage magnitude. Such that the load voltage possess THD of 3.12% with 162.3V peak fundamental value of phase magnitude.

Figure 2.25 shows the simulation results of current compensation against non-linear load, where the quantities are shown as follows (from top to bottom): axis-1: three-phase source currents (i_s), axis-2: three-phase compensating currents (i_{sh}), axis-3: three-phase non-linear load currents (i_L). From Figure 2.25, the following observations can be made:

1. If UPQC is not connected into the system, the source current will be same as that of the load current, which is not sinusoidal. The THD of the load current/source current in this case is 18.54%.
2. The UPQC injects the shunt compensating current (axis-2) in parallel to the PCC, such that the source current becomes sinusoidal and the THD is reduced

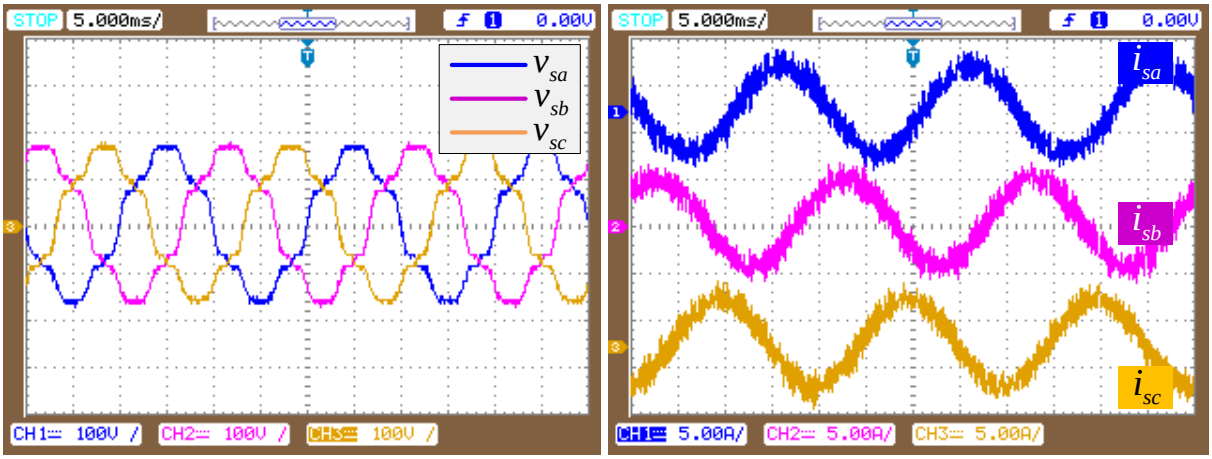
to 4.26% which is well within the limits of IEEE–519–1992 recommended value of 5%, where as the load current possess 18.54%.

3. The rms value of the load current is 3.58A, and that of the source current is 3.62A. The enhancement in the source currents is due to the compensation of real power losses of the inverter.

To validate the simulation results, experimental investigation is performed at the same scale of source voltage used for the simulations. The DSO scope results are presented to justify the simulation results as follows.

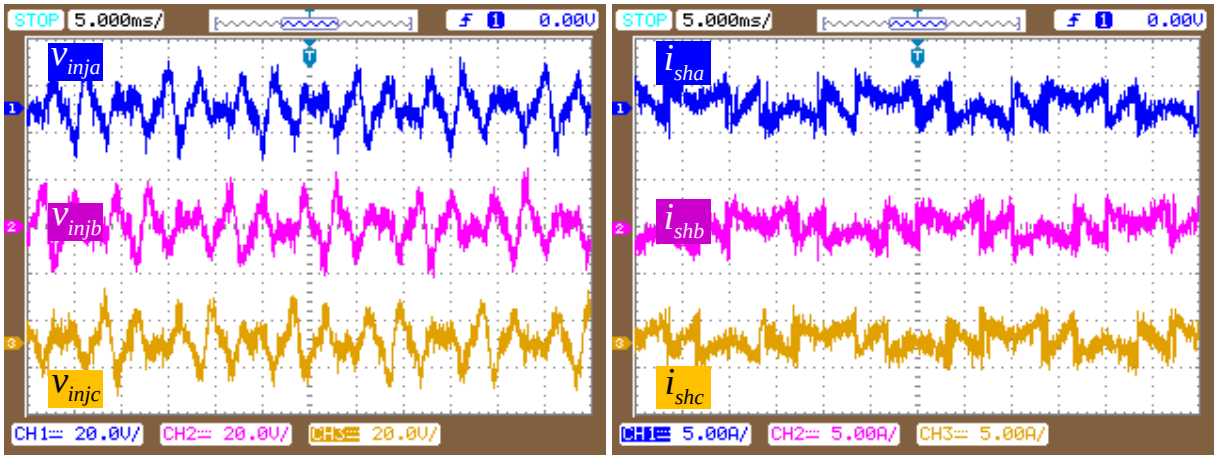
Figure 2.28 to 2.30 shows the experimental scope results of distorted source voltage and non-linear load current compensation. Figures 2.28(a), 2.29(a) and 2.30(a) shows the three-phase voltage compensation characteristics by the series converter part of UPQC to validate simulation results shown in Figure 2.24. The scope traces shows the phase voltage waveforms.

Similarly Figures 2.28(b), 2.29(b) and 2.30(b) shows the current compensation characteristics by the shunt converter part of the UPQC to validate corresponding simulation results shown in Figure 2.25. The compensated load voltage, which is shown in Figure 2.30(a) is having THD of 5.6%, while the generated source voltage is having 12.43%. The phase peak fundamental value of the load voltage is 162.4V, while the desired magnitude of reference load voltage is considered as 163.3V. The compensated source current is shown in Figure 2.26(b), It is having THD of 4.5%, while the load current, which is shown in Figure 2.30(b) is having 18.55%. The rms value of the source current is 3.88A, while load current is 3.42A. It is observed that the rms value of source current is slightly greater than the load current magnitude. The enhancement in the source currents is due to the compensation of active power losses of the inverters. The harmonic spectrum of voltages and currents are shown in Figures 2.26 to 2.27 for simulation study and in Figure 2.31 and 2.32 for experiment.



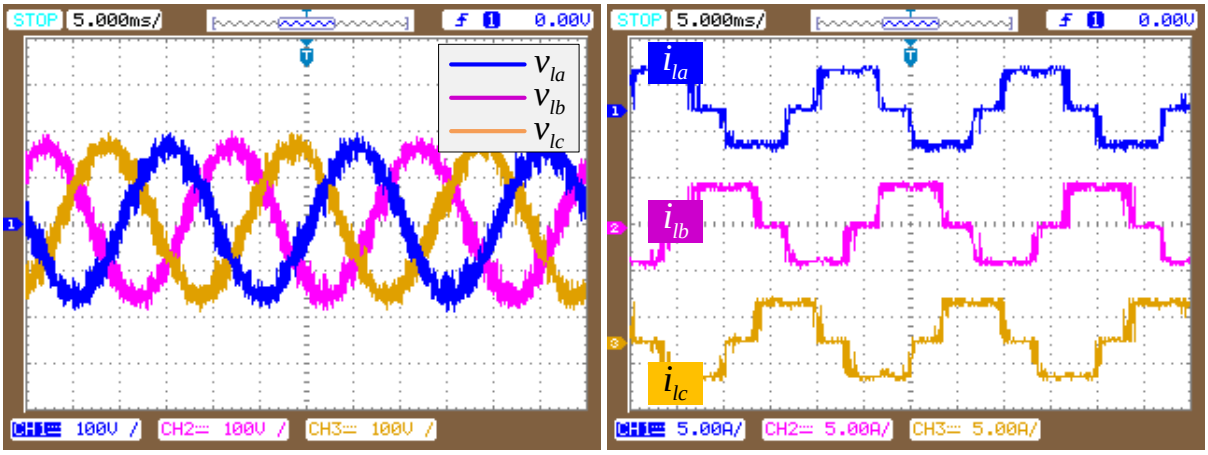
(a) (b)

Fig. 2.28: (a). Three-phase source voltages and (b). Source currents for case-1 in UPQC-2L



(a) (b)

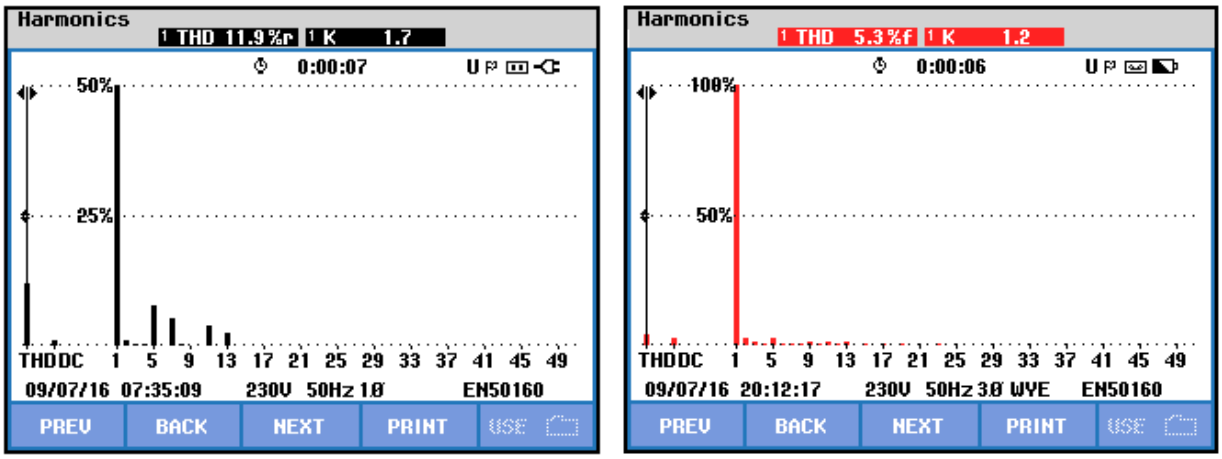
Fig. 2.29: (a). Three-phase series injected voltages and (b). Shunt compensating currents for case-1 in UPQC-2L



(a) (b)

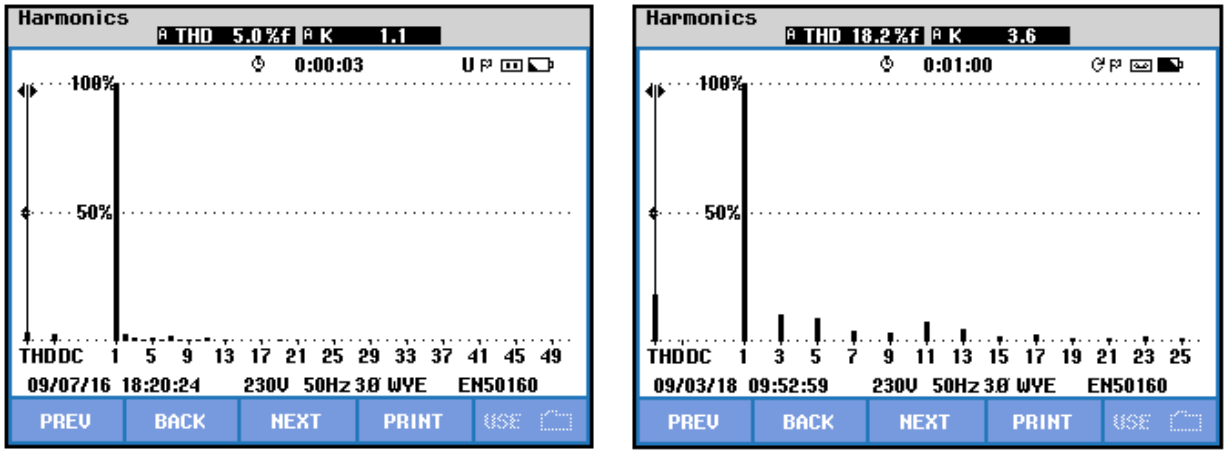
Fig. 2.30: (a). Three-phase load voltages and (b). load currents for case-1 in UPQC-2L

The profile of dc-link voltage is recorded and shown in Figures 2.33 and 2.34 for simulation and experimental work respectively. The required dc-link voltage is selected as designed in (2.5).



(a) (b)

Fig. 2.31: Harmonic spectrum of phase-*a* of (a) source voltage; (b) load voltage



(a) (b)

Fig. 2.32: Harmonic spectrum of phase-*a* of (a) source current; (b) load current

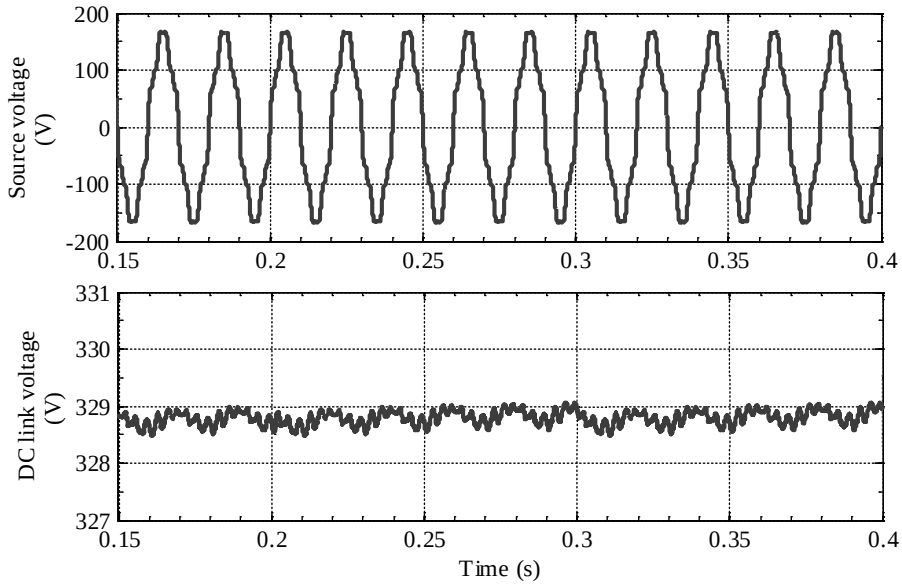


Fig. 2.33: Simulation results showing dc-link voltage variation during case-1 with UPQC-2L

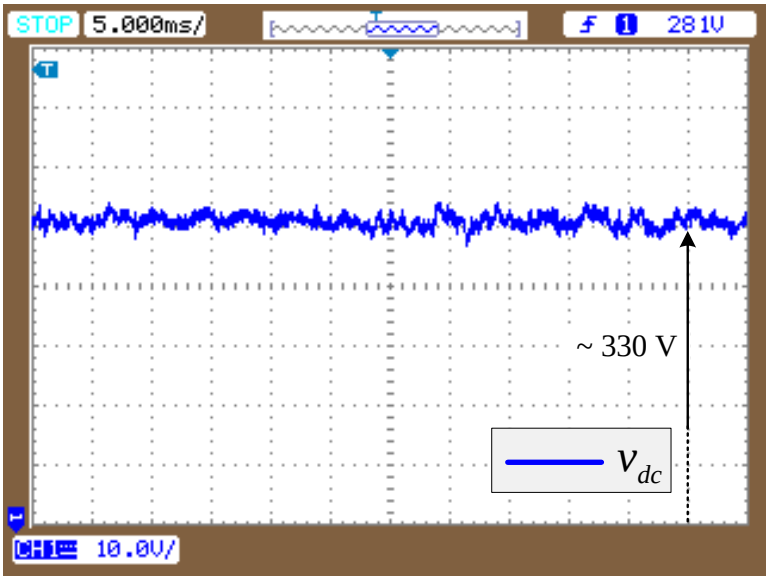


Fig. 2.34: Experimental results showing the dc-link voltage variation during case-1 with UPQC-2L

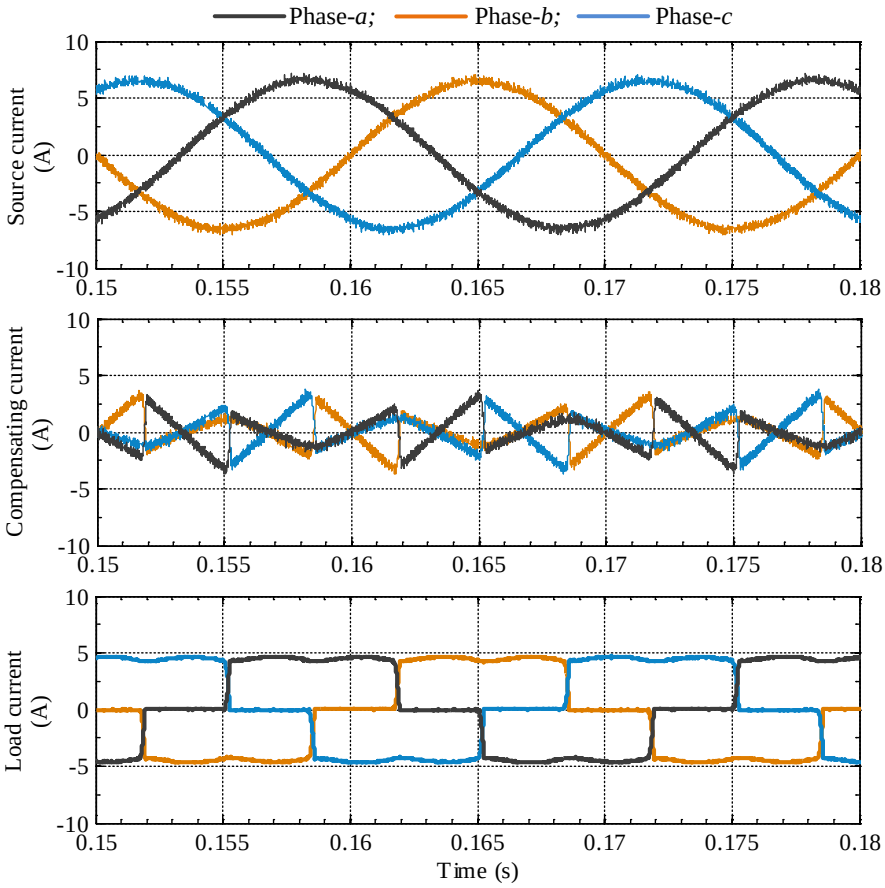


Fig. 2.35: Current compensation characteristics by shunt converter of UPQC-3L

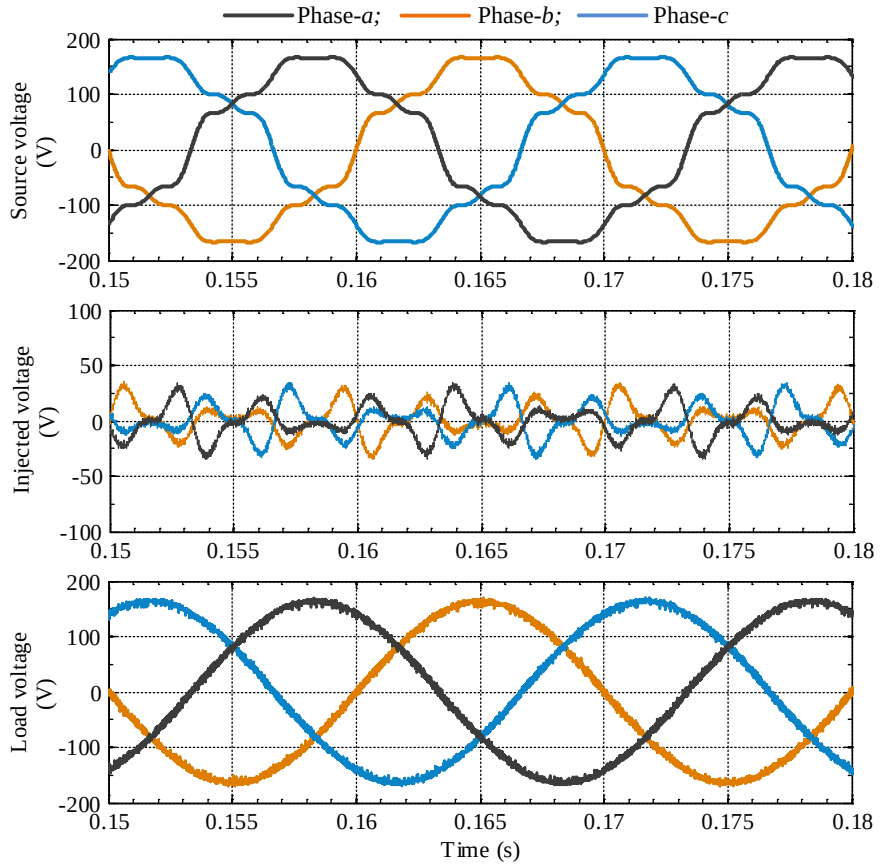


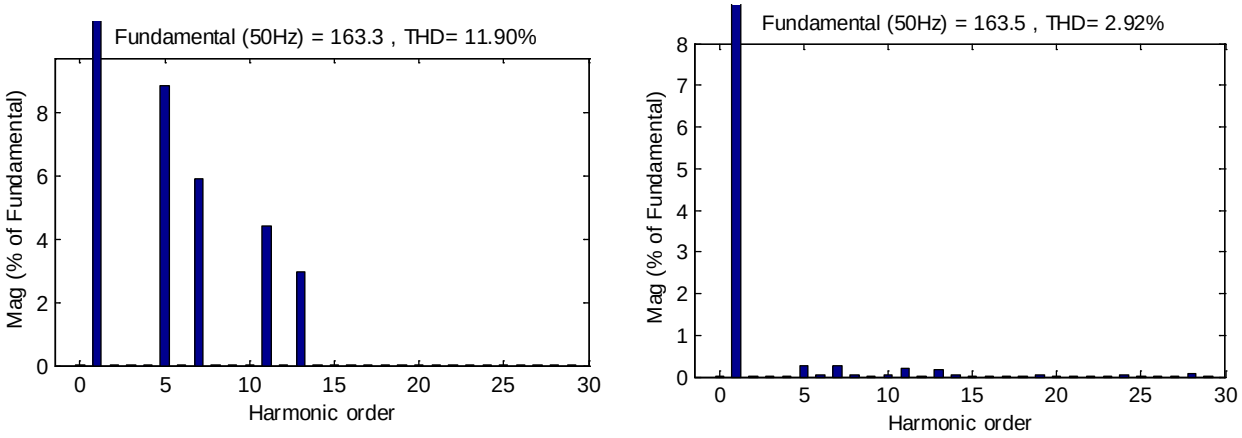
Fig. 2.36: Voltage compensation characteristics by shunt converter of UPQC-3L

The simulation results shows that UPQC is able to maintain the dc-link voltage at an average value of 328.8V, while in experimental scope results shows approximately 329.5V. On comparing the simulation results with the experimental scope results, it can be concluded that experimental results are in good agreement with simulation results.

(B) UPQC-3L

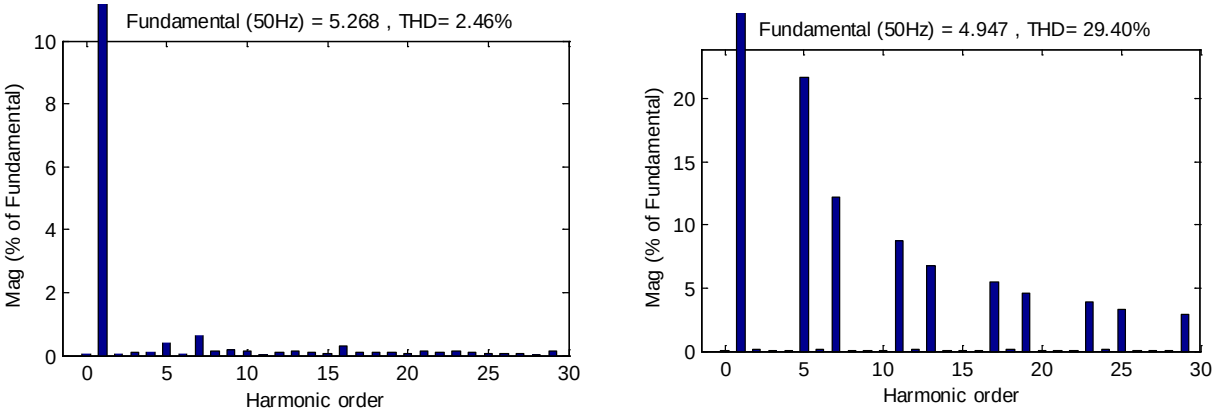
The simulation results of UPQC-3L compensation characteristics are shown in Figures 2.35 and 2.36, Figure 2.35 shows the simulation results of voltage compensation with UPQC-3L, where, the quantities are shown as follows (from top to bottom): axis-1: three-phase source voltages (v_{s_abc}), axis-2: three-phase series injected voltages (v_{inj_abc}), axis-3: three-phase load voltages at PCC (v_{L_abc}). From Figure 2.35, the following observations can be made. The simulation results shows that UPQC-3L injects the compensating voltages (axis-2) the load voltage at PCC is maintained at phase peak fundamental voltage magnitude of 163.0V. Such that the load voltage possess THD of 2.97% while the source voltage is having 12.40%.

Figure 2.36 shows the simulation results of current compensation against non-linear load, where the quantities are shown as follows (from top to bottom): axis-1: three-phase source currents (i_s), axis-2: three-phase compensating currents (i_{sh}), axis-3: three-phase non-linear load currents (i_L). From Figure 2.36, the following observations can be made. The UPQC injects the shunt compensating current (axis-2) in parallel to the PCC, such that the source current becomes sinusoidal and the THD is reduced to 2.44% which is well within the limits of IEEE–519–1992 recommended value of 5%, where as the load current possess 18.55%. The rms value of the load current is 3.56A, and that of the source current is 3.78A. The enhancement in the source currents is due to the compensation of real power losses of the inverter. Figures 2.39(a) to 2.41(a) shows the experimental scope results regarding to the three-phase voltage compensation characteristics by the series converter part of UPQC-3L to validate simulation results shown in Figure 2.35.



(a) (b)

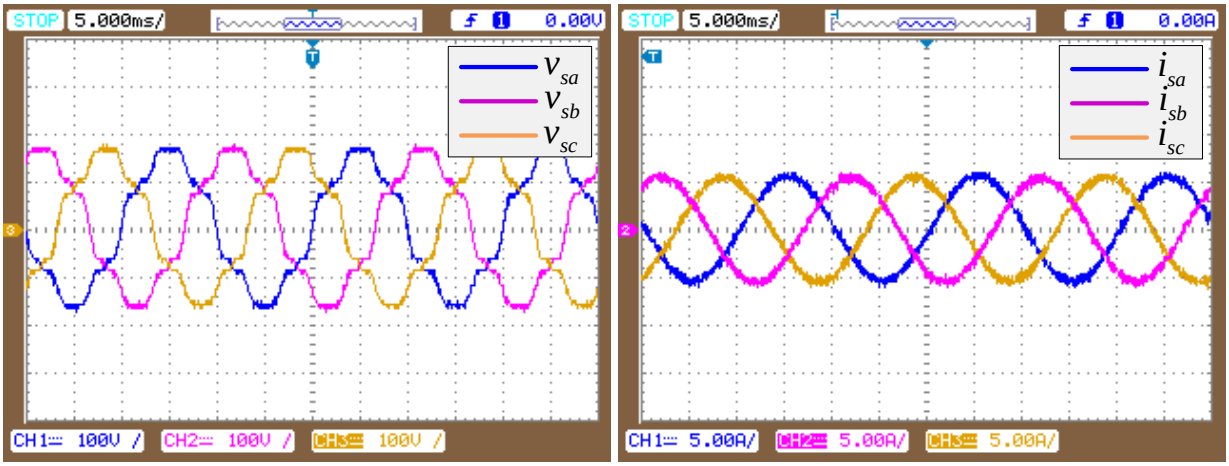
Fig. 2.37: FFT analysis of phase-*a* of (a) source voltage; (b) load voltage



(a) (b)

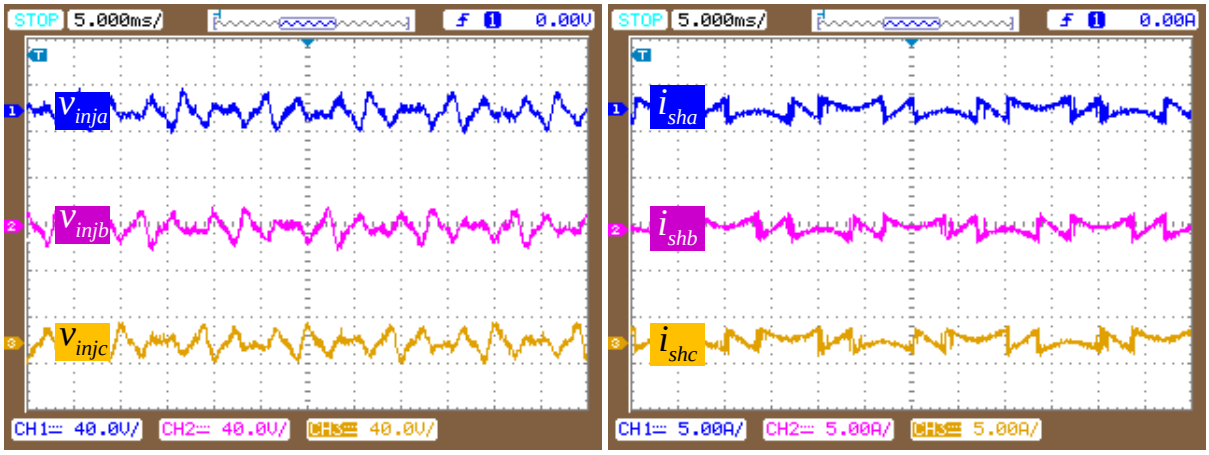
Fig. 2.38: Harmonic spectrum of phase-*a* of (a) source current; (b) load current

The experimental scope traces shows the phase voltage waveforms. Similarly from Figures 2.39(b) to 2.41(b) shows the current compensation characteristics by the shunt converter part of the UPQC-3L to validate corresponding simulation results shown in Figure 2.36.



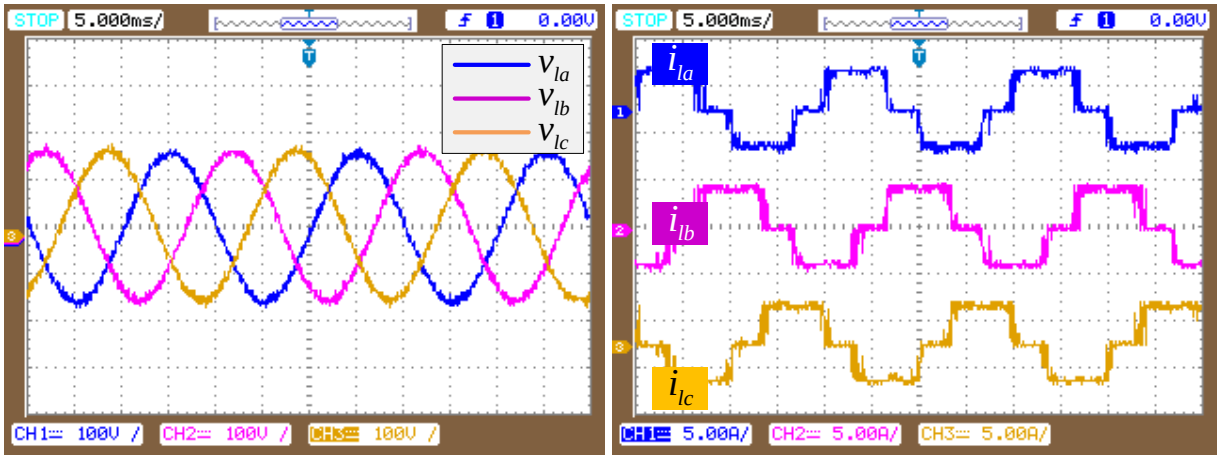
(a) (b)

Fig. 2.39: (a). Three-phase source voltages and (b). Source currents for case-1 with UPQC-3L



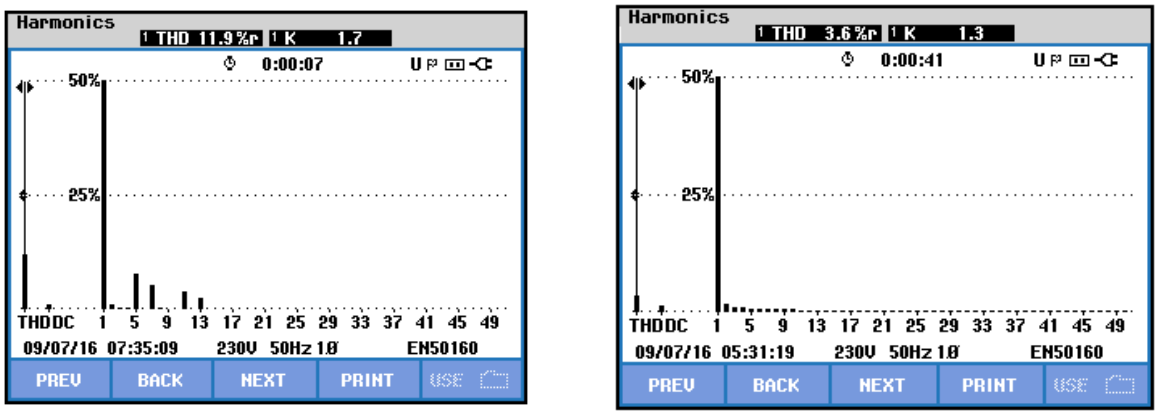
(a) (b)

Fig. 2.40: (a). Three-phase series injected voltages and (b). Shunt compensating currents for case-1 with UPQC-3L



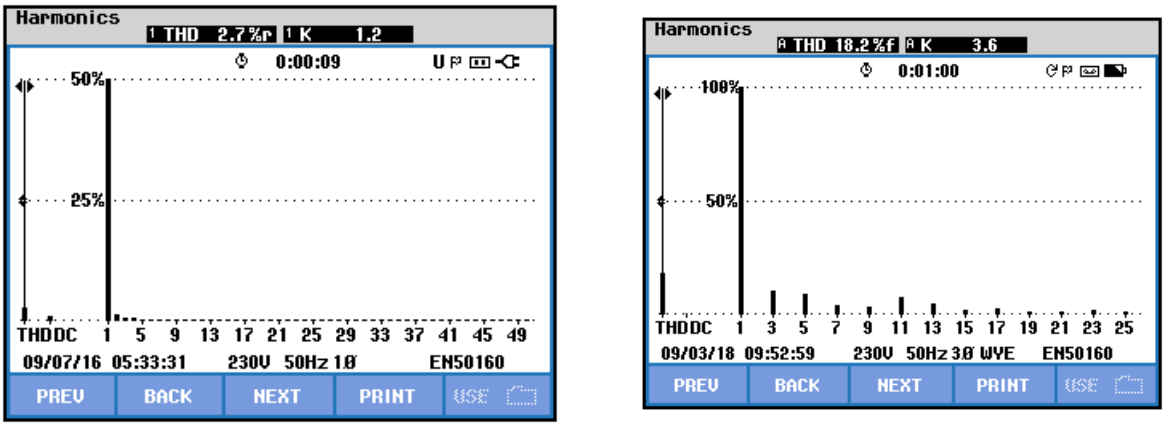
(a) (b)

Fig. 2.41: (a). Three-phase load voltages and (b). load currents for case-1 with UPQC-3L



(a) (b)

Fig. 2.42: Harmonic spectrum of phase-*a* of (a) source voltage; (b) load voltage



(a) (b)

Fig. 2.43: Harmonic spectrum of phase-*a* of (a) source current; (b) load current

The compensated load voltage, which is shown in Figure 2.41(a) is having THD of 3.6%, while the generated source voltage is having 2.97%. The phase fundamental peak value of the load voltage is 163.1V, while the desired magnitude of reference load voltage is considered as 163.3V. The compensated source current is shown in Figure 2.39(b), is having THD of 2.44%, while the load current, which is shown in Figure 2.41(b) is having 18.55%.

Figures 2.37 and 2.38 shows the harmonic spectrum of voltages and currents for simulation study and Figures 2.42 and 2.43 for experiment.

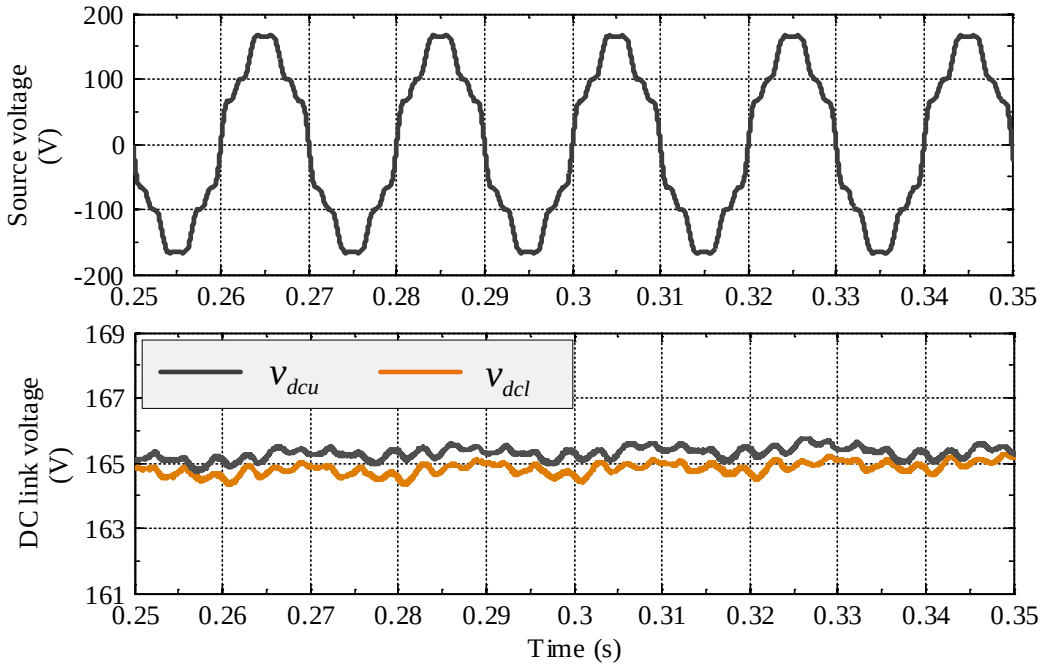


Fig. 2.44: Simulation results showing the dc-link voltage variation during case-1 with UPQC-3L

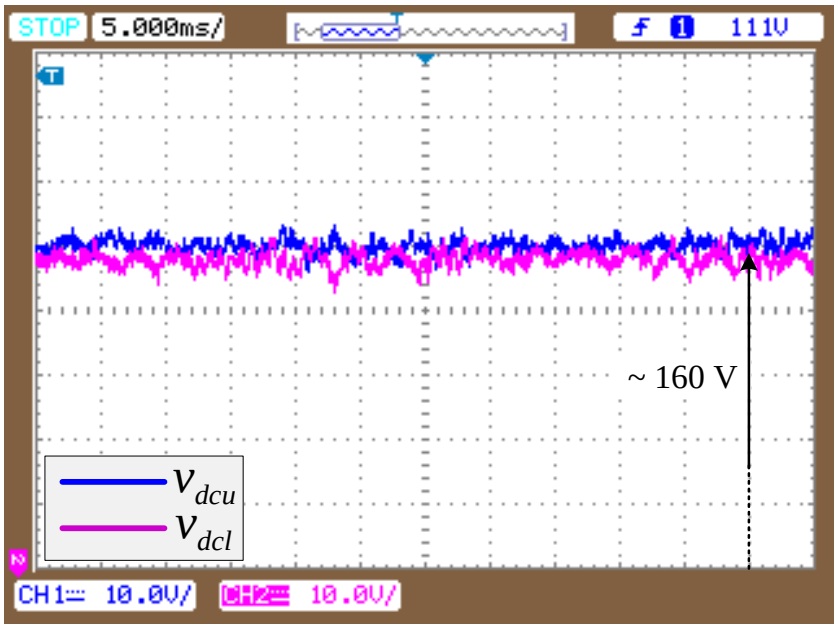


Fig. 2.45: Experimental results showing the dc-link voltage variation during case-1 with UPQC-3L

The profile of dc-link voltage is recorded and shown in Figures 2.44 and 2.45 for simulation and experimental work respectively. The required dc-link voltage is selected as designed in (2.5). The simulation results shows that UPQC is able to maintain the dc-link voltage at an average value of 165.5V and 164.8V on upper and lower dc-link capacitors

respectively, while in experimental scope results shows approximately 160V and 159V on upper and lower capacitors respectively.

(C) Summary

The quantitative comparison between UPQC-2L and UPQC-3L for this case study is given in Table 2.5, where the percentage THD values of experiment are considered for the comparison. The THDs are corresponding to the load voltage at PCC and source current of phase-*a.* From this comparison, it can be concluded that the compensating performance of UPQC-3L is better than UPQC-2L.

Table 2.5: THD Comparison between UPQC-2L and UPQC-3L with distorted source and non-linear load compensation

Type of disturbance (Voltage distortion)	**UPQC-2L**		**UPQC-ML**	
	Load voltage (%)	Source current (%)	Load voltage (%)	Source current (%)
Before compensation	12.40	18.55	12.40	18.55
After compensation	4.81	4.26	2.97	2.44

2.5.2 Case-2: Voltage Sag Compensation under Non-linear Load

The performance of the UPQC-2L and 3L is analysed with the voltage sag condition. The voltage sag is created in with 20% voltage dip in the source voltage from the nominal phase voltage of 115V.

(A) UPQC-2L

Figure 2.46 shows the voltage compensation characteristics under voltage sag condition. The series injected voltage (axis-2) is approximately zero for the normal conditions of the source voltage. When the voltage sag is introduced in the source voltage at $t = 0.2$s, series converter immediately responded and start injecting missing peak phase fundamental voltage magnitude of 32.5V in same phase of the source voltage to lift up the load voltage to the desired peak fundamental voltage magnitude of 163.3V at PCC. However, the UPQC-2L performed to maintain the load voltage at 163.2V. Such that the magnitude of the load voltage is maintained constant irrespective of the voltage sag in supply side. At $t = 0.3$s, the source voltage sag is returned to normal, so the injected voltage becomes zero. Figure 2.47 shows the current compensation characteristics by the shunt converter part. Apart from the voltage sag on the source voltage, to investigate the performance of UPQC, the load is selected as non-linear. The compensation of source current is similar to the previous case before sag occurrence. However when the voltage sag occurs on source voltage, the current drawn by the shunt converter increases such that the source rms current magnitude

increases from 3.62A to 3.71A. The increment in the source current is due to the support offered to the series converter by the shunt converter to provide sufficient active power to compensate the voltage sag on the system. Since the control scheme opted for evaluating the performance of the UPQC-2L is based on compensation concept of UPQC-P, where series converter injects active power to compensate the voltage disturbances arrived from the source voltage. However the percentage THDs of the source current and load voltages are of same as that of case-1. The experimental scope results are shown in Figures 2.48 to 2.50 for the corresponding simulation results. Figure 2.48(a) to 2.50(a) shows the three-phase voltage compensation characteristics by the series converter part of UPQC-2L to validate simulation results shown in Figure 2.46. Similarly Figure 2.48(b) to 2.50(b) shows the current compensation characteristics by the shunt converter part of the UPQC-2L to validate corresponding simulation results shown in Figure 2.47. The compensated load voltage, which is shown in Figure 2.50(a) is having the phase peak fundamental value of the load voltage is 160.0V during source voltage sag condition. The compensated source current is shown in Figure 2.48(b), is having THD of 4.21%, while the load current, which is shown in Figure 2.50(b) having 18.55%. The rms value of the source current is 3.64A under normal operating condition and 3.80A under voltage sag condition. The profile of dc-link voltage is shown in Figure 2.51 and 2.52 respectively for simulation and experimental work.

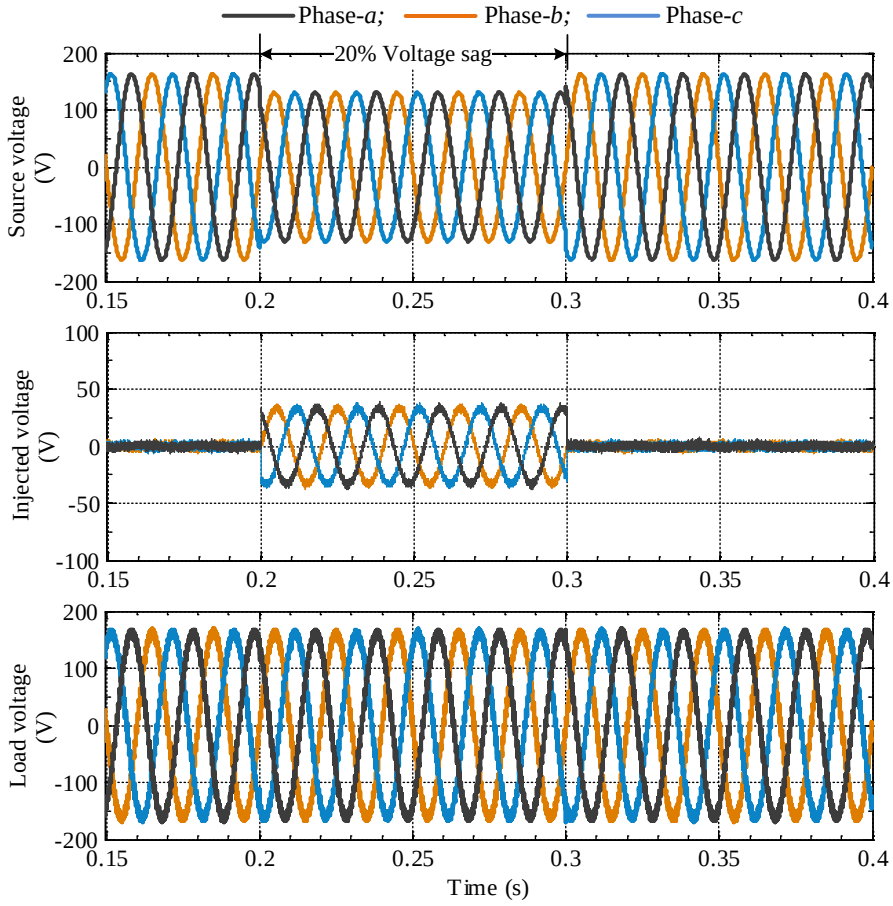


Fig. 2.46: Voltage compensation characteristics by shunt converter of UPQC-2L

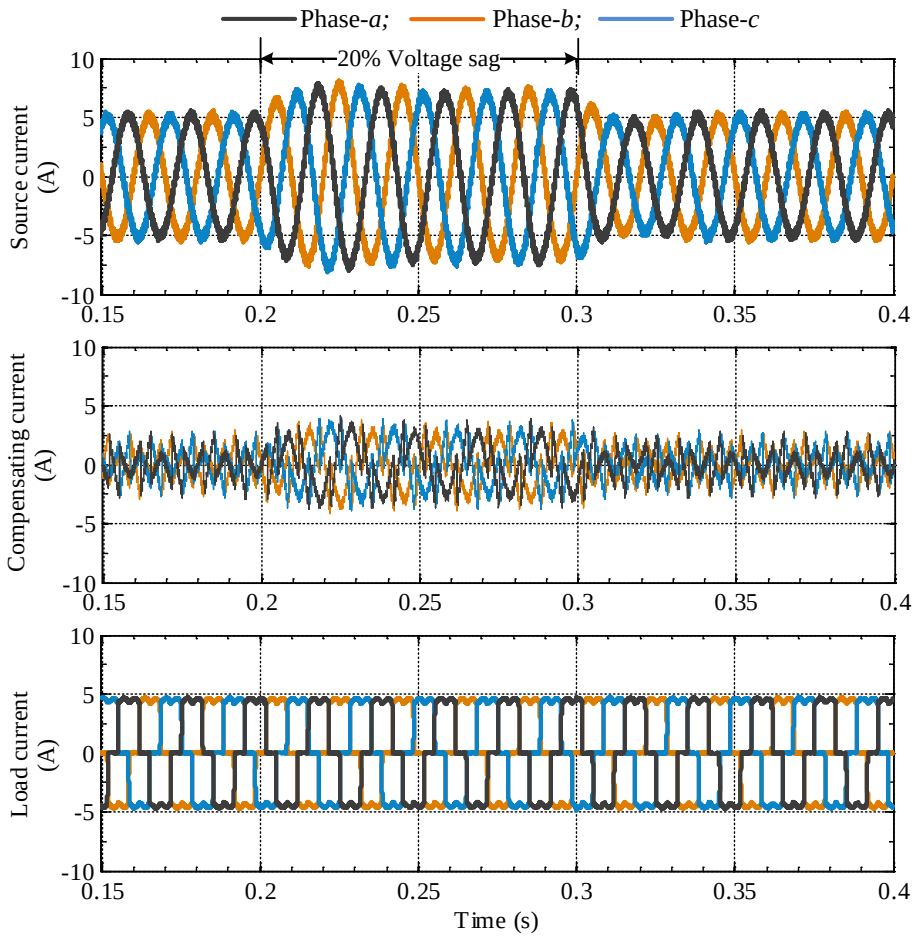
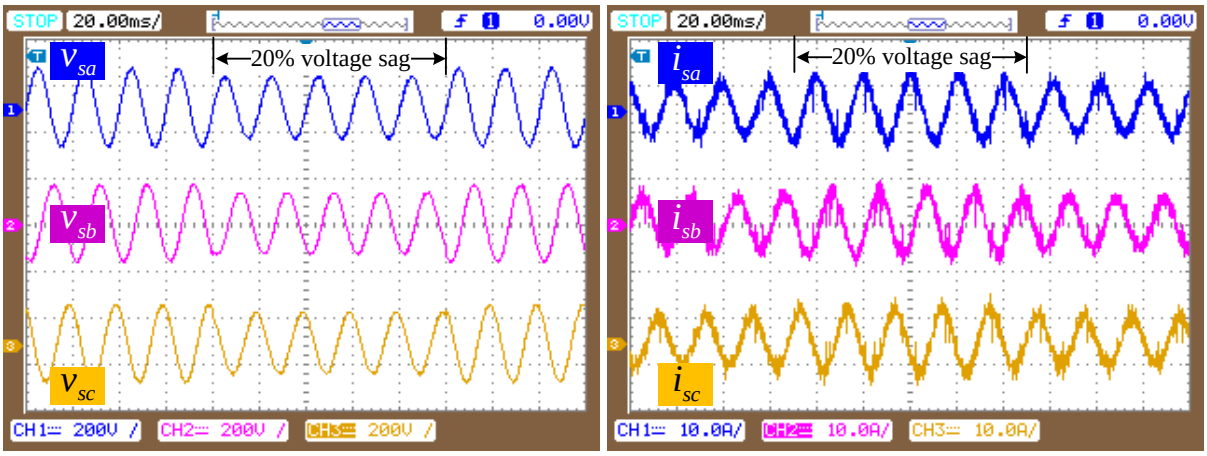


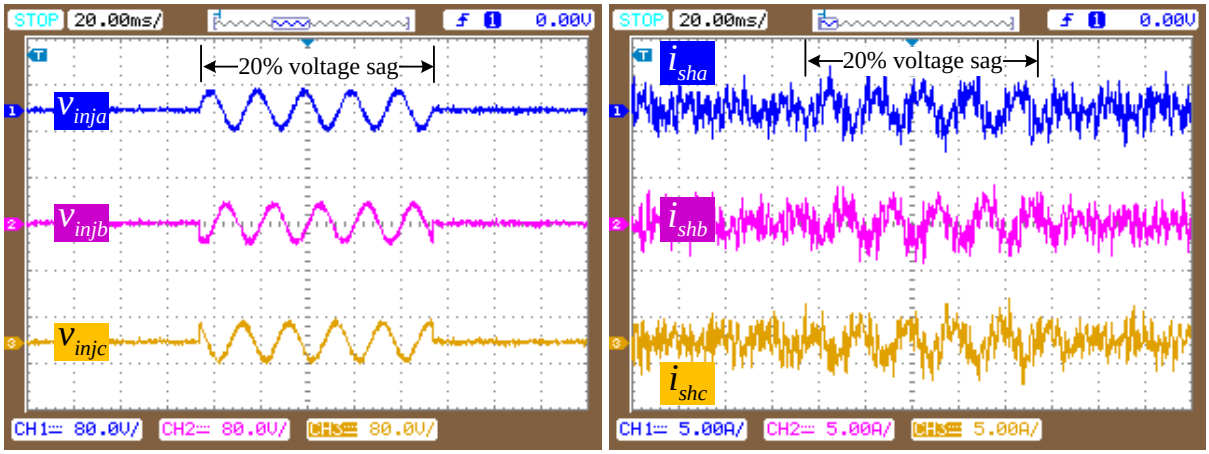
Fig. 2.47: Current compensation characteristics by shunt converter of UPQC-2L

The reference dc-link voltage is selected as 330V, whereas in simulation, the voltage across dc-link capacitor is maintained at an average value of 330V with negligible fluctuations around this value; however, the fluctuation is about 0.5% in experiment results. At the time of sag occurrence in the system, a sudden dip in the voltage magnitude from the nominal dc-link voltage in both simulation and experimental scope results can be overserved. The reason can be explained as follows.



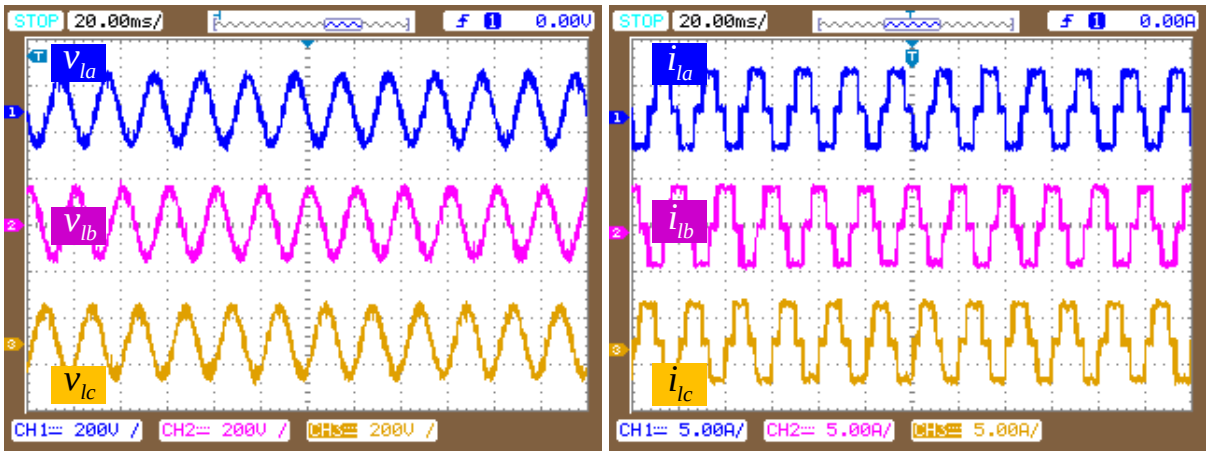
(a) (b)

Fig. 2.48: (a). Three-phase source voltages and (b). Source currents for case-2 with UPQC-2L



(a) (b)

Fig. 2.49: (a). Three-phase series injected voltages and (b). Shunt compensating currents for case-2 with UPQC-2L



(a) (b)

Fig. 2.50: (a). Three-phase load voltages and (b). load currents for case-2 with UPQC-2L

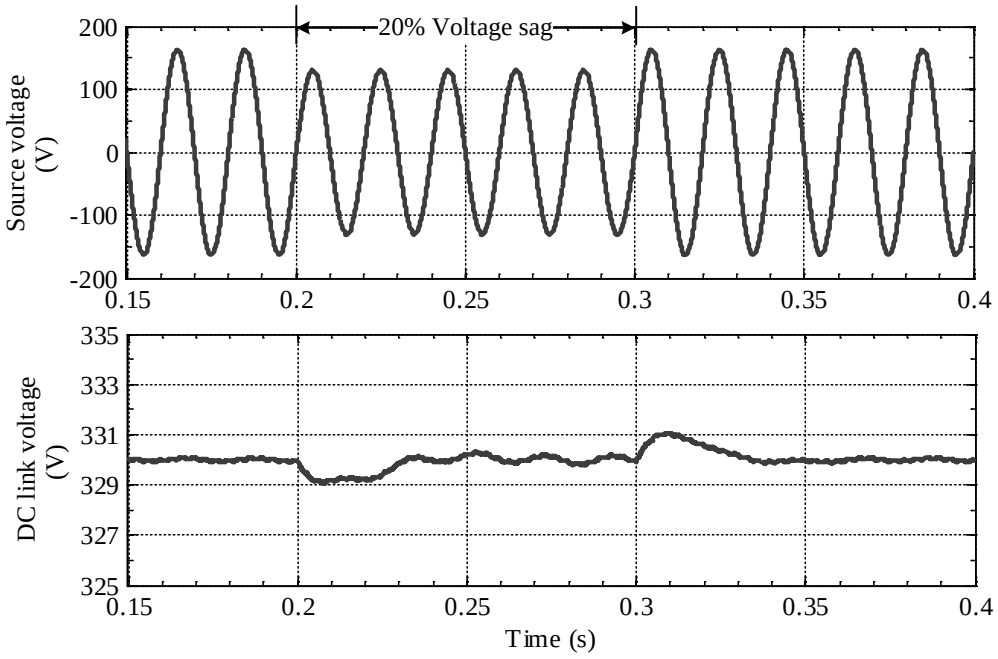


Fig. 2.51: Simulation results showing dc-link voltage variation during case-2 with UPQC-2L

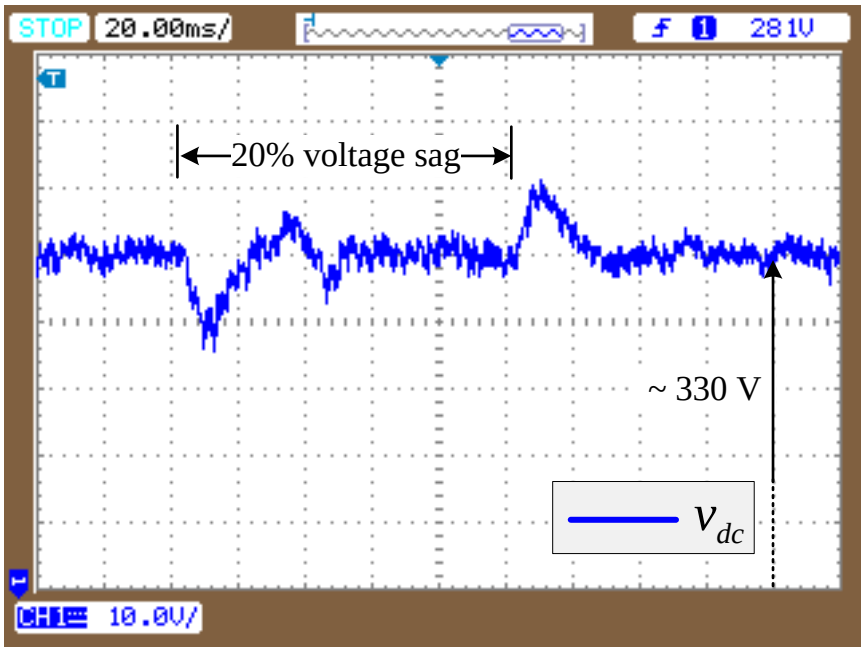


Fig. 2.52: Experimental results showing the dc-link voltage variation during vcase-2 with UPQC-2L

When the voltage sag occurred in the system, the series converter will react immediately to compensate the sag such that it utilises the stored energy from the dc-link capacitor. As the stored energy in the capacitor decreases the magnitude of the dc-link drops from the reference value. After few seconds, the dc-link voltage will rise and maintained at reference value because of the shunt converter starts supporting the compensation performed by the series converter. The fall/rise in dc-link voltage for simulation is 0.33%, whereas for experimental the value is 3%.

(B) UPQC-3L

The performance of UPQC-3L in comparison to UPQC-2L is evaluated with the identical voltage sag, which is applied to the source voltage at t =0.2s and cleared at 0.3s same as the previous case. Figure 2.53 shows the voltage compensation characteristics of series converter and Figure 2.54 shows the current compensation characteristics of shunt converter. The load voltage is maintained at peak fundamental phase magnitude of 162.1V during voltage sag condition, while the source current rms magnitude is increased by 0.8A for UPQC-3L as compared to the UPQC-2L case. The additional amount of current is drawn by the shunt converter to provide the active power losses in the three-level inverters because of the more number of switches as compared to the two-level inverters. However, the performance against voltage sag compensation is improved for UPQC-3L as compared to UPQC-2L. Figures 2.55 to 2.57 shows the corresponding experimental scope results to validate the simulation results. The dc-link voltages are shown in Figures 2.58 and 2.59 for simulation and experiment respectively. It can be observed that the both upper and lower dc-link voltages are well balanced.

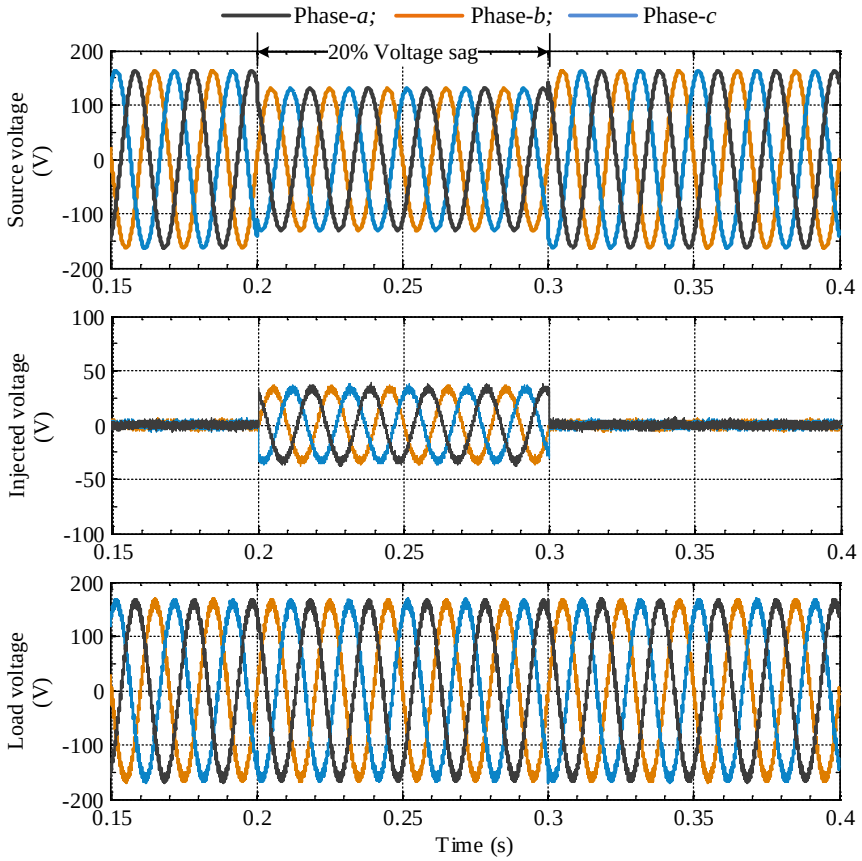


Fig. 2.53: Voltage compensation characteristics by shunt converter of UPQC-3L

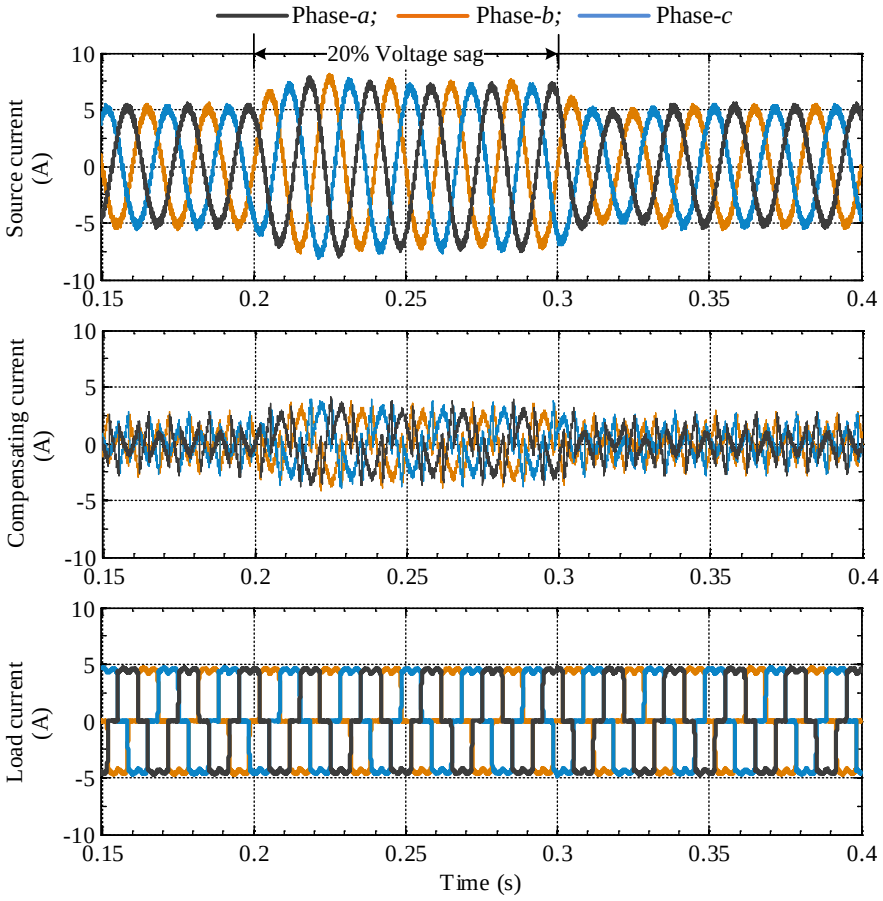
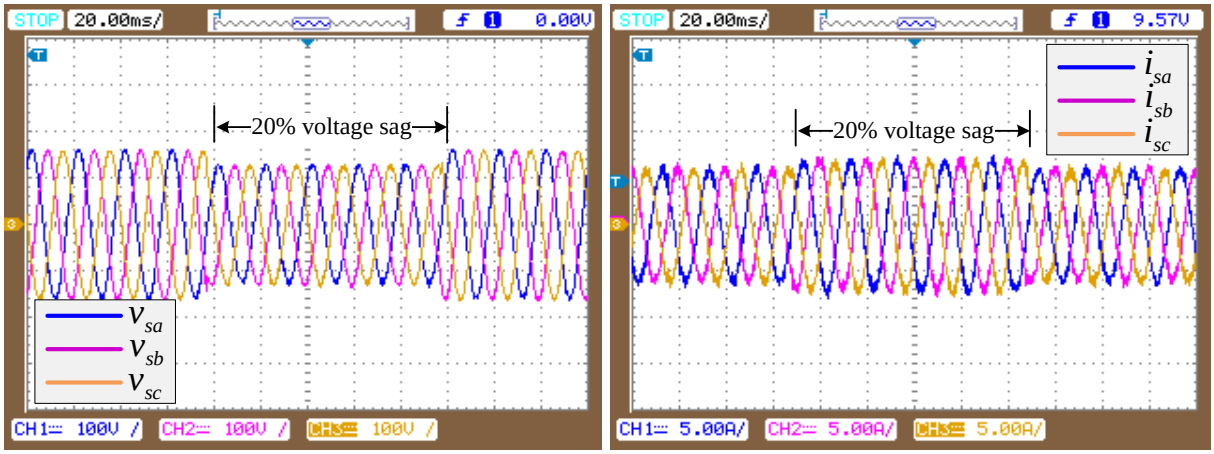
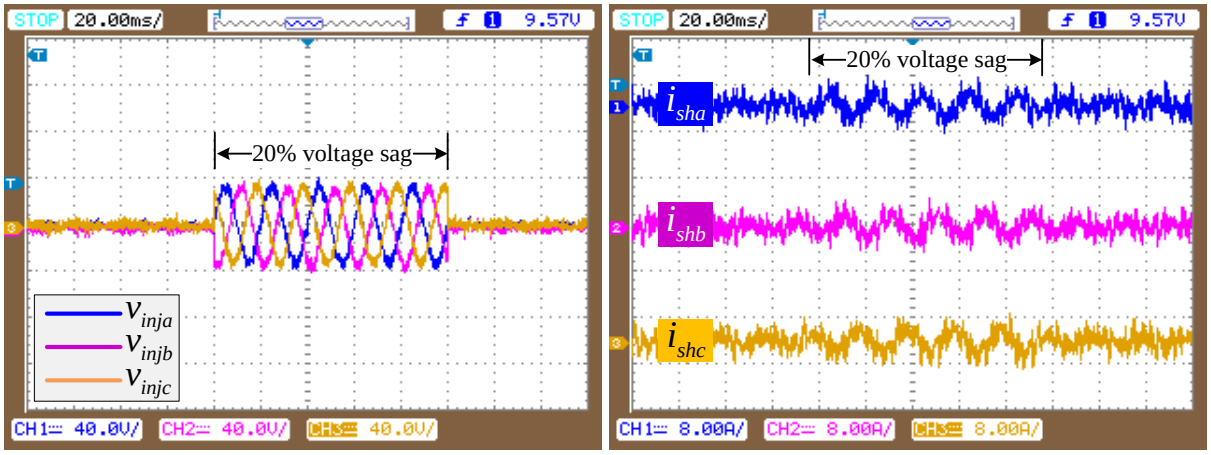


Fig. 2.54: Current compensation characteristics by shunt converter of UPQC-3L



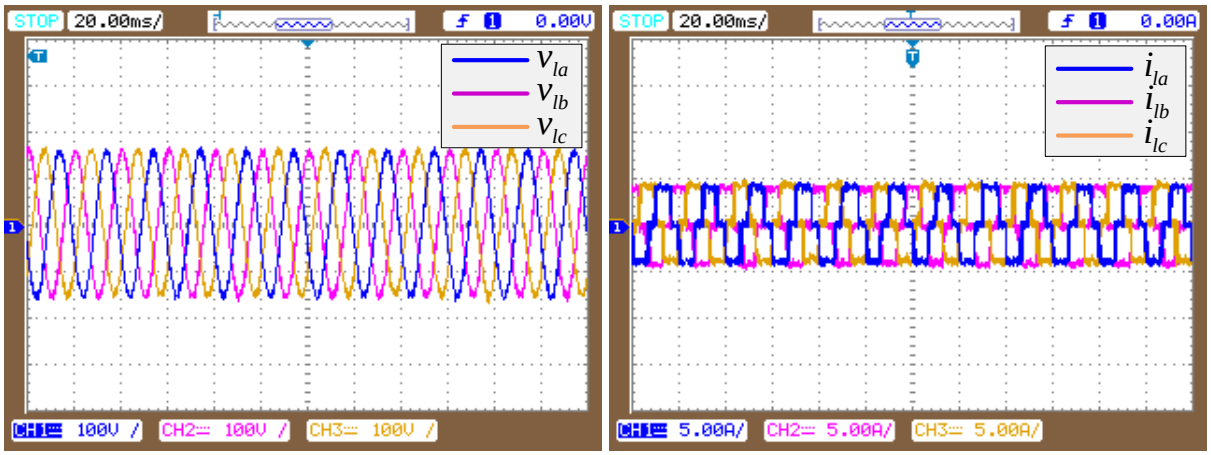
(a) (b)

Fig. 2.55: (a). Three-phase source voltages and (b). three-phase source currents for case-2 with UPQC-3L



(a) (b)

Fig. 2.56: (a). Three-phase series injected voltages and (b). Shunt compensating currents for case-2 with UPQC-3L



(a) (b)

Fig. 2.57: (a). Three-phase load voltages and (b). three-phase load currents for case-2 with UPQC-3L

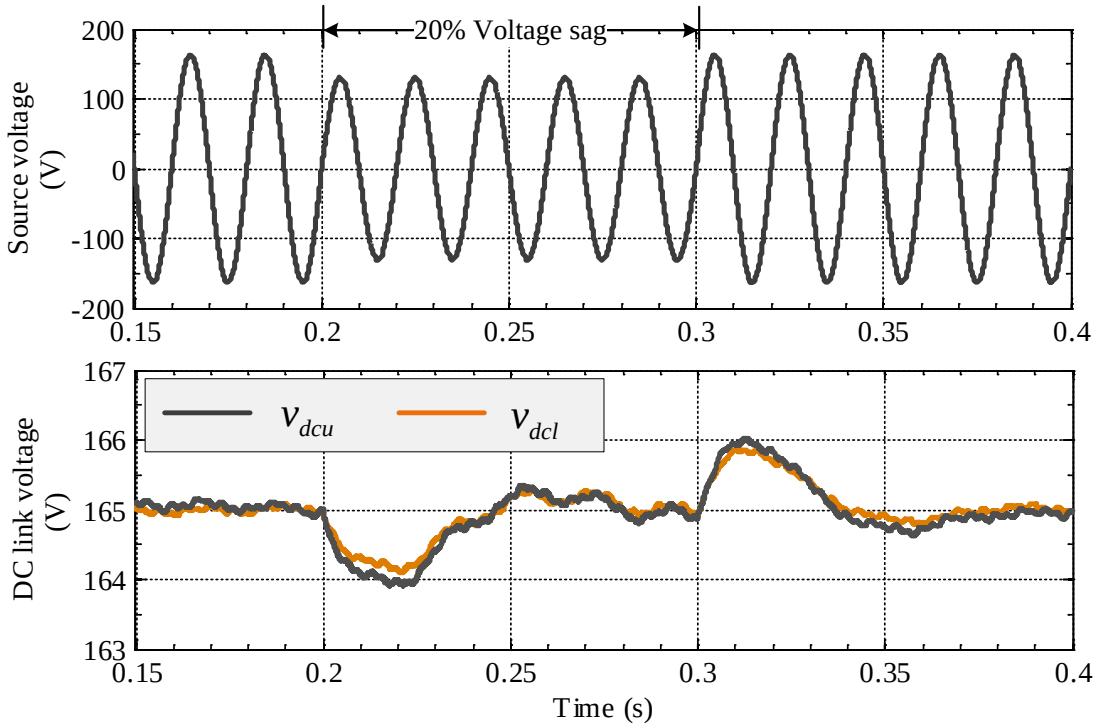


Fig. 2.58: Simulation results showing dc-link voltage variation during case-2 with UPQC-3L

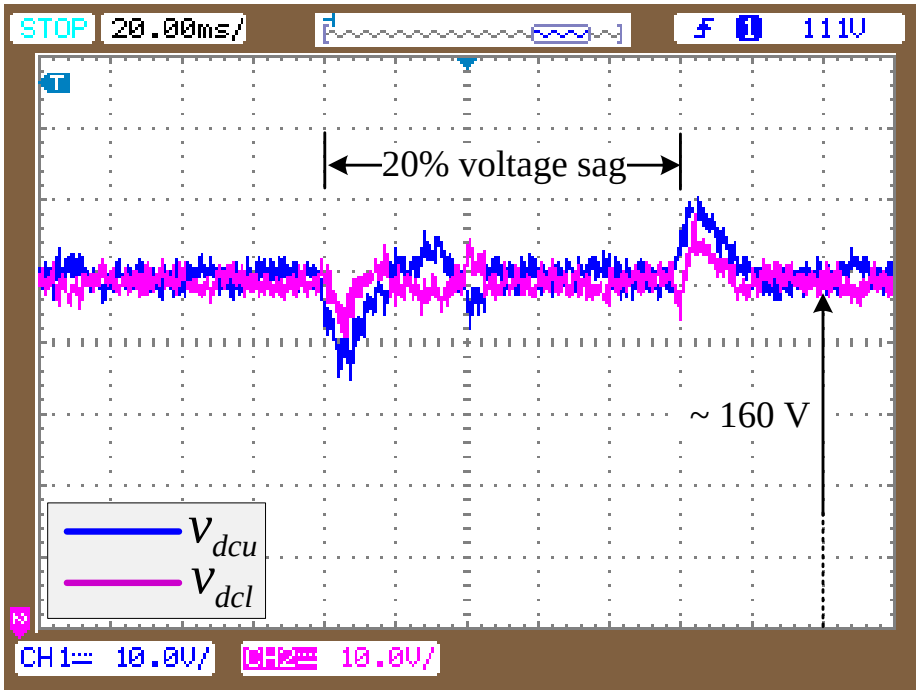


Fig. 2.59: Experimental results showing the dc-link voltage variation during case-2 with UPQC-3L

On comparing the experimental results with the simulation results, the dc-link voltage is slightly less from the dc-link voltage maintained by the simulations. The reference value of split dc-link voltage is selected as 165V, while the simulations shows that the dc-link voltage is well maintained closed to reference value with the average magnitude of 165V. On the other hand, experimental scope results shows that dc-link voltage is maintained at 160V.

(C) Summary

The quantitative comparison of peak fundamental phase magnitude of load voltage and source current between UPQC-2L and UPQC-3L for this case study is given in Table 2.6, where the results are considered from the experiment of phase-*a.*

Table 2.6: Comparison between UPQC-2L and UPQC-3L for sag compensation

Type of disturbance (Voltage sag)	**UPQC-2L**		**UPQC-ML**	
	Load voltage (V)	Source current (A)	Load voltage (V)	Source current (A)
Before compensation	130.6	5.39*	130.6	5.45*
After compensation	160.0	6.86	162.1	7.81

2.5.3 Case-3: Voltage Swell Compensation under Non-linear Load

The performance of the UPQC-2L and 3L is analysed with the voltage swell condition. The voltage swell is created in with 20% voltage rise (ie.32.66 V) in the source voltage from the nominal phase peak fundamental voltage of 163.3V. Such that phase peak fundamental magnitude of source voltage becomes 196V during swell condition.

(A) UPQC-2L

Figure 2.60 and 2.61 shows the performance of UPQC-2L with voltage swell on the source voltage. The response of the series converter to compensate voltage swell is exactly opposite to the voltage sag compensation, which is discussed previous subsection. When the voltage swell occurs on the source voltage at 0.2s, series converter immediately injects the additional amount of voltage from the nominal/reference value in phase opposition to the source voltage in order to maintain load voltage at rated value at PCC. This can be observed from simulation results shown in Figure 2.60. During voltage swell period from 0.2s to 0.3s, the source voltage, injected voltage and load voltage are having phase peak fundamental magnitude of 196V, 32.5, and 163.5V respectively. The current compensation characteristics are shown in Figure 2.61. During voltage swell compensation, the magnitude of source current is decreased from the normal operating condition, due to the reason the shunt converter fed back the additional active power to the source. The shunt converter in this case will be responsible for compensating nonlinear load harmonics along with the support to the series converter for proper compensation by maintaining the dc-link voltage at reference value. From Figure 2.61, it can be observed that the rms magnitude of source current during normal operating condition and voltage swell period from 0.2s to 0.3s is 3.62A and 2.85A respectively, where as load current magnitude is 3.58A, which is not depended on the voltage swell.

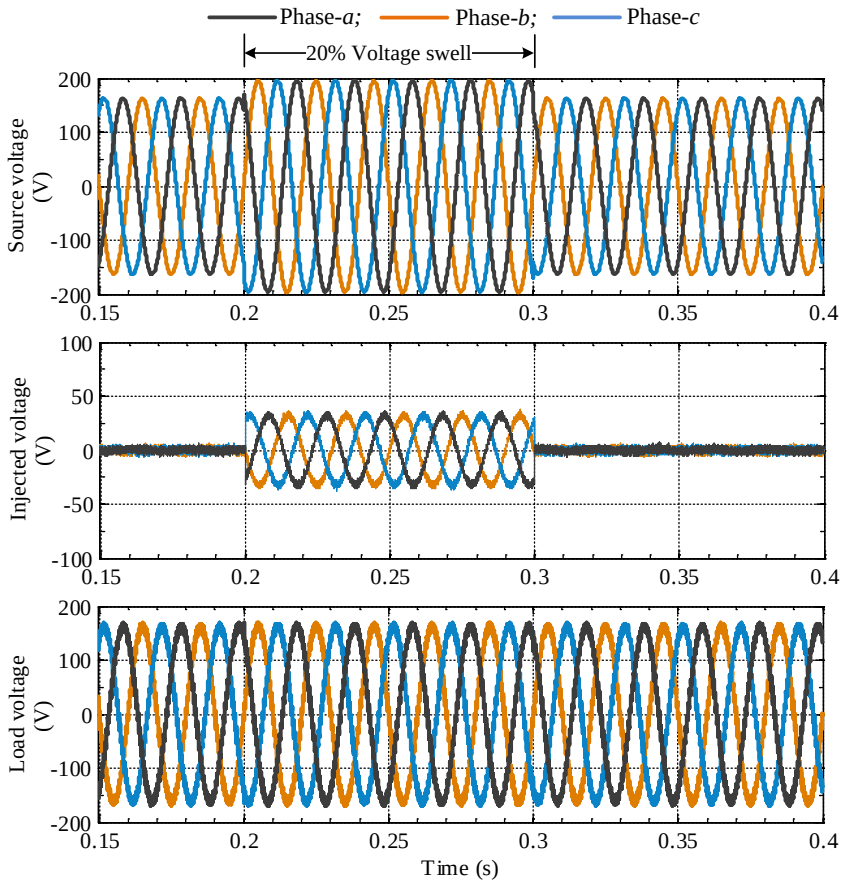


Fig. 2.60: Voltage compensation characteristics by shunt converter of UPQC-2L

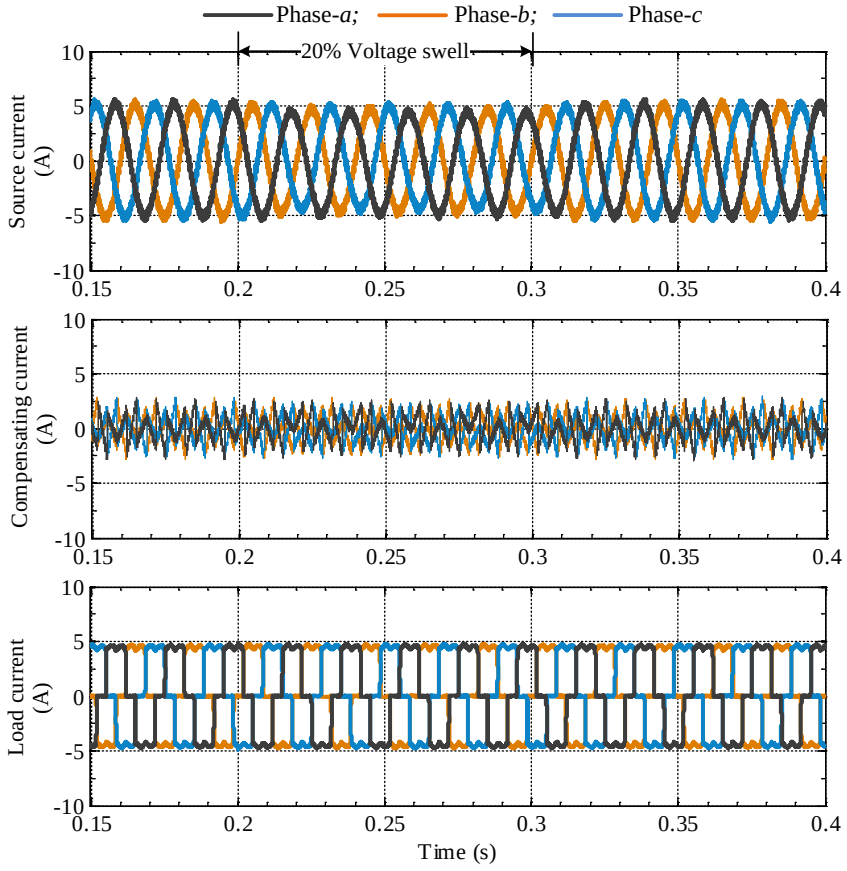
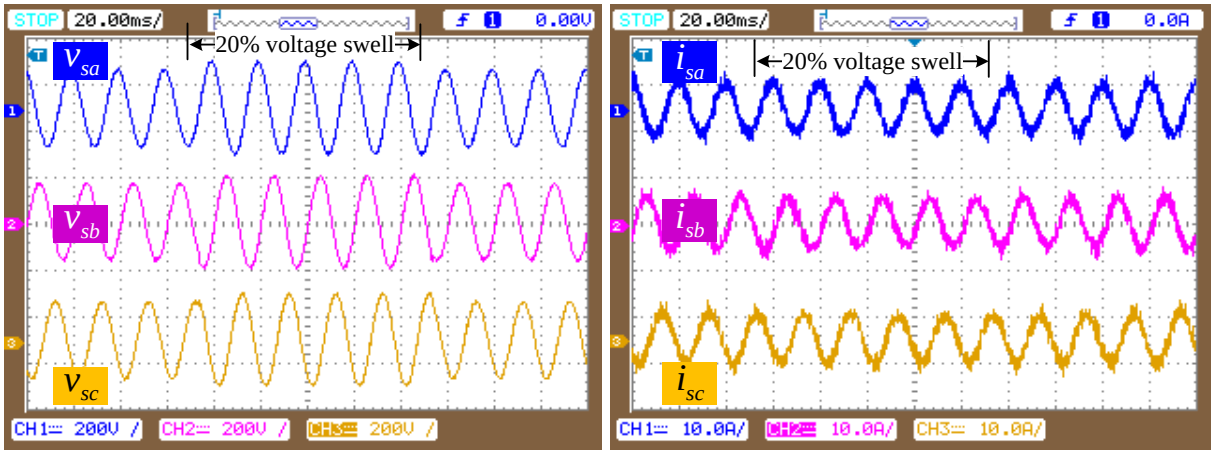
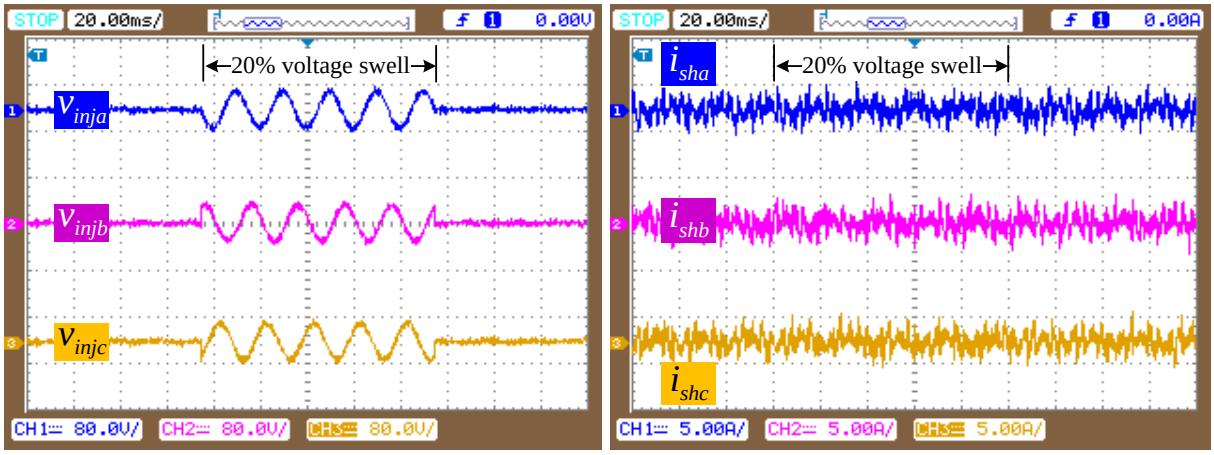


Fig. 2.61: Current compensation characteristics by shunt converter of UPQC-2L



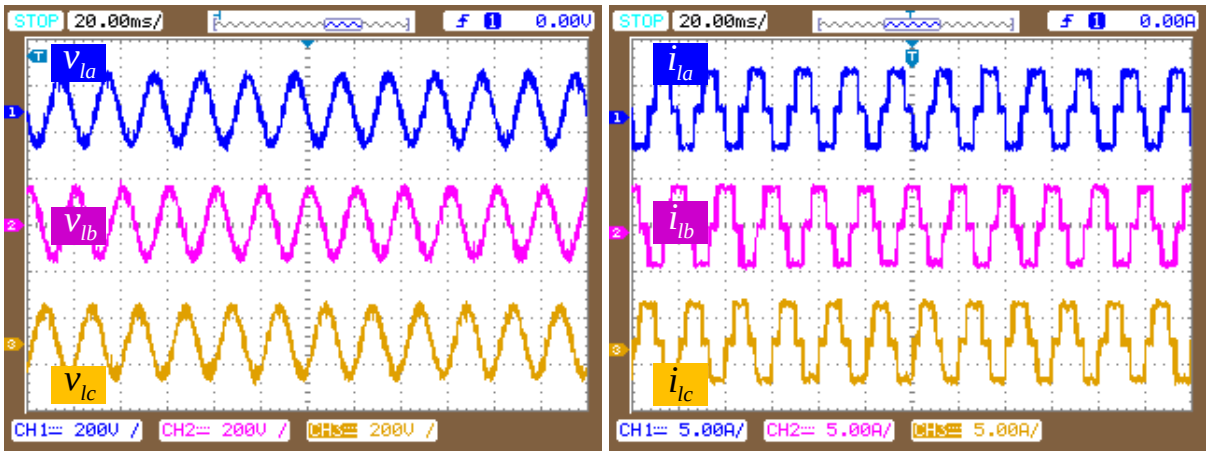
(a) (b)

Fig. 2.62: (a). Three-phase source voltages and (b). three-phase source currents for case-3 with UPQC-2L



(a) (b)

Fig. 2.63: (a). Three-phase series injected voltages and (b). Shunt compensating currents for case-3 with UPQC-2L



(a) (b)

Fig. 2.64: (a). Three-phase load voltages and (b). three-phase load currents for case-3 with UPQC-2L

In comparison to simulation results, the experimental scope results are presented in Figures 2.62 to 2.64. It can be noticed from the quantitative comparison with simulation results, the experimental results are having good agreement with simulation results, as the source voltage, series injected voltage and load voltages are having magnitude of 198V, 31.6V and 166..4V respectively during voltage swell period, whereas the source current is having 3.70A and 3.0A during normal and voltage swell compensation period. The harmonic profile of either source current or load voltages before and after compensation are not presented in this case because of the reason, it matches approximately as the case-1 described in this chapter.

The dc-link voltage is shown in Figures 2.65 and 2.66 with voltage swell for simulation and experiment respectively. From Figure 2.65, it can be observed that at the instant of voltage swell, the dc-link voltage rise up by an amount of 0.34% from the reference value and then after small interval the dc-link voltage is maintained at the reference value of 330V with negligible fluctuations around this value. The criteria of rise/fall the dc-link at the instant of voltage swell is exactly opposite to the instant of voltage sag occurrence in the system as explained in the previous subsection. Figure 2.66 shows the experimental scope results from the voltage sensor across the dc-link of UPQC-2L. The dc-link voltage is maintained at 329V in experimental validation and at 330V in simulation platform, whereas the reference voltage is selected as 330V for the selected line-line voltage magnitude of the system.

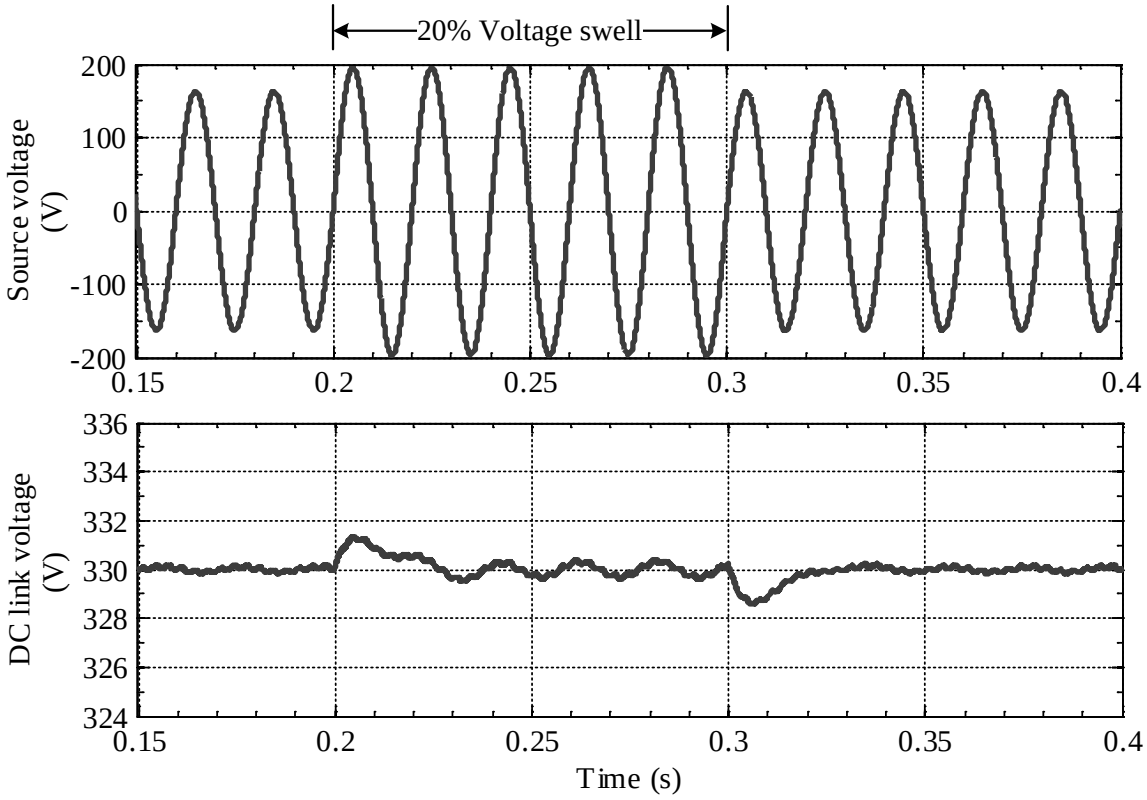


Fig. 2.65: Simulation results showing the dc-link voltage variation during case-3 with UPQC-2L

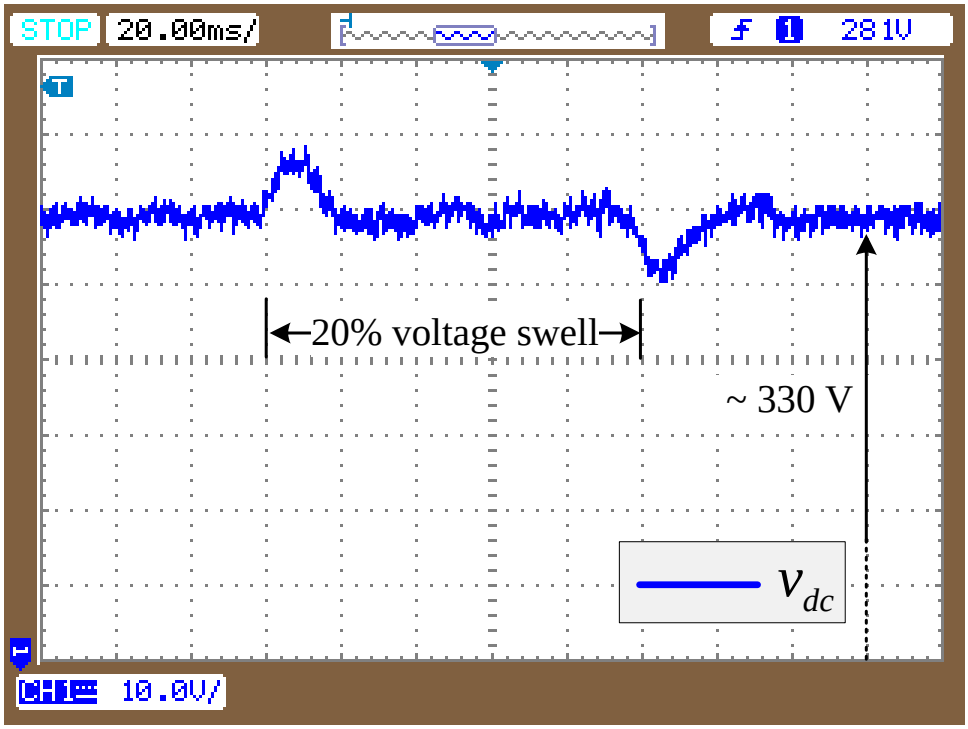


Fig. 2.66: Experimental results showing the dc-link voltage variation during case-3 with UPQC-2L

(B) UPQC-3L

Figures 2.67 and 2.68 shows the simulation results with three-phase voltage swell on the source voltage compensation with UPQC-3L. Similar to the UPQC-2L, UPQC-3L also provides the better compensation characteristics for both voltage and current compensation by providing 99% compensation against voltage swell. The load voltage is maintained at 164.5V with phase peak fundamental value during voltage swell period, while the load reference value is selected as 163.3V. In case of current compensation, the source current is maintained at phase rms value of 3.66A during normal operating conditions and at 3.21A during voltage swell compensation such that a slight increment in the current magnitude as compared to UPQC-2L.

Figures 2.69 to 2.71 shows the experimental results to validate the simulations presented in Figures 2.67 and 2.68. The load voltage is well compensated and it is maintained at 165V and source current is sinusoidal irrespective of the load current. The small decrement in the source current magnitude during voltage swell compensation period is already explained in the simulation results discussion. Figures 2.72 and 2.73 shows the magnitude of dc-link voltage maintained by the UPQC-3L during simulation study and in experimental validation. The reference value for split dc-link is chosen as 165V, while the upper dc-link capacitor is maintained at an average magnitude of 165.5V and lower is at 164.6V in simulation results; on the other hand, the experimental scope results shows that upper dc link is maintained at an average value of 162V and lower is at 160V.

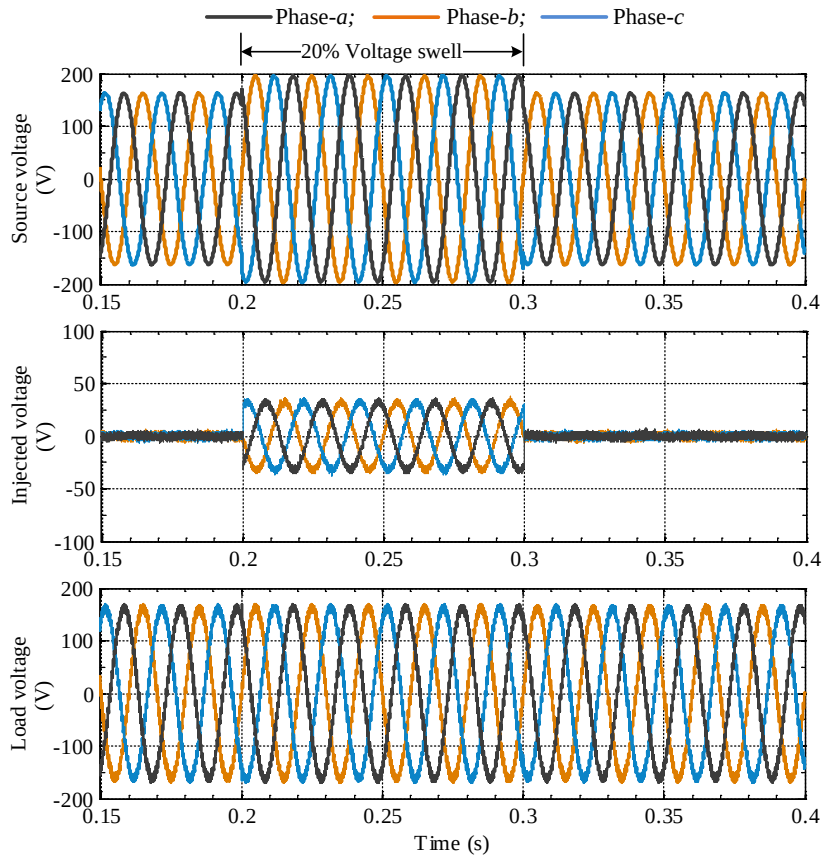


Fig. 2.67: Voltage compensation characteristics by shunt converter of UPQC-3L

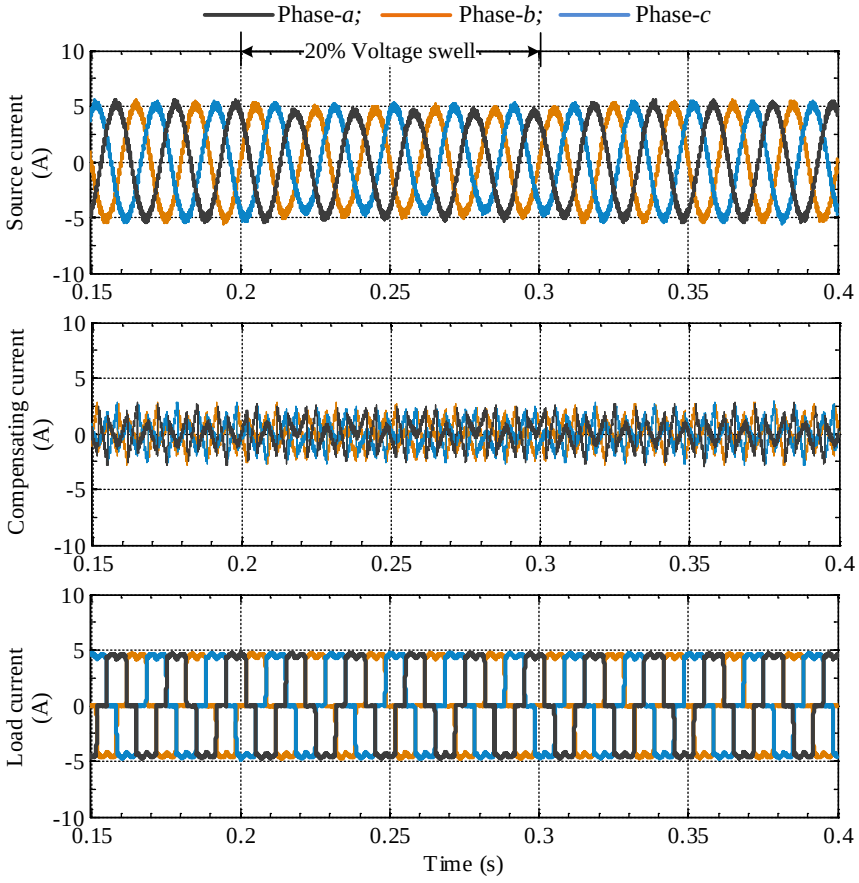
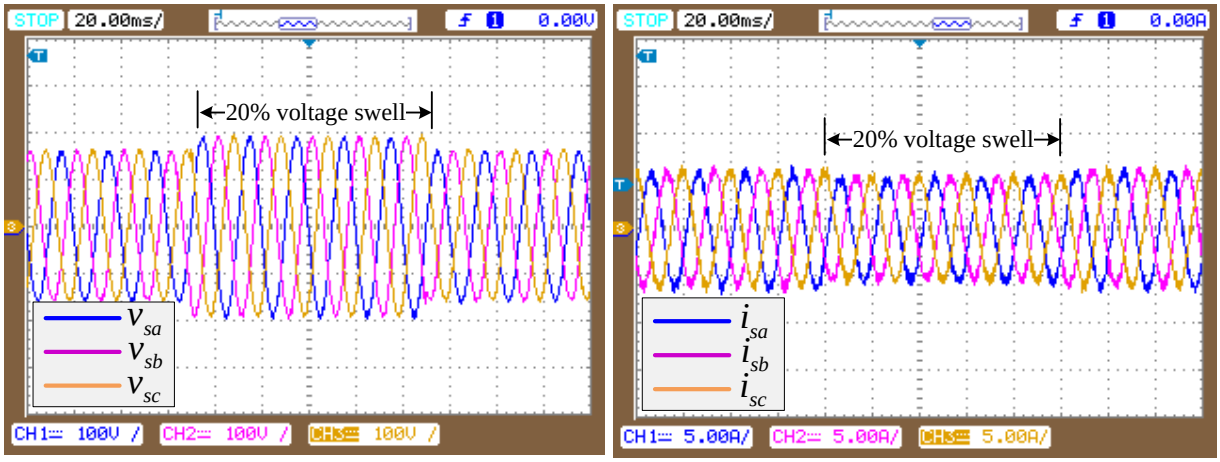
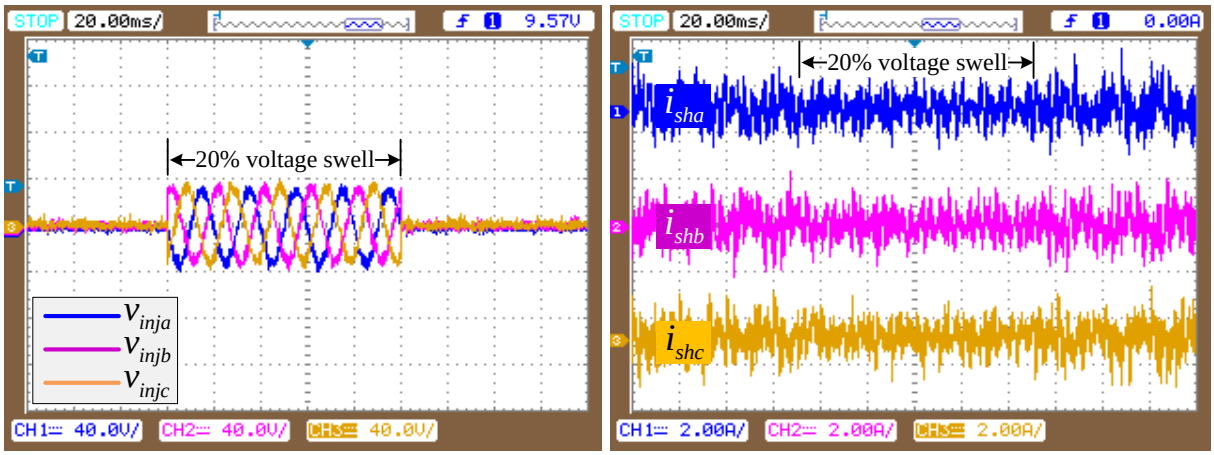


Fig. 2.68: Current compensation characteristics by shunt converter of UPQC-3L



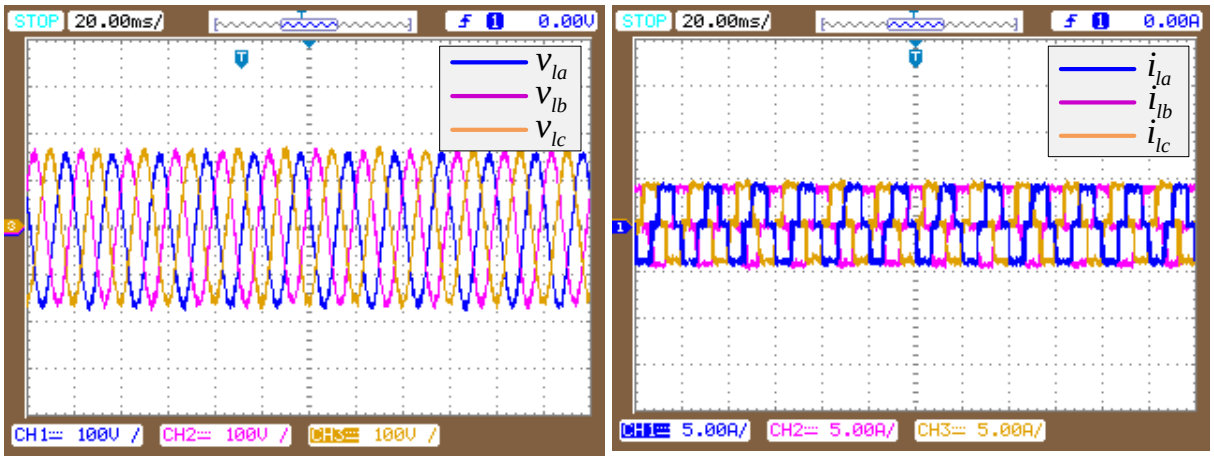
(a) (b)

Fig. 2.69: (a). Three-phase source voltages and (b). three-phase source currents for case-3 with UPQC-3L



(a) (b)

Fig. 2.70: (a). Three-phase series injected voltages and (b). Shunt compensating currents for case-3 with UPQC-3L



(a) (b)

Fig. 2.71: (a). Three-phase load voltages and (b). three-phase load currents for case-3 with UPQC-3L

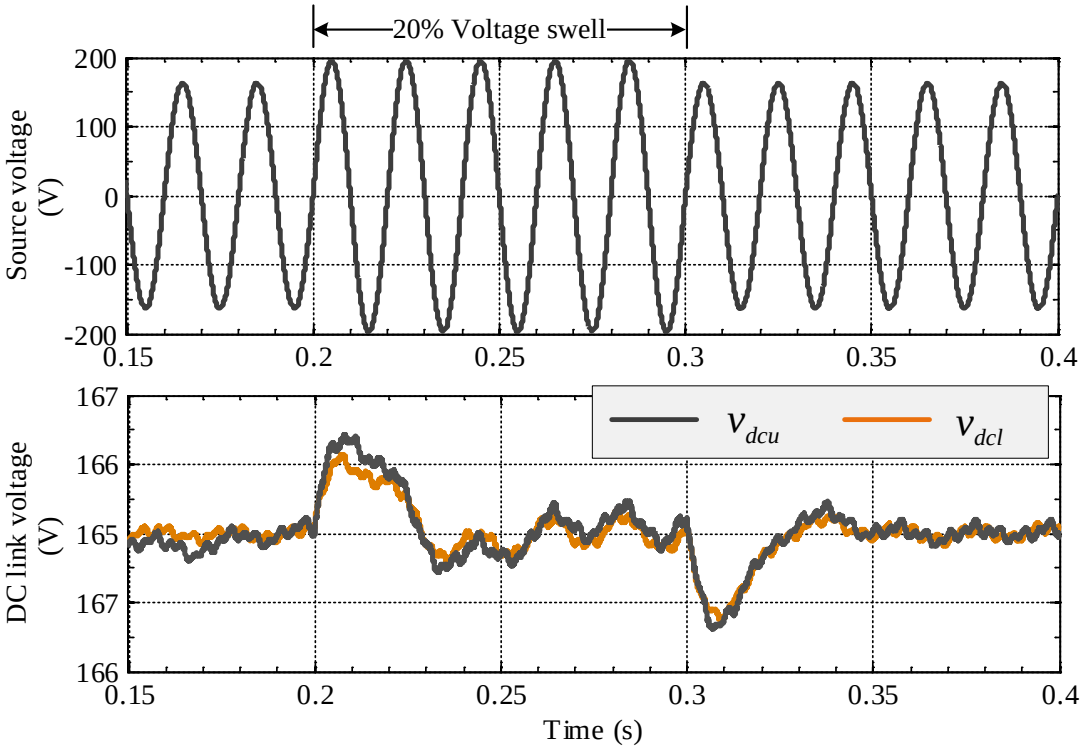


Fig. 2.72: Simulation results showing the dc-link voltage variation during case-3 with UPQC-3L

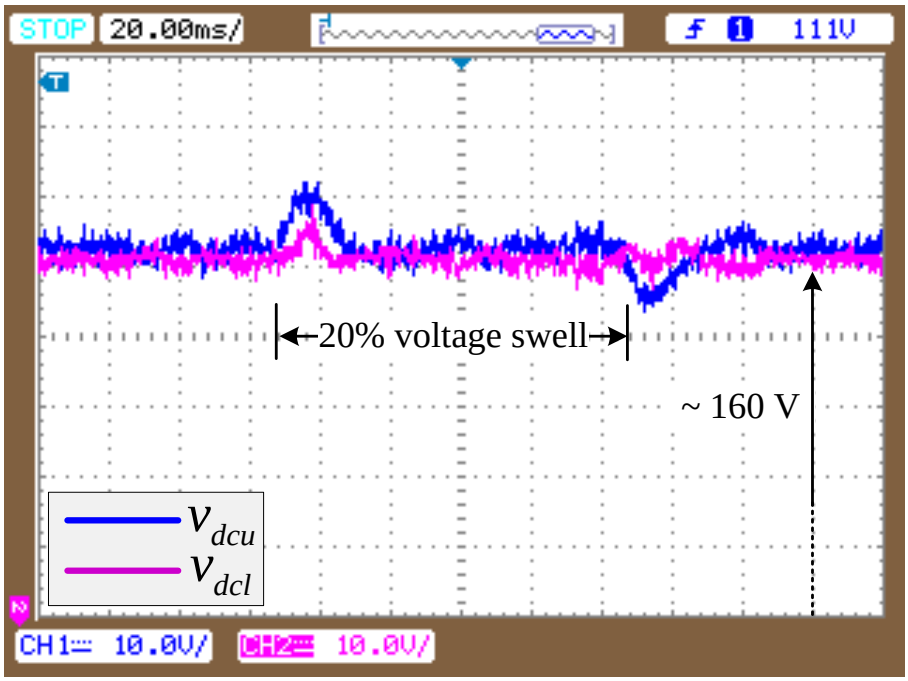


Fig. 2.73: Experimental results showing the dc-link voltage variation during case-3 with UPQC-3L

This can give a conclusion that the dc-link capacitor voltages are well balanced with the dc-link voltage regulator. The overall compensation characteristics against voltage swell along with non-linear load are presented in the following Table 2.7 for the purpose of comparison between UPQC-2L and UPQC-3L.

(C) Summary

The quantitative comparison of peak fundamental phase magnitude of load voltage and source current between UPQC-2L and UPQC-3L for this case study is given in Table 2.7, where the results are considered from the experiment of phase-*a.* The load voltage magnitudes are compared with the rated phase peak fundamental value of 163.3 V. From this comparison, it can be concluded that the compensating performance of UPQC-3L is better than UPQC-2L.

Table 2.7: Comparison of phase-*a* peak fundamental value between UPQC-2L and UPQC-3L for swell compensation

Type of disturbance (Voltage swell)	**UPQC-2L**		**UPQC-ML**	
	Load voltage (V)	Source current (A)	Load voltage (V)	Source current (A)
Before compensation	196.0	5.39*	196.0	5.48*
After compensation	165.3	4.17	164.5	4.21

* steady state value under normal operating conditions with current compensation by shunt converter

2.5.4 Case-4: Unbalanced Source Voltage Compensation

The performance of the UPQC-2L and 3L is analysed with the unbalanced voltage condition. The unbalance is created in with 40% and 20% voltage dip in two phases of three-phase supply. The 40% voltage dip is added to phase-*a*, while 20% voltage dip is added to phase-*c* and phase-*b* is unaffected and considered at rated value of 115V.

(A) UPQC-2L

The unbalanced source voltage is shown in axis-1 of Figure 2.74, where the phase peak fundamental magnitude of phase-*a*, *b*, and *c* are 114.31V, 163.30V, and 130.64V respectively. Figure 2.74 shows the steady state response of UPQC-2L on compensation of unbalance in the load voltage at PCC. The UPQC injects the in-phase component of phase voltage, whose magnitude is equal to the difference between the reference load voltage and source voltage magnitudes. From axis-2, it can be observed that the voltage magnitude of 46.4V has to be injected into phase-*a* in series with the source and the same time 31.6V of injected voltage has to added to phase-*c* to maintain load voltages are at same level of phase-*b*, which is not affected in creating unbalance in the source voltage. Axis-3 from Figure 2.74 shows that load voltage is maintained at phase peak fundamental value of 160.7V, 162.5V, and 161.7V at phase-*a*, *b*, and *c* respectively. The dc-link voltage during compensation period is shown in the axis-4. The UPQC-2L is able to maintain dc-link voltage at an average of 329.5V against reference voltage of 330V.

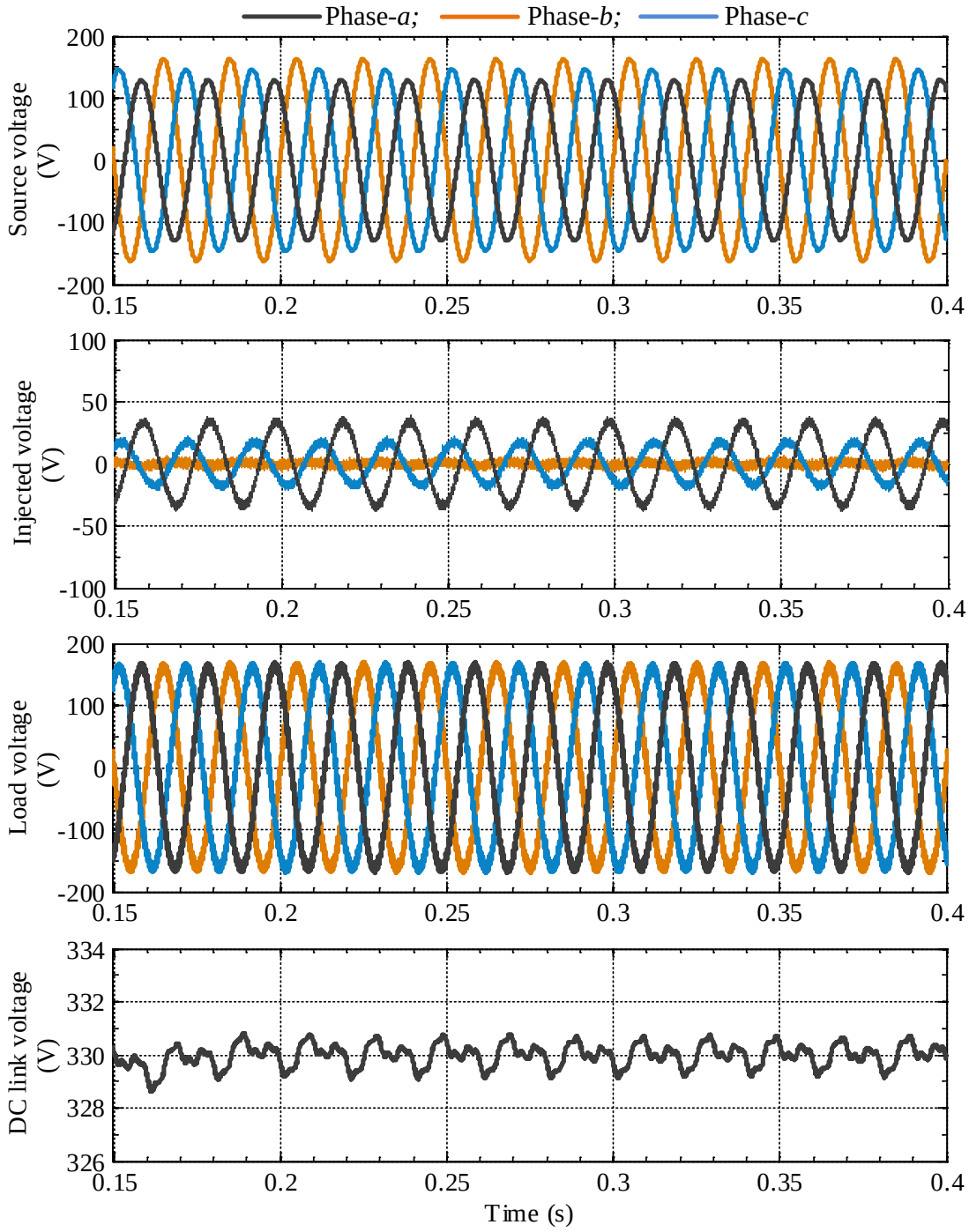
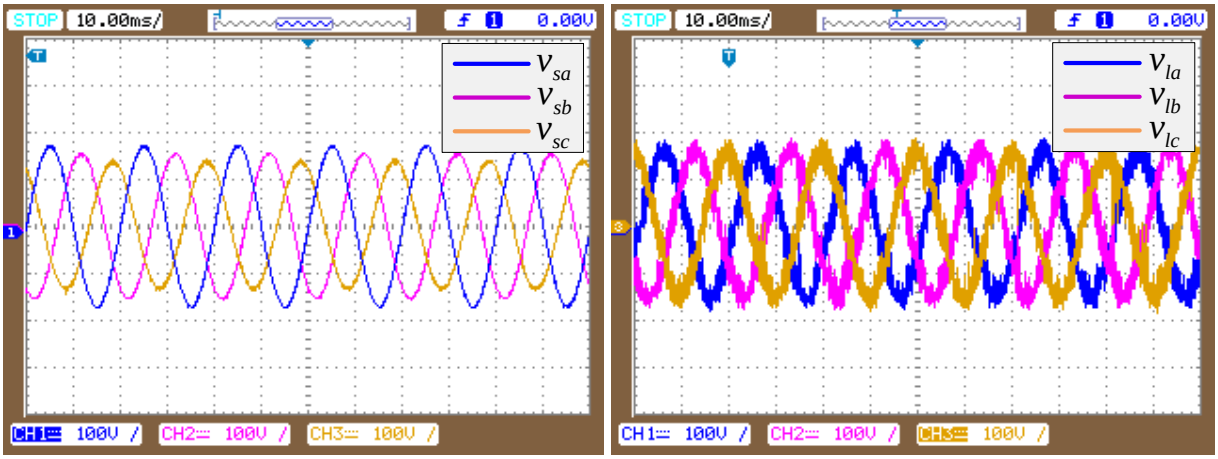


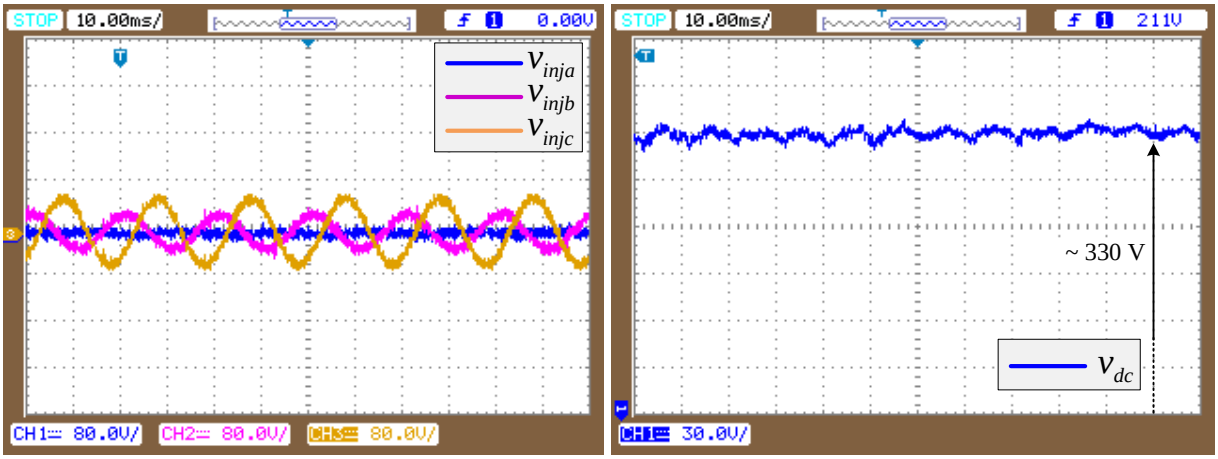
Fig. 2.74: Steady state voltage compensation characteristics of UPQC-2L under case-4.

The experimental scope results are also presented in this case, to justify the simulations results. Figure 2.75 and 2.76 shows that the steady state results of different voltage quantities. From these results it can be observed that, the load voltages are well maintained at against reference phase peak magnitude of 163.3V, with 159.7V, 162.0V, and 160.4V on phase-*a*, *b*, and *c* respectively. Figure 2.76(a), shows that the magnitude equal to 45.4V, 0.8V and 29.8V is generated by the series converter to compensate the unbalancing voltage corresponding to phase-*a*, *b* and *c*. On the other hand, the dc-link voltage is maintained at an average value of 330V with small fluctuations from the reference value.



(a) (b)

Fig. 2.75: (a). Three-phase source voltages and (b). Load voltages for case-4 with UPQC-2L



(a) (b)

Fig. 2.76: (a). Three-phase series injected voltages and (b). The dc-link voltage during case-4 with UPQC-2L

(B) UPQC-3L

The performance evaluation test is conducted on UPQC-3L with similar unbalance parameters to carry out the comparative analysis with UPQC-2L. Figure 2.77 shows the steady state response of UPQC-3L on compensation of unbalance in the source voltage. From axis-2, it can be observed that the magnitude equal to 48.5V, 0.2V and 30.9V is generated by the series converter to compensate the unbalancing voltage corresponding to phase-*a*, *b* and *c*. Axis-3 shows that load voltage is maintained at phase peak fundamental magnitude of 162.8V, 163.4V, and 161.5V at phase-*a*, *b*, and *c* respectively. The dc-link voltage during compensation period is shown in axis-4. The UPQC-3L is able to maintain dc-link voltage at an average of 165.5V on upper capacitor and 165V on lower capacitor against reference voltage of 165V. The experimental results are presented to justify the simulations, which are shown in Figure 2.78 and 2.79 with the steady state results of different voltage quantities.

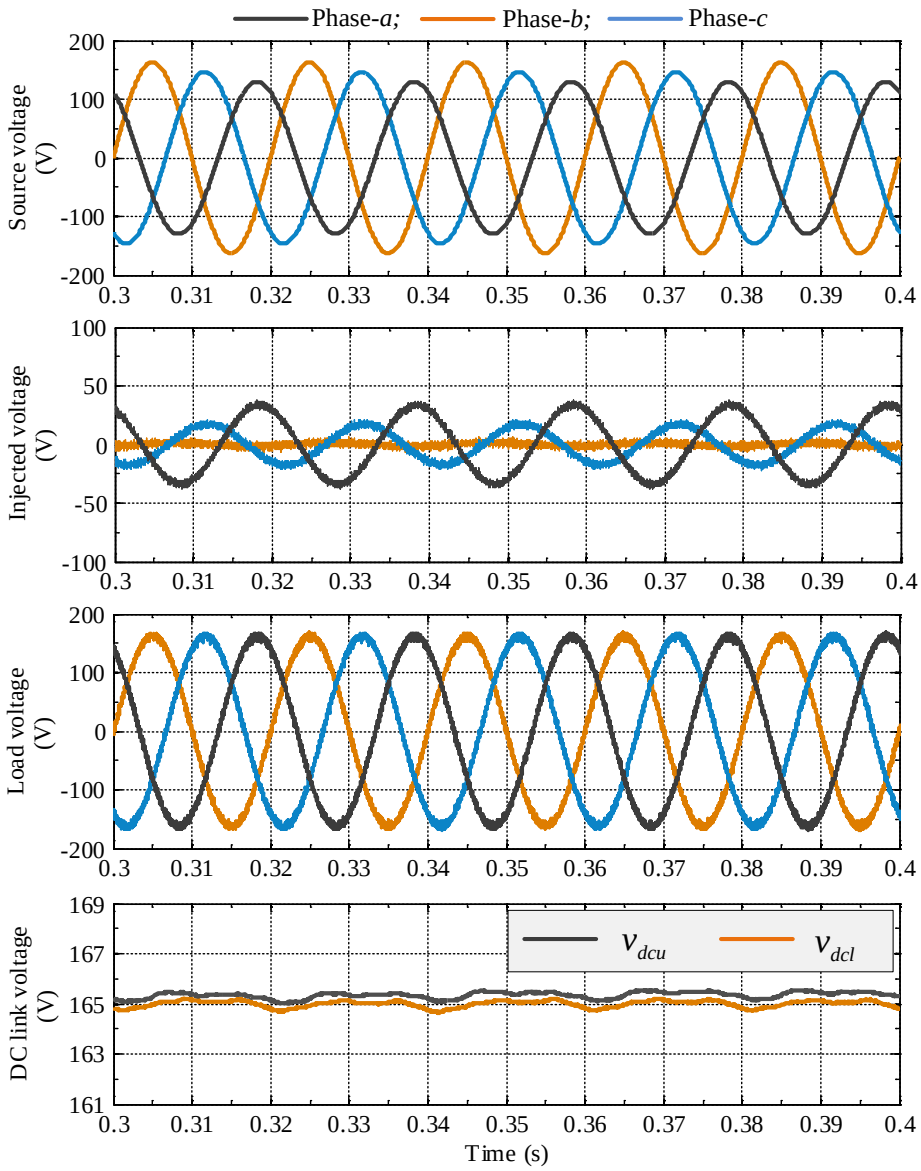
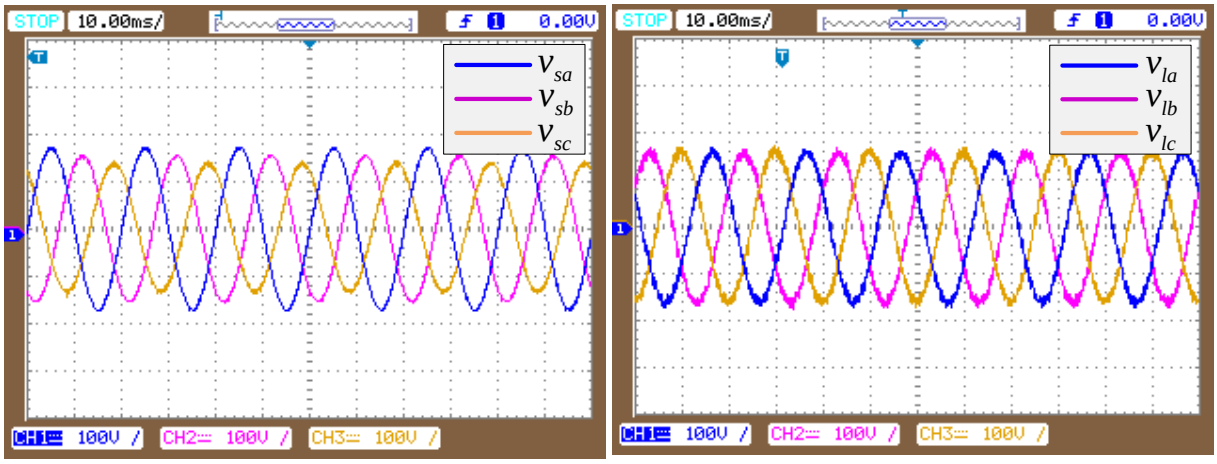
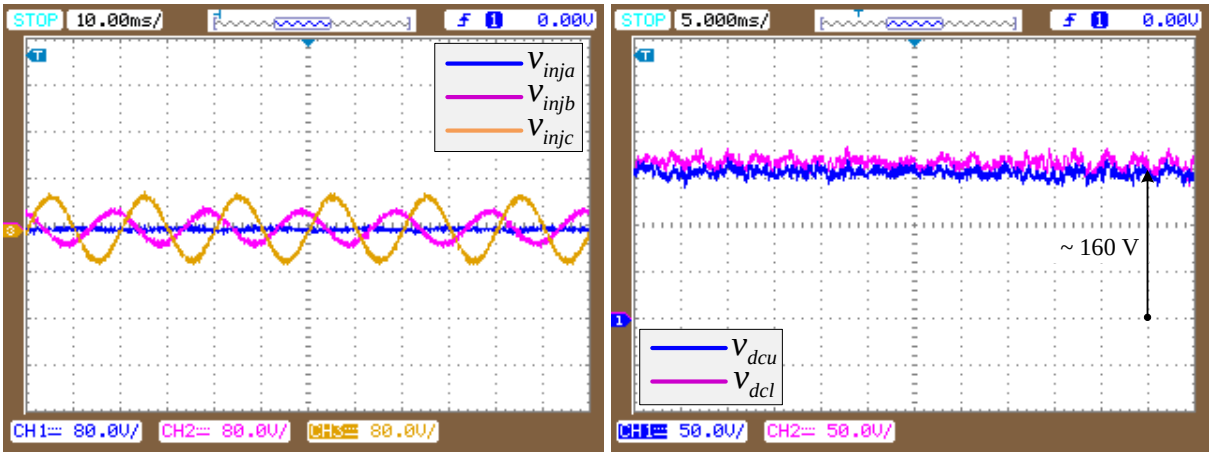


Fig. 2.77: Voltage compensation characteristics by shunt converter of UPQC-3L



(a) (b)

Fig. 2.78: (a). Unbalanced three-phase source voltages and (b). load voltages after compensation for case-4 with UPQC-3L



(a) (b)

Fig. 2.79: (a). Three-phase series injected voltages and (b). dc-link voltage during case-4 by UPQC-3L

It can be observed from these results that, the load voltage is well maintained at against reference phase peak amplitude of 163.3V, with 162V, 163.1V, and 161 on phase-*a*, *b*, and *c* respectively. On the other hand, the dc-link voltage is maintained at an average value of 160V on upper capacitor and 163V on lower capacitor with small fluctuations from the reference value.

(C) Summary

The quantitative comparison of peak fundamental phase magnitude of load voltage at PCC between UPQC-2L and UPQC-3L for this case study is given in Table 2.8, where the results are considered from the simulation results of phase-*a.* The load voltage magnitudes are compared with the rated phase peak fundamental value of 163.3V. From this comparison, it can be concluded that the compensating performance of UPQC-3L is slightly better than UPQC-2L.

Table 2.8: Comparison of phase-*a* peak fundamental value between UPQC-2L and UPQC-3L for voltage unbalancing compensation

Type of disturbance (Unbalanced supply)	**UPQC-2L**	**UPQC-3L**
	Load voltage magnitude (V) (V_{la}, V_{lb}, V_{lc})	Load voltage magnitude (V) (V_{la}, V_{lb}, V_{lc})
Before compensation	163.30, 130.64, 114.31	163.30, 130.64, 114.31
After compensation	162.0, 161.5, 160.7	163.4, 162.8, 161.5

2.5.5 Case-5: Unbalanced Distorted Source Voltage Compensation

In addition to unbalanced voltage compensation, the waveform distortion is added to evaluate the performance of the UPQC-2L and 3L. The unbalance is created in with 40% and 20% voltage dip in two phases of three-phase supply. The 40% voltage dip is added to phase-a, while 20% voltage dip is added to phase-*c* and phase-*b* is unaffected and considered at rated value of 115V as discussed in the case-4. The distorted supply voltage is created with by adding the most dominant harmonic voltages to the fundamental voltage waveform, such as 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics with corresponding magnitudes of $1/5^{th}$, $1/7^{th}$, $1/11^{th}$, and $1/13^{th}$ magnitude of fundamental value. The resultant source voltages after adding distortion to the unbalanced voltages are shown in Figure 2.80 at axis-1.

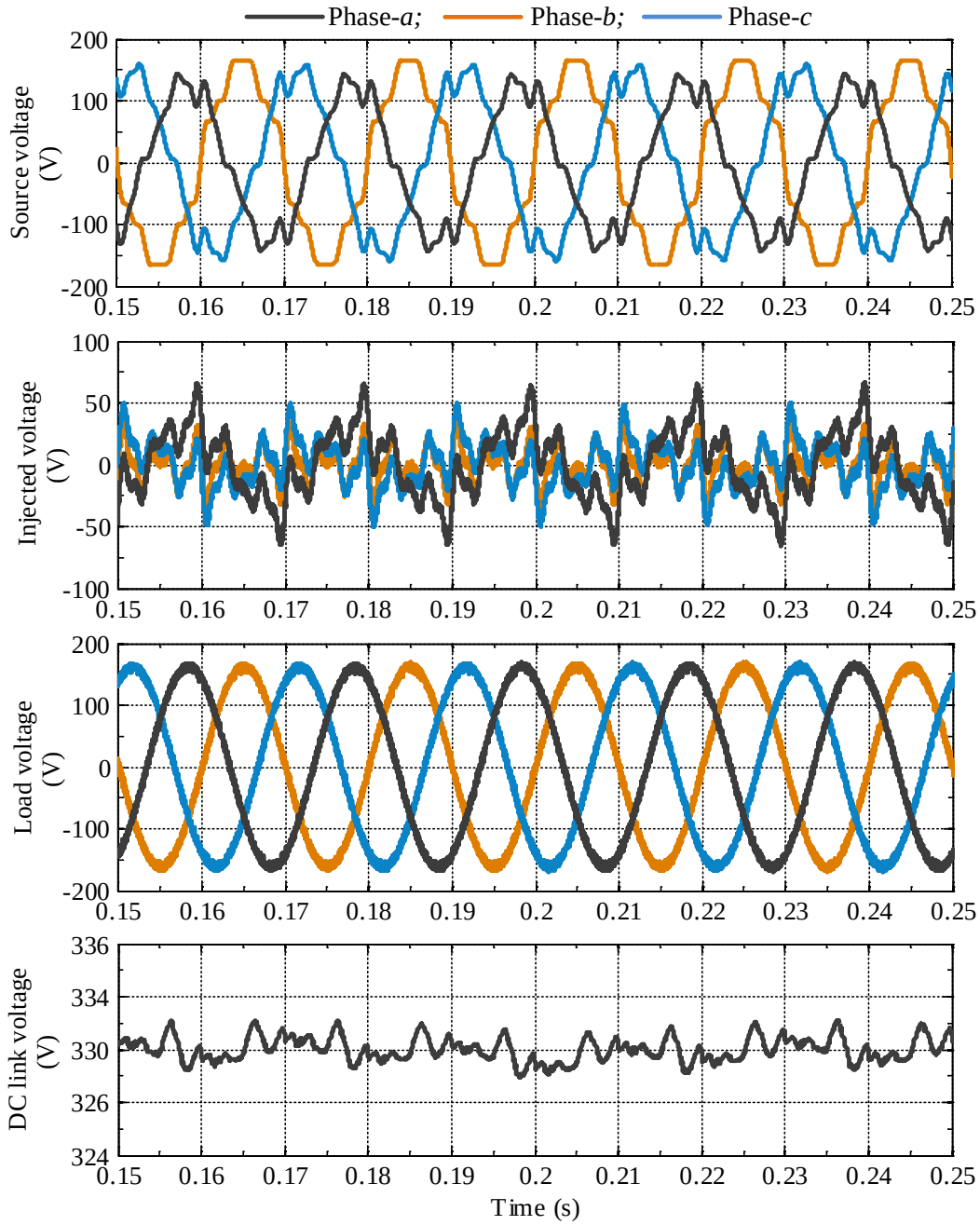


Fig. 2.80: Voltage compensation characteristics by shunt converter of UPQC-2L

(A) UPQC-2L

Figure 2.80 shows the steady state response of UPQC-2L on compensation of distorted and unbalanced source voltage. The distorted unbalanced source voltage is shown at axis-1, where the phase peak fundamental magnitude of phase-*a*, *b*, and *c* are 112.41V, 162.04V, and 141.35V respectively. The series injected voltages are shown at axis-2. It can be observed from axis-3 is that the three-phase load voltages are maintaining sinusoidal and phase magnitude of 159.20V, 160.0V and 159.8V on phase-*a*, *b*, and *c* respectively. The profile of dc-link voltage is shown in axis-4, whose magnitude is maintained around the reference value of 330V with the peak-peak fluctuation of 1.15%.

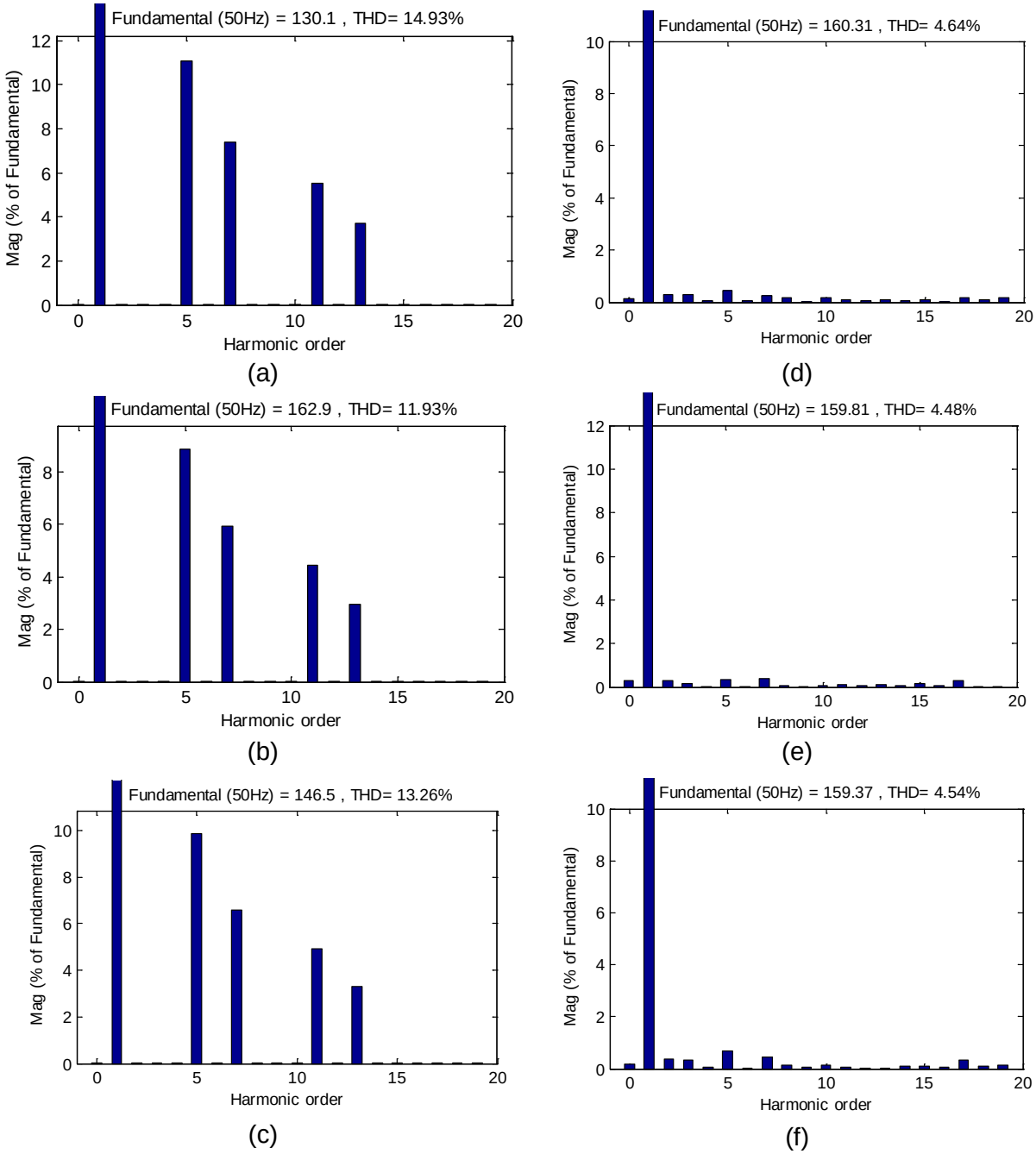
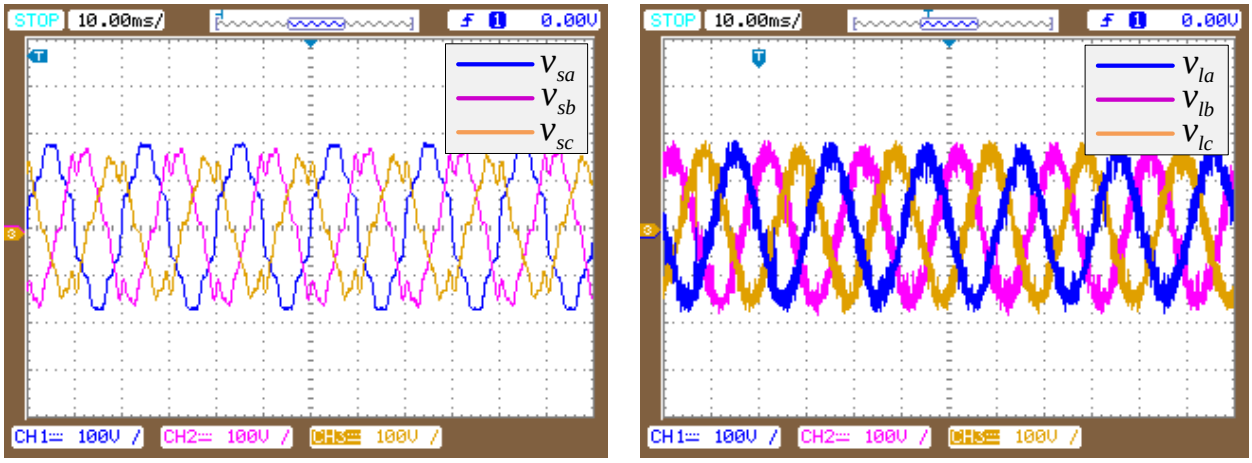
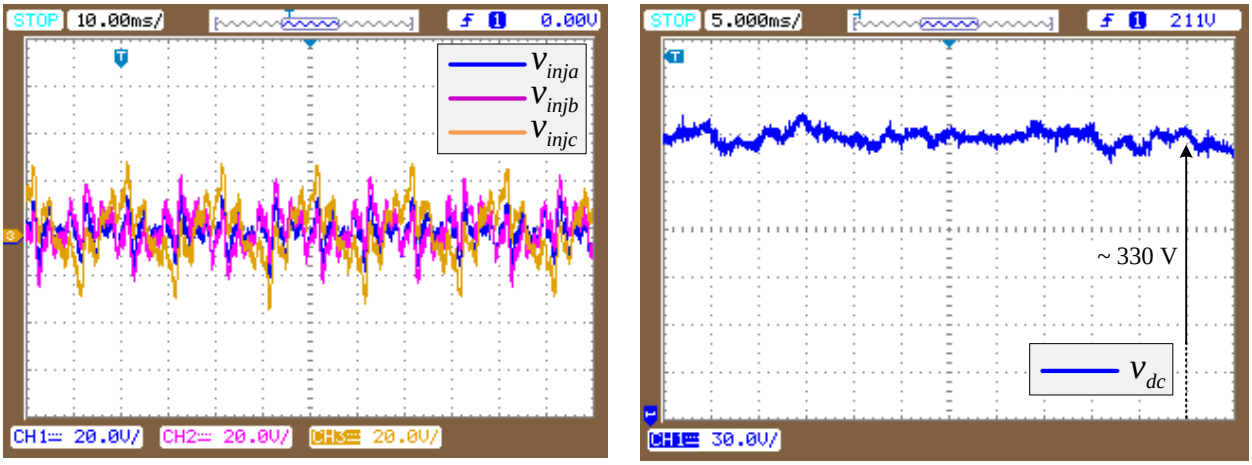


Fig. 2.81: Harmonic spectrum of voltages: (a)-(c) three-phase source voltage; (d)-(f) three-phase load voltage



(a) (b)

Fig. 2.82: (a). Unbalanced and distorted three-phase source voltages and (b). Load voltages after voltage compensation with UPQC-2L



(a) (b)

Fig. 2.83: (a). Three-phase series injected voltages and (b). The dc link voltage during ucase-5 with UPQC-2L

Figure 2.81 shows the FFT analysis captured from MATLAB Simulink of three-phase source and load voltages. The validated experimental results are shown in Figure 2.82 and 2.83. Though the load voltage is having ripple content because of mistuning of series LC filter and due to sampling period offered to the hysteresis controller, the magnitude is maintained at phase peak fundamental value of 158.3V, 159.5 and 158.7V on phase-*a*, *b*, and *c* respectively. The dc-link voltage variation during compensation period is depicted in Figure 2.83(b). Figure 2.84 shows the THD windows captured from the Fluke power analyser for three-phase source and load voltages.

(B) UPQC-3L

The performance of UPQC-3L with distorted unbalanced source voltage is conducted and the simulation and experimental results are presented in the Figures 2.85 and 2.87-2.88 respectively. On comparing the results with UPQC-2L, the UPQC-3L performed improved

compensation characteristics against distorted unbalanced case. It can be observed from axis-3 of Figure 2.85 is that the three-phase load voltages are maintaining sinusoidal and phase magnitude of 160.5V, 162.4V and 161.8V on phase-*a*, *b*, and *c* respectively.

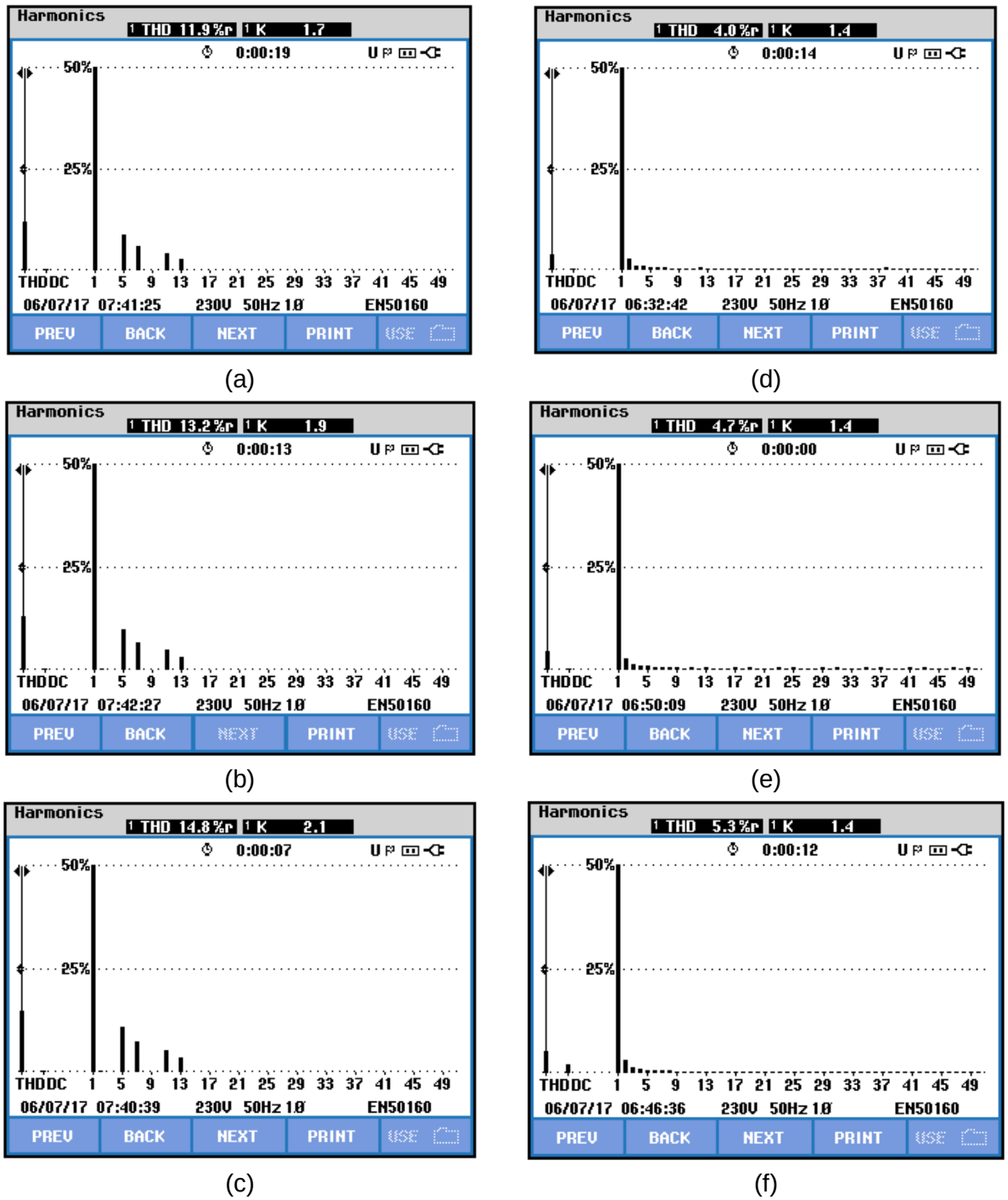


Fig. 2.84: Harmonic spectrum of voltages: (a)-(c) three-phase source voltage; (d)-(f) three-phase load voltage

The variation of dc-link voltage is shown in axis-4, whose magnitude is maintained around the reference value of 165V with the peak-peak fluctuation of 1.12%. The experimental scope results shows that the magnitude of load voltages are maintained at phase peak fundamental value of 159.6V, 161.5 and 161.1V on phase-*a*, *b*, and *c* respectively.

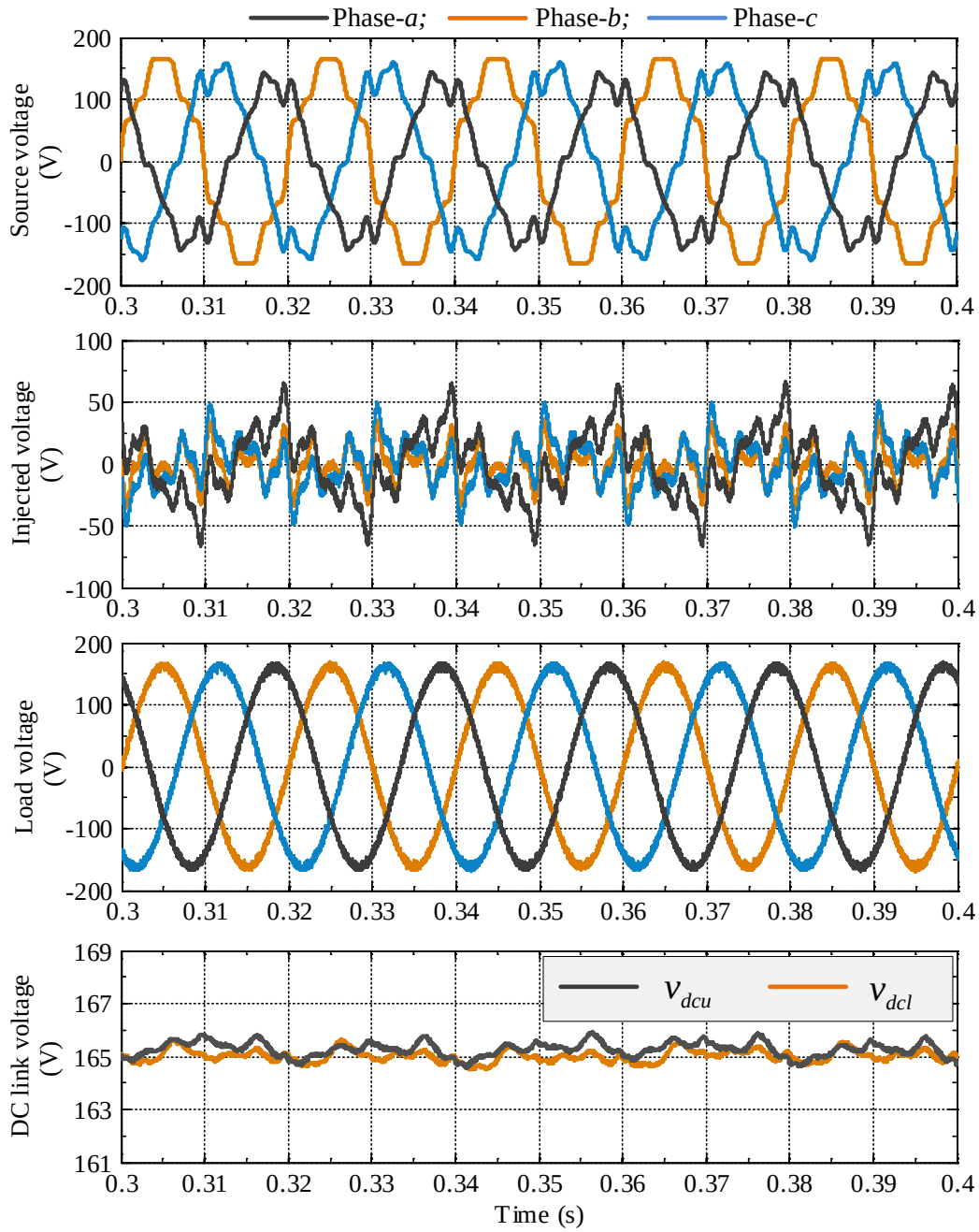
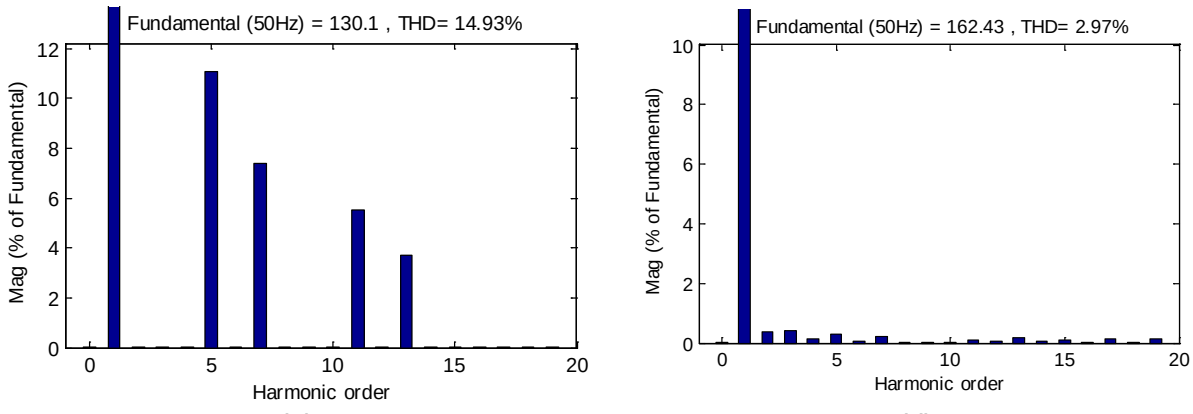


Fig. 2.85: Voltage compensation characteristics by shunt converter of UPQC-3L



(a) (d)

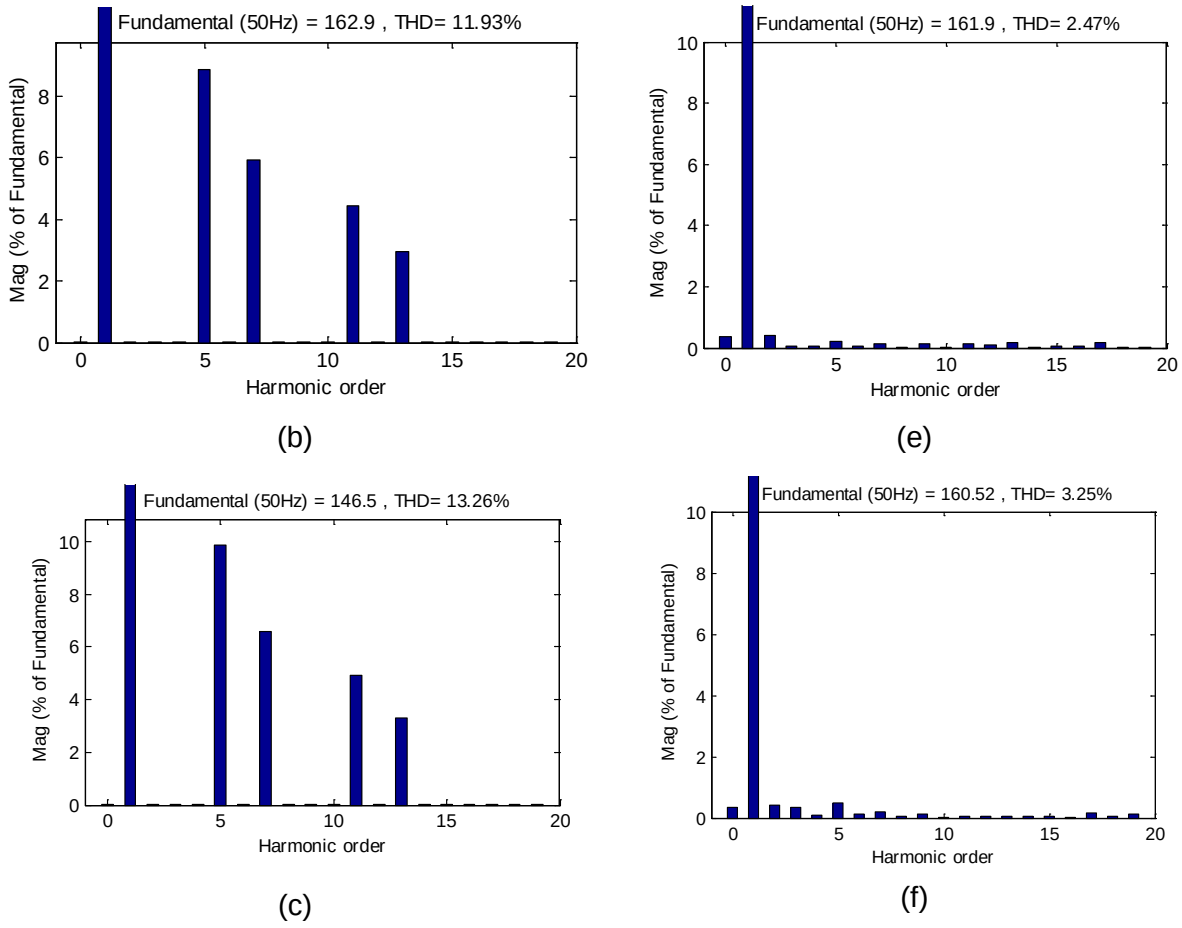


Fig. 2.86: Harmonic spectrum of voltages: (a)-(c) three-phase source voltage; (d)-(f) three-phase load voltage

The dc-link voltage variation on both split capacitors are displayed at Figure 2.88(b). Figure 2.86 shows the FFT analysis captured from MATLAB Simulink of three-phase load voltages, whereas Figure 2.89 shows the THD windows captured from the Fluke power analyser.

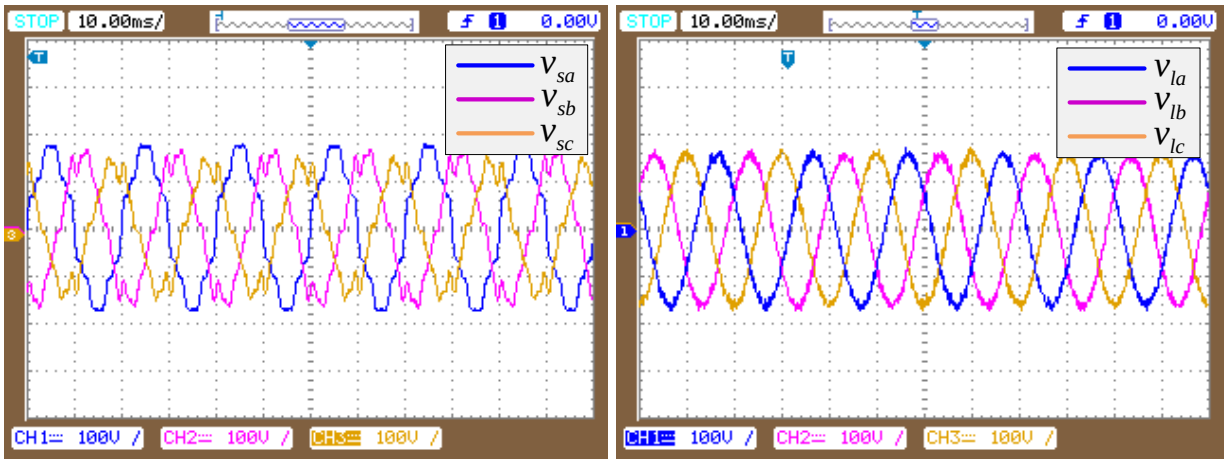
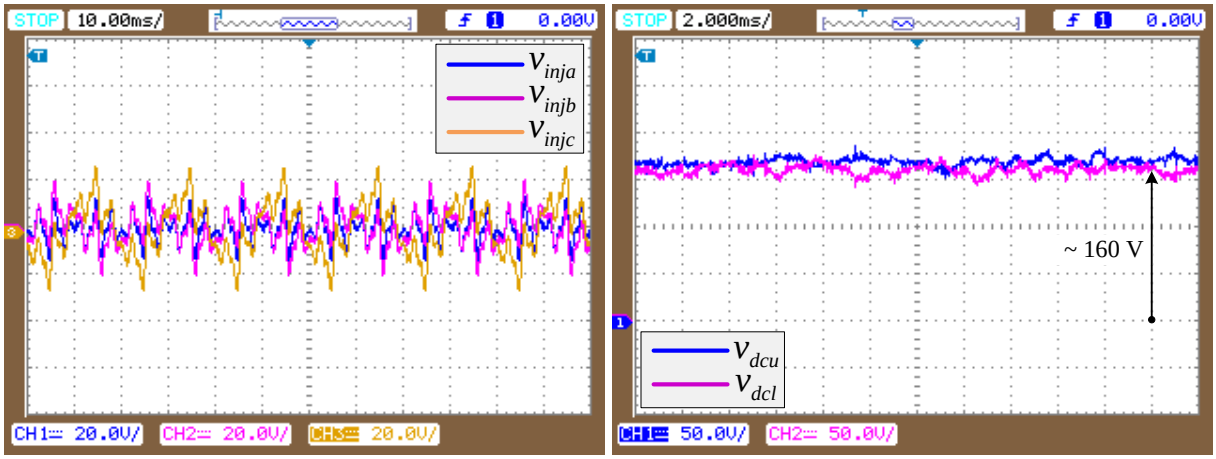


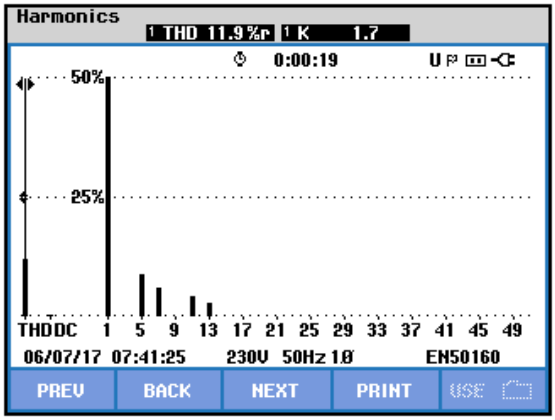
Fig. 2.87: (a). Unbalanced distorted three-phase source voltages and (b). load voltages after compensation with UPQC-3L



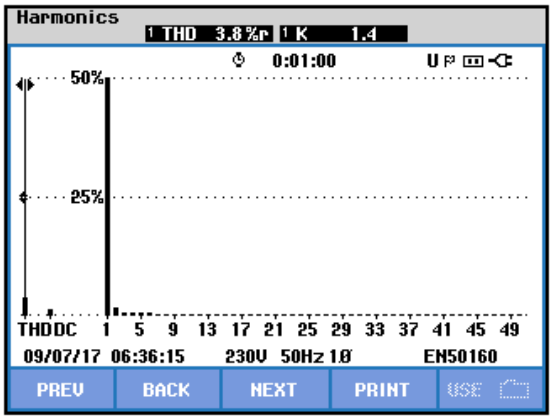
(a) (b)

Fig. 2.88: (a). Three-phase series injected voltages and (b). dc link voltage during case-5 by UPQC-3L

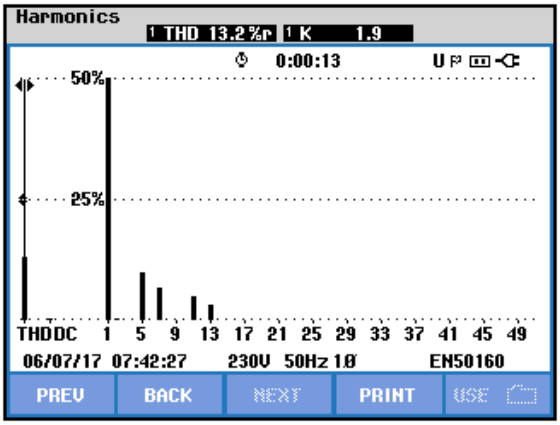
The quantitative comparison of peak fundamental phase magnitude and THDs of load voltage at PCC between UPQC-2L and UPQC-3L for this case study is given in Table 2.9, where the results are considered from the simulation results. The load voltage magnitudes are compared with the rated phase peak fundamental value of 163.3 V. From this comparison, it can be concluded that the compensating performance of UPQC-3L is slightly better than UPQC-2L.



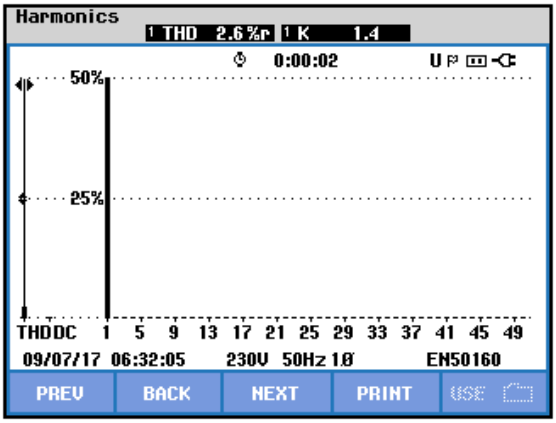
(a)



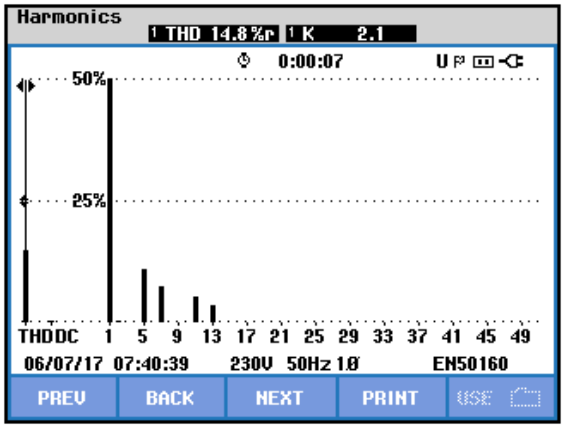
(d)



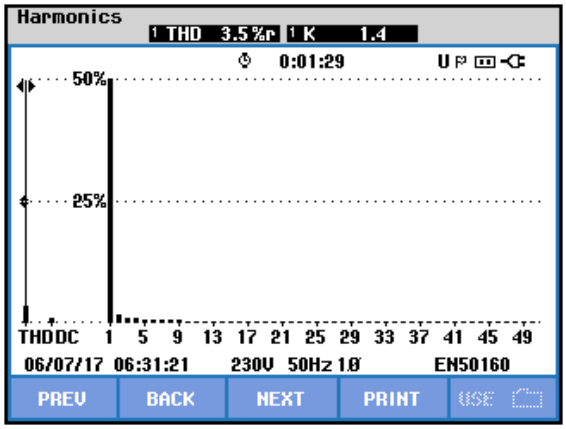
(b)



(e)



(c)



(f)

Fig. 2.89: Harmonic spectrum of voltages: (a)-(c) three-phase source voltage; (d)-(f) three-phase load voltage

(C) Summary

Table 2.9: Comparison of three-phase peak fundamental value and THDs between UPQC-2L and UPQC-3L for distorted unbalancing voltage compensation

Type of disturbance (Voltage unbalanced distortion)	**UPQC-2L**		**UPQC-3L**	
	Load voltage magnitude (V) (Phase-*a*,*b*,*c*)	Load voltage THD (%) (Phase-*a*,*b*,*c*)	Load voltage magnitude (V) (Phase-*a*,*b*,*c*)	Load voltage THD (%) (Phase-*a*,*b*,*c*)
Before compensation	162.04, 141.35, 112.41	18.55, 23.51, 26.23	162.04, 141.35, 112.41	18.55, 23.51, 26.23
After compensation	160.0, 159.8, 159.2	4.11, 4.26, 4.52	162.4, 161.8, 160.5	2.97, 2.44, 3.25

2.5.6 Case-6: Reactive Power Compensation

Apart from the voltage distortions and non-linear load, the performance of UPQC is evaluated with linear load to analyse the reactive power compensation. The following results shown for before and after effects of connecting UPQC into the system. The various cases of loading conditions are considered such as linear, non-linear, unbalanced linear and non-linear loads. The load parameters of linear and non-linear are selected based on the parameters listed in Table 2.4. Figure 2.90 shows the simulated results with linear load, where axis-1 refers to the source voltage and current waveforms of phase-*a*; axis-2: compensating current of phase-*a*; axis-3: dc-link voltage. Before UPQC connected to the system, the source current is sinusoidal because of the linear load but its lagging the source voltage refers to lagging power factor. The shunt compensating current is zero and dc-link voltage starts falling from the pre-set value (330V for UPQC-2L), which is initiated in the simulation.

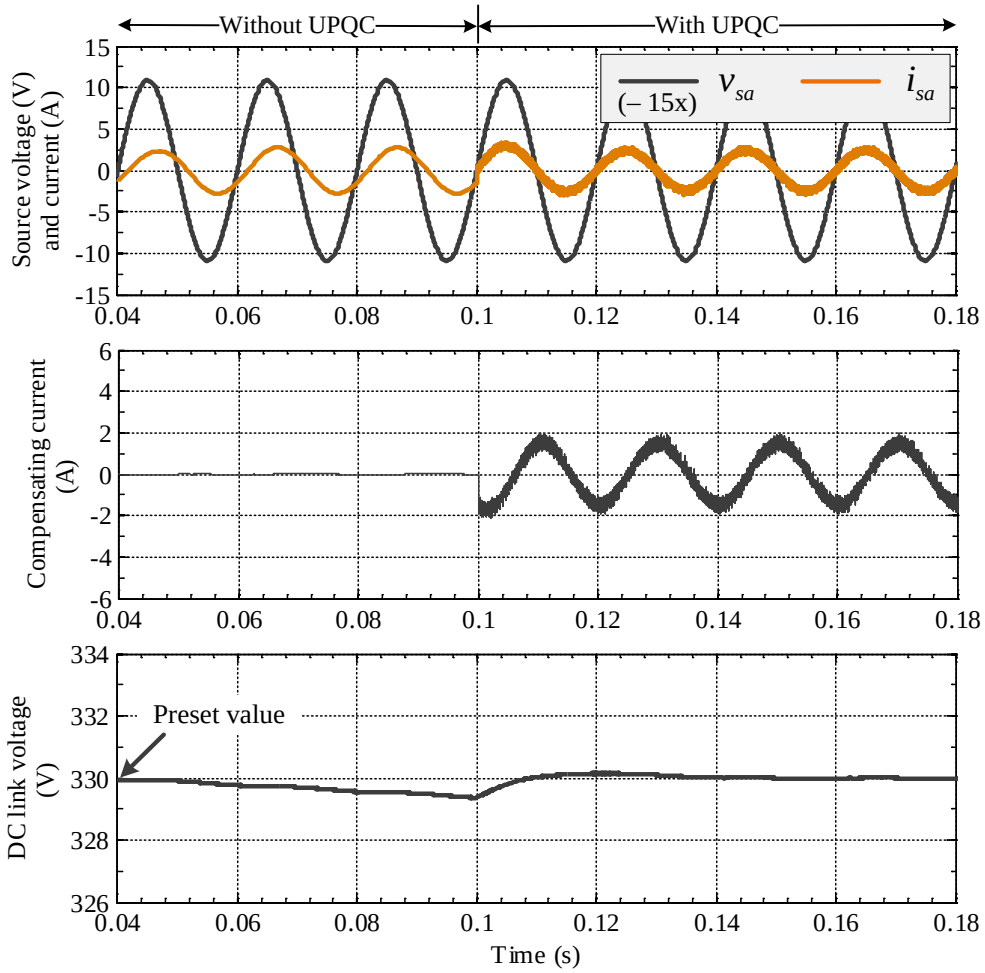
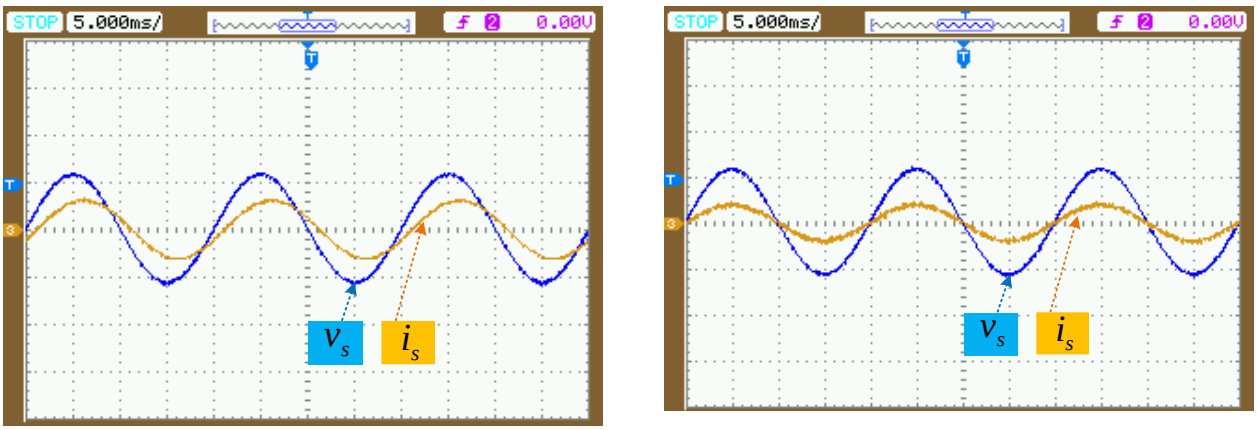


Fig. 2.90: Linear load current compensation (three-phase RL load) by shunt converter of UPQC-2L

The dc-link voltage is taken into control to maintain at reference value of 330V by the PI controller, which is implemented in the shunt converter control strategy. The experimental scope results are presented in Figure 2.91 to justify the simulation results. The similar response can be observed with non-linear loading condition also.



(a) (b)

Fig. 2.91: Phase-*a* source voltage and current (a) before compensation; (b) after compensation with UPQC-2L with linear load

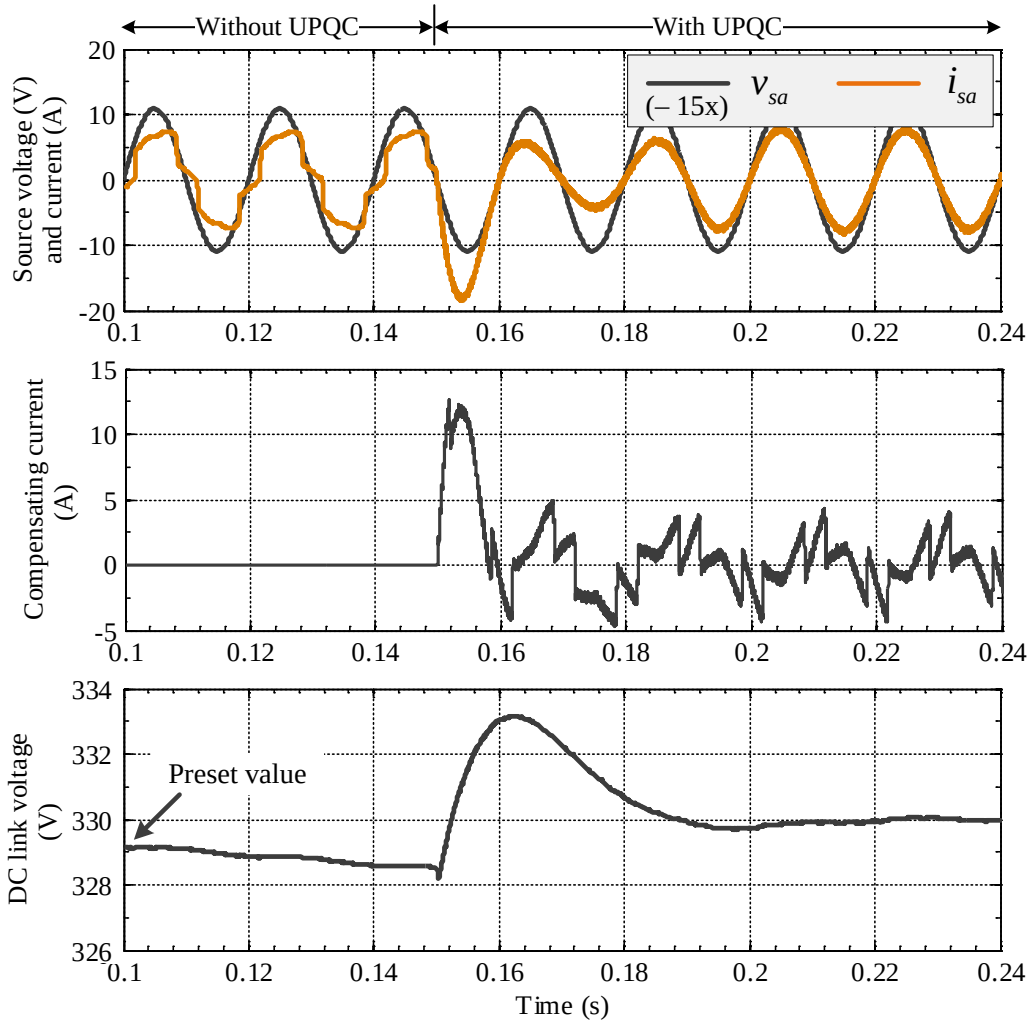


Fig. 2.92: Nonlinear load current compensation (three phase bridge rectifier fed RL load) by shunt converter of UPQC-2L

When the UPQC is connected at t =0.1s, proper amount of shunt compensating current is injected into the PCC, such that forcing source current to follow the voltage with in-phase relation to achieve unity power factor.

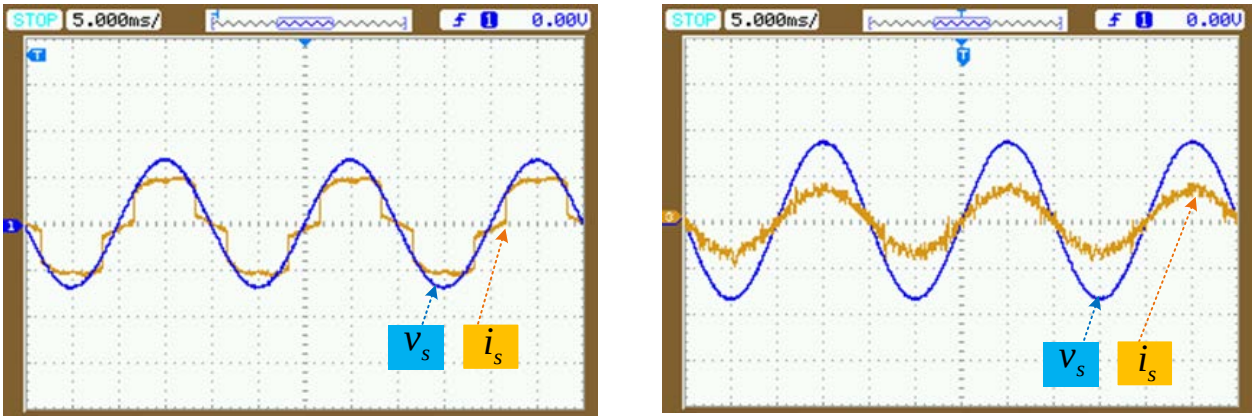


Fig. 2.93: Phase-*a* source voltage and current (a) before compensation; (b) after compensation with UPQC-2L with non-linear load.

The most commonly used type of non-linear load is considered for the evaluation that is the three-phase diode bridge rectifier fed RL load. Figure 2.92 and 2.93 shows the simulation and experiment results with non-linear loading condition respectively. The performance characteristics of UPQC-3L is not presented in this case as the subsection 2.5.6 intended to provide the waveform nature characteristics instead of quantitative analysis to justify the phase relation between source voltage and current waveforms.

2.6 Conclusion

The performance analysis of UPQC is carried out in terms of inverter topology, such as two-level and three-level inverters based UPQC structures (UPQC-2L and UPQC-3L). Both the topologies are subjected to various power quality problems with same control strategy (*d-q* theory). It can be concluded from the simulation/experimental results that the application of UPQC-3L over UPQC-2L provides the better compensation characteristics in overall all types of voltage and current distortions. However, the size and weight of UPQC-3L is more due to increased number of devices as compared to UPQC-2L. The source current measurements from compensation characteristics shows the increased value as compared to UPQC-2L, which leads to make higher active power losses in UPQC-3L.

CHAPTER 3: SIMPLIFIED MODEL PREDICTIVE CONTROL OF UPQC

This chapter describes the application of model predictive control approach to unified power quality conditioner. The advantages of model predictive control over exiting control strategies are discussed and then a new approach is proposed to simplify the model predictive control. To verify the effectiveness of the proposed control scheme, it is applied for UPQC with two-level and three-level inverter structures. Next, the comparative performance analysis is presented for both topology structures. The validation of simulations are carried out with experimental work.

3.1 Introduction

Control strategy is the heart of any power electronics based system. It is the control strategy which decides the behaviour and the desired operation of a particular device. The effectiveness of the APF system (shunt, series or UPQC) solely depends upon its control algorithm. Many methods are implemented to control the switches of the voltage source inverter (VSI) among which pulse width modulation, hysteresis controller, sliding mode controller are to be named as few [9]. In case of UPQC, the control strategy determines the reference signals (current and voltage) and thus decides the switching instants of inverter switches, such that the desired performance can be achieved. One of the distinguishing features of APF is that it does not consume any active power from the source. However, in actual practice there is always some power consumption to overcome the switching losses. There are many control strategies that can be used for UPQC, such as, Instantaneous Reactive Power Theory (or Three-phase *p-q* Theory), Synchronous Reference Frame Method (*d-q* Theory), Deadbeat control, Fuzzy Logic control, Artificial Neural Network (ANN) based control, Symmetrical Component Theory, model predictive control etc. The UPQC controller can be based on one or a combination of the above control strategies. The simplest strategy uses PI controllers in a stationary frame to generate the reference signal for a PWM modulator. However, since the reference signals are periodical quantities containing harmonics, this approach is unable to achieve satisfactory reference tracking performances. The tracking accuracy for specified harmonics may be improved by using multiple related synchronous reference frames [102], [191]. Nevertheless, the interactions among different channels including necessary band-pass filters, make the design and tuning of the whole control system a rather difficult task. Alternatively, a resonant control approach may be used [182] in order to avoid the computational burden involved with frame transformations (presenting however tendency to instability for large parameter variation), or dead beat control strategies [123].

In recent years, Model Predictive Control (MPC) has been applied for the control of power converters due to its several advantages. Predictive control scheme is found afresh in pertinence to the control of power electronics convertor as single phase and three phase VSIs, rectifiers, active power filters, UPS, DC-DC converter, motor drive and power factor

correction [56], [100]–[219]. Algorithms that encompasses real-time optimizations, predictive control has been a recent choice due to its swift dynamic response, simple implementation concept and its ability to deal with nonlinearities and constraints [234–237]. Direct supplication of control action to the converter without the need of modulating stages is the foremost advantage of this method [241]. Lately cost function finite control set model predictive control (FCS–MPC) found utilization in power electronics [255]. This approach acknowledges the converter as a system comprising of restricted number of possible states (voltage vectors). The approach also considers the selection of each sample period and the voltage vector, which reduces a certain cost function to minimum. The cost function describes the covet demeanour of the system and can include different variables to be controlled. The idiosyncrasy was also revised in earlier studies [262], where, in order to reduce the switching frequency of high power inverters, predictive control was employed. The foretasted property is further employed for evaluation of behaviour of the current error for each switching state as represented in [154] for a single phase active filter. Similar studies adopting the scheme is presented in [149] for current control in three phase inverter, matrix converter [215], flux and torque control of induction machine [156] and direct power control in an active front end rectifier. [197].

The model predictive control (MPC) proposed for UPQC by Zhang et al. [125] allows the possibility of considering system dynamics, control objectives and constrains. Multivariable control schemes with comparatively trivial online computation has been studied by Li et al. Multi-input multi-output system has been employed for modelling of UPQC alongside coupling effect between series and shunt inverters. The only task has been considered as compensation of harmonics such that simple Kalman filters were employed. Kalman filters were utilized to deal with compensation of harmonics enabling it to extricate harmonics in supply voltage/ load current [59], [106], [125]. An H∞-based model matching control have been implemented in [62] to track the inverter output waveforms for effective control of UPQC. A Model based solution by means of H∞ loop shaping for UPQC was proposed by Kwan et al. [106]. The Method uses two Kalman filters for UPQC. One to pluck the desired fundamental component and second to behave as a state observer for multi-variable regulator (MVR). The fruitful action of second Kalman filter would generate the switching schemes for consolidated series and shunt active filter, which would in turn compensate supply voltage harmonics, load current harmonics in synchrony with under balanced and unbalanced system operating conditions. Thus, the system control becomes more complex which may increases the computational burden on the processor.

This chapter presents the simplified model predictive control excluding the complex multivariable calculations, in which predictive voltage control for series converter to maintain a constant value of load voltage during voltage disturbances and predictive current control for

shunt converter to maintain source current free from distortions. The sensed voltage and current signals of source and load are used to derive the future predicted values of source current and load voltage from the discrete state space model of UPQC. The appropriate switching state is selected and applied to the converters based on the minimization of the cost function, which is selected as the square of the difference between reference and predicted values. The study is also extended to the another topology i.e. UPQC-ML with three-level inverters.

3.2 Model Predictive Control

Predictive control covers a very wide class of controllers that have found rather recent application in power converters. Predictive control is classified into four major categories. They are, deadbeat control, hysteresis based predictive control, trajectory based predictive control and model predictive control (MPC). The main characteristic of predictive control is the use of a model of the system for predicting the future behaviour of the controlled variables. This information is used by the controller to obtain the optimal actuation, according to a predefined optimization criterion. The optimization criterion in hysteresis-based predictive control is to keep the controlled variable within the boundaries of a hysteresis area [2], while in trajectory-based control the variables are forced to follow a predefined trajectory [3]. In deadbeat control, the optimal actuation is the one that makes the error equal to zero in the next sampling instant [244], [245]. A more flexible criterion is used in model predictive control (MPC), expressed as a cost function to be minimized [256]. The difference between these groups of controllers is that deadbeat control and MPC with continuous control set need a modulator in order to generate the required voltage. This will result in having a fixed switching frequency. The other controllers directly generate the switching signals for the converter, do not need a modulator, and will present a variable switching frequency. One advantage of predictive control is that concepts are very simple and intuitive.

MPC is one that has been successfully used in industrial applications [227]–[229]. Although the ideas of MPC were developed in the 1960s as an application of optimal control theory, industrial interest in these ideas started in the late 1970s [210]. Since then, MPC has been successfully applied in the chemical process industry, where time constants are long enough to perform all the required calculations. Early applications of the ideas of MPC in power electronics can be found from the 1980s considering high-power systems with low switching frequency [218]. The use of higher switching frequencies was not possible at that time due to the large calculation time required for the control algorithm. However, with the development of fast and powerful microprocessors, interest in the application of MPC in power electronics has increased considerably over the last decade. MPC can be employed with either continuous control set or with finite control set. In case of continuous control set, a

modulator is required, however some implementations of MPC can be more complex if the continuous control set is considered.

In the design stage of finite control set MPC for the control of a power converter, the following steps are identified:

- Modelling of the power converter identifying all possible switching states and its relation to the input or output voltages or currents.
- Defining a cost function that represents the desired behaviour of the system.
- Obtaining discrete-time models that allow one to predict the future behaviour of the variables to be controlled.

The total number of switching states of a power converter is equal to the number of different combinations of the two switching states of each switch i.e. on and off. For example a three-phase, two-level inverter has 8 possible switching states, a three-phase, three-level inverter has 27 switching states. The cost function can be designed with the control requirements of application such as current control, voltage control, power control, torque control, etc. The most basic cost function to be defined as error between a reference and a predicted variable. In order to deal with the different units and magnitudes of the controlled variables, each term in the cost function is multiplied by a weighting factor that can be used to adjust the importance of each term. When building the model for prediction, the controlled variables must be considered in order to get discrete-time models that can be used for the prediction of these variables. To get a discrete-time model it is necessary to use some discretization methods. For first-order systems it is useful, because it is simple, to approximate the derivatives using the Euler forward method, that is, using

$$\frac{dx}{dt} = \frac{x(k+1) - x(k)}{T_s} \tag{3.1}$$

where T_S is the sampling time. However, when the order of the system is higher, the discrete-time model obtained using the Euler method is not so good because the error introduced by this method for higher order systems is significant. For these higher order systems, an exact discretization must be used. Figure 3.1 shows the general MPC scheme applied for power converter.

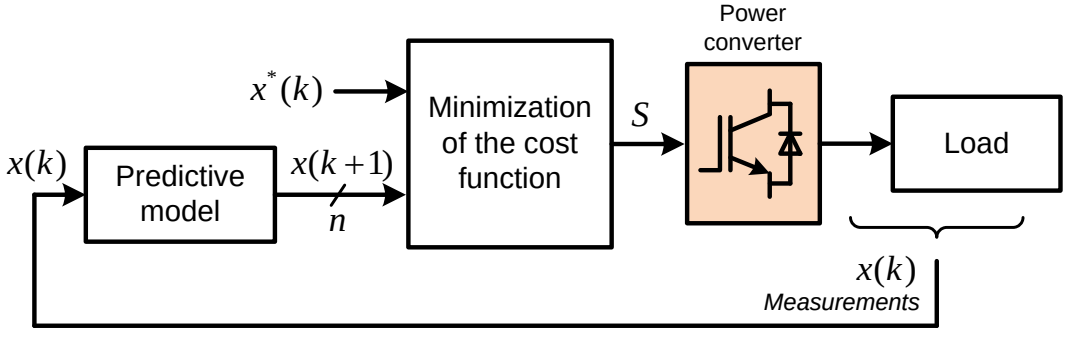


Fig. 3.1: General MPC scheme

The power converter can be from any topology and number of phases, while the generic load shown in the figure can represent an electrical machine, the grid, or any other active or passive load. In this scheme measured variables $x(k)$ are used in the model to calculate predictions $x(k+1)$ of the controlled variables for each one of the *n* possible actuations, that is, switching states, voltages, or currents. Then these predictions are evaluated using a cost function, which considers the reference values $x^*(k)$ and restrictions, and the optimal actuation is selected and applied in the converter.

3.3 UPQC System Model Description

UPQC comprises of series and shunt voltage source converters interleaved via common dc link as depicted in Figure 2.1 [3]. The series converter is connected in series with the distribution system, which supplies power to the load using an injection transformer and LC filter. The shunt converter is connected in parallel to the load side through a coupling inductor L_{sh}. Figure 3.2 shows the single-phase equivalent circuit of UPQC, where source voltage and current are represented by v_s and i_s respectively and load voltage and current are represented by v_l and i_l respectively. The series converter is modelled by $V_{dc}u_1$ and its allied LC filter and losses are modelled by L_{se}, C_{se}, and R_{se}. The switched voltage across shunt converter is modelled by $V_{dc}u_2$ and L_{sh} and R_{sh} are the coupling inductor and losses of the shunt converter respectively. The injected voltage of the series converter is modelled as v_{inj}, while i_{sh} is the injected compensating current by the shunt converter.

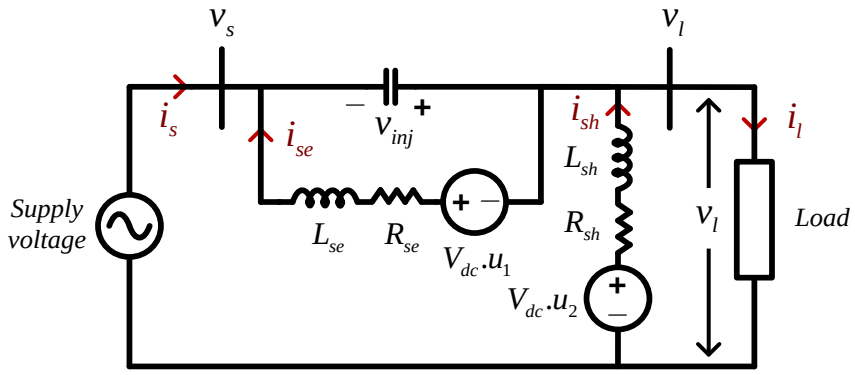


Fig. 3.2: Single-phase equivalent model of UPQC-2L

3.4 Discrete-Time Model for Predictive Control Strategy

The flow of the UPQC is represented by the following differential equations from the single-phase equivalent circuit as shown in Figure 3.2. The state variables are current through filter inductor in the series converter, injected compensating current by the shunt converter and series injected voltage.

$$\frac{di_{se}}{dt} = \frac{V_{dc}.u_1}{L_{se}} - \frac{R_{se}}{L_{se}} i_{se} + \frac{v_{inj}}{L_{se}} \tag{3.2}$$

$$\frac{di_{sh}}{dt} = \frac{v_l}{L_{sh}} - \frac{V_{dc}.u_2}{L_{sh}} - \frac{R_{sh}}{L_{sh}} i_{sh} \tag{3.3}$$

$$\frac{dv_{inj}}{dt} = -\frac{1}{C_{se}} i_s - \frac{1}{C_{se}} i_{se} \tag{3.4}$$

Where i_{se} is the current flowing through R_{se} and L_{se} of the series converter, u_1 and u_2 represent the switching variable of series and shunt converters respectively.

From (3.2)–(3.4), the following state-space representation of the system and its state vector can be derived as

$$\dot{x} = Ax + B_1 u + B_2 z \tag{3.5}$$

Where, $\dot{x} = \begin{pmatrix} \dot{i}_{se} & \dot{i}_{sh} & \dot{v}_{inj} \end{pmatrix}^T$; $x = \begin{pmatrix} i_{se} & i_{sh} & v_{inj} \end{pmatrix}^T$; $u = \begin{pmatrix} u_1 & u_2 \end{pmatrix}^T$; $z = \begin{pmatrix} v_L & i_s \end{pmatrix}^T$;

$$A = \begin{pmatrix} -\frac{R_{se}}{L_{se}} & 0 & \frac{1}{L_{se}} \\ 0 & -\frac{R_{sh}}{L_{sh}} & 0 \\ -\frac{1}{C_{se}} & 0 & 0 \end{pmatrix}; \; B_1 = \begin{pmatrix} \frac{V_{dc}}{L_{se}} & 0 & 0 \\ 0 & -\frac{V_{dc}}{L_{sh}} & 0 \end{pmatrix}^T; \; B_2 = \begin{pmatrix} 0 & \frac{1}{L_{sh}} & 0 \\ 0 & 0 & -\frac{1}{C_{se}} \end{pmatrix}^T$$

The state space form (3.5) at $(k+1)$ sampling instant with sampling time of T_s can be represented as

$$x(k+1) = A_m x(k) + B_{1m} u(k) + B_{2m} z(k) \tag{3.6}$$

Where A_m, B_{1m}, and B_{2m} are the state space matrices and which are deduced as follows,

$$A_m = \begin{pmatrix} \alpha_{11} & \alpha_{12} & \alpha_{13} \\ \alpha_{21} & \alpha_{22} & \alpha_{23} \\ \alpha_{31} & \alpha_{32} & \alpha_{33} \end{pmatrix} = e^{AT_s} \approx I + AT_s + \frac{A^2 T_s}{2}$$

$$= \begin{pmatrix} 1 - \frac{R_{se}T_s}{C_{se}} + \frac{R_{se}^2 T_s}{2L_{se}^2} - \frac{T_s}{2L_{se}C_{se}} & 0 & \frac{T_s}{L_{se}} - \frac{R_{se}T_s}{2L_{se}^2} \\ 0 & 1 - \frac{R_{sh}T_s}{L_{sh}} + \frac{R_{sh}^2 T_s}{2L_{sh}} & 0 \\ -\frac{T_s}{C_{se}} + \frac{R_{se}T_s}{2L_{se}C_{se}} & 0 & -\frac{T_s}{2L_{se}C_{se}} \end{pmatrix} \tag{3.7}$$

$$B_{1m}=\begin{pmatrix}\beta_{11} & \beta_{12}\\ \beta_{21} & \beta_{22}\\ \beta_{31} & \beta_{32}\end{pmatrix}=\int_0^{T_s} e^{A\lambda}B_1 d\lambda \approx \int_0^{T_s}(I+A\lambda)B_1 d\lambda;$$

$$=\begin{pmatrix}\frac{V_{dc}T_s}{L_{se}}-\frac{R_{se}V_{dc}T_s^2}{2L_{se}^2} & 0\\ 0 & \frac{R_{sh}V_{dc}T_s^2}{2L_{sh}^2}\\ -\frac{V_{dc}T_s^2}{2L_{se}C_{se}} & 0\end{pmatrix}; \tag{3.8}$$

$$B_{2m}=\begin{pmatrix}\gamma_{11} & \gamma_{12}\\ \gamma_{21} & \gamma_{22}\\ \gamma_{31} & \gamma_{32}\end{pmatrix}=\int_0^{T_s} e^{A\lambda}B_2 d\lambda \approx \int_0^{T_s}(I+A\lambda)B_2 d\lambda$$

$$=\begin{pmatrix}0 & -\frac{T_s^2}{2L_{se}C_{se}}\\ -\frac{R_{sh}T_s^2}{2L_{sh}^2} & 0\\ 0 & -\frac{T_s}{C_{se}}\end{pmatrix}; \tag{3.9}$$

The predicted value of the current through the series filter, series injected voltage and injected current by the shunt converter are derived in discrete state space domain as follows,

$$\left.\begin{aligned} i_{se}(k+1)=\alpha_{11}i_{se}(k)+\alpha_{12}i_{sh}(k)+\alpha_{13}v_{inj}(k)+\\ \beta_{11}u_1(k)+\beta_{12}u_2(k)+\gamma_{11}v_l(k)+\gamma_{12}i_s(k)\end{aligned}\right\} \tag{3.10}$$

$$\left.\begin{aligned} i_{sh}(k+1)=\alpha_{21}i_{se}(k)+\alpha_{22}i_{sh}(k)+\alpha_{23}v_{inj}(k)+\\ \beta_{21}u_1(k)+\beta_{22}u_2(k)+\gamma_{21}v_l(k)+\gamma_{22}i_s(k)\end{aligned}\right\} \tag{3.11}$$

$$\left.\begin{aligned} v_{inj}(k+1)=\alpha_{31}i_{se}(k)+\alpha_{32}i_{sh}(k)+\alpha_{33}v_{inj}(k)+\\ \beta_{31}u_1(k)+\beta_{32}u_2(k)+\gamma_{31}v_l(k)+\gamma_{32}i_s(k)\end{aligned}\right\} \tag{3.12}$$

On substituting zero valued coefficients of α, β and γ (3.10)–(3.12) can be rewritten as

$$i_{se}(k+1)=\alpha_{11}i_{se}(k)+\alpha_{13}v_{inj}(k)+\beta_{11}u_1(k)+\gamma_{12}i_s(k) \tag{3.13}$$

$$i_{sh}(k+1)=\alpha_{22}i_{sh}(k)+\beta_{22}u_2(k)+\gamma_{21}v_L(k) \tag{3.14}$$

$$v_{inj}(k+1)=\alpha_{31}i_{se}(k)+\alpha_{33}v_{inj}(k)+\beta_{31}u_1(k)+\gamma_{32}i_s(k) \tag{3.15}$$

3.4.1 Selection of Cost Function and Optimization

(A) Defining Cost Function for UPQC-2L

In case of UPQC-2L, there are eight possible switching states for each of the two-level inverter of the series and shunt converter. The switching states of two-level inverter are explained in the Section 2.2.1.1. The predictive value of shunt current ($i_{sh}(k+1)$) and series injected voltages ($v_{inj}(k+1)$) are evaluated for each of the possible switching state. In order to build the cost function, reference values should be evaluated at (k+1) instant. The reference values ($i_{sh}^{*}(k), v_{inj}^{*}(k)$) for both predictive values are generated as explained in the next section at k^{th} instant. However, the future reference value required by cost function at (k+1) instant is unknown. Once the references are obtained in k^{th} instant, they must be extrapolated to (k+1) instant for the use with cost function. When the sampling time T_s is sufficiently small (<20μs), no extrapolation is required. In this case, $i_{sh}^{*}(k+1) = i_{sh}^{*}(k)$ and $v_{inj}^{*}(k+1) = v_{inj}^{*}(k)$. When the sampling time T_s is greater than 20μs, the following fourth-order Lagrange extrapolation [232] can be used:

$$i_{sh}^{*}(k+1) = 3i_{sh}^{*}(k) - 3i_{sh}^{*}(k-1) + i_{sh}^{*}(k-2) \tag{3.16}$$

$$v_{inj}^{*}(k+1) = 3v_{inj}^{*}(k) - 3v_{inj}^{*}(k-1) + v_{inj}^{*}(k-2) \tag{3.17}$$

The cost function (g_i) of the predictive current control is defined as square of difference between the predicted compensating current and actual current of the shunt converter. The cost function of predictive control is illustrated as,

$$g_i(k+1) = \left(i_{sh}^{*}(k+1) - i_{sh}(k+1)\right)^2 \tag{3.18}$$

The cost function (g_v) of the predictive voltage control is square of difference between the voltages of predictive and actual series capacitor of the series converter illustrated as,

$$g_v(k+1) = \left(v_{inj}^{*}(k+1) - v_{inj}(k+1)\right)^2 \tag{3.19}$$

The goal of cost function optimization is to achieve g value close to zero. The voltage vector $u_1(k)$, $u_2(k)$ that minimizes the cost function g_v and g_i is chosen from the SVM block controller as shown in Figure 2.8 for series converter and shunt converter respectively and then applied at the next sampling instant. During each sampling instant, the minimum value of g is selected from the eight function values. At k^{th} instant, the algorithm selects a switching state which would minimize the cost function at the (k+1) instant, and then applies this optimal switching state during the whole (k+1) period.

(B) Defining Cost Function for UPQC-3L

The three-phase three-level diode clamped multi-level inverter generates 27 possible switching states, which produce 19 different voltage vectors. Unlike two-level inverter, three-level diode clamped inverter faces dc-link voltage unbalancing issue across split dc-link

capacitors because of some switching states will have effect on the charging and discharging of the dc-link capacitors as explained in section 2.2.1.2. Therefore, the cost function for UPQC-3L can be designed with including extra control parameter of dc-link balancing in addition to series voltage control and shunt current control parameters. The dynamics of series injection voltage and shunt compensation current of UPQC-2L can be employed to UPQC-3L by considering V_{dc} as the sum of split dc-link capacitor voltages.

$$V_{dc} = V_{dcu} + V_{dcl} \tag{3.20}$$

The dynamics of dc-link capacitor voltages are need to be described by the differential equations to include dc balancing control in the cost function. In general shunt converter of UPQC will take the responsibility to maintain dc-link voltage. Therefore, the differential equations are derived with shunt three-level inverter as shown in Figure 3.2.

$$\frac{dv_{dcu}}{dt} = \frac{1}{C_1} i_{cu} \tag{3.21}$$

$$\frac{dv_{dcl}}{dt} = \frac{1}{C_2} i_{cl} \tag{3.22}$$

Where, C_1 and C_2 are the upper and lower capacitances of the split dc-link can be considered as equal value of C.

$$C_1 = C_2 = C \tag{3.23}$$

The approximation to derivative equations of capacitor voltages can be consider by using the Euler forward method for a sampling time T_s,

$$\frac{dv_{dcx}}{dt} \approx \frac{v_{dcx}(k+1) - v_{dcx}(k)}{T_s} \tag{3.24}$$

This method provides the following discrete-time equations,

$$v_{dcu}(k+1) = v_{dcu}(k) + \frac{1}{C_1} i_{cu}(k) T_s \tag{3.25}$$

$$v_{dcl}(k+1) = v_{dcl}(k) + \frac{1}{C_2} i_{cl}(k) T_s \tag{3.26}$$

Where, currents $i_{cu}(k)$ and $i_{cl}(k)$ depend on the switching state of the three-level diode clamped multilevel inverter and the value of the output currents i_{sh_abc}, and can be calculated using the following expressions.

$$i_{cu}(k) = -\Gamma_{1a} i_{sh\_a}(k) - \Gamma_{1b} i_{sh\_b}(k) - \Gamma_{1c} i_{sh\_c}(k) \tag{3.27}$$

$$i_{cl}(k) = \Gamma_{2a} i_{sh\_a}(k) + \Gamma_{2b} i_{sh\_b}(k) + \Gamma_{2c} i_{sh\_c}(k) \tag{3.28}$$

Where, the variables Γ_{1x} and Γ_{2x} depend on the switching states and are defined as,

$$\Gamma_{1x} = \begin{cases} 1 & \text{if } S_x = \langle + \rangle \\ 0 & \text{otherwise} \end{cases} \tag{3.29}$$

$$\Gamma_{2x} = \begin{cases} 1 & \text{if } S_x = \langle - \rangle \\ 0 & \text{otherwise} \end{cases} \tag{3.30}$$

Where, $x = a, b, c$.

Hence, (3.25)-(3.30) allow to predict the effect of selecting a given switching state on the variation of the capacitor voltages. To compensate the capacitor voltage unbalance, the difference between both capacitors voltages should be minimize and which can be solved through defining cost function.

$$v_{dcu}(k+1) - v_{dcl}(k+1) = v_{dcu}(k) - v_{dcu}(k) + \frac{1}{C} i_c(k) T_s \tag{3.31}$$

Where, total capacitor current $i_c(k)$ is defined as,

$$\begin{aligned} i_c(k) &= i_{cu}(k) - i_{cl}(k) \\ &= \sum_{x=a,b,c} (\Gamma_{2x} - \Gamma_{1x}) i_{sh\_x}(k) \end{aligned} \tag{3.32}$$

The cost function defined as follows with squared error values of the reference and predicted values.

$$g_i(k+1) = \lambda_1 \left(i_{sh}^*(k+1) - i_{sh}(k+1) \right)^2 + \lambda_2 \left\{ v_{dcu}(k+1) - v_{dcl}(k+1) \right\} \tag{3.33}$$

Equation (3.33) show the cost function of shunt converter part of UPQC, which includes the additional term to consider dc-link voltage unbalancing, whereas the cost function can be defined as same as that of two-level inverter based UPQC as (3.19).

The weighting factor λ_1 and λ_2 in (3.33) allows the user definition of the priority levels of current compensation and dc voltage balancing control variable. In general while defining the cost function with different control variables, the errors are weighted by some factors to normalize the distinct errors, which have different units and ranges, and to define the priority level of each error variable. Therefore, these weights are designs of degree of freedom but should be anticipated considering the current and voltages ranges and enforcing, and that allowed errors obey $\lambda_1 e_i^2 \approx \lambda_2 e_{dc}$ to give roughly equal weights to all the controlled variables. Then, in practice, dc capacitor voltage balancing has a lower priority level, so the term $\lambda_2 e_{dc}$ in steady state comparatively should weigh less in cost functional. This means that λ_1 should

be much bigger than λ_2, which must be small (but higher than zero) to give a higher priority level to the controlled currents.

Calculating the cost functional (3.33) and (3.19) at the next sampling period, for the candidate 27 multilevel voltage vectors (Fig. 2.14), the vector showing the minimum value of the cost functional can be found among the available 27 vectors. This optimal vector is chosen and decoded to obtain the IGBTs gate drive signals of the multilevel inverter.

3.4.2 Reference Signal Generation

The Independent generation of reference control signals for both shunt and series converters are performed. The two reference signals are injection voltage by the series transformer into the system, considered for series converter and injectable compensation current by the shunt converter against load distortions, entitled as control reference for shunt converter. The *d-q* method is used as control method with amalgamation of single and three-phase transformation models for series converter.

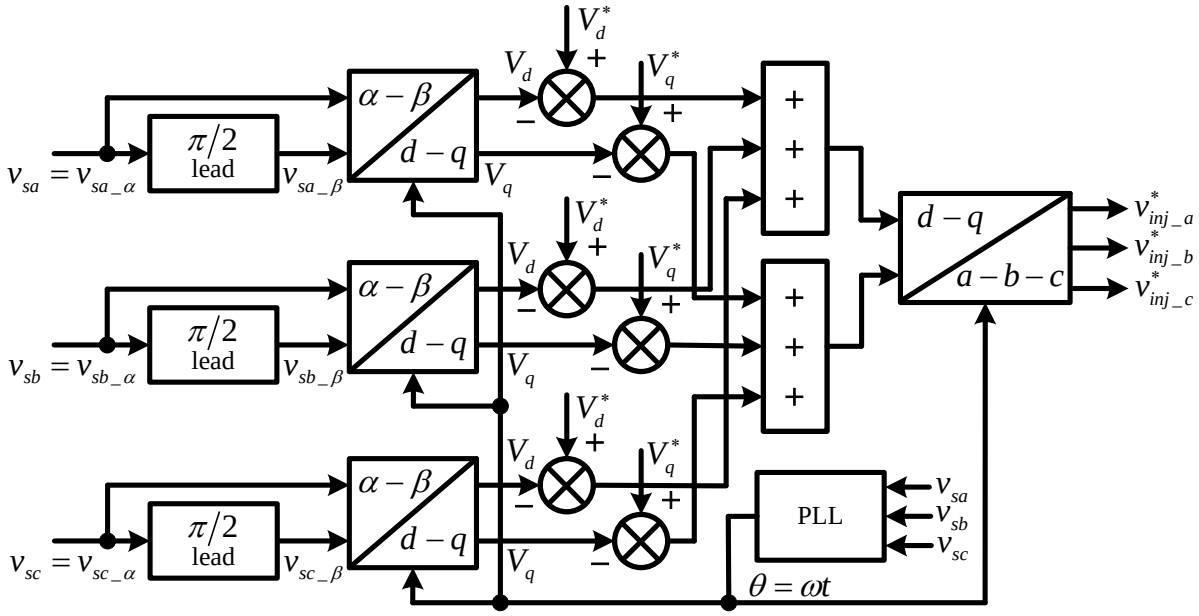


Fig. 3.3: Reference signal generation of series converter

The control block diagram is depicted as in Figure 3.3, which spectacles the generation of reference voltage signal of series converter. Three-phase source voltage is perceived and indoctrinated to virtual orthogonal *α-β* co-ordinates in single-phase manner and then into synchronous *d-q* reference frame.

$$\begin{pmatrix} v_{sa\_\alpha} \\ v_{sa\_\beta} \end{pmatrix} = \begin{pmatrix} v_s(\omega t) \\ v_s(\omega t + \pi/2) \end{pmatrix} \tag{3.34}$$

$$\begin{pmatrix} v_{sa\_d} \\ v_{sa\_q} \end{pmatrix} = \begin{pmatrix} \sin\omega t & -\cos\omega t \\ \cos\omega t & \sin\omega t \end{pmatrix} \cdot \begin{pmatrix} v_{sa\_\alpha} \\ v_{sa\_\beta} \end{pmatrix} \tag{3.35}$$

Segregation of undesirable components from source voltage in *d-q* co-ordinates are executed to preserve the desirable shape and magnitude in spite of gnarled and unbalanced source voltage. To maintain synchronism, phase locked loop (PLL) is used. The reference voltage (v^*_{d-q}) is considered as the expected desirable reference load phase voltage is contemplated such that it possesses only one component out of two in synchronous *d-q* frame as depicted in (3.37).

$$\begin{pmatrix} v^*_{inja\_d} \\ v^*_{inja\_q} \end{pmatrix} = \begin{pmatrix} v^*_{sa\_d} \\ v^*_{sa\_q} \end{pmatrix} - \begin{pmatrix} v_{sa\_d} \\ v_{sa\_q} \end{pmatrix} \tag{3.36}$$

$$\begin{pmatrix} v^*_{sa\_d} \\ v^*_{sa\_q} \end{pmatrix} = \begin{pmatrix} V^*_{mp} \\ 0 \end{pmatrix} \tag{3.37}$$

Where V^*_{mp} is the reference magnitude of the load phase voltage.

$$\begin{pmatrix} v^*_{inj\_d} \\ v^*_{inj\_q} \end{pmatrix} = \begin{pmatrix} v^*_{inja\_d} \\ v^*_{inja\_q} \end{pmatrix} + \begin{pmatrix} v^*_{injb\_d} \\ v^*_{injb\_q} \end{pmatrix} + \begin{pmatrix} v^*_{injc\_d} \\ v^*_{injc\_q} \end{pmatrix} \tag{3.38}$$

$$\begin{pmatrix} v^*_{inj\_a} \\ v^*_{inj\_b} \\ v^*_{inj\_c} \end{pmatrix} = \sqrt{\frac{2}{3}} T^{-1} . \begin{pmatrix} v^*_{inj\_d} \\ v^*_{inj\_q} \end{pmatrix} \tag{3.39}$$

Where, $T^{-1} = \begin{pmatrix} cos\,\omega t & -sin\,\omega t \\ cos\,(\omega t - 2\pi/3) & -sin\,(\omega t - 2\pi/3) \\ cos\,(\omega t - 4\pi/3) & -sin\,(\omega t - 4\pi/3) \end{pmatrix}$

The reference compensating voltage in *d-q* coordinated retrieved for each corresponding voltage are united and further reformed back to three-phase *a-b-c* coordinates. This is performed to fabricate the reference injected voltages by the series converter.

The reference compensating currents for the shunt converter are generated using single-phase instantaneous *p-q* theory [141]. Figure 3.4 represents the block diagram showing the generation of reference signals for shunt converter. The three-phase load voltages and currents are sensed and phase shifted by 90^0 to get virtual orthogonal *α-β* co-ordinates for each phase as given in (3.34). The instantaneous load active and reactive powers are calculated for each phase separately by using voltages and currents derived in *α-β* plane as shown in (3.40).

$$\begin{pmatrix} p_{La} \\ q_{La} \end{pmatrix} = \begin{pmatrix} \overline{p}_{La} + \tilde{p}_{La} \\ \overline{q}_{La} + \tilde{q}_{La} \end{pmatrix} = \begin{pmatrix} v_{La\_\alpha} & v_{La\_\beta} \\ -v_{La\_\beta} & v_{La\_\alpha} \end{pmatrix} . \begin{pmatrix} i_{La\_\alpha} \\ i_{La\_\beta} \end{pmatrix} \tag{3.40}$$

Where, $\bar{p}_{La}$ and $\tilde{p}_{La}$ are the dc and ac components of the fundamental and harmonic load active power of phase-*a*. Similarly $\bar{q}_{La}$ and $\tilde{q}_{La}$ are the fundamental and harmonic load reactive power components of phase-*a*. The shunt converter is aimed to compensate the total load reactive power and harmonic active power drawn from the source and hence provide the balanced source currents the total active and reactive powers are redistributed equally on all phases as given in (3.41) and (3.42).

$$\tilde{p}_{L/ph} = \frac{\tilde{p}_{La} + \tilde{p}_{Lb} + \tilde{p}_{Lc}}{3} \tag{3.41}$$

$$q_{L/ph} = \frac{q_{La} + q_{Lb} + q_{Lc}}{3} \tag{3.42}$$

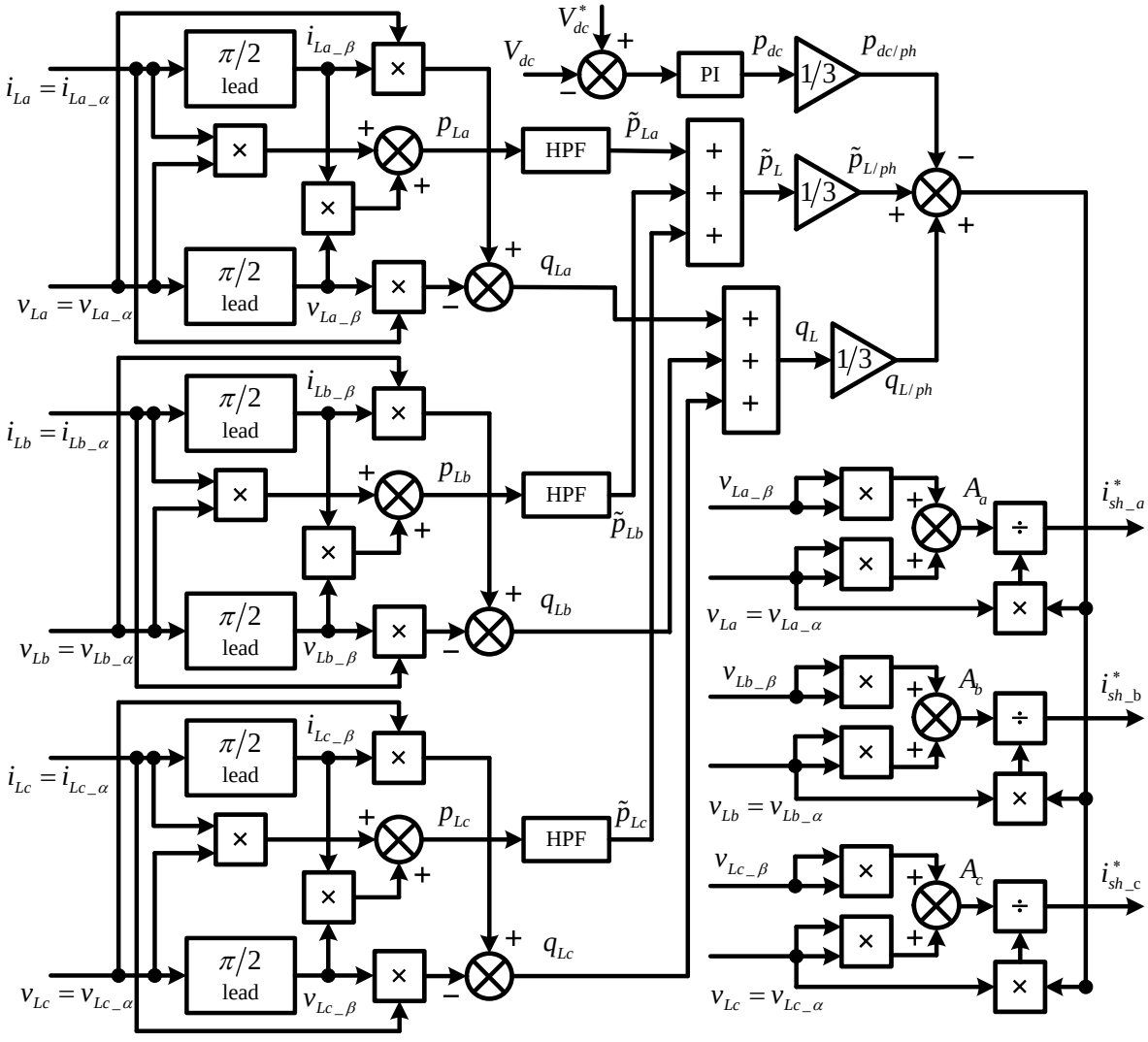


Fig. 3.4: Reference signal generation of shunt converter

The reference shunt compensating currents are deduced from the nonessential instantaneous powers harrowed by the load from source and the required power component to preserve constant dc-link voltage as given in (3.43)–(3.45).

$$i^{*}_{sh\_a}(t)=\frac{v_{La\_\alpha}(t)}{v^{2}_{La\_\alpha}+v^{2}_{La\_\beta}}\left[\tilde{p}_{L/ph}-p_{dc/ph}\right]+\frac{v_{La\_\beta}(t)}{v^{2}_{La\_\alpha}+v^{2}_{La\_\beta}}\left[q_{L/ph}\right] \quad (3.43)$$

$$i^{*}_{sh\_b}(t)=\frac{v_{Lb\_\alpha}(t)}{v^{2}_{Lb\_\alpha}+v^{2}_{Lb\_\beta}}\left[\tilde{p}_{L/ph}-p_{dc/ph}\right]+\frac{v_{Lb\_\beta}(t)}{v^{2}_{Lb\_\alpha}+v^{2}_{Lb\_\beta}}\left[q_{L/ph}\right] \quad (3.44)$$

$$i^{*}_{sh\_c}(t)=\frac{v_{Lc\_\alpha}(t)}{v^{2}_{Lc\_\alpha}+v^{2}_{Lc\_\beta}}\left[\tilde{p}_{L/ph}-p_{dc/ph}\right]+\frac{v_{Lc\_\beta}(t)}{v^{2}_{Lc\_\alpha}+v^{2}_{Lc\_\beta}}\left[q_{L/ph}\right] \quad (3.45)$$

3.5 Simulation and Experimental Results

The proposed predictive control strategy is validated through simulations on MATLAB Simulink platform. Table I shows the parameters of the system selected. The three-phase source voltage is considered as 100V with phase-phase rms value. To authenticate the performance of the prospective control strategy, the UPQC is imposed to voltage sag and swell of 20% magnitude. Further, it is also subjected to distorted voltage in concurrence with nonlinear load.

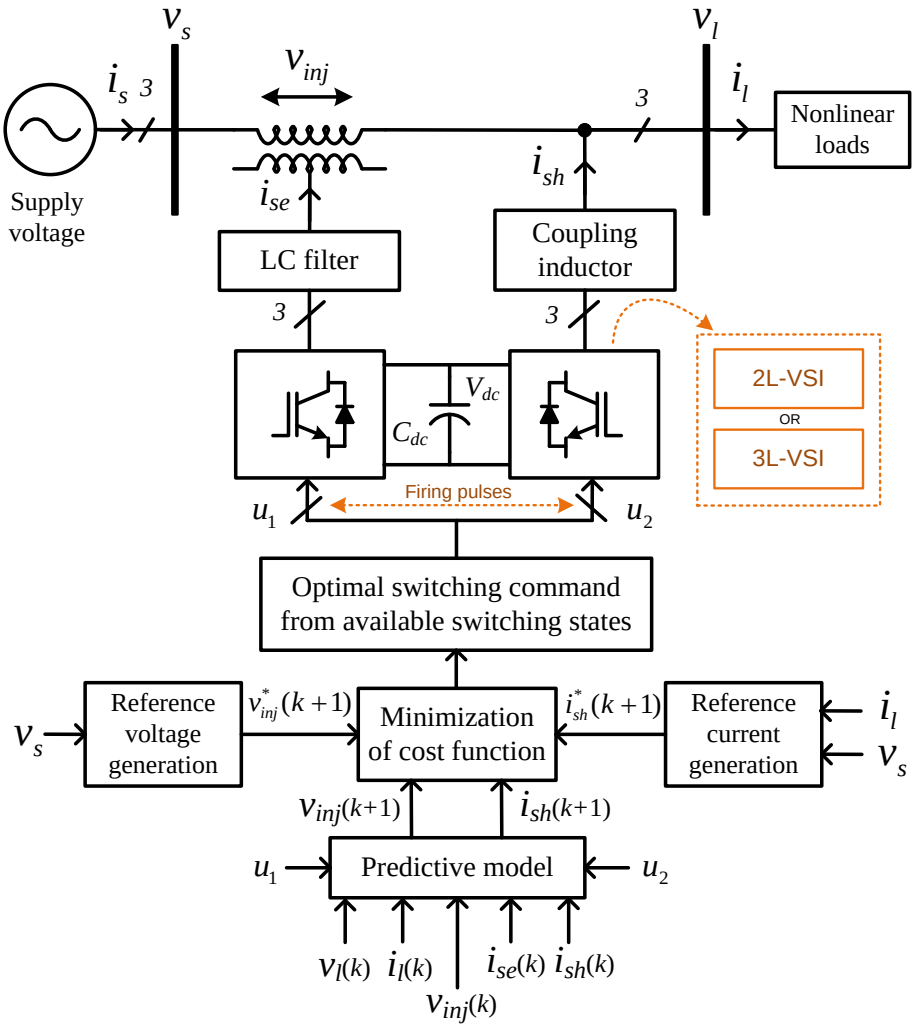


Fig. 3.5: Block diagram of UPQC with MPC control strategy

A sampling time of 50μs (sampling frequency being 20kHz) is considered as it can be conveniently realized through modern DSP processors for practical utility. The validation of simulation results are done with the help of laboratory prototype developed for the previous chapter. Figure 3.5 shows the system block diagram of UPQC with proposed control strategy, where series and shunt converters includes the two-level VSIs for UPQC-2L and three-level VSIs for UPQC-3L. The firing pulses for the switches of VSIs are applied from the selected optimal switching commands, which are filtered out from the available switching states. As discussed in the Chapter 2, eight switching states are available for two-level VSI, whereas 27 states are available for three-level inverter. The optimal switching command is generated from the predictive controller based on the values of predicted signal and reference signal. As described in the above sections, the optimal switching command is generated separately for series and shunt converters by defining separate cost functions related to compensation modes of series and shunt converters of UPQC.

The system parameters for evaluation are selected as shown in Table 3.1. The effectiveness of proposed control strategy is evaluated with UPQC-2L and with UPQC-3L with the same parameters as shown in Table 3.1. The performance comparative analysis is explored between UPQC-2L and UPQC-3L with the simulation results. The experimental results are also discussed in this chapter with proposed control strategy. The details about control board and development of prototype are presented in the Appendix-A.

Table 3.1: System parameters.

Variable	Description	Parameter value
v_{S_L-L}	Three-phase source voltage	100V (L–L rms)
f	Supply frequency	50Hz
T_s	Sampling time	50μs
V_{dc}	DC link voltage (2L)	170V
$V_{dcu};V_{dcl}$	Upper and lower dc link (3L)	85V
C_{dc}	DC link capacitance (2L)	2200μF
$C_1;C_2$	Split DC link capacitance (3L)	1000μF
R_{sh},L_{sh}	Shunt resistance, coupling inductance	0.1Ω, 3mH
R_{se},L_{se},C_{se}	Series resistance and filter components	0.1Ω, 2mH and 20μF
R_{L1},L_{L1}	Three-phase diode rectifier fed RL load	60Ω, 30mH
R_{L2},L_{L2}	Three-phase RL load	110Ω, 30mH

The performance is evaluated with voltage disturbances such as voltage sag, swell, unbalance and unbalanced distorted source voltage; and current related disturbance such as current harmonics generated with non-linear load and reactive power.

3.5.1 Case-1: Distorted Source Voltage and Non-linear Load

The non-linear load is considered with uncontrolled three-phase diode bridge rectifier with RL load and the distorted supply voltage is created with by adding the most dominant harmonic voltages to the fundamental voltage waveform, such as 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics with corresponding magnitudes of $1/5^{th}$, $1/7^{th}$, $1/11^{th}$, and $1/13^{th}$ magnitude of fundamental value.

(A) UPQC-2L

Since the system is assumed to be balanced and the load is also balanced on three-phases of the system, only one phase results are discussed in this chapter. Figure 3.6 shows the simulation results of phase-*a* corresponding voltage compensation characteristics of UPQC-2L under steady state condition.

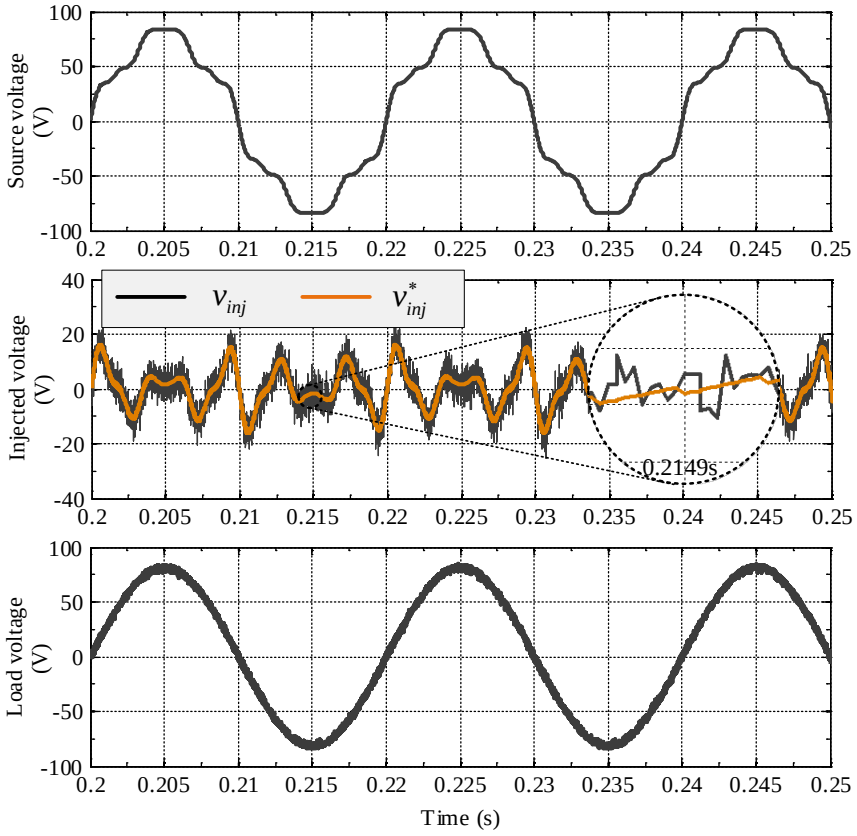


Fig. 3.6: Distorted voltage compensation by the proposed control scheme showing for phase–*a* of UPQC-2L.

The axis-1 shows the source voltage (v_s), which is having phase peak fundamental value of 81.6V with THD of 12.30%. The injected voltage by series converter is shown in axis-2, where the predicted signal is shown with black color and the reference compensating

signal is shown with orange color. The zoomed portion of scope results shows that the predicted value is very close to the reference signal value at a given time to follow the compensation characteristics. The tracking of reference signal by the predicted signal is not continuous in nature, whereas the resolution of tracking is decided by the sampling period (T_s). The smaller the sampling time, the higher the resolution of the reference tracking. However, the sampling period is decided by the controller, which is adopted for the experimental work. At every sampling time, the magnitude of the output of series converter is decided by the switching command that is selected by the predictive voltage controller. The axis-3 of Figure 3.6 shows the load voltage after compensation. The magnitude of phase peak fundamental load voltage is 80.98V, which is almost maintained at the desired value of 81.65V and having THD of 4.51%, which is well within the limits of IEEE–519–1992 recommended value of 5%. The current compensation characteristics of phase-*a* against non-linear load are shown in Figure 3.7. Axis-3 shows the load current of the combination of linear and non-linear load, which is having rms value of 3.53A and %THD of 23.45. The compensating shunt currents are shown in axis-2. As explained for voltage compensation, the predicted shunt compensating current is following the reference compensating current to maintain the source current free from the load harmonics and also to compensate power factor. The source current waveform is shown in axis-1 of Figure 3.7, which is having magnitude and THD of 3.8A and 3.8% respectively.

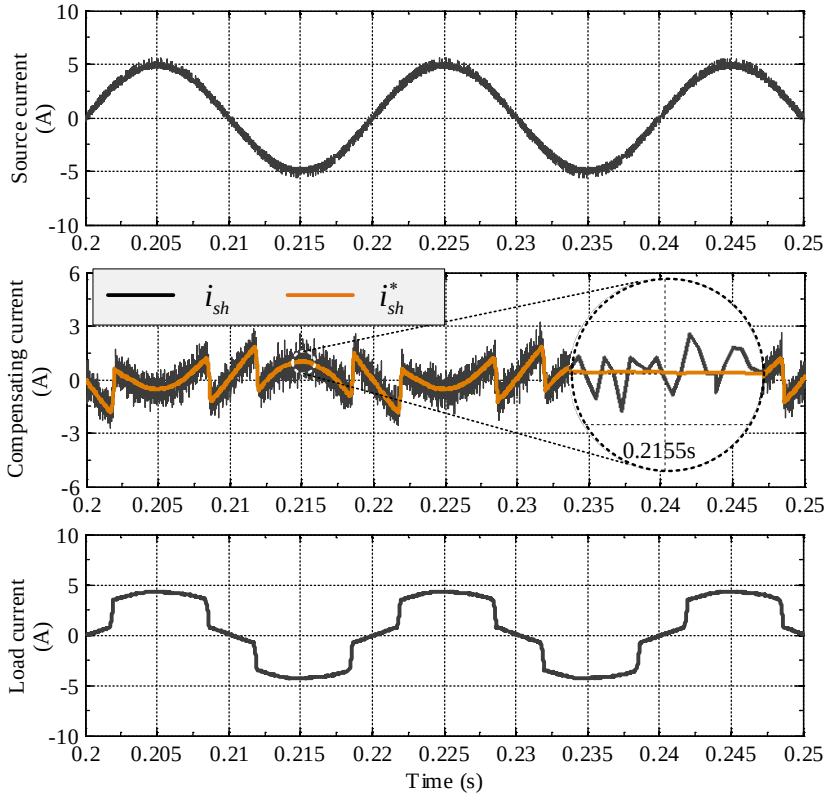
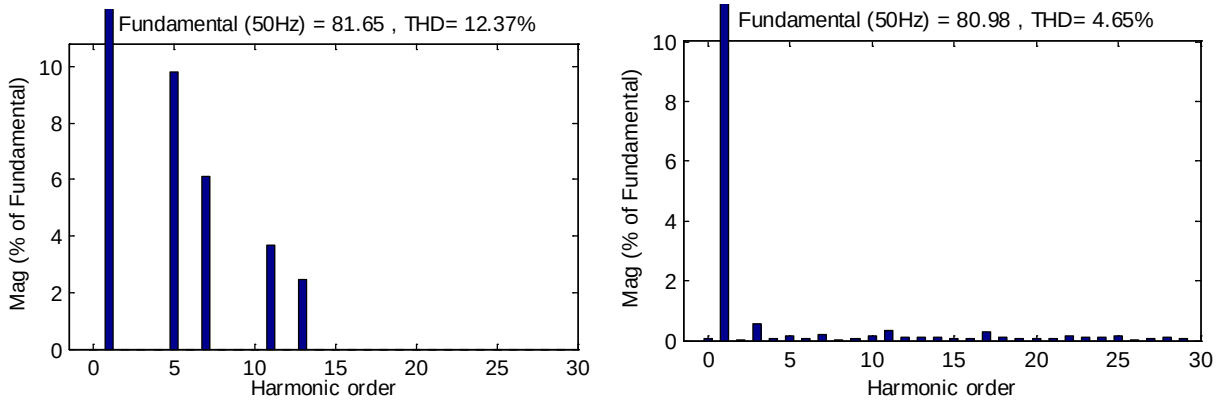
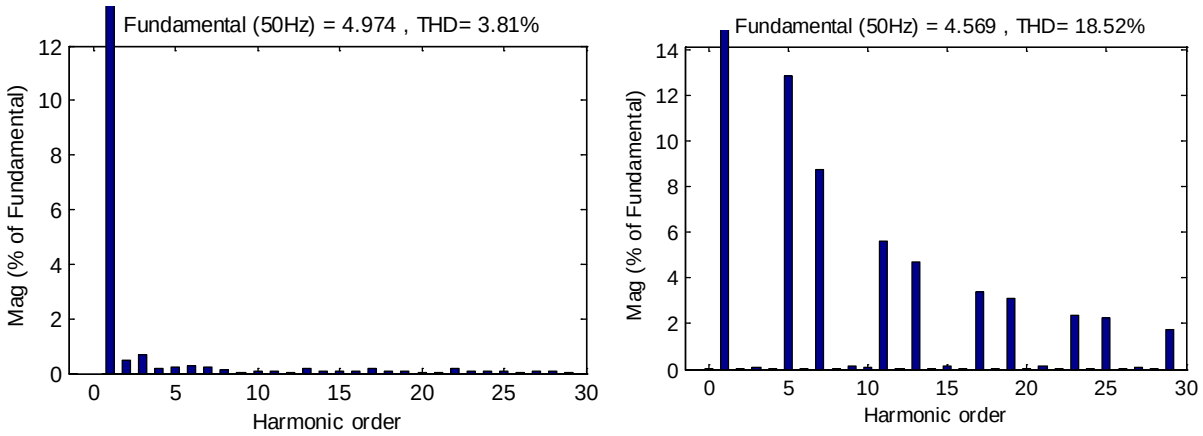


Fig. 3.7: Compensation of source current during distorted voltage along with non-linear load by the proposed control scheme showing for phase-*a* of UPQC-2L.



(a) (b)

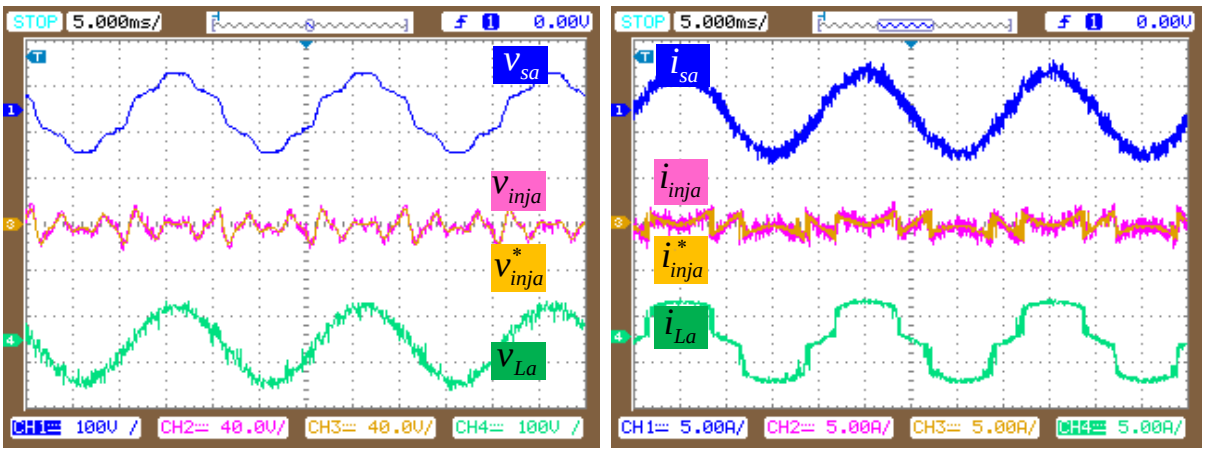
Fig. 3.8: Harmonic spectrum of phase-*a* of (a) source voltage; (b) load voltage



(a) (b)

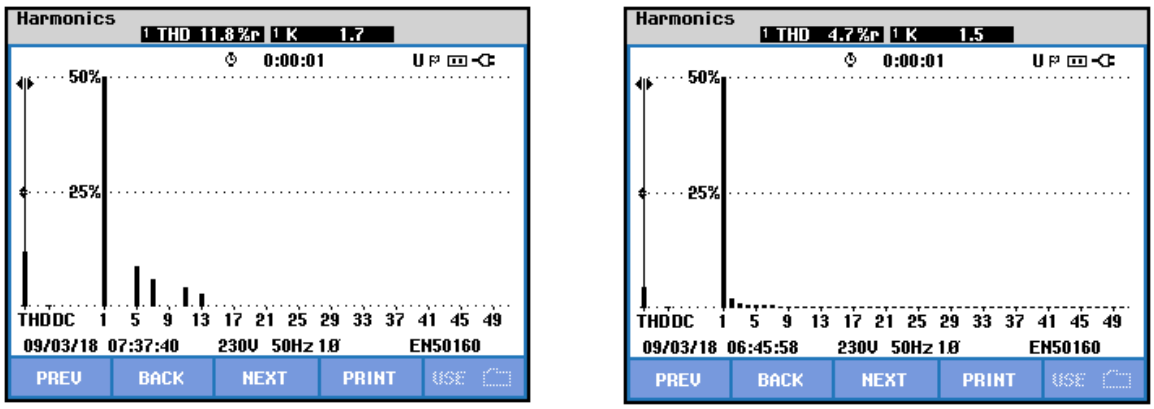
Fig. 3.9: Harmonic spectrum of phase-*a* of (a) source current; (b) load current

The FFT harmonic spectrum of source and load voltage and also the current signals from MATLAB Simulink are shown in Figures 3.8 to 3.9.



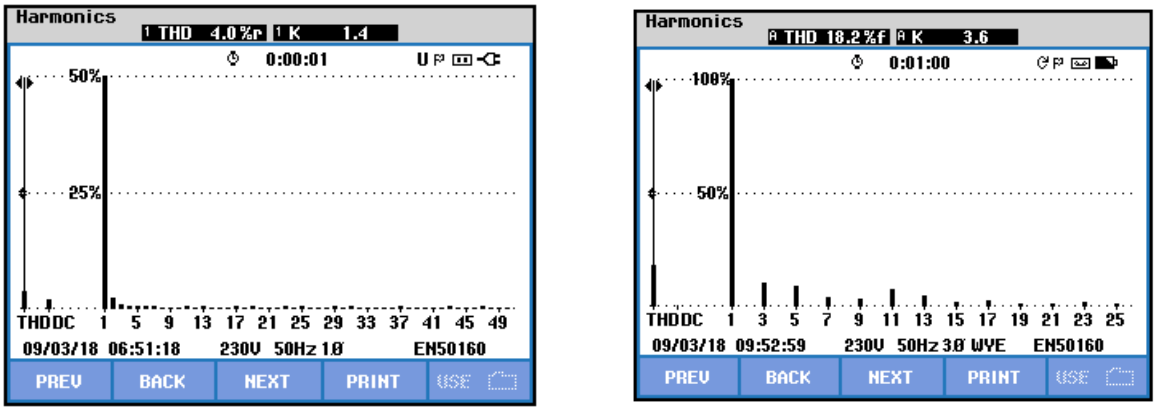
(a) (b)

Fig. 3.10: Distorted voltage compensation by the proposed control scheme showing for phase-*a*



(a) (b)

Fig. 3.11: Harmonic spectrum of phase-*a* of (a) source voltage; (b) load voltage



(a) (b)

Fig. 3.12: Harmonic spectrum of phase-*a* of (a) source current; (b) load current

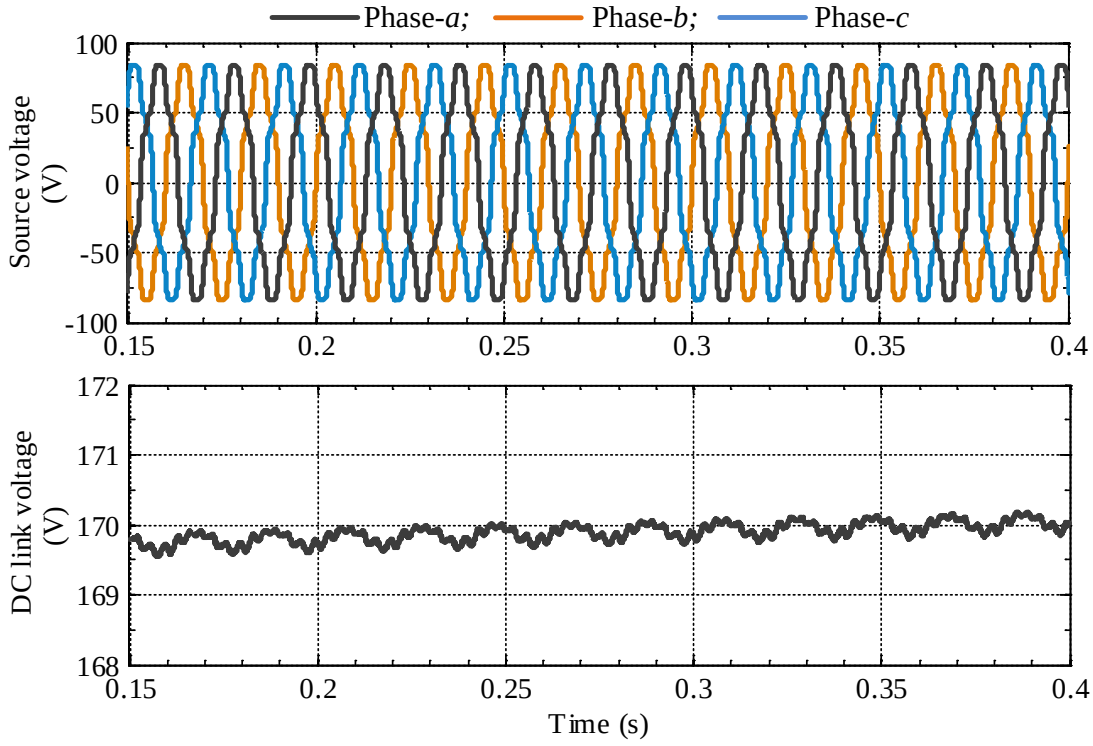


Fig. 3.13: DC-link voltage during distorted voltage compensation of UPQC-2L

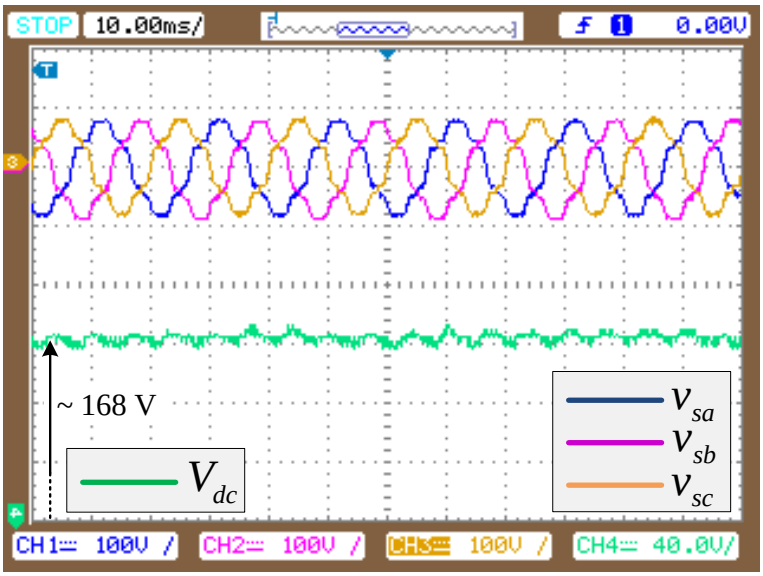


Fig. 3.14: Experimental scope results showing dc-link voltage during distorted voltage compensation of UPQC-2L

The experimental scope results of voltage and current compensation characteristics are shown in Figure 3.10 (a), and (b) respectively for phase-*a*. The traces of Figure 3.10 (a) and (b) are shown as follows:

- Trace-1: Source voltage; source current
- Trace-2: Series injected voltage of predicted signal and reference signal; shunt compensating current of predicted signal and reference signal
- Trace-3: Load voltage; load current

By looking at the quantitative analysis, the compensated load peak fundamental voltage and source rms current are having of 80.3V, 3.8A, while the THD is of 4.51%, 3.82% respectively. Other hand the desired value of phase peak fundamental voltage magnitude is selected as 81.65V. On comparing with simulation results;, the experimental results are little deviated in terms of maintained THD values because of the limited sampling period chosen for implementing model predictive control. he experimental harmonic spectrum of source and load voltage and also the current signals are shown in Figures 3.11 to 3.12, which are captured by using single-phase Fluke power quality meter. Figure 3.13 and 3.14 shows the dc-link variation during compensation in simulation studies and in experimental work respectively. The reference value of dc-link is calculated based on (2.40), which is equal to 170V. The average value of dc-link is measured as 169.8V from 0.15s to 0.4s in simulation results, which is shown in Figure 3.13, whereas the value is 168V in experimental scope results from Figure 3.14.

(B) UPQC-3L

The simulation results of UPQC-3L compensation characteristics related to distorted voltage and non-linear current harmonics are shown in Figures 3.15-3.16.

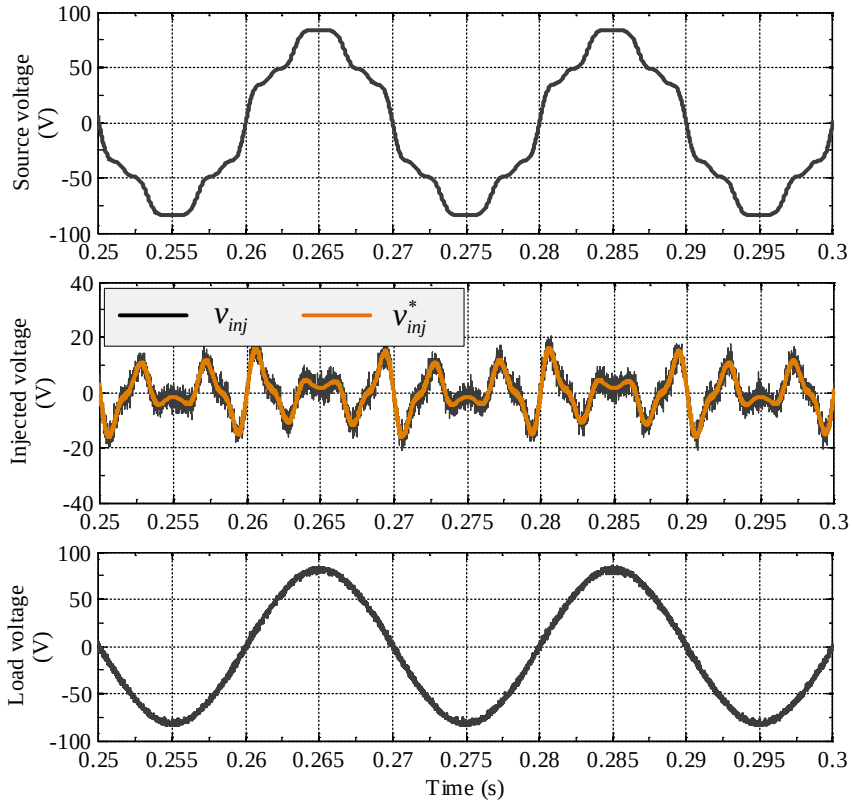


Fig. 3.15: Distorted source voltage compensation by the proposed control scheme showing for phase-*a* of UPQC-3L.

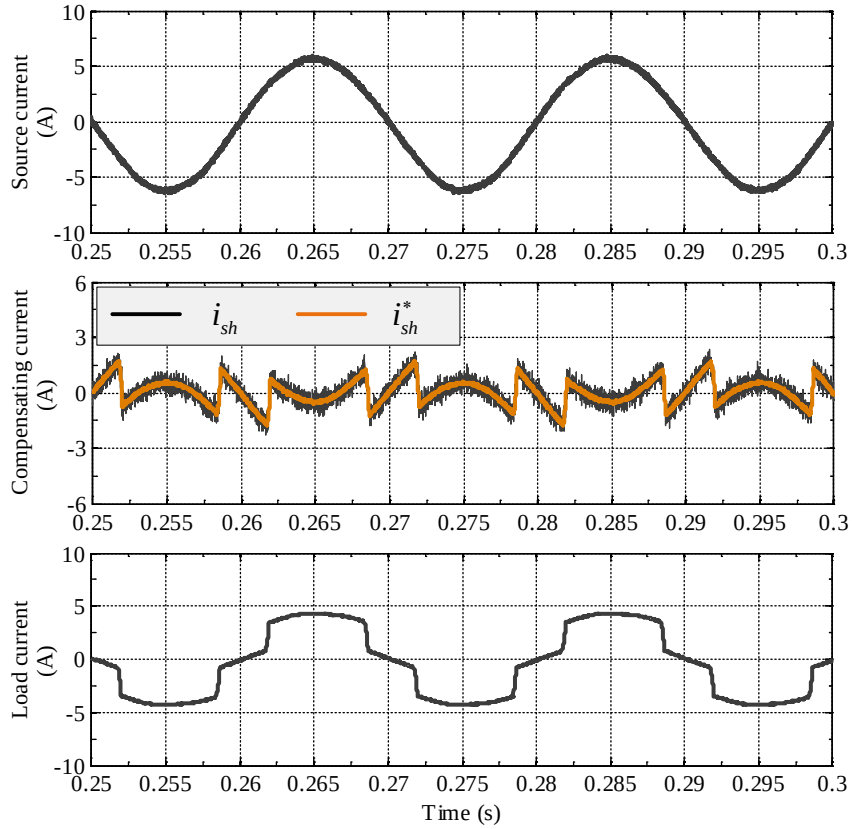
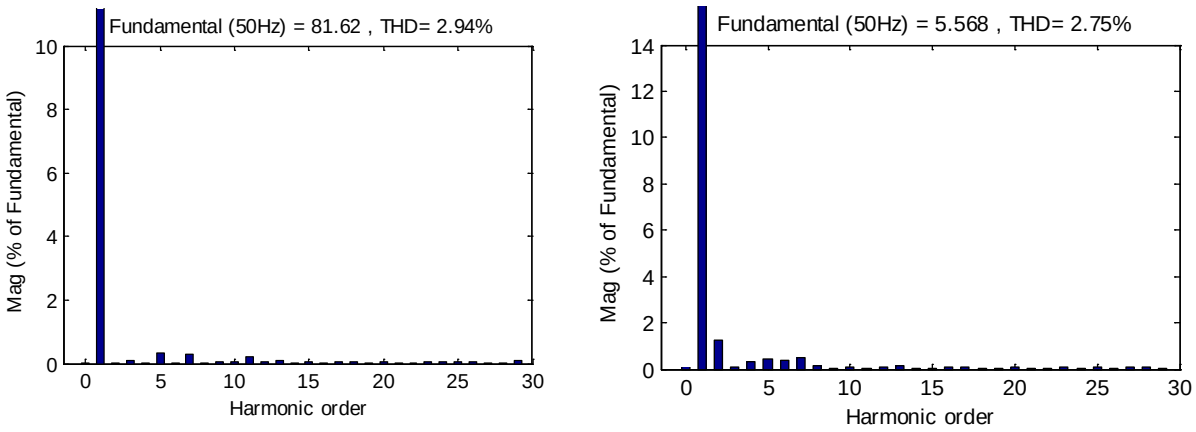


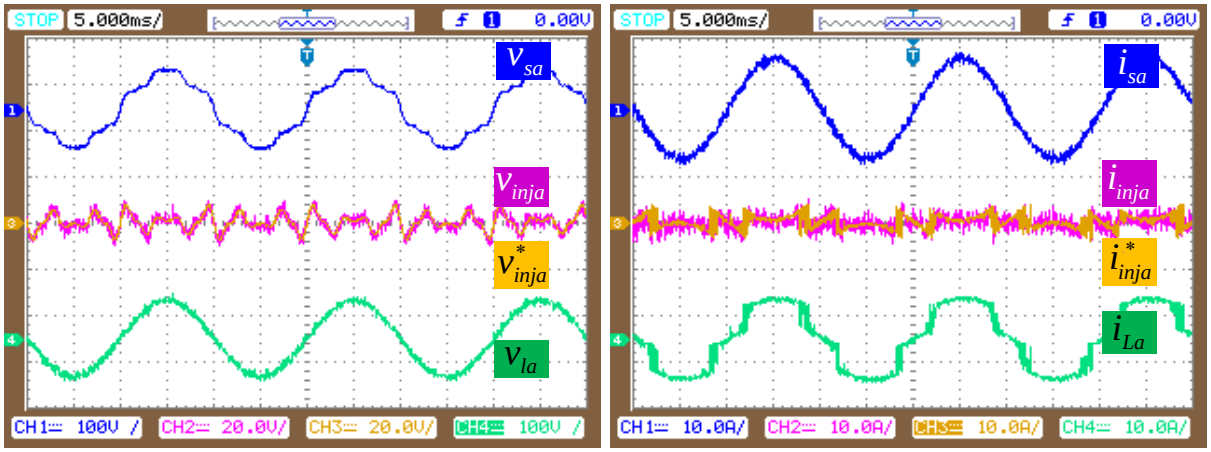
Fig. 3.16: Compensation of source current during distorted source voltage along with non-linear load by the proposed control scheme showing for phase-*a* of UPQC-3L.



(a) (b)

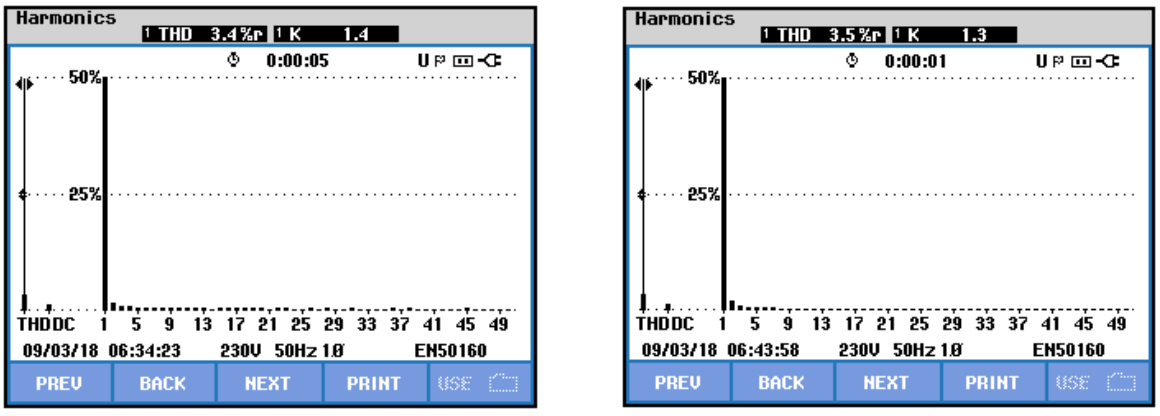
Fig. 3.17: Harmonic spectrum of phase-*a* of (a) load voltage; (b) source current

On comparison with simulation results shown in Figure 3.6-3.7, the UPQC-3L provides the better compensation. The tracking of predicted signal with the reference signal is much accurate, which is observed from axis-2.



(a) (b)

Fig. 3.18: Distorted source voltage compensation showing for phase-*a*



(a) (b)

Fig. 3.19: Harmonic spectrum of phase-*a* of (a) load voltage; (b) source current

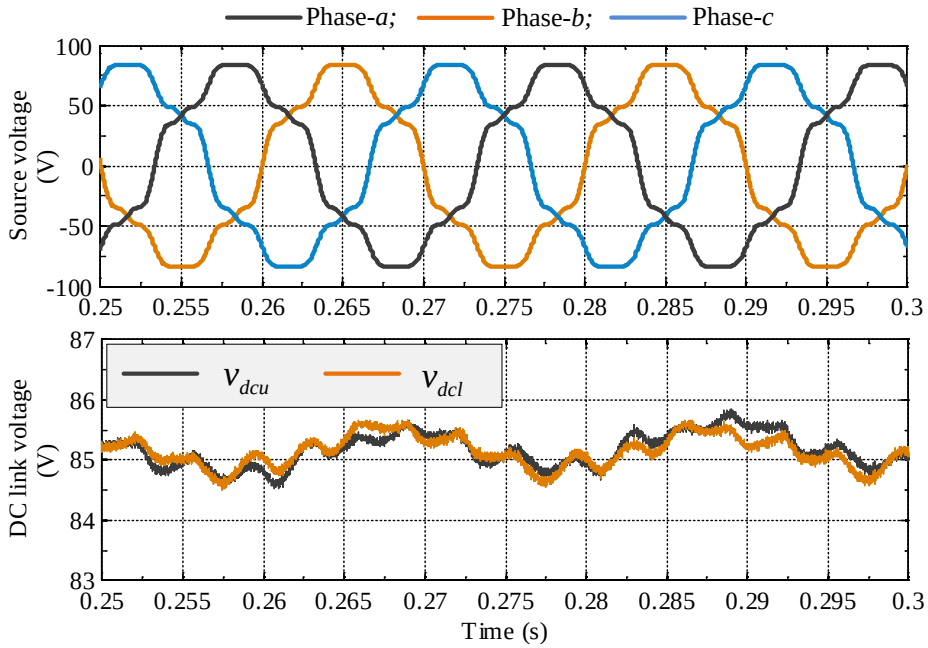


Fig. 3.20: DC-link voltage during distorted source voltage compensation of UPQC-3L

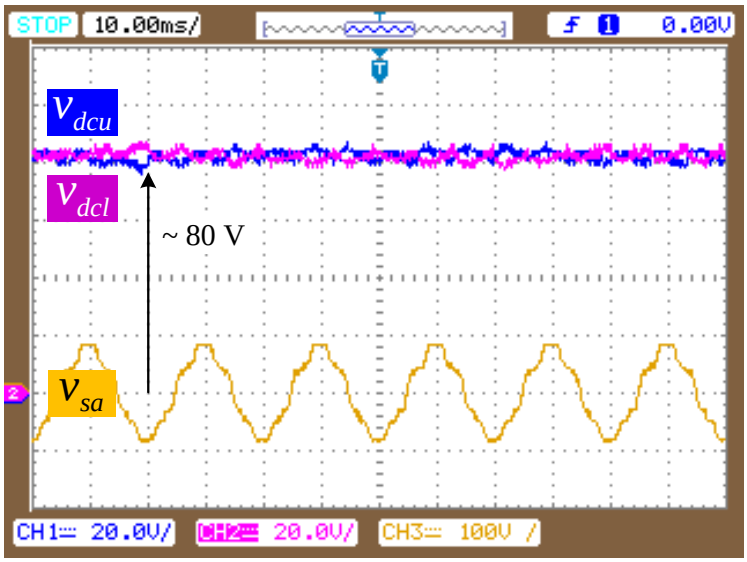


Fig. 3.21: Experimental scope results showing dc-link voltage during distorted source voltage compensation of UPQC-3L

The load voltage is shown in axis-3, which is sinusoidal and having peak fundamental magnitude of 81.2V with THD of 3.17%. The reference signal tracking with predicted signal for compensating currents is also observed from axis-2 of Figure 3.15 with small ripples around the reference signal. The source current is maintained at sinusoidal with rms value of 4.1A, and 2.34% THD, while the load current magnitude is 3.56A and having THD of 23.45%. On comparison with simulation study, the experimental scope results are presented in Figure 3.18. The phase peak load voltage value is 80.4V for phase-*a*, and THD is measured as 3.61%. Similarly the rms value of source current is measured as 4.4A with THD of 3.41%. The dc-link variation of UPQC-3L is shown in Figure 3.20 and 3.21 for simulation and

experimental work respectively. As UPQC-3L has split dc-link, the reference value across each capacitor should be 85V. Figure 3.20 shows that the effectiveness of controller to balance the capacitor voltages balanced and maintained at reference value. The experimental scope results shows that the each capacitor is maintained at average value of 80V, whereas the simulation value is 85V. The harmonic spectrum of load voltage source current from MATLAB Simulink and experiment are shown in Figures 3.17 and 3.19.

(C) Summary

The quantitative comparison between UPQC-2L and UPQC-3L for this case study is given in Table 3.2, where the percentage THD values of experiment are considered for the comparison. The THDs are corresponding to the load voltage at PCC and source current of phase-*a.* From this comparison, it can be concluded that the compensating performance of UPQC-3L is better than UPQC-2L.

Table 3.2: THD Comparison between UPQC-2L and UPQC-3L with distorted source and non-linear load compensation

Type of disturbance (Voltage distortion)	**UPQC-2L**		**UPQC-ML**	
	Load voltage (%)	Source current (%)	Load voltage (%)	Source current (%)
Before compensation	12.30	23.45	12.30	23.45
After compensation	4.51	3.82	3.17	2.34

3.5.2 Case-2: Distorted Unbalanced Source Voltage

The performance is evaluated with unbalancing the distorted source voltages. As discussed in the case-1, the distorted voltages are created and then unbalancing is added with in each phase with different magnitudes from the peak fundamental value of 81.65V. The unbalance is created in with 40% and 20% voltage dip in two phases of three-phase supply. The 40% voltage dip is added to phase-*a*, while 20% voltage dip is added to phase-*c* and phase-*b* is unaffected and considered at rated value. Though the combination of linear and non-linear load is connected at the PCC, the current compensation characteristics are not presented for this case, as because of the response is similar to the previous case-1.

(A) UPQC-2L

Figures 3.22 and 3.23 shows the compensation characteristics with distorted and unbalanced source voltage. The various amounts of harmonics and unbalanced magnitudes are mixed up with fundamental source voltage results the voltages as shown in axis-1. The phase peak value of phase-*a*, *b* and *c* are 58.14V, 81.04V and 70.55V respectively and the THDs of these voltages are 26.21%, 19.85% and 23.21% respectively. The FFT spectrum

windows of source voltages obtained from MATLAB are shown in Figure 3.24. The compensated three-phase load voltage is shown at axis-2, which is maintaining at 79.6V, 80.5V, and 79.2V and possessing THDs of 4.72%, 3.81% and 4.20% on phase-*a*, *b* and *c* respectively. The dc-link voltage during compensation is captured and presented at axis-3. The maximum fluctuation in the dc-link magnitude is 2% with an average value of 169V. Figure 3.23 shows the three-phase series injected voltages by UPQC-2L. The compensating voltage of each phase in terms of predicted signal and reference signal is presented on the same axis. From Figure 3.23, it can be observed each phase compensating voltage is differ from the other with different magnitudes and also having different wave shape. Figure 3.25 shows the experimental scope results to validate the simulation results. In experimental work, the load voltage is able to maintain at 78.9V, 80.0V and 78.6V for phase-*a*, *b* and *c*. The THD of these compensated load voltages are 4.91%, 3.82% and 4.8% for phase-*a*, *b* and *c* respectively such that the load voltages are balanced from the unbalanced distorted source voltages, which is observed from the Figure 3.25(b). To justify the compensating injected voltages of different phases, which are obtained in the simulations, these voltages are sensed and depicted in Figure 3.25(d) to (f) from the experimental work.

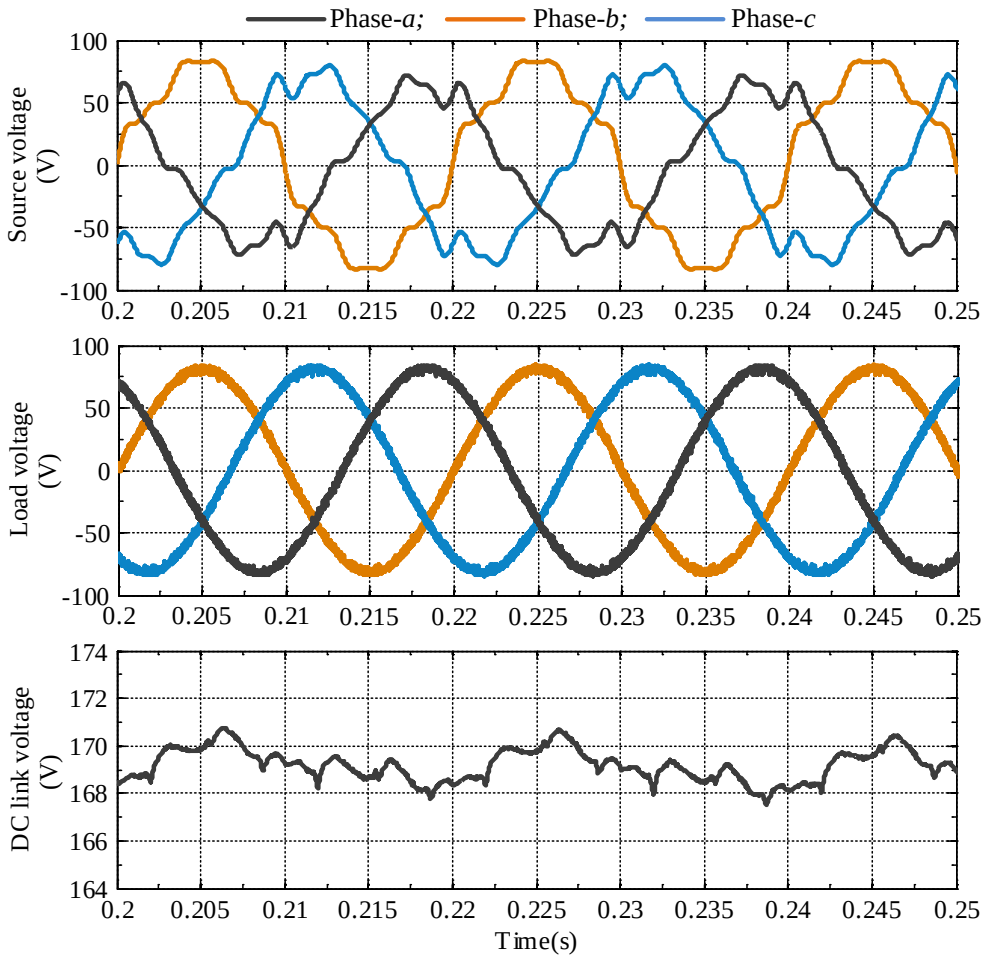


Fig. 3.22: Distorted unbalanced source voltage compensation by the proposed control scheme showing for phase-*a* of UPQC-2L.

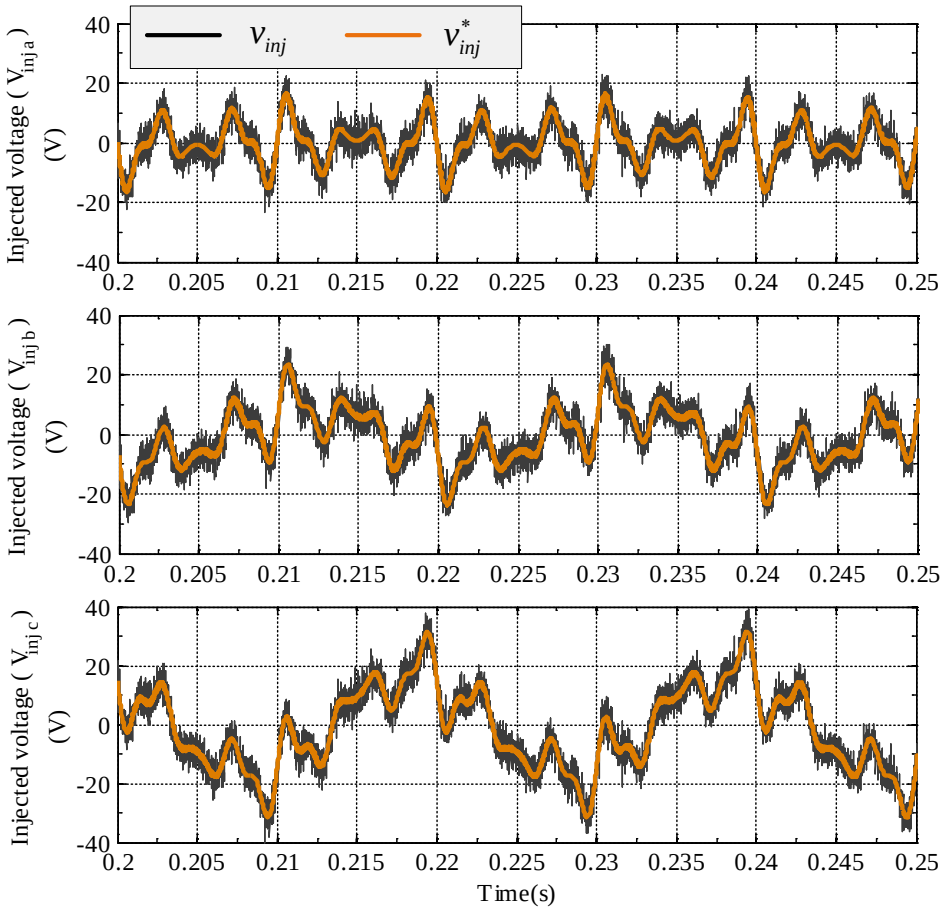
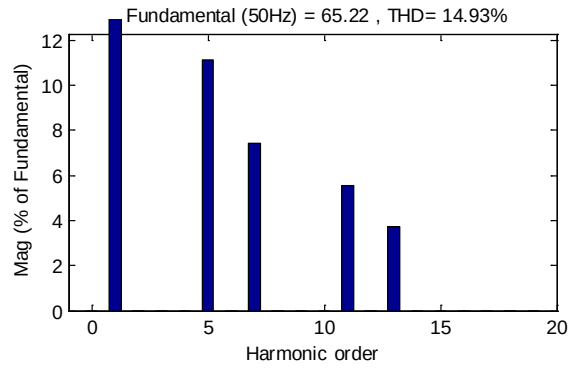
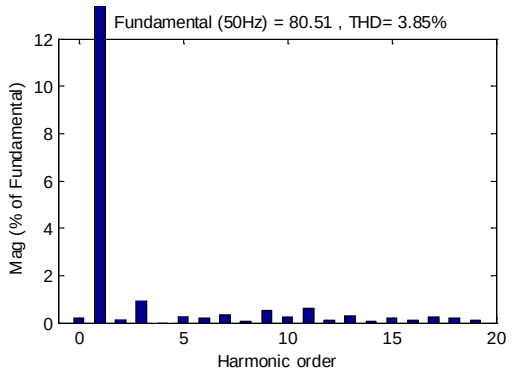


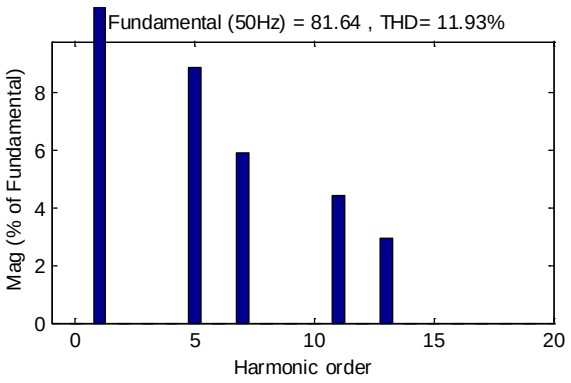
Fig. 3.23: Three-phase injected voltages during distorted unbalanced source voltage compensation of UPQC-2L.



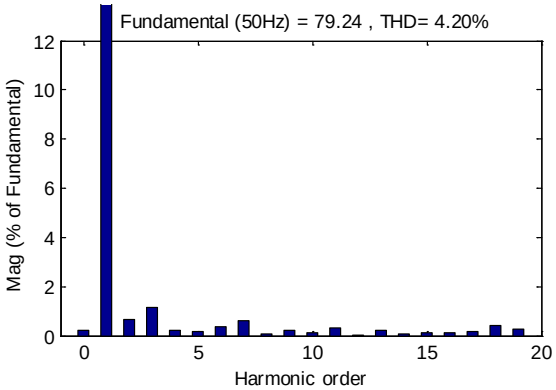
(a)



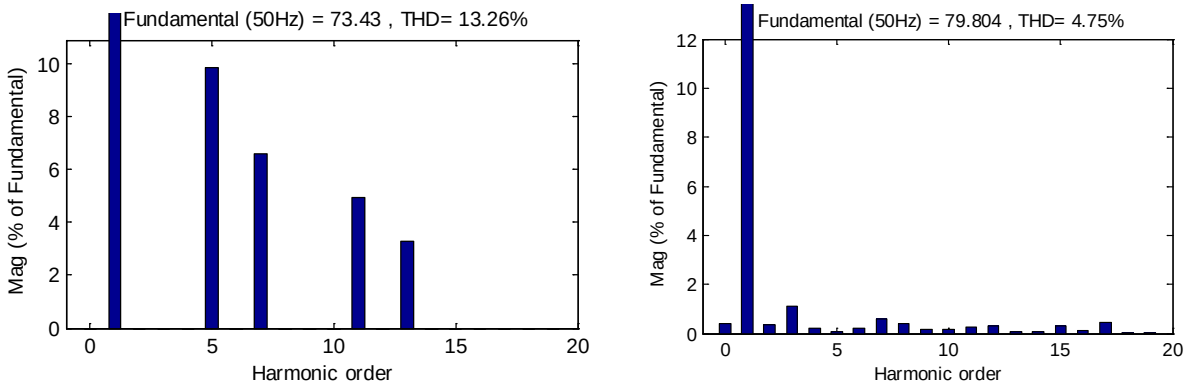
(d)



(b)



(e)



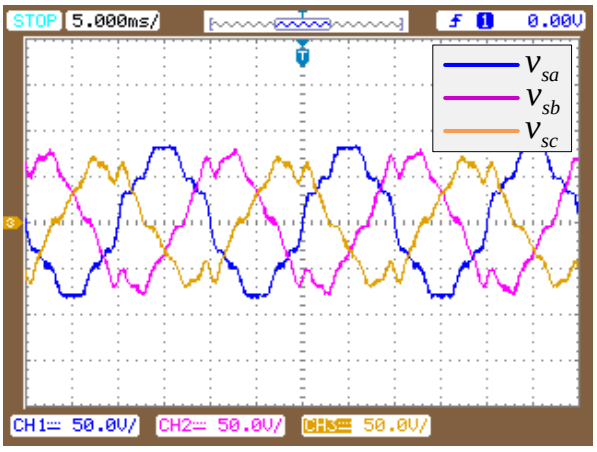
(c) (f)

Fig. 3.24: Harmonic spectrum of voltages: (a)-(c) three-phase source voltage; (d)-(f) three-phase load voltage

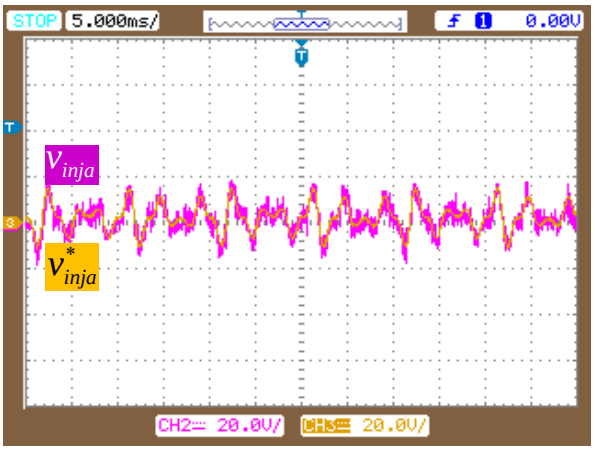
The Fluke power quality meter results are shown in Figure 3.26 to measure the THD of source and load voltages.

(B) UPQC-3L

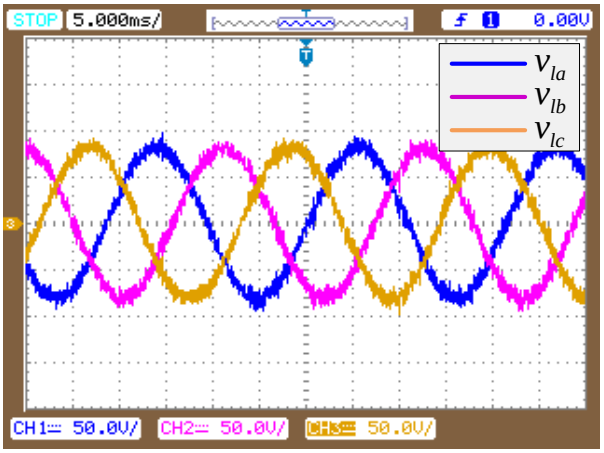
The simulation results of UPQC-3L compensation characteristics related to distorted unbalanced source voltages are shown in Figure 3.29-3.30. Axis-2 from Figure 3.27 shows the three phases of load voltage at PCC after compensation.



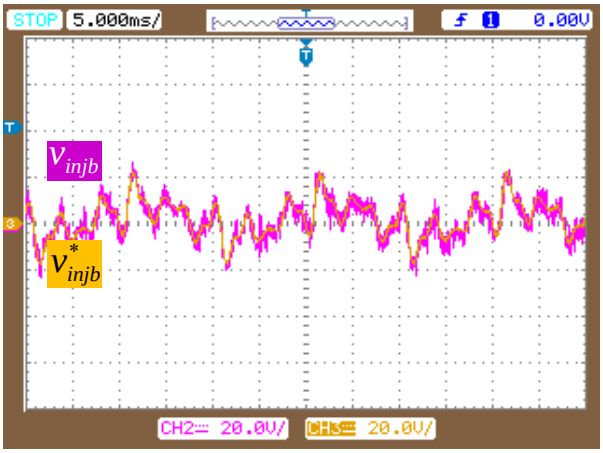
(a)



(d)



(b)



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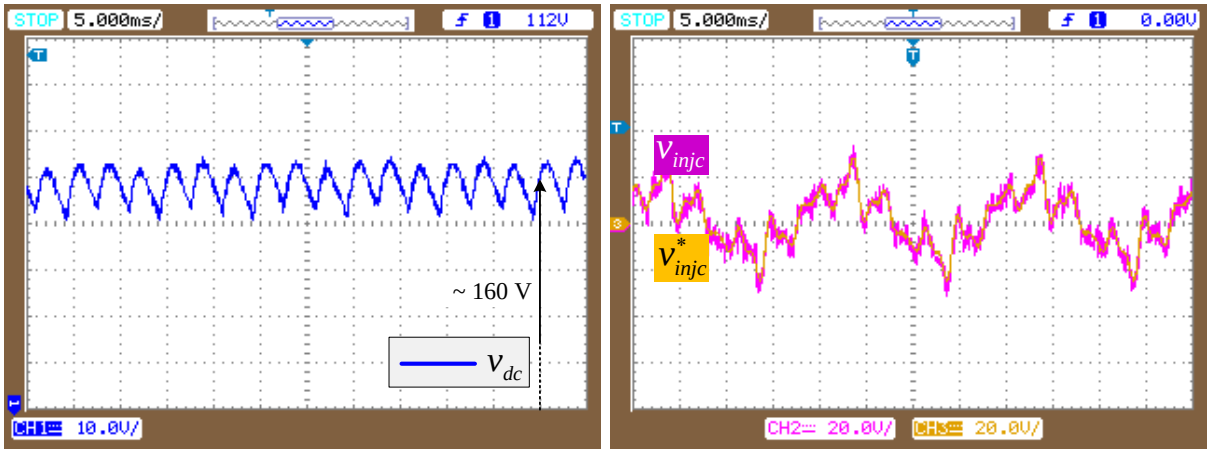
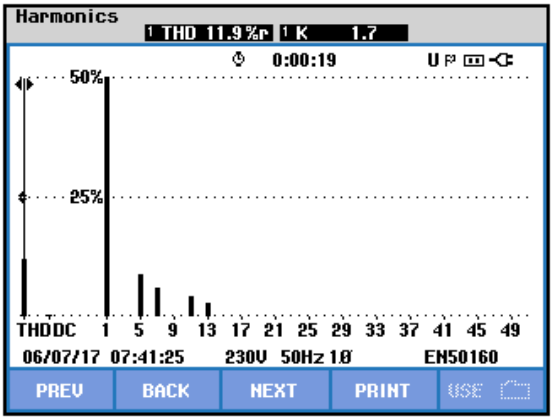


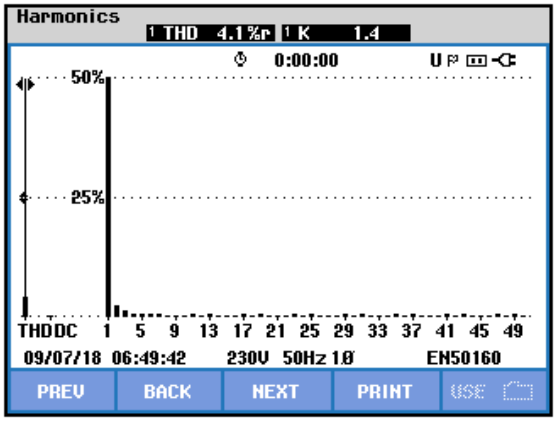
(c) (f)

Fig. 3.25: Distorted unbalanced source voltage compensation by the proposed control scheme showing for UPQC-2L

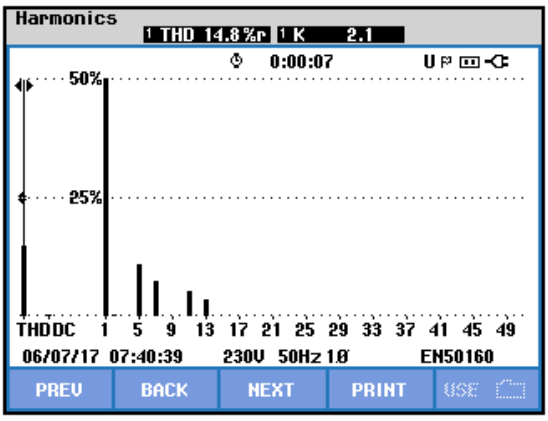
The magnitude of phase load voltage is measured as 79.85V, 80.9V, and 80.3V and having the THD of 3.05%, 2.47%, and 2.39% on phase-*a*, *b* and *c* respectively. As compared with the simulation results shown in Figure 3.22 (axis-2) with UPQC-2L, the load voltage is well compensated with UPQC-3L. The split dc-link is maintained at an average value of 84.5V on upper capacitor and 84.2V on lower capacitor. The predictive controller also ensure that the balancing on both the capacitor voltages.



(a)



(d)



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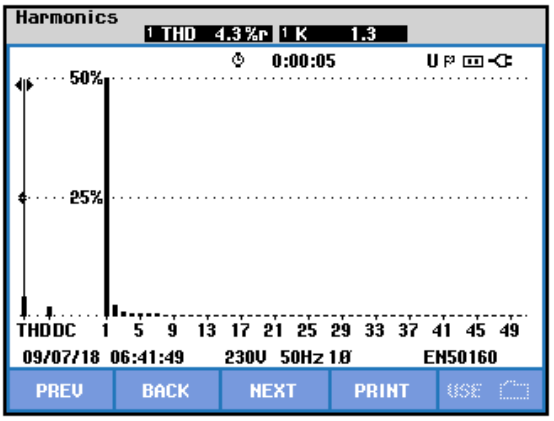

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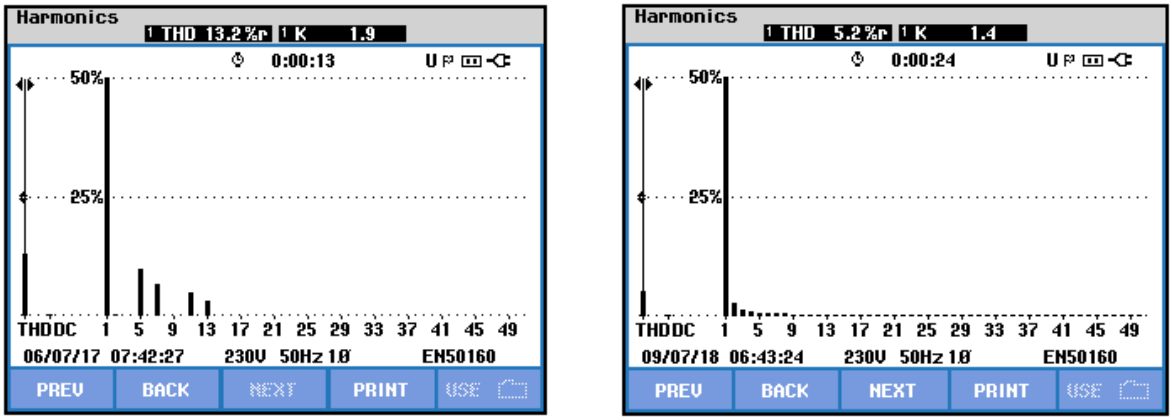


(c) (f)

Fig. 3.26: Harmonic spectrum of voltages: (a)-(c) three-phase source voltage; (d)-(f) three-phase load voltage

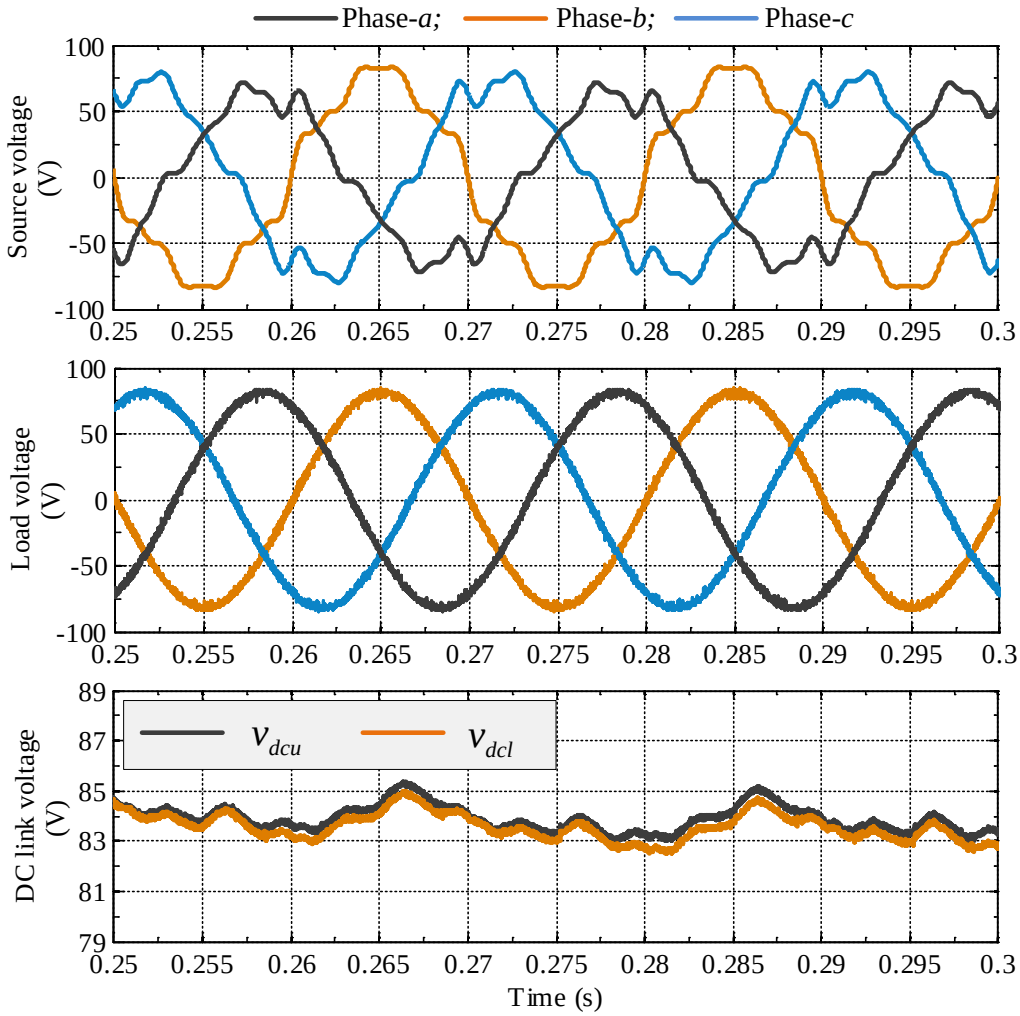


Fig. 3.27: Distorted unbalanced source voltage compensation by the proposed control scheme showing for phase-*a* of UPQC-3L.

Figure 3.28 shows the series injected voltages of phase-*a*, *b* and *c*. On comparing with Figure 3.23, the tracking of predictive signals with reference signals are much improved with UPQC-3L controller.

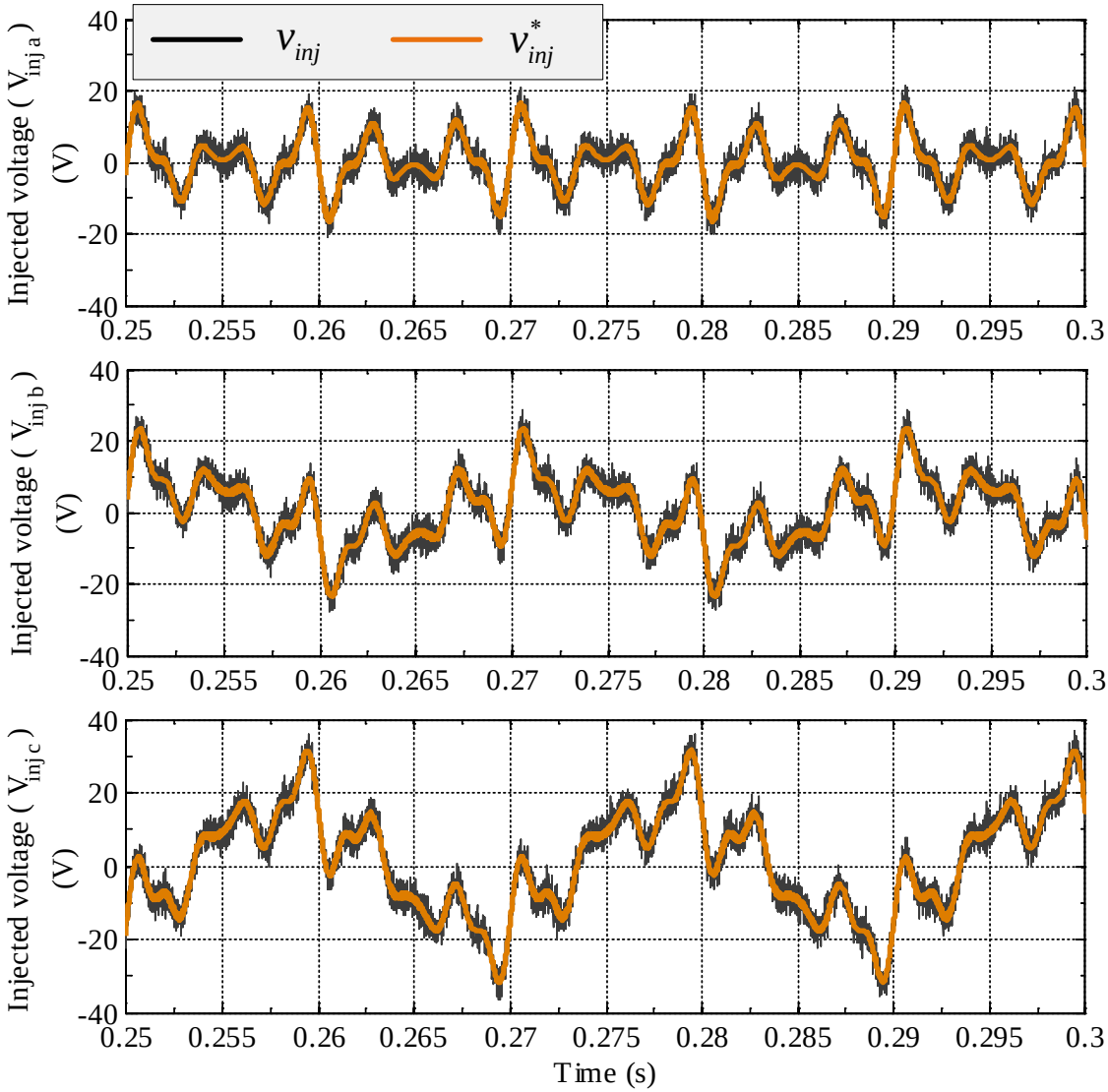
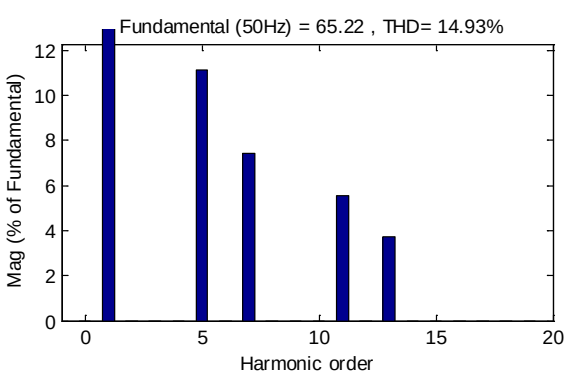
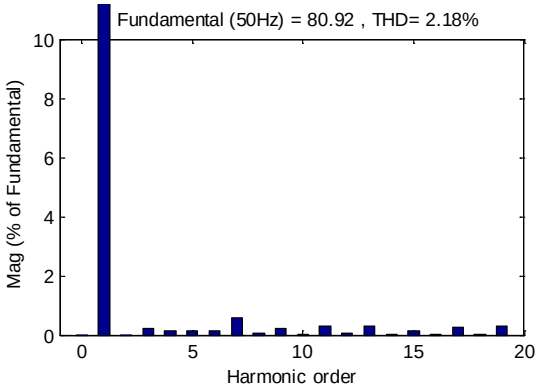


Fig. 3.28: Three-phase injected voltages during distorted unbalanced source voltage compensation of UPQC-3L.

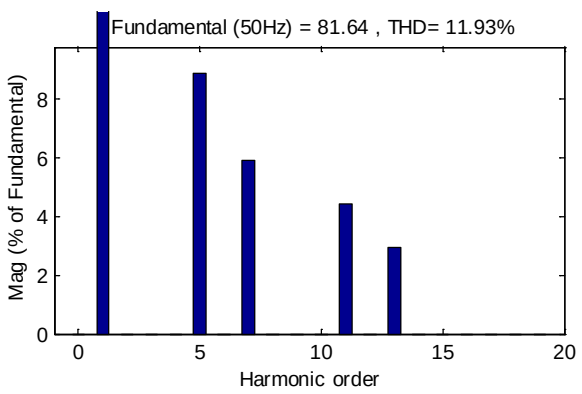
The corresponding experimental results are presented from Figures 3.30. From these results, it can be noticed that the load voltage is maintained at 79.5V, 80.2V, and 79.6V on phase-*a*, *b*, and *c* respectively, while dc-link voltages are settled at 81V on upper dc-link and 80V on lower dc-link.



(a)



(d)



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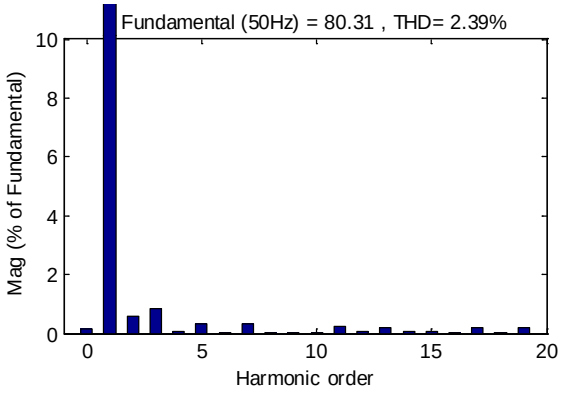

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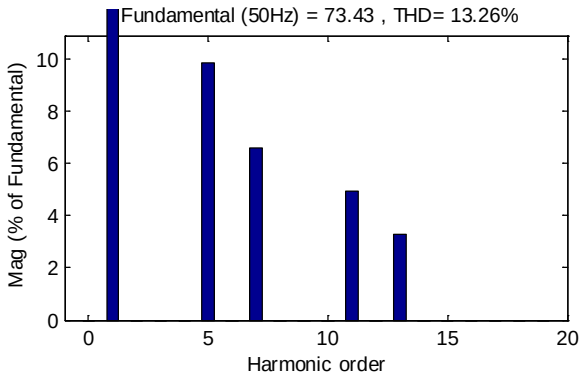
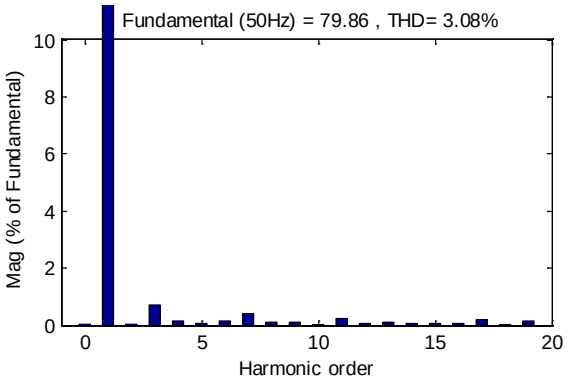


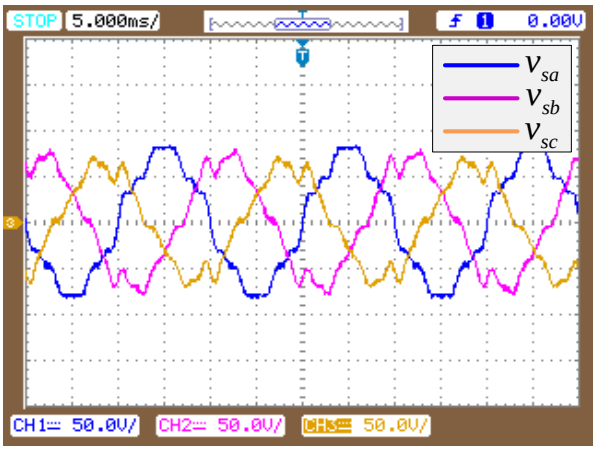
(c)



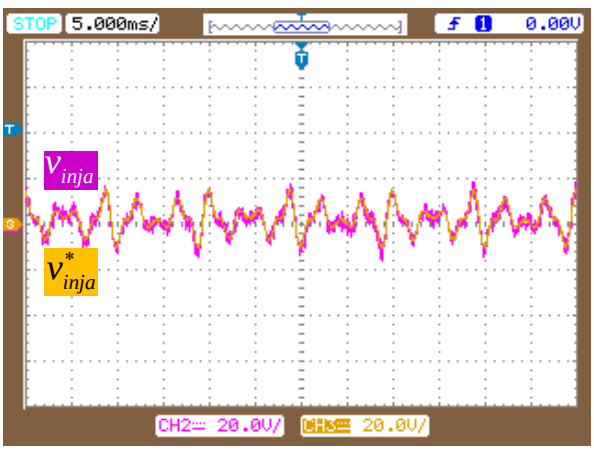
(f)

Fig. 3.29: Harmonic spectrum of voltages: (a)-(c) three-phase source voltage; (d)-(f) three-phase load voltage

The series injected voltages are also in good compromise with the simulation results. The THD of load voltage is captured in Figures 3.29 and 3.31. The quantitative comparison between UPQC-2L and UPQC-3L for this case study is given in Table 3.3, where the values of phase fundamental peak and percentage THDs are considered from simulation study for the comparison.



(a)



(d)

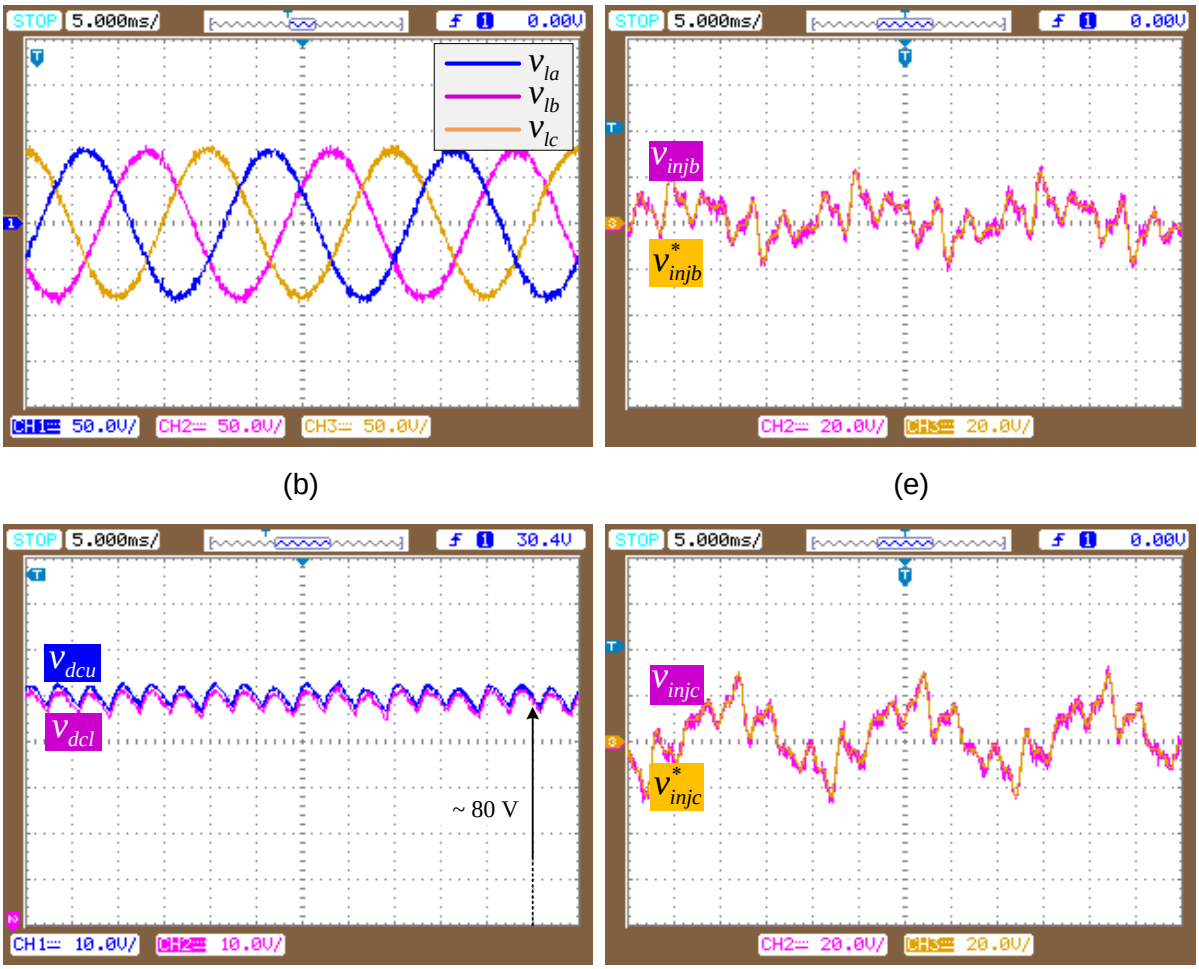
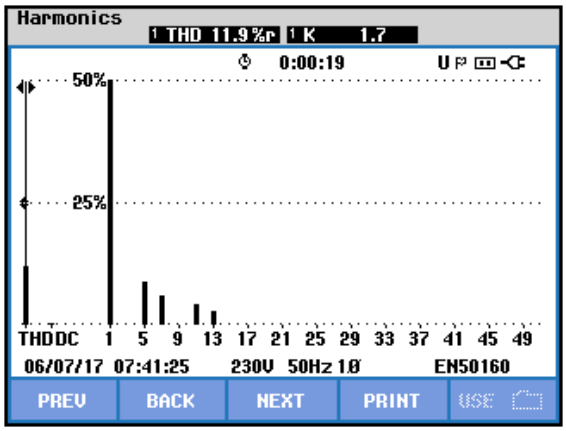


Fig. 3.30: Distorted unbalanced source voltage compensation by the proposed control scheme showing for UPQC-3L

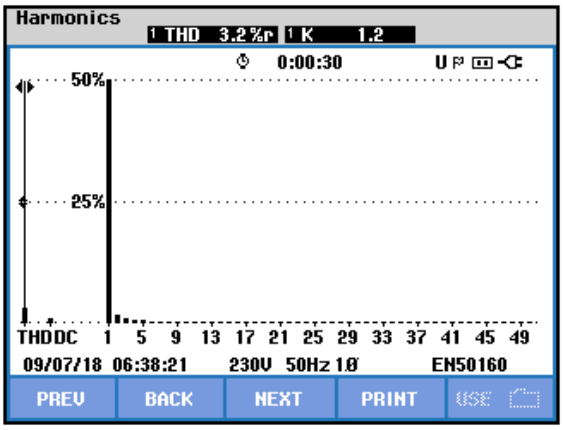
(C) Summary

Table 3.3: THD Comparison between UPQC-2L and UPQC-3L with distorted unbalanced source voltage compensation

Type of disturbance (Voltage unbalanced distortion)	**UPQC-2L**		**UPQC-ML**	
	Load voltage magnitude (V)	Load voltage THD (%)	Load voltage magnitude (V)	Load voltage THD (%)
Before compensation	81.04, 70.55, 58.14	19.85, 23.81, 26.21	81.04, 70.55, 58.14	19.85, 23.81, 26.21
After compensation	80.50, 79.20, 79.60	3.81, 4.20, 4.72	80.90, 80.31, 79.85	2.47, 2.39, 3.05



(a)



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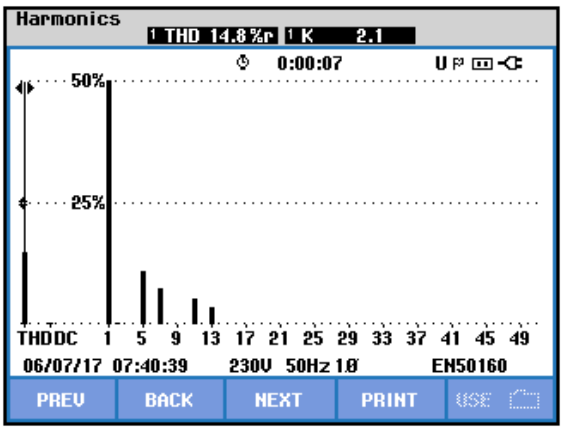
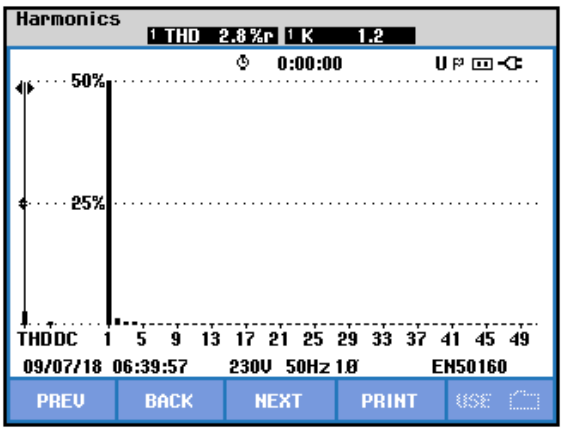
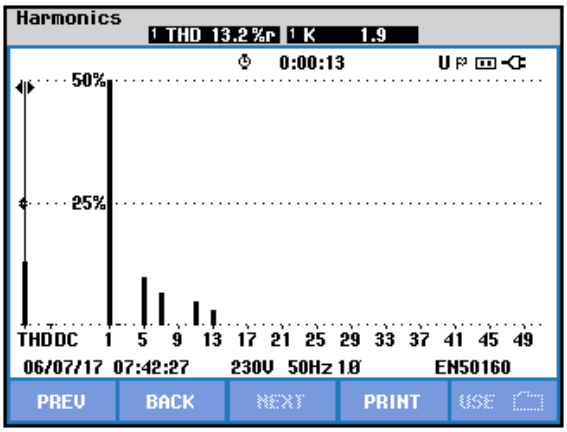


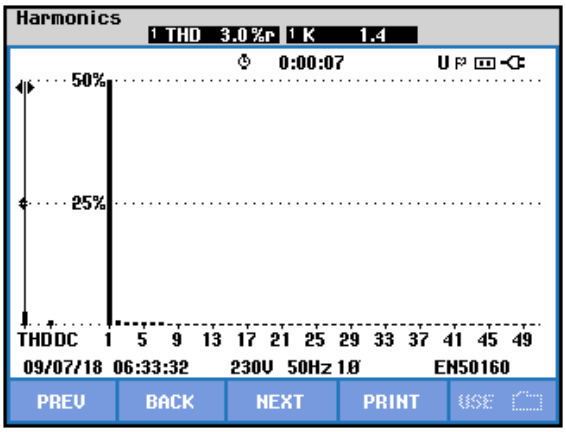
(b)



(e)



(c)



(f)

Fig. 3.31: Harmonic spectrum of voltages: (a)-(c) three-phase source voltage; (d)-(f) three-phase load voltage

3.5.3 Case-3: Voltage Sag with Non-linear Load

The performance of the proposed control scheme is also verified with the very frequent voltage disturbance on distribution system, i.e. voltage sag. The 20% voltage sag is applied on the source voltage at t =0.2s such that the magnitude of source voltage becomes 65.32V

during sag period. The effectiveness of the proposed control scheme is tested with UPQC-2L and also with UPQC-3L. Since the three-phase balanced sag is applied on the system, only one phase results are shown in the following results.

(A) UPQC-2L

Figure 3.32 shows the voltage sag compensation for source voltage imposed to 20% three phase voltage sag at t =0.2s and cleared at 0.3s making the phase peak voltage to be 65.32V during sag period, which is observed from axis-1. Regardless of sag on supply voltage, load voltage is sustained at 79.5V, which is shown at axis-3. Trailing of injected voltage by the series converter with the reference signal portraits the tracking capabilities of the reference with proposed control scheme, as observed from axis-2 of Figure 3.32.

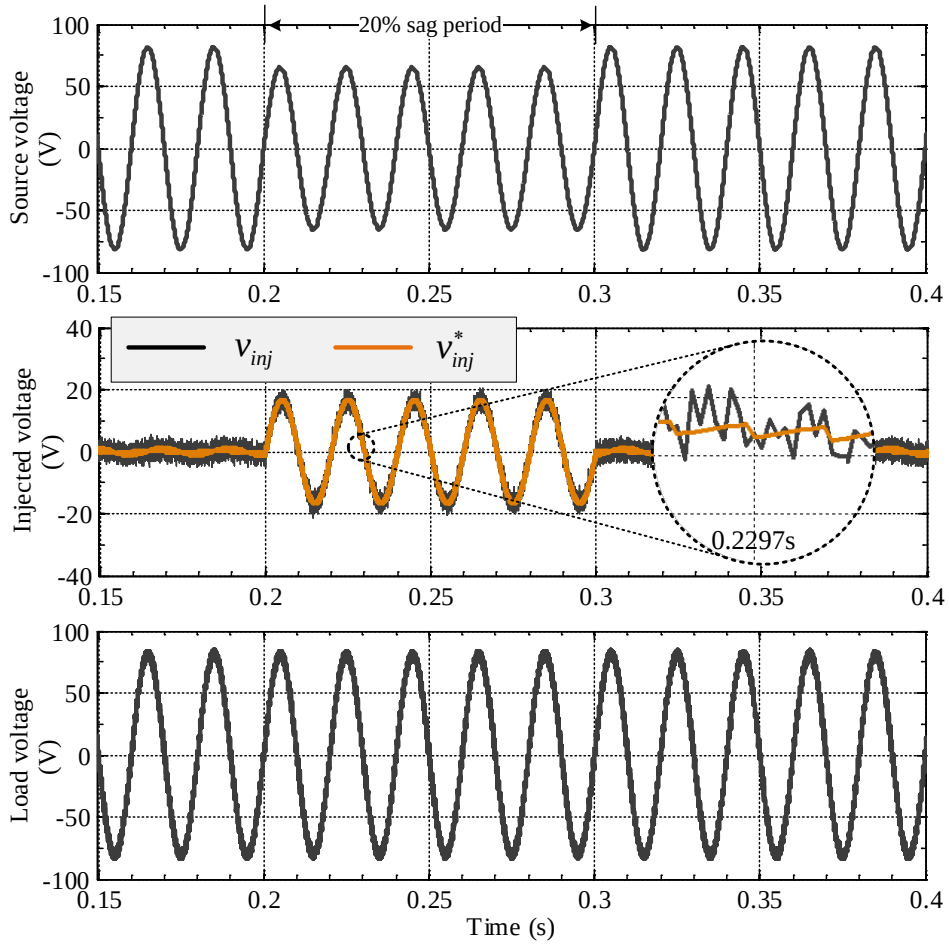


Fig. 3.32: Voltage sag compensation by the proposed control scheme showing for phase-*a* of UPQC-2L.

Involuntary selection of switching state is pegged by the predictive controller to optimize the error between reference and actual injected voltage for each sample time T_s. For the performance validation of the shunt converter, a non-linear load is linked throughout the simulation period. It is realized from Figure 3.33, that there is a supply of compensating current in continuum by the shunt converter to uphold source current with THD of 3.5%, while load current with 23.45%. Peak magnitude of source current (i_{sa}) is meagerly elevated from

5.29A to 6.66A to fulfil the demand of loading active power during this period as well as to maintain constant dc-link voltage, which is overserved from the axis-1 of Figure 3.32. The waveform of compensating current is shown in axis-2, where trace-1 and trace-2 are corresponding to predicted value and reference value signals respectively. The load current of phase-*a* is shown in axis-3.

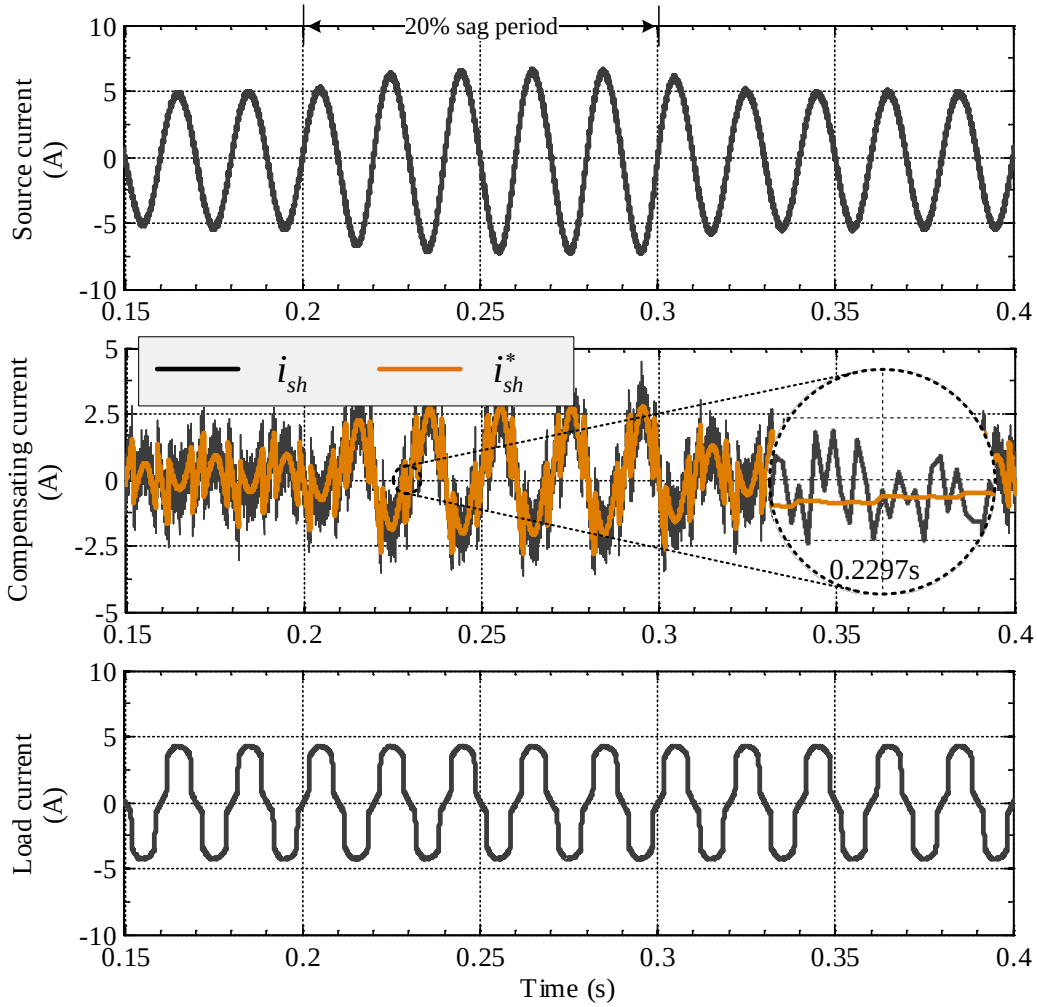
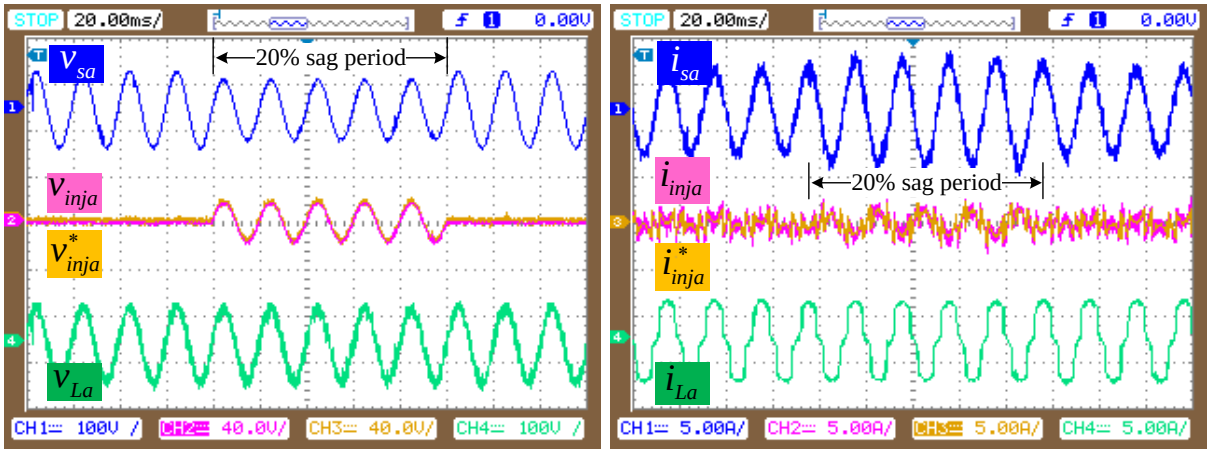


Fig. 3.33: Compensation of source current during voltage sag along with non-linear load by the proposed control scheme showing for phase-*a* of UPQC-2L.

The validated experimental results corresponds to simulation results are shown in Figure 3.34. Figure 3.34(a) refers to the voltage compensation characteristics, whereas Figure 3.34(b) shows the current compensation characteristics. The load voltage of phase-*a* is maintained at 79.3V whereas source current is 5.22A, with THD of 3.1% before sag compensation and is maintained at 6.8A with THD of 3.9% during sag compensation period.

The profile of voltage across dc-link for simulation and experimental work is shown in Figure 3.35 and 3.36 respectively. The average magnitude of dc-link voltage is measured as 169.6V in simulations and 168V at experimental results. The phenomena of drop and rise of dc-link voltage from the reference value at the instant of sag occurrence and at the instant of sag removal is same as explained in the previous chapter.



(a) (b)

Fig. 3.34: Voltage swell compensation by the proposed control scheme showing for phase-*a*

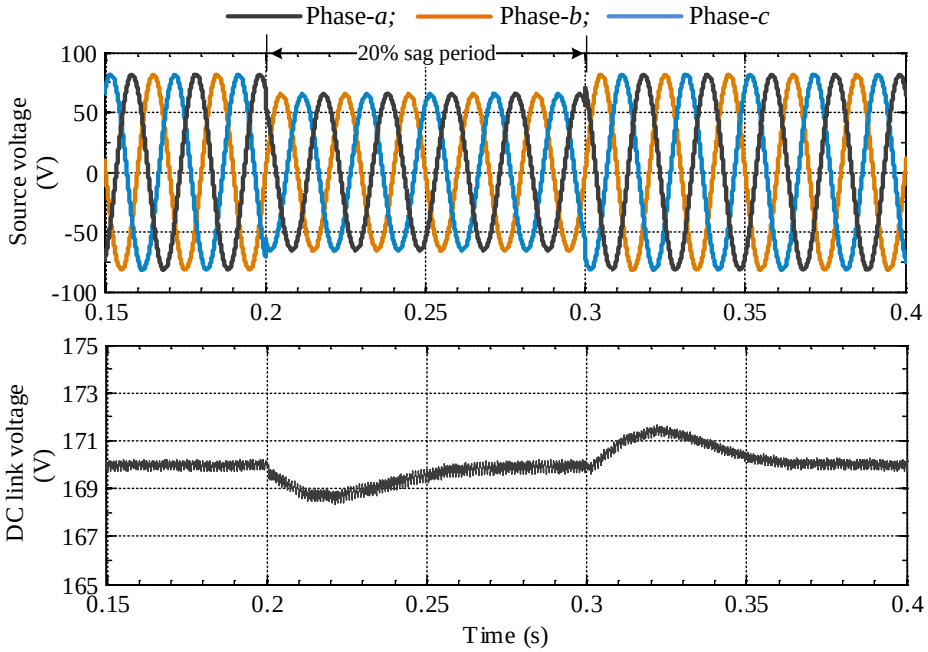


Fig. 3.35: DC-link voltage during sag compensation of UPQC-2L

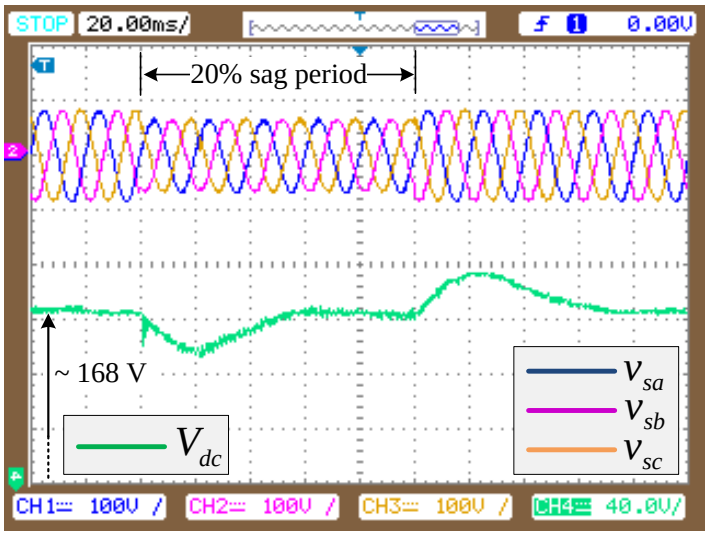


Fig. 3.36: Experimental scope results showing dc-link voltage during sag compensation of UPQC-2L

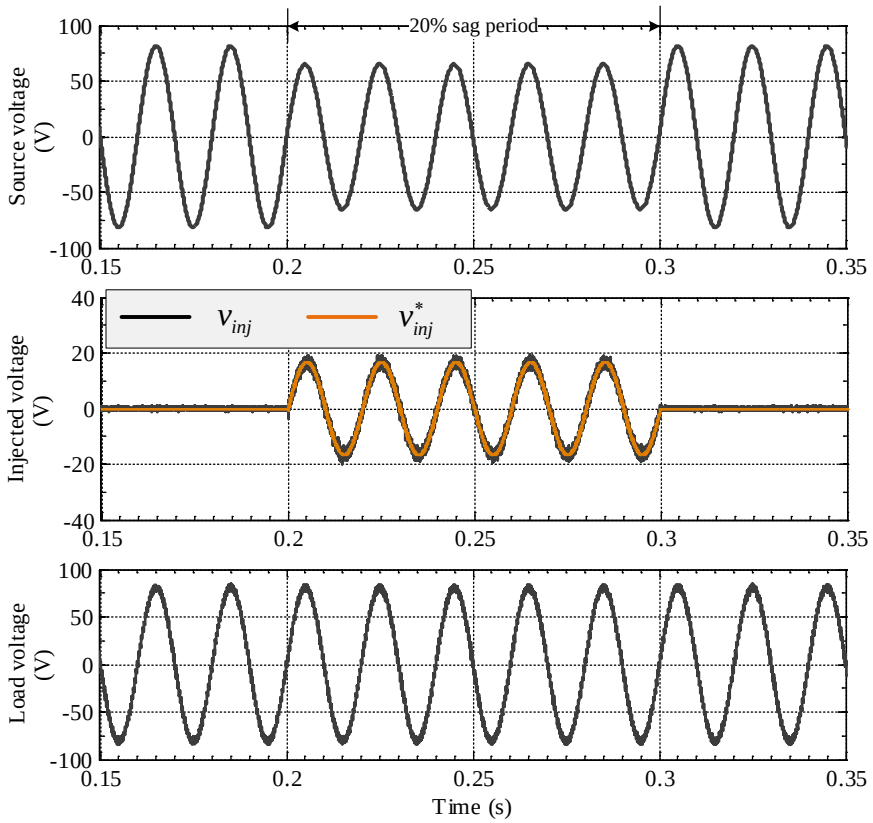


Fig. 3.37: Voltage sag compensation by the proposed control scheme showing for phase-*a* of UPQC-3L.

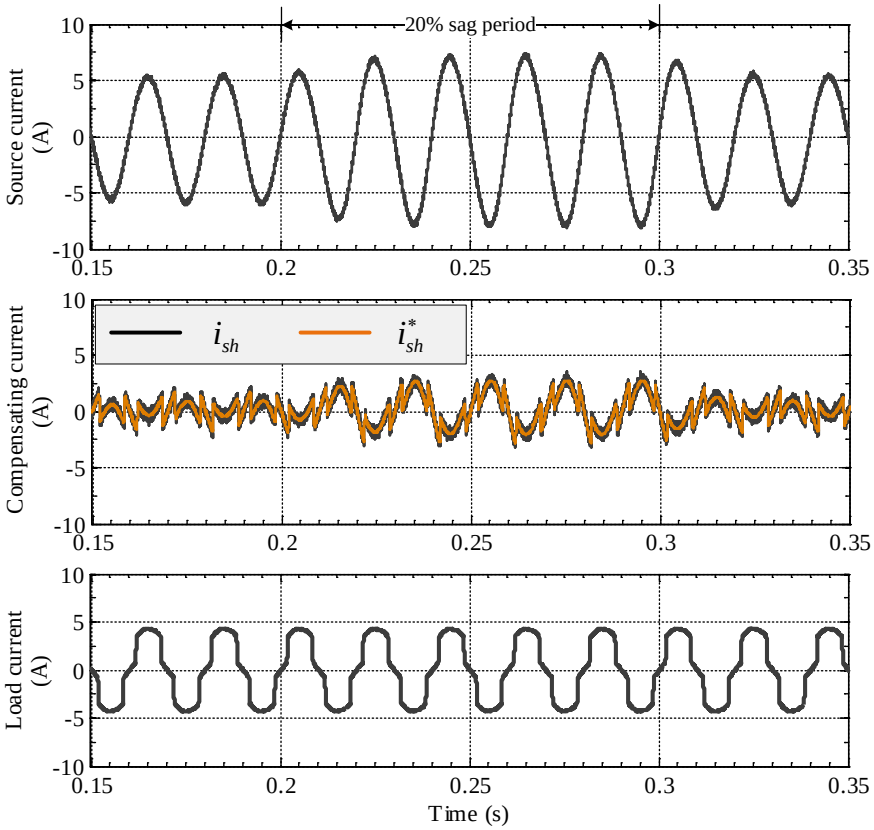
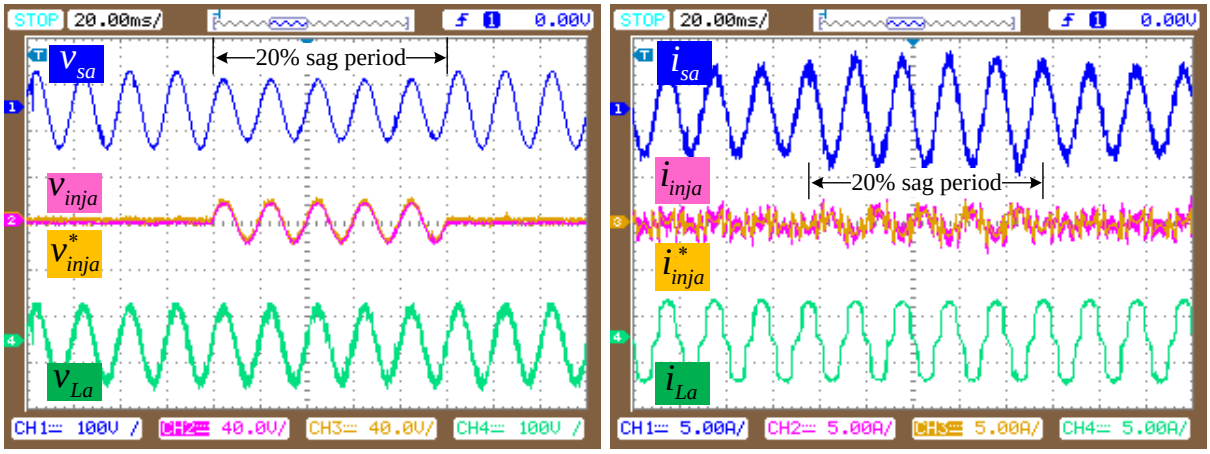


Fig. 3.38: Compensation of source current during voltage sag along with non-linear load by the proposed control scheme showing for phase-*a* of UPQC-3L.



(a) (b)

Fig. 3.39: Voltage swell compensation by the proposed control scheme showing for phase-*a*

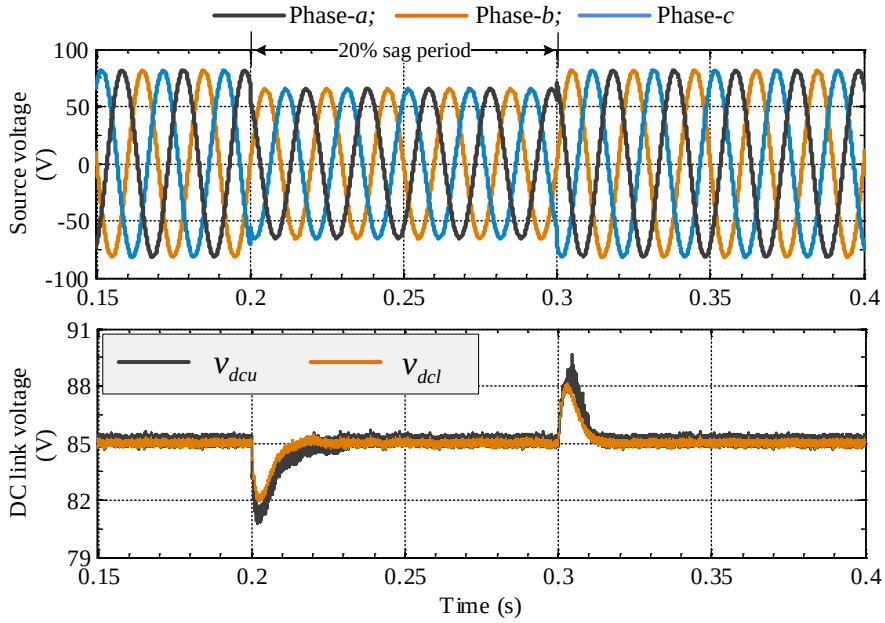


Fig. 3.40: DC-link voltage during sag compensation of UPQC-3L

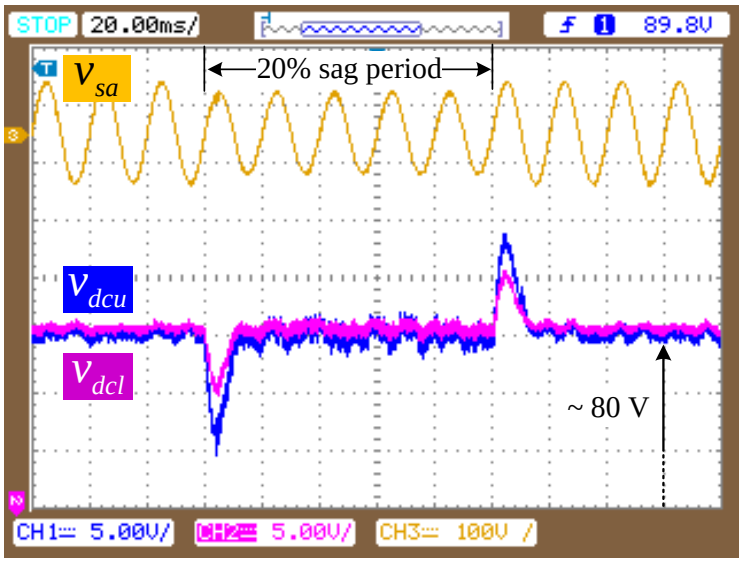


Fig. 3.41: Experimental scope results showing dc-link voltage during sag compensation of UPQC-3L

(B) UPQC-3L

The same level of sag voltage is applied to verify the performance of UPQC-3L with the proposed control scheme. Figure 3.37 shows the voltage compensation characteristics. The tracking of predicted signal with reference signal of series injected voltage is shown in axis-2. The compensated load voltage is shown at axis-3, where the phase peak fundamental value of phase-*a* voltage is measured as 80.5V. The nonlinear current compensation performed by the shunt converter are shown in Figure 3.38. The peak fundamental magnitude phase-*a* source current is 5.2A before voltage sag condition and during sag compensation the magnitude becomes 7.54A, which is slightly greater than the case of UPQC-2L. The experimental scope results are shown in Figure 3.39. From these results, it can be observed that the load voltage is maintained at 80V, whereas the source current is having 6.3A with THD of 2.8% before sag compensation and during compensation these magnitudes are 7.9A and 3.0%. The voltage across dc-link capacitors is shown in Figure 3.40 and 3.41 for simulation and also for experimental results respectively. From both simulation and experimental results, it can be concluded that the dc-link voltages are well balanced in overall compensation period.

(C) Summary

The quantitative comparison between UPQC-2L and UPQC-3L for this case study is given in Table 3.4, where the peak phase fundamental values of simulations are considered for the comparison. The values are corresponding to the load voltage at PCC and source current of phase-*a.* From this comparison, it can be concluded that the compensating performance of UPQC-3L is better than UPQC-2L.

Table 3.4: THD Comparison between UPQC-2L and UPQC-3L with voltage sag compensation

Type of disturbance (Voltage sag)	**UPQC-2L**		**UPQC-ML**	
	Load voltage (V)	Source current (A)	Load voltage (V)	Source current (A)
Before compensation	65.3	5.29*	65.3	5.61*
After compensation	79.5	6.66	80.5	7.45

3.5.4 Case-4: Voltage Swell with Non-linear Load

The performance of both topologies are conducted with voltage swell on source voltage with the magnitude of 20% from the nominal value. The load remain considered as the combination of linear and nonlinear.

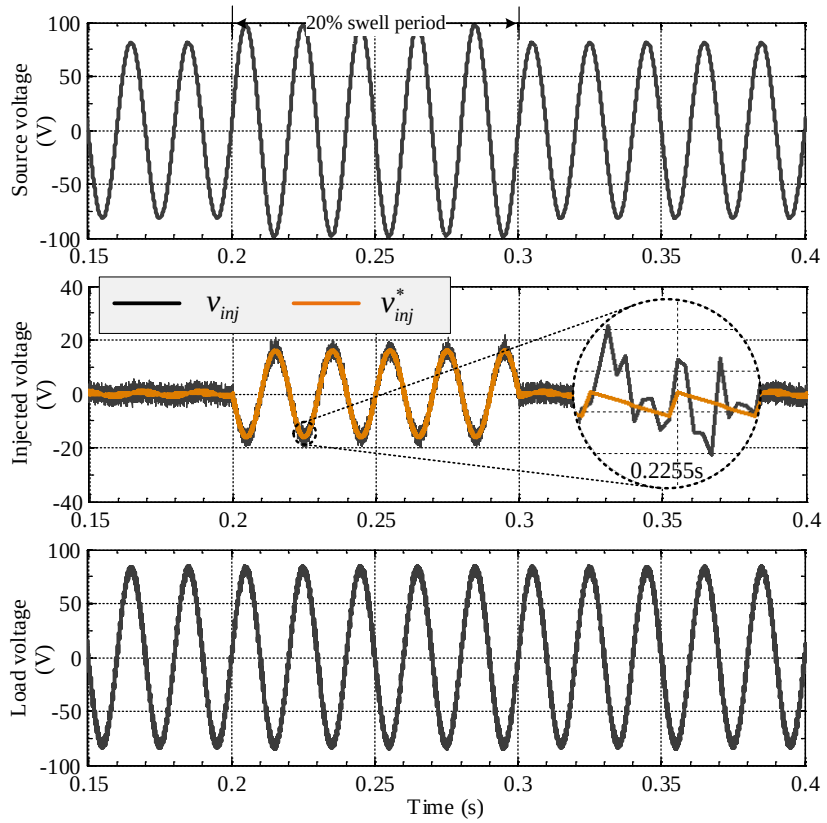


Fig. 3.42: Voltage swell compensation by the proposed control scheme showing for phase-*a* of UPQC-2L.

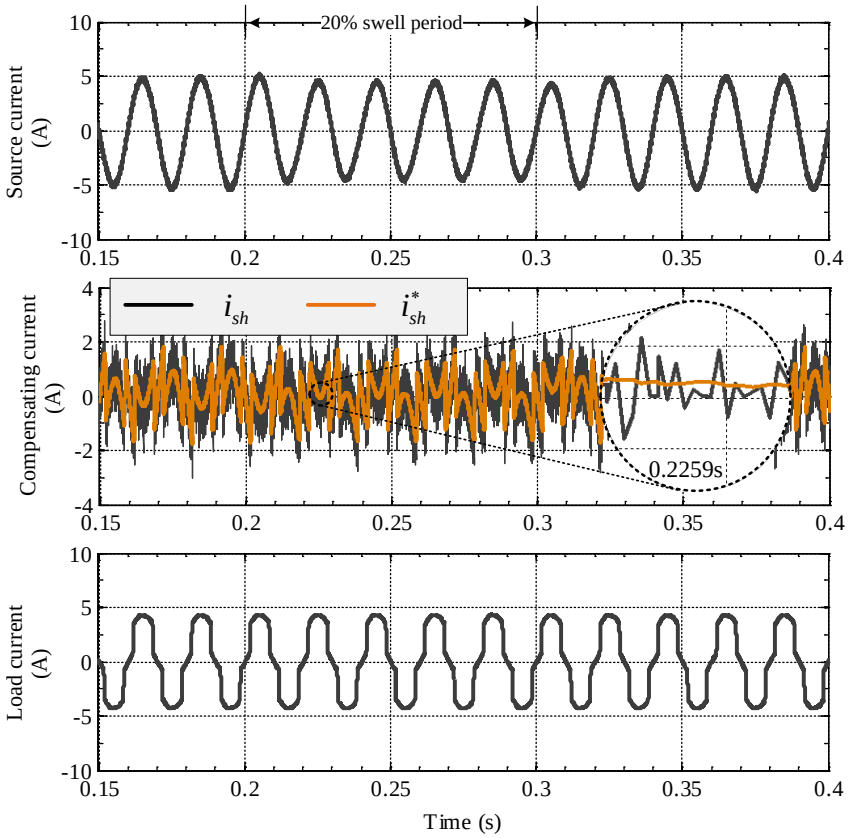
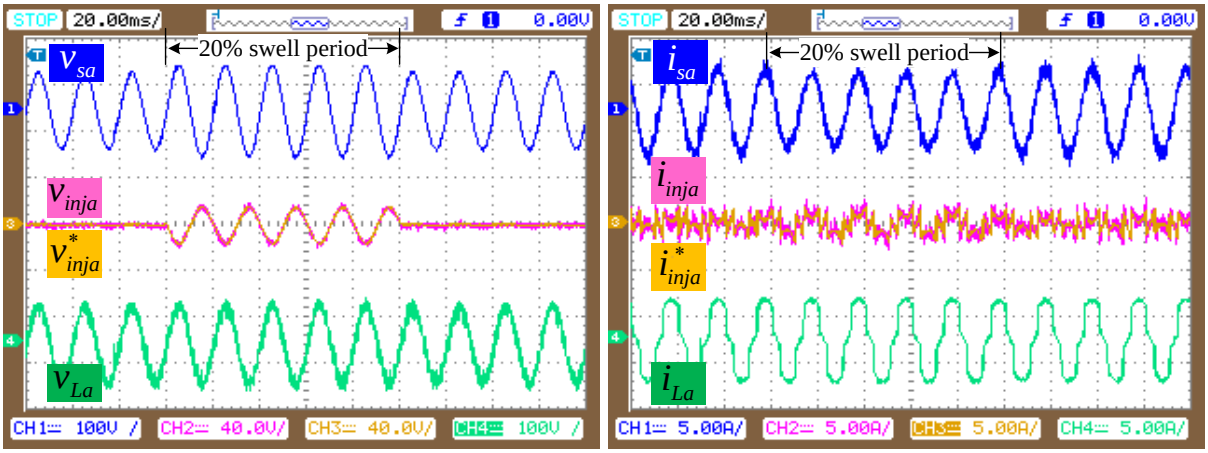


Fig. 3.43: Compensation of source current during voltage swell along with non-linear load by the proposed control scheme showing for phase-*a* of UPQC-2L.



(a) (b)

Fig. 3.44: Voltage swell compensation by the proposed control scheme showing for phase-*a*

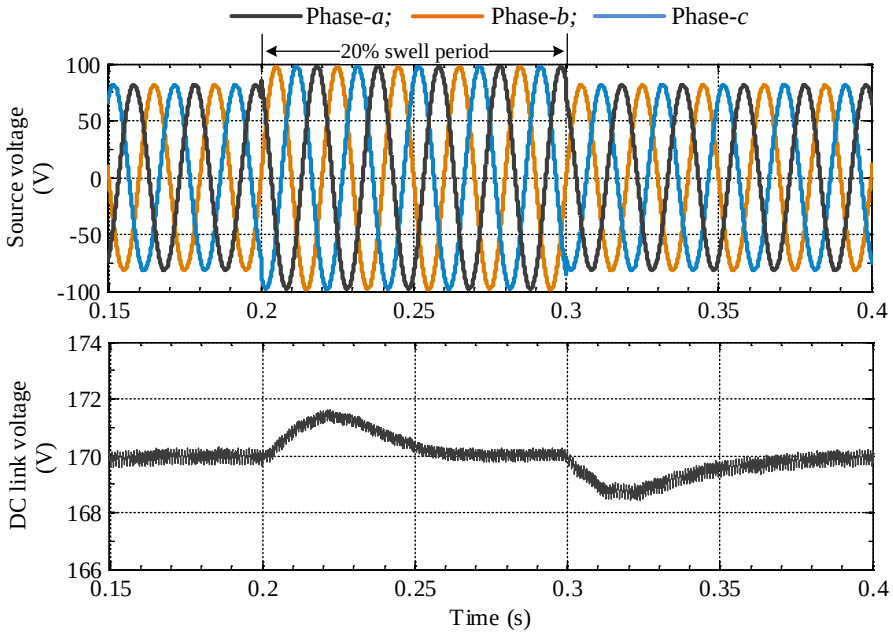


Fig. 3.45: DC-link voltage during swell compensation of UPQC-2L

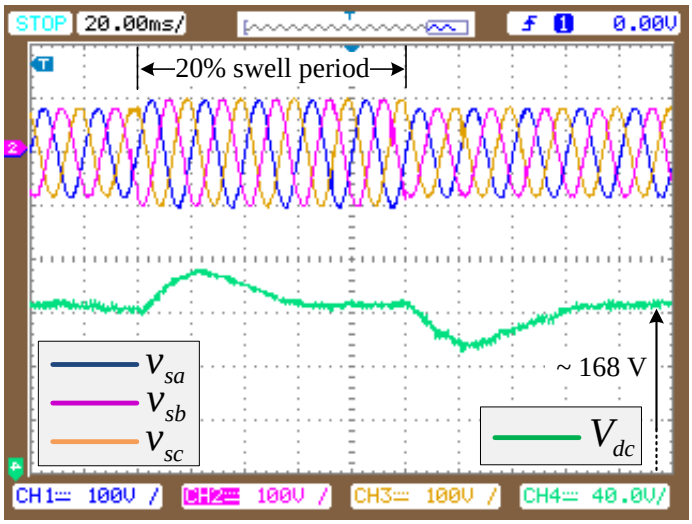


Fig. 3.46: Experimental scope results showing dc-link voltage during swell compensation of UPQC-2L

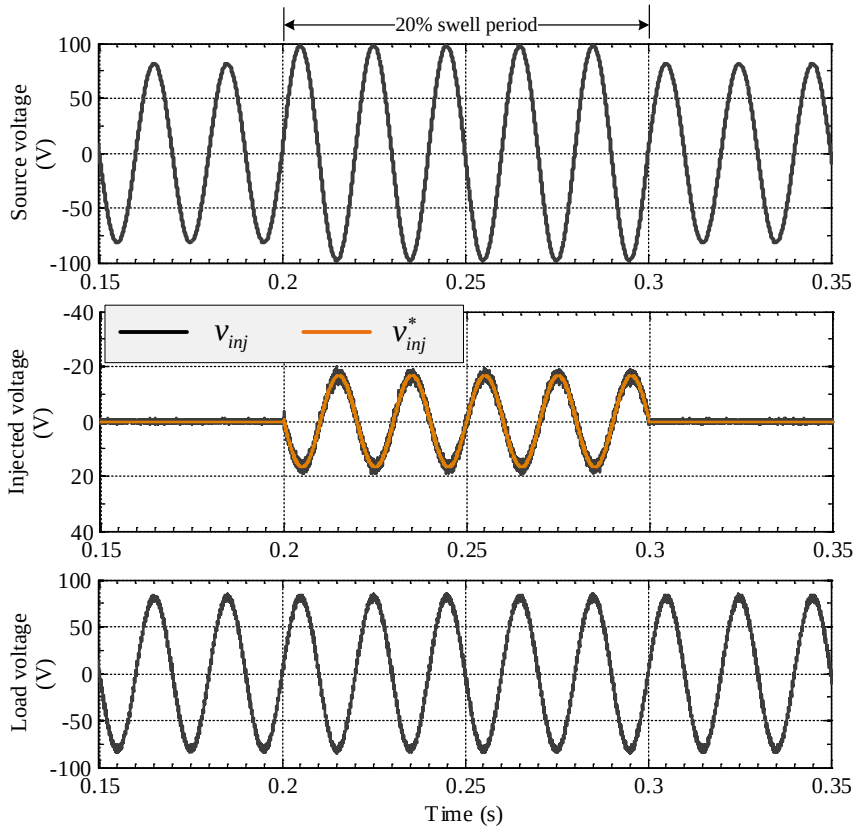


Fig. 3.47: Voltage swell compensation by the proposed control scheme showing for phase-*a* of UPQC-3L.

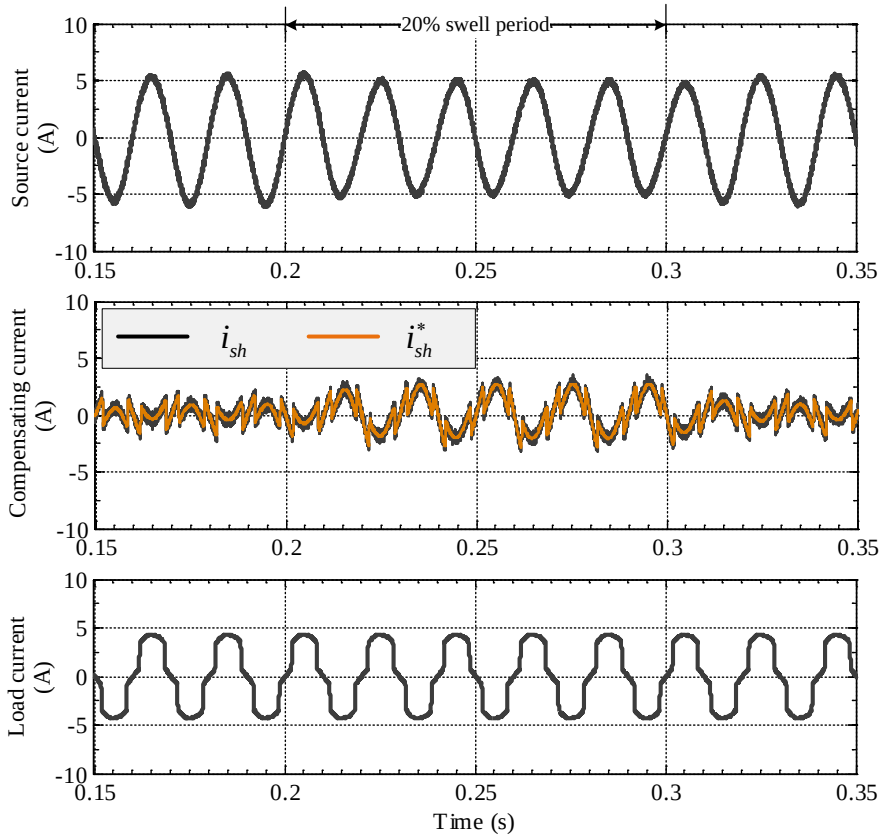
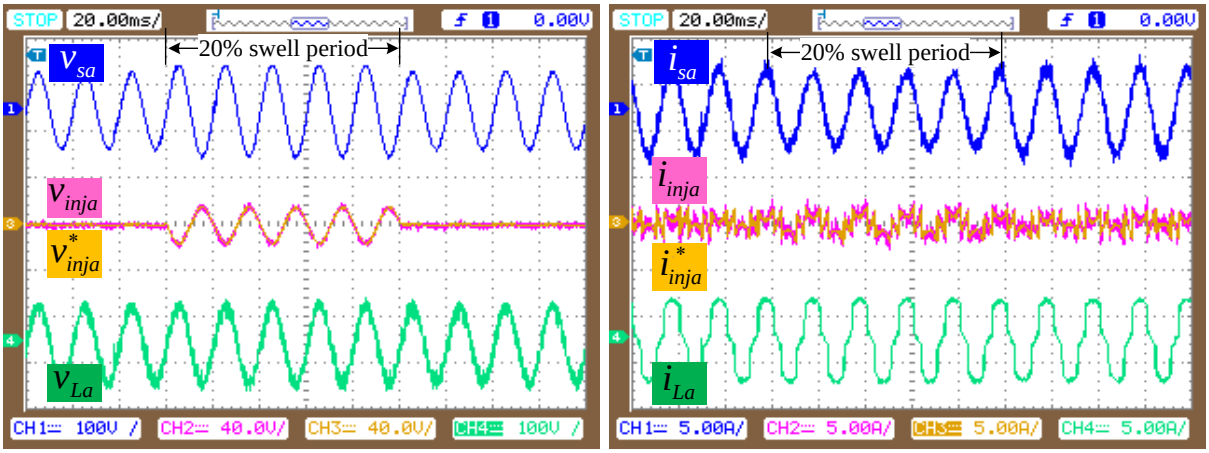


Fig. 3.48: Compensation of source current during voltage swell along with non-linear load by the proposed control scheme showing for phase-*a* of UPQC-3L.



(a) (b)

Fig. 3.49: Voltage swell compensation by the proposed control scheme showing for phase-*a*

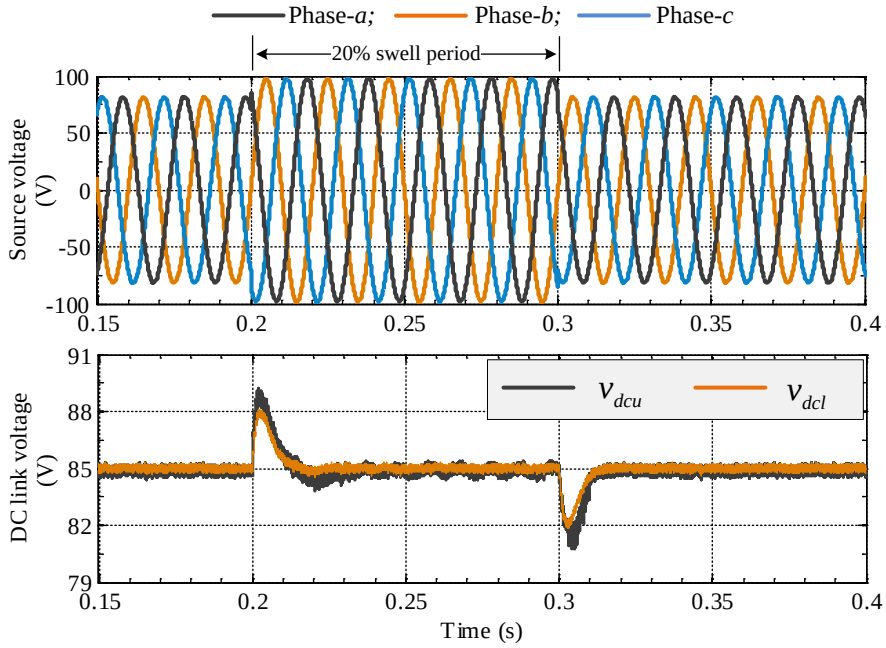


Fig. 3.50: DC-link voltage during swell compensation of UPQC-3L

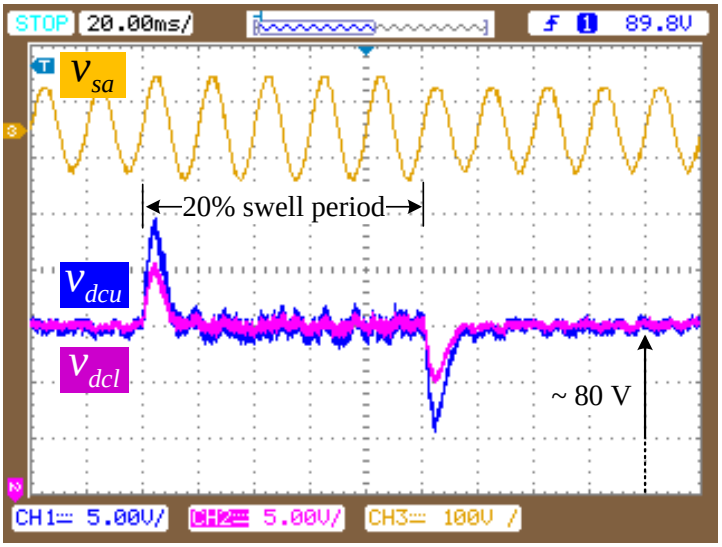


Fig. 3.51: Experimental scope results showing dc-link voltage during swell compensation of UPQC-3L

(A) UPQC-2L

The compensation against voltage swell is performed by the UPQC-2L by adopting the proposed control scheme. The voltage and current compensation characteristics are shown in Figures 3.42 and 3.43 respectively for simulation studies and parallel the corresponding experimental results are also presented in Figures 3.42. The load voltage is maintained at phase peak of 82.7V and 83.3V in simulation and experiment results respectively and the magnitude of source current is 4.86A in simulations and 5.3A in experiment during the swell compensation period. As compared to the voltage swell situation, the magnitude of source current is decreased as shunt converter sending active power back to the source during compensation. The dc-link voltage is measured as 170V and 168V in simulation and in experiment and are shown in Figure 3.45 and 3.46 respectively.

(B) UPQC-3L

From the results, which are shown in Figure 3.47 and 3.48, it can be observed that the magnitude of source voltage is compensated to 82.1V and 83.7V in simulation and in experiment respectively. The source current is measured as 4.11A and 5.54A in simulation and in experiment respectively shows that the shunt converter draws more current than UPQC-2L in order to supply power converter losses. The dc-link voltages are presented in Figures 3.50 and 3.51 for simulation and experiment. The difference between these results are identified as 5.8%, which gives the good compromise between simulation and experimental results.

(C) Summary

The quantitative comparison between UPQC-2L and UPQC-3L for this case study is given in Table 3.5, where phase peak fundamental values of simulations are considered for the comparison. The values are corresponding to the load voltage at PCC and source current of phase-*a.* From this comparison, it can be concluded that the compensating performance of UPQC-3L is better than UPQC-2L.

Table 3.5: THD Comparison between UPQC-2L and UPQC-3L with voltage swell compensation

Type of disturbance (Voltage swell)	**UPQC-2L**		**UPQC-ML**	
	Load voltage (V)	Source current (A)	Load voltage (V)	Source current (A)
Before compensation	98.0	5.26	98.0	5.68
After compensation	82.7	4.86	82.1	4.11

3.6 Conclusion

In this chapter, the application of proposed control strategy i.e. simplified MPC over UPQC-2L and UPQC-3L is verified with simulation and with experiment work. The simplified MPC scheme reduces the complicated mathematical computations, such that saving the processing time of the controller board without imposing much burden on it. The MPC controller is effectively compensates the variety of disturbances in the system with both topologies of UPQC-2L and UPQC-3L. The tracking of predictive signal with reference provides the better response during transient conditions. UPQC-3L over UPQC-2L provides the better compensation characteristics in overall all type of voltage and current distortions same as previous chapter. However, the size of the sampling time period is limited with the processing time of the controller board.

CHAPTER 4: HYBRID UNIFIED POWER QUALITY CONDITIONER

This chapter describes the hybrid structures incorporating passive power filters in conjunction with custom power devices (CPD) are capable of effectively decreasing the burden of VA loading as well as power semiconductor switch rating. This chapter proposes an analytical method to effectively control the dc-link voltage of Hybrid Unified Power Quality Conditioners (H-UPQC). Phase angle control (PAC) is integrated to H-UPQC to enable sharing of the reactive power burden between both shunt and series filter thereby decreasing the dc-link voltage requirement. Thus, the average switching losses and voltage stress of the semiconductor switches are significantly reduced. A detailed comparison between conventional UPQC and Hybrid UPQC is performed to analyse the dc- link voltage and the VA loading of both the structures.

4.1 Introduction

The performance of active filter is immersive influenced by voltage rating of dc-link capacitor. Generally, for shunt active filter, dc-link voltage possesses high value in comparison to peak value of the line to neutral voltage thus enabling and ensuring proper compensation at the source voltage peak to drive current through inductor hence tracking reference currents. To develop the relation between voltage at PCC (V_{PCC}), shunt converter output (V_{sh}), and dc-link voltage (V_{dc}), depending on the topology, various methods and approaches have been presented [10]–[15]. For example, for a three phase three leg system, assuming modulation factor $m_a = 1$, the maximum value of V_{dc} should be a minimum of twice $V_{PCC-max}$ [14], or $2\sqrt{2}V_{sh}$ [15]–[17]. Many researcher have used a higher value of dc capacitor voltage with a multiplication factor of 1.25 to 1.75 times of V_{PCC} based on the application is a common practice [10]–[15]. Equivalently, for series active filter, the value of dc-link voltage is maintained equal to the peak of line-line voltage [16]–[19] for three phase system, or at peak phase voltage of single phase system [20] for proper compensation.

The requirement of dc-link voltage for shunt and series active filter, for UPQC are different. These fluctuations in values lead to a provocative task to assign a common dc link of pertinent rating to achieve adequate shunt and series compensation. Conventionally, to achieve legitimate compensation the shunt filter requires higher dc-link voltage in comparison to the series active filter thus to fulfil this criterion, researchers have been left with no preference other than to choose common dc-link voltage on the basis of shunt active filter prerequisites. This leads to over rating of the series active filters as the requisites are less in comparison to shunt active filter. Thus, literature studies have revealed UPQC topologies with elevated dc-link voltage [21]–[24]. Hence, the voltage source inverters (VSIs) turn out to be bulky due to high value of dc-link capacitor. Additionally, the switch rating has to be chosen with increased value of voltage and current in return the entire cost and size upsurges. It has been observed in literatures, that few attempts have been initiated to minimize the inverter capacity by lowering the storage capacity of dc link voltage by

introducing hybrid APFs, thus intensifying system reliability. A combination of passive power filter (PPF) and APF constitutes the hybrid APF. The usage of MOSFETs as switching devices in the VSI of active filters cutbacks on the rating of active filter elements in hybrid filters with sensibly elevated rating. As a result, it operates at very high frequency contributing to fast response and decrement in size of ripple filter passive elements and size of dc bus capacitor [25].

4.1.1 Passive Power Filter

Passive filters are widely used to limit harmonic propagation, to improve power quality, to reduce harmonic distortion, and to provide reactive power compensation. These are designed for high-current and high-voltage applications. Many such filters are in operation for HVDC transmission systems, large industrial drives, static VAR compensators, and so on. The passive filters are classified into many categories such as shunt, series, hybrid, single tuned, double tuned, damped, band-pass, and high-pass power passive filters. In high power rating such as HVDC systems, they are very much in use even nowadays due to simplicity, low cost, robust structure, and benefits of meeting reactive power requirements in most of the applications at fundamental frequency. Moreover, they are also extensively used in a hybrid configuration of power filters, where major portion of filtering is taken care by passive filters. In majority cases, shunt passive filters have been considered more appropriate to mitigate the harmonic currents and partially to meet reactive power requirement of these loads and to relieve AC network from this problem, especially current-fed types of nonlinear loads (Thyristor converters with constant current dc load). However, in voltage-fed types of loads (diode rectifiers with DC capacitive filter), passive series filters are considered better for blocking of harmonic currents [5].

In case of shunt passive power filter, a single tuned filter that is a notch filter sharply tuned at one particular frequency can be used as single or multiple branches in the distribution system. It is a simple series RLC circuit, in which R is the resistance of the inductor as shown in Figure 4.1. The value of the capacitor, also known as the size of the filter, is decided by the reactive power requirements of the loads and its inductor value is decided by the tuned frequency. Therefore, these types of tuned or notch filters provide harmonic current and voltage reduction and power factor correction because of capacitive reactive power at fundamental frequency as this filter circuit behaves as capacitive impedance at fundamental frequency. The resistance of the reactor (inductor) decides the sharpness of tuning and is responsible for limiting the harmonic current to flow in the passive filter. Normally, the notch filters are used at more than one tuned frequency and may have more than one series RLC circuit for multiple harmonics. Sometimes two tuned filters are combined in one circuit. It is known as a double tuned or double band-pass filter, as shown in Figure 4.2(b), having minimum impedance at both the tuned frequencies [5].

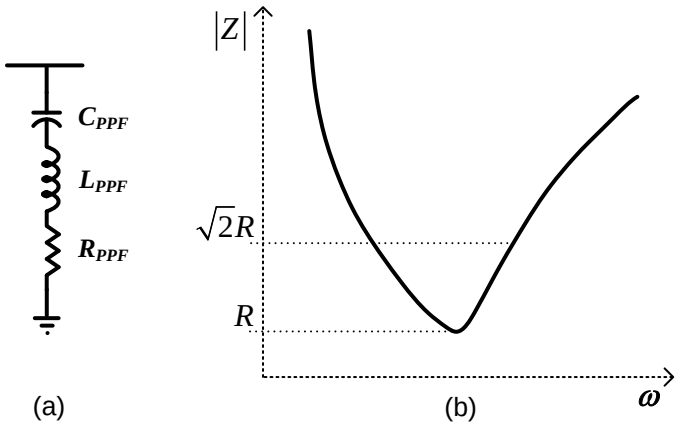


Fig. 4.1: Band-pass filter and its impedance frequency plot

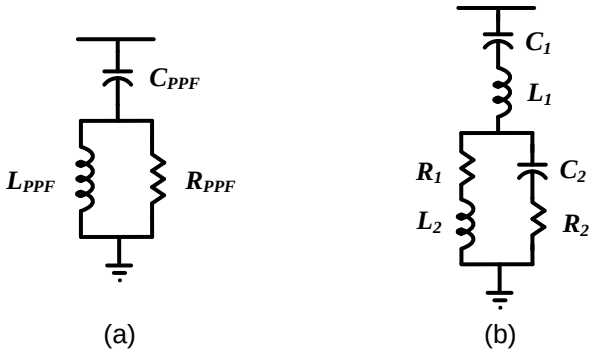


Fig. 4.2: (a) High-pass, (b) Double band-pass filter

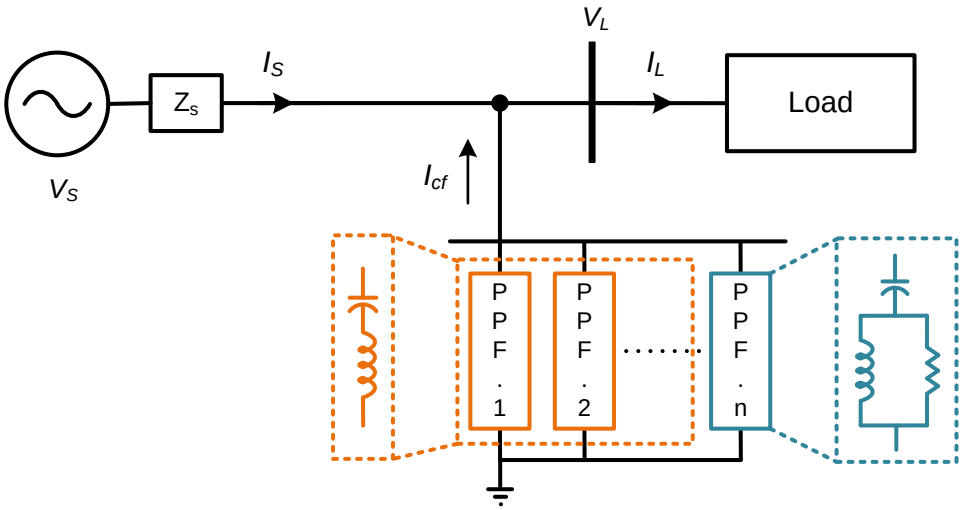


Fig. 4.3: Shunt passive power filters in distribution network

The main use of the double tuned filter is in high-voltage applications because of reduction in the number of inductors to be subjected to full line impulse voltages. More than two tuned filters (triple and quadruple) can also be combined in one circuit, but no specific advantage is achieved and there is difficulty in adjustment. Moreover, more than two tuned filters are rarely used in practice and only in a few applications. Other types of passive filters, shown in Figure 4.2(a), are known as high-pass filters that absorb all higher order harmonics. They are also known as damped filters as they provide damping due to the presence of a

resistor in the circuit. These filters have higher losses, but fortunately, at high frequencies not much higher currents and power losses are present in the loads. Normally each passive filter element employs three tuned filters, the first two being for the lowest dominant harmonics followed by high-pass filter elements. However, in some high-power applications such as HVDC systems, five tuned filter elements are used, having four for the four lower dominant harmonics and the fifth one as a high-pass damped filter element. In each passive filter element of shunt type, two lossless LC components are connected in series, for creating a harmonic valley to sink harmonic currents. All the three or five components of the passive shunt filter are connected in parallel as shown in Figure 4.3.

4.1.2 Passive Power Filter in Hybrid Configurations

Apart from the advantages of passive power filters as discussed in above sections, they also have few limitations and drawbacks such as problem of resonance with the source impedance, fixed compensation, and poor power factor at light loads due to excessive leading reactive power injection. Therefore, instead of using passive power filters alone in the system, they are combined with the active power filters and used as a hybrid power filters in the distribution system.

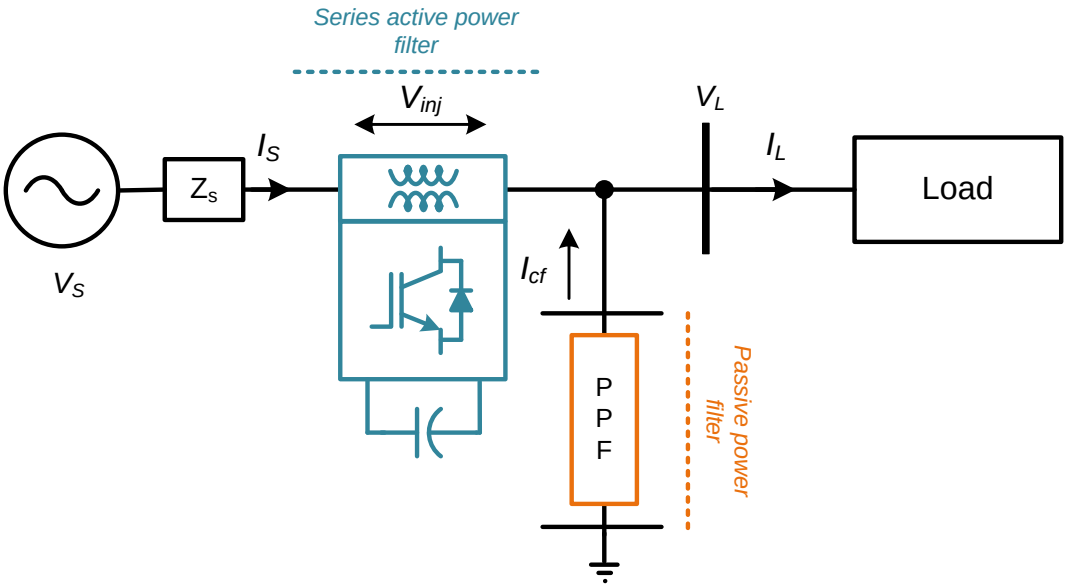


Fig. 4.4: Structure of series hybrid active power filter

A combination of shunt passive power filter (PPF) and series APF constitutes the series hybrid APF (SeHAPF) [226], [227], which is shown in Figure 4.4. SeHAPF is gaining popularity due to its reduced capacity and versatile usage [28-30]. An example to testify the theory would be a hybrid filter as unification of active series filter (5%) and passive series filter (20%) utilizing only 20% rating of load in case of voltage fed loads [225]. Industrial investigation and dedicated research is directed toward series active filters, as they are more popular than shunt counterpart due to its simple configuration and operating procedures. The typical structure of shunt hybrid APF (SHAPF) is shown in Figure 4.5. The SHAPFs are

series connection of passive and active filters for ease of operation at a conducive voltage and current in conjunction to high rating of active filter up to 60%–80% of the load [225], [231]–[234]. The minimum dc-link voltage requirement without negotiating the compensation efficiency is proposed for DSTATCOM in [235]. Also, the former requirement for different loading reactive power conditions are presented in [236], [237].

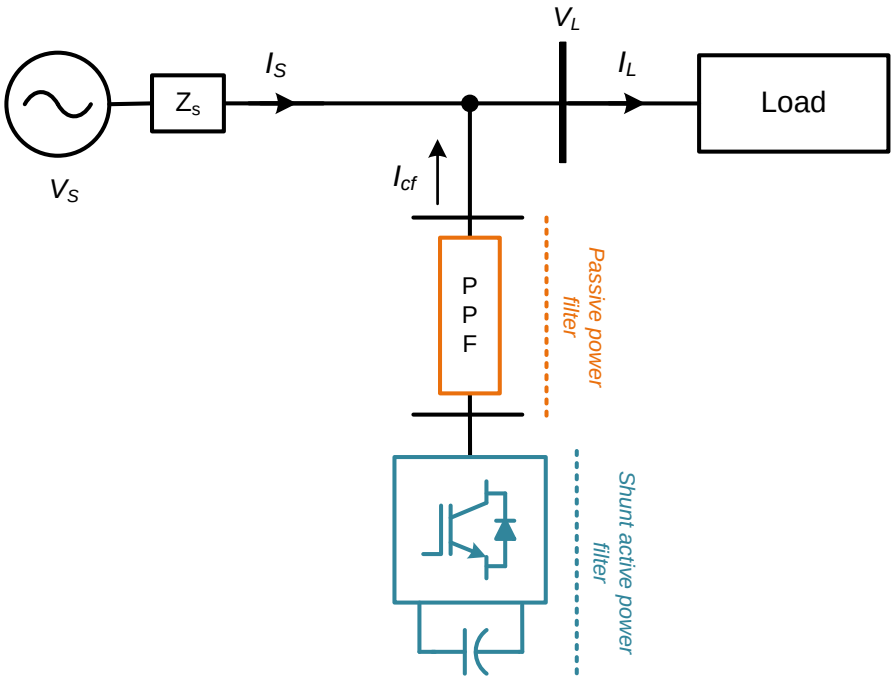


Fig. 4.5: Structure of shunt hybrid active power filter

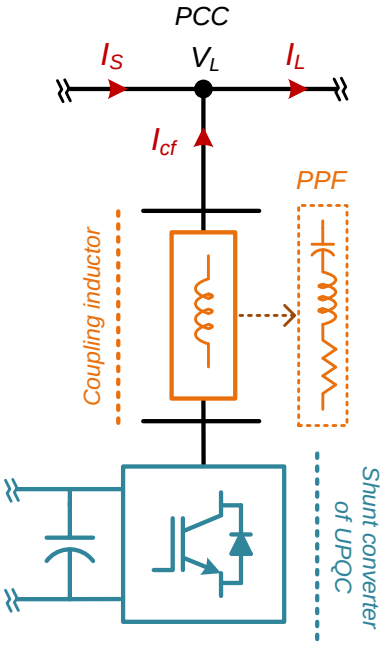


Fig. 4.6: Placement of passive power filter (PPF) in the UPQC application.

Unified power quality conditioner in comparison to series and shunt active filters receives less attention by the researchers by implementing hybrid structures with passive filters. A hybrid UPQC comprises a passive filter in series with the shunt converter as shown

in Figure 4.6. A hybrid UPQC (HUPQC) with a branch of passive filters attached to it, tuned specifically with 3rd, 5th, and 7th order harmonics has been proposed by L.H. Zhou et al [38]. This model reduces the capacity of dc-link of shunt convertor compared to conventional UPQC although no information was discussed on effect of reactive power loading. A different attempt was made to reduced dc-link capacity of UPQC in [239]. Here the author has cleverly chosen a dc-link voltage sufficient enough to perform the operation of both series and shunt converter without sabotaging the compensation capability.

4.2 Concept Background

The present work proposes an analytic method to control the dc-link voltage of hybrid UPQC. In majority of the UPQC based power quality conditioner, load reactive power compensation is performed by shunt APF. It is so because the utilization factor of the shunt APF is much elevated in comparison to series APF when utilized in steady state operation and is heavily influenced by load reactive power needs [40]–[42]. To achieve lower dc-link voltage, the compensation burden on shunt APF rating should be decreased [237]. This can be made possible by adopting phage angle control (PAC). PAC control is developed by V Khadkikar [241] to apply for UPQC-S topology. Unlike UPQC-P and UPQC-Q, this method enables the sharing of reactive power between series and shunt APFs by introducing a power angle difference between source and load voltage, maintaining the magnitude of voltages for both the APFs equal [240]. For better understanding the concept of PAC, the following section explains the phasor representation of UPQC-P, UPQC-Q and UPQC-S. Figure 4.7 shows the voltage phasor representation of UPQC-P during voltage sag and swell compensation. The various voltage quantities indicated in the Figure 4.7-4.9 represents as follows:

V_t – terminal voltage under normal operating condition

V_L – Load voltage at PCC under normal operating condition

V_t' – terminal voltage during voltage sag

V_t'' – terminal voltage during voltage swell

V_{inj}' – series injected voltage during voltage sag

V_{inj}'' – series injected voltage during voltage swell

V_L''' – terminal voltage after compensation of voltage sag/ swell

δ – phase shift angle between terminal voltage and load voltage

γ' – phase angle of series injected voltage during sag compensation

γ'' – phase angle of series injected voltage during swell compensation

The terminal voltage is considered as the voltage available to the customer loads after the deducting the drop (V_z) across the line/system impedance from the source voltage (V_s).

From Figure 4.7, it can be observed that the series APF injects the voltage in phase or out of phase with the terminal voltage to ensure the desirable magnitude at PCC in voltage sag and swell conditions respectively.

The resultant load voltage during voltage sag compensation is given by,

$$V_L\angle 0^0 = V_t'\angle 0^0 + V_{inj}'\angle 0^0 \tag{4.1}$$

The resultant load voltage during voltage swell compensation is given by,

$$V_L\angle 0^0 = V_t''\angle 0^0 + V_{inj}''\angle 180^0 \tag{4.2}$$

That means UPQC uses active power to compensate the voltage sag/swell such that this topology is named as UPQC-P.

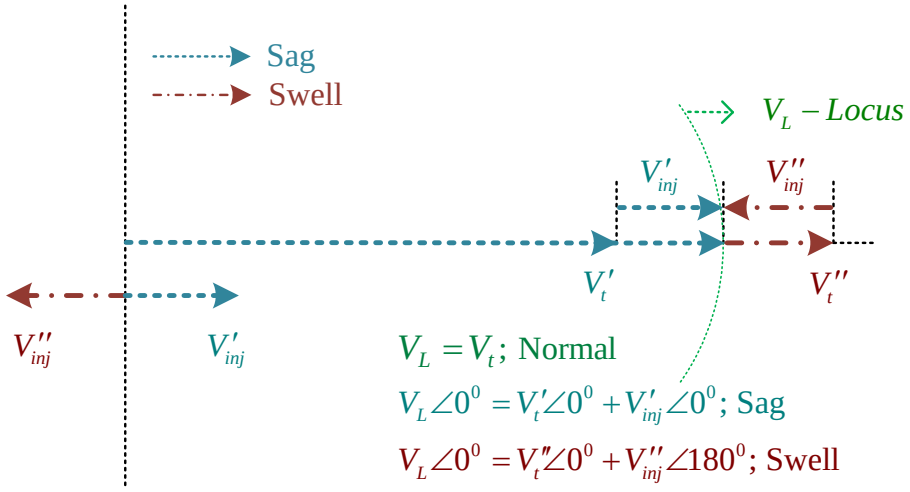


Fig. 4.7: Phasor representation of voltage compensation using UPQC-P [231]

In case of UPQC-Q, the series APF injects the voltage in quadrature with the terminal voltage to ensure the desirable magnitude at PCC in voltage sag, where as in case of voltage swell, the quadrature insertion of voltage never meet the locus of desirable load voltage that makes UPQC-Q is not suitable for voltage swell compensation. Figure 4.8 depicts the phasor representation of UPQC-Q.

The resultant load voltage during voltage sag compensation is given by,

$$V_L\angle 0^0 = V_t'\angle 0^0 + V_{inj}'\angle 0^0 \tag{4.3}$$

The resultant load voltage during voltage swell compensation is given by,

$$V_L\angle 0^0 \neq V_t''\angle 0^0 + V_{inj}''\angle 90^0 \tag{4.4}$$

That means UPQC uses reactive power to compensate the voltage sag such that this topology is named as UPQC-Q.

The injection of compensating voltage with certain phase angle with terminal voltage results, involving both active and reactive powers to operate UPQC during voltage sag/swell compensation makes the effective utilization of both APFs (series and shunt) of UPQC. This type of operation of UPQC named as UPQC-S and controlling the injecting phase angle is

called as phase angle control (PAC) in the literature. Figure 4.9 shows the phasor representation of voltage compensation by the UPQC-S.

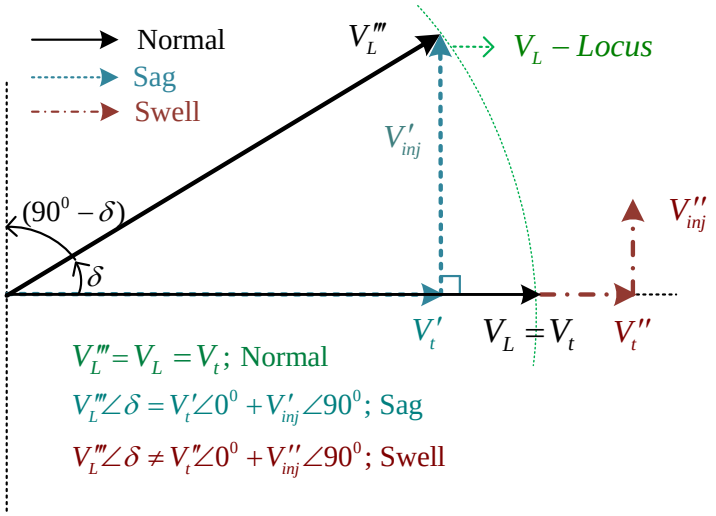


Fig. 4.8: Phasor representation of voltage compensation using UPQC-Q [231]

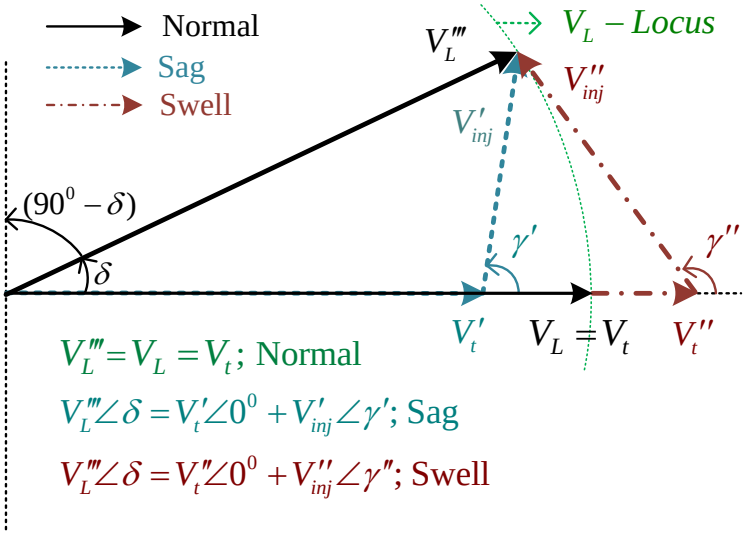


Fig. 4.9: Phasor representation of voltage compensation using UPQC-S [231]

The resultant load voltage during voltage sag compensation is given by,

$$V_L'''\angle\delta = V_t'\angle 0^0 + V_{inj}'\angle\gamma' \tag{4.5}$$

The resultant load voltage during voltage swell compensation is given by,

$$V_L'''\angle\delta = V_t''\angle 0^0 + V_{inj}''\angle\gamma'' \tag{4.6}$$

The present work makes an attempt to maintain the magnitude of voltage on the dc-link as low as possible by application of PAC to hybrid UPQC which enables to achieve further reduction in dc-link voltage in comparison to conventional UPQC.

The algorithm proposed in this article, indirectly identifies the range of minimum possible dc-link voltage for a given load power factor with suitable power angle between source and load voltage. A comparative study is performed for VA loadings and utilization of

power electronic converters of the designed hybrid UPQC under different conditions to the traditional UPQC.

4.3 Hybrid UPQC Topology Description

The configuration of three-phase three-wire hybrid UPQC is shown in Figure 4.10. It consists of passive power filter (PPF) connected in series with the shunt converter of the UPQC. The configuration of the power converter is accomplished by three-phase two level voltage source inverters (VSIs). Three-phase tuned power filter with an inductor in series conjunction with a capacitor in each phase configures the PPF. The PPF has three primary utility: reactive compensation, absorption of harmonic current produced by load, and coupling of the shunt converter of UPQC to the point of common coupling (PCC). As the load is variable, it is recommended to have different levels of reactive compensation and it has lowest possible impedance at the dominating harmonic frequencies to achieve good filtering characteristics.

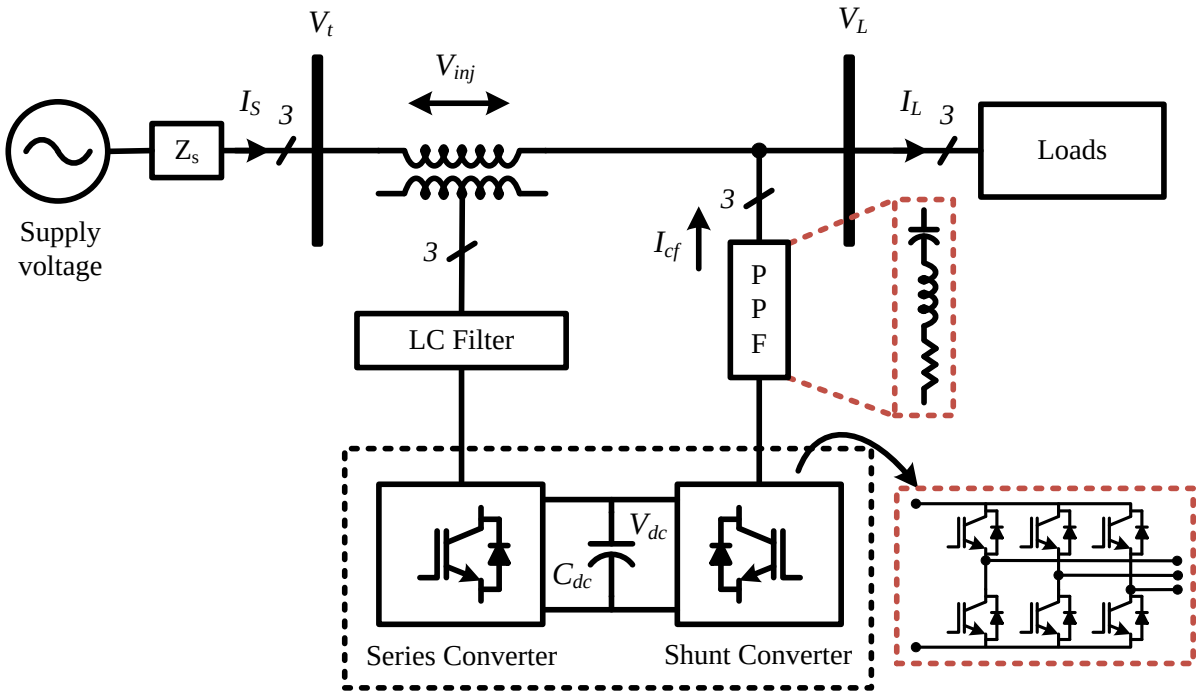


Fig. 4.10: Topology of hybrid UPQC

Implementation of separate passive filters for different harmonic frequencies would be bulky and extravagant cost wise. To overcome this issue, the frequency to be tuned for these passive filters are 5th and 7th harmonics. Likewise, the rating is selected as 75% of the total fundamental loading reactive power. The level of reactive power compensation of PPF is defined by the value of capacitance C_{PPF}.

$$Q_{PPF} = 2.\pi.f.V_L^2.C_{PPF} \tag{4.7}$$

Where Q_{PPF}– reactive power compensation by PPF, V_L– fundamental load voltage at PCC, f– system nominal frequency.

In case the prerequisite values are defined for parameters such as reactive power compensation Q_{PPF}, tuned harmonic frequency f_0, and a typical quality factor Q of PPF, then values of passive parameters such as capacitance (C_{PPF}), inductance (L_{PPF}) and resistance (R_{PPF}) are evaluated as [43],

$$C_{PPF} = \frac{Q_{PPF}}{2.\pi.f.V_L^2} \tag{4.8}$$

$$L_{PPF} = \frac{1}{(2.\pi.f_0)^2.C_{PPF}} \tag{4.9}$$

$$R_{PPF} = \frac{2.\pi.f_0.L_{PPF}}{Q} = \frac{1}{2.\pi.f_0.C_{PPF}.Q} \tag{4.10}$$

If PPF partially compensated some of the load reactive power, the remaining should be compensated by the shunt converter of the UPQC. For the simplicity let the source voltage (V_{s_j}), terminal voltage (V_{t_j}) and voltage at PCC (V_{L_j}) are harmonic free, where $j = a, b, c$. The dc link voltage (V_{dc}) is derived in terms of fundamental output voltage of shunt converter (V_{shf}). Figure 4.11 represents the single-phase fundamental equivalent model of hybrid UPQC.

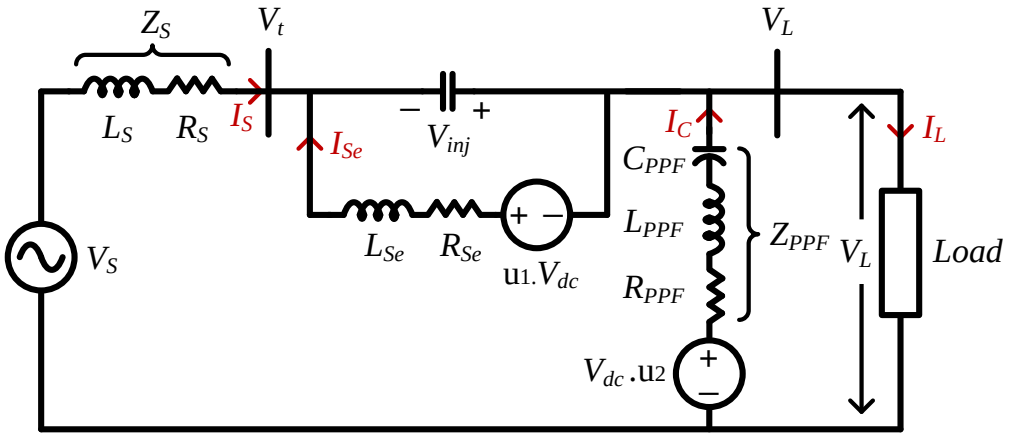


Fig. 4.11: Single-phase equivalent model of hybrid UPQC

V_{inj} represents the magnitude of injecting voltage by the series converter through injecting transformer in series with the terminal voltage for necessary compensation. The shunt converter is represented by an equivalent voltage source (V_{sh}) to provide the additional reactive power compensation in support of PPF. The fundamental output voltage generated by the shunt converter (V_{shf}) is given by,

$$V_{shf} = V_L - jI_{cf}.Z_{PPF} \tag{4.11}$$

Where, I_{cf}– fundamental compensating current provided by the shunt converter along with PPF, Z_{PPF}– impedance of PPF, V_L– fundamental load voltage at PCC.

The compensating current is a vector summation of active and reactive components

$$I_{cf} = I_{cfp} + jI_{cfq} \tag{4.12}$$

The active component (I_{cfp}) is responsible for converter losses, dc-link balancing and sag/swell compensation in support of series converter and reactive component (I_{cfq}) is equal to the total load reactive current component (I_{Lq}).

From (4.11) and (4.12),

$$V_{shf} = V_{shfp} + jV_{shfq} = V_L - jI_{cf}.Z_{PPF} \tag{4.13}$$

Using (4.12) and (4.13), the active and reactive components of shunt converter output is given by,

$$V_{shfp} = V_L + I_{cfq}.Z_{PPF} \tag{4.14}$$

$$V_{shq} = -I_{cfp}.Z_{PPF} \tag{4.15}$$

The fundamental reactive component of load current is given by,

$$I_{Lq} = I_L.\sin(\phi_L) = I_{cfq} \tag{4.16}$$

Where $\emptyset_L$– load power factor angle, I_L– fundamental load current.

By neglecting the losses in the converter, the output voltage of shunt converter without sag/swell in the network is derived by using (4.15) and (4.16),

$$V_{shf} = V_L + I_L.\sqrt{1-\cos^2(\phi_L)}.Z_{PPF} \tag{4.17}$$

Where $\cos\emptyset_L$– load power factor.

From (4,17), the minimum value of dc-link voltage of shunt converter of hybrid UPQC for the given load power factor is deduced as,

$$V_{dc} = 2\sqrt{2}\left\{V_L + I_L.\sqrt{1-\cos^2(\phi_L)}.Z_{PPF}\right\} \tag{4.18}$$

In abnormal terminal voltage conditions, the shunt converter supplies the required active power to series converter through dc-link for proper compensation, this leads to escalation in the active component of compensating current (I_{cfp}), which is not negligible. In this case, the minimum value of dc-link voltage is evaluated by (4.19),

$$V_{dc} = 2\sqrt{2}\left\{\sqrt{(V_L + I_{cfq}.Z_{PPF})^2 + (I_{cfp}.Z_{PPF})^2}\right\} \tag{4.19}$$

4.3.1 PAC based DC-Link Voltage Estimation

According to phase angle control (PAC) approach, the total reactive power of load is shared by both the converter of hybrid UPQC by controlling the injecting angle of compensating voltage (V_{inj}) via series converter unlike UPQC-P. This creates a phase shift of δ in between PCC voltage and actual terminal voltage. The magnitude of the reactive power supplied by series converter is dependent on the power angle shift δ and magnitude of

injected voltage. Figure 4.12 shows the phasor diagram of shunt and series compensations of hybrid UPQC under PAC approach illustrated for normal steady state, voltage sag and swell conditions.

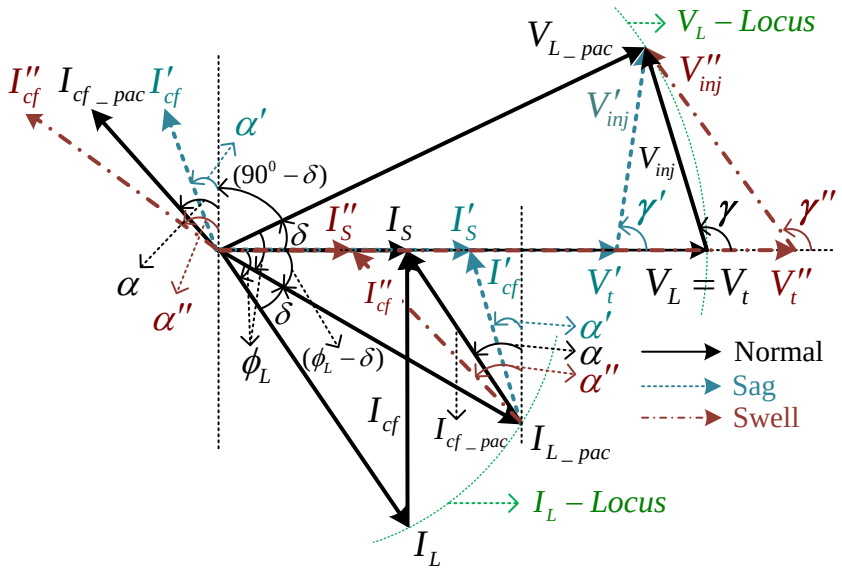


Fig. 4.12: PAC approach to hybrid UPQC

Let k is the sag/swell index, which is defined as $k = 1$ for normal voltage condition, $k < 1$ for voltage sag and $k > 1$ for voltage swell on terminal voltage. The magnitude of series injected voltage is tallied as given in (4.20).

$$V_{injf} = \sqrt{(V_L \cos\delta - kV_t)^2 + (V_L \sin\delta)^2} \tag{4.20}$$

The active and reactive components of $\bar{V}_{inj}$ are given as

$$V_{injfp} = V_L \cos\delta - kV_t \tag{4.21}$$

$$V_{injfq} = V_L \sin\delta \tag{4.22}$$

If shunt converter along with PPF is responsible to meet the reactive power demands by the load, the active power required by the load in normal as well as in condition to sag/swell is entirely burdened upon the source. Thus, the current drawn from the source is computed as [244].

$$I_S = \frac{I_L \cos\phi_L}{k} \tag{4.23}$$

The VA loading of series converter can be expressed as

$$S_{se} = \sqrt{(V_{injfp}.I_S)^2 + (V_{injfq}.I_S)^2} \tag{4.24}$$

The VA loading of series converter of H-UPQC is same as that of series converter of UPQC [241]. The compensating current supplied by the hybrid UPQC for load reactive power compensation and to series converter during sag/swell condition is to maintain power balance computed by (4.25),

$$I'_{cf} = \sqrt{(I_L \cos(\phi_L - \delta) - I_S)^2 + (I_L \sin(\phi_L - \delta))^2} \quad (4.25)$$

The active and reactive components of I'_{cf} are,

$$I'_{cfp} = I_L \cos(\phi_L - \delta) - I_S \quad (4.26)$$

$$I'_{cfq} = I_L \sin(\phi_L - \delta) \quad (4.27)$$

The active and reactive powers taken care of by the shunt converter of the hybrid UPQC are derived as

$$P_{sh} = V_L . I'_{cf} \cos(90^0 - \delta + \alpha) - I'_{cf} . R_{PPF} \quad (4.28)$$

$$Q_{sh} = V_L . I'_{cf} \sin(90^0 - \delta + \alpha) - Q_{PPF} \quad (4.29)$$

Where,

$$\alpha = \tan^{-1}\left[\frac{I'_{cfp}}{I'_{cfq}}\right] \quad (4.30)$$

The VA loading of shunt converter of hybrid UPQC is given by,

$$S_{sh} = \sqrt{P_{sh}^2 + Q_{sh}^2} \quad (4.31)$$

Summation of respective VA loading of series and shunt converters defines the overall VA loading of hybrid UPQC.

$$S_{H-UPQC} = S_{se} + S_{sh} \quad (4.32)$$

The least possible allowance of dc-link voltage of hybrid UPQC required under optimal VA loading by adoption of PAC is calculated as

$$V_{dc} = 2\sqrt{2}\left\{\sqrt{(V_L + I'_{cfq} . Z_{PPF})^2 + (I'_{cfp} . Z_{PPF})^2}\right\} \quad (4.33)$$

4.4 DC-Link Voltage Analysis of Hybrid UPQC

Table 4.1: Design parameters of PPF.

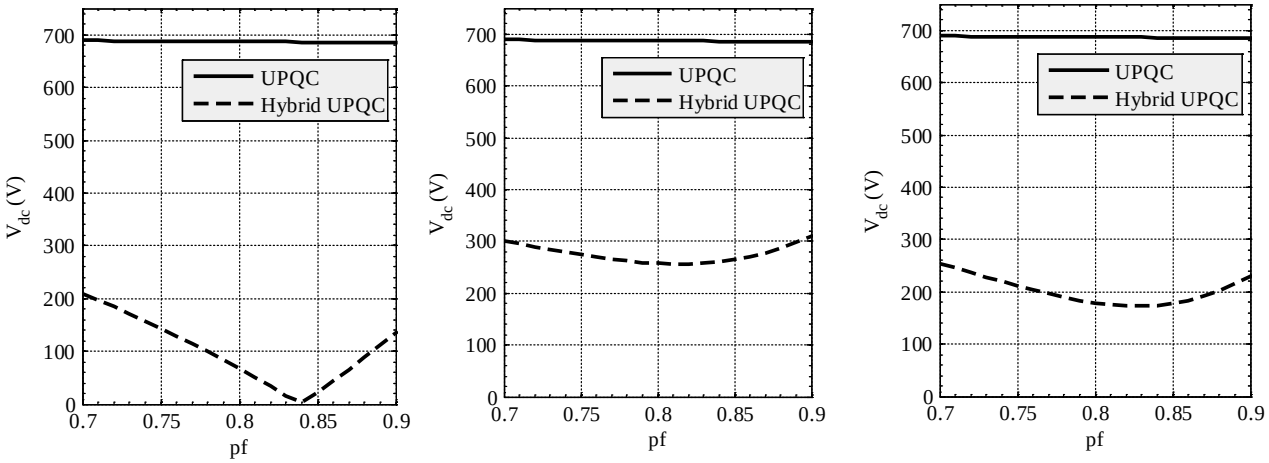
Description	Symbol	Parameter value
Capacitance	C_{PPF}	20.80 μF
Inductance	L_{PPF}	13.54 mH
Resistance	R_{PPF}	0.85 Ω

The analysis and interpretation of the dc-link voltage is illustrated by considering the following case. Let the load be a three-phase star connected lagging load of 1500W + j1500 VAR. The line-line load voltage is 415V and frequency of 50Hz. The segments of PPF are designed as illustrated in (4.8)–(4.10) for 75% of reactive power loading tuned to the

dominant of 5th and 7th harmonics and assuming quality factor (Q) as 45. The parameters of PPF as shown in Table I.

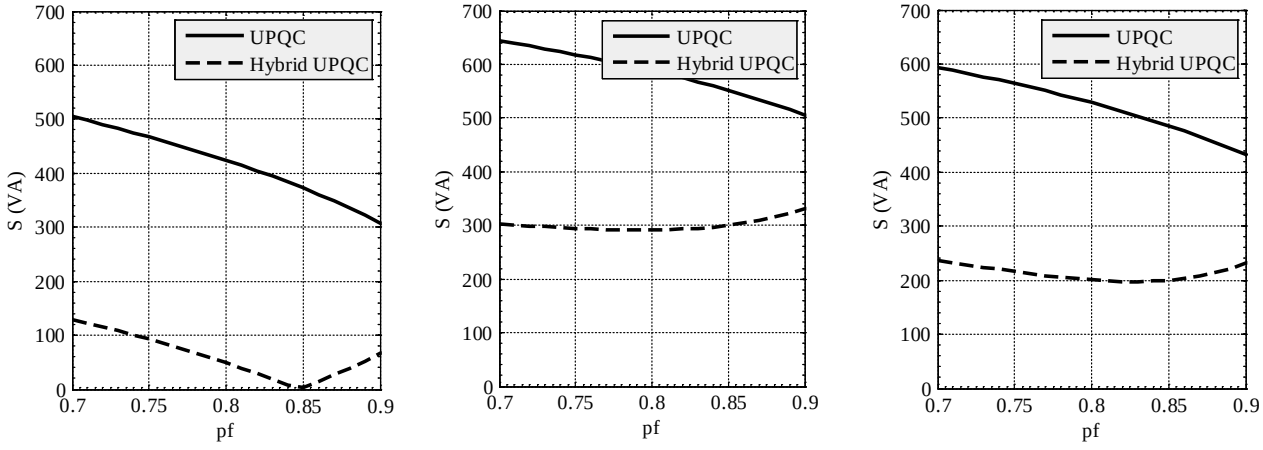
4.4.1 Analysis of Minimum DC-Link Voltage between UPQC and Hybrid UPQC

Figure 4.13 illustrates the minimum dc-link voltage required by shunt converter of both conventional and hybrid UPQC with variation in load power factor ranging from 0.7 to 0.9 which is calculated by (4.19) with an assumption that the terminal and PCC voltage are distortion free and at nominal levels.



(a) $k = 1$ (b) $k = 0.8$ (c) $k = 1.2$

Fig. 4.13: The variation of V_{dc} of UPQC and hybrid UPQC with respect to power factor



(a) $k = 1$ (b) $k = 0.8$ (c) $k = 1.2$

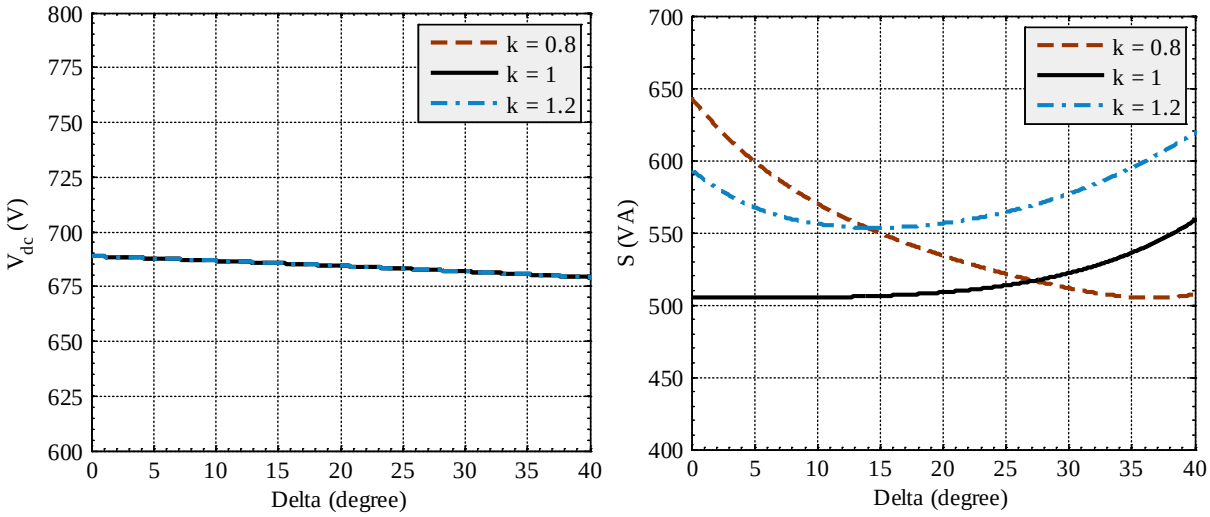
Fig. 4.14: The variation of VA loading of UPQC and hybrid UPQC with respect to power factor

The shunt converter in conventional UPQC is connected to PCC via coupling inductor of 6 mH on the contrary, Hybrid UPQC utilizes PPF. Minimum dc-link voltage is computed for conventional UPQC by substituting Z_L with coupling inductor reactance X_L as depicted in (4.19). Comparison of variation in dc-link voltage for both conventional and hybrid UPQC with respect to power factor is depicted in Figure 4.13 and corresponding variation in VA loading is plotted in Figure 4.14. Figure 4.13(a) presents the dc-link voltage requirement of both conventional UPQC and hybrid model with $k = 1$ and load power factor 0.7. It can be

observed that for the above constrains, conventional model requires 688.9 V whereas hybrid model demands only 209.3 V. A remarkable trend is observed for both traditional and hybrid model, on approaching a power factor of 0.9, a minute percentage of reduction is apprehended in the traditional UPQC whereas the V_{dc} desideratum to zero at 0.847 load power factor completely balancing the load reactive power by the PPF of hybrid UPQC. The variation of required V_{dc} is also evaluated for 20% of voltage sag/swell. The dc-link voltage requirement of conventional UPQC is unchanged while hybrid UPQC demands 301.71V at $k = 0.8$ and 254.53V at $k = 1.2$.

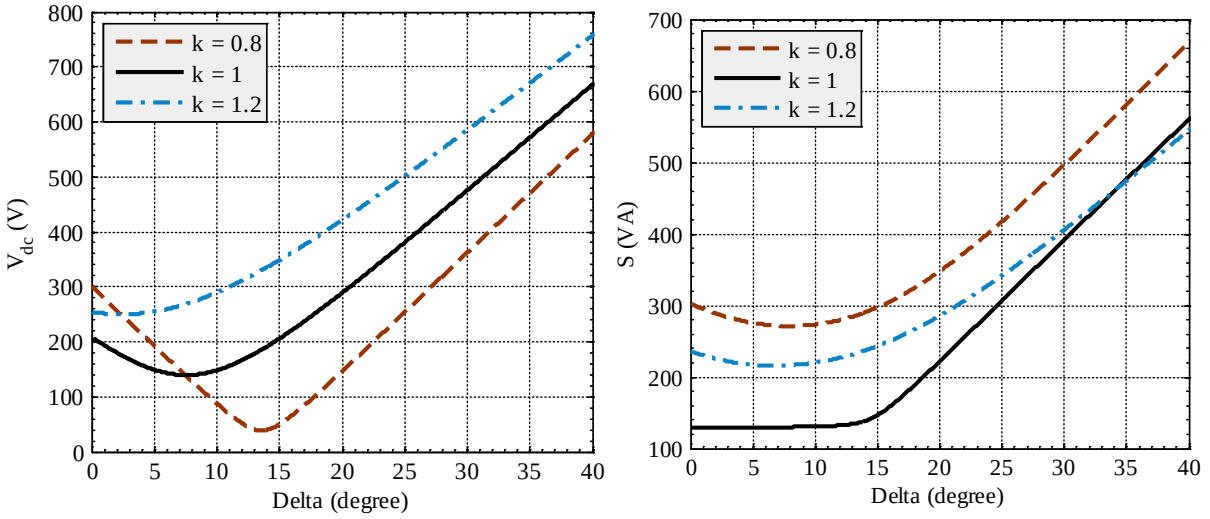
4.4.2 Evaluation of Minimum DC-Link Voltage using PAC Approach

Further investigation on dc-link voltage requirement is carried out by the applying phase angle control (PAC) approach for the traditional and hybrid topologies of UPQC.



(a) (b)

Fig. 4.15: The variation of dc-link voltage and VA loading with respect to δ of conventional UPQC



(a) (b)

Fig. 4.16: The variation of dc-link voltage and VA loading with respect to δ of hybrid UPQC

Figure 4.15 and 4.16, shows the variation of VA loading and dc-link voltage corresponding to angle δ at load lagging power factor of 0.7. It has been observed that in a condition of no sag/swell in the system, minimum VA loading of traditional and hybrid UPQC topology occurs at $\delta = 0^0$ and hybrid structure experiences lesser VA loading in comparison to traditional UPQC. Even though minimum loading occurs at $\delta = 0^0$, with the small increment of 0.07% of VA loading, the dc-link voltage is drastically decreased to 0.3% and 29.4% by shifting phase angle to $\delta = 10^0$ for traditional and hybrid UPQC, which can be observed from Figure 4.15 and 4.16 respectively. Decrement by 5% of the dc-link voltage can be achieved by shifting the angle δ to 1^0 with negligible increment in total VA loading of hybrid UPQC, whereas the dc-link voltage for traditional UPQC is approximately unaffected by the PAC approach.

The average increment in overall VA loading on hybrid UPQC is 0.002% with a minimum dc-link voltage of 139.67 V is achieved at $\delta = 7.64^0$. Investigations were carried out at 20% voltage sag/swell at 0.7 load power factor for both the structures. It is noticeable that with no deviation in the dc-link voltage, a significant change occurs in VA loading of traditional UPQC. For hybrid structure, deviation in dc-link voltage occurs for both $k = 0.8$ and $k = 1.2$. In comparison to the case of steady state ($k = 1$), both dc-link voltage and VA loading are enhanced for 20% voltage sag/ swell. At $\delta = 0^0$, voltage sag condition requires 301.71 V, whereas voltage swell requires 254.53 V. The minimum dc-link voltage of 38.74 V at $\delta = 13.63^0$ and 249.93 V at $\delta = 2.48^0$ is achieved for $k = 0.8$ and $k = 1.2$ respectively.

For a given load power factor, minimal dc-link voltage is obtained at different value of δ for steady state, 20% voltage sag and swell conditions. Hence, variation of the minimum value of dc link voltage and its corresponding value of δ in accordance to the supply voltage sag/swell condition. Table II and III depicts variation of dc-link voltage and VA loading for both traditional and hybrid model of UPQC at phase angles of 0^0, 5^0, 10^0, and 15^0.

Table 4.2: The dc-link voltage variation with respect to phase angle δ

Case	$k = 1$		$k = 0.8$		$k = 1.2$	
	V_{dc_UPQC} (V)	V_{dc_H-UPQC} (V)	V_{dc_UPQC} (V)	V_{dc_H-UPQC} (V)	V_{dc_UPQC} (V)	V_{dc_H-UPQC} (V)
$\delta = 0^0$	688.86	209.26	688.86	301.71	688.86	254.53
$\delta = 5^0$	687.89	149.68	687.89	193.59	687.89	254.64
$\delta = 10^0$	686.82	147.77	686.82	88.69	686.82	289.21
$\delta = 15^0$	685.67	205.15	685.67	49.16	685.68	347.88

The effect of PAC approach on dc-link voltage of traditional UPQC is not significant as in comparison with hybrid UPQC, which can be observed from Table II. It can thus be stated that prime focus of analysis should be of the minimum dc-link voltage of hybrid UPQC. The study proposes an algorithm to abstain habitual variation of dc-link voltage of hybrid UPQC stationed on system sag/ swell condition.

Table 4.3: The variation of VA loading with respect to phase angle δ

Case	$k=1$		$k=0.8$		$k=1.2$	
	S_{UPQC} (VA)	S_{H-UPQC} (VA)	S_{UPQC} (VA)	S_{H-UPQC} (VA)	S_{UPQC} (VA)	V_{H-UPQC} (VA)
$\delta=0^0$	504.77	129.77	643.39	302.97	593.92	236.22
$\delta=5^0$	504.81	129.83	599.68	275.87	567.69	217.35
$\delta=10^0$	505.17	130.74	570.32	273.30	556.18	220.11
$\delta=15^0$	506.25	146.10	549.79	297.14	553.47	243.11

4.4.3 Algorithm to Evaluate Optimal DC-Link Voltage

An algorithm is established to enable selection of a fixed value of dc-link voltage over a range of system sag/swell index. The working of algorithm is explained herein. Maximum dc-link voltages are evaluated for a range of ±10% of system sag/swell index at a given phase angle δ varying from 0^0 to 45^0 and stored in a memory location. An optimal dc-link is selected from the stored value in the memory location. Table II illustrates the variation in dc-link voltage in correspondence to phase angle δ. It is noted that maximum dc-link voltage 301.71 V is selected for 20% variation in voltage sag/swell condition at $\delta = 0^0$. Similarly 254.64 V, 289.21 V, 347.88 V are the maximum values of dc-link voltage at phase angle of 50, 100 and 150 respectively. The optimal dc-link voltage is the minimum value of the selected maximum values. Thus, the optimal dc-link voltage 254.64 V is selected as the best possible minimum dc-link voltage required with a 5^0 phase angle shift with system voltage variation from 20% sag to 20% swell.

The flowchart of the proposed algorithm is shown in Figure 4.17. Evaluation has been performed for computing the possible minimum dc-link voltage for a maximum range of 50% voltage sag/swell with a specified designed value of PPF at a given load power factor. Computations for the VA loading of series and shunt converters, overall VA loading and dc-link voltage are evaluated utilizing (15) and (20)–(22) for every step of phase angle for three cases of system distortion. These distortions are steady state and ±Δ variation in conjunction to voltage sag and swell conditions k_1, k_2 and k_3 respectively. The step size of phase angle

variation is chosen as 0.010. After evaluating the three sets of VA loading and dc-link voltage, the maximum value of dc-link voltage and corresponding loadings are stored in an array.

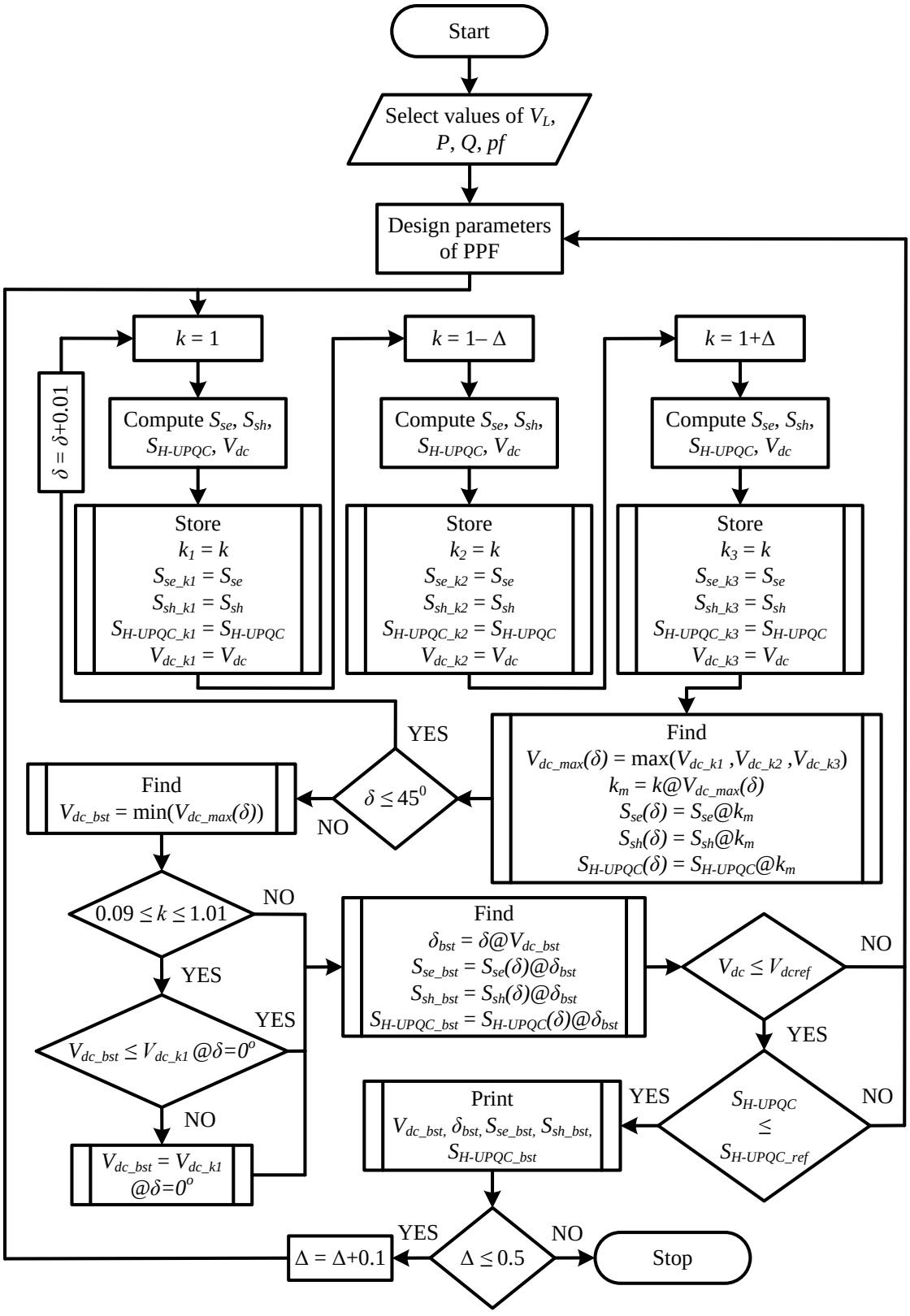


Fig. 4.17: Flowchart of the proposed algorithm to select optimal dc-link voltage of hybrid UPQC

The best possible minimum value of dc-link voltage is figured out from the stored maximum values. To avoid the selection of higher dc-link voltage than the actual required value at condition $k = 1$, further modification is added into the algorithm to select minimum dc-link voltage at this condition. The value of V_{dc} chosen is ensured to fall within the reference range from 0 to V_{dc_ref}. Additionally the overall VA loading corresponding to V_{dc} should be below the rated value.

4.5 Controller for Hybrid-UPQC

This section describes the reference signal generation for series and shunt converters of hybrid UPQC.

4.5.1 Reference Signal Generation for Series Converter

As the proposed algorithm uses the PAC control approach, which generates the required phase angle shift (δ) and optimal dc-link voltage. The generation of reference signals for series converter based on the pre-defined δ requires the series injecting angle (γ).

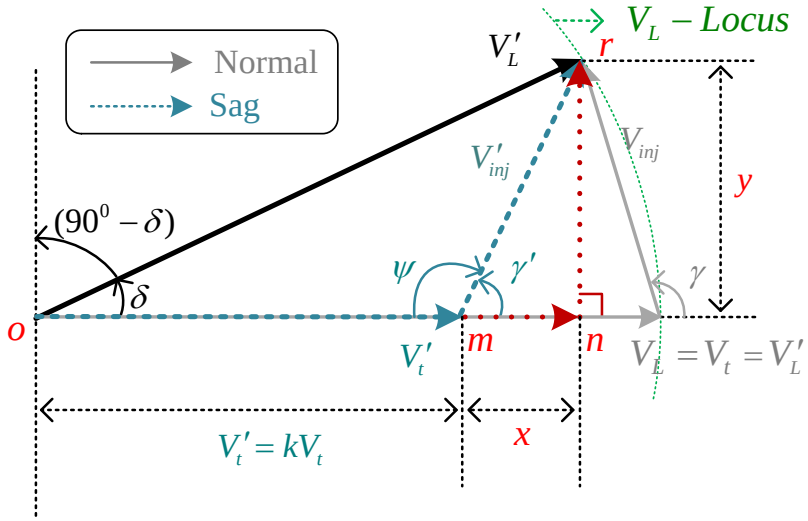


Fig. 4.18: Phasor diagram to estimate the series converter parameters

Figure 4.18 shows the detailed phasor diagram to determine the magnitude and phase of series injection voltage. The phase diagram is selected for the voltage sag condition. The derived series injection voltage magnitude and phase will be applicable for voltage swell condition also. The nominal terminal/load voltage is denoted as $V_t = V_L$. The sag/swell voltage (terminal voltage) is denoted as V'_t and is represented as,

$$k = V'_t / V_L \tag{4.34}$$

Where, *k* is the sag/swell index.

From the phasor of series injecting voltage (V'_{inj}) derived as (4.20), the magnitude can be deduced as (4.35)

$$\left|V'_{inj}\right| = V_L \sqrt{1 + k^2 - 2k\cos\delta} \tag{4.35}$$

The phase of V'_{inj} is calculate from Δmnr,

$$\angle\gamma' = \tan^{-1}\left[\frac{y}{x}\right] \tag{4.36}$$

Where, $y = V'_L sin\delta$, $x = V'_L cos\delta - V'_t$; V'_L –resultant load voltage after injecting voltage, which is equal to the nominal load voltage magnitude. On substituting x, y into (4.36), the phase of the injecting voltage can be derived as,

$$\angle\gamma' = \tan^{-1}\left[\frac{\sin\delta}{\cos\delta - k}\right] \tag{4.37}$$

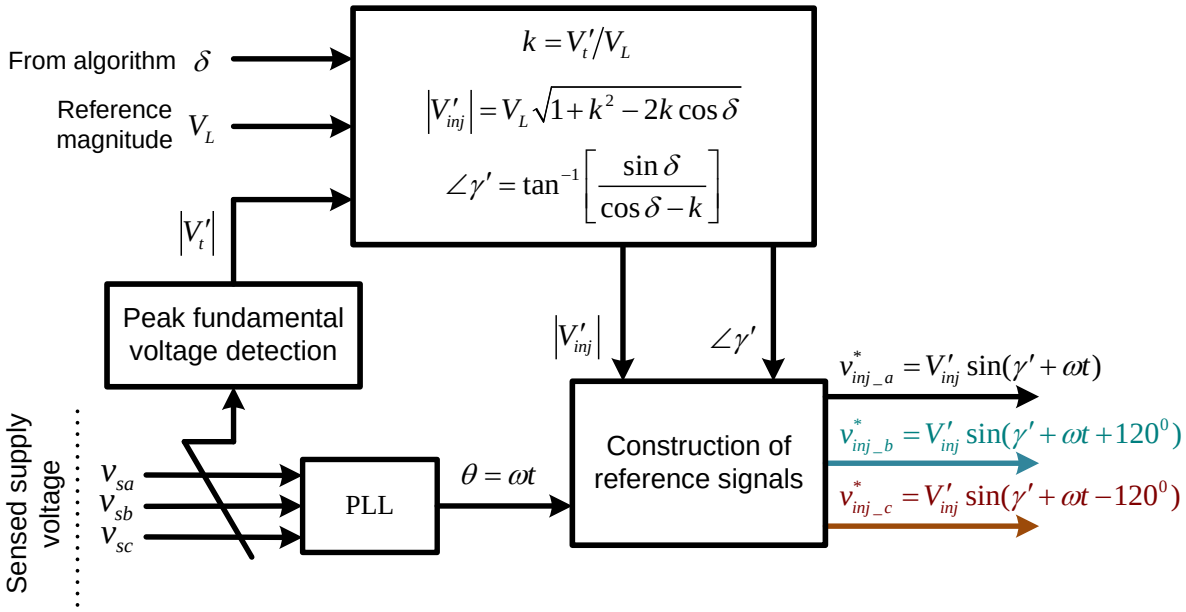


Fig. 4.19: Reference voltage signal generation of series converter

The control block diagram for the generation of series converter operation is shown in Figure 4.19. The inputs for the control block diagram to determine the instantaneous magnitude and phase angle of the series injected voltage involves, the reference load voltage at PCC, phase shift angle, which is obtained from the optimal dc-link voltage algorithm, the instantaneous terminal voltage from the peak fundamental voltage detection block. The instantaneous value of factor *k* is computed by measuring the peak value of the supply voltage in real time. The magnitude of series injected voltage V'_{inj} and its phase angle (γ') are then determined using (4.35) and (4.37). A phase locked loop (PLL) is used to synchronize and to generate instantaneous time variable reference signals ($V^*_{inj\_a}, V^*_{inj\_b}, V^*_{inj\_c}$). The reference signals thus generated give the necessary series injection voltages that will share the load reactive power and compensate for voltage sag/swell as formulated using the proposed approach. The error signal of actual and reference series voltage is utilized to perform the switching operation through PWM controller of series converter of hybrid UPQC as shown in Figure 4.20.

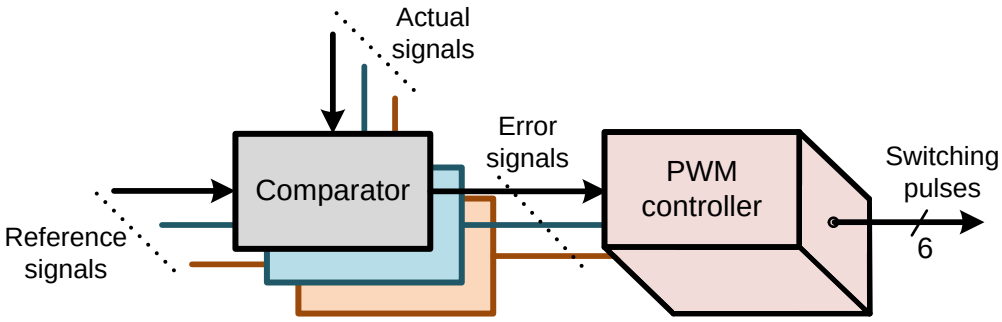


Fig. 4.20: PWM controller for generating switching pulses for converter switches

4.5.2 Reference Signal Generation for Shunt Converter

Instead of calculating the shunt injected current magnitude and its phase angle, an alternative approach is used for shunt part. In this approach reference source currents are generated directly. This indirect control of shunt compensating currents also helps to compensate the harmonics generated by the loads, if any. Therefore, there is no need of load harmonic content extraction. Thus, the reference source current signals can be generated by utilizing the instantaneous load-active power as discussed below. The instantaneous load active power is derived from the single-phase *p-q* theory in which, each phase voltages and currents of original system are defined as a pseudo two-phase system by giving $\pi/2$ lead. Thus, the resultant two-phase system can be represented in *α-β* coordinates. The actual load voltage and load current are considered as *α*-axis quantities, whereas the lead load voltage and lead load current are considered as *β*-axis quantities. Figure 4.21 shows the control block diagram to generate reference source current signals for shunt converter.

Equation (3.40) gives the instantaneous active and reactive power calculations for each phase separately by using voltages and currents derived in *α-β* plane i.e. $i_{Labc\_\alpha\beta}$ and $v_{Labc\_\alpha\beta}$. The per phase fundamental instantaneous load active power can be extracted from by using a low-pass filter (LPF). The average per phase instantaneous active power is calculated as (4.38) from three phase powers,

$$\overline{p}_{L/ph} = \frac{\overline{p}_{La} + \overline{p}_{Lb} + \overline{p}_{Lc}}{3} \tag{4.38}$$

Equation (4.39) gives the reference source current signal shown for phase-*a,* that would supply only fundamental load active power demand and losses associated with UPQC.

$$\begin{aligned} i^{*}_{s\_a}(t) &= \frac{v_{La\_\alpha}(t)}{v^2_{La\_\alpha} + v^2_{La\_\beta}}\left[\overline{p}_{L/ph} + p_{dc/ph}\right] \\ &= \frac{v_{La}(t)}{A_a}\left[\overline{p}_{L/ph} + p_{dc/ph}\right] \end{aligned} \tag{4.39}$$

In (4.39), $p_{dc/ph}$ is the precise amount of active power that should be taken from the source in order to maintain the dc-link voltage at constant level and to overcome the losses associated with UPQC. The quantity A_a is given in (4.40) and is derived as shown in Figure 3.4.

$$A_a = v_{La\_\alpha}^2 + v_{La\_\beta}^2 \tag{4.40}$$

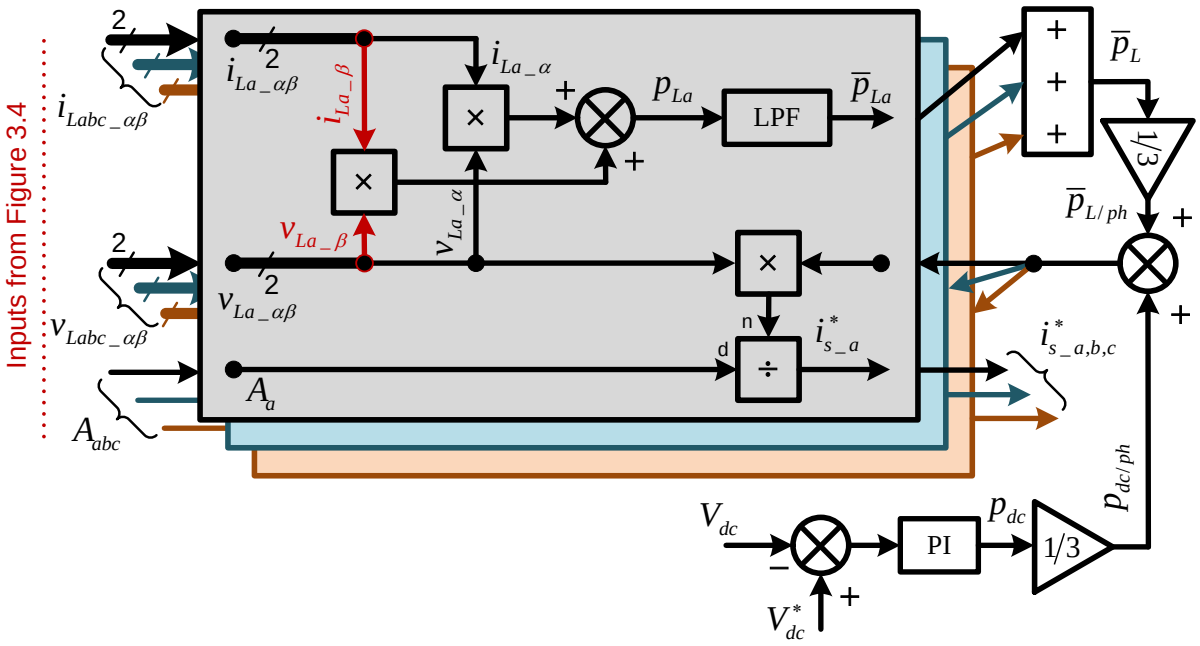


Fig. 4.21: Reference current signal generation for shunt converter

4.6 Simulation Study of Proposed Algorithm of DC-Link Voltage Analysis

The analysis of minimum dc-link voltage requirement is simulated in MATLAB Simulink platform for three cases of k: no voltage sag/swell, 20% sag and swell with the combination of load lagging power factor of 0.7 and the system parameter in consideration is depicted in section IV.

Table 4.4: Best possible dc-link voltage evaluate by the proposed algorithm

Sag/swell index range	V_{dc_H-UPQC} (V)	*Phase angle* δ *(degree)*
0% < k ≤ ±10%	200.86	4.96
±10% < k ≤ ±20%	215.19	4.00
±20% < k < ±30%	309.17	5.86
±30% < k ≤ ±40%	414.14	12.02
±40% < k ≤ ±50%	624.19	24.28

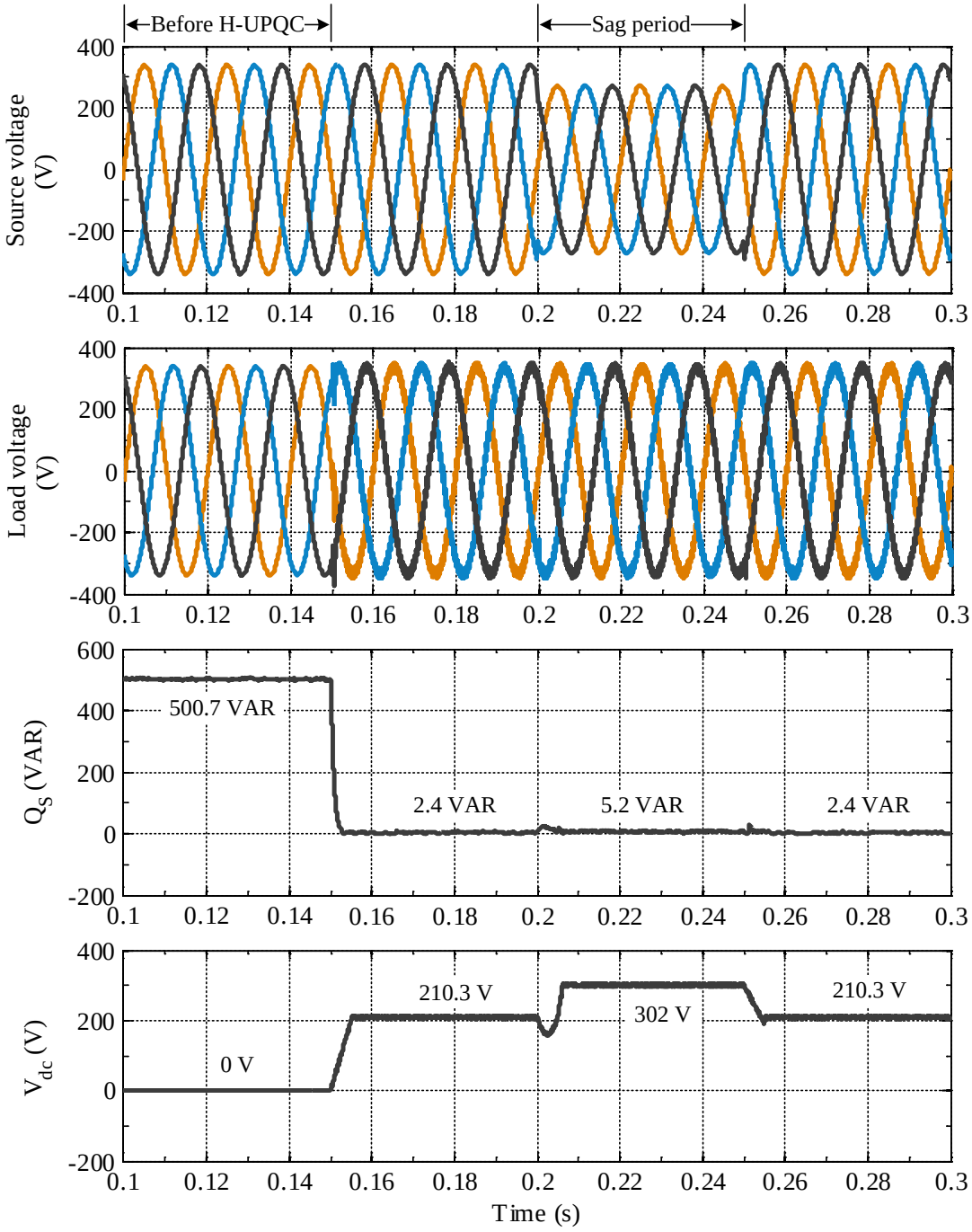


Fig. 4.22: Simulation results of minimum dc-link voltage requirement during voltage sag condition.

The optimal dc-link voltage required by hybrid UPQC is evaluated with direct approach ($\delta = 0^0$) and further possible reduction in V_{dc} is achieved through combination of PAC approach. The proposed algorithm is implemented to achieve the best feasible solution of fixed optimal dc-link voltage over a range of 10% of voltage sag/swell along with the designed values of PPF. Table. 4.4 summarizes the best possible minimum value of dc-link voltage evaluated for the proposed algorithm over different sag/swell index range. It is noticeable that the requirement of dc-link voltage elevates with increase in the depth of sag/swell evaluated at different phase angle shift.

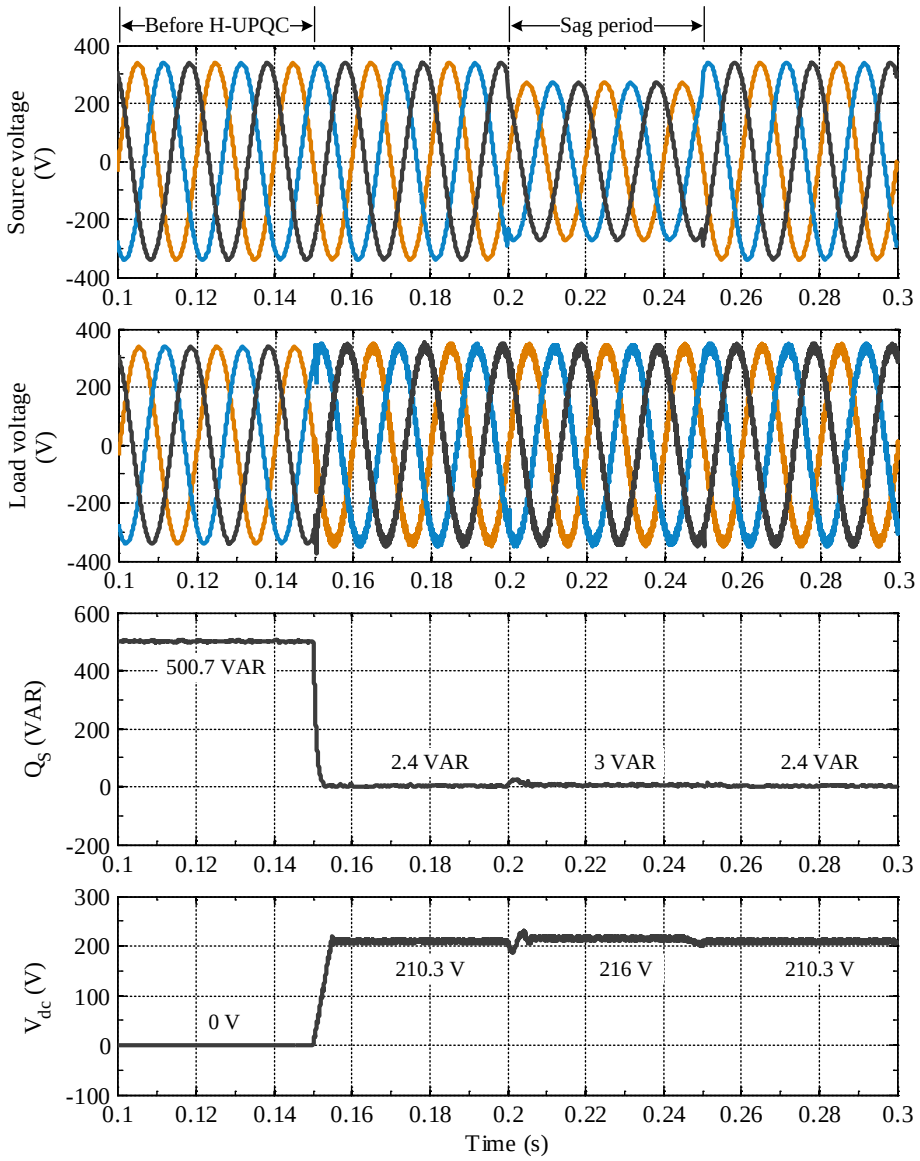
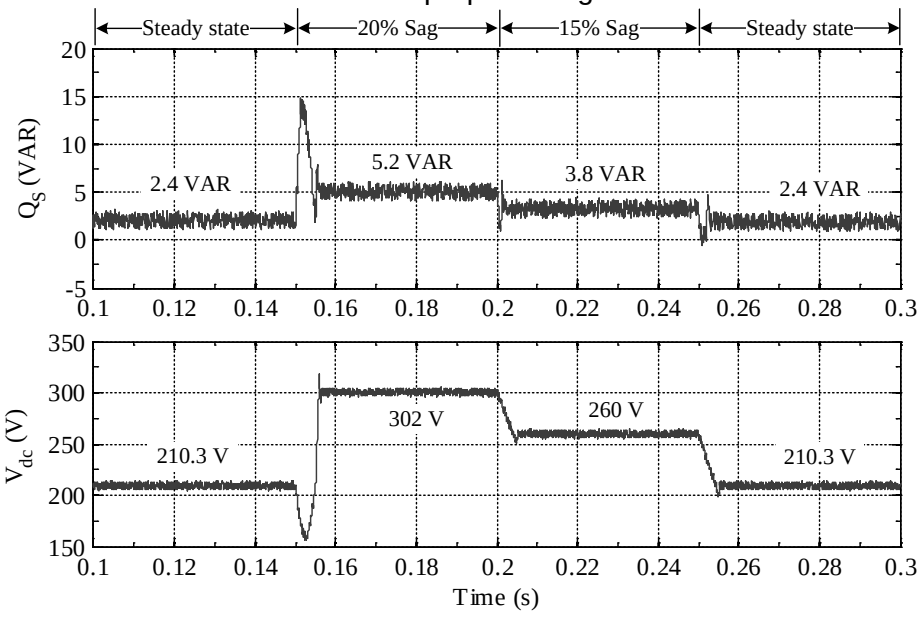
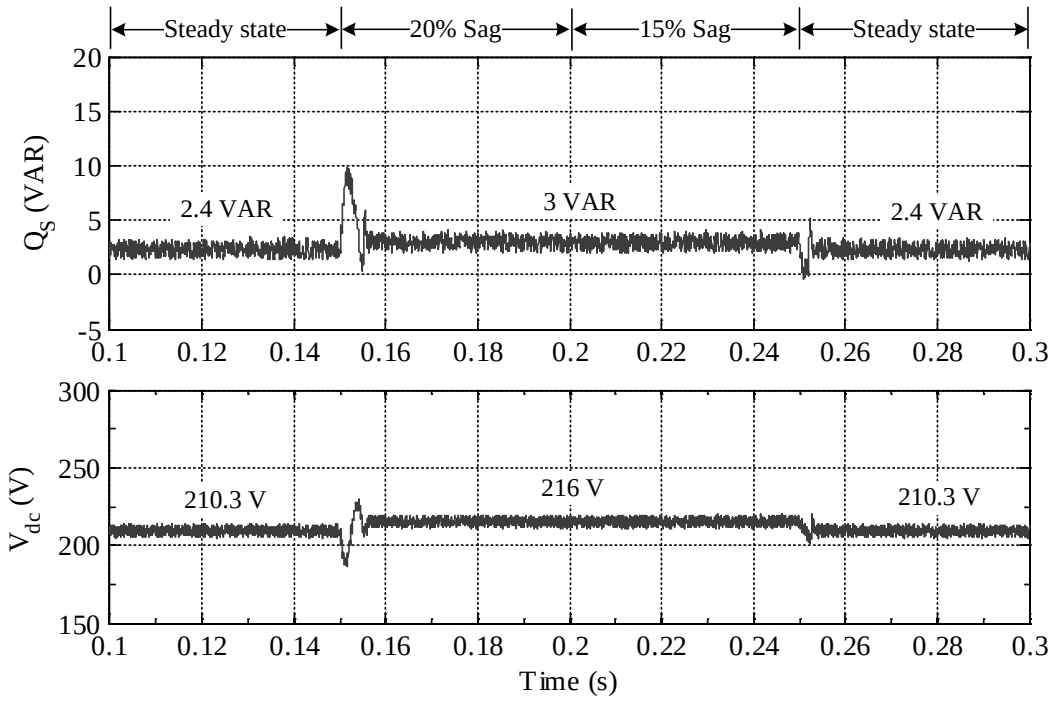


Fig. 4.23: Simulation results of minimum dc-link voltage requirement during voltage sag condition with proposed algorithm.



(a)



(b)

Fig. 4.24: Simulation results of minimum dc-link voltage requirement during variable voltage sag condition (a) with without application of PAC approach and (b) with proposed algorithm.

Figure 4.22 shows the simulated results of load voltage, source reactive power loading and required minimum dc-link voltage for voltage sag of 20% on source voltage. The reactive power required by the load is completely supplied by the source until UPQC is connected to the system at t =1.5s. When UPQC is triggered, the minimum dc-link voltage is settled at 210.3 V. The source supplies only 2.4 VARs to the load. Remnant reactive power is supplied by the hybrid UPQC.

To compensate the voltage sag, which is applied at t =2s, the hybrid UPQC demands 302 V and source supplies the average reactive power of 5.2 VARs in this condition. Whereas the reduced dc-link voltage of 216 V is sufficient to compensate the voltage sag with 3 VARs of source reactive power with the proposed algorithm, which is shown in Figure 4.23. If the voltage sag is varied from 20% to 15%, the minimum dc-link voltage demanded by hybrid UPQC is reduced to 260 V. In the proposed algorithm, the dc-link voltage is unchanged and is maintained at 216 V, which can be observed from Figure 4.24(b) In both the cases (shown in Figure 4.23 and 4.24(b)) when the voltage sag is removed, the proposed algorithm selected the minimum value of dc-link voltage of 210.3 V rather than 216V, which is evaluated for 20% voltage sag/swell deviation from k=1. Similarly the requirement of minimum dc-link voltage is analysed for voltage swell condition, presented in Figure 4.25 and 4.26. The presence of 20% voltage swell demands the dc-link voltage of 255 V and 216 V without and with PAC approach implanted with proposed algorithm. When the voltage swell is removed from the system, the minimum value of dc-link voltage is selected by the proposed algorithm as explained in sag condition.

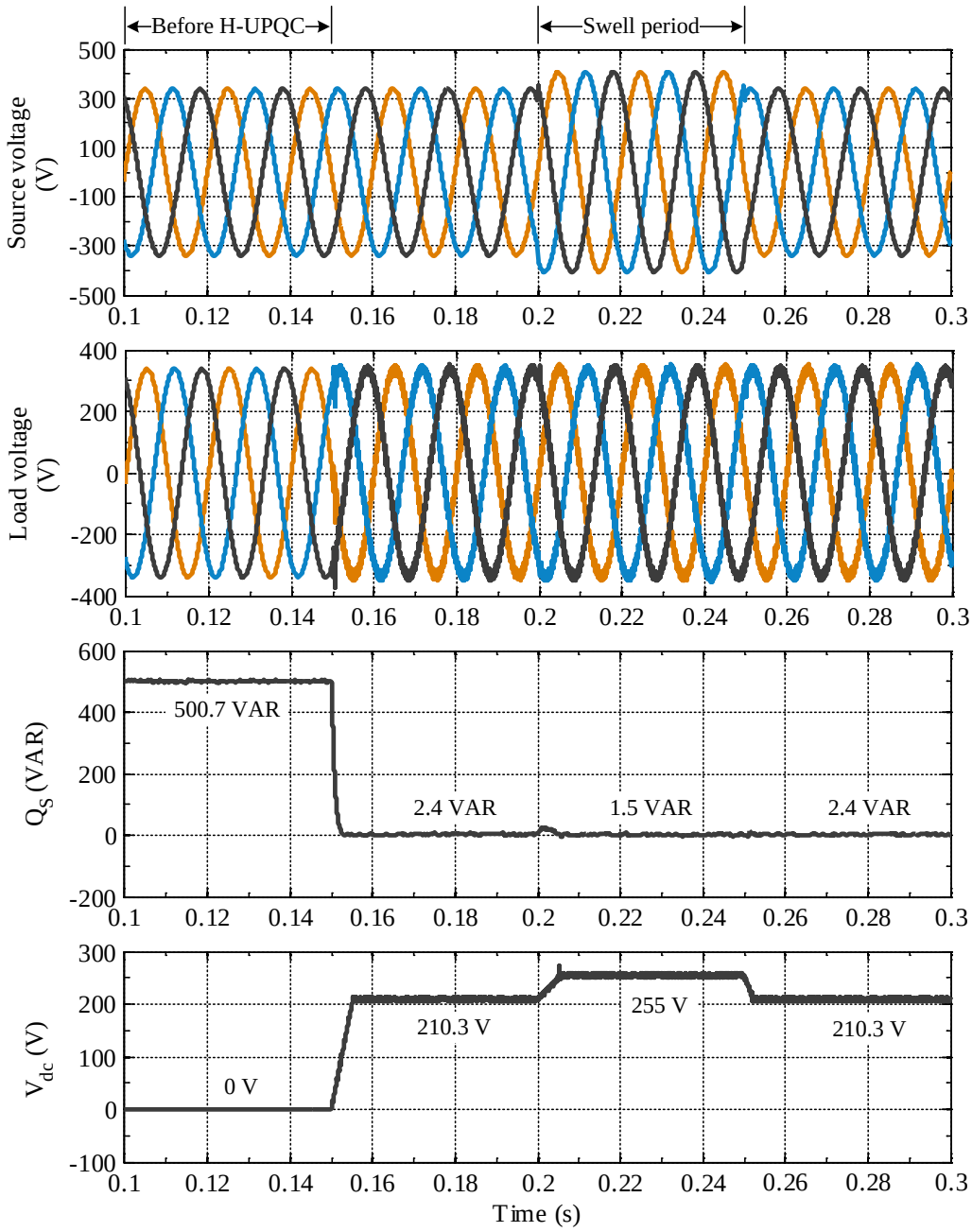


Fig. 4.25: Simulation results of minimum dc-link voltage requirement during voltage swell condition.

From Figure 4.27, it can be observed that the minimum dc-link voltage is varied as voltage swell shifts from 20% to 15% if PAC approach is not implemented, whereas in proposed algorithm the dc-link voltage is unchanged as similar to voltage sag condition, because of the sag/swell index range of ±20%.

4.7 Experimental Verification

The competence of the proposed algorithm is validated through experimental setup, which is developed in the laboratory using system parameters designed same as simulation studies using (4.8-4.10) at source phase rms voltage of 100 V with three-phase linear lagging power factor load of 600W+ j600VAR.

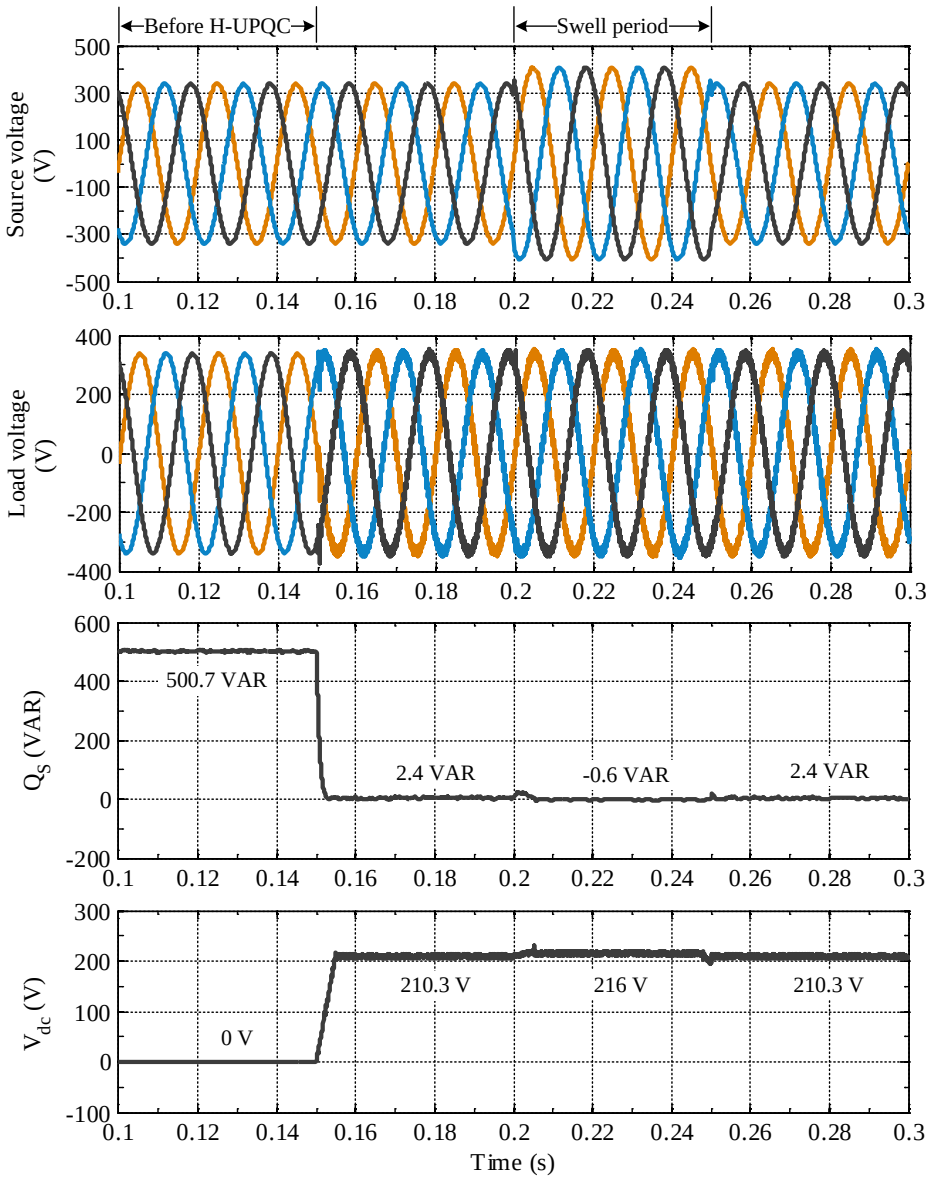
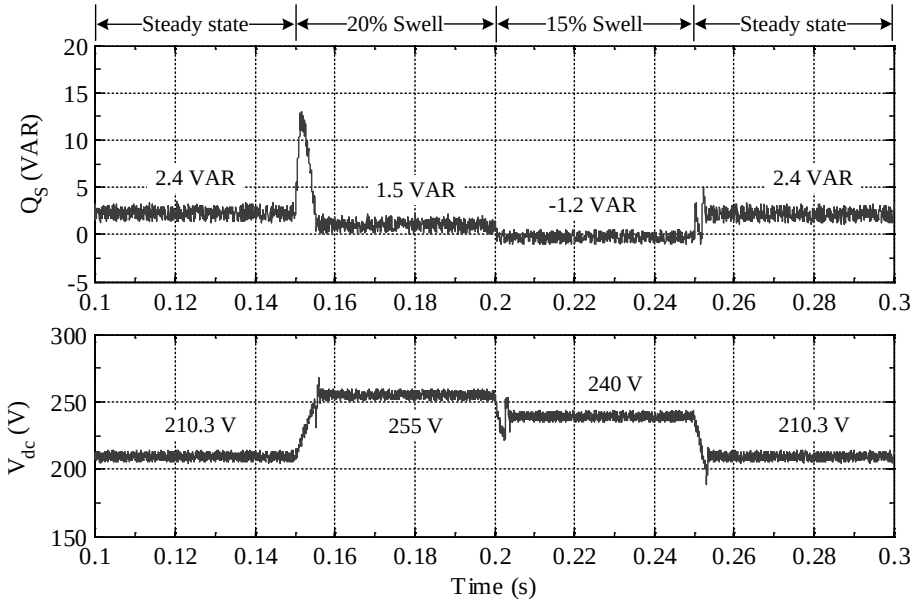
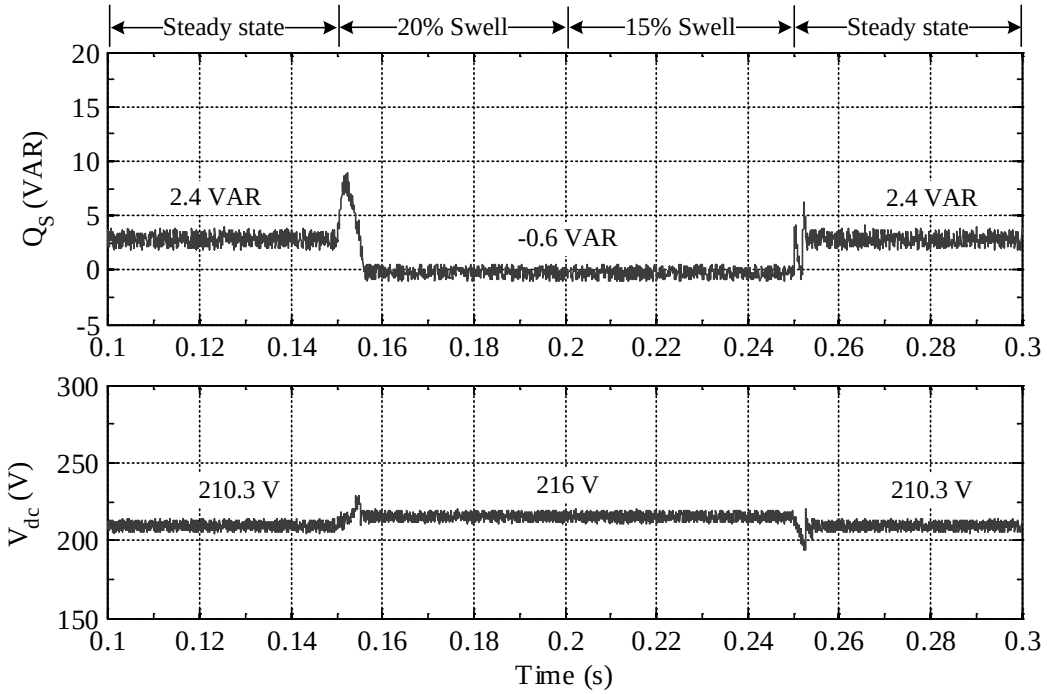


Fig. 4.26: Simulation results of minimum dc-link voltage requirement during voltage swell condition with proposed algorithm.



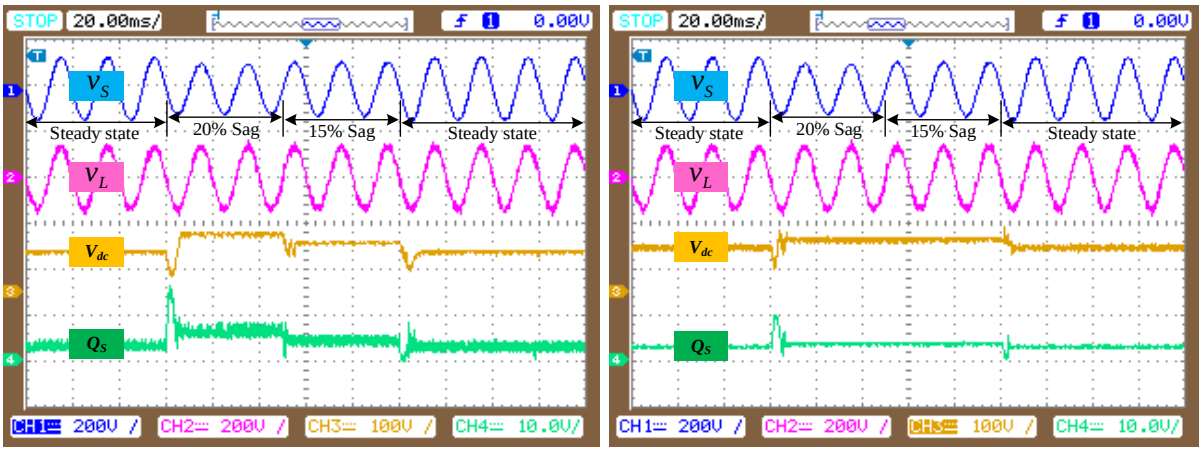
(a)



(b)

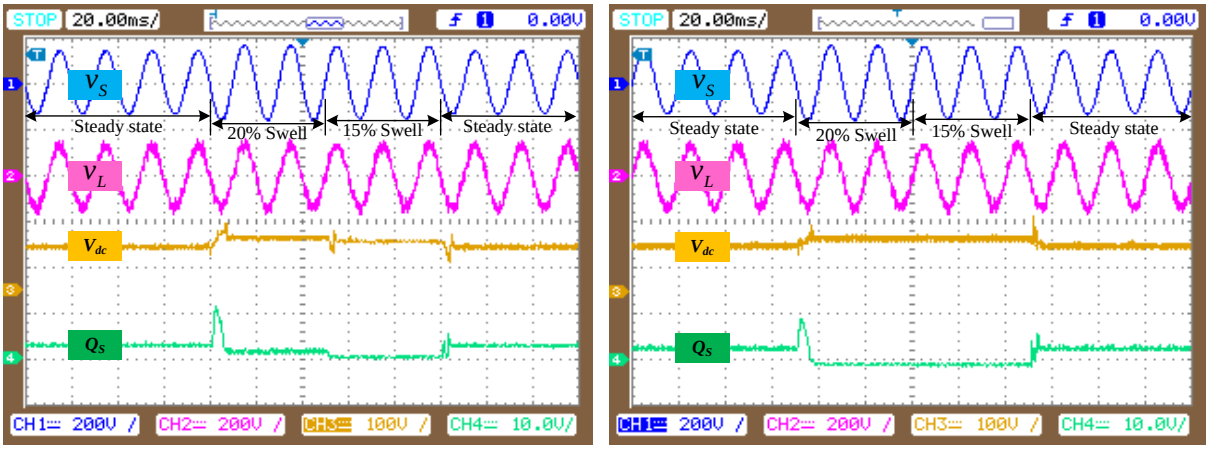
Fig. 4.27: Simulation results of minimum dc-link voltage requirement during variable voltage swell condition (a) with without application of PAC approach and (b) with proposed algorithm.

For implementation of the algorithm with PAC approach, dSPACE DS1006 real time interface (RTI) with DS2201 multi-I/O board is used. The PCB-mounted hall-effect based current transducers (TELCON HTP25) and voltage transducers (AD202JN) are used to scale down the actual current and voltage signals to process with the RTI control board. The firing commands generated by the dSPACE controller are collected from the multi-I/O board to interface with the IGBT based VSI modules. These firing commands are passed through a pulse isolation and amplification circuit to ensure the proper protection measurements and dead band circuits, for the prevention of short circuit in VSI legs through dc link capacitor. To conduct the experimental authentication regarding to voltage sag and swell, a three-phase auto transformer based sag generator setup has been used [245]. The voltage sag of 20% and 15% magnitude are generated with the help of sag generator setup to validate the performance of hybrid UPQC with and without proposed PAC approach. Figure 4.28(a) shows the source voltage and load voltage of phase-A along with dc-link voltage and reactive power supplied by the source to the load before application of PAC control approach ($\delta = 0^0$). It is observed that the hybrid UPQC requires the dc-link voltage of 88 V to compensate load reactive power of approximately 97.9%, if voltage sag in not present in the system. Whenever the sag exists, it demands increased value of dc-link voltage of 130V and 110V with source reactive power of 8VARs and 5.8VARs for voltage sag of 20% and 15% respectively. Whereas the proposed algorithm demands dc-link voltage of 106 V throughout the voltage sag period with effective compensation of voltage sag and reactive power demanded by the load, which is observed from Figure 4.28(b).



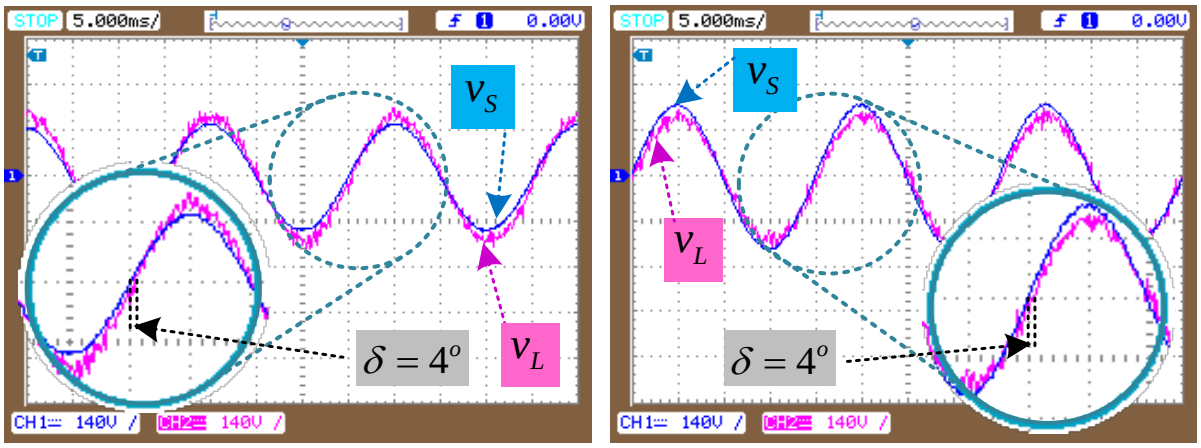
(a) (b)

Fig. 4.28: Experimental results of minimum dc-link voltage requirement during voltage sag condition. (a) without application of PAC approach and (b) with proposed algorithm.



(a) (b)

Fig. 4.29: Experimental results of minimum dc-link voltage requirement during voltage swell condition. (a) without application of PAC approach and (b) with proposed algorithm.



(a) (b)

Fig. 4.30: Phase angle displacement between source voltage and load voltage obtained with the application of proposed algorithm during (a) voltage sag condition and (b) voltage swell condition.

Similarly, the performance of hybrid UPQC is authenticated with the voltage swell of 20% and 15% alternately. During these swell period, the dc-link voltage of 108V and 100V is stipulated by the topology respectively as shown in Figure 4.29(a). With the application of proposed algorithm, it can be comprehended that constant value of 106 V is selected throughout the swell compensation period as shown in Figure 4.29(b). As discussed in simulation studies, the proposed algorithm imposes phase shift of 4^{o} between source and load voltages during voltage sag/swell compensation period within the range of $\pm 10\% < k \leq \pm 20\%$. It can be recognized from Figure 4.30.

4.8 Conclusion

An analytical study to achieve minimum possible dc-link voltage for hybrid UPQC with designed values of PPF is performed in this chapter. Though the required magnitude of dc-link voltage is less in comparison to traditional UPQC, further reduction is achieved by incorporating PAC approach along with optimal VA loading of hybrid UPQC. Additionally, a generalized algorithm is proposed to evaluate optimal dc-link voltage over a percentage range of voltage sag/swell combinations. Thus, the proposed algorithm gives the best fixed minimum dc-link voltage corresponding to within the range fixed by the algorithm based on the compensation level.

CHAPTER 5: TCZ-PPF BASED HYBRID UNIFIED POWER QUALITY CONDITIONER

This chapter extends the control of dc-link voltage to minimize further as compared to PPF based UPQC. The PPF provides the fixed reactance to compensate load reactive power. Adopting thyristor controlled reactor (TCR) to PPF, makes the reactance offered by PPF can be controlled over wide range. This concept is adopted for UPQC and named as thyristor controlled shunt reactance PPF (TCZ) based UPQC (TCZ-PPF-UPQC) to analyse the variation in dc-link voltage requirement. The dc-link voltage is also evaluated by applying PAC control approach. The performance is analysed through MATALB Simulink and also validated by the experimental laboratory setup.

5.1 Introduction

In the previous chapter, the hybrid UPQC is structured with PPF in series with the shunt converter. The limitation of PPF based hybrid UPQC is fixed compensation offered by the PPF. To achieve controllable compensation, the reactance offered by the PPF has to be varied. In the search of reducing rating of active power filter, hybrid active power filters are gaining more attention by the many researchers as discussed in the previous chapter. The further investigation is carried out on hybrid active power filters for different configurations to reduce the rating of the power filter and also to improve the performance of the hybrid power filter. In [20], a combination of a Thyristor controlled reactor (TCR) and a resonant impedance-type hybrid APF for harmonic cancellation, load balancing, and reactive power compensation has been proposed. A combined system of a static var compensator (SVC) and a small-rated APF for harmonic suppression and reactive power compensation has been reported in [221]. The SVC consists of a Y-connected passive power filter and a delta-connected TCR. The APF is used to eliminate harmonic currents and to avoid resonance between the passive power filters and the grid impedance. In [254], a new combination of a shunt hybrid power filter (SHPF) and a TCR (SHPF-TCR compensator) is proposed to suppress current harmonics and compensate the reactive power generated from the load. The hybrid filter consists of a series connection of a small-rated active filter and a fifth-tuned LC passive filter. The major part of the compensation is supported by the passive filter and the TCR while the APF is meant to improve the filtering characteristics and damps the resonance, which can occur between the passive filter, the TCR, and the source impedance. If the shunt APF used alone, it suffers from the high kilo volt-ampere rating of the inverter, which requires a lot of energy stored at high dc-link voltage. On the other hand, as published in [15], the standard hybrid power filter is unable to compensate the reactive power because of the behaviour of the passive filter. Hence, the proposed combination of SHPF and TCR compensates for unwanted reactive power and harmonic currents. In addition, it reduces significantly the volt-ampere rating of the APF part. In the literature, the hybrid shunt APF in terms of modified coupling inductance are named differently by the various researchers. Few of them have been called as capacitive coupling STATCOM (C-STATCOM) [245] or PPF-

STATCOM [254] by adding capacitor in series with the coupling inductance of the shunt converter. To achieve variable capacitance, instead of fixed value, a TCR is connected across the capacitor and named as TCR-STATCOM [251], Thyristor controlled LC (TCLC)-STATCOM [254].

5.1.1 Concept Background

The concept of TCR coupling to the shunt inductor part of APF is arrived from the FACTS (Flexible AC Transmission System) device TCSC (Thyristor Controlled Series Capacitor). TCSC is a capacitive reactance compensator which consists of a series capacitor bank shunted by a thyristor-controlled reactor in order to provide a smoothly variable series capacitive reactance. The structure of TCSC is shown in Figure 5.1. The controllable range of the TCR firing angle α, extends from 90^0 to 180^0. When the TCR firing angle is 180^0, the reactor becomes non-conducting and the series capacitor has its normal impedance. As the firing angle is advanced from 180^0 to less than 180^0, the capacitive impedance increases. At the other end, when the TCR firing angle is 90^0, the reactor becomes fully conducting, and the total impedance becomes inductive, because the reactor impedance is designed to be much lower than the series capacitor impedance. With 90^0 firing angle, the TCSC helps in limiting fault current in the transmission line.

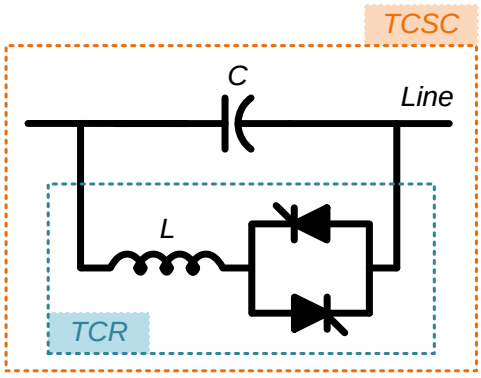


Fig. 5.1: Thyristor controlled series capacitor (TCSC) [5]

The basic idea behind the TCSC scheme is to provide a continuously variable capacitor by means of partially cancelling the effective compensating capacitance by the TCR by controlling the delay angle α. The steady-state impedance of the TCSC is that of a parallel LC circuit, consisting of a fixed capacitive impedance, X_c, and a variable inductive impedance, X_{TCR}, that is,

$$X_{TCSC}(\alpha) = \frac{X_C X_{TCR}(\alpha)}{X_{TCR}(\alpha) - X_C} \tag{5.1}$$

Where, X_{TCR}, is given by,

$$X_{TCR}(\alpha) = \frac{\pi X_L}{2\pi - 2\alpha + \sin 2\alpha} \tag{5.2}$$

The impedance characteristics of TCSC with respect to delay angle α are shown in the Figure 5.2.

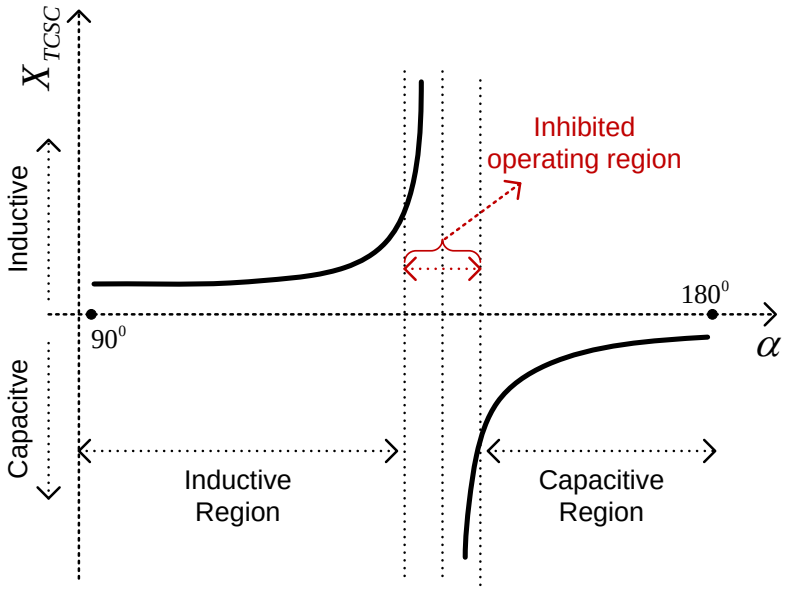


Fig. 5.2: Impedance characteristics of TCSC with respect to delay angle α [5]

From Figure 5.2, it can be observed that as firing angle varies from 90^0 to 180^0, the characteristics of impedance offered by TCSC changes from inductive to capacitive. In such a way the concept of TCSC can be utilised for shunt passive power filter in distribution system to offer variable compensating reactive power from inductive (lagging) to capacitive (leading) against loading reactive power.

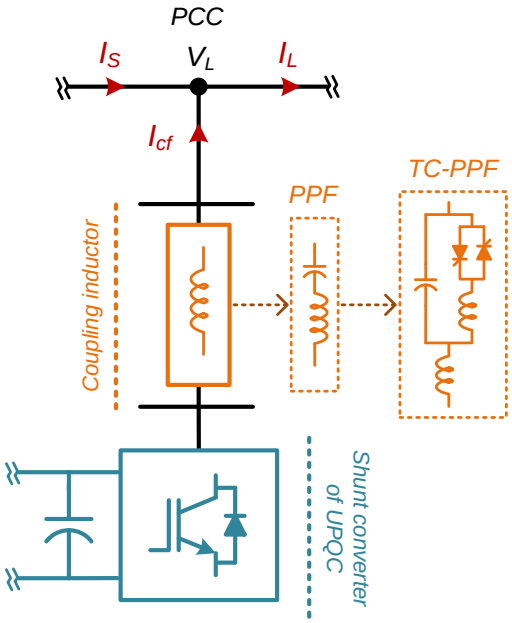


Fig. 5.3: Placement of thyristor controlled impedance (TCZ) in the UPQC application.

Figure 5.3 shows the shunt active power filter part of UPQC, where shunt converter is connected to the PCC through a coupling inductor (L_{sh}). In the previous chapter, an additional capacitor (C_{sh}) is connected in series with the coupling inductor (L_{sh}) in order to

reduce the VA rating and also the dc-link voltage requirement of APF such that the combination of C_{sh} and L_{sh} can be used as passive power filter (PPF). This PPF is used with the fixed reactive power compensation. To achieve variable reactive power compensation levels with wide range from lagging to leading, across capacitor (C_{sh}), a thyristor controlled reactor (TCR) is connected to utilise the concept of TCSC. This branch is named as thyristor controlled impedance (TCZ) in this thesis work. Such that the shunt compensating current (I_{cf}) can be injected into PCC to compensate loading reactive power, which may vary at different levels from lagging to leading along with non-linear current loads. The TCZ part provides a wide reactive power compensation range and a large voltage drop between the system voltage and the inverter voltage so that the active inverter part can continue to operate at a low dc-link voltage level. The small rating of the active inverter part is used to improve the performances of the TCZ part by absorbing the harmonic currents generated by the TCZ part, avoiding mistuning of the firing angles, and preventing the resonance problem.

5.2 Topology Description

Figure. 5.4, shows the structure of TCZ-PPF based hybrid UPQC, in which TCZ-PPF is composed with the shunt coupling inductor (L_{sh}) in series with the parallel connected of TCR controlled inductor (L_{PPF}) and capacitor (C_{PPF}). Z_s is the source line impedance, V_s and I_s are the source voltage and current respectively. V_L and I_L are the load voltage at PCC and load current respectively. The series injected voltage by the series converter is represented as V_{inj} and shunt compensating current by the shunt converter part along with TCZ-PPF as I_{cf}. V_{dc} is the common dc-link between two-level VSI based series and shunt converters.

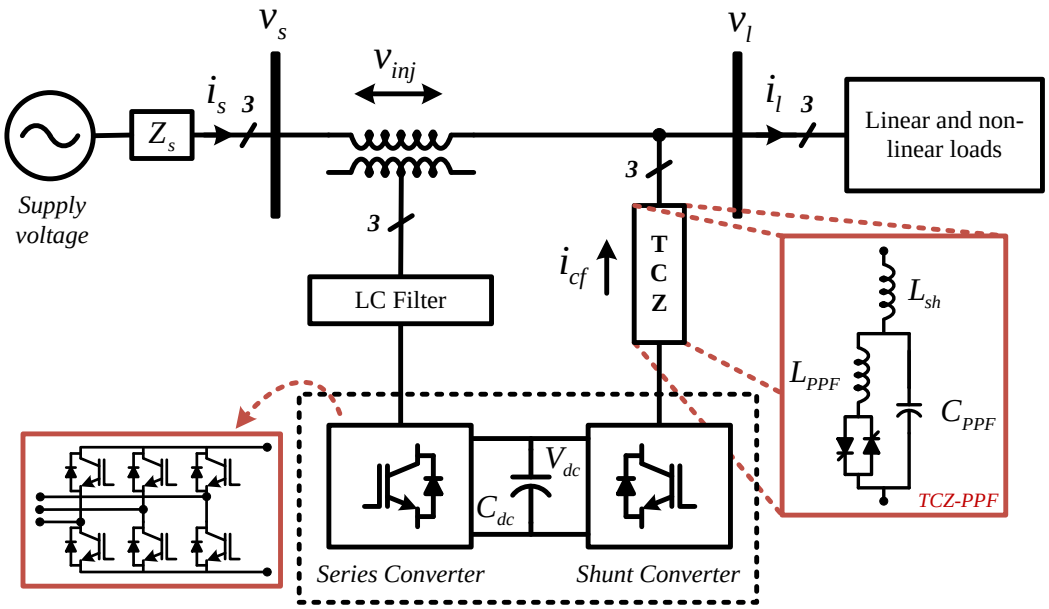


Fig. 5.4: Structure of TCZ-PPF based hybrid UPQC

The single-phase equivalent circuit of TC-PPF based hybrid UPQC at fundamental frequency is shown in Figure 5.5. V_L, V_{inj} and V_{sh} are the fundamental load, series injected

voltage and shunt VSI voltages (represented as phase voltages). I_s, I_{cf} and I_L are the fundamental source, shunt reactive compensating current and load currents. Z_s and V_s are the fundamental source line impedance and source terminal voltage respectively. X_{TCZ} is the fundamental reactance of the TCZ-PPF part.

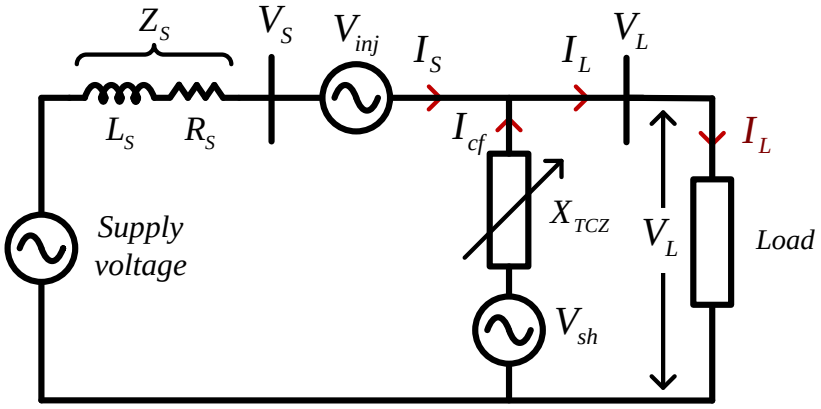


Fig. 5.5: Single-phase fundamental equivalent circuit of TCZ-PPF hybrid UPQC

From Figure 5.1 and 5.4, the phase fundamental reactance value of the TCZ part is,

$$X_{TCZ}(\alpha) = \frac{X_{C\_PPF} X_{TCR}(\alpha)}{X_{C\_PPF} - X_{TCR}(\alpha)} + X_{Lsh} \tag{5.3}$$

Where, $X_{TCZ}(\alpha)$ is given by,

$$X_{TCR}(\alpha) = \frac{\pi X_{L\_PPF}}{2\pi - 2\alpha + \sin 2\alpha} \tag{5.4}$$

On substituting (5.4) into (5.3),

$$X_{TCZ}(\alpha) = \frac{\pi X_{L\_PPF} X_{C\_PPF}}{X_{C\_PPF}(2\pi - 2\alpha + \sin 2\alpha) - \pi X_{L\_PPF}} + X_{Lsh} \tag{5.5}$$

Where, $X_{L\_PPF} = \omega L_{PPF}$, $X_{C\_PPF} = 1/\omega C_{PPF}$, $X_{Lsh} = \omega L_{sh}, \omega = 2\pi f$, f is the fundamental frequency. α is the firing angle of the thyristor switches of the TCR part.

The impedance of TCR is controlled by the firing angle α, there by the impedance of TCZ part. As the firing angle varies from 90^0 to 180^0, the minimum inductive impedance occurs at $\alpha = 90^0$, because of the full conduction of thyristor switches. At $\alpha = 180^0$, TCZ part provides the minimum capacitance, because of non-conductive thyristor switches. The minimum inductive ($X_{TCZ(\min\_ind)} > 0$) and capacitive ($X_{TCZ(\min\_cap)} < 0$) impedances are derived as absolute values and expressed as,

$$X_{TCZ(\text{Min\_Ind})} = \frac{X_{L\_PPF} X_{C\_PPF}}{X_{C\_PPF} - X_{L\_PPF}} + X_{Lsh}; \quad \alpha = 90^0 \tag{5.6}$$

$$X_{TCZ(\text{Min\_Cap})} = -X_{C\_PPF} + X_{Lsh}; \quad \alpha = 180^0 \tag{5.7}$$

The relation between shunt VSI output voltage (V_{sh}) and the voltage at PCC (V_L) can be expressed in terms of impedance of TCZ-PPF is given as,

$$V_{sh} = V_L - X_{TCX\_PPF}(\alpha) I_{cf} \tag{5.8}$$

Where, I_{cf} is the fundamental rms value of the reactive compensating current injected by the shunt converter. This compensating current can be maintained equal to in opposition to the reactive power drawn by the load at PCC. The load current active and reactive components are given as follows,

$$\overline{I}_L = \overline{I}_{Lp} + j\overline{I}_{Lq} \tag{5.9}$$

Where, I_{Lp} and I_{Lq} are the active and reactive current components of the load current respectively. The shunt compensating current can be expressed in terms of load current is as

$$I_{Lq} = -I_{cf} \tag{5.10}$$

Equation (5.8) can be rewritten as,

$$V_{sh} = V_L + X_{TCX\_PPF}(\alpha) I_{Lq} \tag{5.11}$$

Ideally, $X_{TCZ}(\alpha)$ is controlled to be $V_L \approx X_{TCZ}(\alpha) * I_{Lq}$, so that the minimum inverter voltage ($V_{sh} \approx 0$) can be obtained as shown in (5.11). In this case, the switching loss and switching noise can be significantly reduced. A small inverter voltage $V_{sh(\min)}$ is necessary to absorb the harmonic current generated by the TCZ part, to prevent a resonance problem, and to avoid mistuning the firing angles. If the loading capacitive current or inductive current is outside the TCZ part compensating range, the inverter voltage V_{sh} will be slightly increased to further enlarge the compensation range.

As seen in the previous chapter, the coupling impedance part of the shunt converter has been considered as the inductor (X_{Lsh}) for conventional UPQC, whereas PPF (X_{PPF}) for hybrid UPQC as shown in Figure 5.3. In this case, the relationship between the load voltage V_L, the shunt VSI output voltage V_{sh}, the reactive component of load current I_{Lq}, and the coupling impedances can be expressed as

$$V_{sh} = V_L + X_{Lsh} I_{Lq} \text{; Conventional UPQC} \tag{5.12}$$

$$V_{sh} = V_L + X_{PPF} I_{Lq} \text{; PPF-Hybrid UPQC} \tag{5.13}$$

Where,

$$X_{Lsh} = \omega L_{sh}$$
$$X_{PPF} = -\left| \frac{1}{\omega C_{PPF}} - \omega L_{PPF} \right| \tag{5.14}$$

Where, ω is the fundamental angular frequency.

For traditional UPQC as shown in Figure 5.6, the required voltage at the output of shunt converter VSI, V_{sh} is larger than the load voltage at PCC, V_L when the loading is inductive. In contrast, the required V_{sh} is smaller than V_L when the loading is capacitive. Actually, the required inverter voltage, V_{sh} is close to the voltage at PCC, V_L, due to the small value of coupling inductor L_{sh} [5].

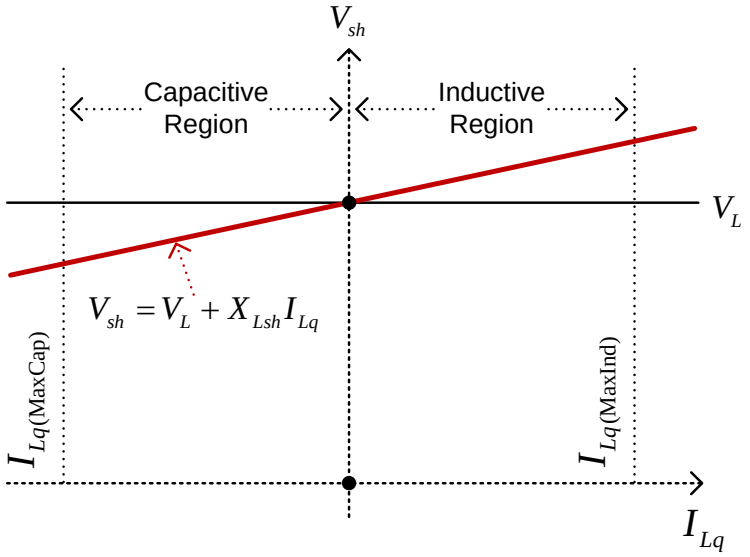


Fig. 5.6: Shunt converter VSI output voltage vs reactive loading current of conventional UPQC.

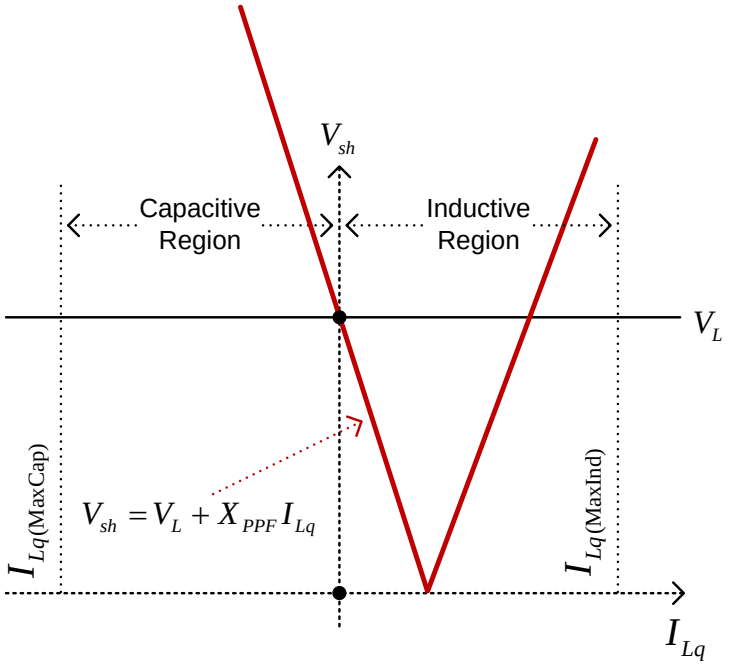


Fig. 5.7: Shunt converter VSI output voltage vs reactive loading current of PPF- hybrid UPQC.

For PPF-Hybrid UPQC as shown in Figure 5.7, it is shown that the required V_{sh} is lower than V_L under a small inductive loading range. The required V_{sh} can be as low as zero when the coupling capacitor can fully compensate for the loading reactive current. In contrast, V_{sh}

is larger than V_L when the loading is capacitive or outside its small inductive loading range. Therefore, when the loading reactive current is outside its designed inductive range, the required V_{sh} can be very large.

For the TCZ-PPF hybrid UPQC as shown in Figure 5.8, the required V_{sh} can be maintained at a low (minimum) level $V_{sh(min)}$ for a large inductive and capacitive reactive current range. Moreover, when the loading reactive current is outside the compensation range of the TCZ part, the V_{sh} will be slightly increased to further enlarge the compensating range. Compared with traditional UPQC and PPF-UPQC, the TCZ-PPF hybrid UPQC has a superior V–I characteristic of a large compensation range with a low shunt converter VSI voltage.

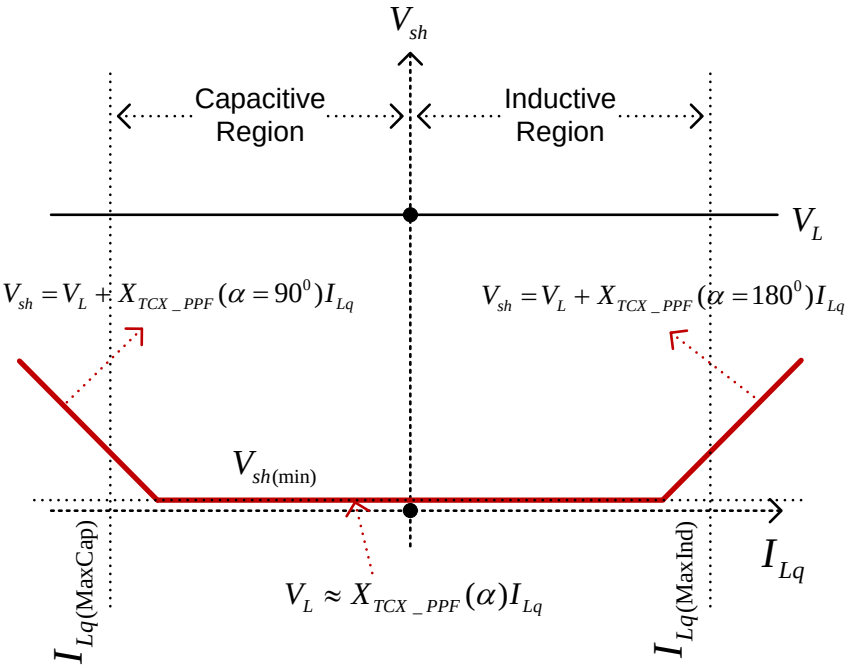


Fig. 5.8: Shunt converter VSI output voltage vs reactive loading current of TCZ-PPF hybrid UPQC.

5.3 Parameter Design of TCZ-PPF Hybrid UPQC

The design part of hybrid UPQC mainly involves on the procedure of choosing parameter values of TCZ-PPF part. The purpose of the TCZ-PPF part is to provide the same amount of compensating reactive power as the reactive power required by the loads but with the opposite direction. Therefore, C_{PPF} and L_{PPF} of the TCZ-PPF part are designed on the basis of the maximum capacitive and inductive reactive power. As already discussed in the previous chapter, the compensating reactive power $Q_{TCZ-PPF}$ range in terms of impedance of TCZ branch can be expressed as

$$Q_{TCZ-PPF}(\alpha) = \frac{V_L^2}{X_{\text{TCZ}-PPF}(\alpha)} \tag{5.15}$$

where V_L is the phase rms value of the load voltage and $X_{TCZ}(\alpha)$ is the impedance of the TCZ part with respect to TCR firing angle α, which can be obtained from (5.5). In (5.15), when the $X_{TCZ\text{-}PPF}(\alpha) = X_{TCZ\text{-}PPF(Min\_Cap)}(\alpha = 180^0)$ and $X_{TCZ\text{-}PPF}(\alpha) = X_{TCZ\text{-}PPF(Min\_Ind)}(\alpha = 90^0)$, the TCZ part provides the maximum capacitive and inductive compensating reactive power $Q_{TCZ-PPF(\max\_cap)}$ and $Q_{TCZ-PPF(\max\_ind)}$, respectively,

$$\begin{aligned} Q_{TCZ-PPF(Max\_Cap)} &= \frac{V_L^2}{X_{\text{TCZ}-PPF}(\alpha = 180^0)} \\ &= \frac{V_L^2}{X_{C\_PPF} - X_{Lsh}} \end{aligned} \tag{5.16}$$

$$\begin{aligned} Q_{TCZ-PPF(Max\_Ind)} &= \frac{V_L^2}{X_{\text{TCZ}-PPF}(\alpha = 90^0)} \\ &= \frac{V_L^2}{\frac{X_{L\_PPF}X_{C\_PPF}}{X_{C\_PPF} - X_{L\_PPF}} + X_{Lsh}} \end{aligned} \tag{5.17}$$

where the minimum inductive impendence ($X_{TCZ-PPF}(\alpha = 90^0)$) and the capacitive impendence ($X_{TCZ-PPF}(\alpha = 180^0)$) are obtained from (5.6) and (5.7), respectively. To compensate for the load reactive power ($Q_{TCZ-PPF} = -Q_L$), C_{PPF} and L_{PPF} can be deduced on the basis of loading maximum inductive reactive power $Q_{L(\max\_ind)}$ $(= -Q_{TCZ-PPF(\max\_cap)})$ and capacitive reactive power $Q_{L(\max\_cap)}$ $(= Q_{TCZ-PPF(\max\_ind)})$ Therefore, based on (5.16) and (5.17), the parallel capacitor C_{PPF} and inductor L_{PPF} can be designed as

$$C_{PPF} = \frac{Q_{L(MaxInd)}}{\omega^2 Q_{L(MaxInd)} L_{sh} + \omega V_L^2} \tag{5.18}$$

$$L_{PPF} = \frac{V_L^2 + \omega L_{sh} Q_{L(MaxCap)}}{-\omega Q_{L(MaxCap)} + \omega^3 L_{sh} C_{PPF} Q_{L(MaxCap)} L_{sh} + \omega^2 V_L^2 C_{PPF}} \tag{5.19}$$

The design of additional inductor L_{sh} involves the consideration of resonance problems. For exciting resonance problems, a sufficient level of harmonic source voltages or currents must be present at or near the resonant frequency. Therefore, L_{sh} can be designed to tune the resonance points to diverge from the dominated harmonics 5th, 7th, 11th, 13th of a three-phase three-wire transmission system to avoid the resonance problem. The TCR part of the TCZ can generate harmonics as switching of the thyristor switches. When TCR is bypassed ($\alpha = 180^0$), TCZ-PPF can be considered as L_{sh} in series with C_{PPF}. In this case, the impedance of nth harmonic is given as,

$$X_{TCZ,n(\alpha=180^0)} = X_{C\_PPF,n} - X_{Lsh,n} \tag{5.20}$$

$$X_{TCZ,n(\alpha=180^0)} = \left| \frac{1-(n\omega)^2 L_{sh} C_{PPF}}{n\omega C_{PPF}} \right| \tag{5.21}$$

The L_{sh} can be calculated from (5.20) as, by considering resonant point n_1 at $X_{TCZn}(n_1) = 0$.

$$L_{sh} = \frac{1}{(n_1\omega)^2 C_{PPF}} \tag{5.22}$$

Similarly, when TCR is fully conducting ($\alpha = 90^0$), TCZ-PPF can be considered as the L_{sh} is in series with the parallel combination of L_{PPF} and C_{PPF}. The nth harmonic impedance at this condition is given as,

$$\begin{aligned} X_{TCZ,n(\alpha=180^0)} &= \frac{X_{L\_PPF,n} X_{C\_PPF,n}}{X_{C\_PPF,n} - X_{L\_PPF,n}} + X_{Lsh,n} \\ &= \left| \frac{n\omega(L_{sh} + L_{PPF}) - (n\omega)^3 L_{sh} L_{PPF} C_{PPF}}{1-(n\omega)^2 L_{PPF} C_{PPF}} \right| \end{aligned} \tag{5.23}$$

The L_{sh} can be calculated at this condition from (5.22) as, by considering resonant point n_2 at $X_{TCZn}(n_2) = 0$.

$$L_{sh} = \frac{1}{(n_2\omega)^2 C_{PPF} - 1/L_{PPF}} \tag{5.24}$$

5.4 DC-Link Voltage Requirement of TCZ-PPF Hybrid UPQC

Based on the analysis studied for the PPF based hybrid UPQC, which is discussed in detail in Chapter. 4, the minimum dc-link voltage (V_{dc}) required across the dc-link capacitor between shunt and series converters of TCZ-PPF Hybrid UPQC is evaluated from (4.13), in which the impedance of PPF (X_{PPF}) is replaced with the impedance offered by the TCZ-PPF ($X_{TCZ-PPF}$).

$$V_{dc} = 2\sqrt{2}\left\{ \sqrt{(V_L + I_{cfq}.X_{TCZ-PPF}(\alpha))^2 + (I_{cfp}.X_{TCZ-PPF}(\alpha))^2} \right\} \tag{5.25}$$

Where, I_{cfp} is the active component of total compensating current (I_{cf}) injected by the shunt converter along with TCZ-PPF. This component is responsible for converter losses, dc-link balancing and sag/swell compensation in support of series converter and I_{cfq} is the reactive component of I_{cf}, which is equal to the total load reactive current component (I_{Lq}); V_L is the phase rms voltage at PCC. The component

The shunt compensating current (I_{cf}) is $X_{TCZ-PPF}$ is not constant as in the case of PPF, which is discussed in the previous chapter. The impedance ($X_{TCZ-PPF}$) depends impedance ($X_{TCZ-PPF}(\alpha)$) offered by the TCR part as given in (5.4) such that it varies between minimum inductive and minimum capacitive values as given in (5.6) and (5.7) respectively.

The evaluation of dc-link voltage from (5.25) is considered without including phase angle control (PAC). In this chapter, the PAC is also implemented to reduce the VA rating of the hybrid UPQC as similar to previous chapter. The required dc-link voltage is evaluated with PAC is given in (5.26).

$$V_{dc} = 2\sqrt{2}\left\{\sqrt{(V_L + I'_{cfq}.X_{TCZ-PPF}(\alpha))^2 + (I'_{cfp}.X_{TCZ-PPF}(\alpha))^2}\right\} \quad (5.26)$$

Where, I'_{cfp} and I'_{cfq} are the active and reactive components of compensating current I'_{cf} respectively on the application of PAC. The component I'_{cf} is given in (4.25), where, the magnitude of I'_{cf} depends on the phase shift angle (δ).

5.4.1 Analysis of Minimum DC-Link Voltage Requirement

In this chapter, the minimum requirement of dc-link voltage of TCZ-PPF based hybrid UPQC is evaluated for different loading reactive powers ranging from leading to lagging, which includes under compensation and over compensation regions by the TCZ-PPF. The evaluation also includes the effect of voltage sag/swell on dc-link voltage requirement. The following system parameters are considered for the dc-link voltage evaluation. The analysis is carried out with three-phase star connected linear load such that the value evaluated with (5.25) and (5.26) gives the fundamental value related to voltage/current signals. This chapter doesn't include the dc-voltage requirement for the nonlinear current harmonic elimination or harmonic voltage compensation. The possibility of extending this work is discussed in the future scope.

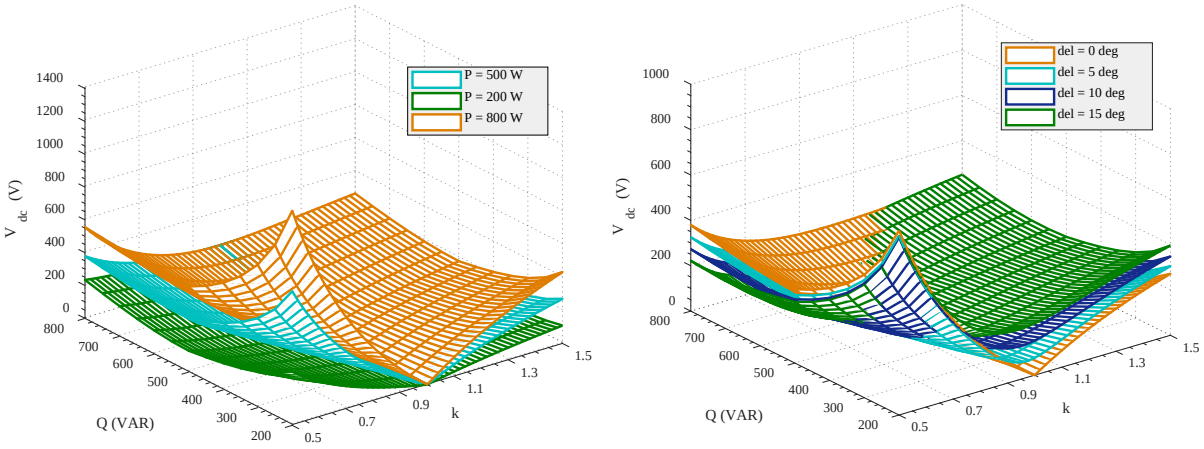
The parameters of TCZ-PPF are evaluated with loading reactive power of 500VAR i.e. the range of reactive power support by the TCAZ-PPF is from +500VAR (lagging) to -500 VAR (leading). The line-line load voltage is considered 200 V and frequency 50Hz. The segments of TCZ-PPF are designed as illustrated in (5.18) and (5.19) for rated reactive power of 500VAR and the value of coupling inductor is evaluated by considering the resonance case as described in (5.22) and (5.24). The parameters of per phase branch of TCZ-PPF are shown in Table 5.1.

Table 5.1: Design parameters of TCZ-PPF.

Description	Symbol	Parameter value
Capacitance	C_{PPF}	117.5 μF
Inductance	L_{PPF}	42.24 mH
Coupling inductance	L_{sh}	0.0025 H

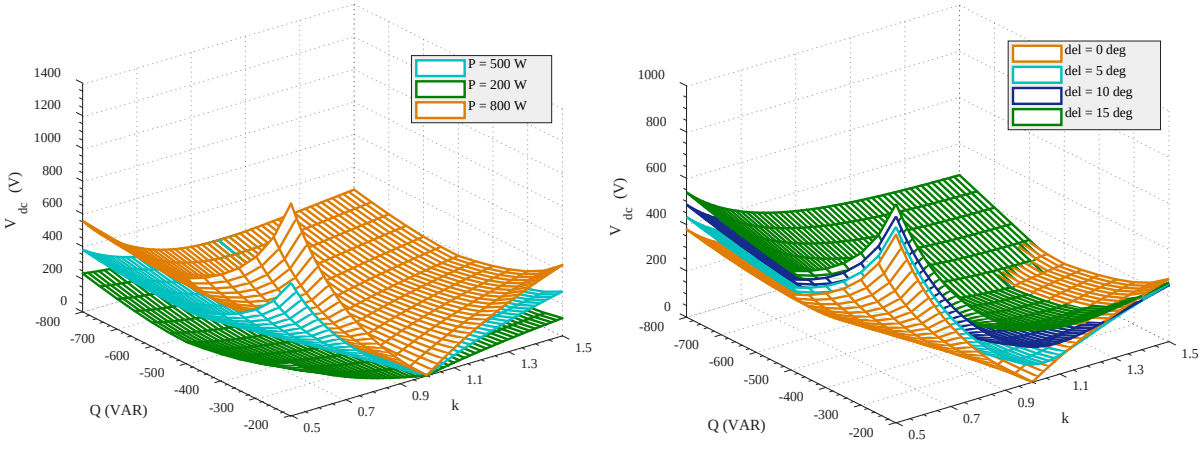
The dc-link voltage is evaluated with respect to lagging power factor load and sag/swell index (k) is shown in Figure 5.9. The power factor is varied from 200VAR to 800VAR and k

is varied from 0.5 to 1.5 i.e. up to 50% voltage sag and 50% voltage swell from the nominal load voltage. Figure 5.9(a) shows the variation of dc-link voltage for different active power levels i.e. 200W, 500W and 800W. It can be observed that the requirement of dc-link voltage is more as the power factor decreases. Figure 5.9(b) shows the dc-link voltage variation with different phase angle (δ) introduced by PAC with P=500W. The plot corresponding to $\delta = 0^0$ refers to the dc-link voltage variation without PAC and is similar to the curve plotted in Figure 5.9(a) with P=500W. From Figure 5.9(b), it can be observed that the minimum dc-link voltage occurs at $\delta = 0^0$ for $k = 1$. As sag/swell index deviates from $k = 1$ then changing phase angle shift provides the lower dc-link voltages. Figure 5.10 shows the variation of dc-link voltage with leading power factor load. Though there are no changes in dc-link voltage at $\delta = 0^0$, increase in δ shows the significant changes in the dc-link value. This can be observed form the Figure 5.10(b).



(a) (b)

Fig. 5.9: Variation of dc-link voltage with lagging power factor of load with respect to sag/swell index (k) and load reactive power (Q) (a). with different load active power levels (P) (b). with different power angles (δ).



(a) (b)

Fig. 5.10: Variation of dc-link voltage with leading power factor of load with respect to sag/swell index (k) and load reactive power (Q) (a). at different load active power (P) levels (b). with different power angles (δ).

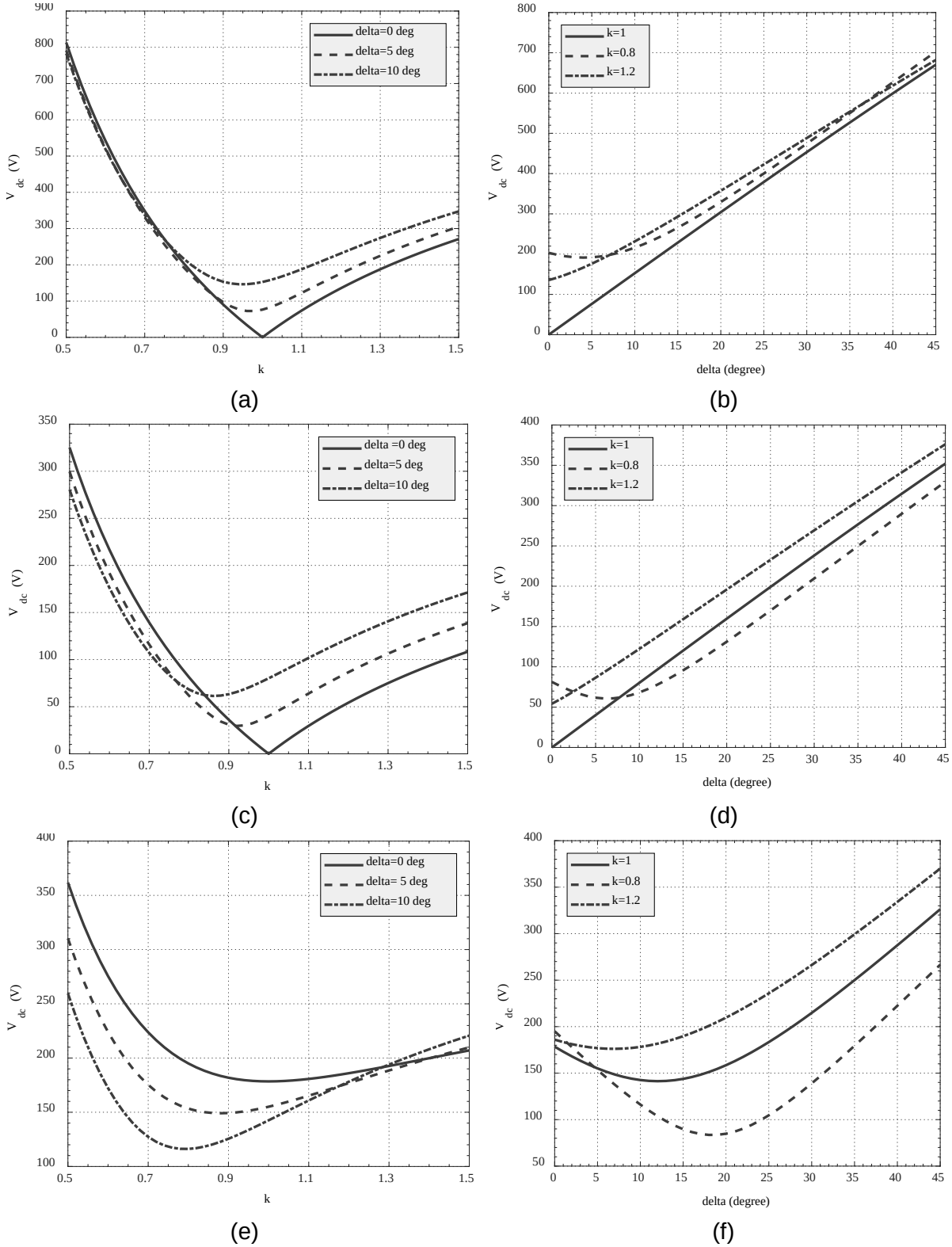


Fig. 5.11: Variation of dc-link voltage with lagging power factor of load with respect to sag/swell index (k) and power angle (δ) for (a), (b) $P = 500W, Q = 200VAR$,(c), (d) $P = 500W, Q = 500VAR$, (e), (f) $P = 500W, Q = 800VAR$.

For better understanding of the dependency of dc-link voltage on k and δ Figure 5.11 is plotted. Figure 5.11 shows the variation of dc-link voltage with respect to k with three different cases of δ and dc-link variation with respect δ to for three different cases of k.

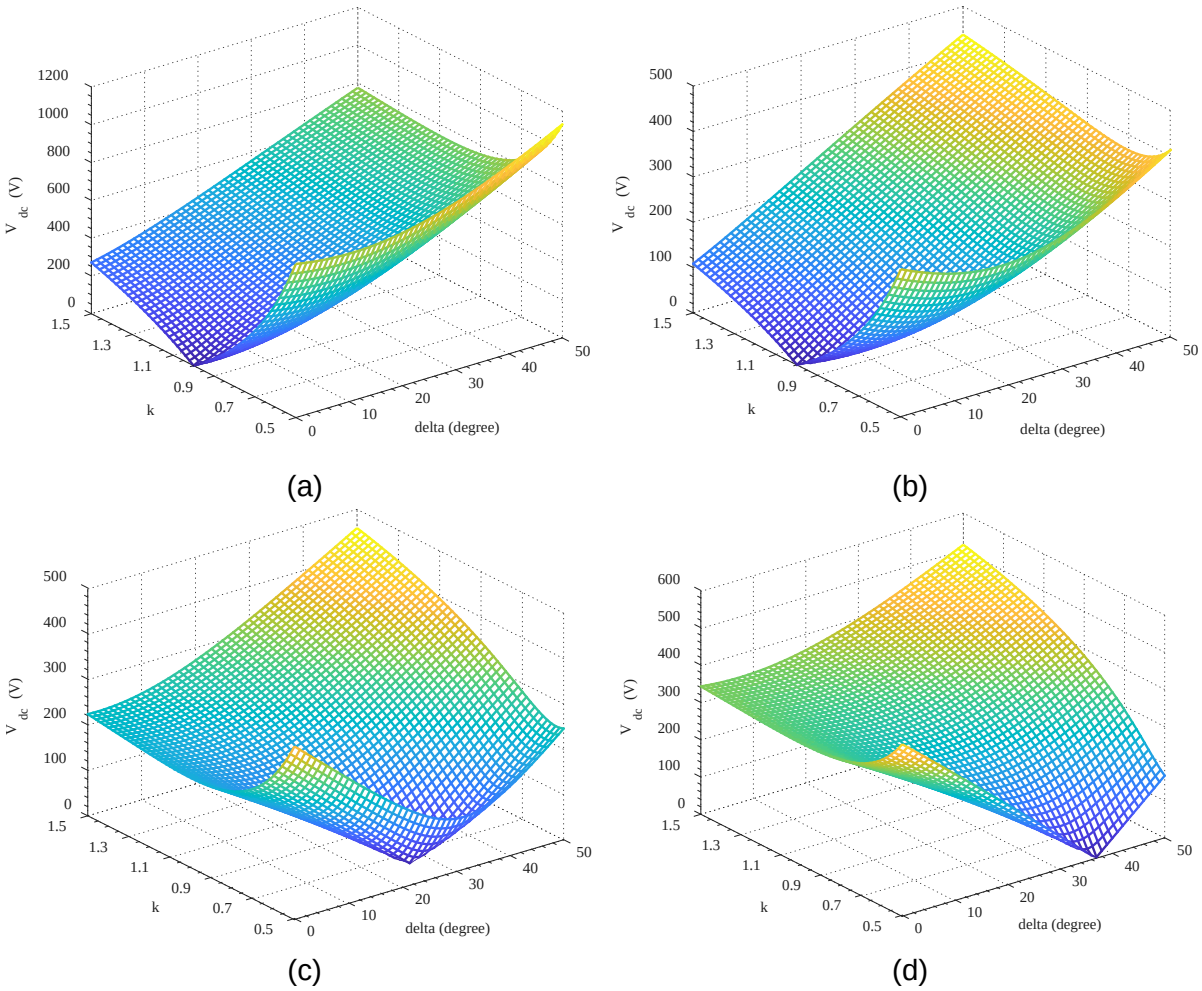


Fig. 5.12: Variation of dc-link voltage with lagging power factor of load with respect to sag/swell index (k) and power angle (δ) for (a), $P = 500W, Q = 200VAR$, (b) $P = 500W, Q = 500VAR$, (c) $P = 500W, Q = 800VAR$, (d) $P = 500W, Q = 1000VAR$.

The two-dimensional plots shown in Figure 5.11 are represented in three-dimensionally in Figure 5.12 for lagging power factor loads, where the dc-link is plotted with respect to k and δ. The value of k is varied from 0.5 to 0.9 in steps of 0.02 and δ is varied from 0^0 to 45^0 in step size of one.

5.4.2 Algorithm to Evaluate Optimal DC-Link Voltage

The best minimum dc-link voltage of hybrid UPQC is evaluated by considering certain constraints such as design parameters of PPF, optimal VA loading of UPQC and reference dc-link voltage (V_{dcref}). Figure 5.13 represents the flow chart of proposed algorithm to estimate optimal dc-link voltage of hybrid UPQC. The overall VA loading of UPQC (S_{H-UPQC}) and dc-link voltage (V_{dc}) are computed and stored in an array using PAC approach with the system parameters for a given load power factor and voltage sag/swell value (k) using (4.32) and (5.26) respectively. Equation (4.32) is evaluated for TCZ-PPF hybrid UPQC by replacing Q_{PPF} with $Q_{TCZ-PPF}$. The power angle δ is varied in a step size of 0.05^0 to a maximum value of 45^0.

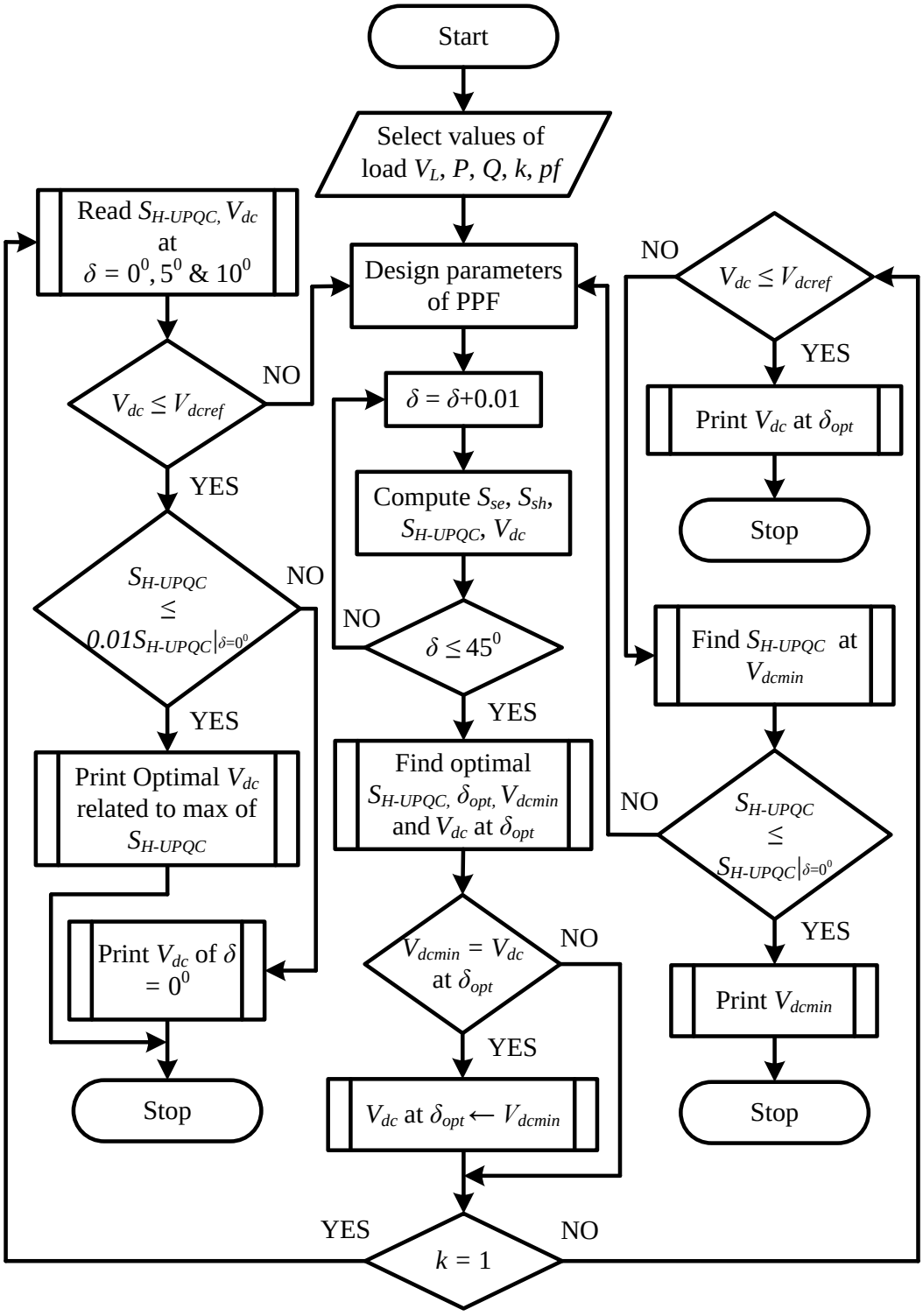


Fig. 5.13: Flow chart to evaluate optimal dc-link voltage of TCZ-PPF based hybrid UPQC.

Beyond 45^0, the VA loading surpasses the requirement as there is a sharp increment in the active and reactive power requirement for compensation to be supplied by the series converter. The data related to optimal VA loading, δ_{opt}, minimum dc-link voltage (V_{dcmin}) and dc-link voltage corresponds to δ_{opt} are selected from the array where these data are stored. If no sag or swell is present in terminal voltage ($k = 1$), calculation of optimal VA loading is possible only at $\delta = 0^0$. Beyond this angle, there is escalation in the VA loading. If $k = 1$ is

satisfied, value of S_{H-UPQC} and corresponding $\delta = 0^0$ is considered for $\delta = 0^0,\ 5^0$ & 10^0. The selected values of V_{dc} are ensured to be within the reference range from 0 to V_{dcref}. The optimal value of dc-link voltage selected corresponds to S_{H-UPQC} with negligible percentage increment in VA loading (≤1%) as compared to value at $\delta = 0^0$. Contrary to $k = 1$, to select the best possible optimal dc-link voltage, either the value corresponds to δ_{opt} or the minimum dc-link voltage (V_{dcmin}) is chosen. The selected optimal value of dc-link voltage should be within the reference value (V_{dcref}) and corresponding VA loading should be below the value corresponding to $\delta = 0^0$. If the condition is false, the design parameter of TCZ-PPF has to be altered and the process should be repeated for the possible optimal dc-link voltage.

5.5 Controller for Hybrid-UPQC

This section describes the reference signal generation for series and shunt converters of hybrid UPQC along with control of impedance of TCZ-PPF.

5.5.1 Generation of Reference Signals for Series and Shunt Converter

Similar to the approach as discussed in chapter 4 in section 4.5, the proposed algorithm uses the PAC control approach, which generates the required phase angle shift (δ) and optimal dc-link voltage. The generation of reference signals for series converter based on the pre-defined phase shift angle δ, whereas the shunt converter utilises the single-phase p-q theory as discussed in the sections 4.5.1 and 4.5.2.

5.5.2 Generation Firing Commands for TCR of TCZ-PPF

The impedance offered by TCZ-PPF is controlled by the TCR based on the loading reactive power demand. Figure 5.14 shows the control block diagram of firing pulses generation to the TCZ part. , the fundamental average load reactive power ($\bar{q}_{Lx}$) is calculated by the single-phase instantaneous *p-q* theory [18], [25], which is used to calculate $X_{TCZ-PPF}$ using (5.15) so as to control the firing angle (α) of the thyristor switch ($S_{1x}$and S_{2x}). When $X_{TCZ-PPF}$ varies within the compensation range of the TCZ part, which means $X_{TCZ-PPF(\max\_cap)}$ ($\alpha = 180^0$) < $X_{TCZ-PPF}$< $X_{TCZ-PPF(\max\_ind)}$ ($\alpha = 90^0$), the corresponding α can be obtained from (5.18) with $X_{TCZ-PPF}(\alpha)$ = $-X_{TCZ-PPF}$. Otherwise, if $\bar{q}_{Lx}$ is outside the TCZ part compensation range, which means $X_{TCZ-PPF(\max\_cap)}$ ($\alpha = 180^0$) >$-X_{TCZ-PPF}$ or $X_{TCZ-PPF(\max\_ind)}$ ($\alpha = 90^0$) < $-X_{TCZ-PPF}$, α would be set to be equal to 180° or 90°, respectively. However, (5.18) has a term of $-2\alpha + \sin(2\alpha)$, which does not have a closed-form solution. Therefore, an lookup table (LUT) ($X_{TCZ-PPF}$ vs α) is built, so that α can be found according to the calculated $X_{TCZ-PPF}$ from $\bar{q}_{Lx}$ easily. Finally, the thyristor switches are triggered by comparing α_x to the phase angle of the load voltage (θ), that is obtained from a phase lock loop (PLL). The TCZ part can compensate the reactive and unbalanced powers.

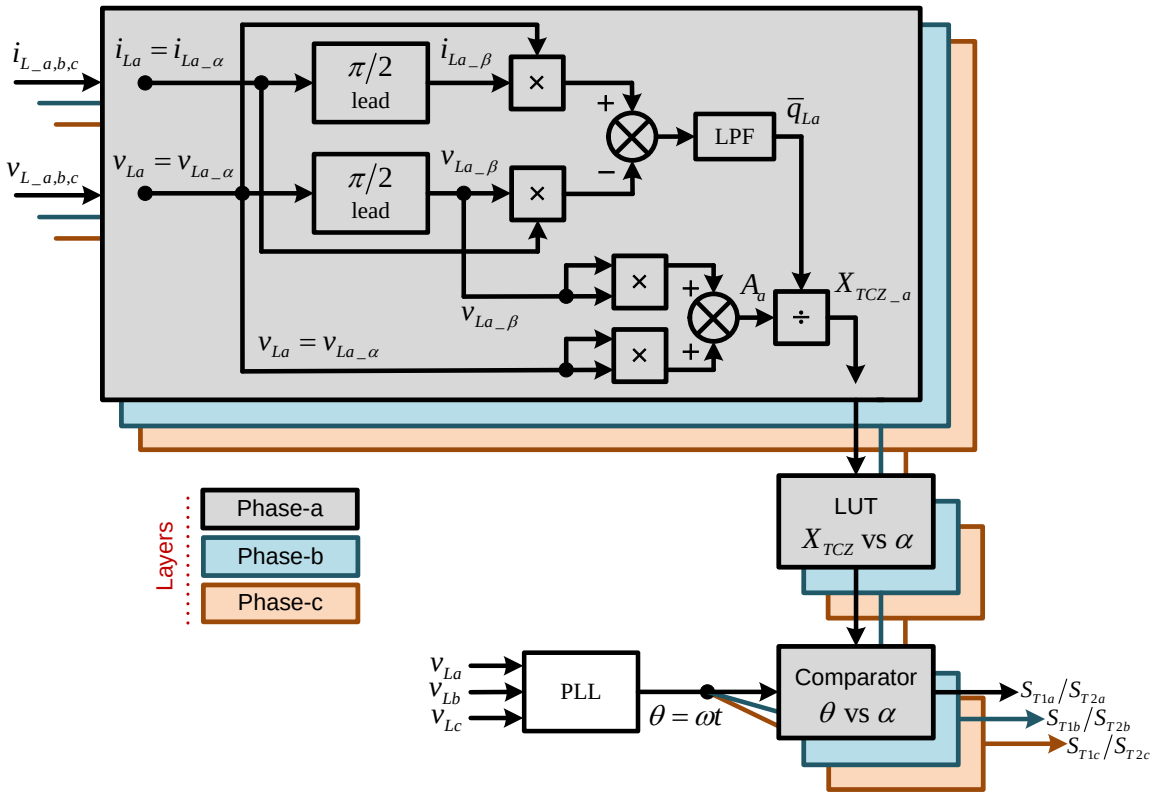


Fig. 5.14: Generation of firing pulses for TCR part of TCZ-PPF hybrid UPQC.

5.6 Simulation Study

The analysis of minimum dc-link voltage requirement of TCZ-PPF based hybrid UPQC is simulated in MATLAB Simulink platform for two cases of k: no voltage sag/swell, 20% sag and two cases of loading reactive power: Q=200, 800VAR.

Figure 5.15 shows the simulated results for load parameters of 500W+200VAR, which comes under compensating range provided by the TCZ-PPF. Ideally, the requirement of dc-link voltage should be zero for this case as discussed in the above sections. The load voltage, source reactive power loading and required minimum dc-link voltage for voltage sag of 20% on source voltage are shown in Figure 5.15. The reactive power required by the load is completely supplied by the source until UPQC is connected to the system at t =1.5s. When UPQC is triggered, the minimum dc-link voltage is settled at 4V. This is because of the active power component drawn by the shunt converter to supply converter losses. The source supplies only 1.2VARs to the load. Remnant reactive power is supplied by the hybrid UPQC. To compensate the voltage sag, which is applied at t =2s, the hybrid UPQC demands 221V and source supplies the average reactive power of 1.8VARs in this condition. Whereas the reduced dc-link voltage of 193V is sufficient to compensate the voltage sag with 1.5VARs of source reactive power with the proposed algorithm, which is shown in Figure 5.16. Figure 5.17 shows the the simulated results for load parameters of 500W+800VAR, which comes under outside compensating range provided by the TCZ-PPF. In this case, the dc-link voltage is not zero as the above case.

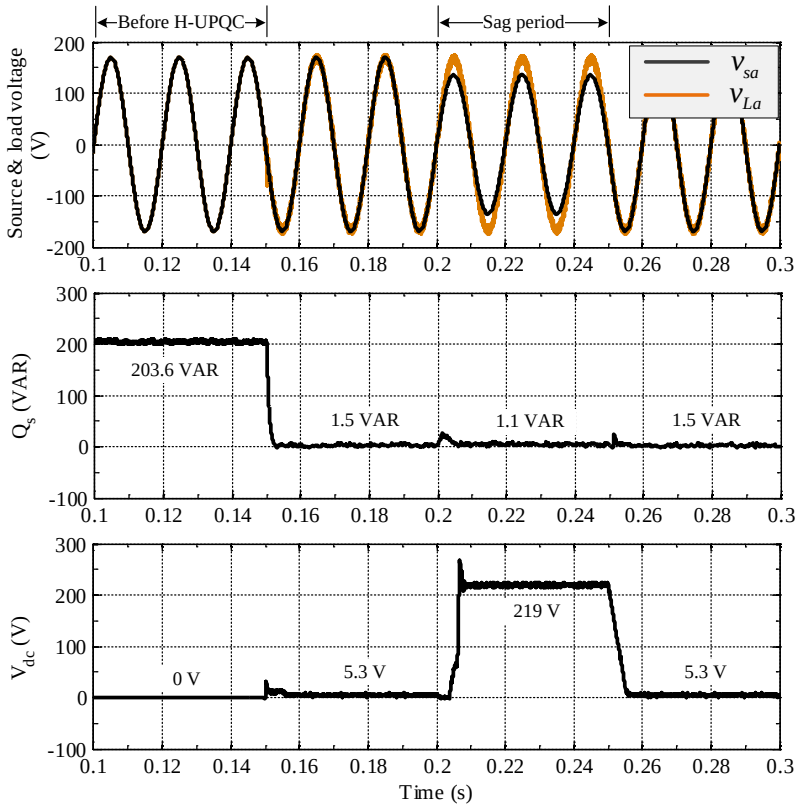


Fig. 5.15: Minimum dc-link voltage requirement during sag condition with 200VAR.

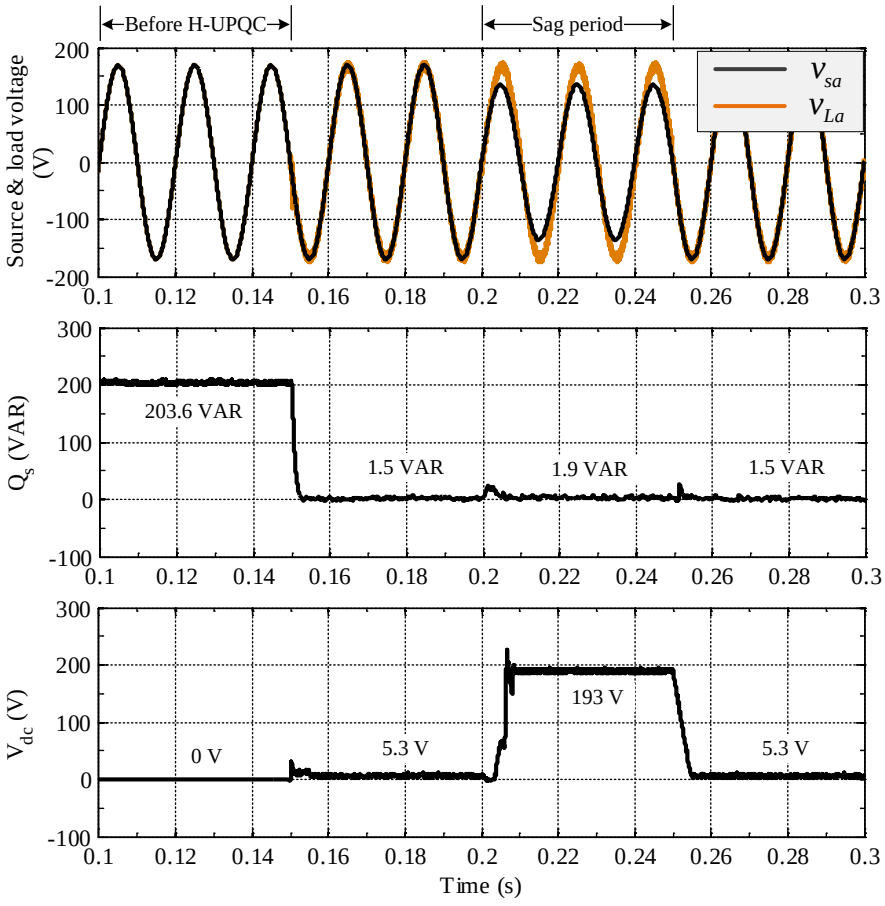


Fig. 5.16: Minimum dc-link voltage requirement during sag condition with 200VAR with PAC control algorithm.

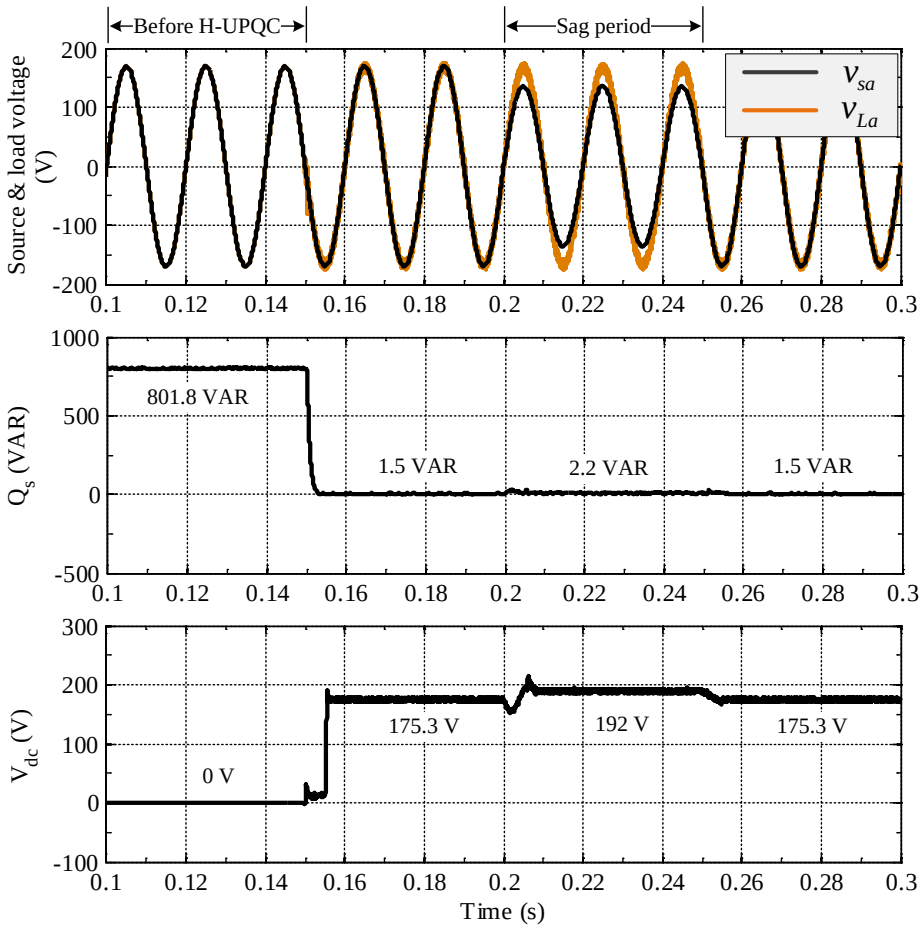


Fig. 5.17: Minimum dc-link voltage requirement during sag condition with 800VAR.

From Figure 5.17, When UPQC is triggered, the minimum dc-link voltage is settled at 175V. This is because of the loading reactive power demand is greater than the reactive power provided by the TCZ-PPF. The source supplies only 2.1VARs to the load. Remnant reactive power is supplied by the hybrid UPQC. To compensate the voltage sag, which is applied at t =2s, the hybrid UPQC demands 192V and source supplies the average reactive power of 2.3VARs in this condition. Whereas the reduced dc-link voltage of 18V is sufficient to compensate the voltage sag with 1.9VARs of source reactive power with the PAC control which can be observed from Figure 5.18.

5.7 Experimental Verification

The competence of the proposed algorithm is validated through experimental setup, which is developed in the laboratory using system parameters designed same as simulation studies at source phase rms voltage of 115V with three-phase linear lagging power factor loads of 500W+ j200VAR and 500W+j800VAR. Figure 5.19 shows the experimental results with loading reactive power demand of 200VAR, which falls within the compensation region of the TCZ-PPF. The voltage sag of 20% magnitude is generated with the help of sag generator setup to validate the performance of hybrid UPQC with and without proposed PAC approach.

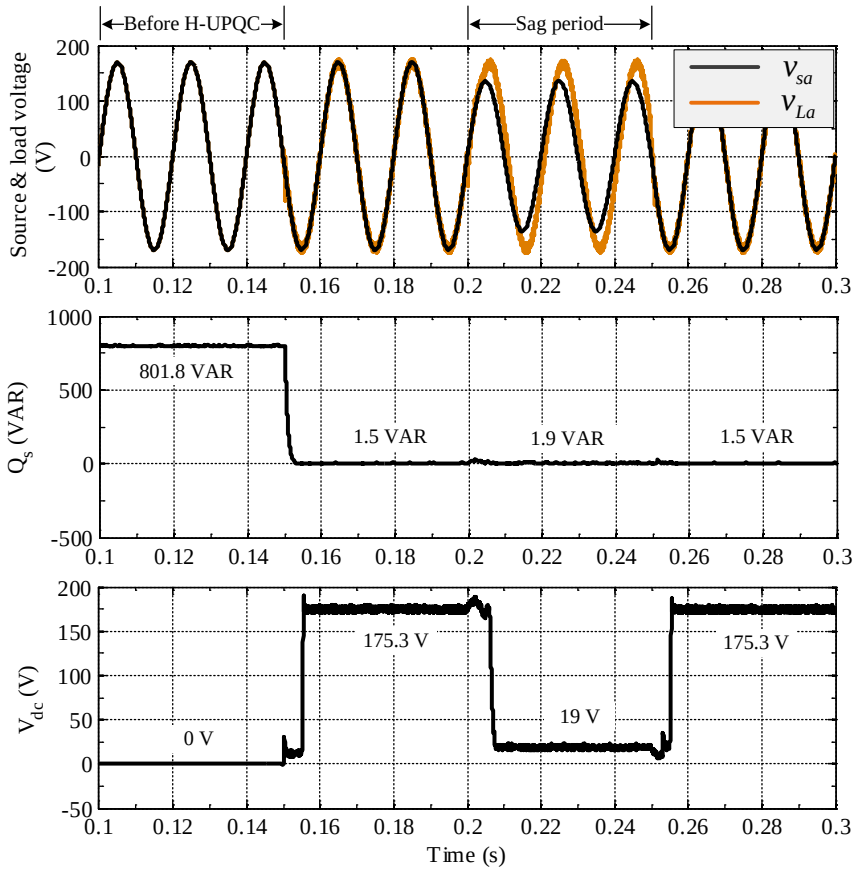
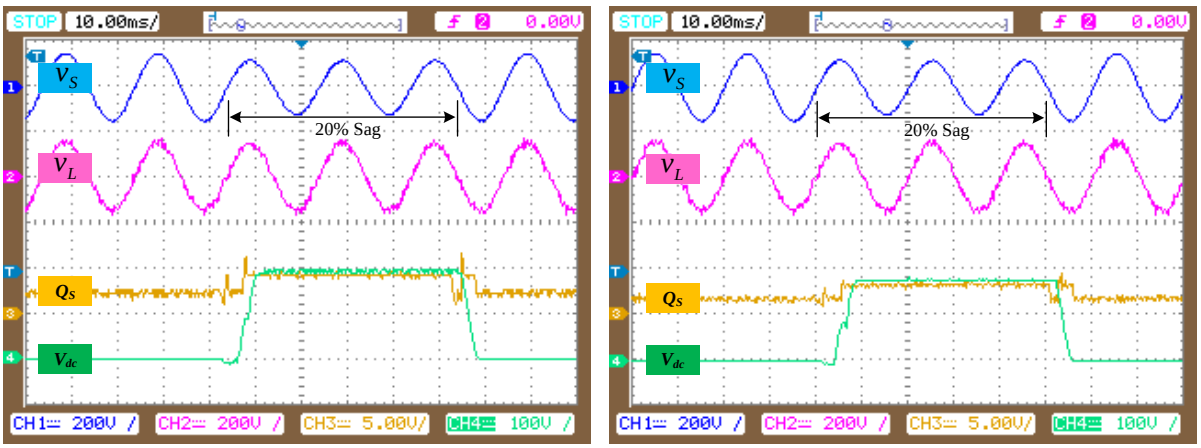


Fig. 5.18: Minimum dc-link voltage requirement during sag condition with 800VAR with PAC control algorithm.

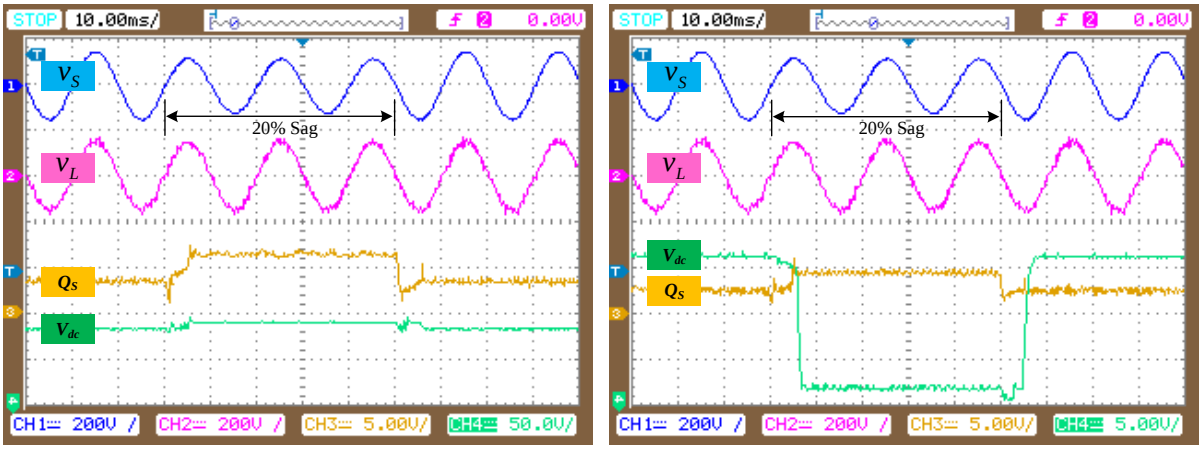
Figure 5.19(a) shows the source voltage and load voltage of phase-*A* along with dc-link voltage and reactive power supplied by the source to the load before application of PAC control approach ($\delta = 0^0$). It is observed that the hybrid UPQC requires the dc-link voltage of ~4V to compensate load reactive power of approximately 98.5%, if voltage sag in not present in the system. Ideally, the dc-link voltage should be zero for the compensation of reactive power of 200VAR, which falls in the design area of TCZ-PPF. However, the small amount of dc-link voltage is required for this case because to supply the losses in the power converters. Whenever the sag exists, it demands increased value of dc-link voltage of 202V with source reactive power of 4.5VARs for voltage sag of 20%. Whereas the PAC algorithm demands dc-link voltage of 186V with phase angle shift of 4^0 throughout the voltage sag period with effective compensation of voltage sag and reactive power demanded by the load, which is observed from Figure 5.19(b) and 5.21(a).

Figure 5.20 shows the experimental results with loading reactive power demand of 800 VAR, which falls outside compensation region of the TCZ-PPF. If there is no voltage sag in the system, then hybrid UPQC demands dc-link voltage of ~170V whereas in case of voltage sag compensation period, it is maintained at ~180V. The application of PAC algorithm reduces the dc-link voltage requirement to 16V with phase angle shift between source voltage and load voltage of 19^0 as shown in Figure 5.21(b).



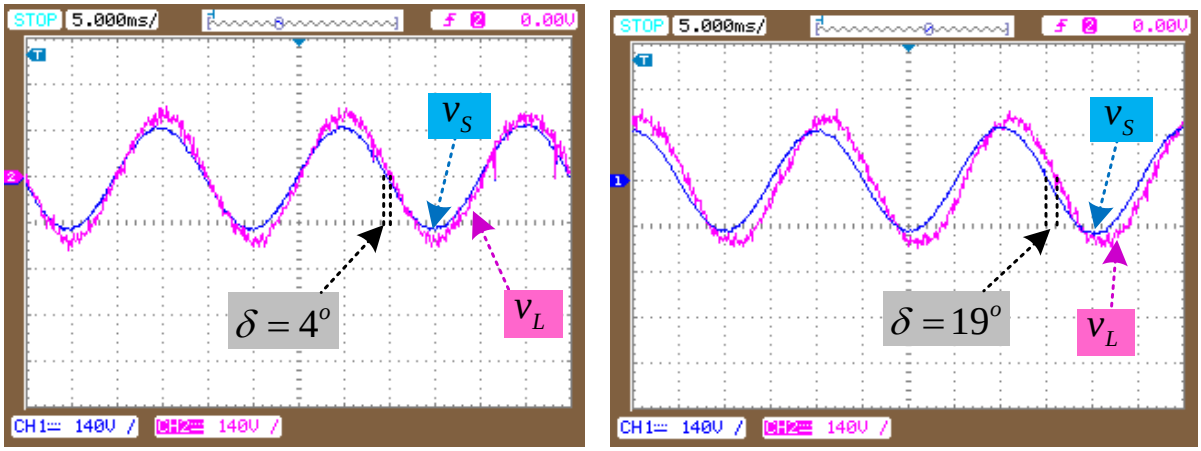
(a) (b)

Fig. 5.19: Experimental results of minimum dc-link voltage requirement during voltage sag condition. (a) without application of PAC approach and (b) with PAC algorithm.



(a) (b)

Fig. 5.20: Experimental results of minimum dc-link voltage requirement during voltage swell condition. (a) without application of PAC approach and (b) with PAC algorithm.



(a) (b)

Fig. 5.21: Phase angle displacement between source voltage and load voltage obtained with the application of proposed algorithm during (a) voltage sag condition and (b) voltage swell condition.

5.8 Conclusion

The extension of the PPF based hybrid UPQC from Chapter 4 is carried out by introducing variable loading reactive power compensation by the control of impedance of PPF with the help of TCR by connecting in parallel to the capacitive reactance. The effectiveness of the proposed topology of TCZ-PPF based hybrid UPQC is evaluated with lagging power factor load. The loading reactive power is selected inside and outside regions of the compensation range provided by TCZ-PPF. An algorithm is proposed to select the optimal phase shift angle to minimize the dc-link voltage requirement. The simulated results shows that the selected minimum dc-link voltage can effectively compensates against voltage sag introduce into the system.

This chapter describes the structure of the transformer-less series injection (TLSI) based UPQC topology is analysed and compared to a conventional 3P4W UPQC topology. The advantages and challenges of the considered topology are highlighted. The solutions to these challenges are also discussed and a control strategy is proposed and discussed in detail to achieve the desired performance from the TLSI-UPQC topology explained. The Simulink model is developed in the MATLAB/Simulink. The performance is evaluated through simulation study and validated with the laboratory experimental results.

6.1 Introduction

UPQC is a topic of research Interest in which research has been carried out to improve performance, efficiency, and reduce cost. Various UPQC topologies have been introduced in an effort to reduce the overall while maintaining its performance and efficiency. A reduction in the number of components can lead to a reduction in the cost of a UPQC. Few attempts were made to decrease the overall size by reducing the number of semiconductor switches in single-phase and in three-phase topologies. In single-phase systems (1P2W), the most common UPQC topology consists of two H-bridge inverters as shown in Figure 6.1 [245]. The total number semiconductor switches in this topology is eight.

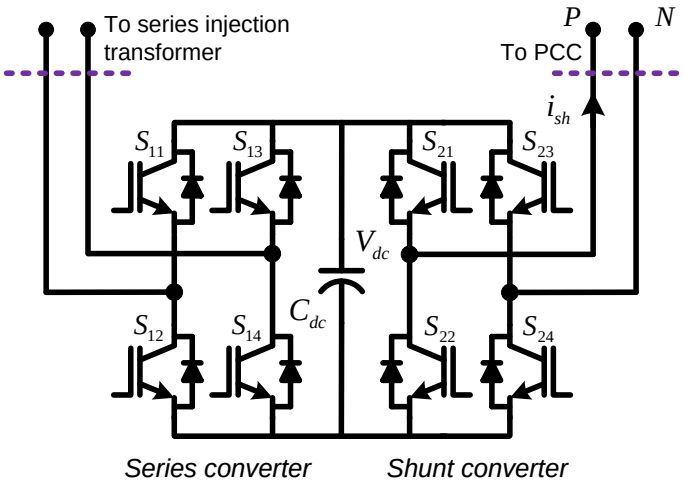


Fig. 6.1: Structure of UPQC for 1P2W system [231].

In [255], a reduced switch count topology is proposed for 1P2W system, which consists of three legs (total six switches) as shown in Figure 6.2(a). In this topology, the first leg handles series voltage injection through transformer while the second leg handles shunt current injection to PCC. The third leg is common for both series and shunt operations and the suitable control is implemented to ensure proper operation of the UPQC. Another example of reduced switch count UPQC for 1P2W system is shown in Figure 6.2(b) [231]. In this case UPQC is realised using two half-bridges with a total number of four switches only [231]. The dc-link in this case is split into two with its centre point connected to the series transformer as well as the neutral wire. One leg with neutral wire performs shunt

compensation while the second leg provides series compensation. Performance wise, reduced component count topologies may have a negative impact on the UPQC's compensation capabilities [235].

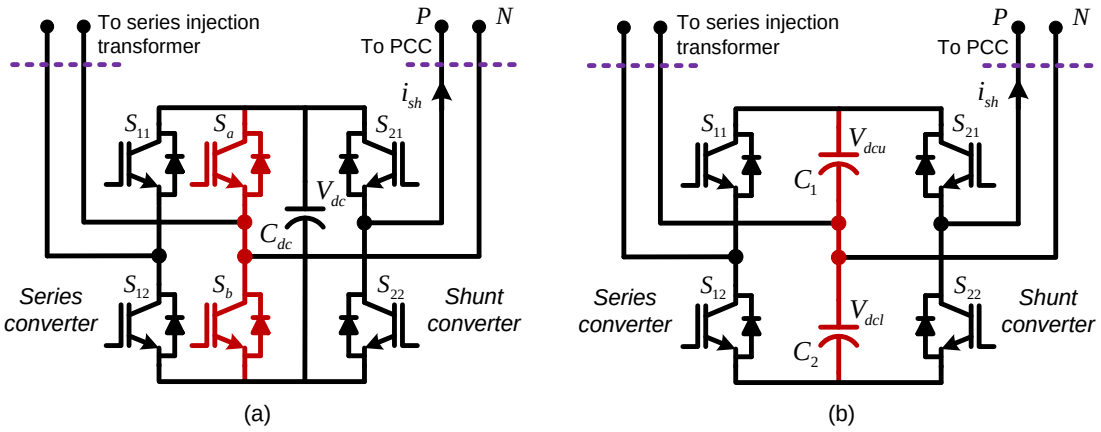


Fig. 6.2: Topology structures of reduced switch count for 1P2W system [231].

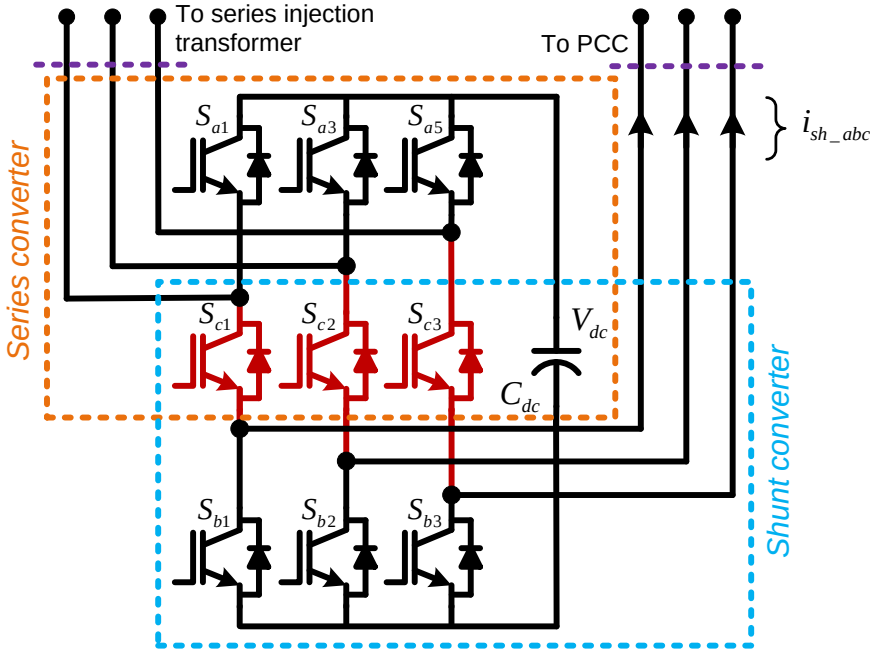


Fig. 6.3: Topology of nine switch UPQC of reduced switch count for 3P3W system [231].

In case of three-phase systems, few topologies are presented with reduced switch count. The conventional UPQC structure consists of twelve switches with six switches of each converter. The switch count is reduced from twelve to eight, nine and ten in [245], [257] and [246] respectively. The nine switch UPQC configuration is shown in Figure 6.3. It consists of a nine-switch converter, which has two groups of outputs, each containing three terminals. The first group of terminals is connected in parallel via coupling inductors and act as the shunt inverter. The second group of terminals is connected in series with the use of injection transformers and functions as the series inverter. Both top and bottom switches are dedicated to function as shunt and series inverters exclusively, whereas, the middle switches are shared between the shunt and series inverters. This sharing imposes a limitation on the

allowed switching states in the converter; all three switches cannot be closed simultaneously in one leg as it would cause the dc-link to short circuit. Using this topology, the number of switches is reduced from twelve to nine, which may reduce the overall cost of the UPQC Shown in Figure 6.4 is the ten switch UPQC, in this configuration, the shunt and series inverters share a common leg, by doing so, the amount of switches is reduced from twelve to ten. Moreover, compared to the nine switch UPQC, the current ratings of the UPQC switches are reduced [257].

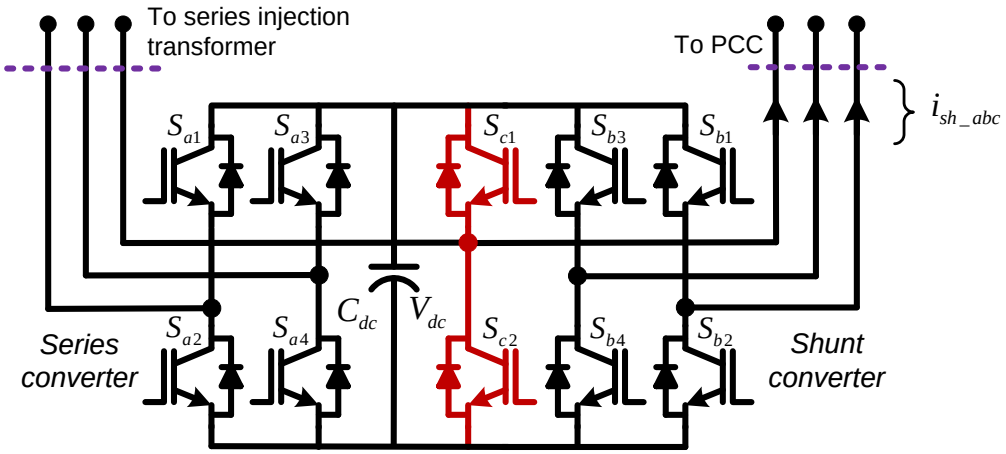


Fig. 6.4: Ten switch topology of UPQC for 3P3W system [257].

Apart from the semiconductor switches, a major common component among all the UPQC topologies is the series injection transformer. This series injection transformer acts as interface between series inverter and supply such that the series part can act as controlled voltage source. However, transformer requires a flux capacity rated at twice the rated injection voltage due to the requirement of generating arbitrary waveforms as fast as possible. As a result, transformer is generally large, heavy, and expensive. Moreover, due to the larger transformer leakage reactance, a sudden voltage Injection by the series converter may cause a DC biasing and thus, may saturate the transformer. This can lead to excessive currents that may damage the series converter if not accounted for [90], [91].

The topic of series injection transformer-less UPQC has not gained the interest of researchers, as there are very few papers published on this subject [254]. One of the key reasons could be the trade-off between cost and galvanic isolation between the source and converter. In [231], a transformerless UPQC is proposed for 1P2W systems, where even reduced switch count of four have been used. It consists of two half-bridge voltage source inverters with one connected in parallel with the load and another one connected in series with the ac mains. The two inverters share the same dc-link.

This chapter focuses on transformer-less series injection configuration for 3P4W UPQC. The authors of [246] proposed a topology, as shown in Figure 6.5, where three H-Bridges are connected in series with the source. Moreover, passive filters are incorporated to remove switching ripples. The series converter in conjunction with the filters injects the

compensating voltage in series with source while forgoing the use of series injection transformer. Although this topology avoids the use of transformer, it utilizes 12 switches per phase in addition to three dc-links, with a total of 36 switches. This increases the component count significantly when compared 12 switches of the 2C topology [45], 14 switches of the 4L topology [13], and 18 switches of the 3HB topology [18]. Furthermore, as seen from the figure, the galvanic isolation between the supply and series converter is lost in the topology, and thus, any fault in series inverter may completely shutdown the entire system. In regular, series transformer based topologies, the series converter can be bypassed through a semiconductor switch across the series injection transformer.

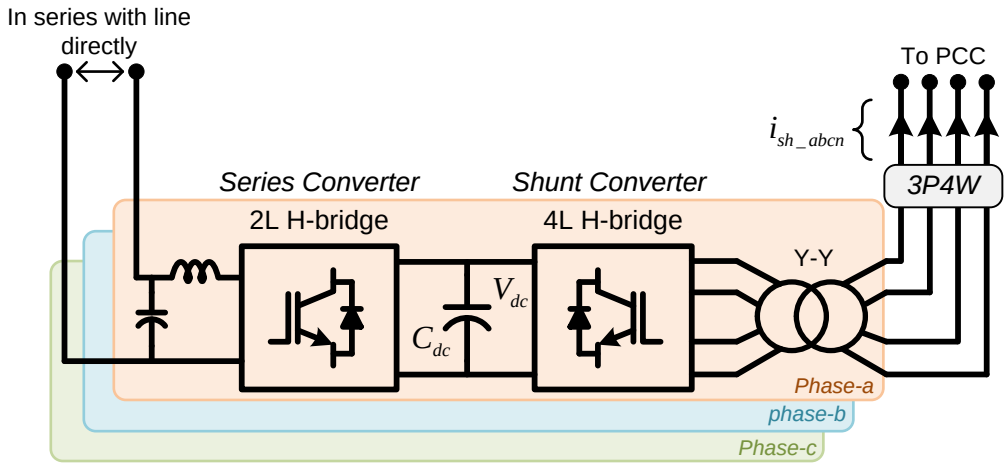


Fig. 6.5: Transformerless UPQC configuration for 3P4W system [264].

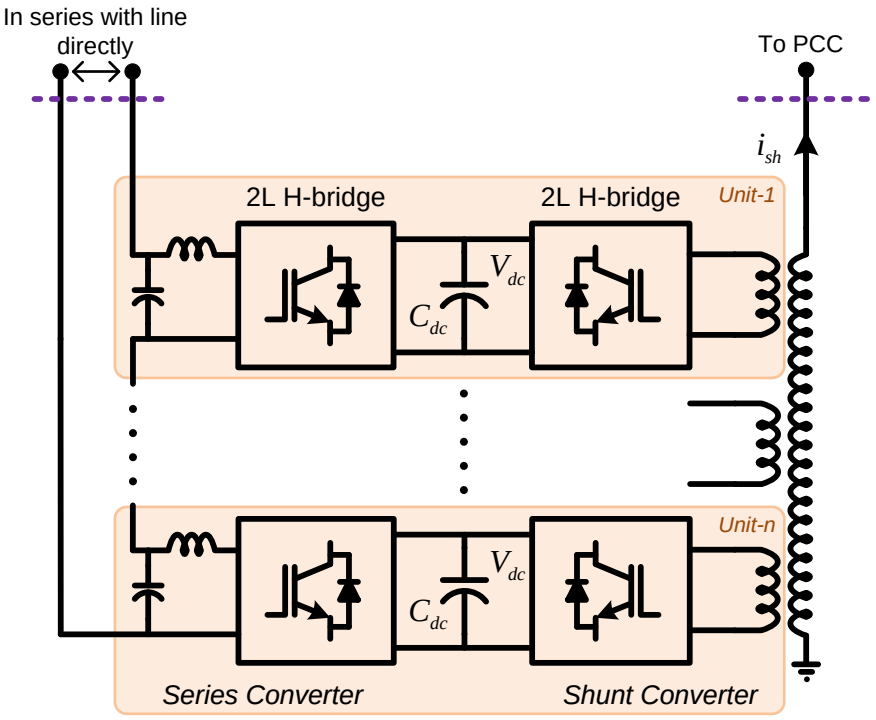


Fig. 6.6: Modular UPQC for 3P3W system (UPQC-MD) [256].

Figure 6.6 shows a configuration of the transformerless UPQC based on several pairs of H-bridge modules for each phase [245]. Each pair has two H-bridge modules connected in

parallel through a common dc-link capacitor. The H-bridge module in shunt part is connected in series through a multi winding transformer, while the H-bridge in series part is directly connected in series and inserted in the distribution line without need of series injection transformer. As the number of modules increase, the voltage handled by each individual H-bridge would reduce, and thus, it can be useful in the medium voltage application to achieve higher power levels. This UPQC-MD would require two H-bridges (eight semiconductor witches) for each of the phases, i.e., 32 semiconductor switches for a three-phase system. Another interesting topology of series transformer-less UPQC is presented in [217].

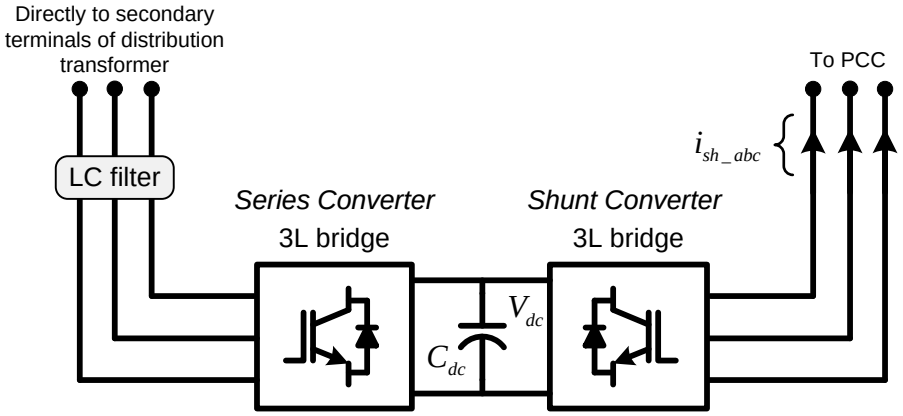


Fig. 6.7: Transformerless UPQC for 3P3W system [217].

In this topology, the UPQC is directly integrated with in-coming distribution transformer in 3P3W system as shown in Figure 6.7. However, this topology is not extended to 3P4W systems and also do not provide the control details. In this chapter, a TLSI-UPQC is proposed for 3P4W system along with the control algorithm to achieve the desired performance.

6.2 Structure Description

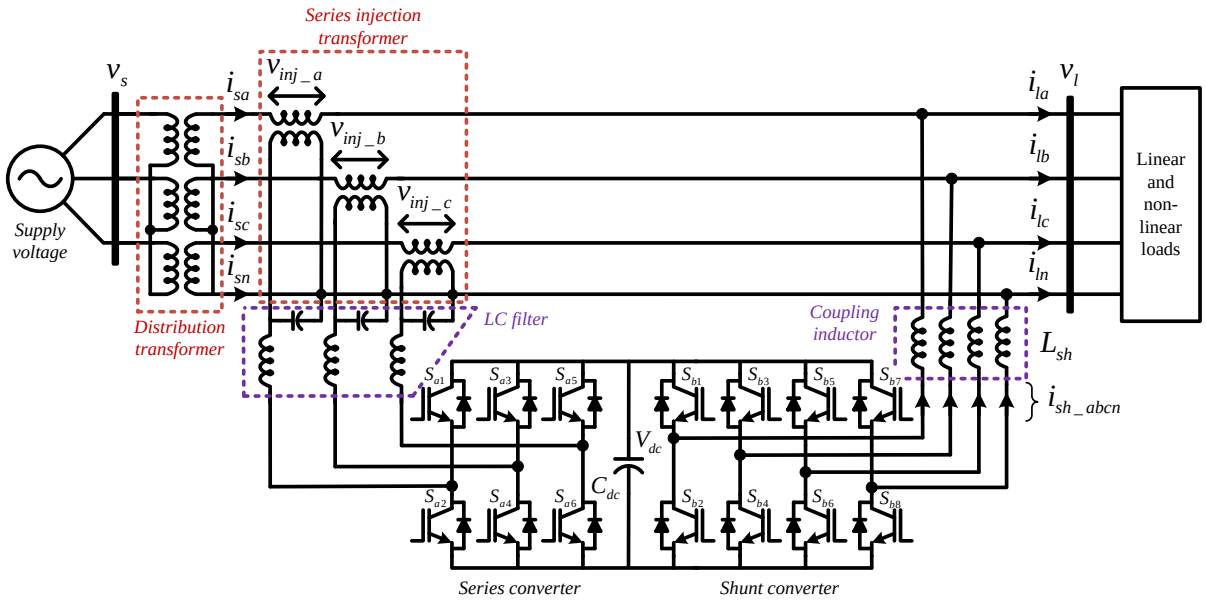


Fig. 6.8: Structure of UPQC for 3P4W system [230].

Figure 6.8 illustrates a four leg (4L) based 3P4W UPQC topology. This configuration is considered as the conventional topology is this work. The series converter is connected to the system through series injection transformer. A 4L shunt converter is connected in parallel to the PCC. The three legs of the shunt converter carry out the harmonic and reactive current compensation in addition to dc-link regulation, while the fourth leg compensates the neutral current. In 3P4W systems, the neutral current can be calculated as shown below [230]:

$$i_{ln} = i_{la} + i_{lb} + i_{lc} \tag{6.1}$$

Where i_{ln}, i_{la}, i_{lb}, and i_{lc} are the load neutral, phase-*a*, phase-*b* and phase-*c* load currents respectively. The reference neutral compensating current for the fourth leg of shunt converter is determined as follows,

$$i^{*}_{sh\_n} = -i_{ln} \tag{6.2}$$

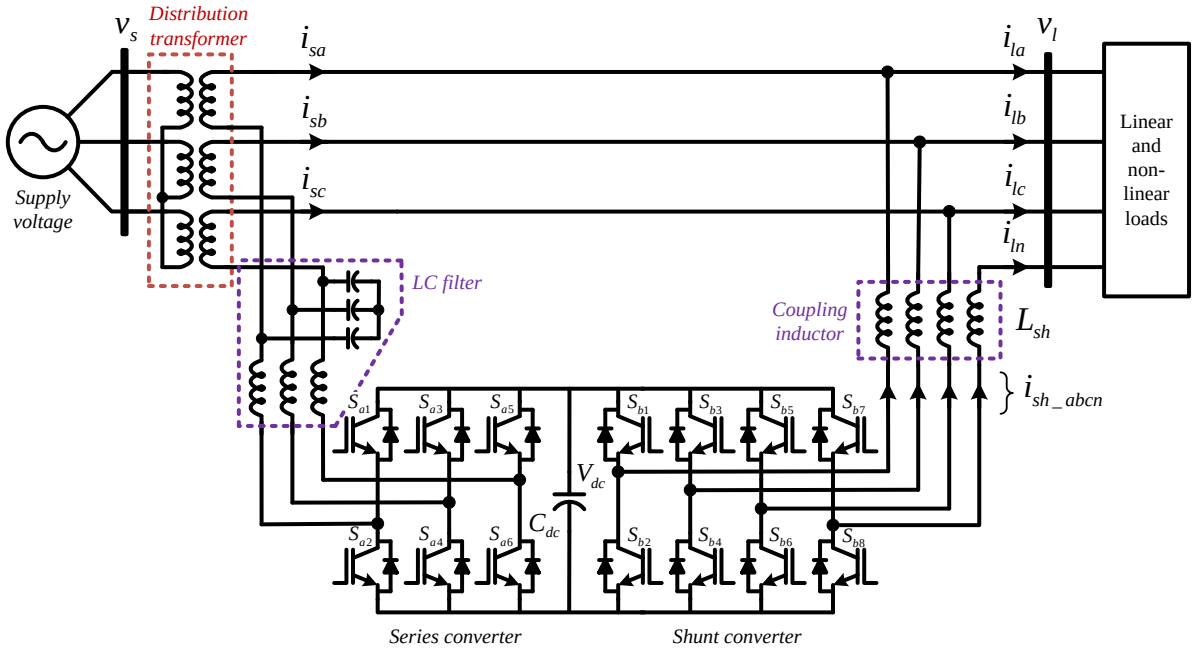


Fig. 6.9: Proposed transformer less series injection based UPQC (TLSI-UPQC) for 3P4W system.

The proposed TLSI-UPQC topology is shown in Figure 6.9. The system consists of a voltage source, distribution transformer, UPQC, and a load. However, instead of connecting the series converter to the system via a series injection transformer, the converter is connected to the bottom terminals of the distribution transformer. The elimination of series injection transformer can decreases the overall size of the system as discussed in the above sections. As normal UPQC configuration, an LC filter is introduced at its terminals to filter out high frequency switching ripples of series converter. For the shunt converter, three out of four legs are connected to the three phases of the system through the coupling inductor. The fourth leg is used to realize a neutral point for single-phase loads. An additional inductor is connected in the neutral leg also to filter the ripples around switching frequency.

6.2.1 Features and Challenges

Through the aforementioned configuration, the need of a series injection transformer is eliminated. Instead, the series converter is integrated into the distribution transformer directly.

Two key advantages are gained by this reconfiguration:

- The number of components is reduced in the UPQC, possibly reducing its overall cost.
- Potential problems associated with the inclusion of a series injection transformer, as mentioned in Section 6.2 are avoided.

Flux requirements for arbitrary waveform generation are handled by the source instead of the converter, and chances of transformer saturation due to dc biasing is significantly reduced due to the large size of the transformer. Furthermore, the location of UPQC in this topology is intuitive since UPQCs are generally placed downstream from distribution transformer.

Despite the advantages, some challenges are also observed:

- The neutral point of distribution transformer is lost due to the series converter transformer connection. Thus, for proper operation, care should be taken such that the series converter provides a virtual neutral to realize a 3P4W system.
- Since the physical neutral point is not available from the distribution transformer, an additional path is needed to connect single-phase loads.

6.2.2 Equivalent Circuit and Operation:

The equivalent circuit of TLSI-UPQC is shown in Figure 6.10. The series converter, comprised of switches S_{a1} through S_{a6}, acts as a voltage source connected in series with the incoming voltage from the distribution transformer. This allows the converter to inject a voltage directly into the system. As mentioned earlier, by connecting the series inverter directly to the distribution transformer's bottom terminals, the neutral point is lost. However, two solutions are possible to the above problem. In the first solution, either the three top switches (marked as S_{a1}, S_{a3}, S_{a5}) or bottom three switches (marked as S_{a2}, S_{a4}, S_{a6}) can be closed during normal operating conditions to form a neutral point. This solution, however, may introduce a dc bias to the distribution transformer, which can cause it to saturate. A tentatively, the series converter is controlled to maintain a zero average voltage across all three legs, which in turn appears as a zero voltage after the LC filter, creating a virtual neutral point. When a voltage related problem is detected, such as sag, the series inverter detects it and injects the appropriate compensation voltage to maintain load voltage at rated value and free of harmonics. On the other hand, three of four shunt inverter legs, denoted as S_{b1} through S_{b6}, perform harmonic and reactive current compensation such that the source sees the load as linear and resistive. Furthermore, these converter legs perform dc-link

regulation to ensure proper operation of the UPQC. The fourth leg of the shunt inverter, denoted as S_{b7} and S_{b8}, offers a path for neutral current.

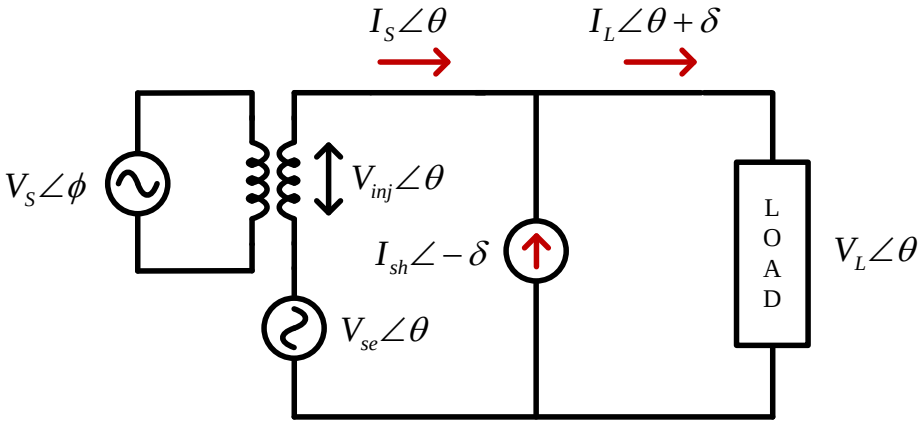


Fig. 6.10: Equivalent circuit of TLSI-UPQC.

6.3 Control Strategy of TLSI-UPQC

The control strategy is realised using synchronous reference frame (*d-q* method) along with Proportional-Resonant (PR) controllers.

6.3.1 Control Strategy of Shunt Converter:

The reference current extraction provides information about the load current, such as harmonic content or unbalance, from which proper switching of the shunt converter is determined.

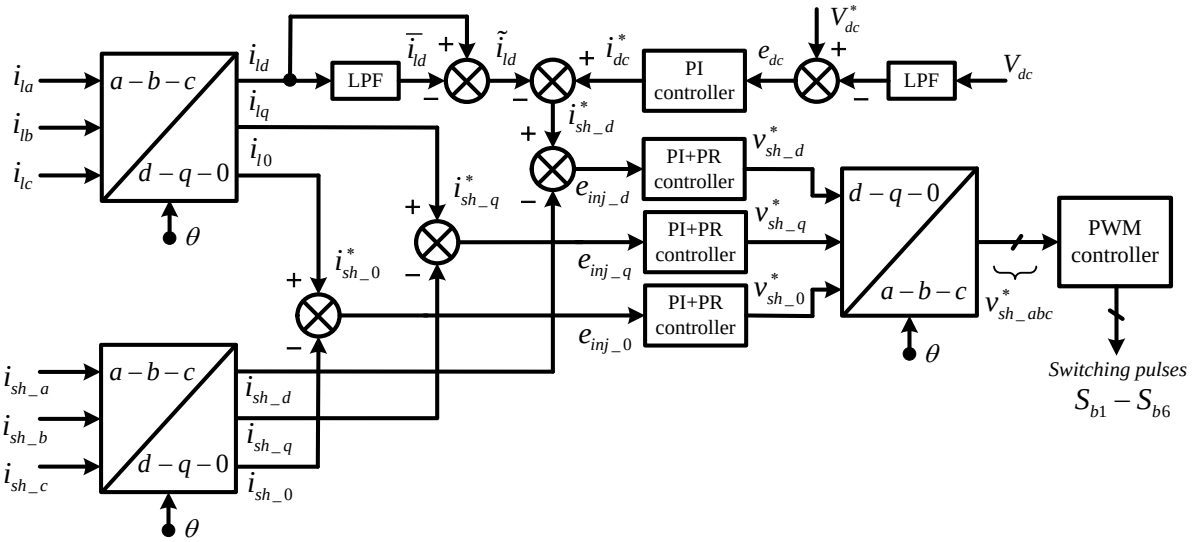


Fig. 6.11: Block diagram of control strategy of shunt converter.

Two conventions are normally used when extracting reference currents, the direct and indirect methods. In the indirect method, the extracted reference corresponds to the ideal source current with no harmonics or reactive power content. By comparing the actual and reference source currents and forcing it to follow the extracted reference, the shunt converter

indirectly injects the correct compensation currents to obtain the reference source waveform. On the other hand, with the direct method, the extracted reference corresponds to the shunt converter current. As a result, no extra knowledge about the source current is required since the shunt converter currents to be injected are directly obtained.

The proposed scheme for TLSI UPQC is shown in Figure 6.11. As seen, for the shunt converter, the load current is measured and transformed from *a-b-c* to *d-q* reference frames using the *d-q* transformation matrix as follows:

$$\begin{pmatrix} i_{ld} \\ i_{lq} \\ i_{l0} \end{pmatrix} = T_{abc}^{dq0} \begin{pmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{pmatrix} \tag{6.3}$$

Where T_{abc}^{dq} is the transformation matrix, is given in (2.2)

$$T_{abc}^{dq0} = \frac{2}{3} \begin{pmatrix} \cos(\omega t) & \cos(\omega t - 120^0) & \cos(\omega t + 120^0) \\ -\sin(\omega t) & -\sin(\omega t - 120^0) & -\sin(\omega t + 120^0) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix} \tag{6.4}$$

Where, ωt is aligned with the load voltage and is extracted using PLL. The *d* and *q* components of the *d-q* transform can be split into a fundamental component ($\bar{\imath}_l$) and a harmonic component ($\tilde{\imath}_l$). These components can be represented as,

$$\begin{pmatrix} i_{ld} \\ i_{lq} \\ i_{l0} \end{pmatrix} = \begin{pmatrix} \overline{i_{ld}} + \tilde{i}_{ld} \\ \overline{i_{lq}} + \tilde{i}_{lq} \\ i_{l0} \end{pmatrix} \tag{6.5}$$

To control the shunt converter, the direct reference current extraction method is used. As mentioned earlier, in the direct method, the extracted reference corresponds to the shunt converter currents. Therefore, $\tilde{\imath}_{ld}$, $\bar{\imath}_{lq}$, $\tilde{\imath}_{lq}$ and i_{lo} are used for the compensation currents. In order to extract $\tilde{\imath}_{ld}$, the load current direct component i_{ld} is passed through a low pass filter with which $\bar{\imath}_{ld}$ is extracted and subtracted from i_{ld}. The reference compensating currents which are obtained in the *d-q* reference frame are shown below.

$$\begin{pmatrix} i_{sh\_a}^{*} \\ i_{sh\_b}^{*} \\ i_{sh\_c}^{*} \end{pmatrix} = \begin{pmatrix} \tilde{i}_{ld} \\ \overline{i_{lq}} + \tilde{i}_{lq} \\ i_{l0} \end{pmatrix} \tag{6.6}$$

The reference current in (6.6) does not consider dc-link regulation nor losses in the UPQC. In order to factor for the above, another current must be added to $i_{sh\_a}^{*}$ that represents the current required to regulate the dc-link and compensate for UPQC losses. This is achieved by comparing the measured dc-link voltage with a reference voltage and

feeding the difference into a PI controller. The output of the PI controller represents the aforementioned current, represented as i_{dc}^{*}. Adding i_{dc}^{*} to $\tilde{\imath}_{ld}$, the final reference currents for the shunt converter obtained is shown below.

$$\begin{pmatrix} i_{sh\_a}^{*} \\ i_{sh\_b}^{*} \\ i_{sh\_c}^{*} \end{pmatrix} = \begin{pmatrix} \tilde{i}_{ld} + i_{dc}^{*} \\ \overline{i_{lq}} + \tilde{i}_{lq} \\ i_{l0} \end{pmatrix} \tag{6.7}$$

The shunt converter should be controlled to inject the extracted currents. To do so, the actual shunt inverter currents are measured and converted from the *a-b-c* to the *d-q* reference frame using the same transformation matrix used in (6.3).

$$\begin{pmatrix} i_{sh\_d} \\ i_{sh\_q} \\ i_{sh\_0} \end{pmatrix} = T_{abc}^{dq0} \begin{pmatrix} i_{sh\_a} \\ i_{sh\_b} \\ i_{sh\_c} \end{pmatrix} \tag{6.8}$$

These currents are then compared to the reference shunt currents obtained in (6.7) from which the error signals are obtained.

$$\begin{pmatrix} e_{sh\_d} \\ e_{sh\_q} \\ e_{sh\_0} \end{pmatrix} = \begin{pmatrix} i_{sh\_a}^{*} \\ i_{sh\_b}^{*} \\ i_{sh\_c}^{*} \end{pmatrix} - \begin{pmatrix} i_{sh\_d} \\ i_{sh\_q} \\ i_{sh\_0} \end{pmatrix} \tag{6.9}$$

The above error signals are then passed to a combination of Proportional-Integral (PI) and Proportional-Resonant (PR) controllers from which the PWM modulation signals (in the *d-q* reference frame) are found. An overview about PR controllers is provided in the Appendix-B.

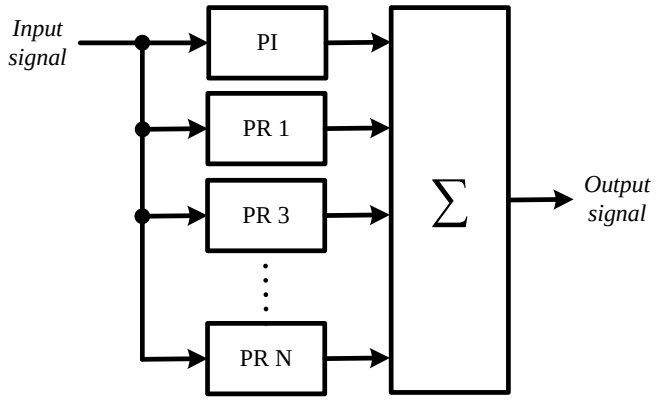


Fig. 6.12: PI+PR controller block diagram.

Because different harmonic components may appear in the *d-q* reference frame depending on loading conditions, multiple controllers are required for correct compensation. As a result, a PI controller in conjunction with several PR controllers are used. The proportional part of the PI controller is used for baseline compensation of all harmonic and fundamental components, whereas the integral part is used for eliminating the steady state

error of the fundamental component, which corresponds to reactive power compensation and dc-link regulation. The PR controllers on the other hand are utilized for unbalance and harmonic compensation.

In *d-q* reference frame, negative sequence currents appear at double the fundamental frequency in the *d* and *q* components. Zero sequence currents appear at the fundamental frequency in the zero component. For compensating unbalanced loads, a PR controller tuned at 100 Hz for the *d* and *q* components, and a PR controller tuned at 50 Hz for the zero component are required. When a nonlinear load is balanced, current harmonics are drawn at (6n-1), rotating with a negative phase sequence, and (6n+1), rotating with a positive phase sequence. However, in the *d-q* reference frame, both harmonics appear at a frequency of (6n), requiring only one controller for every (6n-1) and (6n+1) harmonic pair. In case of unbalanced nonlinear loads, harmonic currents appear at (6n-1) and (6n+1) rotating in the positive and negative phase sequences as with balanced nonlinear loads. Moreover, harmonic currents of the same orders rotating in the opposite directions also appear in addition to a negative phase sequence current. As a result, in the *d-q* reference frame, harmonics appear at (6n-2) and (6n+2) requiring additional PR controllers at those harmonics for correct compensation. Furthermore, additional triplen and odd harmonic currents appear on the *d-q* transform's zero component, requiring controllers at those frequencies to compensate for zero sequence currents. All in all, the following harmonics are chosen for the PR controllers of the shunt converter: for the *d* and *q* components, the PR controllers are tuned to 2nd, 6th, 12th, 18th, 4th, 8th, 10th, and 14th harmonic orders. For the zero component, the PR controllers are tuned to 1st, 3rd, 5th, 7th, 9th, 11th, 13th, 15th, 17th, and 19th harmonic orders. After passing error signals in (6.9) through the aforementioned PI-PR controllers, the desired modulation signals ($v^*_{sh\_d}, v^*_{sh\_q}, v^*_{sh\_0}$) are obtained and then transformed back to the *a-b-c* frame using the inverse *d-q* transformation matrix T^{abc}_{dqo} as shown in (6.10).

$$\begin{pmatrix} v^*_{sh\_a} \\ v^*_{sh\_b} \\ v^*_{sh\_c} \end{pmatrix} = T^{abc}_{dq0} \begin{pmatrix} v^*_{sh\_d} \\ v^*_{sh\_q} \\ v^*_{sh\_0} \end{pmatrix} \tag{6.10}$$

$$T^{abc}_{dq0} = \begin{pmatrix} \cos(\omega t) & -\sin(\omega t) & 1 \\ \cos(\omega t - 120^0) & -\sin(\omega t - 120^0) & 1 \\ \cos(\omega t + 120^0) & -\sin(\omega t + 120^0) & 1 \end{pmatrix} \tag{6.11}$$

The reference modulation signals in (6.10) are then passed through a PWM controller to generate the required gating signals for the shunt converter.

Although the shunt converter is utilized to draw neutral current in place of the missing neutral wire, it is not possible to control it as a current source. Normally, when a neutral wire is available from the source, the neutral current on the load side is forced through the shunt

converter such that it does not flow to the source. In that case, a neutral leg would be able to function by controlling current. However, in TLSI-UPQC, the common point of the loads is floating, therefore, the current cannot be controlled. A voltage control strategy for the fourth leg is proposed, which aims at maintaining the neutral point voltage at zero potential all the time. This proposed approach provides a path for the neutral current. As shown in the highlighted section in Figure 6.13, the neutral leg is controlled by measuring the load voltages in all three phases and summing them as follows:

$$v_n = v_{la} + v_{lb} + v_{lc} \tag{6.12}$$

With this calculation, the neutral voltage due to the unbalance can be obtained. Next, the calculated neutral point voltage is compared to a reference value, zero in this case.

$$e_n = v_n - 0 \tag{6.13}$$

Finally, the switching signals are obtained by passing the error signal to a hysteresis controller.

6.3.2 Control Strategy of Series Converter:

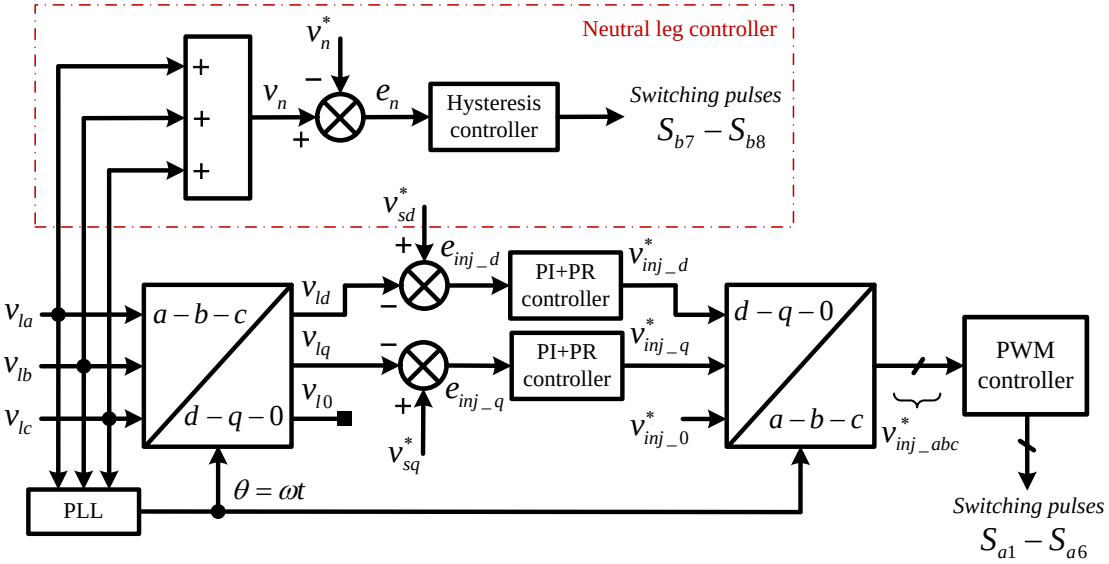


Fig. 6.13: Block diagram of control strategy of series converter

The control diagram of the series converter is highlighted in Figure 6.13. The load voltage is first measured then converted from the *a-b-c* to the *d-q* reference frame using the same *d-q* transformation matrix (T_{abc}^{dqo}) shown in (6.4).

$$\begin{pmatrix} v_{ld} \\ v_{lq} \\ v_{l0} \end{pmatrix} = T_{abc}^{dq0} \begin{pmatrix} v_{la} \\ v_{lb} \\ v_{lc} \end{pmatrix} \tag{6.14}$$

The load voltage itself is used to obtain the angle ωt for the transformation. By doing so, in-phase voltage compensation is facilitated since normal operating conditions results in

d axis value of 1 p.u. and *q* axis value of 0 p.u. Therefore, these values are considered to be the reference values to be targeted by the UPQC. Moreover, since the distribution transformer's primary winding is connected in delta, no zero phase sequence appear on the secondary winding. Consequently, zero sequence voltage does not need to be controlled. After converting the measured voltage to the *d-q* reference frame, it is compared to the reference values for *d* and *q* which are 1 and 0 p.u., respectively to obtain the error.

$$\begin{pmatrix} e_{se\_d} \\ e_{se\_q} \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \end{pmatrix} - \begin{pmatrix} v_{ld} \\ v_{lq} \end{pmatrix} \tag{6.15}$$

The error signal obtained is then sent to a controller that consists of a PI controller and multiple PR controllers. The PI controller is used to compensate for and voltage change in the fundamental component, whereas the PR controller compensates harmonics and unbalance. The PR controllers are tuned in the following manner: one PR controller tuned at 100 Hz is used to regulate the voltage when there are negative phase sequence components in the load voltage (i.e. voltage unbalance). PR controllers are tuned at 6^{th} and 12^{th} harmonics respectively. The output of the controllers correspond to the *d* and *q* components of modulation signal for the series inverter. Next, these signals are then converted from the *d-q* reference frame back to the *a-b-c* reference frame using the inverse of the *d-q* transformation matrix (T_{dqo}^{abc}) as shown below

$$\begin{pmatrix} v_{se\_a}^{*} \\ v_{se\_b}^{*} \\ v_{se\_c}^{*} \end{pmatrix} = T_{dq0}^{abc} \begin{pmatrix} v_{se\_d}^{*} \\ v_{se\_q}^{*} \\ v_{se\_0}^{*} \end{pmatrix} \tag{6.16}$$

Finally, the modulation signals in the *a-b-c* reference frame are sent to a PWM controller to obtain the switching signals of the series converter.

6.4 Simulation and Experimental Results

The investigation on compensation characteristics of proposed topology of TLSI-UPQC is validated through simulations on MATLAB Simulink platform and also verified with the experimental results. Table 6.1 shows the system parameters, which are chosen to implement the MATLAB Simulations and also to conduct experiment on developed prototype. The three-phase delta-star transformer is considered as the distribution transformer on supply side such that primary is assumed to be 11kV and secondary of distribution transformer is step down to 415V. However, the experimental work is carried out at downscale values because of the laboratory limitations on supply system. Based on the available three-phase supply in the laboratory, the primary is connected to 415V and secondary is step down to 200V. At the end of secondary terminals of the transformer, the UPQC system is connected for testing. To authenticate the performance of the prospective

topology, the UPQC is imposed to voltage disturbances such as voltage sag of 20% magnitude, distorted source voltage, unbalanced source voltage; current disturbances such as linear, nonlinear balanced and unbalanced type of loads. The choice of unbalanced load is selected to test neutral line provided by the fourth leg of shunt converter of the proposed topology.

Table 6.1: System parameters.

Description	Parameter value
Supply frequency	50 Hz
Transformer configuration	Delta-Wye
Primary voltage	11kV (L–L rms)
Secondary voltage	415V(L–L rms)
Transformer rated power	30kVA
DC link voltage	700V
DC link capacitance	4700μF
Shunt resistance, coupling inductance	0.1Ω, 2mH
Series resistance and filter components	0.1Ω, 2mH and 30μF
Three-phase diode rectifier fed RL load	60Ω, 30mH
Three-phase RL load	110Ω, 30mH

6.4.1 Source Voltage Sag with Nonlinear Load:

The source voltage is applied with 20% voltage sag at $t = 0.2$s, such that the phase peak magnitude becomes 270.39V during sag period. Figure 6.14 shows the simulation results corresponding to series converter, where axis-1 shows the three-phase source voltage; axis-2 refers to the three-phase series injected voltages; three-phase load voltages are presented in axis-3; axis-4 depicts the dc-link voltage. The dc-link voltage is calculated according to (2.40), which gives 700V for the selected operating conditions of the source voltage. From Figure 6.14 (axis-2), it can be observed that the series converter injects zero voltage during normal operating conditions. When the sag occurs at $t = 0.2$s, the series converter immediately responded and starts injecting the amount of sag voltage in-phase with the supply voltage to ensure the load voltage at PCC is undisturbed. The load voltage in this case is maintained at peak fundamental value of 336.57V and balanced. From the profile of dc-link voltage, it can be noticed that under normal operation of system, the shunt converter control ensures the dc-link voltage remains stable at reference value of 700V. However in the instant of voltage sag, the dc-link voltage is dropped from the reference value and later it is recovered with small fluctuations around the reference value. The validation of

simulation results of Figure 6.14 are performed at downscale in the experiment and presented in Figure 6.15. The scope results are shown for only one phase (phase-a) out of three phases due to balanced condition. Trace-1 shows the source voltage referring to voltage sag period. Trace-2: series injected voltage, which is having magnitude of 31.7V during sag. Trace-3: load voltage at PCC, the magnitude of the phase voltage is measured as 162.4V. Trace-4: the voltage across the dc-link capacitor, which is maintained at an average value of 320V. The reason for the drop in the dc-link voltage at the instant of voltage sag and rise at the instant of sag clearance is same as explained in the Chapter.2. The simulation and experimental results corresponding to the performance of shunt converter are depicted in Figure 6.16 and 6.17 respectively. From Figure 6.16, axis-1 shows three-phase source current, axis-2 refers to three-phase shunt compensating current; axis-3: three-phase load current with non-linear load; axis-4 depicts the neutral current provided by shunt converter. The observations from current characteristics can be made as follows. The rms value of load current is measured as 6.8A, while source current drawn with the rms value of 10.6A, which is slightly greater than the current drawn by the load during sag period.

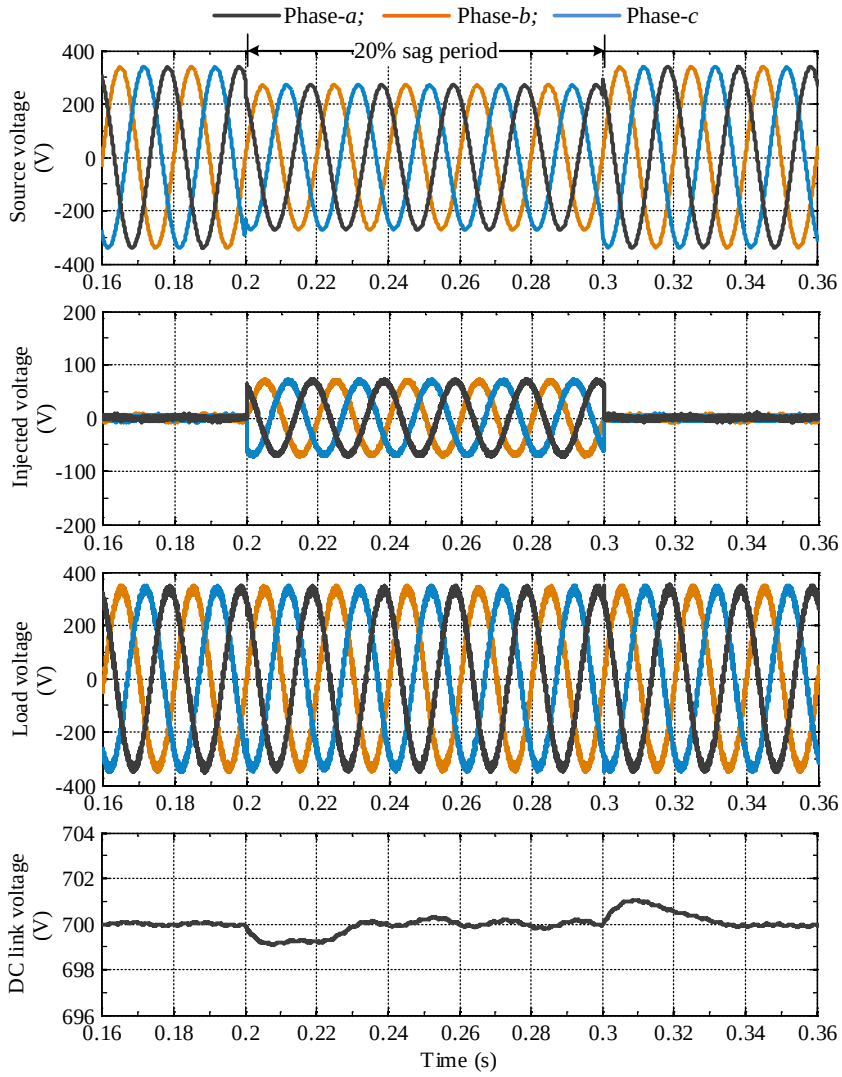


Fig. 6.14: Simulation results of voltage profiles under voltage sag compensation.

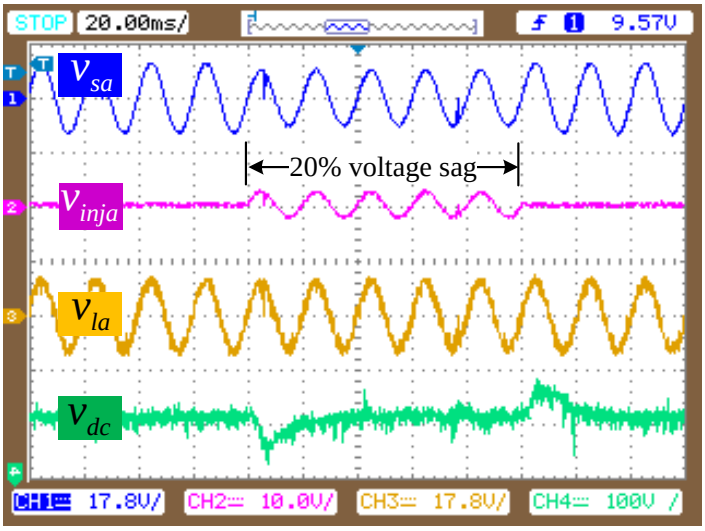


Fig. 6.15: Experimental scope results of voltage profiles under voltage sag compensation for phase–*a* along with dc-link capacitor voltage.

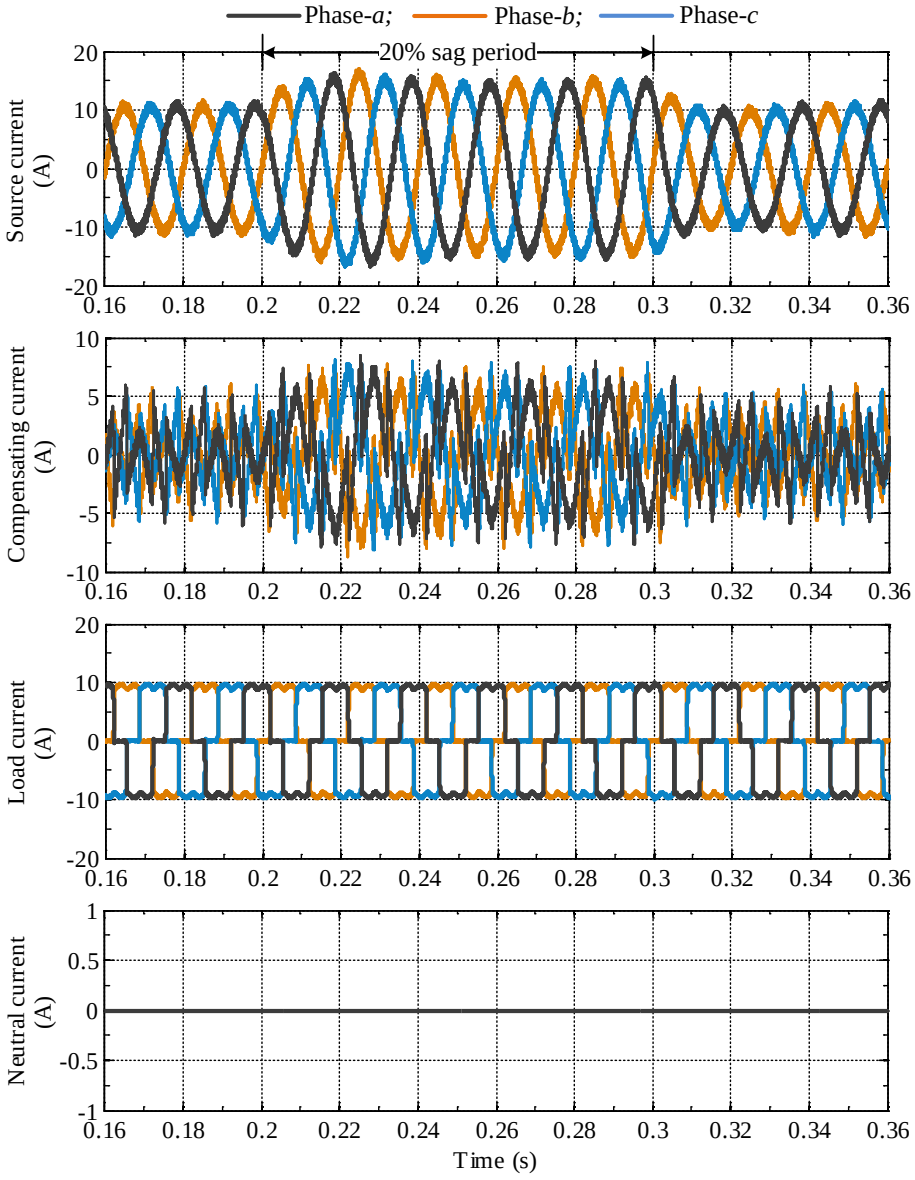


Fig. 6.16: Simulation results of current profiles under voltage sag compensation.

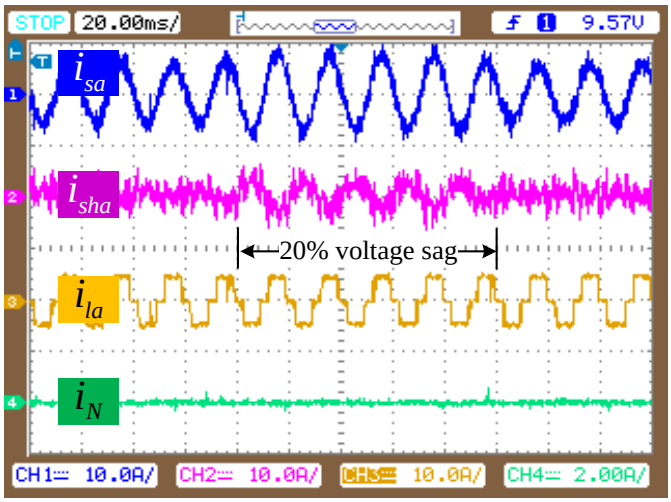


Fig. 6.17: Experimental scope results of current profiles under voltage sag compensation for phase–*a* along with load neutral current.

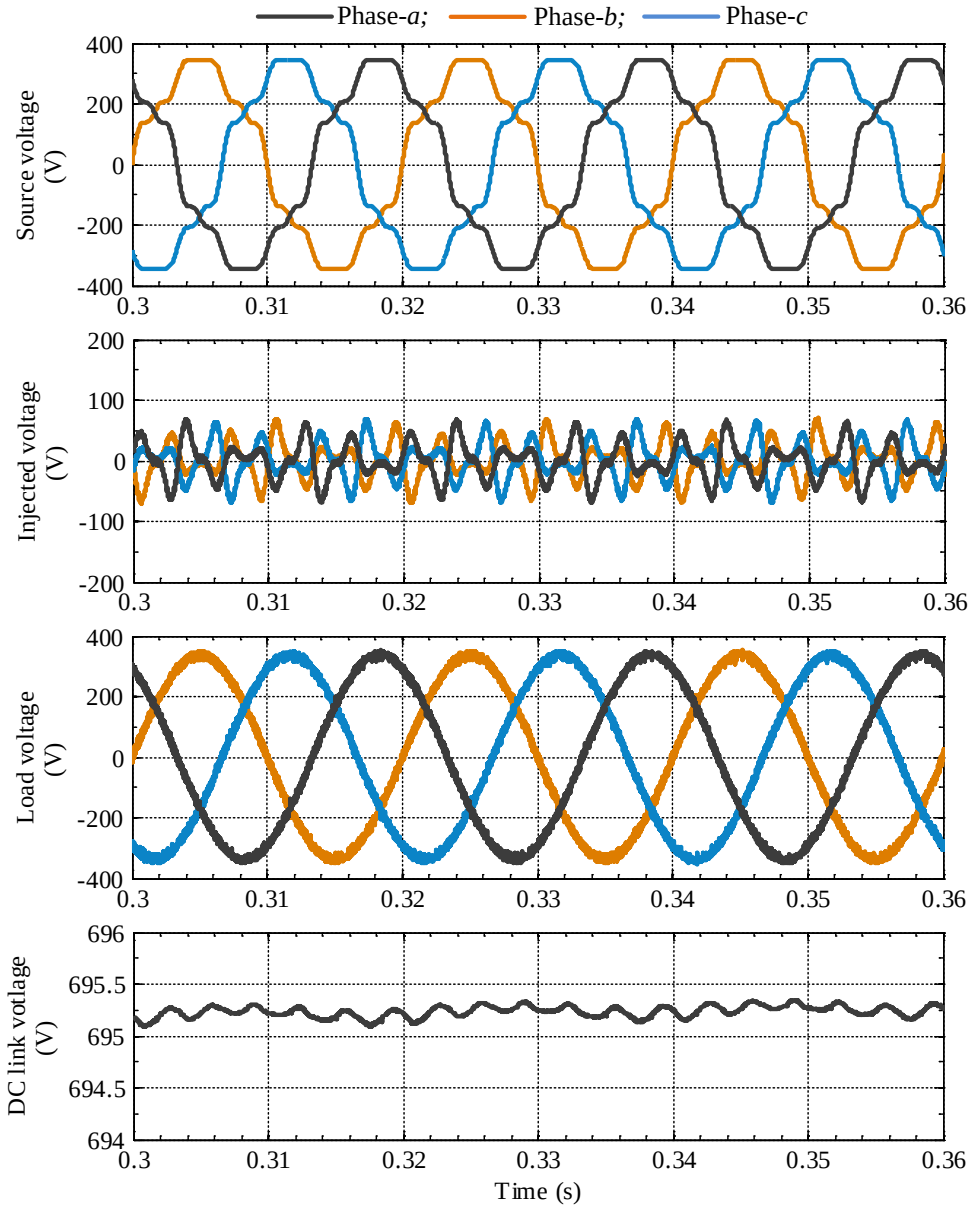
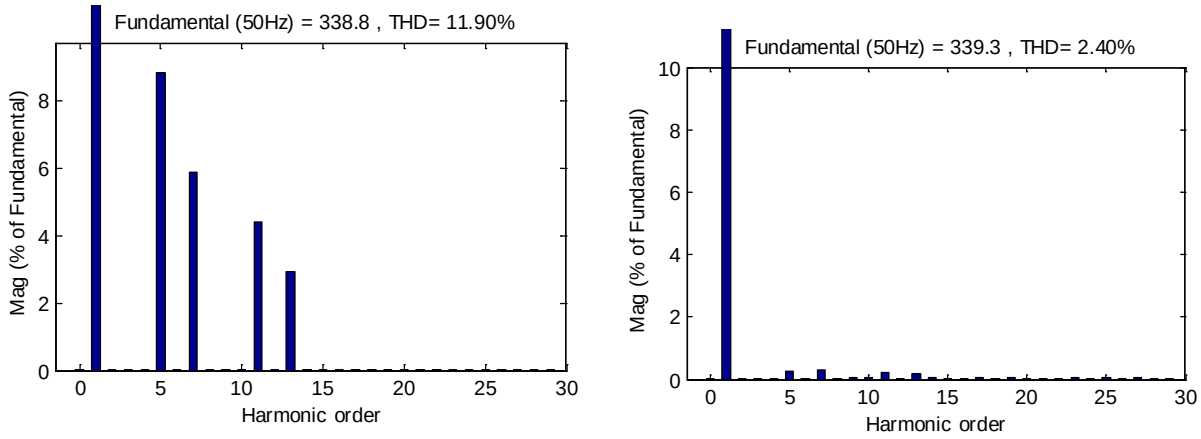


Fig. 6.18: Simulation results of voltage profiles under distorted voltage compensation.

During sag compensation from t =0.2s to 0.3s, the magnitude of source current is further increased from the normal operating conditions. Similar magnitude changes can also be observed in the compensating current waveforms. The reason for such changes are same as explained in the Chapter-2. The THD of source current is 3.5% in this case, which falls within the limits of IEEE-519 standards. The neutral leg current magnitude is zero because of the balanced non-linear load at PCC. From Figure 6.17, trace-1 shows the source current of phase-*a*. The magnitude is measured as 3.8A at normal operation and 5.3A during sag compensation with THD of 4.1%. Trace-2, and trace-3 shows the compensating current and load current corresponding to phase-a respectively. Trace-4 shows the neutral current and which is zero.



(a) (b)

Fig. 6.19: Harmonic spectrum of phase-*a*: (a) source voltage; (b) load voltage

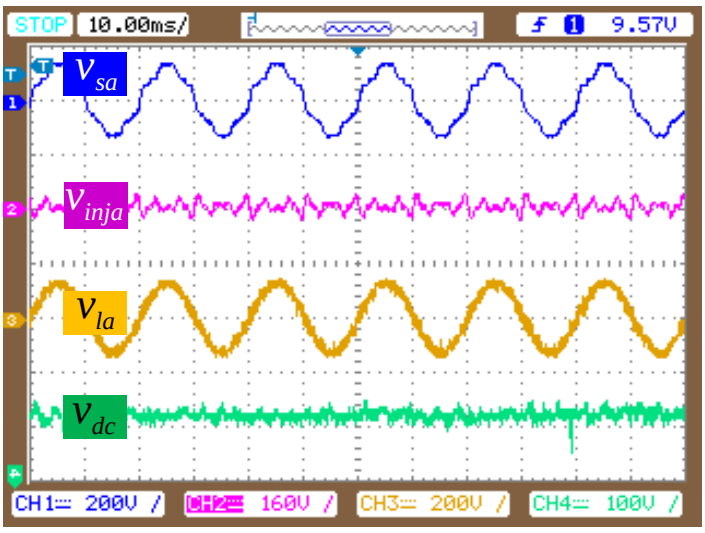
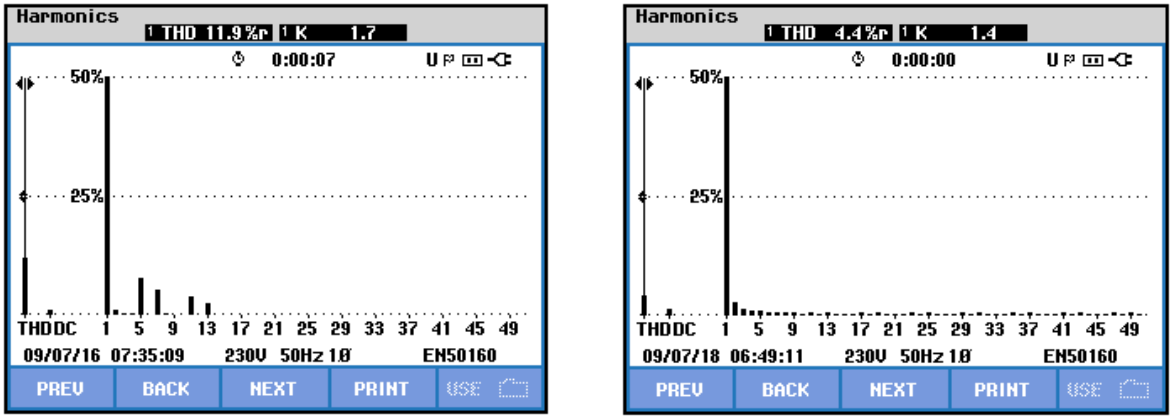


Fig. 6.20: Experimental scope results of voltage profiles under distorted source voltage compensation for phase-*a* along with dc-link capacitor voltage.

6.4.2 Distorted Source Voltage with Nonlinear Load:

Figure 6.18 shows the steady state voltage compensation characteristics with distorted source voltage.



(a) (b)

Fig. 6.21: Harmonic spectrum of phase-*a*: (a) source voltage; (b) load voltage

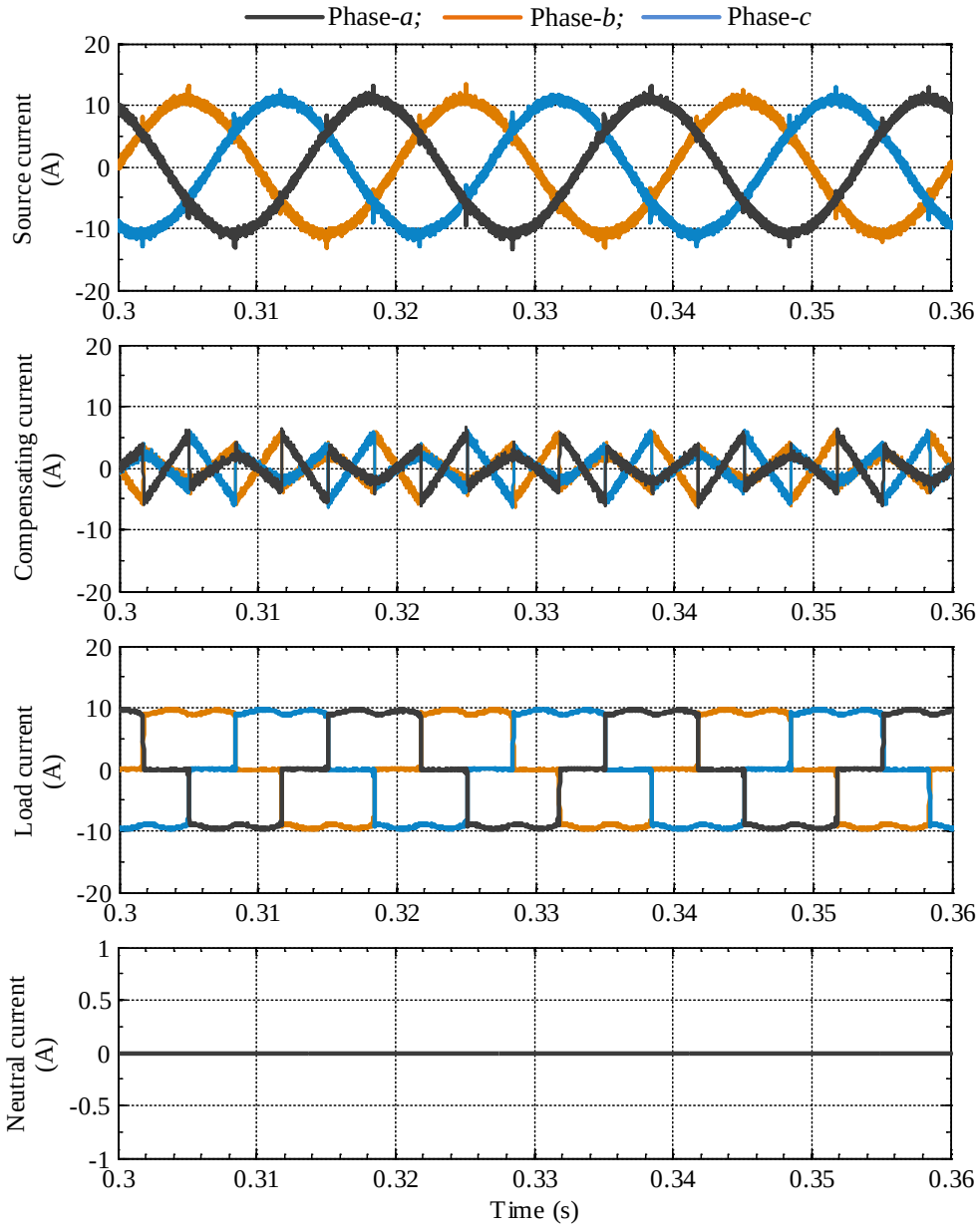
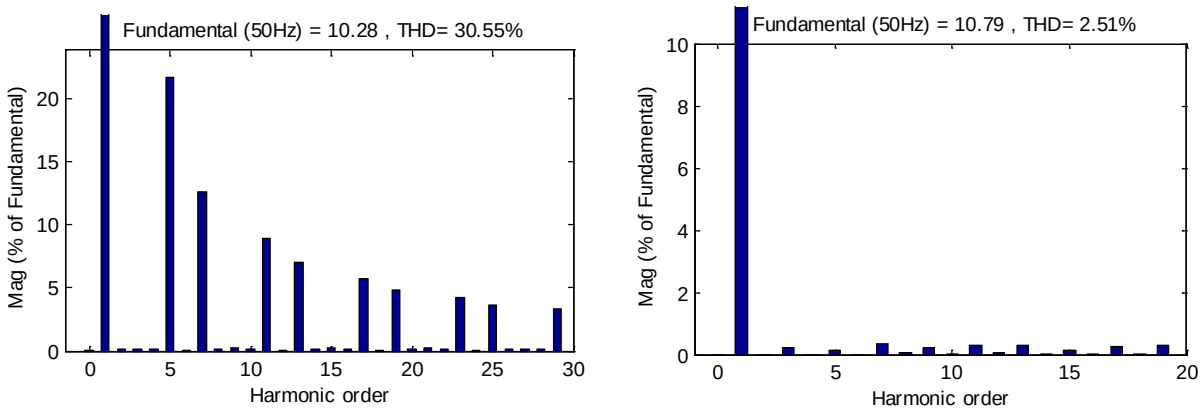


Fig. 6.22: Simulation results of current profiles by the shunt converter under distorted source voltage compensation along with nonlinear load.



(a) (b)

Fig. 6.23: Harmonic spectrum of phase-*a*: (a) load current; (b) source current

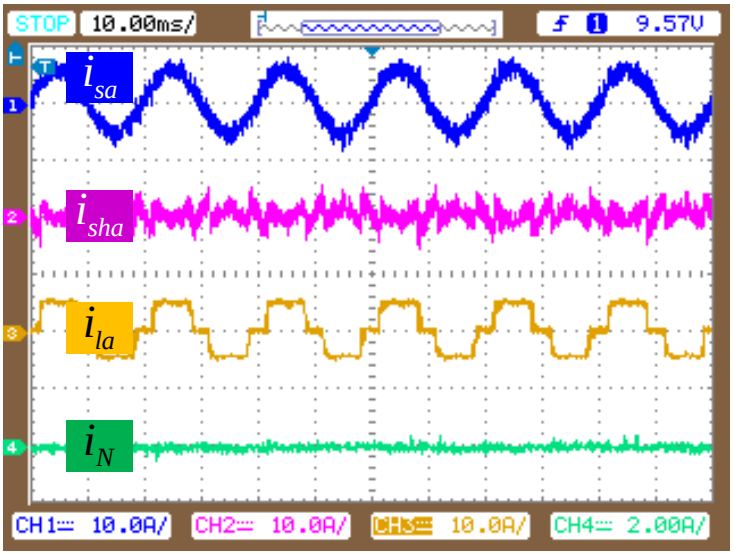
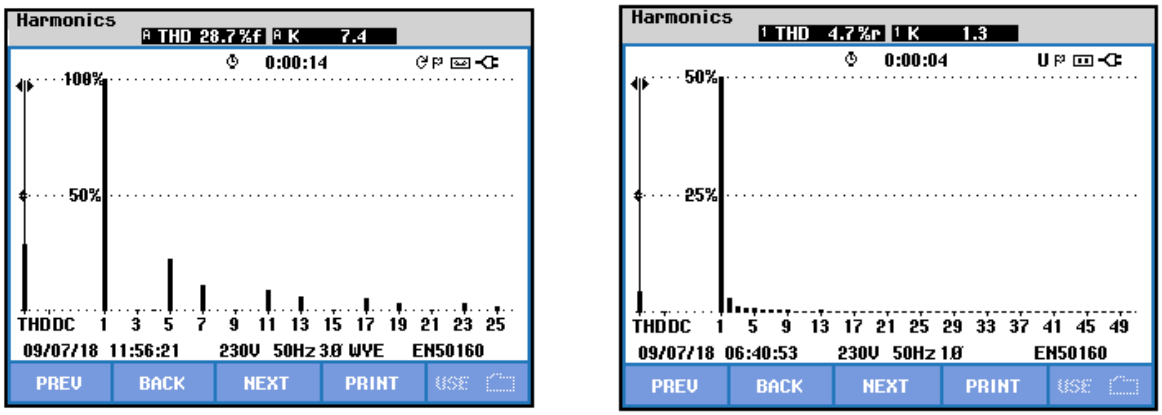


Fig. 6.24: Experimental scope results of current profiles by the shunt converter under distorted source voltage compensation along with nonlinear load.

The distorted source voltage is created as explained in the previous chapters. The three-phase load voltage is shown in axis-3, which is maintained at magnitude of 336.8V with 2.41% of THD by injecting the proper compensating voltages as shown in axis-2. The dc-link voltage is maintained at an average value of 695.24V.



(a) (b)

Fig. 6.25: Harmonic spectrum of phase-*a*: (a) load current; (b) source current

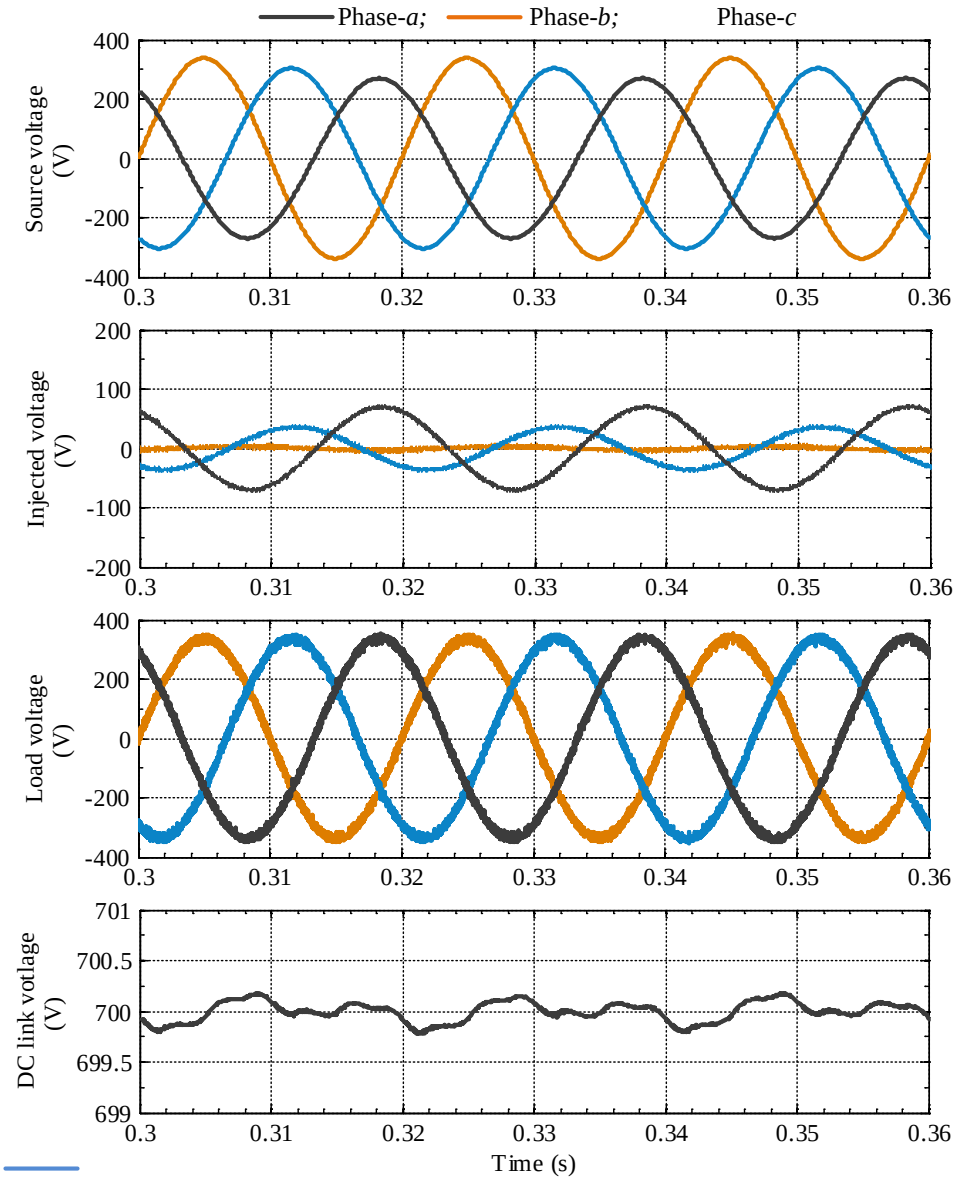
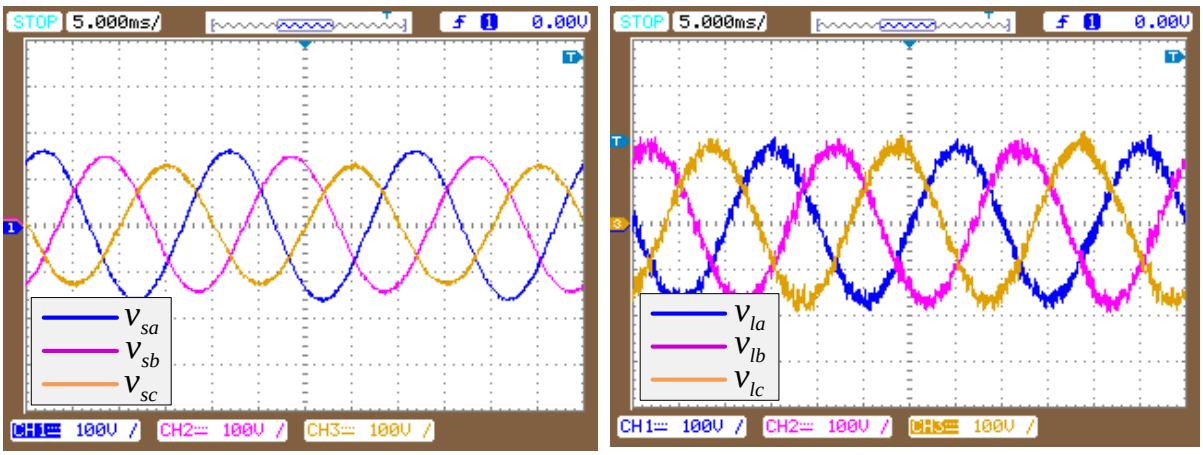
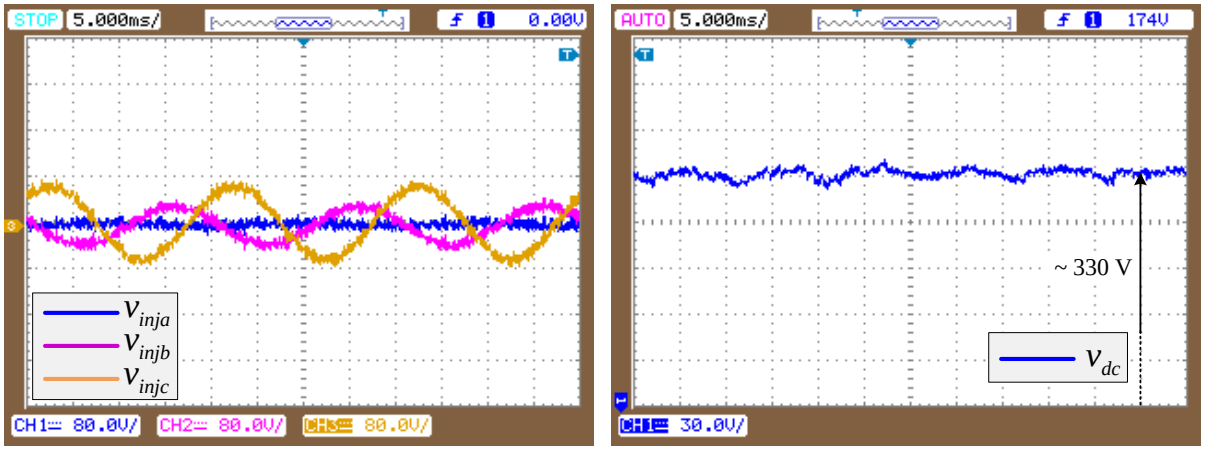


Fig. 6.26: Simulation results of voltage profiles under unbalanced source voltage compensation.



(a) (b)

Fig. 6.27: Unbalanced source voltage compensation (a). Three-phase supply voltages, (b). Three-phase compensated load voltages.



(a) (b)

Fig. 6.28: Unbalanced source voltage compensation (a). Three-phase series injected voltages, (b). The dc-link capacitor voltage.

The magnitude of load voltage and dc-link voltages are measured from the experimental shown in Figure 6.20 are 162.7V and 322V. The THD of load voltage is measured as 4.31%. The current compensation characteristics are shown in Figure 6.22 and 6.24 refers to simulation results and experiment results respectively. The magnitude of source current is 7.2A in simulation results and 3.78A in experimental results with THD of 2.51% and 4.6% in simulation and experiment respectively. The measured values of current characteristics matches with the results, which are presented in the previous case with normal operating conditions i.e. without voltage sag. Because of balanced loading conditions in this case also the neutral leg of shunt converter is idle.

6.4.3 Unbalanced Source Voltage:

The performance of the proposed topology is also verified with the unbalanced source voltage. Since bottom end of the secondary winding of the distribution transformer is connected to the series converter, the neutral point of distribution transformer is lost. If the source voltage on primary is unbalanced then the sum of the three-phase voltages are not equal to zero resulting neutral voltage. To ensure zero neutral voltage to the PCC loads, the series converter has to inject proper amount voltage in each phase. Figure 6.26 shows the steady state simulation results of unbalanced source voltage compensation, where axis-1 shows the three-phase unbalanced source voltage with phase peak value of 202.8V, 338V and 270.4V on phase-*a*, *b* and *c* respectively; axis-2 shows the series injected voltages by the series converter, whose phase peak magnitudes are 133.6V, 1.2V, and 66.1V on phase-*a*, *b* and *c* respectively; axis-3 shows the compensated three-phase load voltages at PCC and axis-4 represents the dc-link voltage. The load voltage is maintained at 336.4V, 339.2V and 338V on three phases against the reference value of 338V. Figures 6.27 and 6.28 depicts the experimental scope results to justify the simulation results shown in Figure 6.26.

The load voltage at PCC is maintained at 162.8V, 162.3V and 161.9V on phase-*a*, *b* and *c*, which is observed from Figure 6.27(b). The injected series voltages are shown in Figure 6.87(a). During the compensation, the dc-link voltage is maintained at 330V, which is shown in Figure 6.28(b).

6.4.4 Unbalanced Linear Load:

The proposed topology has an application to 3P4W network because of the ability to provide neutral access to single-phase loads. As discussed in the above sections, the fourth leg of the shunt converter provides the neutral point access to the single-phase customer loads.

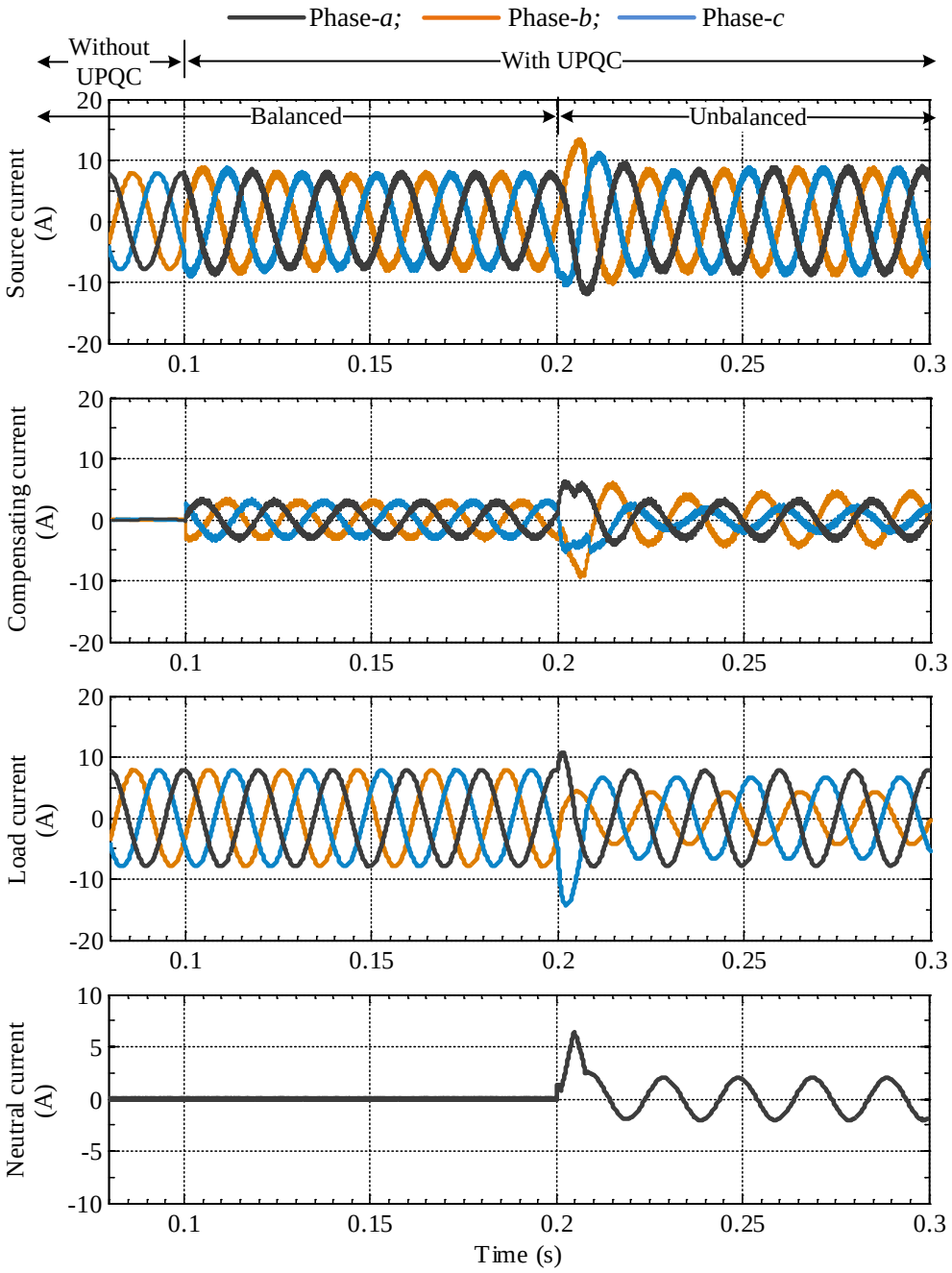


Fig. 6.29: Compensation of source current under unbalanced linear load.

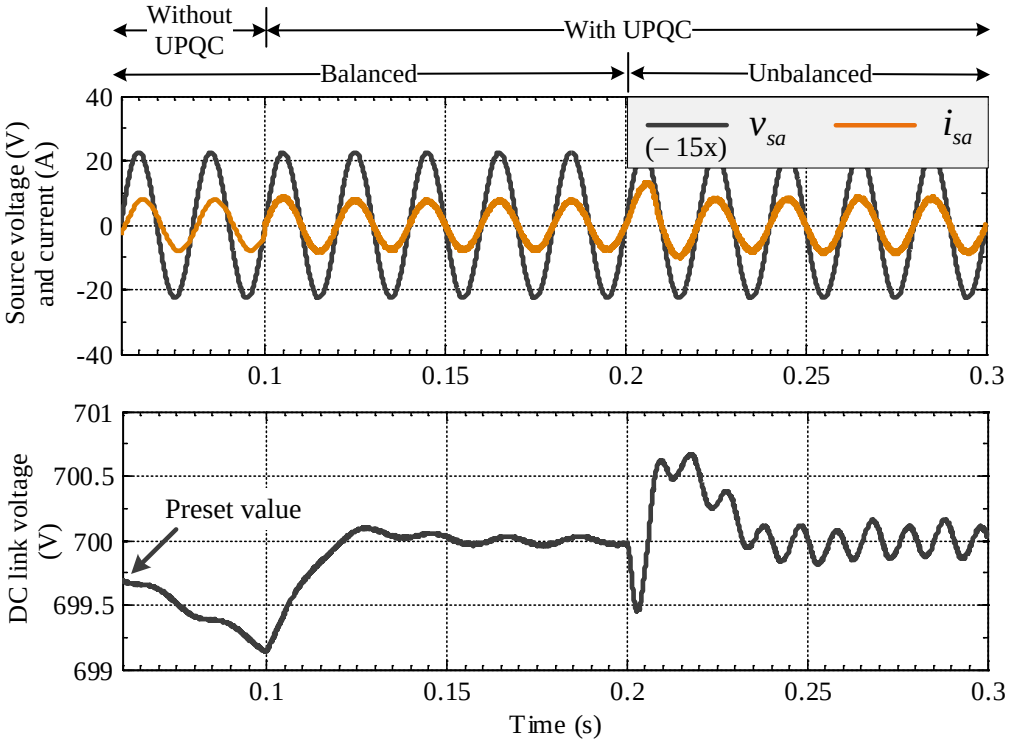


Fig. 6.30: Simulation results showing reactive power compensation under unbalanced linear load.

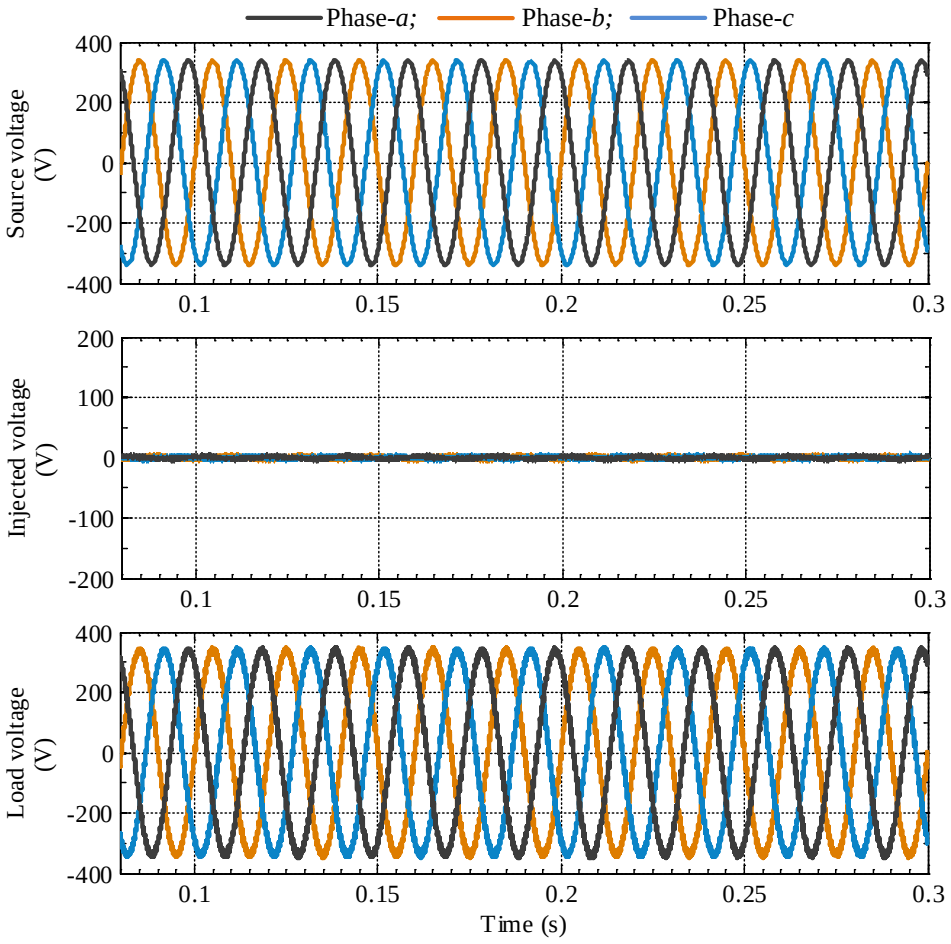


Fig. 6.31: Response of the series converter under unbalanced linear load.

Figure 6.29 shows the simulation results with unbalancing loading condition. In order to study the steady-state and transient performance of the proposed topology, the following events have been assumed to occur in the system for all simulation studies:

- At t =0.1s, the UPQC and its associated control circuit is connected to the system.
- At t =0.2s, an additional load is connected to the system to create unbalancing in the load.

The simulation results are presented below for both voltage and current compensation characteristics. In Figure 6.29, the quantities are shown as follows (from top to bottom): axis-1: three-phase source currents; axis-2: three-phase shunt compensating currents; axis-3: three-phase load currents; axis-4: neutral current. From Figure 6.29, the following observations are made: Before UPQC connected to the system, the source current is sinusoidal because of the linear load and same as that of load current. The shunt compensating current is zero. The magnitude of load current is 5.65A. Since the balanced load is applied at the PCC, the neutral current is zero. When UQPC connected to the system at t =0.1s, shunt converter starts injecting current to compensate the reactive power demanded by the linear load such that the phase of the source current is changed at the instant. The magnitude of source current is 5.71A, which is slightly increased from the previous source current magnitude i.e. 5.65A. The reason can be explained as the additional amount current is drawn by shunt converter to supply the power converter losses. When the unbalancing is created at the system at time t =0.2s, which is observed from axis-3 with the magnitudes of 5.65A, 2.83A, and 4.24A on corresponding phase-*a*, *b*, and *c*; the shunt compensating current is changed to different magnitudes from each other to make source current unaffected. Since the load is unbalanced, the load requires the neutral current, such that the shunt converter provides the path for the neutral current. The magnitude of neutral current is 4.2A. Figures 6.30 shows the phase relation between source voltage (V_{sa}) and current (i_{sa}) and also the dc-link voltage variation. At t =0s, the dc-link voltage is assumed to be at reference value 700V, which is considered as initial value for the simulation block. As there is no controller to maintain the dc-link voltage, it starts decreasing from the pre-set value. From axis-1, it can be observed that the source current is lagging the voltage, which is refers to the reactive power loading condition. At t=0.1s, the UPQC is connected to the system and dc-link voltage starts rising to the reference value and maintained at 700V. The UPQC forces the source current follows the source voltage in-phase relation such that the reactive power required by the load can be compensated by the shunt converter. At t =0.3s, even though the unbalance is created in the load, whereas the source current is maintained in-phase relation with the source voltage, however the small fluctuations are observed in the dc-link voltage.

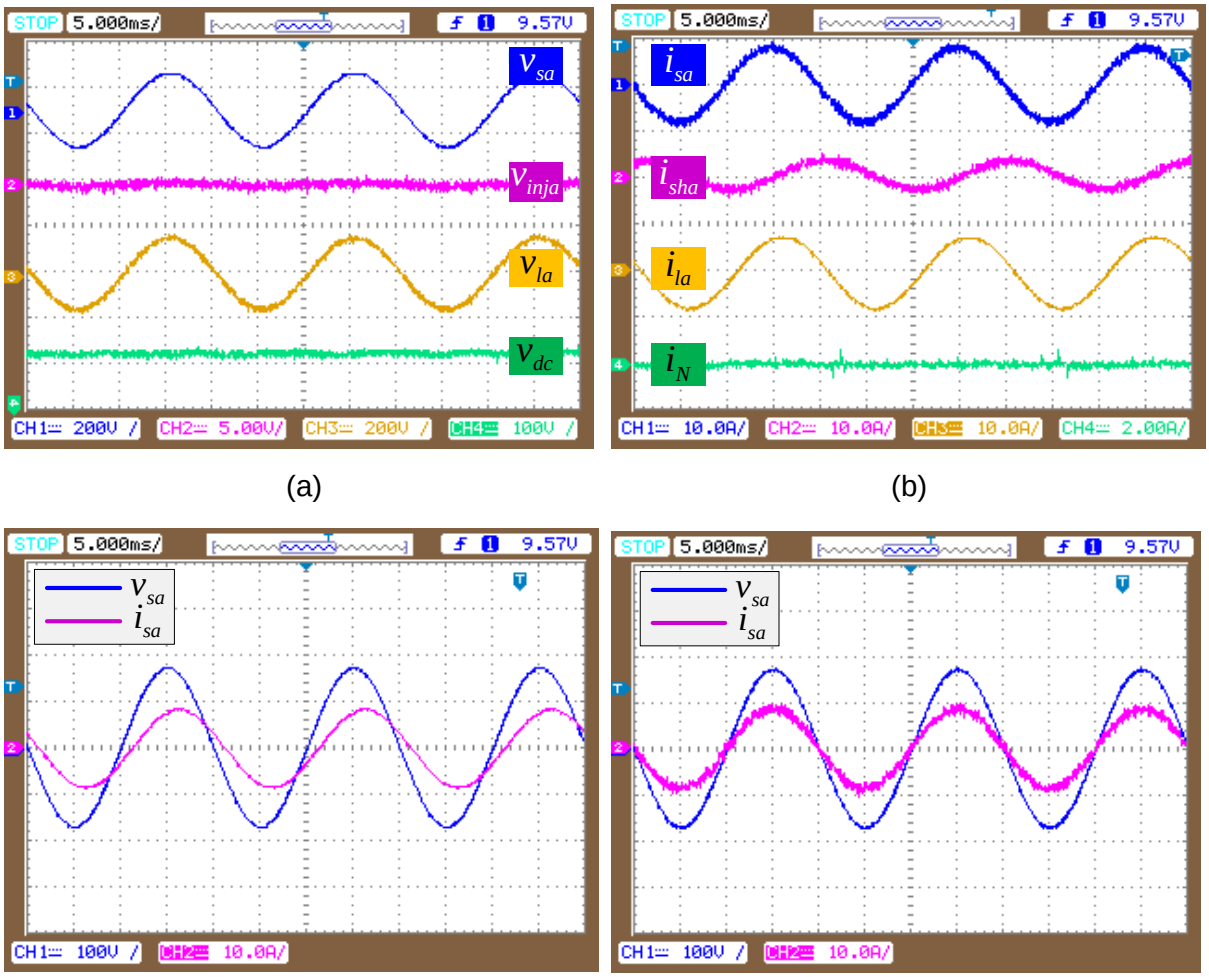


Fig. 6.32: Compensation under balanced linear load (a). Voltage profiles, (b). Current profiles, (c). Phase relation between source voltage and current before compensation, (d). After compensation.

Since no disturbance is created in the source voltage, the series converter remains idle in this case, such that the series compensating voltage is zero, while the load voltage is same as that of source voltage, which is observed from the Figure 6.31.

Figure 6.32 and 6.33 shows the experimental results with linear load by considering both balanced and unbalanced situations. Though the load is balanced on three phases, still UPQC need to compensate for the loading reactive power. Such that series converter behaves idle whereas shunt converter injects the compensating current to bring unity power factor on source. Figure 6.32 (a) shows (from top to bottom) the phase-*a* source voltage, series injected voltage and load voltages of phase-*a*, and dc-link voltage. The load voltage is same as source voltage since the series injected voltage is zero. The dc-link is maintained at 320V. Figure 6.32(b) shows the current compensation characteristics during reactive power compensation, where (from top to bottom) trace-1: source current of phase-*a*, trace-2: shunt compensating current of phase-*a*; trace-3: load current of phase-*a*; trace-4: neutral current. The magnitude of source current is 6.36A, where load current is having 5.8A. The neutral

current is zero in this case of balanced load. From Figure 6.32(b), it can be observed that the phase of source current is shifted left from the load current because of the shunt compensating current injected into the PCC.

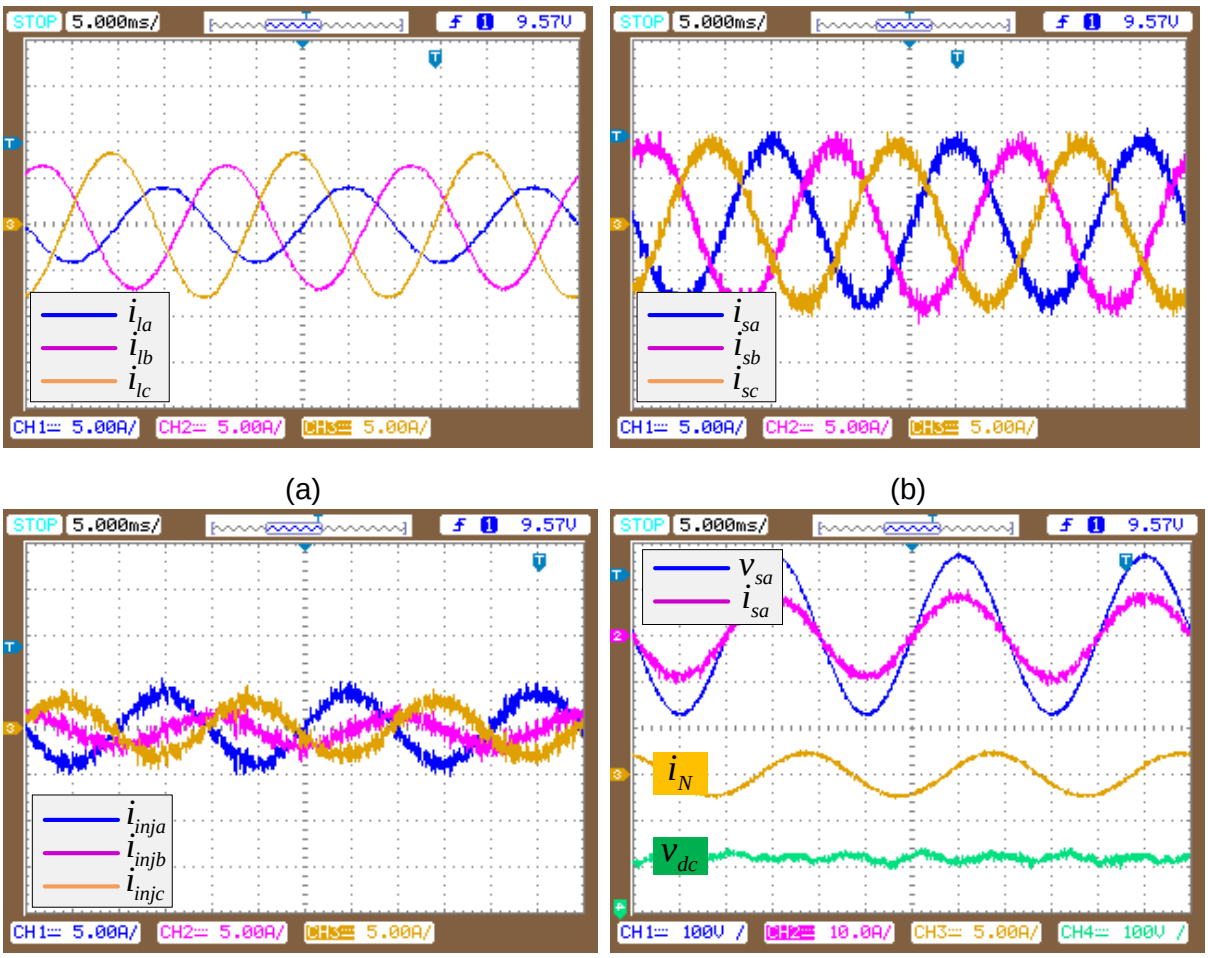


Fig. 6.33: Unbalanced linear load current compensation (a). Three-phase load currents, (b). Three-phase compensated source currents (a). Three-phase shunt compensating currents, (b). Phase relation of source voltage and current; load neutral current and dc-link voltage.

Figure 6.32(c) and (d) shows the phase relation between source voltage and current of phase-*a* before and after compensation respectively. Before compensation source current is lagging the voltage by the angle of 29^0, whereas after compensation source current is in-phase with the source voltage i.e. UPQC is compensated the loading reactive power.

Figure 6.33(a) to (d) shows the experimental results with unbalanced load on PCC. Figure 6.33(a) shows the unbalanced load currents with magnitudes of 2.83A, 4.24A and 5.65A respectively on phase-*a*, *b*, and *c*. Figure 6.33(b) shows the balanced source currents of phase-a, b, and c respectively. The compensating currents of three phases are shown in Figure 6.33(c). Figure 6.33(d) shows the following quantities. From top to bottom, trace-1: source voltage of phase-a, trace-2: source current of phase-*a*, which is aligned to the same ground point with trace-1 on the scope view. This represents that after compensation the source current is in-phase with the source voltage. Trace-3 refers the neutral current required

by the load because of the unbalancing load. Trace-4 refers the dc-link voltage during unbalancing compensation, which is maintained at 315V.

6.4.5 Unbalanced Non-linear Load:

Similar to unbalanced linear load, the performance of the proposed topology is evaluated with unbalanced non-linear load. Figure 6.34 shows the simulation results with unbalancing loading condition. In order to study the steady-state and transient performance of the proposed topology, the following events have been assumed to occur in the system for all simulation studies:

- At t =0.1s, the UPQC and its associated control circuit is connected to the system.
- At t =0.2s, an additional load is connected to the system to create unbalancing in the load.

In Figure 6.34, the quantities are shown as follows (from top to bottom): axis-1: three-phase source currents; axis-2: three-phase shunt compensating currents; axis-3: three-phase load currents; axis-4: neutral current. From Figure 6.34, the following observations are made: Before UPQC connected to the system, the source current is non-sinusoidal because if the non-linear load and same as that of load current. The shunt compensating current is zero. Since the balanced load is applied at the PCC, the neutral current is zero until t =0.2s. When UQPC connected to the system at t =0.1s, shunt converter starts injecting current to compensate the reactive power and also the current harmonics by the non-linear load such that the shape of the source current is changed at the instant into sinusoidal from non-linear. The magnitude of source current is 7.77A, which can be expected to be slightly more than the actual fundamental load current magnitude. The reason can be explained as, the additional amount current is drawn by shunt converter to supply the power converter losses. When the unbalancing is created at the system at time t =0.2s, which is observed from axis-3. The three phases of the load current are distributed with different magnitudes; the shunt compensating current is changed to different magnitudes from each other to make source current unaffected. Since the load is unbalanced, the load requires the neutral current, such that the shunt converter provides the path for the neutral current. This can be observed from the axis-4 of Figure 6.34.

Figures 6.37 shows the phase relation between source voltage (V_{sa}) and current (i_{sa}) and also the dc-link voltage variation. At t =0s, the dc-link voltage is assumed to be at reference value 700V, which is considered as initial value for the simulation block. As there is no controller to maintain the dc-link voltage, it starts decreasing from the pre-set value. From axis-1, it can be observed that the source current is non-sinusoidal and slightly lagging the voltage. At t =0.1s, the UPQC is connected to the system and dc-link voltage starts rising to the reference value and maintained at 700V.

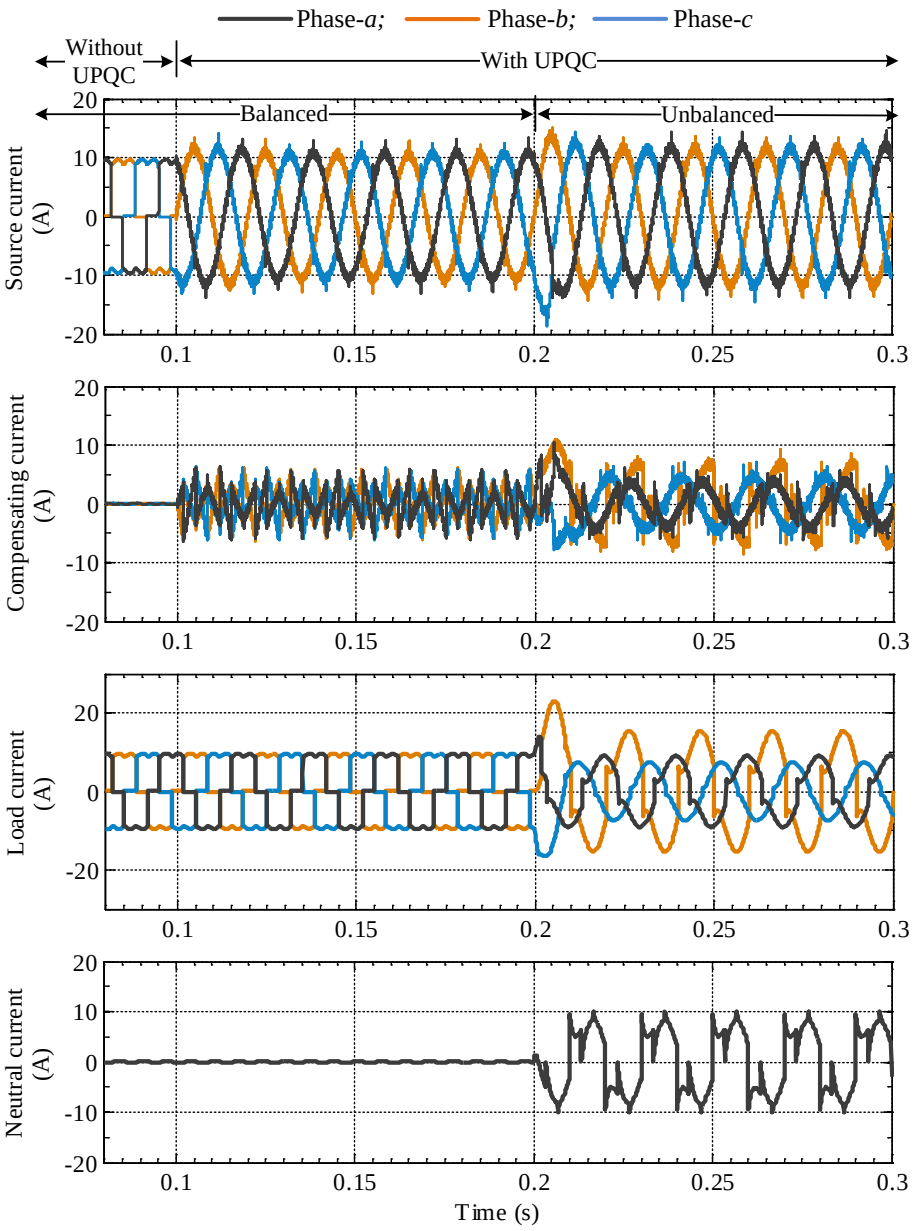
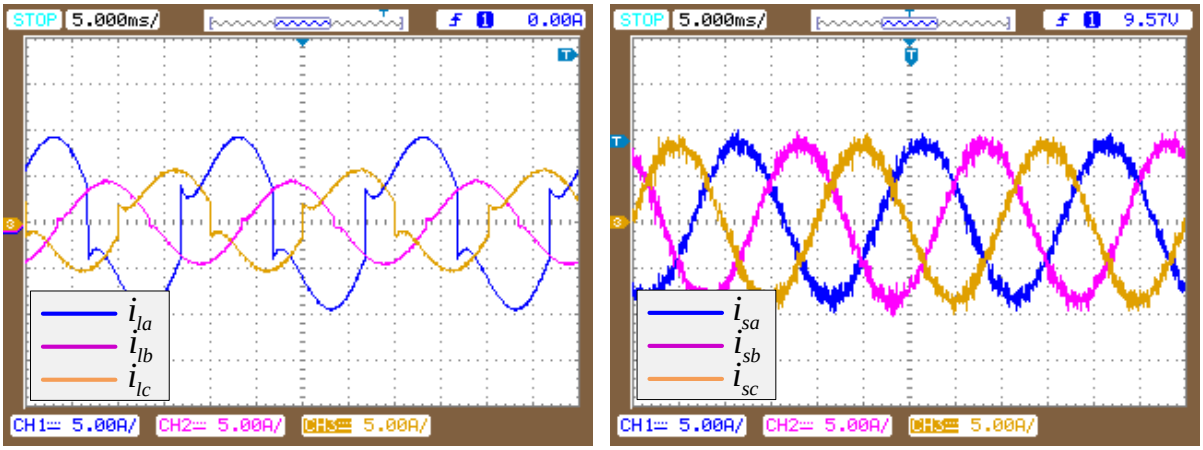
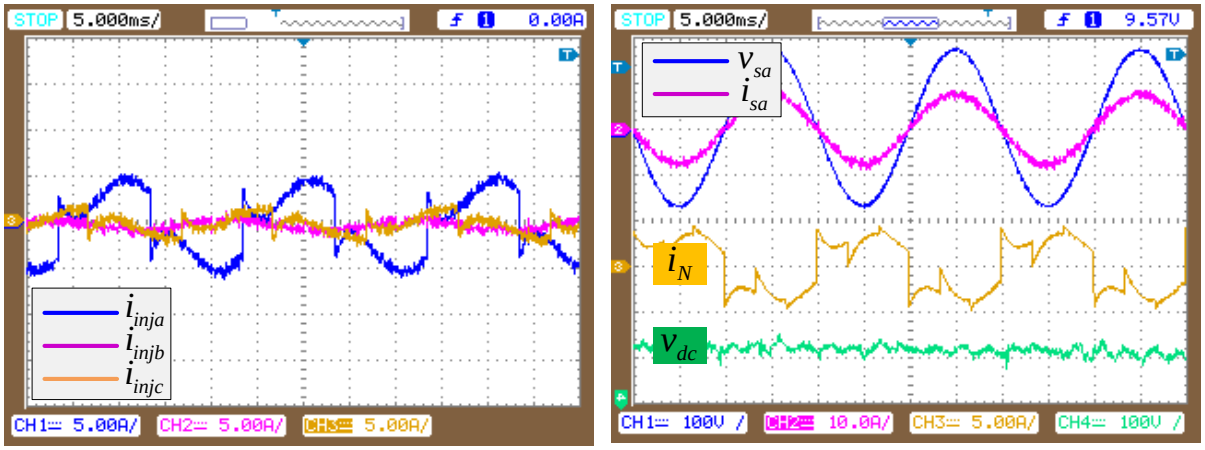


Fig. 6.34: Compensation of source current under unbalanced nonlinear load.



(a) (b)

Fig. 6.35: Unbalanced load current compensation (a). Three-phase load currents, (b). Three-phase compensated source currents.



(a) (b)

Fig. 6.36: Unbalanced nonlinear load current compensation (a). Three-phase load currents, (b). Three-phase compensated source currents.

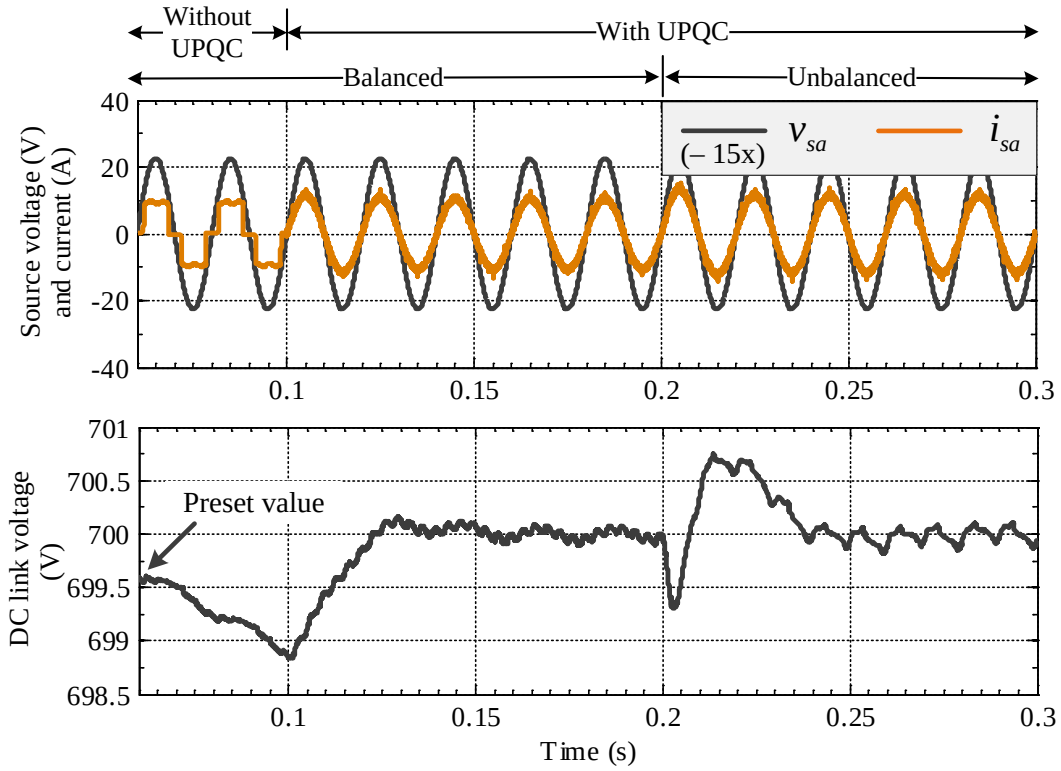


Fig. 6.37: Compensation of source current under unbalanced nonlinear load.

The UPQC forces the source current to be sinusoidal and follows the source voltage in-phase relation. At t =0.2s, even though the unbalance is created in the load, whereas the source current is maintained in-phase relation with the source voltage, however the small fluctuations are observed in the dc-link voltage.

Figure 6.35, 6.36 and 6.38 shows the experimental results with linear load by considering both unbalanced and balanced situations. However, the load is balanced on three phases, still UPQC need to compensate for the current harmonics and loading reactive power. Such that series converter behaves idle whereas shunt converter injects the compensating current to compensate current harmonics entering into the source.

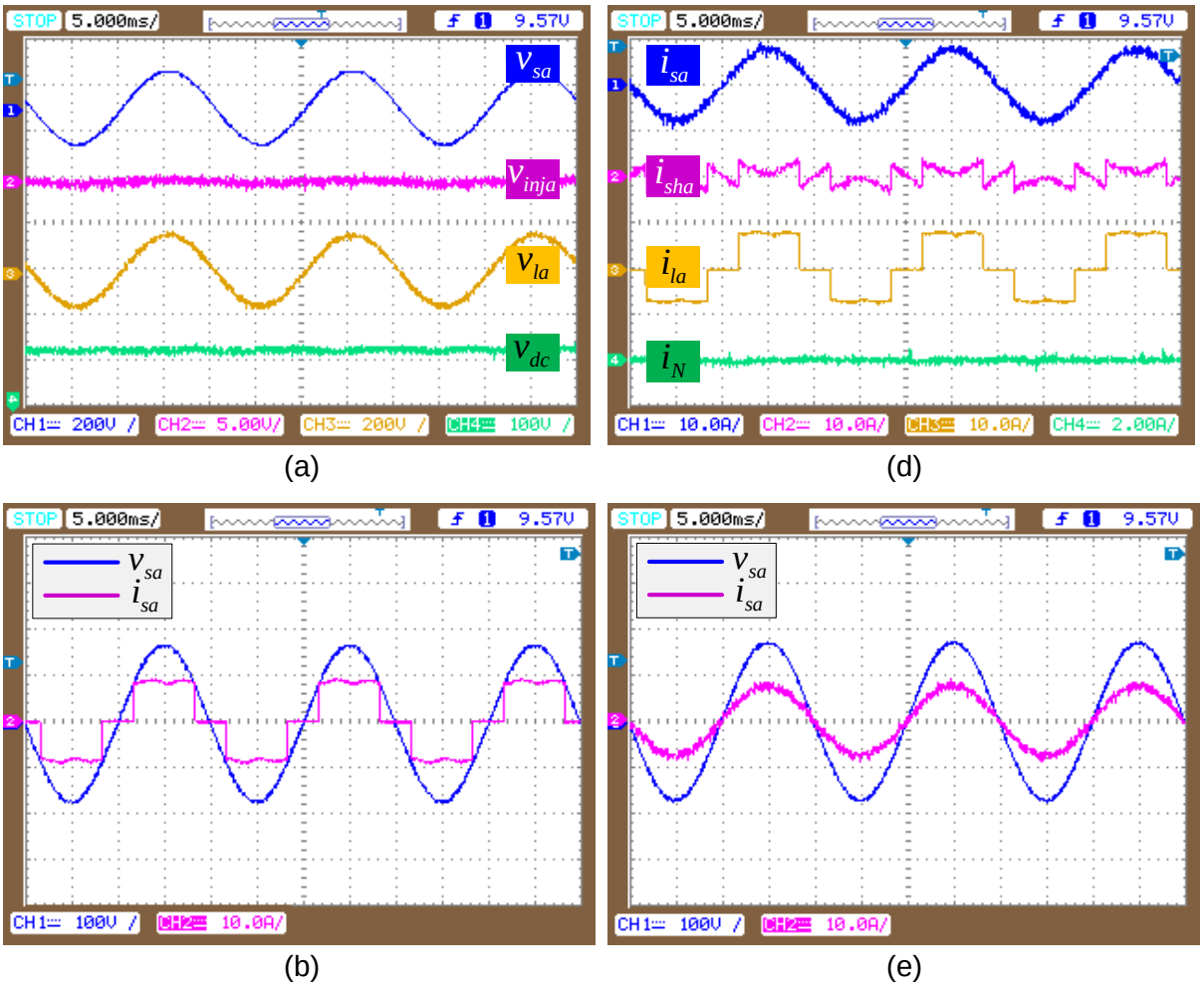


Fig. 6.38: Compensation under balanced nonlinear load (a). Voltage profiles, (b). Current profiles, (c). Phase relation between source voltage and current before compensation, (d). After compensation.

Figure 6.35 and 6.37 shows the experimental results with unbalanced load on PCC. Figure 6.35(a) shows the unbalanced load currents with magnitudes of 4.9A, 3.18A and 3.88A respectively on phase-*a*, *b*, and *c*. Figure 6.35(b) shows the balanced source currents with 5.65A, 5.63A, and 5.64A on phase-*a*, *b*, and *c* respectively. The compensating currents of three phases are shown in Figure 6.37(a). Figure (d) shows the following quantities. From top to bottom, trace-1: source voltage of phase-a, trace-2: source current of phase-*a*, which is aligned to the same ground point with trace-1 on the scope view. This represents that after compensation the source current is in-phase with the source voltage. Trace-3 refers the neutral current required by the load because of the unbalancing load. Trace-4 refers the dc-link voltage during unbalancing compensation, which is maintained at 315V.

Figure 6.38(a) shows (from top to bottom) the phase-*a* source voltage, series injected voltage and load voltages of phase-*a*, and dc-link voltage. The load voltage is same as source voltage since the series injected voltage is zero. The dc-link is maintained at 320V. Figure 6.38(b) shows the current compensation characteristics, where (from top to bottom) trace-1: source current of phase-*a*, trace-2: shunt compensating current of phase-*a*; trace-3:

load current of phase-*a*; trace-4: neutral current. The magnitude of source current is 5.8A, where load current is having 5.2A. The neutral current is zero in this case of balanced load.

Figure 6.38(c) and (d) shows the phase relation between source voltage and current of phase-*a* before and after compensation respectively.

6.4.6 Unbalanced Linear and Non-linear Load:

Similar to above cases, the performance of the proposed topology is tested with the combination of linear and nonlinear and also with unbalanced load. Figure 6.39 shows the simulation results with the combined load of linear and non-linear, which parameters are selected based on the Table 6.1. In Figure 6.39, the quantities are shown as follows (from top to bottom): axis-1: three-phase source currents; axis-2: three-phase shunt compensating currents; axis-3: three-phase load currents; axis-4: neutral current. From Figure 6.39, the following observations are made:

Before UPQC connected to the system, the source current is non-sinusoidal because if the non-linear load and same as that of load current. The shunt compensating current is zero. Since the balanced load is applied at the PCC, the neutral current is zero until t=0.2s. When UQPC connected to the system at t =0.1s, shunt converter starts injecting current to compensate the reactive power and also the current harmonics by the non-linear load such that the shape of the source current is changed at the instant into sinusoidal from non-linear.

When the unbalancing is created at the system at time t =0.2s, which is observed from axis-3. The three phases of the load current are distributed with different magnitudes; the shunt compensating current is changed to different magnitudes from each other to make source current unaffected. Since the load is unbalanced, the load requires the neutral current, such that the shunt converter provides the path for the neutral current. This can be observed from the axis-4 of Figure 6.39.

Figures 6.42 shows the phase relation between source voltage (V_{sa}) and current (i_{sa}) and also the dc-link voltage variation. From axis-1, it can be observed that the source current is non-sinusoidal and lagging the voltage. At t=0.1s, the UPQC is connected to the system and dc-link voltage starts rising to the reference value and maintained at 700V. The UPQC forces the source current to be sinusoidal and follows the source voltage in-phase relation. At t=0.3s, even though the unbalance is created in the load, whereas the source current is maintained in-phase relation with the source voltage, however the small fluctuations are observed in the dc-link voltage.

Figure 6.40, 6.41 and 6.43 shows the experimental results with linear load by considering both unbalanced and balanced situations. However, the load is balanced on three phases, still UPQC need to compensate for the current harmonics and loading reactive power. Such that series converter behaves idle whereas shunt converter injects the compensating current to compensate current harmonics entering into the source.

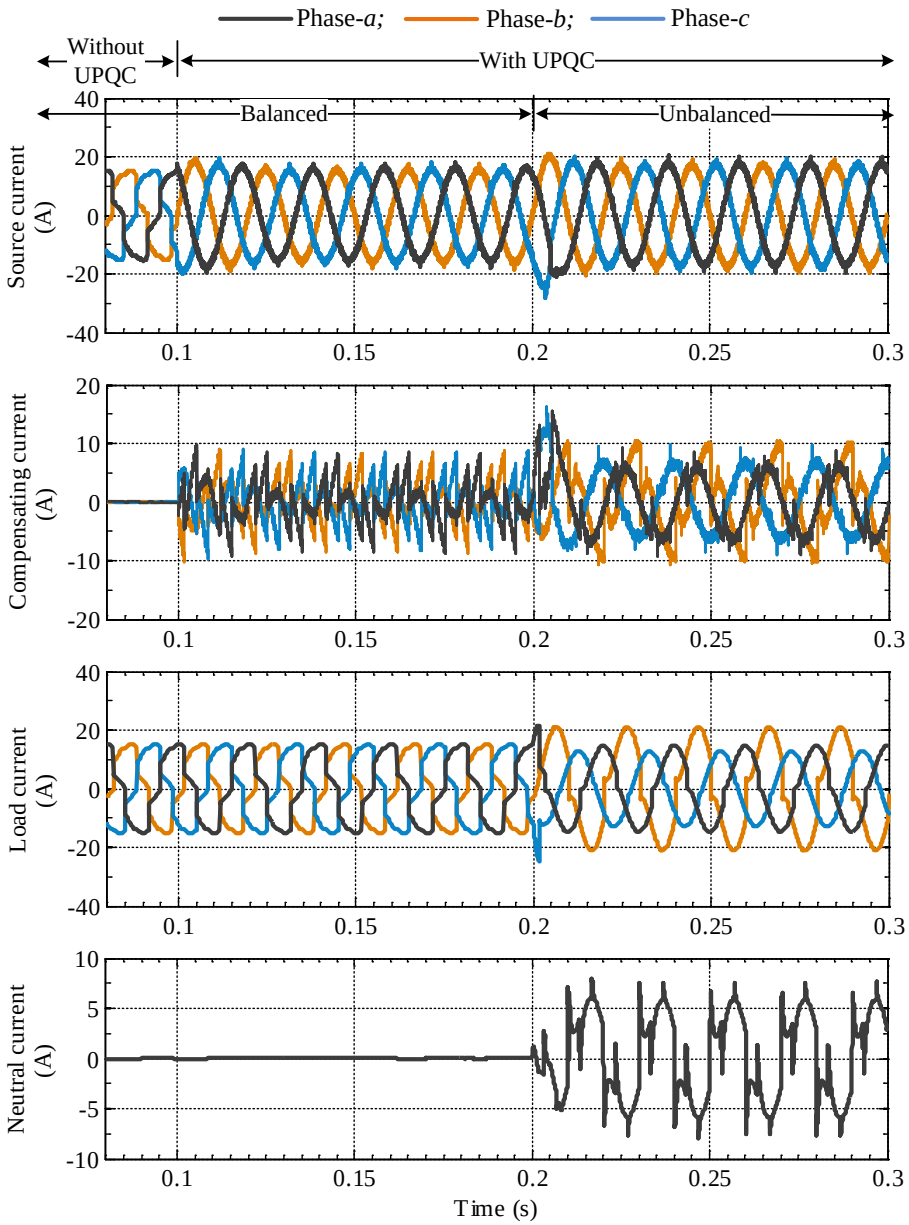
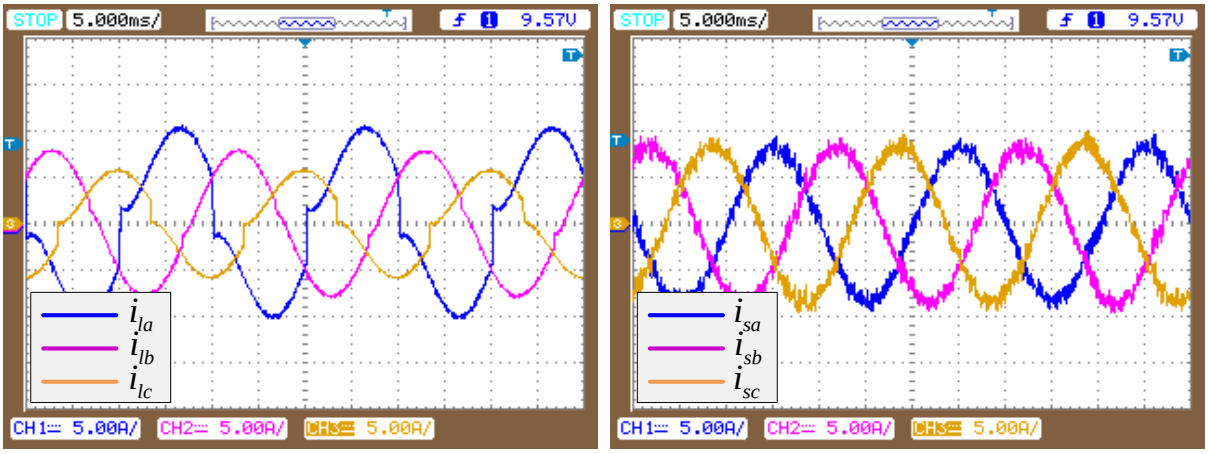
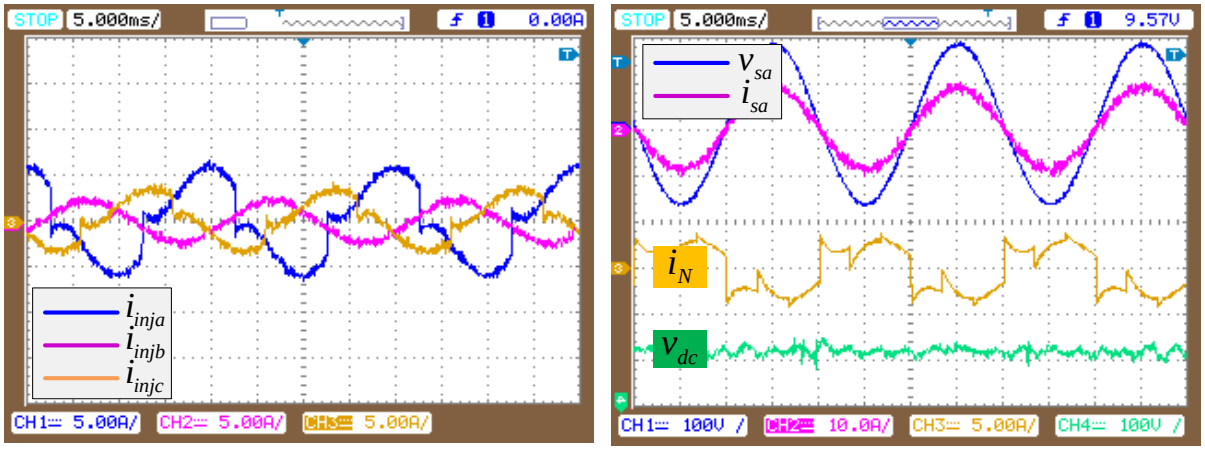


Fig. 6.39: Compensation of source current under unbalanced linear and nonlinear load.



(a) (b)

Fig. 6.40: Unbalanced linear and nonlinear load current compensation (a). Three-phase load currents, (b). Three-phase compensated source currents.



(a) (b)

Fig. 6.41: Unbalanced linear and nonlinear load current compensation (a). Three-phase load currents, (b). Three-phase compensated source currents.

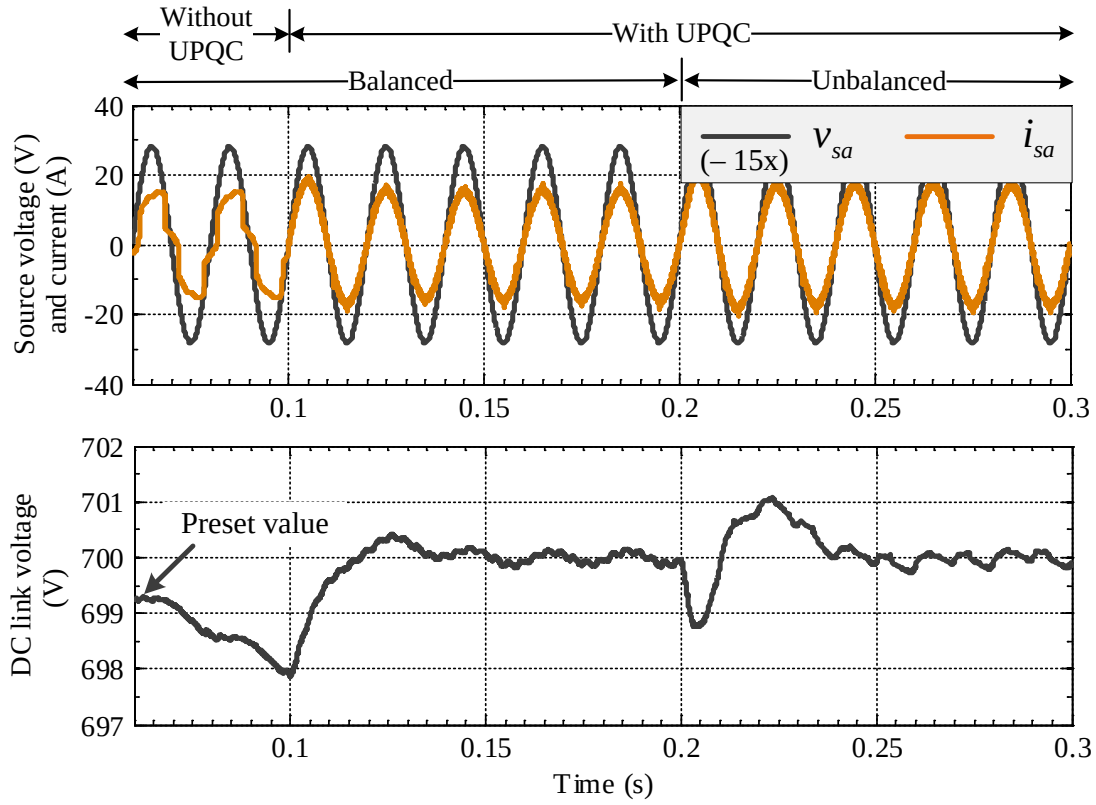


Fig. 6.42: Compensation of source current under unbalanced linear and nonlinear load.

Figure 6.40 and 6.41 shows the experimental results with unbalanced load on PCC. Figure 6.40(a) shows the unbalanced load currents of phase-*a*, *b*, and *c*. Figure 6.40(b) shows the balanced source currents with 5.62A, 5.61A, and 5.63A on phase-*a*, *b*, and *c* respectively. The compensating currents of three phases are shown in Figure 6.41(a). Figure 6.41(b) shows the following quantities. From top to bottom, trace-1: source voltage of phase-a, trace-2: source current of phase-a, which is aligned to the same ground point with trace-1 on the scope view. This represents that after compensation the source current is in-phase with the source voltage. Trace-3 refers the neutral current required by the load because of

the unbalancing load. Trace-4 refers the dc-link voltage during unbalancing compensation, which is maintained at 325V.

Figure 6.43(a) shows the voltage quantities from source, series injected voltage, load voltage and dc-link voltage. The dc-link is maintained at 320V. Figure 6.43(b) shows the current compensation characteristics, where (from top to bottom) trace-1: source current of phase-*a*, trace-2: shunt compensating current of phase-*a*; trace-3: load current of phase-*a*; trace-4: neutral current. The neutral current is zero in this case of balanced load. Figure 6.43(c) and (d) shows the phase relation between source voltage and current of phase-*a* before and after compensation respectively.

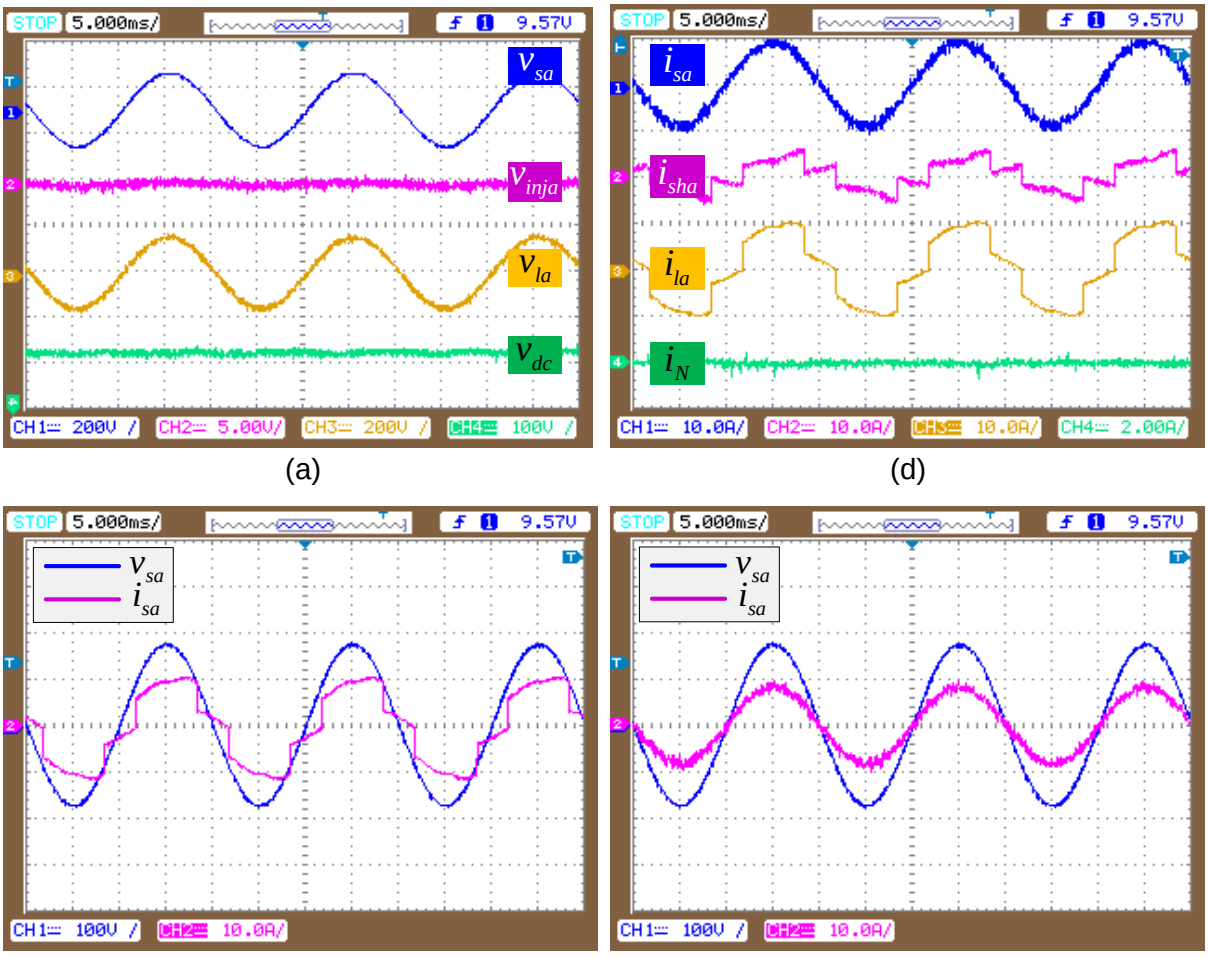


Fig. 6.43: Compensation under balanced linear and nonlinear load (a). Voltage profiles, (b). Current profiles, (c). Phase relation between source voltage and current before compensation, (d). After compensation.

6.5 Conclusion

This chapter proposes a topology intended to reduce the overall size and weight of the UPQC by eliminating the major component i.e. series injection transformer. The proposed topology transformerless series injection UPQC (TLSI-UPQC) is used in 3P4W system. The suitable control strategy is proposed to handle the limitations of TLSI-UPQC of eliminating

distribution transformer neutral connection. To connect single-phase loads in the distribution system, an additional path is provided by the fourth leg of shunt converter and the neutral point at distribution transformer end is controlled by the series converter. The performance of the proposed topology is analysed with MATLAB Simulations and validated through experiment with various type of distortions.

The main conclusions of the presented work and possible future research have been summarised in this chapter.

7.1 Conclusion

In this thesis, digitally controlled UPQC-2L, UPQC-3L and hybrid UPQCs have been proposed to improve the power quality of the load voltage at PCC and source current in 3P3W and 3P4W distribution systems. The major conclusions derived from this work are summarised as follows:

- UPQC is a combination of custom power devices of shunt connected D-STATCOM and series connected DVR, which is realised by using voltage or current source inverter with necessary passive elements and is connected in between source and PCC. The inverter of the D-STATCOM is controlled to draw the compensating current from the ac power source, such that it cancels the reactive and harmonic current contained in the load current. Similarly the inverter of DVR is controlled to inject compensating voltage in series with the supply through series injection transformer to eliminate supply voltage distortions such as voltage sag, swell, unbalance and harmonics. Since voltage source inverter (VSI) is widely used in industrial applications, it has been considered in this thesis. Based on this study, two-level inverter and three-level inverter based UPQC are selected as the power circuit for the UPQC.
- The comparative performance analysis is carried out between both topologies by applying same control technique for various voltage and current distortion problems. Further, experimental studies have also been carried out to investigate the performance of the both topologies. It is concluded that the application of UPQC-3L over UPQC-2L provides the better compensation characteristics in overall all types of voltage and current distortions. However, the size and weight of UPQC-3L is more due to increased number of devices as compared to UPQc-2L. The source current measurements from compensation characteristics shows the increased value as compared to UPQC-2L, which leads to make higher active power losses in UPQC-3L.
- A simplified predictive control is proposed for both the topologies to address the simple control scheme as compared to the complicated model predictive control methods. The Extensive simulation have been used for compensating various voltage distortions with nonlinear load currents are conducted to examine the effectiveness of the UPQC with two-level and three-level structures. The simplified MPC scheme reduces the complicated mathematical computations, such that saving the processing time of the controller board without imposing much burden on it. The MPC controller

is effectively compensates the variety of disturbances in the system with both topologies of UPQC-2L and UPQC-3L. The tracking of predictive signal with reference provides the better response during transient conditions. UPQC-3L over UPQC-2L provides the better compensation characteristics in overall all type of voltage and current distortions same as previous chapter. However, the size of the sampling time period is limited with the processing time of the controller board.

- A hybrid UPQC is introduced with the addition of multi functioning capability to the coupling inductor of the shunt converter to reduce the rating of the overall system. A passive power filter (PPF) is added in the place of coupling inductor, such that the reactive burden on shunt converter is reduced by selecting the lower dc-link voltage. In order to further reduce the dc-link voltage, a phase angle control approach is implemented. A suitable algorithm is proposed to wisely select the optimal dc-link voltage to minimize the VA loading of UPQC. Though the required magnitude of dc-link voltage is less in comparison to traditional UPQC, further reduction is achieved by incorporating PAC approach along with optimal VA loading of hybrid UPQC. Additionally, a generalized algorithm is proposed to evaluate optimal dc-link voltage over a percentage range of voltage sag/swell combinations. Thus, the proposed algorithm gives the best fixed minimum dc-link voltage corresponding to within the range fixed by the algorithm based on the compensation level.
- An alternate solution is proposed to address the fixed compensation by the PPF adopted for UPQC with the inclusion of thyristor controlled reactor (TCR) to the PPF branch. The dc-link voltage is analyzed with variable compensation provided by the thyristor controlled impedance based PPF (TCZ-PPF). The simulation study is carried out to evaluate the effectiveness of the hybrid UPQC for voltage sag compensation with loading reactive power compensation for within compensation range and also above the range offered by TCZ-PPF is analyzed.
- A new topology is proposed to reduce the size and cost of the UPQC by removing the major component i.e. series injection transformer. Series converter is directly connected to the secondary bottom terminals of the distribution transformer. The advantages and challenges of this proposed topology are explored. The topology is employed for 3P4W systems to verify the effectiveness of the transformerless series injection based UPQC (TLSI-UPQC). A control strategy is proposed for TLSI-UPQC to handle the neutral point for the distribution transformer and also to connect single-phase loads on PCC. To connect single-phase loads in the distribution system, an additional path is provided by the fourth leg of shunt converter and the neutral point at distribution transformer end is controlled by the series converter. The performance of the proposed topology is analysed with MATLAB Simulations Further, the

experimental results are validated with simulation results by using the experimental parameters. Therefore, overall results prove that the control algorithm works efficiently with the proposed topology.

7.2 Future Scope of Research

The research work presented in this thesis discloses a number of issues that could be further investigated.

- The conventional PI controller of the UPQC control system can be replaced by soft computing techniques such as fuzzy logic, neural network, and genetic algorithm to further improve the transient response of the system.
- Simplified model predictive control is further need the investigation regards to reduce the total number of sensors.
- The evaluation of dc-link voltage with respect to voltage and current harmonic elimination need to be investigated further to optimize the minimum possible dc-link voltage on the hybrid UPQC based on PPF and also with TCZ-PPF.
- The hybrid UPQC with TCZ-PPF requires further investigation on unbalance compensation with suitable control algorithm to improve the stability of the system.

PUBLICATIONS FROM THE WORK

Journals

[1] **Janardhana Kotturu, Pramod Agarwal and Vinod Khadkikar**, “Optimal DC Link Voltage Control of Hybrid Unified Power Quality Conditioner,” IEEE Transactions on Industrial Electronics (Submitted after 3rd review).

[2] **Janardhana Kotturu, Pramod Agarwal and Vinod Khadkikar**, “Optimal VA Loading of Unified Power Quality Conditioner in Hybrid Structure,” IEEE Transactions on Industrial Electronics (Under review) (1st major review).

[3] **Janardhana Kotturu, Pramod Agarwal,** “Trasnformerless Series Injection based UPQC for Three-Phase Four-Wire System," in Journal of Energies (Accepted).

[4] **Janardhana Kotturu, Pramod Agarwal**, “Comparative Performance Analysis of Two Level and Three Leve based Unified Power Quality Conditioner,” Electric Power Components and Systems, (Under review).

[5] **Janardhana Kotturu, S Kothuru, and Pramod Agarwal**, “Simplified model predictive control of unified power quality conditioner,” in IEEE Transactions on Industrial Applications (Under review).

International conferences

[6] **J. Kotturu and P. Agarwal**, "Performance analysis of unified power quality conditioner based on diode clamped multilevel inverter for 3-phase 3-wire system," 2015 National Power Electronics Conference (NPEC), Mumbai, 2015, pp. 1-5.

[7] **J. Kotturu and P. Agarwal**, "Comparative performance analysis of UPQC using two level and three level inverter for three phase three wire system," 2016 IEEE 6th International Conference on Power Systems (ICPS), New Delhi, 2016, pp. 1-6.

[8] **J. Kotturu, V. Kumar, S. Kothuru and P. Agarwal**, "Implementation of UPQC for three phase three wire system," 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), Delhi, India, 2016, pp. 1-6.

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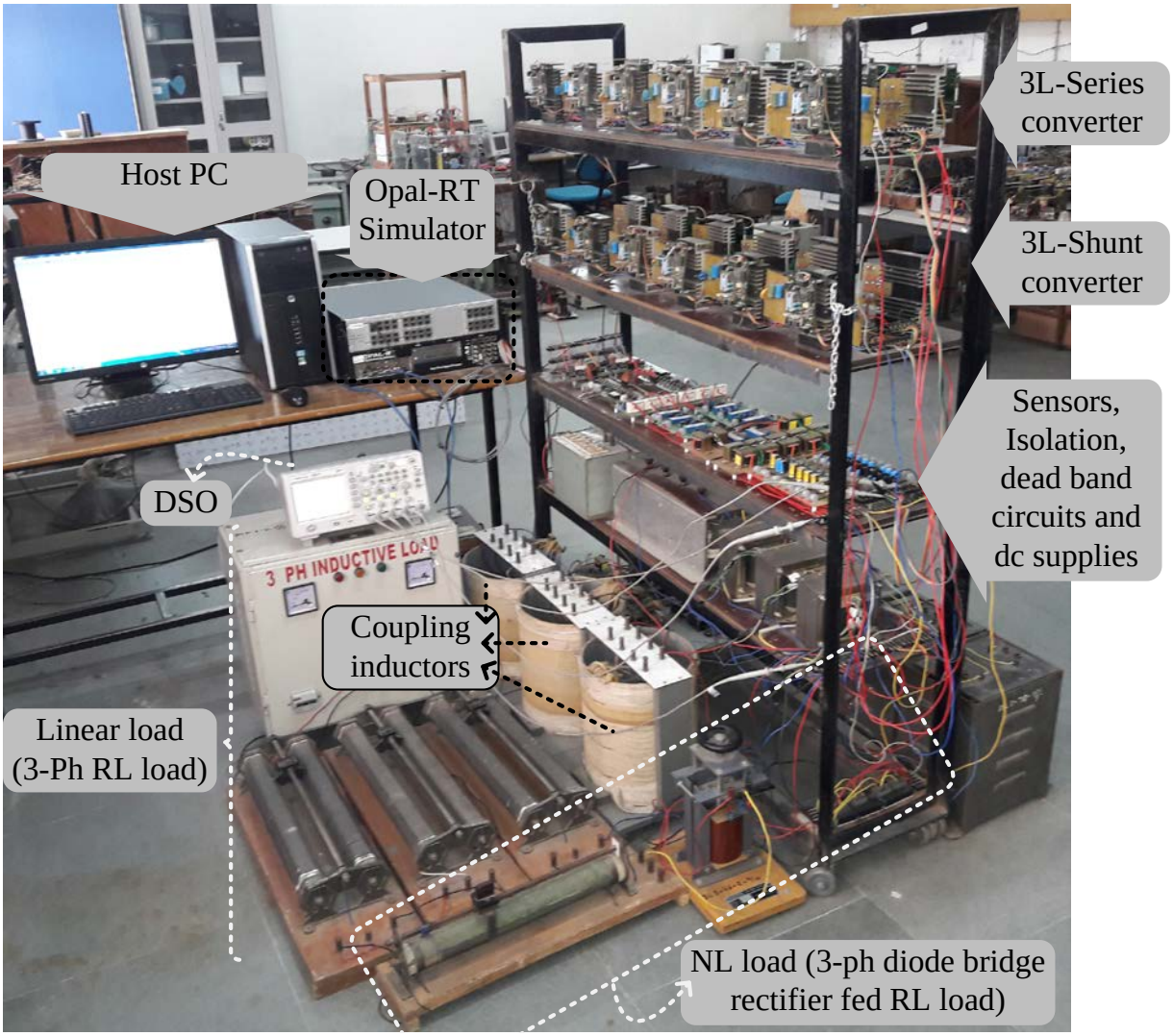

Fig. 1: Experimental setup front view.

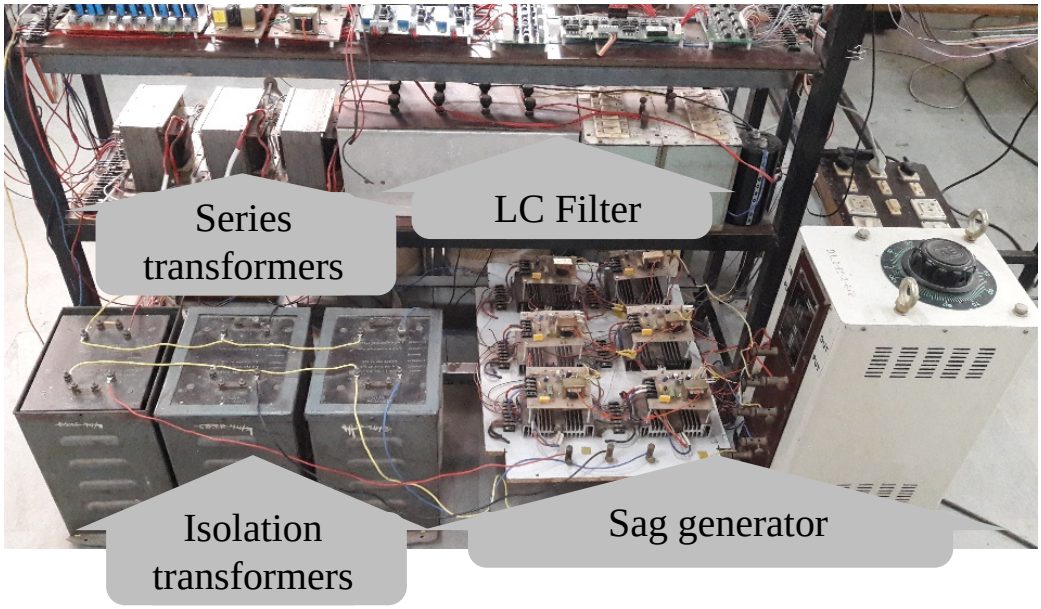

Fig. 2: Experimental setup supply system.

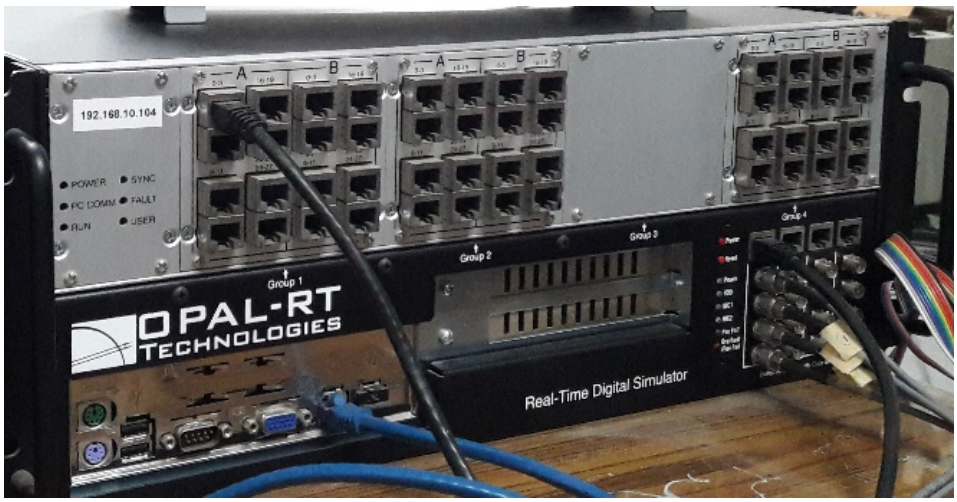

Fig. 3: Opal-RT front panel.

Fig. 4: Opal-RT back panel.

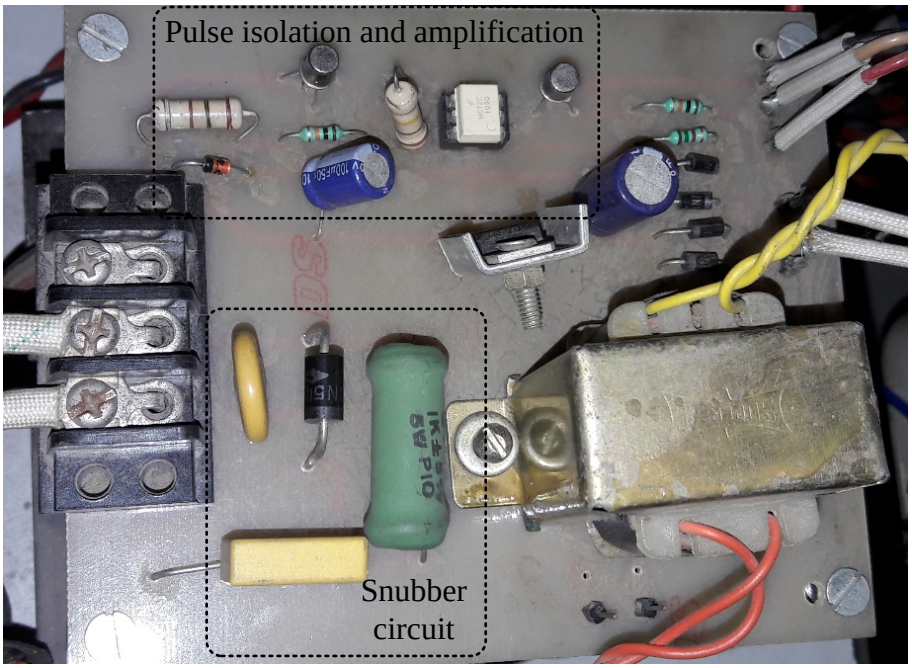

Fig. 5: MOSFET driver circuit.

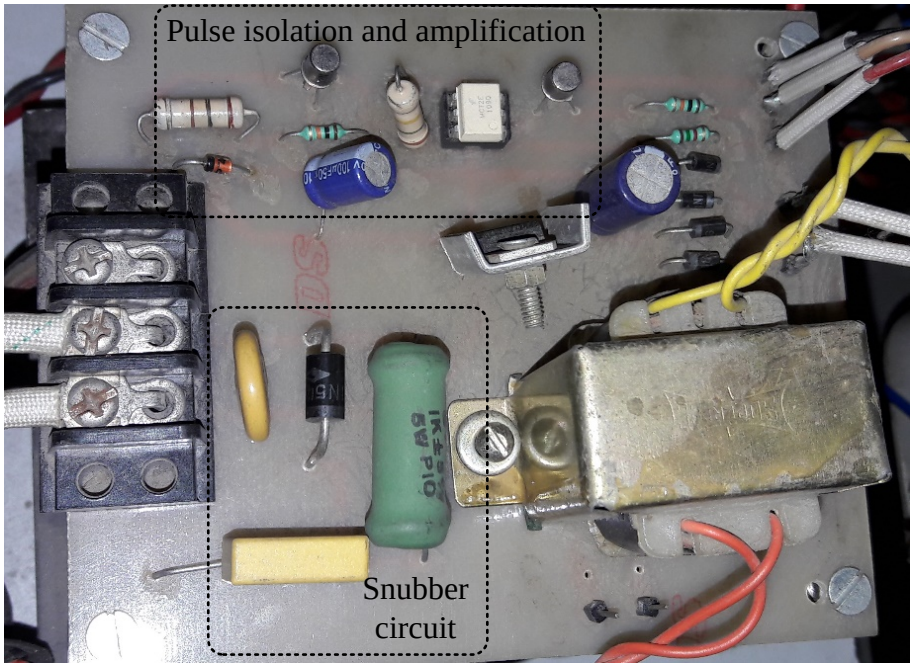

Fig. 6: IGBT driver circuit.

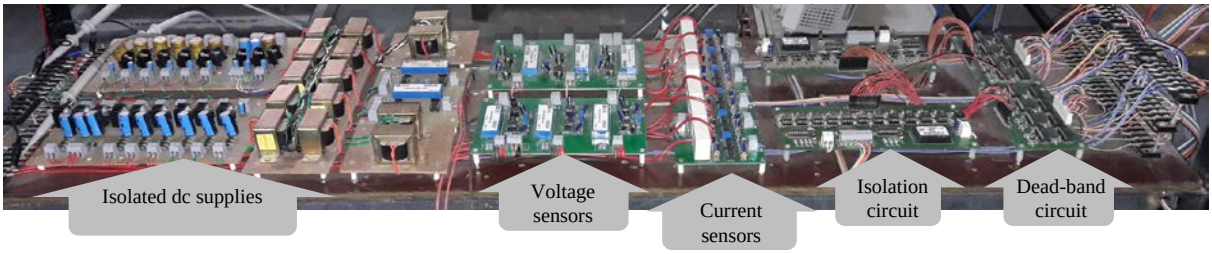

Fig. 7: Control panel board with voltage and current sensors.

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APPENDIX – A: SYSTEM HARDWARE

This appendix presents the design of system hardware and experimentation for prototype model of UPQC topologies. The RT-lab real time digital simulator with Meta controller software interface and Spartan-3 board is used for hardware interface. The proposed control algorithms are implemented in the MATLAB/Simulink and are compiled using the Meta controller interface to generate the switching signals of the different UPQC topologies.

The following prototypes are developed in the laboratory.

- Two-level UPQC (UPQC-2L)
- Three-level UPQC (UPQC-3L)
- Hybrid UPQC with PPF
- Hybrid UPQC with TCZ-PPF
- Transformerless series injection based UPQC (TLSI-UPQC)

For all the topologies mentioned above the power circuits consists IGBTs (IRG4PH40KD) and MOSFETs (SPW47N60C3) as the switching devices. The other hardware components as required for the operation of the experimental set-up such as pulse amplification circuit, dead-band circuit, isolation circuit, voltage and current sensor circuits are designed and developed in the laboratory. The complete schematic diagram for the realisation of UPQC is shown in Figure A.1.

The control algorithm to generate gate pulses for IGBTs is developed in MATLAB/Simulink environment. The RT-Lab is used as a real time HIL (Hardware in loop) controller to implement control algorithm in real time. The RT-Lab compiler converts the MATLAB/Simulink program into a code compatible to Spartan-3 FPGA (field programmable gate array) board The FPGA board generates the control signals which are taken out from digital output port of the RT-Lab. The feedback signals required to generate gate pulses are taken into RT-Lab by using analog input port.

The development of different hardware components as required for the operation of the hardware prototypes are discussed in the upcoming sections.

System Hardware

The developed experimental prototype is comprised of the following basic parts:

1. Measurement circuits
    - DC voltages and Source
    - load currents
2. System software
3. Control hardware
    - IGBT driver circuit

- Buffer (isolation) circuit
- Dead-band circuit

4. Power circuit of inverters

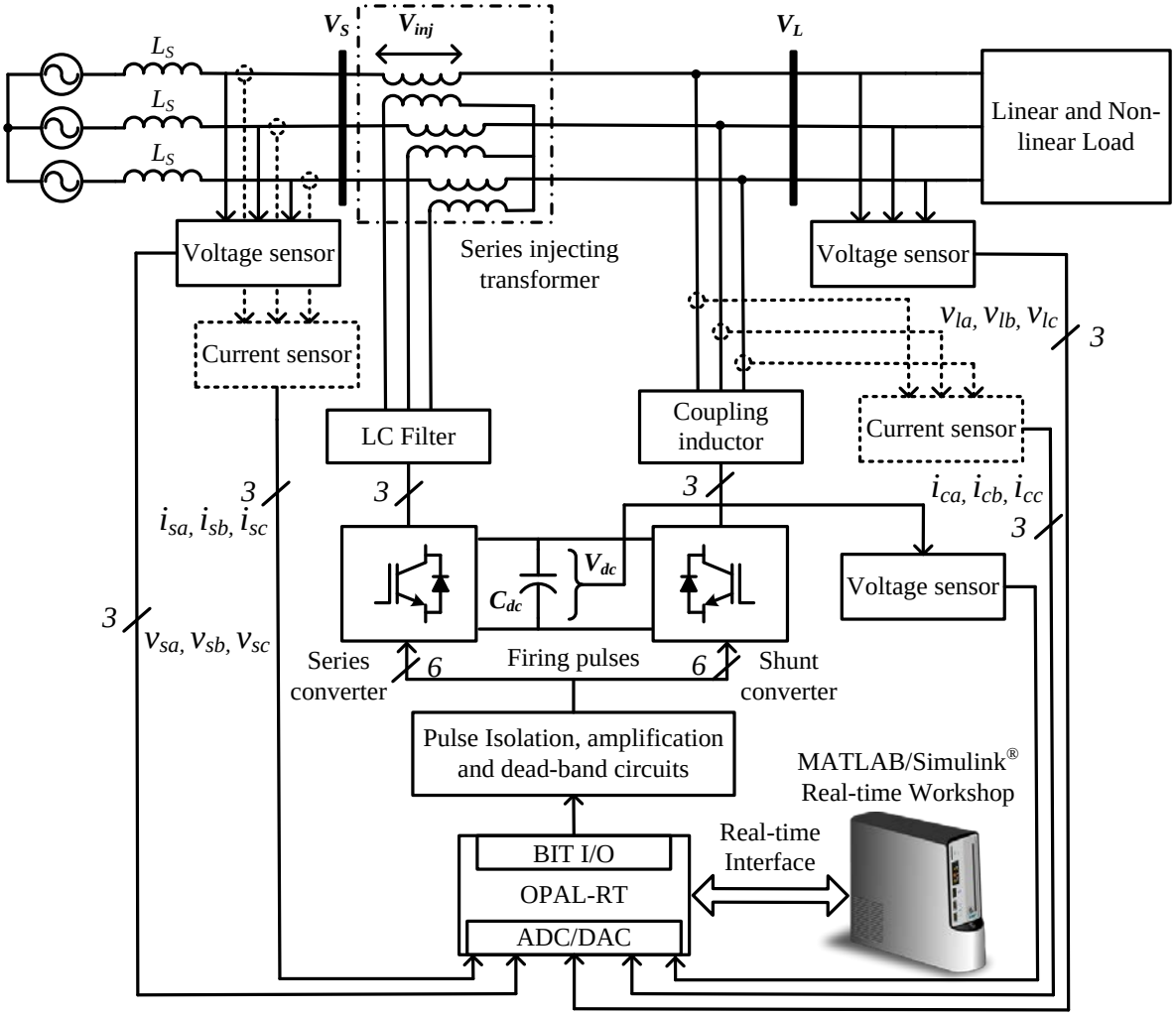


Fig. A.1: Schematic diagram for hardware implementation of UPQC topologies.

Measurement Circuits

For the accurate and reliable operation of a system, measurement of various system parameters and their conditioning is required. The measurement system must fulfil the following requirements:

- High accuracy
- Galvanic isolation with power circuit
- Linearity and fast response
- Ease of installation and operation

With the availability of Hall-effect current sensors and isolation amplifiers, these requirements are fulfilled to a large extent. In order to implement the control algorithm, current and voltage need to be sensed.

Sensing of AC Current

The currents have been sensed using the PCB-mounted Hall-effect current sensors (TELCON HTP50). The HTP50 is a closed loop Hall effect current transformer suitable for measuring currents up to 50 A. The current sensing circuit is shown in Fig. A.1.

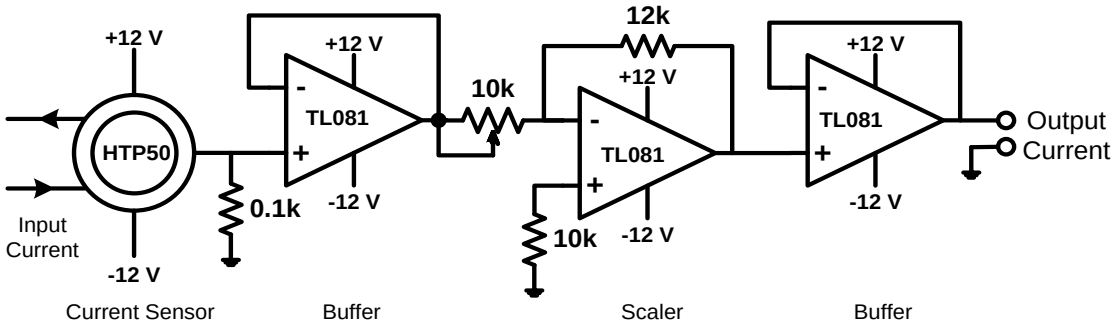


Fig. A.1: Current sensing circuit

This device provides an output current into an external load resistance. These current sensors provide the galvanic isolation between the high voltage power circuit and the low voltage control circuit and require a nominal supply voltage of the range ±12V to ±15V. It has a transformation ratio of 1000:1 and thus, its output is scaled properly to obtain the desired value of measurement.

Sensing of Voltage

The voltages are normally sensed using isolation amplifiers and among them, AD202 is a general purpose, two-port, transformer-coupled isolation amplifier that can be used for measuring both AC and DC voltages.

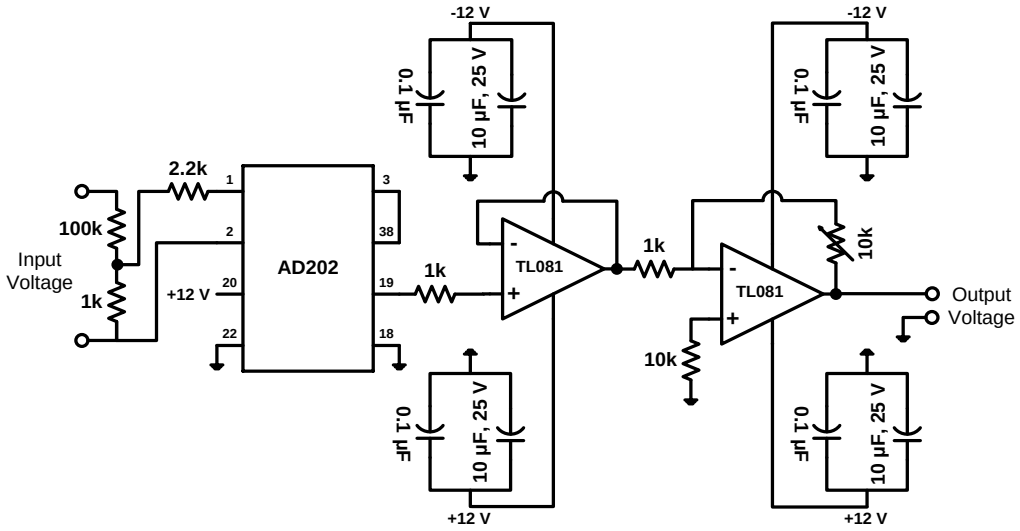


Fig. A.2: AC/DC voltage sensing circuit

The other main features of the AD202 isolation amplifier are:

1. Small physical size
2. High accuracy

3. Low power consumption
4. Wide bandwidth
5. Excellent common-mode performance

This voltage sensor can sense voltages in the range of ±1 kV (peak) and it requires a nominal supply voltage range of ±12V to ±15V. Fig. A.2 shows the circuit diagram for the voltage sensing scheme, which uses AD202 isolation amplifier. The voltage (AC or DC) to be sensed is applied between the terminals 1 and 2 (across a voltage divider comprising of 100 kΩ and 1 kΩ) and the voltage input to the sensor is available at the pins 1 and 2 of AD202 via a resistance of 2.2 kΩ. The isolated sensed voltage is available at the output terminal 19 of AD202. The output of voltage sensor is scaled properly to meet the requirement of the control circuit and is fed to the RT-Lab via its analog input card channel for further processing.

Development of System Software

Historically control software was developed using assembly language. In recent years, industry began to adopt MATLAB/Simulink and Real-Time Workshop (RTW) platform-based method, which provides a more systematic way to develop control software. RT-Lab, from Opal-RT Technologies, is used as real-time hardware-in-loop controller to generate gate pulses for lGBTs in real-time. It is a complete real-time control system based on Intel'" 2.6 GHz processor running at RedHat Linux operating system.

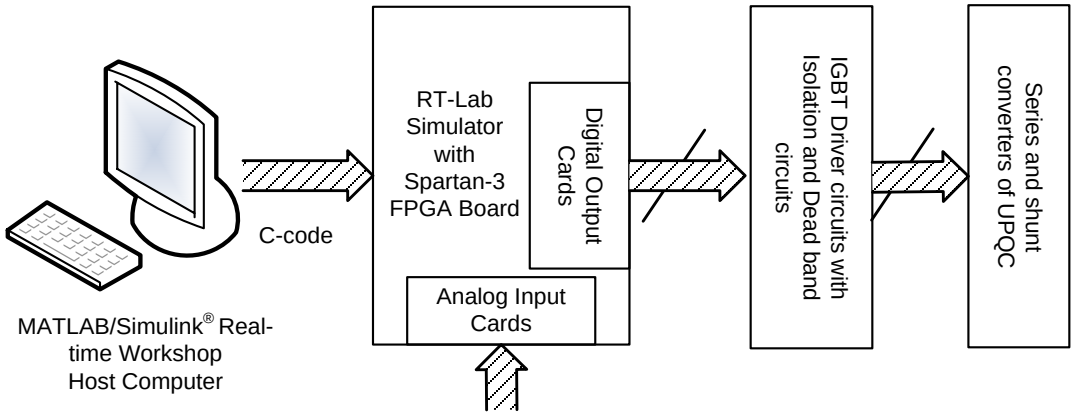


Fig. A.3: RT-Lab and MATLAB real-world interfacing.

The offline control algorithm developed in MATLAB/Simulink platform is converted and transported to the Spartan-3 FPGA board of RT-Lab using Opal-RT's compiler RT-Lab version 10.7. This saves the time and effort twice as there is no need to manually convert the Simulink model into another language such as C and one need not to be concerned about a real-time program frame and I/O function calls, or about implementing and downloading the code onto the RT-Lab. The process is notably very efficient when applied to input/output because RT-Lab provides a set of Simulink block that automatically configure common I/O

functions like analog inputs (feedback signals) and time-stamped digital outputs, with a resolution of 10 nanoseconds. The generated digital output signals are taken out from digital output card and fed to various IGBTs driver circuits via isolation and dead-band circuits. Fig. A.3 shows the schematic diagram of RT-Lab board interfaced with the host computer and the real-world plant (UPQC converter system). The sensed signals from the real-world are fed to the analog input card to use these signals for controlling or monitoring purpose.

Control Hardware

The block diagram of UPQC system connected to linear/nonlinear load is shown in **Error! Reference source not found.**1. The control algorithm is designed and built in MATLAB/Simulink software and the control pulses for IGBTs are generated by Opal-RT real-time simulator using Spartan-3 FPGA board. The optimized C-code of the Simulink model of control algorithm is generated with the help of Meta-controller compiler. The control pulses are generated at digital output card of RT-Lab simulator which are interfaced with the IGBT driver circuits through isolation and dead-band circuits. This ensures the necessary isolation of the RT-Lab controller hardware from the power circuit that is required for its protection. Fig. A.4 shows the basic schematic diagram of interfacing firing pulses from RT-Lab controller hardware board to switching devices of 2L/3L UPQC. In this figure the details of only the phase–*a* series converter of UPQC are shown.

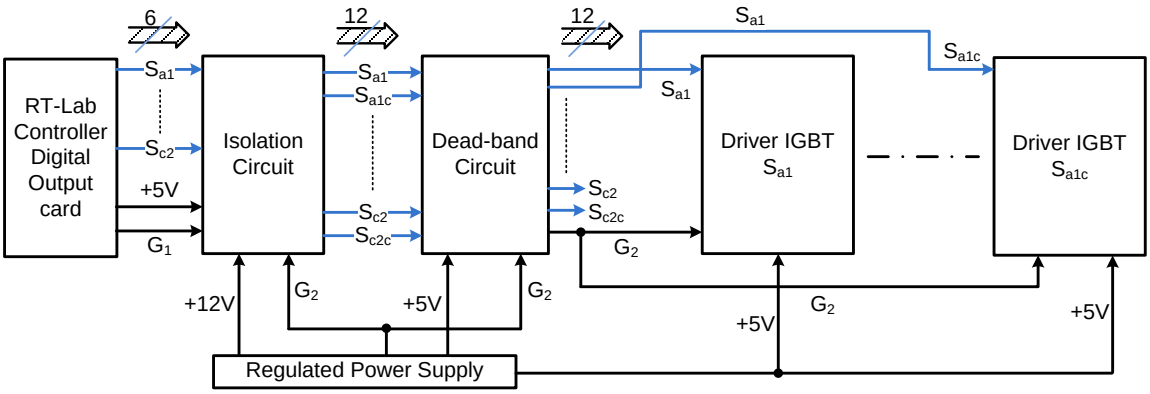


Fig. A.4: Schematic diagram of interfacing firing pulses from RT-Lab controller board to switching devices.

From Fig. A.4, it can be observed that the following hardware circuits are required for interfacing series and shunt converters of UPQC with RT-Lab control hardware.

1. Isolation circuit
2. Dead-band circuit
3. IGBT driver circuits

Isolation Circuit

An isolation circuit board is used for optical isolation of RT-Lab hardware from direct connection with the power circuit. Fig. A.5 shows the circuit diagram of the isolation circuit

between RT-Lab and power devices of a H-bridge cell. Toshiba built opto-coupler chip (6N137) is used for optical isolation.

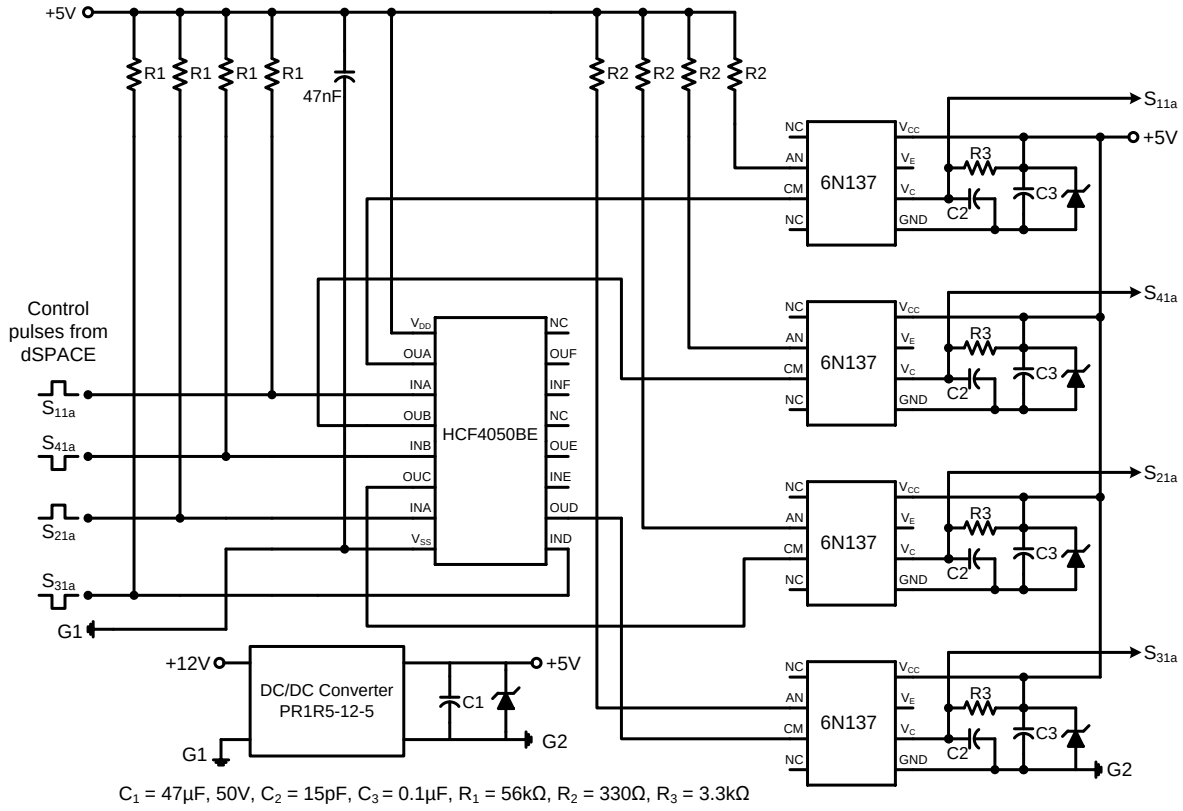


Fig. A.5: Opto-isolation circuit for each switching device.

Dead-band Circuit

A dead-band (dead-time or delay) circuit is employed to provide a delay time (of about 1 µs) between the switching pulses to two complementary devices connected in same leg of an H-bridge cell. This is required to avoid the short circuit of devices in the same leg due to simultaneous conduction. The delay time between switches of the same leg of H-bridge cell is introduced by a *RC* integrator circuit as shown in Fig. A.6.

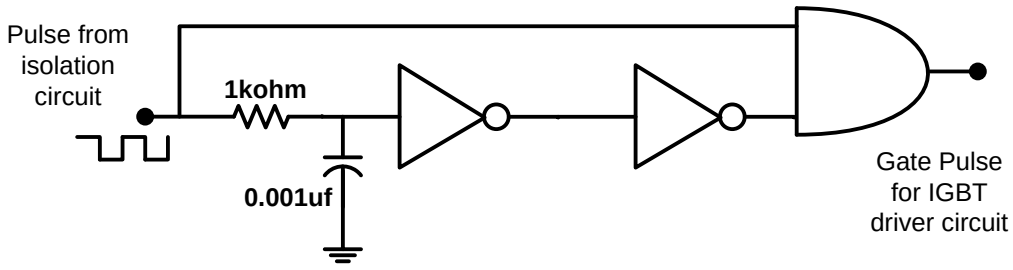


Fig. A.6: Dead-band circuit for each switching device.

An identical dead-band circuit are used for each leg of all H-bridge cells. The different switching signals obtained experimentally for semiconductor devices in the same leg of an H-bridge cell are shown in Fig. A.7 with 1 µs delay. In Fig. A.7 the top and bottom signals are for the switches S_{11a} and S_{41a} respectively.

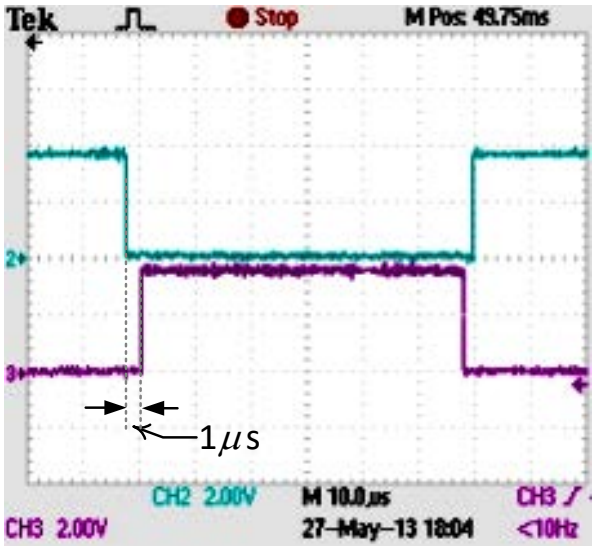


Fig. A.7: Firing signals for the switches S_1 and S'_1 with dead-band circuit.

IGBT Driver Circuits

The IGBT driver circuits are used for pulse amplification and isolation purposes. The IGBT driver circuits not only amplify the pulse signals for driving the devices but also provide an optical isolation. The driver circuit has special features such as fault protection and protection against the under-voltage lockout. HCPL-316J chip from Agilent Technologies is used as an IGBT driver chip. It can drive IGBTs up to 150 A at an applied voltage up tov1200 V. Fig. A.8 shows the circuit diagram of the IGBT driver circuit. During normal operation, V_{out} (pin no. 11) of the HCPL-316J is controlled by either by VLN+ (pin no. 1) or VLN- (pin no. 2), with the IGBT collector-to-emitter voltage being monitored at D_{SAT} (pin no. 14).

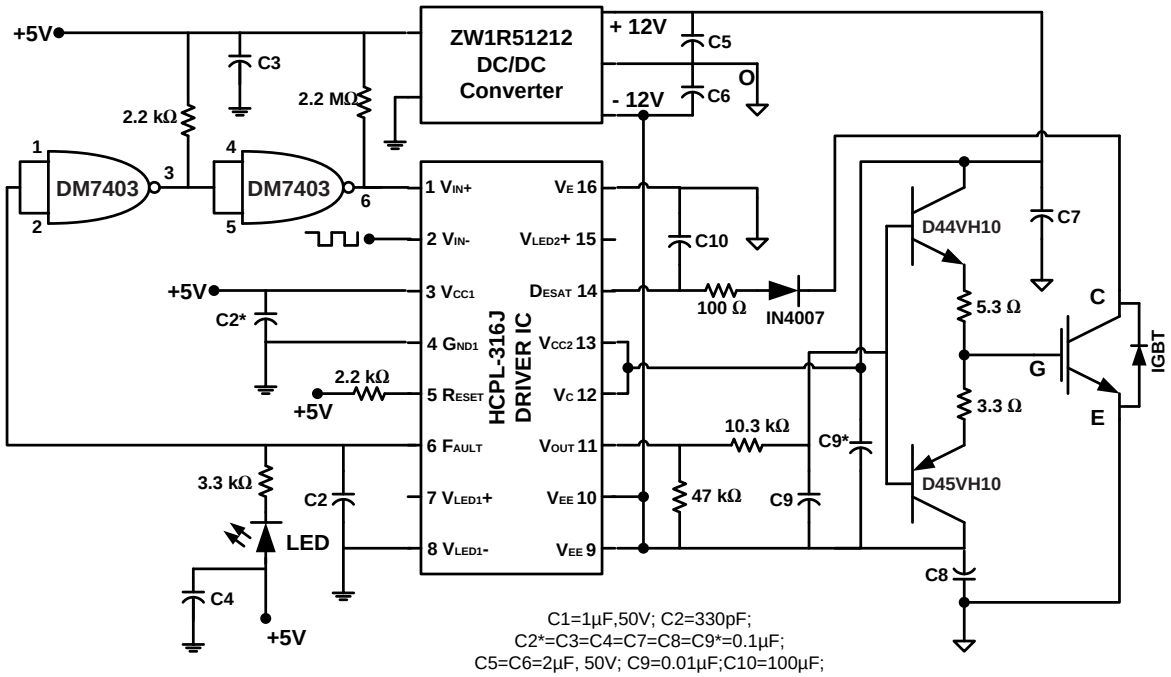


Fig. A.8: IGBT driver circuit.

The FAULT output is high and the RESET input should be held high. (FAULT and RESET are active low signals). When the voltage on the D_{SAT} pin (pin no. 14) exceeds 7 V, while IGBT is on, V_{OUT} on pin no. 11 is slowly brought low in order to “softly” turn-off the IGBT and prevent large induced voltages. Also, an internal feedback channel is activated which brings FAULT output (pin no. 6) low for the purpose of notifying the microcontroller of the fault condition. The FAULT output remains low until RESET is brought low. An LED indication is provided in each driver circuit to indicate the occurrence of a fault, thus prompting a corrective action, either manually or through a microcontroller. The HCPL-316J Under Voltage Lockout (UVLO) feature is designed to prevent the application of insufficient gate voltage to IGBT by forcing the HCPL-316J output low during power-up. IGBTs typically require gate voltages of 15 V to achieve their rated $V_{CE(ON)}$ voltage. At gate voltages below 12 V typically, their on-voltage increases dramatically, especially at higher currents. At very low gate voltages (below 10 V), the IGBT may operate in the linear region and quickly overheat. The UVLO feature causes the output to be clamped whenever insufficient operating supply voltage is applied.

Snubber Circuit

To protect each switching device, a suitably designed snubber circuit is connected across it as shown in Fig. A.9. The snubber comprises of a parallel combination of a resistor and a capacitor connected across a Metal-Oxide Varistor (MOV). All the devices are mounted on heat sinks to ensure proper heat dissipation.

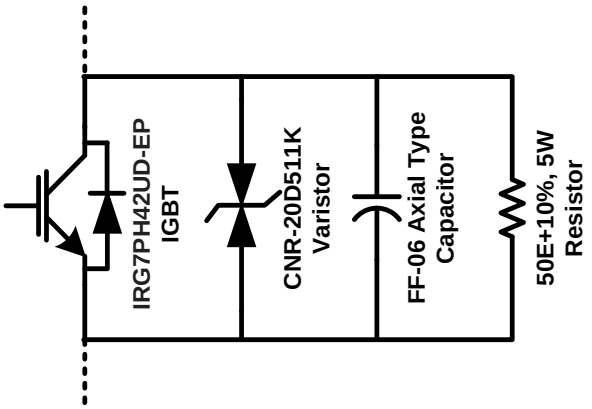
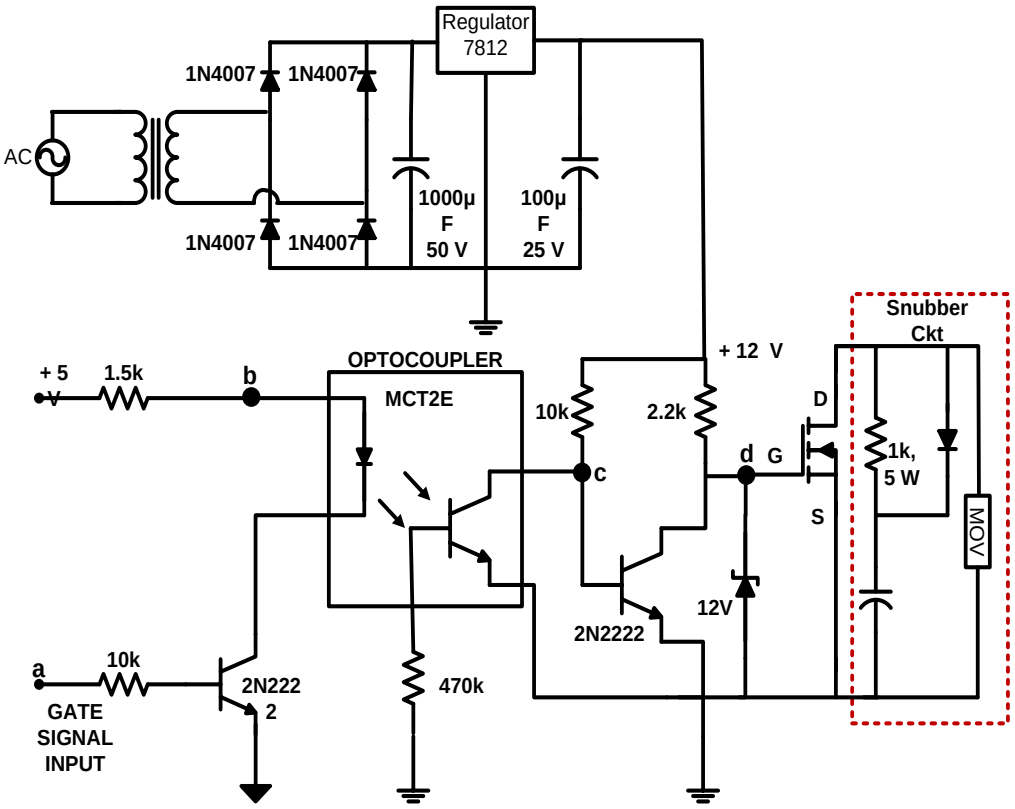


Fig. A.9: Snubber circuit used for switching device

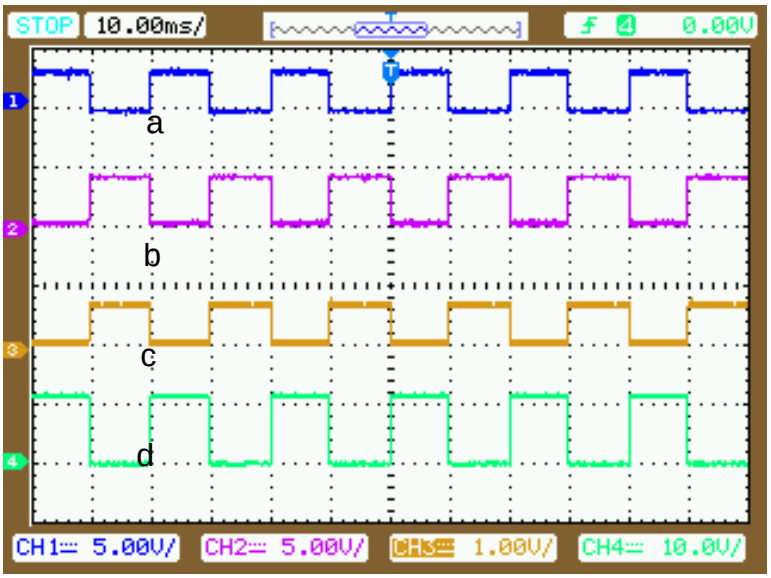
MOSFET Driver Circuits

TheThe MOSFET driver circuits are used for pulse amplification and isolation purposes. The control pulses generated from Opal-RT real-time simulator/dSPACE unit are not efficient to drive the switching devices. Thus, these signals are further amplified by using proper amplifier circuit. Figure A.11 shows a circuit diagram of pulse isolation and amplifier circuit for MOSFET driver circuit. For isolation between power circuit and a control circuit, an opto-coupler (MCT2E) is used. Although common + 5V, regulated DC power supply is used

at the input side of the optocoupler, but individual regulated DC power supplies of +12V are used to connect the output side of optocoupler. In order to test the MOSFET driver, a PWM signal is applied at point ‘a’ of Figure A.11(a) and waveforms at different points (a, b, c and d) are recorded as shown in Figure A.11(b). It is observed that the waveform at point ‘d’ is similar to the PWM signal applied at point ‘a’, but its amplitude is increased to 12V which is used to drive the MOSFET.



(a). MOSFET driver circuit for isolation and amplification



(b). Waveform at different points

Fig. A.11: MOSFET driver circuit and respective wave forms at different positions

APPENDIX – B: PR CONTROLLER

In this appendix, the PR controller, which is used in the Chapter 6 is explained.

In order to achieve correct compensation, proper tracking of the error signal must be achieved. A Proportional-Integral (PI) controller provides proper tracking only if the command signal is a constant waveform. However, If the control signal is time varying, a PI controller cannot guarantee tracking with a steady state error of zero. Increasing the P gain of the PI controller reduces the steady state error, but also amplifies unwanted signals such as switching ripples, electromagnetic interference, and random noise. The reason a PI controller can achieve zero steady state error when the control signal is constant can be seen from the open loop transfer function of the PI controller.

$$G_{PI}(s) = K_P + \frac{K_I}{s} \tag{B.1}$$

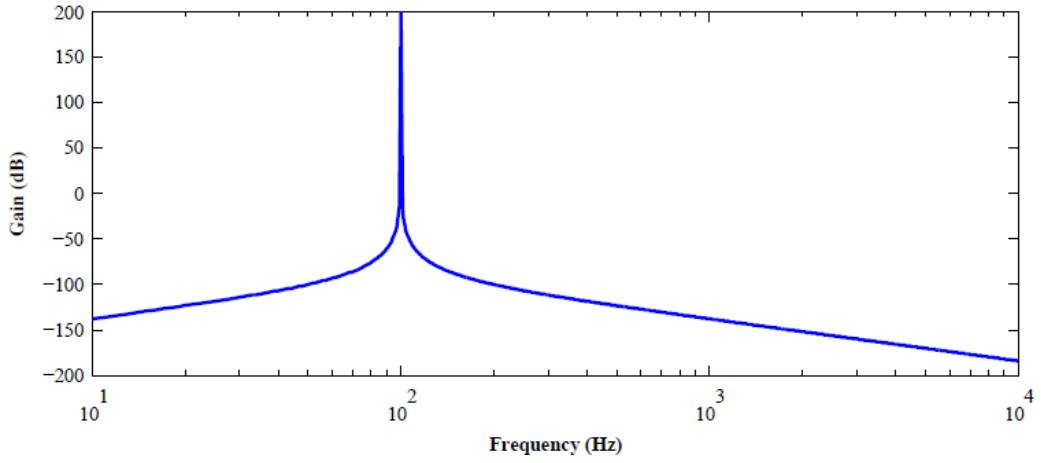


Fig. B1: Bode plot of PR controller tuned at 100 Hz.

As can be seen from the equation above, if the input signal has a frequency of zero (i.e. s=0), meaning that the signal is constant, the gain would go to infinity. In other words, having an infinite gain at a certain frequency ensures perfect tracking at the target frequency. Thus, to have the ability to track time-varying control signals with minimal steady state error, a controller with infinite gain at the control signal's target frequencies must be used. Proportional Resonant (PR) controllers are a type of controller that can achieve this requirement. A PR controller has the following transfer function.

$$G_{PR}(s) = K_P + \frac{K_I s}{s^2 + \omega^2} \tag{B.2}$$

From the transfer function, it can be observed that the gain of the controller goes infinity when $s = j\omega$. This can be also visually shown via bode plot as shown in Figure B1, which illustrates the output gain of a PR controller tuned at 100 Hz given a range of input frequencies. As seen from the figure, at frequencies below or above the target frequency, the gain has negative dB value, meaning that any signals at such frequencies are attenuated.

However, the gain rapidly increases at frequencies approaching 100 Hz, and the gain at 100 Hz is infinity. Consequently, through the use of a PR controller, minimum tracking error can be achieved for an input signal with target frequency ω.