PROTECTION OF DISTRIBUTION SYSTEMS DURING DISTRIBUTED GENERATORS ENVIRONMENT

Ph.D. THESIS

by

YOGESHKUMAR MANIBHAI MAKWANA

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE – 247 667 (INDIA)
OCTOBER, 2018

PROTECTION OF DISTRIBUTION SYSTEMS DURING DISTRIBUTED GENERATORS ENVIRONMENT

A THESIS

Submitted in partial fulfilment of the requirements for the award of the degree

of

DOCTOR OF PHILOSOPHY

in

ELECTRICAL ENGINEERING

by

YOGESHKUMAR MANIBHAI MAKWANA

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE – 247 667 (INDIA)
OCTOBER, 2018

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **"PROTECTION OF DISTRIBUTION SYSTEMS DURING DISTRIBUTED GENERATORS ENVIRONMENT"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electrical Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from July, 2015 to October, 2018 under the supervision of Dr. Bhavesh R. Bhalja, Associate Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institution.

(YOGESHKUMAR MANIBHAI MAKWANA)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

(Bhavesh R. Bhalja)
Supervisor

The Ph. D. Viva-Voce Examination of **Yogeshkumar Manibhai Makwana**, Research Scholar, has been held on .....

Chairman, SRC **Signature of External Examiner**

This is to certify that the student has made all the corrections in the thesis.

Signature of Supervisor **Head of the Department**

Date: _____

Acknowledgement

I would like to thank and express my deep regards and sincere gratitude to my supervisor Dr. Bhavesh R. Bhalja, Associate Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee for his inspiring guidance, constant encouragement, moral support, and keen interest in minute details of the work.

I would like to express my sincere thanks to Ministry of Science and Technology, Department of Science and Technology (DST), Government of India for the necessary financial support under the sanctioned project No. SB/S3/EECE/037/2015. The provided financial assistance has been utilized for the development of the laboratory prototype of proposed work.

I am thankful to Dr. Vinay Pant, Dr. G. B. Kumbhar, E. Fernandiz, Dr. C. P. Gupta, and Dr. Sumit Chaudhary for their invaluable encouragement and assistance in the development of the experimental setup of the proposed work in the laboratory.

I express my sincere thanks to the SRC committee members: Prof. B. Das, Dr. P. Jena, Dr. Dheeraj Khatod and Dr. Sanjay Upadhyay for sparing their valuable time in reviewing and critically examining the work.

My heartfelt gratitude and indebtedness go to all the faculty members of the Department of Electrical Engineering for their encouragement and caring words, providing support and necessary facilities to carry out this research work. I would also like to extend my special thanks to Prof. N. P. Padhy for his moral support & facilities provided in the RTDS laboratory and making my stay pleasant during this period.

I extend my special thanks to Prof. R. P. Maheshwari, Retired Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee for his encouragement and necessary help provided during the initial stage of the work.

I would also like to extend my gratitude to Prof. Ramakrishna Gokaraju, Professor, Electrical & Computer Engineering, College of Engineering, University of Saskatchewan, Saskatoon, Canada for his valuable suggestions and comments in the preparation of research article.

I would like to acknowledge the support and help provided by Shri. Ravindraji, Mr. Manoj and Mr. Vinit, Shri. Amir Ahmadji, Mr. Sanjay during the development and performance of an experimental setup in the laboratory. Further, I would also like to acknowledge the support provided by Mr. Mohan Singh, Mr. Rishabh and Mr. Bhopal Singh in all departmental administrative work.

I express my thank to my co-researchers Mr. Soumitri Jena, Mr. Vishal Gaur, Mr. Ashish Doorwar, Mr. Tejeswar Rao and Mr. Abhishek for sincere support and respect. In addition, a special recognition must be given to Mr. Nawab Alam, Mr. Akhilesh Mathur, Mr. Haresh Shabhadia, Mr. Afroz Alam and Mr. Sukhlal Sisodiya for their valuable suggestions and comments on my progressive work time to time. Further, it would be unfair if I forgot my co-researchers of the RTDS laboratory Mr. Hari Krishna, Mr. Sanjeev Panala, Mr. Krishna Murari, Mr. Chaithanya, Mr. Gururaj, Mr. Shubho, Mr. Phanindra, Mr. Naveen and Mr. Abhishek. They helped me directly or indirectly for the development of the simulation model.

I would like to express my sincere regard to Dr. B. K. Gandhi, QIP Coordinator, QIP Centre, Indian Institute of Technology Roorkee and all the administrative staff member of the QIP Centre for providing their valuable support during my stay at Roorkee.

My heartfelt gratitude and indebtedness to go Mr. S. B. Prajapati & his family, Mr. A. M. Patel & his family, Mr. Dixit Pathak & his family and Mr. Jatinbhai Patel for providing their support and homely environment during my stay at Roorkee.

I am grateful to Dr. U. K. Khare, In-charge Principal, Government Engineering College, Dahod for his continuous support. At the same time, I am very much thankful to my departmental colleague Prof. J. I. Patel, Ms. Minaxi Patel, Mr. Ashesh Shah, Ms. Megha Mahida, Ms. Prafulla Bamaniya, Mr. Pratik, Mr. Hardik Patel and Mr. Rakshit Patel for their very strong support provided during the process of obtaining deputation for higher study.

During my journey of doctoral degree, Mr. Kunal Bhatt and Mr. M. A. Maniar have been continuous motivational force for me to pursue my work. Mr. Bhatt has been with me right from the very first day to the last day of my stay at Roorkee. He helped me a lot in my academic work and domestic need. I am really very much thankful to him for his timely help.

I extend my heartfelt gratitude to my parents with their blessing only I am able to complete my work. I would also like to express my deep regards and gratitude to my brother *Bhavesh* & his wife, my sister & her family, and my family friends for their consistent support and patience.

Word can hardly explain the co-operation and patience of my son *Shubh*. I have no words to express the support of my wife *Hansa* provided me to fulfil my endeavour of doctoral work. She stood by me at every moment and kept me free from almost all the responsibilities of domestic issues during my work. I am also expressing my feeling of love to my newborn baby girl *Vrushali*. I am thankful to God for making her enough strong to survive in very first winter season of her life at Roorkee.

At last but not least, I very much thankful to my God (*Shri Krishna*) for giving me a

chance to live a life at the bank of river *Ganga* and to visit a holy places *Haridwar* and *Rishikesh*.

(**Yogeshkumar M. Makwana**)

Abstract

During the last decade, penetration of Distributed Generators (DGs) in the Distribution Network (DN) has been increased tremendously. In this span, the cost of DG technology has been significantly reduced, which makes it more economical to utilize at the local level to mitigate excessive load demand. The DG plants are utilizing Distributed Energy Resources (DERs) with an inverter or rotating machine based generators. These plants cater the electrical energy demand of the area and, at the same time, distribute the surplus energy to an existing utility grid network. The utilization of DG leads to various advantages such as reduction in land, infrastructure, network integration and losses in power transmission. Along with this, it provides clean, reliable, and environment friendly energy. Besides these advantages, it causes several technical problems such as degradation of power quality, and loss of control over the existing grid network. There are several other issues such as safety of the utility personals/customers, protection of existing network/consumer's property, protection against the abnormal operation of DG, and proper coordination among various protective devices. Among these issues, protection of DN during DG interconnection is the prominent one for the power system engineers.

As the DG is utilized along with the main grid power supply, it is interconnected with the existing utility grid network. In case of fault/abnormal condition, the DG can be disconnected suddenly. This sudden disconnection of DG deviates the voltage magnitude and frequency from its nominal operating range which in turn damage the DN or end user's equipment. Moreover, it is well known that the conventional protection schemes used for the DN are designed for the unidirectional power flow. Nevertheless, an integration of DG into DN changes the direction of current flow in the network. This makes the protective device to mal-operate or in some cases, it may remain unoperated during various abnormal/fault conditions. Therefore, the major protection problems raised by the integration of DG with an existing DN are (i) sudden disconnection of DG widely known as islanding and (ii) loss of existing protection coordination among various protective devices.

In case of an unintentional islanding, the deviation in electrical parameters is large enough to damage the equipment at the consumer end. Hence, in order to protect consumers and DN, the islanding situation must be detected as quickly as possible. According to various standards, the DG in an island network must be disconnected within minimum time (less than 2 s) which can be derived by utilizing anti-islanding protection. This protection can be designed by adopting one of the methods (communication assisted, active, passive and hybrid) of

islanding detection. Though the communication based method gives satisfactory results, it is not economically viable. At the same time, active and hybrid methods require an external signal to be injected into the network which degrades the power quality. Conversely, the passive method is less expensive and easy to implement. However, it suffers from Non-Detection Zone (NDZ) and nuisance trip.

It is well known that all the protective devices such as Overcurrent Relay (OCR), Recloser, and Fuse used in the radial DN are coordinated with each other. However, an integration of DG makes the bi-directional current to flow into the network. Hence, there is a possibility of mis-coordination among the various protective devices. Further, in the presence of DG in the DN, an additional fault current is supplied by the DG. This makes the fuse to blow prior to the recloser for every temporary fault. This is against the fuse saving principle.

Therefore, in order to provide a proper solution to the problems of sudden disconnection of DG and mis-coordination between fuse and recloser in the presence of DG in the DN, the proposed research work has been carried out. The main objective of the thesis is to design and develop effective protection strategies for the islanding detection and to maintain proper coordination between recloser and fuse in the presence of the synchronous based DG in the DN. In the first stage of the research work, an attempt has been made to present an effective and accurate islanding detection scheme. In this attempt, four different islanding detection schemes by acquiring current or voltage signals from the terminal of the target DG have been presented in the proposed work. These schemes have been tested on standard networks/hardware setup by developing a simulation model or laboratory prototype. Further, in order to check the authenticity of the presented technique, a Hardware-In-Loop (HIL) testing has also been carried out. The developed islanding detection techniques have utilized different approaches such as pattern recognition, sequence components, modal components, and auto-correlation.

In a pattern recognition based islanding detection technique, synchronous and inverter based DGs have been utilized which are connected to various buses of the IEEE 34 bus network. A large number of simulation cases of islanding and non-islanding events have been generated on the IEEE 34 bus network in Real Time Digital Simulator (RTDS/RSCAD) environment. Further, in order to proficiently discriminate between islanding situation and non-islanding events, a precise feature selection is very important. Therefore, the process of selection of feature and formation of feature vector has been discussed. In this work, a negative sequence component of currents has been utilized for the formation of the feature vector. Afterwards, the generated test cases have been utilized for the training of the classifier model. Here, in the proposed work, an efficient classifier modal (Relevance Vector Machine (RVM))

has been chosen for its high discrimination efficiency. Furthermore, the minimum percentage (40%) of the acquired data of islanding and non-islanding cases has been utilized for the training of the RVM model. The results obtained in terms of accuracy of the RVM model show that the presented technique efficiently discriminates between islanding situation and non-islanding events. Moreover, it is capable to detect islanding situation with lower or zero mismatch of active/reactive power between load and generation. In addition, it remains immune to the non-islanding events. At the end, the comparative assessment proves that the proposed scheme is superior in discriminating islanding situation with non-islanding events.

Afterwards, sequence component of voltage based islanding detection technique has been presented. In this work, the developed simulation model of IEEE 34 bus network has been utilized for the generation of various islanding and non-islanding test cases. Here, the voltage signals have been acquired from the terminal of the target DG. The sequence components of the voltage signals have been calculated from the phasor values of acquired voltages. These derived sequence components have been further utilized for the derivation of the Islanding Detection Factor (IDF). An effective discrimination between islanding situation and non-islanding events have been carried out by comparing the value of the IDF with the pre-set threshold value. The results obtained in terms of IDF for various islanding and non-islanding situations indicate that the proposed scheme accurately distinguishes islanding situation with the non-islanding event. Further, it senses islanding condition quickly even in case of a very critical islanding situation with perfect power balance condition. Furthermore, during a non-islanding situation, the presented scheme remains stable and does not issue a trip signal. Moreover, the comparison of the proposed scheme with a published scheme establishes its superiority in the detection of islanding situation.

Then, an approach based on modal components of the acquired voltage signals has been presented in the proposed work. In this work, the value of IDF has been calculated by utilizing phasor values of acquired voltages. Further, in order to verify the authenticity of the proposed scheme, a prototype has been developed in the laboratory environment. In this prototype, a synchronous generator based DG has been utilized which is connected to the developed model of the DN. Furthermore, on the prototype, various non-islanding events such as faults with variable fault parameters, switching/starting of capacitor/induction motor and sudden change in load/power factor and islanding situations with different mismatches of active/reactive power have been generated. The experimental results obtained from the prototype show that the presented algorithm is able to detect islanding situation accurately and quickly (within 3 cycles). Moreover, it is capable to detect islanding situation with lower or zero mismatch of active/reactive power between the load and generation. Subsequently, it remains stable during

non-islanding events. At the end, comparative evaluation of the proposed scheme with the existing schemes clearly indicates its superiority in distinguishing islanding situations with non-islanding events.

Thereafter, a new islanding detection approach based on auto-correlation of the acquired voltage signal has been presented. In this work, a Discrimination Factor (DF) which is derived from an Auto-Correlation Factor (ACF) of the voltage signals is utilized for the detection of islanding situation. The value of DF is calculated from the most affected lags of the ACF during various islanding situations and non-islanding events. Discrimination of an islanding situation with the non-islanding events has been achieved by comparing the value DF with the pre-set threshold value. Further, the validation of the presented scheme has been carried out by developing a Hardware-In-Loop laboratory setup. In this setup, a power distribution test network has been virtually developed in RTDS/RSCAD environment which is physically connected to the Digital Signal Processor (DSP) controller. During testing, various islanding and non-islanding cases have been generated on the developed HIL model. The experimental results show that the presented algorithm is able to differentiate between the islanding situation and non-islanding events efficiently. Moreover, the proposed scheme is capable to identify islanding situation even in case of the perfect power balance condition. In addition, it provides better stability against various non-islanding events and hence, it avoids nuisance tripping.

In the second stage of the proposed research work, an effort has been made to provide an effective coordination between recloser and fuse used in the DN along with DG. In this case, an adaptive relaying technique to restore the proper coordination between recloser and fuse based on the network impedance is presented in the proposed work. This technique is based on the positive sequence impedance (Z_{1cal}) of a network seen by the recloser. This impedance varies with respect to the interconnection of DGs in the network. In the presented work, in order to calculate the value of Z_{1cal}, the phasor values of the acquired current and voltage samples have been utilized. Further, the acquisition of the samples of current and voltage signals has been performed at the recloser location. The calculated value of Z_{1cal} is utilized for the derivation of Modification Factor (MF). In the presence of the DG into the DN, the recloser changes its fast operating Time-Current Characteristic (TCC) with respect to the value of MF. The performance of the proposed scheme has been evaluated by modelling an IEEE 34 bus network in RTDS/RSCAD environment. At the same time, appropriateness of the proposed scheme has been verified on a prototype developed in the laboratory. The results obtained from simulations as well as from the laboratory prototype clearly indicate that the proposed scheme restores appropriate coordination between recloser and fuse even in case of

a high as well as a low penetration of DG in the DN.

The presented work is likely to contribute significantly to the area of protection of a radial distribution network in the presence of DG. The different techniques developed will be particularly useful for providing anti-islanding protection and recloser – fuse coordination in the electrical power distribution network. Some suggestions based on observations and simulations in this area are proposed at the end of the thesis for the benefit of potential researchers.

Contents

List of Abbreviations

Acronym		Full Name
3PC	:	Triple Processor Card
AAF	:	Anti-Aliasing Filter
ACF	:	Auto-correlation Factor
ACFV	:	ACF value of Voltage
ADC	:	Analog to Digital
AFD	:	Active Frequency Drift
AI	:	Artificial Intelligence
ANN	:	Artificial Neural Network
APFC	:	Automatic Power Factor Correction
APS	:	Automatic Phase Shift
AVR	:	Automatic Voltage Regulator
C	:	Contactor
CB	:	Circuit Breaker
CCS	:	Code Composer Studio
CHP	:	Combined Heat and Power
CIGRE	:	Council on Large Electric Systems
COROCOF	:	Comparison Of Rate Of Change Of Frequency
CT	:	Current Transformer
CTI	:	Coordination Time Interval
DAC	:	Digital to Analog
DER	:	Distributed Energy Resource
DF	:	Discrimination Factor
DFC	:	Detection Factor Coefficient
DG	:	Distributed Generator
DGCB	:	DG Circuit Breaker
DN	:	Distribution Network
DSO	:	Digital Storage Oscilloscope
DSP	:	Digital Signal Processor
DST	:	Department of Science and Technology
DT	:	Decision Tree
FCDFT	:	Full Cycle Discrete Fourier Transform
FCL	:	Fault Current Limiter
GPS	:	Global Positioning System
GSD	:	Grid Synchronization Device
GTAO	:	Giga-Transceiver Analog Output
GTDI	:	Giga-Transceiver Digital Input
HHT	:	Hilbert-Huang Transform
HIL	:	Hardware-In-Loop
IDF	:	Islanding Detection Factor
IDM	:	Islanding Detection Method
IDMT	:	Inverse Definite Minimum Time
IDT	:	Islanding Detection Technique
IEC	:	International Electrotechnical Commission
IEEE	:	Institution of Electrical and Electronics Engineers

IM-SMS	:	Improved-SMS
LG	:	Line to Ground
LL	:	Line to Line
LLG	:	Double Line to Ground
LLL	:	Triple Line
LLLG	:	Three phases to ground
LOM	:	Loss of Mains
LPF	:	Low Pass Filter
LVRT	:	Low Voltage Ride Through
MCB	:	Miniature Circuit Breaker
MDFT	:	Modified Discrete Fourier Transform
MF	:	Modification Factor
MM	:	Minimum Melting
NDZ	:	Non-Detection Zone
OCR	:	Overcurrent Relay
OF	:	Over frequency
OFP	:	Over Frequency Protection
OFR	:	Over Frequency Relay
OV	:	Over Voltage
PCA	:	Principle Component Analysis
PCC	:	Point of Common Coupling
PF	:	Positive Feedback
pf	:	Power factor
PLCC	:	Power Line Carrier Communication
PMU	:	Phasor Measurement Unit
PR	:	Pattern Recognition
PT	:	Potential Transformer
RF	:	Random Forest
RISC	:	Reduced Instruction Set Code
RNPSCV	:	Ratio of Negative to Positive Sequence Component of Voltage
ROCLNSV	:	Rate of change of inverse hyperbolic secant function
ROCOF	:	Rate of Change of Frequency
ROCOFOP	:	Rate of Change of Frequency Over Power
RPEED	:	Reactive Power Export Error Detection
RTDS/RSCAD	:	Real Time Digital Simulator
RV	:	Relevance Vector
RVM	:	Relevance Vector Machine
SCADA	:	Supervisory Control And Data Acquisition
SCV	:	Superimposed Components of Voltages
SFCL	:	Superconducting Fault Current Limiter
SFS	:	Sandia Frequency Shift
SMS	:	Slip Mode Frequency Shift
SPD	:	Signal Produced by Disconnect
ST	:	S-Transform
StdACFV	:	Standard Deviation of ACF value of Voltage
SV	:	Support Vector
SVM	:	Support Vector Machine
SVS	:	Sandia Voltage Shift

TC	:	Total Clearing
TCC	:	Time-Current Characteristic
TDS	:	Time Dial Setting
THD	:	Total Harmonic Distortion
UCB	:	Utility Circuit Breaker
UF	:	Under Frequency
UFR	:	Under Frequency Relay
UTSP	:	Unified Three-phase Signal Processor
UV	:	Under Voltage
UVP	:	Under Voltage Protection
VCSSCC	:	Voltage and Current Sensor Signal Conditioning Circuit
VS	:	Vector Surge
VSC	:	Voltage Source Converter
VSSCC	:	Voltage Sensor Signal Conditioning Circuit
VU	:	Voltage Unbalance
WT	:	Wavelet Transform

List of Tables

List of Figures

Chapter 1
Introduction

1.1 General Background

During the last decade, penetration of DGs in the distribution network has increased tremendously due to the liberalization policies in the energy market. In this span, the cost of DG technologies has been significantly reduced which makes it more economical to utilize at the local level to cater excessive load demand. Subsequently, during this time, the cost of setting up a new conventional power plant with transmission facilities has also increased exponentially. Hence, it has become more reasonable to develop a small power plant of the order of few kWs/MWs at the location of the load demand rather than a large plant. These plants are utilizing distributed energy resources with an inverter or rotating machine based generators. Such plants are known as DG plants. The DG plant caters the electrical energy demand of the local area, subsequently, the surplus power is distributed over an existing utility grid network. The Council on Large Electric Systems (CIGRE) has defined DG as the plant which is (i) not located at a central location (ii) not dispatching the power centrally (iii) directly connected to the distribution/utility network and (iv) less than 100 MW in capacity/size. The utilization of DG leads to several other advantages such as reduction in land, infrastructure, complex network integration, and power transmission losses. At the same time, the DG technology plays a vital role in the electrical power generation by providing clean, reliable and environment friendly electrical energy [1]–[5].

1.2 Benefits and types of DG

The DG offers various benefits which are listed below:

- It has a low capital cost due to its small size.
- Generally, it is located at the consumer end.
- It delivers power at a higher efficiency as compared to a large system.
- It requires less space and infrastructure as compared to a large system.
- It provides power to the local area and hence, reduces pressure on transmission and distribution network.
- It can be made up of renewable and non-renewable types of energy sources. Therefore, the pollutant emission production will be very less [6].
- It increases system reliability by providing backup or standby power.

Mostly, the DG plant is of small size that includes both conventional and non-conventional types of energy sources. Based on these resources, the developed DG plants are as under:

- Small hydro plant.
- Microturbines plants that run on high energy fossil fuel such as oil, natural gas, propane, and diesel.
- Solar energy based plant.
- Wind energy based plant or Windfarm.
- Biomass-based plant.
- Fuel cell based plant.

The above mentioned plants are utilizing electrical power generation technology based on either the rotating machine or the inverter. These plants can also be categorized with respect to their capacity/size. Table 1.1 shows the capacity wise DG classification of the plants.

Table 1.1 Type of plant along with its capacity [2], [3].

Type of plant	Capacity of Plant
Micro	1 W to 5 kW
Small	5 kW to 5 MW
Medium	5 MW to 50 MW
Large	50 MW to 300 MW

It is to be noted from Table 1.1 that the DG capacity is ranging from 1W to 300 MW. Accordingly, the DG plant size is also ranging from Micro plant to Large plant. Further, in order to supply excess power to the utility grid network, the plant DGs are connected to the main grid supply. Different energy resources are utilized to produce electrical energy. Table 1.2 shows the maximum capacity of DG plants with renewable and non-renewable energy resources. According to the load demand of the area and availability of the energy source, the capacity, and type of the plant is decided. It is to be noted from Table 1.2 that the PV array plant offers the minimum capacity of power generation whereas, the maximum power can be generated with combined cycle plant.

Along with the mitigation of local energy demand, the use of DG directly or indirectly offers several other advantages which are listed below:

- Its setup time is short.
- Its installation and running cost is less.
- It helps in reduction of the greenhouse effect.

- It has lower transmission losses.
- Its voltage profile is almost constant.
- It improves the reliability of supply.

Table 1.2 Maximum capacity of DG plants for renewable/non-renewable energy sources [3].

Source of Energy based Power generation	Capacity of plant (MW)
Non-renewable Energy based plant	
• Combined Cycle Turbine	35 to 400
• IC Engines	0.005 to 10
• Micro Turbine	0.035 to 1
Renewable Energy based plant	
• Micro Hydro Plant	0.025 to 1
• Small Hydro Plant	1 to 100
• Wind Turbine Power Plant	200×10^{-6} to 3
• PV array (Solar Power Plant)	20×10^{-6} to 0.100
• Solar Thermal Power Plant	1 to 80
• Biomass Power Generation	0.100 to 20
• Fuel Cell	0.200 to 5
• Geothermal Power Generation	5 to 100
• Ocean Energy	0.100 to 1
• Battery Storage	0.500 to 5

1.3 Applications of DG and its associated issues

1.3.1 Applications of DG

Generally, the DG is interconnected with the secondary distribution voltage level. According to the type and duration of load demand, the applications of DG are given below:

1. *Stand by DG:* In this type of application, DGs are used as a standby supply for the load like a hospital, process industries, etc., during the main grid outage.
2. *Standalone DG:* In this case, DGs are used as the main source of electrical power generation. It is not connected to the utility grid network. It provides power to the non-electrified or remote area.
3. *Peak load sharing DG:* In this case, DGs are used under peak load demand to assist the industrial customer with reduced per unit energy cost.
4. *Combined Heat and Power (CHP) DG:* In this type of application, DGs are providing CHP with higher efficiency. The heat produced in this situation will be reused for other applications.
5. *Base load DG:* In this type of application, DGs use as a base load plant and supports the main utility grid [2].

1.3.2 Issues associated with the use of DG

The major issues concerned with the application of DGs in a distribution network are categorized as per the following [7], [8]:

1. Energy efficiency
2. Economics of the energy generation and utilization
3. Reliability of the system
4. Environmental issues
5. Interconnection with an existing utility grid network

The utilization of different types of DGs (inverter and synchronous generator) and the integration of these DGs with the existing network, causes deviations in the signal of voltages [9], [10]. Hence, it can be said that among the above mentioned issues, an interconnection of DG with the existing utility grid network is a great challenge for the power system engineers. Moreover, along with certain technical and non-technical problems, it can raise an issue of development of protocol and licensing of the integration of DG with the DN [8].

1.3.3 Technical issues during interconnection of DG with DN

The DG plant is mostly located at the consumer end to supply the energy demand of the load. Similarly, the utility is also supplying power through the grid network to the consumers. In case of peak load demand, the load sharing is carried out between the DG and the utility. However, during off peak period, DG supplies an excess power over the grid network as it is interconnected with the utility grid network. Besides, the various advantage of DG interconnection, it creates several other problems such as degradation of power quality and loss of utility control over the existing grid network. Along with these, there are several other issues which need to be considered during the interconnection of DGs with the existing utility grid network. These are listed below [11], [12].

- The safety of the utility personals working with the utility grid network.
- Safety of the customers.
- Protection of existing distribution network and consumer's property.
- Protection against the abnormal operation of DG.
- Protection coordination of existing distribution network.

1.4 Protection issues during DG interconnection

During integrated mode operation, the load is supplied by the combined power supply from the utility and the DG. In this case, the sudden disconnection of utility makes the DG

feed the load. Therefore, the sudden change in power demand on the DG fluctuates the voltage signal of the DG and load. At the same time, the DG must be capable enough to mitigate the sudden rise in load demand. The sudden deviation in the voltage magnitude and frequency from its nominal operating range damages the DG or equipment of the DN/end user.

Furthermore, it is well known that the conventional protection schemes used for DN are designed for the unidirectional power flow. Hence, all existing protection schemes provide satisfactory results when the direction of current flow is unidirectional. However, an integration of DG into DN changes the direction of current flow in the network. This makes the protective devices to mal-operate or in some cases, it may remain unoperated during various abnormal/fault conditions. In case of fault situation, the protective device located at the fault location must be able to withstand the additional fault current supplied by the DG. Hence, it can be said that the integration of DG into the existing radial DN increases the short circuit level of the network. This leads to the replacement of existing protective devices with higher short circuit current withstand capacity.

Therefore, the major protection problems caused by the integration of DG with an existing DN are (i) Sudden disconnection of utility (Islanding) and (ii) Loss of existing protection coordination among protective devices [13]–[16]. Both the above mentioned protection issues have been thoroughly discussed in the following sections.

1.5 Islanding

The condition in which the part of an electrical power network consisting of one or more number of DGs and load disconnected from the rest of the network is called as islanding [17]–[19]. Fig. 1.1 shows the radial network containing a DG. It is seen from Fig. 1.1 that the DG is interconnected at the secondary distribution. Further, as per Fig. 1.1, a Circuit Breaker (CB) is used to connect or disconnect the DG with the utility. An opening of the CB disconnects the part of the electrical network and creates an electrical island. The islanding is either intentional or unintentional. An intentional islanding is a planned event under the supervision of experts. In this case, the equipment and devices are designed to cope with this event. Furthermore, during the intentional islanding, the voltage and frequency of the island network are monitored and provisions are made to keep them constant or within the prescribed limit. Conversely, in case of an unintentional islanding, the small part of the distribution network containing DGs and loads disconnects suddenly from the rest of the DN. In this situation, DGs are still energizing a small network through a Point of Common Coupling (PCC) [4], [14],

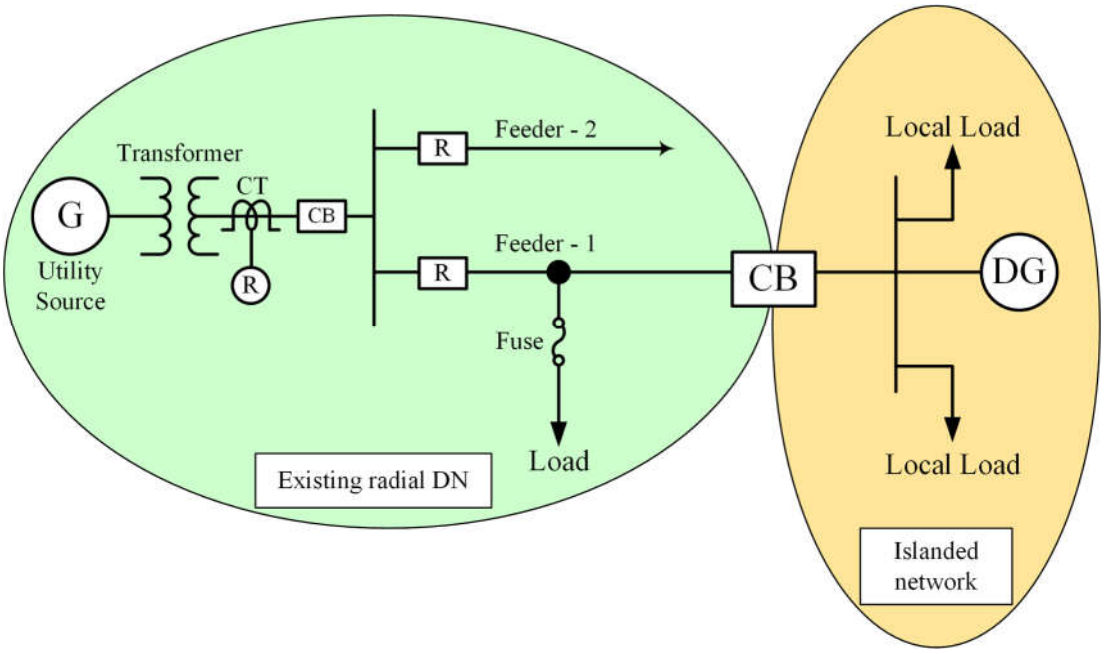


Fig. 1.1 Formation of electrical island

[15], [20]. During such condition, the voltage and frequency of the island network exceed its nominal values. This deviation in the value of voltage magnitude and frequency is large enough to damage the equipment at the consumer end. Moreover, managing a network following an islanding is a very crucial task as the sudden disconnection creates high frequency oscillations in the network, which may lead to maloperation of another relay in the network [21], [22]. In addition, other major problems arise due to the unintentional islanding situation are discussed below.

Power quality issue: The power system operator is responsible for the quality of power provided to the consumers. However, during an islanding situation, the voltage and frequency of the power provided to the customers vary significantly and, sometimes, it may exceed the statutory limits. The power quality issue deals with Over Voltage (OV), Under Voltage (UV), voltage imbalance, waveform distortion (harmonic), voltage fluctuations, Over Frequency (OF), and Under Frequency (UF) [8], [20], [23]–[26]. Further, during this situation, the utility has no control over it. Hence, it is recommended to look after the power quality issue during islanding.

Personnel safety: The power system is designed to work as a passive network with "top-to-down" unidirectional power flow. When the DGs are interconnected with the distribution network, the network power flow becomes bidirectional. In the eventuality of fault in the upstream network, the faulty part will be disconnected from the network by opening a breaker. However, the DG still remains energized and continues to supply the power to the disconnected network. Meanwhile, personnel sent out for maintenance work may get an electric shock

during maintenance work due to power supplied by the DG in an island network. This poses a safety hazard to utility maintenance personnel and the general public [20], [27].

Out of Synchronism reclose: An auto recloser is commonly used in DN to restore service after a fault. It has been reported in the literature that the recloser effectively improves the reliability of supply during temporary faults. During the attempt of reclosing, DG may not be in synchronism, even though a recloser is trying to reconnect the DG with the utility grid. This may cause overvoltage, overcurrent and severe torque transients which subsequently put rotating machines and other equipment at risk [20], [27].

1.6 Islanding detection

In order to avoid damage at the consumer end as well as to the DN, and also to provide personal safety, the islanding situation must be detected as quickly as possible. According to IEEE standard 1547-2003, the DG in an islanded network must be disconnected within 2 *s* from the inception of the event [17]. To fulfil the requirement of the said standard, an accurate and fast islanding detection method is required. Hence, various researchers have proposed different methods of islanding detection. These methods are operated remotely or locally. According to its mode of operation and acquisition of signal(s), these methods are categorized as (1) Remote method and (2) Local method [13]–[15]. The remote method is a communication assisted method whereas, the local method is implemented at the location of the DG. Further, in the remote method, the islanding detection is carried out at the remote location and a trip signal is issued to disconnect the target DG. Conversely, in the case of the local method, the islanding detection is performed at the location of DG [28], [29]. In this method, different electrical parameters and its rate of change are monitored locally. The significant deflection or deviation in these parameters are used to detect an islanding situation. On detection of islanding situation, a trip signal will be executed to disconnect the target DG. The local method is further categorized as (i) Active method (ii) Passive method and (iii) Hybrid method of islanding detection [28]–[32].

1.6.1 Remote method

This method is a communication based method. Fig. 1.2 shows the single line diagram of a network containing a typical communication based islanding detection scheme. In this method, the status of recloser or CB which can cause an island is continuously monitored. During the opening of recloser or CB due to any fault/abnormal condition in the network, a trip signal is initiated to disconnect the DG [31], [33], [34]. This method does not depend upon the type and size of DG. Further, it gives satisfactory results during islanding detection with

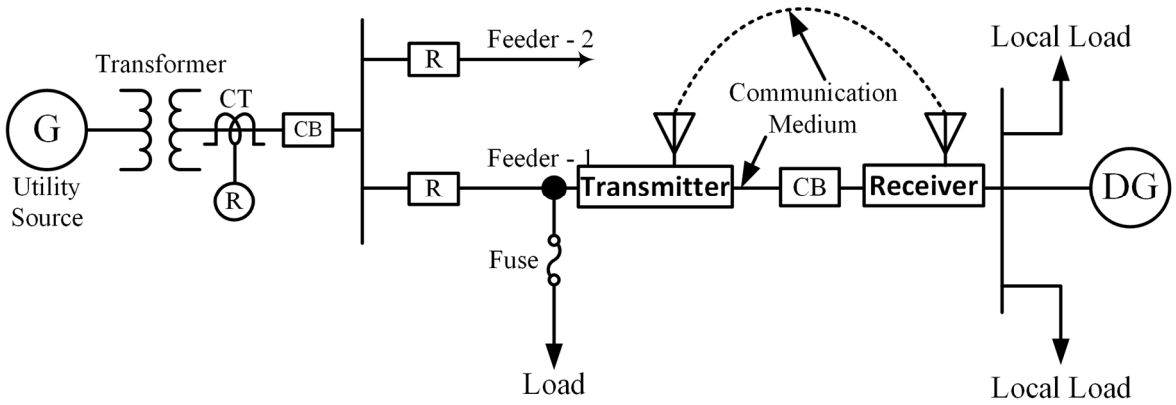


Fig. 1.2 A typical network containing communication assisted islanding detection

minimum or almost zero non-detection zones. However, the main drawback of this method is that it is very expensive and, it requires an almost structural level modification in the existing network. Furthermore, it increases a level of complexity due to the placement of signal transmitters and receivers at all possible switching locations from where the island can be formed [31], [33]–[35]. Moreover, in case of loss of communication between transmitter and receiver, the Loss of Mains (LOM) protection is affected largely. Several conventionally used communication based methods are described as follows.

1.6.1.1 Power line carrier communication (PLCC) based scheme

In this scheme, a distribution line or power line is used as a signal carrier and, a transmitter & receiver are located on grid and DG side, respectively. A low energy signal is broadcasted by the transmitter continuously over the power line which is received by the receiver on the DG side. Here, failure in sensing the signal for three consecutive cycles is considered as islanding situation and immediate activation of disconnection of the DG unit takes place. This method gives a reliable islanding detection with almost zero NDZ. Furthermore, in this method, the installation of transmitters and receivers does not affect the quality of the power. However, the cost associated with the installation of signal transmitter and receiver is very high and, hence, the scheme becomes uneconomical for the network containing a single or less number of DG [36]–[38].

1.6.1.2 Signal Produced by Disconnect (SPD) based scheme

This is similar to the PLCC based scheme. In this scheme, the transmission of a signal is carried out by microwave link or telephone line. Similar to the PLCC based technique, this scheme is also continuously sensing the transmitted signal at the receiver end. Along with the advantage of low NDZ; this method also provides full control of the DG by the utility grid.

This method is helpful during the black start due to its good coordination between the DG and the utility. However, the implementation of this scheme via telephone line requires an increase in communication wiring and setup of a communication protocol which makes it more expensive. Subsequently, with help of microwave link (radio frequency communication), the signal transmission covers a limited area only. Further, to get full coverage of the microwave communication, repeaters are required to install at certain locations. At the same time, the range of working frequencies must be established which might require licensing. This makes the scheme furthermore expensive [39].

1.6.1.3 Supervisory Control And Data Acquisition (SCADA) based scheme

This is basically a transfer trip kind of scheme which requires to monitor and communicate the status of CB to the controlling unit of the network. In this scheme, when the communicated status of utility CB connected to DG is detected as an open condition, an algorithm installed at the central location operates and issues a trip signal to disconnect the target DG of the island area. The advantage of this method is that it is able to take additional control of DG. Further, in this scheme, the NDZ of the islanding detection can be eliminated and the operational efficiency of the scheme can be improved with the proper installation of the communication system. However, it is more expensive due to the requirement of a large number of sensors and other additional features of the system. Furthermore, it is very complex to install this technique in the existing DN. In addition, it is not economical to use this scheme for a network containing a less number of DGs [28], [30], [34], [40].

1.6.1.4 Phasor Measurement Unit (PMU) based scheme

In this scheme, two PMUs are utilized for the detection of islanding situation. Out of two PMUs, one is located at the utility substation, which provides utility voltage and its phase angle, whereas, another one is located at the DG side to obtained the DG voltage and its phase angle. Both the PMUs calculate the phase angle with respect to the Global Positioning System (GPS) time step [41]. This information about voltages and its phase angles are transferred to each PMU of the network with the help of a dedicated communication channel [42]. During the islanding situation, the difference between the phase angle of the utility voltage and DG voltage is calculated. The calculated phase angle difference is then compared with the normal phase angle difference for the detection of islanding situation [43], [44]. Further, in order to avoid error in the phasor, the value of phase difference between the estimated phase angle is continuously updated. On the detection of islanding situation, a trip signal is activated to disconnect the target DG. Recently, another concept based on the systematic Principle

Component Analysis (PCA) has been presented in [45]. These schemes cover significantly higher geographical area and hence, the delay in communication is expected during real-time operation. Moreover, it is uneconomical to the install the PMU for a small capacity of DG [43]–[45].

1.6.2 Active islanding detection method

Active method is one of the local methods. Fig. 1.3 shows the typical active method of islanding detection. As shown in Fig. 1.3, an external turbulence is continually injected into the DG. The islanding situation is detected by observing the response of the system followed by the external signal injection. The system response involves the measurement of various electrical parameters such as voltage, current, frequency, active power, reactive power, and harmonics at the DG location. During normal operating condition, the change in the measured parameters due to external turbulence is not noticeable. However, in the case of islanding, the external turbulent changes one of the measured parameters to a larger magnitude which in turn detects the event as an islanding situation. The foremost advantage of this method is the minimum value of NDZ. However, the major disadvantages of this method are the degradation of power quality and higher detection time due to external signal injection [31], [39], [46], [47]. Many researchers have proposed various active islanding detection schemes. The details of these methods are described in the following subsections.

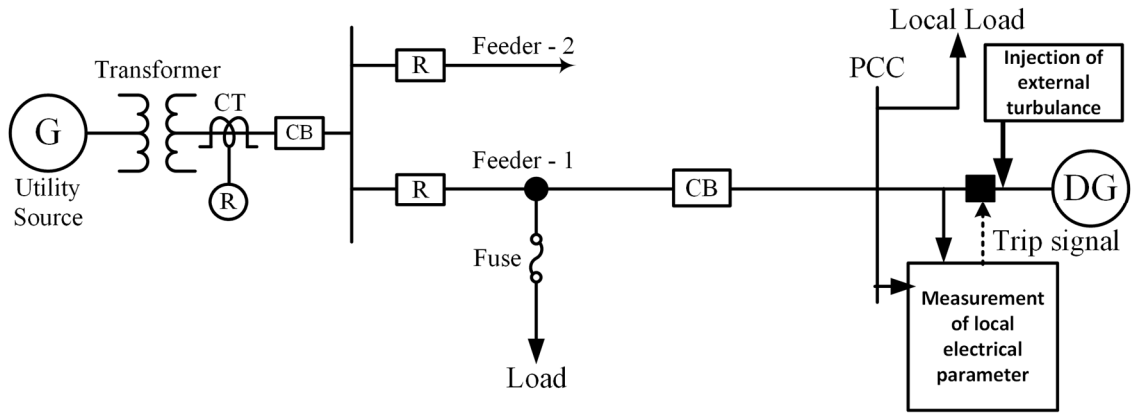


Fig. 1.3 A typical network containing active islanding detection method

1.6.2.1 Current injection based technique

Karimi *et al*. [48] and Bahrani *et al*. [49] proposed an active islanding detection technique based on the injection of negative sequence current into the network which contains a Voltage Source Converter (VSC) based DG. This technique measures the negative sequence voltage at PCC with the help of Unified Three-phase Signal Processor (UTSP) for the detection

of islanding situation. In this technique, the magnitude of the negative sequence current injected into the network is less than 3 %. Though these schemes perform well with small NDZ, injection of negative sequence current into the network degrade the quality of power. Another approach based on the injection of disturbance into direct or quadrature axis current controller has been proposed in [50]. In this scheme, deviation in the measured value of voltage magnitude at the PCC has been utilized for the detection of islanding situation.

1.6.2.2 Slip Mode Frequency Shift method (SMS)

An SMS method is a Positive Feedback (PF) based islanding detection method. Generally, the PF is applied to the amplitude, frequency, and phase of the acquired signal. Smith *et al.* [51] proposed a technique utilizing PF to the phase of the voltage signal at PCC which in turn shifts the phase and short term frequency of the signal. As the inverter base DGs operate with unity power factor, there is no phase angle between the voltage and current of the inverter output. Henceforth, the generated phase angle will be the function of the frequency of the acquired voltage at PCC. During normal operating condition, this method remains stable. Whereas, in case of islanding condition, there is a large deflection in the frequency of PCC voltage which will be detected as an islanding condition. This method has a small NDZ and it is easy to implement. However, it reduces the power quality. Furthermore, its accuracy has been deteriorated due to the error in measurement, noise, and quantization [51]. Later on, these errors have been rectified by Liu *et al.* [52] by applying an additional phase shift to the acquired voltage signal. This method is therefore called as improved-SMS (IM-SMS) method.

1.6.2.3 Active Frequency Drift (AFD) or frequency bias method

In this technique, a PF is applied to the output current of the inverter for acceleration of frequency of the current. During islanding, a phase error is developed between the inverter output current and the PCC voltage. Under this situation, the inverter tries to reduce this error by increasing the frequency of the current. Finally, this increase in frequency exceeds the limit and will be detected by the Over Frequency Protection (OFP) which initiates a trip signal to disconnect the target DG. This method provides benefits in terms of easiness in installation and small NDZ [53], [54]. The scheme based on the similar concept has been reported in [55], [56] which provides improved results in terms of NDZ.

1.6.2.4 Sandia Frequency Shift (SFS) method

The SFS method is an extension of the previously discussed AFD method. In this method, a small error generated in phase tries to amplify the small change in frequency. But,

due to the integration of utility, its effect remains unaffected. However, during islanding, the developed phase error in the PF makes the frequency greater than its threshold. This method has given better results during islanding with smaller NDZ. Further, its performance is also better in terms of power quality as compared to AFD based method [57]–[61].

1.6.2.5 Sandia Voltage Shift (SVS)

This scheme utilizes PF to slightly deviate voltage magnitude for the detection of islanding situation. The deviation in the voltage magnitude does not affect the performance of the system during a normal operating condition. However, during islanding condition, the PF changes the magnitude of voltage significantly and hence, the Under Voltage Protection (UVP) operates and trips the DG. Though this method has very low NDZ, it suffers from the shortcomings of deterioration in the quality of power and reduction in the efficiency of the inverter operation due to positive feedback [39], [62]–[65]. Afterwards, Samui *et al.* [66], [67] proposed another method utilizing the PF with variable voltage signal gain. The response of the scheme proposed in [67] has been verified on the frequency dependent ZIP exponential load model. Though this scheme provides satisfactory results during islanding, its performance largely depends on the value of voltage gain. Further, improper selection of voltage gain affects the performance of the said scheme.

1.6.2.6 Automatic Phase Shift (APS) scheme

In this scheme, a phase shift is introduced in the current signal with respect to the frequency of the voltage. This is inserted at each time during which the frequency changes its state of operation. In this scheme, the islanding situation is detected by Over Frequency Relay (OFR) or Under Frequency Relay (UFR) as the islanding event causes the frequency to deviate from its nominal operating range. Further, the deviation in frequency largely depends on the percentage mismatch of active power between generation and load at the instant of islanding. The performance of this scheme gives a better result for the network containing multiple inverters based DGs. However, its performance during the nonlinear load such as an induction motor with large inertia is poor [68], [69].

1.6.2.7 Impedance estimation based scheme

In an integrated network, the utility grid network offers low impedance as compared to the DG. This fact has been utilized in this technique. Here, the estimated value of impedance seen from the DG is used for the detection of islanding situation. In case of inverter based DG, an external disturbance added to the system affects the voltage signal during

abnormal/transient conditions. Therefore, to detect islanding situation, the variation in *dv*/*di* is required to be calculated which reflects the value of impedance seen by the inverter. This scheme performs satisfactorily with a low mismatch between generation and load power. However, its performance reduces with an increase in a number of the inverter based DGs in the network. Moreover, improper selection of a threshold for impedance seen by DG critically affects the performance of this scheme [70]–[77].

1.6.2.8 Scheme based on Reactive Power Export Error Detection (RPEED)

This scheme is based on reactive power flow through the line connected between the utility grid and the DG. An Automatic Voltage Regulator (AVR) has been used to control the flow of reactive power over the line. Further, an islanding situation has been detected by measuring an error generated in the export of reactive power during a specific time interval. This duration is of the order of 2 – 5 seconds. The scheme effectively detects an islanding situation irrespective of change in generator loading. However, due to higher detection time, it is best suited for backup protection. Moreover, due to almost unity power factor operation of inverter based DG, this scheme is not suitable for the network containing inverter based DGs [34], [78]–[80].

1.6.2.9 Other active methods of islanding detection

Reynen *et al.* [81] proposed an active method of islanding detection based on the correlation between disturbances in system voltage and a pseudo-random sequence. This method has given an acceptable result in the detection of islanding situation. However, implementation of such scheme must fulfil certain requirements such as same pseudo-noise sequence, same phase shift of all the DGs in the network, all DGs must be able to supply an equal fraction of load power, and DGs output must be ideal.

1.6.3 Passive islanding detection method

Fig. 1.4 shows the single line diagram of a typical network, which is used for illustration of the passive islanding detection method.

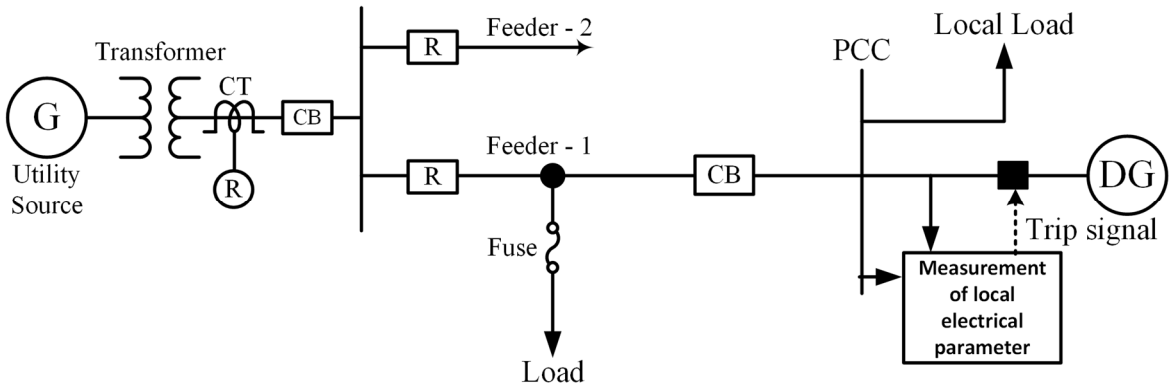


Fig. 1.4 A typical network containing passive islanding detection method

As shown in Fig. 1.4, variations in the magnitude, phase, and frequency of various electrical parameters such as voltage, current, impedance, active power, reactive power, harmonic distortion, and phase angle are monitored at the terminal of the target DG. Moreover, the variation in the rate of change of these parameters with respect to the time as well as with respect to other parameter is also examined for the detection of islanding situation. In addition, different approaches using various transforms, classifiers, and artificial intelligence on the acquired signals or on its features are also utilized for islanding detection. The passive method is easy to implement and less expensive as compared to the communication based and active method. However, this method suffers from the higher value of NDZ and nuisance tripping [28]–[31], [82]. Some of the popularly known passive islanding detection techniques are discussed below.

1.6.3.1 Under Frequency /Over Frequency (UF/OF) relay

During normal operating condition, the frequency of interconnected DG is matched with the grid frequency. Conversely, during sudden disconnection of DG from the utility grid, the frequency deviates from its normal operating range. However, this deflection in frequency depends upon the mismatch between generation and load active power at the instant of islanding. The scheme measures this increase/decrease of frequency for the detection of islanding situation. If the change in frequency crosses a predefined threshold, the UF/OF relay initiates a trip signal to disconnect the DG. This scheme depends upon the active power imbalance between generation and load hence, its performance is not satisfactory for less or zero power imbalance [83], [84].

1.6.3.2 Under voltage /Over Voltage (UV/OV) relay

Similar to the previous scheme, the UV/OV relay operates during an islanding situation

for out of band variation of voltage magnitude. The variation in the voltage magnitude depends upon the reactive power mismatch between generation and load. However, the instantaneous change in voltage magnitude is quite faster than the frequency based relay as there is no inertia involved in this scheme. Further, if the deviation of voltage magnitude is higher or lower than its operating band, the UV/OV relay initiates a trip signal to disconnect the target DG. The major shortcoming of the method is its nuisance tripping and large values of NDZ [84].

1.6.3.3 Rate Of Change Of Frequency (ROCOF) based scheme

This is the most commonly employed method of islanding situation. In this scheme, the deviation of frequency and its rate of change is required to monitor for the detection of islanding situation. Due to the active power imbalance between the generation and the load during sudden disconnection of DG, the frequency increases or decreases beyond its operating limit. However, the value of the rate of change of frequency depends upon the power imbalance at the instant of islanding. The ROCOF relay operates only when the slop of *df*/*dt* exceeds the pre-set threshold value. For such a relay, the typical threshold value is in the range of 0.1 Hz/s to 1 Hz/s. However, this relay fails to detect islanding situation with the zero mismatch of power between generation and load. Furthermore, this scheme suffers from nuisance trip during several network transient conditions such as sudden load change, switching of heavy captative load, and starting of large sized induction motor [85]–[88]. Thereafter, in order to enhance the performance of the ROCOF relay in terms of NDZ, several modifications have been proposed by various researchers [88], [89].

1.6.3.4 Rate Of Change Of Frequency Over Power (ROCOFOP) based scheme

This scheme measures the variation in the rate of change of frequency with respect to the change in the active power output of the DG. It has been observed that the deviation in ROCOFOP during islanding situation is larger in case of the small network compared to the large network. This concept has been employed in this scheme to overcome the NDZ issue of the normal ROCOF relay. During islanding situation with small power mismatch, this scheme has given better performance compared to normal ROCOF based scheme in terms of NDZ. However, it has given unsatisfactory results during perfect power balance condition [90].

1.6.3.5 Vector Surge (VS) relay

This relay detects islanding situation based upon the comparison of one cycle time duration of an output voltage with its previous cycle duration. During non-islanding/islanding condition, this duration is either shorter or longer as compared to the time duration of the steady

state condition. Further, during islanding condition, this duration depends upon the power imbalance between the generation and load. The variation in the time duration of a cycle results in a deflection of the phase angle of the voltage which is the operating parameter of the VS relay. Furthermore, if the variation in phase angle exceeds the pre-set threshold value, the relay initiates a trip signal to disconnect the target DG. Generally, the threshold for the VS relay is in the range of 2º to 20º. However, this relay suffers from the large NDZ. Moreover, it issues a nuisance trip during several non-islanding events such as a fault on the adjacent feeder and sudden load switching [91]–[95].

1.6.3.6 Schemes based on the harmonics of voltage and current

This technique is based on a comparison of Total Harmonic Distortion (THD) of the acquired voltage or current signal with the pre-set threshold. During islanding condition, an inverter produces current harmonics and feeds the island network, which offers higher impedance compared to the grid network. Therefore, due to the harmonic current and load impedance, the network voltage is distorted. This ultimately increases the THD of the voltage signal which goes well above the threshold during islanding situation. Hence, the islanding situation is detected by the relay and finally, it initiates a trip signal to isolate the target DG. The performance of the said scheme is independent of a number of inverter DGs in the network. However, it is sensitive to the critical disturbances in the network, which increases the THD of the voltage. Hence, improper selection of threshold value would result in false tripping of DG [96].

1.6.3.7 Scheme based on Voltage Unbalance (VU)

In this scheme, an unbalance in the three-phase output voltage of DG is continuously monitored for the detection of islanding situation. The unbalance of the voltage depends on the topology of the network, connected load, and the sudden occurrence of the abnormal condition. In this scheme, the VU is monitored at each time step or at a specific interval with the normal steady state condition. However, this method is specifically designed for a three-phase system and hence, it is not applicable to a network containing a single phase DG [96]–[98].

1.6.3.8 Various transform based schemes

The development in the field of signal processing techniques has been utilized in the area of islanding detection. These techniques are applied to extract the useful information from the acquired signals with the help of various transforms. Researchers have proposed different schemes based on several transforms such as time-frequency transform, synchronous

transform, Wavelet Transform (WT), S-Transform (ST), and Hilbert-Huang Transform (HHT). In these schemes, acquired voltage or current signals have been utilized as an input to the transforms. These transforms decompose the input signal into various component such as magnitude, angle, high frequency, low frequency, and energy. Based on these extracted features, an islanding detection schemes have been developed. These schemes have given better results in terms of reduced NDZ and higher stability during non-islanding events. However, it is very difficult to implement these schemes in a real network. In addition, higher sensitivity towards the noise signal and inability to include various signals in the predetermined Gaussian window are shortcomings of the said techniques [99]–[107].

1.6.3.9 Artificial intelligence, pattern recognition and decision tree based approach

Recently, with the advancement in the field of Artificial Intelligence (AI), Pattern Recognition (PR), data mining and Decision Tree (DT), several researchers have proposed different methods of islanding detection based on these techniques. In these schemes, magnitude, frequency, or other extracted features of the acquired signals have been utilized for the detection of islanding situation. These schemes require a large number of datasets related to islanding and non-islanding events. Initially, these datasets are used to train the AI, PR, or DT based model for effective differentiation between islanding and non-islanding event. In a real-time operation, the generated event is passing through the trained modal for classification as islanding or non-islanding event. If the event is detected as islanding event, the relay initiates a trip signal for disconnection of the target DG. However, practical implementation of these schemes is very complex. Further, the performance of such schemes during unseen dataset is not satisfactory [108]–[117].

1.6.3.10 Other passive islanding techniques

Apart from the above discussed schemes, researchers have also presented different other approaches for the detection of islanding situation. A rate of change of impedance based approach has been presented by Shah *et al.* [118] for the detection of islanding situation. Though this technique provides better results during islanding situation with a higher mismatch of power, its performance is not acceptable in case of a lower mismatch of load-generation power. Thereafter, negative sequence voltage, sequence component of current, the rate of change of sequence currents, superimposed components of the current, and multi-feature based passive islanding detection schemes have been proposed by several researchers [119]–[124]. The phase jump based method has been proposed by Singam *et al*. [125]. In this scheme, if the phase angle exceeds a pre-set threshold, it would be detected as islanding situation. Another

method based on mathematical morphology has been proposed in [126], [127]. It has used dilate erode difference filter for the detection of islanding situation. These schemes are able to detect islanding situation with a lower mismatch of active power. However, the verification of the said techniques on experimental/field results has not been conducted. Later on, Bejmert *et al*. [128] proposed a scheme based on the insertion of a capacitor bank in the network during islanding for accurate detection of islanding condition. The main objective of the insertion of the capacitor bank is to provide reactive power during islanding and trying to reduce the power mismatch.

1.6.4 Hybrid method of islanding detection

The hybrid method is a combination of both active and passive methods of islanding detection. In this method, an active technique is applied only if islanding detection is suspected by a passive technique. In this case, the measurement of electrical parameters is carried out at the DG locations only [12], [28], [29], [97]. Some of the hybrid islanding detection methods are discussed below.

1.6.4.1 Positive feedback and voltage unbalance based method

In this scheme, the PF (an active method) is applied, which creates an unbalance in voltage (a passive technique). This VU is not significant in the presence of the utility grid. However, in case of disconnection of the grid network, the UV is large enough for the detection of islanding situation. Nevertheless, the application of this method is limited to three phase systems only [98].

1.6.4.2 SFS/SMS and ROCOF base technique

In this technique, both the active and passive methods in terms of SFS and ROCOF, respectively, have been utilized for the detection of islanding situation. During an abnormal operating condition, the ROCOF relay operates first and activates the SFS scheme which distinguishes an event as an islanding situation or a non-islanding event. On the detection of the islanding situation by the SFS scheme, the relay initiates a trip signal to disconnect the target DG. This method provides a better result in the detection of islanding as compared to only the ROCOF or SFS based scheme. Furthermore, this scheme remains more stable during load switching events. However, due to the incorporation of the active method, this method takes quite a long time for the detection of islanding situations [129]–[131].

1.6.4.3 Average rate of change of voltage and active power based schemes

An average rate of change of voltage and real power shift based technique has been

proposed in [132] for the effective detection of islanding situation. The passive method initiates the active method during islanding or non-islanding situations. In this scheme, if the passive method is unable to clearly distinguish between the islanding and non-islanding event, it shifts the real output power of the DG for further efficient detection of islanding situation. The performance of this method is very efficient for the network containing a large number of the inverter based DGs. Thereafter, using the same concept of average rate of change of voltage with capacitor tap switching, a new technique has been proposed in [133]. In this technique, again the capacitor tap switching occurs when the passive technique is unable to clearly distinguish between the islanding situation and non-islanding event. However, this scheme takes longer time compared to other past published methods of islanding detection.

1.6.4.4 DT classifier and PF based hybrid islanding technique

In this scheme, a DT classifier (passive technique) and a PF for voltage/frequency (active technique) have been used for the detection of islanding situation. The active method has been used to regulate the output power of the DG with respect to the rated value of the DG. Further, the DT classifier has used a feature vector which is made up of various signals such as voltage magnitude, voltage frequency, the rate of change of voltage, the rate of change of frequency, the rate of change of active power, and the rate of change of reactive power. Here, various test cases of islanding and non-islanding have been generated by applying PF to the voltage/frequency. The developed test cases have been utilized for the training of DT classifier model for efficient classification between islanding and non-islanding events. The results of the said scheme indicate the reduction of NDZ of islanding detection. However, the performance during unseen datasets can cause the relay to mal-operate or remain stable [134].

1.7 Loss of existing protection coordination among protective devices

An interconnection of DG with an existing distribution network disturbs the protection coordination of the network [135]–[138]. The said issue can be easily understood from Fig. 1.5. As observed from Fig. 1.5, normally, in a radial distribution network various protective devices such as Overcurrent Relay (OCR), recloser, and fuse are coordinated based on unidirectional power flow [139]. When the DG is interconnected with radial DN, the DG current flows into the network towards the load as well as the source. Hence, the lateral end protective devices see more current than the source end device. In this condition, existing protection coordination may be lost. The above said situation of loss of protection coordination is explained in the following.

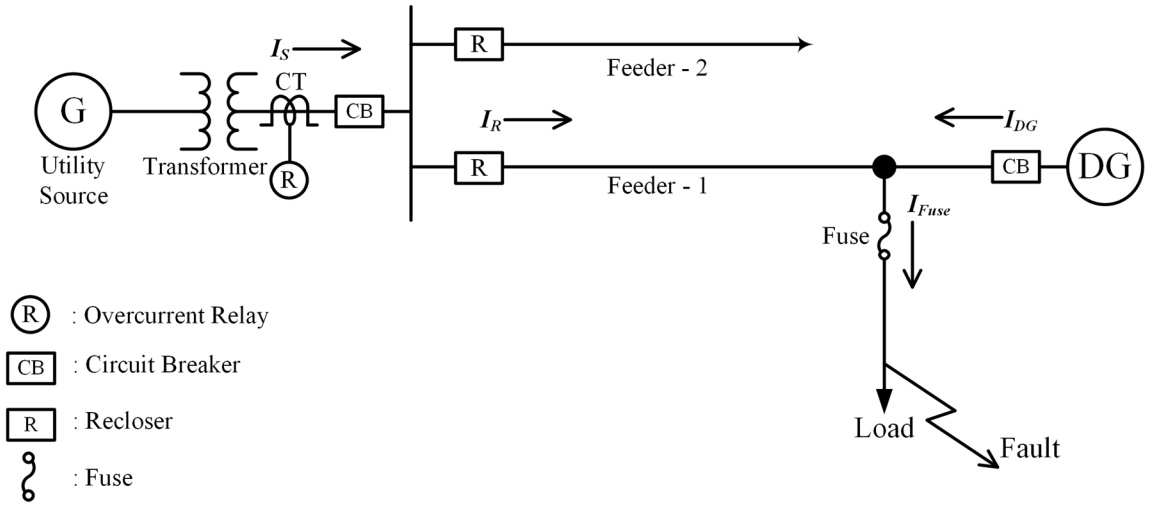


Fig. 1.5 Typical radial distribution network with DG

Let, I_S is the utility source current, I_R is the current seen by recloser, I_{Fuse} is the current flowing through the fuse and, I_{DG} is the current supplied by the DG.

Without DG:

In this case, the current flowing through the recloser and fuse are equal. Further, the current supplied by the DG is zero. This situation is described by equation (1.1).

$$I_{Fuse} = I_R \quad and \quad I_{DG} = 0 \tag{1.1}$$

With DG:

The current flowing from the lateral fuse is the sum of the current flowing from recloser and current supplied by the DG. This situation is described by equation (1.2).

$$i.e.\ I_{Fuse} \neq I_R \quad but \quad I_{Fuse} = I_R + I_{DG} \tag{1.2}$$

Conventionally, in the DN, the low rated fuse is coordinated with a higher capacity upstream fuse. The high rated fuse is coordinated with the upstream recloser and, the recloser is coordinated with the upstream OCR. Finally, the OCR is coordinated with another upstream OCR. In this way, the protection coordination covers the entire DN and provides primary and backup protection to every segment of the DN. The coordinated backup protection protects the network in case of failure of primary protection [140]–[142]. Hence, the protection coordination problem in DN can be categorized as (i) fuse to fuse coordination, (ii) fuse to recloser coordination, (iii) recloser to OCR coordination and (iv) OCR to OCR coordination. Among all coordination issues, the recloser – fuse coordination is very crucial. This is due to the fact that in case of a temporary fault on any of the lateral, the recloser has to operate faster

than the fuse. Conversely, during a permanent fault, the fuse has to blow before the recloser. On contrary, in the presence of DG on the lateral, an additional fault current is supplied by the DG. This makes the fuse to blow prior to the recloser for every temporary fault condition and permanently disconnect the network. This is against the fuse saving principle and makes an expensive fuse to blow even for a temporary fault [135]–[137], [143]–[145].

1.8 Review of techniques for recloser – fuse coordination in presence of DG

Integration of DG in the DN at different locations create many technical challenges among which coordination between recloser and fuse is the prominent one [135]. In this situation, as per the fuse saving concept, the recloser needs to operate faster than the fuse for all temporary faults with its "Fast" operating characteristic. Conversely, for a permanent fault, the fuse must blow before the recloser lock-out [135], [146]. However, due to limited fault current injection capability of inverter based DGs, it would be easy to maintain coordination between recloser and fuse within the minimum and maximum fault current range. Even the newer inverter based DGs are IEEE1547 compliant, and hence, they contribute fault current less than 2.0 pu of the converter rating [147], [148]. Nevertheless, the above coordination is lost during the interconnection of synchronous based DG due to its high fault current injection capacity (several times of the full load rating). To overcome the said problem, researchers have proposed various techniques [149]–[164]. These techniques are based on (i) modification of recloser characteristic according to the ratio of recloser to fuse current (I_R/I_F) (ii) division of DN into different zones (iii) maximum level of penetration and location of DG interconnection and (iv) application of Fault Current Limiter (FCL)/Superconducting Fault Current Limiter (SFCL).

1.8.1 Recloser – fuse coordination technique based on the ratio of I_R/I_F

The methods proposed in [149]–[152] have utilized an adaptive relaying scheme which modifies the Time Dial Setting (TDS) of the recloser's fast TCC according to the ratio of I_R/I_F. However, the prime limitation of the above techniques is the requirement of fuse currents to be measured at all locations in the DN, which increases cost and complexity [137]. Moreover, they involve a dedicated communication channel between recloser and all fuses located in the DN, which reduces the reliability of the scheme.

1.8.2 Approach based on the division of DN into different zones,

The solution proposed in [153], [154] divides the entire DN into different zones. Each zone must be equipped with a DG and a breaker with a communication facility. Furthermore, for each zone, it is necessary to maintain a sufficient balance between the capacity of DG and

the load. However, it is difficult to divide the entire DN into different zones with a proper balance between generation and load. In addition, one of the DGs must be equipped with a load frequency control.

1.8.3 Approach based on the restriction of DG penetration

The third approach, as proposed in [155]–[157], calculates the maximum penetration and location of DG interconnection in the DN outside which the coordination between recloser and fuse is lost. Nevertheless, the techniques proposed in [155], [156] have not provided a generalized approach for maintaining proper coordination between recloser–fuse for higher penetration of DGs. Subsequently, in [157], a solution of step by step reduction in the value TDS of the recloser TCC has been suggested to maintain recloser-fuse coordination.

1.8.4 Solution based on utilizing FCL/SFCL

Afterwards, several researchers have proposed different approaches for sustaining proper coordination between recloser and fuse by utilizing FCL/SFCL [158]–[161], [165], [166]. Though FCL/SFCL limits the short circuit current during fault conditions, it leads to power loss due to its continuous use in the circuit. Furthermore, it is not economically viable to install FCL/SFCL at all possible locations in the existing DN.

1.8.5 Other techniques of recloser – fuse coordination in presence of DG

Apart from the above discussed techniques of restoration of coordination between recloser and fuse, several other methods have also been proposed by different researchers. An adaptive relaying scheme based on two different characteristics (time current and instantaneous) has been proposed in [162]. Though the above scheme maintains coordination between recloser and fuse by adaptively modifying pick-up current of the instantaneous characteristic, its performance would depend on the type of system used. Recently, Jamali *et al*. [163] presented a relaying scheme based on a time-current-voltage characteristic which maintains recloser-fuse coordination by altering the value of the constant '*k*'. However, improper selection of '*k*' for high impedance fault largely affects recloser – fuse coordination. Subsequently, Fani *et al.* [164] have proposed an adaptive current limiting strategy to prevent recloser-fuse miscoordination based on auxiliary control mode. Nevertheless, this technique is dedicatedly designed for a PV based DG only. It may not be applicable to a DN containing synchronous based DG.

1.9 Motivation of research

Integration of different types and size of DG at diverse locations in the distribution

network leads to several technical problems among which islanding and recloser-fuse miscoordination are very vital. As per IEEE standard 1547-2003, the DG must be disconnected from the local load within 2 *s* after the sudden disconnection of DG from the utility with the help of anti-islanding protection technique [17]. Furthermore, in case of recloser-fuse coordination, as per the fuse saving concept, the recloser needs to operate faster than the fuse for temporary faults with its "Fast" operating characteristic [135], [136]. This research is focusing on protection problems such as islanding and recloser – fuse miscoordination exist in the distribution network due to the integration of DGs. Moreover, in this proposed research work, efforts have been made to provide accurate islanding detection schemes to isolate the DG during islanding situation quickly. At the same time, an effective solution to restore the coordination between recloser and fuse coordination in the presence of DG has also been provided.

1.10 Original contribution of the research work

The main objective of the thesis is to design and develop effective protection strategies for the islanding detection and to maintain the protection coordination between recloser and fuse in the presence of the synchronous based DG in the DN. The main contribution of this research can be listed as follows.

1.10.1 A pattern recognition based approach for islanding detection

A pattern recognition based islanding detection technique has been presented in the proposed research work. In this work, synchronous and inverter based DGs have been utilized which are connected at various buses of the IEEE 34 bus network. A large number of simulation cases of islanding and non-islanding events have been generated on the IEEE 34 bus network in RTDS/RSCAD environment. Further, in order to proficiently discriminate between islanding situation and non-islanding events, a precise feature selection is very important. Therefore, the process of selection of feature and formation of feature vector has been included in the thesis. In this work, the negative sequence component of currents has been utilized for the formation of the feature vector. Afterwards, the generated test cases have been utilized for the training of the classifier model. Here, in the proposed work, an efficient classifier modal (RVM) has been chosen for its high discrimination efficiency. Furthermore, the minimum percentage (40%) of the acquired data of islanding and non-islanding cases has been utilized for the training of the RVM model. The results obtained in terms of accuracy of the RVM model show that the presented technique is efficiently discriminate between islanding situation and non-islanding events. Moreover, it is capable to detect islanding

situations with lower or zero mismatch of active/reactive power between load and generation. In addition, it remains immune to the non-islanding events. At the end, the comparative assessment proves that the proposed scheme is superior in discrimination between islanding situation and non-islanding events.

1.10.2 Sequence components based approach for islanding detection

A sequence component of voltage based islanding detection technique has been presented in the proposed work. In this work, synchronous and inverter based DGs have been utilized which are connected at various buses of the IEEE 34 bus network. A large number of simulation cases of islanding and non-islanding events have been generated on the IEEE 34 bus network in RTDS/RSCAD platform. In this work, sequence components of the voltage signals have been calculated from the phasor values of acquired voltages. These derived sequence components have been further utilized for the derivation of the IDF. An effective discrimination between islanding situation and non-islanding events have been carried out by comparing the value of the IDF with the pre-set threshold value. The results obtained in terms of IDF for various islanding and non-islanding situations indicate that the proposed scheme accurately distinguishes islanding situation with the non-islanding event. Further, it senses the islanding condition quickly, even at a very critical islanding situation such perfect power balance condition. Furthermore, during a non-islanding situation, the presented scheme remains stable and does not issue a trip signal. Moreover, the comparison of the proposed scheme with the published scheme shows its superiority in the detection of islanding situation.

1.10.3 Modal components based approach for islanding detection

A new islanding detection approach based on modal components of the acquired voltage signals has been presented in the proposed work. In this work, the value of IDF has been calculated by utilizing phasor values of acquired voltages. Further, in order to verify the authenticity of the proposed scheme, a prototype has been developed in the laboratory environment. In this prototype, a synchronous generator based DG has been utilized which is connected to the developed model of the DN. Furthermore, on the prototype, various non-islanding events such as faults with variable fault parameters, switching/starting of capacitor/induction motor and sudden change in load/power factor and islanding situations with different mismatches of active/reactive power have been generated. The experimental results obtained from the prototype show that the presented algorithm is able to detect islanding situation accurately and quickly (within 3 cycles). Moreover, it is capable to detect islanding situations with lower or zero mismatch of active/reactive power between the load and

generation. Subsequently, it remains stable during non-islanding events. At the end, comparative evaluation of the proposed scheme with the existing schemes clearly indicates its superiority in distinguishing islanding situations with non-islanding events.

1.10.4 An auto-correlation based approach for islanding detection

A new islanding detection approach based on auto-correlation of the acquired voltage signal has been presented in the proposed work. In this work, a discrimination factor which is derived from an ACF of the voltage signals is utilized for the detection of islanding situation. The value of DF is calculated from the most affected lags of the ACF during various islanding situations and non-islanding events. Discrimination of an islanding situation with the non-islanding evens has been achieved by comparing the value DF with the pre-set threshold value. Further, the validation of the presented scheme has been carried out by developing an HIL laboratory setup. In this setup, a power distribution test network has been virtually developed in RTDS/RSCAD environment which is physically connected to the DSP controller. During testing, various islanding and non-islanding cases have been generated on the developed HIL model. The experimental results show that the presented algorithm is able to differentiate between the islanding situation and non-islanding events efficiently. Moreover, the proposed scheme is capable of identifying islanding situation even in the case of the perfect power balance condition. In addition, it provides better stability against various non-islanding events and hence it avoids nuisance tripping.

1.10.5 Novel technique to restore the recloser-fuse coordination for DG interfaced distribution network

A novel adaptive relaying technique to restore the proper coordination between recloser and fuse based on the network impedance has been presented in the proposed work. This technique is based on the positive sequence impedance (Z_{1cal}) of a network seen by the recloser. This impedance varies with respect to the interconnection of DGs in the network. In the presented work, in order to calculate the value of Z_{1cal}, the phasor values of the acquired current and voltage samples have been utilized. Further, the acquisition of the samples of current and voltage signals has been performed at the recloser location. The calculated value of Z_{1cal} is utilized for the derivation of the modification factor. In the presence of the DG into the DN, the recloser changes its fast operating TCC with respect to the value of MF. The performance of the proposed scheme has been evaluated by modelling an IEEE 34 bus network in RTDS/RSCAD environment. At the same time, appropriateness of the proposed scheme has been verified on a prototype developed in the laboratory. The results obtained from simulations

as well as from the laboratory prototype clearly indicate that the proposed scheme restore appropriate coordination between recloser and fuse even in case of a high as well as a low penetration of DG in the DN.

1.11 Aim and objectives of the thesis

The main objective of the thesis is to design and develop effective protection strategies for islanding detection and to maintain the protection coordination between recloser and fuse in the presence of synchronous as well as inverter based DG in the DN. Following are the objectives of the thesis.

- To design a new universal islanding detection scheme which can work on any type of DG (synchronous based or inverter based).
- To develop a laboratory prototype which can simulate islanding situation and different types of non-islanding events. Based on the data acquired from the laboratory prototype, the developed universal islanding detection scheme will be validated.
- To detect islanding condition rapidly (as per IEEE 1547 standards) even in case of perfect power balance condition i.e. during zero active and reactive power mismatch.
- To design a scheme which remains stable during various non-islanding events and at the same time, it removes non-detection zone completely.
- To develop a new adaptive protection scheme which maintains proper coordination between recloser and fuse with distributed generation (synchronous based generator) in the DN.
- To develop a laboratory prototype which can resemble a typical distribution network integrated with synchronous based DG. This prototype must be capable to simulate various fault situations in the presence and absence of the DG. Based on the data acquired from the laboratory prototype, the developed adaptive recloser-fuse coordination protection scheme will be validated.

1.12 Organization of thesis

The work presented in this thesis is divided into seven chapters.

Chapter 1: The first chapter deals with the introduction of the distributed generation, its application, issues of interconnection with existing grid and protection problems of DG interconnection. In this chapter, two major issues (i) islanding and (ii) recloser-fuse miscoordination have been discussed. Further, this chapter emphasizes on the research

opportunities in the area of anti-islanding protection and recloser-fuse coordination. Moreover, this chapter provides the necessary background and a comprehensive literature survey on the existing protection schemes for islanding detection and different techniques available to maintain recloser-fuse coordination in the presence of DG in the distribution network.

Chapter 2: This chapter deals with the development of a new digital protection scheme for islanding detection based on the RVM classifier. In this chapter, simulation modelling of IEEE 34 bus network with synchronous & inverter based DGs and an algorithm of the proposed technique has been discussed. The simulation work has been carried out in RTDS/RSCAD environment. Further, the generation of various islanding and non-islanding cases, selection of the feature signal, formation of the feature vector, and training of the classifier model have been meticulously discussed in this chapter. The results obtained during various islanding situations and non-islanding events in terms of variations in the feature signal and at large in terms of efficiency of the classifier model have been clearly shown. At the end, comparative analysis and conclusion of the proposed work are also shown in the chapter.

Chapter 3: In this chapter, a novel digital protection scheme based on sequence components of voltages for islanding detection has been presented. This scheme has utilized a superimposed component of the acquired voltages. Further, the development of simulation models in RTDS/RSCAD environment based on IEEE 34 bus network and IEC 61850 microgrid by utilizing synchronous and inverter DGs have been thoroughly discussed in the chapter. Furthermore, to evaluate the performance of the proposed technique during various islanding and non-islanding events, a large number of such conditions have been generated on the said networks. The results obtained during these test cases in terms of IDF have been graphically shown in different figures of the chapter. At the end, the comparative analysis and conclusion of the proposed technique are also given in the chapter.

Chapter 4: A digital protection technique based on modal components of the voltage signals has been proposed in this chapter. The performance evaluation of the proposed technique has been carried out by developing a prototype in the laboratory environment. In this chapter, utilization of a synchronous DG and its integration with the laboratory prototype have been discussed. Further, the process of acquisition of samples of the voltage signal, conversion of the acquired analogue signal to digital signal and execution of the proposed algorithm have been systematically explained in this chapter. From the developed laboratory prototype, various islanding and different non-islanding events have been generated. The results obtained during various islanding situations and non-islanding events in terms of IDF have been graphically shown in different figures of this chapter. At the end, comparative analysis and conclusion of the proposed technique are given in the chapter.

Chapter 5: A novel concept of HIL testing for the development of a digital protection technique based on ACF of the voltage signals has been proposed in this chapter. The performance evaluation of the proposed technique has been carried out by developing an HIL test setup in the laboratory environment. In this chapter, interfacing of RTDS/RSCAD with the real protection circuit components has been thoroughly explained. Further, the derivation of DF by utilizing the ACF of the acquired voltage signals is explained. From the developed HIL test setup, various islanding and different non-islanding events have been generated. The results obtained during various islanding situations and non-islanding events in terms of DF have been graphically shown in different figures of this chapter. At the end, comparative analysis and conclusion of the proposed technique are given in the chapter.

Chapter 6: An adaptive relaying technique to resolve recloser-fuse miscoordination due to the integration of DG in the DN has been presented in this chapter. This scheme utilizes the impedance of the network seen by recloser in the presence and absence of the DG. The performance of the presented technique has been evaluated on both the simulation and real laboratory prototype. In the simulation, an IEEE 34 bus network have been modelled in RTDS/RSCAD environment. Subsequently, a real hardware setup has been developed which is capable to simulate the required testing in the laboratory environment. In this scheme, according to the status of DG interconnection with the DN, the recloser modifies its fast TCC based on a modification factor. This modified characteristic of the recloser tries to coordinate with the lateral fuse in such a way that during temporary fault the recloser operates faster than the fuse. The entire concept of the presented technique is well explained and shown with the help of the waveforms of the various recloser and fuse characteristics. At the end, the conclusion of the proposed technique is also discussed in the chapter.

Chapter 7: The final chapter presents the conclusion of the work and highlights the contributions made by the author. Suggestions for carrying out further work in the area of islanding detection and recloser-fuse miscoordination have also been proposed.

Chapter 2
Islanding Detection Technique based on Relevance Vector Machine

2.1 Introduction

In this chapter, a new islanding detection technique based on machine learning has been presented. The machine learning is one of the methods of supervised learning and pattern recognition. This concept is developed from the artificial intelligence. The major applications of the machine learning methods are in the field of classification analysis, regression analysis, clustering analysis, and density estimation. In case of classification analysis, an input pattern is labelled with a target value either '0' or '1' for two different case patterns. In order to achieve effective classification by the classifier model, the classifier model is required to train with the help of available patterns. These patterns are in terms of extracted feature(s) of acquired signals. Each pattern of an event has its own signature of a specific type of event category. Further, the extracted feature of the acquired signal is given as an input to the classifier. The classifier model finds the most "like pattern" and classify the input pattern in that category. The above said technology has been utilized in the presented work for efficient detection of islanding situation.

In the presented work, an RVM is used as a classifier model. In order to achieve accurate discrimination between islanding and non-islanding event, various extracted features of the acquired voltage and current signals have been tested. In this testing, variation in the percentage of training dataset and width parameter of the classifier have been considered. With the rigorous analysis, it has been found that the negative sequence component of current (I_2) has performed better in terms of discrimination efficiency with a lower percentage of training datasets as compared to other feature signals. Moreover, to develop a large number of different patterns of islanding and non-islanding events, various islanding and non-islanding events with variable operating parameters have been generated. In this work, an IEEE 34 bus network has been modelled in RTDS/RSCAD environment. This model is designed in such a way that it generates a large number of islanding situations with a variable percentage of power mismatch between load and generation. At the same time, it is also capable to generate different non-islanding events such as fault, sudden load change, switching of a capacitor bank, starting of an induction motor, etc. The acquired signal of currents during these events is then utilized for the training of the RVM classifier.

2.2 Relevance Vector Machine

The working of RVM is same as Support Vector Machine (SVM) except the usage of a Bayesian platform for implementing regression and classification with corresponding sparsity properties [167], [168]. The main advantage of RVM over SVM is that it requires a smaller number of Relevance Vectors (RVs) than the number of Support Vectors (SVs) required by SVM. The modelling of a feature vector with its target class label which is given as input to the proposed model is given by equation (2.1).

$$\{x_i,\ t_i\}_{i=1}^{N} \tag{2.1}$$

Where, $\{x_i\}$ is an input feature vector and $\{t_i\}$ is its corresponding target class label. Generally, it is required to predict the output of the proposed model in terms of a function as $y(x)$ with respect to input feature vector $\{x_i\}$ in machine learning which is given as equation (2.2).

$$y(x;w)=\sum_{i=1}^{M} w_i \bullet \phi_i(x)+w_0 \tag{2.2}$$

Where, w_0 is a bias parameter, $\phi_i(x)=(\phi_1(x),\ \phi_2(x),\ \phi_3(x),.....,\phi_M(x))^T$ are basic functions, and $w=(w_1, w_2,\ w_3,.....,w_M)^T$ are weights. In the proposed model of RVM classifier, the training set is formulated by utilizing I_2. The target value of this dataset is given as 0 and 1 for islanding and non-islanding event, respectively. The equation (2.2) is the prediction of the given training which can be written as equation (2.3).

$$y(x)=\sum_{i=1}^{M} w_i \bullet K(x,x_i)+w_0 \tag{2.3}$$

Where, $K(\cdot,\cdot)$ is kernel function. The RVM classifier model by applying the logistic sigmoid function can be further written as equation (2.4).

$$p(d=0\mid x)=\frac{1}{1+\mathrm{e}^{-y(x)}} \tag{2.4}$$

Where, $d\in\{0,1\}$ is a class label, and p is the probability. With the help of the Bernoulli distribution for $p(t|x)$, the probability is given by equation (2.5).

$$p(t\mid w)=\prod_{i=1}^{N}\sigma\{y(x_i;w)\}^{t_i}\left[1-\sigma\{y(x_i;w)\}\right]^{1-t_i} \tag{2.5}$$

Where, t is a scalar label vector given by $t = [t_1,...,t_N]^T$ with target $t_i \in \{0,1\}$ and the sigmoid function is given by, $\sigma(y)=1/(1+e^{-y(x)})$. As the weights cannot integrate analytically for getting the marginal likelihood in the classification, the approximation procedure, as described in [168], is followed. The posterior distribution over the weight from Bayes rule is thus given by equation (2.6),

$$posterior\ (p(w|t,\alpha,\sigma^2)) = \frac{likelyhood\ \times prior}{evidence} = \frac{p(t|w,\sigma^2)p(w|\alpha)}{P(t|\alpha,\sigma^2)} \tag{2.6}$$

Where, α is a set of hyperparameters. The posterior $p(w|t,\alpha,\sigma^2) \propto p(t|w,\sigma^2)p(w|\alpha)$ will have a strong peak at the most probable parameters W_{MP} which is given by equation (2.7)

$$W_{MP} = \Sigma\phi^T Bt \tag{2.7}$$

Where, $\Sigma = (\phi^T B\phi + A)^{-1}$, Σ is the posterior covariance matrix for a Gaussian approximation to the posterior over weights centred at W_{MP}. The value of $A=\text{diag}(\alpha_1,\alpha_2.....\alpha_N)$, $B=\text{diag}(\beta_1,\beta_2.....\beta_N)$ where, $\beta_N=\sigma\{y(x_n)\}[1-\sigma\{y(x_n)\}]$. The above process is repeated until a convergence criterion is met. The hyperparameters, resulted by the above method, is used to estimate the target value for input feature vector. At the Gaussian distribution with a sharp peak, the variance is very small and given by equation (2.8)

$$p(W_{MP}|\alpha,\sigma^2) \approx \frac{1}{\sigma_{W_{MN}}} \tag{2.8}$$

Where, $\sigma_{W_{MN}}$ is a standard deviation of the posterior distribution. Then, the equation for $p(t|\alpha,\sigma^2)$ can be expressed as equation (2.9).

$$p(t|\alpha,\sigma^2) \approx p(t|W_{MP},\sigma^2) \times p(W_{MP}|\alpha)\sigma_{W_{MP}} \tag{2.9}$$

The first right side term of the above equation is the best fit likelihood for given hyperparameter σ^2 and if α is very high value then $p(W_{MP}|\alpha) = 1/\sigma_w$. In this case, the second term of the right side of equation (2.9) would be $\sigma_{W_{MN}}/\sigma_w$ which is defined as Occam factor. The evidence is the accuracy of the model for given data multiplied by the Occam factor, which describes the complexity of the model.

2.3 Simulation and test cases

2.3.1 Simulation Model

The authenticity of the proposed scheme has been tested by modelling standard IEEE 34 bus system in RTDS/RSCAD environment. The existing model of various equipment such as distribution line, distributed load, spot load, distribution transformer, and voltage regulator are given at 60 Hz frequency. Hence, in order to utilize the said standard system for the 50 Hz frequency, it is necessary to redesign all the equipment at 50 Hz frequency. This is achieved by modifying parameters of line, spot load, distributed load, and voltage regulator. Fig. 2.1 shows a single line diagram of IEEE 34 bus system modelled in RTDS/RSCAD environment.

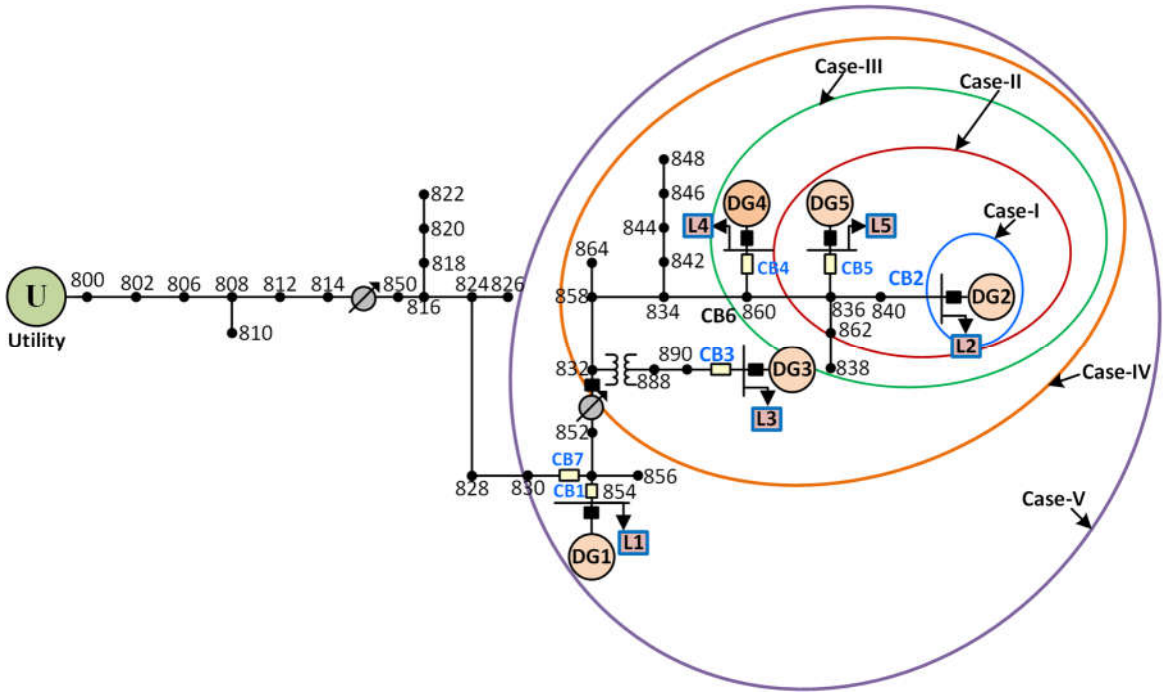


Fig. 2.1 IEEE 34 bus system with DGs.

As shown in Fig. 2.1, synchronous based DGs (DG1 to DG4) are connected at buses 854, 840, 890 and 860 whereas inverter-based DG (DG5) is connected at bus 836. The parameters of these DGs are given in Appendix - A.

2.3.2 Test cases

With reference to Fig. 2.1, islanding condition has been simulated by considering five different cases as shown in Table 2.1. Various types of islanding and non-islanding events have been generated by the varying source, load, and fault parameters. These events are shown in Table 2.2.

Table 2.1 Various cases considered for the simulation of islanding situation

Case	Event
I	Disconnection of DG2
II	Disconnection of DG2 and DG5
III	Disconnection of DG2, DG5 and DG4
IV	Disconnection of DG2, DG5, DG4 and DG3
V	Disconnection of DG2, DG5, DG4, DG3 and DG1

Table 2.2 List of non-islanding and islanding events

1. Non-islanding events	
1.1	LG, LL, LLL and LLLG fault on each phase at 4 different locations (25%, 50%, 75%, and 90% of the main feeder connected between node 858 and 840) from target DG with different loading condition.
1.2	LG, LL, LLL and LLLG fault on each phase at 3 different locations (25%, 50%, and 75% the connected between node 858 and 840) on adjacent feeder with different loading condition.
1.3	Sudden change in load on target DG from 25% to 150% of full load of target DG.
1.4	Sudden change in load on adjacent DG from 25% to 150% of full load.
1.5	Sudden change in power factor from 0.7 to 0.9 of the load on target DG with 25% to 150% load variation of target DG.
1.6	Switching of capacitive load connected at PCC of the target DG.
1.7	Switching of induction motor at PCC of the target DG.
1.8	Effect of LLLG fault on adjacent DG bus with various X/R ratios of the target DG.
1.9	Effect of sudden load change with change in network topology.
1.10	Addition of DGs with load.
1.11	Tripping of DG other than the target DG.
2. Islanding events	
2.1	Islanding at different loading condition; load ranges from 25% to 150% of full load of the target DG.
2.2	Islanding at a different power factor; load ranges from 150% to 25% of full load of the target DG.
2.3	Islanding at different loading condition with various power factor on other than target DG buses.
2.4	Islanding at 100% of the full load of target DG with various X/R ratios.
2.5	Islanding during a change in network topology.

The proposed scheme is basically a pattern recognition type scheme. In this scheme, initially, the classifier model is required to train for most possible events. Here, in this case, various datasets of islanding and non-islanding events as given in Table 2.2 are required to utilize for the training of the said classifier. In the proposed work, a large number of test cases have been generated for both the islanding and non-islanding events. Table 2.3 shows the event wise test cases generated for various islanding and non-islanding conditions. It is to be noted from Table 2.3 that total 483 test cases for both islanding and non-islanding events have been generated. Among these generated test cases, 114 test cases are the islanding situations, and 369 test cases are the non-islanding conditions.

Table 2.3 Generated test cases for islanding and non-islanding events.

Event		Parameter variation	Number of test cases generated
Non-islanding cases			
1	Faults on main feeder • LG, • LL, • LLL, • LLLG	 Load variation (2) × Phase (3) × location (4) Load variation (2) × Phase (3) × location (4) Load variation (2) × Phase (1) × location (4) Load variation (2) × Phase (1) × location (4)	 24 24 08 08
2	Faults on adjacent feeder • LG, • LL, • LLL, • LLLG	 Load variation (1) × Phase (3) × location (3) Load variation (1) × Phase (3) × location (3) Load variation (1) × Phase (1) × location (3) Load variation (1) × Phase (1) × location (3)	 09 09 03 03
3	Sudden load change on target DG	From 10% to 150 % in step of 10% (45)	45
4	Sudden power factor of load change on target DG	Load variation (2) × pf change (18)	36
5	Capacitive load switching at PCC of target DG	Load variation (30) × capacitor (1)	30
6	Induction motor load switching at PCC of target DG	Load variation (30) × induction motor (1)	30
7	Sudden addition of new DG with load	Adjacent DG (3) × adjacent DG load (5) × target DG load (2)	30
8	Sudden tripping of adjacent DG	Target DG load (2) × adjacent DG (3) × adjacent DG load (5)	30
9	Fault on adjacent feeder at various X/R ratio of target DG	Target DG load (2) × X/R ratio (5) × adjacent DG load (5)	50
10	Sudden load change with changed Network topology	From 10% to 150 % in step of 10% (30)	30
Islanding cases			
11	Islanding Cases with variable load on target DG and adjacent DG	Islanding (114)	114
Total cases generated			369+114 = 483

2.4 Proposed scheme

Fig. 2.2 shows working of the proposed scheme. Initially, the proposed classifier has been trained off-line using 40% of the total dataset (193 cases out of 483 total cases). Then, current samples for one cycle duration are acquired from the target DG. Here, a sampling frequency of 4 kHz (80 samples per cycle) for a 50 Hz system is used. Hence, each simulation case of islanding/non-islanding event comprises 240 samples (3 phases × 80 = 240) of currents. Further, the phasor values of the acquired current signals have been obtained by utilizing modified discrete Fourier transform algorithm. These phasor quantities of currents are then converted into sequence components using equation (2.10).

$$\begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix} = \frac{1}{3} \times \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \times \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{2.10}$$

Where, I_0, I_1, and I_2 are zero, positive and negative sequence component of current, respectively. The complex operator $\alpha = 1\angle 120^\circ$ and I_a, I_b and I_c are currents of phase *a*, *b,* and *c*, respectively. During the above conversion, the collected samples of currents are converted into 240 samples of sequence components of currents (each component has 80 samples).

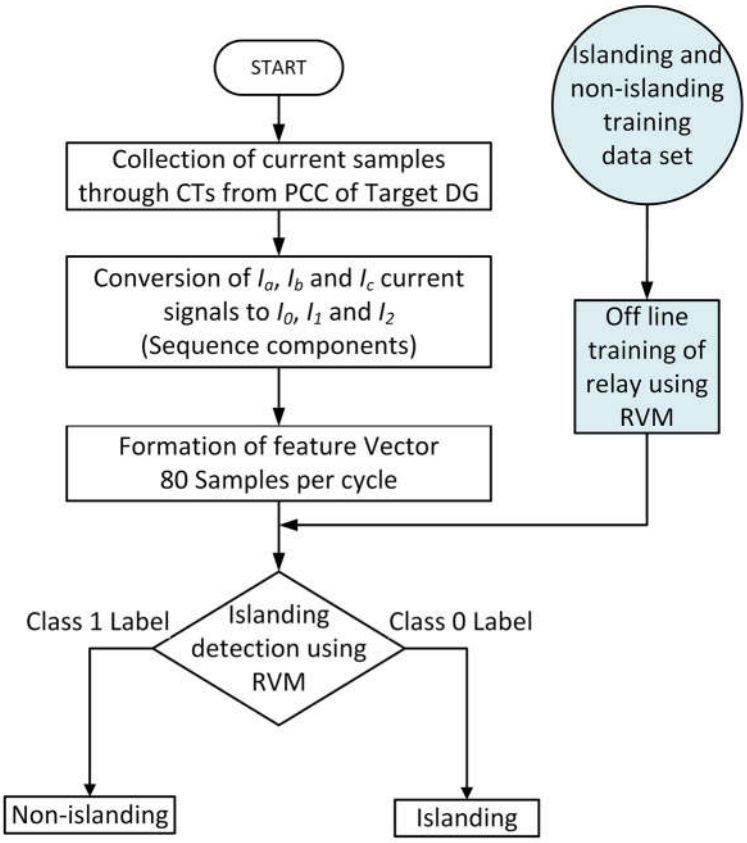


Fig. 2.2 Working of the proposed scheme.

However, the proposed scheme utilizes I_2 only for the formation of a feature vector. The reason for utilizing I_2 for feature vector formation instead of all sequence components of currents or voltages are explained in the next section. A vector consisting of an islanding/non-islanding case, having 80 samples in one raw is used directly as an input to RVM classifier. Therefore, for 193 training data cases, the feature vector having a dimension of 193_{row} (train cases) × 80_{column} (samples of I_2) and a target vector having a dimension of $193_{row} \times 1_{column}$ is formed. Table 2.4 shows the process of formation of feature vectors for training data cases. In the same way, the remaining dataset (483-193=290) is considered for testing of the proposed algorithm. Hence, the dimension of the feature vector for testing dataset is of 290_{row} (test cases) × 80_{column}

(samples of I_2). The output of the proposed classifier is either '1' or '0' which indicates "non-islanding event" or "islanding situation", respectively.

Table 2.4 Formation of feature vector for training datasets.

Various simulation Cases	Samples	Target
Non-islanding Case 1	$1_{row}\times80_{column}$	1
Non-islanding Case 2	$2_{row}\times80_{column}$	1
||	||	1
||	||	||
||	||	||
||	||	||
||	||	||
Non-islanding Case 140	$140_{row}\times80_{column}$	1
Islanding Case 1	$1_{row}\times80_{column}$	0
Islanding Case 2	$2_{row}\times80_{column}$	0
||	||	||
||	||	||
||	||	||
Islanding Case 53	$53_{row}\times80_{column}$	0
Total training cases193	$193_{row}\times80_{column}$	1 or 0

2.5 Training of RVM classifier

2.5.1 Training sequence

The sequence of training to be carried out for the proposed RVM classifier is shown in Fig. 2.3. Initially, as shown in Fig. 2.3, feature vector for the selected training dataset along with their class label as per equation (2.1) are given as input to the proposed RVM based classifier. The feature vector is formed from 40% of the total data by utilizing negative sequence component of current only. On the other hand, there are only two class labels i.e. '1' indicates non-islanding whereas '0' refers to islanding event. Afterwards, the said training dataset has been initialized with weight as given by equation (2.2). Once the training dataset is obtained, the next step is to determine the optimal parameter settings of RVM. In this process, the type of kernel function and the width parameter w must be decided. Therefore, proper kernel function (in this case Gaussian function) is selected for the prediction of input training dataset as per equation (2.3). In the proposed RVM classifier, a generalized linear model with logistic sigmoid function, as per equation (2.4) and (2.5), is selected as RVM classifier model. Thereafter, a separable Gaussian prior, with a distinct hyperparameter for each weight is calculated. The process of calculation of weights and obtaining the marginal likelihood for classification is described in [167]. Thereafter, the most suitable marginal likelihood for the given hyperparameter is determined.

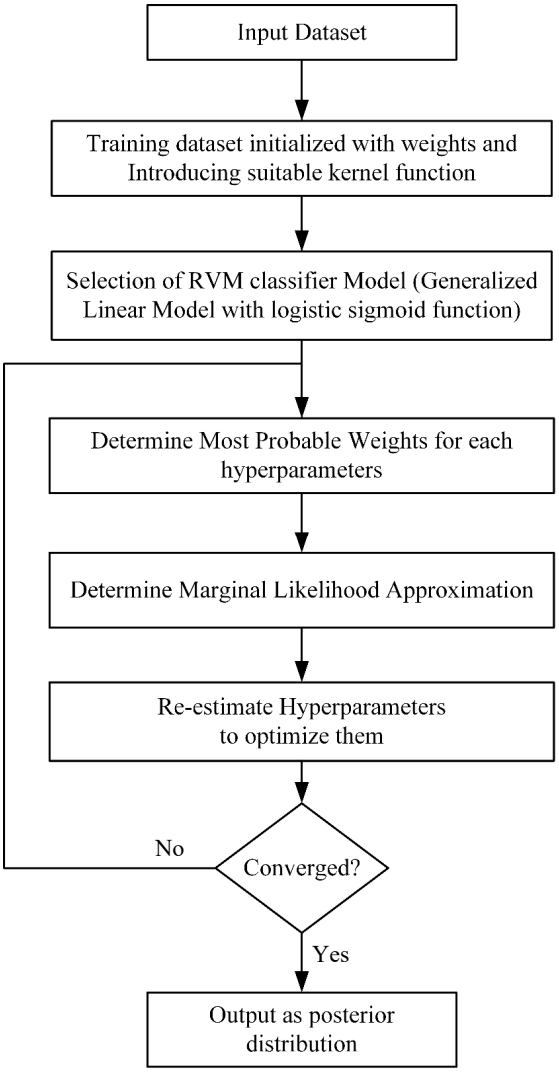


Fig. 2.3 Algorithm for training sequence of the proposed RVM classifier.

The re-estimation of hyperparameter is further carried out to optimize its value. This process is repeated until a convergence criterion is met. The hyperparameters, as resulted by the above process, is used to estimate the target value for input feature vector. The posterior distribution over the weight from Bayes rule and a standard deviation of the posterior distribution is calculated. The RVM training by such a method will give the training vector associated with the remaining non-zero weights which are called as "relevance vectors." Finally, testing of the given dataset (different from the dataset used in training process) has been carried out directly on the already trained RVM classifier model.

2.5.2 Elimination of noise during training of RVM classifier

In the proposed scheme, various simulations containing islanding situation and non-islanding events have been carried out on the standard IEEE-34 bus network. This system is

completely an unbalance system which replicates practical scenario of an existing distribution network. It has been observed from the published literature [169] that the negative sequence component of current is already present during normal condition. It varies in the range of 2% to 10% with respect to positive sequence component of the current. This is due to inequality in load currents in all phases. In the proposed scheme, the negative sequence component of current is used to formulate the feature vector. The samples of three-phase currents are collected with the help of CTs. These currents are converted into phasor values with the help of Modified Discrete Fourier Transform (MDFT) algorithm [170] available in the digital/numerical relay installed at the terminal of DG. Finally, these phasor values are converted into sequence components of current by digital/numerical relay using equation (2.10). The digital/numerical relay consists of signal conditioning block which contains isolation transformer, surge protection circuit and Anti-Aliasing Filter (AAF). Isolation transformer provides the electrical isolation whereas, surge protection circuit gives protection to the digital component against transients and spikes. AAF is a Low Pass Filter (LPF) that blocks the unwanted frequency component/noise [171]. Further, it also avoids aliasing error. Therefore, chances of noise in the samples are very rare. Even though it exists in the training data, training of the proposed classifier has been done using data which contains noise. Hence, accuracy given by the proposed RVM based classifier has not been altered.

2.6 Selection of signal for feature vector formation

In section 2.3, the development of simulation model of IEEE 34 node network has been thoroughly described. As mentioned in Table 2.1, different cases of islanding involving various DGs are possible. Among the various cases of islanding, the islanding situation involving only DG2 considered in the presented work. At the same time, Table 2.2 shows the possible islanding and non-islanding events with respect to DG2. Further, Table 2.3 shows the event wise test cases generated for various islanding and non-islanding conditions considering DG2 as a target DG. Fig. 2.4 shows the waveform of non-islanding event (LLL fault at 50% fault location on main feeder) and islanding situation (islanding with +10% power mismatch) generated by modelling IEEE 34 bus test system in RTDS/RSCAD environment for DG2 as a target DG. These signals of currents and voltages are acquired from the terminal of target DG at a sampling frequency of 4 kHz. In this figure, the switching instance is 0.053sec. As the captured signals of currents and voltages contain may contain noise, higher order harmonics and decaying DC which can affect the performance of the presented scheme. Hence, in order to eliminate these components and to obtained phasor values of the acquired signals, MDFT based phasor computation as discussed in [170] has been carried out. Thereafter, utilizing these

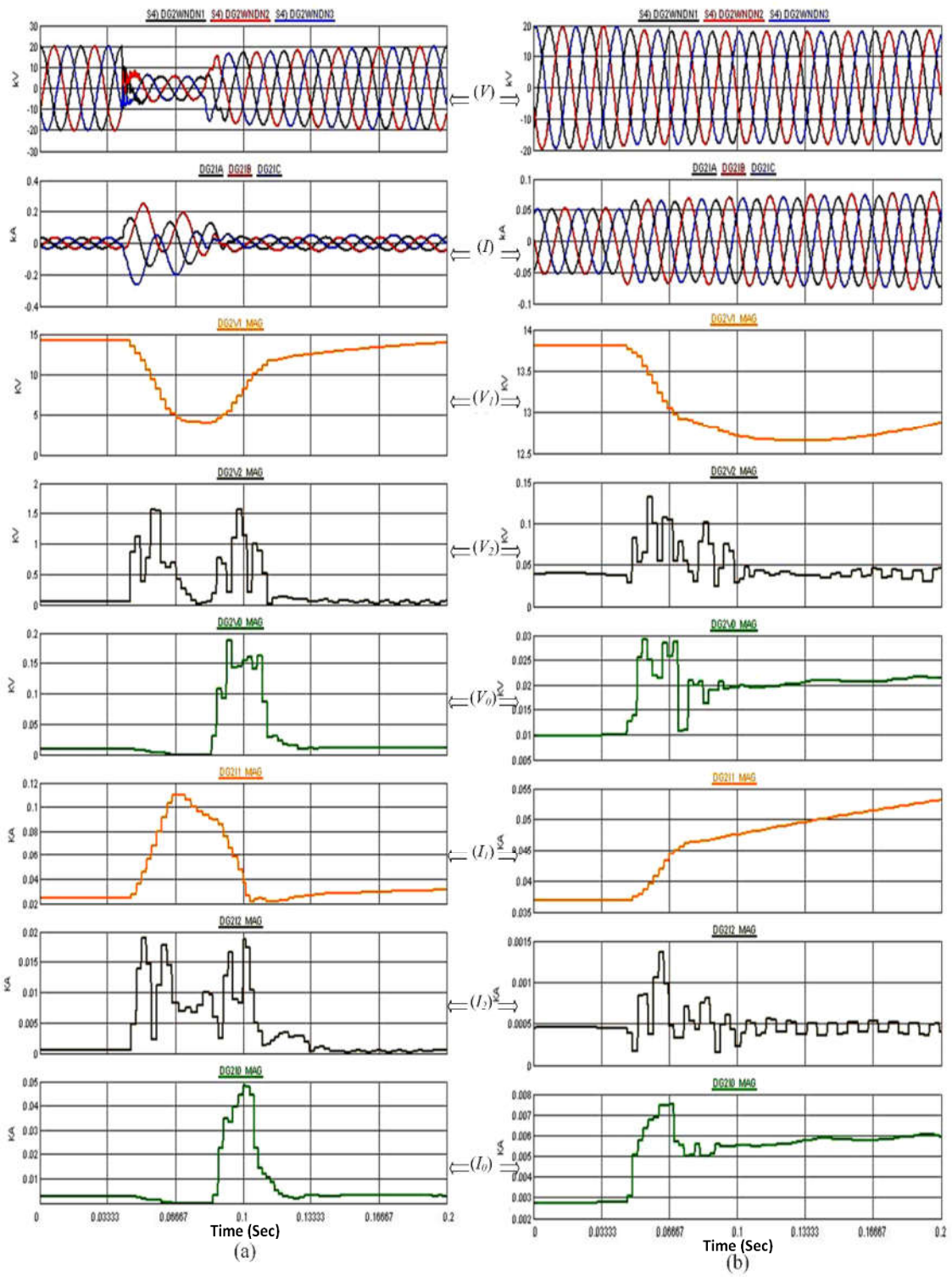


Fig. 2.4 RTDS/RSCAD captured waveform of islanding and non-islanding event (a) non-islanding event (b) islanding event.

phasor values, the sequence components of current and voltages have been calculated. Waveforms of various signals such as three-phase currents (I_a, I_b, and I_c), three phase voltages (V_a, V_b, and V_c), sequence components of currents (I_0, I_1 and I_2) and voltages (V_0, V_1 and V_2) are shown in Fig. 2.4. These signals can be used for formation of feature vectors as significant

variations in the patterns/signatures have been observed during islanding and non-islanding events. In order to formulate feature vectors, sequence components of currents (I_0, I_1, and I_2) and their combinations with each other (I_0+I_1, I_0+I_2, or I_1+I_2 or I_0+I_1+I_2) can be used. Extensive simulations have been carried out by considering various signals/combination of signals with a varying width parameter of RVM and percentage of the training dataset with respect to the total dataset. For each signal/combinations of the signal, discrimination accuracy between islanding situation and the non-islanding event has been obtained by varying the percentage of the training dataset from 10% to 90% of the total dataset. In the presented work, the results obtained during various test cases of islanding and non-islanding events as mentioned in Table 2.3 have been utilized. The output of the presented technique in terms of accuracy is shown in Table 2.5. It is to be noted from Table 2.5 that various input features of sequence components of current and/or voltage signals have been utilized to develop feature vector for the proposed RVM classifier. The width of the proposed RVM model is varied from 0.00005 to 0.5 in order to obtain optimal value of accuracy. It is to be noted from Table 2.5 that the negative sequence component of current (I_2) gives better accuracy in classifying islanding situations with non-islanding events as compared to other features of sequence components of current or/and voltage. Though the accuracy obtained by other feature signals is high as compared to I_2, their corresponding training dataset are also high. The obtained maximum efficiency in discrimination between islanding and non-islanding events with varying training dataset and width by different combination of signals are extracted in Table 2.6. It has been observed from Table 2.6 that the maximum accuracy of the order of 98.62% has been achieved by utilizing I_2 with 40% of the total data as training data. It is to be further noted from Table 2.6 that as the training dataset increases, accuracy of RVM classifier also increases. However, the increase in accuracy is marginal after a certain percentage of training dataset. Furthermore, as shown in Table 2.6, I_2 gives the maximum accuracy (98.62%) with width (w) = 0.003 and 40% of the total data as training data. This clearly indicates its ability to provide effective discrimination between islanding and non-islanding events. Therefore, I_2 is selected for the formation of the feature vector.

Table 2.5 Accuracy (%) of RVM classifier for various input feature at different percentage of training dataset.

Sr. No.	Feature	Width parameter for RVM	Training data as percentage of total dataset								
			10%	20%	30%	**40%**	50%	60%	70%	80%	90%
1	I_0	0.00005	51.16	68.37	45.58	41.40	39.07	42.79	AT	AT	AT
		0.00050	51.16	85.12	88.84	89.30	92.56	94.88	AT	AT	AT
		0.00500	75.35	82.79	97.21	99.07	93.95	99.07	100.00	AT	AT
2	I_1	0.00005	51.16	53.49	45.58	41.40	39.07	42.79	47.44	50.23	51.63
		0.00050	51.16	62.79	73.95	41.40	39.07	86.05	47.44	50.23	51.63
		0.00500	54.88	66.51	69.30	66.98	71.16	78.14	90.23	92.09	92.09
3	I_2	0.00005	51.16	54.88	45.58	41.40	39.07	42.79	47.44	50.23	51.63
		0.00050	51.16	66.51	76.28	41.40	39.07	42.79	47.44	50.23	51.63
		0.00300	86.98	94.88	97.60	**98.62**	96.74	96.28	99.53	100.00	100.00
4	$I_0 + I_1$	0.00500	51.16	80.93	46.98	45.58	41.86	48.84	53.95	58.14	59.53
		0.05000	65.12	81.86	95.35	95.81	96.28	96.28	99.53	99.53	99.53
		0.50000	76.28	78.60	89.77	93.49	AT	AT	AT	AT	AT
5	$I_0 + I_2$	0.00500	73.02	AT	92.81	94.52	95.21	93.84	99.32	96.58	96.58
		0.05000	92.56	AT	97.60	AT	AT	AT	AT	AT	AT
		0.50000	92.09	94.42	94.61	AT	AT	AT	AT	AT	AT
6	$I_1 + I_2$	0.00500	52.09	56.74	58.14	64.38	68.07	70.59	68.06	68.75	70.83
		0.05000	65.58	92.09	94.42	93.15	92.44	94.96	AT	AT	AT
		0.50000	84.65	85.58	94.42	AT	AT	AT	AT	AT	AT
7	$I_0 + I_1 + I_2$	0.00500	51.16	85.12	47.44	44.19	52.94	50.42	47.06	42.02	43.70
		0.05000	65.58	87.91	96.28	95.35	94.96	94.96	100.00	100.00	100.00
		0.50000	85.12	85.12	89.30	93.02	AT	AT	AT	AT	AT
8	V_0	0.00050	51.16	80.93	45.58	41.40	AT	50.52	44.33	35.05	37.11
		0.00500	80.47	64.19	74.42	77.67	AT	74.23	79.38	94.85	94.85
		0.05000	78.14	88.84	96.74	97.67	97.21	92.78	94.85	96.91	96.91
9	V_1	0.00500	51.16	53.95	45.58	41.40	39.07	42.79	47.44	50.23	51.63
		0.05000	51.16	61.40	73.02	41.40	39.07	42.79	47.44	50.23	51.63
		0.50000	70.23	80.93	81.40	89.77	93.02	94.88	96.74	100.00	100.00
10	V_2	0.00500	51.16	54.42	45.58	41.40	39.07	42.79	47.44	50.23	51.63
		0.05000	51.16	66.51	77.67	41.86	40.00	43.72	50.23	53.49	54.88
		0.50000	92.56	93.43	94.18	95.17	94.56	95.23	99.53	100.00	100.00
11	$V_0 + V_1$	0.00500	51.16	53.95	45.58	41.40	39.07	42.79	47.44	50.23	51.63
		0.05000	51.16	61.40	73.02	41.40	39.07	42.79	47.44	50.23	51.63
		0.50000	69.77	80.00	81.40	90.23	89.77	94.88	96.74	100.00	100.00
12	$V_0 + V_2$	0.00500	51.16	54.42	45.58	41.40	39.07	42.79	47.44	50.23	51.63
		0.05000	51.16	66.98	77.67	41.86	40.00	43.72	50.23	53.49	54.88
		0.50000	92.56	96.28	96.74	96.28	98.60	98.60	99.53	100.00	100.00
13	$V_1 + V_2$	0.00500	51.16	53.49	45.58	41.40	39.07	42.79	47.44	50.23	51.63
		0.05000	51.16	60.00	66.98	41.40	39.07	42.79	47.44	50.23	51.63
		0.50000	62.33	77.21	83.72	90.70	91.63	97.21	90.23	92.09	92.09
14	$V_0 + V_1 + V_2$	0.00500	51.16	53.49	45.58	50.68	43.84	43.15	44.52	42.47	43.84
		0.05000	51.16	60.00	66.98	50.68	43.84	43.15	44.52	42.47	43.84
		0.50000	61.86	76.74	83.26	90.70	91.63	96.74	88.37	92.09	92.09
15	$V_0 + I_0$	0.00050	51.16	77.60	45.58	41.40	39.07	42.79	47.44	50.23	51.63
		0.00500	80.93	63.72	65.87	70.06	AT	70.10	AT	AT	AT
		0.05000	83.72	88.84	97.01	97.01	94.12	92.78	97.22	97.92	97.87
		0.50000	66.98	AT	82.63	84.43	AT	AT	AT	AT	AT
16	$V_1 + I_1$	0.00500	51.16	53.95	45.58	41.40	39.07	42.79	47.44	50.23	51.63
		0.05000	51.16	61.40	73.02	41.40	39.07	42.79	47.44	50.23	51.63
		0.50000	70.23	80.93	81.40	89.77	93.02	94.88	96.74	100.00	100.00
17	$V_2 + I_2$	0.00500	51.16	54.42	45.58	41.40	39.07	42.79	47.44	50.23	51.63
		0.05000	51.16	66.51	77.67	41.86	40.00	43.72	50.23	53.49	54.88
		0.50000	92.56	96.28	96.28	95.81	98.60	98.60	99.53	100.00	100.00

*AT = Abnormal Termination of program.

Table 2.6 Maximum accuracy of the proposed scheme at different percentages of training sets with its corresponding value of width.

Sr. No.	Feature	Width (w)	Accuracy (%) at different percentage of training data with respect to total dataset								
			10%	20%	30%	40%	50%	60%	70%	80%	90%
1	I_0	0.005	75.35	82.79	97.21	99.07	93.95	99.07	100.00	AT*	AT
2	I_1	0.005	54.88	66.51	69.30	66.90	71.16	78.14	90.23	92.09	92.09
3	I_2	0.003	86.98	94.88	97.60	98.62	96.74	96.28	99.53	100.00	100.00
4	$I_0 + I_1$	0.05	65.12	81.86	95.35	95.81	96.28	96.28	99.53	99.53	99.53
5	$I_0 + I_2$	0.005	73.02	AT	92.81	94.52	95.21	93.84	99.32	96.58	96.58
6	$I_1 + I_2$	0.05	65.58	92.09	94.42	93.15	92.44	94.96	AT	AT	AT
6	$I_0 + I_1 + I_2$	0.05	65.58	87.91	96.28	95.52	94.96	94.96	100.00	100.00	100.00
7	V_0	0.05	78.14	88.84	96.74	97.67	97.21	92.78	94.85	96.91	96.91
8	V_1	0.5	70.23	80.93	81.40	89.66	93.02	94.88	96.74	100.00	100.00
9	$V2$	0.5	92.56	93.43	94.18	95.17	94.56	95.23	99.53	100.00	100.00
10	$V_0 + V_1$	0.5	69.77	80.00	81.40	90.23	89.77	94.88	96.74	100.00	100.00
11	$V_0 + V_2$	0.5	92.56	96.28	96.74	96.28	98.60	98.60	99.53	100.00	100.00
12	$V_1 + V_2$	0.5	62.33	77.21	83.72	90.70	91.63	97.21	90.23	92.09	92.09
13	$V_0 + V_1 + V_2$	0.5	61.86	76.74	83.26	90.70	91.63	96.74	88.37	92.09	92.09

*AT = Abnormal Termination of program.

2.7 Result and discussion

2.7.1 Discrimination between islanding situation and non-islanding event

The performance of the proposed classifier has been validated on various islanding and non-islanding cases. Testing of the proposed classifier has been carried out on an already trained RVM classifier in which the width has been taken as 0.003. The simulation results in terms of cases classified correctly and incorrectly along with discrimination accuracy are shown in Table 2.7. Moreover, total numbers of cases along with a break-up of non-islanding events are also shown in Table 2.7. It is to be noted from Table 2.7 that the proposed RVM based classifier is capable to identify islanding situations with an accuracy of 98.36%. This shows the capability of the proposed classifier to detect islanding situation accurately. Conversely, it gives an accuracy of 98.69% during non-islanding events which show its stability against nuisance tripping. In addition, the proposed RVM based classifier provides very high overall accuracy of 98.62% for all islanding and non-islanding events. Discrimination between islanding situation at different percentages of power mismatches and non-islanding event at varying load conditions has been evaluated by the proposed classifier. In the presented work, various simulation test cases of sudden load change as mentioned in Table 2.3 have been generated. As this is one of the critical non-islanding events, in all these cases, the value of I_2 has been investigated. By analyzing all those cases, it has been found that the value of I_2 for sudden load change remains always more than 18 A. Similarly, the same

Table 2.7 Discrimination accuracy given by the proposed classifier during islanding & non-islanding conditions.

Sr. No.	Various events	Test Cases	Cases classified correctly	Cases classified incorrectly	Accuracy (%)
Islanding Events		61	60	1	98.36
Non-islanding Events					
1	Faults on main feeder	40	40	0	100.00
2	Faults on adjacent feeder	15	14	1	93.33
3	Sudden load change on target DG bus	28	28	0	100.00
4	Sudden power factor of load change on target DG bus	20	20	0	100.00
5	Capacitive load switching at PCC of target DG	19	19	0	100.00
6	Induction motor load switching at PCC of target DG	19	19	0	100.00
7	Sudden addition of new DG with load	19	19	0	100.00
8	Sudden tripping of adjacent DG	19	18	1	94.74
9	Fault on adjacent feeder at various X/R ratio of target DG	31	31	0	100.00
10	Sudden load change with changed Network topology	19	18	1	94.74
All Non-islanding Events		229	226	3	98.69
Overall Result (Islanding + Non-islanding)		290	286	4	98.62

analysis has been carried out for different cases of islanding with various percentage mismatch between load and generation. By analyzing the islanding cases, it has been found that the maximum value of I_2 for islanding with various percentage mismatch between load and generation remains well below 5.0 A. The waveform of the maximum value of I_2 during islanding and sudden load change with different mismatches between load and generation are plotted in Fig. 2.5. It is to be noted from Fig. 2.5 that a clear separation between islanding and sudden load change cases have been achieved. Moreover, from Fig. 2.5, it could be said that the proposed scheme is able to distinguish between islanding situation and critical non-islanding event such as sudden load change distinctly at different values of power mismatches.

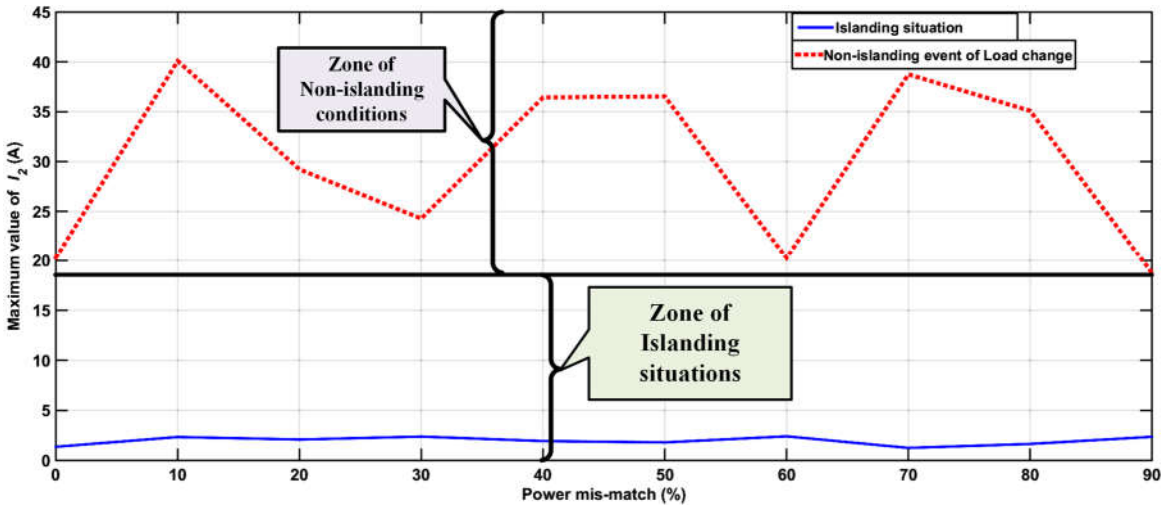


Fig. 2.5 Trend of maximum value of I_2 during islanding and non-islanding events.

2.7.2 Change in X/R ratio

The performance of the proposed scheme has been evaluated on eight different values of the X/R ratio (8, 10, 16, 20, 24, 30, 32 and 40) of the target DG. For a non-islanding event with varying X/R ratio, the three-phase to ground (LLLG) fault on the adjacent feeder (connected between bus 832 and bus 840 in Fig. 2.1) near the target DG has been simulated. The simulation results in terms of I_2 for non-islanding events for two different values of the X/R ratio of the target DG are shown in Fig. 2.6.

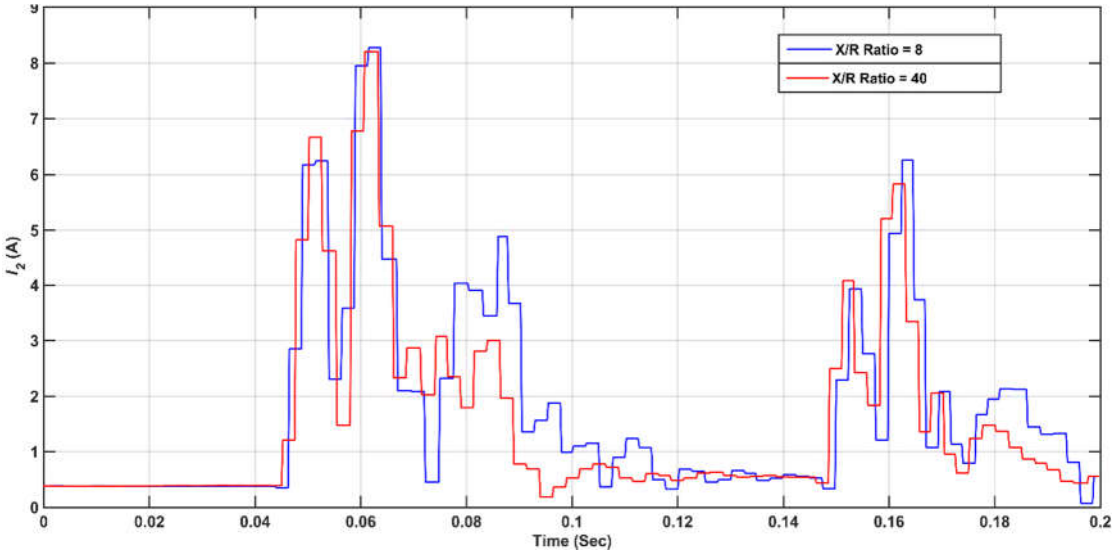


Fig. 2.6 Pattern of I_2 during LLLG fault at various X/R ratio.

It has been observed from Fig. 2.6 that the patterns of I_2 during a non-islanding event in case of two different values of the X/R ratio of the target DG remain almost same. As these similar types of patterns are given as input to the proposed classifier, it is able to classify both events as a non-islanding condition. This clearly indicates that the proposed scheme is immune to the change in X/R ratio of the target DG and hence, avoids nuisance tripping during such type of critical non-islanding events.

2.7.3 Change in network topology

The load on the distribution feeder is continuously changing with respect to time. Hence, the usual practice is to open few sectionalizing switches and close some of the tie switches. This is widely known as reconfiguration of the network. This is required for the distribution network in order to reduce distribution line losses and also to improve the voltage profile. In the proposed IEEE 34 bus system, network reconfiguration is simulated between bus 816 and bus 852. The reason for adopting reconfiguration for the above two buses is the maximum voltage drop that occurred on the line connected between the said two buses. Fig.

2.7 shows the single line diagram of IEEE 34 bus network in which a new distribution line is connected between bus 816 and bus 852. In order to maintain the radial structure of the network during reconfiguration, a tie-switch is connected between bus 852 and bus 854. This tie-switch remains in closed condition under normal operation (without change in network topology) whereas, it becomes open during network reconfiguration. Another tie-switch which is installed on the newly configured line (connected between bus 816 and bus 852) follows reverse operation with reference to the tie-switch connected in the old feeder. Fig. 2.8 shows the simulation results in terms of I_2 during normal condition (Normal route) as well as in case of network reconfiguration (Alternate route) for a specific loading condition.

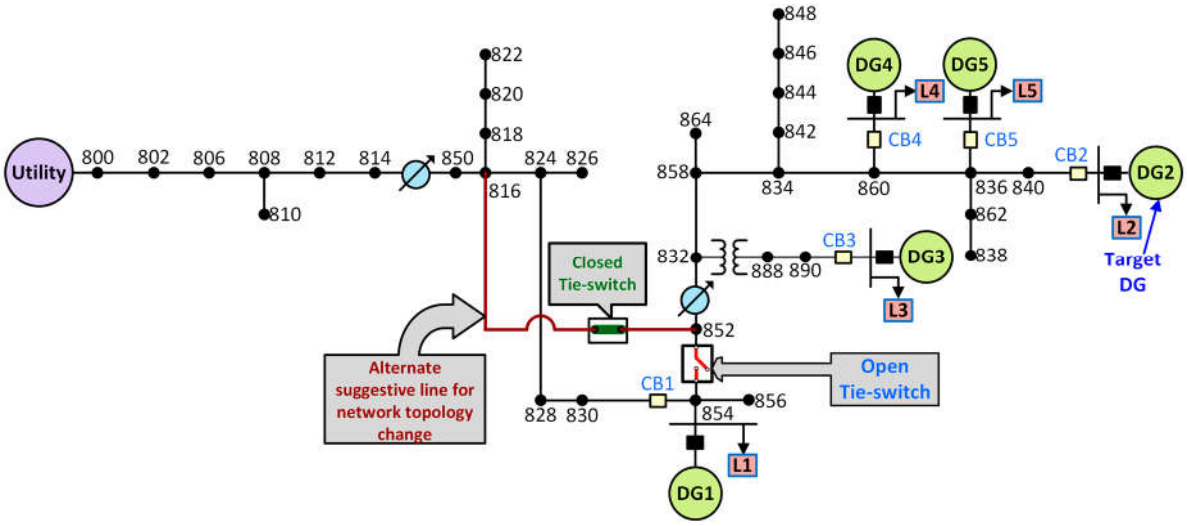


Fig. 2.7 Network topology change configuration in IEEE 34 bus system.

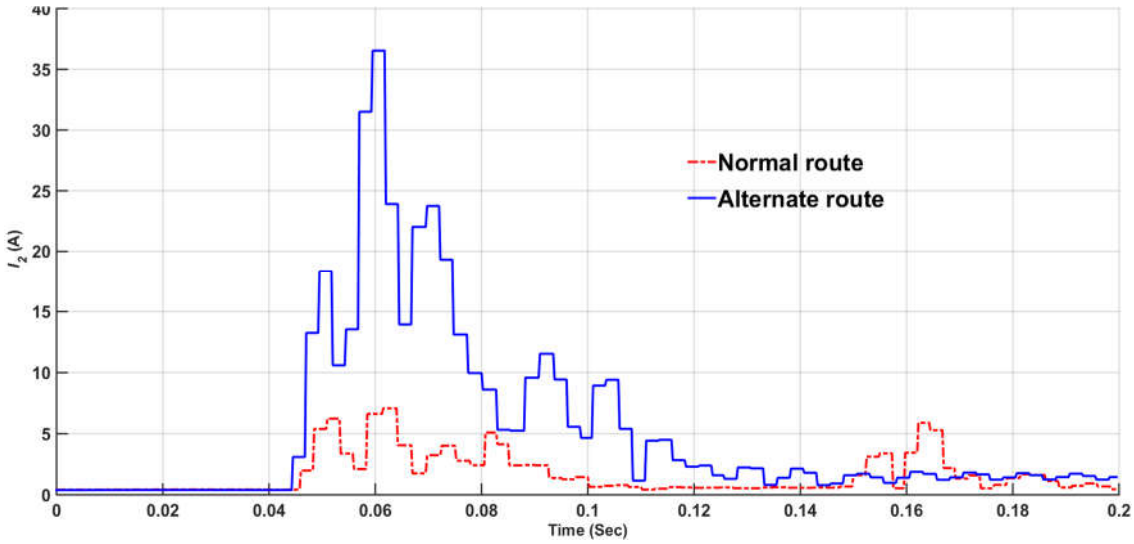


Fig. 2.8 Comparison of effect of network topology change.

It is to be noted from Fig. 2.8 that the signature of I_2 is almost similar for the previous cases. Hence, the proposed RVM based classifier is able to classify the above two events as non-islanding conditions.

2.7.4 Islanding at different power mismatches

The performance of the proposed scheme has been evaluated during islanding situation at two different values of power mismatches i.e. (i) perfect power balance situation (ii) 5% power mismatch at the target DG. The simulation results are shown in Fig. 2.9. It has been observed from Fig. 2.9 that the proposed RVM based scheme is able to detect islanding situation at different values of power mismatches including perfect power balance situation. This is due to the fact that the signatures of feature vectors have similar patterns for islanding situation with different values of power mis-matches.

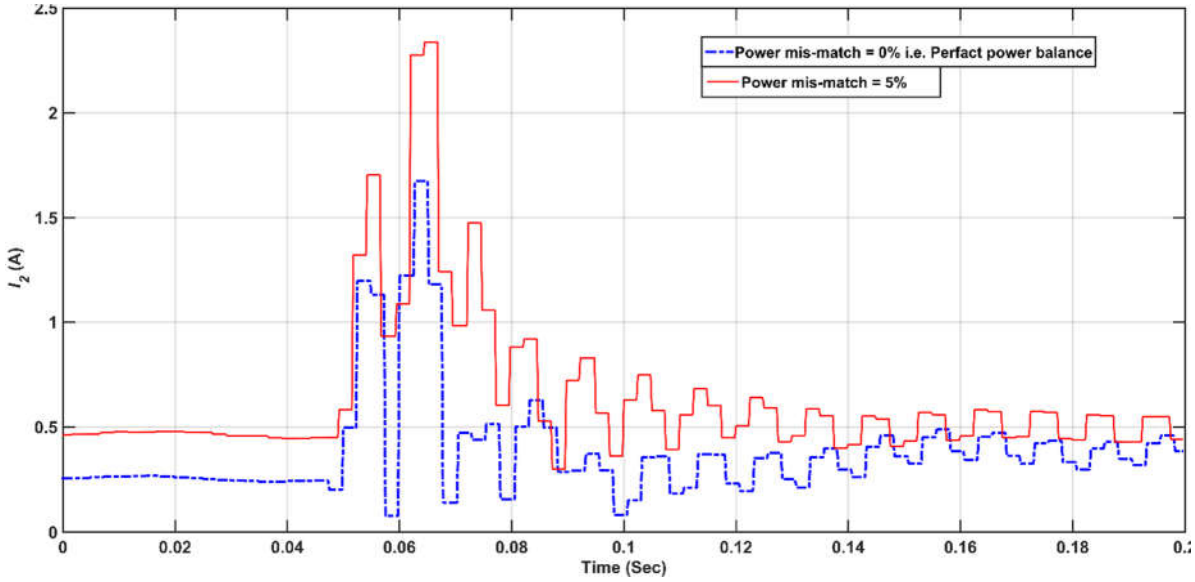


Fig. 2.9 Pattern of I_2 for various power mis-match during islanding.

2.7.5 Comparative evaluation of the proposed classifier with existing classifiers

The performance of the proposed islanding detection scheme is compared with the islanding detection schemes based on SVM and random forest (RF) classifier. The overall accuracy of the all three islanding detection schemes is given in Table 2.8. It has been observed from Table 2.8 that the proposed RVM based scheme gives an overall accuracy of 98.62% compared to 87.58% and 92.76% accuracy given by SVM and RF based scheme, respectively. Hence, the proposed scheme is superior in distinguishing islanding and non-islanding events than SVM and RF based schemes. In addition, the proposed scheme gives an accuracy of 98.69%, whereas SVM and RF based scheme provides an accuracy of 86.90% and 92.14%

during non-islanding events. This confirms the stability of the proposed scheme in case of critical non-islanding events.

Table 2.8 Comparative evaluation of the proposed scheme with other schemes with respect to accuracy.

Events	Test Cases	RF			SVM			RVM		
		Cases classified correctly	Cases classified incorrectly	Accuracy (%)	Cases classified correctly	Cases classified incorrectly	Accuracy (%)	Cases classified correctly	Cases classified incorrectly	Accuracy (%)
All Non-islanding Events	229	221	18	92.14	199	30	86.90	226	3	98.69
Islanding Events	61	59	3	95.08	55	6	90.16	60	1	98.36
Overall result	290	269	21	92.76	254	36	87.58	286	4	98.62

Furthermore, the accuracy given by the proposed scheme during islanding situation is 98.36% compared to 90.16% and 95.08% accuracy given by SVM and RF based scheme. Therefore, the proposed scheme is able to identify islanding situation accurately compared to other classifiers. Moreover, comparative analysis of the proposed classifier with other existing classifiers like SVM and RF has been performed with respect to the training time required to train the classifier model and testing time to classify the given input feature as islanding and non-islanding event. The simulation results are shown in Table 2.9.

Table 2.9 Comparative analysis of the proposed classifier with other existing classifiers with respect to training and testing time.

Training Percentage of Dataset	RVM		SVM		RF	
	Training Time (second)	Testing Time (second)	Training Time (second)	Testing Time (second)	Training Time (second)	Testing Time (second)
10%	0.1005	0.0011	0.0029	0.0032	0.1053	0.0081
20%	0.2012	0.0012	0.0038	0.0037	0.2107	0.0090
30%	0.2691	0.0014	0.0052	0.0041	0.3634	0.0109
40%	0.2811	0.0016	0.0068	0.0048	0.6726	0.0118
50%	0.3026	0.0016	0.0074	0.0049	0.6675	0.0126
60%	0.4178	0.0017	0.0082	0.0054	0.8492	0.0128
70%	0.7324	0.0017	0.0089	0.0056	1.1089	0.0130
80%	0.9100	0.0018	0.0095	0.0069	1.4570	0.0139
90%	1.2300	0.0019	0.0098	0.0068	1.5553	0.0166

It has been observed from Table 2.9 that as the percentage training dataset increases the time taken by all the classifiers increases. The training time required by the proposed

classifier is higher than the SVM based classifier, but lower than the RF based classifier. However, though the training time of the proposed classifier is higher than the SVM based classifier, it is not going to affect the performance of the proposed classifier. This is due to the fact that the training process is an off-line process. Conversely, it has been observed from Table 2.9 that the testing time of the proposed classifier is the lowest among the two existing classifiers. Therefore, as the testing process is an online process, the classification process in discriminating islanding and non-islanding event is very fast. Hence, the performance of the proposed classifier is superior to the existing classifiers. Additionally, in order to compare the classification property of an RVM and an SVM, the variation of relevance vectors and support vectors with the change in the number of percentage of training dataset has been examined. Table 2.10 shows the comparative evaluation of the proposed RVM based classifier with SVM based classifier with respect to a number of RVs and SVs.

Table 2.10 Comparative analysis of the proposed RVM based classifier with SVM based classifier with respect to number of RVs and SVs.

Sr. No.	Training Dataset	No. of RVs for RVM classifier	No. of SVs for SVM classifier
1	10%	4	14
2	20%	5	28
3	30%	5	47
4	40%	8	66
5	50%	8	79
6	60%	9	90
7	70%	11	109
8	80%	12	119
9	90%	14	133

It can be observed from Table 2.10 that even though the numbers of RVs/SVs increase linearly while training the data with the RVM and SVM, the number of RVs are always less than that of SVs. Also, the rate at which the number of RVs increases is also lower than that of SVs. Hence, the sparse property of the RVM makes RVs to sample in each class, which is far from the hyperplane compared to SVs, which are near the hyperplane to outline classifier model.

2.7.6 Effect of the entirely different network on the proposed classifier

In order to further evaluate the performance of the proposed scheme on an entirely different network, an existing Indian power distribution network, as given in [118], has been considered. A total of 80 cases consisting of islanding and non-islanding events have been

generated. These cases are directly used for testing the proposed classifier. The simulation results given by the proposed classifier are shown in Table 2.11. It is to be noted from Table 2.11 that the proposed RVM based classifier is able to provide an accuracy of 93.75%, which is equally compatible with the accuracy given by the same classifier for IEEE 34-bus network.

Table 2.11 Accuracy given by the proposed classifier for entirely different power distribution network

Events	Test Cases	Proposed RVM classifier based scheme		
		Cases classified correctly	Cases classified incorrectly	Accuracy (%)
All Non-islanding Events	55	52	3	94.54
Islanding Events	25	23	2	92.00
Overall result	80	75	5	93.75

2.8 Summary

In this chapter, a new islanding detection technique based on RVM classifier is presented. The proposed scheme utilizes I_2 for discrimination between islanding situation and non-islanding events. Different types of islanding and non-islanding events have been generated by modelling IEEE 34 bus network using RTDS/RSCAD software package. The proposed scheme gives an overall discrimination accuracy of more than 98%, which shows its effectiveness in classifying islanding and non-islanding conditions accurately. Furthermore, the validity of the proposed scheme has been tested during islanding situation at different values of power mismatches including perfect power balance situation. Furthermore, it remains immune to change in network configuration/entirely different network and X/R ratio of various types of DGs. At the end, comparative evaluation of the proposed scheme with the existing schemes shows its superiority in terms of accuracy, testing time and number of RVs.

Nevertheless, this is one of the patterns recognition based technique in which a large number of test cases are required to generate. However, this technique requires only 40% of the total dataset for the training of the classifier modal. In the case of simulation, it is possible to generate a large number of test cases covering all aspects of islanding and non-islanding situations. But, in real time application, it is not feasible to cover all the possibilities of islanding and non-islanding events. Therefore, it has been decided to develop more practicable technique.

Chapter 3

Islanding Detection Technique based on Sequence Components of Voltage

3.1 Introduction

This chapter presents a new islanding detection technique based on islanding discrimination factor which is derived from the Superimposed Components of Voltages (SCVs). The value of IDF is calculated by utilizing the acquired voltage signals from the terminal of DGs. In this work, various islanding and non-islanding events with varying power mismatches have been simulated on two different widely used networks namely (i) IEEE 34 bus network and (ii) IEC61850-7-420 Micro-Grid model using RTDS/RSCAD software. The authenticity of the presented scheme has been verified on diversified islanding and non-islanding cases, generated from the above two models. The results indicate that the proposed scheme is able to distinguish islanding situation with non-islanding event accurately.

3.2 Working principle of the proposed scheme

Fig. 3.1 shows a flow chart of the proposed islanding detection technique. Firstly, voltage samples of three phases for one cycle duration are acquired from the terminal of the target DG. The data acquisition of the above samples is carried out at a sampling frequency of 4 kHz with a fundamental frequency of 50 Hz. The sliding window concept is used by the proposed scheme in which the oldest sample is discarded when the new sample is available [143].

3.2.1 Superimposed components

The superimposed technique is being used for the development of the protection relays since last three decades. It measures incremental change in the value of the input signal. This incremental change is measured over number of samples, full cycle, or half cycle. The proposed scheme utilizes superimposed component of the acquired voltage signals (ΔV_a, ΔV_b and ΔV_c). These are calculated using equation (3.1) [172], [173].

$$\Delta V_{a/b/c}(t) = V_{a/b/c}(t) - V_{a/b/c}(t-T) \tag{3.1}$$

Where, $V_{a/b/c}(t)$ is the instantaneous value of the voltage signal of phase *a*, *b*, and *c*, respectively, *t* is the instant of sample, *T* is the number of samples in the window and $\Delta V_{a/b/c}(t)$ is the superimposed component of the voltage of phase *a*, *b*, and *c*, respectively.

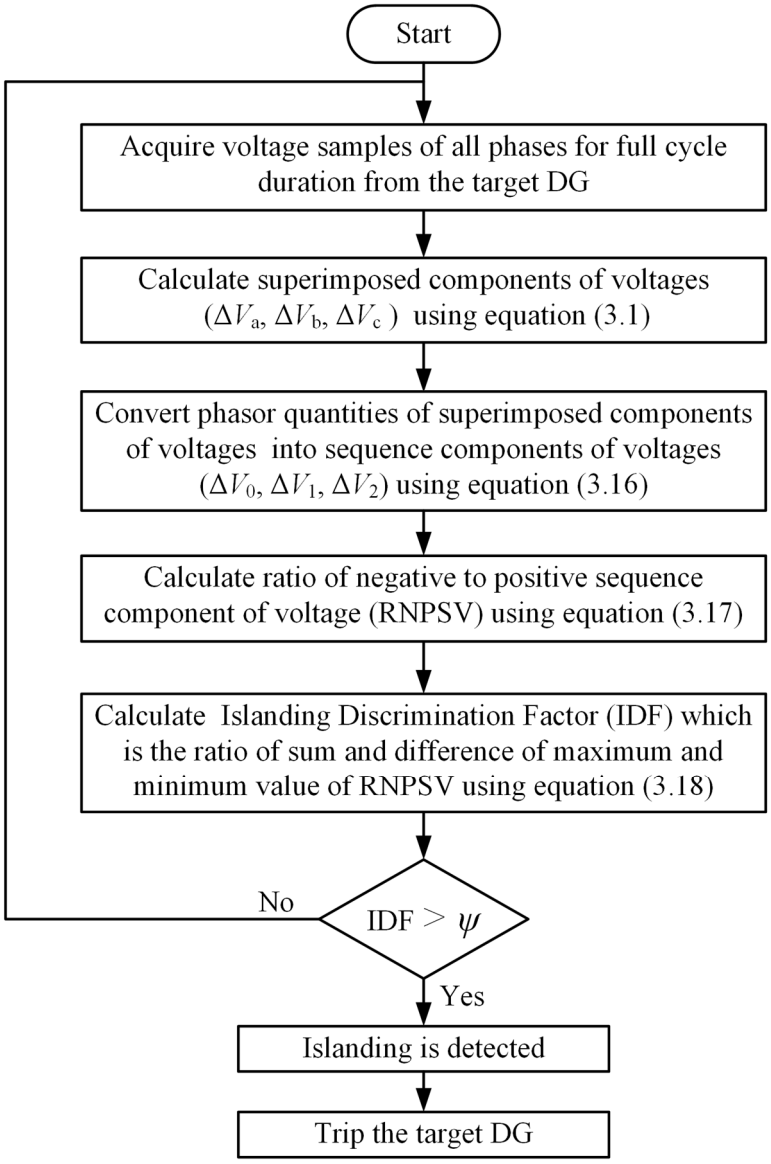


Fig. 3.1 Flowchart of the proposed sequence component of voltage based scheme.

3.2.2 Phasor estimation

The proposed technique relies on estimation of phasor values of superimposed components of voltages. In the proposed scheme, MDFT algorithm is used which is capable to eliminate both higher integer harmonics as well as the decaying DC component [170]. The step by step procedure of the estimation of the phasor value of the given input signal is described in the following.

During abnormal condition, an electrical signal contains fundamental component, few orders of harmonics and decaying dc component. The conventional Full-cycle Discrete Fourier Transform (FCDFT) cannot efficiently reduce the lower frequency components. Therefore, the estimated values of phasor (magnitude and angle) contain errors. To overcome this issue, the

MDFT method, as discussed in [170], is utilized for calculation of phasor values of the given input signal. In MDFT based algorithm, a signal containing few orders of harmonic and a component of decaying dc is given as an input to a first order LPF. This signal (*x(t)*) is expressed as equation (3.2).

$$x(t) = A_0 + \sum_{n=1}^{\infty} A_n \cos(n\omega t + \theta_n) + Be^{-t/\tau} \tag{3.2}$$

Where, *n* is the order of harmonic, *A* is the magnitude of the respective harmonic component, *B* and τ is the magnitude and time constant of a decaying dc component, respectively. When the signal, as represented by equation (3.2), passes through the LPF, its amplitude attenuates and shifts the phase angle according to the cut-off frequency of the filter. The first order LPF in Laplace domain is given as; $H(s) = \frac{1}{1+s\tau_1}$, $\tau_1 > 0$, where, τ_1 is the time constant of the LPF. Therefore, the output of the LPF contains amplitude & time constant of the decaying dc component and the lower order harmonics which is as given by equation (3.3).

$$z(t) = A_0 + \sum_{n=1}^{N-2} C_n \cos(n\omega t + \varphi_n) + De^{-t/\tau} + D_1 e^{-t/\tau_1} \tag{3.3}$$

Where, *D* and D_1 is the amplitude constant of decaying dc and LPF, respectively, and N is the maximum order of harmonic. This signal, as depicted in equation (3.3), is given as an input to MDFT algorithm for removal of higher order harmonics and decaying dc component. Hence, the output of MDFT is given by equation (3.4) and (3.5).

$$Z_{r(N)} = C_1 \cos\varphi_1 + \frac{2}{N}\sum_{k=1}^{N}\left[De^{-k\Delta T/\tau} + D_1 e^{-k\Delta T/\tau_1}\right].\cos\left(\frac{2k\pi}{N}\right) \tag{3.4}$$

$$Z_{r(N)} = C_1 \sin\varphi_1 - \frac{2}{N}\sum_{k=1}^{N}\left[De^{-k\Delta T/\tau} + D_1 e^{-k\Delta T/\tau_1}\right].\sin\left(\frac{2k\pi}{N}\right) \tag{3.5}$$

In order to determine the value of unknown constants *D*, D_1 and τ, following equations, as mentioned in [170], are utilized.

$$\frac{N(Z_{r(N+1)} - Z_{r(N)})}{2\cos(2\pi/N)} = DX(X^N - 1) + D_1K_1(K_1^N - 1) \tag{3.6}$$

Where, $X=e^{-\Delta T/\tau}$ *and* $K_1 = e^{-\Delta T/\tau_1}$

$$\frac{N(Z_{r(N+2)} - Z_{r(N+1)})}{2\cos(4\pi/N)} = DX^2(X^N - 1) + D_1K_1^2(K_1^N - 1) \tag{3.7}$$

$$\frac{N(Z_{r(N+3)} - Z_{r(N+3)})}{2\cos(6\pi/N)} = DX^3(X^N - 1) + D_1K_1^3(K_1^N - 1) \tag{3.8}$$

$$(3.7) - (3.6) \times K_1 = DX(X^N - 1)(X - K_1) \tag{3.9}$$

$$(3.8) - (3.7) \times K_1 = DX^2(X^N - 1)(X - K_1) \tag{3.10}$$

Now, $X = {(3.10)}/{(3.9)}$ (3.11)

The unknow decaying dc constant $D = \frac{(3.9) \times K_1}{X(X^N - 1)(X - K_1)}$ (3.12)

and the unknown decaying dc time constant $\tau = \frac{\Delta T}{\log(1/X)}$ (3.13)

The constant of LPF $D_1 = \frac{[(6) - DX(X^N - 1)]}{K_1(K_1X^N - 1)}$ (3.14)

Finally, the estimated amplitude and phasor angle of the fundamental frequency component is as given by equation (3.15).

Phasor amplitude of fundamental component $A_1 = C_1 / K_{V1}$ and
Phasor angle of fundamental component $\theta_1 = \varphi_1 + K\theta_1$ (3.15)

Where, K_{V1} and $K_{\theta 1}$ is the amplitude gain and correction angle in phase shift of fundamental component, respectively. Both these factors (K_{V1} and $K_{\theta 1}$) are used to correct the effect of LPF. By utilizing the above discussed MDFT algorithm, the estimated phasor values of the acquired voltage signals for one of the islanding cases is shown in the Fig. 3.2. Fig. 3.2. (a), (b), and (c) show the estimated phasor magnitude of the acquired voltage of phase 'a,' 'b,' and 'c,' respectively. Similarly, Fig. 3.2 (d), (e), and (f) show the estimated phasor angle of the acquired voltage of phase 'a,' 'b,' and 'c,' respectively.

Here, in the proposed scheme, the output of the LPF is given to MDFT algorithm for phasor computation. At the end of the MDFT algorithm, the estimated value of phasors of the fundamental frequency component of SCVs (ΔV_{a_est}, ΔV_{b_est}, and ΔV_{c_est}) are obtained. Now, these values are converted into sequence components of voltages using equation (3.16).

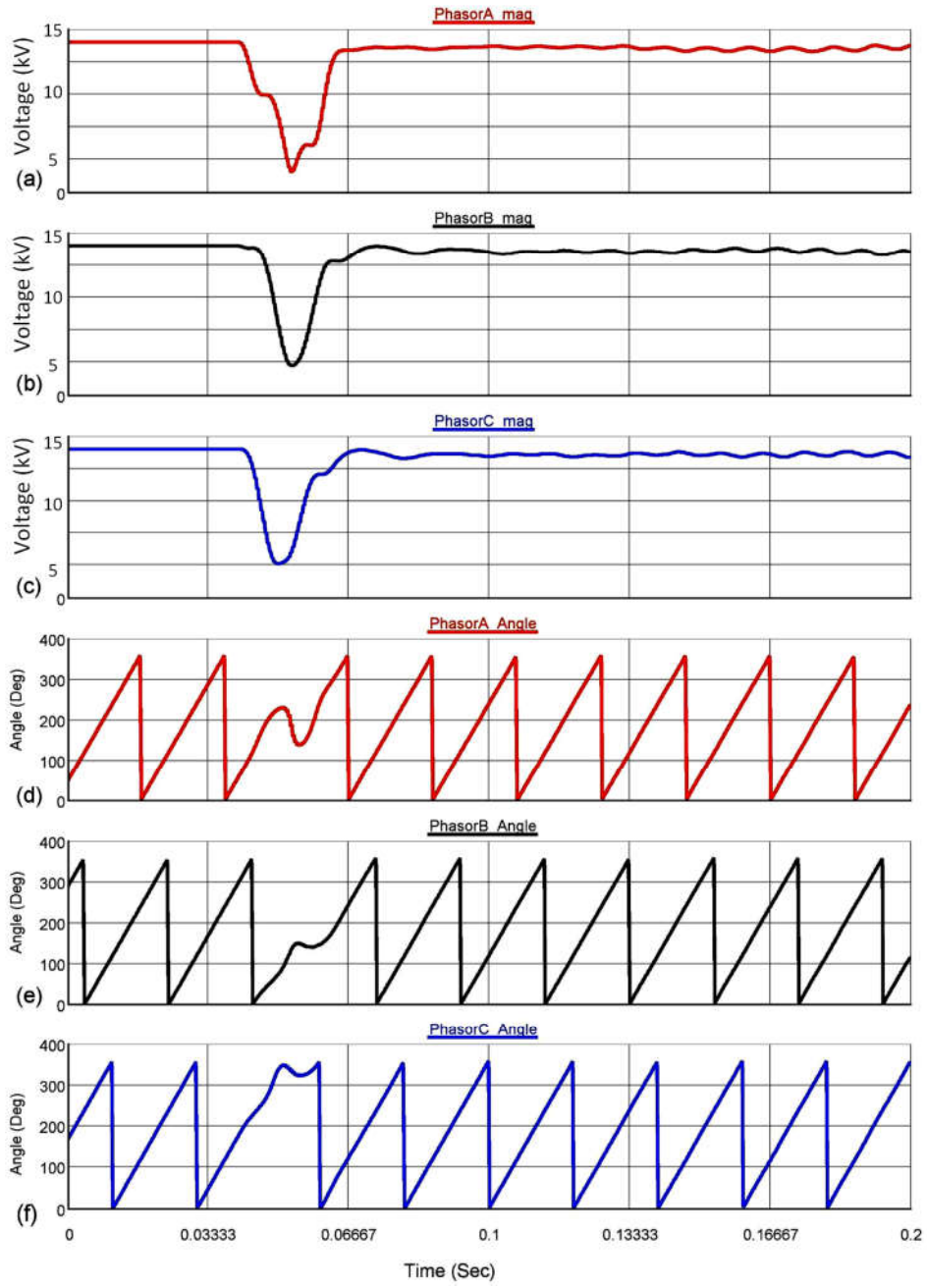


Fig. 3.2 MDFT algorithm based estimated phasor value of the acquired voltage signals (a) estimated voltage magnitude for phase 'a' (b) estimated voltage magnitude for phase 'b' (c) estimated voltage magnitude for phase 'c' (d) estimated voltage angle for phase 'a' (e) estimated voltage angle for phase 'b' (f) estimated voltage angle for phase 'c'.

$$\begin{bmatrix} \Delta V_0 \\ \Delta V_1 \\ \Delta V_2 \end{bmatrix} = \frac{1}{3} \times \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \times \begin{bmatrix} \Delta V_{a\_est} \\ \Delta V_{b\_est} \\ \Delta V_{c\_est} \end{bmatrix} \tag{3.16}$$

Where, ΔV_0, ΔV_1, and ΔV_2 are the zero, positive and negative sequence component of the SCV,

respectively, and the complex operator $\alpha = 1\angle 120^{\circ}$.

3.2.3 Derivation of Islanding Discrimination Factor

After obtaining values of sequence components of the acquired voltage signals, the Ratio of Negative to Positive Sequence Component of Voltage (*RNPSCV*) is determined using equation (3.17).

$$RNPSCV = \frac{|\Delta V_2|}{|\Delta V_1|} \tag{3.17}$$

Finally, an islanding discrimination factor is derived from the ratio of sum and difference of maximum and minimum value of *RNPSCV* as given in equation (3.18).

$$\text{IDF} = \frac{LRNPSCV + SRNPSCV}{LRNPSCV - SRNPSCV} \tag{3.18}$$

where, '*LRNPSCV*' and '*SRNPSCV*' represents the maximum and the minimum value of *RNPSCV*, respectively, during half a cycle.

The calculated value of IDF is then compared with the pre-set threshold (ψ). Here, IDF is used to discriminate islanding situation from non-islanding events. The description of selection of threshold is given in Section 3.3.2. If the value of IDF is more than the pre-set threshold, a signal is initiated to trip the target DG.

3.3 Modelling and Simulation

3.3.1 Cases generated

Validation of the proposed technique is done by modelling standard IEEE 34 bus network in RTDS/RSCAD environment. In the proposed scheme, various components such as distribution line, distributed load, spot load, distribution transformer and voltage regulator have been utilized with a fundamental frequency of 50 Hz. The aforementioned equipment is modelled by changing various parameters. The standard IEEE 34 bus network is highly unbalanced network which contains similar features those exist in the real physical distribution network. This include features such as (i) modelling of each section of the distribution system by actual phase impedance (ii) inclusion of single and two-phase laterals (iii) existence of load on each phase in each section (iv) closely spaced distributed load (v) presence of voltage regulators and capacitive reactive power compensation (vi) lightly loaded long distribution lines and (vii) inclusion of transformer for reducing voltage. Fig. 3.3 shows a single line diagram of IEEE 34 bus network modelled in RTDS/RSCAD environment. As shown in Fig.

3.3, the synchronous based DGs (DG1 to DG3) are connected at buses 854, 840, and 890 whereas inverter-based DG (DG4) is connected at bus 860. The parameters of these DGs are given in Appendix - A. Moreover, with reference to Fig. 3.3 four different islanding cases have been formulated.

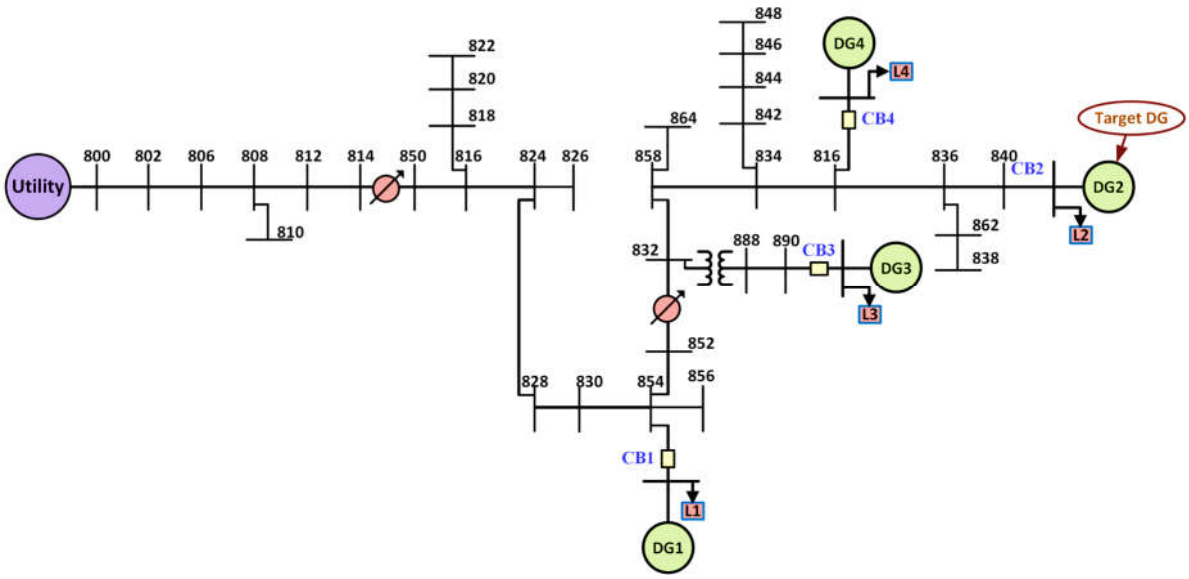


Fig. 3.3 Single line diagram of IEEE 34 bus network with DGs.

As shown in Table 3.1, these cases have been formed by considering different combinations of DGs.

Table 3.1 Various cases considered for island formation.

Case	Island Formation
I	Network contains DG2 only
II	Network contains DG2 and DG4
III	Network contains DG2, DG3 and DG4
IV	Network contains DG1, DG2, DG3 and DG4

Various kinds of islanding and non-islanding cases have been generated by following ways.

1. Simulating all ten types of faults on Feeder-1 and Feeder-2 located between bus 858 and 840 and bus 832 and 890, respectively, at four different fault locations (25%, 50%, 75% and 100% of line length) with four different values of fault resistance (R_f = 0.01, 1.0, 10 and 30 Ω).
2. Active power and reactive power are altered in the range of 25% to 150% in steps of 25% of rated capacity of DG2 (1.5 MVA).

3. Load power factor is changed between 0.7 (lagging) to unity in steps of 0.05.
4. Switching of capacitor bank is carried out in the range of 0.001μF to 100 μF in step of 10 μF.
5. Starting of various capacity of induction motor is performed (1 kW, 10 kW, 100 kW and 1000 kW).
6. Tripping of DGs (DG1, DG3 and DG4) other than target DG (DG2).
7. Variation in all the parameters (as considered in step 1 to step 6) for reconfigured network.
8. Islanding is performed during active power and reactive power mismatches in the range of 0% to 90% in steps of 5%, respectively.
9. Islanding is also carried out in reconfigured network with different active and reactive power mismatches (as considered in the previous steps)

3.3.2 Threshold selection

To achieve proper segregation among islanding condition and non-islanding events, choice of the threshold value is very essential. In this regard, large number of non-islanding and islanding cases, as shown in Table 3.2, have been generated in RTDS/RSCAD environment. The selection of threshold depends on the steady state value during normal condition as well as on various abnormal/non-islanding events. In the proposed scheme, the value of IDF is compared with the pre-set threshold for accurate discrimination between islanding situation and non-islanding conditions. The IEEE 34 bus system is highly unbalanced network due to presence of distributed load and spot load. Therefore, the sequence components of voltage are not negligible during normal condition. The magnitude of these components increases due to disturbances which are generated because of switching of various equipment. The switching/non-islanding events may be due to sudden change in load, energization/de-energization of capacitor bank, starting of induction motor and different types of faults on adjacent feeder. The maximum value of IDF obtained in case of switching of various equipment for IEEE 34 bus network and IEC61850 Micro-Grid Model is shown in Table 3.3.

Table 3.2 Non-islanding and islanding simulation cases generated.

Sr. No.	Event		Fault	Fault location	R_f (Ω)	% change in Load	pf	SOCB**	SIM**	Total Cases
1	Various faults on Feeder-1 (LG, LL, LLG, LLLG)*		3+3+3+1=10	4	4	1	1	-	-	10×4×4×1×1= 160
2	Various faults on Feeder-2 (LG, LL, LLG, LLLG)		3+3+3+1=10	4	4	1	1	-	-	10×4×4×1×1= 160
3	Sudden load change on target DG		-	-	-	6	7	-	-	6×7=42
4	Change in load power factor (pf) at target DG		-	-	-	6	6	-	-	6×6=36
5	Switching of capacitor bank (SOCB).		-	-	-	6	-	6	-	6×6=36
6	Starting of Induction Motor (SIM).		-	-	-	6	-	-	6	6×6=36
7	Tripping of DGs other than target DG (DG Trip)		-	-	-	36	-	-	-	36
8	Non-islanding events for reconfigured network	Faults	320	-	-	-	-	-	-	320+42+36+36+36+36 =506
		Load Change	-	-	-	42	-	-	-	
		pf change	-	-	-	-	36	-	-	
		SOCB	-	-	-	-	-	36	-	
		SIM	-	-	-	-	-	-	36	
		DG Trip	-	-	-	36	-	-	-	
Total non-islanding cases										1012
9	Islanding with varying active and reactive power mismatch.		Active power mismatch (18)			Reactive power mismatch (18)				18×18 =324
10	Islanding with varying active and reactive power mismatch during reconfigured network		Active power mismatch (18)			Reactive power mismatch (18)				18×18 =324
Total islanding cases										648
Total Non-islanding and Islanding cases										1012+648= 1660

* LG: Line to Ground, LL: Line to Line, LLG: Double Line to Lround and LLLG: Triple line to ground.
**SOCB: Switching of capacitor bank, SIM: Starting of Induction Motor.

Table 3.3 Maximum value of IDF for various non-islanding and islanding events.

Sr. No.	Event	Maximum value of IDF	
		IEEE 34 bus Network	IEC61850 Micro-Grid Model
Non-islanding Events			
1	Various faults on Feeder-1		
	• LG fault	7.5	7.8
	• LL fault	8.1	8.6
	• LLG fault	5.2	6.4
	• LLLG fault	1.0	2.3
2	Various faults on Feeder-2		
	• LG fault	6.4	6.9
	• LL fault	6.9	7.6
	• LLG fault	4.3	5.2
	• LLLG fault	1.0	2.4
3	Sudden change in load on target DG.	4.0	5.1
4	Sudden change of load power factor.	3.8	4.6
5	Switching of capacitor bank.	3.2	4.8
6	Starting of Induction motor.	1.6	2.4
7	Tripping of DGs other than the target DG.	3.4	4.8
8	Non-islanding events for reconfigured network.		
	Faults on main feeder.	5.2	6.4
	Sudden change in load.	3.2	4.6
Islanding Event			
9	Islanding at active and reactive power mismatch.	23.4	26

It is worth observing from Table 3.3 that the maximum value of IDF for two different networks during all non-islanding events remain well below 8.7. Subsequently, the behaviour of maximum value of IDF during islanding situation for varying positive and negative active/reactive power mismatches are shown in Fig. 3.4. Here, the positive power mismatch indicates that the load requirement is higher than the total capacity of the DGs whereas negative power denotes that the load demand is lower than the rated capacity of the DGs. Generally, most of the DGs are capable of bearing not more than 30% overload. Hence, the effect of positive active and reactive power mismatch on the proposed scheme has been studied only up to 40% overload compared to the effect of negative active and reactive power mismatch (0-90%). It is seen from Fig. 3.4 that the minimum and maximum value of IDF varies in the range of 14.5 to 30. Hence, considering some safety margin, the threshold value of 10.0 is selected for proper discrimination between islanding condition and non-islanding events.

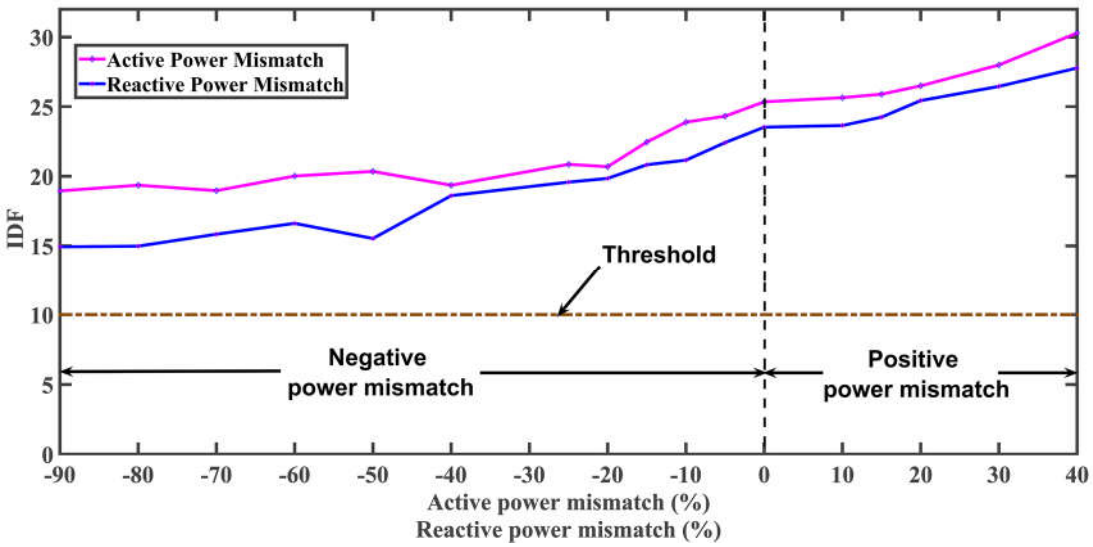


Fig. 3.4 The value of IDF during various percentage of active and reactive power mismatch.

3.3.3 Effect of network unbalance

The level of unbalance of the distribution network has a direct impact on the selection of the threshold value for the proposed scheme. During grid connected mode, the DG is subjected to the unbalance voltage of the grid network. Among various definitions of the unbalance voltage [97], [174], the ratio of negative to positive sequence voltage is extremely important. Various literature published by researchers and standards [175]–[179] have recommended that the unbalance voltage should not be more than 3% for any utility grid network. However, in actual field operation, the level of unbalance may exceed the above-mentioned value which in turn may affect the IDF of the proposed scheme. Nevertheless, in the presented islanding detection scheme, the selection of the threshold is carried out by performing various islanding situations and non-islanding events at different operating conditions on IEEE 34 bus network and IEC61850 Micro-Grid Model networks. The results obtained on these networks during various islanding and non-islanding conditions clearly indicate that the selected value of the threshold is justified for the cases generated in simulations on RTDS/RSCAD platform.

3.4 Performance evaluation of the presented technique

The performance of the presented technique has been evaluated against various non-islanding and islanding situations. The simulation results in terms of IDF are described in this section.

3.4.1 Response of the presented technique in case of islanding situation

The response of the presented technique has been verified during islanding situation for varying active and reactive power mismatches. Fig. 3.5 (a) shows the simulation results in terms of IDF during islanding condition for 5% and 20% active power mismatch.

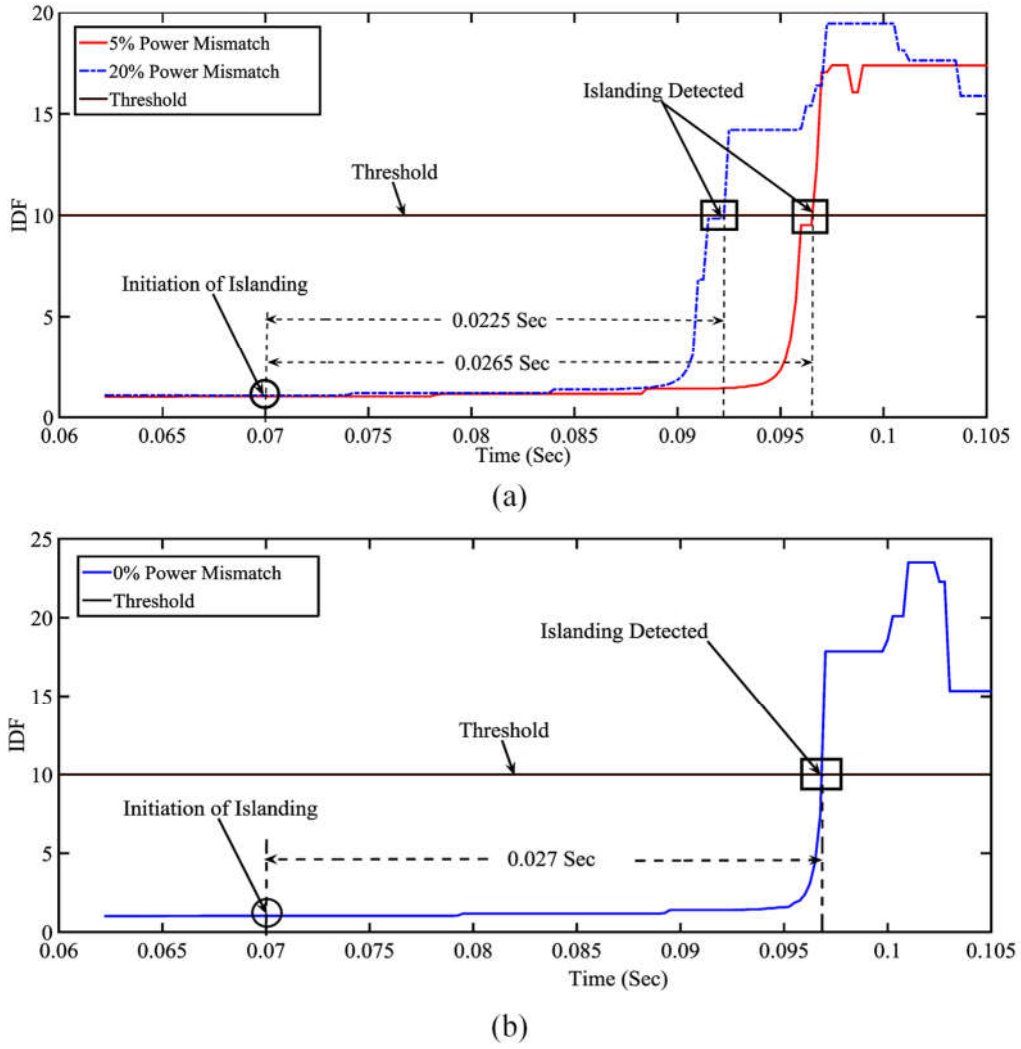


Fig. 3.5 Performance of the presented technique in terms of IDF during islanding with (a) 5% & 20% active power mismatch and (b) 0% active power mismatch.

It has been observed from Fig. 3.5 (a) that the value of IDF exceeds the threshold value and initiates tripping command to trip the target DG. It has been observed from literatures that most of the existing schemes are not capable to sense islanding situation during perfect power balance condition. This problem is rectified by the proposed scheme as it detects islanding situation during 0% active power mismatch rapidly. This is confirmed from Fig. 3.5 (b) which shows the simulation results in terms of IDF given by the presented technique during perfect power balance condition. Therefore, it is clear from Fig. 3.5 that though the islanding detection

time increases with the reduction in the percentage power mismatches, the presented technique is able to detect islanding condition within one and half cycle. In actual field, digital relay is used for anti-islanding protection. In this digital relay, both calculation of SCVs and phasor computation of SCVs are carried out simultaneously (using parallel processing concept). Therefore, the execution of the said algorithm takes not more than 123 samples (83 samples for phasor computation and 40 samples for calculation of IDF) for the detection of islanding situation.

3.4.2 Performance of the presented technique in case of various non-islanding conditions

In distribution network, most of the loads are inductive in nature. Induction motors (IMs) are used by most of the industries. The starting of induction motor generates high starting current (5 to 6 times the full load current). This phenomenon has to be properly distinguished with islanding situation by the islanding detection technique. Moreover, Automatic Power Factor Correction (APFC) panels are widely used by high tension customers in distribution system. It is necessary to maintain power factor close to the unity and also to avoid penalty to be imposed by the utility. This is achieved by APFC panel which contains capacitor banks in various stages. The switching of capacitor banks generates fluctuations in voltage signals. This has to be distinguished with islanding situation by the islanding detection technique. In addition, sudden increase/decrease in load at the target DG will lead to change in terminal voltage of the target DG. The response of the presented scheme has been verified on the aforementioned three phenomena and results are depicted in Fig. 3.6. It is clear from Fig. 3.6 (a) and Fig. 3.6 (b) that the value of IDF stays well below the threshold value for all the three cases. Hence, the presented technique offers improved stability during diversified non-islanding events and hence, avoids nuisance tripping.

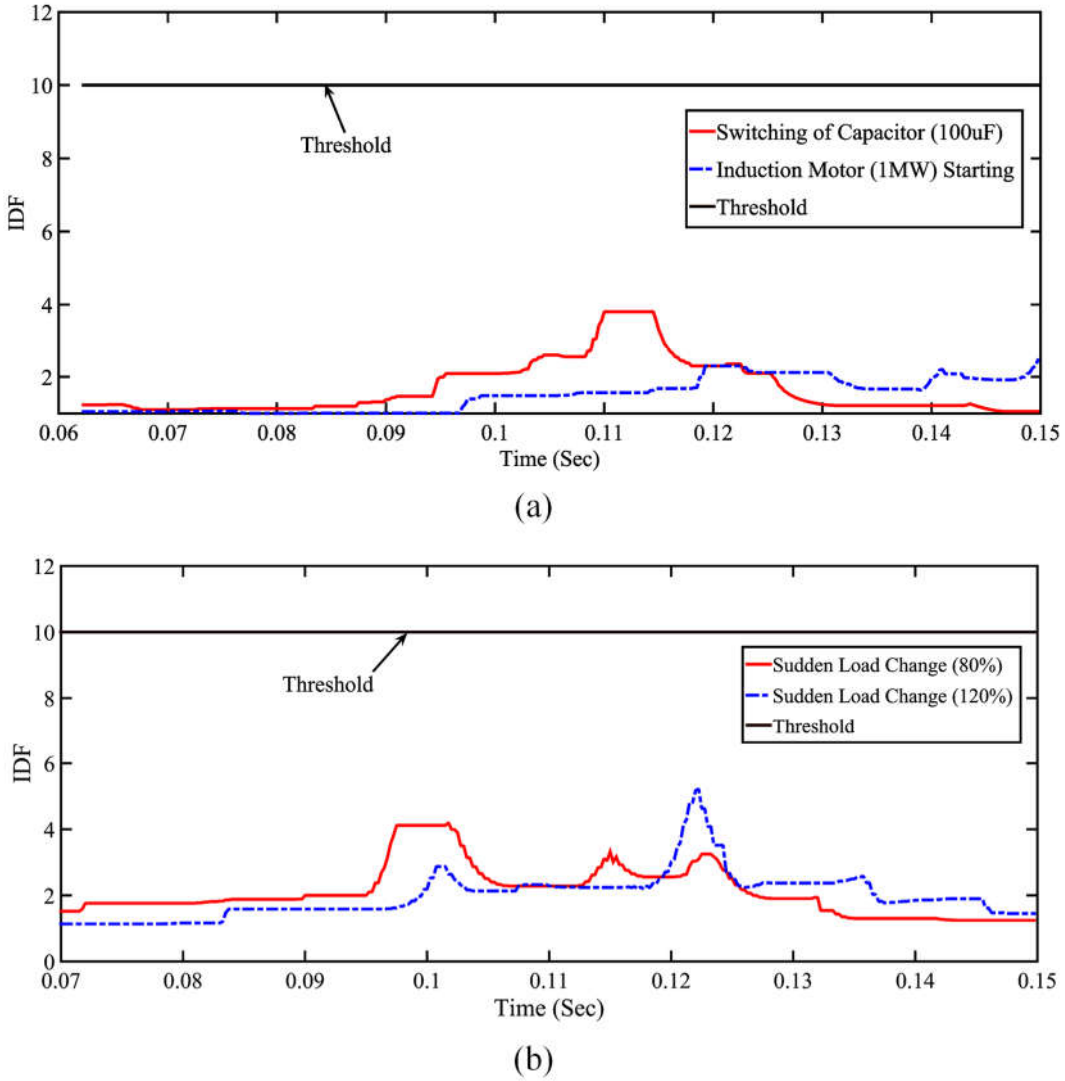


Fig. 3.6 Response of the presented technique in terms of IDF during (a) switching of capacitor & starting of induction motor and (b) sudden change in load.

3.4.3 Response of the presented technique during critical non-islanding events.

In order to evaluate the performance of the proposed scheme during critical non-islanding events, all ten types of faults (LG, LL, LLG and LLLG) have been simulated on Feeder-1 and Feeder-2 located between node 858 and 840 and node 832 and 890, respectively. For faults involving ground i.e. LG, LLG and LLLG, fault resistance in the range of 0.01 Ω to 30 Ω is also considered. Moreover, the said faults have been simulated at different locations with reference to the target DG. Fig. 3.7 (a) and Fig. 3.7 (b) shows the response of the presented technique during three different types of faults on Feeder-2 with low (0.01 Ω) and high (30 Ω) value of fault resistance. It is noted from Fig. 3.7 that the proposed scheme remains stable against all types of faults as the value of IDF stays well below the threshold value.

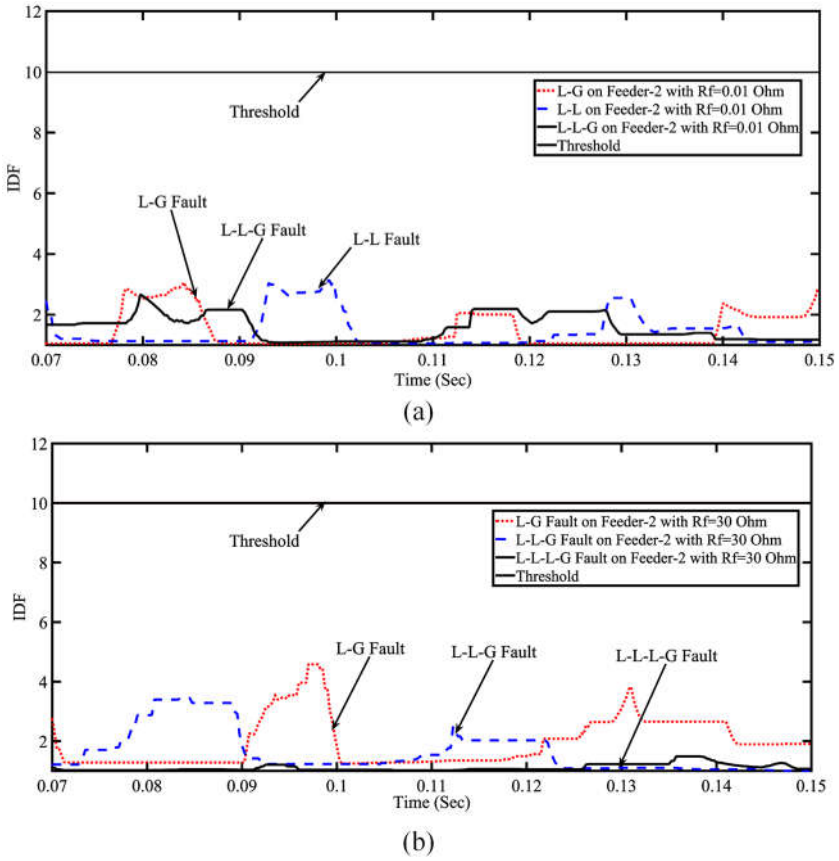


Fig. 3.7 Response of the presented technique in terms of IDF during various types fault on Feeder-2 with (a) R_f =0.01 Ω and (b) R_f =30 Ω.

3.4.4 Response of the presented technique on reconfigured network

Though the distribution networks are operated radially they are generally built as meshed networks. In order to provide uninterrupted electric supply to all the loads and also to reduce power loss, the configuration of distribution networks is changed with the help of manual/automatic switching operations. This is widely known as reconfiguration of the distribution network. This will also help to reduce over loading of the network equipment. The reconfiguration of the distribution network is carried out by opening sectionalizing (normally closed) and closing tie (normally open) switches of the network. The switching of both sectionalizing and tie switches are carried out in such a way that the radial structure of the distribution network is maintained and all of the loads are energized [180]. In order to maintain constant voltage profile at all buses, an alternate line between bus 816 and 852 is proposed in the IEEE 34 bus network. The reconfiguration of this network is achieved by opening sectionalizing switch connected between bus 854 and 852 and closing the tie switch placed in an alternate line connected between bus 816 and 852. The network after reconfiguration is shown in Fig. 3.8.

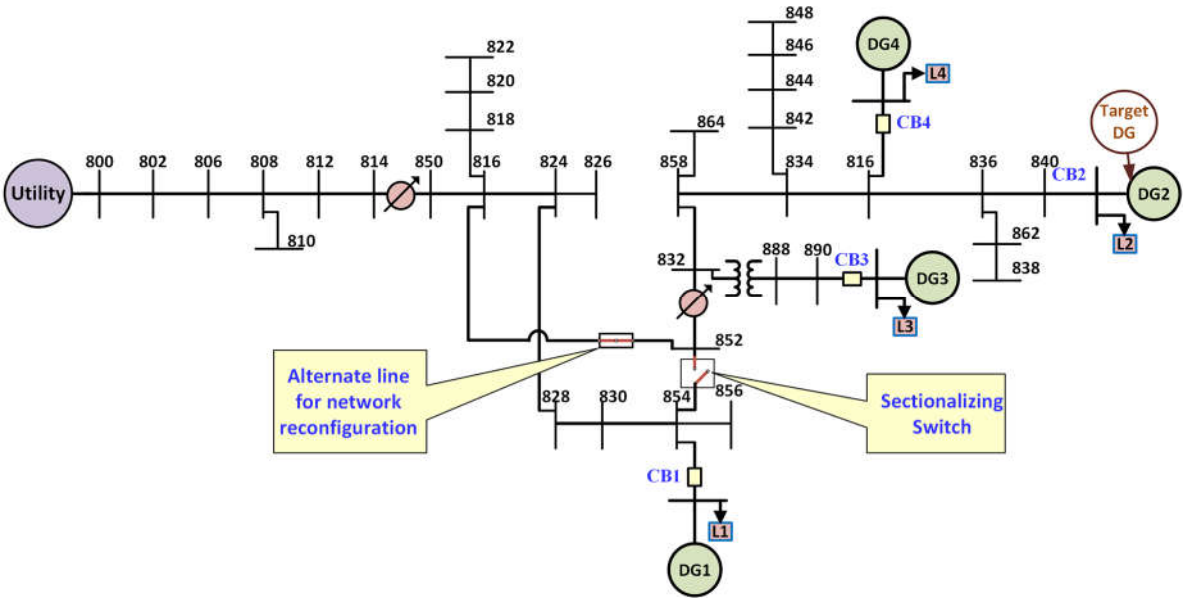


Fig. 3.8 Single line diagram of IEEE 34 bus network after reconfiguration.

As shown in Fig. 3.8 during normal operation, the tie switch remains open and sectionalizing switch remains closed whereas in case of reconfiguration of the network the tie switch closes and the sectionalizing switch becomes open. The effectiveness of the presented technique has been authenticated by generating diversified islanding/non-islanding cases on the reconfigured network. Fig. 3.9 shows the simulation results for reconfigured network during islanding situation and one of the critical non-islanding events (fault on Feeder-1). It is clear from Fig. 3.9 that the value of IDF stays well below the threshold value during non-islanding event whereas it exceeds in case of islanding situation.

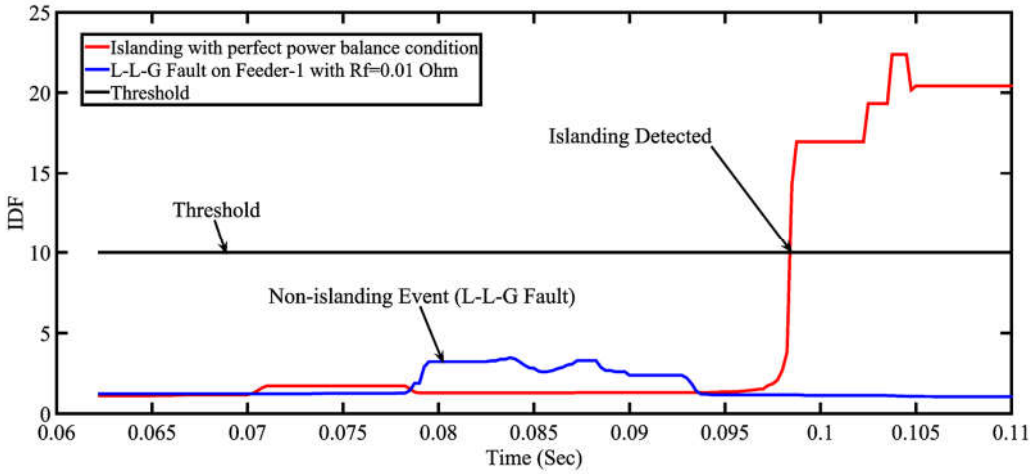


Fig. 3.9 Response of the presented technique during islanding and non-islanding event on reconfigured network.

3.4.5 Response of the presented technique on entirely different network

The response of the presented technique has been verified on IEC61850-7-420 Micro-Grid Model [181] which is entirely different network than the previous IEEE 34 bus network. The model, as shown in Fig. 3.10, is developed in RTDS/RSCAD environment. The DG3 of the said network is the target DG which disconnects when the islanding situation is detected. The simulation results in terms of IDF during islanding situation and one of the non-islanding event are shown in Fig. 3.11. It is clear from Fig. 3.11 that the value of IDF exceeds the threshold value during islanding situation whereas it remains well below the threshold in case of non-islanding condition. This clearly shows the versatility of the proposed islanding detection technique as the selected value of threshold more or less remains constant irrespective of the type of distribution network.

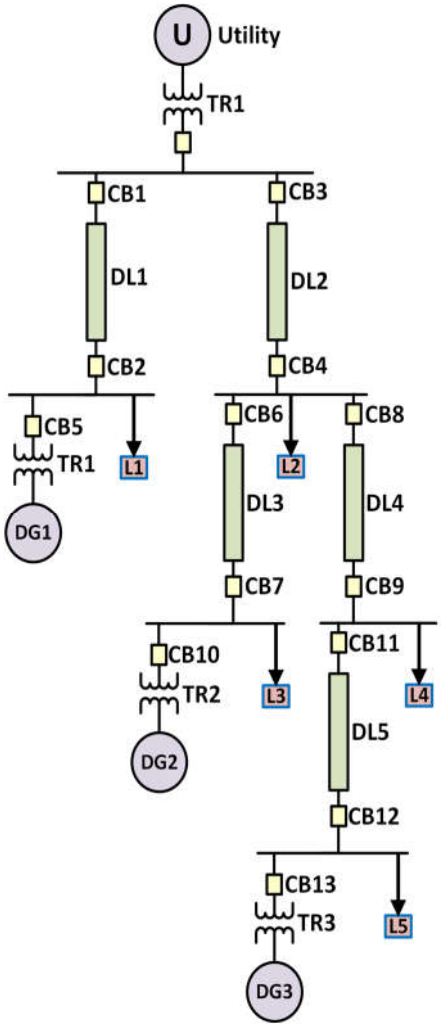


Fig. 3.10 Single line diagram of IEC61850-7-420 Micro-Grid model.

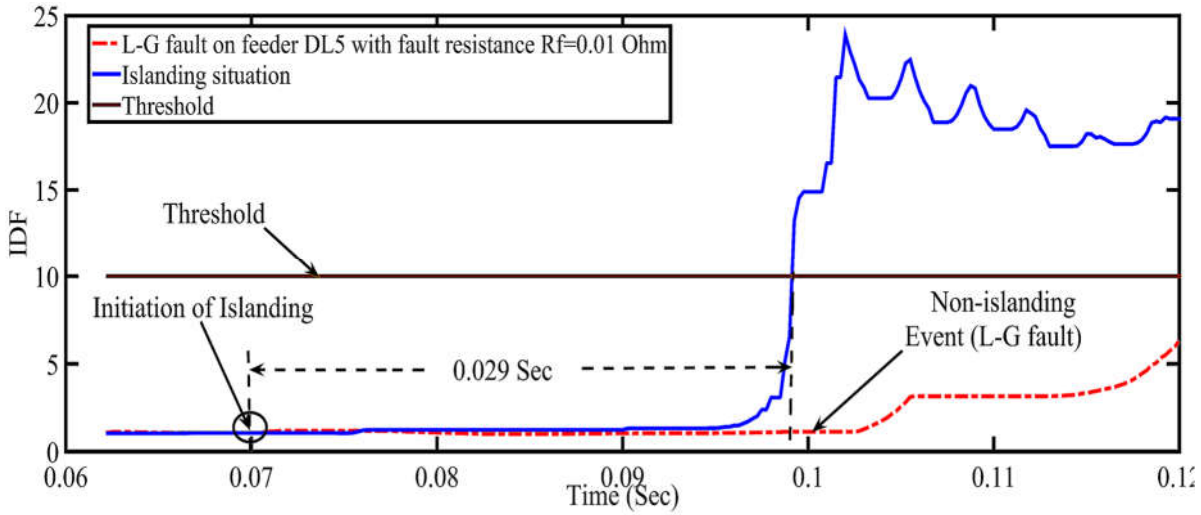


Fig. 3.11 Response of the presented technique during islanding and non-islanding event simulated on IEC61850-7-420 Micro-Grid model.

3.5 Comparison of the proposed scheme with the existing scheme

In this section, comparison of the presented technique is carried out with the recently published oscillatory frequency based method [182]. This method is based on deviation of the frequency during abnormal conditions. The discrimination between islanding situation and non-islanding event is achieved by comparing the oscillatory frequency with the set value of threshold (2.5 Hz as given in [182]). The value of oscillatory frequency remains greater than the set value of threshold for all non-islanding events whereas its value stays well below the threshold during islanding situation for some specific period of time. The comparative analysis of the proposed technique with the technique based on oscillatory frequency during islanding situation with perfect power balance condition is shown in Fig. 3.12.

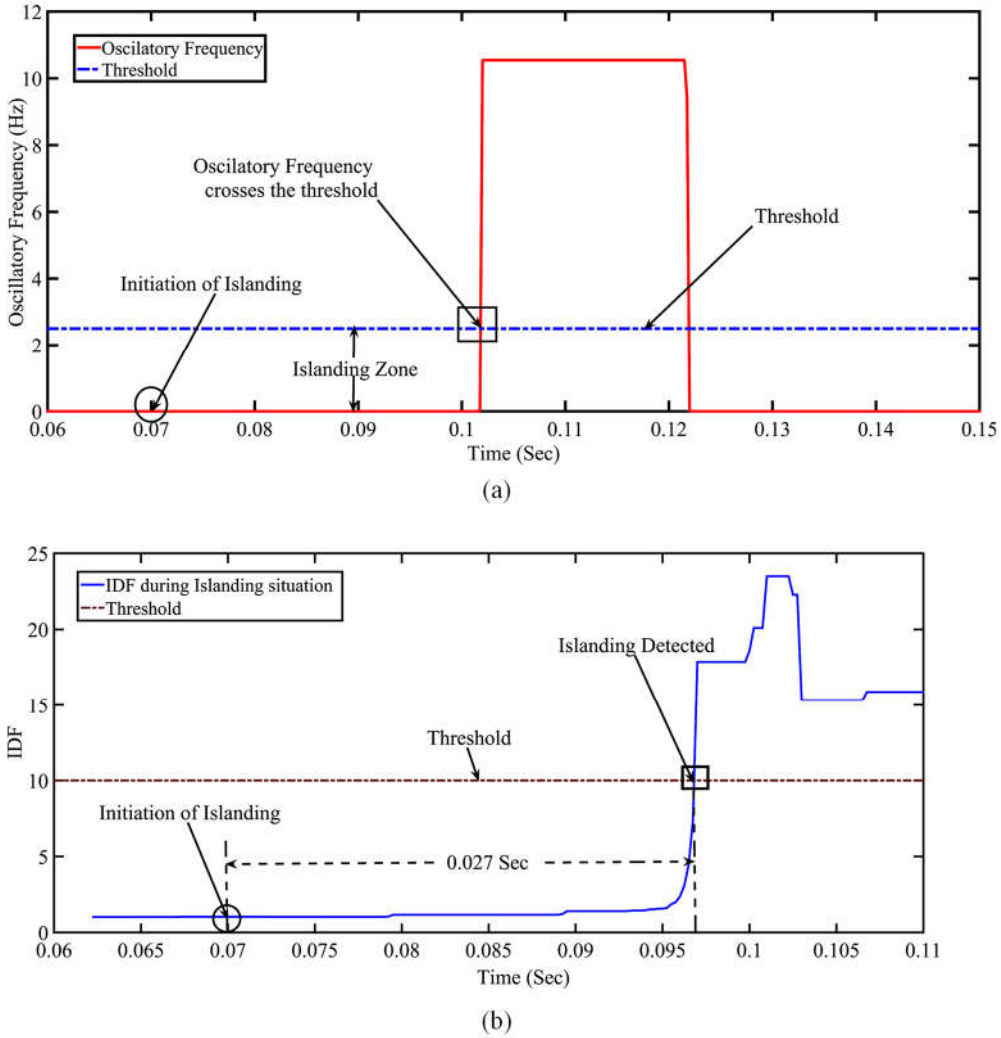


Fig. 3.12 Comparison between (a) the oscillatory frequency based technique and (b) the presented technique during islanding situation with perfect power balance condition.

It is clear from Fig. 3.12 (a) that the oscillatory frequency stays above the threshold value during islanding situation with perfect power balance condition. Hence, the above scheme does not initiate tripping signal. This type of incapability of the above scheme is termed as NDZ. Moreover, the selection of time delay for the set threshold value is the other short-coming of the above technique. In addition, its performance is highly affected by the selection of window size. Conversely, as observed from Fig. 3.12 (b), the presented IDF based technique is able to sense islanding situation in case of perfect power balance situation and hence, avoids NDZ. Furthermore, its performance does not depend on the selection of window size or time delay. Therefore, the presented technique is found to be superior than the existing scheme.

3.6 Summary

In this chapter, a new islanding detection technique based on discrimination factor is presented. This factor is derived from the SCVs which are calculated by utilizing the acquired voltage signals from the terminal of DGs. The validity of the presented technique has been evaluated by modelling two entirely different network namely IEEE 34 bus and IEC61850-7-420 in RTDS/RSCAD environment. Different islanding and non-islanding events have been generated from the said two networks by varying power mismatches, switching of various equipment and fault parameters. The results clearly show the capability of the presented technique in distinguishing islanding situation with various non-islanding conditions. Furthermore, the proposed scheme offers islanding detection time of the order of one and half cycle for all islanding cases even with perfect power balance situation. Moreover, the operation of the presented technique is restrained in case of diversified non-islanding events including reconfiguration of the network. At the end, comparison of the presented technique is also carried out with the scheme recently published in the literature and the results are found to be superior to the existing scheme.

Nevertheless, in order to further authenticate the presented technique on hardware results, a laboratory prototype has been developed. The description of the developed laboratory prototype is given in the next chapter (Chapter 4). In this prototype, a synchronous generator has been utilized as a DG. As the presented technique is a voltage based technique, the voltage signals have been acquired from the terminal of the DG. These signals are further utilized to derive IDF as per the algorithm of the proposed technique (chapter 3 algorithm). The hardware test results indicate that the proposed algorithm has accurately detected islanding situation at all mismatches of active and reactive power between load and generation. However, in case of a sudden load change (100% to 50%), the proposed technique mal-operates. Hence, it is necessary to develop accurate technique for islanding detection, which is able to detect islanding situations from the experimental test results as well as it remains stable during all non-islanding conditions.

Chapter 4

Experimental Performance of an Islanding Detection Scheme Based on Modal Components

4.1 Introduction

It is well known that the terminal voltage of distribution feeder, particularly at the tail end, is the function of line current and the voltage drop (which further depends upon line length). Generally, the length of radial distribution feeder is of the order of few kilometers (it is almost 10 to 15 km as per IEEE 34 bus network [183]). Due to the variations in the distributed load connected at various nodes of the feeder, the terminal voltage at the tail end varies accordingly. Thus, in order to keep the end terminal voltage constant, the usual practice is to connect voltage regulators at one or two nodes [183]. Henceforth, in this chapter, an implementation of a new islanding detection technique based on modal components of the voltage signals is presented. It is based on derivation of islanding detection factor which is derived from the modal transformation of the input voltage signals. Authenticity of the presented technique has been verified by developing a laboratory prototype of the distribution network along with DG. From the developed laboratory prototype, various islanding cases with varying positive/negative active and reactive power mismatches and different non-islanding events have been generated. In the proposed method, it has been shown that the DG is connected at the lateral end of distribution feeder which leads to the significant variation in the voltage. Moreover, the DG will also help in maintaining the end terminal voltage more or less constant.

4.2 Islanding detection algorithm

Fig. 4.1 shows the flow chart of the presented islanding detection method. Firstly, the samples of three-phase voltage signals are obtained from the terminal of the target DG with a sampling frequency of 4 kHz having a fundamental frequency of 50 Hz. The proposed technique is divided into three major parts (i) Phasor estimation (ii) Modal transformation and (iii) Derivation of IDF.

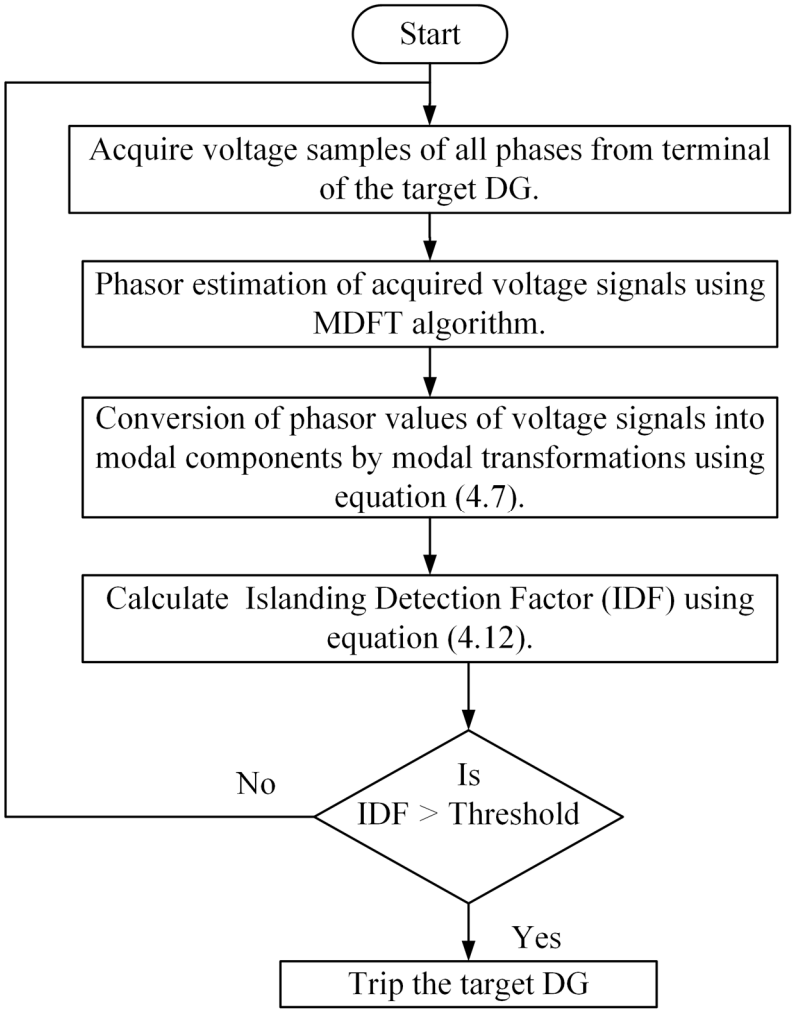


Fig. 4.1 Flowchart of the proposed modal component based islanding detection technique.

4.2.1 Phasor Estimation

In the proposed work, a full-cycle MDFT algorithm [170], as explained in Chapter 3 (Section-3.2.2), is utilized to obtain phasor values of the input voltage signal which is capable of eliminating together integer harmonics as well as the decaying DC component. The MDFT algorithm gives estimated value of amplitude and phase angle of the fundamental frequency component which are further utilized for the calculation of modal components.

4.2.2 Modal Transformation

A modal transform is a linear transformation of the voltage phasors into the modal components. It decouples the phasor quantity into its respective mode values [184]. In this transform, the three-phase system is considered as a three-single circuit which is totally independent of each other. Many researchers have used this concept for the protection of transmission line, fault detection and fault classification [185], [186]. Generally, the distribution lines are un-transposed in nature. The end terminal voltage/current of the three-

phase distribution feeder is the function of line current and voltage drop (this further depends on line length (l)). Hence, the equation of voltages/currents of the distribution feeder in terms of per unit length of series impedance (Z) and shunt admittance (Y) is given by equation (4.1).

$$\frac{d}{dl}V = Zi \quad \text{and} \quad \frac{d}{dl}i = YV \tag{4.1}$$

Differentiating the above equations lead to another equation as given below.

$$\frac{d^2}{dl^2}V = ZYV \quad where,\ Z = \begin{bmatrix} z_{aa} & z_{ab} & z_{ac} \\ z_{ba} & z_{bb} & z_{bc} \\ z_{ca} & z_{cb} & z_{cc} \end{bmatrix},\ Y = \begin{bmatrix} y_{aa} & y_{ab} & y_{ac} \\ y_{ba} & y_{bb} & y_{bc} \\ y_{ca} & y_{cb} & y_{cc} \end{bmatrix} \tag{4.2}$$

Here, the diagonal and off-diagonal elements of Z and Y represent self-impedance/admittance and mutual impedance/admittance of the distribution feeder, respectively. In order to obtain decoupled value of the phase voltages, equation (4.2) needs to be solved. This is achieved by using a standard set of rules which eventually diagonalizes the given matrix (the product of ZY) [187] as described in equation (4.3)-(4.5).

$$\lambda = Q^{-1}\ ZY\ \mathrm{Q} \tag{4.3}$$

Utilizing diagonalization procedure, the eigenvalues are obtained as per equation (4.4).

$$\left|\lambda[U] - ([Z][Y])\right| = 0 \tag{4.4}$$

Where, [λ] is a matrix which contains three eigenvalues and [U] is the unity matrix. For each eigenvalue, the 'eigenvector' [x], which is a column matrix, is calculated as per equation (4.5).

$$\left\{[U]\lambda_m - ([Z][Y])\right\}[x] = [0] \quad \text{Where, } m = 1, 2, 3 \tag{4.5}$$

Finally, by solving equation (4.5), the normalized eigenvector (Q) for each eigenvalue is given by equation (4.6).

$$Q = \frac{1}{3}\begin{bmatrix} 3/2 & 0 & -3/2 \\ 1/2 & -1 & 1/2 \\ 1 & 1 & 1 \end{bmatrix} \tag{4.6}$$

Therefore, the decoupled values of the phase voltages in terms of the modal transform modes

are given by equation (4.7) [188].

$$\begin{bmatrix} V_{m1} \\ V_{m2} \\ V_{m3} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 3/2 & 0 & -3/2 \\ 1/2 & -1 & 1/2 \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{4.7}$$

Where, $[V_{a/b/c}]$ represents a matrix of voltage phasors for *a*, *b,* and *c* phase, respectively, $[V_{m1/2/3}]$ represents a transformed model component matrix with mode *1*, *2*, and *3*, respectively. It is to be noted that the mode-1 and mode-2 are called "Arial" mode whereas the mode-3 is called "Earth" mode [188]. In the proposed technique, mode-1 (V_{m1}) and mode-2 (V_{m2}) components are utilized for calculation of islanding detection factor which is explained in the next sub-section.

4.2.3 Islanding Detection Factor

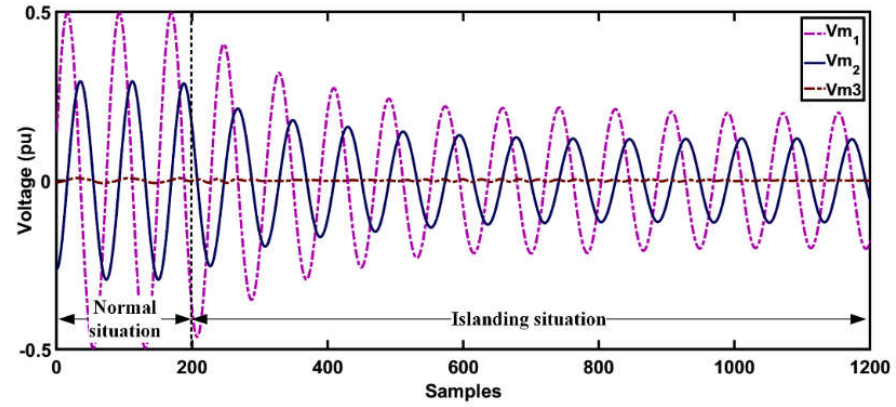
The obtained fundamental voltages, as given in equation (4.8), are used to calculate V_{m1}, V_{m2} and V_{m3} as per equation (4.7).

$$V_a = |V_a| \angle \theta_a,\ V_b = |V_b| \angle \theta_b \text{ and } V_c = |V_c| \angle \theta_c \tag{4.8}$$

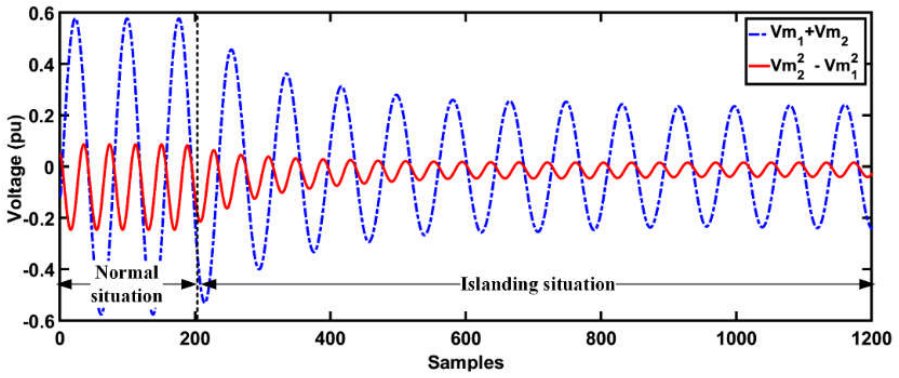
It has been observed from equation (4.7) that the V_{m3} is equivalent to the zero sequence component of voltage signals and its value is almost zero. This is also appreciated by observing Fig. 4.2 (a) which show the waveforms of the all three modes during normal/islanding situation. Hence, only two modes i.e. V_{m1} and V_{m2} are utilized for designing the mathematical equation for the proposed scheme. Fig. 4.2 (b) shows the relation between two modal components. By performing mathematical operations on modal components (V_{m1} and V_{m2}), as shown in equation (4.9) and (4.10), Detection Factor Coefficient (*DFC*) is derived as per equation (4.11).

$$V_{m1} + V_{m2} = 1/3\begin{bmatrix} \left(2|V_a|\left(\cos\theta_a + j\sin\theta_a\right)\right) - \left(|V_b|\left(\cos\theta_b + j\sin\theta_b\right)\right) \\ -\left(|V_c|\left(\cos\theta_c + j\sin\theta_c\right)\right) \end{bmatrix} \tag{4.9}$$

$$\begin{aligned} V_{m2}^2 - V_{m1}^2 &= \left(V_{m2} + V_{m1}\right) \times \left(V_{m2} - V_{m1}\right) \\ &= \left(1/3\begin{bmatrix} \left(2|V_a|\left(\cos\theta_a + j\sin\theta_a\right)\right) - \left(|V_b|\left(\cos\theta_b + j\sin\theta_b\right)\right) \\ -\left(|V_c|\left(\cos\theta_c + j\sin\theta_c\right)\right) \end{bmatrix}\right) \times \\ &\quad \left(1/3\begin{bmatrix} \left(-|V_a|\left(\cos\theta_a + j\sin\theta_a\right)\right) - \left(|V_b|\left(\cos\theta_b + j\sin\theta_b\right)\right) \\ +\left(2|V_c|\left(\cos\theta_c + j\sin\theta_c\right)\right) \end{bmatrix}\right) \end{aligned} \tag{4.10}$$



(a)



(b)

Fig. 4.2 Waveforms of (a) modal components (V_{m1} & V_{m2}) (b) modal components after

$$DFC = \left(\left| \frac{V_{m1} + V_{m2}}{\log\left(\sqrt{(V_{m2})^2 - (V_{m1})^2}\right)} \right| \right) \tag{4.11}$$

In order to distinguish islanding situation with non-islanding event, a clear pattern of sudden change in *DFC* during transient condition is required. Therefore, the minimum, average and maximum value of *DFC* over the period of half cycle has been examined. The waveforms of the minimum, average and maximum value of *DFC* during islanding (with 10% active power mismatch) and non-islanding (LG fault) situations (the details of various islanding and non-islanding conditions are given in section 4.3.3) are shown in Fig. 4.3 (a), (b) and (c), respectively.

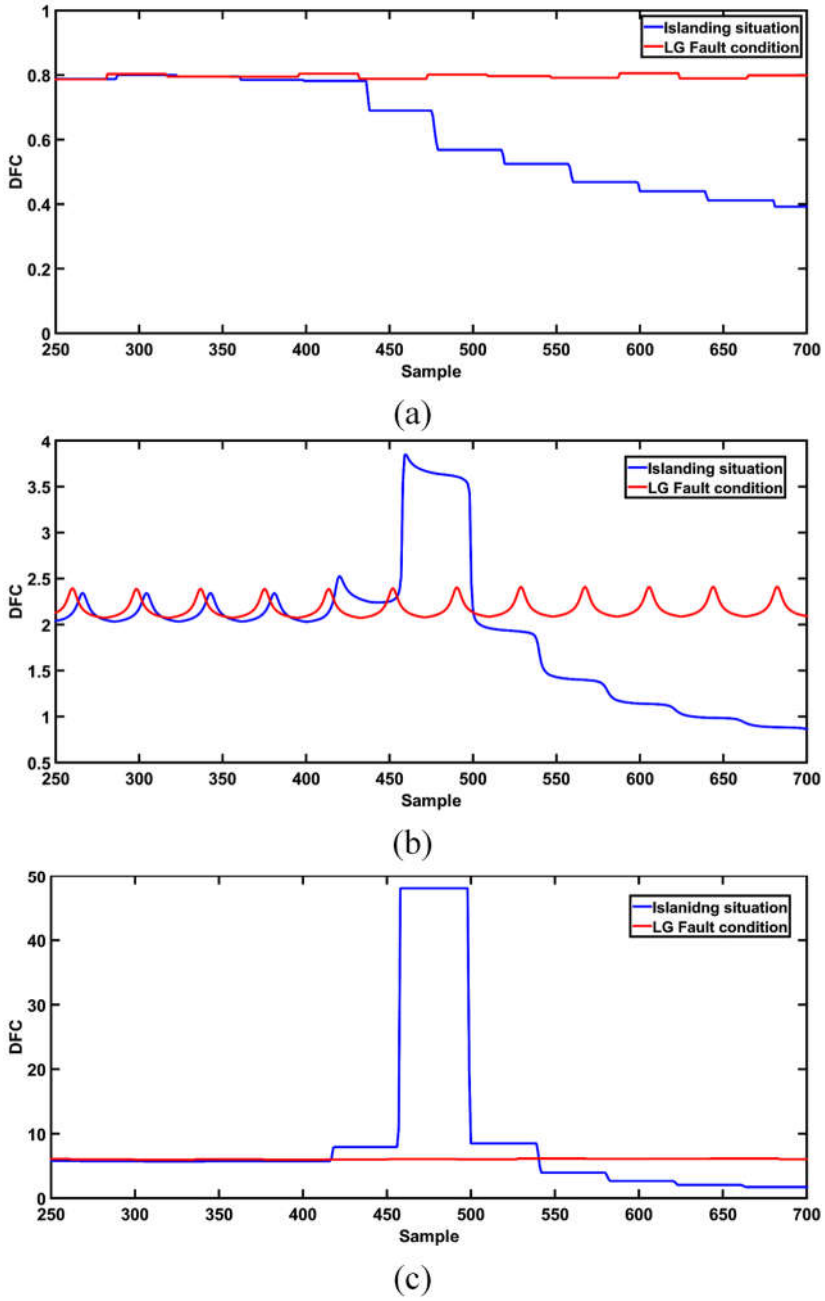


Fig. 4.3 (a) Minimum, (b) Average and (c) Maximum value of DFC during LG fault and islanding situation.

It has been observed from Fig. 4.3 (a) and (b) that the minimum and average value of *DFC* is not able to distinguish islanding situation with non-islanding event. Conversely, Fig. 4.3 (c) shows that the maximum value of *DFC* is capable to discriminate the two events clearly. Hence, the maximum value of equation (4.11) during a half cycle data window has been utilized. Afterwards, an IDF is calculated by taking superimposed components of *DFC* at every half cycle as per equation (4.12).

$$IDF_k = DFC_k - DFC_{k-w} \tag{4.12}$$

Where, *k* is the sample number and w is the window size. In order to maintain number of samples constant, the sliding window concept is used in the above-mentioned equations.

Finally, the calculated value of IDF is compared with the pre-set threshold for the detection of islanding situation. If the value of IDF is greater than the pre-set threshold, an islanding situation is detected. The selection of threshold is explained in the next section.

4.3 Experimental validation of the presented islanding detection scheme

In order to validate the authenticity of the presented algorithm, a hardware setup is developed in the laboratory environment.

4.3.1 Power circuit

The power circuit of the laboratory prototype is shown in Fig. 4.4.

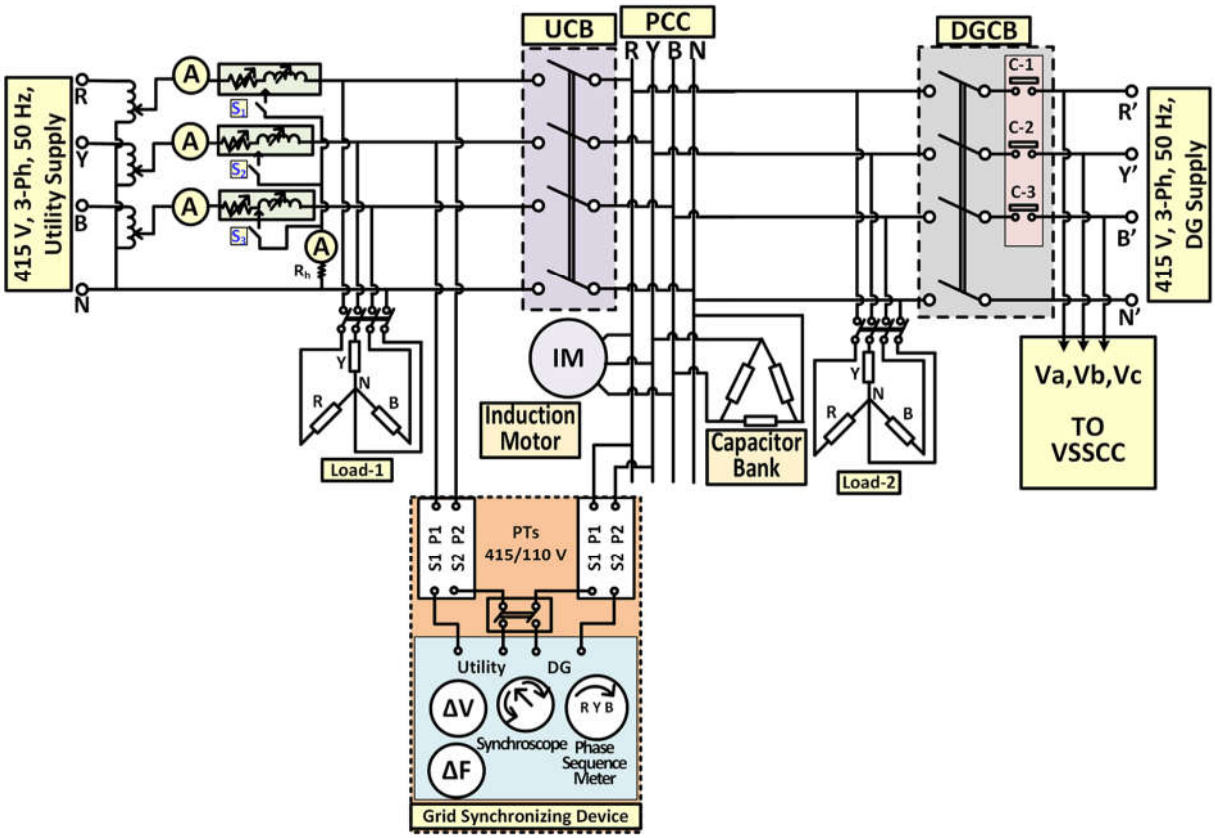


Fig. 4.4 Power circuit of the developed laboratory prototype.

As shown in Fig. 4.4, the distribution feeder is energized from the utility supply (415 V, 3-phase, 50 Hz from a three-phase auto-transformer). The length of distribution feeder is considered as 5 km and its parameters (adjusted using variable rheostats and inductors) are taken from the IEEE 34 bus network. In order to deliver power to the local load, a synchronous

based DG (3 kVA, 415 V, 50 Hz, 0.8 power factor, star grounded) is connected to the above distribution feeder at the PCC. Here, two star connected three-phase series R-L loads (Load-1 and Load-2) are utilized. The combination of Miniature Circuit Breaker (MCB) and contactor are used as Utility Circuit Breaker (UCB) and DG Circuit Breaker (DGCB), respectively. The synchronization of DG with the utility is performed with the help of Grid Synchronizing Device (GSD). The GSD contains two Potential Transformers (PTs) (PT1 and PT2), synchroscope and phase sequence meter. With respect to Fig. 4.4, islanding situation is performed by opening UCB. In order to simulate various non-islanding events, a three-phase delta connected capacitor bank and three phase induction motor are connected at the PCC. Moreover, various types of faults are also created using three switches S1, S2 and S3. The magnitude of fault current is limited with the help of variable rheostat (R_h).

4.3.2 Data acquisition and processing unit

Fig. 4.5 shows the data acquisition and processing unit utilized for the implementation of the presented scheme.

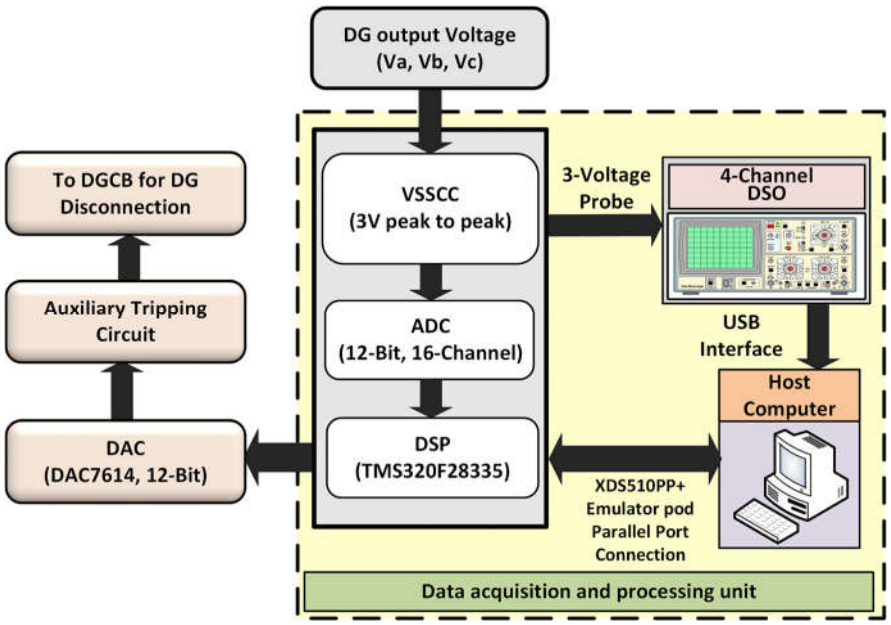


Fig. 4.5 Data acquisition and processing unit of the proposed scheme.

As shown in Fig. 4.5, the voltage signals, from the terminal of the target DG, are acquired by the 12-bit Analog-to-Digital Converter (ADC) of the DSP processor (C2000 Delfino series TMS320F28335) through the Voltage Sensor Signal Conditioning Circuit (VSSCC). The maximum sampling frequency of ADC is 12.5 mega samples per second with the conversion rate of 80 ns [189]. However, in the proposed scheme, the voltage signals are acquired with a

sampling frequency of 4 kHz for a fundamental frequency of 50 Hz. The VSSCC unit scales down the high voltage signal to low voltage signal. This unit is designed in such a way that it gives the maximum 3 V (peak-to-peak) for the maximum input of 500 V. Additionally, the unit has also provided various test points for capturing the waveforms of voltage signals during various islanding/non-islanding events through Digital Storage Oscilloscope (DSO). The DSP processor is interfaced with a host computer through a bidirectional XDS510PP+ emulator pod. This interfaces the DSP with MATLAB for execution of the code. The proposed islanding detection algorithm has been written in "MATLAB 2015b" and compiled and executed with Code Composer Studio (CCS) v5.1 [190]. A trip signal, generated by the proposed algorithm during an islanding situation, is given to DAC7614U which is a Digital-to-Analog Converter (DAC). The output of DAC is in the range of ±2.50 V with a current capacity in the range of ±1.25 mA. As the output of DAC is low, an amplifying circuit is used. Hence, auxiliary tripping circuit is used which initiates tripping command to disconnect the target DG. The pictorial view of the developed laboratory prototype is shown in Fig. 4.6.

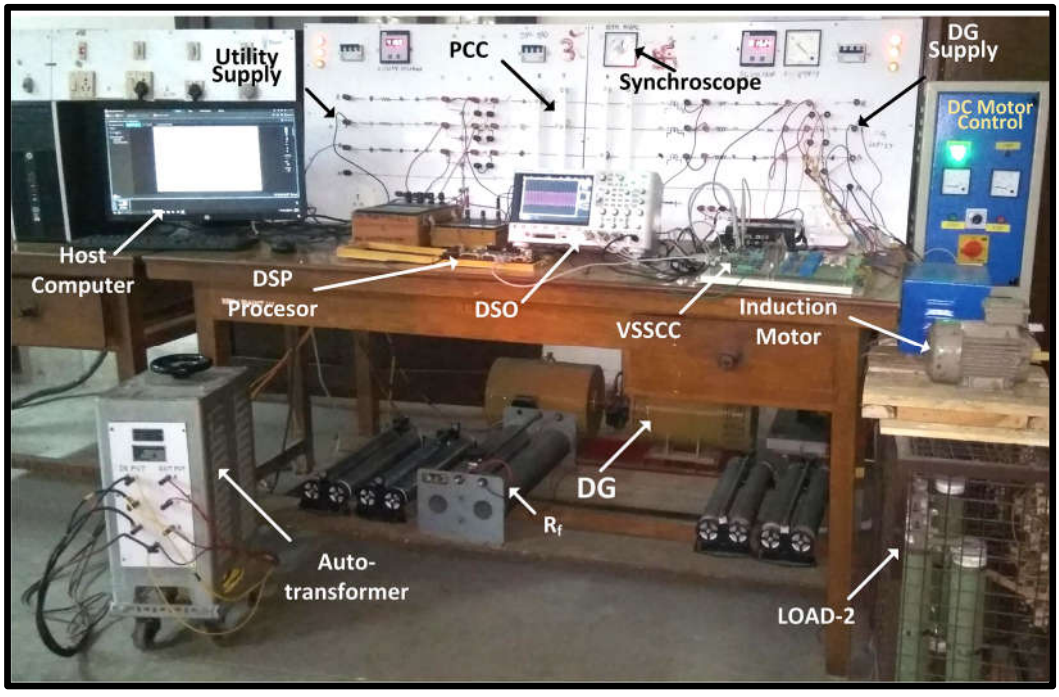


Fig. 4.6 Pictorial view of the developed laboratory prototype.

4.3.3 Cases generated and Threshold selection

In order to evaluate the performance of the proposed technique with unbalance nature of practical distribution network, various islanding and non-islanding cases, as shown in Table 4.1, have been generated from the laboratory prototype. It is to be noted from Table 4.1 that

38-islanding and 685-non-islanding cases have been generated which are used for evaluating the performance of the proposed technique. The selection of threshold depends on the steady state value of IDF during normal situation as well as in case of non-islanding conditions. In this proposed work, selection of threshold has been done by observing the value of IDF from the mathematical equations. At the same time, the calculated value of threshold from the arithmetical equations has also been verified by observing the value of IDF from various test cases generated using the laboratory prototype.

Table 4.1 Various islanding/non-islanding cases generated from the laboratory prototype.

Event	Parameter	Variation in parameter	Cases generated
Islanding	Active power mismatch	Perfect power balance (0%)	1
		0% to -50% in steps of 5%.	10
		0% to +40% in steps of 5%.	8
	Reactive power mismatch	Perfect power balance (0%).	1
		0% to -50% % in steps of 5%.	10
		0% to +40% in steps of 5%.	8
Total islanding cases Generated			38
Non-islanding	Fault on distribution feeder	Types of faults: LG, LLG and LLLG. Total =7	7×7×5 =245
		Fault resistance (R_f) = 3, 5, 10, 15, 20, 25 and 30 Ω. Total =7	
		Fault location (F_L) = 20%, 40%, 60%, 80% and 90% of the line length. Total =5	
	Sudden change in load	Variation in load from 50% to 150% in steps of 5%.	20
	Change in load power factor	(i) Variation in load power factor (lagging) from 0.6 to 1.0 in steps of 0.5. Total = 4 (ii) Variation in load from 50% to 150% in steps of 5%. Total = 20	4×20 =80
	Switching of capacitor bank.	(i) Change in rating of capacitor from 1 kVAr to 4.0 kVAr in steps of 0.25 kVAr. Total =16 (ii) Variation in load from 50% to 150% in steps of 5%. Total=20	16×20 =320
	Starting of three-phase induction motor	i) Motor rating: 1 H. P., 415 V, 50 Hz, Delta connected. Total =1 (ii) Variation in load from 50% to 150% in steps of 5%. Total=20	1×20=20
Total non-islanding cases generated			685
Overall cases generated			38+685=723

4.3.3.1 Threshold selection based on mathematical equation

It is to be noted from equation (4.12) that the value of IDF depends on the amplitude and the angle ($|V_a|, |V_b|$ & $|V_c|$ and θ_a, θ_b & θ_c) of the terminal voltage of the DG during normal/transient condition. Moreover, the value of IDF remains almost zero during normal condition whereas its value changes during non-islanding/islanding events. Various islanding

and non-islanding cases, as shown in Table 4.1, have been evaluated to identify variations in $|V_a|, |V_b|$ & $|V_c|$ and θ_a, θ_b & θ_c. Here, the amplitude and phase angle of the voltage have been changed in the range of ± 15% and ± 20% with respect to base value (rated voltage of the DG) in case of non-islanding and islanding situation, respectively. Utilizing the said voltage variations (both in magnitude and angle) in equation (4.11) and (4.12), the calculated values of IDF during various non-islanding and islanding situations are shown in Table 4.2. It is to be noted from Table 4.2 that the maximum value of IDF remains well below 2.0 during non-islanding situations whereas it stays well above 15.0 during islanding situations.

Table 4.2 Maximum value of IDF obtained based on mathematical equations during non-islanding and islanding situations.

Sr. No.	Event	Voltage amplitude variation (pu)	Voltage angle variation (Deg)	Maximum value of IDF
Non-islanding events				
1.	Fault on feeder	0.0 to 0.85	-15º to +15º	1.87
2.	Sudden load change	0.9 to 1.10	-15º to +15º	0.78
3.	Starting of induction motor	0.0 to 0.90	-15º to +15º	1.06
4.	Switching of capacitor	0.9 to 1.10	-15º to +15º	0.97
Islanding events				
5.	Islanding with 0% active power mismatch	0.80 to 1.20	-20º to +20º	24.23
6.	Islanding with -50% active power mismatch	0.00 to 1.20	-20º to +20º	18.68
7.	Islanding with 0% reactive power mismatch	0.80 to 1.20	-20º to +20º	23.43
8.	Islanding with -50% reactive power mismatch	0.00 to 1.20	-20º to +20º	17.86

4.3.3.2 Threshold verification using various test cases generated from laboratory prototype

The verification of the selected threshold value has also been carried out by performing different test cases, as mentioned in Table 4.1, on the laboratory prototype. The obtained maximum value of IDF during various cases is shown in Table 4.3. It is to be noted from Table 4.3 that the value of IDF is very small during normal operating condition. However, its value varies in a band of 0 to 2.0 during non-islanding conditions. At the same, it has been observed from Table 4.3 that the maximum value of IDF during islanding situation is of the order of 30. The behaviour of the maximum value of IDF during islanding situation for varying active/reactive power mismatches is shown in Fig. 4.7.

Table 4.3 Maximum value of IDF obtained based on laboratory prototype for various non-islanding/ islanding cases.

Sr. No.	Event	Maximum value of IDF
Non-islanding Events		
1.	LG fault on distribution line.	1.30
2.	Switching of capacitor bank.	0.20
3.	Starting of induction motor.	0.50
4.	Abrupt change in load.	0.25
5.	Change in load power factor.	0.25
Islanding event		
6.	With different active and reactive power mismatch.	30.00

It has been observed from Fig. 4.7 that the value of IDF is continuously changing and depends on change in active and reactive power mismatch. However, the minimum and the maximum value of IDF varies in the range of 11 to 30. Subsequently, it is observed from Table 4.2 and Table 4.3 that the maximum value of IDF for the non-islanding event is less than 2.0. Hence, considering double value of safety margin (4.0) with respect to the maximum value of IDF during non-islanding condition (2.0), the threshold value of 4.0 has been selected.

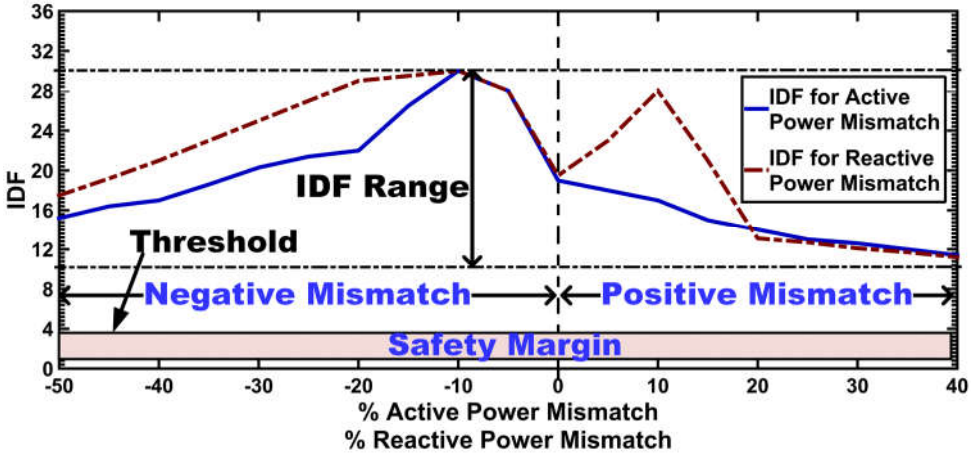


Fig. 4.7 Behaviour of IDF during islanding situation with varying active and reactive power mismatch.

4.4 Experimental results

The authenticity of the presented scheme has been verified on different islanding/non-islanding cases and the results are discussed in the following sub-sections.

4.4.1 Islanding situations

Fig. 4.8 (a) and Fig. 4.9 (a) shows the waveform of voltage signals captured by the DSO during islanding situation with +10% active power mismatch and -20% of reactive power mismatch, respectively. Subsequently, the response of the presented scheme in terms of IDF

for the above-mentioned islanding situations is also shown in Fig. 4.8 (b) and Fig. 4.9 (b), respectively. It is observed from both the figures that the terminal voltage of target DG reduces and subsequently, the value of IDF exceeds the threshold value within three cycles. It has been observed from available literature that most of the passive islanding detection algorithms contain some percentage of NDZ during perfect power balance situation [90], [96], [132], [182], [191]. In order to analyse the response of the presented algorithm, islanding has been carried out on the developed laboratory prototype with perfect power balance situation. The voltage signals captured by the DSO during islanding situation with 0% of active power mismatch is shown in Fig. 4.10 (a). The response of the presented scheme in terms of IDF on the above-mentioned islanding situation is shown in Fig. 4.10 (b). It is to be noted from Fig. 4.10 (b) that the presented scheme detects the islanding situation correctly as the value of IDF exceeds the threshold value.

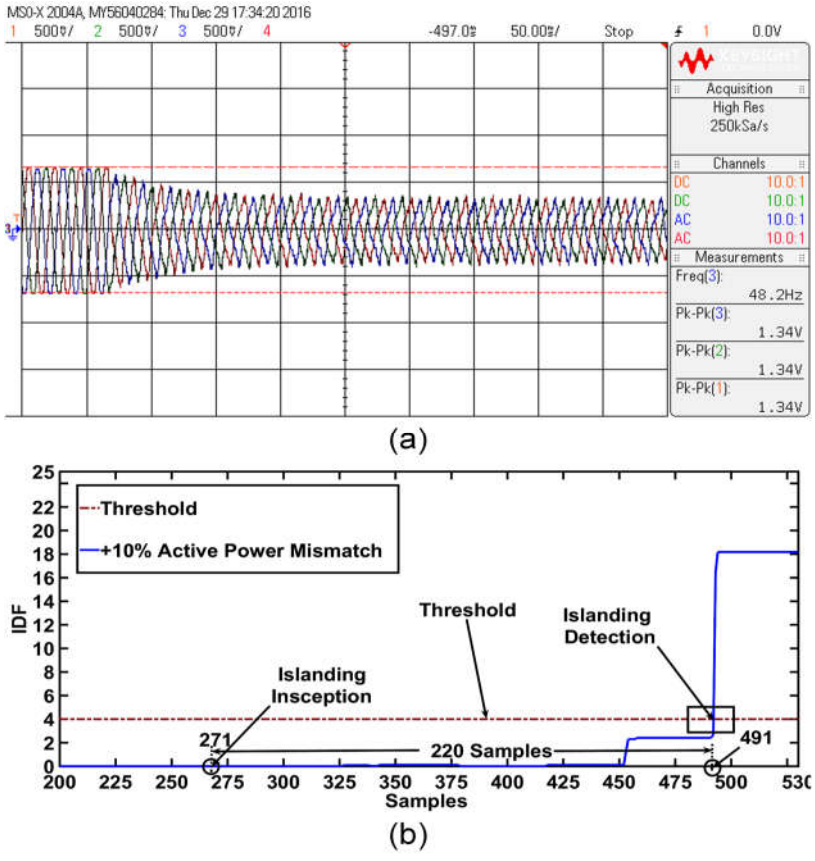


Fig. 4.8 Islanding with 10% active power mismatch (a) voltage signals captured by DSO (b) response of the presented algorithm in terms of IDF.

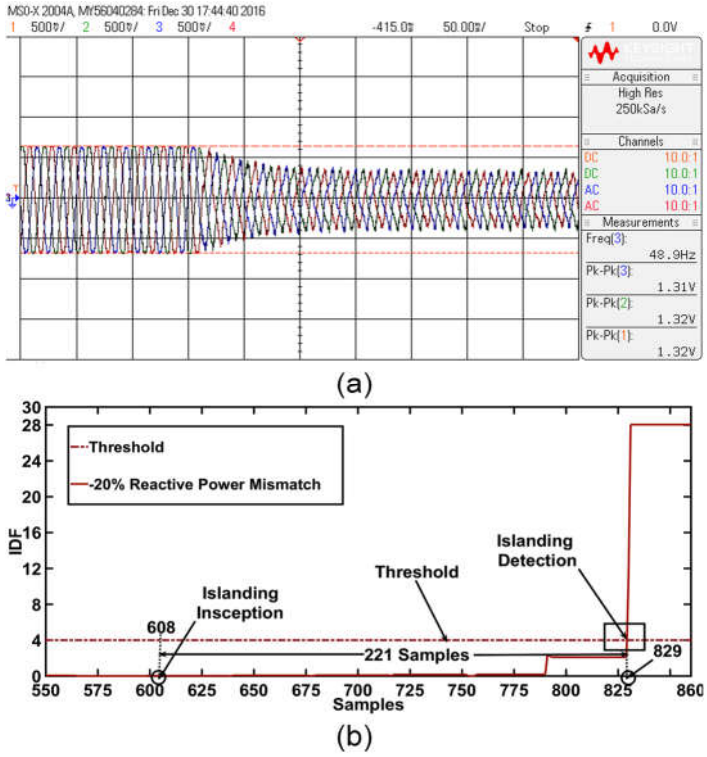


Fig. 4.9 Islanding with -20% reactive power mismatch (a) voltage signals captured by DSO (b) response of the presented algorithm in terms of IDF.

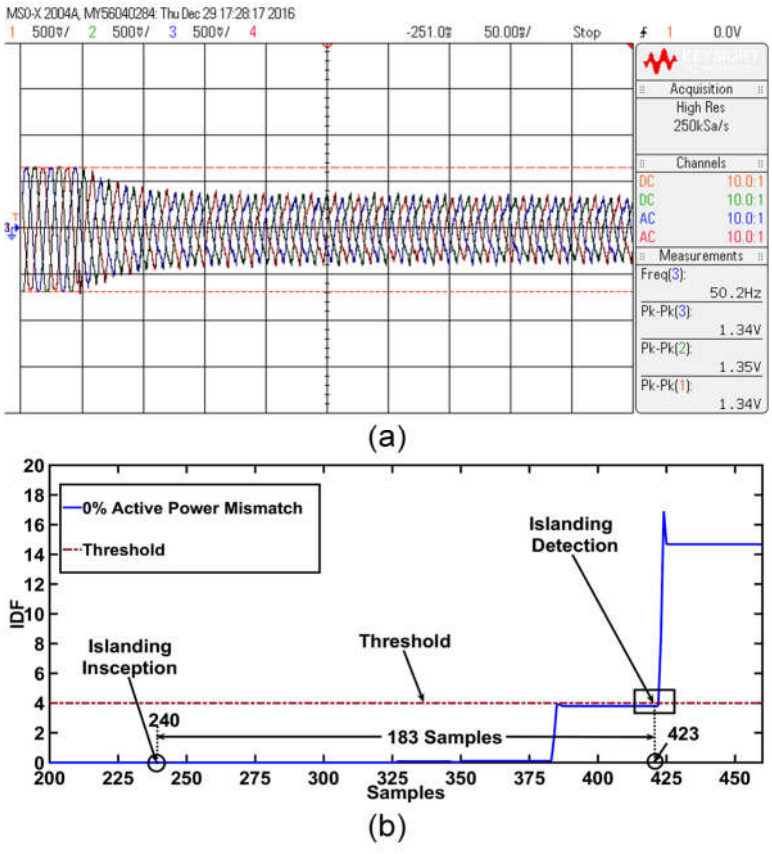


Fig. 4.10 Islanding with 0 % active power mismatch (a) voltage signals captured by DSO (b) response of the presented algorithm in terms of IDF.

4.4.2 Various non-islanding events

4.4.2.1 Faults on distribution feeder:

The performance of the presented algorithm has been evaluated through different types of faults on the distribution feeder with varying fault location and fault resistance. The fault location is varied by changing parameters of the distribution feeder (resistance and inductance). The fault resistance (R_f) is varied with the help of variable rheostat (45 Ω, 10 A) which is connected between phase and earth terminal through fault simulating switches S1, S2, and S3 (refer Fig. 4.4). Here, it is not possible to simulate solid fault (R_f = 0 Ω) due to practical limitation of equipment used in the laboratory prototype in terms of continuous and short time current carrying capability. Fig. 4.11 (a) shows the waveform of voltage signals acquired by the DSO during LG fault on phase C of the feeder at 20% fault location with R_f = 3 Ω. The response of the presented algorithm in term of IDF during the said situation is shown in Fig. 4.11 (b).

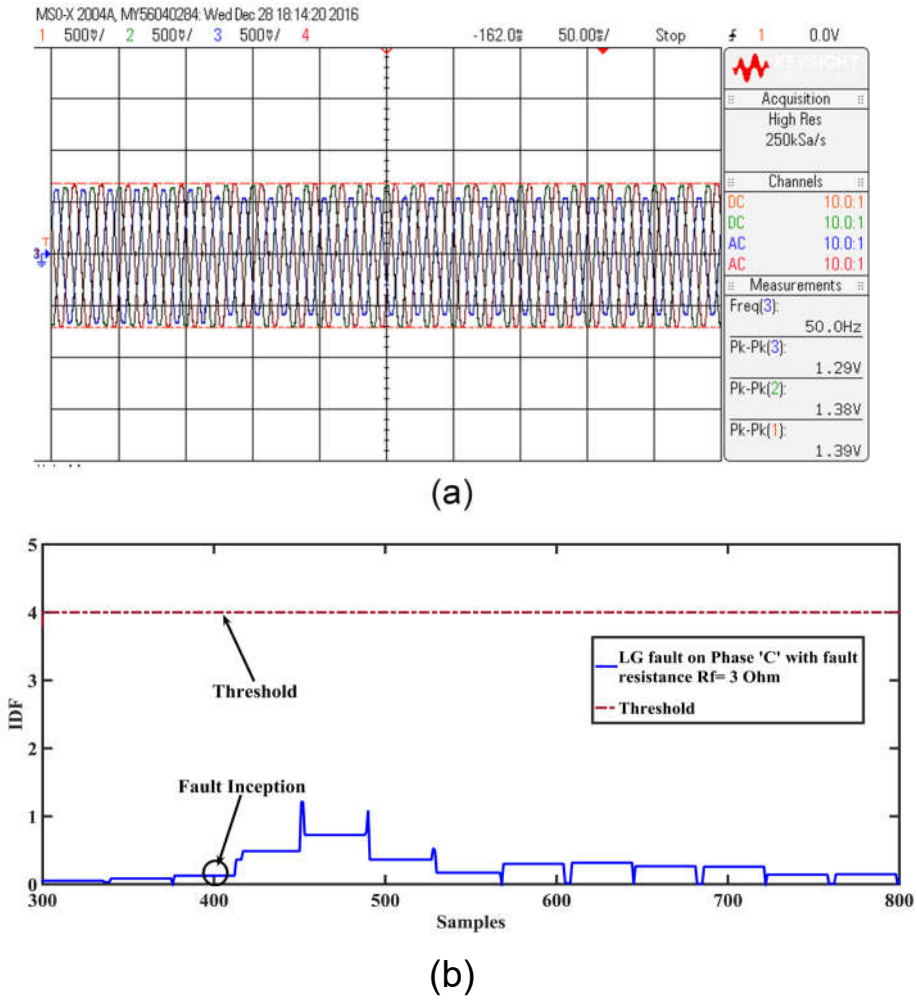


Fig. 4.11 LG fault on feeder with R_f = 3 Ω (a) voltage signals captured by DSO (b) response of the presented algorithm in terms of IDF.

It has been observed from Fig. 4.11 (a) that the voltage signal of the faulted phase has been reduced after the inception of fault on the feeder whereas the voltages of other two phases remain almost constant. It is observed from Fig. 4.11 (b) that though the value of IDF changes rapidly, its value stays well below the threshold value. Hence, the presented scheme remains stable during various types of faults on distribution feeder.

4.4.2.2 Switching of capacitor bank:

An APFC panel is widely used in the distribution network in order to improve power factor. This panel contains group of capacitors (also known as capacitor bank) which is continuously switch ON and OFF. It is necessary to discriminate this switching event with the islanding situation. The performance of the presented algorithm during switching of capacitor bank with 100% load has been evaluated. Fig. 4.12 (a) shows the waveform of voltage signals acquired by the DSO during switching of 80 µF (4.4 kVAR) capacitor bank connected at PCC. The response of the presented algorithm in term of IDF during the said situation is shown in Fig. 4.12 (b).

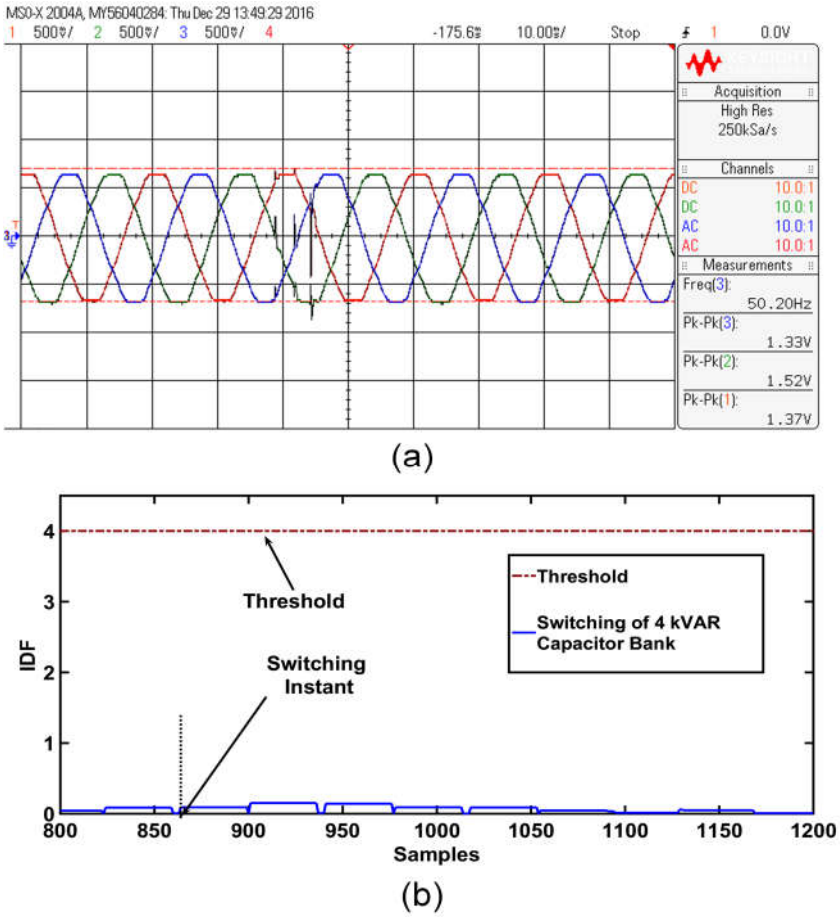


Fig. 4.12 Switching of capacitor bank at PCC (a) voltage signals captured by DSO (b) response of the presented algorithm in terms of IDF.

It has been observed from Fig. 4.12 (a) that though the voltage signals are disturbed during the switching of the capacitor bank, their magnitude is not large. As observed from Fig. 4.12 (b), the value of IDF stays well below the threshold value. Hence, the presented algorithm remains stable during the switching of capacitor bank.

4.4.2.3 Starting of Induction motor:

As the starting current of an induction motor is of the order of 6 to 7 times the full load current, it creates momentary voltage deviations. This condition is simulated in the laboratory prototype by starting 1 H.P. three-phase induction motor at 100% loading conditions. Fig. 4.13 (a) shows the waveform of voltage signals captured by the DSO. The response of the presented algorithm in term of IDF during the said situation is shown in Fig. 4.13 (b).

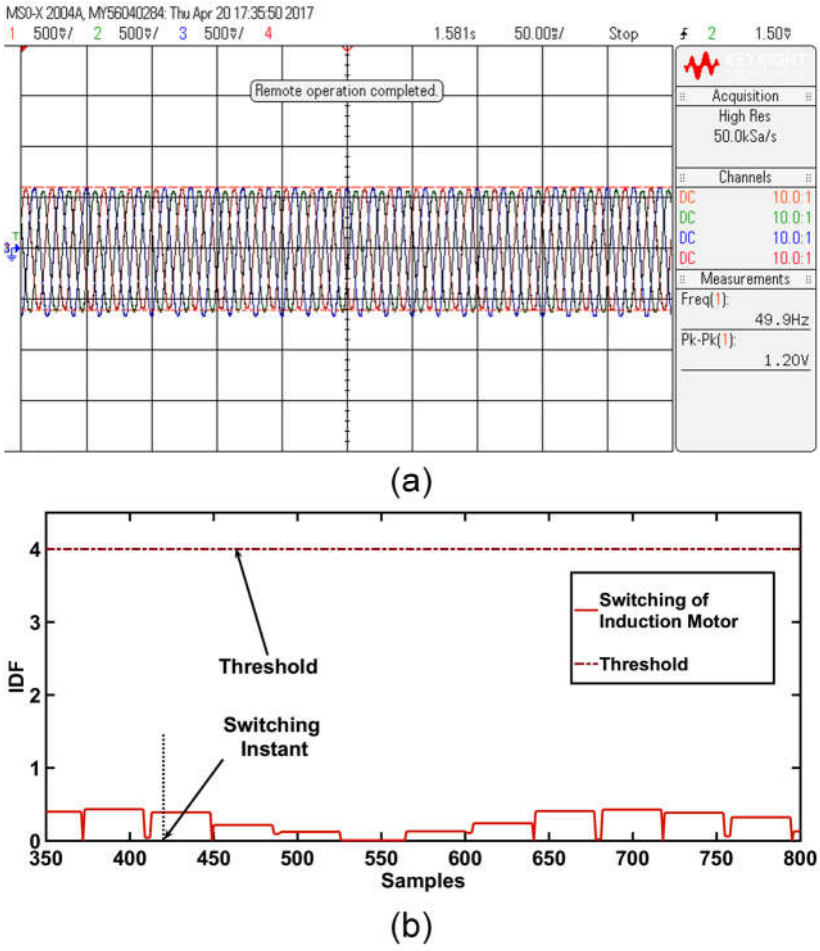


Fig. 4.13 Starting of induction motor at PCC (a) voltage signals captured by DSO (b) response of the presented algorithm in terms of IDF.

It has been observed from Fig. 4.13 (b) that the value of IDF stays well below the pre-set threshold. Hence, the presented algorithm identifies the above-mentioned event as non-islanding situation and does not initiate tripping.

4.4.2.4 Sudden change in load:

In order to verify the performance of the presented algorithm during sudden change in load, various percentage of load is suddenly increased/decreased (from 50 % to 150 % of the rated capacity in the steps of 5 %) on the target DG with reference to its rated capacity. Fig. 4.14 (a) shows the waveform of voltage signals acquired by the DSO during sudden increase in load of 150% on the target DG. The response of the presented algorithm in terms of IDF is shown in Fig. 4.14 (b). It is to be noted from Fig. 4.14 (b) that the value of IDF varies in a narrow range. However, it remains well below the threshold value. Hence, the presented algorithm provides better stability in case of sudden change in loading condition and does not initiate nuisance tripping.

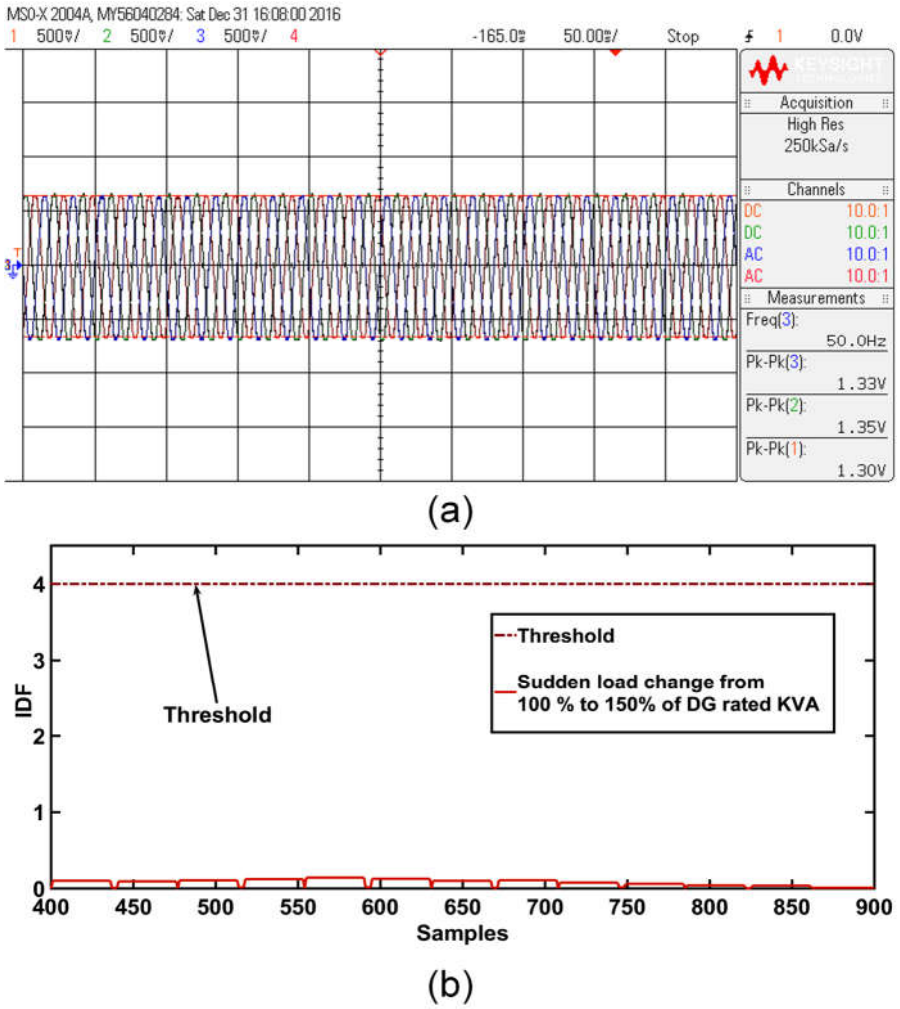


Fig. 4.14 Sudden change in load on target DG (a) voltage signals captured by DSO (b) response of the presented algorithm in terms of IDF.

4.4.3 Performance of the presented technique during low voltage ride through activation

The behavior of the proposed method is important in case of activation of low voltage ride through (LVRT). It has been observed from the past published papers that LVRT control strategies are mainly applied on wind farms/large PV plants [192]–[195]. Very few literature is available on the application of LVRT control strategy for the synchronous generator based DG. Meanwhile, the conventional practice for the LVRT control strategy is to simply disconnect the DG from the grid once the fault is detected. However, in order to avoid nuisance tripping of the DG during LVRT activation, researchers are presenting improved or modified techniques. The objective of this modified techniques is to avoid disconnection of DG during activation of LVRT depending upon time period specified in the grid code. The recent practice in the field is to inject the reactive current in support of the gird to boost up the voltage level up to 85% of nominal voltage during LVRT activation. Several observations, as given below, are noticed from the available literature for synchronous generator based DG during LVRT condition [195].

1. During LVRT condition, the active power is reduced to zero and it achieves its normal value after restoration of the voltage.
2. In case of LVRT, the grid is supported by the reactive current only.
3. The reactive power consumption must not exceed its specified limit after voltage restoration.

In a grid having a provision of both LVRT and anti-islanding protection, the DG is supported by frequency relay that trips the generator if frequency (f) exceeds higher and lower limits as given below.

$$47.5 < f < 51.5$$

The case wise performance of the proposed scheme during islanding in the presence of LVRT control technique is discussed below.

4.4.3.1 Case – 1: Islanding with perfect power balance condition/low mismatch of active power.

During islanding situation with perfect power balance or very low mismatch of active power, the RMS value of voltage does not reduce below 80% of the nominal voltage. Hence, the LVRT mode is not activated. In this event, the proposed islanding detection technique operates and disconnects the target DG.

4.4.3.2 Case – 2: Islanding with a higher mismatch of active power.

During islanding situation with a higher mismatch of active power, the RMS value of voltage drops below 80% of the nominal voltage (let say 15% of the nominal voltage). In this case, as LVRT mode is activated, the anti-islanding protection must be deactivated to avoid negative effects on the grid. In this situation, the active power generation of the synchronous DG becomes almost zero due to very high voltage dip. Hence, the DG will supply reactive current only for restoration of the voltage. Moreover, as per the latest amendment in IEEE 1547 standard [19], the restoration of the voltage must be done within 0.16 to 2.0 s when the voltage goes below 88% of the nominal voltage as otherwise the DG will be disconnected due to LVRT. It is to be noted that the developed laboratory prototype is not equipped with any LVRT control strategy. Therefore, the real-time analysis of the said situation is not possible in the laboratory environment.

4.4.4 Islanding detection time

The detection time of the proposed scheme depends on following parameters.

4.4.4.1 Phasor computation time:

The acquired voltage signals during islanding situation with 10% active power mismatch is shown in Fig. 4.15 (a) whereas the calculated phasor values of these signals are shown in Fig. 4.15 (b). The MDFT based phasor computation algorithm requires (N+3) samples where N is the number of samples/cycle (80). As depicted in Fig. 4.15 (b), from the occurrence of islanding inception (sample number 271), the 1st phasor of islanding instant is obtained at sample number 354 (271+83). From this instant, the phasor computation for the post islanding state is carried out using sliding window concept. Hence, with 4 kHz sampling frequency (sampling period = 0.250 *ms*), the phasor computation time is of the order of 83 × 0.250 = 20.75 *ms*.

4.4.4.2 Response time:

The sequence of islanding detection time in terms of IDF is shown in Fig. 4.15 (c). It is to be noted from Fig. 4.15 (c) that 40 samples of phasor values are required to calculate the first value of DFC as per equation (4.11). Hence, the first value of DFC is available at sample number 394 (354+40). Thereafter, as per equation (4.12), the first value of IDF is obtained by utilizing 40 samples of DFC. Hence, the first value of IDF is available at sample number 434 (394+40). Therefore, the minimum 163 (83+40+40) samples are required from the instance of islanding situation by the proposed algorithm to calculate the first value of IDF.

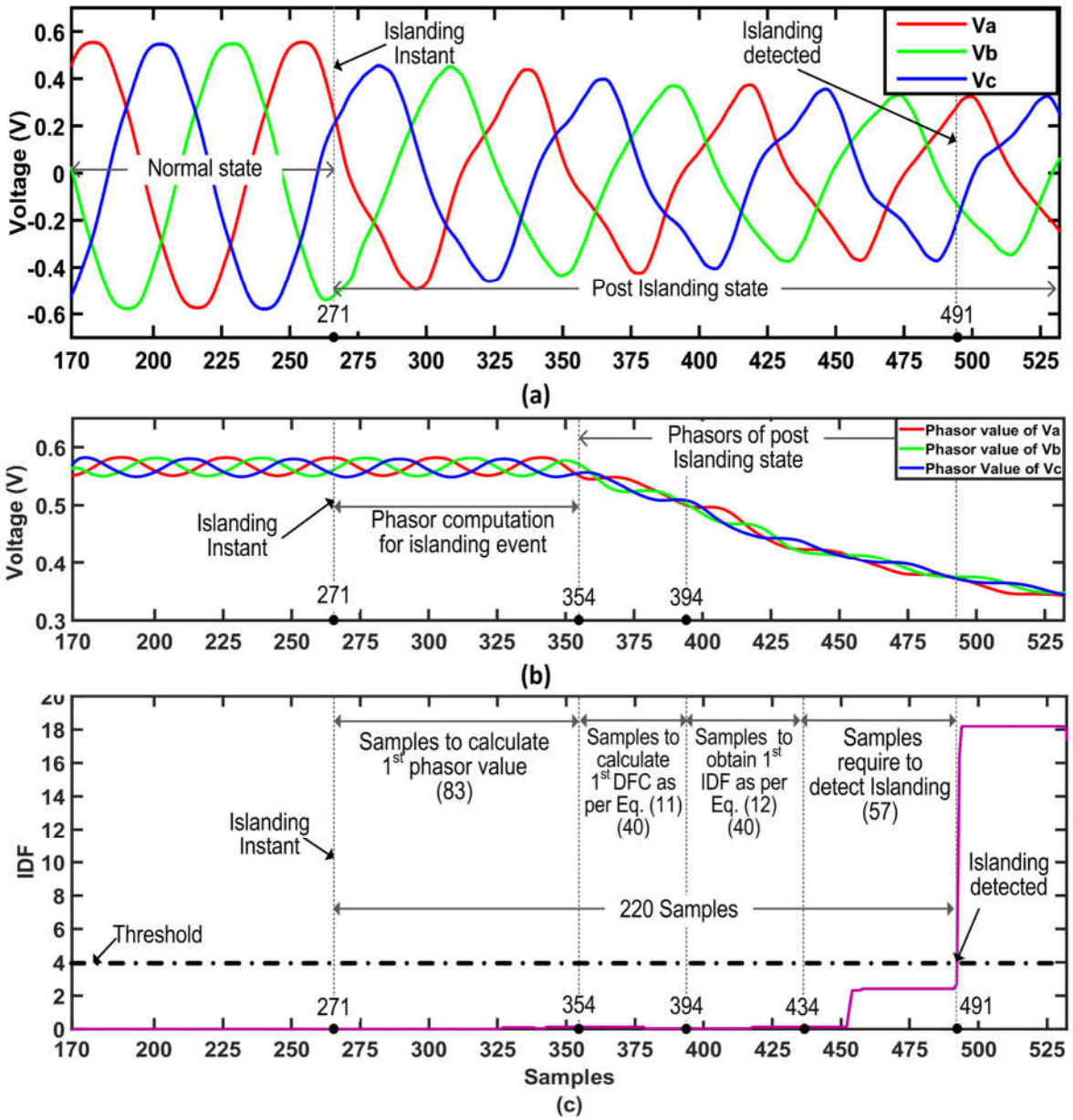


Fig. 4.15 Sequence of islanding detection time (a) acquired voltage signal during islanding (b) phasor values (c) response in terms of IDF.

Afterwards, few numbers of IDF samples are required for the detection of islanding situation until the threshold value is crossed. This depends on the percentage mismatch of active/reactive power of the target DG at the instant of islanding. For the specific case of +10% active power mismatch, as shown in Fig. 4.15 (c), the threshold value is crossed at sample number 491 (434 + 57). Therefore, the total number of samples required to detect islanding situation after phasor computation is 137 (491-354). It has been observed from various islanding situations (by varying active/reactive power mismatch) that the maximum number of samples required to detect islanding condition remains within 80 from the instance of calculation of the first value of IDF. Hence, the maximum number of samples required for islanding detection excluding phasor computation is 160 (40+40+80). This is equivalent to 40 *ms* (160×0.25 *ms*).

4.4.4.3 Program execution time:

As the processing speed of TMS320F28335 processor is 150 MHz, the instruction of the developed algorithm executes at a speed of 6.67 *ns*. Here, the size of the developed islanding detection algorithm is 5 kb. Hence, the overall time to execute the entire algorithm is 6.67 *ns* × 5 kb = 33.35 *ns*.

4.4.4.4 Propagation delay:

Propagation delay due to voltage sensing, scale down of voltage, analogue-to-digital conversion etc., is of the order of 5 *ms*. Finally, the islanding detection time, as per equation (4.13) is around 66 *ms*.

$$\text{Islanding detection time} = \text{Phasor computation time (20.75 } ms\text{)} + \text{Response time (40 } ms\text{)} + \text{Program execution time (34 } ns\text{)} + \text{Propagation delay (5 } ms\text{)} \approx 66\ ms \quad (4.13)$$

4.4.5 Comparative evaluation of proposed scheme with the existing schemes

Comparison of the proposed technique is carried out with the recently published techniques based on (i) oscillatory frequency [182] and (ii) inverse hyperbolic secant function [120].

4.4.5.1 Comparison with Oscillatory frequency-based method

The waveform of oscillatory frequency during islanding situation with perfect power balance condition is shown in Fig. 4.16 (a). Conversely, the performance of the proposed technique for the said situation is shown in Fig. 4.16 (b). It is to be noted from Fig. 4.16 (a) that the value of oscillatory frequency exceeds the threshold value. The oscillatory frequency stays well above the threshold value (2.5 Hz) during islanding situation with perfect power balance condition. Hence, the above scheme does not initiate trip signal. As the oscillatory frequency has to remain below the threshold value for the duration of two cycles, it requires more than six cycles to detect islanding condition from its inception. Conversely, as observed from Fig. 4.16 (b), the proposed technique is able to sense islanding situation with perfect power balance situation in three cycles.

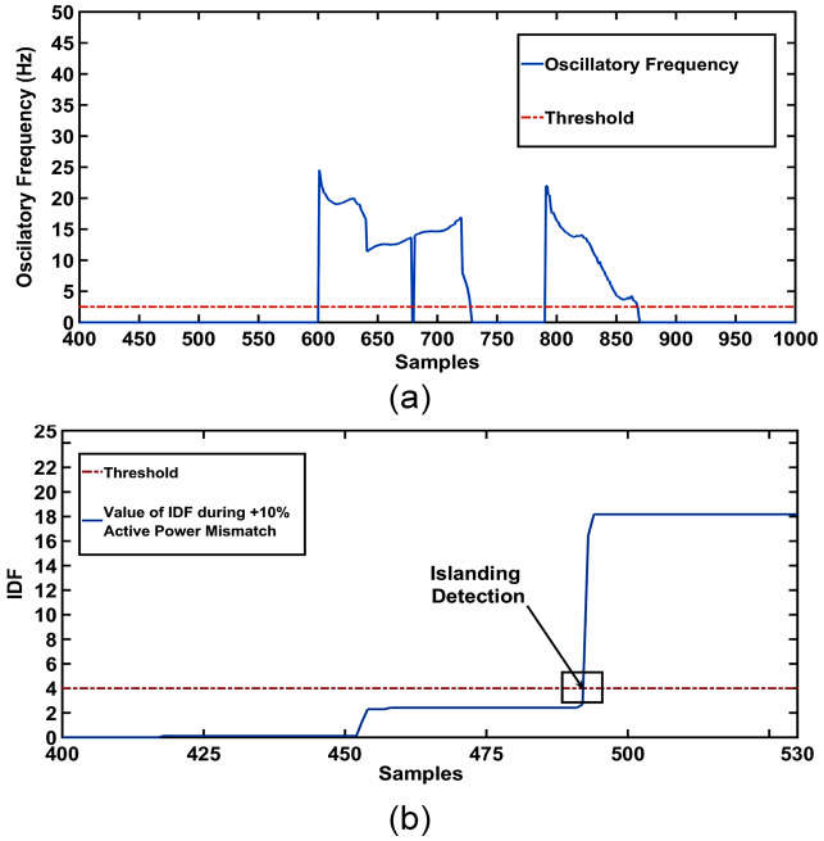


Fig. 4.16 Comparative evaluation during islanding situation with perfect power balance condition (a) the oscillatory frequency-based scheme (b) the proposed modal component based scheme

4.4.5.2 Comparison with Inverse hyperbolic secant function-based method

In order to compare the performance of the proposed method with the said method, an islanding situation with +5% active power mismatch is generated. The calculated value of rate of change of inverse hyperbolic secant function (ROCLNSV) is shown in Fig. 4.17 (a) whereas the response of the proposed technique during the said situation is shown in Fig. 4.17 (b). It has been observed from Fig. 4.17 (a) that the maximum value (2740) of ROCLNSV is obtained after 480 (680-200) samples i.e. after 120 *ms* (480 × 250 *us*) from the inception of islanding situation. The sample number 720 shows the 30% of the maximum value of ROCLNSV. Hence, the overall time span from the inception of the islanding situation to the 30% of maximum value is 130 *ms* (520 × 250 *us*) which is less than the pre-set time delay (135 *ms*). Therefore, the islanding situation is not detected by the said scheme. On the other hand, it is to be noticed from Fig. 4.17 (b) that the proposed scheme is capable to detect the islanding situation in 3 cycles.

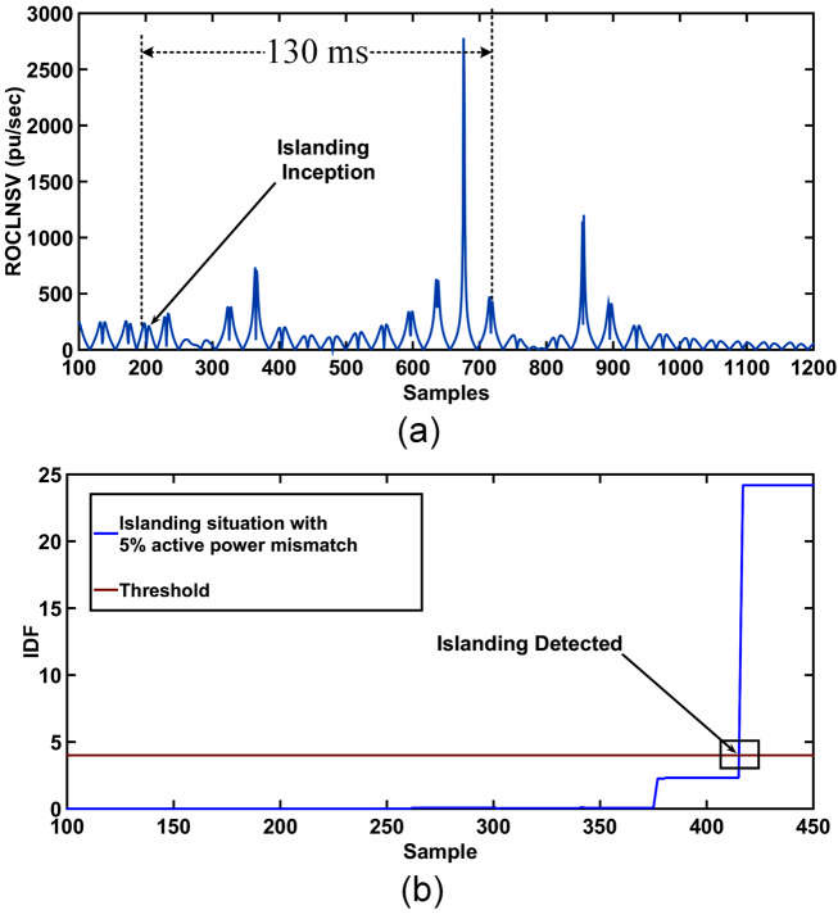


Fig. 4.17 Comparative evaluation during islanding situation with 5% active power mismatch (a) ROCLNSV based scheme (b) proposed modal component based scheme.

4.4.6 Advantages of the proposed technique

The proposed passive islanding detection technique has the following advantages over the existing one.

1. The proposed scheme is capable to detect islanding situation with low/zero mismatch of active/reactive power.
2. As the calculation of IDF requires utilization of phasor estimation algorithm and model transform, practical implementation of the proposed scheme is easier than the schemes based on wavelet transform/artificial intelligence.
3. The proposed scheme remains stable during non-islanding situation and hence, avoids nuisance tripping.
4. As the proposed scheme requires three and half cycle to detect islanding situation, it operates rapidly and hence, its time of operation is equally compatible as per IEEE 1547 standards.

4.4.7 Authentication of the proposed algorithm on the simulation test cases

In this chapter, the presented work is based on the prototype developed in the laboratory. However, due to limited funding, it is not possible to study the effect of inverter based DG on the proposed scheme.

However, as per the recommendation of the examiner, the performance of the presented islanding detection technique is verified by utilizing the simulation results obtained during various non-islanding and islanding situations on IEEE 34 bus distribution network containing both synchronous based DG and inverter based DG. The aforementioned IEEE 34 bus distribution network (as shown in Fig. 3.3 of Chapter-3), simulated in the RTDS/RSCAD platform. In this network, DG3 is an inverter based DG. The response of the proposed islanding detection technique in terms of IDF during islanding situation and non-islanding events (LG fault with fault resistance R_f = 3 Ω and 10 kVAR capacitor bank switching) are shown in Fig. 4.18 (a) and (b), respectively. It is to be noted from Fig. 4.18 that the value of IDF stays well below the threshold value during non-islanding events, whereas it exceeds the threshold value in case of islanding situation. Hence, the presented islanding detection technique is applicable to synchronous DG as well as inverter based DG.

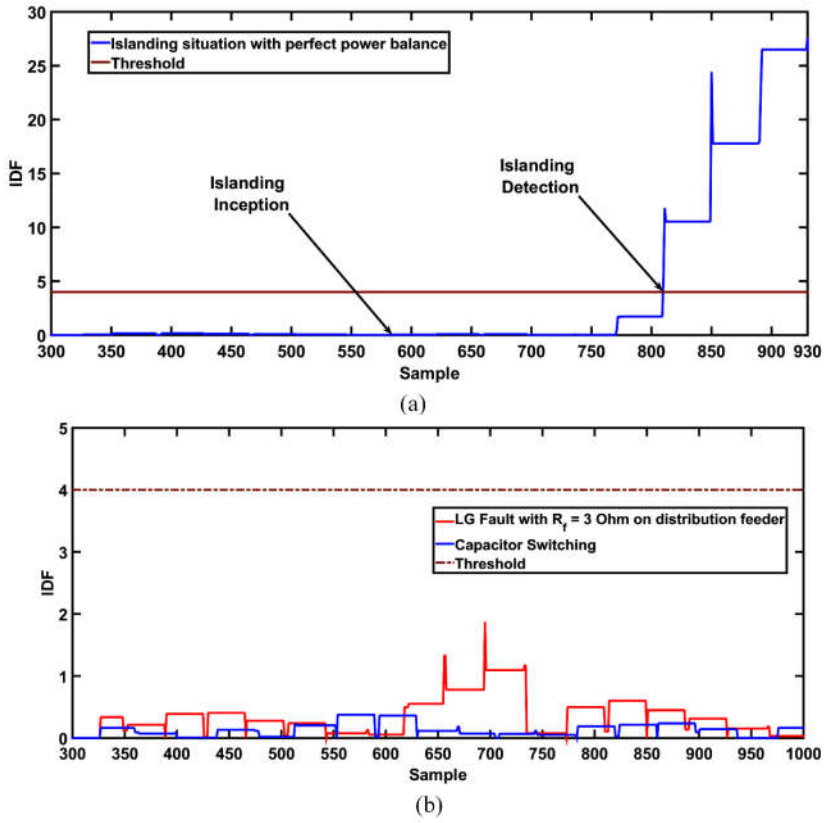


Fig. 4.18 Performance of proposed modal component based scheme during (a) islanding situation with perfect power balance condition and (b) non-islanding events.

4.5 Summary

In this chapter, a new islanding detection technique based on modal components of the voltage signals is presented. It is based on derivation of IDF from the model transformation of voltage signals acquired from the target DG. In order to evaluate performance of the presented scheme, a laboratory prototype has been developed which precisely resembles with the existing distribution feeder along with DG. From the developed laboratory prototype, 38 islanding cases and 685 non-islanding cases have been generated for the verification of the presented algorithm. The results clearly indicate that the proposed scheme is not only able to detect islanding situation within three and half cycles for different values of positive/negative active and reactive power mismatch but also capable to notice the same situation during perfect power balance condition. Subsequently, the proposed scheme does not initiate nuisance tripping during various types of non-islanding events. Finally, comparison of the proposed scheme with the existing schemes clearly indicate its superiority in distinguishing islanding situation with non-islanding events.

Concurrently, the presented algorithm has been tested from the test results obtained in previous chapter (Chapter 3). The results obtained in terms of IDF for islanding and non-

islanding test cases clearly show that the presented algorithm is capable to detect islanding situation with perfect power balance condition accurately. At the same time, it remains stable during non-islanding conditions. Hence, based on the test results obtained from simulation has well as from prototype, it could be said that the presented algorithm is able to detect islanding situation with all mismatch between load and generation utilizing inverter or synchronous based DG. Moreover, it remains immune to all non-islanding conditions.

.

Chapter 5

Hardware-In-Loop Testing of an Auto-correlation Based Islanding Detection Scheme

5.1 Introduction:

In the previous modal component based technique, the detection time is of the order of three and half cycle or higher. In order to further reduce this detection time, an accurate and fast islanding detection method is proposed in this chapter. This chapter describes a novel Islanding Detection Technique (IDT) based on a Discrimination Factor (DF) which is derived from an ACF of the voltage signals acquired from the terminal of the DG. The value of DF is calculated from the most affected lags of the ACF during various islanding and non-islanding conditions. Further, the validation of the presented scheme has been carried out by developing an HIL laboratory setup. In this setup, a power distribution network has been virtually developed in a RTDS/RSCAD which is physically connected to the DSP controller. Various non-islanding and islanding test scenarios have been generated on the developed HIL model.

5.2 ACF based islanding recognition approach

The flow-chart of the presented IDT, as shown in Fig. 5.1, is divided into three parts (i) Phasor computation, (ii) Auto-correlation factor and (iii) Discrimination factor.

5.2.1 Phasor computation

In this technique, the voltage signals of all the three phases are obtained at a sampling rate of 4 kHz from the DG terminal. For acquiring all these signals, 50 Hz fundamental frequency is considered. Further, a full-cycle MDFT algorithm [170], as explained in Chapter 3 (Section-3.2.2), is utilized to obtain phasor values of the input voltage signal which is capable of eliminating together integer harmonics as well as the decaying DC component. The MDFT algorithm gives estimated value of amplitude and phase angle of the fundamental frequency component which are further utilized for the calculation of modal components.

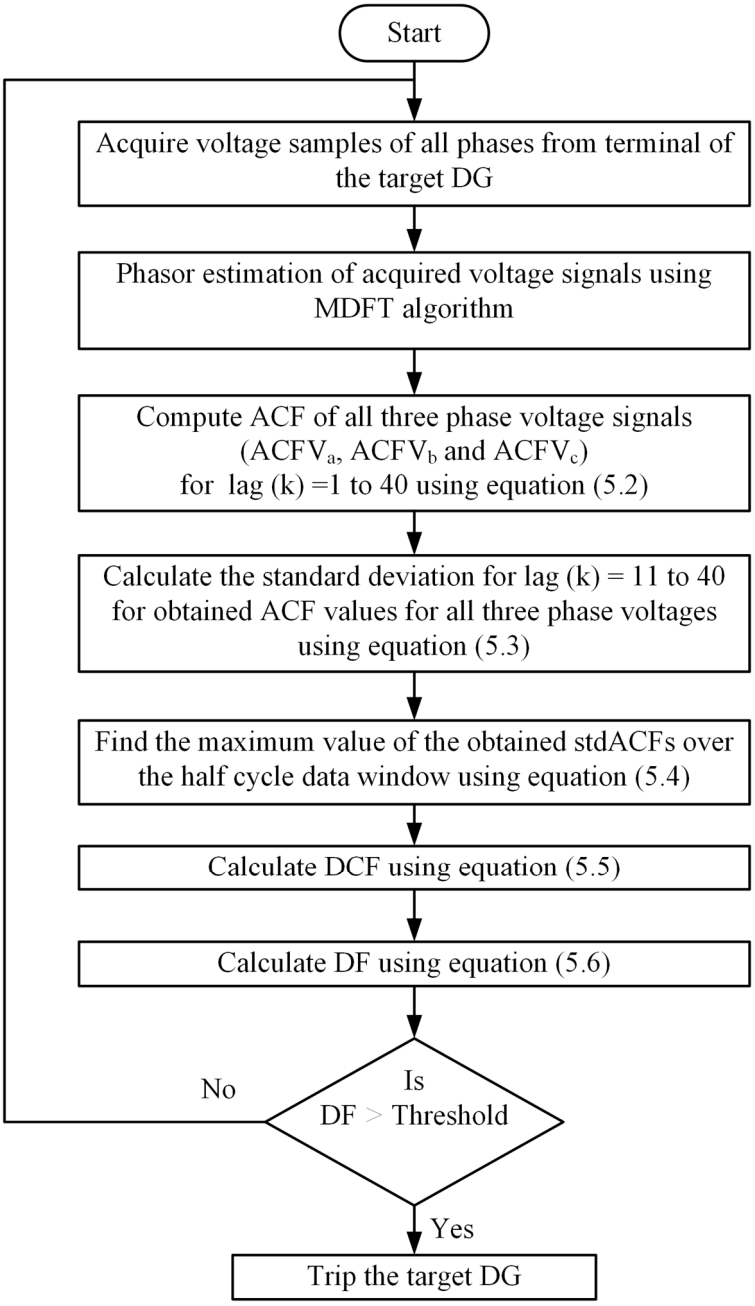


Fig. 5.1 Flowchart of the proposed islanding detection scheme.

5.2.2 Auto-correlation Factor

An ACF is used to find out the similarity of the input signal with itself at different time-steps (lags). It indicates the similarity between observations as a function of the time lag. Hence, it calculates the repeating patterns of the periodic signals in time domain. The ACF gives an index value which shows the similarity in terms of real number which remains in between -1 and +1, where +1 indicates perfect correlation and -1 indicates perfect anti-correlation. Mathematically, for *M* samples data, the correlation between the data at various time-steps (lags) can be given by (5.1).

$$\text{ACF}= r_k = \frac{\sum_{i=1}^{M-k}\left(x_i - x_\mu\right)\left(x_{i+k} - x_\mu\right)}{\sum_{i=1}^{M}\left(x_i - x_\mu\right)^2} \qquad \text{Where, } x_\mu = \frac{\sum_{i=1}^{M}\left(x_i\right)}{M} \tag{5.1}$$

Where, x_i is the value of signal at i^{th} sample, x_μ is the overall mean value of the samples and r_k is known as the ACF at lag k. In this algorithm, the three-phase voltage signals are obtained at 80 samples per cycle. Based on this fact, the maximum time lag is selected for half cycle data (i.e. for 40 samples). Therefore, the analysis of ACF is carried out for the time lag ranging from 1 to 40. The calculated ACF for three-phase (phase a, b and c) voltage signals (ACFV_a, ACFV_b and ACFV_c, respectively) are given by (5.2).

$$\text{ACFV}_a = \text{ACF}(\text{V}_a),\ \text{ACFV}_b = \text{ACF}(\text{V}_b),\ \text{ACFV}_c = \text{ACF}(\text{V}_c) \tag{5.2}$$

Where, ACF() is the function to calculate ACF of the given input signal. Fig. 5.2 (a) and (b) shows the ACF value of an acquired voltage signal with respect to varying time lag during normal and abnormal/transient condition, respectively.

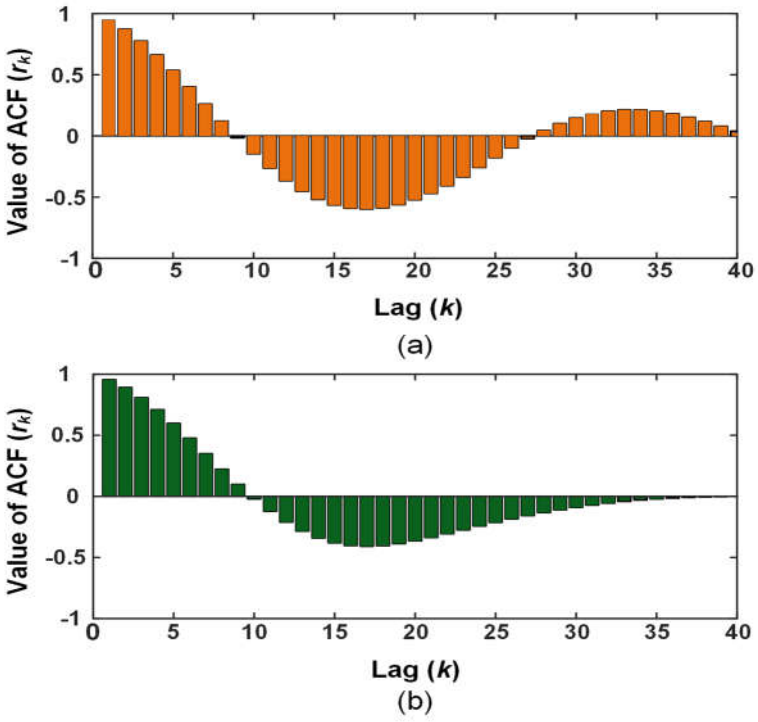


Fig. 5.2 Waveform of ACF values during (a) normal situation (b) abnormal/transient condition.

It is could be seen from Fig. 5.2 that the value of ACF is affected significantly for the time lag 11 to 40 during abnormal condition. Hence, in the proposed algorithm, the value of effective time lag is selected in the range of 11 to 40. The variations obtained during the said time lag is utilized for the calculation of the Discrimination Factor.

5.2.3 Discrimination Factor

The standard deviation of the calculated value of ACF for the most affected lags (between 11 to 40) of the three-phase voltage signals ($StdACFV_a$, $StdACFV_b$, and $StdACFV_c$) are given by (5.3).

$$\begin{aligned} StdACFV_a &= std(ACFV_a(11{:}40)) \\ StdACFV_b &= std(ACFV_b(11{:}40)) \\ StdACFV_c &= std(ACFV_c(11{:}40)) \end{aligned} \tag{5.3}$$

Where, std() indicates the standard deviation function and $ACFV_{a/b/c}()$ represents the ACF of three phase voltage signal for the specified lags (between 11 to 40). Further, the maximum value of $StdACFV_{a/b/c}$ over the specified length of window (w) is calculated using sliding window concept and given by (5.4).

$$\begin{aligned} Max\_StdACFV_a &= \max(StdACFV_a(i)) \\ Max\_StdACFV_b &= \max(StdACFV_b(i)) \quad \text{Where, } i = 1, 2, ...w. \\ Max\_StdACFV_c &= \max(StdACFV_c(i)) \end{aligned} \tag{5.4}$$

Where, max() indicates the function to obtain maximum value among the input argument. The values given by (5.4) are further utilized for the calculation of the discrimination factor coefficient as given by (5.5).

$$DFC=\sqrt{(Max\_StdACFV_a + Max\_StdACFV_b + Max\_StdACFV_c)} \tag{5.5}$$

Finally, the discrimination factor is obtained as per (5.6).

$$DF\ (\%) = \left(\frac{1-DFC}{DFC}\right)\times 100 \tag{5.6}$$

At last, the percentage DF value is matched with a predetermined threshold. If this value is larger than the predetermined threshold, an islanding state is confirmed. A proper choice of predetermined threshold is described in the following section.

5.3 Hardware-In-Loop Testing

To estimate the response of the given approach, an HIL test setup has been developed in the laboratory. The HIL test technique is a hybrid simulation technique in which a virtual real time simulation is interfaced to the physical hardware with the help of ADC and DAC. This testing technique provides flexibility in analysing response of a large power system network in real time due to the accessibility of real time signals.

5.3.1 Hardware devices

In the proposed work, RTDS/RSCAD has been used as a real-time simulator which is capable of performing electromagnetic transient analysis in real-time. This simulator has two major components namely (i) Hardware (RTDS) and (ii) Software (RSCAD). The hardware part contains high speed processor cards such as Triple Processor Card (3PC) and Reduced Instruction Set Code (RISC). These cards are installed in RTDS racks which are equipped with inter-rack and workstation communication facilities. In order to study a large system in RTDS/RSCAD, more than one rack can be interconnected with each other. This study is possible with the parallel processing of RTDS processors of different racks. The software part, which acts as a graphical interface for users, is equipped with various power system and other components that are used for the development of simulation model. The interfacing between software and hardware is carried out by ethernet cable.

In order to execute the presented algorithm in real time operation, a TMS320F28335 (C2000 Delfino series) DSP has been utilized. This is a low cost 32-bit fixed point processor basically used for real time protection and control applications. The DSP board is equipped with a 12-bit ADC having a sampling frequency of 12.5 Mega Samples/Second [189]. In addition, the auxiliary relay has also been used to initiate a trip signal.

5.3.2 Simulation model

Fig. 5.3 shows the circuit diagram of the network modal used in this scheme. The hardware setup of this network model has already been developed in the laboratory environment [196].The simulation modal of this network has been developed in RSCAD software package. In this model, a synchronous generator-based DG has been utilized. The parameters of various components such as distribution line, load, and DG are given in Appendix – B. As observed from Fig. 5.3, a utility supply (3-phase, line-to-line voltage = 415V, frequency = 50 Hz) is interconnected with the DG through a distribution feeder at a PCC. In the developed model, an islanding situation has been simulated with the help of utility circuit breaker. Furthermore, to evaluate the response of the presented approach during

islanding with different load-generation mismatch, series connected R-L load has been used on both sides of the PCC. In case of non-islanding events, provisions are made to simulate various events such as faults with variable fault resistance/location, starting of induction motor, switching of capacitor bank and sudden load change.

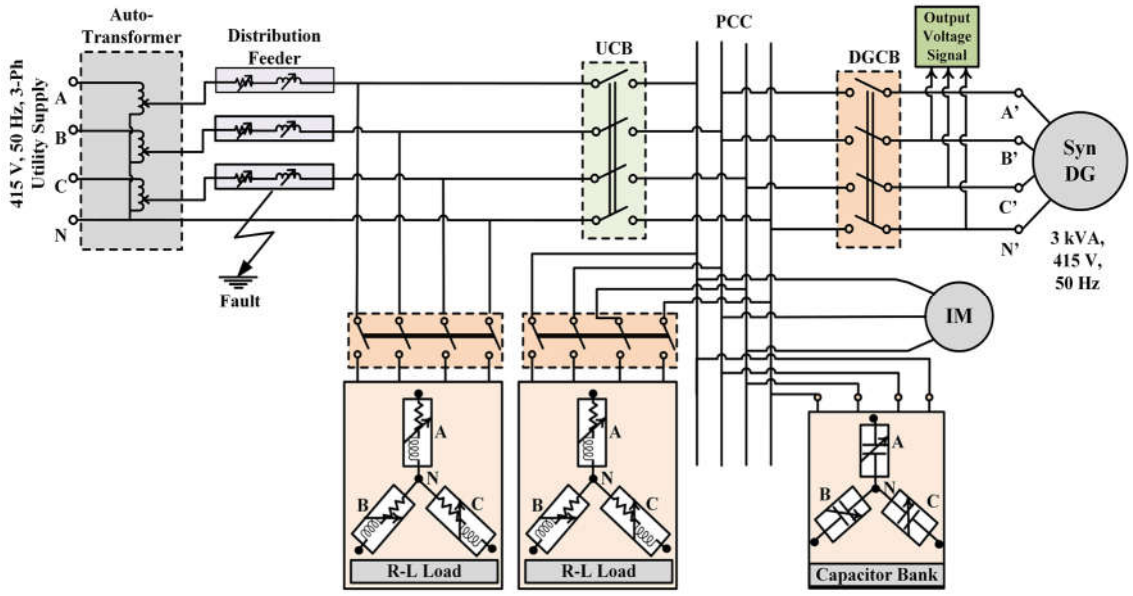


Fig. 5.3 Circuit diagram of the network modelled in RSCAD platform.

5.3.3 Signal acquisition and processing

Fig. 5.4 shows the practical implementation of the proposed algorithm in HIL test setup. As shown in Fig. 5.4, the developed simulation model is interfaced with the RTDS rack through ethernet cable. As the proposed algorithm is based on the voltage signal, the real time analogue voltage signals are physically acquired using Giga-Transceiver Analog Output (GTAO) card of RTDS. This card has 16-bit DAC with 12 analogue output channels. The analogue output voltage ranges from -10 V to +10 V. These signals are then exported to the DSP for the execution of the algorithm. Moreover, the presented approach is written in MATLAB and compiled with the help of CCS v5.1 which has been interfaced with the DSP through XCS510PP emulator pod [190]. On the detection of islanding state by the proposed approach, a trip signal is initiated which is further given to the auxiliary relay. The auxiliary relay is connected to Giga-Transceiver Digital Input (GTDI) card of RTDS which converts analogue signal to digital signal. The output of GTDI card is further utilized to disconnect the DG connected in the developed simulation model. Additionally, a DSO has been used in the developed HIL model to capture the voltage signal waveforms for different operating states.

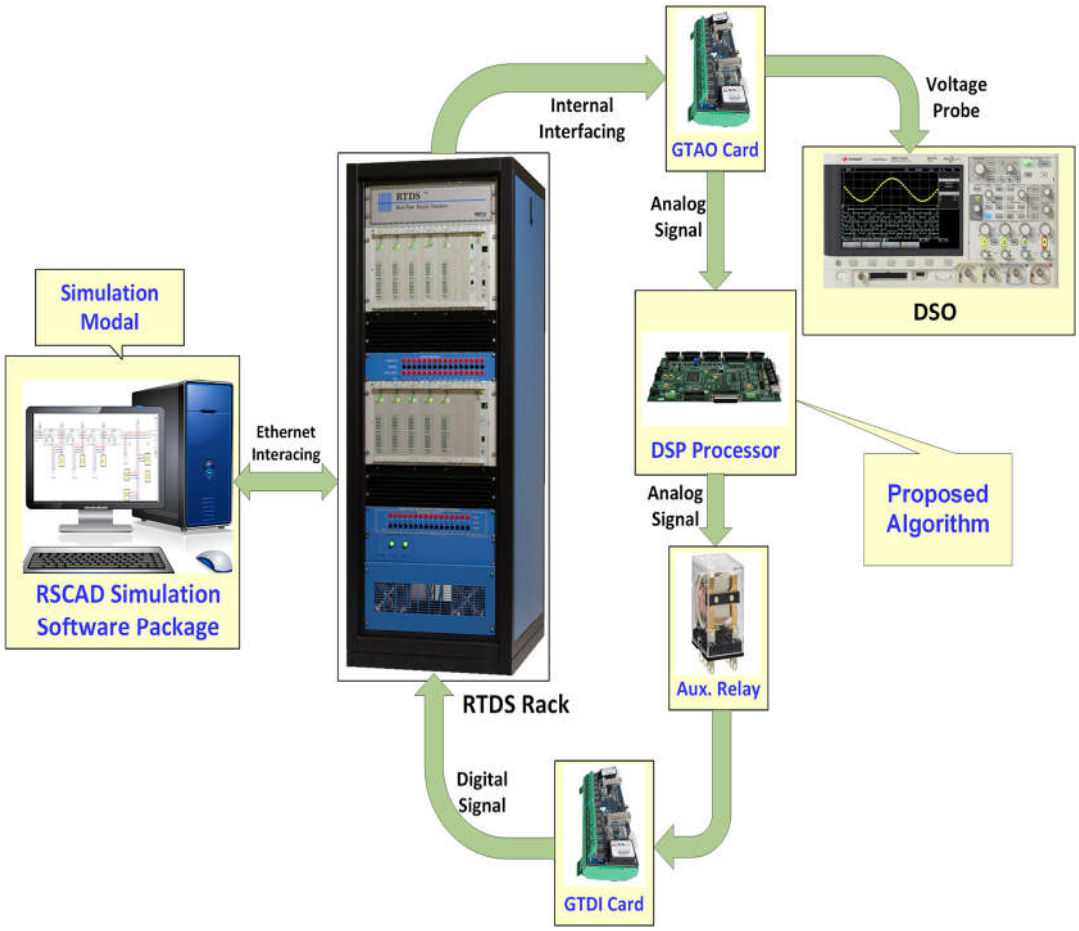


Fig. 5.4 Developed HIL test setup.

5.3.4 Test cases generated

To validate the response of the presented approach, diverse islanding and non-islanding conditions, as depicted in Table 5.1, have been developed. It could be seen from Table 5.1 that among total 626 generated test cases, 46 are for islanding situation whereas 580 are for non-islanding conditions. These cases are utilized by the proposed algorithm.

Table 5.1 Diverse non- islanding/islanding test cases generated from the HIL setup.

Event		Parameter variations		Cases
Non-islanding conditions				
1	Faults on feeder	Various faults: LG, LL, LLG, LLLG	Total fault = 10	10 × 9 × 4 = 360
		Fault Resistance (R_f):0.1, 1, 3, 5, 10, 15, 20, 25, 30	Total R_f = 9	
		Fault location for UCB: 25%, 50%, 75%, 100%.	Total location = 4	
2	Sudden load change	Sudden change in load: 50% to 150% in step of 5%	Total cases: 20	20
3	Capacitor bank switching at PCC	Capacitor bank ratings:1 kVAR to 5 kVAR in step of 1 kVAR	Capacitor ratings: 5	5 × 20 = 100
		Variations of load on DG: 50% to 150% in step of 5%	Total load cases: 20	
4	Induction motor starting at PCC	Induction motor ratings:1 H. P. to 5 H. P. in step of 1 H. P.	Induction motor ratings: 5	5 × 20 = 100
		Variations of load on DG: 50% to 150% in step of 5%	Total load cases: 20	
Islanding events				
5	Islanding with active power mismatch	-50 % to -5% mismatch in step of 5%	Cases: 11	11+1+11 = 23
		0% mismatch	Cases: 1	
		+5 % to +50% mismatch in step of 5%	Cases: 11	
6	Islanding with reactive power mismatch	-50 % to -5% mismatch in step of 5%	Cases: 11	11+1+11 = 23
		0% mismatch	Cases: 1	
		+5 % to +50% mismatch in step of 5%	Cases: 11	
Total Non-islanding and islanding cases generated				580 + 46 = 626

5.3.5 Selection of threshold

As discussed earlier, the detection of islanding state by the presented scheme depends on the percentage value of threshold. The proper value of threshold plays an important role and hence, its selection must be carried out very carefully. In this work, selection of threshold is carried out based on mathematical analysis. The same can be further validated by observing the pattern of DF for various non-islanding and islanding states performed on HIL test setup.

5.3.5.1 Threshold based on mathematical analysis

The proposed algorithm depends on variations in the magnitude and angle ($|V_a|, |V_b|$ & $|V_c|$ and θ_a, θ_b & θ_c) of the acquired voltage signals in case of healthy/abnormal conditions. During healthy situation, the calculated value of standard deviation of the ACF as per (5.3) for lags 11 to 40 is almost zero. Conversely, these values for non-islanding and islanding events are in the range of -1 to +1. Similarly, the maximum value of standard deviation of the ACF, calculated as per (5.4), also remains within ± 1. Now, the value of DFC, derived as per (5.5), remains less than 1.0. Hence, as per (5.6), the value of DF is represented in terms of percentage variation

with respect to DFC. Therefore, in order to decide the threshold value, the magnitude and phase angle variations during islanding and non-islanding states are assumed in the range of ± 20% and ± 25º, respectively, with reference to nominal voltage of the DG. The highest value of DF obtained for different non-islanding and islanding states with respect to the variation in the voltage magnitude and phase angle are depicted in Table 5.2. It can be concluded from Table 5.2 that the highest percentage DF value during non-islanding state remains well below 15 whereas its value stays well above 30 in case of islanding situation.

Table 5.2 Calculated maximum percentage value of DF for islanding and non-islanding states.

Sr. No.	Event	Deviation in the magnitude of voltage (pu)	Deviation in the angle of voltage (º)	Highest percentage DF value
Non-islanding situations				
1.	Faults on distribution feeder	0.0 to 0.8	-20º to + 20º	13.65
2.	Abrupt change in load	0.8 to 1.20	-20º to +20º	5.67
3.	Abrupt induction motor starting	0.0 to 0.85	-20º to +20º	4.16
4.	Capacitor bank switching	0.8 to 1.20	-20º to +20º	5.15
Islanding conditions				
5.	Perfect active power balance	0.75 to 1.25	-25º to +25º	30.62
6.	-50% active load-generation power mismatch	0.00 to 1.25	-25º to +25º	31.85
7.	Perfect reactive power balance condition	0.75 to 1.25	-25º to +25º	31.67
8.	-50% reactive load -generation power mismatch	0.00 to 1.25	-25º to +25º	32.16

5.3.5.2 Threshold based on results obtained from HIL test setup

The percentage DF value obtained with the help of mathematical analysis has been verified from the test scenarios generated, as shown in Table 5.1, on the HIL setup. The found maximum percentage value of DF found for various scenarios is given in Table 5.3.

Table 5.3 Highest percentage DF value achieved through HIL test scenarios.

Sr. No.	Event	Highest percentage DF value
Non-islanding states		
1.	Faults feeder	12.05
2.	Capacitor bank switching	5.83
3.	Abrupt induction motor starting	5.21
4.	Abrupt load change	5.64
Islanding state		
5.	With diverse load-generation mismatches.	32.80

It could be seen from Table 5.3 that the percentage DF value changes in a range of 3 to 12 for non-islanding states. Simultaneously, it could be noted from Table 5.3 that the highest percentage DF value for islanding state is of the order of 32.8. The tendency of the maximum percentage value of DF for islanding state in case of diversified active/reactive load-generation mismatches is also represented in Fig. 5.5. It is noticed from Fig. 5.5 that the percentage value of DF remains almost constant during islanding condition with different values of load-generation mismatches. However, the smallest and largest percentage DF value alter in the band of 29.6 to 32.8, respectively, in the said situation. At the same time, this is clear from Table 5.2 and Table 5.3 that the largest percentage DF value for the non-islanding state is lower than 15. Henceforth, with an adequate safety margin with reference to the largest percentage value of DF for the non-islanding state, the threshold value of 25 is chosen.

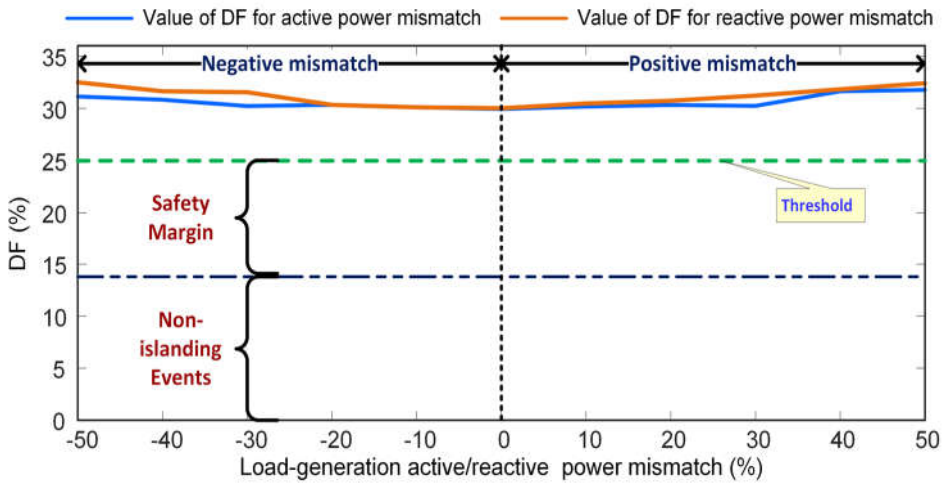


Fig. 5.5 Tendency of the percentage value of DF for islanding state with diversified load-generation power mismatch.

5.4 Results and discussion

5.4.1 Islanding with different active/reactive power mismatches

To analyse the response of the proposed approach, three different cases of islanding events (i) with +10% mismatch in active power (ii) with -5% mismatch in reactive power and (iii) with 0% mismatch in active power have been considered. The simulation results given by the proposed scheme in terms of the value of DF are shown in Fig. 5.6. It could be seen from Fig. 5.6 (a) and (b) that the percentage DF value crosses the pre-set threshold and stays well above the threshold. This indicates that the presented approach is capable of detecting islanding state efficiently for different mismatches of active and reactive power. Moreover, it can be

concluded from Fig. 5.6 (c) that the percentage DF value crosses the threshold at sample number 413. Hence, the presented approach spots the islanding situation within three cycles (173 samples). Therefore, the presented approach is also capable of detecting islanding state accurately even with 0% active power mismatch.

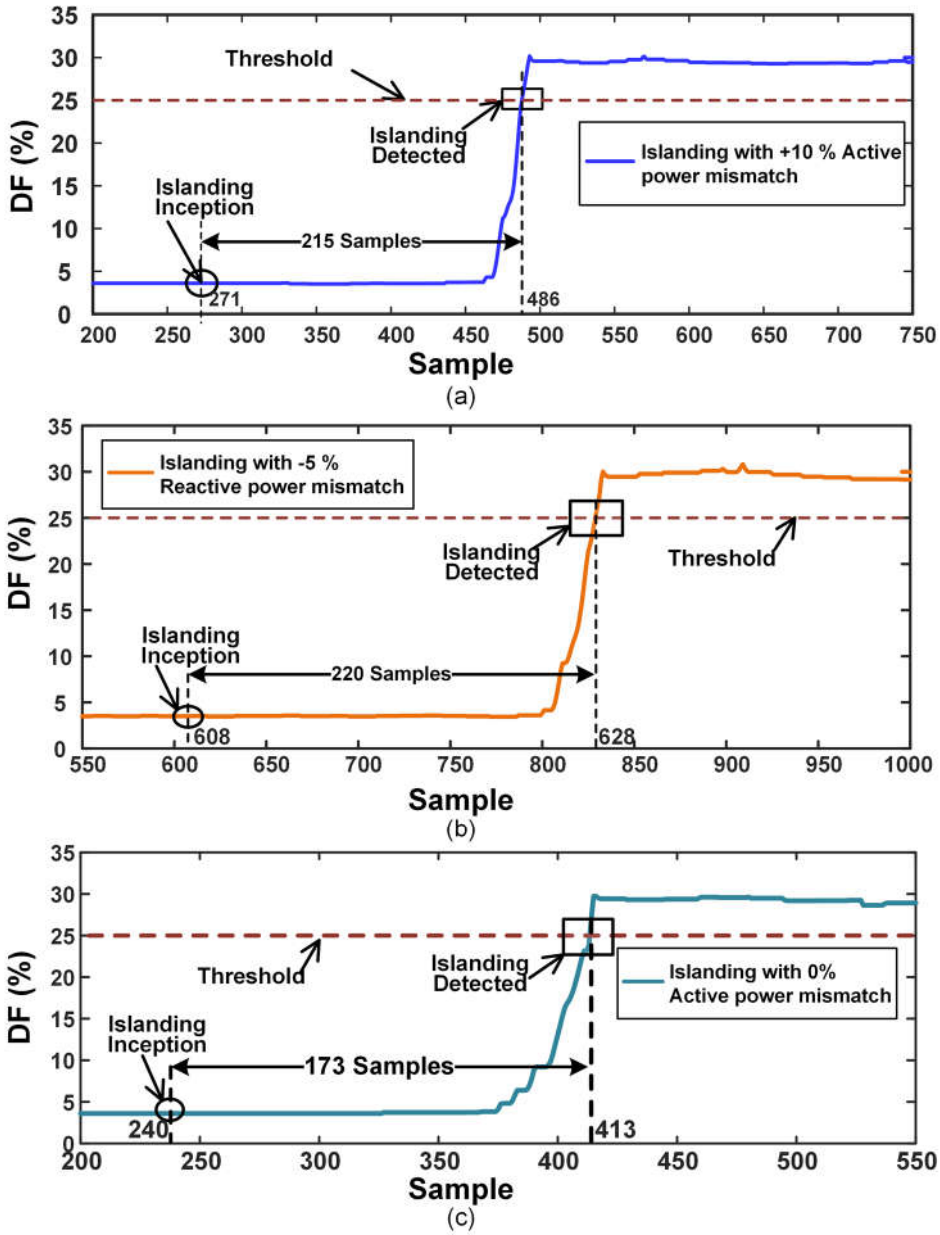


Fig. 5.6 Response of the proposed scheme in terms of DF during islanding situation with (a) +10% active power mismatch (b) -5% reactive power mismatch (c) 0% active power mismatch

5.4.2 Non-islanding conditions

5.4.2.1 Feeder faults and abrupt load change

To examine response of the presented approach for critical non-islanding conditions,

various cases of faults on distribution feeder and sudden change in load have been performed on the HIL setup. Fig. 5.7 (a) shows the response of the proposed approach in the form of DF during an LG fault with R_f = 1 Ω and fault location of 25% of line length from the PCC. At the same time, the response of the proposed approach in the form of DF for abrupt load change (from 100% to 150%) is depicted in Fig. 5.7 (b).

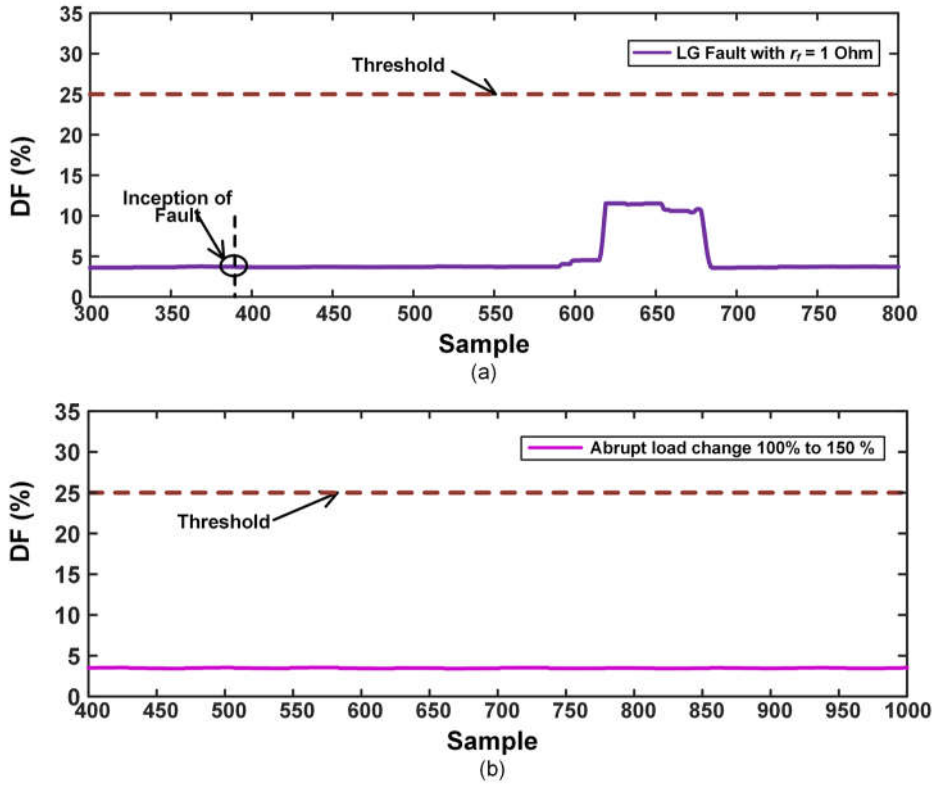


Fig. 5.7 Response of the presented algorithm in terms of DF during (a) LG fault on feeder with Rf = 1 Ω (b) abrupt load change on target DG.

It can be concluded from Fig. 5.7 (a) that the percentage DF value suddenly rises to nearly 11 during feeder fault and maintains the same value up to sample number 678. Subsequently, as spotted from Fig. 5.7 (b), the effect of sudden load change does not affect the pattern of DF significantly. In both the cases mentioned above, the value of DF remains well beneath the threshold. Hence, the proposed approach maintains proper stability for critical non-islanding events and does not issue a trip command.

5.4.2.2 Capacitor Bank switching and starting of Induction Motor

Manufacturing/Engineering industries are one of main users of DG. In these industries, a large number of induction motors are utilized. Consequently, to maintain the power-factor close to unity, variable capacitor banks are installed. Therefore, the response of the proposed scheme must be verified during frequent starting of the induction motor as well as in case of

switching of Capacitor Bank. Here, in the developed HIL setup, a variable Capacitor Bank and different rating of Induction Motor are used to generate various simulation cases of switching/starting of Capacitor Bank/Induction Motor. Fig. 5.8 (a) shows the response of the presented approach in the form of percentage DF value for switching of 4 kVAR Capacitor Bank with 100% load on the DG. At the same time, the response of the presented scheme in case of starting of 5 H.P. Induction Motor with 100% load on the DG is also depicted in Fig. 5.8 (b).

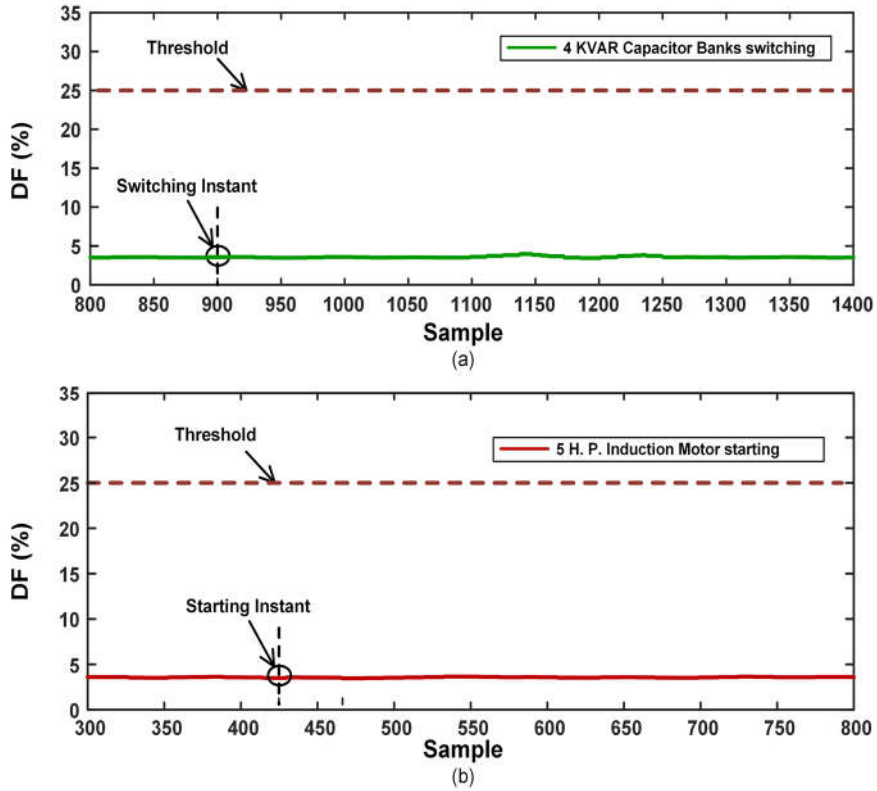


Fig. 5.8 Response of the proposed approach in form of percentage DF value for (a) Capacitor Bank switching and (b) Induction Motor starting at PCC.

It can be concluded from Fig. 5.8 (a) and (b) that in both the cases the value of DF stays well beneath the threshold. Therefore, the presented approach works fine for Capacitor Bank switching and Induction Motor starting.

5.4.3 Detection Time

To calculate the detection time of the presented approach, one of the islanding case with -5% reactive power mismatch has been evaluated. The sequence of islanding detection time given by the proposed scheme for the said case is shown in Fig. 5.9.

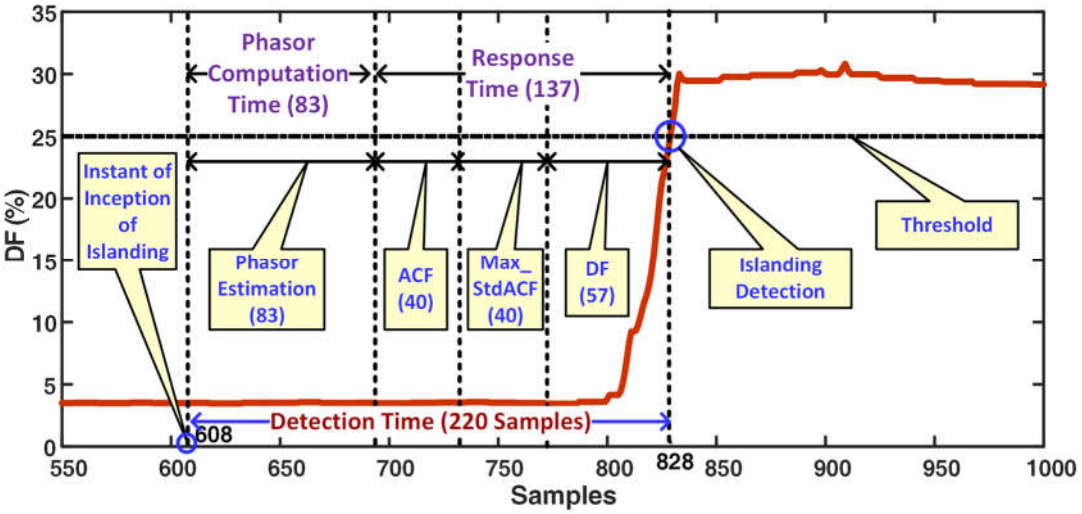


Fig. 5.9 Islanding detection time sequence.

As observed from Fig. 5.9, the entire islanding detection time is divided into phasor computation time, response time, program execution time, and propagation time. Based on this fact, the event wise calculation of islanding detection time is depicted in Table 5.4. As the phasor computation takes minimum 83 samples, the first estimated value of phasor is obtained at 20.75 *ms*. This is based on 4 kHz sampling frequency (0.250 *ms* per sample). Hence, the phasor computation time comes out to be $83 \times 0.250 = 20.75$ *ms*. After that, the response time is based on the total numbers of samples (137) involved in various mathematical calculation after phasor computation. This includes a number of samples involved in the calculation of ACF (40), Max_StdACF (40), and DF (57). It is to be noted that the number of samples required for the calculation of DF varies with respect to the mismatch in load-generation power. Therefore, the total numbers of samples utilized for islanding detection are 220 (83+40+40+57) from the inception of the event. This 220 samples are equivalent to 55 *ms*.

However, in the actual field, the program execution time, and the time due to propagation delay are inevitable. The execution time depends on the speed of the DSP processor. In this case, for TMS320F28335 processor, it is 150 MHz which is equivalent to 6.67 *ns* per instruction. Therefore, the overall islanding detection time from the inception of the islanding event would be around 60 *ms* which is equivalent to three cycles.

Table 5.4 Detection time calculations.

Islanding Detection Time Parameter	Samples required	Time
Phasor computation time	83	83 × 0.250 = 20.75 *ms*
Response time	137	137 × 0.250 =34.25 *ms*
Program execution time	--	6.67 *ns* × 5 kb = 33.35 *ns*
Propagation delay	--	5 *ms*
Total Detection Time		60.00 *ms*

5.4.4 Comparative assessment

The comparative assessment of the proposed scheme in terms of the percentage value of NDZ and detection time with the techniques based on ROCOF [87], Overvoltage /Undervoltage and Over Frequency/Under Frequency [83], Wavelet Transform [113], Data mining [197] , SVM/ RVM classifiers, respectively [112], [198], Oscillatory frequency [182], and Artificial Neural Network (ANN) [109] has been carried out. Table 5.5 shows the comparison of the proposed technique with the technique mentioned above.

Table 5.5 Comparative assessment of the proposed scheme.

Islanding detection schemes	NDZ	Detection Time	Limitation
ROCOF	> 15%	>70 *ms*	It has large value of NDZ in case of lower power mismatches.
Oscillatory frequency	< 5%	> 45 *ms*	It is very difficult to decide multiple thresholds.
OV/UV and OF/UF	> 15%	10 *ms* to 2 *s*	It issues nuisance tripping during critical non-islanding events.
Wavelet Transform	< 1%	10 *ms* to 50 *ms*	It requires both current and voltage signals which increases overall cost.
ANN	<=10 %	>=0.5 *s*	It has large islanding detection time.
Classifier (SVM)	<1 %	>= 20 *ms*	It is sensitive to unseen non-islanding events and hence, issues false tripping.
Data Mining	<5 %	> 200 *ms*	Multiple input signals are required which increases complexity and cost.
Proposed scheme	No-NDZ	<= 60 *ms*	

It is to be noted from Table 5.5 that the conventional techniques such as OV/UV, OF/UF, and ROCOF offer higher value of NDZ particularly in case of a lower mismatch between load and generation power. Further, these techniques may initiate false tripping during critical non-islanding events. Subsequently, it could be seen from Table 5.5 that the techniques based on WT, ANN, SVM, and Datamining are unable to detect islanding condition during balanced power condition. Further, the detection time of these techniques ranges in between 10 *ms* to 0.5 *s*. Moreover, the requirement of multiple input signal, difficulty in hardware implementation and susceptibility to noise and unseen pattern of islanding/non-islanding events are other limitations of the aforementioned schemes. On the other hand, the proposed

technique is economical compared to the multi-feature-based scheme as it requires only one input signal. Further, unlike other techniques, utilization of MDFT algorithm by the proposed technique makes the input signal free from noise and higher order harmonics. Moreover, it remains stable against all types of critical non-islanding events and hence, does not initiate nuisance tripping in case of unseen patterns. Also, the proposed scheme is easy to implement in real time as its applicability has been verified on the developed HIL test setup.

5.5 Summary

In this chapter, a novel IDT based on ACF of the voltage signals is presented. The appropriateness of the proposed scheme has been carried on a Hardware-In-Loop setup established in the laboratory. A large number of islanding and non-islanding test scenarios have been created on the developed test setup. The results confirm that the presented approach is capable of distinguishing islanding state with non-islanding states correctly and quickly (within three cycles from the inception of islanding). Moreover, it is also capable of recognizing islanding state even in the case of a perfect power balanced condition. Additionally, it offers improved steadiness in contrast to various non-islanding states and hence, avoids nuisance tripping. Finally, a relative assessment of the proposed approach compared with other techniques in terms of NDZ and detection time prove its superiority. However, the research work involving the presented ACF based islanding technique is under the review of experts. Hence, it could be said that there may be a chance of improvement in the presented work.

Chapter 6

Restoration of Recloser-Fuse Coordination for DG interfaced Distribution Network

6.1 Introduction:

This chapter presents a new adaptive technique to restore coordination between recloser and fuse connected in the distribution network in the presence of DGs. The proposed technique is based on the derivation of modification factor which is defined as the ratio of the calculated value of positive sequence impedance seen by a recloser (Z_{1cal}) to its predefined value ($Z_{1preset}$). Based on the value of MF, the recloser fast TCC has been altered. The value of Z_{1cal} is obtained by acquiring samples of currents and voltages at the location of the recloser. The performance of the proposed scheme has been evaluated by modeling IEEE 34 bus network in RTDS/RSCAD environment. At the same time, appropriateness of the proposed scheme has been verified on a practical setup developed in the laboratory.

6.2 Proposed adaptive relaying algorithm

6.2.1 Practical radial DN and usual practice

As shown in Fig. 6.1, the secondary distribution of power is carried out with the help of distribution transformers, distribution feeders, and laterals. Further, Inverse Definite Minimum Time (IDMT) overcurrent relay, recloser, and fuse are used for the protection of DN.

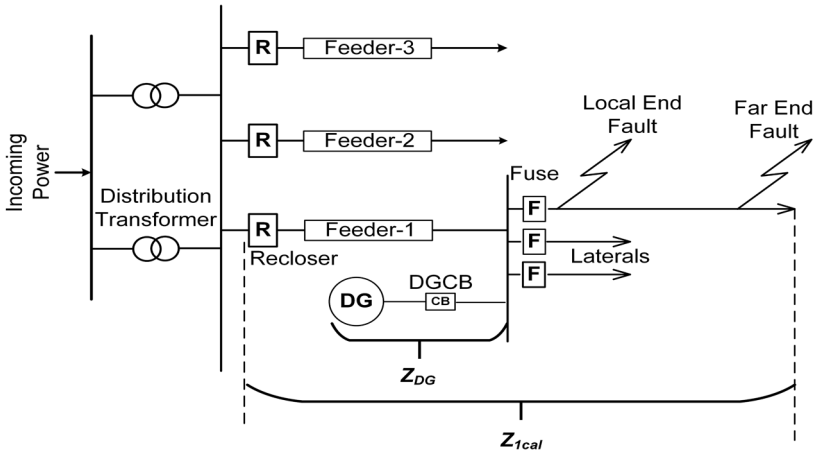


Fig. 6.1 Single line diagram of a typical radial DN with DG.

As the majority of faults on DN are transient in nature [135], [146], fuse saving concept is used by the utilities in the real field. According to this concept, the fuse must not operate for all temporary faults in the DN. In this situation, the recloser has to operate before fuse and hence, giving a chance to clear the transient faults. This is possible by making recloser fast TCC below the fuse Minimum Melting (MM) characteristic. It is well known that the recloser has two characteristics viz (a) Fast TCC and (b) Slow TCC which is given by equation (6.1). Both these characteristics are obtained by different values of *TDS*.

$$t_{op\_rec} = \left[\frac{A}{\left(I_{fault} / I_{pickup} \right)^{p} - 1} + B \right] \times TDS \tag{6.1}$$

Where, A, B, and p are constants for inverse time-current characteristic and can be obtained from [199]. The value of *TDS* is decided based on the coordination among recloser and lateral fuse. Moreover, I_{fault} and I_{pickup} is the fault and relay pickup current, respectively.

In the proposed work, the fuse model is developed according to equation (6.2) which gives the inverse characteristic of a fuse.

$$\log(t_{op\_fuse}) = a \times \log(I_{fuse}) + b \tag{6.2}$$

Where, t_{op_fuse} is the time of operation of the fuse; I_{fuse} is the current flowing through the fuse and, a and b are the fuse constants. In equation (6.2), the value of constant parameter "a" is obtained by calculating the slope of I^2t straight line on a log-log graph. The procedure for calculation of parameter "b" is clearly described in [151], [155], [163].

Due to integration of DGs in the DN, the coordination among recloser and fuse is disturbed because of additional fault current supplied by the DG. Therefore, in order to maintain the coordination between recloser and downstream fuse, the recloser must have an adaptive capability to change its fast-operating characteristic in the presence of DG.

6.2.2 Proposed adaptive algorithm

Fig. 6.2 shows the flowchart of the proposed adaptive algorithm. Initially, samples of currents and voltages are acquired with the help of CTs and PTs at the recloser location. These are given by equation (6.3) and (6.4).

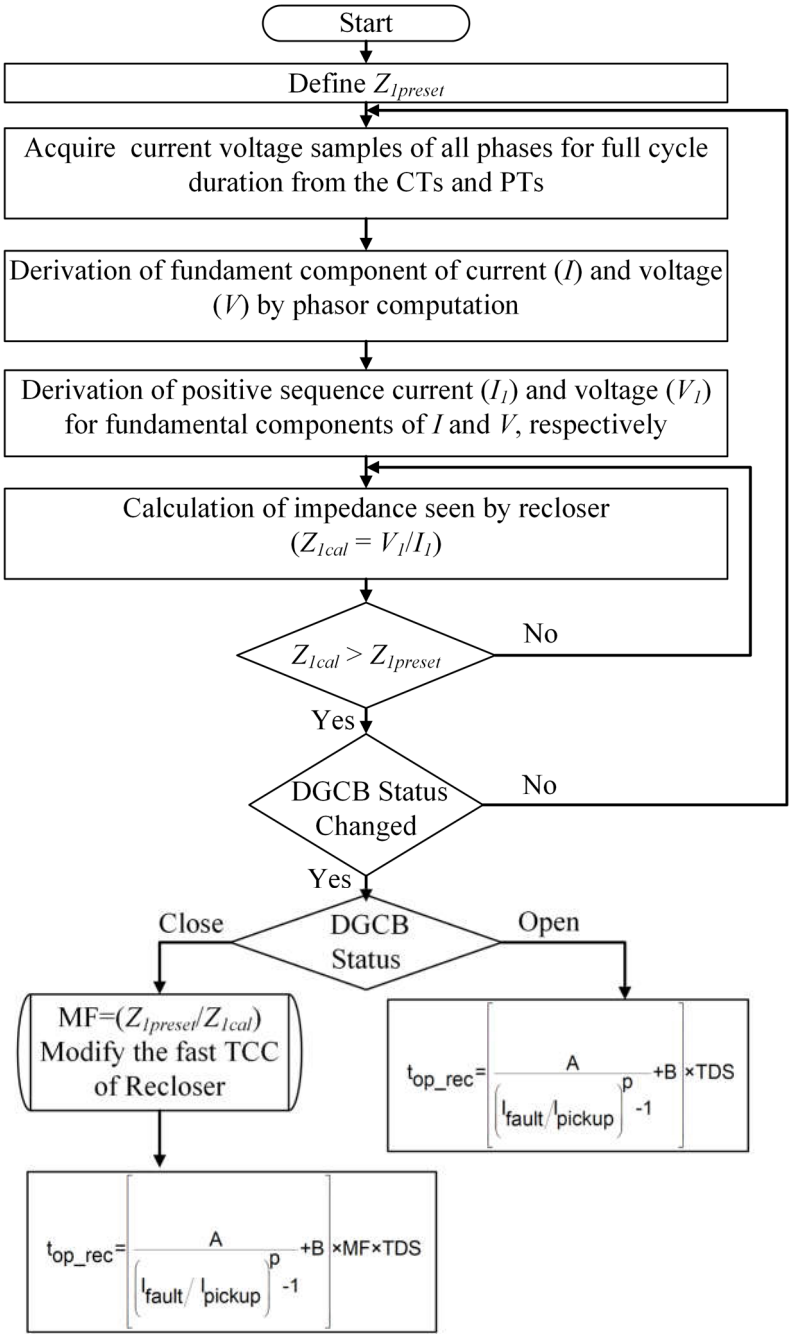


Fig. 6.2 Flow chart of the proposed relaying algorithm.

$$i_{a/b/c} = I_m \sin(wt + \phi_{ia/b/c}) \tag{6.3}$$

$$v_{a/b/c} = V_m \sin(wt + \phi_{va/b/c}) \tag{6.4}$$

Where, $i_{a/b/c}$ and $v_{a/b/c}$ are the three phase (a, b, and c) instantaneous values of currents and voltages, respectively, measured at the recloser location. Thereafter, in order to eliminate higher order harmonics, noise and dc components during normal/abnormal conditions, MDFT algorithm [170] (as discussed in Chapter 3) has been used for calculation of phasor values of

currents and voltages. The output of this algorithm is given by equation (6.5) and (6.6), respectively.

$$I_a = |I_a| \angle \phi_{Ia}, \quad I_b = |I_b| \angle \phi_{Ib}, \quad I_c = |I_c| \angle \phi_{Ic} \tag{6.5}$$

$$V_a = |V_a| \angle \phi_{Va}, \quad V_b = |V_b| \angle \phi_{Vb}, \quad V_c = |V_c| \angle \phi_{Vc} \tag{6.6}$$

Where, $|I_{a/b/c}|$ and $|V_{a/b/c}|$ are the magnitude of current and voltage fundamental phasor (for phase *a*, *b* and *c*), respectively, $\phi_{Ia/b/c}$ and $\phi_{Va/b/c}$ are the angle of current and voltage fundamental phasor (for phase *a*, *b* and *c*), respectively. The derived phasor values are further utilized for the calculation of the sequence components of currents and voltages as per equation (6.7) and (6.8), respectively.

$$[I_{012}] = \tfrac{1}{3} \times [A] \times [I_{abc}] \quad \text{Where, } [A] = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \tag{6.7}$$

$$[V_{012}] = \tfrac{1}{3} \times [A] \times [V_{abc}] \tag{6.8}$$

Where, $[I_{012}]$ and $[V_{012}]$ are the zero, positive and negative sequence components of current and voltage, respectively. The value of I_1 and V_1 is used for calculation of Z_{1cal} as per equation (6.9).

$$Z_{1cal} = \frac{V_1}{I_1} \tag{6.9}$$

Afterwards, the value of Z_{1cal} is compared with $Z_{1preset}$; if the value of Z_{1cal} is higher than $Z_{1preset}$, it is necessary to check the status of the DG Circuit Breaker. However, the value of Z_{1cal} is increased due to the incorporation of the impedance of DG (Z_{DG}). When the DG (s) is connected to the DN (DGCB status is "Close"), it is necessary to modify the recloser fast TCC. This is achieved by calculating the value of modification factor as per equation (6.10) which ultimately changes *TDS* and hence, the modified recloser fast TCC is given by equation (6.11). Conversely, when the status of DGCB is "Open," then the recloser fast TCC need not be modified.

$$\mathrm{MF} = \frac{Z_{1preset}}{Z_{1cal}} \tag{6.10}$$

$$t_{op\_rec} = \left[\frac{A}{\left(I_F / I_{pickup} \right)^p - 1} + B \right] \times \mathrm{MF} \times TDS \tag{6.11}$$

6.2.3 Selection of $Z_{1preset}$

The value of $Z_{1preset}$ is decided based on positive sequence impedance seen by the recloser during the maximum loading condition with no DG integration in the DN. Here, at the recloser location, the value of voltage remains almost constant whereas, the phase current depends on the load impedance (Z_{Load}), network impedance ($Z_{Network}$) and the impedance of DG (Z_{DG}). Furthermore, as the parameters of feeder/lateral remain more or less constant, the value of $Z_{Network}$ also remains almost constant. Conversely, the value of Z_{Load} depends on the load present in the DN. Therefore, the phase current flowing through the recloser without and with DG in the DN is given by (6.12) and (6.13), respectively.

$$I = \frac{V}{\left(Z_{Network} + Z_{Load} \right)} \text{ When DGCB is open} \tag{6.12}$$

$$I = \frac{V}{\left(Z_{Network} + Z_{Load} + Z_{DG} \right)} \text{ When DGCB is close} \tag{6.13}$$

where, V and I are the values of voltage and current, respectively at recloser location. As per equation (6.12), during maximum loading condition of the DN, the current flowing through the recloser is maximum. Hence, as per equation (6.9), the value of Z_{1cal} is minimum, which is the $Z_{1preset}$ of the DN. Conversely, as observed from equation (6.13), the current flowing from the recloser will be reduced depending on the incorporation of number of DGs in the DN.

6.3 Performance of evaluation of the proposed scheme on the standard network

6.3.1 Simulation model

In order to verify the performance of the proposed scheme, standard IEEE 34 bus network has been utilized [183]. This network has been developed in the RTDS/RSCAD environment. Moreover, various network components such as feeders, loads, laterals and voltage regulators have been redesigned and modelled exclusively for 50 Hz frequency. Fig. 6.3 shows the single line diagram of the developed IEEE 34 bus network. As shown in Fig. 6.3, the recloser is located near bus 800. The synchronous generator based DG1 (0.5 MVA),

DG2 (1.0 MVA), DG3 (1.5 MVA) and DG4 (0.3 MVA) are connected at buses 854, 840, 890 and 860, respectively. The parameters of DGs are given in Appendix. In this model, various laterals (single-phase/two-phase/three-phase) are emanated from different buses of the network. As the tailor-made models of recloser and fuse are not available in the RTDS/RSCAD, they have been designed using equation (6.1) and (6.2), respectively. The recloser model is developed in such a way that it is capable to perform single shot reclosing and then remains in lockout condition with a dead time of 300 *ms*. Further, extremely inverse characteristic has been used for fast and slow operation of recloser and the corresponding values of *A*, *B* and *p* are selected from [199]. Moreover, the operating range of recloser is considered as 80 A to 10,000 A. Subsequently, the fuse characteristics have been designed as per the procedure described in section 5.2.1 and the corresponding values of fuse constants "*a*" and "*b*" are considered as -2.58 and 6.81, respectively. In addition, the minimum Coordination Time Interval (CTI) of the order of 0.2 s between recloser fast TCC and fuse MM characteristic has been maintained.

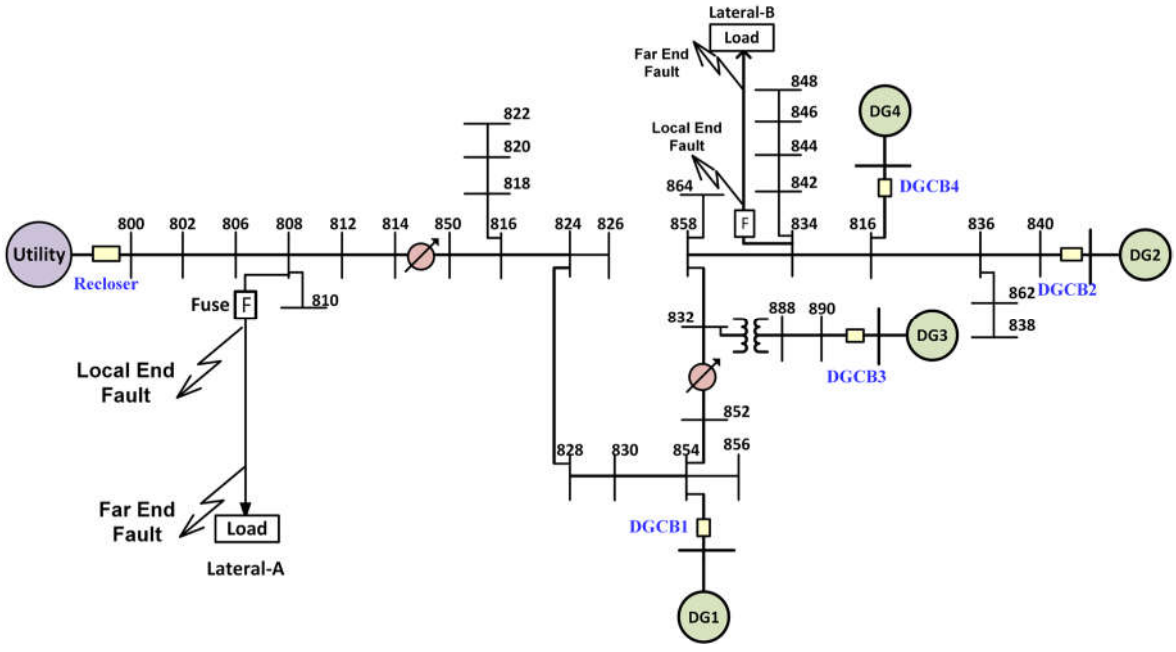


Fig. 6.3 Single line diagram of standard IEEE 34 bus network developed in RTDS/RSCAD environment.

6.3.2 Selection of Z1preset for IEEE 34 bus network

In the proposed work, the value of $Z_{1preset}$ has been selected as the procedure described in Section 5.2.3. Here, samples of the currents and voltages are acquired at recloser location

(bus 800) in the presence/absence of the DG/DGs. These values are utilized for calculation of Z_{1cal} (as per equation (6.9)). In the proposed work, various DGs located at different locations having varying capacity have been integrated. Table 6.1 shows the simulation results in terms of Z_{1cal} obtained (i) when no DG/single is connected and (ii) when multiple DGs with varying capacity/location are connected in the DN. It is to be noted from Table 6.1 that as the capacity of DG and its penetration increases, the value of Z_{1cal} also increases. Furthermore, the minimum value of Z_{1cal} is 312.35 Ω. This is achieved when no DG is connected to the IEEE 34 bus network. Hence, the value of $Z_{1preset}$ is chosen as 312 Ω for IEEE 34 bus network.

Table 6.1 Value of Z_{1cal} without/with DG in IEEE 34 bus network.

Incorporation of single DG	Z_{1cal} (Ω)	Incorporation of multiple DGs	Z_{1cal} (Ω)
No DG	312.35	--	--
DG4	371.62	--	--
DG1	426.32	DG4+DG1	493.23
DG2	475.82	DG4+DG1+DG2	781.43
DG3	538.64	DG4+DG1+DG2+DG3	1792.38

6.3.3 Coordination margin between recloser and fuse

Traditionally, coordination between recloser and fuse is carried out based on unidirectional power flow (with no DG connected in the DN). The said coordination is maintained within the specified minimum and maximum value of fault current, which is widely known as coordination margin. Usually, in the distribution network, high impedance fault takes place when high impedance entity gets in touch with the conductor or when the phase conductor broke down and fall on the ground [200]. At this time, the minimum value of fault current depends on the value of fault impedance. In [201], the minimum value of fault current on IEEE 34 node network has been calculated based on 20 Ω fault impedance. Moreover, according to survey made in [202], it has been found that the most of electric utilities are utilizing 40 Ω fault impedance for the calculation of minimum fault current. Therefore, in the proposed scheme, 40 Ω fault impedance has been used for all simulations. Here, to obtain the minimum and maximum fault current, two types of faults namely LG and triple line (LLL) with varying fault resistance (0.01 Ω and 40 Ω) have been simulated at two different locations (local end and far end) on the lateral. All the aforementioned faults have been performed on the Lateral-A connected at bus 808 (refer Fig. 6.3) with and without considering the integration of DG. Table 6.2 and Table 6.3 show the simulation results in terms of RMS value of recloser ($I_{recloser}$) and fuse (I_{fuse}) current during various fault conditions.

Table 6.2 Recloser and fuse current without/with single DG incorporation in IEEE 34 bus network for fault on Lateral - A.

Fault location	Type of Fault	(R_f) (Ω)	No DG		Incorporation of single DG at a time							
					DG4		DG1		DG2		DG3	
			$I_{recloser}$ (A)	I_{fuse} (A)	$I_{recloser}$ (A)	I_{fuse} (A)	$I_{recloser}$ (A)	I_{fuse} (A)	$I_{recloser}$ (A)	I_{fuse} (A)	$I_{recloser}$ (A)	I_{fuse} (A)
Local end	LG	40	227	186	219	189	214	221	200	206	203	190
	LLL	0.01	551	530	540	555	553	585	547	581	540	572
Far end	LG	40	200	172	184	176	175	203	175	190	178	182
	LLL	0.01	394	379	382	387	386	401	388	406	376	408

Table 6.3 Recloser and fuse current with multiple DGs incorporation in IEEE 34 bus network for fault on Lateral - A.

Fault location	Fault type	R_f (Ω)	With DG4+DG1 incorporation		With DG4+DG1+DG2 incorporation		With DG4+DG1+ DG2+DG3 incorporation	
			$I_{recloser}$ (A)	I_{fuse} (A)	$I_{recloser}$ (A)	I_{fuse} (A)	$I_{recloser}$ (A)	I_{fuse} (A)
Local end	LG	40	205	222	191	223	182	218
	LLL	0.01	554	598	553	619	573	625
Far end	LG	40	175	200	160	203	155	208
	LLL	0.01	378	407	381	426	386	430

It is to be noted from Table 6.2 that the minimum and maximum value of fault current flowing through the fuse is 172 A, and 530 A, respectively; when no DG is connected. Hence, the initial coordination range between recloser and fuse without DG is 358 A (530 A – 172 A). Similarly, as observed from Table 6.3, the minimum and maximum value of fault current flowing through the fuse is 176 A (for DG4), and 585 A (for DG1), respectively; when a single DG with varying capacity is connected to the DN. On the other hand, it could be noted from Table 6.3 that the minimum and maximum value of fault current flowing through the fuse is 200 A (for DG4+DG1) and 625 A (all four DGs), respectively, when multiple DGs are connected to the network. Furthermore, it has been observed from Table 6.2 and Table 6.3 that with the integration of DG in the DN, the existing coordination between recloser and lateral fuse is lost. Therefore, in order to restore the coordination between recloser and fuse in the presence of DG, it is necessary to modify the coordination margin adaptively such that recloser operates before the fuse. In the proposed scheme, this is achieved by adaptively modifying the recloser fast TCC (as per (6.11)). Table 6.4 shows the simulation results in terms of MF and old/modified TDS of recloser fast TCC. The existing and modified coordination margin due to incorporation of single DG(s) and multiple DGs are shown in Fig. 6.4 and Fig. 6.5, respectively.

Table 6.4 Modification of TDS of recloser fast TCC during integration of single/multiple DG.

Status of DGCB	Interconnection of single/multiple DG	MF	Old TDS (Sec)	Modified TDS (Sec)
Open	NO DG	1.00	0.55	0.55
Close	DG4	0.84	0.55	0.46
Close	DG4+DG1	0.63	0.55	0.35
Close	DG4+DG1+DG2	0.40	0.55	0.22
Close	DG4+DG1+DG2+DG3	0.20	0.55	0.15

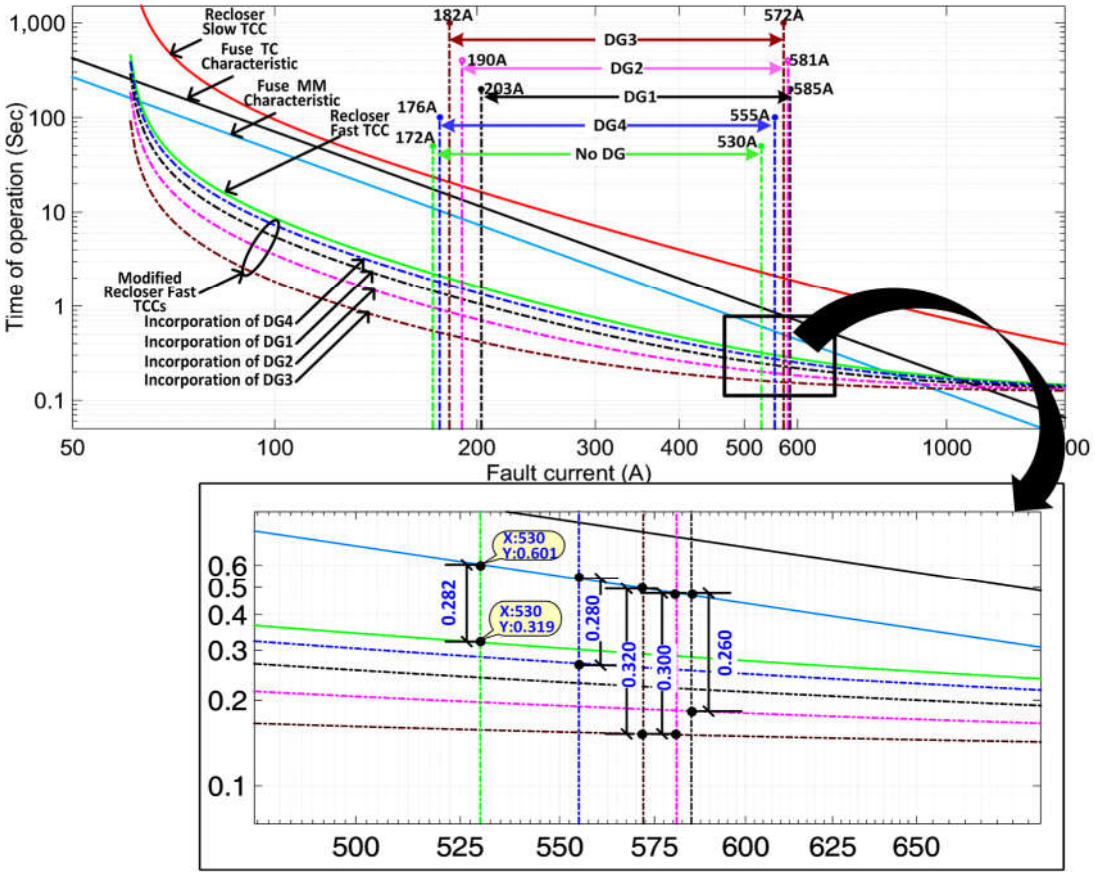


Fig. 6.4 Performance of proposed adaptive scheme for IEEE 34 bus network in terms of coordination margin between recloser and fuse with (single DG incorporation) and without DGs.

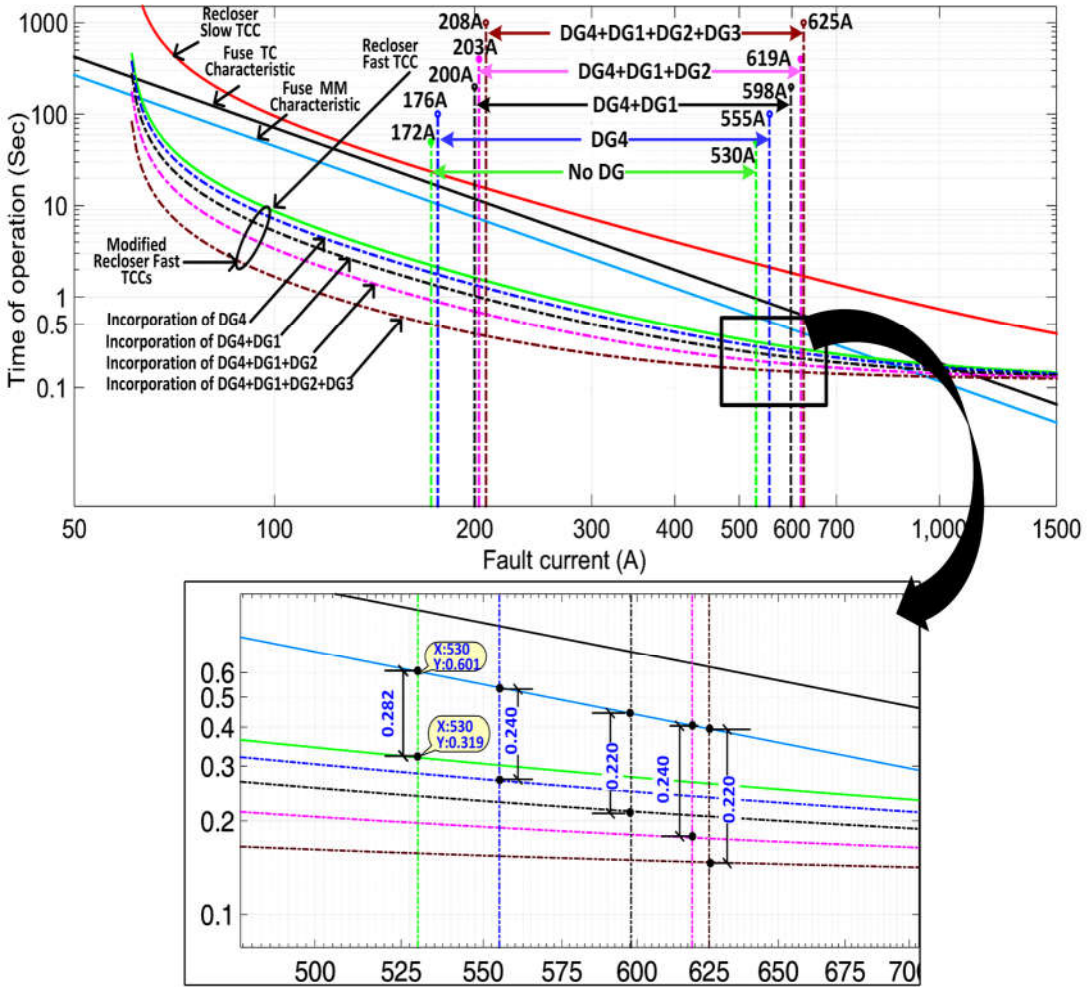


Fig. 6.5 Performance of proposed adaptive scheme for IEEE 34 bus network in terms of coordination margin between recloser and fuse with (multiple DGs incorporation) and without DGs.

As observed from in Fig. 6.4 and Fig. 6.5, due to integration of single/multiple DGs in the DN, the coordination between recloser and fuse is lost. At the same time, the corresponding CTI is not maintained. However, the required coordination is restored by adaptively changing the recloser fast TCC based on MF. As depicted in Table 6.4, with the integration of DG/DGs in the DN, the value of MF changes which in turn reduces the TDS of recloser fast TCC. Hence, the recloser fast TCC moves down depending upon the penetration of the DG, which leads to earlier operation of recloser than fuse. Moreover, it has been further observed from both the figures that the minimum CTI between recloser fast TCC and fuse MM characteristic is maintained of the order of 0.2 s.

6.3.4 Validation of the proposed scheme on another lateral

In order to validate the performance of the proposed scheme during fault on a different lateral, similar type of fault conditions, as carried out for Lateral-A, have been simulated on

the Lateral-B (connected at bus 834). The simulation results obtained in terms of RMS value of recloser and fuse currents are depicted in Table 6.5. It is to be noted from Table 6.5 that the minimum and maximum value of fault current flowing through the fuse is 81 A and 198 A, respectively, when no DG is connected to the DN. On the other hand, with the integration of multiple DGs, the minimum and maximum value of fault current flowing through the fuse is 112 A (for DG4+DG1) and 323 A (for all DGs), respectively. For the above two cases, it has been observed from Fig. 6.5 that the modified recloser fast TCCs, generated by proposed scheme, are capable to provide proper coordination between recloser and fuse within the fault current range of 81 A to 323 A.

Table 6.5 Recloser and fuse current with multiple DGs incorporation in IEEE 34 bus network for fault on Lateral-B.

Fault location	Fault type	R_f (Ω)	With DG4+DG1 incorporation		With DG4+DG1+DG2 incorporation		With DG4+DG1+ DG2+DG3 incorporation	
			$I_{recloser}$ (A)	I_{fuse} (A)	$I_{recloser}$ (A)	I_{fuse} (A)	$I_{recloser}$ (A)	I_{fuse} (A)
Local end	LG	40	108	88	112	117	114	146
	LLL	0.01	232	198	238	289	242	318
Far end	LG	40	96	81	91	112	94	131
	LLL	0.01	148	105	159	206	162	230

6.4 Experimental evaluation of the presented scheme in the laboratory environment

In order to evaluate the performance of the presented algorithm, a prototype has been developed in the laboratory environment.

6.4.1 Laboratory prototype

Fig. 6.6 shows circuit diagram of the developed laboratory prototype. As shown in Fig. 6.6, various electrical circuit components such as autotransformer (10 kVA, 415 V, 50 Hz, 3-phase), contactors (Cs), rheostats, variable choke coils, CTs, PTs, toggle switches (S1, S2, S3, and S4), variable R-L load and fuses (15 A) have been utilized for the development of the said laboratory prototype. In the developed prototype, the contactor acts as a circuit breaker whereas CTs and PTs are used for collection of samples of current and voltage signals. Further, rheostats and variable choke coils are used to design a distribution feeder and a lateral whereas toggle switches have been used to create various faults. Moreover, a variable resistance (R_h) is used to limit the magnitude of fault current. Furthermore, in order to study the impact of DG on the recloser–fuse coordination, a synchronous based DG (3 kVA, 415 V, 50 Hz, 0.8 power

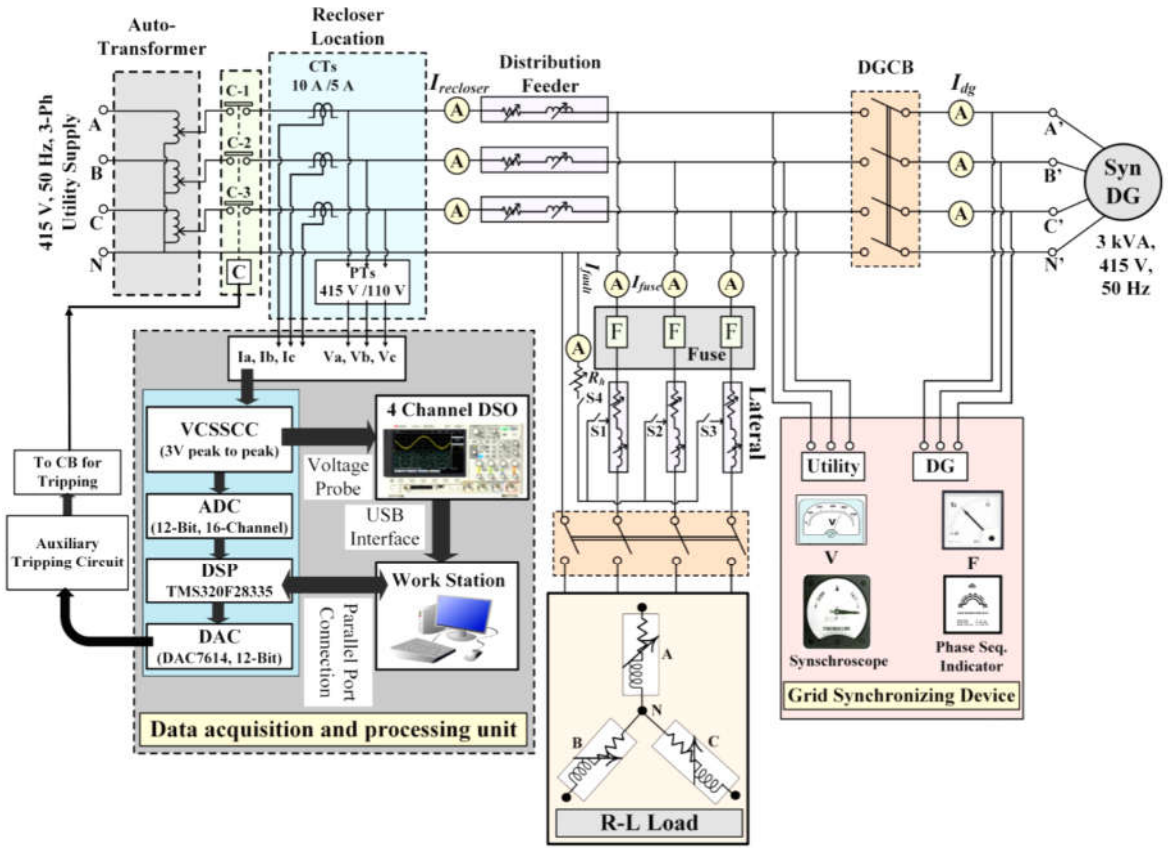


Fig. 6.6 Hardware setup of the developed laboratory prototype

factor, star grounded) has been utilized. This DG is interconnected with the utility supply (415 V, 3-phase, 50 Hz) through distribution feeder and a contactor (DGCB) by performing synchronization process with the help of grid synchronizing device.

6.4.2 Acquisition and processing of current and voltage samples

As observed from Fig. 6.6, the proposed scheme acquires samples of current and voltage at a sampling frequency of 4 kHz for a fundamental frequency of 50 Hz through Voltage and Current Sensor Signal Conditioning Circuit (VCSSCC). The VCSSCC unit scales down the voltage and current signal to low voltage level. It is developed in such a way that it gives a maximum 3 V peak-to-peak for 30 A and 500 V of current and voltage, respectively. The low voltage signal from VCSSCC is further applied to a 12-bit ADC of the DSP processor (TMS320F28335). An interface between MATLAB program (installed in a workstation) and the processor is achieved with the help of XDS510PP emulator pod. The developed algorithm has been written in MATLAB which is compiled and executed with the help of CCS v5.1 [190] on DSP board. On the execution of the programmed code for fault situations, open/trip signal is generated by the proposed algorithm, which is applied to an inbuilt DAC (DAC7614U). At

the end, an auxiliary circuit is used to initiate the opening of the contactor 'C' with its contacts C-1, C-2 and C-3.

6.4.3 Selection of $Z_{1preset}$ for the developed laboratory prototype

In order to select the value of $Z_{1preset}$ for the developed laboratory prototype, the samples of currents and voltages have been acquired at the recloser location during various loading conditions. The variation in load at constant terminal voltage has been made with respect to the full load capacity of the autotransformer in presence and absence of the DG. The acquired samples of voltage and current are processed by the proposed algorithm and the value of Z_{1cal} is calculated for different loading conditions. These are shown in Table 6.6. It is to be noted from Table 6.6 that the value of Z_{1cal} is minimum during 100% loading condition with no DG connected to the network. Hence, the value of $Z_{1preset}$ is selected as 19.00 Ω.

Table 6.6 Value of Z_{1cal} during various percentage loading conditions without/with DG

Loading condition (%)	Z_{1cal} Without DG (Ω)	Z_{1cal} With DG (Ω)
100	19.37	26.31
75	27.13	32.46
50	36.48	40.23
25	62.41	83.64

6.4.4 Recloser – fuse coordination margin of the developed laboratory prototype

As the prototype is developed with the phase voltage level of 230 V, the minimum fault current is obtained for a fault impedance of 10 Ω. Here, it is not feasible to consider higher value of fault impedance (say 40 Ω) as otherwise the magnitude of fault current becomes lower than the full load current of the feeder. At the same time, in order to achieve maximum value of fault current, LLL fault needs to be performed on the laboratory prototype. This is practically not feasible due to restricted short time current capability of the laboratory equipment. Therefore, the above hardware model has been simulated in RTDS/RSCAD platform to obtain the maximum value of fault current. Table 6.7 shows results acquired from the laboratory prototype (for LG faults) and RTDS/RSCAD simulation (for LLL faults) in term of $I_{recloser}$ and I_{fuse}. It has been observed from Table 6.7 that the recloser and fuse current are almost equal during no DG interconnection. Further, the minimum and maximum fault current flowing through the fuse is 27.86 A and 88.32 A, respectively. Conversely, when DG is connected to the network, the minimum and maximum fault current flowing through the fuse is 30.76 A and 116.46 A, respectively. Henceforth, the coordination margin between recloser and fuse without

and with DG is 27.86 A to 88.32 A and 30.76 A to 116.46 A, respectively. These two margins are shown in Fig. 6.7.

Table 6.7 RMS value of recloser and fusecurrent without/with DG incorporation in laboratory prototype.

Fault Location	Fault Type	Rf (Ω)	Without DG		With DG		Results captured
			$I_{recloser}$ (A)	I_{fuse} (A)	$I_{recloser}$ (A)	I_{fuse} (A)	
Local end	LG	10	30.64	30.62	25.72	33.14	Hardware
	LLL	0.01	96.85	88.32	105.68	116.46	Simulation
Far end	LG	10	28.12	27.86	22.58	30.76	Hardware
	LLL	0.01	88.62	82.42	98.84	108.63	Simulation

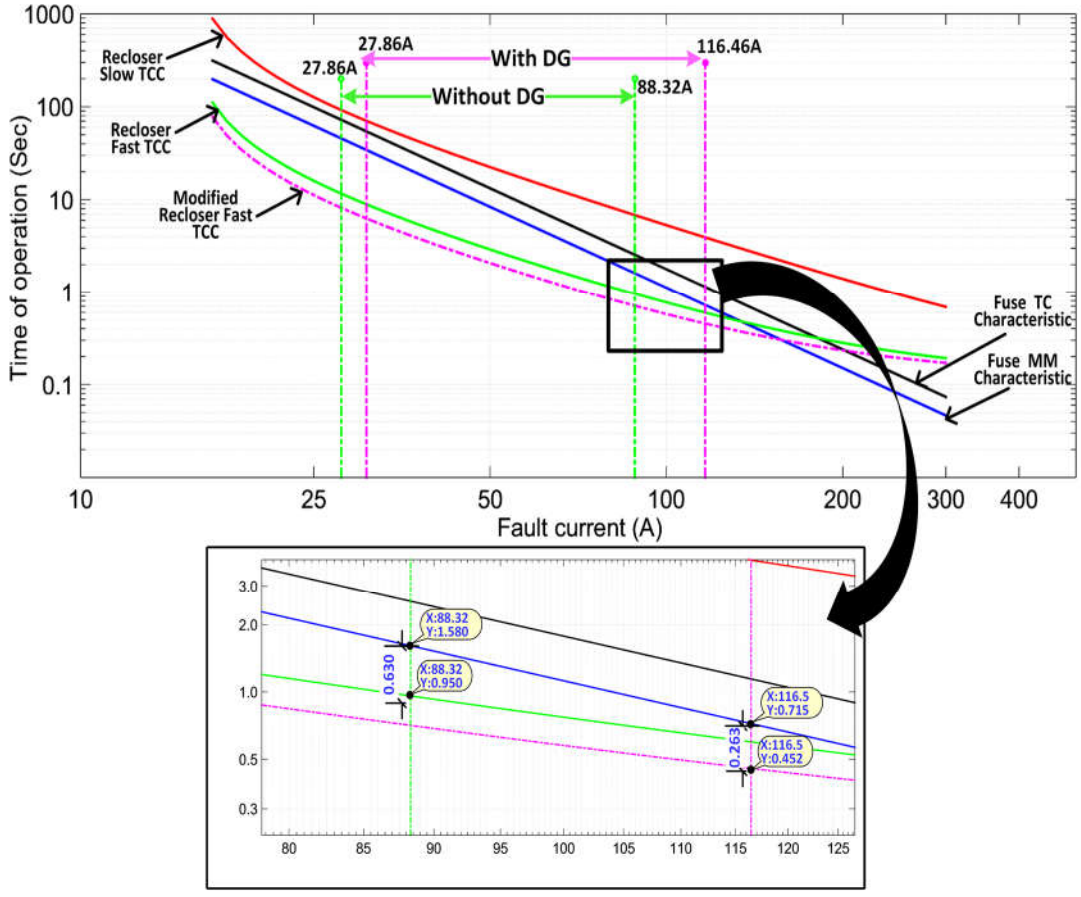


Fig. 6.7 The recloser–fuse coordination TCCs for the developed laboratory prototype

Moreover, in this work, fuse characteristic has been designed by taking fuse constants "*a*" and "*b*" as -2.9 and 5.85, respectively, whereas the pickup current of recloser TCCs are set as 120% of the full load capacity of the autotransformer. It has been observed from Fig. 6.7 that the

coordination between recloser and fuse is lost due to incorporation of DG. In order to maintain the said coordination, the proposed scheme changes the value of MF (0.72) as per equation (6.10) which in turn lowers recloser fast TCC according to equation (6.11). The modified fast TCC of the recloser is also shown in Fig. 6.7. It has been observed from Fig. 6.7 that the recloser now operates prior to the fuse in the presence of DG. Moreover, it has been further observed from Fig. 6.7 that the CTI between recloser fast TCC and fuse MM characteristic without and with DG interconnection is maintained as 0.63 s and 0.263 s, respectively.

6.5 Comparative evaluation

Comparative evaluation of the proposed scheme has been carried out with two existing schemes presented [151] and [163] which is as given below.

Effect of noise, harmonics and decaying DC: In both the schemes presented in [151] and [163], the presence of noise, harmonics and decaying DC in the acquired instantaneous current and voltage signals significantly affects modification index of the recloser fast TCC. This results in improper coordination between recloser and fuse. Whereas, the proposed scheme remains immune against noise, harmonics and decaying DC present in the acquired current signal due to utilization of MDFT phasor computation algorithm. Hence, the coordination between recloser and fuse remains unaffected.

Operating time: Both techniques take higher time to modify the recloser fast TCC due to utilization of post-fault samples of current and voltage signals. Conversely, the proposed scheme consumes low operating time as recloser fast TCC is updated at the time of interconnection of DG and not during fault condition.

Cost: The technique proposed in [151] is economically not viable as it requires communication of all fuse currents to the recloser which increases overall cost. On the other hand, as the proposed scheme requires communication between recloser and DG only, the overall cost is comparatively lower than the scheme reported in [151].

Effect of fault resistance: The technique proposed in [163] has not considered the effect of high fault impedance on the selection of '*k*'. Hence, the coordination between recloser and fuse is not maintained due to significant reduction in the value of '*k'*. On the contrary, the proposed technique is capable to maintain recloser-fuse coordination even during high impedance fault on the network.

Effect of low DG penetration: The technique presented in [163] may not be able to maintain sufficient CTI between recloser fast TCC and fuse MM characteristic during low penetration of DGs. On the other hand, the proposed technique works well during vast variation in the level of penetration of DGs.

Practical/field validation: Both techniques have not been validated on the laboratory prototype/field data. Whereas, the proposed technique is validated by developing a laboratory prototype.

6.6 Summary

In this chapter, a new recloser-fuse coordination technique based on a modification factor of recloser fast time-current characteristic is presented. The modification factor is the ratio of Z_{1cal} (which is calculated by acquiring samples of currents and voltages at the location of recloser) to $Z_{1preset}$. It has been observed that the value of Z_{1cal} changes due to incorporation of DG in the DN which in turn changes the value of MF. The appropriateness of the proposed scheme has been verified by modeling IEEE 34 bus network in RTDS/RSCAD environment. Subsequently, the performance of the presented scheme has also been tested on the developed laboratory prototype. The results obtained from simulations as well as from the laboratory prototype indicate that the proposed scheme upholds appropriate coordination between recloser and fuse even in case of high as well as low penetration of DG in the DN. However, the research work based on this technique is under the review of experts. Hence, it could be said that there may be a chance for improvement in the presented technique.

Chapter 7
Conclusions and Future Scope

7.1 Conclusions

In order to cater an ever increasing energy demand, researchers are finding one or another way of providing reliable electrical energy to the consumer. The DG technology is one of them. At the same time, economically viable DG technology has changed the global scenario of power generation and utilization. In the past, most of the difficulties arose during the transmission of the bulk power over a long distance due to transmission losses and huge infrastructure requirement. Whereas, in today's scenario, the power is generated right at the demand site which has reduced the requirement of transmission infrastructures. This technology provides better reliability of power and, at the same time, it is environment friendly. Nowadays, in DG technology, renewable energy sources such as Solar and Wind have been given significant importance. Though DG provides many advantages over the conventional technology of power generation, it is affected by various technical and non-technical issues. In the technical issues, as the DG is generally interconnected with an existing utility grid network, protection of DN and consumers are the major concerned. In the interconnected mode operation of the DG, the electrical parameters of the network such as voltage and frequency remain within its operating range. However, sudden disconnection of DG from the DN, makes these parameters to deviate at a very high value as compared to its nominal value. These deviations are large enough to damage the equipment/appliances of DN/consumer. Moreover, an integration of DG into DN makes the current flow in two directions in the radial network which may cause mis-coordination of protective devices. Therefore, to provide proper protection to the DN and consumers, research is ongoing in the area of anti-islanding protection and restoration of coordination among protective devices of the DN in the presence of DG.

In case of islanding detection, there are various techniques based on different methods of signal acquisition and utilization reported in literatures. During islanding situation, there is an abrupt change in magnitude of various electrical parameters which are not only damage the DN but also affect consumer's equipment/property. Hence, this situation must be detected as quickly as possible. As per various standards, it must be detected within 2 *s* from its inception. In islanding detection, NDZ is the zone of active/reactive power imbalance between load and generation during which several techniques are unable to detect islanding situation. Subsequently, some techniques detect non-islanding event as islanding situation and issue a nuisance trip to disconnect the DG. In both the cases, an anti-islanding protection fails to fulfil

the selectivity and discrimination criteria of an accurate protection scheme. Moreover, integration of DG into DN mis-coordinates the protective devices which will either mal-operate or remains unoperated during an abnormal/fault condition.

In case of an unintentional islanding, the deviation in electrical parameters is large enough to damage the equipment at the consumer end. Hence, in order to protect consumers and DN, the islanding situation must be detected as quickly as possible. Simultaneously, in order to restore the recloser – fuse coordination, it is desirable to develop fast and accurate digital relaying scheme which is capable to disconnect the DG during islanding within minimum time and restore the proper coordination between recloser and fuse in the presence of DG in the DN. This thesis is devoted to the development of various protection schemes for islanding detection and restoration of recloser – fuse coordination in the presence of DG into DN.

Followings are the major conclusions of the research work carried out in this thesis.

1. Initially, an approach based on pattern recognition for the detection of islanding situation has been presented. In this work, a simulation model of the standard IEEE 34 node network has been developed in RTDS/RSCAD environment. This model dedicatedly designed for the 50 Hz fundamental frequency. A large number of test cases of islanding and non-islanding events have been generated on the developed model. Further, both the current and voltage signals have been acquired from the terminal of the target DG for the formation of feature vector. As the negative sequence component of currents has proved its higher efficiency in discriminating islanding with non-islanding events, it has been utilized for the formation of the feature vector. In the presented work, a relevance vector machine has been used as a classifier model. This has given the highest efficiency of more than 98% in discrimination between islanding and non-islanding events. At the same time, it requires less number of training data. Furthermore, it also accurately discriminates islanding situation in case of perfect power balance condition. In addition, it remains immune to the non-islanding events. At the end, the comparative assessment proves that the proposed scheme is superior in discriminating islanding situation with non-islanding events. Nevertheless, this is one of the patterns recognition based technique in which a large number of test cases are required to generate. However, this technique requires only 40% of the total dataset for the training of the classifier modal. In the case of simulation, it is possible to generate a large number of test cases covering all aspects of islanding and non-islanding situations. But, in real time application, it is not feasible to cover all the possibilities

of islanding and non-islanding events. Therefore, it has been decided to develop more practicable technique.

2. In the second approach, a sequence component of voltage has been utilized for the detection of islanding situation. During this work, the same IEEE 34 node network, developed in RTDS/RSCAD along with inverter and synchronous based DG, has been utilized. A large number of simulation test cases of islanding and non-islanding events have been generated in this model. The derived sequence components have been further utilized for the derivation of the islanding detection factor. An effective discrimination between islanding situation and non-islanding events have been obtained by comparing the value of the IDF with the pre-set threshold value. The results obtained in terms of IDF for various islanding and non-islanding situations indicate that the proposed scheme accurately distinguishes islanding situation with the non-islanding event. Further, it senses islanding condition quickly, even in case of a very critical islanding situation such as perfect power balance between load and generation condition. Furthermore, during a non-islanding situation, the presented scheme remained stable and has not issued a trip signal. Moreover, the comparison of the proposed scheme to the existing scheme proves its superiority in the detection of islanding situation. Nevertheless, in order to further authenticate the presented technique on hardware results, a laboratory prototype has been developed. The acquired voltage signals are further utilized to derive IDF as per the algorithm of the proposed technique. The hardware test results indicate that the proposed algorithm has accurately detected islanding situation at all mismatches of active and reactive power between load and generation. However, in case of a sudden load change (100% to 50%), the proposed technique mal-operates. Hence, it is necessary to develop accurate technique for islanding detection, which is able to detect islanding situations from the experimental test results as well as it remains stable during all non-islanding conditions.

3. In the third approach, modal components of the acquired voltage signals have been utilized in the proposed work. In this work, the value of IDF has been calculated from the obtained values of modal components which are derived from the phasor values of acquired voltage signals. Further, the authenticity of the proposed scheme has been verified by developing a prototype in the laboratory environment. In this prototype, a synchronous generator based DG has been utilized. Furthermore, on this prototype, various non-islanding events and islanding situations have been

generated. The experimental results obtained from the prototype indicate that the presented algorithm is able to detect islanding situation accurately and quickly (within 3.5 cycles). Moreover, it is capable of detecting islanding situations with lower or zero mismatch of active/reactive power between the load and generation. Subsequently, it remains stable during non-islanding events. The comparative evaluation of the proposed scheme with the existing schemes clearly indicate its superiority in distinguishing islanding situations with non-islanding events. Besides, the prototype based execution of the proposed scheme proved that this scheme is easy to implement in the actual field. However, the time taken to detect the islanding is around three and half cycles. Hence, there is a need to develop a new islanding detection technique which takes lower time.

4. In the last approach of islanding detection, a discriminating factor derived from an auto-correlation function of the voltage signals has been utilized for the detection of islanding situation. The value of DF is calculated from the most affected lags of the ACF during various islanding situations and non-islanding events. Discrimination of an islanding situation with the non-islanding events has been achieved by comparing the value DF with the pre-set threshold value. Further, the validation of the presented scheme has been carried out by developing a Hardware-In-Loop laboratory setup. In this setup, a power distribution test network has been virtually developed in RTDS/RSCAD environment. Various islanding and non-islanding test cases have been generated on the developed HIL model. The experimental results show that the presented algorithm is able to differentiate between islanding situation and non-islanding events efficiently. Moreover, the proposed scheme is capable of identifying islanding situation even in case of the perfect power balance condition. In addition, it provides better stability against various non-islanding events and hence, avoids nuisance tripping. The detection time of the proposed ACF based approach is less than three cycles. However, the research work involving the presented technique is under the review of the experts. Hence, it could be said that there may be a chance of improvement in the presented work and the detection time could be further reduced.

5. In case of restoration of coordination between recloser and fuse in the presence of DG into DN, an adaptive relaying technique based on the network impedance has been presented. This technique is based on the positive sequence impedance of a network seen by the recloser. It has been observed that the value of the impedance

of the network seen by the recloser is varied with respect to the interconnection of DGs in the network. Here, to calculate the value of Z_{1cal}, the phasor values of the acquired current and voltage samples from the recloser location have been utilized. The value of Z_{1cal} is further used for the derivation of modifying factor. In the presented scheme, the recloser changes its fast operating TCC based on the value of MF. The authenticity of the proposed technique has been evaluated by developing an IEEE 34 bus network model in RTDS/RSCAD environment. Simultaneously, its appropriateness has also been verified on a prototype developed in the laboratory. The results obtained from simulations as well as from the laboratory prototype indicate that the proposed scheme restores proper coordination between recloser and fuse even in case of a high as well as low penetration of DG in the DN. Apart from this, the prototype demonstration of the proposed scheme attests its easy development of real hardware for its utilization in the actual field. However, the research work involving the presented technique is under the review of the experts. Hence, it could be said that there may be a chance of improvement in the presented work.

7.2 Future scope

As none of the research work is complete, there is always a scope for further improvement. Hence, it is almost impossible to propose a complete protection scheme which is capable to take care of all kinds of abnormal conditions. It is, therefore, important to consider some of the situations for which the further study is required. Following are the suggested areas which can be explored to improve the protection schemes in the presence of DG into DN.

1. Nowadays, an LVRT protection technique becomes a part of DG protection. In this case, LVRT operates during islanding (it causes very low voltage around 15% of nominal value) and does not allow the DG disconnection for a certain period of time. Hence, an islanding detection in the presence of LVRT protection would be one of areas of further research.

2. In the restoration of protection coordination between recloser and fuse in the presence of DG into DN, a data/status communication between recloser and fuse plays a vital role. Failure/delay in the communication would lead to mis-coordination among these protective devices. Therefore, development of a new technique for restoration of coordination between recloser and fuse without

communication channel would be a grey area to be investigated for further research.

3. Integration of DG into DN leads to the change in the direction of current in the network. Due to this, overcurrent relays located in the DN may lose its coordination with other relays. In that case, primary and back up protection of the DN would largely affect. Hence, designing a protection coordination strategy for overcurrent relay placed in a DN in the presence of DG would be one of the areas of research.

Research Publications

1. Published/Accepted in International Journals

[1] Yogesh Makwana and Bhavesh. R. Bhalja, "Islanding detection technique based on relevance vector machine," *IET Renewable Power Generation.*, vol. 10, no. 10, pp. 1607–1615, Nov. 2016.

[2] Yogesh M. Makwana and Bavesh. R. Bhalja, "Islanding detection technique based on superimposed components of voltage," *IET Renewable Power Generation*, vol. 11, no. 11, pp. 1371–1381, Sep. 2017.

[3] Yogesh. M. Makwana and Bhavesh. R. Bhalja, "Experimental Performance of an Islanding Detection Scheme Based on Modal Components," *IEEE Transactions on Smart Grid*, 2017, Early Access, DOI: 10.1109/TSG.2017.2757599.

2. Communicated in International Journals

[1] Yogesh. M. Makwana, Bhavesh. R. Bhalja and Ramakrishna Gokaraju, "Restoration of recloser-fuse coordination for DG interfaced distribution network", *IEEE Transactions on Industrial Informatics*, 2018, under second revision, manuscript ID: TII-18-0940

[2] Yogesh. M. Makwana, Bhavesh. R. Bhalja and Ramakrishna Gokaraju "Hardware-In-Loop testing of an auto-correlation based islanding detection scheme", *IET Generation Transmission and Distribution*, 2018, under revision, manuscript ID: GTD-2018-6370.

Appendix - A.

A.1 Capacity of power generation of the DGs

Table A.1 Capacity of the DGs utilized in the development of RTDS/RSCAD simulation model

Capacity of Power Generation		Capacity (MVA)
DG 1 (Synchronous based DG)	:	1.0
DG 2 (Synchronous based DG)	:	1.5
DG 3 (Synchronous based DG)	:	0.5
DG 4 (Synchronous based DG)	:	1.5
DG 5 (Inverter based DG)	:	2.5

A.2 Simulation parameters of Synchronous based DGs

Table A.2 Various parameters of synchronous based DG used in the development of simulation model in RTDS/RSCAD platform.

Parameters		Value
Rated RMS Line-to-Neutral voltage	:	2.4 kV
Base angular frequency	:	50 Hz
Inertia Constant (H)	:	1.71MWs/KVA
Stator Resistance (Ra)	:	0.003 pu
Stator Leakage Reactance (Xa)	:	0.088 pu
D-axis unsaturated Reactance (Xd)	:	1.56 pu
D-axis unsaturated Transient Reactance (Xd')	:	0.26 pu
D-axis unsaturated Sub-transient Reactance (Xd")	:	0.15 pu
Q-axis unsaturated Reactance (Xq)	:	1.06 pu
Q-axis unsaturated Transient Reactance (Xq')	:	0.62 pu
Q-axis unsaturated Sub-transient Reactance (Xq")	:	0.15 pu
D-axis unsaturated Transient Open Time Constant (Td0')	:	3.7 sec
D-axis unsaturated Sub-transient Open Time Constant (Td0")	:	0.05 sec
Q-axis unsaturated Transient Open Time Constant (Tq0')	:	0.3 sec
Q-axis unsaturated Sub-transient Open Time Constant (Tq0")	:	0.05 sec

Mainly two models of synchronous generator are developed for the RTDS. These are lf_rtds_sharc_sld_MACV31 and rtds_vsc_SM, for both normal time−step (≃ 50 μs) and small time−step (≃ 1.4 − 2.5 μs) modules. In the presented work, lf_rtds_sharc_sld_MACV31 with normal time-step (≃ 50 μs) have been utilized. Fig. A. 1 shows the utilized model along with excitation and governing system. In RTDS all kind of standard excitation systems are given. Among all the available standard excitation system, in the presented work, IEEE Type ST1 excitation system has been utilized. Similarly, in case of governing system IEEE Type 1

Governor/Turbine has been utilized.

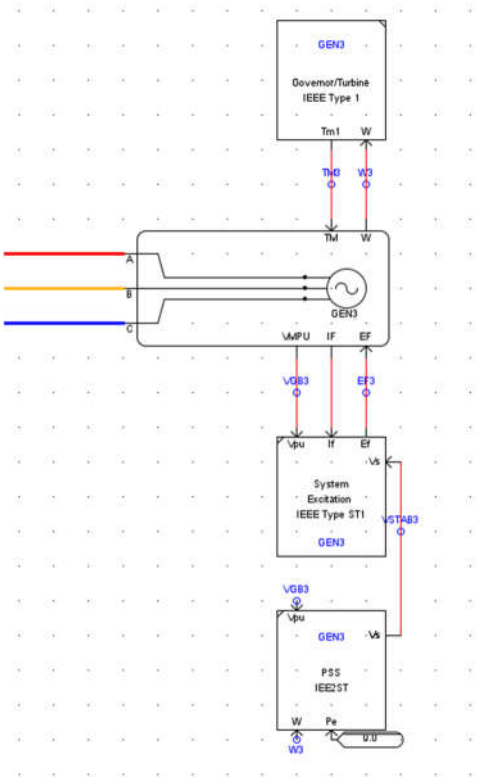


Fig. A.1 Model of the synchronous generator along with excitation and governing system used in the RTDS/RSCAD simulation.

A.3 Simulation parameters of Power Transformers

Table A.3 Various parameters of power transformer used in the development of simulation model in RTDS/RSCAD platform.

Parameters		**Value**
Capacity	:	According to DG
Transformer Primary LL RMS Voltage	:	2.4 kV
Transformer Secondary LL RMS Voltage	:	24.9 kV
Positive Seq. Resistance	:	0.0088667 pu
Positive Seq. Reactance	:	0.059371 pu
Zero Seq. Resistance	:	0.0 pu
Zero Seq. Reactance	:	0.0087 pu

A.4 Simulation parameters of exciters

Table A.4 Various parameters of Exciter used in the development of simulation model in RTDS/RSCAD platform.

Parameters		Value
Voltage Regulator Time Constant (Ta)	:	0.02 sec
Voltage Regulator Gain (Ka)	:	200
AVR lag time constant (Tb)	:	20.0 sec
AVR lead time constant (Tc)	:	1.0 sec
Excitation system regulation factor (Kc)	:	0.175
Maximum controller output (Vrmx)	:	5.7 pu
Minimum controller output (Vrmn)	:	-4.9 pu

A.5 Simulation parameters of Solar PV DG.

Table A.5 Various parameters of Solar PV DG used in the development of simulation model in RTDS/RSCAD platform.

Parameters		Value
No. of series connected Cell per string per PV Module	:	36
No. of parallel string of Cells per PV Module	:	1
No. of PV Module in series	:	115
No. of PV Module in parallel	:	285
Open circuit Voltage per PV Module	:	21.7 Volts
Short circuit Current Per PV Module	:	3.35 Amps
Reference Temperature	:	25 ºC
Reference Solar intensity	:	1000 W/m^2

Appendix - B.

B.1 Simulation modal data for synchronous generator used in HIL setup

Table B.1 Various parameters of synchronous based DG used in the development of simulation model in RTDS/RSCAD platform

Parameter		Value
Capacity	:	3 kVA
Rated RMS Line-to-Neutral voltage	:	0.415 kV
Base angular frequency	:	50 Hz
Inertia Constant (H)	:	4.00 MWs/KVA
Stator Resistance (Ra)	:	0.08 pu
Stator Leakage Reactance (Xa)	:	0.288 pu
D-axis unsaturated Reactance (Xd)	:	1.86 pu
D-axis unsaturated Transient Reactance (Xd')	:	0.36 pu
D-axis unsaturated Sub-transient Reactance (Xd")	:	0.20 pu
Q-axis unsaturated Reactance (Xq)	:	1.46 pu
Q-axis unsaturated Transient Reactance (Xq')	:	0.82 pu
Q-axis unsaturated Sub-transient Reactance (Xq")	:	0.20 pu
D-axis unsaturated Transient Open Time Constant (Td0')	:	4.5 sec
D-axis unsaturated Sub-transient Open Time Constant (Td0")	:	0.08 sec
Q-axis unsaturated Transient Open Time Constant (Tq0')	:	0.5 sec
Q-axis unsaturated Sub-transient Open Time Constant (Tq0")	:	0.08 sec

B.2 Simulation modal data for distribution feeder used in HIL setup

Table B.2 Various parameters of design of distribution feeder used in the development of simulation model in RTDS/RSCAD platform

Parameter		Value
Length of feeder	:	5 km
Resistance	:	1.05 Ω/km
Reactance	:	0.650 Ω/km

B.3 Simulation modal data for load used in HIL setup

Table B.3 Various parameters of Solar PV DG used in the development of simulation model in RTDS/RSCAD platform

Parameter		Value
Maximum current capacity	:	10 A
Rated voltage	:	415 V
Configuration	:	Star / Delta
Type	:	Resistive – Inductive

References

[1] K. Alanne and A. Saari, “Distributed energy generation and sustainable development,” *Renew. Sustain. Energy Rev.*, vol. 10, no. 6, pp. 539–558, Dec. 2006.

[2] W. El-Khattam and M. M. . Salama, “Distributed generation technologies, definitions and benefits,” *Electr. Power Syst. Res.*, vol. 71, no. 2, pp. 119–128, Oct. 2004.

[3] T. Ackermann, G. Andersson, and L. Söder, “Distributed generation: a definition,” *Electr. Power Syst. Res.*, vol. 57, no. 3, pp. 195–204, Apr. 2001.

[4] G. Pepermans, J. Driesen, D. Haeseldonckx, R. Belmans, and W. D’haeseleer, “Distributed generation: definition, benefits and issues,” *Energy Policy*, vol. 33, no. 6, pp. 787–798, Apr. 2005.

[5] M. F. Akorede, H. Hizam, and E. Pouresmaeil, “Distributed energy resources and benefits to the environment,” *Renew. Sustain. Energy Rev.*, vol. 14, no. 2, pp. 724–734, Feb. 2010.

[6] A. K. Srivastava, R. M. Shrestha, S. C. Srivastava, R. Shrestha, and D. Paul, “Power sector development in India with CO2 emission targets: Effects of regional grid integration and the role of clean technologies,” *Int. J. Energy Res.*, vol. 27, no. 7, pp. 671–685, Jun. 2003.

[7] R. C. Dugan and S. K. Price, “Issues for distributed generation in the US,” in *2002 IEEE Power Engineering Society Winter Meeting. Conference Proceedings*, 2002, vol. 1, pp. 121–126.

[8] N. K. Roy and H. R. Pota, “Current status and issues of concern for the integration of distributed generation into electricity networks,” *IEEE Syst. J.*, vol. 9, no. 3, pp. 933–944, Sep. 2015.

[9] R. Kusuma and N.-K. C. Nair, “Assessing impacts of very high penetration of distributed Photovoltaic on real MV network feeders,” in *2015 IEEE Power & Energy Society General Meeting*, 2015, vol. 2015–Septe, pp. 1–5.

[10] A. Mishra, M. Farzinfar, M. Bahadornejad, and N. C. Nair, “Evaluating the impact of different PV control strategies on distribution network operation,” in *2014 Australasian Universities Power Engineering Conference (AUPEC)*, 2014, no. October, pp. 1–6.

[11] S. Shrivastava, S. Jain, and R. K. Nema, “Distributed generation : technical aspects of interconnection,” *Int. J. Emerg. Technol.*, vol. 1, no. 1, pp. 37–40, 2010.

[12] M. S. Thomas and P. P. Terang, “Interconnection issues for distributed resources in a smart distribution system,” in *2012 IEEE 5th India International Conference on Power Electronics (IICPE)*, 2012, pp. 1–6.

[13] A. A. Memon and K. Kauhaniemi, “A critical review of AC Microgrid protection issues and available solutions,” *Electr. Power Syst. Res.*, vol. 129, pp. 23–31, Dec. 2015.

[14] B. J. Brearley and R. R. Prabu, “A review on issues and approaches for microgrid protection,” *Renew. Sustain. Energy Rev.*, vol. 67, pp. 988–997, Jan. 2017.

[15] E. Coster, J. Myrzik, and W. Kling, “Effect of DG on distribution grid protection,” in *Distributed Generation*, InTech, 2010, pp. 93–118.

[16] M. Kezunovic and B. Matic-Cuka, “Improving smart grid operation with new hierarchically coordinated protection approach,” in *8th Mediterranean Conference on Power Generation, Transmission, Distribution and Energy Conversion (MEDPOWER 2012)*, 2012, pp. 59–59.

[17] IEEE Std 1547-2003, “IEEE Standard for interconnecting distributed resources with electric Power systems,” *IEEE Standards*. pp. 1–16, Jul-2003.

[18] IEEE Std 1547-2008 (R2008), “IEEE Standard for interconnecting distributed resources with electric power systems amendment,” *IEEE Standards*. pp. 1–16, Sep-2008.

[19] IEEE Std 1547a-2014, “IEEE Standard for interconnecting distributed resources with electric power systems amendment,” *IEEE Standards*. pp. 1–16, May-2014.

[20] M. H. Bollen and F. Hassan, *Integration of distributed generation in the power system*, vol. 80. John wiley & sons, 2011.

[21] P. Kundu and A. K. Pradhan, “Supervisory protection of islanded network using synchrophasor data,” *IEEE Trans. Smart Grid*, no. Early Access, pp. 1–9, 2017.

[22] M. Tasdighi and M. Kezunovic, “Preventing transmission distance relays maloperation under unintended bulk DG tripping using SVM-based approach,” *Electr. Power Syst. Res.*, vol. 142, pp. 258–267, Jan. 2017.

[23] IEEE Std 1159-1995, “IEEE Recommended practice for monitoring electric power

quality," *IEEE Standards*. pp. 1–70, Jun-1995.

[24] P.-C. Chen, V. Malbasa, and M. Kezunovic, "Analysis of voltage stability issues with distributed generation penetration in distribution networks," in *2013 North American Power Symposium (NAPS)*, 2013, pp. 1–6.

[25] W. A. Qureshi and N.-K. C. Nair, "Wind Farm Protection," in *Large Scale Renewable Power Generation. Green Energy and Technology*, J. Hossain and A. Mahmud, Eds. Springer Singapore, 2014, pp. 311–329.

[26] N.-K. C. Nair and W. A. Qureshi, "Fault Ride-Through Criteria Development," in *Renewable Energy Integration*, J. Hossain and A. Mahmud, Eds. Springer Singapore, 2014, pp. 41–67.

[27] A.-M. Borbely and J. F. Kreider, *Distributed generation: the power paradigm for the new millennium*. CRC press, 2001.

[28] P. Mahat, Zhe Chen, and B. Bak-Jensen, "Review of islanding detection methods for distributed generation," in *2008 Third International Conference on Electric Utility Deregulation and Restructuring and Power Technologies*, 2008, pp. 2743–2748.

[29] W. Y. Teoh and C. W. Tan, "An overview of islanding detection methods in photovoltaic systems," *Int. J. Electr. Comput. Energ. Electron. Commun. Eng.*, vol. 5, no. 10, pp. 1336–1344, 2011.

[30] C. Li, C. Cao, Y. Cao, Y. Kuang, L. Zeng, and B. Fang, "A review of islanding detection methods for microgrid," *Renew. Sustain. Energy Rev.*, vol. 35, pp. 211–220, Jul. 2014.

[31] D. Velasco, C. L. Trujillo, G. Garcerá, and E. Figueres, "Review of anti-islanding techniques in distributed generators," *Renew. Sustain. Energy Rev.*, vol. 14, no. 6, pp. 1608–1614, Aug. 2010.

[32] W. El-Khattam, A. Yazdani, T. S. Sidhu, and R. Seethapathy, "Investigation of the local passive anti-islanding scheme in a distribution system embedding a PMSG-based wind farm," *IEEE Trans. Power Deliv.*, vol. 26, no. 1, pp. 42–52, Jan. 2011.

[33] X. Liu, D. M. Laverty, R. J. Best, K. Li, D. J. Morrow, and S. McLoone, "Principal component analysis of wide area phasor measurements for islanding detection - A geometric view," *IEEE Trans. Power Deliv.*, vol. 30, no. 2, pp. 976–985, Apr. 2015.

[34] M. A. Redfern, O. Usta, and G. Fielding, “Protection against loss of utility grid supply for a dispersed storage and generation unit,” *IEEE Trans. Power Deliv.*, vol. 8, no. 3, pp. 948–954, Jul. 1993.

[35] A. Etxegarai, P. Eguía, and I. Zamora, “Analysis of remote islanding detection methods for distributed resources,” in *International Conference on Renewable Energies and Power Quality (ICREPQ’11)*, 2011, pp. 1–6.

[36] W. Wang, J. Kliber, G. Zhang, W. Xu, B. Howell, and T. Palladino, “A power line signaling based scheme for anti-islanding protection of distributed generators-part II: Field test results,” *IEEE Trans. Power Deliv.*, vol. 22, no. 3, pp. 1767–1772, Jul. 2007.

[37] W. Xu, G. Zhang, C. Li, W. Wang, G. Wang, and J. Kliber, “A power line signaling based technique for anti-islanding protection of distributed generators-Part I: Scheme and Analysis,” *IEEE Trans. Power Deliv.*, vol. 22, no. 3, pp. 1758–1766, Jul. 2007.

[38] Wencong Wang, J. Kliber, and Wilsun Xu, “A scalable power line-signaling based scheme for islanding detection of distributed generators,” *IEEE Trans. Power Deliv.*, vol. 24, no. 2, pp. 903–909, Apr. 2009.

[39] W. Bower and M. Ropp, “Evaluation of islanding detection methods for photovoltaic utility- interactive power systems Task V Report IEA-PVPS T5-09,” 2002.

[40] K. Rajamani and U. . Hambarde, “Islanding and load shedding schemes for captive power plants,” *IEEE Trans. Power Deliv.*, vol. 14, no. 3, pp. 805–809, Jul. 1999.

[41] P. Banerjee and S. C. Srivastava, “An Effective Dynamic Current Phasor Estimator for Synchrophasor Measurements,” *IEEE Trans. Instrum. Meas.*, vol. 64, no. 3, pp. 625–637, Mar. 2015.

[42] K. Seethalekshmi, S. N. Singh, and S. C. Srivastava, “A Synchrophasor Assisted Frequency and Voltage Stability Based Load Shedding Scheme for Self-Healing of Power System,” *IEEE Trans. Smart Grid*, vol. 2, no. 2, pp. 221–230, Jun. 2011.

[43] A. Ishibashi, “New type of islanding detection system for distributed generation based on voltage angle difference between utility network and distributed generation site,” in *Eighth IEE International Conference on Developments in Power System Protection*, 2004, vol. 2004, no. 2, pp. 542–545.

[44] X. Ding and P. A. Crossley, “Islanding detection for distributed generation,” in *2005*

IEEE Russia Power Tech, 2005, pp. 1–4.

[45] Y. Guo, K. Li, D. M. Laverty, and Y. Xue, "Synchrophasor-based islanding detection for distributed generation systems using systematic principal component analysis approaches," *IEEE Trans. Power Deliv.*, vol. 30, no. 6, pp. 2544–2552, Dec. 2015.

[46] Z. Ye, A. Kolwalkar, Y. Zhang, P. Du, and R. Walling, "Evaluation of anti-islanding schemes based on nondetection zone concept," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1171–1176, Sep. 2004.

[47] D. Velasco de la Fuente, C. L. Trujillo Rodriguez, and E. A. Narvaez, "Review of anti-islanding methods: analysis by figures of merit tools for controllers reconfiguration in microgrids," *IEEE Lat. Am. Trans.*, vol. 13, no. 3, pp. 679–686, Mar. 2015.

[48] H. Karimi, A. Yazdani, and R. Iravani, "Negative-sequence current injection for fast islanding detection of a distributed resource unit," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 298–307, Jan. 2008.

[49] B. Bahrani, H. Karimi, and R. Iravani, "Nondetection zone assessment of an active islanding detection method and its experimental evaluation," *IEEE Trans. Power Deliv.*, vol. 26, no. 2, pp. 517–525, Apr. 2011.

[50] G. Hernandez-Gonzalez and R. Iravani, "Current injection for active islanding detection of electronically-interfaced distributed resources," *IEEE Trans. Power Deliv.*, vol. 21, no. 3, pp. 1698–1705, Jul. 2006.

[51] G. A. Smith, P. A. Onions, and D. G. Infield, "Predicting islanding operation of grid connected PV inverters," *IEE Proc. - Electr. Power Appl.*, vol. 147, no. 1, pp. 1–6, 2000.

[52] F. Liu, Y. Kang, Y. Zhang, S. Duan, and X. Lin, "Improved SMS islanding detection method for grid-connected converters," *IET Renew. Power Gener.*, vol. 4, no. 1, pp. 36–42, 2010.

[53] B. Yu, M. Matsui, Y. Jung, and G. Yu, "A combined active anti-islanding method for photovoltaic systems," *Renew. Energy*, vol. 33, no. 5, pp. 979–985, May 2008.

[54] L. A. C. Lopes and H. Sun, "Performance Assessment of Active Frequency Drifting Islanding Detection Methods," *IEEE Trans. Energy Convers.*, vol. 21, no. 1, pp. 171–180, Mar. 2006.

[55] Y. Jung, J. Choi, B. Yu, J. So, G. Yu, and J. Choi, “A novel active frequency drift method of islanding prevention for the grid-connected photovoltaic inverter,” in *IEEE 36th Conference on Power Electronics Specialists*, 2005, pp. 1915–1921.

[56] F. Liu, Y. Kang, and S. Duan, “Analysis and optimization of active frequency drift islanding detection method,” in *APEC 07 - Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition*, 2007, pp. 1379–1384.

[57] M. E. Ropp, “Design issues for grid-connected photovoltaic systems,” Georgia Tech. Univ., Atlanta, GA, 1998.

[58] M. E. Ropp, M. Begovic, and A. Rohatgi, “Prevention of islanding in grid-connected photovoltaic systems,” *Prog. Photovoltaics Res. Appl.*, vol. 7, no. 1, pp. 39–59, Jan. 1999.

[59] H. H. Zeineldin and S. Kennedy, “Sandia frequency-shift parameter selection to eliminate nondetection zones,” *IEEE Trans. Power Deliv.*, vol. 24, no. 1, pp. 486–487, 2009.

[60] H. H. Zeineldin and S. Conti, “Sandia frequency shift parameter selection for multi-inverter systems to eliminate non-detection zone,” *IET Renew. Power Gener.*, vol. 5, no. 2, pp. 175–183, 2011.

[61] M. V. G. Reis, T. A. S. Barros, A. B. Moreira, P. S. Nascimento F., E. Ruppert F., and M. G. Villalva, “Analysis of the Sandia Frequency Shift (SFS) islanding detection method with a single-phase photovoltaic distributed generation system,” in *2015 IEEE PES Innovative Smart Grid Technologies Latin America (ISGT LATAM)*, 2015, pp. 125–129.

[62] V. John, Z. Ye, and A. Kolwalkar, “Investigation of anti-islanding protection of power converter based distributed generators using frequency domain analysis,” *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1177–1183, Sep. 2004.

[63] J. Stevens, R. Nonn, J. Ginn, S. Gonzalez, and G. Kern, “Development and testing of an approach to anti-islanding in utility-interconnected photovoltaic syhstems,” 2000.

[64] H.-L. Jou, W.-J. Chiang, and J.-C. Wu, “A simplified control method for the grid-connected inverter with the function of islanding detection,” *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2775–2783, Nov. 2008.

[65] M. El-Moubarak, M. Hassan, and A. Faza, “Performance of three islanding detection methods for grid-tied multi-inverters,” in *2015 IEEE 15th International Conference on Environment and Electrical Engineering (EEEIC)*, 2015, pp. 1999–2004.

[66] A. Samui and S. R. Samantaray, “New active islanding detection scheme for constant power and constant current controlled inverter-based distributed generation,” *IET Gener. Transm. Distrib.*, vol. 7, no. 7, pp. 779–789, Jul. 2013.

[67] A. Samui and S. R. Samantaray, “An active islanding detection scheme for inverter-based DG with frequency dependent ZIP–Exponential static load model,” *Int. J. Electr. Power Energy Syst.*, vol. 78, pp. 41–50, Jun. 2016.

[68] Guo-Kiang Hung, Chih-Chang Chang, and Chern-Lin Chen, “Automatic phase-shift method for islanding detection of grid-connected photovoltaic inverters,” *IEEE Trans. Energy Convers.*, vol. 18, no. 1, pp. 169–173, Mar. 2003.

[69] J. Yin, Liuchen Chang, and C. Diduch, “A new adaptive logic phase-shift algorithm for anti-islanding protections in inverter-based DG systems,” in *IEEE 36th Conference on Power Electronics Specialists, 2005.*, 2005, pp. 2482–2486.

[70] P. D. Hopewell, N. Jenkins, and A. D. Cross, “Loss-of-mains detection for small generators,” *IEE Proc. - Electr. Power Appl.*, vol. 143, no. 3, pp. 225–230, 1996.

[71] P. O’Kane, “Loss of mains detection for embedded generation by system impedance monitoring,” in *6th International Conference on Developments in Power Systems Protection*, 1997, pp. 95–98.

[72] P. J. O’Kane, B. Fox, and D. J. Morrow, “Impact of embedded generation on emergency reserve,” *IEE Proc. - Gener. Transm. Distrib.*, vol. 146, no. 2, pp. 159–163, 1999.

[73] M. Ropp, J. Ginn, J. Stevens, W. Bower, and S. Gonzalez, “Simulation and experimental study of the impedance detection anti-islanding method in the single-inverter case,” in *2006 IEEE 4th World Conference on Photovoltaic Energy Conference*, 2006, vol. 2, pp. 2379–2382.

[74] K. Jia, H. Wei, T. Bi, D. W. P. Thomas, and M. Sumner, “An islanding detection method for multi-DG systems based on high frequency impedance estimation,” *IEEE Trans. Sustain. Energy*, vol. 8, no. 1, pp. 74–83, Jan. 2017.

[75] M. Sumner, B. Palethorpe, D. W. P. Thomas, P. Zanchetta, and M. C. Di Piazza, “A

technique for power supply harmonic impedance estimation using a controlled voltage disturbance," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 207–215, Mar. 2002.

[76] L. Asiminoaei, R. Teodorescu, F. Blaabjerg, and U. Borup, "A digital controlled PV-inverter with grid impedance estimation for ENS detection," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1480–1490, Nov. 2005.

[77] L. Asiminoaei, R. Teodorescu, F. Blaabjerg, and U. Borup, "Implementation and test of on-Line embedded grid impedance estimation for PV-inverters," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1136–1144, 2005.

[78] Jun Yin, Liuchen Chang, and C. Diduch, "Recent developments in islanding detection for distributed power generation," in *2004 Large Engineering Systems Conference on Power Engineering*, 2004, pp. 124–128.

[79] Jin Beom Jeong, Hee Jun Kim, Soo Hyun Back, and Kang Soon Ahn, "An improved method for anti-islanding by reactive power control," in *2005 International Conference on Electrical Machines and Systems*, 2005, pp. 965–970.

[80] J. E. Kim and J. S. Hwang, "Islanding detection method of distributed generation units connected to power distribution system," in *PowerCon 2000. International Conference on Power System Technology*, 2000, vol. 2, pp. 643–647.

[81] M. B. Reynen, A. H. Osman, and O. P. Malik, "Using gold sequences to improve the performance of correlation based islanding detection," *Electr. Power Syst. Res.*, vol. 80, no. 6, pp. 733–738, Jun. 2010.

[82] M. Sheikholeslamzadeh and T. S. . Sidhu, "Modeling, analysis and improvement of anti-islanding relays for radial distribution system embedding DFIG-DG wind turbines," *25th IEEE Can. Conf. Electr. Comput. Eng.*, pp. 1–5, 2012.

[83] P. J. Moore, J. H. Allmeling, and A. T. Johns, "Frequency relaying based on instantaneous frequency measurement," *IEEE Trans. Power Deliv.*, vol. 11, no. 4, pp. 1737–1742, 1996.

[84] K. Tunlasakun, K. Kirtikara, S. Thepa, and V. Monyakul, "CPLD - based islanding detection for mini grid connected inverter in renewable energy," in *2004 IEEE Region 10 Conference TENCON 2004.*, 2004, vol. D, pp. 175–178.

[85] C. M. Affonso, W. Freitas, W. Xu, and C. D. L. da Silva, "Performance of ROCOF

relays for embedded generation applications," *IEE Proceedings-Generation, Transm. Distrib.*, vol. 152, no. 1, pp. 109–114, Jan. 2005.

[86] J. C. M. Vieira, W. Freitas, W. Xu, and A. Morelato, "Performance of frequency relays for distributed generation protection," *IEEE Trans. Power Deliv.*, vol. 21, no. 3, pp. 1120–1127, Jul. 2006.

[87] J. C. M. Vieira, W. Freitas, Z. Huang, W. Xu, and A. Morelato, "Formulas for predicting the dynamic performance of ROCOF relays for embedded generation applications," *IEE Proc. - Gener. Transm. Distrib.*, vol. 153, no. 4, pp. 399–406, Jul. 2006.

[88] D. Motter, J. C. M. Vieira, and D. V Coury, "Development of frequency-based anti-islanding protection models for synchronous distributed generators suitable for real-time simulations," *IET Gener. Transm. Distrib.*, vol. 9, no. 8, pp. 708–718, May 2015.

[89] C. G. Bright, "COROCOF: Comparison Of Rate Of Change Of Frequency protection. A solution to the detection of loss of mains," in *7th International Conference on Developments in Power Systems Protection*, 2001, no. 479, pp. 70–73.

[90] Fu-Sheng Pai and Shyh-Jier Huang, "A detection algorithm for islanding-prevention of dispersed consumer-owned storage and generating units," *IEEE Trans. Energy Convers.*, vol. 16, no. 4, pp. 346–351, 2001.

[91] W. Freitas, W. Xu, C. M. Affonso, and Z. Huang, "Comparative analysis between ROCOF and vector surge relays for distributed generation applications," *IEEE Trans. Power Deliv.*, vol. 20, no. 2, pp. 1315–1324, Apr. 2005.

[92] W. Freitas and W. Xu, "False operation of vector surge relays," *IEEE Trans. Power Deliv.*, vol. 19, no. 1, pp. 436–438, Jan. 2004.

[93] M. R. Alam, K. M. Muttaqi, and A. Bouzerdoum, "A multifeature-based approach for islanding detection of DG in the subcritical region of vector surge relays," *IEEE Trans. Power Deliv.*, vol. 29, no. 5, pp. 2349–2358, Oct. 2014.

[94] W. Freitas, W. Xu, Z. Huang, and J. C. M. Vieira, "Characteristics of vector surge relays for distributed synchronous generator protection," *Electr. Power Syst. Res.*, vol. 77, no. 2, pp. 170–180, Feb. 2007.

[95] W. Freitas, Z. Huang, and W. Xu, "A practical method for assessing the effectiveness of vector surge relays for distributed generation applications," *IEEE Trans. Power*

Deliv., vol. 20, no. 1, pp. 57–63, Jan. 2005.

[96] S. I. Jang and K. H. Kim, "An islanding detection method for distributed generations using voltage unbalance and total harmonic distortion of current," *IEEE Trans. Power Deliv.*, vol. 19, no. 2, pp. 745–752, Apr. 2004.

[97] T. H. Chen, C. H. Yang, and N. C. Yang, "Examination of the definitions of voltage unbalance," *Int. J. Electr. Power Energy Syst.*, vol. 49, no. 1, pp. 380–385, 2013.

[98] V. Menon and M. H. Nehrir, "A hybrid islanding detection technique using voltage unbalance and frequency set point," *IEEE Trans. Power Syst.*, vol. 22, no. 1, pp. 442–448, Feb. 2007.

[99] S. R. Samantaray, A. Samui, and B. Chitti Babu, "Time-frequency transform-based islanding detection in distributed generation," *IET Renew. Power Gener.*, vol. 5, no. 6, p. 431, 2011.

[100] A. Samui and S. R. Samantaray, "Assessment of ROCPAD relay for islanding detection in distributed generation," *IEEE Trans. Smart Grid*, vol. 2, no. 2, pp. 391–398, Jun. 2011.

[101] P. K. Ray, N. Kishor, and S. R. Mohanty, "Islanding and power quality disturbance detection in grid-connected hybrid power system using wavelet and S-transform," *IEEE Trans. Smart Grid*, vol. 3, no. 3, pp. 1082–1094, Sep. 2012.

[102] A. Samui and S. R. Samantaray, "Wavelet singular entropy based islanding detection in distributed generation," *IEEE Trans. Power Deliv.*, vol. 28, no. 1, pp. 411–418, Jan. 2013.

[103] M. Mishra, M. Sahani, and P. K. Rout, "An islanding detection algorithm for distributed generation based on Hilbert–Huang transform and extreme learning machine," *Sustain. Energy, Grids Networks*, vol. 9, pp. 13–26, Mar. 2017.

[104] K. El-Arroudi, G. Joos, I. Kamwa, and D. T. McGillis, "Intelligent-Based Approach to Islanding Detection in Distributed Generation," *IEEE Trans. Power Deliv.*, vol. 22, no. 2, pp. 828–835, Apr. 2007.

[105] S. R. Samantaray, K. El-Arroudi, G. Joos, and I. Kamwa, "A fuzzy rule based approach for islanding detection in distributed generation," *IEEE Trans. Power Deliv.*, vol. 25, no. 3, pp. 1427–1433, Jul. 2010.

[106] M. Hanif, M. Basu, and K. Gaughan, “Development of EN50438 compliant wavelet-based islanding detection technique for three-phase static distributed generation systems,” *IET Renew. Power Gener.*, vol. 6, no. 4, pp. 289–301, 2012.

[107] A. Pigazo, M. Liserre, R. A. Mastromauro, V. M. Moreno, and A. Dell’Aquila, “Wavelet-based islanding detection in grid-connected PV systems,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4445–4455, Nov. 2009.

[108] A. Khamis, H. Shareef, A. Mohamed, and E. Bizkevelci, “Islanding detection in a distributed generation integrated power system using phase space technique and probabilistic neural network,” *Neurocomputing*, vol. 148, pp. 587–599, Jan. 2015.

[109] V. L. Merlin, R. C. Santos, A. P. Grilo, J. C. M. Vieira, D. V. Coury, and M. Oleskovicz, “A new artificial neural network based method for islanding detection of distributed generators,” *Int. J. Electr. Power Energy Syst.*, vol. 75, pp. 139–151, Feb. 2016.

[110] A. G. Abd-Elkader, D. F. Allam, and E. Tageldin, “Islanding detection method for DFIG wind turbines using artificial neural networks,” *Int. J. Electr. Power Energy Syst.*, vol. 62, pp. 335–343, Nov. 2014.

[111] S. R. Samantaray, B. C. Babu, and P. K. Dash, “Probabilistic neural network based islanding detection in distributed generation,” *Electr. Power Components Syst.*, vol. 39, no. 3, pp. 191–203, Jan. 2011.

[112] M. R. Alam, K. M. Muttaqi, and A. Bouzerdoum, “An approach for assessing the effectiveness of multiple-feature-based SVM method for islanding detection of distributed generation,” *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2844–2852, Jul. 2014.

[113] N. W. A. Lidula and A. D. Rajapakse, “A pattern-recognition approach for detecting power islands using transient signals-Part II: Performance evaluation,” *IEEE Trans. Power Deliv.*, vol. 27, no. 3, pp. 1071–1080, Jul. 2012.

[114] O. N. Faqhruldin, E. F. El-Saadany, and H. H. Zeineldin, “A universal islanding detection technique for distributed generation using pattern recognition,” *IEEE Trans. Smart Grid*, vol. 5, no. 4, pp. 1985–1992, Jul. 2014.

[115] N. W. A. Lidula and A. D. Rajapakse, “A pattern recognition approach for detecting power islands using transient signals-Part I: Design and Implementation,” *IEEE Trans. Power Deliv.*, vol. 25, no. 4, pp. 3070–3077, Oct. 2010.

[116] S. Kar and S. R. Samantaray, “Data-mining-based intelligent anti-islanding protection relay for distributed generations,” *IET Gener. Transm. Distrib.*, vol. 8, no. 4, pp. 629–639, Apr. 2014.

[117] B. Matic-Cuka and M. Kezunovic, “Islanding detection for inverter-based distributed generation using support vector machine method,” *IEEE Trans. Smart Grid*, vol. 5, no. 6, pp. 2676–2686, Nov. 2014.

[118] P. H. Shah and B. R. Bhalja, “A new rate of change of impedance based islanding detection scheme in presence of distributed generation,” *Electr. Power Components Syst.*, vol. 42, no. 11, pp. 1172–1180, Aug. 2014.

[119] K. Sareen, B. R. Bhalja, and R. P. Maheshwari, “Evaluation of superimposed sequence components of currents based islanding detection scheme during DG interconnections,” *Int. J. Emerg. Electr. Power Syst.*, vol. 17, no. 1, pp. 1–14, Jan. 2016.

[120] K. Sareen, B. R. Bhalja, and R. P. Maheshwari, “Islanding detection technique based on inverse hyperbolic secant function,” *IET Renew. Power Gener.*, vol. 10, no. 7, pp. 1002–1009, Aug. 2016.

[121] K. Sareen, B. R. Bhalja, and R. P. Maheshwari, “Current-based islanding detection sheme in presence of distributed generations,” *Electr. Power Components Syst.*, vol. 44, no. 1, pp. 72–81, Jan. 2016.

[122] K. Sareen, B. R. Bhalja, and R. P. Maheshwari, “A hybrid multi-feature based islanding detection technique for grid connected distributed generation,” *Int. J. Emerg. Electr. Power Syst.*, vol. 18, no. 1, 2017.

[123] K. Sareen, B. R. Bhalja, and R. P. Maheshwari, “Universal islanding detection technique based on rate of change of sequence components of currents for distributed generations,” *IET Renew. Power Gener.*, vol. 10, no. 2, pp. 228–237, Feb. 2016.

[124] P. D. Tiwari and O. P. Malik, “Islanding detection of grid connected distributed generation using symmetrical components,” in *2014 6th IEEE Power India International Conference (PIICON)*, 2014, pp. 1–6.

[125] B. Singam and L. Y. Hui, “Assessing SMS and PJD schemes of anti-islanding with varying quality factor,” in *First International Power and Energy Conference, (PECon 2006) Proceedings*, 2006, pp. 196–201.

[126] M. A. Farhan and K. Shanti Swarup, “Mathematical morphology-based islanding detection for distributed generation,” *IET Gener. Transm. Distrib.*, vol. 10, no. 2, pp. 518–525, Feb. 2016.

[127] M. A. A. Farhan and K. S. Swarup, “Islanding detection using mathematical morphology for distributed generation,” in *2017 IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT-Europe)*, 2017, pp. 1–6.

[128] D. Bejmert and T. S. Sidhu, “Investigation Into Islanding Detection With Capacitor Insertion-Based Method,” *IEEE Trans. Power Deliv.*, vol. 29, no. 6, pp. 2485–2492, Dec. 2014.

[129] M. Khodaparastan, H. Vahedi, F. Khazaeli, and H. Oraee, “A novel hybrid islanding detection method for inverter-based DGs using SFS and ROCOF,” *IEEE Trans. Power Deliv.*, vol. 32, no. 5, pp. 2162–2170, Oct. 2017.

[130] S. Akhlaghi, M. Sarailoo, A. Akhlaghi, and A. A. Ghadimi, “A novel hybrid approach using SMS and ROCOF for islanding detection of inverter-based DGs,” in *2017 IEEE Power and Energy Conference at Illinois (PECI)*, 2017, vol. 32, no. 5, pp. 1–7.

[131] P. Gupta, R. S. Bhatia, and D. K. Jain, “Active ROCOF relay for islanding detection,” *IEEE Trans. Power Deliv.*, vol. 32, no. 1, pp. 420–429, Feb. 2017.

[132] P. Mahat, Zhe Chen, and B. Bak-Jensen, “A hybrid islanding detection technique using average rate of voltage change and real power shift,” *IEEE Trans. Power Deliv.*, vol. 24, no. 2, pp. 764–771, Apr. 2009.

[133] M. Garmrudi, H. Nafisi, A. Fereidouni, and H. Hashemi, “A novel hybrid islanding detection technique using rate of voltage change and capacitor tap switching,” *Electr. Power Components Syst.*, vol. 40, no. 10, pp. 1149–1159, Jul. 2012.

[134] B. Zhou *et al.*, “Hybrid islanding detection method based on decision tree and positive feedback for distributed generations,” *IET Gener. Transm. Distrib.*, vol. 9, no. 14, pp. 1819–1825, Nov. 2015.

[135] P. M. Anderson, *Power System Protection*. New York, NY: Wiley, 1998.

[136] A. A. Girgis and S. M. Brahma, “Effect of distributed generation on protective device coordination in distribution system,” in *LESCOPE 01. 2001 Large Engineering Systems Conference on Power Engineering. Conference Proceedings.*, 2001, vol. 24, no. 1, pp.

115–119.

[137] S. T. P. Srinivas and K. S. Swarup, “Optimal relay coordination and communication based protection for microgrid,” in *2017 IEEE Region 10 Symposium (TENSYMP)*, 2017, pp. 1–5.

[138] W. El-khattam and T. S. Sidhu, “Resolving the impact of distributed renewable generation on directional overcurrent relay coordination: a case study,” *IET Renew. Power Gener.*, vol. 3, no. 4, p. 415, 2009.

[139] B. A. Oza, N.-K. C. Nair, R. P. Mehta, and V. H. Makwana, *Power sytem protection and switchgear*, Ist. Tata McGraw Hill Education Private Limited, New Delhi, 2010.

[140] A. Sharma and B. K. Panigrahi, “Phase fault protection scheme for reliable operation of microgrids,” *IEEE Trans. Ind. Appl.*, vol. 9994, no. c, pp. 1–1, 2017.

[141] M. Singh, B. K. Panigrahi, A. R. Abhyankar, R. Mukherjee, and R. Kundu, “Optimal location, size and protection coordination of distributed generation in distribution network,” in *2013 IEEE Symposium on Swarm Intelligence (SIS)*, 2013, pp. 221–227.

[142] A. K. Pradhan, A. Routray, and S. Madhan Gudipalli, “Fault direction estimation in radial distribution system using phase change in sequence current,” *IEEE Trans. Power Deliv.*, vol. 22, no. 4, pp. 2065–2071, Oct. 2007.

[143] B. Bhalja, R. P. Maheshwari, and N. G. Chothani, *Protection and switchgear*. Oxford university press, 2011.

[144] M. Singh, B. K. Panigrahi, and A. R. Abhyankar, “A hybrid protection scheme to mitigate the effect of distributed generation on relay coordination in distribution system,” in *2013 IEEE Power & Energy Society General Meeting*, 2013, pp. 1–5.

[145] M. A. Zamani, A. Yazdani, and T. S. Sidhu, “A communication-assisted protection strategy for inverter-based medium-voltage microgrids,” *IEEE Transactions on Smart Grid*, Dec-2012. [Online]. Available: http://ieeexplore.ieee.org/document/6295696/.

[146] A. A. Sallam and O. P. Malik, *Electric distribution systems*, vol. 68. John Wiley & Sons, 2011.

[147] P. P. Barker and R. W. De Mello, “Determining the impact of distributed generation on power systems. I. Radial distribution systems,” in *Power Engineering Society Summer*

Meeting, 2010, pp. 1645–1656.

[148] T. S. Sidhu and D. Bejmert, "Short-circuit current contribution from large scale PV power plant in the context of distribution power system protection performance," in *IET Conference on Renewable Power Generation (RPG 2011)*, 2011, pp. 134–134.

[149] S. M. Brahma and A. A. Girgis, "Microprocessor-based reclosing to coordinate fuse and recloser in a system with high penetration of distributed generation," in *IEEE Power Engineering Society Winter Meeting. Conference Proceedings*, 2002, vol. 1, pp. 453–458.

[150] A. Zamani, T. Sidhu, and A. Yazdani, "A strategy for protection coordination in radial distribution networks with distributed generators," in *IEEE PES General Meeting*, 2010, pp. 1–8.

[151] P. H. Shah and B. R. Bhalja, "New adaptive digital relaying scheme to tackle recloser–fuse miscoordination during distributed generation interconnections," *IET Gener. Transm. Distrib.*, vol. 8, no. 4, pp. 682–688, Apr. 2014.

[152] M. Yousaf and T. Mahmood, "Protection coordination for a distribution system in the presence of distributed generation," *Turkish J. Electr. Eng. Comput. Sci.*, vol. 25, pp. 408–421, 2017.

[153] S. M. Brahma and A. A. Girgis, "Development of adaptive protection scheme for distribution systems with high penetration of distributed generation," *IEEE Trans. Power Deliv.*, vol. 19, no. 1, pp. 56–63, Jan. 2004.

[154] S. A. M. Javadian and M.-R. Haghifam, "Implementation of a new protection scheme on a real distribution system in presence of DG," in *2008 Joint Int. Conf. on Power System Technology and IEEE Power India Conference*, 2008, pp. 1–7.

[155] S. Chaitusaney and A. Yokoyama, "Prevention of reliability degradation from recloser-fuse miscoordination due to distributed generation," *IEEE Trans. Power Deliv.*, vol. 23, no. 4, pp. 2545–2554, Oct. 2008.

[156] A. Fazanehrafat, S. A. M. Javadian, S. M. T. Bathaee, and M.-R. Haghifam, "Maintaining the recloser-fuse coordination in distribution systems in presence of DG by determining DG's size," in *IET 9th Int. Conf. on Developments in Power Systems Protection*, 2008, vol. 2008, pp. 132–137.

[157] A. F. Naiem, Y. Hegazy, A. Y. Abdelaziz, and M. A. Elsharkawy, “A classification technique for recloser-fuse coordination in distribution systems with distributed generation,” *IEEE Trans. Power Deliv.*, vol. 27, no. 1, pp. 176–185, Jan. 2012.

[158] H. H. Zeineldin and E. F. El-Saadany, “Fault current limiters to mitigate recloser-fuse miscoordination with distributed genertion,” in *10th IET Int. Conf. on Developments in Power System Protection*, 2010.

[159] H. Yazdanpanahi, W. Xu, and Y. W. Li, “A novel fault current control scheme to reduce synchronous DG’s impact on protection coordination,” *IEEE Trans. Power Deliv.*, vol. 29, no. 2, pp. 542–551, Apr. 2014.

[160] A. Elmitwally, E. Gouda, and S. Eladawy, “Restoring recloser-fuse coordination by optimal fault current limiters planning in DG-integrated distribution systems,” *Int. J. Electr. Power Energy Syst.*, vol. 77, pp. 9–18, May 2016.

[161] M.-H. Kim, S.-H. Lim, and J.-C. Kim, “Improvement of recloser-fuse operations and coordination in a power distribution system with SFCL,” *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 2209–2212, Jun. 2011.

[162] B. Hussain, S. M. Sharkh, S. Hussain, and M. A. Abusara, “An adaptive relaying scheme for fuse saving in distribution networks with distributed generation,” *IEEE Trans. Power Deliv.*, vol. 28, no. 2, pp. 669–677, Apr. 2013.

[163] S. Jamali and H. Borhani-Bahabadi, “Recloser time–current–voltage characteristic for fuse saving in distribution networks with DG,” *IET Gener. Transm. Distrib.*, vol. 11, no. 1, pp. 272–279, Jan. 2017.

[164] B. Fani, F. Hajimohammadi, M. Moazzami, and M. J. Morshed, “An adaptive current limiting strategy to prevent fuse-recloser miscoordination in PV-dominated distribution feeders,” *Electr. Power Syst. Res.*, vol. 157, pp. 177–186, Apr. 2018.

[165] W. El-Khattam and T. S. Sidhu, “Restoration of directional overcurrent relay coordination in distributed generation systems utilizing fault current limiter,” *IEEE Trans. Power Deliv.*, vol. 23, no. 2, pp. 576–585, Apr. 2008.

[166] S. Orpe and N.-K. C. Nair, “State of art of fault current limiters and their impact on overcurrent protection,” in *2009 IEEE Power & Energy Society General Meeting*, 2009, pp. 1–5.

[167] M. Tipping, “Sparse Bayesian learning and the relevance vector machine,” *J. Mach. Learn. Res.*, vol. 1, pp. 211–244, 2001.

[168] Tipping Michael, “Relevance Vector Machine,” US Patent 6 633 857 B1, 2003.

[169] B. Bhalja, P. Shah, B. Rakholia, and J. Shah, “A new digital down conductor detection scheme for overhead electrical power distribution systems,” *Int. J. Emerg. Electr. Power Syst.*, vol. 12, no. 5, Jan. 2011.

[170] Sun-Li Yu and Jyh-Cherng Gu, “Removal of decaying DC in current and voltage signals using a modified Fourier filter algorithm,” *IEEE Trans. Power Deliv.*, vol. 16, no. 3, pp. 372–379, Jul. 2001.

[171] S. Das, “Sub-Nyquist rate ADC sampling in digital relays and PMUs: Advantages and challenges,” in *2016 IEEE 6th International Conference on Power Systems (ICPS)*, 2016, pp. 1–6.

[172] B. Bhalja and S. Purohit, “Protection of Double-circuit Transmission Line Using Superimposed Current,” *Electr. Power Components Syst.*, vol. 39, no. 6, pp. 590–604, 2011.

[173] P. K. Nayak, A. K. Pradhan, and P. Bajpai, “A three-terminal line protection scheme immune to power swing,” *IEEE Trans. Power Deliv.*, vol. 31, no. 3, pp. 999–1006, Jun. 2016.

[174] M. T. Bina and A. Kashefi, “Three-phase unbalance of distribution systems: Complementary analysis and experimental case study,” *Int. J. Electr. Power Energy Syst.*, vol. 33, no. 4, pp. 817–826, May 2011.

[175] A. von Jouanne, “Closure on ‘assessment of voltage unbalance,’” *IEEE Trans. Power Deliv.*, vol. 17, no. 4, pp. 1176–1177, Oct. 2002.

[176] P. G. Kini, R. C. Bansal, and R. S. Aithal, “A Novel Approach Toward Interpretation and Application of Voltage Unbalance Factor,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2315–2322, Aug. 2007.

[177] IEC, “Testing and measurement techniques power quality measurement methods,” *IEC 61000-4-30*, 2003.

[178] EN50160, “Voltage characteristics of electricity supplied by public distribution

systems," *Eur. Stand. CLC, BTTF*, pp. 66–68, 1994.

[179] IEEE, "IEEE Recommended Practice for Electric Power Distribution for Industrial Plants," *IEEE Std 141-1993*, 1993.

[180] B. Das, *Power Distribution Automation*, 1st ed. Institution of Engineering and Technology, 2016.

[181] T. S. Ustun, C. Ozansoy, and A. Zayegh, "Modeling of a centralized microgrid protection system and distributed energy resources according to IEC 61850-7-420," *IEEE Trans. Power Syst.*, vol. 27, no. 3, pp. 1560–1567, Aug. 2012.

[182] G. Marchesan, M. R. Muraro, G. Cardoso, L. Mariotto, and A. P. de Morais, "Passive method for distributed-generation island detection based on oscillation frequency," *IEEE Trans. Power Deliv.*, vol. 31, no. 1, pp. 138–146, Feb. 2016.

[183] W. H. Kersting, "Radial distribution test feeders," *IEEE Trans. Power Syst.*, vol. 6, no. 3, pp. 975–985, Aug. 1991.

[184] L. M. Wedepohl, "Application of matrix methods to the solution of travelling-wave phenomena in polyphase systems," *Proc. Inst. Electr. Eng.*, vol. 110, no. 12, p. 2200, 1963.

[185] R. K. Aggarwal, D. V. Coury, A. T. Johns, and A. Kalam, "A practical approach to accurate fault location on extra high voltage teed feeders," *IEEE Trans. Power Deliv.*, vol. 8, no. 3, pp. 874–883, Jul. 1993.

[186] Z. Q. Bo, "A new non-communication protection technique for transmission lines," *IEEE Trans. Power Deliv.*, vol. 13, no. 4, pp. 1073–1078, 1998.

[187] J. A. Brandao Faria and J. H. Briceno Mendez, "Modal analysis of untransposed bilateral three-phase lines-a perturbation approach," *IEEE Trans. Power Deliv.*, vol. 12, no. 1, pp. 497–504, 1997.

[188] C. Christopoulos and A. Wright, *Electrical power system protection*. Springer Science & Business Media, 2012.

[189] Datasheet, "TMS320F28335 Digital signal controllers (DSCs) data sheet," Texas Instruments, 2016.

[190] CCS-v5.1, "Code Composer Studio ™ integrated development environment (IDE)."

[Online]. Available: http://www.ti.com/tool/ccstudio.

[191] H. H. Zeineldin and J. L. Kirtley, “Performance of the OVP/UVP and OFP/UFP method with voltage and frequency dependent loads,” *IEEE Trans. Power Deliv.*, vol. 24, no. 2, pp. 772–778, Apr. 2009.

[192] H.-C. Chen, C.-T. Lee, P.-T. Cheng, R. Teodorescu, and F. Blaabjerg, “A Low-Voltage Ride-Through Technique for Grid-connected Converters with Reduced Power Transistors Stress,” *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8562–8570, Dec. 2016.

[193] W. Guo, L. Xiao, and S. Dai, “Enhancing Low-Voltage Ride-Through Capability and Smoothing Output Power of DFIG With a Superconducting Fault-Current Limiter-Magnetic Energy Storage System,” *IEEE Trans. Energy Convers.*, vol. 27, no. 2, pp. 277–295, Jun. 2012.

[194] C.-T. Lee, C.-W. Hsu, and P.-T. Cheng, “A Low-Voltage Ride-Through Technique for Grid-Connected Converters of Distributed Energy Resources,” *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1821–1832, Jul. 2011.

[195] M. Dietmannsberger, F. Grumm, and D. Schulz, “Simultaneous Implementation of LVRT Capability and Anti-Islanding Detection in Three-Phase Inverters Connected to Low-Voltage Grids,” *IEEE Trans. Energy Convers.*, vol. 32, no. 2, pp. 505–515, Jun. 2017.

[196] Y. M. Makwana and B. R. Bhalja, “Experimental Performance of an Islanding Detection Scheme Based on Modal Components,” *IEEE Trans. Smart Grid*, pp. 1–1, 2017.

[197] H. G. Far, A. J. Rodolakis, and G. Joos, “Synchronous Distributed Generation Islanding Protection Using Intelligent Relays,” *IEEE Trans. Smart Grid*, vol. 3, no. 4, pp. 1695–1703, Dec. 2012.

[198] Y. Makwana and B. R. Bhalja, “Islanding detection technique based on relevance vector machine,” *IET Renew. Power Gener.*, vol. 10, no. 10, pp. 1607–1615, Nov. 2016.

[199] IEEE, “IEEE Std C37.104-2012: IEEE Guide for Automatic Reclosing of Circuit Breakers for AC Distribution and Transmission Lines,” *IEEE Stand.*, vol. 2012, no. July, pp. 1–72, 2012.

[200] S. Chakraborty and S. Das, “Application of Smart Meters in High Impedance Fault

Detection on Distribution Systems," *IEEE Trans. Smart Grid*, no. Early Access, 2018.

[201] H. B. Funmilayo, J. A. Silva, and K. L. Butler-Purry, "Overcurrent Protection for the IEEE 34-Node Radial Test Feeder," *IEEE Trans. Power Deliv.*, vol. 27, no. 2, pp. 459–468, Apr. 2012.

[202] J. Dagenhart, "The 40-Ω ground-fault phenomenon," *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 30–32, 2000.