PERFORMANCE ANALYSIS OF UPS INVERTERS SYSTEM

Ph.D. THESIS

by

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INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
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ROORKEE

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **"PERFORMANCE ANALYSIS OF UPS INVERTERS SYSTEM"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electrical Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from August, 2013 to November, 2018 under the supervision of Dr. Sumit Ghatak Choudhuri, Assistant Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institution.

SANTOSH KUMAR SINGH

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

(Sumit Ghatak Choudhuri)
Supervisor

The Ph.D. Viva-Voce Examination of Santosh Kumar Singh, Research Scholar, has been held on March 2nd, 2019.

Chairperson, SRC **Signature of External Examiner**

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Signature of Supervisor **Head of the Department**

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ABSTRACT

UPS Inverters have been continuously growing during the past years due to power deficits, frequent power cuts, unreliable grid, digital dependency of day to day life, and most important, the demand of clean energy. Developments in power electronic devices, fast processors and advancements in utilisation techniques of renewable sources further catalyse the upsurge. Information Technology (IT) or Information Technology enabled Services (ITeS), such as, Banking, Financial Services and Insurance (BFSI), telecom, healthcare, education and manufacturing sectors heavily rely on UPS. Due to their criticality, at some instances, even a brief interruption is too hazardous and cannot be ignored. Therefore, under such situations, an added backup is utmost essential. Further, predicting future power requirements is almost next to impossible for anyone at the initial stages of planning. Therefore, reliability and power expansion of UPSs are among the major concerns for power supply designers. In addition, high performance, energy efficiency and robust design with low cost have been amongst prime pre-requisites from manufacturer as well as customer end.

This thesis investigates various control strategies for single-phase Pulse Width Modulated (PWM) voltage source inverters used in Uninterruptible Power Supplies (UPS) first for a unit inverter module and then for a parallel bi-module UPS inverter system. For the control of single inverter module, both single-loop and multi-loop control schemes have been examined. It has been observed that multi-loop approaches are better in terms of voltage regulation performance and robustness. However, voltage performance also depends on the compensator or controller utilised in realising the control strategy. Three commonly used integral controllers, namely; Proportional Integral (PI), Proportional Resonant (PR) and Synchronous Reference Frame Proportional Integral (SRF-PI) have been applied to obtain desired the voltage output. Conventionally, PI control suffers from large steady-state error and PR has fixed-point DSP implementation issues. On the other hand, SRF-PI can achieve excellent performance but the design and implementation complexities are high, particularly for the single-phase VSIs. These limitations have been moderated by implementing voltage-loop control in synchronous frame and current-loop in stationary frame of reference.

The presented research investigation further explores different control strategies on parallel inverter modules for enhancement in power rating of the UPS system. The focus has been on different Instantaneous Average Current Sharing (IACS) control schemes due to their better current sharing and expansion flexibilities. At first, using the structure of multi-loop

inductor current feedback control for unit inverters, an Instantaneous Average Current Feed Forward (IACFF) based current sharing scheme has been proposed for multi-inverter UPS system. In this scheme, the instantaneous average current has been feed-forwarded to increase the impedance for the inter-modular circulating current.

Along with the conventional PI and PR based controller based Instantaneous Average Current Sharing (IACS) control schemes, a non-linear and a periodic controller based current sharing control schemes have been attempted for multi-module UPS. An IACS scheme using non-linear controller based Hierarchical Fuzzy Logic (HFL) has been suggested for parallel connection of multi-module UPS inverters. Being a fuzzy based control scheme, the UPS system modelling needs not be precise and robustness of the control is high over wide variations in system parameters. In another IACS control scheme, a periodic controller based Hybrid Iterative Learning (HIL) has also been proposed for the multi-inverter system. Since signals are periodic in UPS application, the HIL has been realised by combining two controllers, i.e. Iterative Learning (IL) and PI control. The steady-state error of the stationary frame PI control can be successfully overcome by employing the IL based controller, whereas the poor transient dynamic of the later can be improved by the PI controller. Therefore, two controllers complement each other in overall performance efficacy of the HIL control. Further, the presented control uses an inductor current feedback to provide both damping to the inverter plant and current sharing control of the multi-inverter UPS system. Therefore, the HIL control reduces the requirement of one sensor per module in the multi-module UPS inverters system to achieve a good voltage regulation and proper current sharing, simultaneously.

A systematic design procedure and control analysis has been presented in due course for the respective control schemes. Simulation investigations and experimental implementations using two single-phase PWM VSIs prove the effectiveness of the proposed theoretical conceptions.

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Santosh Kumar Singh

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LIST OF SYMBOLS

b	System Order
C_j	Filter Capacitance of the j^{th} Inverter
D_{cl}	Denominator of Closed-loop Gain G_{cl}
D_{CM}	Denominator of Current Mode Closed-loop Gain G_{cl}^{CM}
D_{VM}	Denominator of Current Mode Closed-loop Gain G_{cl}^{VM}
d	Repetitive Disturbance
e_1, e_2, e_3	Scaled Error of Fuzzy Logic
e_j	Tracking Error of the j^{th} Inverter
e_{iss}	Steady-State Current Error
e^k	k^{th} Cycle Error
e_{ss}	Steady-State Error
e_{vss}	Steady-State Voltage Error
f	Number of Fuzzy inputs
f_s	Sampling Frequency
g	Fuzzy Subsets
G_c	Current Controller
G_{cl}^{CM}	Closed-loop Voltage Gain in Current Mode
G_{cl}^{CMC}	Closed-loop Voltage Gain for CM Capacitor Current Feedback
G_{cl}^{CMI}	Closed-loop Voltage Gain for CM Inductor Current Feedback
G_{cl}^{CMIL}	Closed-loop Voltage Gain for CM Inductor Plus Load Current Feedback
G_{cl}^{PI}	Closed-loop Voltage Gain Using PI Controller
G_{cl}^{PR}	Closed-loop Voltage Gain Using PR Controller
G_{cl}^{SLVM}	Closed-loop Voltage Gain for Single Loop Voltage Mode
G_{cl}^{SRF}	Closed-loop Voltage Gain Using SRF-PI Controller
G_{cl}^{VM}	Closed-loop Voltage Gain in Voltage Mode
G_{cl}^{VMC}	Closed-loop Voltage Gain for VM Capacitor Current Feedback
G_{cl}^{VMI}	Closed-loop Voltage Gain for VM Inductor Current Feedback
$G_{clK_p}^{SRF}$	Closed-loop Voltage Gain Using SRF-PI Controller with P-Control Only

G_{DB}	Dead Beat Controller Transfer Function
G_f	Fast Controller Transfer Function
G_{FP}^{PI}	Forward Path Gain with PI Controller
G_{FP}^{P-PR}	Forward Path Gain with P-Voltage and PR-Current Controller
G_{FP}^{PR}	Forward Path Gain with PR Controller
G_{FP}^{PR-PR}	Forward Path Gain with PR-Voltage and PR-Current Controller
G_{FP}^{SRF}	Forward Path Gain with SRF-PI Controller
G_{HIC}	Harmonic Impedance Compensation Gain
G_{in}	Inner-Loop Transfer Function
G_p	Open-Loop Plant Transfer Function
G_{pd}	Damped Plant Transfer Function
G_{peff}	Effective Plant Transfer Function
G_{PI}	PI Controller
G_{PR}	PR Controller
$G_{PR}^{'}$	Practical PR Controller
G_{SRF}	SRF-PI Controller
G_v	Voltage Controller Gain
h	Number of Control Variables
H_c	Circulating Current Sharing Controller
$\hat{i}$	imaginary operator
i_c	Filter Capacitor Current
i_{cr}	Circulating Current
i_l	Filter Inductor Current
i_l^*	Reference Inductor Current
i_o	Load Current
i_{o1e}	Current Difference Between FL and HFL Control for Inverter 1
i_{o2e}	Current Difference Between FL and HFL Control for Inverter 2
i_{oav}	Average Load Current
i_{oj}	Output Current of the j^{th} Inverter
i_{oM}	Master Module Output Current
k	Cycle Number
K	RC Constant or IL Gain
K_c	Capacitor Current Active Damping Coefficient or Feedback Gain

K_{ci}	Current Controller Integral Gain
K_{cp}	Current Controller Proportional Gain
K_i	Integral Gain
K_l	Inductor Current Active Damping Coefficient or Feedback Gain
K_p	Proportional Gain
K_v	Voltage Controller Proportional Gain
l	Total Number of Fuzzy Rules
L_j	Filter Inductance of the j^{th} Inverter
m_j	Active Power Droop Coefficient of the j^{th} Inverter
n_j	Reactive Power Droop Coefficient of the j^{th} Inverter
n	Sampling Instant
N	Number of Parallel-Connected Modules
p	Number of Samples in a Fundamental Cycle
P_j	Active power of the j^{th} Inverter
p_1, p_2, p_3	Input Scaling Coefficients of FL
q	Output Scaling Coefficients of FL
$Q(z)$	Low Pass Filter
Q_j	Reactive Power of the j^{th} Inverter
R	Resistance
r_j	Equivalent Series Resistance of the j^{th} Inverter
$S(z)$	Loop Shaping Compensator
S_j	Apparent Power of the j^{th} Inverter
T_s	Sampling Time
$T_{d\text{-}q\rightarrow\alpha\text{-}\beta}$	Inverse Park's Transformation Matrix
$T_{\alpha\text{-}\beta\rightarrow d\text{-}q}$	Park's Transformation Matrix
u_c	Control Signal
$u_{IL}^{\ k}$	k^{th} Cycle Control Signal of IL
V_{dc}	DC Bus Voltage
V_o^*	Nominal Voltage Amplitude
v_e	Voltage Tracking Error
v_i	Inverter Bridge Output
v_m	Modulating Voltage signal
v_o	Output Voltage
v_o^*	Reference Output Voltage

v_{oav}^{*}	Average Reference Voltage
v_{oe}	Voltage Difference Between FL and HFL
v_{oj}	Output Voltage of the j^{th} Inverter
v_{α}	α-Axis Voltage
v_{β}	β-Axis Voltage
x	Control Variable
x_h^{*}	Reference Value of the h^{th} Control Variable
x_{im}	Intermediate Variable
x_h^{pre}	Predicted Value of the h^{th} Control Variable
X	Reactance
y	Output Variable
y^{*}	Reference Command
z^{a}	Time Advancement Unit
Z_{cl}^{CM}	Closed-loop Output Impedance in Current Mode
Z_{cl}^{CMC}	Closed-loop Output Impedance for CM Capacitor Current Feedback
Z_{cl}^{CMI}	Closed-loop Output Impedance for CM Inductor Current Feedback
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$Z_{clK_p}^{SRF}$	Closed-loop Output Impedance Using SRF-PI Controller with P-Control Only
Z_{cr}	Circulating Current Impedance
Z_{cr}^{CM}	Circulating Current Impedance in Current Mode
Z_{cr}^{P-PR}	Circulating Current Impedance with P-Voltage and PR-Current Controller
Z_{cr}^{PR-PR}	Circulating Current Impedance with PR-Voltage and PR-Current Controller

Z_{cl}^{VM}	Circulating Current Impedance in Voltage Mode
Z_j	Output Impedance of the j^{th} Inverter
Z_{lj}	Line Impedance of the j^{th} Inverter
Z_p	Open-Loop Plant Output Impedance
Z_{pd}	Damped Plant Output impedance
z^{-p}	Fundamental Cycle Delay
$\Gamma(z)$	Learning Factor
ε_P	Power Sharing Error
ε_ω	Deviation in Frequency
ζ	Damping Ratio
ϕ	Line Impedance Angle
φ	Initial Phase of the System
δ	Phase Difference between Voltages
θ	Angle between α-β Frame and d-q Frame in rad/s
λ_h	Weighting Factor of the h^{th} Control Variable
ρ	SMC constant
$\mu_i(x_i)$	membership grade
ψ	Sliding Surface or Function
ω	Frequency
ω^*	Nominal Frequency
ω_{bi}	Bandwidth Frequency of Current Controller
ω_c	Cut-off Frequency of PR Controller
ω_n	Natural Frequency of a System
ω_o	Fundamental Frequency
Δv_{fl}	FL Controller Output
ΔE	Maximum Acceptable Amplitude Deviation
ΔI_o	Current Difference between Inverter 1 &2 ($\Delta I_o = I_{o1} - I_{o2}$)
$\Delta\omega$	Maximum Acceptable Frequency Deviation

LIST OF ABBREVIATIONS

3C	Circular Chain Control
AC	Alternating Current
ACC	Average Current Computation
AD	Active Damping
ADC	Analog to Digital Converter
ALCS	Active Load Current Sharing
APF	All Pass Filter
CMC	Current Mode Capacitor
CMF	Cost Minimizing Function
CMI	Current Mode Inductor
CMIL	Current Mode Inductor Load
DC	Direct Current
DSP	Digital Signal Processor / Digital Signal Processing
DTF	Discrete Time Frame
EDF	Error Decay Factor
ESR	Equivalent Series Resistance
FL	Fuzzy Logic
HFL	Hierarchical Fuzzy Logic
HIC	Harmonic Impedance Compensation
HIL	Hybrid Iterative Learning
IACFF	Instantaneous Average Current Feed Forward
IACS	Instantaneous Average Current Sharing
IEC	International Electrotechnical Commission
IGBT	Insulated Gate Bipolar Transistor
IL	Iterative Learning
I-M	Inter-Modular
MF	Membership Function
MLCM	Multi-Loop Current Mode
MLVM	Multi-Loop Voltage Mode
M-M	Multi-Modular
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

MPC	Model Predictive Control
MS	Master Slave
NB	Negative Big
NN	Neural Networks
NS	Negative Small
OSG	Orthogonal Signal Generation
PB	Positive Big
PI	Proportional Integral
PID	Proportional Integral Derivative
PM	Phase Margin
PR	Proportional Resonant
PS	Positive Small
PWM	Pulse Width Modulated
RC	Repetitive Control
RH	Routh Hurwitz
RMS	Root Mean Square
SLVM	Single Loop Voltage Mode
SMC	Sliding Mode Control
SOGI	Second Order Generalised Integrator
SPWM	Sinusoidal Pulse Width Modulated
SRF	Synchronous Reference Frame
SRF-PI	Synchronous Reference Frame Proportional Integral
THD	Total Harmonic Distortion
UPS	Uninterruptable Power Supply
VMC	Voltage Mode Capacitor
VMI	Voltage Mode Inductor
VSI	Voltage Source Inverter
ZOH	Zero Order Hold

CHAPTER 1: INTRODUCTION

The influence of electrical and electronics devices in human being's modern life are emerging day by day. Usually, these devices receive energy from the utility grid. As the power grid is distributed in a wide area, in which generation and consumption have numerous interfaces, which eventually hampers its reliability. Developing nations like, India still face shortage of power due to gap between demand and supply of the electricity. Amidst government's supportive policy interventions and sector reforms, power deficit show a decreasing trend with average energy deficit reduced to 0.7 % and peak deficit to just 2 % [1]. However, these deficits only show the figures for those who are formally connected to the grid. The demand of unconnected users and informal consumers (usually included in line loss) remains unaccounted in these data. Further, power demand from rural India, mostly involved in agriculture sector, is either ignored or calculations are based on limited hours of supply. The true picture therefore can be captured by India's per capita electricity consumption, which is still on the lower side. With an energy consumption of just 818 units, India stands far behind China (4,292), European Union (5,368) and US (11,974) as per statistics in 2015 [2]. Therefore, Uninterruptable power supplies are prerequisite of power security and continuity for any developing economies, like India.

According to a market research report by KEN Research, in recent years, UPS and inverter market have been steadily growing, at an annual growth rate of 8.9% in India [3]. It includes both global UPS manufacturers like Eaton, Emerson, APC and local makers such as Luminous, Microtek, Su-Kam and others. The growth of UPS market itself acknowledges the widening gap between the actual demand and availability of electricity. In an industry report, value wise market size for UPS inverters in India has been projected in Figure 1.1 [4]. Another, recently published TechSci Research report estimates the UPS market of India to surpass 1.2 billion USD whereas the global market to reach about 9.8 billion USD by 2021 [5], [6]. Although, the major thrust for the growth of inverters and UPS is the power deficit, power quality and reliability are becoming crucial for the modern day electronics based equipment. Indian Electricity Rules, 1956 allow variations for voltage and frequency within $\pm$ 6% and $\pm$ 3%, respectively from the nominal value [7]. However in reality, standard voltage of 230 V in India can dip down to 120 V and frequency can go below 45 Hz or above 55 Hz for a 50 Hz grid [8]. Information Technology (IT) or Information Technology enabled Services (ITeS) such as; Banking, Financial Services and Insurance (BFSI), telecom,

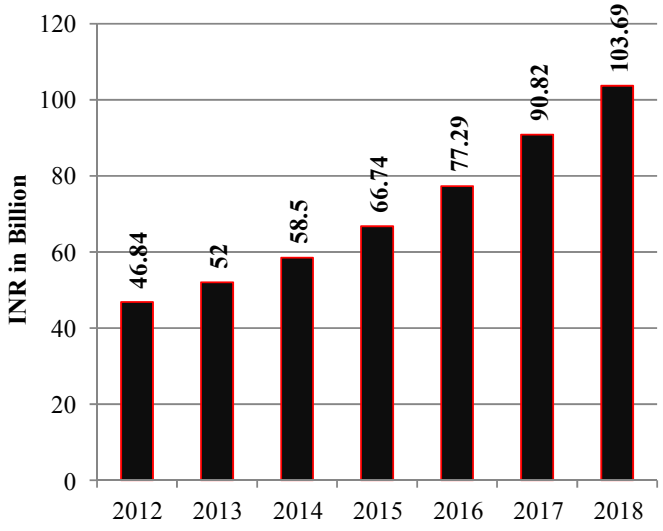


Figure 1.1 India UPS market size in terms of value.[4]

healthcare, education, etc. are now processor based and are very susceptible and sensitive to voltage disturbances. Further, with last mile electricity connectivity, power scenario of rural India has shifted its focus from being just a subsidised agro-based economy to power-demanding consumer based thriving market. As the UPS industry sustains on the power shortage, it would open a new potential market to expand and grow. Moreover, India as an economy is undergoing huge transformations with per capita income of Indians going up and overall improvement in lifestyles. Government initiative schemes such as; Make in India, Digital India and push for the developmental projects in infrastructure, IT/ITeS sectors in Tier II cities, healthcare and residential sectors would definitely expand the India's UPS market in the coming years. Summarily, growth factors of UPS systems can be attributed to power deficits, frequent power cuts, unstable grid, digital dependency of every day's life and rapid industrialisation and commercialisation of services.

The following sections present necessary background, motivation and organisation of the presented work. State-of-art for Uninterruptible power supplies system has been illustrated, with an introduction to modular UPS inverters system. The thesis outline has also been projected in this chapter.

1.1 UPS System Architecture

Uninterruptible Power Supply is a power electronic system that maintains the continuity and quality of power to the critical (which cannot afford power cut) or protected load, when the normal utility grid fails to do so. UPS is generally inserted in-between the utility power

grid and the critical load. UPS provides power supply converting either from the normal source and/or from any stored energy source when the utility fails partially or totally [9]–[11]. The International Electrotechnical Commission (IEC) has categorised UPS systems into three configurations, generally referred to as UPS topologies in IEC Standard 62040-3[12]. The three topologies namely are standby, line interactive and double conversion, which are discussed in the following sub-sections.

1.1.1 Stand-By (Offline) UPS

Figure 1.2 shows typical layout of a Stand-by topology of UPS, generally known as Offline UPS or line preferred UPS [12]. It comprises of a battery charger (AC-DC and/or DC-DC converter), DC-AC inverter, Battery pack and a Bypass Static Switch. In normal mode of operation (shown by blue dashed arrow in Figure 1.2), the load is fed directly from the utility ac mains through the bypass static switch. The battery is also re-charged is in this mode via a set of AC-DC and/or DC-DC converter. Rating of the battery charger need not to be same as the full load inverter system, since it is never loaded directly, which makes the UPS economic as a consequence. If the AC mains falls out of pre-set tolerances, then the UPS enters into stored energy or back-up mode (shown in red dashed arrow), in which the DC-AC inverter directly supplies the load from the battery-pack. This mode lasts until the AC input returns to predefined limits and the UPS enters normal mode or the battery dries up, whichever is sooner.

Stand-by UPS lacks in any kind of isolation between the utility and the load and has no control on voltage and frequency (since load is directly connected to utility normally). The longer transfer time from normal to back up mode is also one of its limitations. However, lower costs and smaller sizes due to the battery charger are among its advantages [13]. Sometimes, passive line conditioning filters are inserted before the load which is a very robust

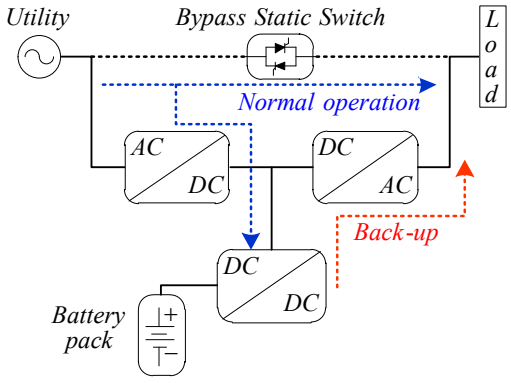


Figure 1.2 Typical stand-by (Offline) topology of UPS.

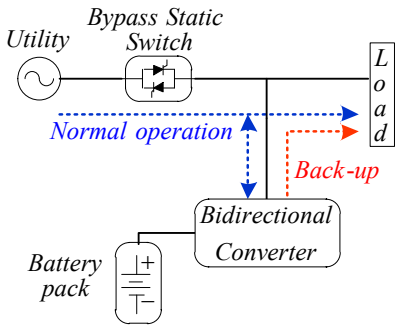


Figure 1.3 Typical line-interactive topology of UPS.

solution to tackle utility distortions [14].

1.1.2 Line Interactive UPS

Line interactive UPS topology, as shown in Figure 1.3, comprises of a Bidirectional Converter, Battery pack and a Bypass Static Switch. In normal mode of operation, load is fed with the conditioned utility supply via the bidirectional converter (inverter) working in parallel to AC mains. At the same time, bidirectional converter also recharges the battery pack. The output voltage magnitude can be regulated but the frequency is utility dependent. On failure of AC mains, the static switch isolates the load from the utility and the battery-inverter set maintains power continuity to the load in the back-up mode. The UPS returns to the normal mode once AC supply pre-set tolerance is restored [15], [16].

The main advantage this topology is that it offers lower cost and high efficiency as compared to double conversion topology (to be discussed in next sub-section). Moreover, Active filtering capabilities provide a better voltage regulation. However, lack of effective isolation and no regulation of output frequency are amongst its primary demerits [13].

1.1.3 Double-Conversion (Online) UPS

Double conversion topology as shown in Figure 1.4, also known as inverter preferred or online UPS is the most popular configuration of the UPS systems. In this topology, the inverter is always connected in series in between utility and load, thus provides the best protection against the raw utility power. Double conversion, as the name suggests, processes the utility power twice i.e., utility to dc-link via AC-DC converter, and then DC-AC inverter processes back to AC to feed the critical load. The main role of the static switch, as shown in Figure 1.4, is not for transferring power modes, but for bypassing the UPS on failure. In normal mode, the load is continuously supplied through rectifier-inverter combination and the battery pack is charged, simultaneously. When the utility voltage and frequency fall out of the

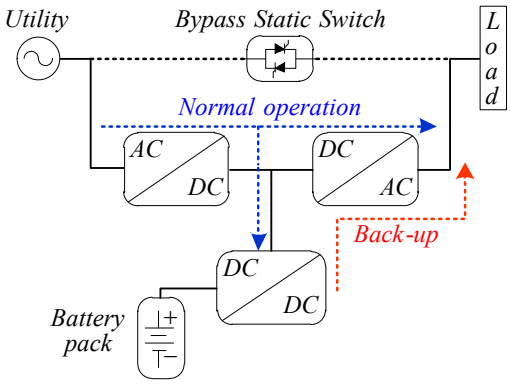


Figure 1.4 Typical double conversion (Online) topology of UPS.

predefined tolerance limits, the battery-inverter set supplies the connected critical load in the stored energy mode. Since, the UPS inverter continuously supplies the load, thus no transfer time is associated in transition from normal to stored energy mode.

The main highlight of the double conversion UPS is wide tolerances of the input voltage, tight regulations of output voltage and frequency and no transfer time on mode transitions. The demerits of this topology are low power factor and high current THD (%) at the input due to the entire load is supported by the front-end converter. Therefore, rating of the rectifier is either equal to the inverter rating or usually higher, to accommodate the battery charging also, which increases overall cost of the UPS. Due to double conversion, efficiency is observed to be relatively lower. However, numerous performance benefits clearly outweigh the drawbacks.

1.2 Modular UPS System

According to [6], the power range segmentation include below 1kVA, 1-5 kVA, 5-10 kVA, 10-20 kVA, 20-50 kVA, 50-100 kVA and above100 kVA. As the size of the organisation expands, in which the UPS is installed, more and more high rating power supplies are required. High rated UPSs however need large heat dispersal mechanism and high current handling capabilities, which eventually lowers reliability and increases installation and operating costs. A possible solution to the problem is modularisation and integration for achieving higher rated critical load power protection. Low power UPS inverter modules can be therefore connected in parallel to feed a common load bus. The use of Multi-Modular (M-M) UPSs have advantages over a single high-capacity inverter such as, low current handling stress, easier shipping and installation, ease of maintenance and repair,

increased reliability, improved thermal management, economical manufacturing and flexibility for power expansion, etc. [17], [18].

1.2.1 Parallel UPS Inverter Configuration

In order to achieve benefits of modularised UPS configuration, following basic structures are discussed. Figure 1.5 shows a modular structure in which only DC-AC inverters are connected in parallel to feed the common AC load [19]. It is easier to control this modular configuration since parallel connection issues related to only DC-AC inverters need to be addressed to. However, the common AC-DC converter and the DC-link limit benefits of true modularity. Moreover, DC-link voltage fluctuates highly on inclusion and exclusion of DC-AC modules, which affects the AC side critical loads. In Figure 1.6(a), another modular configuration is shown in which the complete UPS module (comprising of AC-DC and DC-AC converters) works in parallel [20]. Each module can operate independently as a separate UPS entity as a real modular structure. Nevertheless, control is quite complex as both input and output AC sides are in parallel configuration. Another configuration, in which UPSs with separate power source are connected in parallel, is shown in Figure 1.6(b). Dedicated separate DC-link alleviates from the complexities of control on input side. Further, modularity is not compromised.

1.2.2 Challenges Involved In Modular UPS Inverter

An UPS inverter with close-loop control emulates an ideal voltage source with very low internal impedance. As a result, simply connecting two or more such voltage sources in parallel would not result in proper operation and may even lead to destruction. Inverters are designed with very fast dynamic responses to meet specifications under non-linear loadings

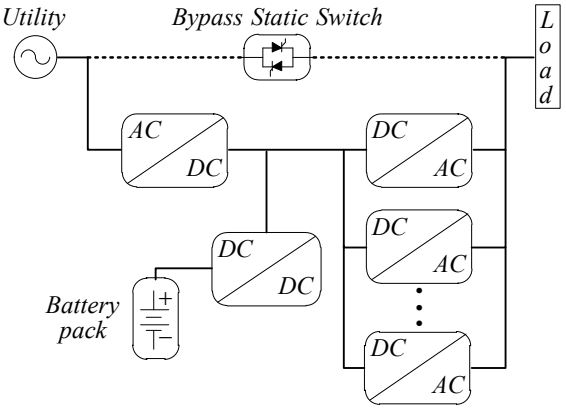


Figure 1.5 Block diagram of a typical UPS system with several inverters in parallel.

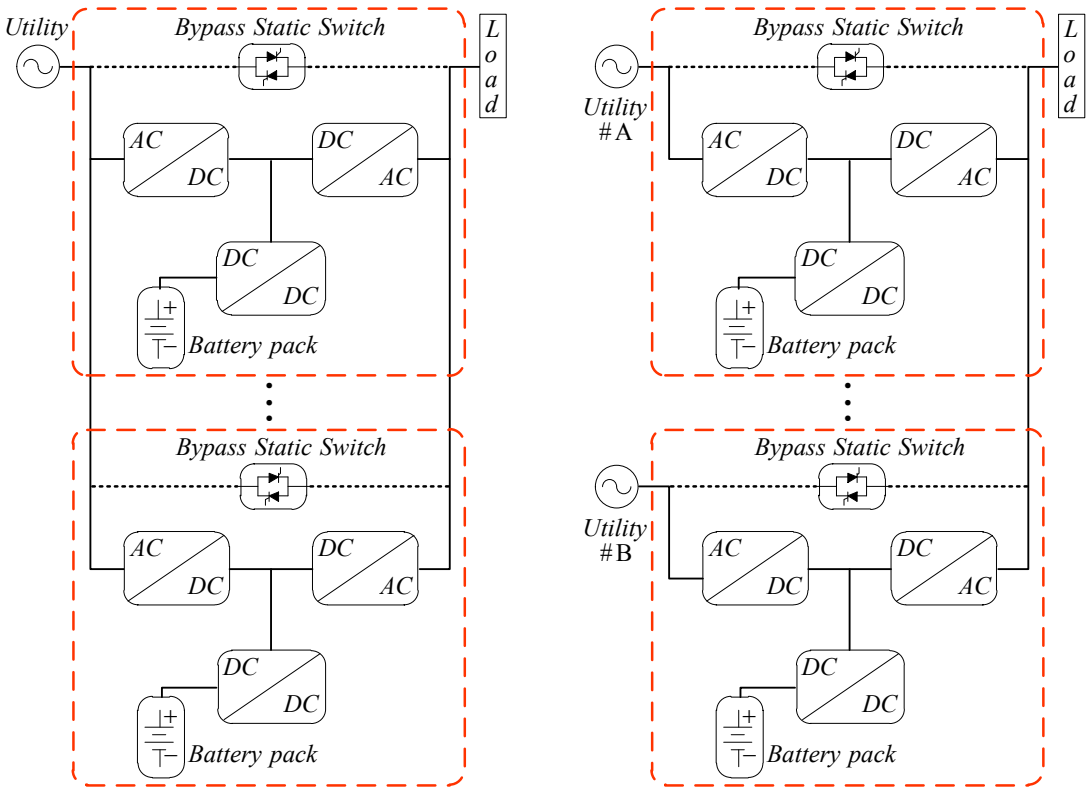


Figure 1.6 Block schematic of (a) UPS systems working in parallel and (b) UPS systems with dedicated power source is working in parallel.

and step load transitions. Therefore, inverter current can change quite fast, and with limited overload capabilities, the inverter enters current limiting mode almost instantaneously.

For an illustration, the Inter-Modular (I-M) circulating current (I_{cir}) between two UPS inverters connected in parallel has been expressed in [21] and is as follows:

$$I_{cir} = \frac{V_1 - V_2}{Z_1 + Z_2} \approx \frac{V_1 - V_2}{2Z} \quad \text{on an assumption, } Z_1 = Z_2 = Z \tag{1.1}$$

where V_1 and V_2 are respective inverter output voltages having internal impedances Z_1 and Z_2. Since, the internal impedance Z is very low, which is usually the case, even a small deviation of phase and amplitude of voltage results into huge circulating currents. In practice, no two inverters have identical terminal voltages due to tolerance in filter parameters, temperature drifts of hardware components, dead band, etc. Such a condition may cause unequal loading of inverters, unnecessary power loss and even distortion of voltage waveform in the parallel

connected inverters system [22]. Out of several available equal current sharing control techniques, primarily, two classifications may be done on the basis of inter-connections among inverter modules: Voltage and Frequency Droop Method (wireless and non-information sharing) and Active Load Current Sharing (ALCS) Method (wire-connected and information sharing) [23]. Although, Droop control method is highly reliable and modular in nature, voltage regulation and power sharing performance are not satisfactory. In order to achieve improved voltage quality and load current sharing simultaneously, the latter approach of ALCS is preferred. ALCS is an instantaneous current sharing technique, which can be further categorised into Centralised control, Master Slave (MS) control, Circular Chain Control (3C) and Instantaneous Average Current Sharing (IACS) control. A detailed review of these current sharing techniques has been discussed in Chapter 2.

In all configurations, the core of the UPS system is a Pulse Width Modulated (PWM) Voltage Source Inverter (VSI). Performance and reliability of UPS systems therefore largely depend on VSIs [24], [25]. The prime objective of the UPS inverter is to produce a sinusoidal output voltage with low Total Harmonic Distortion (THD) under any condition. However, second order model of a typical single-phase UPS inverter, insists for a cautious compensator and controller design process.

The above mentioned output voltage quality and dynamics standards of UPS system, as given by IEC 62040-3, also applies to parallel operation of modules. Therefore, VSIs having second order dynamics with low output impedance poses a serious challenge towards inverter control when connected in parallel for power expansion.

1.3 Research Objectives and Scope

The prime focus of this work is to investigate the advance control architectures for single-phase UPS inverters with an aim to increase the overall power capacity of the UPS system. In due course, the following objectives were set:

- To identify the problems and complexities involved in the control of unit single-phase UPS inverter module.
- To investigate issues with advance control schemes in UPS multi-inverters system and propose a simplified IACS control scheme to limit I-M circulating currents without inserting a physical component in the power circuit.
- Further, to investigate towards achieving a robust and simple control technique to improve voltage regulation and power sharing performance over wide variation of system parameters.

- To explore a possibility of overall cost-reduction using an advance control technique so that the performance of UPS inverter system is not compromised.
- To develop a Digital Signal Processor (DSP) based prototype for validation of the proposed control strategies and thereby compare the performance indices under different operating conditions.

In order to achieve the above-mentioned objectives, the scope of this thesis has been established. Single-phase H-bridge UPS inverters have been used to demonstrate the propositions. Inverters have been assumed to be ideal in nature. In this work, isolated DC voltage sources have been used for respective inverter modules. For analysis, DC link voltages have been assumed to be stiff throughout the investigation.

1.4 Description of the Research Work

Single-phase UPS inverters are basically second order systems whose frequency response shows an undamped resonance peak. Such a high peak may cause large tracking error and pose threat towards stability at corresponding frequencies, particularly on step change of load or command-voltage. Since the reference command is a time varying quantity, elimination of steady-state tracking error is also not simple. In view of the above, following have been executed towards development of unit UPS inverter:

- Classification, mathematical modeling and simulation analysis of different control strategies of UPS inverters have been carried out to analyse and compare performance. This helps to assess the pros and cons of selecting a specific control strategy for a particular application.
- Difficulties and Complexities in control of the single-phase inverter in stationary reference frame and Synchronous Reference Frame (SRF) have been investigated. In due process, a strategy has been developed which tries to reduce implementation complexities by employing control scheme that is a combination of both reference frames.
- Detailed design of the suggested control scheme is presented and dynamic performances of unit UPS Inverter have been compared with Proportional Integral (PI) and Proportional Resonant (PR) based integral controllers through simulation analysis and experimental verifications.

In order to enhance the power level of UPS system, two or more inverters have been connected in parallel to supply the increased load demand. Due to good current sharing, better voltage regulation and independent control structure, IACS control has been selected in this investigation. Figure 1.7, shows a conceptual block schematic that depicts IACS control

strategy for a multi-inverter UPS system. Each inverter module consists of a constant DC source, an H-Bridge inverter and an output LC filter. L_j, r_j and C_j represent the inductance, resistance and capacitance, respectively of the filter. Z_{lj} refers to the line impedance connecting the j^{th} inverter module to the critical load. Three feedback signals namely, output voltage, inductor current and output current of respective modules have been used as feedback variables for the control of inverter. For realisation of IACS strategy, each inverter provides its output current information to an Average Current Computation (ACC) block, which generates an average-current reference signal for all inverter modules of the M-M UPS inverters system. Following work has been performed for proper operation of M-M UPS inverters system.

- Current sharing problem in M-M UPS inverters system has been analysed based on the mathematical modelling of I-M circulating current impedance. I-M circulating current impedance of commonly used control schemes has been investigated and in due process, multi-loop control strategy with inductor current feedback has been observed to have better I-M circulating current immunity. This may serve as the ground base for developing a new current sharing strategy.
- Instantaneous Average Current Feed Forward (IACFF) multi-loop control strategy using inductor current feedback has been proposed for M-M UPS inverters system. This scheme achieves an equal current sharing with a simplified IACS control technique through the direct regulation of the current controller without any additional current sharing loop. Further, effect of voltage controller on circulating currents has

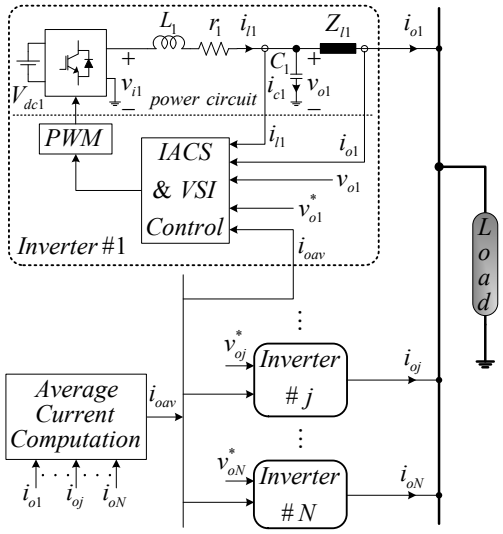


Figure 1.7 Multi-Modular UPS inverters system.

been also investigated. Design and analysis of the proposed control scheme have been validated through simulations in MATLAB/Simulink and practical implementation on TMS320F2812 DSP platform, using two parallel-connected inverters.

- Hierarchical Fuzzy Logic (HFL) control, which inherits the advantages of Fuzzy Logic (FL) control, has been proposed for single-phase M-M UPS inverters system using IACS control technique. The proposed HFL successfully establishes current sharing capability with a better voltage regulation on wide variations in system parameters. On one hand, it eliminates the design complexity of multiple tuning of conventional PI based controllers and on the other hand, it reduces the memory requirements of conventional FL controller.
- Hybrid Iterative Learning (HIL) control methodology using Iterative control and PI control in parallel has been proposed to achieve an almost perfect voltage tracking in steady state and a satisfactory transient state performance for single-phase UPS inverters. An excellent disturbance rejection has been achieved under non-linear loading in spite of using inner-loop inductor current feedback. Learning nature of the HIL controller wipes out load current disturbances on successive iterations. Later, the same concept has been implemented for IACS control of single-phase M-M UPS inverters system. The proposed control scheme utilizes a single inductor current measurement for both active damping and current sharing, which enables the 'N'– Modular inverters system to be successfully operated using '2N' sensors as against to '3N' sensors in the conventional multi-inverter UPS system. Such a strategy thereby helps to reduce the total sensor count leading to enhanced robustness at a lower cost.

1.5 Thesis Organization

This thesis is organised into seven chapters, whose focus and contributions are illustrated briefly as follows:

- **Chapter 1** presents introduction to the research area.
- **Chapter 2** gives a detailed literature review of the existing State-of-Art control techniques for the single-phase UPS inverter. Later, it also covers a detailed survey of standalone parallel-connected multi-inverters system for supplying enhanced load demand. The focus is concentrated towards Instantaneous Average Current Sharing (IACS) control scheme for parallel-connected inverter modules.
- In **Chapter 3**, an instantaneous control of single-phase Uni-Modular inverter is presented. Firstly, alternative close-loop control schemes have been investigated and compared under different operating conditions through a series of MATLAB simulations in Discrete Time

Frame (DTF). The problems and complexities involved in the control of single-phase UPS inverter supplying variable loads have been identified and analysed. Finally, a detailed design of instantaneous control of VSI in combined reference frame has been presented and its performance has been compared using different integral controllers through simulation and experimental investigations.

- **Chapter 4** proposes IACFF strategy based current-sharing scheme for parallel-connected M-M UPS inverters system. Mathematical modeling of I-M circulating current impedance for the parallel inverters system has been derived for different close-loop control strategies. Based on the investigation, IACFF strategy has been presented which exhibits that I-M circulating current impedance can be enhanced with inductor current feedback without compromising on voltage regulation. A step-by-step systematic design procedure using frequency response analysis has been presented in sequence. Finally, the chapter concludes with results and discussions based on simulations and experimental results obtained.
- **Chapter 5** proposes Hierarchical Fuzzy Logic based non-linear control scheme for multi-inverters UPS system. It begins with development of FL control algorithm for the parallel-connected UPS inverters system, followed by systematic conversion of conventional FL rules to HFL rule base. Equivalence of conventional FL and HFL has been established through simulation results in MATLAB environment. In the meantime, robustness of the proposed HFL controlled UPS inverters system has also been demonstrated when the parameters have been varied in a wide range. Finally, the effectiveness of proposed scheme has been verified through simulations and experimental results.
- In **Chapter 6**, a hybrid strategy has been developed through combination of PI and Iterative control, nomenclated as Hybrid Iterative Learning (HIL) control for UPS inverters. HIL control uses inductor current as inner-loop feedback for a single inverter unit. The concept has also been extended for the control of M-M UPS inverters system using IACS scheme for current sharing. In addition to the improvement in system performance, it has also been demonstrated that HIL control has the potential to reduce the total sensor count in case of multi-inverter UPS system. Thereafter, design methodologies proposed in HIL control have been presented in detail. Finally, results have been validated through simulations in MATLAB environment and prototype implementations for both Uni-Modular and M-M UPS inverters system.
- Investigations conclude by stating overall achievements of the research endeavored, in **Chapter 7** and some recommendations for possible future work prospects have also been stated.

CHAPTER 2: LITERATURE SURVEY

2.1 Introduction

In this chapter, at first most common inverter configurations of the single-phase UPS inverter and their dynamic characteristics have been discussed. Then, issues involved in control of the inverter have been analysed from their consequent transfer function model. Next, the most popular and widely used control techniques for single-phase inverters have been surveyed. These control techniques may be classified in different ways, such as analog-digital control, linear-nonlinear control, single loop-multi loop control, etc., [26], [27]. Nowadays, digital control of power electronic converters is in trend due to advantages over their analog counterparts.

Further, as power demand of load rises, either a higher rating module replaces existing UPS or a similar module is added to the present unit. The latter approach appears to be more practical considering installation cost, reliability, redundancy and future expansion plans. However, adding two or more inverters and operating AC output in parallel to increase power level is not an easy task. The final part of the chapter, therefore reviews different aspects of control for paralleling of multi-module UPS inverters with their relative merits and demerits.

2.2 Single-Phase UPS Inverter

UPS systems widely use DC-AC converter as an integral part to maintain high quality constant voltage and constant frequency output. Majority of the UPSs consist of buck-converter topology based VSI whose AC RMS output is always below the DC-link voltage.

2.2.1 UPS Inverter Topologies

Figure 2.1(a) and (b) shows two most frequently used topologies for single-phase applications namely, half-bridge and full-bridge configurations, respectively. The peak output voltage of the full-bridge inverter is twice the half-bridge inverter with the same input DC voltage. A typical VSI system comprises of a stiff DC voltage source V_{dc}, active switching devices (IGBTs or MOSFETs) S_1-S_4 and a low-pass output LC filter. LC filter of the power circuit eliminates high frequency switching disturbances and ensures smooth sinusoidal output voltage with low THD [28], [29]. L, r and C represent inductance, inductor Equivalent Series Resistance (ESR) and capacitance of the filter, respectively for the inverter.

(a) (b)

Figure 2.1 Single-phase UPS inverter (a) Half-bridge and (b) Full-bridge topology.

2.2.2 Dynamic Modelling of UPS Inverter

Inverter dynamics may be described by the following set of differential equations, obtained from Figure 2.1(b).

$$L\frac{di_l}{dt} = v_i - v_o - ri_l \tag{2.1}$$

$$C\frac{dv_o}{dt} = i_l - i_o = i_c \tag{2.2}$$

Applying the Laplace transformation on (2.1) and (2.2) gives,

$$i_l(s) = \frac{1}{sL+r}\{v_i(s) - v_o(s)\} \tag{2.3}$$

$$v_o(s) = \frac{1}{sC}\{i_l(s) - i_o(s)\} = \frac{1}{sC}i_c(s) \tag{2.4}$$

Here, i_l, i_o, i_c, v_i and v_o denote inductor current, output current, capacitor current, inverter bridge output and filter output voltage, respectively. Using (2.3) and (2.4), the block schematic representation of the VSI plant may be obtained as shown in Figure 2.2. Considering the fact, that switching frequency is several times of the fundamental frequency, PWM inverter may be modelled as a linear block of gain '*M*' neglecting any switching dynamics of the inverter bridge [29]. The voltage, v_i is "instantaneous average" value (the average value over one cycle of the switching frequency) of the control input or modulating function v_m. For convenience of controller design and analysis, gain '*M*' may assume to be unity. Consequently, the output LC filter primarily governs the inverter modelling. The output voltage can be obtained by substituting (2.3) in (2.4) and performing some mathematical rearrangements as,

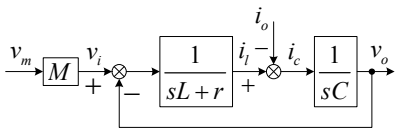


Figure 2.2 Block schematic representation of single-phase voltage source inverter.

Table 2.1 System parameters

Parameter	**Value**
Filter Inductance, L	1 mH
Filter Inductor ESR, r	0.5 Ω
Filter Capacitance, C	18 μF
Switching frequency, f_s	10 kHz

$$v_o(s) = G_p(s)v_i(s) - Z_p(s)i_o(s) \tag{2.5}$$

where, $G_p(s) = \dfrac{1}{s^2LC + srC + 1}$ and $Z_p(s) = \dfrac{sL + r}{s^2LC + srC + 1}$. From (2.5), it can be seen that the output voltage depends on the filter input voltage, v_i and the load current, i_o. The first term $G_p(s)$ is referred as output to input voltage transfer gain and ideally, it should be unity for exact input voltage following. The second term $Z_p(s)$ of (2.5) is commonly designated as the inverter plant output impedance and represents the load current influence on the output voltage. The load current therefore may be considered as a disturbance component to the inverter output and ideally should be zero for perfect voltage tracking.

The parameters of the UPS inverter system used in this research work are enlisted in Table 2.1. The magnitude and phase curves of the voltage gain, $G_p(s)$ and the output impedance, $Z_p(s)$ with the above system parameters are shown in Figure 2.3. Inverter plant shows a resonant peak, like any other under-damped, second order systems. Such a high peak induces oscillations or in the worst case, may even cause instability due to signals at corresponding frequencies. An abrupt change in reference voltage such as, during turn-on, may inject amplified harmonic voltages at the output. Appearance of peak in impedance Z_p introduces distortions in the output voltage due to non-zero second part of the (4.1), particularly in case of non-linear loading. High ESR may bring down the resonant peak magnitude however, at the same time it increases the operating frequency impedance magnitude of the inverter plant, as seen from Figure 2.3(b). This not only deteriorates the reference tracking, but also reduces

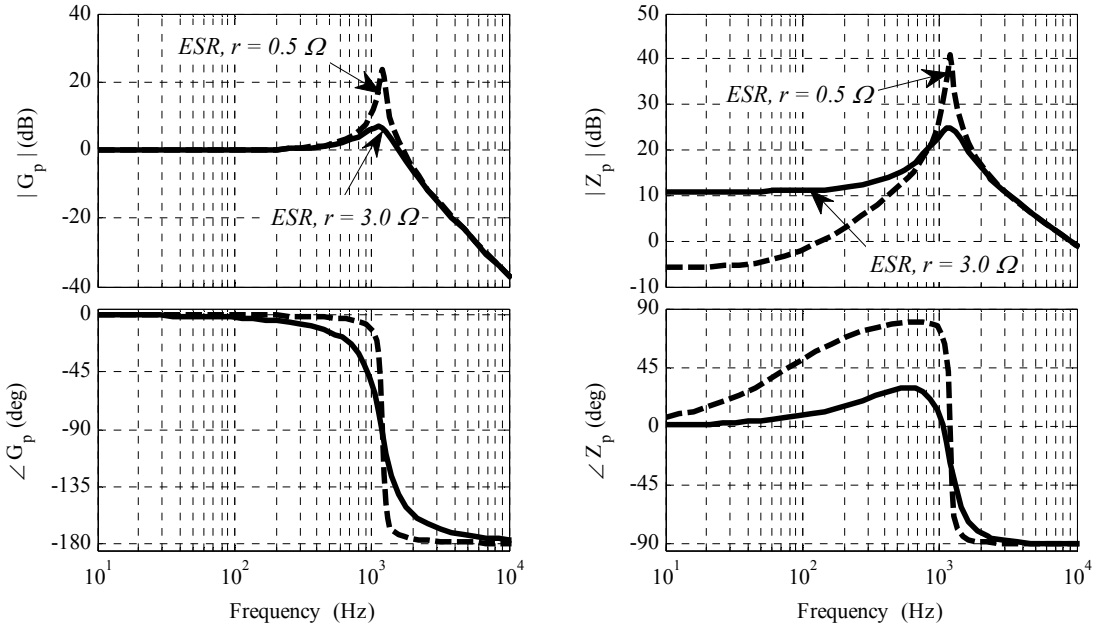


Figure 2.3 Bode plots for inverter plant (a) Voltage gain and (b) Output impedance.

the inverter efficiency. Thus, some provisions to damp the resonant peak need to be incorporated in the compensator while design, to avoid such adverse conditions. Therefore, following are the challenges or requirements of the inverter control:

1. Inverter plant resonant peak reduction or elimination,
2. High control bandwidth for fast dynamic performance which may get affected if the bandwidth is reduced below the resonant peak,
3. Controller should be capable to deal with the AC signals,
4. Good control robustness to tackle parametric variations and tolerances,
5. Finally, cost should be minimal with reduced number of sensors and reduced complexity in design.

2.3 Closed-Loop Control of Single-Phase UPS Inverter

The performance of UPS inverter system depends on the applied closed-loop control strategy [19]. In early control of inverters, only RMS value of the output voltage had been regulated while the waveform shape was mostly overlooked. Although steady state response had been satisfactory under linear loads, non-linear loads greatly distorted the output voltage waveform [30]. Moreover, sub-cyclic disturbances such as, step load changes, require several cycles for recovery [31]. With the advancement in semiconductor devices and digital control

technology, high-speed instantaneous controllers have been developed. Many instantaneous controllers have been discussed in literature, which update the inverter output waveform at the speed of switching frequency, which is typically several order of the fundamental frequency. This can shape the entire cycle of the waveform, rather than mere regulation of the RMS magnitude. Therefore, today almost all schemes of inverter control are instantaneous in nature, which have low voltage %THD and better disturbance rejection with faster and better transient response [32].

In an instantaneous inverter control, the actual output voltage is compared with the reference sinusoidal signal on an immediate basis or sample by sample basis in analog or digital control. After the error is passed through a regulator, the compensated signal is sent to a modulator as control input. The modulator may use a suitable technique such as, Sinusoidal PWM (SPWM) technique for generating switching signals for devices of the inverter.Figure 2.4(a) shows the single-loop control scheme for voltage regulation. Besides output voltage feedback, v_o, inverters also take advantage of either load current, i_o or/and filter inductor current, i_l or/and filter capacitor current, i_c feedbacks to improve its performance. These are multi-loop control schemes in which, both voltage and currents are regulated either for better performance or for employing protection functionality. Figure 2.4(b) shows the multi-loop control scheme where an inner current-loop is also incorporated. Current, i^* is the reference for inner loop which may be any current variable. Several literatures have discussed various control schemes for UPS inverters [30], [33]–[36]. Most of the researchers utilise either output voltage and/or one or more current feedbacks to implement the instantaneous inverter control. Classification and detailed analysis of various control schemes for UPS inverter system has been discussed in Chapter 3.

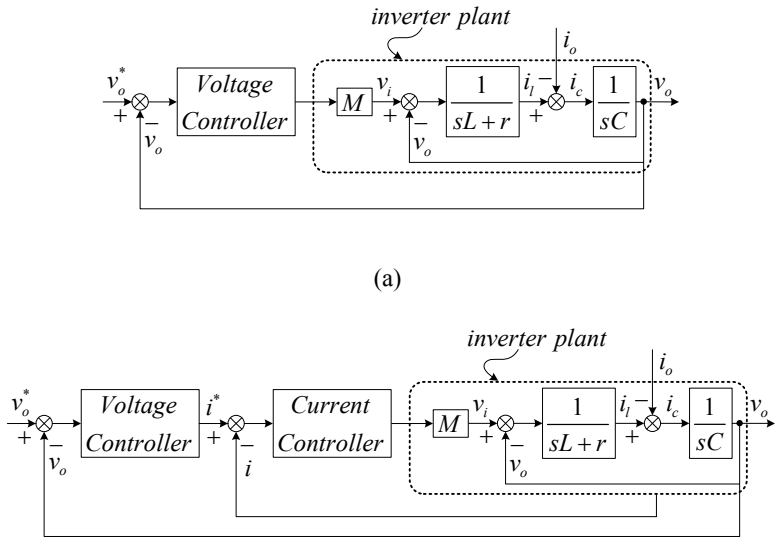
2.3.1 Control Techniques for Single-Phase UPS Inverter

It is clear from preceding discussions that multi-loop control topologies are better alternatives in terms of performance and robustness. The performance of overall control scheme further depends on efficacy of the applied controller. The present section discusses some of the widely used controllers in these multi-loop control schemes in detail.

2.3.1.1 Proportional Integral Controller

A conventional PI controller can be mathematically expressed by the transfer function as,

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{2.6}$$



(a)

(b)

Figure 2.4 Closed-loop instantaneous control of VSI (a) Single-loop and (b) Multiple-loop.

where K_p and K_i are the proportional and integral gains, respectively. The first term of (2.6) affects the entire spectrum equally with an all-pass gain factor K_p to the error signal. Whereas, the second term adds a pole or an infinite gain at the zero frequency, which may eliminate steady-state error for constant or slow varying signals.

The output voltage of the single feedback close-loop control can be derived from Figure 2.4(a) as,

$$v_o(s) = \frac{G_v(s)}{s^2LC + srC + 1 + G_v(s)} v_o^*(s) - \frac{sL + r}{s^2LC + srC + 1 + G_v(s)} i_o(s) \tag{2.7}$$

where v_o^* is the reference command voltage and G_v represents the voltage controller block. On substitution of PI control transfer function of (2.6) into voltage regulator G_v of (2.7), results in the following close-loop output voltage,

$$v_o(s) = G_{cl}^{PI}(s) v_i(s) - Z_{cl}^{PI}(s) i_o(s) \tag{2.8}$$

where, $G_{cl}^{PI}(s) = \frac{sK_p + K_i}{s\left(s^2LC + srC + 1 + K_p\right) + K_i}$ and $Z_{cl}^{PI}(s) = \frac{s(sL + r)}{s\left(s^2LC + srC + 1 + K_p\right) + K_i}$ are designated as the close-loop voltage gain and impedance of inverter, respectively using PI control. From (2.8), $G_{cl}^{PI}(s) = 1$ and $Z_{cl}^{PI}(s) = 0$ may be obtained, when the angular frequency of the reference v_o^* and the disturbance $i_o(s)$ are equal to zero Hz i.e., $s = \hat{i}\omega = 0$. Therefore, it is not possible for the PI controller to eliminate the steady state error for any other frequency

except the zero. That is to say, the output voltage cannot track perfectly an alternately varying reference signal. Although a very high integral gain, K_i may reduce the steady-state error, but simultaneous increase in closed-loop bandwidth and saturation of control signal puts a limit on it [37]. Another solution to achieve unit closed-loop gain for alternating signals is to transform AC signals in stationary frame into time-invariant signals in Synchronous Reference Frame (SRF) using Park's transformation. Therefore, PI regulator may then be employed for compensation in SRF with zero steady-state error. Synchronous Reference Frame Proportional Integral (SRF-PI) control is most widely used and established control approach in three-phase converter applications. However, in single-phase converter systems it is not the most frequently used controller. The major concern with the employment of PI in SRF for single-phase is the unavailability of second phase required for the Park transformation [38].

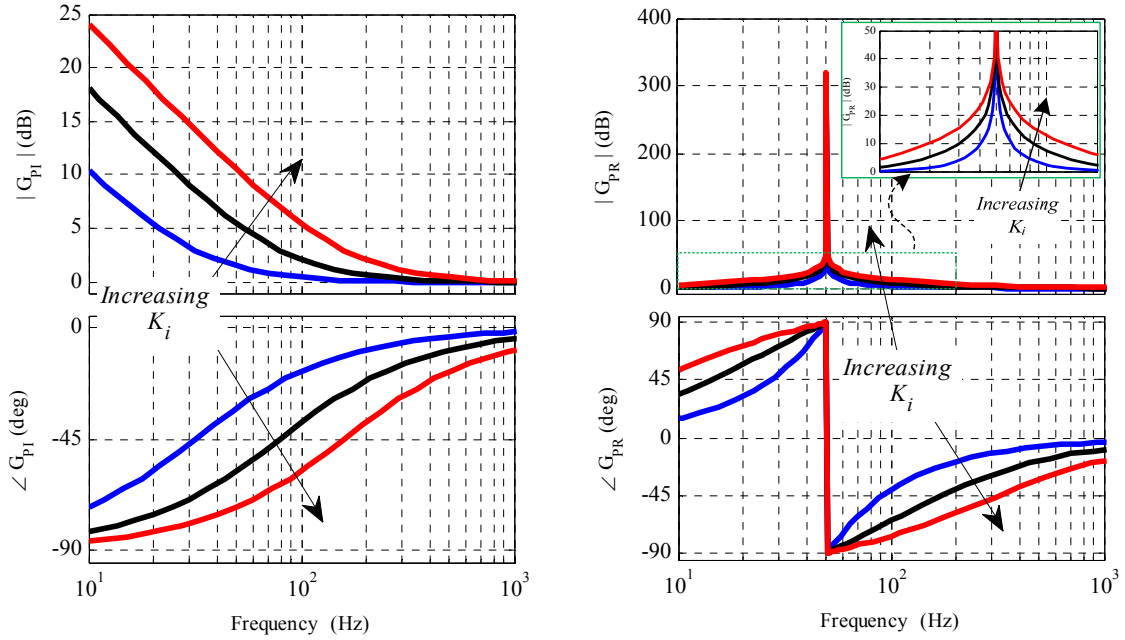
2.3.1.2 Proportional Resonant Controller

Proportional Resonant (PR) controllers have been known to possess superior tracking capability for periodic signals than the PI realised in stationary frame of reference. Basically, PR may be mathematically derived from the SRF-PI as demonstrated by Zmood and Holmes in [39], and can achieve virtually similar dynamic performance. However, the complexity and computational burden due to Park's transformation are far less than that of SRFPI. Moreover, PR can be directly applied to single-phase systems without the complexity of generating the second signal. The transfer function of an ideal PR controller can be written as in [39],

$$G_{PR}(s) = K_p + K_i \frac{2s}{s^2 + \omega_o^2} \tag{2.9}$$

Theoretically, PR compensator introduces an infinite gain at the fundamental frequency, ω_o of AC reference signal due to resonance phenomenon at that frequency. Henceforth, PR controller achieves zero steady-state error for time varying signals in stationary frame of reference. The role of K_p is same as that in PI control and it affects the entire frequency spectrum equally whereas, the resonant part of PR compensator, gives infinite gain at a single AC frequency ω_o, without disturbing the gain and phase at other frequencies.

On substitution of G_{PR} of (2.9) into the voltage regulator G_v of (2.7), closed-loop voltage gain and impedance gain transfer functions are obtained as:



(a) (b)

Figure 2.5 Bode-plot for (a) PI controller, G_{PI} and (b) PR controller, G_{PR} where $K_p = 1$; $K_i = 200$, 500 and 1000.

$$G_{cl}^{PR}(s) = \frac{\left(s^2+\omega_o^2\right)K_p + 2K_i s}{\left(s^2+\omega_o^2\right)\left(s^2LC + srC + 1 + K_p\right) + 2K_i s}$$

$$\text{and, } Z_{cl}^{PR}(s) = \frac{\left(s^2+\omega_o^2\right)(sL+r)}{\left(s^2+\omega_o^2\right)\left(s^2LC + srC + 1 + K_p\right) + 2K_i s} \qquad (2.10)$$

From (2.10), we can obtain the ideal condition of voltage following, i.e., $G_{cl}^{PR}(s) = 1$ and $Z_{cl}^{PR}(s) = 0$, if the reference v_o^* and the disturbance i_o are alternately varying at an angular frequency of ω_o (i.e., $s = \hat{i}\omega = 0$). Therefore, the regulated voltage perfectly tracks the reference voltage without any steady-state error.

Figure 2.5 shows the frequency response of both controllers i.e., for (a) PI and (b) PR. K_p value has been set to 1 and K_i is varied in three discrete steps of 200, 500 and 1000. Unit value of proportional gain, K_p has set the base of the Bode plot at 0 dB for both the controllers. An increase in integral value for PI controller, shown in Figure 2.5(a), enhances the gain at the operating frequency of 50 Hz, though the gain is finite only. This gain might not be sufficient to eliminate the steady state error. Further, increment in K_i may interfere with the switching noise and distort the output response. Moreover, as the integral value rises, larger phase lag gets induced, as seen from the phase plot in Figure 2.5(a). On the other hand, resonance action of the PR controller provides a very high gain at the fundamental frequency,

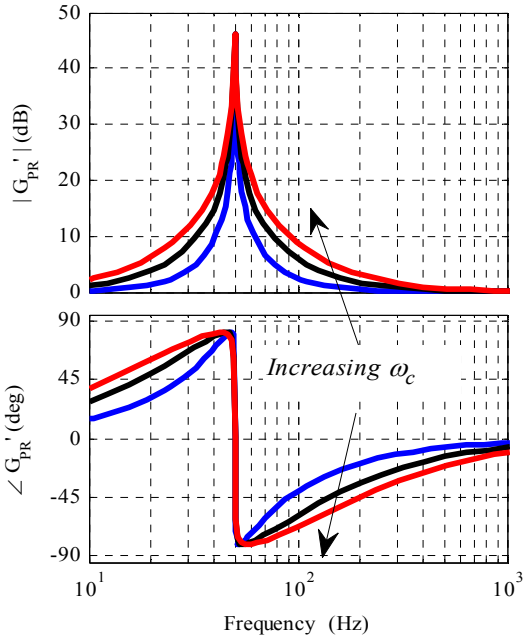


Figure 2.6 Bode-plot for non-ideal PR controller with ω_c variations (2, 5 & 7), where $K_p = 1$; $K_i = 200$.

which is not much dependent on the K_i value as shown in Figure 2.5(b). Besides, phase shifts are also zero at the fundamental frequency for all K_i gains. Magnified portion of the magnitude plot in Figure 2.5(b), shows widening of base of the resonant peak with increasing integral value, which affects other surrounding frequencies too.

Proportional resonant (PR) control is an attractive alternative for instantaneous control of AC signal systems in stationary frame. They show an excellent tracking with zero steady state error due to an infinite gain at the tuned ac frequency. In fact, PI is a special case of PR with a resonance frequency set to zero, which yields an infinite gain to the DC signal. For, other frequencies gain is finite only, even with high K_i values. However, full usability of the theoretical concept is not possible in digital implementation, especially in case of fixed point DSPs. Moreover, sensitivity towards frequency variation and exponentially decaying transient responses are also among the major drawbacks of such controllers [40].

An ideal PR controller is not realisable either in analog or digital form due to its infinite gain at resonance. Henceforth, a practical and implementable form of non-ideal PR, as given in [41], is generally used,

$$G_{PR}'(s) = K_p + K_i \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_o^2} \tag{2.11}$$

where ω_c refers to the cut-off frequency of the PR controller. Figure 2.6 shows the Bode plot for practical PR of (2.11) with the effect of ω_c variation. Although, the resonant peak of (2.9)

reduces to a finite gain but still, is sufficiently large for minimising steady state error to a negligible value at the tuned fundamental frequency. Larger ω_c reduces the sensitivity towards resonant frequency due to the increase in tuned frequency centred bandwidth. In the present design, the cut-off frequency has been taken as ω_c = 5 rad/s. Hereafter, wherever PR controller is used it refers to practical PR only, unless mentioned otherwise.

2.3.1.3 Synchronous Reference Frame of Control

For sinusoidal signal applications, such as in VSIs, stationary frame PI based regulators subject to steady state error due to continuously varying operating point. The Synchronous Reference Frame (SRF) transformation for such an alternating signal systems is widely used to obtain zero steady-state error. In the stationary frame of reference, alternating quantities may be represented in two-phase orthogonal '*α-β*'stationary coordinates. The SRF transformation translates the '*α-β*' stationary signals to the synchronously rotating '*d-q*' frame which rotates at an angular frequency of fundamental. This results in time-varying AC variables of stationary frame to get transformed into time-invariant DC entity in the synchronously rotating SRF at the fundamental frequency. Therefore, conventional PI regulator may now be applied to achieve zero steady-state error along each direct and quadrature components of the '*d-q*' frame.

Figure 2.7 depicts the projection of an arbitrary phase state-variable vector $\vec{a}$ in *α-β* stationary frame. $\vec{a}_\alpha$ and $\vec{a}_\beta$ are the components along the α and *β* axis, respectively of the stationary frame. The *d-q* frame rotates at an angular velocity of '*ω*' rad/s with respect to the *α-β* stationary frame. The angle between *α-β* frame and *d-q* frame at any instant may be defined as,

$$\theta = \int_0^t \omega(\tau)\, d\tau + \theta_0 \tag{2.12}$$

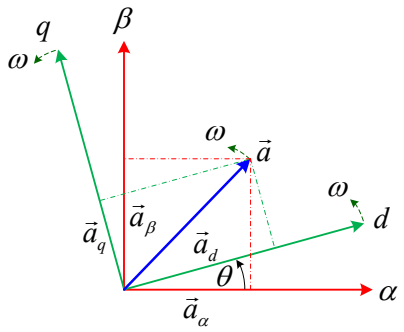


Figure 2.7 Vector representation in stationary and synchronous reference frame.

where 'θ_0' refers to the initial angle of the '*d-q*' reference system in radians and '*t*' refers to the time in seconds. Using trigonometric functions, the relation between stationary and rotating frame can derived from Figure 2.7 as,

$$\begin{bmatrix} \vec{a}_d \\ \vec{a}_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} \vec{a}_\alpha \\ \vec{a}_\beta \end{bmatrix} \tag{2.13}$$

$$\begin{bmatrix} \vec{a}_\alpha \\ \vec{a}_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} \vec{a}_d \\ \vec{a}_q \end{bmatrix} \tag{2.14}$$

The Park's transformation matrices for translating from stationary to rotating frame (*α-β→d-q*) and from rotating back to stationary frame (*d-q→α-β*) can be defined in (2.15) and (2.16), respectively as,

$$T_{\alpha-\beta\to d-q} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \tag{2.15}$$

$$T_{d-q\to\alpha-\beta} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \tag{2.16}$$

Note that, $T_{\alpha-\beta\to d-q} = T^{-1}_{d-q\to\alpha-\beta}$. In Figure 2.7, suppose there is a signal along *α*-axis as $\vec{a}_\alpha = A\cos(\omega t+\varphi)$ in *α-β* frame, where φ is the initial phase of the signal. Therefore, the orthogonal signal $\vec{a}_\beta$ would become, $\vec{a}_\beta = A\sin(\omega t+\varphi)$ along the *β*-axis. On substituting of $\vec{a}_\alpha$, $\vec{a}_\beta$ and $\omega t=\theta$ in (2.13) results in,

$$\begin{bmatrix} \vec{a}_d \\ \vec{a}_q \end{bmatrix} = \begin{bmatrix} A\cos(\theta+\varphi)\cos\theta + A\sin(\theta+\varphi)\sin\theta \\ -A\cos(\theta+\varphi)\sin\theta + A\sin(\theta+\varphi)\cos\theta \end{bmatrix} \tag{2.17}$$

$$\begin{bmatrix} \vec{a}_d \\ \vec{a}_q \end{bmatrix} = \begin{bmatrix} \frac{A}{2}\{\cos\varphi + \cos(2\theta+\varphi) + \cos\varphi - \cos(2\theta+\varphi)\} \\ \frac{A}{2}\{-\sin(2\theta+\varphi) + \sin\varphi + \sin(2\theta+\varphi) + \sin\varphi\} \end{bmatrix} = \begin{bmatrix} A\cos\varphi \\ A\sin\varphi \end{bmatrix} \tag{2.18}$$

From (2.18) it can be seen that $\vec{a}_d$ and $\vec{a}_q$ components are constant, which depends on the φ value. And when φ is zero, *d*-axis and *q*-axis components become $\vec{a}_d = A$ and $\vec{a}_q = 0$, respectively. Therefore, a rotating vector $\vec{a}$ in *α-β* stationary frame becomes a constant vector in *d-q* frame due to the synchronous rotation of the *d-q* reference plane itself. This transformation thus allows the PI regulators to be implemented, as on DC signals, so as to provide an infinite gain to achieve the zero steady-state error.

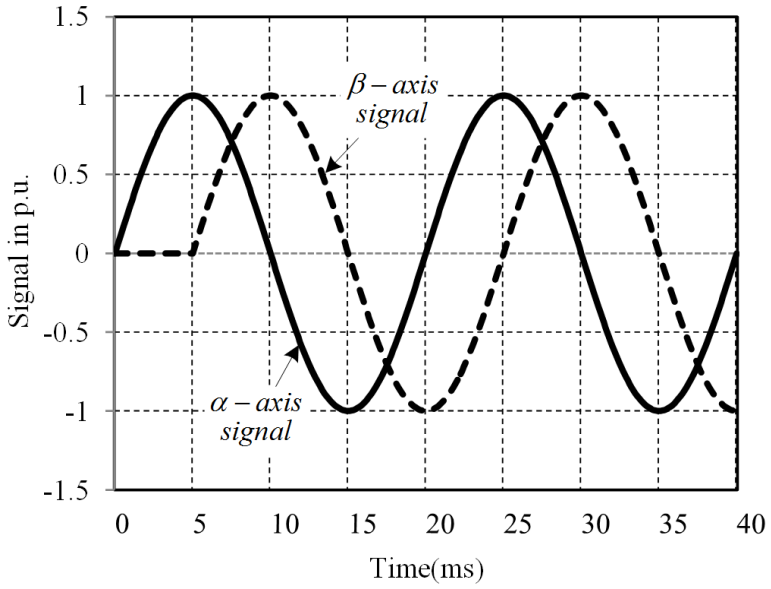


Figure 2.8 Generation of virtual β-axis orthogonal signal from α-axis signal.

2.3.1.4 Orthogonal Signal Generation Technique

SRF regulators are well established and widely used technique in the control of three-phase AC system. However, the same approach cannot be applied directly to the single-phase due to the absence of an orthogonal β-axis variable. In literature, several research papers have proposed Orthogonal Signal Generation (OSG) techniques to generate the β-axis orthogonal component from the original signal. Mainly there are two methods of realisation: (i) in time domain and (ii) in frequency domain. The simplest is time domain realisation, wherein an α-axis signal is delayed by a quarter cycle (90° electrical angle) to obtain the orthogonal signal, as shown in Figure 2.8 [42]–[46]. Although, easy to implement but lacks in fast transient response due to delay in reconstruction of β-axis component.

Table 2.2 Orthogonal signal generators

Orthogonal Signal Generators	**Transfer Function**
Differentiator	$OSG_D(s) = -\frac{s}{\omega_o}$
Second Order Generalised Integrator **(SOGI)**	$OSG_{SOGI}(s) = \frac{k\omega_o^2}{s^2 + k\omega_o s + \omega_o^2}$
All Pass Filter **(APF)**	$OSG_{APF}(s) = -\frac{s-\omega_o}{s+\omega_o}$

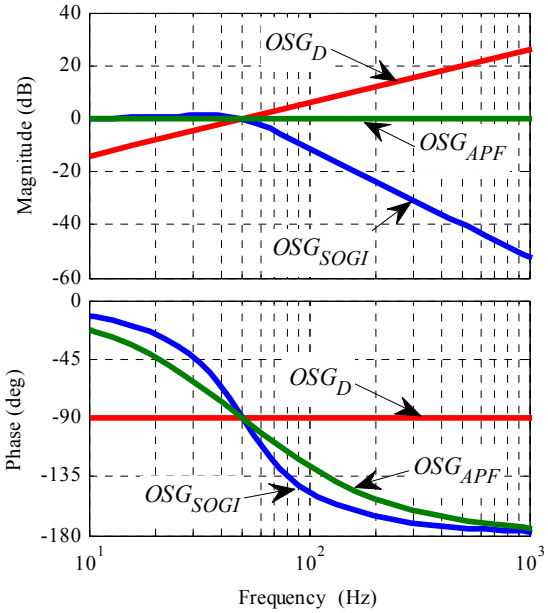


Figure 2.9 Bode-plot for transfer characteristics of orthogonal signal generators.

A frequency domain method to obtain orthogonal signal is, to differentiate the original single-phase ac signal [47]. However, due to noise amplification at high frequencies, it is difficult to implement. Another frequency domain approach is the Second Order Generalised Integrator (SOGI) method suggested in [48]. SOGI method allows only fundamental component and attenuates other harmonics or noise. Hence, the controller has no rejection ability on these harmonic components. All Pass Filter (APF) is a frequency domain method of OSG technique which provides a unity gain and a phase delay of 90° to the α-axis signal without attenuating high frequency components [49]. The transfer function gain of frequency domain OSGs have been summarised in Table 2.2. The corresponding Bode frequency response plots in Figure 2.9 show the capabilities and limitations of OSGs.

2.3.2 Alternate Control Options for Single-Phase UPS Inverters

Apart from these conventional multi-loop linear control techniques, several non-linear and periodic control strategies are also in use for single-phase UPS inverters [26], [27], [32], [50], [51]. Multi-loop control schemes are generally model based control techniques i.e., their design and performance heavily depend on inverter modelling [50]. Other model based instantaneous control options are deadbeat and model predictive control, which fall in the conglomeration of predictive control. In order to achieve better performance and robustness against parameter variations and disturbance rejection, non-linear control techniques have been attempted in several papers [52]–[56]. Further, cyclic/repetitive nature of command

voltage and load current, learning based periodic controllers have been found to be attractive options for UPS inverter control in [57], [58]. A brief review of the predictive, non-linear and periodic control has been presented herewith.

2.3.2.1 Predictive Control

Predictive control is relatively a recent class of controllers attracting more attention with the development of powerful and fast processors [59]. Such a control technique predicts the forthcoming behaviour of the control variable on the basis of the present error and the system model. Wide variations of the predictive control are available according to the control optimisation criteria [60], [61].

- *Deadbeat Control*

Deadbeat controller has been in utilisation for UPS applications since 1980s [62], [63]. This is a type of predictive control, which uses the system model to calculate the control command in each sampling period so that the reference value is achieved in the next sampling instant. That is the output voltage at n^{th} instant, $v_o(n)$ lags the reference voltage $v_o(n+1)$ by an one sample interval. The closed-loop transfer function of the deadbeat controlled system is z^{-1} in discrete domain, which gives deadbeat controller, $G_{DB}(z)$ transfer function as

$$G_{DB}(z) = \frac{1}{P(z)} \frac{1}{(z-1)} \tag{2.19}$$

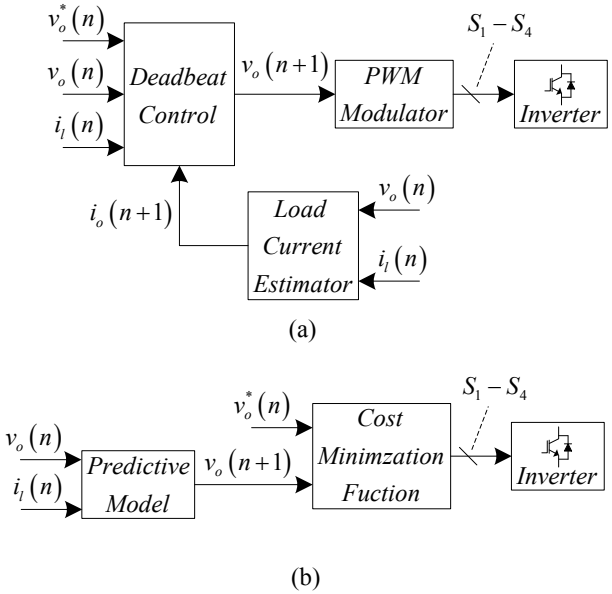


Figure 2.10 Predictive control (a) Deadbeat control and (b) Model predictive control.

where P(z) is the plant transfer function. Figure 2.10(a) displays a typical block schematic of the Deadbeat Control scheme. Output voltage of the next sample $v_o(n+1)$ is predicted using reference voltage $v_o^*(n)$, measured output $v_o(n)$ and filter inductor current $i_l(n)$ of the present sample. An estimate of the unmeasured load current $i_o(n+1)$ is obtained from the load current estimator using $v_o(n)$ and $i_l(n)$. The prime focal point of the Deadbeat controller is its ability to reduce the error to zero in finite number of sampling steps, in fact it gives the fastest dynamic response for digital implementation [64]. The main drawback of this controller is its sensitiveness towards plant modelling error, noise on the sensed variable, computational delays and other unmodelled parameters, which often deteriorates the system performance. Various efforts to improve the performance have been presented, subsequently. Most of them have used either extra sensor or observer to compensate the computation delay, real time parameter estimation to compensate parametric mismatch and disturbances [65]–[69] .

- *Model Predictive Control*

Another approach of prediction control is the Model Predictive Control (MPC) which uses system model and a more flexible criterion to minimise the error with the help of some optimised cost function. Further for predictions, it considers not only the next cycle but up to a specified horizon of time and thus also named as receding-horizon control [60].

Several research papers have discussed the MPC developed for UPS inverters [70]–[77]. It can be implemented as continuous control set using a modulator with fixed switching frequency or with finite control sets having variable switching frequency [61]. In addition, inclusion of different constraints on variables and modelling non-linearities are relatively straight forward in MPC. MPC generally controls the future behaviour of the system by optimising a Cost Minimizing Function (CMF) in every sampling period, repeatedly. One of the many flexible CMFs has following form,

$$CMF = \sum_h \lambda_h \left(x_h^* - x_h^{pre} \right)^2 \tag{2.20}$$

where 'h' is number of control variables, λ_h stands for weighting factor and x_h^* and x_h^{pre} are reference and predicted values for control variable 'x'. In general, different formulations of cost function are possible considering several variables, weighting factors [61]. Figure 2.10(b) shows a MPC applied to the UPS inverter. Here, next sample of the output voltage $v_o(n+1)$ is predicted using the present sample of measured output voltage $v_o(n)$ and filter inductor current $i_l(n)$. The optimal inverter control voltage is applied which results in the minimal cost

function for $v_o(n+1)$. The switching state of the optimal control voltage is saved and applied at the next sampling instant.

Summarily, predictive control may be considered as a strong contender to the conventional PID based controllers due to their simplicity. Predictive controls are easily comprehensible for the complex multi-variable and multi-objective systems. Moreover, constraints and non-linearities can be easily incorporated in the design. However, high amount of calculations require fast processors. Besides, being a model based control scheme, the technique requires reasonable knowledge of system parameters for good quality performance.

2.3.2.2 Non-Linear Control

Inverters being truly a non-linear system with nonlinearities, such as dead time and switching delays, non-linear controllers may be more appropriate for its regulation. Generally, non-linear controllers show better system performance and robustness against uncertainties. However, the design and implementation is quite complicated. The non-linear controllers include Hysteresis Control, Sliding Mode Control (SMC), Neural Networks (NN) Control, Fuzzy Logic (FL) Control, etc. [78], [79].

- *Hysteresis Control*

Hysteresis regulator is one of the simplest and widely used techniques for inverter control. The output of the hysteresis controller toggles between logic zero and one, in order to reduce the voltage error. Therefore, it can directly generate switching signals for the inverter and does not require a modulator, however it also results in widely variable switching frequencies. Generally, a hysteresis band is defined with an upper and lower boundary level of the reference voltage. When inverter positive output hits the upper limit of the reference voltage, a switching state for negative output voltage is applied and vice-versa. Thus, the inverter has only two possible voltage levels i.e., $\pm V_{dc}$. On other side, this leads to a faster transient response with maximum control effort on each switching instant [14], [80].

- *Sliding Mode Control*

Sliding Mode Control (SMC) , also known as Variable Structure System, has been popular for non-linear systems since its inception in late 1950's [81]. According to the SMC theory, a specified surface is defined in state space and the entire control effort is to drive the state trajectory of the plant onto that surface. The structure of the system is changed discontinuously to slide along the switching surface, which resembles switching nature of the

power electronics converters. Therefore, unbounded implementation of SMC implies high-frequency switching [55]. However, this gives insensitivity against uncertainties of the nonlinear system. A discrete SMC scheme for closed-loop control of PWM inverter in applications of UPS under load variations has been introduced in [55]. A feedforward discrete SMC scheme for UPS inverters has been proposed to achieve zero steady-state error with reduced sensors and low sampling rate in [82]. Later, variants of sliding mode controllers using dual-loop[83], variable switching surface [84], three-level sliding function [85] and fixed switching frequency SMC [86] have also been presented for single-phase inverters.

In a typical SMC implementation [86], state variables 'x_h' are sensed and a sliding function or surface ψ is defined using error from the state reference 'x_h^*' as,

$$\psi\left(x_h\right)=\left(\frac{d}{dt}+\rho\right)^{b-1}\left(x_h^*-x_h\right)=0 \tag{2.21}$$

where, 'b' refers to the system order ($b\neq1$) and 'ρ' is a positive SMC constant. Using a suitable control law, signum function is utilised to keep the sliding function ψ zero and hence track the sliding surface. However, finding an appropriate sliding surface is not always simple. Moreover, SMCs also suffer from the problem of chattering, which may lead to variable and high switching frequency.

- *Fuzzy Logic Control*

Fuzzy Logic also belongs to the class of non-linear controllers [79], [87]–[89]. FL based vague, qualitative or multi-valued control is very much suitable for real world non-linear systems or processes whose analysis by conventional quantitative techniques is either too complex, inexact or uncertain. It can convert the linguistic control based on expert knowledge into an automatic control strategy, which would be much closer to human thinking and decisions. The adaptive nature of fuzzy control has been also utilised in power electronic systems with large parameter variations [90]. In [33], the application of fuzzy theory to closed-loop regulation of a PWM inverter for UPS systems with large load variations has been presented. Further, UPS performance with improved FL control has been investigated in [54], [91] even for non-linear loading conditions. Later, FL combined with other control schemes such as predictive control, PI control, SMC, etc., have also been explored in series of literatures [92]–[96].

Interconnection of multi-inverters in parallel modifies the plant characteristics for the controller. Further, non-linearity such as dead time, different switching instants of modules, unknown parameters makes modelling by deterministic equations difficult. These factors

however, can be fairly dealt with FL controllers designed on expert's intuition and experience. Compared to other non-linear control methodologies, FL are relatively easier to understand and simple to implement while maintaining comparable performance. Hence, Fuzzy based methods for parallel-connected UPS inverters have been investigated in Chapter 5 with the objective to achieve better robust performance on wide variations of parameters.

2.3.2.3 Periodic Control

Reference voltage and load current of an UPS inverter system are periodic in nature and repeat cyclically at fundamental frequency. Therefore, periodic control schemes such as Repetitive Control (RC) and Iterative Learning (IL) control are very much suitable in such systems, which perform the same task over and again. These periodic techniques are also known as learning control schemes, since they use the previous repetition information to improve the tracking accuracy of the present repetition. Henceforth, a learning behaviour is demonstrated by the control action working repeatedly on the system to reduce the tracking error in subsequent repetitions or trials. Since data storage is needed, it is more suitable for digital implementation.

- *Repetitive Control*

Repetitive Control (RC) technique has been widely used for the rejection of cyclic fluctuating disturbances in power electronics converter systems [57], [58], [97]–[101]. RC is a special case of internal modal principle for periodic signals. The internal model principle states that the perfect tracking or rejection can be achieved if an accurate model of the reference or disturbance signal is included in the stable closed-loop system [102].

The basic configuration of a typical RC based system is shown in Figure 2.11 in discrete-time domain. $G_p(z)$ is the plant model to be controlled such as, an UPS inverter. $y^*(z)$, $y(z)$ and $e(z)$ are the reference command, output response and the tracking error, respectively. All repetitive disturbances represented by $d(z)$ is added at the system output. Assuming 'p' is to

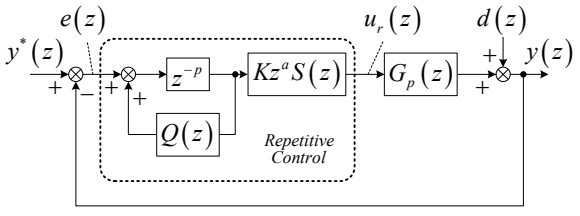


Figure 2.11 Block schematic of a typical repetitive control system.

be the number of sampling instants in each fundamental cycle, 'z^{-p}' introduces a fundamental cycle delay, which is the core of the RC control strategy. $Q(z)$ designates a filter generally included for enhanced system stability but not without a non-zero steady-state error. Often, $Q(z)$ is selected as a low pass filter or simply a unity gain for the ease of implementation. The compensator $S(z)$ is included for shaping of the plant $G_p(z)$ frequency characteristics, for better harmonic rejection. 'z^{a}' is a time advancement unit which advances the control action so as to compensate the aggregate phase delays due to $S(z)$ and $G_p(z)$. 'K' is a constant which determines the speed of error convergence.

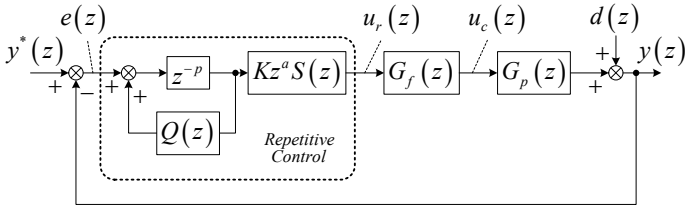
From Figure 2.11, the tracking error 'e' can be derived as,

$$e(z)=\frac{1-z^{-p}Q(z)}{1-z^{-p}\left\{Q(z)-Kz^{a}S(z)G_p(z)\right\}}y^{*}(z)+\frac{z^{-p}Q(z)-1}{1-z^{-p}\left\{Q(z)-Kz^{a}S(z)G_p(z)\right\}}d(z) \quad (2.22)$$

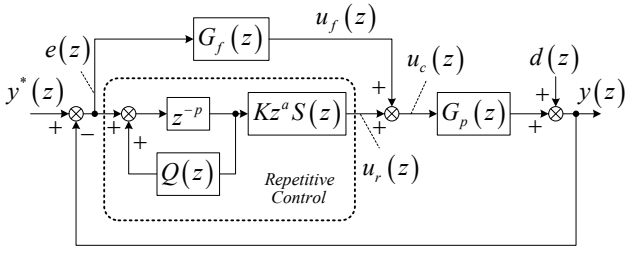
A sufficient condition for system stability is expressed in [57], for which the tracking error is convergent:

$$\left|Q(z)-Kz^{a}S(z)G_p(z)\right|_{z=e^{j\omega T}}<1, \quad \forall\ 0<\omega\le\pi/T \quad (2.23)$$

where T_s is the sample time. In other words, when ω increases from zero to the Nyquist frequency, as long as (2.23) is satisfied, the repetitive control system is asymptotically stable and tracking error decays on successive repetitions.



(a)



(b)

Figure 2.12 Repetitive control using fast controller (a) Cascaded structure and (b) Parallel structure.

However, dynamic response of the stand-alone repetitive control is not satisfactory due to fundamental frequency one cycle delay between input and output. Henceforth, a RC is usually implemented with some fast controller 'G_f' such as deadbeat, to achieve high performance under both steady state and transient conditions. Two possible configurations are possible as shown as in Figure 2.12, when RC is combined with other control strategies namely, cascaded and parallel. The main purpose of the fast controller is to improve the system transient response while the repetitive controller is designed to reduce periodic errors caused by periodic references or disturbances. Parallel structure offers a better compensation for sudden changes because the fast controller is able to operate independently irrespective of the slower RC control action [103].

Therefore, repetitive controller combined other fast controllers is a good control option for inverters of high-performance UPS applications. Moreover, this it achieves with a single voltage sensor [57], [97]. The large memory requirement is the fact, which goes against its frequent application.

- *Iterative Learning Control*

Iterative Learning control is another learning based control scheme, which has been receiving increasing attention from researchers recently [104]. The control strategy is similar to that of RC, except resetting of initial conditions in IL control. RC is typically applied to continuous process whereas IL divides the continuous process into several batches, which repetitively performs a given task over a period of time (called a batch or trial) [105]. Similar to RC, IL deals with the periodic command and disturbances. Application of IL control on UPS inverters has been presented in [106], [107]. As compared to RC, IL control is easier to comprehend in time-domain while achieving similar performance [108].

Therefore, an IL based hybrid control scheme has been presented first for an unit UPS inverter and later for multi-inverter modules to enhance power level of UPS system in Chapter 6, where IL control is has been discussed in more detail.

2.4 Multi-Modular UPS Inverters System

Ever increasing demand of arbitrary load can be fulfilled by using a modular approach of paralleling UPS inverters. The challenge of parallel-connected UPS inverters system is not only to maintain a specified voltage and frequency, but also to ensure the proper sharing of total load current among the inverters. In general, control schemes are categorised into two groups: (a) Droop Control and (b) Active Load Current Sharing Control. The details of the same are discussed in the following sub-sections.

2.4.1 Droop Control Method

The droop control method (also known as communication-less or independent method) is for inverters connected in parallel without any communication or information sharing in-between. This provides a greater reliability and flexibility of physical placement of the inverter system. Droop control is a well-established concept used in large-scale power system grid, which droops the frequency of the ac-generator due to its inertia when output power increases. In a similar manner, UPS inverters can regulate voltage amplitude and frequency independently, according to the output power demand. For this, inverters sense only local voltage and current for the active and reactive power calculations to adjust the frequency and amplitude of the reference voltage. The droop control is a load sharing technique primarily based on power flow theory in AC systems, which is discussed as follow.

2.4.1.1 Power Flow Theory

The theory related to power flow in an AC system may be explained as in [109]–[114]. Figure 2.13 depicts a system with several UPS inverters connected in parallel supplying a load through a common AC load bus. $V_o\angle 0$ refers to the common AC load bus voltage, $V_{oj}\angle\delta_j$ is the Thevenin's equivalent open circuit voltage, I_{oj} is the output current and $Z_{lj}\angle\phi_j$ is the line impedance that connects the output of the j^{th} inverter to the load. The line impedance is highly inductive which is due to predominately inductive nature of the inverter's *LC* filter impedance and line impedance. The complex power supplied by the j^{th} inverter to the load may be expressed as,

$$S_j = P_j + \hat{i}Q_j = V_o I_{oj}^* \tag{2.24}$$

where, $\hat{i}$ is imaginary operator, P_j and Q_j refer to active and reactive power of the j^{th} inverter and I_{oj}^* denotes the complex conjugate of the j^{th} inverter current which can be expressed as,

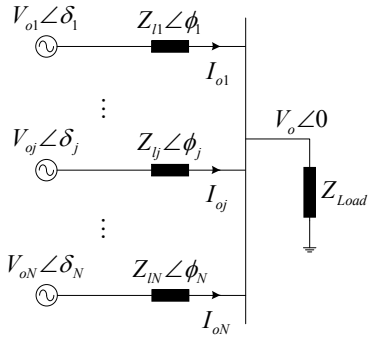


Figure 2.13 Equivalent circuit of UPS inverters system connected in parallel to a common load.

$$I_{oj}^{*} = \frac{V_{oj}\angle\delta_j - V_o}{Z_{lj}\angle\phi_j} \tag{2.25}$$

Therefore, substituting (2.25) in (2.24)

$$\begin{aligned} S_j = V_o I_{oj}^{*} &= V_o \left\{ \frac{V_{oj}\angle -\delta_j - V_o}{Z_{lj}\angle -\phi_j} \right\} \\ &= \frac{V_o V_{oj}\angle\left(\phi_j - \delta_j\right)}{Z_{lj}} - \frac{V_o^2\angle\phi_j}{Z_{lj}} \end{aligned} \tag{2.26}$$

This gives the active and reactive power flowing from the j^{th} inverter as,

$$P_j = \frac{V_o V_{oj}\cos\left(\phi_j - \delta_j\right) - V_o^2\cos\phi_j}{Z_{lj}} \tag{2.27}$$

$$\text{and, } Q_j = \frac{V_o V_{oj}\sin\left(\phi_j - \delta_j\right) - V_o^2\sin\phi_j}{Z_{lj}} \tag{2.28}$$

It can be seen that the line impedance Z_{lj} has an impact on the active or reactive power components of the inverter. As a consequence, the power flow control strategy also depends on the line impedance, which is therefore investigated for two extremes of the Z_{lj}, i.e., purely inductive and purely resistive for further analysis.

2.4.1.2 Inductive Line Impedances, $Z_l = \hat{i}X$

Traditionally, the line impedance is primarily inductive (i.e., $Z_l = \hat{i}X$ and ϕ =90°), which may be assumed due to the inductive nature of both output filter and connecting wire impedance [109], [115]. If that is the case, following expressions of active and reactive powers can be derived from (2.27) and (2.28) and with a simplified assumption of small phase difference δ_j between V_o and V_{oj} ($\sin\delta_j \approx \delta_j$ and $\cos\delta_j \approx 1$),

$$P_j\Big|_{Z_l=\hat{i}X} = \frac{V_o V_{oj}\sin\delta_j}{X_j} \approx \frac{V_o V_{oj}}{X_j}\delta_j \tag{2.29}$$

$$\text{and, } Q_j\Big|_{Z=\hat{i}X} = \frac{V_o V_{oj}\cos\delta_j - V_o^2}{X_j} \approx \frac{V_o\left(V_{oj} - V_o\right)}{X_j} \tag{2.30}$$

Simplified assumptions reveal that the active power P_j is heavily dependent on the phase difference δ_j whereas, the reactive power Q_j is predominantly influenced by the amplitude difference ($V_{oj} - V_o$).

2.4.1.3 Droop Concept

Unlike traditional synchronous generator power plants, static power inverters do not present the inherent operating characteristics of natural coupling, neither between frequency and active power output nor between output voltage and reactive output power [109], [111], [116]–[135]. Therefore, in order to reproduce the dynamics of AC generators, the controllers of the inverter introduce artificial droop characteristics in their reference voltage. The simplest form of droop control law feeding the grid may be expressed as in [115] by,

$$\omega_j = \omega^* - m_j\left(P_j - P^*\right) \tag{2.31}$$

$$\text{and, } V_{oj} = V_o^* - n_j\left(Q_j - Q^*\right) \tag{2.32}$$

where ω^* and V_o^* refer to the nominal output-voltage frequency and amplitude, respectively on no-load. Figure 2.14 shows the block schematic of the droop control for parallel-connected inverters. P_j and Q_j are the measured active and reactive power outputs and m_j and n_j are the frequency and amplitude droop coefficients, respectively of the j^{th} inverter module. P^* and Q^* are the reference active and reactive power, respectively and are kept zero (i.e., $P^* = Q^* = 0$) for grid-isolated parallel connected inverters. Note that, although (2.29) shows a relation of δ_j

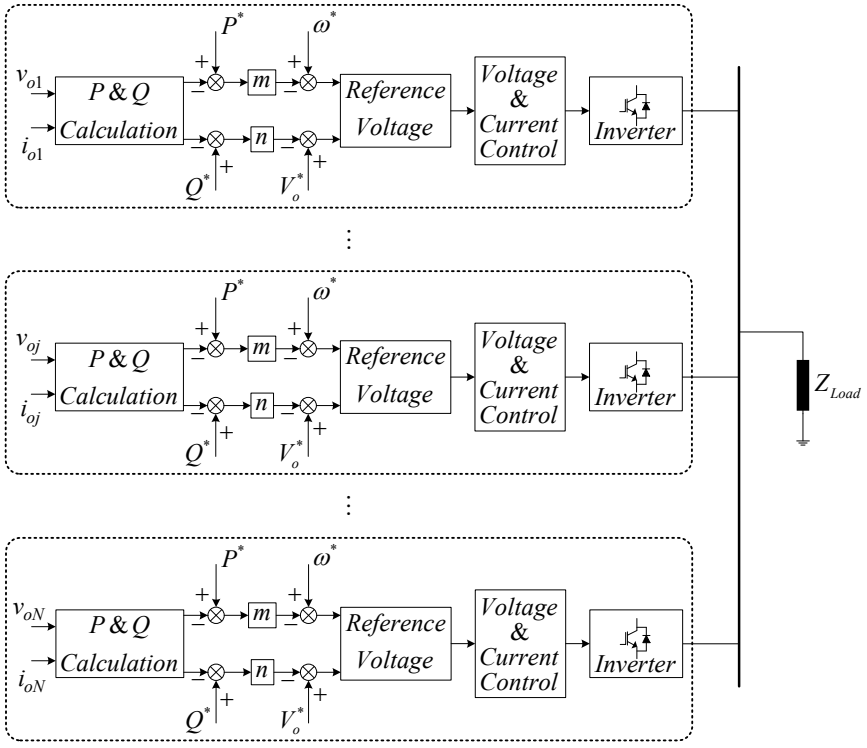


Figure 2.14 Block schematic of droop control for parallel-connected inverters in an UPS system.

with P_j, (2.31) incorporates ω_j in the droop control law. This is due to the fact that the initial voltage phases are unknown to the inverter modules and since frequencies are dynamically related to phases, can be easily set as ω^* for all inverters in parallel.

The droop coefficients 'm_j' and 'n_j' can be designed using (2.31) and (2.32) from the following

$$m_j = \frac{\omega^* - \omega_j}{P_{j\max}} = \frac{\Delta\omega}{P_{j\max}} \tag{2.33}$$

$$\text{and, } n_j = \frac{V_o^* - V_{oj}}{2Q_{j\max}} = \frac{\Delta V_o}{2Q_{j\max}} \tag{2.34}$$

where $\Delta\omega$ and ΔV_o are the maximum acceptable frequency and amplitude deviations, respectively and P_{jmax} and Q_{jmax} are the maximum active and reactive power ratings, respectively of the j^{th} inverter.

The proportionate load sharing by inverters of different ratings connected in parallel may be adjusted by selecting the droop coefficients according to the following relation:

$$m_1 S_1 = m_2 S_2 = \cdots = m_N S_N \tag{2.35}$$

$$\text{and, } n_1 S_1 = n_2 S_2 = \cdots = n_N S_N \tag{2.36}$$

where S_j is the apparent power delivered by the j^{th} UPS module.

The trade-off in droop control approach is in between power sharing accuracy and output voltage regulation. Good power sharing may be achieved if the droop coefficients are

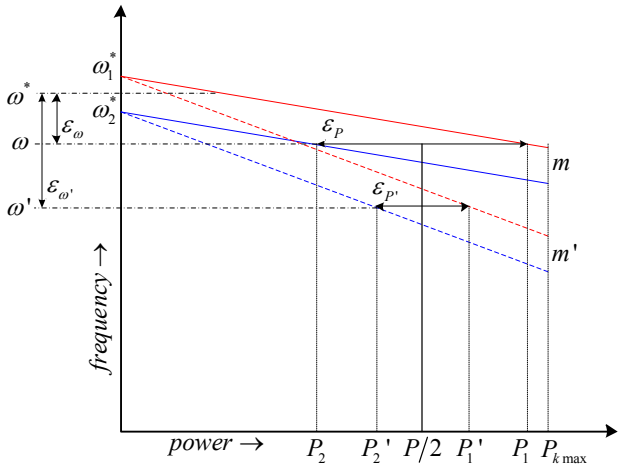


Figure 2.15 Frequency versus active power of two inverters connected in parallel.

increased but that can be realised at the expense of high deviations in frequency and voltage from the nominal values. Figure 2.15 illustrates tradeoff between active power sharing and frequency deviation in the P–ω droop characteristics plot. With a higher droop coefficient (m' > m), power sharing error decreases ($\varepsilon_{P'} < \varepsilon_P$) but at cost of higher deviation in frequency ($\varepsilon_{\omega'} > \varepsilon_\omega$).

2.4.1.4 Resistive Line Impedances, $Z_l = R$

Usually the line impedance is considered to be inductive, however this is not always true, since the closed-loop output impedance also depends on the control strategy and the line impedance (which is predominantly resistive for low voltage cabling). When the line impedance of inverters are considered resistive (i.e., $Z_j = R_j$ and $\phi_j = 0°$), the active and reactive powers in (2.27) and(2.28) becomes

$$P_j\Big|_{Z=R} = \frac{V_o V_{oj}\cos\delta_j - V_o^2}{R_j} \approx \frac{V_o\left(V_{oj} - V_o\right)}{R_j} \tag{2.37}$$

$$\text{and, } Q_j\Big|_{Z=R} = -\frac{V_o V_{oj}\sin\delta_j}{R_j} \approx -\frac{V_o V_{oj}}{R_j}\delta_j \tag{2.38}$$

Hence, when the line impedance is highly resistive, the droop equations exchange their role,

$$\omega_j = \omega^* + m_j\left(Q_j - Q^*\right) \tag{2.39}$$

$$\text{and, } V_{oj} = V_o^* - n_j\left(P_j - P^*\right) \tag{2.40}$$

where $m_j = \Delta\omega/2Q_{j\max}$ and $n_j = \Delta V_o/P_{j\max}$. Consequently, a control scheme based on the P-ω and Q-V droops should be used for the net inductive line impedance while for effective resistive impedance, P-V and Q-ω droops have to be opted for.

Droop control performance is therefore particularly sensitive to the line impedance. For this reason, it is important to design the output impedance properly in order to improve decoupling between active and reactive power and to avoid the line impedance impact over power sharing [114]. Another alternative may be an interface inductor between the inverter and the load bus for fixing the line impedance however, they are heavy and bulky in nature henceforth, not economically advisable.

The sinusoidal reference for the voltage loop of each inverter is obtained from the reference voltage block using the amplitude and the frequency defined by power droop characteristics. Active power and reactive power are obtained using information available locally at inverter module terminal i.e., voltage, current, and frequency. The droop method

exhibits a slow dynamic response, since it generates reference of a smaller bandwidth than that of the closed-loop inverter for the stability purpose [124], [129], [130], [136]–[139]. This works well for linear loads but it will not help to share the distortion component caused by non-linear loads, since the amount of distorted power demanded by the nonlinear loads is not taken into account. [109], [140] suggested a controller to share non-linear loads by adjusting the output voltage bandwidth with the delivered harmonic power. However, the technique has two main limitations: the controller uses an algorithm, which is too complicated to calculate the harmonic current content, and the harmonic current sharing is achieved at the expense of reducing the stability of the system. In another approach, every single term of the harmonic current is used to produce a proportional droop in the corresponding harmonic voltage term, which is added to the output-voltage reference[110], [141].

Thus, the Droop method has following limitations: 1) tradeoff between the power sharing accuracy and the output voltage regulation, 2) power sharing accuracy is strongly affected by the line impedance characteristics, and 3) harmonic power in case of supplying nonlinear loads is poorly shared [112], [114], [127], [142]–[148].

2.4.2 Active Load Current Sharing Techniques

In order to achieve good voltage regulation and proper current sharing some information needs to be shared amongst inverters connected in parallel. A second approach of load sharing is the Active Load Current Sharing (ALCS) technique which uses a communication link for load current information of inverter modules for its suitable operation. Depending on how the current information is shared, reported ALCS techniques may be classified into four categories: (a) Centralised control, (b) Master-Slave (M-S) control, (c) Current Chain Control or 3C control, and (d) Instantaneous Average Current Sharing (IACS) control [18], [23], [144], [145], [149]–[154].

2.4.2.1 Centralised Control

Figure 2.16 shows a block schematic of centralised control strategy for parallel-connected UPS inverters system. In such a scheme, a common outer-voltage control loop regulates the system output voltage of the UPS. The reference for inner-current controller is obtained by adding the voltage controller output and the average load current [23], [155], [156]. The average current of the system is obtained from the total load current by dividing it with the number of parallel-connected modules '*N*',

$$i_{oj}^{*} = \frac{i_o}{N}, \ \forall j = 1, 2, \ldots, N \tag{2.41}$$

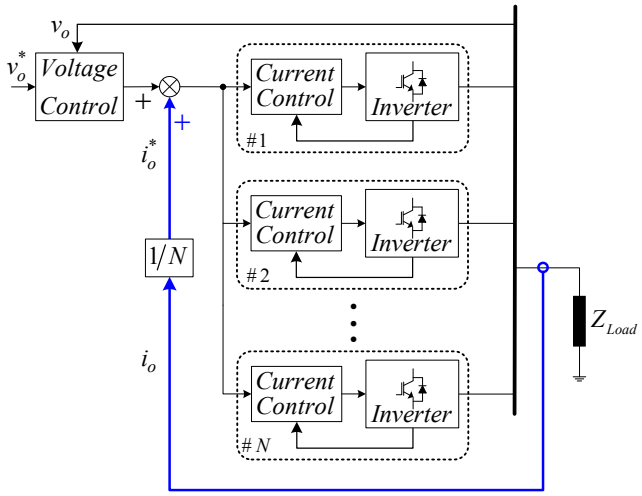


Figure 2.16 Block schematic of centralised control strategy for parallel UPS inverters system.

UPS inverters from the same manufacturer and batch generally have similar characteristics, i.e. in terms of nominal power, output impedance and closed-loop dynamic response [157], [158]. Therefore, with a common voltage control loop and a common current reference for all inverters, good performance may be possible on parallel operation of such inverters. Since, a centralised control board is required for common reference generation, such a configuration is more suitable in UPS system with parallel inverters inside the same equipment. However, since no inverter is allowed to operate as an independent unit, this configuration results in an inadequate redundancy [126], [136].

2.4.2.2 Master-Slave Control

In this ALCS technique, the Master inverter regulates the overall voltage of the UPS system and the output current of the Master module acts as the reference command for other modules referred to as Slave inverters. Slave inverters are controlled to track the reference current [159]–[170]. In this way, the Master operates as a voltage source while the Slave inverters operate as current source. The reference current for the slave modules is the output current of the Master module, here it is the first module #1 of Figure 2.17,

$$i_{oj}^* = i_{oM} = i_{o1}, \ \forall\, j = 2,3,\ldots,N \tag{2.42}$$

The Master module may be a dedicated one or rotary one (arbitrarily) chosen from the parallel-connected inverters system. If the Master module is rotarily chosen, all modules of the UPS system have voltage and current control loops. In case the master unit fails, another module will take the role of master thereby, a higher reliability can be guaranteed. This

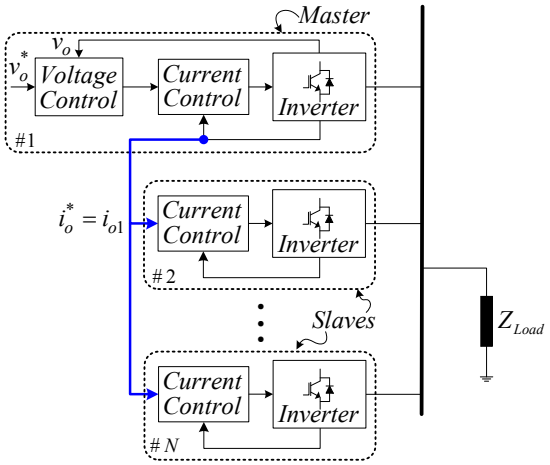


Figure 2.17 Block schematic of Master-Slave (MS) control for parallel-connected UPS inverters system.

system is often adopted when using different UPS units mounted into a rack. It is easy to implement and expand the system capacity because of its modularity.

2.4.2.3 Circular Chain Control (3C)

Circular-Chain-Control (3C) for inverter parallel operation as shown in Figure 2.18 has been presented in [166], [171]. To minimise interconnections, successive modules are connected one by one to make a circular arrangement. The current reference of each inverter module is obtained from the current of the previous inverter module, whereas the current reference of the first inverter is obtained from the current of the last module.

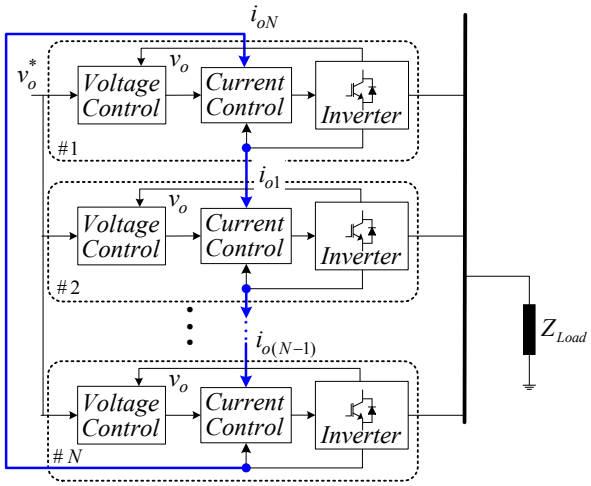


Figure 2.18 Block schematic of Circular Chain Control (3C) for parallel-connected UPS inverters system.

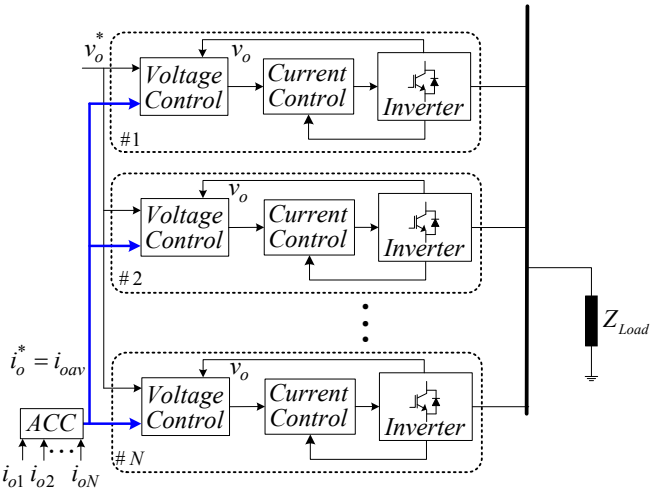


Figure 2.19 Block schematic of Instantaneous Average Current Sharing (IACS) control for parallel-connected UPS inverters system.

$$i_{o1}^* = i_{oN}$$
$$\text{and} \quad i_{oj}^* = i_{o(j-1)}, \ \forall j = 2,\ldots,N \tag{2.43}$$

All modules of the 3C have same control configuration and include an inner current loop and an outer voltage loop. Each module actively participates in both voltage and current regulation. However, a problem occurs when there is a damaged or failed inverter in the loop, which needs to be bypassed and isolated quickly to avoid total system failure. Often, two communication lines are used in order to achieve bidirectional communication and better reliability.

2.4.2.4 Instantaneous Average Current Sharing Control

Instantaneous Average Current Sharing (IACS) control is an ALCS scheme for parallel UPS system wherein the output current of each inverter module follows the average load current of the active modules [143]–[145], [147], [150], [163], [172], [173]. A conceptual block schematic of '*N*' parallel-connected inverter modules supplying a common load has been illustrated in Figure 2.19. The average load current can be obtained either by averaging the inverters output currents at Average Current Computation (ACC) block or directly by using the measured total load current and then dividing it by the number of inverters operating in parallel. The current reference i_{oj}^* for each module can be expressed as

$$i_{oj}^* = \frac{i_o}{N} = \frac{1}{N}\sum_{j=1}^{N} i_{oj}, \ \forall j = 1,2,\ldots,N \tag{2.44}$$

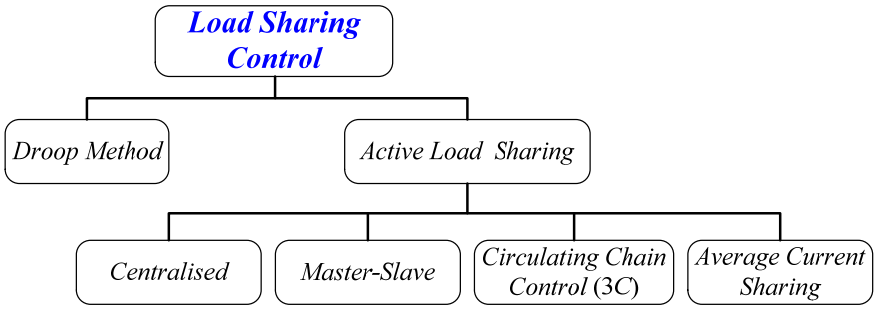


Figure 2.20 Control techniques for parallel operation of UPS inverters system.

This average current becomes reference for the inverter modules, which may be fed from a current sharing bus. The reference voltage is common or synchronised to the make the output voltages in phase. In IACS control configuration, all connected inverters have distributed voltage and current controllers so that they can regulate respective voltage, frequency and current, independently. In this sense, they can be considered as a true democratic ALCS control scheme showing high modularity for further expansion of the UPS system [174].

Summarily, the classification of various control schemes for parallel-connected UPS inverters in may be illustrated as in Figure 2.20.

2.4.3 Review of Instantaneous Average Current Sharing Control

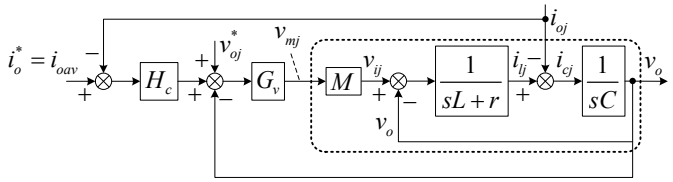
IACS control scheme exhibits a better current sharing performance without sacrificing voltage regulation as compared to droop method. Moreover, being a highly modular and flexible approach of load sharing, it is relatively a more popular kind of ALCS scheme. In [163], instantaneous current sharing control scheme has been proposed which is based on the adjustment of instantaneous reference voltage signal with the inverter output current deviation. Thereafter, various aspects relating to instantaneous current sharing control have been discussed in series of papers [143]–[145], [147], [150], [163], [172], [173], [175], [176]. Modelling, design and stability of voltage and current regulators, considering various causes of current imbalances as disturbance, have been discussed in [150]. Also, the dynamic model of inverter has been established as an equivalent voltage source in series with output impedance. To reduce higher order harmonic circulating currents, proportional gain based voltage reference correction is employed in [144]. VSIs of different power ratings when connected in parallel may be controlled with a current weighing distribution strategy, is shown in [177]. Adaptive gain scheduling for current sharing is employed for IACS scheme when the lengths of interconnecting cables are different [145]. A solution for long connecting cables has also been discussed using inductor current feedback for power sharing in [172].

Most of the aforementioned schemes of the IACS schemes either modify the equivalent voltage source [144], [145], [150], [172] or the output impedance [143], [147], [173] of the inverter to realise the equal power sharing. Circulating current impedance model for inverter, directly supressing the circulating currents without causing any additional drop or distortion in parallel output voltage, is proposed in [176].

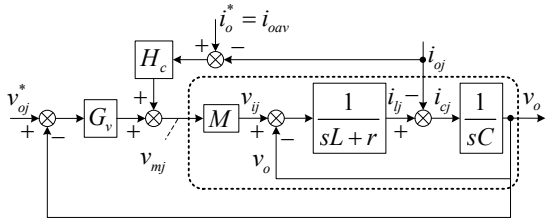
IACS control scheme is a multi-loop control structure in which control of each inverter comprises of at least two loops, i.e., one for voltage regulation and another for current sharing. Two control variants of the IACS scheme are shown in Figure 2.21. Majority of IACS schemes utilise inverter output currents as the feedback variable for equal current sharing except few [172], [175], [178] which uses the filter inductor current. However, for good voltage regulation either capacitor current or load current is also required, along with the filter inductor current [172]. In both cases, anyhow two current sensors are essential for simultaneous control of improved current sharing and voltage performance. The current reference for each module using inductor current can be obtained as

$$i_{lj}^{*} = \frac{\sum_{j=1}^{N} i_{lj}}{N}, \ \forall\, j = 1, 2, \ldots, N \tag{2.45}$$

The inductor current IACS variant invariably requires current measurement of all the modules to generate current reference by the ACC unlike output current IACS where total load current



(a)



(b)

Figure 2.21 Alternate control structures of IACS control for parallel-connected UPS inverters system.

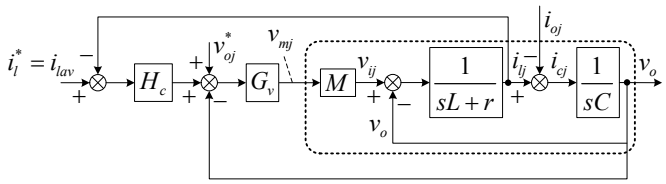


Figure 2.22 IACS control using inductor current for parallel-connected UPS inverters system.

also may generate current reference.

Chapters 4, 5 and 6 present a more detailed analysis on IACS for parallel UPS inverters and investigate further with different control schemes.

2.5 Summary

In first part of the Chapter, review of the single-phase UPS inverter has been presented. It includes discussion on inverter circuit topology, dynamic modelling and control problems. Later, a survey of popular closed-loop control techniques for single-phase inverter has been given in detail with their associated merits and limitations. The control techniques may be divided into three categories mainly i.e., (a) conventional linear control (multi-loop PI, PR, predictive, etc.), (b) non-linear control (hysteresis, sliding mode, fuzzy logic, etc.) and finally (c) periodic control (repetitive, iterative learning).

The second and final part of the chapter reviews control of parallel-connected inverters for UPS applications. The control of parallel inverters again can be classified into two, based on communication link among the modules. Droop control is a communication-less strategy, though its voltage regulation and power sharing is not so good. On the other hand, ALCS uses some kind of communication between inverters for their excellent voltage and current-sharing performance. ALCS schemes in turn can be subdivided into four categories: (a) centralized control, (b) master slave control, (c) current chain control or 3C control, and (d) instantaneous average current sharing control, depending on the way current sharing information is passed. Intercommunications of modules limit their applications in smaller area or closely placed systems. However, with the progress of communication technologies and cost reduction, this may not be a limitation considering the modern day's demand for high performance systems. IACS control has shown advantages over other ALCSs and thus has been selected for investigation in subsequent chapters.

CHAPTER 3: INSTANTANEOUS CONTROL OF SINGLE-PHASE UPS INVERTER IN COMBINED STATIONARY AND SYNCHRONOUS REFERENCE FRAME

3.1 Introduction

Nowadays, UPS inverters invariably employ instantaneous control for maintaining a constant voltage and frequency supply for critical load applications under all operating conditions. In order to achieve the said task, several instantaneous control schemes are prevailing in the literature. These control schemes exploit different feedback control variables and various compensators for their implementation. The first part of the Chapter presents a classification of alternate feedback topologies for instantaneous control, followed by a detailed investigation. The dynamic performances of respective control strategies are comparatively evaluated under both linear and non-linear loading conditions using mathematical modelling and MATLAB/Simulink based simulation. Such a study enables to estimate merits and demerits of respective control topologies based on performance, protection capability, design complexity and cost, thereby help to identify the better approach for a given specific application.

Second part of the Chapter presents an instantaneous voltage-mode control scheme, which exploits combination of stationary and synchronous reference frames of implementation. In this scheme, instead of entire multi-loop control strategy (which comprises of voltage and current loops), only primary control variable i.e., voltage loop, is transferred to the SRF. The presented control scheme uses capacitor current inner-loop for providing damping to the inverter plant response. The voltage mode of inverter control facilitates loop gain adjustments in an independent manner, which does not interfere with other loops during tuning. In addition, reference voltage feed-forward compensation is employed for output voltage disturbance cancellation and to reduce the voltage controller's burden. This not only gives a better tracking efficacy but also simplifies the system modelling and controller design. However, evaluation of close-loop system in Synchronous Reference Frames (SRF) is not possible with conventional control analysis techniques therefore, an equivalent stationary frame model of SRF is attempted for the controller design and stability analysis.

Further, voltage mode of inverter control allows replacement of the voltage controller only, with an alternative controller without affecting the other parts of the control scheme.

The performance of the proposed SRF-PI control scheme has been compared with the PI and PR based integral control for better appreciation through a series of frequency response plots and simulations in the MATLAB/Simulink platform. Later, the control system has been developed on TMS320F2812 based DSP for prototype testing and consequent experimental results are observed to be amicable with the simulations.

3.2 Comparative Evaluation of Alternate Control Structures

The overall performances of the UPS inverter largely rely on the control topology or structure of the employed control schemes. This section first categorizes various control topologies on the basis of control loops and control variables. Next, each close-loop topology for VSI is investigated for reference following ability with a particular focus on their disturbance rejection competency. Finally, steady state and transient performances of respective control strategies have been comparatively evaluated for both linear and non-linear loading conditions using Simulink simulation model.

3.2.1 Classification of UPS Inverter Control Structures

Broadly, UPS inverter control scheme can be classified into two categories of single-loop and multi-loop control [27]. These schemes can be further subdivided into voltage and current mode of control depending on the control variables being regulated. Figure 3.1 categorizes the various control topologies of UPS inverter based on control loops and control variables used. The capacitor or output voltage of inverter is the regulated variable in case of the voltage mode control. This can be a single loop of voltage feedback only or multiple loops utilizing currents along with the voltage feedback. On the other hand, current mode controls are invariably multi-loops with an output voltage and one or two current feedbacks. In this mode,

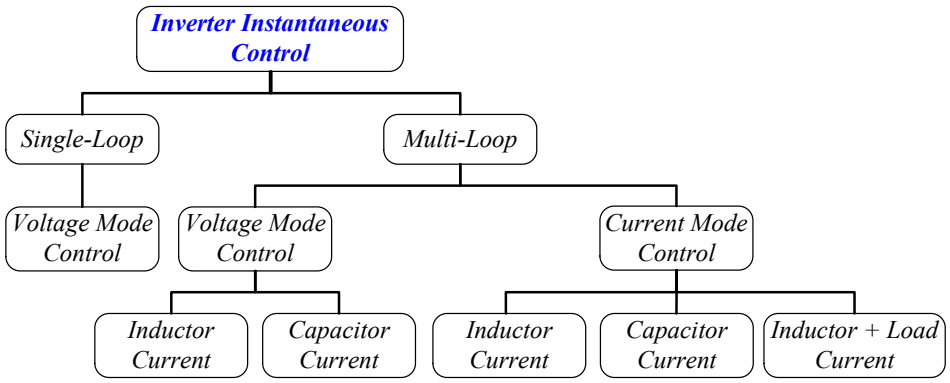


Figure 3.1 Categorisation of closed-loop inverter control.

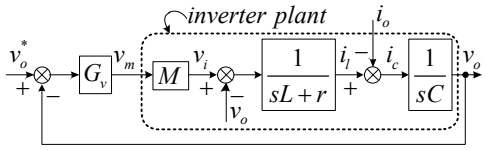


Figure 3.2 Block schematic for single-loop voltage mode inverter control.

both voltage and currents are regulated either for better performance or for protection functionality. Several literatures have discussed various control schemes of inverter using all feasible control state variables [30], [33]–[35], [67]. Being a state variable based close-loop control schemes, it achieves zero steady-state error, only when all the states of the variables and plant parameters are estimated accurately.

3.2.2 Control Structures for UPS Inverters

3.2.2.1 Single-loop Voltage Mode Control

Figure 3.2 shows Single Loop Voltage Mode (SLVM) controlled inverter system with a voltage regulator G_v. The capacitor or output voltage, v_o has been used as the only feedback variable to implement the control scheme. The output voltage, v_o can be derived from the block schematic as,

$$v_o(s) = \frac{G_v(s)}{s^2LC + srC + 1 + G_v(s)} v_o^*(s) - \frac{sL + r}{s^2LC + srC + 1 + G_v(s)} i_o(s)$$

$$= G_{cl}^{SLVM}(s) v_o^*(s) - Z_{cl}^{SLVM}(s) i_o(s) \tag{3.1}$$

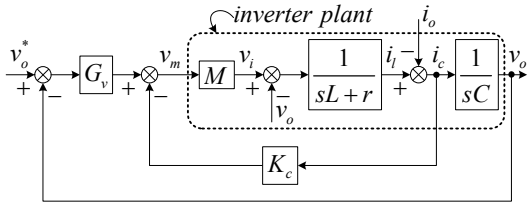
where $G_{cl}^{SLVM}(s) = \frac{G_v(s)}{s^2LC + srC + 1 + G_v(s)}$, is the close–loop voltage gain and $Z_{cl}^{SLVM}(s) = \frac{sL + r}{s^2LC + srC + 1 + G_v(s)}$ is designated as the close–loop impedance for SLVM control topology.

If the voltage controller gain is high enough, such that $G_v(s) >> 1/G_p(s)$, the closed loop voltage gain G_{cl}^{SLVM} may be set to unity, so that the output voltage follows the applied reference voltage. At the same time, it can be seen from (3.1) that the load current disturbance also gets reduced due to low value of second term as a consequence of high gain of the G_v. The load current dependent second term may therefore, can be regarded as a disturbance since the prime objective is to follow the control voltage.

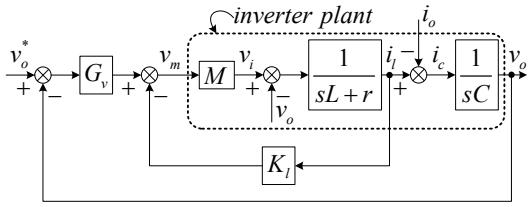
However, as already discussed in sub-section 2.2.2 of chapter 2, *LC* filter introduces an underdamped peak at the resonance frequency. To avoid oscillations on transitions, the voltage gain G_v is limited to a value, which might not be sufficient to eliminate steady state error. Moreover, a low controller gain inflates the output impedance, particularly in low frequency range, which affects the voltage tracking. As a result, SLVM may work well in steady-state for low power linear loads, but its application under non-linear loads and high power inverters are limited. Therefore, although a single-loop reduces the design effort and saves cost, a trade-off has to be made between the inverter performance and its merits.

3.2.2.2 Multi-Loop Voltage Mode Control

The block schematic shown in Figure 3.3 is a Multi-Loop Voltage Mode (MLVM) control scheme for UPS inverters. An outer-loop regulates load voltage, (similar to SLVM control) whereas the inner current loop provides Active Damping (AD) to the inverter plant. As it is already shown in Chapter 2, providing damping by a real physical resistor is inappropriate, a better way is change the plant transfer function characteristics via control. Two common ways of AD using filter capacitor current and inductor current feedbacks are shown in Figure 3.3(a) and (b), respectively. The modifications in the output voltage response with respect to the (3.1) may be derived from Figure 3.3 as,



(a)



(b)

Figure 3.3 Closed-loop inverter control strategy with (a) Voltage Mode Capacitor (VMC) and (b) Voltage Mode Inductor (VMI) current feedback.

$$v_o(s) = \frac{G_v(s)}{s^2LC + s(r+K_c)C + 1 + G_v(s)} v_o^*(s) - \frac{sL + r}{s^2LC + s(r+K_c)C + 1 + G_v(s)} i_o(s)$$

$$= G_{cl}^{VMC}(s) v_o^*(s) - Z_{cl}^{VMC}(s) i_o(s) \tag{3.2}$$

$$v_o(s) = \frac{G_v(s)}{s^2LC + s(r+K_l)C + 1 + G_v(s)} v_o^*(s) - \frac{sL + (r+K_l)}{s^2LC + s(r+K_l)C + 1 + G_v(s)} i_o(s)$$

$$= G_{cl}^{VMI}(s) v_o^*(s) - Z_{cl}^{VMI}(s) i_o(s) \tag{3.3}$$

where G_{cl}^{VMC} and G_{cl}^{VMI} are designated as the close–loop voltage gains for Voltage Mode Capacitor (VMC) and Voltage Mode Inductor (VMI) current feedback control topologies, respectively. On the other hand, Z_{cl}^{VMC} and Z_{cl}^{VMI} refer to the close–loop output impedances for VMC and VMI control strategies, respectively. For both control variants, as stated in (3.2) and (3.3), it may be seen that the voltage gains are identical, if current feedback gains (K_c and K_l) are chosen to be same (to achieve equal damping). However, output impedance for the inductor current is observed to be higher than the capacitor current feedback, due to the appearance of an additional term K_l in the numerator of Z_{cl}^{VMI} in (3.3).

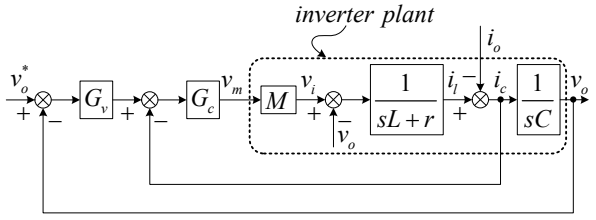
3.2.2.3 Multi-loop Current Mode Control

Multi-Loop Current Mode (MLCM) control or cascaded control uses an approach for controller design, wherein the specified variables are regulated to reach a certain objective by some reference command [30], [41]. The control block schematic in Figure 3.4 shows multi-loop controller for VSI in current control mode. Multi-loop current mode control have three variants, namely (a) capacitor current feedback (CMC), (b) inductor current feedback (CMI), and (c) inductor current feedback with load current feedforward (CMIL). The CMIL is basically a capacitor current realisation, since capacitor current is the difference of inductor and load current. Therefore, the closed-loop output voltage transfer-functions obtained from Figure 3.4 for CMC and CMIL have been given in (3.4) and are same for both.

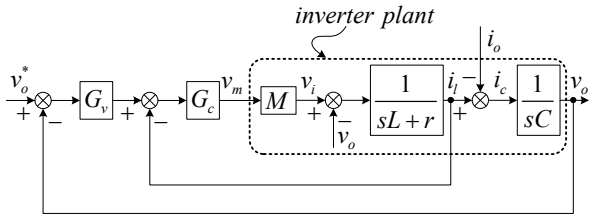
$$v_o(s) = \frac{G_v(s)G_c(s)}{s^2LC + srC + sCG_c(s) + 1 + G_v(s)G_c(s)} v_o^*(s)$$

$$- \frac{sL + r}{s^2LC + srC + sCG_c(s) + 1 + G_v(s)G_c(s)} i_o(s)$$

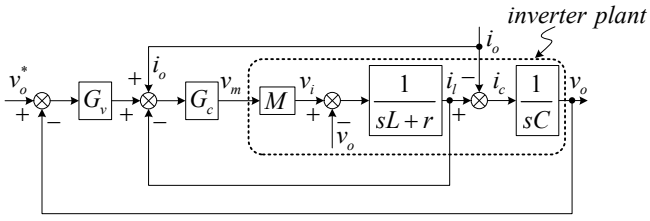
$$= G_{cl}^{CMC}(s) v_o^*(s) - Z_{cl}^{CMC}(s) i_o(s) = G_{cl}^{CMIL}(s) v_o^*(s) - Z_{cl}^{CMIL}(s) i_o(s) \tag{3.4}$$



(a)



(b)



(c)

Figure 3.4 Closed-loop inverter control with (a) Current Mode Capacitor (CMC) & (b) Current Mode Inductor (CMI) current feedbacks and (c) Current Mode Inductor current feedback with Load (CMIL) current feed-forward.

The closed-loop output voltage for CMI is given in (3.5) as,

$$v_o(s) = \frac{G_v(s)G_c(s)}{s^2LC + srC + sCG_c(s) + 1 + G_v(s)G_c(s)} v_o^*(s) - \frac{sL + r + G_c(s)}{s^2LC + srC + sCG_c(s) + 1 + G_v(s)G_c(s)} i_o(s)$$

$$= G_{cl}^{CMI}(s)v_o^*(s) - Z_{cl}^{CMI}(s)i_o(s) \tag{3.5}$$

The closed-loop voltage gains G_{cl}^{CMC}, G_{cl}^{CMI} and G_{cl}^{CMIL} for CMC, CMI and CMIL, respectively are exactly equal for all of the three current mode variants. Z_{cl}^{CMC}, Z_{cl}^{CMI} and Z_{cl}^{CMIL} are the close–loop output impedances for capacitor, inductor and inductor plus load current control structures, respectively. In case of current mode also, similar to voltage mode control, inductor current feedback has been observed with inferior load disturbance

Table 3.1 Controller parameters

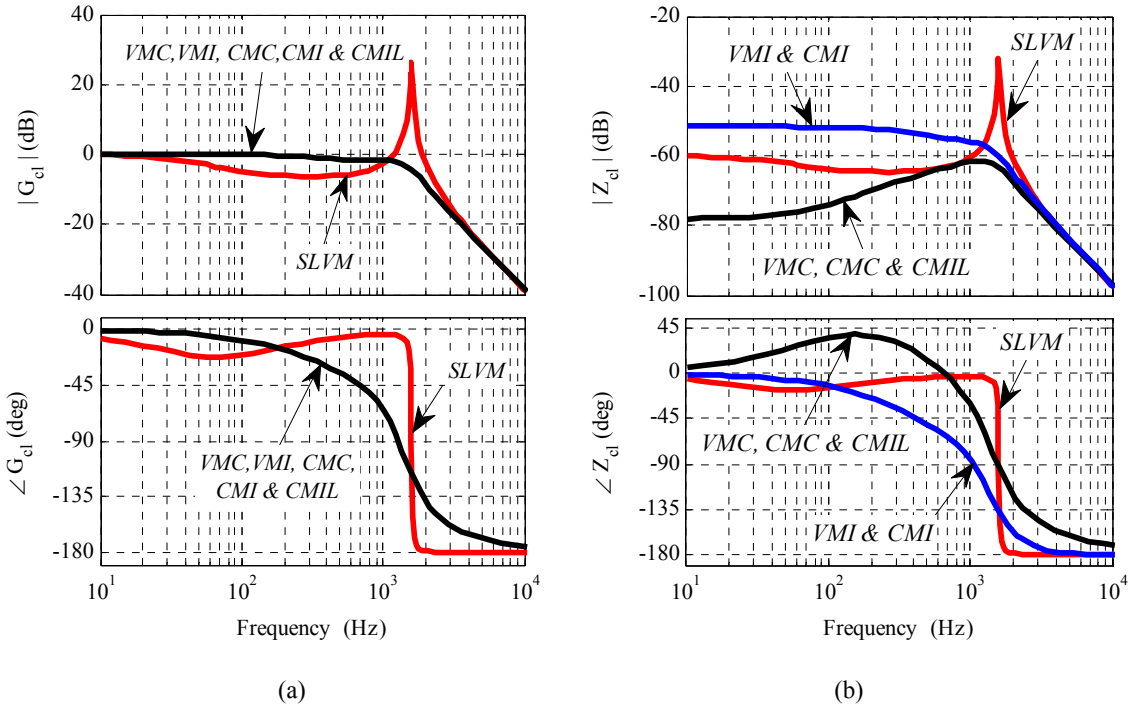
	Voltage Controller (G_v)		*Current Controller* (G_c)	*Damping Coefficient*
	K_p	K_i	K_{cp}	K_c / K_l
SLVM	0.80	500	–	–
VMC	0.80	4000	–	10
VMI	0.80	4000	–	10
CMC	0.08	400	10	–
CMI	0.08	400	10	–
CMIL	0.08	400	10	–

characteristics. This is due to the presence of an additional $G_c(s)$ term in its second part of the voltage equation in (3.5). On the other hand, inductor current feedback with load current feedforward has an identical performance as that of the capacitor current feedback, as evident from its resultant output voltage in (3.4).

A comparative analysis of alternate control topologies may be done from the frequency response plots of the obtained transfer functions. This provides an insight into the anticipated steady-state and transient performance of the UPS inverter system. For simplicity, a proportional integral (PI) regulator for voltage compensator G_v and a Proportional (P) control for current compensator G_c has been used for the study, whose tuned controller parameters are enlisted in Table 3.1.

Bode frequency response characteristics of various control topologies have been plotted in Figure 3.5. It shows a resonant peak in both voltage G_{cl}^{SLVM} and impedance Z_{cl}^{SLVM} plots for the SLVM control. This leads to oscillations in output response on reference voltage and load transitions. Voltage gains of regulator, particularly K_i, are limited to a smaller value due to stability reasons. This results in large steady-state error, both in magnitude and phase plots for SLVM control scheme. Low voltage gain also results in relatively higher output impedance at operating frequencies as seen from Figure 3.5(b), which degrades the disturbance rejection capability of the inverter.

Figure 3.5, further shows the voltage and impedance magnitude plots are well damped for all multi-loop control schemes. Similar, performance can be expected from all the control structures of MLVM and MLCM, as observed from the close-loop voltage gain G_{cl} frequency response plots. However, the impedance Z_{cl} as seen from Bode plots of Figure 3.5(b), creates the main difference in overall performance of the control topologies. Both, MLVM and MLCM inductor current feedback schemes, have almost constant-value large impedance in



(a) (b)

Figure 3.5 Bode-plots for various control structures (a) Voltage gains and (b) Output impedances.

entire control bandwidth. With the selected control parameters, the output impedances have been observed to be even higher than the SLVM, particularly in mid-frequency ranges. This leads to a higher voltage drop and poor disturbance rejection capability on loading with inductor current feedback control schemes. Whereas, the capacitor current and inductor plus load current multi-loop control schemes have identical low output impedance and hence, similar performance may be expected.

Table 3.2 consolidates the transfer functions of alternate control structures for inverter control. In order to evaluate the effect of control structure on the performance of the UPS inverter, control schemes have been extensively simulated in MATLAB/Simulink environment under different operating conditions. The control structures use PI and P control logic for voltage and current regulators, respectively, whose parameters have been already enumerated in Table 3.1. Since PI controller will introduce phase lag, a reference voltage feedforward is employed for better tracking efficacy. Feedforward has a cancelling effect on the output voltage disturbance and improves overall system robustness. A single-phase UPS inverter system has been designed with a specification of 250 VA, 80 V and 50 Hz to investigate the performances of the control algorithms presented above. The inverter comprises of a full bridge module with a constant DC source and a LC filter at the output end. Gating has been generated using uni-polar Sinusoidal Pulse Width Modulation (SPWM)

Table 3.2 Transfer functions for various control strategies

Control Structure	*Voltage Gain* (G_{cl})	*Output Impedance* Z_{cl}
SLVM	$\frac{G_v(s)}{s^2LC+srC+G_v(s)}$	$\frac{sL+r}{s^2LC+srC+G_v(s)}$
VMC	$\frac{G_v(s)}{s^2LC+srC+sCK_c+G_v(s)}$	$\frac{sL+r}{s^2LC+srC+sCK_c+G_v(s)}$
VMI	$\frac{G_v(s)}{s^2LC+srC+sCK_l+G_v(s)}$	$\frac{sL+r+K_l}{s^2LC+srC+sCK_l+G_v(s)}$
CMC	$\frac{G_v(s)G_c(s)}{s^2LC+srC+sCG_c(s)+G_v(s)G_c(s)}$	$\frac{sL+r}{s^2LC+srC+sCG_c(s)+G_v(s)G_c(s)}$
CMI	$\frac{G_v(s)G_c(s)}{s^2LC+srC+sCG_c(s)+G_v(s)G_c(s)}$	$\frac{sL+r+G_c(s)}{s^2LC+srC+sCG_c(s)+G_v(s)G_c(s)}$
CMIL	$\frac{G_v(s)G_c(s)}{s^2LC+srC+sCG_c(s)+G_v(s)G_c(s)}$	$\frac{sL+r}{s^2LC+srC+sCG_c(s)+G_v(s)G_c(s)}$

technique. Loads (both linear and non-linear) have been designed in accordance to the IEC 62040-3 standard for the UPS inverter system.

3.2.3 Simulation Evaluation under Linear Load

Simulations have been carried out for six control topologies, namely; SLVM, VMC, VMI, CMC, CMI and CMIL control schemes. The steady-state responses under rated linear load are displayed in Figure 3.6 for all of them. Output voltage, output voltage error from the reference and respective current waveforms has been plotted in the sub-figures. Figure 3.6(a) shows large voltage error due to selected lower gains in voltage controller to avoid instability at the resonance frequency. Sub-Figure 3.6(b), (d) & (f) show better steady state performance for capacitor current control structures (CMIL is essentially a capacitor current feedback scheme). As the inverter is better damped, a higher gain has been selected for improved voltage regulation. Though gains of the inductor current control structures are same as the capacitor current schemes, large steady-state error in voltages for VMI and CMI in Figure 3.6(c) & (e) can be attributed to higher output impedances.

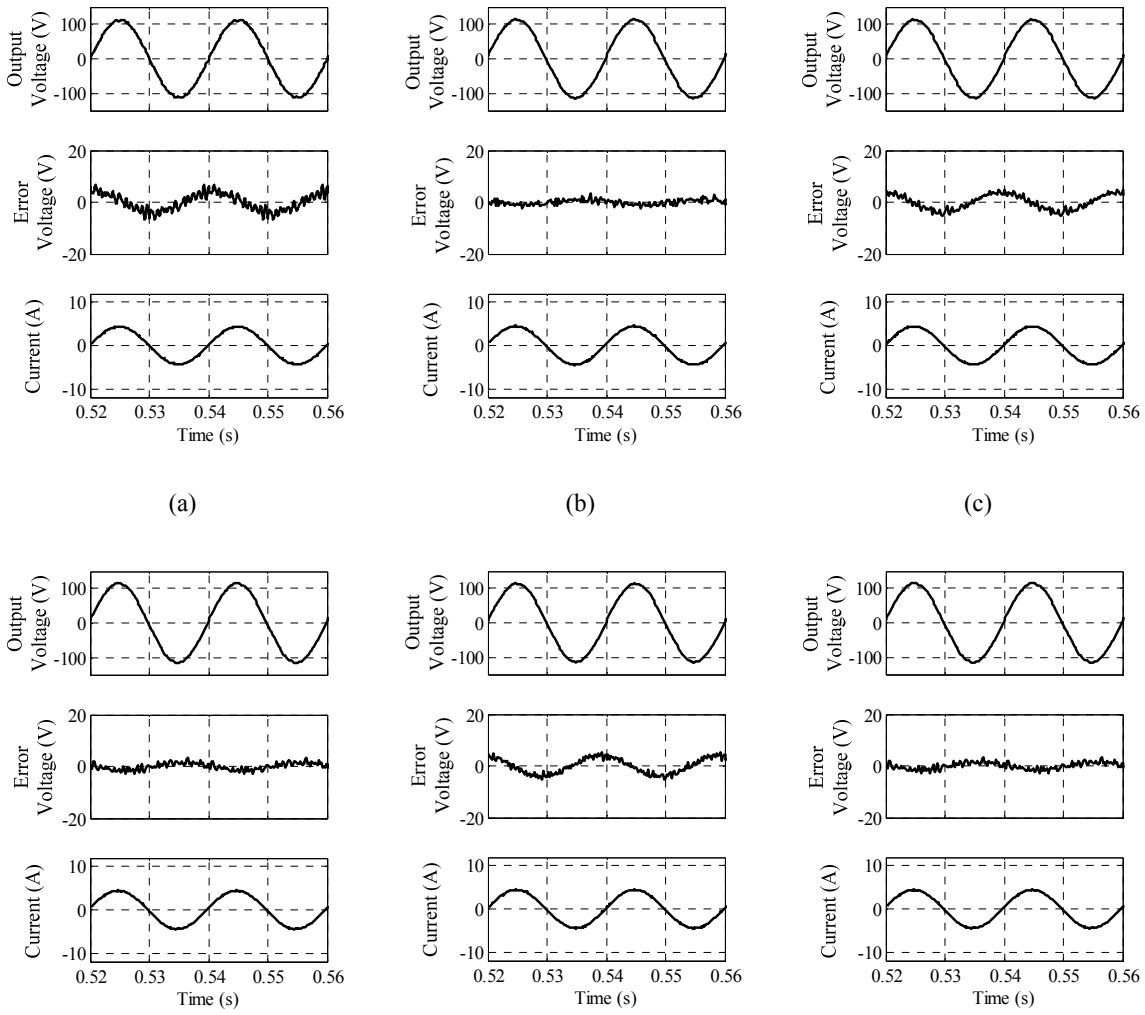


Figure 3.6 Steady-state response for rated linear load (a) SLVM, (b) VMC, (c) VMI, (d) CMC, (e) CMI and (f) CMIL inverter control strategies.

Transient waveforms in Figure 3.7 demonstrate the true benefit of damped resonant peak of the inverter plant. Since there is no provision for damping in SLVM control, turn-off transient response is quite oscillatory. All multi-loop control schemes employ some form of AD and therefore their turn-on and turn-off behaviours are stable.

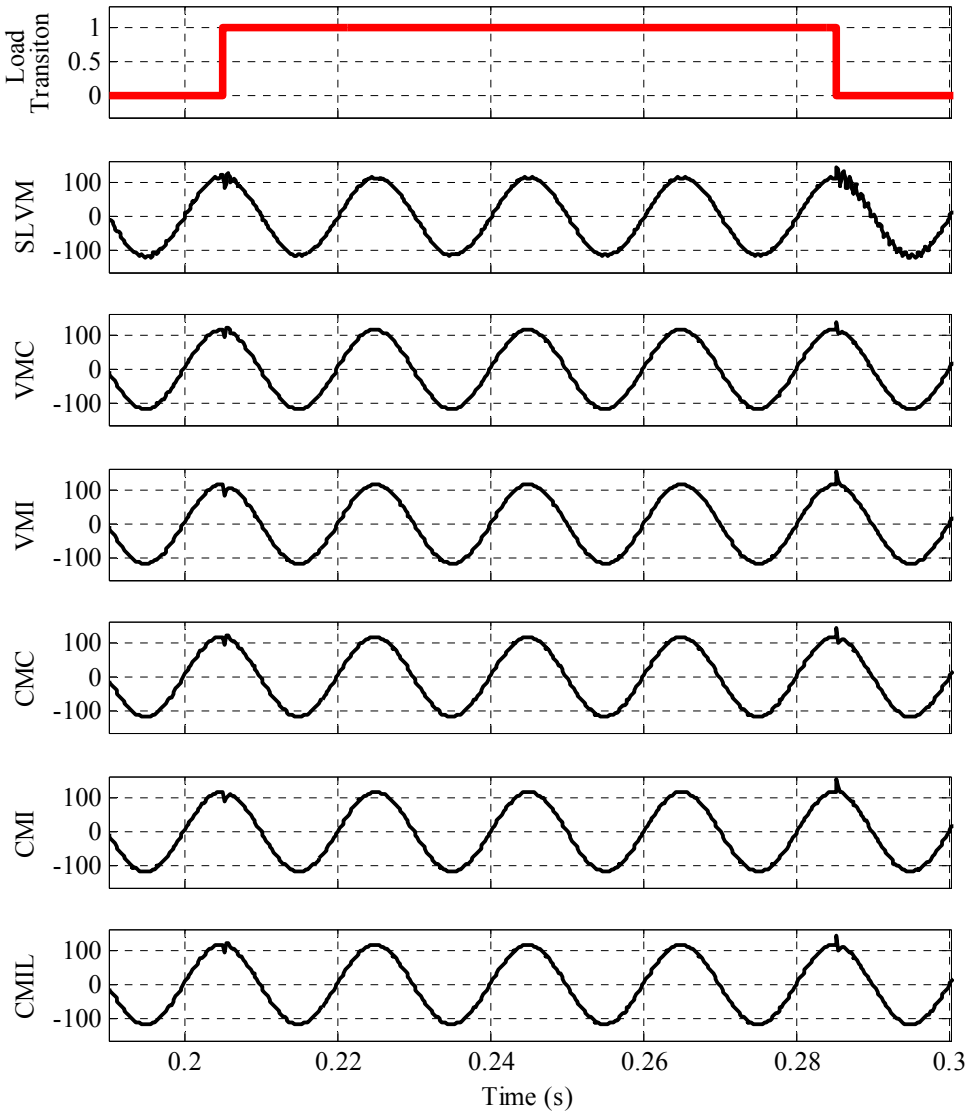


Figure 3.7 Transient voltage (V) waveforms for step transitions of rated linear load with various control schemes.

3.2.4 Simulation Evaluation under Non-Linear Load

Figure 3.8 shows steady state waveforms for the respective control structures under rated non-linear load. The results show patterns similar to the linear loading conditions as per as control structures are concerned. In SLVM control, apart from the large steady-state voltage error, oscillations in output voltage waveform have been observed due to under-damped plant. The effect is more prominent due to the sub-cyclic transient on non-linear loading. The capacitor current feedback schemes have better damping and lower output impedances and

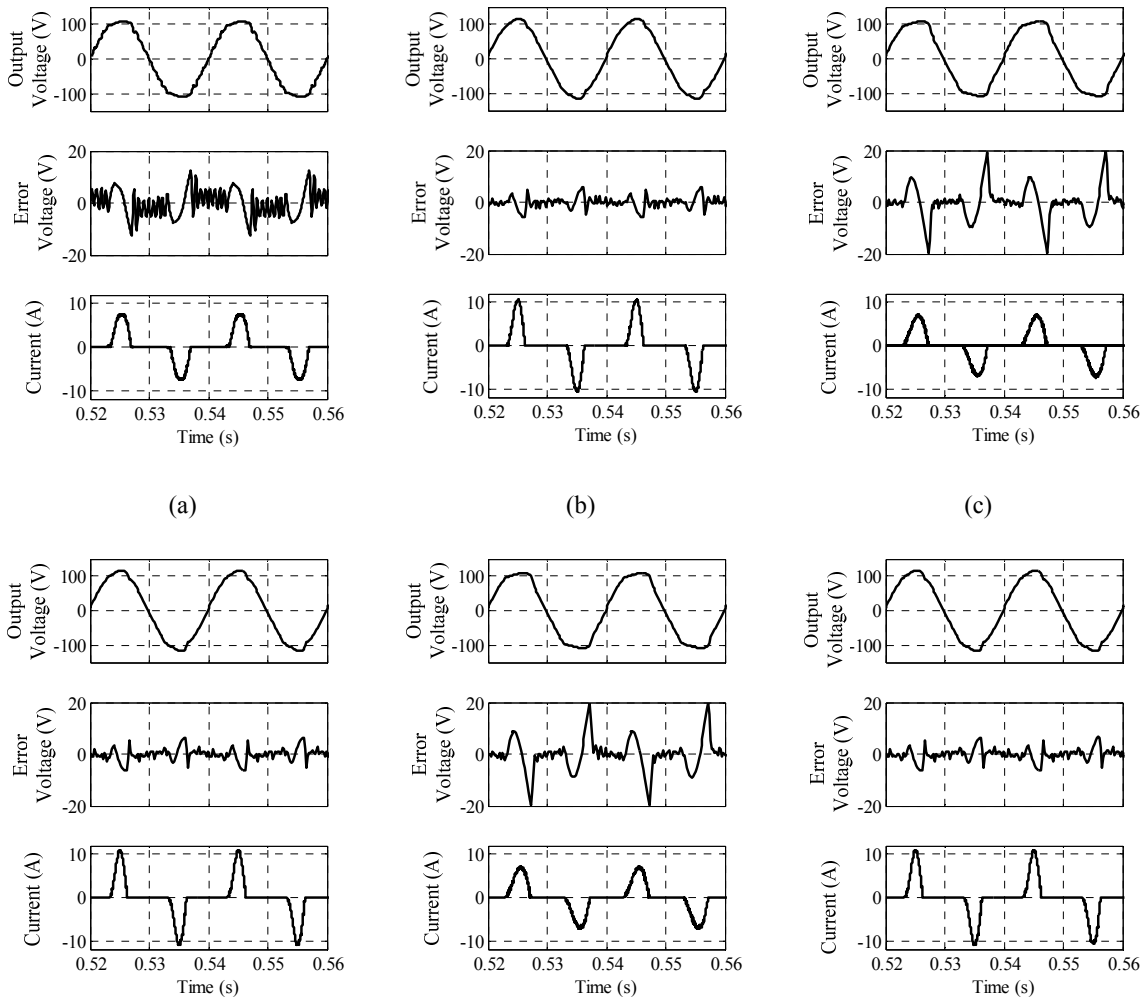


Figure 3.8 Steady-state response for rated non-linear load (a) SLVM, (b) VMC, (c) VMI, (d) CMC, (e) CMI and (f) CMIL inverter control strategies.

hence better performance, as seen from Figure 3.8(b), (d) and (f). On the other hand, the impedance in inductor current schemes is high for the entire frequency spectrum and hence shows poor non-linear loading performance. In fact, the output voltages for VMI and CMI strategies are observed inferior to the SLVM, which may be better understood from their relative output impedances.

Further, Figure 3.9 shows the load transition behaviour of the respective control schemes. Higher oscillations are detected under non-linear loading for SLVM control similar to linear loading. Otherwise, load removal transients are almost similar for all multi-loop

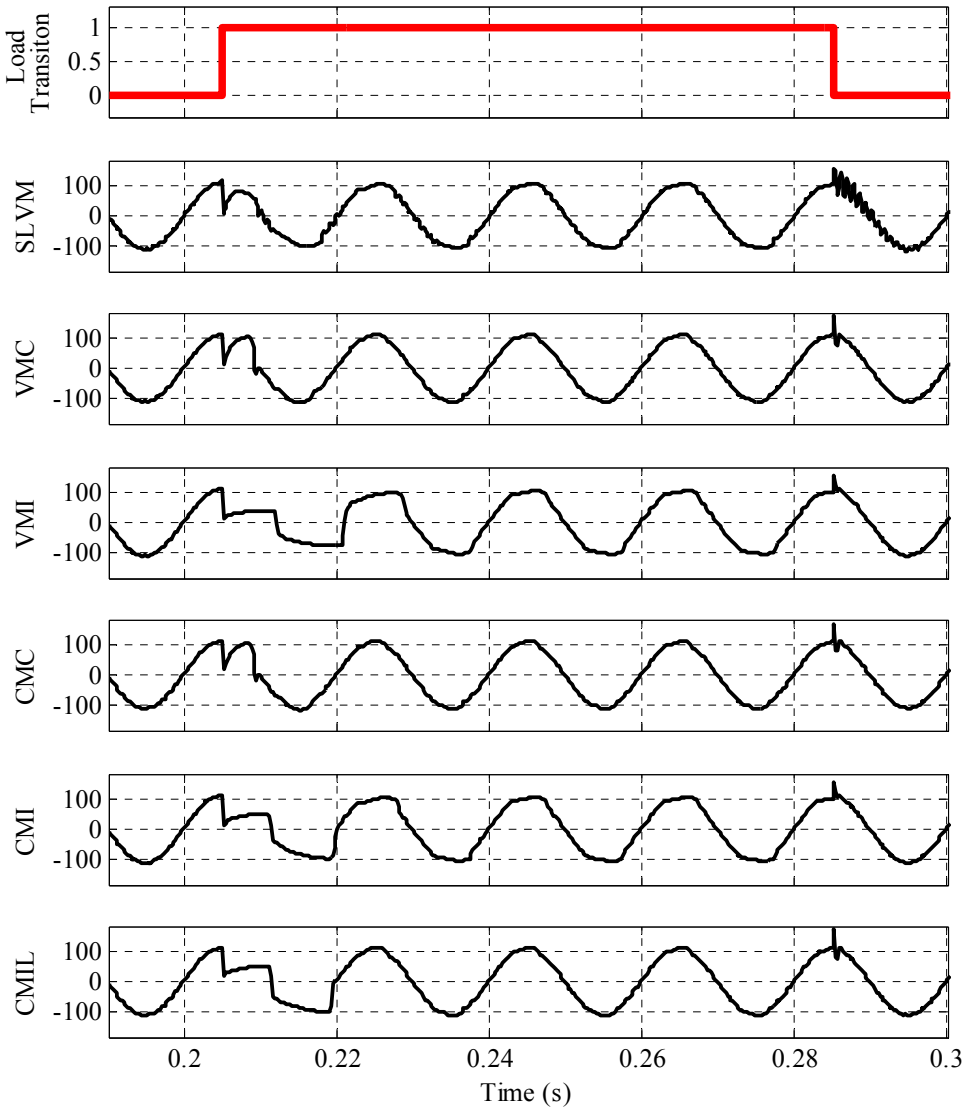


Figure 3.9 Transient voltage (V) waveforms for step transitions of rated non-linear load with various control schemes.

control schemes. A higher recovery time in voltage waveforms during load application for CMI and CMIL is observed due to the current limit implementation.

Performance parameters, namely, percentage voltage error (%ve) and %THD of various control schemes are compared in Table 3.3 for steady-state condition under both linear and non-linear loads. The effect of under-damping in SLVM can be prominently quantified from the linear load %THD value of 1.55 as compared to other control structures. Similar to waveforms, the voltage error and THD data also show superiority of capacitor current feedback schemes. The poor performance figures of inductor current feedback control

schemes, particularly under non-linear loading, are mainly due to the higher impedance even though the plant is effectively damped.

The transient performances such as; percentage undershoot on load application, percentage overshoot during load removal and settling time on load removal are also tabulated

Table 3.3 Steady-state performance on rated load

	Linear Load		**Non-Linear Load**	
	% v_e	**% THD**	**% v_e**	**% THD**
SLVM	4.00	1.55	6.25	5.40
VMC	1.25	0.90	2.87	2.73
VMI	3.50	0.96	7.75	7.40
CMC	1.70	0.97	3.10	2.85
CMI	3.68	0.80	7.87	7.35
CMIL	1.68	0.97	3.12	2.80

Note: % Error =100 x $(v_o^*-v_o)/v_o^*$

Table 3.4 Transient performance on rated linear load

	% Undershoot (Load application)	**% Overshoot (Load removal)**	**Settling-time (ms) (Load removal)**
SLVM	29.00	31.00	7
VMC	22.00	25.25	1
VMI	29.60	37.78	1.5
CMC	18.50	27.36	1
CMI	27.20	37.00	1.5
CMIL	18.50	27.36	1

Note: % Undershoot or % Overshoot =100 x $(|v_o^*-v_o|/v_o^*)$

Table 3.5 Normalized performances under linear load considering CMIL as reference

	SLVM	**VMC**	**VMI**	**CMC**	**CMI**	**CMIL**
Error	2.38	0.74	2.08	1.01	2.19	1.00
THD	1.60	0.93	0.99	1.00	0.82	1.00
Undershoot	1.57	1.19	1.60	1.00	1.47	1.00
Overshoot	1.13	0.92	1.38	1.00	1.35	1.00
Settling-time	7.00	1.00	1.50	1.00	1.50	1.00
Sensors/Cost	0.33	0.67	0.67	0.67	0.67	1.00

in Table 3.4 under linear loading conditions. The load current disturbance on load application is prominent in inductor current feedback schemes. A settling time of 7ms in SLVM is much higher than other control structures because of under-damp oscillations in the voltage waveform. The performance of the inductor plus load current control scheme has all the elements of a present state-of-art control topology. Therefore, taking CMIL as the benchmark control topology, performance indices of other topologies under linear loading are tabulated in Table 3.5. VMC and CMC have the closest match to the benchmark topology. Although overcurrent protection is absent, nevertheless cost reduction of one sensor is a plus point.

Summarily, it can be concluded from the above analysis that SLVM control is generally recommended for applications wherein stringent voltage quality is not mandatory. Such topology has an advantage of reduced design complexity and low cost (due to requirement of only one sensor). Multi-loop control architecture demands for additional sensors for their inner loop implementation. Both, voltage and current mode control show similar performance for respective capacitor and inductor current feedbacks. However, design complexity in case of the voltage mode control is lesser than the current mode with decoupled parameter tunings. Although, inductor current feedback provides the same damping as the capacitor current variants, it suffers from poor load disturbance rejection capability. Nevertheless, only inductor current variants, CMI and CMIL are capable of inherent over current protection. This makes the CMIL as a benchmark for the control topologies with complete features of better damping, good disturbance rejection and overcurrent protection. Therefore, considering all aspects of figure of merit, suitable topology is to be opted for so that performance and reliability are not compromised.

3.3 Synchronous Reference Frame Control of Single-Phase Inverter

Analysis in SRF has been an established technique and widely used in control of three-phase Voltage source inverters (VSIs). In this approach, the control variables are transformed from stationary frame to synchronously rotating reference frame (SRF) wherein they become DC quantities. PI regulators then enable to achieve zero steady-state error. However, the same approach cannot be directly applied in case of single-phase due to the absence of orthogonal quadrature axis (β-axis) variables when in stationary frame. Therefore, complexity of consequent Orthogonal Signal Generation (OSG) in stationary reference frame becomes the main hurdle for use of SRF *d-q* regulators in single-phase applications despite of their popularity in the three-phase [179].

The SRF control scheme has two options, either the control strategy using both voltage and current loops may be realised in *d-q* SRF or only the voltage loop may be implemented

in *d-q* SRF [180]. The latter option has advantages of simplicity in design and reduced transformational-computations. The following sub-sections present a voltage-mode instantaneous control for UPS inverter, wherein both *d-q* (rotating) and *α-β* (stationary) reference frames have been put to application in a combined manner. Investigation therefore comprises of OSG technique applied, overall control scheme and stationary frame equivalency of the complete control strategy.

3.3.1 Orthogonal Signal Generation Technique

In literature review of chapter 2, several OSG techniques to generate the *β*-axis orthogonal component (stationary frame) from the original signal have been discussed in detail. This investigation uses All Pass Filter (APF) as an OSG technique due to their unattenuated transfer characteristics throughout the entire frequency spectrum. The transfer function of the APF having fundamental angular frequency ω_o may be stated as

$$\frac{v_\beta(s)}{v_\alpha(s)} = -\frac{s-\omega_o}{s+\omega_o} \tag{3.6}$$

Once the β-axis variable is obtained, SRF control can be implemented for control of the inverter system.

3.3.2 Combined *d-q* and *α-β* Reference Frame Control Structure

Figure 3.10, shows the implemented voltage-mode inverter control strategy, which has been implemented in combined synchronous and stationary reference frames. There are two main control loops, namely, an outer-loop with voltage controller $G_v(s)$ and an inner-loop with a feedback gain of K_c. In this presented control scheme, only the outer voltage-loop has

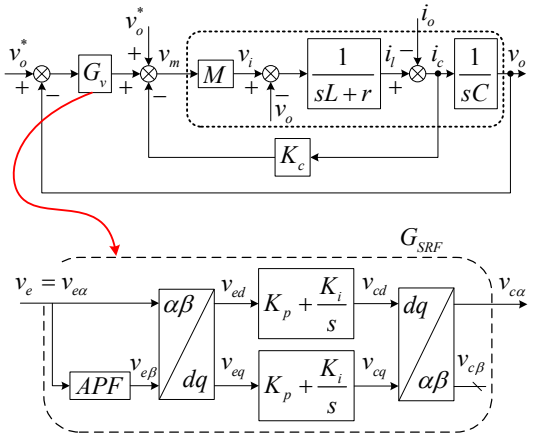


Figure 3.10 Block schematic of single-phase SRF-PI control for UPS inverter.

been implemented in SRF whereas the inner current-loop has been realised in stationary α-β frame of reference. The blow up for $G_v(s)$ has been shown below (G_{SRF}) with dashed boundary in Figure 3.10. Voltage error, v_e has been processed first through an APF block to obtain the β-axis signal. Next, the α-β axis AC signals have been then transformed to d-q frame DC voltage error signals $v_{e(d-q)}$ using Park's transformation (α-$\beta \rightarrow d$-q) matrix. As a consequence, voltage error may therefore be regulated by conventional PI control with zero steady-state error in the rotating d-q frame. The α-β stationary frame compensated voltage signals are obtained by applying inverse Park's transformation (d-$q \rightarrow \alpha$-β) to the output of the d-q frame PI controllers. Since, β-axis signal is a virtual quantity, only the α-axis compensated voltage signal $v_{c\alpha}$ is propagated for further processing.

The α-axis compensated output of the voltage-controller $G_v(s)$ has been further supplemented by a reference voltage (v_o^*) feed-forward signal to improve overall system robustness. A major component of the control effort is the feed-forward signal whereas the voltage controller compensates for the error disturbances and improves the tracking response. An inner capacitor current-loop is also included in the control strategy to provide AD to the otherwise peaky LC filter response. The undamped inverter plant may distorts the output voltage even on lesser harmonic currents and therefore may be a threat to stability on loading step-transitions. Capacitor current with feedback gain K_c virtually emulates a real resistance for damping and is an efficient solution than the actual passive component. Capacitor current feedback has been used for AD because of its better disturbance rejection capability, as already discussed earlier.

The control topology adopted in Figure 3.10 is basically a Multi-Loop Voltage Mode (MLVM) control using capacitor current. Only, difference lies in the fact that the voltage controller realisation has been in the synchronously rotating d-q frame, while rest of the control scheme is in the α-β axis. However, control design and stability analysis of the resultant close-loop system become quite complicated due to mixed frames.

3.3.3 Stationary α-β frame equivalent of SRF-PI

One of the better way of analysis may be the transformation of the PI regulator to the α-β frame itself instead of complex AC signals conversions to the d-q frame [39]. The Park transformation matrices for translating from stationary to rotating frame (α-$\beta \rightarrow d$-q) and from rotating to stationary frame (d-$q \rightarrow \alpha$-β) are defined in (3.7) and (3.8), respectively as,

$$T_{\alpha-\beta \rightarrow d-q} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix} \tag{3.7}$$

$$T_{d-q\to\alpha-\beta}=\begin{bmatrix}\cos\omega t & -\sin\omega t\\ \sin\omega t & \cos\omega t\end{bmatrix} \tag{3.8}$$

From Figure 3.10, the time domain error compensated voltages $v_{c(\alpha\text{-}\beta)}$ can be expressed as,

$$\begin{bmatrix}v_{c\alpha}(t)\\ v_{c\beta}(t)\end{bmatrix}=\begin{bmatrix}\cos\omega t & -\sin\omega t\\ \sin\omega t & \cos\omega t\end{bmatrix}\left\{\begin{bmatrix}G_{PI}(t) & 0\\ 0 & G_{PI}(t)\end{bmatrix}*\left\{\begin{bmatrix}\cos\omega t & \sin\omega t\\ -\sin\omega t & \cos\omega t\end{bmatrix}\begin{bmatrix}v_{e\alpha}(t)\\ v_{e\beta}(t)\end{bmatrix}\right\}\right\} \tag{3.9}$$

where '$*$' refers to the convolution operator. The compensated voltage in s-domain may be obtained by applying Laplace transform on both sides of (3.9),

$$\begin{bmatrix}v_{c\alpha}(s)\\ v_{c\beta}(s)\end{bmatrix}=\frac{1}{2}\begin{bmatrix}G_{PI}\left(s-\hat{i}\omega\right)+G_{PI}\left(s+\hat{i}\omega\right) & \hat{i}G_{PI}\left(s-\hat{i}\omega\right)-\hat{i}G_{PI}\left(s+\hat{i}\omega\right)\\ \hat{i}G_{PI}\left(s+\hat{i}\omega\right)-jG_{PI}\left(s-\hat{i}\omega\right) & G_{PI}\left(s+\hat{i}\omega\right)+G_{PI}\left(s-\hat{i}\omega\right)\end{bmatrix}\begin{bmatrix}v_{e\alpha}(s)\\ v_{e\beta}(s)\end{bmatrix} \tag{3.10}$$

On substitution of $G_{PI}=K_p+K_i/s$ in (3.10), gives

$$\begin{bmatrix}v_{c\alpha}(s)\\ v_{c\beta}(s)\end{bmatrix}=\begin{bmatrix}K_p+K_i\left(\frac{s}{s^2+\omega^2}\right) & -K_i\frac{\omega}{s^2+\omega^2}\\ K_i\frac{\omega}{s^2+\omega^2} & K_p+K_i\left(\frac{s}{s^2+\omega^2}\right)\end{bmatrix}\begin{bmatrix}v_{e\alpha}(s)\\ v_{e\beta}(s)\end{bmatrix} \tag{3.11}$$

Out of this, only α–axis signal is the real quantity of the pseudo two-phase system and can be obtained from (3.11), using (3.6) as

$$v_{c\alpha}(s)=\left[K_p+K_i\left\{\left(\frac{s}{s^2+\omega^2}\right)-\frac{\omega}{s^2+\omega^2}\left(\frac{\omega-s}{\omega+s}\right)\right\}\right]v_{e\alpha}(s) \tag{3.12}$$

The detailed worked out of the above synthesis has been given in Appendix A. Rearranging (3.12), gives the stationary frame equivalent of the SRF-PI voltage controller transfer function as,

$$v_{c\alpha}(s)=\left[K_p+K_i\left\{\frac{s^2+2s\omega-\omega^2}{s^3+s^2\omega+s\omega^2+\omega^3}\right\}\right]v_{e\alpha}(s)=G_{SRF}(s)v_{e\alpha}(s) \tag{3.13}$$

where, $G_{SRF}(s)=K_p+K_i\left\{\frac{s^2+2s\omega-\omega^2}{s^3+s^2\omega+s\omega^2+\omega^3}\right\}$. On substituting $G_{SRF}(s)$ into $G_v(s)$ block of Figure 3.10, the expression for the output voltage can be derived as,

$$v_o(s)=G_{cl}^{SRF}(s)v_o^*(s)-Z_{cl}^{SRF}(s)i_o(s) \tag{3.14}$$

where, $G_{cl}^{SRF}(s)=\dfrac{\left(s^3+\omega_o s^2+\omega_o^2 s+\omega_o^3\right)K_p+\left(s^2+2\omega_o s-\omega_o^2\right)K_i}{\left(s^3+\omega_o s^2+\omega_o^2 s+\omega_o^3\right)\left(s^2LC+srC+sCK_c+K_p\right)+\left(s^2+2\omega_o s-\omega_o^2\right)K_i}$, and

$$Z_{cl}^{SRF}(s)=\frac{\left(s^3+\omega_o s^2+\omega_o^2 s+\omega_o^3\right)(sL+r)}{\left(s^3+\omega_o s^2+\omega_o^2 s+\omega_o^3\right)\left(s^2LC+srC+sCK_c+K_p\right)+\left(s^2+2\omega_o s-\omega_o^2\right)K_i}$$

On substitution ($s=\hat{i}\omega_o$) into (3.14), the closed-loop voltage and impedance gains for SRF-PI regulator may be expressed as:

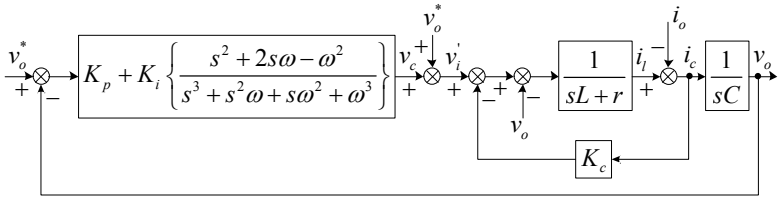
$$G_{cl}^{SRF}(s)=\frac{\left(-\hat{i}\omega_o^3-\omega_o^3+\hat{i}\omega_o^3+\omega_o^3\right)K_p+\left(-\omega_o^2+\hat{i}2\omega_o^2-\omega_o^2\right)K_i}{\left(-\hat{i}\omega_o^3-\omega_o^3+\hat{i}\omega_o^3+\omega_o^3\right)\left(-\omega_o^2LC+\hat{i}\omega_o rC+\hat{i}\omega_o CK_c+K_p\right)+\left(-\omega_o^2+\hat{i}2\omega_o^2-\omega_o^2\right)K_i},$$

$$Z_{cl}^{SRF}(s)=\frac{\left(-\hat{i}\omega_o^3-\omega_o^3+\hat{i}\omega_o^3+\omega_o^3\right)(sL+r)}{\left(-\hat{i}\omega_o^3-\omega_o^3+\hat{i}\omega_o^3+\omega_o^3\right)\left(-\omega_o^2LC+\hat{i}\omega_o rC+\hat{i}\omega_o CK_c+K_p\right)+\left(-\omega_o^2+\hat{i}2\omega_o^2-\omega_o^2\right)K_i} \qquad (3.15)$$

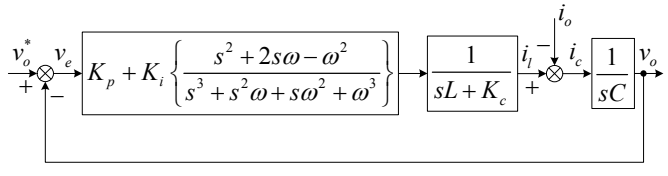
The regulated output voltage perfectly tracks its reference with a zero steady state error i.e., $G_{cl}^{SRF}(s)\to 1$ and $Z_{cl}^{SRF}(s)\to 0$, when the angular frequency is ω_o.

3.3.4 Controller Parameter Design

This section discusses design and analysis of controller parameters for the suggested control strategy. Voltage gain and output impedance frequency-response are the main guiding tools for the entire design process. Detailed design of the presented VSI system comprises of



(a)



(b)

Figure 3.11 Block schematic (a) Equivalent stationary frame representation of SRF-PI inverter control and (b) Simplified model for voltage control-loop.

determining feedback gain K_c, followed by voltage controller gains K_p and K_i, respectively.

Figure 3.11(a) shows the equivalent model of the inverter control in α–β stationary frame with the capacitor current AD loop. The voltage controller G_v has been replaced by a transfer function $G_{SRF}(s)$ block as obtained in (3.13). The capacitor current feedback gain K_c provides the much needed damping to the lightly damped output LC filter. When the inverter is fully loaded, an additional damping is also presented to the system. However, under light loads i.e., as the load impedance increases, the Phase Margin (PM) and hence, the closed-loop stability gets reduced [179]. Therefore, the voltage controller has been designed at no-load, which is the worst-case scenario for the inverter operation. If the closed-loop control of inverter is observed stable at no-load, conservatively, it may be concluded that the stability would be ensured under all operating conditions.

3.3.4.1 Active Damping Coefficient, K_c

Inclusion of active damping modifies the inverter-plant voltage transfer-function as,

$$G_{pd}(s) = \left.\frac{v_o(s)}{v_i'(s)}\right|_{i_o=0} = \frac{1}{s^2LC + sC(r + K_c) + 1} \tag{3.16}$$

A higher value of damping can be achieved by increasing the value of coefficient, K_c. However, K_c gain should be chosen in an optimised manner to avoid large phase-delay, predominantly near the operating frequency range (which may slow down the dynamic response).

Now, the second-order generalised equation as given in [181] is,

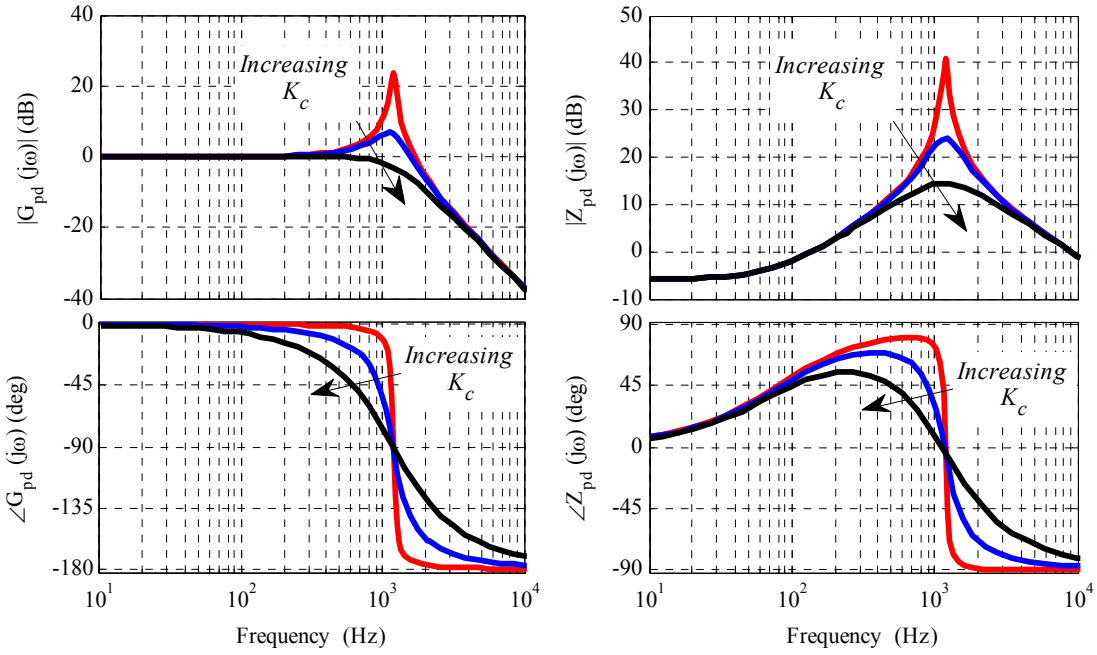
$$G(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.17}$$

where, ω_n is the natural frequency and ζ is regarded as the damping ratio of the system. On comparison of (3.16) with (3.17), following can be deduced:

$$2\zeta\omega_n = \frac{r + K_c}{L} \tag{3.18}$$

where, $\omega_n = \frac{1}{\sqrt{LC}}$. For a given damping ratio (ζ) of the system, damping coefficient K_c may be adjusted using relation (3.19),

$$\zeta = \frac{(r + K_c)}{2}\sqrt{\frac{C}{L}} \tag{3.19}$$



(a) (b)

Figure 3.12 Bode-plot of (a) Voltage gain and (b) Impedance for modified plant with active damping, where $K_c = 0$, 3 and 10.

The variation in resonant peak of G_{pd} with variation in K_c has been shown in Figure 3.12. It also shows the impact of load current on the overall output voltage response through impedance Z_{pd} plot for the modified plant. The impedance of the modified plant is given as,

$$Z_{pd}(s) = \left.\frac{v_o(s)}{i_o(s)}\right|_{v_i'=0} = \frac{1}{s^2LC + sC(r + K_c) + 1} \tag{3.20}$$

For a damping ratio of 0.707, the calculated value of K_c is 10 which is too large than the ESR 'r' and for analytical purpose, it is neglected hereafter for simplicity.

3.3.4.2 Voltage Regulator

Once the damping coefficient K_c is introduced, the plant gain response plot gets modified with the resonant peak clipped off. Next step is to tune the voltage controller, which may be done from the simplified representation of inverter control as in Figure 3.11(b). A perfect output voltage decoupling is assumed here, due to the reference feed-forward path for design simplification. Design of the voltage controller is to determine unknown proportional and integral gains, K_p and K_i, respectively.

Using the output voltage gain transfer function G_{cl}^{SRF} in (3.14), K_p and K_i are obtained on the basis of required close-loop bandwidth ω_{bw} and acceptable steady-state error e_{ss} at the fundamental frequency ω_o. These criteria may be mathematically expressed as

$$\left|G_{cl}^{SRF}\left(j\omega_{bw}\right)\right| = 1/\sqrt{2} \tag{3.21}$$

and,

$$e_{ss} = \left|\frac{v_o^*(s) - v_o(s)}{v_o^*(s)}\right|_{s=j\omega_o} \tag{3.22}$$

Here, K_p is determined assuming integral gain has minimal or almost no effect on the crossover frequency or bandwidth of the voltage controller and hence $K_i = 0$, while applying the criterion of (3.21). However, once the system bandwidth is set, K_p and K_i gains are considered simultaneously to find the steady-state error from (3.22). The choice of system bandwidth has been a trade-off between transient response and the switching noise disturbance rejection. Moreover, higher bandwidth has a better load disturbance blocking capability.

***Proportional Gain*, (K_p)**

The range of frequencies over which the magnitude is equal to or greater than $1/\sqrt{2}$ is defined as the bandwidth ω_{bw} of the controller [181]. Therefore, the closed-loop voltage gain

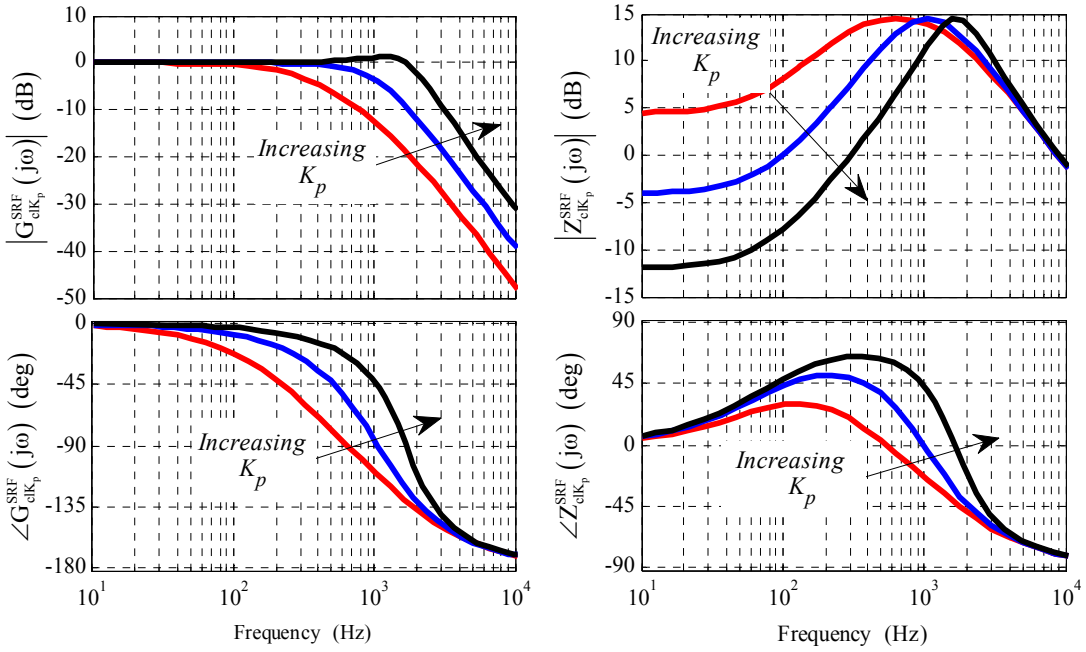


Figure 3.13 Bode-plot (a) Voltage gain (b) Output impedance for proportional gain only, where variation of K_p = 0.3, 0.8 and 2.

of (3.14), on substituting $K_i = 0$, reduces to

$$\left|G_{clK_p}^{SRF}(s)\right|_{K_i=0} = \left|\frac{K_p}{s^2LC + sCK_c + K_p}\right| = \frac{K_p}{\sqrt{\left(K_p - \omega_{bw}^2 LC\right)^2 + \omega_{bw}^2 C^2 K_c^{\,2}}} = \frac{1}{\sqrt{2}} \tag{3.23}$$

Rearranging (3.23), K_p can be computed for a desired bandwidth 'ω_{bw}' from (3.24),

$$K_p = \omega_{bw} C\left(\sqrt{2\omega_{bw}^2 L^2 + K_c^{\,2}} - \omega_{bw} L\right) \tag{3.24}$$

For the design under study, a bandwidth of 1 kHz (6.283 krad/s) is appropriate for both fast dynamics and noise rejection, which results in K_p to be 0.8.

Bode response of voltage gain with only proportional control in Figure 3.13(a) shows that a higher value of K_p increases the system bandwidth (thereby faster response) although, as a consequence, the system also becomes more susceptible to switching noise. In the meanwhile, phase is however observed to be improved, on increasing K_p. Corresponding closed-loop output impedance frequency-plot has been drawn in Figure 3.13(b) using (3.25),

$$Z_{clK_p}^{SRF}(s) = \frac{sL + r}{s^2LC + sCK_c + K_p} \tag{3.25}$$

It shows reduction in the impedance magnitude $|Z_{clKp}|$, as K_p is increased; especially, in the lower order frequency ranges.

Integral Gain, K_i

The integral gain K_i may be obtained by imposing steady-state error criterion of (3.22) and thereafter the resultant relation is given as

$$\begin{aligned} e_{ss} &= \frac{s^2LC + sCK_c}{s^2LC + sCK_c + G_v(s)} \\ &= \frac{\left(s^3 + s^2\omega_o + s\omega_o^2 + \omega_o^3\right)\left(s^2LC + sCK_c\right)}{\left(s^3 + s^2\omega_o + s\omega_o^2 + \omega_o^3\right)\left(s^2LC + sCK_c + K_p\right) + K_i\left(s^2 + 2s\omega_o - \omega_o^2\right)} \end{aligned} \tag{3.26}$$

From (3.26), for a higher value of K_i gain reduces the steady-error however it is limited by the system stability limit. The characteristic polynomial can be derived from the equivalent Figure 3.11 as

$$\begin{aligned} s^5LC + s\left(CK_c + \omega_o LC\right) + s^3\left(\omega_o CK_c + \omega_o^2 LC + K_p\right) + s^2\left(\omega_o^2 CK_c + \omega_o^3 LC + \omega_o K_p + K_i\right) \\ + s\left(\omega_o^3 CK_c + \omega_o^2 K_p + 2\omega_o K_i\right) + \omega_o^3 K_p - \omega_o^2 K_i = 0 \end{aligned} \tag{3.27}$$

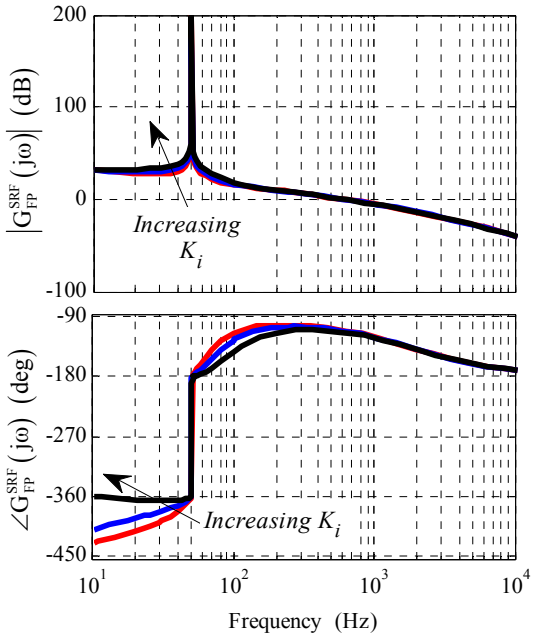


Figure 3.14 Bode-plot for open-loop gain $G_{FP}^{SRF}(s)$ with SRF-PI controller, where K_p = 0.8; K_i = 62, 125 and 250.

Applying, the Routh Hurwitz (RH) criterion of closed-loop stability on (3.27) yields an upper limit for K_i as

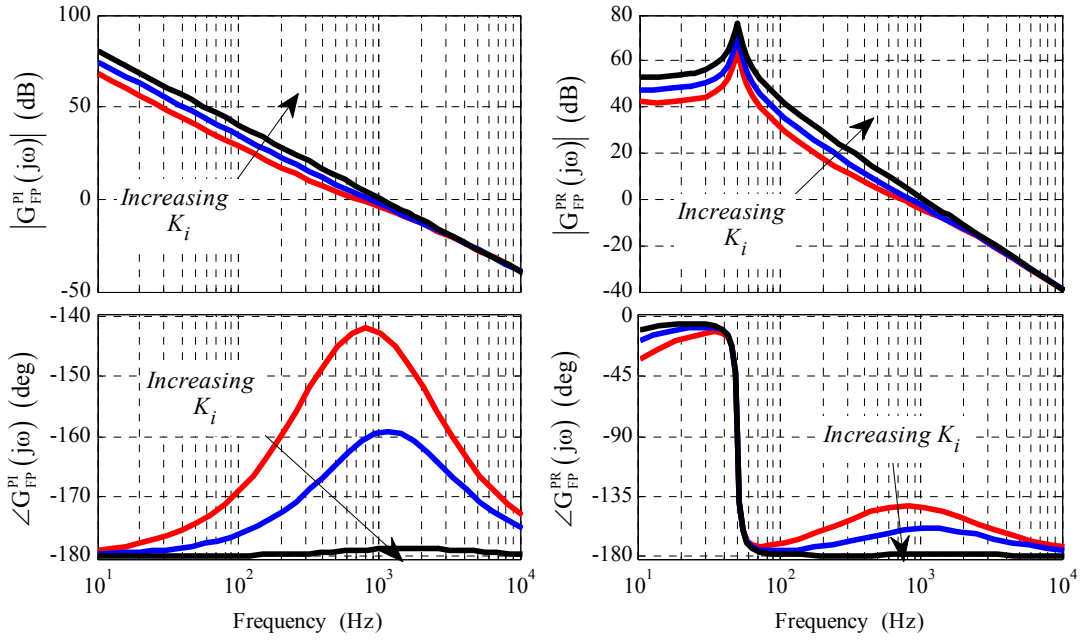
$$K_i < \omega_o K_p \tag{3.28}$$

Practically, it is selected well below the obtained upper limit value to allow safe margin and avoid interference with other frequency components. The stability margin can be better analysed from the open-loop or forward path (in case of unity feedback) transfer function (v_o/v_e), which may be derived from Figure 3.11 (b) as,

$$G_{FP}^{SRF}(s) = \left.\frac{v_o}{v_e}\right|_{i_o=0} = \frac{K_p\left(s^3 + s^2\omega_o + s\omega_o^2 + \omega_o^3\right) + K_i\left(s^2 + 2s\omega_o - \omega_o^2\right)}{\left(s^2LC + sCK_c\right)\left(s^3 + s^2\omega_o + s\omega_o^2 + \omega_o^3\right)} \tag{3.29}$$

The forward path transfer function Bode plot in Figure 3.14 shows that the integral term adds a peak of high amplitude gain at the fundamental frequency ω_o, which is vital for the steady-state error elimination. As K_i value is increased, gain at other frequencies also gets affected. However, PM has almost no variation (which is almost constant, 67° at 630 Hz) up to the stability limit of the integral gain.

The control effort of SRF-PI can be better appreciated on comparison with other integrals such as, PI and PR. The loop transfer function gain may be derived from Figure 3.11 by replacing voltage controller $G_{SRF}(s)$ with $G_{PI}(s)$ and $G_{PR}(s)$ for PI and PR controllers, respectively.



(a) (b)

Figure 3.15 (a) Bode-plot for open-loop gain (a) $G_{FP}^{PI}(s)$ with PI controller where $K_p = 0.8$, $K_i = 2000$, 4000 and 8000; and (b) $G_{FP}^{PR}(s)$ with PR controller where $K_p = 0.8$, $K_i = 100$, 200 and 400.

$$G_{FP}^{PI}(s) = \frac{v_o}{v_e}\bigg|_{i_o=0} = \frac{K_p s + K_i}{\left(s^2 LC + sCK_c\right)s} \tag{3.30}$$

$$G_{FP}^{PR}(s) = \frac{v_o}{v_e}\bigg|_{i_o=0} = \frac{K_p\left(s^2 + 2s\omega_c + \omega_o^2\right) + 2s\omega_c K_i}{\left(s^2 LC + sCK_c\right)\left(s^2 + 2s\omega_c + \omega_o^2\right)} \tag{3.31}$$

Bode plots for the forward path transfer functions can be obtained from (3.30) and (3.31) for PI and PR controllers, respectively. The forward path gain Bode-plot in Figure 3.15 for PI controller shows that K_i increases the magnitude gain linearly, almost in entire frequency spectrum. However, the gain at the tuned fundamental frequency, is only limited which may not be sufficient to eliminate the steady state error. Moreover, PM falls rapidly up to 1° as K_i approaches towards the stability limit of 8000. This justifies the non-preference of the PI control in the stationary frame. The Bode-plot in Figure 3.15(b) shows K_i variation for the practical PR controller with a cut off frequency of ω_c = 5 rad/secs. Although, the fundamental gain is higher than the PI control nevertheless, gain is quite lesser than that of the SRF-PI. Moreover, selectivity is also not as good as SRF-PI control. This is largely due to the non-realisation of the ideal PR control.

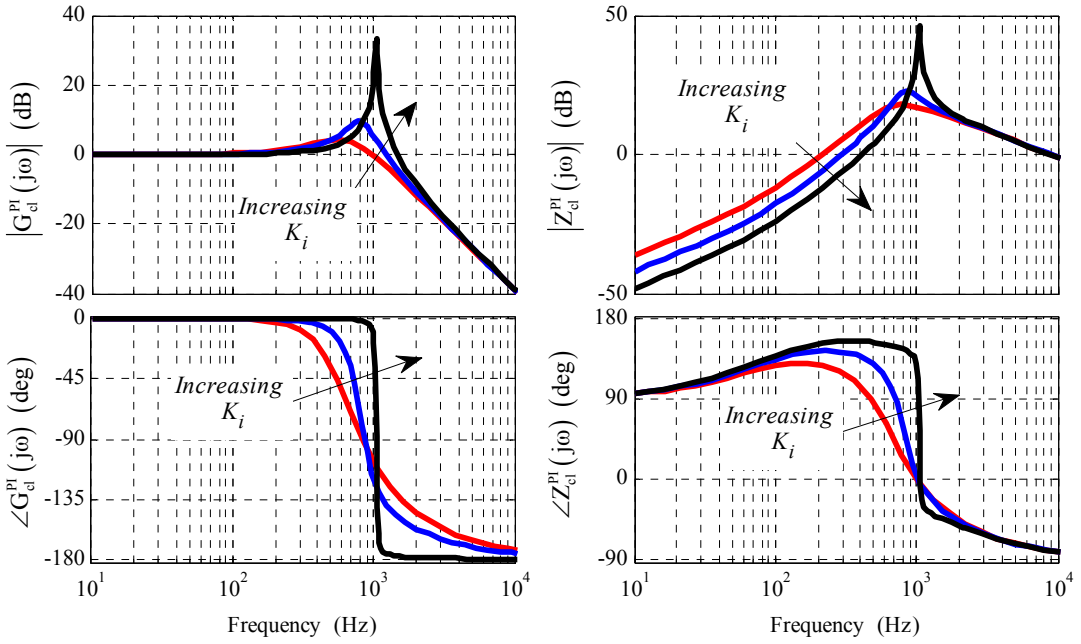


Figure 3.16 Bode-plot for closed-loop (a) Voltage gain and (b) Output impedance with PI controllers, where K_p = 0.8; K_i = 2000, 4000 and 8000.

3.3.4.3 Effect of K_i gain on the close-loop performance of integral controllers

Subsequently, effect of K_i has also been investigated for the closed-loop inverter control, through the Bode response plots of Figure 3.16–Figure 3.18. The close-loop voltage gain and output impedance may be derived from Figure 3.11(b), by replacing the SRF voltage controller with PI and PR controller transfer functions. The respective close-loop voltage gains are

$$G_{cl}^{PI} = \left.\frac{v_o}{v_o^*}\right|_{i_o=0} = \frac{K_p s + K_i}{\left(s^2 LC + sCK_c + K_p\right)s + K_i} \tag{3.32}$$

$$G_{cl}^{PR} = \left.\frac{v_o}{v_o^*}\right|_{i_o=0} = \frac{K_p\left(s^2 + 2s\omega_c + \omega_o^2\right) + 2s\omega_c K_i}{\left(s^2 LC + sCK_c + K_p\right)\left(s^2 + 2s\omega_c + \omega_o^2\right) + 2s\omega_c K_i} \tag{3.33}$$

And, the respective close-loop output impedances of PI and PR controlled inverters may be written as,

$$Z_{cl}^{PI} = \left.\frac{v_o}{i_o}\right|_{v_o^*=0} = \frac{s\left(sL + r\right)}{\left(s^2 LC + sCK_c + K_p\right)s + K_i} \tag{3.34}$$

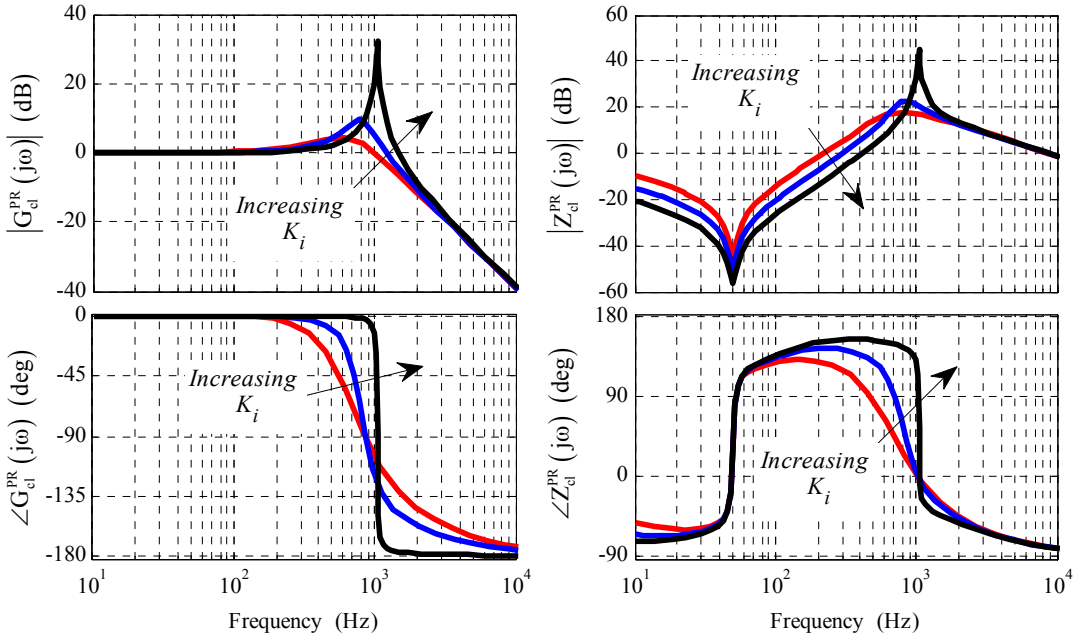


Figure 3.17 Bode-plot for closed-loop (a) Voltage gain and (b) Output impedance using PR control, where K_p = 0.8; K_i =100, 200 and 400.

$$Z_{cl}^{PR} = \left.\frac{v_o}{i_o}\right|_{v_o^*=0} = \frac{\left(s^2 + 2s\omega_c + \omega_o^2\right)\left(sL + r\right)}{\left(s^2 LC + sCK_c + K_p\right)\left(s^2 + 2s\omega_c + \omega_o^2\right) + 2s\omega_c K_i} \tag{3.35}$$

The determination of controller parameters follows the same procedure as for the SRF-PI. In fact, the AD coefficient K_c and the proportional gain K_p are same as before, since PI and PR only alters the integral part of the regulator. Therefore, design of latter regulators requires selection of K_i value, which meets the steady-state error specifications and the stability criterion. More details, regarding design of integral gain K_i for PI and PR controllers have been given in Appendix B.

Figure 3.16 depicts the closed-loop voltage gain G_{cl}^{PI} and output impedance Z_{cl}^{PI} plots for PI based inverter control. As K_i increases, voltage gain magnitude and phase plots improve, however on the verge of stability limit, a high magnitude is observed similar to the under-damped resonant peak. Furthermore, the impedance magnitude plot shows some desirable improvements especially, at lower frequencies which is good on non-linear loads. Again, a high K_i threats system stability around the cut-off frequency.

Close-loop Bode-plots for PR control in Figure 3.17, shows similar variations for voltage gain G_{cl}^{PR} magnitude and phase responses, similar to PI. However, the impedance Z_{cl}^{PR} plot shows a blunt notch at the fundamental frequency in contrary to the PI, where the decline is a

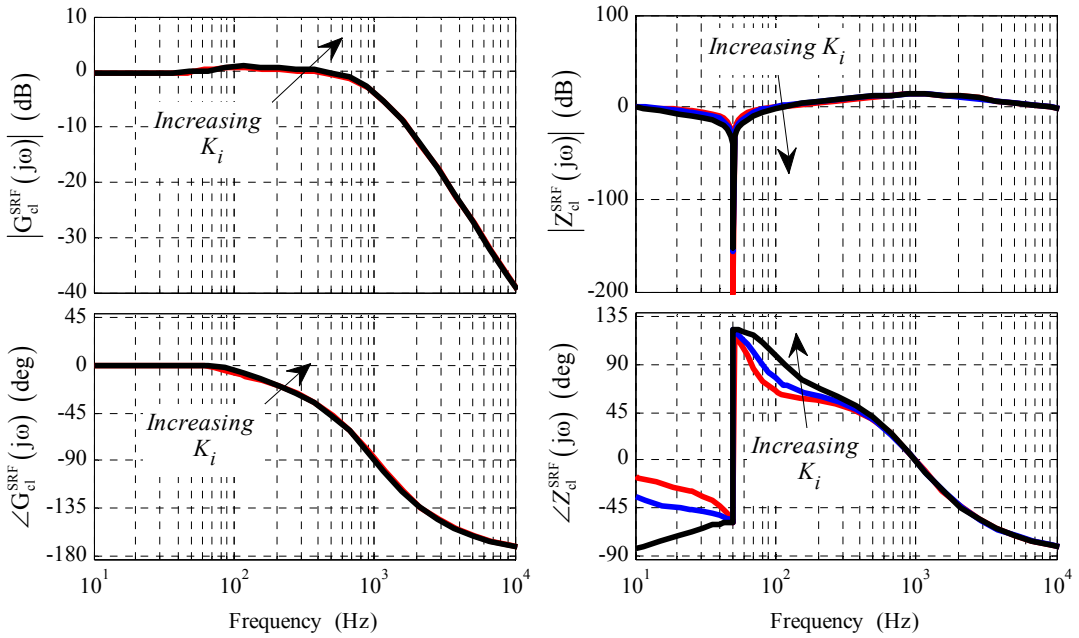


Figure 3.18 Bode-plot for closed-loop (a) Voltage gain and (b) Output impedance using SRF-PI controller, where K_p = 0.8; K_i = 62, 125 and 250.

gradual one. As the stability limit approaches, high peaks are observed in both voltage and impedance plots, with an enhancement in phase response.

Finally, close-loop Bode responses for SRF-PI control are shown in Figure 3.18, which depict the voltage gain, G_{cl}^{SRF} and output impedance, Z_{cl}^{SRF} plots for three different values of K_i within stability limits. The voltage gain magnitude and phase plot do not vary much with K_i. However, some variations in selectivity of the notch around tuned frequency are observed in impedance plots on K_i sweeping. Higher value of K_i may also affect other harmonic orders, which is better for load disturbance rejection. The close-loop output impedance for SRF-PI is obtained from Figure 3.11 and can be written as,

$$Z_{cl}^{SRF} = \frac{v_o}{i_o}\bigg|_{v_o^*=0} = \frac{K_p\left(s^3 + s^2\omega_o + s\omega_o^2 + \omega_o^3\right) + K_i\left(s^2 + 2s\omega_o - \omega_o^2\right)}{\left(s^2LC + sCK_c + K_p\right)\left(s^3 + s^2\omega_o + s\omega_o^2 + \omega_o^3\right) + K_i\left(s^2 + 2s\omega_o - \omega_o^2\right)} \tag{3.36}$$

Preceding analysis shows that a high value of K_i is preferable until it is within safe stability limits. On the other hand, an increase in K_i also affects other frequency components of voltage and impedance gains. Practically, the values are chosen much lower than the stability criterion to give enough space for parameter variations and modelling inaccuracies. In this study, integral gains are selected almost in mid-range value of 4000, 200 and 100 for

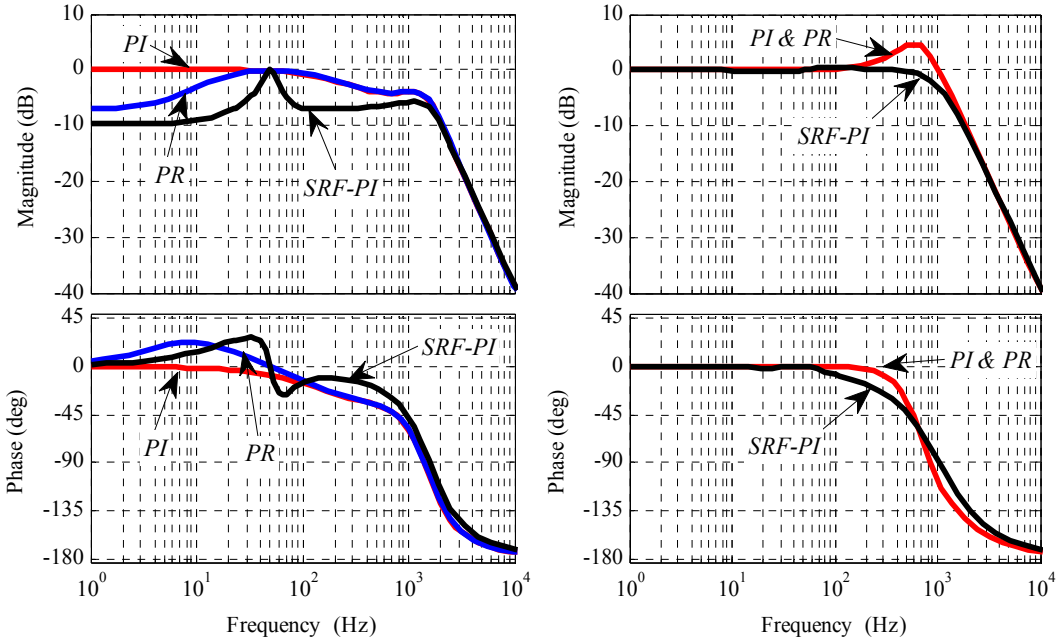


Figure 3.19 Bode-plot for closed-loop Voltage gain (a) without and (b) with voltage feed-forward.

PI, PR and SRF-PI controllers, respectively. SRF-PI clearly shows an edge over the conventional stationary frame integrals; when other control parameters are kept same. The gains are limited of α–β frame, whether been the PI due to its frequency characteristic or the PR because of practical realization. SRF-PI, on the other hand, translates a better gain at fundamental frequency even though the controller is tuned in synchronous d–q frame.

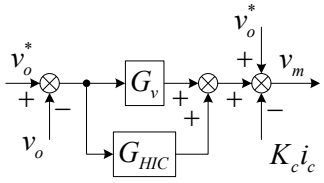
3.3.4.4 Effect of Feed-Forward Compensation

Figure 3.19 (a) and (b) show the Bode-plots of close-loop voltage gains provided by the suggested control structures for PI, PR and SRF-PI controllers, without and with reference voltage feed-forward path. The closed-loop gain is unity (zero dB) only at the fundamental frequency for compensators without feed-forward, whereas the gain is attenuated on both sides of tuned frequency, especially in case of PR and SRF-PI controllers. Although, PI controller with reference feed-forward has unity gain in lower frequencies, it falls down gradually beyond ω_o. The Bode responses in Figure 3.19 (b) clearly show, corresponding control schemes with voltage feed-forward compensation have better gain and bandwidth characteristics. The phase-characteristics particularly in case of PI controller, is also improved with the reference feed-forward.

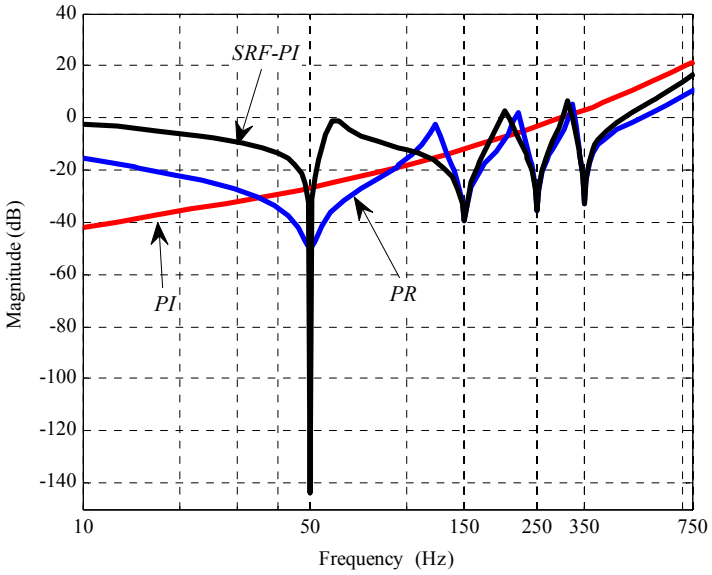
3.3.4.5 Harmonic Impedance Compensation

Non-linear loads draw harmonic currents and consequently, unwanted voltage distortions may appear at the output if the respective harmonic impedance is high. Thus, the effective impedance offered by the close-loop is an important criterion for assessment of the applied control strategy. First few lower order harmonics are more critical and should be kept as low as possible.

With fixed K_p value dictated by bandwidth criterion of (3.21), further reduction of impedance (Z_{cl}) is achieved by K_i gain, although it is designated for a different objective. The impedance magnitude at interested harmonic orders falls considerably for PI control as shown in Figure 3.16 with K_i variation. At the same time, in impedance magnitude plots of SRF-PI of Figure 3.18(b) much variation is not achieved with K_i gain, mainly because of the controllers's selectivity. Therefore, to accomplish lower impedance at harmonic frequencies, multi-compensators tuned for those frequencies can be added to the fundamentally tuned



(a)



(b)

Figure 3.20 (a) Voltage control with Harmonic Impedance Compensation (HIC) and (b) Magnitude bode-plot of Output impedance for respective controllers.

voltage controller, as shown in Figure 3.20 (a). The voltage controller G_v consists of both K_p and K_i terms whereas, the Harmonic Impedance Compensation (HIC) block contains only the integral term whose transfer function is in the following form,

$$G_{HIC}(s) = K_{ih} \sum_{h=3,5,\ldots} \frac{2\omega_c s}{s^2 + 2\omega_c s + (h\omega_o)^2} \tag{3.37}$$

where K_{ih} is the gain of the h^{th} order of harmonic compensator.

The effect of the G_{HIC} control can be better visualized from the closed-loop impedance magnitude-frequency plot in Figure 3.20(b), for PR and SRF-PI controllers. In this plot, harmonic compensators up to 7^{th} order have been used which are sufficient to supress the prominent lower order harmonic distortions of typical UPS application non-linear loads. These compensators introduce troughs at the third, fifth and seventh order harmonics in the controller response apart from the fundamental, for PR and SRF-PI. This greatly reduces the impedance (up to -30dB) and thus, consequent voltage distortions, at these frequencies. On contrary, the impedance of stationary PI, shown for comparison, has gradual increase with frequency.

3.4 Results and Discussions

3.4.1 Simulation Evaluation

Performances of PI, PR and SRF-PI controllers have been extensively investigated on an inverter of 250 VA, 80V, 50 Hz, whose system parameters are tabulated in Table 2.1. The controller parameters are given in Table D.3 of Appendix D. Simulations have been performed in MATLAB DTF environment to emulate digital implementation of the experimental hardware setup. The discrete time transfer characteristics of controllers are obtained through Zero-Order Hold (ZOH) method of discretization with a sampling frequency of 10 kHz. In computer-controlled systems, there is always a transportation lag or time delay due to digital sampling, numerical computation time or PWM updates execution. A time lag or delay of 't_d' seconds corresponds to the transfer function e^{-st_d} in the Laplace transform. In the frequency domain, $e^{-\hat{i}\omega t_d} = 1\angle -\omega t_d$ i.e., the magnitude is unity for all values of ω whereas the phase of the time delay term falls smoothly with frequency. The effective phase plot is obtained by subtracting $-\omega t_d$ rad from the phase curve of open loop $G_{FP}(s)$ for entire ω. As a result, this reduces the PM of the overall system, which degrades the control loop performance and may even threat stability. Though it is needed to include a time delay effect, it may not be always convenient in control loop modelling and design. Rather, an analysis of the PM (since time delays introduce phase lag only) may be sufficient before the design

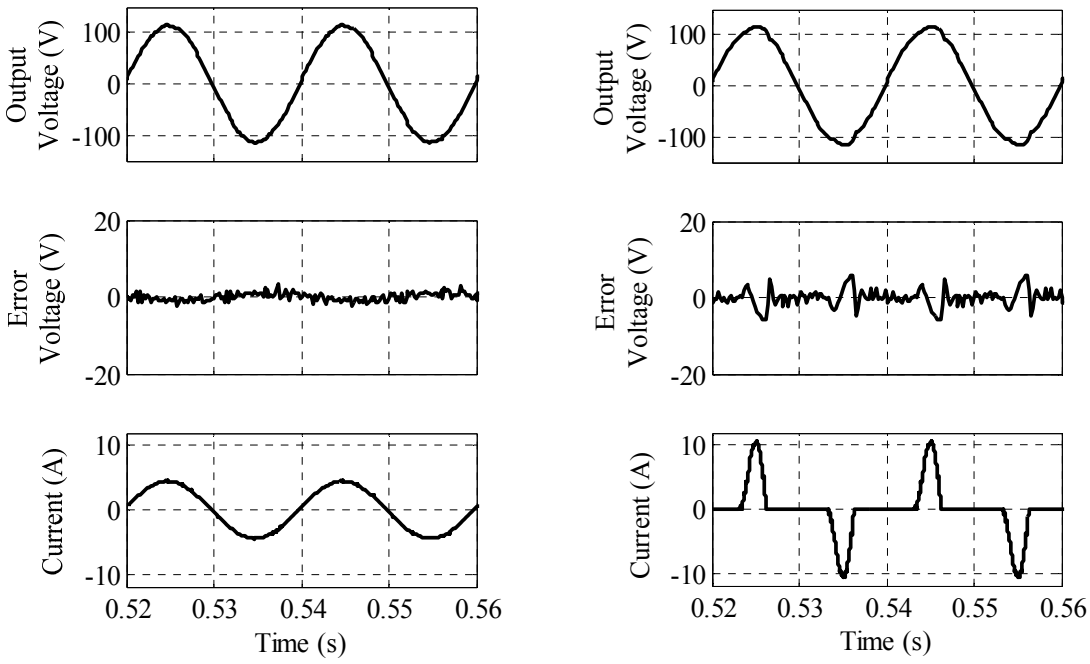
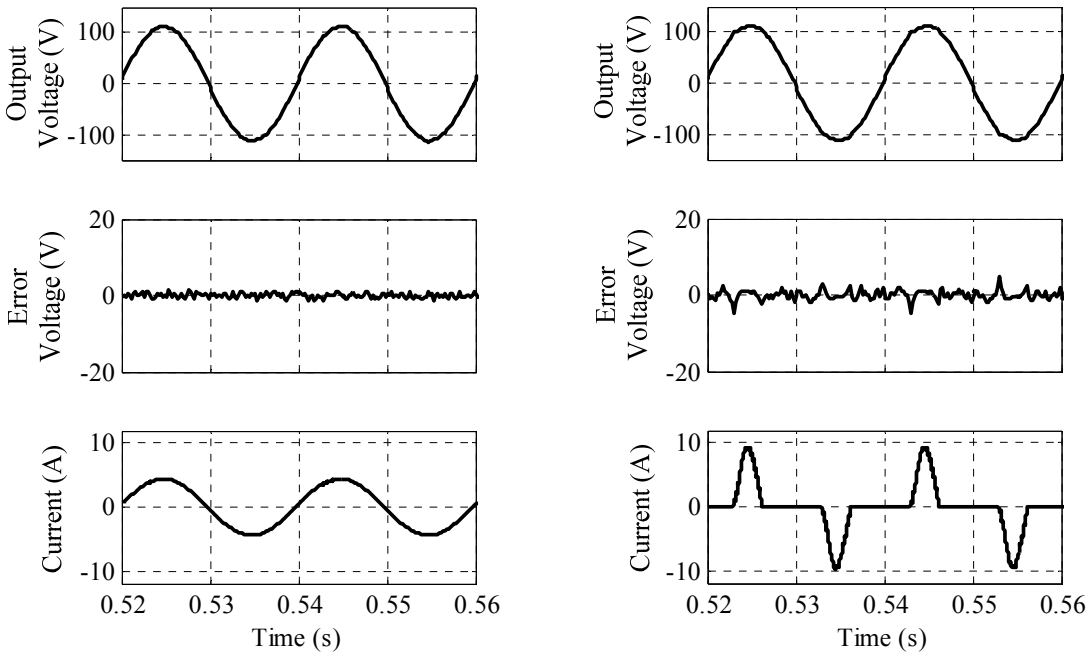


Figure 3.21 Simulated steady-state waveforms using PI voltage controller under rated (a) Linear and (b) Non-linear load.

finalization. For an example, a time delay of one switching period reduces the PM to 45° for SRF-PI with a crossover frequency of the $G_{FP}^{SRF}(s)$ at f_c = 630 Hz in Figure 3.14. The reduced PM is still sufficient to ensure the stability of the overall system. If the PM had not been adequate, the integral gain K_i may be reduced to improve the PM, as clear from Figure 3.14-15, for accommodating the extra phase lag of the time delays.

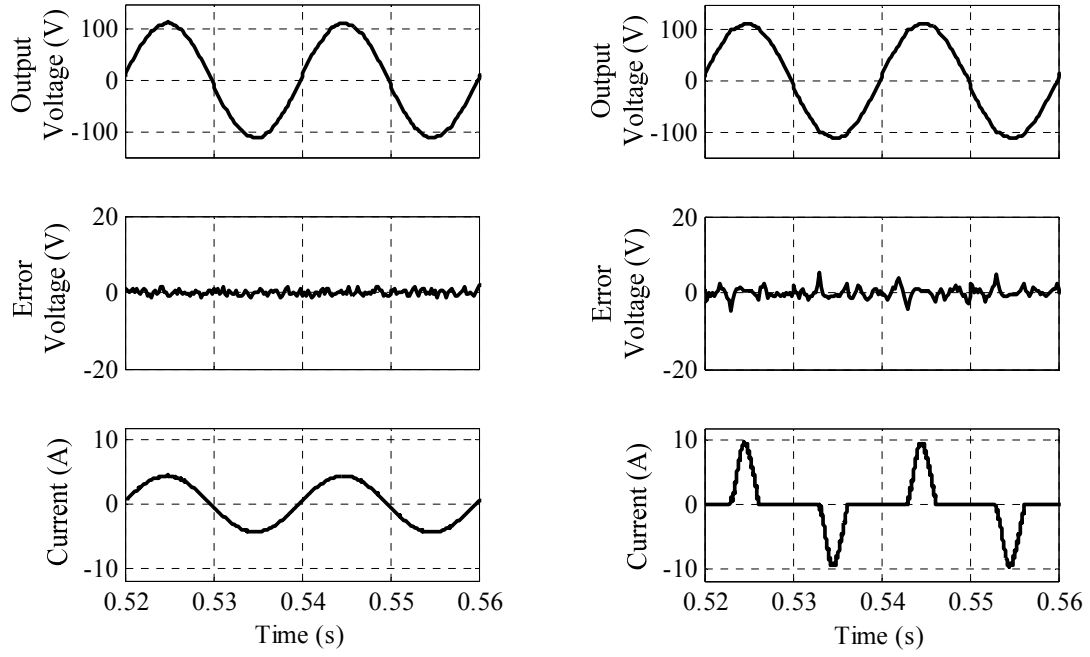
First, steady state performance under linear resistive loading condition has been examined for the controllers. Figure 3.21(a),Figure 3.22(a) and Figure 3.23(a) show the simulated response of output voltage, voltage tracking error and load current for inverter using PI, PR and SRF-PI voltage controllers, respectively. The adopted control scheme shows good voltage waveform on linear loading, though PI controller has some voltage error (1.3 V), PR and SRF-PI have almost negligible tracking error in steady state.

Next, non-linear loading condition has been performed on inverter, where load used consists of a diode rectifier bridge followed by a DC capacitor in parallel with a resistance. Large voltage error has been observed in case of PI control on steady state load. The superiority of the voltage waveforms in PR and SRF-PI over PI control is clearly visible from Figure 3.21(b), Figure 3.22(b) and Figure 3.23(b).



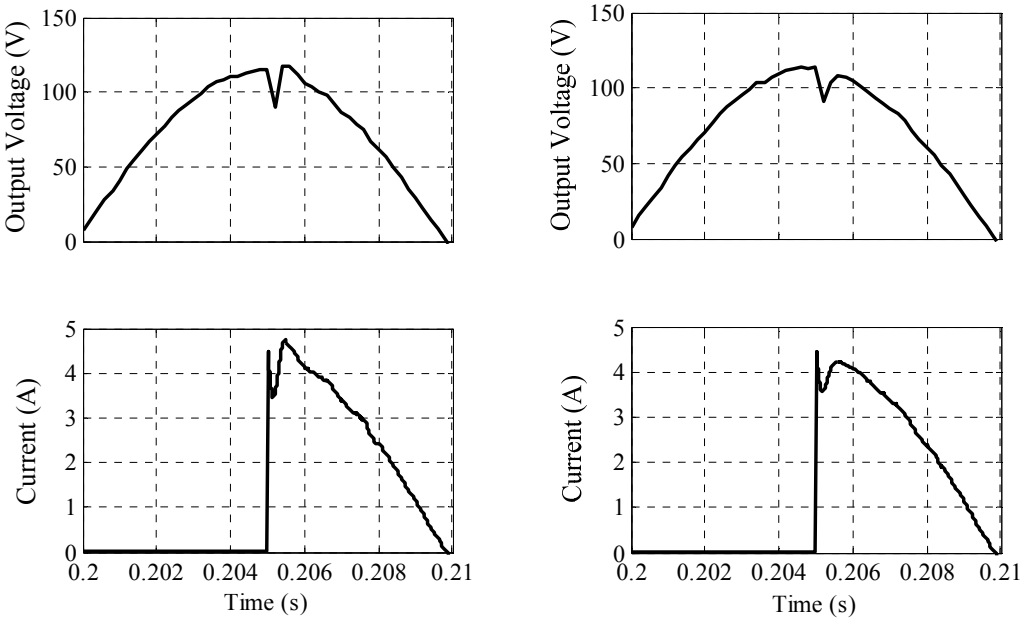
(a) (b)

Figure 3.22 Simulated steady-state waveforms using PR voltage controller under rated (a) Linear and (b) Non-linear load.



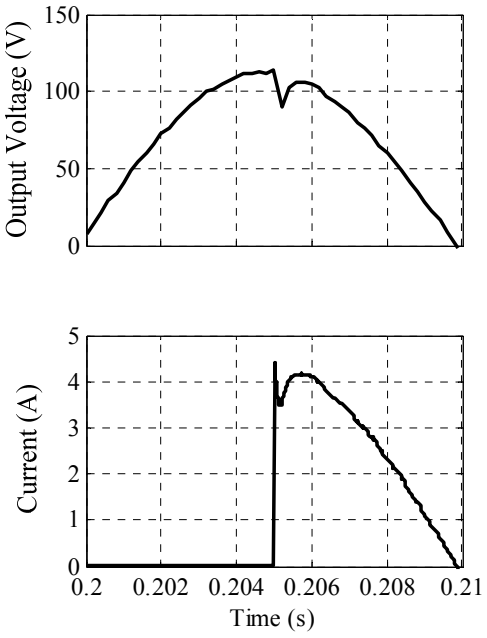
(a) (b)

Figure 3.23 Simulated steady-state waveforms using SRF-PI voltage controller under rated (a) Linear and (b) Non-linear load.



(a)

(b)



(c)

Figure 3.24 Simulated transient response on step-load application from no-load to full-load using (a) PI, (b) PR and (c) SRF-PI voltage controller.

Table 3.6 Steady-state performance comparison

	LINEAR LOAD			NON–LINEAR LOAD		
	PI	**PR**	**SRF-PI**	**PI**	**PR**	**SRF-PI**
%THD	1.20	1.00	1.00	3.80	2.40	2.40
% Error	1.63	0.88	0.88	4.00	1.83	1.63

Note: % Error =100 x $(v_o^* - v_o)/v_o^*$

The simulated results have been quantified in terms of % THD content in the load voltage and voltage tracking error with respect to the reference value (% Error) on loading. The performance comparison data is tabulated in Table 3.6. The SRF-PI based voltage controller has significant perfomance improvement over the stationary frame PI controller and relatively better than the PR controller.

In another study, transient performance of voltage controllers on step load application, from no-load to full load, has been investigated and the consequent results are shown in Figure 3.24. Since proportional control gain is same for all the controllers, no significant variations in transient condition has been observed.

3.4.2 Experimental Results

A single-phase digitally controlled UPS inverter has been experimentally set up to investigate the performance of various controllers. Figure 3.25 shows the block schematic layout of the experimental setup based on TMS320F2812 DSP controller. An inverter module (SEMIKRON make) consisting of a front-end diode-rectifier (uncontrolled AC-DC), a DC link capacitor and an IGBT full-bridge inverter (DC-AC) with mounted gate drivers has been

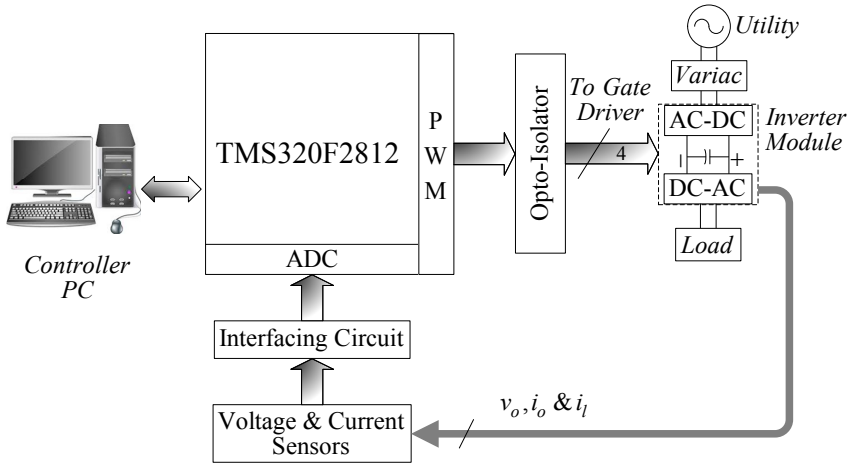
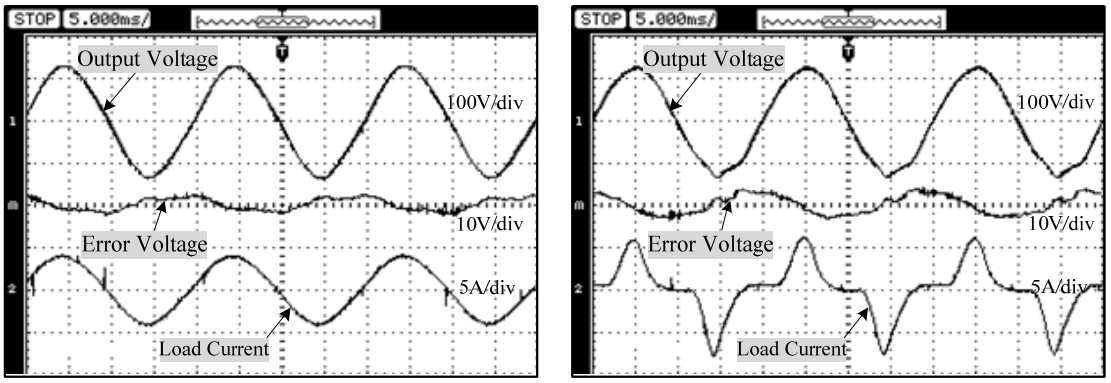


Figure 3.25 Schematic of the TMS320F2812 DSP based Experimental Set-up.

put to use. The module was connected to supply through a single-phase Variac to control the DC-link capacitor voltage. A suitable specification of 250 VA, 80 V, 50 Hz for inverter module has been selected looking into the laboratory limitation constraints for prototype implementation. Experimental results were obtained for both linear and non-linear loads, former being a simple resistive load and the latter comprised of a single-phase diode bridge rectifier feeding a RC load as dictated by IEC62040-3 standard for UPS. The linear load was 25 Ω and the non-linear load had a series bridge resistance of 1 Ω and R and C values of 57 Ω and 2598 μF, respectively as given in Appendix D.

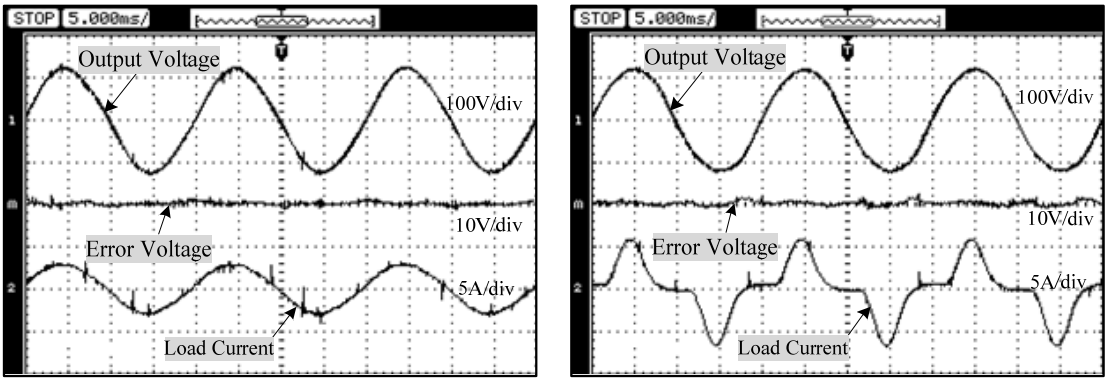
Three signals from inverter module were sensed, out of which, one was output voltage and other two were inductor and load currents respectively. The capacitor current was obtained by the difference of inductor and load current for the control scheme implementation. Current feedbacks were obtained using TELCON-HTP25 Hall-effect current sensors, while voltage was sensed using AD202-JN isolation amplifier. The sensed signals were bi-polar voltages in the range of ±5 V. These signals were converted to uni-polar 0-3 V level using an Op-amp based conditioning and interface circuit, before feeding to the 12-bit ADC channels of the DSP. The sequential sampling frequency of ADC was kept same as that of the switching frequency of the inverter at 10 kHz and the ADC conversion period was 80 ns. All signals were sampled at underflow of GP Timers at the starting of each PWM period, to have maximum time for the control loop computations. The control loop was operated at the ADC sampling frequency for duty cycle update of the inverters. The generated PWM pulses from TMS320F2812 DSP were fed to the gate drivers of the IGBT switches through 6N136 opto-coupler based isolation circuit.

Firstly, steady-state performance of respective controllers has been investigated for both



(a) (b)

Figure 3.26 Experimental steady-state waveforms with PI voltage controller under rated (a) Linear and (b) Non-linear load.

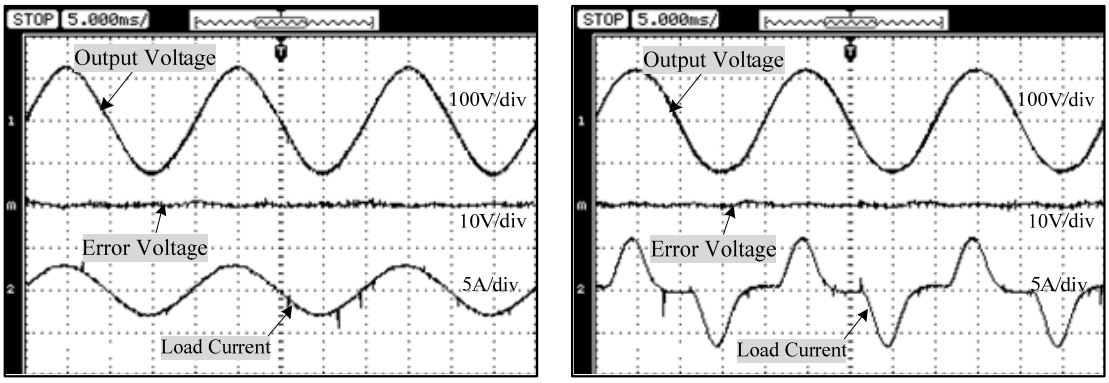


(a) (b)

Figure 3.27 Experimental steady-state waveforms with PR voltage controller under rated (a) Linear and (b) Non-linear load.

rated linear and non-linear loads. The tracking error for PI controller has been observed larger in comparison to PR and SRF-PI as illustrated in Figure 3.26–Figure 3.28. The voltage error in PI control is as high as 5 V (peak to peak) on non-linear loads. Steady state load voltage and voltage tracking error is depicted in Figure 3.27 and Figure 3.28 for PR and SRF-PI shows responses under non-linear loading are as good as their respective linear loads. On close observation, it may be found that PR based voltage control has inferior performance than the SRF-PI, which may be largely attributed to practical implementation issues.

Figure 3.29 shows the output voltage and load current waveforms for a step change in resistive load from zero to rated value with PI, PR and SRF-PI voltage controllers. The turn-on transient responses are in validation with the simulation results, with similar responses for the three controllers.



(a) (b)

Figure 3.28 Experimental steady-state waveforms with SRF-PI voltage controller under rated (a) Linear and (b) Non-linear load.

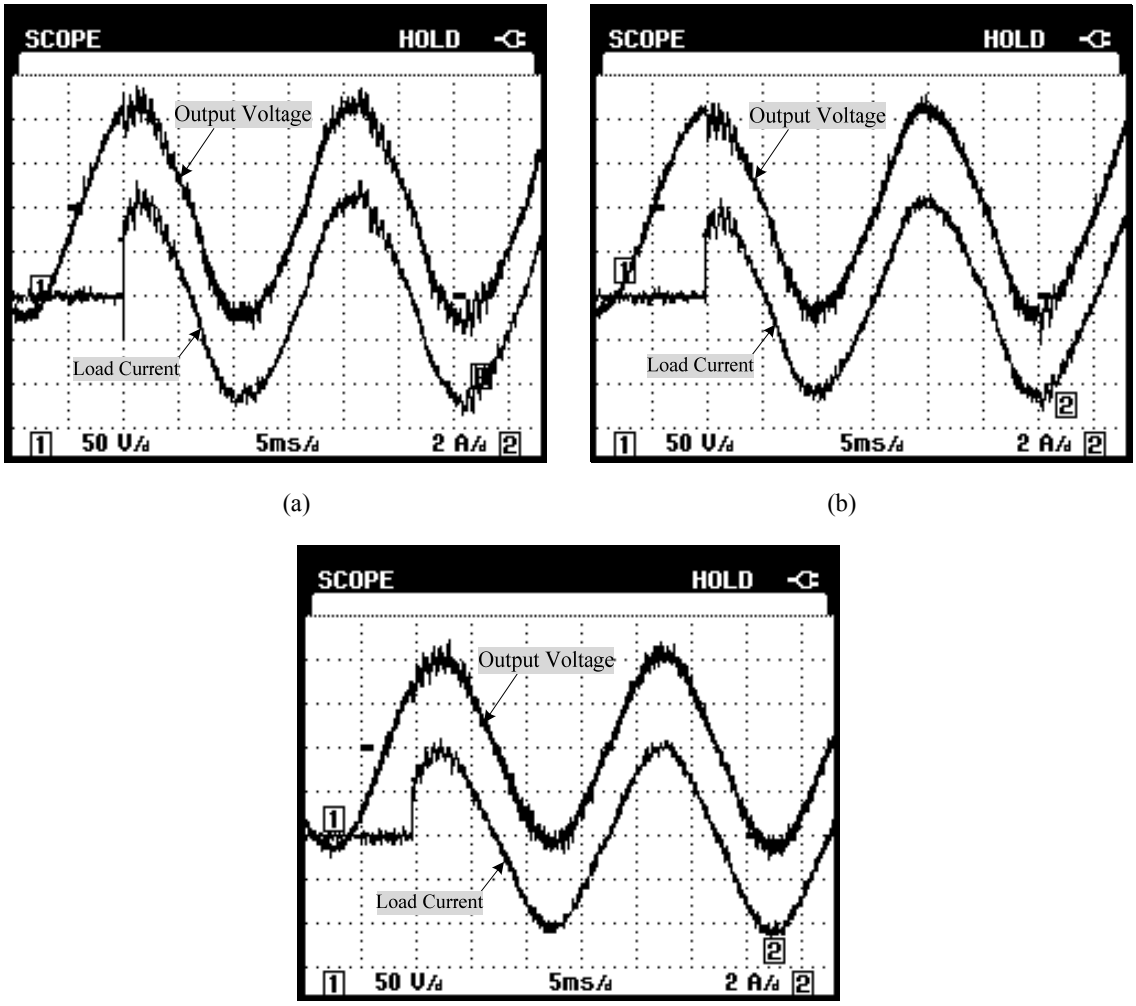


Figure 3.29 Experimental transient response on step-load application from no-load to full-load using (a) PI, (b) PR and (c) SRF-PI voltage controller.

3.5 Summary

This chapter categorises UPS inverter instantaneous control structures and illustrates the fundamental reason for differences in performance between them. While various control topologies using output voltage, capacitor current, inductor current or load current have been investigated, voltage-mode capacitor current feedback scheme proves to be a better alternative. The capacitor current provides required AD and thus has an excellent performance for both transient and steady state conditions, particularly on non-linear loads.

Later, an instantaneous voltage-mode capacitor current feedback scheme has been suggested for single-phase UPS inverter in combined reference frame. In this strategy, only voltage regulator is implemented in the synchronous frame, whereas the remaining part of the

control scheme is in the stationary frame. Subsequently, an equivalent stationary frame model of SRF-PI voltage regulator has been derived. In this way, the entire control scheme may be represented in stationary reference frame, which not only results in a generalised voltage-mode control structure but also simplifies the control analysis. Further, capacitor current feedback has been employed for the AD and reference voltage feedforward has been utilised for better robustness of the control scheme.

Considering generalised voltage-mode control structure as base, a systematic design procedure and analysis has been suggested for three integral controllers namely PI, PR and SRF-PI. This may be done by simply replacing voltage controller by PI, PR and SRF-PI, alternately. The proportional gain for the three controllers come out to be the same for equal control bandwidth, and only the integral gain varies, depending on the stability criterion. The steady-state performance of SRF-PI is concluded to be the better than PR and PI. The main reason for this is limited gain of the PI and practical realisation difficulty of the ideal PR. However, the transient conditions do not show such variations as it primarily depends on the proportional gain, which is same for all the three controllers. These conclusions are supported by the experimental confirmation on a single-phase UPS inverter prototype using TMS320F2812 DSP controller.

CHAPTER 4: INSTANTANEOUS AVERAGE CURRENT FEED-FORWARD CONTROL FOR EQUAL LOAD SHARING IN PARALLEL-CONNECTED UPS INVERTER SYSTEM

4.1 Introduction

Rising power demand of Uninterruptible Power Supplies (UPS) system urges paralleling of several inverter modules for feeding critical loads. Present chapter explores the effect of various available controls and controller of a unit inverter module on parallel operation and suggests a way to improve them for parallel-connection. The comprehensive study includes circulating current impedance modelling of these control topologies and detailed analysis of their immunity to circulating current are presented in sequent. Thereafter, modification in the existing control topology is proposed to enable the inverters for parallel connections and have proper current sharing under different conditions. Further, the effect of voltage controller on circulating currents is investigated, followed by a suggested solution. Design and analysis of the proposed control scheme is validated through MATLAB/Simulink simulations and practical implementation on TMS320F2812 DSP platform, using two parallel-connected inverters.

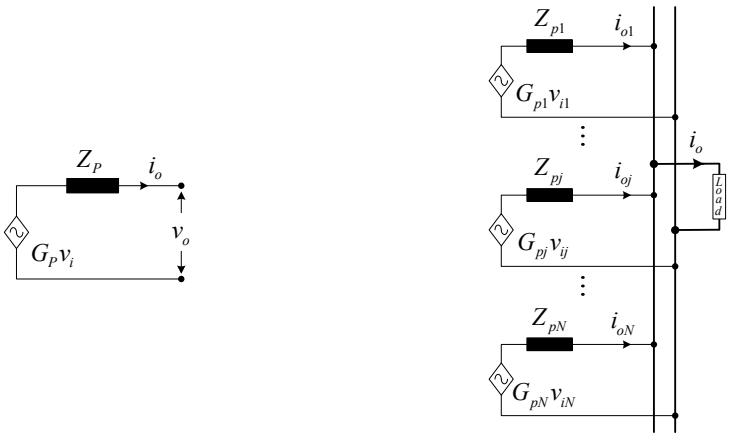
4.2 Modelling and Analysis of Circulating Current for UPS Inverters Connected in Parallel

4.2.1 Open-Loop Inverter System

The output voltage of an inverter plant as derived Figure 2.2 may be stated as:

$$\begin{aligned} v_o(s) &= \frac{1}{s^2LC + srC + 1} v_i(s) - \frac{sL + r}{s^2LC + srC + 1} i_o(s) \\ &= G_p(s) v_i(s) - Z_p(s) i_o(s) \end{aligned} \tag{4.1}$$

where, $G_p(s) = 1/\left(s^2LC + srC + 1\right)$ and $Z_p(s) = \left(sL + r\right)/\left(s^2LC + srC + 1\right)$. Using (4.1), an inverter may be represented by a Thevenin's equivalent circuit, as shown in Figure 4.1 (a). 'G_pv_i' and 'Z_p' are open-circuit voltage and output impedance, respectively for the open-loop inverter plant.



(a) (b)

Figure 4.1 Open-loop equivalent circuit of (a) Unit inverter and (b) '*N*' inverter modules connected in parallel.

The power rating of an UPS system may be enhanced by adding similar inverter modules in parallel. The equivalent circuit configuration for '*N*' inverters connected in parallel is as shown in Figure 4.1(b). The line impedances of connectors can be presumed negligible since inverters are placed closely [4]. Therefore, any two inverters are separated by an impedance of approximately '$2Z_p$' (considering equal Z_p), which is typically too low to limit the current if a voltage deviation exists between them. Therefore, inverter output current for the j^{th} module i_{oj}, comprises of corresponding load current and inter modular circulating current between inverters. The present sub-section presents the concept of circulating current and its subsequent mathematical analysis.

From (4.1), the output voltage of each module in parallel system can be written as:

$$\begin{aligned} v_o(s) &= G_{p1}(s)v_{i1}(s) - Z_{p1}(s)i_{o1}(s) \\ &\vdots \\ v_o(s) &= G_{pj}(s)v_{ij}(s) - Z_{pj}(s)i_{oj}(s) \\ &\vdots \\ v_o(s) &= G_{pN}(s)v_{iN}(s) - Z_{pN}(s)i_{oN}(s) \end{aligned} \tag{4.2}$$

Assuming circuit parameters to be consistent, $G_{p1} = \cdots = G_{pj} = \cdots = G_{pN} = G_p$ and $Z_{p1} = \cdots = Z_{pj} = \cdots = Z_{pN} = Z_p$. Thus, aggregate output voltage of the complete parallel system is obtained by summing all the voltages of (4.2) as

$$\begin{aligned} v_o(s) &= G_p(s)v_{iav}(s) - Z_p(s)i_{oav}(s) \\ \text{where, } v_{iav} &\triangleq \sum_{j=1}^{N} v_{ij} \Big/ N \text{ and } i_{oav} \triangleq \sum_{j=1}^{N} i_{oj} \Big/ N. \end{aligned} \tag{4.3}$$

Now, the j^{th} module circulating current of M-M inverter system is defined in [161], [182] as:

$$i_{crj}(s) = i_{oav}(s) - i_{oj}(s) \tag{4.4}$$

Therefore, using (4.2) and (4.3) in (4.4), I-M circulating current for the j^{th} module may be obtained:

$$i_{crj}(s) = \frac{G_p(s)}{Z_p(s)}\left[v_{iav}(s) - v_{ij}(s)\right] \tag{4.5}$$

Henceforth, the impedance offered to the circulating current by the j^{th} module may be obtained as,

$$Z_{crj}(s) = \frac{Z_p(s)}{G_p(s)} = sL + r \tag{4.6}$$

From the above analysis, it becomes clear that the filter inductor primarily provides impedance to the circulating current. However, good voltage regulation and harmonics disturbance rejection specify the filter impedance to be kept on the lower side. As a consequence, this will contribute to a large circulating current among parallel connected inverters. Therefore, the conflicting requirements draw attention towards a specialised control scheme to meet the objectives of parallel connection.

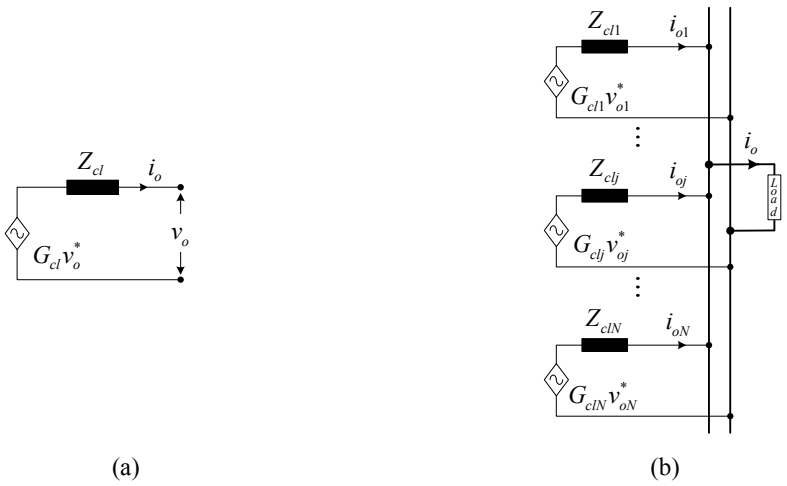
4.2.2 Closed-Loop Inverter Control Topologies and Circulating Current Impedances

For improvement in performance, close-loop feedback control is usually employed for the inverters in UPS. The inverter output voltage under close-loop control may be expressed as:

$$v_o(s) = G_{cl}(s)v_o^*(s) - Z_{cl}(s)i_o(s) \tag{4.7}$$

where, $G_{cl}(s)v_o^*(s)$ and $Z_{cl}(s)$ are the open-circuit voltage and output impedance of Thevenin's equivalent circuit for the inverter with close-loop control, respectively. Thevenin's equivalent circuit for the unit inverter with close-loop control is shown in Figure 4.2 (a). In order to enhance power rating, corresponding close-loop equivalent circuit of '*N*' inverters connected in parallel configuration is shown in Figure 4.2 (b).

From (4.7), the close-loop output voltage of each module in parallel system may be written as:



(a) (b)

Figure 4.2 Closed-loop equivalent circuit of (a) Unit inverter and (b) '*N*' inverter modules connected in parallel.

$$\begin{aligned} v_o(s) &= G_{cl1}(s)v_{o1}^*(s) - Z_{cl1}(s)i_{o1}(s) \\ &\vdots \\ v_o(s) &= G_{clj}(s)v_{oj}^*(s) - Z_{clj}(s)i_{oj}(s) \\ &\vdots \\ v_o(s) &= G_{clN}(s)v_{oN}^*(s) - Z_{clN}(s)i_{oN}(s) \end{aligned} \tag{4.8}$$

Assuming circuit parameters to be consistent, $G_{cl1} = \cdots = G_{clj} = \cdots = G_{clN} = G_{cl}$ and $Z_{cl1} = \cdots = Z_{clj} = \cdots = Z_{clN} = Z_{cl}$. Thus, aggregate output voltage of the complete parallel system is obtained by summing all the voltages of (4.8) as

$$\begin{aligned} v_o(s) &= G_{cl}(s)v_{oav}^*(s) - Z_{cl}(s)i_{oav}(s) \\ \text{where, } v_{oav}^*(s) &\triangleq \sum_{j=1}^{N} v_{oj}^*(s) \Big/ N \end{aligned} \tag{4.9}$$

Using(4.8) and(4.9) in (4.4), circulating current for the j^{th} module may be obtained as

$$i_{crj}(s) = \frac{G_{cl}(s)}{Z_{cl}(s)}\left[v_{oav}^*(s) - v_o^*(s)\right] \tag{4.10}$$

Henceforth, the circulating current for the j^{th} module is generated due to difference in the average reference voltage of '*N*' modules and the reference voltage applied to the j^{th} module. Therefore, the I-M circulating current impedance for the j^{th} module may be expressed as,

$$Z_{crj}(s) = \frac{Z_{cl}(s)}{G_{cl}(s)} \tag{4.11}$$

Table 4.1 Transfer functions of various control topologies

Control Topology	***Voltage Gain*** (G_{cl})	***Output Impedance*** (Z_{cl})	***Circulating Current Impedance*** (Z_{cr})
SLVM	$\frac{G_v(s)}{\sigma(s)+G_v(s)}$	$\frac{sL+r}{\sigma(s)+G_v(s)}$	$\frac{sL+r}{G_v(s)}$
VMC	$\frac{G_v(s)}{\sigma(s)+sCK_c+G_v(s)}$	$\frac{sL+r}{\sigma(s)+sCK_c+G_v(s)}$	$\frac{sL+r}{G_v(s)}$
VMI	$\frac{G_v(s)}{\sigma(s)+sCK_l+G_v(s)}$	$\frac{sL+r+K_l}{\sigma(s)+sCK_l+G_v(s)}$	$\frac{sL+r+K_l}{G_v(s)}$
CMC	$\frac{G_v(s)G_c(s)}{\sigma(s)+sCG_c(s)+G_v(s)G_c(s)}$	$\frac{sL+r}{\sigma(s)+sCG_c(s)+G_v(s)G_c(s)}$	$\frac{sL+r}{G_v(s)G_c(s)}$
CMI	$\frac{G_v(s)G_c(s)}{\sigma(s)+sCG_c(s)+G_v(s)G_c(s)}$	$\frac{sL+r+G_c(s)}{\sigma(s)+sCG_c(s)+G_v(s)G_c(s)}$	$\frac{sL+r+G_c(s)}{G_v(s)G_c(s)}$
CMIL	$\frac{G_v(s)G_c(s)}{\sigma(s)+sCG_c(s)+G_v(s)G_c(s)}$	$\frac{sL+r}{\sigma(s)+sCG_c(s)+G_v(s)G_c(s)}$	$\frac{sL+r}{G_v(s)G_c(s)}$

Note: $\sigma(s)=s^2LC+srC$

Table 4.1shows the transfer functions for various control topologies discussed previously in chapter 3. On substituting the close-loop voltage gain, G_{cl} and close-loop output impedance, Z_{cl} of SLVM from Table 4.1 in (4.11), results

$$Z_{crj}(s)=\frac{sL+r}{G_v(s)} \tag{4.12}$$

The gain of voltage controller $G_v(s)$ is generally high for good voltage regulation and harmonics disturbance rejection. On comparison of (4.6) and (4.12), $|Z_{cr}(s)|_{close\text{-}loop} \ll |Z_{cr}(s)|_{open\text{-}loop}$ due to a large $|G_v(s)|$. Therefore, the circulating current impedance of the inverter falls dramatically under close-loop, which is even less than open-loop inverter and calls an appropriate action. Derivations on similar lines give the circulating current impedance of the various control topologies, which are tabulated in Table 4.1. As an illustration, the I-M circulating current impedance frequency response for various control topologies has been plotted in Figure 4.3. The voltage controller $G_v(s)$ used herein is PR type and current controller $G_c(s)$ is P-type. The parameters used for the plot are given in Table D.4 of Appendix D. The plot clearly shows a sharp reduction in magnitude of Z_{cr} on close-loop control of inverters, particularly at the fundamental frequency. Circulating current impedances

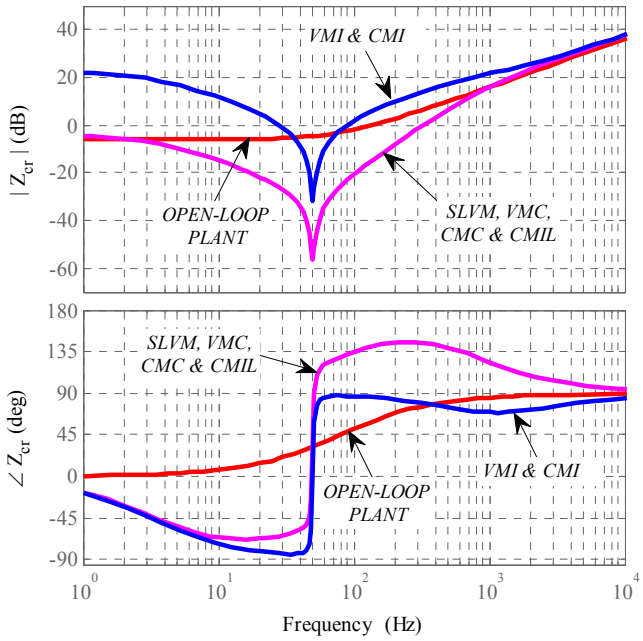


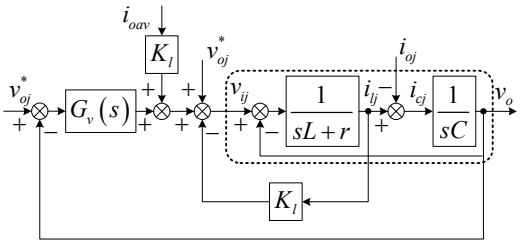
Figure 4.3 Circulating current impedance for various control topologies.

for inductor current feedbacks are relatively higher than that of capacitor current feedbacks for both voltage and current control modes. However, Z_{cr} for VMI and CMI control topologies is still lower than the open-loop inverter plant. Moreover, the output impedances of VMI and CMI are observed to be higher as seen from Table 4.1, which eventually deteriorates the output voltage.

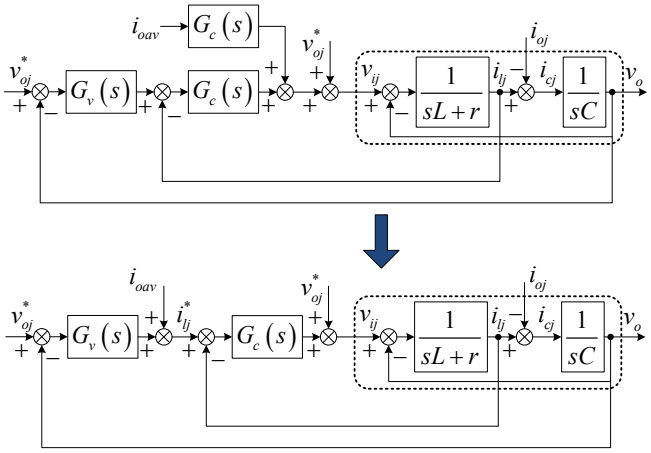
4.3 Development of Instantaneous Average Current Feed Forward (IACFF) Control

The circulating current impedance offered by multi-loop inductor current feedbacks is definitely higher than the other control schemes but certainly not without a larger output impedance. CMIL hints towards a possible way to exclude the additional K_l or $G_c(s)$ term from the output impedance expression. However, that will also decrease the circulating current impedance as enlisted in Table 4.1. The following subsequent analysis leads to a novel technique that increases the circulating current impedance without affecting the output impedance. Output voltages for VMI and CMI schemes using (4.8) and Table 4.1 may be expressed as:

$$\begin{aligned} v_o(s) &= G_{cl}^{VM}(s)v_{oj}^*(s) - Z_{cl}^{VM}(s)i_{oj}(s)\cdots(a) \\ v_o(s) &= G_{cl}^{CM}(s)v_{oj}^*(s) - Z_{cl}^{CM}(s)i_{oj}(s)\cdots(b) \end{aligned} \tag{4.13}$$



(a)



(b)

Figure 4.4 Modified multi-loop inductor current feedback with IACFF control strategy (a) Voltage mode and (b) Current mode with its reduced model.

Since $i_{oav}(s) \triangleq i_{oj}(s) + i_{crj}(s)$, (4.13) can be rearranged as,

$$v_o(s) = G_{cl}^{VM} v_{oj}^*(s) - \frac{sL+r}{D_{VM}(s)} i_{oj}(s) - \frac{K_l}{D_{VM}(s)} \left[i_{oav}(s) - i_{crj}(s) \right] \cdots (a)$$

$$v_o(s) = G_{cl}^{CM}(s) v_{oj}^*(s) - \frac{sL+r}{D_{CM}(s)} i_{oj}(s) - \frac{G_c(s)}{D_{CM}(s)} \left[i_{oav}(s) - i_{crj}(s) \right] \cdots (b) \quad (4.14)$$

where $D_{VM}(s) = s^2LC + s(r+K_l)C + G_v(s)$ and $D_{CM}(s) = s^2LC + s(r+G_c(s))C + G_v(s)G_c(s)$. Adding, $K_l i_{oav}(s)/D_{VM}(s)$ and $G_c(s) i_{oav}(s)/D_{CM}(s)$ in (4.14) gives;

$$v_o(s) = G_{cl}^{VM}(s) v_{oj}^*(s) - \frac{sL+r}{D_{VM}(s)} i_{oj}(s) + \frac{K_l}{D_{VM}(s)} i_{crj}(s) \cdots (a)$$

$$v_o(s) = G_{cl}^{CM}(s) v_{oj}^*(s) - \frac{sL+r}{D_{CM}(s)} i_{oj}(s) + \frac{G_c(s)}{D_{CM}(s)} i_{crj}(s) \cdots (b) \quad (4.15)$$

Figure 4.4 shows modified VMI and CMI multi-loop control schemes with an added average current feedforward term. The average current is added to the control signal with a gain of K_l and $G_c(s)$ in Figure 4.4(a) and (b), respectively. Figure 4.4(b) also displays the reduced model with the average current, i_{oav} being transferred before the current compensator $G_c(s)$ using block reduction technique. As a consequence, i_{oav} added to the voltage compensator output, can be considered as inductor current reference i_{lj}^* for the respective inner controller $G_c(s)$, similar to CMIL.

Since, instantaneous sum of circulating currents is zero i.e., $\sum i_{crj}(s) = 0$, the output voltage of the parallel inverter system are written as

$$\begin{aligned} v_o(s) &= G_{cl}^{VM}(s)\,v_{oav}^*(s) - \frac{sL+r}{D_{VM}(s)}\,i_{oav}(s) \cdots (a) \\ v_o(s) &= G_{cl}^{CM}(s)\,v_{oav}^*(s) - \frac{sL+r}{D_{CM}(s)}\,i_{oav}(s) \cdots (b) \end{aligned} \tag{4.16}$$

The resulting circulating current impedance can be obtained by using (4.4), (4.15) and (4.16) as :

$$\begin{aligned} Z_{crj}^{VM}(s) &= \frac{sL+r+K_l}{G_v(s)} \cdots (a) \\ Z_{crj}^{CM}(s) &= \frac{sL+r+G_c(s)}{G_v(s)G_c(s)} \cdots (b) \end{aligned} \tag{4.17}$$

The circulating current impedances of the j^{th} module, Z_{crj} with IACFF in (4.17) have the same impedances as for VMI and CMI in Table 4.1. On the other hand, the output impedances in (4.18) with IACFF have no term of K_l and $G_c(s)$ in numerators in comparison to that of VMI and CMI, respectively.

$$\begin{aligned} Z_{cl}^{VM}(s) &= \frac{sL+r}{s^2LC + s(r+K_l)C + G_v(s)} \cdots (a) \\ Z_{cl}^{CM}(s) &= \frac{sL+r}{s^2LC + s\big(r+G_c(s)\big)C + G_v(s)G_c(s)} \cdots (b) \end{aligned} \tag{4.18}$$

Therefore from (4.17) and (4.18), the proposed IACFF control shows that gains K_l and $G_c(s)$ provide gains only to the I-M circulating current component and are not included in the output impedances. As a result, the voltage response is expected to be better immuned from load current distortions in case of IACFF control scheme as compared to that of conventional VMI or CMI schemes. In fact, the IACFF control is similar to CMIL as far as the output impedance is concerned, although the Z_{cr} is still as high as in VMI and CMI.

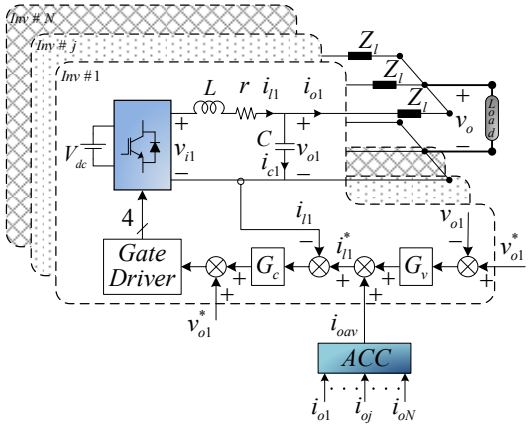


Figure 4.5 Multi-modular UPS inverters system with proposed IACFF control.

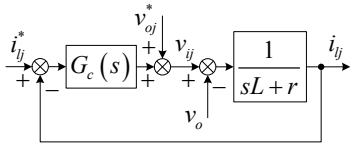
Multi-Modular UPS inverters system configuration with the proposed IACFF control scheme has been shown in Figure 4.5. Line impedances Z_l of the connecting UPSs can be presumed negligible since, inverters are placed in close vicinity to increase the power level. Each j^{th} inverter module provides a measured output current 'i_{oj}' to an Average Current Computation (ACC) block for the generation of current reference 'i_{oav}'. In this work, only CMI with IACFF control has been considered for investigation of the concept.

4.4 Controller Parameter Design

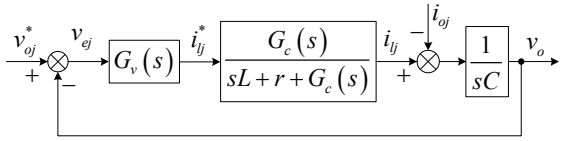
This section discusses the methodology opted for the design of controller parameters. The proposed IACFF scheme is basically a multi-loop current-mode control strategy using average current feed-forward technique. Consequently, in the design strategy, first the inner-loop current controller is set for a specified bandwidth and steady-state error criterion. Thereafter, the outer voltage loop is tuned to ensure a minimum steady-state output voltage error. Finally, it will be shown that the circulating current impedance is heavily dependent on the voltage regulator and eventually affects the final selection of the voltage gain.

4.4.1 Inner Current Control Loop

A simplified version of inductor current feedback inner-loop for inverter control is shown in Figure 4.6(a). It can be seen that the addition of the j^{th} inverter reference voltage feedforward has a cancellation effect on the output voltage and thus, only voltage error ($v_{oj}^* - v_o$) acts as an external disturbance to the inner current loop. The actual inductor current, 'i_l' to reference inductor current, 'i_l^*' transfer function reduces to,



(a)



(b)

Figure 4.6 Block schematic of an inverter module using IACFF control (a) Inner current control loop and (b) Outer voltage control loop.

$$G_{in}(s) = \frac{i_l}{i_l^*} = \frac{G_c(s)}{sL + r + G_c(s)} \tag{4.19}$$

where, $G_{in}(s)$ can be designated as the inner-loop transfer function. Since, conventional proportional integral (PI) control has its own limitations for alternating signals, proportional resonant (PR) control has been considered in this application. However, an ideal PR controller has infinite fundamental gain and hence a practical realisable form of (4.20) as given in [39] has been used,

$$G_c(s) = K_{cp} + K_{ci}\frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_o^2} \tag{4.20}$$

where K_{cp} and K_{ci} are the respective proportional and integral gains for the PR current controller with a tuned fundamental frequency of ω_o = 314 rad⁄s. ω_c refers to the integrator low frequency cut-off that limits the resonant peak and is chosen to be 5 rad⁄s. Substituting(4.20) in (4.19), K_{cp} and K_{ci} can be obtained for the required design specifications.

In the PR based control implementation, transient and steady-state responses are mostly dependent on the K_{cp} and K_{ci} gains, respectively; almost in a decoupled manner [39]. Transient response is better for systems with larger K_{cp} and hence higher bandwidth, which in turn is limited by inverter's switching noise immunity. Therefore, a compromised value for the bandwidth i.e., approximately about one fifth of the switching frequency may be able to block switching frequency noise and satisfactorily eliminate the load current disturbances. With the above conditions and a bandwidth frequency of ω_{bi}, proportional gain of the PR controller can be calculated by substituting $G_c(s) = K_{cp}$ in (4.19) and equating $|G_{in}(s)| = 1/\sqrt{2}$,

$$K_{cp} = \sqrt{\omega_{bi}^2 L^2 + 2r^2} - r \simeq \omega_{bi} L \tag{4.21}$$

Considering ESR '*r*' to be practically negligible, proportional gain is almost equal to $\omega_{bi}L$. A K_{cp} = 10 results in a bandwidth of 1.6 kHz, which can be considered an optimum value for the UPS inverter applications, having both switching and load-disturbance rejection capability. The resonant integral gain K_{ci} value is obtained around 400 with a steady-state current error, e_{iss} of 1 % at the fundamental frequency ω_o, from the following relation

$$\begin{aligned} e_{iss} &= \frac{i_l^* - i_l}{i_l^*} = \frac{sL + r}{sL + r + G_c(s)} \\ &= \left| \frac{\left(s^2 + 2\omega_c s + \omega_o^2\right)(sL + r)}{\left(s^2 + 2\omega_c s + \omega_o^2\right)\left(sL + r + K_{cp}\right) + 2\omega_c K_{ci} s} \right| \end{aligned} \tag{4.22}$$

4.4.2 Outer Voltage Regulation Loop

The outer-loop is tuned next, to achieve the desired voltage regulation and THD specifications. Figure 4.6(b) shows the simplified block diagram representation of the voltage-loop with the inner-loop being replaced by $G_{in}(s)$ as stated in (4.19). The voltage controller, $G_v(s)$ may be a PR controller, as in the case of inner-loop current regulator, to achieve zero steady-state voltage error. However, a conflict of control action exists therein between voltage regulation and current sharing, i.e., for proper current sharing voltage regulation has to be compromised (to be discussed in the subsequent sub-section). Therefore, a voltage regulator of P-type is used in the presented control strategy. Although, a very high gain K_v is required to achieve the zero voltage error, reference voltage feed-forward can effectively help in reducing the required control effort of the P-regulator. Consequently, closed-loop voltage gain transfer-function as obtained from Figure 4.6(b) is:

$$\begin{aligned} G_{cl}(s) &= \frac{G_v(s) G_c(s)}{s^2 LC + s\left(r + G_c(s)\right)C + G_v(s) G_c(s)} \\ &= \frac{\left(s^2 + 2\omega_c s + \omega_o^2\right) K_v K_{cp} + 2\omega_c K_v K_{ci} s}{\left(s^2 + 2\omega_c s + \omega_o^2\right)\left(s^2 LC + srC + sK_{cp} C + K_v K_{cp}\right) + 2\omega_c K_{ci} C s^2 + 2\omega_c K_v K_{ci} s} \end{aligned} \tag{4.23}$$

Steady-state voltage error e_{vss} at the fundamental frequency ω_o has been obtained for selected K_v and the current regulator K_{cp} and K_{ci} values, from the following relation:

$$e_{vss} = \left| \frac{\left(s^2 + 2\omega_c s + \omega_o^2\right)\left(s^2 LC + srC + sCK_{cp}\right) + 2\omega_c K_{ci} C s^2}{\left(s^2 + 2\omega_c s + \omega_o^2\right)\left(s^2 LC + srC + sCK_{cp}\right) + 2\omega_c K_{ci} C s^2 + 2\omega_c K_{ci} K_v s} \right| \tag{4.24}$$

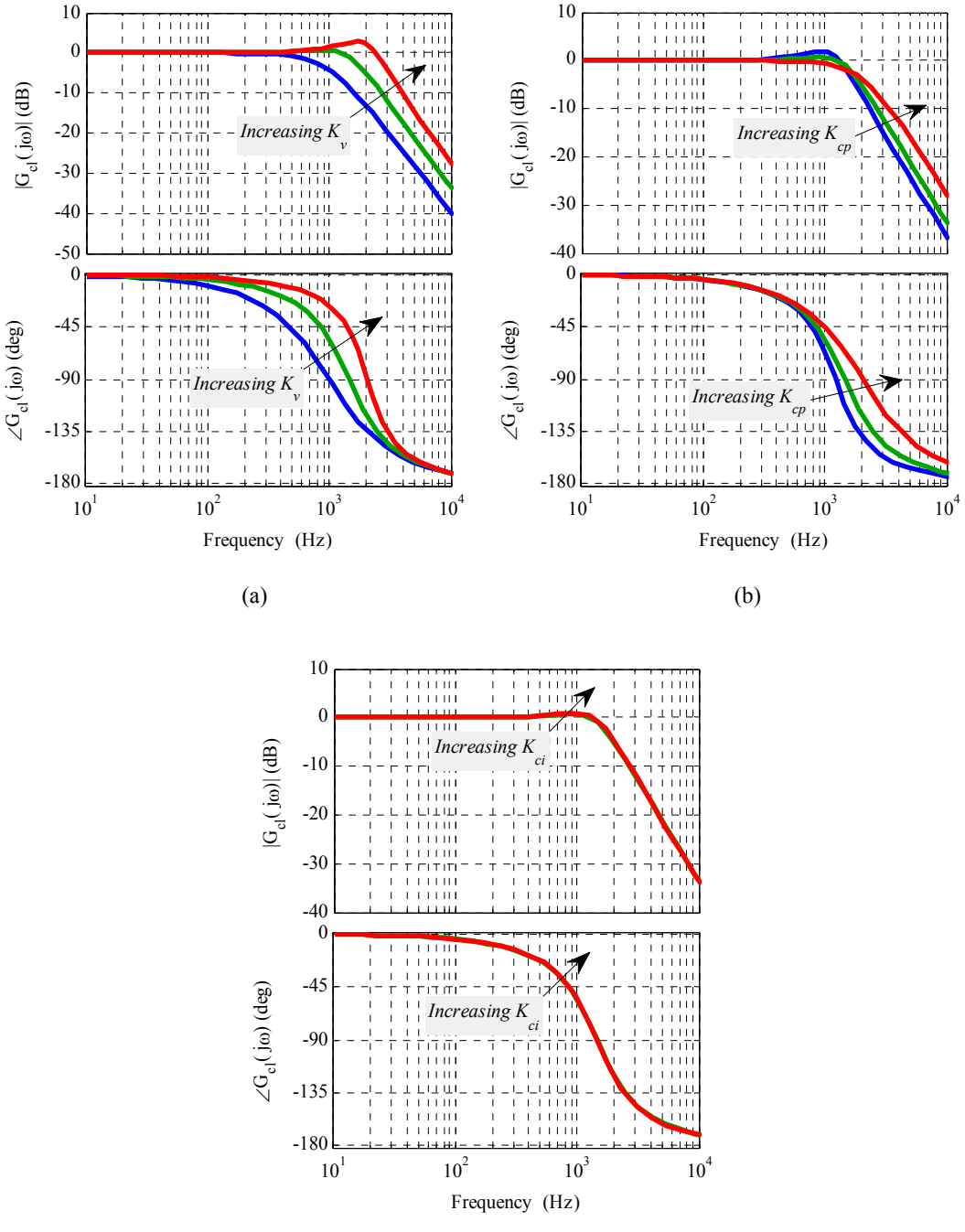


Figure 4.7 Bode-plot depicting effect of controller parameter variations on close-loop voltage gain G_{cl} (a) K_v (0.07,0.15 and 0.3), (b) K_{cp} (7,10 and 20) and (c) K_{ci} (200,400 and 750).

The performance dependency on the controller parameters can be anticipated from the frequency response of the close-loop voltage gain G_{cl}. The Bode response plots of the proposed P-PR control voltage gain G_{cl} are given in Figure 4.7(a), (b) and (c) for K_{cp}, K_{ci} and K_v variations, respectively. The plots are drawn for nominal values of P-PR controller listed in the Table D.5 of Appendix D, with only one variable parameter at a time. The proportional gains for both inner and outer loops largely affect the bandwidth, with a gradual increase on increasing K_v and K_{cp} gains, respectively. Whereas, K_{ci} has a negligible effect on the close-loop voltage gain magnitude and phase plots. The selected value of the voltage gain K_v is 0.15, which gives an optimum THD and steady-state error on rated loading conditions.

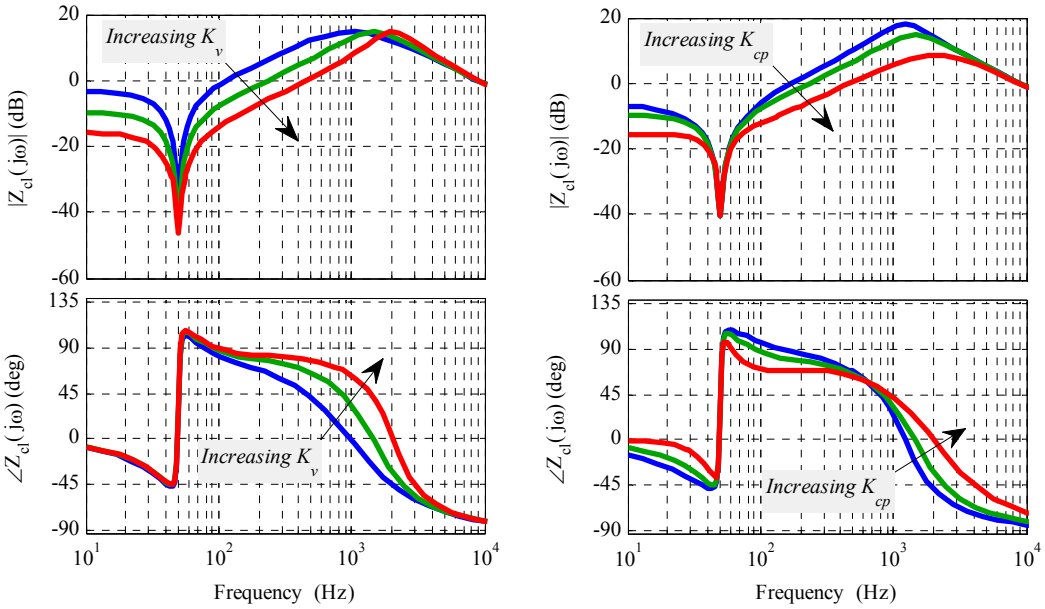
4.4.3 Analysis of Output Impedance, Z_{cl}

Output impedance Z_{cl}, is a direct measure of load current disturbance on the output voltage. Ideally, the impedance should be zero to nullify the voltage distortions due to loading. However, in practice it should be maintained as low as possible. Therefore in design finalisation, an assessment of output impedance dependency on voltage and current controller parameters has been investigated. The output impedance Z_{cl} is obtained from (4.18)(b), wherein P and PR control have been used for the voltage and current controllers, respectively.

$$Z_{cl}(s) = \frac{\left(s^2 + 2\omega_c s + \omega_o^2\right)(sL + r)}{\left(s^2 + 2\omega_c s + \omega_o^2\right)\left(s^2 LC + srC + sK_{cp}C + K_v K_{cp}\right) + 2\omega_c K_{ci} C s^2 + +2\omega_c K_v K_{ci} s} \tag{4.25}$$

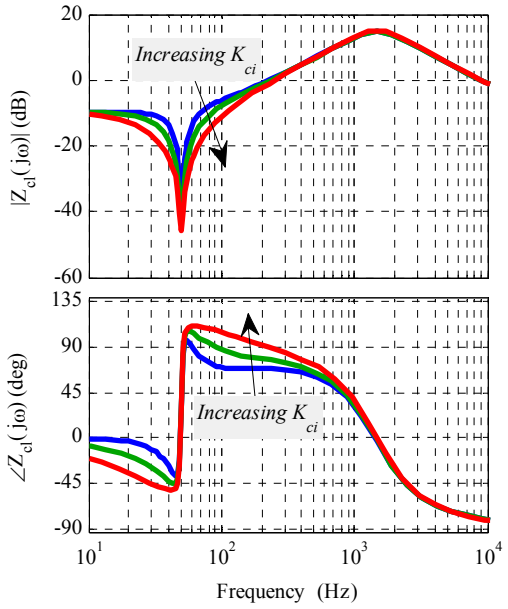
Figure 4.8 shows frequency plots for Z_{cl} with variation in controller parameters. K_v causes variation in the output impedance, Z_{cl} in almost complete frequency spectrum, including the fundamental. Though, K_{cp} also influences the output impedance in the entire frequency spectrum but no effect in the vicinity of fundamental frequency is seen. On the other hand, the effect of K_{ci} is prominent only around the fundamental, as depicted in Figure 4.8 (c).

Further, the effect of harmonic current disturbances (in case of non-linear loads) on the output voltage can be reduced using multi-resonant compensators for other prominent harmonics too [183]. This adds an additional notch at those frequencies and consequent voltage distortions due to respective harmonic components on load gets eliminated. Figure 4.9 shows the impedance Bode Magnitude and Phase plots for resonant compensators at 3^{rd} and 5^{th} harmonics (i.e., $3\omega_o$ and $5\omega_o$, respectively) in addition to the fundamental frequency, ω_o.



(a)

(b)



(c)

Figure 4.8 Bode-plot showing effect of controller parameter variations on Z_{cl} (a) K_v (0.07,0.15 and 0.3), (b) K_{cp} (7,10 and 20) and (c) K_{ci} (200,400 and 750).

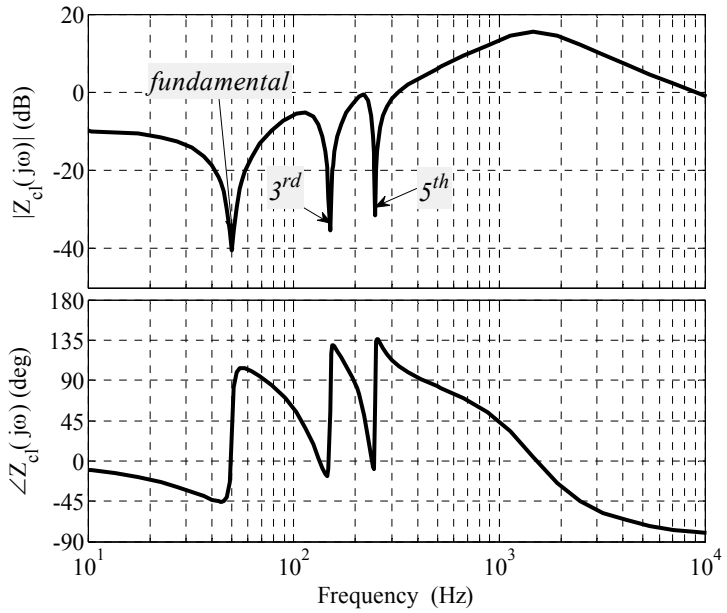


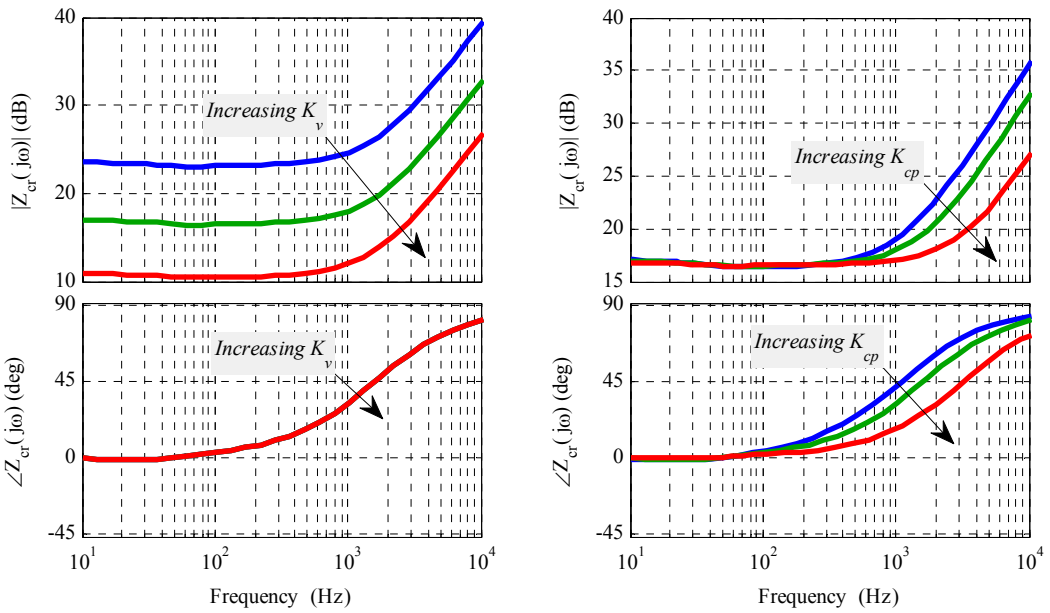
Figure 4.9 Bode-plot for output impedance after incorporating 3rd and 5th harmonic compensation.

4.4.4 Effect of Control Parameters on Circulating Current Impedance, Z_{cr}

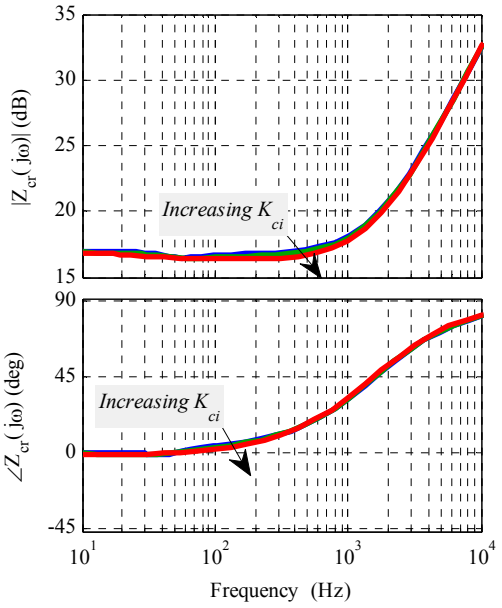
The circulating current impedance transfer function can be obtained using (4.17)(b), by substituting respective P-PR controller gains,

$$Z_{cr}(s) = \frac{\left(s^2 + 2\omega_c s + \omega_o^2\right)\left(sL + r + K_{cp}\right) + 2\omega_c K_{ci} s}{K_v\left[\left(s^2 + 2\omega_c s + \omega_o^2\right)K_{cp} + 2\omega_c K_{ci} s\right]} \tag{4.26}$$

The corresponding variations in Z_{cr} due to controller parameters have been plotted and shown in Figure 4.10. The K_{cp} gain of current controller has no effect on lower frequencies, whereas a gradual reduction in impedance is observed at higher frequency ranges. Controller parameter K_{ci} does not show significant variation in the entire frequency range, except for a slight reduction at the knee point as shown in Figure 4.10(c). However, proportional gain, K_v of the voltage controller on the other hand, introduces a large shift in Z_{cr} magnitude in the entire frequency range. There is a significant reduction in impedance magnitude with the increase in K_v value, while phase remains same as seen from Figure 4.10(a).

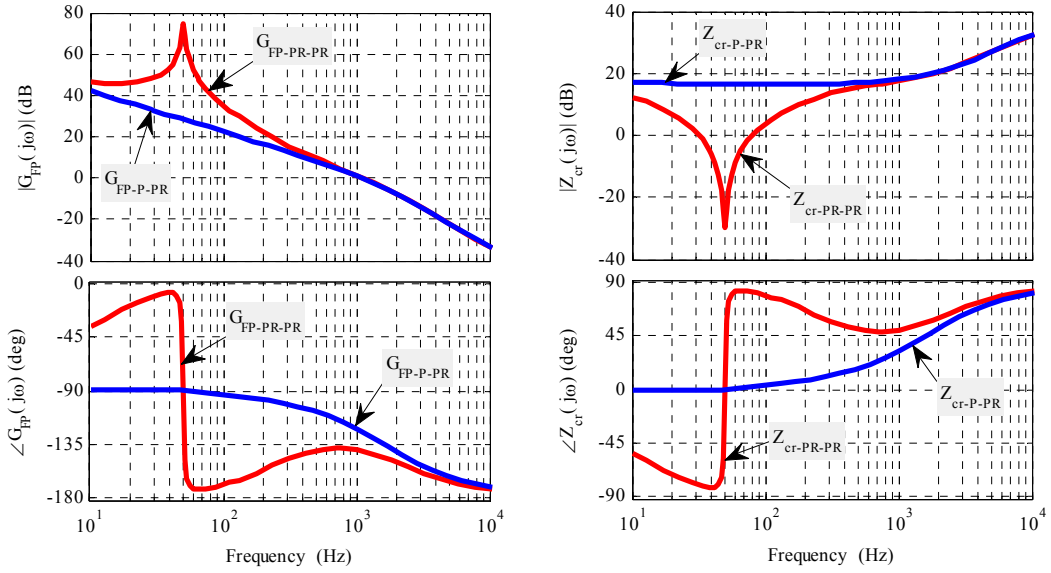


(a) (b)



(c)

Figure 4.10 Bode-plot showing effect of controller parameter variations on Z_{cr} (a) K_v (0.07,0.15 and 0.3), (b) K_{cp} (7,10 and 20) and (c) K_{ci} (200,400 and 750).



(a) (b)

Figure 4.11 Bode-plot (a) Forward path voltage gain G_{FP} and (b) Circulating current impedance Z_{cr}.

4.4.5 Conflict between Voltage Regulation and Circulating Current Impedance (Z_{cr})

The effect of voltage controller type on voltage regulation and circulating current impedance on the proposed control scheme has been investigated in the present sub-section. The voltage regulation capability of the controller can be better analysed through open-loop or forward path transfer function, G_{FP}. Forward path gain, $G_{FP}^{P-PR}(s) = v_o / v_e$ for the proposed P and PR controllers in voltage and current regulators, respectively can be obtained from Figure 4.6(b),

$$G_{FP}^{P-PR}(s) = \frac{G_v(s)G_{in}(s)}{sC} = \frac{G_v(s)G_c(s)}{\left(sL + r + G_c(s)\right)sC}$$
$$= \frac{K_v\left\{\left(s^2 + 2\omega_c s + \omega_o^2\right)K_{cp} + 2\omega_c K_{ci} s\right\}}{\left(s^2 + 2\omega_c s + \omega_o^2\right)\left(sL + r + K_{cp}\right)sC + s^2 2\omega_c K_{ci} C} \tag{4.27}$$

The forward path gain, $G_{FP}^{PR-PR}(s)$ may be obtained from Figure 4.6(b) by using PR control logic for both voltage and current controllers as,

$$G_{FP}^{PR-PR}(s) = \frac{G_v(s)G_{in}(s)}{sC} = \frac{G_v(s)G_c(s)}{\left(sL + r + G_c(s)\right)sC}$$
$$= \frac{\left\{\left(s^2 + 2\omega_c s + \omega_o^2\right)K_{vp} + 2\omega_c K_{vi} s\right\}\left\{\left(s^2 + 2\omega_c s + \omega_o^2\right)K_{cp} + 2\omega_c K_{ci} s\right\}}{\left(s^2 + 2\omega_c s + \omega_o^2\right)^2\left(sL + r + K_{cp}\right)sC + s^2\left(s^2 + 2\omega_c s + \omega_o^2\right)2\omega_c K_{ci} C} \tag{4.28}$$

Generally, for ac signals, PR control for both voltage and current regulators would have given a better steady state performance. Figure 4.11(a) shows a magnitude gain of around 75 dB for G_{FP}^{PR-PR} at the fundamental frequency. In comparison to that, the forward path gain G_{FP}^{P-PR} (when $G_v(s)$ is P control and $G_c(s)$ is PR control), has an approximate magnitude of 30 dB. The phase margin in voltage gain observed for the P-PR combination is however larger than the PR-PR combination, which on other side indicates better system stability.

However, a high gain of *PR-PR* controller in turn reduces the circulating current impedance Z_{cr}^{PR-PR} to a very low value, particularly at the fundamental frequency, as shown in Figure 4.11(b). The Bode response for Z_{cr}^{PR-PR} can be obtained from the following transfer function by substituting *PR* control for both $G_v(s)$ and $G_c(s)$ in (4.17)(b),

$$Z_{cr}^{PR-PR}(s)=\frac{\left(s^2+2\omega_c s+\omega_o^2\right)^2\left(sL+r+K_{cp}\right)+\left(s^2+2\omega_c s+\omega_o^2\right)2\omega_c K_{ci}s}{\left[\left(s^2+2\omega_c s+\omega_o^2\right)K_{vp}+2\omega_c K_{vi}s\right]\left[\left(s^2+2\omega_c s+\omega_o^2\right)K_{cp}+2\omega_c K_{ci}s\right]} \quad (4.29)$$

In contrast, IACFF control with P-PR combination has uniform higher impedance Z_{cr}^{P-PR} unto the *LC* resonance frequency and then monotonically increasing beyond that. Thus, a better circulating current suppression may be achieved with suggested IACFF control scheme using P-PR combination. The circulating current impedance Z_{cr}^{P-PR} used in Bode plot may be obtained from (4.17)(b), by substituting P and PR control in voltage and current regulators, respectively.

4.5 Results and Discussions

The proposed IACFF control strategy has been first simulated in MATLAB/Simulink platform in DTF. An experimental prototype has also been implemented using Texas instruments DSP TMS320F2812 based controller for validation of the proposed scheme. Two inverter modules with nominal ratings of 0.25 kVA, 80 V each, are used for the investigation whose system parameters are enlisted in Table D.1 of Appendix D. Operating switching frequency has been taken as 10 kHz for both the inverter modules respectively.

4.5.1 Simulation Investigations

Simulations have been carried out with an objective to show the effectiveness of the proposed IACFF control strategy when compared with the conventional control scheme using regular voltage controller. Three cases have been taken for simulation study, namely; CMIL without any current sharing scheme, CMIL with the IACFF but with the both voltage and

current regulators as PR control and the proposed IACFF with P-PR control. Although CMI is the control structure from which proposed IACFF has been derived, but it has unacceptable poor voltage regulations. Therefore, CMIL has been chosen for study of current sharing, as it is only different from the proposed IACFF scheme, in respect to the feed-forward variable.

Figure 4.12(a) shows the condition, when two inverters have been connected without IACFF control i.e., respective load currents i_{o1} and i_{o2} have been used as feed-forwarded signals instead of average load current i_{oav}. Significant amount of circulating current exists

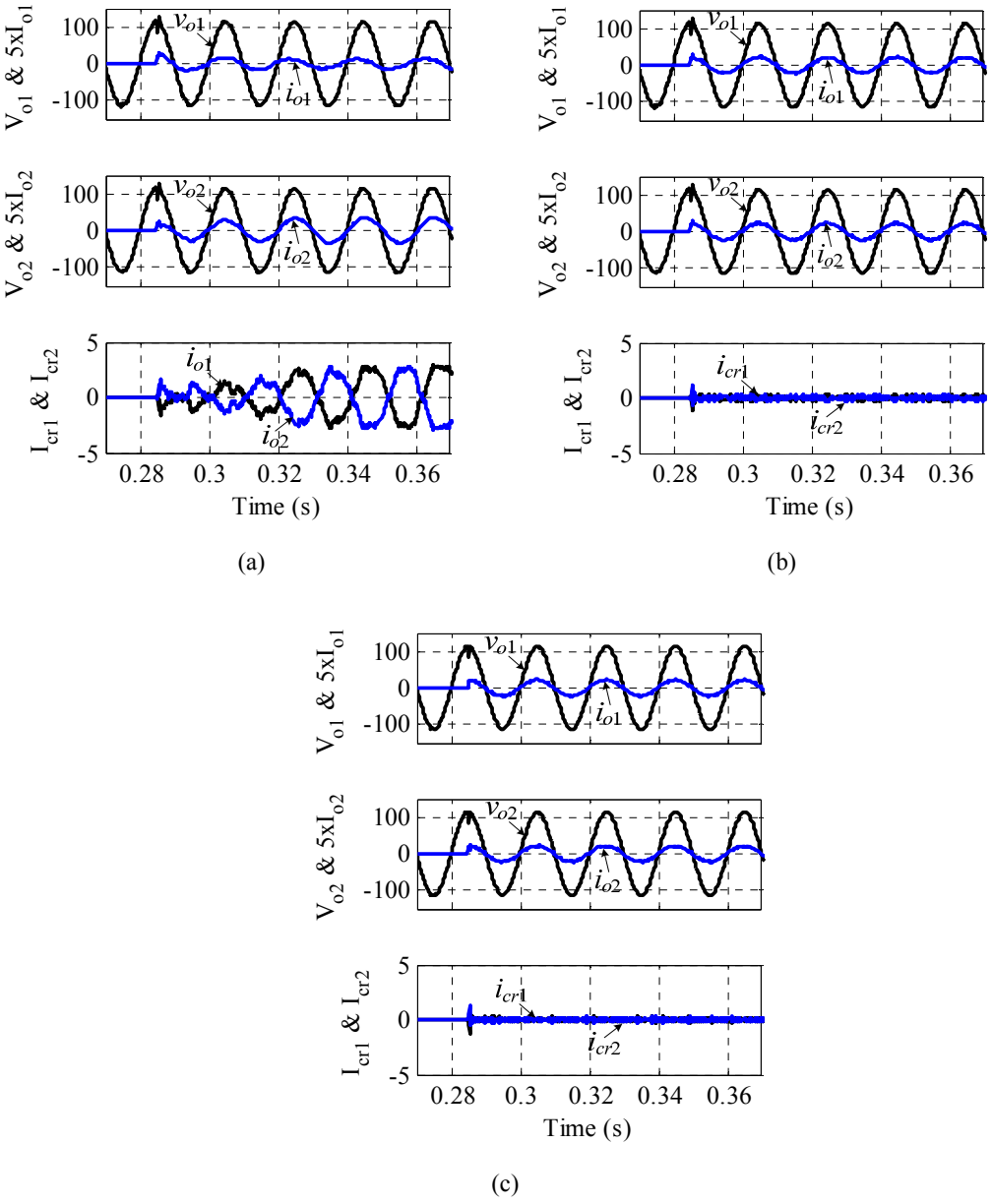


Figure 4.12 Simulated waveforms under rated linear load for (a) PR-PR with no current sharing scheme, (b) PR-PR with IACFF control and (c) P-PR with IACFF control.

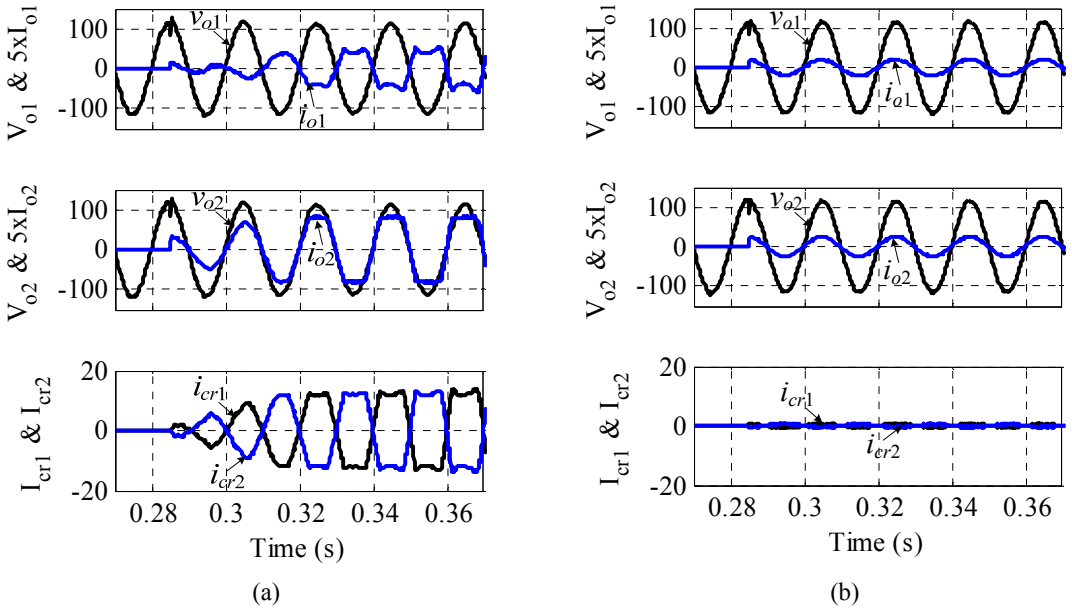


Figure 4.13 Simulated waveforms under 5% reference voltage magnitude variation (80 and 84 V) for (a) PR-PR Control and (b) P-PR Control.

between the two-inverter modules with unequal load currents. Figure 4.12(b) and (c) show the dynamics when IACFF control has been employed for Bi-Modular inverters system. The former uses PR control for both voltage and current regulators whereas, the latter uses P and PR control for voltage and current regulators, respectively. Although performances were almost similar, PR-PR combination showed better voltage regulation and P-PR had better circulating current suppression. The current difference ($\Delta I_o = I_{o1} - I_{o2}$) between the two inverters for the P-PR has been 0.23 A as compared to 0.26 A in the case of PR-PR control as given in Table 4.2.

Subsequently, robustness of the proposed control strategy has been tested when the reference voltages for the two-inverter modules have difference in magnitude and phase. *LC* filter parameters for both the inverters have been set equal to that of inverter #1. Deviation in reference RMS voltage of 5% (80 V and 84 V) between the two inverter modules has been set and consequent simulated waveforms are plotted in Figure 4.13(a) and (b) for PR-PR and P-PR controller combinations, respectively. PR-PR controller shows a larger circulating current of about 25.25A on parallel operation, which in fact; is an unstable operation.

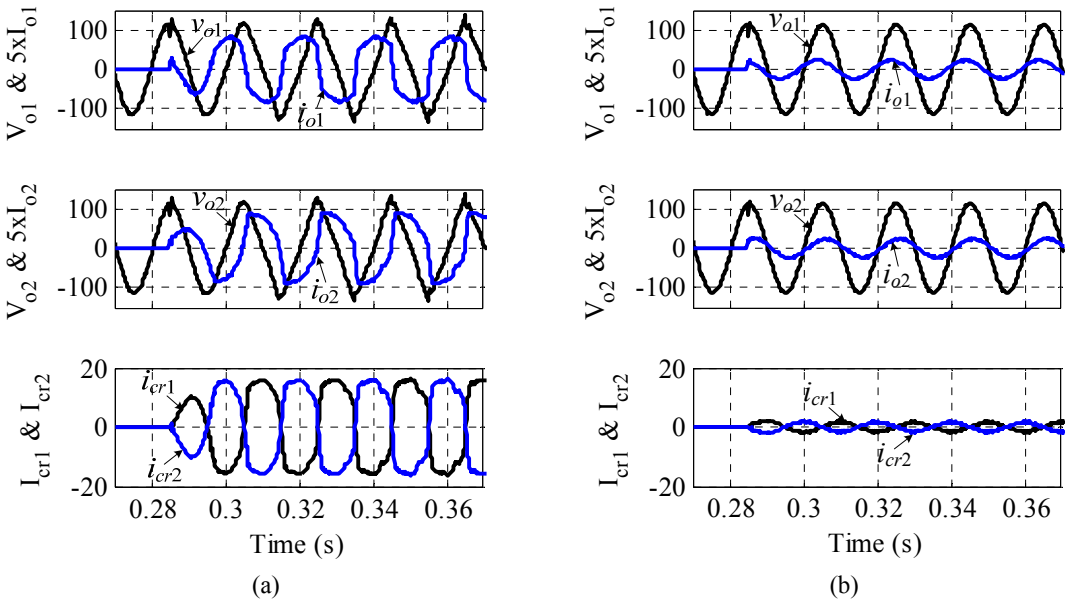


Figure 4.14 Simulated waveforms under 5° reference voltage phase variation (0 and 5°) for (a) PR-PR control and (b) P-PR control.

In a similar manner, comparatively larger circulating current between inverters has been observed for 5˚ phase deviation of reference voltage (0˚ and 5˚) for both controller options as

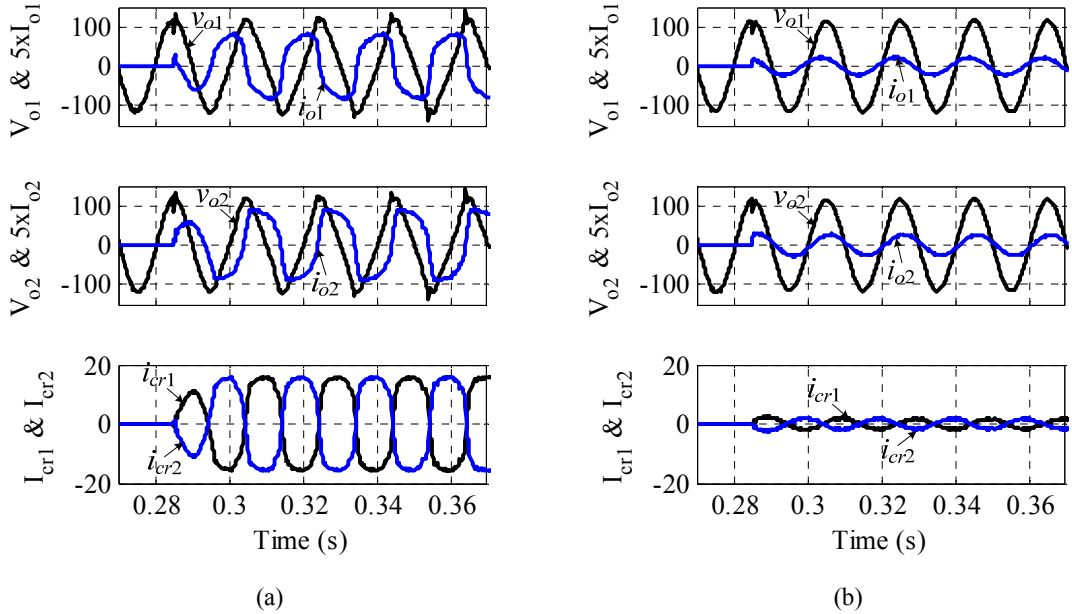


Figure 4.15 Simulated waveforms under 5% magnitude and 5° phase deviation simultaneously applied to reference voltages for (a) PR-PR control and (b) P-PR control.

Table 4.2 Simulation data for inverter currents under different conditions

Reference Voltage Deviation	PR-PR			P-PR		
	I_{o1} (A)	I_{o2} (A)	ΔI_o (A)	I_{o1} (A)	I_{o2} (A)	ΔI_o (A)
No Deviation :	3.10	3.17	0.26	3.15	3.12	0.23
5% (Magnitude) :	10.10	15.63	25.25	2.91	3.51	0.64
5° (Phase) :	13.58	13.96	26.82	3.19	3.23	1.52
5% (Magnitude) and 5°(Phase) :	12.56	14.55	26.41	3.00	3.59	1.67

$\Delta I_o = I_{o1} - I_{o2}$

shown in Figure 4.14. However, in case of PR-PR controller combination, output voltage is distorted and pushes the system towards instability. Finally, 5 % magnitude and 5˚ phase deviations in reference voltages has been applied simultaneously to both UPS inverter modules, and the observed response is shown in Figure 4.15 for both PR-PR and P-PR controllers respectively. P-PR control scheme comparatively demonstrate better performance as depicted in Table 4.2.

4.5.2 Experimental Results

Experimental verification of the proposed IACFF current sharing control scheme has been carried out for two single-phase inverter modules connected in parallel to a common load. Each inverter was connected to the load through a cable length of approximately 2 m. Both inverter systems consist of an IGBT H-bridge with an *LC* output filter. A 150 V DC-link voltage has been fed from a single-phase supply through an auto-transformer followed by a Diode Bridge. The inverter output has been fixed at 80 V, 50Hz for a rated load of 250 VA. The inverters were operated at a switching frequency of 10 kHz. The entire control scheme was realised using a 32-bit fixed point TMS320F2812 DSP (from Texas Instruments) based platform. More details of the TMS320F2812 DSP and test set-up can be found in Appendix C.

Figure 4.16(a) shows the experimental waveforms when two inverters are connected in parallel to a rated common linear load. Channel 1 (CH-1) displays the output voltage and channels 2 and 3 (CH-2 and CH-3) show inverter #1 and #2 output currents, respectively. Channel '*m*' (CH-*m*) depicts the current difference, i_{o1}–i_{o2} of two inverters, which is twice the I-M circulating current of the Bi-Modular inverter system. The load current is equally distributed in both inverters which can be confirmed from the CH-*m* waveform. Next, the inverters have been also loaded with a rectifier-type non-linear load and the consequent

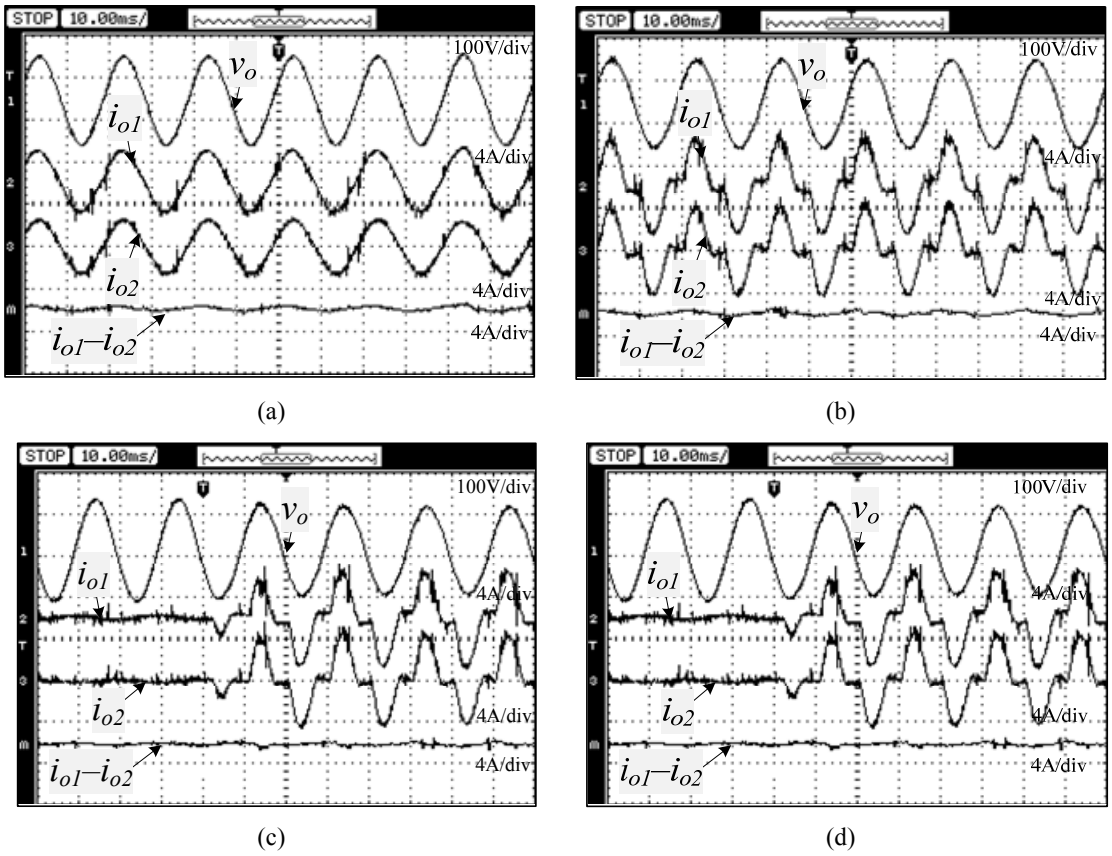


Figure 4.16 Experimental waveforms under following condition: (a) Steady-state for linear load, (b) Steady-state for non-linear load, (c) Step-application of linear load and (d) Step-application of non-linear load.

steady-state results are shown in Figure 4.16(b). In this condition also, current is shared equally among the inverters as seen from the CH-*m* current difference signal, i_{o1}–i_{o2} of the two inverters. The output voltage distortion is as low as in case of linear load and hence demonstrates voltage regulation capability of the proposed control scheme.

Subsequently, inverters have been tested for the transient capability when an abrupt step change from no-load to full load has been applied. The distortion in output voltage on dynamic operation is small and current sharing is excellent as illustrated in Figure 4.16(c) and (d) for both linear and non-linear loads, respectively. The inverters instantly share the total current when load is applied with a small current difference, even on transition.

Further, robustness in inverter control has been verified by varying the reference voltages for both the inverter modules. Figure 4.17(a) shows the condition when a 5% deviation in RMS magnitude of reference voltage has been applied and the consequent results are in synchronism with the simulated results. Similarly, a phase difference of 5° between reference voltages of the two inverters has been applied. Although, current difference is more but a stable operation has been observed as depicted in Figure 4.17(b). Figure 4.17(c) and (d) show

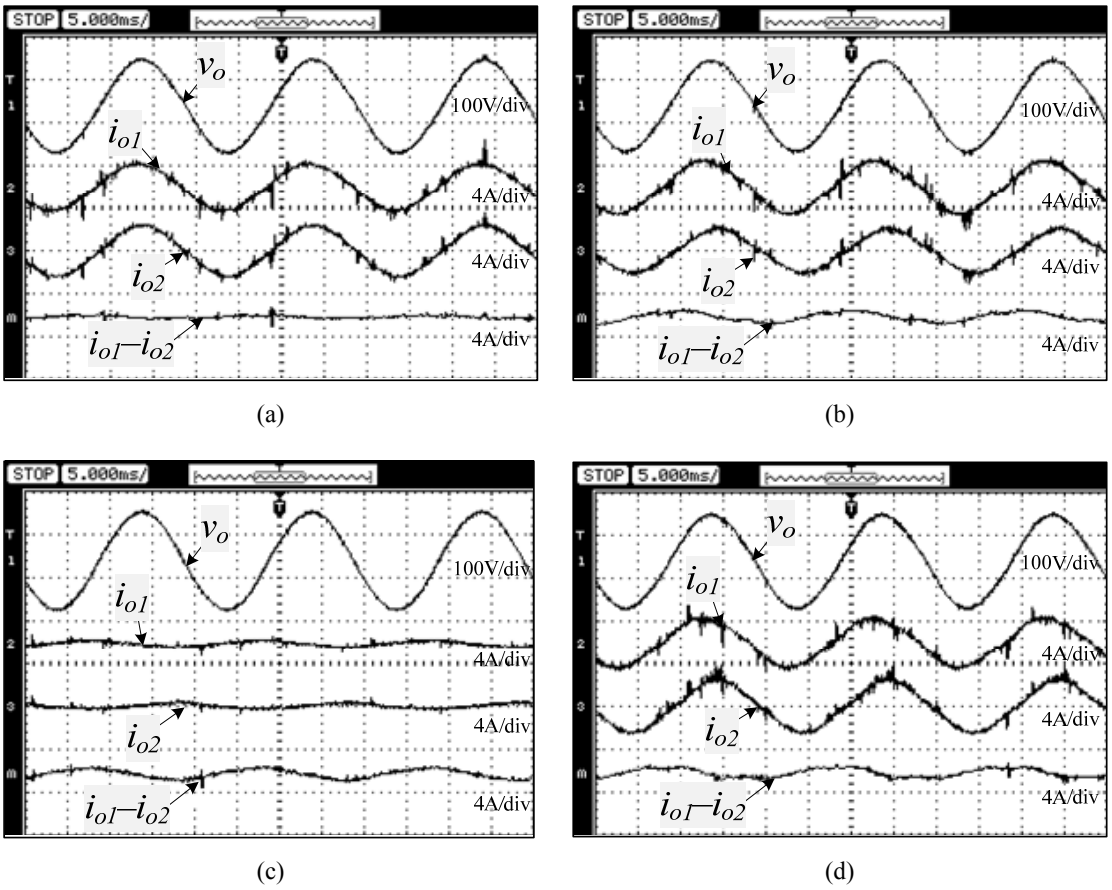


Figure 4.17 Experimental waveforms for verifying controller robustness for the proposed IACFF Control: (a) 5% reference voltage magnitude variation (80 and 84 V), (b) 5° reference voltage phase variation (0 and 5°), (c) 5% magnitude and 5° phase variation of reference voltage under no-load and (d) 5% magnitude and 5° phase variation of reference voltage on load.

results when the inverters have both magnitude and phase deviations in the reference voltages. Former shows the no load condition and the latter depicts the loaded condition. The current deviations between the two modules do exist there, however the parallel operation is stable.

Therefore, the proposed IACFF control scheme can suppress the circulating currents effectively and demonstrate good current-sharing capability under different conditions of operation.

4.6 Summary

Closed-loop control for tight voltage regulation focuses on decreasing the output impedance of inverter, which may become problematic on parallel operation. It has been shown in the early part of the chapter that the output impedance is directly proportional to the circulating current impedance. Inductor current multi-loop feedback control strategies show

enhanced circulating current impedances but not without a comparative poor voltage regulation.

This Chapter proposes a novel IACFF based multi-loop control scheme for the stable parallel operation of the multi-inverter UPS system. A modification in the feed-forward variable of the conventional multi-loop inductor plus load current control topology successfully reduces the circulating current. In the presented technique, an average current is used as a feed-forward signal in the inverter modules instead of their respective output currents. In this way, the circulating current impedance effectively increases without any additional rise in the inverter output impedance as compared to the other multi-loop inductor current feedback schemes. Therefore, the proposed control scheme has the advantage of equal load current sharing and load current decoupling for high quality voltage regulation and disturbance rejection, at the same time. And, this equal current sharing has been achieved through the direct regulation of the inner current loop without any additional current sharing loop. A possible design method and control parameter selection has also been demonstrated in due course. Further, effect of controller parameters on the voltage regulation and circulating current has been discussed in detail through a series of frequency response analysis. Later, a P-controller for voltage regulation and a PR controller for current regulation has been suggested which shows better I-M circulating current immunity and robustness. Investigations show that a compromise exists in the voltage regulation and circulating current reduction. Feasibility of the proposed IACFF control scheme has been finally verified through simulations in MATLAB environment and experimental prototype implementation using TMS320F2812 based DSP control platform.

CHAPTER 5: HIERARCHICAL FUZZY LOGIC BASED INSTANTANEOUS AVERAGE CURRENT SHARING CONTROL FOR MULTI-INVERTER UPS SYSTEM

5.1 Introduction

Considerable research work has been done in the area of multi-inverter system using traditional PID, PR and MPC based controllers due to their ease of realisation and implementation [145], [150], [153], [176]. However, setting of parameters for the controllers requires a precise mathematical modelling of the system. Aforementioned control schemes are essentially model dependent whose performance somewhat deteriorates with inaccurate system modelling. Further, inverter being a truly non-linear system, linear controllers such as PI may not be always suitable for a wide range of operating conditions.

Fuzzy Logic (FL) control has been reported for UPS inverters, though their analysis and investigation on parallel connected multi-inverter applications have been limited [53], [54], [184], [185]. Such a control can handle imprecise mathematical modelling of parallel inverters, parametric variations and wider loading conditions through simple antecedent and consequent rules, solely dependent on the input-output relations. FL control design, in essence, provides an algorithm that converts approximate human decisions into an intelligent automatic control. This is particularly useful when the system is too complex for conventional quantitative analysis [186]. A fuzzy based system consists of a set of rules according to which the output of the controller is inferred depending on the input. The inference mechanism is a non-linear process, which involves numerous mathematical multiplicative and divisive computations. Therefore, as the control-system becomes larger and complex, the number of input variables rises. Suppose, there are 'f' inputs with 'g' fuzzy subsets for each input then 'g^f' rules are required to construct the FL control algorithm. Thus, the number of fuzzy rules involved expands exponentially in such systems. Therefore, the controller needs to process a huge data base with accompanied memory overloads leading to larger computation time [187]. As a result, the overall advantage of introducing FL control gets somewhat diminished.

This chapter proposes Hierarchical Fuzzy Logic (HFL) control for parallel-connected multi-inverter UPS system. It can efficiently handle the problems associated with large rules of the conventional FL. HFL control consists of more than one low-dimensional conventional FLs arranged in a hierarchical manner, generally, taking two input variables at a time for a respective FL stage and the output is combined with the next input for the subsequent FL

stages. This arrangement gives a linear increase in number of rules, with '*g*' fuzzy sets for each '*f*' input variable. Each stage of hierarchy has 'g^2' rules and therefore, the total rules for the HFL system is $(f–1)g^2$, which is a linear function of number of input variable '*f*'. Henceforth, undesirable computational burden of FL can be relieved by the use of HFL for real-time implementation [188]. It will be shown later that the same output to input transfer characteristics is achieved without any compromise in system performance. Control algorithm for parallel-connected UPS inverters system using conventional FL and HFL schemes has been developed, investigated and a comparative equivalence has been established between the two. HFL is further evaluated in terms of ease of design, implementation and performance when compared to conventional PI based control used for multi-inverter system. Interaction of multiple inverters can be controlled in language domain, built in line with human thinking. Handling of several control variables and multiple controllers of conventional design can be easily taken care through simple input-output based intuitions. Feasibility and validation of the proposed scheme has been effectively demonstrated through MATLAB simulations and experimental prototype verification using TMS320F2812 processor.

5.2 Control Philosophy of Applied Instantaneous Average Current Sharing Scheme

Figure 5.1 shows a typical block schematic of IACS control strategy applied to 'j^{th}' module of UPS system for parallel operation [145], [176]. On assumption of homogeneous circuit and control parameters for inverter modules, following can be inferred $L_1=\cdots=L_j=\cdots=L_N=L$, $r_1=\cdots=r_j=\cdots=r_N=r$ and $C_1=\cdots=C_j=\cdots=C_N=C$, $G_{v1}=\cdots=G_{vj}=\cdots=G_{vN}=G_v$, $H_{c1}=\cdots=H_{cj}=\cdots=H_{cN}=H_c$ and $K_{c1}=\cdots=K_{cj}=\cdots=K_{cN}=K_c$. The multi-loop linear model of inverters comprise of capacitor voltage (v_o) and current (i_{cj}) feedback loops for voltage regulation along with a control loop for circulating current (i_{crj}) minimization or inhibition. The capacitor voltage and current feedbacks provide an excellent steady state and transient performances for

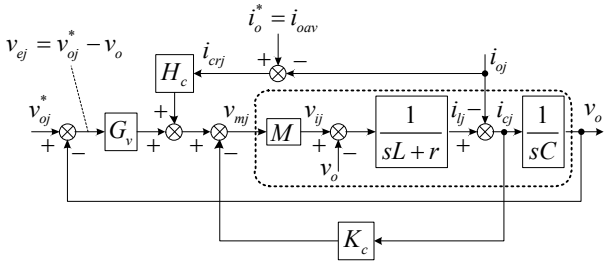


Figure 5.1 Control block schematic showing IACS control applied to j^{th} module of the *N*-modular UPS

individual UPS inverter modules [189]. The capacitor current with feedback gain 'K_c' brings a better disturbance rejection capability by Active Damping (AD) of LC filter resonance peak. The damped plant can have voltage controller, $G_v(s)$ with higher gains that make the response of the overall system faster, with higher stability limits. A current sharing controller, $H_c(s)$ adds corrective signal to the modulating signal, which can effectively reduce inverter current error. Current error is the difference between actual 'j^{th}' module output current (i_{oj}) and average of the output currents (i_{oav}) of all 'N' modules in the system. In this model, the inverter is assumed as a linear amplifier of unity gain, i.e., M =1 in the operating frequency range [150]. Therefore, the close-loop output voltage for the 'j^{th}' inverter module with circulating current regulating loop can be obtained from Figure 5.1 as:

$$v_o(s) = \frac{G_v(s)}{D_{cl}(s)} v_{oj}^*(s) - \frac{sL+r}{D_{cl}(s)} i_{oj}(s) + \frac{H_c(s)}{D_{cl}(s)} i_{crj}(s) \tag{5.1}$$

where $D_{cl}(s)=s^2LC+sC(r+K_c)+1+G_v(s)$ and $i_{crj}(s)=i_{oav}(s)-i_{oj}(s)$. The output voltage of modules when connected in parallel may be expressed as:

$$\left.\begin{aligned} v_o(s) &= \frac{G_v(s)}{D_{cl}(s)} v_{o1}^*(s) - \frac{sL+r}{D_{cl}(s)} i_{o1}(s) + \frac{H_c(s)}{D_{cl}(s)} i_{cr1}(s) \\ &\vdots \\ v_o(s) &= \frac{G_v(s)}{D_{cl}(s)} v_{oj}^*(s) - \frac{sL+r}{D_{cl}(s)} i_{oj}(s) + \frac{H_c(s)}{D_{cl}(s)} i_{crj}(s) \\ &\vdots \\ v_o(s) &= \frac{G_v(s)}{D_{cl}(s)} v_{oN}^*(s) - \frac{sL+r}{D_{cl}(s)} i_{oN}(s) + \frac{H_c(s)}{D_{cl}(s)} i_{crN}(s) \end{aligned}\right\} \tag{5.2}$$

Therefore, aggregate output voltage of the parallel-connected UPS inverters system can be expressed as,

$$v_o(s) = \frac{G_v(s)}{D_{cl}(s)} v_{oav}^*(s) - \frac{sL+r}{D_{cl}(s)} i_{oav}(s) \tag{5.3}$$

where $v_{oav}^* = \sum_{j=1}^{N} v_{oj}^* \Big/ N$, $i_{oav} = \sum_{j=1}^{N} i_{oj} \Big/ N$ and $\sum_{j=1}^{N} i_{crj} = 0$.

Since, instantaneous sum of circulating currents is zero; the output voltage of the parallel system is independent of $H_c(s)$. The circulating current for the 'j^{th}' module in the parallel-connected UPS inverters system may be defined as:

$$i_{crj}(s) = i_{oav}(s) - i_{oj}(s) \tag{5.4}$$

On subtracting, the 'j^{th}' module of (5.2) from (5.3) gives,

$$\frac{G_v(s)}{D_{cl}(s)}\left[v_{oav}^*(s) - v_{oj}^*(s)\right] - \frac{sL+r}{D_{cl}(s)}\left[i_{oav}(s) - i_{oj}(s)\right] - \frac{H_c(s)}{D_{cl}(s)} i_{crj}(s) = 0 \tag{5.5}$$

Thus, obtained circulating current relation is

$$i_{crj}(s) = \frac{G_v(s)}{sL + r + H_c(s)}\left[v^*_{oav}(s) - v^*_{oj}(s)\right] \tag{5.6}$$

Equation (5.6) shows that circulating current can be eliminated, if the gain of $H_c(s)$ is kept high. Therefore, current sharing controller reduces circulating current without affecting the aggregate output voltage of the parallel-connected inverter system.

The modulating signal, v_{mj} in the control block schematic of Figure 5.1 can be mathematically modelled as:

$$v_{mj} = G_v(s)v_{ej} - K_c i_{cj} + H_c(s)i_{crj} \tag{5.7}$$

where, $v_{ej} = (v_{oj}^* - v_o)$ and $i_{crj} = (i_{oav} - i_{oj})$. Therefore, the control law takes into account the effect of output voltage error, capacitor current and current sharing error for parallel operation of the multi-inverter UPS system. With this as the basis for parallel inverter control, FL control for the multi-inverter system is derived and discussed in the following section.

5.3 System Configuration

Figure 5.2 shows a block schematic that depicts IACS control scheme for multi-inverter UPS system using FL control. Each UPS module consists of a constant DC source, H-Bridge inverter and an output LC filter. L_j, r_j and C_j represent inductance, inductor resistance and capacitance of the filter, respectively for the 'j^{th}' inverter module. Three inputs, viz., voltage

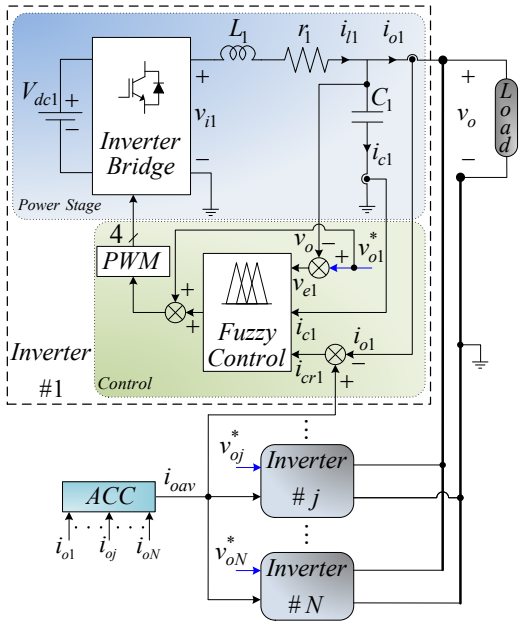


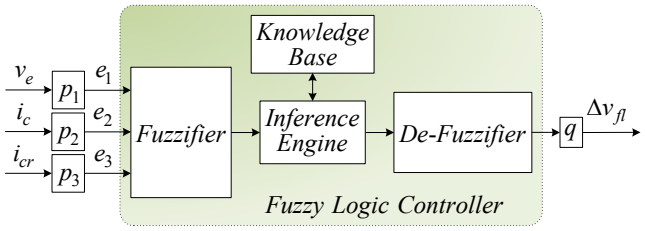
Figure 5.2 Fuzzy logic IACS control for multi-inverter UPS system.

error (v_{ej}), capacitor current (i_{cj}) and circulating current (i_{crj}) of respective inverter module are used as input variables for the FL controller. Voltage controller, circulating current controller and capacitor current loop of conventional IACS scheme of Figure 5.1 are merged in a single FL control block. Tedious analytical design of multiple regulators using conventional control has been replaced by human intuitions and experiences. Reference voltage is added as feedforward signal with the FL output to obtain the modulating signal for PWM generation. FL compensates for disturbance component only, while the major control effort is provided by the reference feedforward signal.

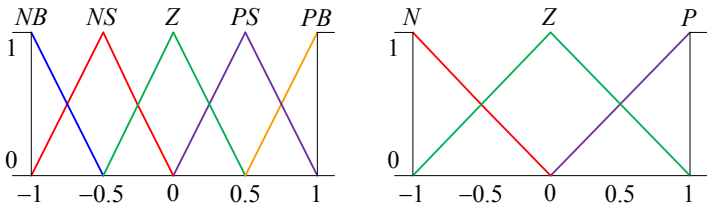
In subsequent sections, first the direct approach of multi-variable FL control design and its shortcomings have been discussed, followed by a presentation of the detailed algorithm for implementing proposed HFL control.

5.4 Conventional Fuzzy Logic Control System

A typical FL controller has basic architecture as shown in the Figure 5.3(a). It consists of a fuzzifier at the input end, knowledge base repository (rules), inference engine (for decision-making) and a de-fuzzifier at the output end [190]. Inputs to the FL controller are variables of the system to be controlled and the output is the control signal. Herein, voltage error (v_e), capacitor current (i_c), and circulating current (i_{cr}) are selected to be the input variables and change in control voltage (Δv_{fl}) is the consequent FL controller output. The voltage and current errors in discrete-time are defined in (5.8) as,



(a)



(b) (c)

Figure 5.3 (a) Block Schematic of multi-input FL controller and designated memberships, (b) Five MFs for voltage error, capacitor current and FL output, and (c) Three MFs for circulating current.

$$\left.\begin{aligned} e_1(n) &= p_1 v_e(n) = p_1\left[v_o^*(n) - v_o(n)\right] \\ e_2(n) &= p_2 i_c(n) \\ e_3(n) &= p_3 i_{cr}(n) = p_3\left[i_{oav}(n) - i_{oj}(n)\right] \end{aligned}\right\} \tag{5.8}$$

where 'n' refers to the corresponding time instant. The universe of discourse for these variables are normalised so as to adjust into the interval between –1 and +1 using suitable coefficients p_1, p_2, p_3 and q. Any input beyond these values, is saturated at ±1 and therefore

Table 5.1 Fuzzy rule base for conventional FL control

e_1	e_2	e_3			Group
		N	**Z**	**P**	
	NB	*NS*	*Z*	*PS*	G3
	NS	*NB*	*NS*	*Z*	G2
NB	Z	*NB*	*NB*	*NS*	G1
	PS	*NB*	*NB*	*NS*	G1
	PB	*NB*	*NB*	*NS*	G1
	NB	*Z*	*PS*	*PB*	G4
	NS	*NS*	*Z*	*PS*	G3
NS	Z	*NB*	*NS*	*Z*	G2
	PS	*NB*	*NS*	*Z*	G2
	PB	*NB*	*NB*	*NS*	G1
	NB	*PS*	*PB*	*PB*	G5
	NS	*Z*	*PS*	*PB*	G4
Z	Z	*NS*	*Z*	*PS*	G3
	PS	*NB*	*NS*	*Z*	G2
	PB	*NB*	*NB*	*NS*	G1
	NB	*PS*	*PB*	*PB*	G5
	NS	*Z*	*PS*	*PB*	G4
PS	Z	*Z*	*PS*	*PB*	G4
	PS	*NS*	*Z*	*PS*	G3
	PB	*NB*	*NS*	*Z*	G2
	NB	*PS*	*PB*	*PB*	G5
	NS	*PS*	*PB*	*PB*	G5
PB	Z	*PS*	*PB*	*PB*	G5
	PS	*Z*	*PS*	*PB*	G4
	PB	*NS*	*Z*	*PS*	G3

generates large corrective signals. Five symmetrical triangular overlapping Membership Functions (MFs) are utilised for the v_e, i_c, and Δv_{fl}. The MFs are labelled as Negative Big (NB), Negative Small (NS), Zero (Z), Positive Small (PS) and Positive Big (PB) as shown in Figure 5.3(b). For design simplicity, only three symmetrical triangular overlapping MFs are used for the circulating current namely, Negative (N), Zero (Z), and Positive (P) as shown in Figure 5.3(c). The most important element of the FL controller is the inference mechanism, which operates with the aid of knowledge base of fuzzy rules. Inference engine relates or maps the input variables to the output according to IF-AND-THEN fuzzy propositions set by the control goals. This investigation employs fuzzy rules which have been used in [54] for single UPS inverter using voltage error and capacitor current. The current sharing is regulated by using the logic that control signal increases with current error i_{cr} and vice versa. There are in total 75 (5 × 5 × 3) rules of equal weights that relate inputs with output, as shown in Table 5.1. The leftmost two columns indicate fuzzy sets for v_e and i_c, respectively and the topmost row displays for i_{cr}. The body enlists rules for FL output. Here, Mamdani's max-min (or sum-product) method of inference mechanism is used [186], [191]. The center of the gravity or the centroid method [186], [190] is used for de-fuzzification to obtain the FL output, which is given by the following equation:

$$\Delta v_{fl} = q \sum_{h=1}^{l} \mu_h(w_h) w_h \Big/ \sum_{h=1}^{l} \mu_h(w_h) \tag{5.9}$$

where 'l' refers to the total number of rules, $\mu_h(w_h)$ refers to the membership grade [0,1] for the h^{th} rule, and w_h is the coordinate corresponding to the output or the consequent membership function i.e. $\{w_h \in (-1, 0.5, 0, 0.5, 1)\}$. The actual crisp data for the control signal Δv_{fl} can be obtained by multiplying a scaling factor 'q' after the process of de-fuzzification is over.

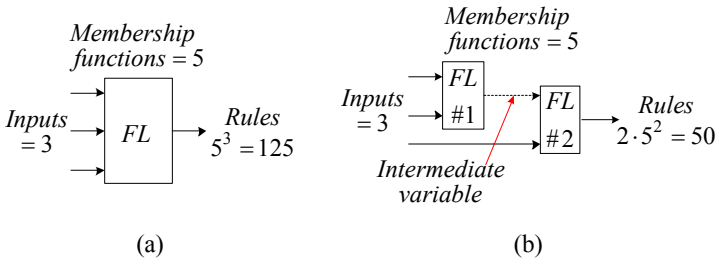


Figure 5.4 Structure of (a) Conventional FL and (b) HFL control.

5.5 Hierarchical Fuzzy Logic Control Scheme

An alternate approach for designing fuzzy set of rules can be by using the concept of HFL, which reduces the total number of rules and consequently the amount of computational burden on the processor drastically. Such an approach targets to segregate the single multi-dimensional fuzzy system into a number of two-dimensional fuzzy sub-systems. For instance, as shown in Figure 5.4(a), a conventional multi-variable FL control with three (f = 3) input variables and five (g = 5) membership functions, would have 125 (g^f =125) rules in its knowledge base repository. In comparison to it, HFL control greatly reduces the number of rules and has only 50 rules, as seen from Figure 5.4(b).

In HFL control, only two inputs are considered for a given FL sub-system at every level and rest of the inputs are utilised further in subsequent levels. Output of the present level FL of the hierarchical structure is fed as one of the two input signals to the next level FL block. However, the intermediate output is either difficult to identify or completely unknown and consequently, designing rule base for the subsequent FL block becomes difficult. To overcome such situations, Limpid-Hierarchical Fuzzy System proposed in [192], has been used in the present control for parallel-connected UPS Inverters system for mapping input-output. In this method, an intermediate mapping variable is obtained by fixing the first two inputs (1st and 2nd in the present case) and sorting same kind of rule sets from the conventional multi-variable rule base. Different sets of rules formulate a kind of membership functions for the intermediate variable. Then, the intermediate variable and the next input form the input for the second stage. The second stage output forms the next intermediate variable and in a similar manner, subsequent levels are mapped. The last level results into same input-output relation (after HFL decomposition) as that achieved from conventional FL.

To illustrate the mapping method, Figure 5.3(a) of conventional FL control can be redrawn with three inputs v_e, i_c and i_{cr} and an output Δv_{fl}, as shown in Figure 5.5. FL#1 and FL#2 are first and second level fuzzy logic units, respectively. The input variables of FL#1 are e_1 and e_2, which give an intermediate output x_{im}. Fixing e_1 and e_2 in Table 5.1, each horizontal rows of output forms a set. Each row with same set of MFs has been assigned a

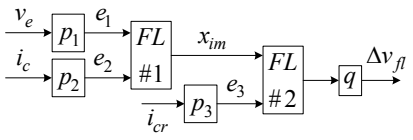


Figure 5.5 Proposed control structure with HFL.

definite group (G1, G2, G3, G4 and G5) as depicted in Table 5.1. For example from the Table 5.1, one can observe

$$\left(x_{im} \text{ is either } NS, Z \text{ or } PS\right) \text{ when } \left(e_1 \text{ is } NB\right) \text{ and } \left(e_2 \text{ is } NB\right) \tag{5.10}$$

Similarly, as in (5.10), it can be seen that same set of x_{im} is obtained from four more combinations of e_1 and e_2, i.e., for *NS* and *NS*, *Z* and *Z*, *PS* and *PS*, and *PB* and *PB*, respectively. This set was assigned G3. In the same way, five different sets (G1 to G5) have been obtained which formulated the mapping variables for x_{im}. The fuzzy rules base for FL#1 can be constructed in Table 5.2 using Table 5.1 in the form of if-then rules, as:

$$\left.\begin{array}{l} \bullet \text{ if } \left(e_1 \text{ is } NB\right) \text{ and } \left(e_2 \text{ is } NB\right) \text{ then } \left(x_{im} \text{ is G3}\right) \\ \bullet \text{ if } \left(e_1 \text{ is } NB\right) \text{ and } \left(e_2 \text{ is } NS\right) \text{ then } \left(x_{im} \text{ is } G2\right) \\ \qquad\qquad \vdots \\ \bullet \text{ if } \left(e_1 \text{ is } PB\right) \text{ and } \left(e_2 \text{ is } PB\right) \text{ then } \left(x_{im} \text{ is } G3\right) \end{array}\right\} \tag{5.11}$$

Table 5.3 tabulates the rule base for *FL* #2:

Table 5.2 Fuzzy rule base for FL #1.

e_1	e_2				
	NB	**NS**	**Z**	**PS**	**PB**
NB	G3	G2	G1	G1	G1
NS	G4	G3	G2	G2	G1
Z	G5	G4	G3	G2	G1
PS	G5	G4	G4	G3	G2
PB	G5	G5	G5	G4	G3

Table 5.3 Fuzzy rule base for FL #2.

x_{im}	e_3		
	N	**Z**	**P**
G1	NB	NB	NS
G2	NB	NS	Z
G3	NS	Z	PS
G4	Z	PS	PB
G5	PS	PB	PB

$$\left.\begin{array}{l} \bullet\ if\left(x_{im}\ is\ G1\right)\ and\ \left(e_3\ is\ N\right)\ then\ \left(\Delta v_{fl}\ is\ NB\right) \\ \bullet\ if\left(x_{im}\ is\ G1\right)\ and\ \left(e_3\ is\ Z\right)\ then\ \left(\Delta v_{fl}\ is\ NB\right) \\ \qquad\qquad \vdots \\ \bullet\ if\left(x_{im}\ is\ G5\right)\ and\ \left(e_3\ is\ P\right)\ then\ \left(\Delta v_{fl}\ is\ PB\right) \end{array}\right\} \tag{5.12}$$

From Table 5.1, the fuzzy output Δv_{fl} obtained from the conventional FL is as follows:

$$if\left(e_1\ is\ NB\right)\ and\ \left(e_2\ is\ NB\right)\ and\ \left(e_3\ is\ N\right)\ then\ \left(\Delta v_{fl}\ is\ NS\right) \tag{5.13}$$

At the same time, from (5.11) and (5.12), the fuzzy output Δv_{fl} from HFL is as follows:

$$\left.\begin{array}{l} \bullet FL\ \#1\text{: }if\left(e_1\ is\ NB\right)\ and\ \left(e_2\ is\ NB\right)\ then\ \left(x_{im}\ is\ G3\right) \\ \bullet FL\ \#2\text{: }if\left(x_{im}\ is\ G3\right)\ and\ \left(e_3\ is\ N\right)\ then\ \left(\Delta v_{fl}\ is\ NS\right) \end{array}\right\} \tag{5.14}$$

Therefore, same input-output relation is maintained in HFL as were obtained in conventional FL. With two levels and two input variables per level, the total number of rules reduces to 40 (5×5+5×3=40) as compared to 75 and hence the memory requirement of the control implementation. This is almost about 47% reduction in the memory need. This has been the case, when MF for circulating current is considered only three otherwise, with five MFs total number of rules would have been 125. And, the memory need from the conventional fuzzy is further reduced to 60%, as seen from Figure 5.4.

5.6 Results and Discussions

5.6.1 Simulation Investigations

The proposed HFL control scheme has been extensively investigated using MATLAB/Simulink DTF simulations for 250 VA, 80V inverter modules whose system parameters are enlisted in Appendix C. The inverter switching frequency has been taken as 10 kHz. A similarity assessment of the proposed HFL and conventional FL has been attempted first and thereafter a performance comparison between classical PI and HFL was evaluated under identical conditions. Later, parametric variations have been examined for robustness of the control algorithm.

5.6.1.1 Comparison of Conventional FL and HFL

As shown in Figure 5.3, the three inputs to FL controller are multiplied by respective scaling factors p_1, p_2, and p_3. The output of FL controller is the change in control signal Δv_f, which is scaled by a linear gain 'q'. Once, the knowledge repository is completed, the design process of FL is left with tuning of respective scaling factors to obtain a satisfactory response.

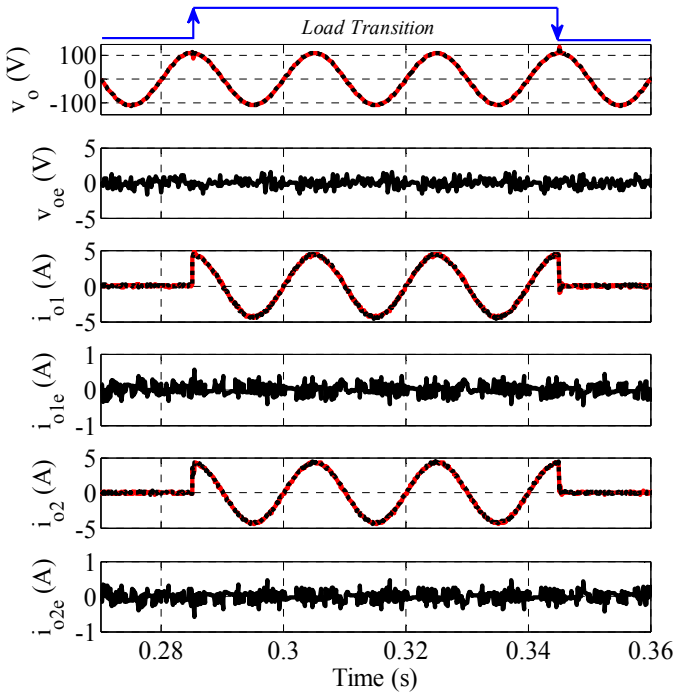


Figure 5.6 Superimposed waveforms of inverter output voltage and output currents for HFL (solid black) and conventional FL (dotted red) control.

Voltage error v_e was normalised first with respect to the peak value of DC bus voltage by adjusting p_1 coefficient. Then, q was tuned, until a minimum steady state error was achieved. Ringing in the output voltage is suppressed once p_2 coefficient of the capacitor current was fixed. This also improves the percentage % THD of the voltage response. Finally, p_3 was adjusted to reduce the circulating currents between inverter modules. A very low value of q takes greater time to response transient disturbances whereas a too high value of q makes response oscillatory. The scaling gains may need some tuning after transformation of rules from conventional FL to HFL, especially, in intermediate FL stages. Therefore, the coefficient p_3 has been re-tuned to obtain the desired response.

Figure 5.6 shows simulation comparison of the HFL control with the conventional multivariable FL for a bi-modular UPS inverters system under rated linear loading condition. With the same reference voltage for each inverter, load voltage v_o, inverter output currents i_{o1} and i_{o2} are plotted on the same scale for both controllers. Their corresponding difference in waveforms, i.e., v_{oe}, i_{o1e} and i_{o2e} are also plotted simultaneously. The dynamic performance with both FL controllers almost superimposes each other, validating the exact input-output mapping of rules. The performance quantities are also tabulated in Table 5.4. From there, it can be seen that the performance is not much affected by the reduction of rules when the rule-

base is transformed from FL to HFL control. The waveforms of the output voltage and output currents of each inverter do not show much variation even on load transitions.

Generally, performance of FL controller worsens with the decrease in number of rules, since they are directly linked with the number of MFs. A better performance is observed with increase in MFs and performance degrades with decrease in MFs. A larger MFs number increases the number of rules, hence requires a larger memory. However, the proposed HFL reduces the involved fuzzy rules without affecting the system performance. Moreover, this it is achieving without reducing the MFs for the same number of inputs.

5.6.1.2 Performance Comparison of PI and HFL Control

Comparison of IACS based parallel-connected multi-inverter operation using conventional PI and HFL control has been carried out under different operating conditions for evaluative study. Design of conventional IACS requires tuning of three control loops, namely, capacitor current loop for damping open-loop plant, voltage regulation loop, and current sharing loop, as shown in Figure 5.1. The voltage controller G_v is a PI type and current sharing is simple P control. The corresponding controller selected parameters K_c, K_p, K_i and H_c values are 10, 0.8, 4000 and 10, respectively.

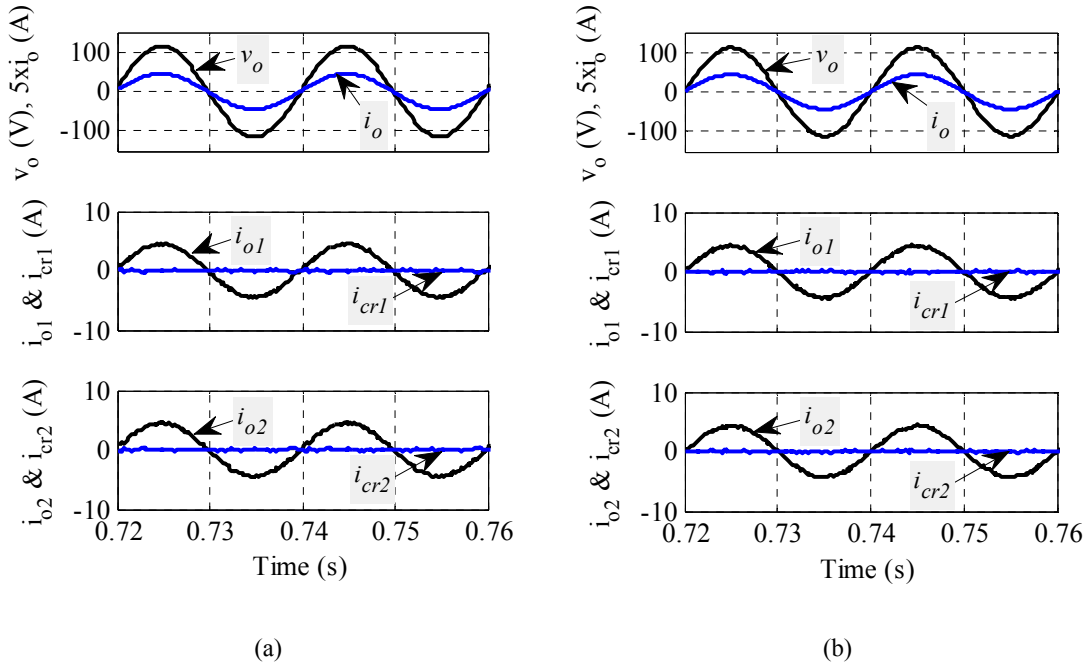
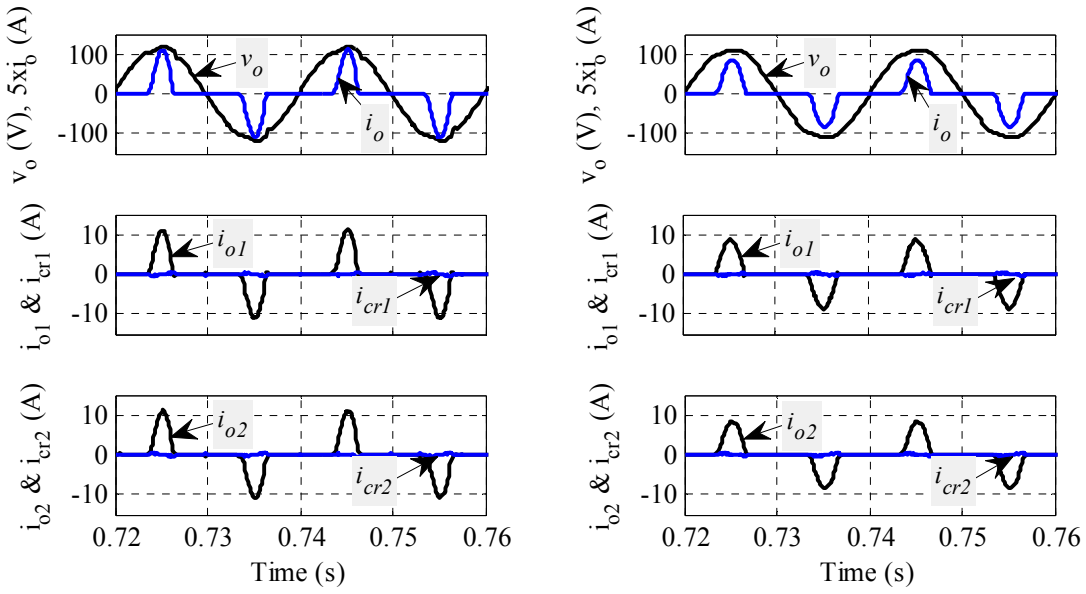
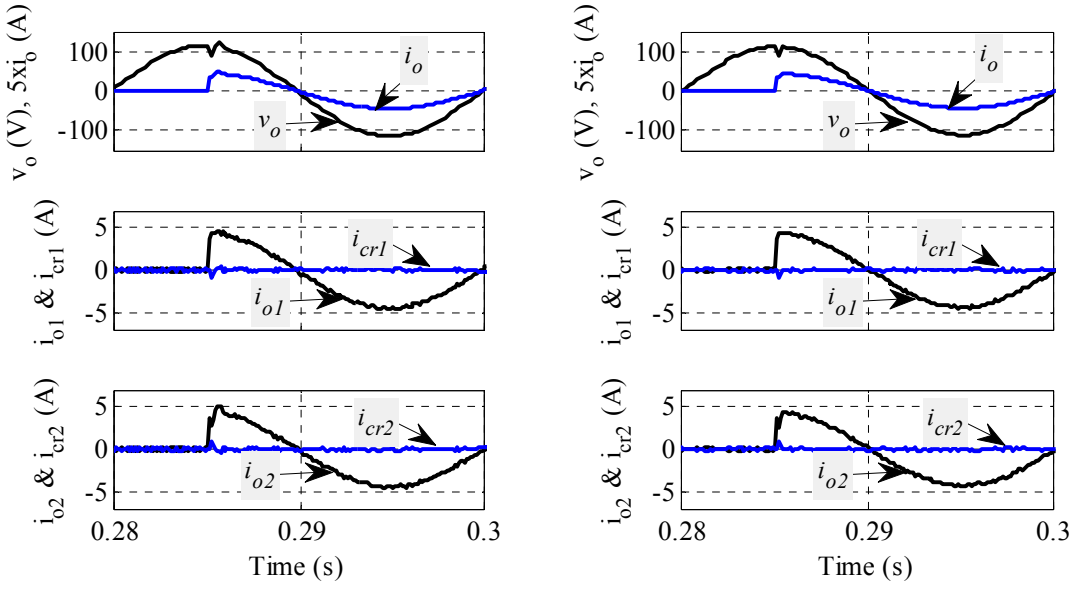


Figure 5.7 Steady-state waveforms under rated linear load for (a) PI and (b) HFL control.



(a) (b)

Figure 5.8 Steady-state waveforms under rated non-linear load for (a) PI and (b) HFL control.



(a) (b)

Figure 5.9 Transient waveforms on step load change from no-load to rated linear load for (a) PI and (b) HFL control.

Table 5.4 Performance comparison

Loading Condition	*Control Scheme*	*Voltage Error (%)*	*THD (%)*	*Circulating Current (A)*
Linear Load	Conventional *FL*	2.68	1.70	0.10
	HFL	2.58	1.67	0.11
	PI	1.58	1.80	0.12
Non-Linear Load	Conventional *FL*	3.02	2.45	0.15
	HFL	2.97	2.30	0.16
	PI	3.88	3.90	0.16

Comparisons of IACS based parallel inverter operation with conventional PI and HFL controller have been carried out under different operating conditions for evaluative study. Figure 5.7 shows simulated waveforms for both the controllers in steady state on rated linear load. The voltage regulation and current sharing performance is satisfactory in both cases. Subsequently, simulation results are also obtained for non-linear loads, as shown in Figure 5.8. However, a significant advantage in performance quantities is observed using HFL control as compared to PI as listed in Table 5.4. The percentage voltage error and THD in case of HFL is not varied much when compared to PI control. The potential of non-linear nature of HFL controller is fully expressed in this case. Transient response performance on 100% step load change for HFL is better than the conventional PI controller, as seen from voltage and current waveforms in Figure 5.9.

5.6.1.3 Effect of Parameters Variation

Ideal design values of components may vary in case of practical inverter modules. This will lead towards alteration from desired voltage waveform and current sharing performance of the inverter system. Moreover, as inferred from (5.6), even a slight deviation in reference voltage command may result in high I-M circulating currents. Therefore, the controller's potential to tackle such variations was investigated through a series of simulations. A single parameter in study was varied at a time, keeping others same for the parallel system of two inverters. For instance, while plotting inductor value mismatch in Figure 5.10 (a) & (b), filter inductance of inverter #1 is considered nominal and kept fixed throughout. Whereas, the filter inductance of inverter #2 is varied from -50% to 400% of the nominal value, keeping other parameters of inverter #1, as it is. Similarly, reference voltage magnitude and phase

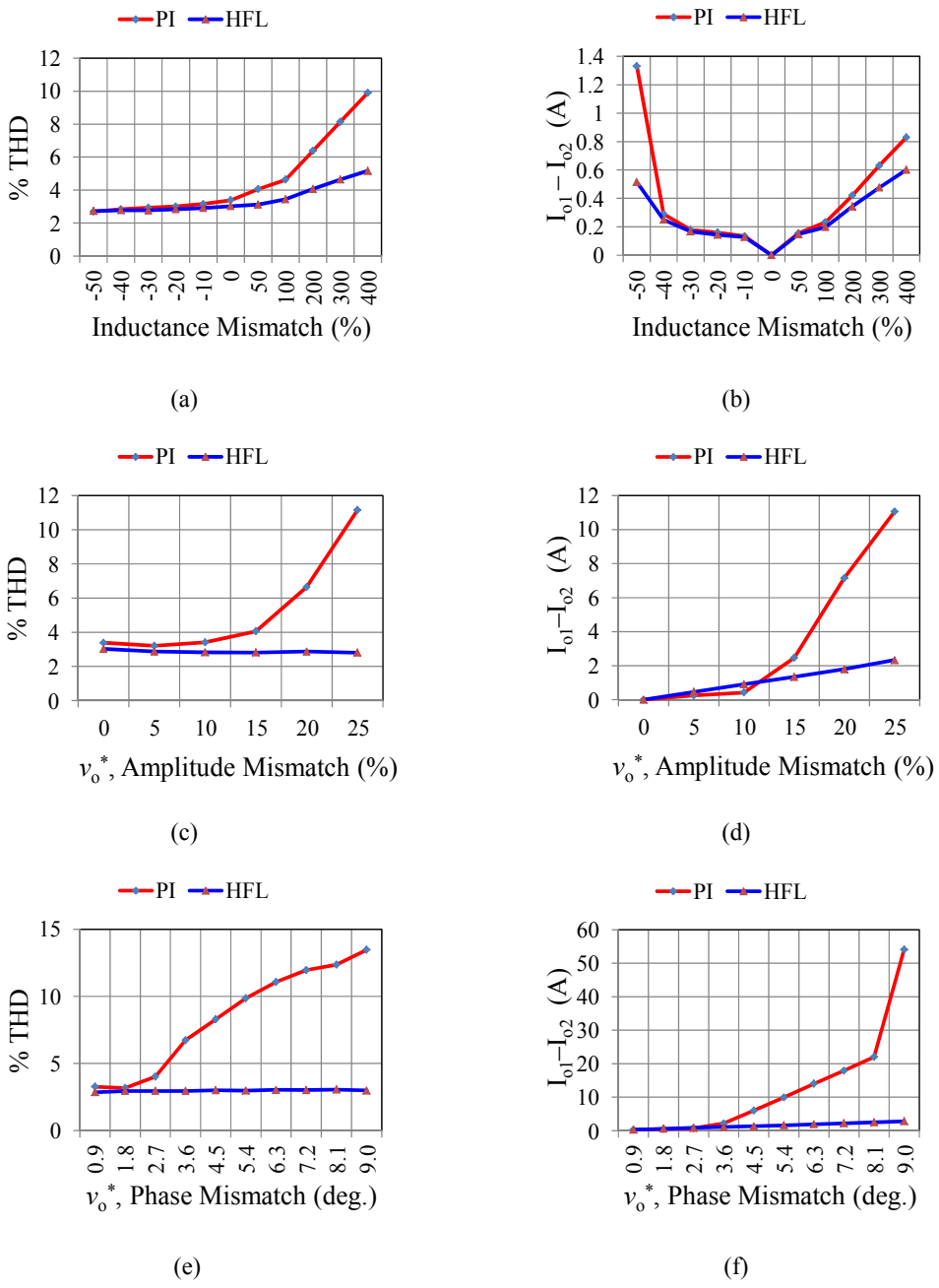


Figure 5.10 HFL Influence of parameter mismatch; %THD of load voltage: (a), (c) and (e) ; and current difference (I_{o1}-I_{o2}): (b), (d) and (f).

deviations are also plotted subsequently in Figure 5.10 (c) & (d) and Figure 5.10 (e) & (f), respectively. Clearly, over a wide range of inductance mismatch, HFL shows a better voltage regulation and current sharing capability. Also, the voltage % THD and RMS current difference variation are steeper in case of PI as compare to HFL, which shows its better insensitivity and robustness towards parametric variations.

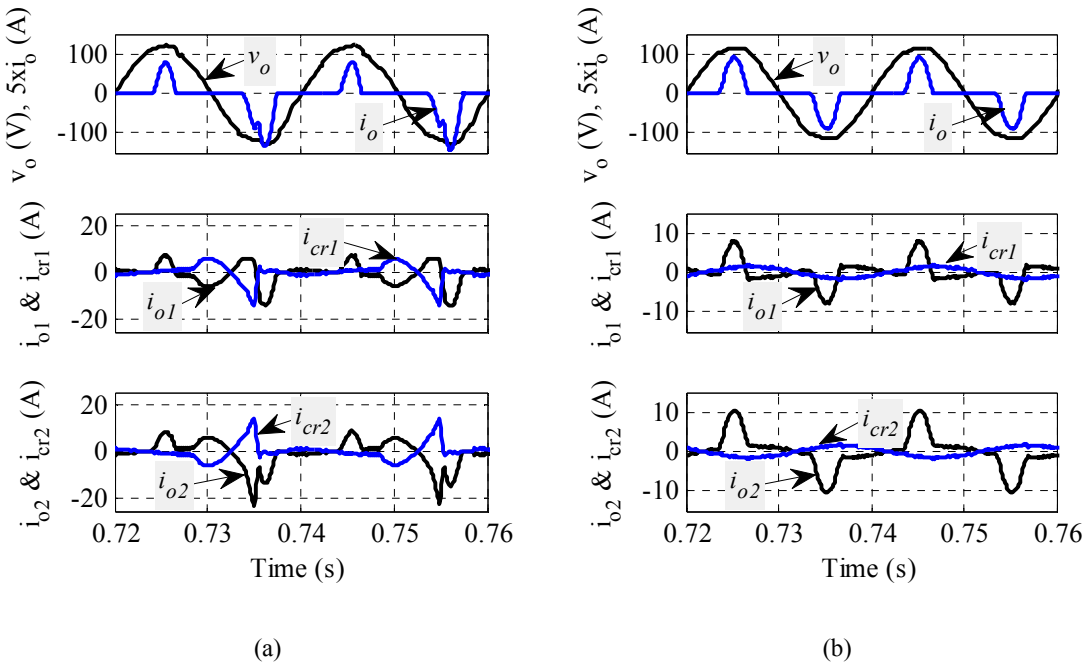
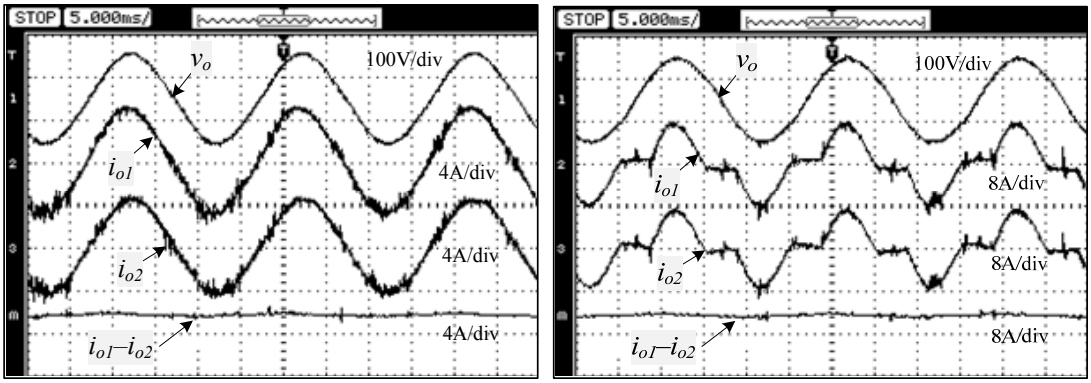


Figure 5.11 Steady-state waveforms on 50% inductance deviation (1mH, 1.5mH), 10% reference amplitude difference(80V, 88V) and 2° reference phase difference (0°, 2°) under rated non-linear load for (a) PI and (b) HFL control.

Finally, to illustrate parametric dependency in a better way, a condition of inductance difference (50%), reference-voltage amplitude deviation (10%) and reference-voltage phase deviation (2°) between the two inverters is simulated. The HFL in Figure 5.11(b) shows stable operation with proper voltage regulation and current sharing capability, as compare to unstable behavior of PI controller in the same operating condition shown in Figure 5.11(a).

5.6.2 Experimental Results

Experimental verification of the proposed current sharing control scheme using HFL has been carried out for two single-phase IGBT based inverter modules connected in parallel to a common load. With the same reference voltage for both inverter modules connected in parallel, Figure 5.12 (a) and (b) illustrate steady state waveforms on linear and non-linear loading conditions, respectively. The load voltage is indicated as v_o is well regulated and properly shared inverter currents waveform are marked as $i_{o1}$and i_{o2}. The difference between the currents i_{o1} and i_{o2}, which is twice of the circulating current for this case, is observed almost to be zero for both linear and non-linear loads respectively.



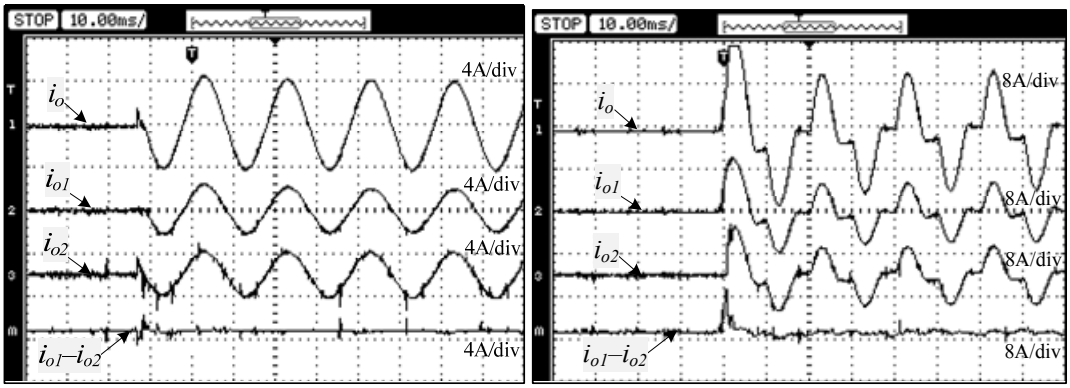
(a) (b)

Figure 5.12 Steady-state waveforms on rated load (a) Linear and (b) Non-linear.

The transient condition performance was also tested for a step variation of load from no-load to the nominal value. The corresponding waveforms are depicted in Figure 5.13(a) and (b), both for linear and non-linear loads, respectively. Equal current sharing is achieved almost instantly when an abrupt insertion of load takes place in the bi-modular parallel inverter system. The current difference (i_{o1}–i_{o2}) shows deviations only during load transitions and is almost same before and after load change. Therefore, the proposed HFL control scheme used for IACS scheme, successfully demonstrates the voltage regulation and the current sharing capability of the UPS inverters system.

5.7 Summary

Backed with advantages of fuzzy based controllers, Hierarchical Fuzzy Logic has been



(a) (b)

Figure 5.13 Transient waveforms on step load change from no-load to rated load (a) Linear (b) Non-linear.

proposed for the single-phase multi-inverter UPS system. Proposed HFL using IACS control strategy successfully establishes the current sharing capability in parallel-connected multi-inverter system. HFL on one hand eliminates the design complexity of multiple tuning of conventional PI based controllers, and on the other hand, it reduces the memory requirements of the conventional FL controllers. HFL demonstrates performance equivalence with conventional multi-variable FL control, despite of having lesser number of rules. Moreover, analysis shows a better robustness on wider parametric variations. The steady state and transient performances are well regulated for output voltage, under both linear and non-linear loading conditions. An equal current sharing is achieved with minimum circulating current under different loading conditions. Observations are validated through both simulation studies and experimental implementations.

CHAPTER 6: HYBRID ITERATIVE LEARNING BASED INSTANTANEOUS AVERAGE CURRENT SHARING CONTROL FOR MULTI-INVERTER UPS SYSTEM

6.1 Introduction

Preceding chapters have presented two IACS schemes using conventional and fuzzy based controllers for the multi-inverter UPS system. It has been shown that both control strategies achieve good voltage regulation along with excellent current sharing performances under different loading conditions. The fuzzy based HFL IACS has a design that is more straightforward and presents higher robustness towards parametric variations. However, both the control schemes use at least three sensors per inverter module, which inevitably raises their cost of implementation.

In recent years, learning controllers such as repetitive and iterative have been becoming popular for UPS applications [57], [104], [106], [193]. Such a strategy becomes valid in cases where the system response or disturbances are periodic/repetitive in nature and the plant dynamics are consistent. Learning controllers adjust their control effort using information stored in preceding cycles to correct the present cycle, i.e., it learns from previous experience like humans. Therefore, it is a kind of integral controller whose action is not limited for immediate sampling steps but on the fundamental-cycle basis. If the plant uncertainty and disturbances are pre-determined on an evenly distributed time axis, then this control can compensate for uncertainties and disturbances in subsequent periods. Moreover, learning controllers accomplish this without much detail of the system and only on the basis of input-output error. Although, they are excellent control strategies for steady state performance, but lacks in transients due to their slow response. This is due to its very nature of the control action, which requires at least one cycle delay for its operation. Therefore, in practical applications, slow dynamics and poor performance due to non-periodic disturbances are the major limitations of such a control technique.

In UPS applications, since control objective is to track the sinusoidal reference voltage, which is typically periodic in nature, only capacitor voltage feedback using a single sensor is sufficient enough to achieve the said objective with the learning based control schemes. Non-linear loads cause more severe distortions of the output voltage in a single-loop control, however due to repetitive nature of load current, such disturbances can be eliminated using learning control. However, the magnitude-frequency characteristics of the inverter LC filter

has a high peak at the resonant frequency, which poses a threat of instability when transitions are near to that frequency values. Hence, harmonic load disturbance rejection is not an issue with the learning control but the concern is poorly damped inverter plant. Therefore, cancellation of this peak is required before any control action may be applied. Digital solutions, such as a low pass filter with a matched zero-phase notch filter have been proposed in [57], [106] . However, slight parametric variations in inductor or capacitor may defy the matching of filters and the consequent magnitude-frequency characteristics. Moreover, higher order digital filters require more processing time and memory, thereby increasing processor's computational burden.

This Chapter proposes a novel IACS scheme using Hybrid Iterative Learning (HIL) control for parallel-connected multi-inverter UPS system. It can overcome the drawbacks of the learning based Iterative Learning (IL) control by combining a relatively faster controller, like PI. The HIL has both the features of excellent steady state and transient response of IL and PI controllers, respectively. Further, in order to damp the resonant peak of the LC filter, an inductor current feedback has been introduced for AD. This has a distinct advantage that with the same inductor current sensing, IACS control can be simultaneously realised on parallel operation of the multi-inverter system. In this way, sensor count reduces to '2*N*' for the proposed HIL based IACS instead of '3*N*' as in conventional control schemes.

Initiating with brief summary of the IL control, proposition of the HIL based IACS control scheme system configuration has been presented. In sequence, design has been carried out using frequency response analysis and performance evaluation has been accomplished through MATLAB/Simulink simulations. Finally, the control strategy has also been verified with experimental implementation.

6.2 Principle of Iterative Learning Control

Iterative learning control strategy is a promising solution to systems, which exhibit repetitive behaviour and execute the same task again and again. It utilizes the system repetitions as experience to improve the control performance even without knowing the complete information of the system. The main idea behind IL control is to iteratively find an input sequence such that the output of the system is as close as possible to the desired output [104]. The simplest formulation of IL control algorithm may be a proportional IL or P-type IL [104], [194], discussed in the following sub-section.

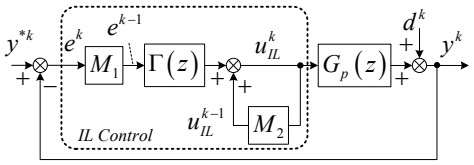


Figure 6.1 Block schematic representation of P-type IL control.

6.2.1 P-type IL Control

Figure 6.1 shows a generalised P-type IL control structure which regulates the k^{th} cycle output y^k of the plant $G_p(z)$. The k^{th} cycle control signal u_{IL}^k is adjusted iteratively from the previous cycle control signal u_{IL}^{k-1} and the learning update algorithm applied to previous repetition e^{k-1}. The memory blocks M_1 and M_2 delay the tracking error e^k and control signal u_{IL}^k respectively, by a complete iterative cycle. Hence, provided the closed loop system is stable, tracking error reduces to zero in finite time with the present iteration equals to the previous cycle of the control signal u_{IL}. Since, applied reference command is purely repetitive i.e., at each iteration its value is constant and hence $y^{*k} = y^{*k-1} = y^*$.

The P-type IL control algorithm as given in Figure 6.1 may be represented by,

$$u_{IL}^k(z) = u_{IL}^{k-1}(z) + \Gamma(z)e^{k-1}(z) \tag{6.1}$$

where, (z) denotes the z-transform of the respective signals. '$\Gamma(z)$' refers to a learning factor or designed compensator transfer function. The k^{th} iteration error $e^k(z)$ between the reference input $y^*(z)$ and actual output $y^k(z)$ of the plant may be expressed as ,

$$e^k(z) = y^*(z) - y^k(z) \tag{6.2}$$

$$\text{where, } y^k(z) = G_p(z)u_{IL}^k(z) + d^k(z)$$

Since, disturbances are periodically repetitive i.e., $d^k(z) = d^{k-1}(z)$, substitution of (6.1) into (6.2) yields

$$e^k(z) = \left\{1 - \Gamma(z)G_p(z)\right\}e^{k-1}(z) \tag{6.3}$$

Error at the k^{th} iteration will decay over successive trials, if

$$\left|1 - \Gamma(z)G_p(z)\right|_{z=e^{j\omega T_s}} < 1, \quad \forall\ 0 < \omega \le \pi/T_s \tag{6.4}$$

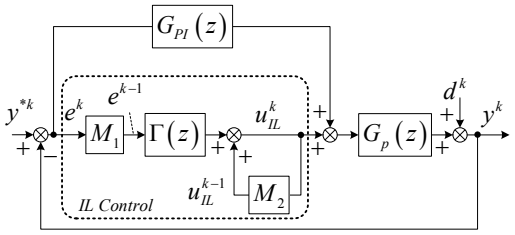


Figure 6.2 Block structure of Hybrid IL (HIL) control.

The quantity $\left|1-\Gamma\left(e^{\hat{i}\omega T_s}\right)G_p\left(e^{\hat{i}\omega T_s}\right)\right|$ is designated as the Error Decay Factor (EDF), where T_s is the sampling interval. EDF imposes an error decay condition for all frequencies, failing which leads towards amplification of error at that respective frequency. Further, a smaller EDF is desirable for faster error convergence. Thus, in designing $\Gamma(z)$, EDF should obey the stability condition (6.4) with a minimum value at the operating frequency.

6.2.2 Hybrid Iterative Learning Control

The P-type IL control is very effective in providing steady-state harmonic compensation, eliminating repetitive disturbances even in case of non-linear loads. However, transient or intra-cycle disturbances do not produce a good response and the controller takes multiple cycles to settle down. Therefore, a hybrid P-type IL control strategy is preferable for the UPS applications wherein, a fast controller is combined with the IL control to improve the poor dynamic response.

The Hybrid IL controller is shown in Figure 6.2, wherein a proportional integral controller $G_{PI}(z)$ is added in parallel to the simple P-type IL control. Therefore, the effective control signal applied to the plant may be expressed as,

$$u_c^k(z) = u_{IL}^k(z) + G_{PI}(z)e^k(z) \tag{6.5}$$

The error $e^k(z)$ between the reference and actual signal is obtained from Figure 6.2 as

$$e^k(z) = y^*(z) - y^k(z) \tag{6.6}$$
$$\text{where, } y^k(z) = G_p(z)u_c^k(z) + d^k(z)$$

Using (6.1), (6.5) and (6.6),

$$e^k(z) = y^*(z) - G_p(z)u_c^{k-1}(z) - d^k(z) - G_p(z)\begin{bmatrix}\Gamma(z)e^{k-1}(z) + G_{PI}(z)e^k(z)\\ +G_{PI}(z)e^{k-1}(z)\end{bmatrix} \tag{6.7}$$

After rearranging (6.7), the relation between subsequent iterations error is obtained as

$$e^k(z)=\frac{1-\Gamma(z)G_p(z)+G_{PI}(z)G_p(z)}{1+G_{PI}(z)G_p(z)}e^{k-1}(z)=\left\{1-\Gamma(z)\frac{G_p(z)}{1+G_{PI}(z)G_p(z)}\right\}e^{k-1}(z) \tag{6.8}$$

Therefore, the stability criterion for HIL control system becomes,

$$\left|1-\Gamma(z)\frac{G_p(z)}{1+G_{PI}(z)G_p(z)}\right|_{z=e^{j\omega T_s}}<1, \qquad \forall\ 0<\omega\le\pi/T_s \tag{6.9}$$

Subsequently on comparison of (6.8) with (6.3), the effective plant $G_{peff}(z)$ experienced by the IL controller can be deduced as,

$$G_{peff}(z)=\frac{G_p(z)}{1+G_{PI}(z)G_p(z)} \tag{6.10}$$

Therefore, the design of IL controller in HIL control scheme needs to also include the PI compensator while its design, rather than just the plant $G_p(z)$ only.

6.3 Proposed HIL Based IACS Control Scheme

The present section proposes a hybrid iterative learning based IACS control scheme for multi-inverter UPS system. HIL is expected with better dynamic response when compared to conventional IL control and inductor current feedback based IACS scheme to solve the dual purpose of AD and current sharing with a single sensing.

6.3.1 System Overview

Figure 6.3 shows the HIL based IACS control scheme for parallel multi-inverter UPS

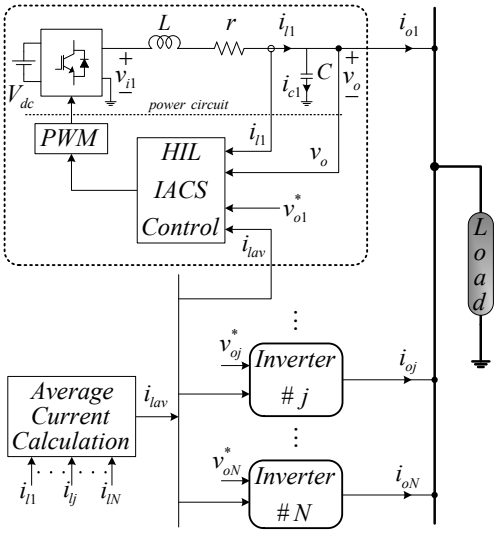


Figure 6.3 HIL based IACS control starategy for parallel connected multi-inverter system.

system connected to a common load. Each UPS module consists of an H-Bridge inverter supplied by a DC power source V_{dcj} and an output ripple smoothening LC filter. L_j, r_j and C_j represent inductance, inductor ESR and capacitance of the filter, respectively for the j^{th} inverter module. The measured inductor current i_{lj} of all modules are sent to the Average Current Computation (ACC) block to synthesize the reference averaged inductor current value for the implementation of current sharing control. The other reference signal is the output voltage v_{oj}^{*} command for independent voltage regulation of the respective inverters. The same inductor current i_{lj}, which was sent to ACC block, and the actual capacitor voltage are the only two measured signals for the control system implementation of each inverter module.

In the previous chapters, equal load sharing has been achieved using output currents i_o of the inverters. In the proposed HIL based IACS control scheme inductor current i_l has been used to implement the current sharing loop. The current sharing equivalence of the inductor current i_l and the output currents i_o can be established from the following analysis. From the power circuit of Figure 6.3, the inverter output voltage may be written as:

$$v_o(s) = v_{ij}(s) - (sL + r) i_{lj}(s) \tag{6.11}$$

And,

$$i_{lj} = i_{oj} + sCv_o \tag{6.12}$$

Assuming, circuit parameters to be consistent and summing all the equations when j varies from 1 to N in (6.11) gives,

$$v_o(s) = v_{iav}(s) - (sL + r) i_{lav}(s) \tag{6.13}$$

$$\text{where } v_{iav}(s) = \frac{1}{N}\sum_{j=1}^{N} v_{ij}(s),\ i_{lav}(s) = \frac{1}{N}\sum_{j=1}^{N} i_{lj}(s)$$

Subtracting (6.11) from (6.13), gives

$$i_{lav} - i_{lj} = \frac{v_{iav} - v_{ij}}{sL + r} \tag{6.14}$$

Now summing (6.12) for all j, as it varies from 1 to N, we get

$$i_{lav} = i_{oav} + sCv_o \tag{6.15}$$

$$\text{where } i_{oav} = \frac{1}{N}\sum_{j=1}^{N} i_{oj}$$

Subtracting (6.12) from (6.15), and using (6.14) gives the circulating current

$$i_{lav} - i_{lj} = i_{oav} - i_{oj} = \frac{v_{iav} - v_{ij}}{sL + r} = i_{crj} \tag{6.16}$$

Therefore, we can conclude that, circulating current i_{crj} definition obtained from output load current is same as it is obtained for the filter inductor current. The circulating current

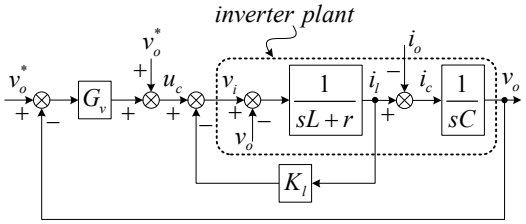


Figure 6.4 Closed-loop voltage control for unit inverter system.

produced by differences of the inverter-bridge voltage v_{ij} and can be controlled by changing the reference command to a value, which can reduce the circulating current. Therefore, if the 'j^{th}' inverter's inductor current equals the average value of all inductor currents, then its circulating current would become zero.

6.3.2 HIL Control of the Unit Inverter

6.3.2.1 Modification of primitive inverter plant

Figure 6.4 shows the block diagram representation of a closed-loop voltage control for an inverter unit in the continuous-time domain. The control scheme has a multi-loop structure, in which innermost AD current loop improves the inverter system stability by shaving off the filter resonance peak. Inductor current i_l feedback has been utilised for the implementation of active damping. Introduction of AD loop basically modifies the plant dynamics experienced by the voltage controller and hence, its design criteria. Amalgamation of the AD loop with the plant model results in the following relation for the inverter output:

$$\begin{aligned} v_o(s) &= \frac{1}{LCs^2 + C(r+K_l)s+1} u_c(s) - \frac{sL+r+K_l}{LCs^2 + C(r+K_l)s+1} i_o(s) \\ &= G_{pd}(s)u_c(s) + Z_{pd}(s)i_o(s) = G_{pd}(s)u_c(s) + d(s) \end{aligned} \tag{6.17}$$

where $G_{pd}(s)$ and $Z_{pd}(s)$ represent the effects of control input voltage u_c and load current i_o respectively, on the output voltage v_o. The inductor current feedback gain K_l basically, increases the damping coefficient without increasing ESR or inserting an additional physical resistor in the power circuit. As a consequence, the effective plant seen by the controller is $G_{pd}(s)$ with better damping characteristics. In (6.17), i_o generally is an unknown or a variable parameter dependent on the load and thus, $Z_{pd}(s)i_o(s)$ can be regarded as a disturbance $d(s)$ to the command voltage. The feedback gain K_l also appears in the $Z_{pd}(s)$ or $d(s)$ expression, which eventually escalates load current disturbance. That is why inductor current is not a preferred AD variable for the voltage regulation.

6.3.2.2 Proposed HIL Control for Unit Inverter

Voltage controller $G_v(s)$ can simply be a proportional-integral based, since after AD inverter plant is invariably a stable system. However, loop gain of the PI is only finite at the operating frequency and would results in a large error at steady-state condition. Therefore, synchronous frame PI has to be implemented which is a complicated affair for the single phase applications [179]. Although PR can be an option, but fixed point DSP implementation is a major issue and moreover, multiple harmonic compensators are needed for the complete elimination of load disturbances. To avoid these complexities, learning based controllers may be a viable solution for the single-phase UPS inverters.

Simple IL control has poor dynamic performance under an aperiodic phenomenon such as step load change. And, since it is a crucial requirement in UPS applications, a hybrid scheme consisting of IL and PI controllers, as shown in Figure 6.5 has been proposed for single-phase inverters. Despite having poor steady-state performance, PI has fairly good dynamic response for applications such as, UPS. Therefore, it can be combined with IL control in parallel whose outputs are summed. The intrinsic nature of the controllers allows good steady-state compensation primarily by the IL control and the dynamic response is regulated by the PI control, almost in an independent manner. A feed-forward reference voltage has also been added to the HIL output to improve the tracking and robustness of the control strategy. Load current and other disturbances such as, switch dead-time etc., can be accumulated as d^k. Since, the load current is repetitive in nature, subsequent cycles iteratively reduce d^k to zero in steady-state. Therefore, HIL can be a very-much preferred solution for UPS inverters with inductor current AD loop having higher output impedance.

The PI controller has the following form in z-domain as obtained in Appendix E,

$$G_{PI}(z) = K_p + K_i \frac{zT_s}{z-1} \tag{6.18}$$

Figure 6.5 also shows the details of blocks used in P-type IL control. $\Gamma(z)$, specified as the '*Learning Factor'*, which includes three components: learning gain 'K', loop shaping

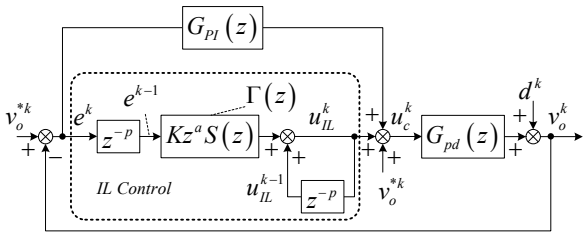


Figure 6.5 HIL control for unit inverter UPS system.

compensator '$S(z)$' and a phase correction factor 'z^a', where 'a' refers to the number of sample advancements. One cycle or period delay in discrete-domain can be represented as z^{-p}, where, $p= f_s / f$ is the number of samples with $f_s=1/T_s$ being the sampling frequency and f being the reference signal frequency.

The UPS inverter model with AD in s-domain of (6.17) can be realised as a plant $G_{pd}(z)$ with disturbance component '$d(z)$' in z-domain, as shown Figure 6.5. The close-loop output voltage for HIL control can be derived from Figure 6.5 as:

$$v_o^k(z) = G_{pd}(z)v_o^{*k}(z) + \left\{\frac{\Gamma(z)}{z^p - 1} + G_{PI}(z)\right\} G_{pd}(z)(z)e^k(z) + d^k(z) \tag{6.19}$$

Since $e^k = v_o^* - v_o^k$, and on substitution in (6.19) and rearrangement gives

$$\left[1 + \left\{\frac{\Gamma(z)}{z^p - 1} + G_{PI}(z)\right\} G_{pd}(z)\right] v_o^k(z) = \left[1 + \left\{\frac{\Gamma(z)}{z^p - 1} + G_{PI}(z)\right\}\right] G_{pd}(z)v_o^{*k}(z) + d^k(z) \tag{6.20}$$

Further, (6.20) can be reorganised as

$$\begin{aligned} v_o^k(z) = {} & \frac{(z^p - 1)G_{pd}(z) + \{\Gamma(z) + (z^p - 1)G_{PI}(z)\} G_{pd}(z)}{(z^p - 1) + \{\Gamma(z) + (z^p - 1)G_{PI}(z)\} G_{pd}(z)} v_o^{*k}(z) \\ & + \frac{(z^p - 1)}{(z^p - 1) + \{\Gamma(z) + (z^p - 1)G_{PI}(z)\} G_{pd}(z)} d^k(z) \end{aligned} \tag{6.21}$$

Given, the condition that the load current disturbance is to be repetitive, i.e., $z^p d^k(z) = d^k(z)$, the second term approaches to zero in steady-state. It can be seen from (6.21) that an IL based controller is very much suited for such a control topology with large output impedance, since the repetitive load disturbances die out on successive iterations. Letting, the second term to be zero and simplification of (6.21) gives following,

$$\begin{aligned} & \{1 + G_{PI}(z)G_{pd}(z)\} z^p v_o^k(z) - \{1 - \Gamma(z)G_{pd}(z) + G_{PI}(z)G_{pd}(z)\} v_o^k(z) \\ & \quad = \{G_{pd}(z) + G_{PI}(z)G_{pd}(z)\} z^p v_o^{*k}(z) - \{G_{pd}(z) - \Gamma(z)G_{pd}(z) + G_{PI}(z)G_{pd}(z)\} v_o^{*k}(z) \end{aligned} \tag{6.22}$$

As z^p is one cycle shift operator, multiplication of it gives next iteration samples i.e., $z^p v_o^k(z) = v_o^{k+1}(z)$ and $z^p v_o^{*k}(z) = v_o^{*k+1}(z)$, hence (6.22) can be written as:

$$\begin{aligned} & \{G_{pd}(z) + G_{PI}(z)G_{pd}(z)\} v_o^{*k+1}(z) - \{1 + G_{PI}(z)G_{pd}(z)\} v_o^{k+1}(z) \\ & \quad = \{G_{pd}(z) - \Gamma(z)G_{pd}(z) + G_{PI}(z)G_{pd}(z)\} v_o^{*k}(z) - \{1 - \Gamma(z)G_{pd}(z) + G_{PI}(z)G_{pd}(z)\} v_o^k(z) \end{aligned} \tag{6.23}$$

Since, reference voltage is a pure repetitive signal and hence, $v_o^{*k+1}(z) = v_o^{*k}(z)$. Therefore, on cancellation of $G_{pd}(z)v_o^{*k}(z)$ and addition of $v_o^{*k}(z)$ on both sides (6.23) gives

$$\begin{aligned}\left\{1+G_{PI}(z)G_{pd}(z)\right\}\left\{v_o^{*k}(z)-v_o^{k+1}(z)\right\} \\ =\left\{1+G_{PI}(z)G_{pd}(z)-\Gamma(z)G_{pd}(z)\right\}\left\{v_o^{*k}(z)-v_o^{k}(z)\right\}\end{aligned} \tag{6.24}$$

Therefore, the successive voltage error $e^{k+1}(z)$ can be obtained from (6.24) as:

$$e^{k+1}(z)=\left\{1-\frac{\Gamma(z)G_{pd}(z)}{1+G_{PI}(z)G_{pd}(z)}\right\}e^{k}(z) \tag{6.25}$$

Therefore, (6.25) is similar to (6.8) with the damped plant $G_{pd}(z)$ and the error decay condition of (6.9) for HIL makes the output voltage to follow the reference. Therefore, irrelevant of system parameters, control objective in HIL control is achieved, if the error decay condition is fulfilled.

6.3.3 HIL Based IACS Control of Multi-Inverter System

For proper current sharing on parallel operation of multi-inverter system, an additional outer current sharing IACS loop is employed, as shown in Figure 6.6. This control structure of IACS is selected, so as not to disrupt the settings of HIL voltage control loop. The current sharing loop comprises of measured inductor current feedback i_{lj}, the average inductor current i_{lav} and a current sharing compensator H_c. The output of the H_c compensator is added with the voltage command of the respective inverter to generate the adjusted voltage reference so as to minimize the current asymmetry of the parallel inverters.

6.3.3.1 Voltage Regulation of the Multi-Inverter System

The simplified block schematic of voltage regulation loop is shown in Figure 6.7 for a j^{th} module of the multi-inverter system. The reference command for the voltage loop is given as

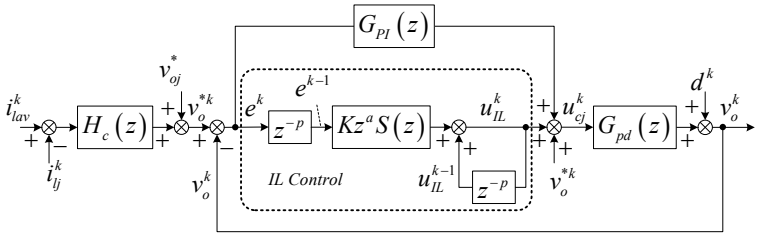


Figure 6.6 HIL IACS control for multi-inverter UPS system.

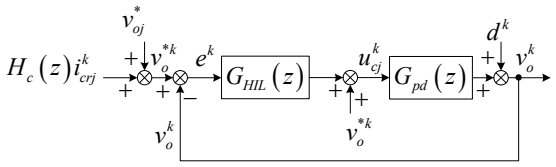


Figure 6.7 Simplified schematic of inner voltage control loop.

the sum total of j^{th} inverter voltage reference $v_{oj}{}^{*k}$ and circulating current $i_{crj}{}^k$ compensation signal,

$$v_o^{*k}(z) = v_{oj}^{*k}(z) + H_c(z) i_{crj}^k(z) \tag{6.26}$$

From Figure 6.7, the output of voltage regulation loop is:

$$v_o^k(z) = u_{cj}^k G_{pd}(z) = \left[G_{HIL}(z)\left\{ v_o^{*k}(z) - v_o^k(z) \right\} + v_o^{*k}(z) \right] G_{pd}(z) \tag{6.27}$$

which gives,

$$v_o^k(z) = \frac{G_{pd}(z) + G_{HIL}(z) G_{pd}(z)}{1 + G_{HIL}(z) G_{pd}(z)} v_o^{*k}(z) = G_{cl}^{HIL}(z) v_o^{*k}(z) \tag{6.28}$$

On substitution of (6.26) in (6.28), gives the output voltage of j^{th} module with HIL control in the paralleled system and can be expressed as,

$$v_o^k(z) = G_{cl}^{HIL}(z) v_{oj}^*(z) + H_c(z) G_{cl}^{HIL}(z) i_{crj}^k(z) \tag{6.29}$$

Further, for parallel system, module output voltage may be arranged as,

$$\begin{aligned}
v_o^k(z) &= G_{cl}^{HIL}(z) v_{o1}^*(z) + H_c(z) G_{cl}^{HIL}(z) i_{cr1}^k(z) \\
v_o^k(z) &= G_{cl}^{HIL}(z) v_{o2}^*(z) + H_c(z) G_{cl}^{H}(z) i_{cr2}^k(z) \\
&\vdots \\
v_o^k(z) &= G_{cl}^{HIL}(z) v_{oN}^*(z) + H_c(z) G_{cl}^{HIL}(z) i_{crN}^k(z)
\end{aligned} \tag{6.30}$$

Also in a parallel system, the sum of instantaneous circulating currents is zero, as obtained below,

$$\sum_{j=1}^{N} i_{crj}^k(z) = N i_{lav}(z) - \sum_{j=1}^{N} i_{lj}^k(z) = N\left(\frac{1}{N} \sum_{j=1}^{N} i_{lj}^k(z) \right) - \sum_{j=1}^{N} i_{lj}^k(z) = 0 \tag{6.31}$$

Therefore, summing all the output voltages of the parallel system gives,

$$v_o^k(z) = G_{cl}^{HIL}(z) v_{oav}^*(z) \tag{6.32}$$

$$\text{where } v_{oav}^*(z) = \frac{1}{N} \sum_{j=1}^{N} v_{oj}^*(z)$$

Equation (6.32) shows that the introduction of the current sharing loop does not affect the overall parallel system output voltage, though the output of individual inverter modules have circulating current compensator H_c term. Thus, the system output voltage-regulation characteristics do not get altered even with the inclusion of inductor current sharing loop.

6.3.3.2 Current Sharing by Suppression of Circulating Current

On subtracting, the output voltage expression of j^{th} module in (6.30) from (6.32) gives

$$G_{cl}^{HIL}(z)\left\{v_{oav}^{*}(z)-v_{oj}^{*}(z)\right\}-H_c(z)G_{cl}^{HIL}(z)i_{crj}^{k}(z)=0 \tag{6.33}$$

Henceforth, the circulating current relation is obtained as,

$$i_{crj}^{k}(z)=\frac{v_{oav}^{*}(z)-v_{oj}^{*}(z)}{H_c(z)} \tag{6.34}$$

Equation (6.34), shows that the circulating current of the multi-inverter system can be eliminated if the gain of $H_c(z)$ is kept high and is independent of the voltage regulation loop.

Now, inductor current of the j^{th} module in the parallel-connected M-M UPS system may be defined as,

$$\begin{aligned} i_{lj}^{k}(z) &= i_{lav}^{k}(z)-i_{crj}^{k}(z) \\ &= i_{lav}^{k}(z)-\frac{v_{oav}^{*}(z)-v_{oj}^{*}(z)}{H_c(z)} \end{aligned} \tag{6.35}$$

Therefore, inductor current i_{lj} is equal to the average inductor current i_{lav} as high gain of $H_c(z)$ reduces the circulating current i_{crj} and thereby, equal current sharing among inverter modules is achieved.

The choice of inductor current i_l as a current sharing variable has therefore, triple benefits with a single measurement. Firstly, damping of resonant LC peak through AD can be implemented for the better robustness of the voltage controller. Secondly, over-load protection of inverter module and finally, equal load sharing can be employed even without sensing the load current. Thus, the proposed HIL based IACS control for multi-inverter UPS system can achieve both good voltage-regulation and proper current sharing effectively. Moreover, this it can accomplish with only one current measurement per module. Therefore, the presented strategy is capable to realise equal current sharing using just '2N' sensors (one voltage and one current per module) as against '3N' sensors (one voltage and two currents per module) for the conventional IACS technique. Thus, '*N*' current sensor count can be saved in an *N*-module parallel UPS inverter system.

6.4 Controller Design

This section presents the design procedure adopted for the proposed HIL control algorithm. The design of fully digitised control system has been carried out using classical approach such as, Bode and Nyquist frequency response plots. First, the crude inverter plant has been compensated for the resonant peak to ensure proper error convergence for entire frequency spectrum in consideration. Then, PI controller design for desired bandwidth, ignoring P-type IL control in parallel, has been presented. Next, inclusion of the P-type IL control in the proposed HIL control scheme has been subsequently discussed, based on the error decay condition. Finally, outer current loop has been tuned for proper sharing of currents among inverters connected in parallel.

6.4.1 Voltage Regulation loop

6.4.1.1 Active Damping of Resonant Peak

The design initiates with shaping of the undamped plant magnitude-phase-frequency characteristics. The digital form of undamped plant model '$G_p(z)$' can be obtained from (6.17) with $K_l = 0$ using Zero-Order Hold (ZOH) discretization method at a sampling frequency of 10 kHz as,

$$G_p(z) = \frac{0.2608z + 0.2564}{z^2 - 1.434z + 0.9512} \tag{6.36}$$

The plant model $G_p(z)$ has a resonant peak of around 23dB at a frequency of 1.2 kHz as shown in Figure 6.8. Inductor current with K_l feedback gain provides an additional damping so as to impart higher robustness to the system. K_l =10 provides a damping factor ζ of 0.707, which is enough to reduce the peak to make a smooth roll-off from lower frequency to higher frequency region. Modified damped plant of (6.17) with AD, presents a new discrete transfer function using ZOH and sampling time T_s as:

$$G_{pd}(z) = \frac{0.1930z + 0.1355}{z^2 - 1.021z + 0.3499} \tag{6.37}$$

Bode-plots in Figure 6.8, clearly depict the differences in peak magnitude response of $G_p(z)$ and $G_{pd}(z)$ obtained from (6.36) and (6.37), respectively .

6.4.1.2 Design of PI Controller

PI controller connected in parallel to P-type IL controller in the HIL control strategy, has been designed by considering as if PI is working alone, ignoring any IL control. The controller has been designed using digital re-design approach, i.e., the PI controller is first designed in

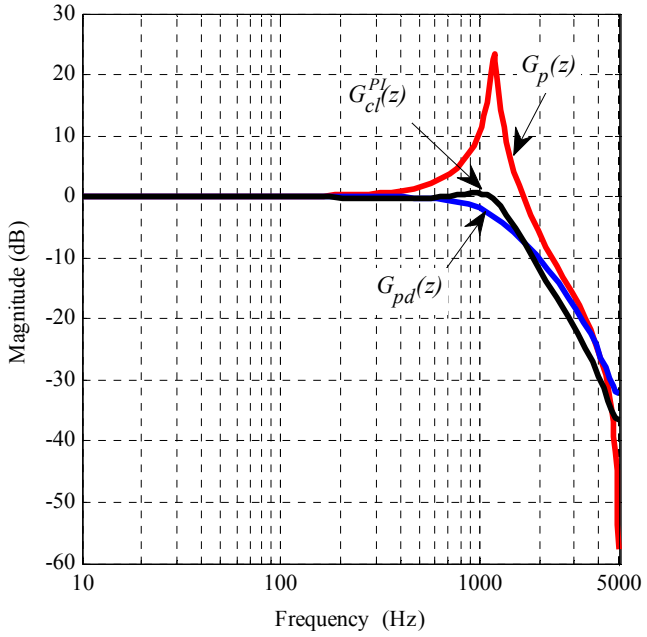


Figure 6.8 Bode-plot for undamped plant $G_p(z)$, modified damped plant $G_{pd}(z)$, and PI tuned damped plant $G_{cl}^{PI}(z)$.

continuous domain and then discretised to digital domain [195]. The closed-loop voltage gain $v_o(s)/v_o^*(s)$ can be derived from Figure 6.4 by substituting PI control in $G_v(s)$,

$$G_{cl}^{PI}(s) = \frac{v_o(s)}{v_o^*(s)} = \frac{sK_p + K_i}{s^3LC + s^2CK_l + sK_p + K_i} \tag{6.38}$$

Note that in (6.38), ESR has been considered negligible as compared to K_l and the command voltage feedforward v_o^{*k} has been included for compensating load voltage v_o^k disturbances. In this specific case, the PI controller has been designed choosing closed-loop bandwidth specification of 6283 rad/s and allowable steady-state error <1%. The selected value of K_p = 0.8 and K_i = 4000 gives pole locations of the $G_{cl}^{PI}(s)$ at (−7930) and (−1040 ± j5190), which are far from the imaginary axis on the left half of s-plane, indicating a stable system. Figure 6.8 shows the Bode-Magnitude response of $G_{cl}^{PI}(z)$ superimposed with the $G_p(z)$ and $G_{pd}(z)$ for comparison. The gain is unity (0 dB) until bandwidth frequency, and thereon a smooth rollover of magnitude plot is observed.

6.4.1.3 Design of Iterative Learning Controller with PI compensator

Hybrid IL control scheme is combination of the PI and the P type-IL control for improved dynamic response. The design of a P-type IL control comprises of determining the learning gain K, loop shaping compensator $S(z)$ and the number of sample advancements to be incorporated via phase correction factor z^a as shown in Figure 6.5. The learning gain 'K'

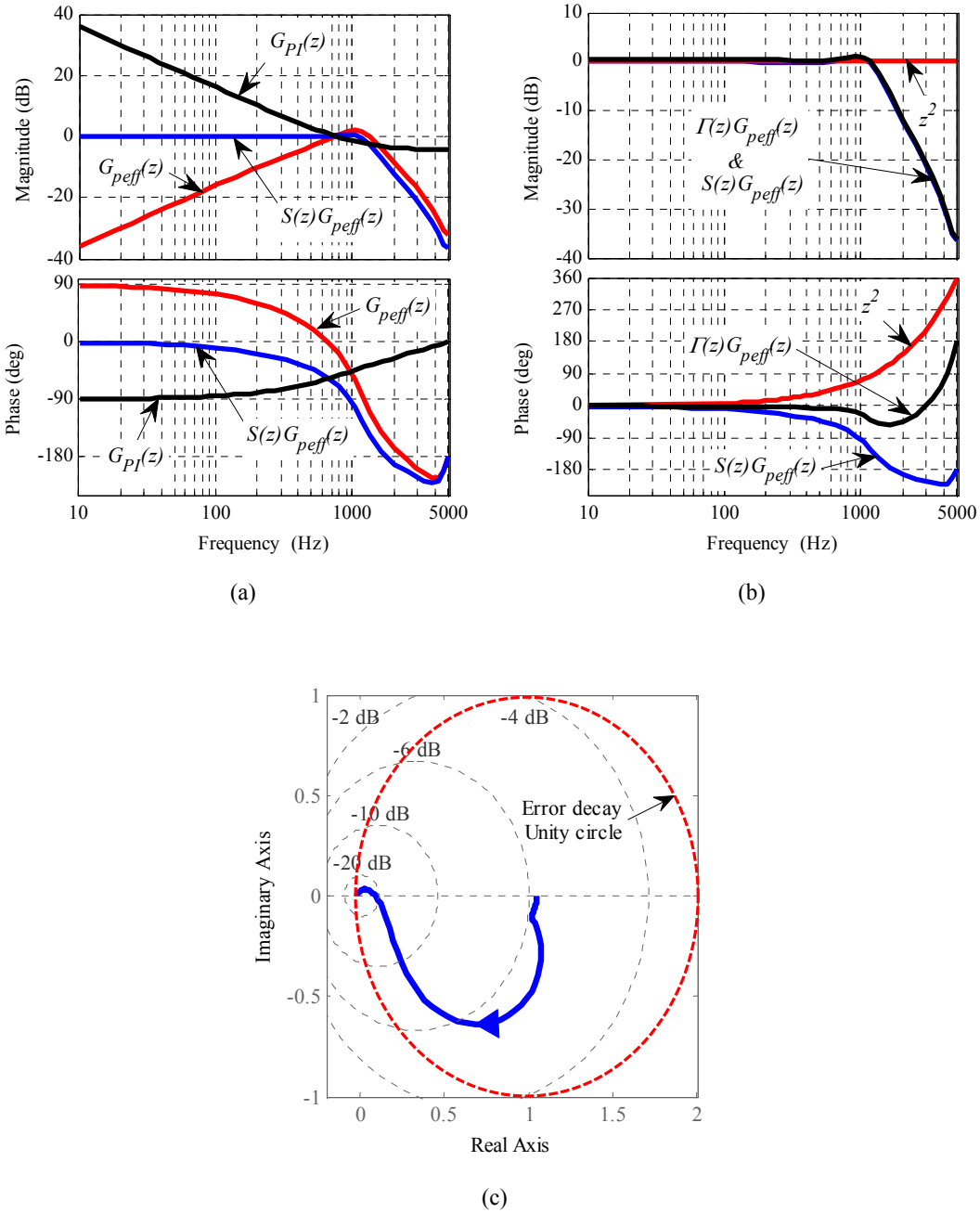


Figure 6.9 Design of HIL control (a) Bode-plot for effective plant $G_{peff}(z)$, $G_{PI}(z)$ and $S(z)G_{peff}(z)$, (b) Bode-plot for z^2, $S(z)G_{peff}(z)$ and $\Gamma(z)G_{peff}(z)$, and (c) Nyquist-plot of vector $\Gamma(z)G_{peff}(z)$.

controls the magnitude of u_{IL} (hence the speed of error convergence) with $S(z)$ shaping the magnitude characteristics of $G_{peff}(z)$ to the expected level. Therefore, sample advancements, 'z^a' are used to compensate the incurred combined phase delay due to $S(z)G_{peff}(z)$, where $G_{peff}(z)$ refers to the effective plant modelled in (6.10).

Since, the resonant peak of undamped plant has already been supressed using AD technique, the effective plant does not pose an immediate threat to stability as depicted in Bode Plots shown in Figure 6.9(a). However, the magnitude-frequency response of $G_{peff}(z)$ is highly attenuated, both below and above the resonant frequency of the LC filter. The $G_{peff}(z)$ plot is a kind of inverse $G_{PI}(z)$ as seen from dotted orange line in Figure 6.9(a), therefore $S(z)$ is selected as $G_{PI}(z)$ to reverse its effect. The compensator $S(z)$ in cascade with $G_{peff}(z)$ makes the gain of $S(z)G_{peff}(z)$ close to unity (0 dB) till cut-off frequency as shown in Figure 6.9(a). Further, the magnitude of $S(z)G_{peff}(z)$ also provides a sufficient roll-off to reject the high frequency disturbances. However, the corresponding phase plot shows a rapid lag beyond resonant frequency, which may violate the stability criterion. Therefore, a time advancement of 'z^2' shown in Figure 6.9(b) (dash-dotted magenta line) is sufficient to make the phase of $S(z)G_{peff}(z)$ within desired limits. Learning gain, K of 1.05 is selected for optimum convergence speed. Figure 6.9(b), also shows the final magnitude and phase plot for $\Gamma(z)G_{peff}(z)$ (solid green line). The magnitude is almost constant unity (0 dB) for frequencies less than the cut-off frequency with a gradual attenuation beyond it. The time advancement unit 'z^2' improves the phase lag till cut-off frequency, beyond which the phase becomes somewhat irrelevant due to the attenuation imposed by the LC filter magnitude characteristics. The attenuation is as below as −30 dB when the phase crosses +90° in the bode plot.

Now, the stability criterion of (6.9) becomes for the proposed HIL control system of UPS inverter becomes,

$$\left|1-\Gamma\left(z\right)G_{peff}\left(z\right)\right|_{z=e^{j\omega T}}<1, \qquad \forall\ 0<\omega\le\pi/T \tag{6.39}$$

$$\text{where, } \Gamma\left(z\right)=Kz^{a}S\left(z\right) \text{ and } G_{peff}\left(z\right)=\frac{G_{pd}\left(z\right)}{1+G_{PI}\left(z\right)G_{pd}\left(z\right)}$$

Error decay condition of (6.39) dictates the IL controller stability criterion. This condition can be represented in Nyquist diagram, where the locus of vector $\Gamma(e^{j\omega T})G_{peff}(e^{j\omega T})$ should not exceed the unit circle with a centre point at (1, 0) and ω is varied from 0 to 31410 rad/s (Nyquist frequency for the sampling frequency of 10kHz). Therefore, once the learning factor $\Gamma(z)$ is determined, the stability condition has to be verified. If not violated, design is finalised otherwise $\Gamma(z)$ needs another design iteration. The locus of the vector $\Gamma(e^{j\omega T})G_{peff}(e^{j\omega T})$ shown in Figure 6.9(c) is well within unit circle of unity error condition as ω sweeps from 0 to Nyquist

Frequency (31410 rad/s). This completes the design procedure of HIL voltage controller for unit inverter and the subsequent current sharing regulator for parallel operation is discussed in the next sub-section.

6.4.2 Design of Current Sharing Control Loop

From (6.35), it can be observed that $H_c(z)$ compensator plays an important role in suppression of the circulating current. The circulating current impedance of the parallel multi-inverter modules can be varied by setting the appropriate $H_c(z)$ gain. The $H_c(z)$ may be a P-type or the circulating current impedance, Z_{cr} can be a pure resistor to provide a constant impedance throughout the entire frequency spectrum. Therefore, an arbitrarily high gain of H_c sets a large enough circulating current impedance to supress the circulating current and achieve a current-sharing control. In this investigation, H_c = 2 has been selected for the current sharing compensator.

6.5 Results and Discussions

The proposed HIL based IACS control scheme has been first investigated in MATLAB/Simulink environment through simulations in DTF. Thereafter, an experimental prototype has been implemented using TMS320F2812 DSP based controller for validation of the proposed control strategy. The complete investigation may be divided into two parts:

(i) HIL control verification for unit inverter and

(ii) HIL IACS control scheme applied to multi-inverter (two-inverter) system.

6.5.1 Simulation Investigations on Unit Inverter

The UPS inverter uses controller data provided in Table D.6 of Appendix D for DTF simulations in MATLAB R1013b environment. For comparison, system response with PI and P-type IL control has also been implemented along with the HIL control. The improvements in steady-state performance with HIL control has been investigated and compared with that of the PI controller. In addition, the dynamic performance using HIL control has been compared against the IL control technique.

Figure 6.10 (a) and (b) show the simulated steady-state load voltage, voltage tracking error and load current waveforms of the inverter system when connected to resistive load under rated conditions using PI and HIL control, respectively. The voltage tracking error for inverter control with PI in Figure 6.10(a) clearly shows a large steady state error as compared to that of HIL control strategy in Figure 6.10(b). The AD gain K_l is causing a drop in voltage for linear load

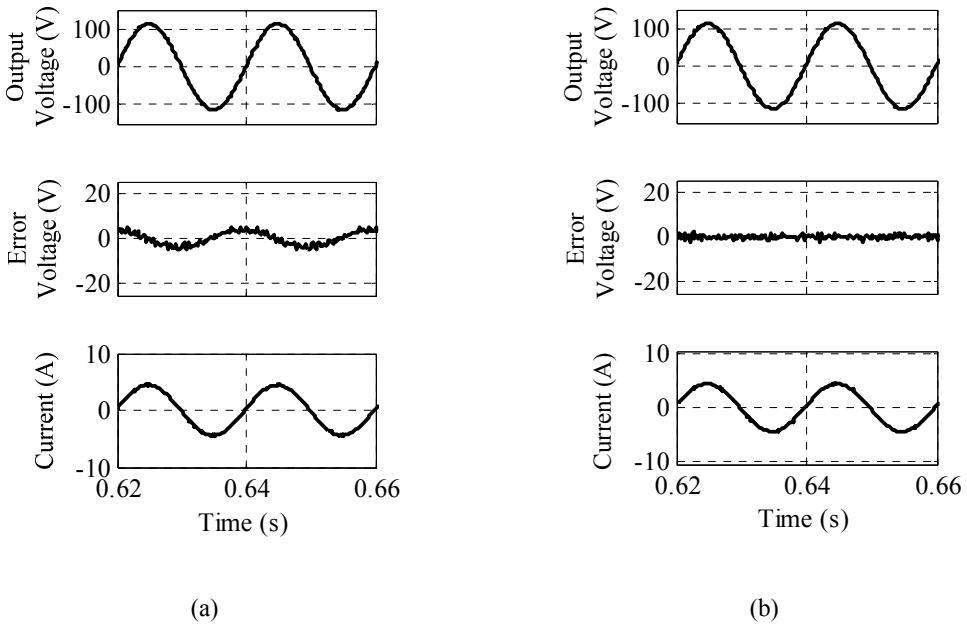


Figure 6.10 Steady-state waveforms under rated linear load for (a) PI and (b) HIL control.

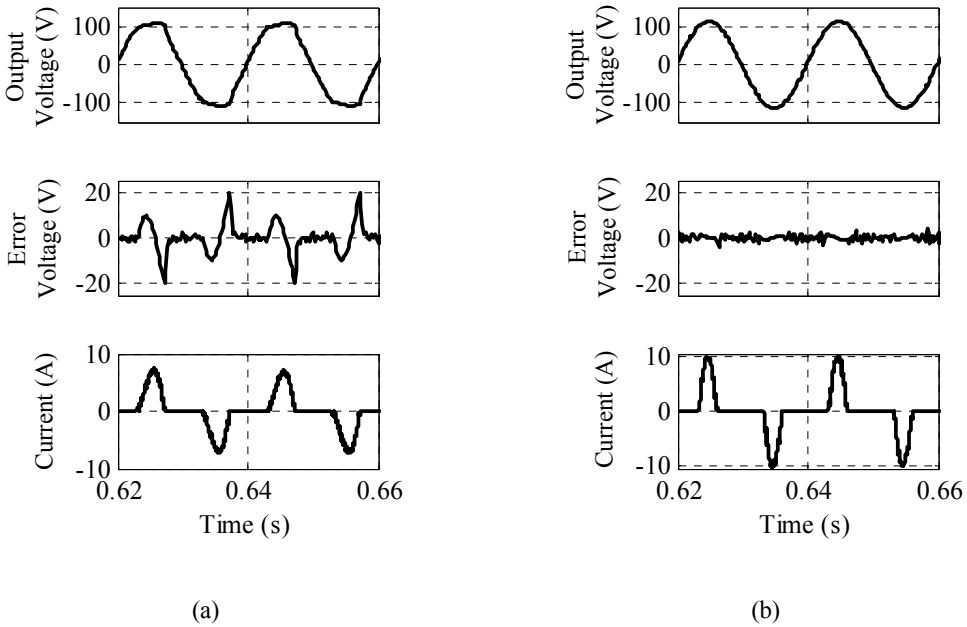


Figure 6.11 Steady-state waveforms under rated non-linear load for (a) PI and (b) HIL control.

with PI controller whereas in case of HIL control no such drop is observed. The iterative action of HIL control totally eradicates the load current disturbances.

Simulated steady-state waveforms of the inverter at rated non-linear load are compared in Figure 6.11(a) and (b) for PI and HIL control, respectively. The voltage tracking error is

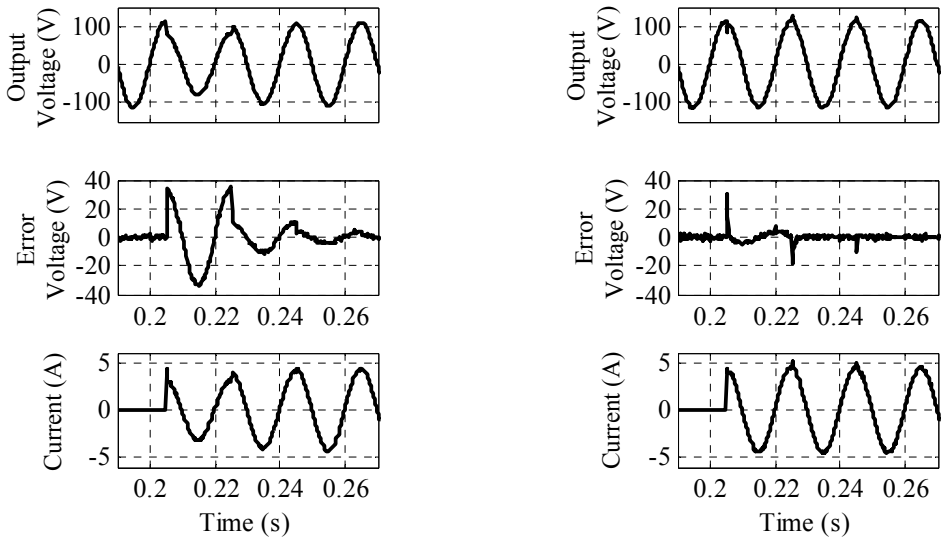


Figure 6.12 Transient response under rated linear load for (a) IL and (b) HIL control.

definitely very large with PI control and the output voltage quality is observed to be degraded. This is largely due to high output harmonic impedance provided by the gain K_I. This is also reflected from THD values of 7.37% and voltage error of 7.81% given in Table 6.1. With same conditions, HIL control maintains an excellent performance even with the non-linear loads as with resistive loads. The waveforms clearly show that HIL control presents low output impedance for harmonic components in the load current and hence better disturbance rejection capability. Thus, HIL strategy eliminates larger disturbances due to presence of high gain in the inductor current AD loop.

The transient condition performance has also been studied on step load application for IL and HIL control strategies respectively as shown in Figure 6.12(a) and (b). Slower transient response on load application is in conformity with the sluggish behaviour of IL control strategy.

Table 6.1 Performance comparison

	LINEAR LOAD			NON–LINEAR LOAD		
	PI	***IL***	***HIL***	***PI***	***IL***	***HIL***
%THD	1.07	–	0.97	7.37	–	1.41
% Error	2.56	–	1.13	7.81	–	1.63
Settling time(ms)	–	105	65	–	355	145

Note: % Error $=100 \times (v_o^* - v_o)/v_o^*$

Proposed HIL control achieves steady conditions within one to two cycles as seen from the tracking error response in Figure 6.12(b).

Table 6.1 summarizes the dynamic performance (under steady state) for PI, IL and HIL control respectively, for both linear and non-linear loads under rated conditions. Tabulated data clearly shows that HIL control can achieve a better performance (%THD and %error) than PI control. It also, shows that transient performance (in terms of settling time) of IL control gets improved, if HIL control strategy is applied.

The individual outputs of the PI and IL control of HIL are shown in Figure 6.13 to have an insight of the constituent-controllers operation. Majority of the HIL control output signal is contributed by the reference feedforward while the PI and IL compensate for the load

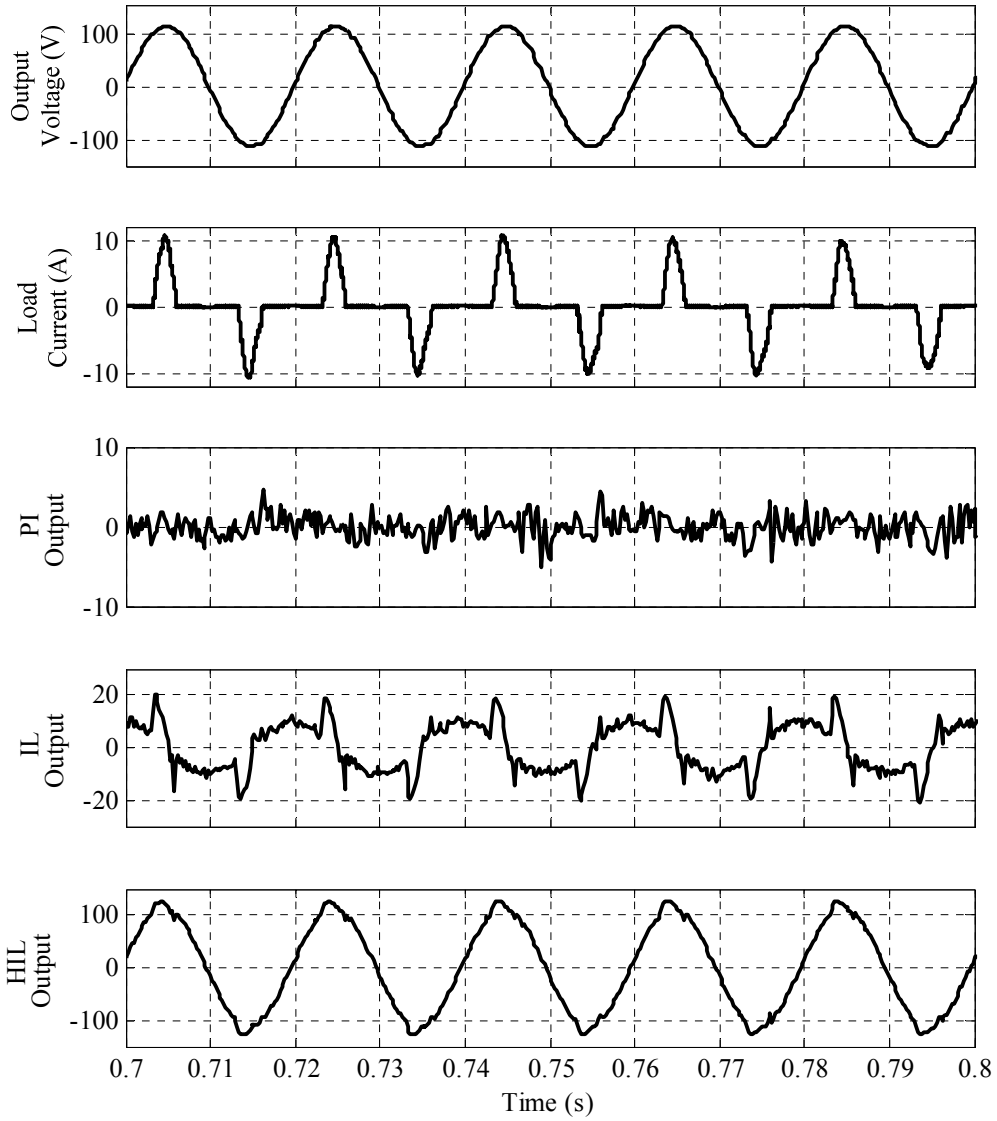


Figure 6.13 Controller response in steady-state under non-linear load.

disturbances. Rather, in steady state it can be seen that only IL controller primarily provides disturbance compensation. As seen from the Figure 6.13, since load current demand or disturbance is periodic, even though load is non-linear, learning based HIL controller is very much effective in such cases, also. However, since the control action of learning based controller depends on the previous cycle information, the transient response is compromised in this case. Figure 6.14 shows constituent-controller's output when the rated resistive load is applied and removed from the inverter terminals. In this case, the PI controller provides majority of the HIL control effort during transitions of the load.

This clearly, demonstrates the capability of the proposed controller in both steady-state and transient conditions. The IL controller primarily compensates the steady-state response

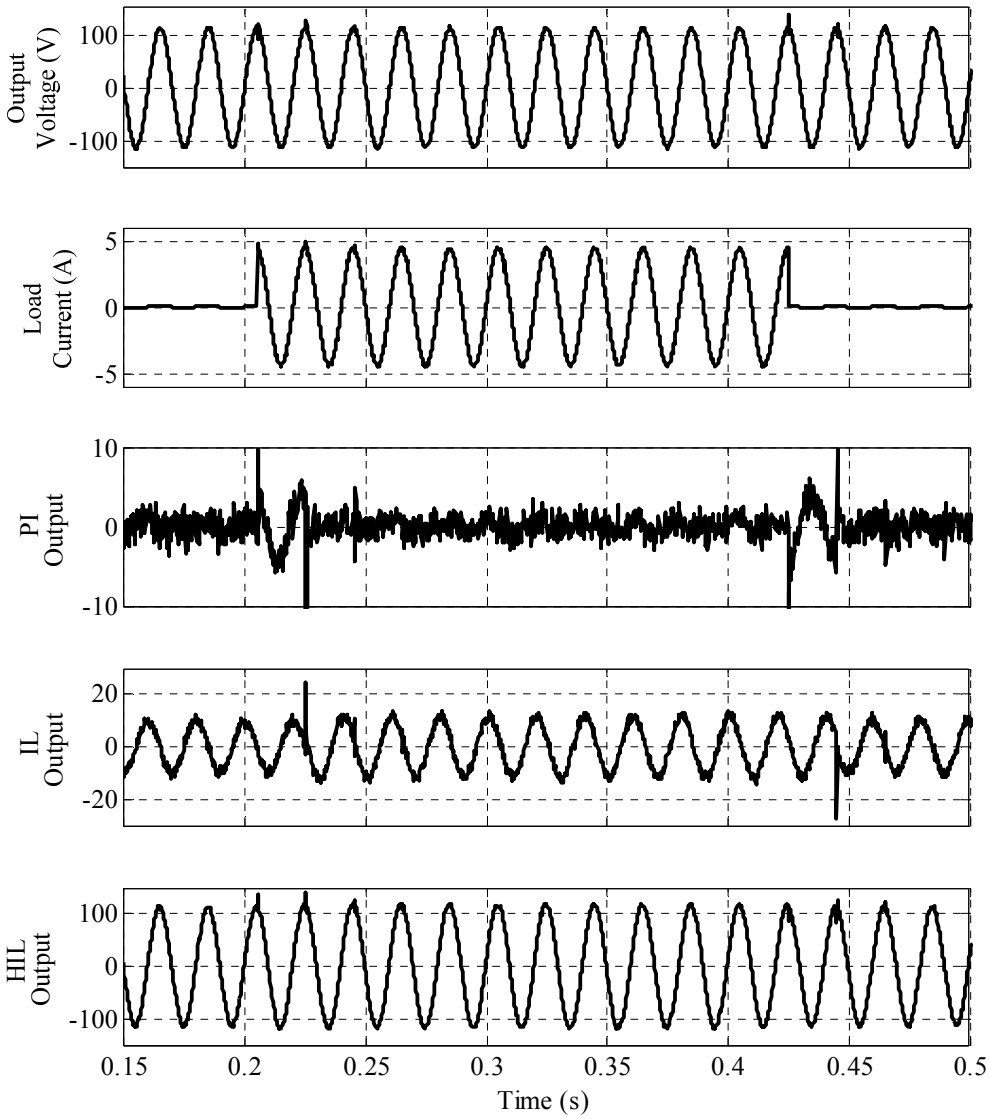


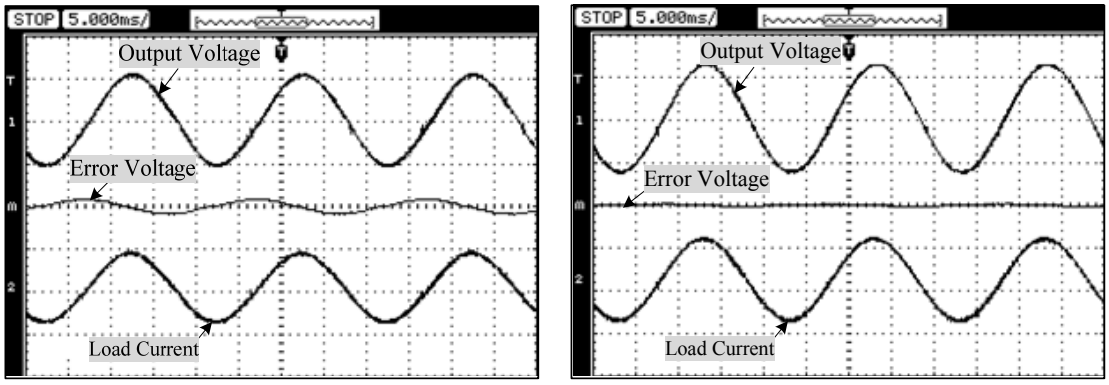
Figure 6.14 Controller response during load transitions.

whereas the PI controller compensates the transient dynamics.

6.5.2 Experimental Results of Unit Inverter system

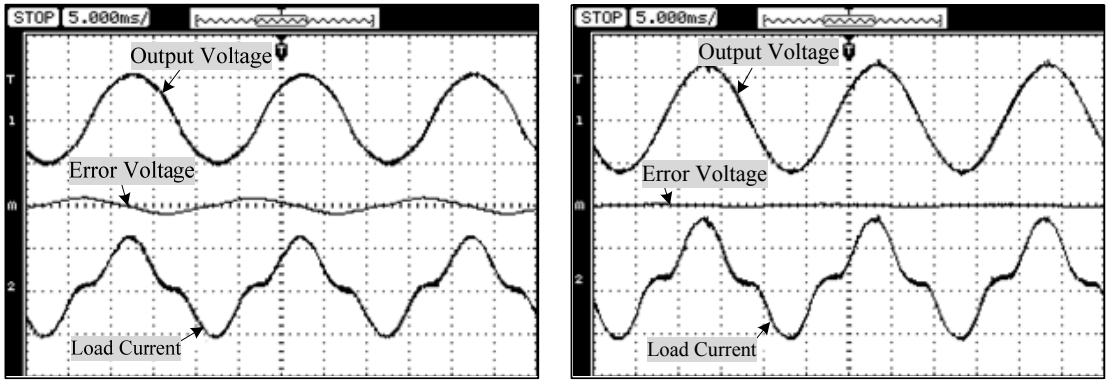
An experimental setup has been built for the validation of theoretical results using HIL control. The complete inverter control system was implemented using a fixed-point 32-bit TMS320F2812 DSP board. ADC sampling frequency has been set equal to the switching frequency 10 kHz. Here again, for comparison purposes, inverter control system with PI and P-type IL alone were also implemented along with the HIL.

Figure 6.15(a) and (b) shows the steady-state experimental results for PI and HIL control on linear load, respectively. The output voltage has a drop due to an inductor current feedback AD with PI controller, similar to the simulated result. In contrast, the voltage error



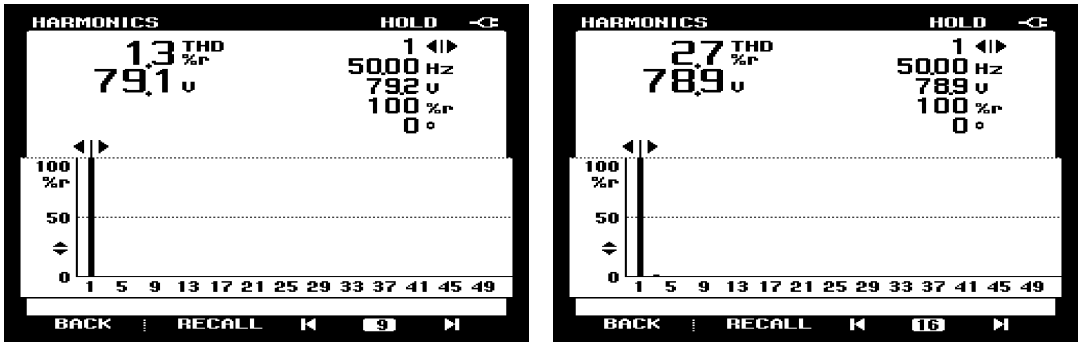
(a) (b)

Figure 6.15 Steady-state experimental waveforms under linear load for (a) PI and (b) HIL control. *CH*-1: Output Voltage (100 V/div), *CH-m*: Tracking Error (10 V/div), and *CH*-2: Load Current (5 A/div).



(a) (b)

Figure 6.16 Steady-state experimental waveforms under non-linear load for (a) PI (b) HIL control. *CH*-1: Output Voltage (100 V/div), *CH-m*:Tracking Error (10 V/div), and *CH*-2: Load Current (5 A/div).



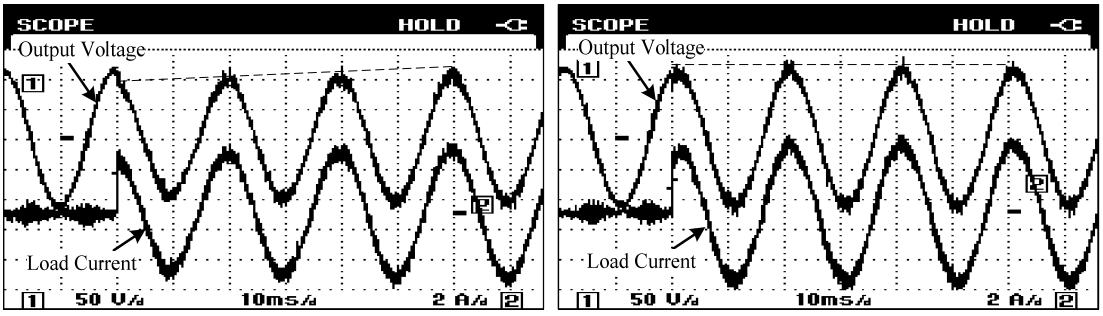
(a) (b)

Figure 6.17 Harmonic spectrum of load voltage using HIL control strategy under rated (a) Resistive load and (b) Rectifier load.

successfully gets eliminated in HIL control with a better tracking. Experimental waveforms for non-linear loading in Figure 6.16 also depict similar trend with a better tracking performance for HIL control. The load current harmonic disturbances were successfully rejected in case of HIL strategy. Corresponding harmonic spectrum plots with HIL control have THD of 1.3 % and 2.7 % under rated linear and non-linear loads, respectively as shown in Figure 6.17.

In another study, a step load application from no load to full load has been considered for both IL and HIL control strategies. The transient response for the HIL in Figure 6.18(b) appears to be faster than the IL control in Figure 6.18(a). The voltage recovery peak is marked in bold dashed line. The system response waveform with IL control takes a few cycles before it settles to specified steady-state value.

Therefore, the presented experimental results for the proposed HIL control clearly



(a) (b)

Figure 6.18 Experimental results on step-load application under rated linear load using (a) IL and (b) HIL control. *CH*-1: output voltage (50 V/div), and *CH*-2: load current (2 A/div).

demonstrate a superior dynamic performance than the PI and IL controls alone.

6.5.3 Simulation Investigations of Multi-Inverter System

The proposed HIL based IACS control scheme has been extensively investigated using MATLAB/Simulink DTF simulations for two inverter modules whose system parameters are enlisted in Table D.1 Appendix D.

The load voltage 'v_o', total load current 'i_o' and output currents 'i_{o1}' and 'i_{o2}' of each inverter are shown in Figure 6.19. The voltage regulation and current sharing performance are satisfactory in both conditions of linear and non-linear loading. The total load current is shared equally between the inverters #1 and #2 and the circulating currents 'i_{cr1}' and 'i_{cr2}' under non-linear load observed to be 0.18 A (RMS), which is same for both inverters in bi-module parallel system. The Load output voltage THD % under linear and non-linear loading have been measured to be 1.1% and 1.5%, respectively.

Transient condition response on step load change for HIL control is shown in Figure 6.20. It can be seen from the load voltage and current waveforms, that the performance of the HIL IACS for multi-inverter is similar to the unit inverter configuration. Waveforms recover quickly from the disruptions and achieve steady state operation well within two fundamental cycles.

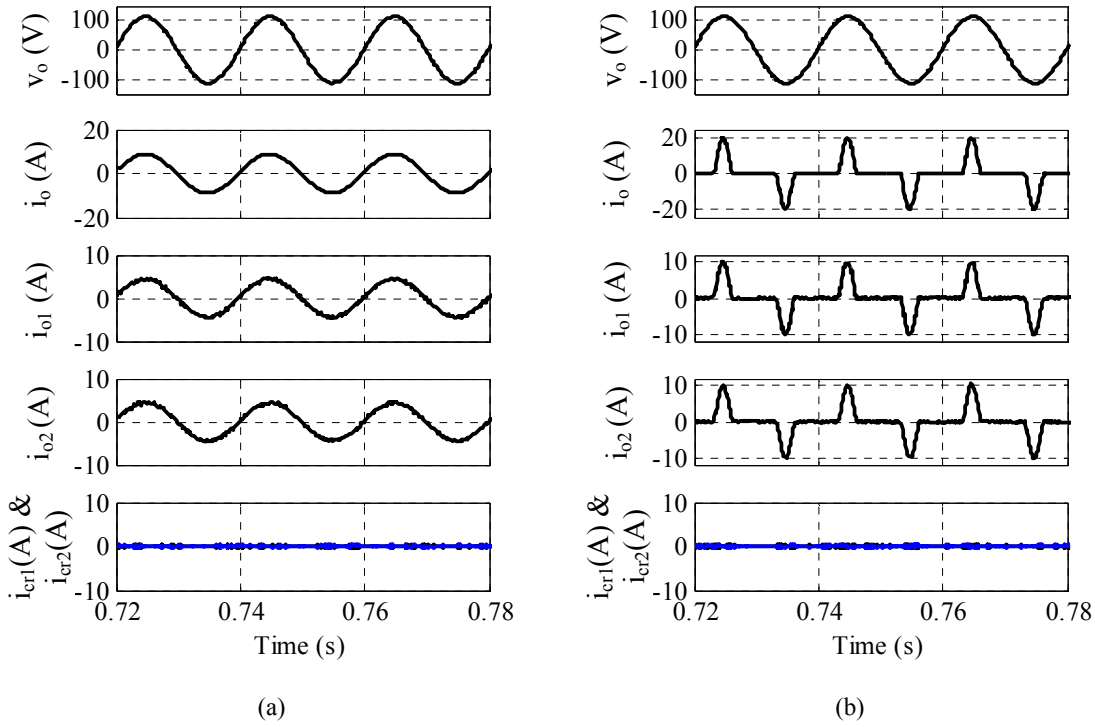


Figure 6.19 Simulated steady-state response under rated (a) Linear and (b) Non-linear load.

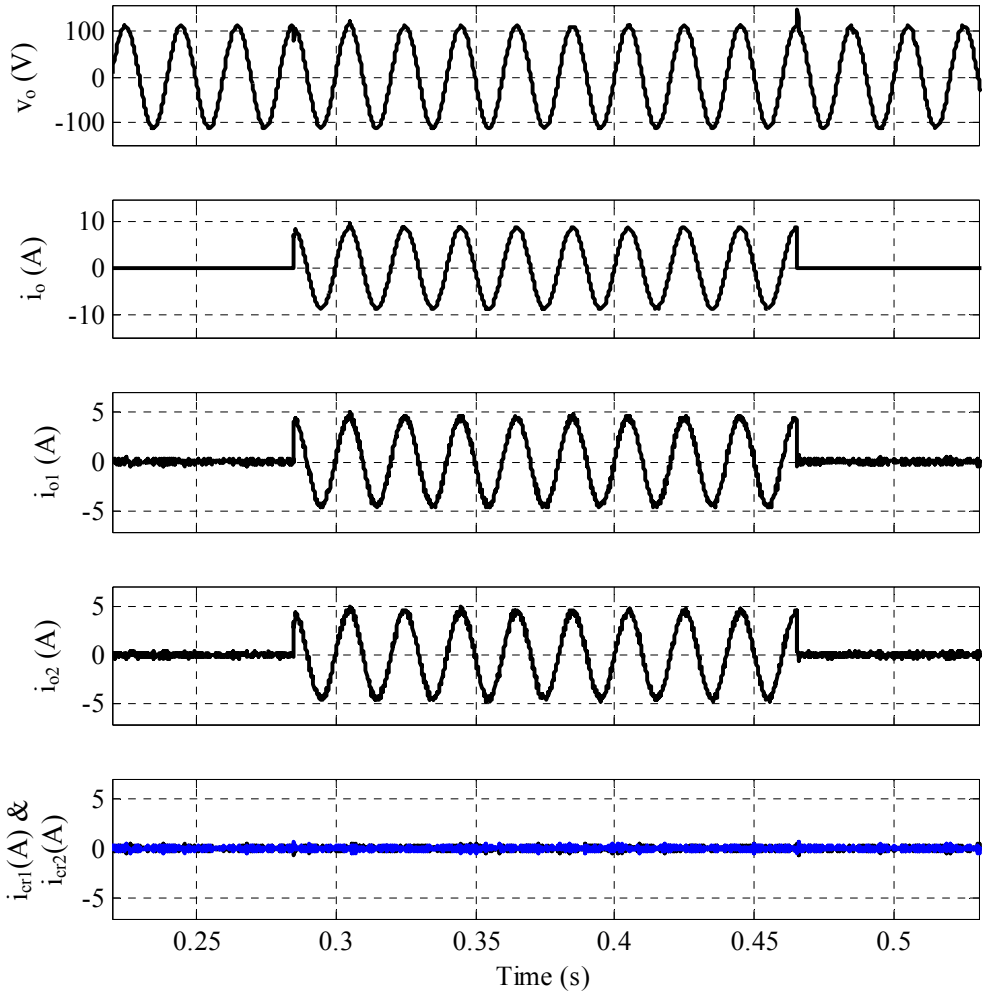


Figure 6.20 Transient response on step-load transition from no-load to rated load.

6.5.4 Effect of Parameters Variation

The effect of parametric and reference voltage variations on the desired voltage waveform and current sharing and hence the controller's potential to tackle such situations has also been investigated. A single parameter under study was varied at a time, keeping other parameters same for a parallel system of bi-module inverter, similar to investigations in chapter 5. The test has been carried out under non-linear loading condition.

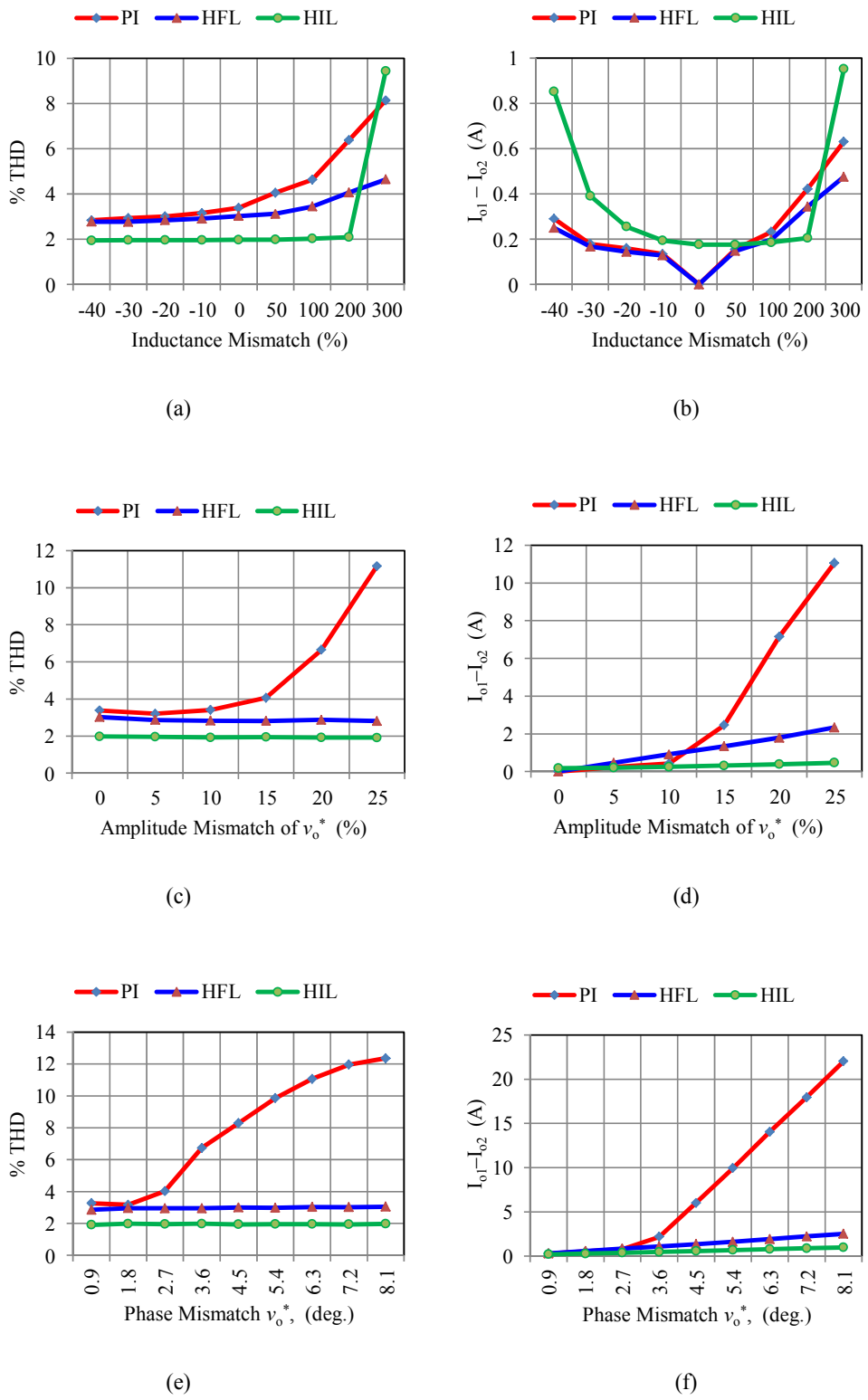


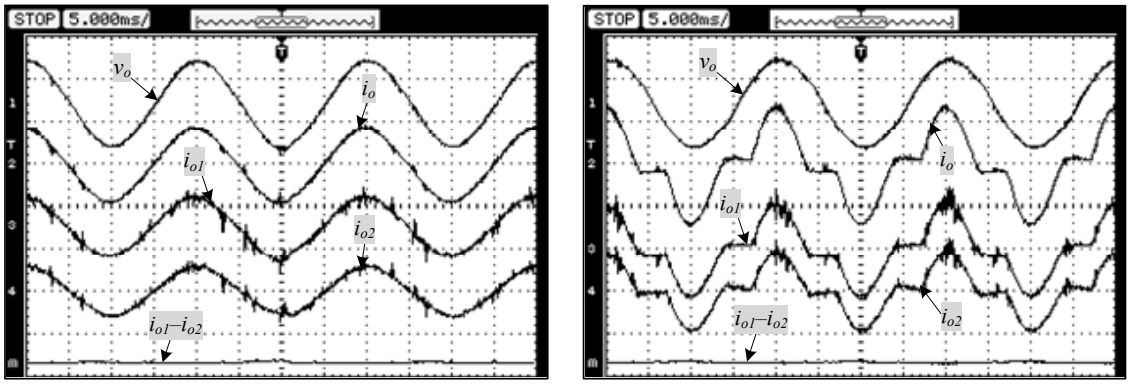
Figure 6.21 Influence of parameter and reference voltage mismatch on % THD of load voltage and current difference (I_{o1}-I_{o2}) (A).

Figure 6.21(a) and (b) show variations in voltage % THD and RMS current difference ($I_{o1}- I_{o2}$) depending on the inductance value mismatch of the filter inductance since circulating current largely depends on inductance. For better comparison, PI and HFL control schemes results are also included in the plot along with the HIL based IACS control. Parameters of inverter #1 has been considered nominal and kept fixed throughout. Whereas, parameters of inverter #2 are retained equal to the inverter #1 except, the filter inductance which has been varied from –40% to 300% of the nominal value. Upto 200% of the nominal range, HIL shows a better robustness on parametric variation and a better performance for the voltage % THD in Figure 6.21(a) and hence regulation. In contrast, current sharing for HIL in Figure 6.21 is not observed to be as good as that of the PI and HFL controls. These can be largely attributed to the learning based HIL in the voltage loop and a simple P control in the current sharing H_c compensator. Also, the voltage % THD and RMS current difference variation are shown in Figure 6.21(c) & (d) for the voltage amplitude deviation of up to 25%. Due to repetitive action, voltage regulation is still better in HIL than HFL and PI over the range. The rise of circulating current or current difference is more moderate in case of HIL than both PI and HFL. HFL is being in-between of both PI and HIL in terms of performance. In a similar manner to voltage amplitude deviation, voltage reference phase between two inverters has been varied up to 8.1 degrees. As shown in Figure 6.21(e) & (f), the voltage regulation and current sharing capability is almost in line with the voltage amplitude deviation, in fact HIL is being the superior one.

6.5.5 Experimental Results of multi-inverter system

Experimental verification of the proposed HIL based IACS control scheme has been carried out for two single-phase inverter modules connected in parallel to a common load. With the same reference voltage for both inverter modules connected in parallel,Figure 6.22 (a) and (b) illustrate the steady state waveforms under linear and non-linear loading conditions, respectively. The load voltage indicated as v_o is observed to be well regulated and properly shared inverter currents waveforms are marked as $i_{o1}$and i_{o2}. The difference between currents i_{o1} and i_{o2}, which is twice of the circulating current for this case, is observed almost to be zero for both linear and non-linear loads respectively.

The transient condition performance has also been tested for step variation of load from no-load to the nominal value. The corresponding waveforms are depicted in Figure 6.23 for linear load. Equal current sharing is achieved almost instantly when an abrupt insertion of load takes place in the bi-modular parallel UPS inverter system. The current difference ($i_{o1}-$



(a) (b)

Figure 6.22 Steady-state response on rated (a) Linear and (b) Non-linear load.

i_{o2}) shows no deviations before and after load change and equal current sharing is achieved even during transient conditions.

Therefore, the proposed HIL based IACS control scheme successfully demonstrates the voltage regulation and the current sharing capability for the multi-inverter system under different loading conditions.

6.6 Summary

This Chapter proposes a novel control strategy named Hybrid Iterative Learning, which comprises of PI and P-type IL control for single-phase UPS inverters system. As the inverter

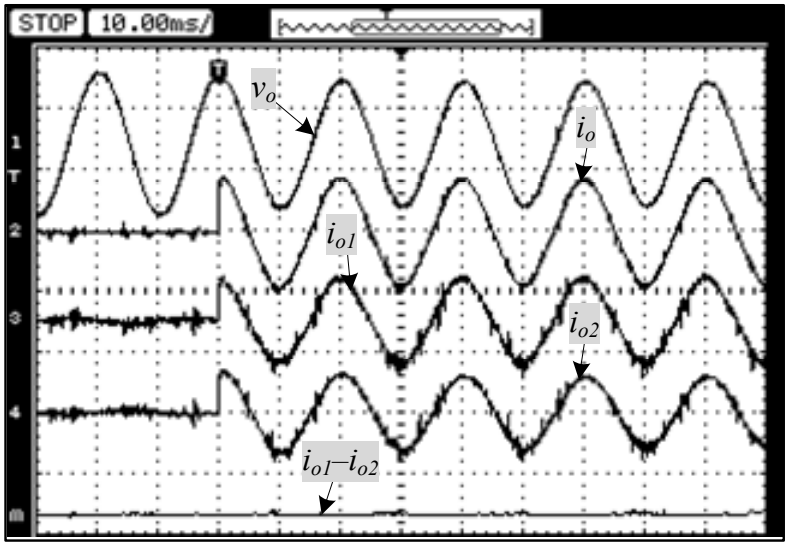


Figure 6.23 Transient response on step-load application from no-load to rated load.

waveforms are periodic in nature, IL based control logic is very much suitable in such conditions. The steady-state error observed on using PI control alone is eradicated by combining it with the IL control. Whereas slow response of the IL control during transients, is eliminated when it is paralleled with PI in the HIL strategy. The PI compensator provides the majority of the control effort during the transient conditions, until it dies out. Further, utilising the advantage of learning algorithm, an inductor current based AD has been employed for the inverter. The effectiveness of the presented HIL control scheme for voltage regulation under both linear and non-linear loads has been successfully demonstrated, despite having relatively higher output impedances in case of inductor current feedback strategy. As the load current is repetitive, due to learning nature of the HIL controller, disturbances die out on subsequent repetitions.

Later, the same HIL control has been further proposed for the multi-inverter UPS system using IACS control scheme, in order to reduce the sensor count of the overall UPS system. The inductor current has been selected as the variable for implementation of current-sharing loop. In this way, with a single measurement of the inductor current, both voltage regulation and current sharing can be achieved. The number of current sensors therefore gets halved for realising average inductor current IACS control when compared to average output current IACS control, which usually also requires either capacitor or inductor current. Since, HIL can achieve a good current sharing performance and an excellent voltage regulation with a single current and single voltage measurement, it gives a distinct advantage to the HIL based IACS control scheme.

The basic philosophy, with a step-by-step design procedure and stability analysis for such a hybrid control scheme has been presented. Simulations and experimentations prove the effectiveness of the proposed HIL control scheme and design, first for the single inverter unit and later for the bi-modular inverter system connected in parallel. The presented control scheme proves to be a cost-effective solution for the multi-inverter UPS systems with reduced sensor count.

CHAPTER 7: MAIN CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

7.1 General

In recent years, uninterruptible power supply (UPS) has gained an immense popularity due to unreliability in grid supply and sensitiveness of electrical and electronic loads. Ever-increasing load demands not only an excellent output voltage performance but also the scalability in terms of power rating. The prime focus of this thesis has been to enhance the power capability of a given UPS inverters system through parallel connection of inverter modules. In the process, in addition to output voltage regulation, total load current should be equally shared among the UPS inverter modules. Therefore, the aim has been to develop a simple and intuitive control algorithm for single-phase UPS inverter system for both unit and multi-modular applications without addition of extra impedance in the power circuit to maintain minimum losses. Further, the control method should preferably require minimum resources such as, in terms of memory requirements, in terms of sensors count, etc. Considering these as the central theme, major objectives of this work have been modeling, analysis, design and implementation of various control strategies of the single-phase UPS inverter system.

Necessary control schemes have been developed in MATLAB/Simulink environment for obtaining simulation results in Discrete Time Frame (DTF). Further, feasibility of the proposed control algorithms has been verified using TMS320F2812 DSP controlled laboratory prototype. Detailed performance results using proposed control schemes during steady state and transient operating modes under linear and non-linear loads has been presented in the preceding chapters. A brief revisit of the main conclusions observed and suggestions for the future work are presented in the following sections.

7.2 Main Conclusions

The presented research work in this thesis mainly deals with the design and analysis of various control strategies, first for a unit inverter and then for multi-module inverters connected in parallel to scale the power rating of the UPS system.

The first chapter of the thesis discussed UPS background, technologies, advantages, development and challenges in the research area. Second chapter briefs the state-of-art single-phase UPS inverter control techniques. Initiating with the control challenges, detailed review

of different control schemes has been carried out. Single-phase UPS inverter close-loop control has various voltage-current feedback options different single or multi-loop control configurations. Further, an employed controller also determines the performance of the inverter output voltage. Thus, a comprehensive study of various compensator and controller has been presented in detail. Later, in second part of the chapter 2, in order to enhance the power capability of the UPS inverter, various available control techniques have been investigated. The paralleling of UPS inverters with a common voltage output is an intuitive solution. However, controlling the parallel UPS system voltage output is not so easy due to the differences in the system parameters of the connected inverters. An inter-modular circulating current starts to flow among inverter modules, which may over load or under load the constituent modules and disrupts the normal operation. In order to share the nominal load currents, specialized current sharing techniques are employed in the inverter control. Mainly, these can be classified into two depending on the communication technique exploited, namely, Droop (wire-less) and Active load current sharing (wired-communication). Active load current sharing having better voltage regulation and current sharing performances has been discussed in some detail and later, Instantaneous Average Current Sharing (IACS), which a type of this method has been opted in the research work. The main contributions and conclusions of the presented work have been summarized as follows.

In the beginning, an exhaustive comparative analysis of various feedback control topologies for single-phase unit UPS inverter has been carried out in chapter 3. Both, single and multi-loop closed-loop control have been assessed in terms of their voltage following and disturbance rejection capability. A series of simulation analysis proves that the multi-loop capacitor current based feedback topologies exhibit better steady state and transient performance. However, to incorporate overload protection functionality, either the inductor or load current is essentially required. Later, a combined reference frame implementation of the voltage-mode control for the single-phase UPS inverter has been developed with an aim to reduce the computational complexity of the synchronous reference frame (SRF). Only, voltage controller has been realised in the SRF while the inner capacitor current active damping loop has been implemented in the stationary frame. Further, derivation of stationary frame equivalent of the aforementioned control strategy significantly simplifies the control design and analysis. The chapter ends showing advantages of the proposed control scheme over the conventional proportional integral (PI) and the proportional resonant (PR) controls through MATLAB simulations and experimental setup.

A novel IACFF based multi-loop control strategy has been presented in chapter 4 for parallel operation of multi-module inverter system. In this scheme, average current of the

entire parallel system has been feed forwarded instead of single module's output current. Therefore, in this way the proposed control scheme has the advantage of equal load current sharing and load current decoupling for high quality voltage regulation, at the same time. The equal current sharing is achieved through the direct regulation of the inner current loop without any additional current sharing loop. Later, a P-controller for the voltage regulation and PR controller for the current control is suggested whose frequency-response analysis shows a better circulating current immunity and robustness. It infers that a compromise exists in the voltage regulation and circulating current reduction. Feasibility of the proposed IACFF control scheme has been finally verified through simulations in MATLAB environment and experimental prototype implementation.

Then, in the process of developing a non-linear controller for the multi-module UPS system, a Hierarchical Fuzzy Logic (HFL) using Instantaneous Average Current Sharing (IACS) control strategy has been proposed in chapter 5. HFL successfully establishes a good voltage regulation and presents a better current sharing capability on the parallel-connected single-phase multi-inverter UPS system. In one hand, it eliminates the design complexity of multiple tuning of conventional PI based controllers, and in the other hand, it also reduces the memory requirements of the conventional Fuzzy Logic (FL) controllers. HFL demonstrates performance equivalence with conventional multivariable FL, despite of having lesser number of rules. Further, analysis shows a better robustness on wider parametric variations for non-linear fuzzy based HFL than conventional PI control. The steady state and transient performances are well regulated for output voltage, under both linear and non-linear loads. An equal current sharing is achieved with minimum circulating current under different operating conditions. Observations are validated through both simulation studies and experimental implementations.

In the last part of the work, a periodic controller based Hybrid Iterative Learning (HIL), which comprises of PI and Iterative Learning (IL) control, has been proposed for the single-phase UPS inverter applications in chapter 6. It employs an inductor current feedback for the active damping of the inverter plant, which has also been utilized for equal current sharing by the HIL based IACS control scheme for multi-inverter UPS system. In this way, number of current sensor has been halved from the conventional load current sensing which usually requires either capacitor or inductor current for good voltage regulation. The steady-state error observed on using PI control alone is eradicated by combining it with the IL control. At the same time, slow response of the IL control during transient condition gets eliminated when combined with the PI in such a hybrid strategy. The basic philosophy, with a step-by-step design procedure and stability analysis for HIL based control scheme has been presented, first

for the single inverter unit and later for the two UPS inverters connected in parallel system. Simulations and experimentations demonstrate the effectiveness of the proposed control scheme and design for both the inverter systems under different loading conditions.

7.3 Suggestions for Further Work

Although objectives set forth at the outset of the investigation have been successfully achieved, certain aspects require further investigation. Some of them have been enlisted as following.

- The present investigation deals with the single-phase UPS inverters system however, the proposed current-sharing schemes may also be equally valid for the three-phase systems. Therefore, investigation of the presented control strategy can be extended for three-phase UPS applications as well.
- In the presented work, only buck-based VSI topology has been investigated for voltage regulation and current sharing control schemes. The control strategies may be verified on other converter topologies also, such as boost or buck-boost based VSIs.
- Investigations of the presented current sharing control schemes may be explored for the grid-connected mode of the UPS inverters system.
- The I-M circulating current in multi-inverter system has been derived assuming negligible line impedance. Further, connected AC load has been assumed to be concentrated. Therefore, a research study may also be done taking into the account the line impedances and distributed load conditions as well.
- The proposed control strategies particularly, HFL and HIL control may also be analysed for other current sharing control techniques (Droop Control, Master Slave Control, etc.).
- The HIL based control scheme may be used for other applications as well, such as, rectifiers and active filters, which are basically a system that tracks a periodic reference. The only difference lies in their plant characteristics yielding distinct operating and stability conditions, which ultimately modifies the control design.
- Iterative Learning control may be investigated in combination with other non-linear control techniques, such as, sliding mode control to improve the inverter's robustness and dynamic performance.

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APPENDIX-A: STATIONARY FRAME EQUIVALENT OF SRF-PI

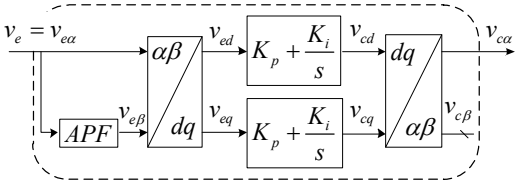

Figure A.1 Block schematic representation of SRF-PI voltage controller in α-β stationary frame.

Figure A.1 demonstrate the stationary frame representation of the SRF-PI controller. Voltage error, v_e has been processed first through an APF block to obtain the β-axis signal. Next, the stationary frame α-β AC signals have been then transformed to d-q frame $v_{e(d\text{-}q)}$ using Park's transformation (α-$\beta \rightarrow d$-q) matrix.

$$\begin{bmatrix} v_{ed}(t) \\ v_{eq}(t) \end{bmatrix} = \underset{(dq \leftarrow \alpha\beta)}{\begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix}} \begin{bmatrix} v_{e\alpha}(t) \\ v_{e\beta}(t) \end{bmatrix} \tag{A.1}$$

According to Euler's formula,

$$\cos\omega t = \frac{e^{\hat{i}\omega t} + e^{-\hat{i}\omega t}}{2} \text{ and } \sin\omega t = \frac{e^{\hat{i}\omega t} - e^{-\hat{i}\omega t}}{2\hat{i}} \tag{A.2}$$

Substituting (A.2) to (A.1) yields,

$$\begin{bmatrix} v_{ed}(t) \\ v_{eq}(t) \end{bmatrix} = \frac{1}{2}\begin{bmatrix} e^{\hat{i}\omega t} + e^{-\hat{i}\omega t} & \hat{i}\left(e^{-\hat{i}\omega t} - e^{\hat{i}\omega t}\right) \\ \hat{i}\left(e^{\hat{i}\omega t} - e^{-\hat{i}\omega t}\right) & e^{\hat{i}\omega t} + e^{-\hat{i}\omega t} \end{bmatrix} \begin{bmatrix} v_{e\alpha}(t) \\ v_{e\beta}(t) \end{bmatrix} \tag{A.3}$$

Applying Laplace transform on both sides and using frequency shift property i.e., $\mathcal{L}\{e^{at}f(t)\}=F(s-a)$, it can be obtained

$$\begin{bmatrix} v_{ed}(s) \\ v_{eq}(s) \end{bmatrix} = \frac{1}{2}\begin{bmatrix} v_{e\alpha}\left(s-\hat{i}\omega\right) + v_{e\alpha}\left(s+\hat{i}\omega\right) + \hat{i}v_{e\beta}\left(s+\hat{i}\omega\right) - \hat{i}v_{e\beta}\left(s-\hat{i}\omega\right) \\ \hat{i}v_{e\alpha}\left(s-\hat{i}\omega\right) - \hat{i}v_{e\alpha}\left(s+\hat{i}\omega\right) + v_{e\beta}\left(s-\hat{i}\omega\right) + v_{e\beta}\left(s+\hat{i}\omega\right) \end{bmatrix} \tag{A.4}$$

Since signals become DC value in d-q frame, voltage errors may be regulated by conventional PI controller $G_{PI}(s)$ to achieve zero steady-state error. Therefore,

$$\begin{bmatrix} v_{cd}(s) \\ v_{cq}(s) \end{bmatrix} = \begin{bmatrix} G_{PI}(s) & 0 \\ 0 & G_{PI}(s) \end{bmatrix} \begin{bmatrix} v_{ed}(s) \\ v_{eq}(s) \end{bmatrix} \tag{A.5}$$

On substituting (A.4) in (A.5) gives,

$$\begin{bmatrix} v_{cd}(s) \\ v_{cq}(s) \end{bmatrix} = \frac{1}{2} \begin{bmatrix} G_{PI}(s)\left\{ v_{e\alpha}\left(s-\hat{i}\omega\right) + v_{e\alpha}\left(s+\hat{i}\omega\right) + \hat{i}v_{e\beta}\left(s+\hat{i}\omega\right) - \hat{i}v_{e\beta}\left(s-\hat{i}\omega\right) \right\} \\ G_{PI}(s)\left\{ \hat{i}v_{e\alpha}\left(s-\hat{i}\omega\right) - \hat{i}v_{e\alpha}\left(s+\hat{i}\omega\right) + v_{e\beta}\left(s-\hat{i}\omega\right) + v_{e\beta}\left(s+\hat{i}\omega\right) \right\} \end{bmatrix} \tag{A.6}$$

Again, the α-β stationary frame compensated voltage signals are obtained by applying inverse Park's transformation (d-$q \rightarrow \alpha$-β) to the compensated output of the d-q frame PI controllers.

$$\begin{bmatrix} v_{c\alpha}(t) \\ v_{c\beta}(t) \end{bmatrix} = \underset{(\alpha\beta \leftarrow dq)}{\begin{bmatrix} \cos\omega t & -\sin\omega t \\ \sin\omega t & \cos\omega t \end{bmatrix}} \begin{bmatrix} v_{cd}(t) \\ v_{cq}(t) \end{bmatrix} \tag{A.7}$$

Applying Laplace transform on both sides, it can be obtained

$$\begin{bmatrix} v_{c\alpha}(s) \\ v_{c\beta}(s) \end{bmatrix} = \frac{1}{2} \begin{bmatrix} v_{cd}\left(s-\hat{i}\omega\right) + v_{cd}\left(s+\hat{i}\omega\right) + \hat{i}v_{cq}\left(s-\hat{i}\omega\right) - \hat{i}v_{cq}\left(s+\hat{i}\omega\right) \\ \hat{i}v_{cd}\left(s+\hat{i}\omega\right) - \hat{i}v_{cd}\left(s-\hat{i}\omega\right) + v_{cq}\left(s-\hat{i}\omega\right) + v_{cq}\left(s+\hat{i}\omega\right) \end{bmatrix} \tag{A.8}$$

On substitution of v_{cd} and v_{cq} from (A.6) in $v_{c\alpha}$ and $v_{c\beta}$, respectively of (A.7) returns

$$\begin{bmatrix} v_{c\alpha}(s) \\ v_{c\beta}(s) \end{bmatrix} = \frac{1}{4} \begin{bmatrix} G_{PI}\left(s-\hat{i}\omega\right)\left\{ v_{e\alpha}\left(s-2\hat{i}\omega\right) + v_{e\alpha}(s) + \hat{i}v_{e\beta}(s) - \hat{i}v_{e\beta}\left(s-2\hat{i}\omega\right) \right\} \\ +G_{PI}\left(s+\hat{i}\omega\right)\left\{ v_{e\alpha}(s) + v_{e\alpha}\left(s+2\hat{i}\omega\right) + jv_{e\beta}\left(s+2\hat{i}\omega\right) - \hat{i}v_{e\beta}(s) \right\} \\ +\hat{i}G_{PI}\left(s-\hat{i}\omega\right)\left\{ \hat{i}v_{e\alpha}\left(s-2\hat{i}\omega\right) - \hat{i}v_{e\alpha}(s) + v_{e\beta}\left(s-2\hat{i}\omega\right) + v_{e\beta}(s) \right\} \\ -\hat{i}G_{PI}\left(s+\hat{i}\omega\right)\left\{ \hat{i}v_{e\alpha}(s) - \hat{i}v_{e\alpha}\left(s+2\hat{i}\omega\right) + v_{e\beta}(s) + v_{e\beta}\left(s+2\hat{i}\omega\right) \right\} \\ \\ \hat{i}G_{PI}\left(s+\hat{i}\omega\right)\left\{ v_{e\alpha}(s) + v_{e\alpha}\left(s+2\hat{i}\omega\right) + \hat{i}v_{e\beta}\left(s+2\hat{i}\omega\right) - \hat{i}v_{e\beta}(s) \right\} \\ -\hat{i}G_{PI}\left(s-\hat{i}\omega\right)\left\{ v_{e\alpha}\left(s-2\hat{i}\omega\right) + v_{e\alpha}(s) + \hat{i}v_{e\beta}(s) - \hat{i}v_{e\beta}\left(s-2\hat{i}\omega\right) \right\} \\ +G_{PI}\left(s-\hat{i}\omega\right)\left\{ \hat{i}v_{e\alpha}\left(s-2\hat{i}\omega\right) - \hat{i}v_{e\alpha}(s) + v_{e\beta}\left(s-2\hat{i}\omega\right) + v_{e\beta}(s) \right\} \\ +G_{PI}\left(s+\hat{i}\omega\right)\left\{ \hat{i}v_{e\alpha}(s) - \hat{i}v_{e\alpha}\left(s+2\hat{i}\omega\right) + v_{e\beta}(s) + v_{e\beta}\left(s+2\hat{i}\omega\right) \right\} \end{bmatrix} \tag{A.9}$$

Rearrangement of terms in (A.9) yields,

$$\begin{bmatrix} v_{c\alpha}(s) \\ v_{c\beta}(s) \end{bmatrix} = \frac{1}{2}\begin{bmatrix} G_{PI}\left(s-\hat{i}\omega\right)\left\{v_{e\alpha}(s)+\hat{i}v_{e\beta}(s)\right\}+G_{PI}\left(s+\hat{i}\omega\right)\left\{v_{e\alpha}(s)-\hat{i}v_{e\beta}(s)\right\} \\ \hat{i}G_{PI}\left(s+\hat{i}\omega\right)\left\{v_{e\alpha}(s)-\hat{i}v_{e\beta}(s)\right\}-\hat{i}G_{PI}\left(s-\hat{i}\omega\right)\left\{v_{e\alpha}(s)+\hat{i}v_{e\beta}(s)\right\} \end{bmatrix}$$
$$= \frac{1}{2}\begin{bmatrix} \left\{G_{PI}\left(s-\hat{i}\omega\right)+G_{PI}\left(s+\hat{i}\omega\right)\right\}v_{e\alpha}(s)+\hat{i}\left\{G_{PI}\left(s-\hat{i}\omega\right)-G_{PI}\left(s+\hat{i}\omega\right)\right\}v_{e\beta}(s) \\ \hat{i}\left\{G_{PI}\left(s+\hat{i}\omega\right)-G_{PI}\left(s-\hat{i}\omega\right)\right\}v_{e\alpha}(s)+\left\{G_{PI}\left(s+\hat{i}\omega\right)+G_{PI}\left(s-\hat{i}\omega\right)\right\}v_{e\beta}(s) \end{bmatrix} \quad \text{(A.10)}$$

The matrix form of the (A.10) is given as in (A.11),

$$\begin{bmatrix} v_{c\alpha}(s) \\ v_{c\beta}(s) \end{bmatrix} = \frac{1}{2}\begin{bmatrix} G_{PI}\left(s-\hat{i}\omega\right)+G_{PI}\left(s+\hat{i}\omega\right) & \hat{i}G_{PI}\left(s-\hat{i}\omega\right)-\hat{i}G_{PI}\left(s+\hat{i}\omega\right) \\ \hat{i}G_{PI}\left(s+\hat{i}\omega\right)-\hat{i}G_{PI}\left(s-\hat{i}\omega\right) & G_{PI}\left(s+\hat{i}\omega\right)+G_{PI}\left(s-\hat{i}\omega\right) \end{bmatrix}\begin{bmatrix} v_{e\alpha}(s) \\ v_{e\beta}(s) \end{bmatrix} \quad \text{(A.11)}$$

Using $G_{PI}(s) = K_p + K_i/s$ in (A.11) and performing mathematical simplification,

$$\begin{bmatrix} v_{c\alpha}(s) \\ v_{c\beta}(s) \end{bmatrix} = \begin{bmatrix} K_p + K_i\left(\frac{s}{s^2+\omega^2}\right) & -K_i\frac{\omega}{s^2+\omega^2} \\ K_i\frac{\omega}{s^2+\omega^2} & K_p + K_i\left(\frac{s}{s^2+\omega^2}\right) \end{bmatrix}\begin{bmatrix} v_{e\alpha}(s) \\ v_{e\beta}(s) \end{bmatrix} \quad \text{(A.12)}$$

Only α–axis signal is the real quantity of the pseudo two-phase system which can be obtained in (A.13) from (A.12), using $v_{e\beta}(s) = \frac{\omega - s}{\omega + s}v_{e\alpha}(s)$ as displayed in Figure A.1.

$$\begin{aligned} v_{c\alpha}(s) &= \left[K_p + K_i\left\{\left(\frac{s}{s^2+\omega^2}\right) - \frac{\omega}{s^2+\omega^2}\left(\frac{\omega-s}{\omega+s}\right)\right\}\right]v_{e\alpha}(s) \\ &= \left[K_p + K_i\left\{\frac{s^2+2s\omega-\omega^2}{s^3+s^2\omega+s\omega^2+\omega^3}\right\}\right]v_{e\alpha}(s) \end{aligned} \quad \text{(A.13)}$$

Rearrangement of (A.13), gives the stationary frame equivalent of the SRF-PI voltage controller transfer function, $G_{SRF}(s)$ as

$$G_{SRF}(s) = \frac{v_{c\alpha}(s)}{v_{e\alpha}(s)} = K_p + K_i\left\{\frac{s^2+2s\omega-\omega^2}{s^3+s^2\omega+s\omega^2+\omega^3}\right\} \quad \text{(A.14)}$$

APPENDIX-B: DERIVATION FOR INTEGRAL GAINS

B.1 PI Control

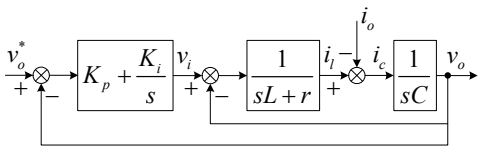

Figure B.1 Block schematic representation of inverter control using PI.

The voltage-gain transfer function of closed-loop inverter control using PI compensator may be obtained from Figure B.1 as

$$G_{cl}^{PI} = \left.\frac{v_o(s)}{v_o^*(s)}\right|_{i_o=0} = \frac{sK_p + K_i}{s^3LC + s^2CK_c + sK_p + K_i} \tag{B.1}$$

The characteristic polynomial for the closed-loop system can be written from (B.1) as

$$s^3LC + s^2CK_c + sK_p + K_i = 0 \tag{B.2}$$

Rouths's array of the (B.2) is given as in Table B.1 ,

Table B.1 Rouths's array for closed-loop inverter control using PI compensator

s^3	LC	K_p
s^2	CK_c	K_i
s^1	$(K_cK_p - LK_i)/K_c$	0
s^0	K_i	0

For the system to be stable, all coefficients of the first column of the Rouths's tabulation must have the same sign, which leads to the following condition for the integral gain:

$$K_i < \frac{K_cK_p}{L} \tag{B.3}$$

B.2 PR Control

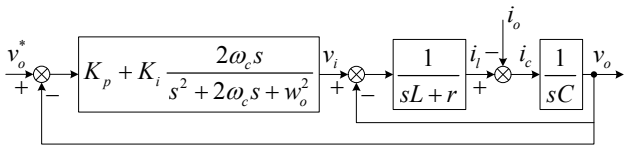

Figure B.2 Block schematic representation of inverter control using practical PR.

The voltage-gain transfer function of closed-loop inverter control with PR compensator can be written from Figure B.2,

$$G_{cl}^{PR} = \left.\frac{v_o(s)}{v_o^*(s)}\right|_{i_o=0} = \frac{s^2 K_p + 2\omega_c\left(K_p + K_i\right)s + K_p\omega_o^2}{\begin{aligned} s^4 LC + s^3\left(CK_c + 2\omega_c LC\right) + s^2\left(2\omega_c CK_c + \omega_o^2 LC + K_p\right) \\ + s\left(\omega_o^2 CK_c + 2\omega_c K_p + 2\omega_c K_i\right) + \omega_o^2 K_p \end{aligned}} \quad \text{(B.4)}$$

The characteristic polynomial can be obtained from (B.4) as,

$$\begin{aligned} s^4 LC + s^3\left(CK_c + 2\omega_c LC\right) + s^2\left(2\omega_c CK_c + \omega_o^2 LC + K_p\right) \\ + s\left(\omega_o^2 CK_c + 2\omega_c K_p + 2\omega_c K_i\right) + \omega_o^2 K_p = 0 \end{aligned} \quad \text{(B.5)}$$

Routhsʼs tabulation of the (B.5) is as obtained in Table B.2,

Table B.2 Routhsʼs array for closed-loop inverter control using PR compensator

s^4	LC	$2\omega_c CK_c + \omega^2 LC + K_p = a_1$	$\omega^2 K_p$
s^3	$CK_c + 2\omega_c LC = a_2$	$\omega^2 CK_c + 2\omega_c K_p + 2\omega_c K_i = a_3$	0
s^2	$(a_1 a_2 - a_3 LC)/a_2 = a_4$	$\omega^2 K_p$	0
s^1	$(a_3 a_4 - a_2 \omega^2 K_p)/a_4$	0	0
s^0	$\omega^2 K_p$	0	0

Applying the RH stability criterion, yields the system stability discriminant as

$$\begin{cases} \left(a_1 a_2 - a_3 LC\right) > 0 \\ \left(K_c + 2\omega_c L\right)\left(2\omega_c CK_c + \omega^2 LC + K_p\right) - \left(\omega_o^2 CK_c + 2\omega_c K_p + 2\omega_c K_i\right)L > 0 \end{cases} \quad \text{(B.6)}$$

The upper bound of the integral gain for PR gain is:

$$K_i < \frac{K_c K_p + 2\omega_c C\left(2\omega_c L K_c + K_c{}^2 + \omega^2 L^2\right)}{2\omega_c L} \simeq \frac{K_c K_p}{2\omega_c L}\left(\text{approx.}\right) \tag{B.7}$$

B.3 SRF-PI Control

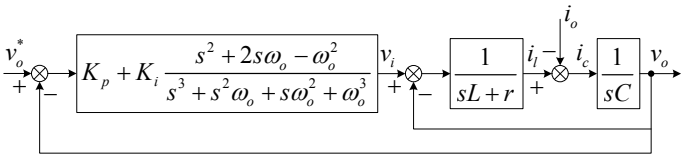

Figure B.3 Block schematic representation of inverter control using Staionary frame equivalent SRF-PI.

The voltage-gain transfer function of closed-loop inverter control with SRF-PI compensator can be derived from Figure B.3,

$$G_{cl}^{SRF} = \left.\frac{v_o(s)}{v_o^*(s)}\right|_{i_o=0} = \frac{s^3 K_p + s^2\left(\omega_o K_p + K_i\right) + s\left(\omega_o^2 K_p + 2\omega_o K_i\right) + \omega_o^3 K_p - \omega_o^2 K_i}{\begin{aligned} &s^5 LC + s^4\left(CK_c + \omega_o LC\right) + s^3\left(\omega_o CK_c + \omega_o^2 LC + K_p\right) \\ &+ s^2\left(\omega_o^2 CK_c + \omega_o^3 LC + \omega_o K_p + K_i\right) \\ &+ s\left(\omega_o^3 CK_c + \omega_o^2 K_p + 2\omega_o K_i\right) + \omega_o^3 K_p - \omega_o^2 K_i \end{aligned}} \tag{B.8}$$

The characteristic polynomial can be obtained from (B.8) as

$$\begin{aligned} &s^5 LC + s^4\left(CK_c + \omega_o LC\right) + s^3\left(\omega_o CK_c + \omega_o^2 LC + K_p\right) \\ &+ s^2\left(\omega_o^2 CK_c + \omega_o^3 LC + \omega_o K_p + K_i\right) + s\left(\omega_o^3 CK_c + \omega_o^2 K_p + 2\omega_o K_i\right) + \omega_o^3 K_p - \omega_o^2 K_i = 0 \end{aligned} \tag{B.9}$$

Rouths's tabulation of the (B.5) in Table B.3 is,

Table B.3 Rouths's array for closed-loop inverter control using SRF-PI compensator

s^5	LC	$\omega CK_c+\omega^2 LC+K_p = b_1$	$\omega^3 CK_c+\omega^2 K_p+2\omega K_i = b_2$
s^4	$CK_c+\omega LC = b_3$	$\omega^2 CK_c+\omega^3 LC+\omega K_p+K_i = b_4$	$\omega^3 K_p - \omega^2 K_i = b_5$
s^3	$(b_1 b_3 - b_4 LC)/b_3 = b_6$	$(b_3 b_2 - \tau LC)/b_3 = b_7$	0
s^2	$(b_6 b_4 - b_3 b_7)/b_6 = b_8$	b_5	0
s^1	$(b_7 b_8 - b_5 b_6)/b_8$	0	0
s^0	b_5	0	0

Applying RH stability criterion leads to the following condition for K_i:

$$K_i < \omega_o K_p \tag{B.10}$$

C.1 Test Rig Structure

Details of the experimental set-up is illustrated in this appendix. The photograph of the test rig is shown in Figure C.1. Important constituents such as Inverter module, TMS320F2812 based DSP trainer kit, voltage and current measuring sensors and load are labelled.

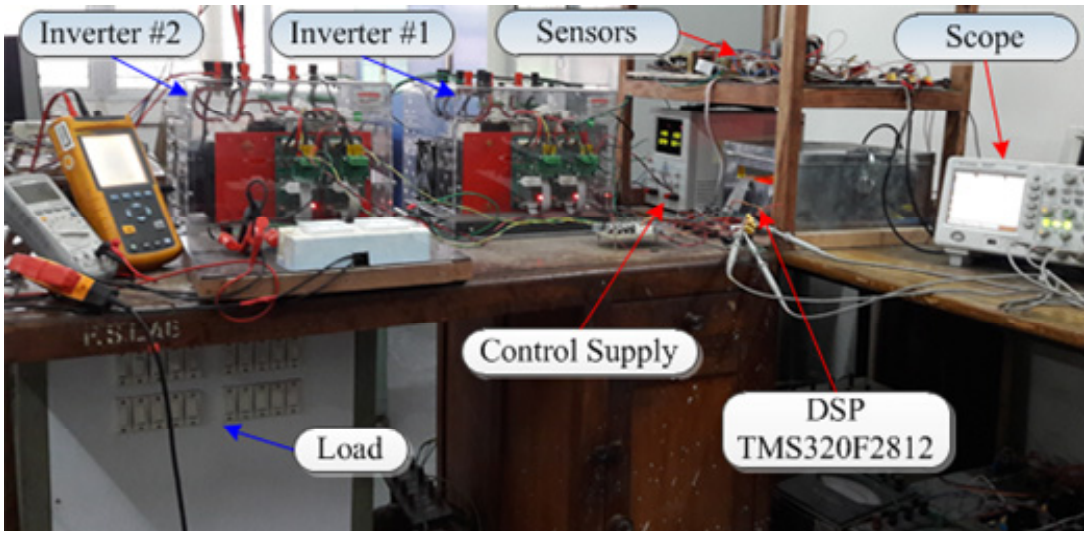

Figure C.1 Photograph of the experimental set-up.

The entire control scheme has been realized on a 32-bit fixed point TMS320F2812 DSP from Texas Instruments. The control architecture of the experimental implementations has been demonstrated in Figure C.2. There are two methods to develop real-time control programs for the TMS320F2812 DSP. One is to use MATLAB/Simulink Embedded Target for Texas Instruments C2000 and another is to code manual in assembly or 'C' language. By using Embedded Target, the simulation model in Simulink can automatically be converted into 'C' language code. Then, the Code Composer Studio (CCS) v3.3 software by Texas Instruments loads the control program into the DSP via its standard parallel port using a JTAG-interface. Since, Simulink Embedded Target offers a simple and faster alternative of implementation programming, it has been used in the present investigation.

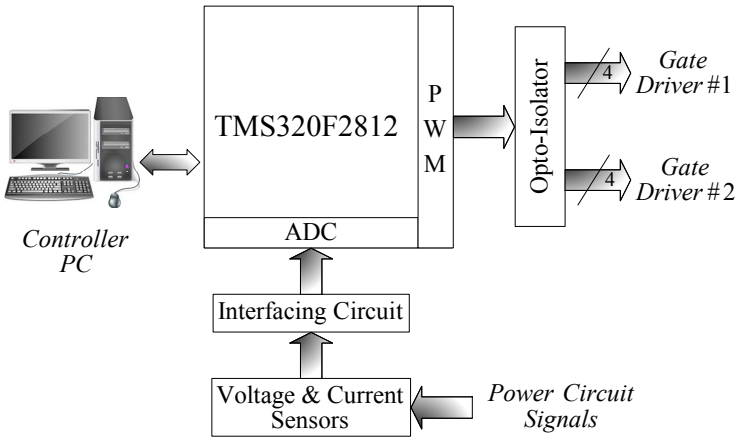

Figure C.2 Contol architecture of the TMS320F2812 DSP based hardware implementation.

C.2 Digital Signal Processor (DSP) Board

The core of the hardware implementation of the UPS inverter system is the DSP. The DSP board generates the PWM signals for inverters processing measured feedback signals according to the employed control algorithm. The measured analog voltage and current feedback signals are digitised through the ADC conversion. The Texas Instruments TMS320F2812 DSP is used in the investigation whose photograph is displayed in Figure C.3. It is an advanced fixed-point processor of the C2000 family series. Important features of the DSP trainer's kit are following:

- High-Performance 32-Bit CPU
- 150 MHz (6.67-ns Cycle Time)
- JTAG-interface with host computer
- On-Chip Memory
  - ✓ Flash Devices: Up to 128K x 16 Flash
  - ✓ ROM Devices: Up to 128K x 16 ROM
- 12-Bit ADC, 16 Channels
  - ✓ 2 x 8 Channel Input Multiplexer
  - ✓ Single/Simultaneous Conversions
  - ✓ Fast Conversion Rate: 80 ns/12.5 MSPS
- Up to 56 General-Purpose I/O (GPIO) Pins
- 12 PWM signal with six of them as independent pairs with programmable dead-bands

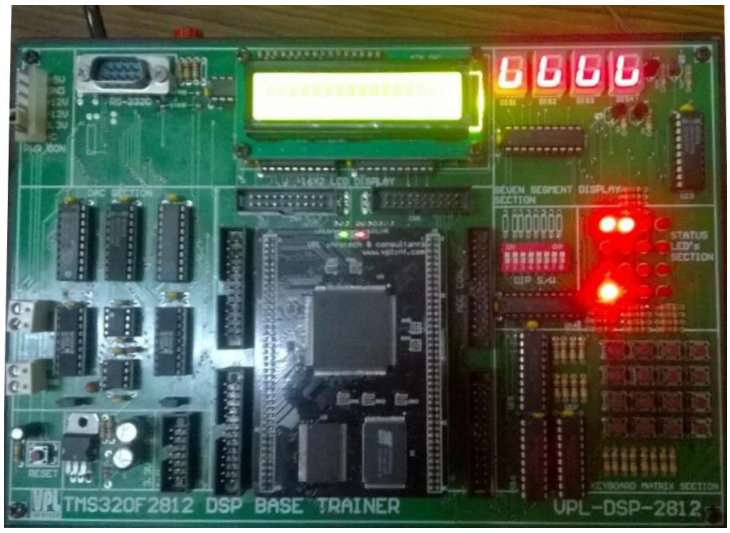

Figure C.3 TMS320F2812 DSP trainer kit.

- Development Tools: Code Composer Studio (CCS) v3.3, MATLAB/Simulink

C.3 Voltage and Current Sensing Circuit

For high performance close-loop operation, voltage and current feedback signals are required for the controllers. The photograph of sensing circuits is shown in Figure C.4. This also contains the ±12 V and 5 V power supply circuit.

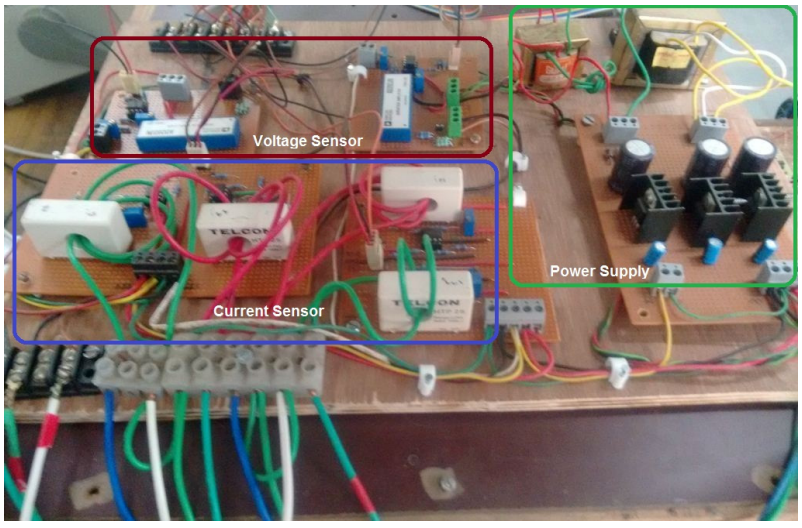

Figure C.4 Photograph of voltage and current sensing circuit.

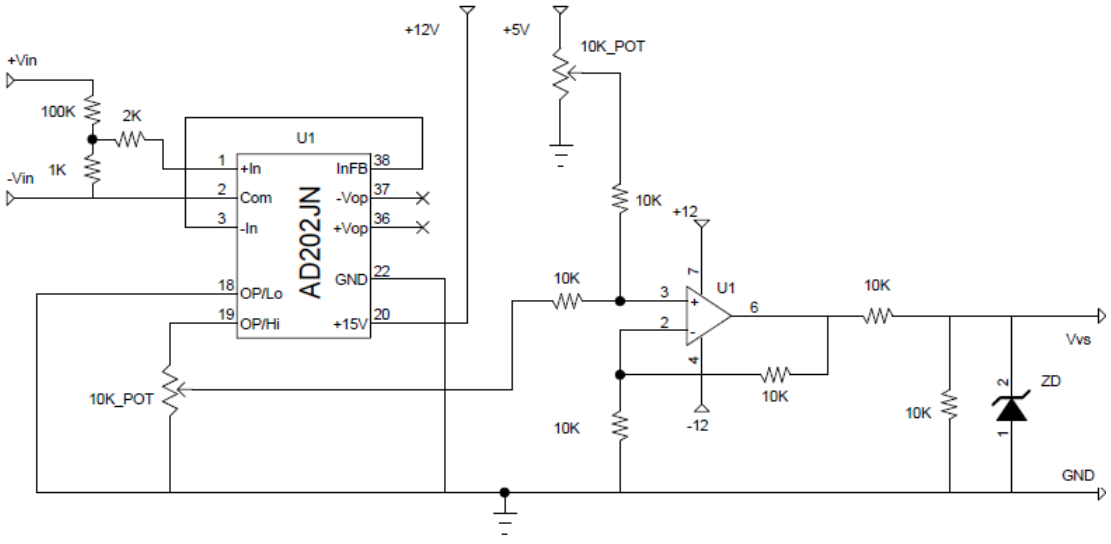

Figure C.5 Schematic circuit diagram of voltage sensor.

C.3.1 Voltage Sensing Circuit

Analog Devices AD202, a low cost miniature isolation amplifier is used in the voltage sensing circuit. It is a general purpose transformer-coupled amplifier to measure input signals and transmit without any galvanic connection between the primary (high voltage) and the secondary circuit (electronic circuit). The sensed signals were bi-polar voltages in the range of ±5 V. These signals are converted to uni-polar 0–3 V level using an Op-amp based conditioning and interface circuit, before feeding to the 12-bit ADC channels of the DSP. In order to get an appropriate voltage to feed the DSP, the signal conditioning circuit is incorporated in the circuit schematic of voltage sensor in Figure C.5.

C.3.2 Current Sensing Circuit

Current feedbacks were obtained using TELCON-HTP25 PCB mounted Hall-effect current sensors. The primary current range is 25 A with a transformation ratio of 1000:1. Like the voltage sensor circuit, the signal conditioning circuit is again integrated to ensure correct voltage at the DSP channel. The circuit schematic of the implemented current sensor is demonstrated in Figure C.6.

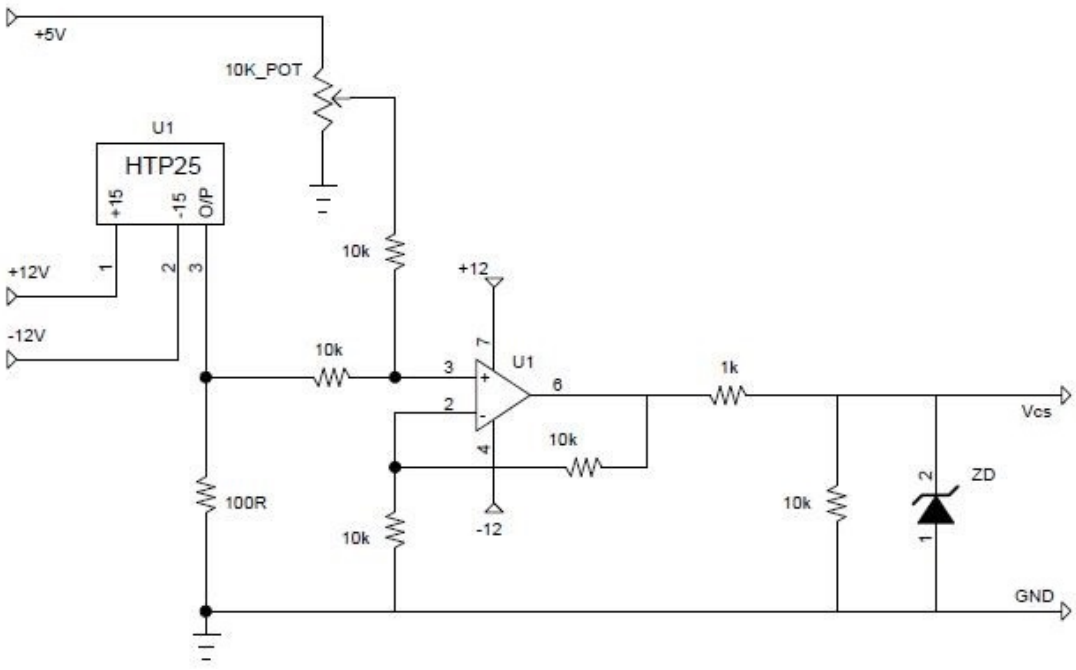

Figure C.6 Schematic circuit diagram of current sensor.

C.4 Isolation and Amplification Circuit for PWM Signals

The photograph and circuit schematic of an optical-isolator to galvanically separate the low voltage DSP controller from the high voltage power circuit have been shown in Figure C.7 and Figure C.8. The PWM pulses generated by the DSP TMS320F2812, which are in order of 3.3 V (V_{DSP}), are connected to input of the Opto-isolator 6N136. The output of the opto-

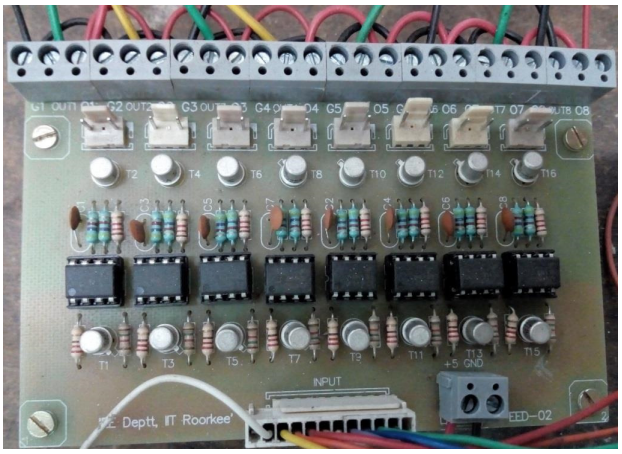

Figure C.7 Photograph of the optical isolator.

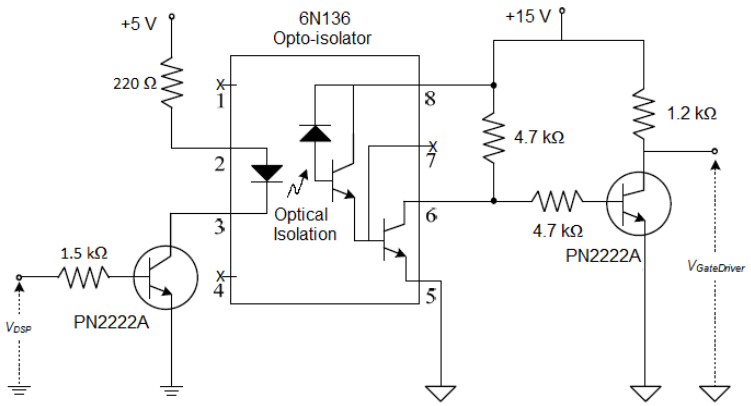

Figure C.8 Schematic circuit diagram of an optical isolator.

coupler, which has been amplified to 15 V with an isolated ground, is directly connected to the IGBT switches via driver circuit. Two PN2222A general-purpose transistors connected at the input and output ends to avoid DSP loading and to act as buffer amplifier, respectively.

APPENDIX-D: KEY PARAMETERS

Table D.1 Parameters for inverter modules

Parameter	***Inverter #1***	***Inverter #2***
Filter Inductances, *L*	1.0 mH	1.5 mH
ESR, r	0.5 Ω	0.7 Ω
Filter Capacitance, *C*	18.0 μF	18.0 μF

Table D.2 Load parameters

***Load*:**	***Linear***	***Non-Linear***		
	***R*(Ω)**	***R_s*(Ω)**	***C*(μF)**	***R*(Ω)**
Values	25.60	1.02	2298.22	57.53

Table D.3 Control parameter used in chapter 3

Controller	***Control Parameter***		
	K_p	***K_i***	***K_c***
PI	0.8	4000	10
PR	0.8	200	10
SRF-PI	0.8	100	10

Table D.4 Controller parameters used for Figure 4.3 in chapter 4

	***Voltage Controller* (G_v: PR)**		***Current Controller* (G_c: P)**	***Damping Coefficient***
	K_p	***K_i***	***K_{cp}***	***K_c / K_l***
SLVM	0.80	20	–	–
VMC	0.80	200	–	10
VMI	0.80	200	–	10
CMC	0.08	20	10	–
CMI	0.08	20	10	–
CMIL	0.08	20	10	–

Table D.5 Control parameter used in chapter 4

Controller	***Control Parameter***			
	Voltage Controller (G_v)		***Current Controller(G_c)***	
	K_{vp}	***K_{vi}***	***K_{cp}***	***K_{ci}***
P-PR	0.15	–	10	400
PR-PR	0.15	20	10	400

Table D.6 Control parameters used in chapter 6

Parameter	***Value***
Proportional gain, K_p	0.8
Integral gain, Ki	4000
Active Damping Coefficient, K_l	10
Learning gain, K	1.05
Advancement unit, z^a	z^2
Current Sharing compensator, H_c	2

APPENDIX-E: PI CONTROLLER DISCERETIZATION

In continuous time, Proportional Integral (PI) controller may be represented as:

$$y(t) = u_p(t) + u_i(t) = K_p x(t) + K_i \int x(t)\,dt \tag{E.1}$$

where u_p is the proportional term, u_i is the integral term, K_p is the proportional gain of the PI controller, K_i is the integral gain of the PI controller and $x(t)$ is the error between the reference and feedback inputs.

In discrete form the integral term can be written as,

$$u_i(n) = K_i T_s \sum_{h=0}^{n} x(h) \tag{E.2}$$

where T_s is the sampling interval. For $(n-1)^{th}$ sample,

$$u_i(n-1) = K_i T_s \sum_{h=0}^{n-1} x(h) \tag{E.3}$$

Subtracting (E.3) from (E.2) and rearranging gives,

$$\begin{aligned} u_i(n) &= u_i(n-1) + K_i T_s x(n) \\ &= z^{-1} u_i(n) + K_i T_s x(n) \end{aligned} \tag{E.4}$$

where, z is a unit sample delay operator. Multiplying both sides of (E.4) by 'z' gives,

$$u_i(n) = K_i T_s \frac{z}{z-1} x(n) \tag{E.5}$$

Therefore, from (E.1) and (E.5) in discrete period the PI controller may be mathematically modelled as,

$$y(n) = \left[K_p + K_i T_s \frac{z}{z-1} \right] x(n) \tag{E.6}$$

LIST OF PUBLICATIONS

International Journals

- S. K. Singh and S. G. Choudhuri, "Proportional Integral Control Realized in Stationary and Synchronous Reference Frames for a Single-Phase UPS Inverter System : A Comparative Study," *IETE Tech. Rev.* (*Taylor & Francis*), 2018. (Accepted and Online)
- S. K. Singh and S. Ghatak Choudhuri, "Hierarchical Fuzzy Control Applied to Parallel Connected UPS Inverters Using Average Current Sharing Scheme," *J. Inst. Eng. Ser. B* (*Springer*), vol. 99, no. 4, pp. 369–381, Aug. 2018.
- S. K. Singh and S. Ghatak Choudhuri, "Hybrid iterative learning control strategy for single-phase UPS inverter using inductor current active damping," *IET J. Eng.*, vol. 2018, no. 4, pp. 230–238, Apr. 2018.
- S. K. Singh and S. Ghatak Choudhuri, "Instantaneous Average Current Feed Forward Control for Equal Load Sharing in Parallel Connected Multi-Inverter UPS System," *IET Journal of Power Electronics.* (Under Review)

International Conferences

- S. Singh and S. Ghatakchoudhuri, "Average Current Feed-Forward Control for Multi-modular Single-Phase UPS Inverters System," *2016 7th International Conference on Intelligent Systems, Modelling and Simulation (ISMS)*, Bangkok, 2016, pp. 244-249.
- S. K. Singh and S. G. Choudhuri, "Active damping control with a feed forward loop for single-phase UPS inverter system: A comparative study," *2015 International Conference on Energy Economics and Environment (ICEEE)*, Noida, 2015, pp. 1-5.
- S. K. Singh and S. Ghatak Choudhuri, "A conflict in control strategy of voltage and current controllers in Multi-Modular single-phase UPS inverters system," *2017 10th International Symposium on Advanced Topics in Electrical Engineering (ATEE)*, Bucharest, 2017, pp. 631-636.
- S. K. Singh and S. G. Choudhuri, "A Comparative study of control topologies for single-phase UPS inverter system," *2017 Asian Conference on Energy, Power and Transportation Electrification (ACEPT)*, Singapore, 2017, pp. 1-6.