THREE PHASE MULTIPOINT CLAMPED INVERTERS AND MODULATION STRATEGIES

Ph.D. THESIS

by

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ROORKEE – 247667 (INDIA)
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ROORKEE

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in this thesis entitled "**THREE PHASE MULTIPOINT CLAMPED INVERTERS AND MODULATION STRATEGIES"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electrical Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from January, 2014 to December, 2018 under the supervision of Dr. Pramod Agarwal, Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(Narendrababu A)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

(Pramod Agarwal)
Supervisor

The Ph.D Viva-Voice examination of Mr. Narendrababu A, Research scholar, has been held on…….

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ABSTRACT

In the recent years, the high penetration of various renewable and other non-conventional distributed generators with greater power capability has been an increasing interest. Sources like photovoltaic (PV) generators, fuel cells, wind-energy systems are widely being integrated into power system at distribution level. The main advantages of renewable sources are that they are inexhaustible and environmentally friendly in nature. However, due to uncertainty and uncontrollability of these sources, energy storage systems, power conversion and conditioning techniques are more challenging than ever for grid-connected systems or stand-alone systems. Power electronics, being the technology of efficient electric power conversion is an essential part for integration of various distributed generation systems (renewable energy and non-renewable energy systems) in power system.

Power converters such as DC-DC-AC and AC-DC-AC are typically required for integration of low voltage distributed generation sources into grid. Theoretically, a DC-DC boost converter followed by a conventional two-level voltage source inverters (VSI) can increase the voltage to desired level. However, the system imposes several limitations due to various factors and existing semiconductor technology. Since the RMS ac voltage output at the DC-AC input stage is always less than the DC link voltage, several PV arrays are connected in series to meet the required voltage level. A conventional two-level VSI does not allow the independent control of individual PV array in such cases.

Multilevel VSIs play the key role in aforementioned scenario by allowing direct connection of several low voltage PV arrays for their independent control and maximum utilization. Over the past few decades, multilevel power conversion technology has generated widespread interest both in the research community and in the industry, as they are becoming a viable technology for many applications. The multilevel topologies like Diode Clamped inverter (DCI), Cascaded H-bridge converter (CHI) and Flying Capacitor inverter (FCI) are considered as conventional multilevel VSIs. They are built with objective of using low voltage rating devices in medium and high voltage applications. However, these conventional multilevel VSI require more switching devices and associated components like driver circuits, power supplies, heatsinks, etc. Therefore, the conventional multilevel VSIs suffers from demerits like complexity, high cost and low reliability compared to two-level VSI counter parts.

Fortunately, with substantial improvement of conventional silicon devices and their packaging technologies, new wide band-gap materials reaching higher junction temperature and voltage blocking levels, are being evolved. As a result, voltage rating of the switching devices is no longer a core concern for opting multilevel VSI in various applications. Conversely,

achieving the functionality of multilevel VSIs (like minimum distortion) with minimum number of switching devices and associated components has become the key factor. This new approach has opened the door to researchers for developing new multilevel topologies aiming different objectives.

The research work starts with the literature survey of the multilevel inverter topologies with reduced device count. These topologies have their relative merits and demerits from the stand point of application requirement. No specific topology can be considered as suitable in all respects in most of the applications. Most of the newly proposed topologies in the literature are basically single-phase structures with “polarity-generation unit” and “level-generation unit”. Some of the multilevel topologies need induvial “polarity-generation unit” and “level-generation unit”, while some other can incorporate single “level-generation unit” for three-phase applications. Such inverters with separate “level-generation unit” must incorporate a greater number of DC-sources as the number of phases increases since they cannot be operated with single DC-link. On the other hand, topologies with common “level-generation unit”, redundancy for generating phase voltage levels is limited and it further leads to unequal load sharing among the DC sources.

In present work, a detailed investigation is carried out on multipoint clamped inverter (MPCI) topologies, which are realized using single DC link for supplying more than one phase. The DC link of MPCI is formed by several low voltage DC sources like PV/Batteries or a front-end converter system. The output voltage levels of each phase are generated passively through number of clamping points in the common DC link of MPCI topology and hence, it is functionally equivalent to a single-pole multiple-throw switch ($n \geq 3$ positions) (e.g., the diode-clamped topology). MPCI structure is also advantageous due to the requirement of least number of DC sources for multi-phase operation compared to other topologies. Furthermore, it can generate balanced phase voltages even under DC input source voltage variations, which are likely when using PV/Batteries. This thesis investigates the three-phase MPCI topologies and modulation strategies for the possible applications including renewable energy grid interface, energy storage system, electric drives and energy control centre for smart grid and micro-grids. The key challenges of the power conversion system are identified as power circuit complexity, modulation algorithms and power quality for MPCI topologies.

The modulation techniques for MPCIs are relatively complex compared to the two-level counter parts. The control techniques are generally classified as Carrier based modulation and space vector modulation (SVM). Carrier based modulation methods are very simple to implement. On the other hand, SVM provides the complete control over the modulation of the VSI. In this thesis, SVM is considered for detailed analysis. In SVM, there are number of ways to select the set of voltage vectors for synthesizing the reference vector. The selected voltage

vectors along with the switching sequence play key role for achieving various functionalities of the VSI like: Power loss reduction, power quality, capacitor voltage balancing etc. In the present work, the SVM strategies are classified as nearest three vector modulation (NTV) and non-nearest three voltage vector modulation (non-NTV). NTV modulations depending on the type voltage vectors selected. NTV strategies are very common as they produce better harmonic performance. However, depending on the MPCI topology, NTV strategies have several limitations. In such cases, non-NTV methods are essential even if they relatively increased harmonic distortion in the output voltage and current waveforms.

Three-level (3L) neutral point clamped inverter (NPCI) is the simplest example of MPCI. These are proven to be excellent tradeoff solution between performance and cost in high-voltage and high-power systems. The main advantages of 3L NPCI are reduced voltage ratings for the switches, good harmonic spectrum (making possible the use of smaller and less expensive filters), and good dynamic response. Even for low voltage applications, the NPCI and equivalent topologies like T-type NPCI are widely used as an alternative to two-level VSIs. In the present work, first 3L NPCI is presented thoroughly. NTV and non-NTV modulation strategies are implemented on 3L NPCI for elimination of low frequency neutral point (NP) voltage oscillations. A simplified implementation algorithm is developed for NTV and non-NTV modulation strategies. Therefore, coordinate transformation, trigonometric expressions and solutions of volt-second balance equations are not required in the proposed algorithms. Moreover, the unique feature the proposed modulation algorithm is that, they do not require independent voltage-second balance equations for NTV and non-NTV modulation strategies. Therefore, these algorithms can be easily modified for implementing the hybrid modulation methods without increasing the computational burden.

Further analysis is focused on reducing the complexity of MPCI topologies by minimizing power semiconductor device (PSD) count. In this context, first, a reduce device count 3L inverter termed as hybrid 2/3 level (2/3L) NPCI is presented based on the concept of non-NTV modulation. It can be formed by addition of two half bridge modules to a two-level inverter thereby uses only ten active switches. It can save two active switches and six clamping diodes compared to the conventional NPCI. However, as a result of reduction in switching combinations, the medium voltage vectors are absent in the SVD of hybrid 2/3 level inverter. The voltage vector selection is also no longer similar to conventional 3L NPCI. In order to address this issue, two types of voltage vector selection methods for hybrid 2/3L NPCI are investigated to approximate the reference vector very closely. Effect of different switching state selections is studied in detail. A new virtual vector modulation to use both the small vectors for entire modulation index range is also proposed. Therefore, the modulation allows the interconnection of Z-source network to the hybrid 2/3L NPCI. Two new switching sequences for

higher modulation range are analyzed to retain the same number of device commutations even with the insertion of shoot-through states.

It was observed that, in case of MPCI, if an attempt is made to reduce the number of active switches, it affects the number of available switching states (or voltage vectors) for synthesizing the reference voltage vector. Therefore, such devices are considered as reduced switching state (RSS) MPCI topologies. The position of available voltage vectors in SVD of a given RSS MPCI depends on i) total number of switching devices and ii) structure of the RSS MPCI topology. This effect is further explored by studying four and five level RSS MPCI topologies in detailed with different possible structures. Modulation techniques for such topologies are also investigated for synthesizing the reference vector using the available voltage vectors for achieving minimum distortion.

Computer simulation studies have been carried out in MATLAB/Simulink to verify the performance of various MPCI topologies and modulation strategies under different load conditions. The simulation study has been carried out for both steady-state and transient conditions. To validate the simulation studies of different topologies, downscaled hardware prototypes have been designed, developed and tested. The Real-Time Interface (RTI) of MATLAB and RT-Lab controller (OP 5600) are used to generate gate pulses for switching devices of the developed prototype. Different hardware components as required for the operation of the experimental set-up such as pulse amplification, isolation circuit, dead-band circuit, voltage and current sensor circuits have been developed and interfaced with the RT-Lab controller. As the experimentation is carried out at reduced voltage, for validating the experimental results, downscale simulation results are also performed and compared with experimental results. The experimental results have been found to be in good agreement with the simulation results. Although all the proposed schemes are experimentally tested and validated on downscaled laboratory prototypes, but the proposed topologies, SVM technique are general in nature and can be easily applied to high power applications.

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(Narendrababu A)

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LIST OF ACRONYMS

ANPCI	Active Neutral Point Clamped Inverter
APOD	Alternative Phase Opposition Disposition
BESS	Battery Energy Storage System
CUPS	Custom Power Systems
CHBI	Cascaded H-Bridge Inverter
DG	Distribution Generation
DCI	Diode Clamped Inverter
DVR	Dynamic Voltage Restorer
DTT	Dual Three-Level T-Type
ESS	Energy Storage Systems
FCI	Flying Capacitor Inverter
FS-MPC	Finite State Model Predictive Control
LS-PWM	Level-Shifted PWM Methods
MT	Main Triangle
MLI	Multilevel Inverter
MPCI	Multipoint Clamped Inverter
MMI	Modular Multilevel Inverter
NPCI	Neutral Point Clamped Inverter
NP	Neutral Point
NTV	Nearest Three Vector
Non-NTV	Non-Nearest Three Vector
OBVS	Optimal Balancing Vector Selection
p.u.	Per Unit
PV	Photovoltaic
PSD	Power Semiconductor Devices
PUC	Packed-U Cell
PWM	Pulse Width Modulation
PS-PWM	Phase Shifted PWM
POD	Phase Opposition Disposition
PD	Phase Disposition
PDR	Phase Duty Ratios
RSS	Reduced Switching State
RTI	Real Time Interface
SVC	Static Var Compensators
STATCOM	Static Synchronous Compensator

SVM	Static Synchronous Compensator
SVD	Space Vector Diagram
SHE	Selective Harmonic Elimination
STV	Selected Three Vector
SMPS	Switch Mode Power Supplies
TBV	Total Blocking Voltage
VSI	Voltage Source Inverter
VV	Virtual Vector
ZNPCI	Z-Source NPCI
2L	Two Level
2/3L	2/3 Level
3L	Three Level
4L	Four Level
5L	Five Level

LIST OF SYMBOLS

f_{Cr}	Carrier Frequency
m_f	Frequency Modulation Index
m	Modulation Index
V_{ref}	Reference Vector
V_{ab}	Line-to-line Voltage
V_{aO}	Pole Voltage
V_{DC}	DC Link Voltage
i_{NP}	Neutral Point Current
φ	Power Factor Angle
θ_1	Angle of Reference Vector with respect to Sector-1
d_x, d_y, d_z	Duty Ratios of Equivalent 2L SVD

Chapter 1: INTRODUCTION

1.1 Overview

Today, most of the users are inactive receivers of electricity without further involvement in the management of the sources and the grid; each user is simply a hole for electrical energy. Due to the ever-increasing demand of electricity, the amount of load has grown above what was predicted when the grid was designed. In response to the above and the climate change challenge, many countries in the recent years have started the process of liberalization of their electrical power systems, encouraging renewable energy sources. As a result, there has been an increasing interest in the penetration of various renewable and other non-conventional energy sources with greater power capability. Sources like photovoltaic (PV) generators, fuel cells, wind-energy systems are widely being integrated into power system at various locations not only at power generation level, but also at power distribution level. These Distribution Generation (DG) sources and other infrastructure are also transforming the radial architecture of distribution systems towards smart distribution to allow the customer to take an active role in the supply of electricity. There is a great opportunity for new players such as Custom Power Systems (CUPS), Energy Storage Systems (ESS) and DG, smart end-user appliances together with communications provide better network capability, flexibility and functionality [1].

Summarizing, a modernized electric grid would create power system that:

- Provides the platform for the use of Renewable and Green energy sources, allowing the backup of inter connected power grid into small, regional clusters during emergencies.
- Cut outs capital costs of new T&D infrastructure as well as generating plants.
- Reduces peak loads and generate reserve margins.
- Lowers T&D line losses together with operation and maintenance costs.
- Redirects power flows, changes load patterns, and improves voltage profiles and stability.
- Enables ESS and DG to participate in system operations.
- Provides system utilities with advanced visualization tools to enhance their ability to oversee the system.

1.2 Role of Power Electronic Systems (PES) in Modern Electric Grids

Power electronics systems (PES) are being used in many industrial and transportation applications from past several years as motor drive for pump, fan compressor, conveyor, grinder or propulsion system, etc. In modern electric grids, PES is an essential part for integration of

various distributed generation systems (renewable energy and non-conventional energy systems) and energy storage systems (ESS) in power system network [2]. Further, they serve as energy router and energy control center in smart grid infrastructure. Modern power electronic arrangements in various levels of power system are: a) PES in transmission system; b) PES in distribution system.

1.2.1 PES in Transmission System

Transmission system technologies are mainly a) ac transmission system and b) dc transmission system. PES in ac transmission system widely known as FACTS devices. Typical examples of FACTS devices are: SVCs (Static Var Compensator); STATCOMs (Static Synchronous Compensator); TCSC (Thyristor Controlled Series Compensator); TSSC (Thyristor Switched Series Compensator) and SSSC (Static Synchronous Series Compensator); SPS (Static Phase Shifter); and UPFC (Unified Power Flow Controller). The FACTS devices can control the electric power flow in AC systems of same frequency.

On the other hand, the dc transmission is built on power conversion technology that converts ac power into dc power and known as HVDC transmission. An advantage of HVDC devices is the capability to transmit energy between systems of various frequencies. In HVDC devices the entire energy from one system flows into the other through inverters. As a result of this cost is high, even in single-station installations. The conventional HVDC transmission uses the SCR thyristors and it is necessary to use large filters and allows only unidirectional power flow. This drawback does not occur when using self-commutated devices, such as GTO thyristors or IGBT transistors.

1.2.2 PES in Distribution System

Distribution systems are mainly consisting of low rating sources and loads. The various functions of PES in distribution are listed as follows.

1) PES plays the key role in the microgrid environment, integrating renewable energy sources and home electronic appliance.
2) PES is essential for interfacing Electric Vehicles in V2G and G2V configurations.
3) Energy storage systems are connected through the PES and serves the purpose of power quality maintenance and balancing the energy in the system.
4) PE converters/controllers control the power flow between various sources and loads.

Figure 1-1 illustrates the most important areas of use of PES in electrical power network, at various levels of power.

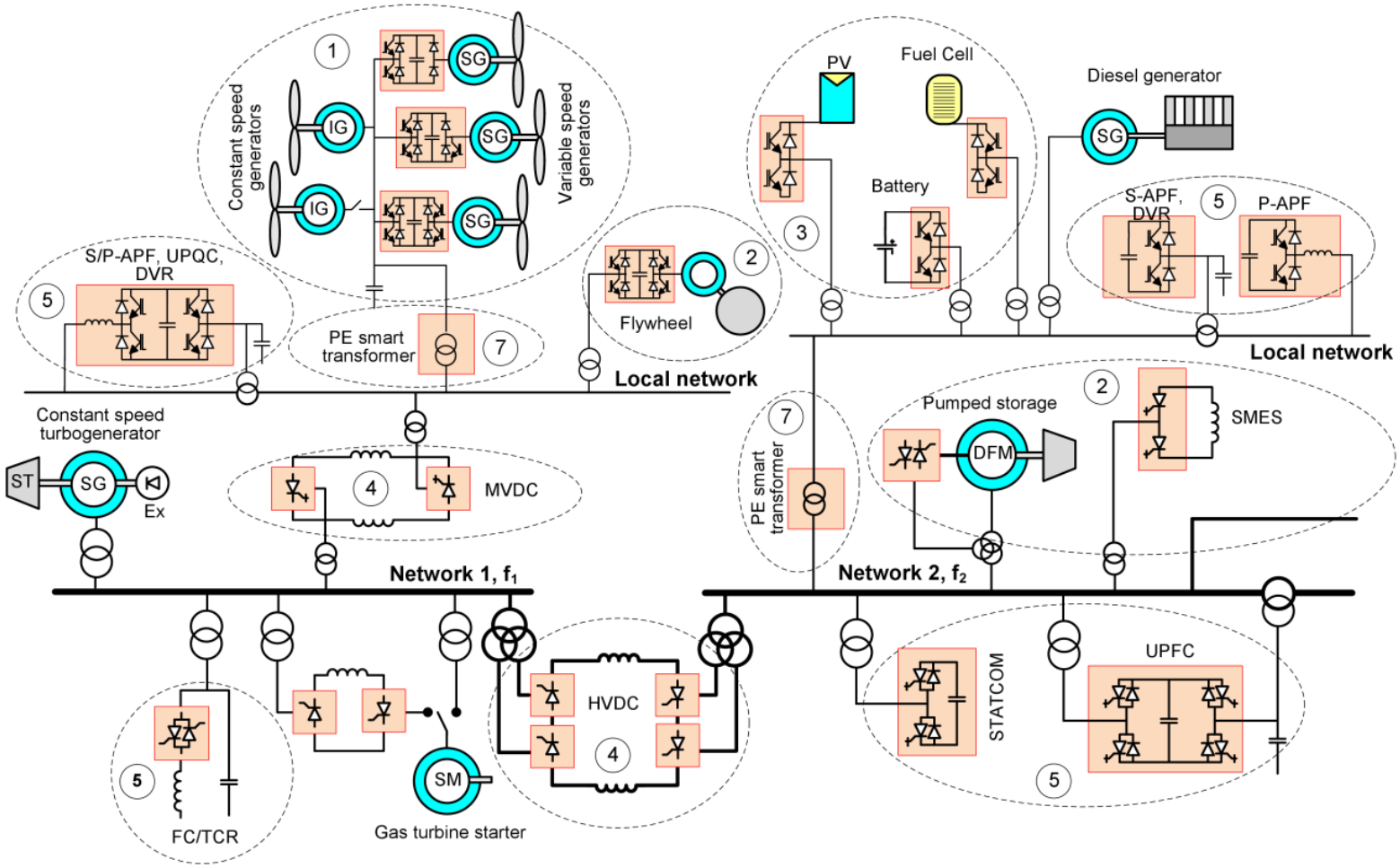


Figure 1-1 Area of application of PE arrangements in electrical energy network: 1) wind generators, 2) energy storage, 3) power supply systems from low-voltage sources, 4) network couplers, 5) devices for improvement of energy quality, 6) devices for control of energy delivery.

1.3 Research Background

Most of the DGs are available either as DC sources or contain an intermittent dc stage. To integrate these sources into existing ac grids and other loads, a DC-AC power conversion system is essential. Conventionally, a two-level voltage source inverter (VSI) is widely used for such conversion stage. However, a practical power conversion system imposes several limitations due to existing semiconductor technology and implementation factors.

The rating of VSI is limited by the available semiconductor devices rating. Figure 1-2 shows the state of art semiconductor technology available from various manufacturers. The high power and high voltage rating can be obtained by a two-level (2L) VSI by connecting the devices in series and parallel. However, the dynamic current and voltage sharing of such connection of devices are still a challenge. The high-power device like IGCT, GTO can only be switched at very low frequency, and are really expensive and requires sophisticated driving circuit, snubber circuit and protection circuit, all of which increases the cost and complexity of the converter.

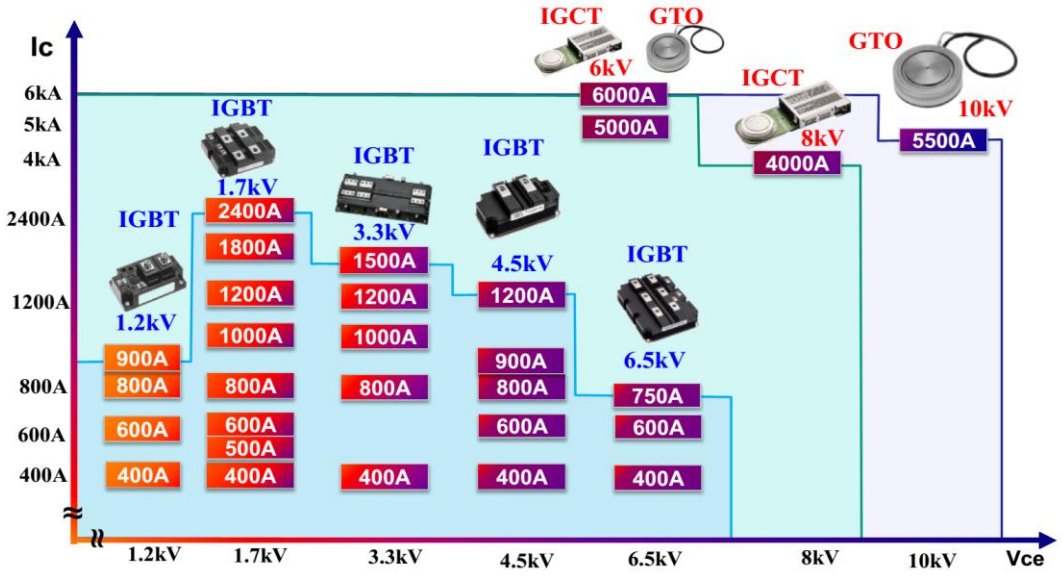


Figure 1-2 Voltage and current rating of the semiconductor devices [3]

Renewable sources (like PV arrays, Fuel cells) and ESS are usually operated at below their maximum installed capacity and are also variable in nature. Therefore, a DC-DC converter is usually employed for voltage regulation and galvanic isolation of these sources. If a centralized 2L VSI is employed for DC-AC conversion, it requires a single regulated DC input voltage which is higher than the peak of the output voltage. In order to meet the required voltage level, regulated DC sources are then connected in series to form strings. Several such strings are further connected in parallel depending on the power level. For example, if a PV system is using a two-level VSI, the following issues are evident [4]:

1) Individual PV panel rating is low (usually a few hundred watts peak (Wp), at operating dc voltages ranging from 15 to 35 V) and hence they require large number of series connections to increase the voltage rating.
2) The series connection of such low voltage sources does not allow the independent control of individual PV module to operate at optimal point (Maximum Power Point) as same current must drive.
3) A mismatch in the I-V characteristics of the series connected PV arrays due nonuniform irradiation (caused by partial shading, dust) or internal parameter variations (caused by panel aging) results in activation of bypass diodes to avoid hot-spot effects. This phenomenon is very common and lead to poor utilization of available power [5].

Therefore, ever if the voltage level is attained by a two-level VSI, it is not preferred solution for integration of low voltage sources like PV; fuel cells and battery/super-capacitor storage systems.

1.4 Multilevel VSI Systems

Multilevel VSIs play the key role in aforementioned scenarios by allowing direct connection of several low voltage DC sources (requires minimum number of series connections) for independent control and maximum utilization. Besides being able to provide more flexibility for integration of low voltage DC sources, the MLIs usually offers several other inherent advantages including (i) reduced voltage ratings for the Switches, (ii) increased efficiency, (iii) a lower output ac-voltage harmonic distortion and (iv) making possible the use of smaller and less expensive filters and good dynamic response. [6],[7],[8]. All the conventional multilevel topologies [8] like Neutral Point Clamped or Diode Clamped inverter (DCI) [9], Cascaded H-bridge inverter (CHBI) [10] and Flying Capacitor inverter (FCI) [11] topologies are extensively examined in past few decades for extended application fields and control and optimization methods are developed [7], [12]–[23][24]. A brief classification of these topologies is shown in Figure 1-3:

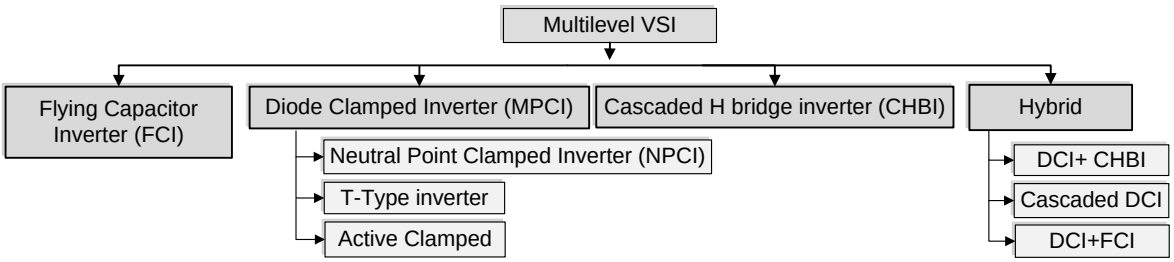


Figure 1-3 Classification of Multilevel VSIs

1.4.1 Diode Clamped Inverter (DCI)

The diode clamped inverter (DCI) has been proposed in [9] and it was technically a three-level VSI or neutral point clamped inverter. Figure 1-4 shows the simplified circuit diagram of a 5L DCI. The DCI employs cascaded DC-link capacitors to form a single high voltage DC-link. The intermediate points “1”, “2” and “3” are called clamping points and are connected to the output terminal x (x=a,b,c) through the clamping diodes and the switches. Each phase-leg of five-level (5L) DCI composed of eight active switches (with antiparallel diodes) from S_1 to S'_4. The upper and lower switches of each phase-leg are operated in complementary manner and the complementary pairs are (S_1, S'_1), (S_2, S'_2), (S_3, S'_3), and (S_4, S'_4). The voltage across each of the dc capacitor is normally equal to one fourth of the total dc voltage ($4V_{dc}$). The structure can be extended to generate higher voltage levels.

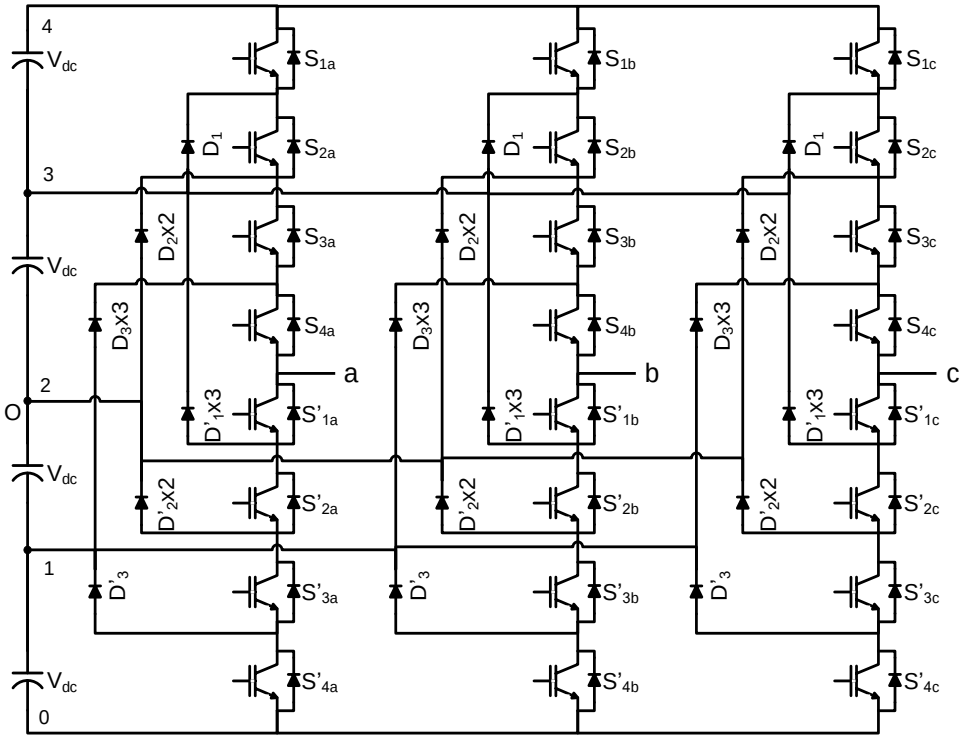


Figure 1-4 A three-phase 5L DCI.

The DCI VSI are best suitable for back-to-back regenerative applications [25]. The NPCI, has found wide application in high-power medium-voltage systems. It has simple power circuit structure and requires minimum capacitors or voltage sources. As the DCI structure is increased to higher number of levels, the number of clamping diodes increases drastically and therefore become less attractive due to increased losses and uneven loss distribution among devices [26]. Some other complications of the diode clamped inverter with higher number of levels is the dc link capacitor voltage balancing problem.

The uneven loss distribution of DCI VSI devices can be substantially improved by replacing the clamping diodes with clamping switches as shown in Figure 1-5. This allows the current to flow in any of the clamping paths irrespective of its direction. These topologies are called active-DCI (ADCI) VSI.

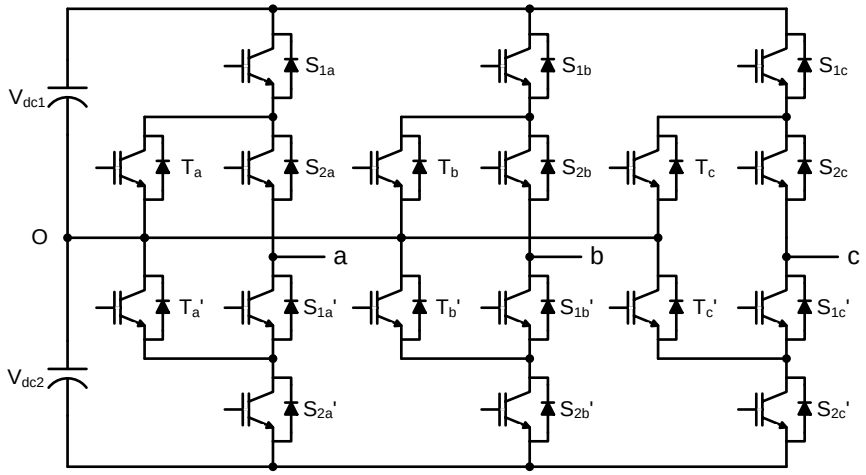


Figure 1-5 A three-phase 3L ANPCI.

1.4.2 Flying Capacitor Inverter (FCI)

The flying capacitor inverter (FCI) is considered as another fundamental multilevel topology formed by series connection of capacitor switching cells [11]. Figure 1-6 shows the circuit configuration of a 5L FCI. Unlike DCI, the FCI has the phase voltage redundancy which can be used to balance the voltages of the flying capacitors (C_F) and equally distribute losses among the semiconductor devices [27]–[29]. In summary, advantages and disadvantages of FCI are as follows.

Advantages:

- The flying capacitors provide extra ride through capabilities during power outage.
- The switching state redundancy of FCI provides a great flexibility for capacitor voltage balancing and power loss distribution among the switches.
- Reconfiguration of circuit is possible during fault or under-rated conditions.

Disadvantages:

- Exponential increase in the required number of flying capacitors as the number of inverter levels is high.
- Package is more difficult and more expensive with the required bulky capacitors.
- Capacitors voltages have to be pre-charged at startup to a value which are close to their nominal values.

FCI have found particular applications for high bandwidth–high switching frequency applications such as medium-voltage traction drives.

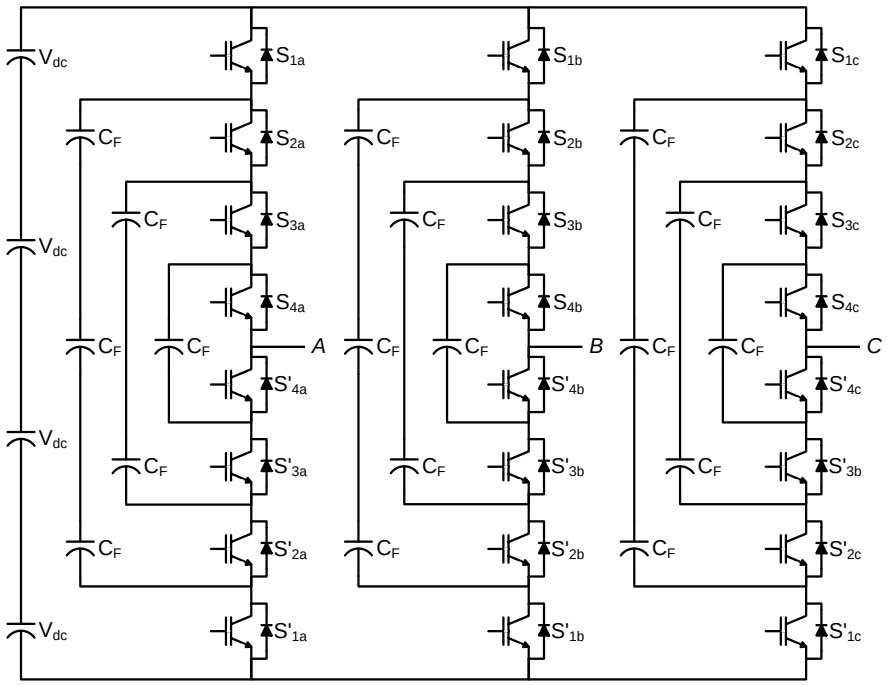


Figure 1-6 A three-phase 5L FCI.

1.4.3 Cascaded H-Bridge Inverter (CHBI)

The CHBI was first appeared in 1988 and slowly gained more attention after 1997. CHBI formed by cascade connection of modular chopper-cells or H-bridge cells to form each cluster or arm [10]. Figure 1-7 shows the 5L CHBI topology formed by two full bridge cells per phase. CHBI topology is suitable for high voltage applications due to its highly scalable and modularized structure.

The asymmetrical CHBI [21] is another version of CHBI topology that contains each H-bridge cell with different DC link voltage. As a result, the same number of H-bridge cells can generate more voltage levels compared to the CHBI. However, this eliminates the per phase redundancy which is one of the important features of the CHBI topology. Moreover, due to the different DC-link voltages, the associated H-bridge cells should have different voltage stress and loss. Therefore, the device rating for each cell becomes different and the system lost some modularity.

The CHBI with two legs per phase with identical bidirectional chopper cells (either full bridge or half bridge cells) are known as Modular Multilevel inverter (MMC) [30]. Unlike the CHBI topology, the MMC topology shares a common DC-link for all the phases. Therefore, does not require isolated DC sources. However, the capacitor of the H-bridge cell will come into picture only once per a fundamental cycle. As a result, the size of the capacitors needs to be relatively

large for withstanding charge for longer duration. In conclusion, a CHBI VSI should require either a greater number of isolated sources or large capacitors. The MMC topology is one of the next-generation multilevel Inverters intended for high or medium-voltage power conversion without line-frequency transformers [31].

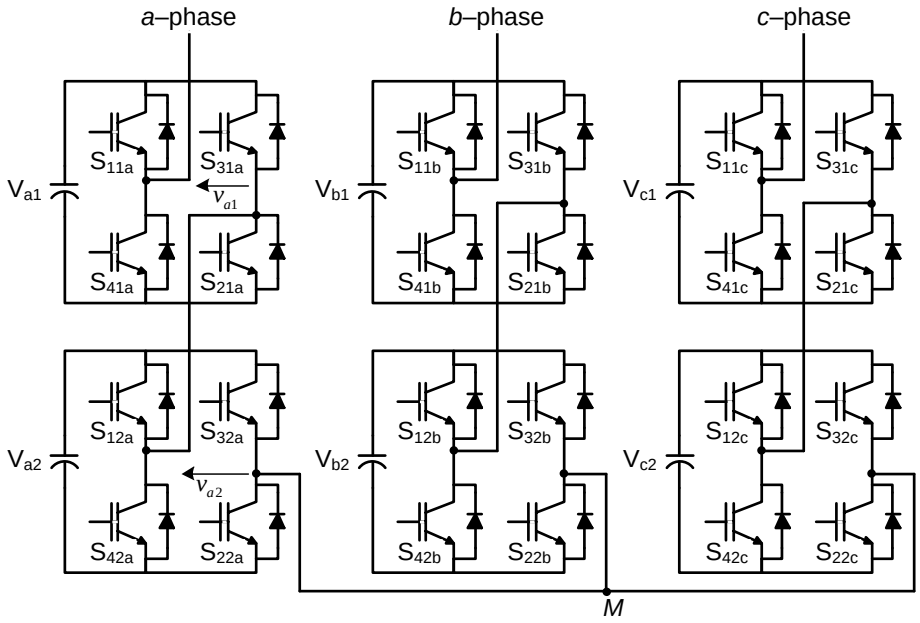


Figure 1-7 A three-phase 5L CHBI topology.

Some of the advantages of CHBI are listed below:

- They have simple construction, flexibility design and can be easily extended to higher number of levels.
- They can achieve high or medium-voltage power levels with low-voltage power semi-conductor devices.
- MMC VSI eliminate the requirement of isolated dc sources, therefore eliminates the heavy and bulky line frequency transformer.
- Reconfiguration of circuit is possible during under-rated or fault conditions.

The applications of CHBI include Static Synchronous Compensator (STATCOM), Battery Energy Storage System (BESS), Dynamic Voltage Restorer (DVR) and HVDC (MMC topologies) systems.

1.5 Comparative Evaluation of Conventional MLIs

Simple comparative analysis of conventional multilevel inverters is given in this section. Table 1-1 gives the comparison of power component required for the above discussed multilevel inverter topologies (m=phaser voltage levels).

Table 1-1 Comparison of power component requirements among three-phase multilevel inverter topologies.

Power component	Inverter topology		
	DCI	FCI	CHBI
Main switching devices	$2(m-1)\times 3$	$2(m-1)\times 3$	$2(m-1)\times 3$
Anti-parallel diodes	$2(m-1)\times 3$	$2(m-1)\times 3$	$2(m-1)\times 3$
Clamping diodes	$(m-1)(m-2)\times 3$	0	0
DC bus capacitors	$(m-1)$	$(m-1)$	$\frac{(m-1)}{2}\times 3$
Flying capacitors	0	$\frac{(m-1)(m-2)}{2}\times 3$	0

1.5.1 Hybrid Multilevel Inverters:

Different combined topologies can be obtained by replacing the various clamping points (like positive bus, negative bus and intermediate points) of the conventional DCI topology [32]. Figure 1-8 shows a 5L hybrid VSI formed by a two-level and three-level topologies. The inverters synthesized by using these techniques usually requires fewer number of clamping diodes compared to DCI counterpart topologies. However, the number of controlled switches (IGBTs/MOSFETs) are equal in both the topologies, which means the driver circuits are actually the same. Therefore, it doesn't significantly cut down the cost in low power applications. In [33], [34] authors have proposed four-level inverter structures as combination of two level inverter and three level neutral point clamped inverter (NPCI). These topologies requires more number of controlled switches (8 in [33] and 10 in [34]) as compared to the DCI counterpart. On the other hand, despite of increased cost, they cannot provide the phase voltage redundancy to improve inverter efficiency. It is also observed that these [32]–[35] requires the controlled switches with high blocking capability which also increases the cost per switch compared to DCI.

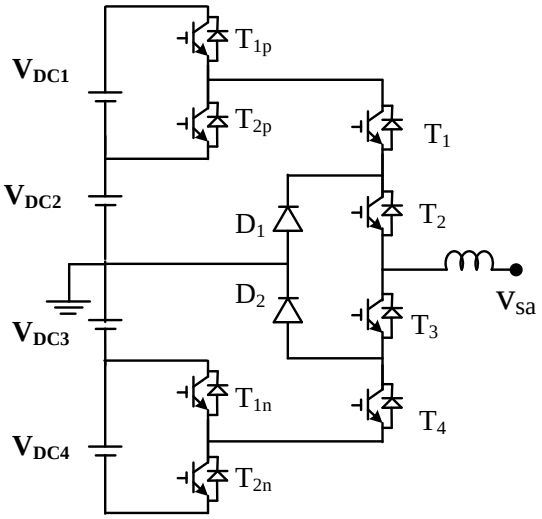


Figure 1-8 A 5L Hybrid VSI proposed in [32].

Therefore, multilevel inverters, exhibit following limitations for increased number of output voltage levels,

i) A large number of power semiconductor switches and gate driver units.
ii) Complexity of the hardware and reduced system reliability.
iii) Protection circuit and heat sink etc., causing overall system to be more expensive, and bulky.
iv) Increased Control system complexity.

1.6 New MLI Topologies with Reduce Device Count

For Multilevel inverters with a high-resolution waveform, therefore, prime concern is to reduce count of Power Semiconductor Devices (PSD) and gate driver circuits. Recently researchers paid attention to minimize the component count in multilevel topologies through various approaches. In general, the newly proposed multilevel VSIs can be classified base on the notions like

i) Switching devices count and auxiliary components,
ii) Total voltage blacking capability required,
iii) Switching frequency of devices,
iv) Use of symmetric and asymmetric sources,
v) Capability for even power distribution among sources etc.

The present work starts with the literature survey of the topologies for multilevel inverter with reduced device count. The new multilevel topologies are evolved fundamentally to minimize the complexity and cost of the VSI systems by minimizing the devices and associated components. These topologies however, have their relative merits and demerits from the stand point of

application requirement. Because of its fundamental characteristics, a given topology may be very advantageous in some applications and may become unsuitable in others. No specific topology can be considered as advantageous in all respects in a particular application. It is also worth mentioned that these topologies also require special and complex modulation/control methods for their operation. Some of the new multilevel topologies and their pros and cons are briefly discussed as follows.

Figure 1-9 through Figure 1-11 show the some of the reduced device count multilevel VSI topologies [36]. Figure 1-9 and Figure 1-10 show two class of topologies with discrete “level-generation unit” and “polarity-generation unit”. Where as, Figure 1-11 shows the topologies which does not require separate polarity generation and level generation units. The function of level generation unit is to generate high frequency variable DC voltage depending on the reference voltages across the polarity generation unit. The polarity generation unit operates in the line frequency to convert the DC voltage to AC voltage across the load/grid. Usually, the polarity generation unit is a H-bridge module with devices like GTO due to requirement of 1) the high blocking voltage across the devices (sum of all the source voltages) and 2) only line frequency switching. Some important observations, from Figure 1-9 to Figure 1-11 are summarized as follows.

1) Some topologies produce single high voltage DC-link through cascading several DC-sources, while others topologies do not. The topologies forming single DC-link can be energized with isolated or non-isolated DC sources, while the other topologies should supply with isolated DC-sources.
2) Some topologies exhibit phase voltage redundancy, with can be used to increase the number of voltage levels when energized with different voltage rated DC sources for the same configuration. However, this leads to unequal load sharing among the DC sources.
3) The operating voltages stresses on the switching devices are not uniform. The maximum blocking voltage requirement of polarity-generation unit will reach to the sum of all the DC sources, while, that of the level-generation unit is significantly increased.
4) In Packed-U cell (PUC) topology, the DC-sources should be asymmetric and isolated in nature for functioning of the inverter. However, some of the DC source can be replaced with simple DC capacitors which can be self-balanced using available switching states.
5) Some topologies require bidirectional voltage blocking devices. Moreover, the positive and negative blocking voltage requirement of these bidirectional devices are not uniform.

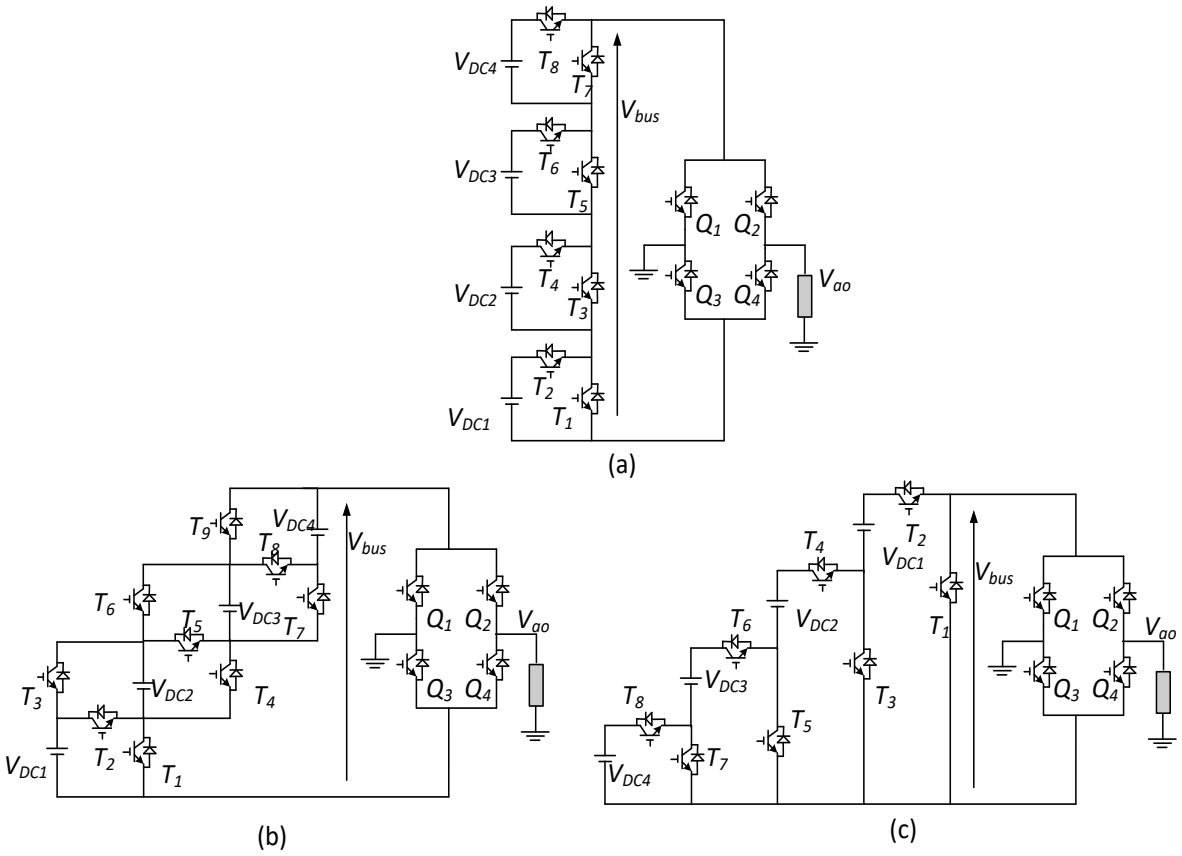


Figure 1-9 Topologies with polarity generation unit which requires isolated DC-sources: (a) and (b) Topologies with phase voltage redundancy and (c) Topology without phase voltage redundancy.

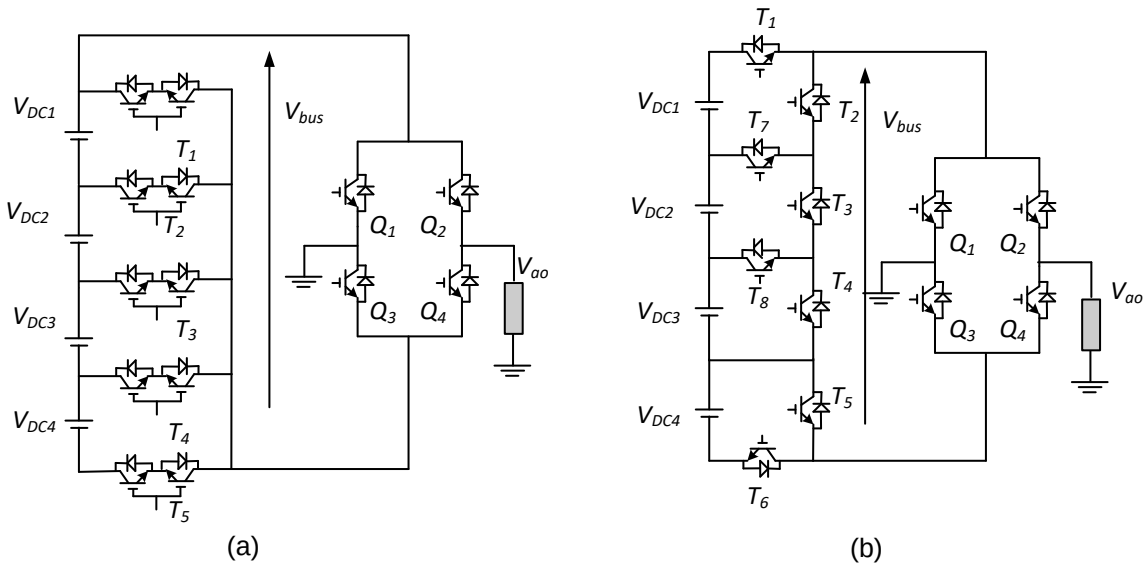


Figure 1-10 Topologies with single high DC-link and dedicated polarity generation unit: (a) Topologies with phase voltage redundancy; (b) Topology with phase voltage redundancy for some voltage levels.

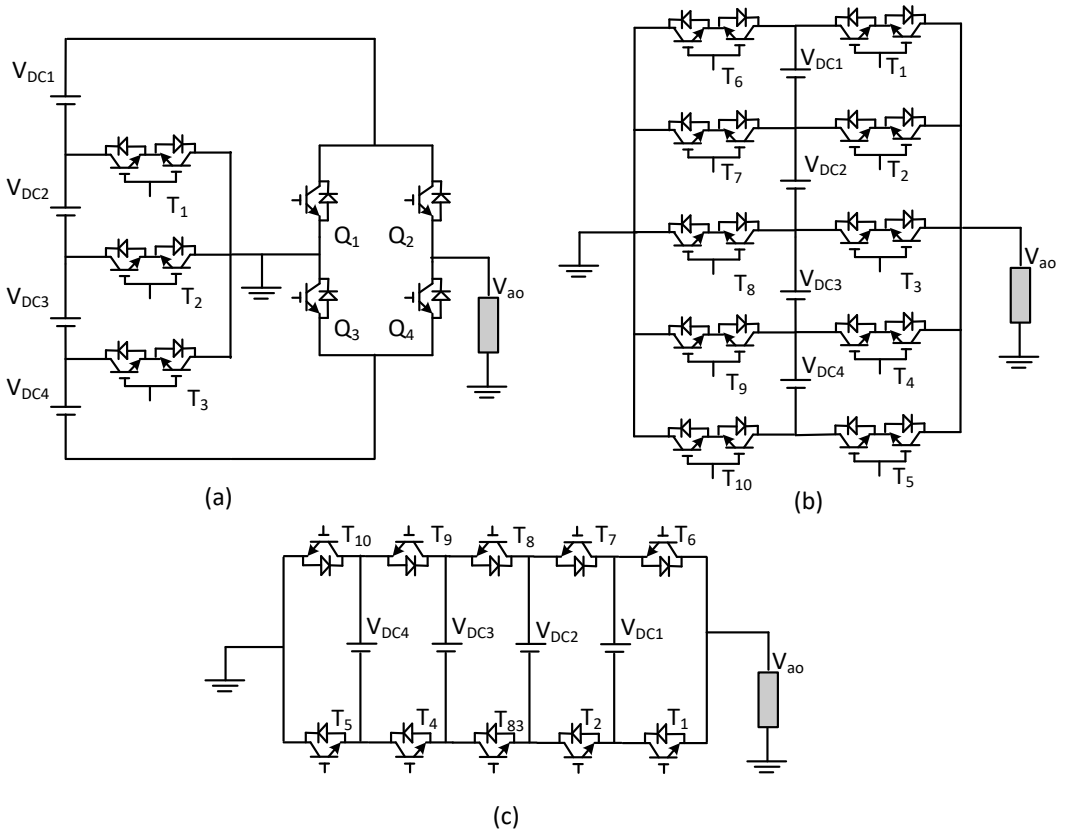


Figure 1-11 Topologies without polarity generator unit: (a) and (b) Topologies with single high voltage DC-link; (c) Packed U-cell topologoy (Topology which requires isolated DC-sources)

On addition, the aforementioned reduced PSD count multilevel VSIs are fundamentally single-phase topologies and therefore, cannot be extended for three-phase applications directly. The important limitations of these topologies when extended to three-phase applications are explained below.

1) The topologies that require isolated DC sources (Figure 1-9 and Figure 1-11 (c)) are not recommended for multiphase operation, as they necessitate separate set of isolated DC sources for each phase. Therefore, the total number of DC-sources and auxiliary circuitry multiplies with the number of phases.
2) If one set of dc sources is commonly used for all the phases, the topologies (Figure 1-10) must incorporate separate “level-generation unit” and “polarity generation unit” per each phase along with a three-phase line frequency transformer.
3) Some topologies do not require separate polarity generation unit (Figure 1-11 (a) and (b)), but still require three-phase line frequency transformer.
4) For topologies without phase voltage redundancy (Figure 1-9 (c) and Figure 1-11 (a)), asymmetrical sources cannot be used to increase the number of levels.

1.7 Three-Phase Multipoint Clamped Inverter (MPCI) Topologies with Reduced Device Count

From above discussion, it is evident that, the newly proposed topologies are attractive for single phase applications to generate higher number of voltage levels with minimum device count, but they show some limitations when extended to three-phase systems. Therefore, in order to avoid the use of line frequency transformer, asymmetrical and isolated DC-source sources in each phase, the topologies which utilizes a single high voltage DC-link for all the phases are considered. Figure 1-12 shows such a generalised multilevel VSI with a common DC-Link. Here, the high voltage DC-link can be formed by single DC source along with capacitors or multiple low voltage DC sources like PV/Batteries. The voltage levels of each phase are generated passively through number of clamping points (1,2,..n-1) equivalent to a single-pole multiple-throw switch ($n \geq 3$ positions). In this thesis, these topologies are termed as Multipoint Clamped Inverters (MPCI).

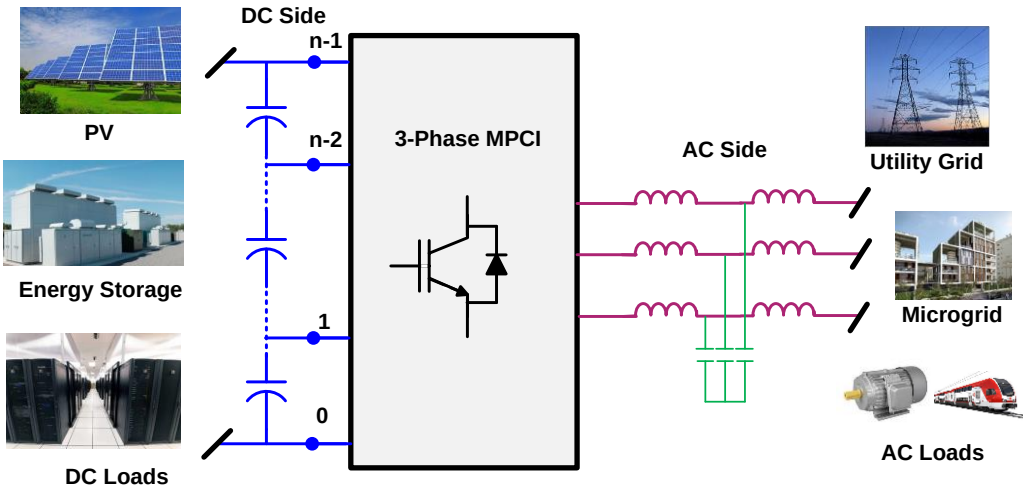


Figure 1-12 A three-phase MPCI structure.

The MPCI topologies are advantageous since, (i) they require least number of DC sources for multi-phase operation compared to other topologies; (ii) the input voltage variation will not cause phase voltage unbalance. Moreover, they are attractive solutions for back-to-back conversion applications like wind energy systems. In this section, some of the newly proposed MPCI topologies are reviewed and compared based on various performance factors.

The diode clamped inverter (DCI) was first proposed in 1981 [9][37]. Since then, many variations like neutral point (NP) clamped inverter (NPCI), active neutral point clamped inverter (ANPCI) have been proposed. The simple structure of these inverters provides several benefits, including utilisation of lower blocking voltage switches (NPCI and ANPCI), improved loss distribution among the switches (ANPCI).

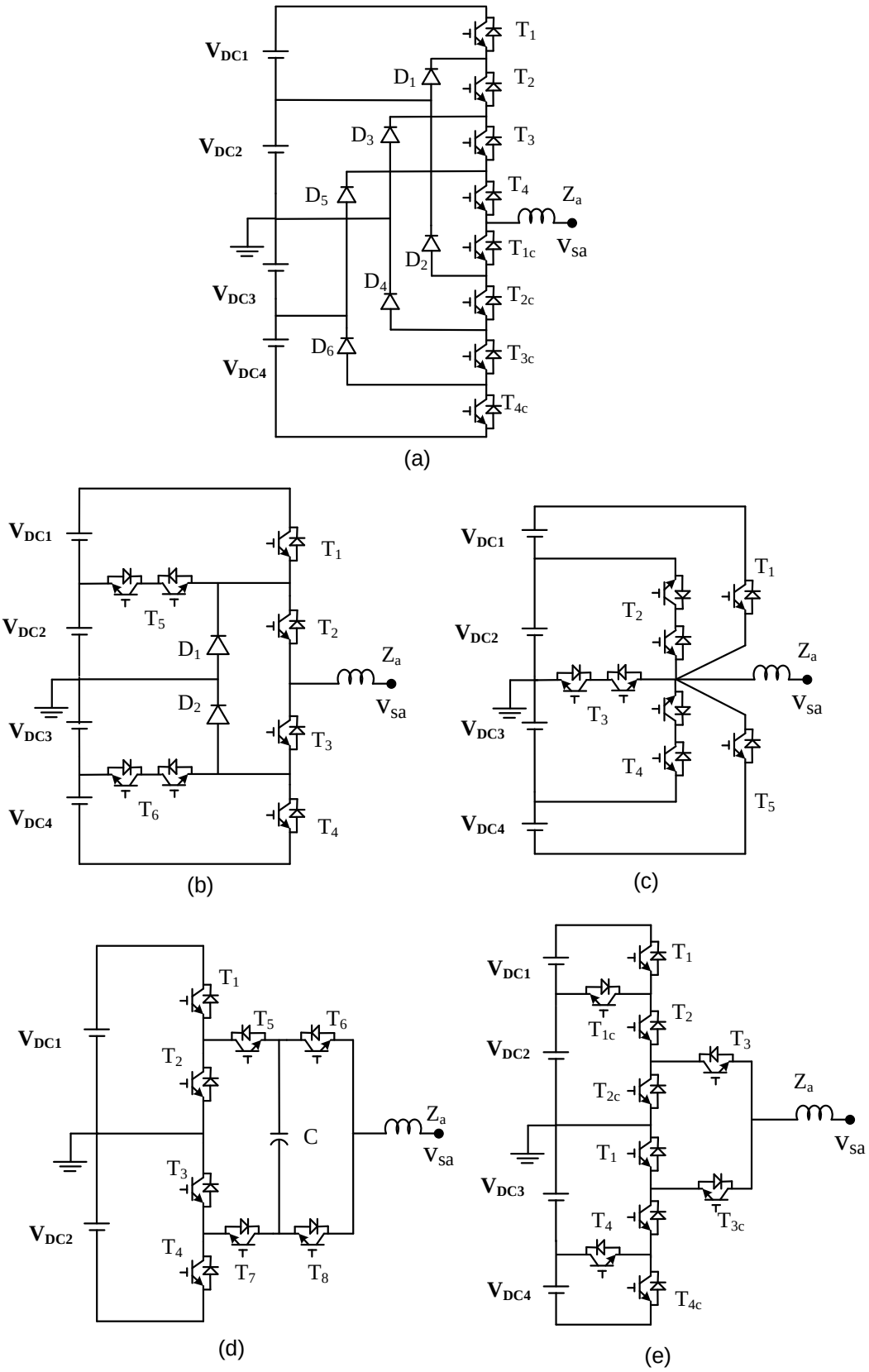


Figure 1-13 Five-level (5L) MPCI topologies in the literature: (a) DCI, (b) Composite multilevel topology proposed in [38], (c) nested multilevel topology [39] (c) ANPC [40] and (d) ANPC for improved loss distribution [41].

In [42][43], the authors proposed a three-level T-type inverter for low-voltage applications, which is an extension of conventional two-level topology with the addition of an active bidirectional switch to the dc-link midpoint, eliminating two clamped diodes per bridge leg. a Combination of NPCI and T-type are also considered for improving the efficiency [44] In [45] author proposed a 5L T-Type-MSSC inverter that has only eight switches and one autotransformer (interphase transformer) with unitary transformation ratio. It presents fewer semiconductors because it does not need clamped diodes consequently reducing the cost and improving the efficiency of the inverter.

An advanced composite multilevel concept is proposed in [38] consists of dual three-level T-type (DTT) topology and a 3L NPCI topology. In this, two bidirectional switches require to block quarter of the DC bus voltage and the remaining switching devices require to block half of the dc bus voltage. in [39], a nested multilevel topology using more number of bidirectional switches (three bidirectional switches for five level) and single common dc link voltage to achieve staircase waveform has been proposed. A new voltage source multilevel inverter topology, that is a hybrid between three-level flying capacitor and T-type inverters, is introduced in [40] as alternative to popular 5L Active Neutral Point Clamped inverter (ANPC) [41]. A modified 5L ANPC with ten switches in each phase is presented in [46] for equal loss distribution.

Figure 1-13 shows some of the 5L MPCI topologies. A brief comparative analysis is carried out and tabulated in Table 1-2. It is observed that, the device count is significantly reduced in presented topologies. However, the active switches are not reduced compared to the conventional DCI. i.e., the number of active switches for the 5L counterparts shown in Figure 1-13 are equal to 8 in all the topologies. Moreover, the elimination of clamping diodes results in increased voltage stress on the active switches. This leads to increased cost of the topologies for high voltage applications due to requirement of high blocking voltage switches.

Table 1-2 Comparison among three-phase MPCI based 5L Topologies

Parameters count	Topologies				
	DCI[47]	DTT [38]	ANPC [41]	Modified ANPC [46]	Nested [39]
IGBTs	24	24	24	30	24
Clamping Diodes	36	12	0	0	0
Bidirectional Switches	0	6	0	0	9
Total blocking voltage of IGBTs (p.u)	24	36	36	42	60
DC sources/ capacitors	4	4	2	4	4
Floating Capacitors	0	0	3	0	0

1.8 Scope of Work and Authors Contribution

To encourage the high penetration of renewable energy, MLI system is chosen as the research target due to the various advantageous over the conventional 2L VSI as discussed earlier. From detailed literature review, it is concluded that, some of the newly proposed MLI have achieved significant reduction in the PSD count and associated equipment. However, due to single-phase nature of these topologies, implementation in three-phase applications is not straight forward.

MLIs with MPCI structure share a common DC-link and hence found suitable for three-phase applications in terms of the required number of isolated DC sources. These are also adventitious for DC sources with variable nature (like PV panels/Batteries) and back-to-back power conversion applications (wind energy). However, the inherent issues in MPCI like capacitor voltage balancing, power loss minimization, equal loss distribution, etc., are still burning challenges.

Several advanced modulation strategies are being developed for MPCI based on Space Vector Modulation (SVM) to address aforementioned issues. However, the implementation of these modulation strategies for addressing aforementioned issues is more complex compared to conventional SVM strategies. Some SVM algorithms based on non-orthogonal coordinate system (60° coordinate systems) and algorithms without transformation (a-b-c system) are efficient for calculation of duty ratios of voltage vectors. However, the vector selection with these methods is limited to nearest three vectors (NTVs). Therefore, implementation of advanced SVM strategies using efficient algorithms is considered for research objective.

Among the MPCI topologies found in the literature, authors claim the significant reduction in PSD count over DCI. However, these topologies are also demanding same number of active switches as that of the DCI. It is observed that the reduction in PSD count in these topologies is limited to the clamping diodes and hence does not significantly reduce complexity and cost of the system. Therefore, this thesis gives special emphasize on various approaches to minimize the active switch count. The MPCI topologies investigated in this thesis are consciously built with either two-level and/or three-level modules as basic building blocks which are readily available from power converter providers like GE, ABB, Siemens etc. As result, no significant design and packaging considerations are required. Fortunately, with substantial improvement of conventional silicon devices and their packaging technologies, new wide band-gap materials reaching higher junction temperature and voltage blocking levels are being and will continue to evolve. As a result, voltage rating of the switching devices is no longer a main concern for most of the applications.

Authors contributions:

- Different space vector-based modulation strategies for MPCI topologies are reviewed and classified on the basis of voltage vector selection as nearest three vector (NTV) and non-nearest three vector (non-NTV) strategies. The existing NTV and non-NTV strategies are evaluated based on various performance and complexity.
- An implementation algorithm suitable for both NTV and non-NTV strategies of MPCI topologies is proposed. The algorithm, is based on equivalent two-level space vector diagram (SVD), and does not require coordinate transformation, trigonometric expressions and volt-second balance equations. The duty ratios of all the voltage vectors for NTV and non-NTV strategies are expressed in terms of readily available line-to-line voltage references. The algorithms are realized on three-level (3L) neutral point clamped inverter (NPCI) for eliminating low frequency neutral point oscillations. Exhaustive simulation results are carried out to evaluate the performance of 3L NPCI for various operating conditions. The algorithm is further extended for higher voltage levels to implement NTV and non-NTV modulations
- In order to improve overall performance of NPCI, NTV strategies are combined with non-NTV strategies to form hybrid modulations. Various combinations NTV and non-NTV selections are studied, evaluated and compared. An algorithm is proposed to implement the hybrid modulation with the help of only NTV duty ratios. It is based on redistribution of NTV duty ratios to non-NTVs in the mapping unit and hence reduces the complex mathematical calculations. A new simple hybrid modulation is also developed and compared with the existing methods.
- A reduced switch count 3L NPCI termed as hybrid 2/3 level (2/3L) NPCI is developed based on the non-NTV selection principle. The hybrid 2/3L NPCI can be formed by addition of two half bridge modules to a two-level inverter. Therefore, the topology uses only ten active (self-commutating) switches compared to the conventional 3L NPCI which requires twelve active switches and six clamping diodes. Reduction in switching combinations lead to the elimination of the medium voltage vectors in the SVD of hybrid 2/3L NPCI. In order to address this issue, two types of voltage vector selection methods are proposed for hybrid 2/3L NPCI to closely approximate the reference vector. Effect of different switching state selections is studied in detail.
- The performance of Z-source integrated hybrid 2/3L NPCI is studied in detail. An advanced virtual vector modulation for hybrid 2/3L Z-source NPCI (Z-NPCI) is proposed. The modulation is designed in a manner to use both the small vectors for entire modulation index range. The new switching sequences at higher modulation range also retains minimum device commutations even with the insertion of shoot-through states.

- Un-balance in the DC-link is one of the potential issues in the Integration of renewable energy sources and hybrid energy storage systems. Therefore, the operation of hybrid 2/3L NPCI for unequal DC-sources is investigated thoroughly with the help of proposed modulation algorithm.
- MPCI topologies for higher voltage levels are studied in detail. A modified T-type topology is developed which can be easily extended to higher voltage levels by cascading two-level modules at the midpoint or top and bottom terminals.
- The modified T-Type MPCI topology is further investigated to reduce the active switch count. Such topologies are termed as reduced switching state (RSS) MPCI topologies due to the reduction in the available switching states in the SVD. The structure and device count of derived RSS MPCI topologies will decide the position of available voltage vectors in SVD. This approach is investigated on four and 5L RSS MPCI topologies in detailed with different possible structures. In addition, modulation strategies for such topologies are proposed.
- To validate the simulation studies of different MPCI topologies, downscaled experimental setup have been designed, constructed, and tested to verify the viability and effectiveness of the proposed modulation algorithms. Capacitor voltage balancing capabilities of the various modulations are also verified on 3L NPCI. Different hardware components as required for the operation of the experimental set-up such as pulse amplification, isolation circuit, dead-band circuit, voltage and current sensor circuits, and reactive loads have been fabricated in lab. The modulation algorithms of various MPCI topologies are implemented by using the RT-Lab real-time interface and MATLAB to generate desired signals for the active switches. These experimental studies are validated with simulation results at experimental parameters.

1.9 Organization of the Thesis

Apart from this chapter, the thesis contains seven more chapters and the work included in each chapter is briefly outlined as follows:

In CHAPTER 2, the modulation strategies for the multilevel inverter are reviewed and classified. A through survey of space vector modulation (SVM) techniques for MPCI is presented. Two types of SVM techniques namely nearest three vector (NTV) and non-nearest three vector (non-NTV) modulations for MPCI are explained in detail addressing capacitor voltage balancing in 3L neutral point clamped inverter (NPCI). Non-NTV modulations in the literature are compared in terms of voltage vector selection, complexity, switching frequency, etc. Modulation techniques MPCI topologies with higher voltage levels are reviewed addressing the capacitor voltage discharge phenomenon at higher modulation indices.

In CHAPTER 3, a new SVM algorithm is presented for implementing NTV and non-NTV modulations. The algorithm is based on equivalent 2L space vector diagram (SVD) formed by outermost voltage vectors in each sector region. The duty ratios of the NTV and non-NTV methods are derived in terms of duty ratios of equivalent 2L SVD. Generic relation among duty ratios of 2L SVD are also deduced to identify the various sub-triangle regions. Therefore, the algorithm requires only duty ratios of 2L SVD which does not require any coordinate transformation and trigonometry expressions. This results in reduced computational burden in implementation. The algorithm is explained in detail with the help of various MATLAB/Simulink simulation results on 3L NPCIs.

In CHAPTER 4, the modulation techniques are further investigated to improve overall performance of 3L NPCIs. Several NTV and non-NTV modulations combined to develop hybrid modulations which can minimize the shortcomings of NTV and non-NTV modulations. A redistribution-based algorithm is developed to implement the hybrid modulations using the NTV duty ratios. The performance of various hybrid modulations is compared with the help of MARLAB simulation results.

In CHAPTER 5, a new hybrid 2/3L NPCI is introduced as an alternative to 3L NPCI which can be implemented using only 10 self-commutating switches. The SVM techniques for the hybrid modulation are investigated and compared. The Z-source integrated hybrid 2/3L NPCI and is also investigated and an advanced virtual vector modulation is proposed. The operation of the VSI for un equal DC voltage sources is also investigated and a modulation method is proposed for suppression of the DC source voltage unbalance effect. The performance of various proposed modulations is validated with the help of MARLAB simulation results.

In CHAPTER 6, A modified T-type VSI is presented as an alternative 3L NPCI leg which can be realized with only two half bridge modules per phase leg. This topology is further extended to higher voltage levels by adding half bridge modules at top and bottom terminals or at the output stage. The generalized MPCI topologies are investigated further to reduce the number of active switches. Thereby developed reduced switching state (RSS) VSI topologies are also studied in detail with the help of 4L and 5L topology versions in order to draw some generalized conclusions.

The detailed discussions for the experimental set-ups have been given in CHAPTER 7. This includes the discussion on the power circuits, RT-Lab Realtime controller, the measuring system and the generation of gating signals for the inverter. The chapter concludes with experimental results and the corresponding discussion.

The main conclusions of the presented work and possible future research have been summarized in this CHAPTER 8.

In the end of thesis, the list of references and appendices regarding hardware implementations are provided.

Chapter 2: MODULATION STRATEGIES FOR MULTIPOINT CLAMPED INVERTERS

[In this chapter, modulation strategies of the MLIs are briefly reviewed. The space vector modulation (SVM) is selected due to the advantages over the other modulation strategies. The SVM based modulation strategies are classified as nearest three vector (NTV) and non-nearest three vector (non-NTV) strategies based on the nature of the selected voltage vectors for approximating the reference voltage vector. Various advanced non-NTV modulations in the literature are reviewed and their comparision is made. Some of the NTV and non-NTV modulation are simulated in detailed using 3L NPCI topology in MATLAB/Simulink and several limitations of these methods are summarised. If the number of voltage levels are more than three, MPCI topologies exhibit capacitor voltage unbalance when a passive frontend is used to power the DC-link. Therefore, the capacitor voltage balancing methods for higher level MPCI topologies are studied briefly.]

2.1 Introduction

Power electronic converters such as DC-DC converters, DC-AC converters, and matrix converters are used to power a wide range of applications in the distribution system. They have become an empowering technology with the increased penetration of distribution generation into the power grid. The rich diversity of applications requires VSIs with different power ratings, operating voltage/current levels, number of phases, semiconductor devices, switching frequency, output frequency, etc. A power converter must be associated with suitable control system for its operation. The basic power converter control is briefly explained in this section.

2.1.1 Principle of Voltage Source Converter Control:

Each power converter is associated with a controller and modulator depending on the application. A controller accepts desired parameter as input and generates the current or voltage reference signal for the power converte, as output. Modulator accepts current or voltage reference signal and generates the switching signals for power semiconductor switches. Depending on the process of generating reference signals, control systems associated with power converter systems are two types namely, 1) open loop control and 2) closed loop control. In an open loop control, a fixed reference signal is given independent of the measured output parameters and it is usually controlled by external factors other than the measured quantities. These control techniques are very simple. Examples: fans, pumps. In a closed loop control, a reference quantity is specified by the user, while the performance of the system is continuously monitored and compared with reference quantities and the error is processed to a controller which generates the reference voltage (or current) signals. The reference signals are processed

to a modulator for generating switching signals for the power switches. Example: Drives, Grid converters. Some closed-loop control systems associate with implicit modulator and are known as direct controllers. Example: Hysteresis control. Figure 2-1 shows block diagram of converter control system for DC-AC converter, commonly known as voltage source inverters (VSIs).

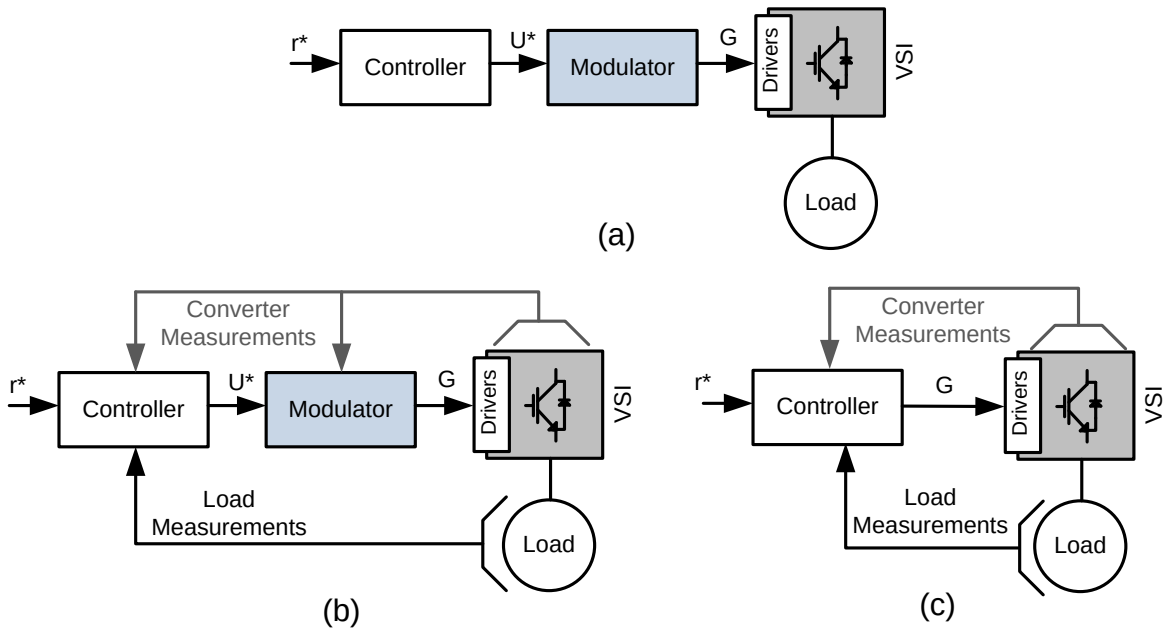


Figure 2-1 Block diagrams of inverter with different controllers. (a) Open loop operation. (b) Closed-loop operation using a controller and a modulator. (c) Closed-loop operation using a controller with implicit modulator.

2.1.2 Modulation Control of Power Converters:

The block that accepts an input reference signal and generates the switching signals for the power converter is called a modulator. Switching signals drive the active switches and produce a switched output current/voltage waveform where its fundamental frequency component in terms of magnitude and phase. The modulation strategies significantly depend on the topology used in the power conversion system.

For example, a two-level VSI is producing two output voltage levels as shown in Figure 2-2. Duration of application of these two states over a sampling period is controlled by an ON-state duty cycle of switches of the two-level VSI. This modulation is called pulse width modulation (PWM) and it is the widely used modulation strategy for VSIs to control the output voltage whose time average output is governed by a reference signal. Depending on the power converter topology, modulation technique should perform several additional tasks like capacitor voltage balancing, common mode voltage elimination unequal voltage compensation etc. Different types of modulation techniques are summarized in section 2.2.

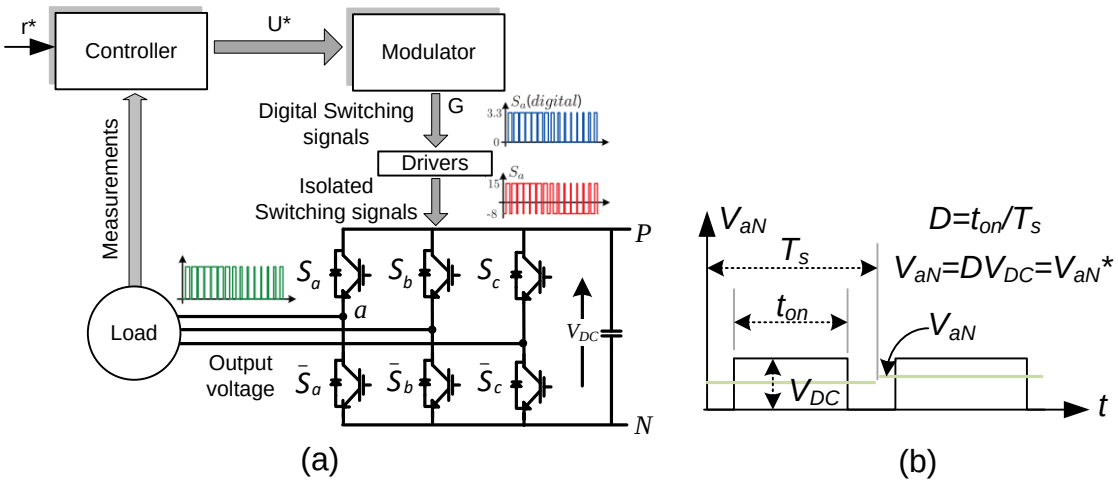


Figure 2-2 (a) Typical structure of control and modulation method for VSI. (b) Switched waveform and average value of the phase voltage V_{aN} .

2.2 Classification of Switching Signals Generation Schemes for MLIs

Figure 2-3 shows the generalized classification of switching signal generation methods [48]. For simplicity, the modulation strategies applicable for multilevel inverters are only focused in this section. These strategies can be applied to two-level with appropriate modifications.

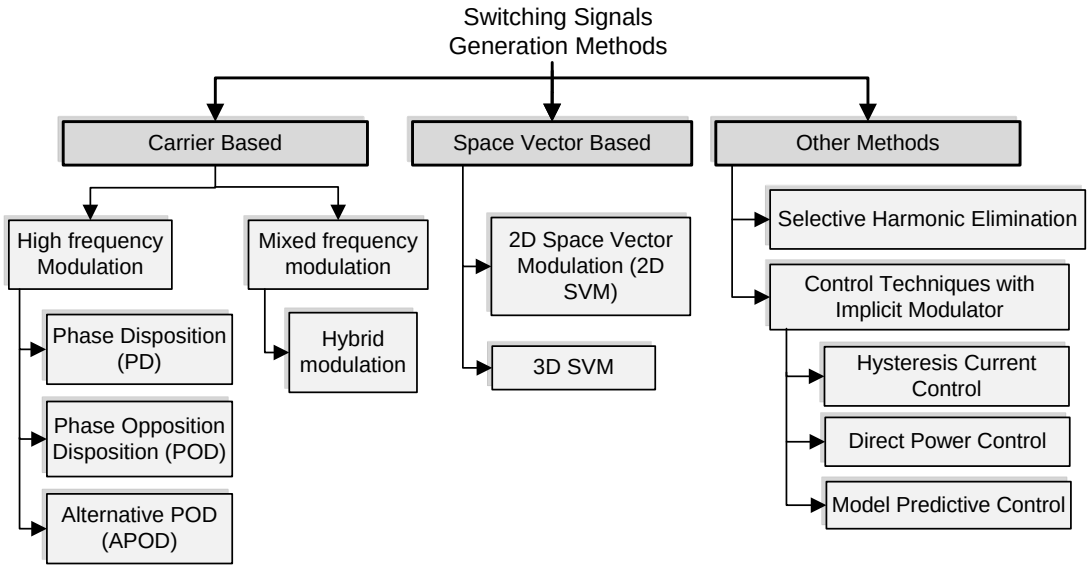


Figure 2-3 Classification of modulation techniques for gating signal generation [48].

2.2.1 Carrier Based PWM Strategies

It is the most popular modulation strategy for MLIs. It can generate the reference waveform with minimum distortion in the lower-order harmonics. In this modulation, the modulating signals (reference signals) are compared with high frequency carrier signals to generate high frequency

switching pulses for active switches of converter. The frequency of the carrier (f_{Cr}) is kept high for reducing the lower order harmonic content in the output. The ratio of the frequencies of carrier wave with the reference wave is called the frequency modulation index (m_f) (2.1). If m_f is an integer, the modulation is called symmetric modulation, otherwise it is called asymmetric modulation. In harmonic spectrum of the PWM waveform, the distortion has moved to the harmonic orders around m_f .

$$m_f = \frac{f_{Cr}}{f} \tag{2.1}$$

The maximum amplitude of the output fundamental voltage can be easily changed using the modulation index (m) (2.2) of the modulating signal. Where V_m and V_r are the peak values of the modulating and carrier signals, respectively. However, the value of m is limited to 1 to avoid the generation of lower-order harmonics.

$$m = \frac{V_m}{V_r} \tag{2.2}$$

The number of carrier signals required for an MLI is given by $(m-1)$, where, $m =$ number of voltage levels. Depending on the distribution of carrier signals, the carrier-based modulation methods for multilevel inverters can be generally classified into two categories: (1) Phase-shifted and (2) Level-shifted PWM methods (LS-PWM) [49]. Phase Shifted PWM (PS-PWM) methods are commonly used for CHBIs for equal power and loss distribution. This concept can be applied to any modular inverter formed by series connection of similar cells. Figure 2-4 show the example of PS-PWM for seven-level CHBI.

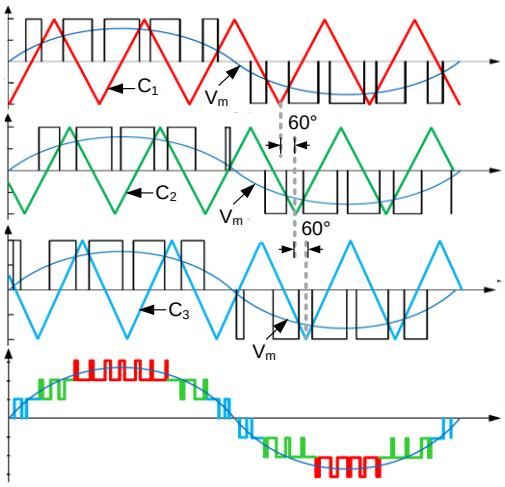


Figure 2-4 PS-PWM for 7-level CHBI.

LS-PWM method is suitable for both CHB and MPCI structured topologies discussed in Chapter 1. These are also called phase disposition (PD) methods. There are several types of PD methods, namely, (1) alternative phase opposition disposition (APOD), where each carrier is phase shifted by 180 from its adjacent carrier; (2) phase opposition disposition (POD), where carriers above the sinusoidal reference zero point are 180 out of phase with those below the zero point; (3) phase disposition (PD), where all carriers are in phase. Figure 2-5 shows different type of of LS-PWMs for 5L CHBI.

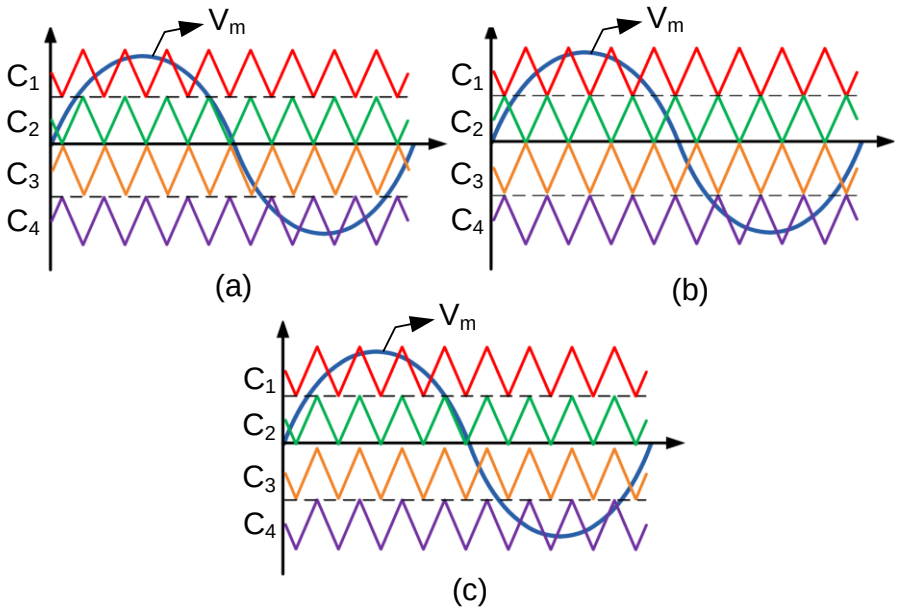


Figure 2-5 LS-PWM methods for 5L VSI: (a) POD, (b) APOD and (C) PD.

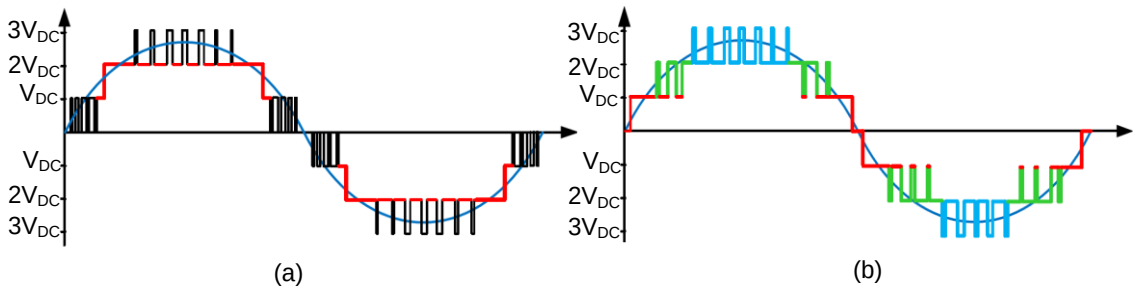


Figure 2-6 Example of output voltages for hybrid carrier-based modulations.

Due to inherent drawback of LS-PWM techniques, the power loss equalization among the switches is not possible. Therefore, they are not preferred for modulating the CHBIs. Some advanced LS-PWM methods [50] are also proposed to equalize the power distribution and power losses by interleaving the gating signals associated with the carrier waves. In case of MPCI structured topologies, each carrier is associated with a pair of switches in the phase leg of the inverter to control the corresponding level of the output voltage.

Hybrid modulations are developed in the literature [51] for some of the advanced Multilevel inverters to improve the power loss distribution and capacitor voltage balancing. For example, active neutral point clamped inverters are modulated with square-wave modulation for higher voltage power devices and a modified PS-PWM methods for balancing DC-link capacitor voltages. Figure 2-6 show the output voltage waveforms with the multiple frequency carrier-based hybrid modulation.

2.2.2 Space Vector Modulation (SVM)

It is basically a PWM method implemented in the $\alpha-\beta$ reference frame for inverter switching signal generation. All the switching states of the VSI are mapped into discrete points in $\alpha-\beta$ frame and represented as voltage vectors. The reference signals are also converted into the $\alpha-\beta$ reference to form a continuously rotating reference vector [52]–[54]. Therefore, the modulation problem is turned into a geometrical mathematical problem to find the best set of voltage vectors and corresponding duty ratios in order to closely synthesizing the reference voltage vector. The rotating reference vector is sampled at a fixed rate called sampling period (T_S) to obtain the average reference vector (V_{ref}). Depending on the position of V_{ref}, nearest voltage vectors are identified. The duration of selection of each of these voltage vectors is determined by the volt-second balance equation (2.3).

$$\left.\begin{aligned} V_1 d_1 + V_2 d_2 + V_3 d_3 &= V_{ref} \\ d_1 + d_2 + d_3 &= 1 \end{aligned}\right\} \tag{2.3}$$

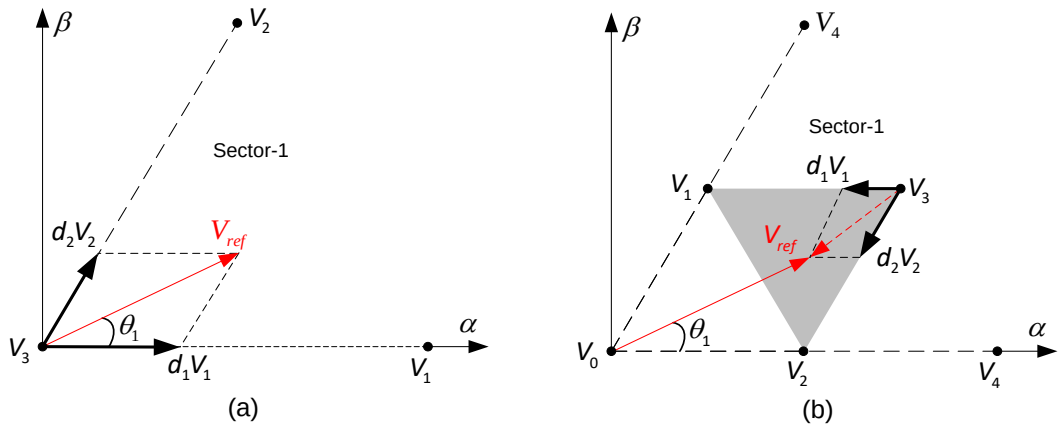


Figure 2-7 Voltage-second balance princple for V_{ref} in (a) 2L SVD and (b) 3L SVD.

Here, V_i is a voltage vector, d_i is duty ratio of the voltage vector V_i. V_{ref} is the averaged reference vector. The voltage vectors and corresponding duty ratios are converted into switching pulses following a predefined order know as switching sequence. Figure 2-7 shows

the space vector diagram (SVD) of the two-level (2L) and 3L inverters when V_{ref} is located in sector-1.

2.2.3 Other Methods

2.2.3.1 Selective Harmonic Elimination (SHE):

Selective Harmonic Elimination (SHE) is not a conventional time-based modulation strategy, such as classic PWM or SVM, but, focused on the output harmonic spectrum of the VSI. SHE is generally used for high power applications to minimise the power losses [55]. The modulation produces desired output voltage with very low switching frequency. Very few switching instants (angles) are allowed within the fundamental cycle for eliminating the low frequency harmonic content in the output voltage. Switching angles are calculated offline and stored in a lookup table by solving system of nonlinear equations for a given modulation index and set of harmonic components to be eliminated. The number of commutations determine the number of harmonics to be eliminated. If the modulation index changes, the angles need to be calculated again. Recently, the researchers have developed real-time algorithms based on artificial intelligence to calculate the switching angles [56].

2.2.3.2 *Control Techniques with Implicit Modulator*

These methods are closed-loop control methods that directly generate the gate signals for the inverter. In this case, these gate signals are not necessarily to follow a reference voltage but is determined to directly reduce the error of the controller goal and, therefore, cannot be considered as modulation strategies. These techniques achieve good results usually at the expense of having a nonconstant switching frequency leading to widespread harmonic spectra.

Hysteresis Current Control: It generates the switching signals to keep the phase currents inside a predefined hysteresis band. This control technique is the simplest implementation of a closed-loop control and has been extensively used in industrial products.

Direct power control: It is widely used for grid-connected applications to control active and reactive power [57].

Finite state Model predictive control (FS-MPC): In this method, controller uses the model of the system to predict the behavior of output voltage when each possible inverter switching state is applied. A pre-defined cost function is the criterion for selecting the switching state that will be applied during the next sampling interval [58]. The cost function usually has multiple objective variables such as phase current, capacitor voltage error, Power loss, etc.

2.3 SVM Strategies for MPCIs

SVM is a widely used pulse width modulation (PWM) method for VSIs due to high DC-voltage utilization and digital implementation friendly nature. In this section, some key SVM strategies of MPCI topologies are studied. This study emphasizes on the selection of voltage vectors for synthesizing the reference voltage vector (V_{ref}).

2.3.1 Three Level (3L) NPCI Topology and Its Space Vector Diagram (SVD)

NPCI is the basic structure of the MPCI family and it has the single intermediate clamping point known as neutral point (NP). Figure 2-8 (a) shows the NPCI operating with single DC source V_{DC}. Taking point 'O' as reference, the output voltage in each phase V_{xo} ($x \in a,b,c$) of the inverter are listed in Table 2-1. Switches $S_{xi}(i \in 1,2)$ are controlled by binary values, where 0 and 1 correspond to OFF and ON states. Switches S_{xi} and $\bar{S}_{xi}$ are complementary in nature (i.e., $S_{xi} + \bar{S}_{xi} = 1$). The aim of the modulation is to synthesize phase voltages given by

$$\begin{aligned} v_a &= V_m \cos(\omega t) \\ v_b &= V_m \cos(\omega t - 2\pi/3) \\ v_c &= V_m \cos(\omega t - 4\pi/3) \end{aligned} \tag{2.4}$$

Here, V_m is the peak value of the reference phase voltage. (2.4) can be represented as a space vector

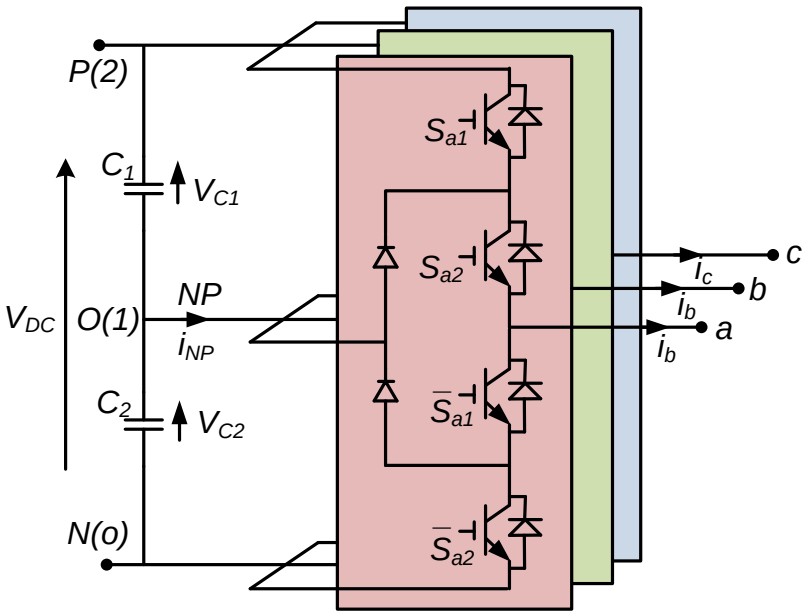
$$V_{ref} = \frac{2}{3}.(v_a + v_b.e^{j2\pi/3} + v_c.e^{j4\pi/3}) \tag{2.5}$$

The output ac terminal $x,(x = a,b,c)$ can be connected to any of the three DC side terminals N, O and P denoted as 0, 1 and 2 respectively. A total of 3^3=27 switching states can be generated by different combinations of gating signals for three phase 3L NPCI. These switching states are transformed to *α-β* reference frame to form 19 voltage vectors. Voltage vectors are used to synthesize the reference voltage vector (V_{ref}) (2.5) mapped in *α-β* reference frame. Figure 2-8 (b) shows the space vector diagram (SVD) of NPCI containing 27 switching states and V_{ref}. The SVD has the six-fold symmetry and each segment is called sector. Each sector is of arch angle of 60°. Depending on the length of the voltage vectors they are classified as small, medium and large voltage vectors. For the convenience, the reference vector in (2.5) is normalized as follows

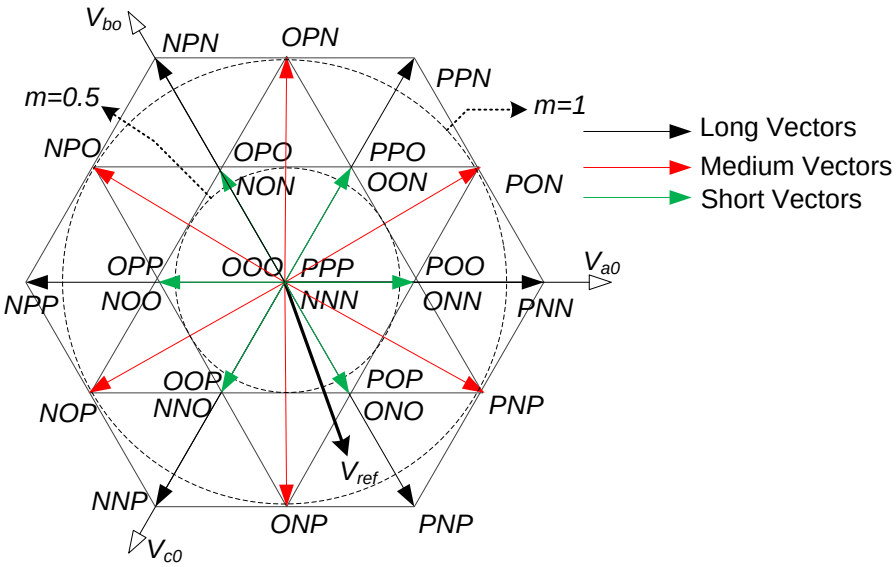
$$V_{ref} = V_m.e^{j\omega t} = m\frac{V_{dc}}{\sqrt{3}}e^{j\omega t} \tag{2.6}$$

Here, m is called modulation index, given by

$$m = \sqrt{3}\frac{V_m}{V_{dc}} \in [0,1] \tag{2.7}.$$



(a)



(b)

Figure 2-8 Three-level (3L) NPCI (b) SVD of 3L NPCI.

Table 2-1 Switching states of NPCI with notation ($x=a,b,c$)

S_{x1}	S_{x2}	$\bar{S}_{x1}$	$\bar{S}_{x2}$	V_{xo}	Notation
1	1	0	0	$V_{C1}(V_{DC}/2)$	$P(2)$
0	1	1	0	0	$O(1)$
0	0	1	1	$-V_{C2}(-V_{DC}/2)$	$N(0)$

The trajectory of the reference vector for different values of modulation index (m) are also depicted in Figure 2-8. Only the case $m \leq 1$ (linear modulation) referring the first sector is analyzed in this chapter.

The reference vector V_{ref} is synthesized using a set of voltage vectors satisfying the volt-sec balance equation (2.3). Depending on the selection of voltage vectors $V_i (\mathrm{i} = 1,2,3)$, several types of modulations are possible. In this regard, SVM strategies for MPCI are broadly classified into two types, namely

1. Nearest three vector (NTV) methods and
2. Non-nearest three vector (non-NTV) methods

NTV methods use three voltage vectors closest to the reference vector V_{ref} and produces the minimum voltage THD. There are several variants in NTV selection based on the utilization of redundant switching states to achieve switching losses minimisation, capacitor voltage balancing control, etc. On the other hand, non-NTV methods utilize the voltage vectors which may or may not be the nearest vectors in order to synthesize V_{ref}. These techniques usually increase the switching frequency, output dv/dt and THD. However, they exhibit specific advantages depending on topology and other output characteristics.

2.3.2 NTV Strategy for 3L NPCI

The nearest-three-vector (NTV) modulation strategies are widely used for multilevel inverters. Depending on the redundant vector selection, an NTV strategy uses either three switching states or four switching states (symmetric modulation) [59][60] to synthesize V_{ref}. Closed loop NTV based control schemes often uses capacitor voltage error [61][62] or, current through NP [63][64] as a feedback signal to modify switching sequence [65], redundant states or reference vector [66] for NP voltage control.

Figure 2-9 shows first sector of 3L NPCI space vector diagram. Four sub-triangle regions within a sector are numbered as $T_0 - T_3$. All the voltage vectors and V_{ref} are normalised based on (2.6) and (2.7). For the given instant of V_{ref}, the nearest three vectors can be identified with the help of sub-triangle region. For example, from Figure 2-9, V_{ref} is located in sub-triangle region T_1 which is mathematically found by

$$m\left(\sqrt{3}\cos\theta_1 - \sin\theta_1\right) > 1 \tag{2.8}$$

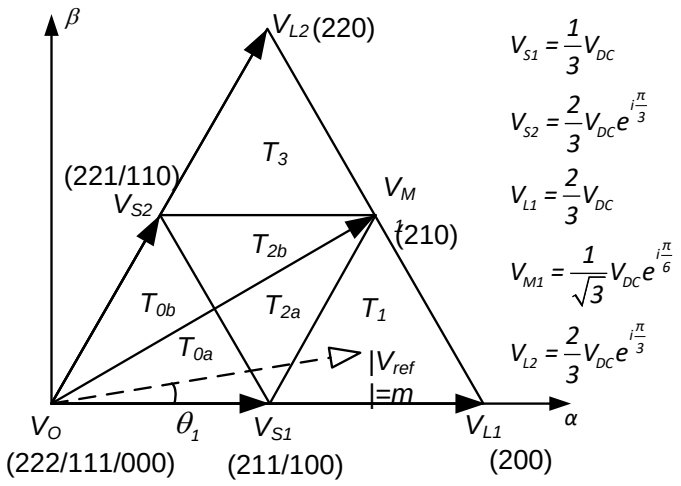


Figure 2-9 Sector-1 of 3L NPCI SVD divided into NTV sub-triangle regions.

Therefore, if (2.8) is satisfied, the nearest vectors of V_{ref} are V_{S1}, V_{M1} *and* V_{L1}. Now, the next step is to calculate the duty ratios of the voltage vectors using the voltage-second balance equation given bellow.

$$\begin{aligned} &d_{S1}V_{S1} + d_{L1}V_{L1} + d_{M1}V_{M1} = V_{ref} \\ &d_{S1} + d_{L1} + d_{M1} = 1 \end{aligned} \tag{2.9}$$

Substituting the voltage vectors expressions, (2.9) become

$$\begin{aligned} &d_{S1}\frac{1}{3}V_{DC} + d_{L1}\frac{2}{3}V_{DC} + d_{M1}\frac{1}{\sqrt{3}}V_{DC}e^{i\frac{\pi}{6}} = V_{ref} = V_m e^{i\theta_1} \\ &d_{S1} + d_{L1} + d_{M1} = 1 \end{aligned} \tag{2.10}$$

Substituting $e^{j\theta} = \cos\theta + j\sin\theta$ in (2.10) and simplifying,

$$\begin{aligned} &d_{S1}\frac{1}{3}V_{DC} + d_{L1}\frac{2}{3}V_{DC} + d_{M1}\frac{1}{\sqrt{3}}V_{DC}\cos\frac{\pi}{6} = V_m\cos\theta_1 \\ &d_{M1}\frac{1}{\sqrt{3}}V_{DC}\sin\frac{\pi}{6} = V_m\sin\theta_1 \\ &d_{S1} + d_{L1} + d_{M1} = 1 \end{aligned} \tag{2.11}$$

Finally, the duty ratios are given by

$$\begin{aligned} d_{S1} &= 2 - \left\{\frac{\sqrt{3}V_m}{V_{DC}}\right\}(\sqrt{3}\cos\theta_1 + \sin\theta_1) \\ d_{M1} &= 2\left\{\frac{\sqrt{3}V_m}{V_{DC}}\right\}\sin\theta_1 \\ d_{L1} &= -1 + \left\{\frac{\sqrt{3}V_m}{V_{DC}}\right\}(\sqrt{3}\cos\theta_1 - \sin\theta_1) \end{aligned} \tag{2.12}$$

From (2.7), the duty ratios expressions are simplified as follows

$$\begin{aligned} d_{S1} &= 2 - m(\sqrt{3}\cos\theta_1 + \sin\theta_1) \\ d_{M1} &= 2m\sin\theta_1 \\ d_{L1} &= -1 + m(\sqrt{3}\cos\theta_1 - \sin\theta_1) \end{aligned} \tag{2.13}$$

A NTV switching sequences using four switching states of the sub-triangle region T_1 is show in Figure 2-10.

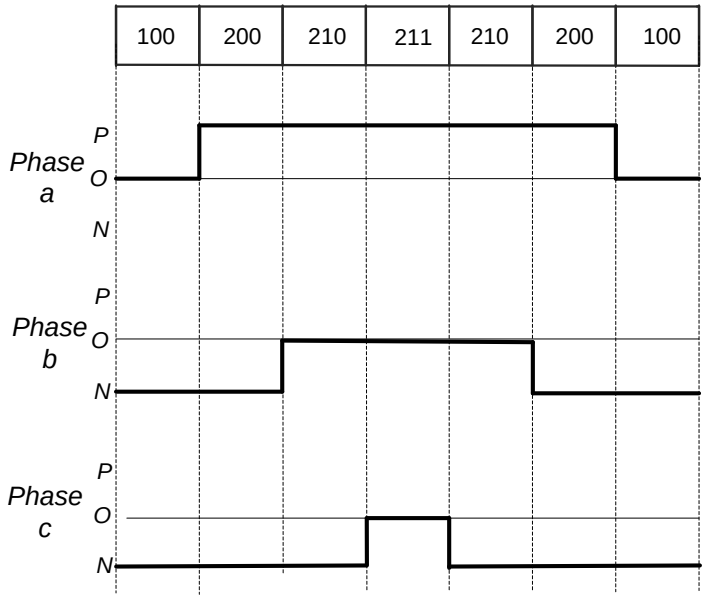


Figure 2-10 Switching sequence for NTV modulation when V_{ref} is located in T_1 .

The duty ratios of voltage vectors to synthesize V_{ref} located in different sub-triangle regions are different. Similar procedure discussed above can be followed to find the duty ratios of voltage vectors for V_{ref} located in remaining triangles. For example, if V_{ref} located in sub-triangle T_2, the duty ratios are given by

$$\begin{aligned} d_{S1} &= 1 - 2.m.\sin\theta_1 \\ d_{S2} &= 1 + m(-\sqrt{3}\cos\theta_1 + \sin\theta_1) \\ d_{M1} &= -1 + m(\sqrt{3}\cos\theta_1 + \sin\theta_1) \end{aligned} \tag{2.14}$$

2.3.2.1 Simplified SVM Algorithms for NTV Modulation:

The implementation of SVM strategy as discussed above, involves coordinate transformation and trigonometric expressions. Therefore, as the number of levels, the complexity of this approach increases. Fortunately, the sub-triangle regions of all NTV strategies are identical and form equilateral triangles in SVD. Due to this symmetry, some advanced simplified modulation algorithms [53], [54], [67], [68] are reported in the literature to reduce the computational burden.

SVM algorithms based on 60° non-orthogonal systems [69][70] and without coordinate transformation [71][72] [73] are efficient for calculation of duty ratios of voltage vectors in case of NTV methods.

2.3.2.2 Low Frequency NP Voltage Oscillations with NTV Modulation:

Usually, a single DC source is connected between terminals *P* and *N* of NPCI (referrer Figure 2-8 (a)) to avoid extra cost owing to additional isolated DC sources. As a result, a floating neutral point (NP) (O) is created and leads to unbalance in the capacitor voltages during the NPCI operation. This must be addressed using a proper modulation method.

NTV based strategies are known to produce low frequency capacitor voltage oscillations at higher modulation index and low power factors due to the increased participation of medium voltage vector (Example: STATCOM, Battery charging applications) [59][74][75]. This voltage oscillations increase low frequency harmonic content (along with even order harmonics due to unequal capacitor voltages) in the output voltage and current [76] and also impose overvoltage stress on the devices. Typically, oversized DC link capacitors are required to suppress this oscillations [59], [77] which increases the cost and decreases the lifetime. Moreover, systems with fast dynamics, such as electric vehicles, cannot rely on the NTV methods alone [39].

2.3.3 Non-NTV Modulation for 3L NPCI

Several non-NTV modulation schemes of 3L NPCI are reported in the literature. The Non-NTV methods as the name implies, use the voltage vectors which are not the nearest three vectors. Non-NTV methods [78]–[81] Capacitor voltage balancing for all m and power factors. Some of the advanced non-NTV methods like selected three vector modulation [79][82], Nearest three virtual vector modulation [83] is proposed to eliminate the low frequency ripples completely in the NP voltage for all loading conditions. Methods [84][85] are some more non-NTV based methods, recently reported which are capable of maintaining NP voltage balance rapidly. [86] is another non-NTV method for reducing capacitor RMS current. Advantages of non-NTV methods are:

i) Complete elimination of low frequency NP voltage ripple.
ii) Use of small DC link capacitors to reduce the overall size.
iii) Can exhibit exceptional dynamic performance in the fast load changing scenarios.

Notably, all the non-NTV methods are inferior in terms of output (voltage and current) distortion and switching frequency when compared to NTV methods.

2.3.3.1 Nearest Three Virtual Vector (NTVV) Modulation

The nearest three virtual vector (NTVV) is proposed in [66] to keep the neutral-point voltage balanced for full range of inverter output voltage and for all load power factors. A set of voltage vectors know as virtual vectors are used for approximating V_{ref} . A virtual vector is defined as a combination of voltage vectors such that, the average NP current is maintained zero in each switching cycle. Figure 2-11 shows all the virtual vectors in the first sector of 3L NPCI SVD. The combinations of actual voltage vectors for these virtual vectors are listed in Table 2-2.

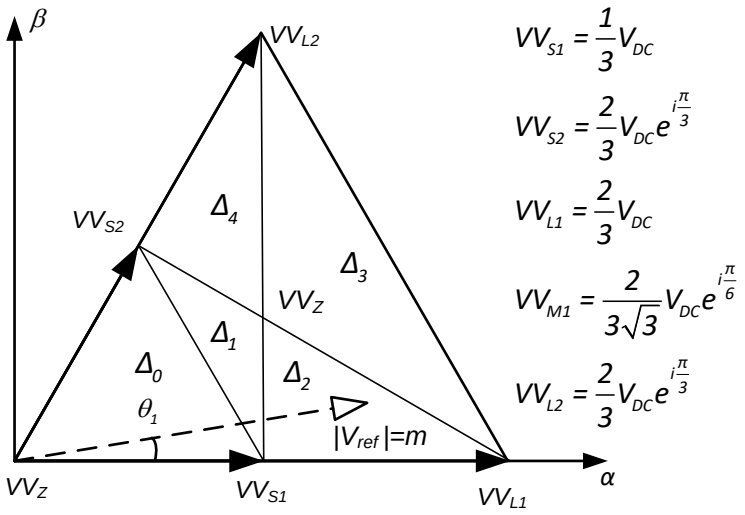


Figure 2-11 Sector 1 of 3L NPCI SVD divided into NTVV sub-triangle regions.

Table 2-2 Virtual vectors in sector-1 of 3L NPCI SVD

Virtual vector	Switching states combination	Resultant NP current
VV_Z	V_{000} / V_{111} / V_{222}	No NP current (0)
VV_{S1}	$\frac{1}{2}(V_{100}+V_{211})$	$\frac{1}{2}(i_a+(-i_a))=0$
VV_{S2}	$\frac{1}{2}(V_{110}+V_{221})$	$\frac{1}{2}((-i_c)+i_c)=0$
VV_{M1}	$\frac{1}{3}(V_{100}+V_{210}+V_{221})$	$\frac{1}{2}(i_a+i_b+i_c)=0$
VV_{L1}	V_{200}	No NP current (0)
VV_{L2}	V_{220}	No NP current (0)

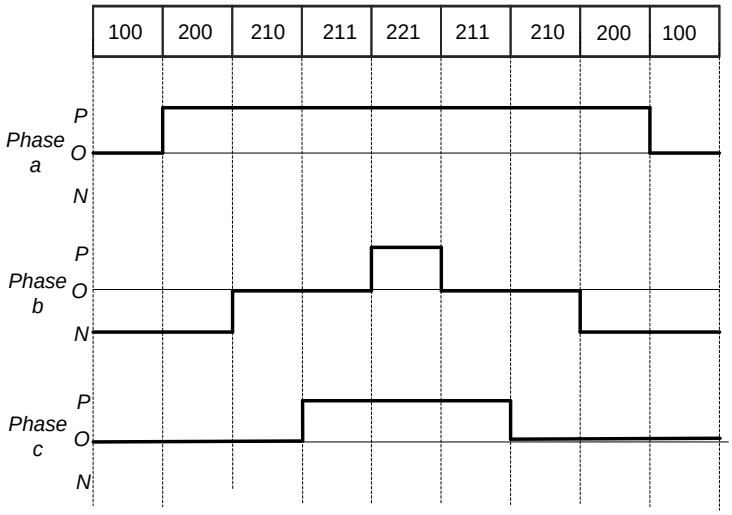


Figure 2-12 Switching sequence for non-NTV modulation when V_{ref} is located in Δ_2 .

Virtual vectors are joined to form five sub-triangle regions Δ_0 - Δ_4 . For example, if V_{ref} is located in triangle Δ_2, voltage vectors: $VV_{S1}, VV_{L1}, VV_{M1}$ become nearest vectors. Therefore, from Table 2-2, the switching sequence is given by: $V_{100} \rightarrow V_{200} \rightarrow V_{210} \rightarrow V_{211} \rightarrow V_{221}$. using the actual voltage vectors. It is designed to allow only one commutation per transition as shown in Figure 2-12. The voltage-second balance equation for the given location of V_{ref} is written as

$$\begin{aligned} &d_1 VV_{S1} + d_2 VV_{L1} + d_3 VV_{M1} = V_{ref} \\ &d_1 + d_2 + d_3 = 1 \end{aligned} \tag{2.15}$$

Substituting the virtual vector expressions from Table 2-2.,

$$\begin{aligned} &d_1\left(\frac{V_{100}+V_{211}}{2}\right) + d_2 V_{200} + d_3\left(\frac{V_{100}+V_{210}+V_{221}}{3}\right) = V_{ref} \\ &\qquad\qquad or \\ &V_{100}\left(\frac{d_1}{2}+\frac{d_3}{3}\right) + V_{211}\left(\frac{d_1}{2}\right) + V_{210}\left(\frac{d_3}{3}\right) + V_{221}\left(\frac{d_3}{3}\right) + d_2 V_{200} = V_{ref} \end{aligned} \tag{2.16}$$

After simplification, the duty ratios of switching states when V_{ref} is located in sub-triangle are given by

$$\begin{aligned} d_{100} &= 1 - \frac{\sqrt{3}}{2} m\cos\theta_1 - \frac{1}{2} m\sin\theta_1 \\ d_{211} &= 1 - \frac{\sqrt{3}}{2} m\cos\theta_1 - \frac{3}{2} m\sin\theta_1 \\ d_{210} &= d_{221} = m\sin\theta_1 \\ d_{200} &= V_{ref} \end{aligned} \tag{2.17}$$

Similar procedure discussed above can be followed to find the duty ratios of voltage vectors for V_{ref} located in remaining triangles.

Unlike the NTV strategies, sub-triangle regions are not identical in NTVV, this is the case with other non-NTV strategies as well. As a result, the simplification algorithms reviewed in section 2.3.2 are not suitable for the non-NTV strategies. NTVV method can also be implemented using a carrier-based method by evaluating phase duty ratios: $d_{xP}, d_{xO}, d_{xN}\ (x = a,b,c)$ as discussed in chapter 2. However, duty ratios of redundant switching states cannot be controlled depending on the NP voltage unbalance. Moreover, this method requires complex offline calculations for a change in the switching sequence. For example, a variant of VV modulation is proposed in [80], in which, the share of redundant switching states are completely different. The approach presented in this paper is very simple in such cases and does not require extra steps. Some of the existing non-NTV methods are compared in TABLE 2-3.

TABLE 2-3 Comparison of non-NTV methods

Modulation method	**Selection of vectors**	**Complexity**	**Remarks**
Gupta, A.K. [79] and Bharatiraja, C. [82]	STV method: Two small vectors and one large vector or two large vectors and one small vectors are selected. Medium vector is completely avoided.	High	• Four sets of voltage-second balance equations are required for STV. • Increases output THD, *dv/dt* and switching frequency (better compared to [78]). • Coordinate transformation and reference vector angle estimation is required.
Busquets-Monge, S. [78]	Three nearest virtual vectors (VV) are selected. 5 switching states are required to synthesize V_{ref} for most of the duration. Equivalent phase duty ratios (PDRs) are used to reduce the complexity.	Medium	• Three PDRs /phase are required. • 5 switching states are used to synthesize V_{ref}. • Increases the switching frequency output THD, (higher than STV [79]). • Requires sum of three phase currents equal to zero ($i_a+i_b+i_c=0$). • The duty ratios of redundant switching states cannot be changed.

Choudhury, A. [83]	Vector selection is similar to [78]. Active control over the duty ratios of redundant switching states is achieved, which is not possible in [78].	High	• Identification of sub-triangle region requires extra computations (β_1 and β_2). • Calculation duty ratio of switching states is more complex and requires trigonometric expressions.
Choi, U.M. [84]	The small vector and/or medium resulting in NP voltage deviation are/is replaced with the zero vector and large vector / zero vector which doesn't affect the NP balance. Implemented using carrier based PWM approach.	Less	• Operation is similar to two level modulation when the NP voltage deviation is detected. • Increases the switching frequency, output THD. (maximum and comparable to two level inverter)
Choudhury, A. [85]	Two long vectors and one of the redundant small vectors is selected depending on the NP voltage deviation. Medium vector is completely avoided.	Medium	• Not suitable for low and medium modulation indices. • Unequal no. of commutations for the conditions $V_{C1} > V_{C2}$ and $V_{C1} < V_{C2}$. • Increased switching frequency and output THD (better [79] for high modulation index).

2.4 Performance Evaluation of 3L NPCI

The performance of NPCI was investigated in MATLAB-Simulink using following parameters: DC link voltage=600 V, switching frequency=2 kHz and DC link capacitors =550µF and RL load=4+jπ/2 Ω. Figure 2-13 through Figure 2-15 show the simulation results for the aforementioned modulation schemes NTV and NTVV at two modulation indices m=0.35 and m=0.95. The duty ratios of the redundant switching states are distributed to achieve zero averaged NP current. From Figure 2-13, it is observed that the NTV strategy is capable of eliminating capacitor voltage oscillations for lower modulation index m=035. However, if the modulation index is increased to m=0.95, oscillations appear in the capacitator voltages. The magnitude of this oscillations depend on the rating of the capacitor and the line currents. The line-to-line voltage (V_{ab}) and pole voltages (V_{aO}) are PWM waveforms with discreate adjacent voltage levels.

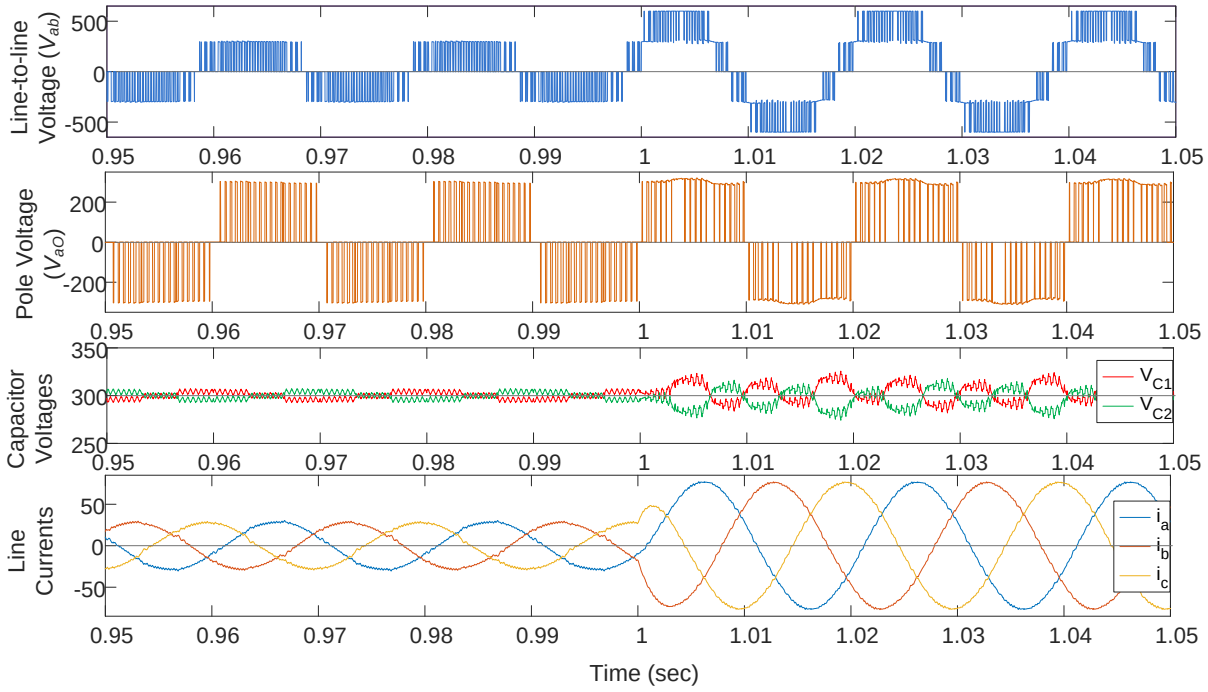


Figure 2-13 NTV strategy simulation for m=0.35 (from t=0.95 to t=1 sec) and m=0.95 (after t=1 sec).

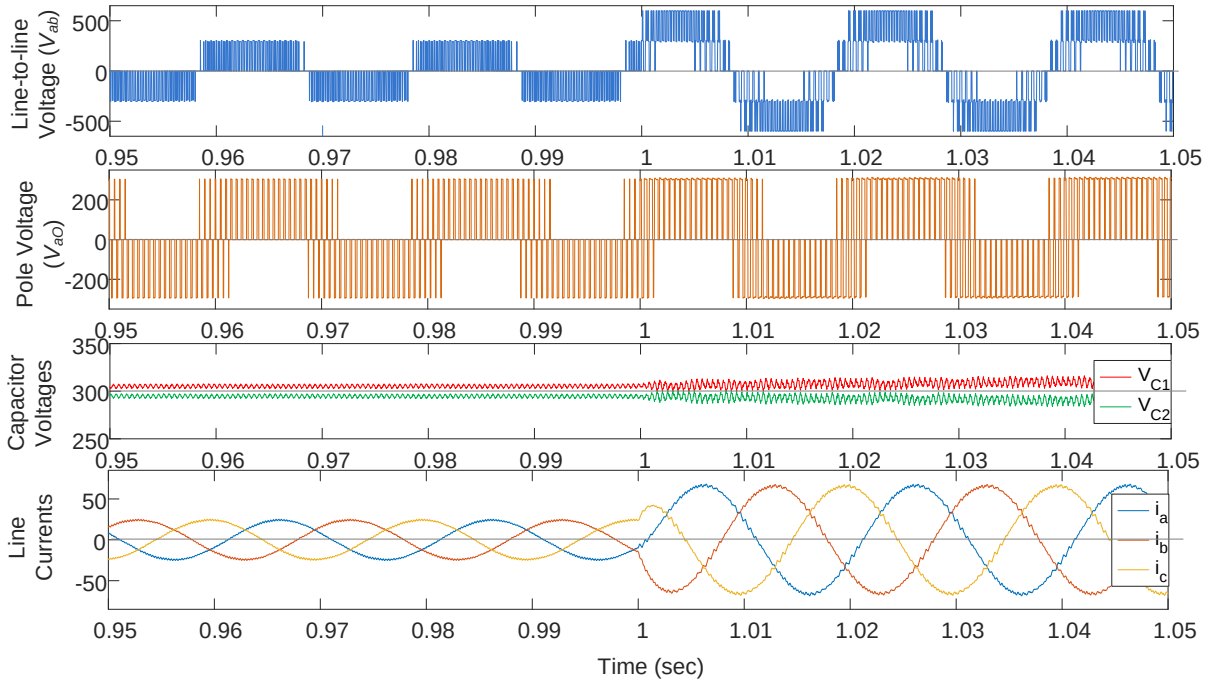


Figure 2-14 NTVV strategy simulation for m=0.35 (from t=0.95 to t=1 sec) and m=0.95 (after t=1 sec).

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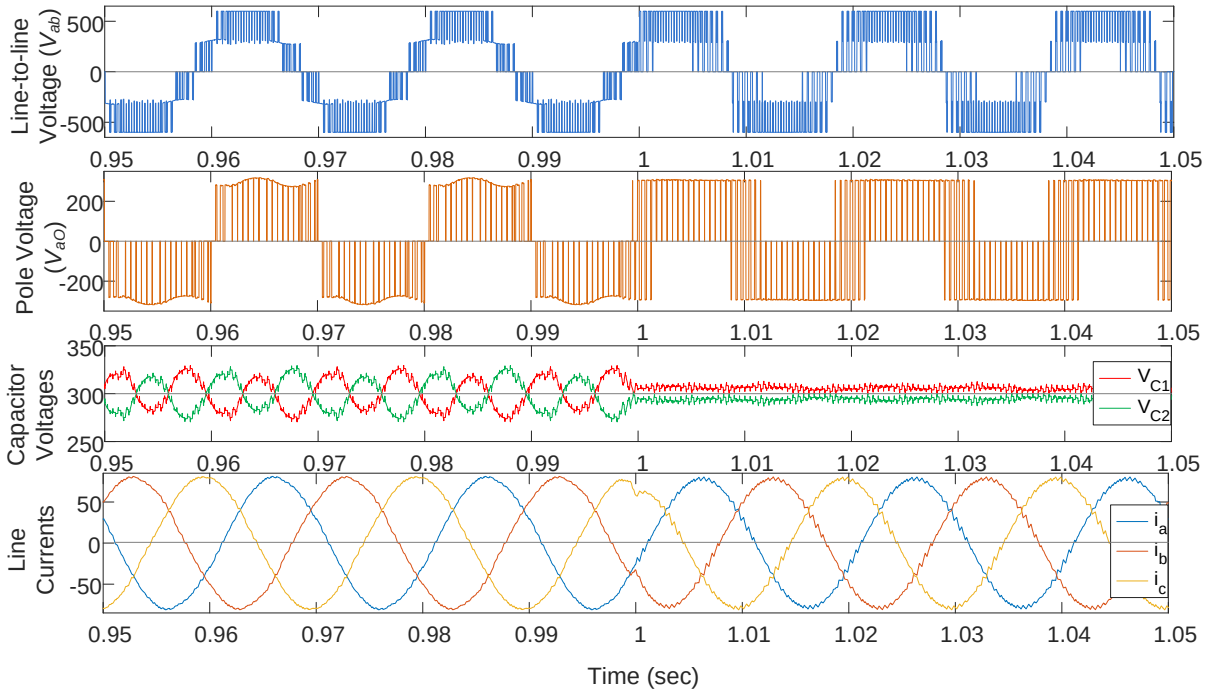


Figure 2-15 Comparison of NTV (from t=0.95 to t=1 sec) and NTVV (after t=1sec) strategies at m=0.98 and RL load=4+jπ/2 Ω.

Figure 2-14 show the simulation results of NTVV strategy. Unlike the NTV modulation, a reduced ripple is observed in the capacitor voltages for the given load at both the modulation indices m=0.35 and m=0.95. It is also observed that, the adjacent voltage levels are not discrete in NTVV strategy. Figure 2-15 shows comparison of NTV and NTVV for same operating conditions. It is clearly evident that, capacitor voltages are effectively maintained by NTVV as compared to NTV scheme which is producing a large third harmonic ripple in pole voltage and capacitor voltages as the reactive component of load increases,

Since the NTVV strategy inherently maintains zero average NP current for each switching cycle, and hence, any existing unbalance in capacitor voltages. This can be observed in the capacitor voltage waveforms of NTVV strategy (refer Figure 2-14). A non-zero NP current must be injected by appropriate selection of small vector redundancy for voltage balancing action to be taken place. For example, in [83], a NTVV-based scheme where in, only one redundant vector is used in each switching cycle depending on the processed voltage error.

2.5 Capacitor voltage balancing for Multilevel MPCI

It has long been recognized by studies that for the diode-clamped inverter with more than three levels, a passive front-end capacitor voltage balancing method is only achievable if the modulation index is limited to about 60% of its maximum value for loads with a typical 0.8 power factor[87][88][89]. If the modulation index is increased more than this value, center capacitors gradually discharge, and finally, the inverter output converges at three levels. The limits for

balanced capacitor voltage operation of high-order multilevel diode-clamped inverters with passive front-ends are defined in [90]. In the case of a single-phase linear load with impedance angle connected in between two inverter legs, the region for balanced operation is defined by

$$m < \frac{2}{\pi\left|\cos(\varphi)\right|} = \frac{0.637}{\left|\cos(\varphi)\right|} \tag{2.18}$$

In the case of a three-phase linear load with phase impedance angle, the region for balanced operation is defined by

$$m < \frac{\sqrt{3}}{\pi\left|\cos(\varphi)\right|} = \frac{0.551}{\left|\cos(\varphi)\right|} \tag{2.19}$$

Where, $m =$ modulation index; φ is power factor angle.

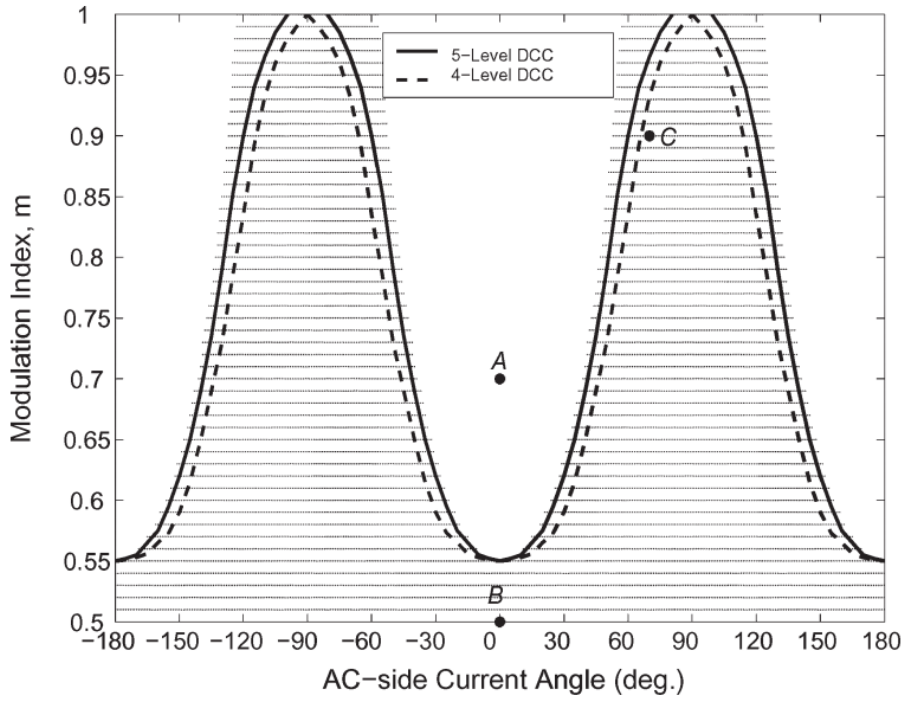


Figure 2-16 Limits of voltage balance of the NTV-SVM-based balancing methods for a 4- and 5L passive front-end DCI [89]. (A) Operating point corresponding to PF = 1 and m = 0 .7 (unstable operation). (B) Operating point corresponding to PF = 1 and m = 0 .5 (stable, line to line voltage with 5 levels). (C) Operating point corresponding to PF = 0.35 and m = 0 .9 (stable, line to line voltage with 9 levels).

Figure 2-16 shows limiting conditions of voltage balance of the NTV-SVM-based balancing methods. It is to be noted that above limits are valid for NTV based SVM scheme in which all the available voltage levels are used in the synthesis of output voltages. Consequently, good output line-to-line voltage spectra are obtained. These studies conclude that for high modulation

indices ($m = V_{L-L1}/V_{dc}$, where $V_{L-L1}$is the peak value of the fundamental component of the line-to-line output voltage; $m \in [0,1]$for linear modulation) the balancing is not possible unless additional hardware is used, especially as the number of levels increases.

Numerous voltage balancing schemes have been suggested to address dc-link imbalance problem for DCI. These can be mainly categorized into two types: 1) hardware: auxiliary circuits on the dc side with specific balancing control strategies and 2) software specific: pulse width modulation (PWM) pattern with voltage balancing control.

2.5.1 External Balancing Circuit

The auxiliary circuits could be utilized to equalize the voltages of dc-link capacitors. There are many articles exploring the DCMC with auxiliary circuits in active and reactive power conversions.

In [91], a generalized multilevel topology with self-voltage balancing is presented. Based on switched-capacitor and diode-clamped inverters, the low voltage ripples on dc capacitors are achieved in [92]. However, these methods need lot of extra switches and clamping capacitors and/or diodes.

Other auxiliary circuits are based on chopper circuits in the dc bus. Inductor switch mode power supplies (SMPS) operate in a discontinuous inductor current mode, are used to balance the dc-link capacitor voltages of a 5L DCI. In [93]–[97] STATCOM, UPFC based on chopper stabilization was proposed. Another balancing circuit with separate capacitor voltage control and inductor current control, achieves voltage equalization as discussed in [98]. Start-up, charge-up, balance dc-link capacitors of inductor based SMPS are described in [99].

Hasegawa, K [100] proposed a new dc-voltage-balancing circuit for a medium-voltage motor drive with a three-phase diode rectifier as front end. This circuit consists of two unidirectional choppers and a single coupled inductor with two galvanically isolated windings. The inductor produces no net dc magnetic flux because the individual dc magnetic fluxes generated by the two windings are canceled out with each other. This makes the inductor compact by a factor of six, compared with the balancing circuit including two noncoupled inductors.

Three capacitor based balancing schemes based on generalized method in [91] namely one-capacitor-based scheme, one-level capacitor-based scheme and simplified one-capacitor-based scheme are proposed and compared with inductive based schemes in [101]. One-inductor-based auxiliary circuit for dc-link capacitor voltage equalization of DCI is also proposed by same author in [102]. Parallel switch-based chopper circuit for DC capacitor voltage balancing is proposed in [103].

The inductor-based scheme even could reduce half number of switches without regarding the voltage limit of switches. Obviously, the less the passive and active devices adopted, the lower hardware cost balancing circuits require. But if loads are unbalanced, the inductor-based scheme would fail to guarantee the voltage equalization. It needs a PWM method by using zero-sequence voltage injection for voltage balancing of the midpoint for the positive and negative nodes. Otherwise, the voltages of upper part capacitors would be unequal to the lower part capacitors. On the contrary, the four capacitor-based schemes provide active power exchange path between the capacitors of upper part and lower part. Therefore, the midpoint voltage would be controlled by the auxiliary balancing circuits.

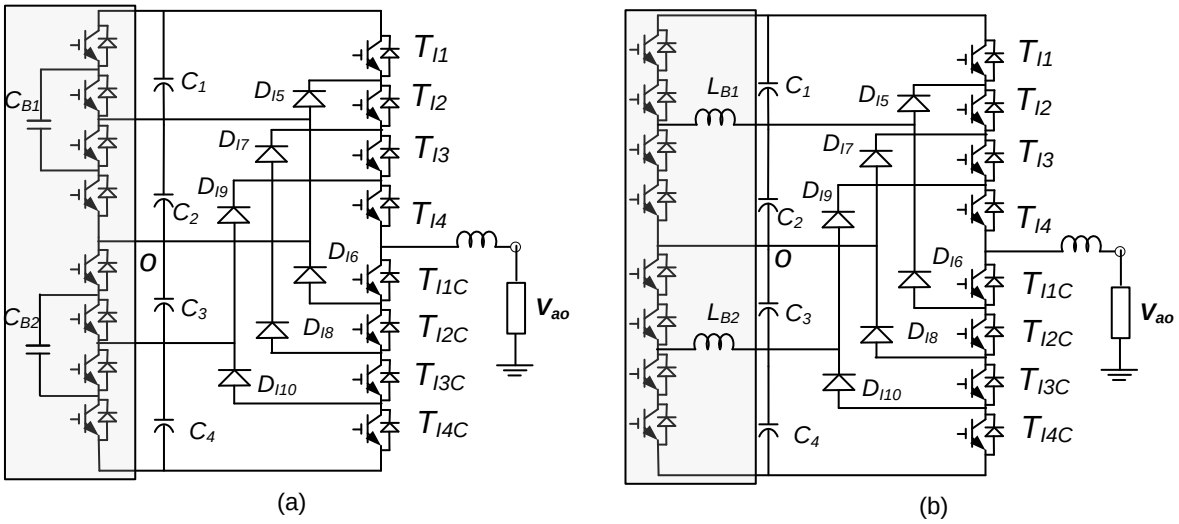


Figure 2-17 External balancing circuits for DCI.

2.5.2 Converter/Inverter Back-to-Back Configuration

Zhiguo Pan [104] presents a novel sinusoidal pulse width modulation control method with voltage balancing capability for the diode-clamped 5L rectifier/inverter system. The voltage balancing effects of the third harmonic offset injection to all three-phase voltages are discussed. Marchesoni, M, [105] presented an effective balancing strategy suitable for MPC conversion systems with any number of DC-link capacitors. AC/DC/AC power conversion, the back-to-back connection of a multilevel rectifier with a multilevel inverter allows the balance of the DC-link capacitor voltages and, at the same time, it offers the power-factor-correction capability at the mains AC input.

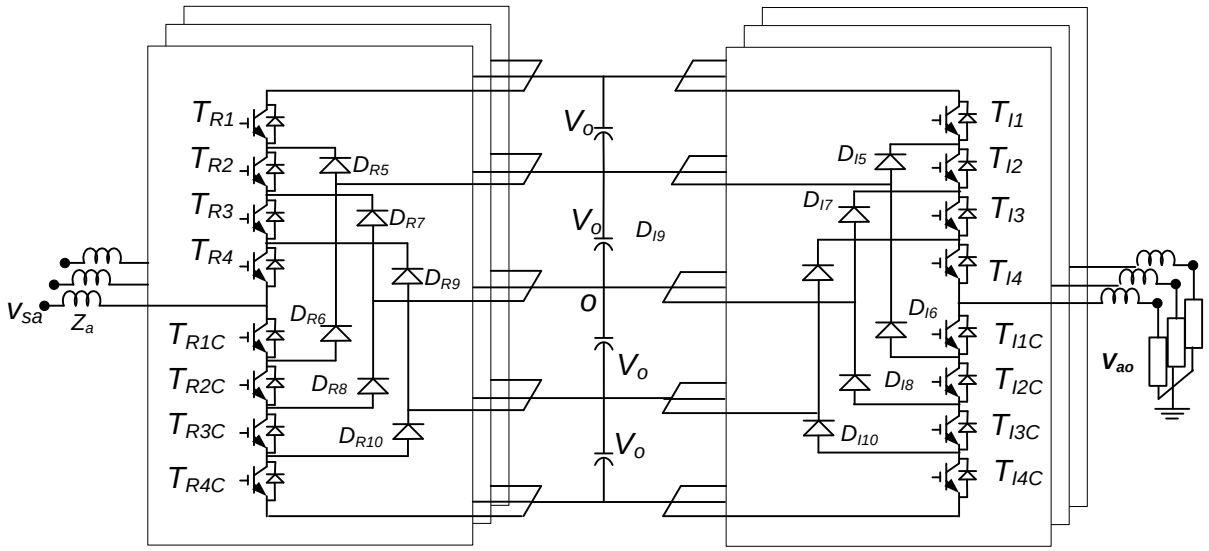


Figure 2-18 AC/DC/AC MPCI converter system with self-capacitor voltage balancing.

2.5.3 Using Modulation Schemes

Many authors proposed PWM strategies for capacitor voltage balancing to avoid extra cost when using active front-end or balancing circuit.

Most of the capacitor voltage balancing schemes are based on the space vector modulation (SVM). There are many simplified SVM method for multilevel inverters, among which three kinds of methods are most popular: 60° coordinate method, 135 ° coordinate method and reference decomposition method. Former two methods are similar, and they only differ at which coordinate they choose. The principle of these two methods is to change the trigonometric operations in rectangular coordinates to integer operations in 60° or 135 ° coordinate system. The reference-decomposition SVM methods are superior as they are based on the basic two-level SVM method: The vector time calculation is as simple as two-level SVM, and the space vector selection and switching sequence selection can be directly based on two-level situations.

In minimum loss SVPWM (MLSVPWM) method, three nearest switching states are selected such that one of the phase is kept on or off for whole switching period and make only one switching event for the other two phases. So MLSVPWM scheme restricts switching to only two phases at any particular time and eventually reduces switching losses by one third over one electrical cycle. In [106] implementation of the MLSVPWM for 3-level and 5L DCI have been presented. Minimum energy criteria based on minimizing a quadratic parameter is given by

$$G = \frac{1}{2} C \sum_{p=1}^{n-1} \Delta v_{Cp}^2 \quad \text{Where} \tag{2.20}$$

n =no. of levels; v_{Cp}= Voltage across capacitor p. was introduced by Marchesoni [107].

J.Pou [108] introduced two voltage-balancing criteria for selecting redundant vectors in the modulation. Derivative minimization and direct minimization which are based on minimizing a quadratic parameter [107] that depends on the voltages of the capacitors. S. Ali Khajehoddin [109] presented a generalized form of above criteria that extended to m-level Diode Clamped Inverter using current flow model. However, methods based on minimum energy criteria [39]-[41] doesn't solve the problem completely and the limitation depicted in Figure 2-16 prevails. [110]

A new concept called virtual space vector PWM is introduced by Sergio Busquets-Monge in [78]. A set of new virtual vectors is defined as a linear combination of the vectors corresponding to certain switching states such that average mid-point currents in each switching cycle must be zero to avoid a variation of mid-point voltages. A pulse width modulation (PWM) strategy derived from VSVM, guaranteeing a dc-link capacitor voltage balance in every switching cycle under any type of load, with the only requirement being that the addition of the three phase currents equals zero was established in [111]. It also provides the expressions of the leg duty-ratio waveforms corresponding to this family of PWMs for an easy implementation. Sergio Busquets-Monge [112] presents a closed-loop control scheme for the 3L NPCI using the optimized nearest three virtual-space-vector pulse width modulation. Extension to the above method for any number of dc-link voltage levels and converter legs (i.e., for single-phase and multiphase systems), guaranteeing the capacitor voltage control for any modulation index value and load (i.e., from idle mode to full power) is presented in [113].

However, the NTV PWM is clearly superior to the VSV-PWM from both the point of view of output voltage harmonic distortion and multilevel inverter switching losses. VSV-PWMM is effective only if the modulation index is less than $1/n - 1$, for which, the output voltage distortion and switching losses are the same for both PWMs since they are equivalent for this modulation index range.

Bouhali, O [114] a new modeling and control strategy of a three-phase 5L DCI is presented. a space-vector scheme by a direct space vector of line-to-line voltages without using a Park transform action is explained. No information about balancing limits are specified clearly. Hotait, H.A [115] proposed a redundancy balancing technique, which balances the four dc-link capacitor voltages at high modulation index and high power factor. The technique is based on dividing the vector space of 5L inverter into six two-level vector spaces. The voltage THD with the proposed technique is better than that of the conventional two-level inverter. It is better than 3L NPCI below 0.5 modulation indices, but, similar above 0.5. It is the same as the five-level below the modulation index 0.5, but worse above a modulation index of 0.5.

2.5.4 Other Emerging Methods

Li Su [116], studied influence of active and reactive current and different switching states on DC voltage, introduced an object function optimizing method for low modulation index (m<=0.5).

Wang Yue [117] proposed a novel strategy that divides the whole 5L space vector diagram into low modulation region ($m \leq 0.5$) and high modulation region ($m > 0.5$). In low modulation region, DC capacitor voltage balance is achieved by combining objective function method with reference voltage decomposition method. In high modulation area, DC capacitor voltage balance is realized by applying an optimal balancing vector selection (OBVS) method. Saha, A [118] developed a MLSVPWM scheme that generates all the available switching sequences, then based on capacitor voltages a 5L DCI can be mapped as any lower level DCI structure to increase available switching redundancy.

It has been pointed out in the introduction of [119] that capacitor voltage balancing and common mode voltage cancellation cannot be achieved concurrently in a multilevel inverter. In general, 0nce a PWM strategy is employed for dc-link capacitor voltage balancing, solving problems such as total harmonic distortion, minimal switching frequency, common-mode voltage cancellation, and leakage current elimination with the same strategy is not feasible.

2.6 Conclusion

In this chapter, first, several switching signal generation schemes for MLI are studied and classified. Then, SVM strategies for NPCI topologies are discussed in detail. Two type of vector selection methods namely NTV and non-NTV are performed on 3L NPCI topology for achieving DC-link capacitor voltage balancing. Relative merits and demerits of these methods are discussed. Vector selection, switching sequence formation and duty ratio calculation for both the type of modulations are derived. It has been found that, the NTV modulations are simple to implement due to the symmetry in the sub-triangle regions of SVD. As a result, the modulation can be implemented without using trigonometric expressions and coordinate transformations, etc. On the other hand, non-NTV methods are relatively complex compared to NTV methods due to inherent nature of the sub-triangle regions of SVD and require complex mathematics for duty ratio calculation. In case of MPCI topologies with passive frontends when the voltage levels are higher (≥ 3), it was found that, the capacitor voltage balancing is the major issue. Therefore, various modulation strategies for addressing this issue are reviewed. It concluded that, any modulation strategy cannot simultaneously achieve the functions like capacitor voltage balancing, minimum harmonic distortion, common mode voltage cancelation, minimal switching losses, etc.

Chapter 3: SPACE VECTOR MODULATION ALGORITM FOR MPCI

[In this chapter, a new generalized space vector-based algorithm for modulating multipoint clamped inverter (MPCI) topologies are presented. This approach is suitable for both nearest thee vector (NTV) and non-NTV modulations unlike the other space vector modulation (SVM) algorithms. The method is based on the two-level (2L) SVM in which, NTV and non-NTV methods are implemented with the help of duty ratios of the equivalent 2L SVD. Therefore, the algorithm does not require any coordinate transformation and trigonometry expressions. This results in reduced computational burden in implementation. The algorithm is explained in detail for three-level (3L) neutral point (NP) clamped inverter (NPCI) in which, the duty ratios of the redundant states are distributed to eliminate the low frequency NP voltage oscillations.]

3.1 Introduction

In the MPCI topologies, as the number of levels increases, the capacitor voltage balancing is one of the major issues. As discussed in Chapter 2, non-NTV strategies are required along with the NTV strategies to completely control the individual capacitor voltages for all power factor and modulation indices. It is also evident that, NTV and non-NTV strategies require different algorithms due to their independent choice of voltage vectors.

NTV strategies are relatively simple due to identical nature of sub-triangle regions. They can be implemented with the help of the simplified SVM algorithms based on non-orthogonal coordinate system (60° coordinate systems) and algorithms without transformation (a-b-c system). On the other hand, the non-NTV methods comprise non-identical and non-equilateral sub-triangle regions in each sector of SVD. This results in increased complexity to identify the sub-triangle regions and calculation of the duty ratios of voltage vectors for a given V_{ref}. Therefore, the aforementioned simplified algorithms are also not suitable for non-NTV methods and they still relay on conventional algorithms which require coordinate transformation and trigonometric expressions. Usually, the non-NTV methods are implementation using the PWM approaches by converting the duty ratios of the switching states to individual phase duty ratios offline (manually) for predefined switching sequence. Therefore, the complete control such as switching sequence selection and freedom over redundant switching state selection are limited and as a result requires special controllers for phase duty ratio adjustment.

In order to address the above-mentioned issues, this chapter develops a simplified implementation algorithm is developed in this chapter which is suitable for NTV and non-NTV methods incorporating capacitor voltage balancing. The proposed algorithm uses an

equivalent 2L SVD formed by outer most voltage vectors (two long vectors) and zero vector (their duty ratios) for

i) Calculating the duty ratios of all the voltage vectors corresponding to NTV and non-NTV methods.
ii) Identifying sub-triangle regions of NTV and non-NTV methods.

In this process, coordinate transformations, trigonometric expressions and solutions of volt-second balance equations, etc., are not required. The approach uses only duty ratios of 2L equivalent SVD which are readily available from the voltage references (line-to-line voltage or phase voltage references). Any appropriate switching sequences can be implemented and the duty ratios of redundant switching states can be changed online for NTV and non-NTV methods. The algorithm is explained in detail for 3L NPCI, to eliminate the low frequency NP voltage oscillations.

3.2 Proposed Modulation Approach Based on 2L Equivalent SVD

Figure 3-1(a) shows the circuit schematic of the 3L NPCI supplied with renewable energy sources. Since single DC source is connected between terminals *P* and *N* of NPCI, the unbalance in the capacitor voltages during NPCI operation must be addressed using a proper modulation method. Figure 3-1(b)-(d) shows some three-level (3L) NPCI topology variations. In this thesis, these topologies are termed as NPCI, since they form a common general structure of 3L NPCI. Figure 3-2 shows the equivalent 2L SVD of the 3L NPCI formed by the long vectors $(V_{L1} - V_{L6})$ and the zero vector (V_O). The 2L SVD forms an equilateral triangle in each sector known as main triangle (MT). The volt-second balance equation for V_{ref} located in the first sector of MT is

$$\begin{aligned} d_z V_O + d_x V_{L1} + d_y V_{L2} &= V_{ref} \\ d_z + d_x + d_y &= 1 \end{aligned} \tag{3.1}$$

Where, d_x, d_y and d_z are the duty ratios of V_{L1}, V_{L2} and V_O respectively. Due to the six-fold symmetry of the SVD shown in the Figure 3-2, the duty ratios of V_{ref} for the other regions are calculated in the same manner. Therefore, further analysis will be carried out only in the first sector.

Now, assuming MT duty ratios are known, the following analysis extracts the duty ratios of 3L NPCI voltage vectors for implementing NTV and non-NTV strategies. The duty ratios of redundant switching states are selected in such a way that the low frequency NP voltage oscillations are eliminated. It is to be noted that, the duty ratio distribution presented here cannot control the existing unbalance, however, this issue can be addressed by implementing the feedback approach which discussed in Chapter 3.4.

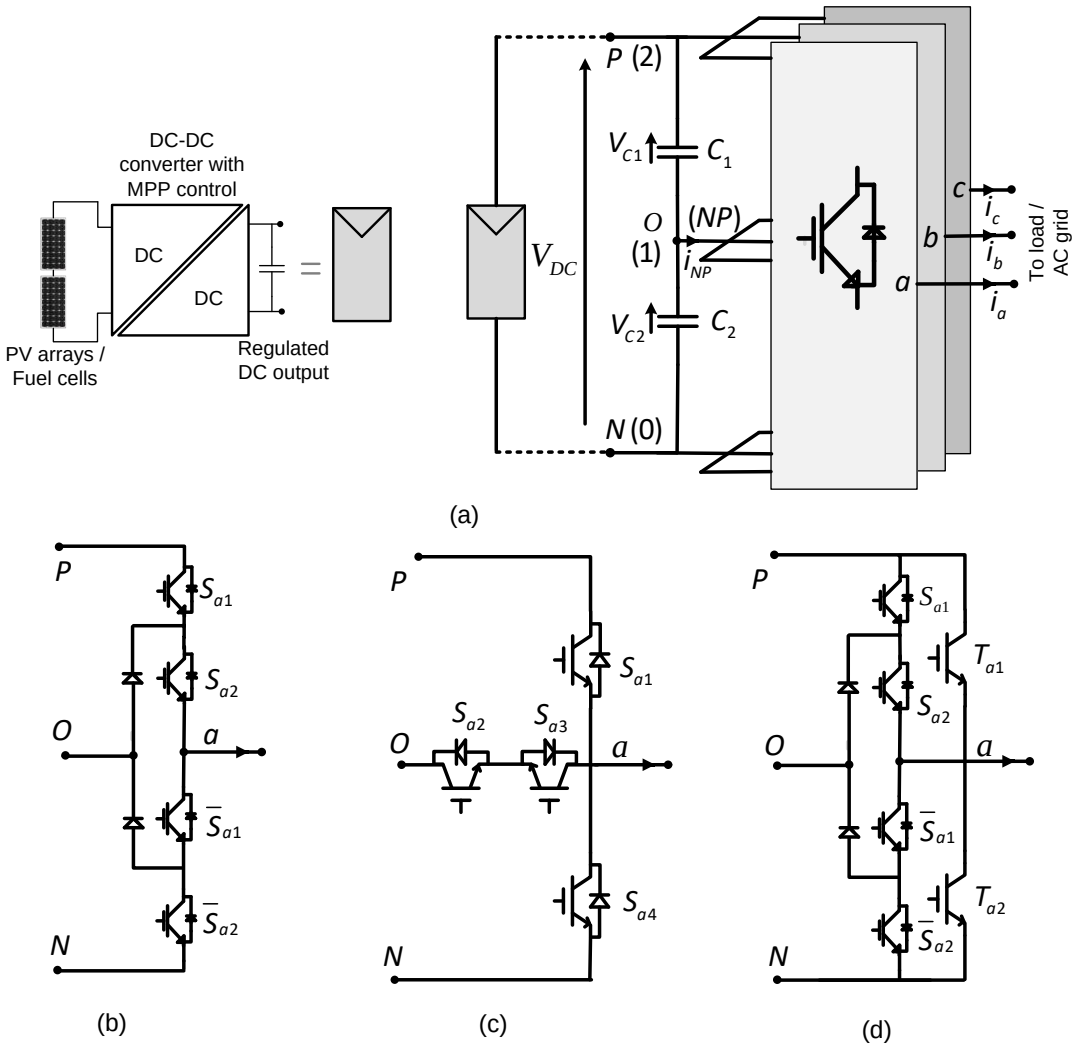


Figure 3-1 (a) Circuit schematic of 3L NPCI, (b) 3L DCI leg, (c) T-type leg and (d) hybrid NPCI leg.

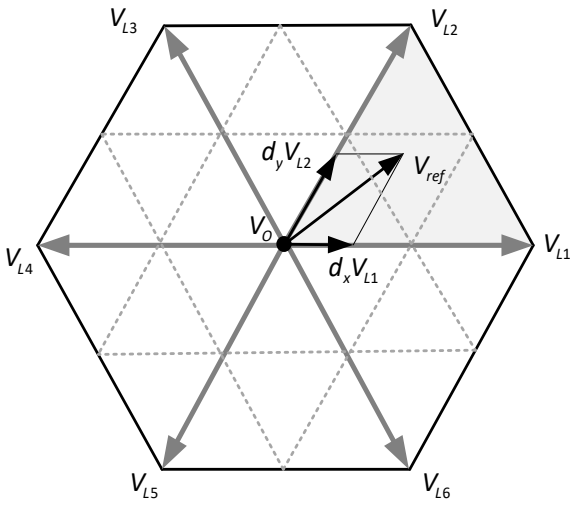


Figure 3-2 Equivalent 2L SVD of 3L NPCI formed by the long vector and zero vector.

3.2.1 NTV Duty Ratio Expressions

Figure 3-3 shows the first sector of the 3L NPCI divided into NTV triangle regions. All the voltage vectors used for NTV modulation are expressed as linear combinations of MT voltage vectors as follows.

$$V_{S1}=\frac{V_O+V_{L1}}{2};\ V_{S2}=\frac{V_O+V_{L2}}{2};\ V_{M1}=\frac{V_{L1}+V_{L2}}{2} \tag{3.2}$$

For instance, if V_{ref} is located in T_{2b} as shown in Figure 3-3, the volt-second balance equation is given by

$$\begin{aligned} d_{M1}V_{M1}+d_{S1}V_{S1}+d_{S2}V_{S2}&=V_{ref}\\ d_{M1}+d_{S1}+d_{S2}&=1 \end{aligned} \tag{3.3}$$

Substituting V_{S1}, V_{S2} and V_{M1} expressions from (3.2) into (3.3) yields that

$$\left\{\frac{d_{S1}+d_{S2}}{2}\right\}V_O+\left\{\frac{d_{S1}+d_{M1}}{2}\right\}V_{L1}+\left\{\frac{d_{M1}+d_{S2}}{2}\right\}V_{L2}=V_{ref} \tag{3.4}$$

Comparing (3.4) with (3.1), the duty-ratios of voltage vectors in terms of MT duty-ratios are obtained as given in (3.5). The duty-ratios of voltage vectors for V_{ref} located in remaining triangles T_0, T_1 and T_3 can be derived in the same manner discussed in (3.3) - (3.5).

$$\begin{aligned} d_{M1}&=d_x+d_y-d_z=1-2d_z\\ d_{S1}&=d_x+d_z-d_y=1-2d_y\\ d_{S2}&=d_y+d_z-d_x=1-2d_x \end{aligned} \tag{3.5}$$

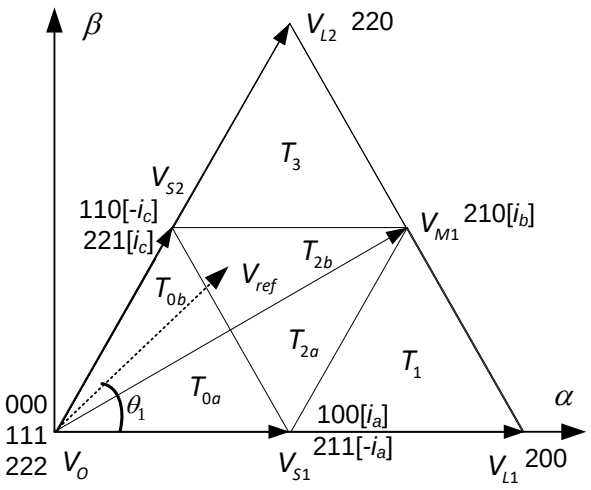


Figure 3-3 First sector of 3L NPCI SVD divided into NTV sub-triangle regions

Once the duty ratios of voltage vectors are identified as described above, the duty ratios of redundant switching states need to be calculated depending on the modulation strategy adopted. In this section, the three-vector four-state synthesis method [120] is adopted. i.e., V_{ref} is synthesized by four switching states in each sub-triangle region $T_0 - T_3$.

In order to eliminate the low frequency NP voltage ripple (third harmonic ripple), the time averaged NP current should be made zero within a switching cycle. For example, if V_{ref} is located in T_{0a} / T_{0b} shown in Figure 3-3, it can be synthesized using two small vectors and one null vector. So, to eliminate low frequency voltage oscillations, the redundant states of the two small vectors (V_{S1} and V_{S2}) are selected for equal duration as given in (3.6). However, if only four vectors are allowed per switching cycle [120], it is not possible to use all redundant switching states and hence equation (3.6) is not valid.

$$\begin{aligned} d_{S1(\mathrm{ONN})} &= d_{S1(\mathrm{POO})} = d_{S1} / 2 = d_x \\ d_{S2(\mathrm{PPO})} &= d_{S2(\mathrm{OON})} = d_{S2} / 2 = d_y \end{aligned} \tag{3.6}$$

A possible switching sequence in the region T_{0a} is '100-110-111-211'. In this sequence, the non-zero neutral current, i_{NP} caused by state '110' is to be compensated by adjusting the duty ratios of redundant states '211' and '100'. It is assumed that the duty-ratios of V_{S1} are distributed as $d_{S1(100)} = k.d_{S1}$ and $d_{S1(211)} = (1-k).d_{S1}$, where $k \in [0,1]$. The time averaged neutral current, $\bar{i}_{NP}$ (for a switching cycle) in T_{0a} region is given by

$$\bar{i}_{NP} = (2k-1) i_a . d_{S1} - i_c . d_{S2} \tag{3.7}$$

Substituting $\bar{i}_{NP} = 0$ into (3.7), the following is obtained:

$$k = \frac{1}{2 d_{S1}} \left[d_{S1} + \frac{i_c}{i_a} . d_{S2} \right] \tag{3.8}$$

Finally, using (3.5) into (3.8) and simplifying, the actual duty ratios are obtained as follows:

$$\begin{aligned} d_{S1(100)} &= k.d_{S1} = \frac{1}{2} \left\{ d_{S1} + \frac{i_c}{i_a} . d_{S2} \right\} = d_x + \frac{i_c}{i_a} . d_y \\ d_{S1(211)} &= d_{S1} - d_{S1(ONN)} = d_x - \frac{i_c}{i_a} . d_y \end{aligned} \tag{3.9}$$

Similarly, when V_{ref} is in triangle T_{2a}, the time averaged neutral current, $\bar{i}_{NP}$ (for each switching cycle) is

$$\bar{i}_{NP} = (2k-1)i_a.d_{S1} - i_c.d_{S2} + i_b d_{M1} \tag{3.10}$$

Substituting $\bar{i}_{NP} = 0$ into (3.10), the following is obtained:

$$k = \frac{1}{2d_{S1}}\left[d_{S1} + \frac{i_c}{i_a}.d_{S2} - \frac{i_b}{i_a}.d_{M1} \right] \tag{3.11}$$

Using (3.5) in (3.11) and simplifying, the actual duty ratios are obtained as follows:

$$\begin{aligned} d_{S1(100)} &= kd_{S1} = d_x + \frac{i_c}{i_a}.d_y \\ d_{S1(211)} &= d_{S1} - d_{S1(ONN)} = d_z + \frac{i_b}{i_a}.d_y \end{aligned} \tag{3.12}$$

When V_{ref} is located in remaining triangles, the duty ratio distributions can be derived in the similar manner. The phase currents associated with the small and medium vectors depend on sector as listed in Table 3-1. All the switching states of first sector and corresponding duty ratios for NTV modulation are summarized in Table 3-2.

Table 3-1 Selection of phase currents for other sectors

Sectors	Phase currents		
	V_{S1}	V_M	V_{S2}
1	i_a	i_b	i_c
2	i_c	i_a	i_b
3	i_b	i_c	i_a
4	i_a	i_b	i_c
5	i_c	i_a	i_b
6	i_b	i_c	i_a

For higher modulation indices and lower power factors, NTV strategies cannot guarantee complete elimination of low frequency NP voltage oscillations. This is due to the involvement of phase currents (magnitude and sign), which make the expressions of duty ratios of the redundant switching states to become negative or greater than unity (saturation). This is an inherent drawback of all NTV strategies and can only be addressed by changing the set of switching states to approximate given V_{ref}. In this context, two non-NTV selections (1) Nearest three virtual vector (NTVV) and (2) Selected three vector (STV) strategies are discussed here.

Table 3-2 Duty ratios of switching states for NTV triangle regions in sector-1

Vectors	Triangles duty ratios					
	T_{0a}	T_{0b}	T_1	T_{2a}	T_{2b}	T_3
$V_{Z(111)}$	$d_z - d_x - d_y$ or$(2d_z - 1)$	$d_z - d_x - d_y$ or$(2d_z - 1)$	-	-	-	-
$V_{S1(100)}$	$d_x + \frac{i_c}{i_a}.d_y$	-	$d_z - \frac{i_b}{i_a}.d_y$	$d_x + \frac{i_c}{i_a}.d_y$	-	-
$V_{S1(211)}$	$d_x - \frac{i_c}{i_a}.d_y$	$2d_x$	$d_z + \frac{i_b}{i_a}.d_y$	$d_z + \frac{i_b}{i_a}.d_y$	$d_x + d_z - d_y$ $(1-2d_y)$	-
$V_{S2(221)}$	-	$d_y + \frac{i_a}{i_c}.d_x$	-	-	$d_y + \frac{i_a}{i_c}.d_x$	$d_z - \frac{i_b}{i_c}.d_x$
$V_{S2(110)}$	$2d_y$	$d_y - \frac{i_a}{i_c}.d_x$	-	$d_y + d_z - d_x$ or$(1-2d_x)$	$d_z + \frac{i_b}{i_c}.d_x$	$d_z + \frac{i_b}{i_c}.d_x$
$V_{M1(210)}$	-	-	$2d_y$	$d_x + d_y - d_z$ or$(1-2d_z)$	$d_x + d_y - d_z$ or$(1-2d_z)$	$2d_x$
$V_{L1(200)}$	-	-	$d_x - d_y - d_z$ or$(2d_x - 1)$		-	-
$V_{L2(220)}$	-	-	-	-	-	$d_y - d_x - d_z$ or$(1-2d_z)$

3.2.2 NTVV Duty Ratio Expressions

Figure 3-4 shows the first sector of the 3L NPCI divided into nearest three virtual vector (NTVV) triangle regions. Similar to Section 3.2.1, the vector positions of VVs are expressed as a linear combination of MT (2L SVD equivalent) vectors as follows:

$$\left.\begin{aligned} &V_{ZO}=V_O;\ V_{ZL1}=V_{L1};\ V_{ZL2}=V_{L2}\\ &V_{ZS1}=\frac{V_O+V_{L1}}{2};\ V_{ZS2}=\frac{V_O+V_{L2}}{2}\\ &V_{ZM1}=\frac{V_O+V_{L1}+V_{L2}}{3}\\ &V_{M1}=\frac{V_{L1}+V_{L2}}{2} \end{aligned}\right\} \tag{3.13}$$

For example, if V_{ref} is located in Δ_1 shown in Figure 3-4, the volt-second balance equation is

$$\begin{aligned} &d_{ZM1}V_{ZM1}+d_{ZS1}V_{ZS1}+d_{ZS2}V_{ZS2}=V_{ref}\\ &d_{ZM1}+d_{ZS1}+d_{ZS2}=1 \end{aligned} \tag{3.14}$$

Substituting V_{ZS1}, V_{ZS2} and V_{ZM1} expressions from (3.13) into (3.14), the following is obtained:

$$\left\{\frac{d_{ZS1}+d_{ZS2}}{2}+\frac{d_{ZM1}}{3}\right\}V_O+\left\{\frac{d_{ZS1}}{2}+\frac{d_{ZM1}}{3}\right\}V_{L1}+\left\{\frac{d_{ZS2}}{2}+\frac{d_{ZM1}}{3}\right\}V_{L2}=V_{ref} \tag{3.15}$$

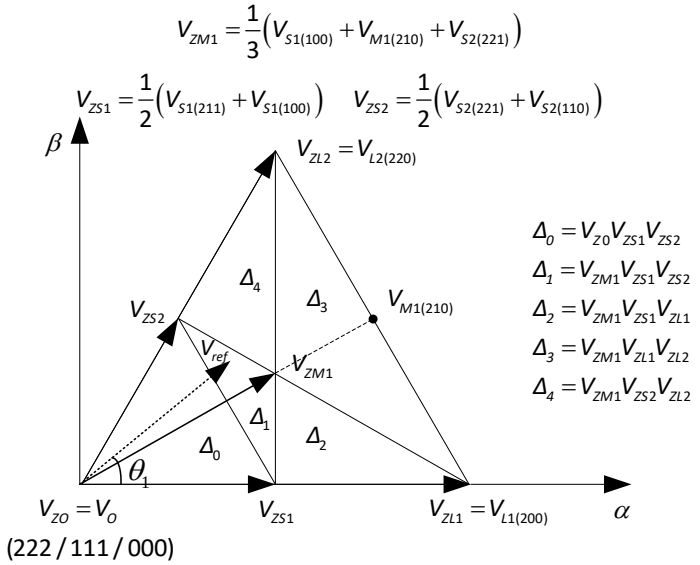


Figure 3-4 First sector of 3L NPCI SVD divided into NTVV sub-triangle regions.

Finally, comparing (3.15) and (3.1)the duty ratios of VVs in terms of MT duty ratios are given by

$$\begin{aligned} d_{ZM1} &= 3(d_x + d_y - d_z) \\ d_{ZS1} &= 2(d_z - d_y) \\ d_{ZS2} &= 2(d_z - d_x) \end{aligned} \tag{3.16}$$

Since, VVs are formed by the linear combination of voltage vectors as shown Figure 3-4, actual duty ratios of switching states need to be calculated as follows:

$$\left.\begin{aligned} d_{S1(100)} &= \frac{1}{2}d_{ZS1} + \frac{1}{3}d_{ZM1} = d_x; \\ d_{S2(221)} &= \frac{1}{2}d_{ZS2} + \frac{1}{3}d_{ZM1} = d_y; \\ d_{S1(211)} &= \frac{1}{2}d_{ZS1} = d_z - d_y; \\ d_{S2(110)} &= \frac{1}{2}d_{ZS2} = d_z - d_x; \\ d_{M1(210)} &= \frac{1}{3}d_{ZM1} = d_x + d_y - d_z; \end{aligned}\right\} \tag{3.17}$$

Similarly, the duty ratios of switching states for remaining locations of V_{ref} are calculated and listed in Table 3-3.

Table 3-3 Duty ratios of switching states for NTVV triangle regions in sector-1

Vectors	Triangles duty ratios				
	Δ_o	Δ_1	Δ_2	Δ_3	Δ_4
V_O	$d_z - d_x - d_y$ or$(2d_z - 1)$	-	-	-	-
$V_{S1(100)}$	d_x	d_x	d_z	d_x	d_z
$V_{S1(211)}$	d_x	$d_z - d_y$	$d_z - d_y$	-	-
$V_{S2(221)}$	d_y	d_y	d_y	d_z	d_z
$V_{S2(110)}$	d_y	$d_z - d_x$	-	$d_z - d_x$	-
$V_{M1(210)}$	-	$d_x + d_y - d_z$ or$(1 - 2d_z)$	d_y	d_x	d_z
$V_{L1(200)}$	-	-	$d_x - d_z$	-	$d_x - d_z$
$V_{L2(220)}$	-	-	-	$d_y - d_z$	$d_y - d_z$

3.2.3 STV Duty Ratio Expressions

Another non-NTV modulation approach known as selected three vector (STV) modulation has been proposed by A.K Gupta [79]. In this modulation, the medium voltage vector which results in non-zero NP current is completely avoided to nullify any NP voltage oscillations. As a result, the phase leg corresponding to medium amplitude reference is switched similar to 2L inverter. First sector of the 3L NPCI divided into various STV regions is shown in Figure 3-5. Unlike the NTVV modulation which uses four vectors in Δ_2 and Δ_3 and five voltage vectors in Δ_4 (refer Figure 3-4), STV method only uses 3 voltage vectors in all the sub-triangle regions.

The duty ratio expressions of STV modulation in terms of MT are derived as follows. For example, if V_{ref} is located in triangle region U_4 as shown in Figure 3-5, the volt-second balance equation is

$$\begin{aligned} &d_{S2}V_{S2} + d_{L2}V_{L2} + d_{S1}V_{S1} = V_{ref} \\ &d_{S2} + d_{L2} + d_{S1} = 1 \end{aligned} \tag{3.18}$$

Using voltage vectors expressions in (3.2), (3.18) is rewritten as

$$\left\{\frac{d_{S1}+d_{S2}}{2}\right\}V_Z + \left\{\frac{d_{S1}}{2}\right\}V_{L1} + \left\{\frac{d_{S2}}{2} + d_{L2}\right\}V_{L2} = V_{ref} \tag{3.19}$$

Comparing (3.19) with (3.1), the duty ratios of the voltage vectors are given by

$$\begin{aligned} &d_{S1} = 2d_x; \\ &d_{S2} = 2(d_z - d_x); \\ &d_{L2} = d_x + d_y - d_z = 1 - 2d_z; \end{aligned} \tag{3.20}$$

In steady state, the duty ratios are divided equally among the redundant switching states. Therefore, in this example, the duty ratios of the switching states are calculated as follows:

$$\begin{aligned} &d_{S1(100)} = d_{S1(211)} = d_x; \\ &d_{S2(110)} = d_{S2(221)} = d_z - d_x; \\ &d_{L2(220)} = d_x + d_y - d_z = 1 - 2d_z; \end{aligned} \tag{3.21}$$

It is to be noted that the NP voltage can be actively controlled by adjusting the duty ratios of the redundant switching states using feedback signal from capacitor voltages or NP current as discussed in Section 3.4. The duty ratios of switching states for V_{ref} located in remaining triangles of STV method are listed in Table 3-4

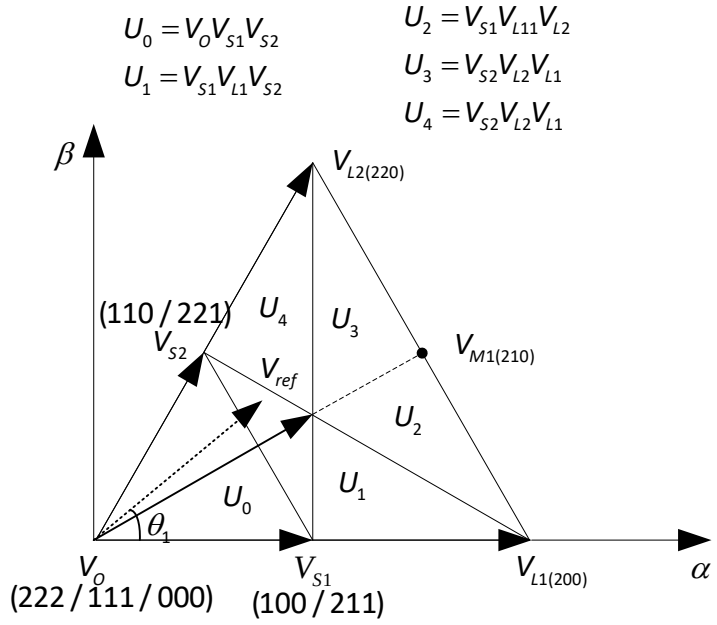


Figure 3-5 First sector of 3L NPCI SVD divided into STV sub-triangle regions.

Table 3-4 Duty ratios of switching states for STV triangle regions in sector-1

Vectors	Triangles duty ratios				
	U_o	U_1	U_2	U_3	U_4
V_O		-	-	-	-
$V_{S1(100)}$	d_x	$d_z - d_y$		-	d_x
	d_x	$d_z - d_y$	d_z	-	d_x
$V_{S2(221)}$	d_y	d_y	-	d_z	$d_z - d_x$
$V_{S2(110)}$	d_y	d_y	-	d_z	$d_z - d_x$
$V_{M1(210)}$	-	-	-	-	-
	$d_z - d_x - d_y$ or$(2d_z - 1)$	$d_x + d_y - d_z$ or$(1 - 2d_z)$	$d_x - d_z$	d_x	
$V_{L2(220)}$	-	-	d_y	$d_y - d_z$	$d_x + d_y - d_z$ or$(1 - 2d_z)$

3.3 Implementation of Proposed Modulation Algorithm

The proposed modulation algorithm embraces two main steps which are summarized in the flow chart shown in Figure 3-6. First, the 2L SVD/MT duty ratios are calculated using the three phase reference voltages regardless of type of modulation to be implemented. Second, the sub-triangle region that comprising the reference voltage vector will be identified along with the duty

ratios of voltage vectors depending on type of modulation. Finally, switching states are converted into PWM gating signals for devices of 3L NPCI.

3.3.1 2L SVD/MT Duty Ratios

As discussed in Section 3.2, the proposed modulation is based on the equivalent 2L SVD. Consequently, first common step is to find the 2L-SVD/MT duty ratios. MT duty ratios d_x, d_y and d_z can be identified by using any of the standard two-level space vector modulation methods like $\alpha-\beta$, $g-h$ (60° coordinate system) or $a-b-c$ reference frames.

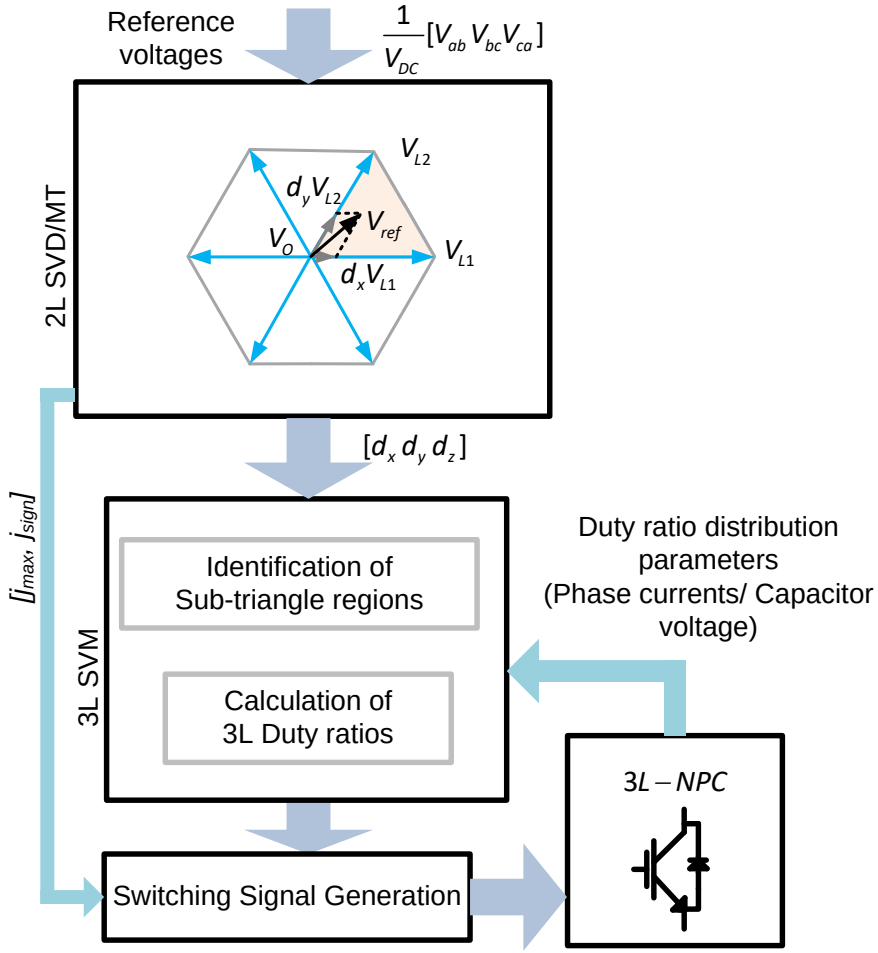
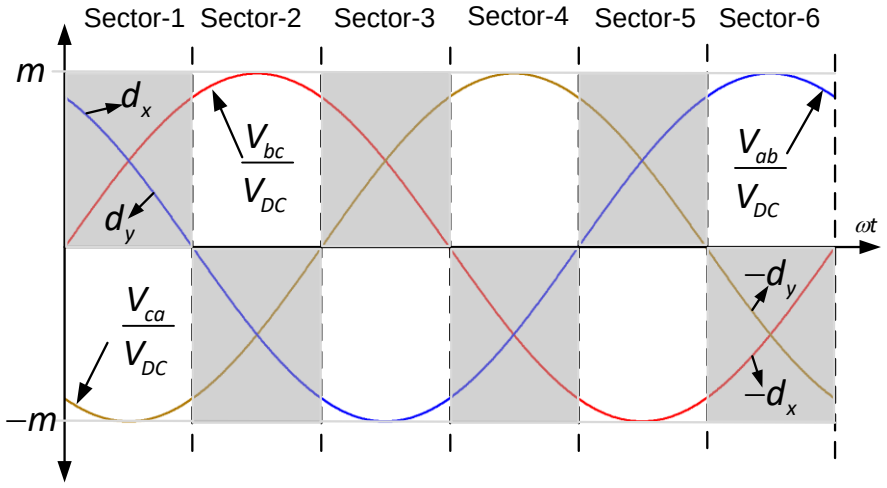


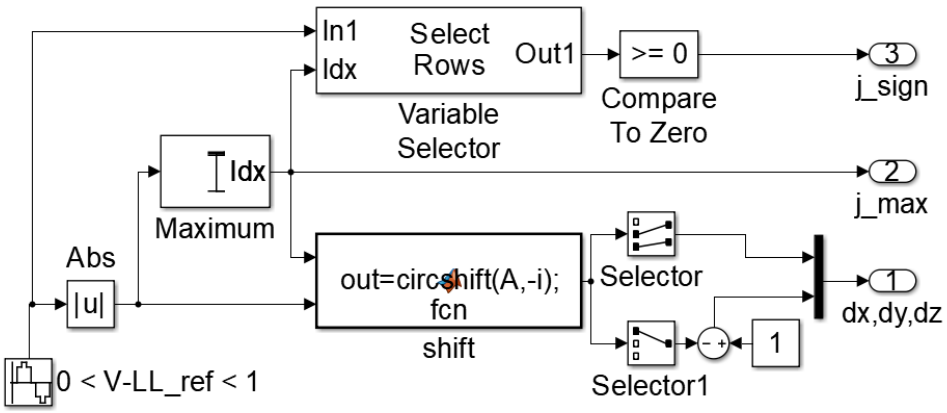
Figure 3-6 Simplified block diagram of proposed modulation algorithm.

3.3.1.1 2L SVD/MT Duty Ratios from Reference Line-To-Line Voltages

From Figure 3-2 and equations (2.4)-(2.7), the volt-second balance equation for the reference vector located in the sector-1 is $V_{ref} = V_{L1}d_x + V_{L2}d_y$. Separating the real and imaginary parts,



(a)



(b)

Figure 3-7 Normalized three phase Line-to line voltages divided into sectors. (b) MATLAB Simulink model for 2L SVD duty ratios generation.

$$V_m \cos(\omega t) = \frac{2}{3}(V_{DC})d_x + \frac{2}{3}(V_{DC})d_y \cos(\frac{\pi}{3})$$
$$V_m \sin(\omega t) = \frac{2}{3}(V_{DC})d_y \sin(\frac{\pi}{3}) \quad (3.22)$$

After simplification,

$$d_x = \frac{\sqrt{3}V_m}{V_{DC}}\sin(\frac{\pi}{3} - \omega t) = m\sin(\frac{\pi}{3} - \omega t)$$
$$d_y = \frac{\sqrt{3}V_m}{V_{DC}}\sin(\omega t) = m\sin(\omega t) \quad (3.23)$$

These two expressions (3.23) are directly related to line-to-line voltage references. Therefore, the duty ratios of MT can be obtained using the line-to-line voltage references as follows.

Table 3-5 Identification of 2L SVD/ MT sectors and duty ratios from line voltage references

Sector	Condition 1	Condition 2	Duty ratios
1	$V_{ab}, V_{bc} \geq 0$	$\lvert V_{ca}\rvert \geq \lvert V_{ab}\rvert, \lvert V_{bc}\rvert;\ V_{ca} < 0$	$d_{L1} = \lvert V_{ab}\rvert;\ d_{L2} = \lvert V_{bc}\rvert$
2	$V_{ca}, V_{ab} \leq 0$	$\lvert V_{bc}\rvert \geq \lvert V_{ca}\rvert, \lvert V_{ab}\rvert;\ V_{bc} > 0$	$d_{L2} = \lvert V_{ca}\rvert;\ d_{L3} = \lvert V_{ab}\rvert$
3	$V_{bc}, V_{ca} \geq 0$	$\lvert V_{ab}\rvert \geq \lvert V_{bc}\rvert, \lvert V_{ca}\rvert;\ V_{ab} < 0$	$d_{L3} = \lvert V_{bc}\rvert;\ d_{L4} = \lvert V_{ca}\rvert$
4	$V_{ab}, V_{ab} \leq 0$	$\lvert V_{ca}\rvert \geq \lvert V_{ab}\rvert, \lvert V_{bc}\rvert;\ V_{ca} > 0$	$d_{L4} = \lvert V_{ab}\rvert;\ d_{L5} = \lvert V_{bc}\rvert$
5	$V_{ca}, V_{ab} \geq 0$	$\lvert V_{bc}\rvert \geq \lvert V_{ca}\rvert, \lvert V_{ab}\rvert;\ V_{bc} < 0$	$d_{L5} = \lvert V_{ca}\rvert\ ;\ d_{L6} = \lvert V_{ab}\rvert$
6	$V_{bc}, V_{ca} \leq 0$	$\lvert V_{ab}\rvert \geq \lvert V_{bc}\rvert, \lvert V_{ca}\rvert;\ V_{ab} > 0$	$d_{L6} = \lvert V_{bc}\rvert;\ d_{L1} = \lvert V_{ca}\rvert$

These two expressions (3.23) are directly related to line-to-line voltage references. Therefore, the duty ratios of MT can be obtained using the line-to-line voltage references as follows.

Figure 3-7 (a) shows the line-to-line voltage references after normalization indicating the six sector regions of 2L SVD and duty ratios of non-zero vectors of MT. If reference voltages V_{ab} and V_{bc} are both positive, it can be identified as sector-1, whereas if they are negative, it can be identified as sector-4. Also, duty ratios of two non-zero vectors are given by $d_x = d_{L1} = \lvert V_{ab}\rvert / V_{DC}$ and $d_y = d_{L2} = \lvert V_{bc}\rvert / V_{DC}$ in the sector-1 and $d_x = d_{L4} = \lvert V_{ab}\rvert / V_{DC}$ and $d_y = d_{L5} = \lvert V_{bc}\rvert / V_{DC}$ in the sector-4. In otherward, the reference voltages are related as $\lvert V_{ca}\rvert \geq \lvert V_{ab}\rvert, \lvert V_{bc}\rvert$ in sectors 1 and 4, such that, $V_{ca} \leq 0$ for sector-1 and $V_{ca} \geq 0$ for sector-4. Table 3-5 summarizes the above analysis for all the sectors which is obtained due to symmetry. A simple shifting algorithm is implemented in MATLAB Simulink to find the duty ratios of 2L SVD as shown in Figure 3-7 (b). Two indices namely j_{Max} and j_{Sign} represents the index of the line voltage with maximum amplitude and its sign respectively. These two variables can be used for sector identification and switching sequence generation. This approach discussed above does not use any coordinate

transformation, reference vector magnitude and angle calculations. Another simple method for obtaining MT duty ratios is also presented in [121].

3.3.2 Identification of Sub-Triangle Regions

In a two-dimensional vector synthesizes, the duty ratios are equal to the distances from the reference vector to the edges of the triangle if the triangle is equilateral and correctly scaled [122]. Figure 3-8(a) shows the basics of vector synthesis for a two-level SVM duty ratios. Therefore, the duty ratio calculations can be simplified with the help of this approach. Figure 3-8(b)-(d) illustrate the division of MT into various regions and corresponding relations among d_x, d_y and d_z. This relation can be easily deduced after simple mathematical steps.

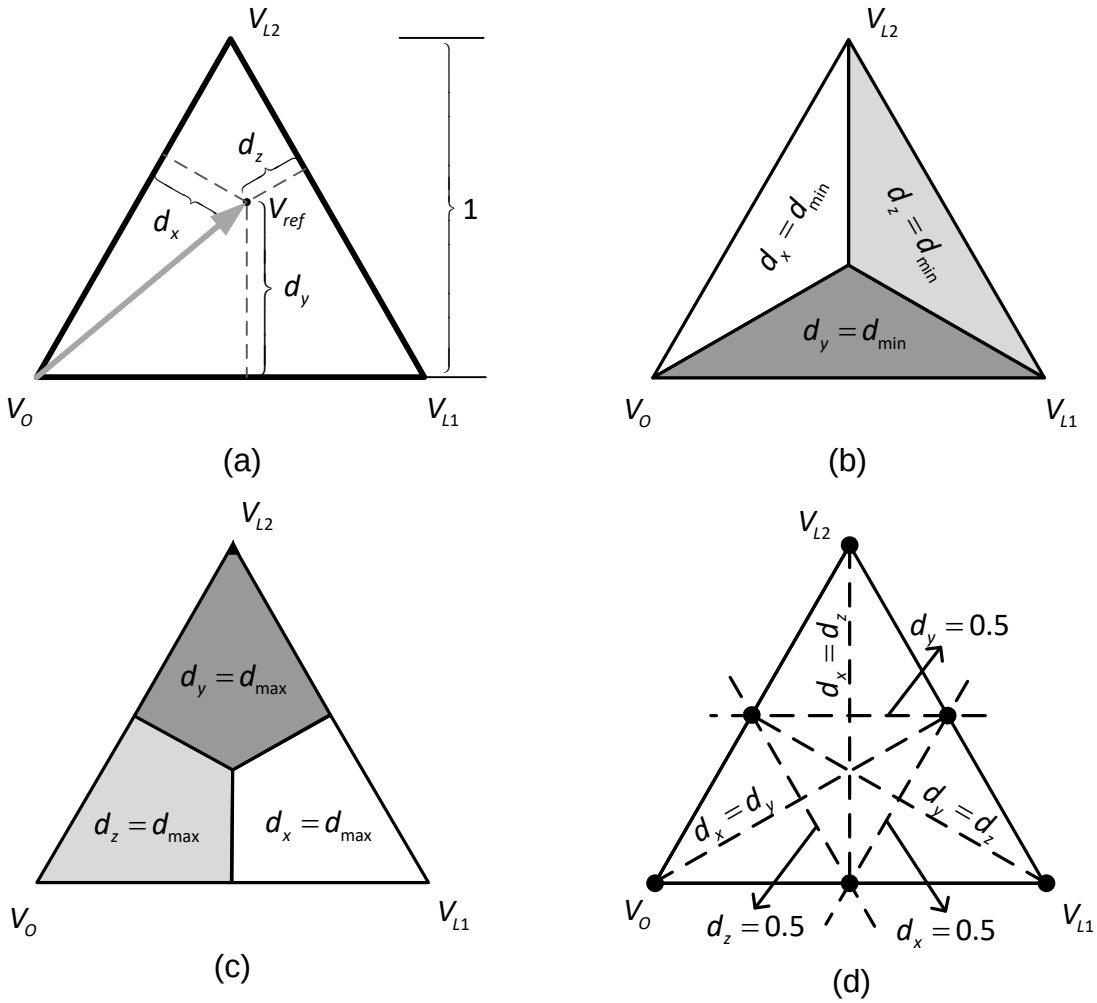
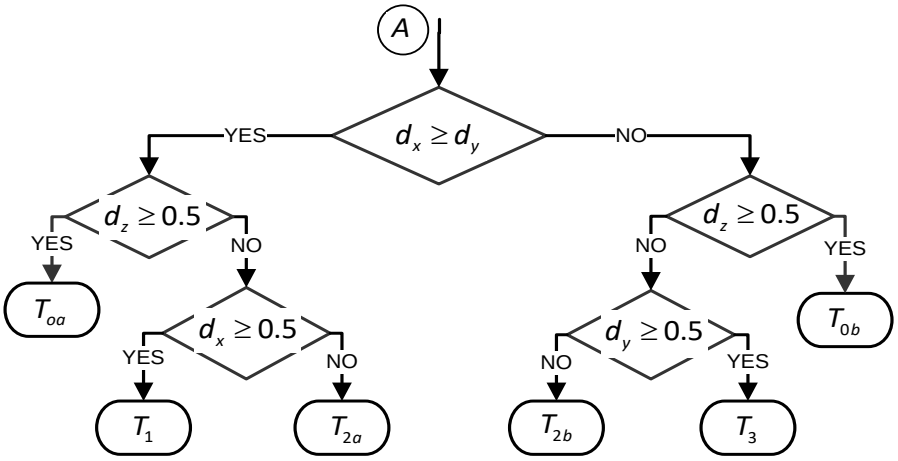


Figure 3-8 Division of first sector of 3L SVD into various sub-triangle regions and the corresponding relations of MT duty ratios.

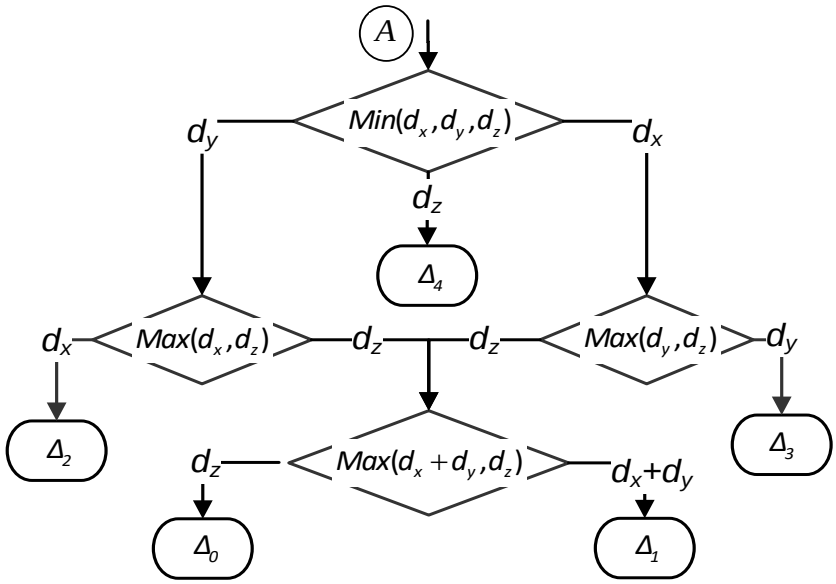
Now, by comparing the duty ratios d_x, d_y and d_z obtained from $2LSVD/MT$ unit (Figure 3-6), the sub-triangle regions of any modulation method can be identified easily. For example, the sub-sector regions T_0, T_1 and T_3 of NTV shown in Figure 3-3 are recognized as conditions

$d_z \geq 0.5, d_x \geq 0.5$ and $d_y \geq 0.5$ respectively. Similarly, if $d_{\min} = d_z$ ($d_{\min}$ is the minimum duty cycle), then it can be identified as Δ_3 of NTVV shown in Figure 3-4. Same relations are valid for all the remaining sectors.

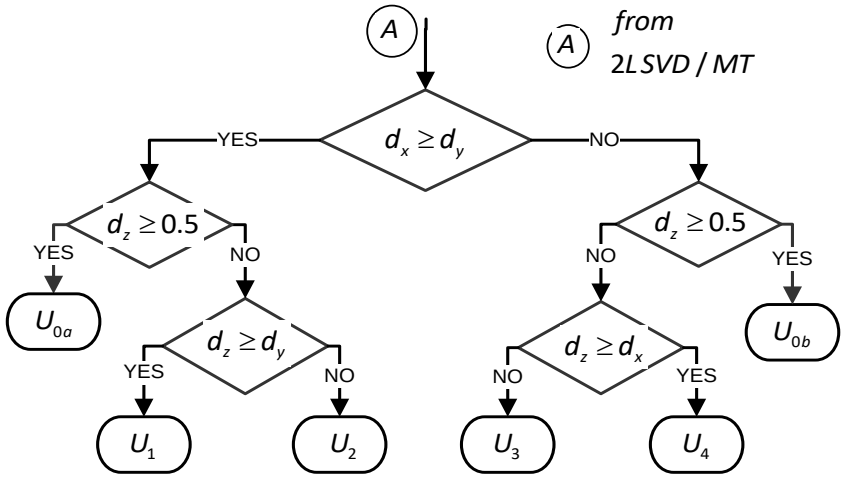
Summarizing above steps to identify the sub-triangle regions, Figure 3-9 shows the 3L SVM unit of Figure 3-6 for NTV and non-NTV modulation methods. It will take MT duty ratios from 2L SVD/MT unit as inputs to identify the sub-triangle regions and duty ratios. Note that, the duty ratios correction for redundant states also requires the phase currents or capacitor voltages as input, however, for simplicity only the sub-triangle identification is depicted here. The actual algorithm requires some extra steps to do the duty ratio correction.



(a)



(b)



(c)

Figure 3-9 Flow chart for identifying the sub-triangle regions from MT duty ratios. (a) NTV (b) NTVV and (c) STV.

3.4 Voltage Imbalance Compensation

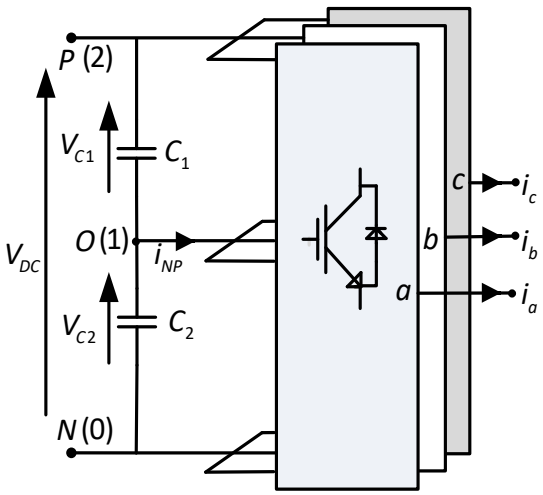


Figure 3-10 Block diagram of 3L NPCI.

Theoretically, if duty ratio distribution maintains $\bar{i}_{NP} = 0$, NP voltage balance can be ensured. However, due to the accumulated error and system imbalances, capacitor voltage will deviate gradually. Therefore, it is necessary to produce $\bar{i}_{NP} \neq 0$ at certain intervals to regulate the capacitor voltages. This must be implemented using the feedback from capacitor voltages and/or phase currents. Some of the existing methods are based on zero sequence voltage injection [123], varied medium vector [124] and multi object optimization algorithm [125]. However, they are complex and require modifications in the duty ratio expressions to achieve NP voltage balance. This section presents a simple duty ratio perturbation method to address

this issue. From Figure 3-10, the NP voltage is defined as $\Delta v = V_{C1} - V_{C2}$. The relation between Δv and NP current (i_{NP}) is given by

$$i_{NP} = i_{C1} - i_{C2} = C\frac{d(V_{C1} - V_{C2})}{dt} = C\frac{d\Delta v}{dt} \tag{3.24}$$

Discretizing above equation in the carrier period T,

$$i_{NP} = \frac{C}{T}\left(\Delta v(K+1) - \Delta v(k)\right) \tag{3.25}$$

Where, i_{NP} is the NP current which can adjust the NP voltage to $\Delta v(k+1)$ at the end of each carrier period. The above equation indicates an unbalance can be controlled by adjusting i_{NP} in successive switching cycles. Therefore, by replacing $\Delta v_{ref} = \Delta v(k+1) = 0$, the non-zero NP current i_{NP} is calculated as

$$i_{NP} = -C\frac{\Delta v(k)}{\Delta t} \tag{3.26}$$

The current i_{NP} must be allowed in consecutive switching cycles by proper selection of voltage vectors (small and medium vectors). This can be achieved by adjusting only the redundant switching state durations. After simplifying (3.26), the perturbation in duty ratios of the redundant states is found to be:

$$\Delta d = \left|\frac{C\Delta V(k)}{i_{NP}T}\right| \tag{3.27}$$

For example, in case of NTVV method, if V_{ref} is located in Δ_2 (refer Figure 3-4), the switching sequence '221-211-210-200-200-100' is used to synthesize V_{ref}. Therefore, the redundant switching states 100 and 211 of V_{S1} are used to compensate the NP voltage imbalance using phase current i_a satisfying the following relation:

$$\begin{aligned} d'_{S1(100)} &= d_{S1(100)} + \Delta d;\ d'_{S1(100)} \in [0, d_{S1}] \\ d'_{S1(211)} &= d_{S1(211)} - \Delta d;\ d'_{S1(211)} \in [0, d_{S1}] \end{aligned} \tag{3.28}$$

Similarly, if V_{ref} is located in Δ_3, the switching states 221 and 110 are used to control the NP voltage imbalance using the phase current i_c. Whereas, if V_{ref} is located in Δ_1, as both the small vector redundant states are available, phase currents i_a or i_c can be used for controlling NP voltage. Proper sign must be incorporated for adjusting duty ratios which must also not exceed

the actual vector duty ratio in order to retain volt-second balance principle. Similar procedure can be implemented for NTV as well as STV to control the NP voltage imbalance.

3.5 Extension SVM Algorithm for Higher Voltage Levels

In this section, the modulation algorithm based on equivalent 2L SVD discussed above is extended for higher voltage levels. The algorithm is explained briefly using a 4L MPCI. Figure 3-11 shows the SVD of the 4L MPCI inverter. Total 64 switching states are available in the SVD which are distributed in 37 voltage vectors: 1 zero vectors; 6 small vectors; 6 medium vectors; 6 small-medium 12 long-medium vectors and 6 long vectors;

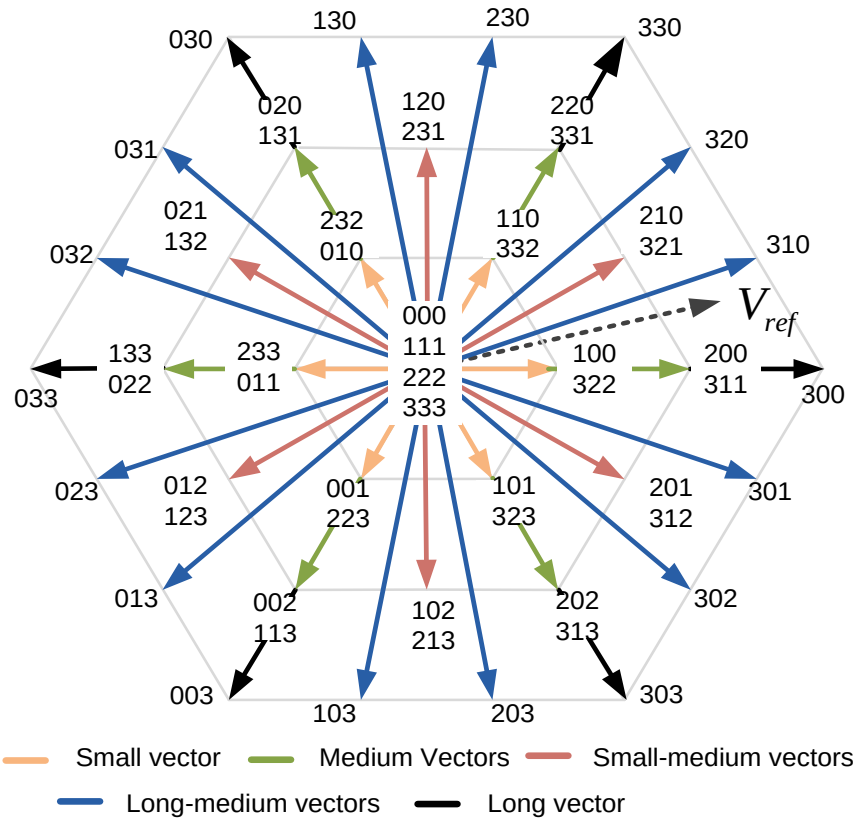


Figure 3-11 SVD of 4L MPCI and switching states.

The duty ratio calculation for a generalized NTV and non-NTV method are explained briefly. The division of first sector of 4L SVD into several sub-triangle regions is shown in Figure 3-12. The VV-based modulation [23] for 4L MPCI is considered here as the non-NTV modulation.

Assuming the duty ratios d_x, d_y, d_z are known, the duty ratios of the voltage vectors of the 4L MPCI can be obtained similar to the 3L NPCI discussed in chapter-3. Figure 3-12 shows various duty ratio relations of 2L SVD/MT duty ratios for the sub-triangle division. For example, if V_{ref} is located sub-triangle region Δ_{347}, the duty ratios of the voltage vectors of the 4L MPCI are given by

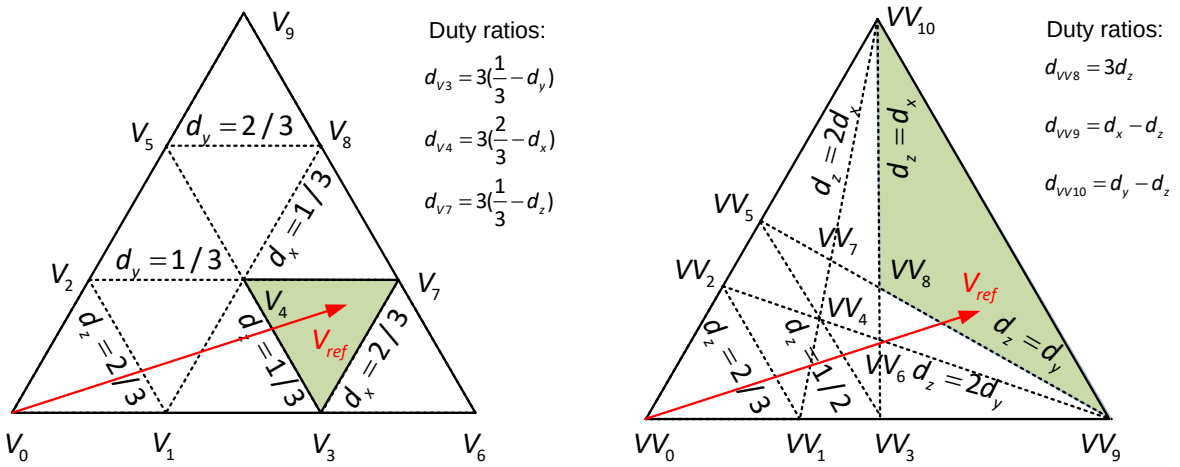


Figure 3-12 Division of first sector of 4L SVD into various sub-triangle regions of (a) NTV modulation and (b) non-NTV modulation and the corresponding relations of MT duty ratios.

$$\begin{aligned} d_{V3} &= 1-3d_y = 3(\frac{1}{3}-d_y) \\ d_{V4} &= 2-3d_x = 3(\frac{2}{3}-d_x) \\ d_{V7} &= 1-3d_2 = 3(\frac{1}{3}-d_z) \end{aligned} \tag{3.29}$$

Similarly, for the virtual vectors given in Figure 3-12(b), the duty ratios of the virtual vectors for the given location of V_{ref} are given by

$$\begin{aligned} d_{VV8} &= 3d_z \\ d_{VV9} &= d_x - d_z \\ d_{VV10} &= d_y - d_z \end{aligned} \tag{3.30}$$

Therefore, the duty ratios for NTV and non-NTV methods can be directly given by the line equations with proper inequalities depending on the location of the voltage vector from the corresponding outermost triangle (equivalent 2L SVD) vertices. Detailed analysis and generalization for multilevel topologies will be considered as future objective.

3.6 Performance Evaluation of Modulation Schemes

Simulations and experiments have been conducted on 3L NPCI to validate the proposed modulation algorithms. The performance is investigated in MATLAB-Simulink using following parameters: DC link voltage=600 V, switching frequency=2 kHz, DC link capacitors =220 µF and variable RL load=10+jπ/2 Ω/phase. Here, the main idea is to eliminate the low frequency (3rd harmonic ripple) in the capacitor voltages. The duty ratios of the redundant switching state are distributed to achieve zero averaged NP current as discussed earlier. NTVV and STV

modulations do not require phase currents or capacitor voltages as feedback, whereas, the NTV modulation require phase currents for duty ratio correction. Small DC link capacitors (220 μF each) and large current (using an adjustable load) is chosen in order to observe the variation of switching ripple depending on the selection of voltage vectors and the effect of change in instantaneous NP current in the capacitor voltages.

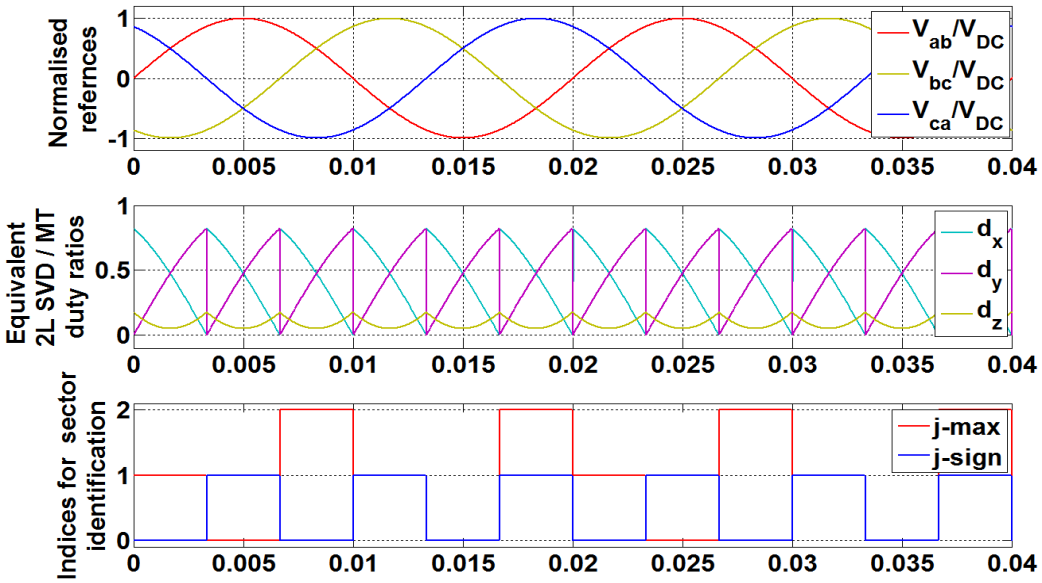


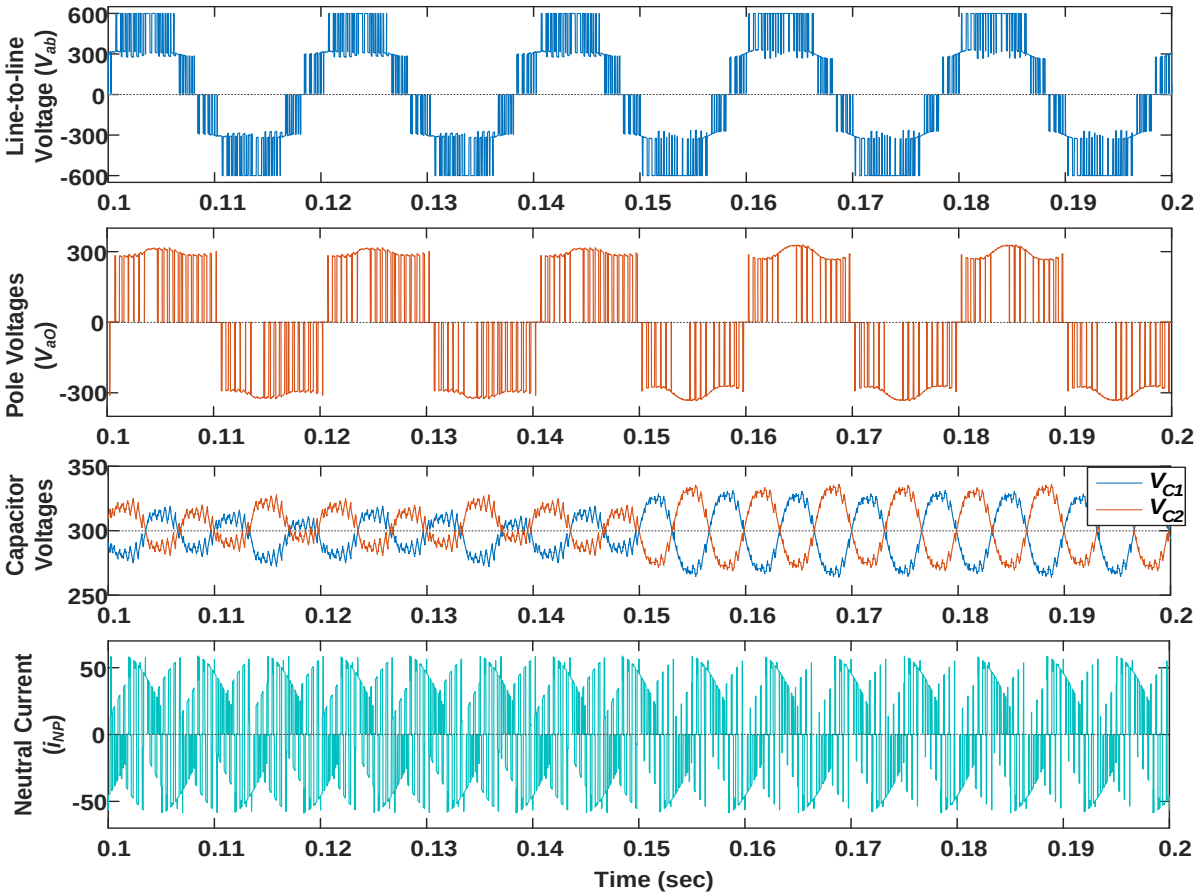
Figure 3-13 Equivalent 2L SVD / MT parameters for m=1.

Figure 3-13 shows the simulated equivalent 2L SVD/MT duty ratios and parameters of from given line-to-line voltage references. The variables j-max and j-sign are used to identify sector and they are directly obtained from the 2L SVD block (refer Figure 3-7 (b)).

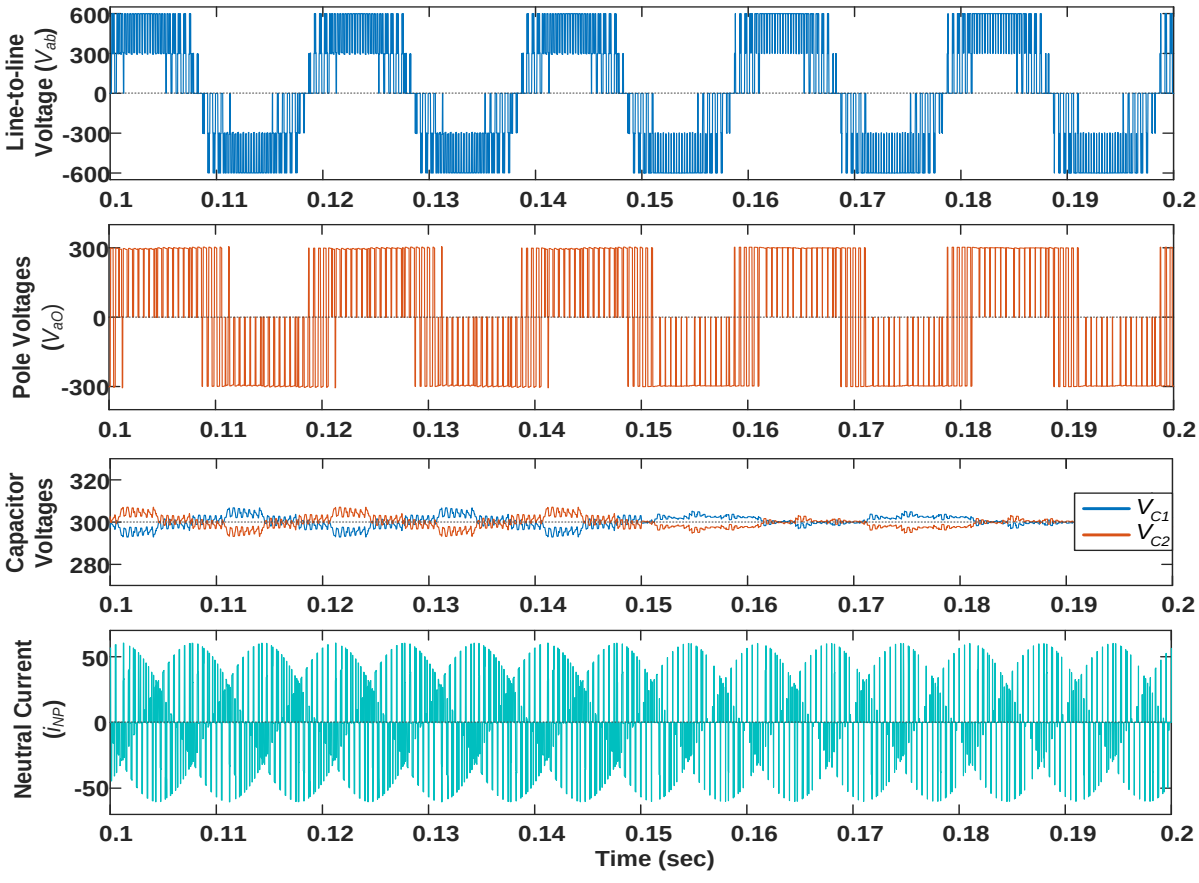
3.6.1 Comparison of Modulation Schemes

3.6.1.1 For $0.5 < m \leq 1$*:*

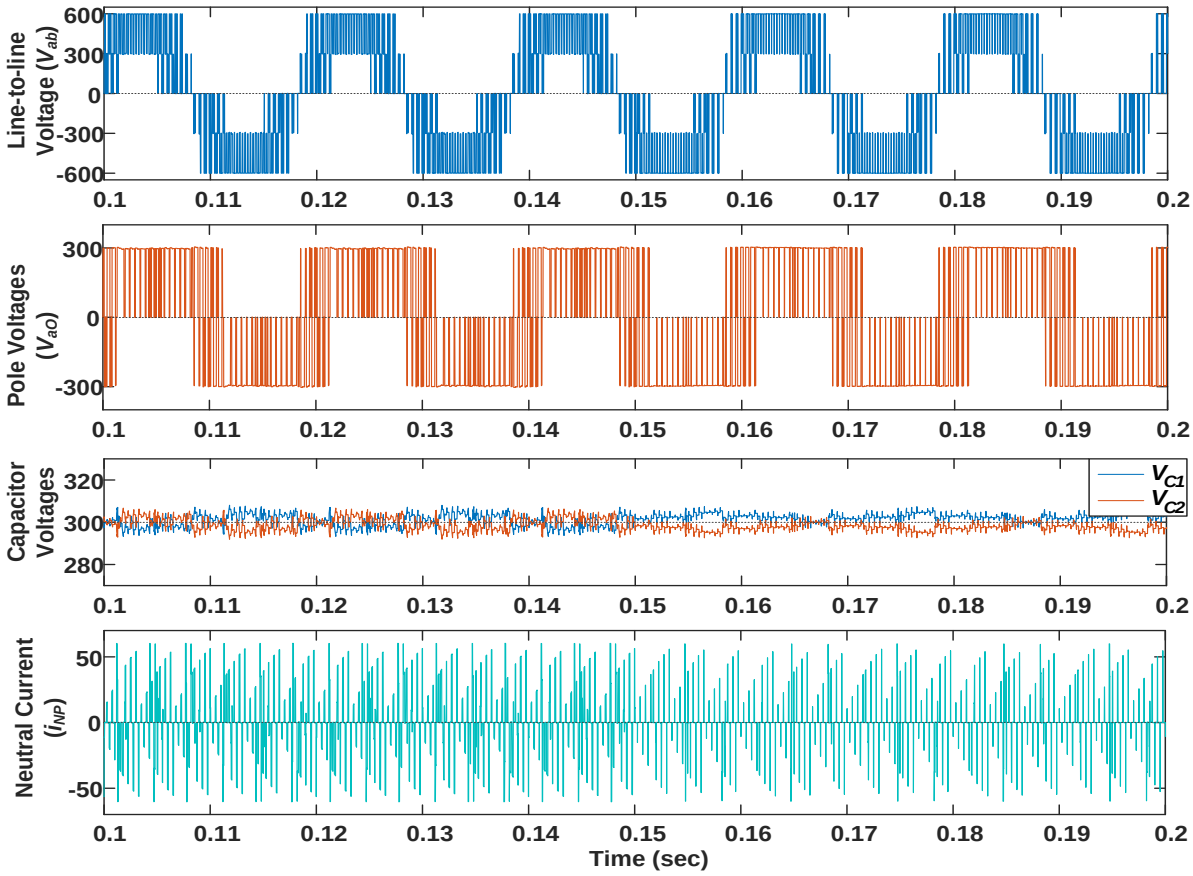
Figure 3-14 shows the steady state waveforms of the NPCI with NTV and non-NTV methods for $m = 0.98$. A balanced three phase current of 60A peak and power factor 0.642 (φ=50º) is flowing into each ac side terminal. The switching sequence is reversed at the middle of each sector in all the modulations to generate symmetrical wave shape [127]. Figure 3-14 (a) shows simulation results of NTV modulation. Clearly, a larger third harmonic ripple (50 V peak to peak) can be observed in the capacitor voltages. This is due to the saturation of duty ratios of redundant vectors for higher modulation index and low PFs in NTV method, resulting in $\bar{i}_{NP} \neq 0$ in large interval of the switching cycle. A positive $\bar{i}_{NP}$ will rise top capacitor voltage V_{C1} and negative $\bar{i}_{NP}$ will rise the lower capacitor voltage V_{C2}.


Line-to-line Voltage (V_{ab})
600
300
0
-300
-600
Pole Voltages (V_{aO})
300
0
-300
Capacitor Voltages
350
300
250
V_{C1}
V_{C2}
Neutral Current (i_{NP})
50
0
-50
0.1
0.11
0.12
0.13
0.14
0.15
0.16
0.17
0.18
0.19
0.2
Time (sec)

(a)

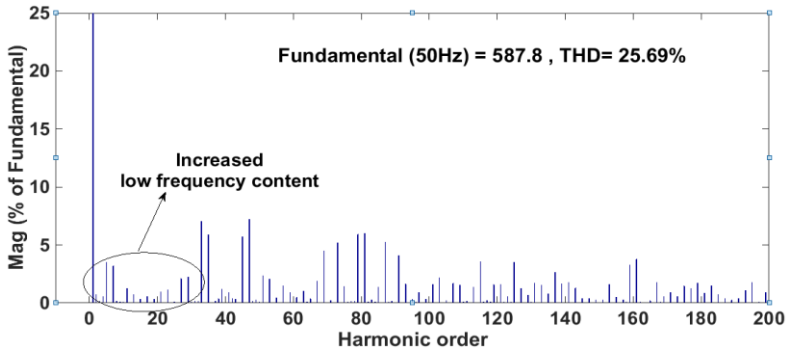

Line-to-line Voltage (V_{ab})
600
300
0
-300
-600
Pole Voltages (V_{aO})
300
0
-300
Capacitor Voltages
320
300
280
V_{C1}
V_{C2}
Neutral Current (i_{NP})
50
0
-50
0.1
0.11
0.12
0.13
0.14
0.15
0.16
0.17
0.18
0.19
0.2
Time (sec)

(b)

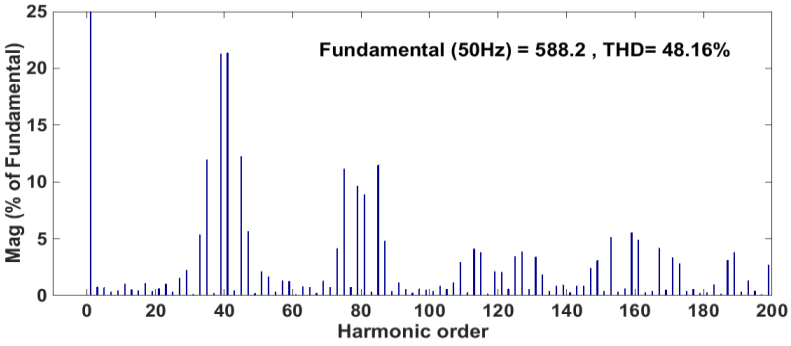


(c)

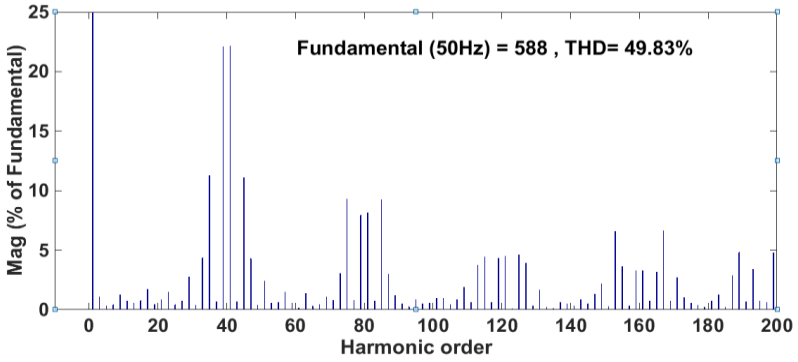
Figure 3-14 Simulation results of NPCI with m=0.98 and and power factor 0.642 for (a) NTV, (b) NTVV and (c) STV.



(a)



(b)



(c)

Figure 3-15 Harmonic spectrum of line-to-line voltages for (a) NTV, (b) NTVV and (c) STV for the operating conditions shown in Figure 3-14 (Fundamental is 100 %).

Figure 3-14 (b) and (c) show the steady state waveforms of NTVV and STV respectively. In contrast to NTV method, $\bar{i}_{NP} = 0$ for each switching cycle in both the non-NTV modulation methods. Therefore, the low frequency voltage ripple is almost negligible. However, a switching ripple (peak to peak voltage of 8V in NTVV and 6V in STV) exists in the capacitor voltages due to the use of small DC link capacitors (220µF each). It is evident that, i_{NP} is significantly different for NTVV and STV. In case of NTVV, more instants of non-zero i_{NP} exists compared to STV modulation. This is due to the participation of medium vector V_M in the case of NTVV modulation for higher modulation indices. On the other hand, V_M is completely avoided in STV modulation. This difference is also evident in the switching ripple of the capacitor voltages in NTVV and STV modulations. Though the low frequency oscillations are eliminated in the non-NTV modulations, a small jump is observed in the capacitors voltage waveforms is due to change in the switching sequence at the middle of each sector to maintain the symmetric waveform [29].

Figure 3-15 shows the harmonic spectrum of line-to-line voltage for the operating conditions shown in Figure 3-14. It can be observed that, the selection of non-nearest voltage vectors to approximate V_{ref} has negative impact on the harmonic spectrum of NTVV and STV modulation methods. However, the increase in spectral content is mainly around the order of switching frequency, which suggest that the weighted THD is approximately same as that of NTV modulation [79]. On the other hand, in case of NTV modulation an increase in the low frequency spectral content is evident as shown in Figure 3-15 (a). This is due to the reflection of third harmonic ripple present in the capacitor voltages onto the ac side waveforms (Figure 3-14 (a)).

3.6.1.2 For $0 < m \leq 0.5$*:*

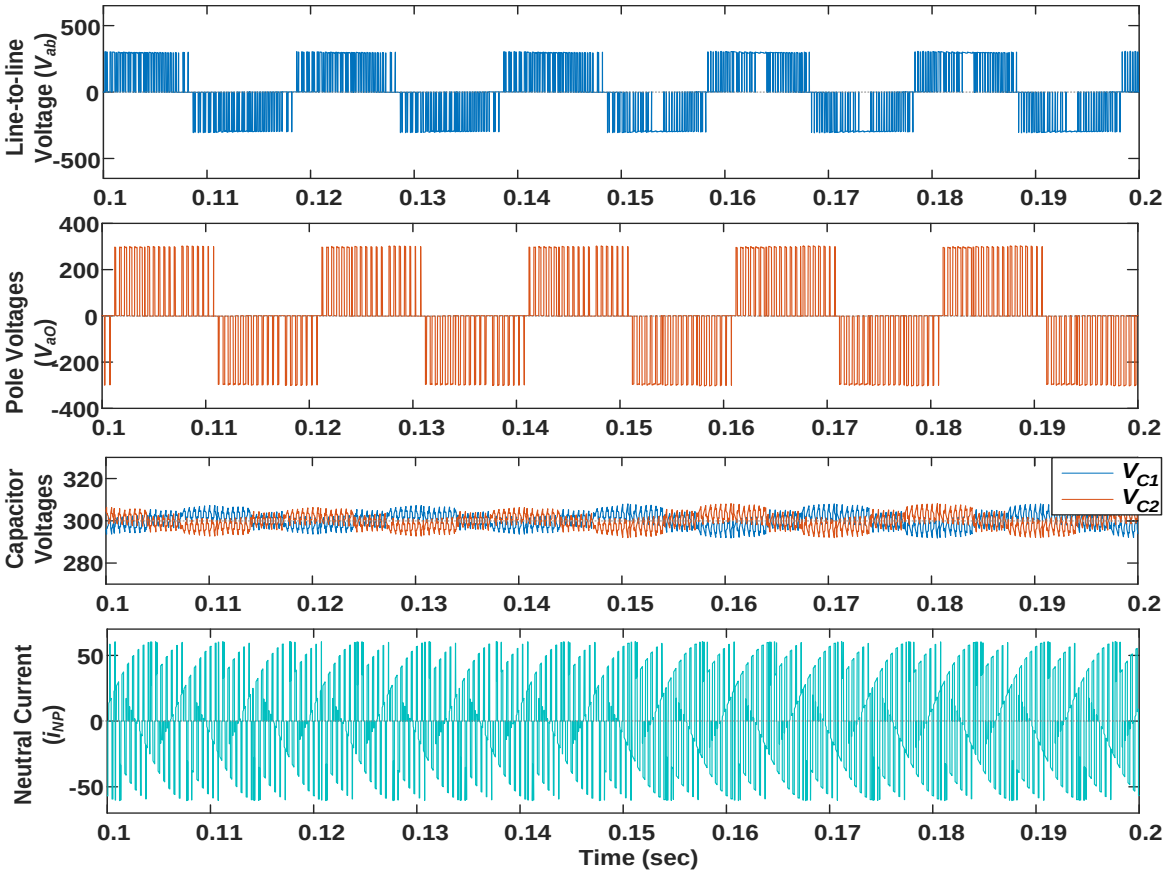
In this modulation index range, the sub-triangle regions of all the modulation methods represents the same area: $T_o / \Delta_0 / U_0$ shown in Figure 3-3. Therefore, the procedure for

identification of the sub-triangle and calculation of duty ratios are mathematically identical for both NTV and non-NTV modulations. However, the duty ratio distributions to the switching states depend on the modulation method. In case of NTV modulation only four switching states are used as discussed in Section 3.2.1. On the other hand, the two non-NTV methods use both the pairs of redundant switching sates for $0 < m \leq 0.5$. Though, theoretically the NTVV methods uses the virtual vectors, it turns out that, both NTVV and STV modulations uses exactly same switching states (refer Section 3.2.2 and 3.2.3). Therefore, for this modulation range, NTVV and STV are represented as NTVV/STV. The three redundant switching states of zero vector 000/111/222 do not cause NP voltage oscillations and can be used in any predefined manner.

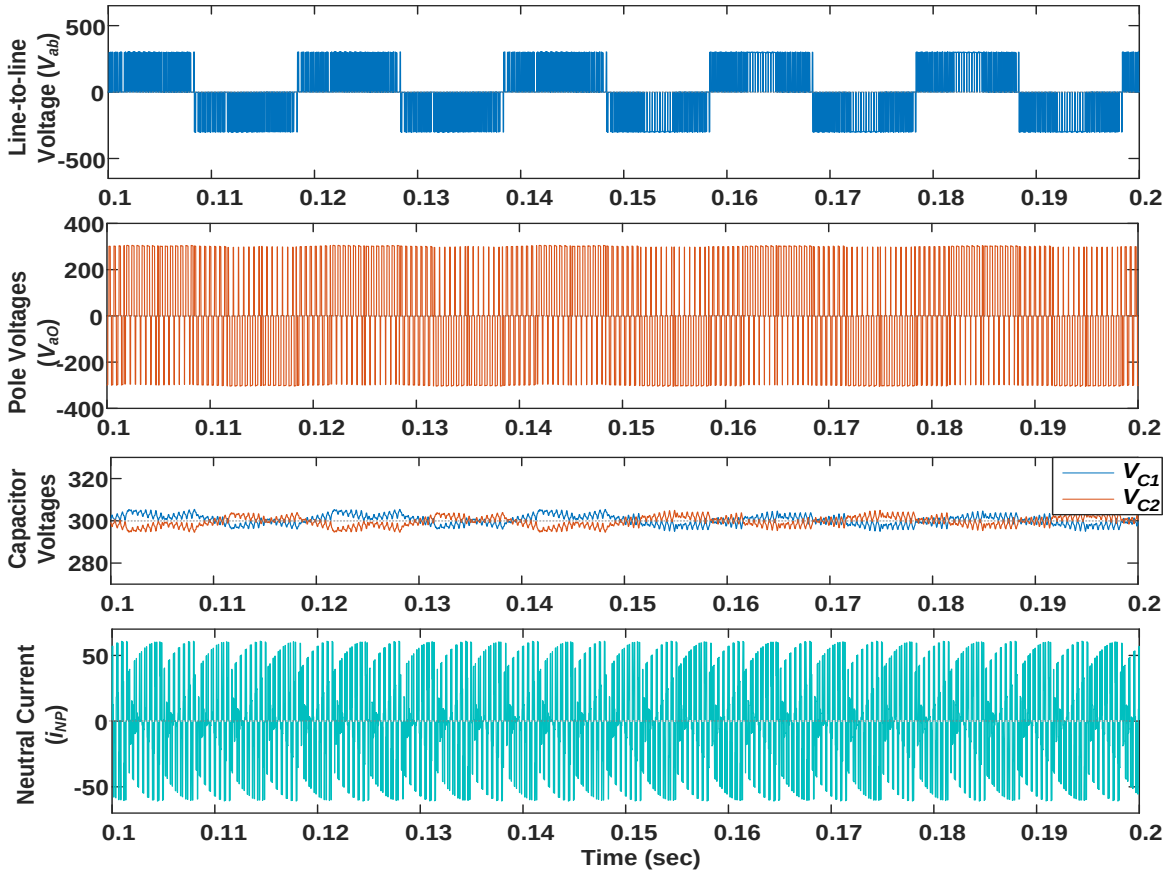
Figure 3-16 shows the performance of 3L NPCI with the aforementioned modulation methods for m=0.5. It can be seen that both NTV and non-NTV modulations are capable of eliminating the low frequency NP voltage oscillations.

NTV modulation (Figure 3-16 (a)) requires only 4 switching states, while, non-NTV modulations require minimum of 5 switching states. Figure 3-16 (b) shows the waveforms of NTVV/STV when all the three zero vector redundancies are utilized following the switching sequence 000-100-110-111-211-221-222 (Sequence-1) [128]. Another possible switching sequence (Sequence-2): 100-110-111-211-221 is formed by discording two redundant switching states of zero vector. In this case the pole voltage waveform is shown in Figure 3-16 (c). THD of the NTV modulation (50.43 %) is found out to be less compared to NTVV/STV with sequence 1(62.85 %) and sequence 2 (52.62 %).

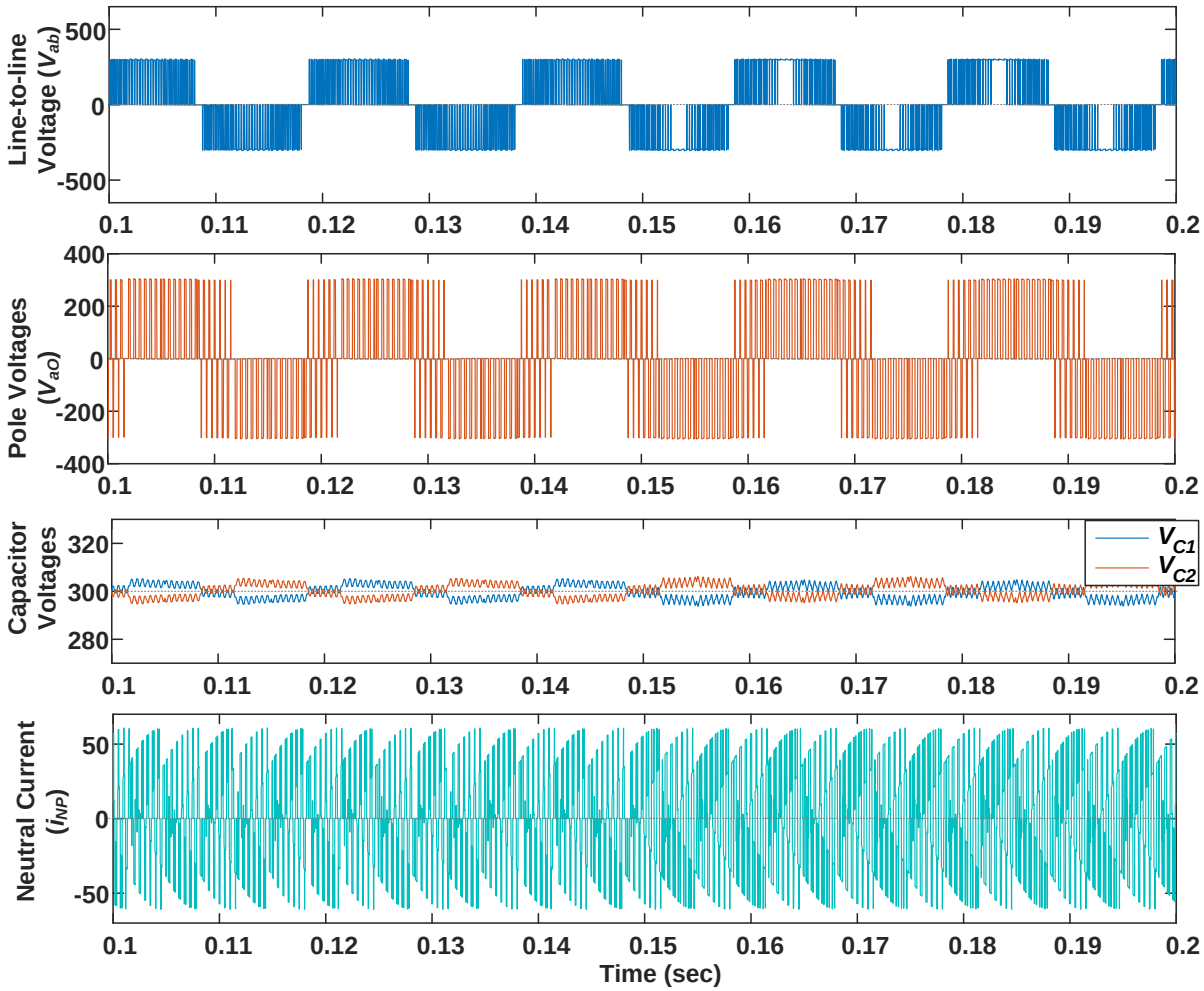
Finally, from above discussion, it can be concluded that for entire linear modulation range $0 < m \leq 1$, NTV method produces minimum voltage distraction compared to both the non-NTV modulations. Moreover, due to the utilization of only 4 switching states, this method is expected to produce minimum switching losses compared to non-NTV modulations.


Line-to-line Voltage (V_{ab})
500
0
-500
Pole Voltages (V_{aO})
400
200
0
-200
-400
Capacitor Voltages
320
300
280
V_{C1}
V_{C2}
Neutral Current (i_{NP})
50
0
-50
0.1 0.11 0.12 0.13 0.14 0.15 0.16 0.17 0.18 0.19 0.2
Time (sec)

(a)


Line-to-line Voltage (V_{ab})
500
0
-500
Pole Voltages (V_{aO})
400
200
0
-200
-400
Capacitor Voltages
320
300
280
V_{C1}
V_{C2}
Neutral Current (i_{NP})
50
0
-50
0.1 0.11 0.12 0.13 0.14 0.15 0.16 0.17 0.18 0.19 0.2
Time (sec)

(b)



(c)

Figure 3-16 Simulation results of NPCI with *m*=0.5 and power factor 0.642 lagging for (a) NTV, (b) NTVV/STV using Sequence-1 and (c) NTVV/STV using Sequence-2.

3.6.2 Capacitor Voltage Unbalance Compensation:

Figure 3-17 shows the voltage balancing capabilities of NTV and non-NTV methods for operating condition described in Figure 3-14. All the three modulations can restore voltage balance for given operating conditions. However, only non-NTV methods can suppress NP voltage oscillations for this operating condition. Moreover, for a given modulation method, the rate of convergence depends on several factors like capacitance value, load current, *m* and *φ*. Whereas, for a given operating condition, it depends on the selection of modulation method. For example, when *φ*=50º, the current associated with V_{s1} is larger (i.e., $|i_a| \geq |i_b| \geq |i_c|$ in Sector 1). Since STV can use i_a as balancing current in entire sub-triangle region U_2, it can restore capacitor voltages little faster compared to NTVV which uses i_b as balancing current in sub-triangle region Δ_4.

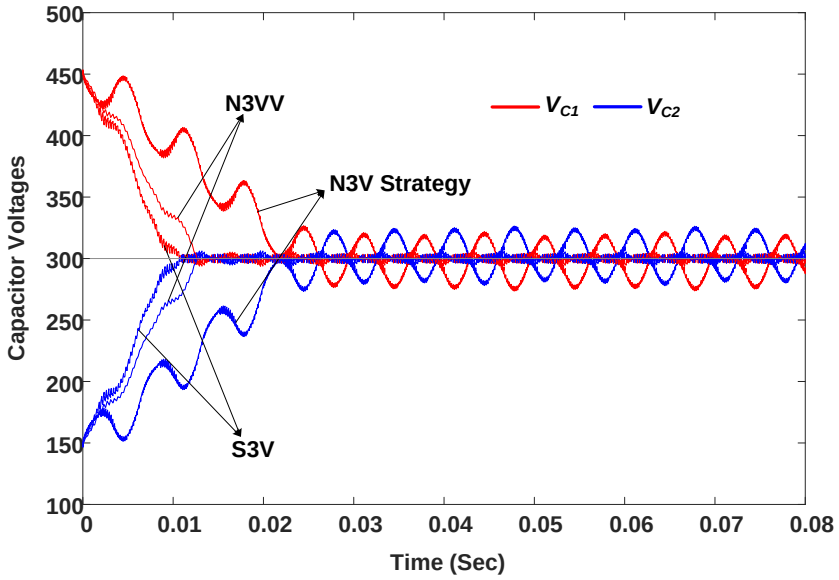


Figure 3-17 Capacitor voltage balancing performance of NTV and non-NTV modulation methods for *m*=0.98 phase current=60A peak and power factor 0.642 lagging.

3.7 Conclusion

This chapter has developed a new approach for modulating MPCI topologies that uses equivalent 2L SVD formed by outermost hexagon. Both NTV and non-NTV modulation schemes have been implemented using the proposed approach which require only MT duty ratios of the equivalent 2L SVD. Duty ratio correction for redundant small vectors can be performed directly on MT duty ratios for any given objective like capacitor voltage balance, switching loss reduction, etc. Therefore, any existing schemes implemented in orthogonal or non-orthogonal frame of reference can be used to find the MT duty ratios, which are then easily modified for actual 3L NPCI switching vectors. Simple methods for calculating MT duty ratios directly from reference line-to-line voltages/phase voltages are also presented. No extra computations are required in the proposed approach for non-NTV methods unlike the other existing methods. This feature facilitates the development of hybrid NTV + non-NTV modulation without increasing the computation burden. The proposed approach is further extended to multilevel operation for implementing NTV and non-NTV modulations. Performance of 3L NPCI with proposed modulation algorithm has been studied and verified in MATLAB/Simulink for various operating conditions.

Chapter 4: HYBRID MODULATION STRATEGIES FOR THREE-LEVEL NPCI

[Neutral point clamped inverters (NPCIs) produce low frequency neutral point (NP) voltage oscillations when modulated with nearest three vector (NTV) methods for certain loading conditions. Non-NTV modulations can address these oscillations at the expense of increased switching frequency, output voltage distortion and complexity. In this context, hybrid modulation strategies formed by combining NTV and non-NTV modulations are discussed, which can also eliminate NP voltage oscillations with the improved overall performance of the 3L NPCI. A new generalized algorithm is formulated for implementation of hybrid modulation strategies with the help of redistributed NTV duty ratios in order to reduce the complexity. Several combinations of NTV and non-NTV modulations are studied and compared. A simplified STV (SSTV) is also derived and a new hybrid NTV-SSTV modulation strategy is also presented.]

4.1 Introduction

A nearest-three-vector (NTV) strategies have the advantage of producing the minimum output THD and power losses. Therefore, these are the most widely used modulation schemes for multilevel inverters modulation uses three voltage vectors closest to the reference vector (V_{ref}). Depending on the redundant vector selection, the NTV methods either use three switching states or four switching states (known as symmetric modulation)[59][60] to approximate V_{ref}. They. However, as discussed in chapter 2, the NTV based methods will cause low frequency NP voltage oscillations due to the increased participation of medium voltage vector for higher modulation index (m) and low power factors.

The non-NTV methods [78], [79], [82]–[85] are developed to eliminate the drawbacks caused by the NTV methods. These methods can completely eliminate the low frequency NP voltage oscillations for any power factors and modulation index. However, in these methods one of the NPCI's leg is to operate as two-level inverter (switching between positive and negative DC rails). In [84], the authors proposed another non-NTV method with reduce complexity, but it forces two inverter's legs to operate as two-level inverter. In [85] a non-NTV is proposed for electric vehicle applications which is suitable for fast change in modulation index, but the operation is similar to two-level VSI. Therefore, these methods have several drawbacks like increased switching frequency, power loss and output THD.

4.1.1 Combination of NTV and Non-NTV Modulations

In view of above shortcomings, different hybrid modulation schemes are evolved to take the advantages of NTV and non-NTV schemes such as minimum output distortion along with low

frequency NP voltage ripple elimination for complete operating range. Several varieties of hybrid modulation schemes are available in the literature [129]–[133] depending on

1) The type of NTV and non-NTV strategies used to develop a hybrid modulation;

2) Condition that determines the selection between NTV and non-NTV methods (selection criteria).

The existing hybrid modulation algorithms considered NTV and non-NTV strategies independently. Therefore, separate set of voltage-second balance equations or trigonometric relations are used to find the duty ratios of the switching states. Moreover, in most of the hybrid modulations [130], [131], [133], the selection criteria to decide the type of modulation (NTV/non-NTV), requires the NTV duty ratios and instantaneous phase currents, therefore, NTV calculations must be performed initially. If the selection criteria chosen the non-NTV method, the non-NTV algorithm needs to be performed separately. In this case, the hybrid modulation algorithm needs to perform both NTV and non-NTV calculations in each sampling time (worse case). As a result, computational burden of the hybrid modulation schemes is relatively high. Existing hybrid modulations are compared on various accepts in Table 4-1.

Table 4-1 Comparison of Hybrid modulation methods

Modulati-on method	**Modulation methods used to form hybrid modulation and selection criteria**	**Complexity**	**Remarks**
Zaragoza, J [129]	Combination of sinusoidal pulse width modulation (SPWM) and a two-carrier based modulation (equivalent to NTVV). The type of modulation is selected manually.	Less	• No active control over the redundant states. • NP voltage oscillation still exist when SPWM is operation. Therefore, cannot completely eliminate NP voltage oscillations.
Gupta, A.K. [79]	A combination of NTV and STV-based on neutral point fluctuation (*npf*). If $npf \leq npf_{max}$ NTV is used, If $npf \geq npf_{max}$ STV is used.	Medium	• Requires to calculate either NTV or STV calculations in each sampling time based on the measured *npf*, therefore needs less processing power. • However, this results in non-optimal and frequent switching between NTV and STV as evaluated in [131] and

			• Always produce $npf=npf_{max}$ (set value). If *npf* is set to zero it uses only STV.
Jiang, W.D. [130]	A combination of NTV and NTVV [78] is implemented using the PDR method. (carrier-based implementation)	High	• Requires the calculation of Phase duty ratios for NTVV when the NTV condition fails. This results in variable execution time for two different conditions. • Optimal switching is obtained. • Requires three PDR /phase. (Total nine). • Sub-sector region identification is not required. Still requires sector identification. • Requires $i_a+i_b+i_c=0$.
Orfanoudakis, G.I. [131]	A combination of NTV and STV [79]. The selection is based on maximum and minimum NP currents (i_{NPhigh} and i_{NPlow})	High	• No implementation method is provided. • Similar to [130], requires to calculate STV parameters separately when the NTV condition fails, results in variable execution time. • High processing power. • No hardware realization.
Busquets-Monge, S. [132]	Optimized the method in [78] to minimize the weighted total harmonic distortion (WTHD). A combination of NTV and NTVV was achieved by selecting certain parameters.	High	• Load power factor angle need to be estimated continuously. • Based on offline computation for non-linear and unbalanced loads results in more complexity. • Requires $i_a+i_b+i_c=0$.
Xia, C. [133]	A combination of NTV and NTVV [78] using SVM.	High	• A proportional parameter (p_m) is introduced to control NP voltage and switching frequency. • When $P_m=0$, it is equivalent to [131]. • NTV and NTVV calculations are performed separately. Results in variable execution time.

As mentioned above, the complexity of existing hybrid modulation strategies is mainly due to the independent nature of NTV and non-NTV modulation methods demanding separate set of calculations. In order to address this issue, in this chapter, a novel relation is developed between

these two strategies in terms of the duty ratios of voltage vectors. These duty ratio relations are used to develop a new hybrid modulation algorithm which is basically an NTV based algorithm with an updated mapping unit. It selects either NTV or non-NTV modulation based on the selection criteria, but will eliminate complex calculations needed to find the sub-triangle regions and duty ratios of the non-NTV modulation for a given V_{ref}. This unique feature will also facilitates the application of many simplified approaches available in the literature to calculate NTV duty ratios [53], [54], [67], [68], which does not require complex coordinate transformation and trigonometric expressions. Therefore, the proposed hybrid modulation algorithm requires less execution time and computational burden compared to the existing hybrid modulation strategies. Here, a selection criterion is developed such that the low frequency NP ripple is eliminated, therefore, very small DC link capacitors can be used to operate NPCI.

In contrast to the existing hybrid modulation schemes discussed above, in this chapter, a novel relation is established between the duty ratios of NTV and non-NTV modulations for a given V_{ref}. This completely avoids the recalculation of non-NTV duty ratios once the selection criteria choose non-NTV modulation and so allows an easy switching between NTV and non-NTV modulations.

4.2 Elimination of Low Frequency NP Voltage Ripple

As discussed in Chapter 3, the time averaged NP current (i_{NP}) should be made zero for each switching cycle in order to eliminate the low frequency voltage ripple in the NP.

4.2.1 Boundary Condition for NTV Modulation

Figure 4-1 shows the first sector of SVD divided in to NTV triangle regions. The constraint need to be fulfilled by the NTV method in order to achieve zero NP voltage oscillations is described briefly as follows.

For $0 \le m \le 0.5$*:* In this case V_{ref} will be synthesized by switching states of the inner triangle T_0. The three vector four switching state selection discussed in chapter 3 or five switching state selection using (4.1) and zero vectors can completely eliminate the NP voltage oscillations.

$$\begin{aligned} d_{S1(ONN)} &= d_{S1(POO)} = d_{S1}/2 \\ d_{S2(PPO)} &= d_{S2(OON)} = d_{S2}/2 \end{aligned} \tag{4.1}$$

For $0.5 \le m \le 1$*: E*quation (4.1) will not hold good for $0.5 \le m \le 1$ due to the presence of medium voltage vector V_M. For example, when V_{ref} is located in the T_2 as shown in Figure 4-1, The average NP current for one switching cycle is given by

$$i_{NP} = (2.k_{p1} - 1).d_{S1}.i_a + d_M.i_b \tag{4.2}$$

Where, k_{p1} is the distribution factor for ONN, such that, $d_{S1(ONN)} = k_{p1}.d_{S1}$ and $d_{S1(POO)} = (1-k_{p1}).d_{S1}$. Substituting $i_{NP} = 0$ in (4.2),

$$k_{p1} = \frac{1}{2}\left[1 - \frac{d_M.(i_b)}{d_{s1}.(i_a)}\right] \tag{4.3}$$

Similarly, is the distribution factor for PPO, when V_{ref} is located in triangle T_3, the average current in the NP is given by

$$i_{NP} = (2.k_{p2} - 1).d_{S2}.i_c + d_M.i_b \tag{4.4}$$

Substituting $i_{NP} = 0$ in (4.4),

$$k_{p2} = \frac{1}{2}\left[1 - \frac{d_M.(i_b)}{d_{s2}.(i_c)}\right] \tag{4.5}$$

When V_{ref} is located in k_{p2} triangle k_{p1} le T_1, and k_{p2} expressions are calculated in the similar manner by equating the average NP current equal to zero.

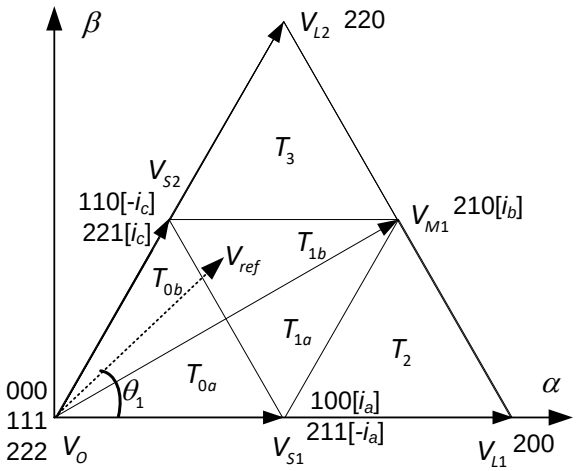


Figure 4-1 Sector-1 of 3L NPCI divided into NTV triangle regions.

The values of and k_{p2} must be a positive real number between 0 and 1 such that all the duty ratios of small vectors $d_{S1(ONN)}, d_{S1(POO)}, d_{S1(PPO)}$ and $d_{S1(OON)}$ are positive. Therefore, the boundary condition for NTV modulation, in order to eliminate the NP voltage ripple is $0 < k_{p1} < 1 / 0 < k_{p2} < 1$. However, it is not possible to get valid k_{p1} and k_{p2} i.e., $k_{p1}, k_{p2} \in (0,1)$ for all power factors angle (φ) for a given modulation index. Figure 4-2 depicts k_{p1} and k_{p2} values for different lagging power factor angles (φ) with two modulation indices $m = 2/3$ and $m = 0.98$. For example, when $m = 2/3$ and φ =30º, the NP voltage can be controlled by NTV modulation in the regions 60º-90º and θ_{a1}-120º. In this case, k_{p1} and k_{p2} are also used in triangle T_1. However, when modulation

index is increased to $m = 0.98$, NP voltage is controllable by NTV in the regions 60º- θ_{a2} and θ_{a3}-120º only. Moreover, as the power factor angle is increased to φ =60º the controllable regions are further decreased as 60º-90º and θ_{b1}-120º for $m = 2/3$ and 60º- θ_{b2} and θ_{b3}-120º for $m = 0.98$.

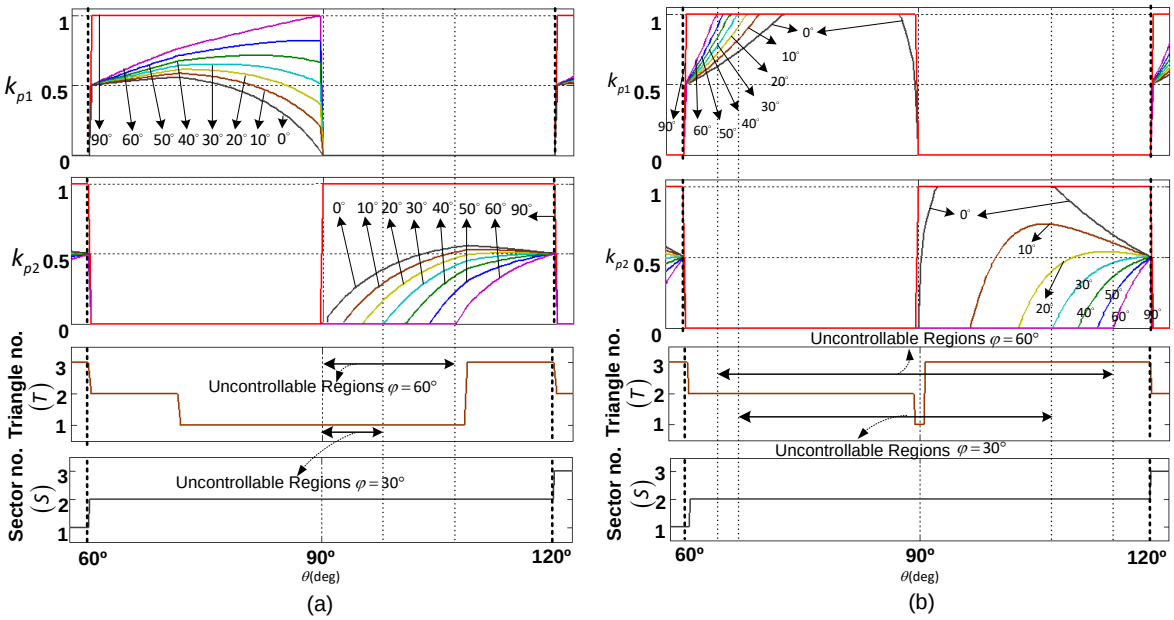


Figure 4-2 Plot of k_{p1} and k_{p2} for different lagging power factor angles (φ) when modulation index is (a) $m = 2/3$ and (b) $m = 0.98$.

(Note: In Figure 4-2, k_{p1} and k_{p2} are made to saturate manually by the algorithm once they have reached the boundary values 0 (Zero) and 1. In the leading power factor operation, k_{p1} and k_{p2} will interchange their behavior).

Figure 4-3 shows the percentage duration of NTV modulation as a function of m and φ (lagging) in a fundamental cycle to eliminate NP voltage oscillations. For a given φ, as m increases, the % NTV sharing to eliminate NP voltage oscillations are decreases. Similarly, for given m, as φ moves towards 90º, the NTV share decreases. In other words, if % NTV is in between 0% to 100% for a given operating points, non-NTV modulations like STV is also needed to control the NP voltage. The plot is not shown for lower modulations indices $(0 \le m \le 0.5)$ as this region is fully controllable with NTV modulation.

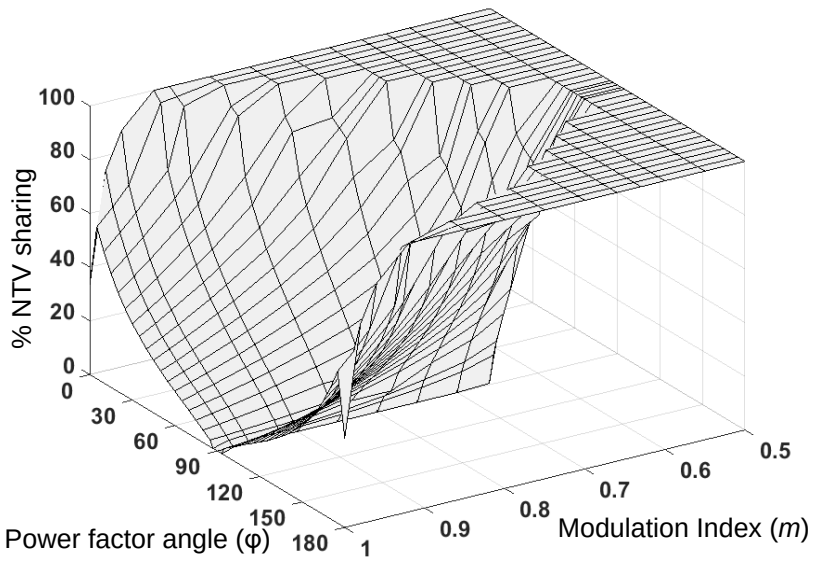


Figure 4-3 Percentage duration of NTV operation in each fundamental cycle to eliminate NP voltage oscillations as a function of m and φ (lagging).

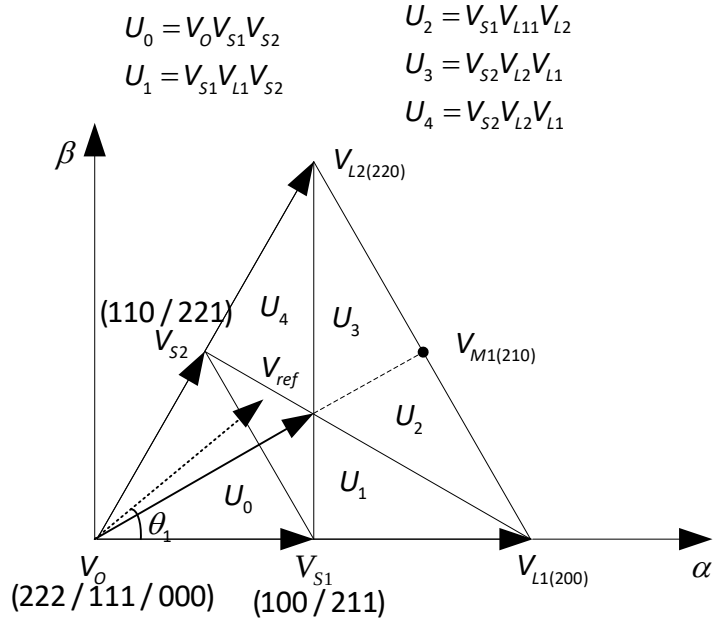


Figure 4-4 Sector-1 of 3L NPCI divided into (a) STV triangle regions and (b) NTVV triangle regions.

As discussed in the previous chapter, the non-NTV methods like STV[79] and NTVV [78] modulations can eliminate the NP voltage oscillations for complete range of m and φ. However, these methods do not use nearest voltage vectors to synthesize V_{ref} resulting in increased THD and switching losses. Moreover, these methods are more complex compared to NTV methods.

The first sector of SVD of STV modulation is shown in Figure 4-4 (a). Only three voltage vectors are used to control the NP current and the medium vector is completely avoided. Depending on the position of V_{ref} , voltage vectors of any one of the triangles $U_0 - U_4$ are selected.

4.3 Proposed Hybrid Modulation Approach

The hybrid modulation strategy uses the ability of NTV and non-NTV modulations to control the NP voltage oscillations by selecting one of these two modulations in each sampling period depending on the operating power factor (φ) and the instantaneous sampled V_{ref} position. The selection criteria described in Table 4-2 is used in the hybrid modulation algorithm since it can avoid the frequent switching between NTV and STV modulations and also maximizes the NTV operation within each fundamental cycle.

Table 4-2 Selection criteria for choosing the Type of modulation (θ_1 is the angle of V_{ref} with in the sector)

Selection criteria		NP voltage controllability by NTV modulation	Type of modulation selected
$\theta_1 \leq 30°$	$0 < k_{p1} < 1$	Controllable	NTV
	$k_{p1} = 1/0$	Uncontrollable	Non-NTV
$\theta_1 > 30°$	$0 < k_{p2} < 1$	Controllable	NTV
	$k_{p2} = 1/0$	Uncontrollable	Non-NTV

4.3.1 Duty Ratios Relations Between NTV and Non-NTV modulations

From Table 4-2, it is clear that the selection criteria (k_{p1} and k_{p2}) requires NTV duty ratios which are calculated at the start of each sampling period for a given V_{ref} . For this reason, the duty ratios of non-NTV modulation are expressed in terms of NTV duty ratios in order to perform non-NTV modulation. This process forms the basis for the proposed algorithm discussed in Section 4.4 which completely omits any separate complex non-NTV calculations for generating hybrid modulation.

4.3.1.1 STV Modulation with Redistributed NTV Duty Ratios

In order to find the relation between the NTV and STV duty ratios, a new virtual medium vector V'_M is defined based on the concept of virtual vectors [134], as

$$V'_M = \frac{V_{L1} + V_{L2}}{2} \tag{4.6}$$

Since $V_M^{'}$ is synthesized by using long vectors V_{L1} and V_{L2} (Figure 4-5 (a)), and will not affect the NP Voltage.

For V_{ref} shown in Figure 4-5 (b), NTV modulation uses triangle T_2 while, STV modulation uses triangle U_1. Based on coordinate system geometry [122],[135], the duty ratios of vectors are expressed as the length of the projections from V_{ref} to the sides of triangle. Assuming the height of NTV triangle T_2 is of unity, the duty ratios of NTV are l,m and n for V_{S1},V_M and V_{L1} respectively as depicted in Figure 4-5 (b). Similarly, by drawing projections from V_{ref} to the sides of STV triangle T_1, the duty ratios of V_{S2} and V_{L1} corresponding to STV modulation are directly obtained as m and $1-l$ respectively. Finally, as the sum of duty ratios is equal to unity, the duty ratio of V_{S1} of U_1 is given by $l-m$.

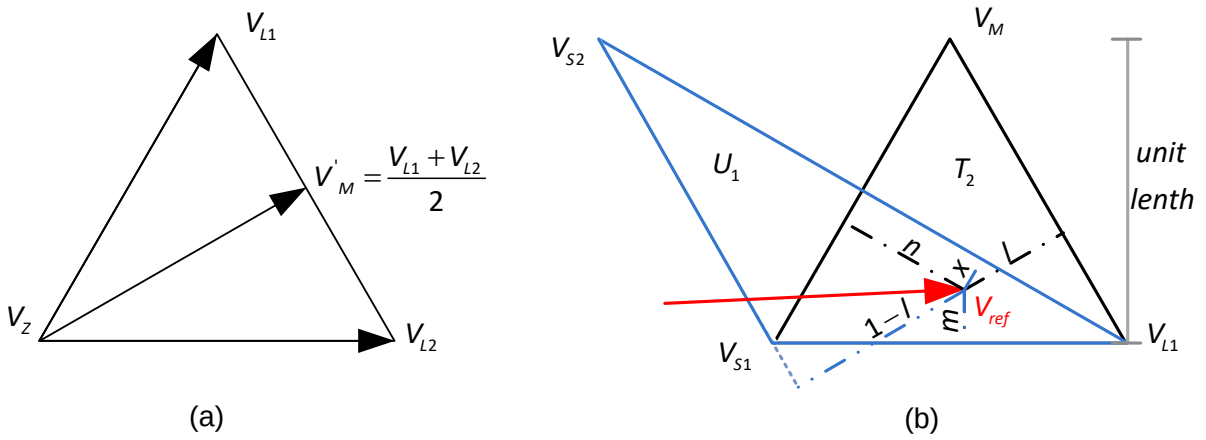


Figure 4-5 Relation between NTV and non-NTV duty ratios: (a) Virtual medium vector $V_M^{'}$ formed by two long vectors V_{L1},V_{L2}, (b) Duty ratio relations between NTV and STV triangles.

Now, by using the previous analysis and the virtual medium vector $V_m^{'}$ in (4.6), the redistribution of duty ratios from NTV to STV will be established as follows. $0\le\gamma\le30^\circ$ As $0\le\gamma\le30^\circ$ and $30^\circ<\gamma\le60^\circ$ are mirror images w.r.t the line $\gamma=30^\circ$. Hence, the redistribution is explained only for $0\le\gamma\le30^\circ$.

Case-1 ($T_2\rightarrow U_1$): For , the volt-sec balancing equation is given by

$$\begin{aligned} d_{S1}V_{S1}+d_{L1}V_{L1}+d_MV_M&=V_{ref}\\ d_{S1}+d_{L1}+d_M&=1 \end{aligned} \tag{4.7}$$

As explained previously (see Figure 4-5 (b)), the STV duty ratios are expressed in terms of NTV duty ratios and the new volt-sec balancing equation for U_1 is given by

$$(d_{S1}-d_M)V_{S1}+d_MV_{S2}+(1-d_{S1})V_{L1}=V_{ref} \tag{4.8}$$

Equation (4.8) is valid only for shaded region of Figure 4-6(a) in which as V_{ref} is nearer to V_{S1} compared to V_M and the inequality (4.9) holds good to guaranty the positive duty ratios.

$$d_{S1}\geq d_M \tag{4.9}$$

In other words, the inequality (4.9) also helps in identifying the STV triangle. i.e., if the two NTV duty ratios satisfy the relation, V_{ref} must be located in STV triangle U_1.

Case-2 ($T_2 \rightarrow U_2$): By substituting V'_M from (4.6) (Figure 4-5 (a)) in (4.8),

$$d_{S1}V_{S1}+d_M\left(\frac{V_{L1}+V_{L2}}{2}\right)+d_{L1}V_{L1}=V_{ref} \tag{4.10}$$

By rearranging (4.10), a new STV volt-sec balancing equation for U_2 is obtained as

$$d_{S1}V_{S1}+\left(\frac{d_M}{2}\right)V_{L2}+\left(d_{L1}+\frac{d_M}{2}\right)V_{L1}=V_{ref} \tag{4.11}$$

Though, (4.11) is valid for V_{ref} located in entire T_2, it can be used only for the non-shaded region of T_2 shown in Figure 4-6(a).

Case-3 ($T_1 \rightarrow U_1$): The volt-sec balancing equation for T_1 (Figure 4-6(c)) is given by

$$\begin{gathered} d_{S1}V_{S1}+d_{S2}V_{s2}+d_MV_M=V_{ref} \\ d_{S1}+d_{S2}+d_M=1 \end{gathered} \tag{4.12}$$

Similar to *Case-1*, the volt-sec balance equation for STV triangle U_1 is given by

$$(d_{S1}-d_M)V_{S1}+d_MV_{L1}+(1-d_{S1})V_{S2}=V_{ref} \tag{4.13}$$

Note that, the relation (4.9) is still valid.

Case-4 ($T_1 \rightarrow U_2$): Similar to *Case-1* and *Case-3*, inequality condition for the region shaded in Figure 4-6(d) is given by

$$d_M\geq d_{S2} \tag{4.14}$$

Now, by using (4.12) and (4.14), let us first synthesize V_{ref} by using the triangle formed by V_{S1}, V_{L2} and V_M as

$$(d_M-d_{S2})V_M+d_{S2}V_{L2}+(1-d_M)V_{S1}=V_{ref} \tag{4.15}$$

By substituting V'_M (4.6) (Figure 4-5 (a)) in (4.15),

$$(d_M - d_{S2})\left(\frac{V_{L1}+V_{L2}}{2}\right)+d_{S2}V_{L2}+(1-d_M)V_{S1}=V_{ref} \tag{4.16}$$

After rearrangement and simplification,

$$\left(\frac{d_M - d_{S2}}{2}\right)V_{L1}+\left(\frac{d_M + d_{S2}}{2}\right)V_{L2}+(1-d_M)V_{S1}=V_{ref} \tag{4.17}$$

The above analysis shows that STV triangles and the duty ratios are easily obtained from known NTV duty ratios. The expressions for STV duty ratio in terms of NTV duty ratios for the entire sector-1 are summarized, in Table 4-3. The approach discussed above can be extended to any other non-NTV methods [78], [83]–[85] easily.

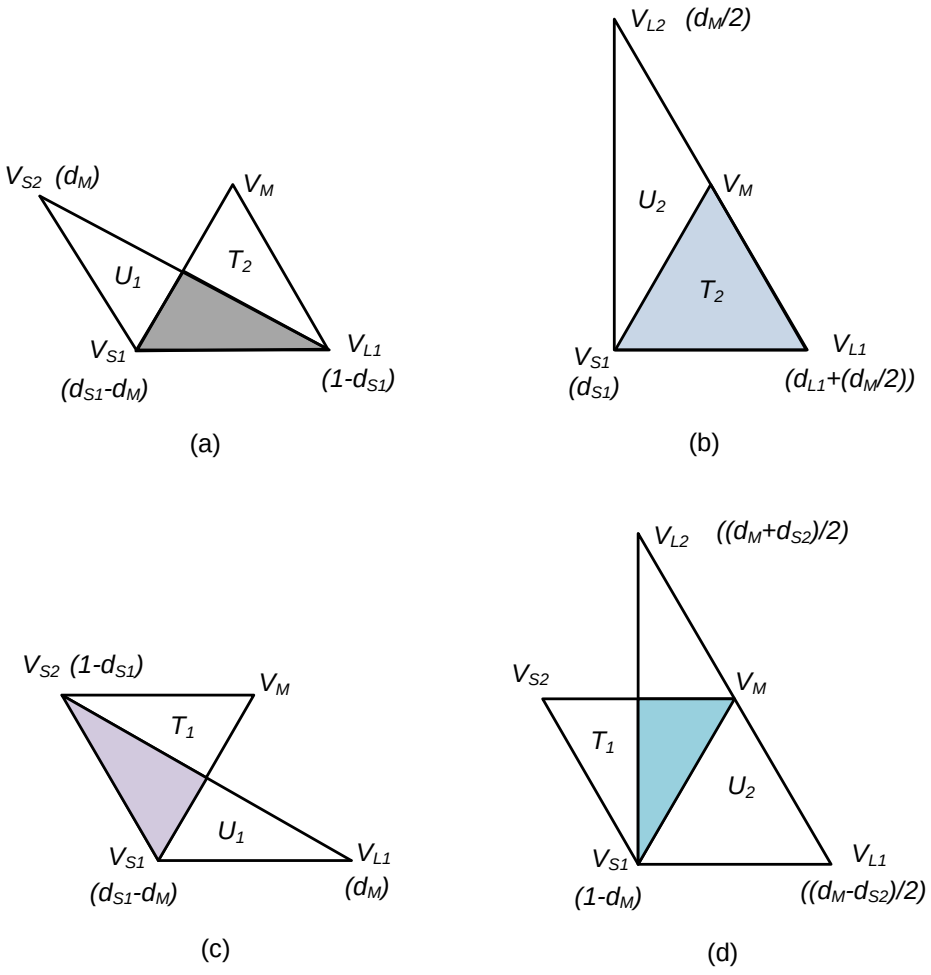


Figure 4-6 Distribution of NTV duty ratios to STV triangles for the region $0 \le \gamma \le 30^\circ$ (a) $T_2 \to U_1$ (b) $T_2 \to U_2$ (c) $T_1 \to U_1$ *and (d)* $T_1 \to U_2$.

Table 4-3 STV duty-ratios in terms of NTV duty-ratios

	Case	Redistribution of NTV duty ratios to STV modulation		
$\theta_1 \le 30°$	$T_2 \to U_1$	$d'_{S1} = d_{S1} - d_M$	$d'_{S2} = d_M$	$d'_{L1} = 1 - d_{S1}$
	$T_2 \to U_2$	$d'_{S1} = d_{S1}$	$d'_{L2} = \frac{d_M}{2}$	$d'_{L1} = d_{L1} + \frac{d_M}{2}$
	$T_1 \to U_1$	$d'_{S1} = d_{S1} - d_M$	$d'_{L1} = d_M$	$d'_{S2} = 1 - d_{S1}$
	$T_1 \to U_2$	$d'_{L1} = \frac{d_M - d_{S2}}{2}$	$d'_{L2} = \frac{d_M + d_{S2}}{2}$	$d'_{S1} = 1 - d_M$
$\theta_1 > 30°$	$T_1 \to U_3$	$d'_{L2} = \frac{d_M - d_{S1}}{2}$	$d'_{L1} = \frac{d_M + d_{S1}}{2}$	$d'_{S2} = 1 - d_M$
	$T_1 \to U_4$	$d'_{S2} = d_{S2} - d_M$	$d'_{L2} = d_M$	$d'_{S1} = 1 - d_{S2}$
	$T_3 \to U_3$	$d'_{S2} = d_{S2}$	$d'_{L1} = \frac{d_M}{2}$	$d'_{L2} = d_{L2} + \frac{d_M}{2}$
	$\Delta_3 \to T_4$	$d'_{S2} = d_{S2} - d_M$	$d'_{S1} = d_M$	$d'_{L2} = 1 - d_{S2}$

4.4 Implementation of Redistribution-Based Hybrid Modulation Algorithm

From the above discussion, it clear that, any non-NTV modulation can be easily implemented with the redistributed NTV duty ratios, so only NTV duty ratios are to be obtained for the given V_{ref}. k_{p1} and k_{p2} are calculated from NTV duty ratios and measured phase currents (equations (4.3) and(4.5)). If $k_{p1}\,\&\,k_{p2} = 1/k_{p1}\,\&\,k_{p2} = 0$ (NTV modulation fails), non-NTV modulation is implemented with the help of redistributed duty ratios (Table 4-3). Figure 4-7 shows the block diagram of the proposed hybrid NTV-STV algorithm. It is a simple NTV modulation algorithm with an updated mapping unit to incorporate STV switching states. Note that, in the existing hybrid modulations, first NTV duty ratios are calculated, but if NTV condition fails (for example, in [131], if $i_{\mathrm{NP,lo}} > 0$ and $i_{\mathrm{NP,hi}} < 0$), the non-NTV algorithm must be executed for the sampled V_{ref} as given in [79] [82].

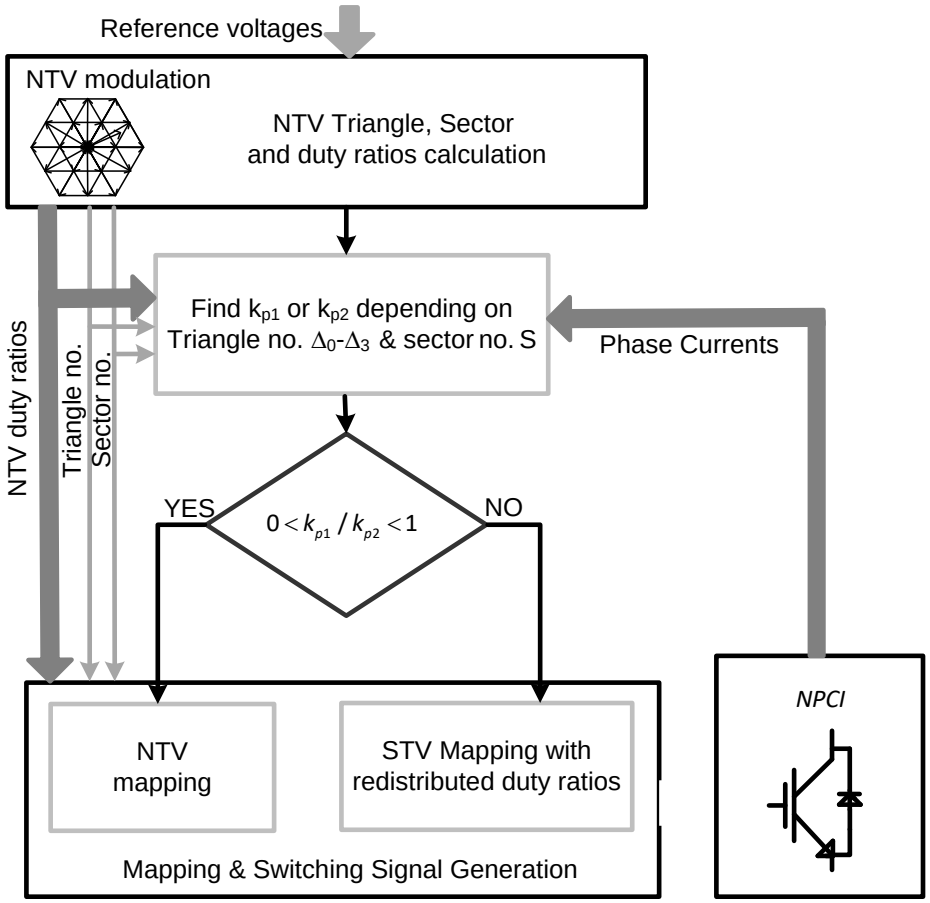


Figure 4-7 Block diagram of the proposed hybrid modulation algorithm.

To exemplify the proposed hybrid modulation algorithm shown in Figure 4-7, a 60º based SVM to find NTV duty ratios is selected. The three-phase quantities are transformed on to stationary non-orthogonal coordinate system ($g-h$ plane) which are further transformed to sector-1 as in [54], [67] is shown in Figure 4-8(a).

For given $V_{ref} = (V_{ref}^g, V_{ref}^h)$, let

$$\left.\begin{aligned} k_1 &= \text{int}(V_{ref}^g);\ k_2 = \text{int}(V_{ref}^h);\ k_3 = \text{int}(V_{ref}^g + V_{ref}^h); \\ k_4 &= \text{int}(V_{ref}^g + \frac{V_{ref}^h}{2});\ k_5 = \text{int}(\frac{V_{ref}^g}{2} + V_{ref}^h) \end{aligned}\right\} \tag{4.18}$$

It is to be noted that k_4 and k_5 are not used in the proposed algorithm. However, they are only used to distinguish the STV triangle regions in the SVD.

The location of V_{ref} is identified by using triangle number, given by

$$T_{NTV} = k_1 + 2k_2 + k_3 \tag{4.19}$$

A new coordinate system ($g1-h1$ plane) is obtained by shifting the origin as follows.

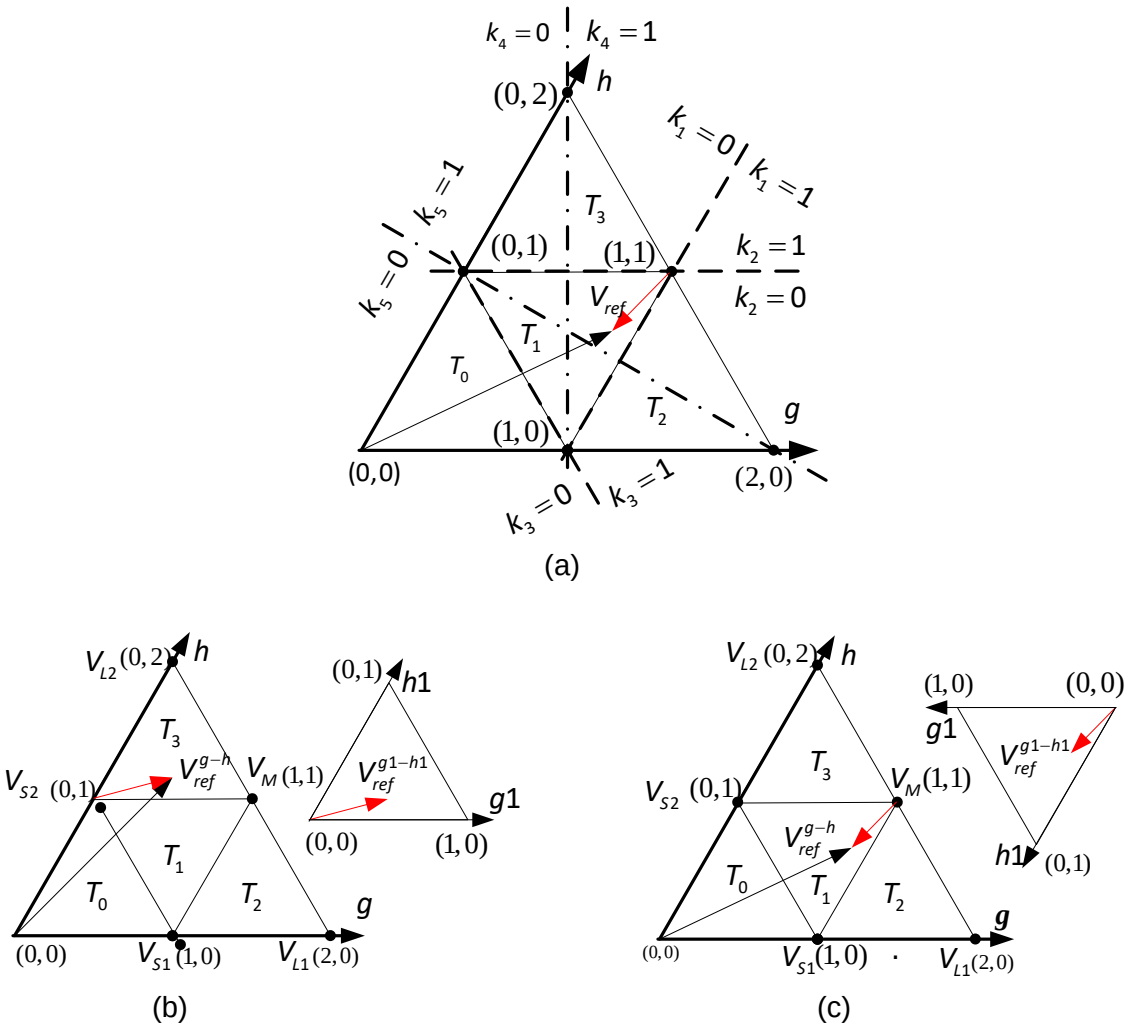


Figure 4-8 First sector of space vector diagram 60º coordinate system. (a) Representation of variables in $g-h$ plane, (b) Transformation from $g-h$ plane to $g1-h1$ plane for T_0, T_2, T_3 and (c) Transformation from $g-h$ plane to $g1-h1$ plane for T_1.

For $T_{NTV}=0,2,3$ the new origin is (k_1,k_2) and the coordinates of V_{ref} are given by

$$\begin{bmatrix} V_{ref}^{g1} \\ V_{ref}^{h1} \end{bmatrix} = \begin{bmatrix} V_{ref}^{g} \\ V_{ref}^{h} \end{bmatrix} - \begin{bmatrix} k_1 \\ k_2 \end{bmatrix} \tag{4.20}$$

Similarly, for $T_{NTV}=1$ the new origin is (k_3,k_3) and the coordinates of V_{ref} are given by

$$\begin{bmatrix} V_{ref}^{g1} \\ V_{ref}^{h1} \end{bmatrix} = \begin{bmatrix} k_3 \\ k_3 \end{bmatrix} - \begin{bmatrix} V_{ref}^{g} \\ V_{ref}^{h} \end{bmatrix} = \begin{bmatrix} 1-V_{ref}^{g} \\ 1-V_{ref}^{h} \end{bmatrix} \tag{4.21}$$

Now, the 3L SVD is converted into two-level SVD as shown in Figure 4-8 (b) and (c). NTVs coordinates for $V_{ref}(V_{ref}^{g1}, V_{ref}^{h1})$ in the new coordinate system are given in Table 4-4.

Table 4-4 NTVs and their coordinates in $g-h$ plane and $g1-h1$ plane

NTVs	*Before transformation*		*After transformation*
	T_{NTV}=0,2,3	*T_{NTV}=1*	
V_0	(k_1, k_2)	$(k_3, k_3) = (1,1)$	$(0,0)$
V_1	$(k_1 + 1, k_2)$	$(k_3 - 1, k_3) = (0,1)$	$(1,0)$
V_2	$(k_1, k_2 + 1)$	$(k_3, k_3 - 1) = (1,0)$	$(0,1)$

Therefore, the volt-sec balance equation in vector form is given by

$$\begin{bmatrix} V_0^{g1} & V_1^{g1} & V_2^{h1} \\ V_0^{h1} & V_1^{h1} & V_2^{h1} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} d_0 \\ d_1 \\ d_2 \end{bmatrix} = \begin{bmatrix} V_{ref}^{g1} \\ V_{ref}^{h1} \\ 1 \end{bmatrix}. \tag{4.22}$$

By substituting coordinates from Table 4-4 in (4.22), the NTV duty ratios are obtained as

$$d_1 = V_{ref}^{g1};\ d_2 = V_{ref}^{g1};\ d_0 = 1 - V_{ref}^{g1} - V_{ref}^{g1} \tag{4.23}$$

The NTV duty ratios for all possible locations of V_{ref} are directly obtained for the equation (4.23) . Now, from NTV duty ratios and T_{NTV} (4.19), the selection criteria is checked to choose NTV or STV modulation to eliminate NP voltage oscillations. A detailed flow chart of the proposed hybrid modulation algorithm is shown in Figure 4-9. Depending on V_{ref} location, either k_{p1} or k_{p2} is calculated from duty ratios and phase currents. If they are within the limit, the NTV modulation is implemented, otherwise STV is implemented using the redistribution duty ratios (Table 4-3) in the 'Mapping & Switching Signal Generation unit' to generate the gating signals [67].

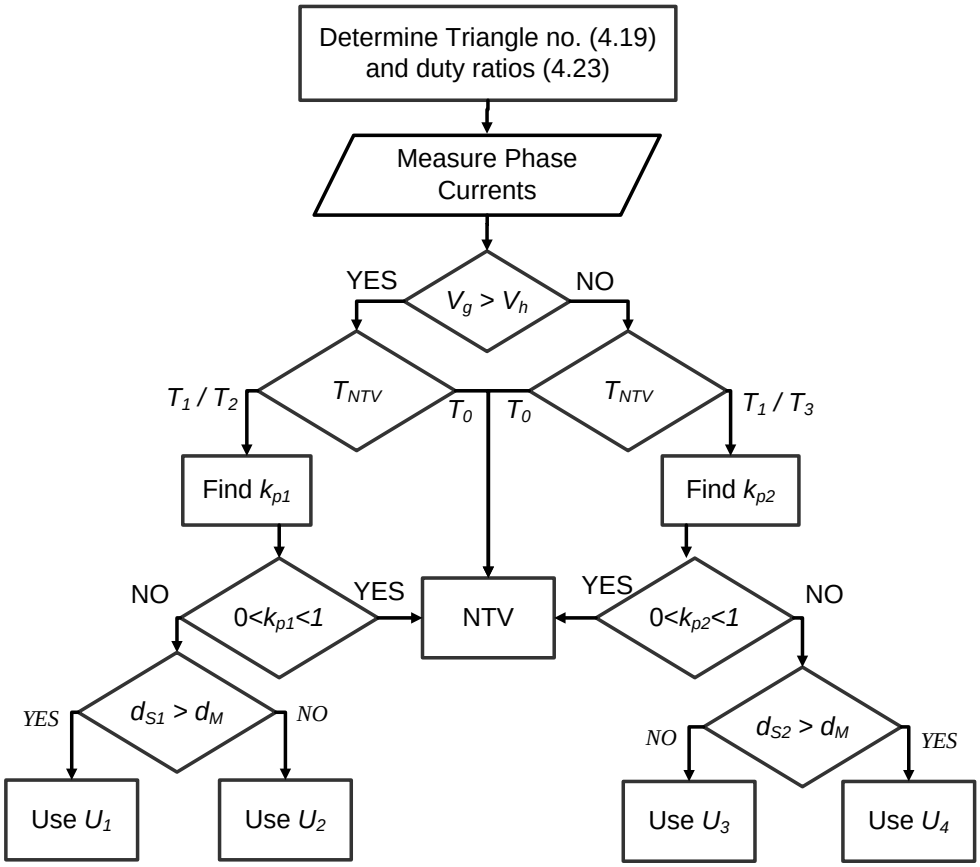
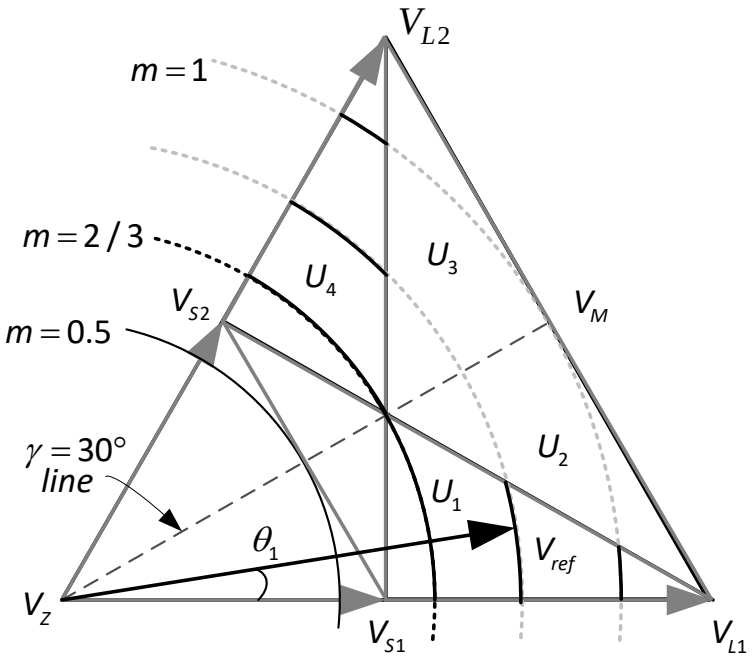


Figure 4-9 Block diagram of the proposed hybrid modulation algorithm for NTV-STV.

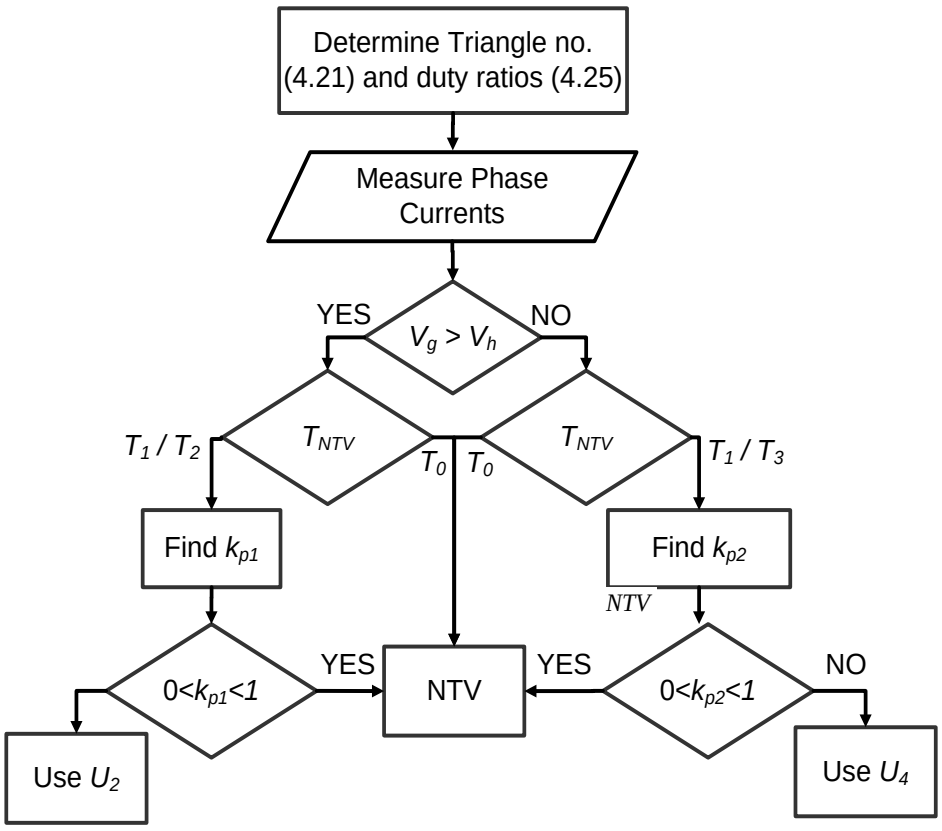
It is to be noted that, the system of linear equations or matrix inverse is not required to find the NTV duty ratios (4.23) which reduces the computational burden. On the other hand, in the conventional approaches, the duty ratios of the STV are directly calculated (either by using g-h / g1-h1 coordinate system shown in Figure 4-8). In this case, the system of linear equations depends on V_{ref} location and will not get simplified as in case of NTV modulation. Moreover in order to find the location of V_{ref}, k_4 and k_5 from (4.18) are also needed. This process requires extra steps to find the duty ratios of STV modulation. Therefore, this results in increased execution time as evaluated in section 4.6.

4.5 Hybrid NTV-SSTV Modulation Strategies

Figure 4-10(a) shows the trajectories of V_{ref} for different modulation indices. In hybrid NTV-STV modulation discussed in Section 4.4 (Figure 4-9), all STV triangles $T_1 - T_4$ are utilized for $0.5 \le m \le 1$. i.e., for V_{ref} trajectory shown in solid line, STV triangles U_1 (for $\theta_1 \le 30°$) and U_4 (for $\theta_1 > 30°$) are selected, while, for dashed part of V_{ref}, STV triangles U_2 (for $\theta_1 \le 30°$) and U_3 (for $\theta_1 > 30°$) are selected. Such selection will cause following shortcomings in hybrid NTV-STV modulation.



(a)



(b)

Figure 4-10 (a)Sector-1 of SVD representing the trajectory V_{ref} for different modulation indices. (b) Simplified algorithm (hybrid NTV-SSTV modulation) by neglecting STV triangles T_1 and T_4 for $m \geq 2/3$

1. In STV triangles U_1 / U_4, all the redundant switching states are used to eliminate the NP voltage ripple, which results in increased number of commutations and switching losses. For example, if U_1 is used, total five switching states are required (POO, ONN of V_{S1}, PPO, OON of V_{S1} and PNN of V_{L1}) to eliminate the NP voltage oscillations. However, if U_2 is used, only four switching states (POO, ONN of V_{S1}, PNN of V_{L1} and PPN of V_{L2}) are required.
2. Moreover, in hybrid NTV-STV modulation, if NTV selection criteria $(0 < k_{p1} / \mathrm{k_{p2}} < 1)$ fails and STV is selected, the switching sequence must be changed completely to accommodate five switching states of STV triangles U_1 / U_4 in "Mapping & Switching Signal Generation" unit. On the other hand, if triangles U_2 / U_3 are used, only one element is to be changed to get the STV switching sequence. (For example, PON is changed to PPN in when modulation is changed from NTV triangles T_1 / T_2 to STV triangle U_2). So, significant simplification is obtained in "Mapping & Switching Signal Generation" unit by omitting U_1 / U_4.

Furthermore, as m increases, the reference vector V_{ref} will be located in triangles U_1 and U_4 for significantly less duration, and causes frequent transition between two STV triangles as the V_{ref} progresses. On the other hand, if , (Figure 4-10(a)), V_{ref} is completely inscribed in U_2 for $\theta_1 \le 30°$ and in U_3 for $\theta_1 > 30°$. Thus, instead of using all the four STV triangles $U_1 - U_4$, only U_2 / U_3 can be used to approximate V_{ref}. Therefore, the hybrid modulation discussed above can be simplified by neglecting the two STV isosceles triangles U_1 and U_4 in each sector. The hybrid modulation formed by reduced STV triangles is named as hybrid NTV-SSTV modulation and the flow chart is shown in Figure 4-10(b). Importantly, for lower modulation indices in the range $0.5 \le m \le 2/3$, NTV can effectively control the NP voltage for all power factors angles (φ) in most of the fundamental cycle. For example, in Figure 4-2, when $m = 2/3$ and power factor angle φ=30º, the duration 90º-θ_{a1} is the only region NTV fails to control NP voltage. For this region, the algorithm can be $2/3 \le m \le 1$ e modified (not shown in figure) either to choose NTV modulation or STV modulation using only triangles U_2. Also, for $m \le 2/3$ in the complete first half of the sector ($\gamma \le 30°$), the relation $0 < k_{p1} < 1$ is valid and only NTV is required. The NTV-SSSTV combination increases voltage THD slightly reduces the switching losses as evaluated in Section 4.6.

4.6 Performance Evaluation of Hybrid Modulation Strategies

The performance of NPCI is investigated using MATLAB-Simulink (Sim Power Systems Toolbox) to study various hybrid modulations. A DC link voltage of 600 V, switching frequency 4 kHz and DC link capacitors of 110μF were used to carry out the simulation. The term "Modulation" indicates the type of modulation at given instant (Modulation=0 for NTV, Modulation=1 for STV and modulation=2 for SSTV)

Figure 4-11 and Figure 4-12 show the simulation results of NPCI for two different operating conditions. A balanced phase currents of 50A peak is flowing in each output terminal of the NPCI in both the cases. When only NTV is used (up to t=1sec), a larger third harmonic ripple can be observed in the capacitor voltages (or NP voltage). This capacitor voltage ripple will also reflect in the ac side output voltages producing low frequency harmonic content. However, when the hybrid NTV-STV modulation is used (t = 1 sec to 1.1 sec), third harmonic voltage ripple is negligible in both the operating conditions. Small oscillations still exist in the capacitor voltages due to the instantaneous non-zero phase currents flowing through small DC link capacitors of 110 μF each depending on the invert state switching state. This effect is further reduced by the proposed hybrid NTV-SSTV modulation initiated at t = 1.1sec. This is mainly because, the new SSTV uses two long vectors in each switching cycle which doesn't change NP voltages, instead of one long vector by the STV modulation when V_{ref} is located in $U_1 \& U_4$. The proposed algorithm is also functional for non-linear and un-balance loads as shown in Figure 4-13. The controllable regions of nonlinear and unbalance loads are different and are not discussed further.

The variation of output line-to-line voltage THD with respect to m and φ for different modulation methods are depicted in Figure 4-14. Clearly NTV modulation is producing less THD compared to STV and SSTV modulations. The hybrid modulations (NTV-STV and NTV-SSTV) produces THD in between the aforementioned modulation schemes. For a given operating condition, if the % NTV sharing is 100%, the THD of the hybrid modulation schemes will coincide with that of the NTV modulation. While, if the NTV sharing is 0%, the hybrid modulation will be converged to non-NTV modulation. The THD of NTV and non-TV modulations will not change with power factor. Whereas, it changes in the hybrid modulations as % NTV sharing changes with respect to power factor. Moreover, compared to NTV-STV combination, the new NTV-SSTV combination is exhibiting slightly more THD for the medium modulation indices (for $0.7 \le m \le 0.85$) is due to the selection of faraway voltage vectors forming right angle triangle regions $U_2 \& U_3$ for longer duration.

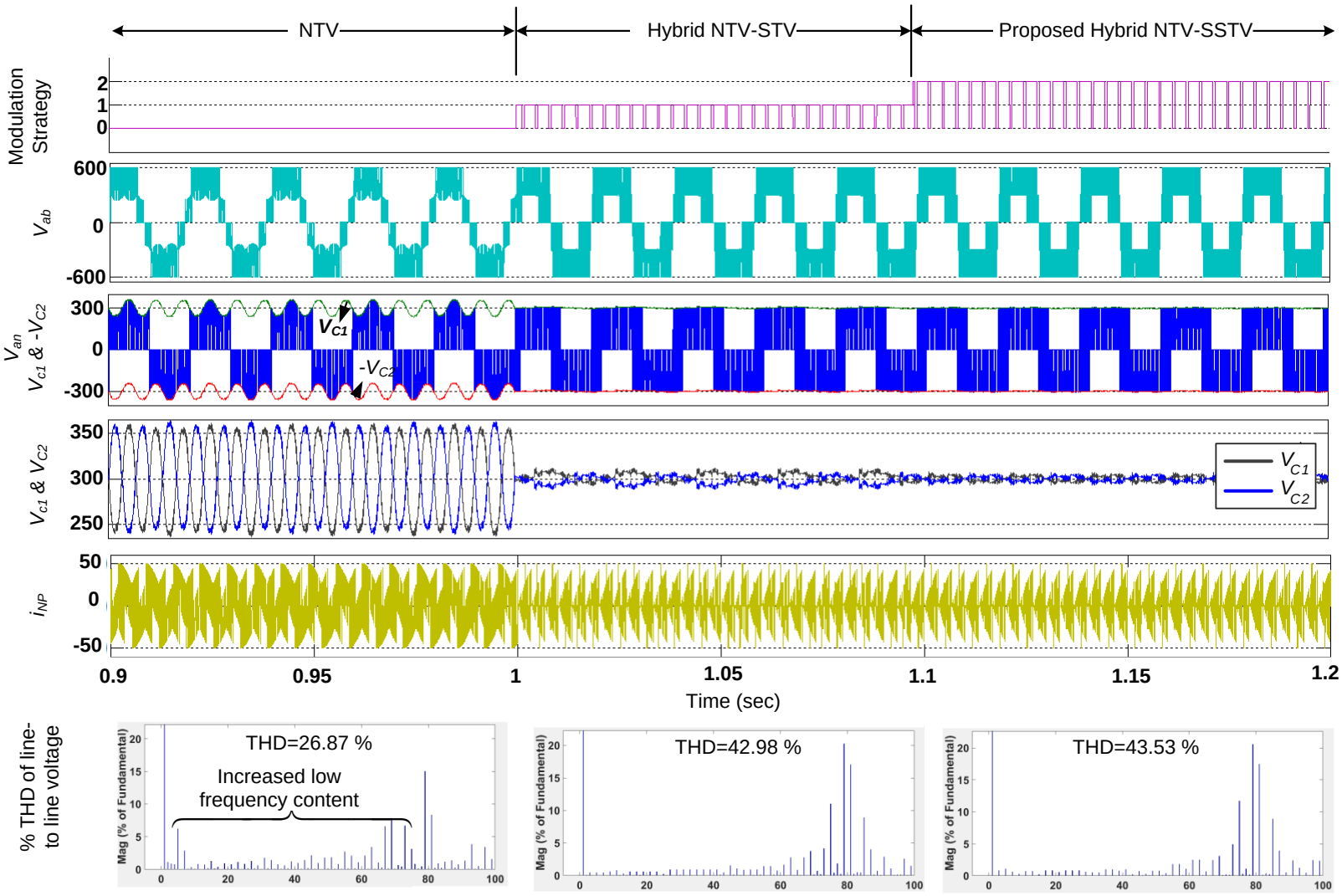


Figure 4-11 Simulation waveforms at m=0.98 and power factor 0.5 lagging (NTV sharing=14.68 %).

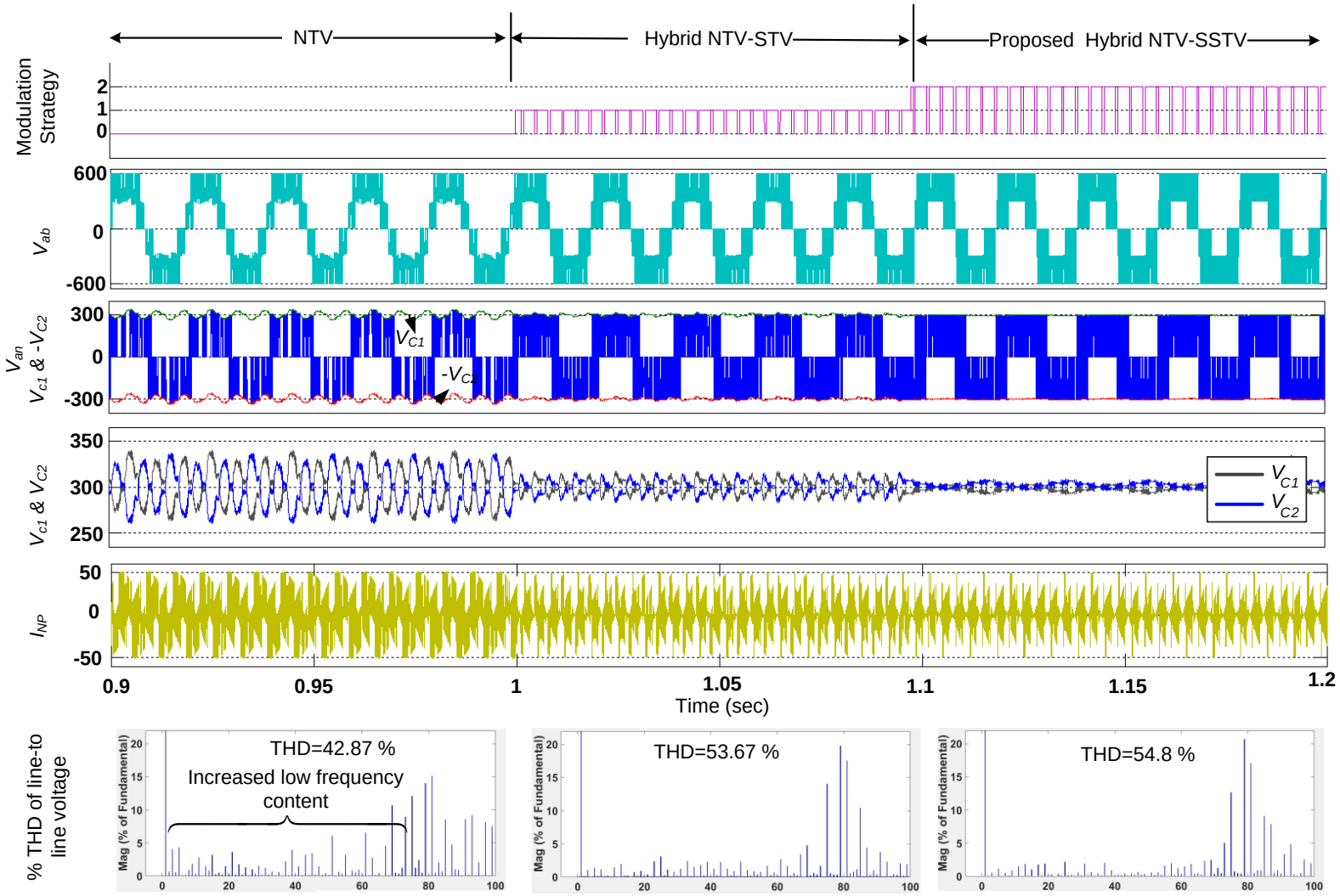


Figure 4-12 Simulation waveforms at m=0.83 and power factor 0.259 lagging (NTV sharing= 17.2 %).

The duration of operation in STV triangle regions U_1 & U_4 shrinks with the increase in modulation index. This effect is inherently present in the hybrid NTV-STV modulation and hence, the THD of two hybrid modulation will converge as the modulation index increases.

The transition from one modulation to another also shows that, there is no abrupt switching of NTV-STV/SSTV combination in a fundamental cycle. Only one forward and one reverse transition is observed in each sector, depending on modulation index and power factor. For a given m, as power factor decreases, the NTV sharing decreases and become almost negligible at ZPF. The features of the proposed redistribution algorithm summarized as follows.

1) Only one volt-sec balancing equation (for NTV) is used to generate the hybrid modulations unlike the existing hybrid modulation algorithms. Therefore, any existing NTV Algorithm and control hardware can be easily modified to generate Hybrid modulation (change in mapping unit is only required depending on non-NTV modulation).
2) The complexity and execution time are greatly reduced; therefore, it is feasible to implementation hybrid modulation strategies in low cost microcontrollers.
3) It maximizes the utilization of NTV modulation for given operation condition and avoids any abrupt transition between NTV and non-NTV modulations (only one forward and one reverse transition in each sector sector).
4) The redistribution of duty ratios is a general relation and will not be affected on the type of NTV, switching sequence etc. It only changes with the type of non-NTV modulation selected. Moreover, any criteria for NTV to non-NTV switching can be implemented.
5) The proposed hybrid NTV-SSTV modulation strategy improved the performance (minimum switching losses and execution time) compared to other existing hybrid modulations without significantly affecting the voltage THD.

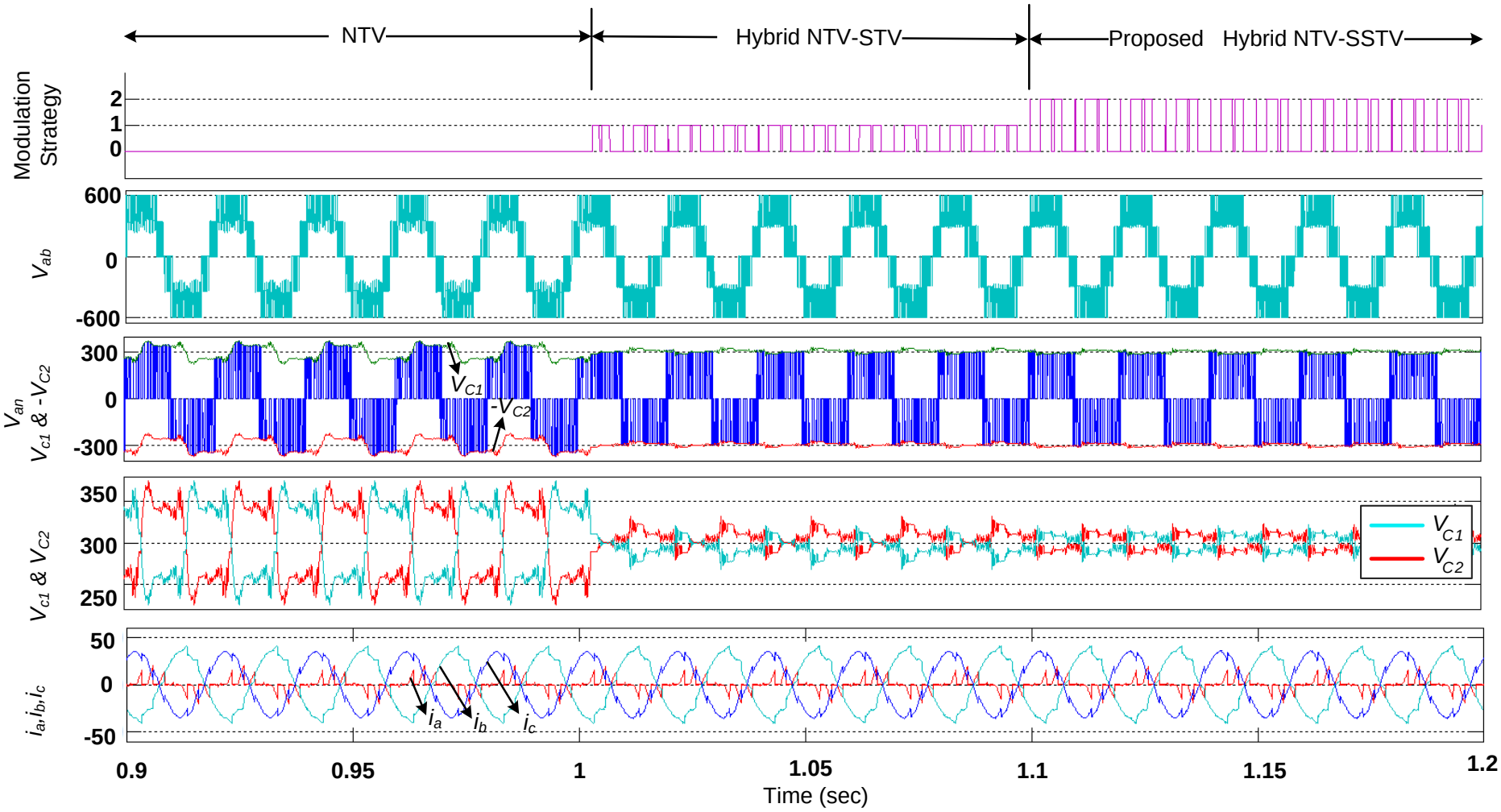
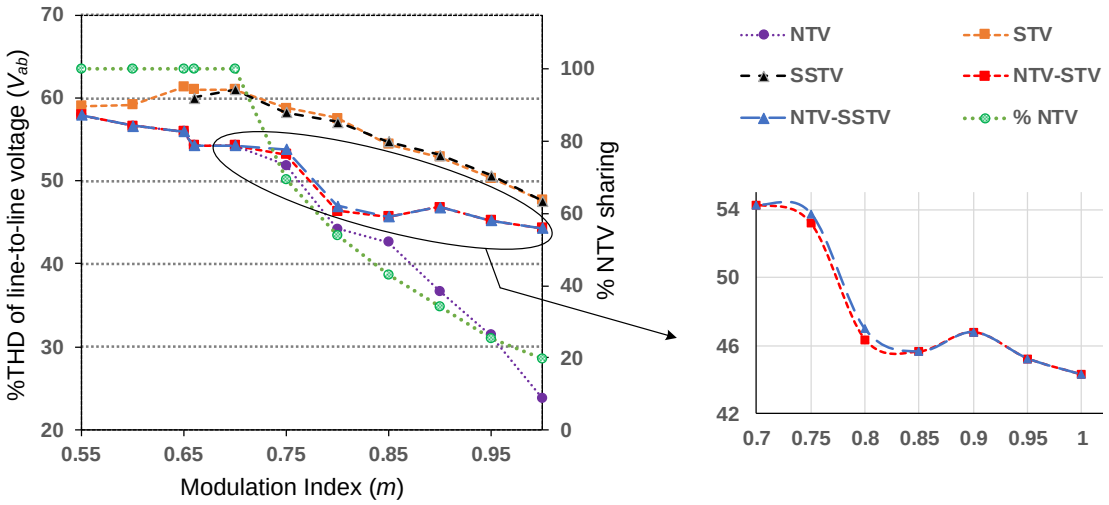
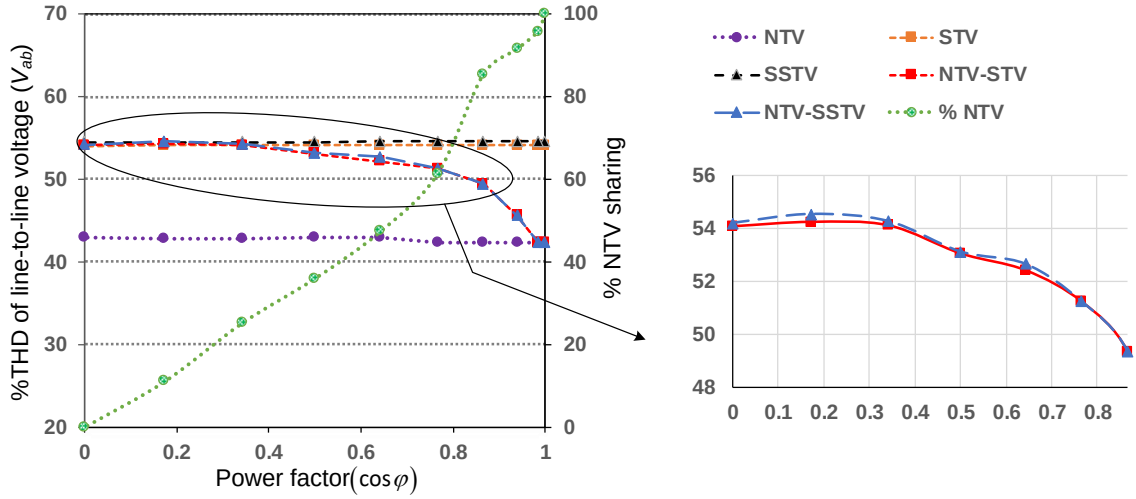


Figure 4-13 Simulation waveforms for a non-linear and un-balanced load.



(a)



(b)

Figure 4-14 Line to line voltage % THD for various modulation schemes: (a) with respect to the modulation index for power factor of 0.707 lagging. (b) with respect to power factor angle for m=0.83.

4.6.1 Comparison of Commutations and Power Losses

As discussed earlier, one of the important drawbacks of non-NTV modulations is the increased number of device commutations. The zoomed view of the waveforms Figure 4-11 and Figure 4-12 are shown in Figure 4-15. The use of five switching states in hybrid NTV-STV modulation when V_{ref} is in U_1 and U_4 results in increase in switching frequency (no. of commutations) as shown in the marked regions Figure 4-15(a) and (c). This effect is more significant if the modulation is decreased as V_{ref} is located in U_1 and U_4 for longer durations. On the other hand, if SSTV is used instead of STV, the commutations are reduced significantly as shown in Figure 4-15(b) and (d) due to the use of only four switching states. This helps in reducing the switching losses during SSTV operation compared to STV operation.

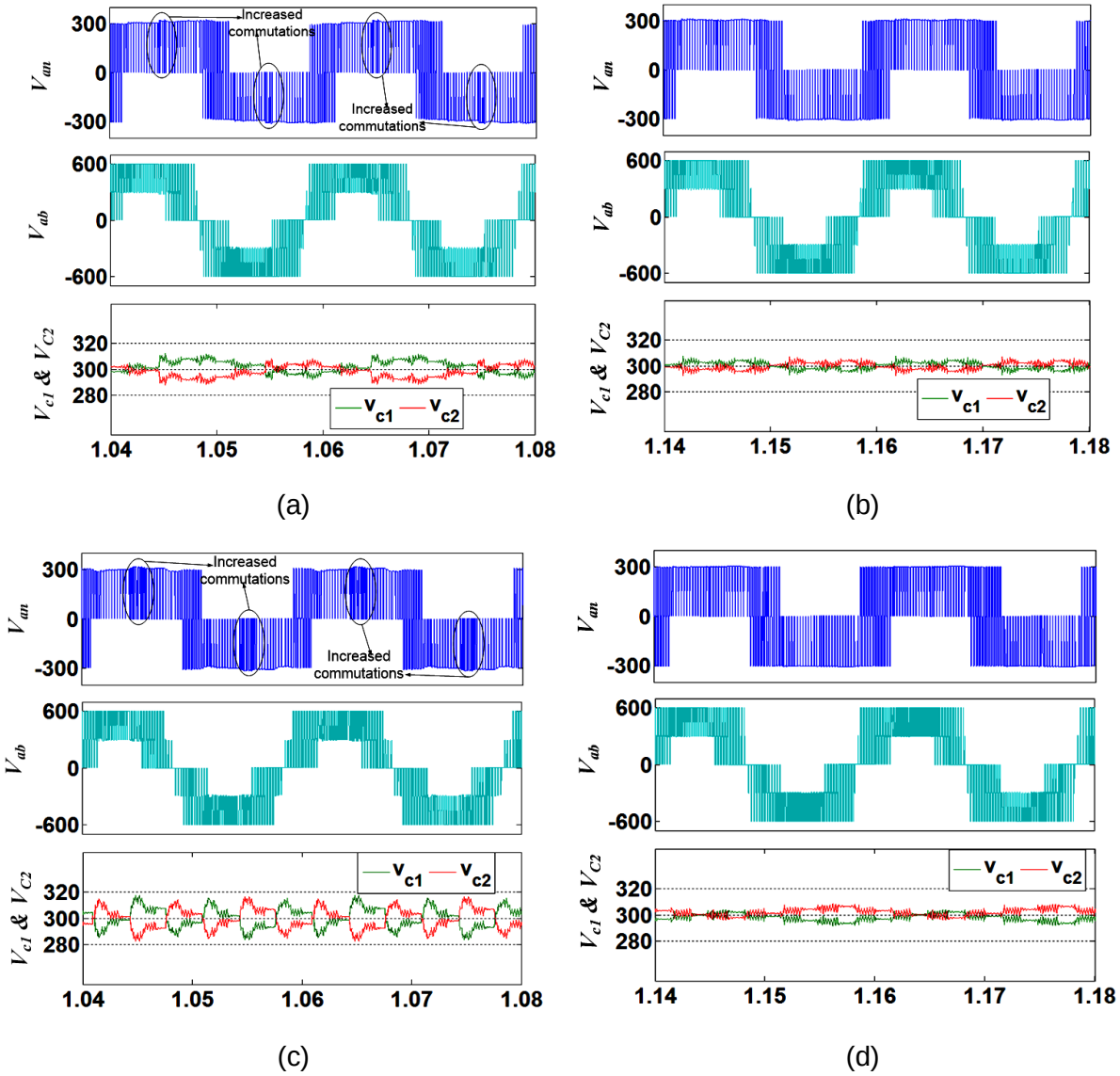


Figure 4-15 Comparison of hybrid NTV-STV and hybrid NTV-SSTV modulations: (a) hybrid NTV-STV (b) NTV-SSTV modulation for m=0.98 and power factor 0.5 lagging and (c) Hybrid NTV-STV (d) Hybrid NTV-SSTV modulation for m=0.83 and power factor 0.259 lagging.

The switching loss distribution for various modulation schemes are illustrated in Figure 4-16. The conduction losses are approximately similar for NTV and non-NTV methods and hence not considered. The losses are evaluated in the similar manner as discussed in [136] . The variation of switching losses with respect to the modulation index is negligible for NTV modulation and assumed 1per unit (pu). Figure 4-16 (a) shows the pu variation of switching losses of non-NTV and hybrid modulations with respect to NTV modulation as a function of m. The hybrid modulations produce 1 pu switching losses if the NTV sharing is 100 %. Meanwhile, as the NTV sharing decreases, the losses will increase in the hybrid modulations. However, the proposed NTV-SSTV modulation always produce either less or equal losses compared to hybrid NTV-STV modulation. Figure 4-16 (b) shows the variation of switching losses as a function of power

factor (lagging) for $m = 0.83$. The switching losses of NTV modulation yield higher value for unity power factor compared to zero power factor. Whereas non-NTV modulations takes high switching losses when φ=90º. Here also, the NTV-SSTV combination produces fewer switching losses for given operating conditions compared to hybrid NTV-STV modulation.

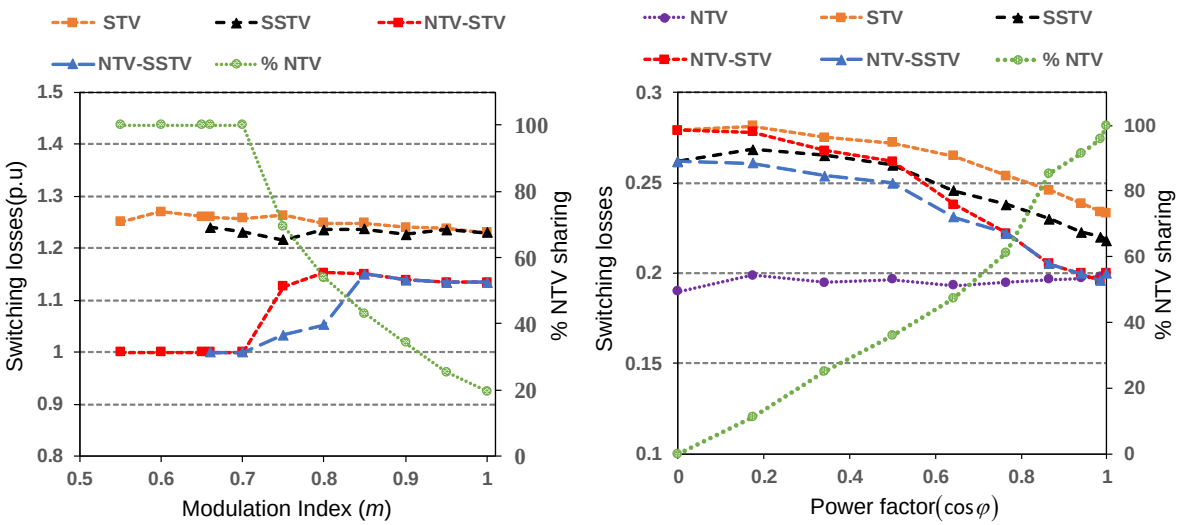


Figure 4-16 Switching losses for various modulation schemes: (a) Variation of switching losses as a function of modulation index for power factor 0.707 lagging; (b) Variation of switching losses as a function of power factor angle for m=0.83.

Note that the performance (THD and loss distribution) of NPCI with other non-NTV and hybrid modulations are either similar or mediocre, compared to the hybrid NTV-STV modulation and hence hey are omitted in the comparison.

4.6.2 Execution Time Comparison of Modulation Strategies

If the NTV sharing for eliminating low frequency NP voltage oscillations lies between 0% and 100%, non-NTV modulation need to be executed separately in each sampling cycle for implementing hybrid modulation. This results in increased execution time. On the other hand, the proposed hybrid modulation algorithm discussed in Section 4.4 is basically an NTV algorithm with an updated mapping unit and does not require complex trigonometric expressions for NTV duty ratio calculation. This results in reduced complexity and less processing power. In order to quantify the improvement in the computation time of the different algorithms, they are tested in OP5600 simulator to find the execution time. A fixed stem size of 10µSec is used to carry out the study. Table 4-5 compares the execution time of various algorithms. The conventional hybrid NTV-STV modulation algorithm [131] is performed such that, if NTV condition fails, the STV algorithm [79] is initiated using the “enable” block in the MATLAB Simulink. The proposed hybrid NTV-STV algorithm presents a lower execution time

(comparable to NTV) and outputs same performance of NPCI as that of conventional hybrid NTV-STV modulation. The new hybrid NTV-SSTV modulation, further reduces the execution time mainly as it cuts the size of STV mapping unit by half.

Table 4-5 Execution time comparison of the modulation strategies

Modulation	Execution Time(μSec)
NTV alone	1.23
Hybrid NTV-STV modulation with independent algorithms [131]	2.41
Proposed algorithm for hybrid NTV-STV	1.7
Proposed algorithm for hybrid NTV-SSTV	1.42

4.7 Conclusion

A generalized modulation algorithm is developed in this chapter for implementation of hybrid modulation strategies based on redistribution of NTV duty ratios. The proposed hybrid modulation algorithm alternately chooses between NTV and non-NTV modulations depending on a selection criterion which is governed by NTV duty ratios and load currents. It avoids the separate non-NTV calculations and uses redistributed NTV duty ratios to implement hybrid modulation. This significantly reduces the computational burden and also enables the use of any simplified methods to obtain NTV duty ratios based on orthogonal and non-orthogonal frames of reference. The hybrid modulation can eliminate the NP voltage oscillations for entire range of modulation index and power factors similar to non-NTV methods, but producing less voltage THD and switching losses. The new hybrid NTV-SSTV modulation strategy further reduces the switching losses produced by the hybrid modulations for the medium modulation indices by using only four switching states. Though it results in slight increase in voltage THD in the high frequency range of the spectrum, it doesn't affect the current THD. Detailed simulation results show the effectiveness of the proposed modulation algorithm and the hybrid modulation strategy.

Chapter 5: HYBRID 2L/3L NPCI WITH SELF-CAPACITOR VOLTAGE BALANCING

[In this chapter, a new NPCI is presented based on the concept of non-NTV modulation discussed in previous chapters. The topology is formed by adding two half bridge modules to a 2L VSI and contains only ten active switches. It is named as hybrid 2/3 level (2/3L) inverter based on the characteristics of the output voltage and current waveforms. All the switching states of the inverter are studied and different types of voltage vector selection methods are investigated to synthesize the reference vector. The non-NTV modulation algorithms discussed in the previous chapters are further improved to generate the switching signals for hybrid 2/3L NPCI. The operation of the inverter with (1) Z-source network and (2) Unequal voltage source across the capacitors are studied in detail. Two new switching sequences for are analyzed higher modulation range, which use both the small vectors for entire modulation index range.]

5.1 Introduction

Multilevel inverters are very motivating solutions for medium voltage and high-power applications due to the advantages such as reduced voltage stress across the devices, low harmonic distortion and reduced dv/dt stress etc. On the other hand, multilevel inverters are debatable for low voltage applications like PV, battery energy storage and fuel cell systems as the voltage ratings can be easily met by the two-level inverters. This is mainly due to the fact that the multilevel topologies are often associated with complex structure and control problems with increased controlled power devices and additional passive components capacitors. Recently, various new multilevel inverters are invented addressing this problem by reducing the number of controllable switches in the multilevel topology. However, most of them are single phase structures [35] which are derived from the conventional multilevel inverter topologies like DCI, FC and CHB.

Three-level NPCI is the most common multilevel topology and it has many inherent advantages [137][138]. Buck-boost Z-source 3L NPCIs are reported with one and two Z-source impedance networks [139][140]. However, compared to two-level inverter, NPCI requires double the number of active switches, driver circuits-auxiliary components. To overcome this limitation, subsequently, to reduce the semiconductor device count, a low-cost hybrid 2/3 level (2/3L) NPCI and its modulation schemes have been investigated and reported [141]. The hybrid 2/3L NPCI can be formed by addition of only two pair of switches to a two-level (2L) inverter and hence, it can reduce the self-commutated device count by two and eliminates the requirement of six clamping diodes compared to the conventional 3L NPCI. However, due to the inherent limitations of the hybrid 2/3L NPCI, the possible switching states are reduced.

In this regard, this chapter presents the hybrid 2/3L NPCI and its modulation approaches for various operating conditions. Two modulation methods are proposed and compared. A single impedance Z-source integrated hybrid 2/3L NPCI configuration suitable for renewable energy conversion applications is presented. A new virtual vector modulation scheme is proposed. The operation of hybrid 2/3L NPCI for unequal DC-sources is investigated thoroughly with the help of a new switching sequence.

5.1 Hybrid 2/3L NPCI

Figure 5-1 shows the hybrid 2/3 level inverter. It is basically a three-level ANPC in which the three level portions are made common for all the phases. The output of the common 3L leg is connected to a conventional two-level inverter. There are two main complementary switch pairs $\left(T,\bar{T}\right)$ and $\left(B,\bar{B}\right)$ in the common 3L leg such that $T+\bar{T}=1$ and $B+\bar{B}=1$. The three switch pairs $\left(S_p,\overline{S_p}\right),\{p=a,b,c\}$ form the three-phase two-level inverter. Assuming $V_{C1}=V_{C2}=V_{DC}/2$, Table 5-1 shows the simplified single-phase switching table for the hybrid 2/3L NPCI (Taking O as reference). Here, the '1' and '0' (Zero) represents 'ON' and 'OFF' states of the corresponding switches, whereas '*X*' represents the don't care condition for obtaining the particular level. However, the exact value of *X* depends on the voltage level demanded by the other phases. The comparison of various 3L NPCI topologies is presented in Table 5-2. The reduction in active switch count as well as the total blocking voltage (TBV) [36] of hybrid 2/3L NPCI is clearly evident. The topology has simple structure and can be formed by addition of two half bridge modules to a conventional 2L VSI.

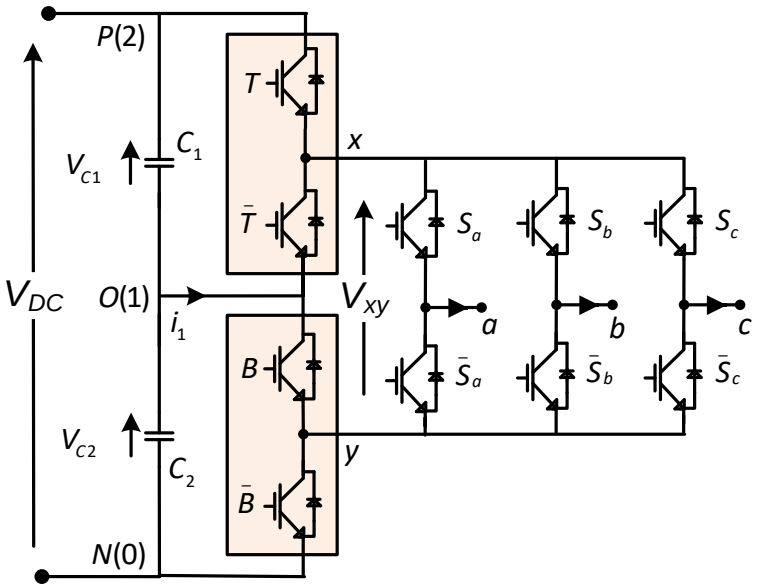


Figure 5-1 Hybrid 2/3L NPCI topology.

Table 5-1 Single phase Switching table of hybrid 2/3L NPCI ($p=a,b,c$)

Voltage	Notation	T	B	S_p
V_{C1}	2	1	X	1
0	1	0	X	1
		X	0	0
$-V_{C2}$	0	X	1	0

Table 5-2 Comparision of 3L NPCI topologies

Parameters count		Topologies		
		3L NPCI	T-Type	Hybrid 2/3L NPCI
IGBTs		12	12 (including bidirectional switches)	10
Clamping Diodes		6	0	0
Bidirectional Switches		0	3	0
Total blocking voltage (TBV) (p.u)	IGBTs	12	18	16
	Diodes	6	0	0

5.1.1 Voltage Level Generation:

Considering two intermediate points at the output of the common 3L leg: x,y for the hybrid 2/3L NPCI as shown in Figure 5-1, the possible switching combinations are listed in Table 5-3. There are three valid modes for the common 3L leg, as a result, three input voltages $V_{xy}=(V_{C1}+V_{C2})/V_{C1}/V_{C2}$ are available for the conventional two-level VSI. Based on the knowledge of 2L VSI, the SVD of hybrid 2/3L NPCI for all the three modes are depicted in Figure 5-2. Each mode of the hybrid 2/3L NPCI has 2^3=8 switching states resulting in total of $3\times8=24$ switching states. However, there are common switching states as follows:

1) Mode-1 and Mode-2 has ‘222’ common switching state.
2) Mode-2 and Mode-3 has ‘000’ common switching state.
3) Mode-1 and Mode-3 has ‘111’ common switching state.

Therefore, the total number of switching states of the hybrid 2/3L NPCI are 24-3=21.

Table 5-3 Expanded Switching table of hybrid 2/3L NPCI

T	$\bar{T}$	B	$\bar{B}$	V_{xO}	V_{yO}	$V_{xy}=V_{xO}-V_{yO}$	Mode
1	0	1	0	$V_{C1}/\frac{V_{DC}}{2}(2)$	Zero (1)	$V_{C1}/\frac{V_{DC}}{2}$	1
1	0	0	1	$V_{C1}=\frac{V_{DC}}{2}(2)$	$-V_{C2}/-\frac{V_{DC}}{2}(0)$	$V_{DC}=V_{C1}+V_{C2}$	2
0	1	0	1	Zero (1)	$-V_{C2}/-\frac{V_{DC}}{2}(0)$	$V_{C2}/\frac{V_{DC}}{2}$	3
0	1	1	0	Zero (1)	Zero (1)	Zero	-

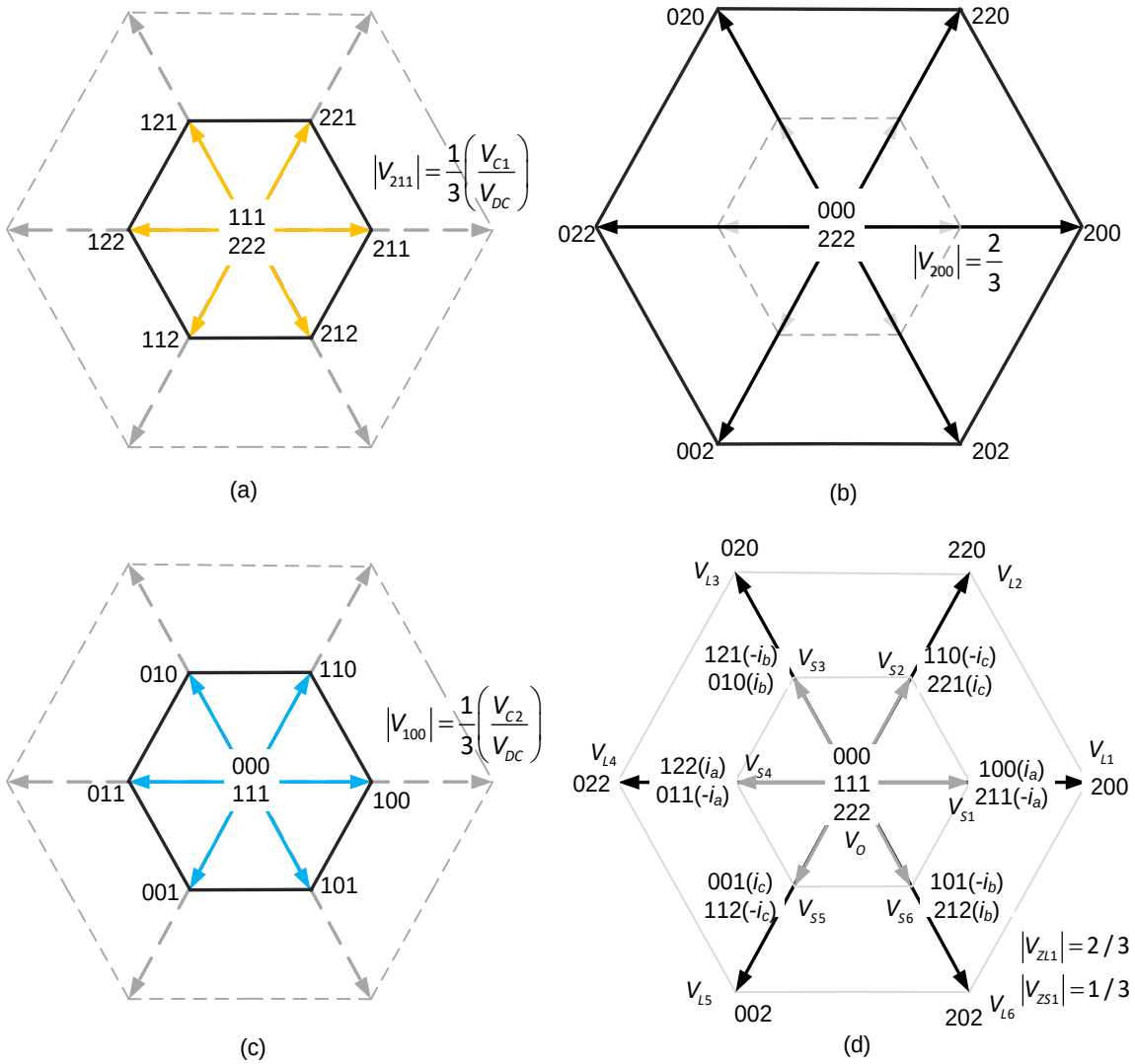


Figure 5-2 Space vector diagram of hybrid 2/3L NPCI for (a) Mode-1, (b) Mode-2 and (c) Mode-3 and (d) Total SVD.

5.1.2 SVD of Hybrid 2/3L NPCI

The complete SVD of the hybrid 2/3L NPCI can be obtained by combining all the SVDs of the three modes. Figure 5-2 (d) shows the SVD of hybrid 2/3L NPCI indicating all the 21 switching states when the two DC-link capacitor voltages are equal. There are six small vectors $(V_{S1} - V_{S6})$ with line voltage redundancy and six long vectors $(V_{L1} - V_{L6})$ without redundancy. The most important effect of making the three-level part common for all the phases is the reduction of available switching states. As compared with the 3L NPCI or ANPC, there are no medium vectors available in SVD of hybrid 2/3L NPCI SVD.

5.2 Investigation of Modulation Methods for Hybrid 2/3L NPCI

Selection of voltage vectors is not straight forward in the case of hybrid 2/3L NPCI. This is due to the absence of medium voltage vector in the SVD as shown in Figure 5-2 (d). The nearest three vector (NTV) modulation of conventional 3L NPCI or ANPC discussed in Chapter 3 is not possible in this case. Therefore, the modulation needs to choose the different set of voltage vectors depending on the position of reference voltage vector (V_{ref}). Other constraints like i) capacitor voltage balancing, iv) Minimizing the number of commutations etc, can be incorporated in the modulation. However, it can be observed that since the nearest voltage vectors are unavailable due to the circuit limitation, the modulation will always be a kind of non-NTV method. As result, the performance is expected to be in between 2L and 3L VSIs.

5.2.1 Virtual Vector (VV) Based Modulation

In this method a virtual medium vector is developed to fill the medium voltage vector location. A virtual medium vector can be formed by various combinations of available vectors. For example, a virtual medium vector formed by using two adjacent long vectors is mathematically expressed as

$$\begin{aligned} V_{Mi}^{'} &= \frac{V_{Li} + V_{\mathrm{L(i+1)}}}{2}, i = 1,2..5; \\ V_{M6}^{'} &= \frac{V_{L6} + V_{\mathrm{L1}}}{2} \end{aligned} \tag{5.1}$$

The virtual medium vector $V_{Mi}^{'}$ will exactly coincide with the actual medium vector of the 3L SVD. Total six virtual medium vectors are now introduced in the SVD of 2/3L NPCI. Therefore, the resulting space vector diagram of the 2/3L NPCI is similar to the conventional 3L SVD as shown in Figure 5-3 (a).

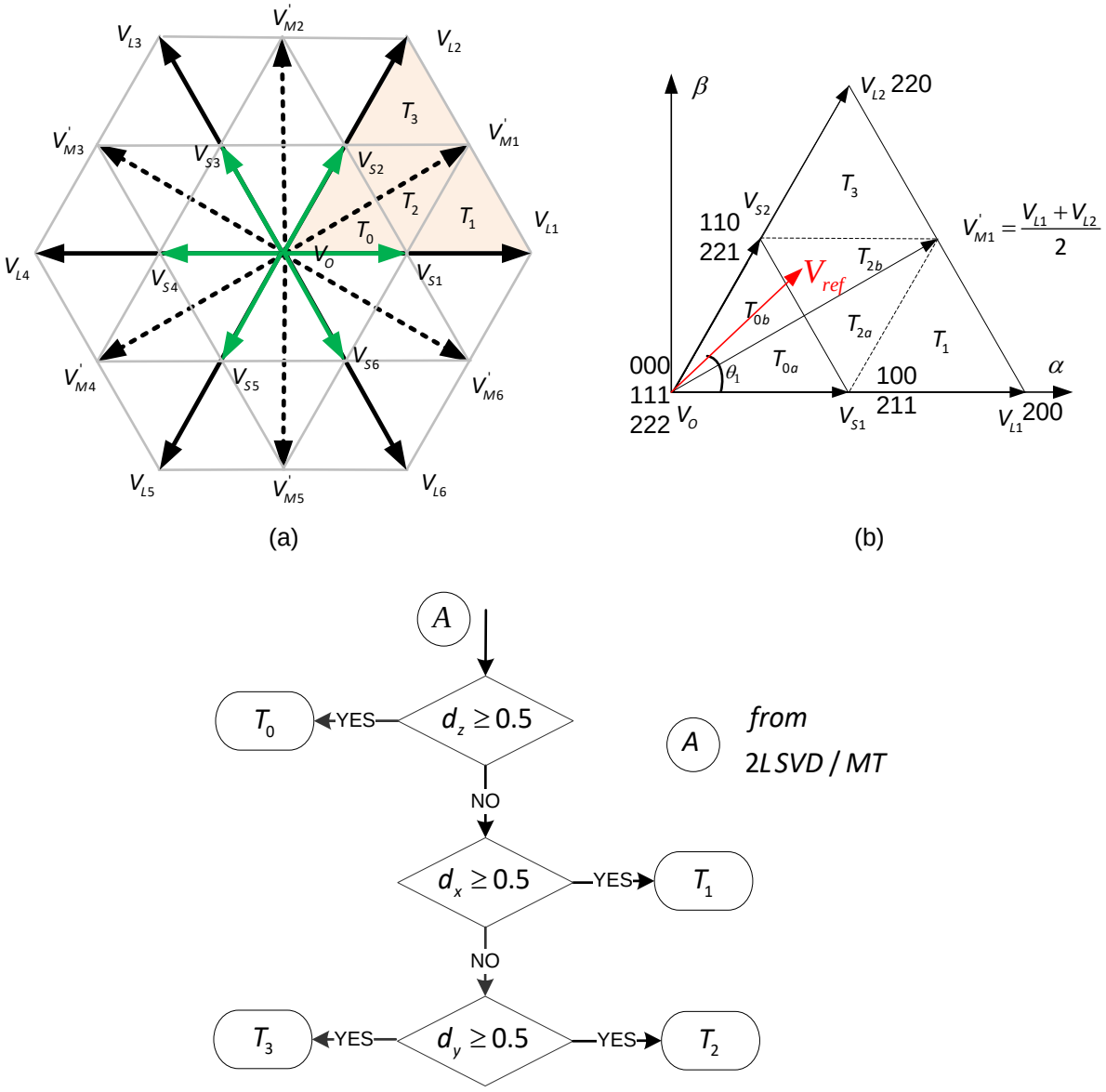


Figure 5-3 (a) SVD of hybrid 2/3L NPCI with introduction of virtual medium vectors, (b) Sector-1 of VV-based modulation and (c) flowchart for identification of sub-triangle regions.

Table 5-4 Voltage vector selection for VV-based method 1.

Triangle	Voltage vectors
T_0	V_0, V_{S1}, V_{S2}
T_1	V_{S1}, V_{L1}, V_{L2}
T_2	$V_{S1}, V_{L1}, V_{L2}, V_{S2}$
T_3	V_{S2}, V_{L2}, V_{L1}

Now, assuming the virtual medium vector similar to the other voltage vectors, any conventional SVM algorithm can be used to identify the sub-triangle regions $T_0 - T_3$ in which the V_{ref} is located. Figure 5-3 (c) shows the flowchart for identification of sub-triangle regions of virtual vector-based modulation. Where, d_x, d_y and d_z are the duty rations of equivalent 2L SVD (Refer section 3.3.2 for more details). The actual vector used to synthesize V_{ref} are not same when compared to conventional 3L NTV modulation. Since the virtual vector is a combination of more than one voltage vector, it cannot be implemented similar to the other voltage vectors. The duration of the virtual vector obtained by the volt-second balance equations are distributed to the actual voltage vectors forming the corresponding virtual vector. Based on the virtual vector given in (5.1), the actual voltage vectors of the 2/3L NPCI used for synthesis of reference vector located in sector-1 are given in Table 5-4. The duty ratios of the different voltage vectors are listed in Table 5-5 for the VV-based modulation in terms of the equivalent 2L SVD duty ratios .With the help of the six-fold symmetry of the SVD, the vector selection in the remaining sectors can be easily obtained. Clearly, the modulation uses 4 voltage vectors when reference vector is located in T_2, while 3 voltage vectors are used when it is located in the other sub-triangles of sector 1. Due to the switching state redundancy, several switching sequences are possible for the same set of voltage vectors.

Table 5-5 Duty ratios of voltage vectors of sector-1 for virtual vector-based modulation of hybrid 2/3L NPCI

Vectors	Triangles duty ratios			
	T_o	T_1	T_2	T_3
V_O	$d_z - d_x - d_y / (2d_z - 1)$	-	-	-
$V_{S1(100)}$	$2d_x$	$2d_z$	$1-2d_y$	-
$V_{S2(221)}$	$2d_y$	-		$2d_z$
$V_{L1(200)}$	-	$2d_x - 1 + d_y$	$(1-2d_z)/2$	d_x
$V_{L2(220)}$	-	d_y	$(1-2d_x)/2$	$2d_y - 1 + d_x$

Figure 5-4 shows one of the possible switching sequences when V_{ref} located in sector-1. The switching sequence is designed in a manner to minimize the number of transitions for a given magnitude and phase of V_{ref}. The switching sequence can produce symmetric waveform with quarter-wave symmetry and can maintain the capacitors voltages to oscillate around the mean $V_{DC}/2$. However, control over the capacitor voltages is limited since NP current is not-directly controlled with the selected switching sequence. This method is very simple to implement since

it is similar to the convention SVM of 3L NPCI. Duty ratios of voltage vectors of sector-1 for virtual vector-based modulation It can be observed that, the there is a jump in each phase when the transition from first half to second half of the sector.

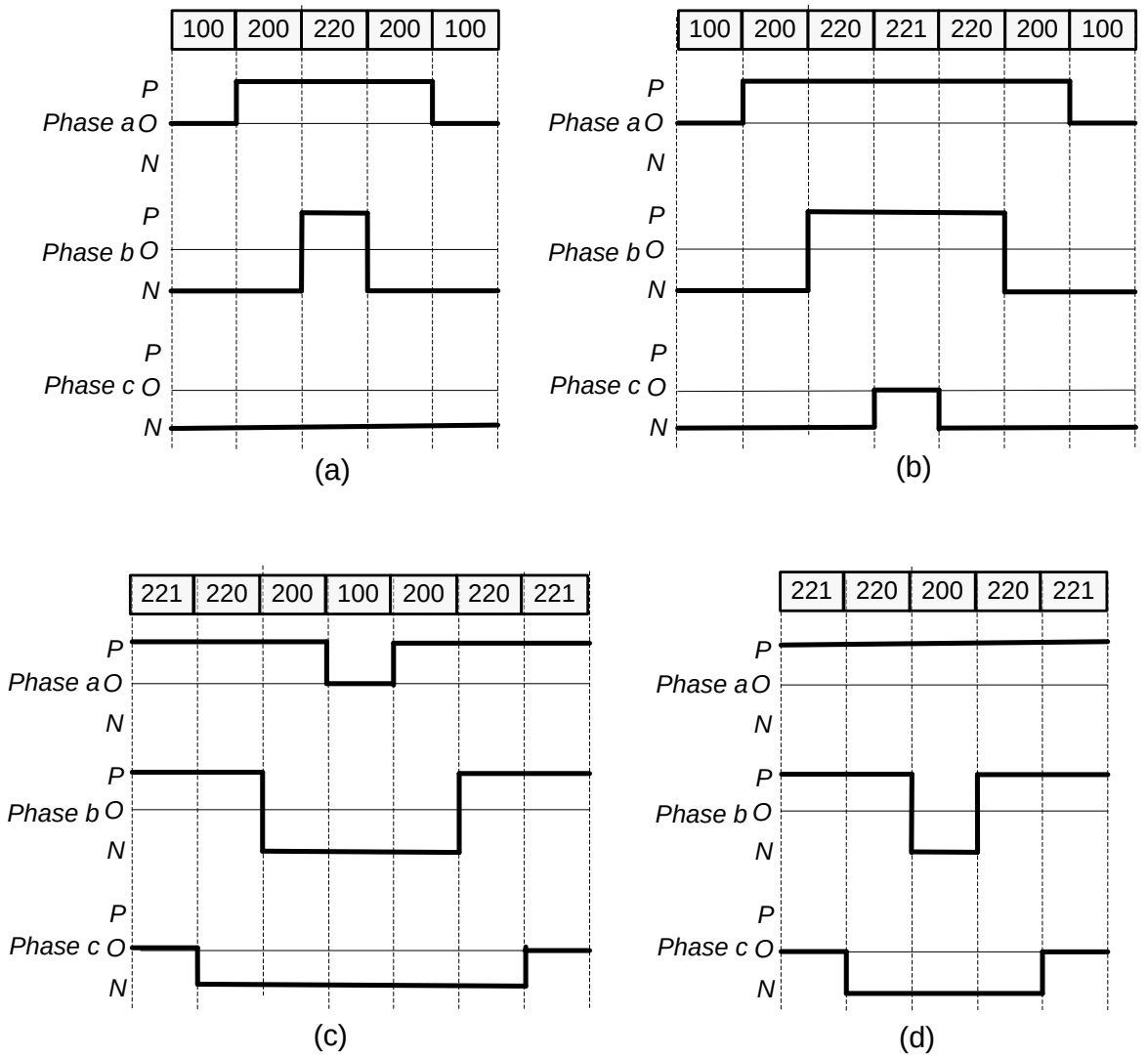


Figure 5-4 Switching sequence for the VV-based modulation of hybrid 2/3L NPCI in sector-1 when V_{ref} is located in sub-triangles (a) T_1 , (b) T_{2a} , (c) T_{2b} and (d) T_3 incorporating quarter wave symmetry.

5.2.2 Selected Three-Vector (STV)-Based Modulation:

The virtual vector based modulation discussed above uses a virtual medium vector V'_{Mi} (5.1), which is a combination of two vectors. As a result, modulation increases the number of commutations when V_{ref} is located in T_2 as shown in Figure 5-4 (b) and (c). Therefore, in order to address this issue, a new approach based on the selected three vector modulation is discussed here.

Figure 5-5 (a) and (b) shows the SVD of hybrid 2/3L NPCI divided into various sub-triangle regions for STV-based modulation. As the name indicates, the modulation uses only 3 vectors for synthesizing the reference vector in any of the sub-triangle regions. The selection of voltage vectors for various triangles regions for the reference vector located in first sector is listed in Table 5-6. For minimizing the number of transitions from one sub-triangle to other, the modulation algorithm is designed to choose either isosceles triangles $(U_1 \& U_4)$ or right-angle triangles $(U_2 \& U_3)$ depending on the modulation index $(0 < m \leq 1)$. This method is analogous to the selected three vector modulation method (STV) discussed in chapter 3 since the sub-triangle division is same, however, the selection of sub triangle region for given position of V_{ref} is different. Figure 5-5 shows flowchart for selecting the sub-triangle using 2L SVD. Each sector is divided into 5 triangles $U_0 - U_4$ as shown in Figure 5-5.

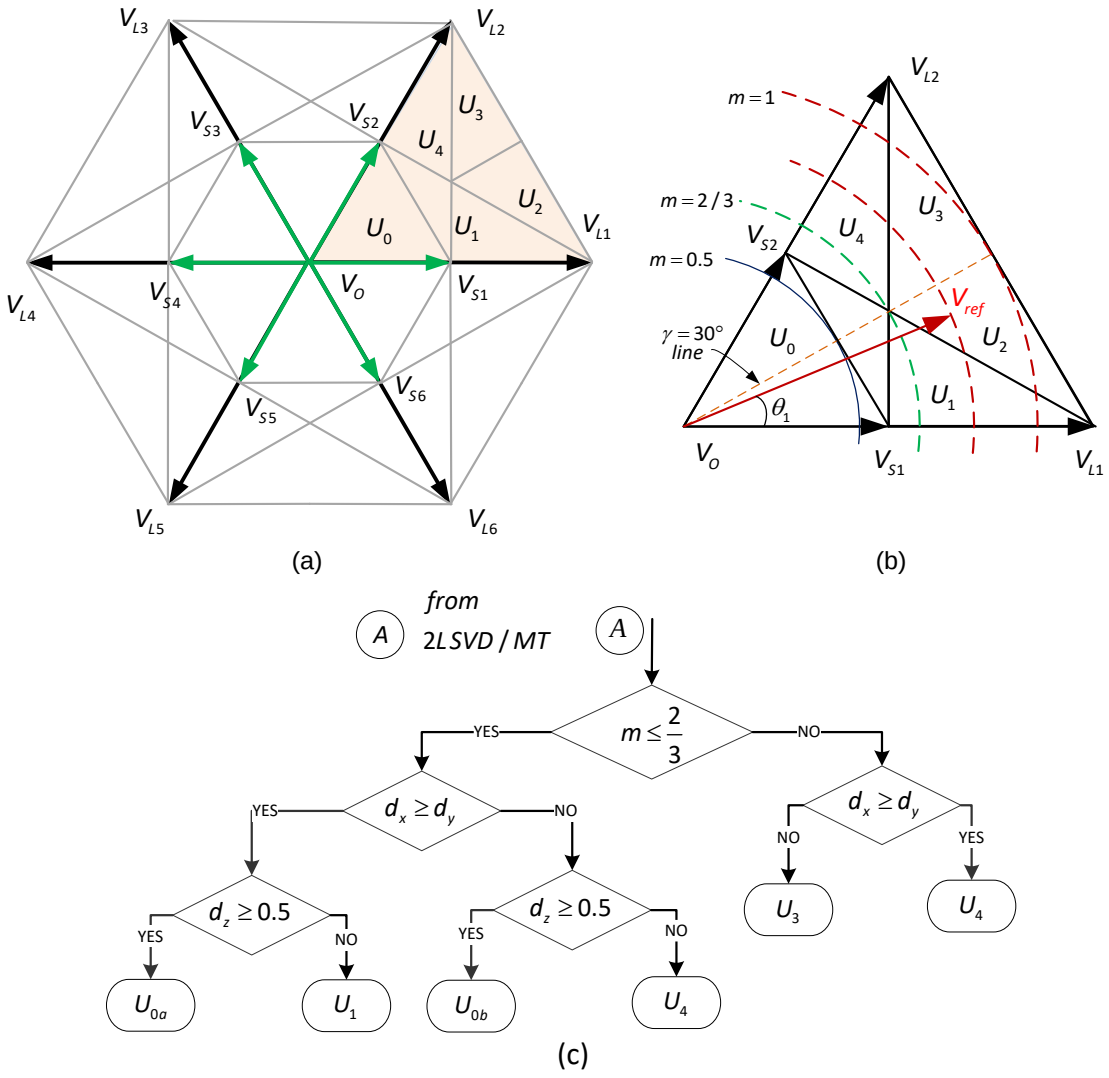


Figure 5-5 SVD of hybrid 2/3L NPCI divided into various sub-triangle regions.

Table 5-6 Voltage vector selection for STV-based method

Sub-triangle	Voltage vectors
U_o	V_0, V_{S1}, V_{S2}
U_1	V_{S1}, V_{L1}, V_{S2}
U_2	V_{S1}, V_{L1}, V_{L2}
U_3	V_{S2}, V_{L2}, V_{L1}
U_4	V_{S2}, V_{L2}, V_{S1}

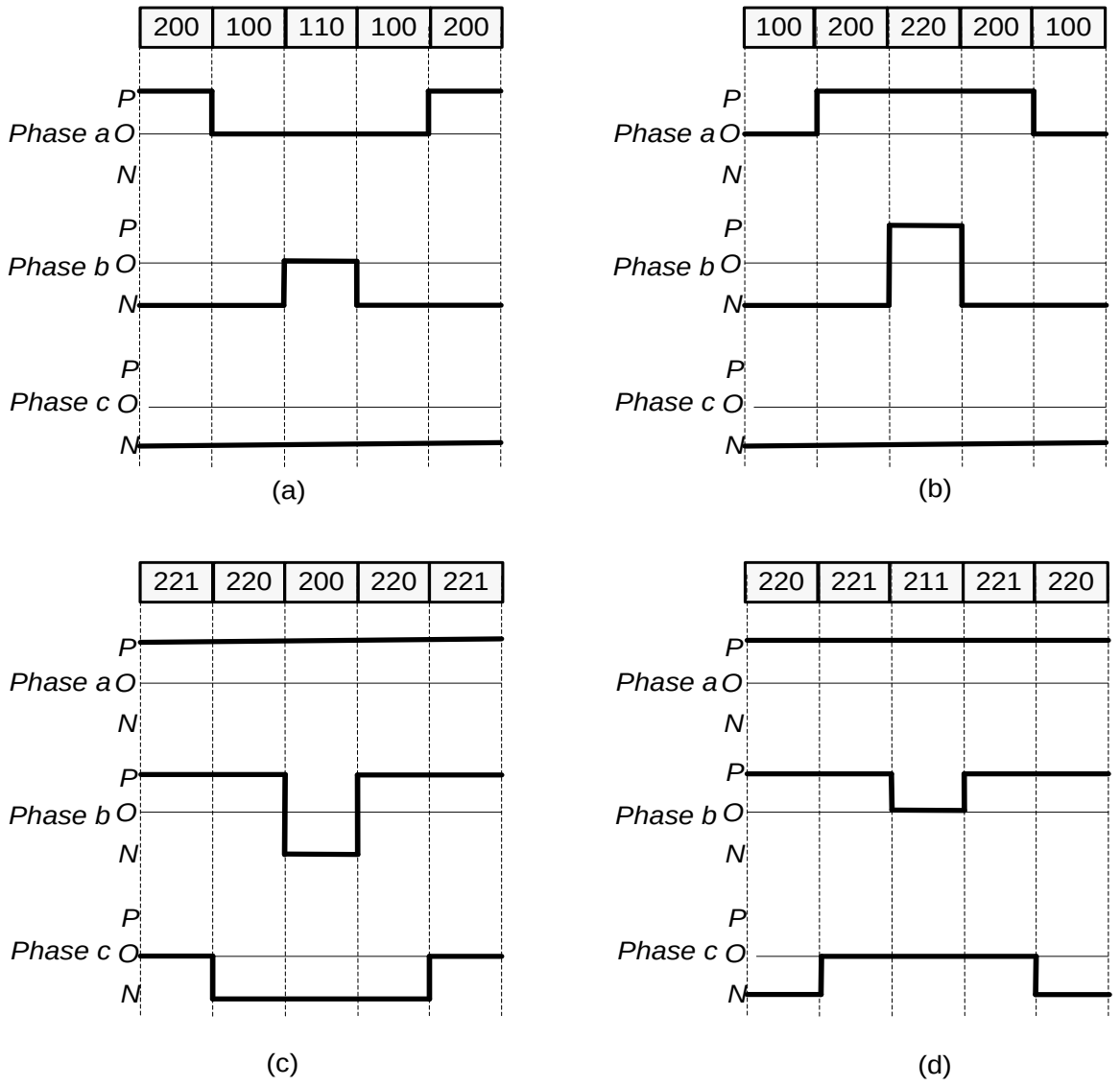


Figure 5-6 Switching sequence for the STV-based modulation of hybrid 2/3L NPCI in sector-1 when V_{ref} is located in sub-triangles (a) U_1 , (b) U_2, (c) U_3 and (d) U_4.

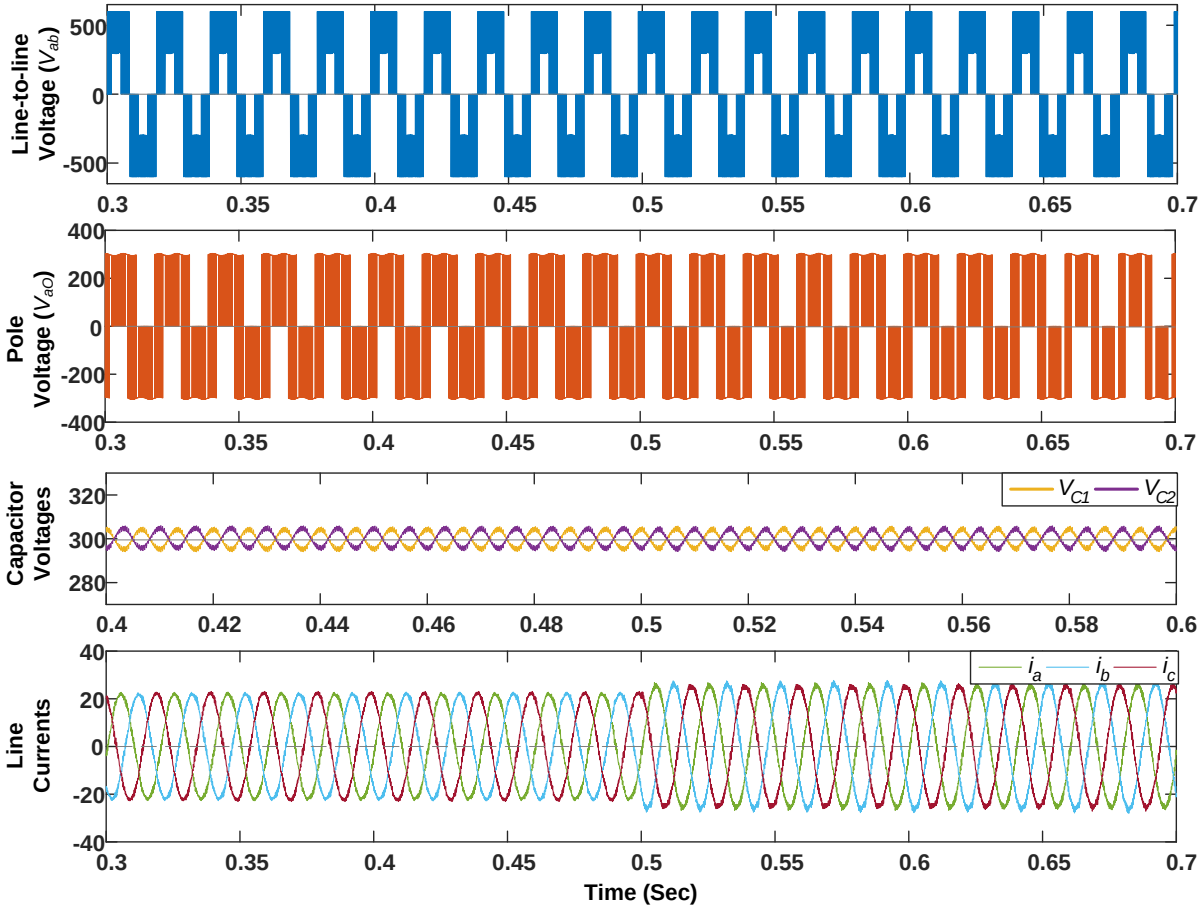
Table 5-7 Duty ratios of voltage vectors of sector-1 for selected three vector-based modulation of hybrid 2/3L NPCI

Vectors	Triangles duty ratios				
	U_o	U_1	U_2	U_3	U_4
V_O	$d_z - d_x - d_y$ *or* $(2d_z - 1)$	-	-	-	-
$V_{S1(100)}$	$2d_x$	$2(d_z - d_y)$	$2d_z$	-	$2d_x$
$V_{S2(221)}$	$2d_y$	$2d_y$	-	$2d_z$	$2(d_z - d_x)$
$V_{L1(200)}$	-	$d_x + d_y - d_z$ *or* $(1 - 2d_z)$	$d_x - d_y$	d_x	-
$V_{L2(220)}$	-	-	d_y	$d_y - d_z$	$d_x + d_y - d_z$ *or* $(1 - 2d_z)$

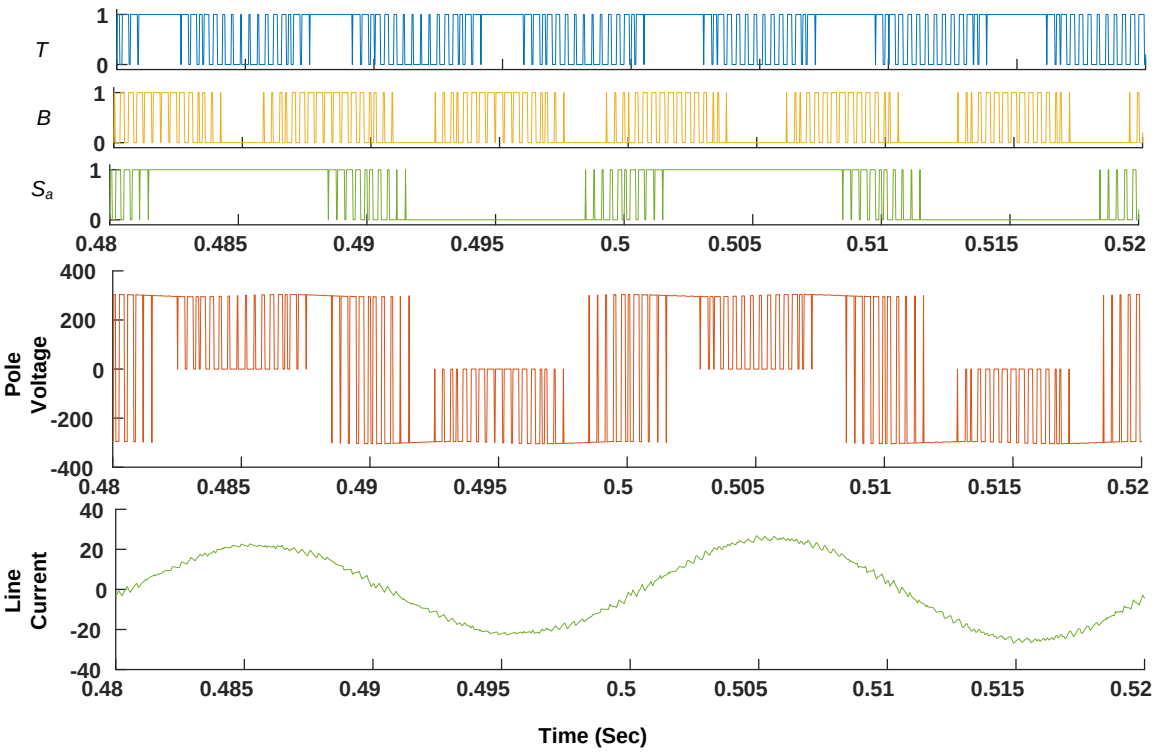
5.3 Comparative Evaluation of Modulation methods for Hybrid 2/3L NPCI

Simulations have been conducted on hybrid 2/3L NPCI to validate and compare the above discussed modulations. The performance is investigated in MATLAB-Simulink using following parameters: DC link voltage=600 V, switching frequency=3 kHz, DC link capacitors =2200µF and RL load: R=10Ω/phase; L=5mH/phase. Here, the main idea is to compare the different voltage vector selection criteria. Voltage vectors are not chosen to eliminate the low frequency (3rd harmonic ripple) in the capacitor voltages. However, two modes 1&2 are utilized equally so that the upper and lower capacitors remain balanced.

Figure 5-7 and Figure 5-8 show the simulation results of VV-based modulation for different modulation indices. Since the sub-triangles used to synthesize the reference vector V_{ref} are T_1, T_2, T_3 for any modulation index considered Here $(0.65 \le m \le 1)$, the shape of the voltage waveforms do not change. The medium magnitude voltage phase will switch as the two level VSI. i.e. 300V to -300V as it can be seen from Figure 5-7 (b) and Figure 5-8 (b). The phases with maximum and minimum amplitude will switch as 3L NPCI.

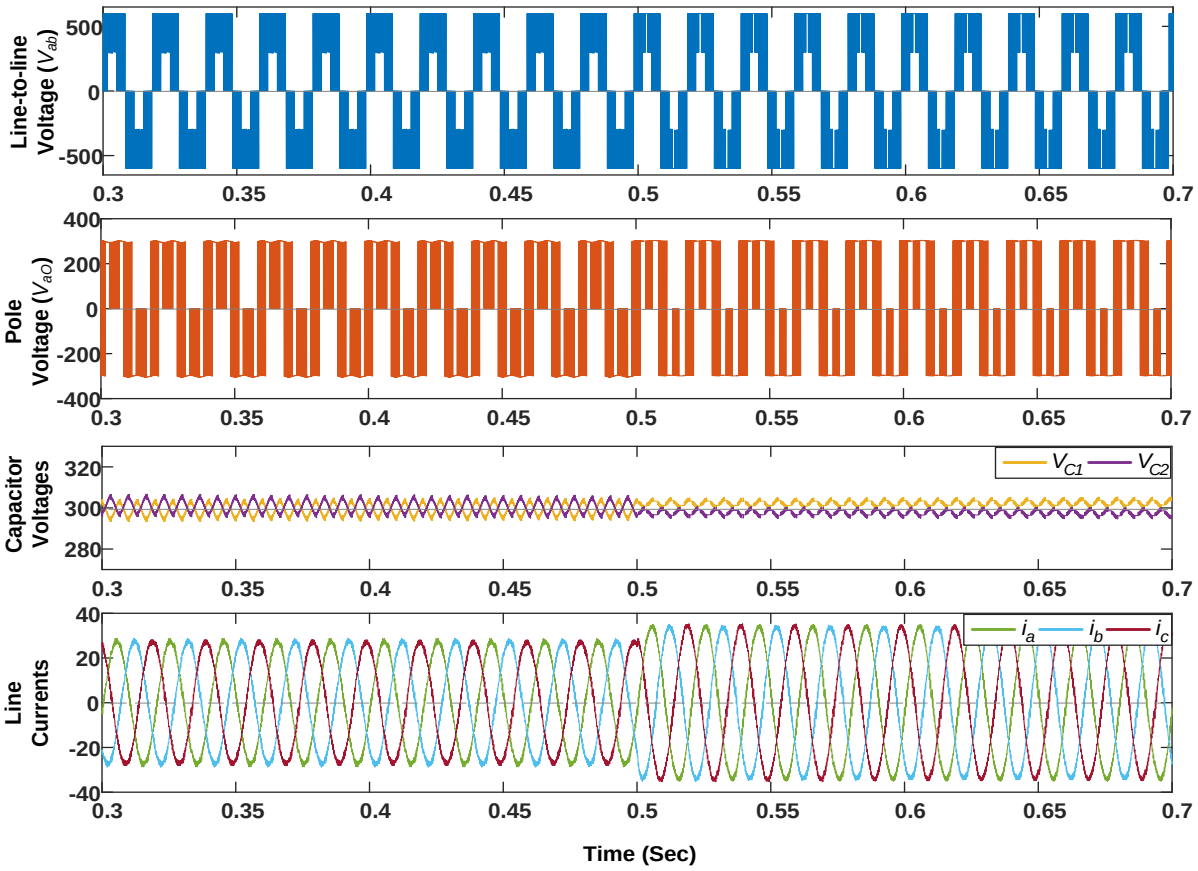


(a)

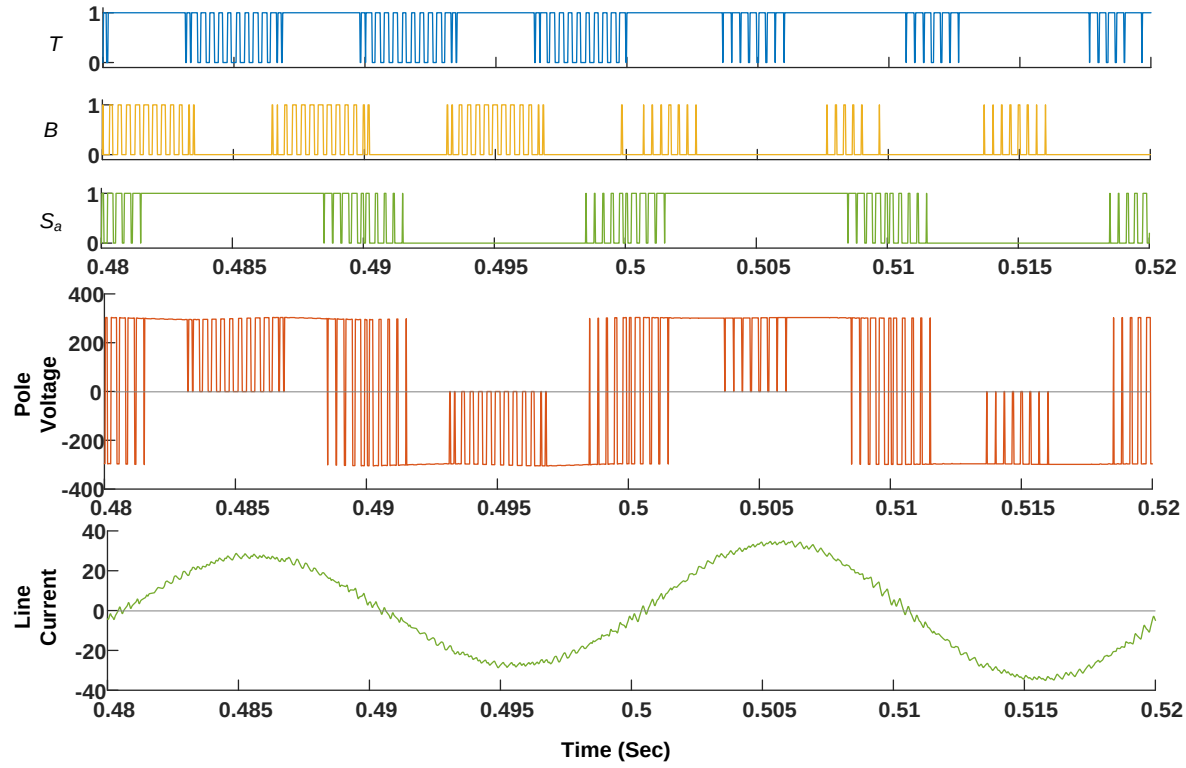


(b)

Figure 5-7 (a) Simulation results of hybrid 2/3L NPCI with VV-based modulation; (b) Zoomed view and switching signals ($m = 0.65$ for time ≤ 0.5 and $m = 0.75$ for time > 0.5).

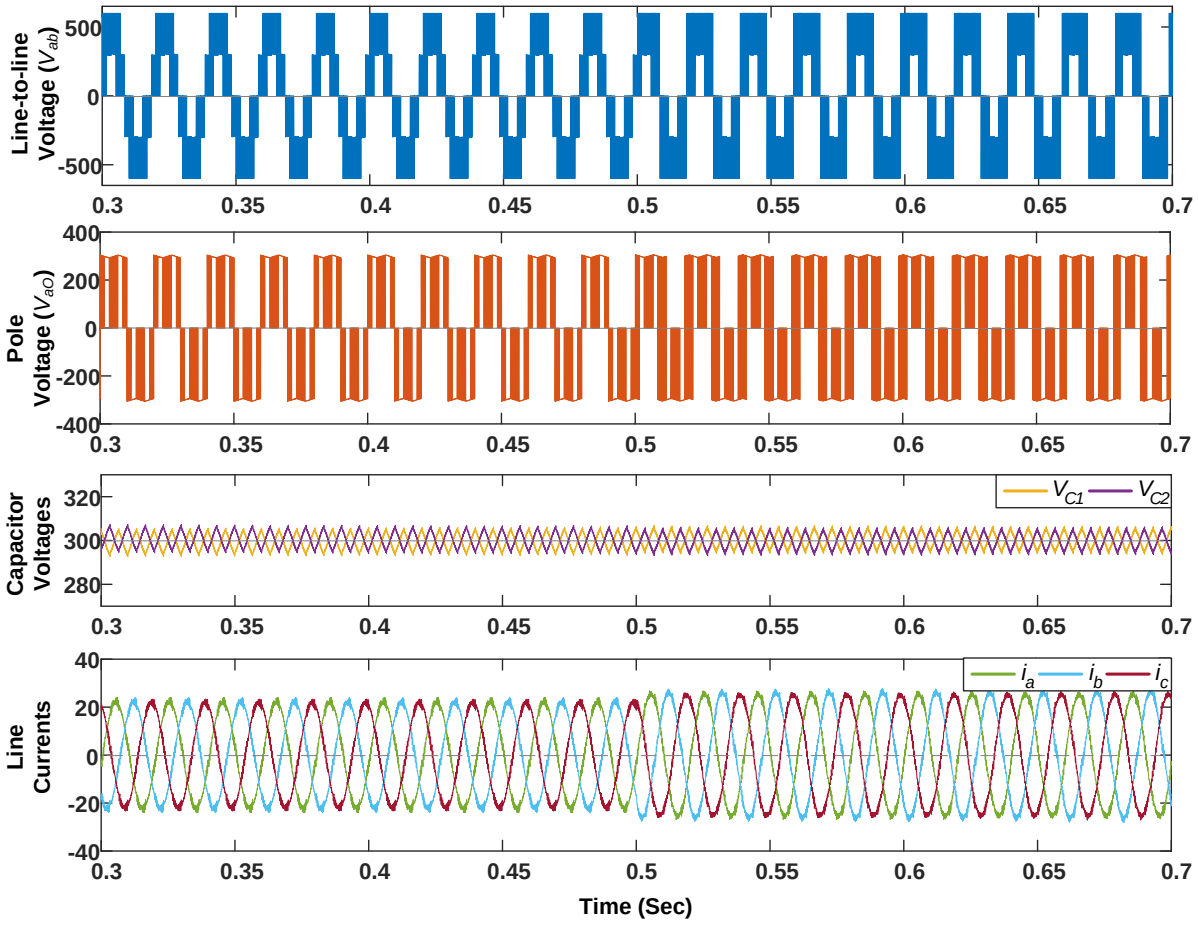


(a)

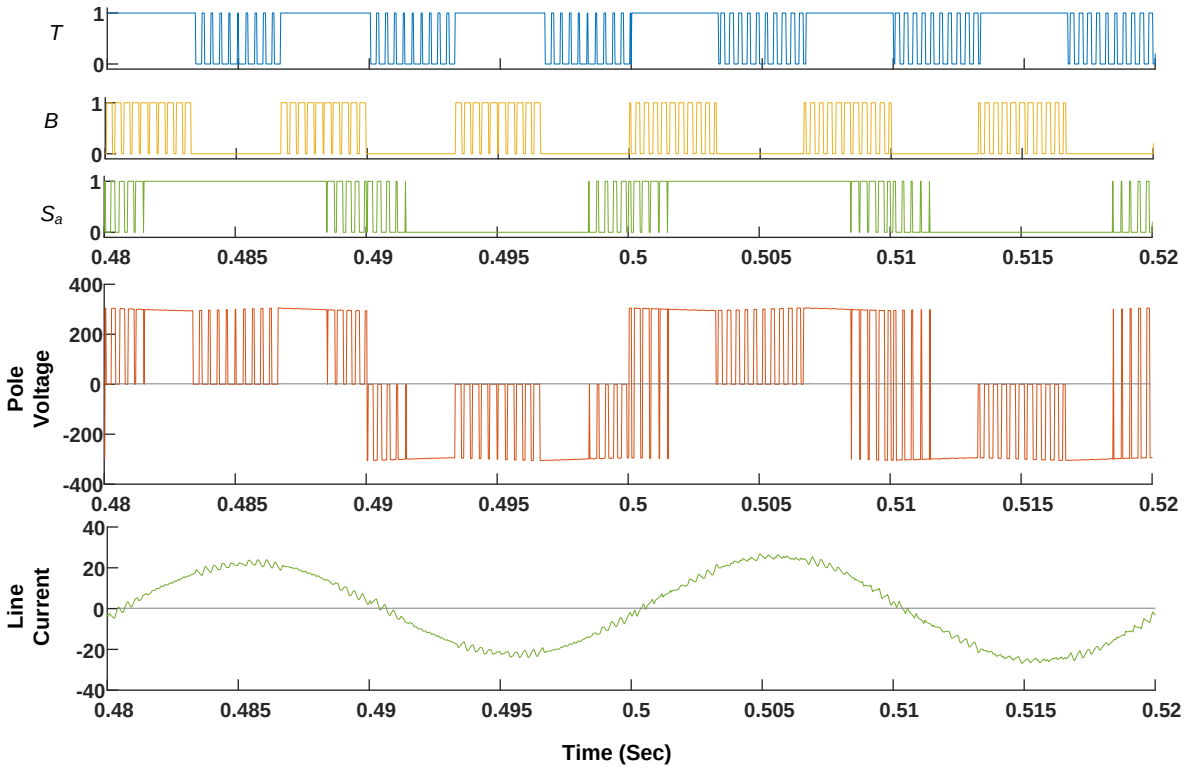


(b)

Figure 5-8 (a) Simulation results of hybrid 2/3L NPCI VV-based modulation; (b) Zoomed view and switching signals ($m = 0.8$ for time ≤ 0.5 and $m = 1$ for time > 0.5).

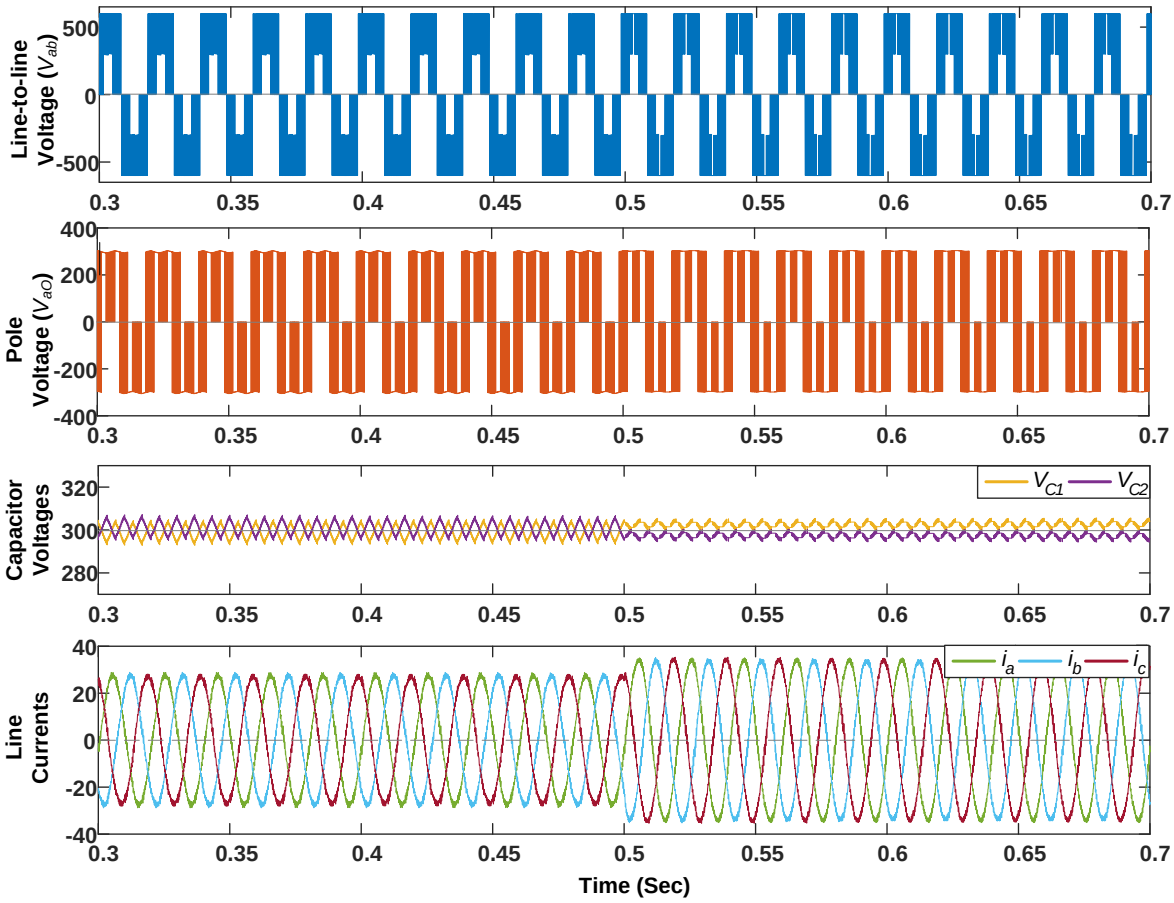


(a)

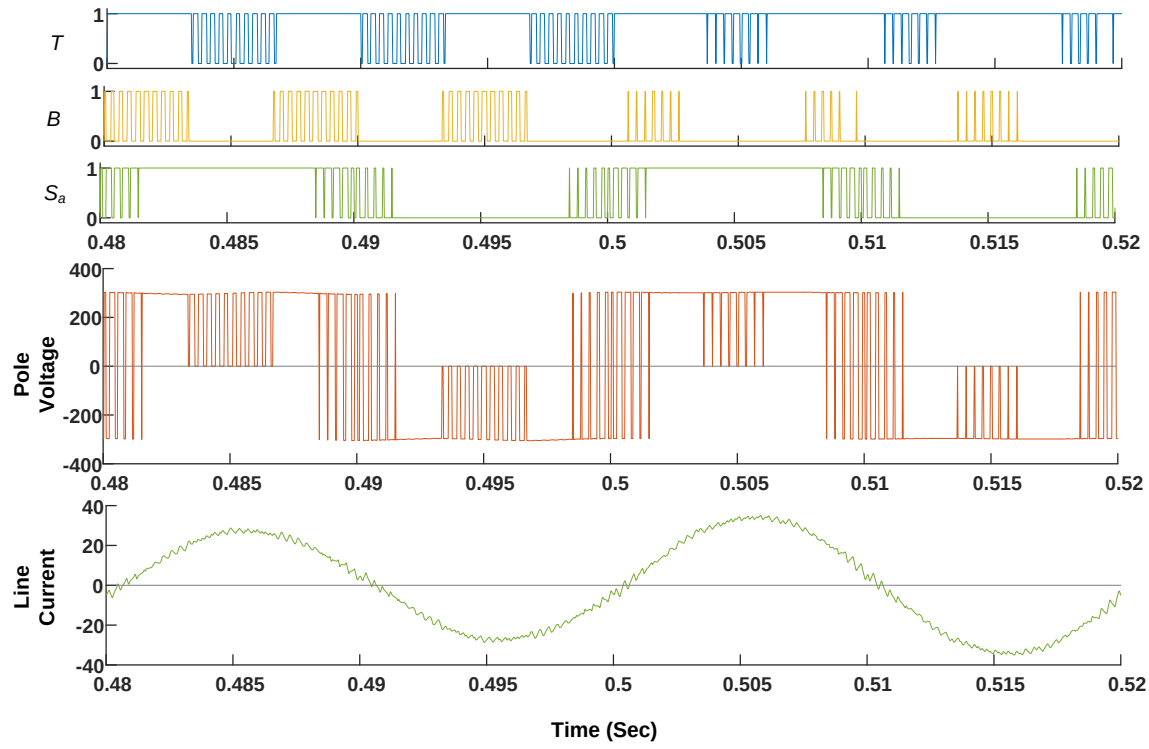


(b)

Figure 5-9 (a) Simulation results of hybrid 2/3L NPCI with STV based modulation; (b) Zoomed view and switching signals ($m = 0.65$ for time ≤ 0.5 and $m = 0.75$ for time > 0.5).



(a)



(b)

Figure 5-10 (a) Simulation results of hybrid 2/3L NPCI with STV-based modulation; (b) Zoomed view and switching signals ($m = 0.8$ for time ≤ 0.5 and $m = 1$ for time > 0.5).

Figure 5-9 and Figure 5-10 show simulation results of STV-based modulation. Unlike the VV-based modulation, the sub-triangle regions for $0.5 \le m \le 2/3$ and $2/3 < m \le 1$ are different in the case of STV-based modulation. When $0.5 \le m \le 2/3$, the modulation uses sub-triangles U_1 / U_4 therefore, the phase voltages will switch similar to 3L NPCI irrespective of their magnitude. As the modulation index increases, the difference between the two modulation methods will reduce. This is because, the duration of the reference vector in the triangle T_2 will reduce with increase in the modulation index. For $m = 1$ both the modulation indices will concide with one other as show in Figure 5-8 and Figure 5-10. For $0 < m \le 0.5$, the modulation of the hybrid 2/3L NPCI can be carried out similar to the conventional 3L NPCI and therefore, it is not discussed here.

5.4 Advanced Modulation Methods for Hybrid 2/3L NPCI

The modulation methods discussed in previous section use only one of the redundant switching states of a small vector in each switching cycle. Therefore, these methods are not suitable for some of the applications like z-source interconnection, and unbalanced source voltage compensation, etc. Moreover, small vectors cause NP current as shown in Figure 5-2 (d), and leads to increased capacitor voltage oscillations at high modulation index and low power factor operations similar to 3L NPCI. Therefore, new switching sequences are investigated for higher modulation indices to address this issue.

Some of the switching transitions do not increase the switching frequency of hybrid 2/3L NPCI. For example, if V_{ref} is located in sub-triangle U_2, the two possible switching sequences are depicted in Figure 5-11. From the switching signals of the hybrid 2/3L NPCI, it can be observed that number of commutations for the semiconductor switches are same for both the sequences. This is because, the switching transition $211 \leftrightarrow 200$ is obtained by $(B, \bar{B}) : (1,0) \leftrightarrow (0,1)$ and hence requires only one commutation. Similarly, the transition $0 \leftrightarrow 2$ observed in *Phase b* also requires on commutation in the phase leg switching pair $\left(S_b, \bar{S}_b\right)$. In the same manner, in case of VV-based modulation, the possible switching sequences when V_{ref} is located in sub-triangle T_2 are depicted in Figure 5-12. The switching transition $110 \leftrightarrow 220$ is obtained by $(T, \bar{T}) : (0,1) \leftrightarrow (1,0)$ and requires one commutation.

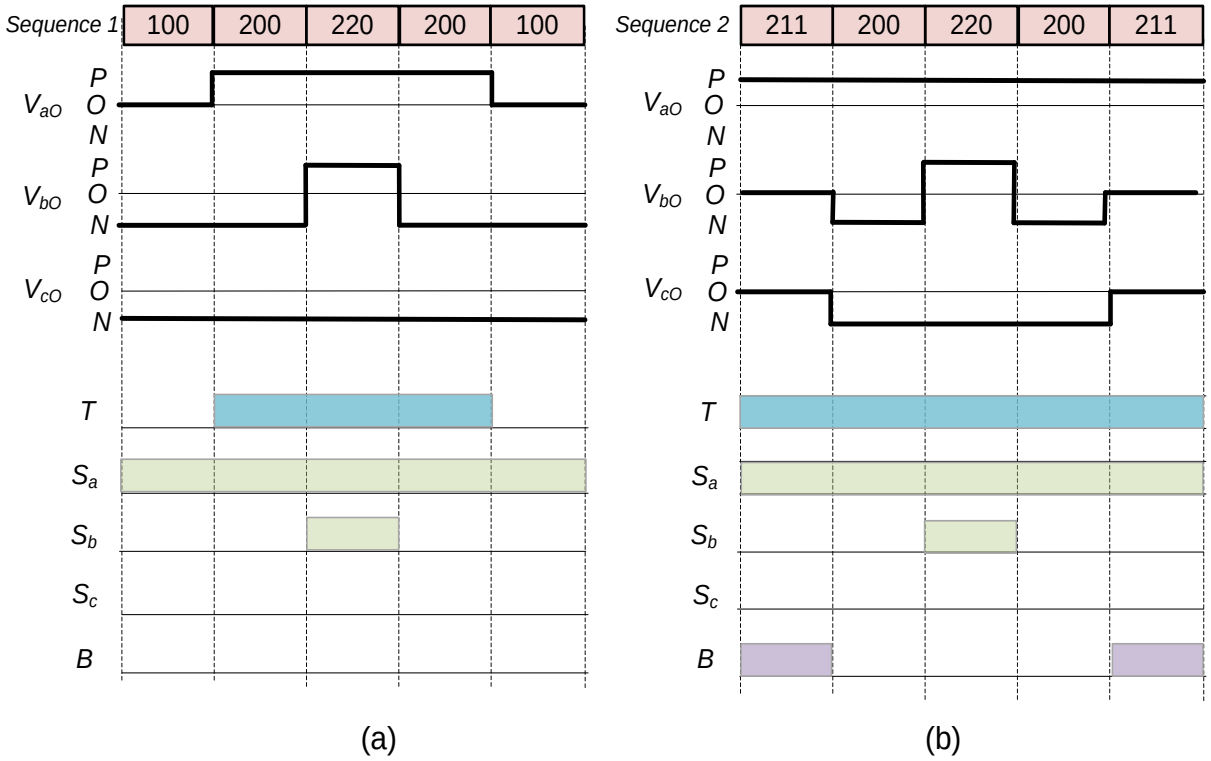


Figure 5-11 Possible switching sequences for the STV modulation when V_{ref} is located in U_2 and switching signals of the hybrid 2/3L NPCI; (a) Sequence-1 and (b) sequence-2.

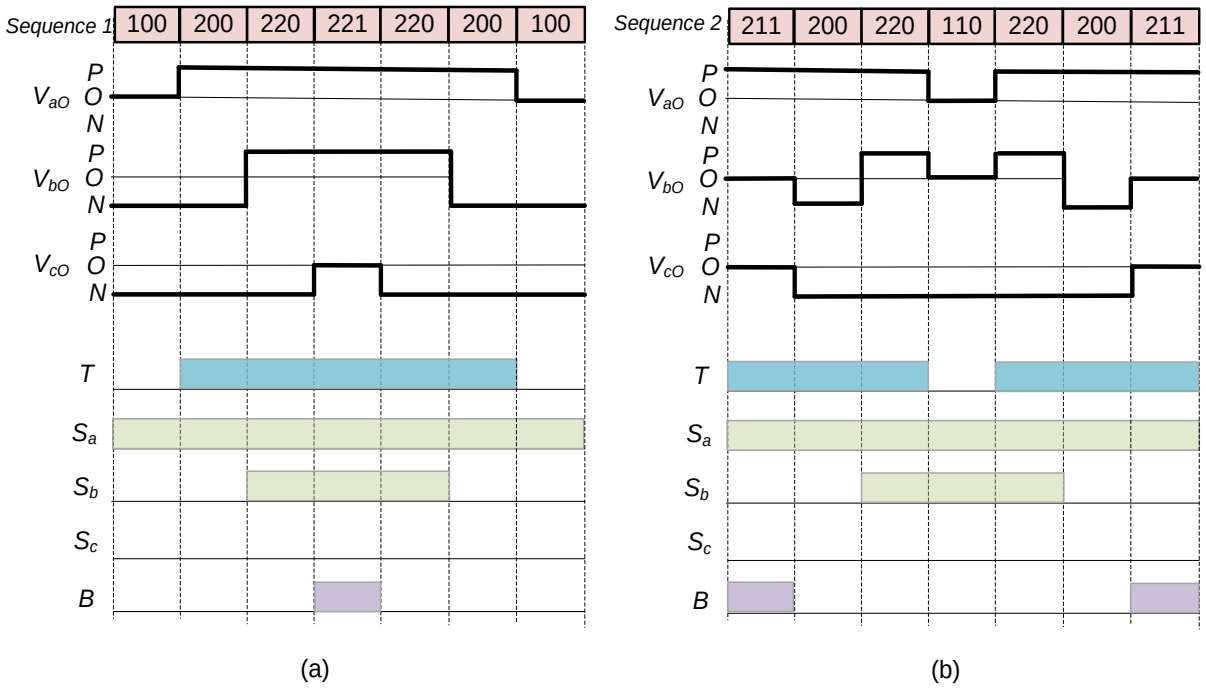


Figure 5-12 Possible switching sequences for the VV modulation when V_{ref} is located in and switching signals of the hybrid 2/3L NPCI; (a) Sequence-1 and (b) sequence-2.

5.5 Hybrid 2/3L Z-Source NPCI (Z-NPCI)

5.5.1 Circuit Description

Figure 5-13 shows the hybrid 2/3L NPCI with a Z-source impedance network connected to a PV panel. Detailed operation of Z-source impedance network is given in [139][140] and therefore, not discussed here. From Figure 5-13, it can be easily observed that the upper leg ST (UST) can be obtained by gating *{T_1, T_2} = {1,1}*, while the lower leg ST (LST) can be obtained using *{B_1, B_2} = {1,1}*. The operation of each inverter phase leg is represented as three switching states “2”,”1” and “0”. Taking “0”as reference, the switching table and corresponding output voltages are given in the Table I. The aim of the VSI is to synthesize the three phase reference voltages at the ac side collectively represented as a space vector given by

$$\left.\begin{aligned} V &= \frac{2}{3}.(v_a + v_b.e^{j2\pi/3} + v_c.e^{j4\pi/3}) \\ &= V_m e^{i\omega t} \\ &= \frac{m}{\sqrt{3}} V_i e^{i\omega t} \end{aligned}\right\} \quad (5.2)$$

Where, ‘V’ is voltage vector, ‘’is peak value of the reference voltage and ‘m’ is the modulation index given by $m = \sqrt{3}V_m / V_{DC}$.

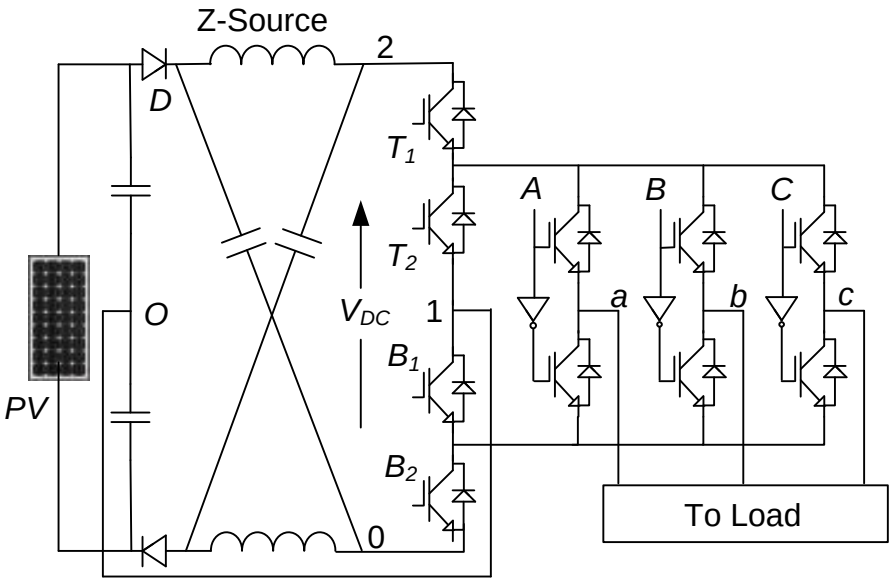


Figure 5-13 Circuit of hybrid 2/3L ZNPCI.

The space vector diagram (SVD) of hybrid 2/3L NPCI is shown in Figure 5-14. Compared to conventional 3L SVD, the medium vectors: “210”, ”120”, “021”, “012”, “102” and “201” are absent in the new 2/3L SVD. While, all the long vectors $V_{L1} - V_{L6}$, small vectors $V_{S1} - V_{S6}$ and zero vector V_z remain unchanged. In other words, due to the switching constraints of hybrid 2/3L

NPCI, at least two of the three phase legs output must be same and independent operation of the phase legs is not possible. Therefore, all the medium vectors are not switchable due to the structure of the hybrid 2/3L NPCI. the SVD is however symmetric and hence, further analysis is only presented with respect to the sector-1 for simplicity.

Table 5-8 Switching table of hybrid 2/3L NPCI

Voltage level	Notation	T_1	B_1	P
V_{DC}	2	1	X	1
$V_{DC}/2$	1	0	X	1
		X	1	0
0	0	X	0	0

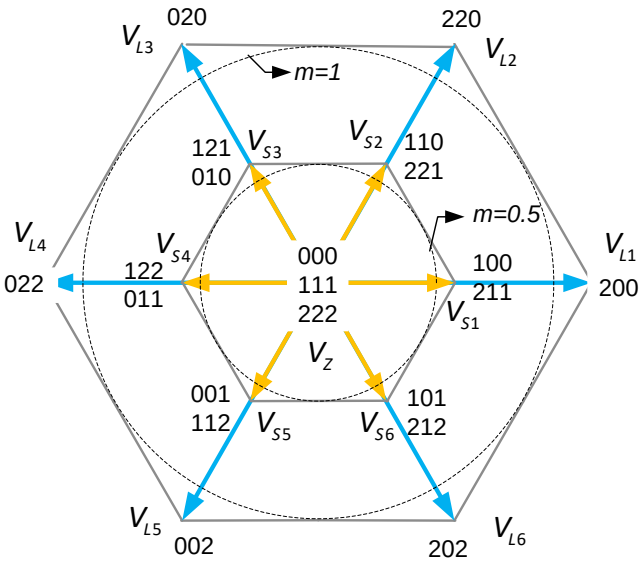
(P =A, B, C); T_2=complement of $T1$; B_2=complement of B_1; X=don't care condition, however it will depend on the voltage level of the remaining phases.

5.5.2 Virtual Vector Modulation for Hybrid 2/3L ZVSI

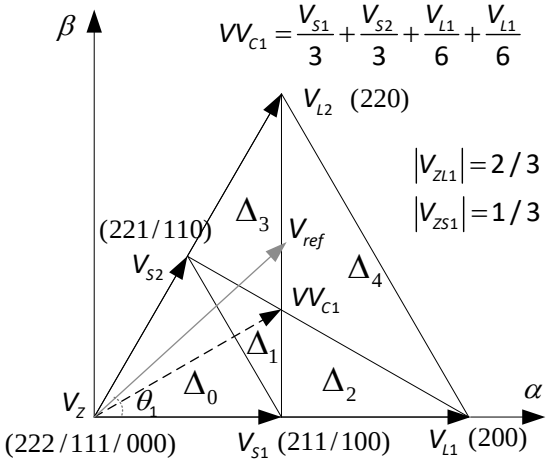
Carrier modulation methods for modulating the 2/3L NPCI are proposed in [141][142]. These methods are similar and divides the switching cycle into three intervals depending on magnitude of reference voltages. The medium magnitude phase is always switch as 2L VSI and either least magnitude or highest magnitude phase is only switched as 3L NPCI. The selection of these intervals is also complex and uses dedicated algorithm. Moreover, the modulation does not use the nearest thee available voltage vectors for $0<m\leq 0.5$, results in degraded performance compared to 3L VSI. the modulations result in unequal utilization of small vectors and consequently cannot be used with Z-source impedance network. This is because, shoot through states cannot be inserted in two of the three intervals as they only used one small vector in each switching cycle.

In this section, a new virtual vector modulation for hybrid 2/3L Z-source NPCI (ZNPCI) is presented. Two switching sequences derived and analyzed in detail for higher modulation range. Unlike the aforementioned modulations developed for hybrid 2/3L NPCI, this new-VV modulation can be directly applied to operate the hybrid 2/3L ZNPCI. The modulation has the following features:

a) Both the small vectors are used for entire modulation index (m) range so that it can incorporate the shoot through (ST) states.
b) The insertion of ST states will not increase the number of device commutations.
c) Improved performance compared to 2L Z-source VSI.
d) For $0<m\leq 0.5$ the modulation is exactly similar to conventional 3L ZNPCI.
e) The modulation is simple to implement.



(a)



(b)

Figure 5-14 (a) SVD of hybrid 2/3L ZNPCI and (b) division of sector-1 in various sub-triangle regions. ($\Delta_0=V_ZV_{S1}V_{S2};\Delta_1=VV_{C1}V_{S1}V_{S2};\Delta_2=VV_{C1}V_{S1}V_{L1};\Delta_3=VV_{C1}V_{L2}V_{S2};\Delta_4=VV_{C1}V_{L1}V_{L2}$).

The modulation needs to synthesize the reference vector (5.2) with the help of available vectors. Meanwhile care should be taken to allocate the durations of small vectors in order to incorporate the shoot through states: LST and UST for equal duration. Therefore, in order to overcome the above-mentioned issues, a new virtual vector modulation is introduced.

A virtual vector located at centroid of the sector-1 (triangle region formed by $V_ZV_{L1}V_{L2}$) is shown in Figure 5-14 (a) which is mathematically expressed as:

$$VV_{C1}=\frac{V_{S1}}{3}+\frac{V_{S2}}{3}+\frac{V_{L1}}{6}+\frac{V_{L2}}{6} \tag{5.3}$$

Similarly, virtual vectors $VV_{C2}-VV_{C6}$ will be present in the remaining sectors 2-6 using the corresponding small and large vectors. Now, with the help of the virtual vector VV_{C1}, the Sector-

1 is divided in to various sub-triangle regions $\Delta_0 - \Delta_4$ as shown in Figure 5-14 (b). The virtual vector VV_{C1} (2) will helps to synthesize the reference vector V_{ref} for $0.5 < m \leq 1$, while the two small vectors and zero vector will be used for $m \leq 0.5$. Therefore, for entire range of modulation index ($0 \leq m \leq 1$), the two small vectors are always used in each switching cycle.

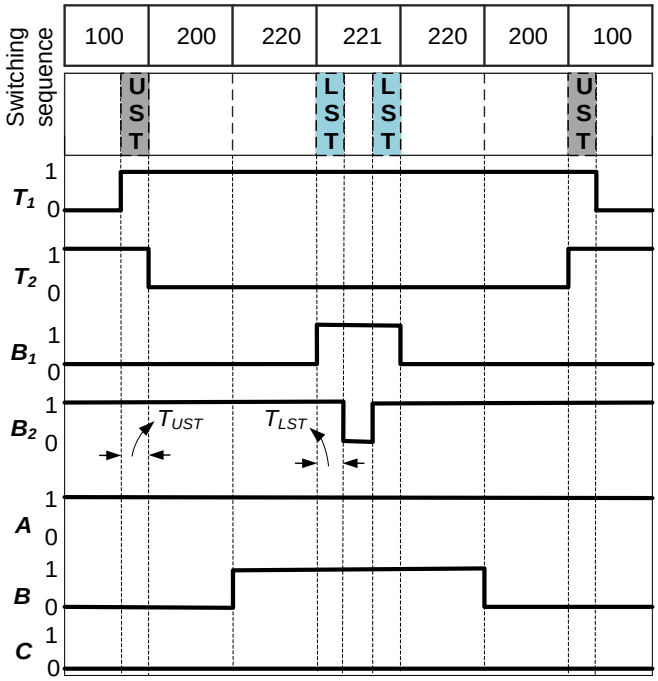
For $0.5 < m \leq 1$: Depending on the instant of sampling and magnitude, V_{ref} can be located in any of the sub-triangles $\Delta_1 - \Delta_4$. VV_{C1} is a common vertex in all these sub-triangle regions and therefore two small and two long vectors are inherently used by the modulation for synthesis (refer equation (2)) in the range $0.5 < m \leq 1$. This also helps in insertion of shoot-through states without increasing the device commutations as discussed in the next sub-section.

For $0 < m \leq 0.5$: V_{ref} will be located in sub-triangle Δ_0 and synthesized using two small vectors and the null vector V_z. In this modulation index range, the modulation will be same as the conventional 3L VSI.

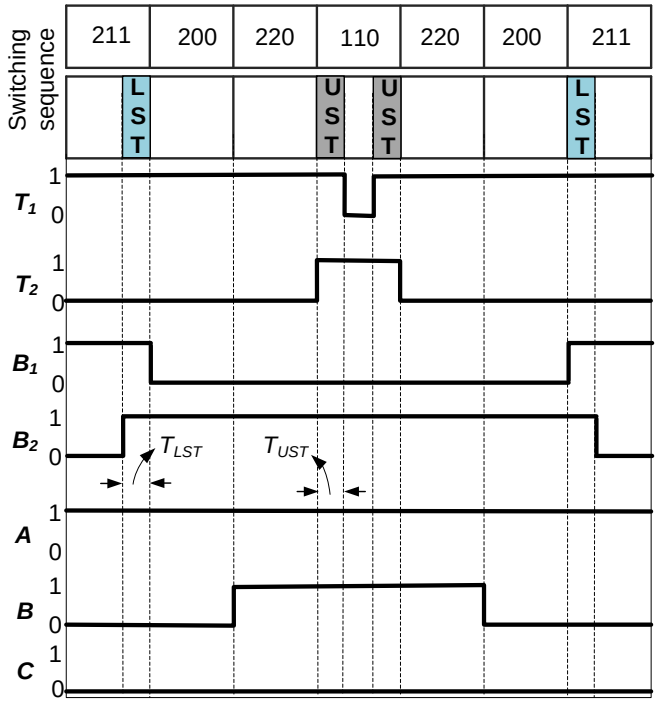
5.5.3 Switching Sequence and Insertion of Shoot-Through States

For higher modulation index $m > 0.5$, the proposed virtual vector modulation uses two small vectors and two large vectors. For example: If V_{ref} is located in Δ_2 the vectors V_{S1}, V_{L1} and VV_{C1} are used to solve the volt-sec balance equation to find the duty ratios. After that, the duty ratio of vector VV_{C1} is distributed to the associated vectors $V_{S1}, V_{L1}, V_{L2}, V_{S2}$ based on equation (2). Two switching sequences (SS): SS1: "100-200-220-221" and SS2: "211-200-220-110" can be used to synthesize V_{ref} in sector-1. This is true for V_{ref} located in sub-triangles Δ_1, Δ_3 and Δ_4 as well. Note that, unlike the conventional NPCI, the two-switching state will not cause extra device commutations in hybrid 2/3L NPCI as shown in Figure 5-15 (a) and (b) respectively.

For a fixed switching cycle, insertion of shoot through states within the small vector intervals with the other intervals maintained constant will not alter the normalized volt–second average per switching cycle seen by the ac load. UST or LST can be added at V_{S1} and V_{S2} ("100" and "110" for UST and "211" and "221" for LST). Insertion of shoot-through states in SS1 and SS2 and corresponding switching signals are depicted in Figure 5-15. No additional device commutations can be observed with the insertion of ST states. Due to the selection of close by voltage vectors, the performance is expected to be improved incomparison to 2L Z-source VSI. Note that the switching sequences "100-200-220-222" or "000-200-220-221" used in [141][142] are not suitable for addition of ST states (UST and LST) within a switching cycle as only one small vector is utilized. Even though sequences like "100-200-220-211" [143] can insert both the ST states, they result in additional device commutations and therefore not suitable.



(a)



(b)

Figure 5-15 Switching sequences for $0.5 < m \leq 1$: (a) SS1 and (b) SS2 (UST: Upper shoot through; LST: Lower shoot through).

From the SVD of hybrid 2/3L NPCI shown in Figure 5-14 (b), it is clear that for $m \leq 0.5$, the reference vector V_{ref} will present in triangle Δ_0. Since all the switching states are present, the operation in this lower modulation index range ($m \leq 0.5$) of the hybrid 2/3 VSI is exactly similar

to that of 3L NPCI. Therefore, the discussion in this paper is limited for $0.5 \le m < 1$. Usually, shoot through states are not used in this interval since boosting operation is not required as the load voltage reference is already less. On the other hand, the shoot through states will increase the losses and degrade the overall performance of VSI.

5.5.4 Modulation Algorithm for Hybrid 2/3L ZVSI

In this section, the duty ratios for the switching states of hybrid 2/3L NPCI are derived. All the duty ratios are expressed with respect to an equivalent 2L SVD formed by outermost voltage vectors V_Z, V_{L1} and V_{L2}. Figure 5-16 (a) shows the equivalent 2L SVD. The volt-sec balance equation for equivalent 2L SVD is given by

$$\begin{aligned} d_z V_Z + d_{L1} V_{L1} + d_{L2} V_{L2} &= V_{ref} \\ d_z + d_{L1} + d_{L2} &= 1 \end{aligned} \tag{5.4}$$

Where, d_x, d_y and d_z are the duty ratios of V_{L1}, V_{L2} and V_Z respectively. Assuming duty ratios d_x, d_y and d_z known, the duty ratios of switching states of hybrid 2/3L NPCI are derived and tabulated in Table 5-9 as explained in detail in [144]. Similarly, the sector-1 of the conventional 3L SVD is also shown in (b) for comparison. The difference between 3L SVD and 2/3L SVD is only the absence of the medium voltage vector V_{M1}. The sector-1 of the 3L NPCI is divided into four equilateral triangles as shown $T_0 - T_3$. The duty ratios of the switching states are also expressed in terms of equivalent 2L SVD and are tabulated in Table 5-10.

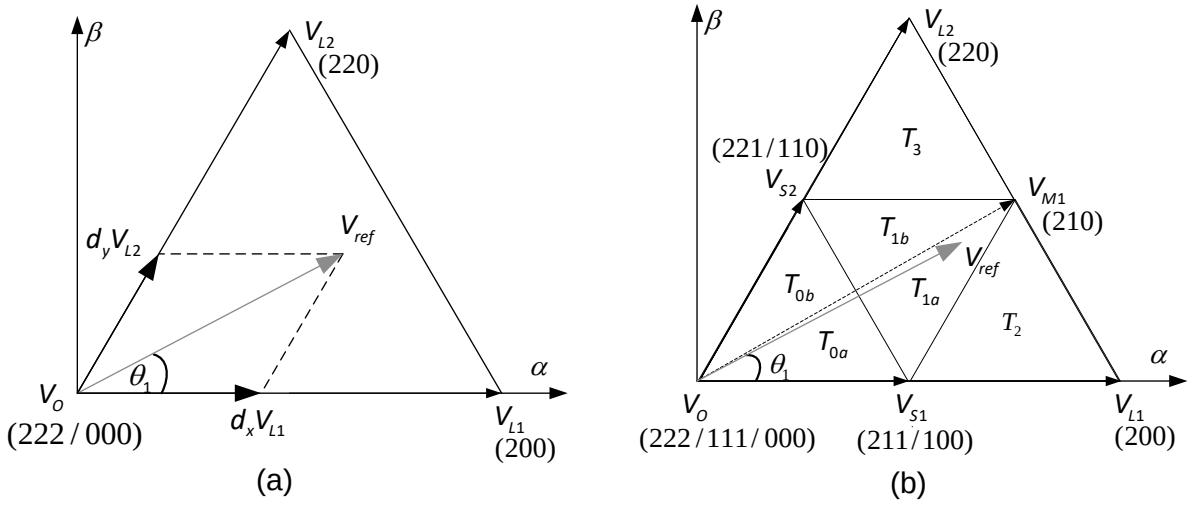


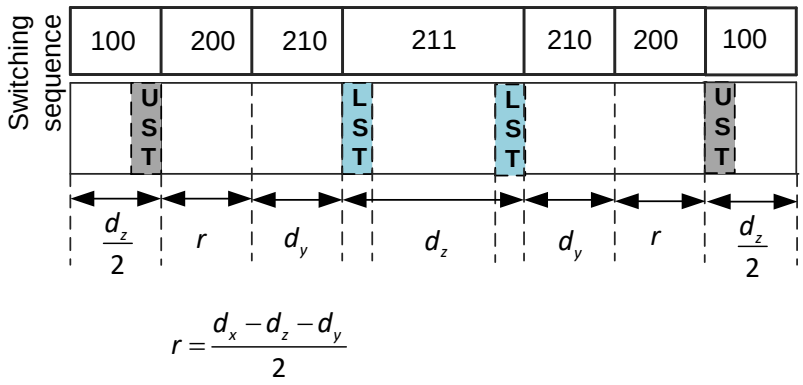
Figure 5-16 Sector-1 of space vector diagram (SVD) of (a) equivalent 2L VSI and (b) 3L VSI.

Table 5-9 Duty ratios of hybrid 2/3L NPCI with the proposed VV modulation for sector 1

Vectors (switching states)	Triangles duty ratios				
	Δ_0	Δ_1	Δ_2		Δ_4
$V_{S1}(100)/(211)$	$2d_x$	$d_x+d_z-d_y$	$2d_z-d_y$	d_x	d_z
$V_{S2}(221)/(110)$	$2d_y$	$d_y+d_z-d_x$	d_y	$2d_z-d_x$	d_z
$V_{L1}(200)$	-	$0.5\left(d_x+d_y-d_z\right)$	$d_x-d_z+0.5d_y$	$0.5d_x$	$d_x-0.5d_z$
$V_{L2}(220)$	-	$0.5\left(d_x+d_y-d_z\right)$	$0.5d_y$	$d_y-d_z+0.5d_x$	$d_y-0.5d_z$
V_O	$d_z-d_x-d_y$	-	-	-	-

Table 5-10 Duty ratios of 3L VSI with the conventional space vector modulation for sector 1

Vectors (switching states)	Triangles duty ratios			
	T_0	T_1	T_2	T_3
$V_{S1}(100)/(211)$	$2d_x$	$d_x+d_z-d_y$	$2d_z$	-
$V_{S2}(221)/(110)$	$2d_y$	$d_y+d_z-d_x$	-	$2d_z$
$V_M(210)$	-	$d_x+d_y-d_z$	$2d_y$	$2d_x$
$V_{L1}(200)$	-	-	$d_x-d_z-d_y$	-
$V_{L2}(220)$	-	-	-	$d_y-d_z-d_x$
V_O	$d_z-d_x-d_y$	-		-



$$r=\frac{d_x-d_z-d_y}{2}$$

Figure 5-17 Switching sequence for 3L NPCI VSI when V_{ref} is located in T_2 using the conventional SVM.

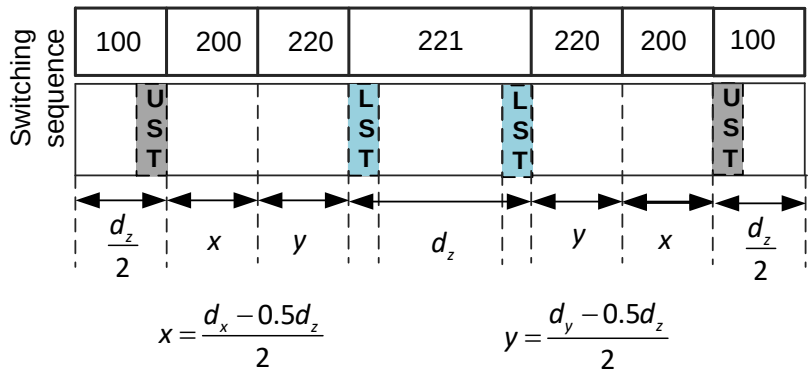


Figure 5-18 Switching sequence SS1 for hybrid 2/3L NPCI when V_{ref} is located in Δ_4 using the proposed VV modulation.

The exact duty ratios of the redundant small vectors will depend on the switching sequence used. For example, in case of hybrid 2/3L NPCI SS1 is used. Duty ratios of the various switching states are as follows: $d_{100} = d_y$; $d_{211} = 0$; $d_{200} = d_x - d_z + 0.5d_y$; $d_{220} = 0.5d_y$; and $d_{221} = d_y$ when V_{ref} is located in Δ_2 (refer Figure 5-14 (b)). Similarly, for 3L SVM [2] the duty ratios of the various switching states are as follows: $d_{100} = p(2d_y)$; $d_{211} = (1-\mathrm{p})(2d_y)$; and $d_{210} = 2d_y$ when V_{ref} is located in T_2 (refer Figure 5-16 (b)). Here, $p \in [0,1]$ is called distribution factor, which distributes the duty ratio of the small vectors to the corresponding redundant states.

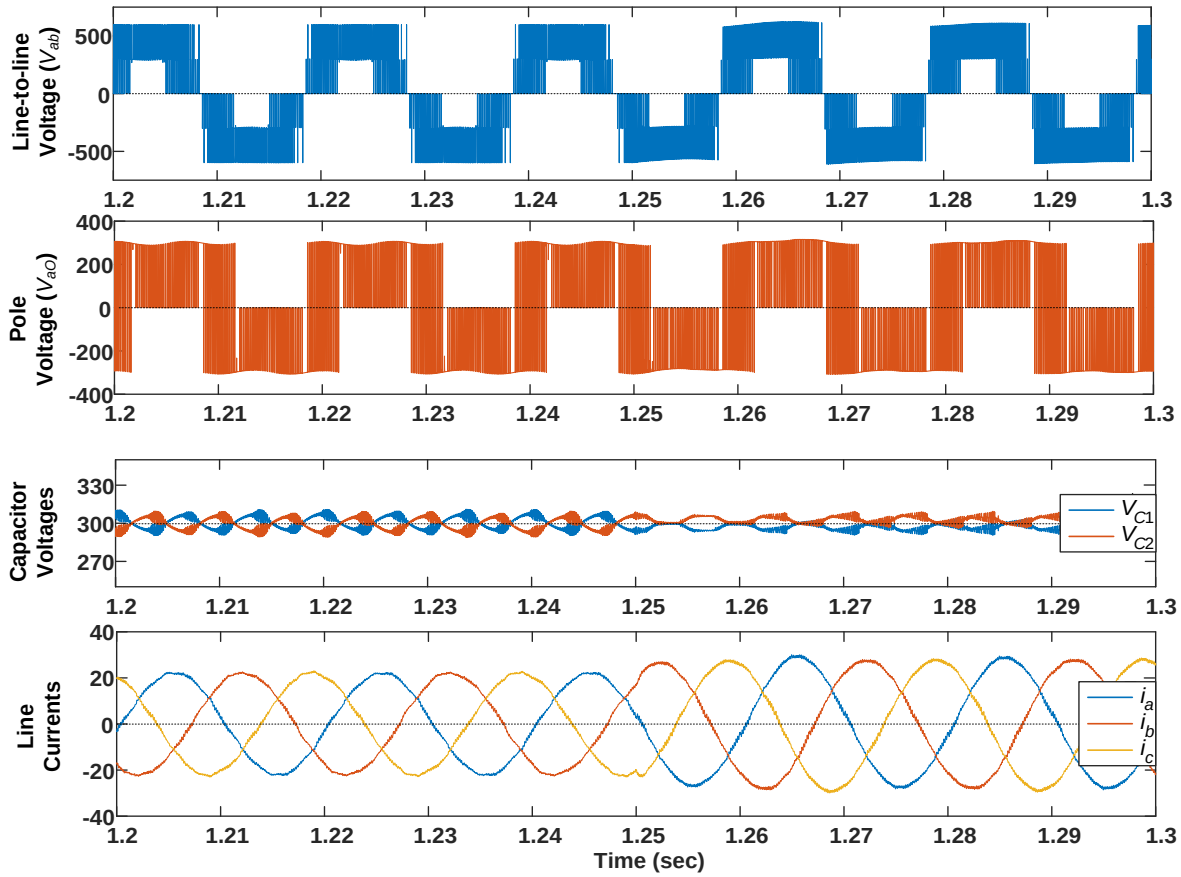
For the proper operation of Z-source network, however, the shoot-through states need to be inserted as discussed in Section II. The UST and LST intervals are maintained equal for proper operation of VSI. In the conventional 3L VSI, the ST states (LST and UST) are inserted with the help of the small vectors. the redundant switching states of the same small voltage vector can be used to insert the shoot-through states in any of the regions $T_0 - T_3$ (Figure 5-16 (b)) without increasing the number of commutations. Therefore, the small voltage vector duty ratio is distributed equally to its redundant switching states for facilitating the shoot-through states. For example, when V_{ref} is located in T_2 the switching sequence and the insertion shoot through states is shown in Figure 5-17. Here, the distribution factor for the small vector V_{S1} is $p = 0.5$, therefore $d_{100} = d_{211} = d_y$ (Figure 5-18). UST is added in the switching state “100” and LST is added in the switching state “211”.

On the other hand, in hybrid 2/3L NPCI, the switching sequences: SS1 and SS2 need to be used to avoid the extra commutations. Therefore, the redundant switching states of same small vector cannot be used. Figure 5-18 shows the duty ratio distribution of different switching states for SS1 when V_{ref} is located in Δ_4.

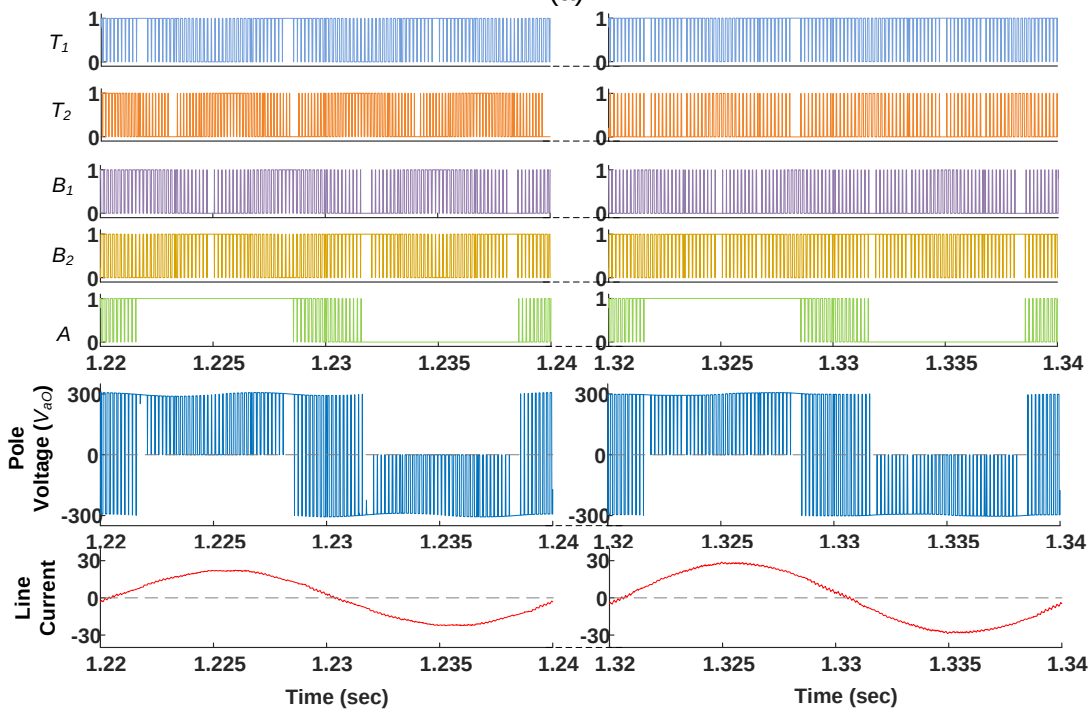
5.5.5 Performance Evaluation of Hybrid 2/3L ZNPCI

To verify the proposed virtual vector modulation for hybrid 2/3L ZNPCI, simulations were performed in MATLAB SIMULINK. The Z-Source network with two 5mH inductors and 2200µF capacitors are used for simulation. The input voltage is assumed as V_{PV} =600 V. A switching frequency of 3 kHz was used for analysis. A standalone star connected RL load of 10Ω and 5mH per phase was used. Only switching sequence SS1 is used in this simulation results, however, SS2 and combination of SS1 and SS2 can be used. UST is added in the "100" state interval and LST was added in "221" state interval (refer Figure 5-15(a)) such that: for $\theta_1 \leq 30°$, $d_{LST} = d_{UST} = d_{max} = d_{221}$ and for $\theta_1 > 30°$, $d_{UST} = d_{LST} = d_{max} = d_{100}$ in the sector-1 (where d_{max}=maximum possible shoot through interval). i.e., the small vector durations are completely used to produce the corresponding ST states.

Figure 5-19 and Figure 5-20 show the simulation results for hybrid 2/3L NPCI with the proposed VV modulation without and with the ST states inserted respectively. Two modulation indices m=0.65 and m=0.82 are used for simulation. The pole voltage V_{aO} (across the output terminal and DC-link midpoint) is switched as 1) 3L NPCI when the the reference magnitude is equal maximum or minimum and 2) 2L VSI when the reference magnitude is medium. The capacitor voltages remain balanced for all the operating conditions. Since the small vector duty ratios are completely used for shoot through states, the boost ratio, varies inversely with the modulation index. Further analysis with the SS2 and partial insertion of ST intervals for functions like simple boost and constant boost [145] will be considered for future research objective.

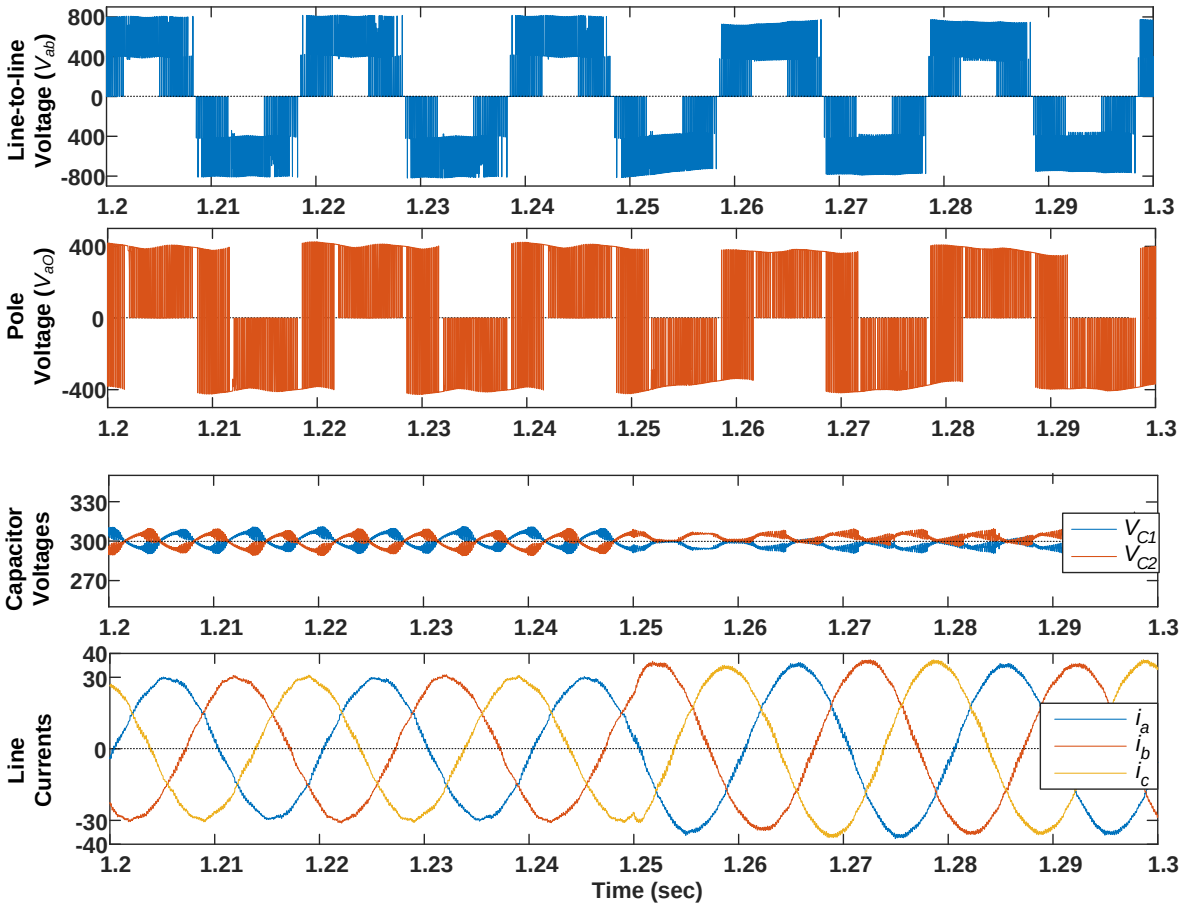


(a)

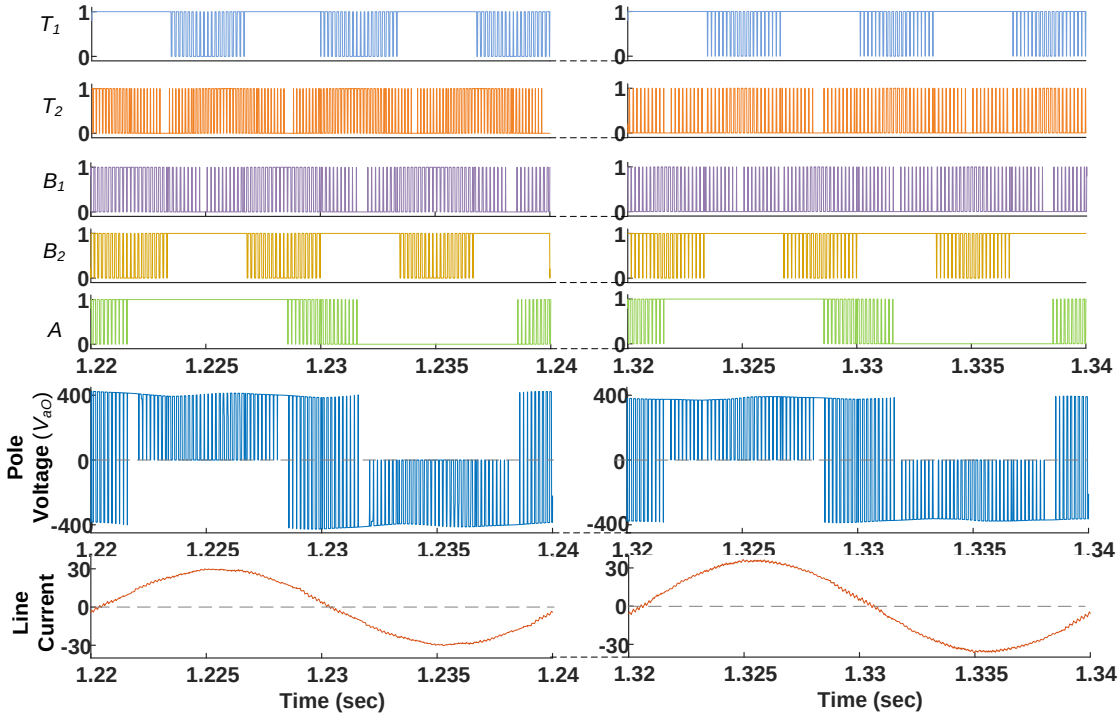


(b)

Figure 5-19 Simulation results (a) without ST states and (b) Zoomed View along with the switching signals for $m = 0.65$ (from t=1.2 sec to t=1.25 sec) and $m = 0.82$ (after t=1.25 sec).



(a)



(b)

Figure 5-20 Simulation results (a) with ST states and (b) Zoomed View along with the switching signals for $m = 0.65$ (from t=1.2 sec to t=1.25 sec) and $m = 0.82$ (after t=0.25 sec).

5.6 Hybrid 2/3L NPCI with Unequal DC Capacitor Voltages

For the renewable energy applications, usually energy source is associated with a storage system to smoothen the fluctuations in the source power. An example of hybrid storage connected at the input side of hybrid 2/3L NPCI is shown in Figure 5-21.

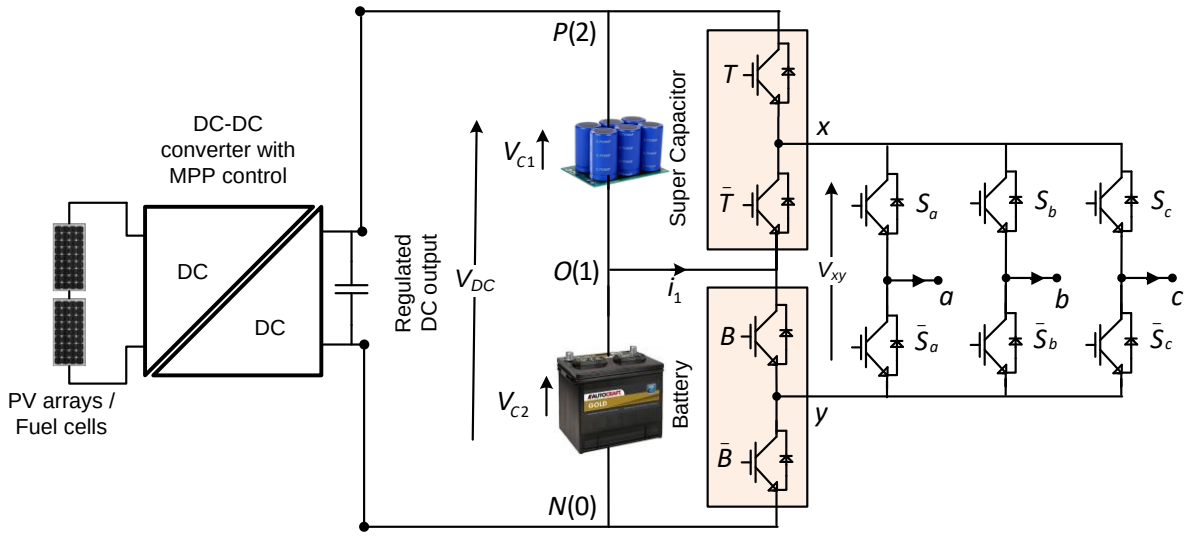


Figure 5-21 Hybrid 2/3L NPCI energized with renewable energy source and hybrid energy storage system.

5.6.1 Switching Sequence for DC Voltage Unbalance Compensation

In practical applications, the DC-link of the hybrid 2/3L NPCI hybrid energy sources as shown in Figure 5-21 need to operate for the voltage variations across the super capacitor and battery during charging, discharging and load sharing conditions. Figure 5-22 (a) and (b) shows the SVD of hybrid 2/3L NPCI for two cases of unequal DC Voltages: $V_{C1} > V_{C2}$ and $V_{C1} < V_{C2}$ respectively.

Based on the concept of virtual vector, the two redundant small vectors are replaced with a new virtual vector formed by combination of these two small vectors. The obtained SVD of hybrid 2/3L NPCI is shown in Figure 5-22 (c). The expressions of virtual vectors are listed in Table 5-11. Two new switching sequences show in Figure 5-23 are used such that the redundant small vectors are switching for equal duration in each switching cycle. The modulation discussed in section 5.5 is used to find the duty ratios of the voltage vectors.

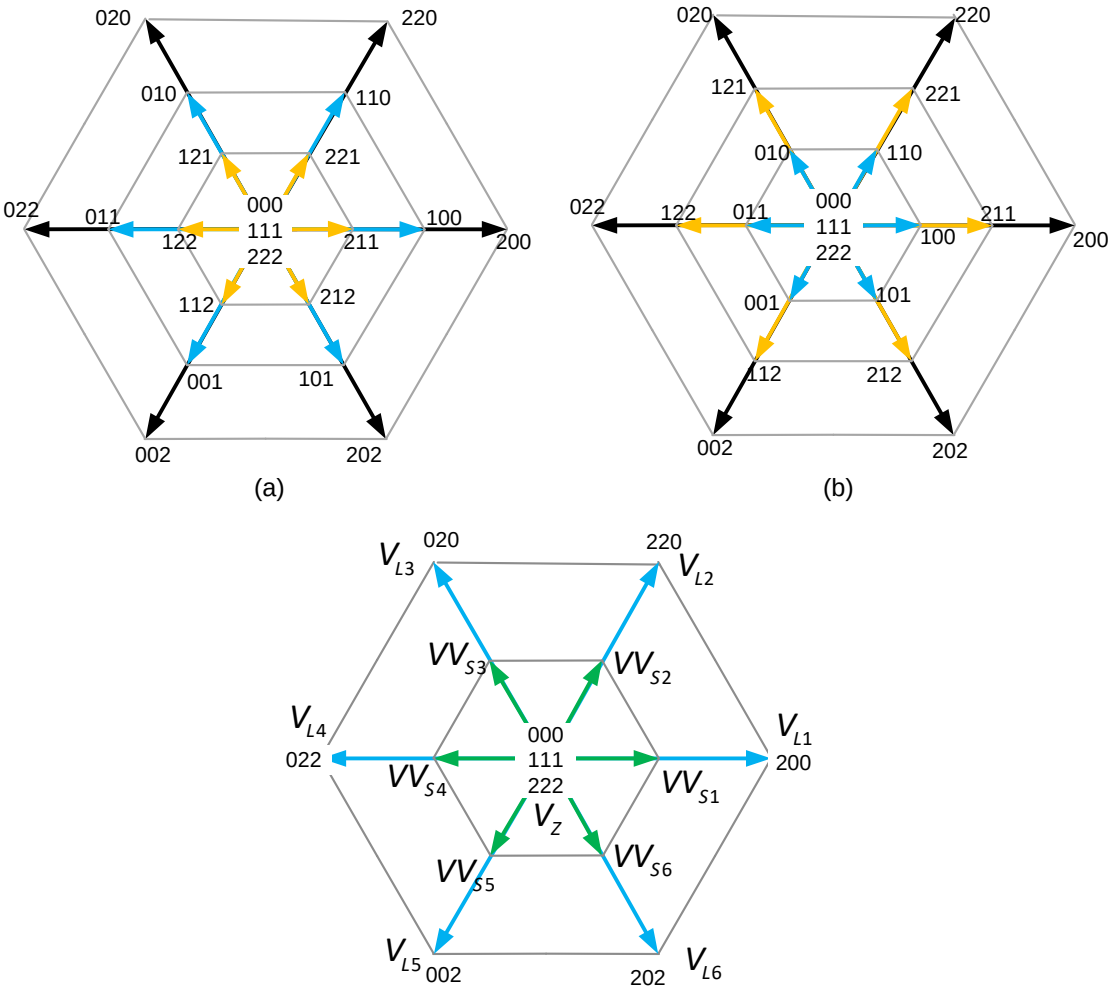


Figure 5-22 SVD of the hybrid 2/3L NPCI for (a) $V_{C1} > V_{C2}$, (b) $V_{C2} > V_{C2}$ and (c) when small vectors are replaced with the virtual small vectors.

Table 5-11 List of virtual vectors in hybrid 2/3L NPCI SVD for unbalance DC voltage compensation

Virtual vector	Expression
VV_{S1}	$(V_{211}+V_{100})/2$
VV_{S2}	$(V_{221}+V_{110})/2$
VV_{S3}	$(V_{121}+V_{010})/2$
VV_{S4}	$(V_{122}+V_{011})/2$
VV_{S5}	$(V_{112}+V_{001})/2$
VV_{S6}	$(V_{212}+V_{101})/2$

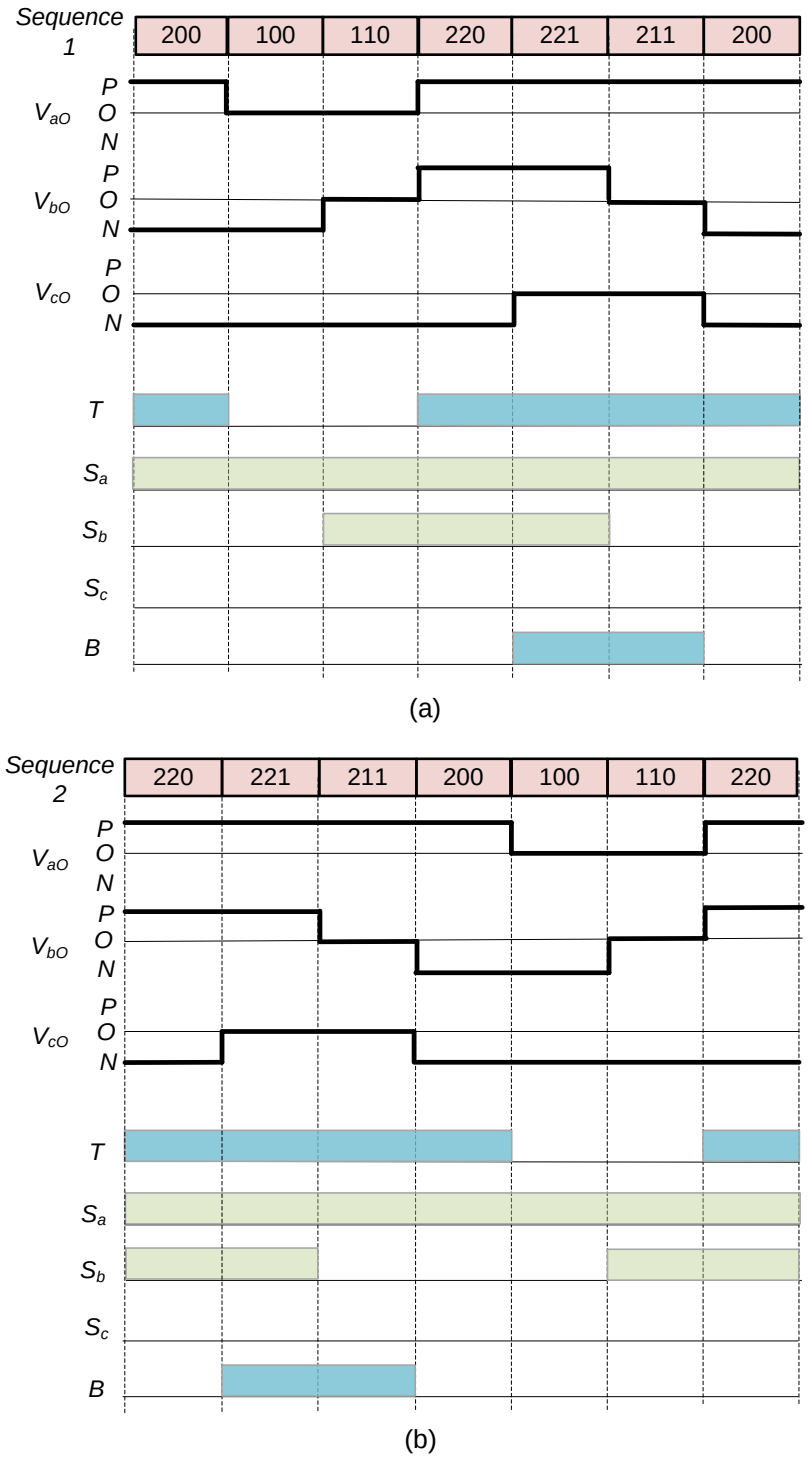
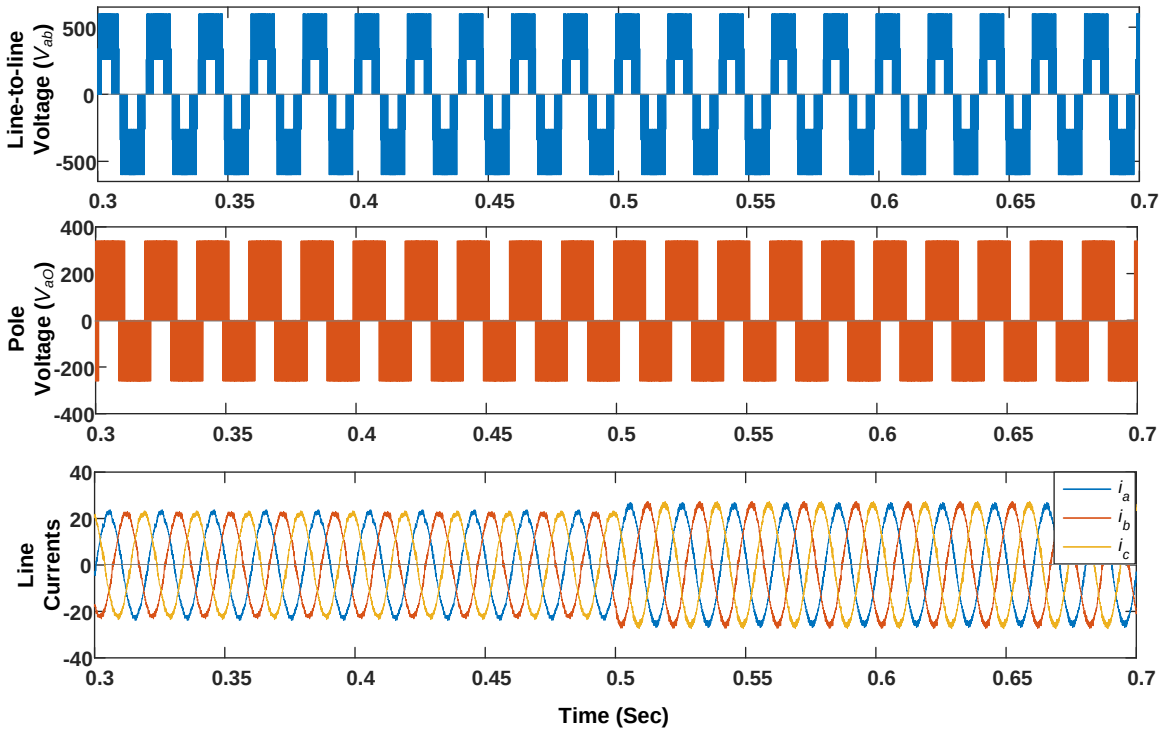


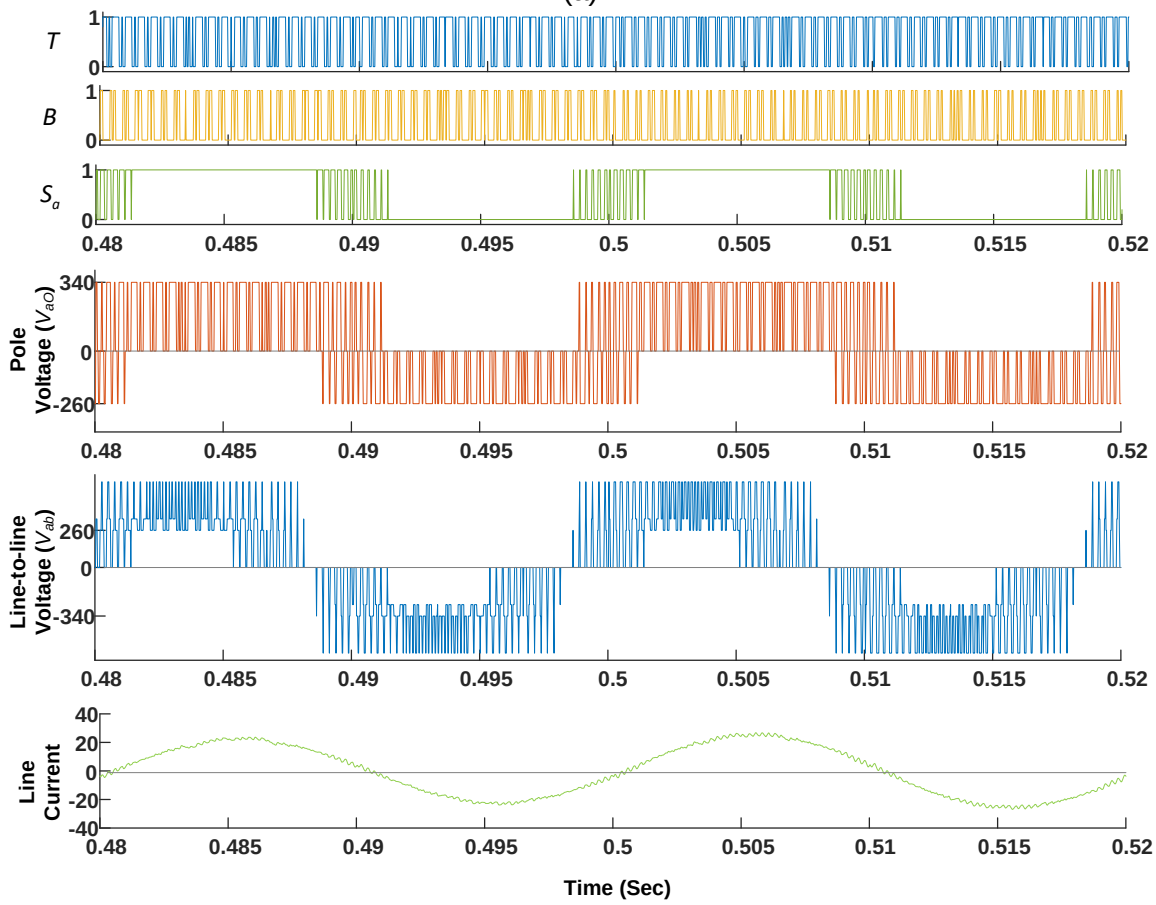
Figure 5-23 switching sequences for DC voltage unbalance compensation

5.6.2 Performance Evaluation

The performance is investigated in MATLAB-Simulink using following parameters: DC link voltage=600V, switching frequency=3kHz, DC link capacitors=2200µF and RL load: R=10Ω/phase; L=5mH/phase. Simulation results of hybrid 2/3L NPCI with unbalanced DC sources such that V_{C1} =340V and V_{C2} =260V are presented in Figure 5-24 and Figure 5-25 for different modulation indices.

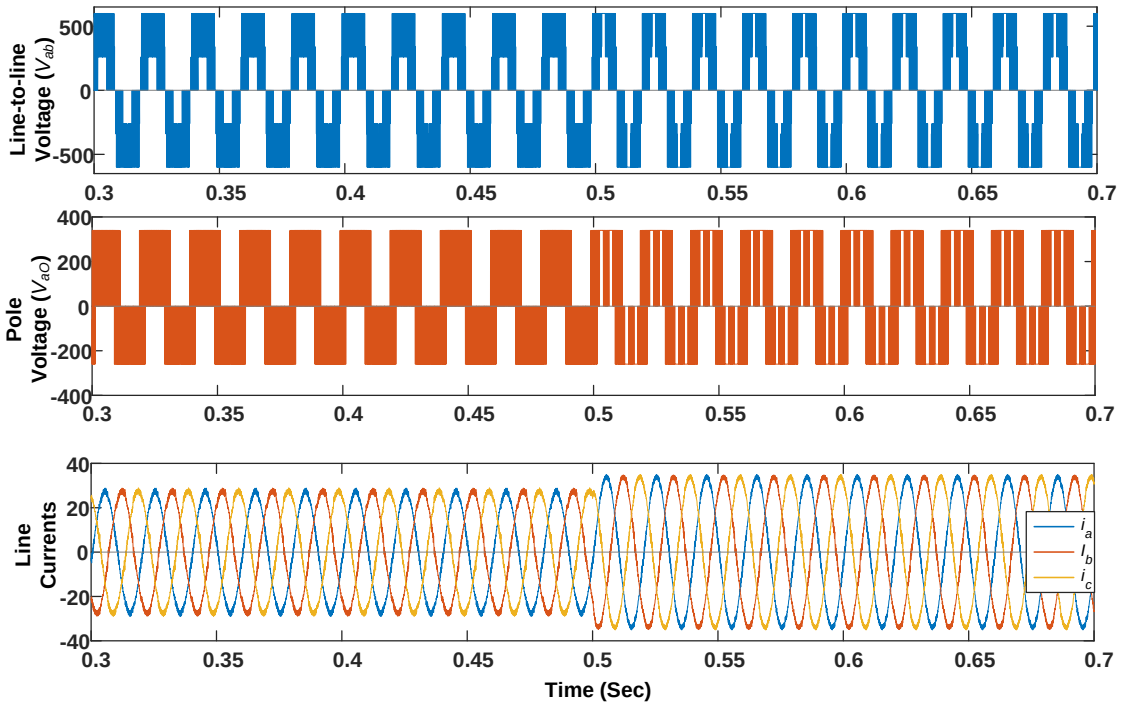


(a)

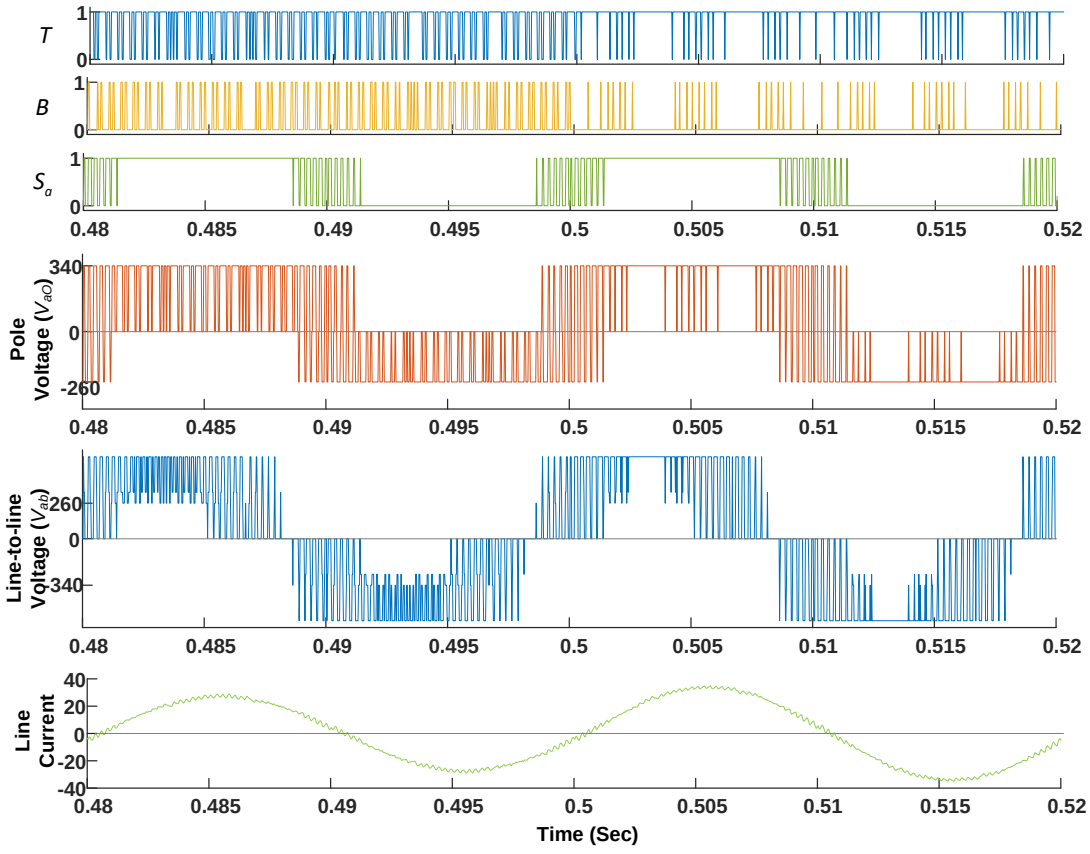


(b)

Figure 5-24 Simulation results of hybrid 2/3L NPCI with unbalanced DC sources ($m=0.65$ from t=0.3 sec to t=0.5 sec and $m=0.75$ after t=0.5); (b) Zoomed view of (a) and switching signals.

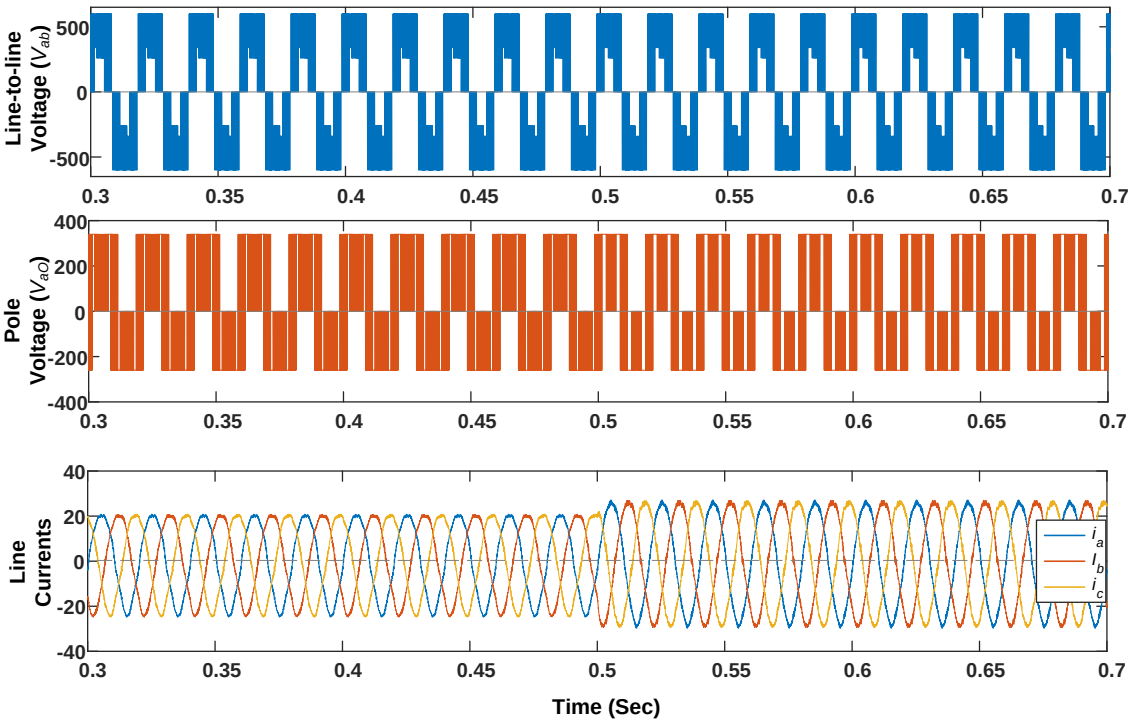


(a)

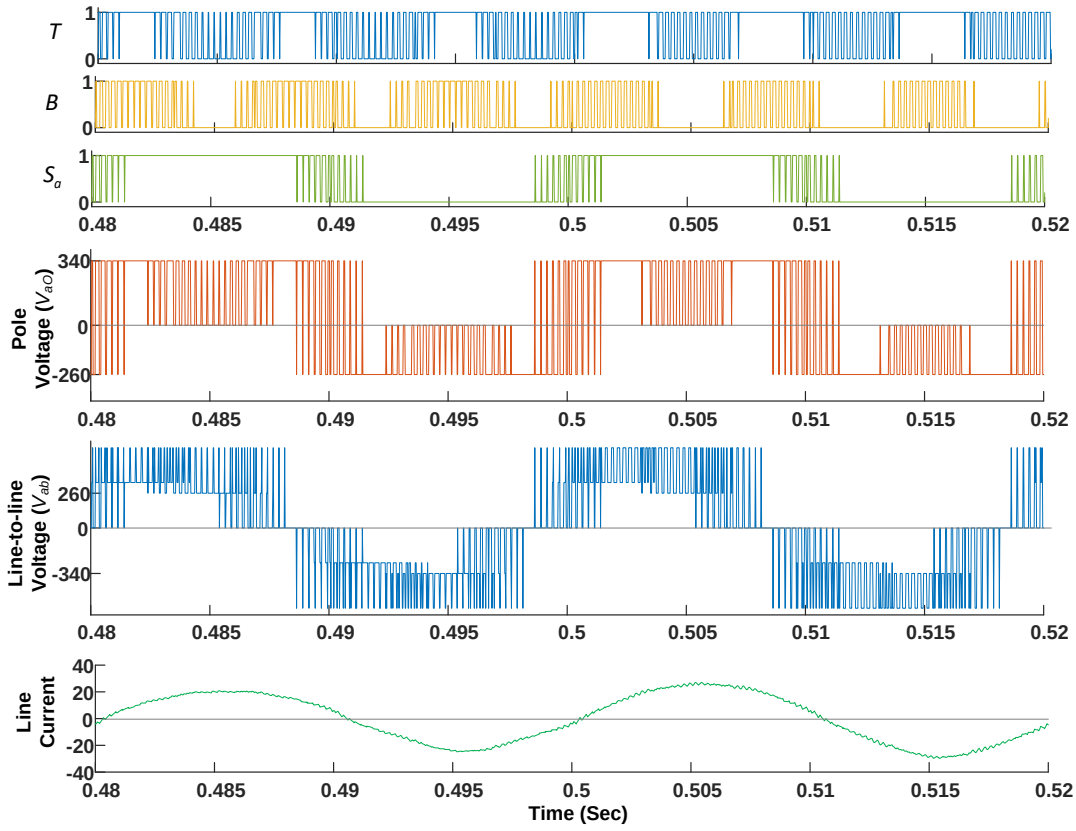


(b)

Figure 5-25 Simulation results of hybrid 2/3L NPCI with unbalanced DC sources ($m=0.8$ from t=0.3 sec to t=0.5 sec and $m=1.0$ after t=0.5 sec); (b) Zoomed view (a) and switching signals.



(a)



(b)

Figure 5-26 Simulation results of hybrid 2/3L NPCI with unbalanced DC sources using conventional VV-based modulation ($m = 0.65$ from t=0.3 sec to t=0.5 sec and $m = 0.8$ after t=0.5 sec); (b) Zoomed view (a) and switching signals.

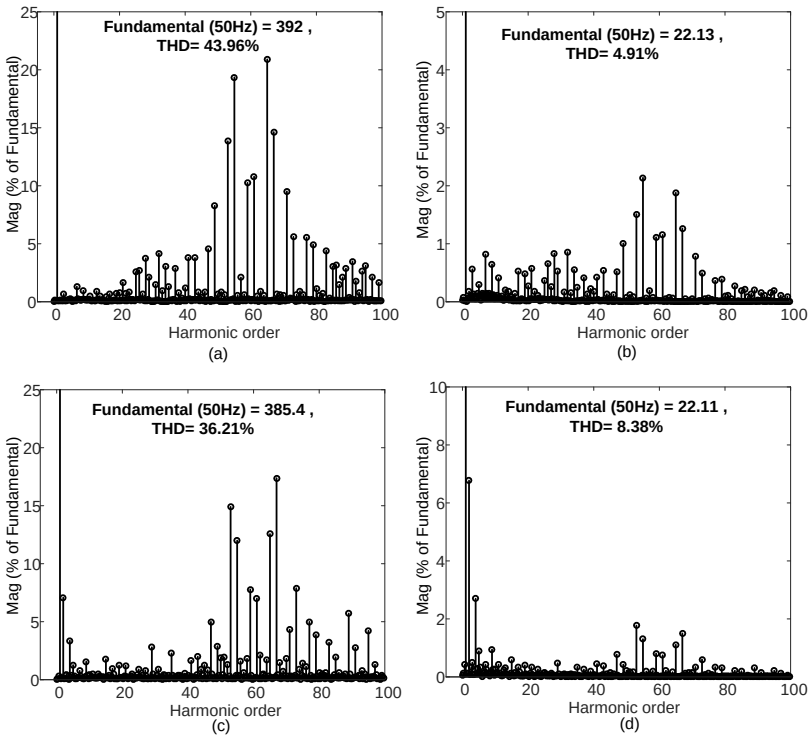


Figure 5-27 THD Comparison of modulation methods for m=0.65: new VV-based modulation (a) Line-to-line voltage and (b) line current and conventional VV-based modulation (c) Line-to-line voltage and (d) line current.

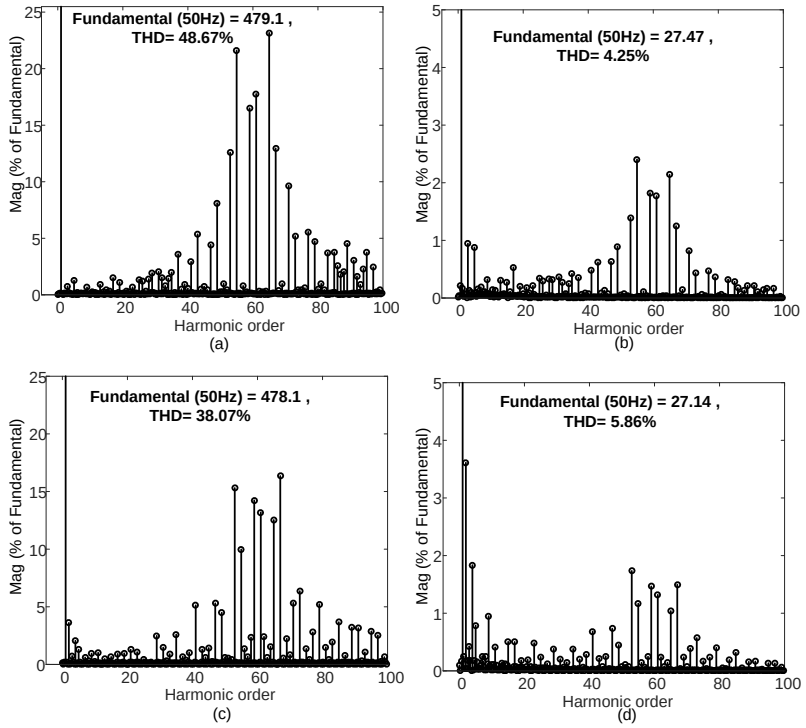


Figure 5-28 THD Comparison of modulation methods for m=0.8: new VV-based modulation (a) Line-to-line voltage and (b) line current and conventional VV-based modulation (c) Line-to-line voltage and (d) line current.

From the simulation results, it is evident that the unbalance is present in the pole voltage V_{aO} measured across the ac terminal and dc-Link midpoint O. The peak in positive side measures 340V, while the peak in negative side measures 260V. However, the line-to-line voltage V_{ab} is symmetrical about the time axis resulting in zero DC component. Similarly, the line current is also sinusoidal with minimum distortion.

For comparison purpose, performance of the hybrid 2/3L NPCI with unbalanced sources is examined using the VV-based modulation discussed in Section 5.2.1. Figure 5-26 shows the voltage and current waveforms at two modulation indices m=0.65 and m=0.8 under the same operating conditions discussed above. The effect of unbalance is clearly observed in the ac side waveforms. Figure 5-27 and Figure 5-28 show the comparison of THDs with the two modulation strategies. From Table 5-12, it is clear that THD of line-to-line voltage is slightly increased in new VV-based modulation, but the effect of unbalanced input DC sources is completely eliminated and resulted in negligible 2nd harmonic content.

Table 5-12 THD Comparison of Modulation strategies for DC source voltage unbalance compensation

Performance Parameter	Modulation index (m)					
	0.65		0.8		1	
	VV	new	VV	new	VV	new
% THD of Line Voltage	36.2	43.96	38.07	48.67	36.04	38.98
% THD of Line Current	8.38	4.91	5.96	4.25	4.10	4.12
% 2nd Harmonic	6.86	0.18	3.53	0.07	0.69	0.16

5.7 Conclusion

A hybrid 2/3L NPCI derived based on the non-NTV modulation principle is studied in detail. The topology can reduce the active switch and eliminates the clamping diodes compared to conventional 3L NPCI. Two modulation strategies are developed compared with the help of simulation results. A new virtual vector modulation scheme is proposed which uses two small vectors for V_{ref} located in all the sub-triangle regions. This property of the proposed modulation enables the integration of Z-source network and unequal DC voltages across capacitors. All the modulation approaches discussed here are designed to minimize the number of commutations. The performance of the hybrid 2/3L NPCI is in between the 2L and 3L inverters since the medium magnitude phase is switched as 2L inverter, while, the minimum and maximum magnitude phases switch as 3L NPCI. The proposed modulation methods are validated with the help of simulation results.

Chapter 6: MULTILEVE MULTI-POINT CLAMPED INVERTERS WITH REDUCED DEVICE COUNT

[In this chapter, MPCI topologies are further investigated for higher voltage levels. Two modified T-type phase legs are derived from 3L T-type NPCI. This topology is extended to higher voltage levels by adding half bridge modules either at top and bottom or at the output ac terminal. It can reduce one switching stress per phase arm and does not require clamping diodes or bidirectional switches. This MPCI topology is further modified to minimize the active switch count in various possible cases thereby resulting multiple reduced switching state (RSS) MPCIs. Detailed analysis of SVD and voltage vector selection for such RSS MPCIs are investigated and modulation algorithms are proposed. A four-level (4L) RSS MPCI and two five-level (5L) RSS MPCI topologies are studied in detail with the help of MATLAB simulation results]

6.1 Introduction

Recently, the multilevel converters have found acceptance in low-power renewable energy source integration applications [146] like wind, PV, Fuel Cells, etc. However, the classical MPCI topologies like diode clamped inverter (DCI) are less attractive due to the increased number of clamping diodes as the voltage level increases. Therefore, researchers paid attention to minimize the Power Semiconductor Devices (PSD) and gate driver circuits through various approaches. Most of the recently proposed MLI topologies are hybrid MLI (H-MLI) [147]–[151] formed by combination of two or more lower level MLIs or 2-level (2L) inverters. The comparative analysis (refer Table 1-2) of newly proposed MPCI topologies reveal that: (i) the number of active switches are same as that of the conventional DCI, but the clamping diodes are significantly reduced. (ii) The elimination of clamping diodes results in increased voltage stress on the active switches demanding of high blocking voltage switches.

In this context, this chapter presents a modified T-type MPCI topology that exhibits a reduction in 1) PSD count and 2) Total voltage stress of the switching devices compared to conventional topologies. The inverter can easily be constructed and can be extended to higher voltage levels by cascading two-level modules at the midpoint or top and bottom terminals. The resultant topologies show similarity with the diode clamped inverter (DCI) topology without utilizing clamping diodes or bi-directional switches. The topology formation and modulation methods are discussed with the help of MATLAB simulation.

Similar to the hybrid 2/3L NPCI discussed in chapter 5, MPCI topologies with reduced number of active switches are further investigated for higher voltage levels. The reduction in the switch count is achieved by making a portion of the inverter called multilevel clamping unit (MCU) common to all the phases. Effect of common clamping of MCUs lead to reduction of number in

available switching states (SSs). Therefore, MPCI topologies thus formed by common-clamping MCUs are referred as reduced switching state (RSS) MPCI (i.e., RSS MPCI) in this chapter. A 4L and 5L RSS MPCI topologies are developed and modulation techniques are investigated in detail in the following sections.

6.2 Modified T-Type 3L MPCI Topology

6.2.1 Topology Synthesis

Figure 6-1 shows two possibilities for formation of three-level (3L) T-type inverter leg. The bidirectional switch of 3L T-type leg can be either in common emitter or common collector configuration comprising two power switches S_{x2}-S_{x4} *(x=a, b) in each leg. Two* modified NPCI legs deduced from 3L T-Type NPCI are as follows.

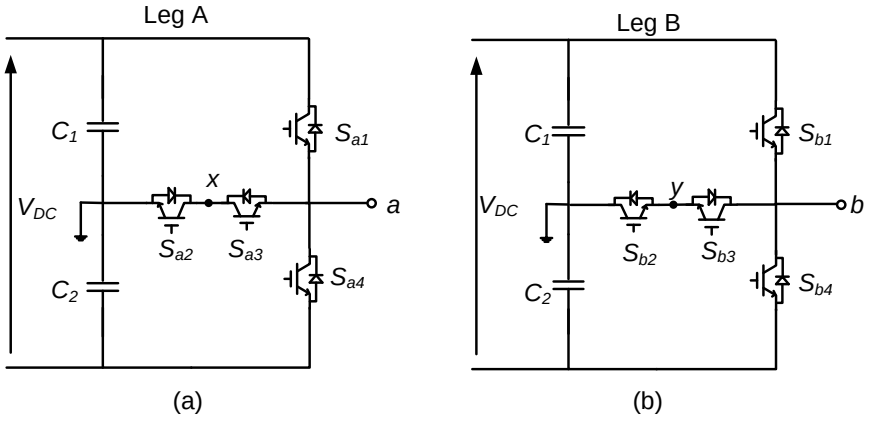


Figure 6-1 T-type Inverter with (a) Common collector; (b) Common emitter configuration [43]

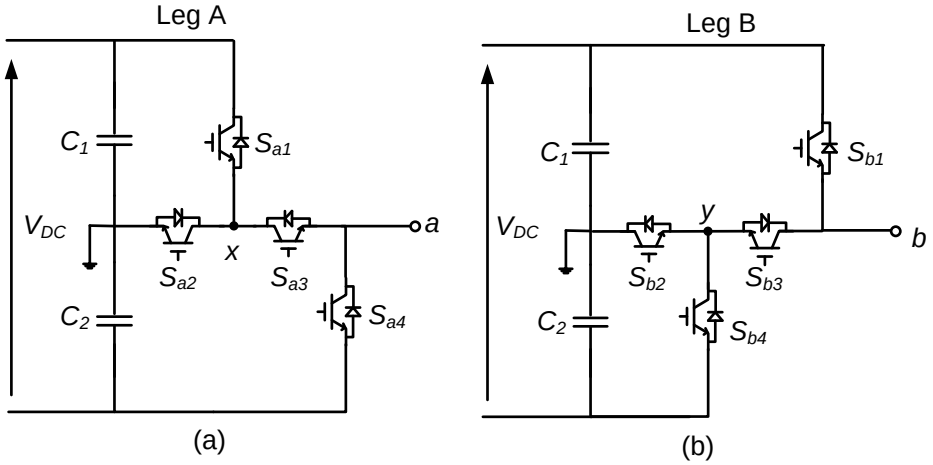


Figure 6-2 Two modified 3L inverter legs.

Figure 6-2 (a) shows one leg of the modified T-type NPCI inverter (leg A). It is realized by connecting emitter terminal of the upper switch S_{a1} to the intermediate point "x" between two switches S_{a2} and S_{a3} in the common collector configuration. Similarly, Figure 6-2 (b) shows the leg B of modified T-type NPCI. It is realized by connecting the collector terminal of the bottom switch S_{b4} to the intermediate point "y" between two switches S_{b2} and S_{b3} in the common emitter configuration.

6.2.2 Circuit Description and Principle of Operation

Figure 6-3 show the two modified T-type inverter legs with rearranged switch numbering. The switching pair $\left(Q_{xy}, \overline{Q}_{xy}\right)$ follows complementary switching logic with switching constraint defined as $Q_{xy} + \overline{Q_{xy}} = 1$; where $x = a, b$ and $y = 1, 2$. The topology requires only eight power switches along with their antiparallel diodes but without any clamping diodes and bidirectional switches. Three voltage levels are obtained at AC terminals V_{a0} and V_{b0}. The switching states for leg A and leg B of the modified T-Type NPCI are listed in Table 6-1and Table 6-2 respectively. Q_{xy} is 1 when the corresponding switch is ON, 0 when it is OFF.

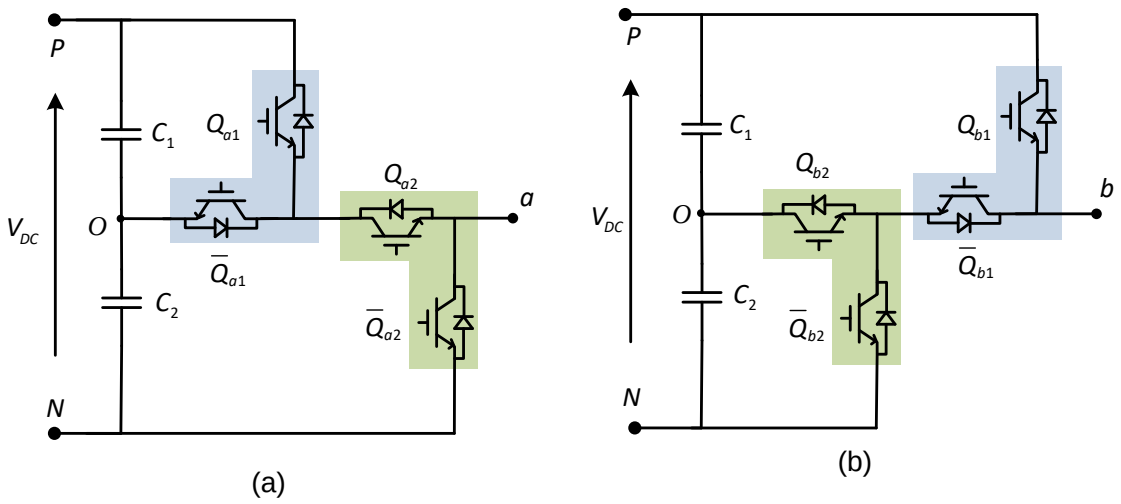


Figure 6-3 Modified T-type three level legs: (a) leg A and (b) leg B.

Table 6-1 Switching Table of modified T-type inverter leg A

V_{a0}	Q_{a1}	$\overline{Q}_{a1}$	Q_{a2}	$\overline{Q}_{a2}$
V_{C1}	1	0	1	0
0	0	1	1	0
$-V_{C2}$	0/1	1/0	0	1

Table 6-2 Switching table of modified T-type inverter leg B

V_{b0}	Q_{b1}	$\overline{Q}_{b1}$	Q_{b2}	$\overline{Q}_{b2}$
V_{C1}	1	0	1/0	0/1
0	0	1	1	0
$-V_{C2}$	0	1	0	1

6.3 Extension to Higher Voltage Levels (Multilevel Operation)

The modified T-Type NPCI can be extended to higher voltage levels by simple addition of H-bridge cells.

Type-1: Figure 6-4 shows the extension of modified T-type NPCI inverter legs (leg A and leg B) for higher voltage levels with addition of H-bridge cells at top and /or bottom.

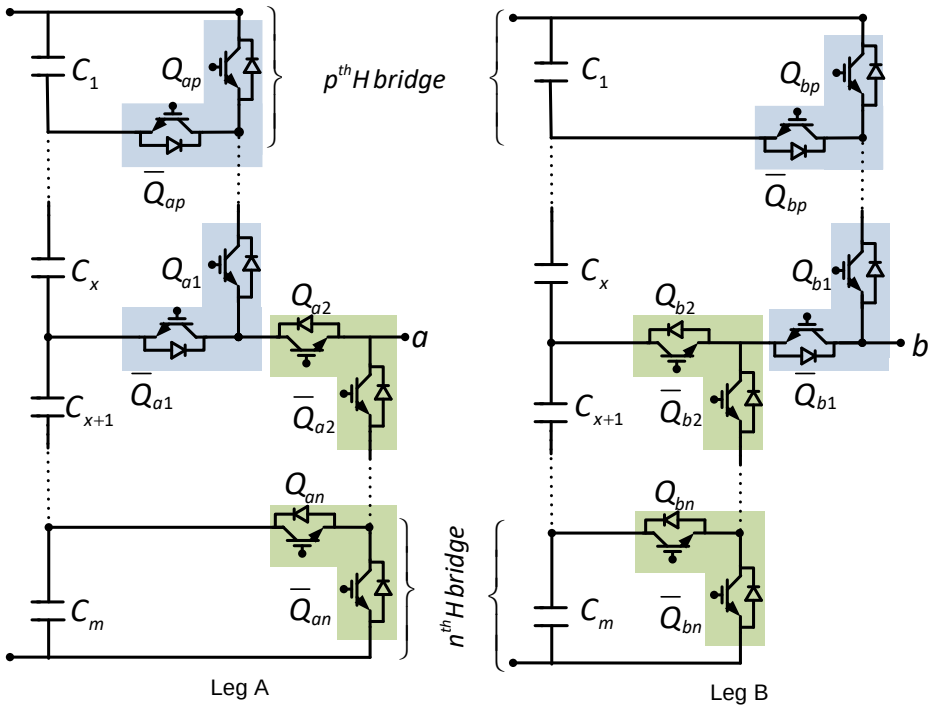


Figure 6-4 Addition of half bridge cells at top and bottom to increase the voltage levels in leg A and leg B (Type-1).

Type-2: Figure 6-5 shows another possible arrangement of modified T-type NPCI topology for extending the phase voltage levels using H-bridge cells. It is obtained by cascading the similar structure at the output of each modified T-type NPCI topology.

The number of active switches in the modified T-type multipoint clamped inverter (MPCI) leg is similar to conventional diode clamped inverter (DCI) leg and other counterparts. However clamping devices and bidirectional switches are completely eliminated. Moreover, it can be shown in further analysis that the modified T-type MPCI has reduced total switch voltage stress in this inverter legs. Leg A and leg B are independent and can be used as an inverter leg for single-phase or multiphase systems individually.

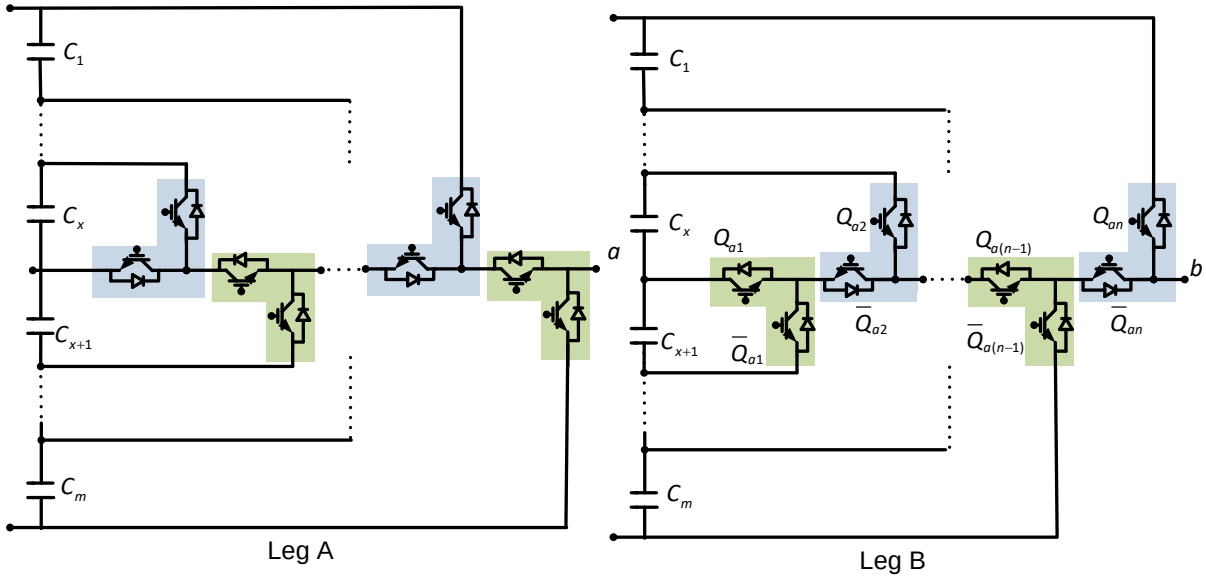


Figure 6-5 Increasing the voltage levels by cascading the modified T-type legs at the output terminal (Type-2).

6.4 Three-Phase 5L Modified T-Type MPCI

The circuit diagram of the three-phase 5L modified T-type MPCI inverter is shown in Figure 6-6. The switching states of proposed inverter referring to generalized phase leg are listed in Table 6-3. T_{xi} is 1 when the corresponding switch is ON, 0 when it is OFF and X indicates don't care condition. X is assumed for the switches in non-conducting path for generating corresponding voltage level because they do not influence the ac side voltage of the inverter. The relation between DC side node currents i_{jx} ($j=1,2,3,4,5$) and phase current i_x, the phase voltage V_{xo} with respect to the DC side mid-point are also shown in Table 6-3. The phase current will flow through one of DC side intermediate nodes and the corresponding capacitor voltage will appear on the ac side based on the switching state. The don't care conditions (X) offer different possibilities for obtaining the voltage level but similar to DCI, the proposed topology will not have phase voltage redundant states to balance the DC link capacitor voltages $V_{C1}-V_{C4}$ Figure 6-7 shows various operating modes of the 5L modified T-type MPCI leg. The dark line indicates conduction path in order to obtain different voltage levels.

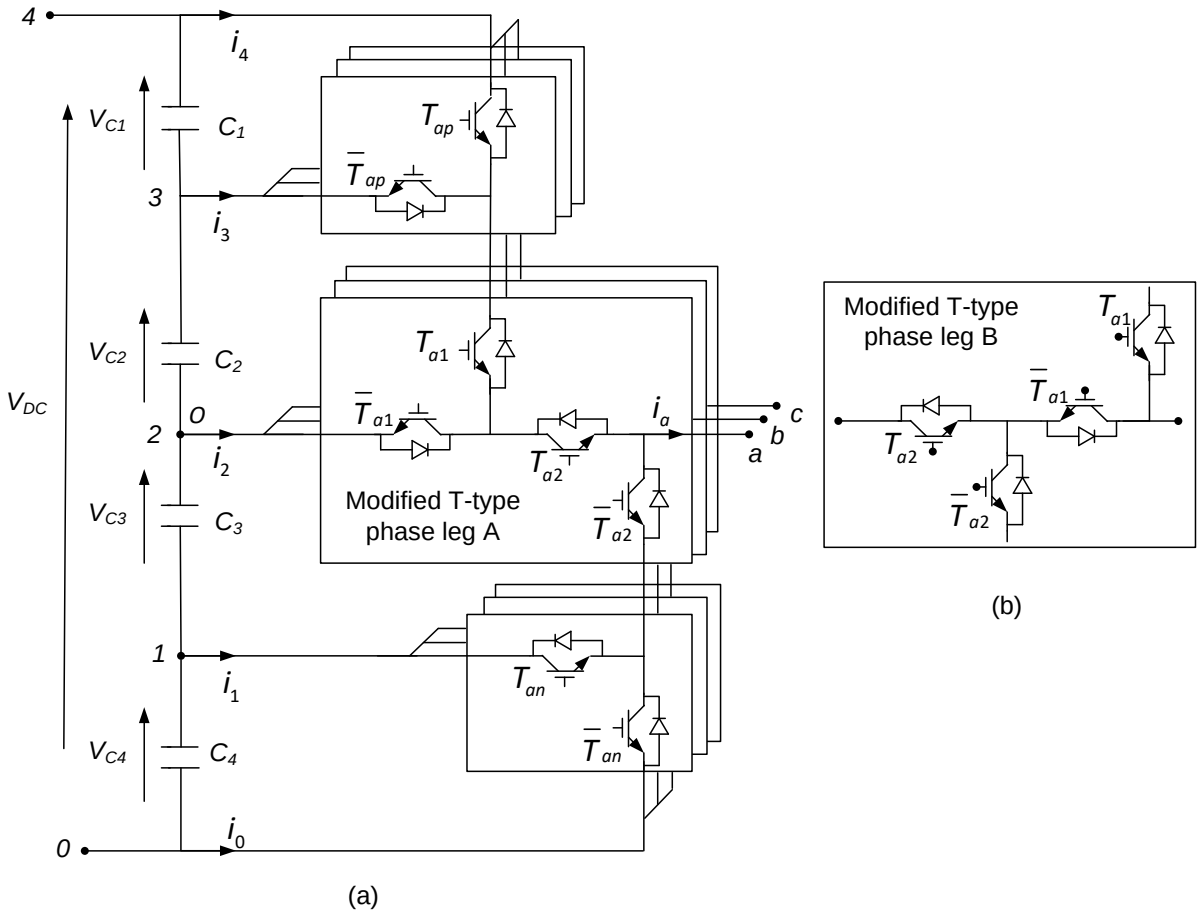


Figure 6-6 Circuit diagram of (a) proposed 5L modified T-type MPCI with leg A which can be replaced with (b) Modified T-type phase leg B.

Table 6-3 Possible switching states of proposed inverter with one leg operation

Switching Signals						Dc side Intermediate node currents					AC side voltages
T_{x1}		T_{x2}		T_{xp}	T_{xn}	i_{0x}	i_{1x}	i_{2x}	i_{3x}	i_{4x}	V_{x0} (Notation)
leg a	leg b	leg a	leg b								
1	X	1	1	1	X	0	0	0	0	i_x	$V_{c1}+V_{c2}(4)$
1	X	1	1	0	X	0	0	0	i_x	0	$V_{c2}(3)$
1	1	0	0	X	X	0	0	i_x	0	0	0(2)
0	0	X	0	X	0	0	i_x	0	0	0	$-V_{c3}(1)$
0	0	X	0	X	1	i_x	0	0	0	0	$-V_{c3}-V_{c4}(0)$

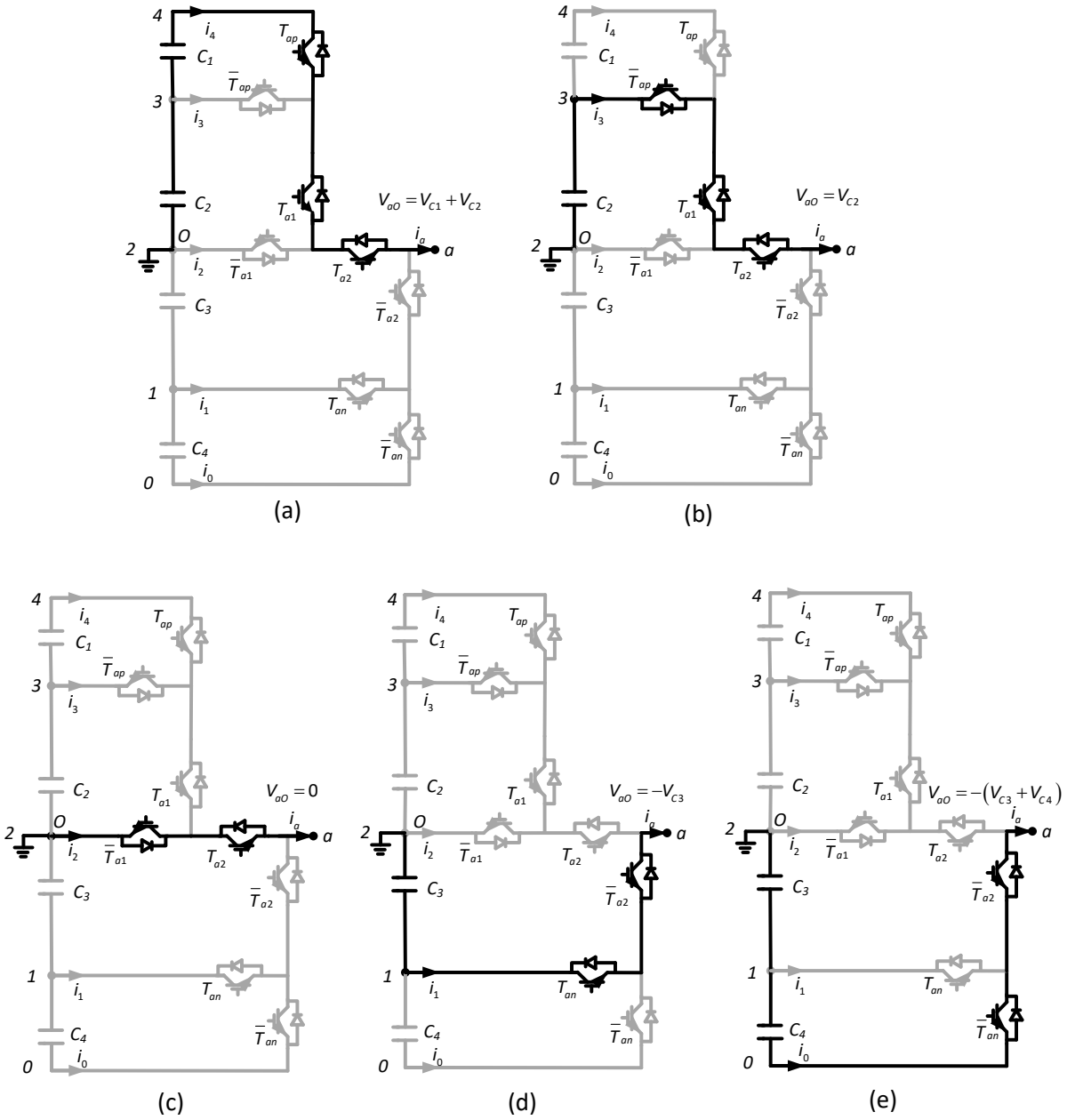


Figure 6-7 Current paths for output voltage levels of 5L modified T-type MPCI leg A.

6.4.1 Switching Signal Generation

In this section, modified T-Type MPCI is examined by with respect to stress considering all possible states of switches with don't care (X) conditions. When X=1, the modulation is considered as PWM-1 and when X=0, the modulation is considered as PWM-2 for simplicity. For example, let us consider ZERO voltage level obtained by using $T_{x1} = 1$, $T_{x2} = 0$ and consider remaining independent switches with X (don't care) are $T_{xp} = T_{xn} = 1$ for PWM-1 and $T_{xp} = T_{xn} = 0$ for PWM-2. The switching states are concisely represented in Table 6-4. The voltage stresses of different switches with PWM-1 and PWM-2 are shown in Figure 6-8. The stresses across the various switches are significantly different in both the cases for attaining different

voltage levels. The stresses across switches are uneven and maximum stresses are significantly reduced to $3V_0$ across $\bar{T}_{x1}$, $2V_0$ across $\bar{T}_{x2}$ for $V_{xO}=2V_0$ level and $2V_0$ across T_{x1} for $V_{XO}=-2V_0$ by PWM 2. The results are summarized in Table 6-5. Clearly, PWM-2 superior than PWM-1in terms of voltage stresses. i.e., the minimum voltage stresses are found when all switches with don't care (X) condition are OFF (X=0).

Table 6-4 Relation between switching states and output voltage levels

For positive states:		For zero states:		For negative states:	
$T_{x1}=T_{x2}=1;$ $V_{xO}=\begin{cases}V_{C1}+V_{C2}=2\mathrm{V}_0; & if \quad T_{xp}=1\\ V_{C1}=\mathrm{V}_0; & if \quad T_{xp}=0\end{cases}$		$V_{xO}=0;$ $if \quad T_{x1}=1;\ \mathrm{T}_{x2}=0$		$T_{x1}=T_{x2}=0;$ $V_{xO}=\begin{cases}-V_{C3}-V_{C4}=-2\mathrm{V}_0; & if \quad T_{xn}=0\\ -V_{C3}=-\mathrm{V}_0; & if \quad T_{xn}=1\end{cases}$	
PWM-1	PWM-2	PWM-1	PWM-2	PWM-1	PWM-2
$T_{xn}=1$	$T_{xn}=0$	$T_{xn}=0$	$T_{xp}=0$ $T_{xn}=0$	$T_{x2}=1$ $T_{xp}=1$	$T_{x2}=0$ $T_{xp}=0$

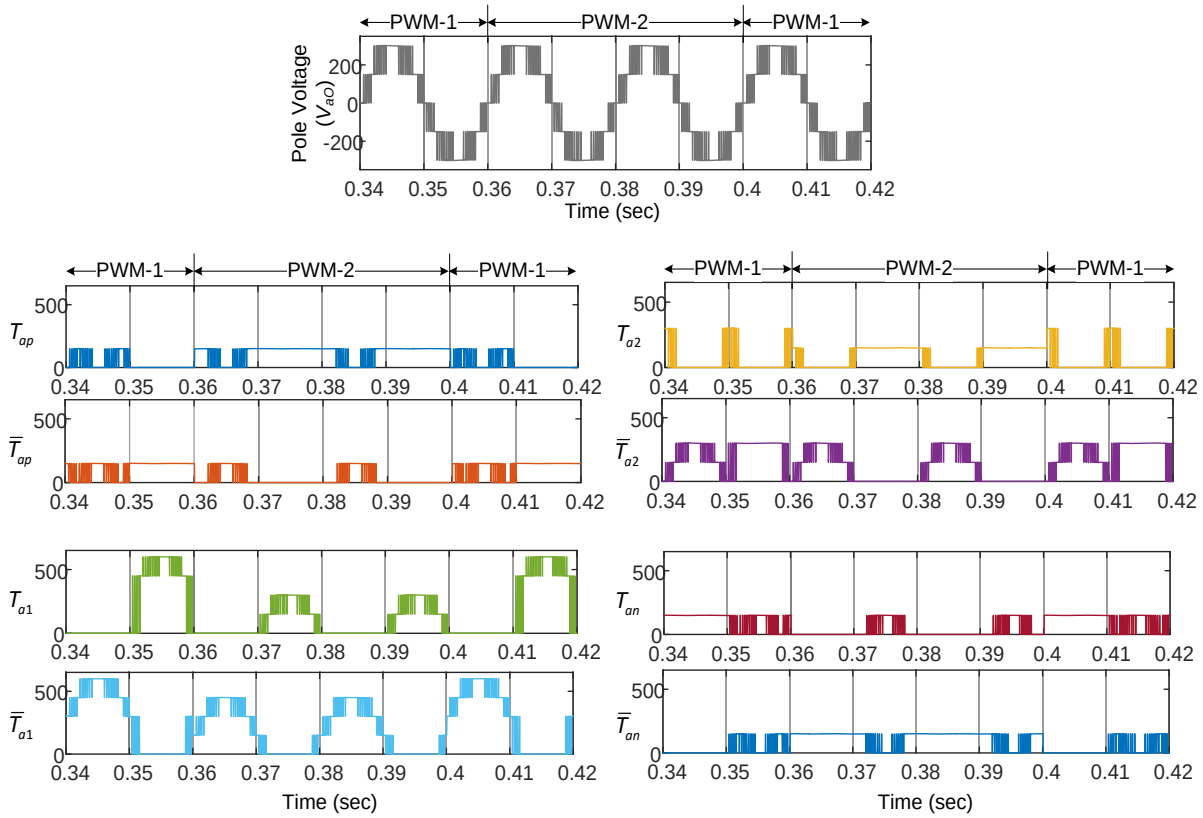


Figure 6-8 Voltage stress across each switch with corresponding voltage levels by PWM-1 (0.34 to 0.36 sec. and 0.4 to 0.42 sec.) And PWM-2 (0.36 to 0.4 sec.)

Table 6-5 Comparison of PWM-1 and PWM-2 with respect voltage stresses across each switch in single leg for different voltage levels (assuming $V_{c1}=V_{c2}=V_{c3}=V_{c4}=V_c$)

LEVELS	PWM	T_{x1}	$\bar{T}_{x1}$	T_{x2}	$\bar{T}_{x2}$	T_{x3}	$\bar{T}_{x3}$	T_{x4}	$\bar{T}_{x4}$
$2V_C$	1	0	$4V_C$	0	$2V_C$	0	V_C	0	V_C
	2	0	$3V_C$	0	$2V_C$	0	V_C	V_C	0
V_C	1	0	$3V_C$	0	V_C	V_C	0	0	V_C
	2	0	$2V_C$	0	V_C	V_C	0	V_C	0
0	1	0	$2V_C$	$2V_C$	0	0	V_C	0	V_C
	2	0	V_C	V_C	0	V_C	0	V_C	0
$-V_C$	1	$3V_C$	0	0	$2V_C$	0	V_C	V_C	0
	2	V_C	0	V_C	0	V_C	0	V_C	0
$-2V_C$	1	$4V_C$	0	0	$2V_C$	0	V_C	0	V_C
	2	$2V_C$	0	V_C	0	V_C	0	0	V_C

6.4.2 Comparison of Voltage Stress

Table 6-6 shows the comparison of voltage stresses across the switching devices of three-phase 5L MPCI topologies. It is clear that the total blocking voltage (TBV) is minimum for the 5L modified T-Type MPCI. Moreover, it does not require clamping diodes and Bidirectional switches.

Table 6-6 Comparison of blocking voltages for 5L MPCI topologies

Parameters count		Topologies					
		DCI[47]	DTT [38]	ANPC [41]	Modified ANPC [46]	Nested [39]	Modified T-Type MPCI
IGBTs		24	24	24	30	24	24
Clamping diodes		36	12	0	0	0	0
Bidirectional switches		0	6	0	0	9	0
Total blocking voltage (p.u)	IGBTs	24	36	36	42	60	36
	Diodes	36	12	0	0	0	0
DC sources/ capacitors		4	4	2	4	4	4
Floating capacitors		0	0	3	0	0	0

6.5 Reduced Switching State (RSS) MPCI Topologies

It is observed from Table 6-6 that the total number of active switches in modified T-Type MPCI still remains same as that of DCI and other topologies. Therefore, MPCI topologies are further investigated in order to reduce the active switch count. From the discussion of hybrid 2/3L NPCI discussed in Chapter 5, it is observed that, if an attempt is made to reduce the number of active switches in MPCI topology, the number of available switching states (or voltage vectors) will be affected. Hence, such topologies are considered as reduced switching state (RSS) MPCI topologies. The position of available switching states in SVD of a given RSS MPCI depends on i) total number of switching devices and ii) structure of the RSS MPCI. This effect is further explored by studying 4L and 5L RSS MPCI topologies. From Figure 6-6 (a), the don't care (X) conditions available for the outer pair of switches ($T_{xp}, T_{xn}; x = a,b,c$) of the 5L modified T-type MPCI will facilitate the development of new MPCI topologies.

6.6 Four Level (4L) RSS MPCI

A 4L RSS MPCI is developed based on the concept of common clamping shown in Figure 6-9. It is formed by connecting a half bridge cell (chopper cell) to the neutral point (N) of a three-phase 3L modified T-type NPCI. It is assumed that the voltage across the dc capacitors ($C_1 - C_3$) is held constant at $V_{DC}/3$ with the help of either external balancing circuit or supported by low voltage DC sources like PV, fuel cells, etc across each capacitor.

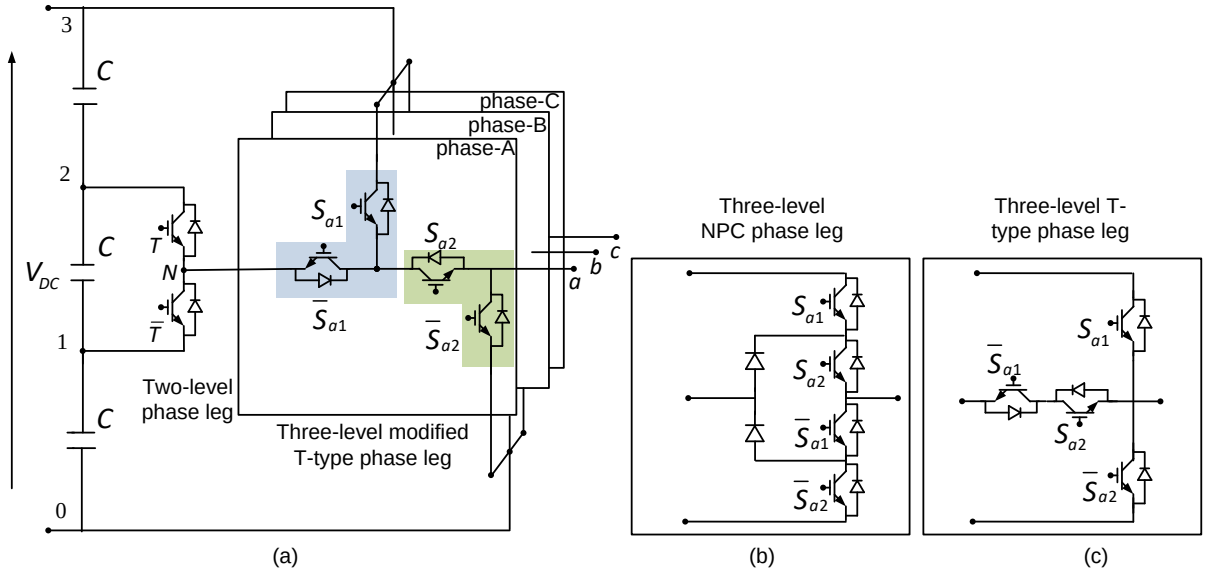


Figure 6-9 (a) 4L RSS MPCI (b) 3L NPCI and (c) 3L T-type phase leg.

The switches: S_{x1}, S_{x2}, T are considered as main switches with respective complementary pairs $\bar{S}_{x1}, \bar{S}_{x2}, \bar{T}$ (for $x = a,b,c$). The output voltage of chopper cell at point N (intermediate pole) V_N, can be either $2V_{DC}/3$ or $V_{DC}/3$ for $T = 1$ and $T = 0$ respectively. Therefore, voltage levels: V_{DC}, V_N

and 0V can be generated at the output of 3L-NPCI (The voltages are measured with respect to the bottom DC rail). All the switching states of main switches and associated voltage levels in phase leg are listed in Table 6-7. Clearly, the voltage levels $2V_{DC}/3$ and $V_{DC}/3$ cannot appear simultaneously at the output of NPCI in any of the three phases. The SVD of the 4L RSS MPCI is shown in Figure 6-10. There are only 46 switching states present instead of 64 switching states available for conventional 4L MPCI. In other words, 4 switching states are absent in each sector while synthesizing voltage vector (for example switching states: 321, 210, 211 and 221 are not available in the first sector). Further analysis is carried out by mapping V_{ref} to the first sector. Two modulation strategies are proposed for 4L RSS MPCI in the following sections.

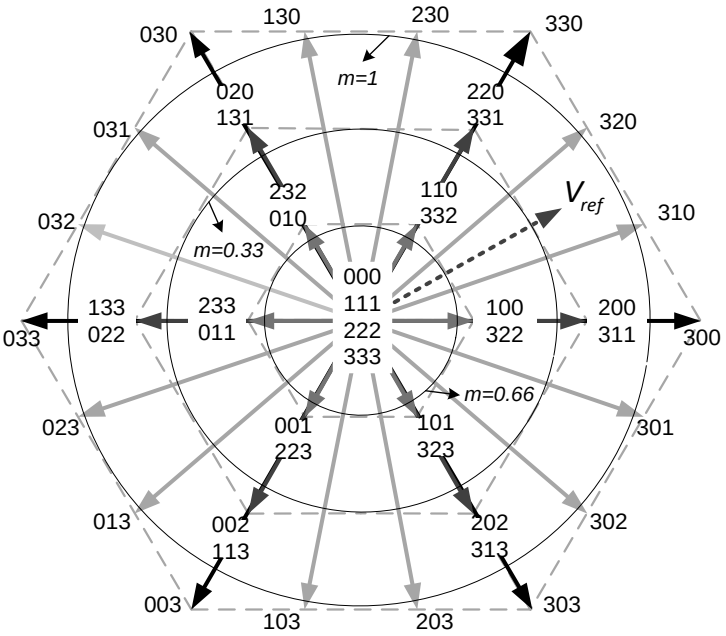


Figure 6-10 Space vector diagram of 4L RSS MPCI.

Table 6-7 Switching table for 4L RSS MPCI

Output voltage level	Notation	Phase leg		Common leg
		S_{x1}	S_{x2}	T
0	0	0	0	X
$V_{DC}/3$	1	0	1	0
$2V_{DC}/3$	2	0	1	1
V_{DC}	3	1	1	X

$x = a, b, c$ & X is 0 or 1

6.6.1 Virtual Vector (VV)-Based Modulation

Figure 6-11 shows sector-1of the 4L RSS MPCI space vector diagram. The voltage vector $V_4 = VV_4$ is the virtual vector introduced in sector-1. Various possible combinations for this vector are listed in (5.3).

$$VV_4 = \begin{cases} \frac{V_{331} + V_{311}}{2} \\ \frac{V_{200} + V_{220}}{2} \\ \frac{V_{320} + V_{322}}{2} \\ \frac{V_{332} + V_{310}}{2} \end{cases} \tag{5.3}$$

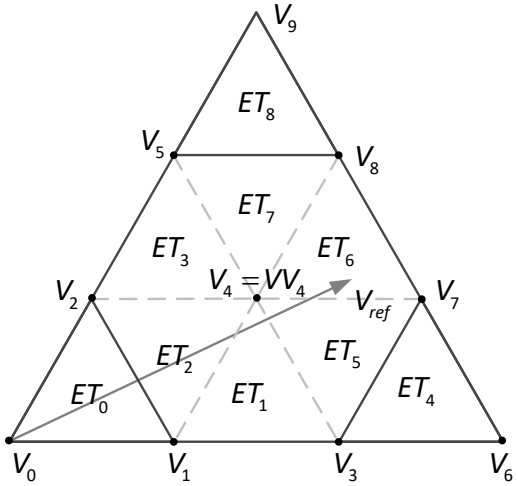


Figure 6-11 First sector of 4L RSS MPCI SVD divided into sub-triangle regions.

It can be observed that, with the introduction of the virtual vector VV_4, SVD of the 4L RSS MPCI will become similar to conventional 4L SVD. As a result, the sub-triangle regions ($ET_0 - ET_8$) are equilateral and symmetrical. Therefore, the modulation is equivalent to the conventional nearest three vector (NTV) modulation. Nevertheless, the actual vector selection is significantly different. Any of the 4 possible combinations can be selected as the virtual vector VV_4, however, only two combinations: $(V_{331} + V_{311})/2$ and $(V_{200} + V_{220})/2$ are selected for simplicity.

Let, V_{ref} is located in any of ET regions: $ET_1 - ET_3$ and $ET_5 - ET_7$ shown in Figure 6-11. The virtual vector ($VV_4 = \frac{V_3 + V_5}{2}$) is one of the NTVs in all these cases and therefore, the modulation actually using the non-nearest three vectors. Figure 6-12 show the vector selection when VV_4 is one of the nearest three vectors. The reference vector (V_{ref}) is synthesized using 4 voltage vectors

forming trapezoid $Tr_1 : V_3V_1V_2V_5$ and $Tr_2 : V_3V_7V_8V_5$ when it is located in ET_2 and ET_6 of SVD respectively. Therefore, this modulation actually uses either 3 or 4 vectors which form either RT or trapezoid respectively when one of the NTVs is a VV. So, the actual vectors used for voltage control are far away from V_{ref}, resulting in inferior ac side voltages and increased switching frequency. This results in increased switching losses due to the increased number of voltage steps. The VV-based modulation is further discussed with the help of simulations.

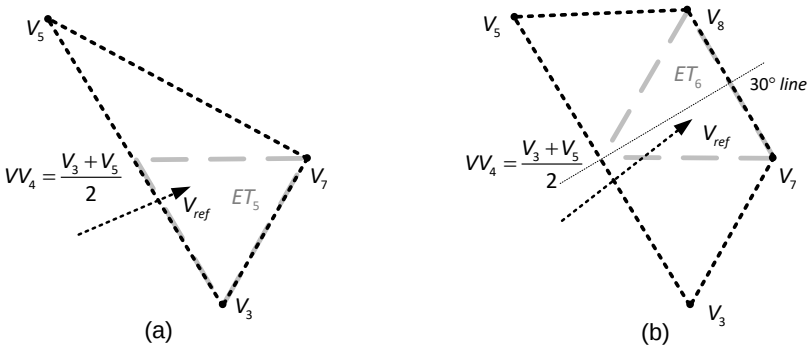


Figure 6-12 Voltage vectors used for synthesising V_{ref} when it is in (a) ET_5 and (b) ET_6.

6.6.2 STV-Based Modulation

A new modulation scheme is developed in order to (i) limit the number of switching states to 3 for any V_{ref} location and (ii) improve the performance for higher modulation indices using better vector selection. This is achieved by introducing non-equilateral triangle regions in SVD. Division of first sector into various triangle regions for 4L RSS-VSI is shown in Figure 6-13. The modulation uses isosceles triangle (IT) along with the ET and RT regions to approximate V_{ref}.

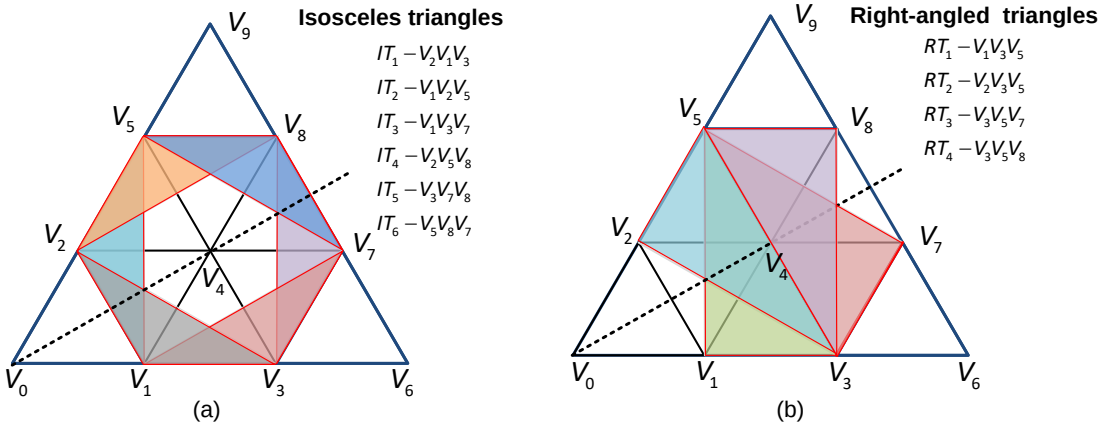


Figure 6-13 First sector of 4L RSS MPCI SVD divided into (a) Isosceles triangle regions, (b) right angle triangle regions (RT) and sub-regions for V_{ref} synthesis for proposed modulation.

There are 6 IT regions (Figure 6-13 (a)) and 4 RT regions (Figure 6-13 (b)) with associated voltage vectors. It is clear that the IT and RT regions have overlapped areas, therefore, three vectors are chosen based on V_{ref} location. A new approach detailed below is adopted for selecting 3 vectors from available vectors. If the V_{ref} is located in any of the IT regions: IT_1-IT_6 as shown in Figure 6-14 (a), the corresponding IT region (shown in Figure 6-13 (a)) is chosen for synthesis.

If V_{ref} is not bounded by any ET or IT region, RT regions are used depending on its location. Only RT_1 or RT_3 regions are used in the first half of the sector (first 30º in each sector) and RT_2 or RT_4 regions are used in the second half of the sector depending on the V_{ref} location.

Based on the above criteria, V_{ref} located in any of the region in4L SVD can be synthesized using only three vectors. The division of sub-regions for VV-based modulation is shown in Figure 6-14 (b) for comparison.

6.7 Modulation Algorithm for 4L RSS MPCI

A general approach that can be used to find the duty ratios of voltage vectors forming non-ET regions from duty ratios of ET regions is also discussed which enables us to use any conventional SVM techniques for finding voltage vectors and duty ratios. A simple algorithm is presented for generating voltage vectors and their duty ratios.

6.7.1 Voltage Vector Duty Ratio Expressions

From the previous section, it is clear that the triangles are not equilateral as in the case of conventional SVM. So, in order to find the on-time durations of the specific vectors, separate volt-second balance equations need to be considered for all IT and RT regions. This process will increase the memory requirement and also execution time for obtaining duty ratios. Moreover, it is very difficult to find the exact region as shown in Figure 6-14 (a). Meanwhile, there are several SVM algorithms for determining the duty ratios of various switching states with minimalistic mathematical operations [53],[152], [67]. However, due to the presence of IT and RT regions in SVM, it is not possible to take advantage of such efficient SVM algorithms.

Therefore, in order to effectively reduce the computational burden and to make use of these advanced NTV based modulation methods for MLI, in this section, duty ratios of non-NTV forming IT and RT regions are expressed in terms of NTV duty ratios. So that, if NTV duty ratios of an ET region containing V_{ref} are known, the duty ratios of the associated IT and RT regions are obtained with simple mathematical operations. Therefore, no separate volt-second balance equations or trigonometric relations are required to obtain the duty ratios of various regions (ET, IT and RT).

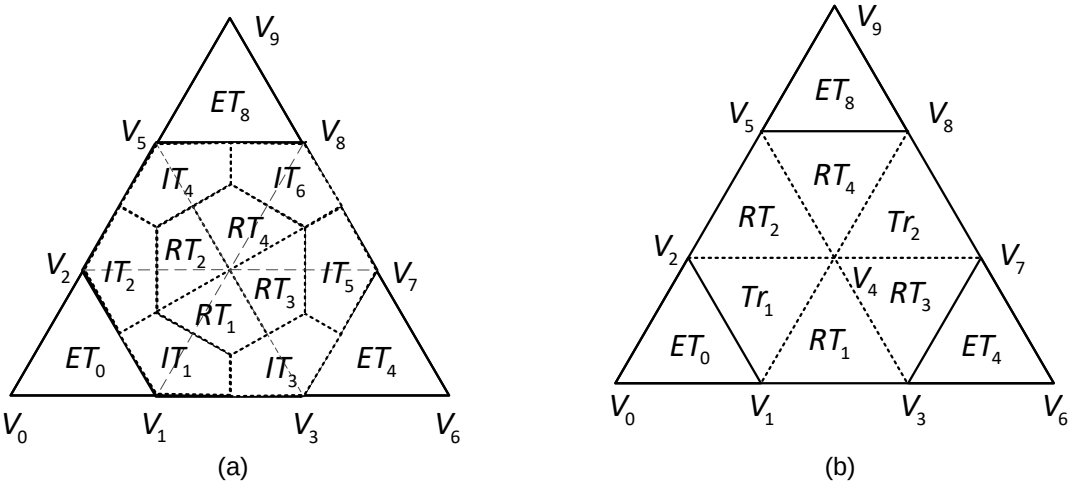


Figure 6-14 Regions for selection of sub-triangle regions for (a) STV-based modulation and (b) VV-based modulation.

Case-1:

In this case, the duty ratios of NTVs forming ET region are transformed to non-NTVs forming IT region. Figure 6-15(a) shows the reference vector V_{ref1} located in triangle ET_5. Let d_3^1, d_4^1 and d_7^1 are duty ratios of vectors V_3, V_4 and V_7 respectively obtained from NTV algorithm [53] to approximate V_{ref1}. However, due to unavailability of voltage vector V_4, V_{ref1} must be approximated by using IT_5 (Refer Figure 6-14 (a)). So, in order to find the duty ratios of voltage vectors of region IT$_5$, a unique relation is established as follows.

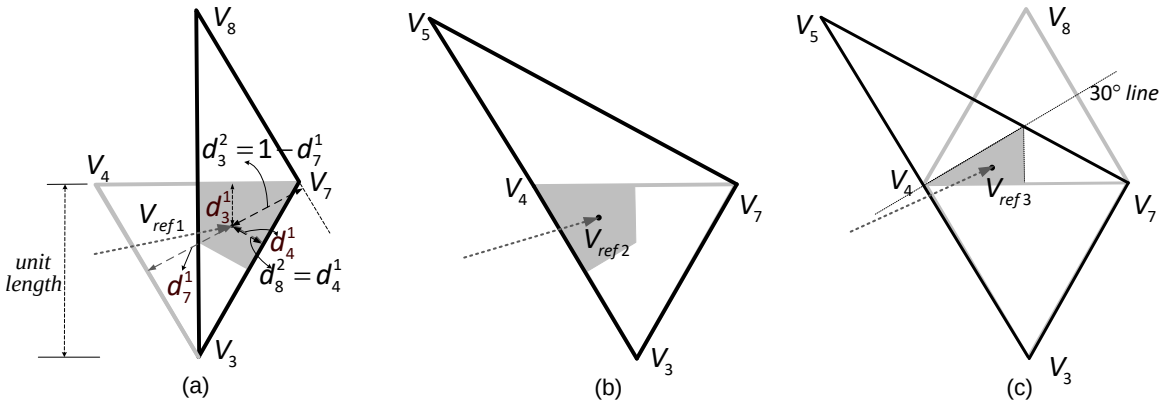


Figure 6-15 Duty ratio relations between ET and IT regions (Where, in d_p^q, subscript p denotes the vector number and super script q denotes the type of modulation: $q=1$ for NTV modulation and $q=2$ for proposed modulation.)

As given by [122], duty ratio of any given vector is equal to the ratio between distance from the endpoint of the reference vector to the line through the endpoints of the other two vectors and

the distance from given vector's endpoint to the line. Assuming, the height of ET to 1 (unity), the duty ratios for V_{ref1} voltage vectors of ET_5 region and IT_5 region are indicated in Figure 6-15 (a). Also note that, ∑d=1. The duty ratios of voltage vectors in terms of NTV duty ratios of triangle are given by

$$\begin{aligned} d_3^2 &= 1 - d_7^1 \\ d_8^2 &= d_4^1 \\ d_7^2 &= d_7^1 - d_4^1 \end{aligned} \tag{5.4}$$

It is important to note that the above-mentioned relations are valid for entire common area shared by ET and IT regions, however, only used for the shaded region shown in Figure 6-15 (a) where, IT_5 is to be used (Figure 6-14 (a)).

Case-II:

In this case, the duty ratios of NTVs forming ET region are transformed to non-NTVs forming RT region as shown in Figure 6-15 (b). The duty ratios can be derived as explained in case I. However, it can be obtained easily by mathematical analysis as follows.

The volt-second balance equation of the triangle to approximate V_{ref2} is given by

$$d_3^1 V_3 + d_4^1 V_4 + d_7^1 V_7 = V_{ref2} \tag{6.4}$$

Substituting $V_4 = (V_3 + V_5)/2$ in (6.4),

$$\left\{ d_3^1 + \frac{d_4^1}{2} \right\} V_3 + \left\{ \frac{d_4^1}{2} \right\} V_5 + d_7^1 V_7 = V_{ref2} \tag{6.5}$$

Therefore, finally the duty ratios of the vectors are given by

$$\begin{aligned} d_3^2 &= d_3^1 + \frac{d_4^1}{2} \\ d_5^2 &= \frac{d_4^1}{2} \\ d_7^2 &= d_7^1 \end{aligned} \tag{6.6}$$

Note that the above duty ratio expressions are valid for entire ET_5 region, however, they are used only for the shaded region shown in Figure 6-15 (b).

Case III:

In this case, the duty ratios of NTVs forming ET region are transformed to non-NTVs forming RT region as shown in Figure 6-15 (c). The reference vector V_{ref3} located in triangle ET_6 should

approximated by triangle RT_3. This case is realized as combination of Case I and Case II. Let us first convert the NTV duty ratios of the triangle ET_6 to the isosceles triangle formed by voltage vectors V_4 , V_5 and V_7. From Case I, the duty ratios are given by

$$\begin{aligned} d_5^2 &= d_8^1 \\ d_5^2 &= 1 - d_4^1 \\ d_4^2 &= d_4^1 - d_8^1 \end{aligned} \tag{6.7}$$

Therefore, the volt-second balancing equation is

$$\left\{d_4^1 - d_8^1\right\} V_4 + d_8^1 V_5 + \left\{1 - d_4^1\right\} V_5 = V_{ref3} \tag{6.8}$$

Now, as in Case II, substituting $V_4 = \left(V_3 + V_5\right)/2$ in (6.8) and simplifying,

$$\left\{\frac{d_4^1 - d_8^1}{2}\right\} V_3 + \left\{\frac{d_4^1 + d_8^1}{2}\right\} V_5 + \left\{1 - d_4^1\right\} V_7 = V_{ref3} \tag{6.9}$$

Therefore, finally the duty ratios of the vectors are given by

$$\begin{aligned} d_3^2 &= \frac{d_4^1 - d_8^1}{2} \\ d_5^2 &= \frac{d_4^1 + d_8^1}{2} \\ d_7^2 &= 1 - d_4^1 \end{aligned} \tag{6.10}$$

Similar to above cases, relations (6.10) are valid for entire common area bounded by the two regions, however, only used for the shaded region.

6.7.2 Implementation of Modulation Algorithm

In this section, an SVM algorithm for 4L RSS MPCI is developed that uses NTVs and their duty ratios obtained from a generalized SVM algorithm for MLIs [53]. Figure 6-16 shows the simplified algorithm for obtaining the three vector and their duty ratios. Coordinate transformation, sector identification and mapping of V_{ref} into first sector can be found in [153]. Let the NTVs and their duty ratios of the first sector referred V_{ref} are

$$\begin{aligned} V_x &= V_{ul}; V_y = V_{lu}; V_z = V_{ll} / V_{uu} \\ d_x^1 &= d_{ul}; d_y^1 = d_{lu}; d_z^1 = d_{ll} / d_{uu} \end{aligned} \tag{6.11}$$

Once, the NTVs and duty ratios of the ET region containing V_{ref} are known, first step is to check whether all the NTVs are switchable or not. For instance, if V_{ref} is in any one of the 6 ET regions

(ET_1-ET_3, ET_5-ET_7) shown in Figure 6-11, one of the NTVs (V_x, V_y, V_z) will be V_4 (not switchable) and therefore, should be synthesized using either IT or RT regions. In order to decide between IT and RT regions, the exact location of V_{ref} within the various sub-regions shown in Figure 6-14 (a) is needed. This can be done with the help of already known NTV duty ratios. A generalized relation between duty ratios and corresponding sub-region containing V_{ref} is given in Figure 6-17. Based on the maximum duty ratio among NTV duty ratios (d_x^1, d_y^1, d_z^1), the subregion can be easily identified. On the other hand, all the NTVs are switchable. if V_{ref} is located in ET_0, ET_4 and ET_8, and therefore IT and RT regions are not required.

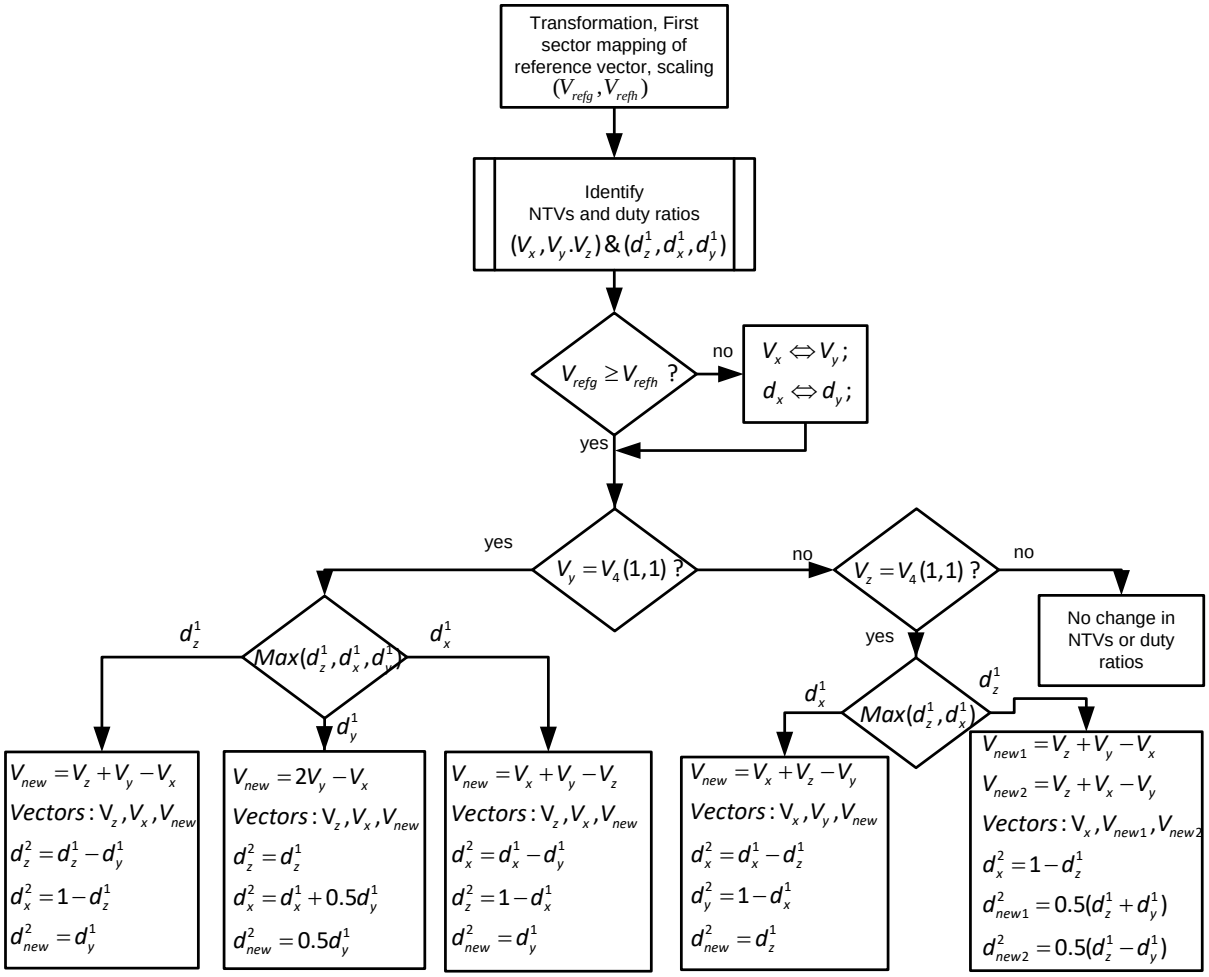


Figure 6-16 Proposed modulation algorithm for 4L RSS MPCI

As the first half of the sector $(V_{refg} \geq V_{refh})$ and second half of a sector $(V_{refg} < V_{refh})$ are mirror images, the swapping operation between V_x and V_y is performed. If $V_y = V_4$, V_{ref} is in any one of the ET regions: ET_1,ET_3, ET_5 and ET_7. Therefore, either case-I or case-II explained in the previous section can be used for obtaining the duty ratios. Similarly, if $V_z = V_4$, V_{ref} is in either

ET_2 or ET_6, therefore, case-III is used. In all the cases, the vector V_4 will be discorded and new vectors will be found online along with corresponding duty ratios.

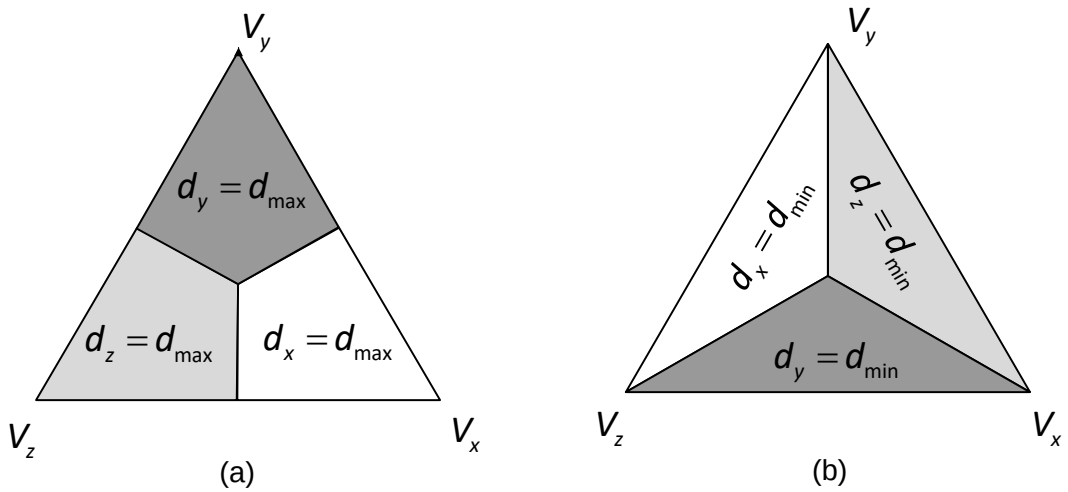
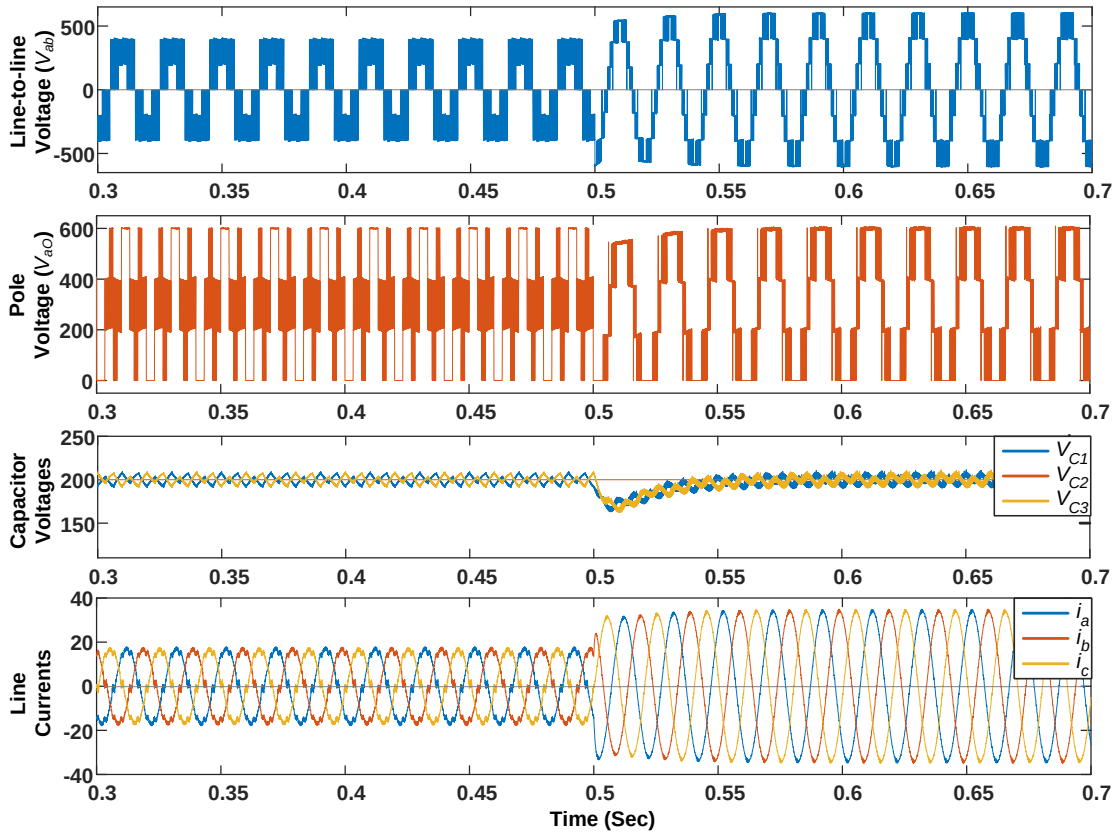


Figure 6-17 Relations of NTV sub-triangle regions with in the ET regions.

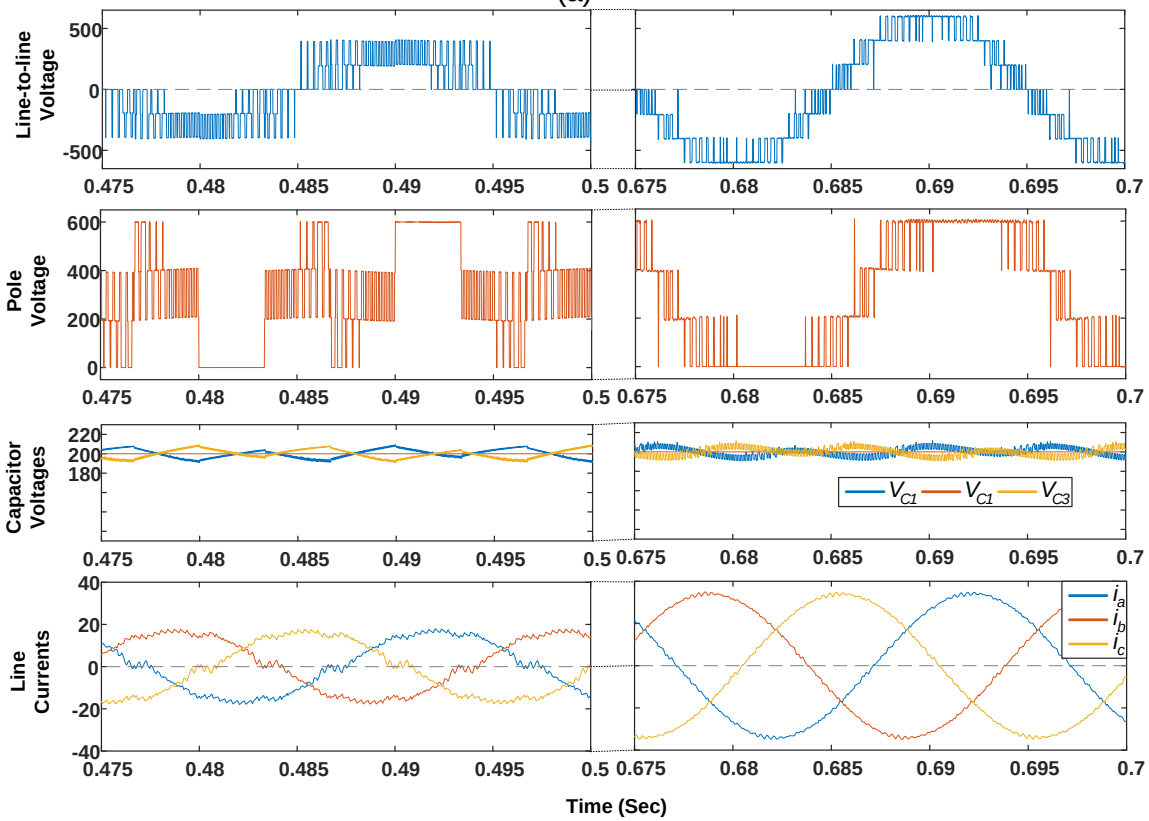
6.8 Performance Evaluation of 4L RSS MPCI

The performance of the 4L RSS MPCI is studied using MATLAB/Simulink for various operating conditions. The inverter is modulated using the STV as well as the VV-based modulation schemes. The modulation index (m) is defined as $m = \sqrt{3}\left(V_m / V_{DC}\right) \in [0,1]$ and $m = 1$ represents the boundary of the linear modulation. Here, V_m is the peak of the fundamental phase voltage. The parameters used for simulation are: DC link voltage=600 V, switching frequency=3 kHz, DC link capacitors =2200μF and RL load: R=10Ω/phase; L=5mH/phase. Two modulation indices m=0.75 and m=0.98 are used for simulation.

Figure 6-18 shows the simulation results of 4L RSS MPCI with the VV-based modulation scheme considering the virtual vector $VV_{321} = (V_{311} + V_{331})/2$. Since non-nearest three vectors are used, some of the phase voltage levels are skipped when V_{ref} is located in ET regions having one of the vectors as a virtual vector. Four switching states forming trapezoid, are used in ET_2 and ET_6 regions (i.e., Tr_1 for ET_2 and Tr_2 for ET_6) while, the switching states are used for V_{ref} located in other regions as shown in Figure 6-14(b). Figure 6-19 shows simulation results of 4L RSS MPCI with STV-based modulation scheme for same operating conditions. Same switching sequence is used in ET and RT regions for STV as that of VV-based shame, however the RT regions are used for reduced portion of SVD by introducing IT regions as shown in Figure 6-14(a).

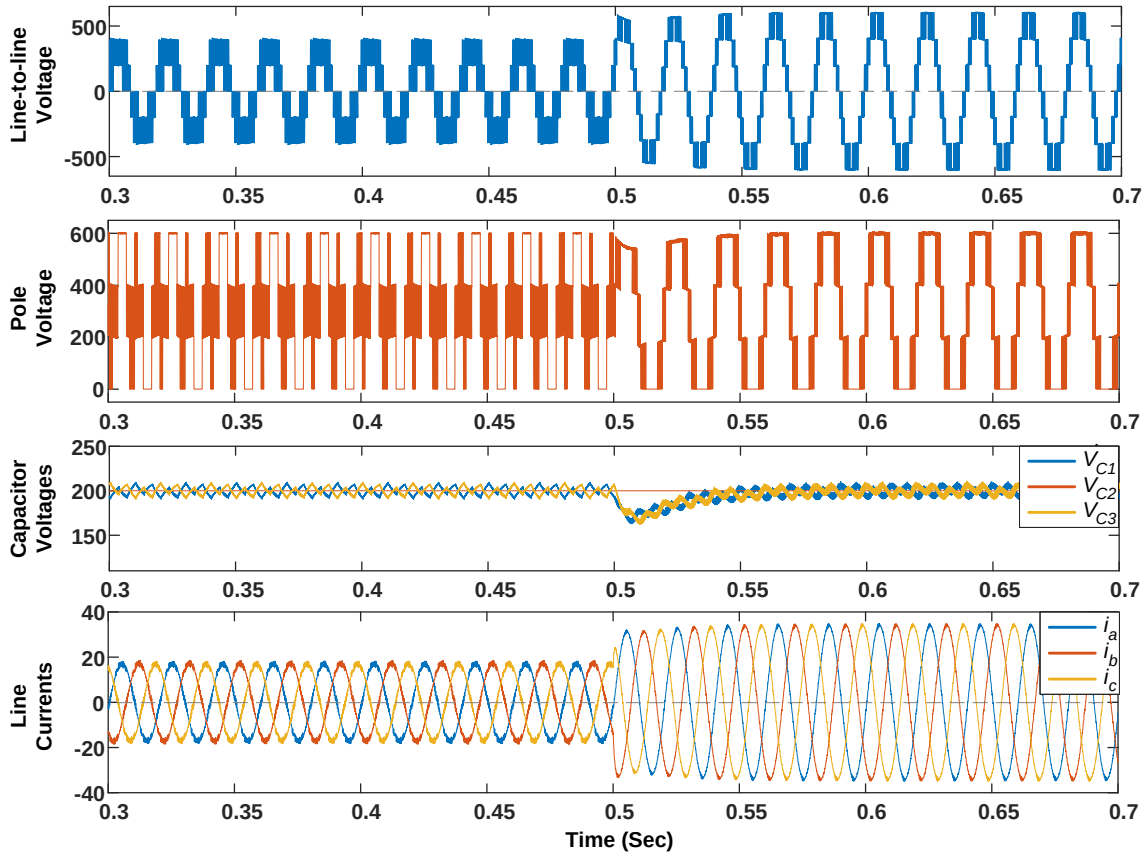


(a)

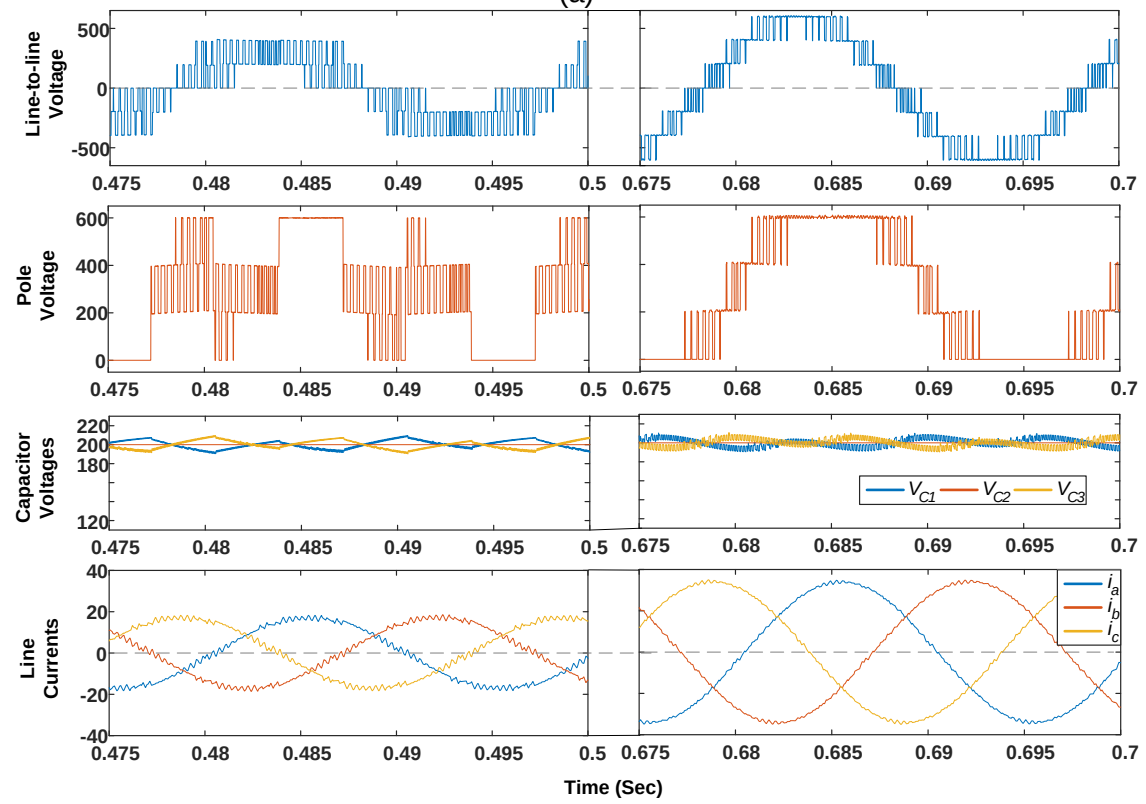


(b)

Figure 6-18 Simulation results of 4L RSS MPCI with VV-based modulation for (a) m=0.75 (0.3 to 0.5 sec) and m=1(0.5 to 0.7 sec) and (b) Zoomed view of (a).



(a)



(b)

Figure 6-19 Simulation results of 4L RSS MPCI with STV-based modulation for (a) m=0.75 (0.3 to 0.5 sec) and m=1(0.5 to 0.7 sec) and (b) Zoomed view of (a).

6.8.1 Comparison of Modulation Schemes

From Figure 6-18 (b) and Figure 6-19 (b), it is observed that, the voltage and current waveforms are different for both the modulation schemes. Due to the use of 4 switching states, VV-based modulation increases in switching frequency when V_{ref} is located in ET_2 and ET_6. For medium modulation indices like m=0.75, this effect is more significant due to increase duration of V_{ref} in the corresponding triangle regions. This also increases the current distortion as observed in current waveform of Figure 6-18 (b). On the other hand, the switching frequency reduced in with the STV modulation due to the use of only three voltage vectors. The voltage and current waveforms are also improved with discrete voltage level jumps using STV-based modulation.

For the range of modulation indices $0 \le m < 0.34$ and $0.89 \le m < 1$, the performance of 4L RSS MPCI is similar to conventional 4L MPCI topologies. This is due to the availability of all the switching states in the SVD as shown in Figure 6-10. In these range of modulation indices, V_{ref} will be synthesized using only $ET_4(V_3V_6V_7)$, $ET_4(V_3V_6V_7)$, $IT_1(V_3V_7V_8)$, $IT_2(V_5V_7V_8)$ and $ET_8(V_5V_8V_9)$ and no RT or trapezoidal regions are used in STV-based modulation scheme. Noticeably, there is no significant difference between line to-line voltages of two modulation schemes for modulation indices near to m=1, however, for all modulation indices, the number of phase voltage jumps are quite high in case of VV-based modulation scheme as compared to the proposed modulation scheme.

6.9 5L RSS MPCI with Common H-Bridge Cells

As the number of voltage levels increase, there is an increased degree of freedom for developing RSS MPCI topologies. In this section two types of RSS topologies are derived from Type-1 and Type-2 MPCIs presented in Section 6.3.

6.9.1 Type-1 5L RSS MPCI

Figure 6-20 shows the 5L RSS MPCI formed by making the top and bottom half bridge cells of Type-1 5L MPCI topology (refer Figure 6-6) common for all the phases. So that, the outer levels (4, 3) and (1, 0) are generated by the H-bridge cells $\left(T_p, \overline{T}_p\right)$ and $\left(T_n, \overline{T}_n\right)$ respectively. The topology consists of only 16 active switches as compared to the conventional 5L topologies with 24 devices. Therefore, saving of 8 switches and associated driver circuits will be obtained, resulting a simple hardware circuitry and significant saving in cost. However, two important consequences of such connection are

1) Positive voltage levels (4, 3) or negative voltage levels (1, 0) cannot be generated simultaneously for any of the 3 phases. The voltage level 4/3 in any phase will not permit

voltage level 3/4 in the remaining phases. Similarly, voltage level 1/0 in any phase will not permit 0/1 on the remaining phases.

2) Switches ($T_p, \bar{T}_p$) and ($T_n, \bar{T}_n$) in the common H-bridge cell are used by the other phases when they are not part of output voltage generation in a phase. Therefore, degree of freedom for reducing voltage stresses by selecting PWM-2 will be lost and therefore, increased voltage stresses on the devices are expected since the modulation scheme of the RSS VSI should be combination of PWM-1 and PWM-2.

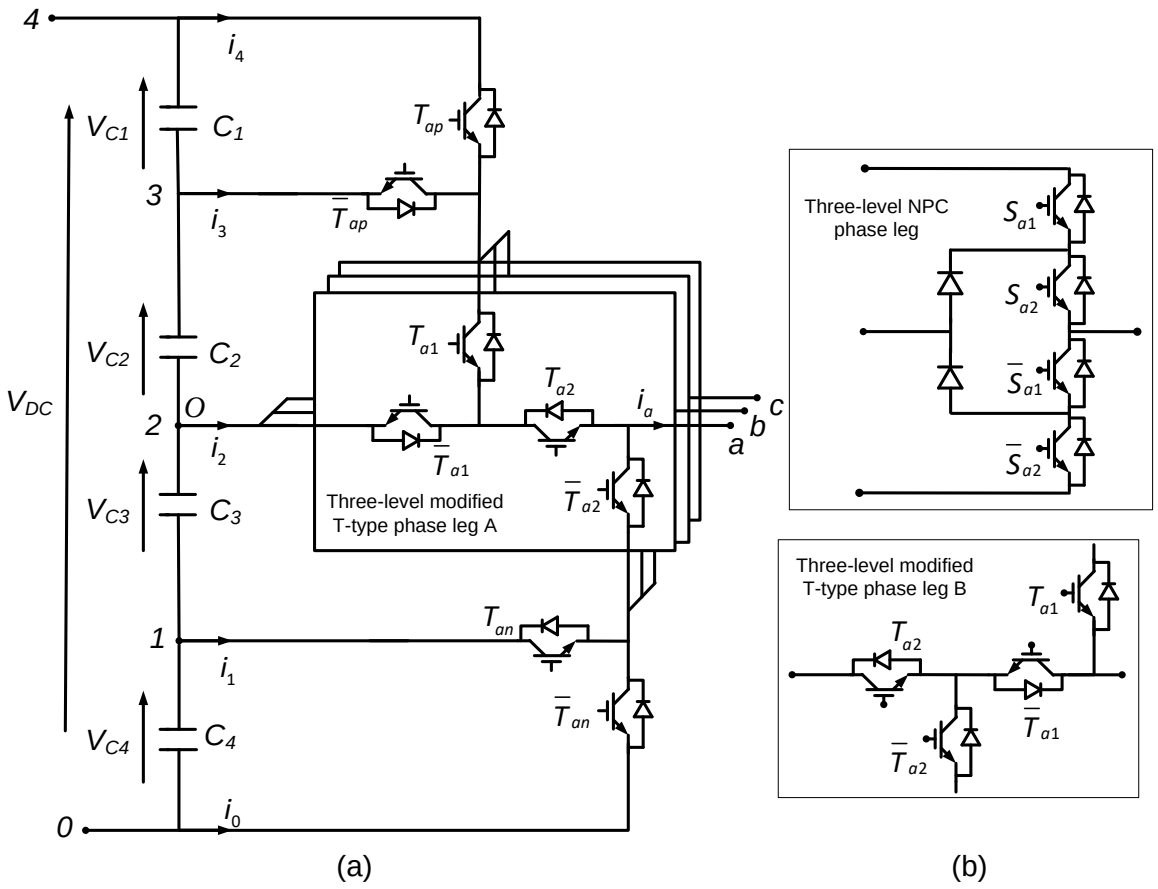
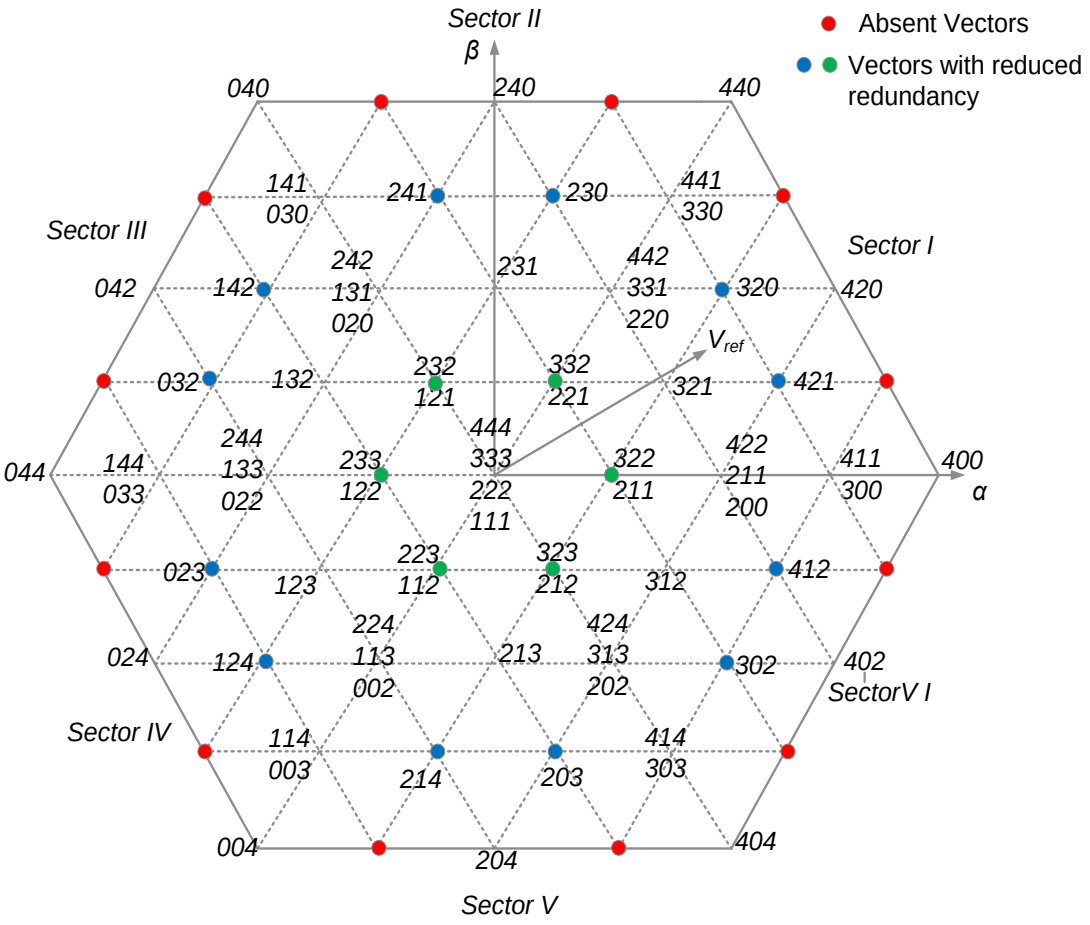
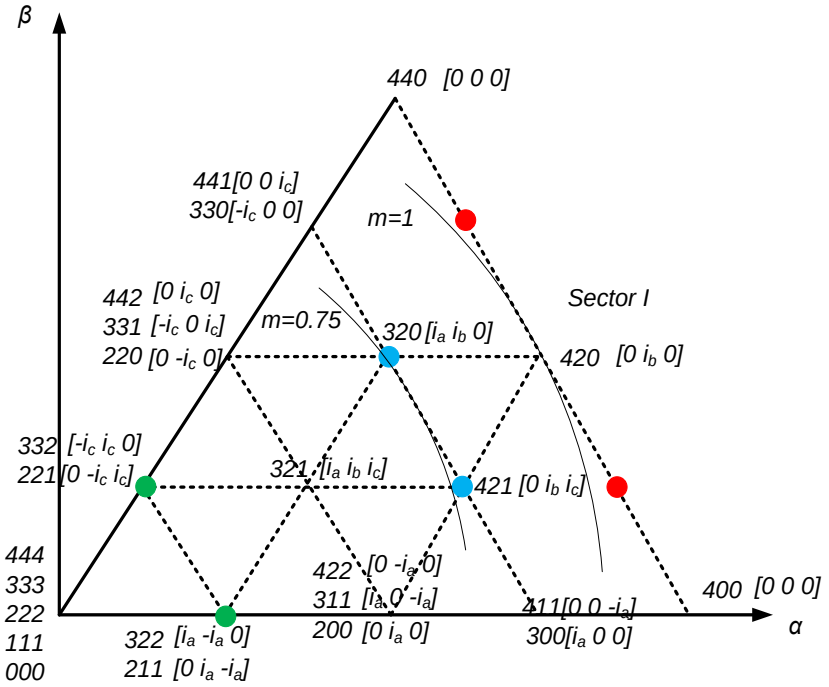


Figure 6-20 Type-1 5L RSS MPCI formed by half bridge modules, (b) Other alternatives for modified T-Type leg.

From the above discussion, it is clear that some of the three phase switching states need to be eliminated in order to avoid short circuit of common H-Bridge. The SVD of Type-1 5L RSS MPCI topology is shown in Figure 6-21.



(a)



(b)

Figure 6-21 SVD of Type-1 5L RSS MPCI formed by half bridge modules: (a) Complete SVD and (b) Sector-1 of SVD.

From Figure 6-21, it is clear, the switching states of 5L RSS MPCI coincides with switching states of the conventional 5L VSI SVD, however, some switching states are absent. As result, the voltage vectors are divided into three categories: 1) vectors with full redundancy; 2) vectors with reduced redundancy and 3) absent vectors. In Figure 6-21 (a), these vectors are marked such that: the vectors in red are completely absent and vectors in blue and green exhibit reduced redundancy. Figure 6-21 (b) shows the sector-1 of the SVD each switching state is associated with set of node currents flowing through the internal node points due to the corresponding switching state. For example, the switching state '311' results in nodes currents $[i_3\, i_2\, i_1]=[i_a\, 0-i_a]$ as shown in Figure 6-22. As a result, the DC link capacitor voltages will be deviated if the DC link is energized with high voltage DC source between the top and bottom DC rails. However, for the distribution generation applications, this problem can be solved by connecting low voltage DC sources across each DC-link capacitor.

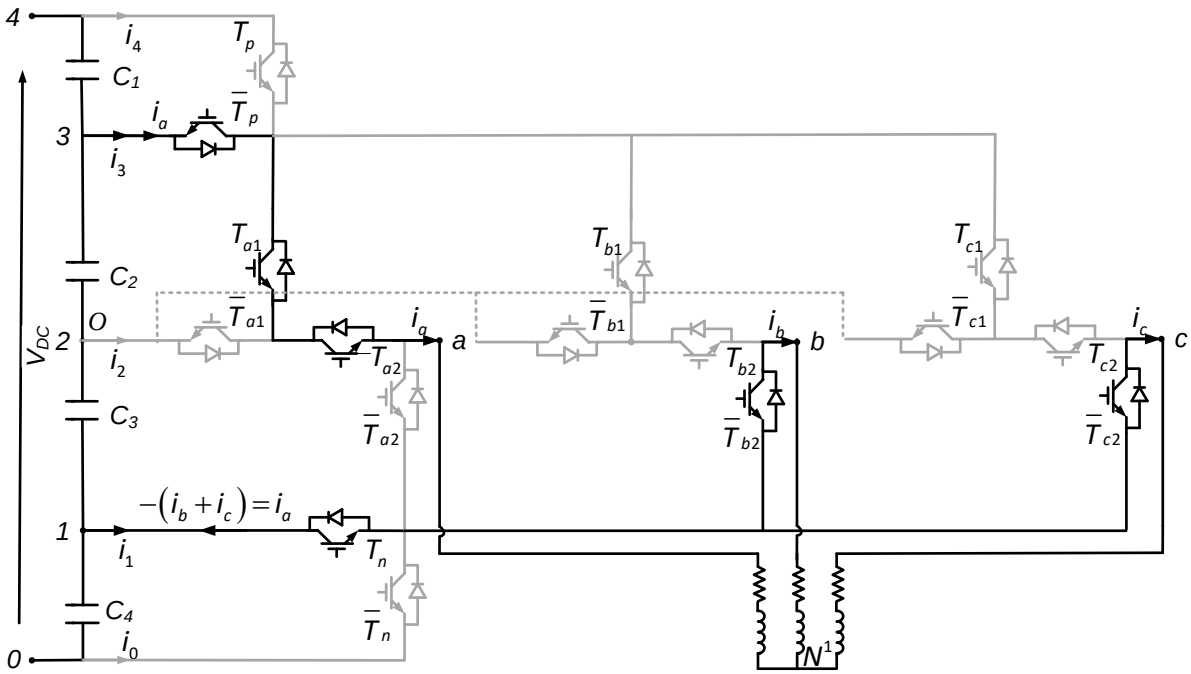


Figure 6-22 Type-1 5L RSS MPCI for switching state '311'.

6.9.2 Type-2 5L RSS MPCI

Figure 6-20 shows another variant of the 5L RSS MPCI derived from the generalized topology discussed in Section 6.3 case-2 by making the inner half bridge modules common for all the phases. The topology is named 5L RSS MPCI (Type-2). Similar to Type-1, topology also consists of only 16 self-commutated devices. However, the SVD of the Type-2 is different from the SVD of Type-1. Figure 6-24 shows the SVD of 5L RSS MPCI (Type-2). Clearly, the absent vectors and the vectors with reduced redundancy are different compared to its counterpart Type-1 topology.

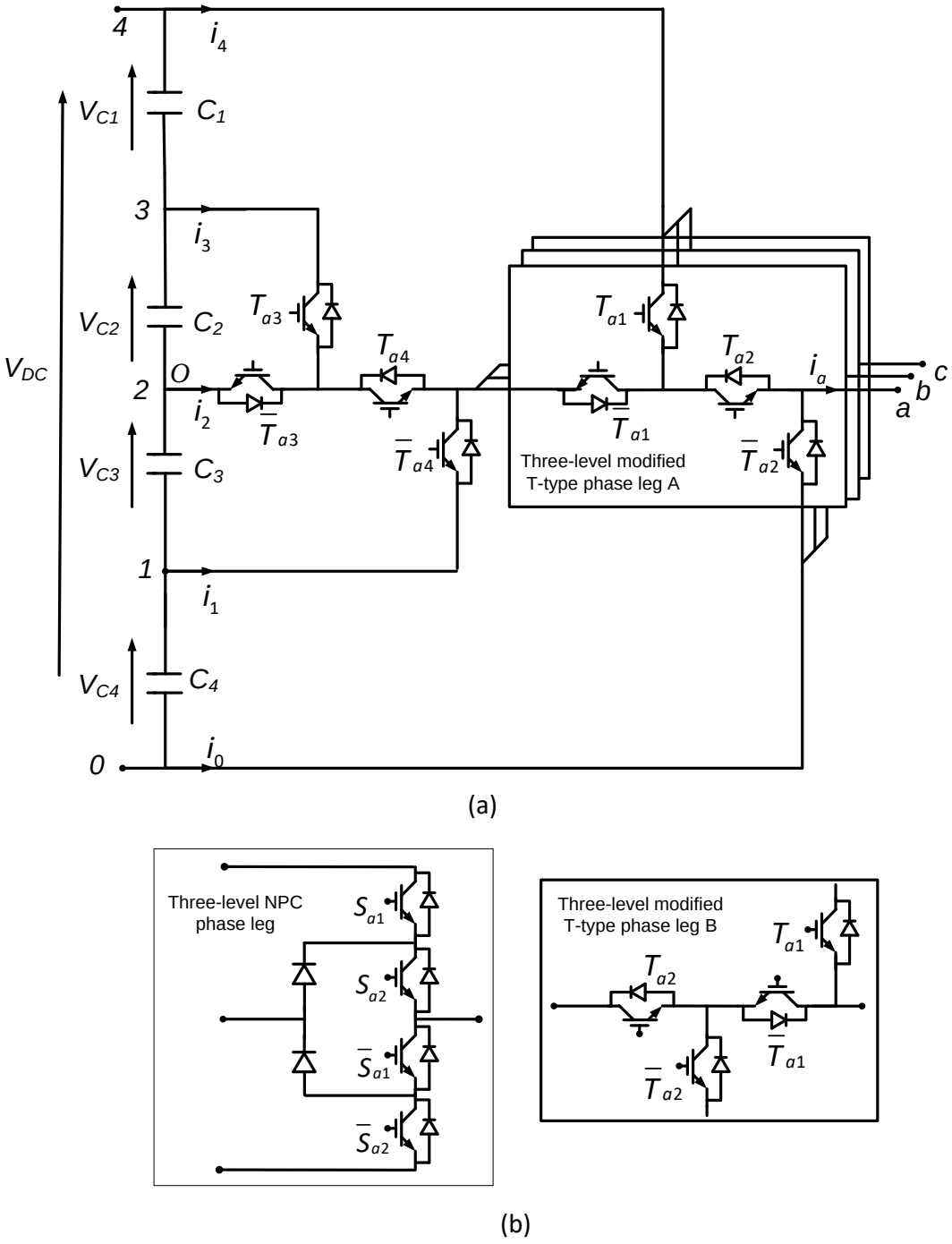
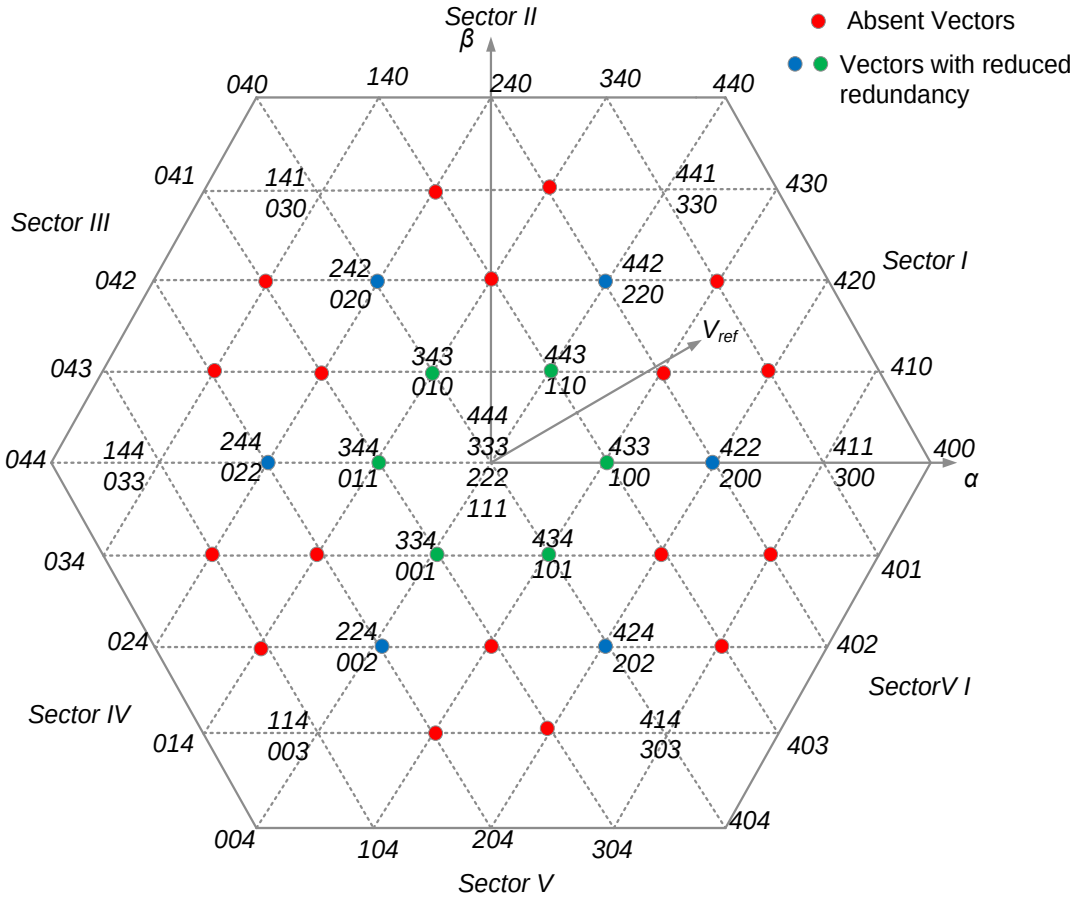
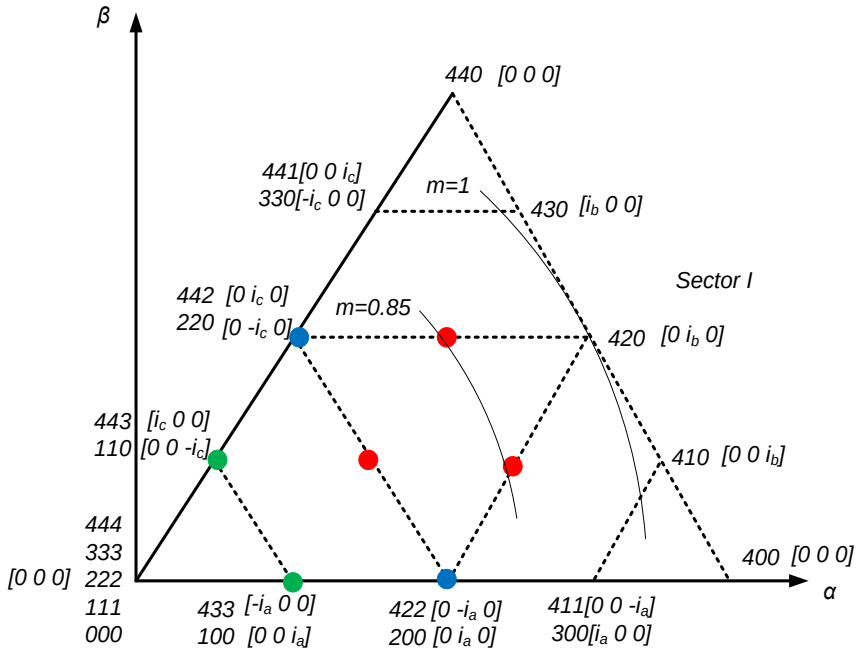


Figure 6-23 A 5L RSS MPCI (Type-2) formed by half bridge modules, (b) Other alternatives for modified T-Type leg.

Comparing the two 5L SVDs, for Type -2 RSS MPCI, the absent vectors are concentrated at center of each sector region, while the absent vectors are distributed for the Type-1 RSS MPCI. For synthesizing V_{ref} , at different modulation indices the voltage vectors nearer to the tip of the V_{ref} are chosen. Therefore, it can be understood that, the Type-2 RSS MPCI need to choose the far away voltage vectors synthesize V_{ref} for medium m values. While, the Type-1 RSS MPCI need to chose far away voltage vectors synthesize V_{ref} for higher m values.



(a)



(b)

Figure 6-24 SVD of 5L RSS MPCI formed by half bridge modules: (a) Complete SVD and (b) Sector-1 of SVD.

6.9.3 Modulation Strategy For 5L RSS MPCI Topologies

Virtual vectors are used in the place of absent vectors in order to complete SVD. It is to be noted that, more than one combination of actual vectors is available for the virtual vectors. The vector relations are used for all the virtual vectors present in Sector 1 of Type-1 5L RSS MPCI are given below:

$$VV_{410} = \frac{V_{400} + V_{420}}{2}; VV_{430} = \frac{V_{420} + V_{440}}{2}; \tag{5.5}$$

Only vector positions which are completely absent are replace with the virtual vectors while the vectors positions with reduced redundancy are directly used. Similarly, the vectors relations used for the virtual vectors present in sector-1 of Type-2 5L RSS MPCI are given by

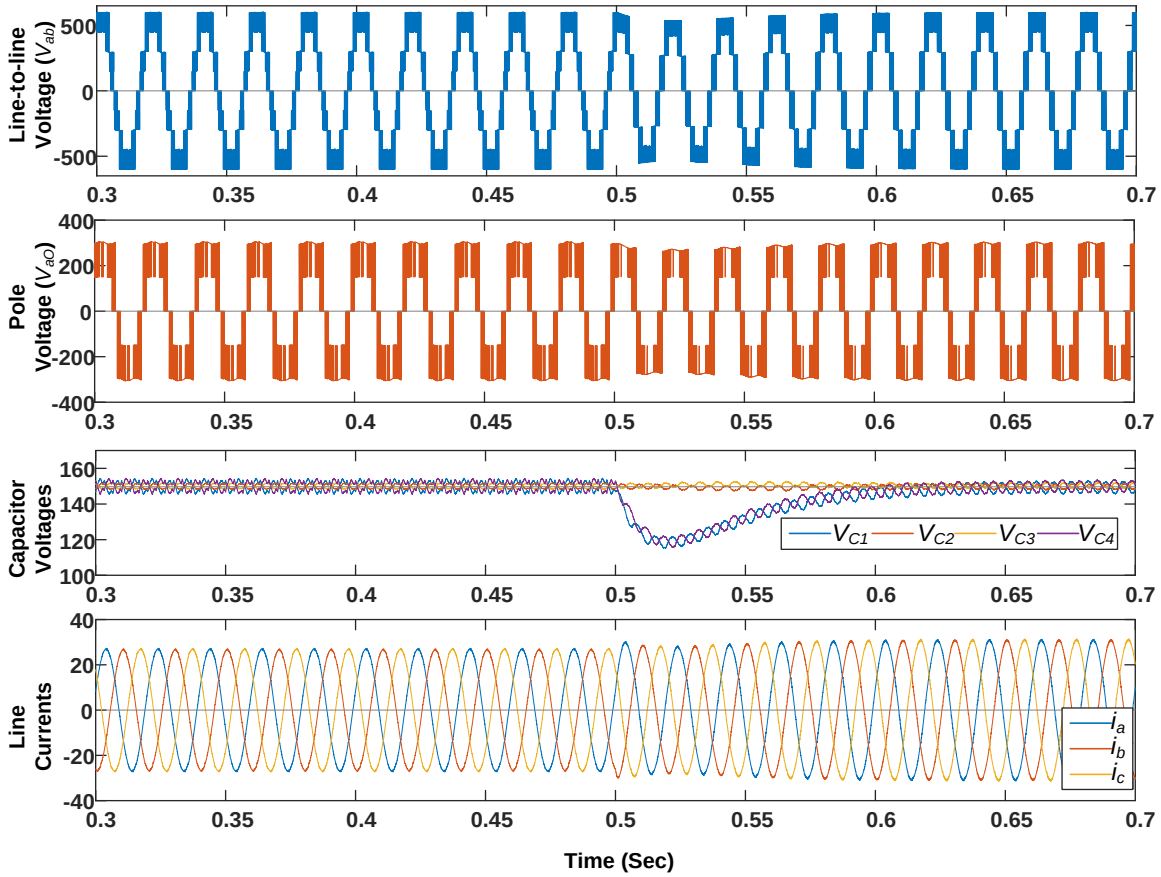
$$\begin{aligned} VV_{432} &= \frac{V_{422} + V_{442}}{2}; VV_{210} = \frac{V_{220} + V_{200}}{2}; \\ VV_{421} &= \frac{V_{420} + V_{422}}{2}; VV_{210} = \frac{V_{220} + V_{420}}{2}; \end{aligned} \tag{5.6}$$

Now the output voltage vector of the VSI is synthesized by using NTV modulation scheme in which, the vectors are either actual vectors or VVs. The SVM algorithm based on 2L SVD discussed in section 6.4, is used to find the duty ratios and gating signals of the 5L RSS MPCI.

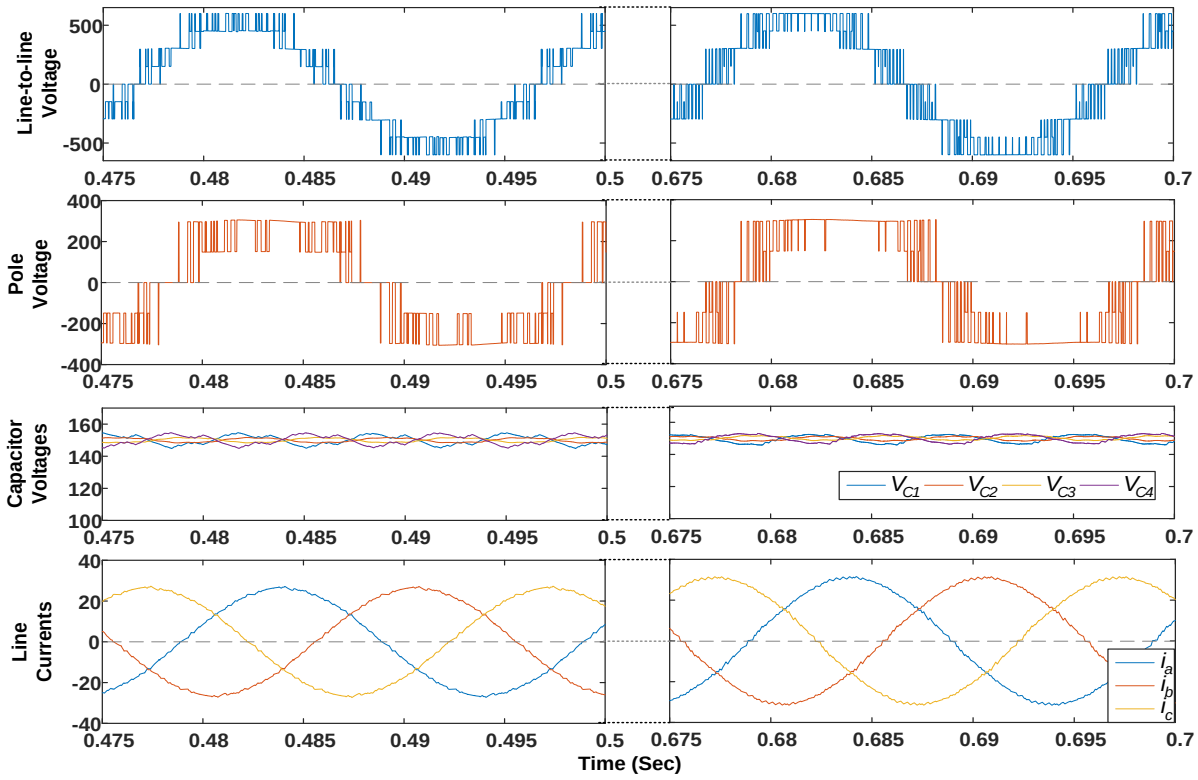
6.10 Performance Evaluation of 5L RSS MPCI Topologies

The performance of the 5L RSS MPCI topologies are evaluated using in MATLAB/Simulink. The parameters used for simulation are: DC link voltage=600 V, switching frequency=3 kHz, DC link capacitors =2200μF and RL load: R=10Ω/phase; L=5mH/phase. Here, the main idea is to compare the different voltage vector selection criteria at medium and high range of modulation indices in order to compensate the absent vectors depending on the 5L RSS MPCI topology used. An external capacitor voltage balancing circuit is used to balance the DC capacitor voltages at the input side of the 5L RSS MPCI topologies. The voltage vectors are chosen to minimize the number of commutations in each switching cycle.

Figure 6-25 show the voltage and current waveforms of Type-1 5L RSS MPCI at two modulation indices m=0.86 and m=1.0. Nine and five voltage levels are obtained in line-to-line and pole voltage waveforms respectively. It is observed that the voltage levels are not discreet due to the absence of switching states near the higher modulation index region as shown in Figure 6-21. This also affects THD of the ac side waveforms. The harmonic spectrum of line-to-line voltages and line currents is shown in Figure 6-26.



(a)



(b)

Figure 6-25 Voltage and current waveforms of Type-1 5L RSS MPCI for change in modulation index: (a) m=0.86 up to t=0.5sec and m=1 from t=0.5 sec onwards and (b) Zoomed view of (a)

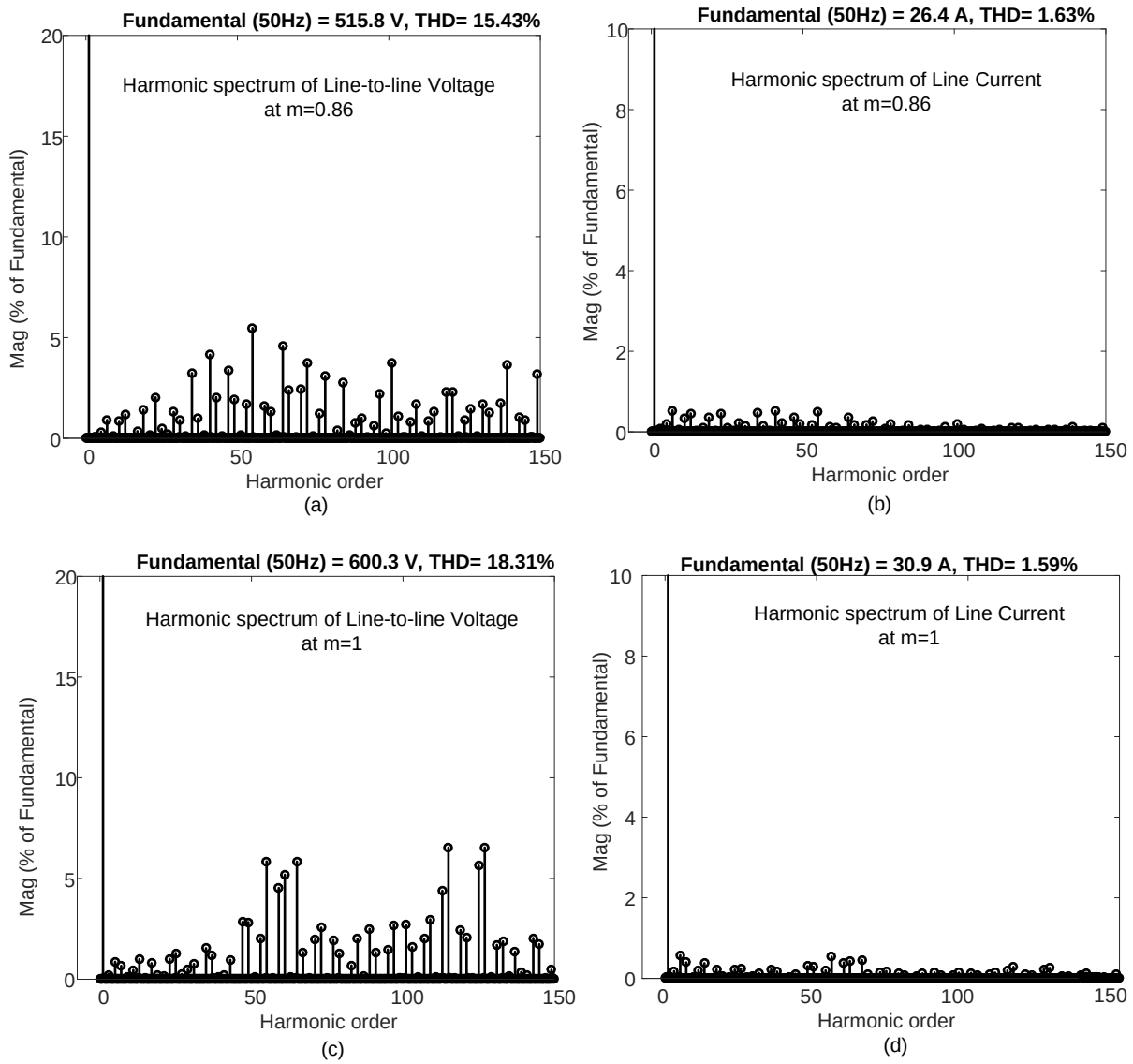
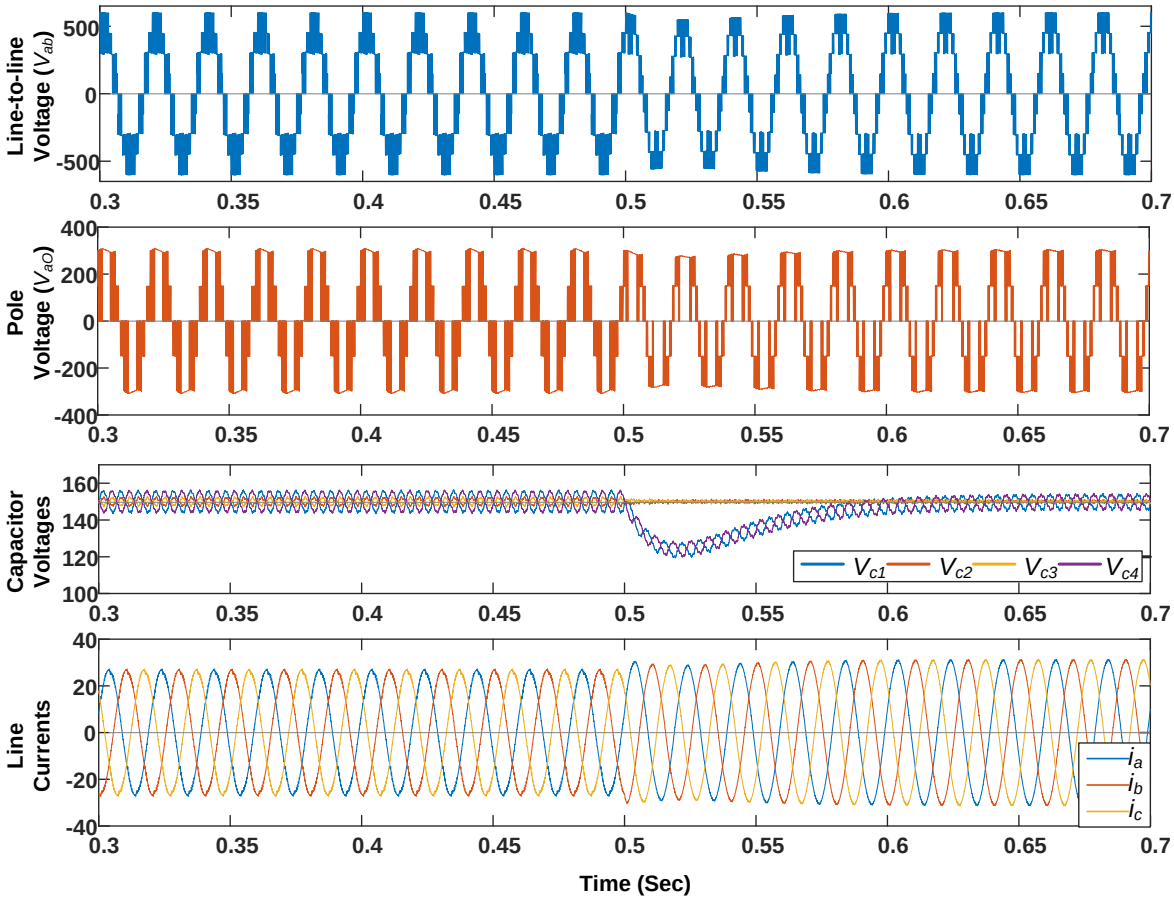
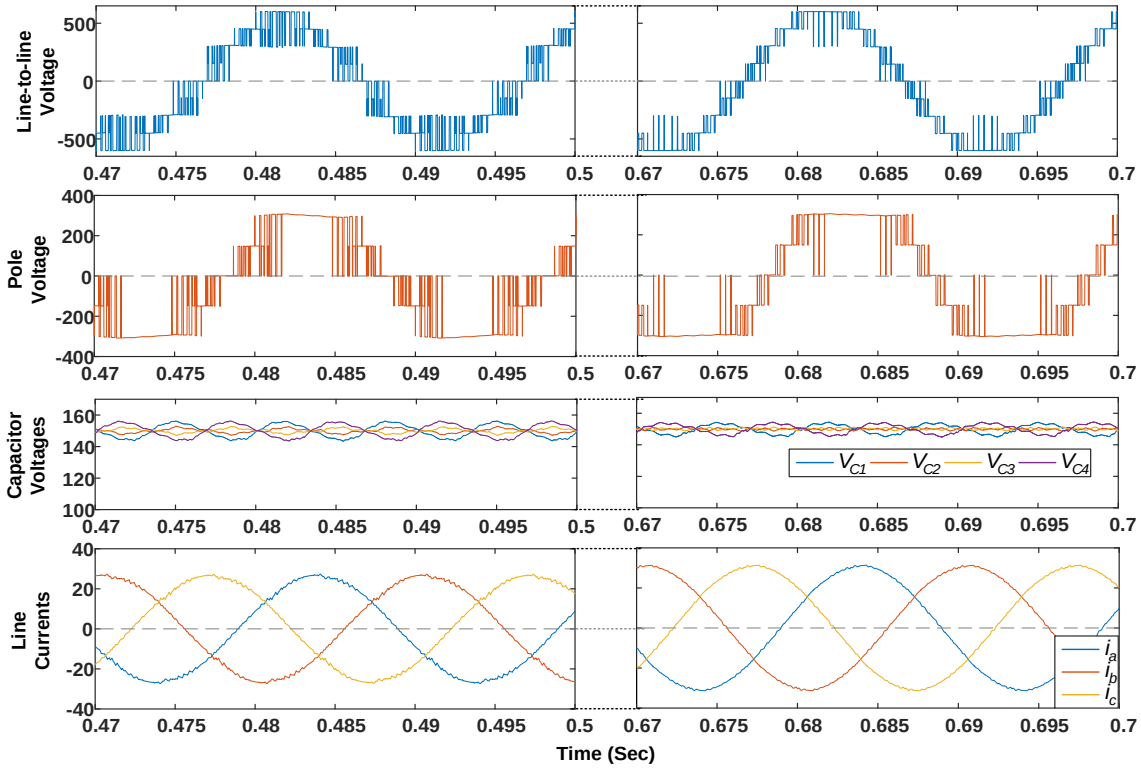


Figure 6-26 Harmonic spectrum of Type-1 5L RSS MPCI: (a) Line-to-line voltage at m=0.86 (b) Line current at m=0.86, (c) Line-to-line voltage at m=1 and (d) Line current at m=1;

Figure 6-27 show the voltage and current waveforms of Type-2 5L RSS MPCI at two modulation indices m=0.86 and m=1.0. Nine and five voltage levels are obtained in line-to-line and pole voltage waveforms respectively. At m=0.86, It is observed that the voltage levels are not discrete due to the absence of switching states near the medium modulation index region as shown in Figure 6-24. At m=1, voltage levels of the line-to-line voltage are relatively more discrete. This is due to the presence of all the switching states in outer most layer in SVD. Figure 6-28 shows the harmonic spectra of line-to-line voltage and line current for two modulation indices m=0.86 and m=1.



(a)



(b)

Figure 6-27 Voltage and current waveforms of Type-2 5L RSS MPCI for change in modulation index: (a) m=0.86 up to t=0.5sec and m=1 from t=0.5 sec onwards and (b) Zoomed view of (a)

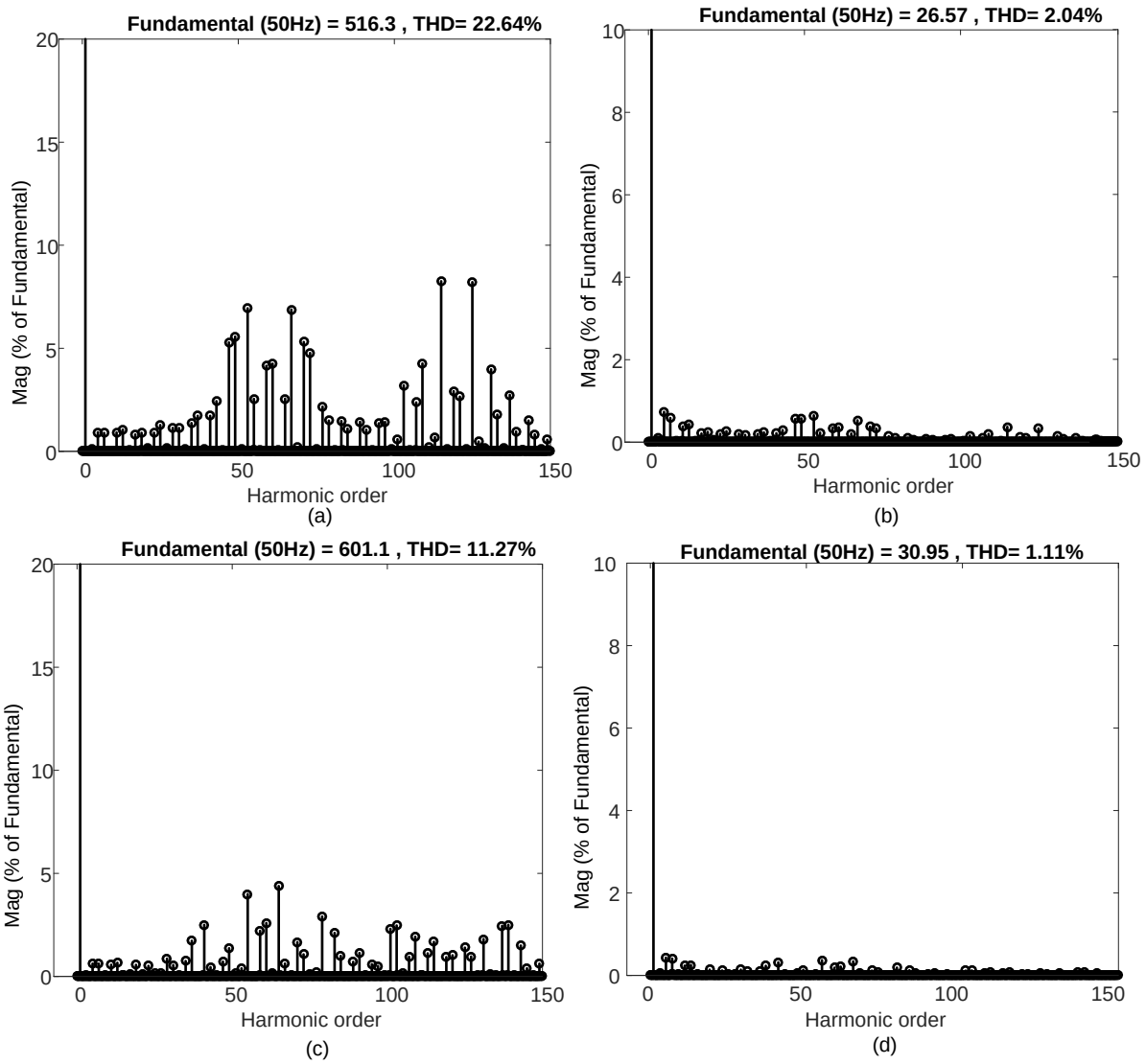


Figure 6-28 Harmonic spectrum of Type-2 5L RSS MPCI: (a) Line-to-line voltage at m=0.86 (b) Line current at m=0.86, (c) Line-to-line voltage at m=1 and (d) Line current at m=1;

6.10.1 Comparative Analysis 5L RSS MPCI topologies

Since the available switching states are dissimilar for Type-1 and Type-2 RSS topologies, the performance for different modulation indices are also different. Table 6-8 lists % THDs obtained for Type-1 and Type-2 5L RSS MPCI for two modulation indices m=0.86 and m=1. It is observed that the performance of Type-2 is superior at modulation indices near to m=1, while the performance of Type-1 is superior for the medium modulation indices. If the modulation indices is reduced further, Type-1 RSS MPCI is expected to perform much better compared to Type-2 RSS MPCI, since all the voltage vectors are available this region of SVD as shown in Figure 6-21.

Table 6-8 Comparision of % THDs for Type-1 and Type-2 5L RSS MPCI

% THD	m=0.86		m=1	
	Type-1	Type-2	Type-1	Type-2
Line-to-line Voltage	15.43 %	22.64 %	18.39 %	11.27 %
Line current	1.63 %	2.04	1.59 %	1.11 %

6.10.2 Switch Rating in RSS MPCI Topolgoies

The proposed RSS MPCI topologies can effectively reduce the number of active switches and clamping diodes compared to the other MPCI counterparts. However, it is observed that the reduction in switch count affects the blocking voltage requirement. Table 6-9 shows the comparison of 5L MPCI topologies. Type-1 and Type-2 5L RSS MPCI topologies only require 16 switches compared to 24 switches in modified T-Type and DCI topologies. Total blacking voltage (TBV) across the active switches is minimum in case of DCI but it requires the clamping diodes with TBV of 36. The Type-2 RSS MPCI requires maximum TBV of 44 across the active switches. Type-1 RSS MPCI requires minimum switches as well as TBC.

Table 6-9 Comparision of 5L MPCI topolgies

Parameters count		Topologies				
		DCI[47]	Modified T-Type MPCI (Type-1)	Modified T-Type MPCI (Type-2)	Type-1 5L RSS MPCI	Type-2 5L RSS MPCI
IGBTs		24	24	24	16	16
Clamping Diodes		36	0	0	0	0
Bidirectional Switches		0	0	0	0	0
Total blocking voltage (TBV) (p.u)	IGBTs	24	36	42	34	44
	Diodes	36	0	0	0	0

6.11 Conclusion

In this chapter, a modified T-type topology is derived from 3L T-Type NPCI leg and it is extended to higher voltage levels in two approaches namely Type-1 and Type-2 based on the location of addition of H-Bridge cells. The modified T-Type MPCI topologies (both Type-1 and Type-2) demand minimum TBC and do not require any clamping diodes and bidirectional switches compared to conventional MPCIs. In order to further reduce active switch count, Type-1 and

Type-2 RSS MPCI topologies are proposed based on common clamping approach and are discussed in detail with the help of 4L and 5L RSS MPCI topologies. The RSS MPCI topologies demand minimum number of active switches and eliminate the requirement of clamping diodes and bidirectional switches and therefore results in simplified and scalable structures. Type-1 RSS MPCI topologies require minimum TBV, however, the performance is slightly deteriorated at higher modulation index. Type-2 RSS MPCI topologies demand more TBV but provides better performance in high modulation index region. Two modulations namely VV-based and STV-based Modulation strategies derived from the non-NTV modulations of 3L NPCI are implemented on the 4L RSS MPCI topologies and obtained simulation results are provided.

Chapter 7: SYSTEM DEVELOPMENT AND EXPERIMENTATION

[This chapter presents the design of system hardware and experimentation for prototype models of different MPCI topologies to validate the simulation results presented in the previous chapters. RT-lab real time digital simulator with Meta controller software interface and Spartan-3 board is used for hardware interface. The proposed modulation algorithms are implemented in the MATLAB/Simulink and are compiled using the Meta controller interface to generate the switching signals of the different MPCI topologies.]

7.1 Introduction

To substantiate the viability and effectiveness of various MPCI topologies and modulation algorithms, the following prototypes are developed in the laboratory.

- Three-level (3L) NPCI.
- Hybrid 2/3L NPCI.
- Four-level (4L) RSS MPCI.
- Five-level (5L) RSS MPCI (Type-1 and Type-2)

Three-phase downscaled multilevel power conversion systems rated at 100 V, 1 kVA are designed and developed to realise the above-mentioned MPCI topologies. For all the topologies mentioned above the power circuits consists IGBTs (IRG4PH40KD) as the switching devices. The power circuit of VSI consists of rectifier system, intermediate DC circuit system. The DC-link voltages are obtained through uncontrolled diode bridge (KBPC3510) and to make it ripple free suitable ratings of DC link capacitors are chosen. The other hardware components as required for the operation of the experimental set-up such as pulse amplification circuit, dead-band circuit, isolation circuit, voltage and current sensor circuits are designed and developed in the laboratory. The complete schematic diagram for the realisation of HPFC is shown in Figure 7-1.

The control algorithm to generate gate pulses for IGBTs is developed in MATLAB/Simulink environment. The RT-Lab is used as a real time HIL (Hardware in loop) controller to implement control algorithm in real time. The RT-Lab compiler converts the MATLAB/Simulink program into a code compatible to Spartan-3 FPGA (field programmable gate array) board The FPGA board generates the control signals which are taken out from digital output port of the RT-Lab. The feedback signals required to generate gate pulses are taken into RT-Lab by using analog input port.

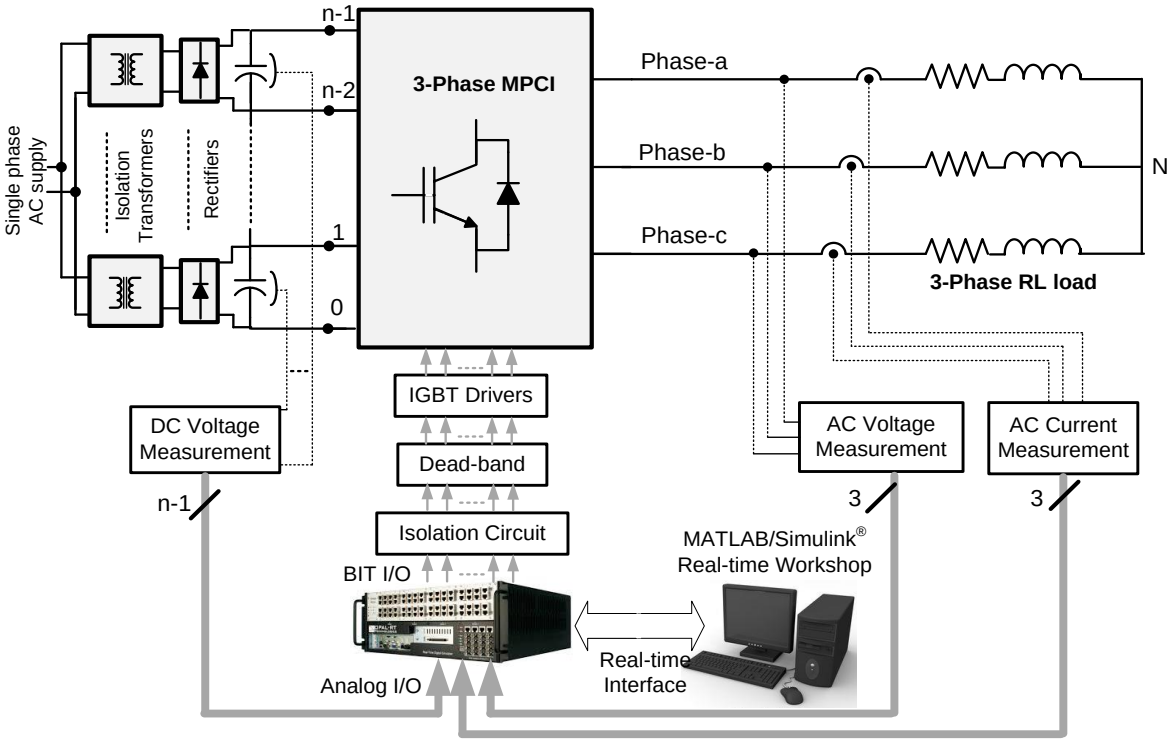


Figure 7-1 Schematic diagram for hardware implementation of MPCI topologies.

The development of different hardware components as required for the operation of the hardware prototypes are discussed in the upcoming sections.

7.1.1 System Hardware

The developed experimental prototype is comprised of the following basic parts:

1. Measurement circuits
    - DC voltages and Source
    - load currents
2. System software
3. Control hardware
    - IGBT driver circuit
    - Buffer (isolation) circuit
    - Dead-band circuit
4. Power circuit of inverters

7.1.2 Measurement Circuits

For the accurate and reliable operation of a system, measurement of various system parameters and their conditioning is required. The measurement system must fulfil the following requirements:

1. High accuracy

2. Galvanic isolation with power circuit
3. Linearity and fast response
4. Ease of installation and operation

With the availability of Hall-effect current sensors and isolation amplifiers, these requirements are fulfilled to a large extent. In order to implement the control algorithm, current and voltage need to be sensed.

7.1.2.1 Sensing of AC Current

The currents have been sensed using the PCB-mounted Hall-effect current sensors (TELCON HTP50). The HTP50 is a closed loop Hall effect current transformer suitable for measuring currents up to 50 A. The current sensing circuit is shown in Figure 7-2.

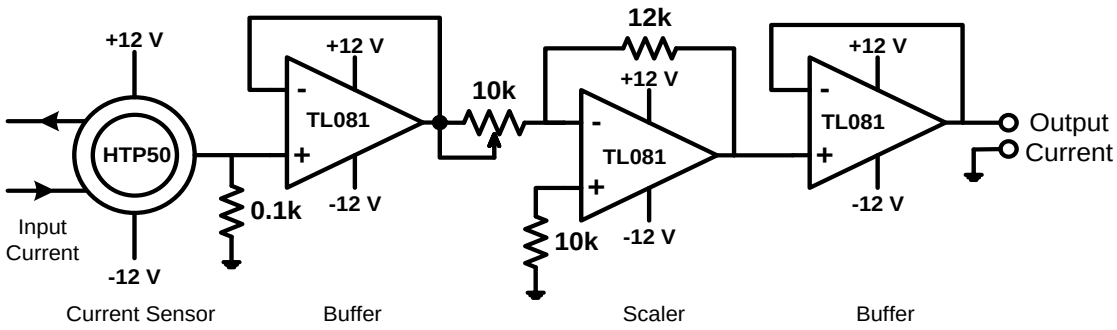


Figure 7-2 Current sensing circuit

This device provides an output current into an external load resistance. These current sensors provide the galvanic isolation between the high voltage power circuit and the low voltage control circuit and require a nominal supply voltage of the range ±12V to ±15V. It has a transformation ratio of 1000:1 and thus, its output is scaled properly to obtain the desired value of measurement.

7.1.2.2 Sensing of Voltage

The voltages are normally sensed using isolation amplifiers and among them, AD202 is a general purpose, two-port, transformer-coupled isolation amplifier that can be used for measuring both AC and DC voltages. The other main features of the AD202 isolation amplifier are:

1. Small physical size
2. High accuracy
3. Low power consumption
4. Wide bandwidth
5. Excellent common-mode performance

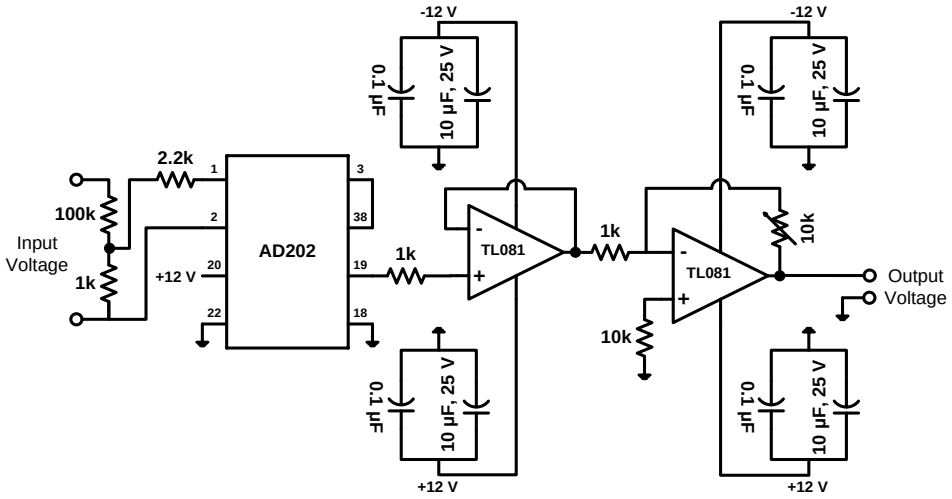


Figure 7-3 AC/DC voltage sensing circuit

This voltage sensor can sense voltages in the range of ±1 kV (peak) and it requires a nominal supply voltage range of ±12V to ±15V. Figure 7-3 shows the circuit diagram for the voltage sensing scheme, which uses AD202 isolation amplifier. The voltage (AC or DC) to be sensed is applied between the terminals 1 and 2 (across a voltage divider comprising of 100 kΩ and 1 kΩ) and the voltage input to the sensor is available at the pins 1 and 2 of AD202 via a resistance of 2.2 kΩ. The isolated sensed voltage is available at the output terminal 19 of AD202. The output of voltage sensor is scaled properly to meet the requirement of the control circuit and is fed to the RT-Lab via its analog input card channel for further processing.

7.1.3 Development of System Software

Historically. control software was developed using assembly language. In recent years, industry began to adopt MATLAB/Simulink and Real-Time Workshop (RTW) platform-based method, which provides a more systematic way to develop control software. RT-Lab, from Opal-RT Technologies, is used as real-time hardware-in-loop controller to generate gate pulses for IGBTs in real-time. It is a complete real-time control system based on Intel'" 2.6 GHz processor running at RedHat Linux operating system. The offline control algorithm developed in MATLAB/Simulink platform is converted and transported to the Spartan-3 FPGA board of RT-Lab using Opal-RT's compiler RT-Lab version 10.7. This saves the time and effort twice as there is no need to manually convert the Simulink model into another language such as C and one need not to be concerned about a real-time program frame and I/O function calls, or about implementing and downloading the code onto the RT-Lab. The process is notably very efficient when applied to input/output because RT-Lab provides a set of Simulink block that automatically configure common I/O functions like analog inputs (feedback signals) and time-stamped digital outputs, with a resolution of 10 nanoseconds. The generated digital output signals are taken out from digital output card and fed to various IGBTs driver circuits via isolation and dead-band

circuits. Figure 7-4 shows the schematic diagram of RT-Lab board interfaced with the host computer and the real-world plant (MPCI converter system). The sensed signals from the real-world are fed to the analog input card to use these signals for controlling or monitoring purpose.

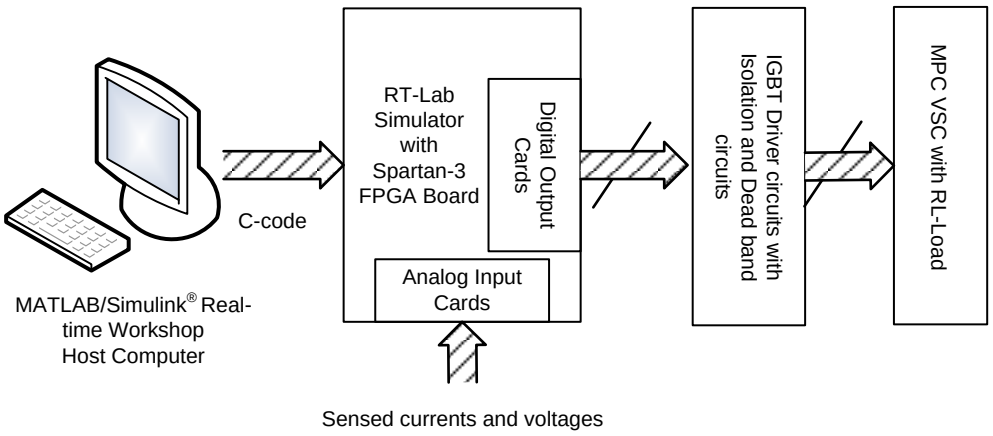


Figure 7-4 RT-Lab and MATLAB real-world interfacing.

7.2 Control Hardware

The block diagram of MPCI system connected to RL load is shown in Figure 7-1. The control algorithm is designed and built in MATLAB/Simulink software and the control pulses for IGBTs are generated by Opal-RT real-time simulator using Spartan-3 FPGA board. The optimized C-code of the Simulink model of control algorithm is generated with the help of Meta-controller compiler. The control pulses are generated at digital output card of RT-Lab simulator which are interfaced with the IGBT driver circuits through isolation and dead-band circuits. This ensures the necessary isolation of the RT-Lab controller hardware from the power circuit that is required for its protection. Figure 7-5 shows the basic schematic diagram of interfacing firing pulses from RT-Lab controller hardware board to switching devices of 3L NPCI and higher level MPCIs. In this figure the details of only the phase–*a* cluster of 3L NPCI are shown. From Figure 7-5, it can be observed that the following hardware circuits are required for interfacing MPCI with RT-Lab control hardware.$\bar{S}_{a1}$

1. Isolation circuit
2. Dead-band circuit
3. IGBT driver circuits

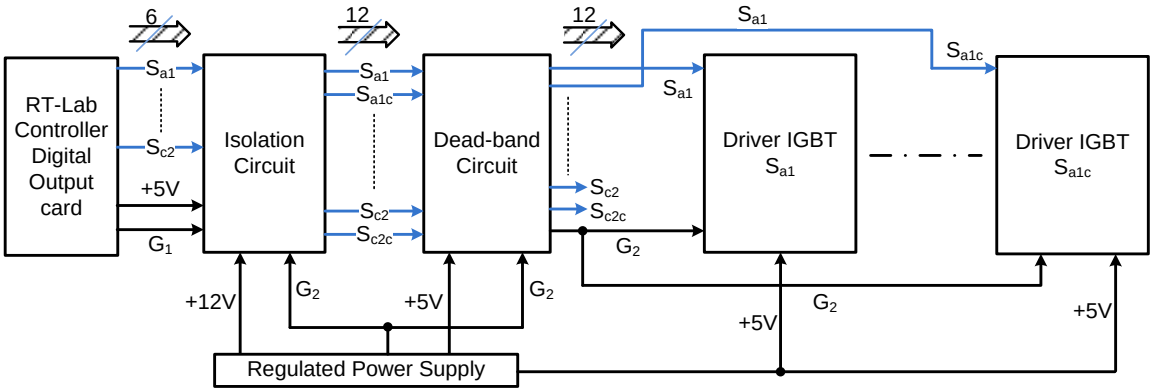


Figure 7-5: Schematic diagram of interfacing firing pulses from RT-Lab controller board to switching devices.

7.2.1 Isolation Circuit

An isolation circuit board is used for optical isolation of RT-Lab hardware from direct connection with the power circuit. Figure 7-6 shows the circuit diagram of the isolation circuit between RT-Lab and power devices of a H-bridge cell. Toshiba built opto-coupler chip (6N137) is used for optical isolation.

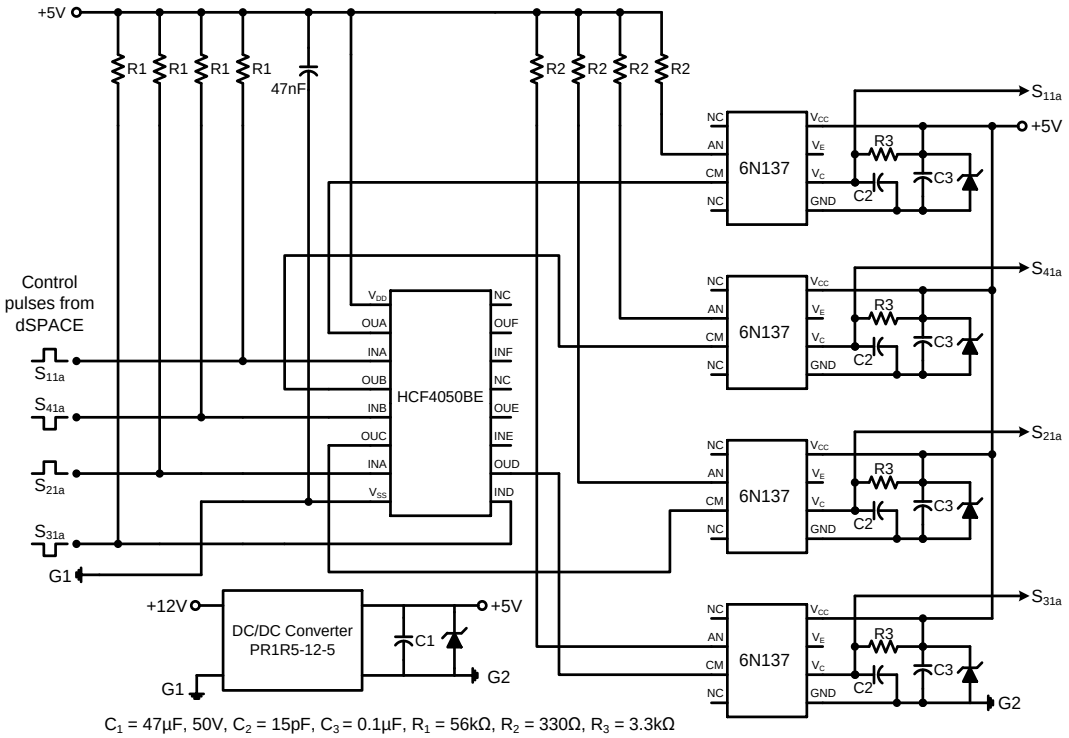


Figure 7-6: Opto-isolation circuit for each switching device.

7.2.2 Dead-band Circuit

A dead-band (dead-time or delay) circuit is employed to provide a delay time (of about 1 µs) between the switching pulses to two complementary devices connected in same leg of an H-bridge cell. This is required to avoid the short circuit of devices in the same leg due to

simultaneous conduction. The delay time between switches of the same leg of H-bridge cell is introduced by a *RC* integrator circuit as shown in Figure 7-7.

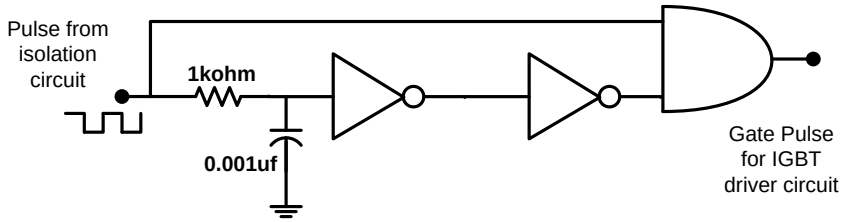


Figure 7-7: Dead-band circuit for each switching device.

An identical dead-band circuit are used for each leg of all H-bridge cells. The different switching signals obtained experimentally for semiconductor devices in the same leg of an H-bridge cell are shown in Figure 7-8 with 1 µs delay. In Figure 7-8 the top and bottom signals are for the switches S_{11a} and S_{41a} respectively.

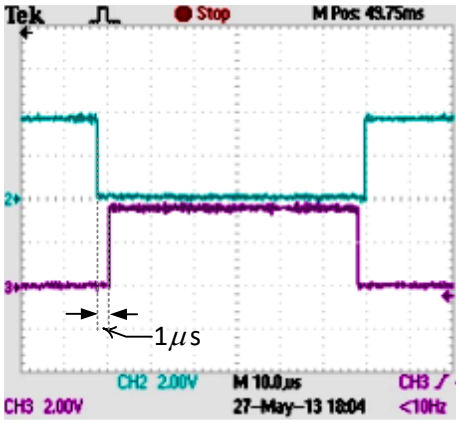


Figure 7-8: Firing signals for the switches S_1 and S'_1 with dead-band circuit.

7.2.3 IGBT Driver Circuits

The IGBT driver circuits are used for pulse amplification and isolation purposes. The IGBT driver circuits not only amplify the pulse signals for driving the devices but also provide an optical isolation. The driver circuit has special features such as fault protection and protection against the under-voltage lockout. HCPL-316J chip from Agilent Technologies is used as an IGBT driver chip. It can drive IGBTs up to 150 A at an applied voltage up to 1200 V. Figure 7-9 shows the circuit diagram of the IGBT driver circuit. During normal operation, V_{out} (pin no. 11) of the HCPL-316J is controlled by either by VLN+ (pin no. 1) or VLN- (pin no. 2), with the IGBT collector-to-emitter voltage being monitored at D_{SAT} (pin no. 14). The FAULT output is high and the RESET input should be held high. (FAULT and RESET are active low signals). When the voltage on the D_{SAT} pin (pin no. 14) exceeds 7 V, while IGBT is on, V_{OUT} on pin no. 11 is slowly brought low in order to “softly” turn-off the IGBT and prevent large induced voltages. Also, an internal feedback channel is activated which brings FAULT output (pin no. 6) low for the purpose of notifying the microcontroller of the fault condition. The FAULT output

remains low until RESET is brought low. An LED indication is provided in each driver circuit to indicate the occurrence of a fault, thus prompting a corrective action, either manually or through a microcontroller. The HCPL-316J Under Voltage Lockout (UVLO) feature is designed to prevent the application of insufficient gate voltage to IGBT by forcing the HCPL-316J output low during power-up. IGBTs typically require gate voltages of 15 V to achieve their rated $V_{CE(ON)}$ voltage. At gate voltages below 12 V typically, their on-voltage increases dramatically, especially at higher currents. At very low gate voltages (below 10 V), the IGBT may operate in the linear region and quickly overheat. The UVLO feature causes the output to be clamped whenever insufficient operating supply voltage is applied.

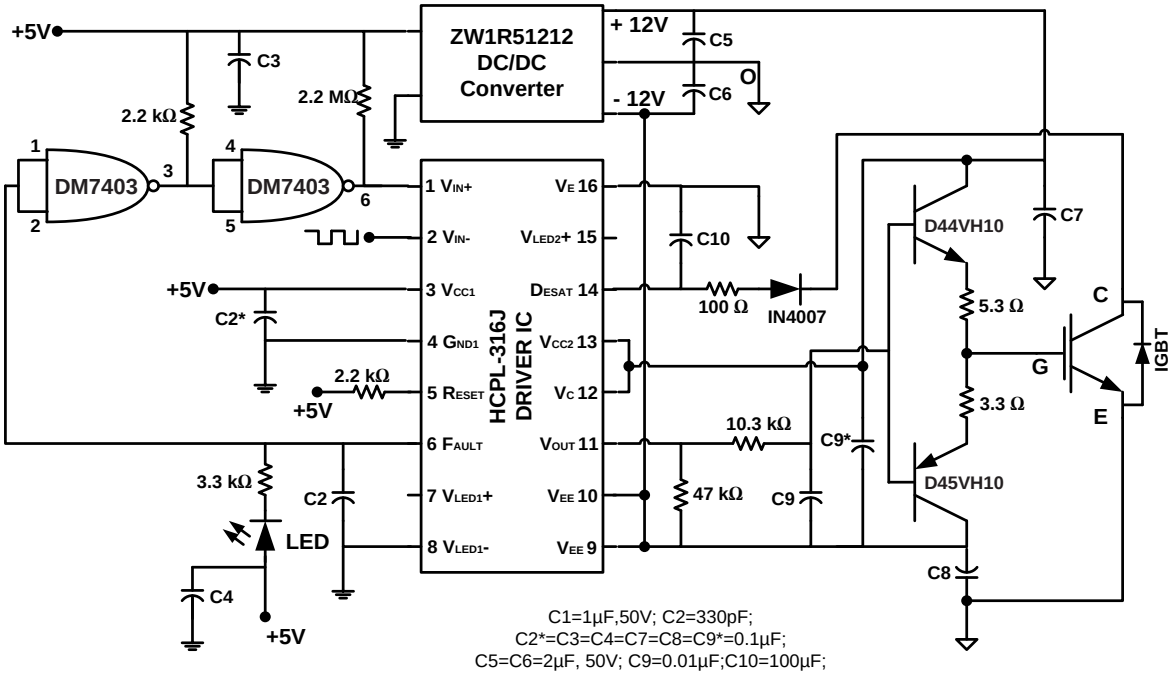


Figure 7-9: IGBT driver circuit.

7.2.4 Snubber Circuit

To protect each switching device, a suitably designed snubber circuit is connected across it as shown in Figure 7-10. The snubber comprises of a parallel combination of a resistor and a capacitor connected across a Metal-Oxide Varistor (MOV). All the devices are mounted on heat sinks to ensure proper heat dissipation.

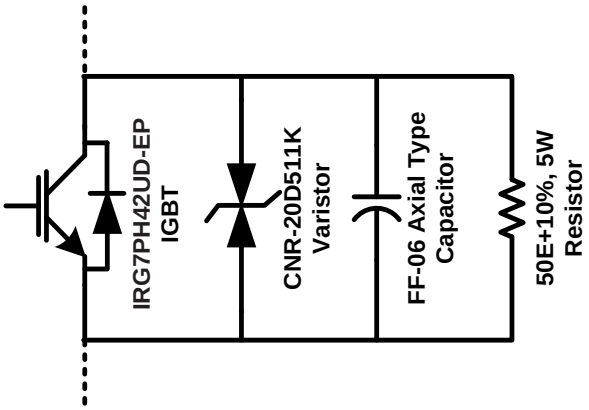


Figure 7-10: Snubber circuit used for switching device

7.2.5 Power Circuit of Inverters

The below mentioned VSI prototypes which are operated as DC-AC converters have been developed in the laboratory.

i. Three-phase 3-level NPCI.
ii. Three-phase hybrid 2/3L NPCI
iii. Three-phase 4L RSS MPCI.
iv. Three-phase 5L MPCI Type-1 and Type-2 RSS VSIs.

These topologies are tested as DC-AC converters and the power circuits were validated with the help of three phase RL load. The power circuits of VSI with suitably designed loads and sources on its AC and DC side are developed respectively. The number of self-commutated power semiconductor switches with anti-parallel diodes (IGBTs) and the number of DC link capacitors depends on the VSI topology used. The isolated four DC supplies for the inverter are provided by two single-phase, three-winding transformers (230/115/115 V, 3 kVA) with single-phase diode bridge rectifiers (KBPC3510) and filter capacitors (450 V, 2200 µF each). A three-phase lamp load and inductors are used as a load for the VSI.

The Simulink models of the various PWM controller schemes of the inverter are implemented using RT-Lab controller. The generated firing pulses are given to the corresponding semiconductor devices of the MPCI topologies with the help of delay and pulse amplification circuits in real-time.

7.3 Performance Investigation of 3L NPCI

The downscaled prototype of 3L NPCI as shown in Figure 7-11 is built and tested for the flowing parameters: V_{DC}=100 V, C_1=C_2=1000µF/47µF, RL load=5Ω/20 mH per phase. The performance with different modulation algorithms discussed in chapter-3 are investigated experimentally and various results are presented.

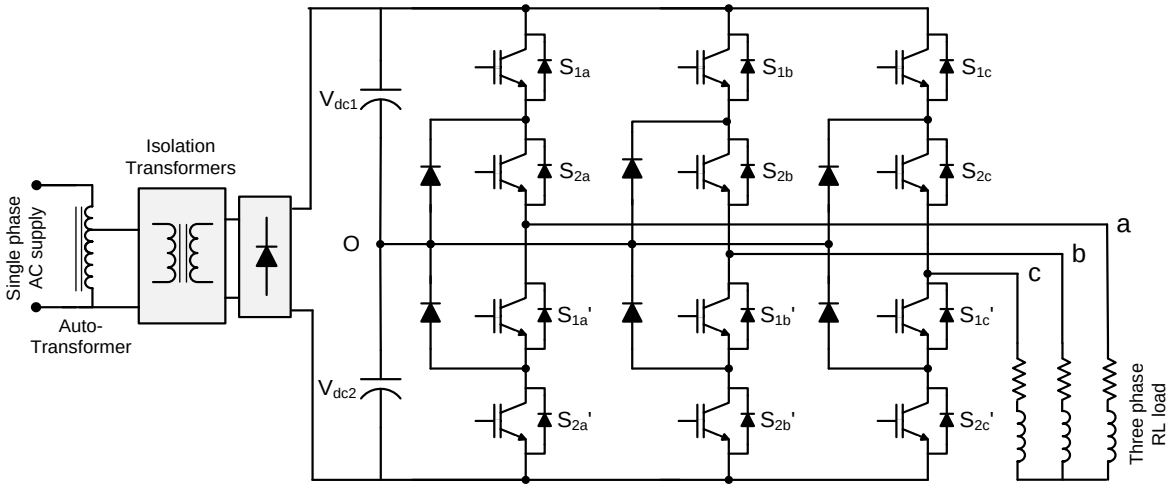


Figure 7-11 Experimental Setup of three-phase 3L NPCI with RL load.

7.3.1 Performance of 3L NPCI With SVM Based on Two-Level SVD:

7.3.1.1 For Higher Modulation Indices

Figure 7-12 through Figure 7-13 show the experimental and simulation results at m=0.98 with NTV modulation discussed in chapter 3. For the given RL load (φ=51.5º lagging), NTV modulation cannot suppress the capacitor voltage oscillations completely. This is due to the load power factor angle, which leads to saturation in the duty ratios of the redundant states. It was found that NTV modulation can suppress the voltage oscillations only 19% of the fundamental cycle. Therefore, low frequency oscillations can be observed in the capacitor voltage waveforms as shown in Figure 7-12 with the NTV modulation even with relatively large DC link capacitance of C_1=C_2=1000μF. The line-to-line voltage and current waveforms are also presented in Figure 7-12. The harmonic spectra plotted for the experientially obtained line-to-line voltage and current waveforms are presented in Figure 7-12 (b) and (c) respectively using the FFT tool in MATLAB up to 100th harmonic.

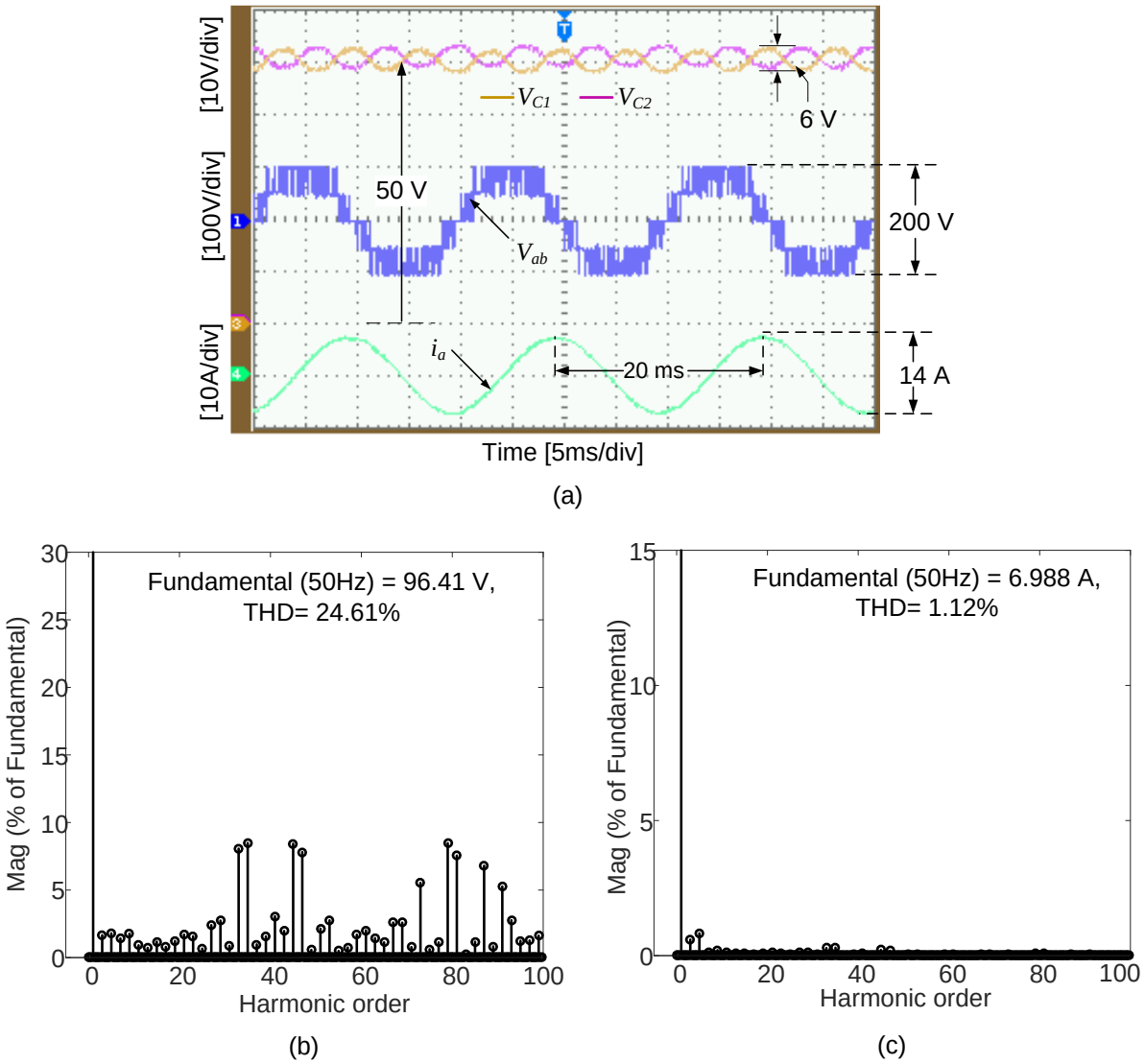
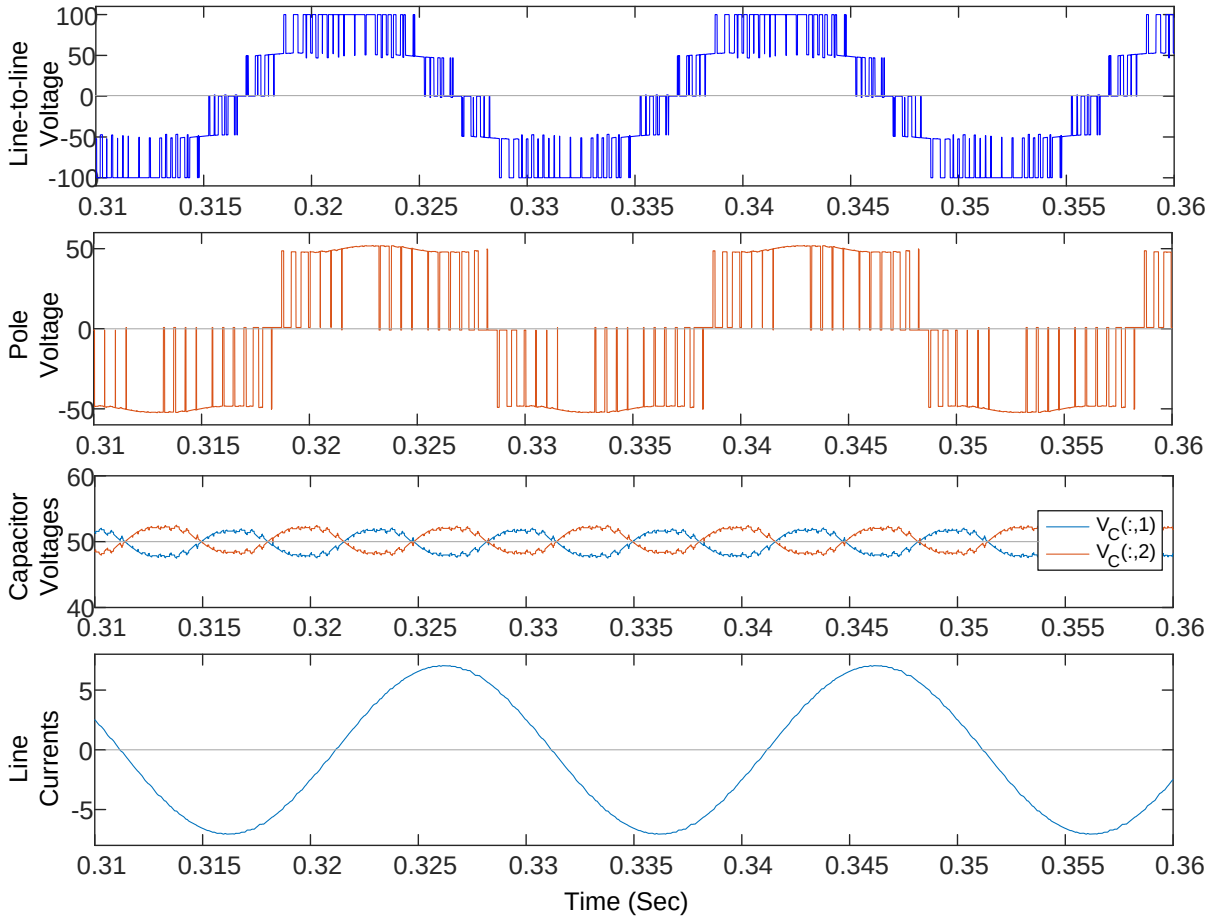
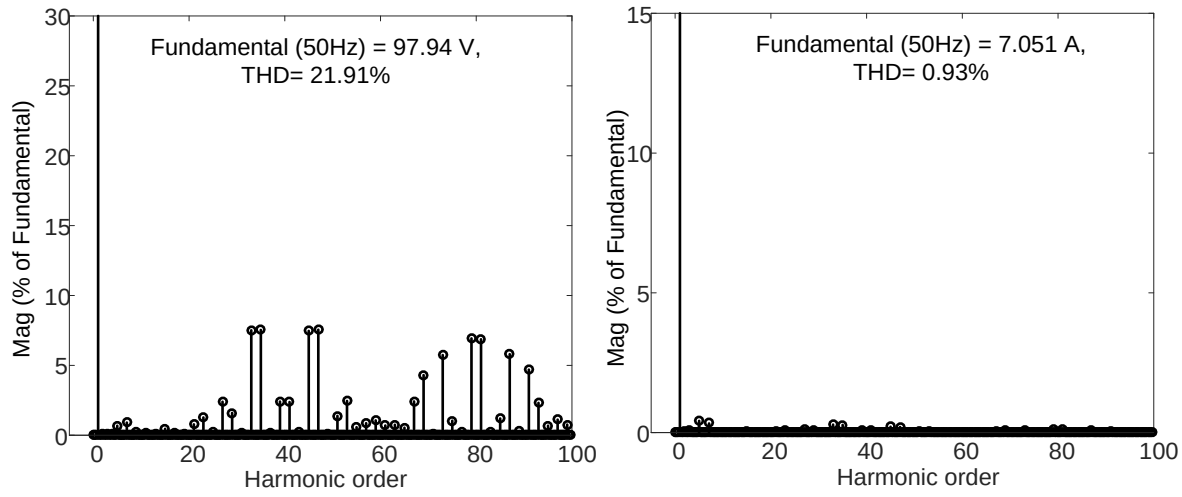


Figure 7-12 Experimental results of 3L NPCI VSI at m=0.98, C_1=C_2=1000μF, RL load=5 Ω/20 mH for NTV modulation: (a) Voltage and current waveforms (top trace: capacitor voltages, middle trace: line-to-line voltage and bottom trace: Phase-a current); Harmonic spectrum of (b) Line to line voltage and (c) Line current.

The down scale simulation has been performed in MATLAB for the same operating conditions. Figure 7-13 (a) shows the obtained simulation waveforms at m=0.98 with NTV modulation. Figure 7-13 (b) and (c) show the harmonic spectra of the line-to-line voltage and current waveforms using the FFT tool up to 100th harmonic are presented respectively. The capacitor voltages and other waveforms show the similar performance with the NTV modulation. Therefore, the hardware results show agreement with the down scale simulation results.



(a)



(b) (c)

Figure 7-13 Simulation Results at m=0.98, C_1=C_2=1000μF, RL load=5 Ω/20 mH with NTV modulation: (a) Voltage and current waveforms; Harmonic spectrum of (b) Line-to-line voltage and (c) Line current.

Figure 7-14 show the experimental results with the NTVV modulation at m=0.98 for the same operating conditions. It is evident that the capacitor voltage ripple is almost negligible by NTVV

modulation. However, the modulation increases the THD of line-to-line voltage is significantly at the high frequency range of spectrum over NTV as shown in Figure 7-14 (b). With regards to line currents, a small increase in THD is noticed as shown in Figure 7-14 (c), because at the high frequency range, the impedance values are also high.

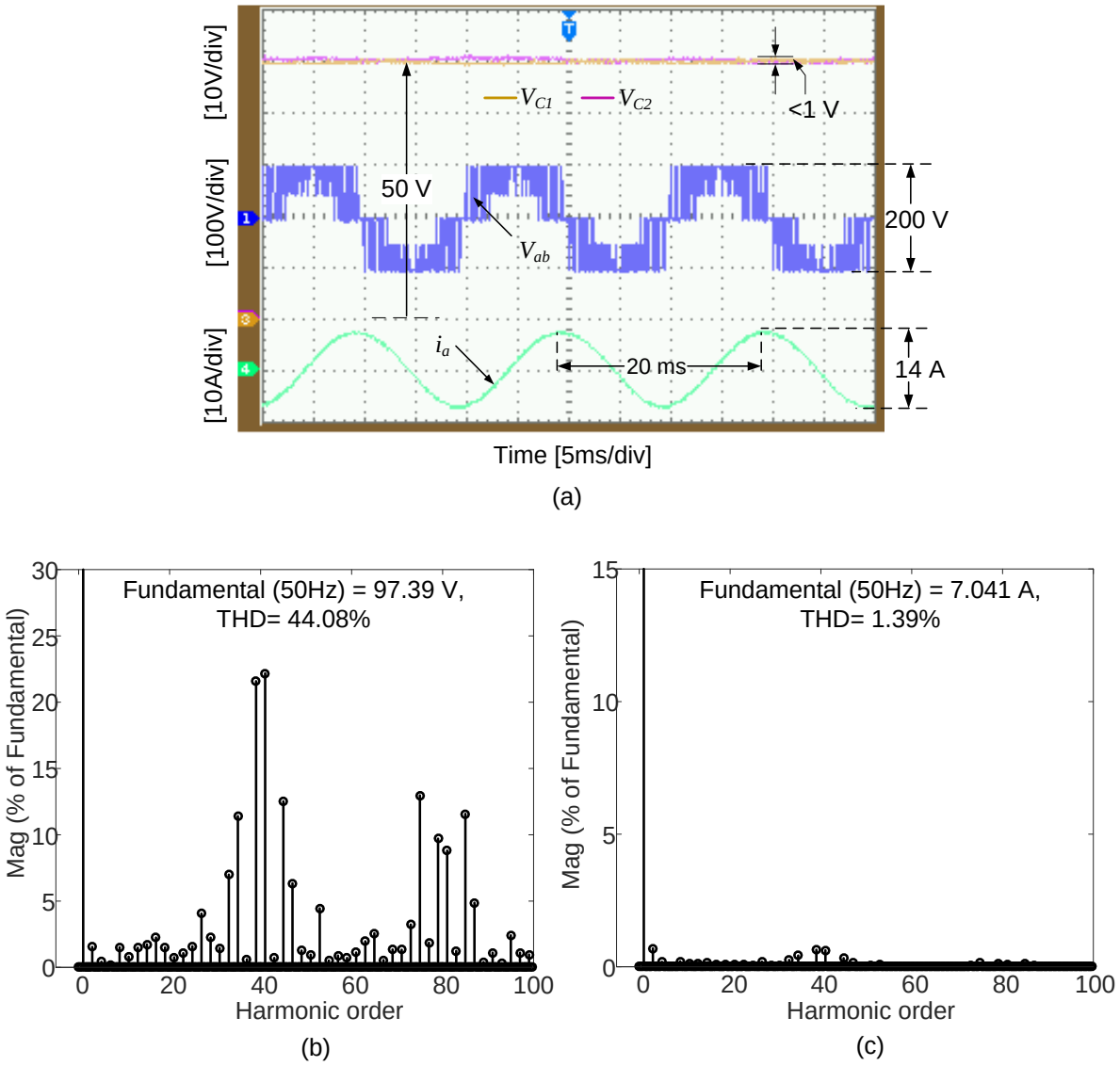
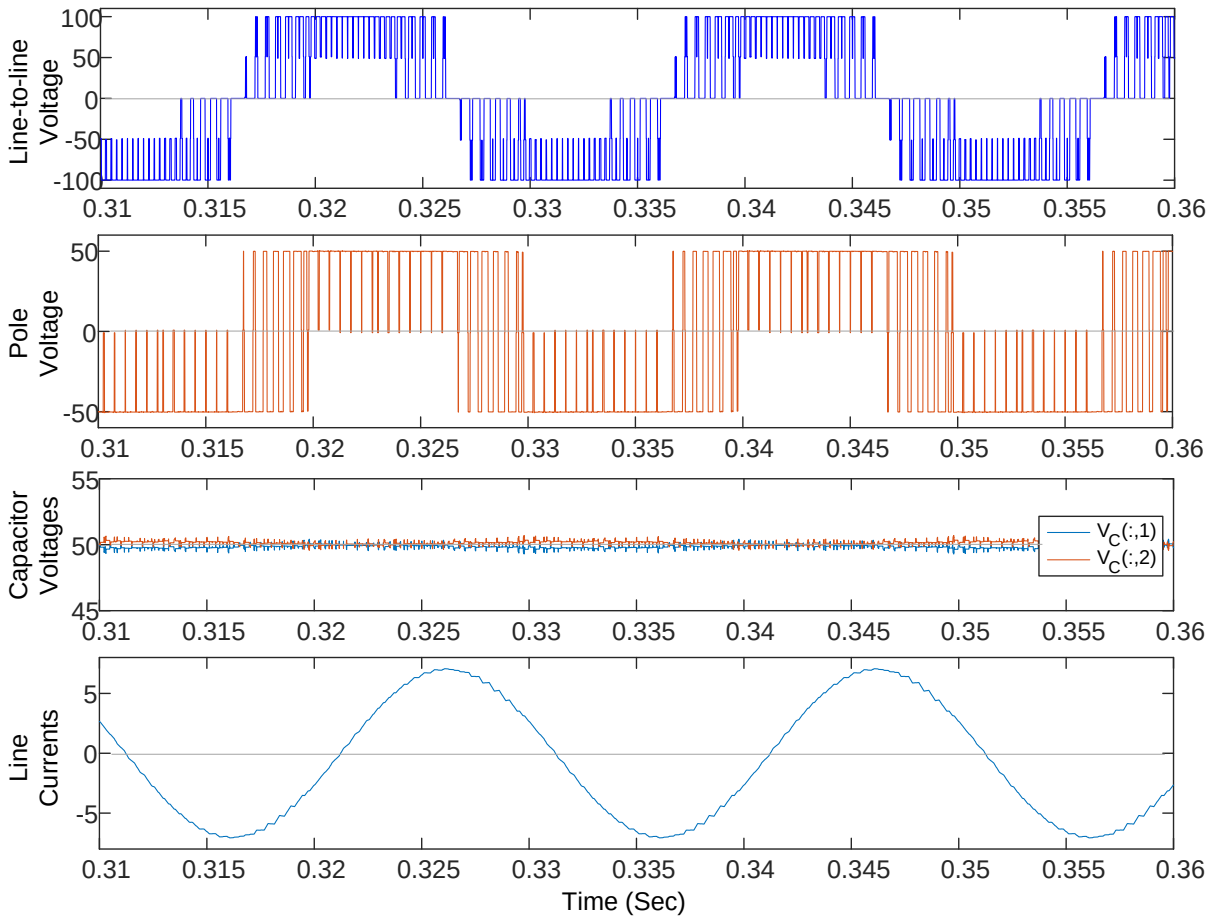
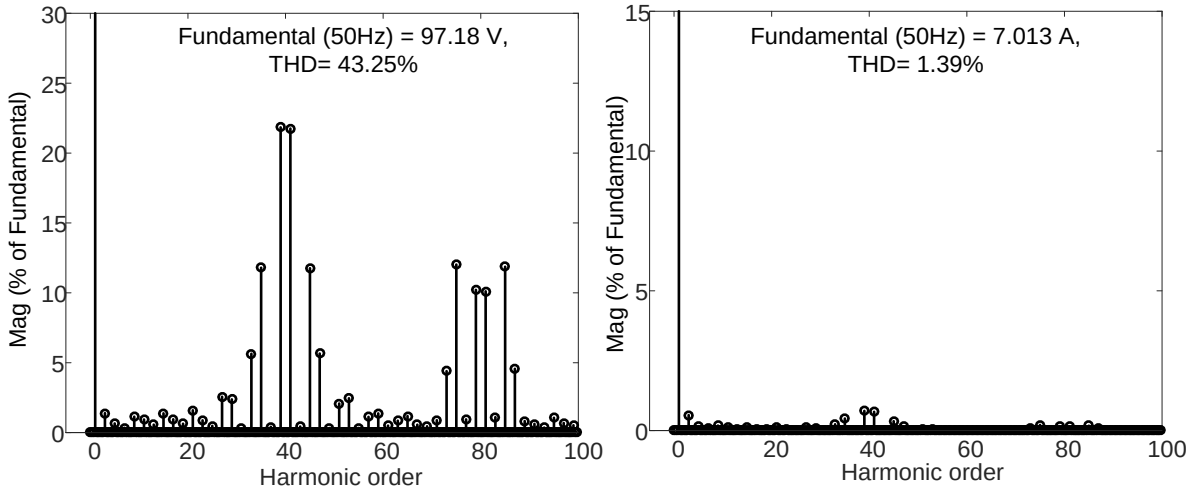


Figure 7-14 Experimental results of 3L NPCI under m=0.98, C_1=C_2=1000μF, RL load=5 Ω/20 mH for NTVV modulation: (a) Voltage and current waveforms (top trace: capacitor voltages, middle trace: line-to-line voltage and bottom trace: Phase-a current); Harmonic spectrum of (b) Line to line voltage and (c) Line current.

The down scale simulation results with NTVV modulation are shown in Figure 7-15 for the same operating conditions. The experimental capacitor voltages and other waveforms show good agreement with the down scale simulation results.



(a)



(b) (c)

Figure 7-15 Simulation Results at m=0.98, C_1=C_2=1000μF, RL load=5 Ω/20 mH for NTVV modulation: (a) Voltage and current waveforms; Harmonic spectrum of (b) Line-to-line voltage and (c) Line current.

Figure 7-16 and Figure 7-17 show the experimental and simulation results with the STV modulation at m=0.98 for the same operating conditions. It can be observed that, STV shows the similar performance outcomes as given by NTVV modulation with low switching frequency. Therefore, it is concluded that the non-NTV modulations: NTVV and STV can completely eliminated that low frequency oscillations for higher modulation index and low power factor operations at the expense of increased line-to-line voltage THD.

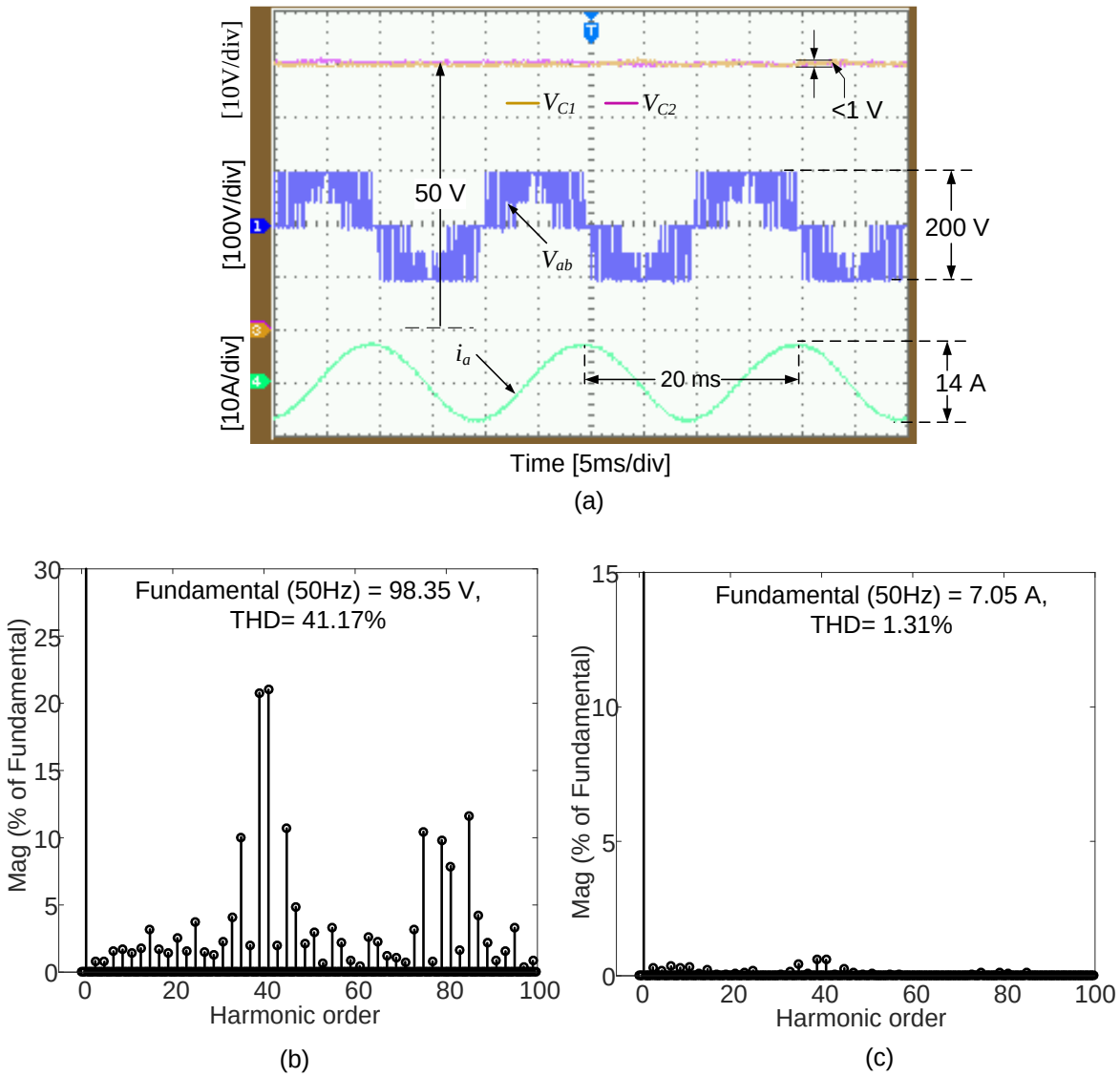
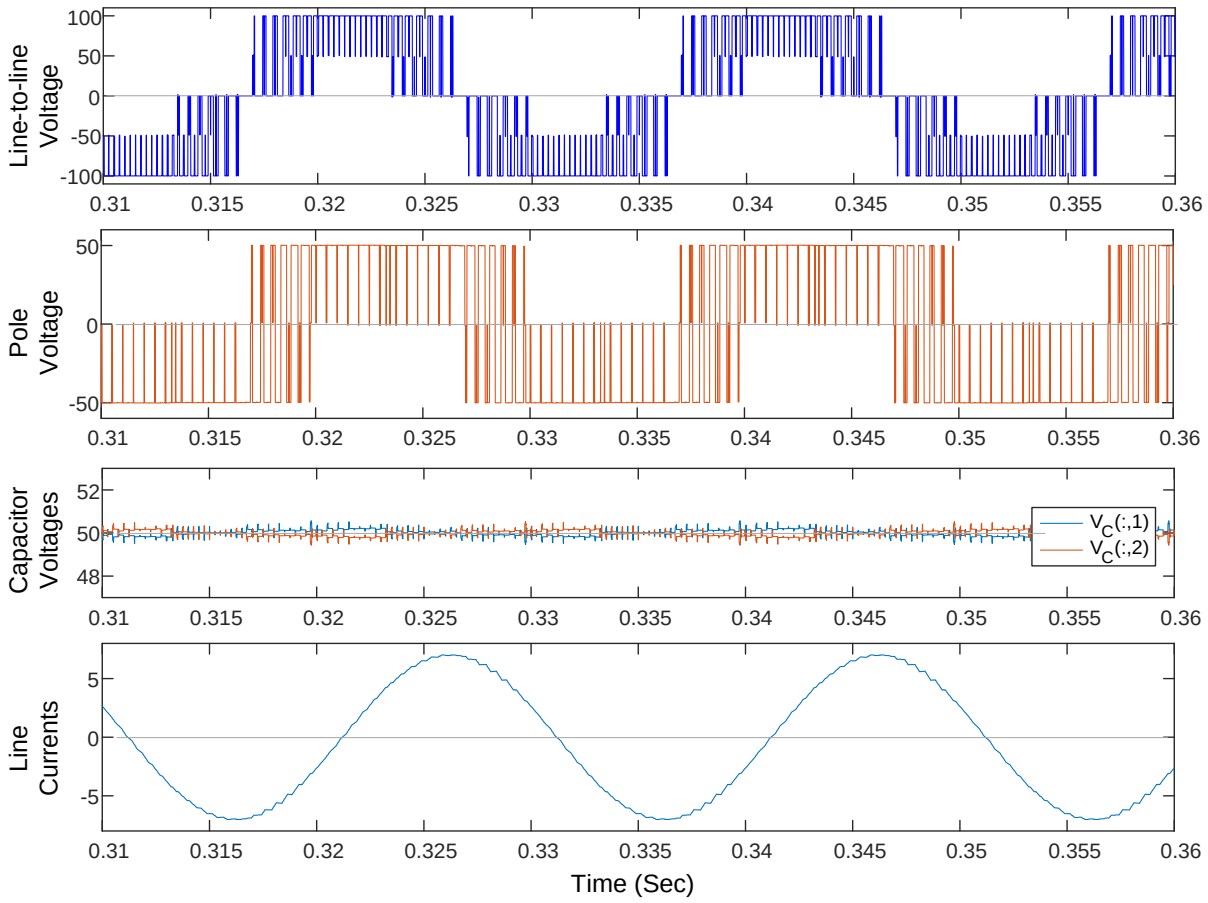
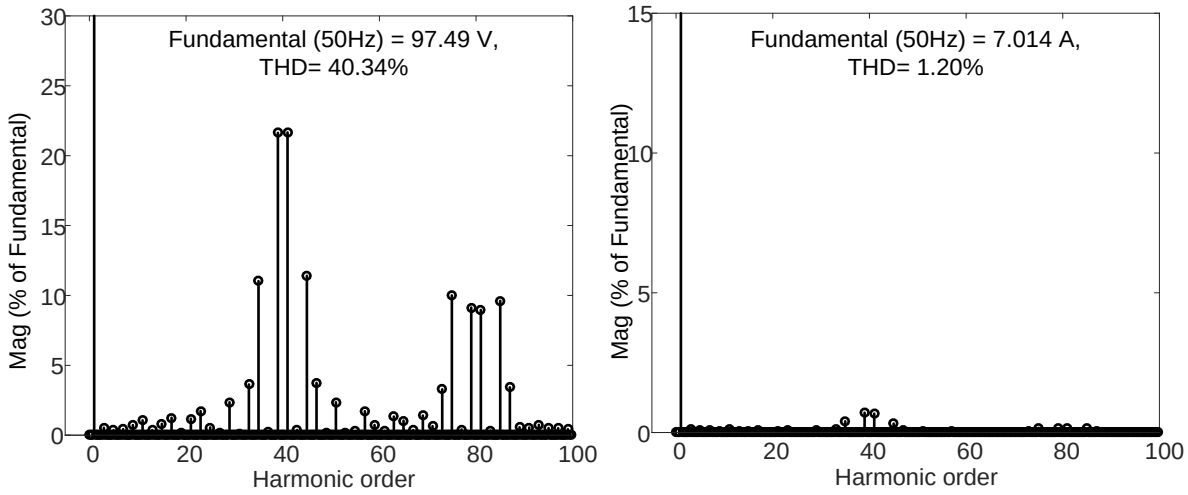


Figure 7-16 Experimental results of 3L NPCI at m=0.98, C_1=C_2=1000μF, RL load=5 Ω/20 mH for STV modulation: (a) Voltage and current waveforms (top trace: capacitor voltages, middle trace: line-to-line voltage and bottom trace: Phase-a current); Harmonic spectrum of (b) Line to line voltage and (c) Line current.



(a)



(b) (c)

Figure 7-17 Simulation Results at m=0.98, C_1=C_2=1000μF, RL load=5 Ω/20 mH for STV modulation: (a) Voltage and current waveforms; Harmonic spectrum of (b) Line-to-line voltage and (c) Line current.

In order to observe the influence of capacitance value of the DC-link capacitors on the modulation methods, DC link capacitors are changed to C_1=C_2=*47µF.* Figure 7-18 (a) and (b) shows the experimental results obtained with the NTV and STV modulations. It can be observed from Figure 7-18 (a) that, as the capacitance value is reduced, the NP voltage ripple is significantly increased in case of NTV modulation. This because of the non-zero NP current flowing in NP for the given RL load of 5 Ω/20 mH per phase flows through the capacitors and results in low frequency voltage oscillations. However, regardless of the capacitance value, the capacitor voltages are oscillations free with the STV modulation as shows in Figure 7-18 (b).

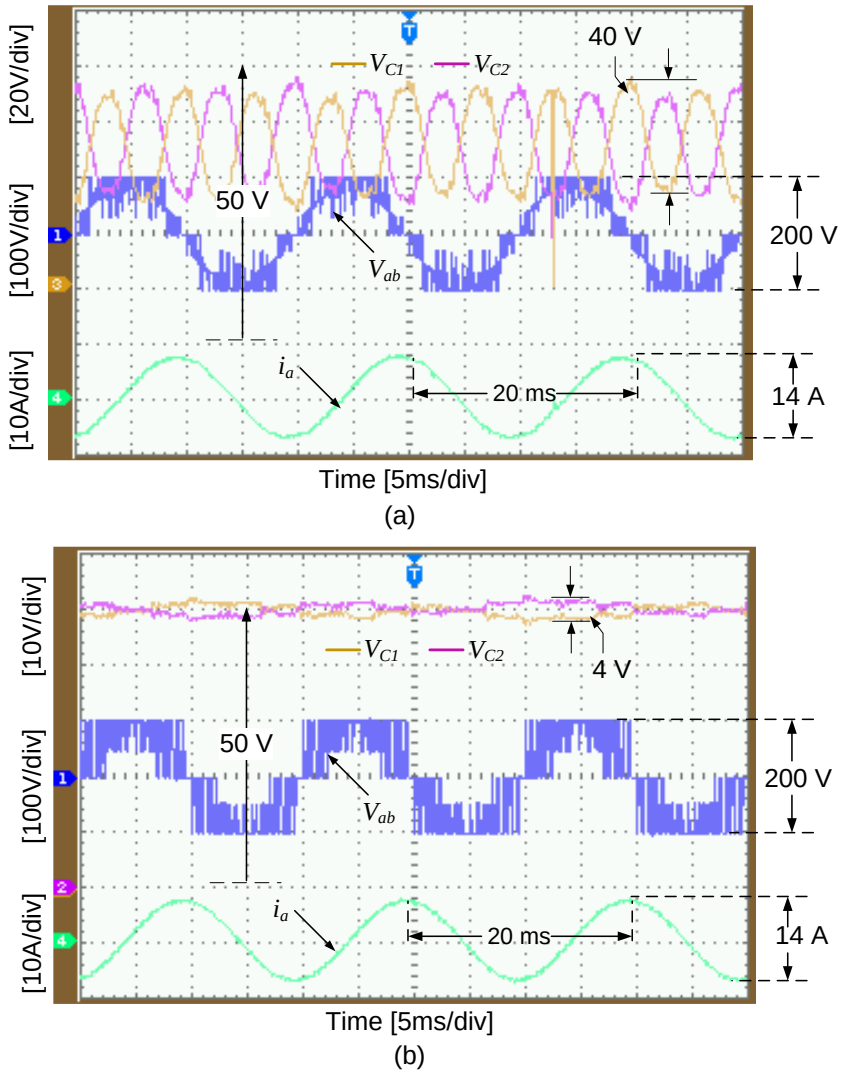


Figure 7-18 Experimental results under *m*=0.98, C_1=C_2=47µF and RL load =*5 Ω/20 mH* for (a) NTV, (b) STV (top trace: capacitor voltages, middle trace: line-to-line voltage and bottom trace: Phase-*a* current).

7.3.1.2 For Lower Modulation Indices

Figure 7-19 and Figure 7-20show the experimental results for m=0.5 with the RL load of 5Ω/20mH per phase. It can be observed that, NTV modulation (Figure 7-19 (a)) itself is capable of maintaining capacitor voltages free from oscillations. The line to-line voltage, pole voltage, capacitor voltage and line current waveforms of experimental and simulation results match closely.

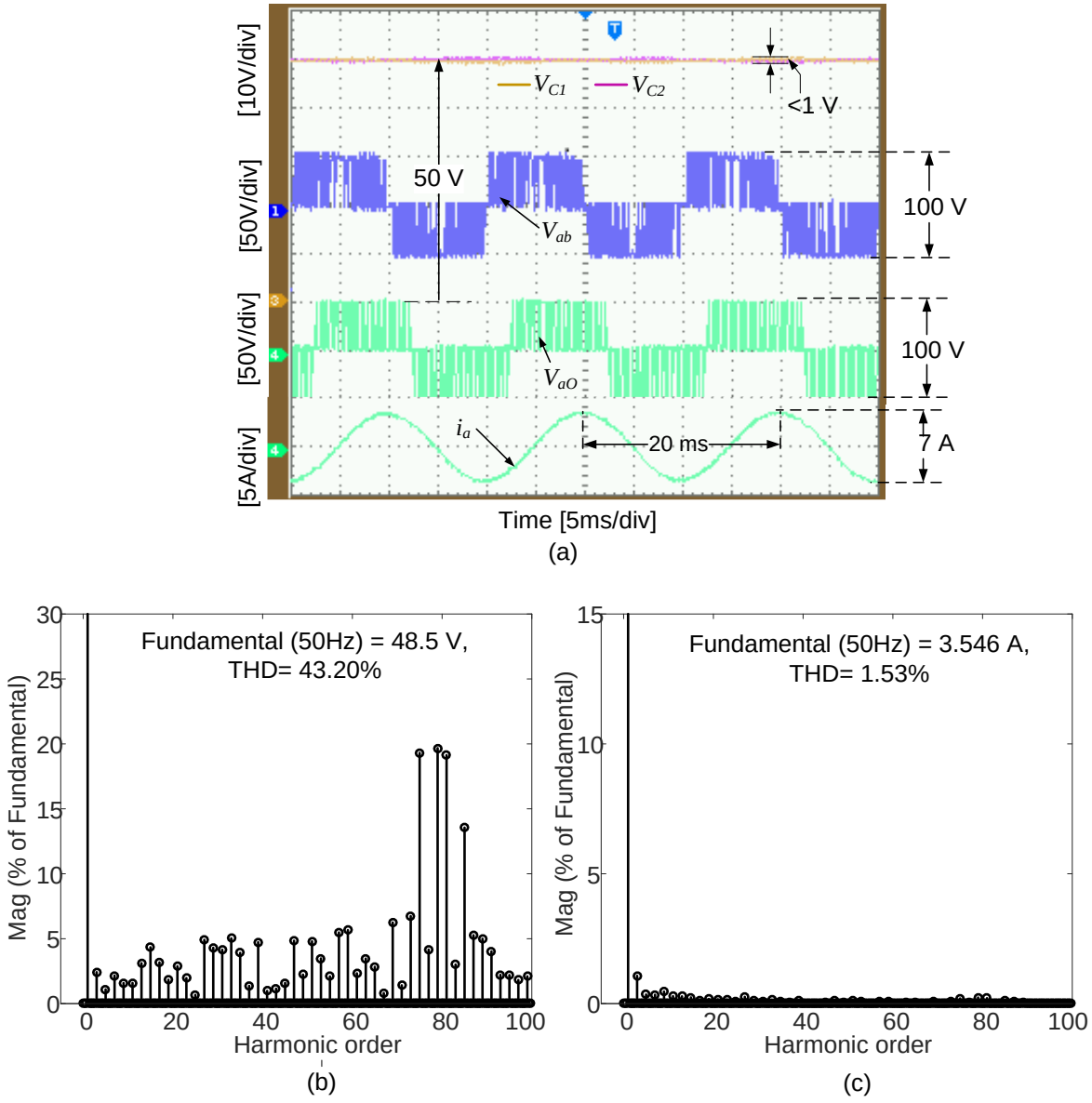
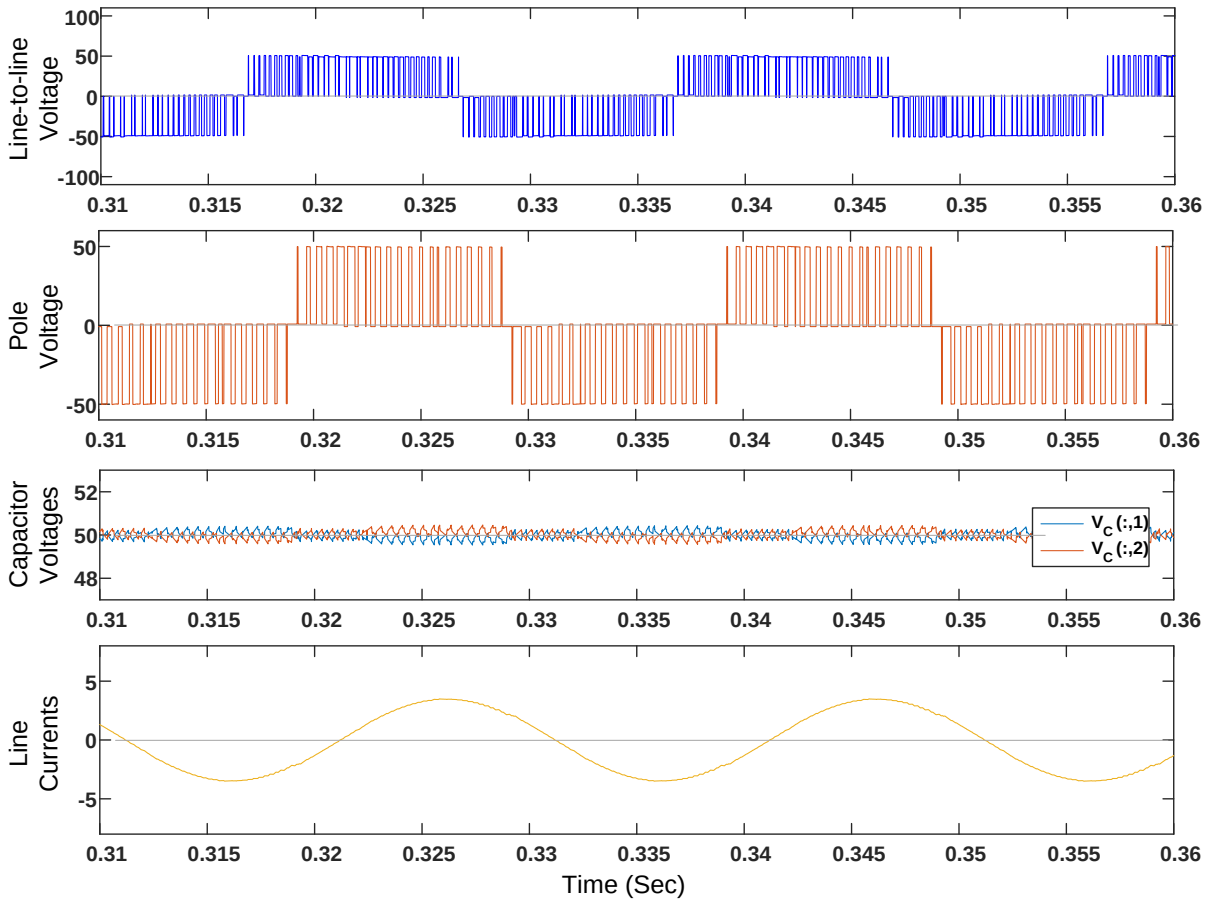


Figure 7-19 Experimental results under m=0.5, C_1=C_2=1000μF and RL load =5 Ω/20 mH for NTV, (top trace: capacitor voltages, top-middle trace: line-to-line voltage, bottom-middle trace: pole voltage and bottom trace: Phase-*a* current).



(a)

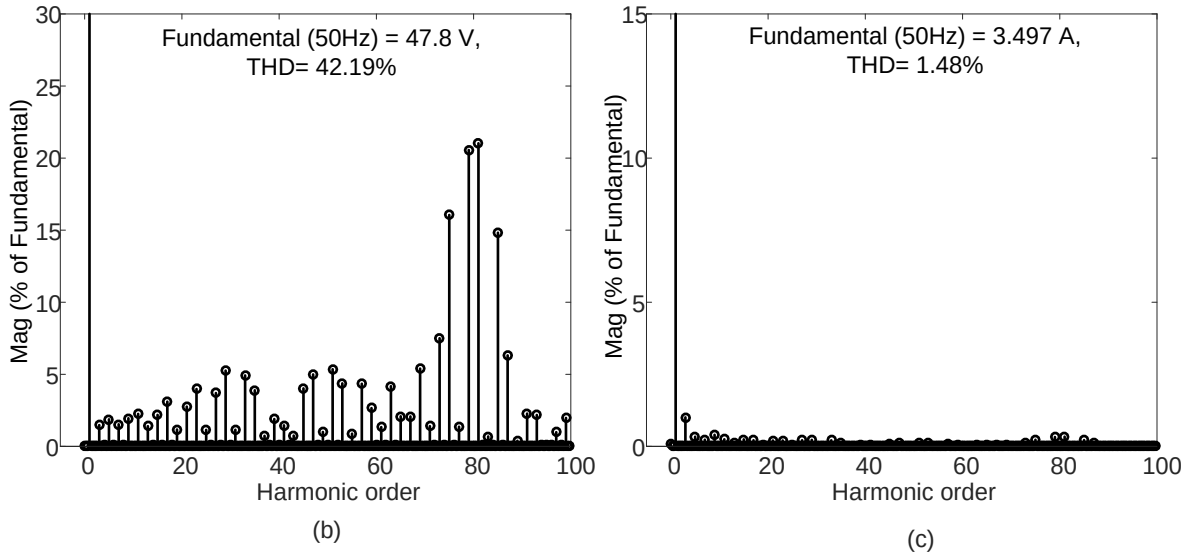


Figure 7-20 Simulation Results at m=0.5, C_1=C_2=1000μF, RL load=5 Ω/20 mH for NTV modulation: (a) Voltage and current waveforms; Harmonic spectrum of (b) Line-to-line voltage and (c) Line current.

NTVV/STV was also tested using the switching sequence-2 discussed in chapter-3 for m=0.5 and obtained waveforms are shown in Figure 7-21(a). the capacitor voltages are maintained oscillation free similar to the NTV modulation. However, a noticeable difference can be

observed in the pole voltages of these two methods. This is due to the selection of different switching states by the two modulation methods. Since the NTV modulation uses a lower number of commutations compared to the NTVV/STV modulation, it is favorable compared to the non-NTV modulation for the lower modulation index range: $0 < m \leq 0.5$.

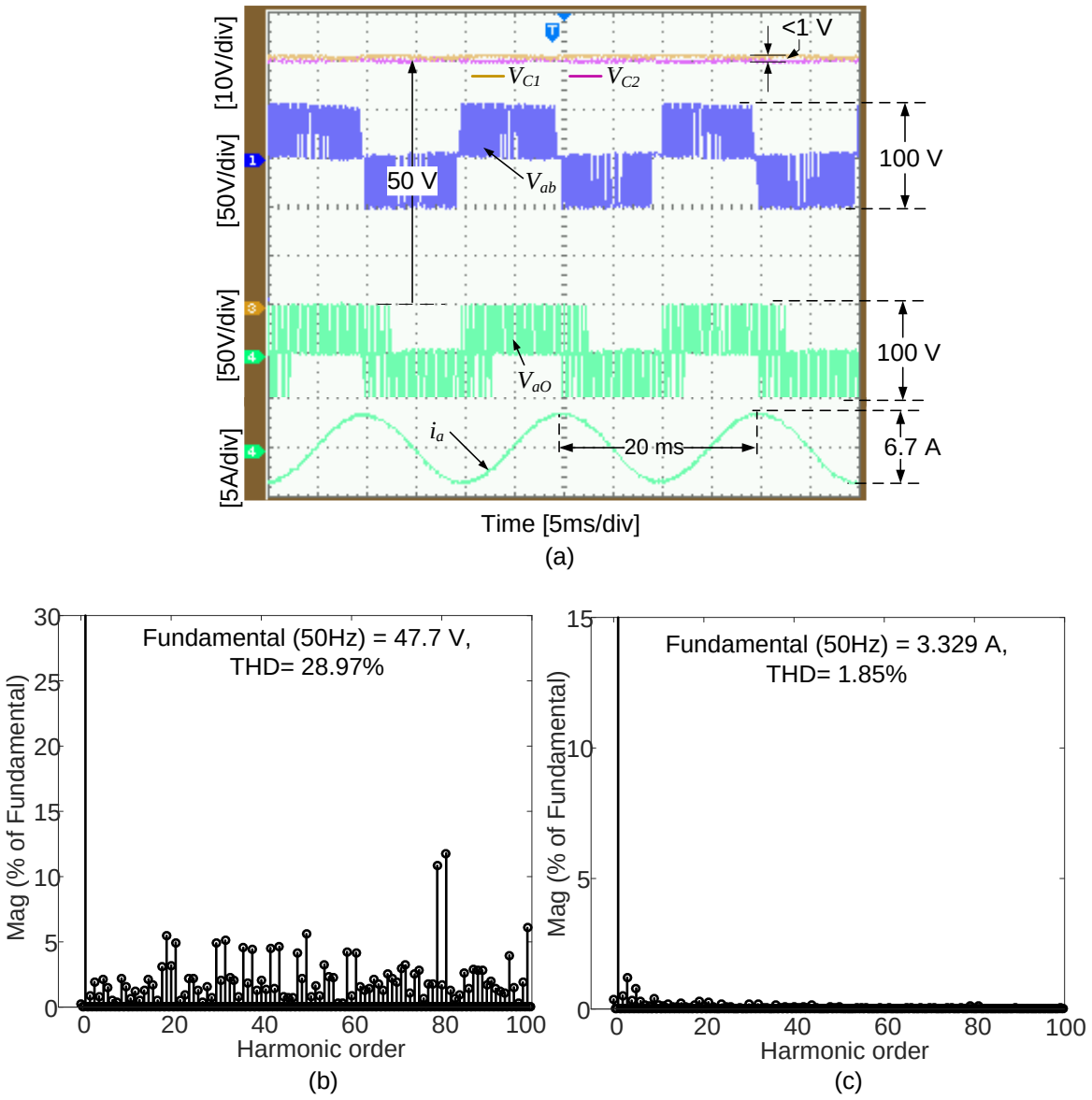
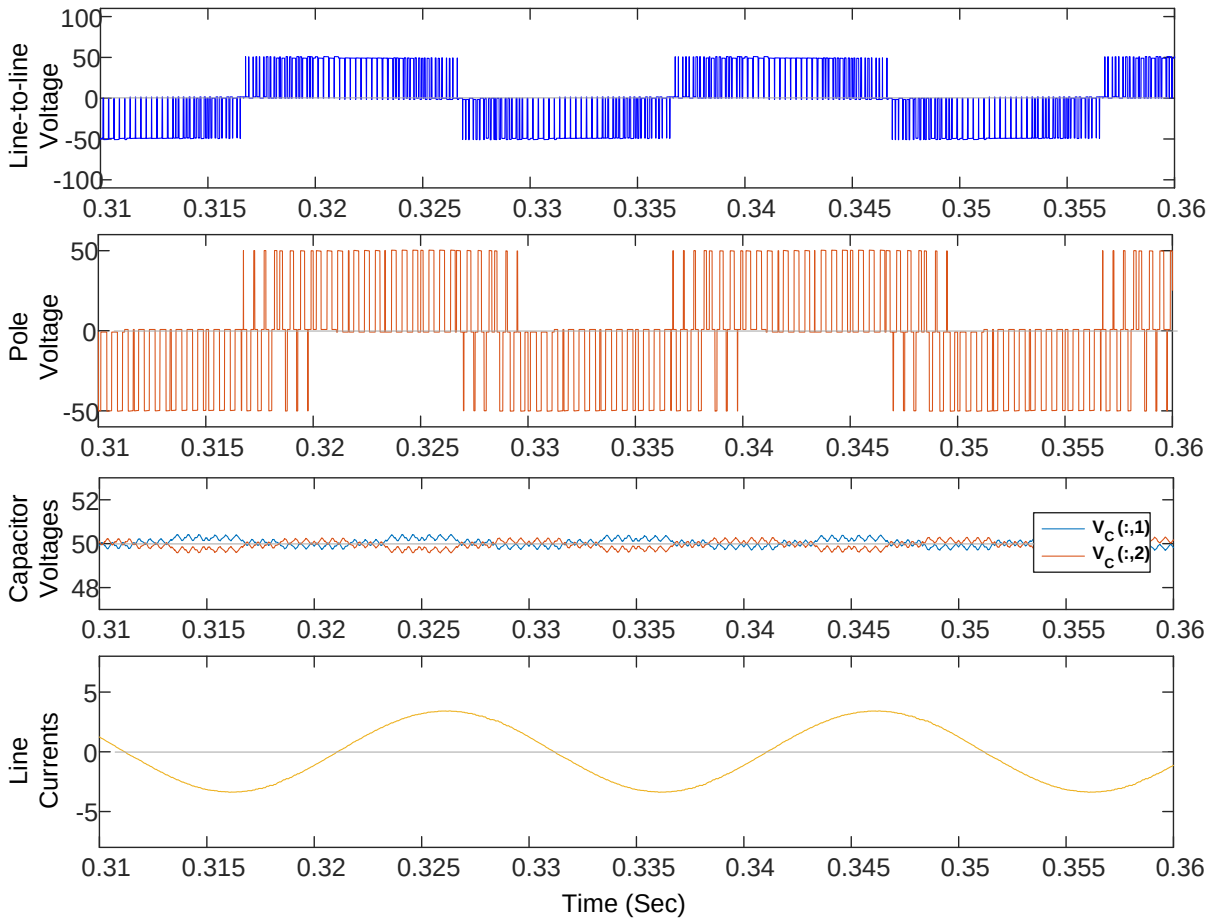
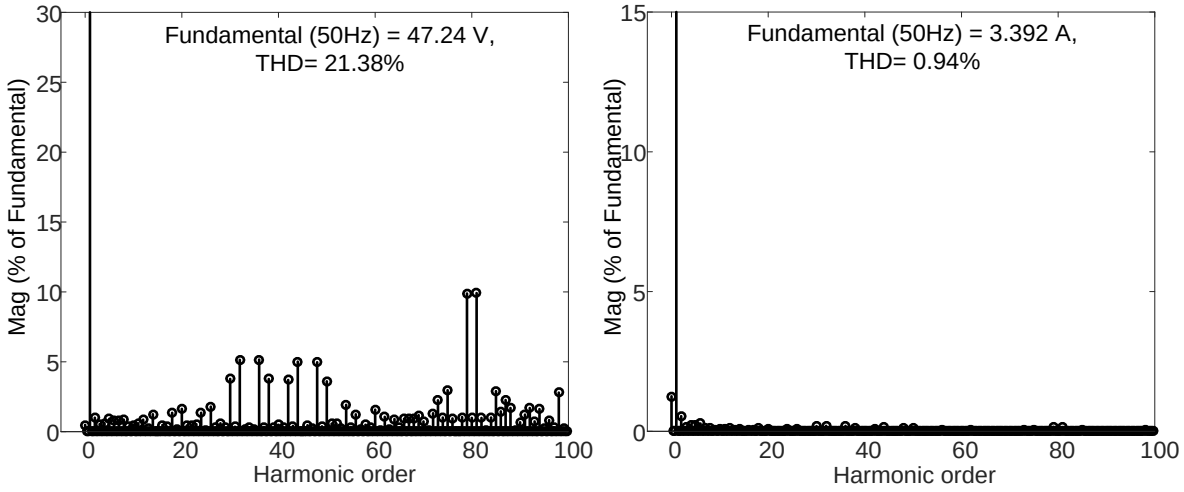


Figure 7-21 Experimental results under m=0.5, C_1=C_2=1000μF and RL load =5 Ω/20 mH for NTVV/STV, (top trace: capacitor voltages, top-middle trace: line-to-line voltage, bottom-middle trace: pole voltage and bottom trace: Phase-*a* current).



(a)



(b) (c)

Figure 7-22 Experimental results under m=0.5, C_1=C_2=1000μF and RL load =5 Ω/20 mH for NTV, (top trace: capacitor voltages, top-middle trace: line-to-line voltage, bottom-middle trace: pole voltage and bottom trace: Phase-*a* current).

The performance of 3L NPCI with various modulation methods for two modulation indices are summarized in Table 7-1

Table 7-1 Comparison of Experimental and downscaled simulation results of 3L NPCI for various modulation methods

Performance Parameter		Modulation index (m)				
		0.98			0.5	
		NTV	NTVV	STV	NTV	NTVV/STV
Line-to-line Voltage (V) (Peak)	Experimental	96.41	97.39	98.35	48.5	47.7
	Simulation	97.94	97.18	97.49	47.8	47.24
% THD of Line-to-line Voltage	Experimental	24.61	44.08	41.17	43.20	28.97
	Simulation	21.91	43.25	40.34	42.19	21.38
Line Current (A) (peak)	Experimental	6.988	7.041	7.05	3.546	3.329
	Simulation	7.05	7.013	7.014	3.497	3.392
% THD of Line Current	Experimental	1.12	1.39	1.31	1.53	1.85
	Simulation	0.93	1.39	1.2	1.48	0.94
Capacitor Voltage Ripple (V)	Experimental	6	<1	<1	<1	<1
	Simulation	5	0.6	0.5	0.5	0.6

7.3.2 Performance of 3L NPCI with Hybrid Modulation Methods:

The experimental validation of the proposed hybrid modulation algorithms discussed in chapter-4 are performed on the downscaled prototype of 3L NPCI shown in Figure 7-11. A DC link voltage of 100V, split capacitors of 470 µF capacitance each, a three phase Wye connected RL load of 5 Ω/20 mH per phase are used for the experimental setup. RT-Lab controller was used to generate firing pluses with switching frequency of 2 kHz for implementing the proposed hybrid modulation strategy.

Figure 7-23 and Figure 7-24 show the various experimental and downscaled simulation results of NPCI operated with NTV modulation method. For the given loading condition with $m = 1$ the NTV sharing is obtained as 16.48 % (from Figure 4-3). This means, the NP voltage oscillations can be eliminated only for 16.48 % duration of fundamental cycle. Therefore, large NP voltage oscillations occurs with the NTV modulation alone as shown in Figure 7-23. This is also apparent from the simulation results shown in Figure 7-24 obtained for the same operating conditions. Due to the large ripple in the capacitor voltages, the line current waveforms are also distorted with significant low frequency harmonic content as show in Figure 7-23 (e) and Figure 7-24 (c).

In order to suppress the capacitor voltage oscillations, the 3L NPCI is tested with the hybrid modulations and the results are provided. Figure 7-25 and Figure 7-26 show the experimental and downscaled simulation results with the hybrid NTV-STV nodulation. It can be observed from Figure 7-25 (c) and Figure 7-26 (a) that, the low frequency NP voltage oscillations are eliminated even with low capacitors of 47µF. From Figure 7-25 (d) and Figure 7-26 (b), it is observed that, the THD of the line-to-line voltage is significantly increased compared to the NTV modulation alone. However, due to the elimination of low frequency NP voltage oscillations, the THD of the line current waveforms are improved compared to that of the NTV modulation as shown in Figure 7-25 (e) and Figure 7-26 (c).

Figure 7-27 and Figure 7-28 show the experimental and downscaled simulation results with the hybrid NTV-SSTV modulation. Similar to the hybrid NTV-STV modulation, the hybrid NTV-SSTV modulation is also capable of eliminating the low frequency capacitor voltage oscillations. However, there is a slight increase in the THD of the line-to-line voltage. Therefore, as discussed in Chapter-4, the hybrid NTV-SSTV can effectively eliminate the NP voltage oscitations, with minimum increase in the switching frequency. For all the operating conditions, the experimental results match with the downscale simulation results.

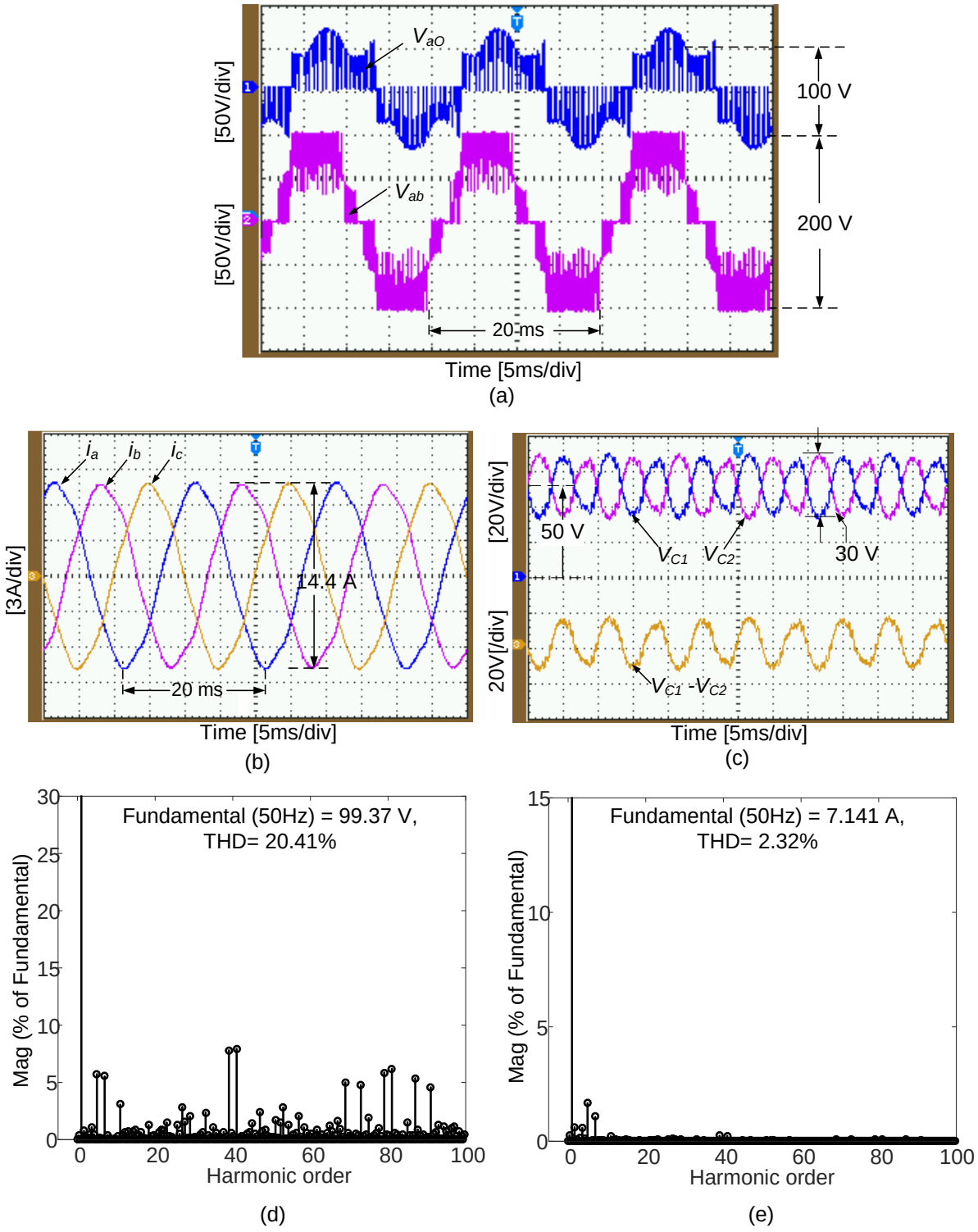
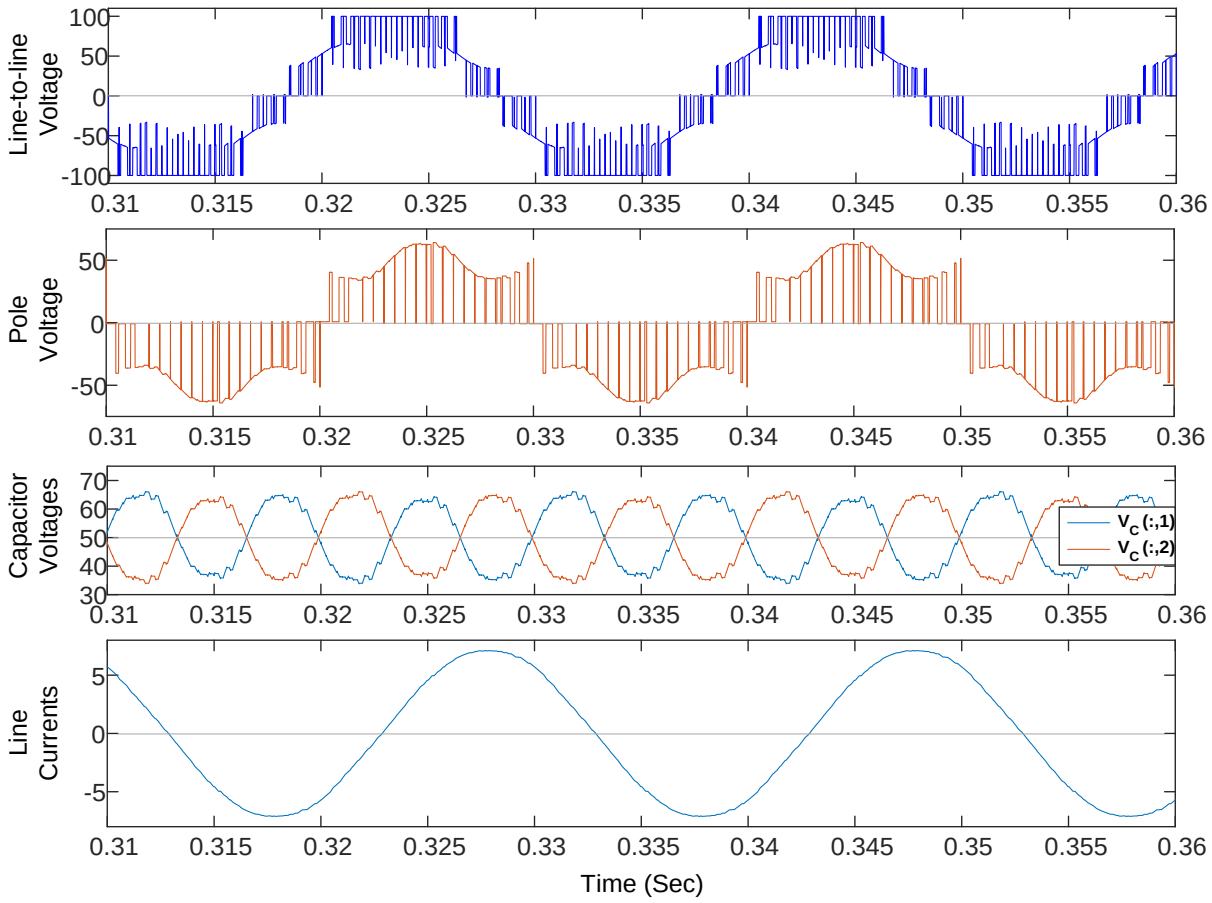


Figure 7-23 Experimental results of 3L NPCI with NTV modulation for m=1: (a) Output voltages, (b) capacitor voltages and (c) phase currents (when $V_{DC} = 100V$, load R=5 Ω and L=20 mH per phase).



(a)

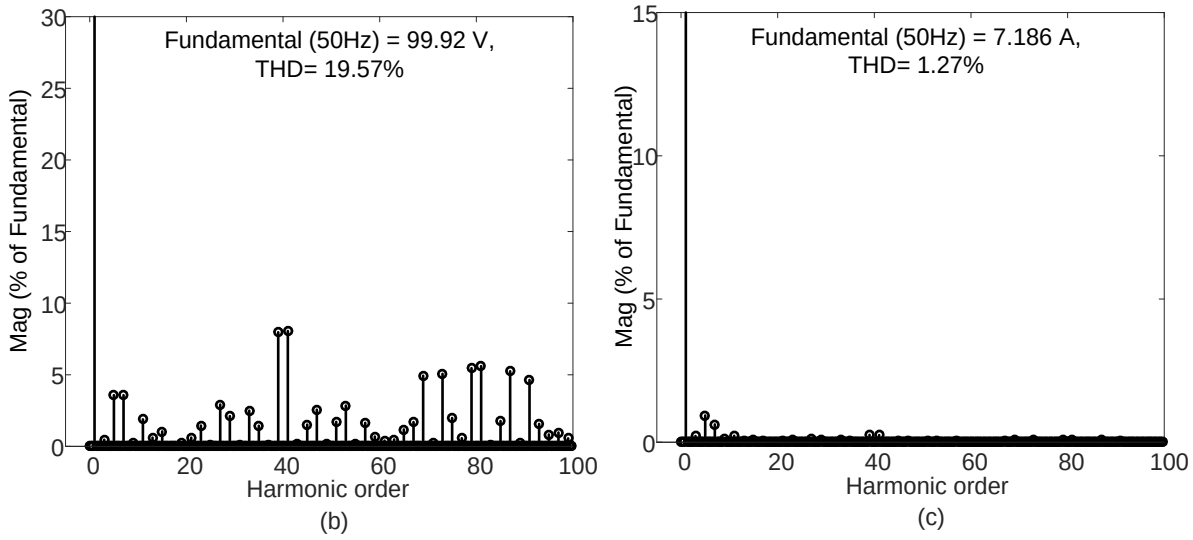


Figure 7-24 Simulation Results at m=1.0, C_1=C_2=1000μF, RL load=5 Ω/20 mH for NTV modulation: (a) Voltage and current waveforms; Harmonic spectrum of (b) Line-to-line voltage and (c) Line current.

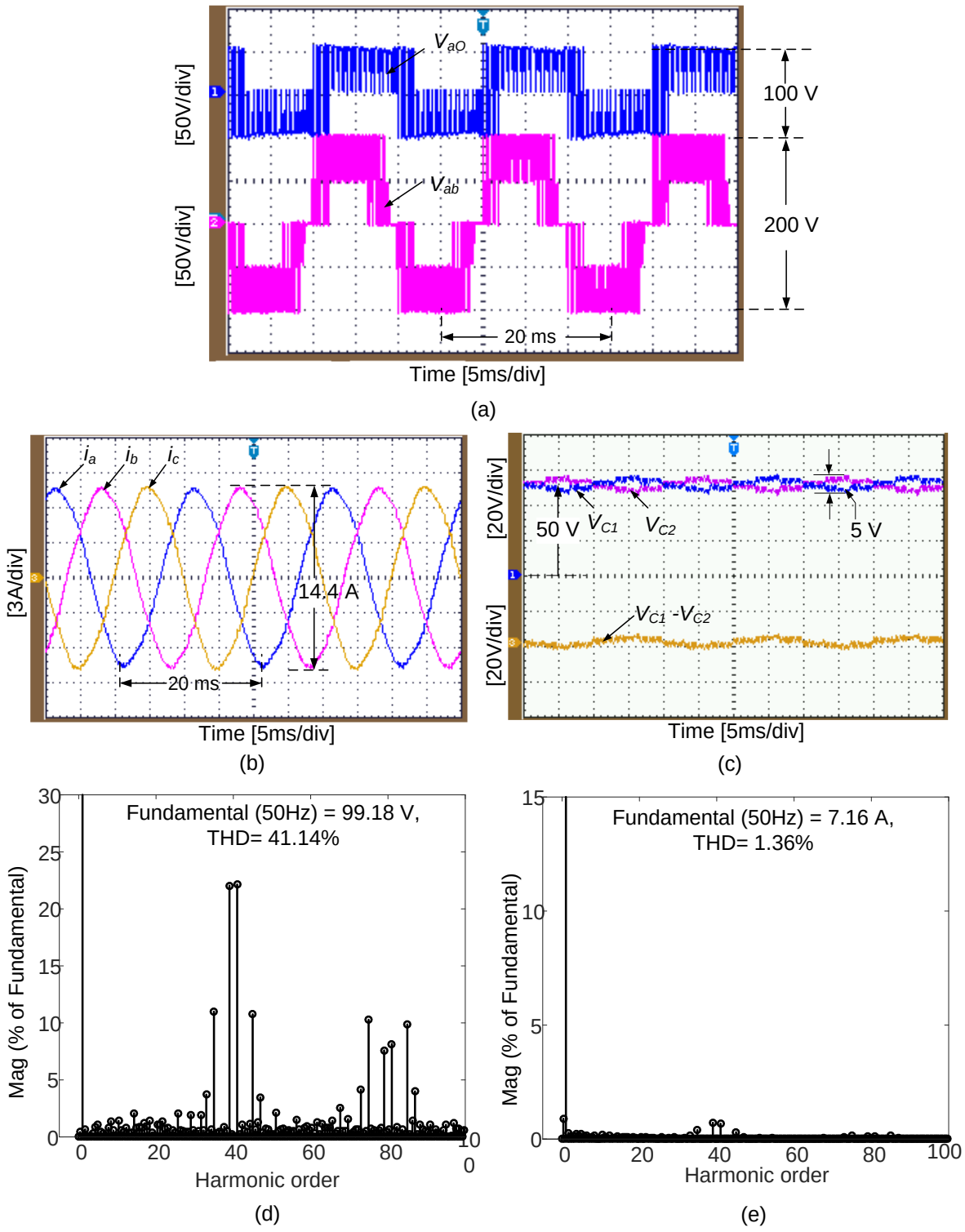


Figure 7-25 Experimental results of 3L NPCI with hybrid NTV-STV modulation for m=1: (a) Output voltages, (b) capacitor voltages and (c) phase currents (when $V_{DC}=100V$, load R=5 Ω and L=20 mH per phase).

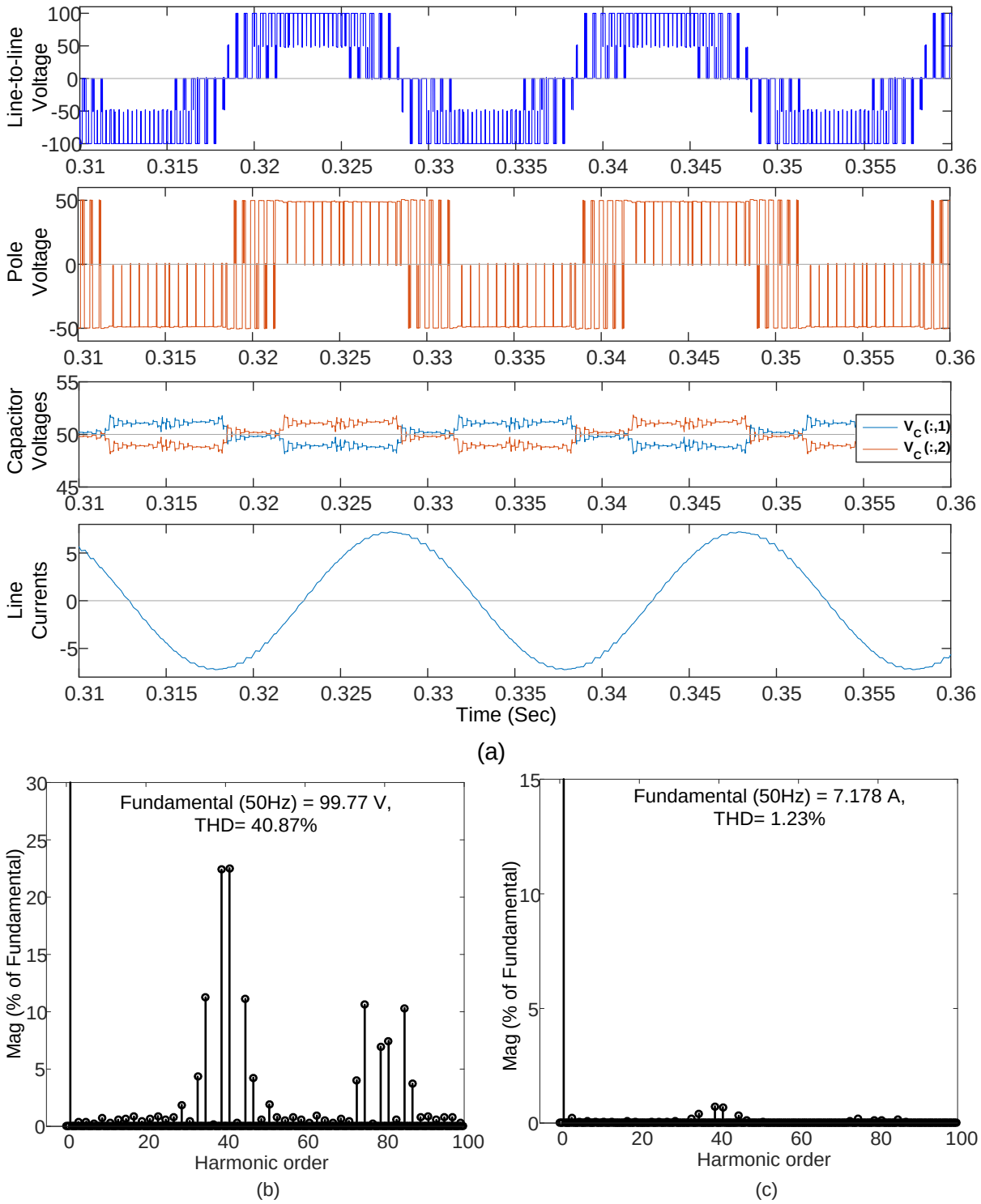


Figure 7-26 Simulation Results at m=1.0, C_1=C_2=1000μF, RL load=5 Ω/20 mH for hybrid NTV-STV modulation: (a) Voltage and current waveforms; Harmonic spectrum of (b) Line-to-line voltage and (c) Line current.

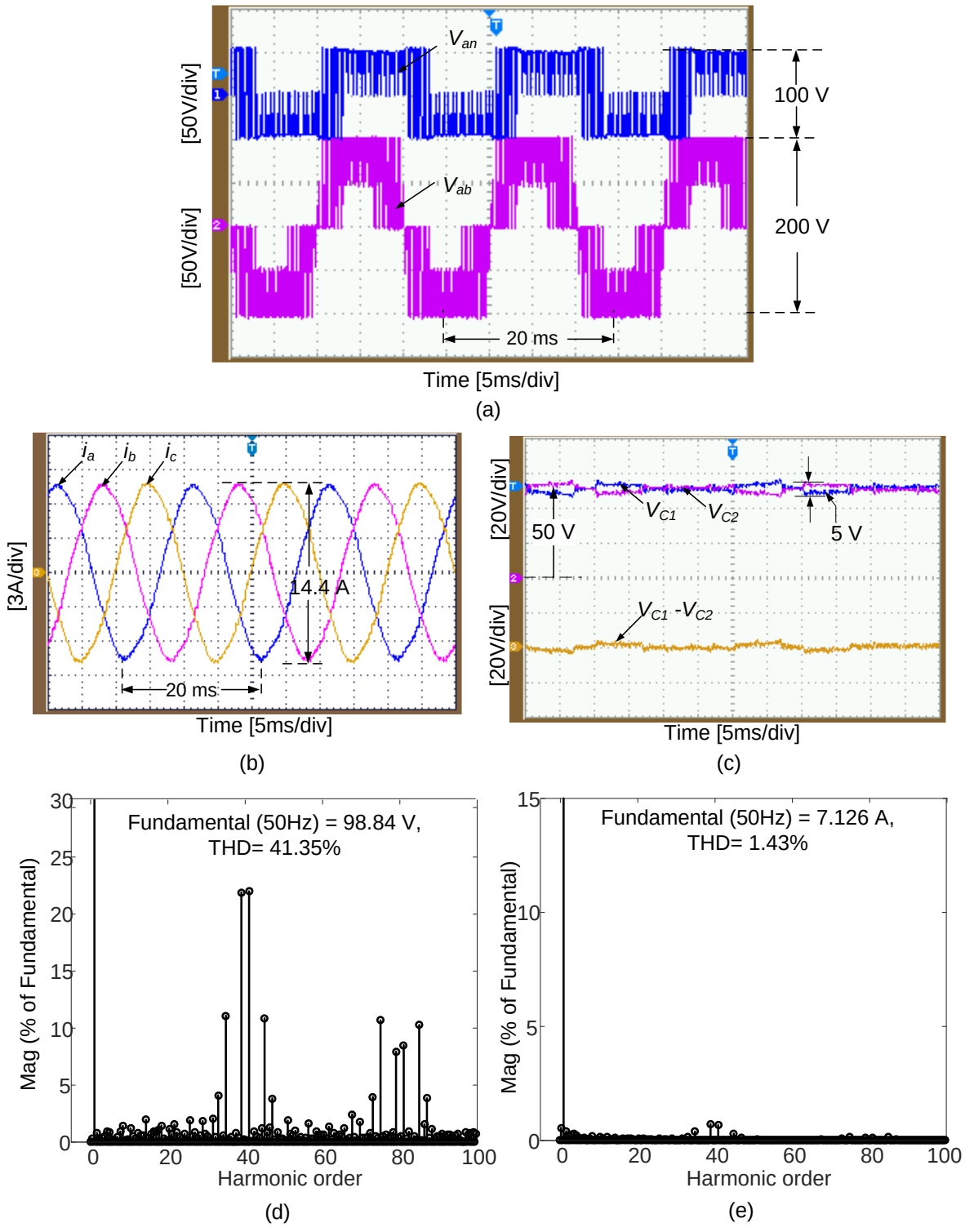
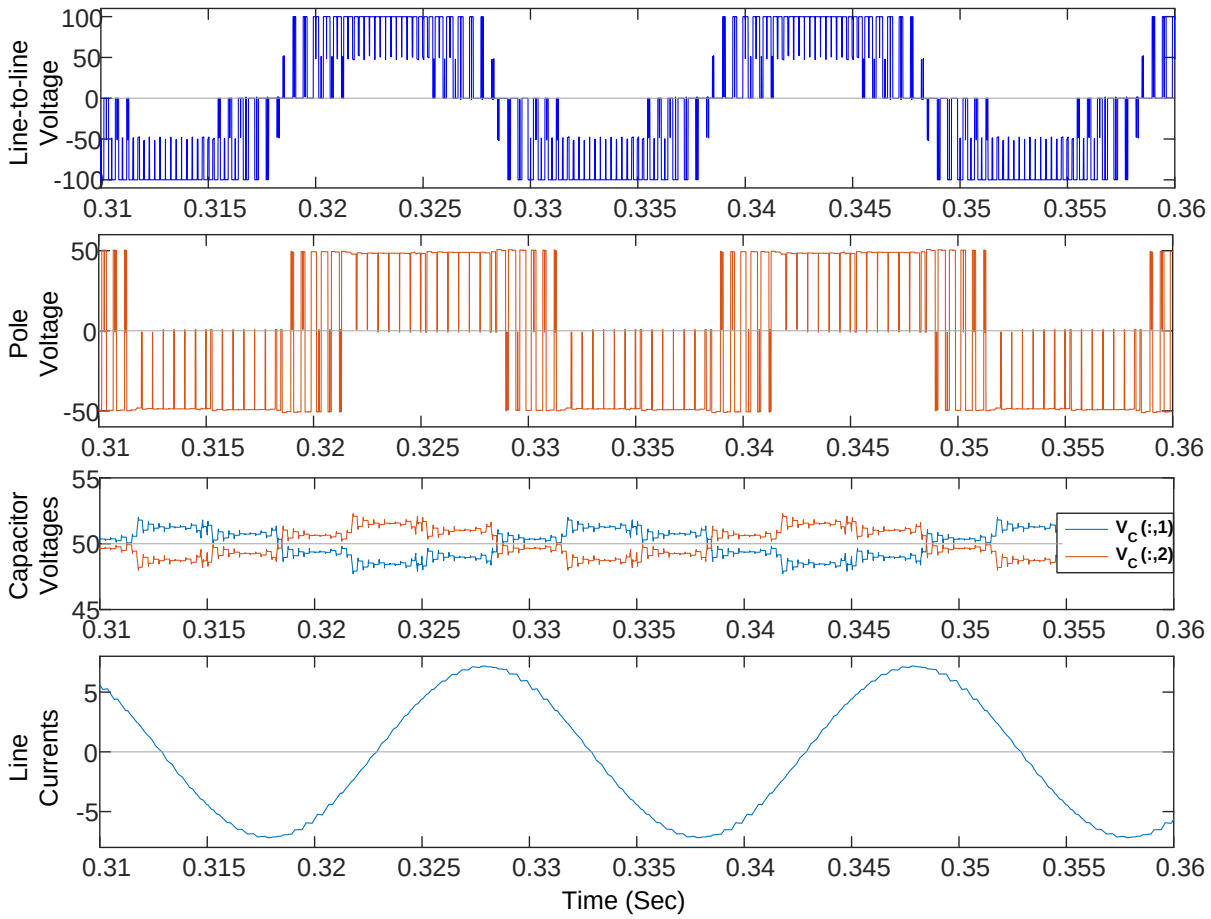


Figure 7-27 Experimental results of 3L NPCI with hybrid NTV-SSTV modulation *for m=1*: (a) Output voltages, (b) phase currents capacitor and (c) voltages (when, load R=5 Ω and L=20 mH per phase).



(a)

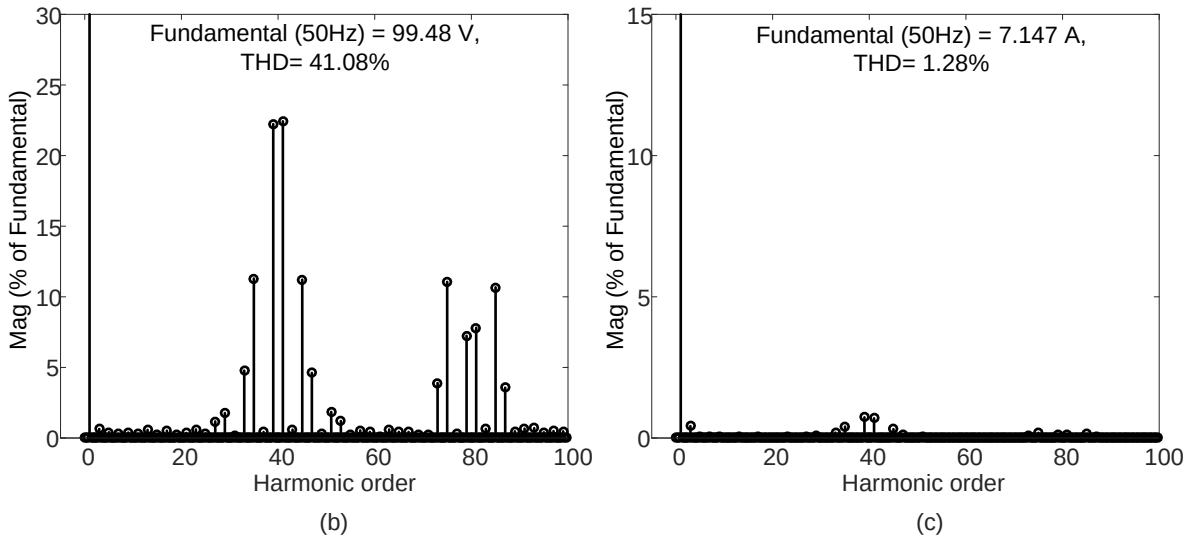


Figure 7-28 Simulation Results at *m=1.0, C_1=C_2=1000μF*, RL load=5 Ω/20 mH for hybrid NTV-SSTV modulation: (a) Voltage and current waveforms; Harmonic spectrum of (b) Line-to-line voltage and (c) Line current.

Figure 7-29 (a) and (b) show capacitor voltages waveforms for 3L NPCI for NTV and STV modulation algorithms respectively. The capacitor initial voltages are kept as V_{C1}=75V and V_{C2} =25V. The perturbation-based voltage balanced control discussed in section 4.6 is used to

compensate the initial capacitor voltage imbalance. Both the NTV and STV modulations are capable of maintaining a desired mean value of 50V, however, only STV can suppress low frequency NP voltage oscillations.

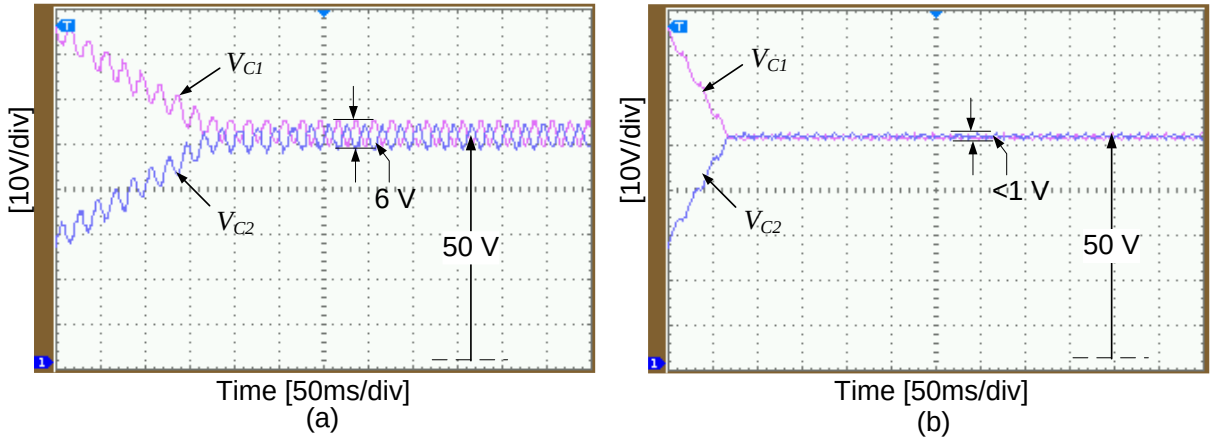


Figure 7-29 Experimental results of capacitor voltages under m=0.98, C_1=C_2=1000μF and RL load =5Ω/20mH for (a) NTV, (b) STV.

The performance of 3L NPCI at m=1 with various hybrid modulation methods are summarized in Table 7-2.

Table 7-2 Comparison of Experimental and downscaled simulation results of 3L NPCI for NTV and hybrid modulation methods

Performance Parameter		Modulation index (m)		
		1.0		
		NTV	NTV-STV	NTV-SSTV
Line-to-line Voltage (V) (Peak)	Experimental	99.37	99.18	98.84
	Simulation	99.92	99.77	99.48
% THD of Line-to-line Voltage	Experimental	20.41	41.14	41.35
	Simulation	19.57	40.87	41.08
Line Current (A) (peak)	Experimental	7.141	7.16	7.126
	Simulation	7.186	7.178	7.147
% THD of Line Current	Experimental	1.42	1.36	1.43
	Simulation	1.27	1.23	1.28
Capacitor Voltage Ripple (V)	Experimental	32	5	5
	Simulation	30	4	4

7.4 Performance Investigation Of Hybrid 2/3L NPCI

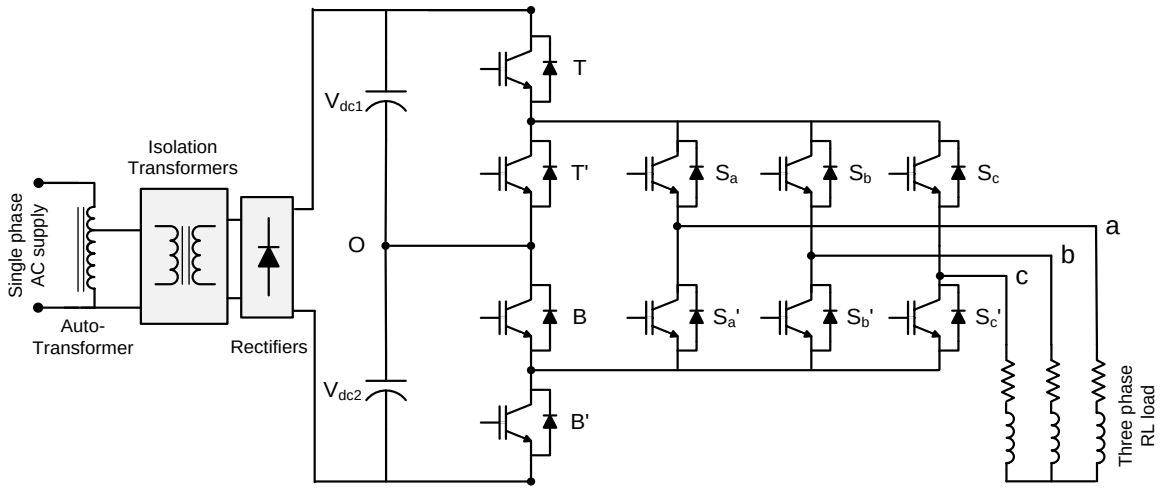


Figure 7-30 Experimental setup of three-phase hybrid 2/3L NPCI with RL load.

The experimental validations of a scale down prototype hybrid 2/3L NPCI shown in Figure 7-30 are performed with various modulation algorithms discussed in chapter-5. A DC link voltage of 100V, split capacitors of 2200µF capacitance each, a three phase Wye connected RL load of 10 Ω/15 mH per phase are used for the experimental setup. RT-Lab controller was used to generate firing pluses with switching frequency of 2 kHz for implementing the proposed modulation strategies (1) VV-based modulation and (2) STV-based modulation. Down scale simulation results with the experimental setup parameters are also performed for the validation. Since the performance of the hybrid 2/3L NPCI for lower modulation indices (m<0.5) is similar to the 3L VSI discussed previously, this operation is not considered here.

7.4.1 Performance of hybrid 2/3L NPCI with VV-based modulation:

Figure 7-31 through Figure 7-34 Figure 7-33show the various experimental and downscaled simulation results of hybrid 2/3L NPCI inverter operated with VV-based modulation method. Two different modulation indices m=0.98 and m=0.65 are considered for experimental testing.

Figure 7-31 (a-c) and Figure 7-32 (a) show experimental and down scaled simulation results at m=0.98 respectively. It can be observed that, the capacitor voltages are balanced with minimum voltage ripple. As discussed in Section 5.2.1, this is due to the minimum duration of operation of small vectors which causes the capacitor voltage ripple. From the SVD of the hybrid 2/3L NPCI (refer Figure 5-3), it evident that, when the modulation index m=0.98, the duration of V_{ref} in triangle T_2 neglectable. The VV-based modulation uses 4 switching states only when the reference vector V_{ref} is located in T_2. The switching signals for the various devices are shown in Figure 7-31 (b). the switches (T,T`) and (B, B`) has the higher switching frequency compared to the phase switch S_a. The harmonic spectra plotted for the experientially obtained line-to-line

voltage and current waveforms are presented in Figure 7-31 (d) and (e) respectively. While the harmonic spectra of simulation waveforms are presented in Figure 7-32 (b) and (c). It can be observed that the experimental and downscaled simulation results match closely.

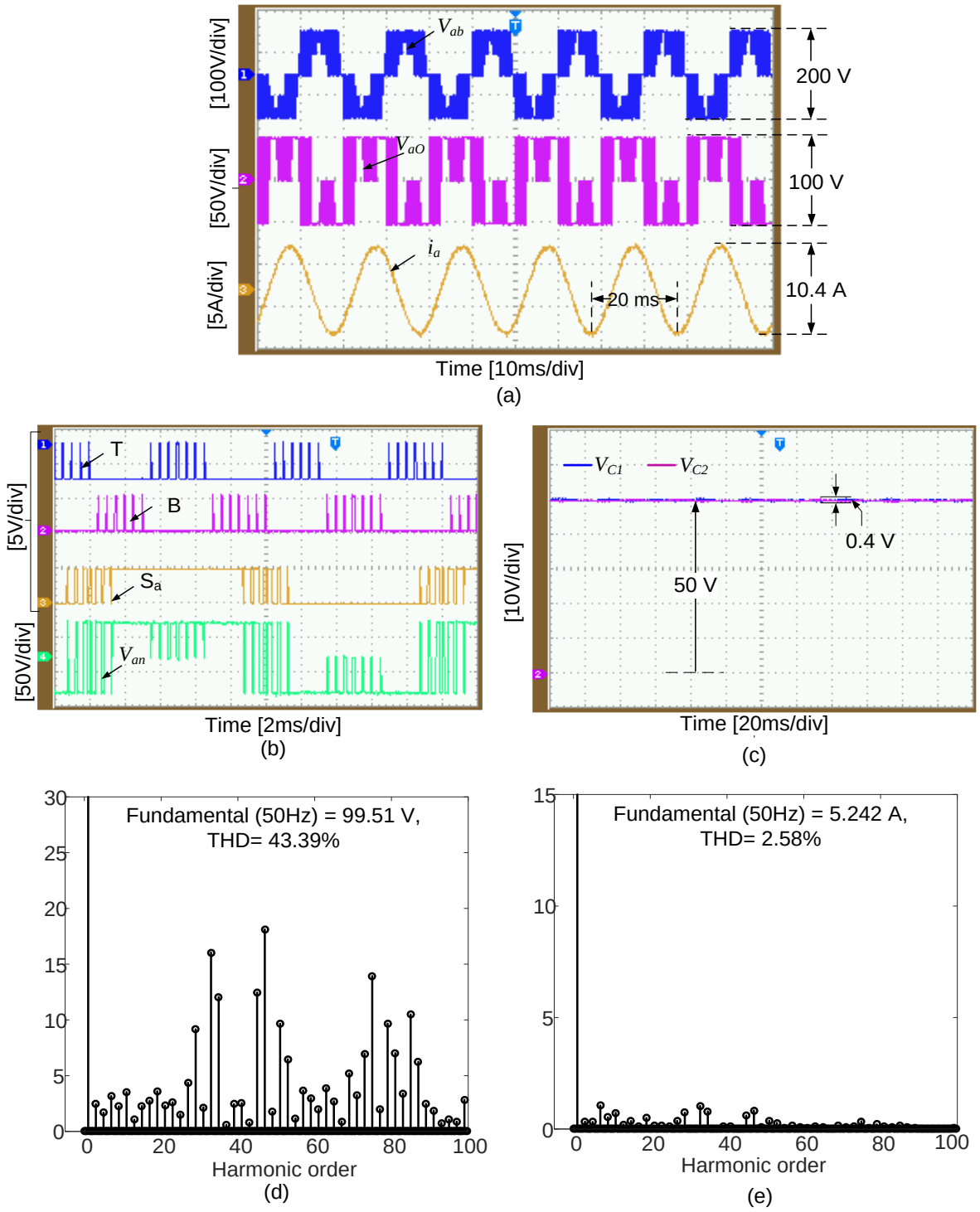


Figure 7-31 Experimental results of hybrid 2/3L NPCI with VV-based modulation for m=0.98: (a) AC side waveforms, (b) Switching signals, (c) capacitor voltages; harmonic spectrum of (d) line-to-line voltage and (e) current.

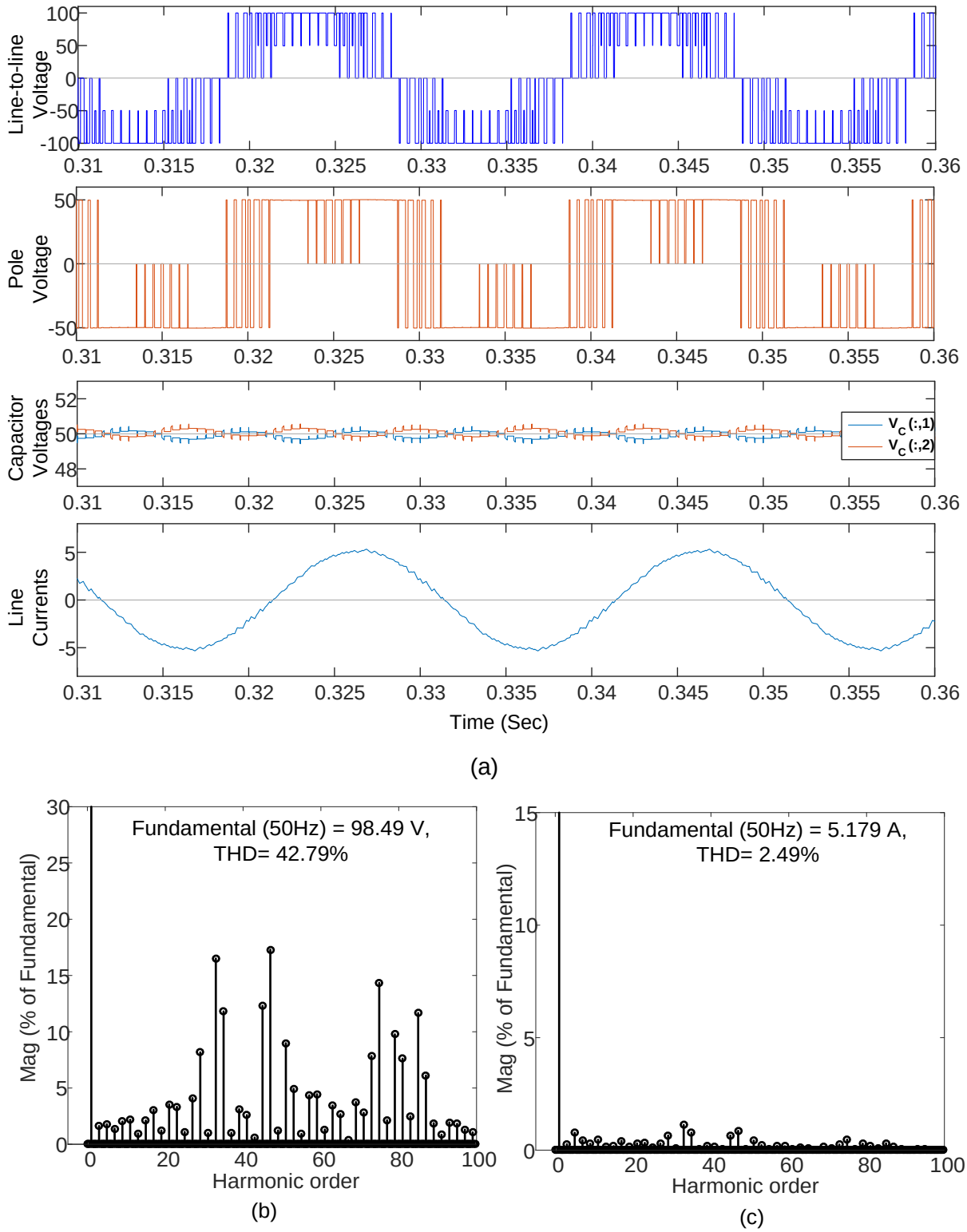


Figure 7-32 Simulation results of hybrid 2/3L NPCI with VV-based modulation at *m=0.98* (a) Voltage and current waveforms; Harmonic spectrum of (b) Line-to-line voltage and (c) Line current.

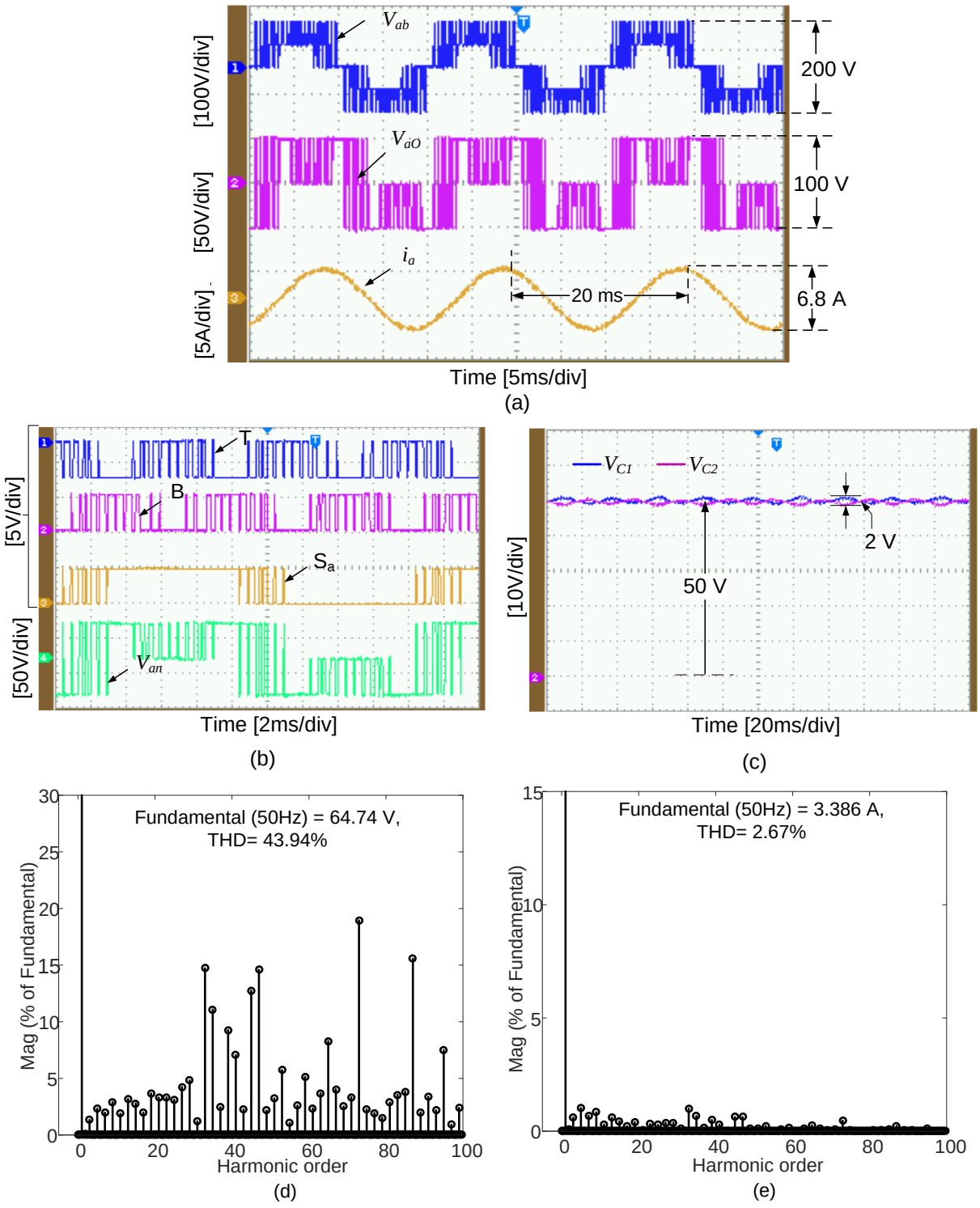
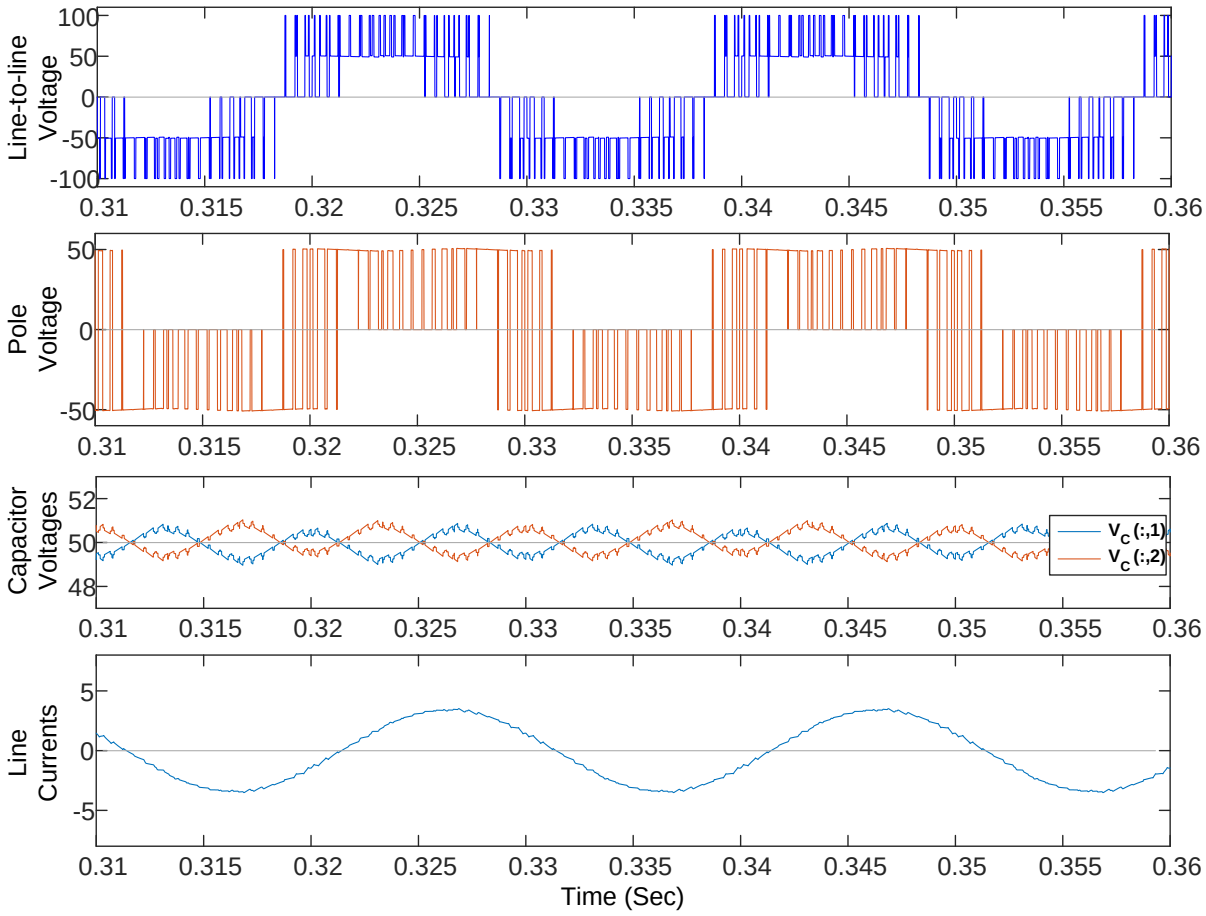


Figure 7-33 Experimental results of hybrid 2/3L NPCI with VV-based modulation for m=0.65 (a) AC side waveforms, (b) Switching signals, (c) capacitor voltages; harmonic spectrum of (d) line-to-line voltage and (e) current.



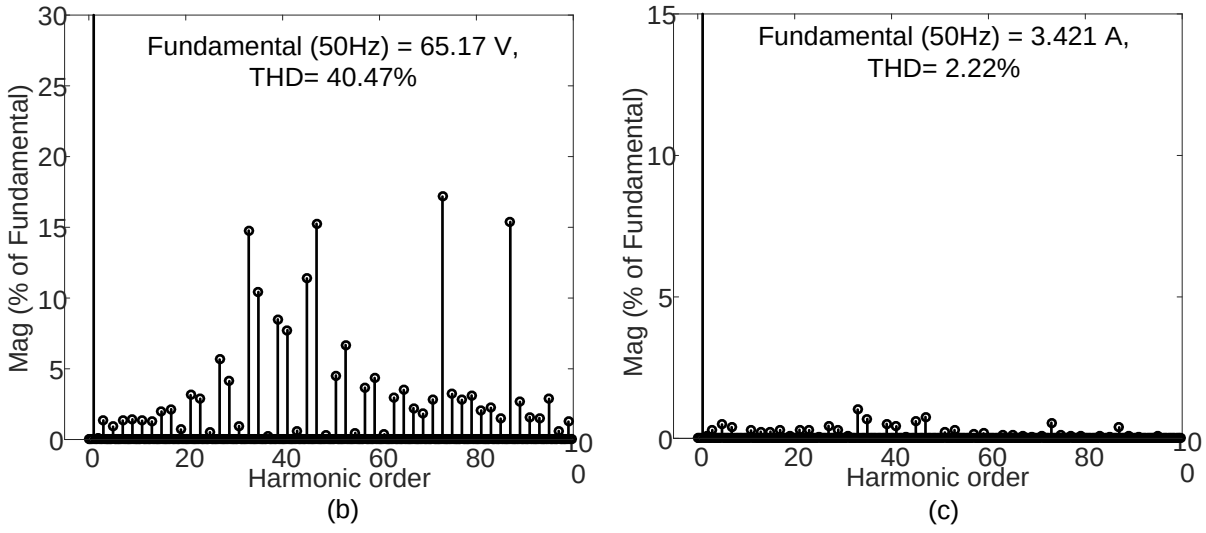


Figure 7-34 Simulation results of hybrid 2/3L NPCI with VV-based modulation at m=0.65 (a) Voltage and current waveforms; Harmonic spectrum of (b) Line-to-line voltage and (c) Line current.

Figure 7-33 (a-c) and Figure 7-34 (a) show experimental and down scaled simulation results at m=0.65 respectively. When the modulation index (*m*) decreases, the duration of reference vector V_{ref} in sub-triangle T_2 increases. As a result, there is an increase in the switching

frequency. This is evident from the switching signals shown in Figure 7-33(b) for m=*0.65*. The shape if the pole voltage (V_{a0}) and line voltages (V_{ab}) for m=0.65 remain unchanged as that of m=0.98 since the reference vector V_{ref} remain in the same sub-triangle regions. Finally, the capacitors experience increased voltage ripple as shown in Figure 7-33(c) due to the increased participation of the small vector in the switching cycle. Similar performance is evident from the down scaled simulation results shown in Figure 7-34. Therefore, it seems that proposed VV-based modulation discussed in Section 5.2 for hybrid 2/3L NPCI gives satisfactory experimental results.

7.4.2 Performance of Hybrid 2/3L NPCI with STV-based Modulation:

Figure 7-35 through Figure 7-38 show the various experimental and downscaled simulation results of hybrid 2/3L NPCI inverter operated with STV-based modulation method. The modulation indices m=0.98 and m=0.65 are considered for experimental testing. Some of the observations are discussed below.

Figure 7-35 (a-c) and Figure 7-36 (a) show experimental and down scaled simulation results at m=0.98 respectively. As discussed in section 5.2 and 5.3, for the higher modulation indices, the performance of STV-based modulation is almost similar to that of the VV-based modulation method. This is evident from the experimental and downscaled simulation results of STV-based modulation method.

Figure 7-37(a) and Figure 7-38 (a) show the experimental and downscaled simulation results obtained for m=0.65 for the same loading conditions discussed above. It is cleared that, the shape of the pole voltage (V_{a0}) and line voltages (V_{ab}) are significantly different as compared to that of the higher modulation indices. This is due to the selection of different sub-triangle regions U_1 and U_4 by the reference vector V_{ref} for the modulation index range $(m<2/3)$ as discussed in Section 5.2.2. A reduction in the switching frequency of hybrid 2/3L NPCI with STV-based modulation for lower modulation indices (m=0.65) is evident from Figure 7-37(b). The harmonic spectra plotted for the experientially obtained line-to-line voltage and current waveforms are presented in Figure 7-37(d) and (e) respectively. While the harmonic spectra of simulation waveforms are presented in Figure 7-38 (b) and (c).

Clearly, the experimental results under different operating conditions are in good agreement with the downscaled simulation results of the hybrid 2/3L NPCI with VV and STV-based modulation methods.

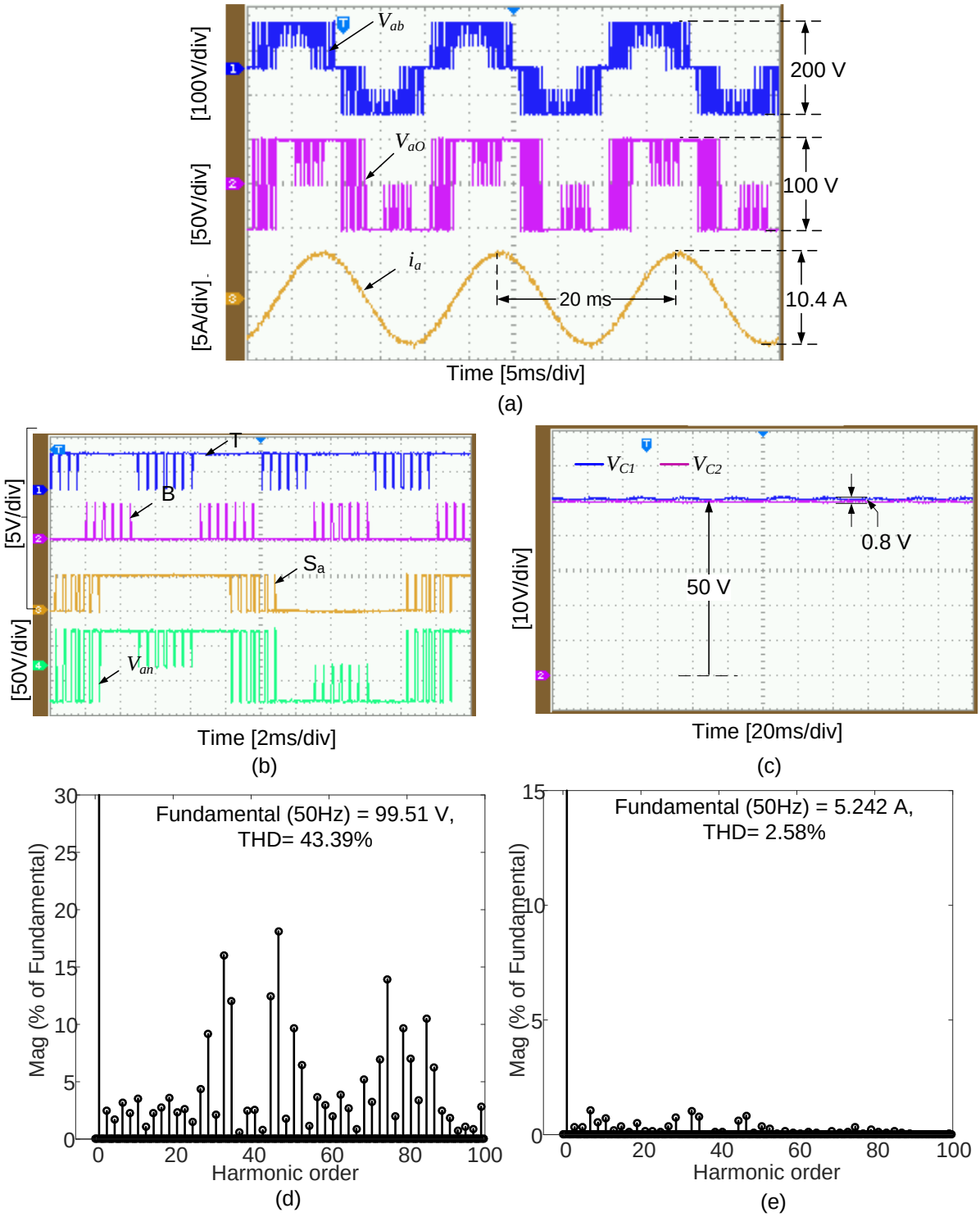
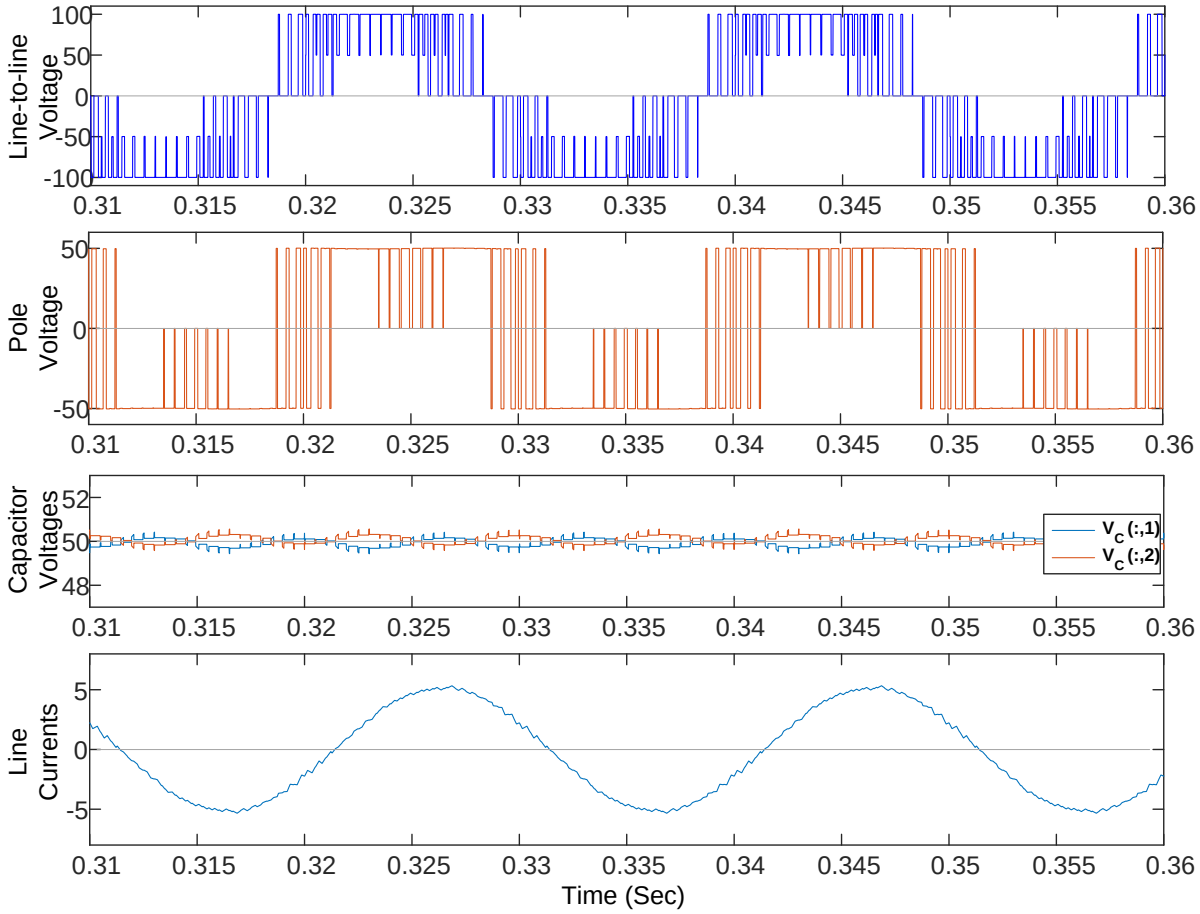


Figure 7-35 Experimental results of hybrid 2/3L NPCI with STV-based modulation for m=0.98: (a) AC side waveforms, (b) Switching signals, (c) capacitor voltages; harmonic spectrum of (d) line-to-line voltage and (e) current.



(a)

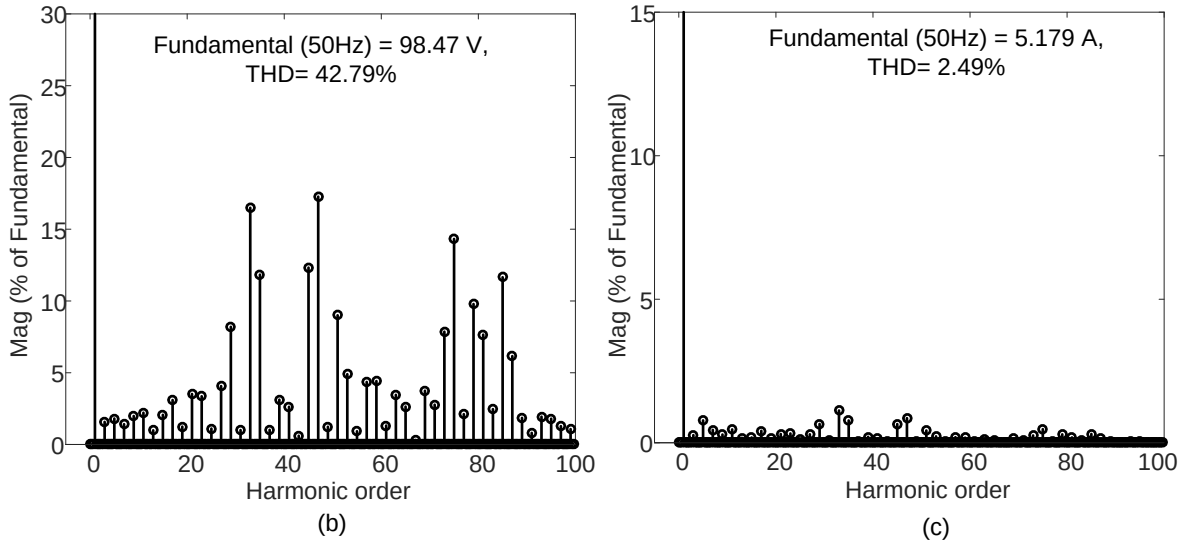


Figure 7-36 Simulation results of hybrid 2/3L NPCI with STV-based modulation at m=0.98 (a) Voltage and current waveforms; Harmonic spectrum of (b) Line-to-line voltage and (c) Line current.

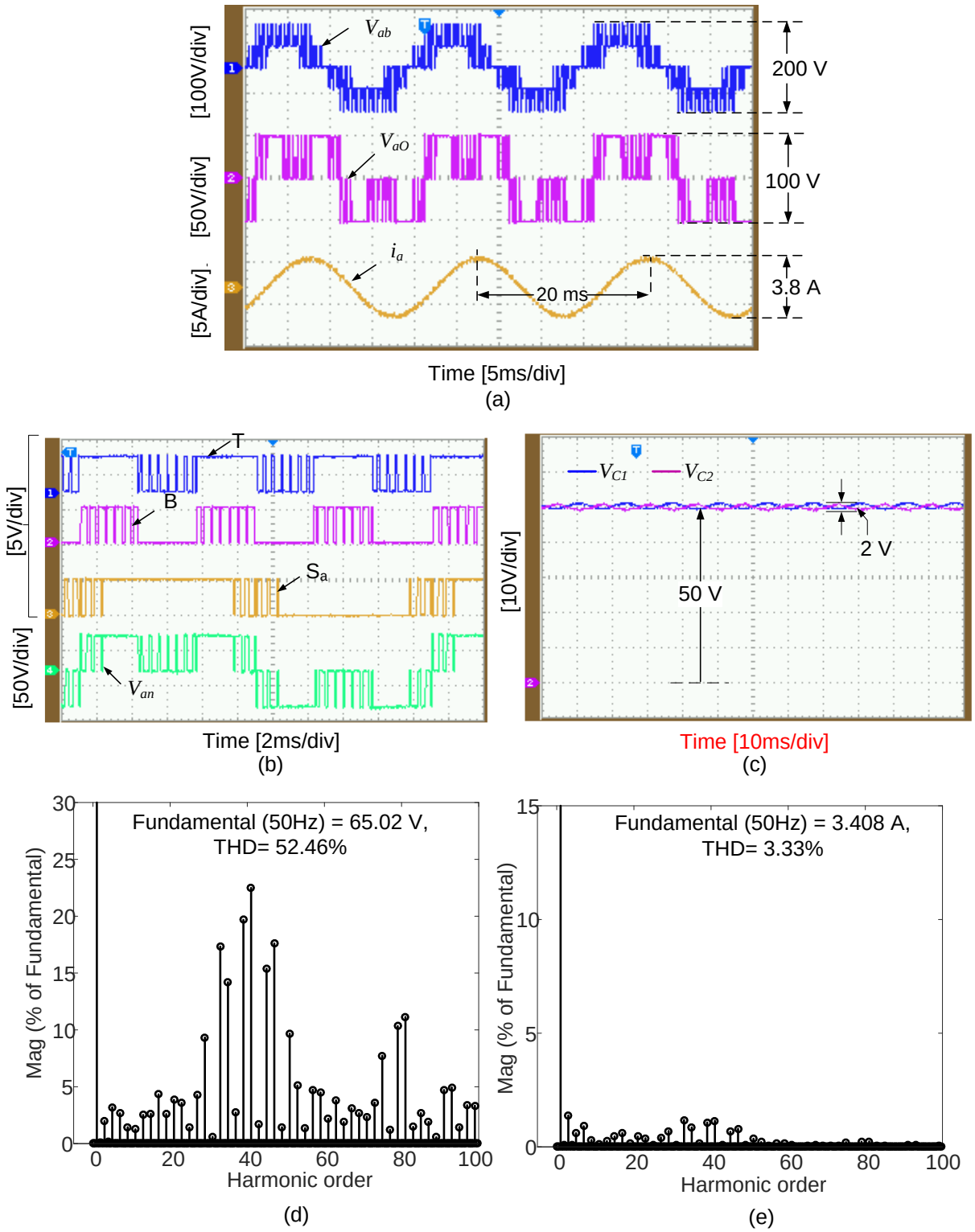


Figure 7-37 Experimental results of hybrid 2/3L NPCI with STV-based modulation for m=0.65 (a) AC side waveforms, (b) Switching signals, (c) capacitor voltages; harmonic spectrum of (d) line-to-line voltage and (e) current.

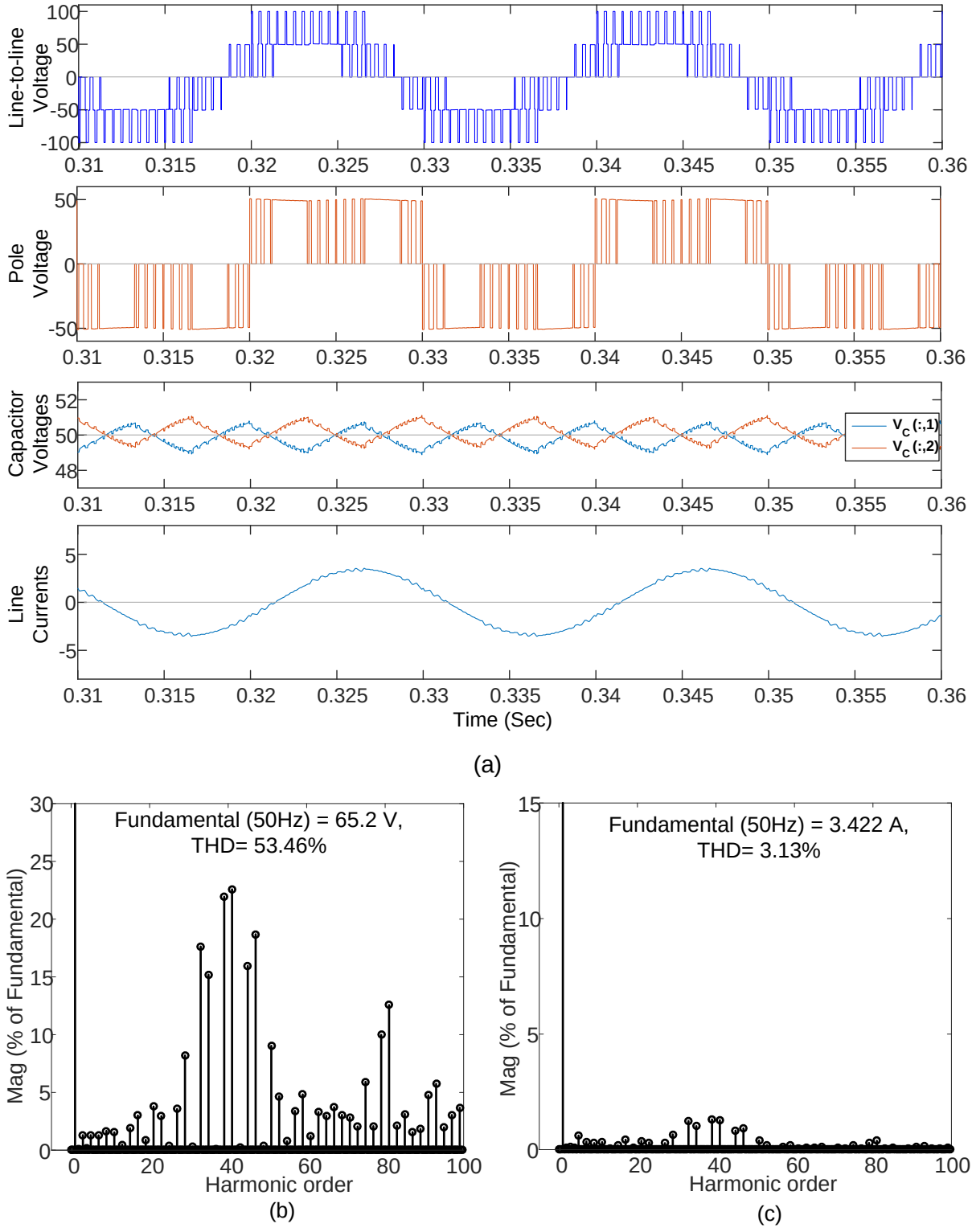


Figure 7-38 Simulation results of hybrid 2/3L NPCI with STV-based modulation at m=0.65 (a) Voltage and current waveforms; Harmonic spectrum of (b) Line-to-line voltage and (c) Line current.

The performance of the hybrid 2/3L NPCI with VV and STV-based modulation methods for two modulation indices are summarized in Table 7-3.

Table 7-3 Comparison of Experimental and downscaled simulation results of hybrid 2/3L NPCI for VV and STV-based modulation methods

Performance Parameter		Modulation index (m)			
		0.98		0.65	
		VV	STV	VV	STV
Line-to-line Voltage (V) (Peak)	Experimental	99.51	99.51	64.74	65.02
	Simulation	98.49	98.47	65.17	65.2
% THD of Line-to-line Voltage	Experimental	43.39	43.39	43.94	52.46
	Simulation	42.79	42.79	40.47	53.46
Line Current (A) (peak)	Experimental	5.242	5.242	3.386	3.408
	Simulation	5.179	5.179	3.421	3.422
% THD of Line Current	Experimental	2.58	2.58	2.67	3.33
	Simulation	2.49	2.49	2.22	3.13
Capacitor Voltage Ripple (V)	Experimental	<0.5	0.8	2	<2
	Simulation	0.4	0.7	1.8	1.8

7.4.3 Performance of Hybrid 2/3L NPCI with Unequal DC Capacitor Voltages:

Experimental results of hybrid 2/3L NPCI at *m=0.98* (a) AC side waveforms, (b) Switching signals of hybrid 2/3L NPCI, (c) Voltage and (d) current harmonic spectrum, (when $V_{C1} = 60V$ & $V_{C2} = 40V$; load R=10 Ω and L=15 mH per phase).

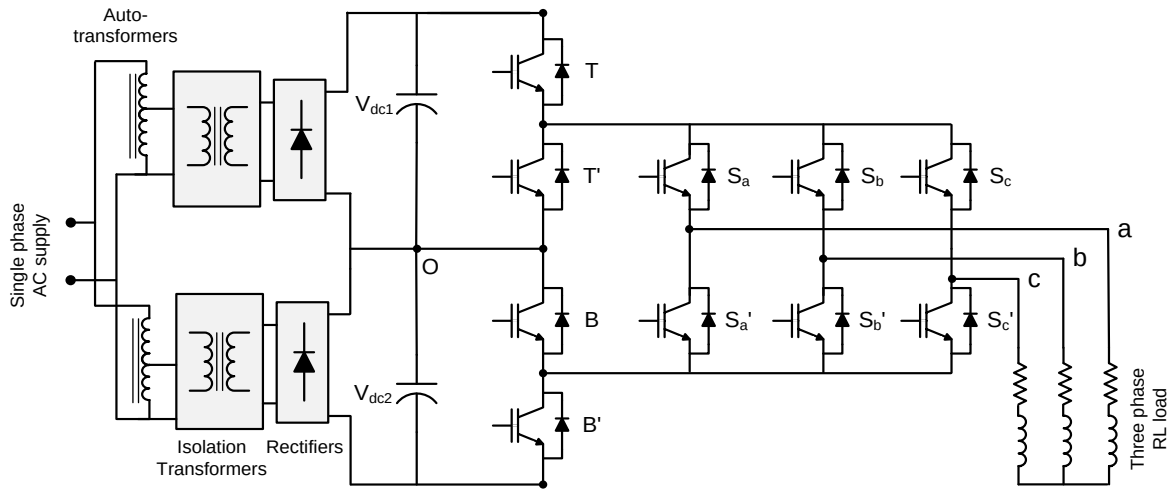


Figure 7-39 Experimental setup of unequal DC source excite three-phase hybrid 2/3L NPCI with RL load.

Figure 7-40 through Figure 7-47 show the various experimental and down scaled simulation results of hybrid 2/3L NPCI inverter operated under unequal voltages across each capacitor. The virtual vector modulation discussed in section 5.6 is used to generate the switching pulses of the VSI for two different modulation indices m=0.98 and m=0.65 respectively. A load of R=10Ω and L=15 mH per phase was used to carry out the experimentation. Some of the observations are discussed below.

Case-I: $V_{C1} = 60V$ an $V_{C2} = 40V$

Figure 7-40 (a) and Figure 7-42 (a) show the ac side waveforms under unbalanced voltages given by $V_{C1} = 60V$ and $V_{C2} = 40V$. The unbalance is evident from the pole voltage V_{aO} measured across the ac terminal and dc side midpoint O. The peak in positive side measures 60V while the peak in negative side measures 40V. However, the line voltage V_{ab} shown in the first trace of Figure 7-40 (a) and Figure 7-42 (a) is symmetrical about the time axis resulting in zero DC component. Similarly, the line current is also sinusoidal with minimum distortion.

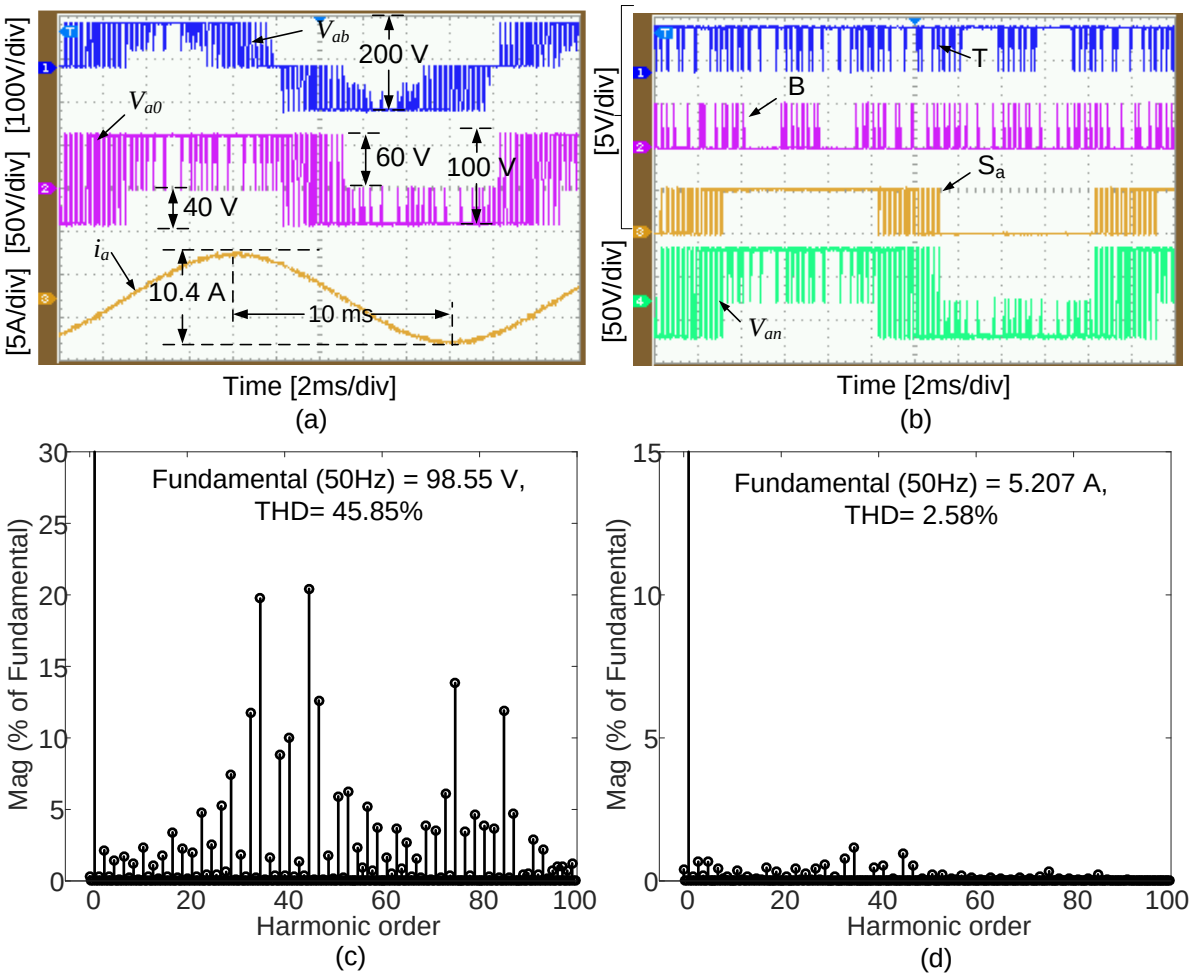
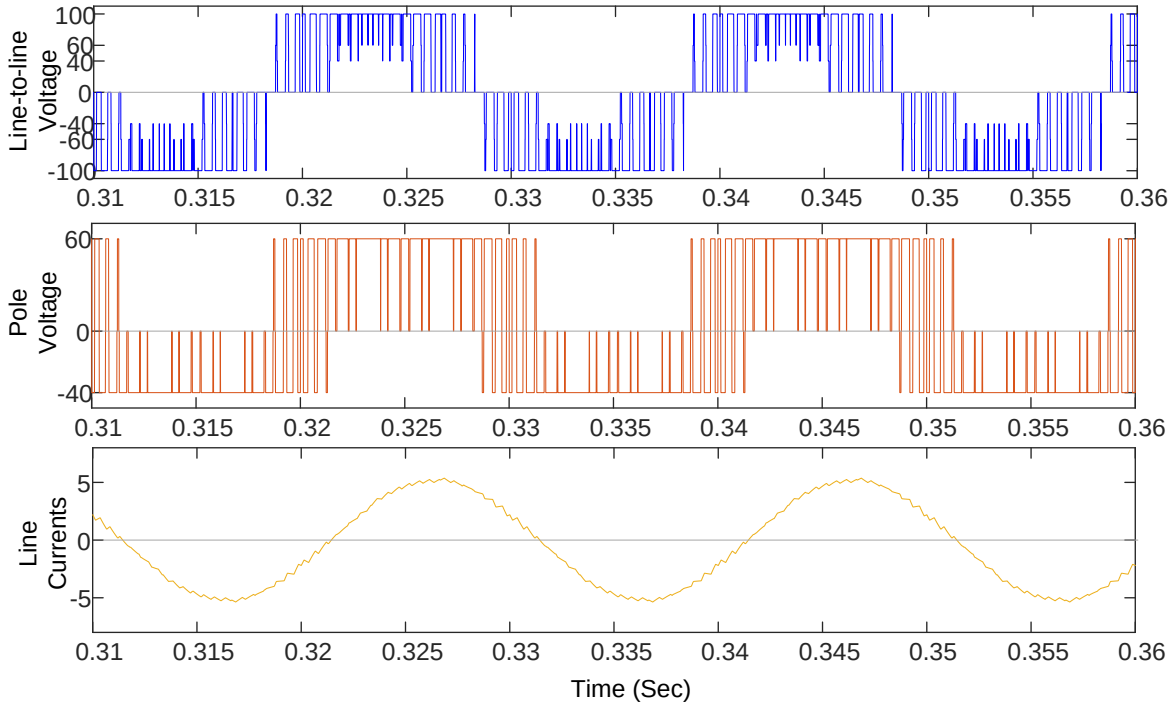


Figure 7-40 Experimental results of at m=0.98 (a) AC side waveforms, (b) Switching signals, (c) Voltage and (d) current harmonic spectrum, (when $V_{c1} = 60V$ & $V_{c2} = 40V$)



(a)

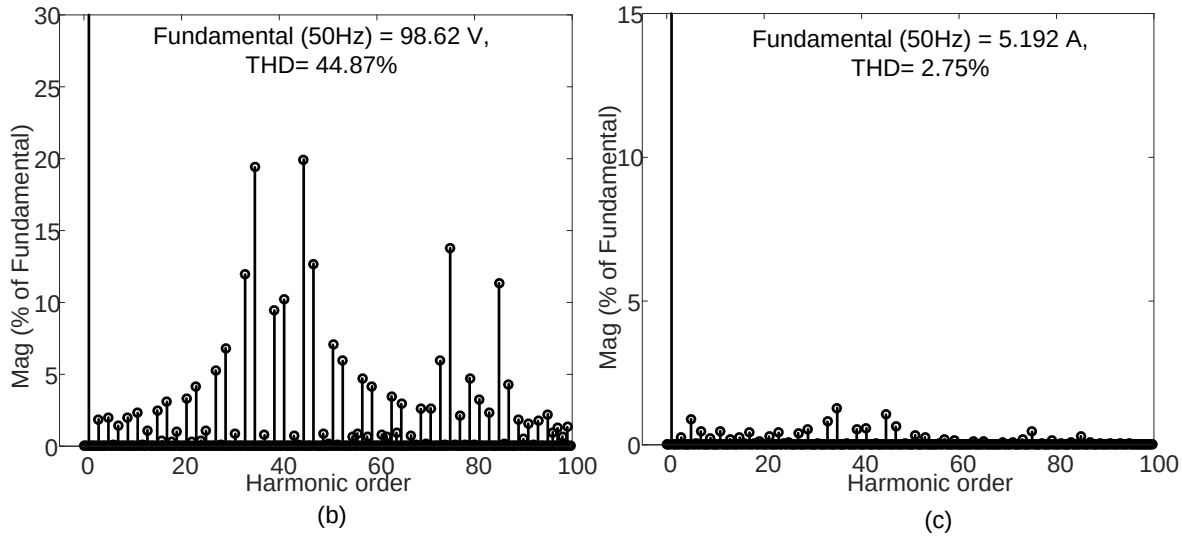


Figure 7-41 Simulation results of hybrid 2/3L NPCI at m=0.98 (a) Voltage and current waveforms, (b) Voltage and (c) current harmonic spectrum, (when $V_{c1} = 60V$ & $V_{c2} = 40V$)

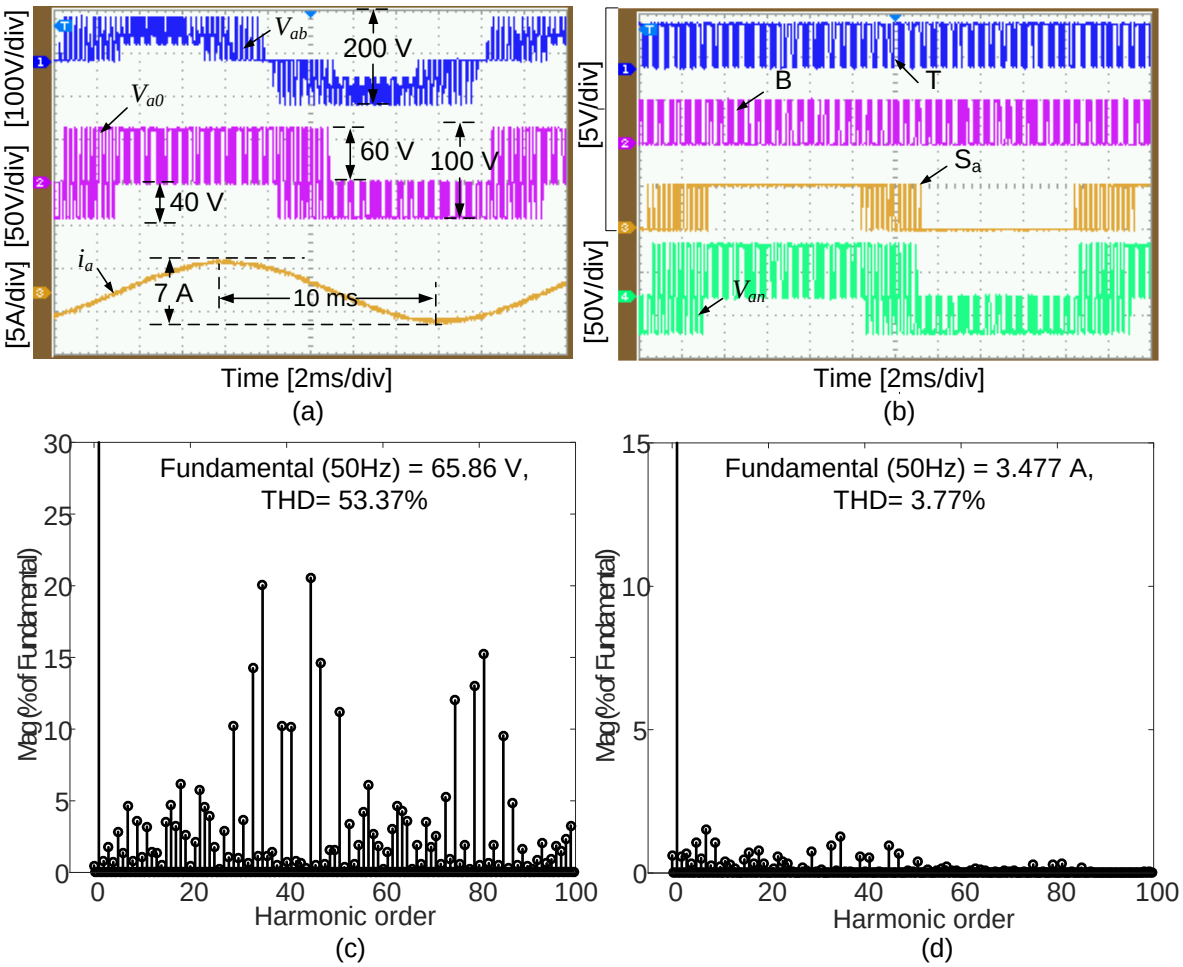


Figure 7-42 Experimental results at m=0.65 (a) AC side waveforms, (b) Switching signals, (c) Voltage and (d) current harmonic spectrum, (when $V_{c1} = 60V$ & $V_{c2} = 40V$)

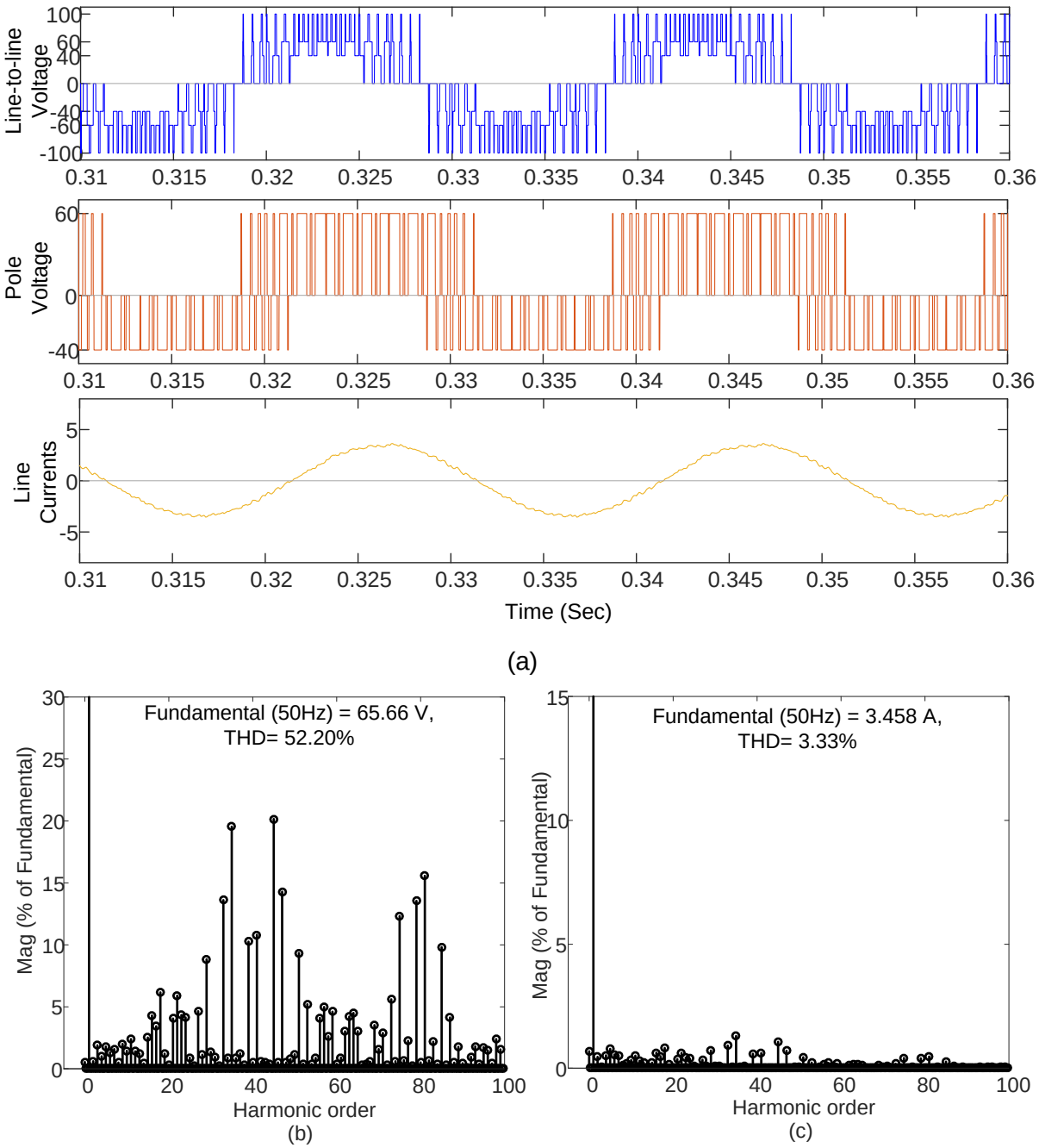


Figure 7-43 Simulation results of hybrid 2/3L NPCI at m=0.65 (a) Voltage and current waveforms, (b) Voltage and (c) current harmonic spectrum, (when $V_{c1} = 60V$ & $V_{c2} = 40V$)

Case-II: $V_{c1} = 30V$ and $V_{c2} = 70V$

Figure 7-44 (a) and Figure 7-46 (a) show the ac side waveforms under unbalanced voltages given by $V_{c1} = 30V$ and $V_{c2} = 70V$. Similar to the Case-I, the pole voltage contains the asymmetry about the time axis, however, the line voltage and line currents are balanced. It can be concluded that the proposed modulation scheme completely eliminated the effect of unbalanced DC capacitor voltages in the ac side waveforms of hybrid 2/3L NPCI.

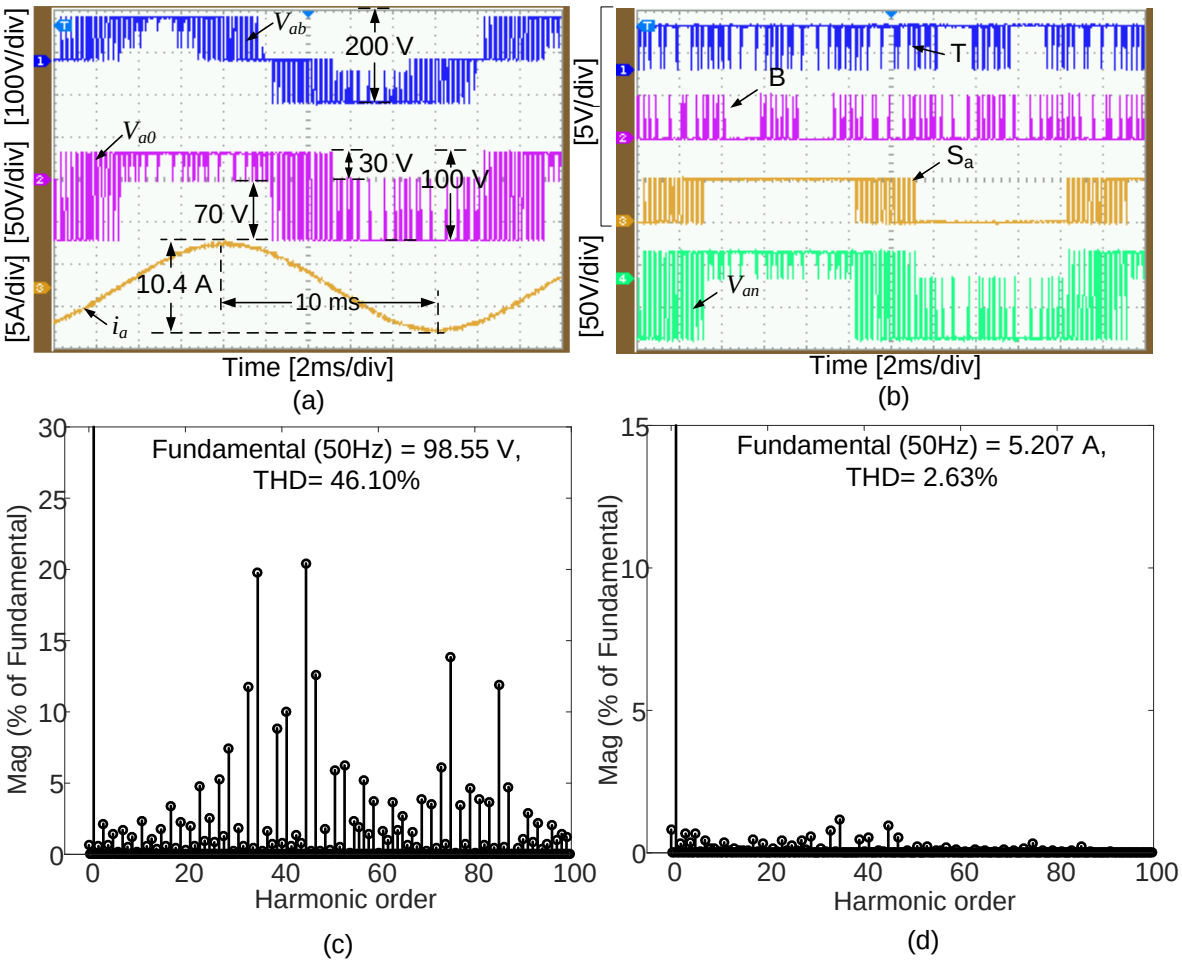
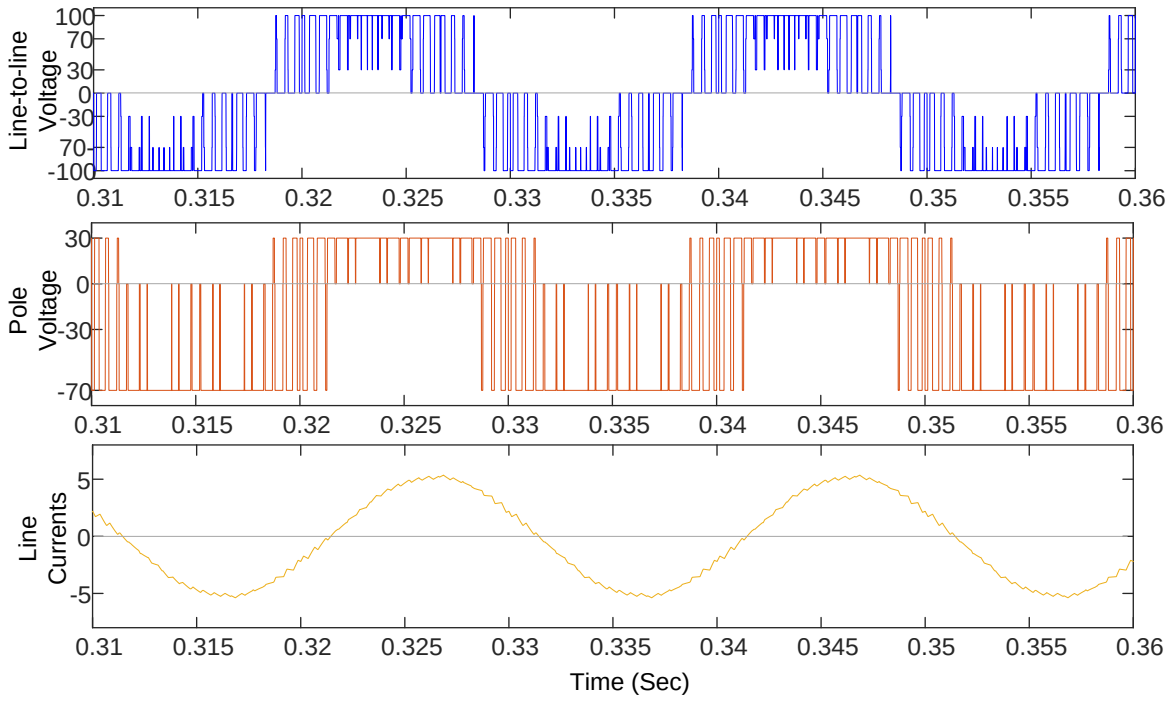


Figure 7-44 Experimental results at *m=0.98* (a) AC side waveforms, (b) Switching signals, (c) Voltage and (d) current harmonic spectrum (when $V_{c1} = 30V$ and $V_{c2} = 70V$).



(a)

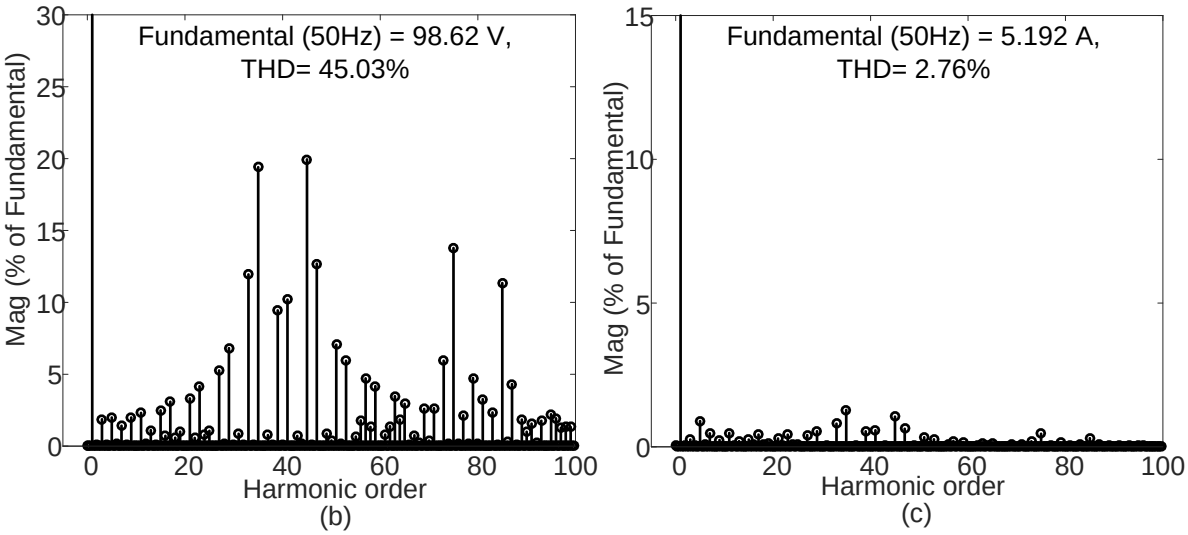


Figure 7-45 Simulation results at m=0.98 (a) AC side waveforms, (b) Switching signals, (c) Voltage and (d) current harmonic spectrum (when $V_{c1} = 30V$ and $V_{c2} = 70V$).

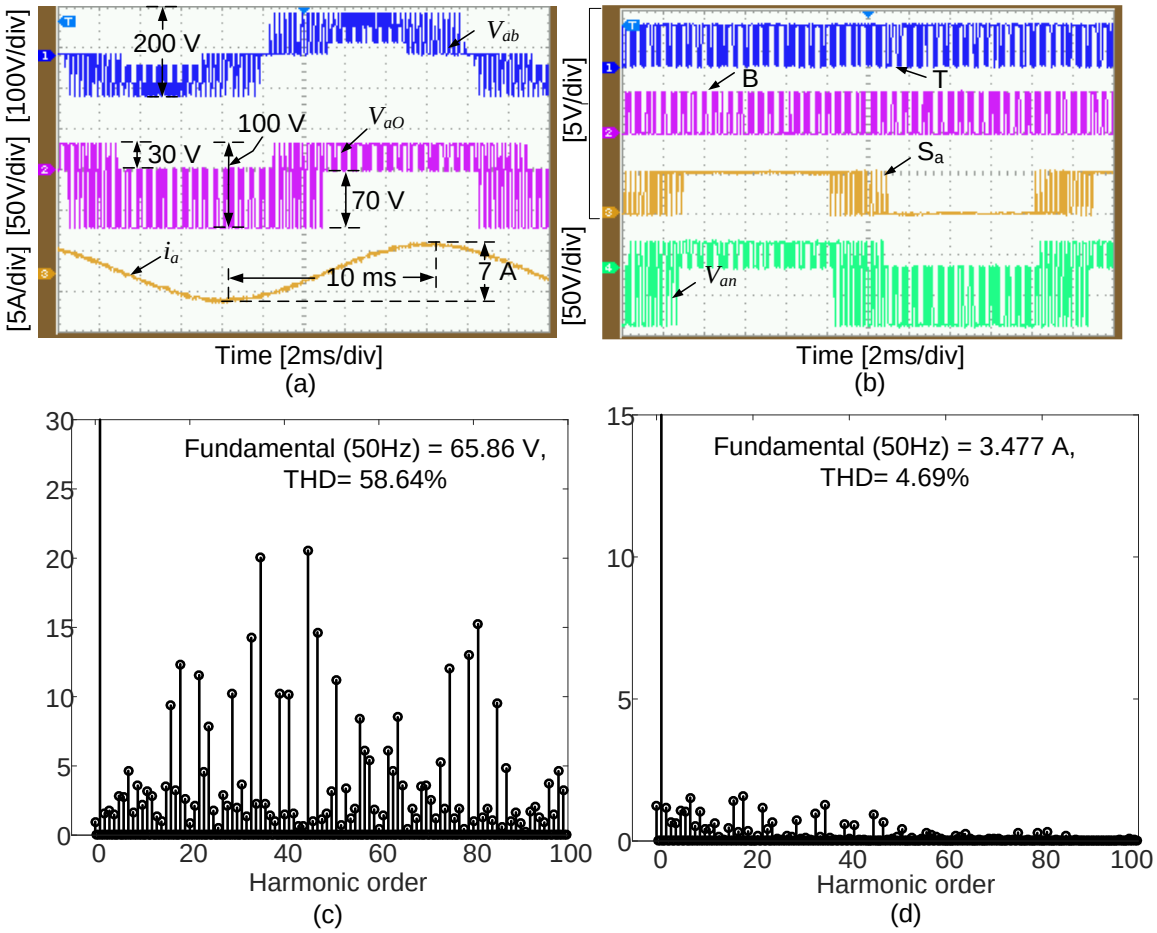
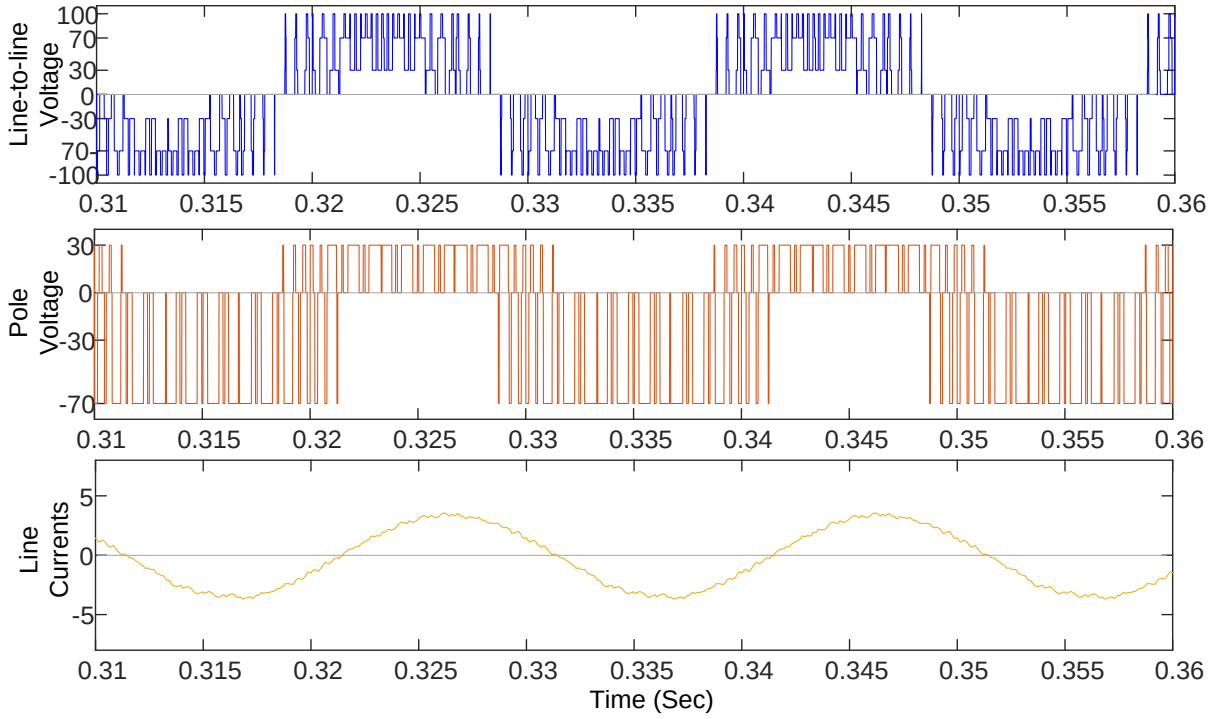


Figure 7-46 Experimental results at m=0.65 (a) AC side waveforms, (b) Switching signals, ((c) Voltage and (d) current harmonic spectrum (when $V_{c1} = 30V$ and $V_{c2} = 70V$).



(a)

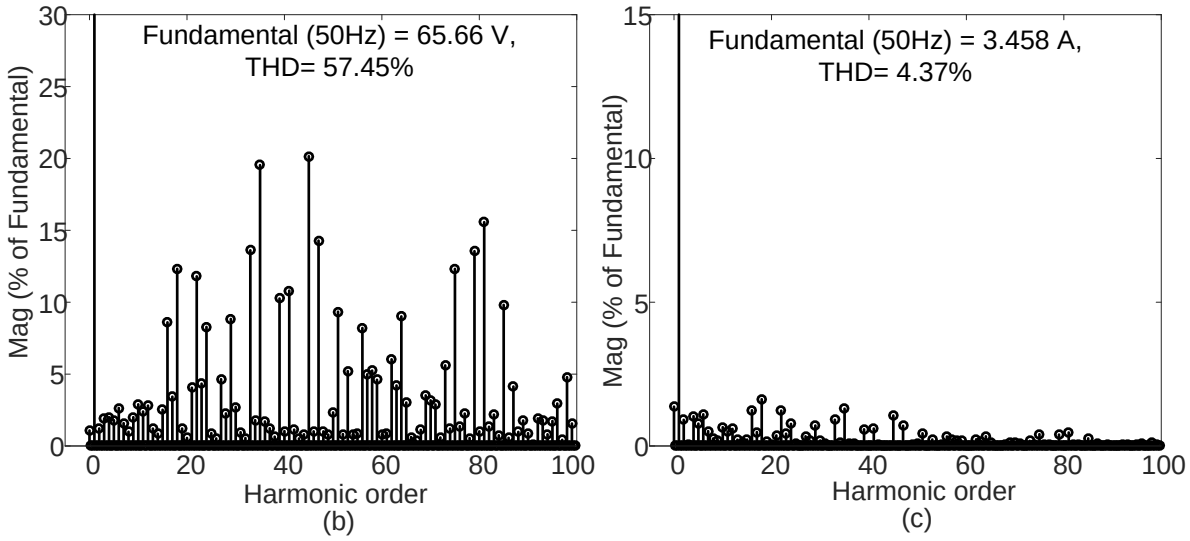


Figure 7-47 Simulation results at m=0.65 (a) AC side waveforms, (b) Switching signals, (c) Voltage and (d) current harmonic spectrum (when $V_{c1} = 30V$ and $V_{c2} = 70V$).

Table 7-3 summarizes the performance of the hybrid 2/3L NPCI when exited with unequal capacitor voltages for two cases (1) V_{C1} = 60V and V_{C2} = 40V and V_{C1} = 30V and V_{C2} = 70V with VV-based modulation method for two modulation indices.

Table 7-4 Comparison of Experimental and downscaled simulation results of 3L NPCI for various modulation methods

Performance Parameter		Modulation index (m)			
		0.98		0.65	
		(V_{C1} = 60V and V_{C2} = 40V)	(V_{C1} = 30V and V_{C2} = 70V)	(V_{C1} = 60V and V_{C2} = 40V)	(V_{C1} =30V and V_{C2} = 70V)
Line-to-line Voltage (V) (Peak)	Experimental	98.55	98.55	65.86	65.86
	Simulation	98.62	98.62	65.66	65.66
% THD of Line-to-line Voltage	Experimental	45.85	46.10	53.37	58.64
	Simulation	44.87	45.03	52.20	57.45
Line Current (A) (peak)	Experimental	5.207	5.207	3.477	3.477
	Simulation	5.192	5.192	3.458	3.458
% THD of Line Current	Experimental	2.58	2.63	3.77	4.69
	Simulation	2.75	2.76	3.33	4.37

Similar to the hybrid 2/3L NPCI, the higher-level RSS MPCI topologies derived in chapter 6 are tested experimentally under same DC link voltage and loading conditions.

7.5 Performance Investigation of 4L RSS MPCI

The 4L RSS MPCI topology and the modulation methods discussed in chapter 6 are experimentally verified in this section. The two proposed modulation schemes for 4L RSS MPCI are implemented and the obtained results are provided. A 3L NPCI phase leg is used instead of modified T-Type NPCI due to availability.

7.5.1 Performance of 4L RSS MPCI with VV-based Method:

To analyze the effect of using the virtual vector $VV_4 = (V_3 + V_5)/2$ discussed in Section 6.6.2, three modulation indices 0.98, 0.87 and 0.75 are chosen.

Figure 7-49 through Figure 7-53 show some of the experimental results for the proposed VV modulation scheme for these three modulation indices.

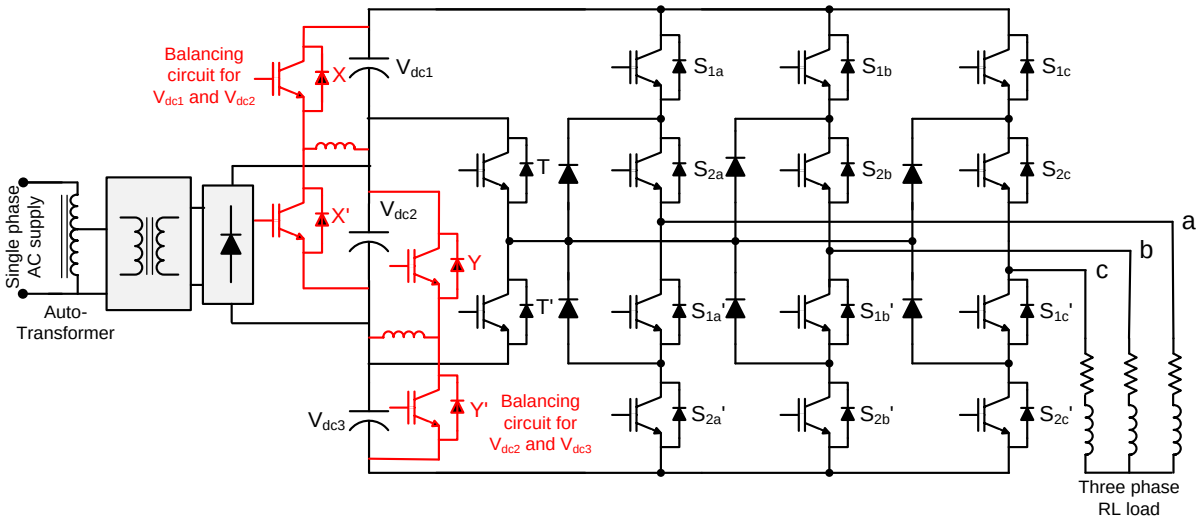


Figure 7-48 Experimental setup of three phase 4L RSS MPCI with RL load.

The experimentally obtained waveforms of the 4L RSS MPCI at modulation index *m=0.98*, are presented in Figure 7-49 At this modulation index, the virtual vector VV_4 is far from V_{ref} results in minimum duty ratio for the VV_4. As a result, the distortion due to additional voltage steps is relatively small. In addition, the 4L RSS MPCI is tested at reduced modulation indices m=0.86 and m=0.75 and obtained results are shown Figure 7-51 and Figure 7-53 respectively. When modulation index is decreasing, the duty ratio of VV_4 increases, and results in increased distortion. This effect is clearly observed from voltage waveforms. The additional steps in the voltage waveforms also distort the line currents which are shown in THD spectrum.

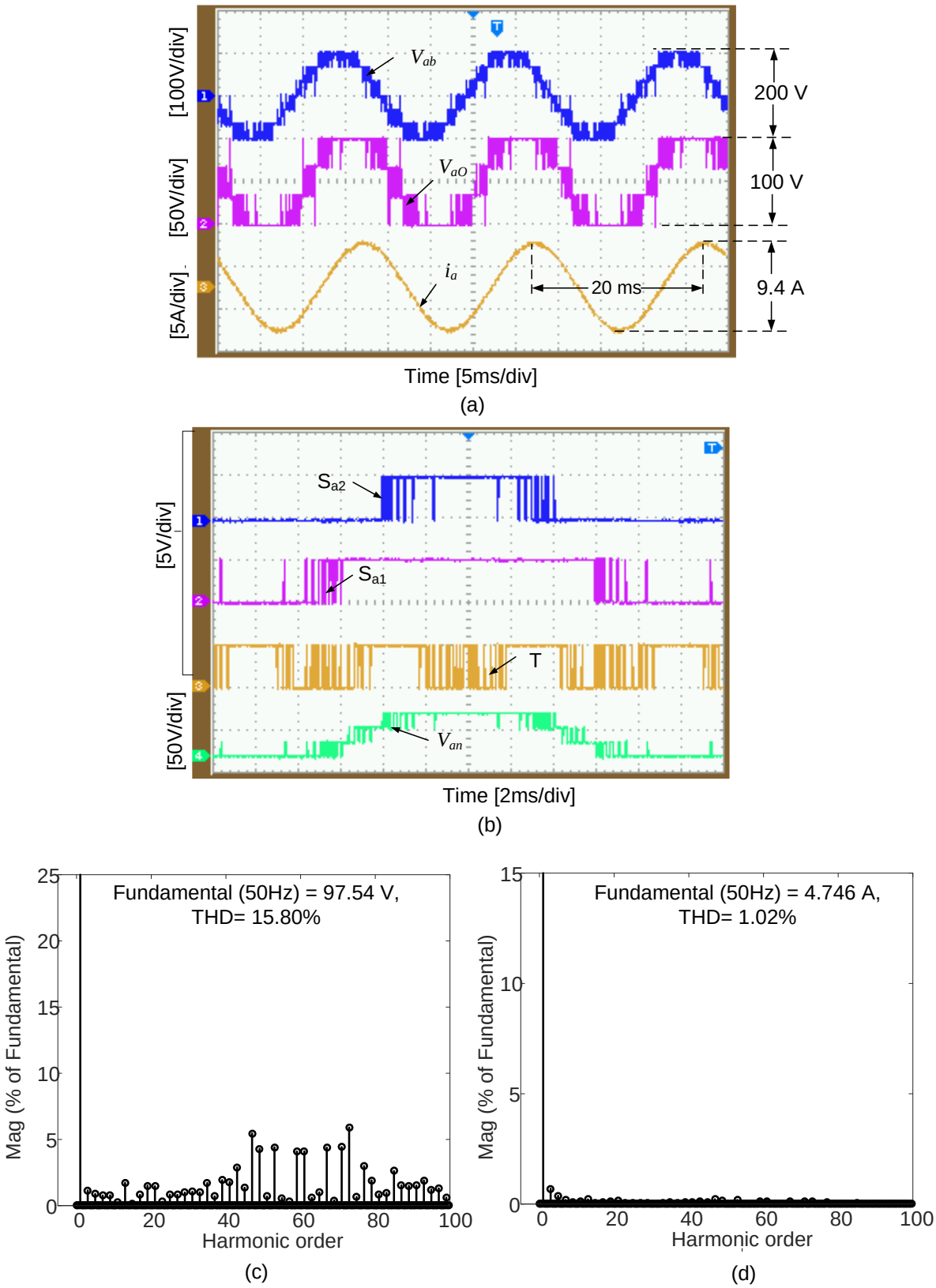
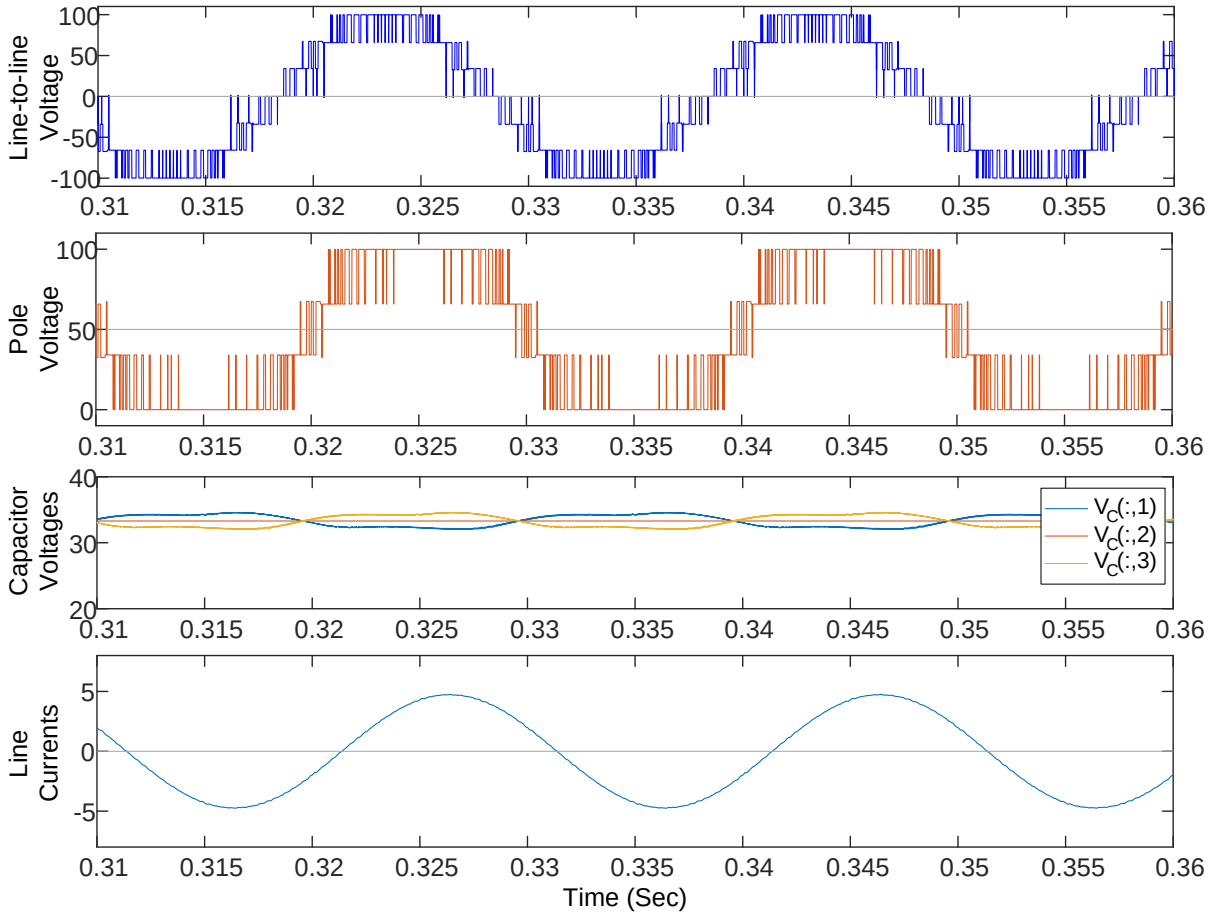
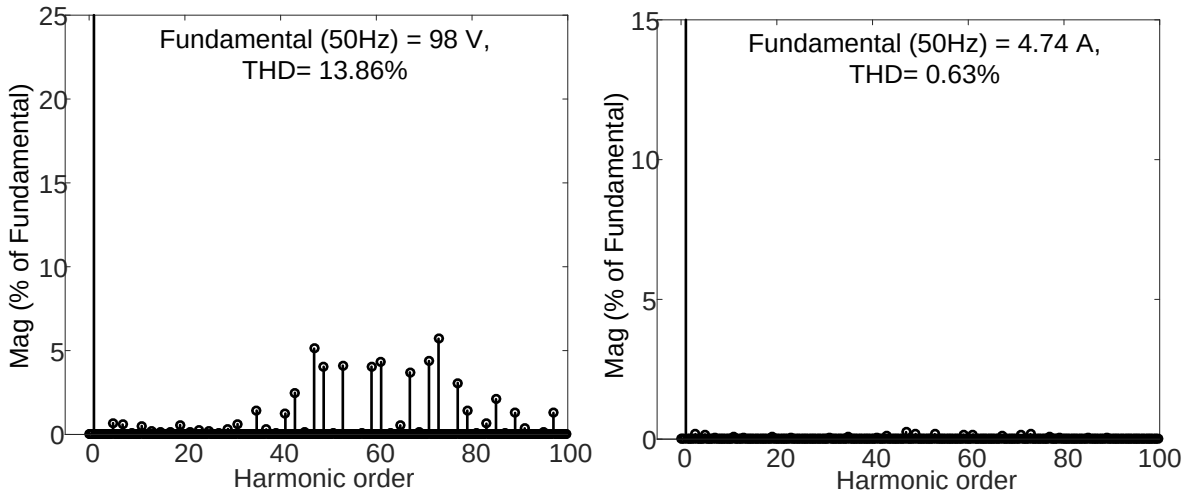


Figure 7-49 Experimental results of 4L RSS MPCI with VV modulation for m=0.98 (a) AC side waveforms, (b) Switching signals, (c) Voltage harmonic spectrum and (d) current harmonic spectrum (when load R=10 Ω and L=5 mH per phase).

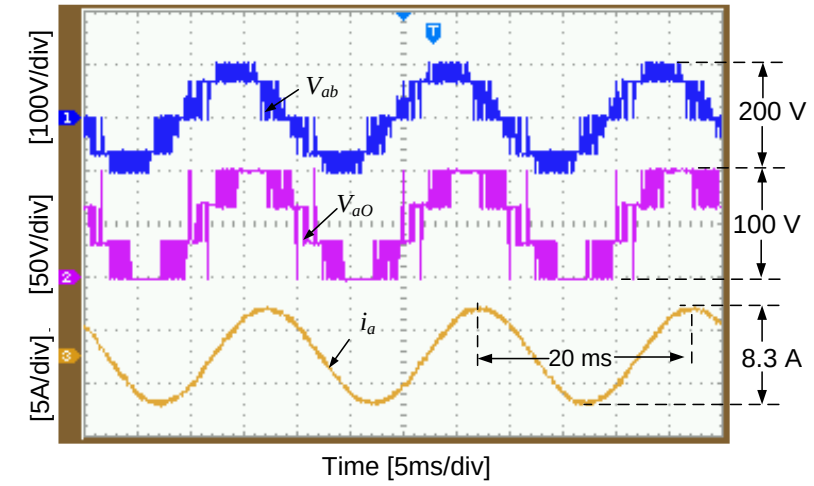


(a)

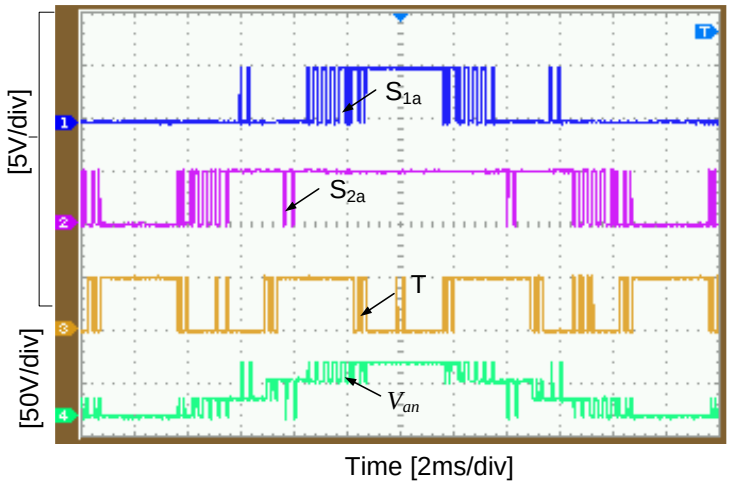


(b) (c)

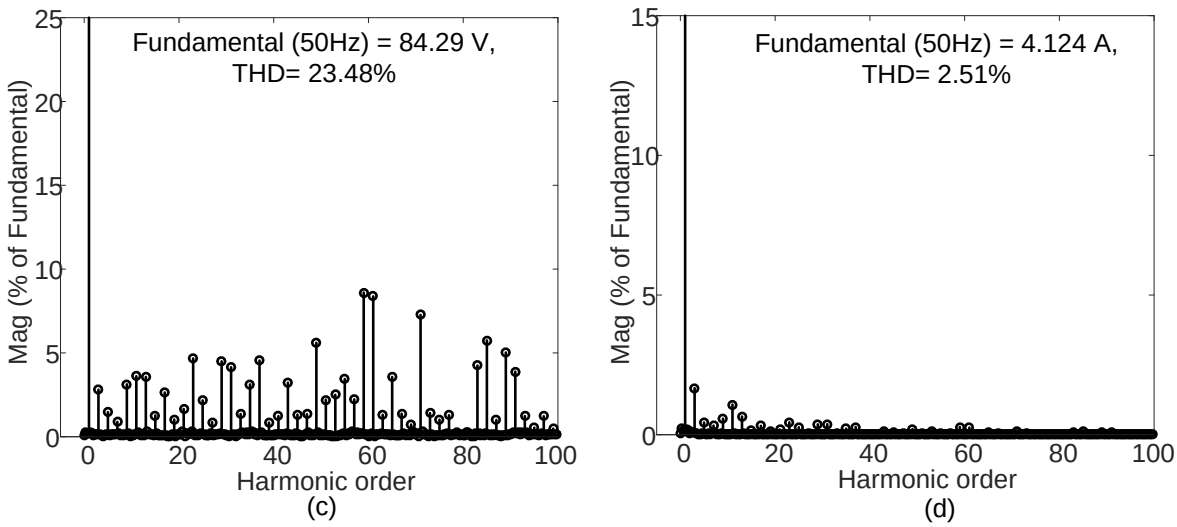
Figure 7-50 Simulation results of 4L RSS MPCI with VV modulation for m=0.98 (a) Voltage and current waveforms, (c) Voltage harmonic spectrum amd (d) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).



(a)

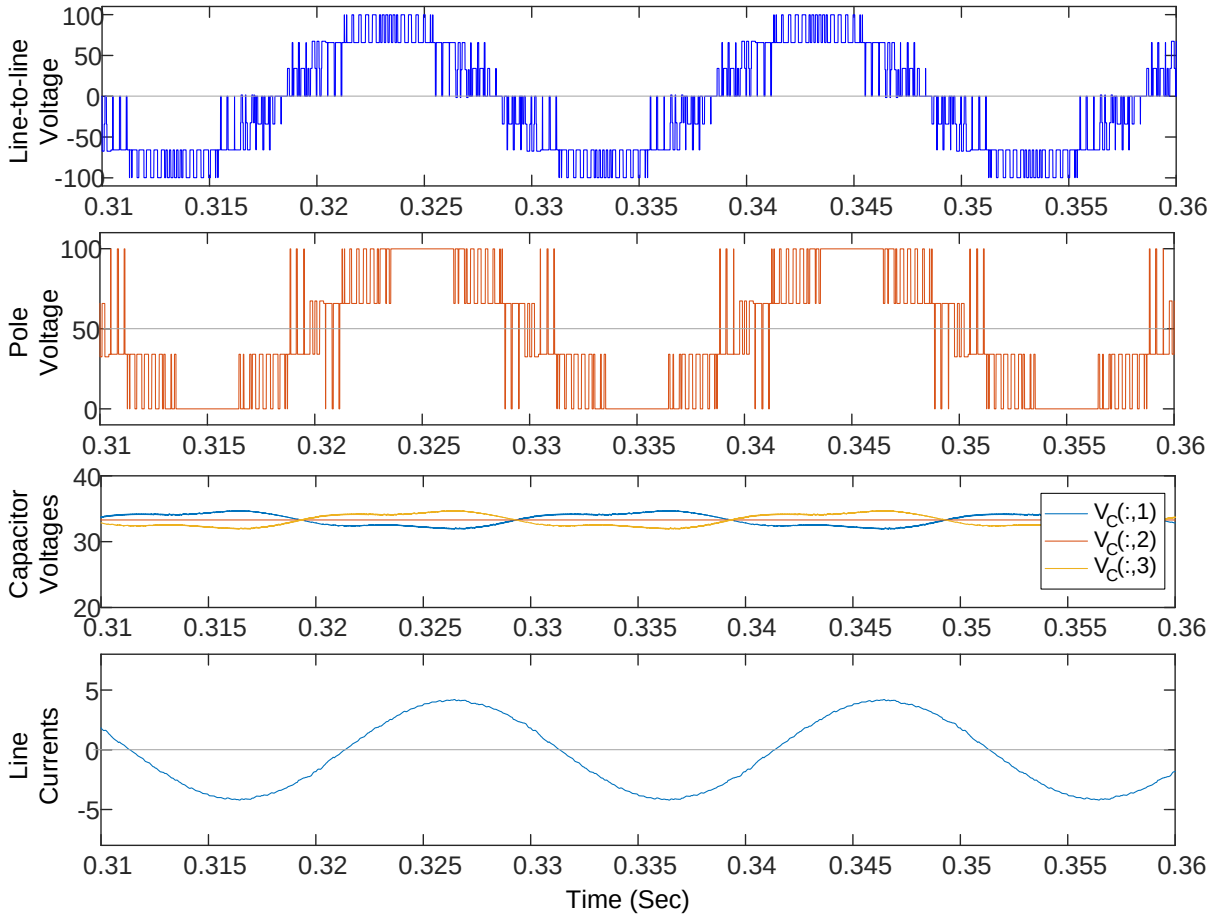


(b)

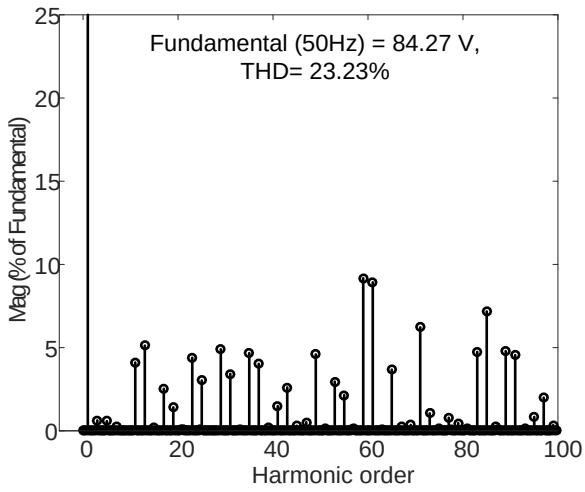


(c) (d)

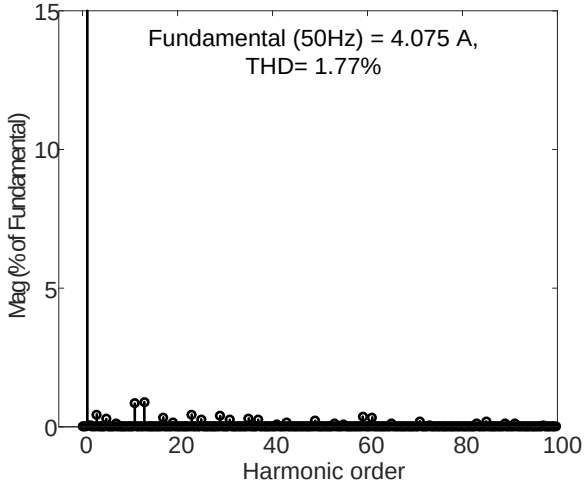
Figure 7-51 Experimental results of 4L RSS MPCI with VV modulation for m=0.86 (a) AC side waveforms, (b) Switching signals, (c) Voltage harmonic spectrum and (d) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).



(a)

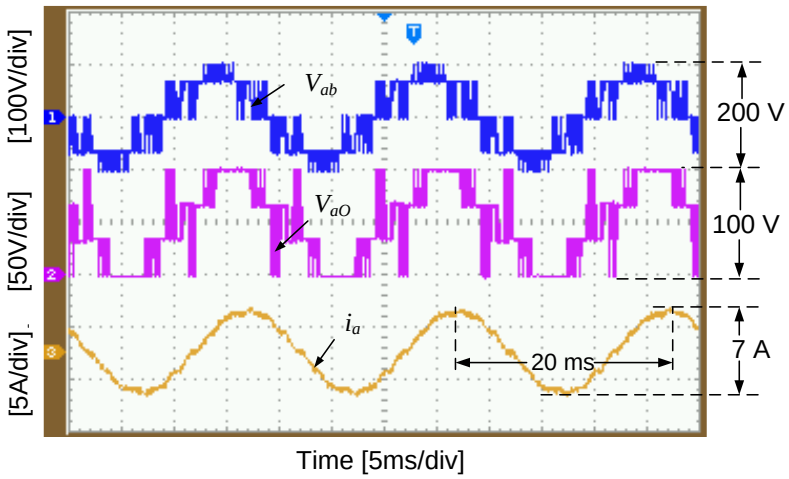


(b)

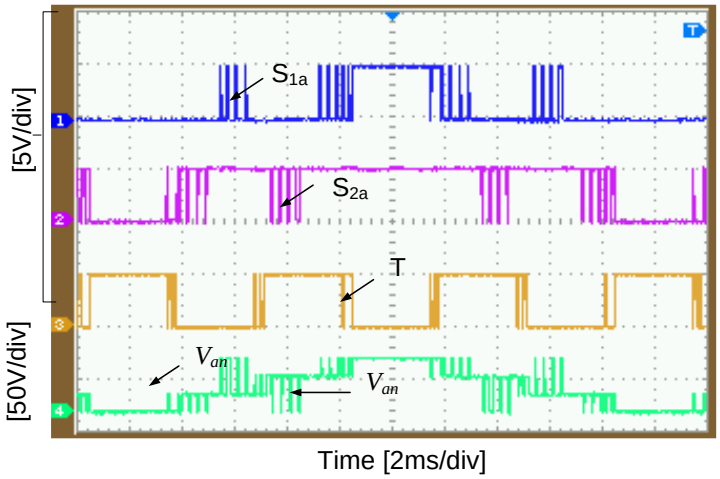


(c)

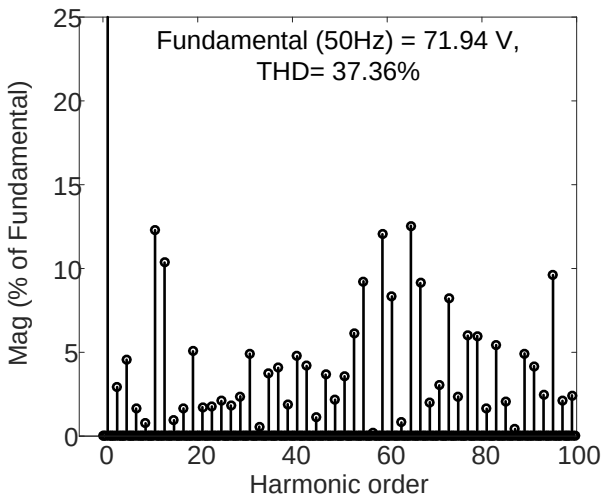
Figure 7-52 Simulation results of 4L RSS MPCI with VV modulation for m=0.86 (a) Voltage and current waveforms, (c) Voltage harmonic spectrum and (d) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).



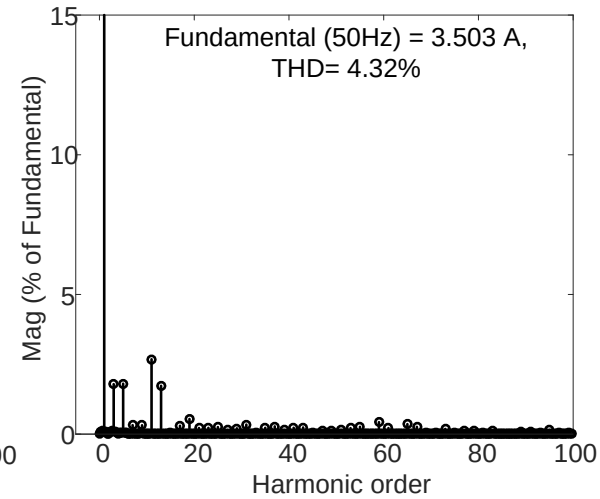
(a)



(b)

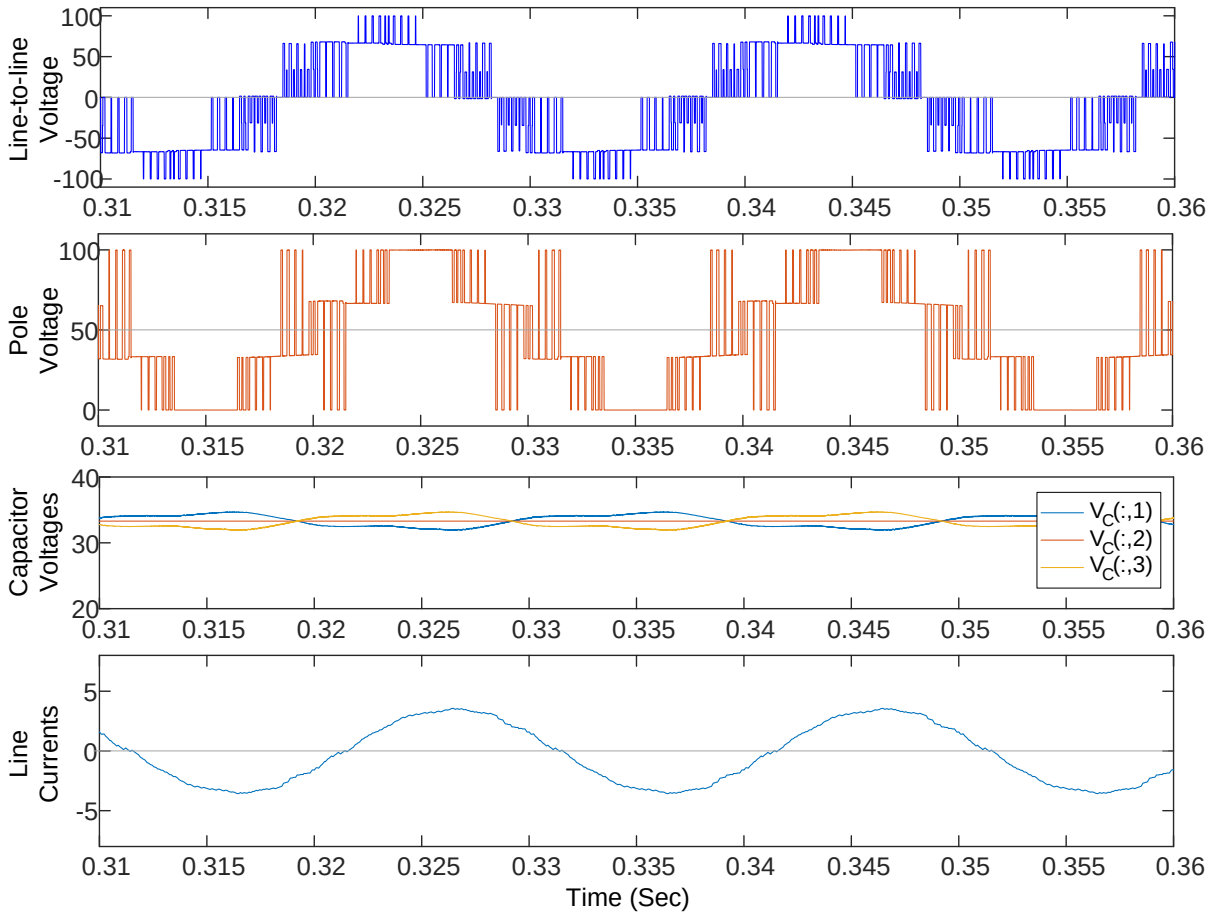


(c)

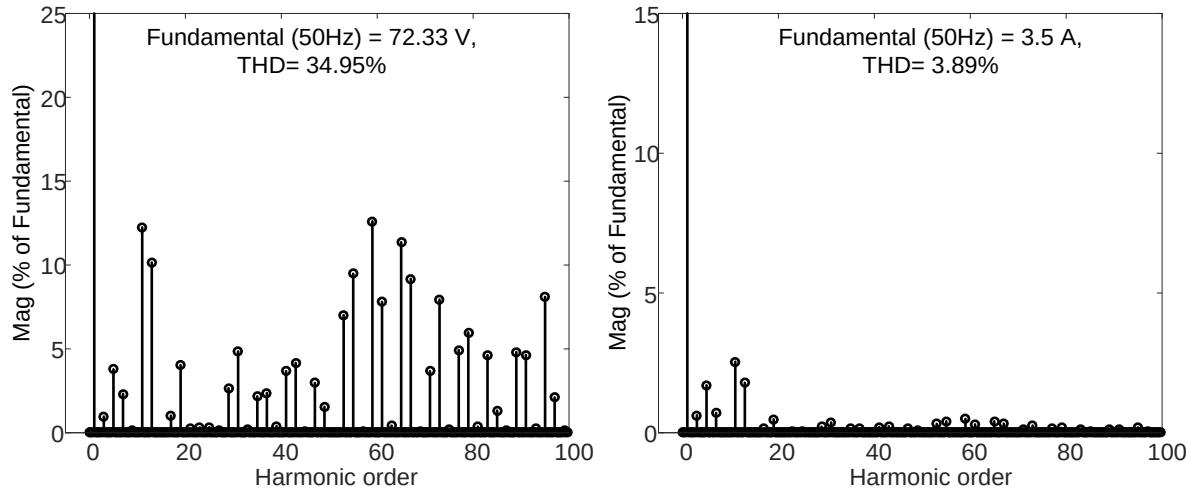


(d)

Figure 7-53 Experimental results of 4L RSS MPCI with VV modulation for m=0.75 (a) AC side waveforms, (b) Switching signals, (c) Voltage harmonic spectrum and (d) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).



(a)



(b) (c)

Figure 7-54 Simulation results of 4L RSS MPCI with VV modulation for m=0.75 (a) Voltage and current waveforms, (c) Voltage harmonic spectrum and (d) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).

Therefore, for all the modulation indices, the experimental performance of 4L RSS MPCI with the VV-based modulation is comparable with the simulation results and theory, thereby validating the experimental results. Table 7-5 summarizes the performance of the 4L RSS MPCI with VV-based modulation method for three modulation indices.

Table 7-5 Comparison of Experimental and downscaled simulation results of 4L RSS MPCI for VV-based modulation method

Performance Parameter		Modulation index (m)		
		0.98	0.86	0.75
Line-to-line Voltage (V) (Peak)	Experimental	97.54	84.29	71.94
	Simulation	98	84.27	72.33
% THD of Line-to-line Voltage	Experimental	15.8	23.48	37.36
	Simulation	13.86	23.23	34.95
Line Current (A) (peak)	Experimental	4.746	4.124	3.503
	Simulation	4.74	4.075	3.5
% THD of Line Current	Experimental	1.02	2.51	4.32
	Simulation	0.63	1.77	3.89
Capacitor Voltage Ripple (V)	Experimental	2	2	2
	Simulation	2.5	2.4	2.5

7.5.2 Performance of 4L RSS MPCI with STV-based Method:

Figure 7-55 through Figure 7-60 show the various experimental and downscaled simulation results of 4L RSS MPCI operated with STV-based modulation method at three different modulation indices m=0.98, m=0.86 and m=0.75 respectively. From Figure 7-55 (a) it is observed that, the pole voltage and line voltage waveforms do not have additional voltage steps at modulation index m=0.98. This is analogous to the theory and simulation results of STV-based modulation discussed in Section 6.6.2 and section 6.8. respectively. The performance of the 4L RSS MPCI with the STV-based modulation is also improved at the medium modulation indices regions which is evident from the experimental waveforms shown in Figure 7-57(a) and Figure 7-59(a) for m=0.86 and m=0.75 respectively. As a result, the current distortion is also significantly reduced compared to VV-based modulation scheme.

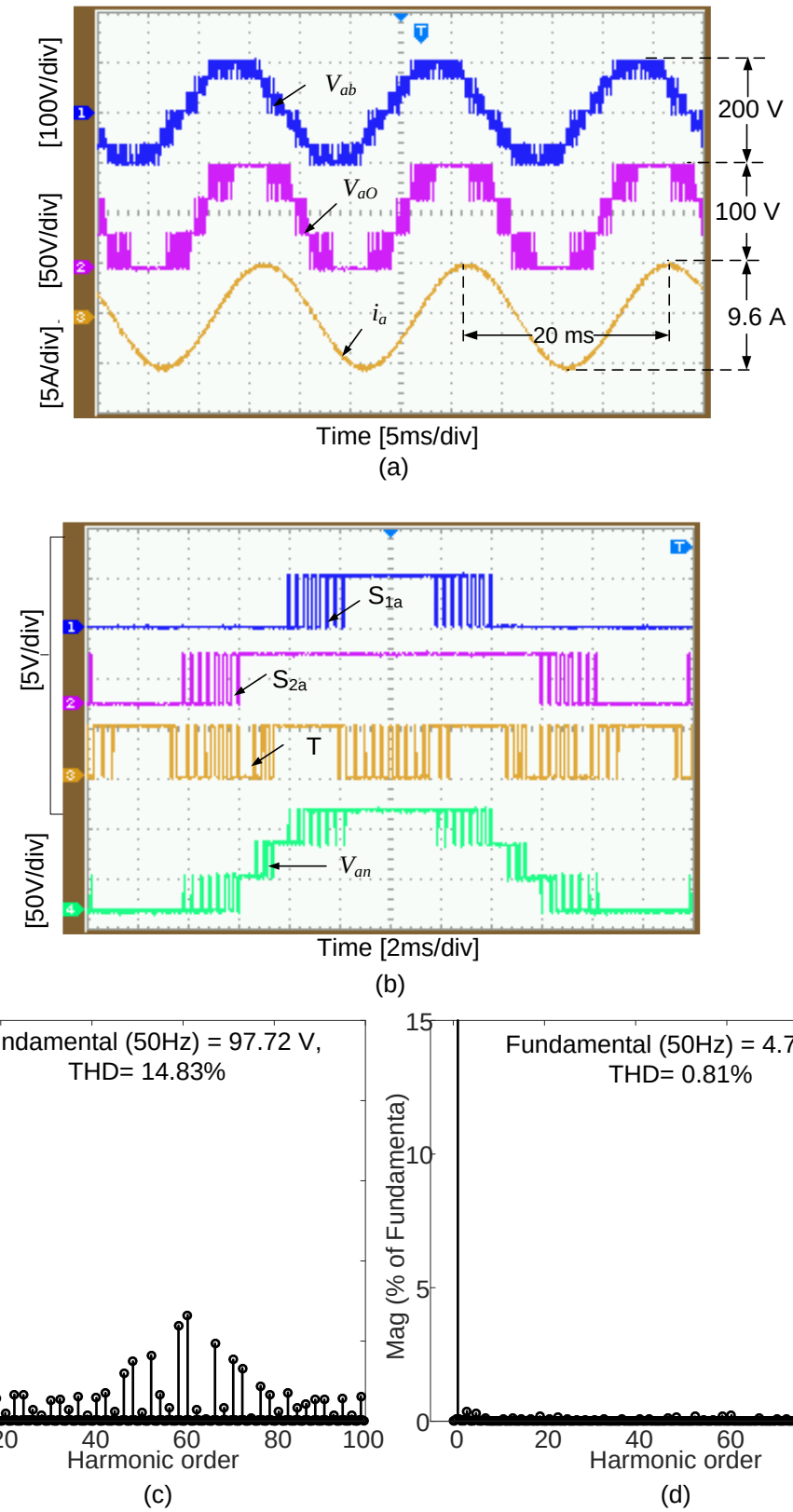
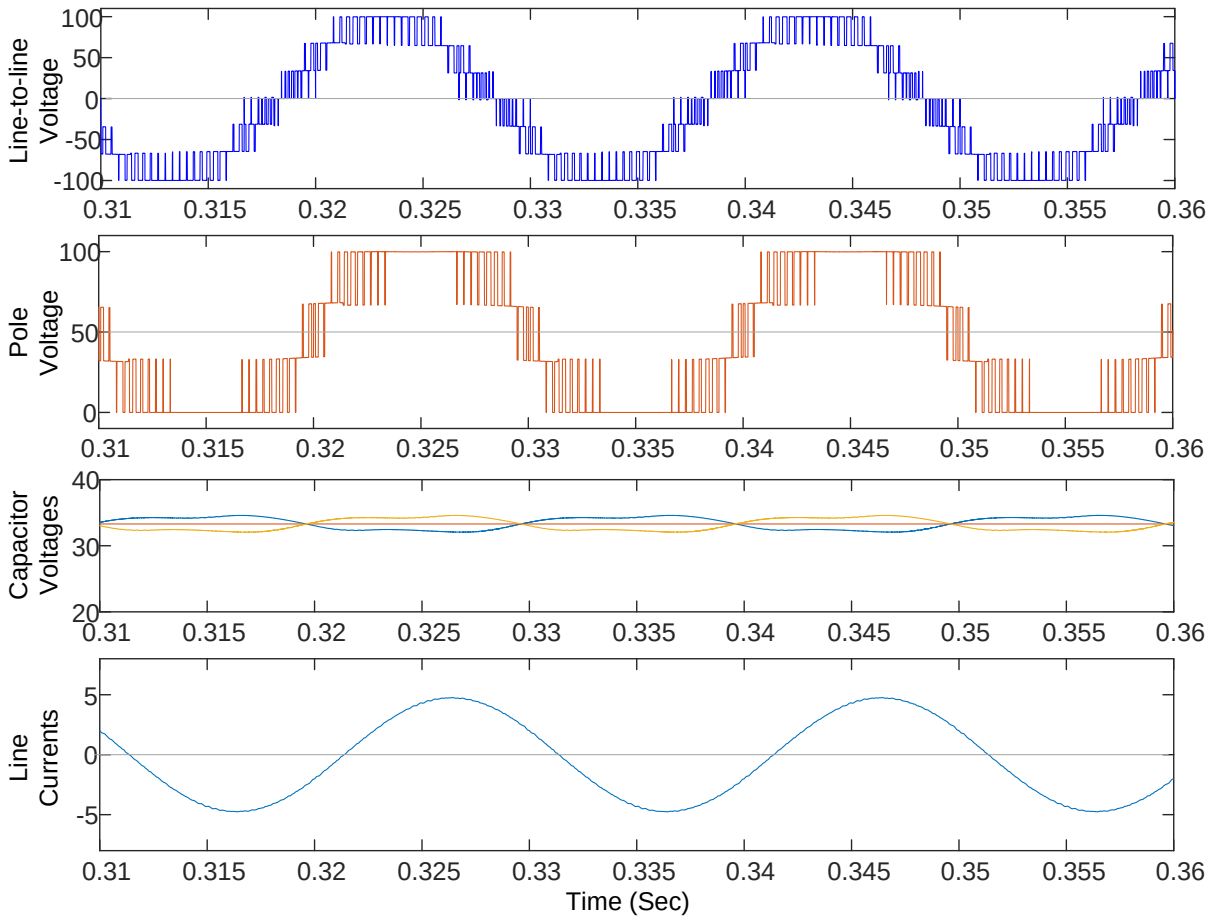
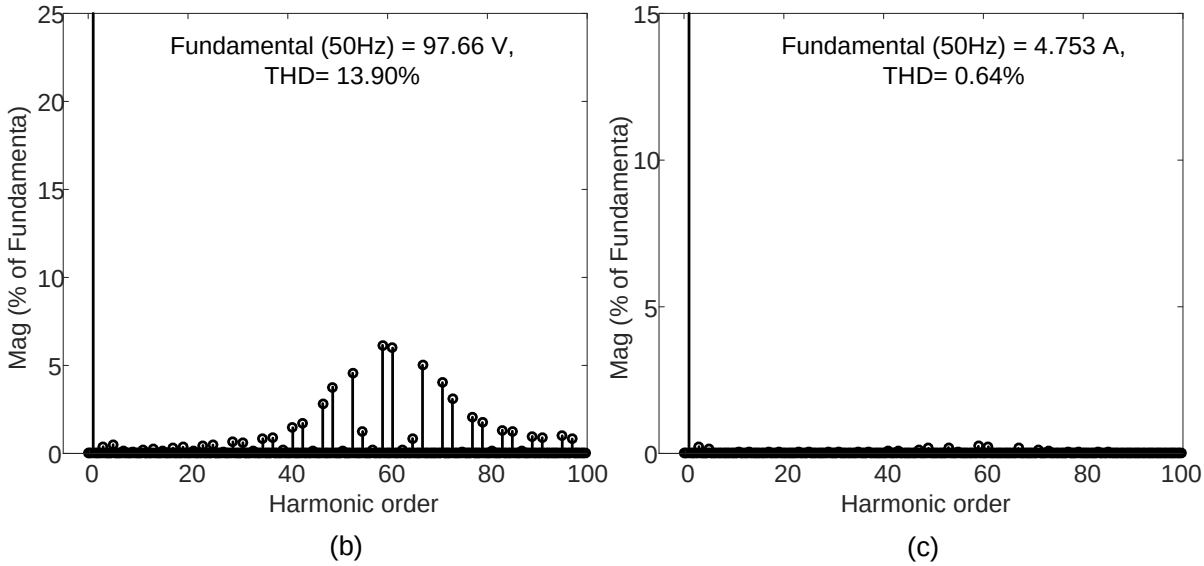


Figure 7-55 Experimental results of 4L RSS MPCI with STV modulation for m=0.98 (a) AC side waveforms, (b) Switching signals, (c) Voltage harmonic spectrum and (d) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).



(a)



(b) (c)

Figure 7-56 Simulation results of 4L RSS MPCI with STV modulation for m=0.98 (a) Voltage and current waveforms, (c) Voltage harmonic spectrum and (d) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).

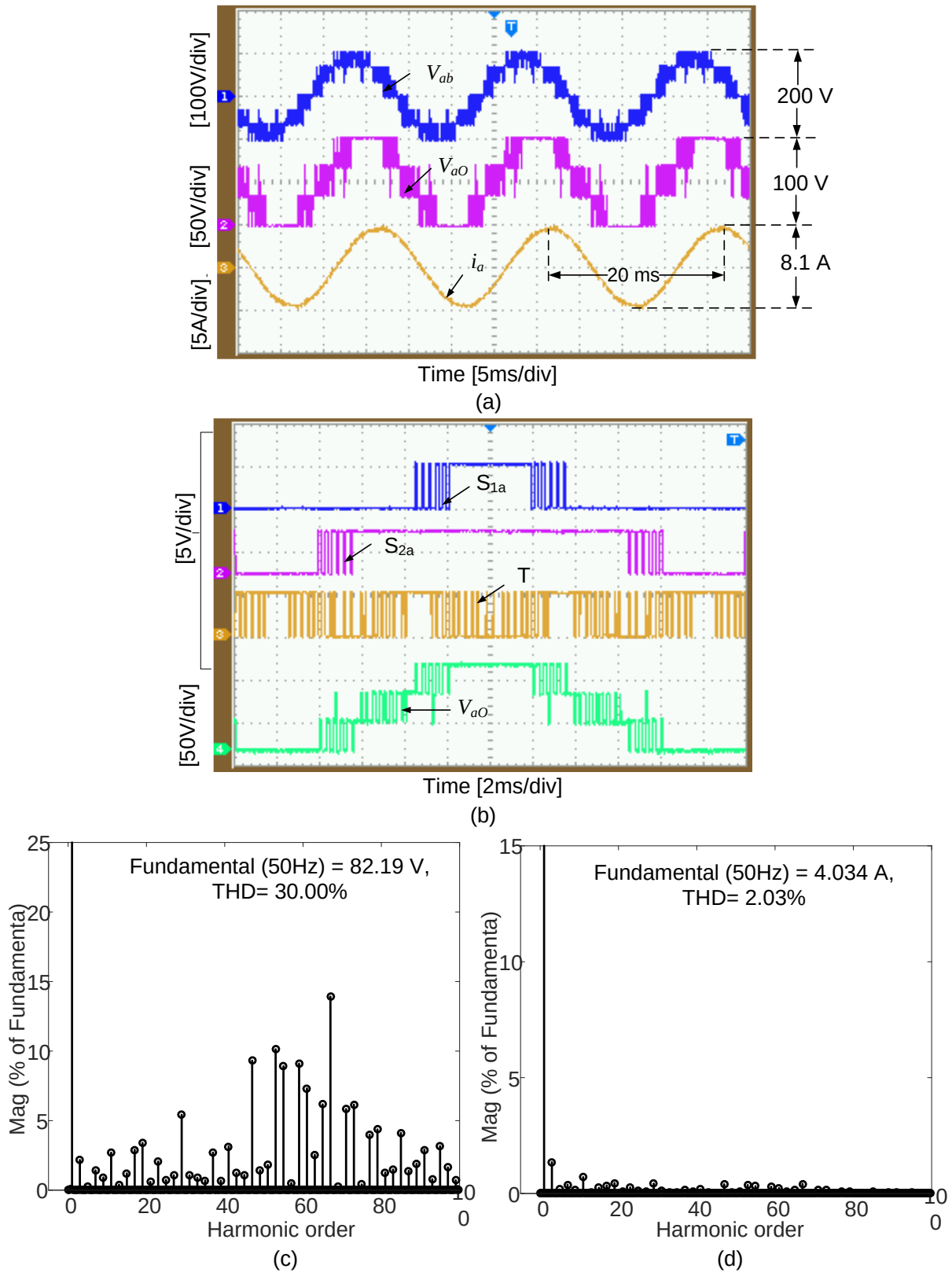
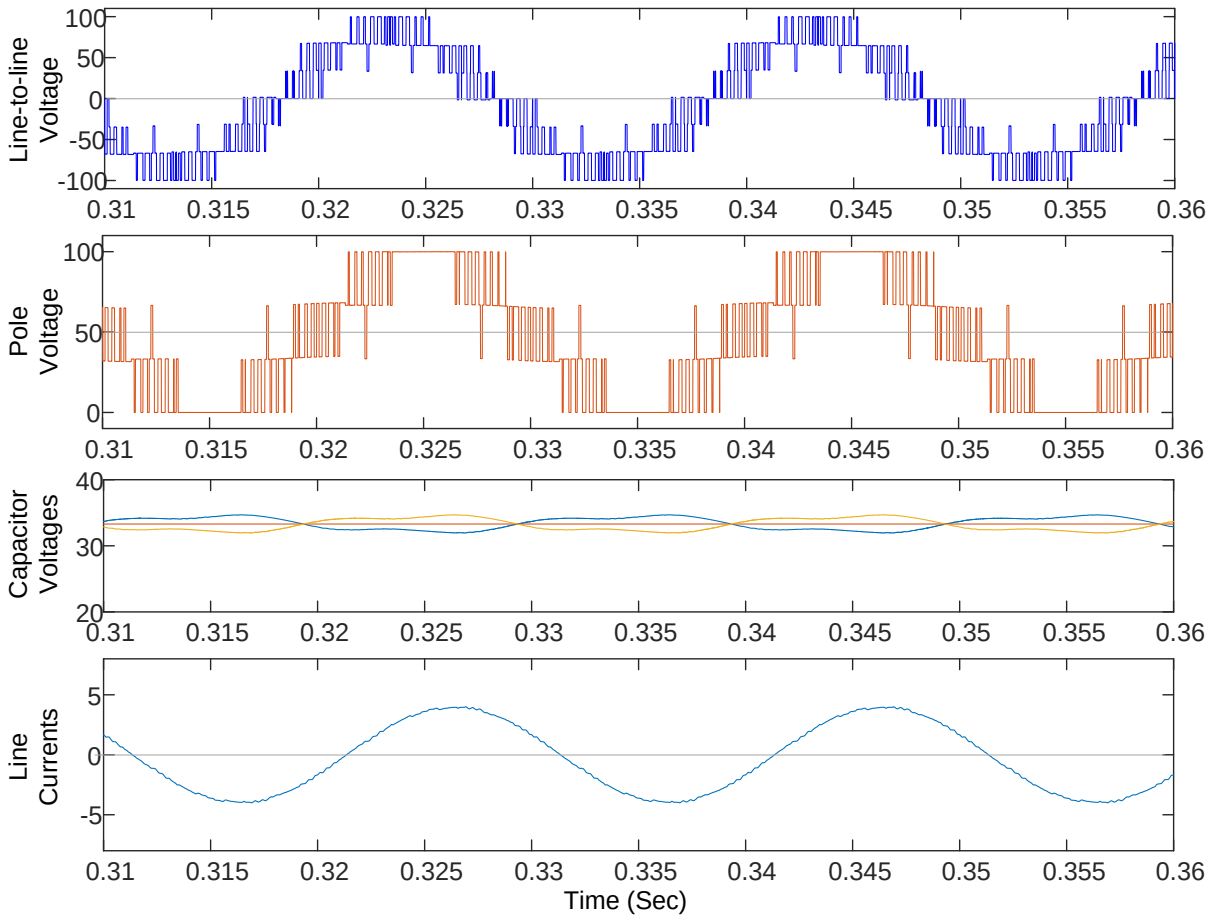
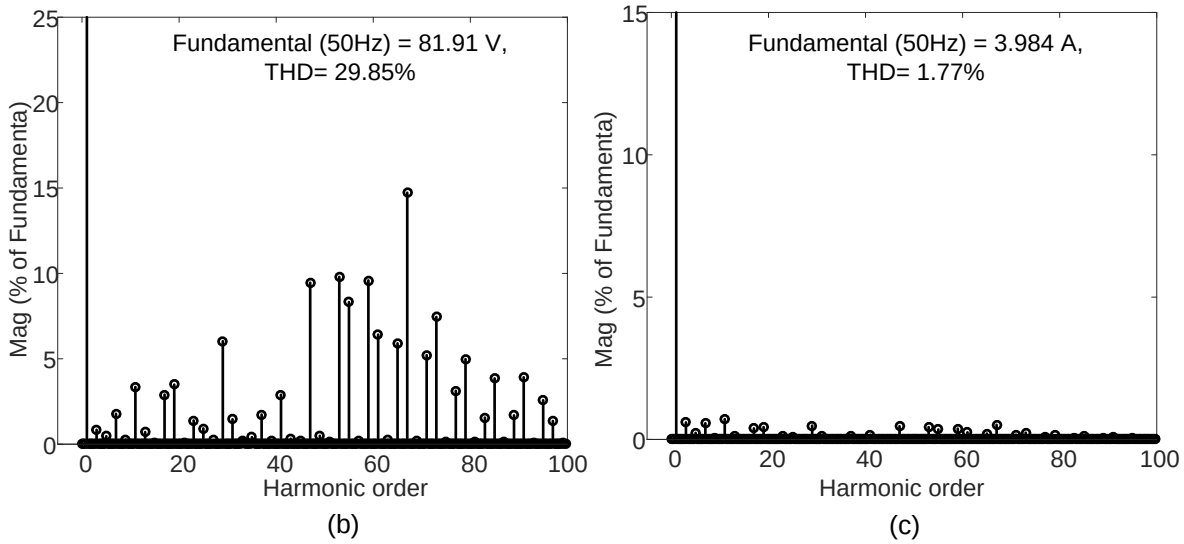


Figure 7-57 Experimental results of 4L RSS MPCI with STV modulation for m=0.86 (a) AC side waveforms, (b) Switching signals, (c) Voltage harmonic spectrum and (d) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).



(a)



(b) (c)

Figure 7-58 Simulation results of 4L RSS MPCI with STV modulation for m=0.86 (a) Voltage and current waveforms, (c) Voltage harmonic spectrum and (d) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).

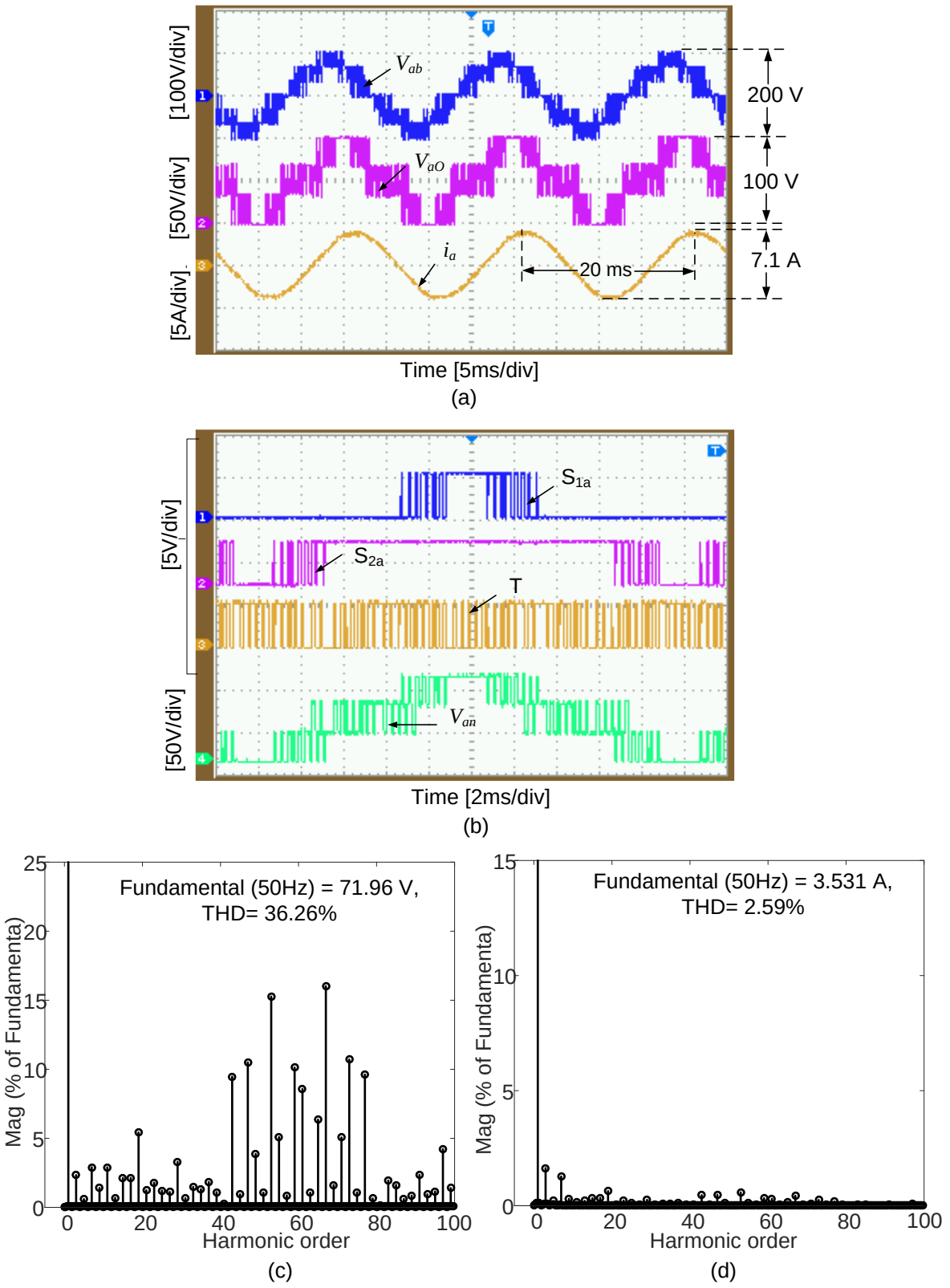
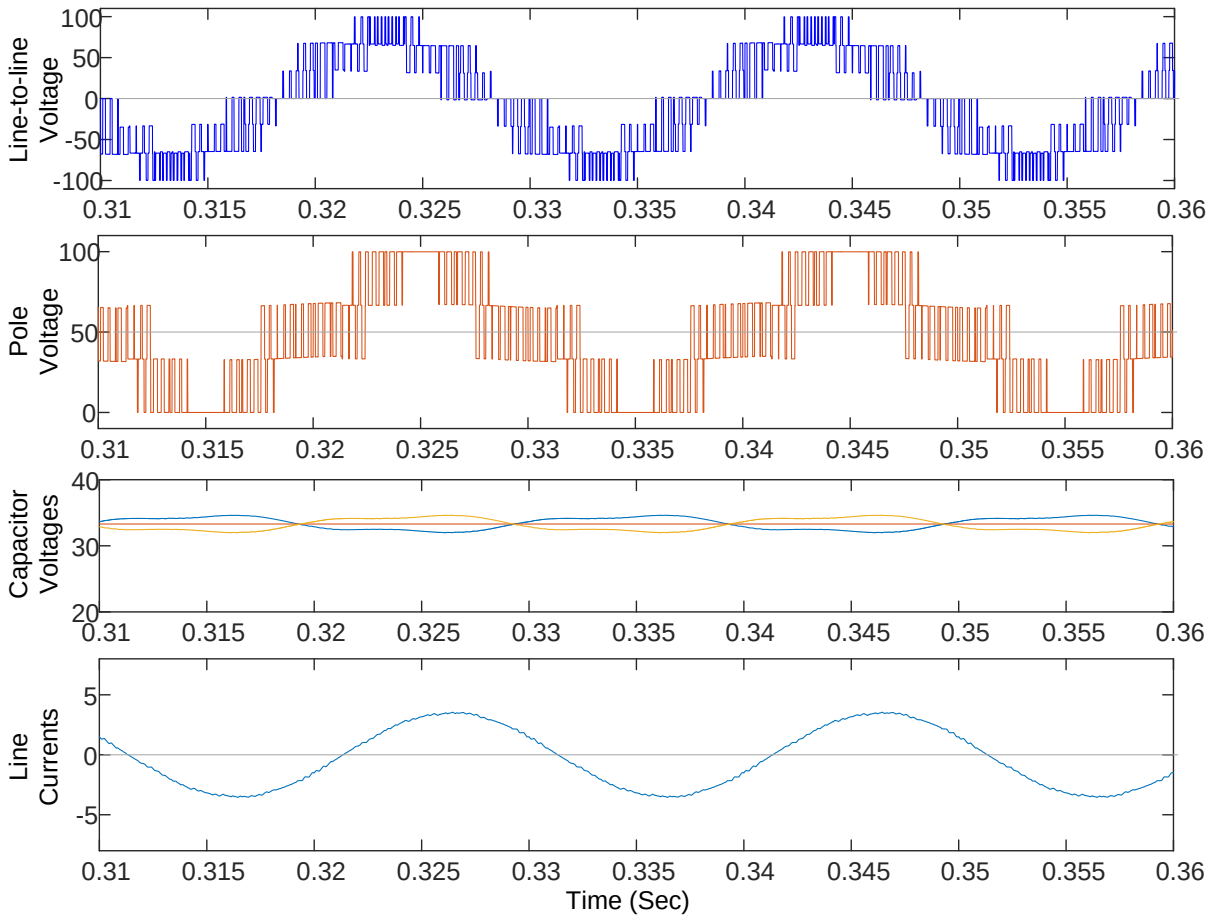
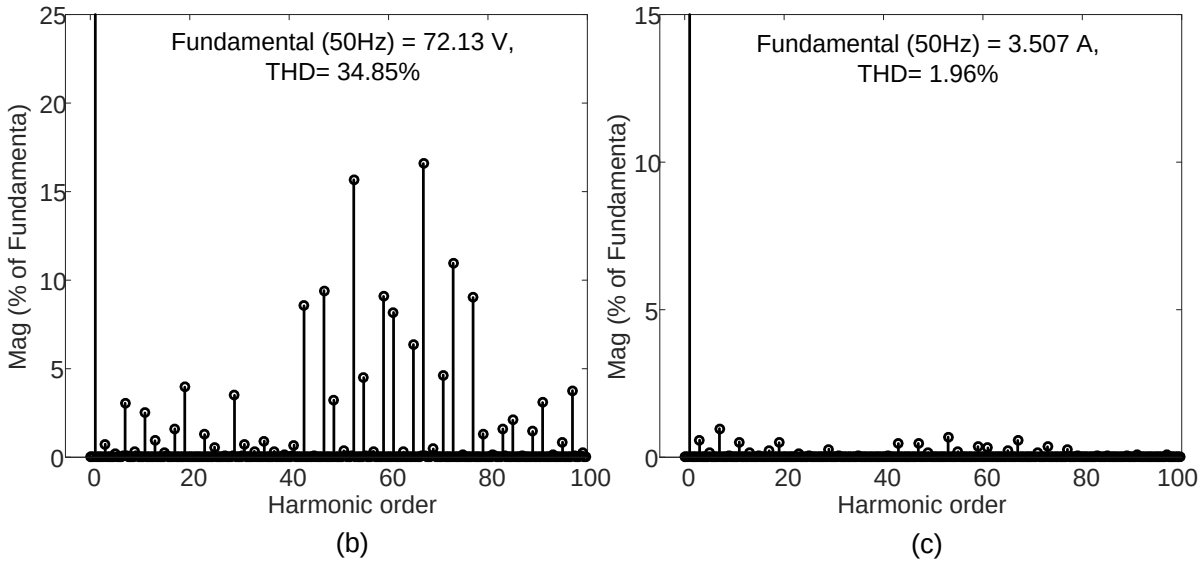


Figure 7-59 Experimental results of 4L RSS MPCI with STV modulation for m=0.75 (a) AC side waveforms, (b) Switching signals of hybrid 2/3L NPCI, (c) Voltage harmonic spectrum, (d) current harmonic spectrum and (when load R=10 Ω and L=15 mH per phase).



(a)



(b) (c)

Figure 7-60 Simulation results of 4L RSS MPCI with STV modulation for m=0.75 (a) Voltage and current waveforms, (c) Voltage harmonic spectrum and (d) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).

Table 7-6 summarizes the performance of the 4L RSS MPCI with STV-based modulation method for three modulation indices.

Table 7-6 Comparison of experimental and downscaled simulation results of 4L RSS MPCI for STV-based modulation method

Performance Parameter		Modulation index (m)		
		0.98	0.86	0.75
Line-to-line Voltage (V) (Peak)	Experimental	97.72	82.19	71.96
	Simulation	97.66	81.91	72.13
THD of Line-to-line Voltage %	Experimental	14.83	30	36.26
	Simulation	13.9	29.85	34.85
Line Current (A) (peak)	Experimental	4.725	4.034	3.531
	Simulation	4.753	3.984	3.507
THD of Line Current %	Experimental	0.81	2.03	2.59
	Simulation	0.64	1.77	1.96
Capacitor Voltage Ripple (V)	Experimental	2	2	2
	Simulation	2.2	2.2	2.5

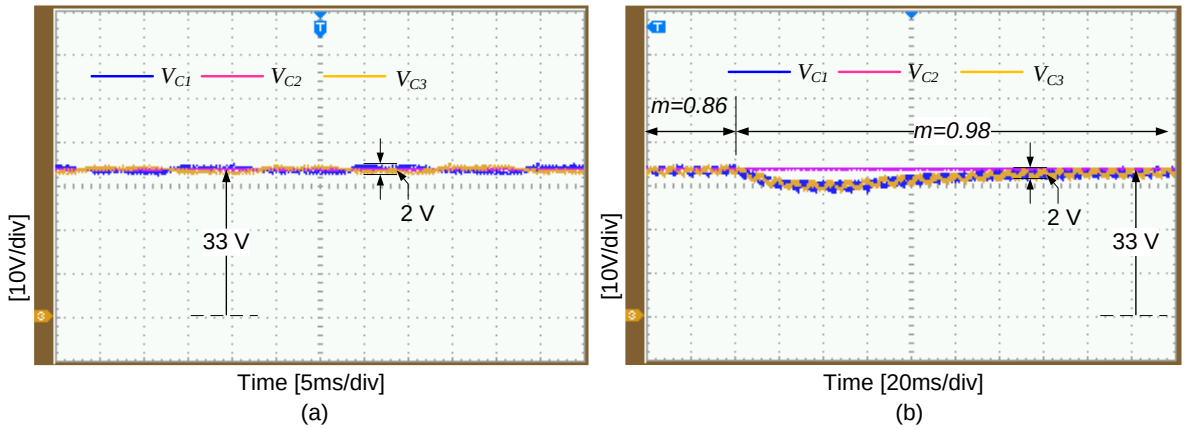


Figure 7-61 Capacitor voltages of 4L RSS MPCI with the balancing circuit. (a) Steady state waveforms for m=0.86 and (b) transient waveforms when for the change on modulation index from m=0.86 to m=0.98.

Figure 7-61 show the experimental capacitor voltage waveforms of 4L RSS MPCI obtained for steady state and transient conditions for the change in the modulation index. The voltage 33.3

V across the capacitor V_{dc2} is transformed to V_{dc1} and V_{dc3} using the balancing circuits shown in Figure 7-48. Therefore, a DC link voltage of 100V has been successfully achieved.

7.6 Performance Investigation of 5L RSS MPCI

The two 5L MPCI RSS VSI topologies: Type-1 and Type-2 discussed in Section 6.11 are built as shown in Figure 7-62 and Figure 7-67 respectively for experimental verification with the proposed VV-based modulation. A 3L NPCI phase leg is used instead of modified T-Type NPCI due to availability. The total DC link voltage and load are kept same for comparison. The isolated DC voltage equal to 50V is generated from single phase AC supply and full wave rectifier and connected across P1 and N1. The top and bottom capacitors V_{dc1} and V_{dc4} are supplied from the two balancing circuits. Two higher modulation indices are tested for validating the simulation results.

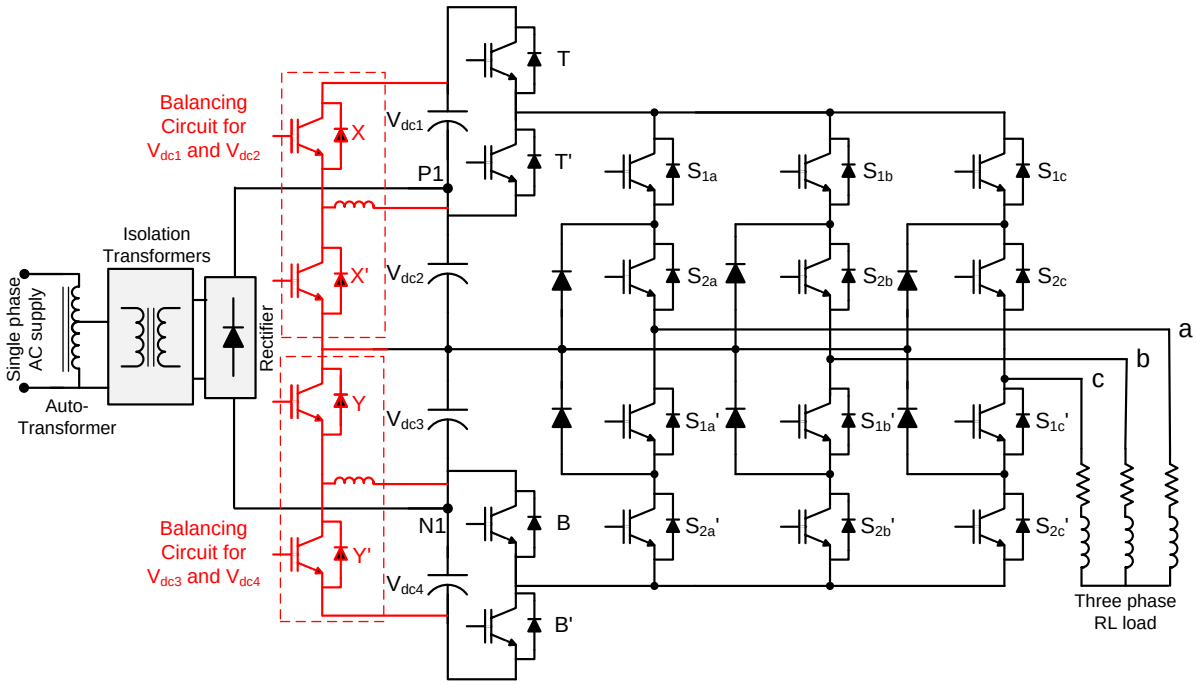
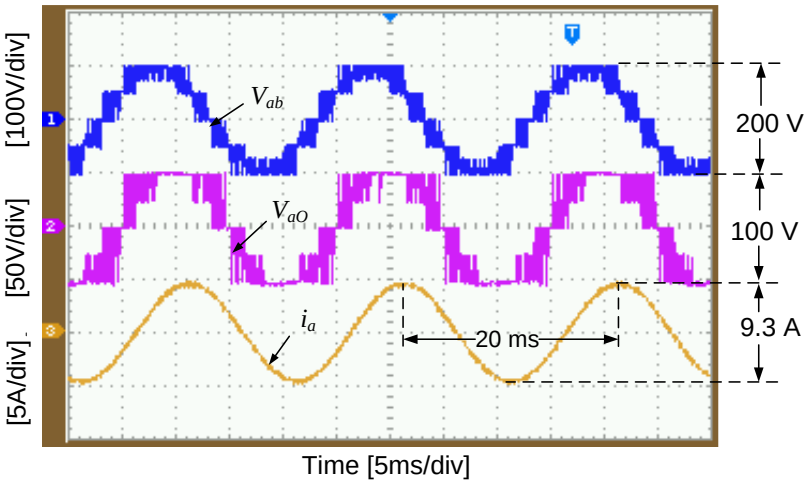


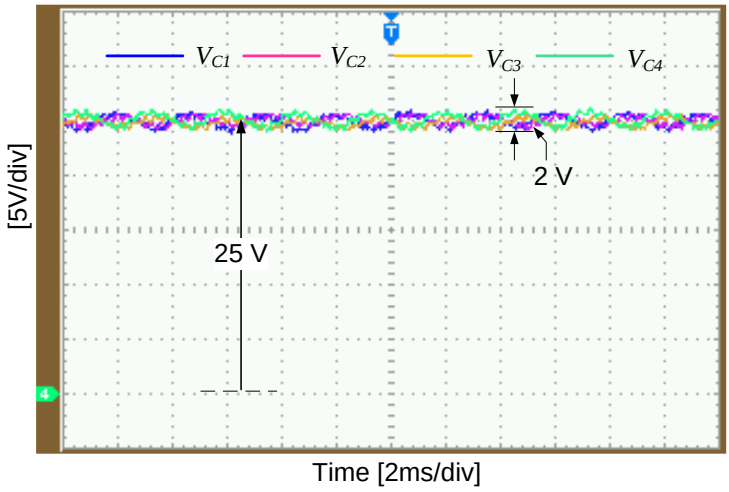
Figure 7-62 Experimental setup three-phase Type-1 5L RSS MPCI with RL load.

7.6.1 Performance of Type-1 5L RSS MPCI with VV-based Method:

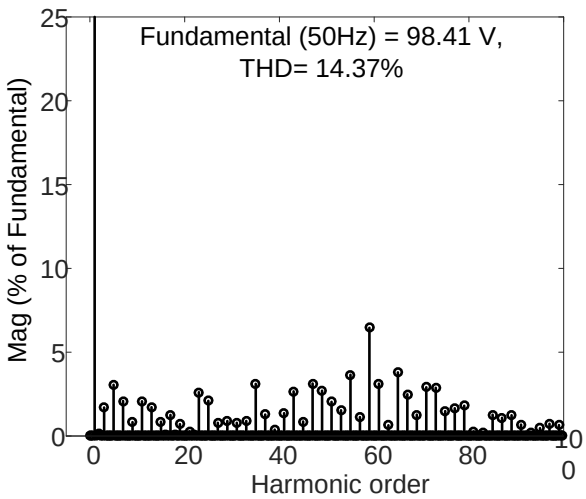
Figure 7-62 shows the experimental setup of Type-1 5L RSS MPCI build with 3L NPCI and two half bridge modules. Figure 7-63 and Figure 7-65show the experimental results obtained at two modulation indices m=0.98 and m=0.86 respectively. Due to the unavailability of voltage vectors at the outermost hexagon of SVD of Type-1 5L RSS MPCI discussed in Section 6.11.1, the line voltage waveforms are slightly more distorted compared to the 4L RSS MPCI for the modulation index m=0.98. However, the current distortion is approximately.



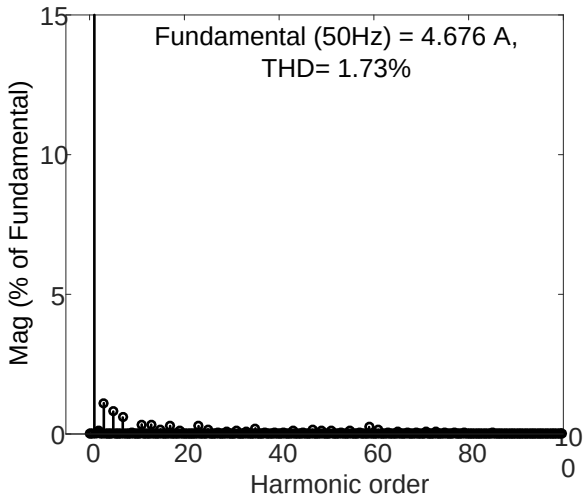
(a)



(b)

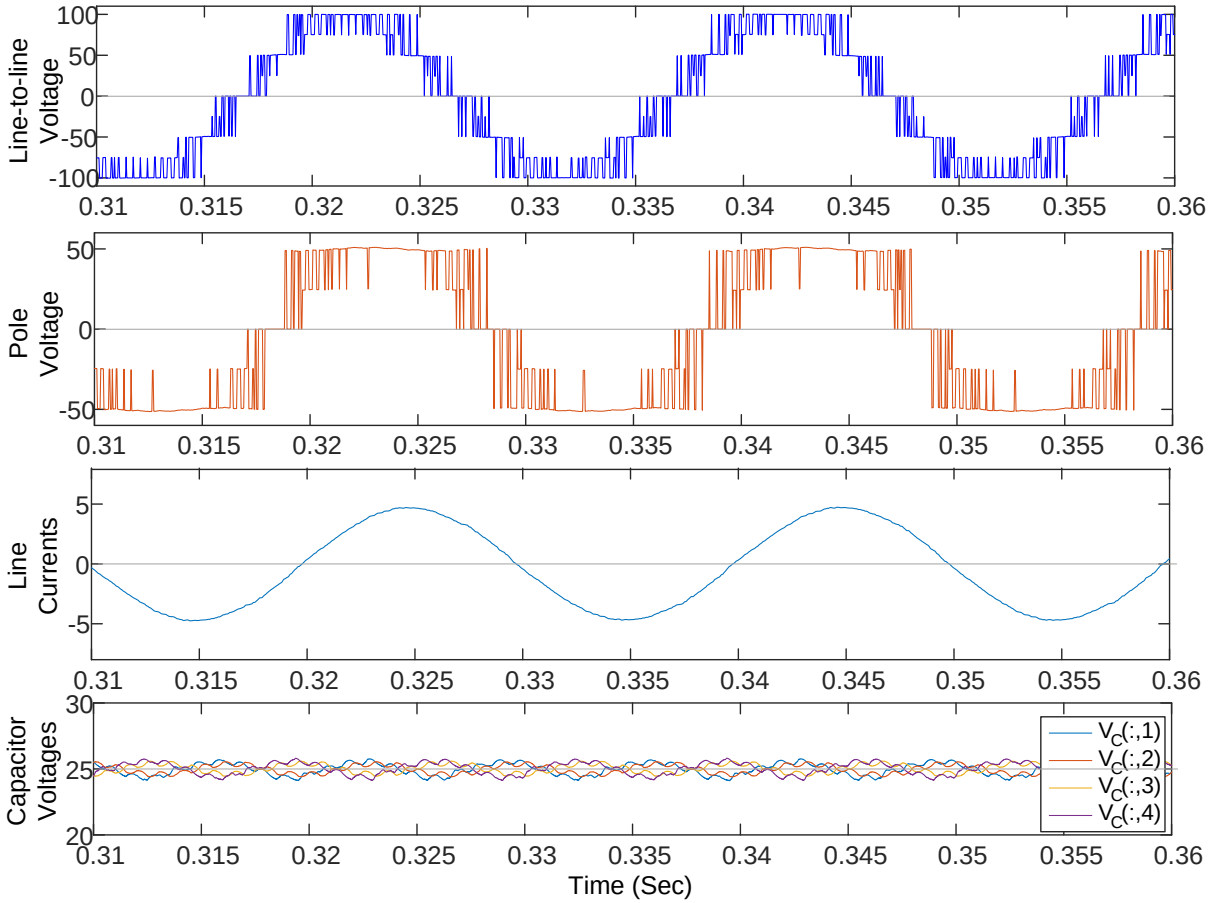


(c)

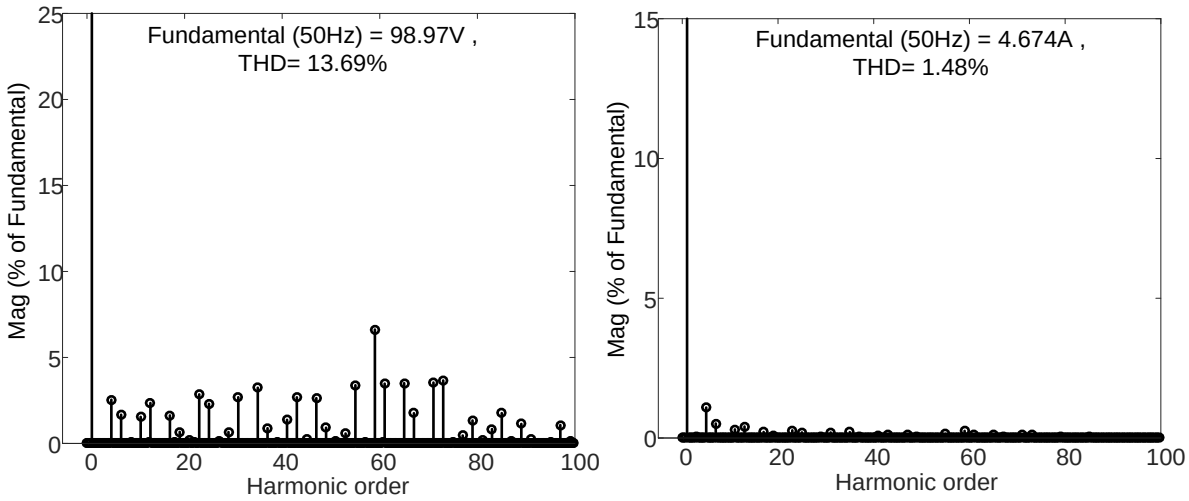


(d)

Figure 7-63 Experimental results of Type-1 5L RSS MPCI with VV modulation for m=0.98 (a) AC side waveforms, (b) Switching signals, (c) Voltage harmonic spectrum and (d) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).

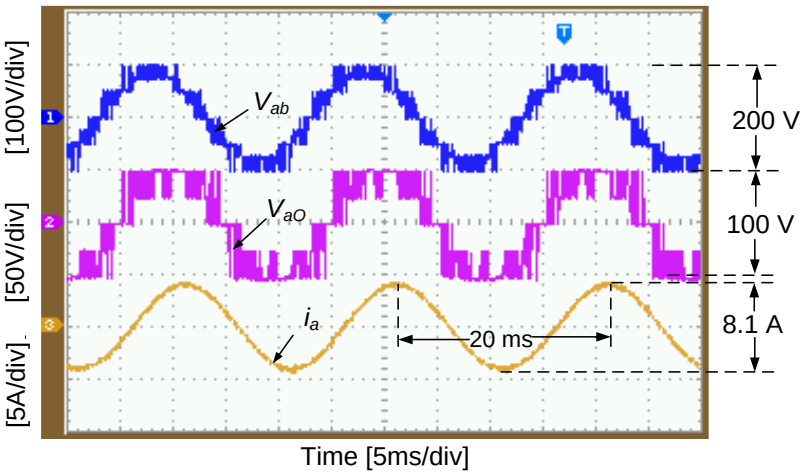


(a)

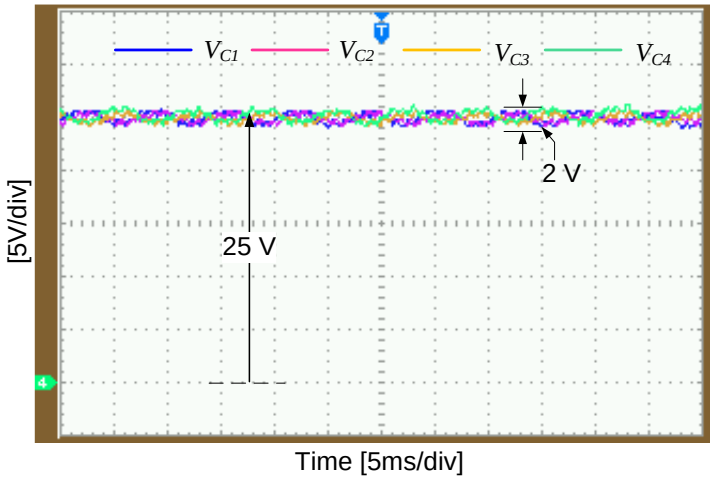


(b) (c)

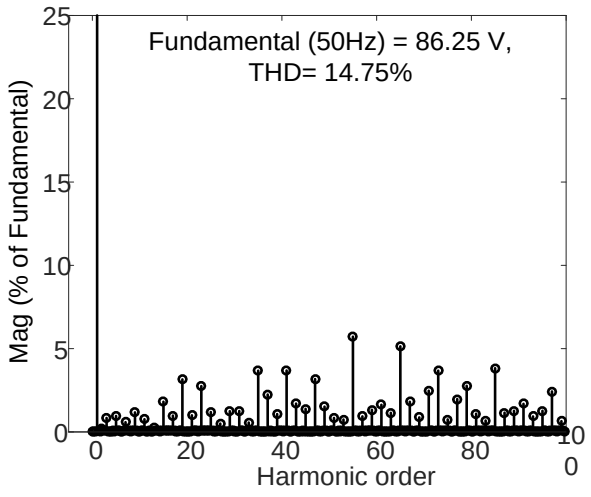
Figure 7-64 Simulation results of Type-1 5L RSS MPCI with VV modulation for m=0.98 (a) Voltage and current waveforms, (b) Voltage harmonic spectrum and (c) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).



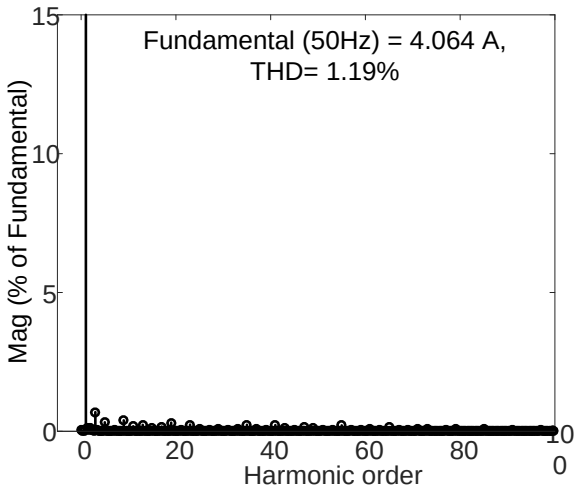
(a)



(b)

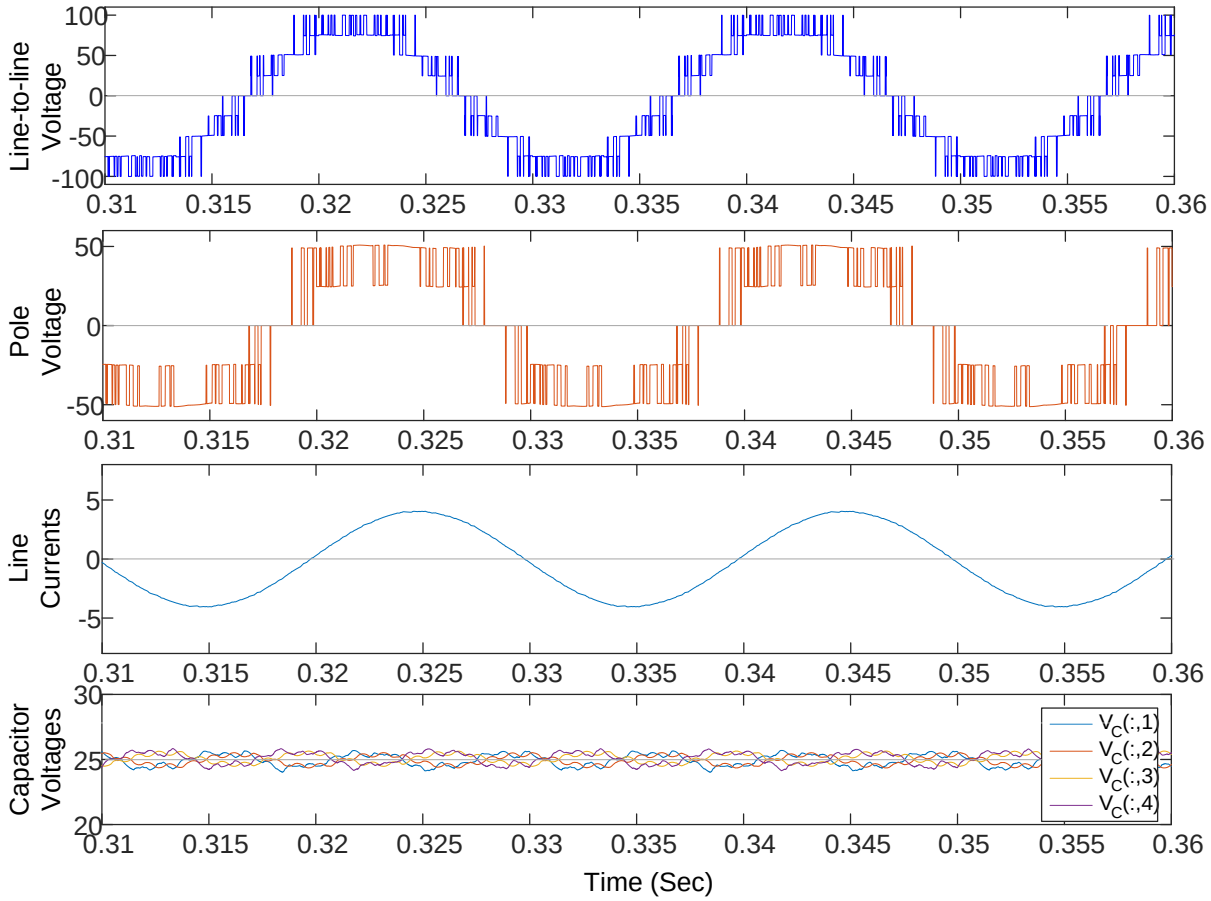


(c)

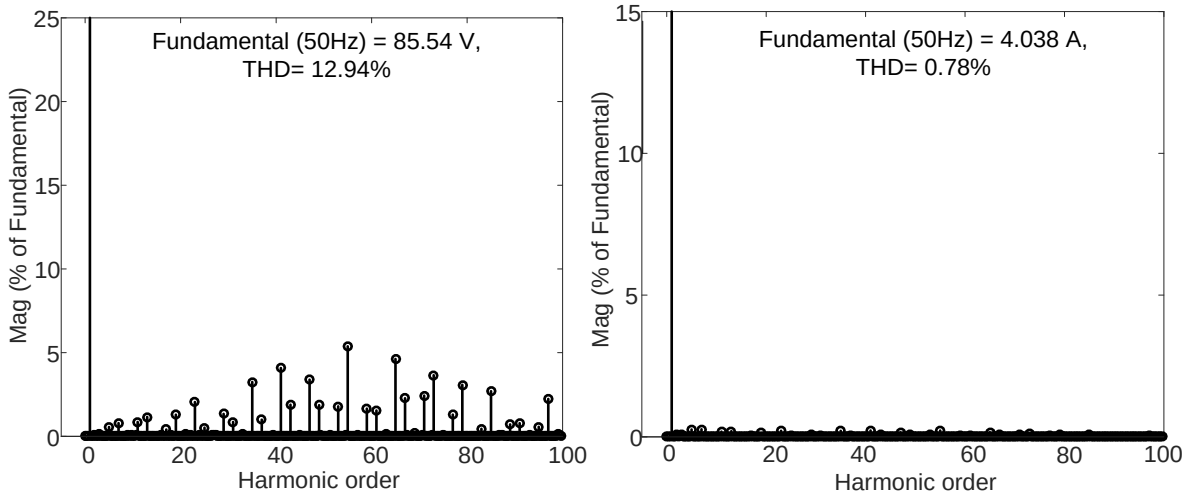


(d)

Figure 7-65 Experimental results of Type-1 5L RSS MPCI with VV modulation for m=0.86 (a) AC side waveforms, (b) Switching signals, (c) Voltage harmonic spectrum and (d) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).



(a)



(b) (c)

Figure 7-66 Simulation results of Type-1 5L RSS MPCI with VV modulation for m=0.86 (a) Voltage and current waveforms, (b) Voltage harmonic spectrum and (c) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).

Table 7-7 summarizes the performance of the Type-1 5L RSS MPCI with VV-based modulation method for two modulation indices.

Table 7-7 Comparison of Experimental and downscaled simulation results of Type-1 5L RSS MPCI VV-based modulation method

Performance Parameter		Modulation index (m)	
		0.98	0.86
Line-to-line Voltage (V) (Peak)	Experimental	98.41	86.25
	Simulation	98.97	85.54
% THD of Line-to-line Voltage %	Experimental	14.37	14.75
	Simulation	13.69	12.94
Line Current (A) (peak)	Experimental	4.676	4.067
	Simulation	4.674	4.038
% THD of Line Current	Experimental	1.73	1.19
	Simulation	1.48	0.78
Capacitor Voltage Ripple (V)	Experimental	2	2
	Simulation	1.8	1.8

7.6.2 Performance of Type-2 5L RSS MPCI with VV-based Method:

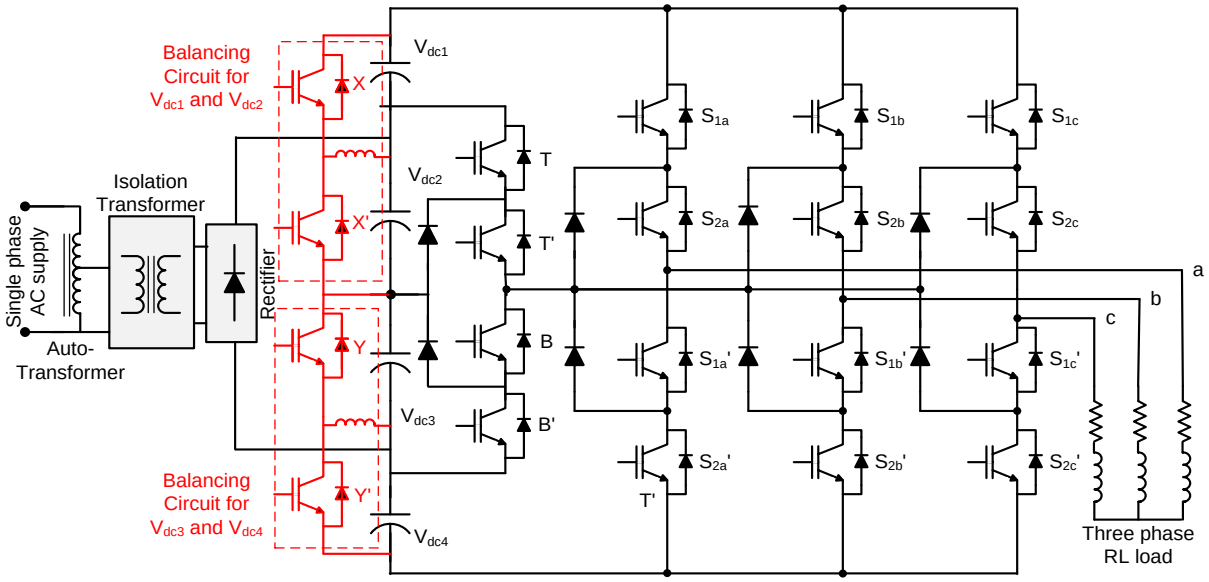
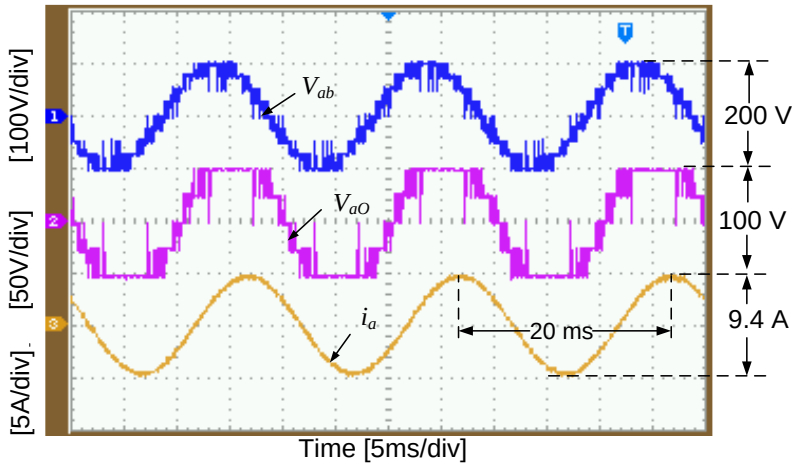


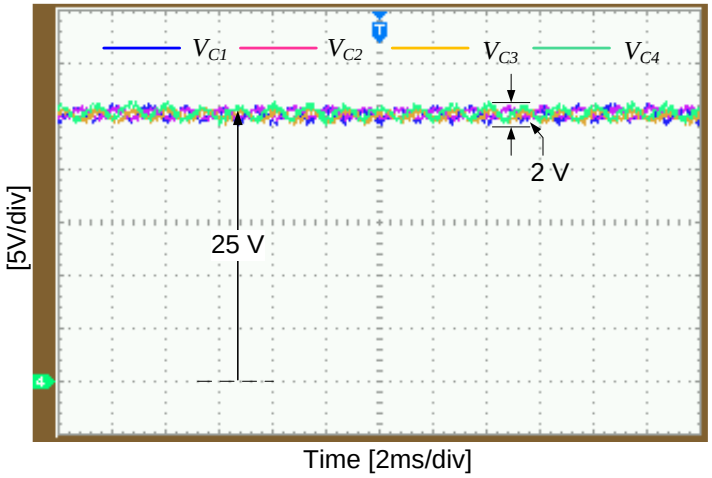
Figure 7-67 Experimental setup three-phase Type-2 5L RSS MPCI with RL load.

Figure 7-67 shows the experimental setup of Type-2 5L RSS MPCI build with four 3L NPCI modules. Figure 7-68 and Figure 7-70 show the experimental results obtained at two modulation indices m=0.98 and m=0.86 respectively. From the discussion presented in Section 6.11.2, all the voltage vectors are present in the SVD of Type-2 5L RSS MPCI, as a result the performance is similar to the conventional 5L VSI for higher modulation indices. This is evident from the experimental results presented in Figure 7-68 for the modulation index m=0.98.

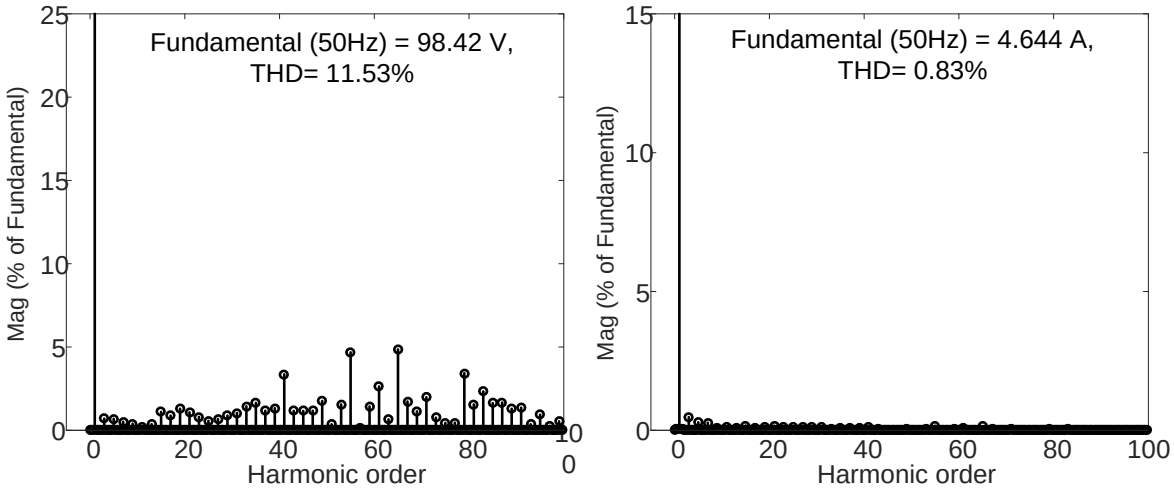
The experimental results obtained at the modulation index m=0.86 are shown in Figure 7-70. It is observed that the voltage waveforms produce additional voltage. This due to selection of virtual vectors for longer durations by the modulation algorithm to compensate the unavailable voltage vectors. Therefore, the experimental results obtained are in good agreement with theory and simulation results.



(a)

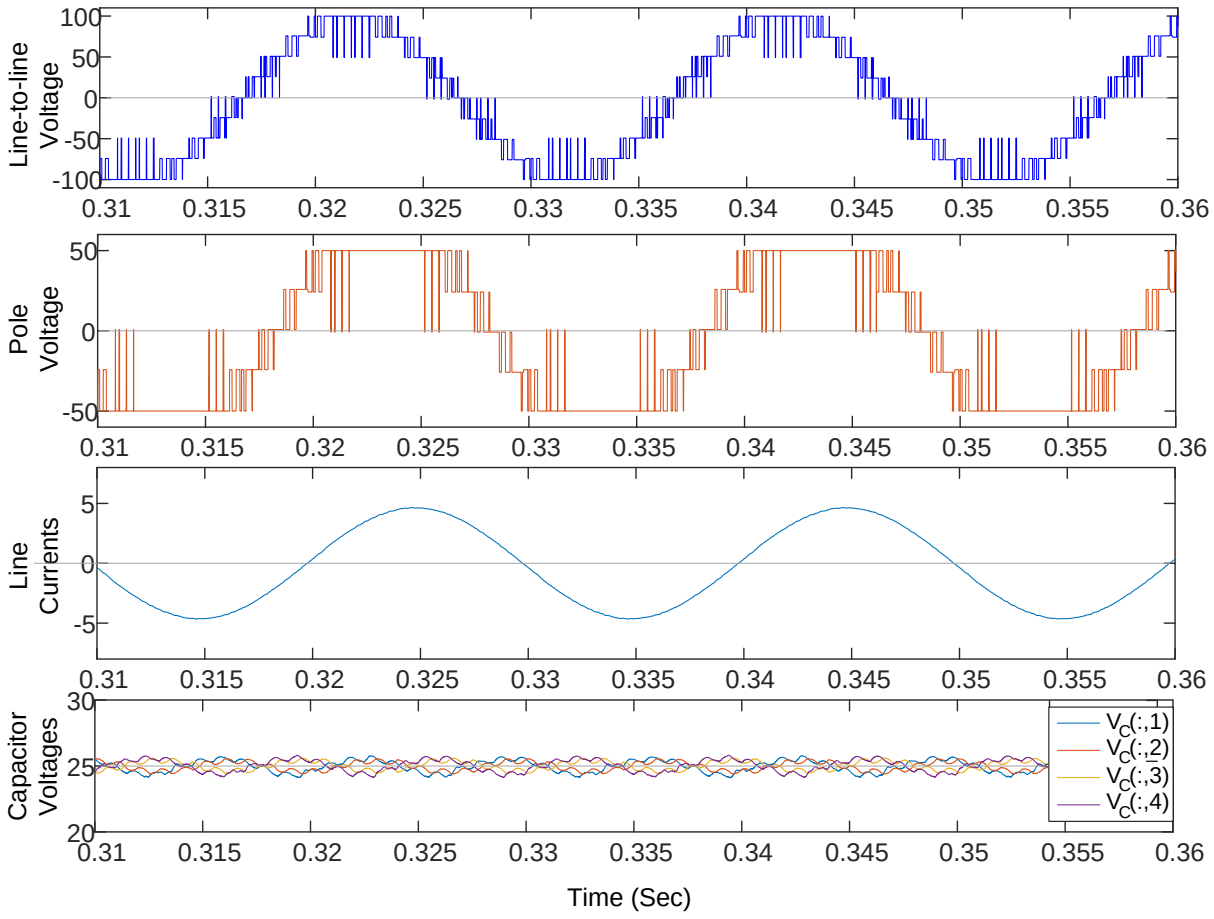


(b)

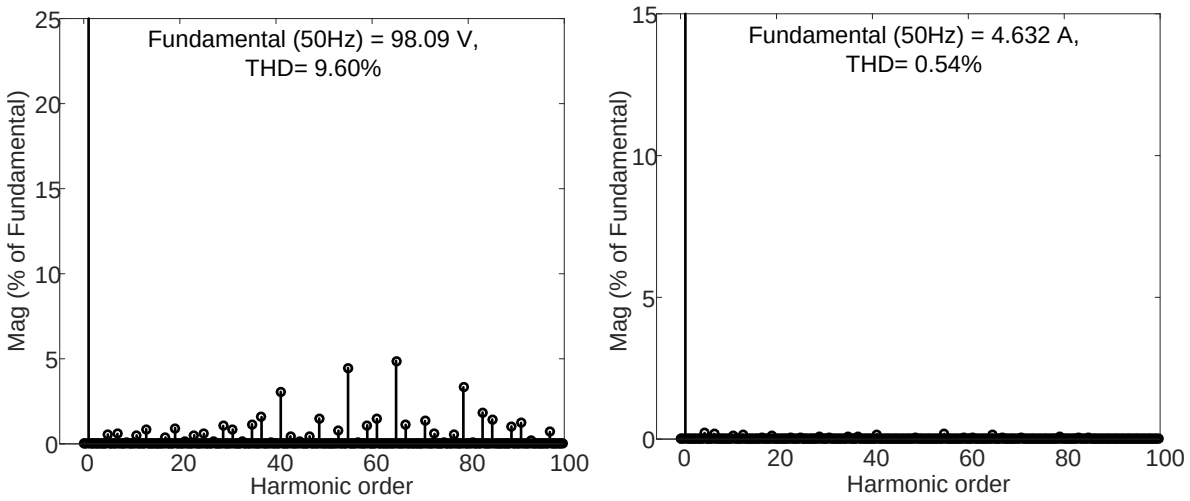


(c) (d)

Figure 7-68 Experimental results of Type-2 5L RSS MPCI with VV modulation for m=0.98 (a) AC side waveforms, (b) Switching signals, (c) Voltage harmonic spectrum and (d) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).

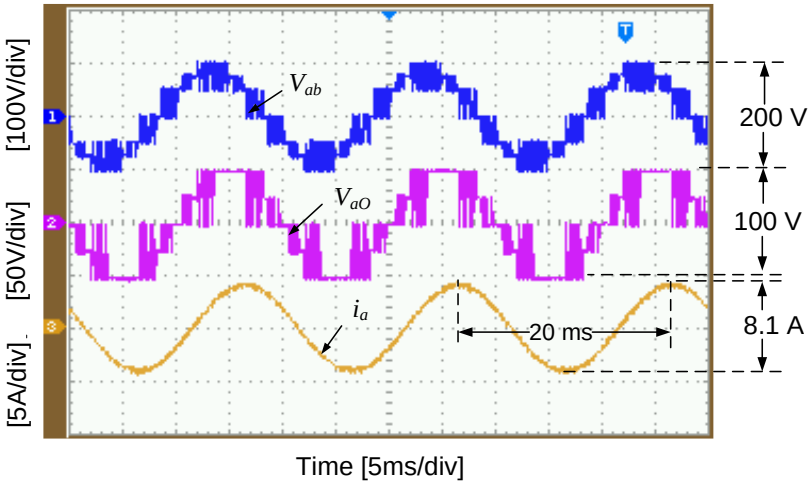


(a)

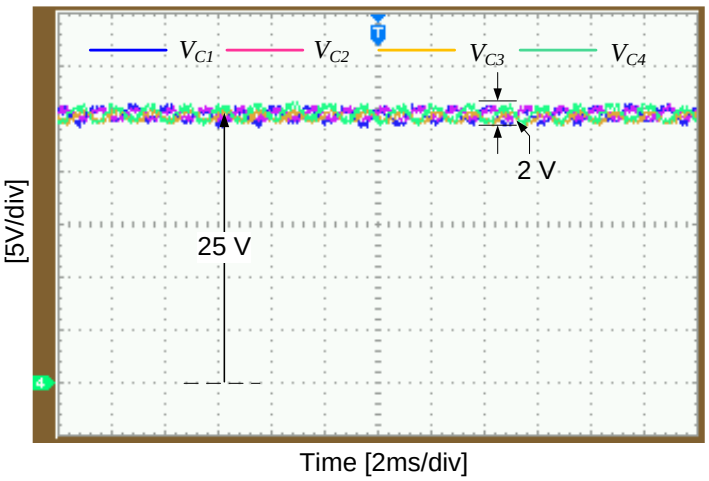


(b) (c)

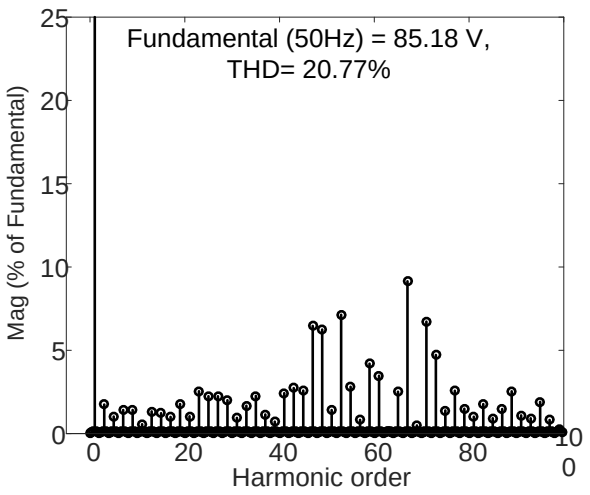
Figure 7-69 Simulation results of Type-2 5L RSS MPCI with VV modulation for *m=0.98* (a) Voltage and current waveforms, (b) Voltage harmonic spectrum and (c) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).



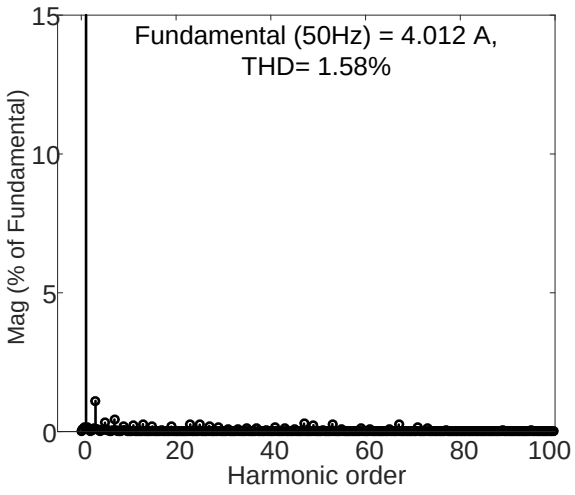
(a)



(b)

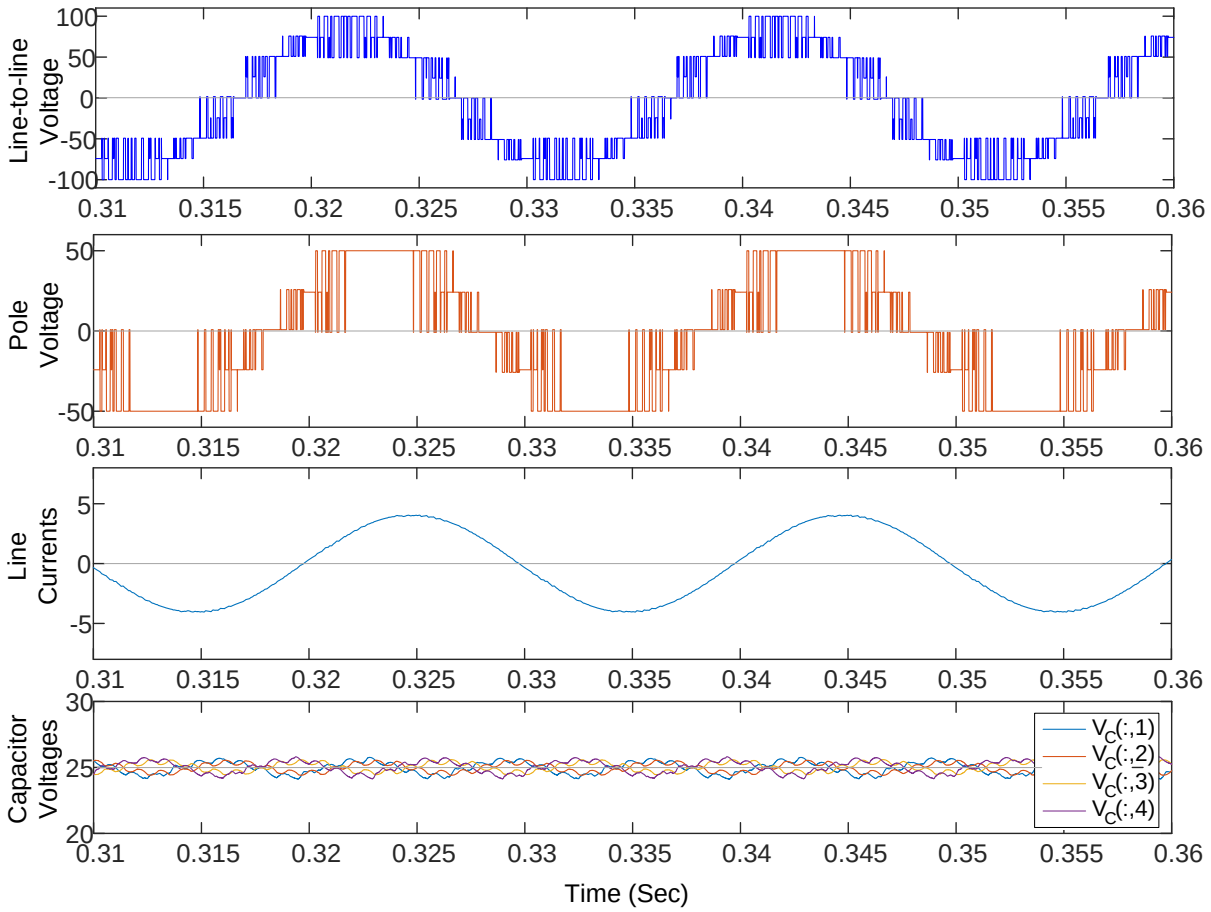


(c)



(d)

Figure 7-70 Experimental results of Type-2 5L RSS MPCI with VV modulation for m=0.86 (a) AC side waveforms, (b) Switching signals of hybrid 2/3L NPCI, (c) Voltage harmonic spectrum and (d) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).



(a)

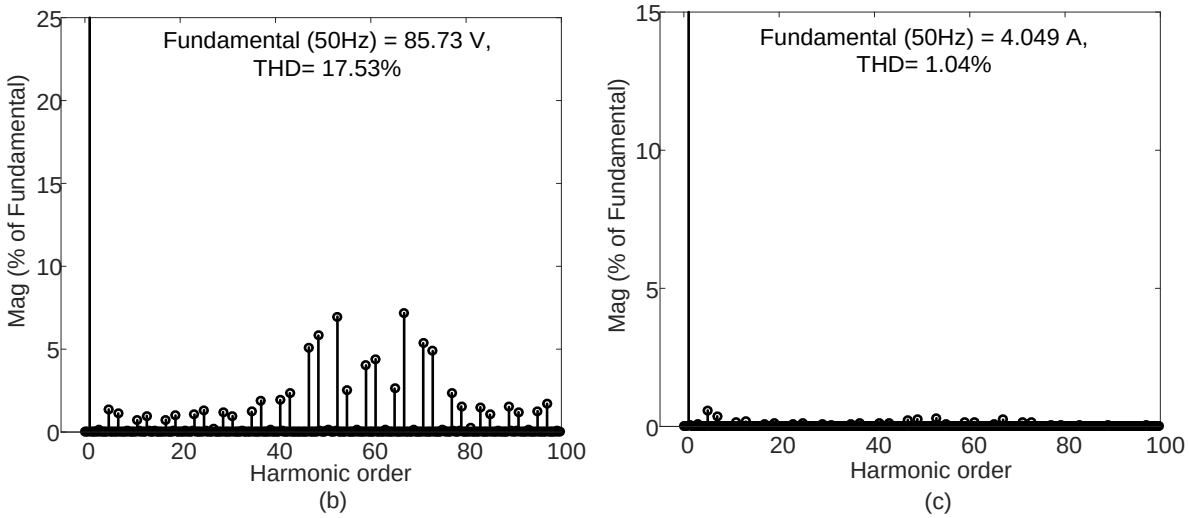


Figure 7-71 Simulation results of Type-2 5L RSS MPCI with VV modulation for m=0.86 (a) Voltage and current waveforms, (b) Voltage harmonic spectrum and (c) current harmonic spectrum (when load R=10 Ω and L=15 mH per phase).

Table 7-8 summarizes the performance of the Type-2 5L RSS MPCI with VV-based modulation method for three modulation indices.

Table 7-8 Comparison of Experimental and downscaled simulation results of Type-2 5L RSS MPCI VV-based modulation method

Performance Parameter		Modulation index (m)	
		0.98	0.86
Line-to-line Voltage (V) (Peak)	Experimental	98.42	85.18
	Simulation	98.09	85.73
THD of Line-to-line Voltage %	Experimental	11.53	20.77
	Simulation	9.6	17.53
Line Current (A) (peak)	Experimental	4.632	4.012
	Simulation	4.674	4.049
THD of Line Current %	Experimental	0.83	1.58
	Simulation	0.54	1.04
Capacitor Voltage Ripple (V)	Experimental	2	2
	Simulation	1.6	1.6

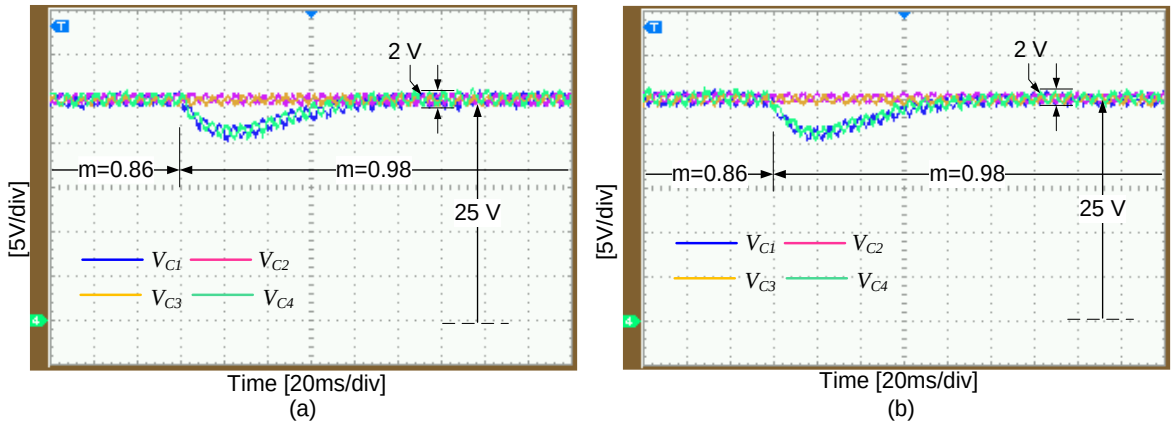


Figure 7-72 Capacitor voltage waveforms of 5L RSS MPCI topologies for the change on modulation index from m=0.86 to m=0.98. (a) Type-1 and (b) Type 2.

Figure 7-72 show the experimental capacitor voltage waveforms of 5L RSS MPCI topologies obtained for steady state an transient conditions for the change in the modulation index. The voltage 25V across series connected capacitors V_{dc2} and V_{dc3} are transformed to V_{dc1} and V_{dc4} respectively using the balancing circuits shown in Figure 7-62 and Figure 7-67.

7.7 Conclusion:

In this chapter, the detailed descriptions for the design and development of laboratory prototype MPCI topologies have been given. lGBTs are used as switching devices for implementation of prototype VSI topologies. RT-Lab, from Opal-RT Technologies is used as real-time hardware-in-loop controller to generate gate pulses for IGBTS in real-time. The different hardware components as required for the proper operation of experimental set-ups such as pulse amplification, isolation and dead-band circuits, voltage and current sensor circuits, loads have been designed, developed and interfaced with RT-Lab real time controller.

The performance of 3L NPCI is evaluated in detail for different NTV, non-MTV and hybrid modulation methods in the entire range of modulation for different load conditions. The NPCI operation with all the modulation algorithms is found satisfactory under steady state as well as transient conditions. It is found that the experimental results are in good agreement with the theoretical analysis discussed in chapter 3 and chapter 4.

In order to verify the theoretical and simulation studies of the hybrid2/3L NPCI, 4L and 5L RSS topologies with MPCI structure, prototype models of these topologies are developed in the laboratory and experimentation is carried out at reduced voltage of 100V (total DC link) and a lagging power factor load using R=10 Ω and L=15mH.

The two modulation algorithms derived from the non-NTV modulations of 3L NPCI discussed in chapter 5 are executed on hybrid 2/3L NPCI prototype for experimental validation. Comparing the experimental results obtained with these modulation schemes, it is confirmed that (i) The STV-based modulation is superior compared to the VV-based method, (ii) The VV-based method and STV-based modulations nearly coincide for modulation indices closer to unity. The conclusions are in good argument with the theory and simulation results previously discussed. The hybrid 2/3L NPCI is also verified with unequal DC voltage sources across each capacitor voltages. The obtained experimental results show the successful elimination of the unbalance effect in the AC side waveforms thereby validating the modulation algorithm for unequal DC voltage sources.

The 4L and 5L RSS MPCI topologies discussed in chapter 6 are also tested experimentally for validating the proposed modulation algorithms. The 4L RSS MPCI is tested for three modulation indices m=0.98, m=0.86 and m=0.75 to verify the effect of absent voltage vector in the voltage waveforms. The obtained experimental results clearly show the additional voltage steps caused by the utilization of virtual vector similar to the simulation results previously discussed. The STV-based modulation algorithm is tested and experimental results are obtained. The performance boost compared to the VV-based method is clearly evident from the experimental results which conforms the theorical and simulation results. Finally, the two 5L RSS MPCI topologies are

tested with the VV-based modulation for higher modulation indices. Experimental results justify the theoretical analysis and simulation results.

Chapter 8: CONCLUSIONS AND FUTURE SCOPE

[The main conclusions of the presented work and possible future research have been summarized in this chapter.]

8.1 Conclusions

In recent years, there has been an increasing interest in electrical power generation from distributed energy sources like PV, Fuel-cell and Wind energy. A power conversion system is essential in such applications for grid-integration and standalone operation. Two-level voltage source inverters (VSIs) encounter few limitations in such applications as they require series connection of several low voltage distribution energy sources to meet the required power and voltage level. This results in loss of control over individual sources and leads poor utilization of available energy.

Multilevel inverters (MLIs) enable direct connection of several low voltage sources and allows independent control for achieving maximum utilization of available energy. This feature of MLI can avoid high gain DC-DC converters and transformers while integrating distributed energy sources. However, major challenges for the MLIs include the complexity, cost and reliability due to increased power semiconductor device (PSD) count. In the present work, the newly proposed MLIs were evaluated based on various factors like (1) possibility of back-to-back conversion structure; (2) required number of isolated DC sources; (3) requirement of symmetrical/asymmetrical DC sources; (4) possibility of operation with isolated/non-isolated DC sources; (5) requirements for single phase and three-phase applications; etc. It was found that the multipoint camped inverter (MPCI) requires least number of isolated DC sources for multiphase operation and therefore ideal choice for high power appellations.

The selection of voltage vectors along with the switching sequence MPCI topologies will play key role for achieving various functionalities of the like: capacitor voltage balancing, switching loss reduction, power quality, etc. Depending on the type voltage vectors selected, the modulations were classified as nearest three vector (NTV) and non-nearest three vector (non-NTV) modulations. NTV and non-NTV methods typically require different algorithms for implementation as they use independent choice of voltage vectors. In general, non-NTV methods are more involved than NTV methods and they require complex algorithms with higher trigonometric computations. The NTV algorithms are also not suitable for non-NTV methods as they comprise non-identical and non-equilateral sub-triangle regions in each sector of SVD. This results in increased execution time and computational burden on the processors.

This thesis investigates the three-phase MPCI topologies and modulation strategies for the possible applications including renewable energy grid interface, energy storage system, motor

drives and tractions, energy control center for smart grid and micro-grids. The key challenges of the power conversion system are identified as power circuit complexity, modulation algorithms and power quality for MPCI topologies. The major conclusions derived from this work are summarized as follows.

- A new SVM algorithm was proposed for MPCI based topologies to implement NTV and non-NTV methods without using the complex trigonometry and coordinated transformation. The proposed algorithm only requires equivalent 2L SVD duty ratios which are readily available from reference phase or line-to-line voltages and hence, no additional calculations are required. An NTV modulation and two non-NTV modulations were implemented on 3L neutral pint clamped inverter (NPCI) using the proposed modulation algorithm to eliminate the low frequency neutral pint (NP) voltage oscillations for entire range of modulation index and power factors. It was concluded that both NTV and non-NTV methods are capable of eliminating the NP voltage oscillations for lower modulation index $m \leq 0.5$. However, as the modulation index increases, non-NTV method must be used to suppress the NP voltage oscillations despite increased switching frequency and THD. It was also observed that the increase in voltage THD is due to the high frequency harmonic content which doesn't significantly increase the current THD.
- The hybrid modulation approach based on redistribution of NTV duty ratios has significantly improved the performance of 3L NPCI for all modulation indices and power factors. The selection criteria depends on NTV duty ratios and phase currents which decides either NTV or non-NTV operation of 3L NPCI, and avoids abrupt change over. The detailed study and comparative analysis of hybrid NTV-STV modulation is performed. It was observed that hybrid modulation effectively reduces the voltage THD and power losses by maximizing the NTV operation in the fundamental cycle. A new simplified STV (SSTV) is also developed and combined with NTV to form hybrid NTV-SSTV modulation which found to be superior in terms of switching frequency and THD. This hybrid modulation is also found to be simple for implementation compared to other hybrid modulations.
- A new hybrid 2/3L NPCI topology can significantly reduce the power semiconductor device (PSD) count. The topology requires only ten active switches compared to 12 active switches and 6 clamping diodes in 3L NPCI and hence, it minimises the cost and complexity. Total of 21 switching states are possible which are distributed over 13 locates in space vector diagram (SVD) of hybrid 2/3L NPCI. Two generalised modulation strategies based on non-NTV modulation were proposed and compared. It was found that, the performance of the hybrid 2/3L NPCI is in between the 2L and 3L inverters since the medium magnitude phase is switched as 2L inverter, while, the minimum and

maximum magnitude phases switch as 3L NPCI. A new virtual vector-based modulation was proposed to operate hybrid 2/3L NPCI with Z-source network. A new switching sequence was developed by including two small vectors for incorporating upper and lower shoot through states without increasing the number of commutations. When the DC link is excited with different sources across each capacitor or hybrid energy storage system like (battery/super capacitor), another virtual vector modulation was implemented for achieving balanced three phased current with minimum distortion and number of commutations.

- A modified T-Type MPCI was constituted based on half bridge modules and it has advantage in terms of total voltage blocking required. The topology can be easily extended to higher voltage levels by adding half bridge modules at top and bottom or at the clamping points. The topology requires equal number of active switches compared to other MPCI counterparts but does not need clamping diodes and bidirectional switches.
- Reduced switching state (RSS) MPCI topologies were derived from the modified T-type MPCI in order to reduce the active switch count significantly. It was found that the reduction of active switches diminishes the number of available switching states in MPCI topologies. The position of available switching states in SVD of a given RSS MPCI depends on i) total number of switching devices and ii) structure of the RSS MPCI. Therefore, two types of RSS MPCI topologies namely Type-1 and Type-2 are investigated. It was found that Type-1 and Type-2 RSS MPCI topologies eliminate the switching states corresponding to higher and medium modulation index range respectively. Therefore, the performance of Type-2 was found to be superior at higher modulation index range compared to Type-1 RSS MPCI topologies. Further analysis of the RSS MPCI topologies revealed that the Type-1 topologies outperform Type-2 in terms of total voltage blocking capability compared to topologies. Thus, a proper RSS MPCI topology can be chosen based on the parameters like operating conditions, cost, etc.

8.2 Future Scope

The research work presented in this thesis discloses a number of issues that could be further investigated. This work is presumed to be an important basis for the future research work as briefly pointed below.

- Performance investigation of 3L NPCI in the overmodulation region for capacitor voltage balancing, THD, etc need to be investigated.
- Investigation on modulation strategies for hybrid 2/3L NPCI topology to eliminate low frequency NP voltage oscillations in the higher modulation range need to performed.

- Detailed investigation on power loss distribution among the switching devices of hybrid 2/3L NPCI and other RSS MPCI topologies with proposed modulation strategies is to be carried out.
- Analysis of RSS MPCI topologies for unequal DC-source voltages need to be investigated.

LIST OF PUBLICATIONS

List of Journal Papers

1. Narendrababu A and P. Agarwal, "Nearest and Non-Nearest Three Vector Modulations of NPCI Using Two-Level Space Vector Diagram—A Novel Approach," in IEEE Transactions on Industry Applications, vol. 54, no. 3, pp. 2400-2415, May-June 2018.

2. Narendrababu A and P. Agarwal, "Hybrid modulation strategy for eliminating low-frequency NP voltage oscillations in NPC using redistribution of NTV duty ratios," in *IET Power Electronics*, vol. 10, no. 12, pp. 1504-1517, 2017.

3. N. Yalla, Narendrababu A and P. Agarwal, "A New Three Phase Multi-Point Clamped 5L-HPFC With Reduced PSD Count and Switch Stress," in IEEE Transactions on Industrial Electronics. DOI: 10.1109/TIE.2019.2910030.

4. Narendrababu A and P. Agarwal, “Optimal Voltage Vector Selection for a Four Level Reduced Switching State Voltage Source Inverter” IEEE Journal of Emerging and Selected Topics in Power Electronics (communicated).

List of Patents

1. P. Agarwal, N. Yalla and Narendrababu A. 2019. NPA: A Multi-level high power factor AC-DC converter. Indian patent application 201911014389. Patent Pending.

List of Publications in International Conferences

1. Narendrababu A and P. Agarwal, "A five level diode clamped rectifier with novel capacitor voltage balancing scheme," IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Mumbai, India, 16-19 Dec. 2014.
2. Narendrababu A and P. Agarwal, "Space vector modulation for three-level NPC inverter using two-level space vector diagram," IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Trivandrum, India 14-17 Dec. 2016.
3. Narendrababu A, Naveen Yalla and P. Agarwal, “A Modified T-type Single Phase Five-Level Inverter with Reduced Switch Voltage Stress” International Conference on Power, Instrumentation, Control and Computing (PICC), Thrissur, India, 18-20 Jan. 2018.
4. Narendrababu A and P. Agarwal, " Virtual Vector Modulated Hybrid 2/3-Level Z-source VSI for PV Applications," IEEE 9th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Charlotte, USA, 25-28 June. 2018.

5. Naveen Yalla, Narendrababu A, and P. Agarwal," A New 5L-UHPFC with reduced part count for wind energy integration," IEEE 9th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Charlotte, USA, 25-28 June. 2018.

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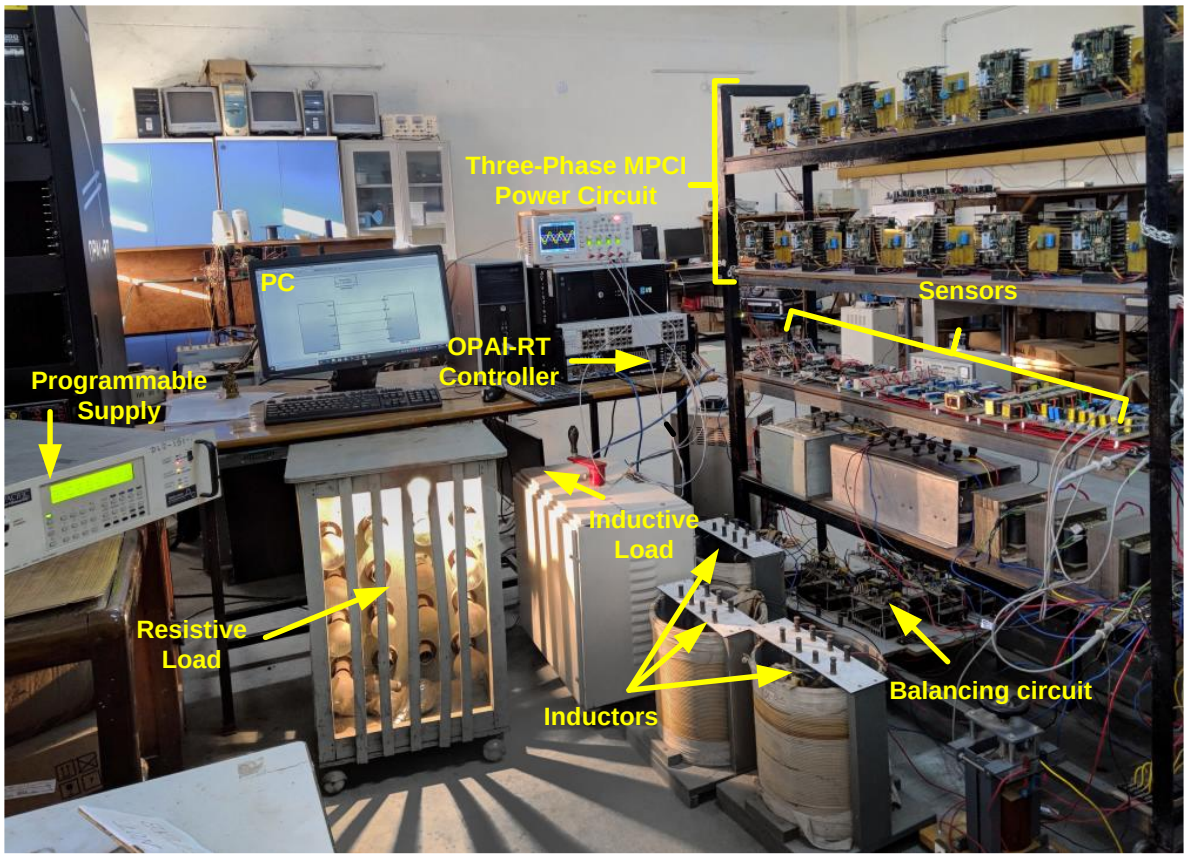

Complete hardware set-up in laboratory