ANALYSIS AND CONTROL OF BIDIRECTIONAL DC-DC CONVERTERS

Ph.D. THESIS

by

GURUSWAMY K P

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE – 247667 (INDIA)
DECEMBER, 2018

ANALYSIS AND CONTROL OF BIDIRECTIONAL DC-DC CONVERTERS

A THESIS

Submitted in partial fulfilment of the requirements for the award of the degree

of

DOCTOR OF PHILOSOPHY

in

ELECTRICAL ENGINEERING

by

GURUSWAMY K P

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE – 247667 (INDIA)
DECEMBER, 2018

INDIAN INSTITUE OF TECHNOLOGY ROORKEE
ROORKEE

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in this thesis entitled **"ANALYSIS AND CONTROL OF BIDIRECTIONAL DC-DC CONVERTERS"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electrical Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from July, 2010 to December, 2018 under the supervision of Dr. S. P. SINGH, Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

Signature of the Candidate

This is to certify that the above statement made by the candidate is correct to the best of my (our) knowledge.

Signature of the Supervisor

The Ph.D Viva-voce Examination of Guruswamy K P, Research Scholar,

has been held on ----------

Chairman, SRC **Signature of External Examiner**

This is to certify that the student has made all the corrections in the thesis

Signature of the Supervisor **Head of the Department**

Date:08/12/2018

ABSTRACT

This thesis introduces the design and implementation of 350W conventional bidirectional dc-dc converter with hard switching operation. A more accurate modeling of non-ideal elements of bidirectional dc-dc converter (BDDC) using state space averaging technique is presented. Steady state and small signal analytical expressions are derived individually for both boost and buck mode of BDDC in continuous conduction mode. Type III error amplifier for boost mode and PID controller for buck mode are designed to achieve the desired loop bandwidth of the converter system. Transient performance of the converter is simulated for both boost mode and buck mode to achieve precise regulation against the line and load abrupt change using MATLAB/SIMULINK software package. Hardware prototype of converter is implemented and tested for performance evaluation. The dynamic performance of the converter is then tested against the load variation. With the experimental measurement, the corresponding design has been verified. Results show that the model is accurate and offers a significant improvement in the computation. Ringing effect due to parasitic impedance across MOSFET switching device at 100 kHz is substantially reduced by proper selection of snubber circuit elements and sophisticated gate drive mechanism.

Analysis of three-phase interleaved bidirectional dc-dc converter (IBDDC) in continuous conduction mode using state space averaging method has been presented in this thesis. Analytical expression of small signal control to duty ratio has been derived for the three-phase IBDDC operates either in boost mode or in buck mode. Two or more identical converters are connected in parallel to reduce both input and output ripple currents, hence size of the capacitor decrease. Non-isolated three-phase IBDDC offers many advantages like equal current sharing capability among individual converter, increased output power, better utilization of switches, lower switching loss, increased efficiency, fast dynamic response, lower per phase ripple, reduced input and output ripple. The basic operation of three-phase IBDDC, steady state, small signal analysis, and voltage mode control of IBDDC are clearly described. Simulation of type 3 error amplifier and fuzzy logic controller based three-phase IBDDC is carried out in Simulink/SimPowerSystem and load dynamic performance is compared with the experimental results.

ACKNOWLEDGEMENTS

I take this opportunity to express my sincere gratitude my august guide Dr. S. P. Singh, Professor, Electrical Engineering Department, Indian Institute of Technology, Roorkee, for their proficient and enthusiastic guidance, advice and encouragement, which were the constant source of inspiration for the completion of this research work.

Their painstaking support and exhaustive involvement in preparation of manuscript, conduction of the experimental investigations and simulation studies are gratefully acknowledged. I sincerely appreciate their pronounced individualities, humanistic and warm personal approach, which has given me strength to carry out this research work on steady and smooth course. I humbly acknowledge lifetime's gratitude to them.

My sincere thanks are also due to Prof. M. K. Vasantha, Prof. N.P. Padhy, Prof. K. S. Hariprasad, Prof. Vinay Pant and Prof. M.K. Pathak for their extending moral support and technical discussions as and when requiring during research work.

I acknowledge my sincere gratitude to the Quality Improvement Program (QIP) of MHRD Govt. of India. The research work is carried out under this scheme. I also acknowledge my appreciation to Coordinator, QIP Centre, Indian Institute of Technology, Roorkee, for their kind co-operation. I express my deep sense of gratitude to the Head, Electrical Engineering Department, Indian Institute of Technology, Roorkee, for providing the excellent laboratory and computing facilities of the department for the research work.

My hearty gratitude to the Vice-chancellor, Registrar Bangalore University, Bengaluru, and H.O.D (Electrical Engineering) U.V.C.E, Bengaluru (my parent Institution) for sponsoring me for Ph.D work. Special thanks are due to my colleagues for extending help during my stay at Roorkee.

I am thankful to the technical staff of computer controlled drives lab Shri Saadi Ram, and other staff member of workshop for their timely co-operation and needful help. Thanks are also due to all those who helped me directly and indirectly for the completion of the work.

I am lucky to get the helping hands from my wife Divya and loving son Jeevith. Even though they have missed me a lot during my research work, they waited patiently for the completion of the work. I appreciate them for the kind of support extended. No words can adequately express my gratitude to them.

(**Guruswamy K P)**

CONTENTS

LIST OF ABBREVIATIONS

Abbreviation	Description
ADC	Analog to Digital Converter
BDDC	Bidirectional DC-DC Converter
CCM	Continuous Conduction Mode
DAB	Dual Active Bridge
DAC	Digital to Analog Converter
dB	Decibel
DCM	Discontinuous Conduction Mode
DPWM	Digital Pulse Width Modulator
DSO	Digital Storage Oscilloscope
DSP	Digital Signal Processor
EA	Error Amplifier
EMI	Electro-Magnetic Interference
ESR	Equivalent Series Resistance
IBDDC	Interleaved Bidirectional DC-DC Converter
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
MOSFET	Metal Oxide Field Effect Transistor
PWM	Pulse Width Modulator
SMPS	Switch Mode Power Supply
SMPC	Switch Mode Power Converter
SSA	State Space Averaging
UPS	Uninterruptible Power Supply

LIST OF SYMBOLS

Symbols	Descriptions
A_p	Area product
I_{LB}	Average inductor current in boost mode of BDDC
I_L	Average inductor current in buck mode of BDDC
I_{o1}	Average load current for buck mode 3-Phase IBDDC
I_{o2}	Average load current for boost mode of 3-Phase IBDDC
I_2	Average load current in boost mode of BDDC
I_1	Average load current in buck mode of BDDC
I_{D1}	Average value of diode current in boost mode of BDDC
I_{D2}	Average value of diode current in buck mode of BDDC
D1	Boost mode diode of BDDC
D_1,D_2, D_3	Boost mode diodes of 3-Phase IBDDC
δ	Boost mode duty ratio of BDDC
$\delta 1$	Buck mode duty ratio of BDDC
D	Boost mode duty ratio in three-phase IBDDC
V_2	Boost mode output voltage
ΔI_{LB}	Boost mode ripple current
S_2	Boost mode switch
S_4, S_5, S_6	Boost mode switches of 3-Phase IBDDC
D2	Buck mode diode of BDDC
D_4, D_5, D_6	Buck mode diodes of 3-Phase IBDDC
$D^{'}$	Buck mode duty ratio of 3-phase IBDDC
V_1	buck mode output voltage
ΔI_L	Buck mode ripple current
S1	Buck mode switch of BDDC
S_1, S_2, S_3	Buck mode switches of 3-Phase IBDDC
v_c	Control voltage
K_c	Crest factor
L_{min}	Critical value of inductance
A_c	Cross section area of core
A_w	Cross section area of window

Symbols	Descriptions
a	Cross section area of wire gauge
f_c	Crossover frequency
J	Current density
$V_{\gamma1}$, $V_{\gamma2}$, $V_{\gamma3}$	Cut in voltage of D_1,D_2, D_3
$V_{\gamma4}$, $V_{\gamma5}$, $V_{\gamma6}$	Cut in voltage of D_4, D_5, D_6
d1,d2,d3,d4,d5,d6	Duration of 3phase IBDDC in boost mode
d_1^1,d_2^1,d_3^1,d_4^1,d_5^1,d_6^1	Duration of 3phase IBDDC in buck mode
E	Energy stored in inductor
v_e	Error voltage
R_{C1}	ESR of C_1
R_{C2}	ESR of C_2
v_f	Feedback voltage
V_{ref}	Fixed reference voltage
R_{f1}	Forward resistance of D_1
R_{f1},R_{f2},R_{f3}	Forward resistance of D_1,D_2, D_3
R_{f4},R_{f5},R_{f6}	Forward resistance of D_4,D_5, D_6
L	Inductor
i_{L1B}, i_{L2B}, i_{L3B}	Inductor currents for boost mode of 3-Phase IBDDC
i_{L1}, i_{L2} ,i_{L3}	Inductor currents for buck mode of 3-Phase IBDDC
L_1, L_2, L_3	Inductors of 3-Phase IBDDC
E_1	Input voltage in boost mode of BDDC
E_2	Input voltage in buck mode of BDDC
i_{LB}	Instantaneous inductor current in boost mode of BDDC
i_L	Instantaneous inductor current in buck mode
r	Internal resistance of L
r1,r2,r3	Internal resistance of L_1,L_2 and L_3
R_2	Load resistor in boost mode of BDDC
R_1	Load resistor in buck mode of BDDC
D_{max}	Maximum boost mode duty ratio
B_m	Maximum flux density
R_{2max}	Maximum load resistor in boost mode of BDDC
R_{1max}	Maximum load resistor in buck mode of BDDC

Symbols	Descriptions
$D_{1\min}$	Minimum buck mode duty ratio
$R_{2\min}$	Minimum load resistor in boost mode of BDDC
$C_{2\min}$	Minimum output capacitor in boost mode of BDDC
$C_{1\min}$	Minimum output capacitor in buck mode of BDDC
M	Mutual inductance
n	Number of phases
N	Number of turns
d_2	Off time duration of boost mode
d_2^1	Off time duration of buck mode
R_{on1},R_{on2},R_{on3}	On state resistance of S_1, S_2, S_3
R_{on4},R_{on5},R_{on6}	On state resistance of S_4, S_5, S_6
R_{DS1}	On state resistance of S_1
R_{DS2}	On state resistance of S_2
d_1	On time duration of boost mode
d_1^1	On time duration of buck mode
f_s	Operating frequency
i_{C2}	Output capacitor current in boost mode of BDDC
i_{C1}	Output capacitor current in buck mode of BDDC
C_2	Output capacitor in boost mode of BDDC
C_1	Output capacitor in buck mode of BDDC
v_{c1pp}	Peak to peak voltage across C_1
v_{c2pp}	Peak to peak voltage across C_2
I_m	Peak value of inductor current
I_{D1rms}	RMS value of diode current in boost mode of BDDC
I_{D2rms}	RMS value of diode current in buck mode of BDDC
I_{Lrms}	RMS value of inductor current
I_{C2rms}	RMS value of output capacitor in boost mode of BDDC
I_{C1rms}	RMS value of output capacitor in buck mode of BDDC
T_s	Switching period
v_{L1B}, v_{L2B}, v_{L3B}	Voltage across an inductors L_1,L_2,L_3 in boost mode
v_{L1}, v_{L2}, v_{L3}	Voltage across an inductors L_1,L_2,L_3 in buck mode
v_{C1}	Voltage across C_1

Symbols	Descriptions
v_{C2}	Voltage across C_2
v_{LB}	Voltage across inductor in boost mode
v_L	Voltage across inductor in buck mode
K_w	Window utilization factor

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1: INTRODUCTION AND LETRATURE REVIEW

[This chapter describes an overview of conventional bidirectional dc-dc converters, interleaved bidirectional dc-dc converters with switching scheme, modelling and control of bidirectional dc-dc converters. This chapter also presents a detailed literature review on non-isolated bidirectional dc-dc converter topologies, isolated bidirectional dc-dc converter topologies, modelling and control of bidirectional dc-dc converters. The scope of the research work has been highlighted and author's contributions are also presented in this chapter].

Switch mode power supply (SMPS) effectively regulates dc output voltage for a given unregulated dc input voltage. A SMPS offers many advantages like higher efficiency and power density compared to linear power supplies, which are operated in linear region with increased switching loss. SMPS consists of energy storage elements and solid-state devices. Energy storage elements include inductors and capacitors which are used for transfer of energy. Solid state elements include transistors and diodes, which are normally operated as switch. Topologies of SMPS are mainly buck derived or boost derived dc-dc converter.

Analog control technique is even good for the control of any topology of SMPS, but it changes the response of the system because of aging of components and temperature dependent characteristic. In order to overcome from the disadvantages of analog control technique, digital control technique is preferred because of higher immunity to temperature, flexibility by changing the software, advanced control techniques and shorter design cycle. Digital controllers like DSPs have maximum computational power capacity compared to microcontroller and hence advanced control algorithms can be easily implemented on digital signal processor (DSP).

1.1 Bidirectional DC-DC Converter

Bidirectional dc-dc converter (BDDC) is a switch mode power converter (SMPC) [1]. It is an essential candidate for many applications such as charging and discharging in uninterruptible power supplies (UPS) [2], renewable energy conversion system, electric vehicle system [3], aviation system and communication systems [4]. DC renewable energy sources like photovoltaic arrays and Fuel cells are providing variable output voltage and power. BDDC with proper control technique is essential to maintain desired constant voltage and power for driving different critical loads. A storage element is required as an energy buffer in all stand-alone systems to bridge the mismatch between available and required energy. Battery is generally the most popular energy storage element. The batteries are charged and often deep discharged and charged, which damages the battery and shortens its

useful life. In addition, the environmental constraints are an important issue in the application. Ultra-capacitor has high power density, which allows the ultra-capacitor to supply more power over a short time. Conversely, the battery has a high energy density, which allows the battery to store maximum energy and supply it over a long period of time. Battery and supercapacitor are used as storage devices as well as input elements for the converter to meet the demand. Battery and supercapacitor will be charged and discharged through BDDC to maintain the DC bus voltage as constant [5]. The BDDC works as a mediator between the DC bus and the energy storage system, Hybrid distribution generation system with back up elements as depicted in Figure 1.1.

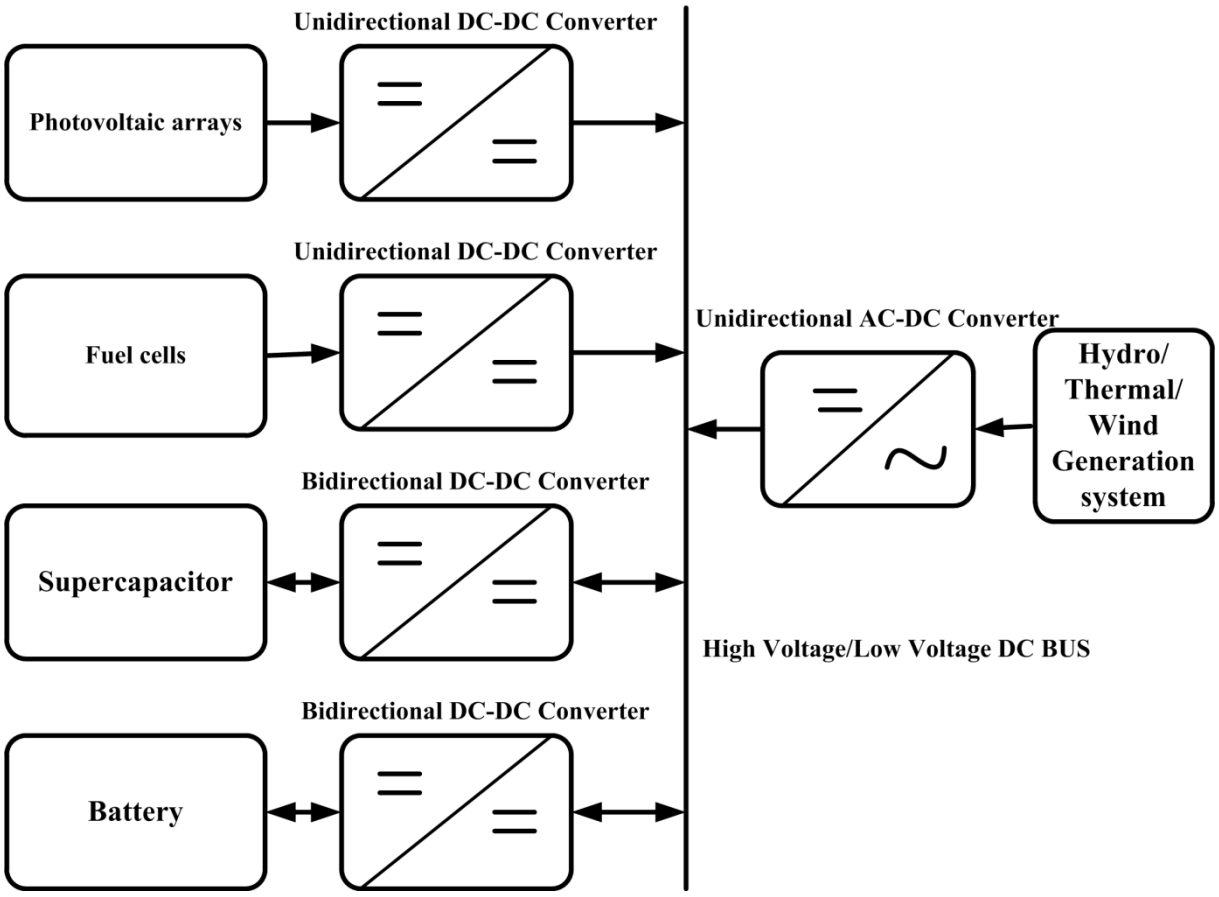


Figure 1.1 Block diagram of hybrid distributed generation system.

BDDC provides higher efficiency, power density and low cost. BDDC can also be used in two quadrant motor drive [6]. In medium power applications, a non-isolated BDDC is preferred. The total power and the direction flow of current are controlled by the suitable control algorithms. Therefore, the BDDC is very attractive for storage backup systems. The bidirectional converter works in two modes; one is forward buck mode to energy storage system and second one is reverse boost mode to supply the point of load. BDDC operating in continuous conduction mode (CCM) have lower conduction loss, and capacitor ripple current,

and have better utilization of switching devices as compared to BDDC operating in discontinuous conduction mode (DCM).

Power sources with wide voltage variation in medium power applications [7], BDDC with transformer is not suitable because of large magnetizing currents, maximum copper losses occur on low voltage side and stored energy is being transformed from the large core.

MOSFET is used as a switching device in high frequency operation; by proper selection of snubber circuit [8], device turnoff loss can be minimized and with the proper selection of gate-drive circuit [9], turn on loss can be reduced and hence achieve increased efficiency.

1.2 Interleaved Bidirectional DC-DC Converter

Many parallel BDDC stages (phases) are used to build multi-phase interleaved bidirectional dc-dc converter topology [10] which can handle relatively high currents in medium and high power applications. The number of phases in interleaved bidirectional dc-dc converter (IBDDC) is related in terms of cost, efficiency, volume and complexity of control. The main advantage of this technique is to reduce the input and output filter size, device stress, alleviation of the effects of current ripple, reliability in a rugged environment, power density and hence achieve the higher efficiency [11]. Using interleaving technique, power stage of IBDDC is divided into smaller and several stages and hence reduces the size of each element. When IBDDC operates in CCM, it minimizes imbalance currents and eliminate current control loop. Interleaved converter share equal amount of load current in each converter [12, 13] and share the same output capacitor. Interleaved converters are used in central processing unit, switching audio amplifier, hybrid electric vehicles [14], power factor correction, renewable energy [15], fuel cell systems [16], and voltage regulator module for microprocessor. The ripple in the output voltage is very small, and requires a small capacitance.

Multi-phase IBDDC has N_{phase} inductors as compared to single phase BDDC, and increase the complexity. Multi-phase IBDDC operates in continuous conduction mode have better utilization of switching devices, lower conduction loss, and reduced electromagnetic interference. An interleaved converter operates in discontinuous conduction mode has reduction of inductor size, fast transient response, increased ripple current and parasitic ringing [17].

1.3 Interleaved Switching Scheme

Multi-phase IBDDC drive signals can be generated by comparing control signal with delayed saw-tooth waveforms, so the drive signals are uniformly distributed over the switching period by following relation

$$delay = \frac{T_{switch}}{N_{phase}} \tag{1.1}$$

where T_{switch} is the switching period and N_{phase} is the number of phases of IBDDC.

Filter capacitor design of multi-phase is easier because of N_{phase} times the current ripple frequency occurrence.

1.4 Modelling and Control of Bidirectional DC-DC Converter

The modelling and control issues of the bidirectional dc-dc converter play an important role to achieve the desired stability, high reliability and high efficiency. In order to obtain the dynamic characteristics of the switching converter circuit in addition to the static ones, a modelling method is imperative. Its transient response directly determines four of the most important characteristics of a power converter: the stability of the feedback loop, the rejection of input ripple and the compatibility with the input EMI filter.

BDDC is a highly nonlinear system because it contains controlled and uncontrolled switching devices. The output voltage of BDDC is to be highly regulated within a specified range for abrupt change in input voltage and load transients. Voltage mode and current mode control techniques are the two control methods for BDDC. In the voltage mode control technique, the BDDC's output voltage is being compared with a constant reference value to generate error signal. Duty cycle of the BDDC is automatically adjusted based on error signal to obtain desired output voltage which follows the reference value. In order to design the voltage mode controller for BDDC, frequency response method is being used. In order to apply linear control theory, nonlinearity should be averaged and linearized. Based on the signal model of the BDDC, the compensator can be easily designed and analog compensator can be implemented by using analog pulse width modulator (PWM) integrated circuits (ICs) along with the suitable values of resistors and capacitors to obtain desired transfer function. Digital compensator can be implemented on DSP using control algorithms. Current mode controller has two loops in which the first loop is the inner current loop and the second is the outer voltage loop. The duty cycle for BDDC can be obtained by comparing the inductor current with its reference value and then reference value for inductor current is generated by voltage loop.

State space averaging (SSA) method [18-20] is used to derive small signal averaged equations of pulse width modulated converter and it requires considerable matrix algebra for deriving various transfer function and step responses. The SSA method provides good intuitive insight into converter behaviour. The state space is canonical form for writing the differential equations which describe a system. Transfer function of BDDC in boost mode has zero in the right half s-plane and this system is called non minimum phase system. Right half plane (RHP) zero determines a phase lag in loop gain of the of the voltage mode controlled BDDC in boost mode forcing the maximum cross over frequency to be placed at most below RHP frequency. Stability analysis of feedback loop requires proper selection of compensator or controller. Feedback compensator can be designed by the K factor method [21] which defines with few algebraic equations and this scheme can be used to achieve desired cross over frequency and the phase margin.

Mathematical modelling of interleaved bidirectional dc-dc converter (IBDDC) is essential to design a proper linear controller, leads to maintain equal current in each phase of the converter. Optimal selection on the number of phases [22] in design of IBDDC results with the current ripple cancellation, high ripple frequency, and higher efficiency. For multi-phase IBDDC, specific DSP as digital control is required to control the IBDDC [23].

Fuzzy logic has been effectively utilized in many field of knowledge to solve control and optimization problems [24]. Typically, the linguistic variables in a fuzzy logic control (FLC) are the state, state error, state error derivative, state error integral, etc. One of the key problems is to find the appropriate fuzzy control rules [25]. In general, membership sets and rule base are generated by trial and error tuning procedure [26].

1.5 LITERATURE REVIEW

Based on the connection of BDDC with auxiliary energy storage element, BDDC can be classified into buck/boost type and buck-boost type. The buck type BDDC is to have auxiliary energy storage placed on the high voltage DC bus side, and the boost type BDDC is to have it placed on the low voltage side. In order to realize bidirectional power flow in BDDC, the switch unit should carry the current in both the directions. The switch unit consist of Power MOSFET in parallel with a antiparallel diode. Depending on the configuration of BDDC to meet different application requirements, BDDC can be majorly classified into two types, non-isolated BDDC and isolated BDDC.

1.5.1 Non-Isolated Bidirectional DC-DC Converter

Non-isolated BDDC topology comprising of a step up stage and step down stage connected in parallel [27]. The high frequency transformer based BDDC system provides isolation between the source and the load. But from the perspective of improving the efficiency, size, weight and cost, the transformer less type converter is attractive. Therefore, in high power and aerospace applications, where size or weight is the major interest, the transformer less BDDC topology is preferred.

Non-isolated bidirectional dc-dc converters are presented so far as follows

1. Bidirectional buck/boost type dc-dc converter [2].
2. Bidirectional buck-boost dc-dc converter [28].
3. Bidirectional Cuk/Cuk dc-dc converter [29].
4. Bidirectional Sepic/Zeta dc-dc converter [30].
5. Bidirectional quasi resonant dc-dc converter [31].
6. Bidirectional coupled inductor dc-dc converter [32].
7. Bidirectional multi-level dc-dc converter [33].
8. Bidirectional switched-capacitor dc-dc converter [34].
9. Multiphase interleaved bidirectional dc-dc converter [41, 42].

The bidirectional buck type and boost type dc-dc converter [2] shown in Figure 1.2(a) consists of step-up converter and which is connected in antiparallel with step-down converter. During the forward step-down operation, S_1 conducts and the switch S_2 is off while D_2 is conducting. Similarly, during backward step-up operation, S_2 conducts and S_1 is off while D_1 is conducting. It has simple circuit structure, equivalent series resistance (ESR) of both inductor and capacitor and the effect of switch limits the step up voltage gain [35]. By using BDDC power converter for charging and discharging of battery [36], a substantial weight saving is possible.

Bidirectional buck-boost dc-dc converter [28] shown in Figure 1.2(b) has additional switch in the conduction path. During the forward power flow mode, S_1 conducts and the switch S_2 is off while D_2 is conducting. Similarly, during backward power flow mode, S_2 conducts and S_1 is off while D_1 is conducting. The buck-boost type BDDC is more costly and less efficient than that of buck type or boost type BDDC and which cannot be operated in wide voltage conversion range.

Bidirectional Cuk/Cuk dc-dc converter [29] shown in Figure 1.2(c) is derived from the basic Cuk dc-dc converter. During the forward power flow mode, S_1 conducts and the switch S_2 is off while D_2 is conducting. Similarly, during backward power flow mode, S_2 conducts

and S_1 is off while D_1 is conducting. It offers low conversion efficiency because this converter consists of two power stage and this type of converter cannot offer wide voltage conversion range.

Bidirectional Sepic/Zeta dc-dc converter [30] shown in Figure 1.2(d) operates as Sepic converter during forward power flow and it operates as Zeta converter during reverse power flow. During the forward power flow mode, S_1 conducts and the S_2 is off while D_2 is conducting. Similarly, during backward power flow mode, S_2 conducts and S_1 is off while D_1 is conducting. It offers low conversion efficiency because this type of converter consists of two power stage and this converter cannot offer wide voltage conversion range.

Bidirectional quasi resonant dc-dc converter [31] is as shown in Figure 1.2(e). During forward power flow S_3 is off, turning on S_1 at zero current (ZC) and turn off S_2 at zero voltage (ZV), then S_1 is turned off at ZC and S_2 is turned on at ZV, then this mode will ends at T_s when S_1 is turned on at ZC and S_2 is turned off at ZV. During reverse power flow S_2 is off, turning on S_1 at ZC and turn off S_3 at ZV, then S_1 is turned off at ZC and S_3 is turned on at ZV, then this mode will ends at T_s when S_1 is turned on at ZC and S_3 is turned off at ZV. It provides load independent characteristics with unlimited load and dc conversion ratio range, increased efficiency and simple operation. This topology also provides the same DC conversion characteristics and small signal control to duty ratio transfer function is same as that of the conventional dc-dc converter.

Bidirectional coupled inductor dc-dc converter [32] is as shown in Figure 1.2(f). During the forward mode of operation, S_1 conducts and the switch S_2 is off while D_2 is conducting. Similarly, during backward mode of operation, S_2 conducts and S_1 is off while D_1 is conducting. Inductors L_1 and L_2 are coupled to achieve higher step-up and step-down gain and also provides the large voltage gain by adjusting the coupled inductor turns ratio. But configurations of the converter circuit are complicated.

Bidirectional multi-level dc-dc converter [33] shown in Figure 1.2(g) made up of two back to back connected diode clamped converter legs. This topology is symmetric. It allows the power in both forward and backward direction for any possible value of $m = V_2 / V_1$.

Bidirectional switched-capacitor dc-dc converter [34] is as shown in Figure 1.2(h). During forward power flow, S_1 is turned on, Q_s is in saturation, rest of the switches are opened, and capacitor C is linearly charged from HV side through S_1 and Q_s for duration $T_S/2$. When S_2 and D_3 are turned on, all other switches are open, C is disconnected from HV side and stored energy is supply to LV side through S_2 and D_3. During backward power flow, D_2 is turned on, Q_s is in saturation, rest of the switches are opened, and capacitor C will be charged

through D_2 and Q_s for duration $T_S/2$. When S_2 and S_3 are turned on, all other switches are open; C is connected in series with LV side through D_1 and S_3 to supply energy to HV side. It provides the large voltage gain but more number of switches and capacitors are required [37]. Moreover, it requires complicated control circuit.

Multistage power converter consisting of many power converter stages (converter "phases") through inputs and outputs connected in parallel and their gating signal shifted by $\frac{360^0}{N_{phase}}$ to make sure the uniform distribution over a switching period and this technique is also called as "interleaving" [38]. With multi-phase interleaved operation, net current ripple can be minimized and it also minimizes the size of passive components.

For the recent high power density BDDC, to improve its power density, multi-phase current sharing technology with minimized inductance has been used in high efficiency high power applications [39-41]. Multiphase BDDC offers the advantage of minimum current stress on the devices, fast dynamic response, low current/voltage ripple and improved efficiency.

Two-phase interleaved bidirectional dc-dc converter [41, 42] is as shown in Figure 1.3(a) in which gate signals are interleaved with 180^o phase difference. In case of buck mode, the PWM switches are S_1 and S_2. Two PWM switches are operated by interleaved operation. Current flows via diode of two switches (S_3,S_4). By adjusting a duty ratio, two switches (S_1,S_2) are controlled. During buck mode operation, power is transferred from HV side to LV side. In case of boost mode, the PWM switches are S_3 and S_4. Two PWM switches are operated by interleaved operation. Current flows via diode of two switches (S_1, S_2). By adjusting a duty ratio, two switches (S_3, S_4) are controlled. During boost mode operation, power is transferred from LV side to HV side. Under this two phases; inductance value, on state resistance of switching device, internal resistance of inductor are symmetric and actual duty ratio for each of the phase is equal. This type of converter provides the optimal DC link voltage, reduces the distortion of voltage and current, and can achieve higher power than the conventional single stage converter using small inductor.

Coupled inductor two-phase interleaved bidirectional dc-dc converter [43, 44] is as shown in Figure 1.3(b). The operation of this converter is same as the two-phase interleaved bidirectional dc-dc converter. A coupling inductance M between the two inductors (L_1, L_2) can represent the coupling effect. The two inductors can be directly coupled or inversely coupled, due to the different direction selection between two winding. The coupling inductance M is positive in direct coupling and negative in inverse coupling. This type of

converter reduces the steady state current ripple, minimizes the conduction loss in MOSFET and improves the dynamic performance. Additionally, the coupling inductor core become simpler and increases the mechanical strength of the core.

Three-phase interleaved bidirectional dc-dc converter [39, 40, 45] shown in Figure 1.3(c) consists of three independent inductors (L_1,L_2,L_3) and each phase switches are interleaved with 120^o phase difference. In case of boost mode, three PWM switches (S_4,S_5,S_6) are operated by interleaved operation. Current flows via diode of three switches (S_1,S_2,S_3). By adjusting a duty ratio, three switches (S_4,S_5,S_6) are controlled. During boost mode operation, power is transferred from LV side to HV side. In case of buck mode, three PWM switches (S_1,S_2,S_3) are operated by interleaved operation. Current flows via diode of three switches (S_4,S_5,S_6). By adjusting a duty ratio, three switches (S_1,S_2,S_3) are controlled. During buck mode operation, power is transferred from HV side to LV side. The ripple current in the total current will be minimized after interleaving and therefore relieves the current stress on both LV and HV side capacitors, and hence the converter uses small value film capacitors. The magnitude of the ripple in an output voltage becomes negligible.

Coupled inductor three phase interleaved bidirectional dc-dc converter [46] is as shown in Figure 1.3(d). The operation of this type of converter is same as the three-phase interleaved bidirectional dc-dc converter. This type of converter utilises three phase coupled inductors for filtering its phase and output currents. It uses smaller inductances as compared to multiphase interleaved converter without inductive coupling. In contrast with uncoupled inductances, this type of converter reduces the ripple current in windings and switches. By minimizing high phase ripple current, it is very easy to operate magnetic material in linear range and this type of converter reliably used in hybrid drive industrial trucks.

Four-phase interleaved bidirectional dc-dc converter [47] shown in Figure 1.3(e) consists of four independent inductor and each phase switches are interleaved with 90^o phase difference. This type of converter provides large power density, used to buffer huge amount of power over a short periods and can be assembled for fast dynamic processes. This type converter is reliably used in wind power applications.

Four-phase coupled inductor interleaved bidirectional dc-dc converter [48, 49] shown in Figure 1.3(f) uses mutli-frequency control technique to avoid control loop instability under dynamic load changes. It also eliminates the instantaneous current sensing necessity to minimize noise susceptibility problems. This type of converter uses multi-phase interleaving with coupled inductor to achieve higher efficiency for a wide range of load.

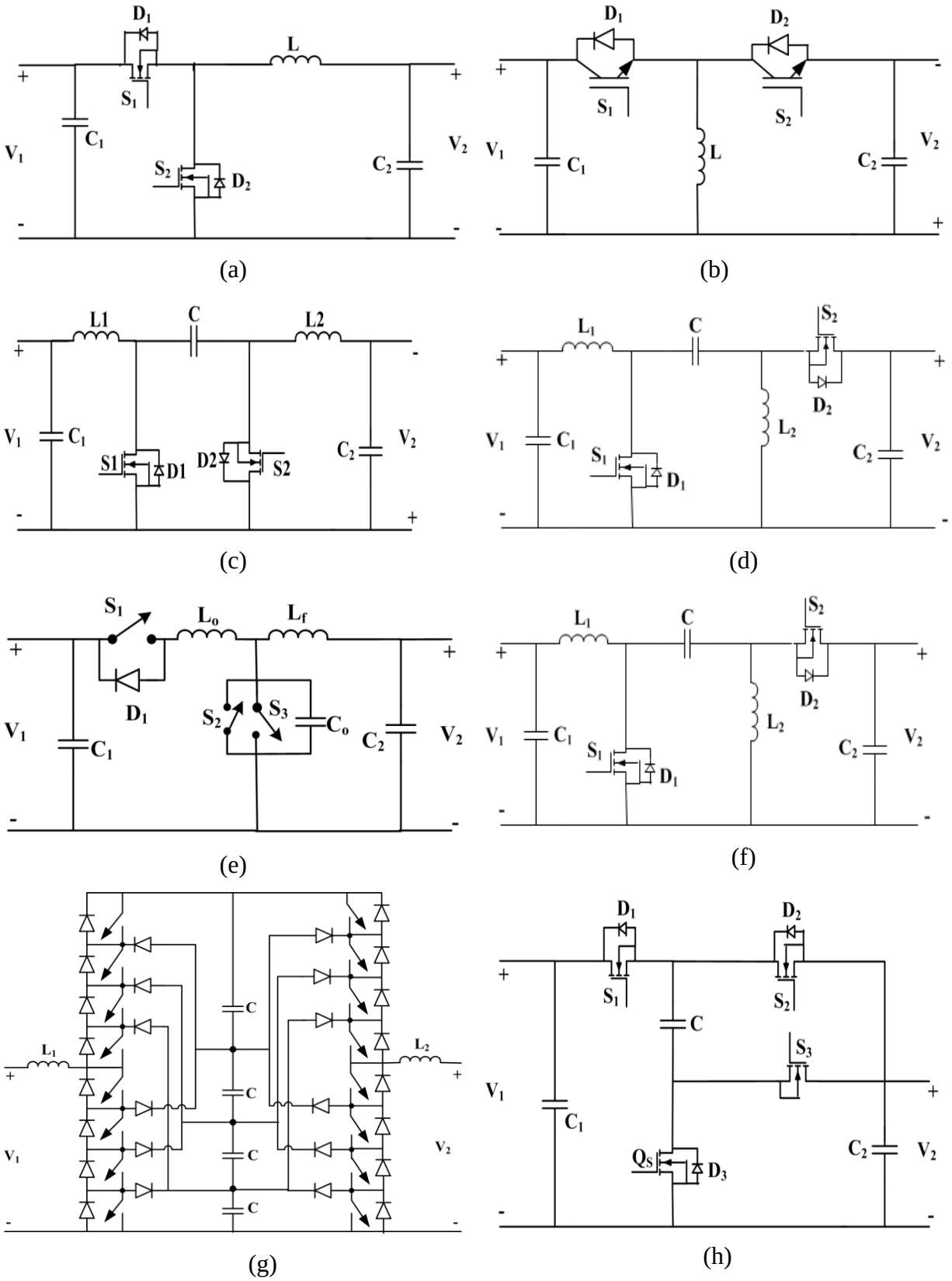


Figure 1.2 Various topologies of non-isolated BDDC;

(a) Buck / Boost type BDDC. (b) Buck-boost BDDC. (c) Cuk/Cuk BDDC. (d) Sepic/Zeta BDDC. (e) Quasi resonant BDDC. (f) Coupled inductor BDDC. (g) Multi-level BDDC. (h) Switched-capacitor BDDC.

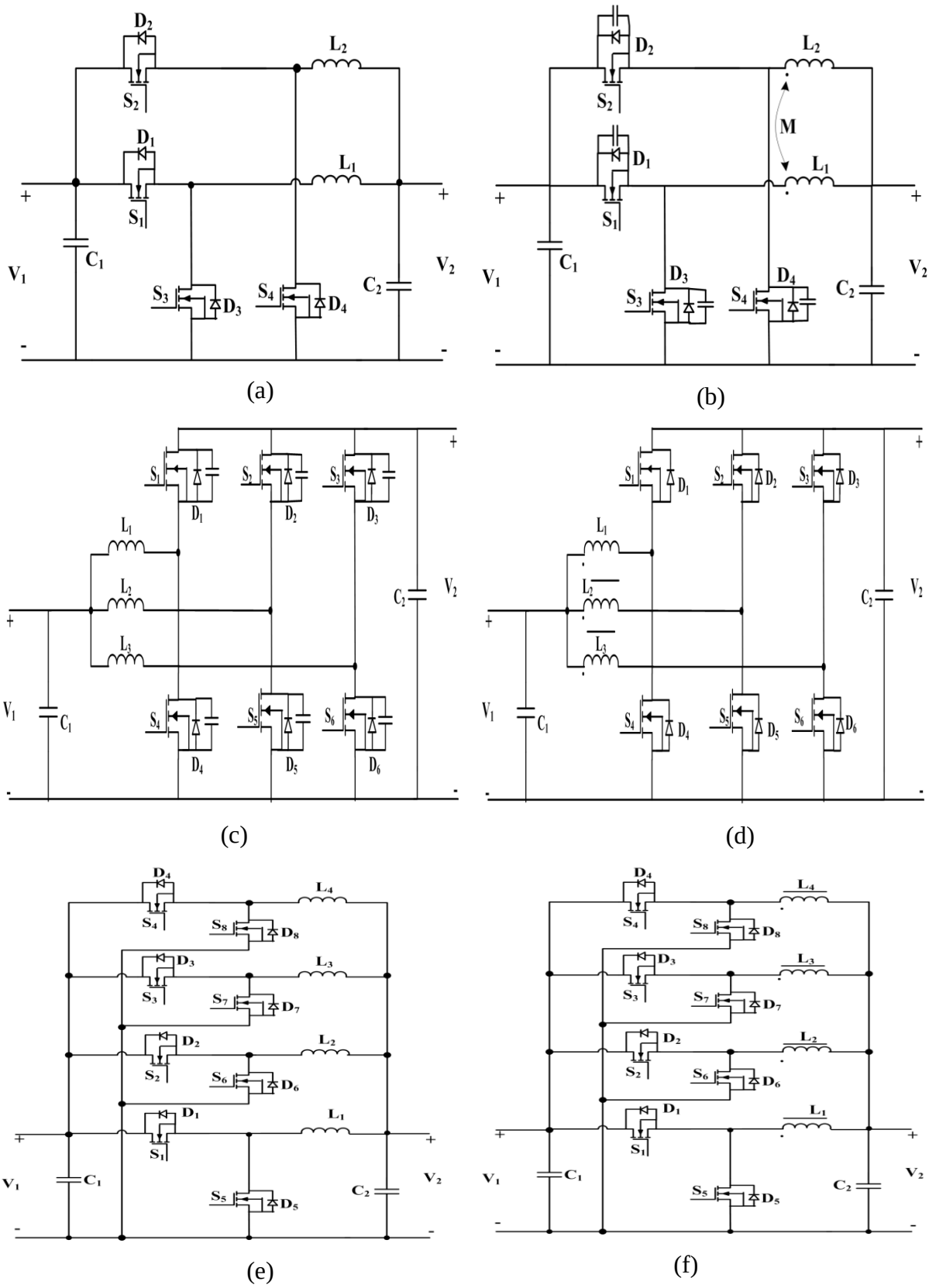


Figure 1.3 Various topologies of non-isolated interleaved BDDC;

(a) Two-phase interleaved BDDC. (b) Two-phase coupled inductor interleaved BDDC.

(c) Three-phase interleaved BDDC. (d)Three-phase coupled inductor interleaved BDDC.

(e) Four-phase interleaved BDDC. (f) Four-phase coupled inductor interleaved BDDC.

1.5.2 Isolated Bidirectional DC-DC Converter

Isolation between low voltage (LV) side and high voltage (HV) side is normally provided by a transformer, but addition of transformer introduces additional cost and losses [3]. Isolated bidirectional dc-dc converter [50] provides the large voltage gain by adjusting the transformer turns ratio. Inductor acts as current source can be placed on either LV side or HV side to allow smooth power transfer. Isolated bidirectional dc-dc converter can be operated as an inverter/rectifier in LV side or HV side. Each inverter/rectifier can be a voltage source in which capacitor comes in parallel with DC bus or current source in which inductor comes in series with DC bus. Isolated bidirectional dc-dc converter topology can be classified into number of types based on current source for LV/HV side and voltage source for LV/HV side.

Isolated bidirectional dc-dc converters are presented in the literature so far as follows

1. Bidirectional flyback (dual flyback) dc-dc converter [51-53].
2. Bidirectional forward-flyback dc-dc converter [54].
3. Bidirectional half bridge (dual active half bridge) dc-dc converter [55, 56].
4. Bidirectional half bridge-push pull dc-dc converter [57].
5. Bidirectional full bridge (dual active bridge) dc-dc converter [58-65].
6. Bidirectional push pull-forward half bridge dc-dc converter [66].
7. Isolated bidirectional multiphase interleaved dc-dc converter [71-75].

Bidirectional flyback (dual flyback) dc-dc converter [51-53] is as shown in Figure 1.4(a). During the forward power flow mode, S_1 is closed and the diode D_2 is reverse biased, the output capacitor supplies energy to the load. When the switch S_1 is opened, D_2 is forward biased; the energy from the transformer can recharges the capacitor and supplies the load. During the reverse power flow mode, S_2 is closed and the diode D_1 is reverse biased; the output capacitor supplies energy to the load. When the switch S_2 is opened, D_1 is forward biased; the energy from the transformer can recharges the capacitor and supplies the load. It has advantage of the simple structure and easy to control. This type of the converter suffers from high voltage on switches and thus it can be used in low power applications. Energy regeneration technique is being used to recycle the leakage inductor stored energy; it reduces the voltage stress on device and hence achieves the improved conversion efficiency.

Bidirectional forward-flyback dc-dc converter [54] is as shown in Figure 1.4(b). In forward power flow mode, S_1 and S_2 are main power switch and clamping switch, respectively. S_3 and S_4 are working as diodes D_3 and D_4 (or synchronous rectifier). In backward power flow mode, S_3 and S_4 are main power switch and clamping switch, respectively. S_1 and S_2 are working as diodes D_1 and D_2 (or synchronous rectifier).It has built

in flyback converter, therefore there is no turn on and turn off problems. An active or passive clamping circuit is required to reduce the voltage stress on the switches and hence this type of converter is suitable for medium power applications.

Bidirectional half bridge (dual active half bridge) dc-dc converter [55, 56] is as shown in Figure 1.4(c). This converter is operated with dual half bridges placed on each side of the isolation transformer. When power flows from the LV side to the HV side, the converter works in boost mode to power the HV side load. Otherwise, it works in buck mode to recharge the LV side battery. Dual active half bridge is proposed to achieve higher power rating; zero voltage switching (ZVS) is possible in both the direction of power flow without using clamping circuit or resonant elements. This type of converter is suitable for high power applications.

Bidirectional half bridge-push pull dc-dc converter [57] shown in Figure 1.4(d) proposes that only one transformer is enough to provide desired power flow for battery charging and discharging as opposed to two transformers are present in separate half bridge and current fed push pull dc-dc converter. In the forward/charging mode of operation, the switches S_1 and S_2 are turned on and the body diodes of S_3 and S_4 provide battery side rectification. In the backup/current fed mode of operation, the switches S_3 and S_4 are turned on and the body diodes of S_1 and S_2 provide rectification at the load side. This type of the converter offers the advantage like low voltage stress on the switches, galvanic isolation, minimum ripple in charging current, minimum active switches and fast switch over on failure.

Bidirectional full bridge (dual active bridge) dc-dc converter [58-64, 67] shown in Figure 1.4(e) consists of high frequency transformer, and two H-bridges placed on primary and secondary winding of transformer [68] correspondingly. Leakage inductance of transformer works as instantaneous energy storage element. The first H-bridge [69] consists of four switches S1, S2, S3, S4 give square wave AC voltage with duty ratio of 50% with respect to the HV side. The second H-bridge consists of four switches S_5, S_6, S_7, S_8 are connected to the secondary side of the transformer and operated by phase shift control. This type of converter is suitable for high power applications.

Bidirectional push-pull-forward half bridge dc-dc converter [66] shown in Figure 1.4(f) is a derivative topology from the dual active bridge (DAB) converter. Instead of using two inductors, this converter uses the coupled inductor and hence optimizes the performance of the converter. Phase shift modulation control strategy is being used to reduce the circuit complexity. This converter has ability to achieve high power density because of smaller size of power elements, and it will be more significant in case where multi input and multi output

phases are paralleled. The design of transformer is more difficult because of the dual primary windings, and this type of converter is employed in low voltage side.

Isolated multiphase interleaved bidirectional dc-dc converter configures the current/ voltage source on LV side and voltage / current source on HV side [70].

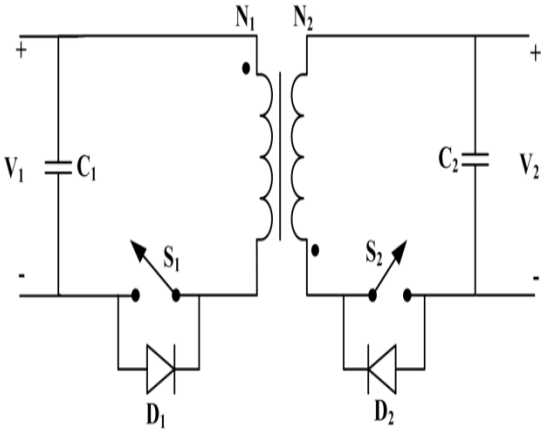
In [4], when the isolated three phase converter operate as full bridge converter, soft switching can be achieved using phase shift modulation and its secondary voltage is the turns ratio times the primary voltage.

Isolated bidirectional interleaved flyback converter [71] shown in Figure 1.5(a) propose the structure with primary windings of two flyback transformers connected in series to share HV side voltage equally and secondary windings are connected in parallel to batteries. Decoupling diodes are added on both HV and LV side, which can be used to recycle the leakage inductance energy of flyback transformer and reduce the voltage stress as well as switching losses during bidirectional power flow. This type of converter is used in battery backup system applications.

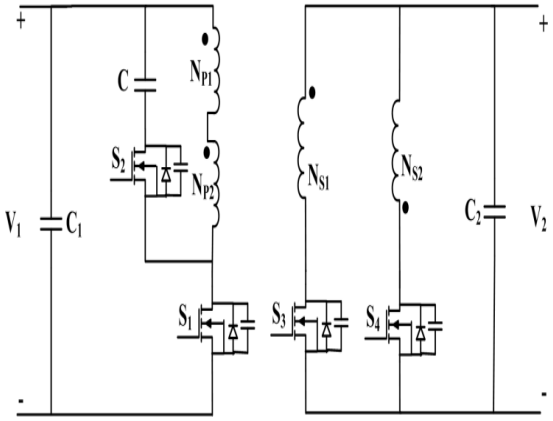
Three phase bidirectional isolated interleaved dc-dc converter [72, 73] shown in Figure 1.5(b) with active clamp provide major features of the converter include; an increased power rating, reduction of ripple current during charging/discharging modes, reduction of losses in switches and transformer windings, reduction of loss in input inductors, alleviated voltage surges as well as in switching noise, and lowering the transformer turns ratio. This type of converter is suitable for battery charger, UPS and hybrid electric vehicles.

Interleaved bidirectional dual active bridge dc-dc converter [74] shown in Figure 1.5(c) minimizes the total ripple current, reduces the current requirement of the switches and reduces the turns ratio of the transformer. Cascaded control loop technique is being used to achieve voltage regulation and provide the balance power distribution between converters. The salient features of this converter include; high power density (filter size reduced) and high voltage ratio (series in the output side). This type of converter is suitable for interfacing ultra-capacitor in micro-grid application.

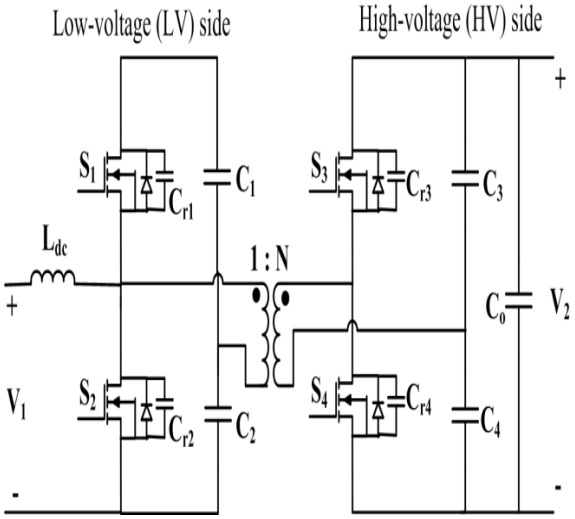
Isolated coupled inductor interleaved bidirectional dc-dc converter [75] shown in Figure 1.5(d) is employed with two symmetrical winding-cross-coupled inductors (WCCIs). WCCIs reduce the current ripple and provide the electric isolation by connecting their secondary windings in series. WCCI reduces the number of passive components, reduces the size of magnetic core and improve the power density. In the HV side, a three-level structure is used to tolerate the high voltage DC bus, but in the LV side an interleaved buck and boost converter is adopted to minimise the current ripple.



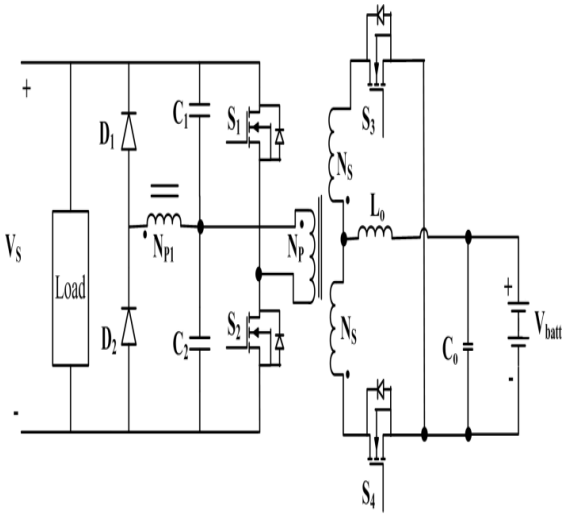
(a) Flyback (dual flyback) BDDC



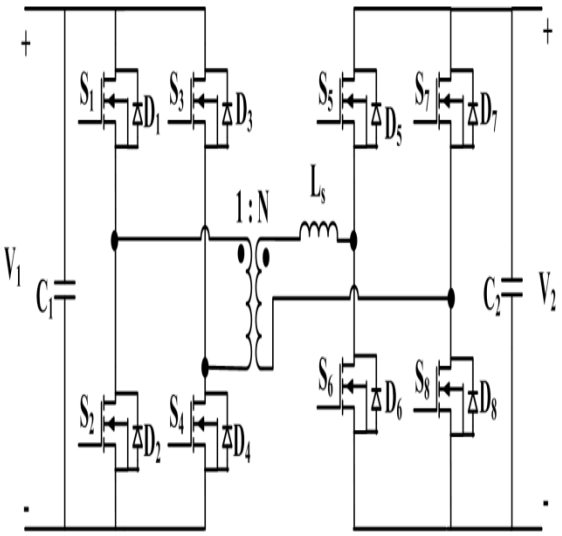
(b) Forward-flyback BDDC



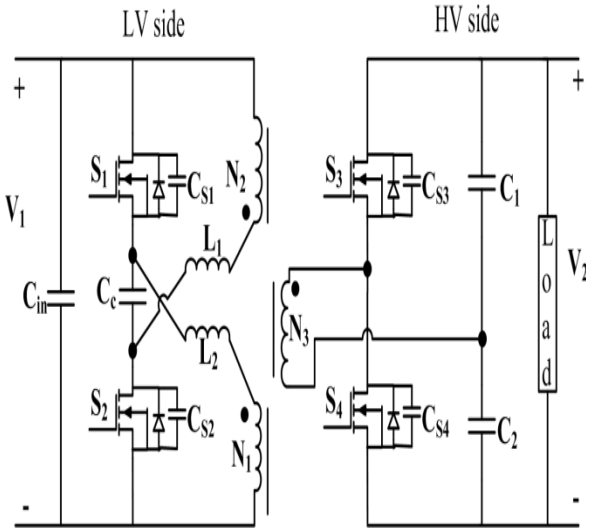
(c) Half bridge (dual active half bridge) BDDC



(d) Half bridge-push pull BDDC

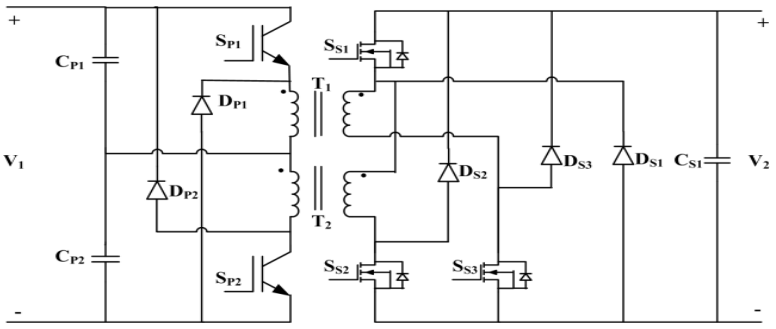


(e) Full bridge (dual active bridge) BDDC

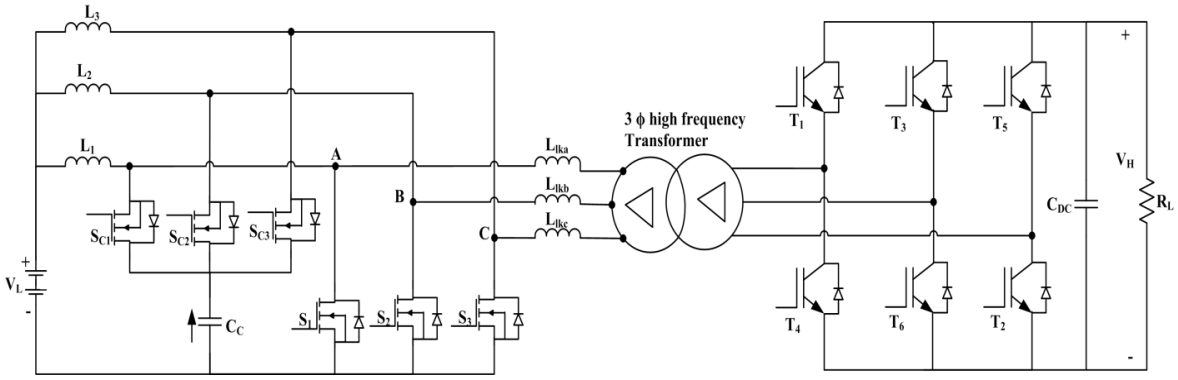


(f) Push pull-forward half bridge BDDC

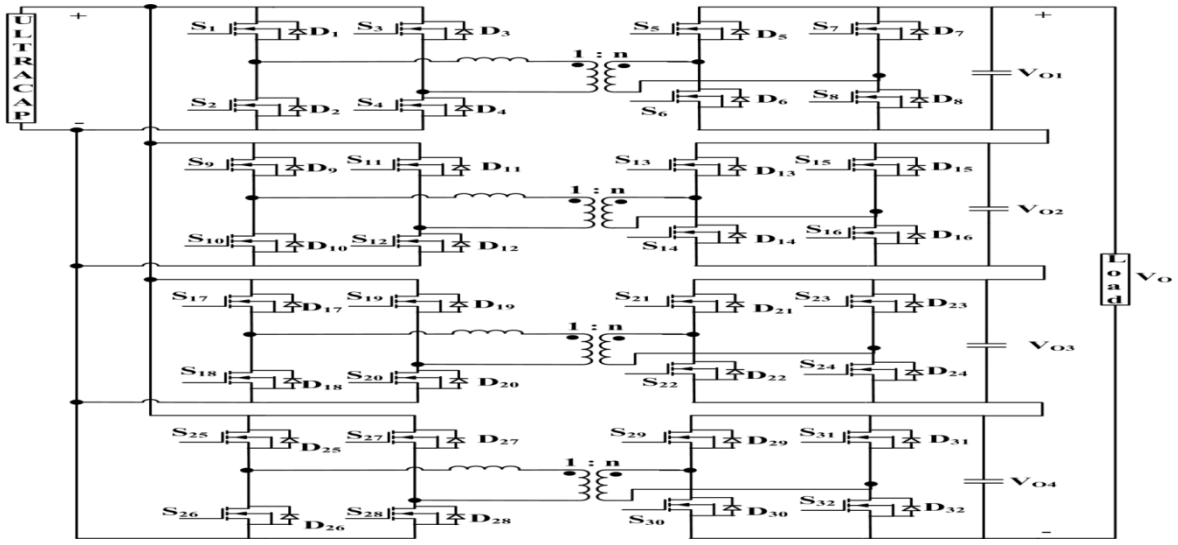
Figure 1.4 Various topologies of isolated BDDC



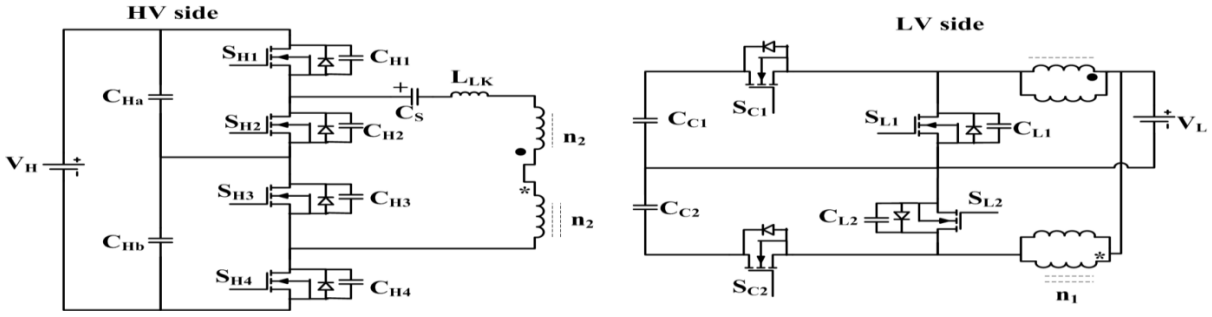
(a) Interleaved flyback BDDC



(b) Isolated three phase interleaved BDDC



(c) Interleaved dual active bridge BDDC



(d) Isolated coupled inductor interleaved BDDC.

Figure 1.5 Various topologies of isolated interleaved BDDC;

Based on the mathematical model of BDDC, linear controllers can be designed to obtain the desired response of the converter. An accurate model is essential to obtain desired regulation of the converter to drive critical loads. Many AC equivalent circuit modelling methods include, circuit averaging, average switch modelling, the current injection approach, and state-space averaging method [76].

Dynamics of the converter is usually a non-linear type, and function of converter duty ratio and load resistance. Small signal non-linear dynamic model of the converter is being derived using a state space averaging technique and digital controller was built to handle seamless bidirectional operation [77, 78].

The increasing interest in digital control of SMPC, different digital control design techniques for SMPC are presented [79]. The techniques include direct and indirect design method. In the indirect design method, small signal models of the converters are first derived and transformed into discrete models, and digital controllers are designed based on the discrete models. In indirect design method, analog controllers are designed based on small signal models of the converters, and then transformed into digital controller.

To develop a switch frequency-dependable average method to estimate the system performance at different switching frequencies, an extended state-space averaged model is developed by [80] to predict large and small-signal characteristics of the converter in either direction of power flow, and a small signal model and the corresponding equivalent circuit are developed for isolated bidirectional converter [81] to derive transfer functions and the dynamic impacts introduced by the phase-shift operation, capacitors and transformer leakage inductance have been explained by the equivalent circuits [82].

In [83], analysis of the interleaved converter operating at discontinuous current mode when it operates at lower switching frequency or at light load is described by state space averaging technique with equivalent circuits. Generalised state space model for multi-phase interleaved converters [84, 85] operating in continuous conduction mode (CCM) is established by using state space averaging technique, in which steady state and the small signal model of the converter can be developed.

Based on [86], an analog current injection control in multi-phase was implemented in [2, 87], and digital controller in BDDC is implemented in [88].

Fuzzy logic controllers can be designed based on expert knowledge of the converter system instead of accurate mathematical model [89]. Digital signal processing technologies have upgraded in handling power and speed, researchers have newly used fuzzy principles to

power electronic systems. Fuzzy logic controllers can be designed to adjust the nonlinear behavior of dc–dc converters under different operating conditions [90].

To achieve a stable and fast response under varying operating points, there are two possible solutions. One is to develop a more accurate model for the converter. However, the model may be too complex to use in controller development. A second solution is to use a nonlinear controller. Linear controllers are designed using frequency response technique applied to small signal model of the converter.

Based on the critical review, the conventional BDDC converter and three-phase IBDDC are selected for the thesis work in order to achieve high voltage diversity, higher efficiency, lower cost and improved performance.

1.5.3 Research Gaps

On the basis of peer literature review, the following research issues were identified;

1. As the past literature has emphasized on the modelling issues of the unidirectional dc-dc converters, the systematic and detailed more accurate modelling of bidirectional dc-dc converter (BDDC) become necessary for further research that needs to be addressed, and investigated.
2. The control of BDDC and its online dynamical changes in mode are the most serious and very essential issues that are required to be addressed for improved performance.
3. The voltage and current stability of a BDDC in charging/discharging applications remain challenging tasks that need to be addressed for efficient use of energy storage system.
4. The advanced control algorithms like fuzzy logic control and artificial neural network are least focused till now for BDDC. Therefore, the implementation and investigation of these advanced control algorithms would be a very interesting and challenging task of research.
5. The digital control techniques to achieve high efficiency and high reliability using fast digital processors like DSP, microcontroller and FPGA are essential and attractive in most of the applications.

The main aim of the thesis work is to develop a BDDC for charge/discharge application using digital controllers and which is to be validated with experimental results. The research work addressed in this thesis is the more accurate modelling, design optimization, control of both BDDC and three-phase IBDDC. Digital controller for both BDDC and three-phase IBDDC is implemented on a DSP ezdsp TMS320F28335.

1.5.4 Objectives of Research Work

Following are the contributions out of the research work pursued by author:

1. Design and comparative performance control of the conventional BDDC and three-phase IBDDC in simulation platform and validate experimental results with laboratory prototype.
2. Modelling and comparative analysis of the BDDC and three-phase IBDDC using state-space averaging technique.
3. Design and implementation of a voltage mode control of BDDC using type III error amplifier for boost mode and PID controller for buck mode; three-phase IBDDC using both type III error amplifier and fuzzy logic controller (FLC) to study its regulation in both boost and buck modes of operation.

1.6 Organisation of Thesis

In this thesis, first a background description and review of BDDC is presented to define the work and its novelty. Then the research challenges are identified to design and control issues in the non-isolated BDDC. The research problem addressed in this thesis is the modelling, design optimisation, control of both BDDC and three-phase IBDDC.

The thesis is organised in to four chapters and the work included in each chapter is briefly outlined as follows

Chapter 1: This chapter describes an overview of conventional bidirectional dc-dc converters, interleaved bidirectional dc-dc converters with switching scheme, modelling and control of bidirectional dc-dc converters. This chapter also presents a detailed literature review on non-isolated bidirectional dc-dc converters, isolated bidirectional dc-dc converter topologies, modelling and control of bidirectional dc-dc converters. The scope of the research work has been highlighted and author's contributions are also presented in this chapter.

This chapter also emphasizes on the design, steady state analysis, dynamic analysis using state space averaging technique, design of type 3 error amplifier controller for BDDC in boost mode, design of PID controller for BDDC in buck mode. Performance of type 3 error amplifier for boost mode, and PID controller for buck mode of conventional bidirectional dc-dc converter are also been emphasized.

Chapter 2: A simulation model of type 3 error amplifier for boost mode and PID controller for buck mode based conventional bidirectional dc-dc converter is developed in MATLAB simulation platform. Several simulation results are obtained for steady state, transient response for both the variations in input voltage and load current changes. Simulated

results and experimental results of conventional BDDC for load transients are also compared in this chapter.

This chapter also emphasizes on the design, steady state analysis, and dynamic analysis using state space averaging technique, design of type 3 error amplifier and fuzzy logic controller for three-phase interleaved bidirectional dc-dc converter. Performance of type 3 error amplifier controller and fuzzy logic controller for three-phase interleaved bidirectional dc-dc converter are also been emphasized.

Chapter 3: A simulation model of type 3 error amplifier and fuzzy logic controller based three-phase interleaved bidirectional dc-dc converter is developed in MATLAB simulation platform. Several simulation results are obtained for steady state, transient response for both the variations in input voltage and load current changes. Simulated results and experimental results of three-phase interleaved bidirectional dc-dc converter for load transients are also compared in this chapter.

Chapter 4: This chapter highlights the main conclusion and significant contribution of the thesis and scope for future work in this research area are also highlighted.

1.7 Conclusion

In this chapter, brief review of the literature on the research topics has been carried out and scope of the research work has been outlined. The author's contribution in the research area summarized. Organisation of the thesis has been outlined.

CHAPTER 2: DESIGN, MODELLING, CONTROL, SIMULATION AND EXPERIMENTATION OF BIDIRECTIONAL DC-DC CONVERTER

[This chapter emphasizes on the design, steady state analysis, dynamic analysis using State space averaging technique, design of type 3 error amplifier controller for BDDC in boost mode, design of PID controller for BDDC in buck mode. Performance of type 3 error amplifier for boost mode, and PID controller for buck mode of conventional bidirectional dc-dc converter are also been emphasized. A simulation model of type 3 error amplifier for boost mode and PID controller for buck mode based conventional bidirectional dc-dc converter is developed in MATLAB simulation platform. Several simulation results are obtained for steady state, transient response for both the variations in input voltage and load current changes. Simulation and experimental results of conventional BDDC for load transients are also compared in this chapter].

2.1 Introduction

A voltage mode control of a BDDC in CCM and design of non-isolated BDDC in boost mode and buck mode is presented. The operating principle, steady state and small signal analysis of non-isolated BDDC are described. Stability analysis of the BDDC is described with the help of K factor method [21]. Type III error amplifier for boost mode and PID controller buck mode is fully implemented on ezdsp TMS320F28335. The concept is verified by simulation and experimental results.

Depending on the simplicity in circuit and system design, reduced stress on switching devices, requirement of safety, and the voltage transfer ratio, BDDC can be non-isolated or isolated. MOSFET can be used as a switching device in high frequency operation; by proper selection of snubber circuit, device turnoff loss can be minimized and with the proper selection of gate-drive circuit, turn on loss can be reduced and hence achieve increased efficiency. BDDC operating in continuous conduction mode (CCM) have lower conduction loss, lower inductor and capacitor ripple current, and have better utilization of switching devices as compared to BDDC operating in discontinuous conduction mode. In renewable energy source applications, a BDDC can be used to deliver the energy to battery when the bus voltage is high, while transfer the energy from battery to the load when the bus voltage is low. BDDC is a highly nonlinear system because it contains controlled and uncontrolled switching devices [91, 92]. In order to apply linear control theory, nonlinearity should be averaged and linearized. The modelling and analysis of BBDC in boost mode and buck mode is presented using state space averaging (SSA) method [18-20]. The SSA method is used to derive small signal averaged equations of pulse width modulated converter and it requires considerable

matrix algebra for deriving various transfer function and step responses. The SSA method provides good intuitive insight into converter behaviour. The state space is canonical form for writing the differential equations which describe a system. The circuit averaging method [41] is based on average value of voltage and current rather than instantaneous values and this method also leads to linear equivalent circuit. Transfer function of BBDC in boost mode has zero in the right half s-plane and this system is called non minimum phase system. Right half plane (RHP) zero determines a phase lag in loop gain of the of the voltage mode controlled BDDC in boost mode forcing the maximum cross over frequency to be placed at most below RHP frequency. Stability analysis of feedback loop requires proper selection of compensator or controller. Feedback compensator can be designed by the K factor method [21] which defines with few algebraic equations and this scheme can be used to achieve desired cross over frequency and the phase margin.

2.2 Steady State Analysis of Bidirectional DC-DC Converter (BDDC)

The basic circuit diagram of conventional bidirectional dc-dc converter is as shown in Figure 2.1. Conventional BDDC constitutes buck and boost dc-dc converter which normally operate in CCM.

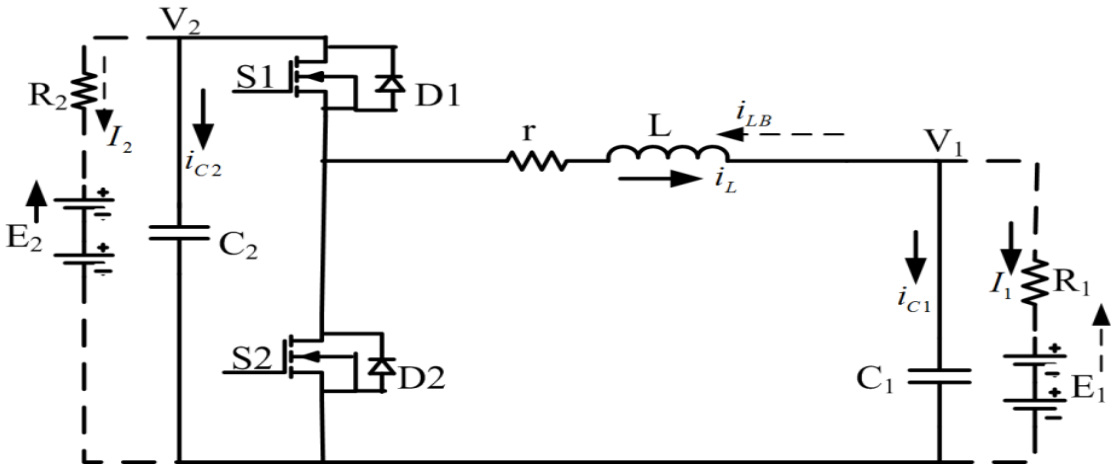


Figure 2.1 Basic circuit diagram of bidirectional dc-dc converter

The equivalent circuits and waveform of BDDC in boost mode (S2 and $D1$ conduct) operates in CCM is shown in Figure 2.2. The operation of BDDC in boost mode is as follows:

During $\mathrm{d1}=\delta \mathrm{T_s}$, S2 is turned on and $D1$ is turned off, an equivalent circuit of BDDC in boost mode is as shown in Figure 2.2(a), and initially charged capacitor ($\mathrm{C_2}$) supplies the power to the load (R_2) and current through inductor (L) increases linearly. During $\mathrm{d2}=(1-\delta)\mathrm{T_s}$, S2 is turned off and $D1$ is turned on, an equivalent circuit of BDDC is as

shown in Figure 2.2(b), and power supplied from the battery (E_1) charges the capacitor (C_2) and supply power to the load.

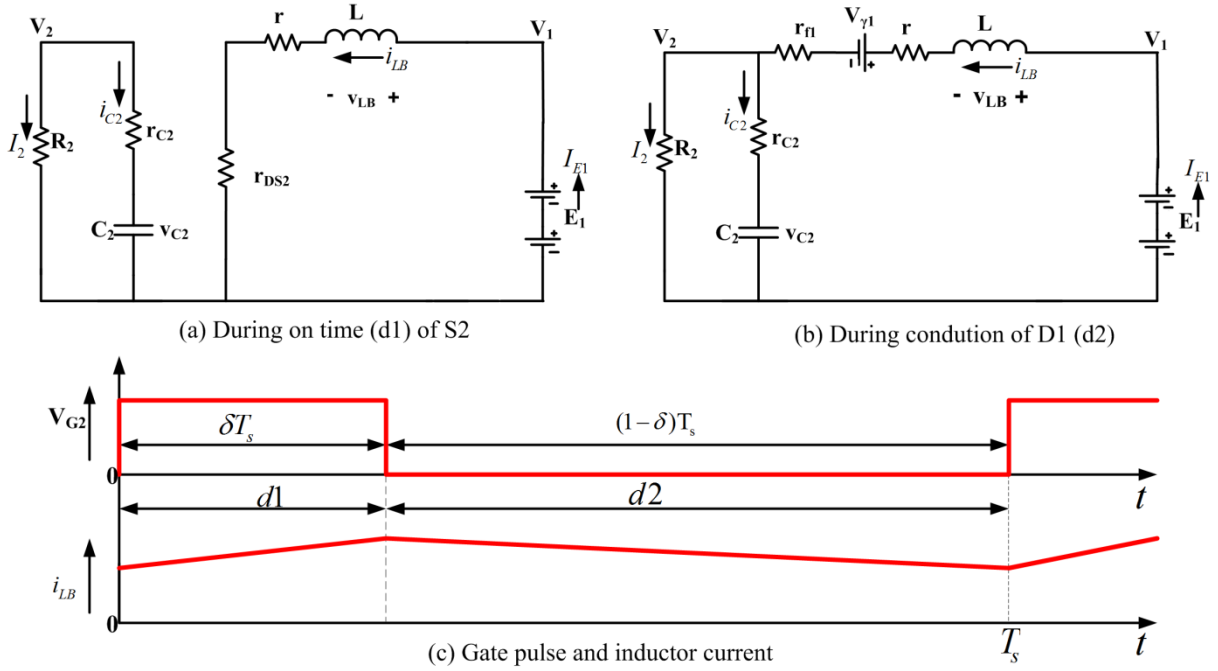


Figure 2.2 Equivalent circuits and waveform of BDDC in boost mode.

Under steady state, the average current through an inductor (I_{LB}) in boost mode is given by

$$I_{LB} = \frac{V_1 - V_{\gamma 1}(1-\delta)}{R_2(1-\delta)^2 + r_L + \delta r_{DS2} + r_{f1}(1-\delta)} \tag{2.1}$$

and an average output voltage (V_2) in boost mode is given by

$$V_2 = \frac{V_1 - I_{LB}[r_L + \delta r_{DS2} + r_{f1}(1-\delta)] - V_{\gamma 1}(1-\delta)}{(1-\delta)} \tag{2.2}$$

where δ is the boost mode duty ratio.

The equivalent circuits and waveform of BDDC in buck mode (S1 and $D2$ conduct) operates in CCM is shown in Figure 2.3.

The operation of BDDC in buck mode is as follows:

During $d_1^1 = \delta_1 T_s = (1-\delta)T_s$, $S1$ is turned on and $D2$ is turned off, an equivalent circuit of BDDC in buck mode is as shown in Figure 2.3(a). Power supplied from the battery (E_2) charges both the capacitor (C_1) and supplies power to the load (R_1) and inductor (L) stores energy. During $d_2^1 = (1-\delta_1)T_s$, $S1$ is turned off and $D2$ is turned on, an equivalent circuit of BDDC is as shown in Figure 2.3(b). Energy stored in an inductor discharge through capacitor (C_1) and supplies the power to the load (R_1).

Under steady state, the current through an inductor L (I_L) is given by

$$I_L = \frac{V_2\delta_1 - V_{\gamma 2}(1-\delta_1)}{R_1 + r_{DS1}\delta_1 + r_L - r_{f2}(1-\delta_1)} \tag{2.3}$$

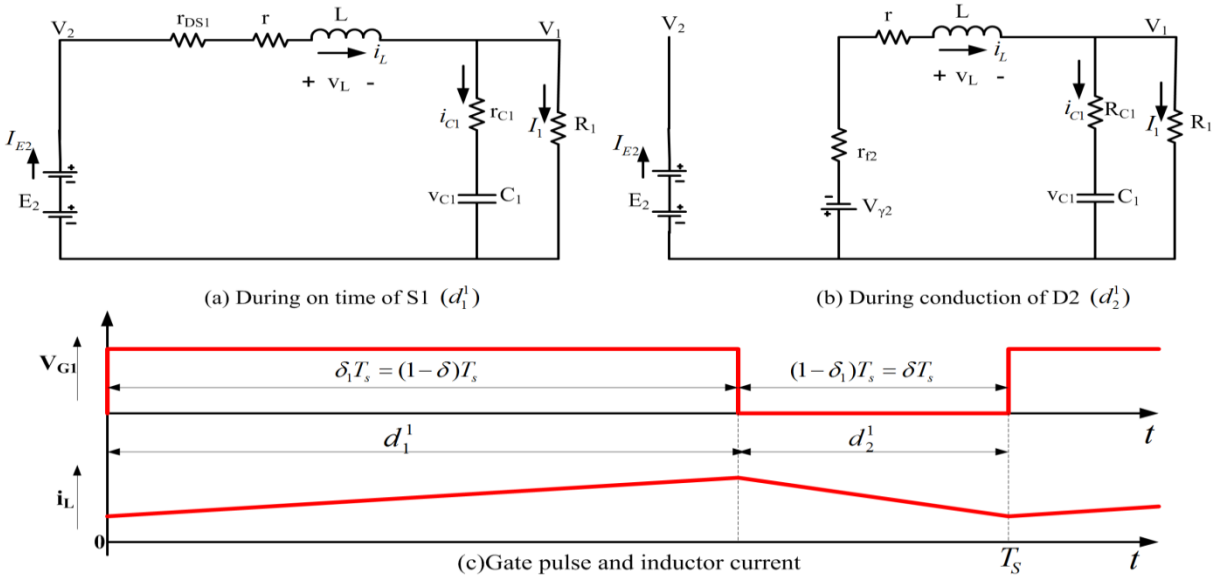


Figure 2.3 Equivalent circuits and waveform of BDDC in buck mode.

and an average output voltage (V_1) in buck mode is given by

$$V_1 = I_1 R_1 = \left[\frac{V_2\delta_1 - V_{\gamma 2}(1-\delta_1)}{R_1 + r_{DS1}\delta_1 + r_L - r_{f2}(1-\delta_1)}\right] R_1 \tag{2.4}$$

where δ_1 is the buck mode duty ratio.

2.3 Design of BDDC for Continuous Conduction Mode

Specification of BDDC in boost mode and buck mode are tabulated in Table 2.1.

Table 2.1 Specification of BDDC

Parameters	**Boost mode**	**Buck mode**
Supply voltage	48 V±10% (E_1)	70V±10% (E_2)
Output voltage	70 V (V_2)	48 V (V_1)
Load current	5 A (I_2)	6 A (I_1)
Operating frequency	100 kHz (f_s)	100 kHz (f_s)
Ripple current	$\Delta i_{LB} = 10\% I_{LB}$	$\Delta i_L = 20\% I_L$
Ripple voltage	$\Delta v_2 = 3\% v_2$	$\Delta v_1 = 1\% v_1$
Efficiency (assumed)	$\eta_b = 90\%$	$\eta = 90\%$

2.3.1 Design of BDDC in Boost Mode for CCM

Based on specifications of BDDC in boost mode for CCM as tabulated in Table 2.1, filter components (inductor L and capacitor C) of BDDC can be designed with help of minimum, nominal and maximum values of DC voltages and currents [20].

Minimum, nominal and maximum values of DC input voltages are given by following

$V_{1\min} = 42\,\text{V}$, $V_{1nom} = 48\,\text{V}$, and $V_{1\max} = 55\,\text{V}$.

The maximum and minimum values of load currents are given by the following

$I_{2\min} = 0.5\,\text{A}$, and $I_{2\max} = 5\,\text{A}$

The maximum and minimum values of output powers are given by the following

$P_{o2\max} = 350\,\text{W}$, and $P_{o2\min} = 70\,\text{W}$

The maximum and minimum values of load resistances are given by the following

$$R_{2\max} = \frac{V_2}{I_{2\min}} = 140\ \Omega$$

$$R_{2\min} = \frac{V_2}{I_{2\max}} = 14\ \Omega$$

Minimum, nominal and maximum values of DC voltage ratio in boost mode are

$$G_{1\min} = \frac{V_2}{V_{1\max}} = \frac{70}{55} = 1.26,$$

$$G_{1nom} = \frac{V_2}{V_{1nom}} = \frac{70}{48} = 1.45, \text{ and}$$

$$G_{1\max} = \frac{V_2}{V_{1\min}} = \frac{70}{42} = 1.66$$

Minimum, nominal and maximum values of duty ratio in boost mode are

$$\delta_{\min} = 1 - \frac{\eta_b}{G_{1\min}} = 0.285,$$

$$\delta_{nom} = 1 - \frac{\eta_b}{G_{1nom}} = 0.32, \text{ and}$$

$$\delta_{\max} = 1 - \frac{\eta_b}{G_{1\max}} = 0.45$$

Since $\delta_{\min} = 0.285 < \frac{1}{3}$, the minimum value of inductance is required to operate BDDC in boost mode for CCM can be calculated as

$$L_{\min} = \frac{R_{2\max}\delta_{\max}(1-\delta_{\max})^2}{2f_s} = \frac{140 \times 0.45 \times (1-0.45)^2}{2 \times 100000} = 95.28\ \mu H$$

Inductor (L) must be selected more than the minimum value such that the converter operates in CCM i.e $L = 1.25 L_{min} = 120\ \mu H$. P42/29 ferrite core is selected with SWG 14 wire gauge to carry the full load current. The detailed steps to select the core and wire gauge are given in Appendix A.

The voltage and current stress on the MOSFET and diode are

$V_{S2\max} = V_{D1\max} = 100\,\text{V}$, and

$$I_{S2\max} = I_{D1\max} = \frac{I_{2\max}}{1-\delta_{\max}} + \frac{V_1 \delta_{\max}\left(1-\delta_{\max}\right)}{2 f_s L} = 9.5\,\text{A}$$

One can select IRFP450 with $V_{DSS} = 120\,\text{V}, I_{S2\max} = 10\,\text{A}, r_{DS2} = 30\ m\Omega$. An MUR1560 ultra-fast recovery diode is also selected, which has $V_{D1\max} = 120\,\text{V}$, $I_{D1\max} = 15\,\text{A}$, $V_{\gamma 1} = 0.7\,\text{V}$ and $r_{f1} = 17.1\ m\Omega$.

The ripple voltage in output is

$V_r = 0.03 V_1 = 0.03 \times 70 = 0.21\,\text{V}$

Let us assume that the ripple voltage is equally divided between the capacitance and the equivalent series resistance (ESR). Thus

$$V_{rc2\,pp} = V_{C2\,pp} = \frac{V_r}{2} = \frac{0.21}{2} = 0.1\,\text{V}$$

Hence, the maximum ESR is

$$r_{C2\max} = \frac{V_{rc2\,pp}}{I_{D1\max}} = \frac{0.1}{15} = 6.66\ m\Omega$$

And the minimum filter capacitance is

$$C_{2\min} = \frac{\delta_{\max} V_2}{f_s R_{2\min} v_{c2\,pp}} = \frac{0.35 \times 70}{100000 \times 14 \times 0.1} = 175\ \mu F$$

Boost mode output capacitor is selected as $C_2 = 200\ \mu F$.

2.3.2 Design of BDDC in Buck Mode for CCM

Based on specifications of BDDC in buck mode for CCM as tabulated in Table 2.1, filter components (inductor L and capacitor C) of BDDC can be designed with help of minimum, nominal and maximum values of DC voltages and currents [20].

The minimum, nominal, and maximum values of the input voltage are $V_{2\min} = 65\,\text{V}$, $V_{2nom} = 70\,\text{V}$, and $V_{2\max} = 75\,\text{V}$. The maximum and minimum values of load currents are $I_{1\min} = 0.75\,\text{A}$, and $I_{1\max} = 6\,\text{A}$

The minimum and maximum values of the DC output power are

$P_{o2\min} = V_1 I_{1\min} = 48 \times 1 = 48\,\text{W}$, and

$P_{o2\max} = V_1 I_{1\max} = 48 \times 6 = 288\,\text{W}$

The maximum and minimum values of load resistances are given by the following

$$R_{1\max} = \frac{V_1}{I_{1\min}} = 64\ \Omega$$

$$R_{1\min} = \frac{V_1}{I_{1\max}} = 8\ \Omega$$

Minimum, nominal and maximum values of DC voltage ratio in boost mode are given by following

$$G_{2\min} = \frac{V_1}{V_{2\max}} = \frac{48}{75} = 0.64,$$

$$G_{2nom} = \frac{V_1}{V_{2nom}} = \frac{48}{70} = 0.685, \text{ and}$$

$$G_{2\max} = \frac{V_1}{V_{2\min}} = \frac{48}{65} = 0.738$$

Minimum, nominal and maximum values of duty ratio in buck mode are given by following

$$\delta_{1\min} = \frac{G_{2\min}}{\eta} = 0.711,$$

$$\delta_{1nom} = \frac{G_{2nom}}{\eta} = 0.7611, \text{ and}$$

$$\delta_{1\max} = \frac{G_{2\max}}{\eta} = 0.82$$

The minimum value of inductance is required to operate BDDC in buck mode for CCM can be calculated as

$$L_{\min} = \frac{R_{1\max}(1-\delta_{1\min})}{2 f_s} = L_{\min} = \frac{64 \times (1-0.71)}{2 \times 100000} = 92.8\ \mu H$$

Inductor(L)must be selected more than the minimum value such that the converter operates in CCM i.e $L = 1.25 L_{\min} = 120\ \mu H$. P42/29 ferrite core is selected with SWG 14 wire gauge to carry the full load current. The detailed steps to select the core and wire gauge are appeared in Appendix A.

The maximum inductor ripple current is

$$\Delta i_{L\max} = \frac{V_1(1-\delta_{1\min})}{f_s L} = \frac{48(1-0.711)}{100000\times120\times10^{-6}} = 1.15\,\text{A}$$

The voltage and current stress on the MOSFET and diode are

$$V_{S1\max} = V_{D2\max} = 100\,\text{V}$$

$$I_{S1\max} = I_{D2\max} = I_{1\max} + \frac{\Delta i_{L\max}}{2} = 6.5\,\text{A}$$

One can select IRFP450P with $V_{DSS} = 120\,\text{V}, I_{S2\max} = 10\,\text{A}, r_{DS2} = 30\ m\Omega$. An MUR1560 ultra-fast recovery diode is also selected, which has $V_{D1\max} = 120\,\text{V}$, $I_{D1\max} = 15\,\text{A}$, $V_{\gamma1} = 0.7\,\text{V}$ and $r_{f1} = 17.1\ m\Omega$.

The ripple voltage in output is

$$V_r = 0.01V_1 = 0.01\times48 = 0.48\,\text{V}$$

If the filter capacitance is large enough, $V_r = r_{C2\max}\Delta i_{L\max}$ and the maximum ESR of the output filter capacitor is

$$r_{C2\max} = \frac{V_r}{\Delta i_{L\max}} = 0.417\ \Omega$$

The minimum value of the capacitance at which the ripple voltage is determined by the ripple voltage across the ESR is

$$C_{1\min} = \max\left\{\frac{\delta_{\max}}{2f_s r_{C2}}, \frac{1-\delta_{\min}}{2f_s r_{C2}}\right\} = \frac{\delta_{\max}}{2f_s r_{C2}}$$

$$C_{1\min} = 3.8\ \mu F$$

Buck mode output capacitor is selected as $C_1 = 4\ \mu F$

2.4 State Space Averaged Model for BDDC

Dynamic behaviour of BDDC can be examined with the help of finding analytical expression for derivative state variables (current through an inductor and voltage across capacitor) during ON and OFF duration in each mode of operation. The number of state variables in the converter in each mode is equal to the number of energy storage elements over the switching period [93]. In order to design the proper controller for stable operation of BDDC, small signal control to duty ratio relationship can be derived with the help of SSA method [18-20]. By taking into account parasitic resistances of filter components and power switches and also the cut in voltage of the power diode, small signal open loop control to output transfer function of BDDC can be derived.

2.4.1 BDDC in Boost Mode

In order to understand the characteristic behavior of BDDC in boost mode operation, small signal equations [94, 95] of the converter can be obtained by applying Kirchhoff's voltage and current law. In boost mode, current through an inductor i_{LB} and voltage across C_2 (v_{C2}) are treated as state variable (x), its derivative parameter and output voltage equation can be obtained in terms of the converter system parameters by applying KVL and KCL for non-ideal equivalent circuits.

During the interval of on state $(d1)$ of BDDC in boost mode as shown in Figure 2.2(a), derivative of state variable $(\dot{x})$ and output voltage equations can be obtained by the following,

State variable $x = \begin{bmatrix} i_{LB} \\ v_{C2} \end{bmatrix}$, and $e_1 = \begin{bmatrix} E_1 \\ V_{\gamma 1} \end{bmatrix}$

$$\frac{di_{LB}}{dt} = -\frac{r_{DS2} + r_L}{L} i_{LB} + \frac{E_1}{L} \tag{2.5}$$

$$\frac{dv_{C2}}{dt} = -\frac{1}{C_2(r_{C2} + R_2)} v_{C2} \tag{2.6}$$

$$v_2 = \frac{R_2}{r_{C2} + R_2} v_{C2} \tag{2.7}$$

During $d1 = \delta T_s$,

$$\dot{x} = A_1 x + B_1 e_1 \tag{2.8}$$

Where $A_1 = \begin{bmatrix} -\frac{r_{DS2} + r_L}{L} & 0 \\ 0 & -\frac{1}{C_2(r_{C2} + R_2)} \end{bmatrix}$ is the system matrix, $B_1 = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \end{bmatrix}$ is the input matrix and output voltage during on time of BDDC in boost mode is given by (2.9)

$$v_2 = C_1^T x \tag{2.9}$$

where $C_1^T = \begin{bmatrix} 0 & \frac{R_2}{r_{C2} + R_2} \end{bmatrix}$ is the output matrix.

During the interval of off state $(d2)$ of BDDC in boost mode as shown in Figure 2.2(b), derivative of state variable $(\dot{x})$ and output voltage (v_2) equations can be obtained by the following relations

$$\frac{di_{LB}}{dt} = -\left[\frac{r_{f1} + r_L}{L} + \frac{r_{C2} R_2}{L(r_{C2} + R_2)} \right] i_{LB} - \frac{R_2}{L(r_{C2} + R_2)} v_{C2} + \frac{E_1}{L} - \frac{V_{\gamma 1}}{L} \tag{2.10}$$

$$\frac{dv_{C2}}{dt} = \frac{R_2}{C_2(r_{C2}+R_2)} i_{LB} - \frac{1}{C_2(r_{C2}+R_2)} v_{C2} \tag{2.11}$$

$$v_2 = \frac{R_2 r_{C2}}{r_{C2}+R_2} i_{LB} + \frac{R_2}{r_{C2}+R_2} v_{C2} \tag{2.12}$$

During $d2 = (1-\delta)T_s$,

$$\dot{x} = A_2 x + B_2 e_1 \tag{2.13}$$

where $A_2 = \begin{bmatrix} -\left(\frac{r_{f1}+r_L}{L} + \frac{r_{C2}R_2}{L(r_{C2}+R_2)}\right) & -\frac{R_2}{L(r_{C2}+R_2)} \\ \frac{R_2}{C_2(r_{C2}+R_2)} & -\frac{1}{C_2(r_{C2}+R_2)} \end{bmatrix}$, $B_2 = \begin{bmatrix} \frac{1}{L} & -\frac{1}{L} \\ 0 & 0 \end{bmatrix}$ and

Output voltage equation during $d2 = 1-\delta T_s$ of BDDC in boost mode is given by (2.14)

$$v_2 = C_2^T x \tag{2.14}$$

where $C_2^T = \begin{bmatrix} \frac{R_2 r_{C2}}{r_{C2}+R_2} & \frac{R_2}{r_{C2}+R_2} \end{bmatrix}$

Small signal open loop control to output transfer function of BDDC in boost mode relationship can be obtained using SSA method [17-19] by the following definition

$$\left.\frac{\hat{v_2}(s)}{\hat{\delta}(s)}\right|_{\hat{v_1}=0} = C^T \left[sI - A\right]^{-1} f + qX \tag{2.15}$$

where $C^T = C_1^T\delta + C_2^T(1-\delta)$, $A = A_1\delta + A_2(1-\delta)$, $f = \left[A_1 - A_2\right]X + \left[B_1 - B_2\right]E_1$, $q = C_1^T - C_2^T$, $X = -A^{-1}BE_1$ and $B = B_1\delta + B_2(1-\delta)$.

By solving the (2.15) equation, small signal open loop control to output transfer function of BDDC in boost mode can be simplified as

$$\left.\frac{\hat{v_2}(s)}{\hat{\delta}(s)}\right|_{\hat{v_1}=0} = -\frac{V_2 r_{C2}}{(1-\delta)(R_2+r_{C2})} \frac{\left(s+\frac{1}{C_2 r_{C2}}\right)\left(s-\frac{1}{L}\left[R_2(1-\delta)^2 - \left\{\delta r_{DS2} + (1-\delta)r_{f1} + r_L\right\}\right]\right)}{s^2 + s\frac{C_2\left[\left\{\delta r_{DS2} + (1-\delta)r_{f1} + r_L\right\}(R_2+r_{C2}) + (1-\delta)^2 r_L r_{C2}\right] + L}{LC_2(R_2+r_{C2})} + \frac{\left\{\delta r_{DS2} + (1-\delta)r_{f1} + r_L\right\} + R_2(1-\delta)^2}{LC_2(R_2+r_{C2})}} \tag{2.16}$$

In the above transfer function, $\hat{v_2}(s)$, $\hat{\delta}(s)$, and $\hat{v_1}$ are the small signal variations of the output voltage, duty cycle, and input voltage of BDDC in boost mode respectively.

Small signal open loop control to output transfer function of BDDC in boost mode (2.16) is a second order low pass function. It has common two-pole low pass filter and two

zeros. The common two-pole low pass filter's corner frequency occurs at $w_c = \frac{1-\delta}{\sqrt{LC_2}}$. The first zero in the left half plane (LHP) occurs at $w_{zn} = -\frac{1}{C_2 r_{C2}}$, and other zero in the right half plane (RHP) occurs at $w_{zp} = \frac{(1-\delta)^2 R_2}{L}$. Variables w_c and w_{zp} are functions of duty ratio δ. The physical occurrence of the RHP zero is that when there is a step rise in duty ratio, the initial slope of the output voltage $\left(\frac{dv_1}{dt}\right)$ is negative, which averages that the output voltage will drop instantly. Special care is required when designing the controller for the system to have acceptable gain and phase margins.

Substituting the design values of boost mode BDDC in (2.16), which results in boost mode BDDC system transfer function (2.17), the corresponding frequency response (bode plot) and unit step response plot are shown in Figure 2.4 and Figure 2.5 respectively.

$$G_{Boost}(s) = \left.\frac{\hat{v}_2(s)}{\hat{\delta}(s)}\right|_{\hat{v}_1=0} = \frac{-0.6119s^2 - 8290s + 1.872\times10^{09}}{s^2 + 975.7s + 1.763\times10^{07}} \qquad (2.17)$$

Equation (2.17) results with complex conjugate poles ($-488 \pm j4.17\times10^{03}$) lie at frequency 668 Hz, one zero (-6.24×10^{04}) at 9.95 kHz and other zero (4.9×10^{04}) lies in RHP at 7.79 kHz. This system is unstable, because one of the zero lies in right half s-plane.

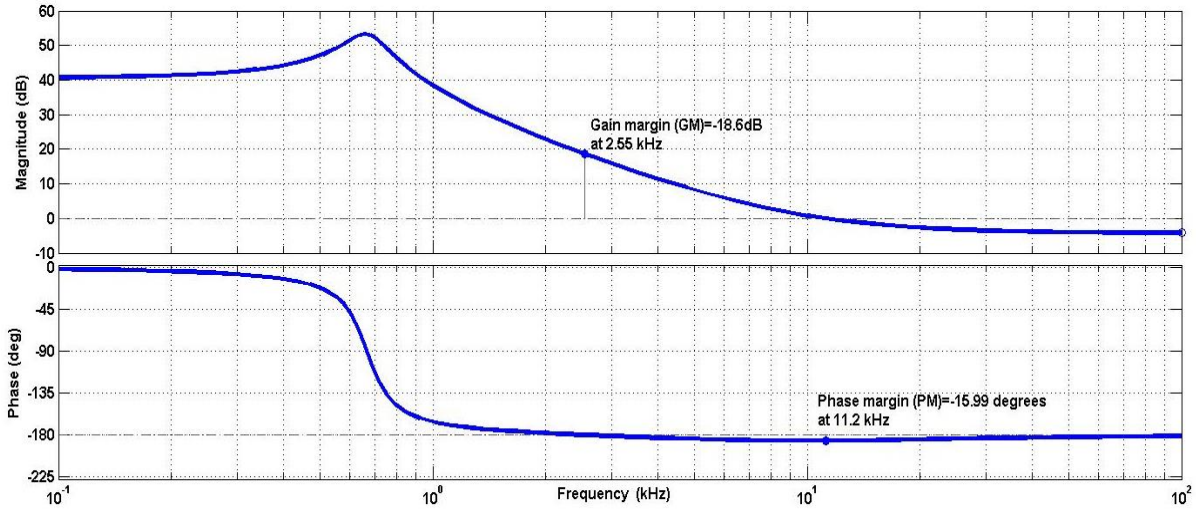


Figure 2.4 Bode plot of the state space averaged model of BDDC in boost mode.

From Figure 2.4, BDDC in boost mode results with the gain margin (GM) of -18.6 dB at $2.55\ kHz$ and phase margin (PM) of -5.99^0 at 11.2 kHz. The above system is a non-minimum phase system.

From Figure 2.5, BDDC in boost mode results with the rise time of 272 µs, peak over shoot of 1.7 V with overshoot of 69.6% at 748 µs, settling time of 7.7 ms and steady state value of 1 V. The above system is an under damped and unstable system.

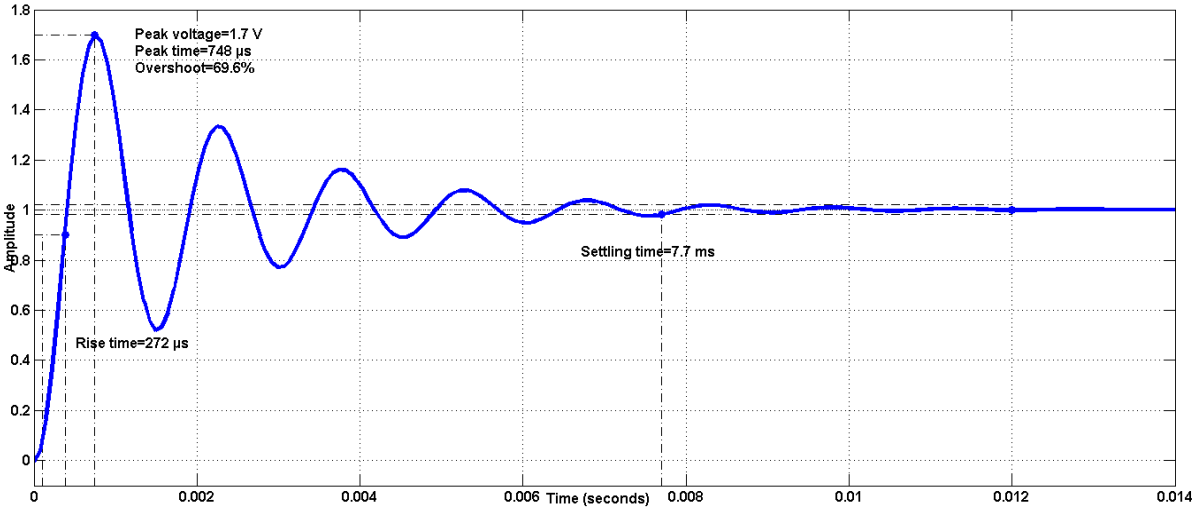


Figure 2.5 Unit step response plot of the state space averaged model of BDDC in boost mode.

2.4.2 BDDC in Buck Mode

In buck mode, current through an inductor L (i_L) and voltage across C_1 (v_{C1}) are treated as state variable (x), its derivative parameter and output voltage equation can be obtained in terms of the converter system parameters by applying KVL and KCL for non-ideal equivalent circuits.

During the interval of on state (d_1^1) of BDDC in buck mode as shown in Figure 2.3 (a), derivative of state variable $(\dot{x}_1)$ and output voltage (v_1) equations can be obtained by the following relations

$$\frac{di_L}{dt} = -\left[\frac{(R_{DS1}+r_L)}{L} + \frac{R_1 R_{C1}}{L(R_{C1}+R_1)}\right] i_L - \frac{R_1}{L(R_{C1}+R_1)} v_{C1} + \frac{E_2}{L} \tag{2.18}$$

$$\frac{dv_{C1}}{dt} = \frac{R_1}{C_1(R_{C1}+R_1)} i_L - \frac{1}{C_1(R_{C1}+R_1)} v_{C1} \tag{2.19}$$

$$v_1 = \frac{R_{C1}R_1}{R_{C1}+R_1} i_L + \frac{R_1}{R_{C1}+R_1} v_{C1} \tag{2.20}$$

During $d_1^1 = (1-\delta)T_s = \delta_1 T_s$, state variable $x_1 = \begin{bmatrix} i_L \\ v_{C1} \end{bmatrix}$, and $e_2 = \begin{bmatrix} E_2 \\ V_{\gamma 2} \end{bmatrix}$

$$\dot{x}_1 = A_3 x_1 + B_3 e_2 \tag{2.21}$$

where $A_3 = \begin{bmatrix} -\left(\frac{(r_{DS1}+r_L)}{L} + \frac{R_1 r_{C1}}{L(r_{C1}+R_1)}\right) & -\frac{R_1}{L(r_{C1}+R_1)} \\ \frac{R_1}{C_1(r_{C1}+R_1)} & -\frac{1}{C_1(r_{C1}+R_1)} \end{bmatrix}$, $B_3 = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \end{bmatrix}$ and

Output voltage equation during on time of BDDC in buck mode is given by (2.22)

$$v_1 = C_3^T x_1 \tag{2.22}$$

where $C_3^T = \begin{bmatrix} \frac{r_{C1}R_1}{r_{C1}+R_1} & \frac{R_1}{r_{C1}+R_1} \end{bmatrix}$

During the interval of off state $\left(d_2^1\right)$ of BDDC in buck mode as shown Figure 2.3 (b), derivative of state variable and output voltage equations can be obtained by the following relations

$$\frac{di_L}{dt} = -\left[\frac{(r_{f2}+r_L)}{L} + \frac{r_{C1}R_1}{L(r_{C1}+R_1)}\right] i_L - \frac{V_{\gamma 2}}{L} \tag{2.23}$$

$$\frac{dv_{C1}}{dt} = \frac{R_1}{C_1(r_{C1}+R_1)} i_L - \frac{1}{C_1(r_{C1}+R_1)} v_{C1} \tag{2.24}$$

$$v_1 = \frac{R_1 r_{C1}}{r_{C1}+R_1} i_L + \frac{R_1}{r_{C1}+R_1} v_{C1} \tag{2.25}$$

During $d_2^1 = T_s - d_1^1 = (1-\delta_1)T_s$,

$$\dot{x}_1 = A_4 x_1 + B_4 e_2 \tag{2.26}$$

where $A_4 = \begin{bmatrix} -\left(\frac{(r_{f2}+r_L)}{L} + \frac{r_{C1}R_1}{L(r_{C1}+R_1)}\right) & -\frac{R_1}{L(r_{C1}+R_1)} \\ \frac{R_1}{C_1(r_{C1}+R_1)} & -\frac{1}{C_1(r_{C1}+R_1)} \end{bmatrix}$, $B_4 = \begin{bmatrix} 0 & -\frac{1}{L} \\ 0 & 0 \end{bmatrix}$ and

Output voltage equation during off time of BDDC in buck mode is given by (2.27)

$$v_1 = C_4^T x_1 \tag{2.27}$$

where $C_4^T = \begin{bmatrix} \frac{r_{C1}R_1}{r_{C1}+R_1} & \frac{R_1}{r_{C1}+R_1} \end{bmatrix}$

Small signal open loop control to output transfer function of BDDC in buck mode operation relationship can be obtained using SSA method [18-20] by the following definition

$$\left.\frac{\hat{v_1}(s)}{\hat{\delta_1}(s)}\right|_{\hat{v_2}=0} = C_5^T\left[sI - A_5\right]^{-1} f_1 + q_1 X_1 \qquad (2.28)$$

where $C_5^T = C_3^T\delta_1 + C_4^T(1-\delta_1)$, $A_5 = A_3\delta_1 + A_4(1-\delta_1)$, $f_1 = \left[A_3 - A_4\right]X_1 + \left[B_3 - B_4\right]E_2$, $q_1 = C_3^T - C_4^T$, $X_1 = -A_5^{-1}B_5E_2$ and $B_5 = B_3\delta_1 + B_4(1-\delta_1)$.

By solving the (2.28) equation, small signal open loop control to output transfer function of BDDC in buck mode can be simplified as

$$\left.\frac{\hat{v_1}(s)}{\hat{\delta_1}(s)}\right|_{\hat{v_2}=0} = \left(\frac{V_1}{\delta_1}\right)\left[\frac{1+sr_{C1}C_1}{1+s\left(r_{C1}C_1+\left[\frac{R_1r_L}{R_1+r_L}\right]C_1+\frac{L}{R_1+r_L}\right)+s^2LC_1\left(\frac{R_1r_{C1}}{R_1+r_{C1}}\right)}\right] \qquad (2.29)$$

In the transfer function, $\hat{v_1}(s)$, $\hat{\delta_1}(s)$, and $\hat{v_2}$ are the small signal variations of the output voltage, duty cycle, and input voltage of BDDC in buck mode respectively.

Small signal open loop control to output transfer function of BDDC in buck mode (2.29) is a common two-pole low pass filter, with a LHP zero introduced by the ESR of the filter output capacitance. The corner frequency of the low pass filter occurs at $w_{c1} = \frac{1}{\sqrt{LC_1}}$. The zero in the left half plane (LHP) occurs at $w_{zn1} = -\frac{1}{C_1r_{C1}}$. The magnitude of the transfer function varies on buck mode duty ratio δ_1.

Substituting the design values of buck mode BDDC in (2.29), which results in buck mode BDDC system transfer function (2.30), the corresponding bode plot and unit step response plot are shown in Figure 2.6 and Figure 2.7 respectively.

$$G_{Buck}(s) = \left.\frac{\hat{v_1}(s)}{\hat{\delta_1}(s)}\right|_{\hat{v_2}=0} = \frac{3316.35s + 2\times10^9}{s^2 + 33354s + 2\times10^9} \qquad (2.30)$$

Equation (2.30) results with complex conjugate poles and one zero. This system is marginally stable because all the poles and zeros lie in the left half s-plane.

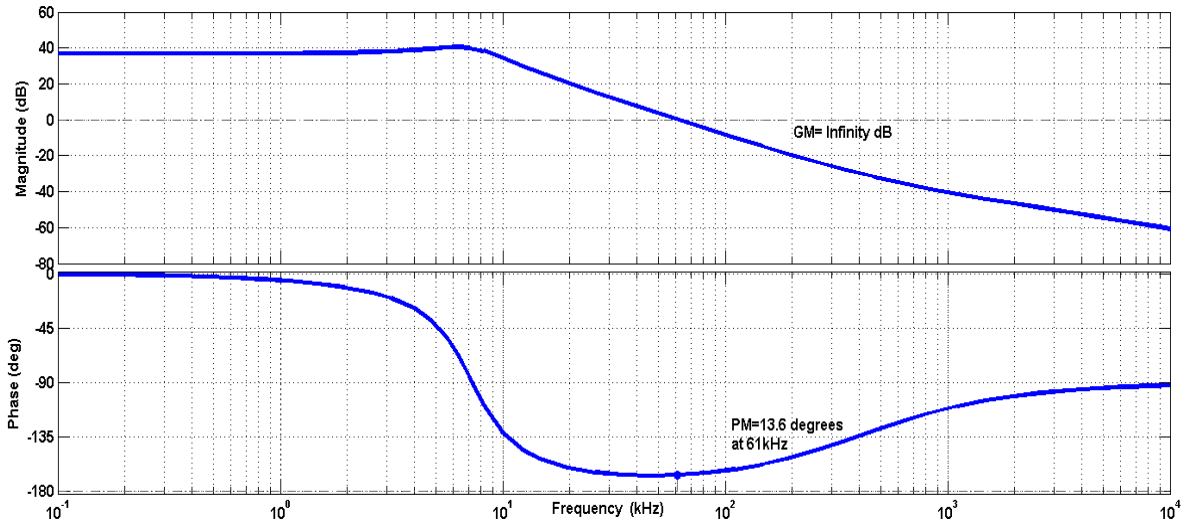


Figure 2.6 Bode plot of the state space averaged model of BDDC in buck mode.

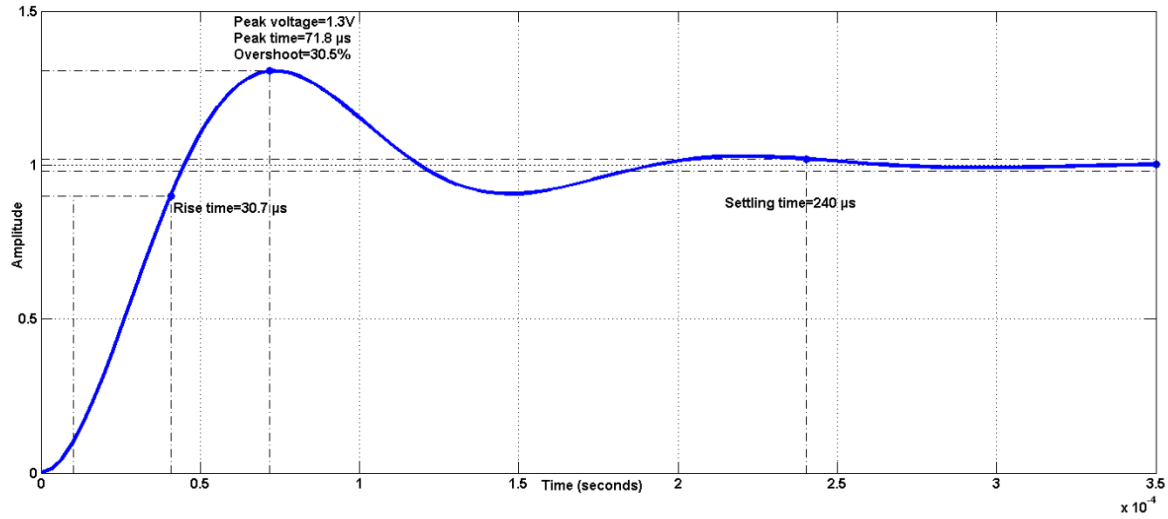


Figure 2.7 Unit step plot response for the SSA model of BDDC in buck mode.

From Figure 2.7, BDDC in buck mode results with the rise time of 30.7 µs; peak over shoot of 1.3 V with overshoot of 30.5% at 71.8 µs, settling time of 240 µs and steady state value of 1 V. The above system is an under damped system.

2.5 Design of Compensator/ Controller for BDDC

2.5.1 Block Diagram of Closed Loop BDDC System

Block diagram of closed loop BDDC either in boost mode or buck mode is as shown in Figure 2.8. Whenever supply voltage and load current change, the converter with the proper feedback circuit should be designed to obtain the reference voltage which corresponds to the desired output voltage and then proper controller must be designed. Pulse width modulator (PWM) compares the control voltage generated by the controller with the fixed frequency saw

tooth wave, and it decides the duty ratio for the switches of BDDC operates either in boost mode or buck mode to meet the desired line and load regulation [96].

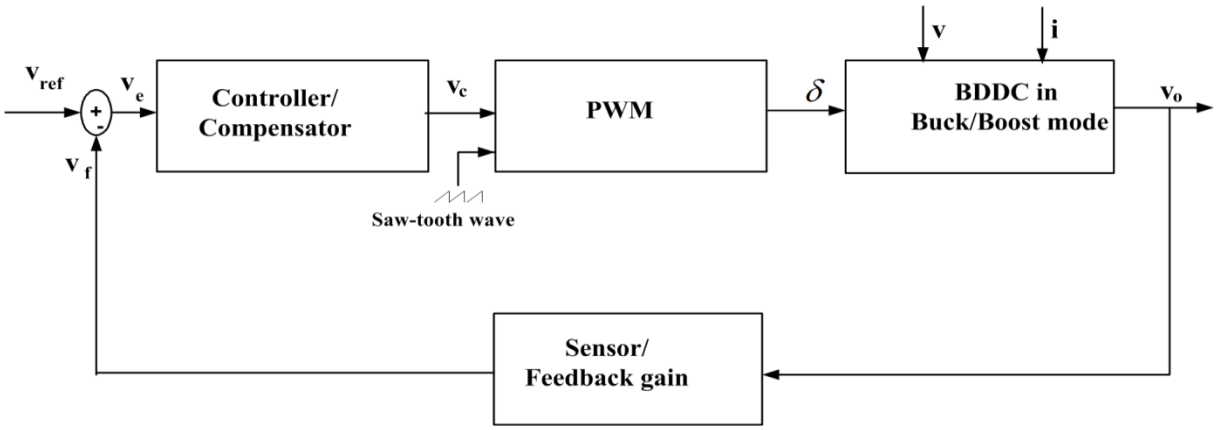


Figure 2.8 Block diagram of closed loop BDDC system.

Type III error amplifier (EA) [21, 97] is also called as third order integral double lead controller is shown in Figure 2.9. It has a pole at origin and has two pole-zero pairs. This controller is designed to provide high gain at low frequency and low gain at high frequency to achieve the reduced dc error, closed loop output impedance is to maintain sufficient degree of relative stability. Phase lag introduced from the actual system can be reduced to desired phase boost over the bandwidth by the type III compensator and leads to faster step response. Typical range of phase margin lies between 45^0 and 60^0, and the gain margin lies between 6 dB and 12 dB. Lower value of phase margin gives the fastest response and shorter settling time, and more ringing with maximum overshoot in transient response. By suitably selecting phase margin and phase boost, type III error amplifier elements can be determined.

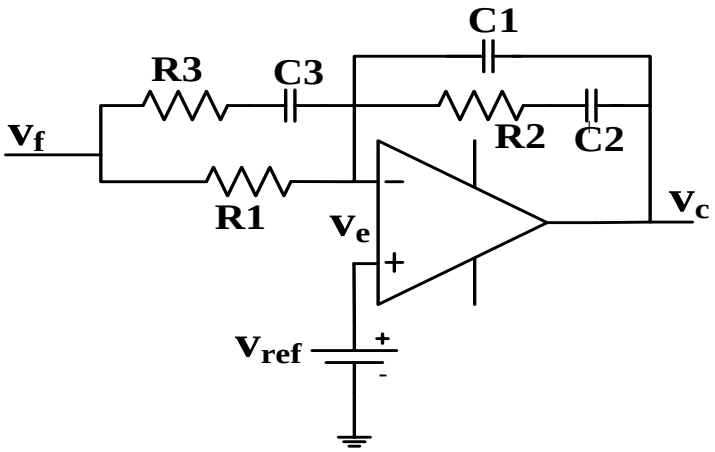


Figure 2.9 Schematic diagram of type III error amplifier/compensator

Figure 2.9 shows the schematic diagram of type III error amplifier and its forward voltage transfer function is given by

$$G_c(s)=\frac{(R1+R3)\left(s+\frac{1}{R2C2}\right)\left(s+\frac{1}{(R1+R3)C2}\right)}{R1R3C1\left(s+\frac{C1+C2}{R2C1C2}\right)\left(s+\frac{1}{R3C3}\right)s} \tag{2.31}$$

The values of resistor and capacitor are suitably designed with open loop system's gain margin and suitable phase margin to achieve desired loop bandwidth of the converter system using 'K' factor method [21].

2.5.2 Design Method of Compensation Network:

Type III compensator [21] for BDDC can be designed with the following steps:

1. Generate open loop bode plot of small signal transfer function control to output voltage of the BDDC system along with the feedback factor and PWM gain.
2. Select a cross over frequency (f_c) between one-tenth and one-fourth of switching frequency (f_s)
3. Select the desired phase margin (PM) between 45^0 and 60^0 for stable operation of the BDDC system.
4. Corresponding to step1, measure the gain corresponding to the selected cross over frequency, and determine error amplifier gain (G) which will be simply negative of measured gain in dB.
5. Corresponding to step1, measure phase shift corresponding to the selected cross over frequency, and determine the required phase boost which is calculated by the following expression

$$Phaseboost = PM_D - PS_S - 90^0 \tag{2.32}$$

where PM_D is the desired phase margin and PS_S is the phase shift introduced by the system.

6. The type 3 error amplifier will be selected where the desired phase boost is less than 180^0.
7. Select the value of R1 as high as possible. R1 reduces the value compensation capacitors.
8. Resistors and compensation capacitors value of the type 3 error amplifier can be calculated using K factor by the following equations

$$K = \left\{ \tan\left[\left(\frac{Phaseboost}{4} \right) + 45^0 \right] \right\}^2 \tag{2.33}$$

$$C2 = \frac{1}{2\pi f_c GR1} \tag{2.34}$$

$$C1 = C2\left(K - 1\right) \tag{2.35}$$

$$R2 = \frac{\sqrt{K}}{2\pi f_c C1} \tag{2.36}$$

$$R3 = \frac{R1}{\left(K - 1\right)} \tag{2.37}$$

$$C3 = \frac{1}{2\pi f_c \sqrt{K} R3} \tag{2.38}$$

With the above values, loop gain of the compensated system will be unity at cross over frequency $\left(f_c \right)$ and phase margin will be as the desired value. The required gain of an error amplifier will be less than the open loop gain of an error amplifier.

2.5.3 Design of Type III Error Amplifier/Compensator for BDDC in Boost Mode

In order to understand the system behaviour of the BDDC in boost mode against line voltage variations and load transients, the open loop bode plot of small signal transfer function control to output voltage of the BDDC in boost mode is plotted for different input voltage ranges 40 V, 45 V, 48 V, 51 V and 55 V, and open loop unit step response plot for the same are shown in Figure 2.10 and Figure 2.11 respectively. Similarly the open loop bode plot of small signal transfer function control to output voltage of the BDDC in boost mode is also plotted for different load current of 1 A, 2 A, 3 A, 4 A, and 5 A, and open loop unit step response plot for the same are shown in Figure 2.12 and Figure 2.13 respectively.

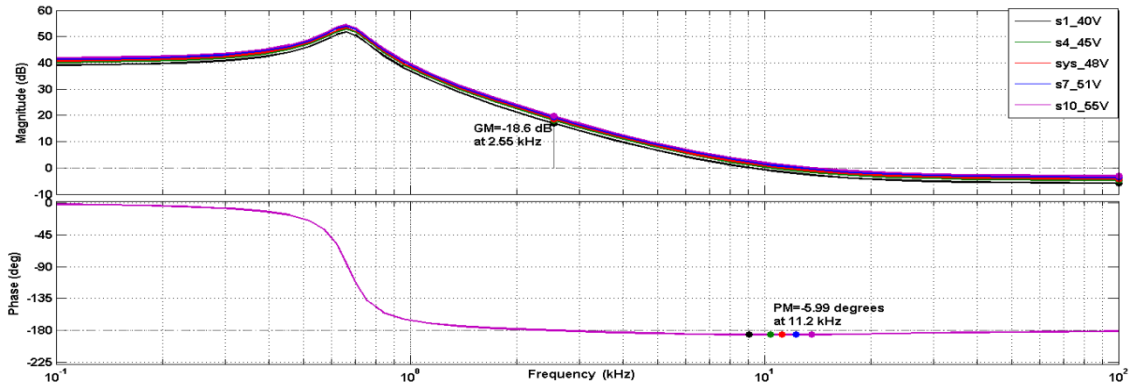


Figure 2.10 Open loop bode for different input voltages of BDDC in boost mode.

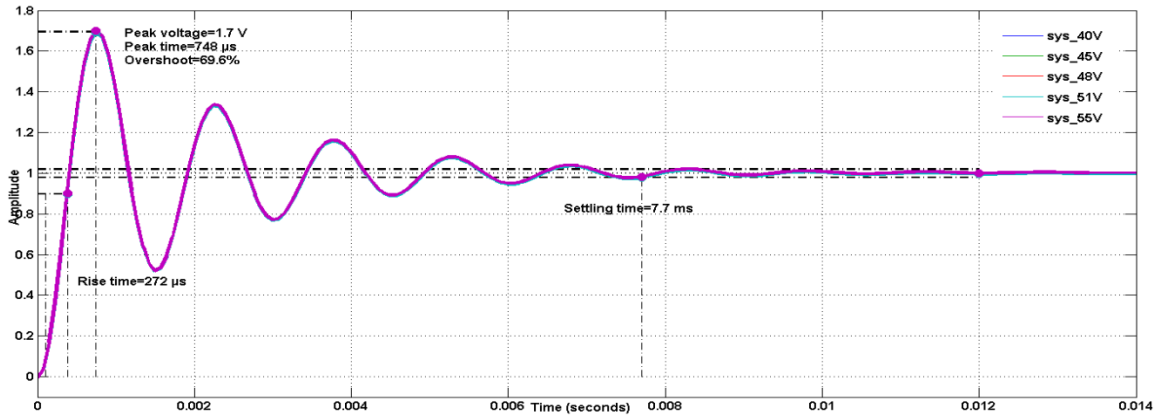


Figure 2.11 Open loop unit step plot for various input voltage of BDDC in boost mode.

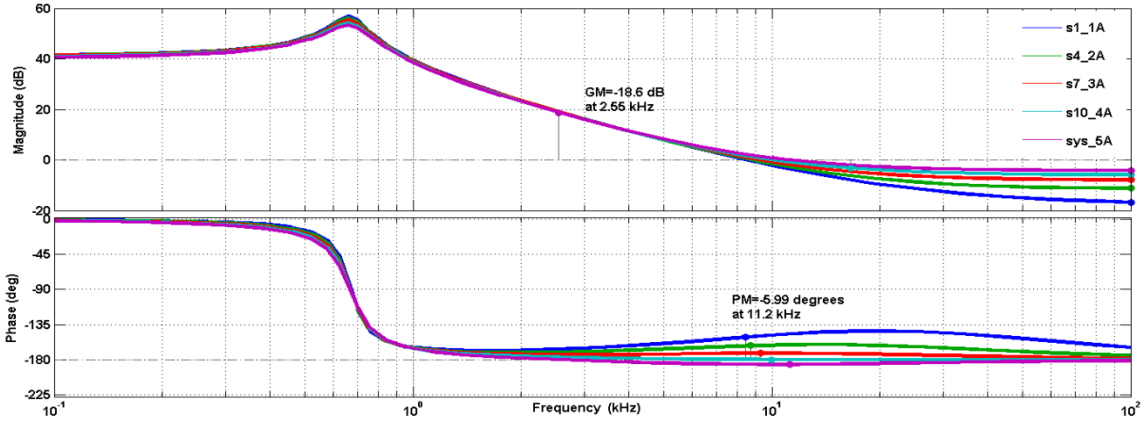


Figure 2.12 Open loop bode for different output load currents of BDDC in boost mode.

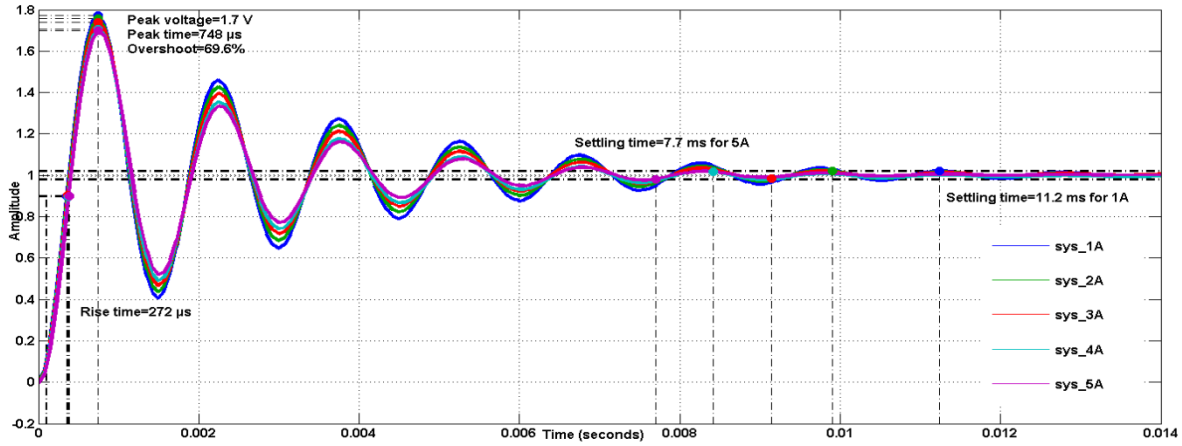


Figure 2.13 Open loop unit step plot for different load current of BDDC in boost mode.

The BDDC in boost mode is not stable for any input voltage of, 40 V, 45 V, 48 V, 51 V and 55 V and also the converter system is not stable even for the output load current of 1 A, 2 A, 3 A, 4 A, and 5 A.

The open loop transfer function of BDDC in boost mode uses with its forward feedback factor $\left(\beta = \frac{1}{70}\right)$ which is used to convert the output voltage to the reference voltage

$\left(V_{ref} = 1V\right)$corresponding to desired output voltage of 70V, and then multiply by the PWM gain$\left(G_{PWM} = \frac{1}{3}\right)$ in which fixed frequency saw tooth wave magnitude of 3 V is considered. Open loop transfer function of BDDC in boost mode along with the feedback factor and modulator is obtained (2.39) and plotted in Figure 2.14.

$$sys2 = \frac{-0.002914s^2 - 39.48s + 8.914\times10^{06}}{s^2 + 975.7s + 1.763\times10^{07}} \qquad (2.39)$$

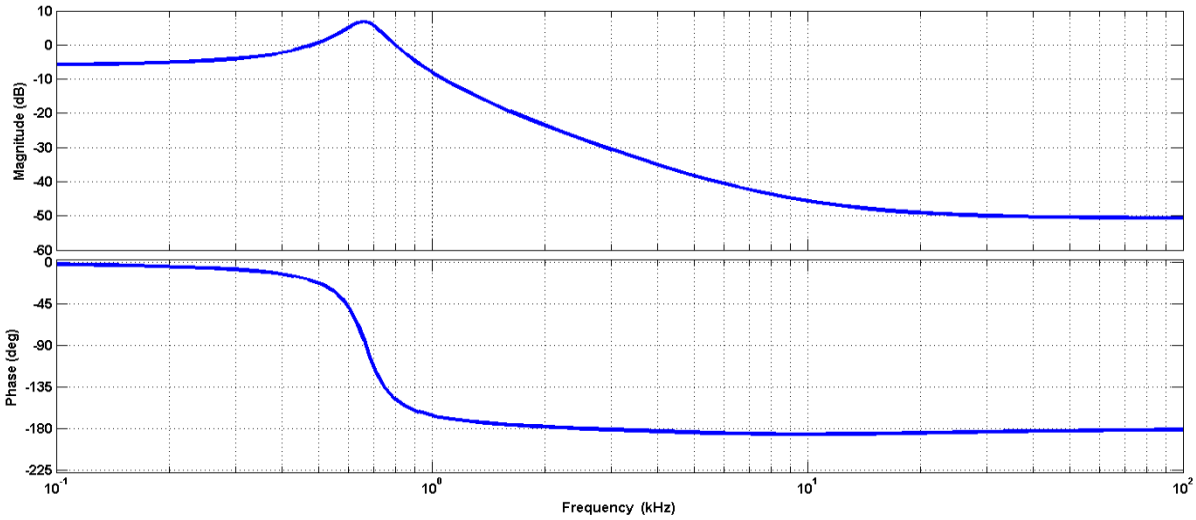


Figure 2.14 Bode plot of open loop BDDC in boost mode with feedback and modulator.

Corresponding to f_C of 2 kHz in Figure 2.14, phase shift of -178^o and gain of -23.5 decibel (dB) are measured. Type III compensator is being selected based on the phase shift introduced by the BDDC in boost mode. Elements of type III compensator are calculated with the help of K factor method in (2.33),(2.34),(2.35),(2.36),(2.37), and (2.38) by assuming the desired PM of 60^o and detailed calculation is given in Appendix-B. After substituting the selected values of resistor and capacitor values in (2.31), the type III compensator forward transfer function for BDDC in boost mode is obtained (2.40) and plotted in Figure 2.15.

$$sys3 = \frac{9.519\times10^6 s^2 + 3.362\times10^{10}s + 2.969\times10^{13}}{s^3 + 1.788\times10^5 s^2 + 7.995\times10^9 s} \qquad (2.40)$$

Loop transfer function of BDDC in boost mode is obtained in (2.41) which combines with the system transfer function, feedback factor, modulator gain and compensator. Loop bode plot of BDDC in buck mode (2.41) is shown in Figure 2.16 and corresponding closed loop unit step response is shown in Figure 2.17 .

$$sys4 = \frac{-2.774\times10^4 s^4 - 4.738\times10^8 s^3 + 8.345\times10^{13} s^2 + 2.986\times10^{17} s + 2.647\times10^{20}}{s^5 + 1.798\times10^5 s^4 + 8.187\times10^9 s^3 + 1.095\times10^{13} s^2 + 1.409\times10^{17} s} \qquad (2.41)$$

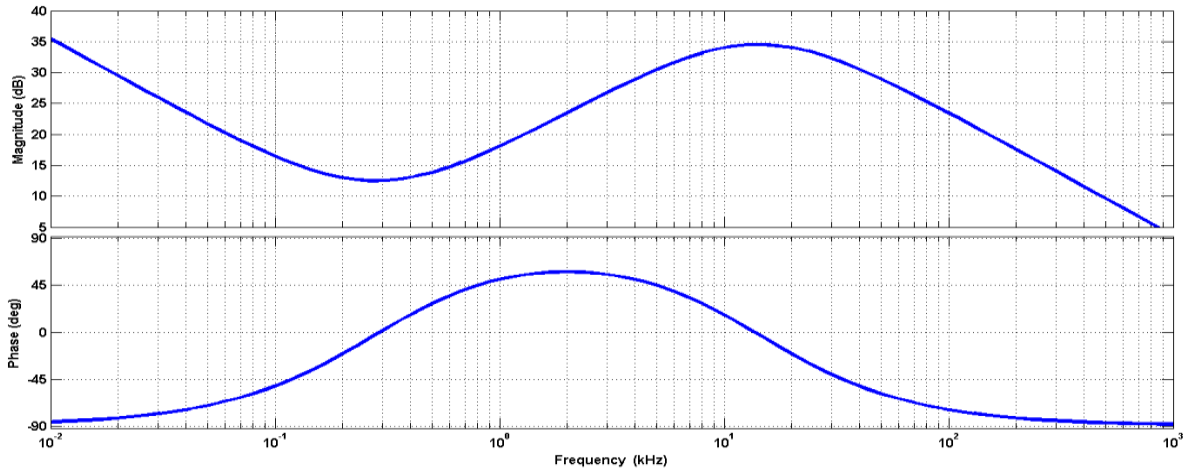


Figure 2.15 Bode plot of type III compensator for BDDC in boost mode.

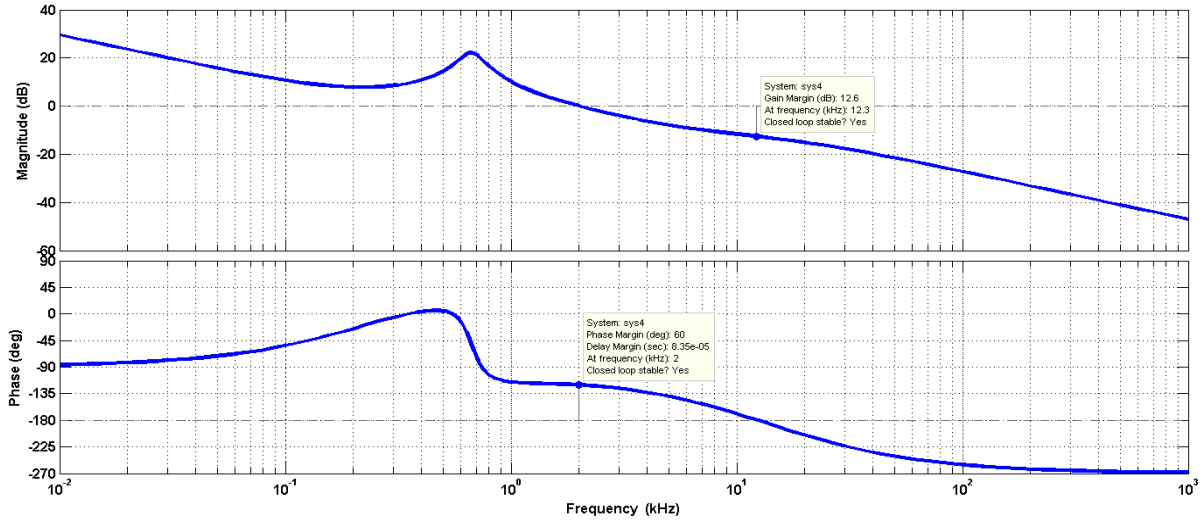


Figure 2.16 Loop bode plot of BDDC in boost mode.

From Figure 2.16, BDDC in boost mode results with PM of 60^{o} which is obtained corresponds to loop cross over frequency of $f_c = 2\ kHz$ and GM of 12.6 dB is obtained corresponds to -180^{0}phase at 12.3 kHz for input voltage of 48 V and load current of 5 A.

From Figure 2.17, BDDC in boost mode results with rise time 90.1 µs, peak over shoot of 1.06 V with 5.63% at 214 µs, settling time of 3.35 ms and steady state value of 1 V for input voltage of 48 V and load current of 5 A.

Loop bode plot and closed loop unit step response of BDDC in boost mode for different input voltages of 40 V, 45 V, 48 V, 51 V, and 55 V are shown in Figure 2.18and Figure 2.19 respectively. Loop bode plot and closed loop unit step response of BDDC in boost mode for different load currents of 1 A, 2 A, 3 A, 4 A and 5 A are plotted in Figure 2.20 and Figure 2.21 respectively.

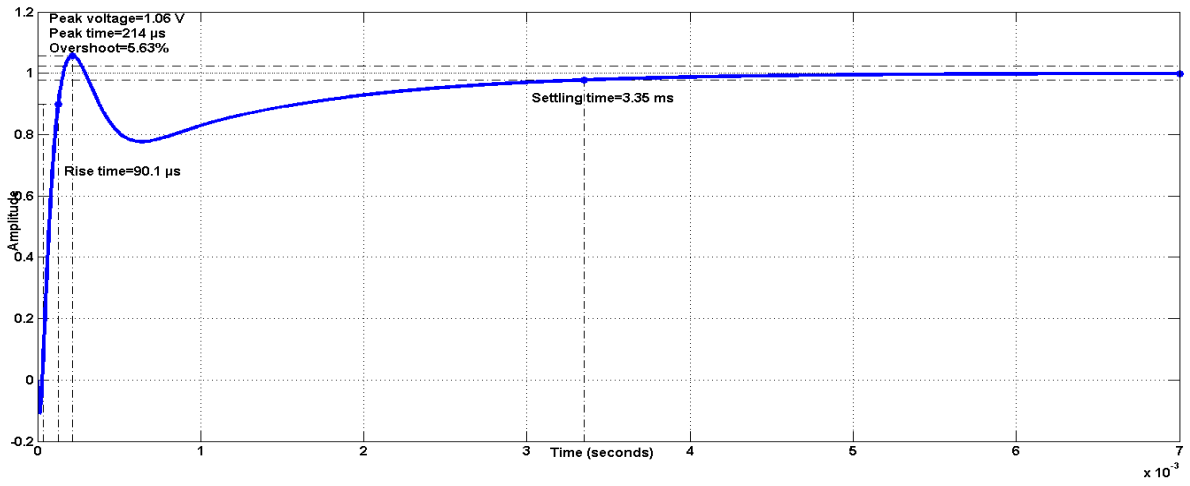


Figure 2.17 Closed loop unit step response plot of BDDC in boost mode

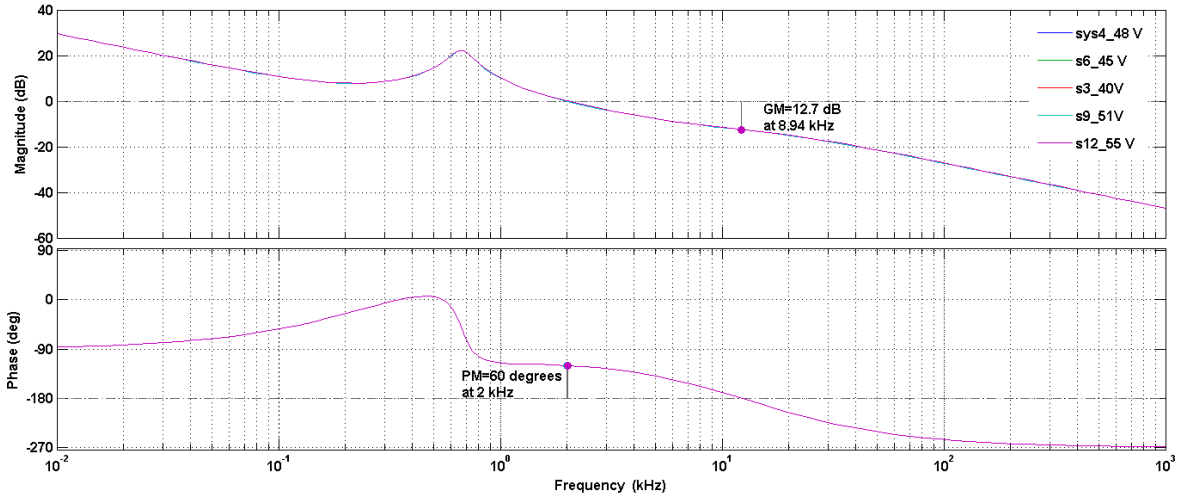


Figure 2.18 Loop bode plot of BDDC in boost mode for different values of input voltage.

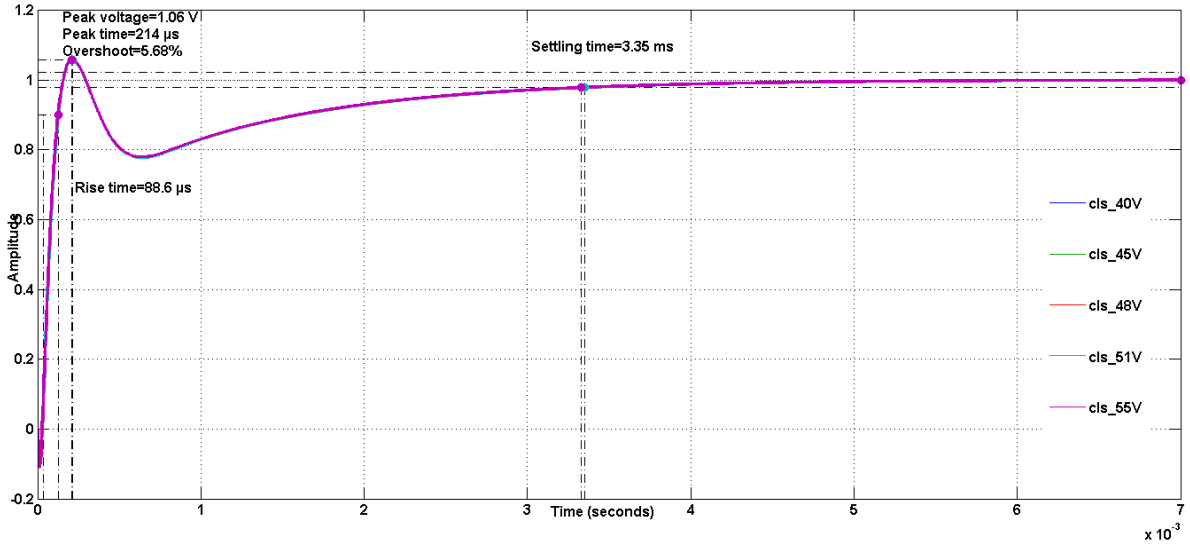


Figure 2.19 Closed loop unit step plot of BDDC in boost mode for different input voltages.

From the loop bode plot as shown in Figure 2.18, GM of 12.7 dB and PM of 60^o are obtained for different values of line voltages of 40 V, 45 V, 48 V, 51 V, and 55 V.

Similarly from the closed loop unit step response as shown in Figure 2.19, BDDC in boost mode for 55 V results with rise time 88.6 µs, peak over shoot of 1.06 V with 5.689% at 214 µs, settling time of 3.35 ms and steady state value of 1 V.

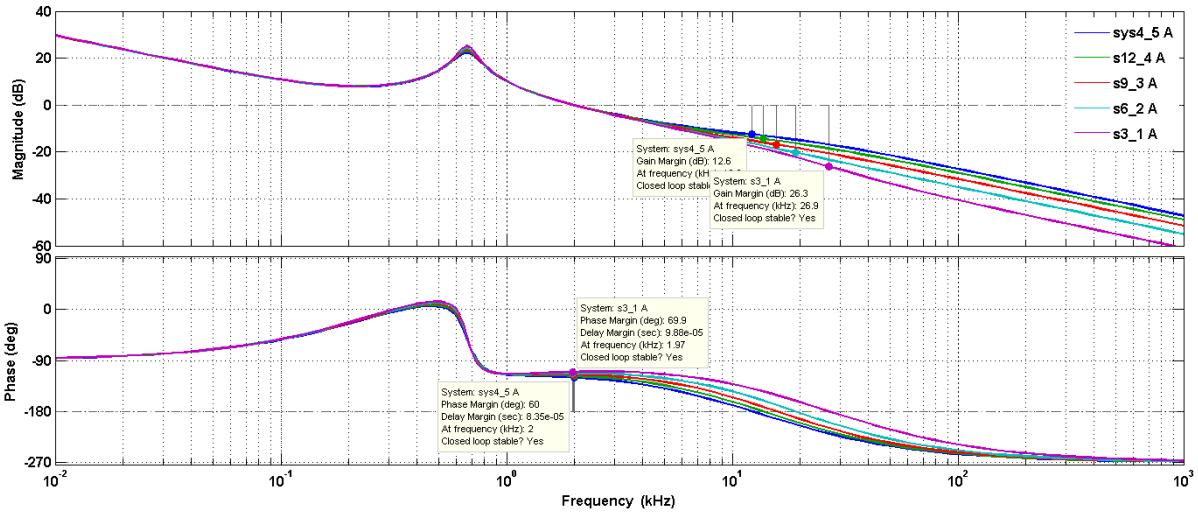


Figure 2.20 Loop bode plot of BDDC in boost mode for different values of load current.

From the loop bode plot as shown in Figure 2.20, GM of 12.7 dB and PM of 50^o are obtained for different values of load current of 1 A, 2 A, 3 A, 4 A and 5 A.

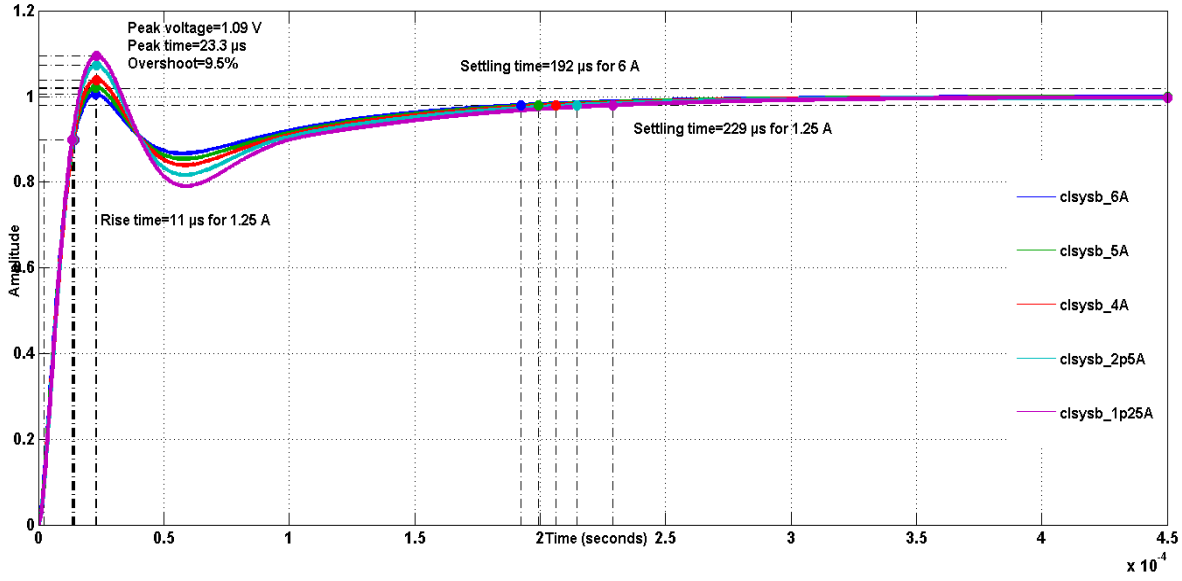


Figure 2.21 Closed loop unit step plot of BDDC in boost mode for different load currents.

From the closed loop unit step response as shown in Figure 2.21, BDDC in boost mode for load current of 5 A results with rise time 85.1 µs, peak over shoot of 1.09 V with 9.09% at

213 µs, settling time of 2.97 ms for 5 A, settling time of 3.08 ms for 1 A and steady state value of 1 V.

GM and PM are within safe limits corresponding to cross over frequency and then the type III compensator stabilises the BDDC in boost mode for different input voltages and load transients.

2.5.4 Design of PID Controller for BDDC in Buck Mode

Proportional-integral-derivative (PID) controller consists of phase lead and lag compensator. Phase lead compensator is a proportional-derivative (PD) controller, and phase lag compensator is a proportional-integral (PI) controller. PID controller can be used to achieve desired phase margin, high loop gain and wide control bandwidth. PID controller is being widely used as controller in most of the power electronics system. The PID controller can be defined by the transfer function, and is represented by the following expression

$$G_{PID}(s) = K_P + \frac{K_I}{s} + K_D s \qquad (2.42)$$

Integral constant K_I leads to increase the gain at low frequency. Derivative constant K_D is responsible for the system stability and transient response by improving PM and f_c at high frequency. Proportional constant part K_P increases the speed of the system response. The PID controllers used in process industry are normally tuned using Ziegler-Nichol's (Z-N) techniques [98]. The block diagram of closed loop PID controller for BDDC in buck is as shown in Figure 2.22. It consists of small signal output to control ratio of BDDC in buck mode transfer function $\left(G_{Buck}(s)\right)$ block, sensor or feedback block $\left(\beta\right)$, PID controller block $\left(G_{PID}(s)\right)$, and PWM gain block $\left(G_{PWM}\right)$.

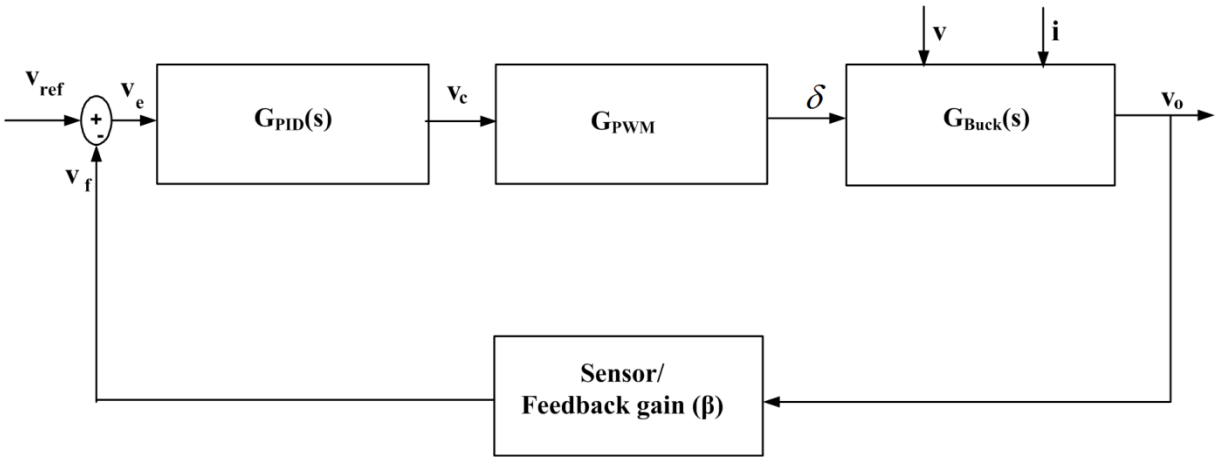


Figure 2.22 Block diagram of closed loop PID Controller for BDDC in buck mode

In order to understand the system behaviour of the BDDC in buck mode against line voltage variations and load transients, the open loop bode plot of small signal transfer function control to output voltage of the BDDC in buck mode is plotted for different input voltage ranges of 60 V, 65 V, 70 V, 75 V and 80 V, and open loop unit step response plot for the same are shown in Figure 2.23 and Figure 3.24 respectively. Similarly, the open loop bode plot of small signal transfer function control to output voltage of the BDDC in buck mode is plotted for different output load current of 1.25 A, 2.5 A, 4 A, 5 A, and 6 A and open loop unit step response plot for the same are shown in Figure 2.25 and Figure 2.26 respectively.

The BDDC in buck mode is stable for any input voltage of 60 V, 65 V, 70 V, 75 V and 80 V, and also the converter system is stable even for the output load current of 1.25 A, 2.5 A, 4 A, 5 A, and 6 A.

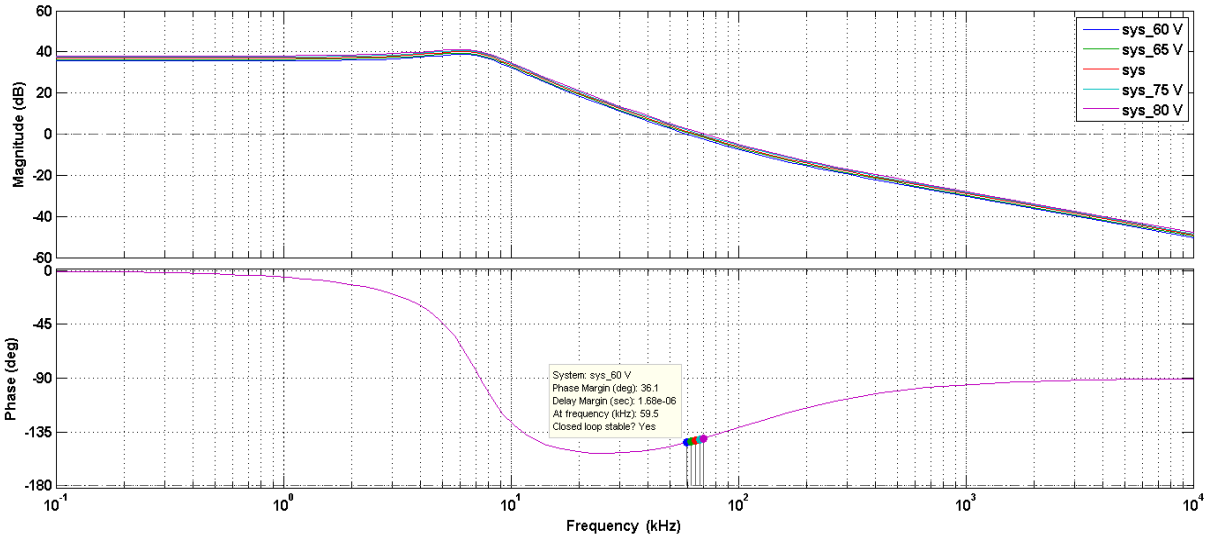


Figure 2.23 Open loop bode for different input voltages of BDDC in buck mode.

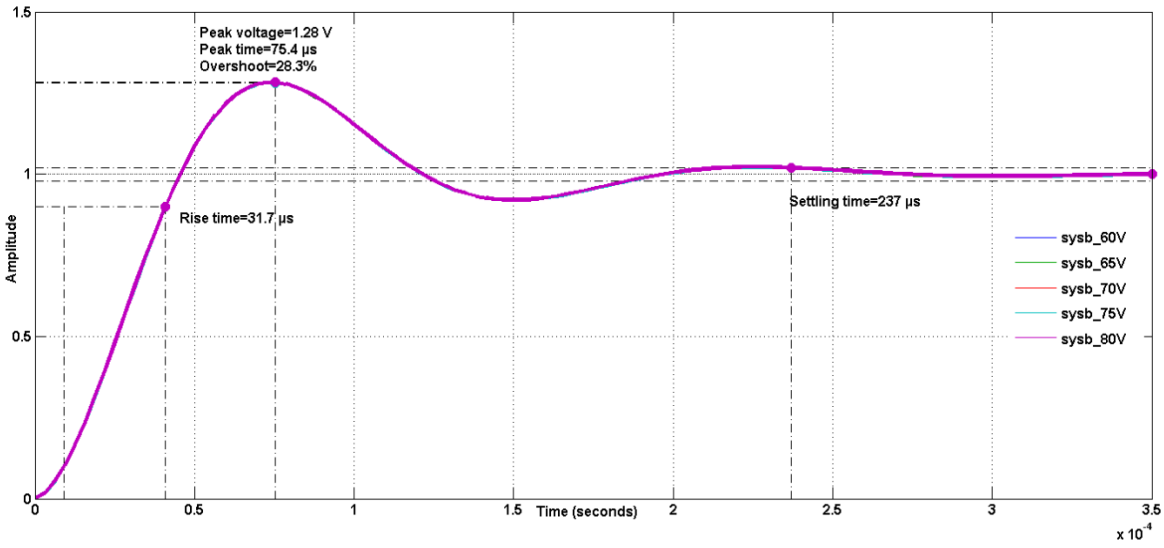


Figure 2.24 Open loop unit step plot of different input voltages of BDDC in buck mode.

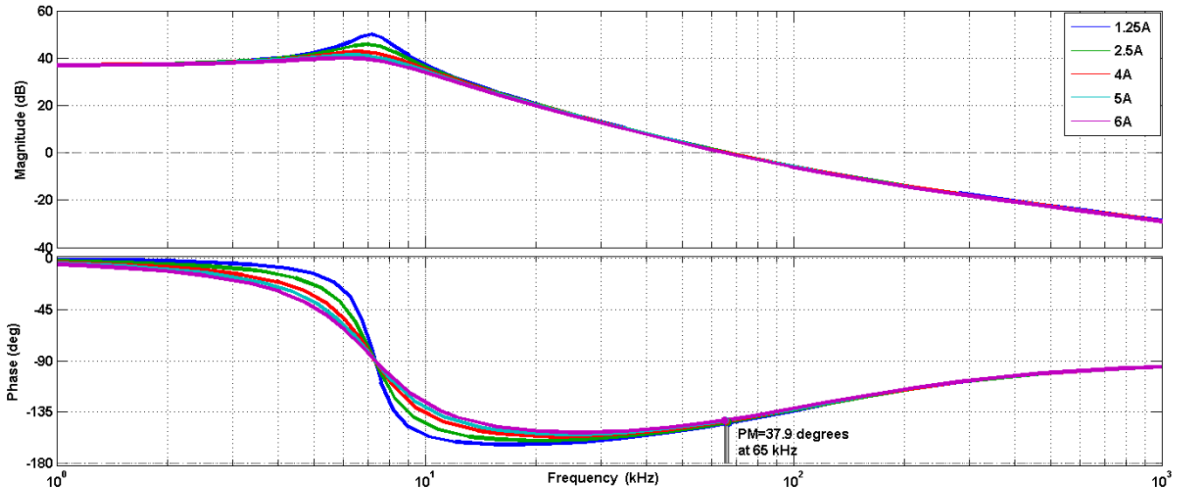


Figure 2.25 Open loop bode plot for different output load currents of BDDC in buck mode.

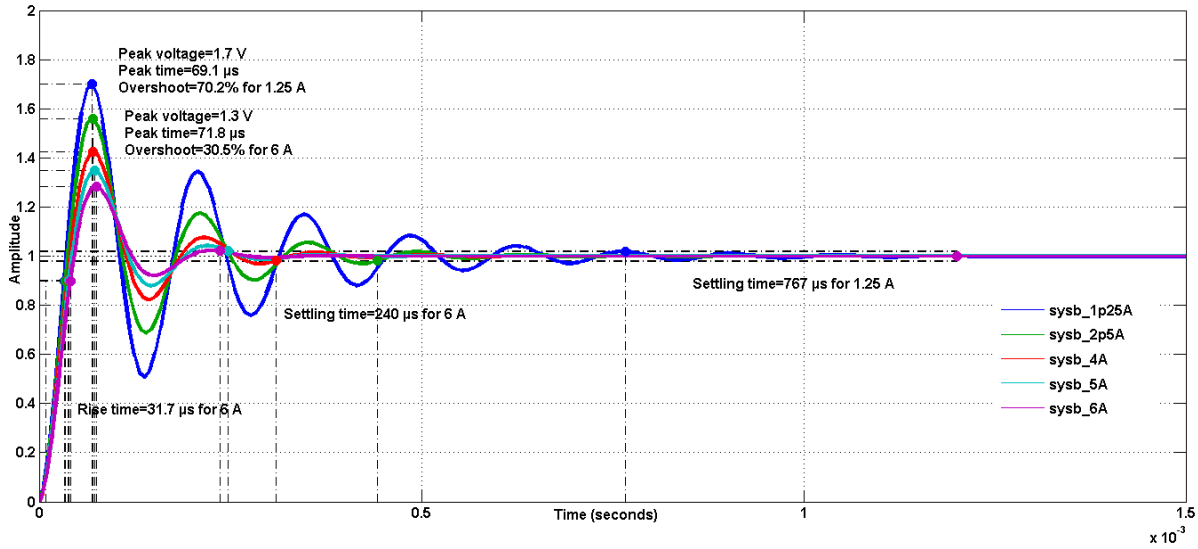


Figure 2.26 Open loop unit step plots for different load currents of BDDC in buck mode.

The open loop transfer function of BDDC in buck mode uses with its forward feedback factor $\left(\beta_1 = \frac{1}{48}\right)$ which is used to convert the output voltage to the reference voltage $\left(V_{ref1} = 1V\right)$ corresponding to desired output voltage of 48 V, and then multiply by the modulator gain $\left(V_{M1} = \frac{1}{3}\right)$ in which fixed frequency saw tooth wave magnitude of 3 V is considered. Open loop transfer function of BDDC in buck mode along with the feedback factor and modulator is given by (2.43)

$$G(s) = \frac{1538.29s + 961.39 \times 10^6}{s^2 + 33394s + 2 \times 10^9} \qquad (2.43)$$

PID controller has been designed for BDDC in buck mode to improve loop gain, crossover frequency and phase margin, zeros of the PID controller are used to cancel out the system's dominant poles. Although this may work, especially when large time delays are present [99, 100]. The transfer function of the PID controller for BDDC in buck mode is given by(2.44)

$$G_{PID}(s) = 9.39 + \frac{17.5\times10^{4}}{s} + 67\times10^{-6}s \qquad (2.44)$$

An equivalent digital controller [88] using bilinear transformation technique in Z domain corresponding to sampling time Ts=10 μs for (2.44) is given by

$$G_{PID}(z) = \frac{23.66z^{2} - 25.05z + 4.885}{z^{2} - 1} \qquad (2.45)$$

Loop transfer function of BDDC in buck mode is obtained in (2.46) which combines with the system transfer function, feedback factor, modulator gain and compensator. Loop bode plot of BDDC in buck mode is shown in Figure 2.27 and corresponding closed loop unit step response is shown in Figure 2.28.

$$G_{Buckclosed}(s) = \frac{0.1031s^{3} + 7.886\times10^{4}s^{2} + 9.297\times10^{09}s + 1.68\times10^{14}}{s^{3} + 33394s^{2} + 2\times10^{9}s} \qquad (2.46)$$

From Figure 2.27, BDDC in buck mode results with PM of 60.3^{o} is obtained corresponds to loop cross over frequency of $f_c = 19.9\ kHz$ and GM of ∞ dB corresponds to -180^{0} phase for input voltage of 70 V and load current of 6 A.

From Figure 2.28, BDDC in buck mode results with rise time 10.5 μs, peak over shoot of 1.1 V with overshoot of 9.88% at 22.2 μs, settling time of 145 μs and steady state value of 1 V for input voltage of 70 V and load current of 6 A.

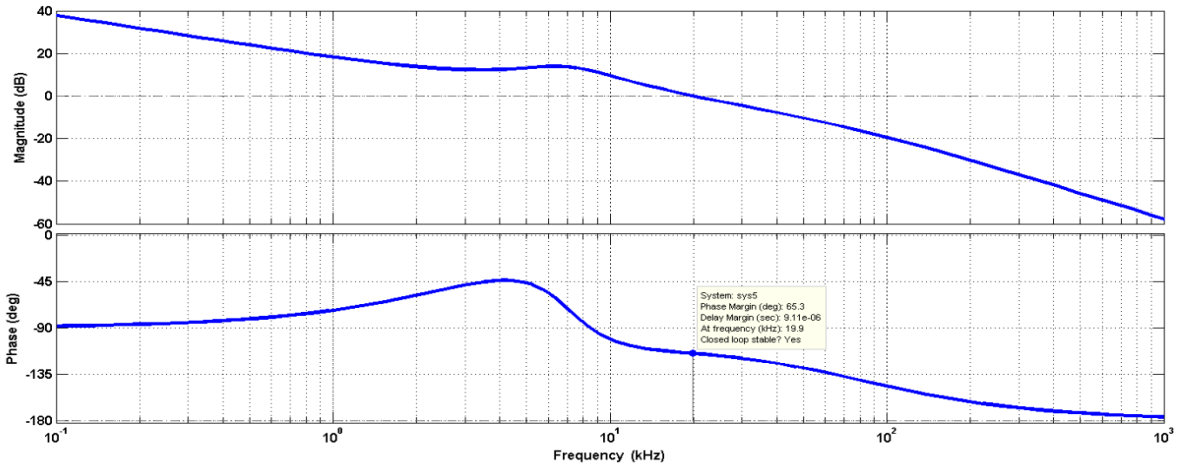


Figure 2.27 Loop bode plot of BDDC in buck mode.

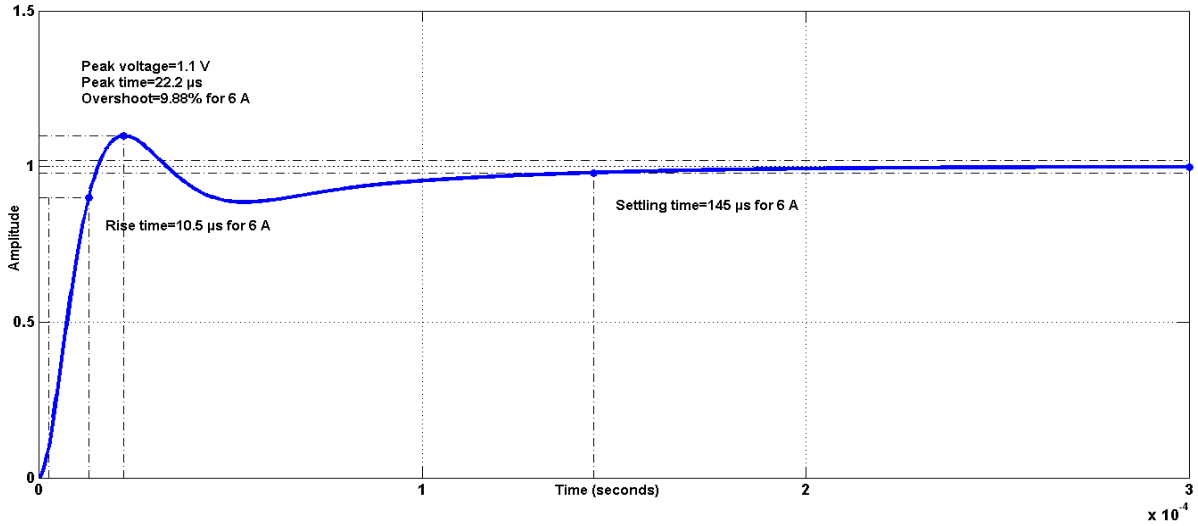


Figure 2.28 Closed loop unit step response plot of BDDC in buck mode.

Loop bode plot and closed loop unit step response of BDDC in buck mode for different input voltages of 60 V, 65 V, 70 V, 75 V, and 80 V are shown in Figure 2.29 and Figure 2.30 respectively.

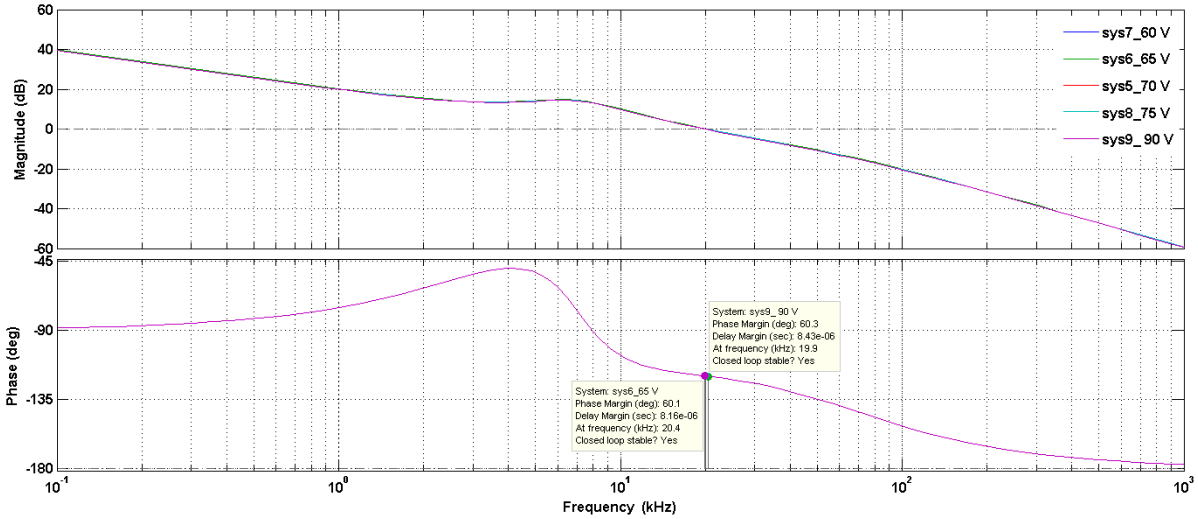


Figure 2.29 Loop bode of BDDC in buck mode for different values of input voltage.

Loop bode plot and closed loop unit step response of BDDC in buck mode for different load currents of 1.25 A, 2.5 A, 4 A, 5 A and 6 A are plotted in Figure 2.31 and Figure 2.32 respectively.

From Figure 2.29, BDDC in buck mode results with PM of 60.3^{o} is obtained corresponds to loop cross over frequency of $f_c = 19.9\ kHz$ and GM of ∞ dB corresponds to -180^{0} phase for different values of input voltages of 60 V, 65 V, 70 V, 75 V, and 80 V.

From Figure 2.30, BDDC in buck mode results with rise time of 11.1 µs, peak over shoot of 1.05 V with overshoot of 4.99% at 22.2 µs, settling time of 166 µs and steady state value of 1 V for input voltage of 80 V.

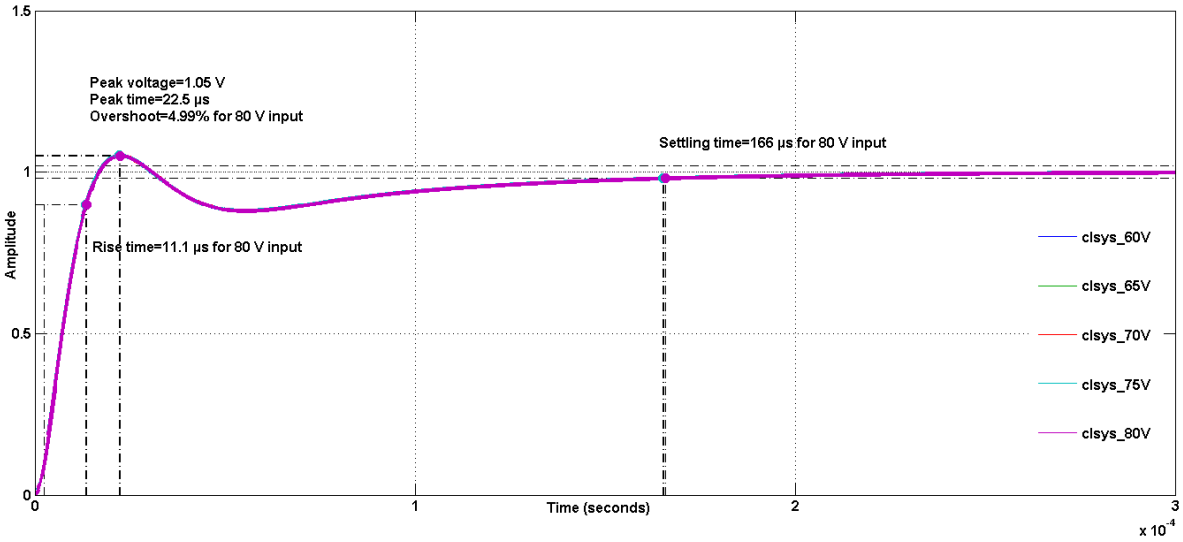


Figure 2.30 Closed loop unit step plot of BDDC in buck mode for different input voltages.

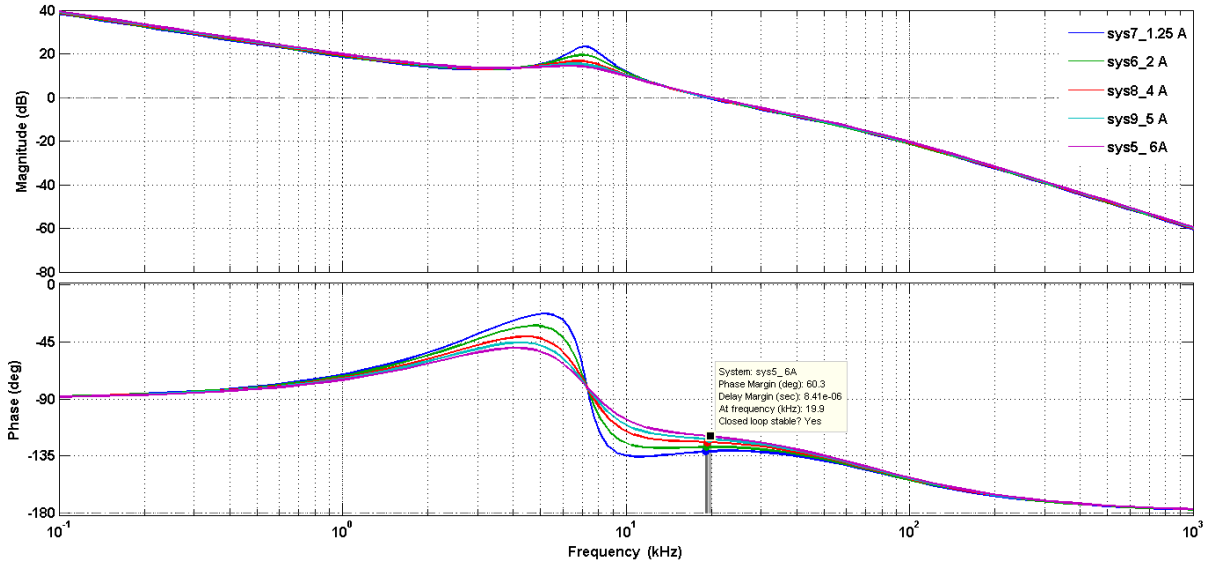


Figure 2.31 Loop bode of BDDC in buck mode for different values of load current.

From Figure 2.31, BDDC in buck mode results with PM of 60.3^{o} is obtained corresponds to loop cross over frequency of $f_c = 19.9\ kHz$ and GM of ∞ dB is obtained corresponds to -180^{0} phase for different values of load current of 1.25 A, 2.5 A, 4 A, 5 A and 6 A.

From Figure 2.32, BDDC in buck mode results with rise time 11.1 µs: peak over shoot of 1.09 V with overshoot of 9.5% at 23.3 µs, settling time of 192 µs for 6 A, settling time of 229 µs for 1.25 A and steady state value of 1 V.

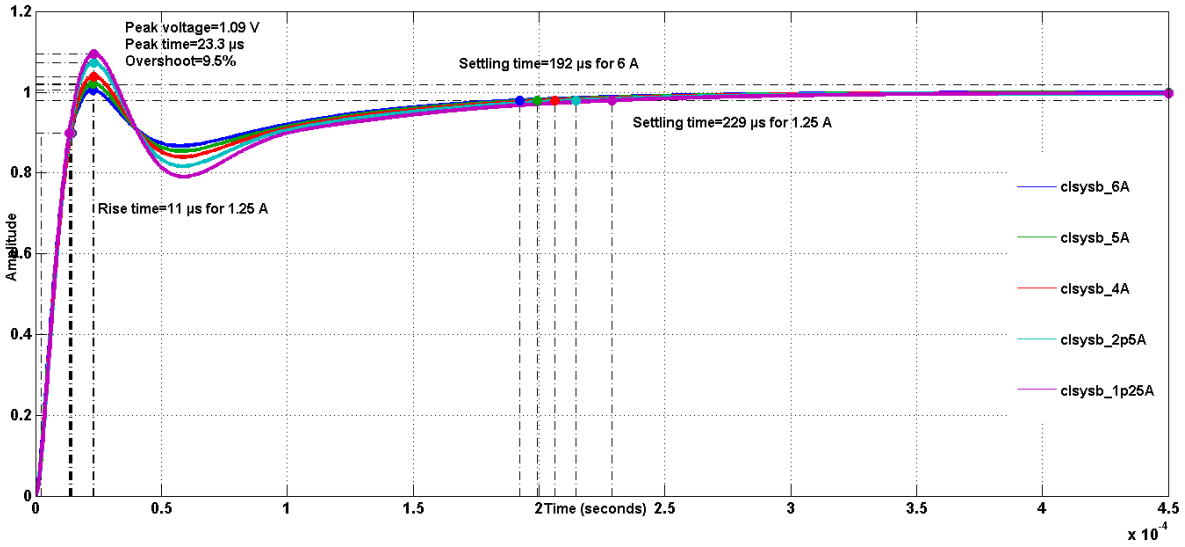


Figure 2.32 Closed loop unit step plot of BDDC in buck mode for different load currents.

The comparative performance of type 3 error amplifier and PID controller on conventional BDDC is as tabulated in Table 2.2.

Table 2.2 Performance of type 3 error amplifier and PID controller on conventional BDDC

Conventional BDDC	Boost mode			Buck mode		
	Type 3 compensator			PID controller		
	t_r (µs)	Overshoot (%)	t_s (ms)	t_r (µs)	Overshoot (%)	t_s (µs)
Line voltage change	88.6	5.689	3.35	11.1	4.99	166
Load current change	85.1	9.09	3.08	11	9.5	229

From the Table 2.2, whenever the line voltage and load current change occurs, type-3 error amplifier for BDDC in boost mode will provide precise output by minimizing the rise time, overshoot voltage and settling time. Similarly, PID controller for BDDC in buck mode improves the performance of the BDDC whenever sudden change in line voltage (minimum to maximum input voltage) and load current (minimum to maximum load) occurs.

2.6 Simulation and Experimentatal results of BDDC

Non-ideal BDDC circuit has been used in the simulation and it has been carried out in MATLAB/SIMULINK software. SimPowerSystem circuit model of BDDC in boost mode and buck mode circuit is as shown in Figure 2.33.

2.6.1 Simulation of Conventional BDDC

To assess the feasibility of the type III error amplifier control strategy for boost mode and PID controller for buck mode, simulations are performed with the specifications as tabulated in Table 2.3 of conventional BDDC power circuit.

Table 2.3 Specification and design parameters of conventional BDDC

Parameters	Boost mode	Buck mode
Supply voltage	48 V ±10% (E_1)	70 V ±10% (E_2)
Output voltage	70 V (V_2)	48 V (V_1)
Load current	5 A (I_2)	6 A (I_1)
Operating frequency	100 kHz (f_s)	100 kHz (f_s)
Duty ratio for nominal values	0.32	0.68
Inductor	120 µH	120 µH
Internal resistance of inductor	10.5 mΩ	10.5 mΩ
Output capacitor	200 µF	4 µF
Internal resistance of capacitor	6.6 mΩ	0.47 Ω
On state resistance of MOSFETs	55 mΩ	55 mΩ
Forward resistance of diodes	17.1 mΩ	17.1 mΩ
Cut-in voltage of diodes	0.7 V	0.7 V

2.6.1.1 Simulation Results and Discussions

In order to understand the behavior of BDDC, simulation circuit shown in Figure 2.33 is carried out for 100 ms duration. BDDC operates as boost DC-DC converter from 0 to 50 ms. Similarly the BDDC operates as buck DC-DC converter from 50 ms to 100 ms. Boost mode average inductor current (I_{LB}) is considered as reference current, which is in the same direction as the initial orientation of I_{LB} from 0 to 50 ms, buck mode average inductor current (I_L) flows opposite to the initial orientation of I_{LB} from 50 ms to 100 ms. During boost mode,

switch S_2 and diode D_1 will conduct, during buck mode switch S_1 and diode D_2 will conduct. BDDC in boost mode carries an average inductor current I_{LB} of 7 A which results in ripple current of 1 A, but BDDC in buck mode carries an average inductor current I_L of 6 A which results in ripple current of 1.2 A as shown in Figure 2.34.

Dynamic response of BDDC in boost mode against input voltage (V_1) variations and load current (I_2) variations using type 3 error amplifier as shown in Figure 2.35 and Figure 2.36 respectively.

In Figure 2.35, when the BDDC operates in boost mode with constant load current I_2 of 5A, it results with negative slope because of RHP zero. When the BDDC operates in boost mode against the input voltage V_1 varied from 48 V to 44 V, 44 V to 50 V, 50 V to 48 V, the desired boost output voltage V_2 has been reached to steady state voltage of 70 V within 5 ms using type 3 error amplifier. In Figure 2.36, when the BDDC operates in boost mode against the load current I_2 varied from 1 A to 3 A, 3 A to 5 A with constant input voltage V_1 of 48 V, the desired boost output voltage V_2 has been reached to steady state voltage of 70 V within 3 ms using type 3 error amplifier.

Dynamic response of BDDC in buck mode against line voltage V_2 variations and load current I_1 variations using PID controller is shown in Figure 2.37 and Figure 2.38 respectively. In Figure 2.37, when the BDDC operates in buck mode with constant load current I_1 of 6 A, when V_2 varied from 70 V to 65 V, 65 V to 68 V, 68 V to 72 V, the desired buck output voltage V_1 has been reached to steady state output voltage of 48 V within 200 µs using PID controller, also minimum overshoot voltage and less oscillations are obtained.

In Figure 2.38, when the BDDC operates in buck mode against the load current I_1 varied from 3 A to 5 A, 5 A to 6 A with constant input voltage V_2 of 70 V, the desired buck output voltage V_1 has been reached to steady state output voltage of 48 V within 0.1 ms using PID controller with minimum overshoot voltage.

From the Figure 2.35, to Figure 2.38, it can be noticed that, at any instant of the load change, output voltage is stabilized at faster rate to the desired values in both the respective boost mode and the buck mode. Also, it can be noticed that, the smaller overshoots and under shoots during the instant of load changes from one load to other load.

2.6.2 Experimental Setup of BDDC

For conventional BDDC in boost mode, gate pulses are generated by the ezdsp TMS320F28335 by comparing control voltage in counts with the up-down counter (saw-tooth voltage) waveform. The compare values are 510 and 240 for BDDC in boost mode and buck

mode respectively, and time base period (TBPRD) register is loaded with a value of 750. The corresponding pulses are generated from the DSP processor are fed to TLP250 driver IC to obtain required magnitude for switching operation of MOSFET switches of BDDC for boost mode and buck mode operation. LA25 current transducers are used for measurement of inductor current (both in boost mode and buck mode), LEM voltage transducers are used to sense the input/output voltage of conventional BDDC.

2.6.2.1 Implementation of Digital Controller for Conventional BDDC

Using direct form-I structure, type III error amplifier digital compensator and digital PID controller is being implemented with the help of TMS320F28335 ezdsp to control the dynamic response of the BDDC either in boost mode or buck mode. IRFP450 MOSFET which is used as the switching device, which has drain-source breakdown voltage 500 V, drain-source on state resistance of 0.33 Ω at 150^0c in converter system to achieve desired output voltage against line and load variation and MBRF2010CT switch mode schottky diode has been used to have low conduction loss and drop. MOSFET is connected with two set of snubber circuit elements of 15 Ω and 10 nF and hence reduces ringing across device substantially to desired level. The stress on the lower diode in buck mode operation has also been reduced significantly with the help of snubber elements of 56 Ω and 1 nF. Each channel output is optically isolated with the help of gate driver IC TLP250. The self-inductance of the converter system to operate in CCM with P42/29 ferrite core is 120.4 μH. Low voltage (48V) and high voltage bus (70V) are precisely maintained constant during the converter testing at 100 kHz operation.

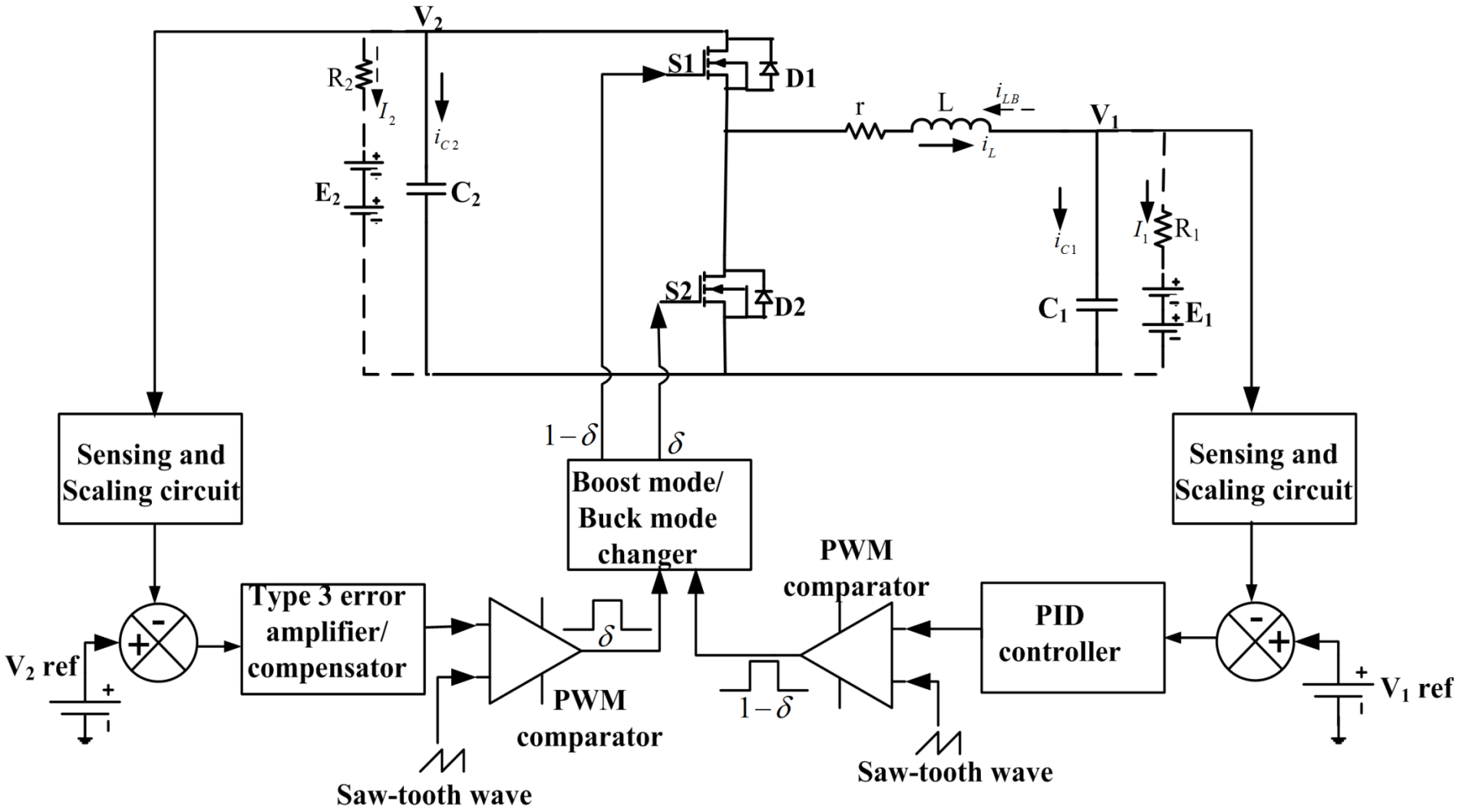


Figure 2.33 Simulation circuit of BDDC.

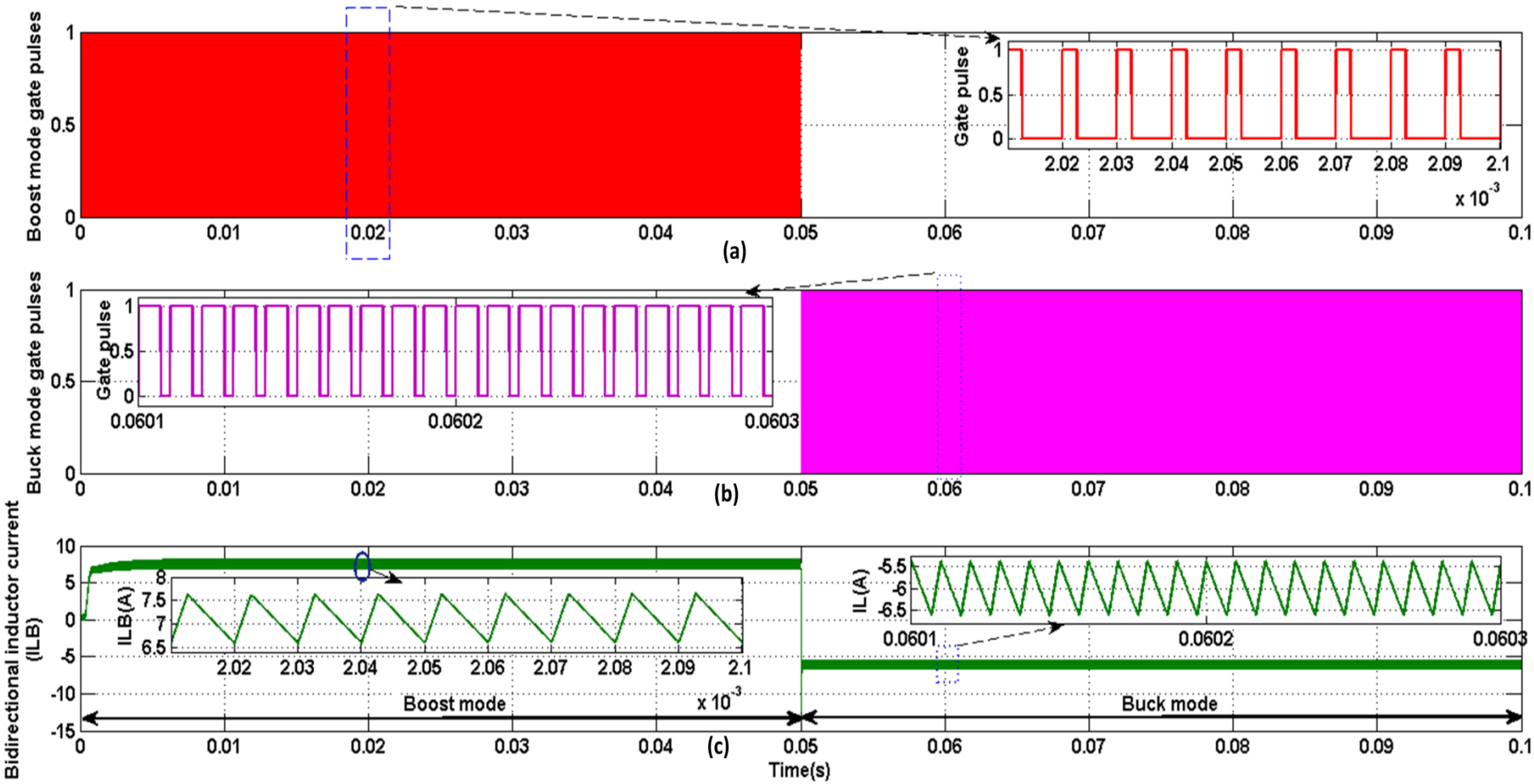


Figure 2.34 Simulation results of BDDC

(a) Boost mode gate pulses. (b) Buck mode gate pulses. (c) Bidirectional inductor current.

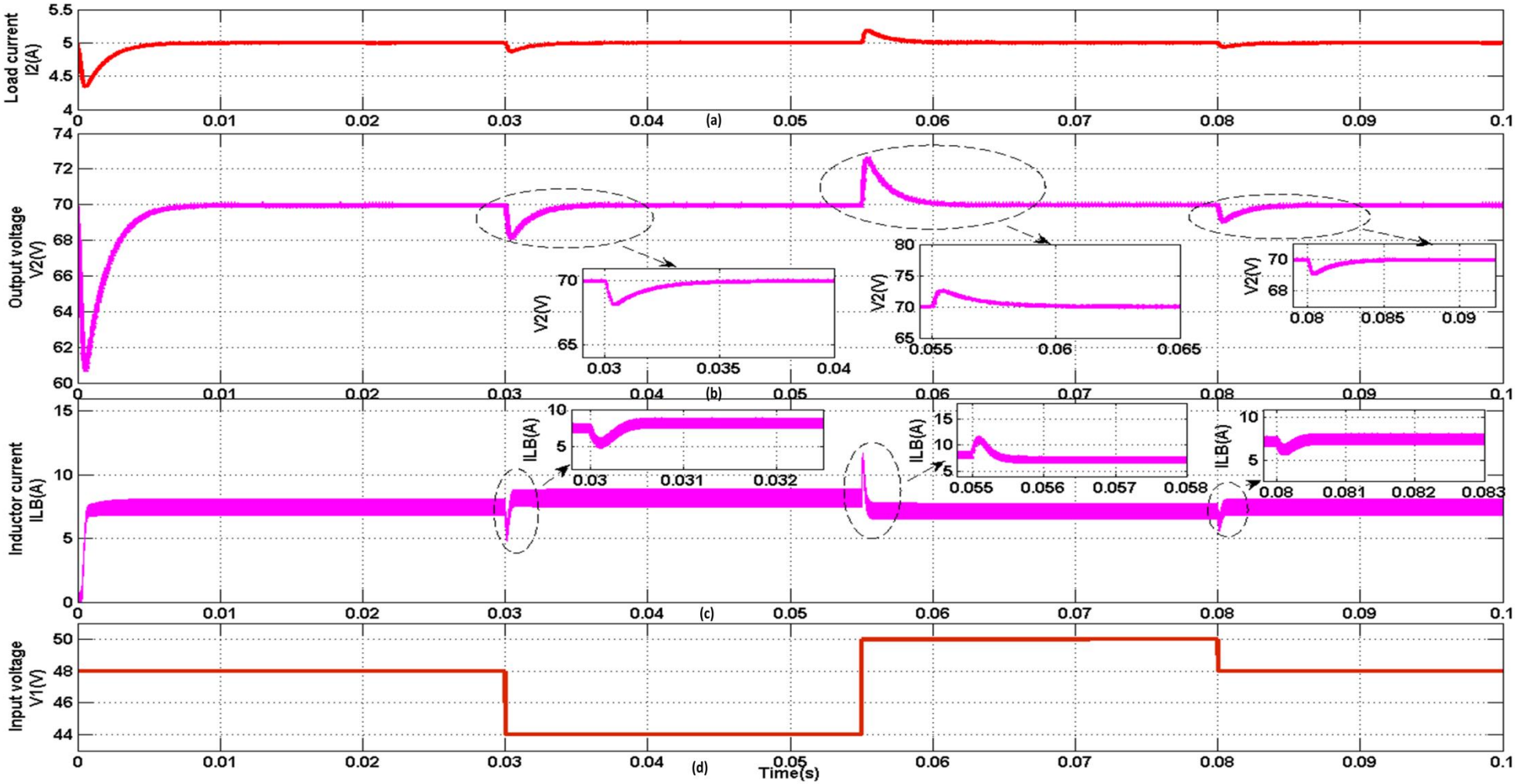


Figure 2.35 Simulation results of BDDC in boost mode against input voltage variation

(a) Load current against input voltage. (b) Output voltage against input voltage. (c) Inductor current against input voltage. (d) Input voltage variation

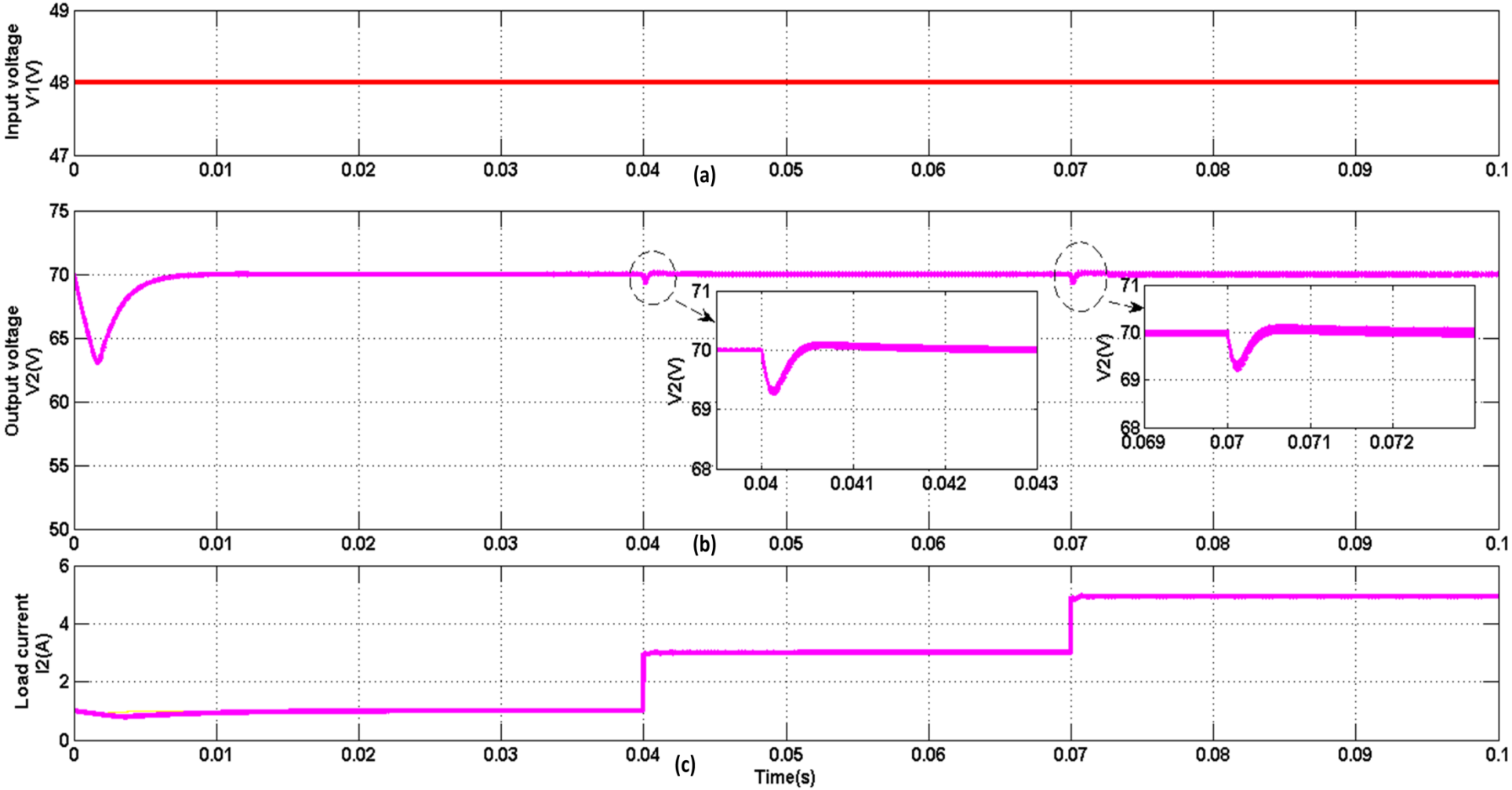


Figure 2.36 Simulation results of BDDC in boost mode against load current variation.

(a) Input voltage (b) Output voltage against load current (c) Load current variation

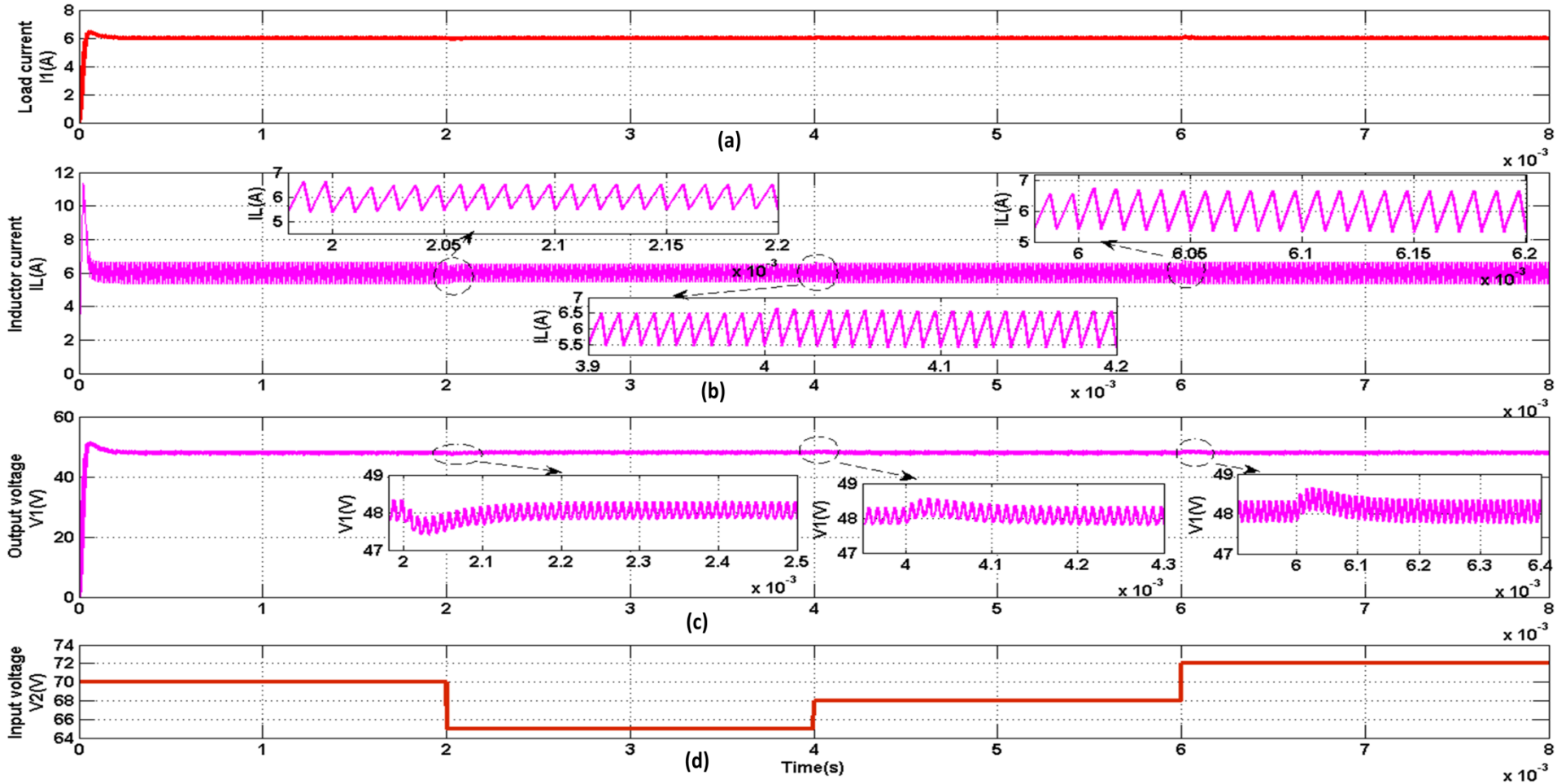


Figure 2.37 Simulation results of BDDC in buck mode against input voltage variation.

(a) Load current against input voltage (b) Inductor current against input voltage (c) Output voltage against input voltage (d) Input voltage variation

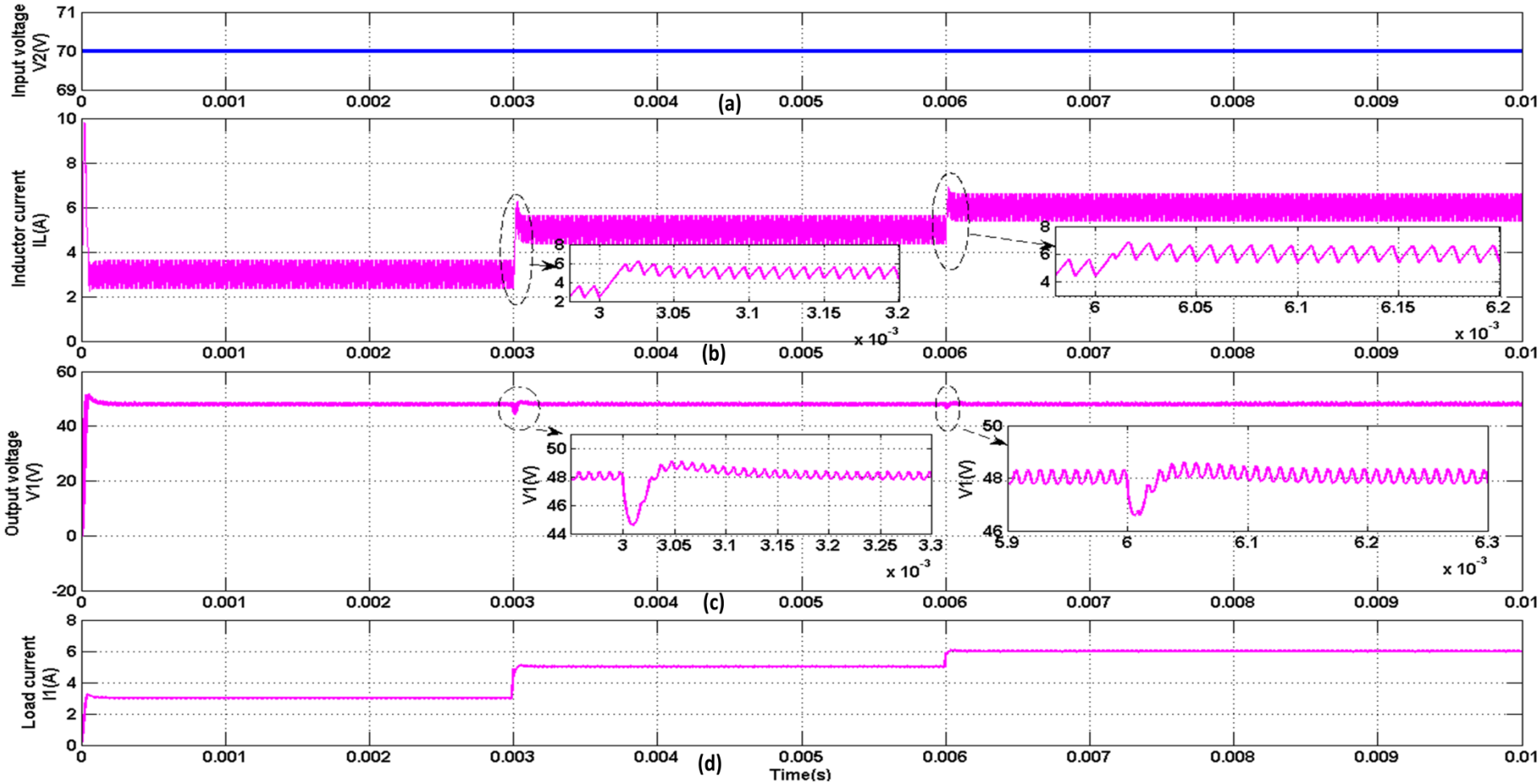


Figure 2.38 Simulation results of BDDC in buck mode against load current variation.

(a) Input voltage. (b) Inductor current against load current. (c) Output voltage against load current. (d) Load current variation.

2.6.2.2 Experimental Results and Discussions

Steady state waveforms of BDDC both in boost mode and buck mode are as shown in Figure 2.39 and Figure 2.40 respectively. Transient response BDDC in boost mode against load current variation using type 3 EA and BDDC in buck mode against load current variation using PID controller are given in Figure 2.41 and Figure 2.42 respectively.

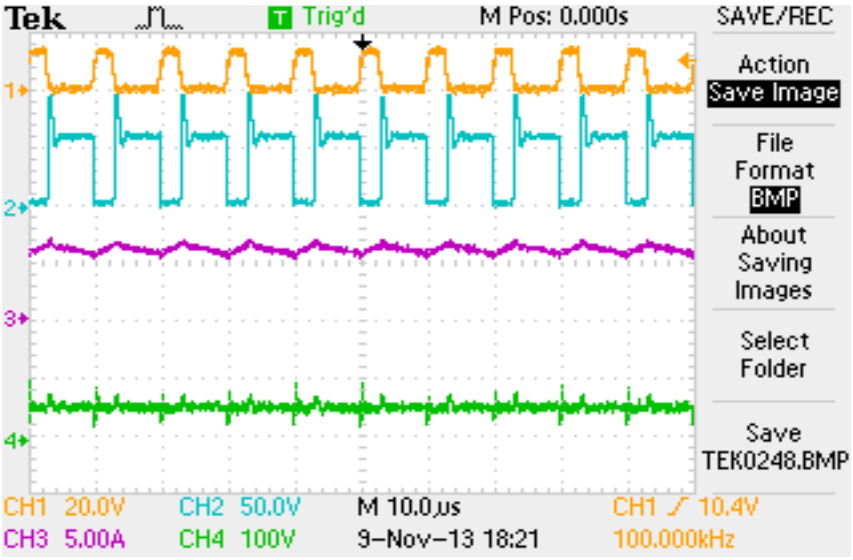


Figure 2.39 Steady state waveforms of BDDC in boost mode.

(Ch1- gate pulse, Ch2- switch voltage, Ch3- inductor current, Ch4- output voltage)

Figure 2.39 shows steady state output voltage (Ch4) for BDDC in boost mode at 70 V , steady state inductor current (Ch3) at 7.2 A while supplying 350 W with input voltage of 48 V. When the gate pulses (Ch1) are applied to turn on the switch S2, voltage across the switch (Ch2) results with 48 V during off time of gate pulses.

Figure 2.40 shows steady state output voltage (Ch4) for BDDC in buck mode at 48 V, steady state inductor current (Ch2) at 6 A while supplying 288 W with input voltage of 70 V. When the gate pulses (Ch1) are applied to turn on the switch S1, voltage across the switch (Ch3) results with 48 V during off time of gate pulses.

Dynamic performances of BDDC in boost mode against load current I_2 varied from 1 A to 5 A with constant input voltage of 48V using type 3 error amplifier is as shown in Figure 2.41. In Figure 2.41, the performance of BDDC in boost mode with the sudden step change in load current I_2 (Ch4) varied from 1 A to 4 A and load current I_2 (Ch4) varied from 2.5 A to 5 A are shown in Figure 2.41(a) and Figure 2.41(b) respectively, with constant input voltage V_1 (Ch1) of 48 V, type 3 error amplifier provides steady state output voltage V_2 (Ch3) of 70 V within 100 ms.

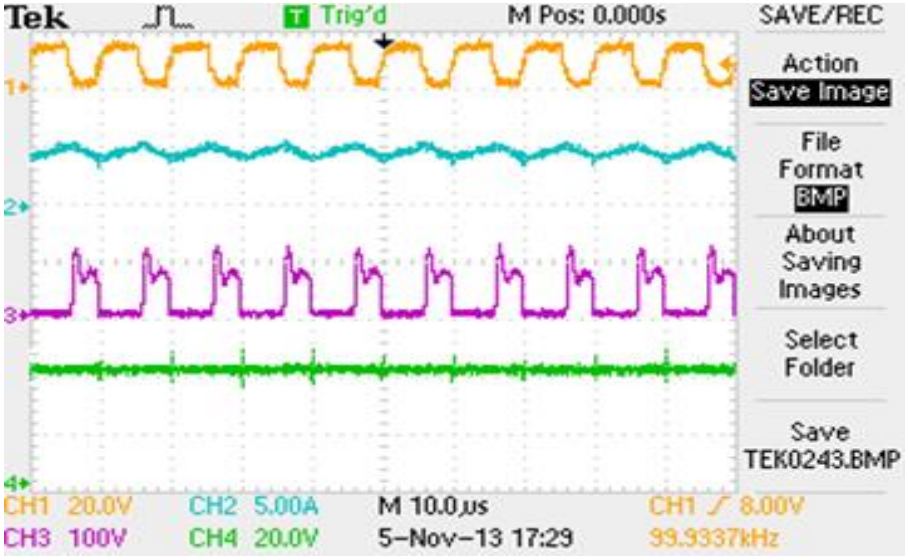
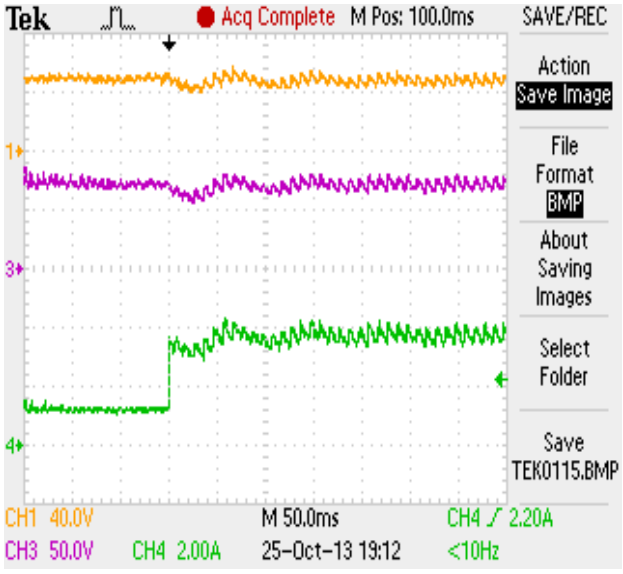
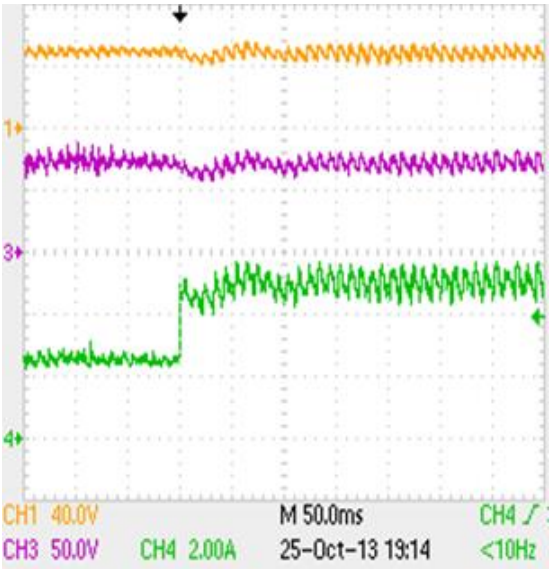


Figure 2.40 Steady state waveforms of BDDC in buck mode

(Ch1- gate pulse, Ch2- inductor current, Ch3- switch voltage, Ch4- output voltage)





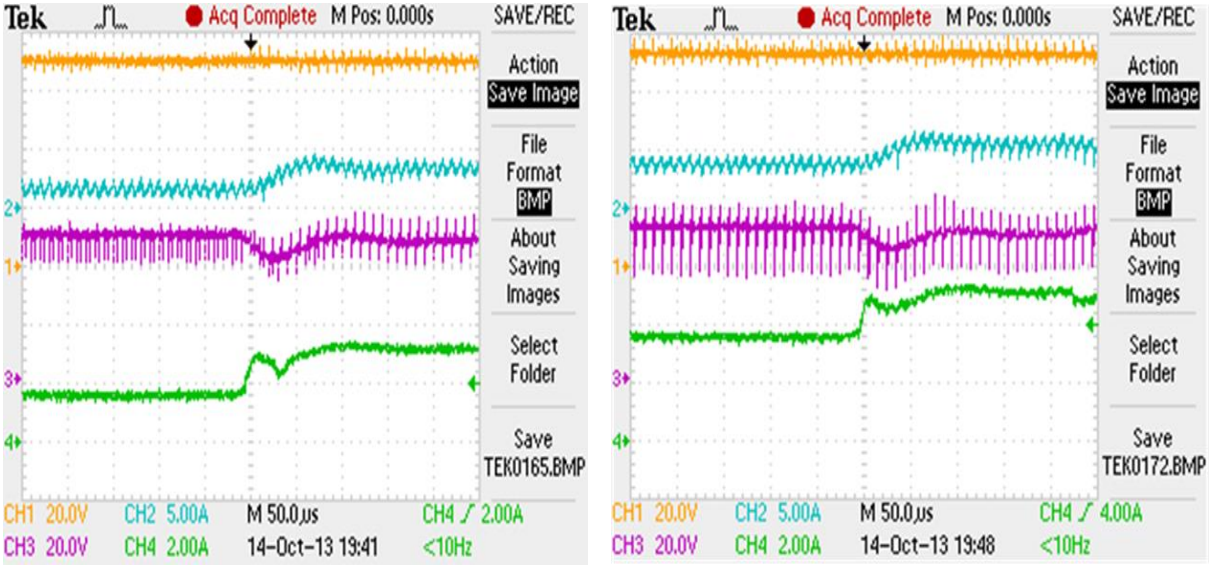
(a) Load current varied from 1A to 4 A (b) Load current varied from 2.5 A to 5 A

Figure 2.41 Experimental results of BDDC in boost mode against load current I_2 variation using type 3 EA.

(Ch1- input voltage $V_1 = 48V$, Ch3- output voltage V_2 , Ch4- load current)

Practical waveforms of BDDC in boost mode against load current I_2 varied from 1 A to 5 A with constant input voltage V_1 of 48 V , the desired output voltage V_2 of 70 V is obtained using type 3 error amplifier which is closely matches with the simulated result.

Dynamic performances of BDDC in buck mode against load current I_1 varied from 1 A to 5 A with constant input voltage V_2 of 70 V using PID controller is as shown in Figure 2.42.



(a) Load current varied from 1.75 A to 3 A. (b) Load current varied from 3.75 A to 5 A.

Figure 2.42 Experimental results of BDDC in buck mode against load current I_1 variation using PID controller.

(Ch1- input voltage V_2, Ch2- inductor current I_L, Ch3- output voltage V_1, Ch4- load current)

In Figure 2.42, the performance of BDDC in buck mode with the sudden step change in load current I_1 (Ch4) varied from 1 A to 4 A and load current I_1 (Ch4) varied from 2.5 A to 5 A are shown in Figure 2.42(a) and Figure 2.42(b) respectively, with constant input voltage V_2 (Ch1) of 70 V, PID controller provides steady state output voltage of V_1(Ch3) 48 V within 150 µs and steady state inductor current (Ch2) at 5 A.

Practical waveforms of BDDC in buck mode against load current I_1varied from 1 A to 5 A with constant input voltage V_2 of 70 V, the desired output voltage V_1 of 48 V is obtained using PID controller which closely matches with the simulated result.

2.7 Conclusion

A comprehensive analysis, design, dynamic analysis using state space averaging technique of conventional bidirectional dc-dc converter has been carried out. Design of type 3 error amplifier controller for BDDC in boost mode and design of PID controller for BDDC in buck mode has been carried out, and performance of type 3 EA for boost mode and PID controller for buck mode of conventional BDDC are also carried out.

From the analysis, design optimisation, modelling and design of controller for conventional bidirectional dc-dc converter, the following conclusions are drawn

(i) With the help of type 3 error amplifier for boost mode, phase margin of 60^0 and gain margin of 12.7 dB are obtained corresponds to cross over frequency.

(ii) With the help of PID controller for buck mode, phase margin of 60.3^o is obtained corresponds to cross over frequency.

(iii) Type 3 error amplifier and PID controller make the BDDC as stable against the line or load change occur.

From the simulation and experimentation, the following conclusions are drawn

(i) Only common inductor is enough to achieve bidirectional operation of the non-isolated BDDC. Optimistic selection of snubber circuit minimizes the parasitic impedance effect at 100 kHz operation of BDDC.

(ii) Design and implementation of 350 W BDDC with hard switching operation is tested against load variation in both boost mode and buck mode separately.

(iii) Design and implementation of BDDC with hard switching is being tested using type III error amplifier for boost mode and PID controller for buck mode against load current changes. Experimental results indicate type III error amplifier for boost mode and PID controller for buck mode provide the less oscillation during steady state and fast transient response during load transients.

(iv) Results obtained during load transition in practice are closely matches with the simulated results.

CHAPTER 3: DESIGN, MODELLING, CONTROL, SIMULATION AND EXPERIMENTATION OF THREE-PHASE INTERLEAVED BIDIRECTIONAL DC-DC CONVERTER

[This chapter emphasizes on the design, steady state analysis, dynamic analysis using state space averaging technique, design of type 3 error amplifier and fuzzy logic controller for three-phase interleaved bidirectional dc-dc converter. Performance of type 3 error amplifier controller and fuzzy logic controller for three-phase interleaved bidirectional dc-dc converter is also emphasized. This chapter also describes the simulation model of type 3 error amplifier for boost mode and PID controller for buck mode based three phase interleaved bidirectional dc-dc converter is developed in MATLAB simulation platform. Several simulation results are obtained for steady state, transient response for both the variations in input voltage and load current changes. Simulation and experimental results of three-phase IBDDC for load transients are compared in this chapter].

3.1 Introduction

In order to achieve the reduction of either voltage or current stress on the power circuit elements, and better efficiency, a single power converter requires multiple devices in parallel to handle higher magnitude of currents. Multi-phase interleaved bidirectional dc-dc converter offers a significant input current ripple reduction and hence minimizes the size of filter components and results in cost reduction. Optimal selection on the number of phases in design [22] of IBDDC results with the current ripple cancellation, high ripple frequency, and higher efficiency. Three-phase IBDDC has three inductors as compared to single phase BDDC, and it increases the complexity. Three phase IBDDC operates in continuous conduction mode have better utilization of switching devices, lower conduction loss, and reduced electromagnetic interference. An interleaved converter operates in discontinuous mode has reduction of inductor size, fast transient response, increased ripple current and parasitic ringing [17]. With the help of interleaving technique, the total current through an inductor of IBDDC can be easily reduced, current stress on the both low voltage and high voltage side, and resulting with the reduced size of the filter components. Mathematical modelling of interleaved bidirectional converter is essential to design a proper linear controller, leads to maintain equal current in each phase of the converter. In order to apply linear control theory, nonlinearity should be averaged and linearized. The modelling and analysis of IBDDC in boost mode and buck mode is presented using state space averaging (SSA) method [18-20]. The K factor method is defined with a few algebraic equations to achieve preferred cross over frequency and the phase margin. Advanced power devices and

control strategy is required to achieve high efficiency and high frequency operation. Digital signal processor (DSP) is suitable for control of high frequency operation of the IBDDC either in boost mode or in buck mode.

A voltage mode control of IBDDC in CCM and design of non-isolated IBDDC in boost mode and buck mode is presented. The operating principle, steady state and small signal analysis of non-isolated IBDDC are described. Stability analysis of the IBDDC is described with the help of K factor method [21]. Type III error amplifier/compensator and fuzzy logic controller is fully implemented using ezdspTMS320F28335 processor. Design and implementation of 350 W, 100 kHz three-phase IBDDC has also been described. Simulation of three phase IBDDC is carried out to test the design and the performance of the converter using MATLAB/SIMULINK SimPowerSystem; the same converter also been experimentally tested in steady state and dynamic load change when the converter operates in either boost or buck mode. Analysis is carried out for 32% duty ratio (D) in boost mode and 68% duty ratio (D') in buck mode of three-phase IBDDC.

3.2 Principle Operation of Three Phase Interleaved Bidirectional DC-DC Converter

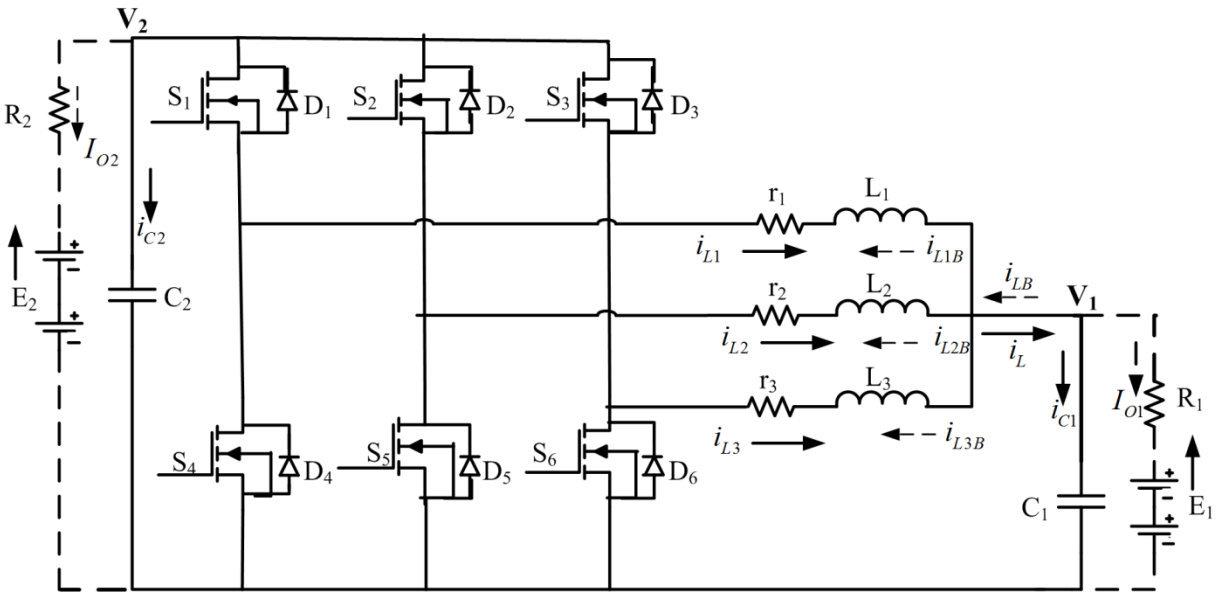


Figure 3.1 Basic circuit diagram of three-phase interleaved bidirectional dc-dc converter.

Figure 3.1 shows the basic circuit configuration of three phase interleaved bidirectional dc-dc converter (IBDDC) consisting of 3 single stage bidirectional dc-dc converter and normally operates either in boost mode or buck mode. Input and output capacitor is common in IBDDC. Each of the phase current in boost mode is equal to $\frac{1}{3}$ times the input current, but

phase current in buck mode will be equal to $\frac{1}{3}$ times the load current [38-40]. Each phase gate pulse and inductor currents are shifted by 120^0. Depending on the duty ratio of the IBDDC, conduction in switches may overlap or not. When the IBDDC operates in overlapped mode, the supply current ripple decreases. Input current ripple in boost /buck mode has 3 times the switching frequency and will be equal to the sum of individual phase currents. Switching devices can be controlled by providing phase shifted pulses. Phase of each pulse can be calculated by the relation $\left(\frac{2\pi}{N}\right)$ where 'N' is the number of phases. Three boost/buck converters are connected in parallel to increase the power by three times.

Considering the direction of inductor current as the reference, three-phase IBDDC converter behaves as a three-phase boost dc-dc converter in one direction, and as a three-phase buck dc-dc converter in other direction. When the Three-phase IBDDC operates as boost dc-dc converter, switches S_4, S_5 and S_6 conduct for DT_s duration, and diodes D_1, D_2 and D_3 conduct for $(1-DT_s)$ duration. When the Three-phase IBDDC operates as buck dc-dc converter, switches S_1, S_2 and S_3 conduct for $D'T_s$ duration, and diodes D_4, D_5 and D_6 conduct for $(1-D'T_s)$ duration.

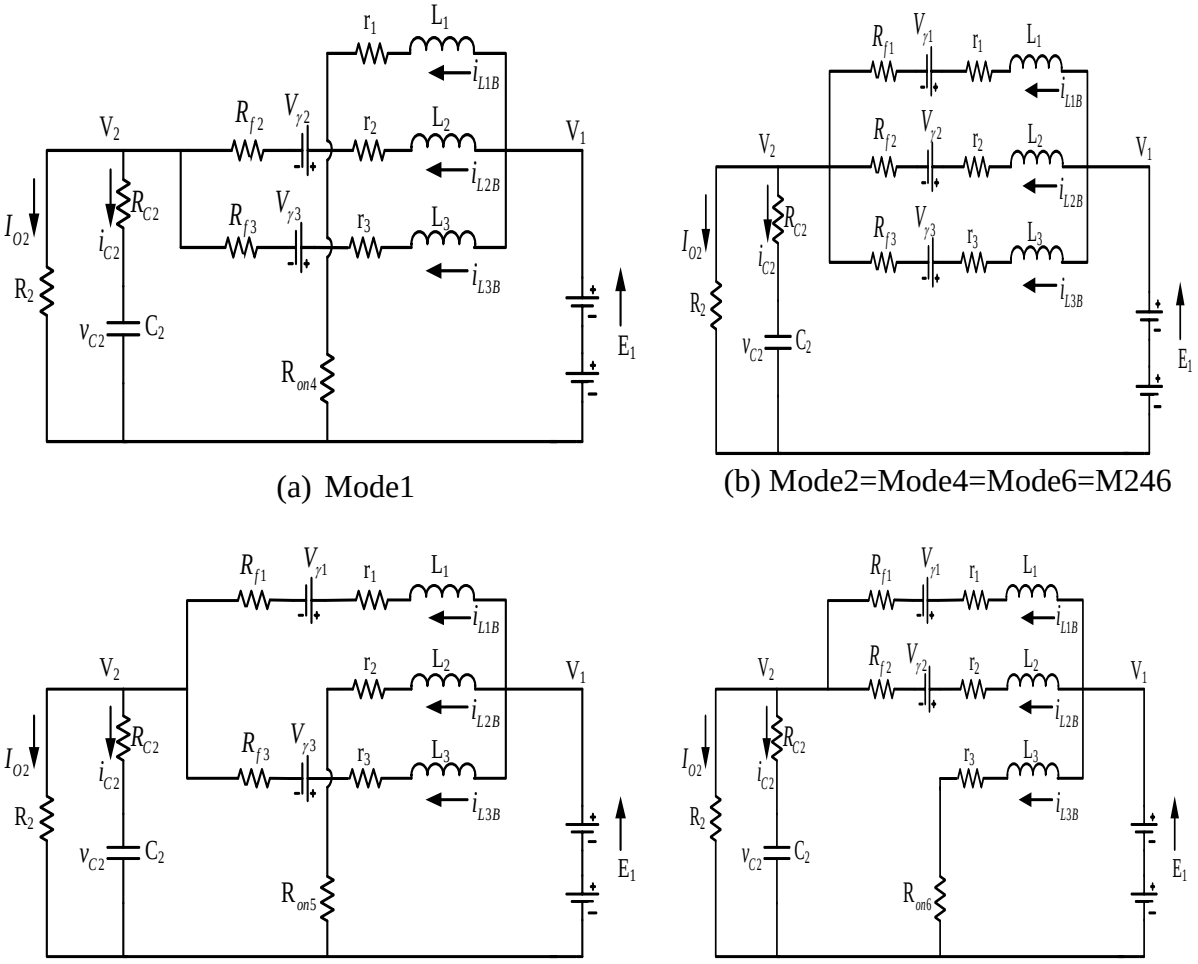
3.3 Steady State Analysis of Three-Phase IBDDC in Boost Mode

The operation of the three-phase IBDDC in boost mode operates in CCM is explained with the non-ideal equivalent circuits, and the conduction of the switches with different states is as shown in Figure 3.2. The waveforms corresponding to three phase IBDDC in boost mode operates in CCM are as shown in Figure 3.3 for duty ratio D of 32%.

Three-phase IBDDC in boost mode operates in CCM, when the duty ratio D lies between 0 and $\frac{1}{3}$ with $E_2 = 0, R_1 = 0$ and $i_{C1} = 0$. It has 6 modes of operation and each of the mode is explained as follows:

Mode1: At t=0, gate pulse is applied to the switch S_4 i.e during $d1 = DT_s$, switch S_4, diodes D_2 and D_3 conduct, i_{L1B} increases linearly and i_{L2B}, i_{L3B} decreases linearly. The net i_{LB} becomes sum of slopes of i_{L1B}, i_{L2B} and i_{L3B}. Initially charged capacitor (C_2) supplies the power to the load (R_2). An equivalent circuit of mode1 of three-phase IBDDC in boost stage is as shown in Figure 3.2(a).

Mode2=Mode4=Mode6=M246: During $d2 = d4 = d6 = \left(\frac{2}{3} - D\right)T_s$, diodes D_1, D_2 and D_3 conduct. i_{L1B} increases linearly and i_{L2B}, i_{L3B} decreases linearly. The net i_{LB} will be sum of the slopes of i_{L1B}, i_{L2B} and i_{L3B}. Energy stored in the inductors supply the power to the load as well as charges the capacitor C_2. An equivalent circuit of mode2 of three-phase IBDDC in boost stage is as shown in Figure 3.2(b).



(a) Mode1

(b) Mode2=Mode4=Mode6=M246

(c) Mode3

(d) Mode5

Figure 3.2 Equivalent circuits of three-phase IBDDC in boost mode with different states

Mode3 : At $t = \frac{T_s}{3}$, gate pulse is applied to the switch S_5, i.e During $d3 = DT_s$, switch S_5, diodes D_1 and D_3 conduct. i_{L2B} increases linearly and i_{L1B}, i_{L3B} decreases linearly. The net i_{LB} becomes sum of slopes of i_{L1B}, i_{L2B} and i_{L3B}. Initially charged capacitor (C_2) supplies the power to the load (R_2). An equivalent circuit of mode3 of three-phase IBDDC in boost stage is as shown in Figure 3.2(c).

Mode5 : At $t = \frac{2T_s}{3}$, gate pulse is applied to the switch $S_{6,}$ i.e During $d5 = DT_s$,switch S_6 , diodes D_1 and D_2 conduct. i_{L3B} increases linearly and i_{L1B}, i_{L2B} decreases linearly. The net i_{LB} will be sum of the slopes of i_{L1B}, i_{L2B} and i_{L3B}. Initially charged capacitor (C_2) supplies the power to the load (R_2). An equivalent circuit of mode5 of three-phase IBDDC in boost stage is as shown in Figure 3.2(d).

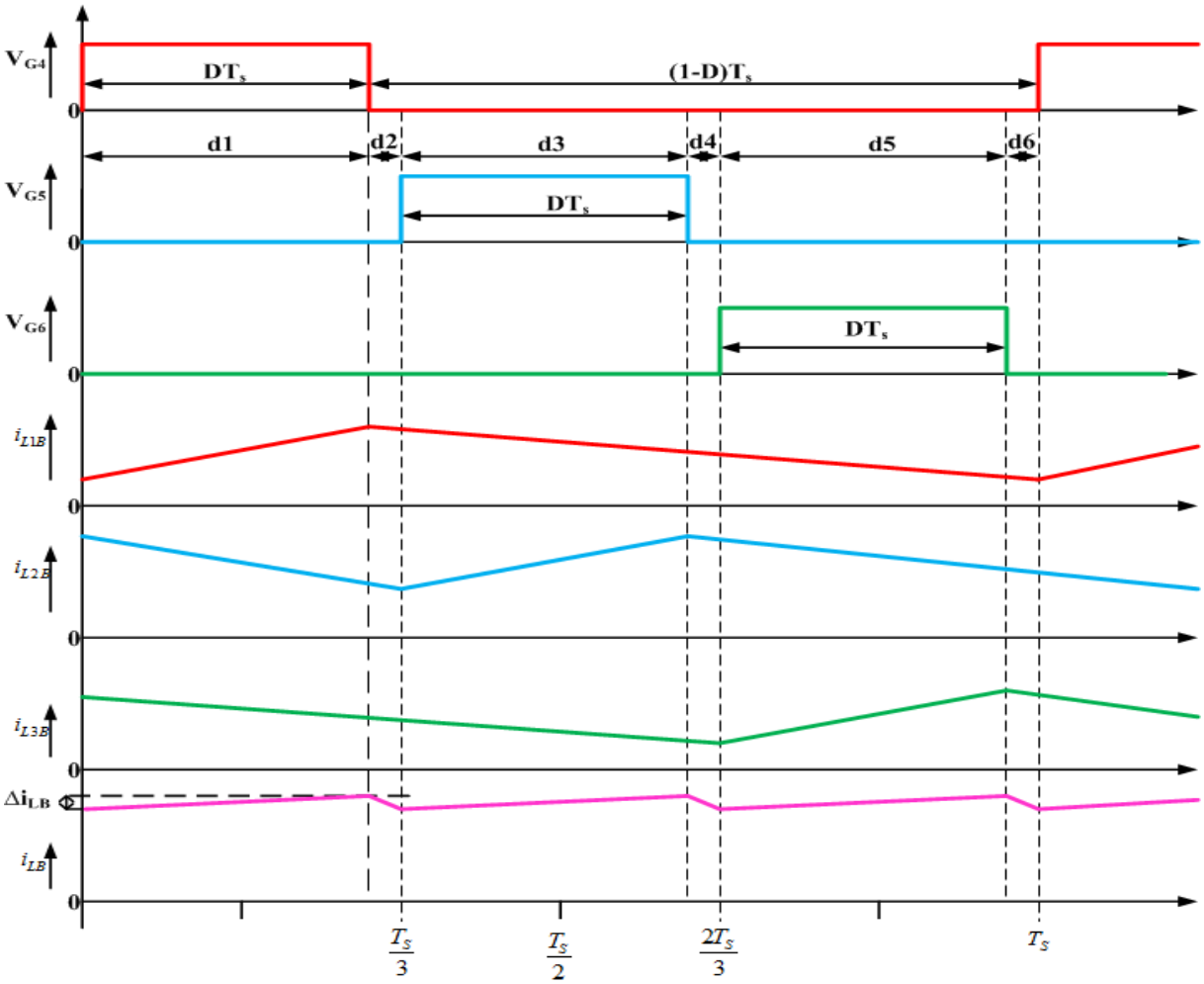


Figure 3.3 Three-phase IBDDC in boost mode operates in CCM with duty ratio D=0.32.

The total current through an inductor i_{LB} will be sum of the slopes of i_{L1B}, i_{L2B} and i_{L3B} and an average current through an inductor I_{LB} of three-phase IBDDC in boost mode is calculated by the following expression

$$I_{LB} = \frac{V_1 - V_\gamma(1-\mathrm{D})}{R_2(1-\mathrm{D})^2 + \frac{\mathrm{r} + \mathrm{DR}_{on} + R_f(1-\mathrm{D})}{3}} \qquad (3.1)$$

Average value of output voltage of three-phase IBDDC in boost mode is calculated by the following expression

$$V_2 = I_{LB} R_2 (1-\mathrm{D}) = \left[\frac{V_1 - V_\gamma (1-\mathrm{D})}{R_2 (1-\mathrm{D})^2 + \frac{\mathrm{r}_1 + \mathrm{DR}_{on} + R_f (1-\mathrm{D})}{3}} \right] R_2 (1-\mathrm{D}) \qquad (3.2)$$

Input ripple current of three-phase IBDDC in boost mode with duty ratio of $D = 0.32$ is calculated by the following relation

$$\Delta I_{LB} = \frac{V_1}{L_1} \left[\frac{1-3D}{1-D} \right] DT_S \qquad (3.3)$$

3.4 Steady State Analysis of Three Phase IBDDC in Buck Mode

The operation of the three-phase IBDDC in buck mode operates in CCM is explained with the non-ideal equivalent circuits, and the conduction of the switches with different states is as shown Figure 3.2 . The waveforms corresponding to three phase IBDDC in buck mode operates in CCM are as shown in Figure 3.5 for duty ratio D' of 68%.

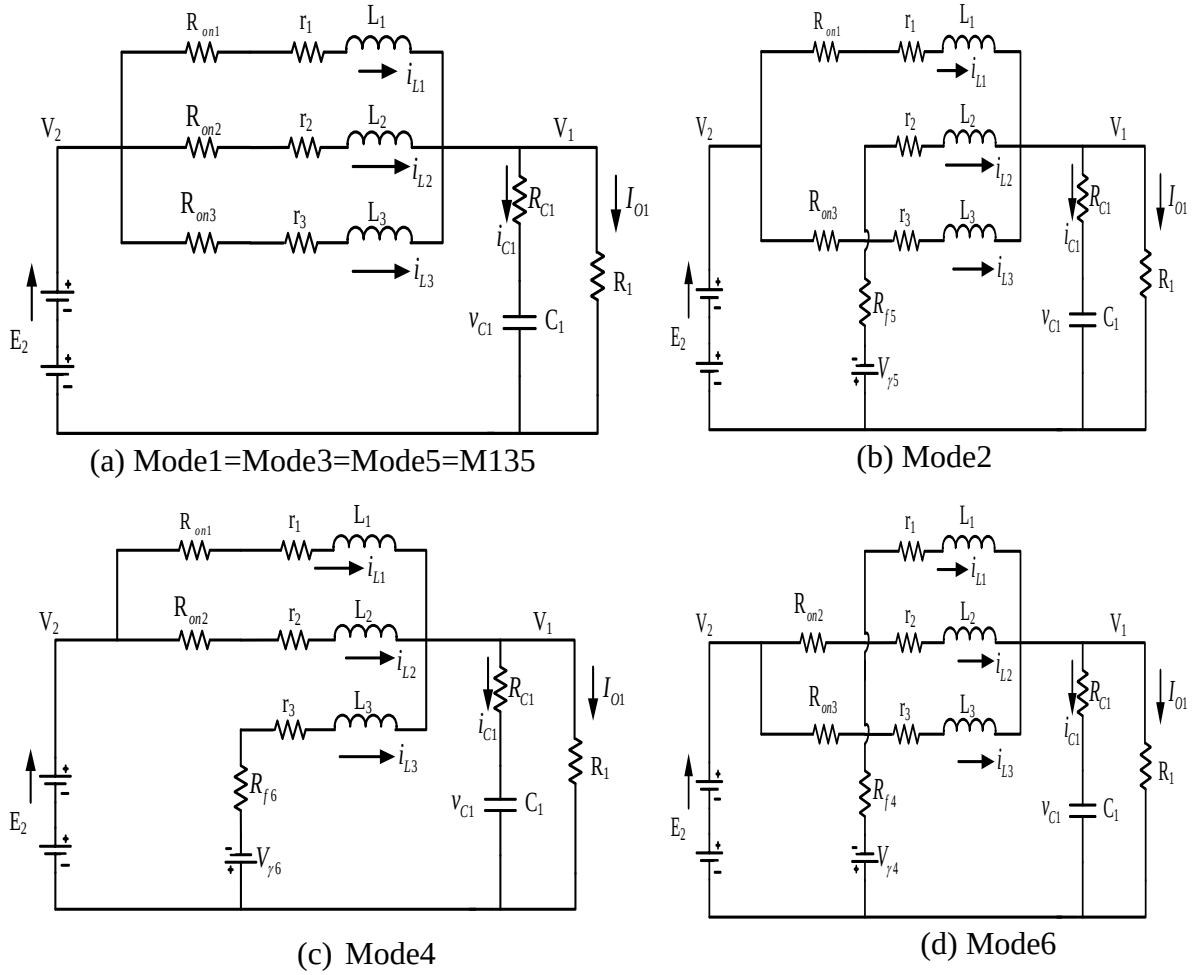


Figure 3.4 Equivalent circuits of three-phase IBDDC in buck mode with different states.

Three-phase IBDDC in buck mode operates in CCM, when the duty ratio D' lies between $\frac{2}{3}$ and 1 with $E_1 = 0, R_2 = 0$ and $i_{C2} = 0$. It has 6 modes of operation and each of the mode is explained as follows:

Mode1=Mode3=Mode5=M135: At t=0, i.e during $d_1' = d_3' = d_5' = D'T_s$, switches S_1, S_2 and S_3 conduct. i_{L1}, i_{L2} and i_{L2} increase linearly. The net i_L becomes sum of slopes of i_{L1}, i_{L2} and i_{L3}. In this mode, voltage source (E_2) supplies the power to the load (R_1). An equivalent circuit of mode1, mode3, and mode5 of three-phase IBDDC in buck stage is as shown in Figure 3.4(a).

Mode2: During $d_2' = (1-D')T_s$, switches S_1 and S_3 , diode D_5 conduct. i_{L1} and i_{L3} increases linearly and i_{L2} decreases linearly. The net i_L becomes sum of slopes of i_{L1}, i_{L2} and i_{L3}. An equivalent circuit of mode2 of three-phase IBDDC in buck stage is as shown in Figure 3.4(b).

Mode4 : During $d_4' = (1-D')T_s$, switches S_1 and S_2 , diode D_6 conduct. i_{L1} and i_{L2} increases linearly and i_{L3} decreases linearly. The net i_L becomes sum of slopes of i_{L1}, i_{L2} and i_{L3}. An equivalent circuit of mode4 of three-phase IBDDC in Buck stage is as shown in Figure 3.4(c).

Mode6 : During $d_6' = (1-D')T_s$, switches S_2 and S_3 , diode D_4 conduct. i_{L2} and i_{L3} increases linearly and i_{L1} decreases linearly. The net i_L becomes sum of slopes of i_{L1}, i_{L2} and i_{L3}. An equivalent circuit of mode6 of three-phase IBDDC in buck stage is as shown in Figure 3.4(d).

The switching sequence and current through an inductor is shifted by 120^0 phase shift angle. The total current through an inductor i_L will be the sum of the slope of i_{L1}, i_{L2} and i_{L3}. An average current through an inductor I_L of three-phase IBDDC in buck mode is calculated by the following expression

$$I_L = \frac{V_2 D' - V_\gamma (1-D')}{R_1 + \frac{R_{on} D' + r + R_f (1-D')}{3}} \tag{3.4}$$

Average value of output voltage of three-phase IBDDC in buck mode is calculated by following expression

$$V_1 = I_L R_1 = \left[\frac{V_2 D' - V_\gamma (1-D')}{R_1 + \frac{R_{on} D' + r + R_f (1-D')}{3}} \right] R_1 \tag{3.5}$$

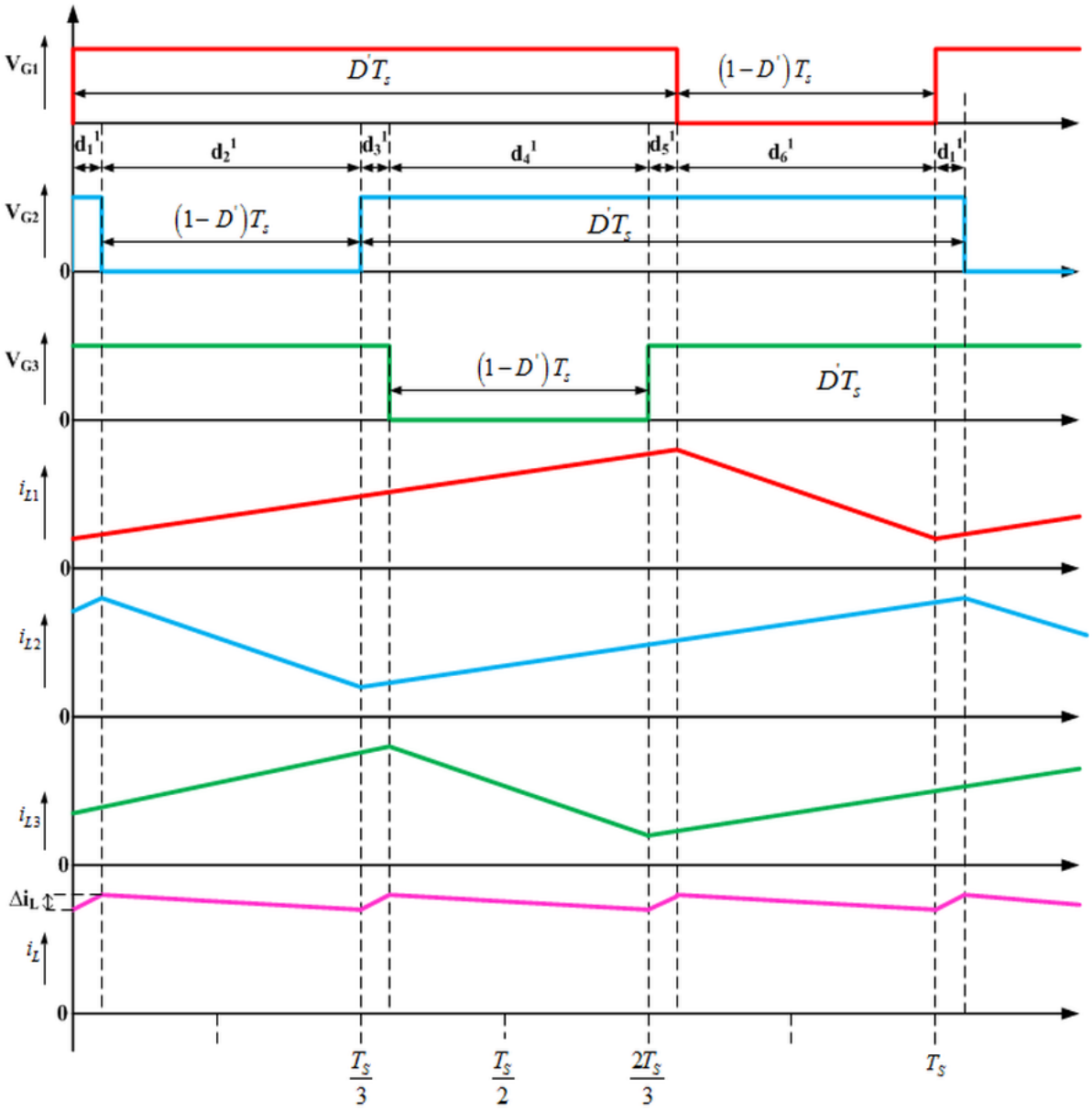


Figure 3.5 Three-phase IBDDC in buck mode operates in CCM with duty ratio $D' = 0.68$.

Input ripple current of three-phase IBDDC in buck mode with duty ratio of $D' = 0.68$ is calculated by the following relation

$$\Delta I_L = \frac{V_2(3-3D')}{L_1}\left(D' - \frac{2}{3}\right)T_s \qquad (3.6)$$

3.5 Design of Three-Phase IBDDC in CCM

Specification of three-phase IBDDC both in boost mode and buck mode operated with CCM are tabulated in Table 3.1.

Table 3.1 Specification of three-phase IBDDC in boost mode and buck mode

Parameters	**Boost mode**	**Buck mode**
Supply voltage	48 V ±10% (E_1)	70 V ±10% (E_2)
Output voltage	70 V (V_2)	48 V (V_1)
Duty ratio for nominal value	32% (D)	68% (D')
Load current	5 A (I_{o2})	6 A (I_{o1})
Operating frequency (f_s)	100 kHz	100 kHz

3.5.1 Design of Three-Phase IBDDC Inductor in Boost Mode

When the three-phase IBDDC in boost mode operates in CCM, inductor is designed with inductor ripple current for $0 < D < \frac{1}{3}$ is calculated by the following relation

$$L = D(1-3D)\frac{V_2 T_s}{\Delta I_{LB}} \tag{3.7}$$

By substituting the specification details of three-phase IBDDC in boost mode has been tabulated in Table 3.1 with (3.3) and (3.7), the value of an inductor is calculated as L=120 µH. EE ferrite core is selected with 24 turns of SWG14 gauge wire to carry full load current and its self-inductance value is $L_1 = L_2 = L_3 = L = 120\ \mu H$.

3.5.2 Design of Three-Phase IBDDC Output Capacitor in Boost Mode

Based on the RMS value of capacitor current of three-phase IBDDC in boost mode, the output capacitor C_2 can be designed for $0 < D < \frac{1}{3}$ is calculated by the following relation

$$C_2 = \frac{V_2 D}{R_2 f_s \Delta v_2} \tag{3.8}$$

The value of capacitor of three-phase IBDDC in boost mode is selected as $C_2 = 100\ \mu F$.

3.5.3 Design of Three-Phase IBDDC Output Capacitor in Buck Mode

Based on the RMS value of capacitor current of three-phase IBDDC in buck mode, the output capacitor C_1 can be designed for $\frac{2}{3} < D' < 1$ is calculated by the following relation

$$C_1 = \frac{\Delta i_L}{8 f_s \Delta v_1} \tag{3.9}$$

where $\Delta i_L = \dfrac{V_2(1-D')N\left(D'-\dfrac{m}{N}\right)\left(\dfrac{m+1}{N}-D'\right)}{Lf_sD'(1-D')}$, here $\mathrm{m}=\mathrm{floor}\left(\mathrm{ND}'\right)$ is an integer value, and N=number of phases.

The value of capacitor of three-phase IBDDC in buck mode is selected as $C_1 = 1\ \mu F$.

3.6 Dynamic Analysis of Three-Phase IBDDC

Dynamic behaviour of three-phase IBDDC can be examined with the help of finding analytical expression for derivative state variables (current through an inductor and voltage across capacitor) during ON and OFF duration in each mode of operation. The number of state variables in the converter in each mode is equal to the number of energy storage elements over the switching period. In order to design the proper controller for stable operation of three-phase IBDDC, small signal control to duty ratio relationship can be derived with the help of SSA method [17-19]. By taking into account parasitic resistances of filter components and power switches and also the cut in voltage of the power diode, small signal open loop control to output transfer function of three-phase IBDDC can be derived.

3.6.1 Three-Phase IBDDC in Boost Mode

In order to understand the characteristic behavior of three-phase IBDDC in boost mode operation, small signal equations of the converter can be obtained by applying Kirchhoff's voltage and current law. In boost mode, current through an inductors $\left(i_{L1B}, i_{L2B}, i_{L3B}\right)$ and voltage across C_2 $\left(v_{C2}\right)$ are treated as state variable $\left(x\right)$, its derivative parameter and output voltage equation can be obtained in terms of the converter system parameters by applying KVL and KCL for non-ideal equivalent circuits.

Small signal analysis of three-phase IBDDC in boost mode can be understood with the help of state space averaging technique for different states over the one switching period and is explained as follows:

During the interval of on state $d1 = DT_s$ of three-phase IBDDC in boost mode as shown in Figure 3.2(a), derivative of state variable $\left(\dot{x}\right)$ and output voltage equations can be obtained.

State variable $x = \begin{bmatrix} i_{L1B} \\ i_{L2B} \\ i_{L3B} \\ v_{C2} \end{bmatrix}$, $e_1 = \begin{bmatrix} V_1 \\ V_{\gamma 1} \\ V_{\gamma 2} \\ V_{\gamma 3} \end{bmatrix}$ and $\alpha = \dfrac{R_2 R_{C2}}{R_2 + R_{C2}}$

$$\frac{di_{L1B}}{dt} = -\frac{R_{on1} + r_1}{L_1} i_{L1B} + \frac{V_1}{L_1} \tag{3.10}$$

$$\frac{di_{L2B}}{dt} = -\frac{1}{L_2}\left(\mathrm{R}_{f2} + \mathrm{r}_2 + \frac{R_2 R_{C2}}{R_2 + R_{C2}}\right) i_{L2B} - \frac{1}{L_2}\left(\frac{R_2 R_{C2}}{R_2 + R_{C2}}\right) i_{L3B} - \frac{1}{L_2}\left(\frac{R_2}{R_2 + R_{C2}}\right) v_{C2} + \frac{V_1}{L_2} - \frac{V_{\gamma 2}}{L_2} \tag{3.11}$$

$$\frac{di_{L3B}}{dt} = -\frac{1}{L_3}\left(\frac{R_2 R_{C2}}{R_2 + R_{C2}}\right) i_{L2B} - \frac{1}{L_3}\left(\mathrm{R}_{f3} + \mathrm{r}_3 + \frac{R_2 R_{C2}}{R_2 + R_{C2}}\right) i_{L3B} - \frac{1}{L_3}\left(\frac{R_2}{R_2 + R_{C2}}\right) v_{C2} + \frac{V_1}{L_3} - \frac{V_{\gamma 3}}{L_3} \tag{3.12}$$

$$\frac{dv_{C2}}{dt} = \frac{1}{C_2}\left(\frac{R_2}{R_2 + R_{C2}}\right) i_{L2B} + \frac{1}{C_2}\left(\frac{R_2}{R_2 + R_{C2}}\right) i_{L3B} - \frac{1}{C_2}\left(\frac{1}{R_2 + R_{C2}}\right) v_{C2} \tag{3.13}$$

Assuming $r_1=r_2=r_3=r$, $R_{f1}=R_{f2}=R_{f3}=R_f$, and $L_1=L_2=L_3=L$, above equations can be represented by matrix form during $d1 = DT_s$,

$$\dot{x} = A_1 x + B_1 e_1 \tag{3.14}$$

here $A_1 = \begin{bmatrix} -\frac{1}{L}(R_{on} + r) & 0 & 0 & 0 \\ 0 & -\frac{1}{L}(R_f + r + \alpha) & -\frac{\alpha}{L} & -\frac{\alpha}{LR_{C2}} \\ 0 & -\frac{\alpha}{L} & -\frac{1}{L}(R_f + r + \alpha) & -\frac{\alpha}{LR_{C2}} \\ 0 & \frac{\alpha}{C_2 R_{C2}} & \frac{\alpha}{C_2 R_{C2}} & -\frac{\alpha}{C_2 R_2 R_{C2}} \end{bmatrix}$ is the system matrix,

and $B_1 = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 \\ \frac{1}{L} & 0 & -\frac{1}{L} & 0 \\ \frac{1}{L} & 0 & 0 & -\frac{1}{L} \\ 0 & 0 & 0 & 0 \end{bmatrix}$ is the input matrix.

Output voltage during $d1 = DT_s$ of three-phase IBDDC in boost mode is given by the following relation

$$v_2 = C_1^T x \tag{3.15}$$

here $C_1^T = \begin{bmatrix} 0 & \alpha & \alpha & \frac{\alpha}{R_{C2}} \end{bmatrix}$ is the output matrix.

Similarly during the interval $d2 = d4 = d6 = \left(\frac{2}{3} - D\right) T_s$ as shown in Figure 3.2(b), derivative of state variable and output voltage equations are obtained by following relations

$$\dot{x} = A_2 x + B_2 e_1 = A_4 x + B_4 e_1 = A_6 x + B_6 e_1 \tag{3.16}$$

where $A_2 = A_2 = A_6 = \begin{bmatrix} -\frac{1}{L}\left(R_f + r + \alpha\right) & -\frac{\alpha}{L} & -\frac{\alpha}{L} & -\frac{\alpha}{LR_{C2}} \\ -\frac{\alpha}{L} & -\frac{1}{L}\left(R_f + r + \alpha\right) & -\frac{\alpha}{L} & -\frac{\alpha}{LR_{C2}} \\ -\frac{\alpha}{L} & -\frac{\alpha}{L} & -\frac{1}{L}\left(R_f + r + \alpha\right) & -\frac{\alpha}{LR_{C2}} \\ -\frac{\alpha}{LR_{C2}} & \frac{\alpha}{C_2 R_{C2}} & \frac{\alpha}{C_2 R_{C2}} & -\frac{\alpha}{C_2 R_2 R_{C2}} \end{bmatrix}$

and $B_2 = B_4 = B_6 = \begin{bmatrix} \frac{1}{L} & -\frac{1}{L} & 0 & 0 \\ \frac{1}{L} & 0 & -\frac{1}{L} & 0 \\ \frac{1}{L} & 0 & 0 & -\frac{1}{L} \\ 0 & 0 & 0 & 0 \end{bmatrix}$.

Output voltage during $d2 = d4 = d6 = \left(\frac{2}{3} - D\right)T_s$ of three-phase IBDDC in boost mode is given by the following relation

$$v_2 = C_2^T x = C_4^T x = C_6^T x \tag{3.17}$$

where $C_2^T = C_4^T = C_6^T = \begin{bmatrix} \alpha & \alpha & \alpha & \frac{\alpha}{R_{C2}} \end{bmatrix}$.

Similarly during the interval $d3 = DT_s$ as shown in Figure 3.2(c), derivative of state variable and output voltage equations are obtained by following relations

$$\dot{x} = A_3 x + B_3 e_1 \tag{3.18}$$

Here $A_3 = \begin{bmatrix} -\frac{1}{L}\left(R_f + r + \alpha\right) & 0 & -\frac{\alpha}{L} & -\frac{\alpha}{LR_{C2}} \\ 0 & -\frac{1}{L}\left(R_{on} + r\right) & 0 & 0 \\ -\frac{\alpha}{L} & 0 & -\frac{1}{L}\left(R_f + r + \alpha\right) & -\frac{\alpha}{LR_{C2}} \\ -\frac{\alpha}{L} & 0 & \frac{\alpha}{C_2 R_{C2}} & -\frac{\alpha}{C_2 R_2 R_{C2}} \end{bmatrix}$ and $B_3 = \begin{bmatrix} \frac{1}{L} & -\frac{1}{L} & 0 & 0 \\ \frac{1}{L} & 0 & 0 & 0 \\ \frac{1}{L} & 0 & 0 & -\frac{1}{L} \\ 0 & 0 & 0 & 0 \end{bmatrix}$

Output voltage during $d3 = DT_s$ of three-phase IBDDC in boost mode is given by the following relation

$$v_2 = C_3^T x \tag{3.19}$$

where $C_3^T = \begin{bmatrix} \alpha & 0 & \alpha & \frac{\alpha}{R_{C2}} \end{bmatrix}$.

Similarly during the interval $d5 = DT_s$ as shown in Figure 3.2(d), derivative of state variable and output voltage equations are obtained by following relations

$$\dot{x} = A_5 x + B_5 e_1 \tag{3.20}$$

here $A_5 = \begin{bmatrix} -\frac{1}{L}\left(R_f + r + \alpha\right) & -\frac{\alpha}{L} & 0 & -\frac{\alpha}{LR_{C2}} \\ -\frac{\alpha}{L} & -\frac{1}{L}\left(R_f + r + \alpha\right) & 0 & -\frac{\alpha}{LR_{C2}} \\ 0 & 0 & -\frac{1}{L}\left(R_{on} + r\right) & 0 \\ \frac{\alpha}{C_2 R_{C2}} & \frac{\alpha}{C_2 R_{C2}} & 0 & -\frac{\alpha}{C_2 R_2 R_{C2}} \end{bmatrix}$ and $B_5 = \begin{bmatrix} \frac{1}{L} & -\frac{1}{L} & 0 & 0 \\ \frac{1}{L} & 0 & -\frac{1}{L} & 0 \\ \frac{1}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$

Output voltage during $d5 = DT_s$ of three-phase IBDDC in boost mode is given by the following relation

$$v_2 = C_5^T x \tag{3.21}$$

here $C_5^T = \begin{bmatrix} \alpha & \alpha & 0 & \frac{\alpha_2}{R_{C2}} \end{bmatrix}$.

Small signal control to duty ratio relationship of three- phase IBDDC in boost mode using state space averaging (SSA) method [17-19] can be obtained by the following definition and its details are provided in Appendix D.

$$\left.\frac{\hat{v_2}(s)}{\hat{d}(s)}\right|_{\hat{v_1}=0} = C_7^T \left[sI - A_7\right]^{-1} f_1 + q_1 X_1 \tag{3.22}$$

where $C_7^T = (C_1^T + C_3^T + C_5^T)D + C_2^T(1-3D)$, $A_7 = (A_1 + A_3 + A_5)D + A_2(1-3D)$,

$f_1 = \left[A_1 + A_3 + A_5 - 3A_2\right]X_1 + \left[B_1 + B_3 + B_5 - 3B_2\right]V_1$, $q_1 = C_1^T + C_3^T + C_5^T - 3C_2^T$, $X_1 = -A_7^{-1}B_7 V_1$

and $B_7 = (B_1 + B_3 + B_5)D + B_2(1-3D)$

The solution for the equation (3.22) is given by the following

$$\left.\frac{\hat{v_2}(s)}{\hat{d}(s)}\right|_{\hat{v_1}=0} = \frac{G\left[s + \frac{1}{C_2 R_{c2}}\right]\left[s - \frac{1}{L}\left(\frac{3R_2\alpha}{R_{c2}}(1-D)^2 + 2\alpha - r - R_{on}\right)\right]}{s^2 + s\left(\frac{R_f}{L}(1-D) + \frac{1}{L}(r + R_{on}) + \frac{\alpha}{L}(3-5D) + \frac{\alpha}{R_2 C_2 R_{c2}}\right) + K} \tag{3.23}$$

where $G = \frac{-3\alpha R_{c2}\left(V_1 - V_\gamma + DV_\gamma\right)}{3R_2\alpha\left(1-2D+3D^2\right) + R_{c2}\left(r + R_f(1-D) + \alpha(3-5D) + DR_{on}\right)}$ and

$$K=\frac{\alpha}{LC_2R_{c2}^2}\left(3\alpha(1-D)^2+\frac{1}{R_2}\left(\alpha(3-5D)+r+R_f(1-D)+DR_{on}\right)\right).$$

In the transfer function, $\hat{v}_2(s)$, $\hat{d}(s)$, and $\hat{v}_1$ are the small signal variations of the output voltage, duty cycle, and input voltage of three-phase IBDDC in boost mode respectively.

By substituting the design parameters in the system matrices, input matrices and output matrices and then in small signal duty ratio to output voltage transfer function relation (3.23) results with the three-phase IBDDC boost mode system transfer function (3.24), the corresponding frequency response (bode plot) and unit step plot are shown in Figure 3.6 and Figure 3.7 respectively.

$$G_{Boost3}(s)=\frac{-2.311s^2+300\times10^3 s+1.16\times10^{10}}{s^2+4634s+112\times10^6} \tag{3.24}$$

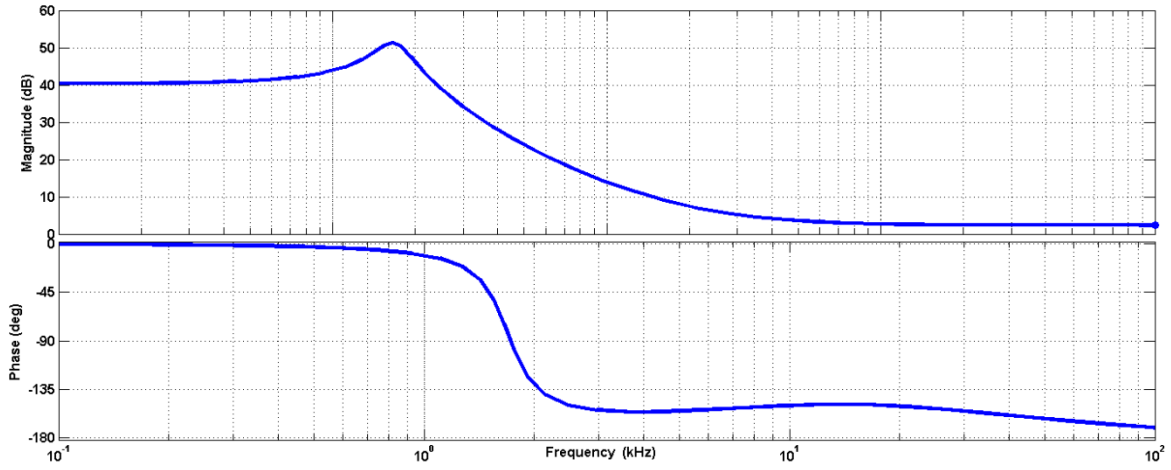


Figure 3.6 Open loop bode plot of three-phase IBDDC in boost mode

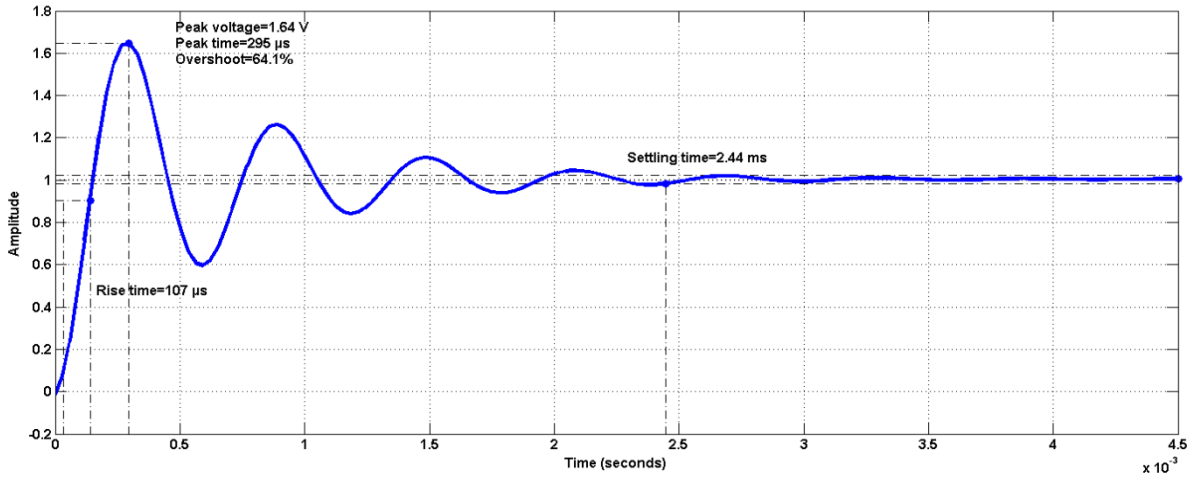


Figure 3.7 Open loop unit step response plot of three-phase IBDDC in boost mode

From Figure 3.7, three-phase IBDDC in boost mode results with the rise time of 107 µs, peak over shoot of 1.64 V with overshoot of 64.6% at 295 µs, settling time at 2.44 ms and

steady state value of 1 V. The above system is an under damped and non-minimum phase system.

3.6.2 Three-Phase IBDDC in Buck Mode

In order to understand the characteristic behavior of three-phase IBDDC in buck mode operation, small signal equations of the converter can be obtained by applying Kirchhoff's voltage and current law. In buck mode, current through an inductors (i_{L1}, i_{L2}, i_{L3}) and voltage across C_1 (v_{C1}) are treated as state variable (x_1), its derivative parameter and output voltage equation can be obtained in terms of the converter system parameters by applying KVL and KCL for non-ideal equivalent circuits.

Small signal analysis of three-phase IBDDC in buck mode can be understood with the help of state space averaging technique for different states over the one switching period and is explained as follows:

During the interval of on state $d_1^{'} = d_3^{'} = d_5^{'} = \left(D' - \frac{2}{3} \right) \mathrm{T_s}$ of three-phase IBDDC in buck mode as shown in Figure 3.4(a), derivative of state variable $(\dot{x}_1)$ and output voltage equations can be obtained.

State variable $x_1 = \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ v_{C1} \end{bmatrix}$, $e_2 = \begin{bmatrix} V_2 \\ V_{\gamma 4} \\ V_{\gamma 5} \\ V_{\gamma 6} \end{bmatrix}$

$$\frac{di_{L1}}{dt} = -\frac{1}{L_1}\left(\mathrm{R}_{on1} + \mathrm{r}_1 + \frac{R_1 R_{C1}}{R_1 + R_{C1}} \right) i_{L1} - \frac{1}{L_1}\left(\frac{R_1 R_{C1}}{R_1 + R_{C1}} \right) i_{L2} - \frac{1}{L_1}\left(\frac{R_1 R_{C1}}{R_1 + R_{C1}} \right) i_{L3} - \frac{1}{L_1}\left(\frac{R_1}{R_1 + R_{C1}} \right) v_{C1} + \frac{V_2}{L_1} \quad (3.25)$$

$$\frac{di_{L2}}{dt} = -\frac{1}{L_2}\left(\frac{R_1 R_{C1}}{R_1 + R_{C1}} \right) i_{L1} - \frac{1}{L_2}\left(\mathrm{R}_{on2} + \mathrm{r}_2 + \frac{R_1 R_{C1}}{R_1 + R_{C1}} \right) i_{L2} - \frac{1}{L_2}\left(\frac{R_1 R_{C1}}{R_1 + R_{C1}} \right) i_{L3} - \frac{1}{L_2}\left(\frac{R_1}{R_1 + R_{C1}} \right) v_{C1} + \frac{V_2}{L_2} \quad (3.26)$$

$$\frac{di_{L3}}{dt} = -\frac{1}{L_3}\left(\frac{R_1 R_{C1}}{R_1 + R_{C1}} \right) i_{L1} - \frac{1}{L_3}\left(\frac{R_1 R_{C1}}{R_1 + R_{C1}} \right) i_{L2} - \frac{1}{L_3}\left(\mathrm{R}_{on3} + \mathrm{r}_3 + \frac{R_1 R_{C1}}{R_1 + R_{C1}} \right) i_{L3} - \frac{1}{L_3}\left(\frac{R_1}{R_1 + R_{C1}} \right) v_{C1} + \frac{V_2}{L_3} \quad (3.27)$$

$$\frac{dv_{C_1}}{dt} = \frac{R_1}{C_1(R_1 + R_{C1})} i_{L1} + \frac{R_1}{C_1(R_1 + R_{C1})} i_{L2} + \frac{R_1}{C_1(R_1 + R_{C1})} i_{L3} - \frac{1}{C_1(R_1 + R_{C1})} v_{C1} \quad (3.28)$$

Above equations can be represented by matrix form during $d_1^{'} = d_3^{'} = d_5^{'} = \left(D^{'} - \frac{2}{3} \right) \mathrm{T_s}$,

$$\dot{x}_1 = A_{a1} x_1 + B_{b1} e_2 = A_{a3} x_1 + B_{b3} e_2 = A_{a5} x_1 + B_{b5} e_2 \quad (3.29)$$

where $A_{u1} = A_{u3} = A_{u5} = \begin{bmatrix} -\frac{1}{L_1}\left(\mathrm{R}_{on}+\mathrm{r}+\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1}{R_1+R_{C1}}\right) \\ -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\mathrm{R}_{on}+\mathrm{r}+\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1}{R_1+R_{C1}}\right) \\ -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\mathrm{R}_{on}+\mathrm{r}+\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1}{R_1+R_{C1}}\right) \\ \frac{R_1}{C_1(R_1+R_{C1})} & \frac{R_1}{C_1(R_1+R_{C1})} & \frac{R_1}{C_1(R_1+R_{C1})} & -\frac{1}{C_1(R_1+R_{C1})} \end{bmatrix}$ is system matrix

and $B_{b1} = B_{b3} = B_{b5} = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 \\ \frac{1}{L} & 0 & 0 & 0 \\ \frac{1}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$ is the input matrix.

Output voltage during $d_1^{'} = d_3^{'} = d_5^{'} = \left(D' - \frac{2}{3}\right)\mathrm{T_s}$ of three-phase IBDDC in buck mode is given by the following relation

$$v_1 = C_{c1}^T x_1 \tag{3.30}$$

where $C_{c1}^T = C_{c3}^T = C_{c5}^T = \begin{bmatrix} \frac{R_1R_{C1}}{R_1+R_{C1}} & \frac{R_1R_{C1}}{R_1+R_{C1}} & \frac{R_1R_{C1}}{R_1+R_{C1}} & \frac{R_1}{R_1+R_{C1}} \end{bmatrix}$ is the output matrix.

Similarly during the interval of on state $d_2^{'} = (1-D')\mathrm{T_s}$ of three-phase IBDDC in buck mode as shown in Figure 3.4(b), derivative of state variable and output voltage equations can be obtained by the following equations

$$\dot{x}_1 = A_{a2}x_1 + B_{b2}e_2 \tag{3.31}$$

where $A_{a2} = \begin{bmatrix} -\frac{1}{L}\left(\mathrm{R}_{on}+\mathrm{r}+\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1}{R_1+R_{C1}}\right) \\ -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\mathrm{R}_{f}+\mathrm{r}+\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1}{R_1+R_{C1}}\right) \\ -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\mathrm{R}_{on}+\mathrm{r}+\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1}{R_1+R_{C1}}\right) \\ \frac{R_1}{C_1(R_1+R_{C1})} & \frac{R_1}{C_1(R_1+R_{C1})} & \frac{R_1}{C_1(R_1+R_{C1})} & -\frac{1}{C_1(R_1+R_{C1})} \end{bmatrix}$

and $B_{b2}=\begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L} & 0 \\ \frac{1}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$

Output voltage during $d_2^{'}=(1-D')\mathrm{T_s}$ of three-phase IBDDC in buck mode is given by the following relation

$$v_1 = C_{c2}^T x_1 \tag{3.32}$$

here $C_{c2}^T=\begin{bmatrix} \frac{R_1R_{C1}}{R_1+R_{C1}} & \frac{R_1R_{C1}}{R_1+R_{C1}} & \frac{R_1R_{C1}}{R_1+R_{C1}} & \frac{R_1}{R_1+R_{C1}} \end{bmatrix}$

Similarly during the interval of on state $d_4^{'}=(1-D')\mathrm{T_s}$ of three-phase IBDDC in buck mode as shown in Figure 3.4(c), derivative of state variable and output voltage equations can be obtained by the following equations

$$\dot{x}_1 = A_{a4}x_1 + B_{b4}e_2 \tag{3.33}$$

where $A_{a4}=\begin{bmatrix} -\frac{1}{L}\left(\mathrm{R}_{on}+\mathrm{r}+\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1}{R_1+R_{C1}}\right) \\ -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\mathrm{R}_{on}+\mathrm{r}+\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1}{R_1+R_{C1}}\right) \\ -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\mathrm{R}_{f}+\mathrm{r}+\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1}{R_1+R_{C1}}\right) \\ \frac{R_1}{C_1(R_1+R_{C1})} & \frac{R_1}{C_1(R_1+R_{C1})} & \frac{R_1}{C_1(R_1+R_{C1})} & -\frac{1}{C_1(R_1+R_{C1})} \end{bmatrix}$ and $B_{b4}=\begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 \\ \frac{1}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L} \\ 0 & 0 & 0 & 0 \end{bmatrix}$

Output voltage during $d_2^{'}=(1-D')\mathrm{T_s}$ of three-phase IBDDC in buck mode is given by the following relation

$$v_1 = C_{c4}^T x_1 \tag{3.34}$$

where $C_{c4}^T=\begin{bmatrix} \frac{R_1R_{C1}}{R_1+R_{C1}} & \frac{R_1R_{C1}}{R_1+R_{C1}} & \frac{R_1R_{C1}}{R_1+R_{C1}} & \frac{R_1}{R_1+R_{C1}} \end{bmatrix}$

Similarly during the interval of on state $d_6^{'}=(1-D')\mathrm{T_s}$ of three-phase IBDDC in buck mode as shown in Figure 3.4(d), derivative of state variable and output voltage equations can be obtained by the following equations

$$\dot{x}_1 = A_{a6}x_1 + B_{b6}e_2 \tag{3.35}$$

where $A_{a6}=\begin{bmatrix} -\frac{1}{L}\left(R_f+r+\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1}{R_1+R_{C1}}\right) \\ -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(R_{on}+r+\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1}{R_1+R_{C1}}\right) \\ -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(R_{on}+r+\frac{R_1R_{C1}}{R_1+R_{C1}}\right) & -\frac{1}{L}\left(\frac{R_1}{R_1+R_{C1}}\right) \\ \frac{R_1}{C_1(R_1+R_{C1})} & \frac{R_1}{C_1(R_1+R_{C1})} & \frac{R_1}{C_1(R_1+R_{C1})} & -\frac{1}{C_1(R_1+R_{C1})} \end{bmatrix}$ and $B_{b6}=\begin{bmatrix} 0 & -\frac{1}{L} & 0 & 0 \\ \frac{1}{L} & 0 & 0 & 0 \\ \frac{1}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$

Output voltage during $d_6^{'}=(1-D')\mathrm{T_s}$ of three-phase IBDDC in buck mode is given by the following relation

$$v_1=C_{c6}^{T}x_1 \tag{3.36}$$

where $C_{c6}^{T}=\begin{bmatrix} \frac{R_1R_{C1}}{R_1+R_{C1}} & \frac{R_1R_{C1}}{R_1+R_{C1}} & \frac{R_1R_{C1}}{R_1+R_{C1}} & \frac{R_1}{R_1+R_{C1}} \end{bmatrix}$

Small signal control to duty ratio relationship of three- phase IBDDC in buck mode using SSA method can be obtained by the following definition

$$\left.\frac{\hat{v}_1(s)}{\hat{d}^{'}(s)}\right|_{\hat{v}_2=0}=C_{c7}^{T}\left[sI-A_{a7}\right]^{-1}f_2 \tag{3.37}$$

where $C_{c1}^{T}=C_{c2}^{T}=C_{c3}^{T}=C_{c4}^{T}=C_{c5}^{T}=C_{c6}^{T}=C_{c7}^{T}$, $A_{a7}=A_{a1}(3D'-2)+(A_{a2}+A_{a4}+A_{a6})(1-D')$,

$f_2=\left[3A_{a1}+A_{a2}-A_{a4}-A_{a6}\right]X_2+\left[3B_{b1}+B_{b2}-B_{b4}-B_{b6}\right]V_2$, $X_2=-A_{a7}^{-1}B_{b7}V_2$

and $B_{b7}=B_{b1}(3D'-2)+(B_{b2}+B_{b4}+B_{b6})(1-D')$.

The solution for the equation (3.37) is given by the following

$$\left.\frac{\hat{v}_1(s)}{\hat{d}^{'}(s)}\right|_{\hat{v}_2=0}=\frac{Qs+Z}{LC_1\left(R_1+R_{c1}\right)\left(3R_1+r+R_f\left(1-D'\right)+D'R_{on}\right)\left[s^2+sP+\frac{3R_1+r+R_f\left(1-D'\right)+D'R_{on}}{LC_1\left(R_1+R_{c1}\right)}\right]} \tag{3.38}$$

where $Q=R_1C_1R_{c1}\left[3R_1\left(V_1\left(7+6D^{'}\right)+6V_\gamma\left(1+D^{'}\right)\right)+V_1\left(r+R_f\right)\left(7-6D^{'}\right)+V_\gamma\left(1-D^{'}\right)\left(6r-R_f\right)+7V_\gamma R_{on}\left(1+D^{'}\right)\right]$

$Z=R_1V_1\left[\left(3R_1+r+R_f\right)\left(7-6D^{'}\right)\right]+R_1V_\gamma\left(1-D^{'}\right)\left(18R_1+6r+7R_{on}-R_f\right)$ and

$$P=\frac{R_1\left(r+R_{c1}+R_f\right)+R_{c1}\left(r+R_f\right)+D^{'}\left(R_1\left(R_{on}-R_f\right)+R_{c1}\left(R_f+R_{on}\right)\right)}{LC_1\left(R_1+R_{c1}\right)}$$

By substituting the design parameters in the system matrices, input matrices and output matrices and then in small signal duty ratio to output voltage transfer function relation (3.38)

results in three-phase IBDDC buck mode system transfer function (3.39), the corresponding frequency response (bode plot) and unit step response plot are shown in Figure 3.8 and Figure 3.9 respectively.

$$G_{Buck3}(s) = \frac{5129.74\times10^{3}s + 1080\times10^{9}}{s^{2} + 153.37\times10^{3}s + 15.72\times10^{9}} \tag{3.39}$$

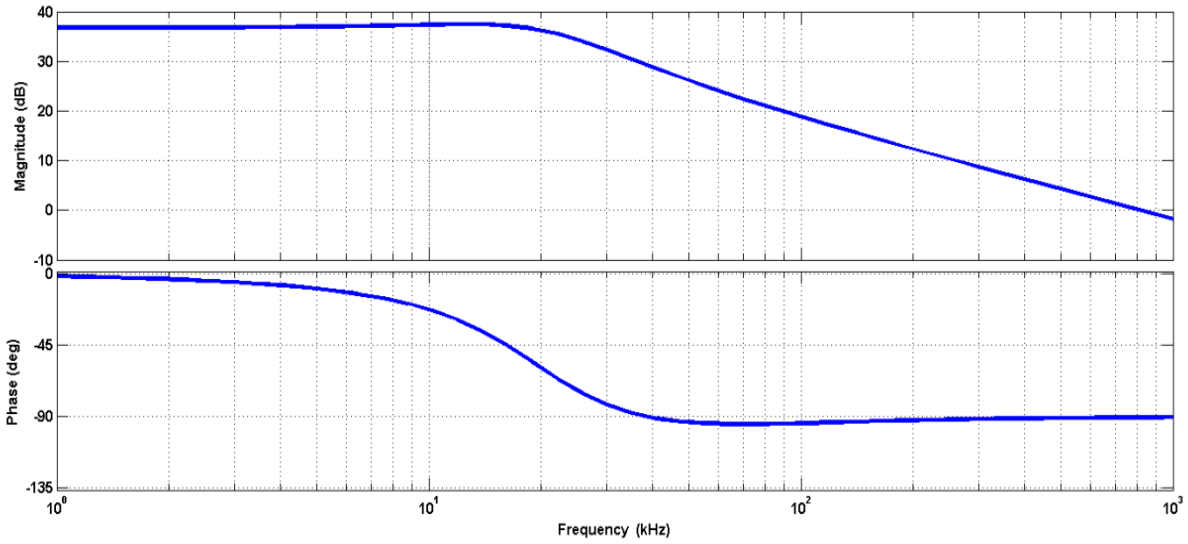


Figure 3.8 Open loop bode plot of three-phase IBDDC in buck mode

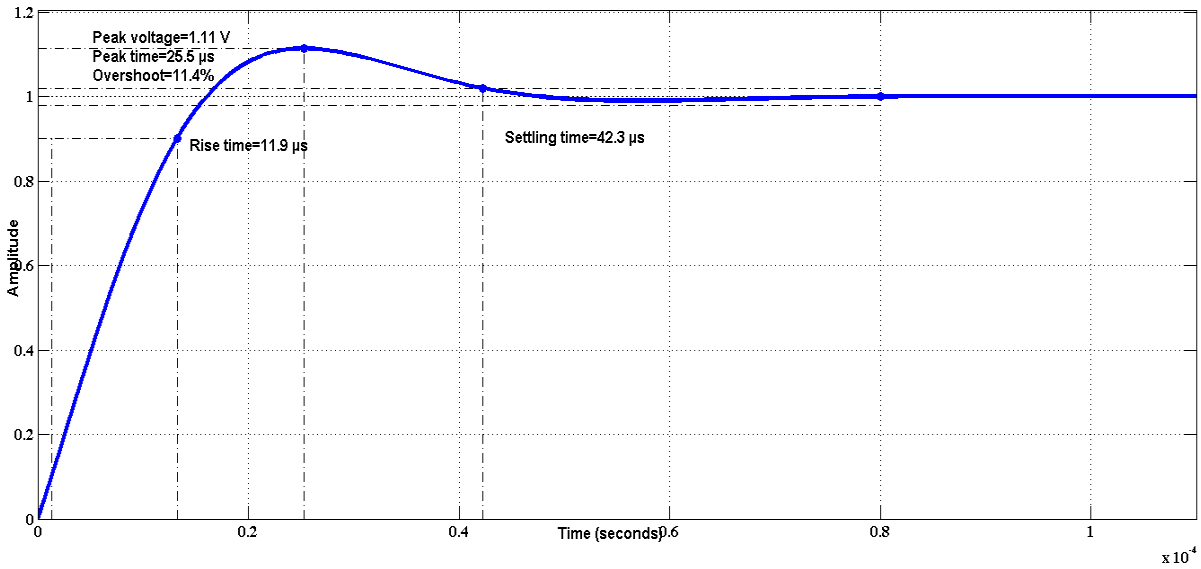


Figure 3.9 Open loop unit step response plot of three-phase IBDDC in buck mode.

From Figure 3.9, three-phase IBDDC in buck mode results with the rise time of 11.9 µs, peak over shoot of 1.11 V with overshoot of 11.4% at 25.3 µs, settling time at 42.3 µs and steady state value of 1 V. The above system is a stable system.

3.7 Design of Compensator/ Controller for Three-Phase IBDDC

3.7.1 Block Diagram of DSP Based Digital Control of Three-Phase IBDDC System

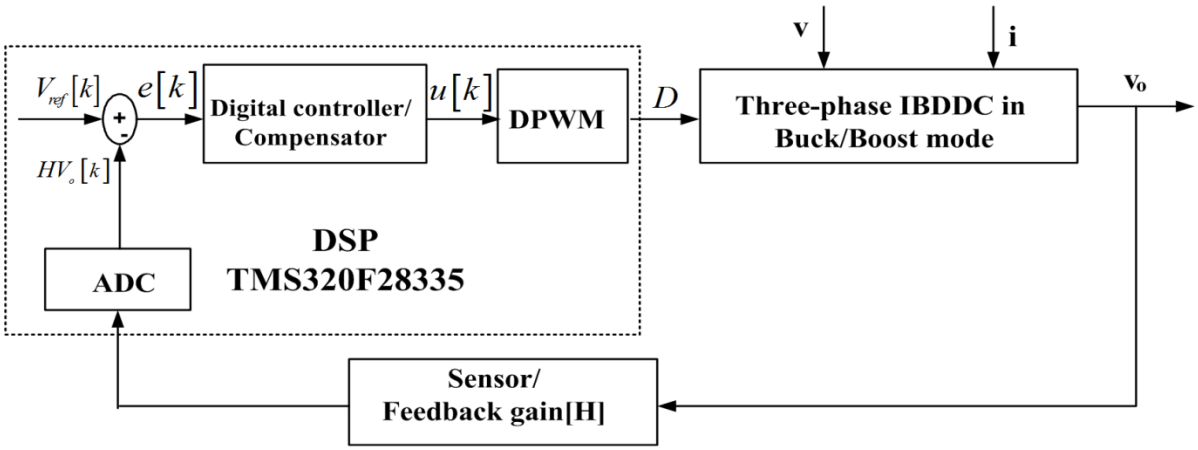


Figure 3.10 Block diagram of DSP based digital control of three-phase IBDDC system.

Indirect design procedure for design of digital controller has been preferred to implement the same on DSP ezdsp TMS320F28335 floating point processor.

Type III controller [20, 97] is also called as third order integral lead controller. It has a pole at origin and has two pole-zero pairs. This controller is designed to provide high gain at low frequency and low gain at high frequency, to achieve the reduced dc error, closed loop output impedance and to maintain sufficient degree of relative stability. Phase lag introduced from the actual system can be reduced to desired phase boost over the bandwidth by the type III compensator and leads to faster step response. Typical range of phase margin is between 45^0 and 60^0 and the gain margin is between 6 dB and 12 dB. Lower value of Phase margin gives the fastest response and shorter settling time, and more ringing with maximum overshoot in transient response. By suitably selecting phase margin and phase boost, type III compensator elements can be determined.

3.7.2 Design of Type III Error Amplifier for Three-Phase IBDDC in Boost Mode

In order to understand the system behaviour of the three-phase IBDDC in boost mode against line voltage variations and load transients, the open loop bode plot of small signal transfer function control to output voltage of the three-phase IBDDC in boost mode is plotted for different input voltage ranges 35 V, 42 V, 48 V, 55 V and 60 V, and open loop unit step response plot for the same are shown in Figure 3.11 and Figure 3.12 respectively. Similarly the open loop bode plot of small signal transfer function control to output voltage of the three-phase IBDDC in boost mode is also plotted for different load current of 1 A, 2 A, 3 A, 4 A, and 5 A, and open loop unit step response plot for the same are shown in Figure 3.13 and Figure 3.14 respectively.

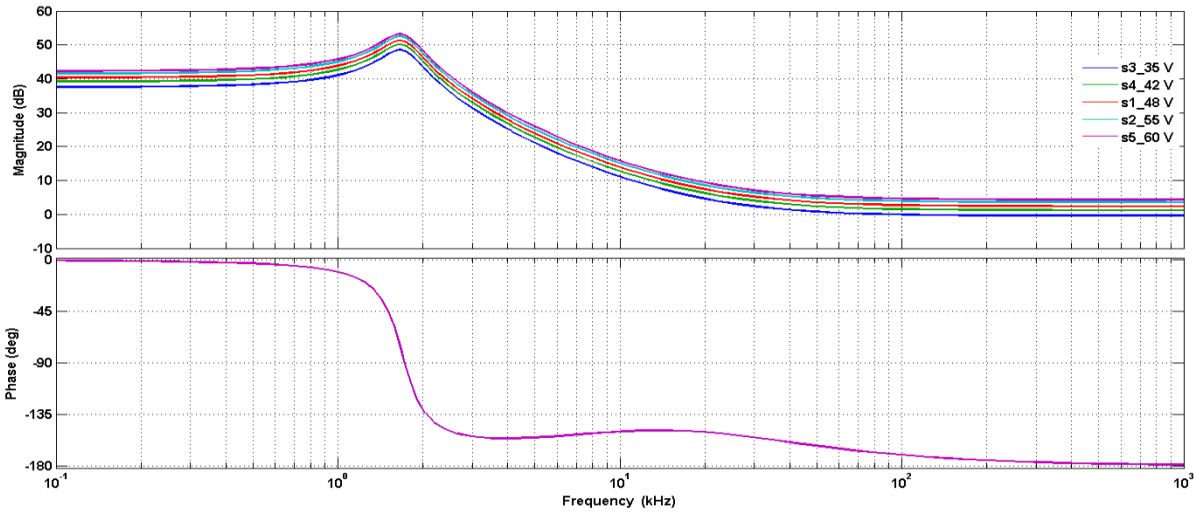


Figure 3.11 Open loop bode for various input voltages of three-phase IBDDC in boost mode

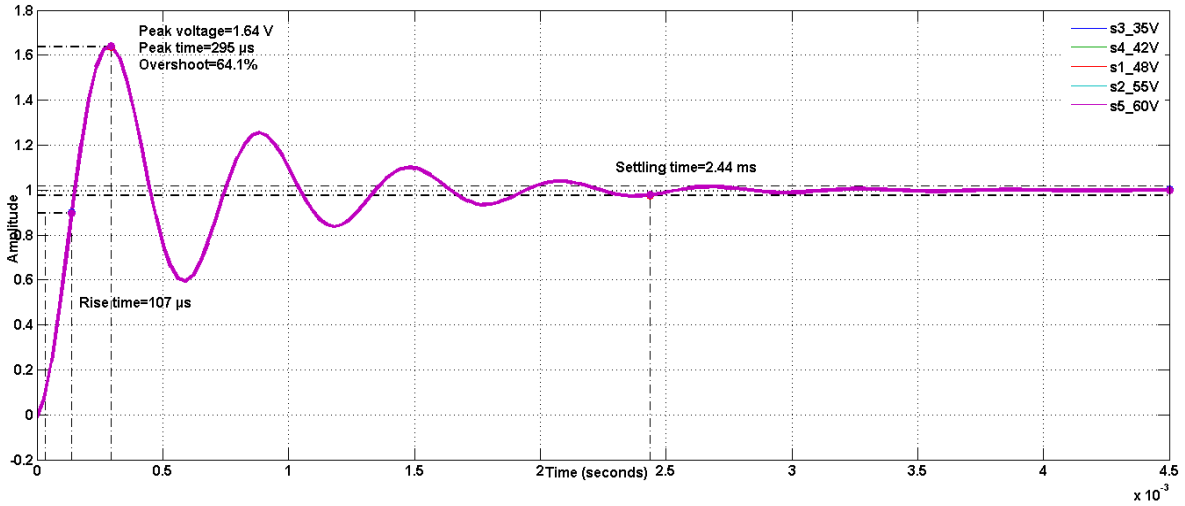


Figure 3.12 Open loop unit step plot of three-phase IBDDC in boost mode for different values of input voltage.

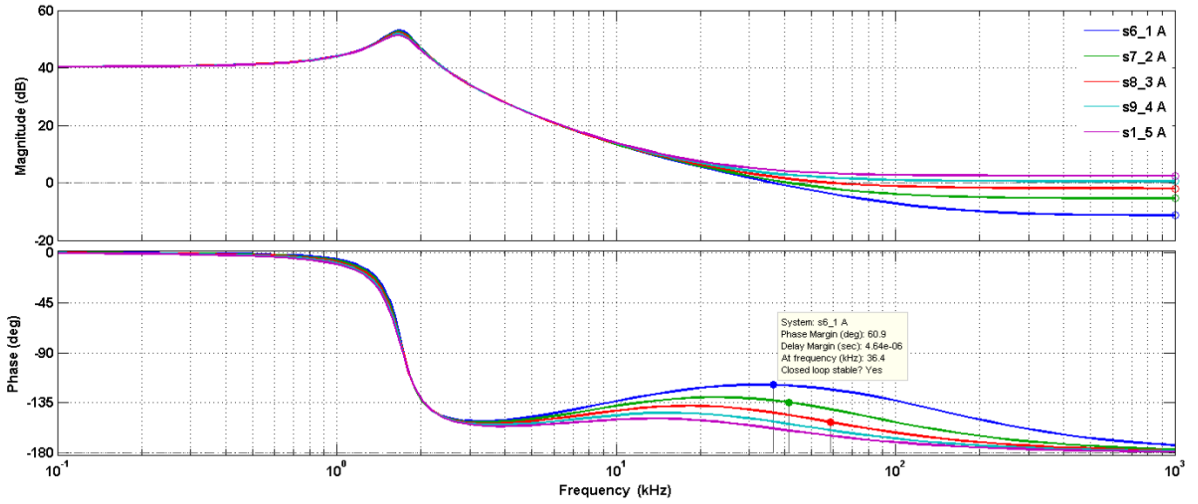


Figure 3.13 Open loop bode for different load current of three-phase IBDDC in boost mode.

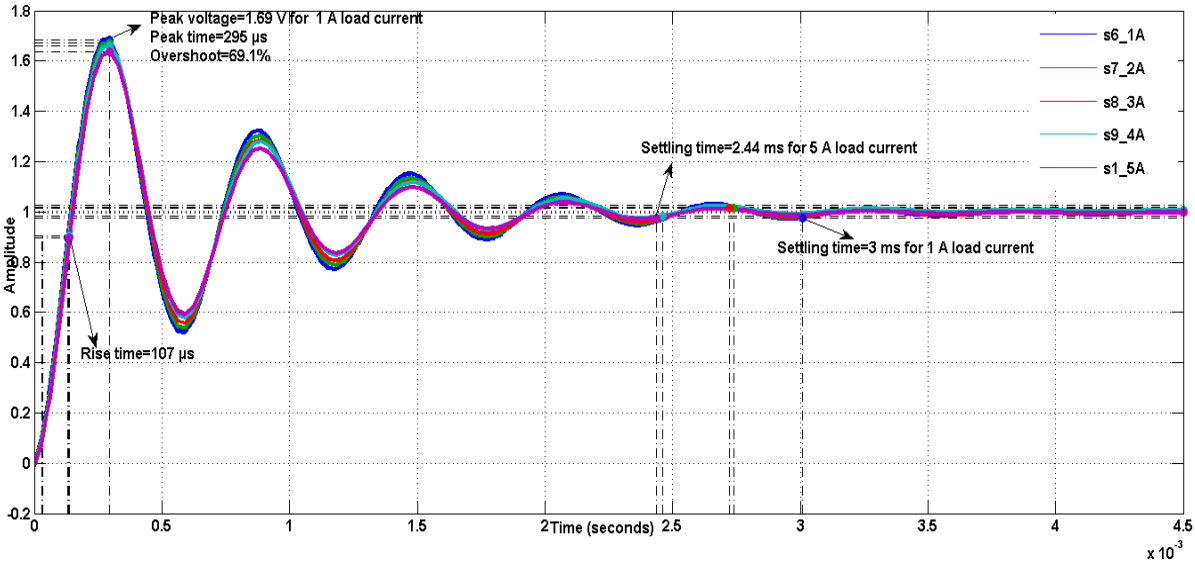


Figure 3.14 Open loop unit step plot of three-phase IBDDC in boost mode for different values of load current.

The three-phase IBDDC in boost mode is not stable for any input voltage of, 35 V, 42 V, 48 V, 55 V and 60 V and also the converter system is not stable even for the output load current of 2 A, 3 A, 4 A and Full load, but stable for load current of 1 A.

The open loop transfer function of three-phase IBDDC in boost mode uses with its forward feedback factor $\left(\beta = \frac{1}{70}\right)$ which is used to convert the output voltage to the reference voltage $\left(V_{ref} = 1V\right)$ corresponding to desired output voltage of 70 V, and then multiply by the modulator gain $\left(V_M = \frac{1}{3}\right)$ in which fixed frequency saw tooth wave magnitude of 3 V is considered. Open loop transfer function of three-phase IBDDC in boost mode along with the feedback factor and modulator is obtained (3.40), and its bode plot is shown in Figure 3.15.

$$sys2 = \frac{-0.011s^2 + 1431s + 55.5\times10^6}{s^2 + 4634s + 112\times10^6} \tag{3.40}$$

Corresponding to f_C of 4 kHz in Figure 3.15, phase shift of -156^o and gain of -18.5 dB are measured. Type III compensator is being selected based on the phase shift introduced by the three-phase IBDDC in boost mode. Elements of type III compensator is calculated with the help of K factor method in (2.33), (2.34), (2.35), (2.36), (2.37), and (2.38) by assuming the desired PM of 50^o.

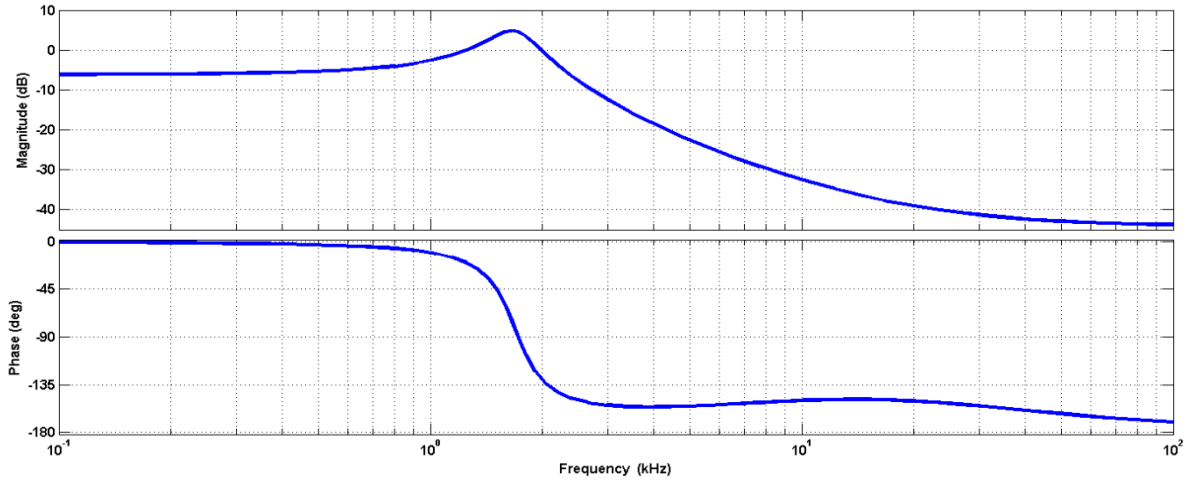


Figure 3.15 Bode plot of three-phase IBDDC in boost mode with feedback and modulator.

After substituting the selected values of resistor and capacitor values in (2.31), the type III compensator forward transfer function for three-phase IBDDC in boost mode is obtained (3.41). Bode plot of type III compensator for three-phase IBDDC in boost mode (3.41) is shown in Figure 3.16.

$$sys3 = \frac{9.519\times10^{06}s^2 + 3.362\times10^{10}s + 2.969\times10^{13}}{s^3 + 1.788\times10^{05}s^2 + 7.995\times10^{09}s} \qquad (3.41)$$

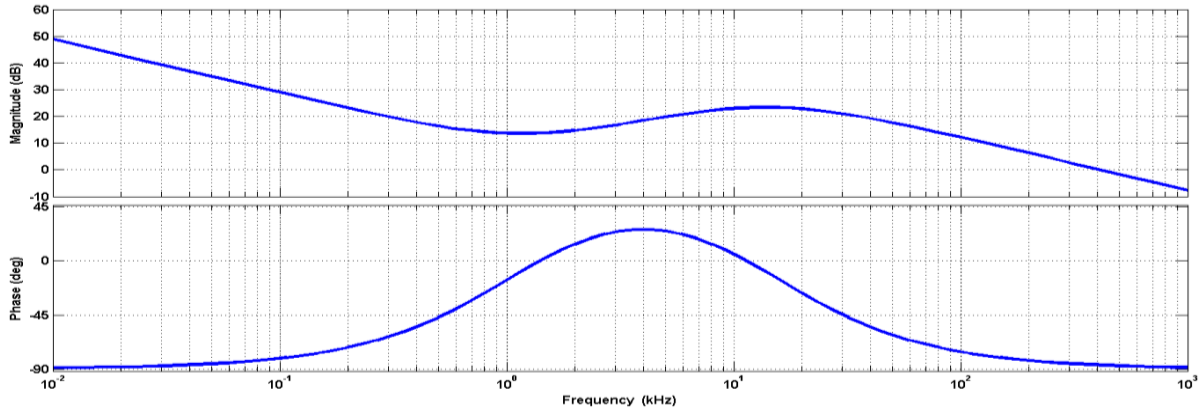


Figure 3.16 Bode plot of type III compensator for three-phase IBDDC in boost mode.

In Figure 3.16, gain of 18.5 dB can be obtained corresponds to f_C of 4 kHz at which controller forces the system to be a stable for any line or load transient occurs. An equivalent digital controller using bilinear transformation technique in Z-domain corresponding to sampling time Ts=10 µs for (3.41) is given by

$$sys3d = \frac{1.757z^3 - 1.515z^2 - 1.749z + 1.523}{z^3 - 2.203z^2 + 1.565z - 0.3619} \qquad (3.42)$$

Loop transfer function of three-phase IBDDC in boost mode is obtained in (3.43) which combines with the system transfer function, feedback factor, modulator gain and

compensator. Loop bode plot of BDDC in boost mode is shown in Figure 3.17 and corresponding closed loop unit step response is shown in Figure 3.18 .

$$sys4 = \frac{-5624s^4 + 6.5\times10^8 s^3 + 3.849\times10^{13} s^2 + 4.41\times10^{17} s + 1.44\times10^{21}}{s^5 + 1.039\times10^5 s^4 + 3.042\times10^9 s^3 + 2.26\times10^{13} s^2 + 2.77\times10^{17} s} \quad (3.43)$$

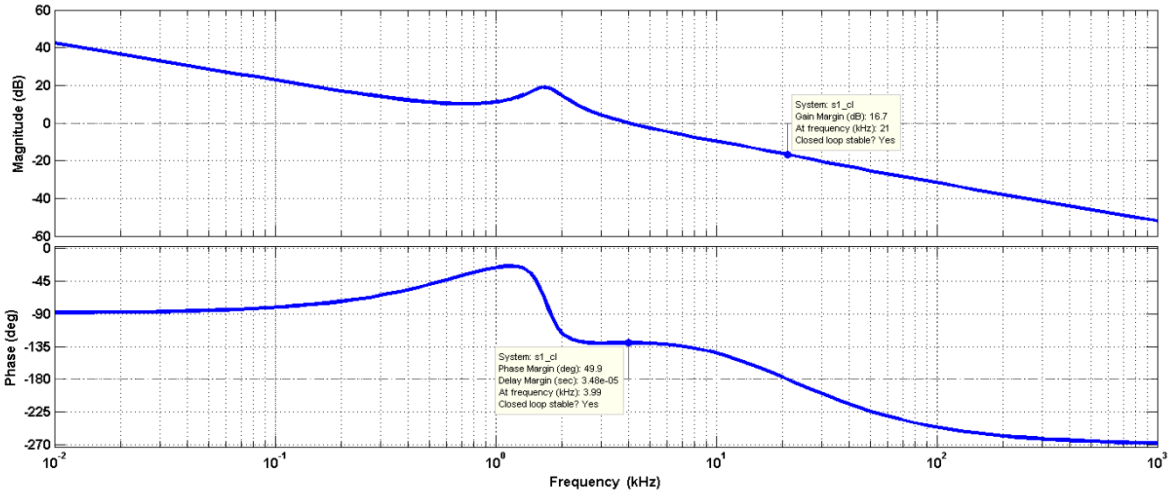


Figure 3.17 Loop bode plot of three-phase IBDDC in boost mode

From Figure 3.17, three-phase IBDDC in boost mode results with PM of 50^0 is obtained corresponds to loop cross over frequency of $f_c = 3.99$ kHz and GM of 16.7 dB is obtained corresponds to -180^0 phase at 21 kHz for input voltage of 48 V and load current of 5 A.

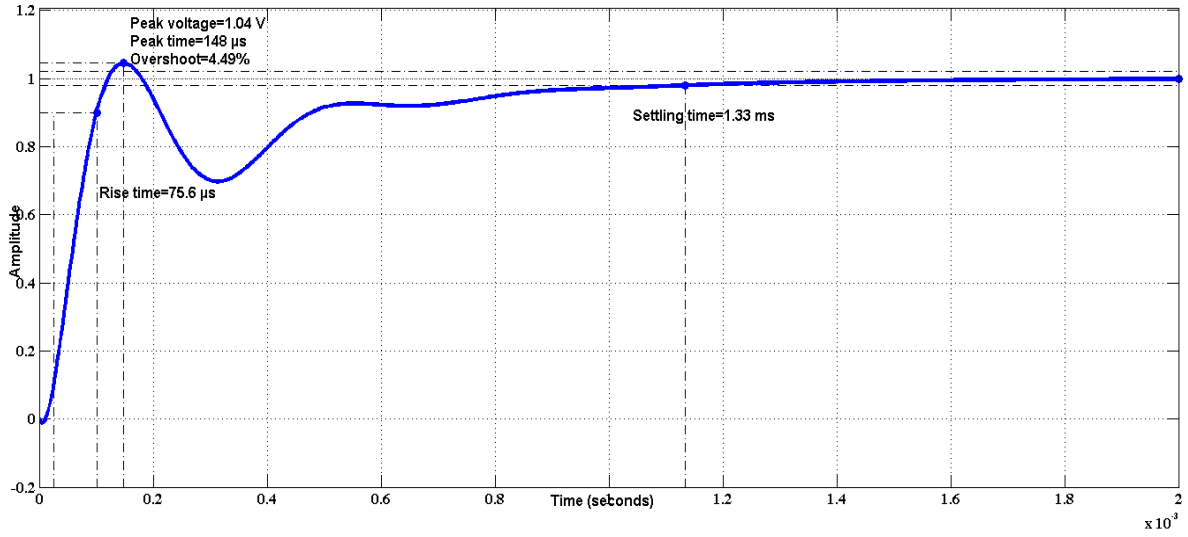


Figure 3.18 Closed loop unit step response plot of three-phase IBDDC in boost mode.

From Figure 3.18, three-phase IBDDC in boost mode results with rise time 75.6 µs, peak over shoot of 1.04 V with 4.49% at 148 µs, settling time of 1.13 ms and steady state value of 1 V for input voltage of 48 V and load current of 5 A.

Loop bode plot and closed loop unit step response of three-phase IBDDC in boost mode for different input voltages of 35 V, 42 V, 48 V, 55 V, and 60 V are shown in Figure 3.19 and Figure 3.20 respectively. Loop bode plot and closed loop unit step response of three-phase IBDDC in boost mode for different load currents of 1 A, 2 A, 3 A, 4 A and 5 A are plotted in Figure 3.21 and Figure 3.22 respectively.

From the loop bode plot as shown in Figure 3.19, GM of 16.8 dB and PM of 49.9^{o} are obtained for different values of line voltages of 35 V, 42 V, 48 V, 55 V, and 60 V.

Similarly from the closed loop unit step response as shown in Figure 3.20, three-phase IBDDC in boost mode results with rise time 48 µs, peak over shoot of 1.09 V with 8.72% at 109 µs, settling time of 995 µs and steady state value of 1 V for different values of input voltages.

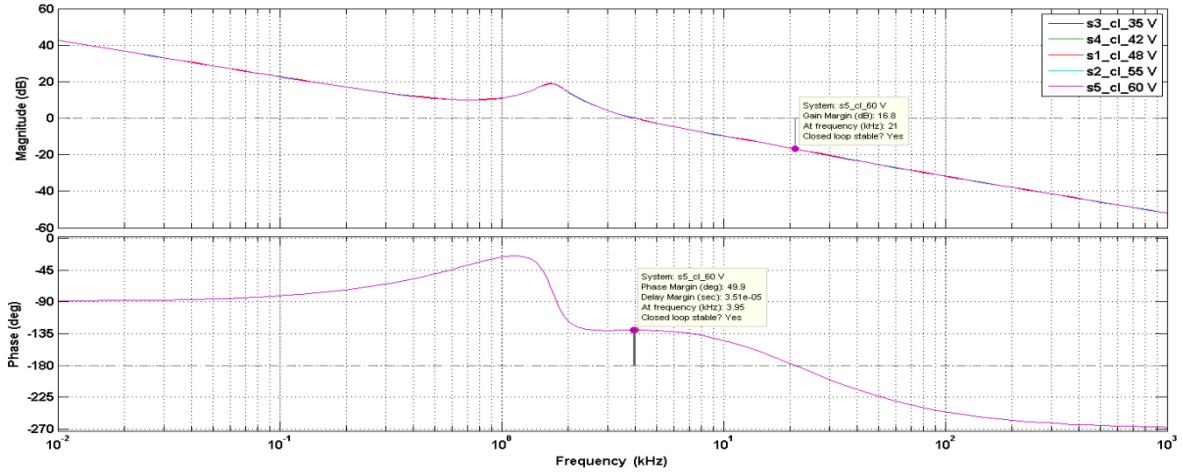


Figure 3.19 Loop bode plot of three-phase IBDDC in boost mode for different values of input voltage V_1.

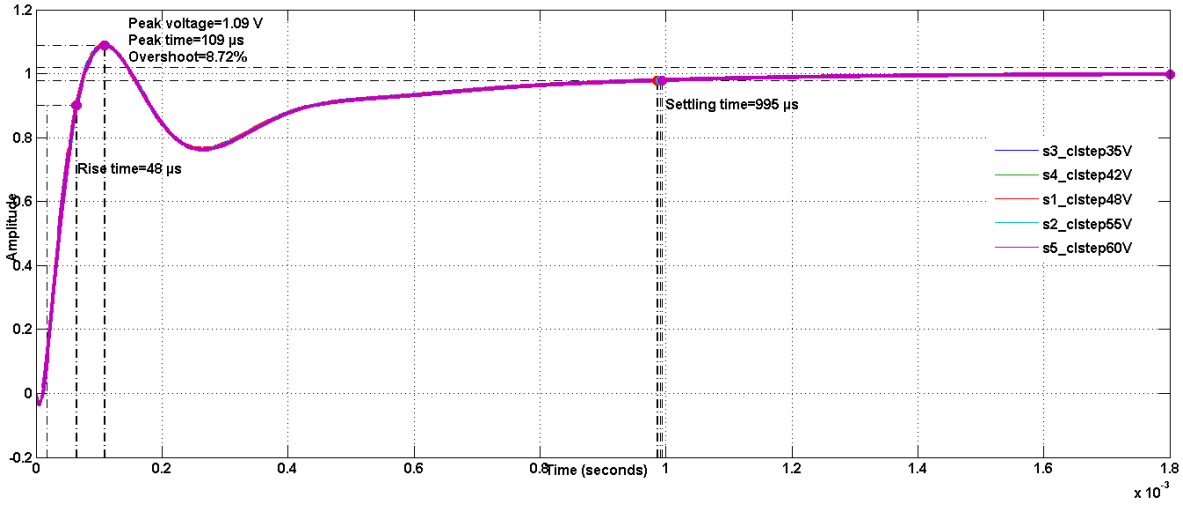


Figure 3.20 Closed loop unit step plot of three-phase IBDDC in boost mode for different values of input voltage.

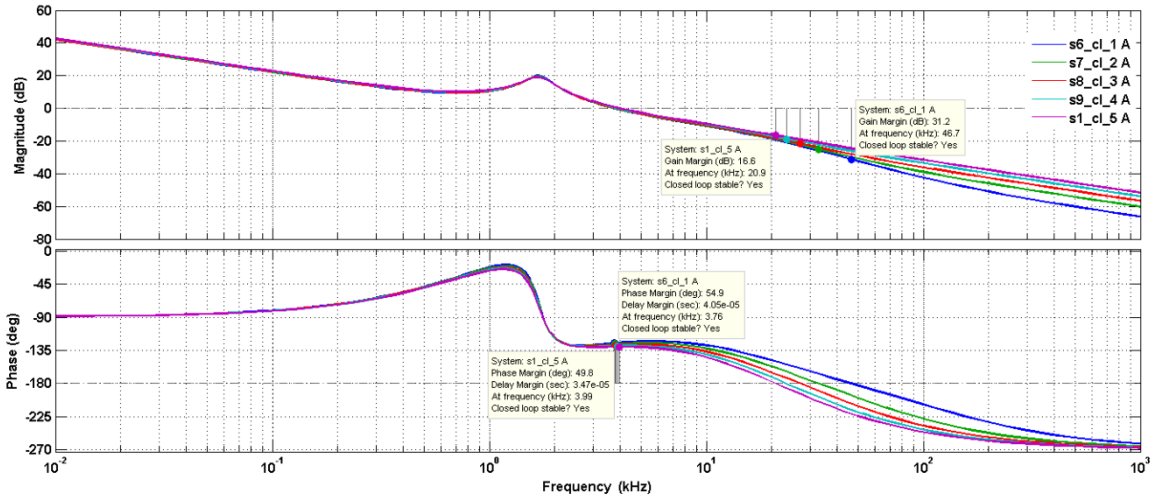


Figure 3.21 Loop bode plot of three-phase IBDDC in boost mode for different values of load current I_{o2}.

From the loop bode plot as shown in Figure 3.21, GM of 16.6 dB and PM of 49.9^0 are obtained for 5 A current, and PM of 54.9^0 is obtained different values of load current of 1 A, 2 A, 3 A and 4 A.

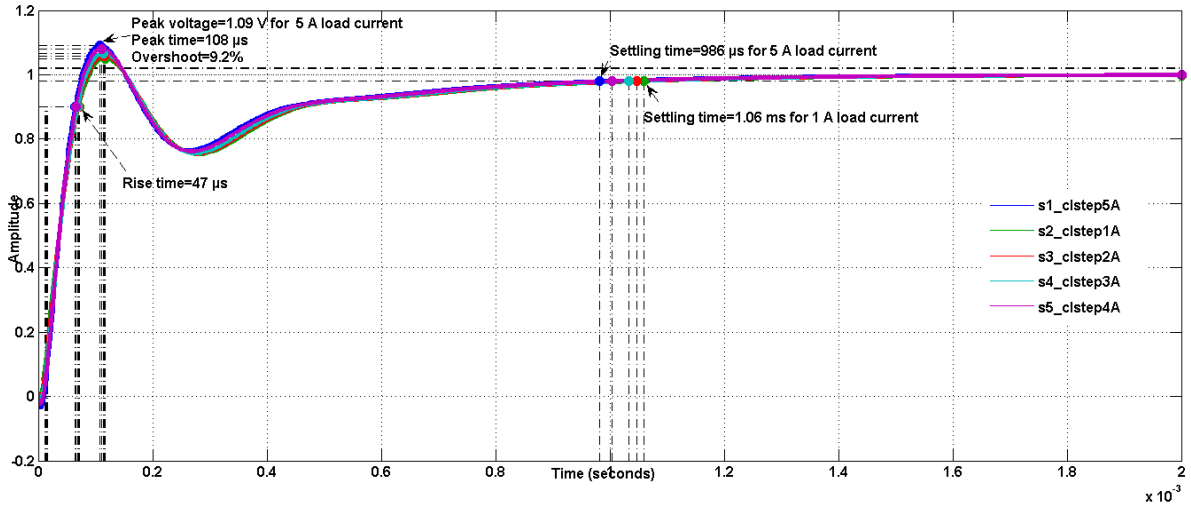


Figure 3.22 Closed loop unit step plot of three-phase IBDDC in boost mode for different load current I_{o2}.

From the closed loop unit step response as shown in Figure 3.22, three-phase IBDDC in boost mode for load current of 5 A results with rise time 47 µs, peak over shoot of 1.09 V with overshoot of 9.2% at 108 µs, settling time of 986 µs for 5 A, settling time of 1.06 ms for 1 A with steady state value of 1 V.

GM and PM are within safe limits corresponding to cross over frequency and then the type III compensator stabilises the three-phase IBDDC in boost mode for different input voltages and load transients.

3.7.3 Design of Type III Error Amplifier for Three-Phase IBDDC in Buck mode

In order to understand the system behaviour of the three-phase IBDDC in buck mode against line voltage variations and load transients, the open loop bode plot of small signal transfer function control to output voltage of the three-phase IBDDC in buck mode is plotted for different input voltage ranges 60 V, 65 V, 70 V, 75 V and 80 V, and open loop unit step response plot for the same are shown in Figure 3.23 and Figure 3.24 respectively. Similarly the open loop bode plot of small signal transfer function control to output voltage of the three-phase IBDDC in buck mode is also plotted for different load current of 1.25 A, 2.5 A, 4 A, 5 A, and 6 A, and open loop unit step response plot for the same are shown in Figure 3.25 and Figure 3.26 respectively.

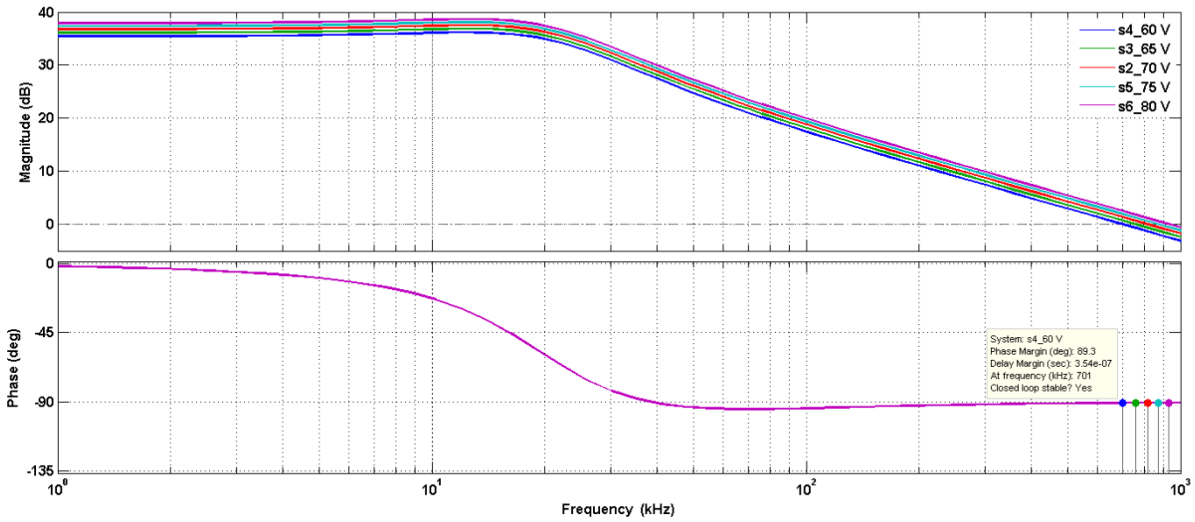


Figure 3.23 Open loop bode of different values of input voltage V_2 for three-phase IBDDC in buck mode.

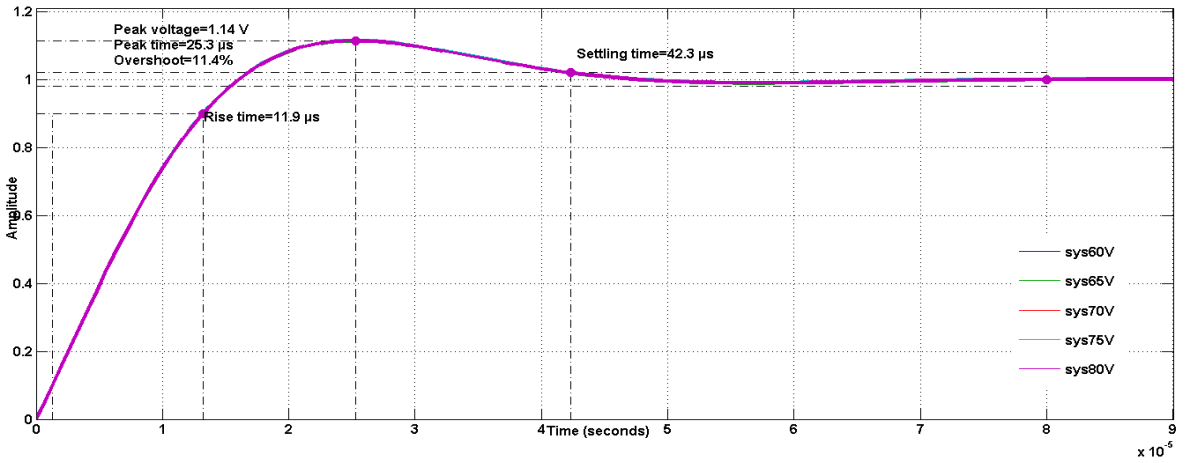


Figure 3.24 Open loop unit step plot of three-phase IBDDC in buck mode for different input voltages.

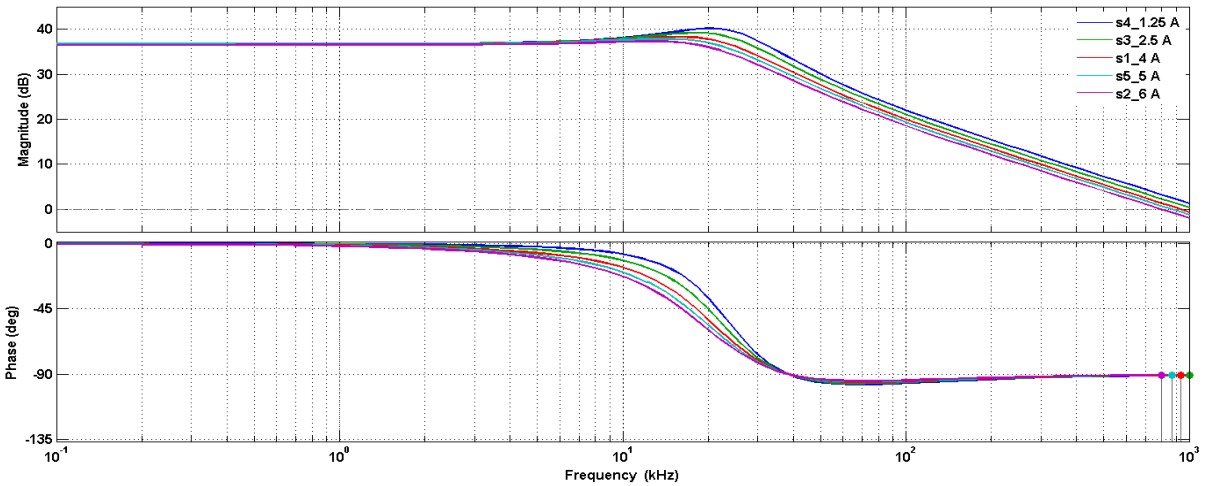


Figure 3.25 Open loop bode of three-phase IBDDC in buck mode for different load currents.

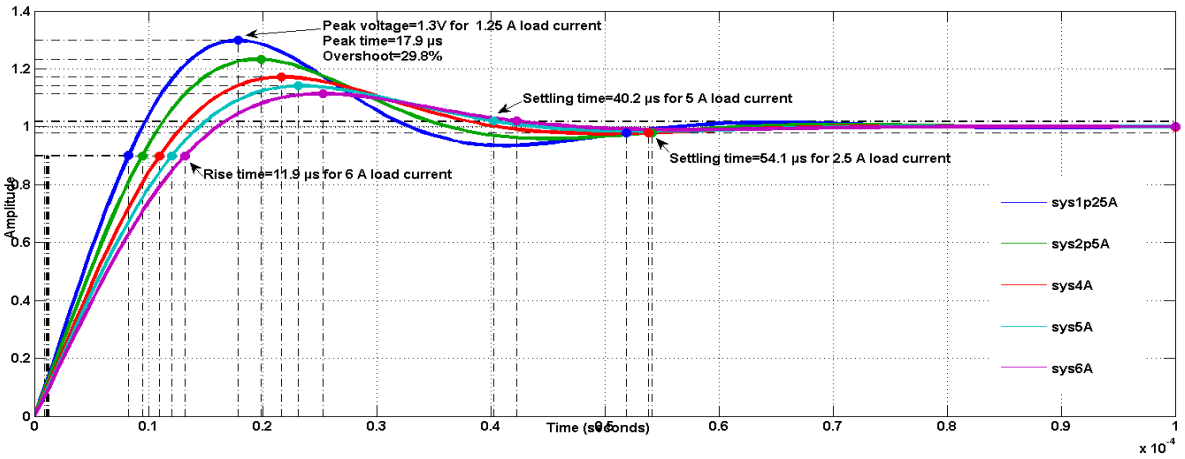


Figure 3.26 Open loop unit step plot of three-phase IBDDC in buck mode for different load currents.

Initially, the three-phase IBDDC in buck mode is stable for any input voltage of 60 V, 65 V, 70 V, 75 V and 80 V, and also the converter system is stable even for the output load current of 1.25 A, 2.5 A, 4 A, 5 A, and 6 A.

The open loop transfer function of BDDC in buck mode uses with its forward feedback factor $\left(\beta_1 = \frac{1}{48}\right)$ which is used to convert the output voltage to the reference voltage $\left(V_{ref1} = 1V\right)$ corresponding to desired output voltage of 48 V, and then multiply by the modulator gain $\left(V_{M1} = \frac{1}{3}\right)$ in which fixed frequency saw tooth wave magnitude of 3 V is considered. Open loop transfer function of three-phase IBDDC in buck mode along with the feedback factor and modulator is obtained(3.44). Bode plot of open loop three-phase IBDDC in buck mode with feedback and modulator is shown in Figure 3.27.

$$sys6 = \frac{35626s + 7501\times10^{6}}{s^{2} + 153.35\times10^{3}s + 15.7\times10^{9}} \tag{3.44}$$

Corresponding to f_C of 25 kHz in Figure 3.27, phase shift of -73.34^{o} and gain of $-8.84\ dB$ are measured. Type III compensator is being selected based on the phase shift introduced by the three-phase IBDDC in buck mode. Elements of type III compensator is calculated with the help of K factor method in (2.33),(2.34),(2.35),(2.36),(2.37), and (2.38) by assuming the desired PM of 55^{o}.

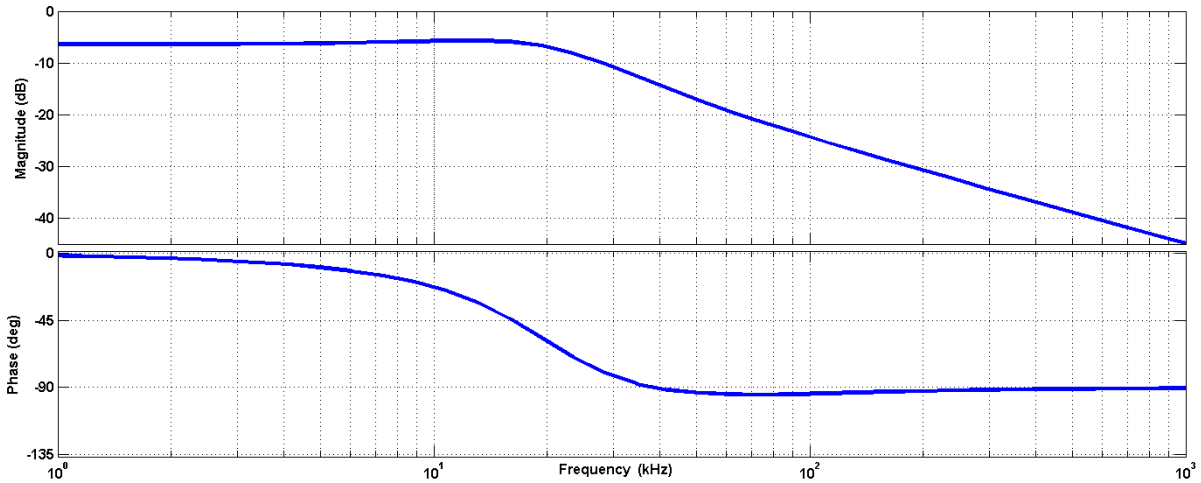


Figure 3.27 Bode plot of three-phase IBDDC in buck mode with feedback and modulator.

After substituting the selected values of resistor and capacitor values in (2.31), the type III compensator forward transfer function for three-phase IBDDC in buck mode is obtained . Bode plot of type III compensator for three-phase IBDDC in buck mode is shown in Figure 3.28

$$sys3 = \frac{9.519\times10^{06}s^{2} + 3.362\times10^{10}s + 2.969\times10^{13}}{s^{3} + 1.788\times10^{05}s^{2} + 7.995\times10^{09}s} \tag{3.45}$$

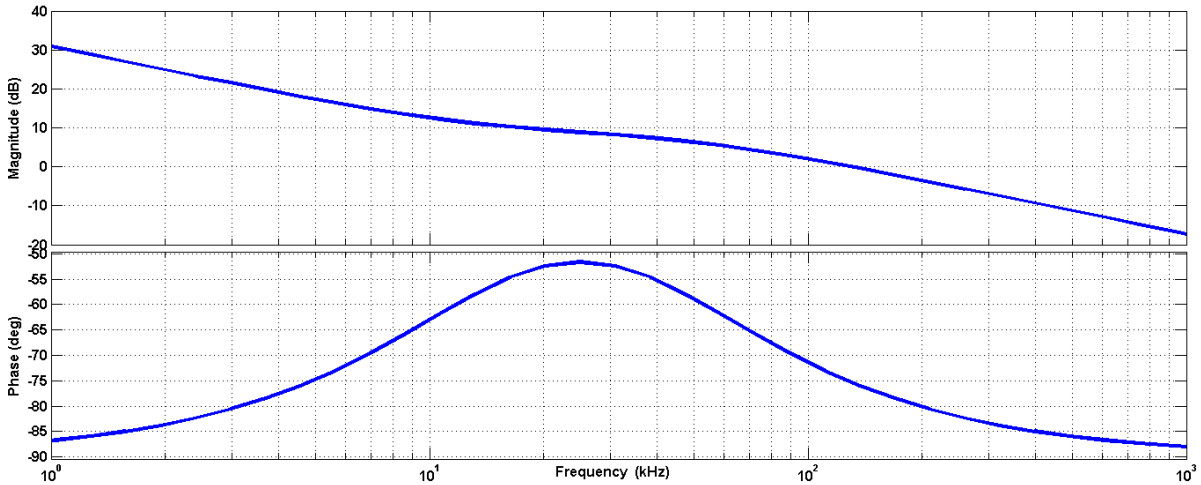


Figure 3.28 Bode plot of type III compensator for three-phase IBDDC in buck mode.

In Figure 3.28, gain of 8.84 dB can be obtained corresponds to f_C of 25 kHz at which controller forces the system to be a stable for any line or load transient occurs. An equivalent digital controller using bilinear transformation technique in Z-domain corresponding to sampling time T_s=10 µs for (3.45) is given by

$$sys3d = \frac{2.357z^3 + 1.02z^2 - 1.147z + 0.1896}{z^3 - 0.9001z^2 - 0.09741z - 0.002495} \tag{3.46}$$

Loop transfer function of three-phase IBDDC in buck mode is obtained in (3.47) which combines with the system transfer function, feedback factor, modulator gain and compensator. Loop bode plot of IBDDC in buck mode is shown in Figure 3.29 and corresponding closed loop unit step response is shown in Figure 3.30.

$$sys4 = \frac{3.0826\times10^{10}s^3 + 1.33\times10^{16}s^2 + 1.823\times10^{21}s + 8.046\times10^{25}}{s^5 + 5.95\times10^5 s^4 + 1.324\times10^{11}s^3 + 1.44\times10^{16}s^2 + 7.147\times10^{20}s} \tag{3.47}$$

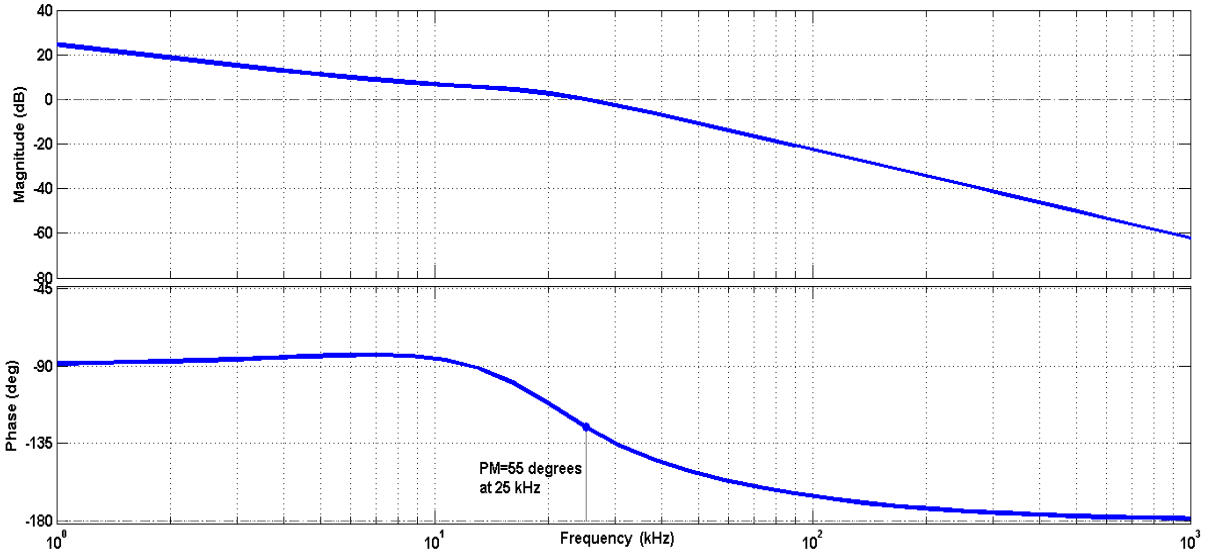


Figure 3.29 Loop bode plot of three-phase IBDDC in buck mode.

From Figure 3.29, three-phase IBDDC in buck mode results with PM of 55^0 is obtained corresponds to loop cross over frequency of $f_c = 25\ kHz$ and GM of ∞ dB is obtained corresponds to -180^0 phase for input voltage of 70 V and load current of 6 A.

From Figure 3.30, three-phase IBDDC in buck mode results with rise time 9.6 µs, peak over shoot of 1.06 V with 5.71% at 18.3 µs, settling time of 48.1 µs and steady state value of 1 V for input voltage of 48V and load current of 5 A.

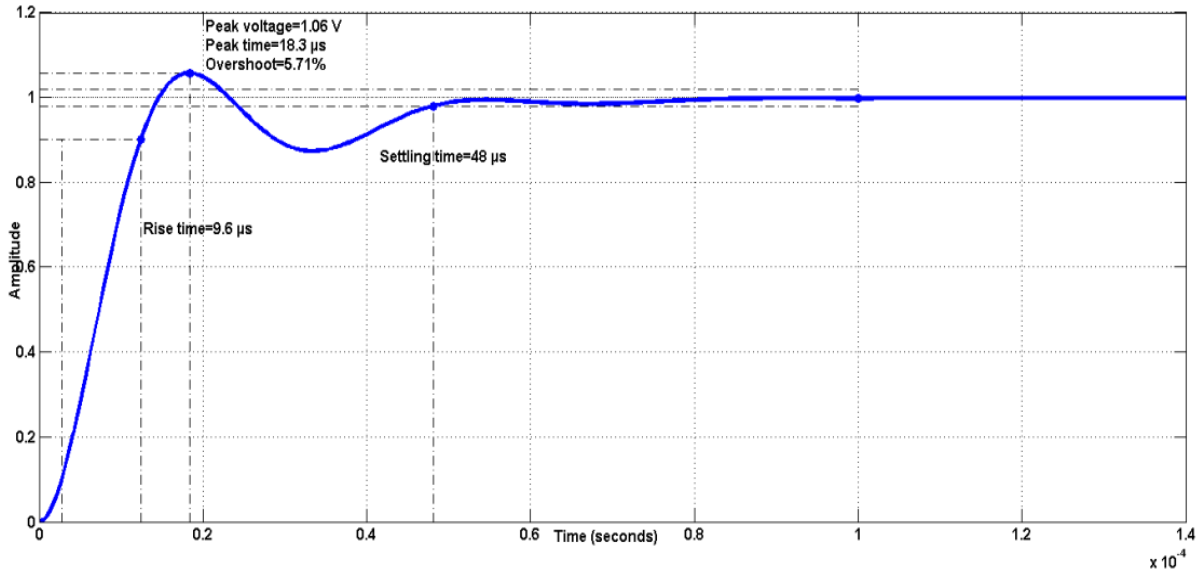


Figure 3.30 Closed loop unit step response plot of three-phase IBDDC in buck mode.

Loop bode plot and closed loop unit step response of three-phase IBDDC in buck mode for different input voltages of 60 V, 65 V, 70 V, 75 V, and 80 V are shown in Figure 3.31 and Figure 3.32 respectively. Loop bode plot and closed loop unit step response of three-phase IBDDC in buck mode for different load currents of 1.25 A, 2.5 A, 4 A, 5 A and 6 A are plotted in Figure 3.33 and Figure 3.34 respectively.

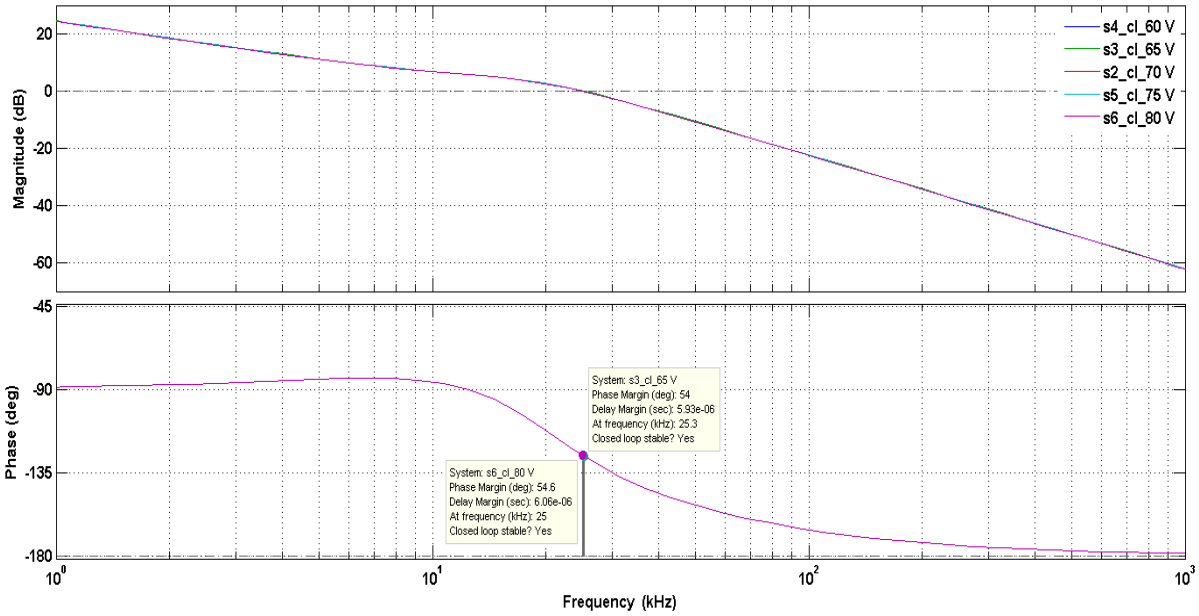


Figure 3.31 Loop bode plot of three-phase IBDDC in buck mode for different input voltages.

From the loop bode plot as shown in Figure 3.31, GM of ∞ dB and PM of 55^{o} are obtained for different values of line voltages of 60 V, 65 V, 70 V, 75 V, and 80 V.

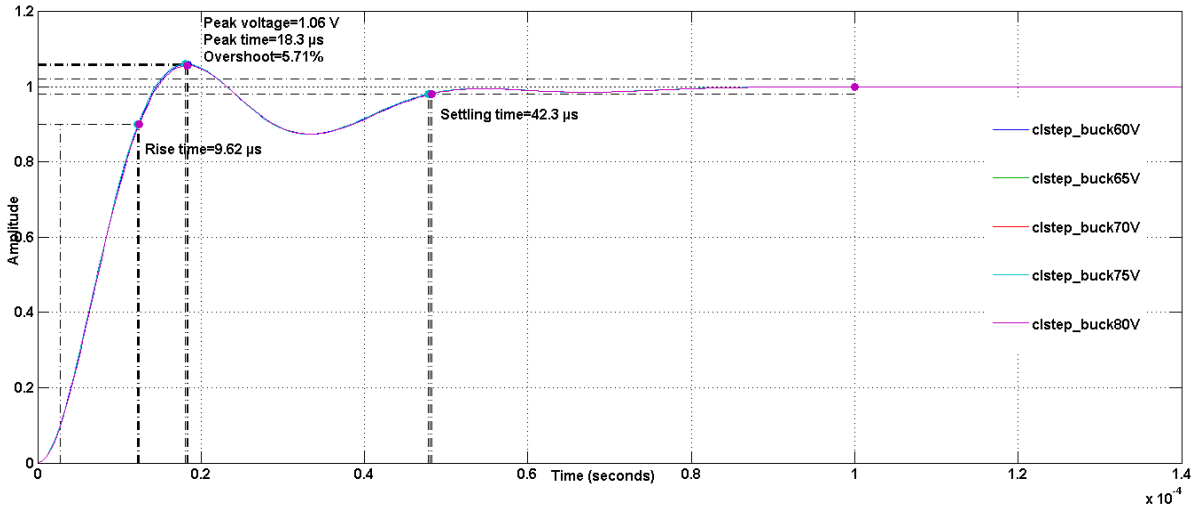


Figure 3.32 Closed loop unit step plot of three-phase IBDDC in buck mode for different input voltages.

Similarly from the closed loop unit step response as shown in Figure 3.32, three-phase IBDDC in buck mode results with rise time 9.62 µs, peak voltage of 1.06 V with overshoot of 5.71% at 18.3 µs, settling time of 42.3 µs and steady state value of 1 V for different values of input voltages.

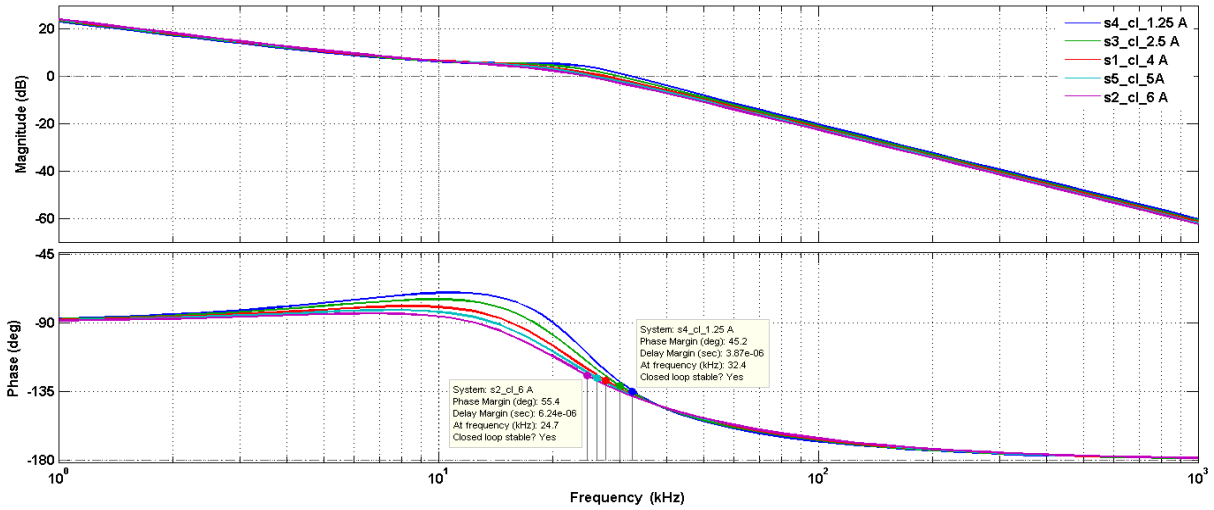


Figure 3.33 Loop bode plot of three-phase IBDDC in buck mode for different values of load currents.

From the loop bode plot as shown in Figure 3.33, GM of ∞ dB and PM of 55.4^0 are obtained for 6 A current, and PM of 45.2^0 for 1.25 A is obtained.

From the closed loop unit step response as shown in Figure 3.34, IBDDC in buck mode for load current of 1.25 A results with rise time 11 µs, peak voltage of 1.07 V with overshoot of 6.74% at 23.3 µs, and settling time of 229 µs. Similarly, IBDDC in buck mode for load current of 6 A results with rise time 4.27 µs, peak voltage of 1.05 V with overshoot of 5.12% at 9.35 µs, and settling time of 192 µs.

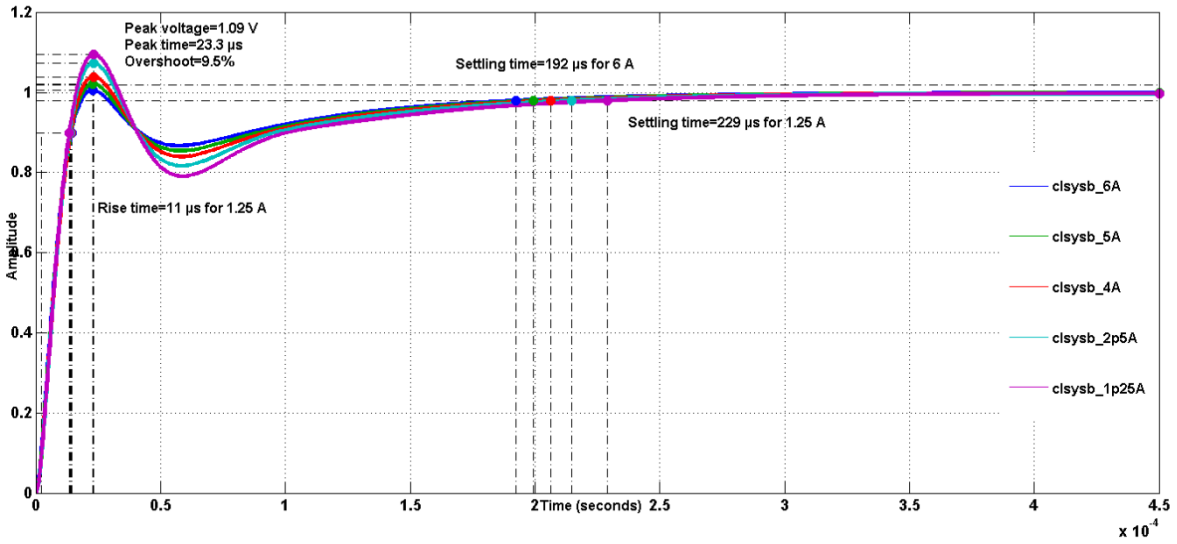


Figure 3.34 Closed loop unit step plot of three-phase IBDDC in buck mode for different load currents.

GM and PM are within safe limits corresponding to cross over frequency and then the type III compensator stabilises the three-phase IBDDC in buck mode for different input voltages and load transients.

The performance analysis of type 3 error amplifier for three-phase IBDDC is tabulated in Table 2.1.

Table 3.2 Performance of type 3 error amplifier on three-phase IBDDC.

Three-phase IBDDC	Boost mode			Buck mode		
	t_r (µs)	Overshoot (%)	t_s (ms)	t_r (µs)	Overshoot (%)	t_s (µs)
Line voltage change	48	8.72	0.995	9.62	5.71	42.3
Load current change	47	9.2	1.06	4.27	4.27	35.9

From the above table, whenever the line voltage (minimum to maximum input voltage) and load current (minimum to maximum load) change occurs, type-3 error amplifier for three-phase IBDDC in both boost mode and buck mode will provide precise output by minimizing the rise time, overshoot voltage and settling time.

3.8 Fuzzy Logic Controller for Three-Phase IBDDC

The block diagram of Fuzzy Logic Controller (FLC) for three-phase IBDDC is as shown in Figure 3.35 . FLC takes the error (e) as the one of the input and change in error (ce) as the other input which are given by

$$e = V_f - V_{ref} \tag{3.48}$$

$$ce = e_k - e_{k-1} \tag{3.49}$$

where V_f is the feedback voltage, V_{ref} is the reference voltage corresponds to output voltage and e_k and e_{k-1} are the error at kth and (k-1)th sample.

The change in duty cycle (∂d_k) is the output of FLC and the duty cycle d_k is given by

$$d_k = I_k + \partial d_k \tag{3.50}$$

Where I_k is the linear integrator output of the error e_k . The linear integrator is used to obtain zero steady state error.

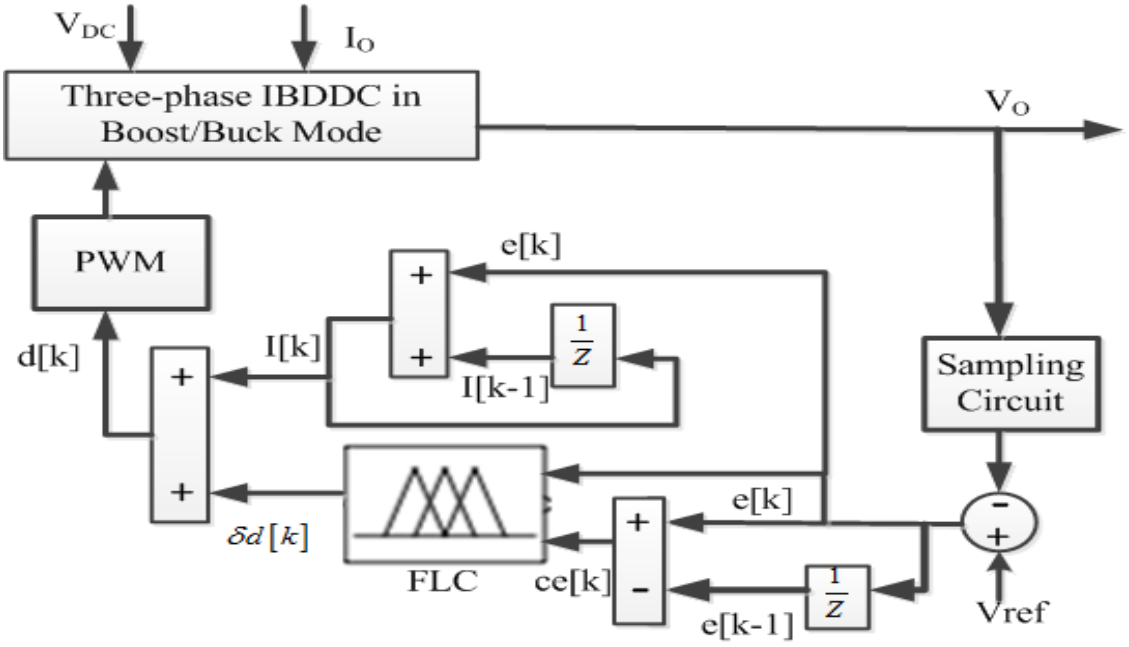


Figure 3.35 Block diagram of FLC for three-phase IBDDC

There are 9 subsets are in FLC for three-phase IBDDC in boost mode: N4, N3, N2, N1, Z, P1, P2, P3 and P4 and there were 7 subsets are in FLC for three-phase IBDDC in buck mode: N3, N2, N1, Z, P1, P2 and P3. Where N represents negative, Z indicates zero and P represent positive. The relation between the fuzzy inputs (e_k and ce_k) and corresponding membership degree variables $\left(\mu_e[e_k] and \mu_{ce}[ce_k]\right)$ are as shown in Figure 3.36 and Figure 3.37 respectively.

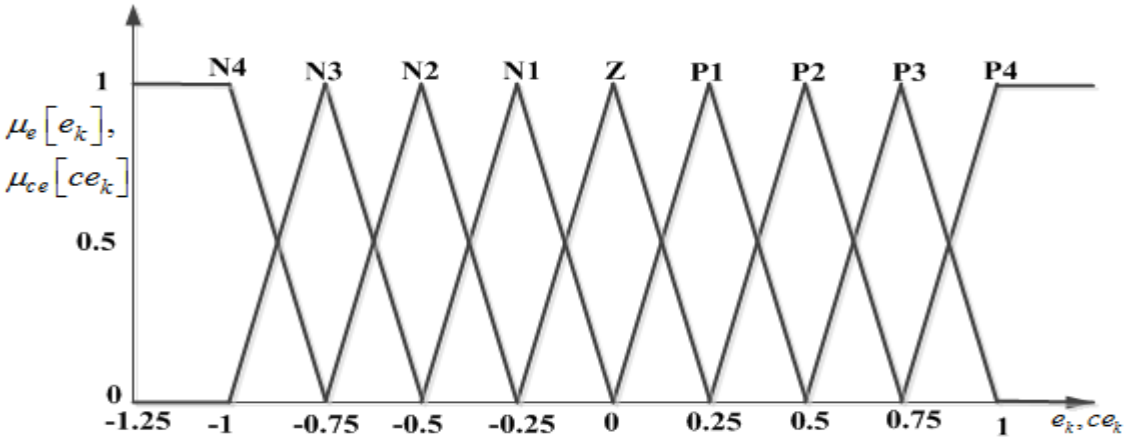


Figure 3.36 Membership function of e_k and ce_k for three-phase IBDDC in boost mode

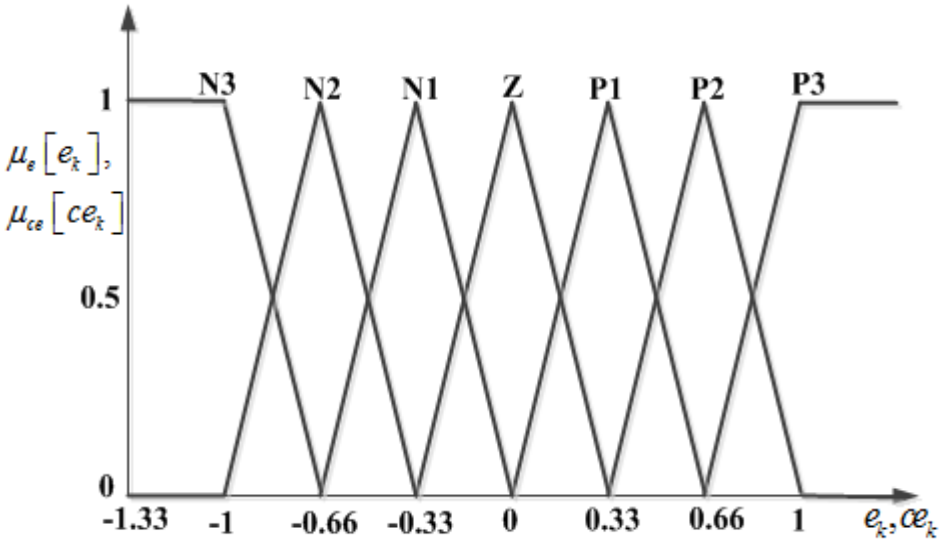


Figure 3.37 Membership function of e_k and ce_k for three-phase IBDDC in buck mode

9*9 rule base is designed and implemented for three-phase IBDDC in boost mode. 7*7 rule base is designed and implemented for three-phase IBDDC in buck mode.

Rule base FLC of three-phase IBDDC in boost and in buck mode are tabulated in Table 3.3 and Table 3.4 respectively. The result of inference mechanism consists of weighting factor (w_i) of the individual rule and degree of change of duty cycle (c_i). The corresponding weighting factor is obtained by Mamdani's min fuzzy implication and is given by the following relation

$$w_i = \min\left(\mu_e\left[e_k\right], \mu_{ce}\left[ce_k\right]\right) \tag{3.51}$$

Inferred output of each rule is given by the following relation

$$z_i = w_i \times c_i = \min\left\{\mu_e\left[e_k\right], \mu_{ce}\left[ce_k\right]\right\} \times c_i \tag{3.52}$$

z_i is the change of duty cycle inferred by ith rule.

Table 3.3 Rule base table of FLC for three-phase IBDDC in boost mode

		Change in error(*ce*)								
		N4	N3	N2	N1	Z	P1	P2	P3	P4
Error(*e*)	P4	Z	N1	N2	N3	N4	N4	N4	N4	N4
	P3	P1	Z	N1	N2	N3	N4	N4	N3	N4
	P2	P2	P1	Z	N1	N2	N3	N2	N4	N4
	P1	P3	P2	P1	Z	N1	N1	N2	N3	N4
	Z	P4	P3	P2	P1	Z	N1	N2	N3	N4
	N1	P4	P3	P2	P1	P1	Z	N1	N2	N3
	N2	P4	P4	P2	P2	P2	P1	Z	N1	N2
	N3	P4	P3	P3	P3	P2	P2	P1	Z	N1
	N4	P4	P4	P4	P4	P3	P2	P2	P1	Z

Table 3.4 Rule base table of FLC for three-phase IBDDC in buck mode

		Change in error(ce)						
		N3	N2	N1	Z	P1	P2	P3
Error(e)	P3	Z	N1	N2	N3	N3	N3	N3
	P2	P1	Z	N1	N2	N3	N2	N3
	P1	P2	P1	Z	N1	N1	N3	N3
	Z	P3	P2	P1	Z	N1	N2	N3
	N1	P3	P3	P1	P1	Z	N1	N2
	N2	P3	P2	P3	P2	P1	Z	N1
	N3	P3	P3	P3	P3	P2	P1	Z

Centre of average method is being preferred to defuzzify the result to obtain the crisp value of change of duty cycle. When triangle shaped member function is being used, at most 4 rules must be considered at any time for the best performance.

The change of duty cycle is given by the following relation

$$z = \partial d\left[k\right] = \frac{\sum_{i=1}^{M} z_i}{\sum_{i=1}^{M} c_i} = \frac{\sum_{i=1}^{M} w_i \times c_i}{\sum_{i=1}^{M} c_i} \tag{3.53}$$

where M represents the maximum number of effective rules.

3.9 Simulation and Experimental Results of IBDDC

Non ideal three-phase IBDDC circuit has been used in the simulation and it has been carried out in MATLAB/SIMULINK software. SimPowerSystem circuit model of three-phase IBDDC in boost mode and buck mode circuit is as shown in Figure 3.38.

3.9.1 Simulation of Three-Phase IBDDC

To assess the feasibility of the type III compensator control strategy and FLC, simulations are performed with the specifications as tabulated in Table 3.5 of three-phase IBDDC circuit.

Table 3.5 Specification and design parameters of three-phase IBDDC

Parameters	Boost mode	Buck mode
Supply voltage	48 V ±10% (E_1)	70 V ±10% (E_2)
Output voltage	70 V (V_2)	48 V (V_1)
Load current	5 A (I_{o2})	6 A (I_{o1})
Operating frequency	100 kHz (f_s)	100 kHz (f_s)
Duty ratio for nominal values	0.32	0.68
Inductors (L1=L2=L3)	120 μH	120 μH
Internal resistance of inductor	10.5 mΩ	10.5 mΩ
Output capacitor	100 µF	1 µF
Internal resistance of capacitor	0.18 Ω	4.7 Ω
On state resistance of MOSFETs	55 mΩ	55 mΩ
Forward resistance of diodes	17.1 mΩ	17.1 mΩ
Cut-in voltage of diodes	0.7 V	0.7 V

3.9.1.1 Simulation Results and Discussions

In order to understand the behavior of three-phase IBDDC, simulation circuit shown in Figure 3.38 is carried out for 50 ms duration, three-phase IBDDC operates as boost DC-DC converter from 0 to 25 ms. Similarly three-phase IBDDC operates as buck DC-DC converter from 25 ms to 50 ms. Average boost inductor current (I_{LB}) is considered as reference current, which is in the same direction as the initial orientation of (I_{LB}) from 0 to 50 ms, average buck inductor current (I_L) flows opposite to the initial orientation of (I_{LB}) from 25 ms to 50 ms.

During boost mode, switches S_4, S_5 and S_6, and diodes D_1, D_2 and D_3 will conduct. During buck mode, switches S_1, S_2 and S_3, and diodes D_4, D_5 and D_6 will conduct. Three-phase IBDDC in boost mode carries an average inductor current I_{LB} of 8.26 A which results in ripple current of 0.1 A. Three-phase IBDDC in buck mode carries an average inductor current I_L of 6 A which results in ripple current of 0.1 A as shown in Figure 3.39.

Dynamic response of three-phase IBDDC in boost mode against line voltage (V_1) variations and load current (I_{o2}) variations using type 3 compensator and FLC are shown in Figure 3.40 and Figure 3.41 respectively.

In Figure 3.40, when the three-phase IBDDC operates in boost mode with constant load current I_{o2} of 5A, it results with negative slope because of RHP zero. When the three-phase IBDDC operates in boost mode against the input voltage V_1 varied from 48 V to 44 V, 44 V to 50 V, the desired boost output voltage V_2 has been reached to steady state voltage of 70 V within 1 ms using FLC, which results less overshoot voltage and reduced oscillations, but using type 3 compensator, the output voltage V_2 will reach to steady state output voltage of 70 V within 3 ms, which results more overshoot voltage compared to FLC.

In Figure 3.41, when the three-phase BDDC operates in boost mode against the load current I_{o2} varied from 1 A to 3 A, 3 A to 5 A with constant input voltage V_1 of 48 V, the desired boost output voltage V_2 has been reached to steady state voltage of 70 V within 200 µs using FLC, which results less overshoot voltage and reduced oscillations, but using type 3 compensator, the output voltage V_2 will reach to steady state output voltage of 70 V within 200 µs, which results more overshoot voltage compared to FLC.

Dynamic response of three-phase IBDDC in buck mode against line voltage (V_2) variations and load current (I_{o1}) variations using type 3 compensator and FLC are shown in Figure 3.42 and Figure 3.43 respectively.

In Figure 3.42, when the three-phase IBDDC operates in buck mode with constant load current I_{o1} of 6 A, against the input voltage V_2 varied from 70 V to 65 V, 65 V to 68 V, 68 V to 72 V, the desired buck output voltage V_1 has been reached to steady state value of 48 V

within 20 μs using FLC, which results less overshoot voltage and reduced oscillations, but using type 3 compensator, the output voltage V_1 will reach to steady state output voltage of 70 V within 50 μs, which results more overshoot voltage compared to FLC.

In Figure 3.43, when the three-phase IBDDC operates in buck mode against the load current I_{o1} varied from 3 A to 5 A, 5 A to 6 A with constant input voltage V_2 of 70 V, the desired buck output voltage V_1 has been reached to steady state output voltage of 48 V within 20 μs using FLC, which results less overshoot voltage and reduced oscillations, but using type 3 compensator, the output voltage V_1 will reach to steady state output voltage of 48 V within 40 μs, which results more overshoot voltage and more oscillations compared to FLC.

3.10 Experimental Setup of IBDDC

Three-phase IBDDC has 3 set of boost/buck converter modules. LA25 current transducers are used for measurement of individual inductor currents (both in boost mode and buck mode), total input, and output load current of three-phase IBDDC. LEM voltage transducers are used to sense the input/output voltage of three-phase IBDDC.

3.10.1 Implementation of Digital Controller

For three-phase IBDDC in boost mode, gate pulses are generated by the TMS320F28335 ezdsp by comparing control voltage in counts with the up-down counter (sawtooth voltage) and shifted up-down counter (sawtooth) waveform. The compare value is 510. Time base period (TBPRD) register is loaded with a value of 750, then time base phase (TBPHS) value corresponding to the slave 2 is loaded with 500 to obtain 120^0 phase shift and TBPHS value corresponding to the slave 3 is loaded with 500 counts to obtain 240^0 phase shift. For three-phase IBDDC in buck mode, gate pulses are generated by the TMS320F28335 ezdsp by comparing control voltage with the up down counter (sawtooth voltage) and shifted down counter (sawtooth) waveform. The compare value is 240. TBPRD register is loaded with a value of 750, TBPHS value corresponding to the slave 2 is loaded with 500 to obtain 120^0 phase shift and TBPHS value corresponding to the slave 3 is loaded with 500 counts to obtain 240^0 phase shift. Using direct form-I structure, type III digital compensator is being implemented with the help of TMS320F28335 ezdsp to control the dynamic response of the three-phase IBDDC either in boost mode or buck mode.

3.10.2 Development of the Fuzzy Logic Controller on DSP

All the input variables of FLC are quantified and stored in individual memory. For each fuzzy set, the degree of membership is generated and stored in individual memory. The rule

base is stored in a dedicated memory block. The method of development consists of 3 steps. Firstly, the FLC is designed and then tuned using MATLAB with the help of Simulink and the fuzzy logic toolbox. The FLC is saved as a respective MATLAB file. Secondly, memory blocks are prepared using FLC. For each of the sub set, input variables are quantified and obtain the degree of membership. The rule base is coded such a way that the index of membership function leads to the corresponding rule base. At the final step, a binary file is created out of the stored MATLAB-file. The binary file then can be downloaded to the DSP.

3.10.3 Experimental Results and Discussions

Steady state inductor current waveforms of three-phase IBDDC in boost mode and buck mode are shown in Figure 3.44 and Figure 3.45 respectively. Dynamic load change transient waveforms of three-phase IBDDC in boost mode and buck mode; using type III error amplifier and FLC are shown in Figure 3.46, Figure 3.48 and Figure 3.47, Figure 3.49 respectively.

Figure 3.44 shows steady state inductor current (Ch4) for three-phase IBDDC in boost mode at 5 A, inductor current in phase 1 (Ch1), inductor current in phase 2 (Ch2) and inductor current in phase 3 (Ch3) while supplying 350 W with input voltage of 48 V.

Figure 3.45 shows steady state inductor current (Ch4) for three-phase IBDDC in buck mode at 6 A, inductor current in phase 1 (Ch1), inductor current in phase 2 (Ch2) and inductor current in phase 3 (Ch3) while supplying 288 W with input voltage of 70 V.

Dynamic performances of three-phase IBDDC in boost mode against load current I_{o2} varied from 1 A to 5 A with constant input voltage V_1 of 48 V using type III error amplifier is as shown in Figure 3.46. In Figure 3.46, the performance of three-phase IBDDC in boost mode with the sudden step change in load current I_{o2} (Ch4) varied from 2 A to 4 A and load current I_{o2} (Ch4) varied from 3 A to 5 A are shown in Figure 3.46(a) and Figure 3.46(b) respectively, with constant input voltage V_1 (Ch1) of 48 V, type III error amplifier provides steady state output voltage V_2 (Ch3) of 70 V within 100 ms.

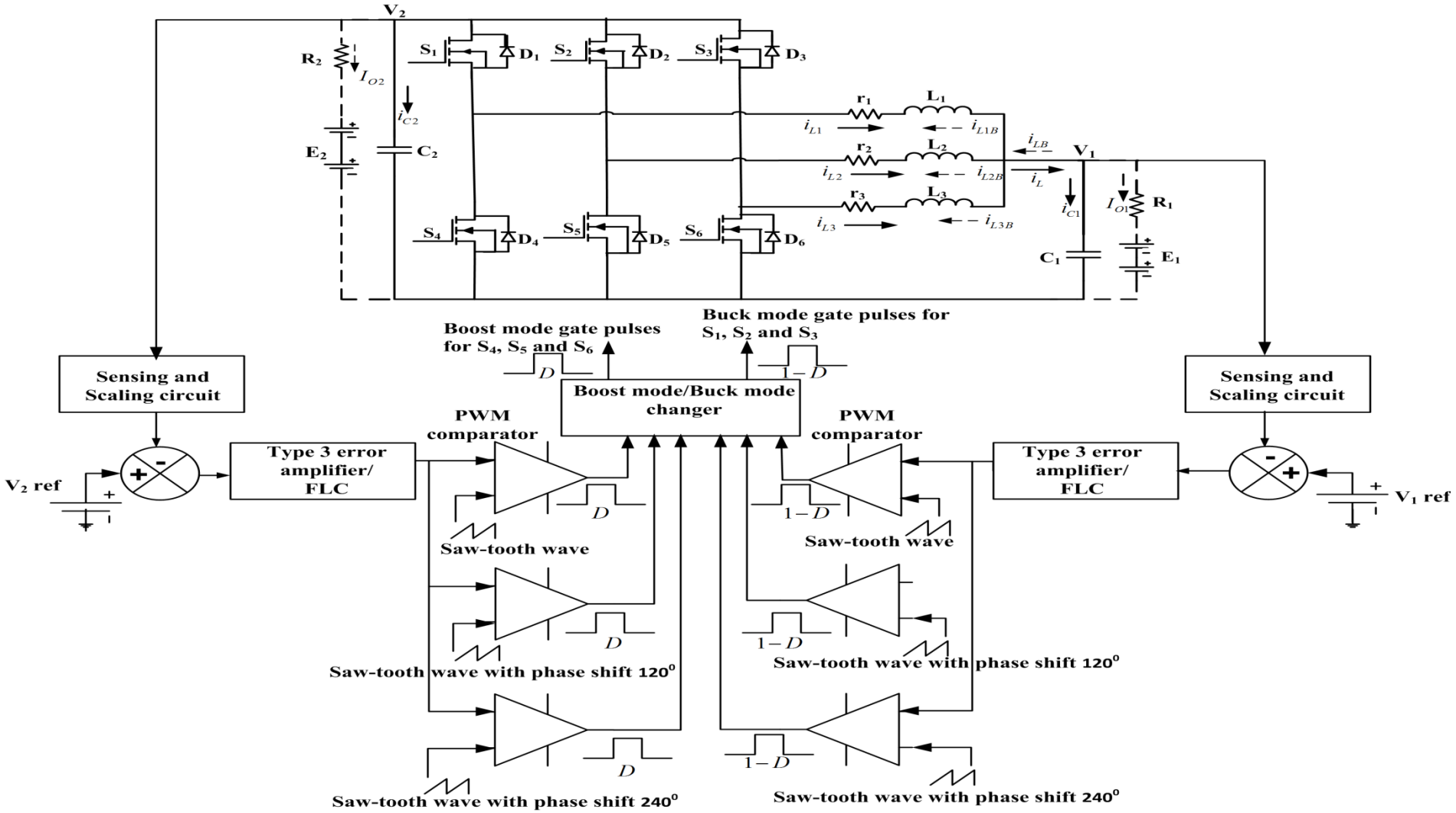


Figure 3.38 Simulation circuit of three-phase IBDDC.

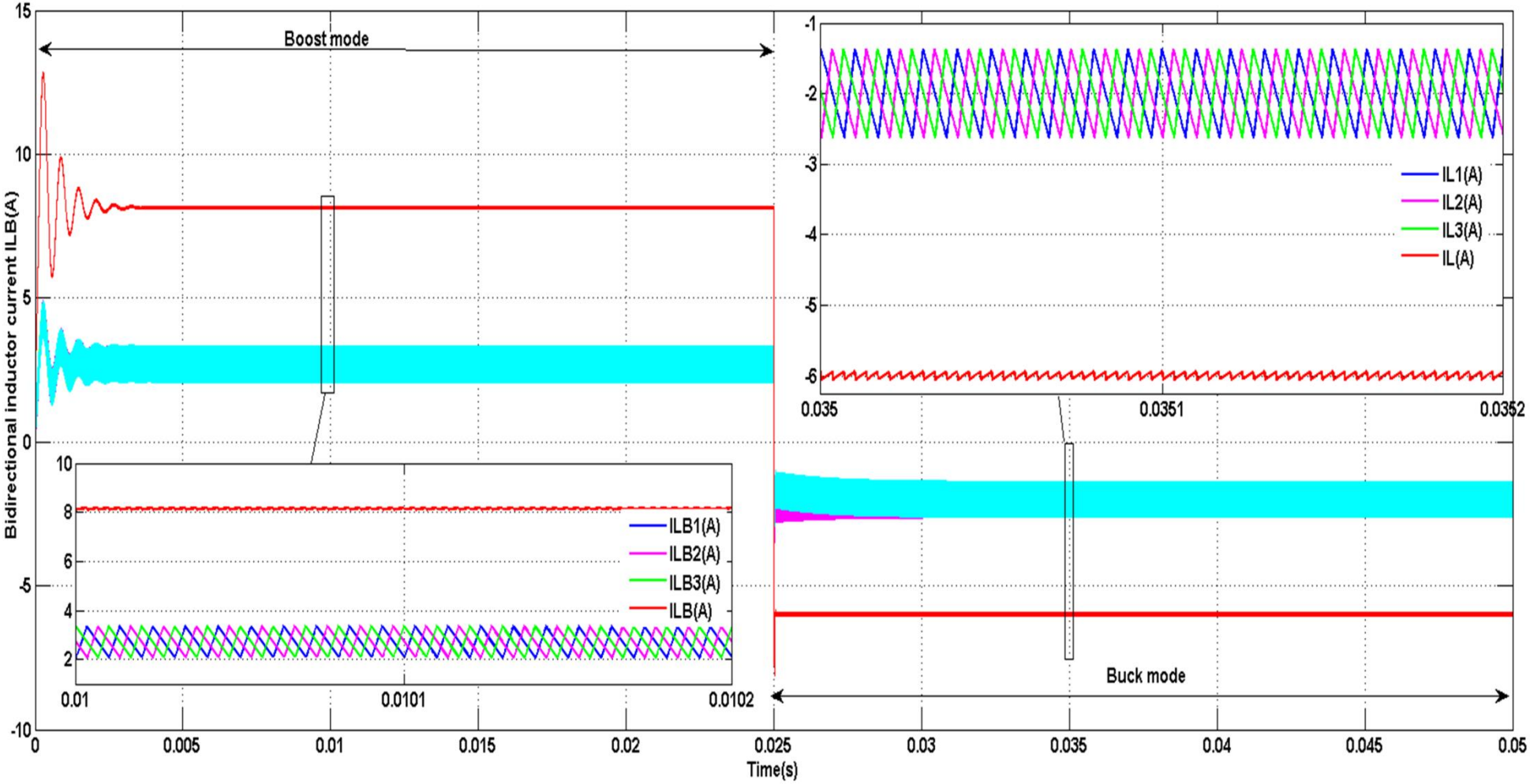


Figure 3.39 Simulation results for bidirectional and individual inductor current of three-phase IBDDC

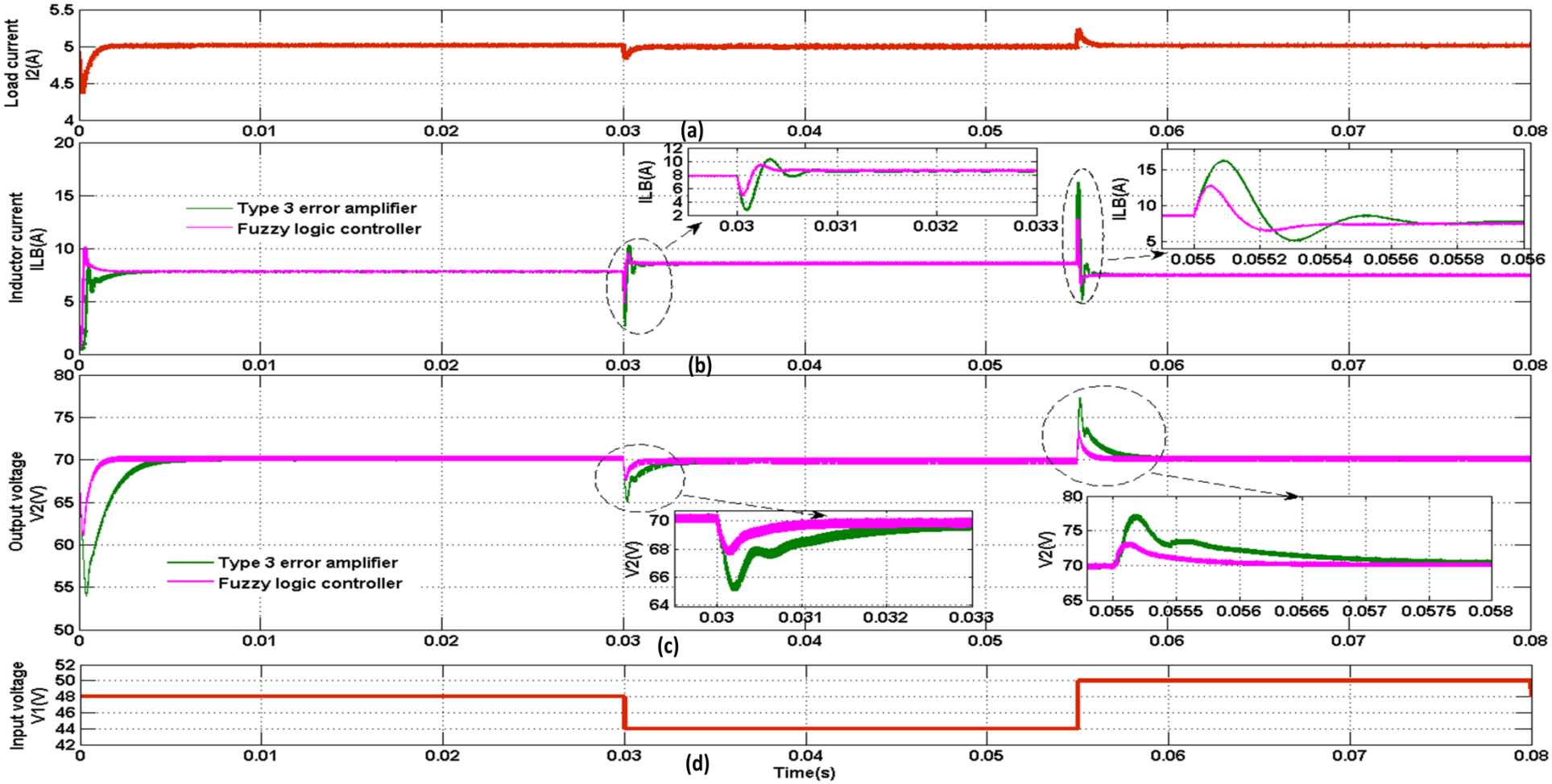


Figure 3.40 Simulation results of three-phase IBDDC in boost mode against input voltage V_1 variation

(a) Load current. (b) Output voltage against input voltage. (c) Inductor current against input voltage. (d) Input voltage variation.

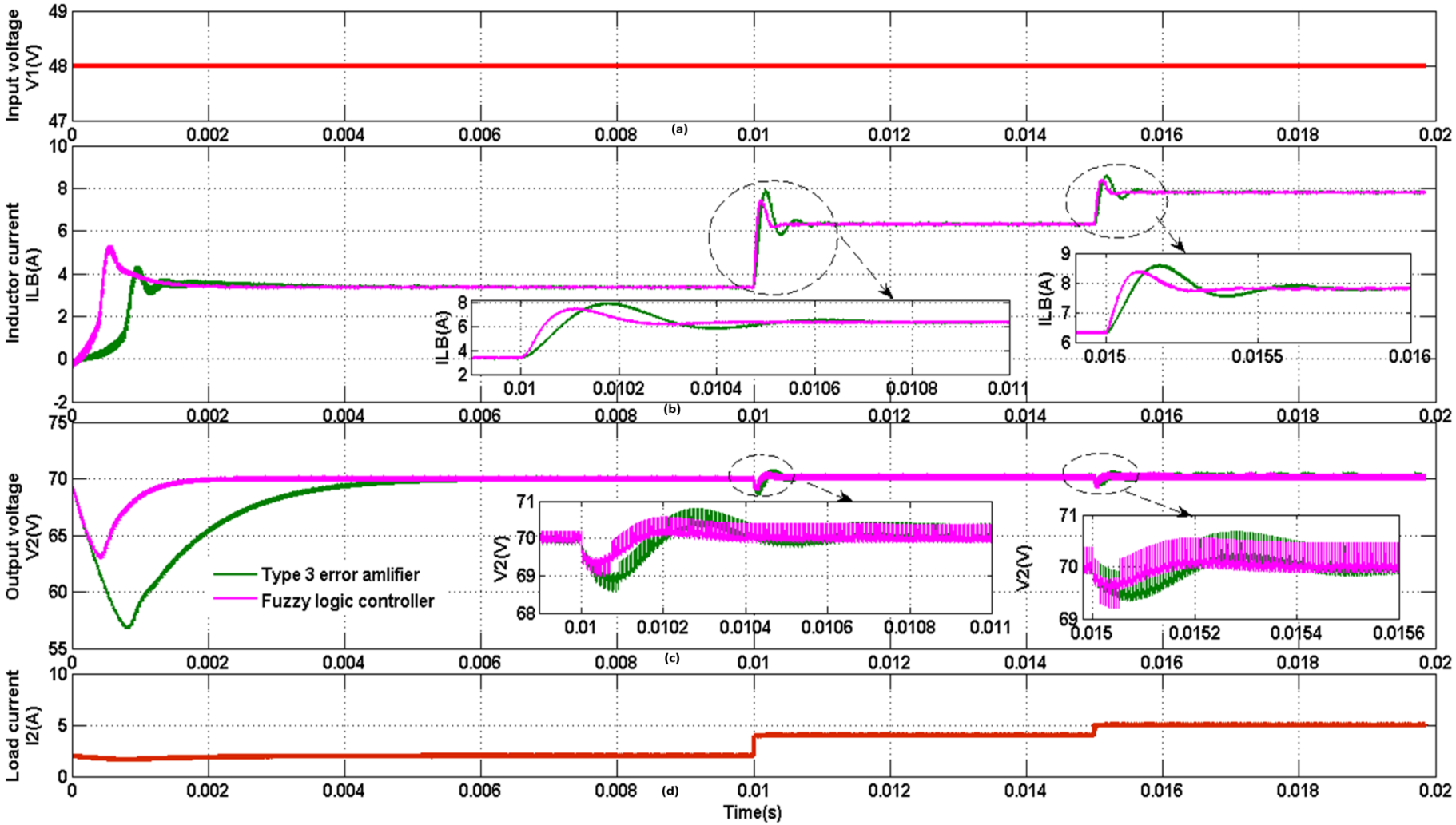


Figure 3.41 Simulation results of three-phase IBDDC in boost mode against load current variation.

(a) Input voltage (b) Inductor current against load current. (c) Output voltage against load current. (d) Load current variation

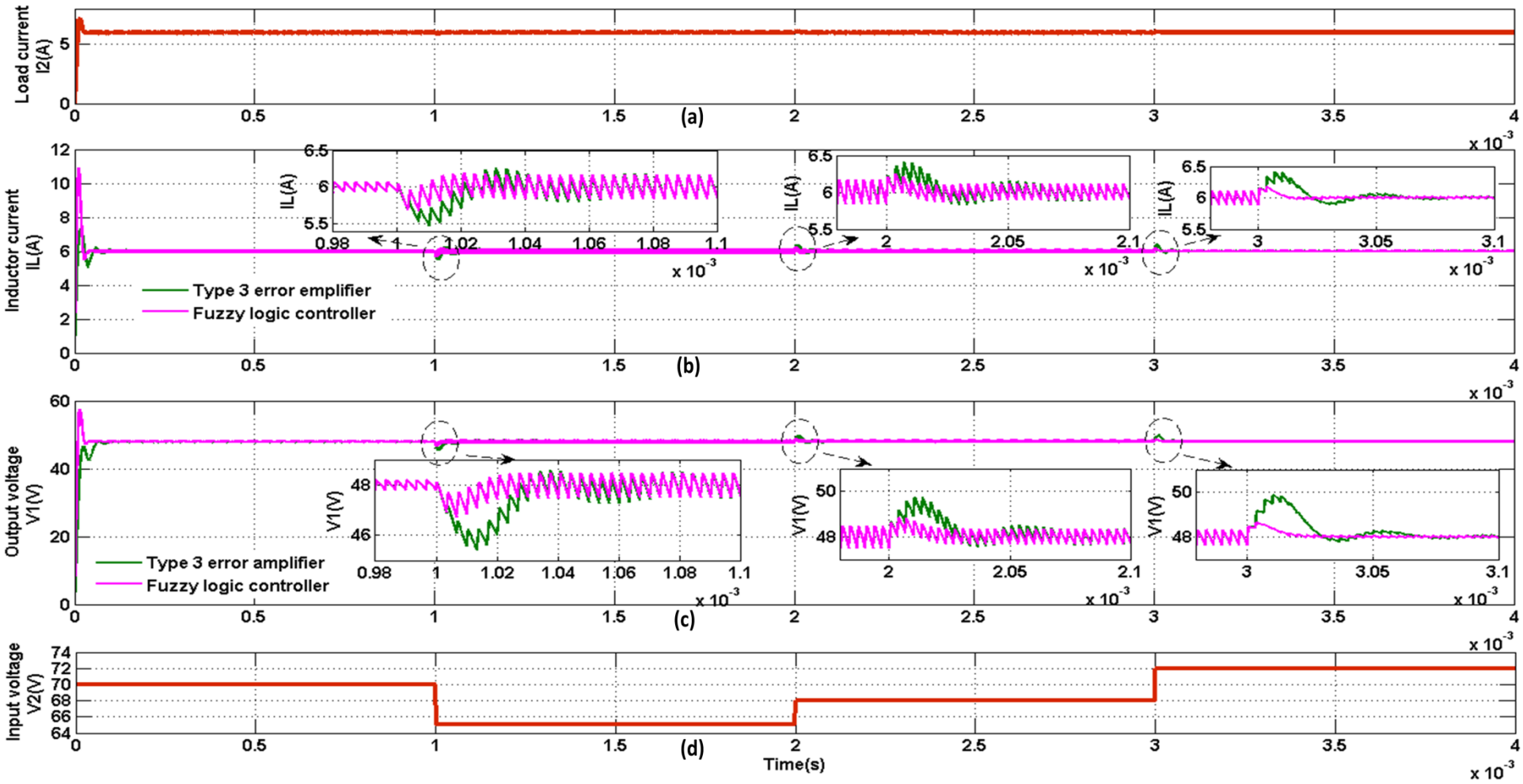


Figure 3.42 Simulation results of three-phase IBDDC in buck mode against input voltage variation.

(a) Load current. (b) Inductor current against input voltage. (c) Output voltage against input voltage. (d) Input voltage variation.

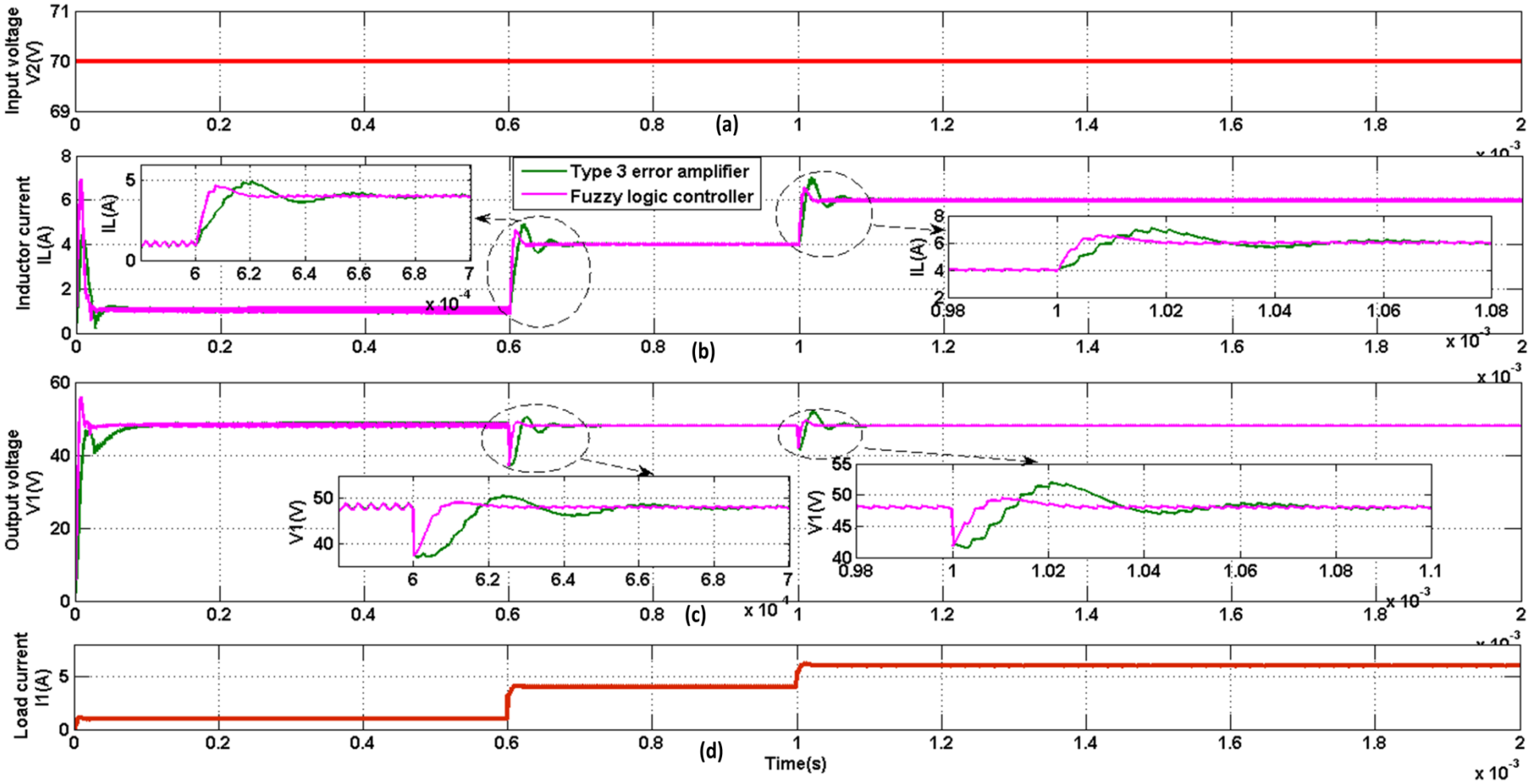


Figure 3.43 Simulation results of three-phase IBDDC in buck mode against load current variation.

(a) Input voltage. (b) Inductor current against load current. (c) Output voltage against load current. (d) Load current variation.

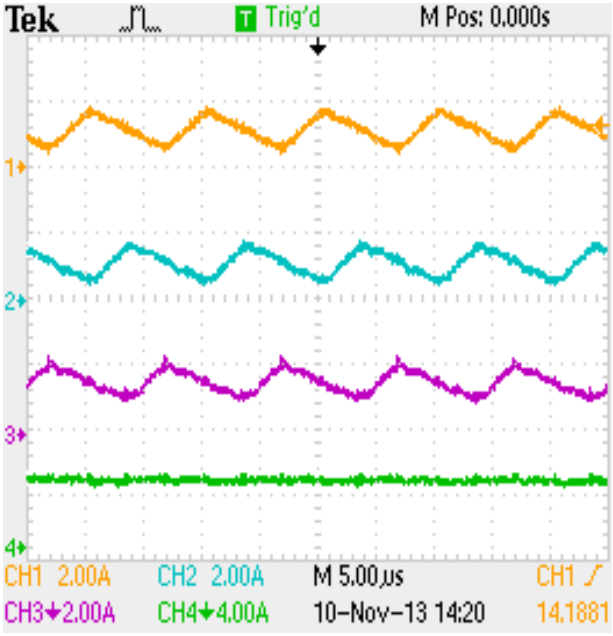
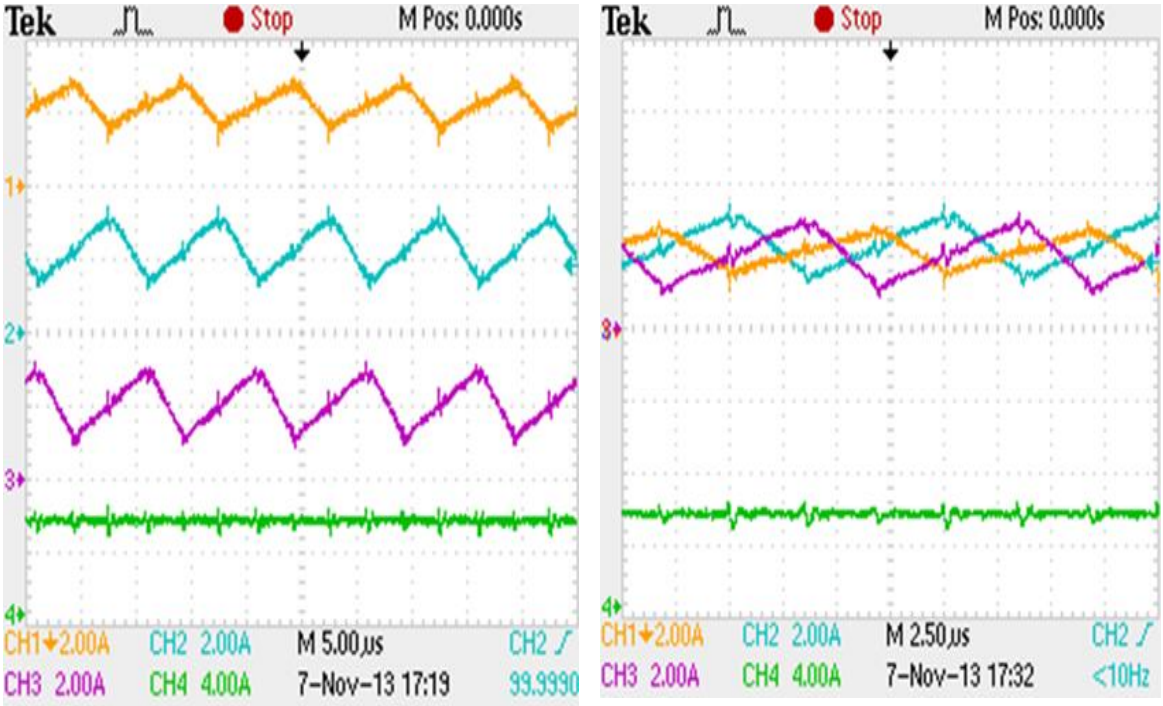


Figure 3.44 Steady state inductor current waveforms of three-phase IBDDC in boost mode.

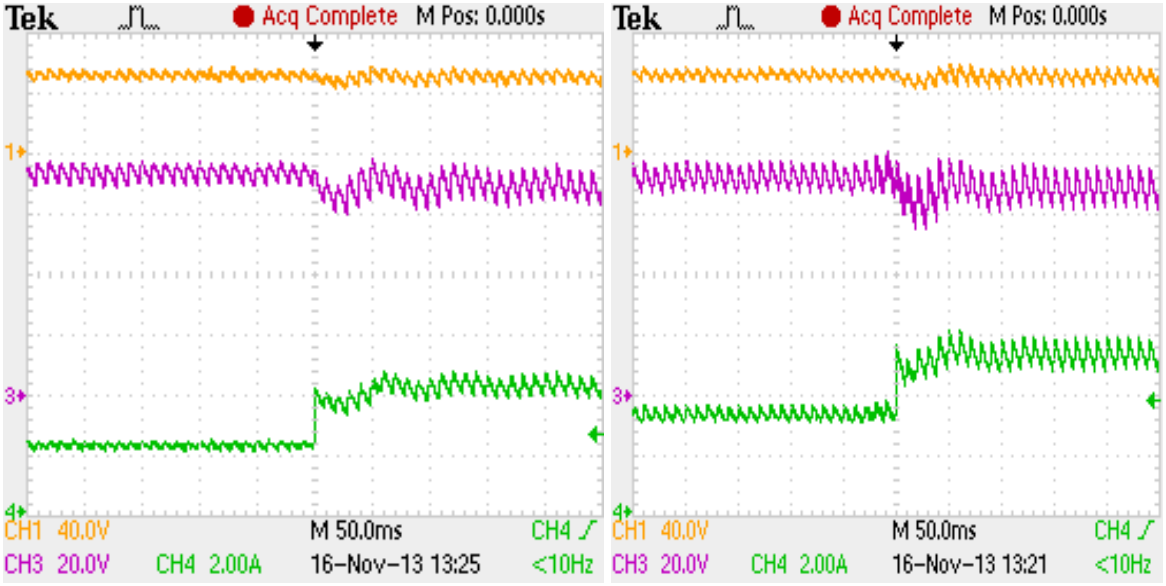
(Ch1- I_{L1B}, Ch2- I_{L2B}, Ch3- I_{L3B}, Ch4- total inductor current I_{LB})



(a) (b)

Figure 3.45 Steady state inductor current waveforms of three-phase IBDDC in buck mode.

(Ch1- I_{L1}, Ch2- I_{L2}, Ch3- I_{L3}, Ch4- total inductor current I_L)



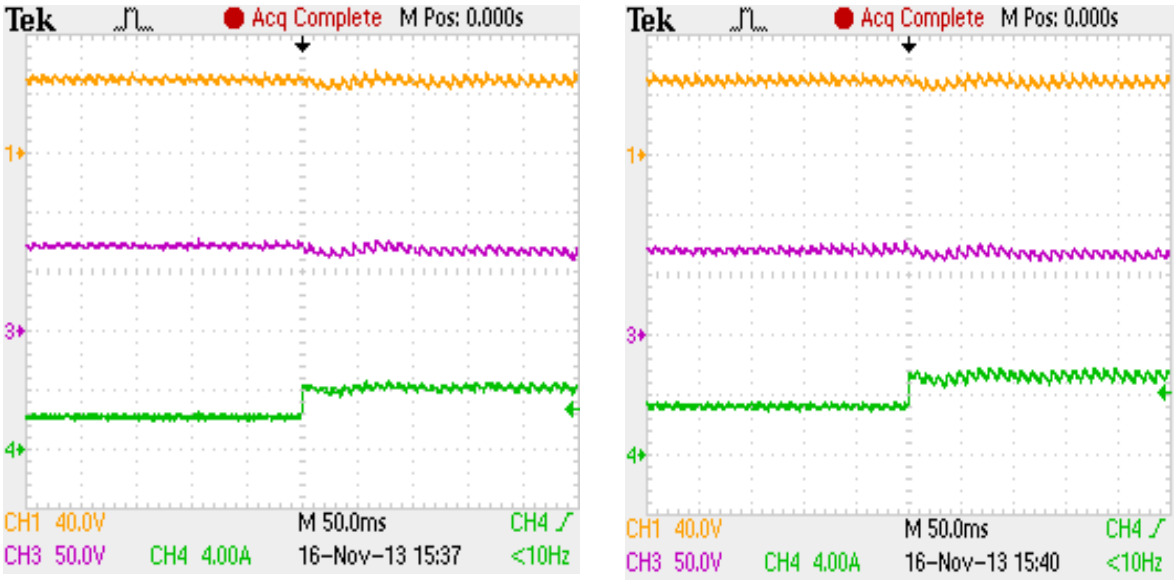
(a) (b)

Figure 3.46 Experimental results of three-phase IBDDC in boost mode using type III EA for different values of load current I_{o2}

(a) Load current varied from 2 A to 4 A. (b) Load current varied from 3 A to 5 A.

(Ch1- input voltage V_1=48 V, Ch3- output voltage V_2, Ch4- load current I_{o2})

Dynamic performances of three-phase IBDDC in boost mode against load current I_{o2} varied from 2 A to 5 A with constant input voltage V_1 of 48 V using FLC is as shown in Figure 3.47.



(a) (b)

Figure 3.47 Experimental results of three-phase IBDDC in boost mode using FLC for different values of load current I_{o2}

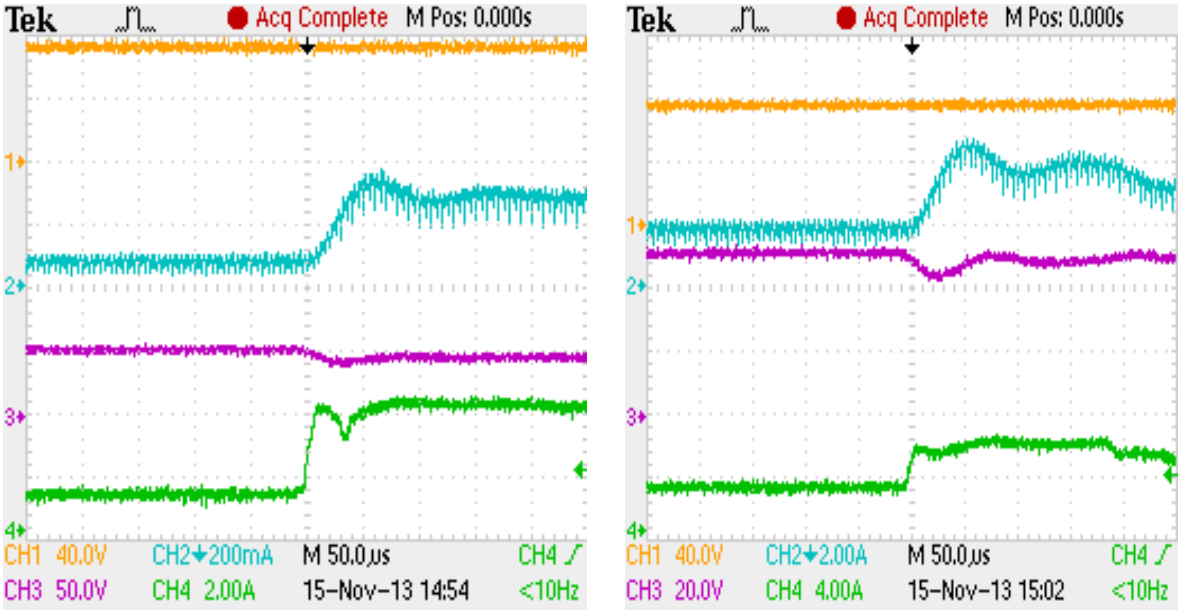
(a) Load current varied from 2 A to 4 A. (b) Load current varied from 3 A to 5 A.

(Ch1- input voltage V_1=48 V, Ch3- output voltage V_2, Ch4- load current I_{o2})

In Figure 3.47, the performance of three-phase IBDDC in boost when the sudden step change in load current I_{o2} (Ch4) varied from 2 A to 4 A and load current I_{o2} (Ch4) varied from 3 A to 5 A are shown in Figure 3.47(a) and Figure 3.47(b) respectively, with constant input voltage V_1 (Ch1) of 48 V, FLC provides steady state output voltage V_2 (Ch3) of 70 V within 25 ms.

Practical waveforms of three-phase IBDDC in boost mode against load current I_{o2} varied from 2 A to 5 A with constant input voltage V_1 of 48 V to meet the desired output voltage V_2 of 70 V using type 3 error amplifier and FLC are closely matching with the simulated result.

Dynamic performances of three-phase IBDDC in buck mode against load current I_{o1} varied from 1 A to 5 A with constant input voltage V_2 of 70 V using type 3 error amplifier are shown in Figure 3.48.



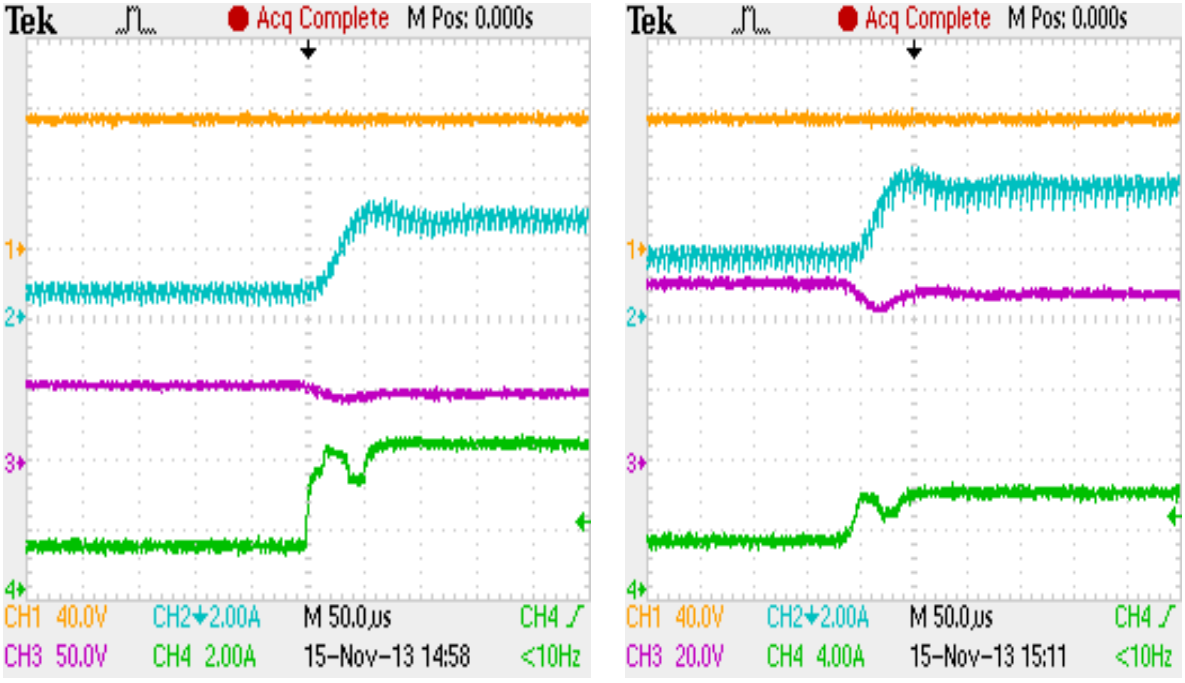
(a) (b)

Figure 3.48 Experimental results of three-phase IBDDC in buck mode using type III EA for different values of load current I_{o1}
(a) Load current varied from 1.5 A to 3.5 A. (b) Load current varied from 3 A to 6 A.
(Ch1- input voltage V_2, Ch2- inductor current I_L, Ch3- output voltage V_1, Ch4- load current)

In Figure 3.48, the performance of three-phase IBDDC in buck mode when the sudden step change in load current I_{o1} (Ch4) varied from 1.5 A to 3.5 A and load current I_{o1} (Ch4) varied from 3 A to 5 A are shown in Figure 3.48(a) and Figure 3.48(b) respectively , with constant input voltage V_1 (Ch1) of 70 V, type III error amplifier provides steady state output voltage V_2 (Ch3) of 48 V within 100 µs.

Dynamic performances of three-phase IBDDC in buck mode against load current I_{o1} varied from 1 A to 7 A with constant input voltage V_2 of 70 V using FLC is as shown in Figure 3.49.

In Figure 3.49, the performance of three-phase IBDDC in buck mode when the sudden step change in load current I_{o1} (Ch4) varied from 1 A to 4 A and load current I_{o1} (Ch4) varied from 2.5 A to 5 A are shown in Figure 3.49(a) and Figure 3.49(b) respectively , with constant input voltage V_2 (Ch1) of 70 V, FLC provides steady state output voltage V_1 (Ch3) of 48 V within 50 µs.



(a) (b)

Figure 3.49 Experimental results of three-phase IBDDC in buck mode using FLC for different values of load current I_{o1}
(a) Load current varied from 1.5 A to 3.5 A. (b) Load current varied from 3 A to 6 A.
(Ch1- input voltage V_2, Ch2- inductor current I_L , Ch3- output voltage V_1 , Ch4- load current)

Practical waveforms of three-phase IBDDC in buck mode against load current I_{o1} varied from 1.5 A to 6 A with constant input voltage V_2 of 70 V, the desired output voltage V_1 of 48 V is obtained using type III compensator and FLC, and they are closely matching with the simulated result.

3.11 Conclusion

A comprehensive analysis, design, dynamic analysis using state space averaging technique of three-phase interleaved bidirectional dc-dc converter has been carried out. Design of type 3 error amplifier controller and design of fuzzy logic controller for three-phase

IBDDC has been carried out, and performances of type 3 error amplifier on three-phase IBDDC are also carried out.

From the analysis, design optimisation, modelling and design of controller for three-phase interleaved bidirectional dc-dc converter, the following conclusions are drawn

(i) With the help of type III error amplifier for both boost mode and buck mode of three-phase IBDDC, phase margin of 60^0 and gain margin of 11.1 dB are obtained corresponds to cross over frequency.

(ii) Type III error amplifier make the three-phase IBDDC as stable against the line voltage or load current change occurs.

From the simulation and experimentation of three-phase IBDDC, the following conclusions are drawn

(i) Design and implementation of three-phase IBDDC with hard switching is tested in both boost mode and buck mode using type III error amplifier and FLC against load current changes.

(ii) Experimental results indicate FLC with rule base provide the less oscillation during steady state and better transient response during load transients.

4.1 Conclusions

A comprehensive analysis, design, dynamic analysis using state space averaging technique of conventional bidirectional dc-dc converter and three-phase IBDDC has been carried out. Design of type 3 error amplifier controller for BDDC in boost mode and design of PID controller for BDDC in buck mode has been carried out, and performance of type 3 error amplifier for boost mode and PID controller for buck mode of conventional BDDC are also carried out.

Design of type 3 error amplifier, design of FLC for three-phase IBDDC in both boost and buck mode has been carried out, and performance of type 3 error amplifier and FLC for three-phase IBDDC are also carried out.

From the analysis, design optimisation, modelling, design of controller, simulation and experimentation on both conventional BDDC and three-phase IBDDC, the following conclusions are drawn

- Analytical expression for steady state, and small signal model of both BDDC and three-phase IBDDC using state space averaging technique have been derived to illustrate the behaviour of converter.
- The closed loop stability analysis of the conventional BDDC and three-phase IBDDC have been extensively studied, results show that significant improvement in transient dynamic responses using voltage mode controller.
- In order to achieve bidirectional operation, only common inductor is enough to operate BDDC in both boost and buck mode.
- In order to achieve bidirectional operation, only common inductor is enough to operate BDDC in both boost and buck mode.
- Optimum selection of inductor in CCM gives the best dynamic performance of the converter for input voltage and output load current variation.
- Optimal design of converter elements are selected for effective utilization of the conventional BDDC and three-phase IBDDC operates either in boost mode or in buck mode.
- Based on duty ratio of the system specification, optimal selection of number of phases in interleaved operation is chosen to minimize ripple inductor current and output voltage ripple.

- Design and implementation of 350 W BDDC is being tested in both boost mode using type 3 compensator for boost mode and PID controller for buck mode against load current changes.
- Experimental results indicate type III error amplifier for boost mode and PID controller for buck mode provide the less oscillation during steady state and faster transient response during load transients.
- Optimistic selection of snubber circuit minimizes the parasitic impedance effect at 100 kHz operation of conventional BDDC and three-phase IBDDC.
- Design and implementation of 350 W three-phase IBDDC is also tested in both boost mode and buck mode using type III error amplifier and FLC against load current changes.
- Experimental results indicate FLC with rule base provide the less oscillation during steady state and faster transient response during load transients.
- Simulation results are validated with experimental results.
- Three-phase IBDDC with minimum number of switching devices can be successfully operate to minimize ripple in input current and output voltage. Three-phase IBDDC can be used in aircraft power supply, renewable source fed converter, and the system with high power applications.

4.2 Future Scope

Following directions are identified for future research works in this area are;

1. Further investigation of different control techniques is required to improve the performance of the BDDC and IBDDC.
2. Further improvement can be made for the BDDC by designing the PID controller using genetic optimization techniques and prototype of BDDC can be developed using DSP/ FPGA.
3. Equal sharing current and phase shifting in IBDDC can be achieved by sensing current in all the phases of IBDDC, it can be developed and implemented on DSP/FPGA.
4. Unified digital and artificial intelligent controller can be developed to achieve fast dynamic response instead of individual controller for improved response.
5. Silicon carbide MOSFETs can be used as switching device in high power applications in future research.

6. Coupled inductor bidirectional dc-dc converter topology with artificial intelligence techniques is also suggested to develop prototype of IBDDC to avoid use of individual inductors.
7. Direct design procedure can be preferred over the indirect design procedure for design of digital controller.

PUBLICATIONS FROM THE WORK

1. Guruswamy K P., and S. P. Singh., "Modeling and Performance Control of Interleaved Bidirectional DC-DC Converter" *IETE Technical Review**: Resubmitted.***
2. Guruswamy K P., and S. P. Singh., "Modeling and Control of Bidirectional DC-DC Converter" *Journal of Power Electronics; **Under Review***.

BIBLIOGRAPHY

[1] S. B. Dewan and A. Straughen, Power semiconductor circuits: Wiley, 1975.

[2] D. M. Sable, F. C. Lee, and B. H. Cho, "A zero-voltage-switching bidirectional battery charger/discharger for the NASA EOS satellite," in Applied Power Electronics Conference and Exposition, pp. 614-621, 1992.

[3] L. Jih-Sheng and D. J. Nelson, "Energy Management Power Converters in Hybrid Electric and Fuel Cell Vehicles," Proceedings of the IEEE, vol. 95, pp. 766-777, 2007.

[4] D. D. S. Oliveira and I. Barbi, "A three-phase ZVS PWM DC/DC converter with asymmetrical duty cycle for high power applications," IEEE Transactions on Power Electronics, vol. 20, pp. 370-377, 2005.

[5] L. Zhiling and R. Xinbo, "Control strategy of bi-directional DC/DC converter for a novel stand-alone photovoltaic power system," in IEEE Vehicle Power and Propulsion Conference, pp. 1-6, 2008.

[6] T. M. U. Ned Mohan, William P. Robbins, "Power electronics converters, applications and design," 3rd ed: John Wiley, pp. 802, 2008.

[7] J. B. V. Reddy, G. Bhuvaneswari, and B. Singh, "A Single DC-DC Converter Based Multiple Output SMPS with Fully Regulated and Isolated Outputs," in 2005 Annual IEEE India Conference - Indicon, pp. 585-589, 2005.

[8] P. C. Todd, "Snubber circuits: theory, design and application," in Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM-900. Unitrode, 1993.

[9] L. Balogh, "Design and application guide for high speed MOSFET gate drive circuits," in Texas Instruments/Unitrode Corporation,Power Supply Design Seminar, SEM, 2001.

[10] O. Garcia, P. Zumel, A. de Castro, and A. Cobos, "Automotive DC-DC bidirectional converter made with many interleaved buck stages," IEEE Transactions on Power Electronics, vol. 21, pp. 578-586, 2006.

[11] N. Liqin, D. J. Patterson, and J. L. Hudgins, "High Power Current Sensorless Bidirectional 16-Phase Interleaved DC-DC Converter for Hybrid Vehicle Application," IEEE Transactions on Power Electronics, vol. 27, pp. 1141-1151, 2012.

[12] S. Augustine, M. K. Mishra, and N. Lakshminarasamma, "Circulating current minimization and current sharing control of parallel boost converters based on Droop Index," in IEEE International Symposium on Diagnostics for Electric Machines, Power Electronics and Drives (SDEMPED), pp. 454-460, 2013.

[13] S. Augustine, M. K. Mishra, and N. Lakshminarasamma, "An improved droop control algorithm for load sharing and circulating current control for parallel DC-DC converters

in standalone DC microgrid," in Annual International Conference on Emerging Research Areas: Magnetics, Machines and Drives (AICERA/iCMMD), pp. 1-6, 2014.

[14] G.-J. Su and L. Tang, "A multiphase, modular, bidirectional, triple-voltage DC–DC converter for hybrid and fuel cell vehicle power systems," IEEE Transactions on Power Electronics, vol. 23, pp. 3035-3046, 2008.

[15] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," IEEE Transactions on Industrial Electronics, vol. 58, pp. 1239-1250, 2011.

[16] Z. Ouyang, Z. Zhang, O. C. Thomsen, and M. A. Andersen, "Planar-integrated magnetics (PIM) module in hybrid bidirectional dc–dc converter for fuel cell application," IEEE Transactions on Power Electronics, vol. 26, pp. 3254-3264, 2011.

[17] X. Huang, X. Wang, T. Nergaard, J.-S. Lai, X. Xu, and L. Zhu, "Parasitic ringing and design issues of digitally controlled high power interleaved boost converters," IEEE Transactions on Power Electronics, vol. 19, pp. 1341-1352, 2004.

[18] R. D. Middlebrook and S. ĆUk, "A general unified approach to modelling switching-converter power stages," International Journal of Electronics, vol. 42, pp. 521-550, 1977.

[19] R. W. Erickson and D. Maksimovic, Fundamentals of power electronics: Springer, 2001.

[20] M. K. Kazimierczuk, Pulse-width modulated DC-DC power converters: John Wiley & Sons, 2008.

[21] H. D. Venable, "The K factor: A new mathematical tool for stability analysis and synthesis," in Proc. Powercon, pp. H1-1, 1993.

[22] G.-Y. Choe, H.-S. Kang, B.-K. Lee, and W.-Y. Lee, "Design consideration of interleaved converters for fuel cell applications," in ICEMS. International Conference on Electrical Machines and Systems, pp. 238-243, 2007.

[23] H. Xudong, T. Nergaard, L. Jih-Sheng, X. Xingyi, and L. Zhu, "A DSP based controller for high-power interleaved boost converters," in Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition, vol. 1, pp. 327-333, 2003.

[24] L. Zadeh, "Fuzzy Sets," Information and Control, vol. 8, pp. 338-353, 1965.

[25] C. C. Lee, "Fuzzy logic in control systems: fuzzy logic controller. II," IEEE Transactions on Systems, Man and Cybernetics, vol. 20, pp. 419-435, 1990.

[26] T. Gupta, R. R. Boudreaux, R. M. Nelms, and J. Y. Hung, "Implementation of a fuzzy controller for DC-DC converters using an inexpensive 8-b microcontroller," IEEE Transactions on Industrial Electronics, vol. 44, pp. 661-669, 1997.

[27] F. Caricchi, F. Crescimbini, G. Noia, and D. Pirolo, "Experimental study of a bidirectional DC-DC converter for the DC link voltage control and the regenerative braking in PM motor drives devoted to electrical vehicles," in Ninth Annual Applied Power Electronics Conference and Exposition, APEC '94, vol. 1, pp. 381-386, 1994.

[28] M. A. Sofla and Wang, L, “Control of DC-DC Bidirectional Converters for Interfacing Batteries in Microgrids.” in IEEE/PES Power Systems Conference and Exposition, pp. 1-6, 2011.

[29] P. Jose and N. Mohan, "A novel ZVS bidirectional Cuk converter for Dual Voltage Systems in Automobiles," in IEEE 35th Annual Power Electronics Specialists Conference, PESC 04, vol. 1, pp. 343-349, 2004.

[30] K. In-Dong, P. Seong-Hwan, A. Jin-Woo, N. Eui-Cheol, and K. Jong-Sun, "New Bidirectional ZVS PWM Sepic/Zeta DC-DC Converter," in IEEE International Symposium on Industrial Electronics, pp. 555-560, 2007.

[31] B. Ray, "Single-cycle resonant bidirectional DC/DC power conversion," in Eighth Annual Applied Power Electronics Conference and Exposition, APEC '93, pp. 44-50, 1993.

[32] J. Majo, L. Martinez, A. Poveda, L. G. de Vicuna, F. Guinjoan, A. F. Sanchez, M. Valentin, and J. C. Marpinard, "Large-signal feedback control of a bidirectional coupled-inductor Cuk converter," IEEE Transactions on Industrial Electronics, vol. 39, pp. 429-436, 1992.

[33] S. Busquets-Monge, S. Alepuz, and J. Bordonau, "A Bidirectional Multilevel Boost-Buck DC-DC Converter," IEEE Transactions on Power Electronics, vol. 26, pp. 2172-2183, 2011.

[34] Y. S. Lee and Y. Y. Chiu, "Zero-current-switching switched-capacitor bidirectional DC-DC converter," IEE Proceedings-Electric Power Applications, vol. 152, pp. 1525-1530, 2005.

[35] S. Waffler and J. W. Kolar, "A Novel Low-Loss Modulation Strategy for High-Power Bidirectional Buck+Boost Converters," IEEE Transactions on Power Electronics, vol. 24, pp. 1589-1599, 2009.

[36] C. Sreekumar and V. Agarwal, "Hybrid control approach for the output voltage regulation in buck type DC-DC converter," IET Electric Power Applications, vol. 1, pp. 897-906, 2007.

[37] P. K. Peter, P. Sharma, and V. Agarwal, "Switched capacitor DC-DC converter based current equalization scheme for maximum power extraction from partially shaded PV modules without bypass diodes," in 38th IEEE Photovoltaic Specialists Conference (PVSC), pp. 001422-001427, 2012.

[38] D. J. Perreault and J. G. Kassakian, "Distributed interleaving of paralleled power converters," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 44, pp. 728-734, 1997.

[39] Z. Junhong, K. Rae-Young, and L. Jih-Sheng, "High-Power Density Design of a Soft-Switching High-Power Bidirectional DC-DC Converter," in 37th IEEE Power Electronics Specialists Conference, PESC '06., pp. 1-7, 2006.

[40] D. P. Urciuoli and C. W. Tipton, "Development of a 90 kW bi-directional DC-DC converter for power dense applications," in Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, APEC '06., pp. 4-9, 2006.

[41] H. Dong-Hyun, P. Nam-Ju, L. Kui-Jun, L. Dong-Gyu, and H. Dong-Seok, "Interleaved Bidirectional DC-DC Converter for Automotive Electric Systems," in IEEE Industry Applications Society Annual Meeting, IAS '08., pp. 1-5, 2008.

[42] H. Sung Pil, L. Jung Hyo, H. Jung Pill, C. Jun Hyuk, and W. Chung Yuen, "Two phase interleaved bidirectional DC-DC converter for electric vehicle using variable DC-link voltage," in IEEE Vehicle Power and Propulsion Conference (VPPC), pp. 748-752, 2012.

[43] W. Pit-Leong, X. Peng, B. Yang, and F. C. Lee, "Performance improvements of interleaving VRMs with coupling inductors," IEEE Transactions on Power Electronics, vol. 16, pp. 499-507, 2001.

[44] C. Junyoung, C. Honnyong, and K. Heung-Geun, "Analysis and design of two-phase zero-voltage switching bidirectional dc-dc converter using coupled inductor," in IEEE International Conference on Industrial Technology (ICIT), pp. 301-306, 2014.

[45] D. S. Oliveira and I. Barbi, "A three-phase ZVS PWM DC/DC converter with asymmetrical duty cycle associated with a three-phase version of the hybridge rectifier," IEEE Transactions on Power Electronics, vol. 20, pp. 354-360, 2005.

[46] C. Rudolph, "Hybrid drive system of an industrial truck using a three-phase DC-DC converter feeding ultra-capacitors," in 13th European Conference on Power Electronics and Applications, EPE '09., pp. 1-10, 2009.

[47] S. Grunau, M. Fox, and F. W. Fuchs, "Comparison of a three and four phase interleaved bidirectional DC/DC-converter for the operation in an energy storage system in wind turbines," in 15th International Power Electronics and Motion Control Conference (EPE/PEMC), pp. DS3d.6-1-DS3d.6-8, 2012.

[48] Y. Wensong and L. Jih-Sheng, "Ultra high efficiency bidirectional dc-dc converter with multi-frequency pulse width modulation," in Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2008., pp. 1079-1084, 2008.

[49] L. Yuang-Shung, K. Yi-Pin, C. Ming-Wang, and L. Li-Jen, "Multiphase Zero-Current Switching Bidirectional Converters and Battery Energy Storage Application," IEEE Transactions on Power Electronics, vol. 28, pp. 3806-3815, 2013.

[50] F. Krismer, J. Biela, and J. W. Kolar, "A comparative evaluation of isolated bi-directional DC/DC converters with wide input and output voltage range," in Fourtieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, vol. 1, pp. 599-606, 2005.

[51] K. Venkatesan, "Current mode controlled bidirectional flyback converter," in 20th Annual IEEE Power Electronics Specialists Conference, PESC '89, vol. 2, pp. 835-842, 1989.

[52] H. S. H. Chung, C. Wai-leung, and K. S. Tang, "A ZCS bidirectional flyback DC/DC converter," IEEE Transactions on Power Electronics, vol. 19, pp. 1426-1434, 2004.

[53] C. Gang, L. Yim-Shu, S. Y. R. Hui, X. Dehong, and W. Yousheng, "Actively clamped bidirectional flyback converter," IEEE Transactions on Industrial Electronics, vol. 47, pp. 770-779, 2000.

[54] Z. Fanghua and Y. Yangguang, "Novel Forward-Flyback Hybrid Bidirectional DC-DC Converter," IEEE Transactions on Industrial Electronics, vol. 56, pp. 1578-1584, 2009.

[55] L. Hui and F. Z. Peng, "Modeling of a new ZVS bi-directional dc-dc converter," IEEE Transactions on Aerospace and Electronic Systems, vol. 40, pp. 272-283, 2004.

[56] B. R. Lin, C. L. Huang, and Y. E. Lee, "Asymmetrical pulse-width modulation bidirectional DC-DC converter," IET Power Electronics, vol. 1, pp. 336-347, 2008.

[57] M. Jain, M. Daniele, and P. K. Jain, "A bidirectional DC-DC converter topology for low power application," IEEE Transactions on Power Electronics, vol. 15, pp. 595-606, 2000.

[58] C. Mi, H. Bai, C. Wang, and S. Gargies, "Operation, design and control of dual H-bridge-based isolated bidirectional DC-DC converter," IET Power Electronics, vol. 1, pp. 507-517, 2008.

[59] B. Hua, N. Ziling, and C. C. Mi, "Experimental Comparison of Traditional Phase-Shift, Dual-Phase-Shift, and Model-Based Control of Isolated Bidirectional DC-DC Converters," IEEE Transactions on Power Electronics, vol. 25, pp. 1444-1449, 2010.

[60] W. Tsai-Fu, C. Yung-Chu, Y. Jeng-Gung, and K. Chia-Ling, "Isolated Bidirectional Full-Bridge DC-DC Converter With a Flyback Snubber," IEEE Transactions on Power Electronics, vol. 25, pp. 1915-1922, 2010.

[61] X. Yanhui, S. Jing, and J. S. Freudenberg, "Power Flow Characterization of a Bidirectional Galvanically Isolated High-Power DC/DC Converter Over a Wide Operating Range," IEEE Transactions on Power Electronics, vol. 25, pp. 54-66, 2010.

[62] R. T. Naayagi, A. J. Forsyth, and R. Shuttleworth, "High-Power Bidirectional DC-DC Converter for Aerospace Applications," IEEE Transactions on Power Electronics, vol. 27, pp. 4366-4379, 2012.

[63] Z. Zhe, O. Ziwei, O. C. Thomsen, and M. A. E. Andersen, "Analysis and Design of a Bidirectional Isolated DC-DC Converter for Fuel Cells and Supercapacitors Hybrid System," IEEE Transactions on Power Electronics, vol. 27, pp. 848-859, 2012.

[64] S. Jalbrzykowski, A. Bogdan, and T. Citko, "A Dual Full-Bridge Resonant Class-E Bidirectional DC-DC Converter," IEEE Transactions on Industrial Electronics, vol. 58, pp. 3879-3883, 2011.

[65] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," IEEE Transactions on Industry Applications, vol. 27, pp. 63-73, 1991.

[66] Z. Zhe, O. C. Thomsen, and M. A. E. Andersen, "Optimal Design of a Push-Pull-Forward Half-Bridge (PPFHB) Bidirectional DC-DC Converter With Variable Input Voltage," IEEE Transactions on Industrial Electronics, vol. 59, pp. 2761-2771, 2012.

[67] H. Daneshpajooh, A. Bakhshai, and P. Jain, "Modified dual active bridge bidirectional DC-DC converter with optimal efficiency," in Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1348-1354, 2012.

[68] B. Singh, S. Singh, and G. Bhuvaneswari, "Boost full bridge DC-DC converter based modular converter for Telecom Power Supplies," in IEEE Fifth Power India Conference, pp. 1-5, 2012.

[69] S. Yujin and P. N. Enjeti, "A new soft switching technique for bi-directional power flow, full-bridge DC-DC converter," in 37th IAS Annual Meeting. Conference Record of the Industry Applications Conference, vol. 4, pp. 2314-2319, 2002.

[70] M. Hong, Y. Liangbin, W. Caisheng, and I. Batarseh, "Analysis of Inductor Current Sharing in Nonisolated and Isolated Multiphase dc-dc Converters," IEEE Transactions on Industrial Electronics, vol. 54, pp. 3379-3388, 2007.

[71] C. Shih-Ming, L. Tsorng-Juu, and H. Yong-Hong, "A isolated bidirectional interleaved flyback converter for battery backup system application," in IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1328-1331, 2013.

[72] J. Hyunsik and C. Hanju, "Parallel operation of three-phase bi-directional isolated interleaved DC-DC converters for battery test system," in Twenty-Ninth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1584-1589, 2014.

[73] C. Hanju, C. Jungwan, K. Woojung, and V. Blasko, "A New Bi-directional Three-phase Interleaved Isolated Converter with Active Clamp," in Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2009., pp. 1766-1772, 2009.

[74] Z. Haihua, D. Tran, S. Siew Tuck, and A. M. Khambadkone, "Interleaved bi-directional Dual Active Bridge DC-DC converter for interfacing ultracapacitor in micro-grid application," in IEEE International Symposium on Industrial Electronics (ISIE), pp. 2229-2234, 2010.

[75] L. Wuhua, X. Chi, Y. Hongbing, G. Yunjie, and H. Xiangning, "Analysis, design and implementation of isolated bidirectional converter with winding-cross-coupled inductors for high step-up and high step-down conversion system," IET Power Electronics, vol. 7, pp. 67-77, 2014.

[76] R. W. Erickson and D. Maksimovic, Fundamentals of power electronics: Springer Science & Business Media, 2007.

[77] A. D. Swingler and W. G. Dunford, "Development of a bi-directional DC/DC converter for inverter/charger applications with consideration paid to large signal operation and quasi-linear digital control," in IEEE 33rd Annual Power Electronics Specialists Conference, pesc 02, vol. 2, pp. 961-966, 2002.

[78] Y. Hu, J. Tatler, and Z. Chen, "A bidirectional DC/DC power electronic converter for an energy storage device in an autonomous power system," in The 4th International Power Electronics and Motion Control Conference, IPEMC 2004., vol. 1, pp. 171-176, 2004.

[79] Y. Duan and K. Jin, "Digital controller design for switchmode power converters," in Fourteenth Annual Applied Power Electronics Conference and Exposition, APEC '99., vol. 2, pp. 967-973, 1999.

[80] L. Hui, P. Fang Zheng, and J. S. Lawler, "A natural ZVS medium-power bidirectional DC-DC converter with minimum number of devices," IEEE Transactions on Industry Applications, vol. 39, pp. 525-535, 2003.

[81] L. Hui, L. Danwei, F. Peng, and S. Gui-Jia, "Small Signal Analysis of A Dual Half Bridge Isolated ZVS Bi-directional DC-DC converter for Electrical Vehicle Applications," in IEEE 36th Power Electronics Specialists Conference, PESC '05., pp. 2777-2782, 2005.

[82] S. Lei, S. Liping, X. Dehong, and C. Min, "Optimal design and control of 5kW PWM plus phase-shift (PPS) control bidirectional dc-dc converter," in Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, APEC '06., pp.5-12, 2006.

[83] M. Veerachary, T. Senjyu, and K. Uezato, "Modeling and analysis of interleaved dual boost converter," in IEEE International Symposium on Industrial Electronics, ISIE 2001., vol. 2, pp. 718-722, 2001.

[84] T. Senjyu, M. Veerachary, and K. Uezato, "Steady-state analysis of PV supplied separately excited DC motor fed from IDB converter," Solar Energy Materials and Solar Cells, vol. 71, pp. 493-510, 2002.

[85] N. Jantharamin and L. Zhang, "Analysis of multiphase interleaved converter by using state-space averaging technique," in 6th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology, ECTI-CON 2009., pp. 288-291, 2009.

[86] S. J. Kim and B. H. Cho, "Analysis of Spacecraft Battery Charger Systems," in Proceedings of the 25th Intersociety Energy Conversion Engineering Conference, 1990. IECEC-90., pp. 365-372, 1990.

[87] L. Woo-Cheol, L. Kyuchan, and S. Inyoung, "Current Mode PWM Controller for a 42V/14V bidirectional DC/DC Converter," in 37th IEEE Power Electronics Specialists Conference, PESC '06., pp. 1-6, 2006.

[88] M. Veerachary and A. K. Singh, "Digital controller for fourth-order bi-directional DC-DC converter," in International Conference for Convergence of Technology (I2CT), , pp. 1-5, 2014.

[89] A. G. Perry, F. Guang, L. Yan-Fei, and P. C. Sen, "A Design Method for PI-like Fuzzy Logic Controllers for DC-DC Converter," IEEE Transactions on Industrial Electronics, vol. 54, pp. 2688-2696, 2007.

[90] K. Viswanathan, R. Oruganti, and D. Srinivasan, "Nonlinear function controller: a simple alternative to fuzzy logic controller for a power electronic converter," IEEE Transactions on Industrial Electronics, vol. 52, pp. 1439-1448, 2005.

[91] A. K. S. Bhat, "Analysis and design of a DC/DC converter using square-wave output resonant inverter," IEEE Transactions on Industrial Electronics, vol. 35, pp. 494-501, 1988.

[92] A. K. S. Bhat, "Analysis and design of a modified series resonant converter," IEEE Transactions on Power Electronics, vol. 8, pp. 423-430, 1993.

[93] K. Mandal, S. Banerjee, and C. Chakraborty, "A New Algorithm for Small-Signal Analysis of DC-DC Converters," IEEE Transactions on Industrial Informatics, vol. 10, pp. 628-636, 2014.

[94] S. Kapat, S. Banerjee, and A. Patra, "Modeling and analysis of DC-DC converters under Pulse Skipping Modulation," in IEEE Region 10 Conference TENCON 2008, , pp. 1-6, 2008.

[95] K. Mandal, A. Abusorrah, M. M. A. Hindawi, Y. Al-Turki, D. Giaouris, and S. Banerjee, "Dynamical analysis of single-inductor dual-output DC-DC converters," in IEEE International Symposium on Circuits and Systems (ISCAS2013), pp. 2755-2758, 2013.

[96] M. H. Todorovic, L. Palma, and P. Enjeti, "Design of a wide input range DC-DC converter with a robust power control scheme suitable for fuel cell power conversion," in Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, APEC '04., Vol. 1, pp. 374-379, 2004.

[97] A. I. Pressman, K. H. Billings, and T. Morey, Switching power supply design: McGraw-Hill, 2009.

[98] J. G. Ziegler and N. B. Nichols, "Optimum settings for automatic controllers," trans. ASME, vol. 64, 1942.

[99] J. A. Karl and T. Hägglund, "PID controllers: theory, design and tuning," ed: USA: Instrument Society of America, 1995.

[100] P. Cominos and N. Munro, "PID controllers: recent tuning methods and design to specification," IEE Proceedings - Control Theory and Applications, vol. 149, pp. 46-53, 2002.

[101] L. Umanand and S. Bhat, Design of magnetic components for switched mode power converters: Wiley Eastern, 1992.

[102] http://c2000.spectrumdigital.com/ezf28335/docs/ezdspf28335c_techref

Design of Inductor

Inductor for conventional BDDC can be designed with the following steps [101]

Step1: Inductor value

First step is to find the value of common inductor in the conventional BDDC is $L = 120\mu H$.

Step2: Area product

The Energy to be handled by inductor core is calculated by

$$E = \frac{1}{2} L I_m^2 \tag{A.1}$$

where $I_m = I_{LB} + \frac{\Delta i_{LB}}{2} = 10.582A$ is the maximum value of inductor current. Then energy stored in inductor is calculated as $E = 6.718 \times 10^{-3}$ *joules*

Area product for the inductor core is given by

$$A_P = A_w A_c = \frac{2E}{K_w K_c J B_m} \tag{A.2}$$

where $K_w = 0.6$, $K_c = 1$(for square wave input), $J = 3A/mm^2$, and $B_m = 0.2T$ for ferrite core. The area product becomes $A_P = 37326mm^4$

Now choose the core from Appendix-I [101] which has A_P greater than the calculated value, P42/29 is being selected and which has $A_c = 264mm^2$ and $A_w = 181mm^2$

Step3: Number of turns

The number of turns can be calculated by the following equation

$$N = \frac{L I_m}{A_c B_m} \tag{A.3}$$

Substituting the values for the variable in the above, we have $N = 24Turns$

Step4: Wire gauge

The wire gauge of the conductor can be calculated by the following

$$a = \frac{I_{LB}}{J} \tag{A.4}$$

Substituting the values for the variable in the above, we have $a = 3.2mm^2$.

Select the wire gauge from the appendix-II [101] which has the wire cross section more than the calculated value $a = 3.243mm^2$

Step5: Cross check

The inequality $A_w K_w > aN$ has to be checked,

$108.6 > 77.76$

Step6: Air gap length

The length of the air gap can be calculated by the following equation

$$l_g = \frac{\mu_o A_c N^2}{L} \qquad \text{(A.5)}$$

where $\mu_o = 4\pi \times 10^{-7} H / m$

Substituting the values for the variable in the above, we have $l_g = 1.59mm$.

Design of Compensation Network Elements [20]

Elements of compensation network for the BDDC in boost mode can be calculated by following steps

1. Generate open loop bode plot of small signal transfer function control to output voltage of the BDDC in boost mode along with the feedback factor and PWM gain (1.6) .
2. Select a cross over frequency $\left(f_c\right)$ of non-minimum phase system (BDDC in boost mode) below RHP zero frequency of (1.7) i.e $f_C = 2$ kHz.
3. Select the desired phase margin (PM_D) between 45^0 and 60^0 for stable operation of the BDDC in boost mode i.e $PM_D = 60^0$.
4. Corresponding to step1, measure the gain corresponding to the selected cross over frequency, and determine error amplifier gain $\left(G\right)$ which will be simply negative of measured gain in dB i.e. $G = 23.5$ dB.
5. Corresponding to step1, measure phase shift (PS_S) corresponding to the selected cross over frequency i.e. $PS_S = -178^o$, and determine the required phase boost which is calculated by the following relation

$$Phaseboost = PM_D - PS_S - 90^0 = 60^0 - (-178^0) - 90^0 = 148^0$$

Type 3 error amplifier has been selected because the desired phase boost is less than 180^0.

6. Select the value of R1 as high as possible. R1 reduces the value compensation capacitors i.e. $R1 = 10$ kΩ.
7. Resistors and compensation capacitors value of the type 3 error amplifier can be calculated using K factor by the following relation

$$K = \left\{\tan\left[\left(\frac{Phaseboost}{4}\right) + 45^0\right]\right\}^2 = 50.16,$$

$$C2 = \frac{1}{2\pi f_c G R1} = 532 \text{ pF},$$

$$C1 = C2\left(K - 1\right) = 26 \text{ nF}$$

$$R2 = \frac{\sqrt{K}}{2\pi f_c C1} = 22 \text{ kΩ}$$

$$R3 = \frac{R1}{(K-1)} = 200\ \Omega$$

$$C3 = \frac{1}{2\pi f_c \sqrt{K} R3} = 56\ \text{nF}$$

Table C.1 Major components used for prototype of conventional BDDC

Components	Conventional BDCC
MOSFET switches S_1 and S_2	IRFP450 (2)
Diodes D_1 and D_2	MBRF2010CT(2) MUR1560(2)
Ferrite Core	P42/29
Processor	ezdspTMS320F28335
Driver ICs	TLP250 (2)
Voltage sensors	LEM LV100(2) LEM AV100(2)
Inductor wire gauge	SWG14
Filter Capacitors	C_1=4μF/63V C_2=200μF/200V
Load Rheostats	100Ω/50W (10)
Current sensors	LEM LA25 (2)
Snubber circuit Elements	15Ω/10W (4) 56Ω/10W (4) 10nF/100V(4) 1nF/63V (4)

Table C.2 Major components used for prototype of three-phase IBDDC

Components	Three-phase IBDCC
MOSFET switches	IRFP450 (6)
Diodes	MBRF2010CT (6) MUR1560 (6)
Ferrite Core	P42/29 (3)
Processor	ezdspTMS320F28335
Driver ICs	TLP250 (6)
Voltage sensors	LEM LV100(2) LEM AV100(2)
Inductor wire gauge	SWG14
Filter Capacitors	C_1=1μF/63V C_2=100μF/200V
Load Rheostats	100Ω/50W (10)
Current sensors	LEM LA25 (8)
Snubber circuit Elements	15Ω/10W (6) 56Ω/10W (6) 10nF/100V(6) 1nF/63V (6)

C.1 Overview of the eZdspTMF28335 [102]

The eZdspTMF28335 is a stand-alone card--allowing developers to evaluate theTMS320F28335 digital signal controller (DSC) to determine if it meets their application requirements. Furthermore, the module is an excellent platform to develop and run software for the TMS320F28335 processor. The eZdspTMF28335 is shipped with a TMS320F28335 DSC. The eZdspTMF28335allows full speed verification of F28335 code. Several expansion connectors are provided for any necessary evaluation circuitry not provided on the as shipped configuration. To simplify code development and shorten debugging time, a C2000 Code Composer Studio TM driver is provided. In addition, an onboard JTAG connector provides interface to emulators, with assembly language and ‘C’ high level language debug.

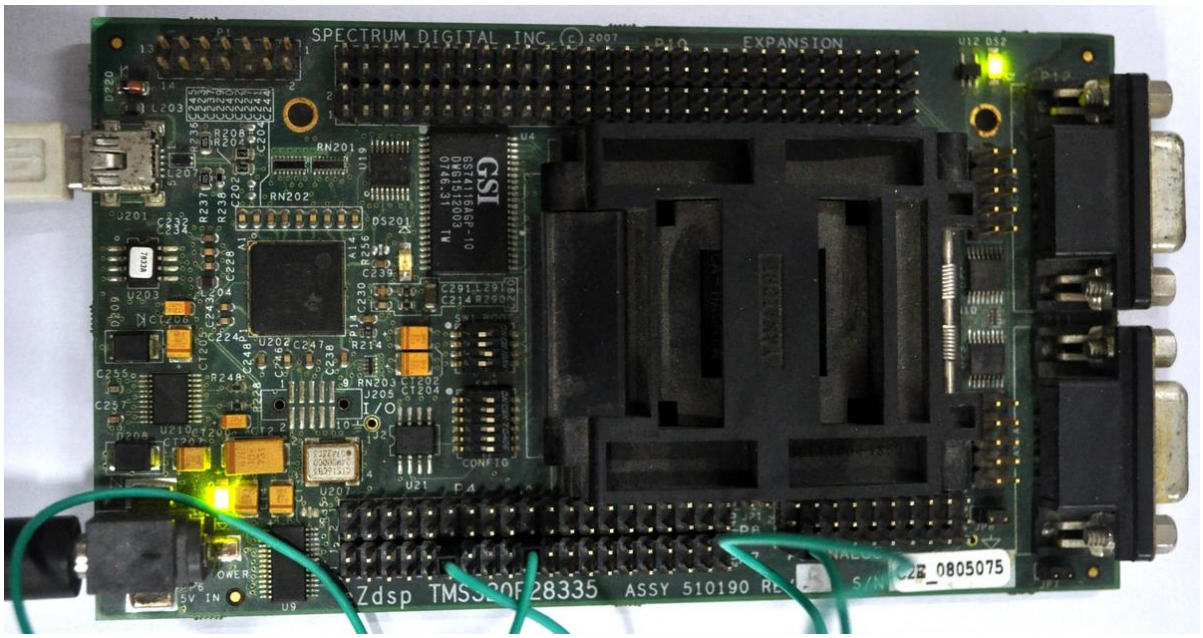


Figure C.1 eZdspTMS320F28335 Hardware

(source ti.com)

C.2 Key Features of the eZdspTMF28335

C.2.1 Hardware Features

The eZdspTMF28335 has the following features:

- TMS320F28335 Digital Signal Controller
- 150 Mhz. operating speed
- On chip 32-bit floating point unit
- 68K bytes on-chip RAM
- 512K bytes on-chip Flash memory
- 256K bytes off-chip SRAM memory
- On chip 12 bit Analog to Digital (A/D) converter with 16 input channels

• 30 MHz. input clock

• On board RS-232 connector with line driver

• On board CAN 2.0 interface with line driver and connector

• Multiple Expansion Connectors (analog, I/O)

• On board embedded USB JTAG Controller

• 5-volt only operation with supplied AC adapter

• On board IEEE 1149.1 JTAG emulation connector

C.2.2 Software Features

• TI F28xx Code Composer Studio TM Integrated Development Environment,Version 3.3

• Texas Instruments' Flash APIs to support the F28335

• Texas Instruments' F28335 header files and example software

C.3 Functional Overview of the eZdspTMF28335

Figure C.2 shows a block diagram of the basic configuration for the eZdspTMF28335.The major interfaces of the eZdsp are the JTAG interface, and expansion interface.

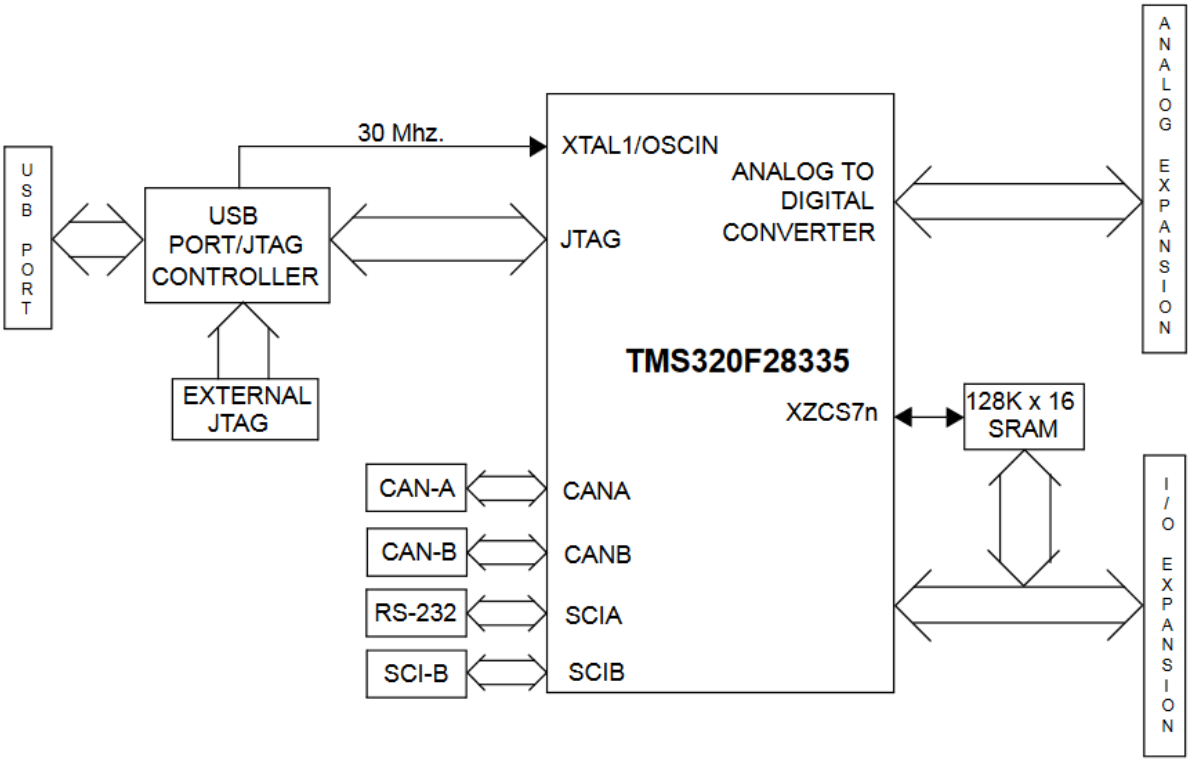


Figure C.2 Block diagram of the basic configuration for the eZdspTMF28335

Dynamic and output equation of three-phase IBDDC in boost mode with duty ratio $0 < d < 1/3$

Referring to the Figure 3.2, using SSA method [20] small signal control to the duty ration can be obtained by the following during $0 < d < 1/3$

During $dTs = d1 = d3 = d5$ and during $\left(\frac{1}{3} - d\right)T_S = d2 = d4 = d6$,

$$A2 = A4 = A6$$

$$A = (A1 + A3 + A5)d + A2(1 - 3d)$$

$$B2 = B4 = B6$$

$$B = (B1 + B3 + B5)d + B2(1 - 3d)$$

$\dot{x} = Ax + Bv_1$ and $v_2 = C^T x$

Steady state equations can be obtained by the following

$$\dot{X} = AX + BV_1$$

Under steady state, output parameters become constant and its derivatives are treated as zero, and given by the following

$$0 = AX + BV_1$$

$$X = -A^{-1}BV_1$$

Steady state output is given by the following

$$V_2 = C^T X$$

$$V_2 = -C^T A^{-1} BV_1$$

Small signal model equations can be obtained by the following

$$\dot{x} = \left[(A1 + A3 + A5)d + A2(1 - 3d)\right]x + \left[(B1 + B3 + B5)d + B2(1 - 3d)\right]v_1$$

$$v_2 = C^T x$$

Small signal perturbances are given by the following

$$d = D + \hat{d}, \frac{\hat{d}}{D} << 1,\ v_1 = V_1 + \hat{v_1},\ \frac{\hat{v_1}}{V_1} << 1,\ x = X + \hat{x},\ v_2 = V_2 + \hat{v_2}$$

$$\dot{X} + \dot{\hat{x}} = \left[(A1 + A3 + A5)(D + \hat{d}) + A2(1 - 3D - 3\hat{d})\right](X + \hat{x}) + \left[(B1 + B3 + B5)(D + \hat{d}) + B2(1 - 3D - 3\hat{d})\right](V_1 + \hat{v_1})$$

By separating steady state and small signal quantities from the above, steady state component can be obtained as below

$$\dot{X} = \left[(\mathrm{A1} + \mathrm{A3} + \mathrm{A5})\mathrm{D} + \mathrm{A2}(1 - 3\mathrm{D})\right] X + \left[(B1 + B3 + B5)\,\mathrm{D} + B2(1 - 3D)\right] V_1$$

$$0 = \left[(\mathrm{A1} + \mathrm{A3} + \mathrm{A5})\mathrm{D} + \mathrm{A2}(1 - 3\mathrm{D})\right] X + \left[(B1 + B3 + B5)\,\mathrm{D} + B2(1 - 3D)\right] V_1$$

$$X = -A^{-1} B V_1$$

Small signal component can be obtained as below

$$\dot{\hat{x}} = \left[(\mathrm{A1} + \mathrm{A3} + \mathrm{A5})\mathrm{D} + \mathrm{A2}(1 - 3\mathrm{D})\right] \hat{x} + \left[\left[(B1 + B3 + B5)\,\mathrm{D} + B2(1 - 3D)\right]\right] \hat{v}_1 + \left\{\left[A1 + A3 + A5 - 3A2\right] X + \left[B1 + B3 + B5 - 3B2\right] V_1\right\} \hat{d}$$

Above can be simplified as

$$\dot{\hat{x}} = A\hat{x} + B\hat{v}_1 + f\hat{d}\text{, where } f = \left[A1 + A3 + A5 - 3A2\right] X + \left[B1 + B3 + B5 - 3B2\right] V_1$$

And its small signal output can be obtained as

$$v_2 = C^T x$$

$$V_2 + \hat{v}_2 = C^T X + C^T \hat{x}$$

By separating steady state and small signal quantities from the above, steady state component can be obtained as below

$$V_2 = C^T X$$

Small signal component can be obtained as below

$$\hat{v}_2 = C^T \hat{x}$$

Small signal control to the duty ration can be obtained by the following

$$\left.\frac{\hat{v}_2(s)}{\hat{d}(s)}\right|_{\hat{v}_1 = 0} = C^T \left[sI - A\right]^{-1} f + qX$$

Where $\mathrm{A} = (\mathrm{A1} + \mathrm{A3} + \mathrm{A5})\mathrm{D} + \mathrm{A2}\left(1 - 3\mathrm{D}\right)$, $B = (B1 + B3 + B5)D + B2\left(1 - 3\mathrm{D}\right)$, $C^T = (C_{11}^T + C_{31}^T + C_{51}^T)D + C_{21}^T(1 - 3D)$

and $q = C_{11}^T + C_{31}^T + C_{51}^T - 3C_{21}^T$

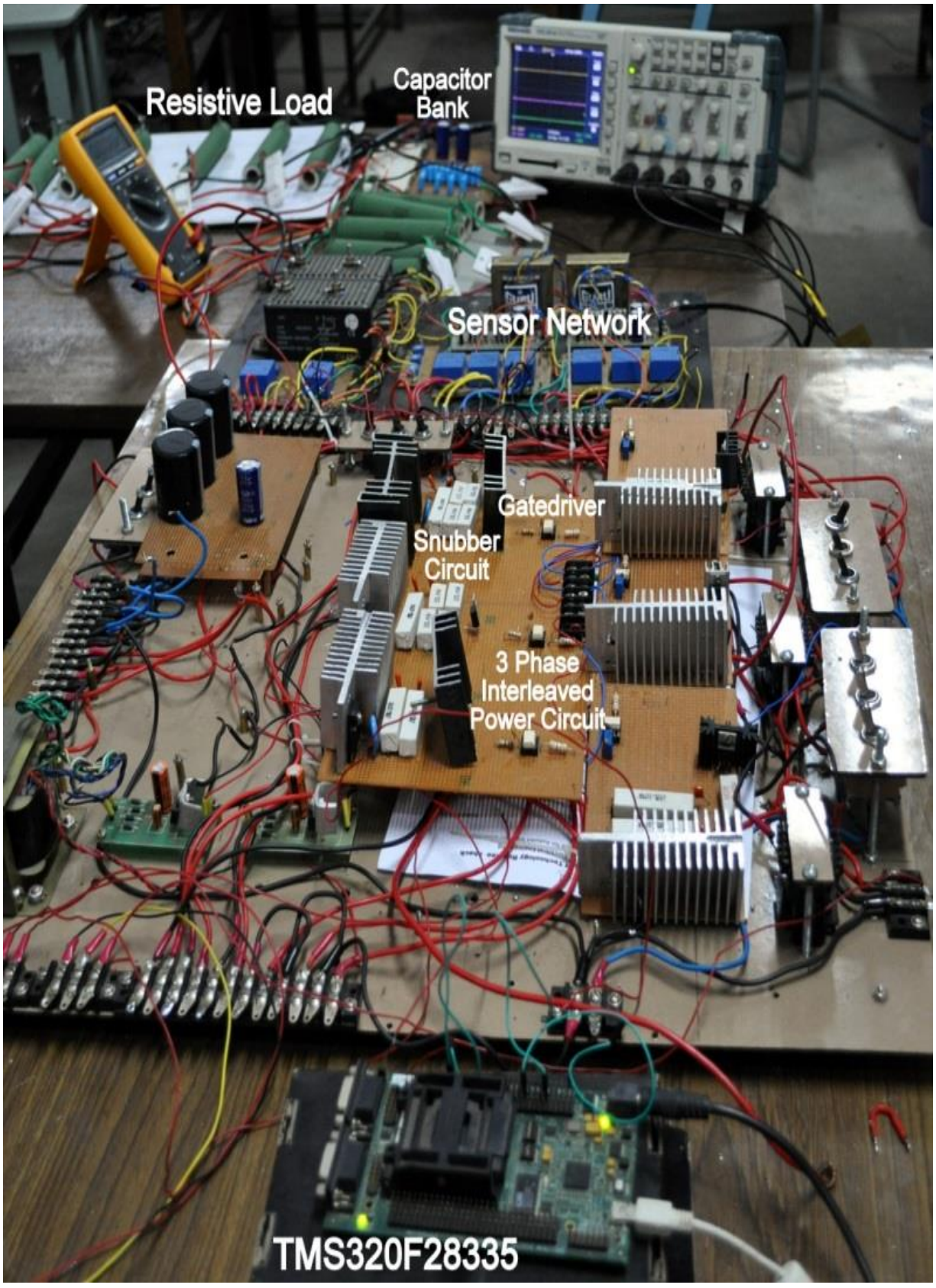


Figure E.1 Photograph of hardware setup of BDDC and three-phase IBDDC