PERFORMANCE ANALYSIS OF GNR INTERCONNECTS

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ELECTRONICS & COMMUNICATION ENGINEERING

(With Specialization in Microelectronics and VLSI)

By

NARASIMHA REDDY K

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE - 247 667 (INDIA)

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CANDIDATE'S DECLARATION

I hereby declare that the work, which is being reported in this dissertation report, entitled **"Performance Analysis of GNR Interconnects",** is being submitted in partial fulfillment of the requirements for the award of the degree of **Master of Technology** in **Microelectronics and VLSI,** in the Department of Electronics and Communication Engineering, Indian Institute of Technology, Roorkee is an authentic record of my own work, carried out from June 2012 to June 2013, under guidance and supervision of **Dr. B. K. Kaushik,** Assistant Professor and **Dr. Anand Bulusu**, Assistant Professor, Department of Electronics and Communication Engineering, Indian Institute of Technology, Roorkee.

The results embodied in this dissertation have not submitted for the award of any other Degree or Diploma.

Date : 14/06/2013
Place : Roorkee

K. Narasimha Reddy
Narasimha Reddy K

CERTIFICATE

This is to certify that the statement made by the candidate is correct to the best of my knowledge and belief.

Date: 15/6/2013
Place: Roorkee

Dr. B. K. Kaushik

Assistant Professor
Department of E & CE
Indian Institute of Technology, Roorkee

B. Anand

Dr. Anand Bulusu

Assistant Professor
Department of E & CE
Indian Institute of Technology, Roorkee

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Narasimha Reddy K

M.Tech (MEV)

ABSTRACT

In the era of nano-technology, Graphene nano-ribbons (GNRs) considered as an emerging material for the purpose of interconnects. It is because of their extremely good electrical, mechanical and thermal properties as compared to copper and other interconnects. The improvement in propagation delay, power dissipation and crosstalk as compared to regular Cu interconnects. The bandwidths and stabilities are much higher as compared to Cu/MWCNT interconnects at global interconnect lengths, the improvements become more significant with technology scaling and increasing wire lengths. In 2013, the ITRS predicts a higher value of current density of 3.3×10^{6} A/cm^{2}. As per current technology this higher values can only be supported by GNRs, as theoretical and experimental reports shows the value of current densities for GNRs is upto 10^{9} A/cm^{2}. So, for future high-speed VLSI interconnects technology, GNRs can prove as most outstanding organic material.

For MLGNR, multi-conductor transmission (MTL) line and equivalent single conductor (ESC) models have been presented also shown that both models are in good agreement with each other.

Propagation delay, power dissipation and crosstalk influenced propagation delays are discussed. By using dual axis propagation delay and power dissipation graphs, we estimated the optimum thickness of MLGNR for different interconnect lengths.

Bandwidth and relative stabilities of MLGNR interconnects analyzed and compared with MWCNT and Cu interconnects.

MLGNR interconnects performance deviations under the influence of process variations, which are due deviation in dimensions at time of manufacturing. These process induced effects are discussed in detail at different interconnect lengths and widths by varying only one dimension at a time also discussed all dimensional variations on performance of MLGNR interconnects.

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CHAPTER 1

INTRODUCTION

The progression of technology in the nanometer regime considers high density, high speed multifaceted ULSI circuits. A challenging and multifaceted task in modern technology is that transmission of signal through on chip interconnects between devices and circuit blocks. In nano-scale regime tightly packed and miniaturized transistors necessitates smaller wire cross-sections for local level connections whereas long-distance communication at global levels due to speedy growth of chip size and functional density. At present, interconnect delay plays a key role with belligerent device scaling and turn out to be substantial in the uninterrupted improvements in IC speed and density.

In the first four decades of the semiconductor industry, transistor delay and power dissipation limited system performance entirely. With technology scaling, interconnect performance shows a negative impact on system performance due to transistor delay and power performances are significantly reduced [1]. Severe effect on propagation delay of multifaceted ULSI circuit metal interconnects such as Al and Cu due to increment in resistance for nano-scale technologies [2]. With technology scaling, the cross-sectional area of Cu interconnects reduces that results in increasing resistivity under the influence of scattering effects such as grain and surface scatterings, and at gigahertz frequency of operation in ULSI circuits major hillocks is due to the electromigration. Thus, at higher frequencies, Cu interconnects may exhibit certain problems like crosstalk-induced spikes and delay, signal degradation and skin effect [3]. Therefore, it became necessary to find a substitution for global ULSI interconnects. This chapter introduces graphene nanoribbon interconnect technology used for designing of complex high speed integrated circuits (ICs).

1.1 Basics of GNRs

During the recent past, graphene nanoribbons (GNRs) have rapidly gained importance as an upcoming material that used for interconnects and depleted channels FETs [4-8]. The GNRs can be considered as a graphene sheet, stacked one upon another having similar dimension. Single layer of graphite sheet known as Graphene, in those carbon molecules arrangement is 2D honeycomb (hexagonal) lattice structure [9] as shown in Fig. 1.1.

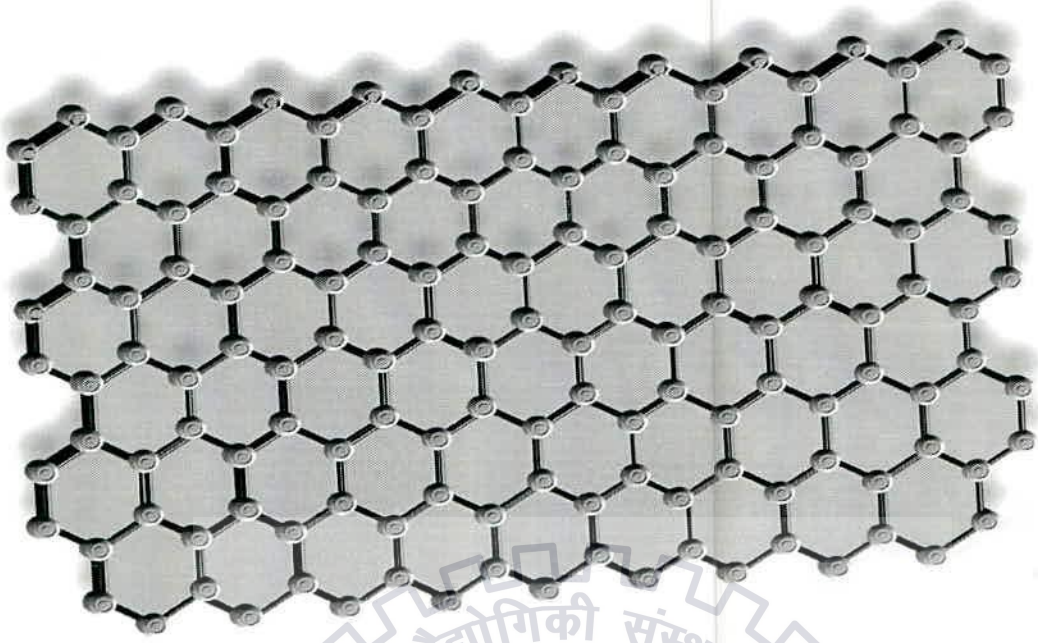


Fig. 1.1: Graphene hexagonal structure

1.2 Band structure and properties

Carbon atoms in graphene forms sp^2 covalent bonding using one σ-bond and two π-bonds because detached carbon atom having four valence electrons located in $2s$, $2p_x$ and $2p_y$ whereas $2p_z$ is empty which doesn't participate in bonding as shown in Fig. 1.2. In a graphene sheet, bond length between two corbon atoms is about 0.142nm. Stacked graphene layers form multilayer graphene nanoribbons with an interlayer distance of 0.34nm [10]. The core materials for graphene are charcoal, carbon nanotubes, and fullerenes due to their structural similarity.

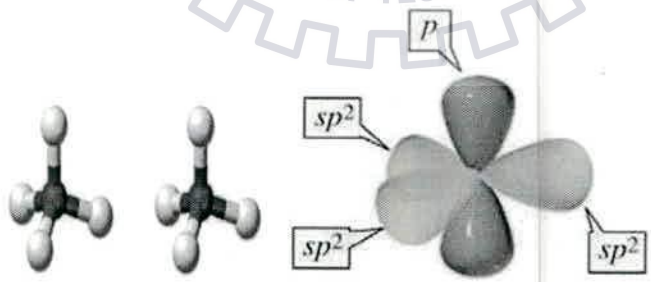


Fig. 1.2 Bonding of two carbon atoms in graphene [11]

Usually graphene, electrical signal transmission properties depends on holes (electrons) near to the Fermi level, after application of signal these bonded holes (electrons) excited to occupied (unoccupied) states ($2p_z$) [11]. These dependable signal transmission properties of graphene responsible for long mean free paths (MFPs) ranging from 1-5μm that exhibits in ballistic transport phenomenon for local interconnect lengths (<1μm). Due to the

large MFPs, GNRs have higher carrier mobility's up to 10^5 $cm^2V^{-1}s^{-1}$ and larger current densities of 10^8 A/cm^2 as compared to Cu [12-15]. Depending on the number of stacked graphene sheets, GNRs classified as single-layer GNR (SLGNR) and multi-layer GNR (MLGNR) as shown in Fig. 1.3 [16]. Due to the higher resistivity possess by SLGNR, implies MLGNR has considered as a potential interconnect material [17].

(a) (b)

Fig. 1.3: Lattice structures of (a) SLGNR and (b) MLGNR [16]

Graphene in plane electrical conductivity is $1.25x10^4$ S/cm whereas for Cu electrical conductivity is $5.9x10^5$ S/cm. As approaches to achieve the expected conductivity, there are two possibilities, they are, enhance the mobility in MLGNR or increasing the number of carriers. Mobility of carriers in GNRs increased by improving their physical and chemical degree of precision by using high-temperature treatment (HTT) technique in order to reduce defect or void scatterings of carriers [18]. Even though high quality GNR is not used for conductive purposes, so in order to increase conductivity further, approach is to intercalate doping of highly ordered MLGNR with AsF_5 or SbF_5 by exposing graphene to the vapors of AsF_5 at high pressures which raises the number of carriers [18]. By the above intercalation doped MLGNR with AsF_5, conductivity increased to $3.2x10^5$ S/cm, and it is slightly more than copper, and both reproducibility and stability to electromigration are very good. The degree of doping, decided by stage indices where stages-s designates the number of undoped GNR layer present between two intercalative doping layers, different stages of intercalated doped MLGNR shown in Fig. 1.4. This stage index's' depends mainly on growth time and intercalant vapor pressure. For stage-2 AsF_5 intercalative doped MLGNR case the spacing between undoped and doped layers is taken as δ_1=0.34nm and δ_2=0.815nm respectively [19]. For outstanding electrical and thermal properties of MLGNR considered as future, interconnect materials in ULSI.

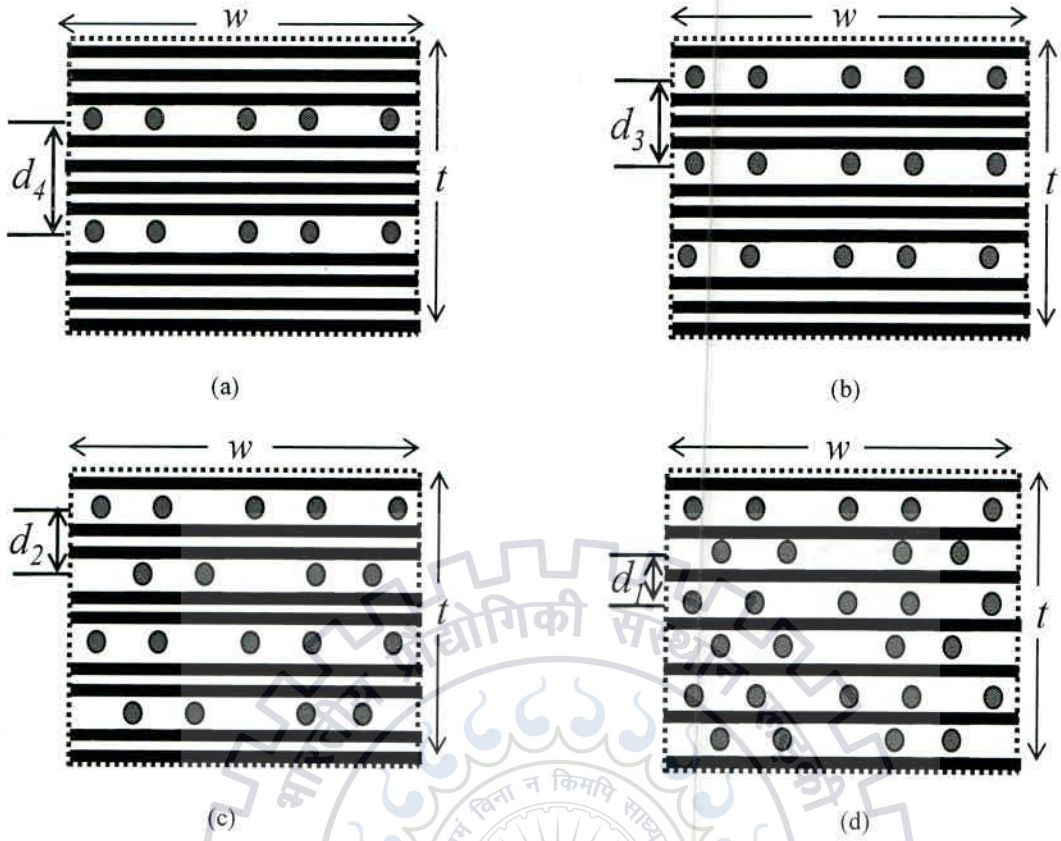


Fig. 1.4: Different of intercalation doping in GNR interconnects (a) Stage-4 (b) Stage-3 (c) Stage-2 and (d) Stage-1 and d_1, d_2, d_3 and d_4 values are 1.835nm, 1.495nm, 1.129nm and 0.815nm respectively

1.3 Classification of GNR

The electrical properties of GNR depend on the edge structures,, which is decided by their chirality/asymmetry. Depending on their chiral indices (n, m), GNRs are classified as armchair-GNR (ac-GNR) and zig-zag GNR (zz-GNR) as shown in Fig. 1.5, whose chiral indices are n or m equal to zero and n=m respectively. The assumption that graphene nanoribbons is further distinguished into semiconducting and metallic depending on number of carbon rings (N) present across the width of GNR that has fixed along the its length. Metallic properties in armchair GNRs to be determined by the condition of N=3P+2, whereas semiconducting properties determined using the condition of N=3P or 3P+1, where P is 0 or any natural number. Apart from this, zig-zag GNRs are always metallic due to conduction band and valence band both touches each other for all widths independent of N. The tight binding model estimates band structures of ac-GNR and zz-GNR based on atomic simulations [20].

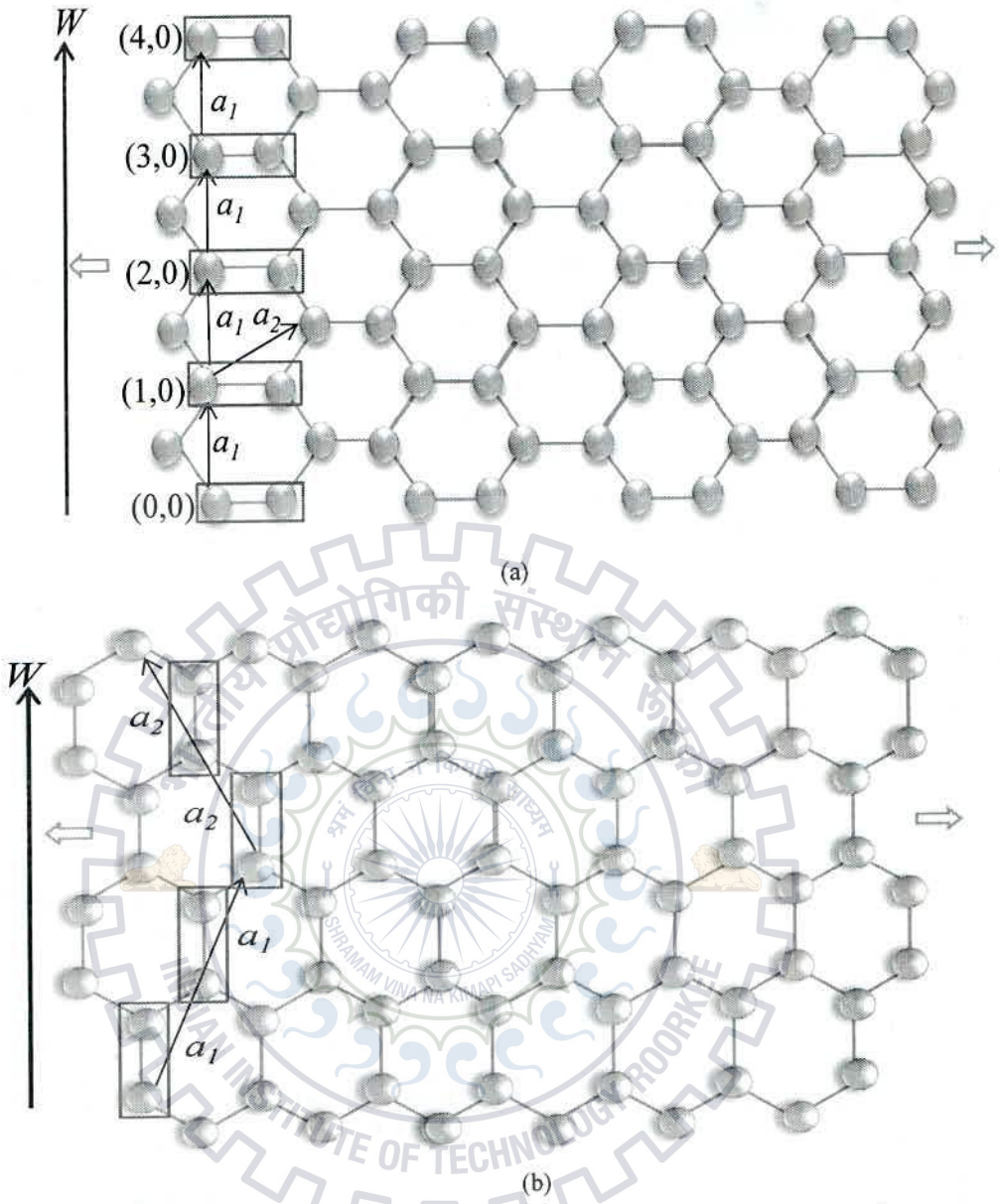


Fig. 1.5: Graphene nanoribbon (a) (4, 0) armchair (b) (3, 3) zig-zag structures

Progress in science and recent technology designates that GNR have invoked many concerns, research based on their fabrication advantageous, which represented in [21]. Photolithographic fabricated GNRs used for different purposes those are channel of a MOSFET, interconnects, 3D-vias, sensors etc.

1.4 Motivation

For current nano scale or deep submicron technologies GNRs can be considered as more assuring material than other mainstream interconnects such as Cu or Al because of their robustness to electromigration, absence of grain boundary scatterings and other novel properties. As discussed above properties like, long ballistic transport length, high thermal

conductivity, high current density and material durability has given the motivation to do research further. Multi-conductor transmission line model is complex and time consuming to do analysis so equivalent single conductor model is proposed by some researchers. So in chapter-2 presents whether equivalent single conductor model is showing good agreement with multi-conductor transmission line model or not? If not, how much deviation between two models at different interconnect lengths? What is performance deviation between SLGNR and MLGNR having different thickness, and how the crosstalk will affect the performance of MLGNR at different interconnect thickness for varying lengths, are presented in chapter-3. Performance comparison of MLGNR with Cu and MWCNT interconnects in frequency as well in time domains in chapter-4. Manufacturing process variations arises due to temperature, pressure, environment and manufacturing process changes will affect the interconnect dimensions. How much deviation on performance of MLGNR interconnects because of these process variations discussed in chapter-5.

1.5 Organization of the thesis

Chapter-1 introduces graphene structure and chemical bonding between two carbon atoms as well some properties of graphene. This chapter also presents classification of GNRs based on their chirality likewise classification based on intercalate doping of MLGNR with AsF_5 between two layers.

Chapter-2 presents multi-conductor transmission line model of SLGNR and MLGNR. A brief discussion on interconnect parasitics and how they depend on interconnect dimensions. It also incorporates equivalent single conductor model for MLGNR and its validity with respect to multi-conductor transmission line model.

Chapter-3 demonstrates the comparison of propagation delay variation of SLGNR and MLGNR at different interconnect widths and lengths. This chapter possesses crosstalk delay variation for different MLGNR interconnect thicknesses. Moreover, a new technique is introduced to find the optimum thickness of MLGNR interconnects with which minimum delay and power dissipation has been achieved.

Chapter-4 presents the analysis of relative stability and bandwidth for MLGNR, MWCNT and Cu interconnects in frequency domain. A transfer function of a DIL system is used to find the analytical expression of output voltage waveform.

Chapter-5 explains the effect of process induced width, length, dielectric thickness and a dielectric constant variation on overall delay of MLGNR interconnects.

Chapter-6 draws a brief summary of the dissertation report.

CHAPTER 2

GNR INTERCONNECT MODEL

2.1 Introduction

Interconnect is a metallic wire and its operation is similar to a waveguide in signal transmission. Well-established metallic interconnects such as Al and Cu denoted by the equivalent *RLC* network as in Fig. 2.1. An equivalent *RLC* model for Cu interconnects as in Fig. 2.1 is not valid for small dimensions because it required to add some more additional inductance and capacitance paracitics. These parasitics, like resistance, capacitance, inductance are depends on the dimensions of interconnects by which performance analysis can be performed. While formal interconnect transmission-line model having a scattering resistance (R), an electrostatic capacitance (C_e)a and magnetic inductance (L_m),, whereas a kinetic inductance (L_k) and a quantum capacitance (C_q) are introduced for CNT/MLGNR interconnects by P. J. Burke based on Luttinger theory [22].

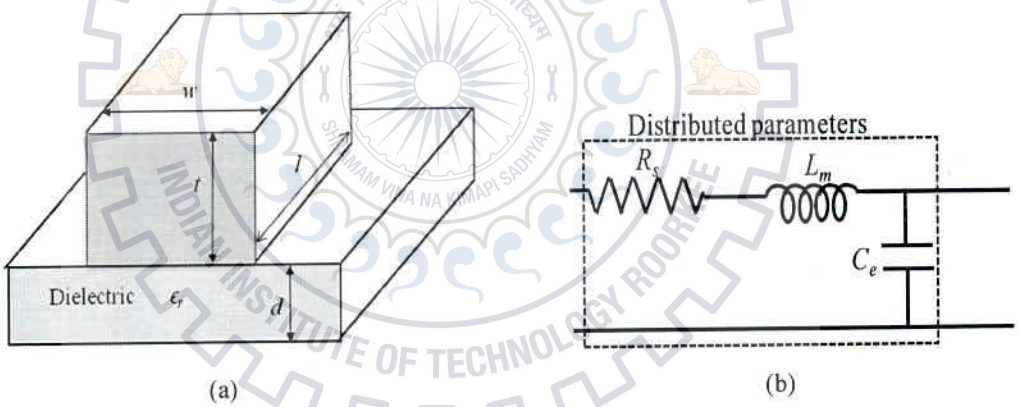


Fig. 2.1: Cu interconnects (a) Geometry and (b) Equivalent distributed *RLC* circuit

Kinetic inductance (L_k) and quantum capacitance (C_q) depend on conducting channels (or modes or sub-bands) which approximated to $D/\hbar\langle v\rangle$ where $\langle v\rangle$ average velocity, $\hbar$ is Plank's constant and D is the density of states. The number of channels can approximated as twice the number of wavelengths of carriers that exactly fit into the cross-section of interconnects which is similar to the modes of waveguide in electromagnetics. These conducting channels increase linearly with the cross-sectional area of interconnect [23]. For larger cross-sections, number of conducting channels is higher so L_k decreases and C_q increases (L_k and C_q dependence on modes and its equation discussed later in this chapter).

The ratio of the velocity of propagation and speed of light $[(L_mC_e)/(C_qL_k)]^{0.5}$ is 10^{-2} for this to happen a number of conducting channels has to go beyond the several thousands. For this to happen the dimension of Cu interconnect should be more the $100nm^2$, whereas wave length of the electron is considered as 0.2nm (approximately $\sqrt{h^2/2meV}$). From above discussion, Cu also exhibits kinetic inductance and quantum capacitances at lower interconnect cross-sections.

2.2 SLGNR geometry and its equivalent *RLC* model

Fig. 2.2 (a) exhibits the cross-sectional view of SLGNR interconnects above ground plane which is separated by dielectric whose permitivity (dielectric constant) ε_r=2.2. The transmission line model of SLGNR as in Fig. 2.2 (b) and its parasitic values depends on its width (w), ε_r, and dielectric thickness (d) in its geometry.

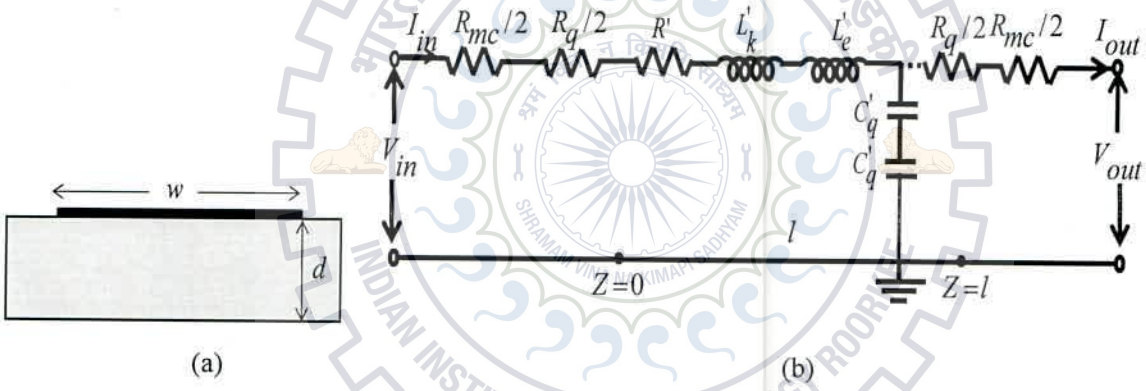


Fig. 2.2: Distributed single-conductor transmission line model of SLGNR interconnects having contact resistance of R_{mc}

2.3 MLGNR geometry and its equivalent *RLC* model

Fig. 2.3 (a) exhibits the cross-sectional view of MLGNR interconnects above ground plane which is separated by dielectric. The equivalent multi-conductor transmission line (MTL) model of MLGNR [23] is also shown in Fig. 2.3 (b) and its parasitic values depends on its width (w), ε_r, and dielectric thickness (d) in its geometry. The total number of layers (N_{layer}) in MLGNR can be calculated using thickness (t) and δ. The parameter δ represents the interlayer distance which is equivalent to 0.34nm for neutral MLGNR interconnects.

$$N_{layer} = 1 + Integer(t/\delta) \quad (1)$$

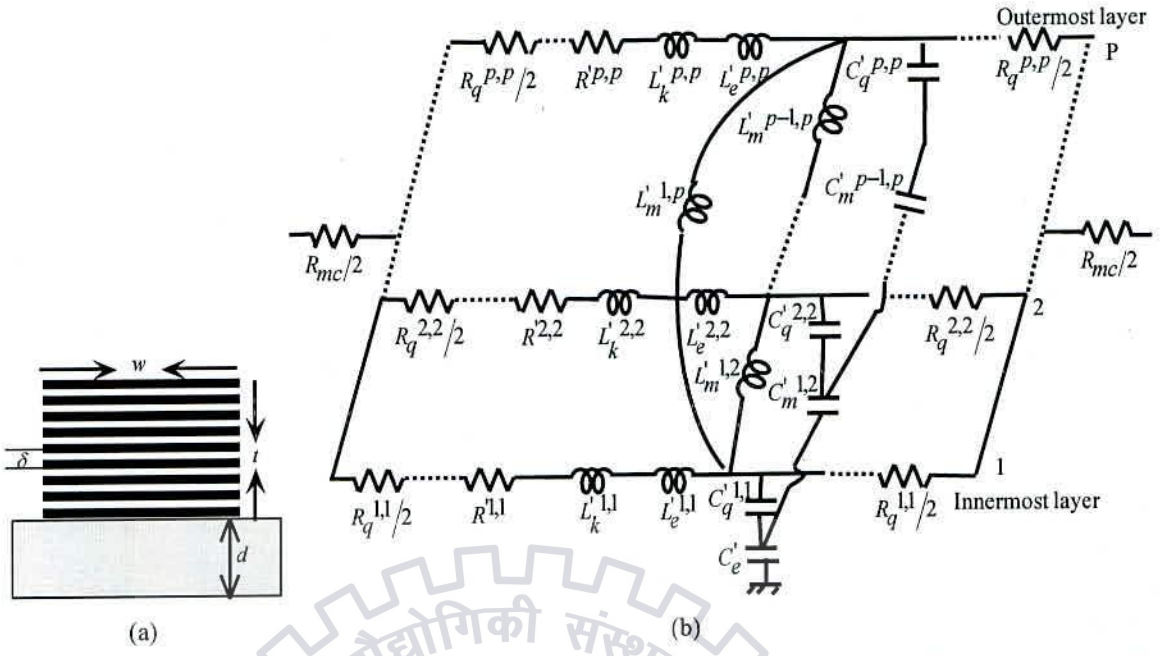


Fig. 2.3: Distributed multi-conductor transmission line model of MLGNR interconnects having contact resistance of R_{mc}

2.4 Conducting channels

Before discussing the parasitic of MLGNR, one of the major physical parameters which is used for the estimation of quantum resistance, scattering resistance, quantum capacitance and kinetic inductance in MTL model known as number of conducting channels (N_{ch}). Conduction and valence bands contain quantized energy in finite numbers of sub-bands due to quantum confinement across nanoscale width of a MLGNR (w). N_{ch} is a physical constant, which depends on Fermi energy E_F, at a given temperature T and hole and electron contributions in the conduction in the valence and conduction sub-bands respectively, and it expressed as [24]

$$N_{ch} = N_{ch,electrons} + N_{ch,holes}$$

$$= \sum_{j=0}^{n_V}\left[1+\exp\left(E_F - E_{n,hole}/K_BT\right)\right]^{-1} + \sum_{j=0}^{n_C}\left[1+\exp\left(E_{n,electron} - E_F/K_BT\right)\right]^{-1} \quad (2)$$

2.5 Resistance

2.5.1 Contact resistance

Figs. 2.2(b) and 2.3(b) represents equivalent models of SLGNR and MLGNRs, exhibits an imperfect metal-nanoribbon contact resistance (R_{mc}) that possess a typical value ranging from 1kΩ to 6kΩ depending on the current fabrication process [24].

2.5.2 Quantum resistance

Another fundamental resistance in the MTL model of MLGNR interconnects is quantum resistance that experiences due to the quantum confinement of carriers in transverse direction due to smaller widths. This quantum capacitance depends on transverse energies of confined electrons in MLGNR interconnects and it calculated as [25]

$$R_q^{j,j} = \frac{h}{2e^2 N_{ch}} = 12.9\ k\Omega / N_{ch} \tag{3}$$

where N_{ch} is conducting channels per layer in GNR sheet, h is Plank's constant and e is electronic charge.

2.5.3 Scattering resistance

The equivalent *RLC* model of Figs. 2.2(b) and 2.3 (b) exhibits one more resistance due to scattering of carriers in MLGNR interconnect such as line edge roughness (LER), acoustic phonon (AP) and static impurity (SI) scatterings [26-29]. This scattering resistance denoted as $R^{j,j}$, and primarily depends on the mean free path (MFP) of carriers (λ_L) and its length, so per unit length (*p.u.l.*) scattering restance $R'^{j,j}$ can be calculated as

$$R'^{j,j} = \frac{h}{2e^2 N_{ch} \lambda_L} \Omega / m \tag{4}$$

If the interconnect length is less than MFP in such applications the carriers don't experience any scatterings, therefore in the MTL model $R'^{j,j}$ becomes zero that is smaller MLGNR interconnect lengths (less than 1μm) experiences ballistic transport. At global interconnect lengths this scattering resistance is dominating than quantum and contact resistance.

2.6 Inductance

2.6.1 Kinetic inductance

In higher alternating electric fields, the carriers in MLGNR interconnects experience more eminent kinetic energies. Because of these higher kinetic energies, confined carriers possess higher velocities experiences some inertia due to its mass at high frequencies in signal transmission, this causes inductance which is called as kinetic inductance and it is in series with the scattering resistance $R'^{j,j}$. The *p.u.l.*kinetic inductance, denoted as $L_k'^{j,j}$ and it is expressed as [22]

$$L_k^{'j,j} = \frac{h}{4e^2 v_F N_{ch}} \approx 8\,nH/\mu m \tag{5}$$

where $v_F \approx 8\times10^5$m/s represents the Fermi velocity of carriers in MLGNR [22].

2.6.2 Magnetic inductance

The magnetic inductance of a conductor is defined as using Lenz's law, current through a conductor experiences a inductance which induces a proportional voltage which opposes a change in current. *p.u.l.* magnetic inductance is denoted as $L_e^{'j,j}$ and is expressed as [25]

$$L_e^{'j,j} = \frac{\mu_0 d}{w} H/m \tag{6}$$

2.6.3 Mutual inductance

The adjacent layers in MLGNR exhibits mutual inductance that exists due to the induced *emf* in a magnetic field between the layers. Unit length mutual inductance $L_m^{'j-1,j}$ expressed as [25]

$$L_m^{'j-1,j} = \frac{\mu_0 \delta}{w} H/m \tag{7}$$

2.7 Capacitance

2.7.1 Quantum capacitance

Serge Luryi, first introduced term quantum capacitance, which depends on the density of states (DOS) in solids. DOS calculated based on effective mass of carriers, which depends on material properties and its dimensions. The *p.u.l.* quantum capacitance denoted as $C_q^{'j,j}$ and it expressed as [22]

$$C_q^{'j,j} = \frac{4e^2}{hv_F}.N_{ch} \approx 193aF/\mu m \tag{8}$$

2.7.2 Electrostatic capacitance

The innermost layer of MLGNR experiences an electrostatic capacitance with a ground line due to the electrostatic energy stored between them, it primarily depends on the MLGNR interconnect width (w), length (l) and dielectic thickness (d). *p.u.l.* electrostatic capacitance is denoted as $C_e^{'}$, which is expressed as [25]

$$C_e^{'} = \frac{\varepsilon_0 w}{d} F/m \tag{9}$$

2.7.3 Mutual capacitance

The adjacent layers in MLGNR exhibits mutual capacitance that exists due to the charge carrier transport between the layers respectively. Mutual capacitance is represented by $C_m^{'}{}^{j-1,j}$ and it is expressed as [25]

$$C_m^{'}{}^{j-1,j} = \frac{\varepsilon_0 w}{\delta} F/m \tag{10}$$

2.8 ESC model of MLGNR

To reduce computational effort of MTL model is reduced to ESC model as shown in Fig. 2.4 by considering an equal potential at any arbitrary cross section of MLGNR interconnect. Based on this key assumption, L_m and C_m between adjacent layers can be neglected. The performance of the robust ESC model shows a good accuracy with the equivalent MTL model of MLGNR interconnects Fig. 2.3 (b). Thus, the equivalent parasitics in Fig. 2.4 can be calculated using the total number of conducting channels associated with MLGNR layers [].

Fig. 2.4: The ESC model of MLGNR having interconnect length l

Equivalent quantum resistance, scattering resistance and kinetic inductance of ESC model of MLGNR is equal to single layer quantum resistance, scattering resistance and kinetic inductance divided with number of layers respectively.

$$R_{q,esc} = \frac{h/2e^2}{N_{ch}N_{layer}} \tag{11}$$

$$R_{esc}^{'} = \frac{h/2e^2}{N_{ch}N_{layers}\lambda_L} \tag{12}$$

$$L_{k,esc}^{'} = \frac{h}{4e^2 v_F N_{ch}N_{layers}} \tag{13}$$

Equivalent quantum capacitance of ESC model of MLGNR is equal to single layer quantum capacitance multiplied with number of layers respectively.

$$C_{qesc} = \frac{4e^2}{hv_F} N_{ch} N_{layers} \tag{14}$$

Quantitative value of electrostatic capacitance in MTL and ESC model are same because, it does not depend on the thickness of MLGNR and depends on width and dielectric thickness.

$$C_{e,esc} = C_e \tag{15}$$

2.8 Comparison of ESC and MTL models

For the driver interconnect load system (DIL) as shown in Fig. 2.5 having CMOS driver at 32nm technology node having NMOS and PMOS widths of 640nm and 1280nm respectively and a load capacitance C_L=10fF. As in Fig. 2.5, the input signal have rise and fall times equal to 10ps and pulse width of 50ns and pulse width of 200ns. To find propagation delay, inputs triggered at 50% rising pulse signal and output targeted at the same 50 % but at a falling pulse signal. This MLGNR interconnects is represented by the conventional MTL model or the reduced ESC model to perform time-domain analysis. The robustness of ESC model with respect to MTL model represented as below.

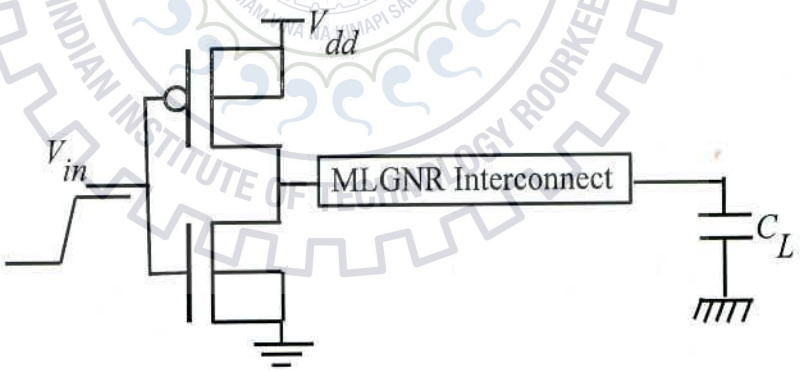


Fig. 2.5: The driver interconnect load system (DIL), MLGNR is placed between the driver and load

From Fig. 2.6, it is observed that the output responses of MTL and ESC models are in good agreement for smaller interconnect lengths whereas for longer interconnect lengths, there is some deviation between the multi-conductor transmission line and equivalent single conductor models. This deviation primarily arises due to the neglected mutual inductance and capacitances in ESC model. For different interconnect lengths average percentage of deviation is not more than 6 percent, from this the conclusion is that ESC is a robust model.

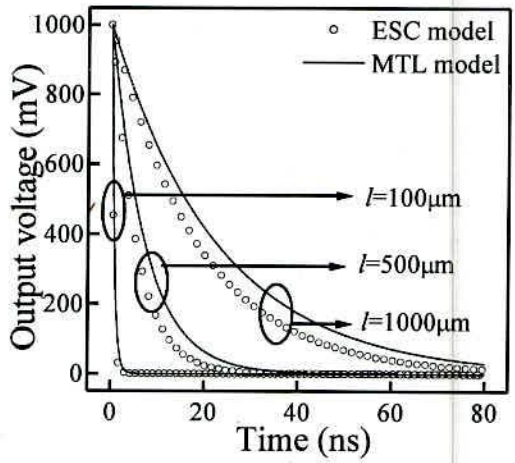


Fig. 2.6 Output transient falling waveforms of MLGNR for MTL and ESC models at N_{layer} = 40

CHAPTER-3

DELAY, POWER AND CROSSTALK ANALYSIS

In this chapter, the performance analyses based on propagation delay, power dissipation and crosstalk delay at different interconnect dimensions. Propagation delay found by applying a rising pulse signal to a DIL system as shown in Fig. 2.5, implies output to be falling signal. To get 50% propagation delay both input and outputs triggered and targeted at 50% of their peak values. Average power dissipation occurred for transmission of a pulse signal from source end to destination end. This power dissipation mainly due to impedance exhibited by MLGNR interconnects. In coupled interconnects, crosstalk noise broadly classified into two categories: (1) functional and (2) dynamic crosstalk noise. This chapter presents dynamic cross talk effects on MLGNR performance.

3.1 Analysis of propagation delay

In this section, HSPICE simulations performed for different number of MLGNR layers at different interconnect lengths by varying widths. Fig. 3.1 (a) to (e) shows the delay variation for different interconnect lengths for varying widths. From this analysis, it noticed that the delay increases for increasing interconnect lengths due to its parasitic values proportional to its length. As the number of layers increases, the delay is decreasing due to increasing the number of conducting channels, which decreases ${R_q}^{j,j}$, ${R_s}^{j,j}$ and ${L_k}^{j,j}$ but it increases ${C_q}^{j,j}$ which is not a dominating parasitic. For increasing widths, delay decreases up to some critical width after that it increases due to electrostatic capacitance increases more compared to decrease in equivalent quantum and scattering resistances.

In MLGNR delay decreases sharply as the number of layers increases initially and it saturates at a certain value. If the number of layers (N_{layer}) increases after a certain limit the delay is going to be constant because the dominating electrostatic capacitance is constant and the decrease in equivalent resistance and inductances are negligible in an MTL model of MLGNR interconnects. Propagation delay versus the number of layers at different interconnect lengths as in Fig. 3.2. It observed that propagation delay has saturated above 40 layers for all interconnect lengths. Table-1 shows the percentage variation in delay of

MLGNR N_{layer}=20 with respect to SLGNR, MLGNR N_{layer}=4 and MLGNR N_{layer}=10. The percentage reduction in delay increases for higher length of GNR interconnects.

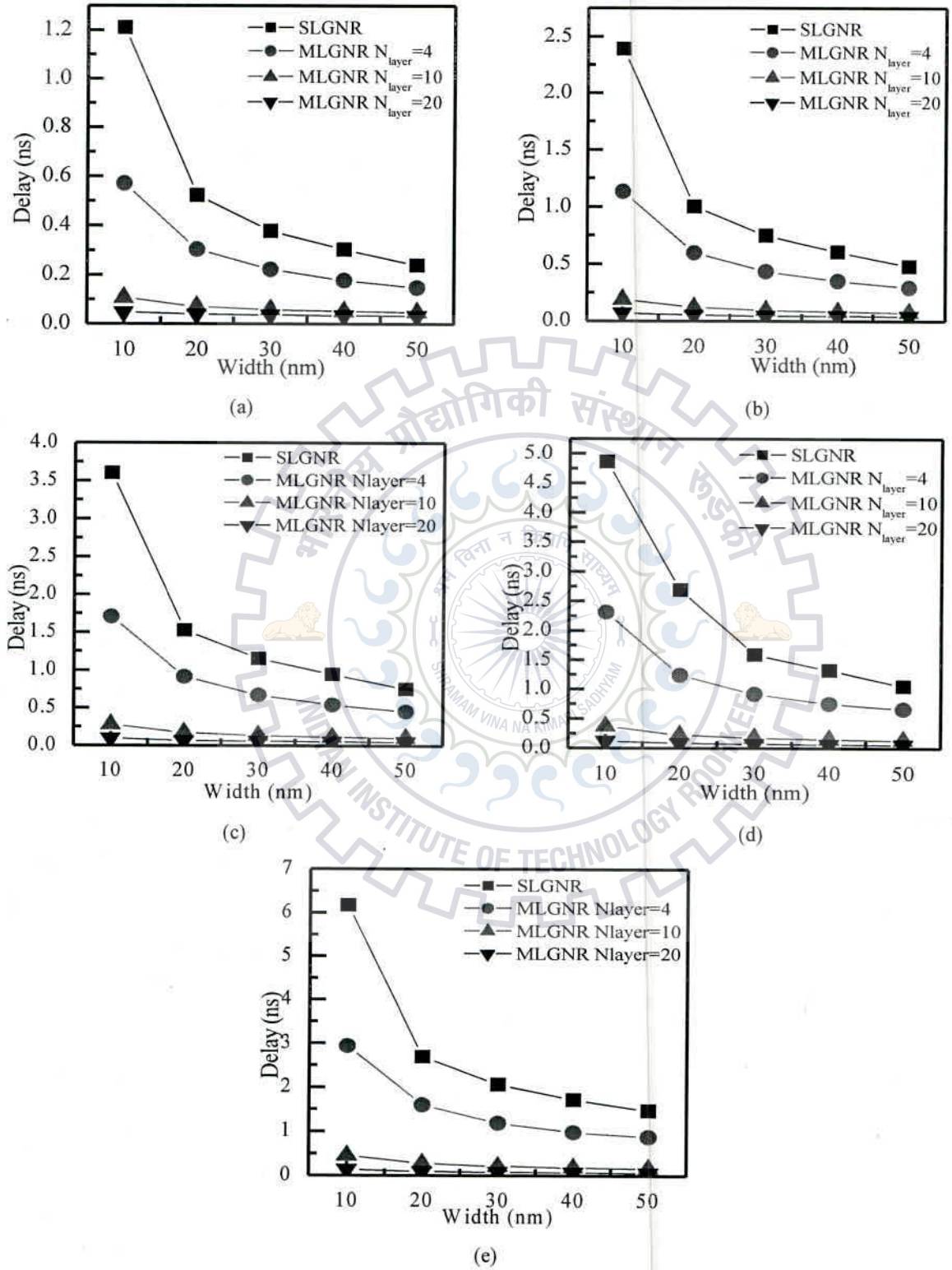


Fig. 3.1: Propagation delay of GNR with varying widths at the interconnect lengths (a) 100μm (b) 200μm (c) 300μm (d) 400μm (e) 500μm

Table-3.1: Percentage improvement in delay of MLGNR N_{layer}=20 with respect to SLGNR, MLGNR of N_{layer} = 4 and N_{layer} = 10

Length of GNR interconnects (μm)	Width GNR (nm)	% improvement in delay of MLGNR N_{layer}=20 *w.r.t*		
		SLGNR	MLGNR N_{layer}=4	MLGNR N_{layer}=10
100	10	96	91.5	55.1
	20	92.5	87.2	45.4
	30	90.5	83.8	38.7
	40	88.7	80.8	33.7
	50	86.1	77.6	30.3
200	10	97.1	93.8	63.1
	20	94.8	91.3	56.4
	30	93.9	89.5	51.5
	40	93.0	87.9	46.8
	50	91.5	86	43.6
300	10	97.4	94.5	66.3
	20	95.7	92.8	61.3
	30	95.1	91.6	57.1
	40	94.5	90.5	53.6
	50	93.5	89.2	50.9
400	10	97.6	94.9	68.1
	20	97	93.6	64.1
	30	95.8	92.7	60.7
	40	95.3	91.8	57.8
	50	94.5	91.3	55.6
500	10	97.7	95.2	69.1
	20	96.4	94.0	65.9
	30	96.1	93.3	63
	40	95.8	92.6	60.5
	50	95.4	92.4	58.8

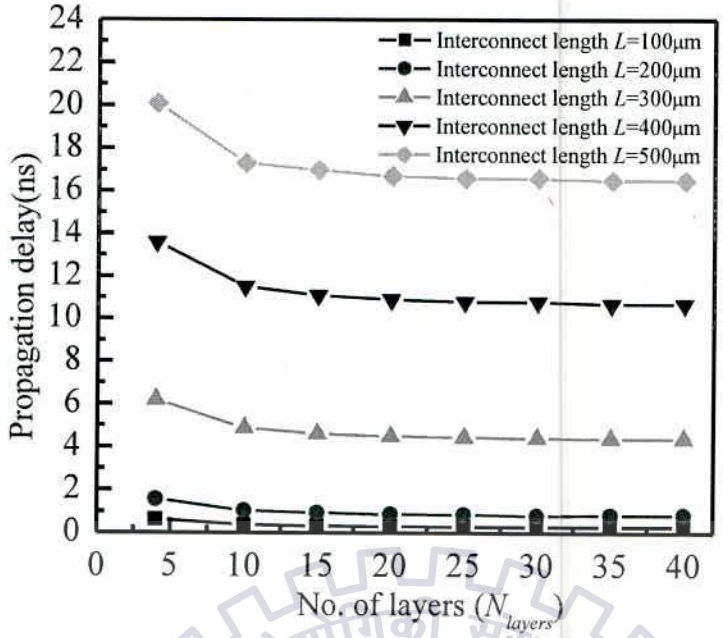


Fig. 3.2: Propagation delay of MLGNR interconnects with respect to the number of layers

3.2 Optimum thickness of MLGNR interconnects

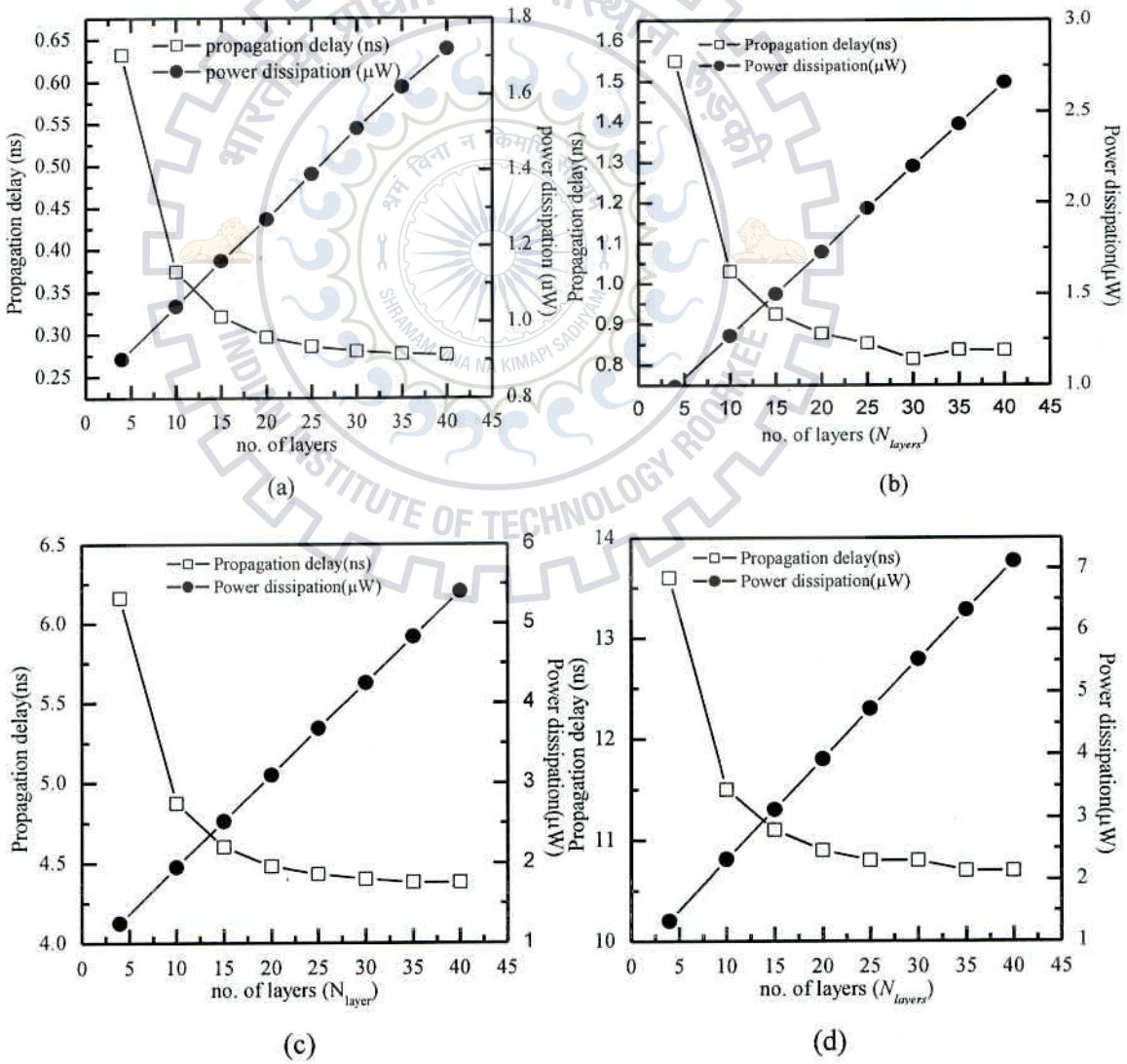
Optimum thickness can found by using power-delay graphs, in which thickness on x-axis and propagation delay and power dissipations plotted on dual Y-axis in the graphs. The thickness for which delay and power plots meet, that point considered as optimum thickness because at that thickness both delay and power dissipation are optimized. To find optimum delay and power dissipation for different number of layers at global interconnect lengths ranging from 100μm to 1000μm corresponding geometry of MLGNR suggested in Fig. 2.3 (b). Simulation setup uses a driver-interconnect-load (DIL) system as shown in Fig. 2.5, employing CMOS driver at 32nm technology node for accurate estimation of delay and power dissipation. The DIL system is driven by a supply voltage (V_{dd}) = 1V and terminated by a load capacitance C_L of 10aF.

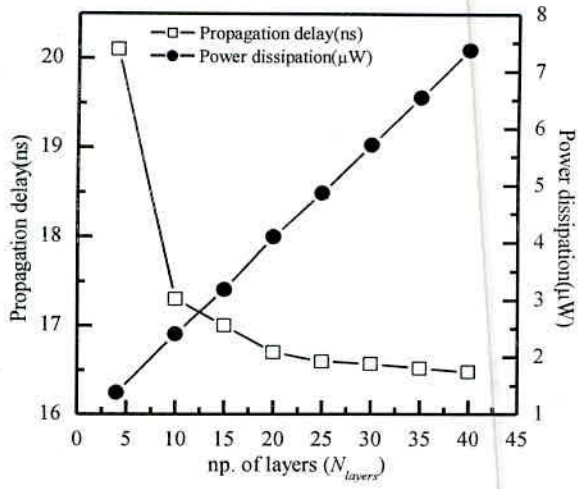
3.2.1 Optimal delay and power performances

For a different number of MLGNR layers at global interconnect lengths using the above-mentioned setup is shown in Fig. 2.5. HSPICE simulations performed to calculate the delay and power dissipation. Fig. 3.3 illustrates the change in delay and power dissipation with respect to the altering number of layers of different interconnect lengths of 100, 300, 500, 800 and 1000μm respectively. It is observed that the propagation delay and power dissipation performance increase with interconnect lengths whereas the minimum delay and maximum power dissipation took place for the higher number of MLGNR layers. Increasing number of

layers in MLGNR reduces the propagation delay whereas power dissipation is increased and for increasing the lengths, both delay and power dissipation is increased. Fig. 3.3 used to find the optimum number of stages where both the curves are intersecting to each other. From the curves of propagation delay and power dissipation, PDP with respect to the number of layers exhibits parabola, which is symmetric with the y-axis.

Optimum number of layers for all interconnect lengths is 10 to 15, for which optimum delay and power performances had obtained. Table-II indicates the power delay product of MLGNR interconnect for different interconnect layers varying from 4 to 40 and interconnect lengths are varying from 100 to 1000μm. Table-III demonstrates the improvement in propagation delay for MLGNR having N_{layer}=40 with respect to varying the layers from 4 to 35 and interconnect lengths are varying from 100 to 1000μm. For higher MLGNR layers and large interconnect lengths, more fruitful results have been found.





(e)

Fig. 3.3: Propagation delay and power dissipation with varying MLGNR layers at (a) 100μm (b) 300μm (c) 500μm (d) 800μm (e) 1000μm interconnect lengths

Table-3.2: Comparison of PDP for different MLGNR layers at global interconnect lengths

MLGNR layers	Power-delay product (in μW-ns) at different interconnect lengths of				
	L=100μm	L=300μm	L=500μm	L=800μm	L=1000μm
4	0.570	1.54	10.7	28.1	47.8
10	0.389	1.31	9.68	26.7	41.6
15	0.371	1.39	11.6	34.6	54.1
20	0.378	1.52	13.9	42.8	68.6
25	0.396	1.68	16.3	51.1	80.9
30	0.422	1.79	18.7	59.5	94.5
35	0.448	2.03	21.1	67.9	108.0
40	0.477	2.22	23.6	76.4	122.0

Table-3.3: Percentage improvement in propagation delay for higher number of MLGNR layers at global VLSI interconnects

MLGNR Lengths (μm)	% improvement in delay for MLGNR N_{layer}= 40 as compared to MLGNR with N_{layer}						
	4	10	15	20	15	25	35
100	17.81	4.30	2.61	1.25	0.61	0.26	0.06
300	21.00	6.84	3.26	1.57	0.69	0.34	0.04
500	28.95	10.12	4.91	2.37	1.07	0.38	0.07
800	46.12	19.03	9.72	4.84	2.81	1.13	0.38
1000	56.31	26.01	13.81	7.01	3.20	1.13	0.21

3.3 Crosstalk delay

In general, cross talk defined as undesirable coupling with electric and magnetic fields from adjacent interconnect wire to a network node causes an interference which consequences disturbance in other wires, which acts as a noise source and governs to intermittent errors. Tracing of these crosstalk-induced errors are difficult, since the added noise depends upon the transient value of the other signals routed in the neighborhood. In integrated circuits, this inter signal coupling can be both capacitive and inductive as shown in Fig. 3.5. Capacitive crosstalk is the dominant effect at current switching speeds, even though magnetic coupling forms a main concern in the design of the input-output circuitry of mixed-signal circuits. In ULSI circuits reliability, timing, and functionality are very crucial and these are significantly affected crosstalk noise.

3.3.1 Calculation of coupling parameters

In this research work, the crosstalk analysis and other performance with respect to the numbers of layers between two interconnect lines are analyzed. These two interconnect wires called as victim and aggressors. The mutual inductance (L_m) between two interconnect lines can be calculated by [25]

$$L_m = 2\times10^{-7} l\times\left[\ln\left(\frac{l}{a}+\sqrt{\left(\frac{l}{a}\right)^2+1}\right)+\frac{a}{l}-\sqrt{\left(\frac{a}{l}\right)^2+1}\right] \quad \text{If } a>3w \tag{16}$$

$$L_m = 2\times10^{-7} l\times\left[\ln\left(\frac{2l}{a}-1\right)\right] \quad \text{If } l>>a,\ a>3w \tag{17}$$

where l is the length of interconnects and a is the distance between the two interconnects middle points. In this case, the L_m is very low so neglecting in this analysis. The coupling capacitance (C_{CM}) demonstrates the crosstalk effect and can expressed as [25]

$$C_{CM} = \frac{0.5}{1+\left(S_{a-v}/(t+d)\right)^2} C_{[BCP]}\left(\frac{d}{S_{a-v}/2}, \frac{2t}{S_{a-v}/2}\right) + \frac{0.87}{1+\left(S_{a-v}/2(t+d)\right)} C_{[CP]}\left(\frac{w}{S_{a-v}}\right) \tag{18}$$

where $S_{a\text{-}v}$ spacing between aggressor and victim lines, C_{CP} capacitance between two co-planar plates, C_{BCP} represents the capacitance to ground of the bottom side of the layer, d is dielectric thickness and t is thickness of MLGNR interconnects [24]. The interconnect line in bus architecture can be either replaced by MLGNR multi-conductor transmission line model or ESC model. In this simulation setup CMOS inverter used as a driver for accurate

estimation of crosstalk delay. Below is shown two coupled line bus architecture has load capacitance C_L=10fF [25]. Crosstalk delay analyzed in the following two cases:

(1) In-phase delay

and (2) Out-phase delay

3.3.2 In-phase delay

The in-phase delay occurs in interconnects for the application same type of pulse signals means having same rise and fall times, pulse width, pulse period and having zero phase difference between them. In this case propagation delays occurred in both interconnects are same because two bus lines are excited by the same phase and equal amplitude so current carrying is same at equidistant points. Therefore, the effective coupling capacitance between two bus lines is zero.

3.3.3 Out-phase delay

The out-phase delay is the delay occurs in the interconnects for the application different type of input signals means having same rise and fall times, pulse width, pulse period and having 180 phase difference between them, that means if one rises another one falls and vice-versa. In this case two signals could not reach destination at same time, this case the maximum difference between cross talk delays will occurs moreover delays are increased as compared to in-phase case. Because of out-phase signals currents carrying in interconnect and fields also different so maximum effective coupling capacitance will occur. So here the worst-case delay is taken as out-phase delay. HSPICE simulations are used to examine the effect of crosstalk, for varying lengths of interconnect ranging from 100μm to 500μm with a step size of 100μm

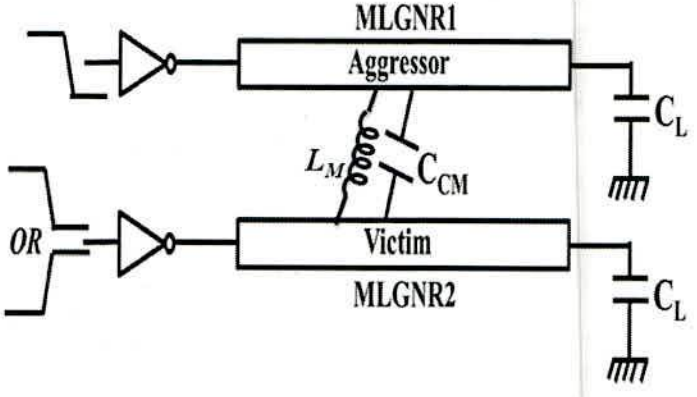
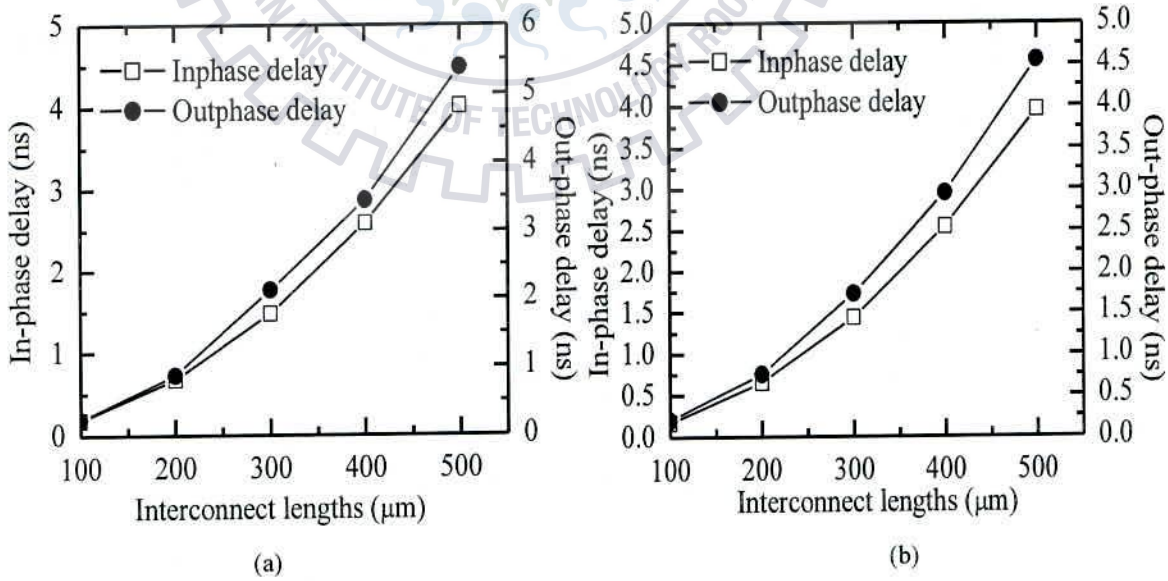


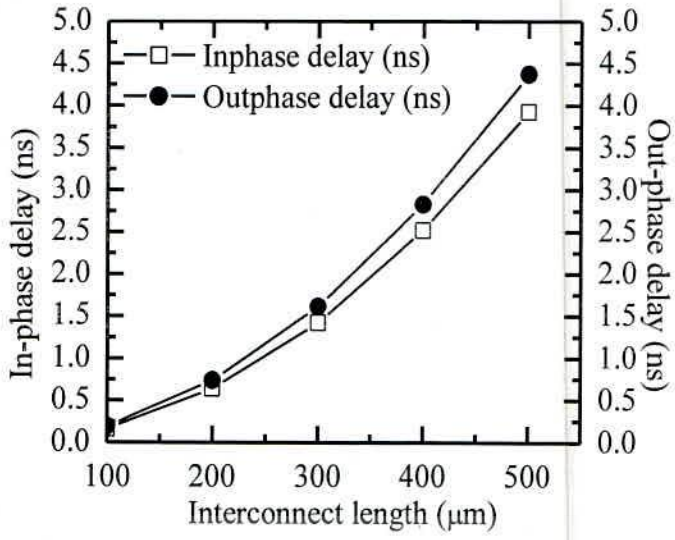
Fig. 3.4: Capacitive and inductive coupled MLGNR interconnects

Using DIL setup as in Fig. 3.4, for two parallel global MLGNR interconnects out-phase and in-phase delays (dynamic crosstalk delays) are accomplished using Hspice simulations by altering N_{layer} from 4, 10 and 20 for interconnect width of 50nm by varying interconnect lengths. It is noticed that the dynamic crosstalk delay deviations from out-phase to in-phase is more as for higher thickness compared to lower thickness. Generally interconnect delays increases with lengths in similar to that cross-talk delays are also increasing with lengths of interconnects.

3.3.4 Crosstalk analysis

Table 3.4 resumes the percentage of progress in crosstalk delays for MLGNR (N_{layer} = 20) *w.r.t.* MLGNR (N_{layer}=4, 10). It noticed that, crosstalk influenced propagation delay MLGNR has substantially improved for N_{layer}=20 even though the coupling is more for that thickness. Here it can notice that increasing interconnect lengths crosstalk delays also increasing. This fact realized by using the concept called area of field coupling. This coupling field area depends on thickness and length of interconnects. For increasing number of layers in MLGNR, the conducting channels also increases due to total conducting channels is directly proportional to number of layers. Thus, MLGNR with N_{layer} = 20 has higher effect in crosstalk as compared to with N_{layer} = 4 and 10. Below table-2 shows the crosstalk delay values for different lengths and thicknesses.





(c)

Fig. 3.5: Crosstalk delay of GNR with varying length at fixed interconnect layers (a) N_{layer} = 4(b) N_{layer} = 10 (c) N_{layer}=20

Table-3.4: Crosstalk delay for different interconnect lengths and thicknesses of MLGNR interconnects

Length of Interconnect (μm)	In-phase delay (ns)			Out-phase delay (ns)		
	N_{layers}=4	N_{layers}=10	N_{layers}=20	N_{layers}=4	N_{layers}=10	N_{layers}=20
100	0.18167	0.17035	0.16376	0.22436	0.19944	0.19119
200	0.67230	0.64975	0.63659	0.87115	0.75619	0.73697
300	1.4746	1.43829	1.4211	2.1214	1.7286	1.6109
400	2.5885	2.5436	2.5173	3.4518	2.9523	2.8230
500	4.0141	3.9581	3.9253	5.3813	4.5538	4.3733

CHAPTER-4

ANALYSIS OF RELATIVE STABILITY AND BANDWIDTH

4.1 Distributed transfer function of DIL system

Using the DIL setup, this section implements a transfer function (TF) for MLGNR and MWCNT interconnects that is used to find output responses in the time domain and it is used to find analytical expression for propagation delay. With the above TF, Bode and Nyquist plots can be found to analyze the bandwidths and stabilities of an interconnects. In DIL system interconnect is replaced with it's ESC model. To find the TF of a DIL setup primarily uses the transmission parametric matrices which are obtained from the equivalent *RLC* model of DIL system Fig. 4.1.

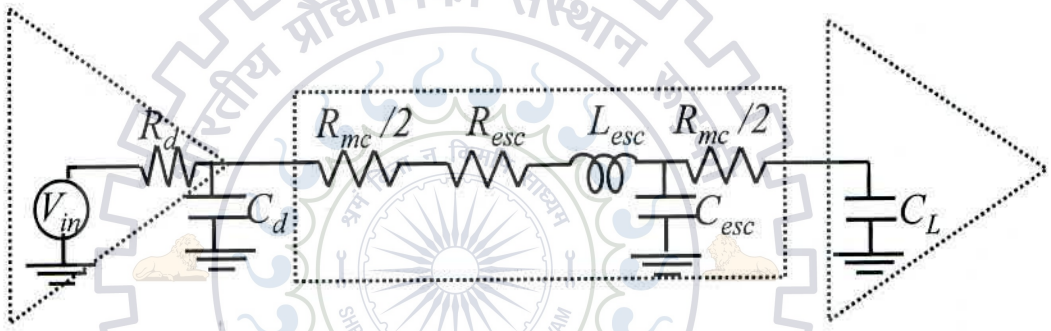


Fig. 4.1: Equivalent *RLC* configuration of DIL system.

Using telegraphers equation for transmission lines

$$\frac{\partial V}{\partial x} = -(R+sL)I(x) \qquad 19(a)$$

$$\frac{\partial I}{\partial x} = -(G+sC)\mathrm{V}(x) \qquad 19(b)$$

Differentiating above equation *w.r.t. x,* then above equations becomes

$$\frac{\partial^2 V}{\partial x^2} = (R+sL)(G+sC)\mathrm{V}(x) \qquad 20(a)$$

$$\frac{\partial^2 I}{\partial x^2} = (R+sL)(G+sC)\mathrm{I}(x) \qquad 20(b)$$

where G is transconductance, its value is very small can be neglected. Then the above equations becomes

$$\frac{\partial^2 V}{\partial x^2} = sC(R+sL)\mathrm{V}(x) \qquad 21(a)$$

$$\frac{\partial^2 I}{\partial x^2} = sC\left(R + sL\right)\mathrm{I}(x) \qquad 21(b)$$

$$\frac{\partial^2 V}{\partial x^2} = \gamma^2\,\mathrm{V}(x) \qquad 22(a)$$

$$\frac{\partial^2 I}{\partial x^2} = \gamma^2\,\mathrm{I}(x) \qquad 22(b)$$

where $\gamma^2 = sC(R + sL)$. The solution for above differential equations

$$V = V^+ e^{-\gamma x} + V^- e^{\gamma x} \qquad 23(a)$$

$$I = I^+ e^{-\gamma x} + I^- e^{\gamma x} \qquad 23(b)$$

Where $e^{\gamma x}$ component in above equation gives wave propagation in negative X direction, which means reflected wave component and it is very small and neglected. Then above voltage and current equations becomes

$$V = V_0 e^{-\gamma x} \qquad 24(a)$$

$$I = I_0 e^{-\gamma x} \qquad 24(b)$$

For interconnect length of l the above equation becomes, multiplication of $n=l/x$ times of above equations

$$V = V_0 e^{-n\gamma x} \qquad 25(a)$$

$$I = I_0 e^{-n\gamma x} \qquad 25(b)$$

To make the analytical derivation for transfer function easy, the above expressions 25(a) and 25(b) simplified to

$$V = V_0 \cosh(\gamma nx) - V_0 \sinh(\gamma nx) \qquad 26(a)$$

$$I = I_0 \cosh(\gamma nx) - I_0 \sinh(\gamma nx) \qquad 26(b)$$

After simplification of above equation

$$V = V_0 \cosh(\gamma nx) + I_0 Z_0 \sinh(\gamma nx) \qquad 27(a)$$

$$I = I_0 \cosh(\gamma nx) + V_0 / Z_0 \sinh(\gamma nx) \qquad 27(b)$$

$$\begin{bmatrix} V \\ I \end{bmatrix} = \begin{bmatrix} \cosh(\gamma nx) & Z_0 \sinh(\gamma nx) \\ 1/Z_0 \sinh(\gamma nx) & \cosh(\gamma nx) \end{bmatrix} \begin{bmatrix} V_0 \\ I_0 \end{bmatrix} \qquad (28)$$

The resultant transmission line matrix becomes

$$T_{effect} = \begin{bmatrix} 1 & R_{dr} \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ sC_{dr} & 1 \end{bmatrix}\begin{bmatrix} 1 & R_1 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} \cosh(\gamma nx) & Z_0\sinh(\gamma nx) \\ 1/Z_0 \sinh(\gamma nx) & \cosh(\gamma nx) \end{bmatrix}\begin{bmatrix} 1 & R_1 \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \quad (29)$$

$$A = (1+sR_{dr}C_{dr})\cosh(\gamma x) + \left(R_1(1+sR_{dr}C_{dr})+R_{dr}\right)\frac{\sinh(\gamma nx)}{Z_0} \quad 29(a)$$

$$B = R_1\left((1+sR_{dr}C_{dr})\cosh(\gamma nx)+\left(R_1(1+sR_{dr}C_{dr})+R_{dr}\right)\frac{\sinh(\gamma nx)}{Z_0}\right) + Z_0\sinh(\gamma nx)(1+sR_{dr}C_{dr}) \quad 29(b)$$
$$+\left(R_1(1+sR_{dr}C_{dr})+R_{dr}\right)\cosh(\gamma nx)$$

$$C = sC_{dr}\cosh(\gamma nx) + \left(sR_1C_{dr}+1\right)\frac{\sinh(\gamma nx)}{Z_0} \quad 29(c)$$

$$D = R_1\left(sC_{dr}\cosh(\gamma nx) + (1+sR_{dr}C_{dr})\frac{\sinh(\gamma nx)}{Z_0}\right) + \left(Z_0 sC_{dr}\sinh(\gamma nx) + (1+sR_{dr}C_{dr})\cosh(\gamma nx)\right) \quad 29(d)$$

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}\begin{bmatrix} V_{out} \\ -I_{out} \end{bmatrix} \quad (30)$$

$$\frac{V_{out}}{V_{in}} = TF = \frac{1}{A+sC_LB} \quad (31)$$

where $I_{out} = -\frac{1}{sC_L}V_{out}$. To find transfer function of driver interconnect load system A and B values are necessary, so simplified A and B values as represnted as shown equation below

$$A = 1 + s\left[\frac{RC(nx)^2}{2!} + R_{dr}C_{dr} + C(nx)(R_1+R_{dr})\right] + s^2\left[\frac{LC(nx)^2}{2!} + \frac{R^2C^2(nx)^4}{4!} + \frac{RR_{dr}CC_{dr}(nx)^2}{2!} + \frac{RC^2(nx)^3(R_1+R_{dr})}{3!}\right.$$
$$\left. + R_1R_{dr}C_{dr}C(nx)\right] + s^3\left[\frac{2RLC^2(nx)^4}{4!} + \frac{R^3C^3(nx)^6}{6!} + R_{dr}C_{dr}\left(\frac{LC(nx)^2}{2!} + \frac{R^2C^2(nx)^4}{4!}\right) + \left(R(nx)+R_{dr}\right)\right.$$
$$\left.\times\left(\frac{LC^2(nx)^3}{3!} + \frac{R^2C^3(nx)^5}{5!}\right) + \frac{RR_1R_{dr}C_{dr}C^2(nx)^3}{3!}\right] + s^4\left[\frac{L^2C^2(nx)^4}{4!} + \frac{3R^2LC^2(nx)^5}{6!} + \frac{R^4C^4(nx)^8}{8!} + R_{dr}C_{dr}\right.$$
$$\left.\times\left(\frac{2RLC^2(nx)^4}{4!} + \frac{R^3C^3(nx)^6}{6!}\right) + \left(R(nx)+R_{dr}\right)\left(\frac{2RLC^3(nx)^5}{5!} + \frac{R^3C^4(nx)^7}{7!}\right) + R_1R_{dr}C_{dr}\left(\frac{LC^2(nx)^3}{3!} + \frac{R^2C^3(nx)^5}{5!}\right)\right]$$

$$B = \left(2R_1 + R_{dr} + R\right) + s\left[\frac{RC}{2!}\left(2R_1+R_{dr}\right) + 2R_1R_{dr}C_{dr} + \frac{R^2C}{3!} + L + R_1{}^2C + RR_{dr}C_{dr} + R_1R_{dr}C\right]$$
$$+ s^2\left[\left(2R_1+R_{dr}\right)\left(\frac{LC}{2!}+\frac{R^2C^2}{4!}\right) + R_1R_{dr}RCC_{dr} + \frac{2RLC}{3!} + \frac{R^3C^2}{5!} + \frac{R_1{}^2RC^2}{3!} + \frac{R^2R_{dr}C_{dr}C}{3!} + \frac{RR_1R_{dr}C^2}{3!}\right.$$
$$\left. + R_{dr}C_{dr}\left(L + R_1{}^2C\right)\right] + s^3\left[\left(2R_1+R_{dr}\right)\left(\frac{2RLC^2}{4!}+\frac{R^3C^3}{6!}\right) + 2R_1R_{dr}C_{dr}\left(\frac{LC}{2!}+R^2C^2\right) + \frac{2R^2LC^2}{5!} + \frac{R^4C^3}{7!}\right.$$
$$\left. + \left(L + R_1{}^2C + R_{dr}C_{dr}R + R_1R_{dr}C\right)\left(\frac{LC}{3!} + \frac{R^2C^2}{5!}\right) + \frac{RR_{dr}C_{dr}C}{3!}\left(L + R_1{}^2C\right)\right]$$

General fourth order transfer function of distributed driver interconnect load system is

$$TF = \frac{1}{a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4 + a_5 s^5 + a_6 s^6} \tag{32}$$

where $a_0 = 1$,

$$a_1 = \left(\frac{RC(nx)^2}{2!} + R_{dr}C_{dr} + C(nx)(R_1 + R_{dr}) \right) + C_L \left(2R_1 + R_{dr} + R(nx) \right)$$

$$a_2 = \left(\frac{LC(nx)^2}{2!} + \frac{R^2C^2(nx)^4}{4!} + \frac{RR_{dr}CC_{dr}(nx)^2}{2!} + \frac{RC^2(nx)^3(R_1 + R_{dr})}{3!} + R_1 R_{dr} C_{dr} C(nx) \right)$$
$$+ C_L \left(\frac{RC}{2!}\left(2R_1 + R_{dr}\right) + 2R_1 R_{dr} C_{dr} + \frac{R^2 C}{3!} + L + R_1{}^2 C + RR_{dr}C_{dr} + R_1 R_{dr} C \right)$$

$$a_3 = \left[\frac{2RLC^2(nx)^4}{4!} + \frac{R^3C^3(nx)^6}{6!} + R_{dr}C_{dr}\left(\frac{LC(nx)^2}{2!} + \frac{R^2C^2(nx)^4}{4!} \right) + \left(R(nx) + R_{dr} \right) \right.$$
$$\left. \times \left(\frac{LC^2(nx)^3}{3!} + \frac{R^2C^3(nx)^5}{5!} \right) + \frac{RR_1R_{dr}C_{dr}C^2(nx)^3}{3!} \right] + C_L \left[\left(2R_1 + R_{dr}\right)\left(\frac{LC}{2!} + \frac{R^2C^2}{4!} \right) + \right.$$
$$\left. + R_1 R_{dr} RCC_{dr} + \frac{2RLC}{3!} + \frac{R^3C^2}{5!} + \frac{R_1{}^2RC^2}{3!} + \frac{R^2R_{dr}C_{dr}C}{3!} + \frac{RR_1R_{dr}C^2}{3!} + R_{dr}C_{dr}\left(L + R_1{}^2C \right) \right]$$

$$a_4 = \left[\frac{L^2C^2(nx)^4}{4!} + \frac{3R^2LC^2(nx)^5}{6!} + \frac{R^4C^4(nx)^8}{8!} + R_{dr}C_{dr}\left(\frac{2RLC^2(nx)^4}{4!} + \frac{R^3C^3(nx)^6}{6!} \right) \right.$$
$$\left. + \left(R(nx) + R_{dr} \right)\left(\frac{2RLC^3(nx)^5}{5!} + \frac{R^3C^4(nx)^7}{7!} \right) + R_1 R_{dr} C_{dr}\left(\frac{LC^2(nx)^3}{3!} + \frac{R^2C^3(nx)^5}{5!} \right) \right]$$
$$+ C_L \left[\left(2R_1 + R_{dr}\right)\left(\frac{2RLC^2(nx)^4}{4!} + \frac{R^3C^3(nx)^6}{6!} \right) + 2R_1 R_{dr} C_{dr}\left(\frac{LC(nx)^2}{2!} + R^2C^2(nx)^4 \right) + \frac{2R^2LC^2(nx)^5}{5!} \right.$$
$$\left. + \frac{R^4C^3(nx)^7}{7!} + + \left(L(nx) + R_1{}^2C(nx) + R_{dr}C_{dr}R(nx) + R_1R_{dr}C(nx) \right)\left(\frac{LC(nx)^2}{3!} + \frac{R^2C^2(nx)^4}{5!} \right) \right.$$
$$\left. + \frac{RR_{dr}C_{dr}C(nx)^2}{3!}\left(L(nx) + R_1{}^2C(nx) \right) \right]$$

$$a_5 = \left[R_{dr}\left(C_{dr} + C_L \right) + 2R_1C_L \right] \times \left(\frac{L^2C^2(nx)^4}{4!} + \frac{3R^2LC^3}{6!} + \frac{R^4C^4(nx)^8}{8!} \right) + 2R_{dr}R_1C_{dr}C_L$$
$$\times \left(\frac{2RLC^2(nx)^4}{4!} + \frac{R^3C^3(nx)^6}{6!} \right) + \left(R_{dr}R_1\left(C_{dr} + C_L \right) + R_1^2C_L + \frac{RR_{dr}C_{dr}C_L}{C} \right)$$
$$\times \left(\frac{2RLC^3(nx)^5}{5!} + \frac{R^3C^4(nx)^7}{7!} \right) + \left(R_{dr}R_1{}^2C_{dr}C_L + \frac{LR_{dr}C_{dr}C_L}{C} \right)\left(\frac{LC^2(nx)^3}{3!} + \frac{R^2C^3(nx)^5}{5!} \right)$$

$$a_6 = 2R_{dr}R_1C_{dr}C_L\left(\frac{L^2C^2(nx)^4}{4!}+\frac{3R^2LC^3(nx)^6}{6!}+\frac{R^4C^4(nx)^8}{8!}\right)+\left(R_{dr}R_1^2C_{dr}C_L+\frac{LR_{dr}C_{dr}C_L}{C}\right)$$
$$\times\left(\frac{2RLC^3(nx)^5}{5!}+\frac{R^3C^4(nx)^7}{7!}\right)$$

To find analytical equation for output and bandwidth/cutoff frequency of driver interconnect load system, the transfer function (32) reduced to second order as in (33),

$$TF = \frac{1}{a_0 + a_1 s + a_2 s^2} \tag{33}$$

where a_0=1, then roots of above expression is

$$s_1 = \frac{-a_1 + \sqrt{a_1^2 - 4a_2}}{2a_2} \text{ and } s_2 = \frac{-a_1 - \sqrt{a_1^2 - 4a_2}}{2a_2} \tag{34}$$

Insignificant time delay is the for which has lower time constant $\tau_2 = \frac{2a_2}{-a_1 - \sqrt{a_1^2 - 4a_2}}$ which doesn't affect the output response of system much and dominant time delay has higher time constant which majorly affects the output response of driver interconnect load system and its value $\tau_1 = \frac{2a_2}{-a_1 + \sqrt{a_1^2 - 4a_2}}$. Output voltage expression for second order transfer function for given input of raising pulse from 0V to 1V, having a raise time of 1ps is given in below expression (35)

$$V_{out} = \frac{10^{12}}{a_2}\left[-\tau_1\tau_2\left(\tau_1+\tau_2\right)+\tau_1\tau_2 t+\frac{\tau_1^3\tau_2}{\tau_1-\tau_2}e^{-t/\tau_1}\right] \tag{35}$$

Bandwidth/cutoff frequency calculated using expression (36)

$$f_c = \frac{1}{2\pi}\sqrt{\frac{(2a_2 - a_1^2) + \sqrt{(2a_2 - a_1^2)^2 + 4a_2^2}}{2a_2^2}} \tag{36}$$

4.2 Comparison of MLGNR and MWCNT

4.2.1 Bandwidths

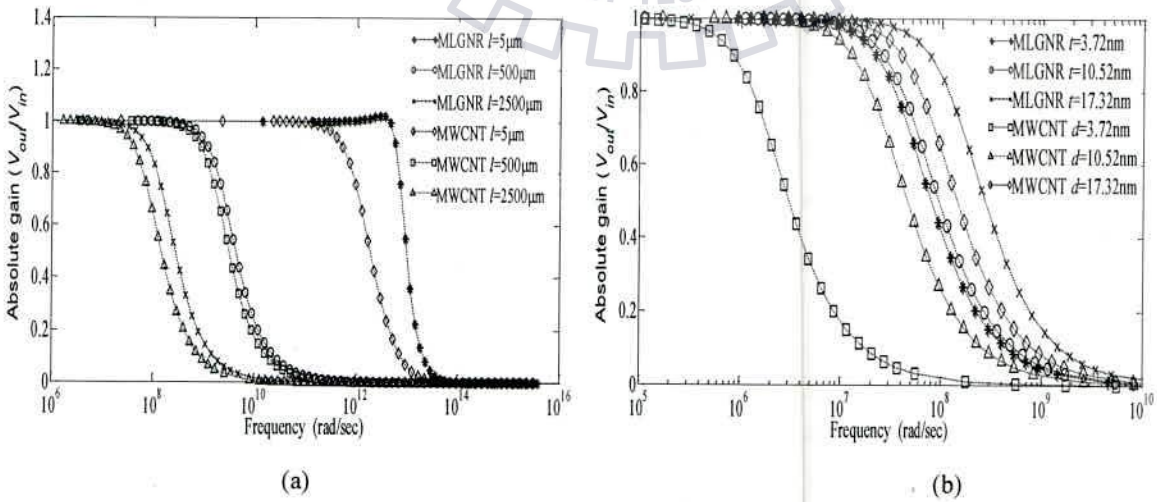
The TF is used to calculate the bandwidth of MLGNR and Cu interconnects that can be defined as the range of frequencies for which output signal is reconstructed without loosing information. The dominating parameters of C_{esc} and R_{esc} in MLGNR and Cu leads to form an RC low pass filter that has a cutoff frequency approximates to $f_c = 1/2\pi R_{esc}C_{esc}$.

The expression for transfer function (32) utilized to analyze the cutoff frequency (f_c) that depends on the parasitics of the MLGNR/ MWCNT interconnects as presented in Table VII. The parasitics evaluated for the equivalent diameter of MWCNT and thickness of MLGNR. The geometry of MWCNT and MLGNR is as shown in 2.3 (a) is conceived as above ground having a fixed d and ε_r of 50nm and 2.2 respectively. A comparative analysis of bandwidth (BW) is persuaded by altering interconnect lengths (l) and widths (w) as presented in Figs. 4.2(a) and (b)respectively using expression (22). Irrespective of interconnects lengths and widths, it is observed that the MLGNR demonstrates a higher bandwidth in contrast to the MWCNT interconnects. The reason behind this is that the dominating parasitic C_{esc} of MWCNT causes a lower value of f_c in comparison to MLGNR as presented in Table 4.1.

$$f_c = \frac{1}{2\pi\left[\left(\frac{RC(nx)^2}{2!}+R_{dr}C_{dr}+C(nx)(R_1+R_{dr})\right)+C_L(2R_1+R_{dr}+R(nx))\right]} \tag{37}$$

Table 4.1: MWCNT and MLGNR interconnects equivalent unit length parasitics

Interconnect parasitic	Quantitative values of parasitic for equivalent thickness and diameter of	
	MLGNR	MWCNT
R'_{esc} (Ω/μm)	149.99	21.10
L'_{esc} (nH/μm)	0.098	0.057
C'_{esc} (aF/μm)	6.739	89.781



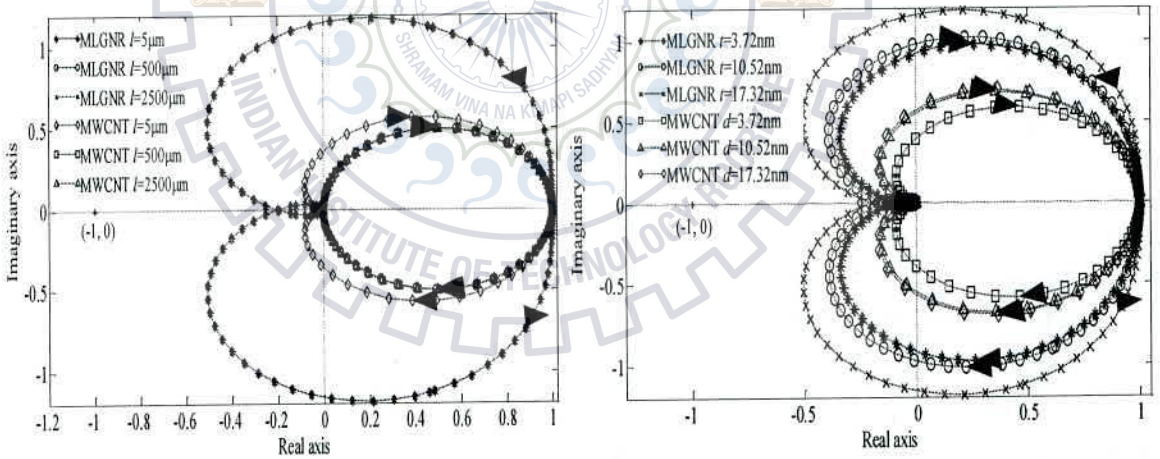
(a) (b)

Fig. 4.2: Absolute gain response of MLGNR and MWCNT for different *(a)* interconnect lengths (l) at t = 17.32nm *(b)* interconnect widths (w) at l = 2500μm

4.2.2 Relative stability

What is system stability? For the application of bounded inputs, the response of system should be a bounded then that system called as stable system. This stability depends on the inputs and disturbances present inside the system. The relative stability concept arises for comparison of stability of two stable systems. A system having higher switching delay and lower peak over shoot system is relatively more stable as compared to other [31]. The Table-4.2 presents the output rise time and percentage peak overshoot for different diameters and thickness of MLGNR and MWCNT at different interconnect lengths. The values of percentage peak overshoot and output rise time mainly influenced by the damping coefficient (ξ), which increases for higher values of interconnect parasitics at semi-global (l=500μm) and global interconnect lengths (l=2500μm) as denoted in (38). For local interconnect lengths (l=5μm), the lower quantitative values of parasitics diminishes the value of ξ lesser than 1, which results under-damped condition. The as the damping factor decreases further, results in increase in peak overshoot at output that effects lower system stability.

$$\xi = 0.5(1+C_L/C'_{esc}l)^{1/2}\left[\left(0.5R'_{esc}l+2R_c+R_{dr}\right)\left(\sqrt{C'_{esc}/L'_{esc}}\right)+\left(R'_{esc}l+2R_c+R_{dr}\right)\sqrt{C_L^2/L'_{esc}C'_{esc}l^2}\right] \quad (38)$$



(a) (b)

Figs. 4.3: Nyquist plots of MLGNR and MWCNT interconnects for different *(a)* interconnect lengths (l) at t = 17.32nm *(b)* interconnect widths (w) at l = 5μm

Employing the Nyquist plots in Figs. 4.3(a) and 4.3(b) illustrates relative stability of MLGNR and MWCNT for different interconnect lengths and widths. It noticed that intersection points on X-axis in Figs. 4.3(a) and 4.3(b) moves away from the critical point (-1, 0) for increasing interconnect lengths that results greater system stability. By the observation

of Fig 4.5 (a), MLGNR stability relatively lower in compared to MWCNT at local interconnect lengths which can be described using the lower equivalent capacitance of MLGNR as compared to MWCNT as denoted in Table 4.2. The lower value of capacitive parasitic substantially decreases the value of ξ that demonstrates lower system stability for MLGNR in comparison to MWCNT interconnects.

Table 4.2: Percentage Peak Overshoot (Mp) and Switching Delay (T_r) for the equivalent diameter of MWCNT and thickness of MLGNR

Length l (μm)	Thickness (nm)	MLGNR		MWCNT	
		M_P (%)	T_r (ns)	M_P	T_r (ns)
5	3.72	5.86	0.0006	0	0.0867
	10.52	12.8	0.0003	0	0.0058
	17.32	19.7	0.0002	0.1	0.0015
500	3.72	0	3.05	0	50.1
	10.52	0	1.63	0	3.46
	17.32	0	0.57	0	1.51
2500	3.72	0	75.4	0	1250
	10.52	0	40.3	0	83
	17.32	0	14.0	0	27.7

4.3 Comparison of MLGNR and Cu

Previous theoretical simulations, it has been predicted that undoped GNRs will outperform the Cu interconnects for smaller widths less than 8nm whereas for doped MLGNR shows much better performance for all thickness and widths due to higher conducting channels (N_{ch}). For deep submicron and nano-scale device dimensions, sidewalls scatterings and grain boundary scatterings are most prominent in Cu interconnects which will affect the performance of Cu interconnects. Using the similar width (w), thickness (t) and length (l) for MLGNR and Cu interconnects, here illustrated a comparative analysis to address the effect of propagation delay and power dissipation.

4.3.1 Delay and power

The DIL system as in Fig. 2.5 is used to measure the power dissipation and propagation delay of MLGNR and Cu interconnects. The equivalent single conductor model MLGNR and corresponding *RLC* model Cu represents the interconnect line in DIL system. For a CMOS driver supplied voltage is 1V and given a input signal of 1V having a rise time

of 10ps used to drive the interconnect line, which has a load capacitance of 10aF. Using the above-mentioned setup, power dissipation and propagation delay performances are compared by altering interconnect lengths from 100μm to 1000μm.

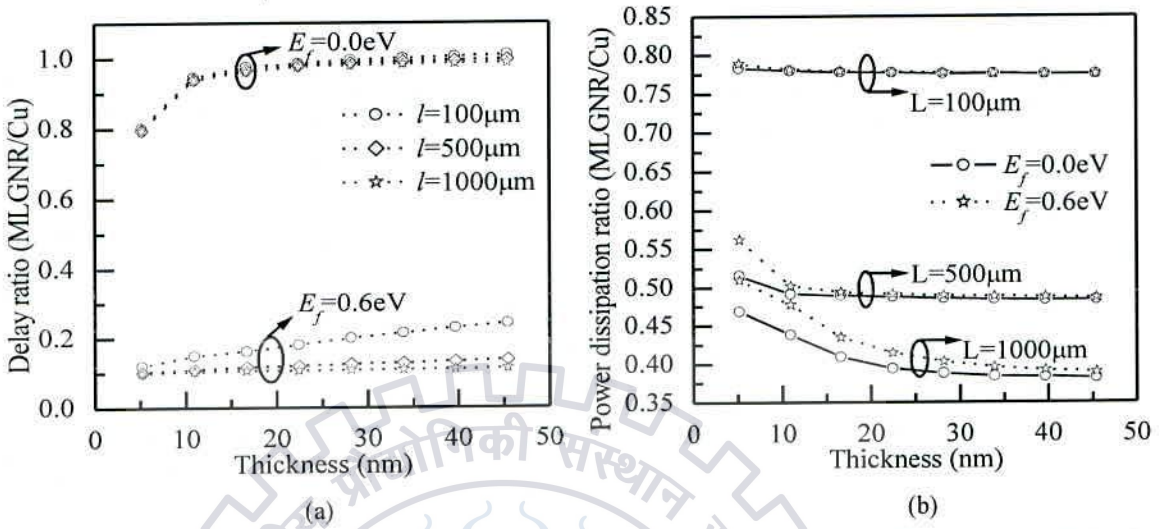


Fig. 4.4: MLGNR to Cu (a) delay and (b) power dissipation ratios at global interconnect lengths for altering thickness.

Table-4.3: Delay and power dissipation improvement in for doped MLGNR as compared to Cu interconnects

Thickness (nm)	% improvement in delay for			% improvement in power for		
	100μm	500μm	1000μm	100μm	500μm	1000μm
5.75	88.01	89.79	90.11	49.39	49.39	54.04
11.50	85.13	88.97	89.61	50.93	50.93	57.17
17.25	83.78	88.44	89.42	51.12	51.12	59.14
23.00	81.91	87.98	89.27	51.32	51.32	60.61
28.75	80.05	87.53	89.15	51.47	51.47	61.21
34.50	78.46	87.10	89.04	51.57	51.57	61.57
40.25	77.11	86.67	88.92	51.66	51.66	61.72
46.00	75.76	86.25	88.82	51.69	51.69	61.81

Figs. 4.4(a) and 4.4(b) shows the ratio of neutral and doped MLGNR with Cu delay and power dissipation ratios for varying thickness. It is observed that the MLGNR to Cu delay and power ratio reduces at higher interconnect lengths and it varies negligibly with variation in thickness. Additionally, the delay and power ratios are considerably reduced for doped MLGNR as shown in Fig. 4.4(a) and Fig. 4.4(b) respectively. The reason behind this reduction is the lower resistive and capacitive parasite that has a significant effect in delay

and power dissipation. At higher doping concentration, the number of conducting channels in MLGNR increases due to the increasing carrier density in each layer of MLGNR.

The higher number of conducting channels considerably reduces the equivalent resistance and inductance values whereas dominating electrostatic capacitance is constant. Therefore, a doped MLGNR interconnects results in least delay and power consumption as compared to Cu interconnects. Table 4.3 shows the development in delay and power dissipation in percentage, MLGNR as compared to Cu at different interconnect lengths. It is observed that for a doped MLGNR, the overall power dissipation and propagation delay performances are improved by 43.72%and 86.13% respectively as compared to the Cu interconnects.

4.3.2 Performance comparison in frequency domain

Transfer function (TF) of DIL configuration in frequency-domain has presented based on a rigorous analysis of the transmission parameters. Performances of DIL system not only depend on interconnect parasitics but also substantial dependence on driver parasitics, which has series resistance and output parasitic capacitance. Using transfer function, here analyzed bandwidths of MLGNR and Cu for different interconnect lengths, widths and thickness. MLGNR showed much better bandwidth as compared to Cu because of its lower *RLC* parasitic values. In transient response, the output voltage that exceeds the steady state (final value) during their rise and fall transitions referred as overshot. This overshoot represents a distortion in signal, using Nyquist criterion it used to find relative stabilities of MLGNR interconnects which tells distortion in output signal.

The open loop TF in equation (22) is used to calculate the absolute frequency response by assuming fixed d=50nm, l=1000μm, w=10nm and t=28.2nm for MLGNR and Cu interconnects. Fig. 4.5(a) shows the absolute gain response of doped MLGNR and Cu interconnects for different frequency and interconnect lengths ranging from 5μm to 2500μm. It is observed that the doped MLGNR exhibits a significant improvement of 3dB bandwidth in comparison to Cu at global lengths. The reason for this improvement can be explained as, lower resistive and capacitive parasitics of doped MLGNR that significantly increases the cutoff frequency (f_c).

For different widths, Fig. 4.5(b) exhibits the absolute gain response that specifies an insignificant improvement in 3dB frequency for doped MLGNR for increasing widths due to the reduction in equivalent scattering resistance is compensated by increase in electrostatic capaciatnce. Whereas in case of Cu for increasing widths the reduction in scattering

resistance is much higher as compared to electrostatic capacitance due to surface and edge scattering diminishes for larger widths.

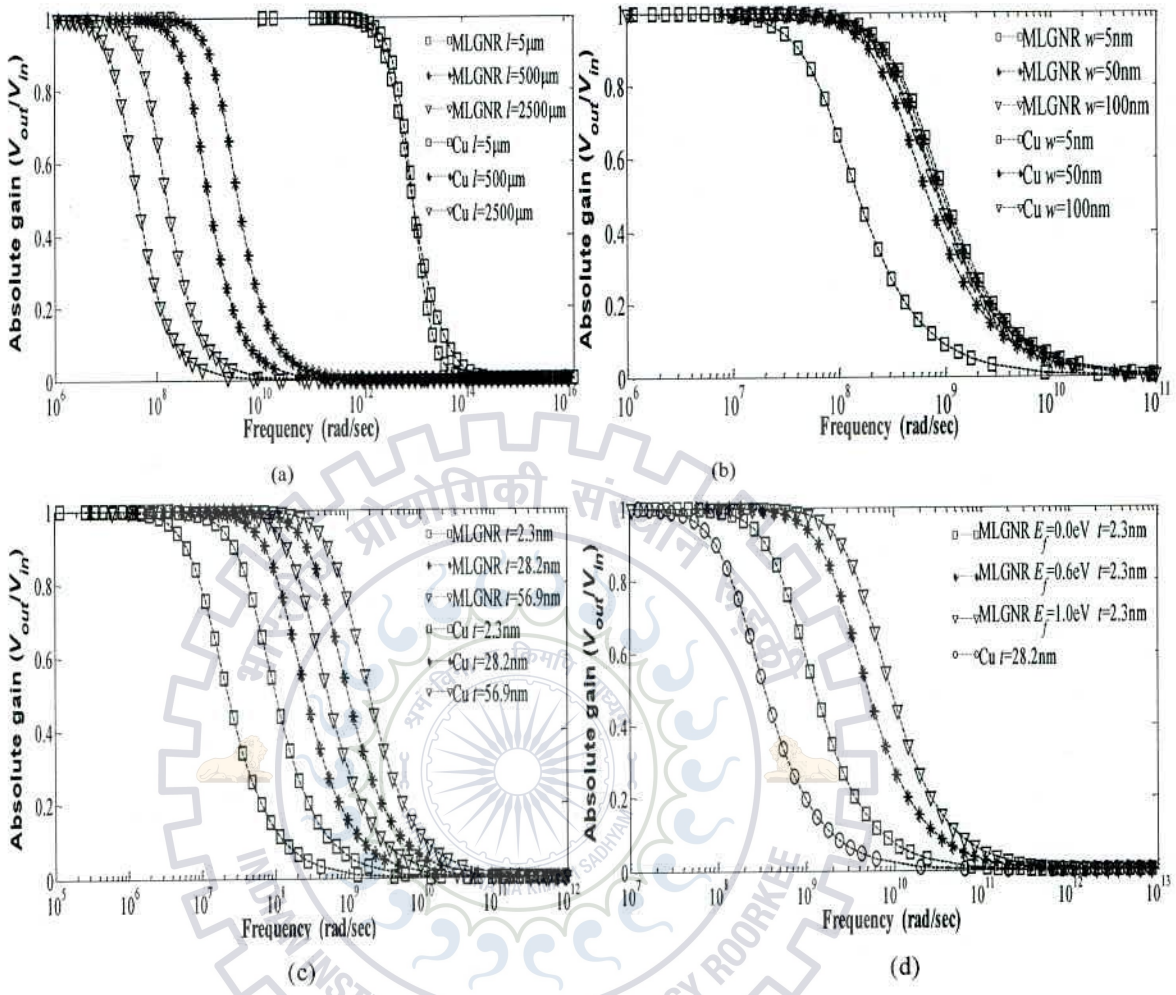


Fig. 4.5: Absolute gain response of doped MLGNR and Cu interconnects for different (a) lengths, (b) widths, (c) thickness and (d) doping density.

Fig. 4.5 (c) and Fig. 4.5 (d) illustartes that absolute gain response for increasing thickness and doping density of MLGNR and Cu interconnects. For higher thickness and doping density, a doped MLGNR exhibits a considerable improvement in 3dB bandwidth as compared to Cu interconnects. With an increasing thickness and doping density, the quantitative value of N_{ch} in doped MLGNR increases which in turn reduces the R_{esc} with a constant value of C_{esc}. Therefore, the f_c is considerably increased for lower values of R_{esc} and C_{esc} associated with doped MLGNR interconnects. Thus, for higher thickness and doping, MLGNR interconnects exhibits a considerable improvement in bandwidth as compared to Cu interconnects.

4.4 Relative stability analysis of MLGNR interconnects

Nyquist plot is a parametric plot of a transfer function, which used to examine the relative stability in signal transmission analysis. Stability is determined by using the number of encirclements of the point at (-1, 0) [31]. Using the Nyquist plot, this section demonstrates the relative stability of doped MLGNR for different interconnect lengths (l), widths (w), thickness (t) and doping density (E_f) as indicated in Figs. 4.6(a), 4.6(b), 4.6(c) and 4.6(d) respectively.

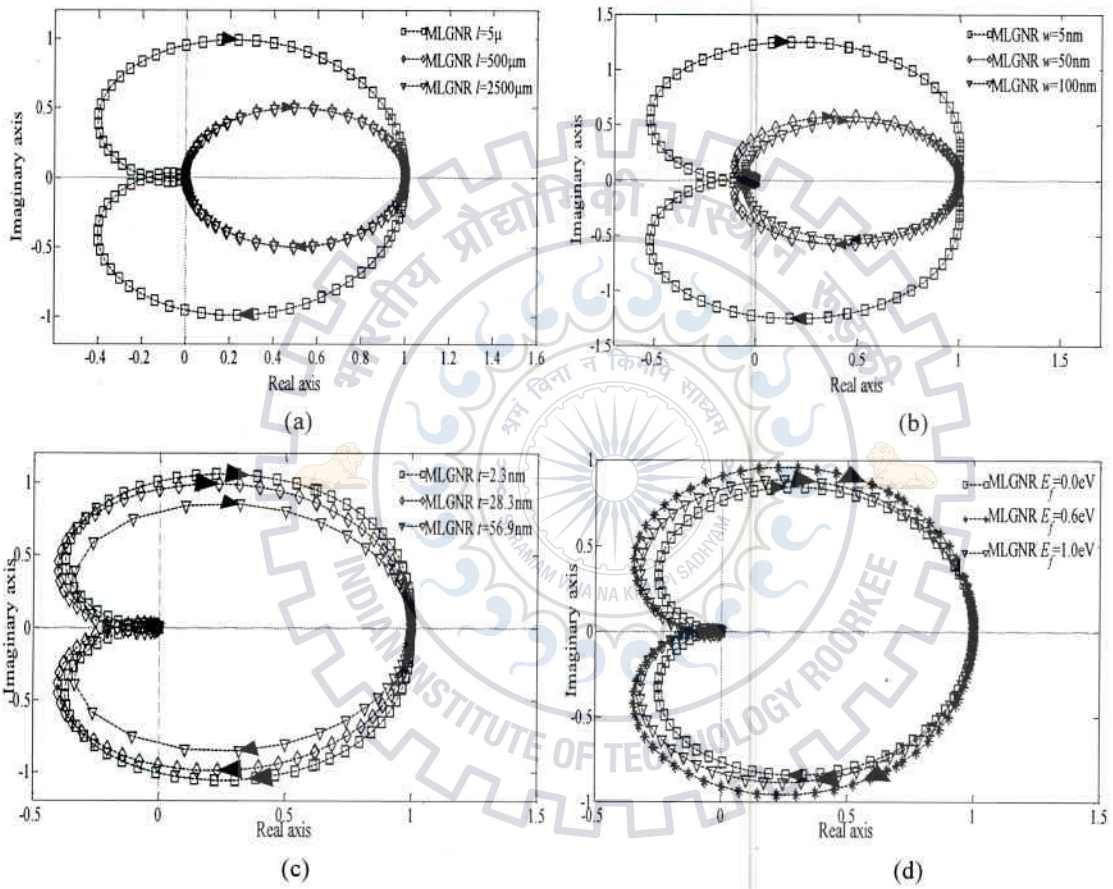


Fig. 4.6: Nyquist plots of doped MLGNR interconnect for different (a) lengths, (b) widths, (c) thickness and (d) doping density.

It is noticed that the encirclements are moving away from (-1, 0) for higher interconnect lengths which in turn increases the system stability. A system considered as stable for higher output switching delay (T_r) and zero peak overshoot voltage (M_p) as indicated in Table 4.4, due to output damps much faster before it it reaching steady state value. The quantitative values of T_r and M_p primarily depends on the damping factor (ξ) that increases for higher quantitative values of interconnect parasitics at global interconnect

lengths (l=2500μm). For local interconnect lengths (l=5μm), the lower parasitics reduces the value of T_r that results in a lower value of ξ less than 1. The least value of ξ is responsible for lower stability of the system as it possess the under-damped condition. The time response of under-damped system exhibits exponentially decaying oscillations before reaching to the steady state value.

Table-4.4: Switching delay (T_r) and % peak overshoot (M_p) at different interconnect lengths

Constant parameter	Value of parameter	T_r (in ps) for		% M_P for	
		l=5μm	l=1000μm	l=5μm	l=1000μm
Widths	5nm	0.105	762	22.5	0
	50nm	0.386	801	0.0	0
	100nm	0.749	867	0.0	0
Thickness	2.3nm	0.306	744	15.2	0
	28.2nm	0.108	757	11.1	0
	56.9nm	0.096	385	4.0	0
Doping level	0eV	0.239	890	11.1	0
	0.6eV	0.108	757	7.04	0
	1eV	0.096	414	4.8	0

CHAPTER-5

PROCESS VARIATION EFFECTS ON MLGNR PERFORMANCE

The performance of integrated circuits (ICs), adversely affected due to the shrinking device dimensions of 32nm or below. During the manufacturing process, the circuit performance becomes less predictable due to the poor control in physical parameters and geometrical characteristics. Uncertainties due to the variations in fabrication process reflected in variations of circuit parameters. Examples of the manufacturing variation are the variation in geometrical process such as width, dielectric thickness, dielectric constant, doping concentration etc for a multi-layer graphene nanoribbon (MLGNR) interconnects.

5.1 Modeling of process induced parameters variation

This chapter analyzes, deformations in interconnect due to process variations in manufacturing process can lead to significant performance degradation in ULSI circuits due to the variability of some geometrical quantities. In specific, the variability of the nano-wire w, d, Fermi energy due to doping density variations, d, R_c, ε_r and interlayer distance of the external medium are considered. The cross-sectional geometry of doped MLGNR interconnect is positioned above a conducting ground plane they are detached by a linear dielectric material, having relative permittivity ε_r as shown in Fig. 2.5.

5.2 Analysis of performance deviations

This section primarily presents process variation effects on MLGNR interconnects to state the effect of delay at different interconnect lengths and widths using Monte Carlo simulations. Using DIL setup, having a CMOS driver, the nominal values of the propagation delays, in addition to this worst and best case deviations with respect to nominal delays in relation to of the interconnect length and widths are found. In this way, it is achieved that relative robustness of the doped MLGNR interconnects is quantified as an indication that, at which dimensions variation in propagation delay less sensitive to the process variations. Analysis of 90% delay performances for MLGNR interconnects with different number of layers for varying lengths from local to global ranging from 5μm to 2500μm by using the geometries

suggested in Fig. 2.3 (a). Simulation setup uses a driver-interconnect-load (DIL) system employing CMOS driver at 32nm technology node for accurate estimation of delay, the supply voltage of 1V and it terminated with a load capacitance C_L of 1fF as shown in Fig. 2.5.

Table-5.1: Percentage of variation of parameters and their ranges

Name of parameter	Notation	Nominal value	Variation	Minimum value	Maximum value
Width (nm)	W	25	±10%	22.5	27.5
Dielectric thickness (nm)	D	200	±10%	180	220
Relative permittivity	ε_r	2.2	±10%	2.0	2.4
Contact resistance (kΩ)	R_c	3.2	±50%	1.6	4.8
Doping variation (eV)	E_f	0.6	±10%	0.54	0.66
Mean free path (μm)	λ_{mfp}	1.04	±50%	0.52	1.56

Table-5.2: *p.u.l.* parasitic variations in MLGNR interconnects in indvidual parameter variation

Variation of parameters →		Width	Fermi Energy	Dielectric Thickness	Dielectric Constant	Mean free Path
R_q(ohm)	*Nominal*	356.9985	356.9985	356.9985	356.9985	356.9985
	Max	396.5991	398.6079	356.9985	356.9985	356.9985
	Min	324.5729	322.6587	356.9985	356.9985	356.9985
R_s(ohm)	*Nominal*	686.5356	686.5356	686.5356	686.5356	686.5356
	Max	762.6906	766.5536	686.5356	686.5356	1373.071
	Min	624.1787	620.4975	686.5356	686.5356	457.6904
L_k(nH)	*Nominal*	0.442789	0.442789	0.442789	0.442789	0.442789
	Max	0.491906	0.494397	0.442789	0.442789	0.442789
	Min	0.402571	0.400197	0.442789	0.442789	0.442789
L_e(pH)	*Nominal*	2.51	2.51	2.51	2.51	2.51
	Max	2.79111	2.51	2.7632	2.51	2.51
	Min	2.28364	2.51	2.2608	2.51	2.51
C_q(aF)	*Nominal*	3613.46	3613.46	3613.46	3613.46	3613.46
	Max	3974.453	3998.033	3613.46	3613.46	3613.46
	Min	3252.655	3236.263	3613.46	3613.46	3613.46
C_e(aF)	*Nominal*	9.735	9.735	9.735	9.735	9.735
	Max	10.7085	9.735	10.81666667	10.62	9.735
	Min	8.7615	9.735	8.85	8.85	9.735

As a result, it is evident that awareness not only in the nominal value of interconnect performances and parameters, but also their variation range is required for a more accurate comparison among the possible MLGNR aspect ratio alternatives and for an effective and reliable design of the interconnect. Depending on the Monte Carlo approach [33], [34] a numerous number of simulations can be done for the variation of interconnect parasitics due to process variations. These Monte Carlo simulations will trials will give range of variation of delays corresponding variation of parameters in MLGNR interconnects due to process variation effects.

5.3 Impact of process induced length variations on delay

Deviations in width of MLGNR interconnects taken to consideration while remaining all parameters kept constant makes change in all parasitic values as shown in table 5.2. The width is directly proportional to number of conducting modes and C_e in MLGNR, which will affect the propagation delay. A+ is much higher as compared to A- because percentage increases in resistance and inductance values more as compared to percentage of decrease this effect much prominent in higher interconnect lengths.

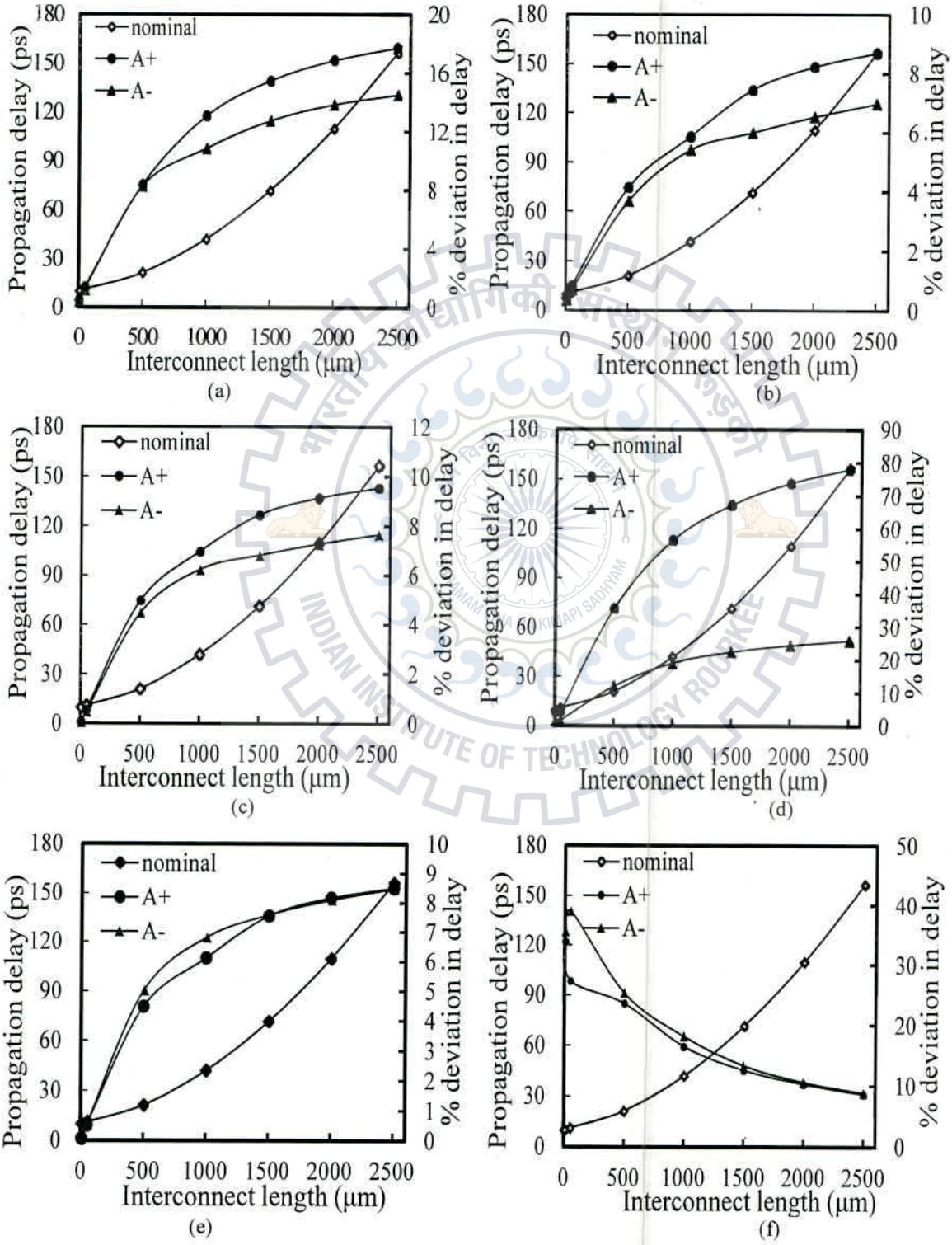
Intercalative doping density of MLGNR varied, while remaining all parameters are constant makes change in all parasitic values except L_e and C_e due to varying in number of conducting channels as shown in table 5.2. In this case also A+ is much higher as compared to A- because percentage increases in resistance and inductance values more as compared to percentage of decrease this effect much prominent in higher interconnect lengths.

For deviation in dielectric thickness of MLGNR while remaining all parameters are constant makes a change L_e and C_e and left over parasitics remains constant as shown table 5.2.

By varying mean free path of carriers in MLGNR while remaining all parameters are constant makes change in only scattering resistance (R_s) as shown in table 5.2. In this case also A+ is much higher as compared to A- because percentage increases in scattering resistance and inductance values more as compared to percentage of decrease this effect much prominent in higher interconnect lengths.

For deviation in dielectric constant of MLGNR while remaining all parameters are constant makes change in only electrostatic capacitance (C_e) as shown in table 5.2. In this case A+ and A- are comparable these are increases with length.

Contact resistance of MLGNR depends on fabrication process and it is varied 50%, while remaining all parameters are constant. In this case A+ and A- values are higher at lower interconnect lengths because, contact resistance is comparable to scattering resistance. After that A+ and A- values are decreasing with interconnect lengths due to scattering resistance increases with lengths.



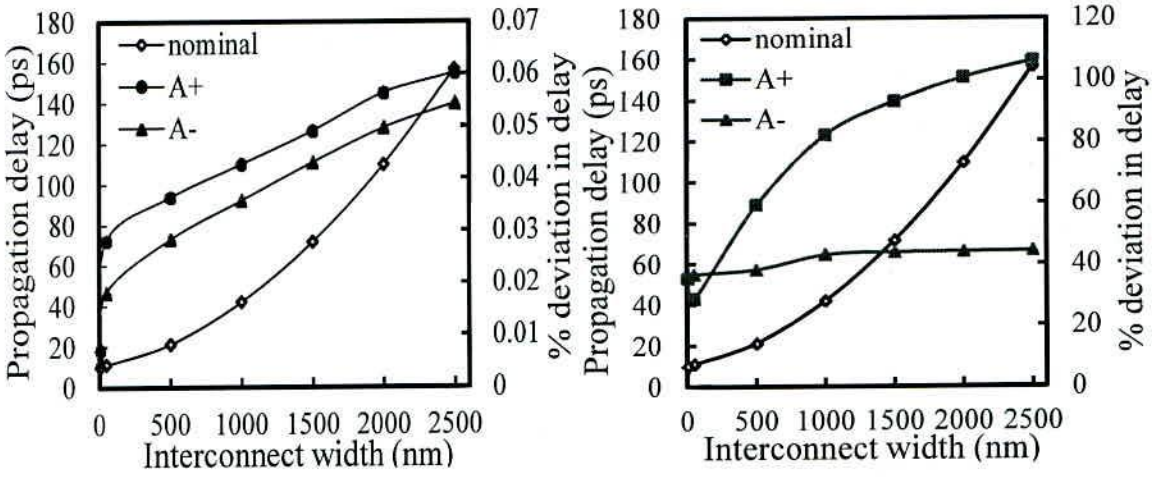


Fig. 5.1: Performance deviations for variation of one parameter while remaining all unchanged parameter varied for different interconnect lengths (a) width (b) doping (c) dielectric thickness, (d) mean free path, (e) dielectric constant, (f) contact resistance (g) interlayer distance and (h) represents varying of all parameters at a time.

Fig. 5.1 (h) shows percentage deviation of interconnects performance from nominal value to worst-case and best-case delays. This deviation more at global interconnect lengths, because of variation in mean free path makes scattering resistance twice.

5.4 Impact of process induced width variations on delay

By varying widths of MLGNR while remaining all parameters are constant makes a change in all parasitic values as shown in table 5.2. The width is directly proportional to number of conducting modes and C_e in MLGNR, which will affect the propagation delay. A+ is much higher as compared to A- because percentage increases in resistance and inductance values more as compared to percentage of decrease this effect much prominent in higher interconnect widths.

By varying intercalative doping density of MLGNR while remaining all parameters are constant makes change in all parasitic values except L_e and C_e by varying in number of conducting modes as shown in table 5.2. In this case also A+ is much higher as compared to A- because percentage increases in resistance and inductance values more as compared to percentage of decrease this effect much prominent in higher interconnect widths.

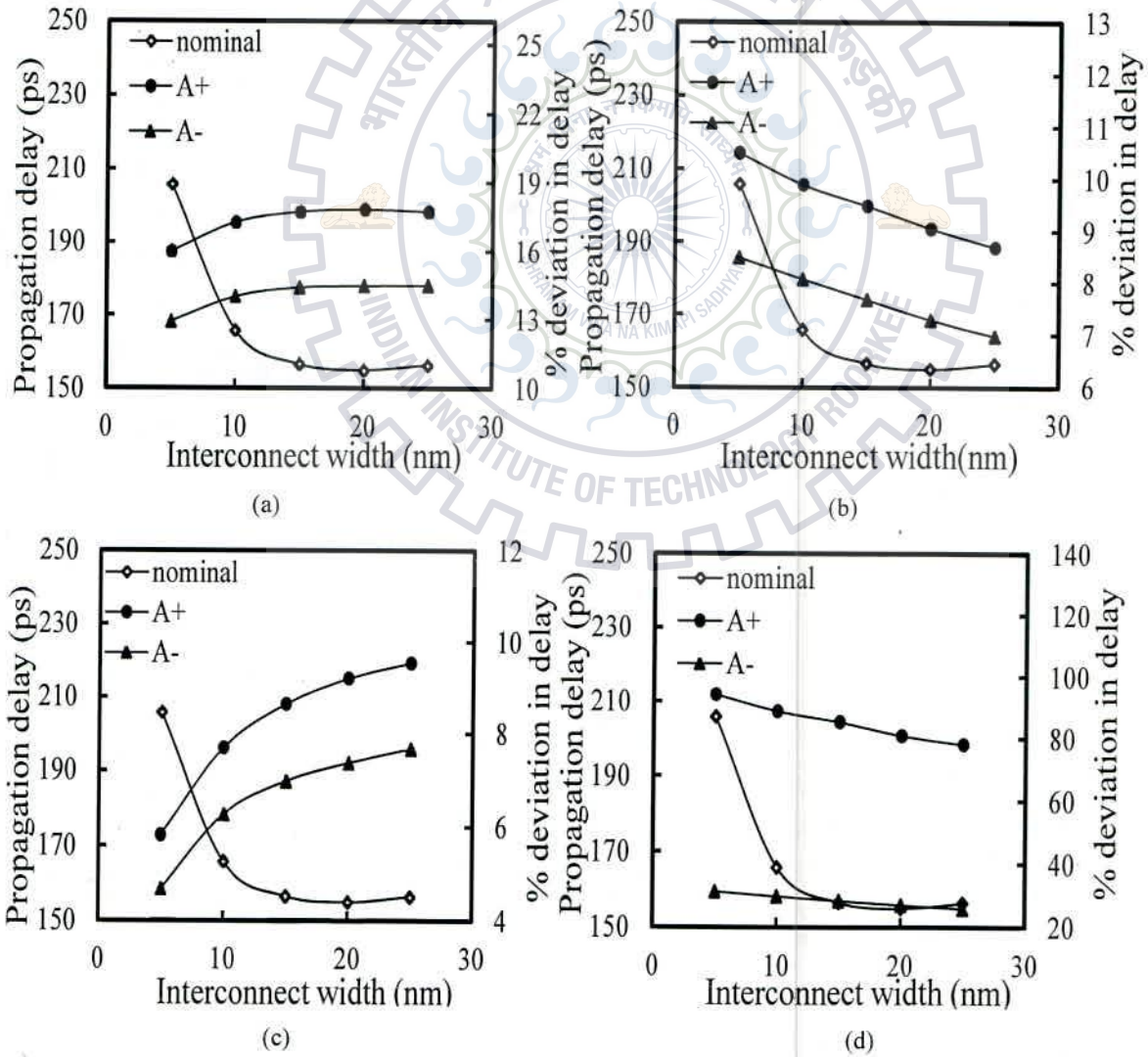
By varying dielectric thickness of MLGNR while remaining all parameters are constant makes change L_e and C_e and remaining all parasitics are constant in table 5.2. A+ and A- are increases with interconnect widths due to large value of C_e.

By varying mean free path variation of MLGNR while remaining all parameters are constant makes change in only scattering resistance (R_s) as shown in table 5.2. In this case

also A+ is much higher as compared to A- because percentage increases in scattering resistance and inductance values more as compared to percentage of decrease this effect much prominent in lower interconnect widths due to higher value of parasitic values.

By varying dielectric constant of MLGNR while remaining all parameters are constant makes change in only electrostatic capacitance (C_e) as shown in table 5.2. The effect of variation of dielectric constant on performance shown in Fig. 5.1, where A+ is deviation worst-case delay from nominal delay and A- is deviation of best-case delay from nominal delay.

By variation in contact resistance of MLGNR while remaining all parameters are constant. In this case A+ and A- values are higher at large interconnect widths because scattering resistance is lower at wider widths so contact resistance effect will be considerable factor at this dimension.



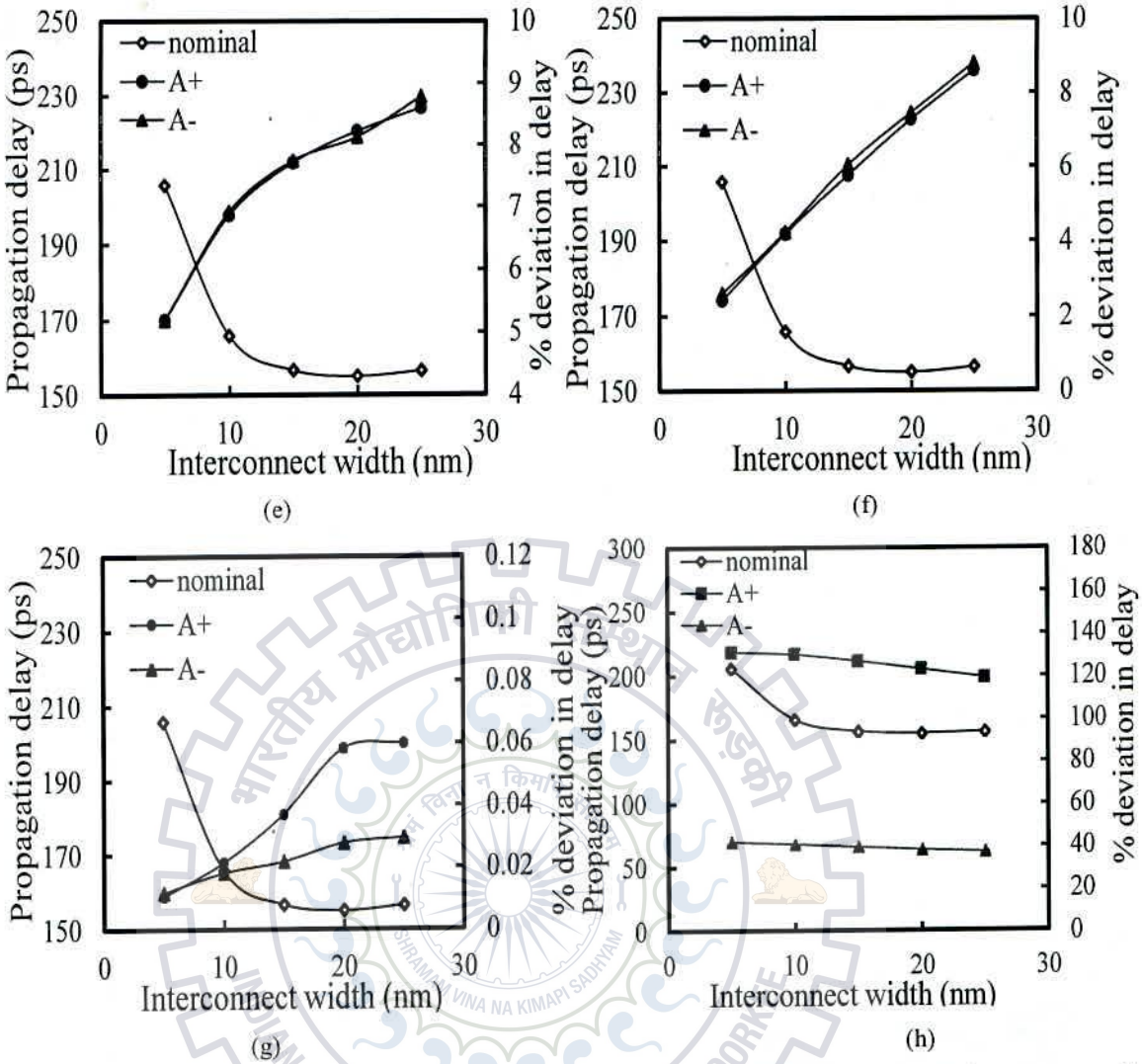


Fig. 5.2: Performance deviations for variation of one parameter while remaining all unchanged parameter varied for different interconnect widths (a) width (b) doping (c) dielectric thickness, (d) mean free path, (e) dielectric constant, (f) contact resistance (g) interlayer distance and (h) represents varying of all parameters at a time

Chapter 6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

In nano-scale and deep-submicron regime, graphene nanoribbons (GNRs) are conceived as an emerging interconnect material because of their high reluctance to electromigration and other novel properties. Initially, the interconnect parasitics of an MLGNR is modeled using the MTL formulation which is further simplified to an ESC model. For an input rising pulse of 1V, the output voltage waveforms for both the MTL and the ESC models are in good agreement with each other. MTL model used to analyze the time domain applications such as propagation delay, average power dissipation, crosstalk, etc and ESC model used for frequency domain applications such as gain, Nyquist plot and bandwidth.

A DIL system is used to analyze the propagation delay of SLGNR and MLGNR interconnects. It has observed that an MLGNR with higher number of layers exhibits a significant improvement in delay as compared to SLGNR and MLGNR employing lower number of layers. Moreover, an undoped MLGNR shows optimum delay and power performance for 10 to 15 layers at global interconnect lengths. Apart from this, a capacitively coupled interconnect line is used to analyze the crosstalk delay for different number of MLGNR layers. The higher number of layers exhibits a significant improvement in crosstalk delay as compared to the lower one.

The DIL system further employed to analyze the transfer function of an equivalent *RLC* model. Depending on the transfer function, bandwidths and relative stability of MLGNR compared with MWCNT and Cu interconnects. MLGNR exhibits much higher bandwidths for local, intermediate and global interconnect dimensions as compared to MWCNT/Cu interconnects. The relative stability of MLGNR is lower as compared to MWCNT/Cu at local interconnect lengths and at global interconnects all DIL systems are highly stable. This dissertation work has introduced an analytical expession of 90% propagation delay that shows a good accuracy with H-spice simulated results.

The uncertainties and variations in geometrical processes may produce a remarkable alteration in interconnect dimensions. Monte Carlo approach has been adopted in order to study the impact of process variations on MLGNR interconnects. This approach requires

large numbers of simulation trials and is used to analyze the worst case delay and best delay variations with respect to nominal delay.

6.2 FUTURE SCOPE

Here in this work we consider the *RLC* parasitic parameters MLGNR based on previous modeling to verify this fabricate virtual MLGNR on software and do electromagnetic simulations to get parasitics.

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1. Manoj Kumar Majumder, **Narasimha Reddy K.**, B. K. Kaushik and S. K. Manhas, "Analysis of MWCNT and MLGNR Interconnects: Impact on Delay and Area," *IEEE Electron Device Lett.*,(**Major review**).

2. **Narasimha Reddy K.,** M. K. Majumder, B. K. Kaushik and B. Anand, "Delay, Power and Frequency Domain Analysis of MLGNR in Comparison to Cu Interconnects," *IEEE trans. VLSI syst.* (**communicated**).

3. **Narasimha Reddy K.**, M. K. Majumder, B. K. Kaushik and B. Anand, "Bandwidth and stability analysis of MLGNR and MWCNT interconnects," *IET Electronic Lett.*, (**communicated**).

4. **Narasimha Reddy K**, Manoj Kumar Majumder, B. K. Kaushik, S. K. Manhas and B. Anand "Dynamic Crosstalk Effect in Multi-Layer Graphene Nanoribbon Interconnects," in *Proc. IEEE International Conference on Communications, Devices and Intelligent systems (CODIS 2012),* Kolkata, India, Dec 28-29, 2012, DOI: 10.1109/CODIS.2012.6422241.

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6. Manoj Kumar Majumder, **Narasimha Reddy K**, B. K. Kaushik, and S. K. Manhas, "Comparison of Propagation Delay in Single- and Multi-layer Graphene Nanoribbon Interconnects," in Proc. *IEEE 5th International Conference on Computers and Devices for communication 2012 (CODEC 2012)*, Kolkata, India, Dec. 17-19, 2012, DOI: 10.1109/CODEC.2012.6509357.

Comparison of Propagation Delay in Single- and Multi-layer Graphene Nanoribbon Interconnects

Manoj Kumar Majumder
Microelectronics and VLSI Group, Department of Electronics and Computer Engineering
Indian Institute of Technology Roorkee
Roorkee, INDIA
manojbesu@gmail.com

Narasimha Reddy. K
Microelectronics and VLSI Group, Department of Electronics and Computer Engineering
Indian Institute of Technology Roorkee
Roorkee, INDIA
nr120@iitr.ernet.in

B. K. Kaushik
Microelectronics and VLSI Group, Department of Electronics and Computer Engineering
Indian Institute of Technology Roorkee
Roorkee, INDIA
bkk23fec@iitr.ernet.in

S. K. Manhas
Microelectronics and VLSI Group, Department of Electronics and Computer Engineering
Indian Institute of Technology Roorkee
Roorkee, INDIA
samanfec@iitr.ernet.in

Abstract—**Multi-layer graphene nanoribbons (MLGNRs) have potentially provided attractive solution over single-layer GNR (SLGNR) interconnects. This research paper presents an equivalent *RLC* model for GNR interconnects to study the effect of propagation delay. A driver-interconnect-load (DIL) system employing CMOS driver is used to analyze the performance. It has been observed that the overall delay performance is improved by 94.5% for MLGNR as compared to SLGNR.**

Keywords-Graphene nanoribbon (GNR); single-layer GNR (SLGNR); multi-layer GNR (MLGNR); propagation delay; interconnect lengths, VLSI.

I. INTRODUCTION

Recent development in science and technology indicates that graphene nanoribbons (GNRs) have aroused a lot of research interests for their potential applications in the area of field effect devices and interconnects [1-4]. Ballistic transport [5-7] in graphene makes it suitable for not only interconnects but also for switching transistors. A monolithic system can be constructed using graphene for both transistors and interconnects. Compared to silicon and even *n* or *p*-type semiconductors, graphene has superior mobility. Theoretically, it has been predicted that GNRs will outperform the Cu interconnects for smaller widths less than 8nm [8]. For nanoscale device dimensions, Cu interconnects is mostly affected by grain boundaries and sidewalls scatterings [9]. Therefore, researchers are forced to find an alternative solution for global VLSI interconnects.

Graphene is a sheet of graphite tightly packed into a two dimensional (2D) honeycomb lattice structure, and can be defined as a basic building block of graphite, carbon nanotubes (CNTs), graphene nanoribbons (GNRs) etc. Since GNRs can be considered as unrolled version of single walled carbon nanotubes (SWCNTs), most of the electronic properties of GNRs are similar to SWCNTs. In a high quality graphene sheet, the mean free path (MFP) is ranging from 1-5μm [10]. GNRs can carry large current densities more than 10^8 A/cm^2 [11] than that of regular interconnects such as Cu [10]. It offers higher carrier mobilities that can reach upto 1,00,000 cm^{2}v^{-1}s^{-1} [11]. For outstanding electrical and thermal properties of GNRs, it is necessary to understand the electronic band structures of GNRs. The band structures of armchair and zigzag edged GNRs (ac-GNRs and zz-GNRs) are calculated using a tight binding model [12]. According to the tight binding model [12], graphene is a zero bandgap semiconductor or semi metal. Depending on chirality, GNRs can be classified as armchair and zigzag GNRs (ac- and zz-GNRs) as shown in Figs. 1(a) and 1(b) respectively. The ac-GNRs can be further differentiated as metallic and semiconductor based on the number of hexagonal rings (*N*) present across the width of GNR that is fixed along with the length. In ac-GNRs, metallic properties depends on the condition of $N=3p-1$ or $3p+2$ whereas $N=3p$ or $3p+1$ satisfies the semiconducting properties in which *p* can be defined as any integer. Apart from this, zz-GNRs are always metallic independent of *N*. Depending on the number of layers formed by the hexagonal rings of carbon atoms, GNRs can be categorized as single-layer GNR (SLGNR) and multi-layer GNR (MLGNR).

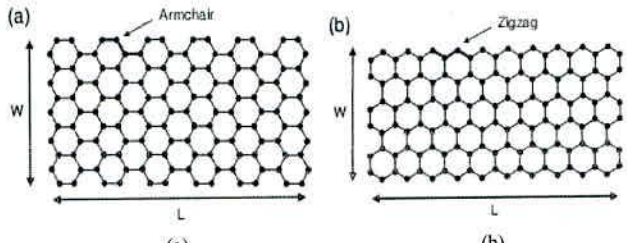

Fig.ure 1. GNR structures for (a) armchair and (b) zigzag chirality [12]

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This research paper primarily focuses on the comparison of propagation delay for different lengths, widths and thickness by considering the effects of long range scattering, acoustic phonon scattering and line edge scattering [13, 14]. A comparative analysis is performed between SLGNR and MLGNE to address the effect of propagation delay. The organization of this paper is as follows: section I introduces the recent research scenario and briefs about the works carried out. Section II presents the equivalent *RLC* models of SLGNR and MLGNR whereas the details of simulation setup are provided in section III. Comparative analysis of propagation delay between different GNR structures is presented in section IV. Finally, section V draws a brief summary of this paper.

II. GNR INTERCONNECT MODEL

Equivalent *RLC* models of SLGNR and MLGNR primarily depends on their basic geometries. Fig. 2 and Fig. 3 presents the geometries and equivalent *RLC* models for SLGNR and MLGNR respectively. Geometrically, the GNR layers are placed on ground at a distance of d. The permittivity of the medium above the ground is assumed as ε_r as shown in Fig. 2.

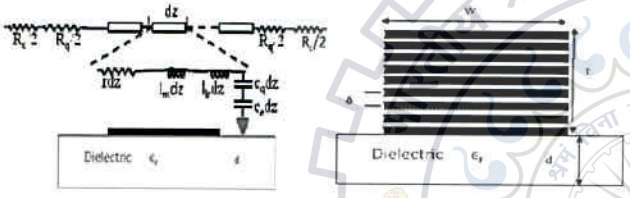

Figure 2. Geometries of (a) SLGNR and its equivalent *RLC* model, (b) MLGNR interconnect.

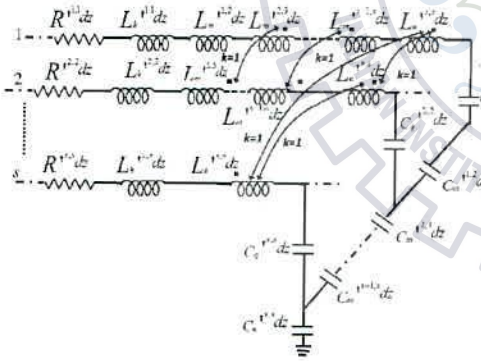

Figure 3. Equivalent *RLC* model of MLGNR interconnect

Equivalent contact resistance (R_c) of GNR interconnects depends on their fabrication process. As per current fabrication technology, GNR exhibits an imperfect contact resistance of 3.2kΩ at both ends of the interconnect line. Apart from this, the fundamental quantum resistance is associated with each GNR layer that is due to the confinement of carriers in a quantum wire. In general, the quantum resistance can be expressed as [8]

$$R_q = \frac{h/2e^2}{N_{ch}N_{layer}} = 12.9k\Omega / N_{ch} \quad (1)$$

where h is Plank's constant, e is electronic charge and N_{ch} represents the number of conducting channels in a GNR sheet. For SLGNR case, the denominator can be reduced to N_{ch} because N_{layer} =1. N_{ch} depends on the number of sub-bands, width of GNR, Fermi energy, temperature and geometry (*i.e.*, ac-GNR or zz-GNR). It can be formulated as [13]

$$N_{ch} = N_{ch,\,electrons} + N_{ch,\,holes}$$

$$= \Sigma_n\left[1+\exp\left(E_{n,\,electron} - E_F \Big/ K_B T\right)\right]^{-1} + \Sigma_n\left[1+\exp\left(E_F - E_{n,\,hole} \Big/ K_B T\right)\right]^{-1} \quad (2)$$

where E_F is Fermi energy, $E_{n,electron}$, $E_{h,hole}$ is the energies of electron and holes, T is the temperature and K_B is Bolzman constant. Equation (2) can be solved by using iterative method and curve fitting methods [13]. Quantum capacitance (c_q) arises due to the quantum energies stored in carriers which is a effect of quantum confinement and can be expreesed as [14]

$$C_{q,\,channel} = \frac{4e^2}{hv_F} \approx 193\,aF/\mu m \quad (3)$$

where v_F is the Fermi velocity of GNR ≈ 8×10^5m/s. On the other hand, kinetic inductance (l_k) is due to inertial mass of mobile charge carriers that will oppose the change in electric fields as an equivalent series inductance. It can be expressed as [14]

$$l_{k/channel} = \frac{h}{4e^2 v_F} \approx 8\,nH/\mu m \quad (4)$$

Thus for MLGNR, the total C_q and l_k can be expressed by considering the total number of conducting channels N_{ch} [14]

$$C_q = \frac{4e^2 N_{ch}}{hv_F} \approx 200.N_{ch}\,aF/\mu m \quad (5)$$

$$l_k = \frac{4e^2 N_{ch}}{hv_F} = \frac{8}{N_{ch}}\,nH/\mu m \quad (6)$$

The equivalent *RLC* model of Fig. 3 comprises of *p.u.l.* magnetic inductance (l_e) and electrostatic capacitance (c_e) that can be represented in terms of the stored energy in magnetic and electric fields respectively. Therefore, the *p.u.l.* l_e and c_e can be expressed as [11]

$$l_e = \frac{\mu_0 d}{w}\,nH/\mu m \quad (7)$$

$$c_e = \frac{\varepsilon_0 w}{d}\,aF/\mu m \quad (8)$$

For the case of MLGNR, mutual inductance (l_m) and mutual capacitance (C_m) exists between two layers due to the electron tunnel transport phenomenon. It can be given as [15]

$$l_m^{(j-1,j)} = \frac{\mu_0 \delta}{w}\,nH/\mu m \quad (9)$$

$$C_m^{(j-1,j)} = \frac{\varepsilon_0 w}{\delta}\,aF/\mu m \quad (10)$$

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where w is defined as the width of MLGNR interconnects, δ is the interlayer distance of MLGNRs, μ_0 and ε_0 represents magnetic permeability and electrostatic permittivity of free space respectively.

The equivalent *RLC* model of Fig. 3 considers the conductance modeling of GNR with scattering effect that was first introduced in [8] using Landauer formula. The approach of conductance modeling is used to find scattering resistance (distributed resistance) of GNRs. Scattering resistance (R_s) of GNR interconnects is modelled by using various types and sources of scattering that has an impact on charge carrier transport [16]. The main sources of scattering in GNR is due to static impurity scattering, defects, line edge roughness scattering (LER) and acoustic phonon scattering [17-19]. The impurities present in graphene can result in long range scattering of carriers. λ_L is the mean free path of carriers in presence of impurities. For SLGNR, this typical value of λ_L is in the range of 1-5μm [8]. In this paper, the quantitaive value of λ_L is considered as 4μm and 0.42μm for SLGNR and MLGNR respectively. Therefore, by considering the effect of different scattering mechanisms, the *p.u.l.* resistance of j^{th} layer in MLGNR (as in Fig. 3) can be expressed as [15]

$$r^{(j,j)} = \frac{h/2e^2}{N_{ch}\lambda_L} \tag{11}$$

III. Simulation Setup

This research paper presents a comparative analysis of propagation delay for SLGNR and MLGNR at different interconnect lengths ranging from 100μm to 500μm using the geometries suggested in [15]. A driver-interconnect-load (DIL) system employing a CMOS driver is used to accurate estimation of delay as shown in Fig. 4. The interconnect line in DIL system is represented by the equivalent *RLC* models of SLGNR and MLGNR. The interconnect line is terminated with a load capacitance C_L = 10aF [20].

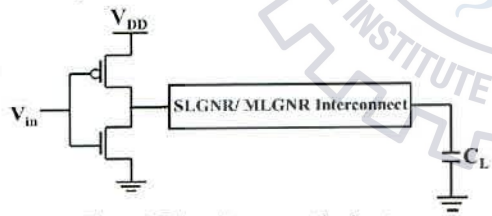

Figure 4. Driver interconnect load system

IV. Results And Discussions

Using the above mentioned simulation setup, propagation delay is compared for SLGNR and MLGNR. HSPICE circuit simulations have been performed for SLGNR and MLGNR that considers different number of layers such as 4, 10 and 20. Fig. 5 through Fig. 9 presents a comparative analysis between different GNR layers at global interconnect lengths. It is observed that the delay increases for longer interconnect lengths whereas reduces with increasing widths and number of layers in GNRs. This fact can be realized by using the concept of conducting channels that depends on the number of layers and widths of GNRs. From energy band diagram of graphene [18], it can be understood that the number of conducting channels varies with GNR width due to the flow of electron concentration. The increasing width of GNR also increases the number of conducting channels resulting in lesser propagation delay. Apart from this, increasing number of layers resulting in reduction of resistive parasitic as shown in equation (1). Therefore, MLGNR with N_{layer} = 20 resulting in lesser effect of delay as compared to SLGNR and MLGNR with N_{layer} = 4, 10.

Table I summarizes the percentage improvement in delay for MLGNR (N_{layer} = 20) with respect to SLGNR and MLGNR (N_{layer}=4, 10). It is observed that the delay is significantly improved for MLGNR N_{layer}=20 with increasing interconnect lengths. Therefore, MLGNR with more number of layers is useful for global interconnect lengths.

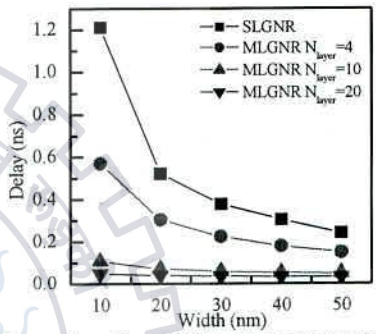

Figure 5. Propagation delay of GNR with varying widths at 100μm interconnects length.

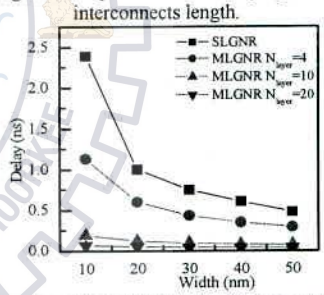

Figure 6. Propagation delay of GNR with varying widths at 200μm interconnects length.

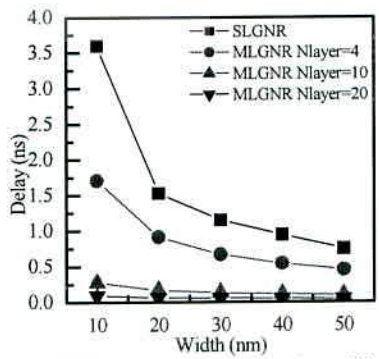

Figure 7. Propagation delay of GNR with varying widths at 300μm interconnects length.

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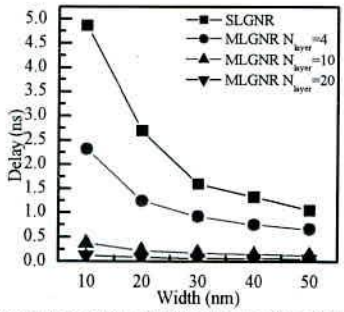

Figure 8. Propagation delay of GNR with varying widths at 400μm interconnects length.

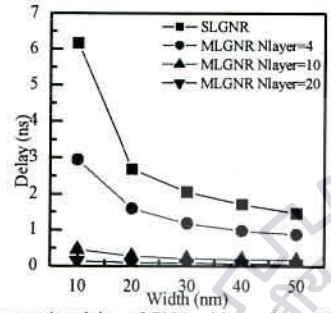

Figure 9. Propagation delay of GNR with varying widths at 100μm interconnects length.

TABLE I. PERCENTAGE IMPROVEMENT IN PROPAGATION DELAY AT GLOBAL INTERCONNECT LENGTHS

Interconnect lengths (μm)	Widths of GNRs (nm)	% improvement in delay for MLGNR (N_{layer}=20) as compared to		
		MLGNR N_{layer}=10	MLGNR N_{layer}=4	SLGNR N_{layer}=1
100	10	55.12	91.53	96.00
	50	30.32	77.61	86.15
200	10	63.10	93.85	97.19
	50	43.64	86.00	91.50
300	10	66.32	94.56	97.42
	50	50.91	89.27	93.50
400	10	68.12	94.90	97.65
	50	55.63	91.31	94.54
500	10	69.11	95.23	97.77
	50	58.86	92.41	95.40

V. CONCLUSION

This research paper presents equivalent *RLC* models of GNR interconnects by considering the effect of scattering and width of GNR. Propagation delay is compared for different number of GNR layers using DIL system employing CMOS driver. As compared to SLGNR, the delay performance is significantly improved for MLGNR with increasing number of layers for longer interconnect lengths. Therefore, MLGNR can be proved as an emerging material for future high-speed global VLSI interconnects.

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Dynamic Crosstalk Effect in Multi-layer Graphene Nanoribbon Interconnects

Narasimha Reddy K., Manoj Kumar Majumder, B. K. Kaushik, S. K. Manhas and B. Anand
Microelectronics and VLSI Group, Department of Electronics and Computer Engineering
Indian Institute of Technology Roorkee
Roorkee, INDIA
narasimhareddy.422@gmail.com, manojbesu@gmail.com, {bkk23fec, samanfec, anandfec}@iitr.ernet.in

Abstract—**Multi-layer graphene nanoribbon (MLGNR) is a potential candidate for deep-nanometer-interconnect applications due to its superior conductivity and current carrying capabilities. This research paper presents an equivalent *RLC* model for MLGNR interconnects to study the dynamic crosstalk effect. A two-coupled line bus architecture employing CMOS driver is used to analyze the in-phase and out-phase crosstalk delays. On an average, the in-phase and out-phase crosstalk delays are improved by 4.75% and 18.04% respectively for MLGNR with higher number of layers as compared to the lesser ones.**

Keywords-Graphene nanoribbon (GNR); multi-layer GNR (MLGNR); in-phase and out-phase delay; interconnects; VLSI.

I. INTRODUCTION

In recent nanoscale device dimensions, Cu interconnects are mostly affected by grain boundaries and sidewall scatterings [1]. Therefore, researchers are forced to find an alternative solution for global VLSI interconnects. Graphene is considered as an emerging interconnect material [2-5] due to its unique physical properties that includes higher current density, thermal conductivity [6], long mean free path (MFP) [7] etc. Due to long *mfp*, graphene exhibits the unique ballistic transport [7-9] that makes it suitable for not only interconnects but also for switching transistors. The resistivity of graphene arises due to scattering of electrons wherein the current carriers participate in the transport.

Graphene is a sheet of graphite tightly packed into two dimensional (2D) honeycomb lattice structure, and can be defined as a basic building block of graphite, carbon nanotubes (CNTs), graphene nanoribbons (GNRs) etc. Since GNRs can be considered as unrolled version of single walled carbon nanotubes (SWCNTs), most of the electronic properties of GNRs are similar to SWCNTs. In a high quality graphene sheet, the mean free path (MFP) is ranging from 1-5μm [10]. GNRs can carry large current densities of more than 10^8 A/cm^2 [11] that of regular interconnects such as Cu [10]. It offers higher carrier mobilities that can reach upto 1,00,000 cm^{2}v^{-1}s^{-1} [11]. For outstanding electrical and thermal properties of GNRs, it is necessary to understand the electronic band structures of GNRs. The band structures of armchair and zigzag edged GNRs (ac-GNRs and zz-GNRs) are calculated using tight binding model [12]. According to the tight binding model [12], graphene is a zero bandgap semiconductor or semi metal. Depending on chirality, GNRs can be classified as armchair and zigzag GNRs (ac- and zz-GNRs). The ac-GNRs can be further differentiated as metallic and semiconductor based on the number of hexagonal rings (N) present across the width of GNR that is fixed along the length. The zz-GNRs are always metallic independent of N. Depending on the number of layers formed by the hexagonal rings of carbon atoms, GNRs can be categorized as single-layer GNR (SLGNR) and multi-layer GNR (MLGNR).

For conventional interconnects, crosstalk coupling may cause signal delays, speed-ups and glitches (usually referred to as crosstalk noise). It can induce a delay on coupled lines with negative impact on performance. The delay depends on several factors, such as coupling capacitance, relative strength of drivers (which may cause different skew rates in the signals), and the relative transition time skew [13]. Apart from this, crosstalk may cause an undesired voltage glitch on a bus line due to transition in one or more adjacent bus line. Therefore, reliability is a main concern of crosstalk effect. Crosstalk noise in coupled lines can be broadly divided into two categories: (1) functional crosstalk noise, and (2) dynamic crosstalk noise [14]. Under functional crosstalk category, a victim line experiences a voltage spike when an aggressor line switches [15]. On the other hand, dynamic crosstalk is observed when aggressor and victim line switches simultaneously. A change in signal propagation delay is experienced under dynamic crosstalk when adjacent line (aggressor and victim) switches either in-phase or out-of-phase.

This research paper primarily focuses on the comparison of dynamic crosstalk delay for different lengths, widths and thickness of MLGNR by considering the effects of long range scattering, acoustic phonon scattering and line edge scattering [16, 17]. A comparative analysis is performed for MLGNR with different number of layers to address the effect of dynamic crosstalk delay. The organization of this paper is as follows: section I introduces the recent research scenario and briefs about the works carried out. Section II presents the geometry and equivalent *RLC* models of MLGNR whereas the details of simulation setup are provided in section III. Comparative analysis of in-phase and out-phase crosstalk delays between different GNR structures is presented in section IV. Finally, section V concludes the paper.

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II. GEOMETRY AND EQUIVALENT *RLC* MODEL

Equivalent *RLC* model of MLGNR primarily depends on its basic geometry. Fig. 1 and Fig. 2 present the geometry and equivalent *RLC* model of MLGNR interconnects. Geometrically, GNR with multiple layers is placed on ground plane at a distance of *d*. The permittivity of the medium above the ground plane is assumed as ε_r as shown in Fig. 1. The width and thickness of the MLGNR are considered as *w* and *t* respectively. The interlayer distance $\delta = 0.34$nm presents the vander waals gap between two carbon atoms [9].

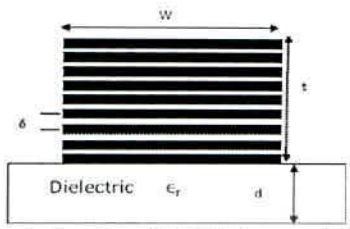

Figure 1. Geometries of MLGNR above ground plane

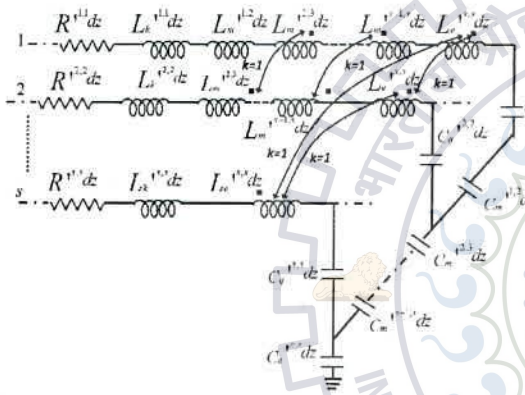

Figure 2. Equivalent *RLC* model of MLGNR interconnect

Equivalent contact resistance (R_c) of GNR interconnects depends on their fabrication process. As per current fabrication technology, GNR exhibits an imperfect contact resistance of 3.2kΩ at both ends of the interconnect line. Apart from this, the fundamental quantum resistance is associated with each GNR layer that is due to the confinement of carriers in a quantum wire. In general, the quantum resistance can be expressed as [9]

$$R_q = \frac{h/2e^2}{N_{ch}N_{layer}} = 12.9k\Omega / N_{ch} \quad (1)$$

where *h* is known as Planck's constant, *e* is electron charge and N_{ch} represents the number of conducting channels in a GNR sheet. N_{ch} depends on the number of sub-bands, width of GNR, Fermi energy, temperature and geometry (*i.e.*, ac-GNR or zz-GNR). It can be formulated as [16]

$$N_{ch} = N_{ch,\,electrons} + N_{ch,\,holes}$$

$$= \Sigma_n \left[1 + \exp\left(E_{n,\,electron} - E_F / K_B T\right)\right]^{-1} + \Sigma_n \left[1 + \exp\left(E_F - E_{n,\,hole} / K_B T\right)\right]^{-1} \quad (2)$$

where E_F is the Fermi energy, $E_{n,electron}$, $E_{h,hole}$ are the energies of electron and holes, *T* is the temperature and K_B is Bolzman constant. Equation (2) can be solved by using iterative method and curve fitting methods [16]. Quantum capacitance (C_q) arises due to the quantum energies stored in carriers which is a effect of quantum confinement and can be expreesed as [17]

$$C_{q,\,channel} = \frac{4e^2}{hv_F} \approx 193\,aF/\mu m \quad (3)$$

where v_F is the Fermi velocity of GNR $\approx 8\times10^5$m/s [9]. On the other hand, kinetic inductance (l_k) is due to inertial mass of mobile charge carriers that will oppose the change in electric fields as an equivalent series inductance. It can be expressed as [17]

$$l_{k/channel} = \frac{h}{4e^2 v_F} \approx 8\ nH/\mu m \quad (4)$$

Thus for MLGNR, the total C_q and l_k can be expressed by considering the total number of conducting channels N_{ch} [17]

$$C_q = \frac{4e^2 N_{ch}}{hv_F} \approx 200 N_{ch}\ aF/\mu m \quad (5)$$

$$l_k = \frac{4e^2 N_{ch}}{hv_F} = \frac{8}{N_{ch}} nH/\mu m \quad (6)$$

The equivalent *RLC* model of Fig. 2 comprises of *p.u.l.* magnetic inductance (l_e) and electrostatic capacitance (c_e) that can be represented in terms of the stored energy in magnetic and electric fields respectively. Therefore, the *p.u.l.* l_e and c_e can be expressed as [12]

$$l_e = \frac{\mu_0 d}{w} nH/\mu m \quad (7)$$

$$c_e = \frac{\varepsilon_0 w}{d} aF/\mu m \quad (8)$$

For the case of MLGNR, mutual inductance (l_m) and mutual capacitance (C_m) exists between two layers due to the electron tunnel transport phenomenon. It can be given as [18]

$$l_m^{(j-1,j)} = \frac{\mu_0 \delta}{w} nH/\mu m \quad (9)$$

$$C_m^{(j-1,j)} = \frac{\varepsilon_0 w}{\delta} aF/\mu m \quad (10)$$

where *w* is defined as the width of MLGNR interconnects, δ is the interlayer distance of MLGNRs, μ_0 and ε_0 represents magnetic permeability and electrostatic permittivity of free space respectively.

The equivalent *RLC* model of Fig. 2 considers the conductance modeling of GNR with scattering effect that was first introduced in [9] using Landauer formula. The approach of conductance modeling is used to find scattering resistance (distributed resistance) of GNRs. Scattering resistance (R_s) of GNR interconnects is modelled by using various types and

sources of scattering that has an impact on charge carrier transport [19]. The main sources of scattering in GNR is due to static impurity scattering, defects, line edge roughness scattering (LER) and acoustic phonon scattering [20-23]. The impurities present in graphene resulting in long range scattering of carriers. λ_L is the mean free path of carriers in presence of impurities. This resaerch paper considers the quantitaive value of λ_L as 4μm for MLGNR [9]. Therefore, by considering the effect of different scattering mechanisms, the *p.u.l.* resistance of j^{th} layer in MLGNR (as in Fig. 2) can be expressed as [18]

$$r^{(j,j)} = \frac{h/2e^2}{N_{ch}\lambda_L} \tag{11}$$

III. Simulation Setup

Using a two-coupled line bus architecture, crosstalk delay is estimated for MLGNR with different number of layers as shown in Fig. 3. Out of these two lines, one is referred as aggressors and the other one is as victim. The coupling capacitance (C_{CM}) demonstrates the crosstalk effect that primarily depends on the spacing (S_{a-v}) between aggressor and victim lines and can be expressed as [24]

$$C_{CM} = \frac{0.5}{1+\left(S_{a-v}/(t+d)\right)^2} C_{[BCP]}\left(\frac{d}{S_{a-v}/2}, \frac{2t}{S_{a-v}/2}\right) + \frac{0.87}{1+\left(S_{a-v}/2(t+d)\right)} C_{[CP]}\left(\frac{w}{S_{a-v}}\right) \tag{12}$$

where C_{BCP} represents the capacitance to ground of the bottom side of the layer and C_{CP} is the coupling capacitance between two co-planar plates [24]. The interconnect line in bus architecture can be replaced by MLGNR with different number of layers. A CMOS driver is used for accurate estimation of crosstalk delay. The bus architecture has the following values of load capacitance (C_L) and power supply voltages (V_{dd}): C_L = 10aF and V_{dd} = 1V [25]. Crosstalk delay is analyzed for the following two cases: (1) in-phase and (2) out-phase. To analyze the effect of dynamic crosstalk, different global interconnect lengths ranging from 100μm to 500μm with an increasing step size of 100μm are used for simulation purpose.

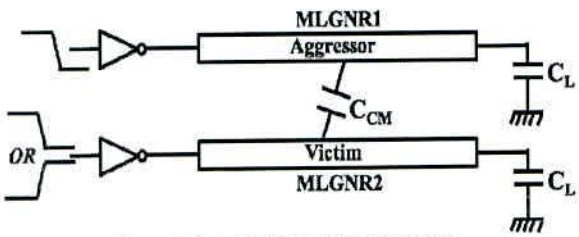

Figure 3. Two-coupled line bus architecture

IV. Results And Discussions

Using the above mentioned setup, dynamic crosstalk delays (in-phase and out-phase) are observed for MLGNR interconnects. HSPICE circuit simulations have been performed for MLGNR with different number of layers such as 4, 10 and 20. Fig. 4 through Fig. 6 presents the variation of crosstalk delays with interconnects lengths for different number of GNR layers. It is observed that the crosstalk delays increases with interconnect lengths whereas the increment of out-phase delay is more as compared to the in-phase delay. This fact can be realized by the effect of Miller Coupling Factor (MCF) [15]. This factor mainly influences the coupling capacitance (C_{CM}) between aggressor and victim lines as seen in Fig. 3. The effect of MCF can be observed for the following two cases: (1) when the two wires (aggressor and victim) transition is in the same direction (in-phase), the C_{CM} has no effect and thus MCF=0 and (2) the worst case occurs for opposite transition (out-phase) in aggressor and victim line which leads the factor MCF=2. Therefore, the out-phase crosstalk delay can be concluded as worst case delay in high-speed global VLSI interconnects.

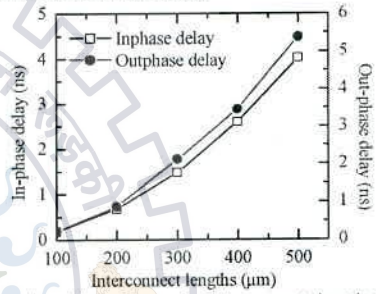

Figure 4. Propagation delay with varying interconnects lengths for MLGNR of N_{layer} = 4.

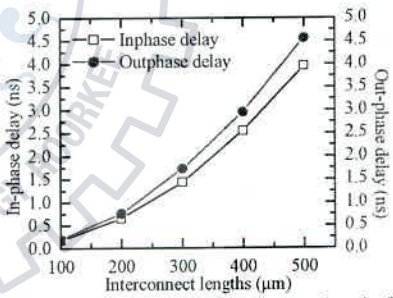

Figure 5. Propagation delay with varying interconnects lengths for MLGNR of N_{layer} = 10.

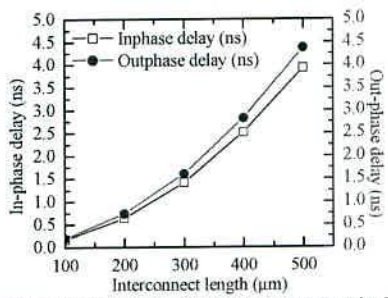

Figure 6. Propagation delay with varying interconnects lengths for MLGNR of N_{layer} = 20.

Table I summarizes the percentage improvement in crosstalk delays for MLGNR (N_{layer} = 20) with respect to MLGNR (N_{layer} = 4, 10). It is observed that propagation delay under the influence of crosstalk is significantly improved for MLGNR N_{layer}=20 for higher interconnect lengths. This fact can be understood using the concept of conducting channels that depends on the number of layers and widths of GNRs. From energy band diagram of graphene [18], it can be realized that the number of conducting channels varies with thickness of GNR layers due to the flow of electron concentration. The increasing thickness of GNR also increases the number of conducting channels resulting in lesser delay. Therefore, MLGNR with N_{layer} = 20 has lesser crosstalk effect as compared to the MLGNR with N_{layer} = 4 and 10.

TABLE I. PERCENTAGE IMPROVEMENT IN CROSSTALK DELAYS FOR MLGNR (N_{LAYER}=20) AT GLOBAL INTERCONNECT LENGTHS

Interconnect lengths (μm)	% improvement in in-phase delay for MLGNR (N_{layers}=20) *w.r.t.*		% improvement in out-phase delay for MLGNR (N_{layers}=20) *w.r.t.*	
	N_{layer} = 4	N_{layer} = 10	N_{layer} = 4	N_{layer} = 10
100	2.21	0.83	14.78	2.54
200	2.75	1.03	15.40	3.96
300	3.63	1.19	17.22	4.14
400	5.31	2.03	18.73	4.38
500	9.86	3.87	24.06	6.81

V. CONCLUSION

This research paper presents equivalent *RLC* model of MLGNR interconnects by considering the effect of scattering and width of GNR. Propagation delay under the effect of dynamic crosstalk is compared for different number of GNR layers using two-coupled line bus architecture employing CMOS driver. The crosstalk delay is significantly improved for MLGNR with higher number of layers at global interconnect lengths as compared to the lower one. Therefore, MLGNR with higher number of layers can be considered as potential material for future high-speed global VLSI interconnects.

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Analysis of MWCNT and MLGNR Interconnects: Impact on Delay and Area

Manoj Kumar Majumder, Narasimha Reddy K., B. K. Kaushik and S. K. Manhas

Abstract—**This letter presents a comparative analysis between multi-layer GNR (MLGNR) and multi-walled CNT (MWCNT) at different global interconnect lengths in terms of delay and area. An accurate analytical model of MLGNR and MWCNT is presented in time domain by using both the multi-conductor transmission line (MTL) formulation and the equivalent single conductor (ESC) model. Using a driver-interconnect-load system, an analytical expression of delay is proposed that exhibits significant accuracy. As compared to the HSPICE simulation results, the analytical delay model exhibits an average error of 6.29% and 9.37% for MLGNR and MWCNT interconnects, respectively. It is observed that the similar delay performance is obtained for fewer numbers of shells using MWCNT as compared to the number of MLGNR layers. Therefore, on an average, an MWCNT requires 54.5% lesser area as compared to the MLGNR interconnects for the similar performance of delay.**

Index Terms—**Multi-walled carbon nanotube (MWCNT), multi-layer graphene nanoribbon (MLGNR), interconnect, nanotechnology, propagation delay, area.**

I. Introduction

During recent past, multi-walled carbon nanotubes (MWCNTs) and multi-layer graphene nanoribbons (MLGNRs) have drawn much attention in scientific research due to their unique physical properties such as high thermal conductivity, current carrying capability, mechanical strength, etc [1-4]. MLGNRs can be considered as unrolled MWCNTs formed by hexagonal rings of carbon atoms. Both the MWCNT and MLGNR can support large current densities upto 10^9A/cm^2 and have long mean free paths ranging from 1-5μm. However, from the fabrication point of view, MLGNR is preferred over MWCNT due to its better controllability [1, 2].

This letter primarily analyzes the delay performance for MLGNR and MWCNT based driver-interconnect-load (DIL) system. The interconnect line in DIL, driven by a CMOS driver, is modeled by using an equivalent single conductor (ESC) line of either an MLGNR or an MWCNT interconnect as shown in Fig. 1. Using the DIL setup, an analytical expression is presented for output voltage waveform and delay. At different interconnect lengths; the number of shells in MWCNT is obtained for a delay performance that is equivalent to a fixed numbers of layers in MLGNR. Later on, the area comparisons are also made.

Manoj Kumar Majumder, Narasimha Reddy K., B. K. Kaushik and S. K. Manhas are with the Microelectronics and VLSI Group, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, INDIA (e-mail: manojbesu@gmail.com).

II. ESC Model

Based on the multi-conductor transmission line (MTL) formulation [2], this section presents an ESC model of MLGNR and MWCNT interconnects. The MLGNR (or MWCNT) have s numbers of layers (or shells) with an interlayer (or intershell) distance $\delta = 0.34$nm [2, 4]. The total number of layers (N_{layer}) and shells (N_{shell}) in MLGNR and MWCNT primarily depends on their thickness and outershell diameter (D_{outer}), respectively. Therefore, the areas of MLGNR and MWCNT are obtained as ($= w.t$) and $\pi(D_{outer}/2)^2$ respectively, where w, t represents the width and thickness of MLGNR respectively.

The ESC model of MLGNR or MWCNT is shown in Fig. 1 where the interconnect parasitics (*i.e.*, resistance, inductance and capacitance) are modeled using the number of conducting channels (N_{ch}) associated with each layer (or shell) in MLGNR (or MWCNT). N_{ch} takes into accounts the effect of spin and sub-lattice degeneracy of carbon atoms and depends on the number of sub-bands, Fermi energy, temperature and dimensions of MLGNR and MWCNT [4]. N_{ch} for MLGNR and MWCNT can be expressed as [3, 4]

$$N_{ch(MLGNR)} = a_0 + a_1 w + a_2 w^2 + a_3 E_F + a_4 w E_F + a_5 E_F^2 \quad (1)$$

and

$$N_{ch(MWCNT)} \approx \begin{cases} k_1 T D_i + k_2, & D_i > d_T/T \\ 2/3, & D_i \le d_T/T \end{cases} \quad (2)$$

where, a_0 to a_5 are the constant parameters for metallic GNRs at room temperature (300K) with Fermi energy $E_F > 0$ [3]. On the other hand, D_i represents the diameter of i^{th} shell in MWCNT, k_1 and k_2 are equivalent to 2.04×10^{-4}nm^{-1} K^{-1} and 0.425 respectively [4]. The thermal energy of electrons and the gap between the sub-bands determines the quantitative value of d_T which is equivalent to 1300nmK at room temperature (T=300K) [4]. Thus, the total numbers of conducting channels (N_{total}) in an MLGNR (or MWCNT) are obtained by the summation of N_{ch} associated with each layer (or shell).

The N_{total} is used to model the scattering resistance (R'_{ESC}) that primarily arises due to the confinement of carriers in a quantum wire (*i.e.*, CNT) having length longer than the mean free path (*mfp*) of electrons and can be expressed as (3). MLGNR or MWCNT interconnect is terminated by a lumped contact resistance (R_{cESC}) that exhibits the imperfect metal-nanotube contact resistance with a typical value of 3.2kΩ [4].

$$R'_{ESC} = h/4e^2 N_{total} \quad (3)$$

The effective *p.u.l.* total inductance (L'_{ESC}) in Fig. 1 is the summation of kinetic and magnetic inductances that primarily

represents the stored energy in magnetic field and inertial mass of mobile charge carriers respectively. Therefore, the effective *p.u.l.* kinetic (L'_{kESC}) and magnetic (L'_{eESC}) inductances of the ESC model can be expressed as [2, 4]

$$L'_{kESC} = L'_{k0}/N_{total}\,; \text{ where } L'_{k0} = h/2e^2 v_F \tag{4}$$

and

$$L'_{eESC} = (1/N_{total})\left[\mu_0\varepsilon_0/C'_{eESC0}\right] \tag{5}$$

where v_F represents the Fermi velocity of CNT and graphene ≈ 8×10^5m/s and C'_{eESC0} is the effective *p.u.l.* electrostatic capacitance of the ESC embedded in free space.

The outermost shell in MWCNT experiences an electrostatic capacitance (C'_{eESC}) with respect to the ground that appears in series with the quantum capacitance (C'_{qESC}) as shown in Fig. 1. Therefore, the effective *p.u.l.* C'_{eESC} and C'_{qESC} can be expressed as [1, 2]

$$C'_{eESC} = \left[2\pi\varepsilon/\cosh^{-1}(H/D_{outer})\right] \tag{6}$$

$$C'_{qESC} = N_{total}C'_{q0};\text{ where } C'_{q0} = 2e^2/hv_F \tag{7}$$

where H represents the distance between the center of MWCNT and ground plane.

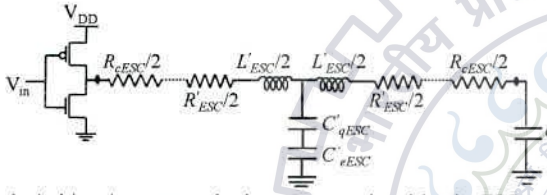

Fig. 1. A driver-interconnect-load system, constituted by the ESC model of either an MLGNR or an MWCNT interconnect

III. Transient Analysis of MTL and ESC Models

The transient analysis of the DIL (Fig. 1) is obtained using both the conventional MTL [2] and the reduced ESC models. The interconnect line is terminated by a load capacitance C_L = 10fF. For a rising input of 1V, the output response in frequency domain can be expressed as

$$V_{out}(s) = \frac{(C_Q+C_E)}{\left[\begin{array}{l} s^2\left\{R^2C_QC_EC_L+LC_L(C_Q+C_E)+LC_QC_E\right\} \\ +s\left\{2RC_L(C_Q+C_E)+RC_QC_E\right\}+(C_Q+C_E)\end{array}\right]}V_{in}(s) \tag{8}$$

Taking inverse Laplace Transform,

$$V_{out}(t) = 10^{12}\left[\begin{array}{l}\left(2RC_L+RC_QC_E(C_Q+C_E)\right)+(C_Q+C_E)t \\ +(C_Q+C_E)\left\{\left(\tau_1^2\tau_2/\tau_1-\tau_2\right)e^{-t/\tau_1}\right\}\end{array}\right] \tag{9}$$

For a given interconnect length l, $R \approx (R_{cESC}+R'_{ESC}l)$, $L \approx L'_{ESC}l$, $C_Q \approx C'_{qESC}l$ and $C_E \approx C'_{eESC}l$. In expression (9), τ_1 and τ_2 represents the time constants and can be expressed as

$$\tau_1 = \frac{2A}{B-\sqrt{B^2-4A}} \quad \text{and} \quad \tau_2 = \frac{2A}{B+\sqrt{B^2-4A}} \tag{10}$$

where $A = \left[\begin{array}{l}\left(R_{cESC}+R'_{ESC}l\right)^2C'_{qESC}C'_{eESC}C_Ll^2 \\ +L'_{eESC}C_L\left(C'_{qESC}+C'_{eESC}\right)l^2 \\ +L'_{eESC}C'_{qESC}C'_{eESC}l^2\end{array}\right] \Big/ \left(C'_{qESC}+C'_{eESC}\right)l$

and $B = \left[\begin{array}{l}2\left(R_{cESC}+R'_{ESC}l\right)\left(C'_{qESC}l+C'_{eESC}l\right)C_L \\ +\left(R_{cESC}+R'_{ESC}l\right)C'_{qESC}C'_{eESC}l^2\end{array}\right] \Big/ \left(C'_{qESC}+C'_{eESC}\right)l$

The output voltage waveforms for MLGNR and MWCNT at different interconnect lengths of 100, 500 and 1000μms are shown in Figs. 2(a) and 2(b) respectively. It is observed that the output responses using the MTL and ESC models are in good agreement with each other.

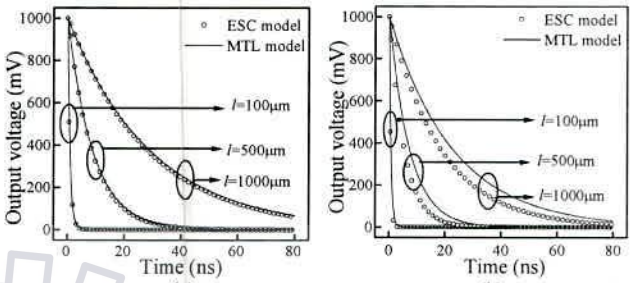

Fig. 2. Transient waveforms of the output voltages of (a) MLGNR (N_{layer} = 40) and (b) MWCNT (N_{shell} = 10) interconnects

IV. Area and Delay Analysis

The transient performance of the DIL system is characterized by the 90% time delay $\tau_{90\%}$. The $\tau_{90\%}$ is obtained using the transient response of the DIL setup, constituted by either an MLGNR or an MWCNT interconnect as shown in Fig. 1. Thus, $\tau_{90\%}$ can be expressed as

$$\tau_{90\%} = \frac{2.2(2A)}{B-\sqrt{B^2-4A}} \tag{11}$$

Using the analytical expression of (11), propagation delay is compared with the simulation results for MLGNR and MWCNT having different numbers of layers and shells as shown in Figs. 3(a) and 3(b) respectively. As compared to the HSPICE simulation results, the proposed delay model exhibits an average error of 6.29% and 9.37% for MLGNR and MWCNT interconnects respectively. Apart from this, Table I summarizes the number of shells and area in an MWCNT *vis-a-vis* the number of layers and area in an MLGNR for same delay at different global interconnect lengths. The percentage reduction in area for MWCNT as compared to the MLGNR is provided in Table II.

As the number of shells in MWCNT and the number of layers in MLGNR increases, the N_{total} value of MWCNT and MLGNR increases. The higher value of N_{total} effectively reduces the resistive and inductive parasitics that in turn significantly lowers the delay as shown in Fig. 3. As observed in Table I, a similar delay performance is achieved for fewer numbers of shells using MWCNTs in comparison to the layers in an MLGNR that encouragingly results in the reduction of area using MWCNT interconnects. Furthermore, Table II presents an improvement in percentage savings in area for MWCNT. The savings are more pronounced for higher number of MLGNR layers. On an average, an MWCNT requires 54.5% lesser area in comparison to the MLGNR interconnects.

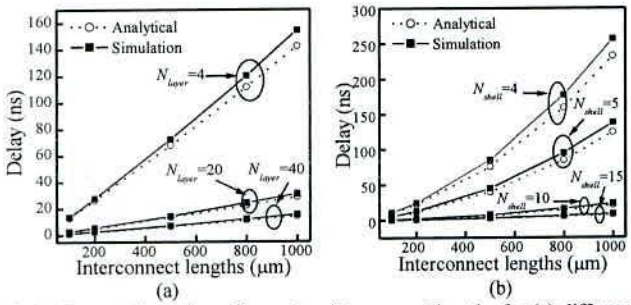

Fig. 3. Propagation delay with varying interconnect lengths for (a) different number of layers in MLGNR and (b) different number of shells in MWCNT

TABLE I
DEMONSTRATION OF AREA FOR MLGNR AND MWCNT INTERCONNECTS

Interc-onnect length (μm)	For same delay, the numbers of shells and area (nm^2) in MWCNT for the MLGNR layers and area of					
	N_{layer} =4	Area= 13.6nm^2	N_{layer} =20	Area= 64.6nm^2	N_{layer} =40	Area= 132.6nm^2
100	4	7.26	7	20.26	9	32.57
200	4	7.26	7	20.26	9	32.57
500	4	7.26	8	26.05	10	39.82
800	5	10.87	9	32.57	11	47.76
1000	5	10.87	9	32.57	12	56.45

TABLE II
PERCENTAGE REDUCTION IN AREA OF MWCNTS *W.R.T.* MLGNRS FOR SIMILAR DELAY PERFORMANCE

Number of layers in MLGNRs (Area in nm^2)	Percentage reduction in area at different lengths (μm) of				
	100	200	500	800	1000
4 (13.6)	46.6	46.6	46.6	20.1	20.1
20 (64.6)	68.6	68.6	59.7	49.6	49.6
40 (132.6)	75.4	75.4	69.9	63.9	57.4

V. CONCLUSION

This paper presented the transient voltage responses to a rising input for conventional MTL and the reduced ESC models. The obtained results are in good agreement with each other which validates the proposed ESC model. Using ESC model in DIL setup, an analytical expression of delay is obtained that exhibits an average error of 6.29% and 9.37% as compared to the simulation results for MLGNR and MWCNT interconnects, respectively. For same delay performance, the overall area is reduced by 54.5% for MWCNT as compared to the MLGNR at different interconnect lengths.

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Optimized Delay and Power Performances in Multi-layer Graphene Nanoribbon Interconnects

Narasimha Reddy K., Manoj Kumar Majumder, B. K. Kaushik, B. Anand and Pankaj Kumar Das
Department of Electronics and Computer Engineering
Indian Institute of Technology Roorkee
Roorkee, INDIA
narasimha_120@yahoo.co.in, manojbesu@gmail.com, bkk23fec@iitr.ernet.in, anandfec@iitr.ernet.in, pankaj_jkd@yahoo.co.in

***Abstract*—Multi-layer graphene nanoribbon (MLGNR) can be considered as an emerging interconnect material in current deep-submicron and nano scale technology. This research paper presents an equivalent *RLC* model for MLGNR interconnects that is primarily based on the geometry. Using the *RLC* model, propagation delay, power dissipation and power-delay product are analyzed for different number of layers in MLGNR. Based on the simulation results, approximate number of layers have been calculated for optimized delay and power performances at global interconnect lengths.**

***Keywords*—Graphene nanoribbon (GNR), multi-layer GNR (MLGNR), interconnect, propagation delay, power dissipation, power delay product (PDP), VLSI.**

I. INTRODUCTION

In modern VLSI technology, on-chip interconnect communication between devices and circuit blocks has become a complex and challenging task. The connection between miniaturized and closely packed transistors requires reduced wire cross-sections in the local levels, while the rapid growth of functional density and chip size leads to longer-distance communication in the global levels. Now-a-days, interconnect delay plays in a significant role with aggressive device scaling and becomes significant in the continuous improvements in device density and speed. As illustrated by the International Technology Roadmap for Semiconductors (ITRS 2010) [1], interconnect *RLC* delay dominates the gate delay in advanced technology nodes. Each international technology working group (ITWG) has identified the needs of new materials to meet future technology requirements, and it has assessed the potential for low dimensional materials [2].

Graphene, a two dimensional mono-atomic thick building block of a carbon allotrope, has emerged as an exotic material of the 21st century, and has received world-wide attention due to ambipolar carrier conduction [3]. Graphene has higher carrier mobility of more than 10^6cm^2/V-sec, and a defect density of ~1×10^{10}/cm^2 [4]. This mobility is better than the mobility reported for small gap InSb and also is practically independent of temperature, thus opening the possibility of room temperature ballistic transport at the sub-micrometer scale. Theoretically, it has been predicted that graphene nanoribbons (GNRs) will outperform the Cu interconnects for smaller widths less than 8nm [5]. The electronic states of GNRs largely depend on the edge structures. Zigzag edges provide the edge localized state with non-bonding molecular orbital's near the Fermi energy. They are expected to have large changes in optical and electronic properties from quantization [6-8]. Calculations based on tight binding model predict that zigzag GNRs are always metallic while armchairs can be either metallic or semiconducting, depending on their width *i.e.*, on number of hexagonal rings (N) present across the width of GNR that is fixed along with the length. However, recent DFT calculations show that armchair GNRs are semiconducting with an energy gap scaling with the inverse of the GNR width [9-10]. In ac-GNRs, metallic properties depends on the condition of N=3p-1 or 3p+2 whereas N=3p or 3p+1 satisfies the semiconducting properties in which p can be defined as an integer [9-11]. Apart from this, zz-GNRs are always metallic independent of N, where N is the number of hexagonal rings present across the width. Depending on the number of layers formed by the hexagonal rings of carbon atoms, GNRs can be categorized as single-layer GNR (SLGNR) and multi-layer GNR (MLGNR). The electrical conductance of SLGNR is relatively high. Hence, the modern interconnect applications prefer MLGNR because of their reduced equivalent resistance [12, 13].

This research paper primarily focuses on the analysis of propagation delay and power dissipation for MLGNR interconnects with different number of layers. Based on the simulation results, power-delay product (PDP) is also calculated at different global interconnect lengths from where optimum delay and power performances have been achieved. The organization of this research paper is as follows. Section I introduces the current research scenario and briefs about the structures and properties of GNRs. Section II presents the equivalent *RLC* models of MLGNR interconnects whereas the details of simulation setup are provided in section III. Comparative analysis of propagation delay and power dissipation for different MLGNR layers is presented in section IV. Finally, section V concludes the paper.

II. EQUIVALENT *RLC* MODEL FOR MLGNR INTERCONNECTS

The geometry of MLGNR over a metallic plane is shown in Fig. 1. The MLGNR is made of N_{layer} of single GNR layers with lengths l, thickness t and width W. As per the fabrication technology, the distance between two layers in MLGNR can be considered as δ=0.34nm. The number of graphene layers in MLGNR can be expressed as [13]

$$N_{layer} = 1 + Integer(t/\delta) \quad (1)$$

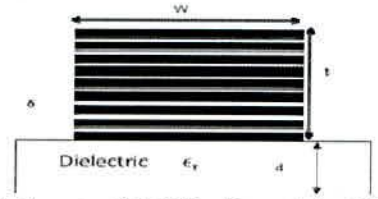

Figure 1. Geometry of MLGNR and its equivalent *RLC* model

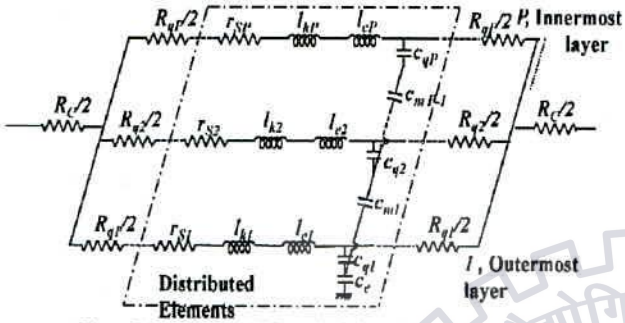

Figure 2. Equivalent *RLC* model of MLGNR interconnects

Based on geometry, an equivalent *RLC* model of MLGNR interconnect is shown in Fig. 2, where R_C, R_Q and R_S represent the equivalent resistances introduced by the imperfect contacts, the quantum effect, and the carriers scatterings, respectively. Contact resistance ($R_{MC} \approx 3.2\text{k}\Omega$) of MLGNR primarily depends on the quality of contact that can be determined during fabrication process. Quantum resistance (R_q) of each layer exists due to confinement of carriers in a quantum wire and can be expressed as [13-16]

$$R_q = \frac{h/2e^2}{N_{ch}N_{layer}} = 12.9\,k\Omega/N_{ch} \quad (2)$$

where h is known as Planck's constant, e is the electron charge and N_{ch} represents the number of conducting channels in a MLGNR sheet. N_{ch} depends on the number of sub-bands, width of GNR, Fermi energy, temperature and geometry (*i.e.*, ac-GNR or zz-GNR). It can be formulated as [16]

$$N_{ch} = N_{ch,electrons} + N_{ch,holes} = \Sigma_n \left[1 + \exp\left(E_{n,electron} - E_F / K_B T\right)\right]^{-1} + \Sigma_n \left[1 + \exp\left(E_F - E_{n,hole} / K_B T\right)\right]^{-1} \quad (3)$$

where E_F is the Fermi energy, $E_{n,electron}$, $E_{h,hole}$ are the energies of electron and holes, T is the temperature and K_B is Boltzmann constant. Equation (3) can be solved by using iterative method and curve fitting methods [16]. Quantum capacitance (C_q) exists due to the quantum energies stored in carriers that is a effect of quantum confinement and can be expressed as [17]

$$C_{q,channel} = \frac{4e^2}{hv_F} \approx 193aF \quad (4)$$

where v_F is the Fermi velocity of GNR $\approx 8\times10^5$m/s [9]. Apart from this, kinetic inductance (l_k) of MLGNR can be defined as the inertial mass of mobile charge carriers that will oppose the change in electric fields as an equivalent series inductance. It can be expressed as [17]

$$l_{k/channel} = \frac{h}{4e^2 v_F} \approx 8nH \quad (5)$$

Therefore, the total C_q and l_k of an MLGNR depends on the total number of conducting channels N_{ch} and can be expressed as [17]

$$C_Q = \frac{4e^2 N_{ch}}{hv_F} \approx 200.N_{ch}\,aF \quad (6)$$

$$l_k = \frac{4e^2 N_{ch}}{hv_F} \approx \frac{8}{N_{ch}}nH \quad (7)$$

The equivalent *RLC* model of Fig. 2 comprises of *p.u.l.* magnetic inductance (l_e) and electrostatic capacitance (c_e) that can be represented in terms of the stored energy in magnetic and electric fields respectively. Apart from this, per unit length mutual capacitance (C_m) and mutual inductance (l_m) exists between two GNR layers due to the electron tunnel transport phenomenon. It can be expressed as [13]

$$C_m^{(j-1,j)} = \frac{\varepsilon_0 w}{\delta} aF/\mu m \quad (8)$$

$$l_m^{(j-1,j)} = \frac{\mu_0 \delta}{w} nH/\mu m \quad (9)$$

where μ_0 and ε_0 represents magnetic permeability and electrostatic permittivity of free space respectively

III. Simulation Setup

This research paper analyzes the power and delay performances for MLGNR with different number of layers at global interconnect lengths ranging from 100μm to 1000μm by using the geometries suggested in [18]. Simulation setup uses a driver-interconnect-load (DIL) system employing CMOS driver at 32nm technology node for accurate estimation of delay. The reason behind is that transistor in a CMOS gate operates partially in linear region and partially in saturation region during switching. But, a transistor can be accurately approximated by a resistor only in the linear region. In the saturation region, the transistor is more accurately modeled as a current source with a parallel high resistance. The DIL system is driving by a supply voltage (V_{DD}) = 1V and terminated with a load capacitance C_L of 10aF [18] as shown in Fig. 3.

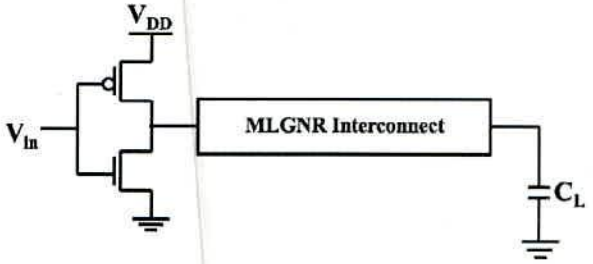

Figure 3. A driver-interconnect-load system