A LOW POWER SAR ADC DESIGN FOR MEDICAL IMPLANT DEVICES

A DISSERTATION

Submitted in Partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ELECTRONICS & COMMUNICATION ENGINEERING

(With Specialization in Microelectronics and VLSI)

By

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JUNE, 2013

CANDIDATE'S DECLARATION

I hereby declare that the work, which is being reported in the dissertation entitled, "**A Low Power SAR ADC Design For Medical Implant Devices**", which is submitted in the partial fulfilment of the requirements for the award of degree **Master of Technology** in **Microelectronics & VLSI**, submitted in the Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee (India), is an authentic record of my own work carried out from June 2012 to May 2013 under the supervision of **Dr. Sudeb Dasgupta**, Associate Professor and **Dr. Ashok K. Saxena**, Professor, Department of Electronics & Communication Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter embodied in the dissertation report to the best of my knowledge has not been submitted for the award of any other degree elsewhere.

Dated: 27/06/13

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CERTIFICATE

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ACKNOWLEDGEMENT

At the outset, I express my heartfelt gratitude to Dr. S. Dasgupta, Associate Professor and to Dr. Ashok K Saxena, Professor, Department of Electronics and Computer Engineering at Indian Institute of Technology Roorkee, for his valuable guidance, support, encouragement and immense help. I consider myself extremely fortunate for getting the opportunity to learn and work under their able supervision. I have deep sense of admiration for their innate goodness and inexhaustible enthusiasm. It helped me to work in right direction to attain desired objectives. Working under their guidance will always remain a cherished experience in my memory and I will adore it throughout my life.

My sincere thanks are also due to all the Research Scholars of my VLSI Design LAB without whom availing of lab facilities during non-working hours wouldn't have been possible. I also extend my sincere thanks to rest of the faculty in the Department of Electronics and Computer Engineering at Indian Institute of Technology Roorkee, for the technical knowhow and analytical abilities they have imbibed in us which have helped me in dealing with problems I encountered during the project.

I am greatly indebted to my family and all my friends, who have willingly applied themselves to the task of helping me with ample moral support and valuable suggestions. I would also like to extend my gratitude to all those persons who directly or indirectly helped me in the process and contributed toward this work. Finally, I would like thank God, whose gracious presence strengthened my faith which helped me to get through troublesome situations my work.

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ABSTRACT

The Analog to Digital Converters represent one half of the link between the world we live in - analog - and the digital world of computers, which can handle the computations required in digital signal processing. This dissertation report is focused on ADCs for biomedical applications, where ultra-low power consumption and small form factor is required with medium frequency range. Successive approximation register analog-to-digital converters (SAR ADCs) are attractive when low power operation is important and high-speed operation is not a concern. SAR ADCs appear to be most promising candidate for implantable biosensors, such as implantable heart-rate sensors or sensors used in neuroprosthesis applications.

This dissertation report presents a 10-bit successive approximation register ADC design for medical implant devices. Two step capacitor switching is implemented using delay based control logic to reduce DAC power consumption. A dual supply scheme is used to further reduce the power consumption of SAR Logic. SAR logic is operated at 400mV while other analog circuits at 1V. Maximum simplicity is provided on the ADC's high voltage level architecture, while all the complicated circuit for charge sharing switching scheme is implemented in lover voltage level along with the digital control logic circuit. Full range sampling is used to minimize the required voltage level. The ADC is designed in GPDK 90nm process and simulated in Cadence Virtuoso Front and Back Design Environment. It consumes 24nW and achieves an ENOB of 9.2 bits.

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LIST OF ABBREVIATION

Abbreviation	Meaning
ADC	Analog to Digital Converter
DAC	Digital to Analog Converters
NMOS	N-Type Metal Oxide Semiconductor
PMOS	P-Type Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
LSB	Least Significant Bit
MSB	Most Significant Bit
INL	Integrated Non-Linearity
DNL	Differential Non-Linearity
SNR	Signal to Noise Ratio
SoC	System on Chip
SAR	Successive Approximation Register
MIM	Metal-Insulator-Metal
SCE	Short Channel Effect
RSCE	Reverse Short Channel Effect
FSM	Finite State Machine
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FOM	Figure of Merit
SNDR	Signal to Noise Distortion Ratio
SFDR	Spurious Free Dynamic Range

Chapter 1

INTRODUCTION

The Analog to Digital Converters (ADCs) are heart of a system using digital signal processing. In the modern era a rapid evolution in digital signal processing is noticed. All the real world signals are analog. Analog to digital converters are the only medium which acts as intermediate link between the real world analog signals and modern digital signal processors. ADCs are a matter of research from long time and still lot of research is going on for different types of ADCs to improve their accuracy, to increase the speed and to reduce the power consumption, simultaneously.

As the technology has grown up the use of electronics is increased significantly in medical science. The evolution in the semiconductor technology has made it feasible to have system-on-chip (SOC) having very low power consumption. The SOCs specially designed for low power applications can be operated with a small battery power for a long time. This feature has invoked the use of SOCs in medical implantable devices significantly. Cardiac pacemakers, neuroprosthesis sensors, and implantable cardiac defibrillators etc. are such medical implant devices. ADCs are very critical components in medical implant devices in terms of power consumption. Power consumption of such devices should be extremely low in order to operate for 5-10 years [1], on a small non-rechargeable battery power. In nowadays ADCs are available for medical implant devices with ultra-low power consumption. But there is still need to reduce the power consumption and form factor without degrading the ADC performance.

1.1 ADC Terminology

There are a lot of ADC designs are available in the market. So, we need a baseline to compare the performance of various ADCs. There are many parameters on which an ADC performance can be compared. Some important parameters which are standardized worldwide are covered in this section. These parameters are characterized in two major sections 1) static parameters and 2) dynamic parameters.

The parameters which characterize the DC input characteristics of the ADC are called static characteristics. Thus, static parameters are measured with DC input voltage. The dynamic parameters are measured with varying input signal and they tell us the frequency response of ADC.

1.1.1 Static Parameters

For an ADC the error calculation is done by the taking the difference between the theoretical input and the actual input which is required to generate a particular code at the output. There are different types of errors defined as static parameters for an ADC which are listed following.

Analog Resolution:

The smallest increment in the analog input voltage corresponding to the change of output code by 1 LSB is called the analog resolution of the A/D converter. As an example, for a 10-bit ADC with a full scale input range of 0V-1V the resolution is about 0.97mV ($(1-0)/2^{10}$).

Offset Error:

The difference between the theoretical input and the actual input voltage that is needed to change the initial output 000...00 to the next output 000...01 is called offset error of the ADC. Fig. 1.1 (a) shows ideal 3-bit ADC transfer characteristic. Offset error is shown in Fig. 1.1 (b)

Gain Error:

The difference between the slope of the lines connecting the initial output transition 000...00 to 000...01 and full scale output transition 111...10 to 111...11 on the input output graph for actual and the theoretical transitions. Fig. 1.1 (b) shows the gain error for a 3-bit ADC.

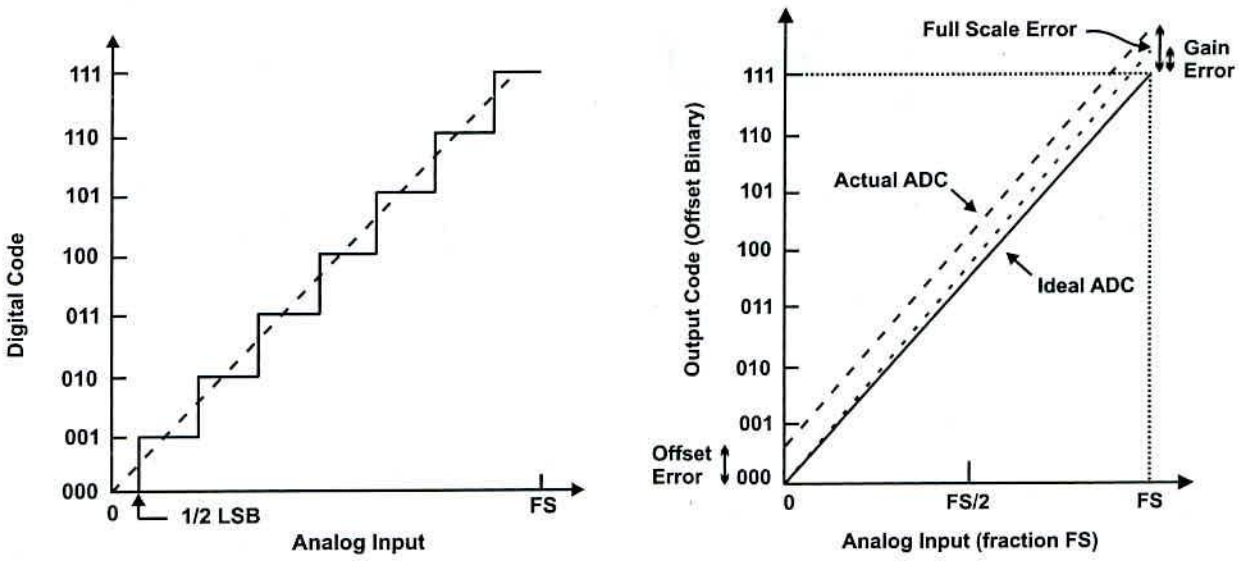


Figure 1.1: (a) Ideal 3-bit ADC Output (b) Offset and gain error

Differential Non-Linearity Error (DNL):

The difference in the step size of an ideal ADC and that of real ADC is called differential non-linearity error. If the transition width (bin) of each code of ideal ADC is Δ and the bin for k^{th} output code of ADC is Δ_k, then the differential nonlinearity error for the k^{th} bit will be:

$$DNL_k = \frac{\Delta_k - \Delta}{\Delta} \tag{1.1}$$

Integral Non-Linearity Error (INL):

The INL shows the difference of the transfer function of a real ADC from the ideal ADC. As the name specifies INL is summation of previous differential nonlinearity errors of all the previous bits.

$$INL_k = \sum_{1}^{k} DNL_i \tag{1.2}$$

1.1.2 Dynamic Parameters

The dynamic parameters tell us about the speed and the frequency response of the analog components of the ADC. These parameters are defined in terms of frequency, data-rate conversion or time or defined corresponding to dynamic conditions. The quality of dynamic features is determined as their capacity to remain same for the full dynamic operation range.

Signal-to-Noise Ratio (SNR):

SNR accounts for the noise introduced by the circuit itself and the quantization noise for the entire Nyquist interval. For the calculation of SNR of an ADC a sinusoidal signal having peak-to-peak voltage equal to the full scale input range of the ADC is applied to its input. The output of the ADC obtained is a quantized sinusoidal signal along with the noise added by the ADC circuit. The Fourier transform of the output is calculated. SNR is given by the ratio of amplitude at the input signal frequency and root mean square value of other frequency bins excluding the harmonic noise. The SNR is generally dependent on the frequency of the input signal.

For an ideal ADC the noise present in the output signal is only due to the quantization error. Thus, the SNR of the ideal ADC is only dependent on the number of bits N which decide the quantization error. For an N-bit ideal ADC the expectation value of the quantization error voltage will be given by:

$$E\{\in^2\} = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} \in^2 d\in = \frac{\Delta^2}{12} \tag{1.3}$$

where, Δ is the resolution of the ADC. The rms value (V_{rms})of full-scale peak-to-peak input voltage (V_{FS}) is given by:

$$V_{rms} = \frac{V_{FS}}{2\sqrt{2}} = \frac{2^N \times \Delta}{2\sqrt{2}} \tag{1.4}$$

Thus the SNR for an N-bit ideal ADC is:

$$SNR = \left(\frac{V_{rms}}{\sqrt{E\ \in^2}}\right) = 2^N\sqrt{1.5} \tag{1.5}$$

Generally the SNR is expressed in db.

$$SNR_{dB} = 6.02N + 1.76\ dB \tag{1.6}$$

Signal-to-Noise-and-Distortion Ratio (SINAD, S/N+D or SNDR):

SINAD is same as that to SNR in terms of definition but the difference is that the distortion occurred due to the input sine wave frequency is also added to the noise for the noise calculation. For an M-point FFT of the output of ADC with sinusoid signal applied at its input, if the frequency of the input signal f_{in} resides in the frequency bin m, then the SNDR of the ADC is given by:

$$\mathrm{SNDR} = 10\log\left[A_m^2\left(\sum_{k=1}^{m-1}A_k^2 + \sum_{k=m+1}^{M/2}A_k^2\right)\right] \tag{1.7}$$

where, A_k is the amplitude of the k^{th} frequency bin.

Very often several bins close to fundamental frequency f_{in} are not accounted in the calculation to avoid the spectral leakage. The SNDR depends on the frequency and the amplitude of the input signal and degrades at higher amplitude and frequency.

Effective Number of Bits (ENOB):

ENOB is simply a way of representing the SNDR in terms of bits rather than in decibels. The representation in bits is done by solving the ideal ADC SNR equation:

$$\mathrm{SNR} = 6{:}02N + 1{:}76\ \mathrm{dB}$$

using the measured SNDR, for the number of bits N. The ENOB is thus given by:

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76\ \mathrm{dB}}{6.02\ \mathrm{dB/bit}} \tag{1.9}$$

1.2 Selection of the Right ADC Architecture

Among the different ADC architectures, choosing the right architecture is a very crucial decision. For medical implant application the requirement is extremely low power consumption with a sampling frequency range from 1-100 KHz approximately. Sampling rate with respect to resolution of different ADC architecture's is shown in Fig. 1.2 [2]. Sigma-delta ADCs have high resolution but though are slow. Thus, Sigma-delta ADCs are commonly used in industrial management, audio and voice band. The Successive

Approximation (SAR) ADCs have a medium frequency range and has a resolution from 8 bits to 18 bits practically and are suitable for data acquisition. Flash ADCs are used for high frequency and low resolution. Pipeline ADCs are used at GHz range up to a resolution of 16 bits.

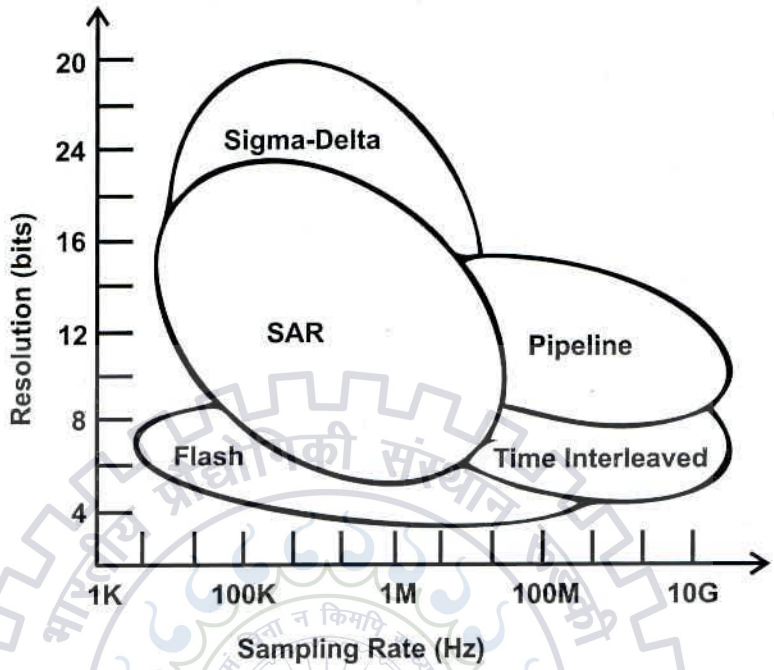


Figure1.2: Sampling rate vs. resolution of various ADC'S types [2]

SAR ADCs appear to be best candidate for medium frequency range and low power consumption. The SAR logic and comparator consume most of the power for lower resolution SAR ADCs (<6b), while charging and dis charging of capacitive array DAC is most power consuming for higher resolution ADCs. Since the capacitive array size increases exponentially with increasing resolution, so the power consumption and the area also increase exponentially.

1.3 Thesis Contribution

This dissertation report presents a SAR ADC design at 90nm technology. Designing an extremely low power ADC for such a low sampling rate at deep sub-micron technologies (≤ 90nm) incur significantly different problems. One of the big problem is that leakage i.e. sub-threshold conduction increases with reducing device size. For the digital circuit design leakage increases the static power consumption while for the analog circuit design leakage deteriorates the ADC performance as well. In a capacitive array SAR ADC the input is

sampled and held on the capacitor array in the form of stored charge. This stored charge gets altered significantly because of high leakage through the sampling switches deteriorating the performance. Low leakage circuit design techniques are employed to address the issue. Apart from leakage high gate current of MOS transistors [3] at deep submicron technologies is a great matter of concern. The capacitive arrays of SAR ADCs are connected to the comparator for the comparison. The charge stored on capacitive DAC gets altered significantly by the gate current of a MOS transistor of the comparator to which it is connected. To resolve this issue the comparator is designed in two stages. The first stage is specially designed in such a way that it reduces the corresponding gate current to an acceptable range. The next stage of the comparator is designed to amplify the output of first stage and to obtain rail to rail output.

This thesis presents a 10-bit SAR ADC design that achieves ultra-low power consumption of 24nW at an operating frequency of 1kS/s with an ENOB of 9.2 bits near the Nyquist input frequency. A dual supply scheme is used to minimize the power consumption in SAR logic as well as maintaining high ENOB. SAR Logic is operated at 0.4V supply and analog supply is kept at 1V.

1.4 Thesis Organization

This thesis consists of six chapters. The chapters are organized as following.

Chapter 2 provides the basic understanding about SAR ADC architecture and its working principle. It describes the principles and working of the differential SAR ADC architecture which is implemented in the dissertation work. It also describes about the different techniques which are employed to the differential SAR ADC architecture to reduce the power consumption and to improve the ADC performance.

Chapter 3 is about the design and implementation of analog components required for the differential SAR ADC. It deals with the capacitor array DAC design. The proposed design of delay circuit for 2-step capacitor switching implementation is presented in this chapter. The proposed two stage comparator design to reduce the gate current of the input of the comparator is also presented here. It also shows the design of sampling switch and level shifter employed in the implemented SAR ADC.

Chapter 4 deals with the design of the digital components employed in the implemented SAR ADC. It shows the SAR logic design, 4-bit counter design, decoder and multiplexer

design. The design of proposed transmission gate T flip-flop with enable and asynchronous reset input is shown in this chapter. The design of different D flip-flops optimized with SAR logic operation is presented here. This chapter also presents the D flip-flop design incorporated with the delay circuit used for 2-step capacitor switching implementation.

Chapter 5 shows the final simulation results of the ADC. It shows the output waveform of the ADC. The layout of the different sections of the ADC and the complete layout is also shown here. The simulated static and dynamic performance of the implemented SAR ADC is also shown here. This chapter also shows the total power consumption and the power consumption of the different sections of the ADC is shown here.

Chapter 6 concludes this dissertation report.

Chapter 2

SAR ADC

2.1 SAR ADC Basic Architecture

Fig. 2.1 shows the simple SAR ADC architecture. It consist of a DAC, a track and hold device, a comparator, an N-bit shift register and a SAR logic controller. A SAR ADC utilizes binary search algorithm.

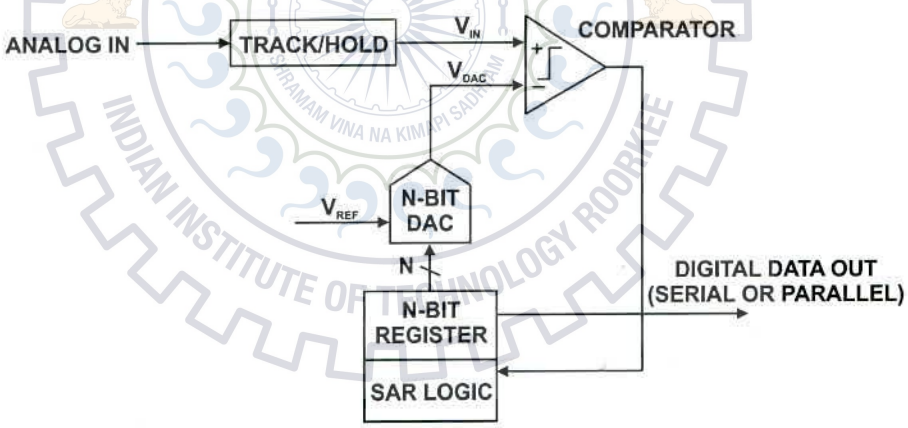


Figure 2.1: SAR ADC Basic architecture

The input (V_{IN}) which is to be converted to digital signal is applied to track and hold device. To apply successive approximation algorithm the MSB of N-bit shift register is set to HIGH keeping the other bits LOW. The DAC converts the output of shift register to the corresponding analog voltage. All the bits of N-bit shift register have binary weightage (MSB = $V_{REF}/2$, MSB-1 = $V_{REF}/4$ etc.). Since the weightage of MSB is $V_{REF}/2$, thus the DAC output is $V_{REF}/2$. The DAC output is then compared with the sampled input analog voltage (V_{IN}) by the comparator. If $V_{IN} > V_{REF}/2$ the output of comparator is HIGH and LOW if V_{IN} is less

than $V_{REF}/2$. Now the decision for MSB is taken depending upon comparator output. If comparator output is HIGH (LOW), MSB is kept HIGH (LOW) for the entire conversion process. The SAR logic now moves to MSB-1 and is set to HIGH for the next comparison. The process continues until all the bits up to LSB are decided. The converted digital output is now available at N-bit shift register output.

2.2 Description of Internal Major Blocks

The SAR consists of the three major sections. Firstly the capacitor array DAC, the SAR logic and the comparator.

2.2.1 Capacitor Array DAC

Fig. 2.2 shows a 5-bit DAC using binary weighted capacitor array. R-2R resistive ladder network can also be used but are avoided to constant power dissipation in the resistive network. Capacitive array DAC is mostly used for low power consumption. The capacitor array consists of one additional capacitor equal to that of LSB capacitor. Switches are used to connect the bottom plate of the capacitors to predefined voltage levels. A comparator is used to compare top plate voltage level of capacitors to a reference voltage. Three steps are required for a conversion to be accomplished.

Sample Mode:

In the sample mode input is sampled at the top plates of the capacitor array of the DAC. Firstly the top plates of the capacitor array are connected to ground and the bottom plates are connected to the input voltage through the switches as shown in Fig. 2.2. The capacitor array gets charged proportional to the input voltage.

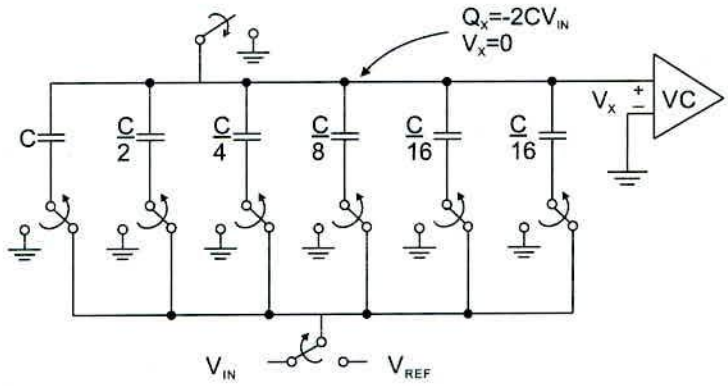


Figure 2.2: 5-bit A/D converter illustrating the sample mode operation [4]

Hold Mode:

Fig. 2.3 shows operation for hold mode of the DAC. The switch which earlier had connected the top plates of the capacitor array to the ground is opened. The bottom plates of the capacitor array are connected to ground. Because of charge conservation on top plates of the capacitor array the potential on top plate becomes – V_{IN}.

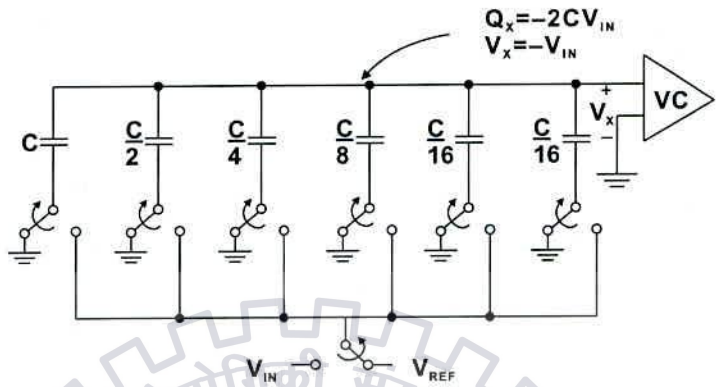


Figure 2.3: Pre-redistribution hold mode operation [4]

Charge Redistribution Mode:

Fig. 2.4 shows charge redistribution. Once the input gets sampled on the top plates of the capacitor array in the hold mode the comparison of bits starts successively from MSB to LSB. Firstly for the MSB testing the bottom plate of the MSB capacitor (largest capacitor) is connected to the reference voltage V_{REF}. The capacitor array now acts as a voltage divider network with two equal capacitors in series. Thus the voltage (V_X) at top plates of the capacitor array gets raised by $V_{REF}/2$. Since V_X was equal to $-V_{IN}$ due to the stored charge on the capacitor array, V_X now becomes:

$$V_X = -V_{IN} + V_{REF}/2$$

The comparator senses the polarity of V_X. The output of comparator is HIGH if $V_X < 0$ and LOW if $V_X > 0$. Alternatively this means comparator goes HIGH if $V_{IN} > V_{REF}/2$ otherwise goes LOW if $V_{IN} < V_{REF}/2$. Thus MSB is set to HIGH for $V_{IN} > V_{REF}/2$ or set to LOW for $V_{IN} < V_{REF}/2$ accordingly. The switch connecting MSB capacitor to V_{REF} S1 is returned to GND only if MSB is LOW. SAR logic now moves for the comparison of MSB-1 bit. Bottom plate of MSB-1 capacitor is connected to V_{REF} and comparison is made for the next decision. The process continues in a similar manner until all the bits are decided. The converted digital output is now available. N-bit conversion requires N charge redistribution cycles.

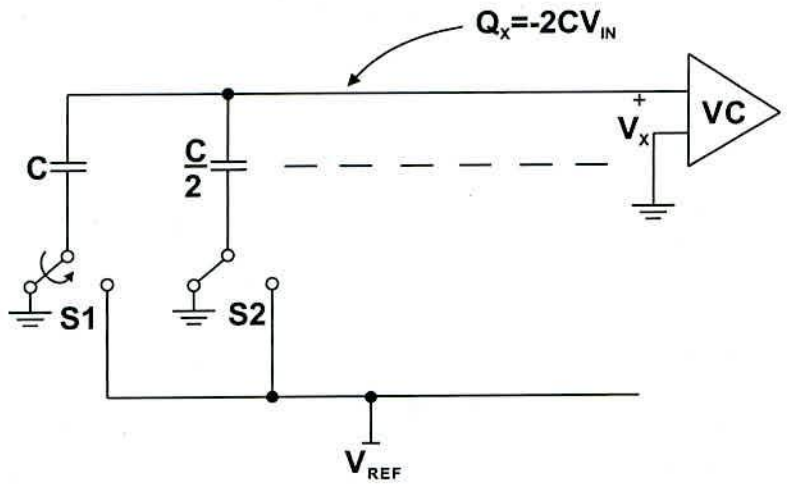


Figure 2.4: Charge Redistribution Mode Operation [4]

2.2.2 Comparator

A comparator compares two analog inputs and generates a binary output depending upon the result of the comparison. The input terminals of the comparator are generally named as inverting terminal and non-inverting terminal. The comparator output is HIGH if non-inverting terminal voltage is greater than the inverting terminal voltage. This behavior is defined for an ideal comparator. A practical comparator has many limitations such as it has a finite gain, input offset slew-rate limitation etc. The comparator has a smaller delay time if the input voltage difference is larger but it also has a upper limit due to slew-rate. Because of the input offset voltage the comparator output does not changes if the voltage difference at the input is smaller than the input offset voltage of the comparator.

2.2.3 SAR Logic

The SAR control logic consists of several D flip-flops and a processor which controls the inputs of the D flip-flops. The processor generates the control signals which control the switches of the capacitor array DAC and the multiplexes to connect the output of comparator to D flip-flops or to memorize the result of data conversion.

Fig. 2.5 shows the controller has three inputs clock, clear and the output of comparator. Depending upon the output of the comparator the current state of the ADC the processor generates the control signal for the switches of capacitor array DAC for the next bit comparison and stores the current bit result into the corresponding D flip-flop.

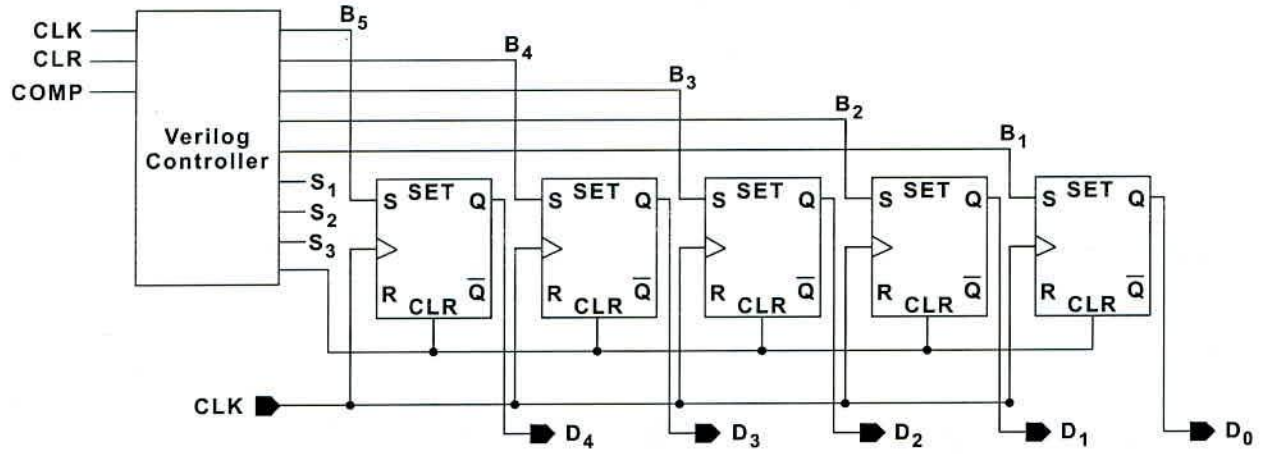


Figure 2.5: Schematic of SAR control logic

2.3 Implemented SAR ADC Differential Architecture

A 10-bit differential SAR ADC architecture is shown in Fig. 2.6 (a) and the switching waveform of capacitor array DAC is shown in Fig. 2.6 (b). It consists a binary weighted capacitive DAC, a two stage reduced gate current dynamic latched comparator, an ultra-low-power delay based SAR logic employing 2 step capacitor switching, and a contention mitigated low power level shifters between the low voltage SAR control logic and high voltage analog sections. Differential ADC architecture is utilized to minimize the common-mode noise.

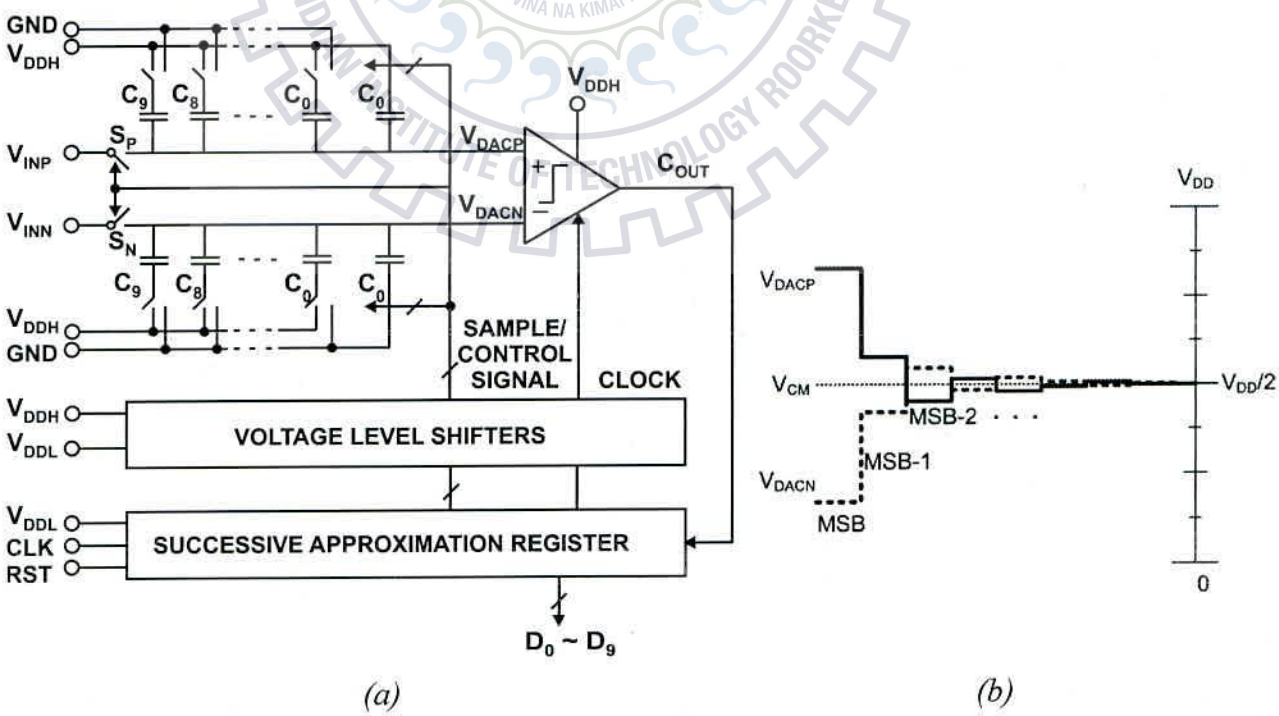


Fig. 2.6: (a) Differential SAR ADC architecture (b) Waveform of DAC switching [5]

2.3.1 Top Plate Sampling

In a conventional SAR ADC [4] top plates are set at a fixed voltage or reset to ground, the sampling of input voltage is done on the bottom plates of the capacitor array. Commonly one of the power rails are chosen as a reference voltage in order to avoid an extra voltage level (V_{REF}=V_{DD}). But the most common problem in choosing the rail voltage as reference voltage is that the output goes beyond the rails when input sampling range is rail to rail. The input sampling range can be decreased to solve this problem but at a cost of reduced signal to noise ratio.

A different sampling and switching scheme is used in this ADC in order to avoid the DAC output going beyond the rails and also to use full range input sampling. MSB is preset in this ADC and the sampling is done at the top plates of the capacitors instead of bottom one to achieve full range input sampling keeping DAC output within the rails. As the Fig. 2.7 shows, the inputs to be sampled are connected initially to the top plates of the capacitor array through the sampling switches and MSB is set to HIGH keeping all the other bits LOW, simultaneously. In the next clock cycle the sampling switches are opened and the input data gets sampled on the top plates of the capacitor array. The input is applied to the comparator for the first comparison. MSB in this case is a sign bit. If V_{DACP} is greater than V_{DACN}, the MSB remains HIGH or goes LOW otherwise. The next approximation step starts by setting MSB-1 to HIGH, and again comparison is performed by the comparator in the same manner. The process continues in a similar manner until all the 10-bits are compared.

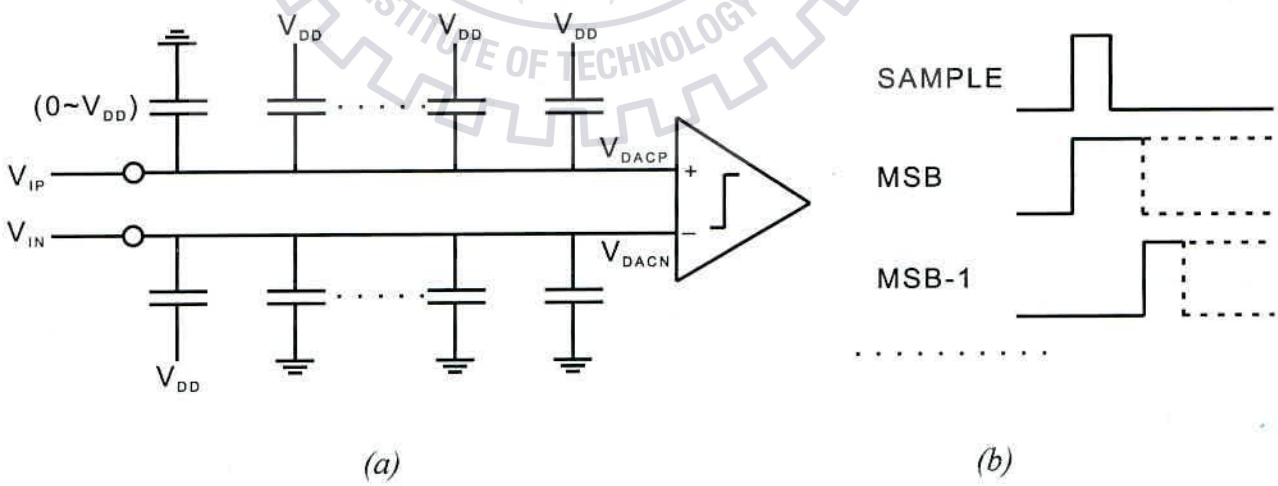


Fig. 2.7: (a) Capacitive DAC sampling phase with MSB preset (b) Related time sequence [1]

As shown in Fig. 2.7 bottom plates of MSB capacitors are connected to opposite rail in comparison to entire capacitive array. If sampled voltage V_{IN} is greater than V_{IP}, MSB is reset. The polarity of bottom plates of the MSB capacitors changes. The top plate voltage of the two capacitor arrays now becomes:

$$V_{DACP} = V_{IP} + V_{REF}/2$$

$$V_{DACN} = V_{IN} - V_{REF}/2$$

$$V_{DACP} - V_{DACN} = V_{IP} - V_{IN} + V_{REF}$$

Since the difference $V_{DACP} - V_{DACN}$ gets added by a voltage V_{REF} and V_{IP} and V_{IN} are within the supply rails, V_{DACP} now becomes greater than V_{DACN}. Thus, the DAC output remains within the rails for the entire conversion cycle. For full-scale sampling of the input the common mode of the differential input is equal to the mid-rail voltage and thus the common mode voltage of the output of the DAC is also at the mid-rail voltage. If the common mode input of the comparator is constant it reduces the dynamic offset of the comparator [6].

2.3.2 2-Step Switching

2-step switching is implemented in this design to reduce the switching power of the capacitor array DAC. This section shows the advantage of 2-step switching method over single step switching method. For the ease of computation the calculations are carried out for only 2-bit capacitor array DAC.

The conventional 1 step switching is shown in Fig. 2.8 in which the MSB capacitor (C_2) is switched down and the MSB/2 capacitor (C_1) is switched up simultaneously. The energy in this case drawn from V_{REF} is [7]:

$$E_{1\rightarrow 2,1Step} = \frac{5}{4} C_0 V_{REF}^2 \qquad (2.1)$$

For implementation purpose this method is simple as numbers of switches required are less and the numbers of required clock cycles for the switching are also less.

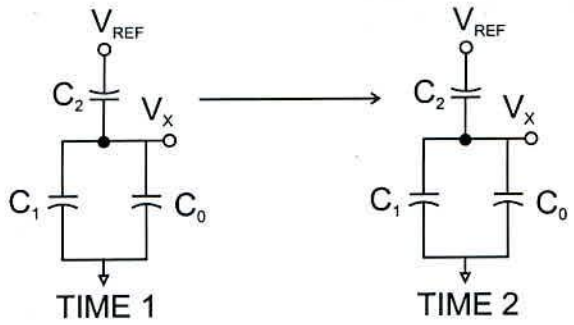


Figure 2.8: 1-step switching method for a "down" transition [7]

In the two step switching method same transition is done in two steps rather than one step. In the 1st first step of switching (time T1 to T1.5), both the capacitors C_1 and C_2 are connected to V_{REF}. In the second step, at time T1.5, the capacitor C_2 (largest) is disconnected from V_{REF} and connected to ground, as shown in Fig. 2.9.

The total switching energy drawn in this case is [7]:

$$E_{1\rightarrow 2,2Step} = \frac{3}{4} C_0 V_{REF}^2 \tag{2.2}$$

Comparing the eq. 2.1 with eq. 2.2 we can see that 40% of the switching energy while down switching can be saved by two step switching method. Qualitatively, some of the stored charge of C_2 is shared with C_1. Two step switching method is shown in Fig. 2.9.

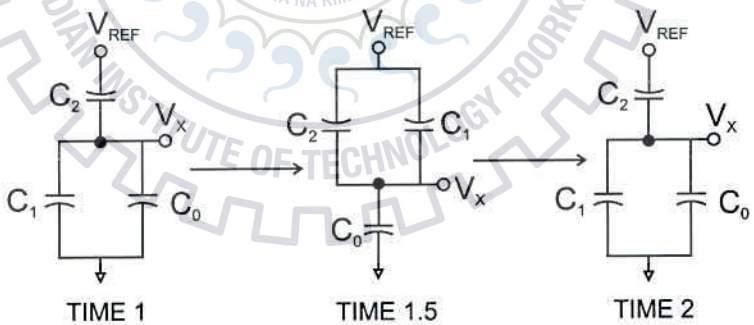


Figure 2.9: 2-step switching method for a "down" transition [7]

2.3.3 Dual Supply Scheme

Operating at lower supply voltage is an effective technique to reduce power consumption due to leakage as well as to reduce the switching power consumption also. At significantly lower data rates as our requirement is, low supply voltage operation is very effective to minimize the static as well as dynamic power consumption. The transistors become slow at lower supply voltage but can still fulfill the speed requirement because of low frequency operation.

The problem with using lower supply voltage is that the effect of noise increases on the analog circuit and their dynamic range is also reduced which can degrade the performance of the ADC severely. To avoid degrading the ADC performance because of lower supply voltage a dual supply scheme is used. The digital circuit is operated at lower supply voltage to reduce the power consumption while supply for the analog voltage is kept higher to maintain the ADC performance in a reasonable limit. Voltage level shifters are used to communicate between the SAR logic and the capacitive array DAC. Voltage level shifters convert the low voltage level digital signal generated by the SAR logic to high voltage level digital signal.

Chapter 3

DESIGN OF ANALOG COMPONENTS

3.1 Capacitive Array DAC Design

To minimize the power consumption and area of a binary weighted capacitive DAC, its unit capacitor should be kept as small as possible. More commonly the size of the unit capacitor is determined by thermal noise or capacitor mismatch.

Generally, the modeling of the unit capacitor is done with a nominal name of C_u and with a standard deviation of σ_u. The worst-case standard deviation of integral nonlinearity error (INL) and differential nonlinearity error (DNL) occurs at the MSB transition for a binary-weighted capacitive array ADC. This happens because of the accumulation of mismatch of the capacitors.

The DNL and INL can be represented in terms of LSB according to the analysis in [8] as following:

$$\sigma_{DNL,MAX} = \sqrt{2^N - 1}\frac{\sigma_u}{C_u}\text{LSB} \tag{3.1}$$

$$\sigma_{INL,MAX} = \sqrt{2^{N-1}}\frac{\sigma_u}{C_u}\text{LSB} \tag{3.2}$$

where N is the resolution of the ADC. Comparing eq. (3.1) with eq. (3.2), the worst case standard deviation of the DNL derived is greater than that of the worst case standard

deviation of the INL. Therefore, eq. (3.1) is taken as a reference to analyze the value of unit capacitor. The standard deviation for a typical metal-insulator-metal (MIM) capacitor is given by:

$$\sigma\left(\frac{\Delta C}{C}\right)=\frac{K_{\sigma}}{\sqrt{A}} \text{ and } C=K_{C}\bullet A \tag{3.3}$$

where $\sigma(\Delta C/C)$ is the capacitor mismatch standard deviation, A is the capacitor implementation area, K_σ is the capacitor matching coefficient, and K_C is the density parameter of the capacitor. The standard deviation of a nominal value single capacitor is smaller than the standard deviation of the difference between two capacitors by a factor $\sqrt{2}$. Thus, $\sigma(\Delta C/C)$ divided by $\sqrt{2}$ is equal to σ_u/C_u. $3\sigma_{DNL,MAX}$ should be greater than 0.5LSB for high yield. Combining the earlier equations, the minimum value obtained for the unit capacitor to avoid mismatch effects is:

$$C_u=18\times 2^{N}-1\times K_{\sigma}\times K \tag{3.4}$$

The density of MIM capacitor is 1.1fF/μm^2 in this technology and has a matching coefficient of 1%. According to the above calculations the minimum unit capacitance is obtained to be 2.2fF. All of the above calculations discussed so far, is for the single-ended capacitive array DAC architecture.

Because of the differential ADC architecture, the unit capacitance can be halved in this design while still fulfilling the requirement for the mismatch. This can be done because the signal range gets doubled by the differential mode but the voltage error introduced because of the mismatch is increased only $\sqrt{2}$ times.

Two more factors are there which are dominant over the mismatch to decide the value of unit capacitance. The first one is leakage through the sampling switch and the next one is the tunnel gate current of the transistor of the comparator to which it is connected. Because of the deep submicron technology both of these effects alter the stored charge on the top plates of the capacitor array. Thus, the unit capacitor is set higher than 2.2fF to minimize the error introduced by them.

Except of that, the design rule itself has limit on the minimum value of the MIM capacitance which can be fabricated. The minimum value of MIM capacitance which can be fabricated by this process is 17.6fF. Accordingly, the value of unit capacitance in our work is

defined to be 8.8fF, which is implemented by the series connection of two minimum MIM capacitors defined by the process limitation. Thus, the total capacitance of each side of the capacitive array DAC is about 9pF.

A partial common centroid layout scheme is used for binary weighted DAC capacitor array implementation. A common-centroid configuration is utilized for the layout of the MSB capacitors (C_9-C_5) to reduce the errors which occurs due to the non-uniform growth of the oxide during fabrication of the MIM capacitors. The other capacitors (C_4-C_0) are placed near the switches connecting the bottom plates of the corresponding capacitors in order to reduce the parasitic capacitances and resistances due to interconnect and to simplify the routing as well. The layout floor plan of one side of the capacitive array is shown in Fig 3.1. The layout of other side of the capacitive array is its mirror image.

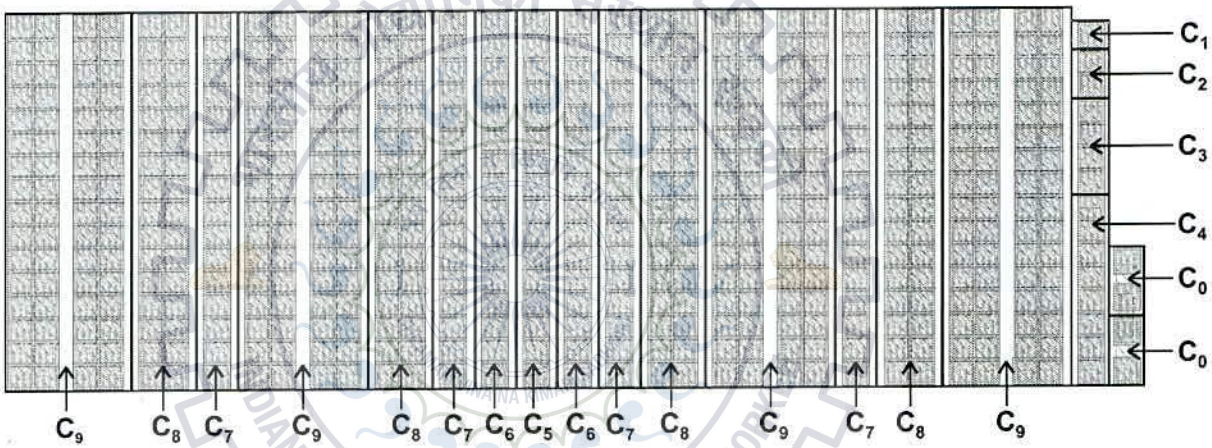


Figure 3.1: Partial centroid layout of capacitor array DAC

3.2 2 Step Switching Implementation

2 step switching scheme is implemented using the delay circuit. The delay circuit associates the delay only to the falling edge of input signal. The circuit is explained further in section 3.3. For D_8 to D_0 switching the delay circuit is inserted between the two latches of the flip-flops used in SAR logic as shown in Fig. 3.2. It increases clock to output delay of the flip-flop for the rising edge only. For MSB flip-flop delay is inserted at the rising edge of the set input as it switches opposite to others in the first clock cycle of each conversion. Since the delay circuit increases transition time, special care has been taken in the succeeding latch design such that the transition time is minimized at the inputs of level shifters.

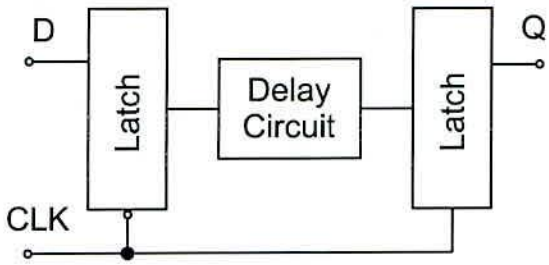


Figure 3.2: D flip-flop using delay circuit

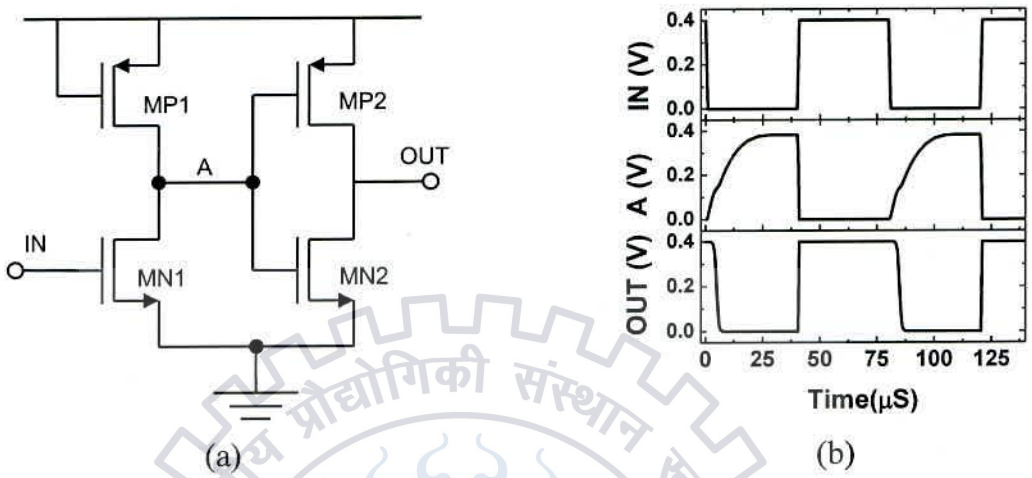
3.3 Delay Circuit

Since the delay required is in order of few μS, it is not practical to be obtained by using the inverter delay [9]. Fig 3.3(a) shows the delay circuit. This circuit introduces the delay only to the falling edge of the input waveform. The input is applied to the NMOS MN1whose drain is connected to the V_{DD} through a source-gate connected PMOS transistor MP1 so that MP1 always remains in OFF condition. MP1 and MN1 are sized in such a way that the OFF state leakage current of MP1 is significantly higher than OFF state leakage current of MN1. Thus, when the input is LOW i.e. both the transistors are in OFF condition, node A remains HIGH. At the falling edge of the input the MN1 turns OFF and MP1 charges 'node A' slowly which causes the delay. At the rising edge of the input MN1 turns ON and 'node A' goes LOW sharply. Thus, the delay is associated to the falling edge of the input only.

For a process, the OFF state leakage current of a PMOS transistor is an order of magnitude lower than that of NMOS. Therefore, MP1 is implemented by using a low threshold transistor utilizing its high OFF state leakage current feature in order to avoid the need of an extra wide transistor. The delay is associated by MP1 to rising edge of node A but not at the falling edge. When the input is low both the transistors MP1 and MN1 are in OFF state thus their drain to source resistance are high. Since, both these resistances act as a voltage divider network. Even though drain to source resistance of MP1 (OFF state) is designed to be much smaller than drain to source resistance of MN1 (OFF state) but still they are comparable to each other. As a result 'node A' remains at few millivolts (20 mV approx.) lower to V_{DD}. Thus, the succeeding stage should be designed in such a way that the leakage current due to lower voltage at 'node A', can be minimized. An inverter is used to minimize this sub-threshold leakage current. It also maintains the rise and fall time of the pulse in reasonable limit. Fig. 3.3(b) shows the simulated waveform of the delay circuit.

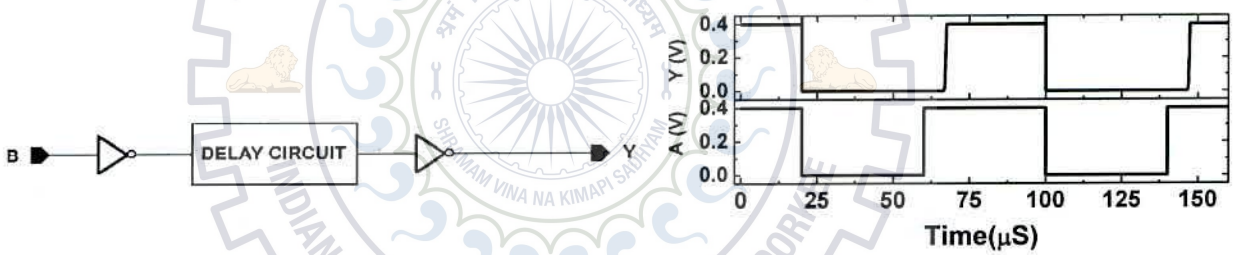
Since, the sub-threshold current of a PMOS transistor is an order of magnitude lower than that of a NMOS transistor for a given technology, same circuit is used to associate a

delay in rising edge of a signal with the help of inverter. If a complementary delay circuit with a source gate connected NMOS transistor is used to associate a delay in rising edge of a pulse, the sub-threshold leakage current of the NMOS of succeeding inverter will cause comparatively much higher power consumption. Fig. 3.4(a) and 3.4(b) shows the rising edge delay circuit and its simulated waveform, respectively.



(a) (b)

Figure 3.3: (a) Delay circuit (b) Simulated waveform.



(a) (b)

Figure 3.4: (a) Rising edge delay circuit (b) Simulated waveform.

3.4 Comparator Design

The top plates of capacitive array DAC are connected to the comparator for comparison. Since, there is a finite tunneling gate current of MOS transistors for each technology, the charge stored on the top plates of the capacitors is consumed by the comparator. At such a low sampling rate of 1kS/s the total charge consumed per conversion cycle is significant. As the technology length of the MOS decreases the thickness of gate oxide also gets reduced resulting in higher tunnel gate current. Because of the increasing gate current with decreasing channel length, stored charge consumed by the gate current of the comparator significantly alters the DAC top plate voltage level, degrading the ADC performance.

The gate current of NMOS is an order of magnitude higher to that of PMOS for a given CMOS technology. Thus, the comparator design is chosen in such a way that the transistors to which the top plates of capacitive array DAC are to be connected, should be PMOS transistors. Even though gate current of PMOS is much less than that of NMOS, it is much higher at lower technology length to deteriorate the ADC performance. Fig. 3.5(b) shows the gate current of PMOS for two different configurations, 1) drain and source of PM1 is tied together and its source voltage is varied from 0V to 1V keeping gate at 0V and 2) gate drain of PM2 is connected to ground and its source is varied from 0V to 1V. Fig. 3.5(a) shows the circuit used for gate current evaluation. The graph shows the gate current of PM1 is almost double to that of PM2 even though the V_{DS} of PM1 is zero. This shows that the gate current is not due to hot carrier effect. The gate current of PM1 is approximately double to that of PM2 because both the drain and source of PM1 are at high potential while only the source of PM2 is at high potential.

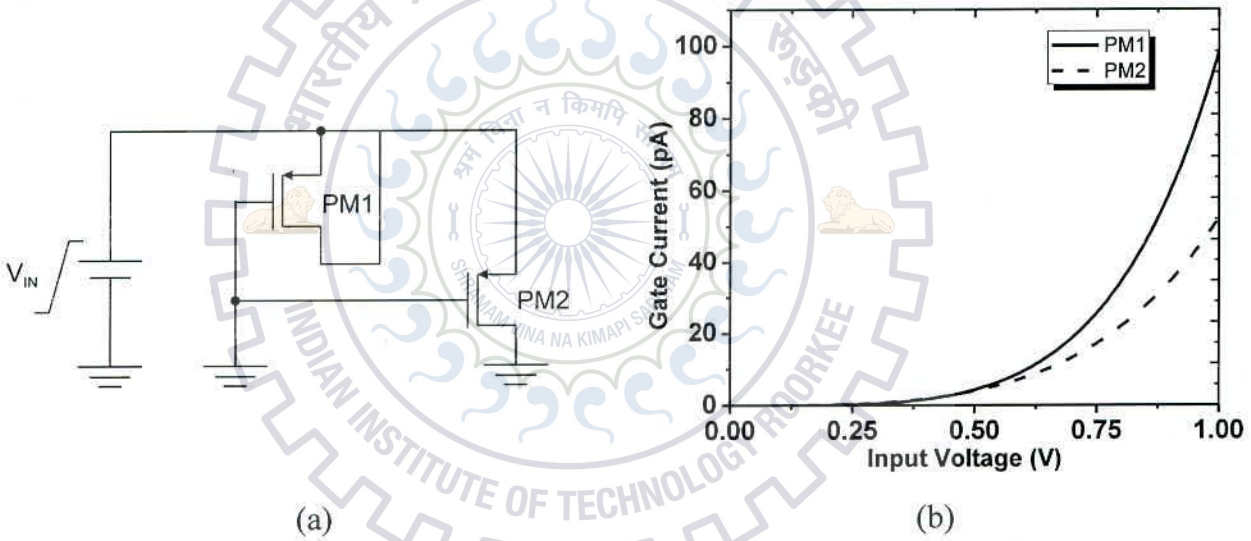
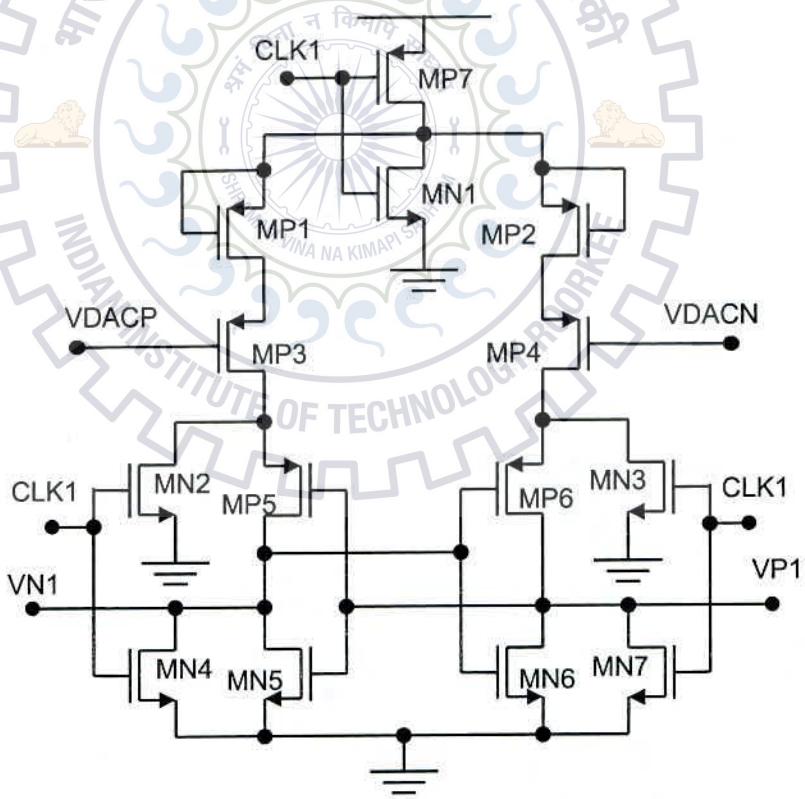


Figure 3.5: (a) Gate current circuit (b) Gate current for 90nm technology with $(W/L)_{min}$

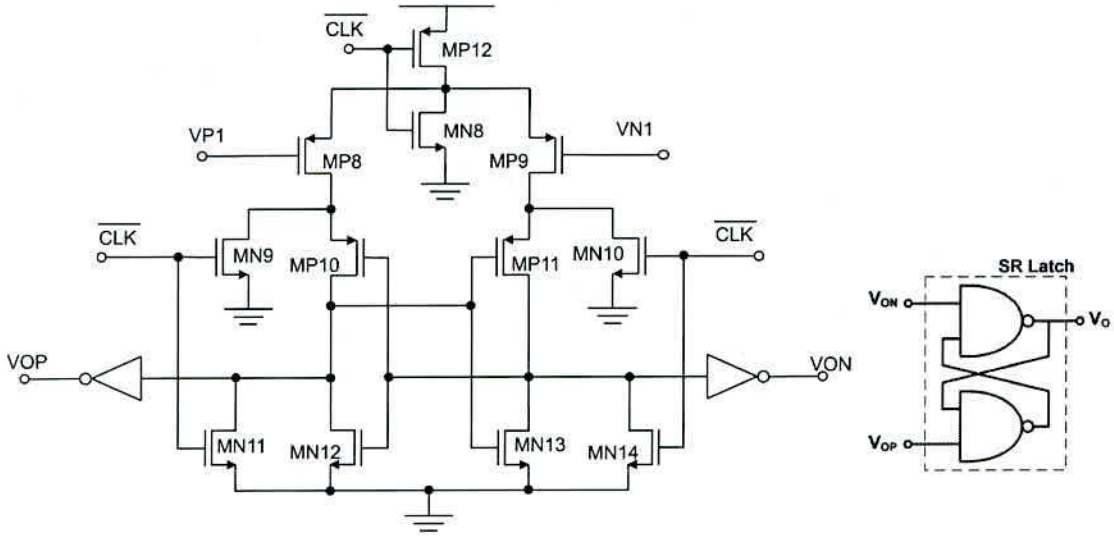
As we see from graph of Fig. 3.5 (b) the gate current of PM2 is about 50pA. For a sampling frequency of 1kS/s the hold time of the DAC is about 833µs. The comparator is in comparison mode for only half of the clock cycle. Thus, the total charge consumed in one conversion cycle is about 21fC ($Q = I \times T$). Since, the total capacitance of each side of the DAC is about 9.1pF, the total voltage change on each side is about 2.3mV ($V = Q/C$). For a 10-bit differential ADC with input range 0-1V the resolution is 1.95mV. Thus, the error introduced is not acceptable.

From graph of Fig. 3.5 (b) we got the conclusion that both the drain and source terminal of the PMOS should be kept at lower potential to reduce the gate current. One way to do that is to reduce the power supply (V_{DDH}) but it will degrade the ADC performance in other design aspects. Furthermore, the current through those PMOS is limited by a series connection of a PMOS operating in sub-threshold region.

Two stage dynamic latch comparator is shown in Fig. 3.6. The first stage of the comparator is inherently designed to minimize the effect of the gate current. The dynamic latch comparator proposed by [10] is modified with MP1 and MP2 connected in OFF state to minimize the current through MP3 and MP4 respectively, thus minimizing the effect of gate current. Because of extremely low driving current of 1st stage output VP1 and VP2 does not achieve rail to rail voltages and are sensitive to loading effect. 2nd stage of comparator is used to obtain rail to rail output without having a loading effect on the 1st stage. The output of the second stage is followed by a SR latch to make the output available for full clock cycle.



(a)



(b) (c)

Figure 3.6: Dynamic latch comparator (a) 1st stage, (b) 2nd stage and (c) SR latch

Fig. 3.7 shows the simulated waveform for comparator. CLK1 and $\overline{CLK}$ both are low for approximately 10μS. Consequently, both comparator stages are in the evaluation phase for this 10μS. A delay element is used to provide delay in the rising edge of CLK1 which is explained further in section 2.3.

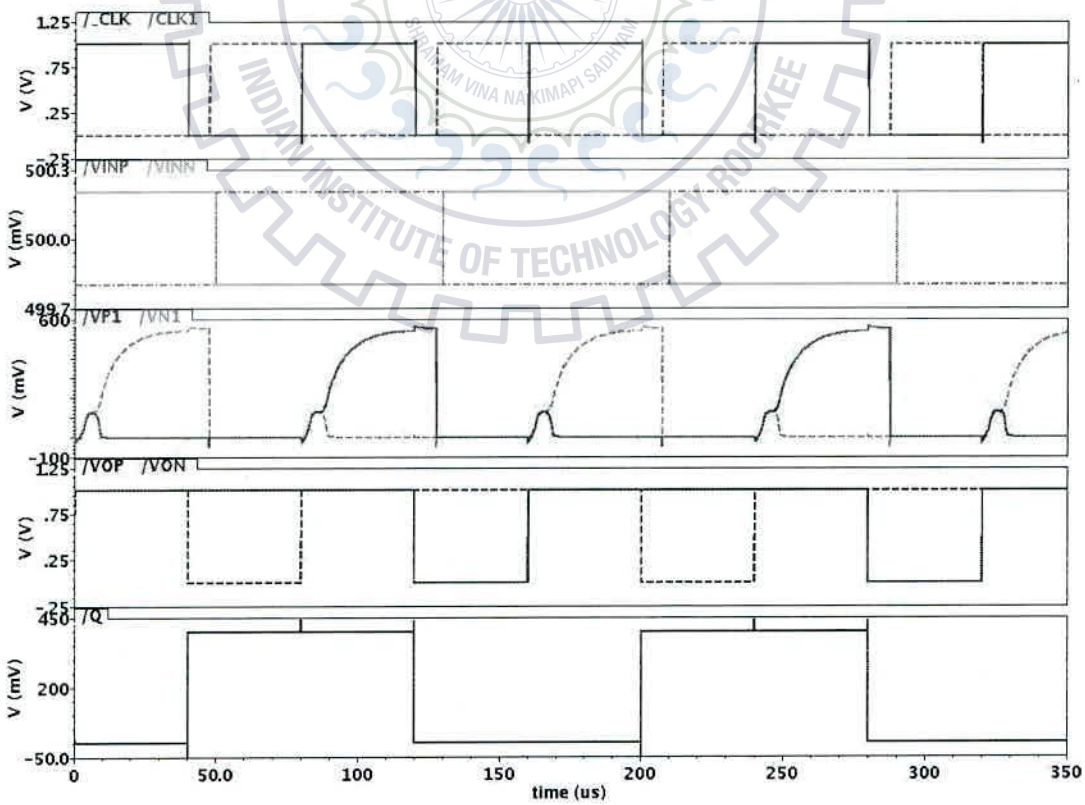


Figure 3.7: Simulated waveform of 2-stage comparator.

3.5 Sample Switch Design

Sampling switch connected to the top plates of the capacitor array is implemented through a transmission gate, to achieve full range sampling of the input. The DAC capacitor array along with a sampling switch performs the sample and hold operation of the ADC. For the sampling switch design of an N-bit SAR ADC the settling error of the voltage sampled on the top plates of capacitor array should be less than half of LSB. For an N-bit ADC, the settling error of the sampled voltage should be less than LSB/2. The required criterion for this is [11]:

$$f_{3dB} > \frac{(N+1)\bullet \ln 2}{\pi} f_s \tag{3.5}$$

where f_S is the sampling frequency. The sampling frequency for this design is determined by the clock frequency. The clock frequency for this circuit is N +2 times higher than the sampling rate. Thus, eq. (3.5) can be written as:

$$f_{3dB} > \frac{(N+2)\bullet(N+1)\bullet \ln 2}{\pi} f_s \tag{3.6}$$

Based on the eq. (3.6), the minimum required switch resistance is about 30 kHz for a 1-kS/s SAR ADC with 10-bit resolution. Since, the total capacitance of single side of capacitor array DAC is about 9.1pF, the on-resistance of the sampling switch should be less than 583 kΩ so that the settling error remains less than half of LSB.

Apart from settling error, the leakage current of the sampling switch is also one of the major issues because of high leakage current at deep-submicron technology level. Since, the sampling rate of the ADC is very low i.e. 1kS/s the error voltage introduced by the sampling switch leakage current can degrade the performance of the ADC severely. Due to deep-submicron technology design the OFF resistance of the transistor is comparatively very low. Thus, OFF state leakage current of the transistor is dominant. Also, the leakage current has a non-linearly dependent over the voltage drop across the sampling switch. Because of this non-linear dependency the leakage current introduces harmonic distortion. One common solution to bring down the sub-threshold leakage is to increase the channel length of the transistor. Another effective way of leakage current reduction is to use stacked-transistor [12] (shown in Fig. 3.8).

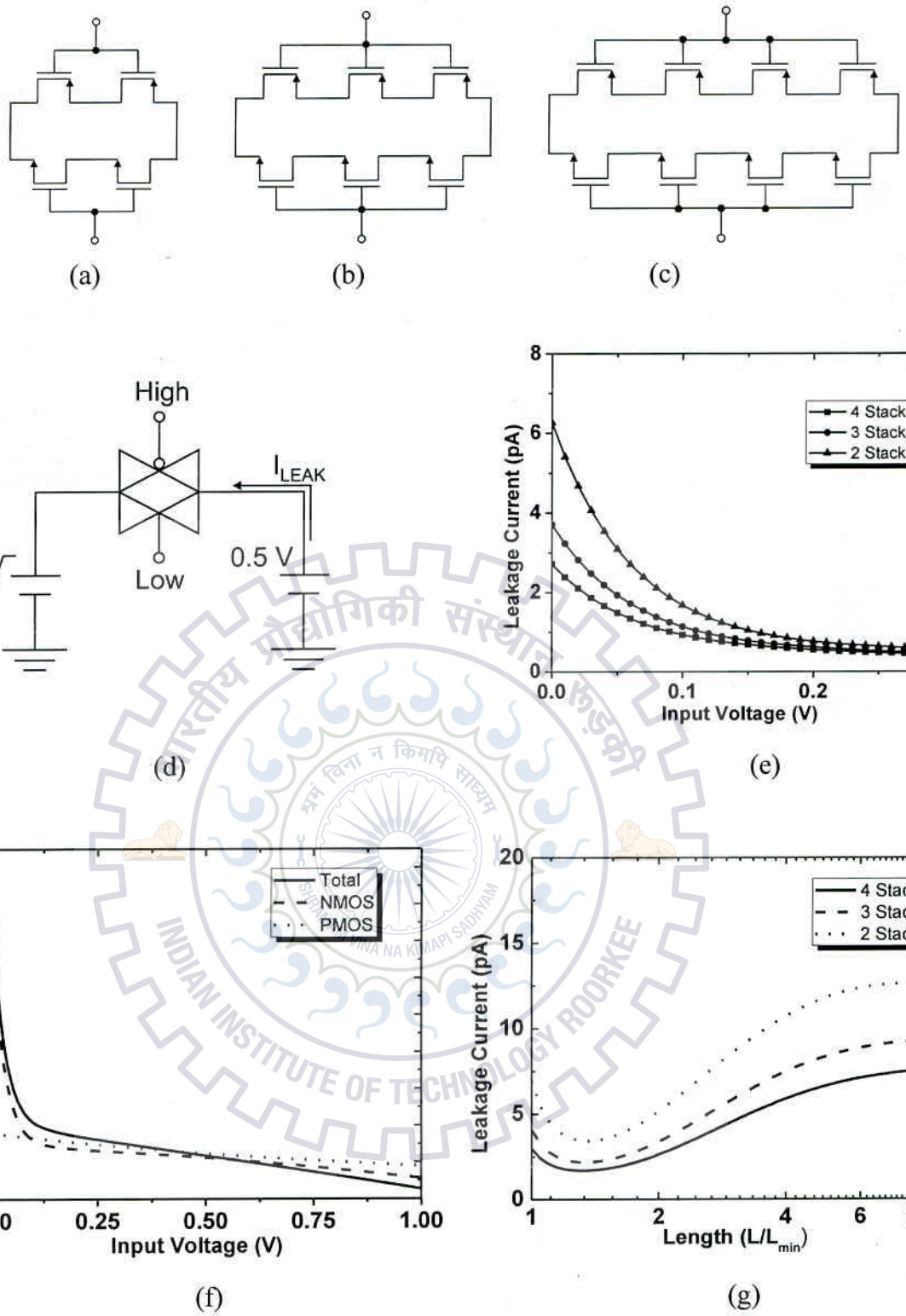


Figure 3.8 (a) 2-transistor stack, (b) 3-transistor stack, (c) 4-transistor stack, (d) Leakage circuit, (e) Leakage current vs. input voltage for 2, 3 and 4-transistor stack with equivalent length of 600nm, (f) Leakage current contribution of NMOS & PMOS vs. input voltage for 2-transistor stack with equivalent length of 600nm (300nm each), (g) Leakage current vs. channel length for VIN =0. All graphs are for 90nm technology (GPDK090 process) with W=120nm

Fig. 3.8 (e) shows the leakage current of 2, 3 and 4 transistor stacked transmission gate (shown in Fig. 3.8 (a), 3.8 (b) and 3.8 (c) respectively) switches with respect to input voltage. The circuit used to plot the leakage current is shown in Fig. 3.8 (d). It can be observed that the leakage current as the number of stacked transistor in the switch increases. The reduction in the leakage current with the increasing number of stacked transistors decreases exponentially.

Fig. 3.8 (f) shows the contribution of NMOS and PMOS leakage current in the total leakage current with respect to input voltage variation of two transistor stack. It can be observed from the graph that the leakage current contribution of NMOS is much higher than that of PMOS. It also can be observed that the leakage current due to the NMOS increases significantly when the input voltage reaches near 0V.

Fig. 8.3 (g) shows the leakage current of 2, 3 and 4 transistor stacked transmission gate with respect to channel length. The length of each transistor in the stack was varied from L_{min} to $10L_{min}$. It can be observed from the graph that the leakage current is minimum, when the channel length is about $1.2L_{min}$ to $1.3L_{min}$. This happens due to the combined effect of short channel effect (SCE) and reverse short channel effect (RSCE) [13].

Keeping the above facts in mind sampling switch is implemented through a transmission gate having 4-transistor stack of NMOS and 2-transistor stack of PMOS. Fig. 3.9 shows the sampling switch circuit diagram. The charge injected on the top plates of the capacitor array through the PMOS and NMOS of the sampling switch is of opposite polarity. Thus, the net charge injected is comparatively smaller. The introduced error voltage is significantly small because charge introduced by the sampling switch is shared by the entire capacitor array.

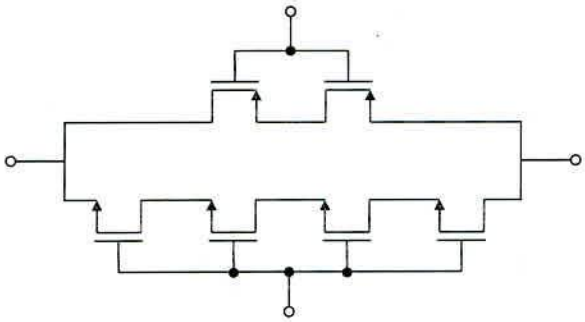


Figure 3.9: Sampling switch

3.6 Level Shifter

A level shifter is required to control the DAC and the sampling switch by the SAR logic. The contention mitigated level shifter [14] shown in Fig. 3.10 is used. Its complementary outputs can be directly used to control the bottom-plates of the both the capacitor arrays. Thirteen level shifters; ten for DAC control signals, two for the two clocks of two stage dynamic latch comparator, and one for the sampling switch, are used in the entire design.

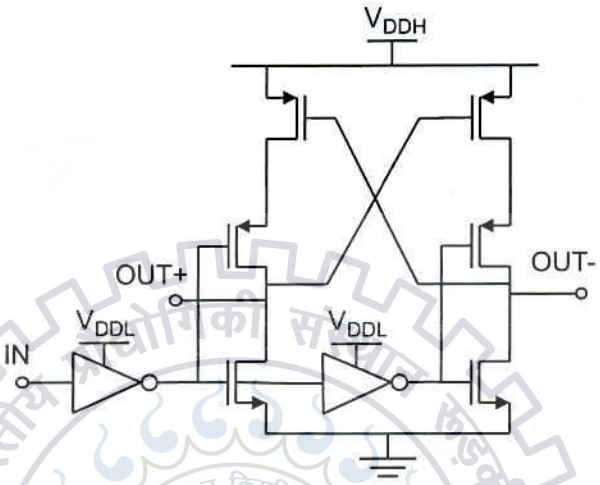


Figure 3.10: Level Shifter [14]

Chapter 4

DESIGN OF DIGITAL COMPONENTS

4.1 SAR Logic Design

SAR Logic generates control signals for DAC and sampling switches. Fig. 4.1 shows the block diagram for SAR logic. The working mechanism of 10-bit shift resister is similar to that of [15].

A 4-bit counter followed by 4 to 2 decoder (output for 0 and 11 only) is used to generate 1 KHz internal clock for sample signal and counter reset signal. The generated sample signal itself is used as set and reset signals for the shift register. Synchronous counter is used instead of asynchronous, in order to avoid glitch in the sample signal to preserve the performance of the ADC. 14 transmission-gate flip-flops are used for entire SAR control logic.

Several power reduction techniques have been utilized: 1) optimized channel length considering the effect of SCE and RSCE; 2) use minimum transistor width; 3) stacked pair transistors wherever required mostly for NMOS; 4) lower supply voltage for SAR logic operation. Because of low drive current, drive strength of gates are poor. Input signal transition times were evaluated carefully at each gate input to avoid unwanted increase in short-circuit current.

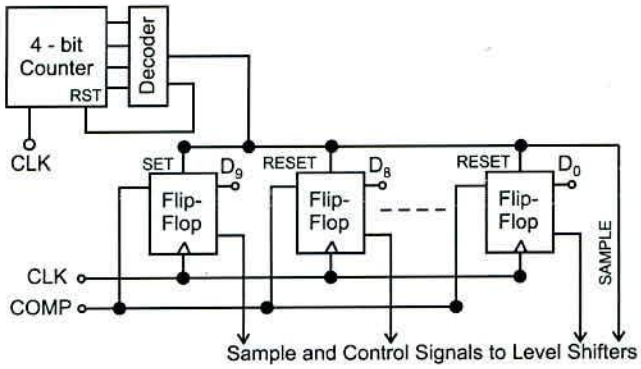


Figure 4.1: SAR Logic Block Diagram

4.1.1 SAR Operation

The SAR assumes that keeping the other bits LOW, the MSB is set to HIGH for the initialization step. The digital word stored in the 10-bit shift register is applied to the capacitor array DAC, which generates the corresponding analog output which is FS/2 (where FS is full-scale sampling range of the analog input). The DAC output is then compared to the input voltage V_{IN}. If V_{IN} is greater than the DAC output then the comparator output obtained is HIGH. SAR keeps the MSB HIGH if the output of the comparator is HIGH. If the output of the comparator is low, the SAR logic sets the MSB to low. The value of MSB is known at this stage. The digital word is once more applied to the DAC with MSB having its previously known value and the next bit to MSB (MSB–1) is set to high keeping all the other remaining bits low. Again, the comparison is made with the sampled input and the output of the DAC is applied to the SAR logic. If the comparator output is high, the next bit to the MSB (MSB–1) is proven to be high otherwise low. The successive approximation step is applied to the other remaining bits also until the value of LSB is determined. The finite state machine (FSM) sequence for a 10-bit SAR logic is shown in table 4.1.

Table 4.1: FSM sequence, N = 10

Step	Input D/A Word										Comp o/p
	1	0	0	0	0	0	0	0	0	0	a9
	a9	1	0	0	0	0	0	0	0	0	a8
0	a9	a8	1	0	0	0	0	0	0	0	a7
1	a9	a8	a7	1	0	0	0	0	0	0	a6
2	a9	a8	a7	a6	1	0	0	0	0	0	a5
3	a9	a8	a7	a6	a5	1	0	0	0	0	a4
4	a9	a8	a7	a6	a5	a4	1	0	0	0	a3
5	a9	a8	a7	a6	a5	a4	a3	1	0	0	a2
6	a9	a8	a7	a6	a5	a4	a3	a2	1	0	a1
7	a9	a8	a7	a6	a5	a4	a3	a2	a1	1	a0
Result	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0	-

4.1.2 SAR Circuit

The SAR logic is basically a 10-bit shift register as shown in Fig. 4.1. To initialize the conversion cycle the 'MSB' flip-flop is set to high and all the other flip-flops are reset to low. This state is called the initialization state. A mechanism is needed for initialization which can bring the 10-bit shift register in the initialization state. The mechanism used here to initialize the flip-flops is that the flip-flops are used with set and reset inputs and a control signal (start) is connected. If the control signal is high it sets the MSB flip-flop and resets all the other flip-flops. For the next states, a generic flip-flop (k^{th} flip-flop) should have a mechanism to choose between three data inputs which are coming from:

- The output of the (k^{th}) flip-flop itself (memorization)

- The output of the comparator (a) (data load).

- The output of the $(k+1)^{th}$ FF (shift right).

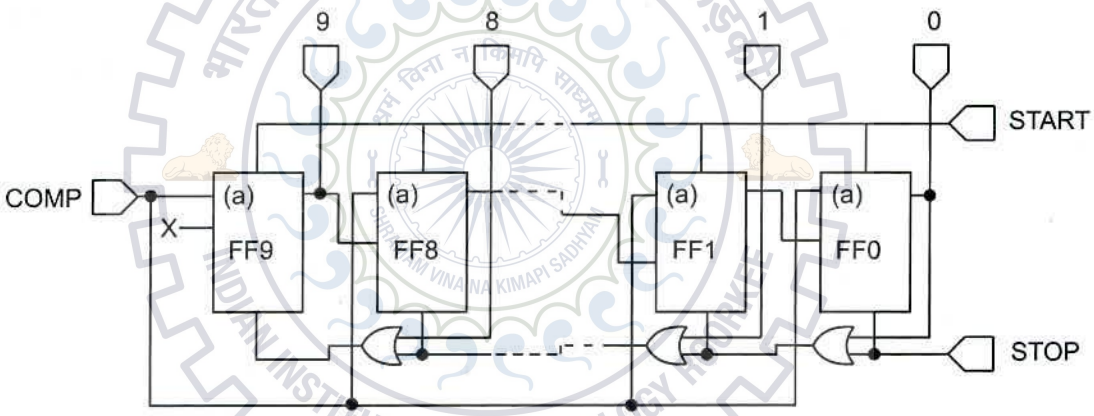


Figure 4.2: 10 bit multiple input SAR

A multiplexer is used to select the desired input from these three inputs. This multiplexer is added to each flip-flop as shown in Fig. 4.2. According to the k^{th} flip-flop algorithm a chain of OR gates is used which is connected to the output of all the less significant bits than the k^{th} (k-1, k-2. ,.., 0) to reveal the zero states for all the corresponding less significant bits. The multiplexer needs two selector inputs in order to select the correct input for the k^{th} flip-flop. The first input is the output of the OR gate (from chain of OR gates) connected to the preceding flip-flop (A). The second input is the output of the k^{th} flip-flop itself (B) as mentioned in Table 4.2. Fig. 4.3 shows the k^{th} flip-flop symbol and its internal structure.

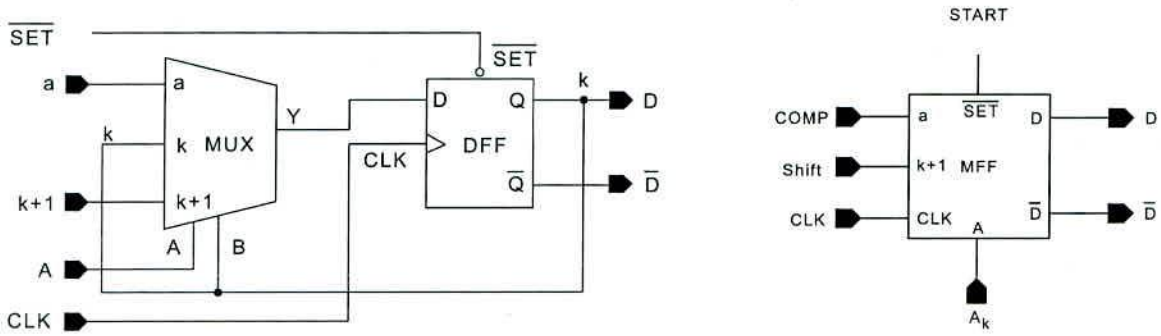


Figure 4.3: k^{th} FF symbol and k^{th} FF internal structure

At the end of the conversion cycle a control signal (stop) can be applied to the chain of OR gates at the LSB flip-flop OR gate to stop the conversion. When the control signal (stop) is active it forces the output of all the OR gates in the chain to high due to which all the 10-bit shift register goes to memorization mode.

Table 4.2 FF outputs

A	B	Operation
1	-	memorization*(k)*
0	1	data load *(a)*
0	0	shift right *(k+1)*

The delayed clock generated for comparator stage 1 (CLK1) shown in Fig. 3.7 is used for SAR logic operation so that comparator output is stabilized and available for SAR Logic. Fig. 4.4 shows the SAR logic clock waveform compared to the clock applied to the two stages of the comparator. The output of comparator is available to the SAR logic when the clock of stage 2 of the comparator (CLK_STAGE2) goes LOW i.e. prior to the rising edge of SAR logic clock (SAR_CLK). Thus, the two stage operation of the comparator does not need any extra clock cycle.

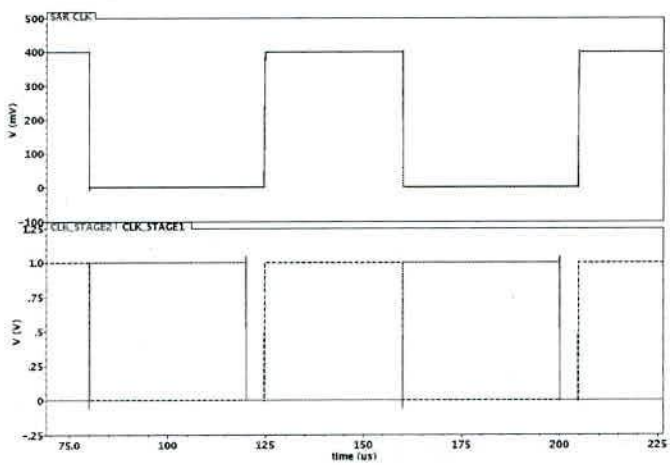


Figure 4.4: SAR clock timing diagram

4.2 4-bit Counter Design

To design 4-bit counter we looked up for both synchronous and asynchronous designs. Generally asynchronous designs are used for high frequency ADCs in order to avoid the high frequency clock signal running throughout the system. An asynchronous counter can be useful in this design in terms of low power consumption and less hardware requirement.

Fig. 4.5 (a) shows a 4-bit asynchronous counter using T flip-flop. Since, T flip-flop can be easily implemented using transmission gates and inverters only, thus the power consumption is very low. For our design the power consumption of a 4-bit counter using T flip-flop obtained through simulation at 90nm technology length is about 155pW. The main drawback of using asynchronous T flip-flop counter in our design is the glitches produced in the output. Since, the output of the counter is used to control the top plates sampling switches of the capacitor array DAC; these glitches can degrade the ADC performance severely.

A synchronous counter design eliminates the problem of glitches. A conventional synchronous counter is made up by using JK flip-flops. Fig. 4.5 (b) shows a 4-bit synchronous counter design using JK flip-flop. In comparison to T flip-flops it is hard to implement JK flip-flop using transmission gates. Using static gates for JK flip-flop design increases the power consumption. According to simulation results the 4-bit counter using JK flip-flop shows a power consumption of about 750pW.

Fig. 4.5 (c) shows a 4-bit synchronous counter design using T flip-flop. The T flip-flop used in this design needs an extra enable signal. Because of low power operation static gates should be avoided to introduce this enable input. The low power T flip-flops designs are available with reset and enable input but using domino circuits. Because of low frequency operation domino circuits cannot be used in our design. Thus, the enable signal should be incorporated in the T flip-flop by using transmission gates only. Fig. 4.6 (b) shows T flip-flop design with enable and asynchronous reset input using transmission gates and inverters only. According to simulation results the 4-bit counter using this T flip-flop shows a power consumption of about 235pW. Thus, this is the best counter design suitable for our application.

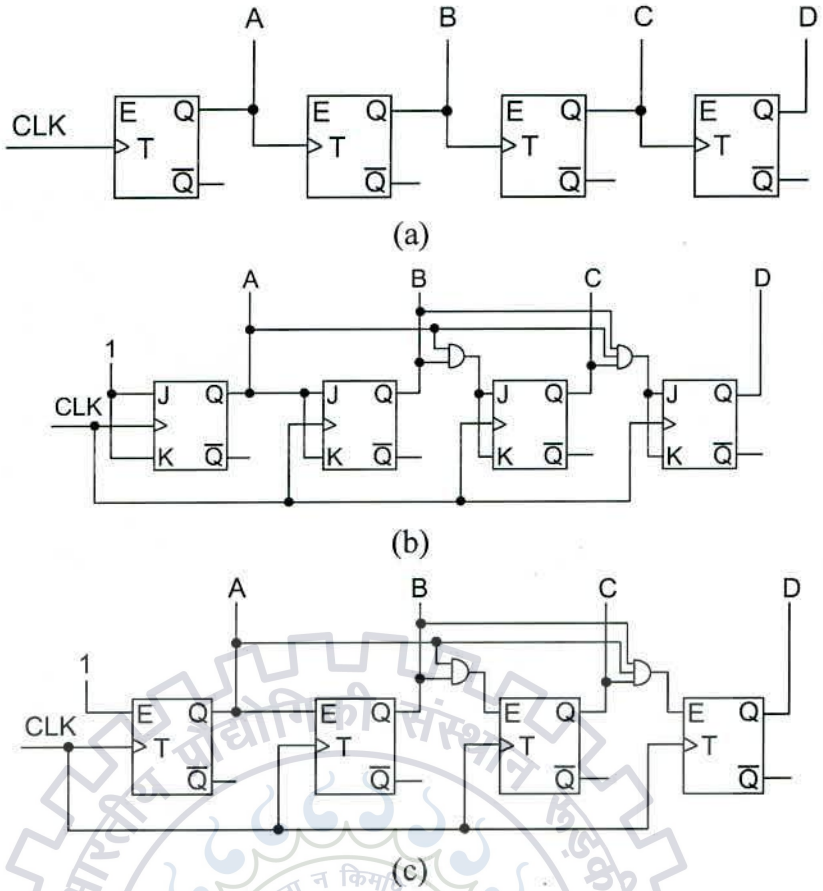


Figure 4.5: 4-bit counter (a) using T flip-flop (asynchronous), (b) using JK flip-flop (synchronous) and (c) using T flip-flop with enable input (synchronous)

4.3 T Flip-Flop Design

The T flip-flop used in 4-bit synchronous counter is shown in Fig. 4.6 (b). This is a master-slave positive edge triggered T flip-flop and incorporates enable signal and asynchronous reset input. 12 transmission gates and 4 inverters are used in the design. The basic design is taken is of master-slave positive edge triggered transmission gate D flip-flop [16] shown in Fig. 4.6 (a).

The output $\overline{Q}$ of the D flip-flop is fed to D input of the flip-flop to get T flip-flop operation. To incorporate asynchronous reset operation both the latches (latch 1 and latch 2 shown in Fig. 4.6 (a)) are broken at 'node 1' and 'node 2' and two transmission gates are inserted at both the nodes (TRST1 and TRST2 at 'node 1' and TRST3 and TRST4 at 'node 2'). The two transmission gates TRST3 and TRST4 are inserted at 'node 2' keep the output Q LOW when reset is HIGH and TRST1 and TRST2 are inserted keep the output of latch 1 HIGH simultaneously. TRST1 and TRST2 are used to ensure that when reset goes LOW the output Q goes HIGH only at the next rising edge of clock.

To incorporate the 'enable input' the output Q and $\overline{Q}$ of the D flip-flop are fit to its D input through 2-to-1 transmission gate multiplexer. The enable input is used as the selector signal for the 2-to-1 multiplexer. A transmission gate TEN1 is added to latch 2 so that it latches its own value even if the clock is HIGH if the enable input is LOW. The transmission gate TEN2 is added to detach the output of latch 1 from the input of latch 2 when the enable input is LOW to hold the toggle operation.

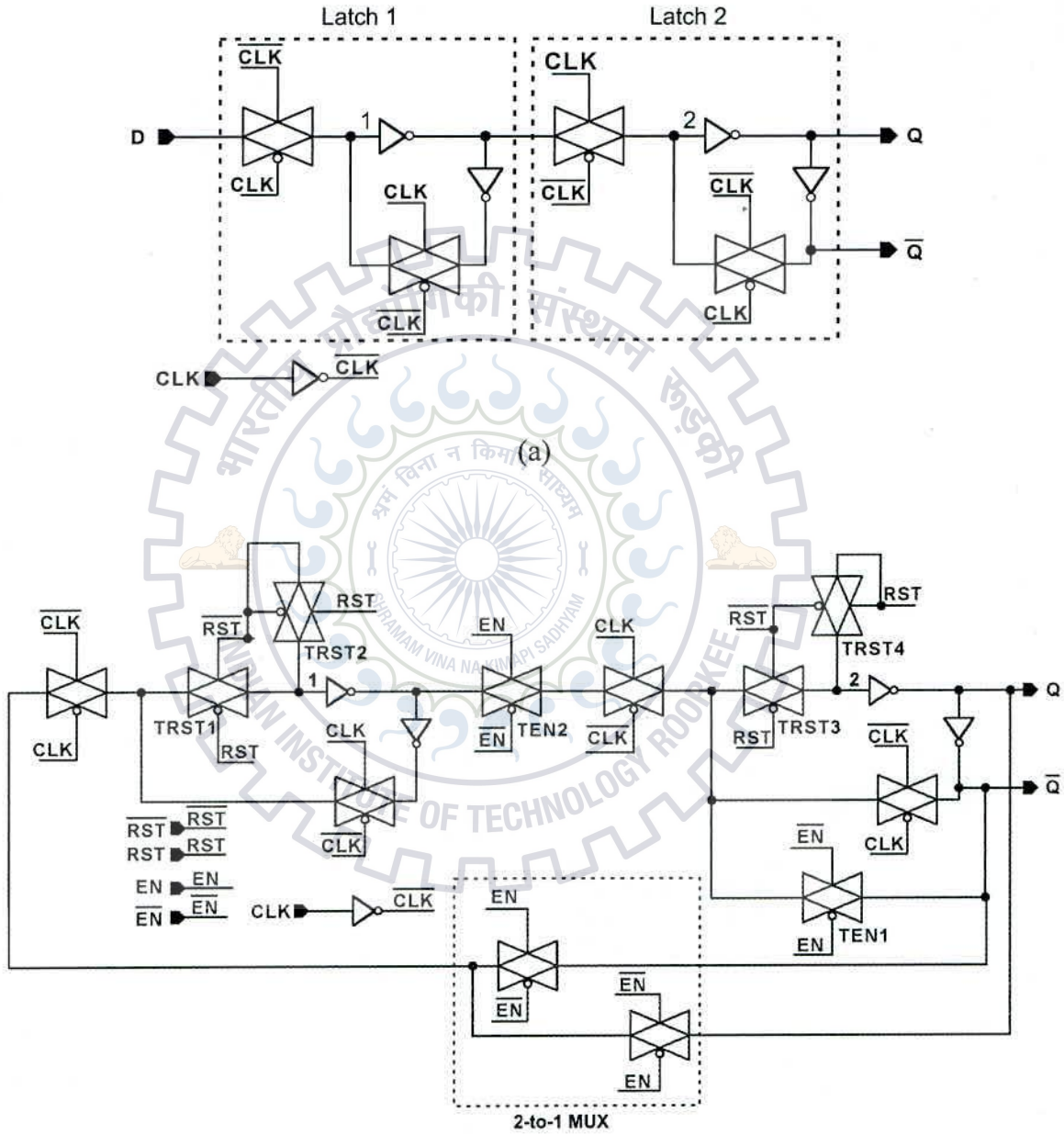


Figure 4.6: (a) Basic Tx-gate D flip-flop (b) Tx-gate T flip-flop with enable and asynchronous reset

4.4 Decoder Design

Decoder is used to generate the sample signal for top plate sampling switches of the capacitor array DAC, reset signal for 10 bit shift register and stop signal to reset the counter. Fig. 4.7 shows the decoder circuit. It consists of only three NOR gates for the three output signals. Fig. 4.8 shows the simulated waveform of the decoder when the output of 4-bit counter applied to its input and the stop signal of the decoder applied to the reset input of the comparator. I3 is the MSB input and I0 is LSB.

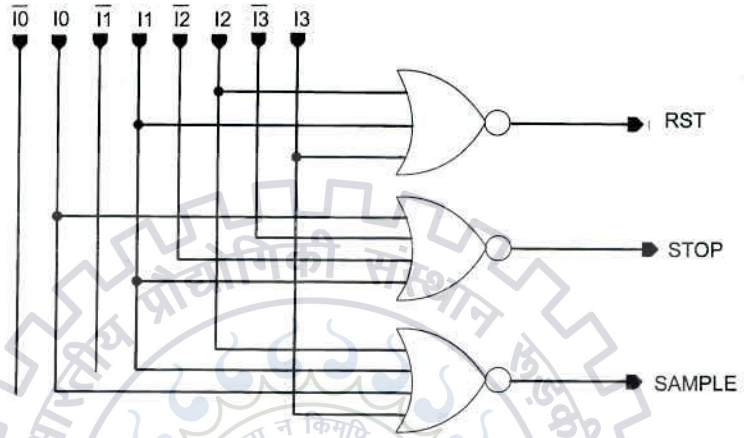


Figure 4.7: Decoder circuit diagram

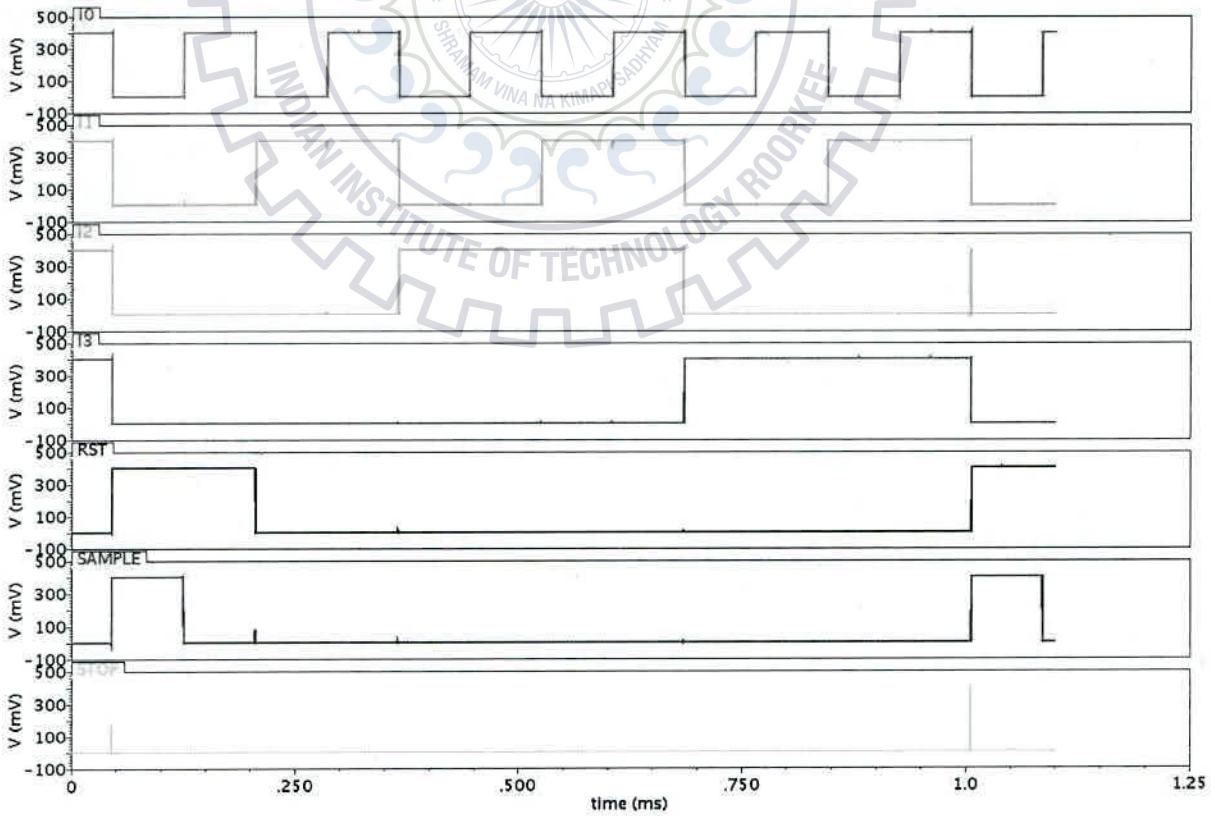


Figure 4.8: Decoder output waveform with input applied through 4-bit counter

4.5 Multiplexer Design

Multiplexer is used in the SAR logic to put the D flip-flops of the 10-bit shift register in three modes of operation; memorization, data load and shift right according to the different states of the ADC as explained in section 4.1. The multiplexer is implemented by the use of transmission gates only and uses only five transmission gates. Fig. 4.9 shows the multiplexer circuit according to the truth table given in table 4.2. The k input of the multiplexer itself is used as the second selector input (B).

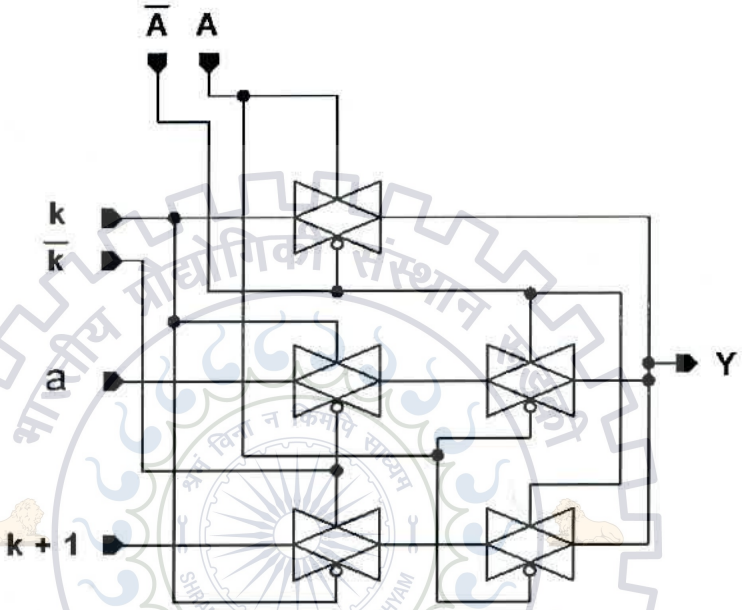


Figure 4.9: Multiplexer circuit diagram

4.6 D Flip-Flop Design

Depending upon the different operations of the D flip-flop required in the 10-bit shift register of the SAR logic three different types of circuits are used to implement the 10-bit shift register. The flip-flop for bit D_9 requires only set input while flip-flops for bit D_8 to D_0 require reset input only.

4.6.1 D Flip-Flop for D_9

Fig. 4.10 shows the circuit diagram of the D flip-flop used for bit D_9. Since, D_9 is set HIGH in the beginning of the ADC conversion cycle, no delay circuit is required for this D flip-flop for implementation of 2-step capacitor switching. The basic design of the transmission gate D flip-flop is taken from Fig. 4.6 (a). Two extra transmission gates are added to the second latch incorporate the set input operation. The operation is similar to that of reset input operation

discussed in section 4.3. Since, the time period of the set input applied to the D flip-flop is always greater than one clock time period and also the input to the D flip-flop remains HIGH when the set input is HIGH no transmission gates are required to be added to the first latch to keep its output LOW as in case of T flip-flop discussed in section 4.3. So the synchronous behavior of the D flip-flop is maintained throughout the operation of SAR logic.

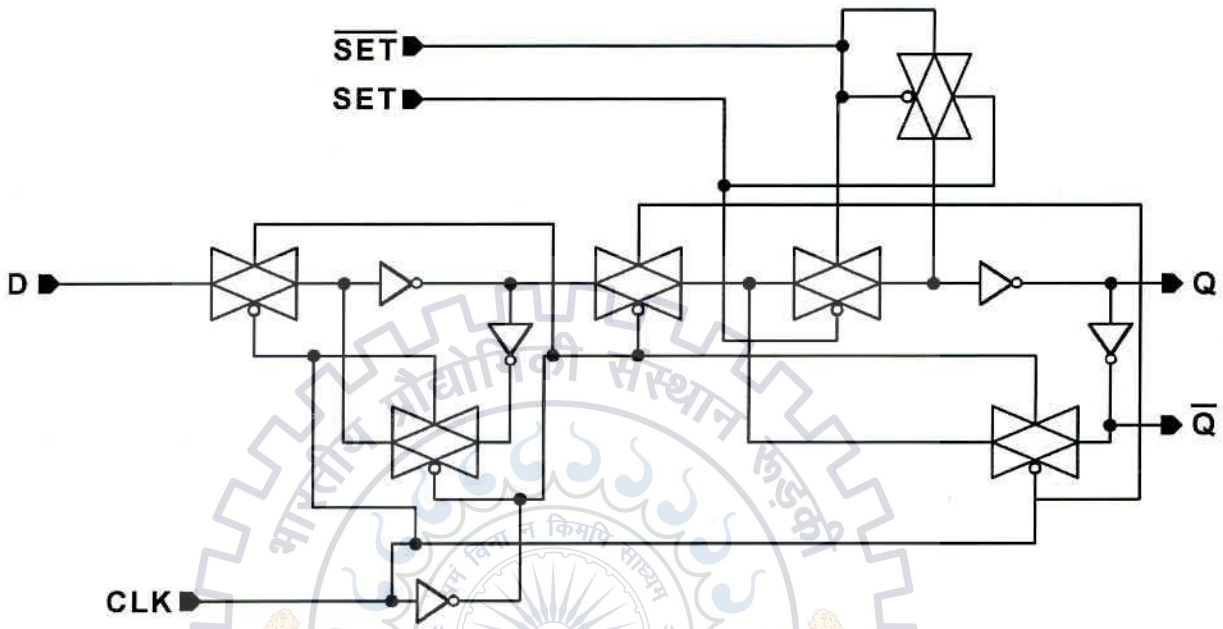


Figure 4.10: D flip-flop circuit diagram for D_9

4.6.2 D Flip-Flop for D_8

According to the SAR logic operation, if the decision for bit D_9 is taken LOW by the comparator D_9 goes LOW and bit D_8 goes HIGH simultaneously for the next bit comparison. Since, both the capacitors corresponding to bit D_8 and D_9 are switch in opposite direction thus a delay should be provided in the rising edge of output of D flip-flop corresponding to bit D_8 in order to implement 2-step capacitor switching. There are two ways to add this delay to the rising edge of output of D flip-flop. First one is that the delay circuit is inserted in the path of D to Q but then two extra transmission gates are required to be added in the first latch similar to TRST1 and TRST2 shown in Fig. 4.6 (b) in order for proper reset operation. The second way is that the delay circuit is added in the reset path in such a way that it delays the falling edge of reset signal. Since, the output of D_9 is applied at the input of D flip-flop of bit D_8 at this time (shift-right operation), the input D of D flip-flop is HIGH at this time. Thus, the output Q of D flip-flop goes HIGH as we remove the reset. So, a delay is provided to the

falling edge of the reset signal to introduce a delay in rising edge of output Q. Fig. 4.11 shows the circuit diagram of the D flip-flop used for bit D_8 which uses the second method to implement the 2-step switching.

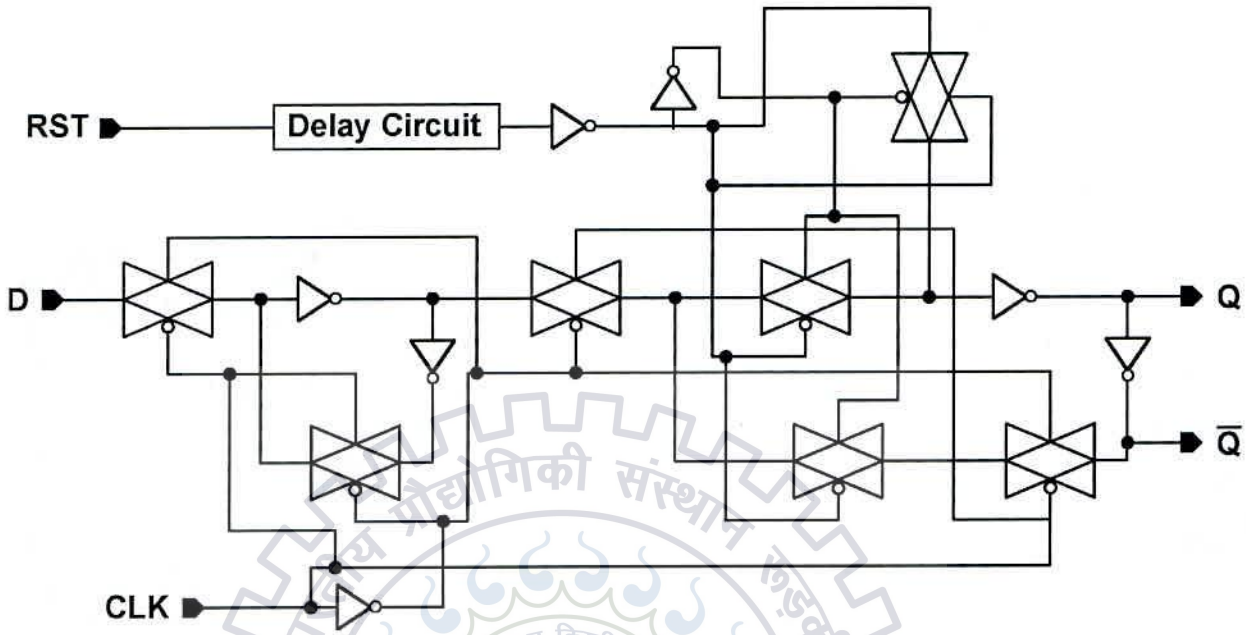


Figure 4.11: D flip-flop circuit diagram for D_8

4.6.3 D Flip-Flop for D_7 to D_0

As per the SAR logic operation the reset input applied to the D flip-flops corresponding to bit D_7 to D_0 has time period more than a clock cycle and also the input applied to the D input of all the flip-flops is LOW (shift-right mode operation). Thus, no transmission gates are required to be inserted in the first latch of the flip-flop for proper reset operation. Fig. 4.12 shows the circuit diagram of the D flip-flop used for bit D_7 to. The Delay circuit is inserted in D to Q path of the second latch to provide delay in the rising of output Q in order to implement 2-step capacitor switching. Since, the delay circuit increases the transition time of the output and the output of D flip-flop is directly applied to the input of level shifters, it increases the power consumption. If the transition time of the input of the level shifters is high, the short-circuit current of the level shifter due to V_{DDH} supply causes large power consumption. Thus, an extra inverter is added at the output to reduce the transition time of output Q.

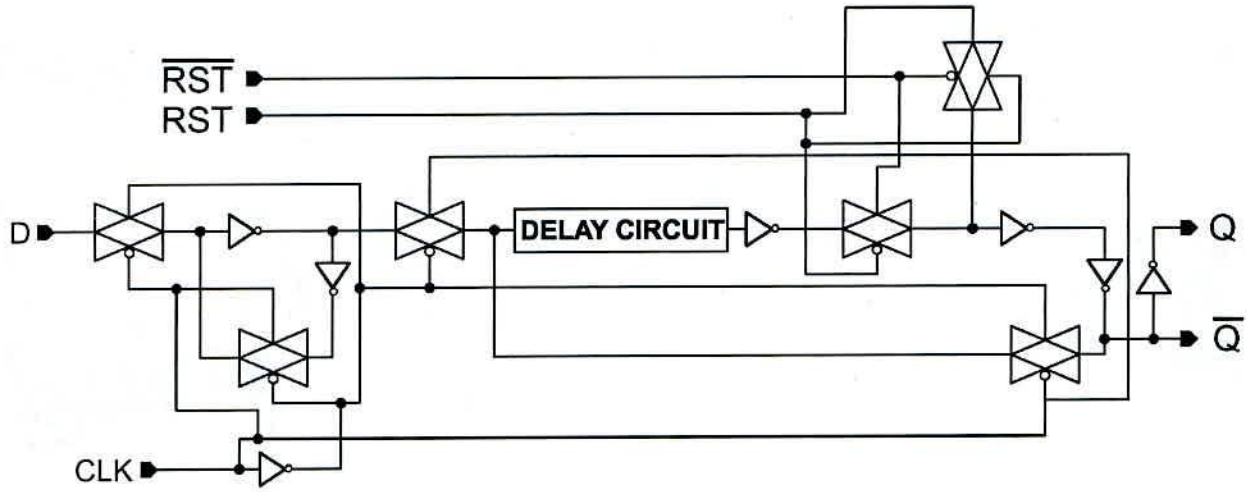


Figure 4.12: D flip-flop circuit diagram for D_7 to D_0

Chapter 5

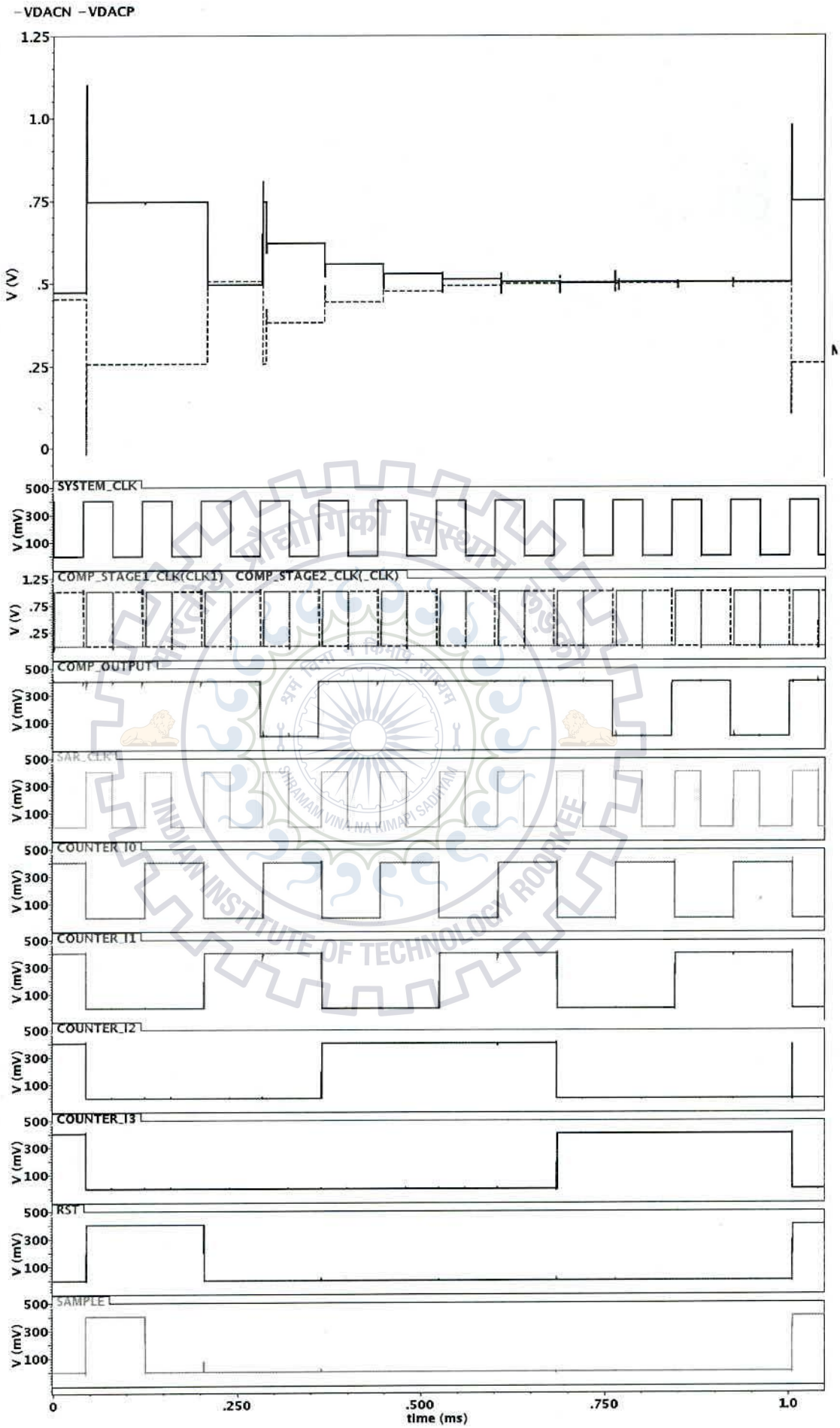
SIMULATION RESULTS

The complete ADC is implemented in the GPDK 90nm CMOS process. The layout and parasitics extraction is done with CADENCE Virtuoso Layout XL. The simulation is done in CADENCE Virtuoso Front to Back Design Environment.

5.1 ADC Waveform

The complete ADC waveform is shown in Fig. 5.1 with constant DC input applied to the sampling switches. V_{INP} and V_{INN} were set to be 0.745V and 0.255V respectively. The digital output code which should be obtained for this input voltage is "1011111010". The output code obtained is same as that to be obtained ideally.

It can be seen from the switching graph of bit D_8 and D_7 that there is a difference of few μs between D8 going LOW and D_7 going HIGH which shows that 2-step switching is implemented. The same switching pattern can also be seen at the switching time of D_2 and D_1. It also shows the clock applied to the two stages of the comparator (COMP_STAGE1_CLK and COMP_STAGE2_CLK). It can be seen form the wave form that the output of two stage comparator is available prior to the clock applied to the SAR logic (SAR_CLK).


-VDACN -VDACP
1.25
1.0
.75
.5
.25
0
V (V)
SYSTEM_CLK
500
300
100
V (mV)
COMP_STAGE1_CLK(CLK1) COMP_STAGE2_CLK(_CLK)
1.25
.75
.25
V (V)
COMP_OUTPUT
SAR_CLK
COUNTER_I0
COUNTER_I1
COUNTER_I2
COUNTER_I3
RST
SAMPLE
0
.250
.500
.750
1.0
time (ms)

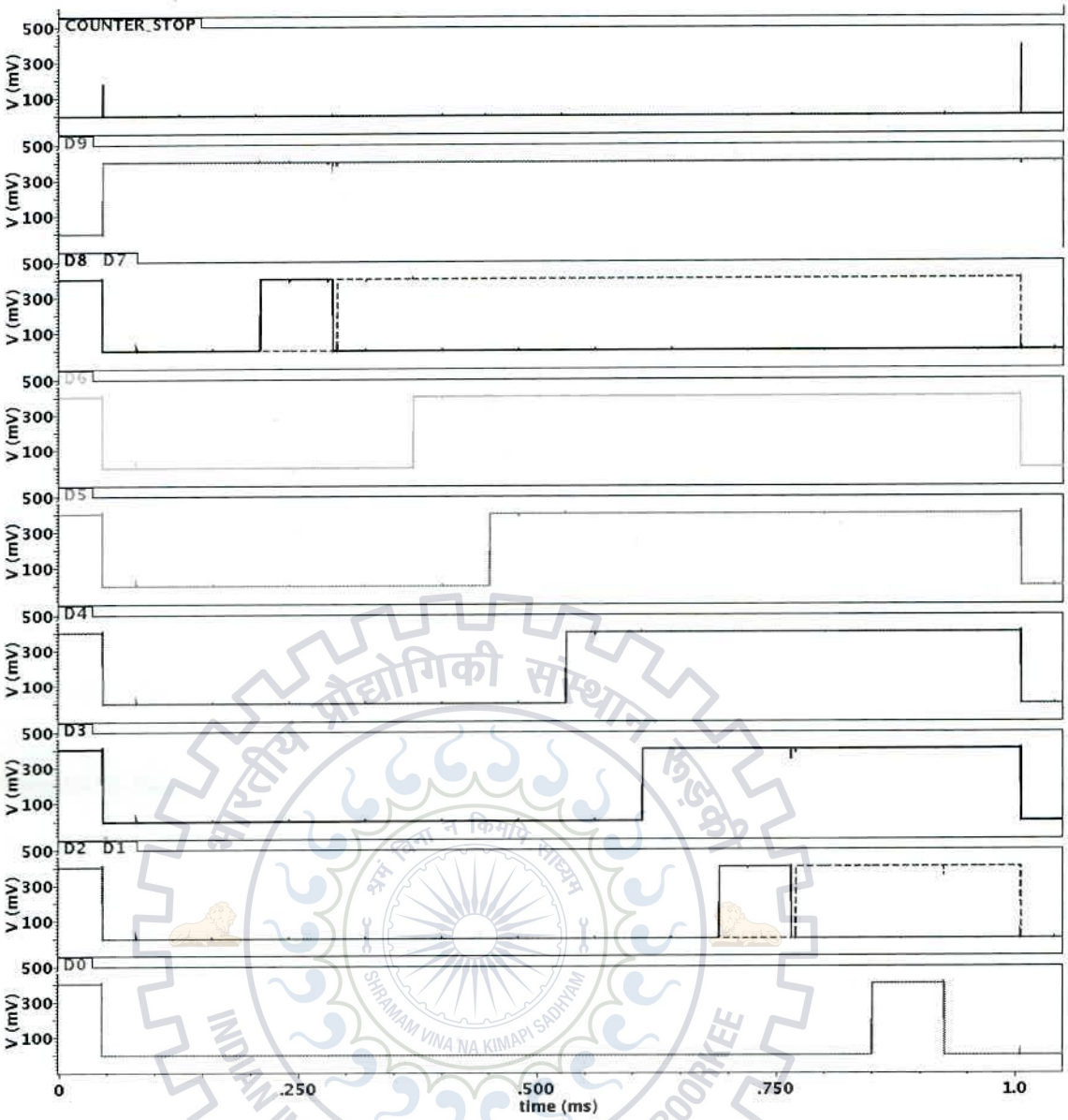
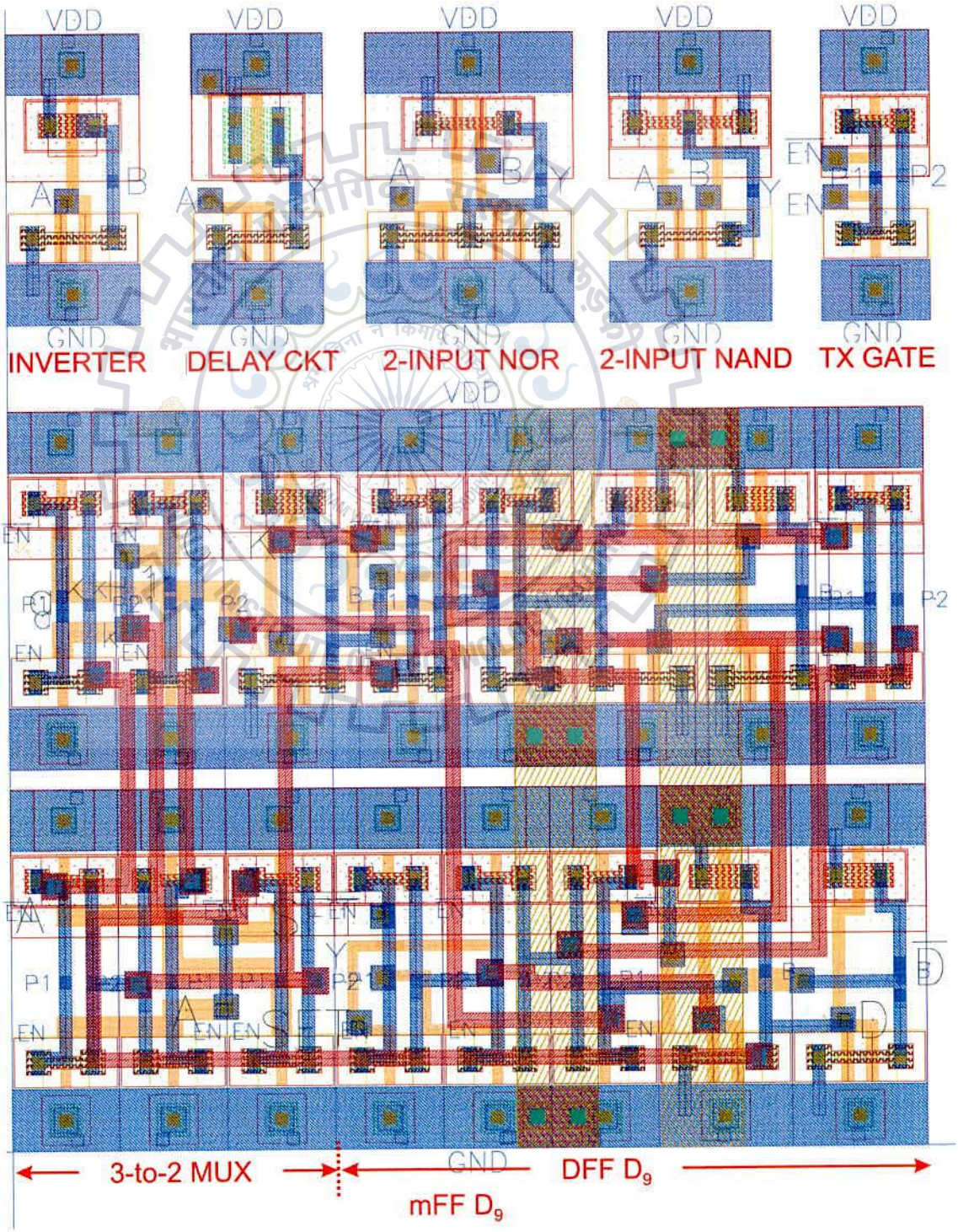


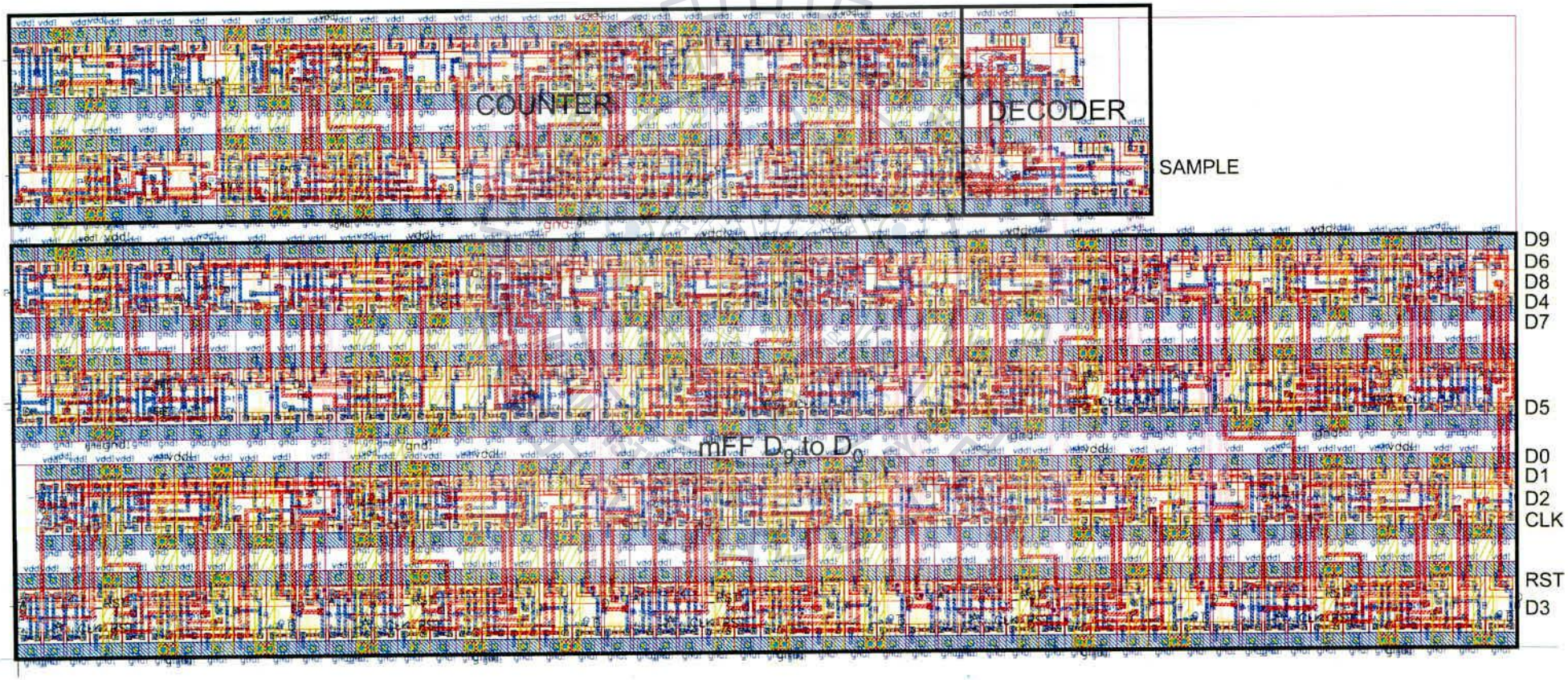
Figure 5.1: 10-bit SAR ADC Simulated Waveform

5.2 ADC Layout

Fig. 5.2 shows the layout of different sections of the implemented SAR ADC. The implementation area is about 222 × 140μm^2. The capacitor array acquires most of the chip area as expected. The total implementation area of capacitor array DAC is about 193 × 140μm^2 which is about 87 % of total implementation area of the ADC. The SAR logic is implemented in about 60 × 25μm^2.


Via1 drawing
Pimp drawing
PWdummy drawing
Nhvt drawing
Cont drawing
Oxide drawing
Phvt drawing
Via2 drawing
Via3 drawing
Via4 drawing
Via5 drawing
Metal3 drawing
Metal4 drawing
Metal5 drawing
Metal6 drawing
prBoundary drawing
text drawing
Metal2 drawing
Nimp drawing
Nwell drawing
Poly drawing
Metal1 drawing


VDD
GND
INVERTER
DELAY CKT
2-INPUT NOR
2-INPUT NAND
TX GATE
3-to-2 MUX
DFF D_9
mFF D_9


COUNTER
DECODER
SAMPLE
mFF D_9 to D_0
D9
D6
D8
D4
D7
D5
D0
D1
D2
CLK
RST
D3

SAR LOGIC

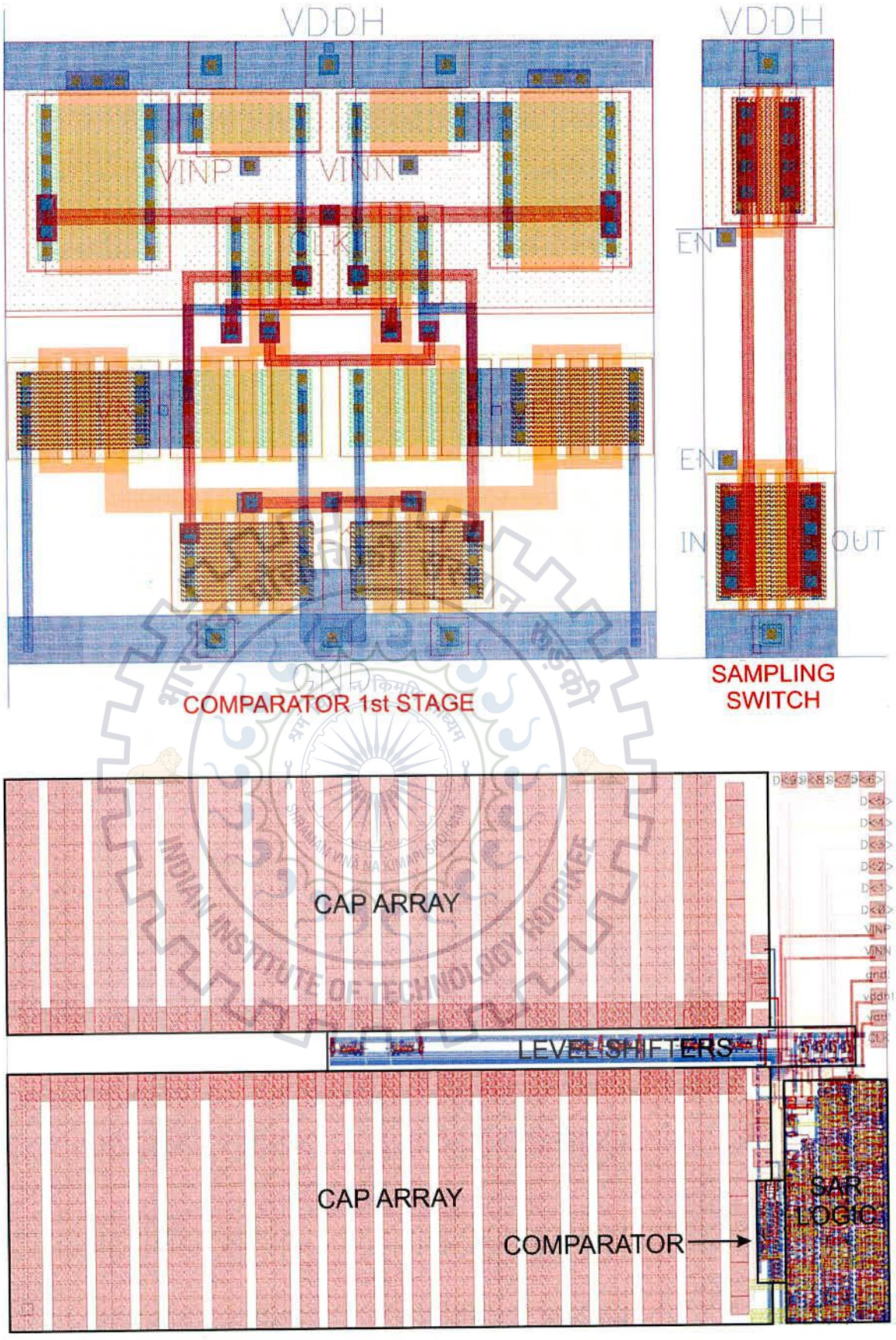


Figure 5.2: ADC Layout

5.3 Static Characteristics

Fig. 5.3 and Fig. 5.4 show the simulated differential nonlinearity (DNL) and the integral nonlinearity (INL) errors, respectively. DNL and INL are less than +0.44/-0.5LSB and +0.38/-0.44LSB, respectively with 10-bit resolution at a supply voltage of 1V. The figure shows that transition of the MSB capacitor results in major error.

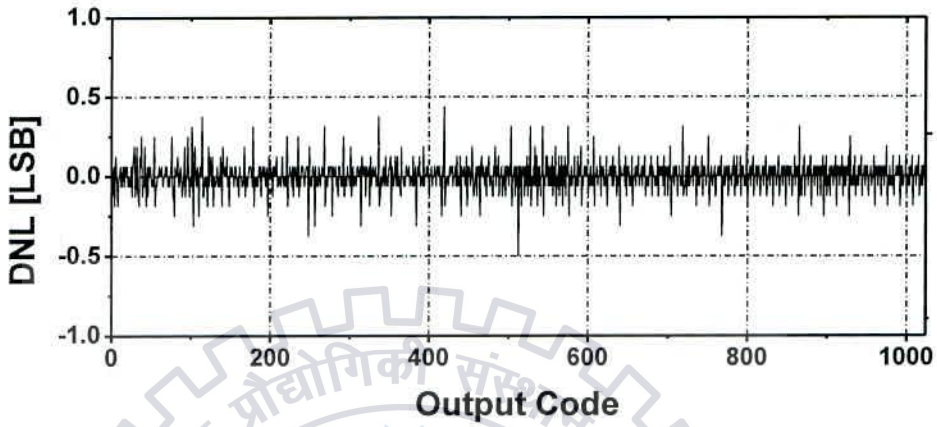


Figure 5.3: Simulated DNL for 10-bit SAR ADC

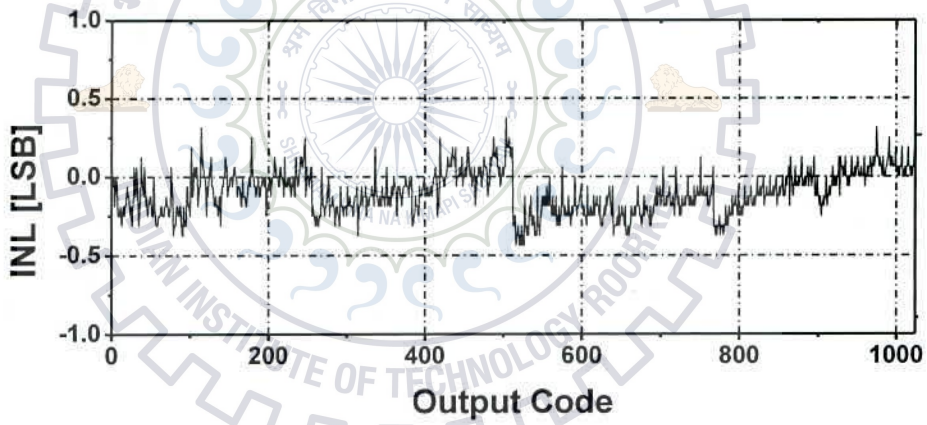


Figure 5.4: Simulated INL for 10-bit SAR ADC

5.4 Dynamic Characteristics

Fig. 5.5 shows the simulated FFT spectrum with rail to rail input with near Nyquist frequency, at a sampling rate of 1kS/s. The SNDR is 57.3dB, providing an ENOB of 9.2 bits. Fig. 5.6 shows the ENOB of the ADC with respect to the input frequency.

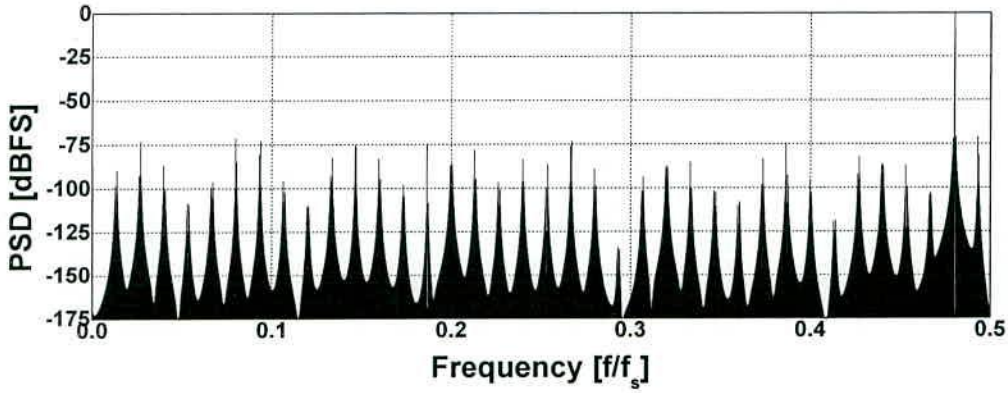


Figure 5.5: FFT plot of 10-bit SAR ADC output near Nyquist

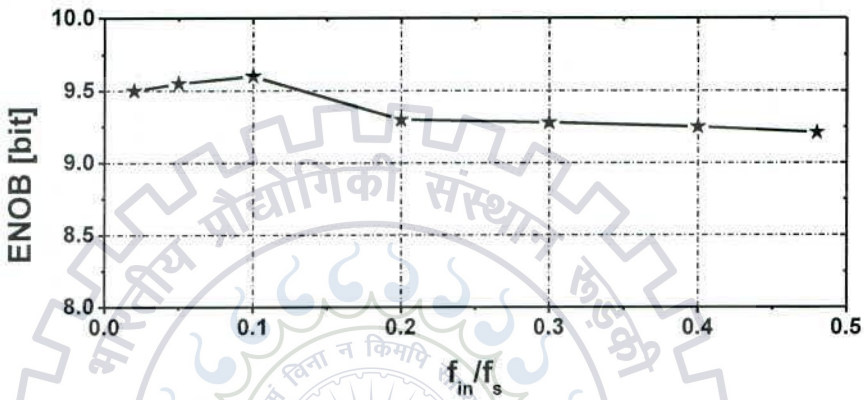


Figure 5.6: ENOB vs. input frequency of 10-bit SAR ADC

5.5 Power Consumption

The total power consumption of the SAR ADC obtained through the simulation is about 24nW. Table 5.1 shows the power consumption of different sections of the SAR ADC. The capacitor array DAC consumes 17nW which is about 71% of the total power.

Table 5.1 ADC Power Breakdown

DAC	17nW
Comparator	1.2nW
Level Shifter	4.5nW
SAR Logic	1.3nW

5.6 Summary of ADC Performance

The simulated ADC performance including extracted parasitics of 10-bit ADC is summarized in Table 5.2. The figure-of-merit (FOM) which is used for ADC performance comparison is defined as:

FOM = Power/(2ENOB@Nyquist *fs)

Table 5.1, shows the power breakdown of ADC in different blocks. Table 5.2 shows the AD performance summary. Table 5.3, shows the comparison of previously published SAR ADCs of 1 kS/s sampling rate to simulated results of this work. The comparison shows, lowest power and FOM are achieved by this ADC.

Table 5.2 ADC Performance Summary

Sampling Rate	1kS/s
Chip Area	0.03mm2
SAR logic supply voltage	0.4V
DAC and Comparator supply voltage	1V
Input Range	1V
INL	+0.38/-0.44 LSB
DNL	+0.44/-0.5 LSB
SFDR (near Nyquist)	70 dB
SNDR (near Nyquist)	57.3 dB
Total Power	24nW

Table 5.3 ADC Comparison

Author/ Year	Zou 2009 [17]	Zhang 2012 [4]	This Work
Technology [nm]	350	130	90
Sample Rate [kS/s]	1	1	1
Power [nW]	230	53	24
ENOB [bit]	10.2	9.12	9.2
FOM [fJ/Conv.]	195	94.5	40.8

Chapter 6

CONCLUSION

A 10-bit 1KS/s SAR ADC is designed for ultra-low power consumption which makes it well suited for bio-medical implantable applications (e.g. implantable heart rate sensors). A full range sampling scheme without extra reset voltage and switch bootstrapping is utilized. SAR logic is operated at reduced supply voltage of 400mV to reduce the power consumption. A delay based control logic is used to implement 2 step switching to minimize the DAC switching power without extra switches. A two stage comparator is designed to minimize the effect of gate current at deep submicron technology level. The ADC delivers 9.2 ENOB near Nyquist frequency at a sampling rate of 1kS/s with a power consumption of 24nW.

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