INVESTIGATIONS ON ENHANCED-BOOST Z-SOURCE INVERTERS

Ph.D. THESIS

by

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in this thesis entitled "**INVESTIGATIONS ON ENHANCED-BOOST Z-SOURCE INVERTERS"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electrical Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from July, 2013 to February, 2018 under the supervision of Dr. Sharmili Das, Assistant Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(**VADTHYA JAGAN**)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

(Sharmili Das)
Supervisor

Date: _____

ABSTRACT

Increased demand of energy throughout the world, shortage of fossil fuels, and environmental problems caused by conventional power generation has led to an urgent search for renewable energy sources (RES) and harvest maximum energy from them. Renewable energy is energy that comes from natural resources such as sunlight, wind, tides, and geothermal heat, which are naturally replenished at a constant rate. These comprise of wind, biomass, geothermal, thermoelectric generation (TEG), solar photovoltaic (SPV), tidal, and wave energy systems. Renewable energy sources are clean, inexhaustible, and are thought to be “free” energy sources, such as solar and wind energies.

Among all these renewable energy sources, the photovoltaic energy is being widely utilized because of the ubiquity, abundance and sustainability of solar radiant energy. These photovoltaic cells or solar cells directly use the energy from the sun to generate electricity. But, the photovoltaic cell or module produces the peak (or maximum) power at a particular terminal voltage of the cell or module. Thus in order to extract this peak power from the module, a power conditioning circuit (also termed as power electronic interface) is needed. In addition, this power electronic interface is also need to feed extracted power from photovoltaic module to the grid or to the load at a required voltage level. To achieve this, generally traditional single-stage voltage source inverters (VSIs) were used as power electronic interface. But there are several limitations and disadvantages of single-stage inverters (VSIs) like: a) it is only a buck converter for DC-AC power conversion. b) The two semiconductor switches from the same arm or leg of the inverter bridge cannot be gated on simultaneously. Otherwise, a shoot-through will destroy the devices. c) Dead time must be employed, which will cause output voltage/current distortion. Therefore, usually DC-DC boost converter is cascaded in between the VSI bridge and supply terminals to boost the voltage to the required level. But, other drawbacks are remaining same. Reliability of these single-stage and two-stage power conversion topologies is less.

Therefore, in order to avoid the aforementioned drawbacks and limitations of both single-stage and two-stage power conversion systems, impedance (Z)-source inverter was proposed in 2002 with increased reliability. The Z-source inverter (ZSI) provides both buck and boost DC-AC inversion in a single-stage with high electromagnetic interference (EMI). First developed Z-source inverter (ZSI) has certain drawbacks like: a) it draws discontinuous input current from the supply, b)

more stress across the capacitors, c) huge inrush current at start-up condition, d) does not share common ground with source, and e) modulation index is limited by the shoot-through duty ratio which leads to poor utilization of the dc-link voltage and higher stress on the semiconductor switches. Except the last point, remaining all drawbacks can be eliminated by the quasi-Z-source inverters (qZSIs) with same boost factor. Many active impedance (Z)-source inverters (i.e., the impedance network consist of one active switch, two-diodes, and one capacitor) were proposed in the literature which produces the boot factor about same as that of the traditional ZSIs. But, the main drawbacks of these topologies are more stress across the capacitor and semiconductor switches. Generally, solar photovoltaic (SPV) module systems need high boost inverters to connect it to the grid/load. Therefore, to increase the boost factor, the switched-inductor Z-source inverter (SL-ZSI) was presented. But, the SL-ZSI has same drawbacks as the traditional ZSI. So, in order to avoid the drawbacks of SL-ZSI, the SL-qZSIs and Diode/Capacitor-Assisted qZSIs were proposed.

To further improve the boost factor, many magnetically coupled impedance source (MCIS) network topologies were proposed in the literature with less number of components (i.e., both passive and active) in the impedance network. The main disadvantages of coupled-inductor (MCIS) based topologies are; their leakage inductance must be low or they must be tightly coupled, otherwise a high voltage spike appears across the semiconductor switches and dc-link of the inverter bridge. Moreover, the stress across the elements of the impedance network and power switch is also increased. This can lead to use of high rating devices, which in turn increase the cost of the system.

Therefore, enhanced-boost Z-source inverter (EB-ZSI) with two switched-impedance networks topology was proposed recently which provides high boost at low shoot-through duty ratio without any high spikes across the dc-link voltage and power switches. Moreover, the stress across the switches and the components are less. Even though the EB-ZSI topology uses more number of components in the impedance network (i.e., four inductors, four capacitors, and five diodes) when compare to existing topologies, the stresses across those devices (capacitors, diodes, and switches) is less. Therefore, lower rating devices can be used which results in low cost. The EB-ZSI also has similar drawbacks to that of the traditional ZSI/ SL-ZSI. In order to modulate and to control the all existing Z-source inverters,

many modulation techniques were presented in the literature. But for simplicity most of the impedance source networks were analyzed using simple boost method of control.

In this thesis, improved enhanced-boost Z-source inverters are presented which provides high voltage boost in a single-stage at low shoot-through duty ratio and at high modulation index with high reliability, and shares common ground with the source and inverter bridge. Moreover, these presented topologies reduce the starting inrush current problem and capacitor stress. The expressions for inductance and capacitance design are derived. All the inductors, capacitors, switches and diodes with lower ratings can be used owing to the lower voltage stresses so that the cost is largely decreased. Throughout this thesis, the analysis of these presented topologies is carried out using simple boost control (SBC) technique due to its simple structure.

Firstly, the analysis and derivations of different voltage stresses of One switched-inductor ‘Z-source’ / ‘Improved Z’-source inverter is presented. Then, the voltage-lift type of ‘Z-source’ / ‘Improved Z’-source inverter which is derived from one switched-inductor Z-source inverter (One SL-ZSI) is proposed to get high voltage boost with same number of elements in the impedance network just by replacing the middle diode of SL-cell with voltage-lift capacitor. Then, the two configurations of enhanced-boost quasi Z-source inverters (EB-qZSIs) are proposed in this thesis which provides similar voltage boost compare to EB-ZSI using same number of passive components, and draws continuous input current from the input supply which improves the lifespan of passive components. In addition to this, the stress across the capacitors is also reduced. To reduce the capacitor stress of EB-ZSI further, improved topology of EB-ZSI is proposed in this thesis which is named as enhanced-boost series Z-source inverter (EB-SZSI). Therefore, lower rating capacitors can be used to reduce the cost of the system. Another enhanced-boost quasi Z-source inverter is proposed in this thesis which is named as four different configurations of enhanced-boost quasi Z-source inverters which reduces the capacitor stresses further. Except the discrete input current, the other advantages of EB-qZSIs are remained. All these presented topologies are compared with existing Z-network topologies. For the same input voltage and boost factor, the proposed topologies provides less stress across the capacitors, diodes, and semiconductor switches in comparison with existing topologies. Moreover, the proposed topologies require low

shoot-through duty ratio and high modulation index to obtain the same voltage boost. Even though these proposed topologies uses more number of components in the impedance network, the stresses across those devices (capacitors, diodes, and switches) is less which results in low cost and less weight.

The thesis is organized into eight chapters. In **Chapter 1**, a brief introduction of traditional inverters for solar photovoltaic systems such as single-stage and two-stage conversion systems has been given. The drawbacks of traditional single-stage inverter and two-stage inverter topology and the need of impedance (Z)-source inverter (ZSI) topology are discussed. The major contributions of the thesis and the organization of the thesis are also detailed.

Chapter 2 starts with state-of-art of different impedance (Z)-network inverter topologies including conventional Z-source inverter are provided. All these impedance (Z)-source network topologies are broadly classified into coupled-based and non-coupled based inverter topologies and are discussed briefly. Among the non-coupled based topologies available in the literature, the enhanced-boost Z-source inverter (EB-ZSI) with two-switched impedance network topology provides very high boost factor at low shoot-though duty ratio and high modulation index and provides better quality output waveforms. The boost factor of the existing inverter topologies is provided for gain comparison. Some of the magnetically coupled impedance source (MCIS) networks are also addressed, which gives high boost factor at low shoot-through duty ratio with less number of components and the drawback of MCIS networks are also highlighted.

In **Chapter 3**, the circuit development of the one switched-inductor Z-source inverter (one SL-ZSI) from a conventional Z-source inverter is presented. The operating principle, steady-state operation and boost factor derivation of one SL- is explained. The comparison and advantages of one switched-inductor improved Z-source inverter over one SL-ZSI is described in detail. The steady-state operation of one switched-inductor improved Z-source inverter is also validated in experiments.

Chapter 4 presents the voltage-lift concept of Z-source/improved Z-source inverters which is derived from one switched-inductor Z-source inverter. Steady-state operation, derivation of boost factor and voltage gain, and performance comparison of voltage-lift ZSI/improved ZSI is described. The advantages and comparison of both the topologies is discussed in detail. The simulation and experimental results is also given to validate the theoretical analysis.

In **Chapter 5**, the circuit development of the enhanced-boost quasi Z-source inverters (EB-qZSIs) with two switched-impedance network is discussed in detail. The steady-state and principle of operation of EB-qZSIs is explained and the mathematical equation for capacitors and voltage gain is established. The performance comparison of the proposed and existing topologies is also described. The advantages and drawbacks of the proposed EB-qZSIs and other Z-network topologies are described. The steady-state operation of the enhanced-boost quasi Z-source inverters is validated in simulations and experiments to verify the theoretical analysis.

In **Chapter 6**, high boost switched-impedance Z-source inverter, named enhanced-boost series Z-source inverter with two switched impedance network is studied in details. The theoretical analysis of the switched-impedance network series ZSI is validated in simulations and experiments. The detailed performance of the series switched-impedance Z-source inverter is compared in its class to uncover its operational advantages.

Chapter 7 describes another enhanced-boost quasi Z-source inverter, named as four different configurations of enhanced-boost quasi Z-source inverters. In this chapter, four configurations of EB-qZSIs topologies are presented. All these topologies provide same boost factor or voltage gain but with different capacitor stresses. The detail steady-state analysis, design of impedance networks and comparison with other EB-ZSIs are presented. Simulation and experimental tests are conducted in order to validate the theoretical expressions.

The general conclusions of the presented work and possible future research have been summarized in **Chapter 8**.

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This Thesis is dedicated:

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TO MY BROTHERS

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LIST OF ACRONYMS

ac, AC	Alternating Current
dc, DC	Direct Current
VSI	Voltage Source Inverter
CSI	Current Source Inverter
EMI	Electro Magnetic Interference
MPP	Maximum Power Point
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
ZSI	Z-Source Inverter/ Impedance-Source Inverter
qZSI	Quasi Z-Source Inverter
SPV	Solar Photovoltaic
TEG	Thermo Electric Generation
FC	Fuel Cell
HEV	Hybrid Electric Vehicles
UPS	Uninterruptible Power Supplies
MPPT	Maximum Power Point Tracking
ASD	Adjustable Speed Drive
PWM	Pulse Width Modulation
SVM	Space Vector Modulation
DA	Diode-Assisted
CA	Capacitor-Assisted
EB	Enhanced-Boost
IEEE	Institute of Electrical & Electronics Engineers
DSO	Digital Storage Oscilloscope
pf, PF	Power Factor
THD	Total Harmonic Distortion
LCCT	Inductor-Capacitor-Capacitor-Transformer
SL	Switched-Inductor
VL	Voltage-Lift
SI	Switched-Impedance
MCIS	Magnetically Coupled Impedance Source
CL-LSI	Coupled-Inductor L-Source Inverter
SBI	Switched Boost Inverter
CFSI	Current Fed Switched Inverter
L-ZSI	Inductor Z-Source Inverter

SSI	Split Source Inverter
ΔSI	Δ-Source Inverter
YSI	Y-Source Inverter
SZSI	Series Z-Source Inverter
IZSI	Improved Z-Source Inverter
DE-ZSI	Developed Embedded-ZSI
IGBT	Insulated Gate Bipolar Transistor
MLI	Multilevel Inverter
SBC	Simple Boost Control
MBC	Maximum Boost Control
MCB	Maximum Constant Boost
rms, RMS	Root Mean Square
DCM	Discontinuous Conduction Mode
CCM	Continuous Conduction Mode
KVL	Kirchhoff’s Voltage Law
KCL	Kirchhoff’s Current Law
RTW	Real-Time Workshop
MOV	Metal-Oxide Varistor
RTI	Real-Time Interface
TDE	Total Development Environment
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
PCI	Peripheral Component Interconnect
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Array

D_0	Shoot-through duty ratio
F_S	Switching frequency
M	Modulation index
G	Voltage gain
B	Boost factor
Γ	Gamma
Δ	Delta
T	Transformer
Σ	Sigma
V_{DC}	Input dc-voltage
$\hat{V}_{PN}$	Peak-dc link voltage
$\hat{V}_{an}$	Peak-phase voltage
v_{ab}, v_{bc} and v_{ca}	Three-phase line voltages
i_{an}, i_{bn} and i_{cn}	Three-phase currents
C_1, C_2, C_3 and C_4	Z-source network capacitors
L_1, L_2, L_3 and L_4	Z-source network inductors
D_1, D_2, D_3 and D_4	Z-source network diodes
D_{in}	Input diode
K_0	Number of shoot-through states
f_m	Modulating signal frequency
f_{cr}	Carrier signal frequency
m_f	Frequency modulation index
m_a	Amplitude modulation index
V_{C1}, V_{C2}, V_{C3} and V_{C4}	Capacitor voltages
I_{L1}, I_{L2}, I_{L3} and I_{L4}	Average inductor currents
V_{D1}, V_{D2}, V_{D3} and V_{D4}	Diode voltages
V_{Din}	Input diode voltage
I_{in}	Input current
S_0	Gate signal control for switch S
T_S	Switching time period
T_0	Shoot-through period
C_{VL}	Voltage-lift capacitor
V_S	Switch stress
I_{PN}	Average DC-link Current

K_Y	Turns ratio of the transformer in case of Y-source inverter
K_Δ	Turns ratio of the transformer in case of Δ-source inverter
K_δ	Winding factor of the transformer for quasi/ improved Y-source inverter

This chapter describes introduction to the research work that has been carried out in this thesis. The initial study start with some background of renewable and non-renewable energy sources, the benefits of renewable energy sources, and the drawbacks of traditional single-stage and two-stage voltage source inverters used for solar photovoltaic/fuel systems. In continuation to that, the need of high boost Z-source inverters is also highlighted. Then, the advantages and applications of impedance-source inverter topologies are described. Finally, scope of work, author's contribution and thesis outlines are explained.

1.1 Overview

Renewable energy systems have gained much popularity due to their non-emissive nature and abundance. Due to the rapid contraction of the fossil fuel reserve and its detrimental effect on the environment, there is a growing trend towards exploring different renewable energy sources and maximizing energy harvesting out of those sources [1]. Renewable energy sources are inexhaustible, clean and pollution free, recyclable, and are thought to be "free" energy sources, such as solar and wind energies. Over the past few years, renewable energies represent a rapidly growing share of total energy supply, including heat and transportation. In 2016 (the latest year for which data are available), about 15.7% of global final energy consumption came from renewables, and the share of renewable energy sources (including hydro) in electricity generation is around 19.3% [2].

Following are the major problems with conventional energy sources [1, 2];

- Non-renewable (i.e., at projected consumption rates, natural gas and petroleum will be depleted by the end of the 21st century).
- Impurities are the major source of pollution.
- Burning fossil fuels produces large amount of CO_2, which contributes to global warming.
- Makes us rely on other countries for our energy needs and
- Makes us vulnerable.

Therefore, the renewable energy sources like solar photovoltaic, fuel, wind, biomass and biofuels, tidal, geothermal, thermoelectric generation (TEG), and wave energy are attracting more attention as an alternative energy [2 – 4]. Among all these renewable energy sources, the solar photovoltaic (SPV) energy is being widely utilized because of the ubiquity, abundance, clean and pollution free, little

maintenance, and sustainability of solar radiant energy. These photovoltaic cells or solar cells directly use the energy from the sun to generate electricity.

By the end of 2016, the world installed capacity of solar photovoltaic power generation system has reached to 303.1 GW. The annual installed capacity of China, USA, Japan, and India in 2016 was 34.5 GW, 14.7 GW, 8.6 GW, and 4 GW, correspondingly [5].

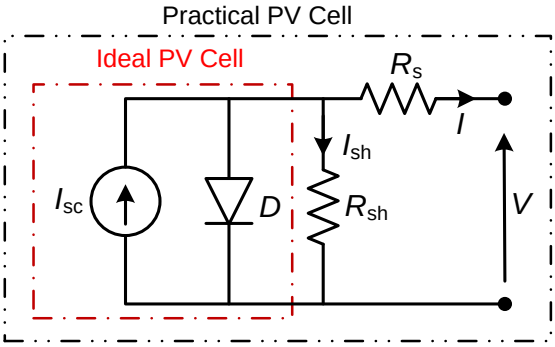


Fig. 1.1: Equivalent circuit of a solar cell.

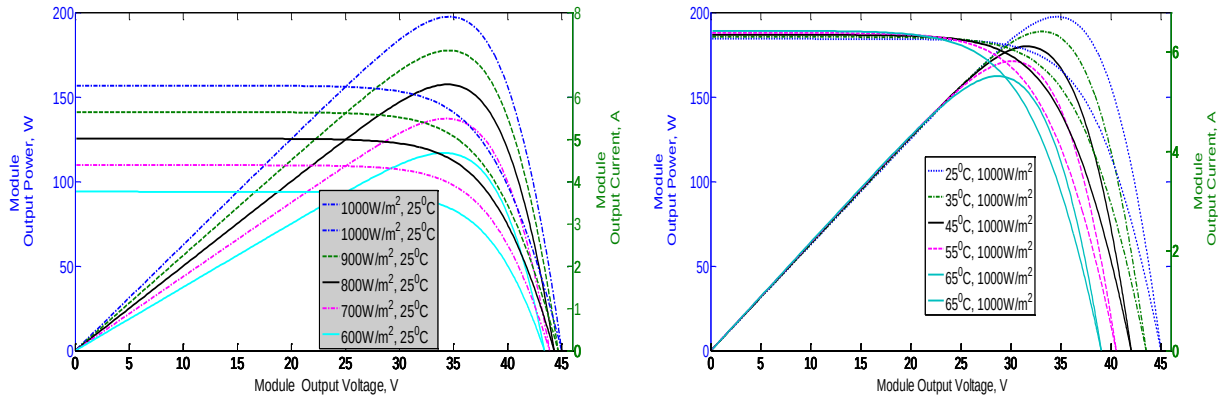
A solar photovoltaic cell can be modelled as a current source I_{SC} in parallel with a diode D as shown in Fig. 1.1. Magnitude of the source current is dependent on the solar irradiation and cell temperature [6]. Voltage drop due to external contacts are represented by a resistance R_s in series with the solar cell. Leakage currents are taken in to account by a parallel resistance R_{sh} connected across the cell. The ideal and practical equivalent circuit of solar cell is clearly shown in Fig. 1.1. Genearlly, in order to get higher output voltage; the cells are to be connected in series. Similarly, to provide more output current, the number of cells is to be connected in parallel combination. Depending upon the load/output requirement, these cells can be connected in parallel or in series combination. The basic equation of a practical solar photovoltaic cell is given by,

$$I = I_{sc} - I_0\left[\exp\left(\frac{V + R_s I}{V_T}\right) - 1\right] - \frac{V + R_s I}{R_{sh}} \tag{1.1}$$

where, I_{sc} – cell current, I_0 – saturation current of the cell, and V_T – thermal voltage of PV cell.

The output power P versus terminal voltage V curve (P vs V curve) as wellas output current I versus terminal voltage V curve (I vs V curve) of a typical solar PV module at different irradiation (assuming constant temperature) and temperature (irradiation kept constant) are shown in Fig. 1.2(a) and Fig. 1.2(b) respectively. From this figure, it is observed that the output power of a PV module mainly depends on

the solar irradiation and its cell temperature. The solar PV module output power may maximum at a particular PV terminal voltage which is the maximum power point (MPP) voltage of a module. Therefore, in order to track/ extract the peak (maximum) power point of the solar PV module/ array, many papers have been discussed in the literature [6 – 10].



(a) (b)

Fig. 1.2: Characteristics of solar photovoltaic module: (a) variation of irradiation at constant temperature of 25^0C; (b) variation of temperature at constant irradiation of 1000W/m^2.

The most common PV technologies are the monocrystalline and the multicrystalline silicon modules, however PV cells with other materials like Cadmium Telluride (CdTe), Gallium Arsenide (GaAs), etc., to name few.

1.2 Solar Photovoltaic Inverter Topologies

Solar photovoltaic (SPV) inverter systems can be broadly categorised into following four groups [11]. They are:

a) The Past—Centralized PV Inverters

The past technology, illustrated in Fig. 1.3(a), was based on centralized inverters that interfaced a large number of PV modules to the grid [11]. The PV modules were divided into series connections (called a string), each generating a sufficiently high voltage to avoid further amplification. These series connections were then connected in parallel, through string diodes, in order to reach high power levels. This centralized inverter includes some severe limitations, such as high-voltage dc cables between the PV modules and the inverter, power losses due to a centralized maximum power point tracking (MPPT), mismatch losses between the PV modules, losses in the string diodes, and a nonflexible design where the benefits of mass production could not be reached.

b) The Present—String Inverters

The string inverter, shown in Fig. 1.3(b), is a reduced version of the centralized inverter, where a single string of PV modules is connected to the inverter [11]. The input voltage may be high enough to avoid voltage amplification. The possibility of using fewer PV modules in series also exists, if a dc–dc converter or line-frequency transformer is used for voltage amplification. There are no losses associated with string diodes and separate MPPTs can be applied to each string. This increases the overall efficiency compared to the centralized inverter, and reduces the price, due to mass production. However, the major drawback of such topology is that there is a voltage de-rating of the semiconductor.

c) The Future—Multi-String Inverters

The multi-string inverter depicted in Fig. 1.3(c) is the further development of the string inverter, where several strings are interfaced with their own dc–dc converter to a common dc–ac inverter [11, 12]. This is beneficial, compared with the centralized system, since every string can be controlled individually. Thus, the operator may start his/her own PV power plant with a few modules. Further enlargements are easily achieved since a new string with dc–dc converter can be plugged into the existing platform. A flexible design with high efficiency is hereby achieved. This configuration uses two-stages (i.e., dc-dc converter is used to extract maximum power from PV and then dc-ac converter to connect it to grid) to transfer the power, which increases the cost.

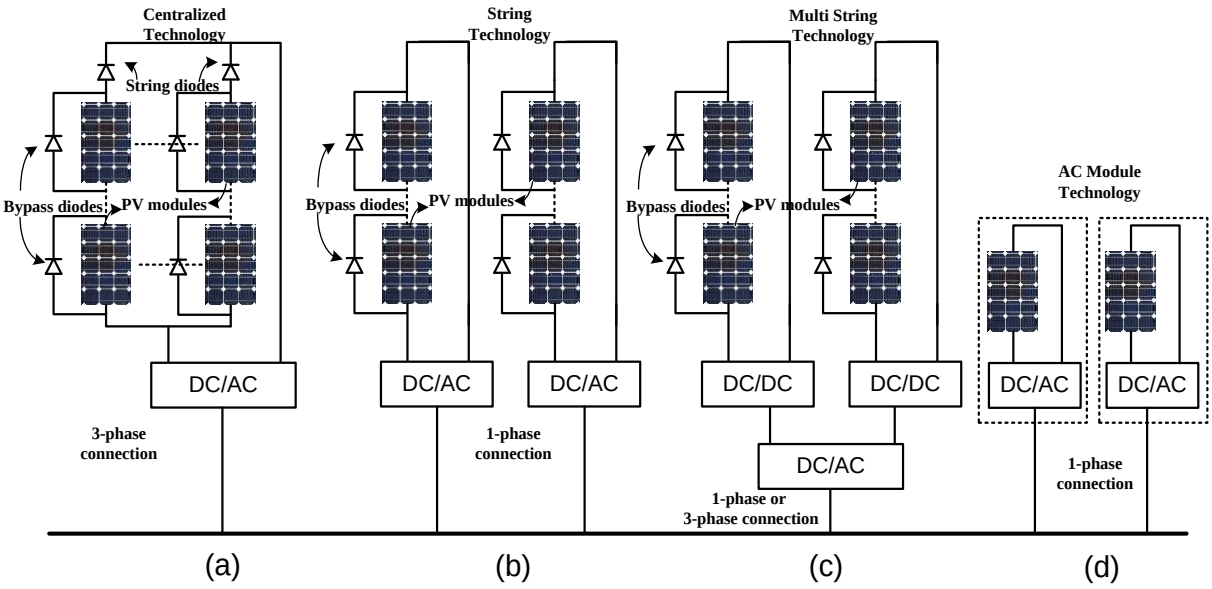


Fig. 1.3: Historical overview of PV inverters: (a) past centralized technology; (b) present string technology; (c) present and future multi-string technology; (d) present and future ac-module and ac cell technologies.

d) AC Modules

The converter module in Fig. 1.3(d) is a reduction of the string inverter, where each PV module has its own integrated power electronics interface to the utility.

The ac module depicted in Fig. 1.3(d) is the integration of the inverter and PV module into one electrical device [12]. It removes the mismatch losses between PV modules since there is only one PV module, as well as supports optimal adjustment between the PV module and the inverter and, hence, the individual MPPT. It includes the possibility of an easy enlarging of the system, due to the modular structure. The opportunity to become a “plug and play” device, which can be used by persons without any knowledge of electrical installations, is also an inherent feature. On the other hand, the necessary high voltage-amplification may reduce the overall efficiency and increase the price per watt, because of more complex circuit topologies. On the other hand, the ac module is intended to be mass produced, which leads to low manufacturing cost and low retail prices.

The present solutions use self-commutated dc–ac inverters, by means of insulated gate bipolar transistors (IGBTs) or metal oxide semiconductor field-effect transistors (MOSFETs), involving high power quality in compliance with the standards.

Next follows a classification of different inverter technologies used in solar photovoltaic systems. The topologies are categorized on the basis of number of power processing stages.

1.2.1 Single-stage DC- AC Power Conversion

The inverter shown in Fig. 1.4 is a single-stage inverter, which must handle all tasks itself, i.e., MPPT, grid current control and, perhaps, voltage amplification [11]. This is a typical configuration of centralized inverter shown in Fig. 1.3(a). The inverter must be designed to handle a peak power of twice the nominal power.

Single-stage inverters only need one power stage to process power conversion from dc to ac and provide the dc input voltage to required output voltage level as shown in Fig. 1.4 [13, 14]. Single-stage inverters usually have a relative simple topology, and employ the fewer components, thus cause a higher efficiency. As shown in this figure, each power switch is realized by MOSFET/IGBT and has an anti-parallel diode to facilitate bi-directional power transfer between the input and output terminals. The output of each leg, for example V_{AN} (with respect to the negative dc bus), depends only on V_{DC} and the switch status; the output voltage is

independent of the output load current since one of the two switches in a leg is always on at any instant. The blanking time is ignored in practical circuits by assuming the switches to be ideal. Therefore, the inverter output voltage is independent of the direction of the load current.

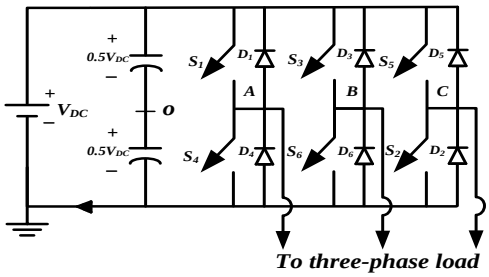


Fig. 1.4: Schematic of conventional voltage source inverter.

1.2.1.1 Limitations and Drawbacks of the Single-stage Conversion

Following are the few limitations of the traditional single-stage VSI [13 – 17]:

1. The peak AC output voltage is always less than the input dc-link voltage or in other word; the input dc-link voltage has to be greater than the desired peak AC output voltage.
2. If the modulation index is increased beyond 1, the harmonic content in the output voltage increases. So, the output filter size has to be higher. Even with a higher size filter the theoretical rms ac output voltage cannot exceed 0.85 times the dc input voltage.

Moreover, in addition to the above mentioned limitations, the traditional single-stage VSI also has some of the following drawbacks [14, 18]:

1. The upper and lower switching devices of any phase leg cannot be turned on simultaneously either purposefully or by electromagnetic interference (EMI). If they are turned on at the same time, it will result in shoot-through and flow of high short circuit current which can be detrimental for the switching devices. The shoot-through phenomenon due to the EMI noise is a major drawback of the VSI topology and reason for its low reliability. Generally, dead-band between the switching signals is provided in VSI to avoid the shoot-through, but the chances of shoot-though due to EMI still remains.
2. Introduction of dead-band between the switching signals of complementary switches of the inverter legs causes AC output distortion and requires for complex dead-band compensation circuits.
3. A line frequency step-up transformer can also be used to achieve step up at the AC output although transformer based systems have the disadvantage of

higher weight, space requirement, and reduced system efficiency and reliability.

1.2.2 Two-stage Power Conversion

The configuration of dual-stage inverter is depicted in Fig. 1.5. The dc–dc converter is now performing the MPPT (and perhaps voltage amplification or electrical isolation). Dependent on the control of the dc–ac inverter, the output from the dc–dc converters is either a pure dc voltage (and the dc–dc converter is only designed to handle the nominal power), or the output current of the dc–dc converter is modulated to follow a rectified sine wave (the dc–dc converter should now handle a peak power of twice the nominal power) [13, 14]. The dc–ac inverter is in the former solution controlling the grid current by means of pulse width modulation (PWM) or bang-bang operation. In the latter, the dc–ac inverter is switching at line frequency, “unfolding” the rectified current to a full-wave sine, and the dc–dc converter takes care of the current control. A high efficiency can be reached for the latter solution if the nominal power is low. On the other hand, it is advisable to operate the grid-connected inverter in PWM mode if the nominal power is high.

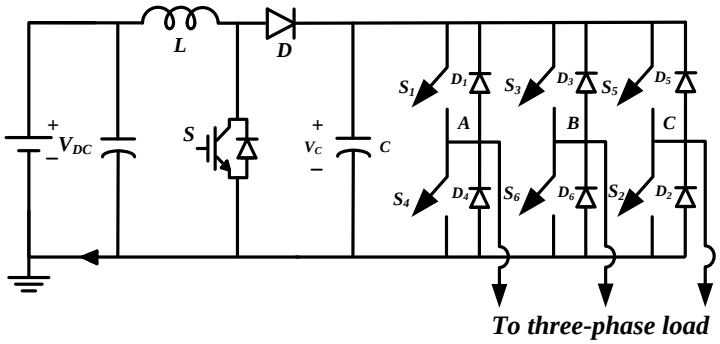


Fig. 1.5: Illustration of two-stage converter.

Two-stage inverters can solve the problems when single-stage inverters meet with high power, high performance requirement. As shown in Fig. 1.5. In the circuit, a dc-dc boost converter is ahead of the dc-ac inverter. With the first stage, input voltage is boost to suited dc voltage, and output ac voltage can be obtained by a high frequency PWM inverter through the second stage. The whole process flows as the dc-dc-ac process.

Two-stage high boost inverters can be realized using high boost DC-DC converter cascaded voltage source inverter topology, isolated DC-DC boost type converter cascaded VSI topology, etc as shown in Fig. 1.5 where a conventional boost converter cascaded with a VSI to feed power to a load.

Maximum gain of conventional boost, cascaded boost converters, or quadratic boost converters is limited and is achieved at extremely high duty ratio (D_0) i.e., at near unity duty ratio. Thus, they are not well suited for high boost inversion. When a boost converter operates at near unity duty ratio, the diode and the output capacitor has to carry a current of high amplitude with very small pulse-width. This results in severe reverse recovery current of the diode, increased conduction loss and production of electromagnetic interference (EMI). The problem becomes more severe when operating at very high switching frequency as the reverse-recovery time of the device may be smaller than the time available during (1- D_0) interval [15].

1.2.2.1 Drawbacks of Two-stage Converter

Similar to single-stage converter, the two-stage converter is also has certain drawbacks [13 – 17];

1. The upper and lower switching devices of any phase leg of VSI bridge cannot be turned on simultaneously either purposefully or by electromagnetic interference (EMI). If they are turned on at the same time, it will result in shoot-through and the dc-link capacitor will be short citcuited. The shoot-through phenomenon due to the EMI noise is a major drawback of the VSI bridge and reason for its low reliability. Generally, dead-band between the phase legs is provided in VSI bridge to avoid the shoot-through, but the chances of shoot-though due to EMI still remains.
2. Introduction of dead-band between the switching signals of complementary switches of the inverter legs causes AC output distortion and requires for complex dead-band compensation circuits.
3. Moreover, the power switch and additional components in DC-DC boost converter increases the cost.

Many traditional converter topologies were discussed in [16 – 18] and have certain disadvatages. The overview and comparison of different single-phase topologies for ac module applications shown in Fig. 1.3 were discussed in [19]. Therefore, in order to avoid the above aforementioned drawbacks and limitations of both single-stage and two-stage power conversion topologies, many impedance (Z)-source power electronic converters were discussed in [20] along with their modulation technique, applications, and modeling and control.

The next section, explains about the traditional Z-source inverter (ZSI) proposed by F.Z. Peng in 2002 [21].

1.2.3 Single-stage Impedance (Z)-Source Network DC-AC Power Conversion

As illustrated in Fig. 1.3(d), the ac module concept is the combination of one PV module with a grid-connected single-stage inverter.

As discussed in above sections of this chapter, the single-stage and two-stage inverter topologies have certain drawbacks and limitations. In order to avoid those aforementioned drawbacks, the single-stage Z-source inverter (ZSI) with buck-boost capability has been proposed in [21]. The circuit configuration of classical Z-source inverter is shown in Fig. 1.6 in which the impedance network consists of two split inductors (L_1, L_2), two capacitors (C_1, C_2), and an input diode D_{in}. The use of series or input diode D_{in} allows the boosting of voltage and also prevents the reverse current flow.

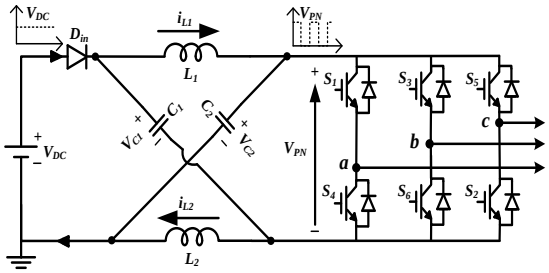
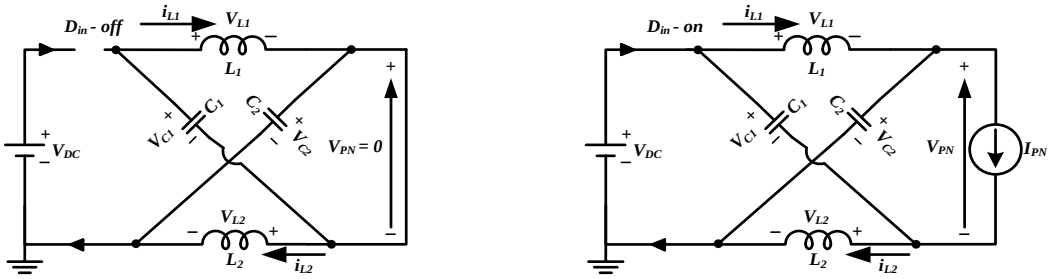


Fig. 1.6: Illustration of conventional Z-source inverter.

Insertion of shoot-through state in the inverter operation allows ZSI to achieve high boost capability at its end. As shoot-through state of the inverter bridge is a valid operating state of ZSI, it exhibits better electromagnetic interference (EMI) immunity than the single-stage and two-stage topologies. This feature allows the converter to alleviate requirement of dead-band circuit and thus avoiding waveform distortion.



(a) (b)

Fig. 1.7: Circuit configurations of Z-source inverter: (a) shoot-through state; (b) non-shoot-through state.

To explain the steady-state operation of the ZSI, let us assume that the inverter bridge is in one of the fifteen possible states (i.e., six active, two zero, and seven shoot-though states) for three-phase system.

During shoot-through state, the equivalent circuit is shown in Fig. 1.7(a). As shown in this figure, the inverter bridge is represented by a short circuit during the interval D_0T_S. The input diode D_{in} operates in forward blocking mode and the energy stored in the capacitors is transferred to the inductors through the inverter bridge. Therefore, from this figure, inductor voltages can be written as

$$V_{L1} = V_{L2} = V_L = V_C \tag{1.2}$$

$$V_{Din} = 2V_C; \quad V_{PN} = 0. \tag{1.3}$$

For the remaining duration, the inverter bridge is in one of the eight non-shoot-through states. In this interval, the input diode D_{in} is in forward conducting mode. The inverter bridge is represented by a current source in this interval as depicted in Fig. 1.7(b). Now, the input voltage V_{DC}, and inductors together supply power to the inverter bridge and the capacitors are charged through input diode D_{in}. From Fig. 1.7(b), we have,

$$V_L = V_{DC} - V_C \tag{1.4}$$

$$V_{Din} = V_{DC}; \quad V_{PN} = 2V_C - V_{DC}. \tag{1.5}$$

Applying volt-sec balance principle to inductor, one can write as

$$D_0.V_C + (1-D_0).(V_{DC} - V_C) = 0 \tag{1.6}$$

From the above equation, the capacitor voltage can be obtained as

$$V_C = \frac{(1-D_0)}{(1-2D_0)} V_{DC} \tag{1.7}$$

Similarly, the peak dc-link voltage across the inverter bridge can be expressed as

$$\begin{cases} \hat{V_{PN}} = \dfrac{1}{(1-2D_0)} V_{DC} \\ \hat{V_{PN}} = BV_{DC} \end{cases} \tag{1.8}$$

The boost factor B is defined as the ratio of peak dc-link voltage across the inverter bridge to the input supply voltage V_{DC} can be expressed as

$$B = \frac{\hat{V_{PN}}}{V_{DC}} = \frac{1}{1-2\left(\dfrac{T_0}{T_S}\right)} = \frac{1}{1-2D_0} \tag{1.9}$$

where T_0 is the shoot-through zero state interval during a switching period T_S and D_0 is the shoot-through duty ratio of each cycle and is equal to T_0/T_S .

From (1.9), it is seen that shoot-through duty ratio D_0 is limited to the range from minimum value zero to the maximum value 0.5 in which the impendence network can perform the step-up dc–dc conversion from V_{DC} to V_{PN}. For the practical applications, in order to provide a very high boost factor for the low-voltage dc energy source, usually a large value of D_0 needs to be taken, i.e., the Z-source converter would have to be operated under the extreme condition of a long interval of the shoot-through zero state. Unfortunately, the constraint of low M and high D_0 will cause a new conflict of the output power quality and system boost inversion ability (i.e., poor inversion ability at the fundamental frequency). For simple boost control method, the modulation index M is limited by shoot-through duty cycle and is given as

$$M \leq 1 - D_0 \tag{1.10}$$

where,

$$M = \frac{\text{Amplitude of the modulation waveform}}{\text{Amplitude of the carrier waveform}}$$

The modulation index M has a linear relation to the magnitude of the output voltage at the fundamental frequency [17, 18].

For an optimum system design of the Z-source inverter, the practical values of M have to be made close to *1*, and D_0 has a small upper limit according to (1.10). Therefore, the practical boost factor of Z-source impedance network is usually restricted seriously by two.

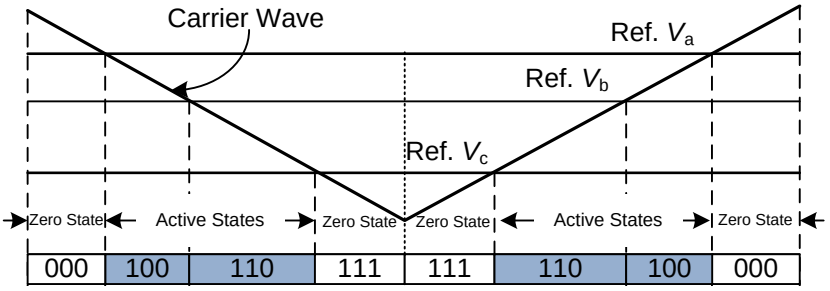
The major factor is the actual physical voltage gain produced by the z-source inverter. Although, theoretically the voltage gain or boost factor of the inverter can be boosted to any desired value without any upper limit. But, due to the presence of the parasitic influences generally lowers the attainable gain to a finite (sometimes unsatisfactory) value. This degradation is usually more prominent at high gain, high-duty-ratio operating conditions, during which the boost inductor is charged over a longer time duration and discharged (or recovered back to its initial state) within an unrealistically short time interval.

The Z-source concept can be applied to all dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion.

In order to modulate the traditional Z-source inverter, the following section provides the brief information about simple boost control method.

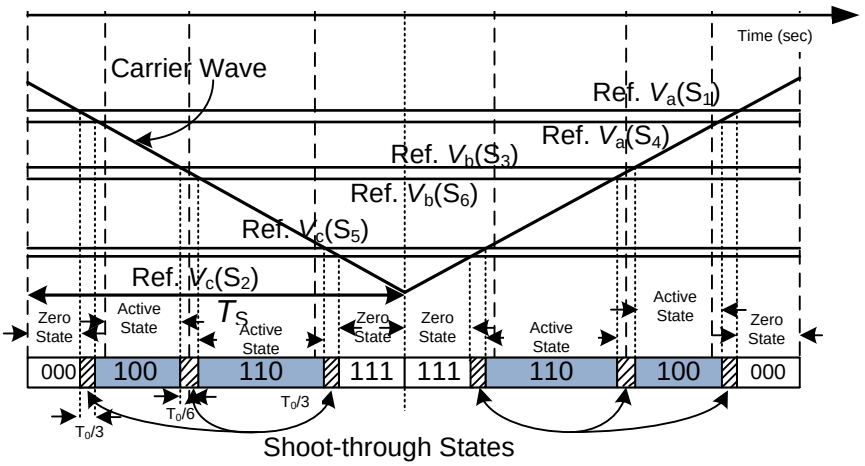
1.2.3.1 Modulations Techniques of the Three-phase Impedance (Z) - Network Inverter Topologies

In this thesis, all the presented topologies are anaysed using simple boost control as the modulation technique [21]. Therefore, in order to understand the basic concept of the simple boost control method, this section describes the switching states, equivalent cuircuits and corresponding output voltages which is derived from conventional sinusoidal PWM technique.



Conventional VSI PWM Technique

(a)



Simple Boost Control PWM Technique of ZSI

(b)

T/6

Fig. 1.8: Modulation techniques of three-phase: (a) voltage source inverter; (b) Impedance (Z)-source inverter.

Fig. 1.8(a) illustrates the switching state sequence of a conventional three-phase-leg VSI, where three state transitions occur (e.g., null {000} →active {100} →active {110} →null {111}) and the null states at the start and end of a switching cycle span equal time intervals to achieve optimal harmonic performance. With three-state transitions, three equal-interval shoot-through states can be added immediately adjacent to the active states per switching cycle for modulating a Z–source inverter and is depicted in Fig. 1.8(b). Preferably, the shoot-through states should be inserted

such that equal null intervals are again maintained at the start and end of the switching cycle to achieve the same optimal harmonic performance.

The preferred state sequence and placement are shown in the Fig. 1.8(b), where the middle shoot-through state is symmetrically placed about the original switching instant. The active states {100} and {110} are left/right shifted accordingly by $T_0/6$ with their time intervals kept constant, and the remaining two shoot-through states are lastly inserted within the null intervals, immediately adjacent to the left of the first state transition and to the right of the second transition. This way of sequencing inverter states also ensures a single device switching at all transitions. The other shoot-through states cannot be used since they require the switching of at least two phase-legs at every transition.

The switching combinations and their equivalent circuits of inverter legs of VSI bridge at different instant of switching states of switches/legs are shown in Fig. 1.9. The switching states of six active states (i.e., S1 to S6) and two null (zero) states (i.e., S0 and S7) are depicted in Fig. 1.9(a). Similarly, the Fig. 1.9(b) shows the seven different combinations of shoot-through states (i.e, E1 to E7).

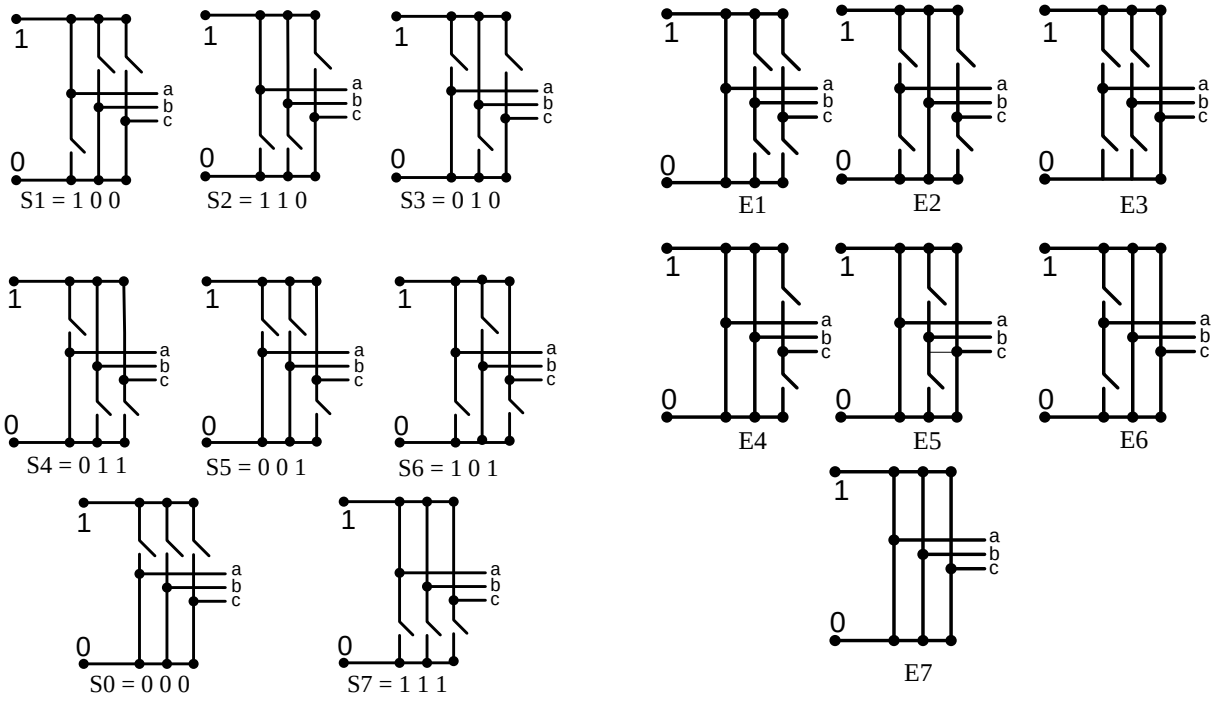


Fig. 1.9: Typical switching states of the three-phase Z-source inverter: (a) eight switching states including 6-active and 2-zero states; (b) seven shoot-through states.

Table. 1.1 lists the fifteen switching states and their corresponding output voltages for Fig. 1.9 of a three-phase-leg Z-source inverter. In addition to the six active and two null (zero) states associated with a conventional VSI, the Z-source

inverter has seven shoot-through states representing the short-circuiting of a phase-leg (shoot-through states E1 to E3), two phase-legs (shoot-through states E4 to E6) or all three phase-legs (shoot-through state E7).

These shoot-through states (E1 to E7) boost the dc link capacitor voltages and can partially supplement the null states within a fixed switching cycle without altering the normalized volt–sec average, since both states similarly short-circuit the inverter three-phase output terminals, producing 0 V across the ac load. Shoot-through states can therefore be inserted to existing PWM state patterns of a conventional VSI to derive different modulation strategies for controlling a three-phase-leg Z-source inverter.

Table. 1.1: Switching states and their corresponding output voltages of three-phase-Z-source inverter ($!s_x$ represents complement of s_x, where x =1, 3, or 5)

Switching State	Output Voltage	S_1	S_4	S_3	S_6	S_5	S_2
Active State S1 {100}	finite	1	0	0	1	0	1
Active State S2 {110}	finite	1	0	1	0	0	1
Active State S3 {010}	finite	0	1	1	0	0	1
Active State S4 {011}	finite	0	1	1	0	1	0
Active State S5 {001}	finite	0	1	0	1	1	0
Active State S6 {101}	finite	1	0	0	1	1	0
Zero State S0 {000}	0 V	0	1	0	1	0	1
Zero State S7 {111}	0 V	1	0	1	0	1	0
Shoot-through State E1	0 V	1	1	S_3	$!S_3$	S_5	$!S_5$
Shoot-through State E2	0 V	S_1	$!S_1$	1	1	S_5	$!S_5$
Shoot-through State E3	0 V	S_1	$!S_1$	S_3	$!S_3$	1	1
Shoot-through State E4	0 V	1	1	1	1	S_5	$!S_5$
Shoot-through State E5	0 V	1	1	S_3	$!S_3$	1	1
Shoot-through State E6	0 V	S_1	$!S_1$	1	1	1	1
Shoot-through State E7	0 V	1	1	1	1	1	1

1.2.3.2 Advantages of Z-source Inverter

Following are the some advantages of the Z-source inverter when compared to both traditional single-stage and two-stage converters [20, 21].

1. The rms ac output voltage of the ZSI can be either higher or lower than the available source voltage. Provides wide range of ouput voltage capability.

2. The ZSI allows the inverter bridge to be operated in shoot-through state. So, the dead-band circuit is not necessary which in turn reduces the cost.
3. As the ZSI allows shoot-through state, it exhibits better EMI noise immunity when compared to the traditional VSI.
4. Moreover, it also improves the reliability of the system.

1.2.3.3 Limitations of the Traditional Z-source Inverter

Following are the some of the limitations of the conventional ZSI.

1. To obtain high boost factor/ voltage gain, the shoot-through duty ratio has to increase which results in distortion in output voltage quality and increases the total harmonic distortion (THD).
2. Due to parasitic effects of passive components, the boost factor is limited two.
3. If the ZSI is operated at high boost factor, the passive and active components have to be designed at higher rating.
4. High boost factor ZSI increases the capacitance and inductance size, which increases the cost of the system, and
5. The stress across the device is also more.

Without any modifications in the impedance network of ZSI, some modulation techniques were available in the literature which increases the boost factor and reduces the device stress [22, 23].

In order to modulate the Z-source inverters, many modulation techniques were reported in [21 – 40]. To avoid the aforementioned drawbacks and improve the performances of traditional ZSI, many impedance source network topologies were presented in the literature [41 – 102]. These different Z-network inverter topologies were used in many applications and were described in [103 – 140]. The modeling and control of Z-source inverters has been elaborated in [141 – 156].

1.3 Need for High Boost Impedance Source Network Inverter Topologies

High boost inversion is essential in several renewable energy systems like small roof-top solar photovoltaic, fuel cell applications when the output of the system is connected to 110V AC systems. As discussed in the last section, the module SPV inverter system provides maximum power harvesting, a high boost inverter system is thus essential. In a traditional voltage source inverter, either a step-up transformer at the inverter output or a dc-dc boost converter at the input side of inverter is used.

This line frequency step-up transformer or the additional dc-dc converters used for step-up purpose have the disadvantages of higher weight, more space requirement, bulky, reduced system efficiency and reliability of the system [16 – 18].

Therefore, now a days, the use of high boost Z-source inverters (ZSIs) finds wide applications in industrial motor drives systems [103 – 111], hybrid electric vehicles (HEV) [112 – 116], uninterruptible power supplies (UPS) [117], fuel-cell applications [118 – 120], and solar photovoltaic (SPV) [121 – 140] etc., to name a few.

1.4 Scope of the Thesis and Author's Contribution

To overcome the aforementioned shortcomings of conventional single-stage and two-stage power conversion topologies of PV inverters, novel single-stage high boost impedance (Z)-source network based inverter topologies are investigated in this thesis. The proposed inverters provide very high boost AC output with buck-boost capability. Thus, they are capable of operating in a wide input range. The development of the inverter topology and analysis are the main features of this thesis. The major contributions of this thesis are summarized as follows.

1. Development of VL-ZSI/ VL-Improved ZSI from One SL-ZSI/Improved ZSI.
2. Development and analysis of enhanced-boost quasi Z-source inverter topologies.
3. Steady-state analysis and state-space analysis of the enhanced-boost series Z-source inverter topology.
4. Derivation of four different configuartions of enhanced-boost quasi Z-source inverter topologies derived from enhanced-boost quasi Z-source inverters and their steady-state analysis.
5. Validation of the proposed topologies in simulation and experiments tests.

1.5 Organization of the Thesis

Apart from this chapter, the thesis contains seven more chapters and the work included in each chapter is briefly outlined as follows:

Chapter 2 starts with state-of-art of different Z-source inverter topologies including conventional Z-source inverter are provided. All these Z-source inverter topologies are broadly classified into coupled-based and non-coupled based inverter topologies and are discussed briefly. Among the non-coupled based topologies available in the literature, the enhanced-boost Z-source inverter with two-switched

impedance network topology provides very high boost factor at low shoot-though duty ratio and high modulation index. Some of the magnetically coupled impedance source (MCIS) networks are also addressed in this thesis which gives high boost factor at low shoot-through duty ratio with less number of components and the drawback of MCIS networks are also highlighted.

In Chapter 3, the circuit development of the one switched-inductor Z-source inverter (one SL-ZSI) derived from a conventional Z-source inverter is presented. The operating principle, steady-state operation and boost factor derivation of one SL-ZSI is explained. The comparison and advantages of one switched-inductor improved Z-source inverter over one SL-ZSI is described in detail. The steady-state operation of one switched-inductor improved Z-source inverter is validated with simulation results.

Chapter 4 presents the voltage-lift concept of Z-source/improved Z-source inverter which is derived from one switched-inductor Z-source inverter. Steady-state operation, derivation of boost factor and voltage gain, and performance comparison of voltage-lift ZSI is described. The simulation and experimental results is also obtained to validate the theoretical analysis.

Chapter 5 discusses a high boost switched-impedance Z-source inverter, named enhanced boost quasi Z-source inverters with two switched impedance network. The detailed performance comparison between various non-coupled based inverter topologies like ZSI, SL-ZSI, extended boost-qZSIs, enhanced-boost Z-source inverter, and the enhanced-boost quasi Z-source inverters is done to unfurl its operational advantages. The steady-state operation of the enhanced-boost quasi Z-source inverters is validated in simulations and experiments to verify the theoretical analysis.

In Chapter 6, another high boost switched-impedance Z-source inverter, named switched-impedance series Z-source inverter with two switched impedance network is studied in details. The detailed performance of the series switched-impedance Z-source inverter is compared in its class to uncover its operational advantages. The state-space analysis of the proposed topology is also carried out. The theoretical analysis of the two switched-impedance network series ZSI is validated in simulations and experimental tests.

Chapter 7 describes the four configurations of enhanced-boost quasi Z-source inverters which may operate in continuous* input current configurations. The detail steady-state analysis, design of impedance networks and comparison with other EB-

ZSIs are presented. Simulation and experimental tests are conducted in order to validate the theoretical expressions.

Chapter 8 provides concluding remarks along with the future scope of the research related to this thesis.

CHAPTER 2: STATE-OF-ART OF Z-SOURCE INVERTER TOPOLOGIES

This chapter narrates state-of-art-of the impedance (Z)-network inverter topologies. It starts with traditional Z-source inverter (ZSI) and some modifications in the impedance (Z) - network to enhance the boost factor (or voltage gain) of conventional Z-source inverters. Then, the classification of the Z-source inverters based on the magnetic coupling and non-magnetic coupled inductor Z-network topologies are also discussed. Next, the drawbacks and effect of leakage inductances on the magnetic coupled based Z-network topologies are explained.

2.1 Introduction

As discussed in the previous chapter, the single-stage conventional voltage source (or voltage fed) inverter (VSI) has some drawbacks like: a) the output AC voltage cannot be greater than the input DC voltage, b) the switching on of both the devices in a leg can destroy the semiconductor devices, therefore a dead-band circuit is needed to provide the time delay between the switching pulses, c) due to the dead-band circuit, the distortion appears in the output waveforms and increases the total harmonic distortion (THD) [163]. Accordingly, many authors in the literature have presented two-stage converters in which the DC-DC boost converter is cascaded in between input DC supply and the VSI bridge to get higher AC output voltage than the input DC voltage but other drawbacks are retained the same.

In order to avoid above mentioned drawbacks of both the single-stage and two-stage converters, an impedance source (or impedance fed) inverter (ZSI) was proposed in 2002 by F. Z. Peng [21]. Later on many Z-Network topologies are presented in the literature to improve their performances. To improve the voltage gain (or to increase the efficiency), some of the research papers are explained about pulse width modulation techniques [21 – 40].

The traditional ZSI has certain drawbacks [41]. To avoid these drawbacks, the quasi ZSIs [43] and improved ZSI [45] were proposed in 2008 and 2009 respectively with same boost factor. In order to improve the boost factor, the extended-boost qZSIs were proposed in [47] with additional elements. To further improve the boost factor, the switched-inductor ZSI [49] and switched-inductor quasi ZSIs [50, 51] were proposed in which the two inductors (L_1, L_2) of traditional ZSI and qZSIs respectively were replaced with switched-inductor (SL) cells.

Many switched-boost inverters (SBIs) [59 – 68] were presented in the literature with less number of passive components but with additional active switches to get

about same boost factor as that of the traditional ZSI. The voltage gain can also be increased with help of voltage-lift unit with less number of passive and active components [69, 100]. But these SBIs topologies results in high stress across the capacitors and semiconductor switches. To increase the boost factor and decrease the inrush current problem, the L-Z-source inverter (L-ZSI) was proposed in [70] with only diodes and inductors (which forms switched-inductor cell) and without any capacitors in the impedance network.

To enhance the boost factor further, many magnetically-coupled impedance source (MCIS) inverters were proposed in the literature [75 – 97] by varying both duty cycle and turn's ratio freely with less number of elements in the impedance network. Depending on their components used in the impedance network, these MCIS networks can be classified as two winding [75 – 88], three winding [89 - 93], and active MCIS networks [94 – 96]. But, their magnetic coupling must be strong or their leakage inductance must be small enough. Otherwise huge voltage spikes will appear across the dc-link/ switches which require higher voltage rating switching devices which in turn increases the cost [98, 99].

Keeping at account, enhanced-boost Z-source inverter (EB-ZSI) was proposed in [73] which produce high voltage gain at low shoot-through duty ratio and high modulation index. For the same shoot-through duty ratio, the EB-ZSI provides high boost factor among all the Z-source network topologies. The main objective of the EB-ZSI was the use of the high number of elements (i.e., both passive and active) with low rating instead of using a low number of elements with high rating in a way that tolerate high voltages in high voltage gains [73]. Due to lack of transformer/magnetic coupling in all the proposed topology, there is no problem about magnetic coupling. Similar to ZSI, the EB-ZSI has certain drawbacks; such as discrete input current, does not share common ground with supply, large inrush current, and high capacitor stress. To avoid these drawbacks, author has proposed improved enhanced-boost Z-source inverter topologies.

2.2 Review of Z-Source Network Topologies

In this section, a broad overview of different Z-source network topologies is addressed [91]. Based on the type of components used in the impedance networks, these impedance (Z)-network topologies are categorised into coupled/transformer based and non-coupled inductor based topologies and some of the Z-network topologies are depicted in Fig. 2.1.

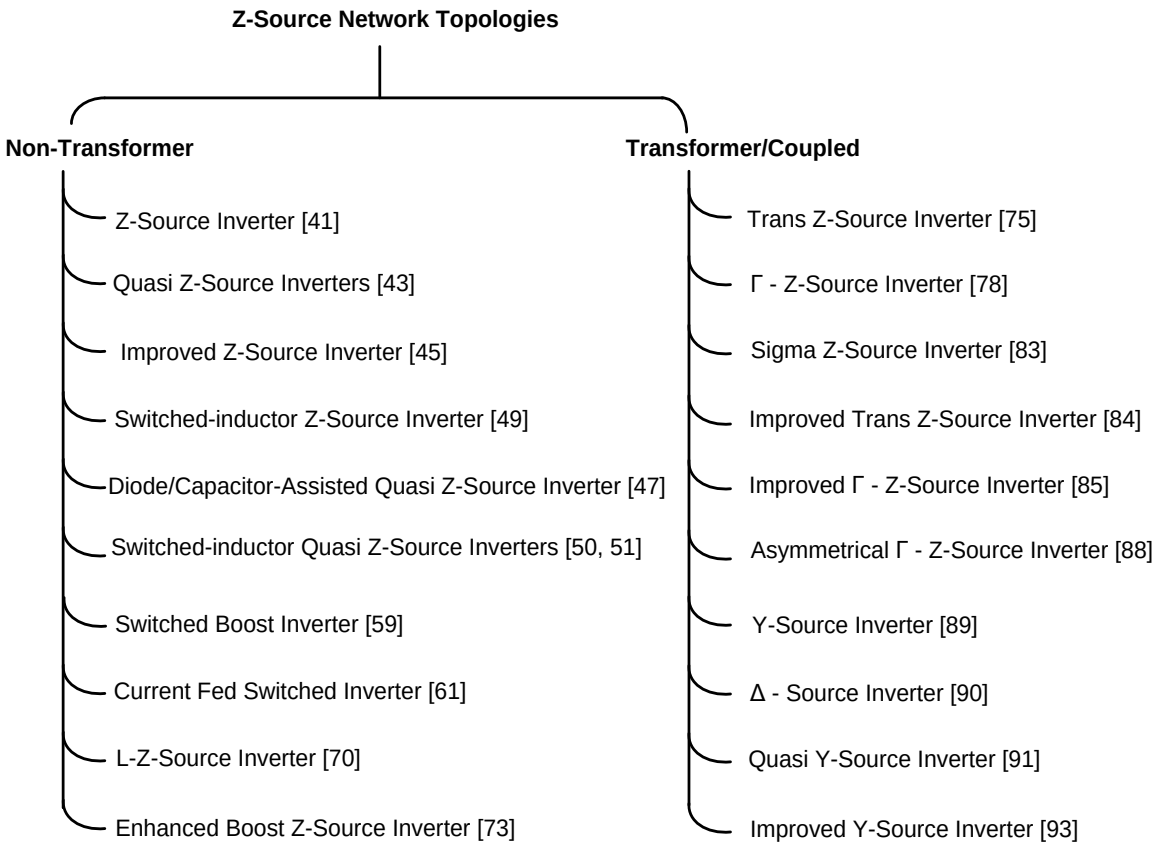


Fig. 2.1: Overview of impedance (Z)-source network topologies (*as of Dec. 2017*).

In the next section, some of the Z-source network topologies will be discussed along with their advantages and disadvantages.

2.3 Non-coupled based Z-Source Network Topologies

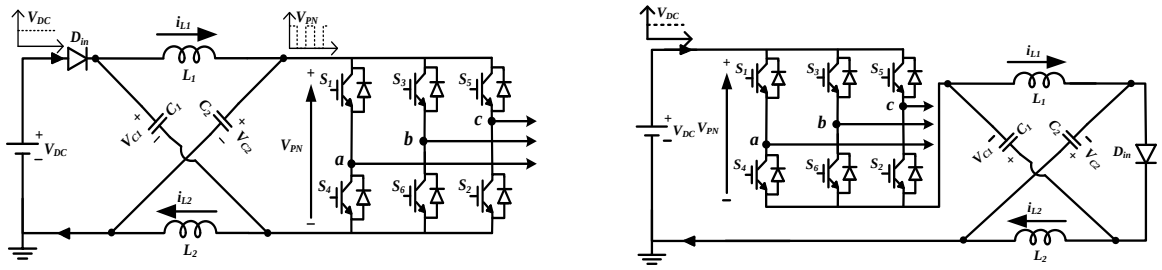
To increase the boost factor (or to improve the performance characterises) and to reduce the stress across the devices there are many topologies are proposed in the literature with separate inductors [41 – 74].

In the next subsections, different types of non-coupled inductor topologies will be addressed.

2.3.1 Conventional "Z"/ "Quasi-Z" - Source Inverters

As shown in Fig. 2.2(a), the traditional Z-source inverter (ZSI) consists of two separate inductors (L_1, L_2), two capacitors (C_1, C_2), and an input diode D_{in} which are cascaded between VSI bridge and input supply [41]. The use of input diode D_{in} allows the boosting of voltage and prevents the reverse current flow. Moreover, due to input diode D_{in}, the ZSI provides discontinuous input current. In addition, the traditional ZSI does not share common ground with source and inverter, provides huge inrush current at start-up condition, and high stress across the capacitors.

Therefore, to reduce the capacitor voltage stress and inrush current at start-up condition with same number of passive and active components, the improved Z-source inverter was proposed in [45] and is shown in Fig. 2.2(b) in which the input supply, impedance network, and the VSI bridge are connected in series configuration.

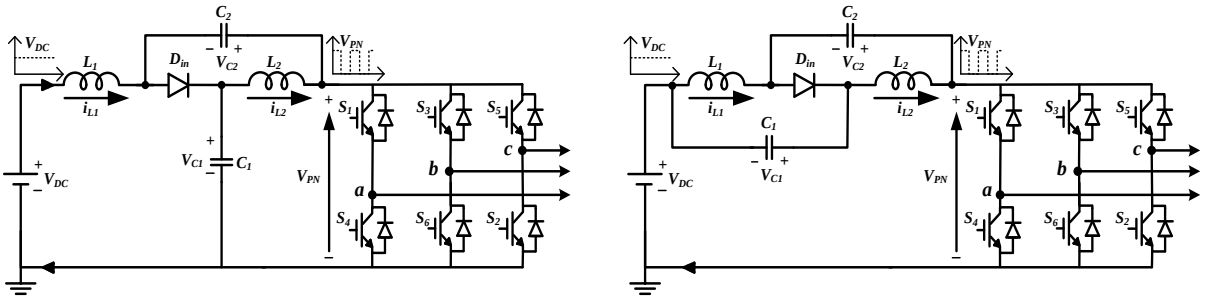


(a) (b)

Fig. 2.2: Schematic diagram of: (a) Z-source inverter; (b) improved Z-source inverter.

In 2008, the quasi-ZSIs (qZSIs) have been presented in four different configurations [43]. The two configurations of the qZSIs, namely continuous and discontinuous configurations of qZSIs are shown in Fig. 2.3(a), and Fig. 2.3(b) respectively. Similar to improved ZSI [45], these topologies reduce the stress across the capacitors and starting inrush current. Therefore, lower rating capacitors can be used which reduces the cost, space, and weight of the system. Moreover, these topologies provide continuous input current and shares common ground with the supply and inverter bridge. The number of components used, stress across switch, and the boost factor of the qZSIs [43] is same as that of the traditional ZSI [41] and improved-ZSI [45]. All these Z-network topologies [41, 43, and 45] can boost the voltage to the desired value in single-stage with improved reliability. The expression for boost factor of all these four topologies and the traditional ZSI/IZSI is given as

$$B = \frac{1}{1-2D_0} \tag{2.1}$$



(a) (b)

Fig. 2.3: Configuration of: (a) continuous; (b) discontinuous input current quasi Z-source inverters.

The major factor is the actual physical gain produced by the Z-source inverter. Theoretically, the boost factor can be increased to any desired value without any upper limit. But, due to the presence of the parasitic influences generally lowers the attainable gain to a finite value. For example, to increase the boost factor/output voltage, the duty cycle of the shoot-through (ST) state must be increased; as a result, the voltage stress on the switches of the inverter bridge increases. In addition, the output voltage waveforms deteriorate.

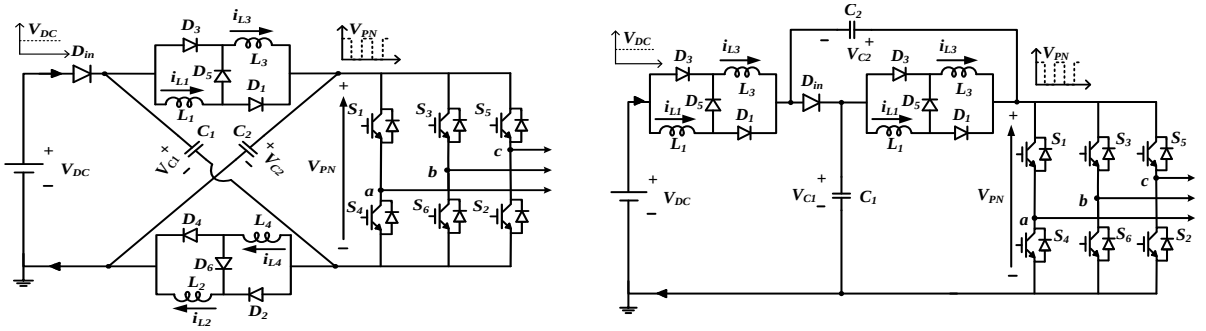


Fig. 2.4: Illustration of: (a) switched-inductor Z-source inverter; (b) two switched-inductor quasi Z-source inverters.

2.3.2 Switched-Inductor "Z"/ "Quasi-Z"- Source Inverters

In order to enlarge the boost factor, the two inductors (L_1, L_2) of traditional ZSI [41] shown in Fig. 2.2(a) is replaced with two switched-inductor (SL) cells and was named as SL-ZSI [49] as shown in Fig. 2.4(a), where each SL cell is composed of three diodes and two inductors. The combinations of L_1–D_1–L_3–D_3–D_5 acts as top SL cell and the combinations of L_2–D_2–L_4–D_4–D_6 acts as bottom SL cell for SL-ZSI. Even though the boost factor was increased with increased number of (i.e., both passive and active) components; the drawbacks of the SL-ZSI was same as the traditional ZSI.

Therefore, to avoid those drawbacks, the two-SL-qZSI was proposed in [51] with same number of components and is depicted in Fig. 2.4(b). The switch stress and the boost factor of SL-ZSI [49] and rSL-qZSI [51] are same for a given shoot-through duty ratio D_0 and input voltage. For the same voltage boost, the SL-qZSI has lower capacitor stress and low inrush current at start-up condition. In addition, it shares common ground with the source and inverter. The boost factor expression of SL-ZSI and rSL-qZSI shown in Fig. 2.4 is given as

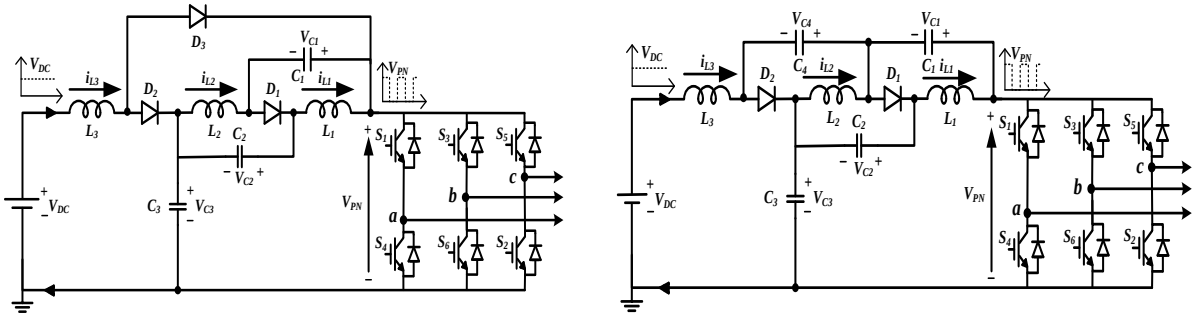
$$B_{SL} = \frac{1+D_0}{1-3D_0} \tag{2.2}$$

2.3.3 Diode/ Capacitor-Assisted Quasi Z-Source Inverters

The boost factor can be improved further with the addition passive and active components in the impedance network of qZSI [47] and is shown in Fig. 2.5. The two configurations namely, diode-assisted (DA) and capacitor-assisted (CA) qZSIs are depicted in Fig. 2.5(a) and Fig. 2.5(b) respectively. But, the number of inductors and diodes used in DA/CA-qZSI is less when compared to SL-ZSI. To enhance the boost factor further, another stage can be cascaded at the front end. The boost factor of CA-qZSI (B_{CA}) is more that of DA-qZSI (B_{DA}) and are given as

$$B_{CA} = \frac{1}{1-3D_0} \tag{2.3}$$

$$B_{DA} = \frac{1}{(1-2D_0)(1-D_0)} \tag{2.4}$$



(a) (b)

Fig. 2.5: Illustration of: (a) diode-assisted; (b) capacitor-assisted quasi Z-source inverters.

2.3.4 Active Impedance (Z)-Source Inverters

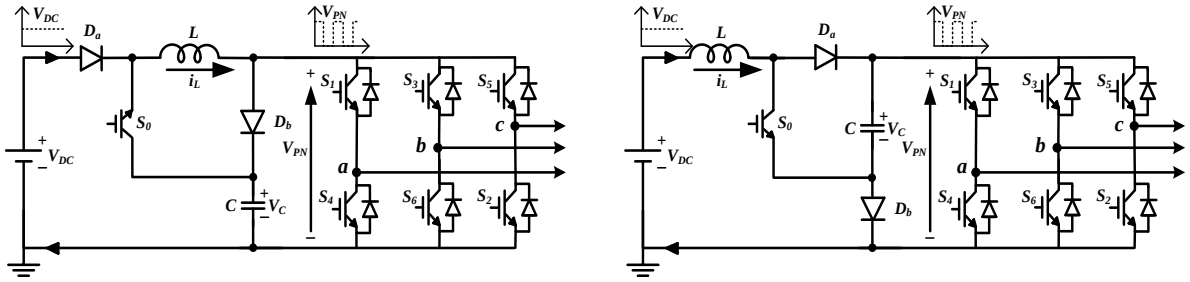
The traditional ZSI [41] uses two pair of *LC* (inductor, capacitor) components which increases the cost, volume, and space requirements and can make it unsuitable for low power application. Therefore, the switched-boost inverter (SBI) was proposed in [59] and is shown in Fig. 2.6(a) with only one pair of *LC* components but with an extra active switch S_0 and one diode. The boost factor of the SBI can be expressed as

$$B_{SBI} = \frac{1-D_0}{1-2D_0} \tag{2.5}$$

The main drawback of SBI is it provides discrete input current due to input diode D_a with less boost factor and the voltage stress across capacitor is equal to the dc-link voltage peak. Therefore, to increase the boost factor and to get continuous input current from the supply with same number of components, the current fed switched inverter (CFSI) was proposed and is shown in Fig. 2.6(b), but the voltage stress

across capacitor is equal to the dc-link voltage [61]. This CFSI combines the high boost property of ZSI [41] as well as lower passive component count of SBI [59]. The boost factor or voltage boost of traditional ZSI and CFSI is same and is expressed as follows;

$$B_{CSFI} = \frac{1}{1-2D_0} \tag{2.6}$$



(a) (b)

Fig. 2.6: Illustration of: (a) switched boost inverter; (b) current fed switched inverter.

2.3.5 L - Z-Source Inverter

To increase the boost factor and decrease the inrush current problem, the L-Z-source inverter (L-ZSI) was proposed in [70] with only diodes and inductors (which forms switched-inductor cell) and without any capacitors in the impedance network. This topology provides common ground with source and inverter. Moreover, it prohibits the inrush current problem at start-up.

The circuit diagram of L-ZSI is depicted in Fig. 2.7. The expression for boost factor in case of *n* - number of inductors in the Z-network of switched-inductor cell is given as

$$B_{L-ZSI} = \frac{1+(n-1)D_0}{1-D_0} \tag{2.7}$$

The boost factor of L-ZSI can be adjusted with the variation in shoot-through duty ratio and switched-inductor (SL) cells. The multiple SL cells in this topology cause lower efficiency and higher volume and weight.

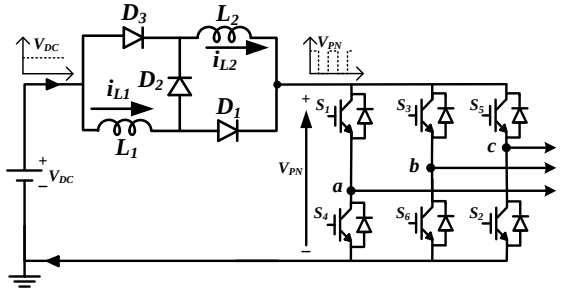


Fig. 2.7: Circuit diagram of L- Z-source inverter.

2.3.6 Enhanced-Boost Z-Source Inverter

To further enhance the boost factor, the enhanced-boost Z-source inverter (EB-ZSI) was proposed, in which the impedance network is consists of two switched-impedance (SI) cells and is shown in Fig. 2.8, where each SI cell is composed of two diodes, two capacitors and two inductors [73]. The main objective of this topology is the use of the high number of elements with low rating instead of using a low number of elements with high rating in a way that tolerate high voltages in high voltage gains. The combination of L_1–L_3–D_1–D_3–C_1–C_3 acts as one (top) SI cell and the combination of L_2–L_4–D_2–D_4–C_2–C_4 acts as another (bottom) SI cell. A very small shoot-through duty ratio was required to get the high boost factor at high modulation index which improves the output voltage quality and THD. The EB-ZSI provides very strong boost factor among all the non-coupled-inductor topologies and the expression for boost factor is expressed as

$$B_{EB-ZSI} = \frac{1}{1-4D_0+2D_0^2} \tag{2.8}$$

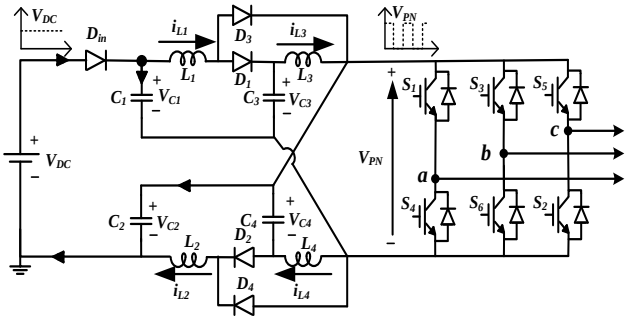


Fig. 2.8: Enhanced-boost ZSI with two switched-impedance network.

Even though the boost factor is increased with reduced switch stress, the enhanced-boost ZSI [73] has the drawbacks similar to the traditional ZSI [41]. Therefore to avoid these drawbacks, the authors have presented various configurations, which will be discussed in later chapter of this thesis.

2.4 Boost Factor and Switch Stress Comparison of Different Existing Topologies

Fig. 2.9 shows the boost factor comparison of all the existing non-coupled based inverter topologies. Table 2.1 compares the boost factor, capacitor stress, nature of input current, and the number of components used in the different non-coupled based inverter topologies which are discussed in this chapter.

The voltage stress across power semiconductor devices can be defined as the ratio of the peak dc-link voltage ($\hat{V}_{PN}$) to the minimum DC voltage (GV_{DC}) needed by the traditional ZSI to produce the same AC output voltage at M = 1 [22]. Fig. 2.10

depicts the stress across the semiconductor switches of the different existing non-coupled based topologies. From this figure, it can be observed that the EB-ZSI [73] is having less stress across the switch for same given voltage conversion ratio *G* when compare to the other existing topologies. Even though the EB-ZSI uses more number of elements in the impedance network, but the stress across them is less.

Table 2.1: Comparison of different non-coupled based inverter topologies.

S.No	Topology	Boost Factor	Capacitor Stress	Input Current Nature	Components			
					L	C	D	S
1	ZSI [41]	$\frac{1}{1-2D_0}$	$\frac{V_{C1,C2}}{V_{DC}}=\frac{1-D_0}{1-2D_0}$	Discontinuous	2	2	1	6
2	qZSI [43]	$\frac{1}{1-2D_0}$	$\frac{V_{C1}}{V_{DC}}=\frac{1-D_0}{1-2D_0}$, $\frac{V_{C2}}{V_{DC}}=\frac{D_0}{1-2D_0}$	Continuous	2	2	1	6
3	qZSI [43]	$\frac{1}{1-2D_0}$	$\frac{V_{C1,C2}}{V_{DC}}=\frac{D_0}{1-2D_0}$	Discontinuous	2	2	1	6
4	IZSI [45]	$\frac{1}{1-2D_0}$	$\frac{V_{C1,C2}}{V_{DC}}=\frac{D_0}{1-2D_0}$	Discontinuous	2	2	1	6
5	SL-ZSI [49]	$\frac{1+D_0}{1-3D_0}$	$\frac{V_{C1,C2}}{V_{DC}}=\frac{1-D_0}{1-3D_0}$	Discontinuous	4	2	7	6
6	rSL-qZSI [51]	$\frac{1+D_0}{1-3D_0}$	$\frac{V_{C1}}{V_{DC}}=\frac{1-D_0}{1-3D_0}$, $\frac{V_{C2}}{V_{DC}}=\frac{2D_0}{1-3D_0}$	Continuous	4	2	7	6
7	DA-qZSI [47]	$\frac{1}{(1-2D_0)(1-D_0)}$	$\frac{V_{C1,C2}}{V_{DC}}=\frac{D_0}{(1-2D_0)(1-D_0)}$ $\frac{V_{C3}}{V_{DC}}=\frac{1}{(1-D_0)}$	Continuous	3	3	3	6
8	CA-qZSI [47]	$\frac{1}{1-3D_0}$	$\frac{V_{C1,C2,C4}}{V_{DC}}=\frac{D_0}{(1-3D_0)}$ $\frac{V_{C3}}{V_{DC}}=\frac{1-2D_0}{(1-3D_0)}$	Continuous	3	4	2	6
9	SBI [59]	$\frac{1-D_0}{1-2D_0}$	$\frac{V_C}{V_{DC}}=\frac{1-D_0}{1-2D_0}$	Discontinuous	1	1	2	7
10	CFSI [61]	$\frac{1}{1-2D_0}$	$\frac{V_C}{V_{DC}}=\frac{1}{1-2D_0}$	Continuous	1	1	2	7
11	L-ZSI [70]	$\frac{1+(n-1)D_0}{1-D_0}$	Not Applicable	Continuous	2	0	3	6
12	EB-ZSI [73]	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{V_{C1,C2}}{V_{DC}}=\frac{(1-D_0)^2}{1-4D_0+2D_0^2}$	Discontinuous	4	4	5	6

where, L – the number of inductors, C – is the number of capacitors, and D – is the number of diodes used in the impedance network, and S – is the number of semiconductor switches.

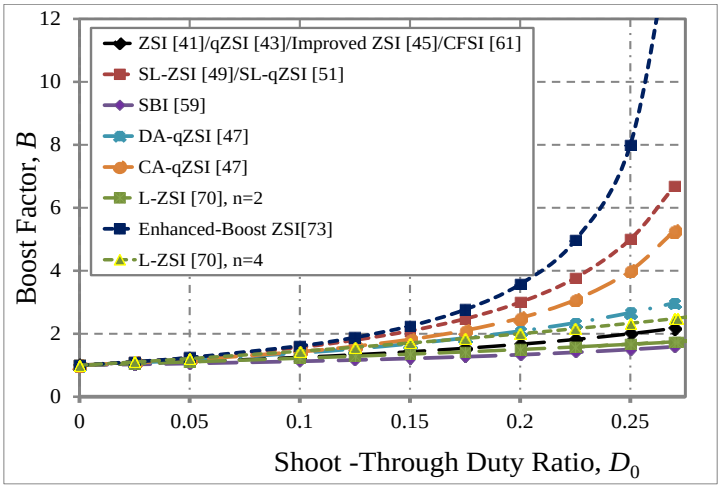


Fig. 2.9: Boost factor versus shoot-through duty ratio of different topologies.

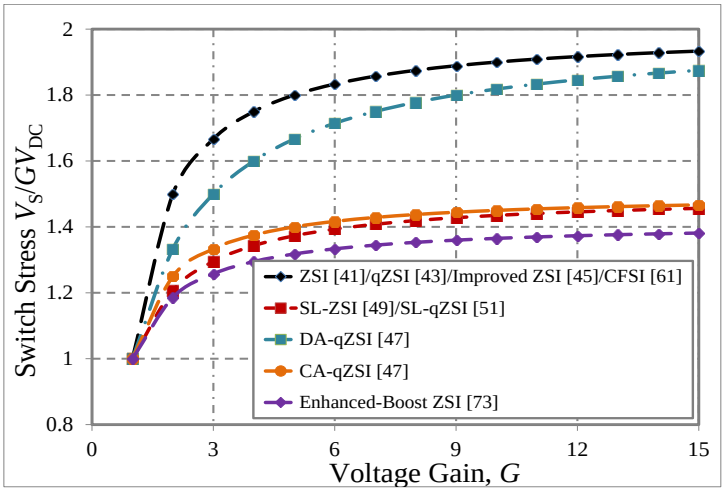


Fig. 2.10: Switch versus voltage gain of different topologies.

All the topologies discussed in this section is based on the non-coupling inductors and in order to increase the boost factor, the components in the impedance network has to be increased which increases the size, volume, cost, and space requirements of the system.

Therefore, the coupled inductor based topologies have been discussed in next section with less number of components in the impedance network to improve the boost factor which was addressed in [75 – 97].

2.5 Magnetically Coupled based Z-Source Network Topologies

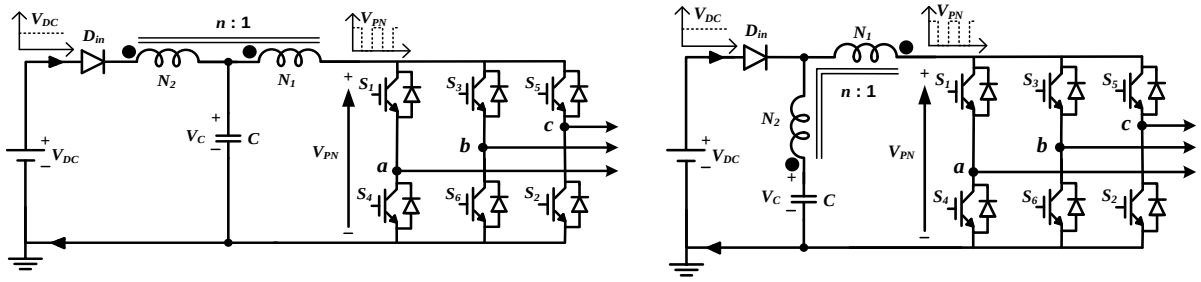
To enhance the boost factor further, many magnetically coupled impedance source (MCIS) inverters with less number of elements were proposed in literature [75 – 97]. Depending on their components used in the impedance network, these MCIS networks are broadly classified in following three categories, namely two winding MCIS [75 – 88], three winding MCIS [89 – 93], and active MCIS networks [94 – 96].

2.5.1 Two-winding Magnetically Coupled Impedance Source (MCIS) Networks

The two winding MCIS networks are again broadly categorized in two types based on the number of components used, namely with less number of components and with more number of components.

2.5.1.1 With Less Number of Components

In this category, the impedance network is having only one capacitor (*C*), one diode (D_{in}), and one two-winding coupled inductor/transformer with their turn's ratio *n*. In order to increase the boost factor and to improve the performance of the inverter, many topologies were discussed in [75 – 78] with same number of elements.



(a) (b)

Fig. 2.11: Configuration of: (a) trans-Z-source inverter; (b) Γ-Z-source inverter.

The four configurations of trans-Z-source inverters (trans-ZSI) were presented in [75]. Out of four configurations only one configuration is shown in Fig. 2.11(a) and the expression for boost factor is as follows

$$B_{T-ZSI} = \frac{1}{1-(n+1)D_0} \tag{2.9}$$

where $n = N_2/N_1 \geq 1$ is the turns ratio of the transformer. If $n = 1$ then the boost factor *B* of trans-ZSI is same as the traditional ZSI [41].

It is clearly observed from (2.9) and Fig. 2.12(a), that the boost factor can be increased with increase in turn's ratio *n*. At high boost factor, the turn's ratio becomes very high which increases the cost and space. Therefore, it is difficult to implement this inverter for high power applications where transformers have to design with high leakage inductance which results in overshoot in the peak dc-link voltage as well as across the switch.

Next, the Γ-Z-source inverter (Γ-ZSI) was proposed in [78] in line with previous topology with same number of components in the impedance network but with some rearrangement as depicted in Fig. 2.11(b) and the boost factor can be raised by lowering the transformer turn's ratio *n* rather than increasing it. Therefore, at high

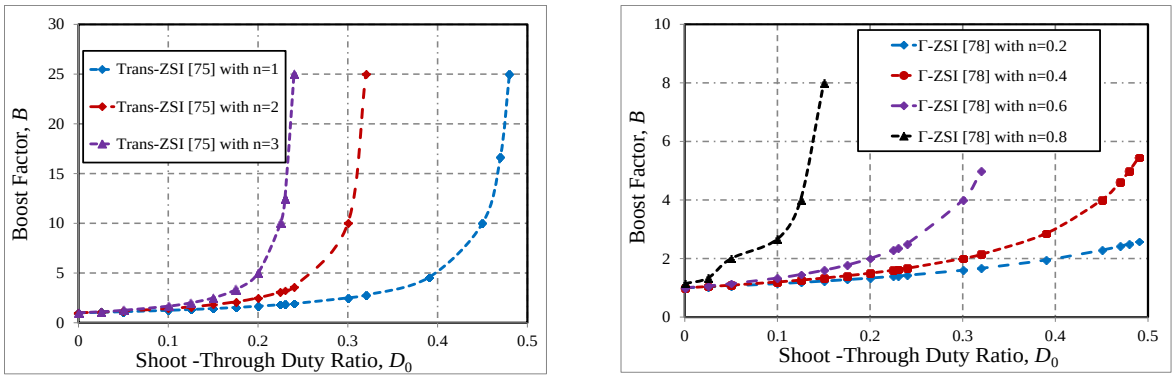
boost factor, this topology requires very less turns ratio *n* which in turn reduces the weight, volume, cost, and space requirement of the system.

The boost factor of Γ-ZSI can be expressed as

$$B_{\Gamma-ZSI} = \frac{1}{1-\left(1+\frac{1}{n-1}\right)D_0} \tag{2.10}$$

where *n* is the transformer turn's ratio of Γ-ZSI.

The boost factor plot of trans-ZSI and Γ-ZSI is depicted in Fig. 2.12 for varying shoot-through duty ratio and turn's ratio.

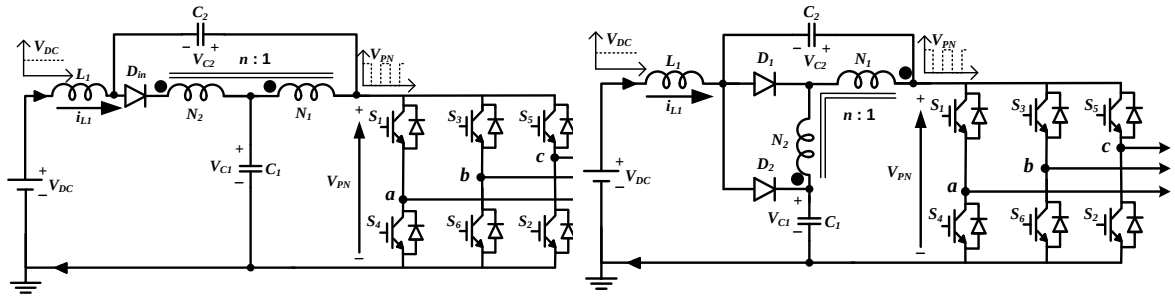


(a) (b)

Fig. 2.12: Boost factor comparison of: (a) trans-Z-source inverter; (b) Γ-Z-source inverter.

2.5.1.2 With More Number of Components

In this category, the impedance network is having more than one capacitor and diode, and one two-winding coupled inductor and were discussed in the literature [79 – 85]. In order to increase the boost factor and to improve the performance of the inverter, many topologies were presented in [79 – 85].



(a) (b)

Fig. 2.13: Circuit configuration of: (a) improved trans-Z-source inverter; (b) improved Γ-ZSI.

Fig. 2.13(a) shows the improved trans-ZSI modified from trans-ZSI with the addition of capacitor C_2 and inductor L_1 to have continuous input current and higher

boost factor than the trans-ZSI [84]. In addition, this topology suppresses the inrush current and improves the input current profile.

The boost factor of improved trans-ZSI is expressed as

$$B_{\text{ImpT}-ZSI} = \frac{1}{1-(2+n)D_0} \tag{2.11}$$

If n = 0 then the boost factor B of improved trans-ZSI is same as the traditional ZSI [41].

Fig. 2.13(b) shows the improved Γ-ZSI modified from the Γ-ZSI with the addition of inductor L_1 and capacitor C_2 to have continuous input current and higher voltage gain [85]. The additional clamping diode D_C or D_2 clamps the dc-link voltage. For the suppression of voltage overshoot caused by the leakage inductance of coupled inductor, the additional clamping diode D_C or D_2 is used. This additional clamping diode D_C also improves the efficiency of the inverter slightly [99]. The boost factor of the improved Γ-ZSI is given as

$$B_{\text{ImpΓ}-ZSI} = \frac{(n-1)}{[n(1-2D_0)-1+D_0]} \tag{2.12}$$

The boost factor curve for Improved Trans-ZSI and Improved Γ-ZSI is shown in Fig. 2.14. It can be inferred that the improved Γ-ZSI provides higher boost at a particular turns ratio and D_0 compared to improved Trans-ZSI counterpart.

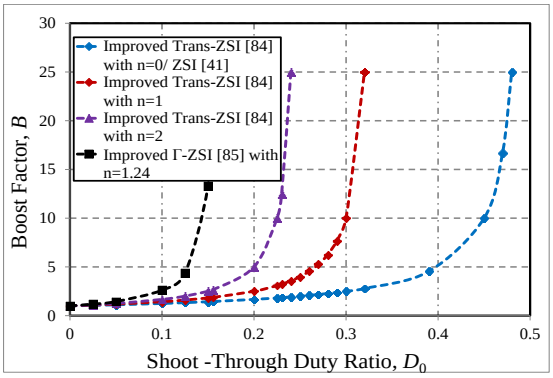


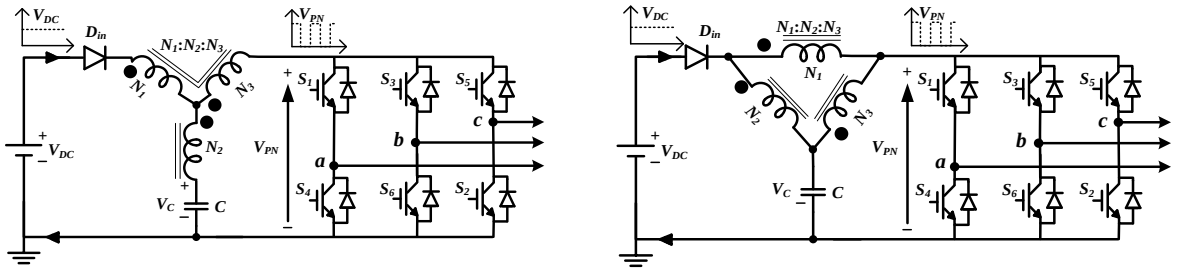
Fig. 2.14: Boost factor comparison for Improved trans-Z-source inverter and Improved Γ-Z-source inverter.

2.5.2 Three-winding Magnetically Coupled Impedance Source (MCIS) Networks

In This section, it deals with three winding coupled inductors to achieve higher voltage gain and was presented in [89 – 93].

2.5.2.1 With Less Number of Components

In this section, the impedance network is consists of only one diode D_{in}, one capacitor C, and one three winding transformer as presented in [89, 90].



(a) (b)

Fig. 2.15: Circuit diagram of: (a) Y-source inverter; (b) Δ-source impedance network.

The Y-source inverter (YSI) has been presented in [89] and is depicted in Fig. 2.15(a). The Y-source inverter has more degrees of freedom for setting the voltage gain and modulation index than other classical impedance-source networks. Due to input diode D_{in}, it provides discrete input current.

The expression for the boost factor of Y-source inverter is given as

$$B_Y = \frac{1}{1 - K_Y D_0} \tag{2.13}$$

where, $K_Y = \dfrac{N_3 + N_1}{N_3 - N_2}$ is the turn's ratio of the transformer.

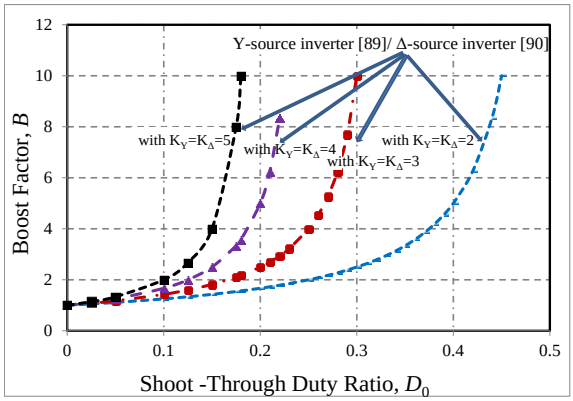


Fig. 2.16: Boost factor comparison for Y-source inverter and Δ-source inverter.

The Δ-source network was proposed in [90] with same number of component as that of the Y-source network but with rearrangement of components in the impedance network and is shown in Fig. 2.15(b). The Δ-source converter offers smaller winding losses and magnetizing current compared to the Y-source network. Similar to Y-source network, the Δ-source converter provides discrete input current and shares common ground with the source and inverter. In addition, with this Δ-connected configuration, the adverse effect of leakage inductance on dc-link rail is significantly reduced. The boost factor for the Δ-source network is expressed as

$$B_\Delta = \frac{1}{1 - K_\Delta D_0} \tag{2.14}$$

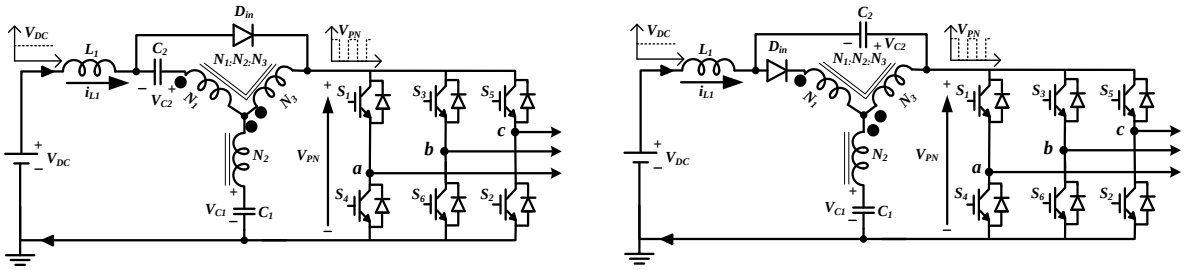
where, $K_\Delta = \frac{N_1}{N_3}$ is the turn's ratio of the transformer.

The boost factor plot for Y-source inverter [89] and Δ -source inverter [90] is shown in Fig. 2.16 for a particular K_Y/K_Δ (where K_Y/K_Δ is deifined as above) and shoot-through duty ratio D_0.

2.5.2.2 With More Number of Components

The above discussed three winding coupled networks provides discrete input current [89, 90] which are not suitable solar photovoltaic (SPV) applications to track maximum power. Therefore, many other topologies were presented in the literature [91 – 93] to avoid the aforementioned drawbacks.

To get continuous input current, one extra input inductor L_1, and capacitor C_2 is added to conventional Y-source network [91, 93] and is shown in Fig. 2.17. With the addition of inductor and capacitor, the boost factor of the topology is also increased.



(a) (b)

Fig. 2.17: Circuit diagram of: (a) quasi-Y-source inverter; (b) improved Y-source inverter.

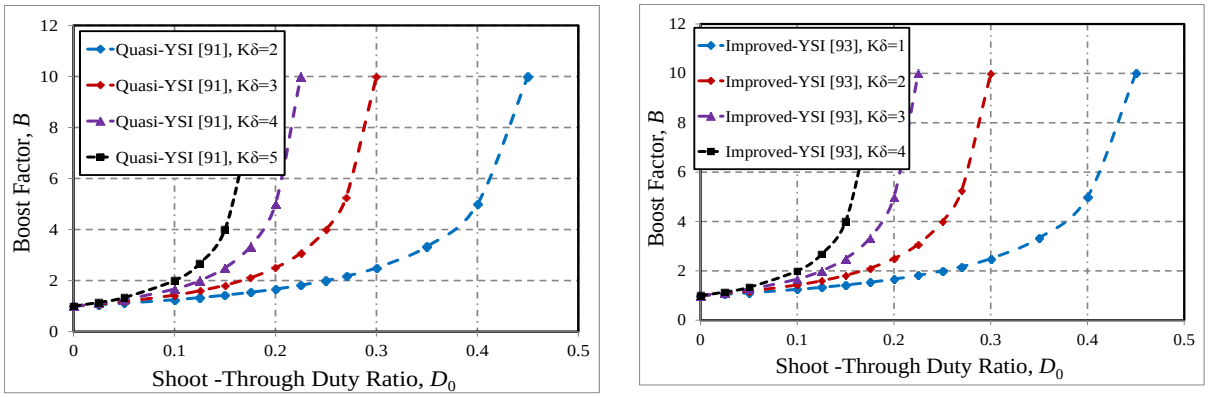
Fig. 2.17(a) and Fig. 2.17(b) show the quasi Y-source [91] and improved Y-source inverters [93] respectively; which inherits all advantages of the original Y-source network counterparts [89]. In addition to this, the quasi/improved Y-source inverter provides continuous input current, reduced source stress, suppresses the starting inrush current problem, and lower component ratings when compared to the traditional Y-source network [89]. Moreover, its two capacitors are placed such that they block dc current from flowing through the coupled inductor, and hence preventing its core from saturation. Boost factor of the quasi Y-source and improved Y-source inverter respectively is given as

$$B_{quasiY} = \frac{1}{1 - K_\delta D_0} \tag{2.15}$$

$$B_{impY} = \frac{1}{1 - (1 + K_\delta) D_0} \tag{2.16}$$

where, $K_\delta = \dfrac{N_2 + N_1}{N_2 - N_3}$ is the winding factor of the transformer.

The boost factor plot of qYSI [91] and improved YSI [93] is shown in Fig. 2.18(a) and (b) respectively for winding factor K_δ = 1, 2, 3, 4 which shows that the boost factor at a particular D_0 increases with the increase in winding factor K_δ.

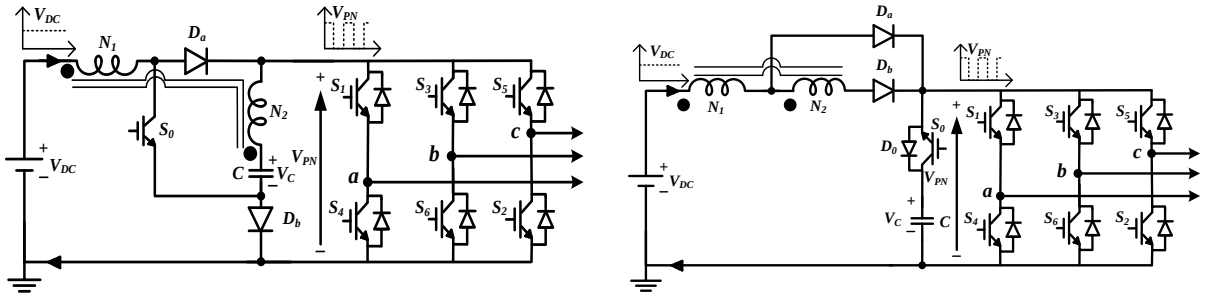


(a) (b)

Fig. 2.18: Boost factor comparison of: (a) quasi-Y-source inverter; (b) improved-Y-source inverter.

2.5.3 Active Magnetically Coupled Impedance Source (MCIS) Networks

In this section, active magnetically coupled impedance source (MCIS) networks are discussed which consists of one extra active switch S_0 in the impedance network in addition to passive components and diodes [94 – 96]. The circuit configurations consist of two diodes (D_a, D_b), one capacitor C, one coupled inductor, and one active switch S_0. Shoot-through duty cycle D_0 is applied to the active switch S_0. Therefore, the voltage gain/ dc-link voltage can be regulated by turn's ratio n and D_0.



(a) (b)

Fig. 2.19: Illustration of coupled-inductor: (a) high boost switched inverter;

(b) L-source inverter (CL-LSI).

The high-boost switched inverter shown in Fig. 2.19(a) was presented in [94], which needs even narrower turns-ratio range ($0 \le n < 1$) to achieve high voltage boost. The variation of the boost factor with different duty ratio and turns ratio n is

shown in Fig. 2.20. Moreover, the current drawn from the supply is continuous and it also shares common ground with source, which is best suitable for solar PV applications. The boost factor expression is given as

$$B_{\text{Imp.T-CFSI}} = \frac{1-n}{1-n-2D_0} \tag{2.17}$$

where, $n = N_2/N_1$ is the turn's ratio of the coupled inductor.

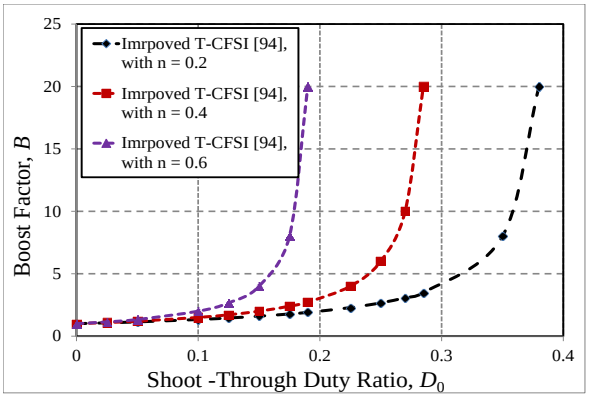


Fig. 2.20: Comparisons of boost factor for Improved Trans-CFSI.

The above discussed impedance source inverters improve the performances of traditional ZSI [41], but the current existing inverters [41 – 95] all have a common drawback: the inductor current cannot be discontinuous. If the inductor currents of the inverters enter discontinuous conduction mode, it will make dc-link voltage drop to influence output waveform, and disconnect impedance source networks with load.

The coupled-inductor L-source inverter (CL-LSI) was presented in [96] and is shown in Fig. 2.19(b). This CL-LSI uses an auxiliary switch S_0 with an anti paralleled diode D_0 in series with a storage capacitor C and coupled-inductor cell with turn's ratio n to form an L-shape network and the boost factor for continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is given as

$$B_{CCM} = \frac{1+nD_0}{1-D_0} \tag{2.18}$$

$$B_{DCM} = \frac{1+nD_0-D_2}{1-D_0-D_2} \tag{2.19}$$

The CL-LSI topology has the following advantages over other topologies [96]:

1. The CL-LSI can flexibly work in DCM and CCM, and solve the dc-link voltage drop while the coupled-inductor cell works in DCM.
2. Compared to CCM, the CL-LSI in DCM can produce the higher voltage gain, reduce the voltage stresses across passive components and lower the coupled-inductor values and power losses.

3. Realizing the common ground to reduce the electromagnetic interference.
4. Suppresses the inrush current at startup condition.

Table 2.2: Comparison of different coupled inductor based inverter topologies

S.No	Topology	Boost Factor	Capacitor Stress	Nature of Input Current	Components				
					L	C	D	S	L_C
1	Trans-ZSI [75]	$\frac{1}{1-(n+1)D_0}$	$\frac{V_C}{V_{DC}}=\frac{1-D_0}{1-(n+1)D_0}$	Discontinuous	0	1	1	6	1
2	Γ-ZSI [78]	$\frac{1}{1-\left(1+\frac{1}{n-1}\right)D_0}$	$\frac{V_C}{V_{DC}}=\frac{1-D_0}{1-\left(1+\frac{1}{n-1}\right)D_0}$	Discontinuous	0	1	1	6	1
3	Improved Trans-ZSI [84]	$\frac{1}{1-(2+n)D_0}$	$\frac{V_{C1}}{V_{DC}}=\frac{1-D_0}{1-(2+n)D_0}$ $\frac{V_{C2}}{V_{DC}}=\frac{1+D_0}{1-(2+n)D_0}$	Continuous	1	2	1	6	1
4	Improved Γ-ZSI [85]	$\frac{(n-1)}{[n(1-2D_0)-1+D_0]}$	$\frac{V_{C1}}{V_{DC}}=\frac{(1-D_0)(n-1)}{[n(1-2D_0)-1+D_0]}$ $\frac{V_{C2}}{V_{DC}}=\frac{nD_0}{[n(1-2D_0)-1+D_0]}$	Continuous	1	2	2	6	1
5	YSI [89]	$\frac{1}{1-K_Y D_0}$	$\frac{V_C}{V_{DC}}=\frac{1-D_0}{1-K_Y D_0}$	Discontinuous	0	1	1	6	1
6	ΔSI [90]	$\frac{1}{1-K_\Delta D_0}$	$\frac{V_C}{V_{DC}}=\frac{1-D_0}{1-K_\Delta D_0}$	Discontinuous	0	1	1	6	1
7	Quasi-YSI [91]	$\frac{1}{1-K_\delta D_0}$	$\frac{V_{C1}}{V_{DC}}=\frac{1-D_0}{1-K_\delta D_0}$, $\frac{V_{C2}}{V_{DC}}=\frac{\left(\frac{N_1+N_3}{N_2-N_3}\right)D_0}{1-K_\delta D_0}$	Continuous	1	2	1	6	1
8	Improved -YSI [93]	$\frac{1}{1-(1+K_\delta)D_0}$	$\frac{V_{C1}}{V_{DC}}=\frac{\delta D_0}{1-(1+K_\delta)D_0}$, $\frac{V_{C2}}{V_{DC}}=\frac{1-D_0}{1-(1+K_\delta)D_0}$	Continuous	1	2	1	6	1
9	Improved CFSI [94]	$\frac{1-n}{1-n-2D_0}$	$\frac{V_C}{V_{DC}}=\frac{1-n+2nD_0}{1-n-2D_0}$	Continuous	0	1	2	7	1
10	CL-LSI [96]	$\frac{1+nD_0}{1-D_0}$	$\frac{V_C}{V_{DC}}=\frac{1+nD_0}{1-D_0}$	Continuous	0	1	2	7	1

Note: L_C – is the number of coupled inductors used in the impedance network.

Table 2.2 compares the boost factor, capacitor stress, nature of input current, and the number of components (i.e., both passive and active) used in the different coupled inductor based inverter topologies which are discussed in this section.

2.5.4 Effect of Leakage Inductances on Magnetically Coupled Impedance Source (MCIS) Networks

As discussed in the above subsections, the magnetically coupled (MCIS) based inverter topologies are used to get high voltage boost at low shoot-though duty ratios with less number of components [75 – 97] and at high modulation index. But, their magnetic coupling must be strong or their leakage inductance must be small enough. Otherwise huge voltage spikes will appear across the dc-link/switches. Therefore, the switching device has to design for higher voltage rating which increases the cost of the semiconductor switching devices [98]. The clamping diode was used to avoid the severe over voltage spikes which appear across the dc-link [99]. The analysis of inrush current during switching operation is elaborated in [158, 159].

For the suppression of voltage overshoot caused by the leakage inductance of coupled inductor, the additional clamping diode D_C was used. Moreover, this additional clamping diode D_C improves the efficiency of the inverter slightly [99].

2.6 Ideal Characteristics of High Boost Impedance (Z)-Source Network Topologies

Based on the comparative discussion in the previous section of this chapter, several operating characteristics are listed in this section which can be treated as ideal characteristics of high boost impedance network inverter topologies. These characteristics are as follows:

1. It should provide single-stage DC-to-AC power conversion.
2. It should possess high voltage boost inversion capability at low shoot-through duty ratio D_0.
3. It should possess good electromagnetic interference (EMI) noise immunity.
4. It should have high reliability.
5. It should draw continuous input current making it suitable for renewable application without the necessity of using input filter.
6. It should produce low voltage spikes across the switching devices.
7. It should not require extreme shoot-through duty ratio operation to achieve high voltage boost
8. It should not require dead-band circuit for the switching the semiconductor devices so that waveform distortion is avoided and hence total harmonic distortion (THD) is improved.
9. It should not have any dynamic stability related problems.

2.7 Conclusion

In this Chapter, both coupled and non-coupled inductor based Z-source network inverter topologies are discussed including their advantages and disadvantages. In case of non-coupled inductor based topologies, to increase the boost factor and to reduce the switch stress, the components (both passive and active) used in the impedance network of inverters are increased which increases the size, cost, and volume of the system. Each topology has its own advantages and disadvantages. Depending on the users requirement any of the topology can be used.

In case of coupled inductor based topologies, to increase the boost factor and to reduce the switch stress, the less number of components (both passive and active) are used in the impedance network when compared to non-coupled inductor based topologies. The boost factor can be varied easily with help of tappings. But, the magnetically coupled impedance source (MCIS) networks provides very huge peak in the dc-link voltage due leakage inductance in the coupled inductors. Therefore, high ratings of semiconductor devices need to be used which increases the cost.

In this chapter, manily discusses two topologies of Z-source inverter (ZSI) are presented namely, one switched-inductor Z-source inverter (One SL-ZSI) and one switched-inductor improved Z-source inverter (One SL-IZSI). These presented One SL-ZSI/ One SL-IZSIs topology are based on the traditional ZSI topology and adds only one inductor and three diodes. Similar to SL-qZSI, these presented topologies provides same voltage boost/ voltage gain with same number of elements. Moreover, the proposed One SL-IZSI can suppress inrush current at start-up, which might destroy the switching devices and reduces the capacitor stress. The operating principle, boost factor and voltage gain derivation, parameter design and comparison analysis is carried out for the one switched-inductor improved Z-source inverter (One SL-IZSI) topology. The theoretical analysis of the presented topology is also validated with the simulation results in MATLAB/Simulink.

3.1 Introduction

The Z-source inverter (ZSI) was proposed in [41] by F.Z. Peng mainly to overcome the drawbacks of the traditional single-stage voltage source inverter (VSI) and two-stage power conversion systems. The conventional ZSI is also has certain drawbacks. To avoid those drawbacks, quasi-ZSIs (qZSIs) [43] and improved ZSI [45] were proposed in 2008 and 2009 respectively having same boost factor capability as that of the ZSI. To enhance the boost factor/ voltage gain, the switched-inductor ZSI (SL-ZSI) and SL-qZSIs were presented in [49] and [50, 51] respectively but with more elements in the impedance network. Later, to improve the performance of SL-ZSI, the SL-qZSI was proposed in 2011 [50]. The configuration of One SL-qZSI is depicted in Fig. 3.1. The SL-qZSI shown in Fig. 3.1 is based on the well-known qZSI topology and adds only one inductor and three diodes [50]. The boost factor expression of the SL-qZSI is as follows

$$B = \frac{1+D_0}{1-2D_0-D_0^2} \tag{3.1}$$

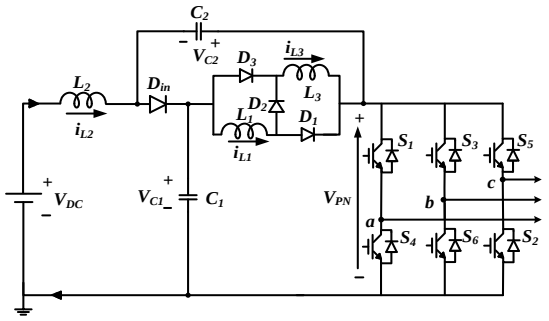


Fig. 3.1: Illustration of one switched-inductor quasi Z-source inverter.

Akin to SL-qZSI [50], this chapter proposes two more topologies which provide same boost factor/ voltage gain with same number of components (i.e., both passive and active) [52, 53]. From these two proposed topologies, the One SL- improved ZSI (One SL-IZSI) is having more advantages for the same boost factor and same number of elements. Therefore, in this chapter, the One SL-IZSI topology is taken an example for analysis and simulation. Similar to SL-qZSI, the One SL-IZSI topology reduces the capacitor stress and starting inrush current problem. Moreover, the One SL-IZSI may draw continuous input current from the supply if maximum boost control (MBC) technique is used [52].

This chapter presents the one switched-inductor “Z-source”/ “improved Z-source” inverter topologies to increase the boost factor to a required voltage level with the addition of one extra inductor and three diodes when compare to traditional ZSI [41]. The passive (L, C) and active (diodes) components used in the presented topologies is less than the SL-ZSI [49] and are more than that of the traditional ZSI, but is same as the SL-qZSI [50]. The boost factor and capacitor stress of the proposed topology are higher than the ZSI and is lower than the SL-ZSI. Both these topologies provide same boost factor for a given input voltage and shoot-through duty ratio with same number of components. The operating principle, boost factor derivation, theoretical analysis, and simulation of the proposed inverter topology are carried out in this chapter to validate the proposed topology.

This chapter is organized as follows. Section 3.2 describes the circuit configuration and their explanation. The steady-state operation and derivation of boost factor is explained in Section 3.3. Section 3.7 and Section 3.5 describes about starting inrush current and parameter design respectively. The extension of the proposed One SL-IZSI is elaborated in Section 3.6. The comparison of the proposed topologies and the existing topologies are made in Section 3.7. Finally, the theoretical analysis is validated with simulation results and their discussion is given in Section 3.8.

3.2 Circuit Diagrams and Explanation of the Proposed Topologies

As discussed in the introduction part of this chapter, the boost factor of the proposed topologies is same as the SL-qZSI [50] with same number of the elements in the impedance network. The circuit configuration of both the proposed topologies is depicted in Fig. 3.2 in which the impedance network consists of two capacitors (C_1, C_2), three inductors (L_1, L_2, and L_3) and four diodes (D_{in}, D_1, D_2, and D_3).

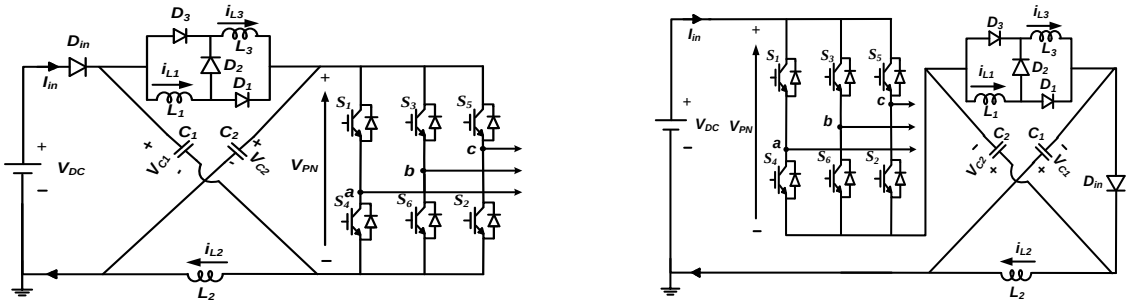


Fig. 3.2: Configuration of the presented topologies: (a) One SL-ZSI; (b) One SL-improved ZSI.

3.2.1 One Switched-Inductor Z-Source Inverter

As depicted in Fig. 3.2(a), the proposed inverter topology consists of two capacitors (C_1, C_2), three inductors (L_1, L_2, and L_3), and four diodes (D_{in}, D_1, D_2, and D_3). The combination of D_1–L_1–D_2–D_3–L_3 forms the one switched-inductor (SL) cell. The number of inductors and the diodes in the proposed topology is lower than the SL-ZSI [49] and is higher than the conventional ZSI [41]. Whereas, the number of capacitors are remains same.

3.2.2 One Switched-Inductor Improved Z-Source Network Inverter with Reduced Capacitor Stress

Similar to One SL-ZSI shown in Fig. 3.2(a), the One SL improved Z-source inverter also consists of two capacitors (C_1, C_2), three inductors (L_1, L_2, and L_3), and four diodes (D_{in}, D_1, D_2, and D_3) and is depicted in Fig. 3.2(b). Akin to One SL-ZSI, the numbers of inductors used in the presented topology are lower than the SL- ZSI [49] and are higher than the ZSI [41]. The diodes used in the presented topology are also lower than the SL-ZSI [49] and is higher than the ZSI [41]. Whereas, the number of capacitors are remains same when compared to ZSI and SL-ZSI. The number of passive (L, C) and active (diodes) components used in this topology is same as that of the SL-qZSI presented in [50].

In order to reduce the capacitor voltage stress, and to suppress the inrush current, the impedance network is connected in series with the dc voltage source and bridge inverter and is depicted in Fig. 3.2(b). This topology also shares common ground with the source and bridge inverter.

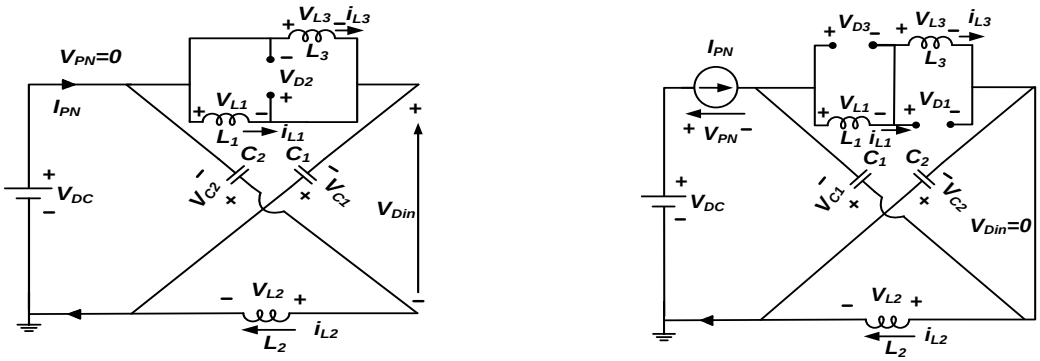
Both the configurations are having same number of components and produces same boost factor. The only differences between these topologies are that, the impedance network along with input diode D_{in} is cascaded in between input supply

and VSI in case of One SL-ZSI. Whereas, the impedance network is placed in series with the input supply and VSI bridge in the case of One SL-improved ZSI to reduce the stress across the capacitor and to suppress the inrush current at start-up condition. Moreover, One SL-improved ZSI shares common ground with source and inverter. Considering these advantages, the One SL-improved ZSI is used for the analysis in this chapter as an example and compares with other existing Z-source network topologies.

3.2.3 Advantages of One SL- Improved ZSI

The following are the main advantages of the One SL-improved ZSI whern compare to One SL-ZSI.

1. Shares common ground between input source and inverter.
2. Suppresses the starting inrush current problem due to circuit configurations.
3. May draw continuous input current form the source if maximum boost control method is used.
4. Results into less capacitor stress.



(a) (b)

Fig. 3.3: Illustration of One SL-improved ZSI in: (a) Shoot-through state; (b) Non-shoot-through state.

3.3 Principle of Operation and Analysis of One SL-IZSI

As discussed in above section, the one SL-improved ZSI is taken as the example for the analysis purpose and the configuration of One SL-IZSI is depicted in Fig. 3.2(b). Similar to traditional ZSI, the presented topology consist of seven shoot-through states and eight non-shoot-through states (i.e., six active states and two zero states) for the three-phase system. The equivalent circuits during shoot-through and non-shoot-through state are depicted in Fig. 3.3(a) and Fig. 3.3(b) respectively.

3.3.1 Shoot-Through State

As shown in Fig. 3.3(a), due to capacitor voltage ($V_{DC} < V_C$), the input diode D_{in} and diode D_2 are turned OFF in this state and whereas the diodes D_1 and D_3 are ON. The inductors L_1, L_2, and L_3 are charged from capacitors and input supply. The inductor current increases linearly during the period D_0. These inductors store the energy during this state. Remember that where D_0 represents the duty cycle ratio.

The following equations can be written across the inductors and diodes after applying Kirchhoff's voltage law (KVL) to Fig. 3.3(a).

$$\begin{cases} V_{L1} = V_{L3} = V_{DC} + V_{C1} \\ V_{L2} = V_{DC} + V_{C2} \end{cases} \tag{3.2}$$

$$\begin{cases} V_{Din} = -(V_{C1} + V_{C2} + V_{DC}) \\ V_{D2} = -(V_{C1} + V_{DC}) \end{cases} \tag{3.3}$$

and the dc-link voltage, $V_{PN} = 0$.

Similarly, the capacitor currents can be obtained as

$$\begin{cases} i_{C1} = -2i_{L1} \\ i_{C2} = 2i_{L1} - I_{PN} \end{cases} \tag{3.4}$$

3.3.2 Non-Shoot-Through State

The Illustration of the presented topology during the period (1- D_0) is shown in Fig. 3.3(b). The input diode D_{in} and diode D_2 are turned ON and whereas diodes D_1 and D_3 are OFF. The capacitors (C_1, C_2) are charged from input supply through the inductors. The inductor current decreases linearly during non-shoot-through state. The stored energy in these inductors and the input energy boost the input voltage to the required voltage levels.

After applying the KVL to Fig. 3.3(b), the equations across the inductors and diodes of the proposed inverter is as follows:

$$\begin{cases} V_{L1} = V_{DC} - V_{C2} - V_{L3} \\ V_{L2} = V_{DC} - V_{C1} \end{cases} \tag{3.5}$$

$$\begin{cases} V_{Din} = 0 \\ V_{D1} = V_{D3} = V_{L1\_\text{non-shoot}} \end{cases} \tag{3.6}$$

From (3.2) and (3.5), the following expression is obtained

$$\begin{cases} (V_{L1} = V_{L3})_{non-shoot} = \dfrac{D_0(V_{DC} + V_{C1}) + (1 - D_0)(-V_{C2})}{(1 - D_0)} \\ V_{L2} = -V_{C1} \end{cases} \tag{3.7}$$

In the same manner, applying Kirchhoff's current law (KCL) in the loop of Fig. 3.3(b), the capacitor and diode D_{in} currents can be written as

$$\begin{cases} i_{C1} = i_{L2} - I_{PN} \\ i_{C2} = i_{L1} - I_{PN} \\ i_{Din} = i_{L1} + i_{L2} - I_{PN} \end{cases} \tag{3.8}$$

From Fig. 3.3(b), the peak dc-link voltage can written as

$$\hat{V_{PN}} = V_{C1} + V_{C2} + V_{DC} \tag{3.9}$$

3.3.3 Boost Factor and Inductor Currents Derivation

After applying volt-sec balance principle to inductors L_1, the following equation can be obtained

$$V_{C1} = \frac{2D_0(V_{DC} + V_{C2})}{(1 - D_0)} \tag{3.10}$$

Similarly, the average voltage across the inductor L_2 is also zero. Therefore, the expression for capacitor voltage is derived as

$$V_{C1} = \frac{(1 - D_0)V_{C2} - D_0 V_{DC})}{D_0} \tag{3.11}$$

From (3.10) and (3.11), the following capacitor C_1 voltage can be obtained as

$$V_{C2} = \frac{2D_0}{1 - 2D_0 - D_0^2} V_{DC} \tag{3.12}$$

After substituting the expression of capacitor C_2 in (3.11), the capacitor C_1 voltage can be obtained as

$$V_{C1} = \frac{D_0(1 + D_0)}{1 - 2D_0 - D_0^2} V_{DC} \tag{3.13}$$

Substituting the capacitor C_1, C_2 voltages in (3.9), the peak dc-link voltage can be obtained as

$$\begin{cases} \hat{V_{PN}} = \dfrac{1 + D_0}{1 - 2D_0 - D_0^2} V_{DC} \\ \hat{V_{PN}} = BV_{DC} \end{cases} \tag{3.14}$$

$$B = \frac{1 + D_0}{1 - 2D_0 - D_0^2} \tag{3.15}$$

where B – is the voltage boost, V_{DC} – is the supply voltage, D_0 – is the duty cycle ratio over a period, T.

By charge balance (or current-sec balance) of the capacitor C_1, we get

$$< i_{C1} >_{T_0} = 0 = D_0(-2i_{L1}) + (1- D_0)\ (i_{L2} - i_{PN}) \tag{3.16}$$

$$i_{L1} = \frac{(1- D_0)}{2D_0}\ (i_{L2} - i_{PN}) \tag{3.17}$$

Similarly, the charge balance of capacitor C_2 can be written as

$$< i_{C2} >_{T_0} = 0 = D_0(-i_{L2}) + (1- D_0)\ (i_{L1} - i_{PN}) \tag{3.18}$$

$$i_{L2} = \frac{(1- D_0)}{D_0}\ (i_{L1} - i_{PN}) \tag{3.19}$$

From (3.17) and (3.19), we get average inductor currents I_{L1} and I_{L2} respectively, as

$$i_{L1} = \frac{(1- D_0)}{1- 2D_0 - D_0^2}\ i_{PN} \tag{3.20}$$

$$i_{L2} = \frac{(1- D_0^2)}{1- 2D_0 - D_0^2}\ i_{PN} \tag{3.21}$$

From (3.1) and (3.15) it is observed that the boost factor of the SL-qZSI [50] and the proposed topology is same.

After substituting the expression of capacitor C_1, C_2 voltages in (3.3) and (3.7) the diode (D_{in}, D_1, D_2, and D_3) voltages can be obtained as

$$V_{Din} = \frac{-(1+ D_0)}{1- 2D_0 - D_0^2} V_{DC} \tag{3.22}$$

$$V_{D2} = \frac{-(1- D_0)}{1- 2D_0 - D_0^2} V_{DC} \tag{3.23}$$

$$V_{D1} = V_{D3} = \frac{-D_0}{1- 2D_0 - D_0^2} V_{DC} \tag{3.24}$$

From the above obtained diode voltage expressions and from SL-qZSI [50], it can be observed that the expressions of diode voltages are same in these presented topologies.

The average dc-link signal of the proposed topology is expressed as

$$\tilde{V_{PN}} = \frac{(1- D_0)(1+ D_0)}{1- 2D_0 - D_0^2} V_{DC} \tag{3.25}$$

The peak phase output signal of the proposed inverter topology is expressed as

$$\begin{cases} \hat{V_{an}} = M.\dfrac{\hat{V_{PN}}}{2} \\ \quad = M.B\dfrac{V_{DC}}{2} = G.\dfrac{V_{DC}}{2} \end{cases} \tag{3.26}$$

where G – is the voltage conversion ratio or voltage gain, $\hat{V}_{PN}$ - is the peak dc-link signal, and M – is the modulation index.

The voltage gain G in terms of the M for the proposed inverter is written as

$$G = \frac{M(2-M)}{(4M-M^2-2)} \tag{3.27}$$

Except the capacitor voltage expressions; the boost factor, diode voltages, voltage gain, peak dc-link voltage, and the average dc-link voltage of the One SL-ZSI is same as the presented One SL-IZSI.

3.4 Suppression of Inrush Current at Start-up Condition

As discussed in the introduction, similar to SL-qZSI [50] and Improved ZSI [45], the One SL-Improved ZSI also suppresses the starting inrush current problem. The circuit configuration of One SL-ZSI during starting condition is depicted in Fig. 3.4.

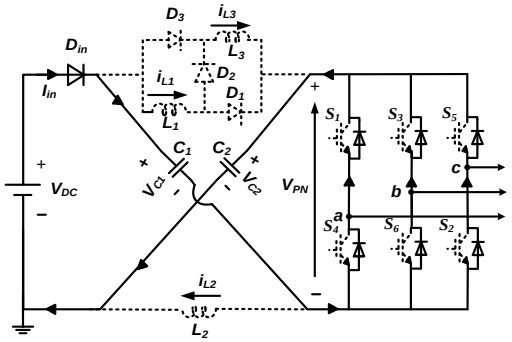


Fig. 3.4: Circuit diagram for inrush current of One SL-ZSI during starting condition.

In case One SL-ZSI, due to the initial voltage across the capacitors (C_1, C_2) in the impedance network and resonance of impedance network, there exist huge inrush current at starting condition. This inrush can be suppressed with One SL-improved ZSI where the impedance network and VSI bridge are connected in series with the input supply and as depicted in Fig. 3.2(b).

3.5 Z-Network Parameter Design

The inductors (L_1, L_2, and L_3) and capacitors (C_1, C_2) of the impedance network can be designed as follows. The rating of diodes and semiconductor switches is depends on the individual voltage and current stresses.

3.5.1 Design of Inductors

In shoot-through state, the inductors are charged by the capacitors and the input supply and the current through the inductor increases linearly. Therefore, the inductor voltages in shoot-through state can be written as

$$\begin{cases} L_{1,3}\dfrac{di_{L1,L3}}{dt} = V_{L1,L3} = \dfrac{(1-D_0)}{(1-2D_0-D_0^2)}V_{DC} \\ L_2\dfrac{di_{L2}}{dt} = V_{L2} = \dfrac{(1-D_0^2)}{(1-2D_0-D_0^2)}V_{DC} \end{cases} \tag{3.28}$$

Therefore, the impedance network inductors of the One SL-improved ZSI can be obtained from the following equations

$$\begin{cases} L_{1,3} = \dfrac{T_S D_0}{\Delta i_{L1,L3} k_0}\dfrac{(1-D_0)}{(1-2D_0-D_0^2)}V_{DC} \\ L_2 = \dfrac{T_S D_0}{\Delta i_{L2} k_0}\dfrac{(1-D_0^2)}{(1-2D_0-D_0^2)}V_{DC} \end{cases} \tag{3.29}$$

where, $\Delta i_{L1,L2,L3}$ represents the inductor current ripples and K_0 is the number shoot-through states over a period, T_S.

3.5.2 Design of Capacitors

Similarly, the capacitance of the Z-impedance network can be designed as follows

$$\begin{cases} C_1 = \dfrac{T_S D_0}{\Delta V_{C1} k_0}\dfrac{2(1-D_0)}{(1-2D_0-D_0^2)}I_{PN} \\ C_2 = \dfrac{T_S D_0}{\Delta V_{C2} k_0}\dfrac{(1-D_0^2)}{(1-2D_0-D_0^2)}I_{PN} \end{cases} \tag{3.30}$$

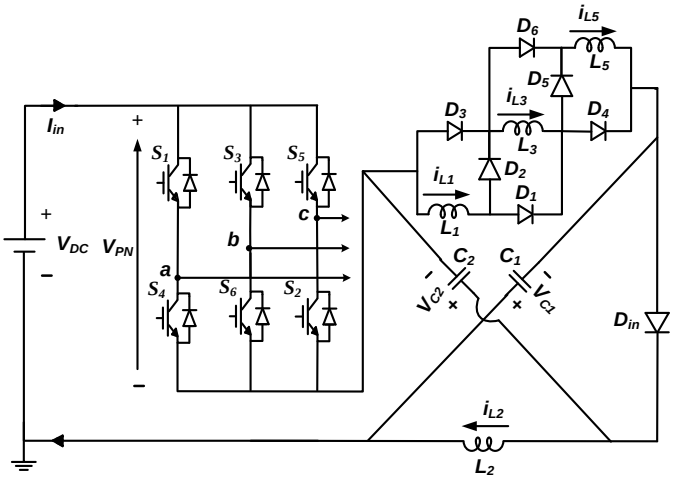


Fig. 3.5: Configuration of the extended One SL-improved ZSI.

3.6 Extension of the One SL-improved ZSI

In order to enhance the boost factor of One SL-ZSI and One SL-IZSI further, another switched-inductor cell can be inserted easily. As depicted in Fig. 3.5 for One SL-IZSI, an addition of only one extra inductor and three diodes increases the boost

factor further and the expression for the boost factor of this configuration is expressed as follows

$$B = \frac{1+2D_0}{1-2D_0-2D_0^2} \tag{3.31}$$

Table 3.1: Performance comparison of the proposed topologies with existing topologies

Parameter		Topologies for comparison				
		ZSI [41]	SL-ZSI [49]	SL-qZSI [50]	Presented topologies	
					One SL-ZSI	One SL-IZSI
Boost Factor	$\frac{\hat{V}_{PN}}{V_{DC}}$	$\frac{1}{(1-2D_0)}$	$\frac{1+D_0}{(1-3D_0)}$	$\frac{1+D_0}{(1-2D_0-D_0^2)}$	$\frac{1+D_0}{(1-2D_0-D_0^2)}$	$\frac{1+D_0}{(1-2D_0-D_0^2)}$
Capacitor Stress	$\frac{V_{C1}}{V_{DC}}$	$\frac{1-D_0}{(1-2D_0)}$	$\frac{1-D_0}{(1-3D_0)}$	$\frac{1-D_0}{(1-2D_0-D_0^2)}$	$\frac{1-D_0}{(1-2D_0-D_0^2)}$	$\frac{D_0(1+D_0)}{(1-2D_0-D_0^2)}$
	$\frac{V_{C2}}{V_{DC}}$	$\frac{1-D_0}{(1-2D_0)}$	$\frac{1-D_0}{(1-3D_0)}$	$\frac{2D_0}{(1-2D_0-D_0^2)}$	$\frac{1-D_0^2}{(1-2D_0-D_0^2)}$	$\frac{2D_0}{(1-2D_0-D_0^2)}$
	$\frac{V_{Din}}{V_{DC}}$	$\frac{-1}{(1-2D_0)}$	$\frac{-(1+D_0)}{(1-3D_0)}$	$\frac{-(1+D_0)}{(1-2D_0-D_0^2)}$	$\frac{-(1+D_0)}{(1-2D_0-D_0^2)}$	$\frac{-(1+D_0)}{(1-2D_0-D_0^2)}$
Diode Stress	$\frac{V_{D1,D3}}{V_{DC}}$	N.A	$\frac{V_{D2,D4,D5}}{V_{DC}} = \frac{-D_0}{1-3D_0}$	$\frac{-D_0}{(1-2D_0-D_0^2)}$	$\frac{-D_0}{(1-2D_0-D_0^2)}$	$\frac{-D_0}{(1-2D_0-D_0^2)}$
	$\frac{V_{D2}}{V_{DC}}$	N.A	$\frac{V_{D3,D6}}{V_{DC}} = \frac{-(-D_0)}{1-3D_0}$	$\frac{-(1-D_0)}{(1-2D_0-D_0^2)}$	$\frac{-(1-D_0)}{(1-2D_0-D_0^2)}$	$\frac{-(1-D_0)}{(1-2D_0-D_0^2)}$
Inductor Current		$i_{L1,L2} = \frac{1-D_0}{1-2D_0} I_{PN}$	$i_{L1,L2,L3,L4} = \frac{1-D_0}{1-3D_0} I_{PN}$	$i_{L1,L3} = \frac{1-D_0}{1-2D_0-D_0^2} I_{PN};\ i_{L2} = \frac{1-D_0^2}{1-2D_0-D_0^2} I_{PN}$		
Average DC-Link Current, I_{PN}		$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$
Input Current, I_{in}		$2i_{L1}-I_{PN}$	$2i_{L1}-I_{PN}$	i_{L2}	$i_{L1}+i_{L2}-I_{PN}$	I_{PN}

*Note: N.A- Not Applicable

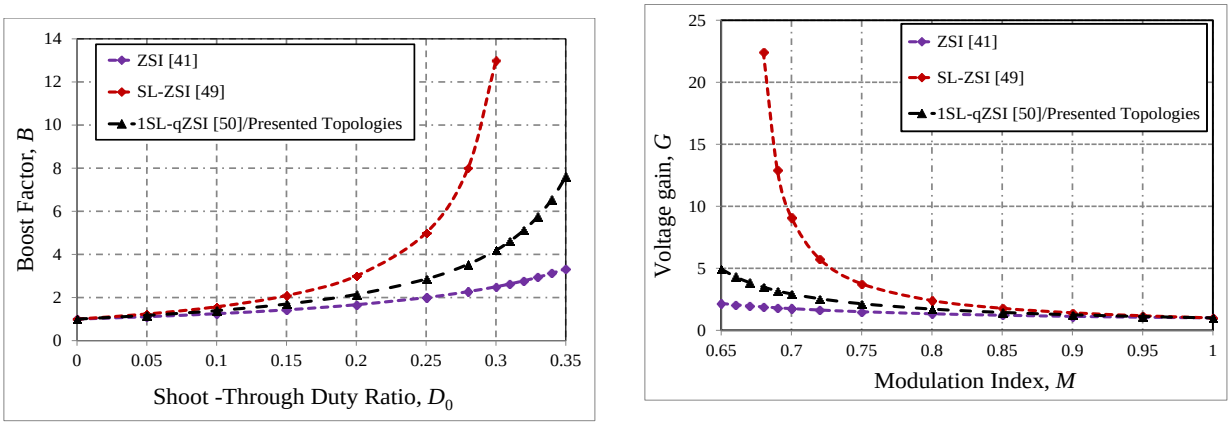
3.7 Performance Comparison of Proposed Inverters with Other Topologies

This section compares the performance of proposed topologies with the existing Z-source network topologies like ZSI [41], SL-ZSI [49], and SL-qZSI [50]. Table 3.1 compares the boost factor, capacitor and diode stresses, inductor currents and

average dc-link currents. Similarly, the number of components used, start-up current, and the nature of input current is compared in Table 3.2.

3.7.1 Boost Factor and Voltage Gain Comparison

From (3.13) it is observed that, the voltage boost or boost factor of the proposed topology is more than the ZSI [41]. The comparison of boost factor with duty cycle ratio D_0 for the traditional ZSI [41], SL-ZSI [49], SL-qZSI [50], and the proposed inverter topology is depicted in Fig. 3.6(a). From this figure, it is observed that for the same shoot-though period, the voltage boost B of the presented topology is higher than the ZSI and is lower than the SL-ZSI. But, the voltage boost B of the presented inverter topology is same as the SL-qZSI [50].



(a) (b)

Fig. 3.6: Comparison of: (a) boost factor; (b) voltage gain.

Similarly, the voltage gain G of the proposed inverter and the inverters proposed in [41], [49], and [50] are shown in Fig. 3.6(b). For the same voltage conversion ratio G and supply voltage V_{DC}, the proposed inverter utilizes higher modulation index M when compared to ZSI. The modulation index required producing the voltage gain as that of the SL-qZSI and proposed inverter is same. The increased modulation index results in improved output voltage quality.

3.7.2 Voltage Stress Comparisons

In this section, the stresses across the capacitors and semiconductor power switches of the inverter bridge for the presented topologies and the existing topologies are examined.

3.7.2.1 Switch Stress versus Voltage Gain

The stress across the semiconductor switch (which is defined as the ratio of V_S/GV_{DC} [23]) of the ZSI, SL-ZSI, SL-qZSI and presented topologies is depicted in

Fig. 3.7. The semiconductor switch stress of the presented inverter is more than the SL-ZSI and is lower than the ZSI, but is same as that of the SL-qZSI for the same voltage conversion ratio *G* and boost factor, *B*.

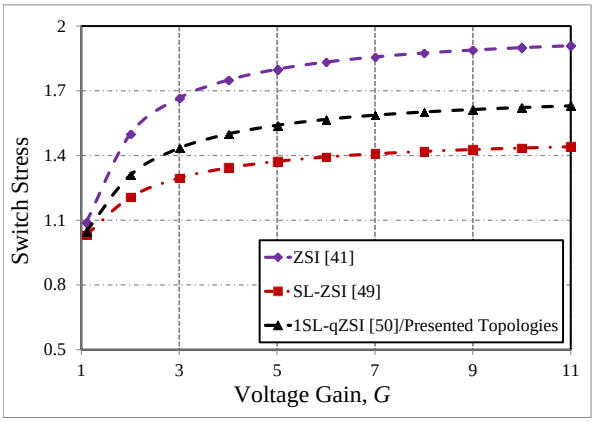


Fig. 3.7: Switch stress comparison.

3.7.2.2 Capacitor Stress versus Voltage Gain

Similarly, the capacitor stress (which is defined as the ratio of V_C/GV_{DC} [23]) comparison of the proposed inverter with respect to existing ZSI, SL-ZSI, and the SL-qZSI is depicted in Fig. 3.8. The overall stress across the capacitors of proposed topology is less when compare to ZSI and SL-ZSI for the same voltage conversion ratio *G*.

From Table 3.1, it can observe that the capacitor stress of the proposed topology is less when compared to that of SL-qZSI [50]. Therefore, lower rating capacitors can be used for the proposed inverter which reduces the cost, weight and space requirement.

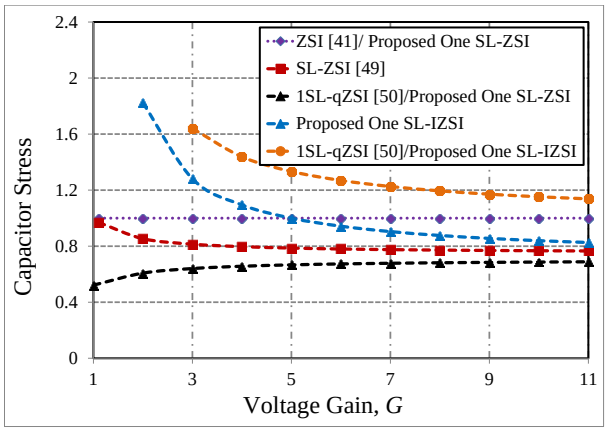


Fig. 3.8: Capacitor stress comparison.

3.7.3 Component Count

The number of components (i.e., both active and passive) used in the presented topologies and other existing topologies [41, 49, and 50] are compared in Table 3.2.

The passive and active components used in the presented topologies are lower than the SL-ZSI [49] and higher than the ZSI [41]. Whereas the components used in the proposed topology are same as that of the SL-qZSI [50]. Therefore, the boost factor or voltage gain can be increased with increase in number of components (both passive and active). To enhance the boost factor further, the SL cells can be increased which in turn increases the space and components.

Table 3.2: Common ground, start-up current, number of elements, and nature of input current comparison

Parameter		Topologies for comparison				
		ZSI [41]	SL-ZSI [49]	SL-qZSI [50]	Presented topologies	
					One SL-ZSI	One SL-IZSI
Common Ground		No	No	Yes	No	Yes
Start-up Current		Yes	Yes	No	Yes	No
Input Current		Discontinuous	Discontinuous	Continuous	Discontinuous	Continuous*
Number of Components	L	2	4	3	3	3
	C	2	2	2	2	2
	D	1	7	4	4	4
	S	6	6	6	6	6

*Note: For maximum boost control technique [22]

3.7.4 Nature of Input Current

As depicted in Fig. 3.10, the input current in both the topologies is discontinuous in case of simple boost control. It can be observed from Fig. 3.10(b), that the input current of One SL-improved ZSI is having more ripples when compare to One SL-ZSI shown in Fig. 3.10(a). Table 3.2 compares the nature of input current of different topologies along with the presented topologies. It is noted in this table, that the input current drawn from the supply can be continuous for maximum boost control PWM technique.

3.7.5 Average DC-link Current and Inductor Current Expressions

The expressions of average dc-link current and inductor currents are derived for both the proposed topologies and are compared with the existing topologies in Table 3.1.

Table 3.3: Components and parameters used for the simulation

S.No	Parameters/Descriptions	Values[a]
1	Input voltage, V_{DC}	60 V
2	Inductors ($L_1 = L_2 = L_3$)	0.7 mH
3	Capacitors ($C_1 = C_2$)	2000 μF
4	Switching frequency, f_s	10 kHz
5	Fundamental frequency, f	50 Hz
6	Modulation index, M	0.65
7	Duty cycle ratio, D_0	0.35
8	R-L Load	R_l = 20 Ω, L_l = 2.5 mH

3.8 Discussion on Simulation Results

To validate the theoretical analysis as discussed in the above section for the proposed One SL-IZSI topology, the simulations are carried out in MATLAB/Simulink platform using the simple boost control (SBC) method [21]. The modeling parameters are shown in Table 3.3 with duty cycle ratio of D_0 = 0.35 and supply voltage of V_{DC} = 60 V. From (3.12), (3.13), (3.14), (3.15) and (3.27), we obtain the theoretical values of V_{C1} = 159.7 V, V_{C2} = 236.6 V, V_{PN} = 456 V, B = 7.6, and G = 5 respectively when modulation index M = 0.65.

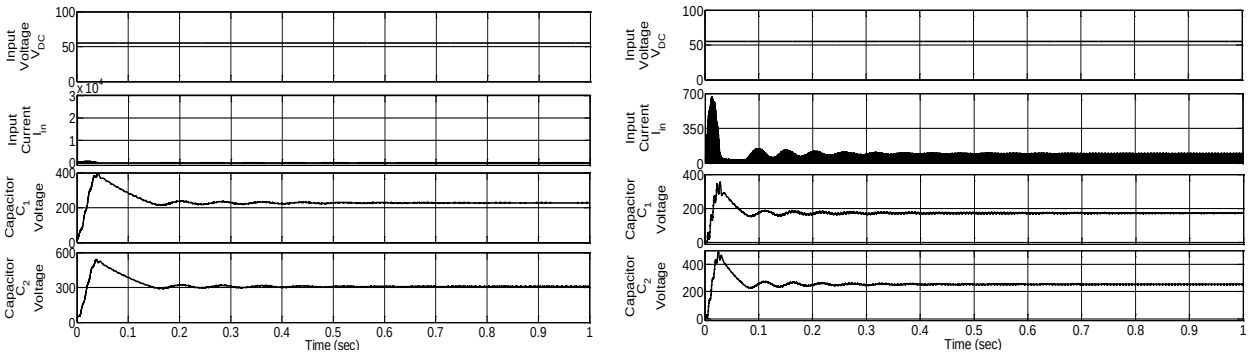
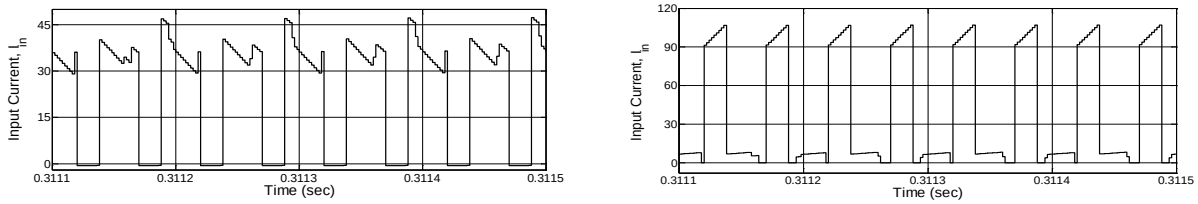


Fig. 3.9: Simulation results of input voltage (V_{DC}), input current (I_{in}), and capacitor voltages (V_{C1} and V_{C2}) for: (a) One SL-ZSI; (b) One SL-improved ZSI.

The simulation results of the input supply voltage, input current, and capacitor C_1, C_2 voltages are depicted in Fig. 3.9 for both the topologies when the input voltage is 60 V at duty cycle ratio D_0 = 0.35 and M = 0.65. It can be observed from Fig. 3.9(b), that the inrush current and capacitor voltages of One SL-improved ZSI are less when it is compared with One SL-ZSI shown in Fig. 3.9(a). This figure also shows that the capacitor voltages in steady-state condition and are almost same as the theoretical value obtained. As discussed in Section 3.4, In case of One SL-ZSI,

due to the initial voltage across the capacitors (C_1, C_2) in the impedance network, there exist inrush current at starting condition as can be observed from Fig. 3.9(a). This inrush current can be suppressed with One SL-improved ZSI and it can also be observed from Fig. 3.9(b) which is less than the One SL-ZSI.



(a) (b)

Fig. 3.10: Simulation results of input current (I_{in}) in steady-state condition for: (a) One SL-ZSI; (b) One SL-improved ZSI.

The steady-state input current of the both presented topologies are depicted in Fig. 3.10. From this figure, it is observed that both the presented topologies provide discrete input current. It is also observed from Fig. 3.10(b) that the input current ripple is more in case of One SL-IZSI. The current is zero in zero states, and it is non-zero in other states. Therefore, we can get continuous input current in case of One SL-IZSI by using the maximum boost control PWM technique.

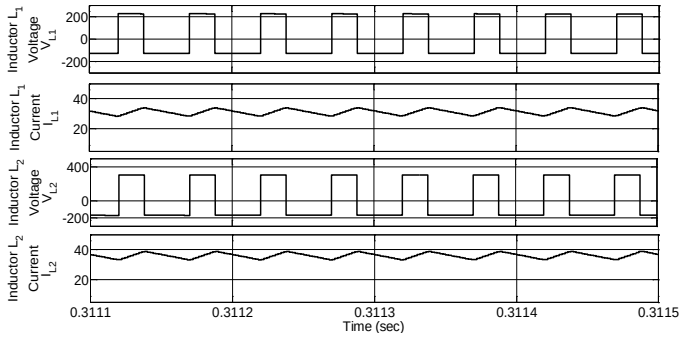


Fig. 3.11: From top to bottom; Simulation results of inductor L_1 voltage (V_{L1}), inductor L_1 current (I_{L1}), inductor L_2 voltage (V_{L2}), and inductor current (I_{L2}) respectively.

The inductor L_1 voltage and its current are shown in Fig. 3.11. The inductor current is linearly increasing in shoot-through state and it is decreasing in non-shoot-through state. Similarly, this figure is also shows the inductor L_2 voltage and its current respectively.

The simulation results of dc-link voltage signal, diode D_{in} voltage, and diode D_{in} current in steady-state condition of One SL-improved ZSI are depicted in Fig. 3.12 and will be same for One SL-ZSI. The peak-dc link signal is approximately same as the theoretical value obtained that is about 460 V. From this figure, it can observe that the dc-link signal is zero in the interval D_0 and peak voltage appears across the dc-link during the (1-D_0) period. In the interval of D_0, the peak voltage appears across

the diode D_{in} and will be zero due conduction of D_{in} in the remaining period. The current flowing through diode D_{in} is also noted in this figure and it can be observed that the current flowing through diode D_{in} is zero during shoot-through state.

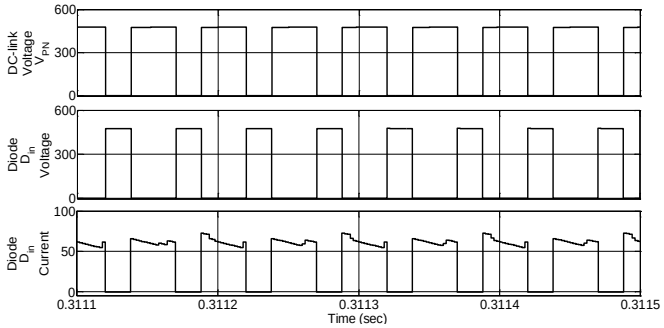


Fig. 3.12: From top to bottom; Simulation results of peak dc-link voltage (V_{PN}), diode voltage (V_{Din}), and diode current (I_{Din}).

The diode D_1 voltage and current flowing through diode D_1 is depicted in Fig. 3.13. The diode D_1 is ON during shoot-through period and therefore current flowing through this diode D_1 is the charging current of the inductor L_2. Whereas, the diode D_2 is ON during non-shoot-through period and therefore current flowing through this diode D_2 is the discharging current of the inductor L_1 or L_3.

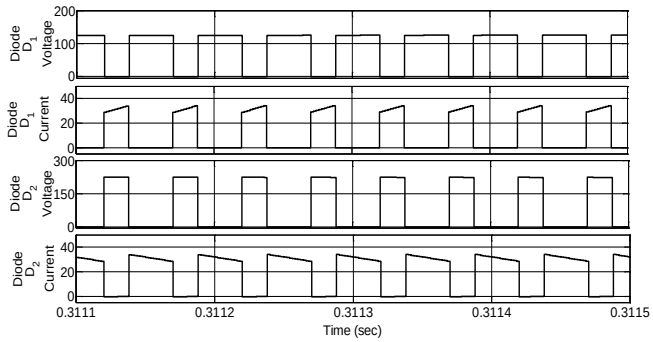


Fig. 3.13: From top to bottom; Simulation results of diode voltage (V_{D1}), diode current (I_{D1}), diode voltage (V_{D1}), and diode current (I_{D1}).

Fig. 3.14 depicts the line voltage, phase voltage, and phase currents respectively from top to bottom. The voltages obtained in simulations are almost same as the theoretical values.

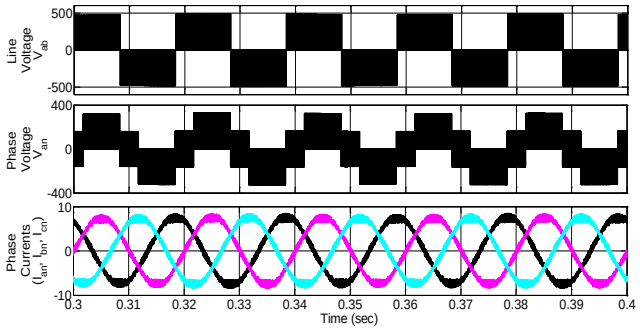


Fig. 3.14: Simulation results of line voltage (V_{ab}), phase voltage (V_{an}), and phase currents (I_{an}, I_{bn}, and I_{cn}).

3.9 Conclusion

This chapter presents some novel topologies based on the one switched-inductor concept which is applied to traditional ZSI and Improved Z-source inverter topology. These proposed inverters provide the same boost factor as that of the One SL-qZSI. Similar to one SL-qZSI, the One SL-IZSI topology shares common ground with the source, suppresses the input inrush current at start-up condition. In addition to that, less capacitor stress can be achieved in the proposed topology when compare to the One SL-qZSI. Therefore this topology is best suitable for the fuel cell/ solar PV system.

CHAPTER 4: VOLTAGE-LIFT Z-SOURCE/ IMPROVED Z-SOURCE INVERTERS

This chapter presents the two topologies of voltage-lift type Z-source/ Improved Z-source inverters (ZSIs). The middle diode in switched-inductor (SL) cell of One SL-ZSI/ One SL-IZSI is replaced with a voltage-lift capacitor to obtain the high boost factor. Therefore, the number of passive components and diodes are reduced, which reduces the cost, weight, and space requirement of the system when compared with SL-ZSI, extended-boost qZSIs, and enhanced-boost ZSI. Moreover, these proposed inverter topologies utilize very small shoot-through duty ratio to obtain the required boost factor at high modulation index which improves the overall output waveform quality with low THD for a given input voltage. It also results in less switch stress which improves the system efficiency. These proposed topologies are analysed in the steady-state condition and their theoretical analysis is validated in MATLAB/Simulink and then tested with laboratory prototype experimental setup.

4.1 Introduction

Recent research in the field of single-stage topologies has been focused on impedance (-Z) source network topologies like Z-source inverter (ZSI) [41], quasi-ZSIs (qZSIs) [43], improved-ZSI (IZSI) [45], switched-boost inverter (SBI) [59], developed embedded-ZSI (DE-ZSI) [65], and current-fed switched inverters (CFSI) [61]. One of the main disadvantages of these topologies is that the modulation index M of the inverter is restricted by the shoot-through duty ratio D_0. For example, in simple boost control (SBC), $D_0 \leq (1-M)$ (For maximum boost control (MBC) [22] and constant boost control (CBC) [23], this restriction is little relaxed). Thus achieving higher boost factor (i.e., ratio of peak dc-link voltage to the input dc voltage) at lower D_0 became a topic of interest among the researchers so that modulation index M can be made higher at lower dc input voltage to provide high quality output waveform with improved THD.

Therefore, to improve the boost factor, recently one switched-inductor ZSI was and one switched-inductor improved ZSI are proposed in [52] and [53] respectively to improve the performance characteristics of traditional ZSI and the circuit configurations of these topologies are shown in Fig. 4.1. The switched-inductor qZSI was presented in 2011 which provides same boost factor as the One SL-ZSI [52] but with improved performances [50]. The boost factor of the topologies presented in [50, 52, and 53] were same and is represented as

$$B = \frac{1+D_0}{1-2D_0-D_0^2} \tag{4.1}$$

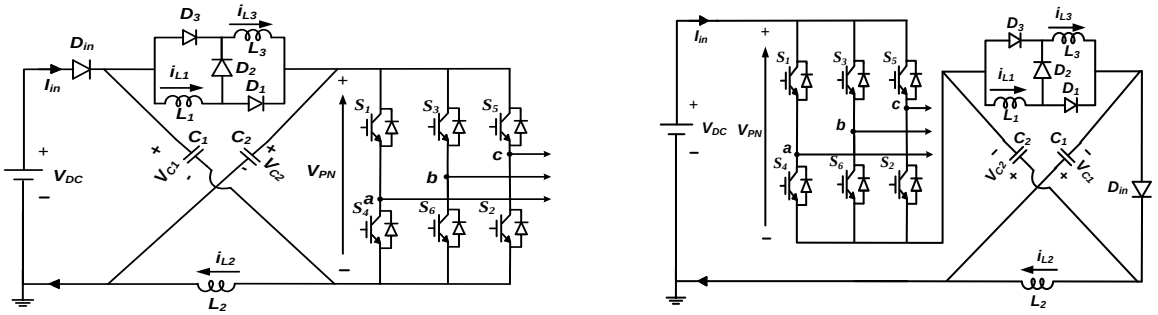


Fig. 4.1: Illustration of: (a) One SL-ZSI; (b) One SL-improved ZSI.

Many coupled-inductor based network inverters with less elements in the impedance network were presented in the literature which can achieve higher voltage gain at lower shoot-through duty ratios [75 – 97]. These topologies may provide high boost factor at low duty ratio, but they produce high voltage spikes across the dc-link as well as across the power semiconductor switches [98, 99]. Therefore, many non-coupled based topologies like SL-ZSI [49], diode-assisted/ capacitor-assisted (DA/CA)-qZSIs [47], SL-qZSIs [51], and enhanced-boost ZSI (EB-ZSI) [73] were proposed in the literature with increased number of components in the impedance network.

Among them, the EB-ZSI provides the highest boost factor *B* at the lowest shoot-through duty ratio using two-pair of switched-impedance network [73]. The each switched-impedance cell consists of two-diodes, two-capacitor, and two-inductors.

Although it is theoretically possible to achieve gain of any order, practically achievable highest gain of a converter is finite and depends on the on-state drop of the switching losses, equivalent series resistance (ESR) of capacitors, DC resistance of inductors, etc. On-state drop of the switching devices play a big role in dictating the circuit gain and efficiency, especially in renewable energy applications like low voltage DC (24 V/ 36 V/ 48 V) to 110/ 220 V rms AC conversions.

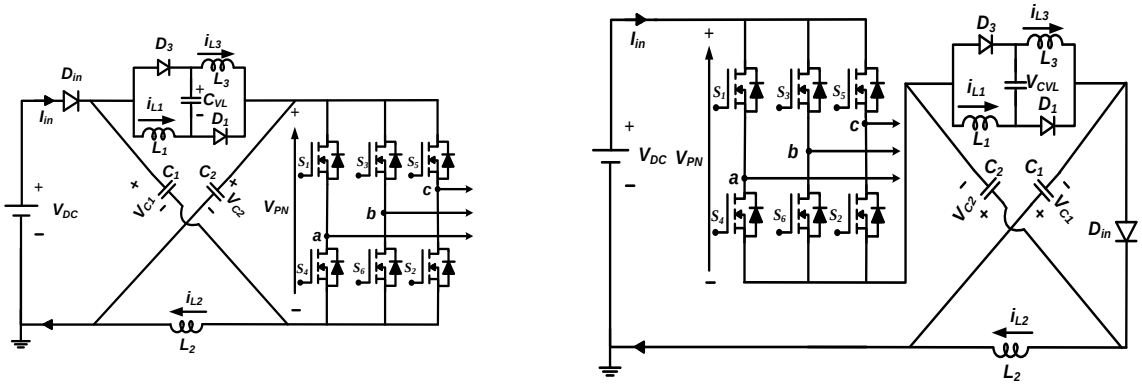
While achieving higher voltage gain has been the primary aim, some other desirable properties of the high gain inverters are:

1. Reduced component count for compact, small volume, high efficiency, and reliable system design.
2. Input current continuity which eliminates or reduces the need for an input filter stage.

The EB-ZSI uses more number of elements in the impedance network, in order to achieve above mentioned properties. Some novel topologies with high gain are

proposed based on voltage-lift concept. It provides very high boost factor when compared to other existing non-coupled based topologies at low shoot-through duty ratios with very less number of passive as well as active components. Due to this low shoot-through period, the conduction losses are less and hence, it improves the overall system efficiency. The middle diode of One SL-ZSI/ One SL-IZSI discussed in Chapter 3 is replaced with voltage-lift capacitor C_{VL} and is named as voltage-lift unit and is depicted in Fig. 4.2. The voltage-lift unit consists of two-diodes (D_1, D_3), two-inductors (L_1, L_3), and one voltage lift capacitor, C_{VL}.

In the next section, the evolution of the voltage-lift type of ZSI and improved ZSIs are discussed along with its operating principle. Section 4.2 describes the derivation of voltage-lift concept. The steady-state characteristics, voltage gain derivation of the proposed inverters are discussed in Section 4.3. The suppression of inrush current is also described in Section 4.4. Section 4.5 elaborates the designing of impedance parameters. Section 4.6 describes the performance comparison of conventional ZSI, SL-ZSI, extended boost-qZSI and enhanced-boost ZSI with the proposed VL-ZSI/VL-improved-ZSI. Finally, the discussions on the simulation and experimental results are included in Section 4.7 and 4.8 respectivily.



(a) (b)

Fig. 4.2: Configuration of proposed VL-impedance network topologies: (a) Voltage-lift ZSI; (b) Voltage-lift improved ZSI.

4.2 Derivation of Voltage-lift Concept from One Switched-Inductor Z-Source / Improved Z-Source Inverters and their Circuit Diagrams.

The topology illustrated in Fig. 4.1 provides voltage boost to only certain extent. To further heighten the boost factor in single-stage with increased reliability, the middle diode D_2 in switched-inductor (SL) cell of One SL-ZSI is replaced with voltage-lift capacitor (C_{VL}) and is shown in Fig. 4.2(a) and is termed as voltage-lift ZSI (VL-ZSI). Where, the voltage-lift unit consists of two-diodes, two-inductors, and one

voltage-lift capacitor (or the combination of L_1 – D_1 – C_{VL} – D_3 – L_3 forms voltage-lift unit). The number of components used in the proposed VL-ZSI and One SL-ZSI [52] are remaining same with increased boost factor. But, the drawbacks of VL-ZSI are akin to One SL-ZSI; therefore to avoid those drawbacks, the voltage-lift improved ZSI (VL-IZSI) is proposed and is shown in Fig. 4.2(b).

4.3 Proposed Voltage-lift ZSI and Voltage-lift Improved-ZSI

The proposed inverter topologies of ZSI and improved ZSIs are shown in Fig. 4.2(a) and Fig. 4.2(b) respectively. The difference between the SL-ZSI, SL-improved ZSI, and SL-qZSI with the proposed inverter topology is that only one of the two SL-cells is used as a voltage-lift (VL) unit. Therefore number of elements is reduced. The middle diode of the SL cell is replaced with capacitor C_{VL} to obtain the high boost factor at low shoot-through duty ratio and high modulation index which provides the better quality output waveform with low total harmonic distortion (THD) for the same input and output voltages.

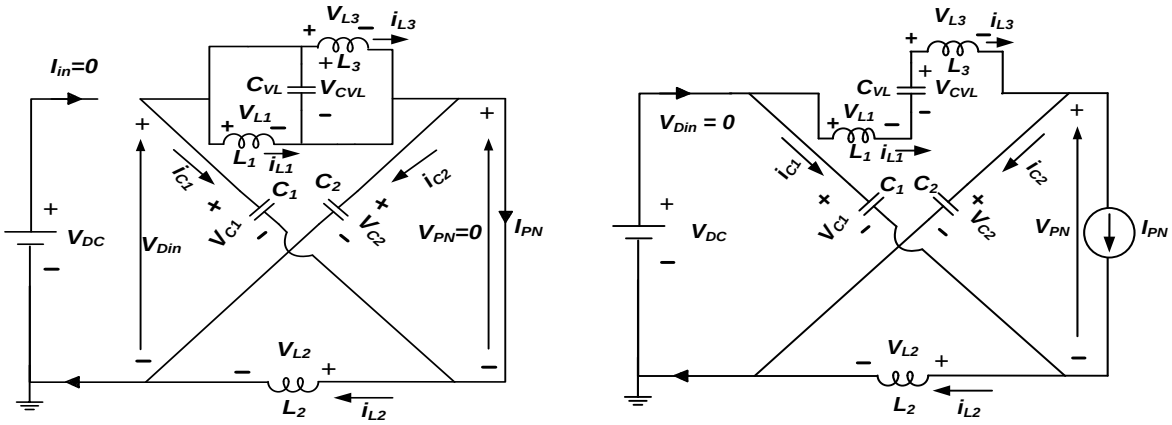
At low shoot-through duty ratio (i.e. $D_0 \leq 0.25$), the boost factors of both the proposed inverter topologies are same and are more than that of the conventional ZSI [41], SL-ZSI [49], SL-qZSI [50, 51], DA/CA-qZSIs [47], and the EB-ZSI [73] for the same input voltage and duty ratio D_0. Even at $D_0 = 0$, the dc-link voltage of the proposed inverters is twice the input voltage. This is due to the voltage-lift capacitor. The operating principle and boost factor derivations of the proposed VL-ZSI and VL-Improved-ZSI are obtained in Section 4.3.1 and Section 4.3.2 respectively.

4.3.1 Steady-state Operation and Boost Factor Derivation of Voltage-lift Z-Source Inverter

As shown in Fig. 4.2(a), the impedance network of VL-ZSI consists of three diodes, three inductors, and three capacitors. The top SL-cell of SL-ZSI is replaced with VL unit and bottom SL-cell is replaced with single inductor L_2 and the capacitors are placed similarly to that of SL-ZSI. Only the top SL-cell of SL-ZSI is used as the VL unit by replacing the middle diode with the VL capacitor to boost the input voltage to the required level. Therefore, when compared with the SL-ZSI [49], DA/CA-qZSIs and EB-ZSI [73], the proposed inverter topology uses less number of passive (i.e. capacitor and inductor) and active (i.e. diodes) components which reduces the space, cost, weight, and complexity of the system. Moreover, it uses a very small

duty ratio to produce the required voltage boost and hence, the system efficiency is improved.

Similar to the conventional ZSI, the VL-ZSI has seven shoot-through states in addition to the eight non-shoot-through states (i.e. six active states and two zero states) which are described next.



(a) (b)

Fig. 4.3: Circuit diagram of voltage-lift type-ZSI in : (a) shoot-through; (b) non-shoot-through states

4.3.1.1 Shoot-Through State

The equivalent circuit of VL-ZSI in the shoot-through states is shown in Fig. 4.3(a). The diodes D_1, D_3 are turned on and diode D_{in} is off. The input current is zero and peak dc-link voltage is also zero during the period, D_0. The inductors L_1, L_3 are charged by a parallel capacitor C_1, whereas capacitor C_{VL} obtains energy from C_1 which significantly magnifies the voltage boost and the inductor L_2 is charged by the parallel capacitor C_2. The inductors store the electromagnetic energy.

Applying Kirchoffs voltage law (KVL) to Fig. 4.3(a), the following equations can be obtained as

$$\begin{cases} V_{L1} = V_{L3} = V_{C1} = V_{CVL} \\ V_{L2} = V_{C2} \\ V_{Din} = V_{C1} + V_{C2} \end{cases} \tag{4.2}$$

4.3.1.2 Non-Shoot-Through State

The equivalent circuit during non-shoot-through states is shown in Fig. 4.3(b). Diodes D_1, D_3 are off and input diode D_{in} is turned on. The stored energies in the series inductors L_1, L_2, and L_3 and capacitor C_{VL} are transferred to main dc-link circuit during the period (1 - D_0) to boost the voltage gain. The capacitors are charged from

the input supply through inductors. Applying KVL to Fig. 4.3(b), the following equations can be obtained.

$$\begin{cases} V_{L1} = V_{DC} + V_{C1} - V_{L3} - V_{C2} \\ V_{L2} = V_{DC} - V_{C1} \\ V_{L3} = V_{DC} + V_{C1} - V_{L1} - V_{C2}, \quad \text{and } V_{Din} = 0 \end{cases} \tag{4.3}$$

$$V_{PN}^{\wedge} = V_{C2} - V_{DC} + V_{C1} \tag{4.4}$$

From (4.2) and (4.3), the voltage across the inductors L_1 and L_3 is as follows

$$(V_{L1} = V_{L3})_{non\_shoot} = (V_{DC} + V_{C1} - V_{C2}) + D_0 \frac{V_{C1}}{(1 - D_0)} \tag{4.5}$$

Since the average voltages across the inductors are always zero, therefore the following equations are obtained as

$$V_{C2} = \frac{(V_{C1} - V_{DC})(1 - D_0)}{D_0} \tag{4.6}$$

$$V_{C2} = \frac{1 + D_0}{1 - D_0} V_{C1} + V_{DC} \tag{4.7}$$

From (4.6) and (4.7), the voltage across capacitor C_1 can be obtained as

$$V_{C1} = \frac{1 - D_0}{1 - 3D_0} V_{DC} \tag{4.8}$$

Similarly, after substituting (4.8) in (4.7), the voltage expressions for capacitors C_2 and C_{VL} (or C_3) can be obtained as

$$V_{C2} = 2\frac{1 - D_0}{1 - 3D_0} V_{DC} \tag{4.9}$$

$$V_{C3} = V_{CVL} = \frac{1 - D_0}{1 - 3D_0} V_{DC} \tag{4.10}$$

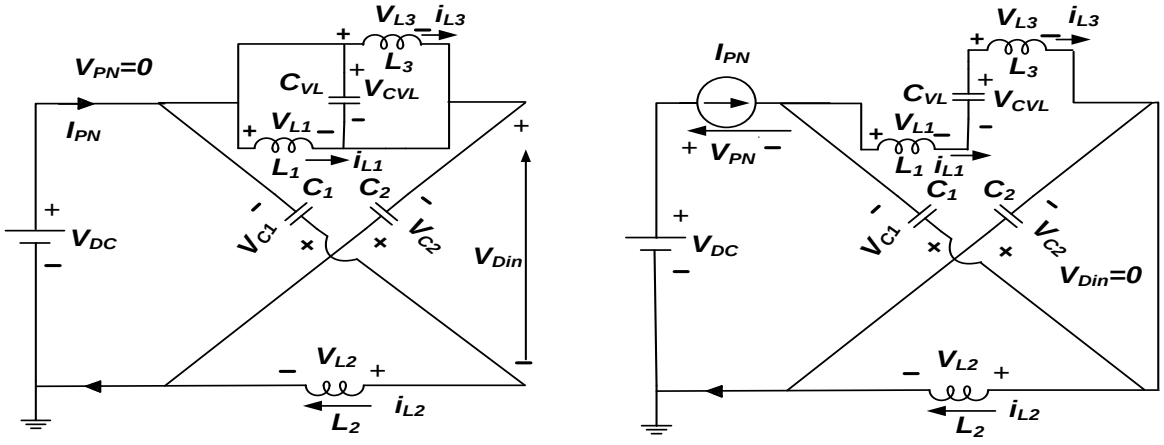
The peak dc-link signal is derived from Fig. 4.3(b). Substituting the capacitor voltages V_{C1} and V_{C2} in (4.4), the peak dc-link voltage can be obtained as

$$V_{PN}^{\wedge} = \frac{2}{1 - 3D_0} V_{DC} \tag{4.11}$$

The VL-ZSI gives the discontinuous input current because the input diode is in series with the input supply. Also, the VL-ZSI does not share the common ground with the source and the stress across the capacitors is more similar to ZSI [41] and SL-ZSI [49]. Therefore, to avoid the aforementioned drawbacks of VL-ZSI, the VL-improved ZSI is also discussed in this chapter for the analysis.

4.3.2 Steady-state Operation and Boost Factor Derivation of Voltage-lift Improved Z-Source Inverter

Similar to VL-ZSI, the Z- network of VL- improved-ZSI consists of three diodes, three inductors, and three capacitors as depicted in Fig. 4.2(b). In order to reduce the capacitor voltage stress, and to suppress the inrush current, the impedance network is connected in series with the dc voltage source and bridge inverter. Moreover, this topology shares common ground with the source and bridge inverter.



(a) (b)

Fig. 4.4: Circuit diagram of voltage-lift type improved-ZSI in: (a) shoot-through state; (b) non-shoot-through state.

4.3.2.1 Shoot-Through State

As depicted in Fig. 4.4(a), the diodes D_1, D_3 are turned on and diode D_{in} is off. The inductors L_1, L_3 are charged by a capacitor C_2 and input supply, whereas the capacitor C_{VL} obtains energy from C_2 which significantly magnify the voltage boost. The inductor L_2 is charged from the input and capacitor C_1. These inductors store the electromagnetic energy during this period. Applying KVL to Fig. 4.4(a), the following equations can be obtained.

$$\begin{cases} V_{L1} = V_{L3} = V_{CVL} = V_{DC} + V_{C2} \\ V_{L2} = V_{DC} + V_{C1} \\ V_{Din} = -V_{DC} - 2V_{C2} \end{cases} \tag{4.12}$$

4.3.2.2 Non-Shoot-Through State

The equivalent circuit in the non-shoot through states is shown in Fig. 4.4(b). The diodes D_1, D_3 are off and diode D_{in} is turned on. The energies stored in inductors L_1, L_2, and L_3 and capacitor C_{VL} are transferred to the main dc-link circuit in order to

boost the voltage. The capacitors C_1, C_2 are charged by the input supply through inductors.

$$\begin{cases} V_{L1} = V_{DC} + V_{C2} - V_{C1} - V_{L3} \\ V_{L2} = -V_{C2} \\ V_{L3} = V_{DC} + V_{C2} - V_{C1} - V_{L1} \end{cases} \tag{4.13}$$

The average voltage across the inductor L_2 is zero in steady-state condition and applying volt-second balance principle to L_2, it can be written as

$$V_{C2} = \frac{D_0(V_{DC} + V_{C1})}{1 - D_0} \tag{4.14}$$

The voltage across the inductors L_1 and L_3 in non-shoot through state can be written as

$$(V_{L1} = V_{L3})_{non\_shoot} = (V_{DC} - V_{C1} + V_{C2}) + \frac{D_0}{(1 - D_0)}(V_{C1} + V_{DC}) \tag{4.15}$$

Similarly, applying volt-second balance principle to L_2, following equation is obtained

$$V_{C2} = \frac{1 - D_0}{1 + D_0} V_{C1} - V_{DC} \tag{4.16}$$

From (4.14) and (4.16), the capacitor voltages can be derived as

$$V_{C1} = \frac{1 + D_0}{1 - 3D_0} V_{DC} \tag{4.17}$$

$$V_{C2} = \frac{2D_0}{1 - 3D_0} V_{DC} \tag{4.18}$$

$$V_{C3} = V_{CVL} = \frac{1 - D_0}{1 - 3D_0} V_{DC} \tag{4.19}$$

The peak dc-link voltage of the VL-IZSI can be derived from Fig. 4.4(b),

$$\hat{V}_{PN} = V_{C2} + V_{DC} + V_{C1} \tag{4.20}$$

After substituting (4.17) and (4.18) in (4.20), the peak dc-link voltage of the bridge inverter can be written as

$$\hat{V}_{PN} = \frac{2}{1 - 3D_0} V_{DC} \tag{4.21}$$

$$\hat{V}_{PN} = B V_{DC} \tag{4.22}$$

where, B is the boost factor of the impedance network.

4.3.3 Expression of Voltage Gain and Switch Stress

The peak phase output voltage ($\hat{V}_{an}$) of both the proposed inverter can be obtained as follows

$$\begin{cases} \hat{V}_{an} = M\dfrac{\hat{V}_{PN}}{2} \\ \hat{V}_{an} = G\dfrac{V_{DC}}{2} \end{cases} \tag{4.23}$$

From (4.11) and (4.21), it can be observed that the peak dc-link voltage of the VL-ZSI and VL-improved ZSI is same. Therefore, the voltage gain ($G = MB$) for the simple boost control scheme [21] in terms of the modulation index (assuming ideal case) for both the topologies can be defined as

$$G = MB = \frac{\hat{V}_{an}}{(V_{DC}/2)} = \frac{2M}{3M-2} \tag{4.24}$$

The switch stress V_S in terms of the voltage gain G for the proposed topology can be obtained as follows

$$V_S = BV_{DC} = \frac{3G-2}{2}V_{DC} \tag{4.25}$$

4.4 Suppression of Inrush Current at Startup Condition

The huge inrush current flows through input diode D_{in} at the starting condition of conventional ZSI [41], SL-ZSI [49], and EB-ZSI [73] and also in the proposed VL-ZSI due to the presence of energy storage elements in the impedance networks as depicted in Fig. 4.5.

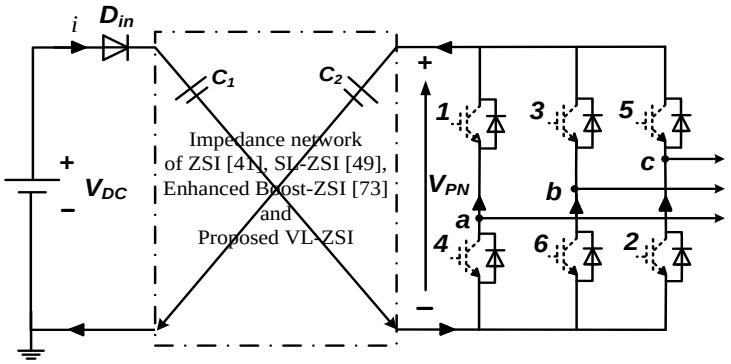


Fig. 4.5: Inrush current equivalent circuit at starting condition.

At the starting condition, all the feedback diodes of semiconductor switches and input diode D_{in} conduct through capacitors C_1 and C_2. Since the initial voltages across these capacitors are zero. The capacitors are immediately charged to half of the input voltage. Then, the capacitors and inductors of the impedance network start

resonating and generate huge voltage and current spikes in ZSI, SL-ZSI, EB-ZSI and in the proposed VL-ZSI. The proposed VL-improved ZSI suppresses the problem of inrush current because there is no closed path for the current to flow from input side to the main bridge circuit. So there is a reduction in voltage and current spikes. The current, *i(t)* through diodes and capacitors at the starting condition and at time, *t* can be written as follows

$$i(t) = \frac{V_{DC}}{R} e^{-(\frac{2}{RC})t} \tag{4.26}$$

where, *R* - is the internal resistance of the diodes and capacitors (C_1, C_2) and *C* - is the equivalent capacitance of the capacitors (C_1, C_2)

4.5 Designing of Impedance Network Parameters

The input voltage appears across the capacitors when there is no boost operation involved and the voltage across the inductor is zero. Therefore, a pure DC current flows through the inductors. In order to boost the voltage, the shoot-through duty ratio is inserted. Therefore, the ripple current exits in the inductor. The purpose of the inductor and capacitor is to limit the current and voltage ripples respectively. During shoot-through, the inductors are charged by the capacitors and the inductor current increases linearly.

The voltage across the inductor is same as the capacitor voltage as given below

$$\begin{cases} V_{L1} = V_{L3} = V_{C1} = V_{C3} \\ V_{L2} = V_{C2} \end{cases} \quad \text{For VL-ZSI} \tag{4.27}$$

$$\begin{cases} V_{L1} = V_{L3} = V_{C3} = V_{C2} + V_{DC} \\ V_{L2} = V_{C1} + V_{DC} \end{cases} \quad \text{For VL-improved ZSI} \tag{4.28}$$

Therefore, the inductors of both the proposed topologies can be designed as

$$\begin{cases} L_{1,3} = \dfrac{T_S D_0}{\Delta i_{L1,3} k_0} \dfrac{(1-D_0)}{(1-3D_0)} V_{DC} \\ L_2 = \dfrac{T_S D_0}{\Delta i_{L2} k_0} \dfrac{2(1-D_0)}{(1-3D_0)} V_{DC} \end{cases} \tag{4.29}$$

In order to design the capacitors, the inductor current is same as the capacitor current in shoot-through state. Therefore, the capacitors can be designed by using

$$\begin{cases} C_{1,3} = \dfrac{T_S D_0}{\Delta V_{C1,3}} \dfrac{i_{L1,3}}{k_0} \\ C_2 = \dfrac{T_S D_0}{\Delta V_{C2}} \dfrac{i_{L2}}{k_0} \end{cases} \tag{4.30}$$

Here, the inductor currents expressions $i_{L1/L3}$, i_{L2} are derived as follows

$$\begin{cases} i_{L1L3} = \dfrac{1-D_0}{1-3D_0} I_{PN} \\ i_{L2} = \dfrac{2(1-D_0)}{1-3D_0} I_{PN} \end{cases} \tag{4.31}$$

where, k_0 is the number of shoot-through states over a period, T_S

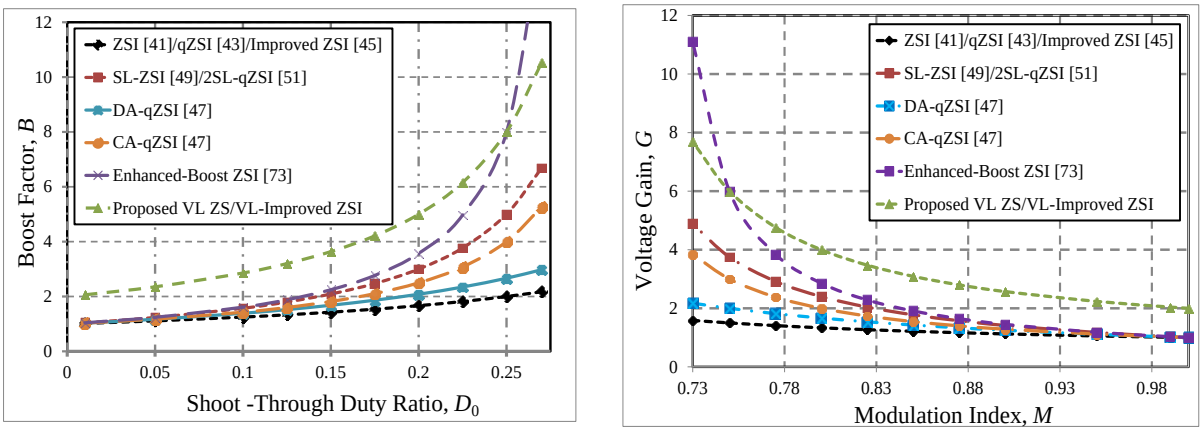
4.6 Performance Comparison of the Voltage-Lift Impedance Network Inverter Topologies

The performance comparison like boost factor, voltage gain, stress across switch and capacitor, and capacitor and inductor ripples of various topologies and the presented topology are compared in this section.

4.6.1 Boost Factor and Voltage Gain Comparison

As can be seen from Fig. 4.6(a), the boost factor of the proposed topologies is higher than that of conventional ZSI [41], SL-ZSI [49], extended boost-qZSI [47], and EB-ZSI [73] for the duty ratio D_0 with less passive and active components.

The Fig. 4.6(b) depicts the comparison of voltage gain G of both the proposed topologies with ZSI, SL-ZSI, extended-boost-qZSI, and EB-ZSI at the same modulation index and input voltage. It can be observed from Fig. 4.6(b) that the proposed inverter topology has the higher voltage gain.



(a) (b)

Fig. 4.6: Comparison of proposed VL-ZS/Improved ZSI topologies: (a) boost factor versus duty ratio; (b) voltage gain versus modulation index.

4.6.2 Voltage Stress Comparison

In this section, the stress across the switch and capacitor stress of the presented topology are compared with the existing topologies that are noted in Table 4.1 at voltage gain G.

4.6.2.1 Switch Stress versus Voltage Gain

Fig. 4.7 depicts the comparison of switch stress, which is defined as the ratio of V_S and GV_{DC} [23], for the proposed VL-ZSI/VL improved-ZSI with that of other inverter topologies. As can be observed from this figure that if voltage gain is below five (i.e., $G \leq 5$), the stress across the switch is lower than all the existing inverter topologies. But, after $G \geq 5$ the stress across the semiconductor switch is slightly higher than EB-ZSI [73] and less than that of ZSI [41], SL-ZSI [49], and extended boost-qZSIs [47] for the same voltage gain and duty ratio. Therefore, for a given shoot-through duty ratio and input voltage, the proposed inverter topologies provide less switch stress when compared to the existing topologies which decreases the switch conduction loss and thus, the efficiency of the system is improved.

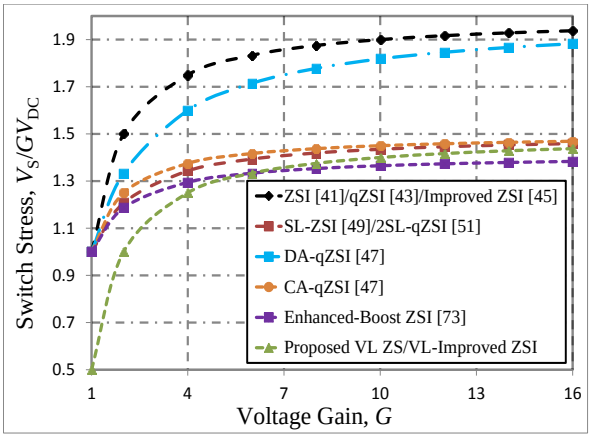


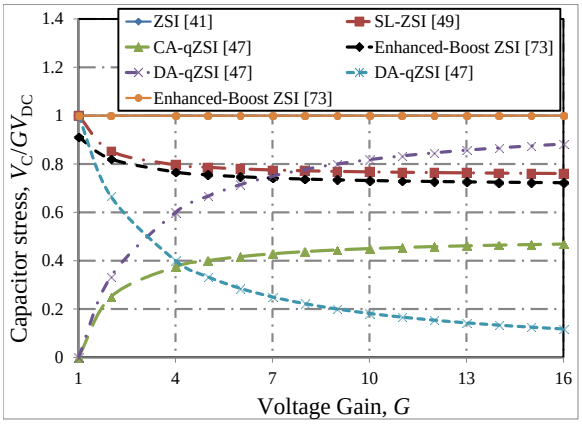
Fig. 4.7: Comparison of switch stress versus voltage gain for different topologies

4.6.2.2 Capacitor Stress versus Voltage Gain

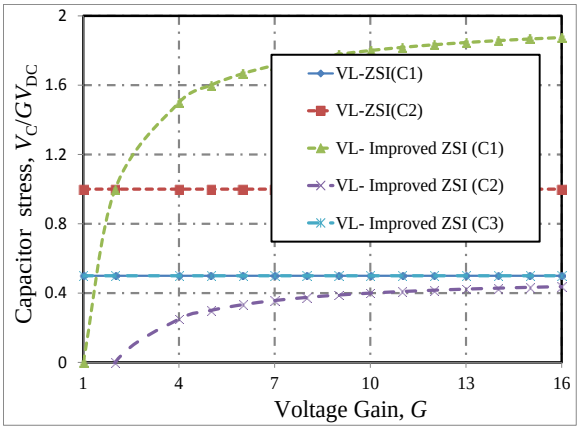
The capacitor stress is defined as V_C/GV_{DC} [23]. A comparative study of capacitors stress for different topologies (i.e., ZSI, SL-ZSI, extended-qZSI and EB-ZSI) is depicted in Fig. 4.8(a). Fig. 4.8(b) depicts the capacitor voltage stress comparison for the proposed VL-ZSI and VL-improved ZSI. It can be observed from Fig. 4.8(a) and Fig. 4.8(b) that the stress across the capacitors in the proposed topologies is slightly less when compared to the conventional ZSI, SL-ZSI, extended boost-qZSIs, and EB-ZSI. But, the stress across the capacitor C_1 in VL-IZSI is more than that of all existing topologies.

4.6.3 Ripple Analysis and Comparisons

This section describes the capacitor and inductor ripples equivations of the presented topology and compares them with the traditional ZSI, SL-ZSI, DA/Ca-qZSIs, and EB-ZSI.



(a)



(b)

Fig. 4.8: Comparison of capacitor stress of: (a) conventional impedance network inverters; (b) proposed VL-ZS/improved –ZSIs.

4.6.3.1 Inductor Current Ripple Analysis

For any Z-source topology, the inductor charges in shoot-through states and discharges in non-shoot-through states, and the high-frequency current ripples are presented in the inductor current. Moreover, the length of every shoot-through time interval may affect the current ripples.

Using (4.29), the inductor current ripple becomes

$$\begin{cases} \Delta i_{L1,3} = \dfrac{T_S D_0}{k_0 L_{1,3}} \dfrac{(1-D_0)}{(1-3D_0)} V_{DC} \\ \Delta i_{L2} = \dfrac{T_S D_0}{k_0 L_2} \dfrac{2(1-D_0)}{(1-3D_0)} V_{DC} \end{cases} \tag{4.32}$$

For the constant T_S, V_{DC}, k_0, and $L_{1,2,3}$, the current ripple is proportional to the coefficient $kI_{1,2,3}$ of inductor current ripple, that is

$$\begin{cases} kI_{1,3} = \dfrac{D_0(1-D_0)}{(1-3D_0)} \\ kI_2 = \dfrac{2D_0(1-D_0)}{(1-3D_0)} \end{cases} \tag{4.33}$$

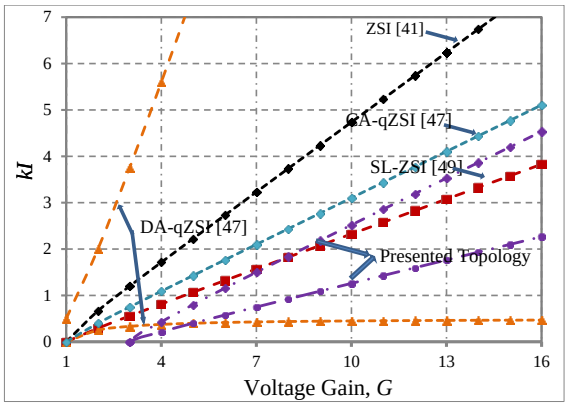


Fig. 4.9: kI versus voltage gain comparison.

The coefficient of *kI* versus voltage gain *G* is shown in Fig. 4.9. According to the above expression, the *kI* is a good measure for inductor volume for the same output power. In this figure, it is shown that the proposed scheme has lower inductor volume (inductance) compared with conventional ZSI and SL-ZSI methods. This is due to the fact that the proposed scheme requires smaller D_0 to produce a high boost factor *B*. Smaller D_0 will result in lower inductances.

Fig. 4.9 shows the coefficient of inductor current ripple against voltage gain for the topologies compared in Table 4.1. It can be seen that the current ripple coefficient rises with the shoot-through duty ratio D_0 (i.e., voltage gain) increasing. From (4.11), (4.21) and (4.23), if the DC input voltage is lower, the required shoot-through duty ratio is larger to obtain the desired DC-link peak voltage and the desired AC output voltage. As a result, the Z-source inductor current ripple increases when the DC source voltage decreases.

4.6.3.2 Capacitor Voltage Ripple Analysis

In shoot-through, the capacitors' current is equal to the inductors' current; hence, the capacitors can be calculated based on (4.30).

The average capacitor current is zero in one period and for the constant value of T_S, i_L, Δ_{VC}, and K_0, the coefficient $kC_{1,2,3}$ will be defined as

$$\begin{cases} kC_{1,3} = \dfrac{1-D_0}{1-3D_0} \\ kC_2 = \dfrac{2(1-D_0)}{1-3D_0} \end{cases} \tag{4.34}$$

It can be seen that the capacitance ripple has direct relation with average inductor current; hence, the more capacitor (inductor) current will lead to higher capacitor size and increased cost.

4.6.4 Component Count Comparison

The passive and active components comparisons are made in Table 4.1. From this table, it can be observed that the number of inductors used in the proposed topologies is less when compared to the SL-ZSI [49] and EB-ZSI [73] and is same as that of the extended-boost qZSI [37]. The number of capacitors used in the proposed inverter topologies is also less when compared to the EB-ZSI and CA-qZSI and is same as that of DA-qZSI, but it requires one extra capacitor when compared to SL-ZSI. The number of diodes used in the proposed topology is very less when compared to the SL-ZSI and EB-ZSI, but more or less same as extended boost qZSI.

Therefore, for the same input voltage and duty cycle with less number of passive and active components, the proposed inverter topologies give high boost factor and less switch stress.

Table 4.2 gives the comparison of the peak dc-link voltage, capacitor voltages, switch stress, and boost factor for the proposed topologies and conventional inverter topologies with the same input voltage and shoot-through duty ratio. The comparison made in Fig. 4.8(a) and Fig. 4.8(b) is based on Table 4.2 and shows that the boost factor of the proposed inverter topologies is higher than the all other mentioned topologies.

Table 4.1: Comparison of component count, nature of input current, inrush current, and common ground for different topologies.

S.No	Topology	Common Ground	Start-up Current	Input Current Nature	Components			
					L	C	D	S
1	ZSI [41]	No	Yes	Discontinuous	2	2	1	6
2	SL-ZSI [49]	No	Yes	Discontinuous	4	2	7	6
3	DA-qZSI [47]	Yes	No	Continuous	3	3	3	6
4	CA-qZSI [47]	Yes	No	Continuous	3	4	2	6
5	High set-up qZSI [69]	Yes	No	Continuous	3	3	3	6
6	EB-ZSI [63]	No	Yes	Discontinuous	4	4	5	6
7	VL-ZSI	No	Yes	Discontinuous	3	3	3	6
8	VL-improved ZSI	Yes	No	Continuous*	3	3	3	6

Note: If maximum boost control method is used [22].

As discussed in Section 4.3.1, the proposed VL-ZSI also suffers from several drawbacks such as discontinuous input current, it does not share common ground with the source, and has large inrush current during the starting condition similar to ZSI [41], SL-ZSI [49], and EB-ZSI [73]. Moreover, the stress across the capacitors is high. In addition, for solar PV grid-connected systems, the proposed VL-ZSI needs an extra LC-low pass filter at the input side due to the discrete input current drawn from the supply, which increases the cost and space requirements [84]. But, the qZSI proposed in [50, 51] for the solar PV systems and proposed VL-IZSI do not require any extra filter at the input side due to continuous* input current drawn from the

supply and they also reduces the switching ripples seen by the solar PV arrays. The VL-I ZSI shown in Fig. 4.2(b) has the following features when compared to VL-ZSI.

- Shares common ground between input source and bridge inverter
- Reduced stress across the capacitors and
- Suppresses the inrush current problem.

The only drawback with the VL-improved ZSI when compare to VL- ZSI is that, the stress across the capacitor C_1 is more.

Table 4.2: Boost factor, voltage stress, input currents, average DC-link current, and inductor current comparison with the same voltage gain and duty ratio D_0.

Para-meter		Topologies for comparison						
		ZSI [41]	SL-ZSI [49]	DA-qZSI [47]	CA-qZSI [47]	EB-ZSI [73]	VL-ZSI	VL-IZSI
Boost Factor	$\frac{\hat{V}_{PN}}{V_{DC}}$	$\frac{1}{(1-2D_0)}$	$\frac{1+D_0}{(1-3D_0)}$	$\frac{1}{(1-2D_0)(1-D_0)}$	$\frac{1}{(1-3D_0)}$	$\frac{1}{(1-4D_0+2D_0^2)}$	$\frac{2}{(1-3D_0)}$	$\frac{2}{(1-3D_0)}$
Switch Stress	$\frac{V_S}{GV_{DC}}$	$2-\frac{1}{G}$	$\frac{2}{-3G+2+\sqrt{9G^2-4G+4}}$	$\frac{2G}{G+1}$	$\frac{3-(1/G)}{2}$	$\frac{4G}{1+\sqrt{8G^2+1}}$	$\frac{3-(2/G)}{2}$	$\frac{3-(2/G)}{2}$
Input Current		$2i_{L1}-I_{PN}$	$2i_{L1}-I_{PN}$	i_{L3}	i_{L3}	$2i_{L1}-I_{PN}$	$i_{L1}+i_{L2}-I_{PN}$	I_{PN}
Avg.DC-Link Current		$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$
DC-Link Voltage		$\frac{V_{DC}}{(1-2D_0)}$	$\frac{V_{DC}(1+D_0)}{(1-3D_0)}$	$\frac{V_{DC}}{(1-2D_0)(1-D_0)}$	$\frac{V_{DC}}{(1-3D_0)}$	$\frac{V_{DC}}{(1-4D_0+2D_0^2)}$	$\frac{2V_{DC}}{(1-3D_0)}$	$\frac{2V_{DC}}{(1-3D_0)}$
Inductor Current		$i_{L1,L2}=\frac{1-D_0}{1-2D_0}I_{PN}$	$i_{L1,L2,L3,L4}=\frac{1-D_0}{1-3D_0}I_{PN}$	$i_{L1,L2}=\frac{1-D_0}{1-2D_0}I_{PN}$ $i_{L3}=\frac{1-D_0}{1-3D_0}I_{PN}$	$i_{L1,L2,L3}=\frac{1-D_0}{1-3D_0}I_{PN}$	$i_{L1,L2}=\frac{1}{(1-D_0)}i_{L3,L4}$	$i_{L1,L3}=\frac{1-D_0}{1-3D_0}I_{PN}$ $i_{L2}=\frac{2(1-D_0)}{1-3D_0}I_{PN}$	
Capacitor Stress	$\frac{V_{C1}}{GV_{DC}}$	1	$\frac{2}{3G+2-\sqrt{9G^2-4G+4}}$	$\frac{3G-2-\sqrt{G^2+2G+1}}{4G}$	$\frac{1-(1/G)}{2}$	$\frac{1+\sqrt{8G^2-1}}{4G}$	$\frac{1}{2}$	$2-(2/G)$
	$\frac{V_{C2}}{GV_{DC}}$	1			$\frac{1-(1/G)}{2}$	$\frac{1+\sqrt{8G^2-1}}{4G}$	1	$\frac{2-(4/G)}{4}$
	$\frac{V_{C3}}{GV_{DC}}$	N.A	N.A	$\frac{4}{G+1+\sqrt{G^2+2G+1}}$	$\frac{1-(1/G)}{2}$	$\frac{4G-1-\sqrt{8G^2-1}}{4G}$	$\frac{1}{2}$	$\frac{1}{2}$
	$\frac{V_{C4}}{GV_{DC}}$	N.A	N.A	N.A	$\frac{3-(1/G)}{2}$	$\frac{4G-1-\sqrt{8G^2-1}}{4G}$	N.A	N.A
Stress	$\frac{V_{Din}}{GV_{DC}}$	$2-\frac{1}{G}$	$\frac{2}{-3G+2+\sqrt{9G^2-4G+4}}$	$\frac{2G}{G+1}$	$\frac{3-(1/G)}{2}$	$\frac{4G}{1+\sqrt{8G^2+1}}$	$\frac{3-(2/G)}{2}$	$\frac{3-(2/G)}{2}$

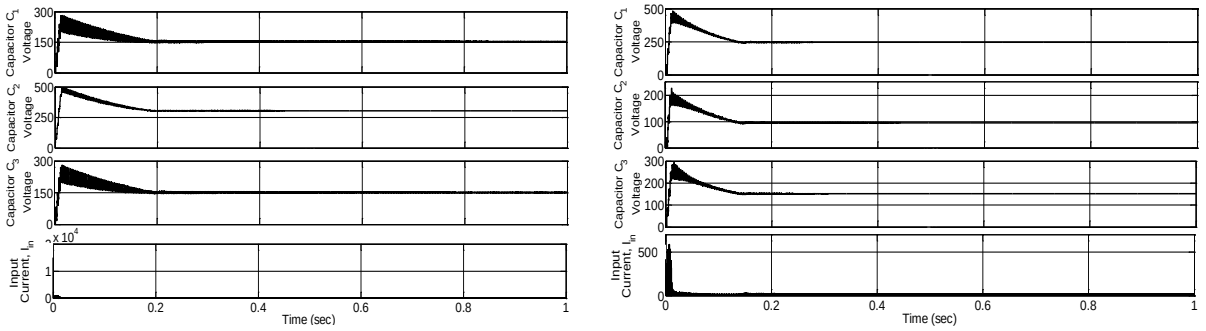
*Note: N.A - Not Applicable

4.6.5 Average DC-link Current and Inductor Current

The expressions for average dc-link current and the inductor current are derived and are compared in Table 4.2. For a given input current and the shoot-through duty ratio, the average dc-link current and the inductor currents for the proposed topologies and high set-up qZSI presented in [69] is same.

4.7 Simulation Results and Discussion

To validate the theoretical analysis of the proposed VL-ZS/improved-ZS inverters, the simulation is carried out in MATLAB/Simulink at V_{DC} = 60 V, D_0 = 0.233, and M = 0.767 with R - L load (R_l = 40 Ω, L_l = 2.5 mH). Simple boost control modulation technique [21] is used for this purpose.



(a) (b)

Fig. 4.10: From to bottom, simulation results of capacitor C_1, C_2, and C_3 voltages and input current I_{in} for: (a) VL-ZSI; (b) VL-improved ZSI.

Fig. 4.10 depicts the simulation results of capacitor voltages (V_{C1}, V_{C2} and V_{C3}) and input current of both the presented topologies from top to bottom respectively. The capacitor voltages obtained in simulations is almost same as the theoretical values obtained in above section. The main advantage of the VL-IZSI topology when compare to VL-ZSI is the stress across the capacitor C_2 and C_3 is less. Moreover, the VL-IZSI suppresses the starting inrush current problem.

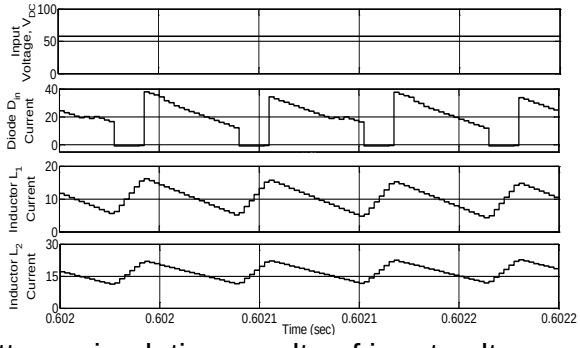


Fig. 4.11: From to bottom, simulation results of input voltage, diode D_{in} current, and inductor L_1, L_2 currents of both proposed VL-ZS/ VL-improved ZSI.

The simulation results of input voltage signal, inductor L_1, L_2 currents, and input diode D_{in} currents are shown in Fig. 4.11. From this figure it is observed that, the inductor currents are linearly increasing in shoot-through state and it is decreasing linearly in the non-shoot-through state. The current flowing through the input diode D_{in} is same for both the presented topologies. During shoot-through state, the current flowing through diode D_{in} is zero due to reverse biased diode.

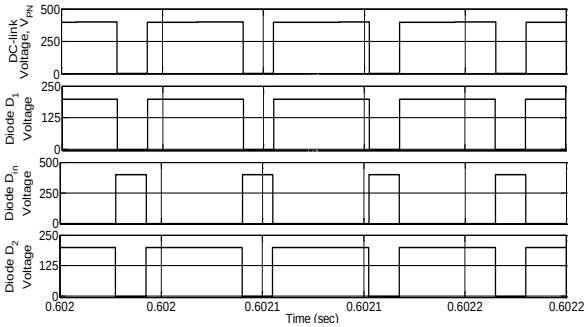


Fig. 4.12: From to bottom, simulation results of dc-link voltage, diode D_1, D_{in} and D_2 voltages of both proposed VL-ZS/ VL-improved ZSI.

As can be observed from (4.11) and (4.21), the peak dc-link voltage of both the topologies is same and therefore, the dc-link voltage, and diode D_1, D_2, and D_{in} voltages respectively from top to bottom is also same which is shown in Fig. 4.12 when the supply voltage is 60 V at D_0 = 0.233. The peak-dc link signal is approximately same as the theoretical value obtained. From this figure, it can be observed that the dc-link voltage is zero in shoot-through state and peak voltage appears across the dc-link during the non-shoot-through state. The diode D_{in} voltage is almost zero (forward voltage of the diode) during non-shoot-through state and during shoot-through state, the voltage across the D_{in} is peak value.

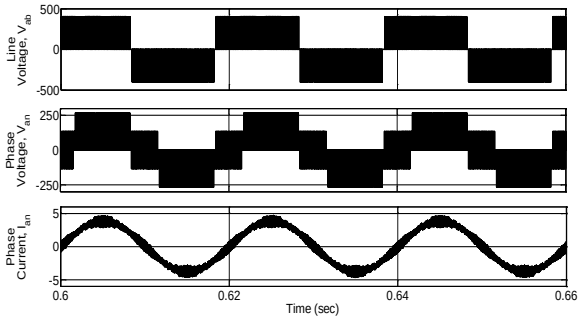


Fig. 4.13: Simulation results of ac-side voltages and current of both proposed VL-ZS/ VL-improved ZSI.

The line voltage (V_{ab}), phase voltage (V_{an}), and current (I_{an}), are depicted in Fig. 4.13 for the resistive-inductive load (R_l = 40 Ω, L_l = 2.5 mH).

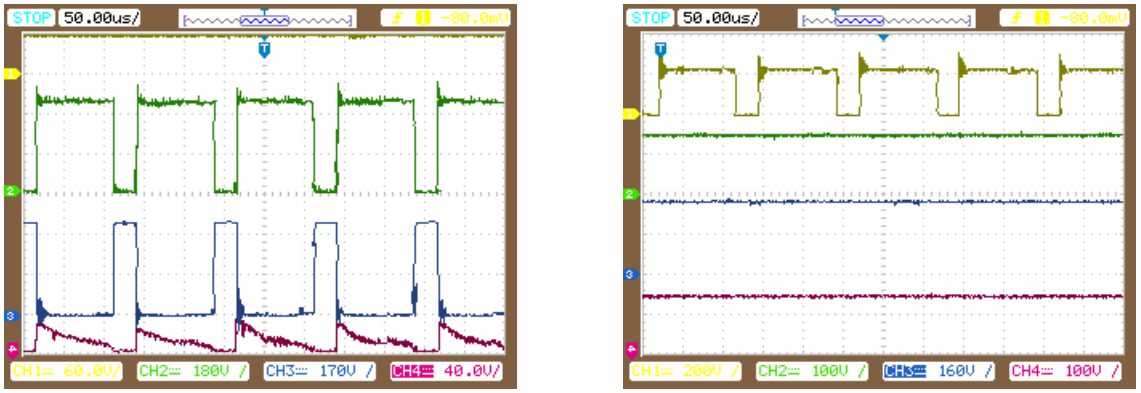
4.8 Experimental Validation and Discussion

In order to validate the simulation results and theoretical analysis, the experimental test is carried out in the laboratory with the parameters shown in Table 4.3.

Table 4.3: Components and parameters specifications used for hardware set-up

S.No	Parameters/Descriptions	Values
1	Input Voltage, V_{DC}	60 V
2	Inductors ($L_1 = L_2 = L_3$)	0.16 mH, 20 A
3	Capacitors ($C_1 = C_2 = C_{VL}$)	1000 µF, 450 V
4	Switching frequency, f_s	4 kHz
5	Fundamental frequency, f	50 Hz
6	Modulation index, M	0.767
7	Shoot-through duty ratio, D_0	0.233
8	Diodes (D_1,D_3, and D_{in}) (16KSR40)	500 V
9	Power MOSFETs (IRF460)	500 V, 21 A, R_{DS}(on) = 0.27 Ω
10	3-phase load per phase values	40 Ω, 2.5 mH.

From top to bottom, the waveforms of input voltage, dc-link voltage, diode D_{in} voltage and input current of VL-ZSI is depicted in Fig. 4.14(a). It can be seen from this figure that, the dc-link voltage is zero in shoot-through state; this is due to the short circuited dc-link and it is peak during non-shoot-through condition. It can also be observed from Fig. 4.14(a), that the input current of VL-ZSI is discontinuous due to the input diode D_{in} (i.e., in shoot-through state, the current drawn from the supply is zero).

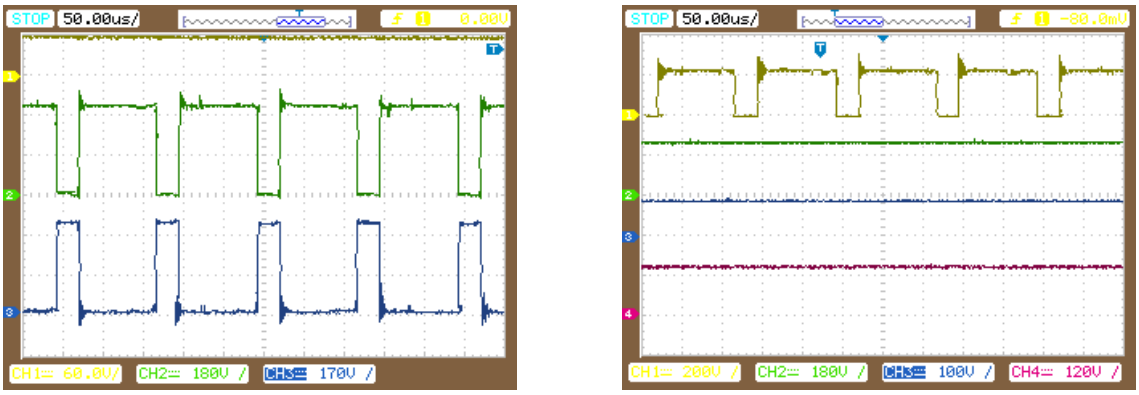


(a) (b)

Fig. 4.14: From top to bottom, Experimental results of VL-ZSI: (a) input, dc-link, and diode D_{in} voltages and input current; (d) diode and capacitor C_1, C_2, and C_3 voltages.

Fig. 4.14(b) show the diode D_1 voltage (top) and the capacitor voltages V_{C1}, V_{C2}, and V_{C3} respectively of the VL-ZSI. It can be observed from this figure that, the

capacitor voltage across C_3 is same as the V_{C1}. Morover, it also seen that; the stress voltage the capacitor C_2 is twice the capacitor C_1 voltage.



(a) (b)

Fig. 4.15: From top to bottom, Experimental results of VL-improved ZSI: (a) input dc, peak dc-link, and diode D_{in} voltages; (b) diode D_1 and capacitor voltages.

Fig. 4.15(a) depicts the input voltage V_{DC}, dc-link voltage, and the diode D_{in} voltages of the VL-improved ZSI respectivily. It is observed from Fig. 4.14(a) and Fig. 4.15(a) that the magnitude of dc-link voltages of the both presented topologies are same and is about 385 V peak approximately.

Fig. 4.15(b) depicts the diode D_1 and capacitor C_1, C_2, and C_3 voltages respectively from top to bottom. It can be observed from this figure that the overall capacitors' voltage stress is less in the case of VL-improved ZSI when compare to the VL-ZSI. Due to parasitic effects of the impedance networks and drop across the semiconductor devices and diodes, the experimental results give less magnitude when compared to simulation results.

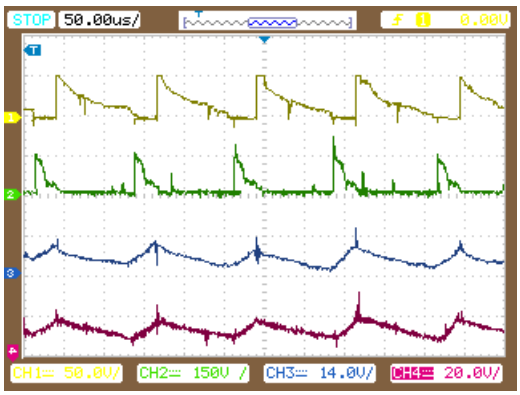


Fig. 4.16: From top to bottom, Experimental results of diode D_{in} current, input current I_{in}, and the inductor L_2, and L_1/L_3 currents of VL improved–ZSI.

The diode D_{in}, input and inductors currents of the proposed VL-improved ZSI are depicted in Fig. 4.16 and it can be seen in this figure that the input current is also discontinuous for simple boost control method (i.e., in zero-state, the input current drawn from the supply is zero). Therefore, to draw continuous input current; the

maximum boost control method is best choice in which all the zero-states can be used as shoot-through states. The inductor currents of both the presented topologies are same and are shown Fig. 4.16.

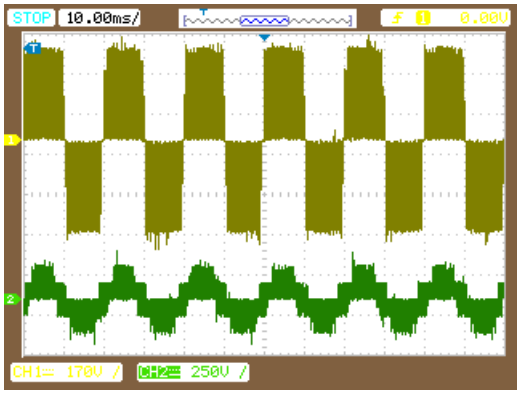


Fig. 4.17: Experimental results of line and phase voltages.

The waveforms of ac-side voltages (i.e., line (top) and phase (bottom)) of the presented topology are depicted in Fig. 4.17. These ac-side voltages are same for both the presented topologies for the same input voltage V_{DC} and shoot-through duty ratio D_0.

4.9 Conclusion

The novel topology of ZSI/improved-ZSI has been proposed in this chapter to boost the voltage gain using voltage-lift unit. For the same input voltage and shoot-through duty ratio, these topologies give high voltage boost and use less number of passive and active components which reduces the space, cost, weight, and complexity of the system. To get the same voltage boost, these proposed VL-ZSI/improved-ZSIs utilize less shoot-through duty ratio and give high modulation index which reduce stress across the semiconductor switches and provide a better quality output waveform and overall, improves the system efficiency. Later, by using VL-improved ZSI, the drawbacks of VL-ZSI have been eliminated. The VL-improved ZSI reduces stress across the capacitors, suppresses the starting inrush current, and shares a common ground with source and bridge circuit. Therefore, the VL-improved ZSI is better suitable for solar PV system to track maximum peak power from the source.

CHAPTER 5: ENHANCED-BOOST QUASI-Z-SOURCE INVERTERS

In this chapter, two topologies are presented for the enhanced-boost quasi-Z-source inverters (EB-qZSIs) which operate in continuous input current configurations with two switched-impedance networks. Similar to enhanced-boost Z-source inverter (EB-ZSI), these presented inverter topologies possess very high boost voltage inversion at low shoot-through duty ratio and high modulation index to provide an improved quality output waveform. Compared to EB-ZSI with two switched Z-source impedance networks, these proposed inverter topologies shares common ground with source and bridge inverter, overcomes the starting inrush problem, draws continuous input current and the lower voltage across the capacitors. Moreover, the input ripple current is negligible. This chapter presents the operating principles, impedance network parameter design, efficiency evaluation and analysis of both configurations of EB-qZSIs with two switched impedance networks and compares them with ZSI, SL-ZSI, DA/CA-qZSIs, and EB-ZSIs. The theoretical analysis is done and is validated through simulation and experimental results.

5.1 Introduction

As discussed in the previous chapter, Z-source inverter (ZSI) was proposed as a buck-boost inverter for single stage DC-to-AC inversion with high boost capability and high EMI immunity [41]. The major factor is the actual physical gain produced by the Z-source inverter. Although, theoretically the voltage gain or boost factor of the inverter can be boosted to any desired value without any upper limit. But, due to the presence of the parasitic influences generally lowers the attainable gain to a finite (sometimes unsatisfactory) value. This degradation is usually more prominent at high gain, high-duty-ratio operating conditions, during which the boost inductor is charged over a longer time duration and discharged (or recovered back to its initial state) within an unrealistically short time interval.

Therefore to enhance the boost factor, the two-inductors (L_1, L_2) in conventional ZSI are replaced with the switched-inductor (SL) cells and was proposed in [49]. The combination of L_1–D_1–L_3–D_3–D_5 acts as top SL cell and the combinations of L_2–D_2–L_4–D_4–D_6 acts as bottom SL cell for switched-inductor ZSI (SL-ZSI). The diode-assisted/capacitor-assisted extended-boost qZSIs (DA/CA-qZSIs) were proposed in [47] with using a large number of passive and active components in the impedance network but its boost factor is not high.

The boost factor further can be heightened in enhanced-boost Z-source inverter (EB-ZSI) with the use of two switched-impedance (SI) networks as proposed in [73].

The combination of L_1–L_3–D_1–D_3–C_1–C_3 forms one (top) switched-impedance network and the combination of L_2–L_4–D_2–D_4–C_2–C_4 forms other (bottom) switched-impedance network as shown in Fig. 5.1. Smaller shoot-through duty ratio was required to get the required voltage boost, therefore, the modulation index is increased which gives good quality output voltage with better total harmonic distortion (THD). This inverter topology gives much heightened voltage boost and it was given as

$$B = \frac{1}{1 - 4D_0 + 2D_0^2} \tag{5.1}$$

The EB-ZSI has following drawbacks [73]:

1. The stress across the capacitor is high,
2. Huge inrush current at start-up condition,
3. Does not share common ground between source and input supply and
4. Provides discontinuous input current.

Similar to traditional ZSI [41] and SL-ZSI [49], the EB-ZSI proposed in [73] provides discontinuous input current due the input series diode D_{in}. But, compared to ZSI [41] and SL-ZSI [49], for the same given input and output voltages, the inverter topology proposed in [73] gives higher voltage boost with very low shoot-through duty ratio and high modulation index which gives low THD. Small shoot-through duty ratio D_0 reduces the conduction losses and improves the overall system efficiency. In addition to that, the proposed novel enhanced-boost quasi Z-source inverters (EB-qZSIs) with two switched-impedance networks inverter topology provides continuous input current which makes it suitable for renewable applications, reduces the capacitor voltage stress to use lower component rating devices, shares common ground with DC source and it overcomes the starting inrush current problem. Moreover, the input current ripple is also zero and it can be negligible.

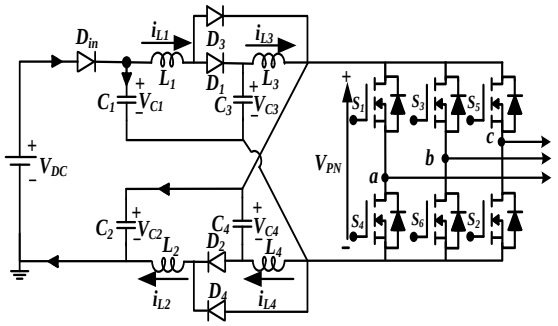


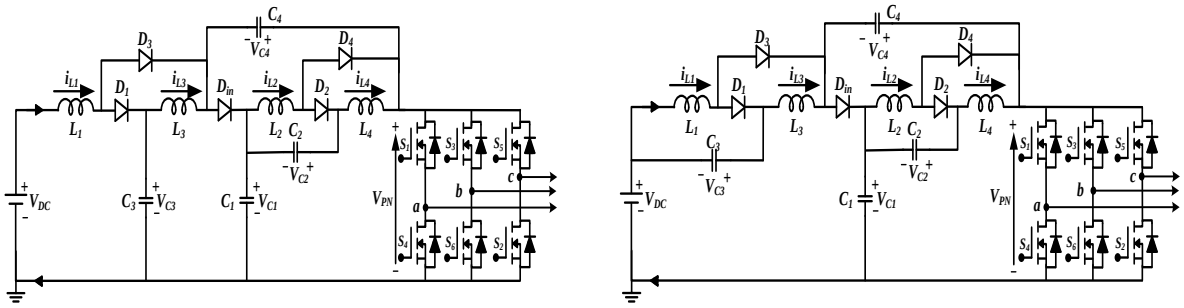
Fig. 5.1: Enhanced-boost Z-source inverter with two switched Z-impedance source network.

The main objective of the proposed topologies is the use of the high number of elements (i.e., both passive and active) with low rating instead of using a low number of elements with high rating in a way that tolerate high voltages in high voltage gains [74]. Due to lack of transformer in the proposed topology, there is no problem about magnetic coupling.

The organization of this chapter is as follows. The circuit diagrams, principle of operations, and derivation of boost factor and voltage gain for both the configurations of EB-qZSIs is explained in Section 5.2 and 5.3 respectively. The description about the inrush current is given in Section 5.4. Section 5.5 describes the impedance network parameter design. Performance comparison is made in Section 5.6. The theoretical validation of the EB-qZSI for configuration-1 is done with simulation and hardware results in Section 5.7 and 5.8 respectively.

5.2 Circuit Diagrams and Explanations of the Enhanced-Boost Quasi Z-Source Inverters

As discussed in above section, the EB-ZSI proposed in [73] is having certain drawbacks. To overcome those mentioned drawbacks, the EB-qZSIs are presented in [74]. Fig. 5.2(a) and Fig. 5.2(b) show the proposed novel inverter topologies for continuous input current configuration-1 and configuration-2 respectively.



(a) (b)

Fig. 5.2: Continuous input current enhanced-boost quasi ZSIs with two-switched impedance networks for: (a) configuration-1; (b) configuration-2.

As shown in Fig. 5.2, both configurations have the same number of components (i.e., four capacitors, four inductors, and five diodes are utilized) as that of the EB-ZSI [73]. The only difference between these proposed topologies is that, the negative polarity of capacitor C_3 is connected to negative terminal of input DC supply in case of configuration-1 and the negative polarity of capacitor C_3 is connected to positive terminal of input DC supply in case of configuration-2. The configuration-1 is used for analysis in this chapter as an example. The boost factor

and voltage stress across the capacitors C_1, C_2, and C_4 are same for both the configurations, but the stress on capacitor C_3 is less (same as capacitor C_2) in case of configuration-2 when compare to continuous input current configuration-1 and can be seen in Table 5.1.

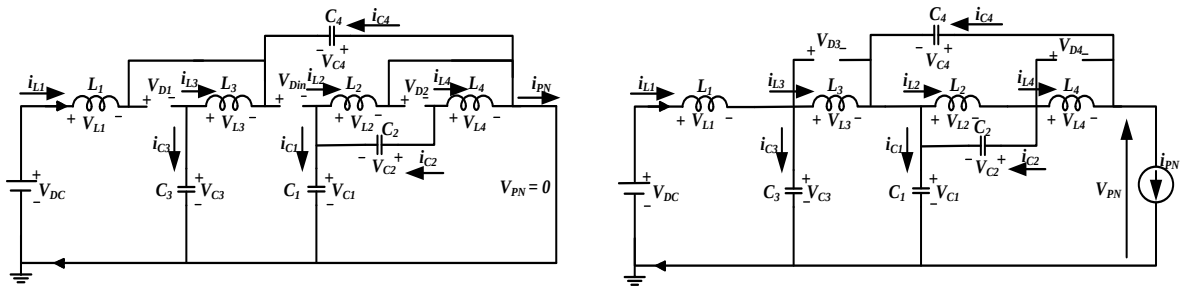
5.3 Steady-state Operations and its Derivations

The configurations of the presented topologies are depicted in Fig. 5.2. The operating principles of the proposed topologies is same as that of the conventional ZSI, having shoot-through (i.e., seven) states in addition to the non-shoot-though states (i.e., traditional six active states and two zero states for three phase system). In order analyze the proposed topologies and to derive the expressions of boost factor and voltage gain, the following assumptions are made;

1. Equivalent series resistances (ESR) of inductances are zero.
2. Equivalent series resistances (ESR) of capacitances are zero.
3. Forward voltage drop of all the diodes are zero.
4. All the semiconductor switches are ideal.
5. Converter should operate in continuous conduction mode (CCM).

5.3.1 Operating Principle for Configuration-1

The equivalent circuits of continuous input current EB-qZSI for configuration-1 during shoot-through state and non-shoot-through states are depicted in Fig. 5.3(a) and (b) respectively.



(a) (b)

Fig. 5.3: Equivalent circuits of the proposed continuous input current configuration-1 enhanced-boost quasi ZSI in: (a) shoot-through; (b) non-shoot-through states.

5.3.1.1 Shoot-Through State

As shown in Fig. 5.3(a), in this shoot-through state both lower and upper power devices of any one–phase or any two–phase or all the three–phase legs are turned on at the same time to boost the input voltage. During this state, the diodes D_{in}, D_1,

and D_2 are OFF, whereas diodes D_3 and D_4 are turned ON. Inductors are charged by the capacitors and these inductors store the electromagnetic energy. By applying Kirchhoff's voltage law (KVL) in the impedance network, the inductor voltages and diode voltages in steady-state condition are as follows:

$$\begin{cases} V_{L1} = L_1 \dfrac{di_{L1}}{dt} = V_{DC} + V_{C4} \\ V_{L2} = L_2 \dfrac{di_{L2}}{dt} = V_{C1} \\ V_{L3} = L_3 \dfrac{di_{L3}}{dt} = V_{C3} + V_{C4} \\ V_{L4} = L_4 \dfrac{di_{L4}}{dt} = V_{C1} + V_{C2} \end{cases} \tag{5.2}$$

$$\begin{cases} V_{Din} = V_{C1} + V_{C4} \\ V_{D1} = V_{D2} = V_{C3} + V_{C4} \end{cases} \tag{5.3}$$

and the dc-link voltage, $V_{PN} = 0$.

5.3.1.2 Non-Shoot-Through State

As shown in Fig. 5.3(b), the non-shoot-through state consists of two-zero state and six-active states. During this state, the diodes D_{in}, D_1, and D_2 are turned ON, whereas the diodes D_3 and D_4 are OFF. The capacitors are charged from input source through inductors. The electromagnetic energy stored in inductors is transferred to the main circuit which boosts the input voltage. The voltage across the inductors and diodes can be written as follows after applying KVL in the impedance network.

$$\begin{cases} V_{L1} = L_1 \dfrac{di_{L1}}{dt} = V_{DC} - V_{C3} \\ V_{L2} = L_2 \dfrac{di_{L2}}{dt} = -V_{C2} \\ V_{L3} = L_3 \dfrac{di_{L3}}{dt} = V_{C3} - V_{C1} \\ V_{L4} = L_4 \dfrac{di_{L4}}{dt} = V_{C2} - V_{C4} \end{cases} \tag{5.4}$$

$$V_{D3} = V_{D4} = V_{C1} - V_{C3} \tag{5.5}$$

The peak dc-link voltage across the three-phase inverter bridge can be represented as

$$V_{PN}^{\wedge} = V_{C1} + V_{C4} \tag{5.6}$$

5.3.1.3 Derivation of Boost Factor and Voltage Gain

In steady-state condition, the average voltage across the inductor L_1 is zero and applying volt-second balance principle to L_1.

$$V_{C3} = \frac{V_{DC} + D_0 V_{C4}}{(1 - D_0)} \tag{5.7}$$

In steady state condition, the average voltage across the inductor L_2 is zero, therefore

$$V_{C2} = \frac{D_0}{(1 - D_0)} V_{C1} \tag{5.8}$$

In steady state condition, the average voltage across the inductor L_3 is also zero which gives

$$V_{C3} + D_0 V_{C4} - (1 - D_0) V_{C1} = 0 \tag{5.9}$$

Similarly, for inductor L_4, the average voltage over one switching period is zero in steady state condition

$$V_{C2} + D_0 V_{C1} - (1 - D_0) V_{C4} = 0 \tag{5.10}$$

Substituting (5.7) into (5.9), yields

$$V_{DC} + V_{C4}(2D_0 - D_0^2) = V_{C1}(1 - D_0)^2 \tag{5.11}$$

Similarly, substituting (5.8) into (5.10), yields

$$V_{C1} = \frac{(1 - D_0)^2}{2D_0 - D_0^2} V_{C4} \tag{5.12}$$

By substituting above equation in (5.11), we will get V_{C4} as

$$V_{C4} = \frac{2D_0 - D_0^2}{1 - 4D_0 + 2D_0^2} \; V_{DC} \tag{5.13}$$

From (5.12),

$$V_{C1} = \frac{(1 - D_0)^2}{1 - 4D_0 + 2D_0^2} V_{DC} \tag{5.14}$$

Similarly, from (5.7) and (5.8), we will get the voltage across the capacitors C_3 and C_2 respectively as

$$V_{C3} = \frac{1 - 3D_0 + D_0^2}{1 - 4D_0 + 2D_0^2} V_{DC} \tag{5.15}$$

$$V_{C2} = \frac{D_0 - D_0^2}{1 - 4D_0 + 2D_0^2} V_{DC} \tag{5.16}$$

Substituting the expressions of capacitor voltages in (5.3) and (5.5), we get the following diode voltages as

$$V_{Din} = \frac{1}{1-4D_0+2D_0^2}V_{DC} \tag{5.17}$$

$$V_{D1} = V_{D2} = \frac{1-D_0}{1-4D_0+2D_0^2}V_{DC} \tag{5.18}$$

$$V_{D3} = V_{D4} = \frac{D_0}{1-4D_0+2D_0^2}V_{DC} \tag{5.19}$$

From (5.13) – (5.14) and (5.6), the peak dc-link voltage across the three-phase inverter bridge can be expressed as

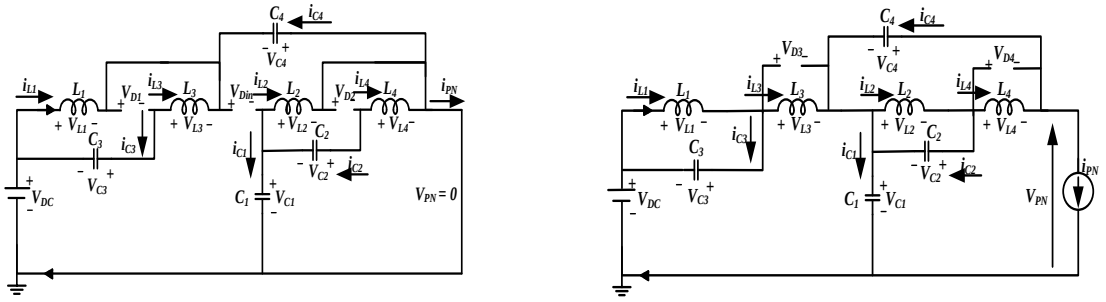
$$\begin{cases} \hat{V_{PN}} = V_{C1}+V_{C4} = \dfrac{1}{1-4D_0+2D_0^2}V_{DC} \\ \hat{V_{PN}} = BV_{DC} \end{cases} \tag{5.20}$$

Therefore, boost factor, B (ratio of $\hat{V_{PN}}/V_{DC}$) of the enhanced-boost qZSI with two switched-impedance networks is given by

$$B = \frac{\hat{V_{PN}}}{V_{DC}} = \frac{1}{1-4D_0+2D_0^2} \tag{5.21}$$

5.3.2 Operating Principle for Configuration-2

To reduce the capacitor stress across the C_3, the negative terminal of capacitor C_3 is connected to positive terminal of supply instead of negative terminal as in configuration-1 by keeping remaining connections same and is shown in Fig. 5.4.



(a) (b)

Fig. 5.4: Equivalent circuits of the proposed continuous input current configuration-2 enhanced-boost quasi ZSI in: (a) shoot-through; (b) non-shoot-through states.

5.3.2.1 Shoot-Through State

The input diode D_{in} and diodes D_1, D_2 are turned OFF due to reverse biased voltages across them; whereas the diodes D_3 and D_4 are ON in this state. The

inductors are charged from parallel capacitors. Inductor current increases linearly in this state. These inductors store the energy during this state. The following equations can be obtained across the inductors and diodes after applying KVL to Fig. 5.4(a).

$$\begin{cases} V_{L1} = L_1 \dfrac{di_{L1}}{dt} = V_{DC} + V_{C4} \\ V_{L2} = L_2 \dfrac{di_{L2}}{dt} = V_{C1} \\ V_{L3} = L_3 \dfrac{di_{L3}}{dt} = V_{DC} + V_{C3} + V_{C4} \\ V_{L4} = L_4 \dfrac{di_{L4}}{dt} = V_{C1} + V_{C2} \end{cases} \tag{5.22}$$

$$\begin{cases} V_{D1} = -V_{L3} = -(V_{DC} + V_{C3} + V_{C4}) \\ V_{D2} = -V_{L4} = -(V_{C1} + V_{C2}) \\ V_{Din} = -(V_{C1} + V_{C4}) \end{cases} \tag{5.23}$$

and the dc-link voltage, $V_{PN} = 0$.

5.3.2.2 Non-Shoot-Through State

The input diode D_{in} and diode D_1, D_2 are turned ON: whereas diodes D_3 and D_4 are OFF in this state. The capacitors are charged from input supply through the inductors. Inductor current decreases linearly, the stored energy in the inductors and input energy boosts the input voltage. After applying the KVL to Fig. 5.4(b), the voltage across the inductors and diodes can be obtained as

$$\begin{cases} V_{L1} = L_1 \dfrac{di_{L1}}{dt} = V_{DC} - V_{C3} \\ V_{L2} = L_2 \dfrac{di_{L2}}{dt} = -V_{C2} \\ V_{L3} = L_3 \dfrac{di_{L3}}{dt} = V_{DC} + V_{C3} - V_{C1} \\ V_{L4} = L_4 \dfrac{di_{L4}}{dt} = V_{C2} - V_{C4} \end{cases} \tag{5.24}$$

$$\begin{cases} V_{D3} = V_{L3} = V_{DC} + V_{C3} - V_{C1} \\ V_{D4} = V_{L4} = V_{C2} - V_{C4} \end{cases} \tag{5.25}$$

5.3.2.3 Derivation of Boost Factor and Voltage Gain

Similar to Section 5.3.1.3, in steady-state condition, the average voltage across all the inductors is zero. From the above equations, the following capacitor voltages can be written as

$$V_{C1} = \frac{(1 - D_0)^2}{1 - 4D_0 + 2D_0^2} V_{DC} \tag{5.26}$$

$$V_{C2} = \frac{D_0 - {D_0}^2}{1 - 4D_0 + 2D_0^2} V_{DC} \tag{5.27}$$

$$V_{C3} = \frac{D_0 - {D_0}^2}{1 - 4D_0 + 2D_0^2} V_{DC} \tag{5.28}$$

$$V_{C4} = \frac{2D_0 - {D_0}^2}{1 - 4D_0 + 2D_0^2} V_{DC} \tag{5.29}$$

From Fig. 5.4(b), the dc-link signal of the impedance network can be obtained by applying the KVL as

$$\hat{V_{PN}} = V_{C1} + V_{C4} \tag{5.30}$$

After substituting the capacitor C_1, C_4 voltages in above equation

$$\hat{V_{PN}} = \frac{1}{1 - 4D_0 + 2D_0^2} V_{DC} \tag{5.31}$$

$$\hat{V_{PN}} = BV_{DC} \tag{5.32}$$

$$B = \frac{1}{1 - 4D_0 + 2D_0^2} \tag{5.33}$$

It is clear from (5.21) and (5.33) that the boost factor of the proposed EB-qZSIs and EB-ZSI [73] is same. The average dc-link signal, $\tilde{V_{PN}}$ of the proposed inverter can be expressed as follows

$$\tilde{V_{PN}} = \frac{1 - D_0}{1 - 4D_0 + 2D_0^2} V_{DC} \tag{5.34}$$

The peak-phase output voltage of the three-phase inverter is expressed by

$$\begin{cases} \hat{V_{an}} = M.\dfrac{\hat{V_{PN}}}{2} \\ \hat{V_{an}} = M.B\dfrac{V_{DC}}{2} \\ \hat{V_{an}} = G\dfrac{V_{DC}}{2} \end{cases} \tag{5.35}$$

where G – is the buck-boost factor or voltage gain and M – is the modulation index.

The overall DC-AC voltage conversion ratio G of the proposed EB-qZSIs with two switched-impedance networks in ideal case in terms of modulation index M can be defined by

$$\text{Voltage gain, } G = M.B = \frac{M}{2M^2 - 1} \tag{5.36}$$

5.4 Suppression of Inrush Current at Start-up Condition

At the starting condition of the conventional ZSI [41], SL-ZSI [49], and EB-ZSI [73] very high inrush current will flows through input diode D_{in} and capacitors (C_1, C_2) which is given in (5.37) due to presence of energy storage elements (capacitors and inductors) in the impedance network.

$$i(t) = \frac{V_{DC}}{R_{eq}} e^{-(\frac{2}{R_{eq}C_{eq}})t} \tag{5.37}$$

where R_{eq} – is the equivalent series resistance of diodes and capacitors (C_1, C_2) and C_{eq} – is the equivalent capacitance of the capacitors (C_1, C_2).

In case of EB-ZSI [73], due to some initial voltage across the capacitors, the huge inrush current will flow through input diode (D_{in}) and feed-forward diodes of the power switches as depicted in Fig. 5.5. Then, capacitors and inductors of impedance network start resonating and generate huge voltage and current spikes.

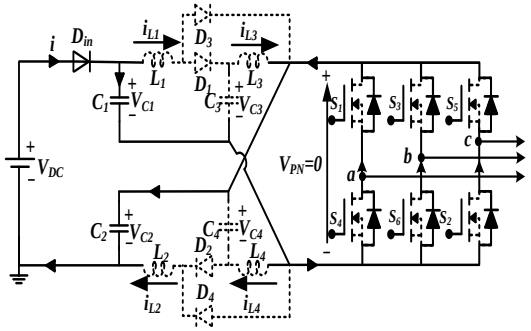


Fig. 5.5: Equivalent circuit for inrush current at starting condition of enhanced-boost ZSI with two switched Z-impedance source network.

But in the proposed EB-qZSIs as the initial voltage across the Z-source capacitors is zero because no current flows to the main circuit at start-up. Although, the inrush current in the proposed EB-qZSI appears due to the resonance of the quasi-Z-source inductors and capacitors, and it is lower than that of the EB-ZSI.

5.5 Designing of Impedance Network Parameters and their Expressions

In the shoot-through state, the inductors are charged by the capacitors and inductor currents increases linearly. The voltage across the inductors in shoot-through state can be written as follows

$$\begin{cases} L_{1,2}\dfrac{di_{L1,L2}}{dt} = V_{L1,L2} = \dfrac{(1-D_0)^2}{(1-4D_0+2D_0^2)}V_{DC} \\ L_{3,4}\dfrac{di_{L3,L4}}{dt} = V_{L3,L4} == \dfrac{(1-D_0)}{(1-4D_0+2D_0^2)}V_{DC} \end{cases} \tag{5.38}$$

Therefore, the inductors in the impedance network of the proposed EB-qZSIs can be designed by

$$\begin{cases} L_{1,2} = \dfrac{T_S D_0}{\Delta i_{L1,L2} k_0} \dfrac{(1-D_0)^2}{(1-4D_0+2D_0^2)} V_{DC} \\ L_{3,4} = \dfrac{T_S D_0}{\Delta i_{L3,L4} k_0} \dfrac{(1-D_0)}{(1-4D_0+2D_0^2)} V_{DC} \end{cases} \tag{5.39}$$

Similarly, the capacitors can be designed as

$$\begin{cases} C_{1,4} = \dfrac{T_S D_0}{\Delta V_{C1,C4} k_0} \dfrac{(2-3D_0+D_0^2)}{(1-4D_0+2D_0^2)} I_{PN} \\ C_{2,3} = \dfrac{T_S D_0}{\Delta V_{C2,C3} k_0} \dfrac{(1-D_0)^2}{(1-4D_0+2D_0^2)} I_{PN} \end{cases} \tag{5.40}$$

where k_0 is the number of shoot-through states over a period, T_S.

5.6 Performance Comparison of the Enhanced-Boost Quasi-ZSIs with other Topologies

The juxtaposition of voltage stress, current stress, volt-sec of the inductors, input ripple current, and the power losses in the impedance network of the proposed enhanced-boost qZSI and the other existing topologies like ZSI [21], SL-ZSI [49], extended-boost ZSI [47], and EB-ZSI [73] with same shoot-through duty ratio D_0 are evaluated in this section.

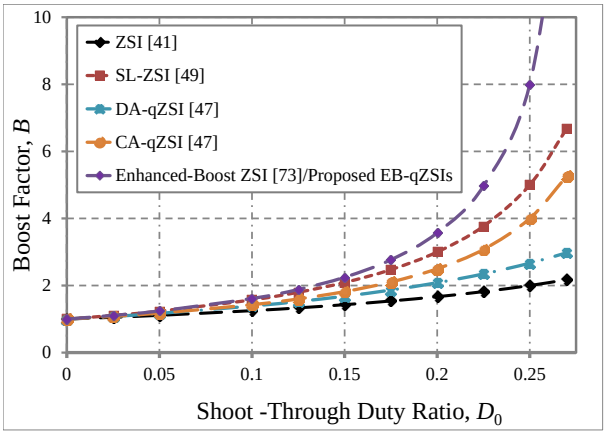


Fig. 5.6: Boost factor comparison of different Z-source inverters with proposed inverter topologies.

5.6.1 Boost Factor and Voltage Gain Comparisons

Fig. 5.6 shows a comparative study of boost factor B versus shoot-though duty ratio of the proposed inverters with existing inverters compared in Table 5.1 and it is contemplated that the boost factor of the enhanced-boost qZSI is higher than ZSI

[21], SL-ZSI [49], DA/CA-qZSI [47] and is same as that of EB-ZSI [73] for the shoot-though duty ratio D_0.

Table 5.1: Comparison of the voltage stress, boost factor, current stress, DC-link voltage, and input current ripple of the proposed inverter with conventional topologies.

Parameter		ZSI [41]	SL-ZSI [49]	Extended-boost qZSIs		EB-ZSI [73]	Proposed EB-qZSIs	
				DA-qZSI [47]	CA-qZSI [47]		Fig. 5.2(a)	Fig. 5.2(b)
Capacitor stresses	C_1	$\frac{1-D_0}{1-2D_0}V_{DC}$	$\frac{1-D_0}{1-3D_0}V_{DC}$	$\frac{D_0}{(1-2D_0)(1-D_0)}V_{DC}$	$\frac{D_0}{1-3D_0}V_{DC}$	$\frac{(1-D_0)^2}{1-4D_0+2D_0^2}V_{DC}$	$\frac{(1-D_0)^2}{1-4D_0+2D_0^2}V_{DC}$	$\frac{(1-D_0)^2}{1-4D_0+2D_0^2}V_{DC}$
	C_2	$\frac{1-D_0}{1-2D_0}V_{DC}$	$\frac{1-D_0}{1-3D_0}V_{DC}$	$\frac{D_0}{(1-2D_0)(1-D_0)}V_{DC}$	$\frac{D_0}{1-3D_0}V_{DC}$	$\frac{(1-D_0)^2}{1-4D_0+2D_0^2}V_{DC}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}V_{DC}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}V_{DC}$
	C_3	NA	NA	$\frac{1}{1-D_0}V_{DC}$	$\frac{1-2D_0}{1-3D_0}V_{DC}$	$\frac{1-D_0}{1-4D_0+2D_0^2}V_{DC}$	$\frac{1-3D_0+D_0^2}{1-4D_0+2D_0^2}V_{DC}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}V_{DC}$
	C_4	NA	NA	NA	$\frac{D_0}{1-3D_0}V_{DC}$	$\frac{1-D_0}{1-4D_0+2D_0^2}V_{DC}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}V_{DC}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}V_{DC}$
Diode stresses	D_1/D_2	NA	$\frac{D_0}{1-3D_0}V_{DC}$	$\frac{V_{D2}}{1-2D_0}$	$\frac{1}{1-3D_0}V_{DC}$	$\frac{1-D_0}{1-4D_0+2D_0^2}V_{DC}$	$\frac{1-D_0}{1-4D_0+2D_0^2}V_{DC}$	$\frac{1-D_0}{1-4D_0+2D_0^2}V_{DC}$
	D_3/D_6	NA	$\frac{1-D_0}{1-3D_0}V_{DC}$	$\frac{2D_0}{(1-2D_0)(1-D_0)}V_{DC}$	NA	$\frac{D_0}{1-4D_0+2D_0^2}V_{DC}$	$\frac{D_0}{1-4D_0+2D_0^2}V_{DC}$	$\frac{D_0}{1-4D_0+2D_0^2}V_{DC}$
	D_4/D_5	NA	$\frac{D_0}{1-3D_0}V_{DC}$	NA	NA	$\frac{D_0}{1-4D_0+2D_0^2}V_{DC}$	$\frac{D_0}{1-4D_0+2D_0^2}V_{DC}$	$\frac{D_0}{1-4D_0+2D_0^2}V_{DC}$
Boost Factor		$\frac{1}{1-2D_0}$	$\frac{1+D_0}{1-3D_0}$	$\frac{1}{(1-2D_0)(1-D_0)}$	$\frac{1}{1-3D_0}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$
Voltage Gain, G		$\frac{M}{2M-1}$	$\frac{2M-M^2}{3M-2}$	$\frac{1}{2M-1}$	$\frac{M}{3M-2}$	$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$
V_{Din}/Switch / dc-link voltage		$\frac{1}{1-2D_0}V_{DC}$	$\frac{1+D_0}{1-3D_0}V_{DC}$	$\frac{1}{(1-2D_0)(1-D_0)}V_{DC}$	$\frac{1}{1-3D_0}V_{DC}$	$\frac{1}{1-4D_0+2D_0^2}V_{DC}$	$\frac{1}{1-4D_0+2D_0^2}V_{DC}$	$\frac{1}{1-4D_0+2D_0^2}V_{DC}$
Input Current, I_{in}		$2i_{L1}-I_{PN}$	$2i_{L1}-I_{PN}$	i_{L3}	i_{L3}	$2i_{L3}-I_{PN}$	i_{L1}	i_{L3}
Inductor Currents		$i_{L1,L2}=\frac{1-D_0}{1-2D_0}I_{PN}$	$i_{L1,L2,L3,L4}=\frac{1-D_0}{1-3D_0}I_{PN}$	$i_{L1,L2}=\frac{1-D_0}{1-2D_0}I_{PN}$ $i_{L3}=\frac{1-D_0}{1-3D_0}I_{PN}$	$i_{L1,L2,L3}=\frac{1-D_0}{1-3D_0}I_{PN}$	$i_{L1,L2}=\frac{(1-D_0)}{1-4D_0+2D_0^2}I_{PN}$ $i_{L3,L4}=\frac{(1-D_0)^2}{1-4D_0+2D_0^2}I_{PN}$	$i_{L1,L2}=\frac{(1-D_0)}{1-4D_0+2D_0^2}I_{PN}$ $i_{L3,L4}=\frac{(1-D_0)^2}{1-4D_0+2D_0^2}I_{PN}$	
Avg. dc-link current, I_{PN}		$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$
Input Current ripple, ΔI_{in}		$\lvert i_{L1}-I_{PN}\rvert$	$\lvert(1-D_0)i_L-I_{PN}\rvert$	0	0	$\lvert(1-2D_0)i_{L3}-(1-D_0)I_{PN}\rvert$	0	0

*NA- Not Applicable

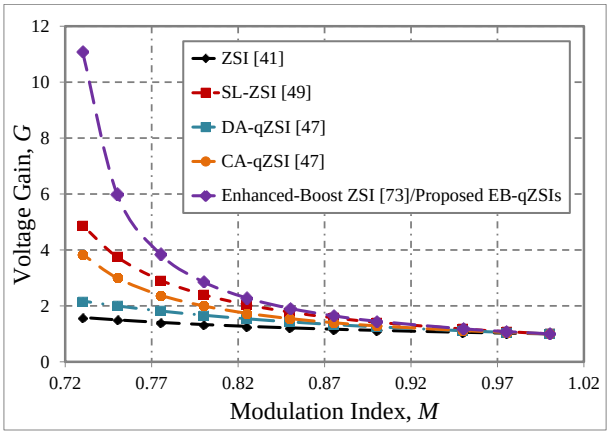


Fig. 5.7: Voltage gain comparison of different Z-source inverters with proposed inverter topologies.

Fig. 5.7 shows the voltage gain *G* versus modulation index comparison of proposed inverter with other inverter topologies like ZSI, SL-ZSI, DA/CA-qZSI, enhanced-boost ZSI and it is observed that the voltage gain of the enhanced-boost qZSI is higher than ZSI, SL-ZSI, DA/CA-qZSI and is same as that of enhanced-boost ZSI for any given modulation index *M*. A high modulation index results in the output waveform enhancement.

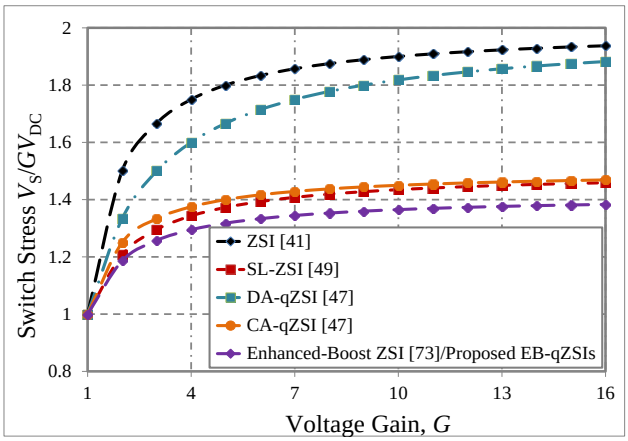


Fig. 5.8: Comparison of switch stress.

5.6.2 Voltage Stress Comparisons

In this subsection; the switch, capacitor, and diode stress of the existing topologies like ZSI [41], SL-ZSI [49], DA/CA-qZSIs [47], and EB-ZSI [73], and the proposed topologies are compared. Table 5.1 compares the expressions of dc-link voltage, capacitor voltages, voltage stress across the diodes, boost factor, switch stress, inductor currents, and input currents of the proposed enhanced-boost qZSI topologies with ZSI, SL-ZSI, CA-qZSI, and EB-ZSI.

5.6.2.1 Switch Stress versus Voltage Gain

The voltage stress across power semiconductor devices can be defined as the ratio of the peak dc-link voltage ($V_{PN}^{\wedge}$) to the minimum DC voltage (GV_{DC}) needed by the traditional ZSI to produce the same AC output voltage at M = 1 [23]. Fig. 5.8 depicts the stress across the semiconductor switches of the proposed inverters and other inverter topologies. From this figure, it can observe that the proposed inverter gives less stress across the switch for same given voltage gain G when compare to the ZSI, SL-ZSI, and DA/CA-qZSI and is same as that of the EB-ZSI.

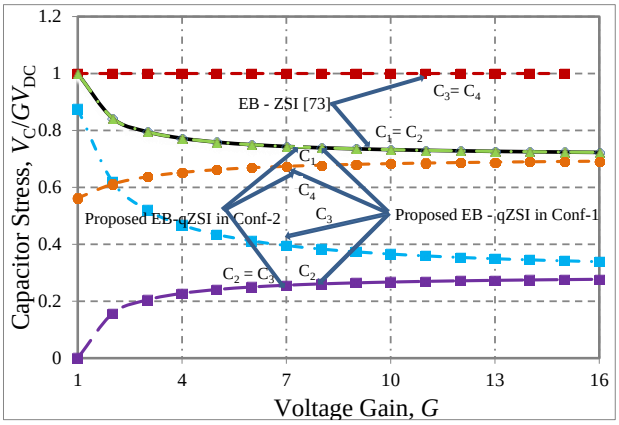


Fig. 5.9: Capacitor voltage stress comparison of enhanced-boost ZSI and proposed enhanced-boost qZSIs.

5.6.2.2 Capacitor Stress versus Voltage Gain

The comparison of the capacitor voltage stresses [23] (ratio of V_C/GV_{DC}) of EB-ZSI and the proposed enhanced-boost quasi-Z-source inverter topologies is shown in Fig. 5.9. This figure shows that the stress across the capacitors is less in proposed inverter when compared with the EB-ZSI [73], therefore lower rating capacitors can be used to reduce the cost and size for the same voltage gain G.

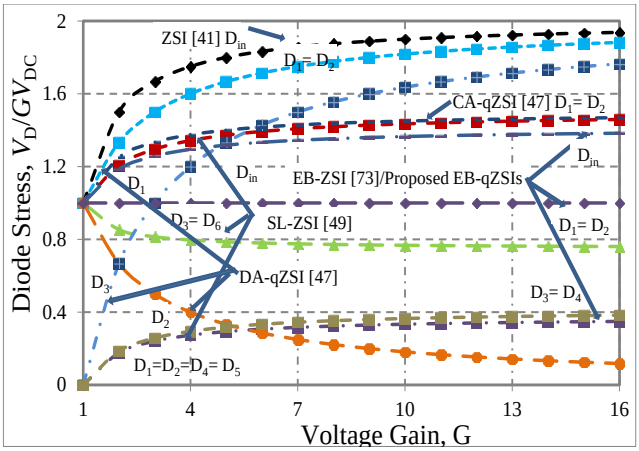


Fig. 5.10: Diode stress comparison of different existing topologies and the proposed topologies.

5.6.2.3 Diode Stress versus Voltage Gain

The diode stress comparison of the proposed enhanced-boost qZSIs with the other existing impedance source inverters is shown in Fig. 5.10. The stresses across the diodes of the proposed topologies are less than the stress across the diodes of ZSI, SL-ZSI and CA-qZSIs and same as that of the EB-ZSI.

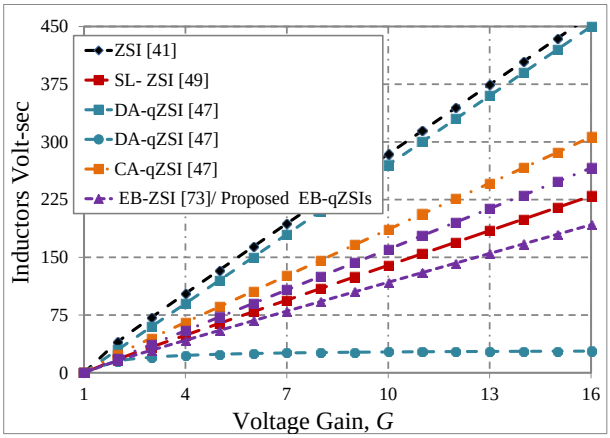


Fig. 5.11: Flux (volt-sec) comparison of the inductors.

5.6.3 Flux (volt-sec) Comparison of the Inductors

The inductors volt-sec (flux) comparison of the proposed topologies and the other five existing topologies are shown in Fig. 5.11. It is observed that the volt-sec of the proposed topology is same as that of the enhanced-boost ZSI and is less when compare to the ZSI, DA-qZSI, and CA-qZSI.

Table 5.2: Input current nature and components (both passive and active) count comparison of the proposed inverter with conventional inverter topologies.

Parameters	ZSI [41]	SL-ZSI [49]	Extended-boost qZSIs		EB-ZSI [73]	Proposed EB-qZSIs	
			DA-qZSI[47]	CA-qZSI[47]		Fig. 5.2(a)	Fig. 5.2(b)
No. of Inductors	2	4	3	3	4	4	4
No. of Capacitors	2	2	3	4	4	4	4
No. of Diodes	1	7	3	2	5	5	5
Power Switches	6	6	6	6	6	6	6
Input Current Nature	Discrete	Discrete	Continuous	Continuous	Discrete	Continuous	Continuous

5.6.4 Average DC-link Current and Inductor Currents

The derivation of the average dc-link current and inductor currents of the all five topologies including the proposed topologies are done and are tabulated in Table 5.1. From this table is can be observed that the average dc-link current and the inductor currents of the enhanced-boost ZSI and the proposed enhanced-boost qZSIs are same.

5.6.5 Component Count

As can observed from Table 5.2, the number of passive (inductors and capacitors) and active (diodes and switches) components used in proposed topologies is same as the EB-ZSI [73]. The number of inductors used in the proposed topologies is more than that of the DA/CA-qZSIs [47]. But, the number of capacitors is same in case of the CA-qZSI and less in case of the DA-qZSI in comparison with the proposed topologies. The diodes used in this inverter are less when compare to SL-ZSI.

5.6.6 Nature of Input Current

The input current nature of the different existing topologies and the presented topologies are tabled in Table 5.2. As can be observed from Fig. 5.1, due the input series diode D_{in} the current drawing from the source is discrete in case of enhanced-boost ZSI [73]. To draw continuous input current from the supply, the enhanced-boost qZSIs are proposed and is shown in Fig. 5.2. Therefore, the nature of input current in the proposed inverter is continuous which improves the life time of the passive components.

5.6.7 Input Current Ripple

As discussed in [51], the input current ripple expression can be derived for the enhanced-boost ZSI and proposed inverter. As can be observed from Table 5.1, the input current for the EB-ZSI [73] is

$$i_{in} = 2i_{L3} - I_{PN} \tag{5.41}$$

From (5.41), the input current in traditional zero states is twice i_{L3} and in the shoot-through state is zero. In steady-state condition, the inductor currents of enhanced-boost ZSI [73] is

$$\begin{cases} i_{L1} = \dfrac{(1-D_0)}{1-4D_0+2D_0^2} I_{PN} \\ i_{L3} = \dfrac{(1-D_0)^2}{1-4D_0+2D_0^2} I_{PN} \end{cases} \tag{5.42}$$

After substituting the value of i_{L3} in (5.41); the average input current of the EB-ZSI [73] is

$$\overline{I_{in}} = \frac{i_{L3}}{(1-D_0)} \tag{5.43}$$

The deviation of average input current and input current is expressed as

$$\Delta i_{in} = \left| i_{in} - \overline{I_{in}} \right| = \left| (1-2D_0) i_{L3} - (1-D_0) i_{PN} \right| \tag{5.44}$$

Similarly, the input current for the proposed inverter in both the states is i_{L1}. Therefore, the average current of the proposed inverter is expressed as

$$\overline{I_{in}} = i_{L1} \quad \text{(or)} \quad \overline{I_{in}} = \frac{i_{L3}}{(1-D_0)} \tag{5.45}$$

This commensurate those of the EB-ZSI [73]. The deviation of the average and its input current can be expressed by

$$\Delta i_{in} = \left| i_{in} - \overline{I_{in}} \right| = 0 \tag{5.46}$$

Therefore, the input ripple current in the proposed enhanced-boost qZSIs is zero and it can be negligible.

5.6.8 Inductance and Capacitance Values

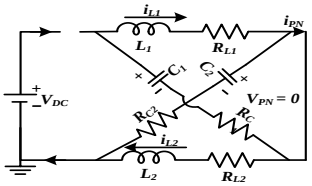
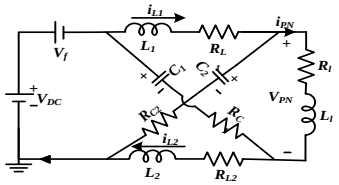
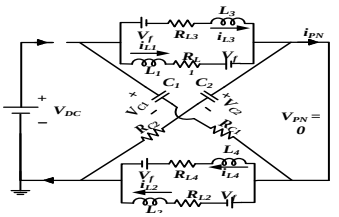
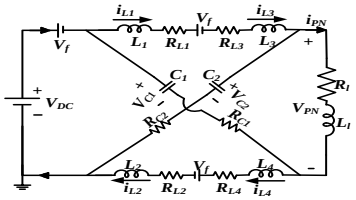
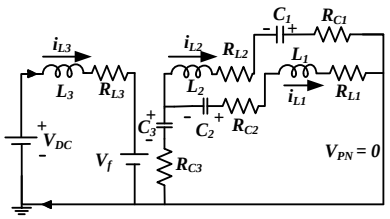
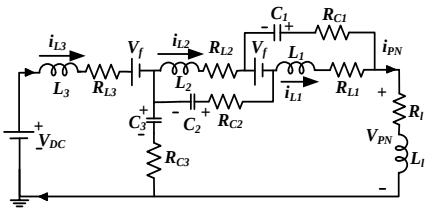
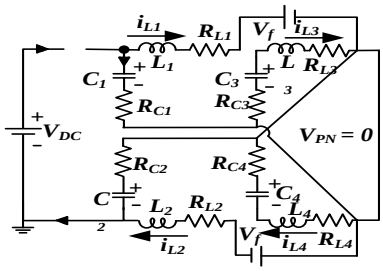
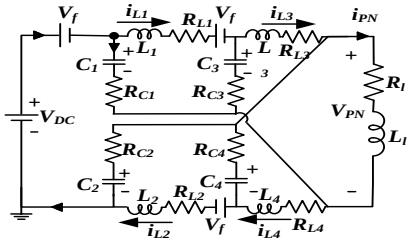
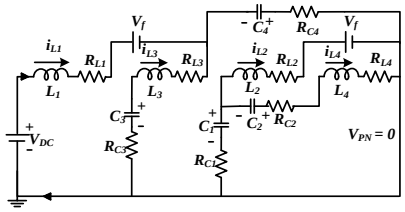
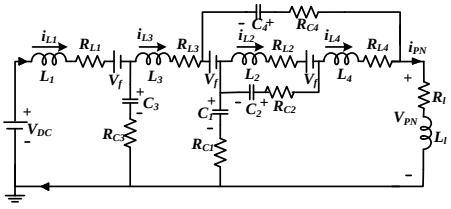
The comparison of inductances and capacitances for the conventional topologies and the proposed topologies are shown in Table 5.3 to achieve the same capacitor voltage ripple and inductor current ripple under the same boost factor [73].

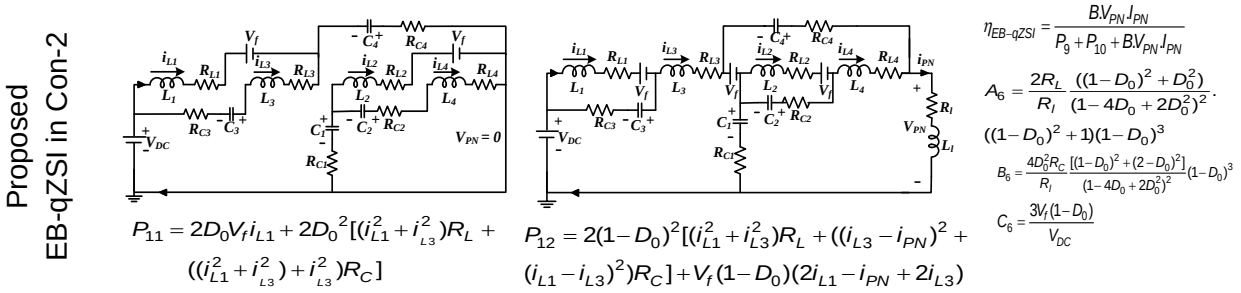
Table 5.3: Comparison of inductances and capacitances and their values for the boost factor, B = 6.6.

Parameters	ZSI [41]	SL-ZSI [49]	Extended-boost qZSIs		EB-ZSI [73]	Proposed EB-qZSIs	
			DA-qZSI [47]	CA-qZSI [47]		Fig. 5.2(a)	Fig. 5.2(b)
Inductances	$L_{1,2} = k_L \frac{D_0(1-D_0)}{(1-2D_0)}$	$L_{1,2,3,4} = k_L \frac{D_0(1-D_0)}{(1-3D_0)}$	$L_{1,2} = k_L \frac{D_0}{(1-3D_0+2D_0^2)}$ $L_3 = k_L D_0$	$L_{1,2,3} = k_L \frac{D_0(1-D_0)}{(1-3D_0)}$	$L_{1,2} = k_L \frac{D_0(1-D_0)^2}{(1-4D_0+2D_0^2)}$ $L_{3,4} = k_L \frac{D_0(1-D_0)}{(1-4D_0+2D_0^2)}$		
Capacitances	$C_{1,2} = k_C \frac{(1-D_0)}{(1-2D_0)}$	$C_{1,2} = k_C \frac{2(1-D_0)}{(1-3D_0)}$	$C_{1,2} = k_C.D_0 .(1-2D_0).(1-D_0)^2$ $C_3 = k_C.2D_0(1-D_0)^2$	$C_1 = k_C.2D_0(1-3D_0)$ $C_{2,4} = k_C.(1-3D_0)$ $C_3 = k_C \frac{2D_0(1-3D_0)}{(1-2D_0)}$	$C_{1,2} = k_C.\frac{D_0(1-D_0)}{1-4D_0+2D_0^2}$ $C_{3,4} = k_C.\frac{D_0(1-D_0)^2}{1-4D_0+2D_0^2}$	$C_{1,4} = k_C.\frac{D_0(2-3D_0+D_0^2)}{1-4D_0+2D_0^2}$ $C_{2,3} = k_C.\frac{D_0(1-D_0)^2}{1-4D_0+2D_0^2}$	
Gain, G	3.8	4.758	4.1	4.73	5	5	
Duty cycle, D_0	0.4242	0.279	0.3782	0.2828	0.24112	0.24112	
Inductance Values	L_1, L_2 =1.289mH	L_1, L_2, L_3, L_4 = 0.987 mH	L_1, L_2 = 1.99 mH, L_3 = 0.302 mH	L_1, L_2 , L_3 = 1.07 mH	L_1, L_2 = 0.731 mH, L_3, L_4 = 0.9643mH	L_1, L_2 = 0.731 mH, L_3, L_4 = 0.9643mH	
Capacitance Values	C_1, C_2 = 4747µF	C_1, C_2 = 9818 µF	C_1, C_2 = 45 µF C_3 = 366 µF	C_1 =107µF, C_3=246.8 µF C_2, C_4=190 µF	C_1, C_2 = 1507µF, C_3, C_4 = 1143.4µF	C_1, C_4 = 2650 µF, C_3, C_2 = 1143.4 µF	

$K_L = V_{DC} / k_i f_0 \overline{i_{in}}$, $K_C = \overline{i_{in}} / V_{DC} k_v f_0$ where k_i – is defined as the ratio of the peak-to-peak inductor current ripple to the average current of the inductor and the factor k_v – is defined as the ratio of the peak-to-peak capacitor voltage ripple to the average voltage of capacitor, f_0 is the operating frequency, which is twice the switching frequency f_s.

Table 5.4: Expression for the efficiency of all topologies.

Topologies	Equivalent circuits and their expressions in: Shoot-through state	Equivalent circuits and their expressions in: Non-shoot-through state	Efficiency (η)
ZSI[41]	 $P_1 = 2D_0^2 i_L^2 (R_L + R_C)$	 $P_2 = 2(1-D_0)^2[i_L^2 R_L + (i_L - i_{PN})^2 R_C] + V_f(1-D_0)(2i_L - i_{PN})$	$\eta_{ZSI} = \frac{B.V_{PN} I_{PN}}{P_1 + P_2 + B.V_{PN} I_{PN}}$ $\eta_{ZSI} = \frac{1}{A_1 + B_1 + C_1 + 1}$ $A_1 = \frac{2R_L}{R_l}\frac{(1-D_0)^3}{(1-2D_0)^2}[(1-D_0)^2 + D_0^2]$ $B_1 = \frac{4R_C}{R_l}\frac{D_0^2(1-D_0)^3}{(1-2D_0)^2}$; $C_1 = \frac{V_f(1-D_0)}{V_{DC}}$
SL-ZSI [49]	 $P_3 = 4D_0^2 i_L^2 (R_L + 2R_C) + 4D_0 V_f i_L$	 $P_4 = 2(1-D_0)^2[2i_L^2 R_L + (i_L - i_{PN})^2 R_C] + V_f(1-D_0)(4i_L - i_{PN})$	$\eta_{SL-ZSI} = \frac{B.V_{PN} I_{PN}}{P_3 + P_4 + B.V_{PN} I_{PN}}$ $\eta_{SL-ZSI} = \frac{1}{A_2 + B_2 + C_2 + 1}$ $A_2 = \frac{4R_L}{R_l}\frac{(1-D_0)^3}{(1-3D_0)^2}[(1-D_0)^2 + D_0^2]$ $B_2 = \frac{16R_C}{R_l}\frac{D_0^2(1-D_0)^3}{(1-3D_0)^2}$; $C_2 = \frac{3V_f(1-D_0)}{V_{DC}}$
DA-qZSI [47]	 $P_5 = D_0^2[(2i_{L1}^2 + i_{L3}^2)R_L + 6i_{L1}^2 R_C] + D_0 V_f i_{L3}$	 $P_6 = V_f(1-D_0)(2i_{L1} - i_{PN} + i_{L3}) + (1-D_0)^2 .$ $[(2i_{L1}^2 + i_{L3}^2)R_L + (2(i_{L1} - i_{PN})^2 + (i_{L3} - i_{PN})^2)R_C]$	$\eta_{DA-qZSI} = \frac{B.V_{PN} I_{PN}}{P_5 + P_6 + B.V_{PN} I_{PN}}$ $\eta_{DA-qZSI} = \frac{1}{A_3 + B_3 + C_3 + 1}$ $A_3 = \frac{R_L}{R_l}[3 + 22D_0^2 - 16D_0].$ $\frac{(1-D_0)^3((1-D_0)^2 + D_0^2)}{(1-2D_0)^2.(1-3D_0)^2}$ $B_3 = \frac{4D_0^2 R_C}{R_l}\frac{(3+22D_0^2-16D_0)}{(1-2D_0)^2.(1-3D_0)^2}(1-D_0)^3$ $C_3 = \frac{V_f(1-D_0)^2}{V_{DC}}\frac{(2-5D_0)}{(1-3D_0)}$
EB-ZSI [73]	 $P_7 = 2[D_0^2(i_{L1}^2 + i_{L3}^2)(R_L + R_C) + D_0 V_f i_{L1}]$	 $P_8 = 2(1-D_0)^2[(i_{L1}^2 + i_{L3}^2)R_L + ((2i_{L3} - i_{L1} - i_{PN})^2 + (i_{L1} - i_{L3})^2)R_C] + V_f(1-D_0)(2i_{L1} - i_{PN} + 2i_{L3})$	$\eta_{EB-ZSI} = \frac{B.V_{PN} I_{PN}}{P_7 + P_8 + B.V_{PN} I_{PN}}$ $\eta_{EB-ZSI} = \frac{1}{A_4 + B_4 + C_4 + 1}$ $A_4 = \frac{2R_L}{R_l}\frac{((1-D_0)^2 + D_0^2)}{(1-4D_0+2D_0^2)^2}.$ $((1-D_0)^2 + 1)(1-D_0)^3$ $B_4 = \frac{4D_0^2 R_C}{R_l}\frac{(1-D_0)^3((1-D_0)^2+1)}{(1-4D_0+2D_0^2)^2}$; $C_4 = \frac{3V_f(1-D_0)}{V_{DC}}$
Proposed EB-qZSI in Con-1	 $P_9 = 2D_0 V_f i_{L1} + 2D_0^2[(i_{L1}^2 + i_{L3}^2)R_L + ((i_{L1}^2 + i_{L3}^2) + i_{L3}^2)R_C]$	 $P_{10} = 2(1-D_0)^2[(i_{L1}^2 + i_{L3}^2)R_L + ((i_{L3} - i_{PN})^2 + (i_{L1} - i_{L3})^2)R_C] + V_f(1-D_0)(2i_{L1} - i_{PN} + 2i_{L3})$	$\eta_{EB-qZSI} = \frac{B.V_{PN} I_{PN}}{P_9 + P_{10} + B.V_{PN} I_{PN}}$ $\eta_{EB-qZSI} = \frac{1}{A_5 + B_5 + C_5 + 1}$ $A_5 = \frac{2R_L}{R_l}\frac{((1-D_0)^2 + D_0^2)}{(1-4D_0+2D_0^2)^2}.$ $((1-D_0)^2 + 1)(1-D_0)^3$ $B_5 = \frac{4D_0^2 R_C}{R_l}\frac{[(1-D_0)^2 + (2-D_0)^2]}{(1-4D_0+2D_0^2)^2}(1-D_0)^3$ $C_5 = \frac{3V_f(1-D_0)}{V_{DC}}$



where R_{L1}= R_{L2}= R_{L3}= R_{L4}= R_L (= 92 mΩ) – is the ESR of inductors, R_{C1} = R_{C2} = R_{C3} = R_{C4} = R_C (= 120 mΩ) – is the ESR of capacitors, V_f (= 1.3 V) – is the forward voltage drop of the diode, I_L – is the inductor currents, and I_{PN} –is the peak dc-link current and $P_{1\text{-}12}$ represents the power losses in the impedance network.

For the input voltage of 60 V, $\bar{i}_{in}$ = 15 A, the factors k_i = 50%, k_v = 2% and the required shoot-through duty ratio to achieve the boost factor B = 6.6. The values of inductances and capacitances for the conventional topologies and the proposed topology are summarized in Table 5.3. The compiled value of inductances required at the proposed topologies is slightly higher than those of both the ZSI [41] and CA-qZSI [47] and less than that of the SL- ZSI [49] and DA-qZSI [47], but same as the EB-ZSI [73]. The capacitance value for the proposed topology is much lower than the summarized value of capacitances required at the ZSI and SL-ZSI topologies and is higher than the EB-ZSI.

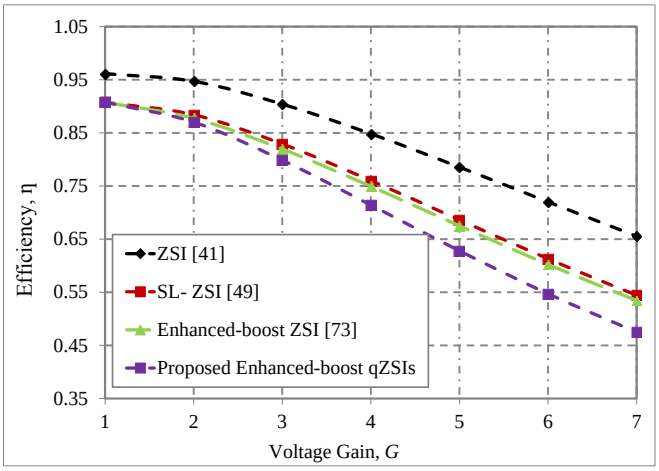


Fig. 5.12: Efficiency comparison of different Z-network topologies.

5.6.9 Impedance Network Power Loss Analysis

In order to analyze the power losses in an impedance network of the all four topologies and the proposed inverter topologies, the equivalent series resistances (ESR) of inductors and capacitors are assumed to be same for all the topologies [60]. Also, the forward conduction loss of the all the diodes is same for all the compared topologies. Table 5.4 shows the expression for the efficiency of all topologies. The efficiency of the proposed topology is less than the other topologies which can be

observed from Table 5.4. This is due to higher value of capacitance in the proposed topology and hence results in more capacitor loss.

For a given duty ratio D_0, the losses in the proposed topology are higher than the losses in ZSI [41], extended-boost ZSI [47], SL-ZSI [49], and EB-ZSI [73]. Power loss analysis of the impedance network for all the five topologies including the proposed inverter is done in Table 5.4 and is compared in Fig. 5.12. From this table, it is observed that for a given input voltage and voltage gain, the losses in the proposed topology is higher than the ZSI, SL-ZSI, extended-boost ZSI, and EB-ZSI which decreases the efficiency of the proposed topology and is shown in Fig. 5.12.

For the purpose of comparison, the efficiency of the proposed topology and the other existing topologies were calculated randomly by considering the resistive load of 10 Ω and were plotted in Fig. 5.12. To compare the calculated efficiency of the proposed inverter topology with the measured values, the Fig. 5.12 is plotted at the resistive load of 60 Ω corresponding to 600 W.

5.7 Simulation Results and Discussions

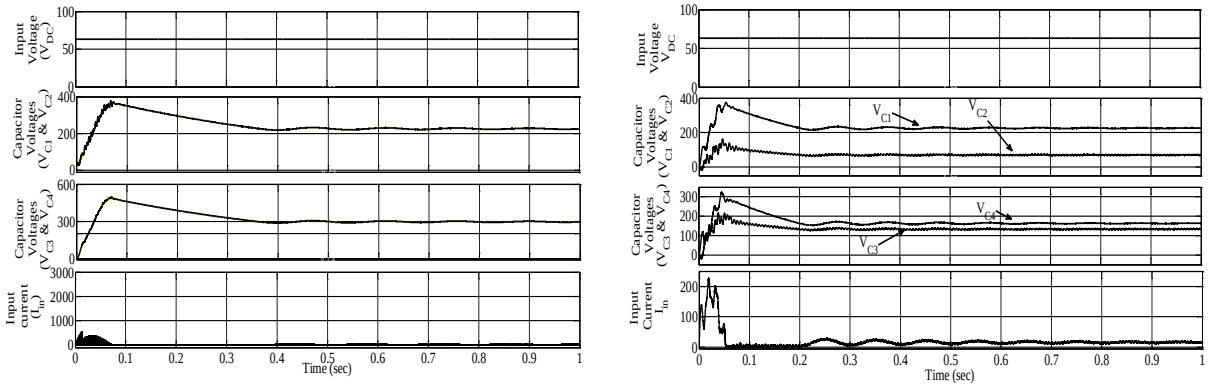
To validate the theoretical analysis discussed in Subsection 5.3.1, the simulation is carried out with simple boost control method [41] in MATLAB/Simulink with the parameters as depicted in Table 5.5 at 10 kHz switching frequency. To produce the output phase voltage of 110 Vrms from the 60 V input dc voltage with simple boost control for the proposed inverter, a shoot-through duty ratio D_0 = 0.24112 is needed at modulation index M = 0.75888.

Table 5.5: Components and parameters used for the simulation and hardware.

S.no	Parameters/Descriptions	Values[a]
1	Input voltage, V_{DC}	60 V
2	Inductors ($L_1 = L_2 = L_3 = L_4$)	1 mH
3	Capacitors ($C_1 = C_2 = C_3 = C_4$)	2200 μF
4	Switching frequency, f_s	4 kHz
5	Fundamental frequency, f	50 Hz
6	Modulation index, M	0.75888
7	Shoot-through duty ratio, D_0	0.24112
8	Diodes (D_1, D_2, D_3, D_4 and D_{in}) (25NSR60)	600 V, 25 A
9	Power MOSFETs (IRF460)	500 V, 21 A, R_{DS}(on)=0.27Ω
10	Load	R_l = 40 Ω, L_l = 2.5 mH

[a]Values; V = volt, H = henry, F = farad, m = milli, μ = micro, k = kilo, Ω = ohm, Hz = hertz, A = ampere.

The continuous input current EB-qZSI configuration-1 is used for theoretical, simulation and experimental analysis. Thus, from (5.13) - (5.19) it can be obtained as: V_{C1} = 226.2 V, V_{C2} = 72.5 V, V_{C3} = 132.6 V, and V_{C4} = 170 V and the diode D_{in}, D_1/D_2, and D_3/D_4 voltages are 396 V, 300.5 V, and 95.5 V respectively. Similarly, from (5.32) – (5.33) and (5.36) we can obtain V_{PN} = 396.2 V, B = 6.6, and G = 5 respectively.



(a) (b)

Fig. 5.13: Simulation results of: (a) enhanced-boost ZSI [73]; (b) proposed enhanced-boost qZSI with M = 0.75888 and D_0 = 0.24112.

The simulation results of input voltage, capacitor (C_1, C_2, C_3, and C_4) voltages, and input current I_{in} for the EB-ZSI [73] and the proposed enhanced-boost qZSI are shown in Fig. 5.13(a) and (b) respectively, when M = 0.75888. From Fig. 5.13(a) for the EB-ZSI [73], the capacitor C_1/C_2 and C_3/C_4 voltages are boosted to 226 V and 300 V respectively in steady-state condition and huge inrush current occurs at the start-up condition. The initial voltage of capacitors C_1 and C_2 is 19 V and 43 V respectively, and the resonance of the Z-source inductors and capacitors starts. The huge inrush current flows through series diode D_{in} and the capacitors C_1, C_2 as shown in Fig. 5.5. From Fig. 5.13(b) for the proposed enhanced-boost qZSI, the capacitor C_1, C_2, C_3, and C_4 voltages are boosted to 226 V, 71 V, 130.5 V, and 168 V respectively in steady-state condition and there exists certain inrush current occurs at the start-up. The inrush current in the proposed enhanced-boost qZSI appears due to the resonance of the quasi-impedance networks; however, the inrush current of the proposed enhanced-boost qZSI is lower than that of the EB-ZSI due to the capacitor C_1 and C_2 have no initial value because no current flows to the main circuit at start-up.

It can be observed from Fig. 5.14, that the simulation results of dc-link voltage and capacitor voltages of the proposed topology are almost same as that of the theoretical values obtained. The peak dc-link voltage is 393 V in the non-shoot-

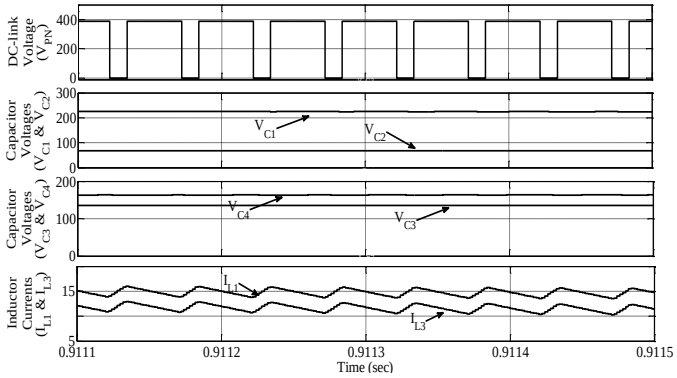


Fig. 5.14: From top to bottom: Simulation results of dc-link voltage (V_{PN}), capacitor voltages (V_{C1}, V_{C2}, V_{C3}, and V_{C4} respectively), and inductor currents (I_{L1} and I_{L3}).

-through period and it is zero in shoot-through state and the voltages across the capacitors C_1, C_2, C_3, and C_4 are 225 V, 71 V, 130.5 V, and 168 V respectively in a steady-state condition. Fig. 5.14 also shows that the inductors are charged in shoot-through state and in the non-shoot-through state, the energy stored in these inductors are transferred to the main circuit.

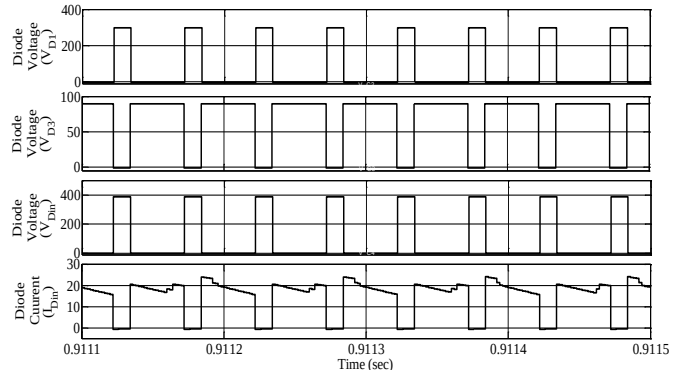


Fig. 5.15: From top to bottom: Simulation results of diode voltages (V_{D1}, V_{D3}, and V_{Din}) and diode D_{in} current in steady state condition.

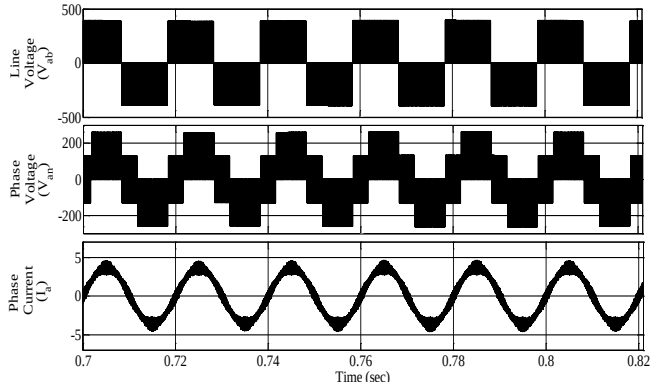


Fig. 5.16: From top to bottom: Simulation results of line voltage (V_{ab}), phase-voltage (V_{an}) and load current without filter.

The diode (D_1/D_2, D_3/D_4, and D_{in}) voltages and I_{Din} current are shown in Fig. 5.15. It can be observed from these results, the diode D_1/D_2, D_3/D_4, and D_{in} voltages are 292 V, 94.5 V, and 393 V respectively in a steady-state condition. The results

obtained in simulation results are matching with the values obtained in the theoretical analysis. The simulation waveforms of line voltage (V_{ab}), phase voltage (V_{an}), and phase current (I_a) are shown in Fig. 5.16.

Fig. 5.17: Photograph of experimental setup.

5.8 Experimental Validation and Discussions

To validate the theoretical analysis and simulation results discussed in Section 5.7 of the proposed enhanced-boost qZSI, the laboratory test is performed for the circuit shown in Fig. 5.2(a) with the parameters shown in Table 5.5 using simple boost control method [41]. The firing pulses to proposed inverter switches are generated using dSPACE DS1104 based hardware environment. The experimental prototype is shown in Fig. 5.17 in order to conduct the test on the proposed enhanced-boost qZSI and the results are taken for V_{DC} = 60 V, D_0 = 0.24112 and M = 0.75888.

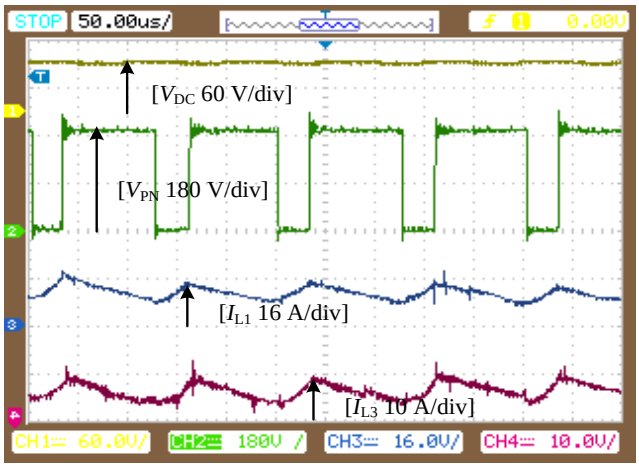


Fig. 5.18: From top to bottom: Experimental results of input voltage, dc-link voltage, and inductor (L_1, L_3) currents respectively.

Fig. 5.18 depicts from top to bottom, the input voltage, peak dc-link voltage, and inductor L_1, L_3 currents waveforms. The dc-link voltage is boosted to 390 V from 60 V

input voltage at modulation index of 0.75888. It is also shown in Fig. 5.18, the inductor currents are increasing in shoot-through state and are decreasing in non-shoot-through state, which represents inductors are charging and discharging during shoot-through and non-shoot-through states respectively. The Fig. 5.19 depicts the capacitor voltages V_{C1}, V_{C2}, V_{C3}, and V_{C4} respectively (from top to bottom) and is slightly less than the simulation results.

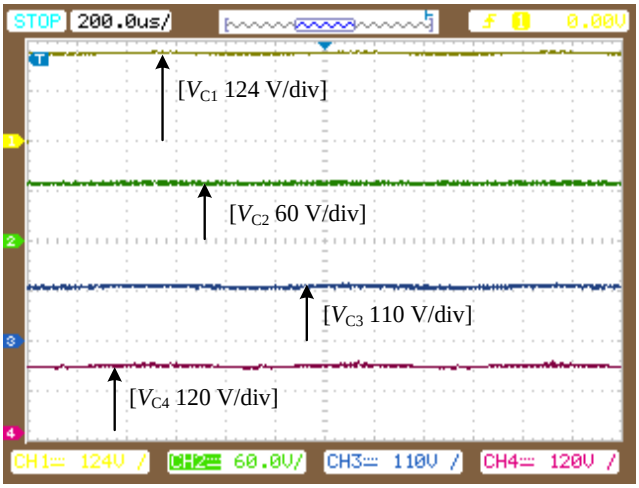


Fig. 5.19: From top to bottom: Experimental results of capacitor C_1, C_2, C_3, and C_4 voltages respectively.

The line voltage (V_{ca}), phase voltage (V_{an}), and phase current (i_a) are depicted in Fig. 5.20(top to bottom) for the load parameters as mentioned in Table 5.5. The values obtained in the experimental results are less than the values obtained in simulation results and theoretical analysis. This is due to the drop across the diodes, semiconductor power switches, and parasitic resistances of the inductors and capacitors.

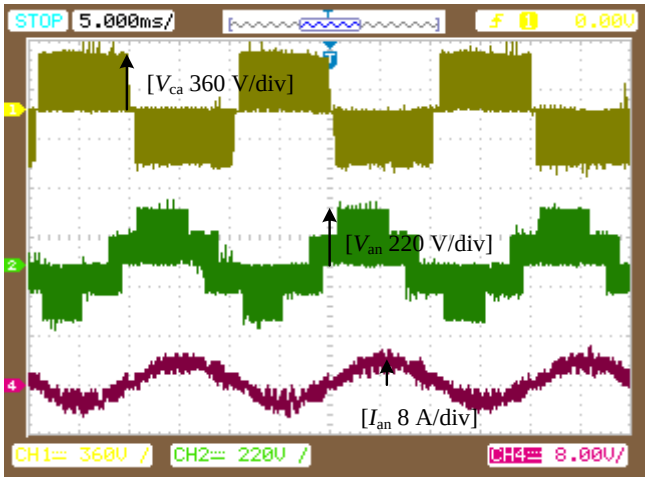
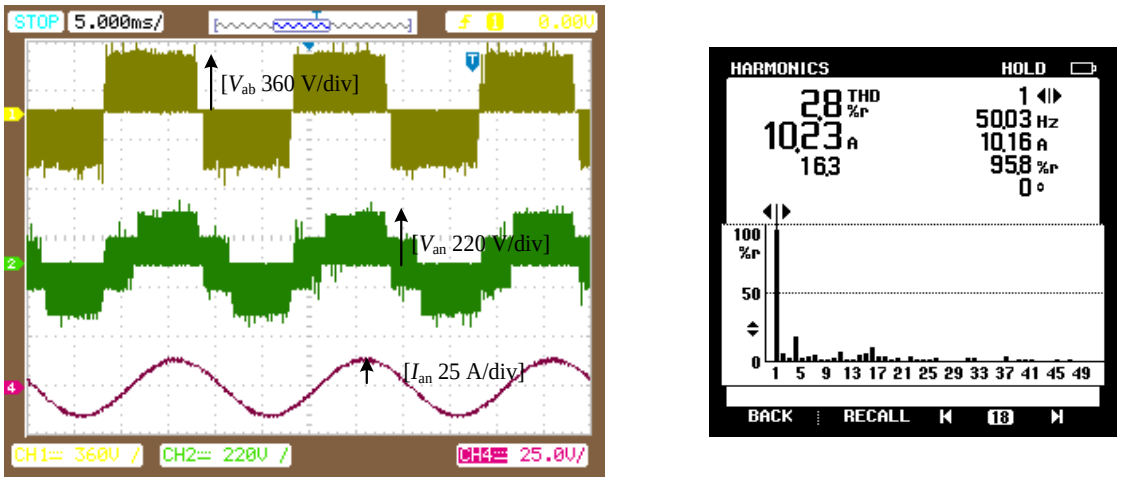


Fig. 5.20: From top to bottom: Experimental results of line-voltage, phase-voltage, and phase-current respectively.

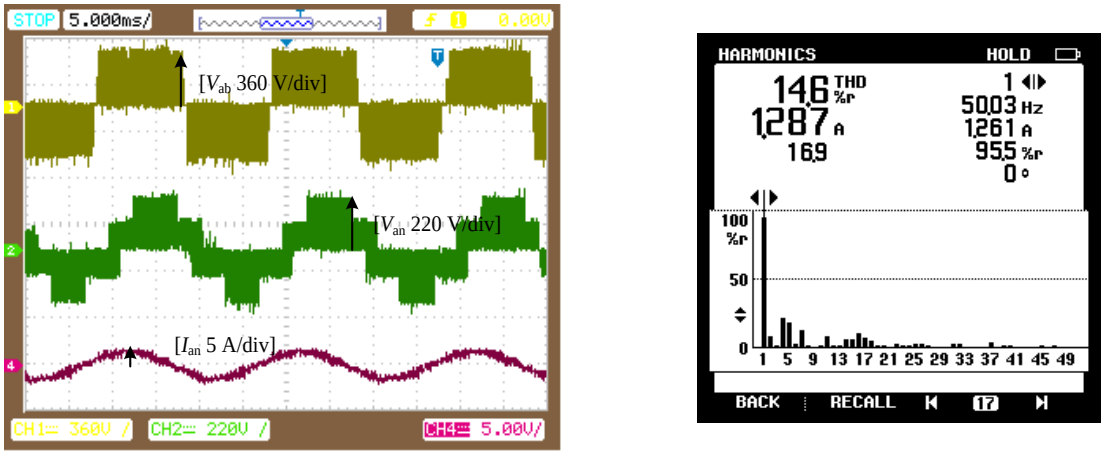
The performance of the proposed topology is also tested with different kind of loads such as lagging, leading, and nonlinear loads of three-phase star (Y-) connected *R-L*, *R-L-C*, and diode bridge rectifier with *R-L* load respectively. Fig. 5.21(a) depicts the load voltage (V_{ab}), phase voltage (V_{an}) and the phase current of phase-A (I_a) with three-phase load parameters of 10 Ω and 10 mH. It can be clearly seen that load current lags the corresponding phase voltage by a phase shift of 17^0. Fig. 5.21(b) indicates the %THD as 2.8 of output phase current.



(a) (b)

Fig. 5.21: Experimental results for lagging load: (a) From top to bottom: line-voltage, phase-voltage, and phase-current; (b) Its output current THD.

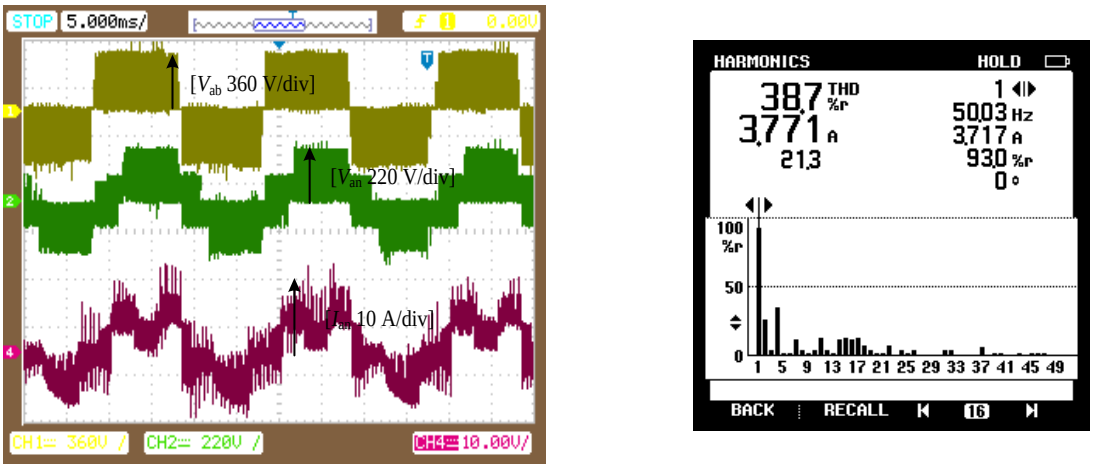
Similarly, the results with three-phase leading load of 50 Ω, 5 mH and 45 μF are presented in Fig. 5.22(a), shows the phase current leads the corresponding phase voltage by a phase shift of 53^0 and hold the %THD value of 14.6 as shown in Fig. 5.22(b).



(a) (b)

Fig. 5.22: Experimental results for leading load: (a) From top to bottom: line-voltage, phase-voltage, and phase-current; (b) Its output current THD.

In the case of a nonlinear load of three-phase diode bridge rectifier feeding to *R-L* load of 40 Ω and 5 mH, the phase current is much distorted than the lagging and leading load conditions which are shown in Fig. 5.23(a), with THD value of 38.7% as shown in Fig. 5.23(b).



(a) (b)

Fig. 5.23: Experimental results for non-linear load: (a) From top to bottom: line-voltage, phase-voltage, and phase-current; (b) Its output current THD.

The starting inrush current of the proposed enhanced-boost qZSI topology is captured with the help of Fluke 43B Power Quality Analyzer and is depicted in Fig. 5.24.

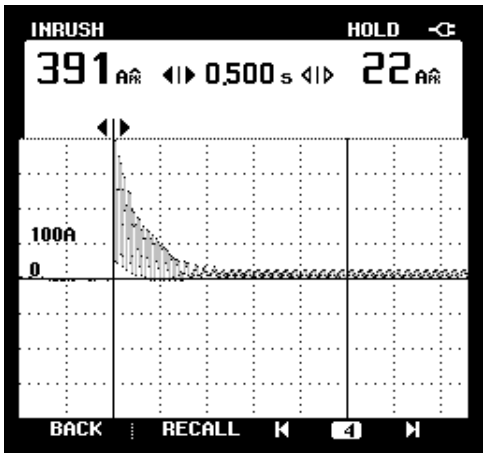


Fig. 5.24: Inrush current of the proposed enhanced-boost qZSI.

The efficiency of the proposed enhanced-boost qZSI is obtained experimentally and is shown in Fig. 5.25 by changing the load from 560 W to 1760 W keeping the boost factor *B* is 6.6 at the modulation index *M* of 0.75888 and the input voltage is 60 V to obtain 110 V rms as output phase voltage. The maximum efficiency obtained as 88.7% at 1180 watt power level. The experimentally obtained data points are shown in Fig. 5.25 using MOSFET as the switching devices.

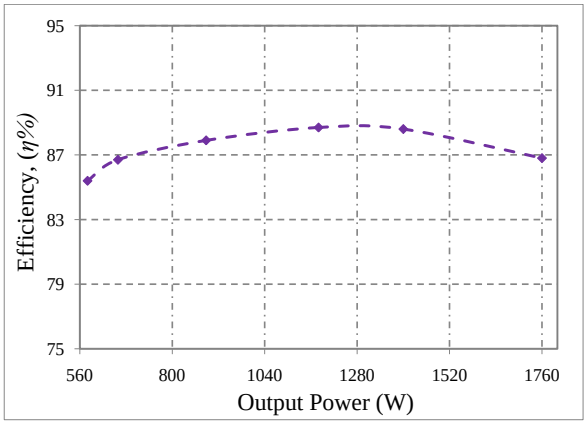


Fig. 5.25: Efficiency versus output power plot of the EB-qZSI at 110 Vrms output voltage and at V_{DC} = 60 V, D_0 = 0.24112.

5.9 Conclusion

In this chapter, two topologies of enhanced-boost quasi-Z-source inverters (EB-qZSIs) with two switched impedance network is presented and compares them with conventional ZSI, SL-ZSI, DA/CA-qZSI and enhanced-boost ZSIs. These proposed inverters possesses high boost factor at the low shoot-though duty ratio and high modulation index. The continuous input current configuration-1 of enhanced-boost qZSI is used for theoretical, simulation and experimental analysis. The stress across the capacitors is less so lower rating capacitors can be used, it provides common ground with source and inverter, and overcomes the problem of starting inrush current. Moreover, the input current ripple in the proposed inverters is also zero and it can be negligible. A peak efficiency of 88.7% is achieved.

This chapter presents the enhanced-boost series-Z-source inverter (EB-SZSI) with reduced capacitor stress. Similar to the enhanced-boost ZSI (EB-ZSI) and enhanced-boost qZSIs (EB-qZSIs) with two switched-impedance networks, this proposed inverter topology possess very high voltage boost at low shoot-through duty ratio and high modulation index to provide better quality output waveform. In addition to this, the proposed topology provides less voltage across the capacitors. Accordingly, lower rating capacitors can be used to reduce the size, cost, and weight of the system. Moreover, akin to EB-qZSIs, this proposed topology is able to solve the problem of starting inrush current, shares common ground with source and bridge inverter. This chapter presents the operating principles and boost factor derivation of EB-SZSI and compares with conventional EB-ZSI and EB-qZSIs. The Z-network component design, inductor current ripple, capacitor voltage ripple, efficiency evaluation and state-space analysis of the proposed topology is also carried out. Finally, the theoretical validation of the proposed topology is verified in MATLAB/Simulink and then tested using experimental setup with 60 V DC input voltage and 110 Vrms as output voltage.

6.1 Introduction

Many impedance-source network topologies were presented in the literature [40 – 97] and few of them are discussed in Chapter 2. Among these discussed non-coupled based inductor topologies, the enhanced-boost Z-source inverter (EB-ZSI) in [73] possesses very high boost factor.

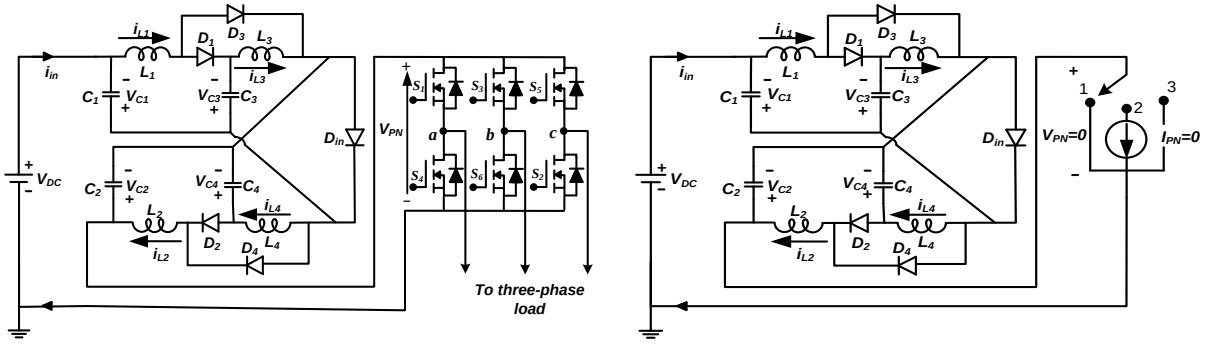
However, lack of common ground for the input source and bridge inverter, more capacitor stress and the current discontinuity still prevailed. As a measure two configurations of EB-qZSIs with two switched impedance networks are proposed [74] which successfully avoids these drawbacks while retains the high boost factor, along with starting inrush current limiting capability. The boost factor of the EB-ZSI [73] and EB-qZSIs [74] is given in (6.1)

$$B = \frac{1}{(2D_0^2 - 4D_0 + 1)} \tag{6.1}$$

As mentioned in Chapter 5, the drawbacks of EB-ZSI [73] can overcome with the EB-qZSIs [74]. But, still the enhanced-boost Z-source/ quasi Z-source inverters presented [73, 74] provides high stress across the capacitors. Therefore, the enhanced-boost series Z-source inverter (EB-SZSI) is presented in this chapter which reduces capacitors stress with same number of passive and active components at same boost factor. Moreover, similar to enhanced-boost quasi Z-

source inverters [74], the presented topology shares common ground with source, and reduces starting inrush current. The only drawback of this topology is it provides discrete input current. Either by adding extra input filters or by using maximum boost control method as modulation technique, it can be obtained continuous input current. Therefore this topology reduces the cost, weight, size of the capacitors.

The organization of this chapter is as follows. Section 6.2 provides the circuit analysis of the presented topology. The state-space analysis for the same is carried out in Section 6.3. In Section 6.4, the detail comparison of proposed topology and the enhanced-boost Z-source/ quasi-Z-source inverters is done. The expression for power loss and efficiency of the Z- network is expressed in Section 6.5. The Section 6.6 and Section 6.7 respectively describe the simulation and experimental results of the proposed EB-series ZSI to validate the theoretical analysis. Finally, Section 6.8 concludes the work.



(a) (b)

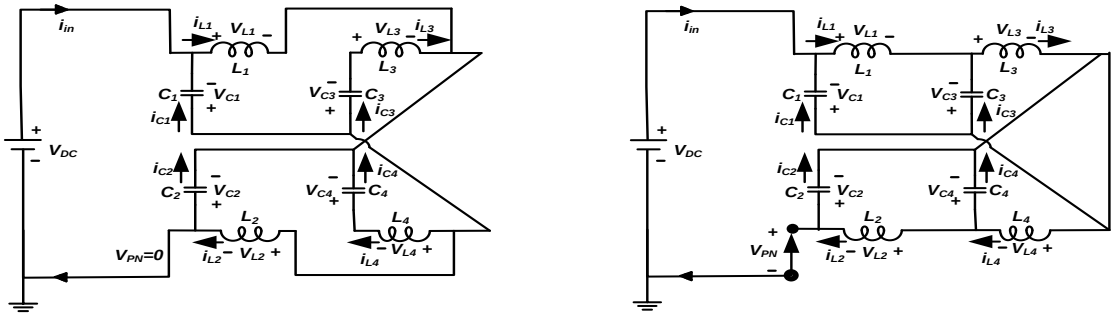
Fig. 6.1: Illustration of: (a) the proposed enhanced-boost series-ZSI; (b) Its simplified circuit.

6.2 Operating Principles and Circuit Analysis of the Proposed Enhanced-Boost Series-ZSI Topology

The configuration of the proposed impedance network inverter topology has the same components (i.e. four capacitors, five diodes, and four inductors) as [73, 74] which can be seen in Fig. 6.1 and provides the same voltage boost. In addition to this, the proposed topology may provide continuous input current and reduces the capacitor stress (which enables the use of small rating capacitors). Moreover, similar to the EB-qZSIs [74], proposed topology reduces starting inrush current problem and shares the common ground with the source and inverter bridge. Note that three-phase bridge inverter is used to analyze the circuit diagram in this chapter, but the propsed topology can also be applied to single-phase H-bridge inverter.

6.2.1 Operation Principle and Boost Factor Derivation of the Proposed Enhanced-Boost Series-ZSI

The operating principle of the proposed topology is same as that of the conventional ZSI, having a shoot-through state in addition to the eight non-shoot-though states (i.e., traditional six active states and two zero states) for three phase system. For the purpose of analysis, the operating states are simplified into shoot-through and non-shoot-through states. The equivalent circuits of enhanced-boost series-ZSI during shoot-through state and non-shoot-through states are depicted in Fig. 6.2(a) and Fig. 6.2(b) respectively.



(a) (b)

Fig. 6.2: Proposed series-ZSI equivalent circuits: (a) shoot-through state; (b) non-shoot-through state.

6.2.1.1 Shoot-through State

As illustrated in Fig. 6.2(a), both the upper and lower semiconductor devices of any one phase leg (i.e., a/ b/ c-phase leg) or the legs of any two phases (i.e., ab/ bc/ ca -phase legs) or the legs of all the three phases (abc-phase legs) are turned on simultaneously so that the dc-link is shorted. The diodes D_{in}, D_1, and D_2 are reverse biased, while the diodes D_3 and D_4 are turned on. The inductors are charged by the capacitors and these inductors store the electromagnetic energy. During this state, power transfer is not performed to the load. By applying Kirchhoff's voltage law (KVL) in the impedance network, the inductor voltages in steady-state condition are given as follows

$$\begin{cases} V_{L1} = L_1 \dfrac{di_{L1}}{dt} = V_{DC} + V_{C2} \\ V_{L2} = L_2 \dfrac{di_{L2}}{dt} = V_{DC} + V_{C1} \\ V_{L3} = L_3 \dfrac{di_{L3}}{dt} = V_{DC} + V_{C2} - V_{C3} + V_{C1} \\ V_{L4} = L_4 \dfrac{di_{L4}}{dt} = V_{DC} - V_{C4} + V_{C1} + V_{C2} \end{cases} \tag{6.2}$$

Similarly, by applying Kirchhoff's current law (KCL) in the impedance network of Fig. 6.2(a), the four capacitor currents (i_{C1}, i_{C2}, i_{C3}, i_{C4}) are derived as

$$\begin{cases} i_{C1} = C_1 \dfrac{dV_{C1}}{dt} = -i_{L2} - i_{L3} - i_{L4} \\ i_{C2} = C_2 \dfrac{dV_{C2}}{dt} = -i_{L1} - i_{L3} - i_{L4} \\ i_{C3} = C_3 \dfrac{dV_{C3}}{dt} = i_{L3} \\ i_{C4} = C_4 \dfrac{dV_{C4}}{dt} = i_{L4} \end{cases} \tag{6.3}$$

Further, the peak dc-link voltage, $\hat{V}_{PN}$ is zero because of shorted legs/dc-link.

6.2.1.2 Non-shoot-through State

As illustrated in Fig. 6.2(b), non-shoot-through state consists of eight sub-states (i.e. two zero (null) states and six active states) for the three-phase system. During this condition, the diodes D_{in}, $D1$, and D_2 are turned on, while the diodes D_3 and D_4 are off. The capacitors are charged from input source through inductors. The electromagnetic energy stored in the inductors and input energy is transferred to the main circuit which boosts the input voltage. After applying KVL in Fig. 6.2(b), the following inductor voltages can be written as follows.

$$\begin{cases} V_{L1} = L_1 \dfrac{di_{L1}}{dt} = V_{C3} - V_{C1} \\ V_{L2} = L_2 \dfrac{di_{L2}}{dt} = V_{C4} - V_{C2} \\ V_{L3} = L_3 \dfrac{di_{L3}}{dt} = -V_{C3} \\ V_{L4} = L_4 \dfrac{di_{L4}}{dt} = -V_{C4} \end{cases} \tag{6.4}$$

In the similar manner and applying KCL to Fig. 6.2(b), the four capacitor currents (i_{C1}, i_{C2}, i_{C3}, i_{C4}) in this state can be written as

$$\begin{cases} i_{C1} = C_1 \dfrac{dV_{C1}}{dt} = i_{L1} - i_{PN} \\ i_{C2} = C_2 \dfrac{dV_{C2}}{dt} = i_{L2} - i_{PN} \\ i_{C3} = C_3 \dfrac{dV_{C3}}{dt} = i_{L3} - i_{L1} \\ i_{C4} = C_4 \dfrac{dV_{C4}}{dt} = i_{L4} - i_{L2} \end{cases} \tag{6.5}$$

where, I_{PN} is the average dc-link current.

In Fig. 6.2(b), the peak dc-link voltage across the three-phase inverter bridge can be described as

$$V_{PN}^{\wedge} = V_{DC} + V_{C1} + V_{C2} \tag{6.6}$$

6.2.1.3 Boost Factor Derivation

Here the boost factor or voltage gain of the proposed inverter topology is calculated using the inductor voltage-second balance law.

The average voltage of inductor L_1 in steady state condition can be written as

$$\begin{cases} \int_0^{T_S} V_{L1}\,dt = 0 \\ \int_0^{T_S D_0} (V_{DC} + V_{C2})\,dt + \int_{T_S D_0}^{T_S} (1 - D_0)(V_{C3} - V_{C1})\,dt = 0 \end{cases} \tag{6.7}$$

Similarly, applying the inductor voltage-second balance law to L_2 the average voltage of inductor L_2 is given as

$$\begin{cases} \int_0^{T_S} V_{L2}\,dt = 0 \\ \int_0^{T_S D_0} D_0(V_{DC} + V_{C2})\,dt + \int_{T_S D_0}^{T_S} (1 - D_0)(V_{C4} - V_{C2})\,dt = 0 \end{cases} \tag{6.8}$$

The capacitor C_3 is charged by inductor L_3 alone and the capacitor C_4 is charged by inductor L_4 alone. Therefore, the average voltage across the inductors L_3 and L_4 is zero. Now, the capacitor voltages C_3 and C_4 are equal and can be written as

$$V_{C3} = V_{C4} = D_0(V_{C1} + V_{C2} - V_{DC}) \tag{6.9}$$

From (6.7) and (6.9), the capacitor C_1 voltage is obtained as

$$V_{C1} = \frac{V_{C2}(2D_0 - D_0^2) + V_{DC}(2D_0 - D_0^2)}{(D_0^2 - 2D_0 + 1)} \tag{6.10}$$

Similarly, from (6.8) and (6.9), the capacitor C_2 voltage is given as follows

$$V_{C2} = \frac{V_{C1}(2D_0 - D_0^2) + V_{DC}(2D_0 - D_0^2)}{(D_0^2 - 2D_0 + 1)} \tag{6.11}$$

Simplifying (6.10) and (6.11), the capacitor voltages V_{C1} and V_{C2} are as

$$V_{C1} = V_{C2} = \frac{(2D_0 - D_0^2)}{(2D_0^2 - 4D_0 + 1)} V_{DC} \tag{6.12}$$

Now, by substituting (6.12) into (6.9), the voltage across the capacitors C_3 and C_4 can be written as follows

$$V_{C3} = V_{C4} = \frac{D_0}{(2D_0^2 - 4D_0 + 1)} V_{DC} \tag{6.13}$$

From (6.6) and (6.12), the peak dc-link voltage in non-shoot-through state is derived as follows

$$\begin{cases} \hat{V_{PN}} = \dfrac{1}{(2D_0^2 - 4D_0 + 1)} V_{DC} \\ \hat{V_{PN}} = BV_{DC} \end{cases} \tag{6.14}$$

where B is written as

$$B = \frac{1}{(2D_0^2 - 4D_0 + 1)} \tag{6.15}$$

The boost factor from (6.15) indicates that when shoot-through duty cycle D_0 is between 0 and 0.29, boost factor B varies in (1, ∞).

The average dc-link signal of the proposed inverter can be expressed as follows

$$\tilde{V_{PN}} = \frac{(1 - D_0)}{(2D_0^2 - 4D_0 + 1)} V_{DC} \tag{6.16}$$

where, $\tilde{V}_{PN}$ is the average dc-link voltage.

The relationship between modulation index M and boost factor B depends on the PWM control strategy. In this thesis, the simple boost control (SBC) in [21] is used for the analysis. Therefore, the overall DC-AC voltage conversion ratio, G of the proposed series-ZSI for SBC method in the ideal case can be defined by

$$\text{Voltage gain, } G = M.B = \frac{M}{2M^2 - 1} \tag{6.17}$$

The fundamental peak phase output voltage can be written as follows

$$\begin{cases} \hat{V_{ac}} = M.\dfrac{\hat{V_{PN}}}{2} \\ \hat{V_{ac}} = M.B.\dfrac{V_{DC}}{2} \\ \hat{V_{ac}} = G.\dfrac{V_{DC}}{2} \end{cases} \tag{6.18}$$

where G is the voltage gain and M is the modulation index.

In the case of SBC scheme, the shoot-through duty ratio is limited by the modulation index as follows:

$$D_0 \leq (1 - M) \tag{6.19}$$

Depending upon the availability of the input voltage, the shoot-through duty ratio and modulation index can be adjusted to satisfy the output voltage requirement. The

AC output voltage can be varied from zero to infinity theoretically, by varying the modulation index and shoot-through duty cycle.

6.2.2 Suppression of Huge Inrush Current at Start-up Condition

Similar to conventional ZSI [41] and SL-ZSI [49], the enhanced-boost ZSI proposed in [73] produces very high inrush current, *i(t)* due to the presence of energy storage elements (i.e. capacitors and inductors) in the impedance network as can be seen in Fig. 6.3 and is given in (6.20) at time, *t.*

$$i(t) = \frac{V_{DC}}{R} e^{-(\frac{2}{RC})t} \qquad (6.20)$$

where, R is the internal resistance of anti-parallel diodes of switches and input diode D_{in}, and capacitors (C_1, C_2) and C is the equivalent capacitance of series capacitors C_1 and C_2.

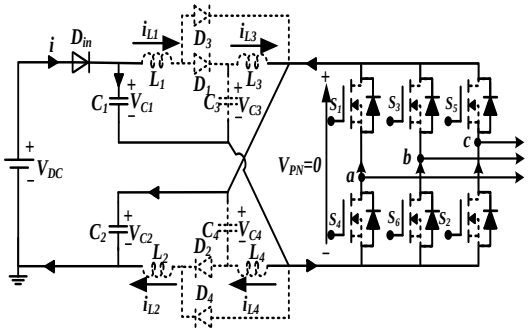


Fig. 6.3: Inrush current equivalent circuit of enhanced boost-ZSI.

Initially, the voltage across the capacitors is zero and therefore, huge inrush current will flow through the input diode D_{in} and feed-forward diodes of the semiconductor switches and the capacitors are immediately charged to half of the input voltage. Then the capacitors and inductors of the impedance network start resonating and generate huge voltage and current spikes.

In the proposed EB-SZSI, the problem of inrush current is eliminated. Beacuse there is no closed path for the current to flow from input side to the main circuit that is depicted in Fig. 6.1.

6.2.3 Impedance Network Design

If there is no boost operation involved, then the inductor voltages are zero and the capacitor voltages are equal to the input voltage. In order to boost the voltage gain, the shoot-through state is applied to switches. The inductors are charged by the capacitors and the inductor current increases linearly. Thus, by simplifying (6.2), (6.12) and (6.13), the inductors current ripple can be obtained as follows

$$\begin{cases} \Delta i_{L1,2} = \dfrac{T_S D_0}{L_{1,2} k_0} \dfrac{(D_0^2 - 2D_0 + 1)}{(2D_0^2 - 4D_0 + 1)} V_{DC} \\ \Delta i_{L3,4} = \dfrac{T_S D_0}{L_{3,4} k_0} \dfrac{(1 - D_0)}{(2D_0^2 - 4D_0 + 1)} V_{DC} \end{cases} \tag{6.21}$$

where k_0 is the number of shoot-through states in one switching period T_S.

Therefore, the inductors of the proposed topology can be designed as

$$\begin{cases} L_{1,2} = \dfrac{T_S D_0}{\Delta i_{L1,2} k_0} \dfrac{(D_0^2 - 2D_0 + 1)}{(2D_0^2 - 4D_0 + 1)} V_{DC} \\ L_{3,4} = \dfrac{T_S D_0}{\Delta i_{L3,4} k_0} \dfrac{(1 - D_0)}{(2D_0^2 - 4D_0 + 1)} V_{DC} \end{cases} \tag{6.22}$$

Applying the principle of capacitor charge balance from (6.3) and (6.5), the average currents of inductors can be derived as follows

$$\begin{cases} i_{L1,2} = \dfrac{(1 - D_0)}{(2D_0^2 - 4D_0 + 1)} I_{PN} \\ i_{L3,4} = \dfrac{(1 - D_0)^2}{(2D_0^2 - 4D_0 + 1)} I_{PN} \end{cases} \tag{6.23}$$

To design the capacitors of the proposed topology, the following consideration are kept in account that is the inductor current is same as the capacitor current in the shoot-through state. According to (6.3), the capacitors voltage ripple can be obtained as follows

$$\begin{cases} \Delta V_{C1,2} = \dfrac{T_S D_0}{C_{1,2} k_0} \dfrac{(2D_0^2 - 5D_0 + 3)}{(2D_0^2 - 4D_0 + 1)} I_{PN} \\ \Delta V_{C3,4} = \dfrac{T_S D_0}{C_{3,4} k_0} \dfrac{(1 - D_0)^2}{(2D_0^2 - 4D_0 + 1)} I_{PN} \end{cases} \tag{6.24}$$

Therefore, the capacitors can be designed as

$$\begin{cases} C_{1,2} = \dfrac{T_S D_0}{\Delta V_{C1,2} k_0} \dfrac{(2D_0^2 - 5D_0 + 3)}{(2D_0^2 - 4D_0 + 1)} I_{PN} \\ C_{3,4} = \dfrac{T_S D_0}{\Delta V_{C3,4} k_0} \dfrac{(1 - D_0)^2}{(2D_0^2 - 4D_0 + 1)} I_{PN} \end{cases} \tag{6.25}$$

6.3 State-Space Analysis of the Proposed Topology

The simplified circuit of the proposed enhanced-boost series-ZSI is depicted in Fig. 6.4. The ac-side circuit is represented by its simplified equivalent dc-load ($Z_l = R_l + sL_l$) in parallel with the active switch *S* [59, 64].

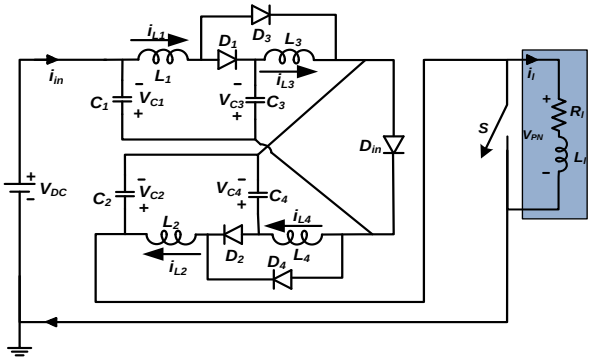


Fig. 6.4: Simplified diagram of the proposed network.

Using the state-space analysis method in [156], the state-space averaged model of the proposed series-ZSI is as follows

$$K.\dot{x} = A.x + B.u, \text{ and } y = E.x + F.u \tag{6.26}$$

where,
$$A = A_1 D_0 + A_2(1 - D_0)$$
$$B = B_1 D_0 + B_2(1 - D_0)$$

$$x = \begin{bmatrix} i_{L1} \\ i_{L3} \\ v_{C1} \\ v_{C3} \\ i_l \end{bmatrix}$$

$$u = [V_{DC}]$$

$$K = \begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_3 & 0 & 0 & 0 \\ 0 & 0 & C_1 & 0 & 0 \\ 0 & 0 & 0 & C_3 & 0 \\ 0 & 0 & 0 & 0 & L_l \end{bmatrix}$$

$$A = \begin{bmatrix} 0 & 0 & D_0 - 1 & 1 - D_0 & 0 \\ 0 & 0 & D_0 & -1 & 0 \\ 1 - D_0 & -D_0 & 0 & 0 & D_0 - 1 \\ D_0 - 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 - D_0 & 0 & -R_l \end{bmatrix}$$

$$B = \begin{bmatrix} D_0 \\ D_0 \\ 0 \\ 0 \\ 1 - D_0 \end{bmatrix}$$

$$E = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \quad \text{and} \quad F = [0]$$

The control to capacitor C_1 voltage transfer function can be obtained as

$$\left.\frac{v_{C1}}{d_0}\right|_{v_{DC}=0} = \frac{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0}{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{6.27}$$

The coefficients of (v_{C1}/d_0) in (6.27) are expressed as

$a_0 = L_l R_l (1 - 8D_0 + 20D_0^2 - 16D_0^3 + 4D_0^4)$

$a_1 = L_l (1 - 8D_0) + 2L_1 (1 - 4D_0 + 3D_0^2) + 2D_0^2 L_3 (1 - 2D_0 + D_0^2) + 4D_0^2 L_l (5 - 4D_0 + D_0^2)$

$a_2 = L_l R_l [(C_1 L_1 + C_1 L_3 + C_3 L_3) - D_0 L_3 (2C_1 + 4C_3 - C_1 D_0) + 4C_3 D_0^2 (L_1 + L_3)]$

$a_3 = 2C_3 L_1 L_3 + L_l (L_1 + L_3)(C_1 + 4C_3 D_0^2) + C_3 L_3 (L_l - 4D_0 L_1) - 2L_3 L_l D_0 (C_1 + 2C_3) + 2C_3 D_0^2 L_1 L_3$

$a_4 = C_1 C_3 L_1 L_3 L_l R_l;\ a_5 = C_1 C_3 L_1 L_3 L_l$

$b_0 = L_l R_l (L_1 r_5 r_6 - L_3 r_7 r_8);\quad b_1 = r_1 r_3 R_l - L_l [C_1 R_l r_3 r_4 - L_1 r_5 r_6 + L_3 r_7 r_8 - r_9 r_{10}]$

$b_2 = r_1 r_2 - C_1 L_l r_3 r_4 + C_3 L_1 L_3 L_l R_l [r_5 (1 - 2D_0) - 2D_0 r_7]$

$b_3 = C_3 L_1 L_3 L_l [r_5 (1 - 2D_0) - C_1 R_l r_3 - 2D_0 r_7 + r_9 (1 - D_0)];\quad b_4 = -C_1 C_3 L_1 L_3 L_l r_3$

$r_1 = L_3 (1 + 2D_0^2 - 3D_0) + 2D_0 L_1;\ r_2 = C_3 I_{L1} L_l;\ r_3 = i_l + 2I_{L1} - 2I_{L3};$

$r_4 = L_3 (D_0^2 + 1 - 2D_0) + L_1;\ r_5 = 2V_{C1} - V_{C3} + V_{DC};\quad r_6 = 2D_0^2 - 4D_0 + 1;$

$r_7 = 2V_{C1} + V_{DC};\ r_8 = 2D_0^3 - 6D_0^2 + 5D_0 - 1;\ r_9 = 2V_{C1} - V_{DC};\ r_{10} = L_3 D_0^2 (1 - D_0) - L_1 (3D_0 - 1).$

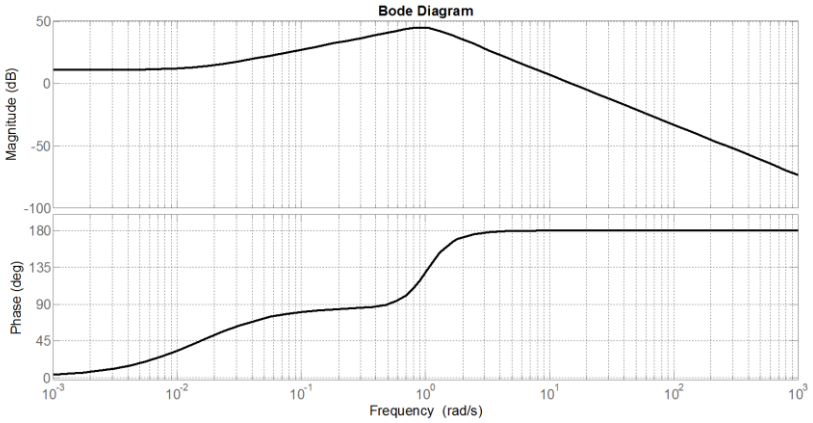
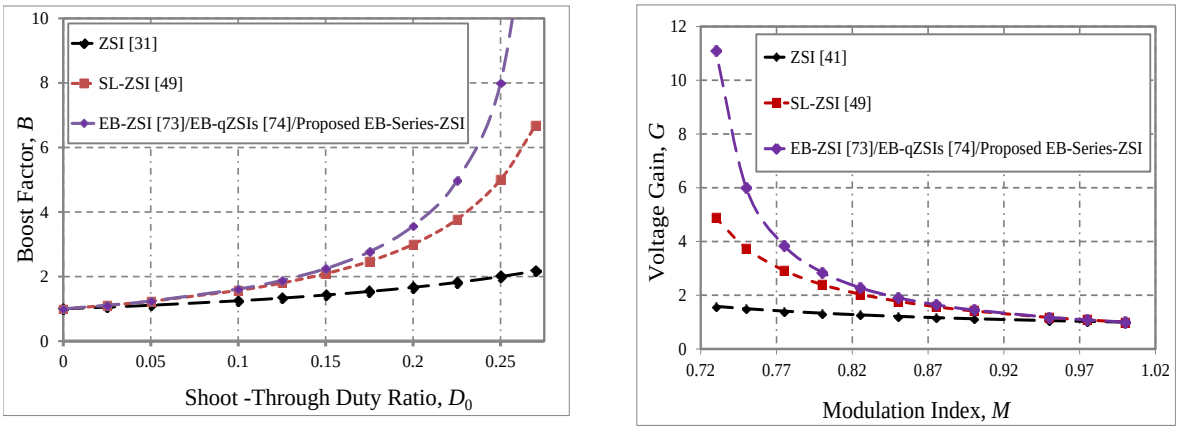


Fig. 6.5: Normalized Bode diagram for the control-to-capacitor-voltage transfer function.

For closed loop controller design, the above transfer function is used. The dynamic performance and stability analysis of the entire system can be analyzed with the help of the same. Bode plot of the open loop control-to-capacitor-voltage transfer function is shown in Fig. 6.5.

6.4 Performance Comparison of Enhanced-Boost Series-ZSI with other Topologies

In this section, the juxtaposition between the proposed inverter topology and impedance-network inverter topologies compared in Table 6.1 (i.e., ZSI [41], SL-ZSI [49], EB-ZSI [73], and the EB-qZSIs [74]) are considered. Detailed comparison of boost factor and voltage gain, voltage and current stresses, topology characteristics, power loss and efficiency are analyzed as follows.



(a) (b)

Fig. 6.6: Comparison of: (a) boost factor; (b) voltage gain.

6.4.1 Boost Factor and Voltage Gain Comparisons

As can be observed from Fig. 6.6(a) and the expressions in (6.1) and (6.15), the boost factor of the proposed enhanced-boost series-ZSI and the inverter topologies proposed in [73, 74] is same and is higher than the ZSI [41] and SL-ZSI [49], when the shoot-through duty ratio increases to almost 0.29.

Similarly, it is observed from Fig. 6.6(b) that for a given modulation index *M*, the voltage gain *G* of the proposed enhanced-boost series-ZSI and the inverters proposed in [73, 74] is same and is higher than the ZSI and SL-ZSI. Therefore to produce the same voltage gain *G*, the proposed inverter requires lower shoot-through duty ratio and provide higher modulation index *M* so as to improve the output voltage waveform.

6.4.2 Voltage Stress Comparisons

Table 6.1 compares the capacitor voltages, voltage stresses across the diodes and switches of the SL-ZSI, EB-ZSI, EB-qZSIs and proposed topology with same duty ratio and voltage gain. It can be observed that the proposed topology has relatively lower voltage stress across capacitors than EB-ZSI and EB-qZSI. Table 6.1

also shows that except the SL-ZSI all other three inverter topologies have the same maximum voltage stress across diodes and switches.

6.4.2.1 Diode Stress versus Voltage Gain

The diode stress which is defined as V_D/GV_{DC} [23] is compared in Fig. 6.7(a), from this figure it can observe that the diode stress in the EB-ZSI/ EB-qZSIs and in proposed topology is same and is less when compare to the ZSI and SL-ZSI. Therefore lower rating diodes can be used to reduce the cost.

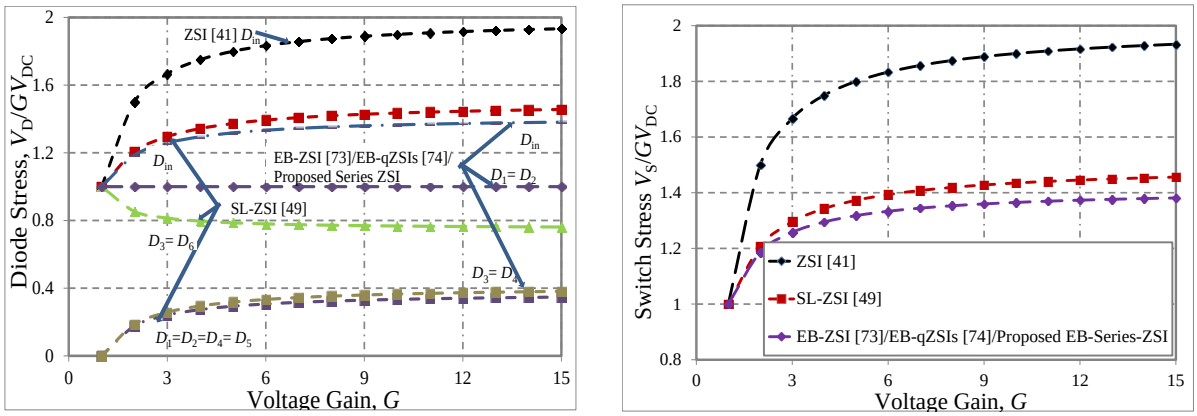
Table 6.1: Comparison of voltage stress in the same duty ratio and voltage gain.

	Parameters	SL-ZSI [49]	EB-ZSI [73]	EB-qZSIs [74]	Proposed Series-ZSI
	Boost factor, B	$\frac{1+D_0}{1-3D_0}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$
	Voltage gain, G	$\frac{M(2-M)}{3M-2}$	$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$
	Switch stress, (V_S/GV_{DC})	$\frac{2}{-3G+2+\sqrt{9G^2-4G+4}}$	$\frac{4G}{1+\sqrt{8G^2+1}}$	$\frac{4G}{1+\sqrt{8G^2+1}}$	$\frac{4G}{1+\sqrt{8G^2+1}}$
CAPACITOR STRESSES	V_{C1}/GV_{DC}	$\frac{2}{3G+2-\sqrt{9G^2-4G+4}}$	$\frac{1+\sqrt{8G^2+1}}{4G}$	$\frac{1+\sqrt{8G^2+1}}{4G}$	$\frac{8G^2+1}{4G(1+\sqrt{8G^2+1})}$
CAPACITOR STRESSES	V_{C2}/GV_{DC}	$\frac{2}{3G+2-\sqrt{9G^2-4G+4}}$	$\frac{1+\sqrt{8G^2+1}}{4G}$	$\frac{4G-1-\sqrt{8G^2+1}}{4G}$	$\frac{8G^2+1}{4G(1+\sqrt{8G^2+1})}$
CAPACITOR STRESSES	V_{C3}/GV_{DC}	Not Applicable	1	$\frac{-4G^2+2G+1+(2G+1)(\sqrt{8G^2+1})}{2G(1+\sqrt{8G^2+1})}$	$\frac{4G-1-\sqrt{8G^2+1}}{1+\sqrt{8G^2+1}}$
CAPACITOR STRESSES	V_{C4}/GV_{DC}	Not Applicable	1	$\frac{8G^2+1}{4G(1+\sqrt{8G^2+1})}$	$\frac{4G-1-\sqrt{8G^2+1}}{1+\sqrt{8G^2+1}}$
DIODE STRESS	$V_{D1,D2,D5}/GV_{DC}$	$\frac{(3G-\sqrt{9G^2-4G+4})}{G(2-9G+3\sqrt{9G^2-4G+4})}$	1	1	1
DIODE STRESS	$V_{D3,D4,D6}/GV_{DC}$	$\frac{2}{2+3G-\sqrt{9G^2-4G+4}}$	$\frac{4G-1-\sqrt{8G^2+1}}{1+\sqrt{8G^2+1}}$	$\frac{4G-1-\sqrt{8G^2+1}}{1+\sqrt{8G^2+1}}$	$\frac{4G-1-\sqrt{8G^2+1}}{1+\sqrt{8G^2+1}}$
DIODE STRESS	V_{Din}/GV_{DC}	$\frac{2}{-3G+2+\sqrt{9G^2-4G+4}}$	$\frac{4G}{1+\sqrt{8G^2+1}}$	$\frac{4G}{1+\sqrt{8G^2+1}}$	$\frac{4G}{1+\sqrt{8G^2+1}}$
	DC-link voltage	$\overline{S_s}\frac{1+D_0}{1-3D_0}V_{DC}$	$\overline{S_s}\frac{1}{1-4D_0+2D_0^2}V_{DC}$	$\overline{S_s}\frac{1}{1-4D_0+2D_0^2}V_{DC}$	$\overline{S_s}\frac{1}{1-4D_0+2D_0^2}V_{DC}$

6.4.2.2 Switch Stress versus Voltage Gain

The switch stress comparison is depicted in Fig. 6.7(c) and it is observed that, for the same produced voltage gain, the switch stress of the proposed enhanced-

boost series-ZSI and the topologies proposed in [73, 74] is same and is lower than the ZSI and SL-ZSI.



(a) (b)

Fig. 6.7: Comparison of the proposed series-ZSI with the existing topologies: (a) voltage gain G versus diode stress; (b) voltage gain G versus switch stress V_S.

6.4.2.3 Capacitor Stress versus Voltage Gain

The main advantage of this proposed enhanced-boost series-ZSI when compared to other topologies compared in Table 6.1 is that the stress across the capacitor is low (defined as the ratio of V_C/GV_{DC} [23]) for the same voltage gain and it can be observed from Fig. 6.8. Therefore, lower rating capacitors can be used in the proposed topology to reduce the cost, weight, and size of the system.

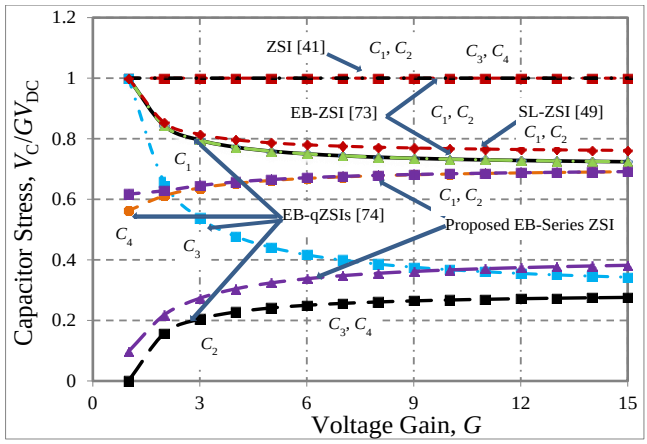


Fig. 6.8: Capacitor stress comparison.

6.4.3 Ripple Analysis and Comparison

From (6.21), for the constant value of T_S, V_{DC}, Δi_L, and K_0, the coefficient kI can be defined as

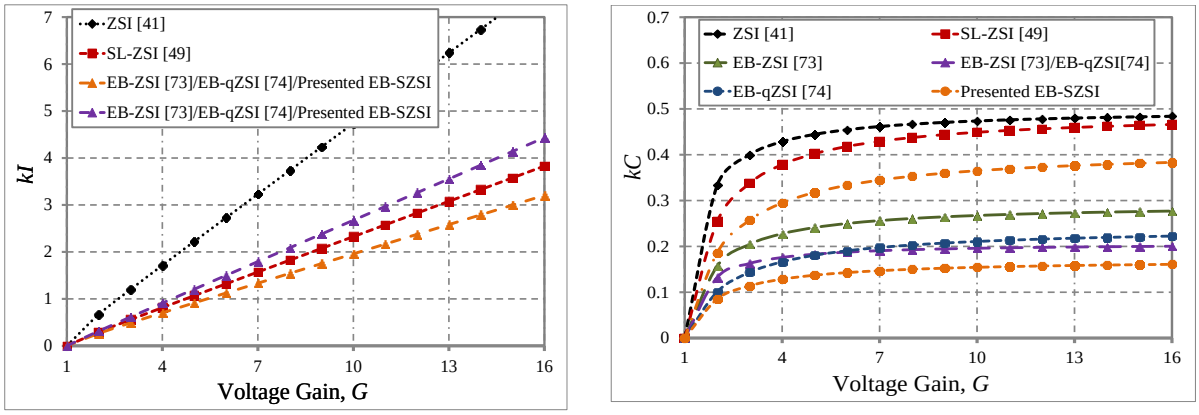
$$\begin{cases} kI_{1,2} = \dfrac{D_0(D_0^2 - 2D_0 + 1)}{(2D_0^2 - 4D_0 + 1)} \\ kI_{3,4} = \dfrac{D_0(1 - D_0)}{(2D_0^2 - 4D_0 + 1)} \end{cases} \tag{6.28}$$

The coefficient of *kI* versus voltage gain is shown in Fig. 6.9(a). According to above expression, the *kI* is a good measure for inductor volume for the same output power. In this figure, it is shown that the proposed scheme has lower inductor volume (inductance) compared with conventional ZSI and SL-ZSI methods. This is due to the fact that the proposed scheme requires smaller D_0 to produce a high boost factor *B*. Smaller D_0 will result in lower inductances.

Similarly, from (6.24) for the constant value of T_S, ΔV_C, and K_0, the coefficient *kC* will be defined as

$$\begin{cases} kC_{1,2} = \dfrac{D_0}{(2-D_0)} \\ kC_{3,4} = \dfrac{D_0}{(2-D_0)} \end{cases} \tag{6.29}$$

The coefficient of *kC* versus voltage gain is shown in Fig. 6.9(b). According to (6.21), the *kC* is a powerful tool for capacitor volume (capacitance) in ZSIs. As indicated in Fig. 6.9(b), for the same voltage gain, the proposed scheme has lower capacitance than those of the conventional ZSI, SL-ZSI, and EB-ZSIs topologies. This is due to the fact that the proposed inverter has a high boost factor with lower D_0.



(a) (b)

Fig. 6.9: Comparison of ripples: (a) *kI* versus voltage gain; (b) *kC* versus voltage gain.

6.4.4 Topology Characteristics

Table 6.2 depicts the comparison of topology characteristics between the SL-ZSI, EB-ZSI, EB-qZSIs and proposed topology. It is noted that components used in the inverter bridge and output *LC* filter are not considered in the comparison. The proposed topology has all inherent advantages of EB-qZSIs including common ground point, continuous input current*, and no startup inrush current.

6.4.4.1 Input Current Nature

As can be seen from Table 6.2, the current drawn from the input source is discontinuous in case of SL-ZSI and EB-ZSI. But, the EB-qZSIs draws continuous input current due to inductor L_3, so the input current ripple is negligible and it is equal to zero [74]. Whereas, the proposed topology can also draw continuous input current* if maximum boost control technique as the modulation method.

6.4.4.2 Common Ground Sharing and Start-up Current Suppression

Similar to EB-qZSIs presented in [74], the proposed topology also shares common ground between source and bridge inverter to reduce the leakage current problem. Moreover, the presented topology also reduces the starting inrush current problem.

Table 6.2: Comparison of topology characteristics.

Topology Characteristics		SL-ZSI [49]	EB-ZSI [73]	EB-qZSIs [74]	Proposed Series-ZSI
Common Ground		No	No	Yes	Yes
Startup Inrush Current		Yes	Yes	No	No
Number of Component	Inductors	4	4	4	4
	Capacitors	2	4	4	4
	Diodes	7	5	5	5
Input Current Nature		Discontinuous	Discontinuous	Continuous	Continuous*

Note*: For maximum boost control [22]

6.4.4.3 Component Count

Comparison of the components (i.e., both passive and active) is shown in Table 6.2. The components used in the proposed inverter topology and the topologies proposed in [73, 74] is same, but less number of diodes are used when compared to SL-ZSI [49].

6.4.5 Comparison of Current Stresses

The current stresses of SL-ZSI, EB-ZSI, EB-qZSIs and the proposed topology are tabulated in Table 6.3. The current stresses of switches in the inverter bridge vary with different control methods. The comparison is carried out with simple boost control method (SBC) [21] for all the topologies. It can be seen that the EB-ZSI, EB-qZSIs and the proposed topologies have the same inductor currents under the same

operating conditions. It is contemplated that the current stress across diodes of the proposed inverter is same as that of the EB-ZSI and EB-qZSI.

6.4.6 Inductor Currents and Average dc-link Current

For the proposed topology, the expressions of inductor currents are derived in Section 6.2.3 and are tabulated in Table 6.3. From this table it is observed that the expressions of inductor currents are same for the proposed topology and for the topologies presented in [73, 74]. Table 6.3 also compares the average dc-link currents and diode currents expressions for all the topologies. The proposed topology gives more input current ripple. Whereas the input current ripples is nigligible in case of EB-qZSIs [74].

Table 6.3: Current stress comparisons with same dc-link current and load.

Parameter		SL-ZSI [49]	EB-ZSI [73]	EB-qZSIs [74]	Proposed Series-ZSI
Input current, i_{in}		$2i_{L1}-I_{PN}$	$2i_{L3}-I_{PN}$	i_{L1}	I_{PN}
Input Current ripple, ΔI_{in}		$\lvert(1-D_0)i_L-i_{PN}\rvert$	$\lvert(1-2D_0)i_{L3}-(1-D_0)i_{PN}\rvert$	0	$\lvert(1-2D_0)i_{L3}-(1-D_0)i_{PN}\rvert$
Inductor Currents		$i_{L1,L2,L3,L4}=\frac{1-D_0}{1-3D_0}I_{PN}$	$i_{L1,L2}=\frac{(1-D_0)}{1-4D_0+2D_0^2}I_{PN}$ $i_{L3,L4}=\frac{(1-D_0)^2}{1-4D_0+2D_0^2}I_{PN}$	$i_{L1,L2}=\frac{(1-D_0)}{1-4D_0+2D_0^2}I_{PN}$ $i_{L3,L4}=\frac{(1-D_0)^2}{1-4D_0+2D_0^2}I_{PN}$	$i_{L1,L2}=\frac{(1-D_0)}{1-4D_0+2D_0^2}I_{PN}$ $i_{L3,L4}=\frac{(1-D_0)^2}{1-4D_0+2D_0^2}I_{PN}$
Average dc-link current, I_{PN}		$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$
Diode D_{in} current		$\overline{S_s}(2i_{L1}-I_{PN})$	$\overline{S_s}(2i_{L3}-I_{PN})$	$\overline{S_s}(2i_{L3}-I_{PN})$	$\overline{S_s}(2i_{L3}-I_{PN})$
Diode Currents	i_{D1}	$S_s i_{L1}$	$\overline{S_s}i_{L1}$	$\overline{S_s}i_{L1}$	$\overline{S_s}i_{L1}$
	i_{D2}	$S_s i_{L2}$	$\overline{S_s}i_{L2}$	$\overline{S_s}i_{L2}$	$\overline{S_s}i_{L2}$
	i_{D3}	$S_s i_{L3}$	$S_s i_{L1}$	$S_s i_{L1}$	$S_s i_{L1}$
	i_{D4}	$S_s i_{L4}$	$S_s i_{L2}$	$S_s i_{L2}$	$S_s i_{L2}$
	$i_{D5,D6}$	$\overline{S_s}i_{L1}$	Not Applicable	Not Applicable	Not Applicable

where, S_s is the shoot-through switching function in the inverter. S_s is equal to 0 when the inverter operates in the non-shoot-through states and 1 when it is in the shoot-through states.

6.5 Power Loss Analysis and Expression for Efficiency Evaluation

In order to analyze the power loss in the impedance network of proposed inverter topology, the non-ideal equivalent circuit of impedance network during shoot-through state and non-shoot-through states are drawn in Fig. 6.10(a) and Fig. 6.10(b) respectivily.

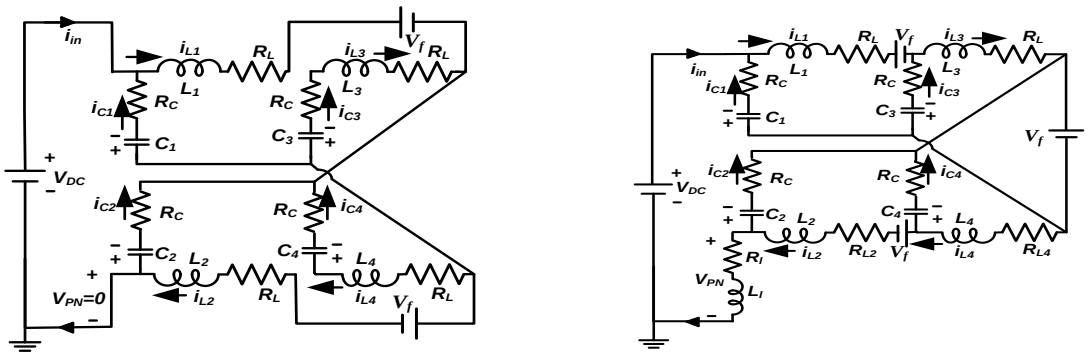


Fig. 6.10: Non-ideal equivalent circuits for efficiency evaluation of the proposed topology during: (a) shoot-through state; (b) non-shoot-through states.

From Fig. 6.10, the expressions of power loss in an impedance network of proposed topology during shoot-through state (P_1) and non-shoot-through states (P_2) are obtained as follows

$$P_1 = 2D_0{}^2[(i_{L1}^2 + i_{L3}^2)R_L + ((i_{L1} + 2i_{L3})^2 + i_{L3}{}^2)R_C] + 2V_f D_0 i_{L1} \tag{6.30}$$

$$\begin{cases} P_2 = 2(1-D_0)^2[(i_{L1}^2 + i_{L3}^2)R_L + ((i_{L1} - i_{PN})^2 + (i_{L1} - i_{L3})^2)R_C] \\ \quad + V_f(1-D_0)(2i_{L1} + 2i_{L3} - i_{PN}) \end{cases} \tag{6.31}$$

where R_L is the equivalent series resistances of the inductors, R_C is the equivalent series resistances capacitors, and V_f is the forward voltage drop of the diodes.

From the (6.30) and (6.31), the efficiency of the proposed series-ZSI can expressed as

$$\eta_{ImpZSI} = \frac{B.V_{PN}.I_{PN}}{P_1 + P_2 + B.V_{PN}.I_{PN}} = \frac{1}{X + Y + Z + 1} \tag{6.32}$$

where

Inductor loss, $X = \dfrac{2R_L(1-D_0)^3}{R_l} . \dfrac{[(1-D_0)^2 + D_0^2][(1-D_0)^2 + 1]}{(1-4D_0 + 2D_0^2)^2}$

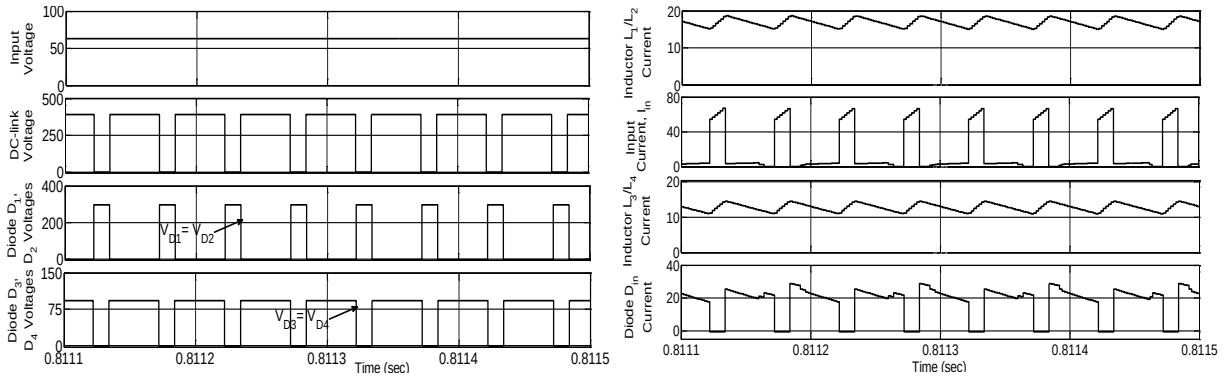
Capacitor loss, $Y = \dfrac{4D_0^2 R_C(1-D_0)^3}{R_l} . \dfrac{[(3-2D_0)^2 + (1-D_0)^2]}{(1-4D_0 + 2D_0^2)^2}$; and

Diode loss, $Z = \dfrac{3V_f(1-D_0)}{V_{DC}}$

6.6 Simulation Results and Discussions

To validate the theoretical analysis as discussed in Subsection 6.2.1 of this chapter and to compare the results with [73, 74], the simulation studies are carried

out in MATLAB/Simulink with the given parameters: V_{DC} = 60 V, f_s = 10 kHz, D_0 = 0.24112, and M = 0.75888 to produce a phase voltage of 110V rms. The capacitor and inductor ripples are choosen as $\Delta V_{C1,2} = \Delta V_{C3,4}$ = 2%, $\Delta i_{L1,2} = \Delta i_{L3,4}$ = 50% respectively. Thus $L_1 = L_2$ = 0.731 mH, $L_3 = L_4$ = 0.964 mH, $C_1 = C_2$ = 3700 µF, and $C_3 = C_4$ = 1143 µF are obtained for the impedance network based on equations (6.22) and (6.25) respectively in Subsection 6.2.3. The theoretically results are $V_{C1} = V_{C2}$ = 167.6V, $V_{C3} = V_{C4}$ = 95.3V, $\hat{V}_{PN}$ = 395.3V, V_{ac} = 110 V rms, and G = 5 are obtained based on the equations derived from Subsection 6.2.1 for the simple boost control method [41]. Similarly, the peak values of diode voltages can be obtained as V_{Din} = 395.3 V, $V_{D1} = V_{D2}$ = 300 V, $V_{D3} = V_{D4}$ = 95.3 V.



(a) (b)

Fig. 6.11: From top to bottom; Simulation results of: (a) input, dc-link, diode D_1/D_2, and diode D_3/D_4 voltages; (b) inductor L_1, input I_{in}, inductor L_3, and diode D_{in} currents respectively.

From top to bottom, the simulation results of the input, dc-link, diode D_1/D_2, and diode D_3/D_4 voltages respectively are depicted in Fig. 6.11(a). It can be observed from Fig. 6.11(a) that the dc-link voltage is zero in shoot-through state due to short circuited dc-link/legs and maximum in the non-shoot-through state. Fig. 6.11(a) shows the diode voltages and it can be observed that the simulation results are perfectly matching the values obtained above theoretically.

Similarly, the inductor L_1, L_3 currents (I_{L1}, I_{L3}), input current (I_{in}), and diode D_{in} currents are depicted in Fig. 6.11(b) for the proposed inverter. It can be seen from this figure, that inductors are charged during shoot-through states and discharged during non-shoot-through states (i.e., inductor current increases linearly in shoot-through state and decreases linearly in non-shoot-through state). It is also observed from Fig. 6.11(b) that the input current drawn from the supply is discontinuous with some ripple (i.e., during zero (null) states, the current drawn from the supply is zero and during other states there exists certain current).

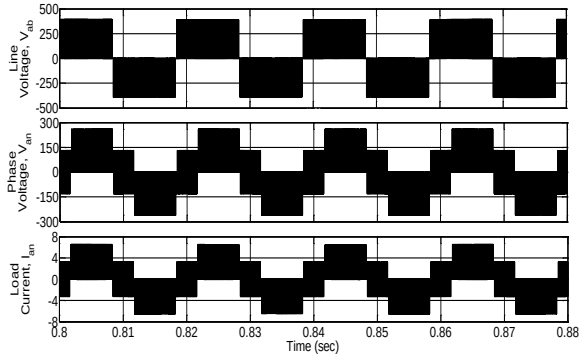


Fig. 6.12: From top to bottom: Simulation results of line voltage, phase voltage and phase current for resistive load.

Fig. 6.12 show the simulations results of ac-side voltages and currents at duty cyle D_0 = 0.24112 and input voltage of 60 V. The line voltage (V_{ab}), phase voltage (V_{an}), and current, (I_{an}) are depicted in Fig. 6.12 for resistive load of R_l = 40 Ω.

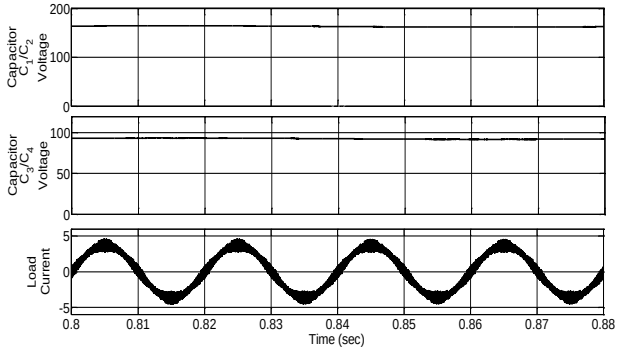


Fig. 6.13: Simulation results of capacitor voltages and load current for resistive-inductive load.

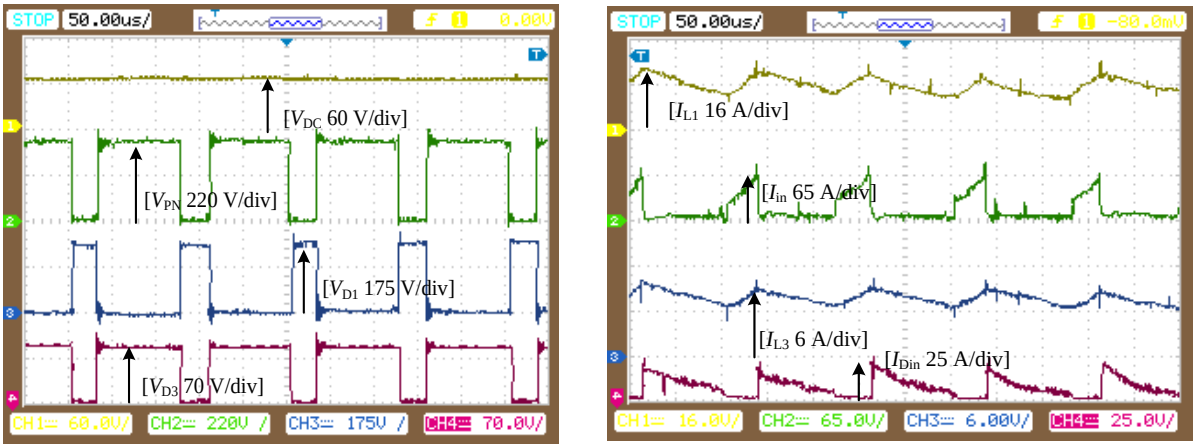
As discussed earlier, the main advantages of this proposed topology is that; it results in less capacitor stress. It is observed From Fig. 5.9 and Fig. 6.13 that the proposed topology provides less capacitor voltage at the same shoot-through duty cycle and input voltage. The capacitor voltages V_{C1}/ V_{C2} and V_{C3}/ V_{C4} are boosted to about 165 V and 95 V, respectively, these values are coincident with the calculated values (6.12) and (6.13). Fig. 6.13 depicts the simulation results of load current for the resistive-inductive load (R_l = 40 Ω, L_l = 2.5 mH). Hence, the aforementioned operation principles in Section 6.2.1 are validated properly through the above simulation results.

6.7 Experimental Validation and Discussions

For the validation of theoretical analysis discussed in subsection 6.2.1 and the above obtained simulation results of the proposed EB-SZSI, the hardware results are obtained at V_{DC} = 60 V, D_0 = 0.24112, and M = 0.75888 for R – L load. The power MOSFET (IRF460) is used as the semiconductor switches. The firng pulses to the

power switches are provided with the help of dSPACE DS1104. The experimental results are taken in a similar way as that of the simulation results with simple boost control method as the modulation technique.

As shown in Fig. 6.14(a), the input voltage applied to the Z-network inverter is 60 V; the peak dc-link voltage is about 386 V in non-shoot-through state and is zero during shoot-through state due to short circuited inverter. Meanwhile, the peak voltage of diodes D_1/D_2 and D_3/D_4 are 285 V and 85 V respectively for D_0 = 0.24112.



(a) (b)

Fig. 6.14: Experimental results: From top to bottom; (a) input, dc-link, diode D_1, and diode D_3 voltages; (b) inductor L_1, input, inductor L_3, and diode D_{in} currents.

The inductor L_1, input, inductor L_3, and diode D_{in} currents are depicted in Fig. 6.14(b). And it is observed that the waveforms are exactly similar to that of simulation results shown in Fig. 6.11(b). It can also be observed from Fig. 6.14(b) that the currents of inductors increase linearly in the shoot-through state and decrease linearly in the non-shoot-through state. From this figure, it can also be observed that the current from the source is discrete.

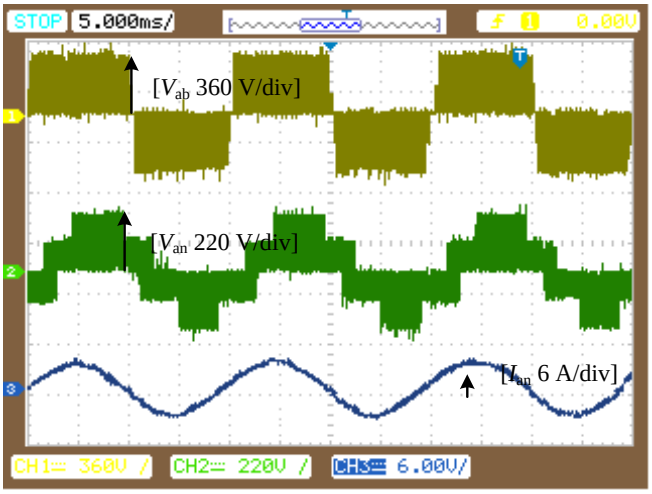
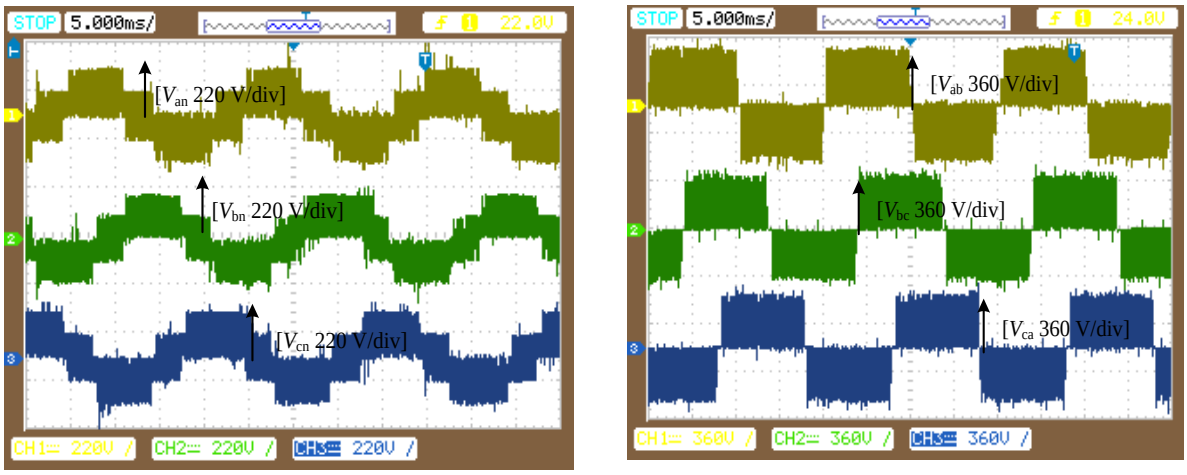


Fig. 6.15: Experimental results, From top to bottom: line voltage V_{ab}, phase voltage V_{an}, and load current I_{an} for resistive-inductive load.

Fig. 6.15 depicts the output side voltages and current waveforms for R – L load (R_l = 40 Ω, L_l = 2.5 mH) at 60 V input voltage. From this figure it can observe that the output current lags the voltage.

Three-phase voltages V_{an}, V_{bn}, and V_{cn} from top to bottom are shown in Fig. 6.16(a). Similarly, Fig. 6.16(b) depicts the three line voltages V_{ab}, V_{bc}, and V_{ca} respectively across the load terminals from top to bottom. The experimental results give less magnitude of voltages when compare to the simulation results due to the drop across diodes and semiconductor switches.



(a) (b)

Fig. 6.16: From top to bottom, experimental results of: (a) three-phase voltages (V_{ab}, V_{bc}, and V_{ca}); (b) line voltages (V_{an}, V_{bn}, and V_{cn}) respecitively.

Afterward, Fig. 6.17 depicts the steady-state capacitor C_1, C_2, C_3, and C_4 voltages are also obtained from the experimental setup. These experimental results are almost similar to that of simulation results. The experimental values are slightly less when compared to theoretical values obtained; this is due to non-idealities of components (i.e., drop across the switches, diodes, and parasitic resistances of inductors and capacitors).

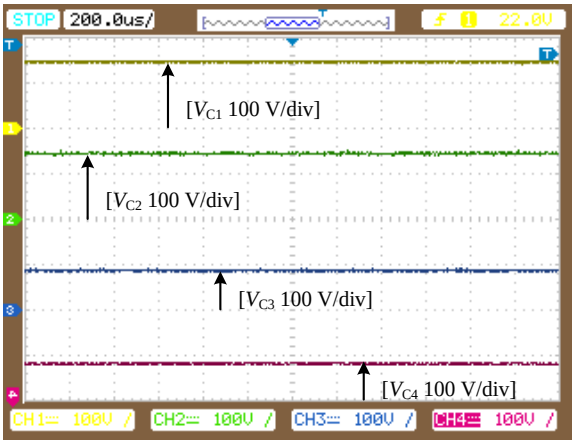
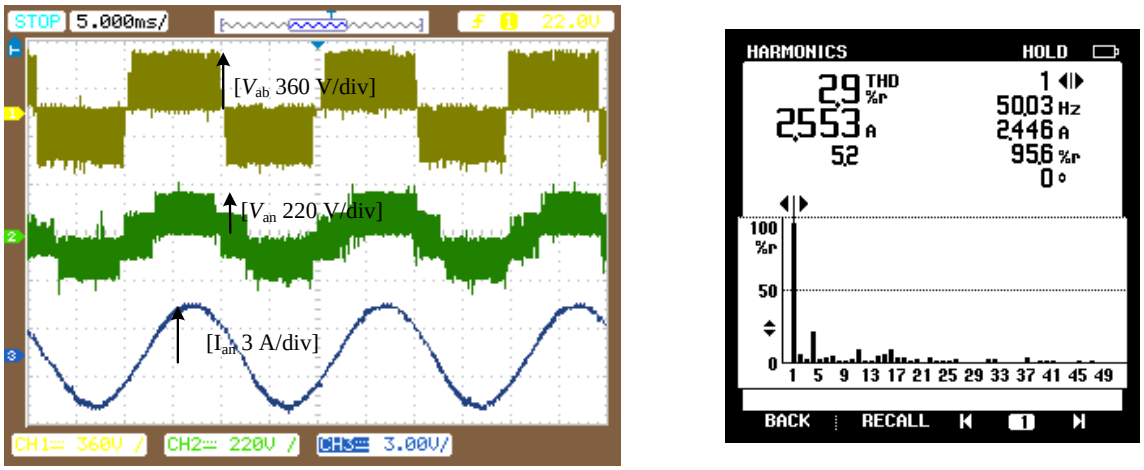


Fig. 6.17: Experimental results of capacitor voltages.

The proposed topology then has been tested with R – L load with R_l = 40 Ω and L_l = 40 mH, as shown in Fig. 6.18. Fig. 6.18(a) shows the experimental results for lagging load. It can be seen that load current lags the output voltage by a phase shift of 17°. Fig. 6.18(b) also shows the load current total harmonic distortion (THD) of fundamental frequency (50 Hz) is obtained as 2.9%.



(a) (b)

Fig. 6.18: Experimental results: (a) ac-side voltages and load current; (b) output current THD for resistive-inductive load.

6.8 Conclusion

In this study, a novel topology of enhanced-boost series-Z-source inverter with reduced capacitor stress was proposed and compared with the traditional ZSI, SL-ZSI, enhanced-boost ZSI, and enhanced-boost qZSIs. Similar to enhanced-boost ZSI/enhanced-boost qZSIs, the proposed topology possesses high boost factor at low shoot-through duty ratio and high modulation index to provide the better quality output waveform. In addition to that, the stress across the capacitors was lower when compared to the enhanced-boost ZSI and enhanced-boost qZSIs, so lower rating capacitors can be used to reduce the cost, size, and weight of the system. Moreover, similar to the enhanced-boost qZSIs, the proposed topology shares common ground with source and inverter, and reduces the problem of starting inrush current at start-up condition. The power loss analysis of impedance network and the efficiency evaluation of the proposed impedance network were carried out. The small signal analysis of the proposed inverter was also carried out.

CHAPTER 7: FOUR DIFFERENT CONFIGURATIONS OF ENHANCED-BOOST QUASI-Z-SOURCE INVERTERS

This chapter presents a new family of four enhanced-boost quasi Z-source inverters (EB-qZSIs). These presented topologies provide same voltage boost or voltage gain as that of the enhanced-boost Z-source inverter (EB-ZSI) / enhanced-boost qZSIs (EB-qZSIs). Compare to EB-ZSI and EB-qZSIs, these topologies provides less stress across the capacitors which reduce the volume and cost of the system. Similar to EB-qZSIs, the proposed inverters shares common ground with the source and inverter bridge and reduces the starting inrush current problem. Among all the four proposed configurations of EB-qZSIs, the configuration-1 provides less stress across the capacitors and low inrush current at start-up condition. Therefore, configuration-1 is taken as an example for hardware implementation. The operating principle, impedance network parameters design, and comparison with other Z-networks are carried out. Finally, the theoretical analysis is validated with simulation and experimental tests.

7.1 Introduction

The enhanced-boost Z-source inverter (EB-ZSI) was proposed in [73] which produce high voltage gain at low shoot-through duty ratio and the illustration of EB-ZSI was shown in Fig. 5.1. Similar to traditional ZSI [41], the EB-ZSI proposed in [73] has certain drawbacks; such as discrete input current, does not share common ground with supply, large inrush current, and high capacitor stress. These drawbacks are minimised by enhanced-boost qZSIs (EB-qZSIs) with same number of components in the impedance network [74] and the two configurations of EB-qZSIs were shown in Fig. 5.2. But, the stress across the capacitor is still high in case of EB-qZSIs [74]. Therefore, to reduce the capacitor stresses and maintaining all other advantages of EB-qZSIs [74], the enhanced-boost series Z-source inverter (EB-SZSI) was discussed in Chapter 6. The boost factor of EB-ZSI [73], EB-qZSIs [74], and EB-SZSI is same and is given as follows;

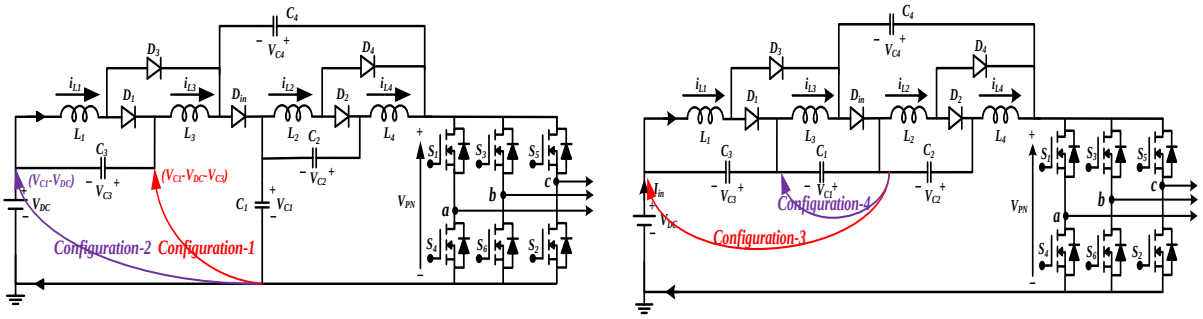
$$B = \frac{\hat{V}_{PN}}{V_{DC}} = \frac{1}{1 - 4D_0 + 2D_0^2} \tag{7.1}$$

This chapter presents the four different configurations of EB-qZSIs which are derived from continuous input current EB-qZSI shown in Fig. 5.2(b). The stress across the capacitors is less in these presented topologies. Moreover, the other advantages of EB-qZSIs remained same in these topologies. These derivations are described in Section 7.2. Section 7.3 describes the circuit configurations, boost factor derivation and operating principles of all four configurations. Design of impedance

network parameters are carried out in Section 7.4. In Section 7.5, the comparison of existing enhance-boost Z-network topologies and the proposed topologies are made. Finally, to validate the theoretical analysis, the simulation and experimental test is carried out in Section 7.6. Section 7.7 provides the concluding remarks.

7.2 Derivations of Different Configurations of Enhanced-Boost Quasi Z-Source Inverters

Before accessing on the main issue of this chapter, it is necessary to introduce general procedures to derive the four different configurations of EB-qZSIs from the continuous input current EB-qZSIs presented in [74]. The four configurations of EB-qZSIs derived from Fig. 7.1 are depicted in Fig. 7.2 look different at the first sight, but they are basically similar and, as will be explained below. The derivations are quite simple and intuitive.



(a) (b)

Fig. 7.1: Derivation of different configurations of EB-qZSIs from continuous input current EB-qZSI: (a) derivation of configuration-1 and configuration-2; (b) derivation of configuration-3 and configuration-4.

7.2.1 Derivation from Continuous Input Current EB-qZSI to Four Different Configurations of EB-qZSIs

Fig. 7.1 show the derivation from continuous input current EB-qZSI to four configurations of EB-qZSIs. The original EB-qZSI in configuration-2 depicted in Fig. 5.2(b) comprises of four capacitors (C_1, C_2, C_3, and C_4), four inductors (L_1, L_2, L_3, and L_4), and five diodes (D_{in}, D_1, D_2, D_3, and D_4) in the impedance network. A closer look at the EB-qZSI shown in Fig. 7.1(a) discloses that the input voltage source V_{DC}, inverter bridge, and the capacitor C_1 share the common ground. Therefore, capacitor C_1 can be moved to top side as illustrated in Fig. 7.1(a) and then the voltage across the capacitor C_1 is reduced to ($V_{C1} – V_{DC} – V_{C3}$) in case of configuration-1 and to ($V_{C1} – V_{DC}$) in case of configuration-2. After rearrangement, the circuits can lead to the EB-qZSIs for configurations-1 and configurations-2 which is depicted in Fig. 7.2(a)

and Fig. 7.2(b) respectively. With these configurations, the stress across the capacitors is reduced. Similarly, the negative polarity of capacitor C_2 of configuration-1 shown in Fig. 7.1(b) can be connected to negative and positive polarities of capacitor C_3, which lead to the two more configurations of EB-qZSIs for configurations-3 and configurations-4 shown and are shown in Fig. 7.2(c) and Fig. 7.2(d) respectively.

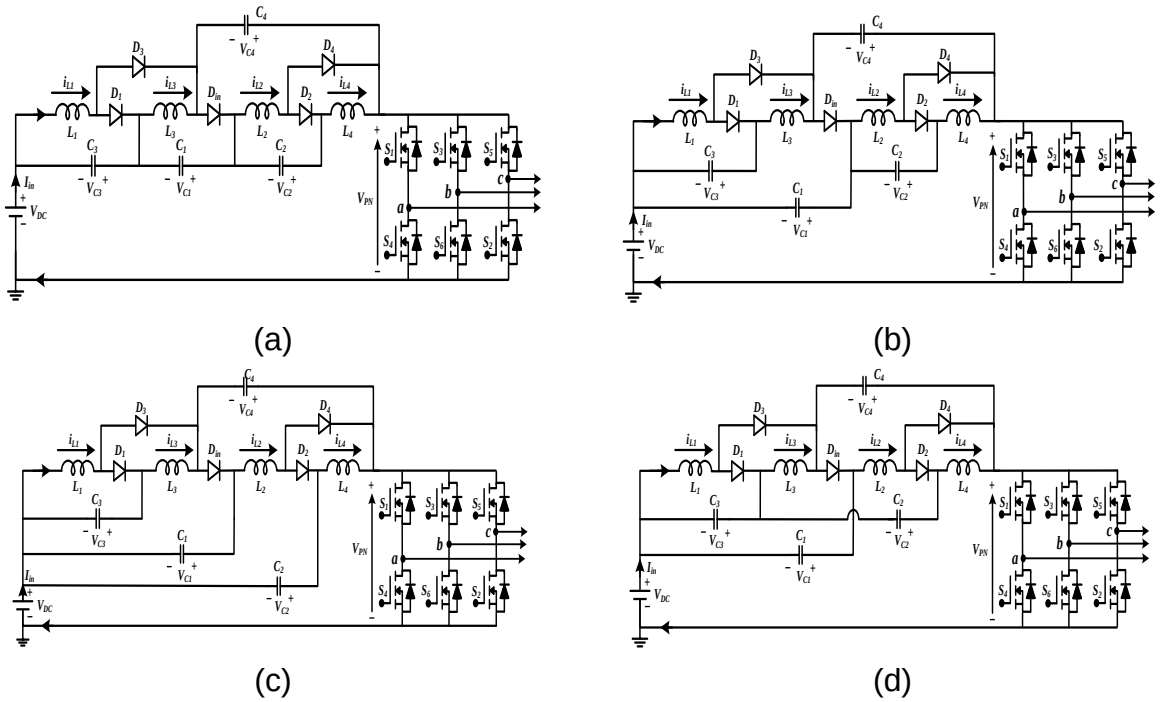


Fig. 7.2: Different configurations of proposed EB-qZSIs for: (a) configuration-1; (b) configuration-2; (c) configuration-3; and (d) configuration-4.

7.3 Circuit Configurations and Operating Principles of the Proposed Topologies

The four different circuit configurations of the proposed enhanced-boost qZSIs topologies are shown in Fig. 7.2. The components (i.e., both passive and active) used in these four topologies are same as that of the EB-ZSI [73]/ EB-qZSIs [74] (i.e., the impedance network is having four inductors (L_1, L_2, L_3, and L_4), four capacitors (C_1, C_2, C_3, and C_4), and five diodes (D_{in}, D_1, D_2, D_3, and D_4)). These components are grouped into two-switched impedance networks. The combination of L_1–L_3–D_1–D_3–C_1–C_3 forms one switched-impedance network and the combination of L_2–L_4–D_2–D_4–C_2–C_4 forms other switched-impedance network.

As discussed in [73], the EB-ZSI provides discrete input current due to input diode D_{in}. To increase the boost factor, shoot-through duty ratio has to increase which increases the discontinuity in the input current.

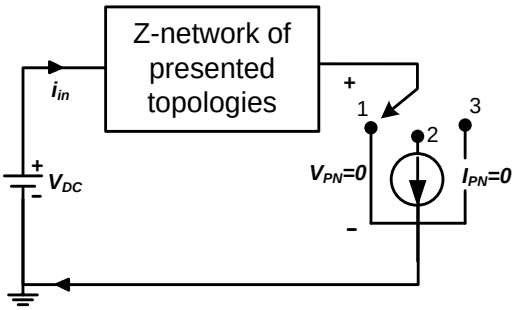


Fig. 7.3: Simplified equivalent circuit of presented topologies.

Similar to EB-SZSI discussed in Chapter 6, these proposed topologies also provide discrete input current as can be seen from Fig. 7.3. Moreover, these topologies reduce the starting inrush current problem. Akin to EB-qZSIs [74], the presented topologies shares common ground with the source and inverter bridge, reduces the capacitors stress, and reduces staring inrush current. The only difference between these proposed topologies and the EB-qZSIs [74] is that, the input current drawing from the supply is discontinuous. All these topologies can be modulated using the modulation methods proposed for the traditional ZSIs [21 – 40]. In this context, the simple boost method [21] is used for the analysis and hardware tests. All these four topologies are presented in the following sections.

7.3.1 Configuration-1

The illustration of enhanced-boost qZSI in configuration-1 is depicted in Fig. 7.2(a), which consists of four inductors, four capacitors, and five diodes in the impedance network.

The operating principle of the proposed topology is same as that of the traditional ZSI, having shoot-through states in addition to the non-shoot-though states (i.e., traditional six active states and two zero states for three phase system). The operating states of the EB-qZSI for configuration-1 shown in Fig. 7.2(a) can be divided into two states: shoot-through state and non-shoot-through state.

7.3.1.1 Shoot-Through State

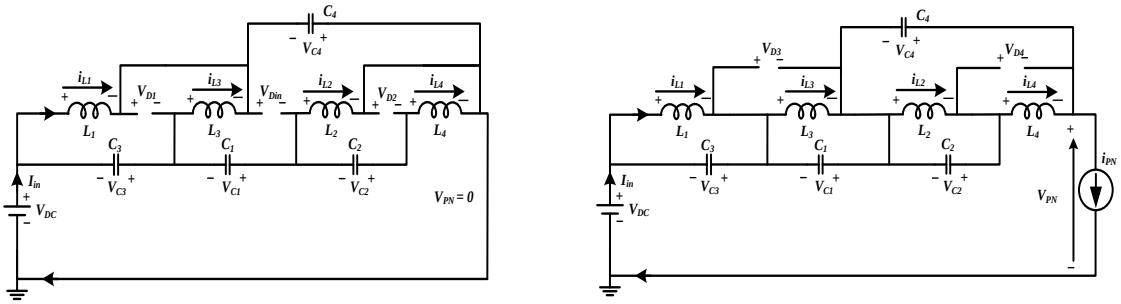
The equivalent circuit of the proposed topology in configuration-1 during shoot-through state is shown in Fig. 7.4(a). During this state, both the devices of any one–phase or any two–phase and all the three–phase legs are turned on simultaneously to boost the input voltage. The diodes D_{in}, D_1, and D_2 are off, while the diodes D_3 and D_4 are turned on during this condition. All the inductors are charged by the input supply and the capacitors and these inductors stores the energy.

According to Kirchhoff's voltage law (KVL), the inductor and diode voltages can be expressed as

$$\begin{cases} V_{L1} = V_{DC} + V_{C4};\ V_{L2} = V_{DC} + V_{C1} + V_{C3} \\ V_{L3} = V_{DC} + V_{C3} + V_{C4};\ V_{L4} = V_{DC} + V_{C1} + V_{C2} + V_{C3} \end{cases} \tag{7.2}$$

$$\begin{cases} V_{Din} = -(V_{DC} + V_{C1} + V_{C3} + V_{C4});\ V_{D1} = -(V_{DC} + V_{C3} + V_{C4}) \\ V_{D2} = -(V_{DC} + V_{C1} + V_{C2} + V_{C3}) \end{cases} \tag{7.3}$$

and the dc-link voltage, $V_{PN} = 0$.



(a) (b)

Fig. 7.4: Equivalent circuits of configuration-1 in: (a) shoot-through state; (b) non-shoot-through state.

7.3.1.2 Non-Shoot-Through State

Fig. 7.4(b) shows the equivalent circuit of the proposed topology in configuration-1 during non-shoot-through state. During this state, diodes D_{in}, D_1, and D_2 are on, while the diodes D_3 and D_4 are turned off during this condition. The electromagnetic energy stored in inductors and the input energy is transferred to the dc-link to boost the voltage. The capacitors are charged from the supply and store the energy.

The following equations can be obtained after applying KVL to Fig. 7.4(b).

$$\begin{cases} V_{L1} = -V_{C3};\ V_{L2} = -V_{C2} \\ V_{L3} = -V_{C1};\ V_{L4} = V_{C2} - V_{C4} \end{cases} \tag{7.4}$$

$$V_{D3} = -V_{C1};\ V_{D4} = V_{C2} - V_{C4} \tag{7.5}$$

7.3.1.3 Derivation of Boost Factor Expression

Applying voltage-second balance principle to inductor L_1, L_2 and L_3, the following expression can be derived respectively,

$$V_{C3} = \frac{D_0(V_{DC} + V_{C4})}{(1 - D_0)} \tag{7.6}$$

$$V_{C2} = \frac{D_0(V_{DC} + V_{C1} + V_{C3})}{(1 - D_0)} \tag{7.7}$$

$$V_{C1} = \frac{D_0(V_{DC} + V_{C3} + V_{C4})}{(1 - D_0)} \tag{7.8}$$

Similarly, in steady-state condition, the average voltage across the inductor L_4 is zero, therefore

$$D_0(V_{DC} + V_{C1} + V_{C2} + V_{C3}) + (1 - D_0)(V_{C2} - V_{C4}) = 0 \tag{7.9}$$

Substituting equation (7.6) and (7.7) in the above equation, we get

$$V_{C1}D_0(2 - D_0) + V_{C3}D_0 + V_{C4}(2D_0 - 1) + 2V_{DC}D_0 = 0 \tag{7.10}$$

After substituting (7.8) in (7.10), we get the following expression in terms of V_{C3} and V_{C4} as

$$V_{C3}D_0(D_0 + 1 - D_0^2) + V_{C4}D_0 + V_{C4}(3D_0 - D_0^3 - 1) + V_{DC}D_0(2 - D_0^2) = 0 \tag{7.11}$$

By substituting (7.6) in above expression, we get the capacitor C_4 voltage as

$$V_{C4} = \frac{D_0(2 - D_0)}{1 - 4D_0 + 2D_0^2} V_{DC} \tag{7.12}$$

Now from (7.6), the stress across the capacitor C_3 can be expressed as

$$V_{C3} = \frac{D_0(1 - D_0)}{1 - 4D_0 + 2D_0^2} V_{DC} \tag{7.13}$$

From (7.12) and (7.13), the capacitor C_1 voltage can be obtained from (7.8) as

$$V_{C1} = \frac{D_0}{1 - 4D_0 + 2D_0^2} V_{DC} \tag{7.14}$$

After substituting the expressions of V_{C1} and V_{C3} in (7.7), the capacitor C_2 voltage is obtained as

$$V_{C2} = \frac{D_0(1 - D_0)}{1 - 4D_0 + 2D_0^2} V_{DC} \tag{7.15}$$

The peak dc-link voltage across the inverter bridge during non-shoot-through state can be expressed as

$$\hat{V_{PN}} = V_{DC} + V_{C1} + V_{C3} + V_{C4} \tag{7.16}$$

Substituting the capacitor C_1, C_3, and C_4 voltages in above equation,

$$\begin{cases} \hat{V_{PN}} = \dfrac{1}{1 - 4D_0 + 2D_0^2} V_{DC} \\ \quad = B_1 V_{DC} \end{cases} \tag{7.17}$$

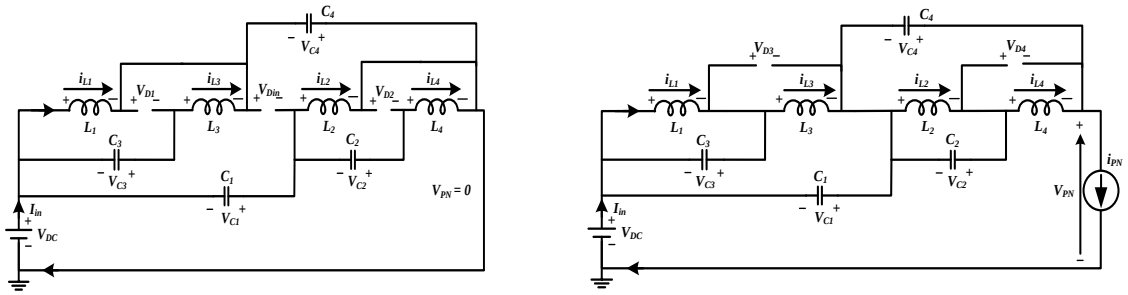
where B_1 is the boost factor of configuration-1 and defined as

$$B_1 = \frac{\hat{V_{PN}}}{V_{DC}} = \frac{1}{1-4D_0+2D_0^2} \tag{7.18}$$

Similarly, the expression of boost factor can be obtained for remaining three configurations as below.

7.3.2 Configuration-2

Similar to configuration-1, the impedance network of configuration-2 is also having four inductors, four capacitors, and five diodes and is depicted in Fig. 7.2(b). In this topology, the negative terminal of capacitors C_1 and C_3 are connected to positive polarity of the input supply, whereas the negative terminal of capacitor C_2 is connected to positive polarity of capacitor C_1. This configuration is also having two operation states: shoot-through and non-shoot-through states.



(a) (b)

Fig. 7.5: Equivalent circuits of configuration-2 in: (a) shoot-through state; (b) non-shoot-through state.

7.3.2.1 Shoot-Through State

Fig. 7.5(a) shows the equivalent circuit of the proposed topology in configuration-2. During this state, both the switching devices of any phase leg are turned on simultaneously and diodes D_{in}, D_1, and D_2 are off, while the diodes D_3 and D_4 are turned on. All the inductors are charged by the input supply and the capacitors and these inductors stores the electromagnetic energy.

Applying KVL to Fig. 7.5(a), the following inductor and diode voltages can be derived as

$$\begin{cases} V_{L1} = V_{DC} + V_{C4};\ V_{L2} = V_{DC} + V_{C1} \\ V_{L3} = V_{DC} + V_{C3} + V_{C4};\ V_{L4} = V_{DC} + V_{C1} + V_{C2} \end{cases} \tag{7.19}$$

$$\begin{cases} V_{Din} = -(V_{DC} + V_{C1} + V_{C4});\ V_{D1} = -(V_{DC} + V_{C3} + V_{C4}) \\ V_{D2} = -(V_{DC} + V_{C1} + V_{C2}) \end{cases} \tag{7.20}$$

and the dc-link voltage, $V_{PN} = 0$.

7.3.2.2 Non-Shoot-Through State

Fig. 7.5(b) shows the illustration of the proposed topology during non-shoot-through state. During this state, diodes D_{in}, D_1, and D_2 are on, while the diodes D_3 and D_4 are turned off during this condition. The electromagnetic energy stored in inductors and the input energy is transferred to main circuit.

The following expressions can be obtained according to Fig. 7.5(b).

$$\begin{cases} V_{L1} = -V_{C3};\ V_{L3} = V_{C3} - V_{C1} \\ V_{L2} = -V_{C2};\ V_{L4} = V_{C2} - V_{C4} \end{cases} \tag{7.21}$$

$$V_{D3} = V_{C3} - V_{C1};\ V_{D4} = V_{C2} - V_{C4} \tag{7.22}$$

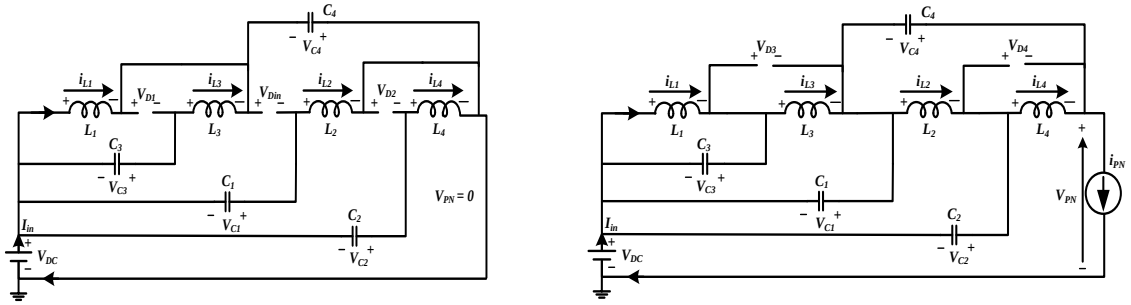
After applying volt-sec balance principle to inductors L_1, L_2, L_3, and L_4, the capacitor C_1, C_2, C_3, and C_4 voltages can be obtained as

$$\begin{cases} V_{C1} = V_{C4} = \dfrac{D_0(2-D_0)}{1-4D_0+2D_0^2} V_{DC} \\ V_{C2} = V_{C3} = \dfrac{D_0(1-D_0)}{1-4D_0+2D_0^2} V_{DC} \end{cases} \tag{7.23}$$

From Fig. 7.5(b), the peak dc-link voltage can be written as

$$\hat{V}_{PN} = V_{DC} + V_{C1} + V_{C4} = \frac{1}{1-4D_0+2D_0^2} V_{DC} = B_2 V_{DC} \tag{7.24}$$

where B_2 is the boost factor of configuration-2.



(a) (b)

Fig. 7.6: Equivalent circuits of configuration-3 in: (a) shoot-through state; (b) non-shoot-through state.

7.3.3 Configuration-3

Similar to aforementioned topologies, the impedance network of the configuration is having four inductors, four capacitors, and five diodes in the impedance network and is depicted in Fig. 7.2(c). In this configuration, the negative terminal of capacitors C_1, C_2, and C_3 are connected to positive polarity of the input supply V_{DC}. The configuration-3 also has two operation states: shoot-through and non-shoot-through states.

7.3.3.1 Shoot-Through State

Fig. 7.6(a) shows the equivalent circuit diagram for shoot-through state. During this state, the both switching devices in any phase legs are turned on simultaneously in order to boost the voltage. The diodes D_{in}, D_1, and D_2 are off, while the diodes D_3 and D_4 are turned on during this state. All the inductors are charged by the capacitors and these inductors stores the electromagnetic energy. The following expressions can be obtained after applying KVL in the impedance network of Fig. 7.6(a), the inductor and diode voltages can be expressed as

$$\begin{cases} V_{L1} = V_{DC} + V_{C4};\ V_{L2} = V_{DC} + V_{C1} \\ V_{L3} = V_{DC} + V_{C3} + V_{C4};\ V_{L4} = V_{DC} + V_{C2} \end{cases} \tag{7.25}$$

$$\begin{cases} V_{Din} = -(V_{DC} + V_{C1} + V_{C4}) \\ V_{D1} = -(V_{DC} + V_{C3} + V_{C4});\ V_{D2} = -(V_{DC} + V_{C2}) \end{cases} \tag{7.26}$$

and the dc-link voltage, $V_{PN} = 0$.

7.3.3.2 Non-Shoot-Through State

Fig. 7.6(b) shows the equivalent circuit of the proposed topology in configuration-3 during non-shoot-through state. During this state, diodes D_{in}, D_1, and D_2 are on, while the diodes D_3 and D_4 are turned off during this condition.

The following relationships across the inductors can be obtained after applying KVL to Fig. 7.6(b).

$$V_{L1} = -V_{C3};\ V_{L2} = V_{C1} - V_{C2};\ V_{L3} = V_{C3} - V_{C1};\ V_{L4} = V_{C2} - V_{C1} - V_{C4} \tag{7.27}$$

$$V_{D3} = V_{C3} - V_{C1};\ V_{D4} = V_{C2} - V_{C1} - V_{C4} \tag{7.28}$$

By applying volt-sec balance principle to inductors, the following capacitor voltages can be obtained as

$$\begin{cases} V_{C1} = V_{C4} = \dfrac{D_0(2 - D_0)}{1 - 4D_0 + 2D_0^2} V_{DC} \\ V_{C2} = \dfrac{D_0}{(1 - D_0)} \dfrac{(3 - 5D_0 + 2D_0^2)}{(1 - 4D_0 + 2D_0^2)} V_{DC} \\ V_{C3} = \dfrac{D_0(1 - D_0)}{1 - 4D_0 + 2D_0^2} V_{DC} \end{cases} \tag{7.29}$$

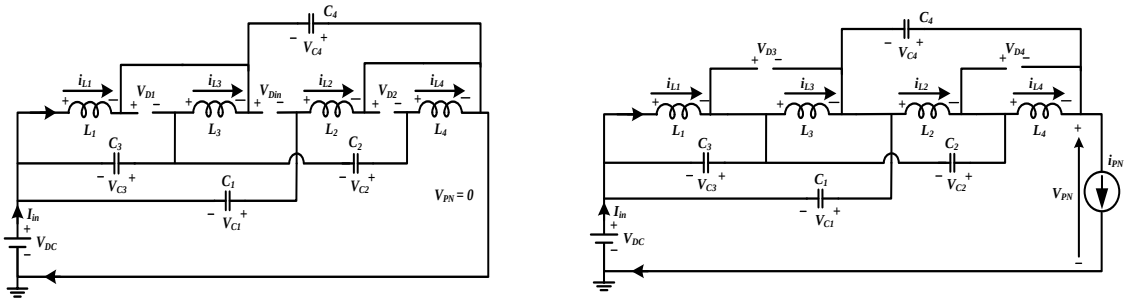
The peak dc-link voltage can be expressed as

$$\hat{V_{PN}} = V_{DC} + V_{C1} + V_{C4} = \frac{1}{1 - 4D_0 + 2D_0^2} V_{DC} = B_3 V_{DC} \tag{7.30}$$

where B_3 is the boost factor for configuration-3.

7.3.4 Configuration-4

As shown in Fig. 7.2(d), the negative terminal of capacitors C_1 and C_3 are connected to positive polarity of the input supply which is similar to Fig. 7.2(b). But the negative terminal of capacitor C_2 is connected to positive polarity of capacitor C_3 instead of C_1 to reduce the stress across the capacitor C_2. The components used in this configuration are also same as that of the other topologies.



(a) (b)

Fig. 7.7: Equivalent circuits of configuration-4 in: (a) shoot-through state; (b) non-shoot-through state.

7.3.4.1 Shoot-Through State

The illustration of the presented topology operates in shoot-through state is depicted in Fig. 7.7(a). During this state, the diodes D_3 and D_4 are on, while the diodes D_1, D_2, and D_{in} are turned off. The input voltage V_{DC} and capacitors discharges the energy to the inductors.

According to the KVL, the inductor L_1, L_2, L_3, and L_4 voltages and diode voltages are obtained as

$$\begin{cases} V_{L1} = V_{DC} + V_{C4};\ V_{L2} = V_{DC} + V_{C1} \\ V_{L3} = V_{DC} + V_{C3} + V_{C4};\ V_{L4} = V_{DC} + V_{C2} + V_{C3} \end{cases} \tag{7.31}$$

$$\begin{cases} V_{Din} = -(V_{DC} + V_{C1} + V_{C4}) \\ V_{D1} = -(V_{DC} + V_{C3} + V_{C4});\ V_{D2} = -(V_{DC} + V_{C2} + V_{C3}) \end{cases} \tag{7.32}$$

and the dc-link voltage, $V_{PN} = 0$.

7.3.4.2 Non-Shoot-Through State

The equivalent circuit of the presented topology operates in non-shoot-through state is depicted in Fig. 7.7(b). During this state, the diodes D_3 and D_4 are off, while the diodes D_1, D_2, and D_{in} are on. Capacitors C_1, C_2, C_3, and C_4 store energy, whereas the inductors L_1, L_2, L_3, and L_4 and the input voltage source discharge the energy to main circuit.

Applying KVL to Fig. 7.7(b), the following inductor voltages can be obtained.

$$\begin{cases} V_{L1} = -V_{C3};\ V_{L2} = V_{C1} - V_{C2} - V_{C3} \\ V_{L3} = V_{C3} - V_{C1};\ V_{L4} = -V_{C1} + V_{C2} + V_{C3} - V_{C4} \end{cases} \quad (7.33)$$

$$V_{D3} = V_{C3} - V_{C1};\ V_{D4} = -V_{C1} + V_{C2} + V_{C3} - V_{C4} \quad (7.34)$$

Applying the volt-sec balance principle to the inductors of impedance networks. The capacitor (C_1, C_2, C_3, and C_4) voltages can expressed as

$$\begin{cases} V_{C1} = V_{C2} = V_{C4} = \dfrac{D_0(2 - D_0)}{1 - 4D_0 + 2D_0^2} V_{DC} \\ V_{C3} = \dfrac{D_0(1 - D_0)}{1 - 4D_0 + 2D_0^2} V_{DC} \end{cases} \quad (7.35)$$

From Fig. 7.7(b), the peak dc-link voltage across the inverter bridge can be expressed as

$$\hat{V}_{PN} = V_{DC} + V_{C1} + V_{C4} = \frac{1}{1 - 4D_0 + 2D_0^2} V_{DC} = B_4 V_{DC} \quad (7.36)$$

where B_4 is the boost factor for configuration-4.

From the expressions (7.1), (7.18), (7.24), (7.30), and (7.36), it can be observed that the peak dc-link voltage of all the proposed topologies and topologies proposed in [73, 74] are same at any given input voltages and duty ratio.

After substituting the capacitors expressions expressed in (7.3), (7.20), (7.26), and (7.32), the expressions for diode D_{in} and D_1/D_2 voltages can be obtained as

$$V_{Din} = \frac{-1}{1 - 4D_0 + 2D_0^2} V_{DC} \quad (7.37)$$

$$V_{D1} = V_{D2} = \frac{-(1 - D_0)}{1 - 4D_0 + 2D_0^2} V_{DC} \quad (7.38)$$

Similarly, from (7.5), (7.22), (7.28), and (7.34), the expression for diode D_3/D_4 voltage is written as

$$V_{D3} = V_{D4} = \frac{-D_0}{1 - 4D_0 + 2D_0^2} V_{DC} \quad (7.39)$$

From the above expressions, it is observed that the voltage across the diodes in all four topologies is same and it is tabulated in Table 7.1. It is also observed in [73, 74] (as discussed in the last two chapters) that, the stress across diodes are same.

The comparison of boost factor or voltage boost of the topologies compared in Table 7.1 is depicted in Fig. 7.8(a). From this figure it is examined that the voltage boost of the proposed topologies are higher than the traditional ZSI, SL-ZSI and is same as the topologies proposed in [73, 74].

Similarly it can be derived that the average dc-link voltage across the inverter bridge of the proposed topologies is same as the EB-ZSI [73], EB-qZSIs [74] and is expressed as

$$V_{PN}^{\sim} = \frac{1-D_0}{1-4D_0+2D_0^2}V_{DC} \tag{7.40}$$

The peak-phase output voltage of the three-phase inverter is expressed by

$$V_{an}^{\wedge} = M.\frac{V_{PN}^{\wedge}}{2} = M.B\frac{V_{DC}}{2} = G\frac{V_{DC}}{2} \tag{7.41}$$

where G is the voltage gain and M is the modulation index.

The overall voltage conversion ratio G of the proposed topologies in ideal case in terms of modulation index can be defined by

$$\text{Voltage gain, } G = M.B = \frac{M}{2M^2-1} \tag{7.42}$$

7.4 Z-Network Parameter Design

Generally, the design of impedance network parameters mainly depends on the component current and voltage stresses which are summarized in Table 7.1. In this section configuration-1 is taken as an example to illustrate the parameters design and the parameters for other three topologies can be desighed in a similar way.

7.4.1 Inductors Design

As explained in Section 7.3, in shoot-through state, the inductors are charged by the capacitors, and it is also observed that the inductor voltages ($V_{L1} = V_{L2}$ and $V_{L3} = V_{L4}$) are same for all the proposed topologies and the topologies proposed in [73, 74].

Therefore, the inductors in the impedance network of all the four proposed enhanced-boost qZSI topologies are same and can be designed by

$$\begin{cases} L_{1,2} = \dfrac{T_S D_0}{\Delta i_{L1,L2} k_0} \dfrac{(1-D_0)^2}{(1-4D_0+2D_0^2)} V_{DC} \\ L_{3,4} = \dfrac{T_S D_0}{\Delta i_{L3,L4} k_0} \dfrac{(1-D_0)}{(1-4D_0+2D_0^2)} V_{DC} \end{cases} \tag{7.43}$$

7.4.2 Capacitors Design

In shoot-through, the capacitors' current is equal to the inductors' current; hence, the capacitors can be calculated as

$$\begin{cases} C_{1,4} = \dfrac{T_S D_0}{\Delta V_{C1,C4} k_0} \dfrac{(2-3D_0+D_0^2)}{(1-4D_0+2D_0^2)} I_{PN} \\ C_2 = \dfrac{T_S D_0}{\Delta V_{C2} k_0} \dfrac{(1-D_0)^2}{(1-4D_0+2D_0^2)} I_{PN} \\ C_3 = \dfrac{T_S D_0}{\Delta V_{C3} k_0} \dfrac{(3-5D_0+2D_0^2)}{(1-4D_0+2D_0^2)} I_{PN} \end{cases} \quad (7.44)$$

where k_0 is the number of shoot-through states over a period, T_S, Δi_{Li} and ΔV_{Ci} (where *i = 1, 2, 3, 4*) represents the inductor current and capacitor voltage ripples respectively.

Table 7.1: Parameter comparison of proposed topologies with same input voltage and shoot-through duty ratio.

Parameters		EB-ZSI [73]	EB-qZSI [74]	EB-qZSI [74]	EB-SZSI	Proposed four configurations of EB-qZSIs			
						Fig. 7.2(a)	Fig. 7.2(b)	Fig. 7.2(c)	Fig. 7.2(d)
Boost Factor	$\frac{\hat{V}_{PN}}{V_{DC}}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$
Capacitor's Stress	$\frac{V_{C1}}{V_{DC}}$	$\frac{(1-D_0)^2}{1-4D_0+2D_0^2}$	$\frac{(1-D_0)^2}{1-4D_0+2D_0^2}$	$\frac{(1-D_0)^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$
	$\frac{V_{C2}}{V_{DC}}$	$\frac{(1-D_0)^2}{1-4D_0+2D_0^2}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0(3-5D_0+2D_0^2)}{(1-D_0)(1-4D_0+2D_0^2)}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$
	$\frac{V_{C3}}{V_{DC}}$	$\frac{(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{1-3D_0+D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0}{1-4D_0+2D_0^2}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{D_0(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{D_0(1-D_0)}{1-4D_0+2D_0^2}$
	$\frac{V_{C4}}{V_{DC}}$	$\frac{(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$
Diode's Stress	$\frac{V_{Din}}{V_{DC}}$	$\frac{-1*S_S}{1-4D_0+2D_0^2}$	$\frac{-1*S_S}{1-4D_0+2D_0^2}$	$\frac{-1*S_S}{1-4D_0+2D_0^2}$	$\frac{-1*S_S}{1-4D_0+2D_0^2}$	$\frac{-1*S_S}{1-4D_0+2D_0^2}$	$\frac{-1*S_S}{1-4D_0+2D_0^2}$	$\frac{-1*S_S}{1-4D_0+2D_0^2}$	$\frac{-1*S_S}{1-4D_0+2D_0^2}$
	$\frac{V_{D1,D2}}{V_{DC}}$	$\frac{-(1-D_0)*S_S}{1-4D_0+2D_0^2}$	$\frac{-(1-D_0)*S_S}{1-4D_0+2D_0^2}$	$\frac{-(1-D_0)*S_S}{1-4D_0+2D_0^2}$	$\frac{-(1-D_0)*S_S}{1-4D_0+2D_0^2}$	$\frac{-(1-D_0)*S_S}{1-4D_0+2D_0^2}$	$\frac{-(1-D_0)*S_S}{1-4D_0+2D_0^2}$	$\frac{-(1-D_0)*S_S}{1-4D_0+2D_0^2}$	$\frac{-(1-D_0)*S_S}{1-4D_0+2D_0^2}$
	$\frac{V_{D3,D4}}{V_{DC}}$	$\frac{-D_0*\overline{S_S}}{1-4D_0+2D_0^2}$	$\frac{-D_0*\overline{S_S}}{1-4D_0+2D_0^2}$	$\frac{-D_0*\overline{S_S}}{1-4D_0+2D_0^2}$	$\frac{-D_0*\overline{S_S}}{1-4D_0+2D_0^2}$	$\frac{-D_0*\overline{S_S}}{1-4D_0+2D_0^2}$	$\frac{-D_0*\overline{S_S}}{1-4D_0+2D_0^2}$	$\frac{-D_0*\overline{S_S}}{1-4D_0+2D_0^2}$	$\frac{-D_0*\overline{S_S}}{1-4D_0+2D_0^2}$
Switch Stress	$\frac{V_S}{V_{DC}}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$
Inductor Currents		$i_{L1,L2}=\frac{(1-D_0)}{1-4D_0+2D_0^2}I_{PN}$, $i_{L3,L4}=\frac{(1-D_0)^2}{1-4D_0+2D_0^2}I_{PN}$				$i_{L1,L2}=\frac{(1-D_0)}{1-4D_0+2D_0^2}I_{PN}$, $i_{L3,L4}=\frac{(1-D_0)^2}{1-4D_0+2D_0^2}I_{PN}$			
dc-link current		$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$	$(1-D_0)\frac{\hat{V}_{PN}}{R_l}$
Input Current		$2i_{L3}-I_{PN}$	i_{L1}	i_{L3}	I_{PN}	I_{PN}	I_{PN}	I_{PN}	I_{PN}

where, S_s is the shoot-through switching function in the inverter. S_s is equal to 0 when the inverter operates in the non-shoot-through states and 1 when it is in the shoot-through states.

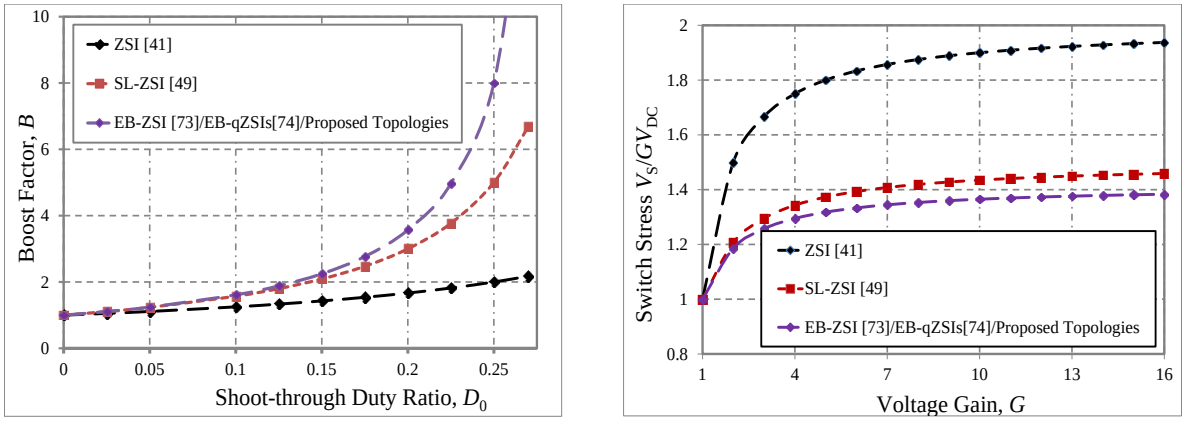
7.5 Comparison of the Proposed Topologies

In this section, the proposed four topologies are compared with other Z-source networks, such as the traditional ZSI [41], SL-ZSI [49], EB-ZSI [73], and the EB-qZSIs [74]. The comparison of boost factor, components voltage and current stresses, and the expression for input current is summarized in Table 7.1. The diodes voltage of the proposed topologies and the EB-ZSI/EB-qZSIs is same and is less than the SL-ZSI. Similarly, the number of components used, start-up current, and the nature of input current are summarized in Table 7.2. The comparisons are performed on their boost abilities and components stresses.

Table 7.2: Comparison of proposed topologies with other Z-networks

S.No	Topology	Common Ground	Start-up Current	Input Current Nature	Components			
					L	C	D	S
1	SL-ZSI [49]	No	Yes	Discontinuous	4	2	7	6
2	EB-ZSI [73]	No	Yes	Discontinuous	4	4	5	6
3	EB-qZSI [74]	Yes	No	Continuous	4	4	5	6
4	EB-qZSI [74]	Yes	No	Continuous	4	4	5	6
5	EB-SZSI	Yes	No	Continuous*	4	4	5	6
6	Proposed Topologies Fig. 7.2(a)	Yes	No	Continuous*	4	4	5	6
7	Proposed Topologies Fig. 7.2(b)	Yes	No	Continuous*	4	4	5	6
8	Proposed Topologies Fig. 7.2(c)	Yes	No	Continuous*	4	4	5	6
9	Proposed Topologies Fig. 7.2(d)	Yes	No	Continuous*	4	4	5	6

*Note: For Maximum boost control (MBC) method [22]



(a) (b)

Fig. 7.8: Comparison of: (a) boost factor; (b) switch stress.

7.5.1 Boost Factor and Switch Stress Comparison

Fig. 7.8 depicts the comparison of boost factor and stress across the semiconductor switch for the ZSI, SL-ZSI, EB-ZSI, EB-qZSIs and the proposed

topologies. As depicted in Fig. 7.8(a), for the same duty ratio D_0, the boost factor of the proposed topologies are same as the EB-ZSI/ EB-qZSIs and is stronger than the ZSI and SL-ZSI.

Similarly, the plot of switch stress versus voltage gain G for the proposed topologies and the ZSI, SL-ZSI, EB-ZSI, and EB-qZSIs are shown in Fig. 7.8(b). From this figure it is observed that the stress across the switch in the proposed topologies are same as that of the EB-ZSI/ EB-qZSIs and is less when compare to ZSI, and SL-ZSI. Therefore, lower rating switching devices can be used which reduces the cost.

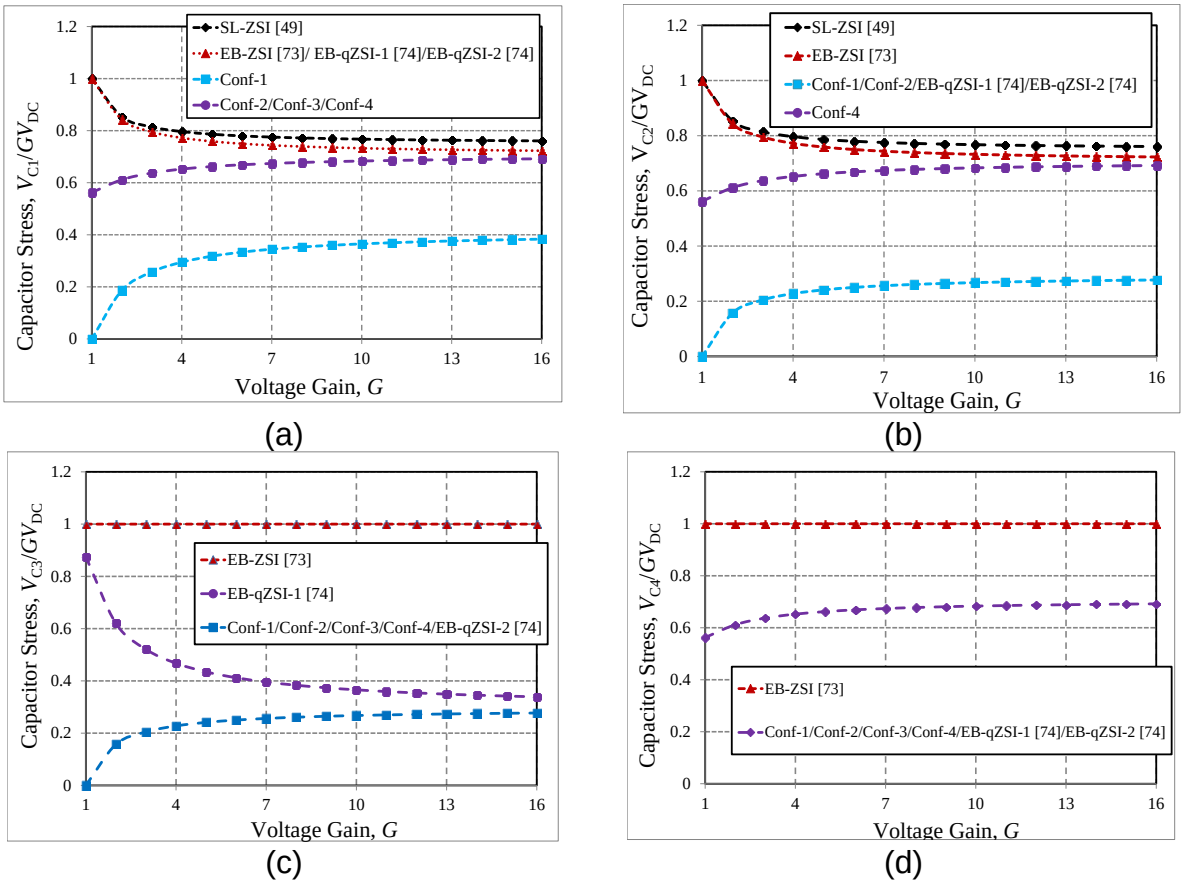


Fig. 7.9: Capacitor stress comparison of proposed topologies: (a) capacitor C_1 stress comparison; (b) capacitor C_2 stress comparison; (c) capacitor C_3 stress comparison; and (d) capacitor C_4 stress comparison.

7.5.2 Comparison of Capacitor Stresses

Fig. 7.9 depicts a plot of the capacitor's stress versus voltage gain for the proposed inverters, SL-ZSI, EB-ZSI and EB-qZSIs. The capacitor stress comparison of all the topologies compared in Table 7.1 shown in Fig. 7.9. From this figure it can be observed that the overall stress across the capacitors is less in the proposed topologies when compared to other topologies. Moreover, it is also observed that the

capacitor stress of the proposed topology in configuration-1 is less when compared to other three proposed configurations. Therefore lower rating capacitors can be used which reduces the cost of the system.

7.6 Discussion on Simulation and Experimental Results

To validate the theoretical analysis discussed in Section 7.3, the simulation and experimental test is performed with parameters shown in Table 7.3. In order to produce 110 Vrms output voltage, the proposed converter is operated using simple boost control [21] at V_{DC} = 60 V, D_0 = 0.24112, and M = 0.75888. For a given input voltage and duty cycle, all the four proposed configurations provide same dc-link voltage and are obtained as 396.3 V peak theoretically. Similarly, the theoretical values of boost factor B and voltage gain G for all the four topologies are obtained as 6.6 and 5 respectively.

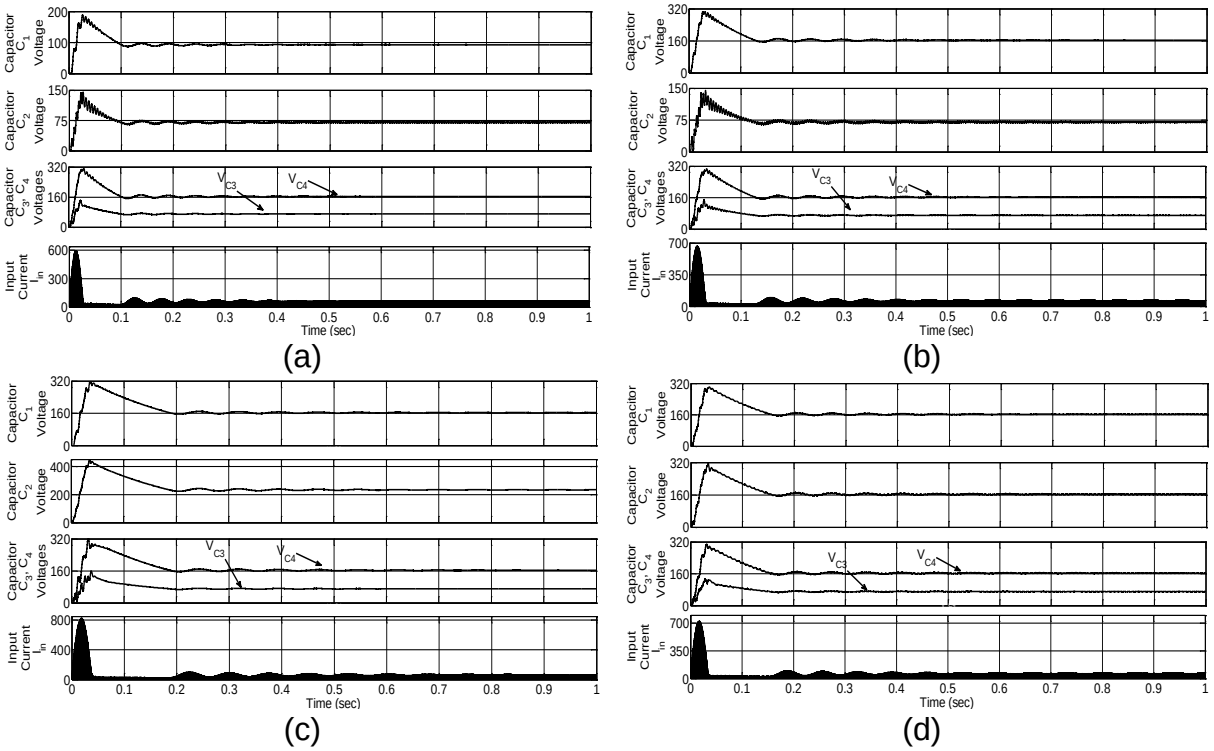


Fig. 7.10: Simulations results of capacitor voltages and input current for: (a) configuration-1; (b) configuration-2; (c) configuration-3; (d) configuration-4.

7.6.1 Simulation Results

The simulation is performed with the parameters shown in Table 7.3 at 10 kHz switching frequency. The simulation results of capacitor voltages along with input current are shown in Fig. 7.10 for all the four proposed topologies and it can be observed that the theoretical values of capacitor voltages are matching with that of simulation results. It can be seen from Fig. 7.10 and Table 7.1 that the stress across

the capacitor C_3 and C_4 is same for all the four proposed topologies. It is also observed that, the inrush current and overall capacitor stresses are less in case of configuration-1 when compare to other three configurations with same boost factor and input voltage. Therefore, configuration-1 is reported to extract other simulation and experimental results.

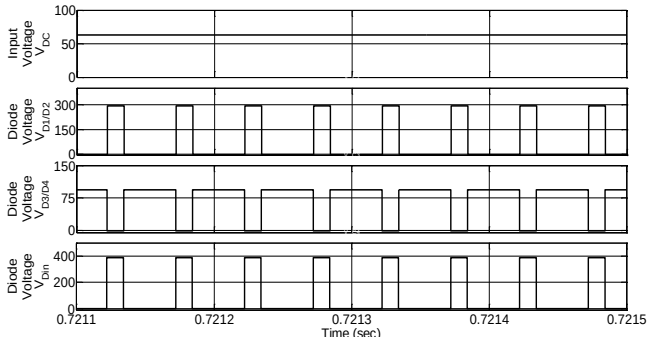


Fig. 7.11: From top to bottom, simulation results of input voltage V_{DC}, diode D_1, D_3, and D_{in} voltages.

Fig. 7.11 shows input and diode (D_1/D_2, D_3/D_4, and D_{in}) voltages. As discussed in Section 7.3, during shoot-through state, D_3 and D_4 are conducting; therefore the voltage across them is zero. Similarly in non-shoot-through state, the diode D_{in}, D_1, and D_2 are in conducting state; therefore the voltage across them also zero. The peak voltage appears across the diode D_{in}, D_1, and D_2 in shoot-through state.

The steady-state dc-link voltage, inductor, diode D_{in}, and dc-link currents are depicted in Fig. 7.12. The dc-link voltage is zero in shoot-through state due to short circuit across the inverter bridge and it provides the peak value of about 395 V in non-shoot-through state. The inductor current is increasing in shoot-though state which implies that the inductors are charging, in non-shoot-though state, the current flowing through inductor is decreasing to discharge the inductors.

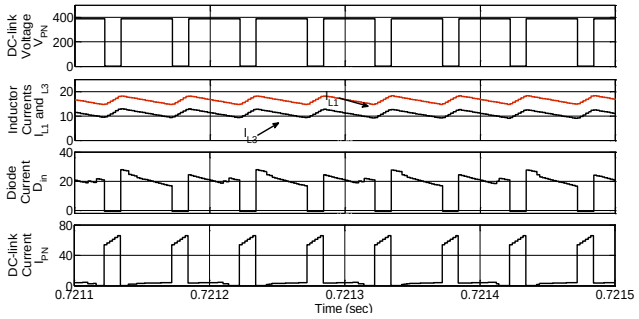


Fig. 7.12: From top to bottom, simulation results of dc-link voltage, inductor L_1, L_3 currents, diode D_{in} current and dc-link currents.

As depicted in Fig. 7.12, the dc-link current (which is same as input current) is discontinuous (i.e., during zero state, the current drawn from the supply is zero). In case of simple boost control (SBC), in zero-state, the current is zero and during

shoot-though and active states the current is non-zero. Therefore to avoid discontinuity in the input current, the maximum boost control (MBC) method can be used [22] in which all the zero states are used as shoot-through states. Moreover, the MBC also improves the boost factor due to increased shoot-through period and reduces the switch stress.

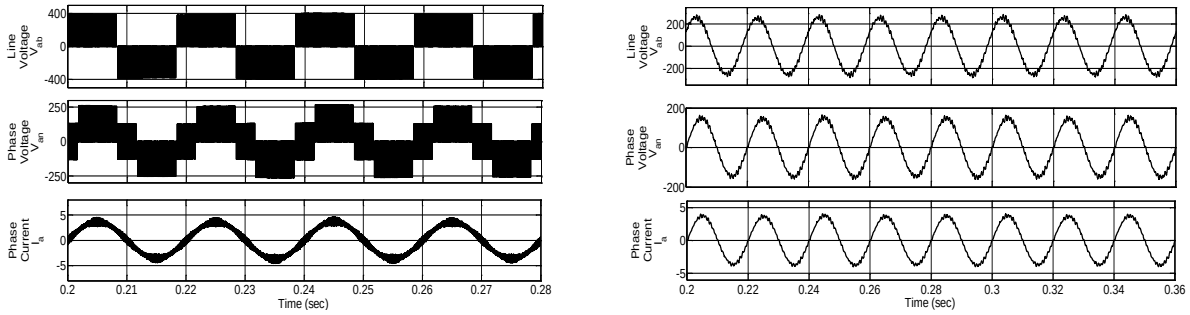


Fig. 7.13: From top to bottom, simulation results of ac-side voltages and currents: (a) without *LC* filter; (b) with *LC* filter.

Fig. 7.13 (a) depicts the ac-side output voltages (V_{ab} and V_{an}) and phase currents of the presented topology without *LC* filters. The ac-side line voltage, phase voltage and phase current with *LC* filters (1 mH, 20 µF) at output side are shown in Fig. 7.13(b). It is seen from this figure that, the line and peak phase voltages are about 280 V and 160 V (i.e., 110 V rms) respectively.

Table 7.3: Parameters for hardware setup

S.No	Parameters/ Part number	Values
1	Input DC voltage	60 V
2	Inductors	1 mH
3	Capacitors	1000 µF
4	Diodes (25NSR60)	600 V, 25 A
5	Power semiconductor switches (IRF460)	500 V, 21 A, R_{DS}(on)=0.27 Ω
6	Fundamental frequency, *f*	50 Hz
7	Duty ratio, D_0	0.24112
8	Modulation index, *M*	0.75888

7.6.2 Experimental Results

The experimental test is conducted in the laboratory with the same parameters as shown in Table 7.3 at 4 kHz swithching frequency. The input voltage along with dc-link voltage and diode voltages are depicted in Fig. 7.14(a). The peak dc-link voltage and diode D_1 voltages are boosted to 382 V and 285 V respectivily. The

diode D_3 voltage is boosted to 89 V in non-shoot-through state and is almost zero in shoot-through state.

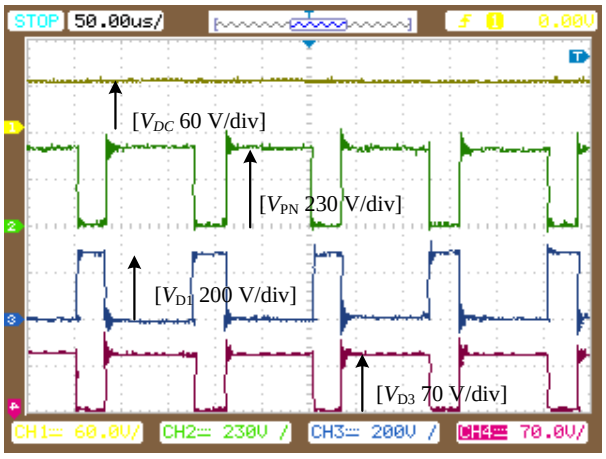


Fig. 7.14: Experimental results of input, dc-link and diode voltages.

Fig. 7.15 depicts the inductor L_1 and L_3 currents along with input I_{in} and diode D_{in} currents. It is observed that the inductors currents are increasing linearly in shoot-through state and it is decreasing linearly in non-shoot-through state which represents charging and discharging of the inductors respectively. It can be seen from this figure that the input current (same as dc-link current) is zero during zero state and it is non-zero in other states (i.e., during shoot-through state and active states).

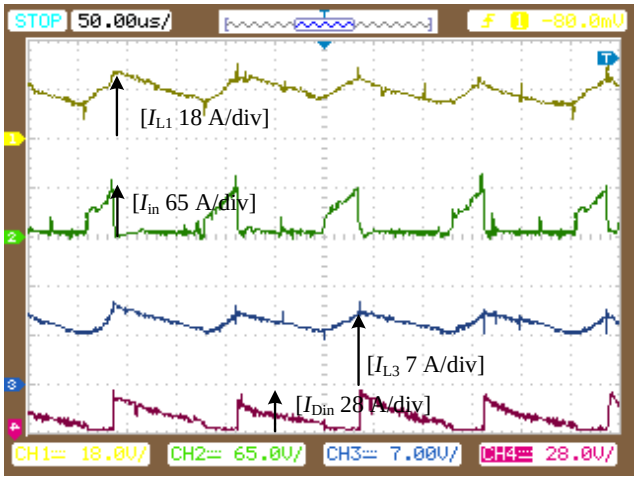


Fig. 7.15: Experimental results of inductor, input and diode currents.

Fig. 7.16 shows the steady-state capacitor C_1, C_2, C_3 and C_4 voltages. From these figures it is seen that due to drop across the diodes, inductors and switches; the experimental values are slightly less when compared to simulation and theoretical values.

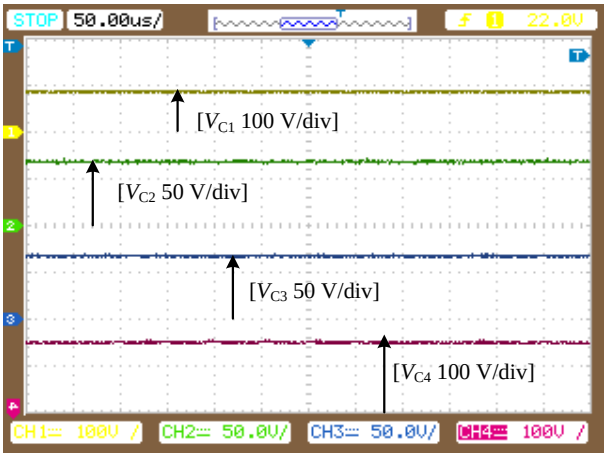
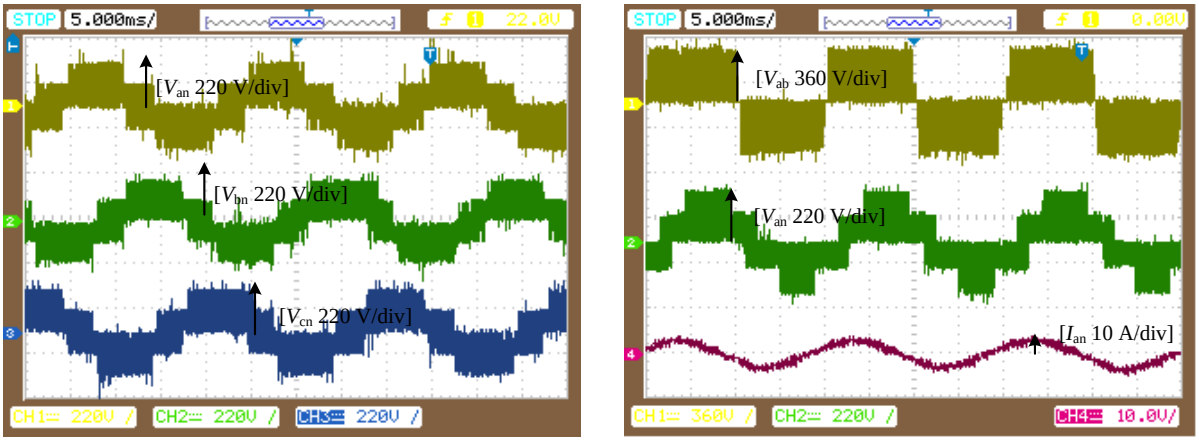


Fig. 7.16: Experimental results of capacitor C_1, C_2, C_3, and C_4 voltages (from top to bottom).

Fig. 7.17(a) depicts the phase voltages (i.e., V_{an}, V_{bn}, and V_{cn}) of three-phase system at M = 0.75888. The line voltage, phase voltage and the phase current is also obtained in Fig. 7.17(b) and it seen that the magnitude of voltages are less when compared to simulation and theoretical values.



(a) (b)

Fig. 7.17: Experimental results of: (a) ac-side voltages; (b) ac voltages and current.

7.7 Conclusion

This paper presents a new family of four different configurations of enhanced-boost quasi Z-source inverters. The proposed topologies provides very high voltage boost at high modulation index which results into high quality waveforms. Moreover, these topologies share common ground with input source and VSI bridge to reduce leakage problem. In addition, the proposed topologies reduce the capacitors stress and inrush current problem. The steady-state analysis and derivation of voltage gain and capacitor voltage stresses has been derived. The simulation and experimental results have been verified againest the theoretical expressions.

CHAPTER 8: CONCLUSIONS AND FUTURE SCOPE OF THE RESEARCH

The general conclusions of the thesis have been presented in Section 8.1. The scope for future work related to this research work has been provided in Section 8.2.

8.1 Conclusions

The general conclusion of this thesis can be divided into three parts:

a) Analysis and implementation of One SL-ZSI/ One SL-improved ZSI,
b) Analysis and implementation of high boost voltage-lift ZSI/ voltage-lift improved ZSI, and
c) Analysis and implementation of high boost inverters namely, enhanced-boost qZSIs, enhanced-boost series ZSI, and four different configurations of enhanced-boost qZSIs which are derived from enhanced-boost ZSI.

The detailed conclusions on these parts are detailed next.

As explained in introduction chapter, the high boost inverters are necessary in several renewable energy system applications mainly in solar photovoltaic (SPV) and fuel cell systems when the output of the system is connected to 110 V AC systems. As discussed in Chapter 1, the SPV module provides maximum power harvest at a particular point; therefore an inverter with high boost factor is essential. In case of traditional inverters, either a step-up transformer is used at the output terminals or a DC-DC boost converter is used at the input terminals of the inverter. Therefore, traditional voltage source inverters (VSIs) cannot provide required output voltage to AC loads/grid and an input dc-link voltage is higher than the desired peak AC output voltage. The two-stage boosted VSI provides limited boost and its reliability is not high due to shoot-through failures. These drawbacks can be alleviated by Z-source inverters (ZSI). But the traditional ZSI also provides limited boost (i.e., atmost two). Moreover, the stress across the capacitors and switches devices is high. In order to avoid these drawbacks first SL-ZSI is presented. To further reduce the stress across the switch and the capacitors, the enhanced-boost ZSI (EB-ZSI) is presented. The presented EB-ZSI is also has some drawbacks like discrete input current, more stress across the capacitors, does not share common ground, and large inrush current problem. In order to alleviate these problems, improved enhanced-boost Z-source inverters has been proposed in this thesis.

The operating principle of these presented enhanced-boost Z-source inverters is based on the shoot-through principle. Hence, high reliability and can be achieved.

Additionally, these presented enhanced-boost Z-source inverter topologies reduces the size of the capacitors when compare to EB-ZSI. Moreover, they shares common ground and reduces the problem of starting inrush current.

The enhanced-boost quasi Z-source inverters (EB-qZSIs), provides continuous input current, shares common ground, reduces capacitor stress, and eliminates the inrush current problem with same boost factor as that of the EB-ZSI. The operation and theoretical analysis is validated with simulation and experimental tests.

The enhanced-boost series Z-source inverter (EB-SZSI) is proposed to further reduce the capacitor stress with remaining advantages similar to EB-qZSIs except the discrete input current. The operation principle is validated in experimental tests.

Other enhanced-boost quasi Z-source inverters are developed based on different postioning of the capacitors at different points of enhanced-boost quasi Z-source inverters. The developed inverters are named as four different configurations of enhanced-boost quasi Z-source inverters. These four configurations EB-qZSIs provides further reduction in capacitors stress. Therefore, cost and weight of the whole system is reduced. These presented topologies are validated in experimental tests.

All these proposed topologies are tested in open loop condition by using simple boost control method as the modulation technique.

8.2 Scope of the Future Work

Some suggestions for the future research in this filed are the following.

1. With the simple boost method of PWM control, the gain of proposed high boost VL-ZSI/ VL-improved ZSI, enhanced-boost qZSIs, enhanced-boost series ZSI and four configurations of enhanced-boost qZSIs is limited by the condition that the addition of the shoot-through duty and the modulation index of the inverter bridge cannot be greater than the unity. However, in constant boost control (CBC) and maximum boost control method (MBC) of PWM this limit on the modulation index is little relaxed which can result in higher gain in these inverters.
2. More number of components (i.e., both passive and active) is used in the enhanced-boost qZSIs, enhanced-boost series ZSI and four configurations of enhanced-boost qZSIs to produce high boost factor, which may increase the size of the system. Therefore, new topologies can be explored with less

number of components in the impedance network to produce same boost factor.

3. This thesis has presented only open-loop operation of the three-phase improved enhanced-boost ZSIs. A closed loop control system for the three-phase system can be developed as part of the future research.
4. For the digital implementation of the PWM control algorithm and control system, a dSPACE DS1104 has been used in this thesis. The possibility of the digital signal processor (DSP) and field-programmable gate array (FPGA) based digital implementation of the control system can be explored as part of the future research.

Fig. 1: Front view of the experimental set-up and host computer running D-SPACE.

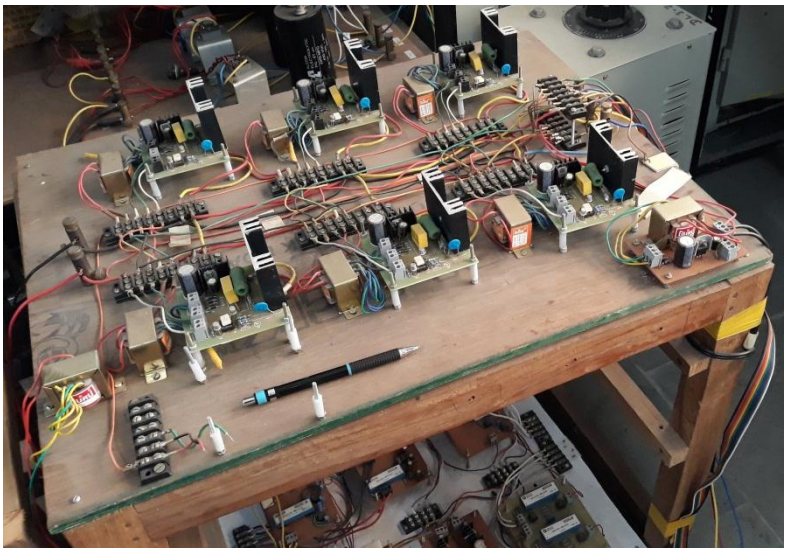


Fig. 2: Side view of the experimental set-up VSI bridge.

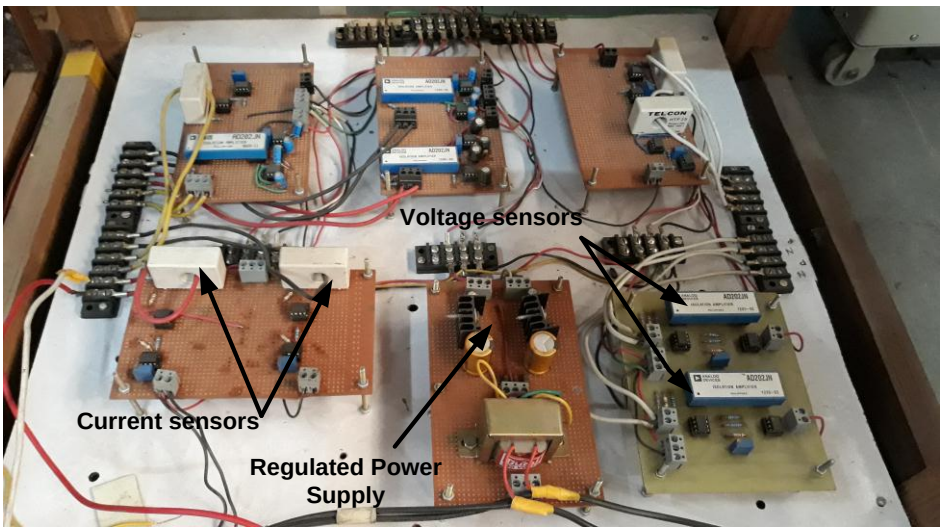


Fig. 3: Circuit diagrams of voltage and current sensors.

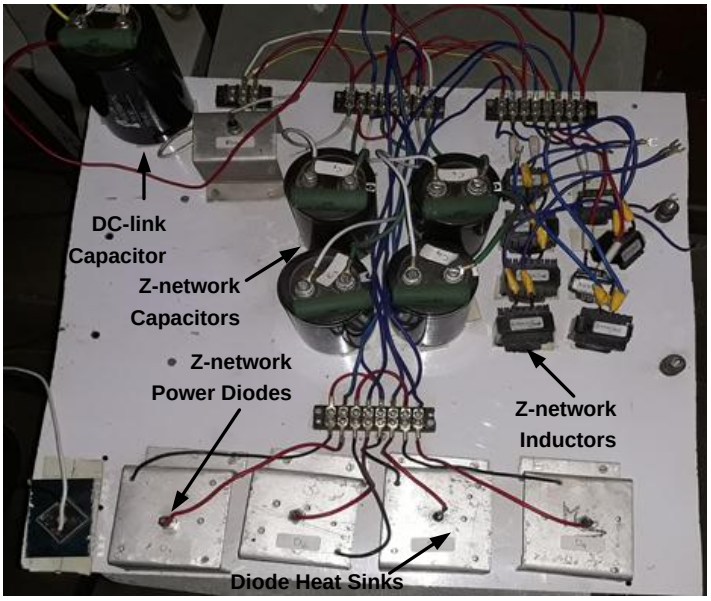


Fig. 4: Impedance (-Z) source network.

PUBLICATIONS FROM THE WORK

IEEE Transactions and Journals:

[1] **V. Jagan,** J. Kotturu, and S. Das, “Enhanced-Boost Quasi-Z-Source Inverters with Two Switched-Impedance Network*,” IEEE Transactions on Industrial Electronics,* vol. 64, no. 09, pp. 6885-6897, Sept. 2017.

[2] **V. Jagan** and S. Das, “Four Different Configurations of Enhanced-Boost Quasi-Z-Source Inverters**,”** *IEEE Transactions on Industrial Electronics,* (Under Review).

[3] **V. Jagan** and S. Das, “Steady-state and state-space analysis of enhanced-boost series Z-source inverter,” Electric Power Components and Systems, Taylor and Francis. (Submitted)**.**

IEEE International and National Conferences:

[1] **V. Jagan** and S. Das, “High boosting type Z-source inverter/ improved Z-source inverter for solar photovoltaic system,” in *Proc. of 12th Annual IEEE India Int. Conf. (INDICON 2015)*, Dec. 2015, pp. 1–6.

[2] **V. Jagan** and S. Das, “Two-Tapped Inductor quasi Impedance Source Inverter (2TL-qZSI) for PV applications,” in *Proc. IEEE 6th Int. Conf. on Power Systems (ICPS 2016)*, Mar. 2016, pp. 1–6.

[3] **V. Jagan** and S. Das, “Modified Switched Boost Inverter with reduced Voltage Stress across the Switch,” in *Proc. IEEE First Int. Conf. on Power Electronics, Intelligent Control and Energy Systems (ICPEICES 2016)*, July. 2016, pp. 1–5.

[4] **V. Jagan** and S. Das, “One Switched-Inductor Z-Source Inverter,” in *Proc. IEEE Int. Conf. on Innovations in Power and Advanced Computing Technologies (i-PACT 2017)*, Apr. 2017, pp. 1–6.

[5] **V. Jagan,** V. Bhaskar, and S. Das, “Reduced Capacitor Stress One Switched-Inductor Improved Z-Source Inverter,” in *Proc. IEEE Int. Conf. on Innovations in Power and Advanced Computing Technologies (i-PACT 2017)*, Apr. 2017, pp. 1–6.

[6] .**V. Jagan** and S. Das, “Reduced Capacitor Stress Enhanced-Boost Improved-Z-Source Inverter,” in *Proc. of 14th Annual IEEE India Int. Conf. (INDICON 2017)*, Dec. 2017, pp. 1-6.

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Ripple and Voltage Stress," IEEE Transactions on Industry Applications, vol. 42, no. 3, pp. 770-778, May-June 2006.

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The hardware system, interfacing of dSPACE–DS1104, and experimentation for the laboratory prototype of the proposed impedance (Z)-network topologies have been described in detail to validate the theoretical analysis and simulation results presented in previous chapters. Further, these experimental studies have been validated with simulation results using the experimental parameters.

A.1 Introduction

In order to verify the theoretical analysis and to validate the simulations of the proposed topologies performed in the respective chapters, the laboratory prototype has been developed.

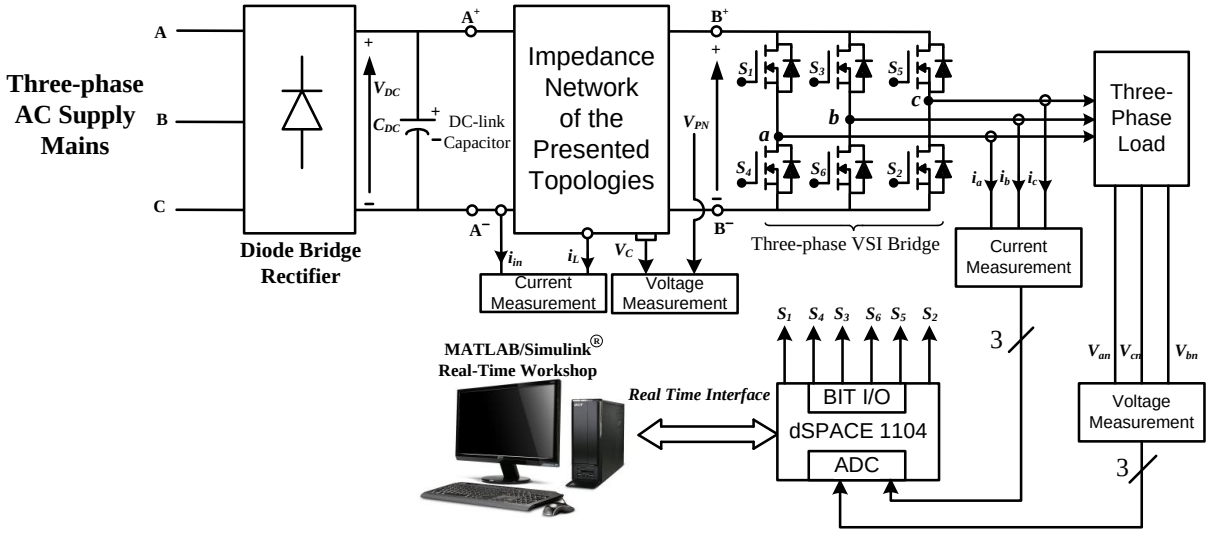

Fig. A. 1: Schematic diagram for hardware implementation.

The complete schematic diagram to perform the laboratory test for the various proposed topologies is shown in Fig. A. 1. The DC-supply to the Z-network is obtained from diode bridge rectifier and the ripples are suppressed with dc-link capacitor C_{DC}. The impedance network is a two-port network. One port (i.e., input port) of the impedance network is connected to A^+ and A^- terminals of input supply V_{DC} and other port (i.e., output port) is connected to B^+ and B^- terminals as can be seen from Fig. A. 1. The dSPACE DS 1104 has been used for the real-time simumation and implementation of control techniquies. By using the Real-Time Workshop (RTW) of MATLAB and Real-Time Interface (RTI) feature of dSPACE DS-1104, the Simulink models of the various PWM techniques for the prototypes can be implementaed. But, in this thesis, the simple boost control PWM technique is used for hardware implementation; therefore, the Simulink model for the simple boost control method has been implemented. The RTW of MATLAB generates the optimized C-

code for real-time implementation. The interface between MATLAB/Simulink and digital signal processor (DS1104 of dSPACE) allows the control algorithm to be run on the hardware. The master bit I/O is used to generate the required gate pulses to the three-phase voltage source inverter (VSI) bridge and 6 analog to digital converters (ADCs) are used to interface the sensed load currents and load voltages. An opto-isolated interface board is also used to isolate the entire DSP master bit I/O.

The development of different hardware components as required for the operation of the hardware prototypes are discussed in the next section.

A.2 Development of System Hardware

The developed experimental prototype is comprised of the following basic parts:

A.2.1. Power circuit of proposed inverter topologies

A.2.2. Control hardware development

A.2.2.1. MOSFET driver circuit

A.2.2.2. Isolation and amplification circuit

A.2.3. Measurement circuits

A.2.3.1. Current measurement circuit

A.2.3.2. Voltage measurement circuit

A.2.4. System software

A.2.1 Development of Power Circuit

A three-phase two-level voltage source inverter (VSI) with suitably designed impedance networks on its dc-side (eg. terminals B^+, B^-) has been developed. The configuration of the circuit diagram for hardware implementation is shown in Fig. A. 1. It consists of 6 self-commutated power semiconductor switches with anti-parallel diodes. The switches are realized by the MOSFETs (IRF460). To protect each switching device, a suitably designed snubber circuit is connected across it. Fig. A. 3 shows the snubber comprises which of a parallel combination of a resistor R_S and a diode D_S and this parallel combination is connected in series with capacitor C_S which is connected across a Metal-Oxide Varistor (MOV). The switching devices are mounted on heat sinks to ensure proper heat dissipation. Various parameters and rating of passive components are designed as per the design criterion.

A.2.2 Development of Control Hardware

The control/modulation algorithm is designed and built into the MATLAB/Simulink software and the control pulses for the power switches of bridge inverter are generated by real-time simulation using the dSPACE-1104. The

optimized C-code of the Simulink model of control algorithm is generated with the help of Real-Time Workshop (RTW) of MATLAB. The RTW of MATLAB and the Real-Time Interface (RTI) of dSPACE result in the real-time simulation of the model. The control pulses are generated at the various Master-bit I/Os of the dSPACE which are interfaced with the MOSFET driver circuits through pulse amplification and isolation circuits. This ensures the necessary isolation of the dSPACE hardware from the power circuit that is required for its protection. Fig. A. 2 shows the basic schematic diagram of interfacing firing pulses from the dSPACE board to switching devices of inverter. From Fig. A. 2, it can be observed that the following hardware circuits are required for interfacing of DC-AC converters with dSPACE board.

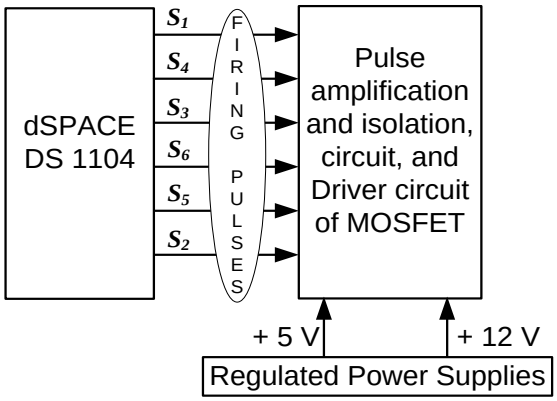

Fig. A. 2: Schematic diagram of interfacing firing pulses from dSPACE controller board to switching devices.

A.2.2.1 MOSFET Driver Circuit

To reduce the over voltage stress, the driver circuit of MOSFET along with snubber circuit for the protection of the semiconductor switch is shown in Fig. A. 3. In order to protect the switching devices, a suitably designed snubber circuit is connected across it. Fig. A. 3 shows the snubber which comprises of a parallel combination of a resistor R_S and a diode D_S and this parallel combination is connected in series with capacitor C_S which is connected across a Metal-Oxide Varistor (MOV).

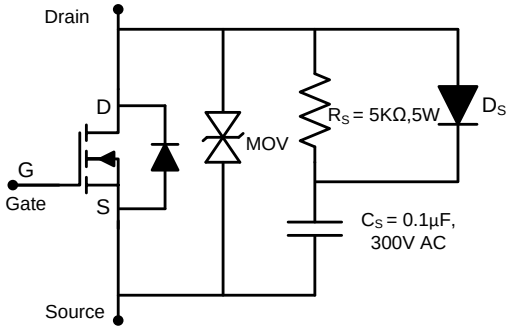

Fig. A. 3: MOSFET switch with snubber circuit for protection.

A.2.2.2 Isolation and Amplification Circuits

The MOSFET driver circuits are used for pulse amplification and isolation purposes. The control pulses generated from dSPACE unit are not efficient to drive the switching devices. Thus, these signals are further amplified by using proper amplifier circuit. Fig. A. 4 shows the circuit diagram of pulse isolation and amplifier circuit for MOSFET driver circuit. For isolation between power circuit and a control circuit, an optocoupler (MCT2E) is used. Although common + 5V, regulated DC power supply is used at the input side of the optocoupler, but individual regulated DC power supplies of + 12V are used to connect the output side of the optocoupler. In order to test the MOSFET driver, a PWM signal is applied at point 'a' of Fig. A. 4. It is may be observed that the waveform at point 'b' is similar to the PWM signal applied at point 'a', but its amplitude is increased to 12V which is used to drive the MOSFET.

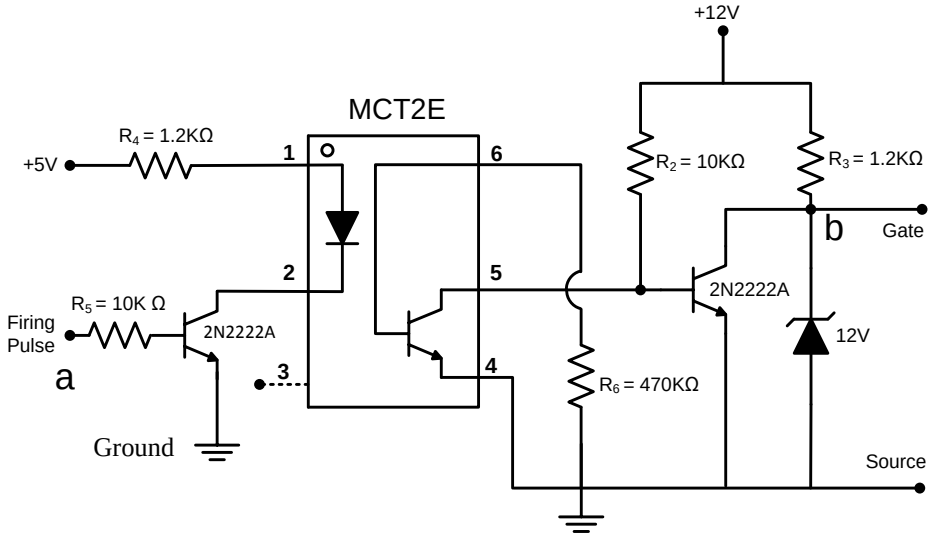

Fig. A. 4: Pulse amplification and isolation circuit.

In order to provide +5 V to pulse amplification circuit and isolation circuit, the regulated supply circuit is designed and shown in Fig. A. 5. Similarly, to provide ±12V to current and voltage sensing circuits and also for the pulse amplification and isolation circuit the regulated supply is designed and is shown in Fig. A. 6.

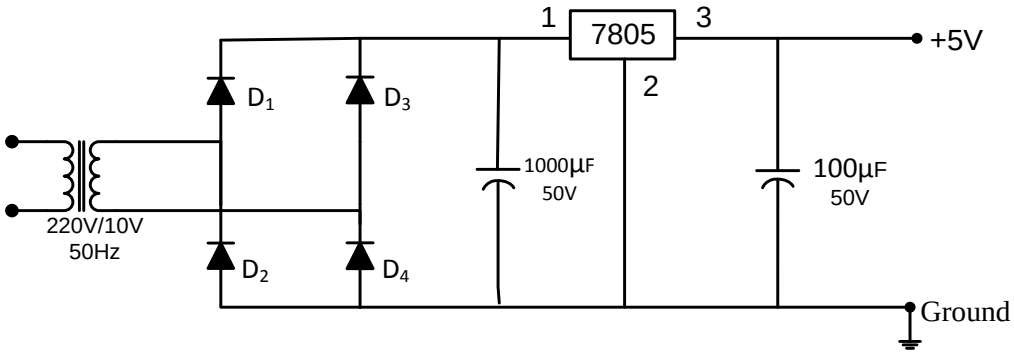

Fig. A. 5: Connection diagram for +5V regulated power supply.

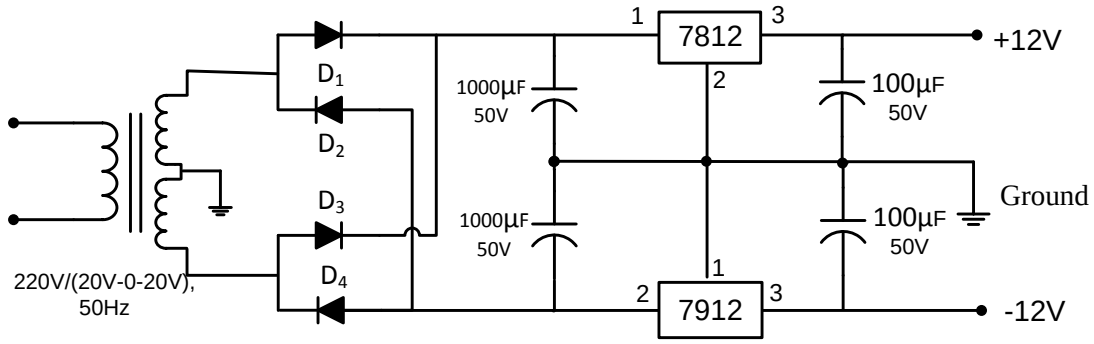

Fig. A. 6: Connection diagram for regulated power supplies: -12V, 0V, and +12V.

A. 2.3 Measurement Circuits

For accurate and reliable operation of a system, the measurement of various system parameters and their conditioning is required. The measurement system must fulfil the following requirements:

- High accuracy
- Galvanic isolation with power circuit
- Linearity and fast response
- Ease of installation and operation

With the availability of Hall-effect current sensors and isolation amplifiers, these requirements are fulfilled to a large extent.

A.2.3.1 Sensing of Current

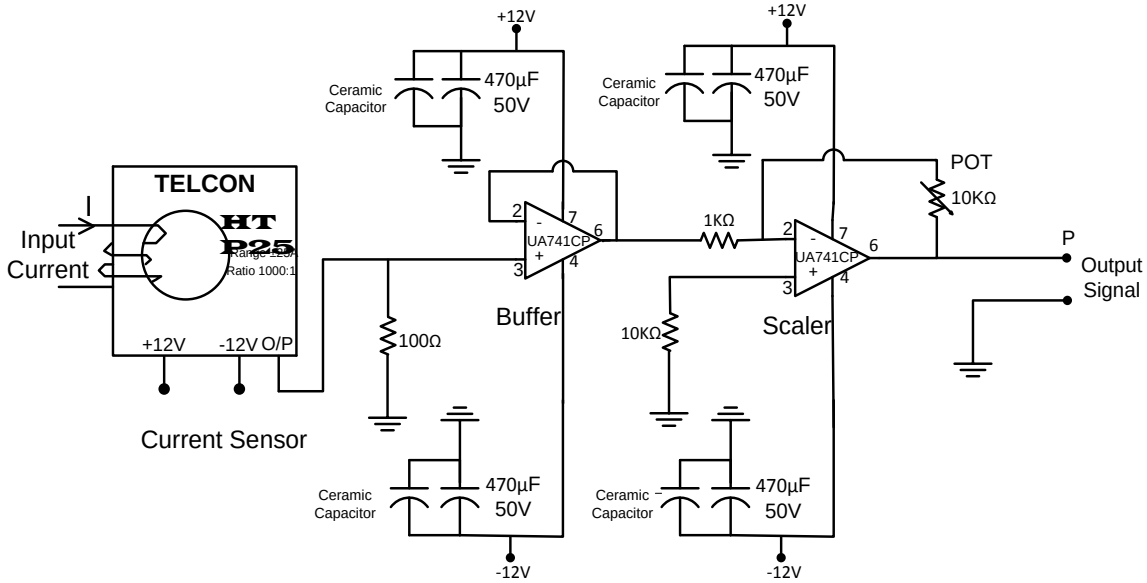

Fig. A. 7: Illustration of current sensing circuit.

The currents (eg, input current, inductor currents, and load currents) have been sensed using the PCB-mounted Hall-effect current sensors (TELCON HTP25) to extract the results. The HTP25 is a closed loop Hall-effect current transformer

suitable for measuring currents up to 25 A. This device provides an output waveform at point *P*. this oupt signal can be scalled to any value with the help of POT 10KΩ. These current sensors provide the galvanic isolation between the high voltage power circuit and the low voltage control circuit and require a nominal supply voltage of the range ±12V to ±15V. It has a transformation ratio of 1000:1 and thus, its output is scaled properly to obtain the desired value of measurement. The circuit diagram of the current sensing scheme is shown in Fig. A. 7.

A.2.3.2 Sensing of Voltage

The voltages are normally sensed using isolation amplifiers and among them, AD202JN is a general purpose, two-port, transformer-coupled isolation amplifier that can be used for measuring both ac and dc voltages. The other main features of the AD202JN isolation amplifier are:

- Small physical size
- High accuracy
- Low power consumption
- Wide bandwidth
- Excellent common-mode performance

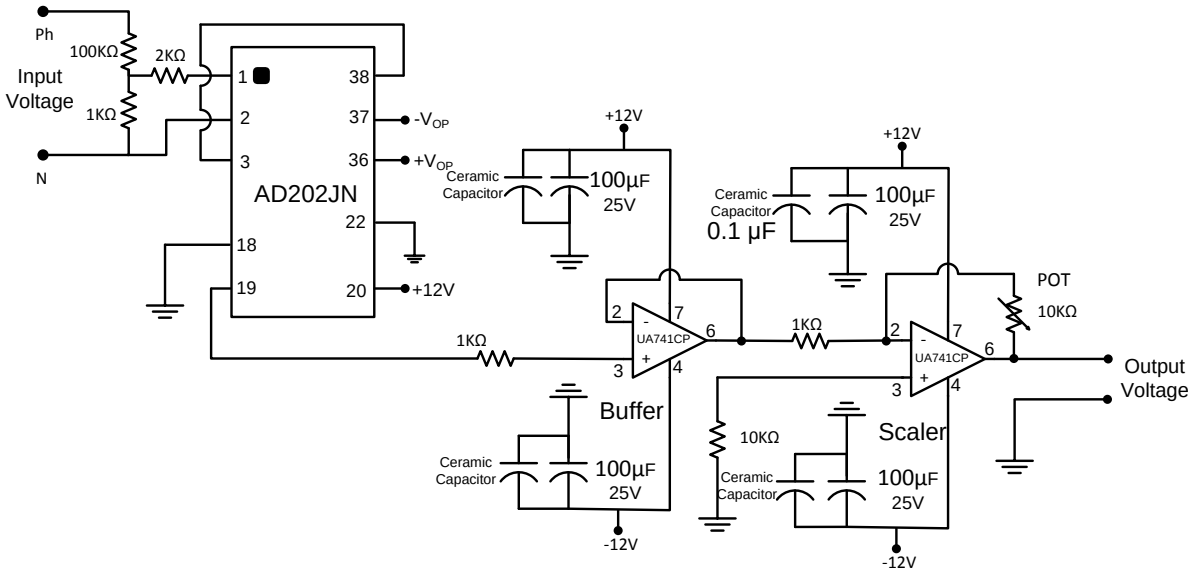

Fig. A. 8: Schematic diagram of voltage sensing circuit.

This voltage sensor can sense voltages in the range of ±1 kV (peak) and it requires a nominal supply voltage range of ±12V to ±15V. The circuit diagram for the voltage sensing scheme, which uses AD202JN isolation amplifier is depicted in Fig. A. 8.

The voltage (i.e., input DC voltage V_{DC}, capacitor voltage V_C, dc-link voltage

V_{PN}, and output volatges) to be sensed is applied between the terminals 1 and 2 (across a voltage divider comprising of 100 kΩ and 1 kΩ) and the voltage input to the sensor is available at the pins 1 and 2 of AD202JN via a resistance of 2kΩ. The isolated sensed voltage is available at the output terminal 19 of AD202JN. The output of voltage sensor is scaled properly by POT 10 kΩ to meet the requirement of the control circuit and is fed to the dSPACE via its ADC channel for further processing.

A.2.3 Development of System Software

Historically, control software was developed using assembly language. In recent years, industry began to adopt MATLAB/Simulink and Real-Time Workshop (RTW) platform based method, which provides a more systematic way to develop control software. Fig. A. 9 shows the Total Development Environment (TDE) of dSPACE and its major component blocks are explained as below:

- MATLAB is widely used as an interactive tool for modelling, analysis and visualization of systems, which itself contains more than 600 mathematical functions and supports additional toolboxes to make it more comprehensive.
- Simulink is a MATLAB add-on software that enables block diagram based modelling and analysis of linear, non-linear, discrete, continuous and hybrid systems.
- RTW is a Simulink add-on software that enables automatic C or ADA code generation from the Simulink model. The generated optimised code can be executed on PC, microcontrollers, and signal processors.
- Real Time Interface (RTI) by add-on software of dSPACE provides block libraries for I/O hardware integration of DS1006 R&D controller and generates optimized code for master and slave processors of the board.

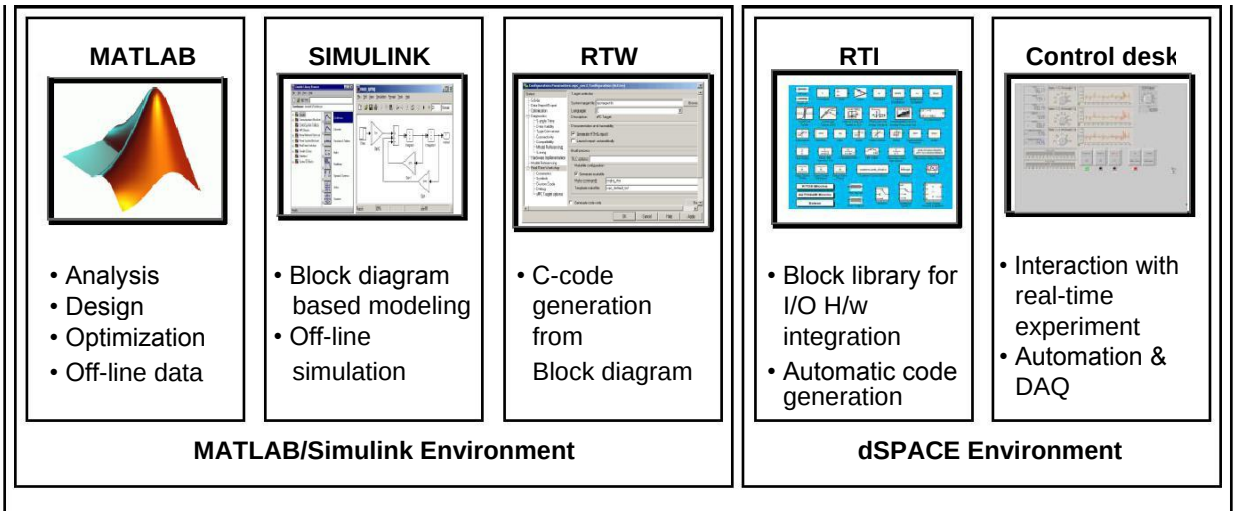

Fig. A. 9: Total Development Environment of dSPACE with MATLAB.

- dSPACE's control desk is a software tool interfacing with real-time experimental setup and provides easy and flexible analysis, visualization, data acquisition and automation of the experimental setup. The major feature of real-time simulation is that the simulation has to be carried out as quickly as the real system would actually run, thus allowing to combine the simulation and the inverter (real plant).

The DSP DS 1104 R&D controller board of dSPACE is a standard board that can be plugged into Peripheral Component Interconnect (PCI) slot of a desktop computer. The DS 1104 is specially designed for the development of high-speed multivariable digital controllers and real-time simulations for various applications. It is a complete real-time control system based on an AMD Opteron™ processor running at 2.6 GHz. It has 256 MB DDR-400 SDRAM local memory for the application and dynamic application data and 128 MB SDR SDRAM global memory for host data exchange. DS 1104 R&D controller is a very good platform for the development of dSPACE prototype system for cost-sensitive RCP applications. It is used for the real-time simulation and implementation of the control algorithm in real-time.

The sensed ac and dc voltages are fed to the dSPACE Multi-I/O Board (DS2201) of DS 1104 via the available ADC channels on its connector panel. In order to add an I/O block (such as ADCs and master bit I/Os in this case) to the Simulink model, the required block is dragged from the dSPACE I/O library and dropped into the Simulink model of the SSBC based D-STATCOM. In fact, adding a dSPACE I/O block to a Simulink model is almost like adding any Simulink block to the model. The master bit I/Os configured in the output mode, are connected to the model for issuing a gate signal tp the MOSFETs. In addition, ADCs are connected to the model for giving different sensed parameters as input to the dSPACE hardware.

The sensed signals of each topology are used for the processing in the disgned control algorithm. The vital aspect for real-time implementation is the generation of real time code of the controller tolink the host computer with the hardware. For dSPACE systems, Real-Time Interface (RTI) carries out this linkinh function. Together with RTW from the Mathswork, it automatically generates the real-time code from Simulink model into another language such as 'C'. RTI carries out the necessary steps needing only addition of the required dSPACE blocks (I/O interfaces) to the Simulink model. In other words, RTI is the interface between Simulink and various dSPACE platforms. It is basically the implementation software

for single-board hardware and connects the Simulink control modles to the I/O of the board. In the present case, the optimized C-code of the Simulink model of the control algorithm is automatically generated by the RTW of MATLAB in conjunction with RTI of dSPACE.

The generated code is then automatically downloaded into the dSPACE hardware where it is implemented in real-time and the gating signals are generated. The gating pulses for the power switches of converter are issued via the Master-bit I/Os available on the dSPACE board. The DS2201 Connector/LED combo panel provides easy-to-use connections between DS1104 board and the devices to be connected to it. The panel also provides an array of LEDs indicating the states of digital signals (gating pulses). The gating pulses are fed to various power devices driver circuits. Fig. A. 10 shows the schematic diagram of dSPACE-DS1104 board interfaced with the host computer and the real-world plant. Sensed signals are fed to the ADCs and generated gating pulses are given at Master bit I/Os.

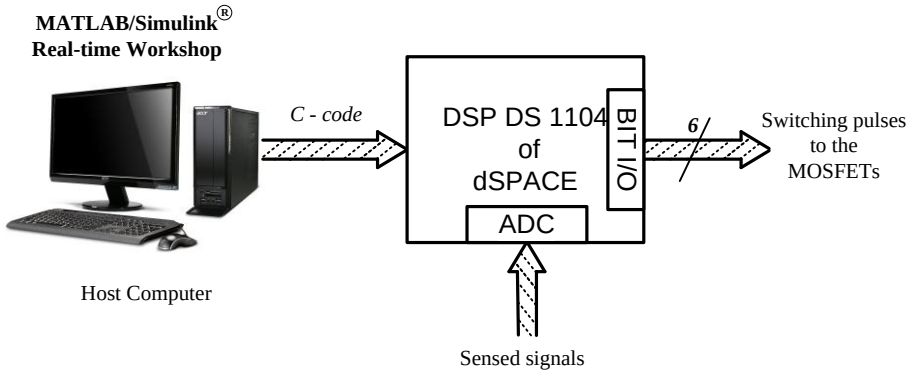

Fig. A. 10: DSP (dSPACE) circuit board interfacing.

APPENDIX – B

In this appendix, the screenshots of the MATLAB/Simulink models are shown.

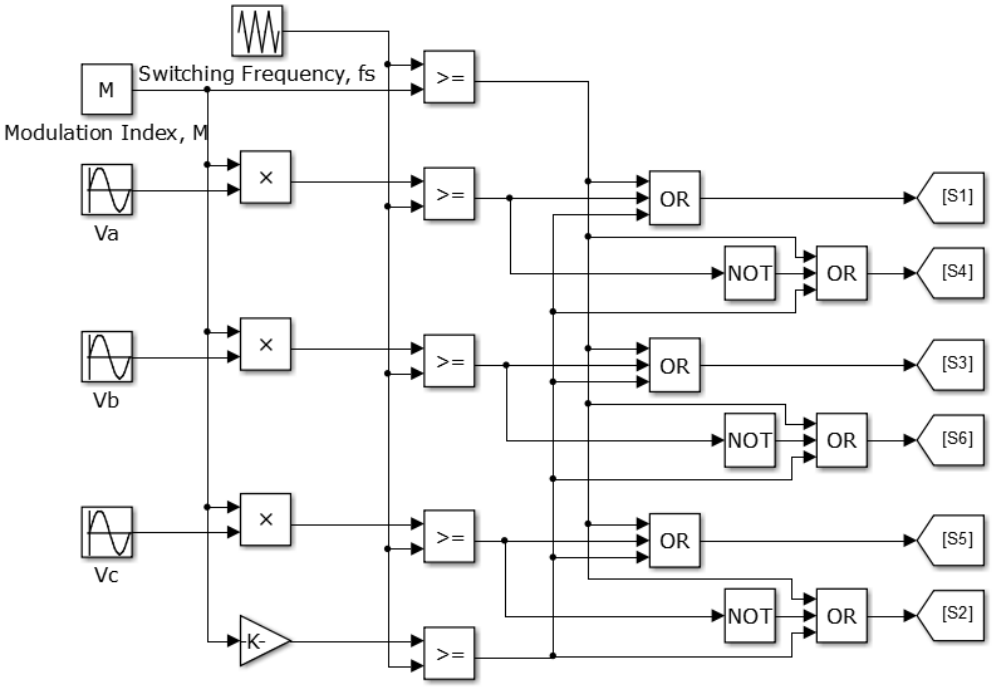

Fig. B. 1: MATLAB/Simulink model of simple boost control method for generating the firing pulses.

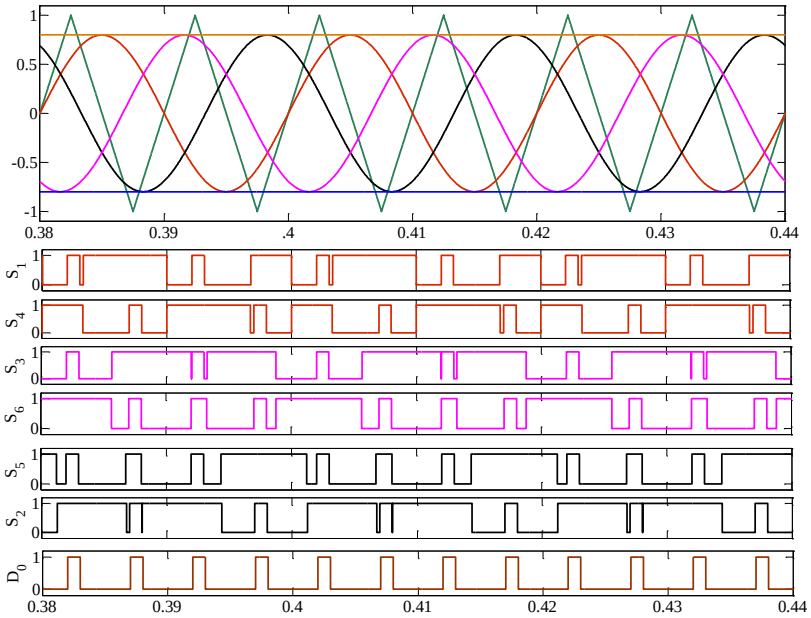

Fig. B. 2: Generation of firing pulses of simple boost control method.

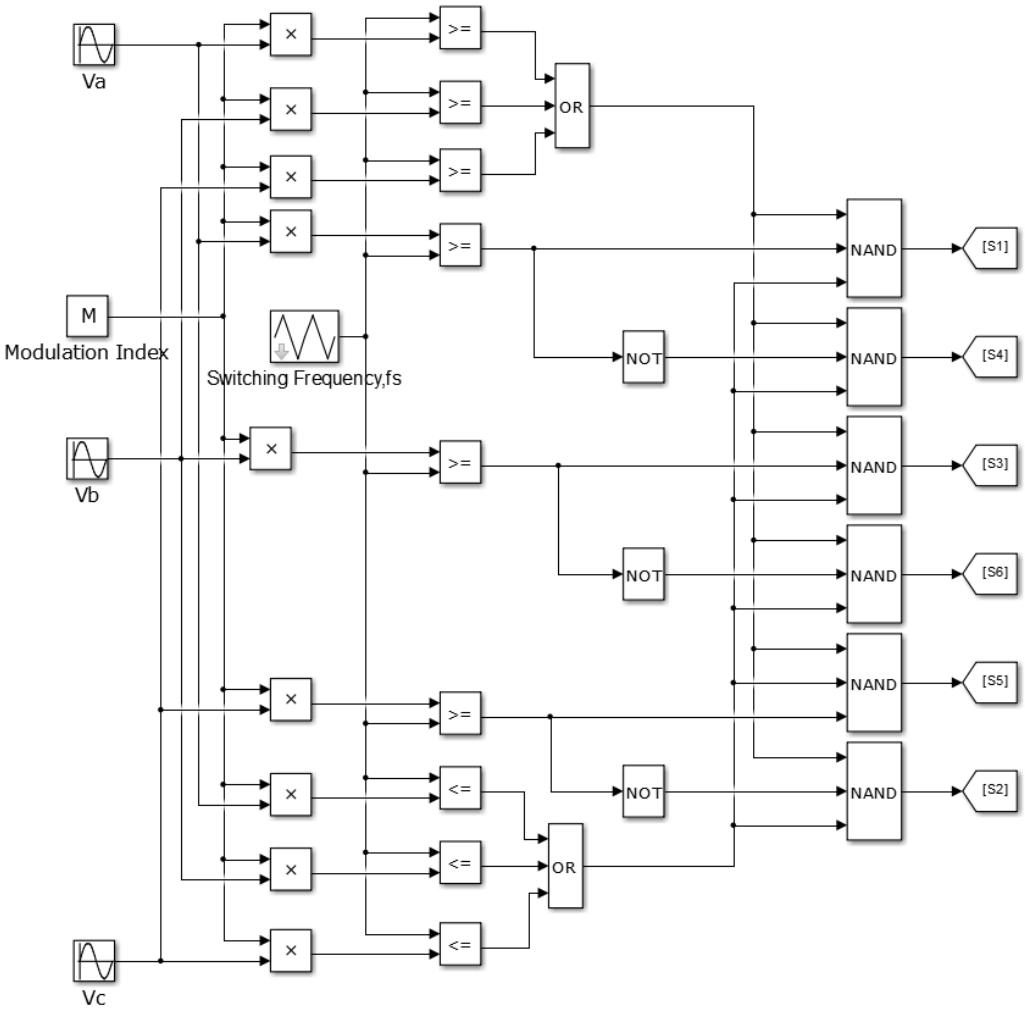

Fig. B. 3: Maximum boost control method MATLAB/Simulink model for generating firing pulses to the switches.

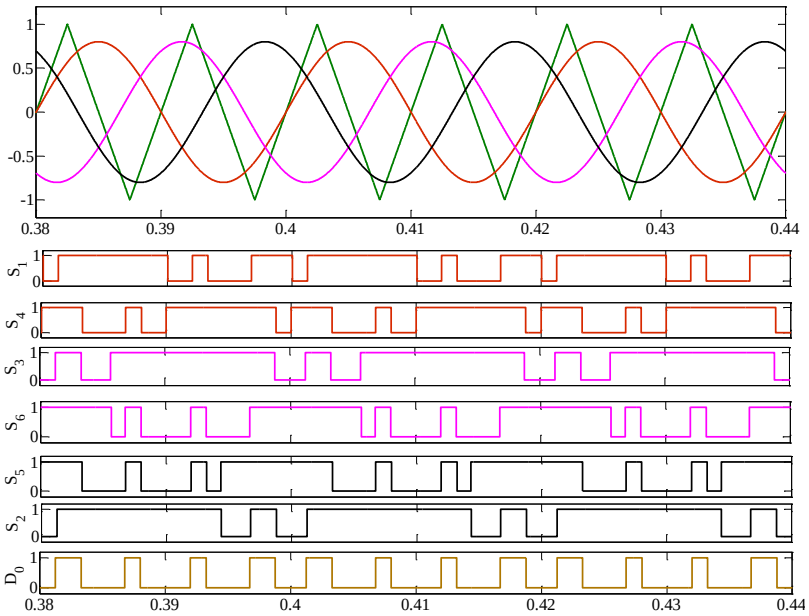

Fig. B. 4: Generation of firing pulses of maximum boost control method.