POWER QUALITY IMPROVEMENT USING MODULAR D-STATCOM

Ph.D. THESIS

by

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in this thesis entitled "**POWER QUALITY IMPROVEMENT USING MODULAR D-STATCOM"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electrical Engineering of Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from January, 2013 to March, 2018 under the supervision of Dr. M.K Pathak, Associate Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(YARLAGADDA SRINIVASA RAO)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

(M. K Pathak)
Supervisor

Dated: _____

ABSTRACT

In present scenario, majority of loads such as motor drives, fans, pumps, and power electronic converters put reactive power burden on the distribution systems. Excessive reactive power demand results into low power factor, poor voltage regulation and increases feeder losses and reduces the active power flow capability of the distribution system. Moreover, situation worsens in the presence of non-linear loads and raises power quality issues on distribution system. The primary source that draw non-linear currents from the distribution systems are power electronic devices. The operation of non-linear loads on distribution systems draw harmonics currents, which may interrupt the normal operation of other electrical equipment connected to the network. With ever-increasing penetration of power electronic devices, the power quality problem is becoming more challenging. At the same time these equipments are typically equipped with sophisticated microprocessor-based controllers which are quite sensitive to deviations of the voltage from its ideal waveform. In recent years, with the advent of sophisticated electrical and electronic equipment, the electric power quality (PQ) has become an issue of concern and extensive research is being carried out to improve the power quality.

In the early days, synchronous condenser and mechanically switched capacitors and inductors have been used for reactive power compensation. However, due to their slow response and mechanical wear and tear, use of these devices is limited for the applications where fast compensation is not needed. With the advent of the first generation of Flexible AC Transmission System (FACTS) devices, thyristor-controlled static var compensators (SVCs) schemes made significant advances in reactive power compensation as these devices are fast in operation and smooth control of reactive power compensation can be obtained with these devices. Despite the attractive theoretical simplicity of the SVC schemes, their penetration has been hindered by a number of disadvantages such as large size of capacitor and inductor banks, dependency of the reactive power compensation on operating voltage. With the remarkable progress of gate commutated semiconductor devices, attention has been focused on second generation FACTS devices which are based on self-commutated inverters. Among them, Static Synchronous Compensator (STATCOM) has attracted more attention of researches and power industry for reactive power compensation and voltage regulation in transmission systems.

Harmonic regulations or guidelines such as IEEE 519-1992 and IEC 61000 have become acceptable standards and are being applied to limit the current and voltage harmonics levels. To

meet these requirements, harmonics must be mitigated by using harmonic filters. Active and passive filters are used either together to form hybrid filters or separately to mitigate harmonics.

Conventional power quality mitigation equipment can respond only to a particular power quality problem, and this fact has attracted the attention of power engineers to develop dynamic and adjustable solutions to power quality problems. One modern and very promising group of solutions that deals with load current and/or supply voltage imperfections is the Custom Power Devices (CPDs). CPDs rectify most of the distribution system problems and many of the existing compensation devices are being replaced by CPDs, thereby reducing the cost. The family of CPDs includes distribution static synchronous compensator (D-STATCOM), dynamic voltage restorer (DVR) and unified power quality conditioners (UPQC) which are used for compensating the power quality problems in the current and/or voltage waveforms. Among these members, D-STATCOM is a shunt-connected device, which takes care of the power quality problems in the current waveform. In this thesis, an attempt has been made to develop a robust computer-controlled D-STATCOM for power quality improvement in single phase and 3P3W distribution systems.

It is well known that high performance and cost-effective inverter is a prerequisite for the realization of a D-STATCOM. These inverters can be broadly categorised into two classes, namely, voltage source inverter (VSI) and current source inverter (CSI). A critical comparison of the performance of VSI and CSI when used as a power circuit of D-STATCOM is beyond the scope of this thesis. However, in the present work, VSI has been considered as a power circuit for D-STATCOM as it has higher market penetration and a more noticeable development on VSI has taken place over the last decade, in comparison to CSI topologies. The high harmonic content of the output voltage makes basic six-pulse (two-level) VSI impractical for direct use in high-power, medium-voltage applications. Instead of using filters and connecting several switching devices in series to achieve the required voltage level, several alternative possible solutions are reported in the literature and can be broadly categorized into two groups: multipulse and multilevel inverters. The first one requires complex phase-shifting transformers and therefore, its application is limited to high-power, high-voltage systems. The second approach, multilevel inverters, uses the concept of addition of multiple small voltage levels for achieving the required voltage level with the help of additional switching devices and few components like diodes or capacitors. This approach does not require complex phase shifting transformers and hence these topologies are best suited for medium-power applications. The common multilevel inverters (MLI) topologies are the diode-clamped (DCMLI), flying capacitor (FCMLI), and cascaded multilevel inverters (CMLI) or modular multilevel cascade inverters (MMCI).

The selection of individual inverter topologies for D-STATCOM applications depends on their performance, cost, size, and implementation issues. DCMLI topology seems to be the most suited for D-STATCOM applications. But, the large number of power components and voltage unbalance problem at higher levels limits the DCMLI for low power rating applications. On the other hand, FCMLI has a natural voltage balancing operation and modular structure, but its application as a D-STATCOM is limited due to the requirement of large number of capacitors and their pre-charging. On the other hand, MMCI is one of the next generation multilevel inverters intended for high or medium-voltage power conversion without the requirement of line-frequency transformers. The MMCI is based on cascade connection of multiple single-phase H-bridge converter cells per leg. Among the members of MMCI, single-star bridge cell (SSBC) and single-delta bridge cell (SDBC) are characterized by the cascade connection of multiple single-phase H-bridge cells per leg.

The least component requirement, low cost, modular structure, easy expansion to any number of levels, high fault tolerance and absence of complex input transformer and non-initialization of the capacitor voltages make SSBC and SDBC best suited for D-STATCOM applications. Both SSBC and SDBC can reach higher output voltages and power levels (13.8 kV, 30 MVA) with readily available medium-voltage semiconductor devices. The SSBC and SDBC inverters have found input transformerless applications such as STATCOM, Battery Energy Storage System (BESS), and DVR. In this work, the application of MMCI has been extended to D-STATCOM, intended for direct installation on a medium-voltage distribution system for reactive power compensation and harmonic compensation. Towards this goal, the SSBC based inverter configuration has been chosen over SDBC as the number of converter-cells required for SDBC is 1.732 ($=\sqrt{3}$) times that required for SSBC.

In order to control the output voltage of the inverter of D-STATCOM to act as a controllable current source, a suitable modulation technique is be required for the SSBC inverter. Although a large number of different modulation schemes for multilevel inverters have been proposed in the literature, for industrial application, carrier based PWM schemes are still preferred because of their proven technology, simplicity and ease of implementation.

The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted PWM (PSPWM) and level-shifted PWM (LSPWM) techniques. The LSPWM technique produces the better harmonic performance when compared with the PSPWM technique, but it avoids the current harmonic cancellation at the input side of the phase-shifting transformer. Nevertheless, because of the unequal device conduction periods of the

LSPWM technique, it has penetrated smaller market even in those applications where transformer is not required at the input side, such as FACTS and CPDs, electric vehicle applications. The unequal device conduction periods affect the charging and discharging of the dc bus capacitors and cause non-uniform power and heat distribution in the inverter. The PSPWM distribute the switching and conduction losses evenly if the H-bridges characteristics are ideal. However if the devices characteristics are uneven or the SSBC inverter is supplying the unbalanced currents in PSPWM, the capacitor voltages deviate from the reference voltage. To prove this statement, a five level inverter the losses in a H-bridge are modeled in MATLAB from the data sheet of device characteristics to observe uneven losses among the H-bridges when supplying the unbalanced current or with different devices. In the present work, the control algorithms for capacitor voltage balancing are extended to single phase and three phase SSBC inverter with PSPWM modulation.

Towards the goal of achieving harmonic elimination and reactive power compensation with D-STATCOM, a 2.2-kV industrial three-phase, three-wire (3P3W) distribution system has been considered. For a 2.2-kV system, generally the inverter is equipped with a transformer for galvanic isolation and voltage matching between the industrial/utility distribution system voltage and the inverter voltage. However, weight and size of the transformer is more than 50% of the inverter. To alleviate this problem, the focus of this research is to design a SSBC based D-STATCOM without any line frequency transformer. The cascade number (*N*, i.e. the number of cascaded voltage source H-bridge inverters in each phase) is one of the most important design parameters for designing a transformerless PWM D-STATCOM. The value of *N* depends on the blocking voltage of the switching devices, cost, size and performance of the inverter. In the present work, IGBT has been used as the switching device and further, a cascade number of *N* equal to 2 has been chosen, considering percentage total harmonic distortion (%THD), the dc voltage requirement and the voltage rating of IGBT. This allows the use of 1.7-kV IGBTs, which are available readily at a reasonable cost. For this D-STATCOM, a suitable value of reference dc voltage for each H-bridge cell has been chosen. Ratings of various components of D-STATCOM such as DC capacitors for each H-bridge cell and inductance of coupling reactors have been designed and carefully selected.

For a single phase D-STATCOM the pq theory is used for load harmonic current extraction but if supply voltage is distorted, then a proper Reference current generated for D-STATCOM is not possible. The modified single phase pq theory with PLL is used to generate a proper reference current for D-STATCOM. The performance of modified and original pq theory is compared for different harmonic and reactive power loads. The unequal power losses arising because of

asymmetries in device characteristics and the consequent deviation of capacitor voltages is investigated with an improved modulating signal method (IMS) and is compared to active voltage superposition (AVS) method.

The performance of three-phase D-STATCOM largely depends on the control algorithm used for its implementation. The control algorithm considered in this work aims to eliminate harmonics, compensate reactive power as well as control and balance all the dc capacitor voltages of the SSBC in steady-state and in transient conditions. The load harmonic currents have been derived by using the measured voltages at point of common coupling (PCC), load currents, and the dc bus voltages of the H-bridge cells of the SSBC using Synchronous reference frame (SRP) theory. The performance of two current controllers namely PI and PI with resonant controller is investigated for different types of non-linear loads. In order to control the voltages of the floating dc capacitors of the 5-level SSBC based D-STATCOM while absorbing the unbalanced currents, the dc voltage balancing control has been divided into two control parts: (a) cluster voltage balancing control and (b) individual voltage balancing control. The former calculates the zero sequence voltage for balancing the three cluster voltages of the inverter and the later modifies the individual modulating signal for floating dc capacitors to follow their corresponding reference values. The capacitor voltage balancing method is investigated for unity power factor (UPF) and zero voltage regulation (ZVR) modes.

Computer simulation studies under different load conditions have been carried out to verify the performance of the 3P3W D-STATCOM for harmonic elimination and reactive power compensation. The simulation study of the entire system has been carried out in MATLAB/Simulink environment. Extensive simulation studies have been carried out to investigate the performance of the D-STATCOM current controllers PI and PI with resonant. The simulation studies have been performed for both steady-state and transient conditions with different non-linear and reactive loads. Further, performance of the D-STATCOM has been investigated with unity power factor and zero voltage regulation mode, the capacitor voltage balancing among the individual dc capacitors of the D-STATCOM.

In order to further verify the simulation studies of a single phase and a three-phase downscaled SSBC based inverter has been designed, constructed, and tested to verify the viability and effectiveness of the control theories, current controllers and capacitor voltage balancing methods. For hardware implementation, the power circuit of D-STATCOM is made with MOSFETs (IRFP460) as switching devices. Different hardware components as required for the operation of the experimental set-up such as pulse amplification, isolation circuit, dead-band

circuit, voltage and current sensor circuits, and non-linear/reactive loads have been designed and developed. By using the Real-Time Workshop (RTW) of MATLAB and Real-Time Interface (RTI) feature of dSPACE-DS1006, the Simulink models of the various controllers of the prototypes have been implemented. The generated firing pulses have been given to the corresponding semiconductor devices of each H-bridge of the inverter through isolation, delay, and pulse amplification circuits in real-time.

The developed prototype SSBC based D-STATCOM is used to verify the viability and effectiveness of the Current controllers for harmonic elimination and reactive compensation. In D-STATCOM implementation, each H-bridge cell is equipped with a galvanically isolated and floating dc capacitor without any power source or circuit. The SRF based controller of the D-STATCOM has been implemented in dSPACE. An uncontrolled rectifier with *RL* elements on DC side have been used as a nonlinear load.

After compensation with D-STATCOM, the source currents have been observed to be sinusoidal and their corresponding THDs being within the limits of IEEE–519–1992 recommended value of 5%. The source displacement and power factors have been found to be close to unity. The switching response and the dynamic performance of D-STATCOM for a step change in the load have been studied and in both cases, a smooth control of source current has been achieved. The regulation of capacitor voltages has been ensured by the DC voltage regulator. A smooth control of dc voltages ensures the effectiveness of the DC voltage controller. Further, the experimental results of the capacitor voltage balancing dynamics of the H-bridge cells with zero sequence voltage injection and individual capacitor voltage balancing have been studied. The experimental results have been found to be in good agreement with the simulation results.

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(Yarlagadda Srinivasa Rao)

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LIST OF SYMBOLS

v_{Sa}, v_{Sb} and v_{Sc}	Three-phase source voltages
i_{Sa}, i_{Sb} and i_{Sc}	Three-phase source currents
i_{La}, i_{Lb} and i_{Lc}	Three-phase load currents
i_{Ca}, i_{Cb} and i_{Cc}	Three-phase D-STATCOM currents
m	Number of levels in inverter
N	Cascade number
f_{cr}	Carrier signal frequency
f_m	Modulating signal frequency
m_a	Amplitude modulation index
m_f	Frequency modulation index
L_s	Source inductance
L_C	Coupling inductor of D-STATCOM
L_f	Coupling inductor of single-phase APF
L_{ac}	Commutation inductance
p, q	Instantaneous real and reactive powers
$V_{ref,c}$	Cluster reference voltage
$V_{ref,i}$	Reference dc voltage for each H-bridge cell
k_p, k_i	Proportional and integral gains

LIST OF ABBREVIATIONS

3P3W	Three-phase, Three-wire
3P4W	Three-phase, Four-wire
ac, AC	Alternating Current
APF	Active Power Filter
ASD	Adjustable Speed Drive
CHB	Cascaded H-bridge
CSD	Custom Power Device
CSI	Current Source Inverter
dc, DC	Direct Current
DCMLI	Diode Clamped Multilevel Inverter
DPF	Displacement Power Factor
DSO	Digital Storage Oscilloscope
DSP	Digital Signal Processor
D-STATCOM	Distribution Static Synchronous Compensator
EMI	Electro Magnetic Interference
FACTS	Flexible AC Transmission System
FCMLI	Flying Capacitor Multilevel Inverter
GTO	Gate Turn-off Thyristor
HVDC	High Voltage Direct Current
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical & Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
LSPWM	Level-shifted Pulsewidth Modulation
MLI	Multilevel Inverter
MOSFET	Metal Oxide Semiconductor Field-effect Transistor
PCC	Point of Common Coupling
pf, PF	Power Factor
PI	Proportional and Integral
PSPWM	Phase-shifted Pulsewidth Modulation
PWM	Pulsewidth Modulation
rms, RMS	Root Mean Square
SMPS	Switch Mode Power Supply
STATCOM	Static Synchronous Compensator

SVC	Static var Compensator
TCR	Thyristor Controlled Reactor
THD	Total Harmonic Distortion
SRF	Synchronous Reference Frame
ZVR	Zero voltage regulation
UPF	Unity power factor

CHAPTER 1: INTRODUCTION

[This chapter describes introduction to the research work. It starts with brief background on foremost power quality problems in distribution systems. Then, the various solutions to the problem have been discussed, through which D-STATCOM is selected. Finally, scope of work, author's contribution, and thesis outlines are explained.]

1.1 Overview

Traditionally, the role of the alternating current (ac) distribution system is to provide a link between the generation and transmission system to industrial, commercial, and residential load centres. The distribution system has always been susceptible to problems due to reactive power and unbalance from the very beginning [1]–[3]. But, with rapid development of semiconductor device technology in last three decades, the present day power distribution systems are also suffering from severe power quality problems[4].

The voltage and current variations in terms deviation from ideal sinusoidal waveform including frequency and amplitude variations from base values beyond the permissible levels, which are caused by the various possible situations are considered under power quality issues. Some of the causes of power quality problems are listed out as follows:

- Energization of large capacitor banks and transformers.
- Operation of reactive, non-linear and unbalanced loads.
- Failure of equipment, e.g. transformers and cables.
- Inexperience operation of distribution substations and plants.
- Lightning.
- Switching or start-up of large loads such as motors.

The above power system disturbances leads to power quality problems to the both utility and customers. Among them, reactive power, non-linear and unbalanced loads are considered to be most significant causes of power quality problems in modern distribution systems.

The low power factor, higher harmonic currents, poor voltage regulation and excess neutral currents are caused by the operation of non-linear and unbalanced loads on power distribution systems. The increased reactive power, harmonics and unbalance cause increase in line losses, and voltage distortion in the power system. For completeness, the aforementioned problems are briefly discussed below.

1.2 Reactive Power Burden

Reactive power burden on distribution systems is due to the operation of loads that draw high reactive power from the system. Reactive power is a concept used by engineers to describe the background energy movement in an ac system arising from the production of electric and magnetic fields. These fields store energy which is exchanged through each ac cycle. Devices which store energy by virtue of a magnetic field produced by a flow of current are said to absorb reactive power; while those which store energy by virtue of electric fields are said to generate reactive power. Volt-ampere reactive (VAR) is a unit used to measure reactive power in an ac system.

Reactive power (var) is required to maintain the voltage to deliver active power (watt) through transmission lines and distribution feeders. Motor loads and other loads require reactive power for their successful operation. When enough reactive power is not available, the voltage sags and it is not possible to push the real power demanded by the loads through the lines.

For better understating, a simple power system model indicating the coupling between source and load[5], [6] is shown in Figure 1.1.

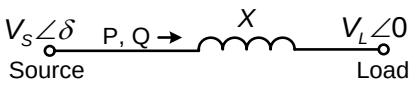


Figure 1.1 A small power system model.

In general the flow of active and reactive powers in a power system is governed by the following equations.

The transmitted active power (P) is given by,

$$P = \frac{V_S V_L}{X}\sin\delta \tag{1.1}$$

For small value of δ, the reactive power (Q) transferred to the load is given as,

$$Q = \frac{V_S(V_S - V_L)}{X} \tag{1.2}$$

The load voltage (V_L) is given by,

$$V_L = V_S - \frac{QX}{V_S} \tag{1.3}$$

Eq. (1.1) shows that the active power flow depends on the amplitudes of source voltage and load voltage and it flows from the leading voltage bus to lagging voltage bus. On the other hand, the reactive power depends mainly on the difference of voltage amplitudes across a feeder and it flows from higher voltage side to lower voltage side as given by eq. (1.2).It can be observed from eq. (1.3) that to keep the V_L fixed for a given value of V_S, the drop $\left(\frac{QX}{V_S}\right)$ must remain constant. In this expression the only variable quantity is Q, which must be locally adjusted to keep V_L fixed. In other words, let Q be the value of reactive power which keeps V_L to be a specified value, and any deviation in Q at load end must be locally adjusted. If Q is made zero (i.e. the load reactive power is supplied locally), the source and load voltages will be the same. The local generation of reactive power can be accomplished by any of the reactive power compensating device. This is the fundamental mechanism for controlling the reactive power in electric power system.

1.2.1 Sources of Reactive Power

The major sources that draw reactive power from distribution systems are[7]:

1. Phase-controlled rectifiers
2. Motors
3. Transformers, tap-changing transformers
4. Choke inductors.

1.2.2 Problems due to High Reactive Power

The high reactive power burden leads to the underutilisation of power system capacity due to:

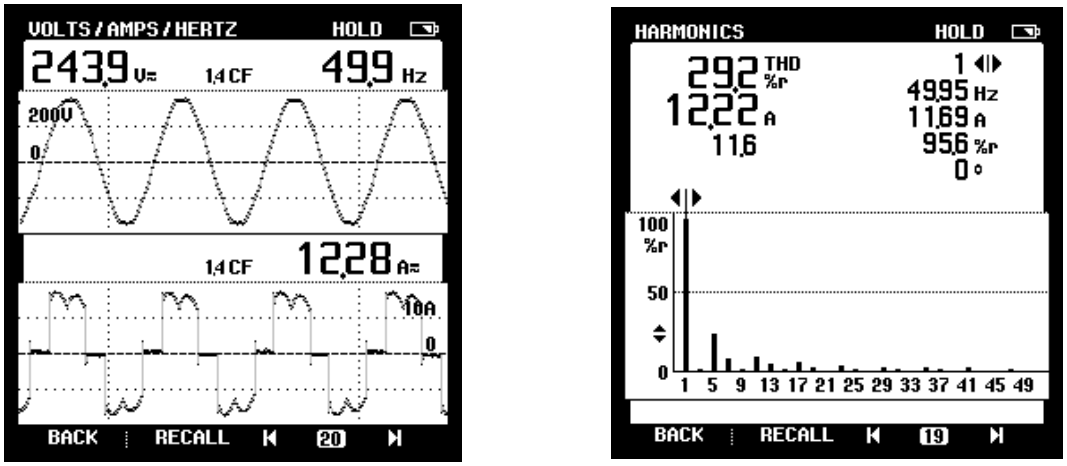
- Increased losses in the transmission and distribution systems.
- Overrated equipment within the ac system: due to larger current drawn for a given real power demand, and low efficiency owing to more losses.
- Low power factor and poor voltage regulation.

1.3 Harmonic Distortion

Harmonic distortion is caused by the operation of non-linear loads in the power system. Nonlinear loads change the sinusoidal nature of the ac power current, thereby resulting in the flow of harmonic currents in the power system that can cause interference with communication circuits and other types of electrical and electronic equipments[4], [8], [9]. Harmonics are basically the additional frequency components present in the mains voltage or current which are

integral multiples of the mains (fundamental) frequency. Interharmonics are a special category of harmonics which are non-integer multiples of the fundamental frequency. Sub-harmonics are special category of interharmonics, which have frequency values less than the fundamental frequency. Most equipments only produce odd harmonics but some devices have a fluctuating power consumption over a duration of half cycle period or less, which may generate even, inter-harmonic, or sub-harmonics currents. The harmonic distortion of each device depends on its consumption of active power, background voltage distortion and source impedance.

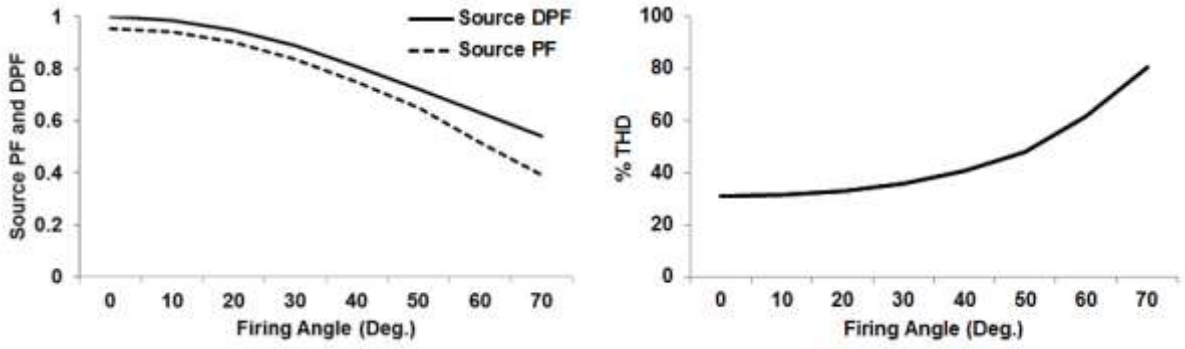
Phase controlled rectifiers are major source for harmonics and reactive power burden. They have a wide range of applications, from small rectifiers to large High Voltage Direct Current (HVDC) transmission systems. They are used for electro-chemical process, motor drives[10], traction equipment, controlled power supplies, and many other applications. The phase-a current drawn by a three phase-controlled rectifier is shown in Figure 1.2(a). The corresponding harmonic spectrum of source current is shown in Figure 1.2(b). From Figure 1.2(b) it is observed that the source current contains large amount of low order harmonics with an observed THD of 29.2%.



(a) (b)

Figure 1.2 Performance of a phase-controlled rectifier: (a) Source current of phase-a; (b) Harmonic spectrum of phase-a.

The phase-controlled rectifiers have following distinct features: a) they draw significant fundamental reactive power, whose magnitude depends on the firing angle of the rectifier, b) They draw currents with sharp rising and falling edges with high harmonic content. Source power factor, displacement factor and %THD of the load current of the phase controlled rectifier as a function of firing angle are plotted in Figure 1.3(a) and (b). From Figure 1.3 it is observed that the reactive power demand and %THD of the load current increases with the increase in firing angle of the rectifier.



(a) (b)

Figure 1.3 Performance of phase controlled rectifier: (a) Variation of source power factor and displacement factor with firing angle; (b) Variation of %THD of load current with firing angle.

1.3.1 Effects of Harmonics

Harmonics can lead to mal-operation of power system components. Some of the ways that harmonics may affect equipments negatively are listed below[8]:

1. Communication interference: Magnetic (or electrostatic) coupling between electrical power circuits and communication circuits can cause communication interference. Current flowing in the power circuit produces a magnetic (or electrostatic) field which, in turn, induces a current (or voltage) in the nearby conductors of the communication circuit. The amount of interference depends upon the magnitude of the induced current (or voltage), frequency, and the magnetic (or electrostatic) coupling. Other types of communication interference are:
    - Induced line noise
    - Interference with power line carrier systems
    - Relay malfunctions.
2. Heating: Harmonic currents can cause excessive losses in motors, capacitors and transformers connected to the system. This in turn, may cause excessive heat in the winding, thus leading to the failure of insulation and danger of fire hazard.
3. Malfunction of solid-state devices: Harmonics can cause solid-state devices to malfunction if the equipment is sensitive to zero crossings or operates in response to the peak values of utility voltage. The typical malfunctions are:
    - Errors in measurement equipment
    - Nuisance tripping of relays and breakers
    - Unstable operation of zero-voltage crossing firing circuit
    - Interference with motor controllers.

4. Damage to capacitors: The presence of capacitors, such as those used for power factor correction, can result in local system resonances, which, in turn, can lead to excessive currents and possible subsequent damage to the capacitors.
5. Malfunction of utility Meters: May record measurements incorrectly, result in higher billings to consumers.
6. Failure of sophisticated electronic equipments: Failure of sophisticated electronic equipments such as computers, remote monitoring systems, air conditioning systems and premature failure of switched-mode power supplies (SMPS) and uninterrupted power supplies (UPSs).
7. Flickering of lights: Due to the operation of arcing devices such as arc furnaces, arc welders, and discharge type lightning with magnetic ballasts, flickering of light may take place.

1.3.2 Harmonic Standards

There are various organizations on national and international levels working closely with engineers, equipment manufactures, and research organizations to come up with standards governing guide lines, recommended practices, and harmonic limits. The primary objective of the standards is to provide a common ground for all involved parties to work together to ensure compatibility between the end-user equipments and the system equipments. The most commonly used harmonic standards are IEEE–519–1992[11], International Electrotechnical Commission standard IEC–61000[12], South African standard NRS–048, and European standard EN–50160.

IEEE–519–1992 standard limits the amount of current harmonics injected by a user at the Point of Common Coupling (PCC). For example, the IEEE–519–1992 standard recommends a limit of 5% Total Harmonic Distortion (THD) in the current at the PCC in a weak system. The THD in the current is the ratio of the rms value of its distortion components to the rms value of its fundamental-frequency component. It is given as,

$$\%THD = \frac{\sqrt{\left(\sum_{h=2}^{\infty} I_h^2\right)}}{I_1} \times 100\% \qquad (1.4)$$

Where, l_h = rms value of the current at harmonic order h, and I_1 = rms value of the fundamental-frequency current component.

1.4 Solutions to Power Quality Problem in Distribution System

Poor quality power affects electricity customers in many ways. The lack of quality power can cause loss of production, damage of equipment or appliances or can even be detrimental to

human health. Therefore, it is very important to maintain high standard of power quality. Utilities and researchers all over the world have for decades worked on the improvement of power quality. There are sets of conventional solutions to the power quality problems, which have existed for a long time. However these conventional solutions use passive elements and do not always respond correctly as power system conditions change. The ever increased power capabilities, ease of control, and reduced costs of modern semiconductor devices have made power electronic converters affordable for many applications. New flexible solutions to many power quality problems have become possible with the help of these power electronic converters.

1.4.1 Reactive Power Compensators

Reactive power compensators or VAR compensators are used to control and/or regulate the terminal voltage in transmission/distribution system and to provide power factor correction[7], [13]. Two types of compensation problems are normally encountered in practical applications. The first is the load compensation where the requirements are usually to reduce or cancel the reactive power demand of large, and fluctuating industrial loads, such as electric arc furnaces, rolling mills, phase-controlled rectifiers. The second type of compensation is related to the voltage support of transmission/distribution lines.

In general, var compensators are classified depending on the technology used in their implementation[14]. They are broadly classified as rotating and static var compensators. The first one uses electro-mechanical power device like synchronous machine[6] and the later one uses power electronic technologies to accomplish the task. Again, there are two approaches for the realization of power electronics based var compensators[15], the one that employs thyristor-switched capacitors and reactors with tap-changing transformers, and the other approach uses static inverter circuits. A brief description of the most commonly used shunt compensators are presented below.

1.4.1.1 Thyristor Controlled Static Var Compensators (SVC)

Advances in high power semiconductor and sophisticated electronic control technologies have made the development of thyristor-controlled static var compensators (SVCs) possible. These compensators were originally developed[16] for arc furnace compensation in the early 1970s, and a few years later they were adopted for transmission and distribution systems[17]. SVC is essentially a variable impedance type var compensator. Two basic schemes of SVC are available in the literature. The first one controls the leading vars by synchronously switching capacitor banks to the lines; the second one achieves the control of lagging vars with a thyristor-controlled

variable inductor. They are named as, thyristor switched capacitors (TSC) and thyristor controlled reactors (TCR), respectively.

(a) Thyristor Switched Capacitors (TSC)

The basic idea of thyristor switched shunt capacitors is to split up a capacitor bank into appropriate number of capacitor steps and switch these steps on and off individually using anti-parallel thyristors as switching elements. Figure 1.4(a) shows the basic scheme.

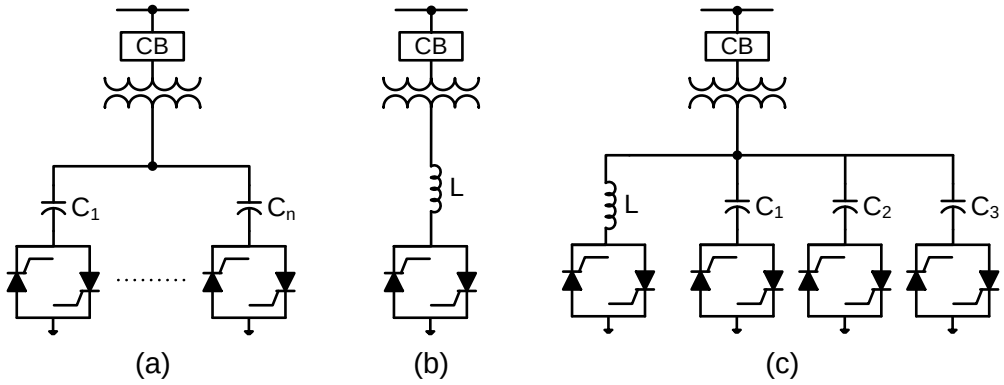


Figure 1.4 Static var compensators: (a) Thyristor-switched shunt capacitors; (2) Thyristor controlled shunt reactor; (c) Combination of both.

The TSC is characterized by:

- Stepwise control.
- Average one half-cycle (max one-cycle) delay for executing a command from the regulator.
- Practically no transients.
- No generation of harmonics.

(b) Thyristor Controlled Reactors (TCR)

An elementary single-phase thyristor controlled reactor (TCR) is shown in Figure 1.4(b). It consists of a fixed reactor (usually air-core) of inductance *L*, and a bidirectional thyristor switches. The basic idea of TCR is to control the fundamental frequency current component through the reactor by delaying the switching 'ON' instant of the thyristor switch with respect to the voltage across the TCR. The TCR is characterized by:

- Continuous control.
- Maximum one half-cycle delay for executing a command from the regulator.

- Generation of harmonics.

For many applications, a thyristor controlled shunt reactive power control device built up with a large steps of TSCs and one or two TCRs is quite attractive. Figure 1.4(c) combines the favourable properties of the two thyristor schemes discussed above. It provides continuously variable reactive power output from full lagging range to full leading range with good response and reduced harmonic generation.

Despite the simplicity of the thyristor switched static var compensator schemes, its popularity has been hindered by a number of practical disadvantages:

- The var compensation is not continuous in all cases.
- Each capacitor bank requires a separate thyristor switch and therefore it is not economical for high-voltage applications unless a step-down transformer is used.
- The steady-state voltage across the non-conducting thyristor switch is twice that of the peak supply voltage.
- The thyristor switch must be rated for, or protected by external means, against line voltage transients and fault currents.
- It occupies large footprint, high initial and maintenance cost.

1.4.1.2 VAR Generators Employing Static Inverters

The possibility of generating controllable reactive power directly, without use of large banks of capacitors and bulky inductors, by various switching power inverters was presented first in 1976. These approaches employ various dc-to-ac or ac-to-ac converter circuits. Among these, approaches employing dc-to-ac converter are more popular and are discussed here.

The dc-to-ac converters can be operated as a controllable voltage or current source and produce reactive power essentially without any reactive energy storage elements by circulating the current among the phases of the ac system. Functionally, from the viewpoint of reactive power generation, their operation is similar to that of an ideal synchronous machine. Similar to the synchronous machine, they can also exchange real power with the ac system if supplied from an appropriate energy source. Because of these similarities with synchronous machine, they are termed as Static Synchronous Generator (SSG) or more popularly Static Synchronous Compensator (STATCOM) and these come under the family of shunt connected second generation Flexible AC Transmission System (FACTS) device.

In the beginning, inverters were realized with force commutated thyristor switches, but with the remarkable progress of gate commutated semiconductor devices, attention has been focused on

self-commutated inverters. These self-commutated inverters can be broadly categorised[4] into two classes, namely, voltage source inverters (VSI) and current source inverters (CSI). The voltage-source approach shown in Figure 1.5(a) uses a capacitor with a regulated dc voltage, while the CSI, displayed in Figure 1.5(b) uses a reactor supplied with a regulated dc current.

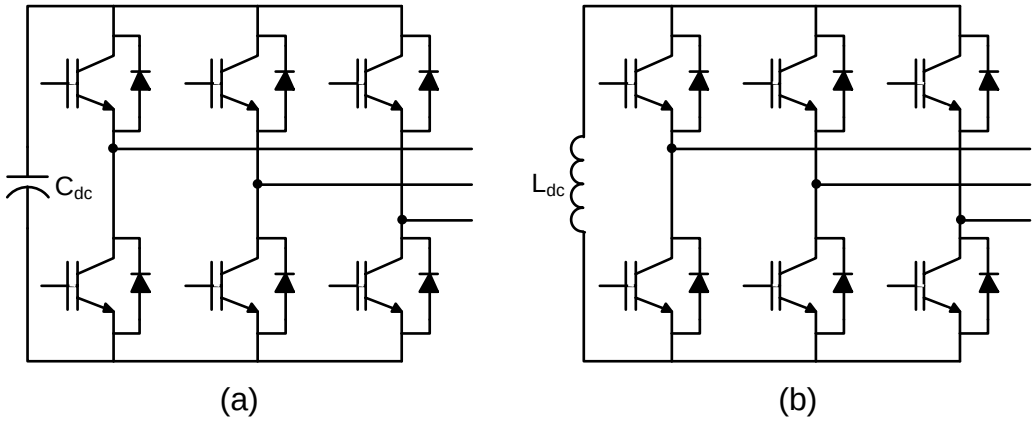


Figure 1.5 Topologies of inverters (a) Voltage source inverter; (b) Current source inverter.

Figure 1.6 shows the basic configuration of a VSI based STATCOM for reactive power compensation. It consists of a VSI connected in shunt to the ac system through coupling reactors (L_c). For the present discussion it is assumed that the VSI output voltages are sinusoidal, although the basic operating principles remain valid for any wave shape produced by a practical inverter. For purely reactive power flow, the inverter output voltages V_{oa}, V_{ob}, and V_{oc} are in phase with the ac system voltages V_a, V_b and V_c respectively. By controlling the amplitude (V_o) of the inverter output voltages, the reactive power can be controlled from full leading to full lagging. By Increasing V_o above the amplitude V of the system voltages, draws leading (capacitive) current from the ac system. On the other hand, decreasing V_o below V results in lagging (inductive) current drawn from the ac system.

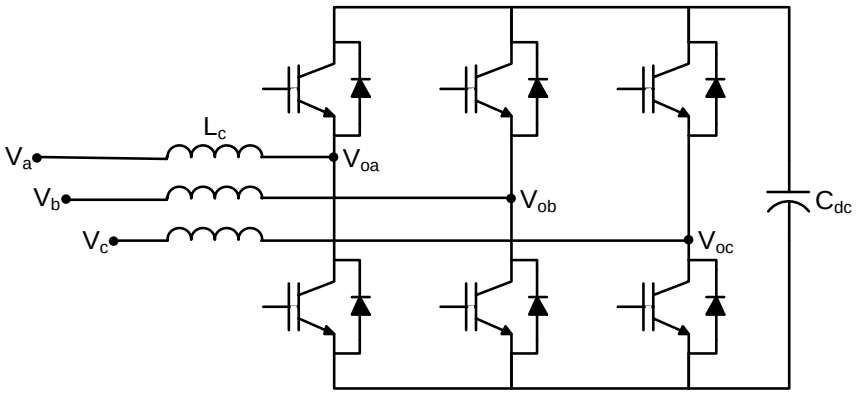


Figure 1.6 Schematic diagram of a VSI based STATCOM.

When the inverter is operated strictly as a reactive power source, as described above, it absorbs no real power from the ac system and thus its losses have to be replenished from a separate dc supply. However, the dc supply can be dispensed with if a suitable dc capacitor is used and inverter output voltage of each phase is made to lag the corresponding ac system phase voltage by a little amount. Under this condition, a real component of current will flow from the ac system to the inverter to replenish its losses.

A typical *V–I* characteristics of STATCOM are shown in Figure 1.7. It is observed from figure that the STATCOM can provide both capacitive and inductive compensation and is able to control its output current in the range spanning from maximum capacitive rating to maximum inductive rating practically independent of the ac system voltage[5]. Figure 1.7 also illustrates that the STATCOM has an increased transient rating in both the inductive and capacitive operating regions[18], [19]. The maximum attainable transient current in the capacitive region is determined by the maximum current turn-off capability of the inverter switches. In the inductive region, the inverter switches are naturally commuted and therefore the transient current rating is limited by the maximum allowable junction temperature of the inverter switches.

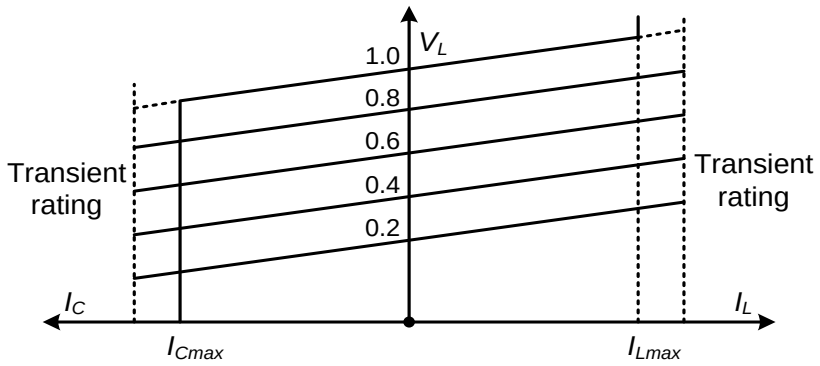


Figure 1.7 V–I characteristics of a STATCOM.

The commercial success of STATCOM is due to acceptable cost, coupled with desirable technical features such as extremely fast response time, flexibility of control, and continuous operation with virtually no maintenance. The principal advantages of STATCOM are the significant reduction in size, and the potential reduction in cost achieved from the elimination of a large number of passive components. Because of its smaller size, a STATCOM is well suited for applications where space is a premium. STATCOMs are also used to stabilize transmission systems[20], improve voltage regulation and compensation of poor power factor.

The benefits and drawbacks of the studied topologies are summarized in Table 1.2. The significant advantages of self-commutated device based compensators make them an interesting alternative to improve both compensation characteristics and the performance of ac power system.

Table 1-1: Comparison of basic types of shunt var compensators.

Aspect	Synchronous Condenser	SVC		STATCOM
		TCR (with Shunt Capacitors if Necessary)	TSC (with TCR if necessary)	
Accuracy of Compensation	Good	Very Good	Good, very good with TCR	Excellent
Control Flexibility	Good	Very Good	Good, very good with TCR	Excellent
Reactive Power Capability	Leading/ Lagging	Lagging/Leading	Leading/Lagging Indirect	Leading/ Lagging
Control	Continuous	Continuous	Discontinuous (Continuous with TCR)	Continuous
Response time	Slow	Fast, 0.5 to 2 cycles	Fast, 0.5 to 2 cycles	Very fast
Harmonics	Very Good	Very high (filters are needed)	Good (filters are needed with TCR)	Good
Losses	Moderate	Good (less) but increase in lagging mode	Good (less) but increases in leading mode	Very good (least) but increases with switching frequency
Phase Balancing Ability	Limited	Good	Limited	Very good
Cost	High	Moderate	Moderate	Low to moderate

1.4.2 Harmonic Compensation

To deal with harmonics, there are three basic choices: (a) to reinforce the distribution system to withstand the harmonics by derating the transformers and oversizing the conductors, (b) to incorporate current waveshaping circuits within the equipment so that they draw sinusoidal currents[21], and (c) to install devices to attenuate or remove the harmonics.

The first two choices are not cost-effective solutions and the only option is to incorporate filters to remove the harmonics. For reducing the harmonics, passive and/or active filters are used. These filters are either used separately or used in a combined fashion to form a hybrid filter.

1.4.2.1 Passive Power Filters

Passive filters can be connected either in parallel with the load (shunt passive filter) or in series with load (series passive filter). Shunt passive filters have traditionally been used to absorb current harmonics in power systems. Shunt passive filters provide low-impedance paths to divert harmonics to ground and discourage the flow of harmonics into the power system[22]. There are several types of shunt passive filters: single-tuned, double-tuned, automatically tuned, damped, and band-pass filters. Among these shunt passive filter topologies, single-tuned, double-tuned and high-pass damped filters are most commonly used. The tuned filters are designed to exhibit low impedance at one or more harmonic frequencies, while the high-pass damped filters provide low impedance for a wide spectrum of harmonics. The single-phase circuits of single-tuned, double-tuned and second order high-pass damped shunt passive filters are shown in Figure 1.8.

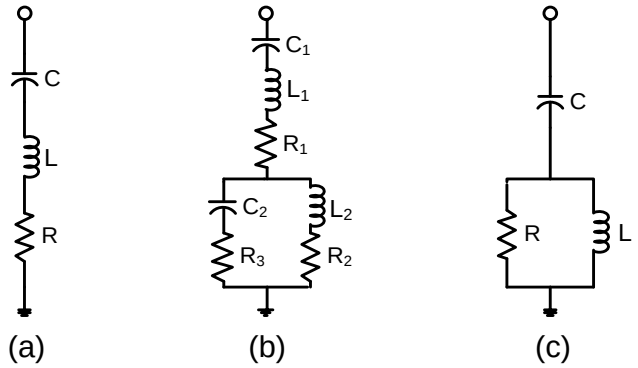


Figure 1.8 Shunt passive filters: (a) Single-tuned; (b) Double-tuned; (c) Second-order high-pass damped.

Passive filters have hitherto been used in power system because of their advantages which are:

1. Simple implementation, high efficiency and almost maintenance-free operation.
2. A single installation can serve many purposes, i.e., reactive power compensation, voltage support on critical buses, and reducing the impact and voltage drop due to the starting of a large motor.
3. Implementation in medium power level is possible.

However, passive filters have many problems to discourage their applications and are given below:

1. Passive filters are not suitable for changing system conditions. Once installed, neither the tuned frequency nor the size of the filter can be changed so easily.
2. The filters can either be switched “on” or “off.” Thus, a stepless control of reactive power with enhancement or reduction of load demand is not possible.

3. The source impedance, which is not accurately known and varies with the system configuration, strongly influences the filtering characteristics.
4. The change in the system operating conditions, addition of new compensating devices, aging, deterioration, and temperature effects may increase the designed tolerances thereby causing detuning of the filter.
5. The parallel resonance between the system and the filter may cause an amplification of the current at characteristic and noncharacteristic harmonics.
6. Single-tuned or double-tuned filters are not possible to employ for certain loads like cycloconverters or when the power system has interharmonics.
7. Outage of a parallel branch can totally alter the resonant frequency, resulting in overstressing of the filter components and increased harmonic distortion.

The design complexity and high cost of losses of the conventional passive filters, as well as their restricted capability to eliminate inter-harmonics and non-characteristic harmonics has encouraged the development of harmonic compensation technique by means of power electronic devices, commonly referred to as active power filters (APF).

1.4.2.2 Active Power Filters

In the last two decades, considerable progress has been made in active power filters (APFs). Similar to the STATCOM, APFs are inverter circuits, comprising of active devices i.e. semiconductor switches that can be controlled such that the APF can be made to act as harmonic current or voltage generators. Different topologies[22][4] of APFs have been proposed including shunt, series, and combination of these two. However, only the shunt APFs are considered in the present work.

The shunt active power filter acts as a current source and compensates load current harmonics by injecting equal-but opposite harmonic compensating current at the PCC. Figure 1.9 shows the connection of a shunt active power filter.

The main advantages of APFs are:

1. APFs are superior to passive filters in terms of filtering characteristics.
2. A single installation can serve many purposes, i.e. reactive power compensation, flicker mitigation, and imbalance compensation.
3. They are compact in size.
4. Non-susceptibility to resonance problem.
5. Step-less control characteristics.

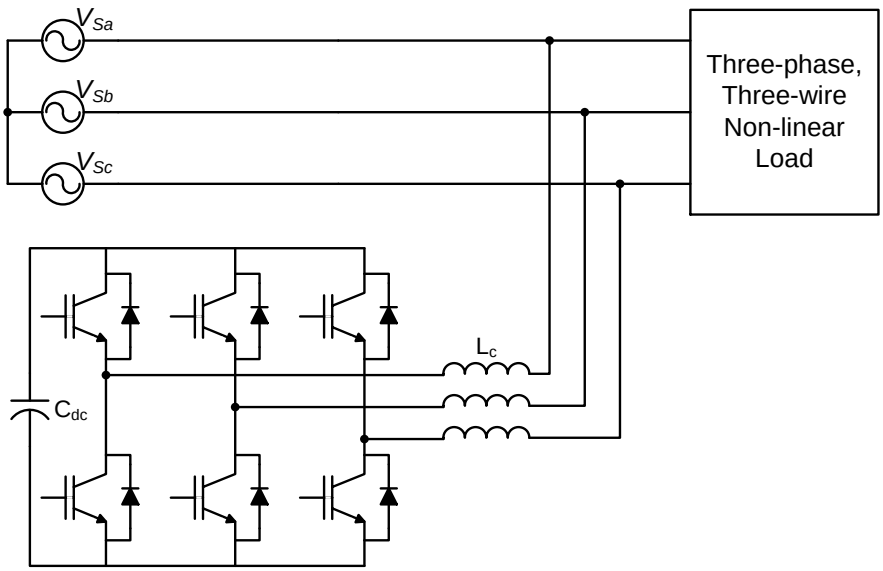


Figure 1.9 A voltage source inverter based shunt active power filter.

However, high initial cost of active power filters has discouraged their applications in high power systems. To overcome this, the hybrid power filters have been proposed and installed in recent years[23].

1.4.2.3 Hybrid Power Filters

Hybrid power filters are the combinations of passive and active power filters. Several combinations are possible and a typical combination of shunt passive and shunt active filter topology[4] is shown in Figure 1.10. Hybrid power filters[24] improve the compensation characteristics of passive filters, and allow the use of relatively low rating active power filters in high-power applications at a relatively low cost. Moreover, compensation characteristics of already installed passive filters can be significantly improved by retrofitting an active power filter at its terminals, giving more flexibility to the compensation scheme.

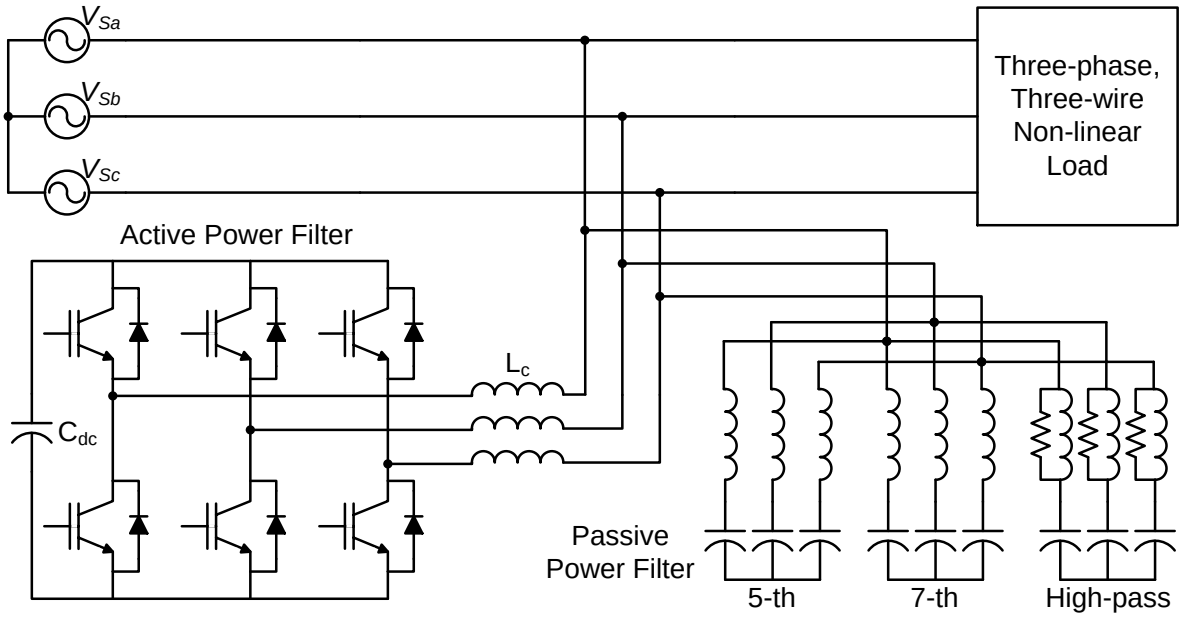


Figure 1.10 A hybrid power filter.

1.5 Power Quality Improvement using D-STATCOM

The conventional power quality mitigation equipment is proving to be inadequate for an increasing number of applications, and this fact has attracted the attention of power engineers to develop dynamic and adjustable solutions to power quality problems. One modern and very promising group of solutions that deals with load current and/or supply voltage imperfections are Custom Power Devices (CPDs). Custom power devices solve most of the distribution system problems and can be replaced by the existing compensation devices because of its versatile functionalities thereby reducing the cost. Custom Power is a concept based on the application of power electronic controllers in the distribution system to supply value-added, reliable and high quality power to its customers. Custom power solutions can be categorized as network reconfiguring type or compensating type[25]. The network reconfiguring devices are usually called switchgear and they perform current limiting, circuit breaking and current transferring operations. Network reconfiguring types of custom power devices are Static Current Limiter, Static Circuit Breaker and Static Transfer Switch. The compensating type devices improve the quality of supplied voltage and/or current. The compensating types of custom power devices include the D-STATCOM (Distribution Static Synchronous Compensator), DVR (Dynamic Voltage Restorer)[26] and UPQC (Unified Power Quality Conditioner)[27], which are used for compensating the power quality problems in current waveform or voltage waveform or both[28].

The D-STATCOM is a shunt-connected device, which takes care of the power quality problems in the current waveform. The commercial success of D-STATCOM is due to its acceptable cost, coupled with desirable technical features such as extremely fast response time, flexibility of control, continuous operation with virtually no maintenance[29]. The present work exploits this fact and concerned with the development of a robust computer-controlled D-STATCOM for power quality improvement in single phase and 3P3W distribution systems. For completeness and better understanding of the thesis, the compensation principle, topologies and control of D-STATCOM are briefly discussed below.

1.6 Distribution Static Synchronous Compensator (D-STATCOM)

The STATCOM is a vital solution to maintain grid voltages by supplying or consuming reactive power. It has been installed in the transmission grids, and its use is spreading to the medium-voltage distribution grids as a distribution STATCOM (D-STATCOM).

1.6.1 STATCOM in Transmission and Distribution Systems

STATCOMs in both transmission systems and distribution systems have the same structure, but their objectives are different. Some of the primary objectives of a STATCOM in a transmission system are as follows:

- Improvement of transient stability margin by increasing the maximum transmittable power in the transmission line.
- Midpoint voltage regulation for a line segment in order to increase the transmittable power in the transmission system.
- Voltage support at the end of a line requires the compensation of load having poor power factor. This increases the maximum power transmission capability of the transmission line while improving the voltage instability limits.
- Power oscillation damping so that oscillations in the machine angle due to any minor disturbance can be damped out rapidly.

On the other hand, the objectives of these shunt compensators in a distribution system are as given below.

- Compensation of poor load power factor such that the current drawn from the source has a unity power factor.
- Suppression of harmonics in loads so that the current drawn from source is sinusoidal.
- Voltage regulation for the loads that cause fluctuations in the supply voltage.

- Cancellation of the effect of unbalance loads so that the current drawn from the source is balanced.

All of these objectives are not necessarily met by a typical STATCOM. The required STATCOM should be designed in view of the needs of compensation parameters.

1.6.2 Basic Compensation Principle of D-STATCOM

D-STATCOM consists of two distinct main blocks.

1. The inverter (power circuit)
2. The D-STATCOM controller

The inverter is responsible for synthesizing the compensating current that should be drawn from the power supply. The D-STATCOM controller is responsible for signal processing in order to determine the compensating currents, which are continuously passed to the inverter. Figure 1.11 shows the connection of D-STATCOM for reactive and harmonic current compensation in 3P3W distribution system. A voltage source inverter with necessary passive components is used as a D-STATCOM and is connected in parallel at the point-of-common coupling (PCC).

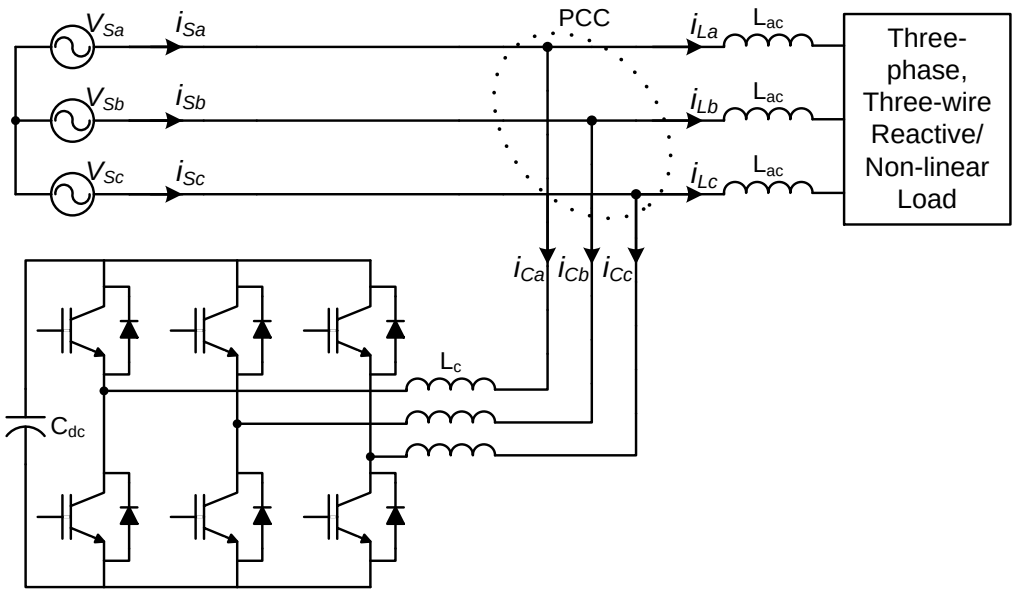


Figure 1.11 A D-STATCOM connected to the 3P3W distribution system for harmonic elimination and reactive power compensation.

To illustrate compensation principle[4], Figure 1.12 depicts voltage and current waveforms of the ac power source v_{Sa}, the source current i_{Sa}, the load current i_{La}, and the D-STATCOM current i_{Ca} respectively in the *a*-phase, under the following assumptions: (1) the smoothening reactor L_{dc} in the dc side of the phase-controlled rectifier is large enough to make the dc current constant,

(2) the D-STATCOM operates as an ideal controllable current source, and (3) the ac inductor L_{ac} is equal to zero.

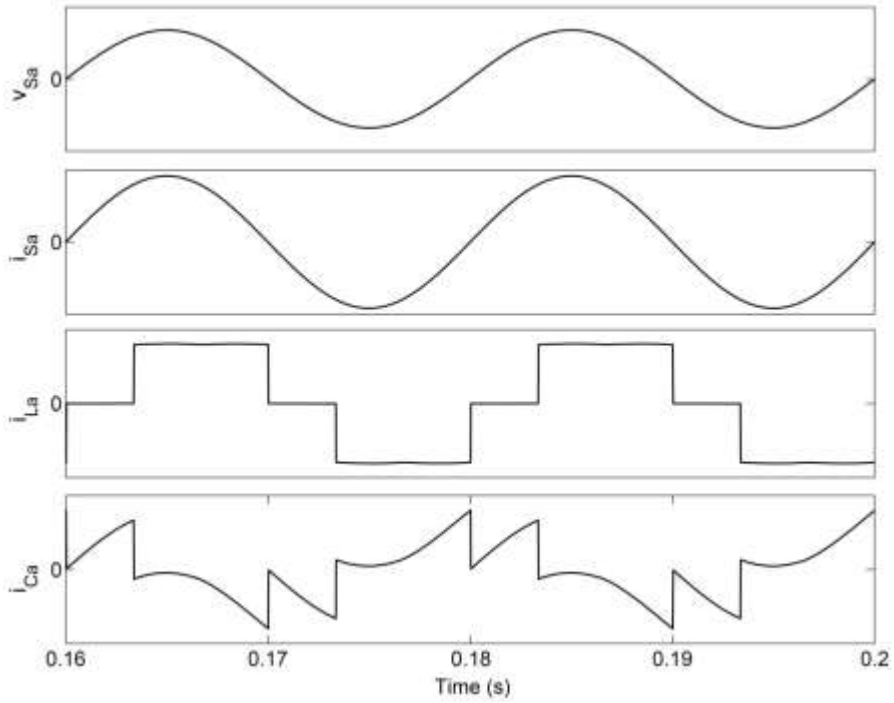


Figure 1.12 Basic compensation principle of D-STATCOM: phase-a waveforms of source voltage, source current after compensation, load current and D-STATCOM current.

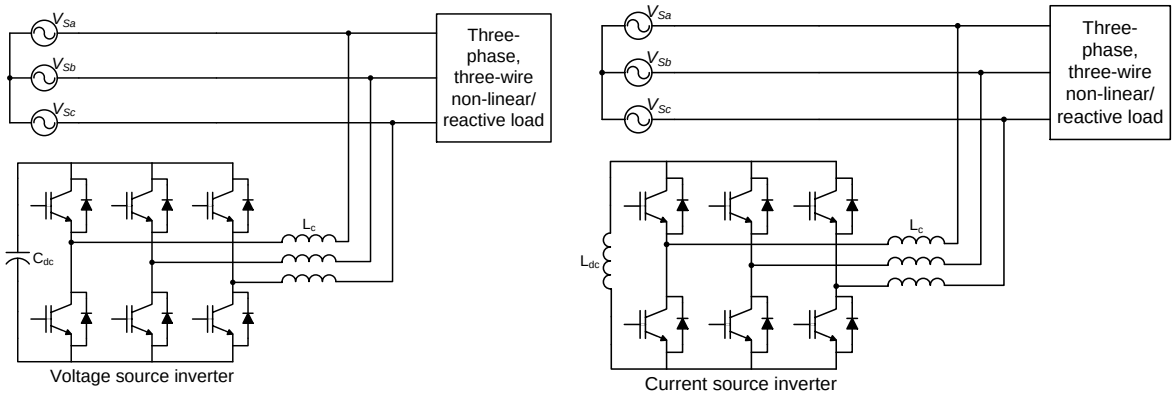
The D-STATCOM is controlled to draw the compensating current i_{Ca} from the ac power source, such that it cancels the reactive and harmonic current contained in the load current i_{La}. After compensation with D-STATCOM the source current (i_{Sa}) is sinusoidal and in phase with its respective source voltage waveform (v_{Sa}).

1.7 Configurations of D-STATCOM

D-STATCOM's can be broadly classified based on its power circuit topology and the type of the supply and they are discussed below:

1.7.1 Power Circuit Based Classification

Similar to the STATCOM, the power circuit of D-STATCOM can also be made either with voltage source inverters (VSI) or current source inverters (CSI)[30]–[32]. The VSI approach shown in Figure 1.13(a) uses a capacitor with a regulated dc voltage, while the CSI, displayed in Figure 1.13(b) uses a reactor supplied with a regulated dc current.



(a) (b)

Figure 1.13 (a) Voltage source inverter based D-STATCOM; (b) Current source inverter based D-STATCOM.

However, these simple topologies are not suitable for high-power, medium-voltage applications because of their high harmonic content and increased cost. For high-power, medium-voltage applications, the CSI based D-STATCOMs can be realised using pulsewidth modulated current source inverters (PWM-CSIs) or load commutated inverters (LCIs). On the other hand, VSI for high-power, medium-voltage applications can be broadly categorized into two groups: multipulse and multilevel type inverters. These inverters present great advantages compared with conventional and very well-known two-level VSI. These advantages are fundamentally focused on improvements in the output signal quality and a nominal power increase in the inverter.

In multipulse inverters, several six-pulse inverter units can be arranged using transformers as magnetic interfaces, which is a useful technique to achieve high power rating and perform harmonic neutralization. The higher the number of six-pulse units, the lower the distortion of the resultant output voltage.

Multilevel inverters have become increasingly popular in recent years. It uses the concept of utilizing multiple small voltage levels to perform power conversion. Advantages of this approach include good power quality, good electromagnetic compatibility (EMC), low switching losses, and high voltage capability. They synthesize an output voltage waveform from several levels of capacitor voltage sources. As the number of levels increases, the synthesized output waveform approaches the sinusoidal wave with the reduced harmonic distortion. At present, there are three benchmark multilevel inverter topologies are reported in literature. They are:

1. Diode Clamped Multilevel Inverter (DCMLI)
2. Flying Capacitor Multilevel Inverter (FCMLI)

3. Cascade multilevel Inverters (CMLI)

These three multilevel inverter topologies could be considered now as the classic or traditional multilevel topologies that first made it into real industrial products during the last two decades.

1.7.2 Supply System Based Classification

The classification of D-STATCOM can also be based on the supply and/or the load system having single-phase, three-phase three-wire (3P3W) or three-phase four-wire (3P4W) systems.

1.7.2.1 Single-phase D-STATCOMs

The single-phase[22] (two-wire) D-STATCOMs are used for compensation of harmonics and reactive power generated by the operation of nonlinear loads, such as domestic appliances, connected to single-phase supply systems. Figure 1.14 shows the connection of D-STATCOM for reactive and harmonic current compensation in single-phase applications.

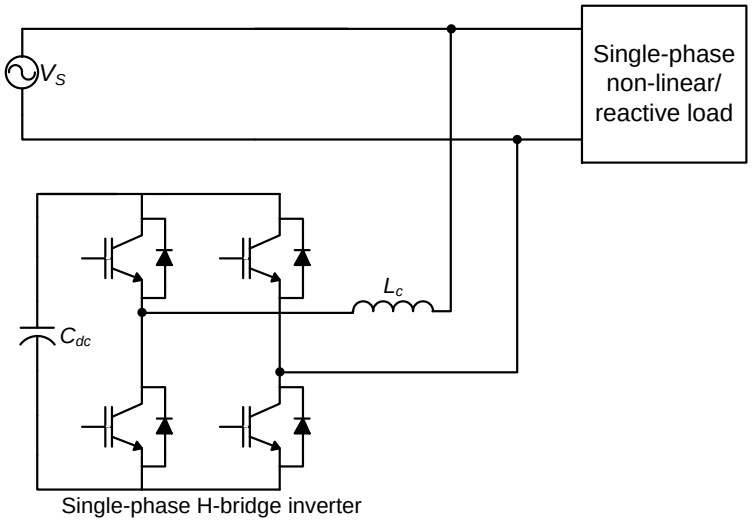


Figure 1.14 D-STATCOM for two-wire systems.

1.7.2.2 Three-phase, Three-wire D-STATCOMs

In three-phase, three-wire (3P3W) distribution systems, the neutral wire is absent and these systems are used to provide supply for high-power loads such as adjustable speed drives, transactions, arc furnaces, and other industrial applications. For compensation of harmonics and reactive power in these systems, a 3P3W D-STATCOM is used. Figure 1.11 shows the connection of D-STATCOM for reactive and harmonic current compensation in 3P3W distribution system.

1.7.2.3 Three-phase, Four-wire D-STATCOMs

D-STATCOMs are specially designed to 3P4W systems for compensating neutral current along with the necessary compensation features of the 3P3W D-STATCOMs. Three different topologies are available for 3P4W systems and are given below[33]:

1. Three H-bridge D-STATCOM topology
2. 3P4W capacitor mid-point (or split-capacitor) D-STATCOM topology
3. 3P4W four-leg D-STATCOM topology

1. Three H-bridge D-STATCOM Topology

Figure 1.15 shows the three H-bridge D-STATCOM topology. It consists of three single-phase full-bridges (H-bridge) with a common dc bus. These H-bridge inverters are connected to the 3P4W system by using three single-phase isolation transformers. Considering the structural advantage of this topology, the control can be done either as a three-phase unit or three separate single-phase units. An independent phase control approach based on single-phase instantaneous reactive power theory is presented in[34].

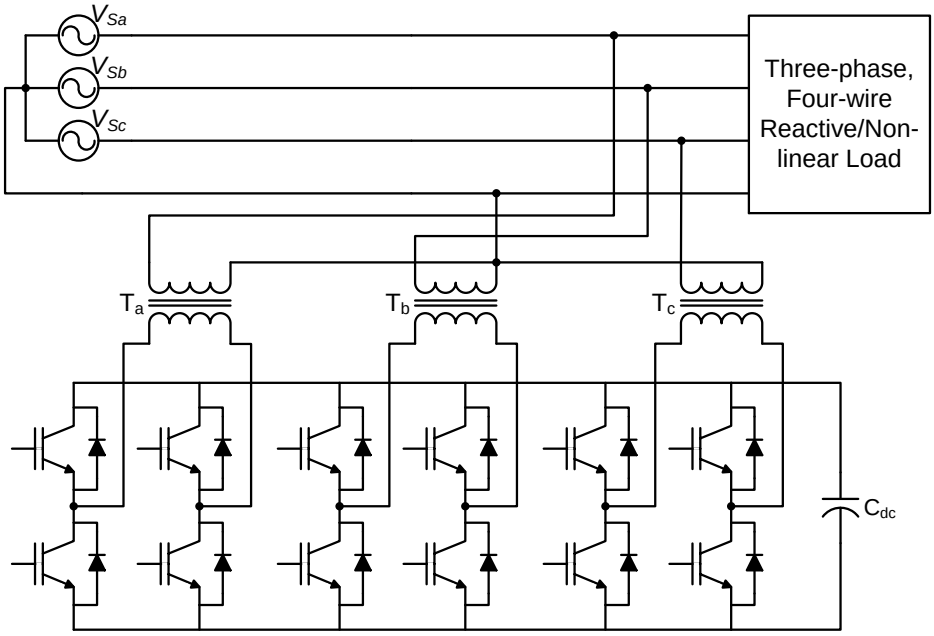


Figure 1.15 The three H-bridge D-STATCOM topology.

In this topology the maximum voltage that appears across each H-bridge is the single-phase voltage and not the three-phase line-to-line voltage, as in the case of split capacitor or four-leg topology. This result into a reduction of dc bus voltage by a factor of $\sqrt{3}$ and thus the reference dc bus voltage needed for proper operation of shunt D-STATCOM also reduces by a maximum

factor of $\sqrt{3}$. This, in turn, reduces the rating of inverter. But, the main disadvantage of this topology is the increased number of switching devices.

2. Three-phase, Four-wire Capacitor Mid-point D-STATCOM Topology

The capacitor mid-point D-STATCOM topology utilizes the standard three-phase conventional inverter where the dc capacitor is split and the neutral wire is directly connected to the electrical midpoint of the capacitors through an optional inductance. Figure 1.16 shows the capacitor mid-point D-STATCOM topology used in 3P4W system. The split capacitors allow load neutral current to flow through one of the dc capacitors $C_{dc1,}$ C_{dc2} and return to the ac neural wire.

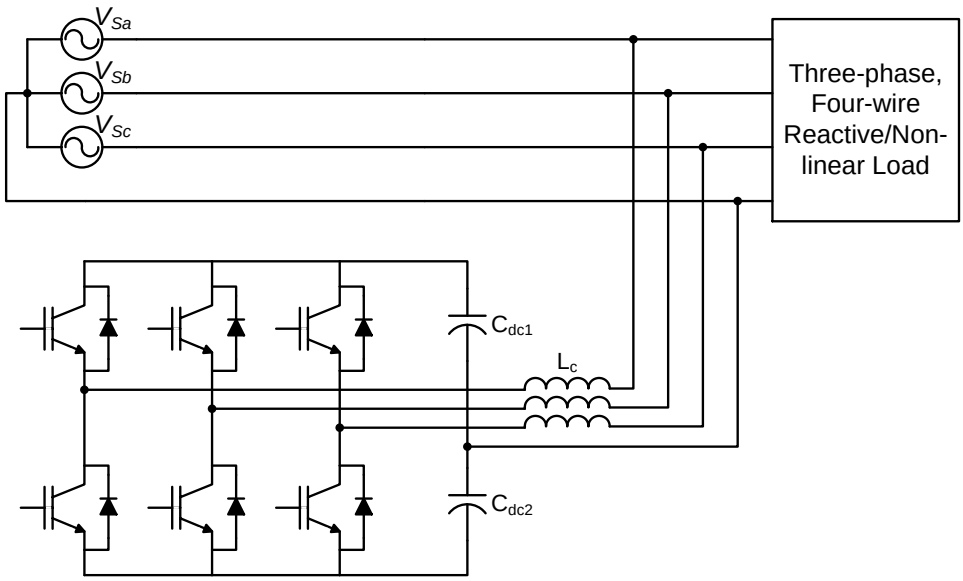


Figure 1.16 The three H-bridge D-STATCOM topology.

3. Three-phase, Four-wire Four-leg D-STATCOM Topology

Figure 1.17 shows the four-leg D-STATCOM topology used in 3P4W systems. In this topology, three of the switch legs are connected to the three phase conductors through a series inductance while the fourth switch leg is connected to the neutral conductor with an optional inductor[33]. This topology is most suitable for compensation of high neutral currents. Despite having higher number of switching devices this topology, outweighed the split capacitor topology by number of factors:

Better controllability: In this topology only one dc-bus voltage needs to be regulated, as opposed to two in the capacitor midpoint topology. This significantly simplifies the control circuitry with better controllability.

Lower dc voltage and current requirement: This topology requires a lower dc-bus voltage and capacitor current.

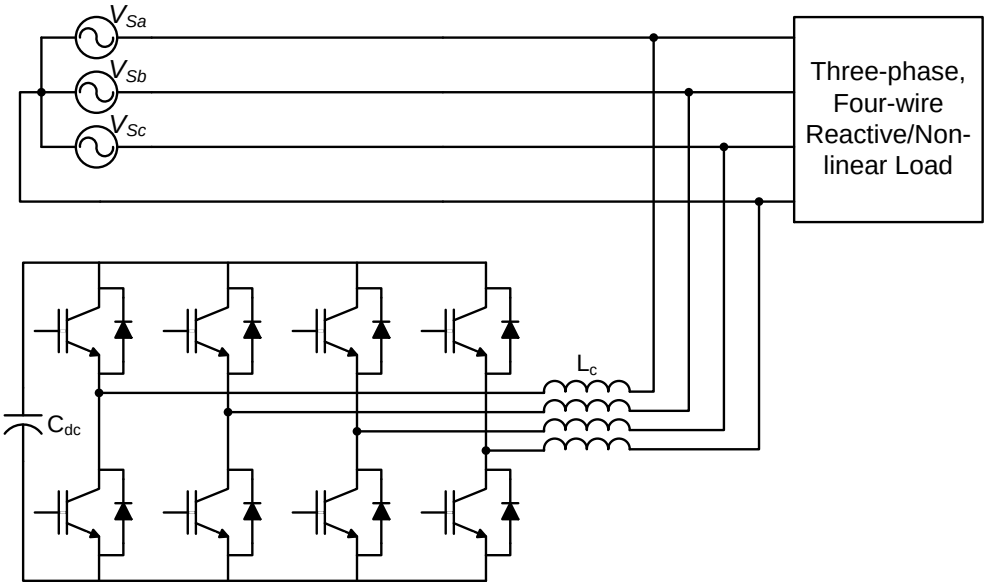


Figure 1.17 The 3P4W four-leg topology.

1.8 D-STATCOM Controller

The effectiveness of the D-STATCOM depends basically on the design characteristics of the controller.

Control strategy of the D-STATCOM is implemented in three stages and they are:

1. In the first stage, the essential voltage and current signals are sensed using potential transformers (PT's), current transformers (CT's), isolation amplifiers, and Hall-effect sensors to gather accurate system information.
2. In the second stage, compensating commands in terms of current or voltage levels are derived based on control methods and D-STATCOM configurations. Based on the operational requirements, type of application, system configuration and loss optimisation, this part of the control scheme calculates the current reference waveforms for each phase of the inverter by maintaining a constant dc bus voltage.
3. In the final stage of control, the controller forces the inverter to draw the desired compensating currents from the source. This part of the control scheme is responsible for generating the gating signals for the solid-state devices of the inverter of D-STATCOM using different current control techniques such as PWM, hysteresis, sliding-mode.

The combined controller of the D-STATCOMs is realized using analog and digital devices or advanced microelectronic devices, such as single-chip microcomputers, DSP's, and FPGA.

1.9 Scope of Work and Author's Contribution

Although the term "power quality" encompasses all disturbances encountered in a power system, it has been found that reactive power burden, harmonic currents, and unbalanced operation are the most dominant types of power quality problems in modern distribution systems. This thesis exploits this fact and evaluating the solutions based on custom power devices for improving the power quality of the distribution systems. In this thesis, an attempt has been made for improving power quality in single phase and in 3P3W with D-STATCOM.

The main contributions of the author can be summarized as follows:

- To begin with, a literature survey on available inverter topologies for the realisation of D-STATCOM is studied. Based on this study, single-star bridge cells (SSBC) based modular multilevel inverter has been selected as a power circuit for the D-STATCOM. The Pulse width modulation suitable for SSBC based D-STATCOM is investigated, the necessary components to make DC capacitor voltage balancing is identified.
- A 1.2-kV, 100-KVA CHB based transformerless PWM D-STATCOM has been designed for single phase system. This specific design approach does not require line frequency transformer and high power switching devices, and therefore the cost and size of the D-STATCOM are reduced. The DC capacitor voltage balancing methods are identified, one of the existing balancing technique auxiliary control calculation is improved. Extensive simulation study has been carried out to examine the control theories required to generate the reference currents for the D-STATCOM for harmonic elimination and reactive power compensation with different loads and at distorted voltage conditions is examined.
- A 2.2-kV, 1-MVA SSBC based transformerless PWM D-STATCOM has been designed for 3P3W distribution system. This specific design approach does not require line frequency transformer and high power switching devices, and therefore the cost and size of the D-STATCOM are reduced. Extensive simulation study has been carried out to examine the effectiveness of the D-STATCOM current controller's i.e, with PI and PI with resonant controller for harmonic elimination and reactive power compensation with different loads. The DC capacitor voltage balancing methods individual and cluster balancing is investigated for the D-STATCOM at the unbalanced current compensation.

- In order to further verify the simulation studies of the proposed schemes, a downscaled five-level SSBC based D-STATCOM rated at 100-V, 5-kVA has been designed, developed, and tested to verify the viability and effectiveness of single phase D-STATCOM capacitor voltage balancing methods and the current controller performance for 3P3W D-STATCOM. The effectiveness of D-STATCOM in unity power factor mode and zero voltage regulation mode along with DC capacitor voltage balancing is verified with the unbalanced linear load. By using real-time workshop (RTW) of MATLAB and real-time interface (RTI) feature of dSPACE, the real-time simulation of the SIMULINK models of the controllers of the D-STATCOM have been implemented. MOSFET has been selected as the switching device. The experimental results have been found to be in good agreement with the simulation results.

1.10 Organization of the Thesis

Apart from this chapter, the thesis contains six more chapters and the work included in each chapter is briefly outlined as follows:

CHAPTER 2 starts with an overview of different topologies of inverters used in high-power, medium-voltage systems. Among the available topologies, the SSBC based modular multilevel inverter for the power circuit of D-STATCOM has been addressed. The PWM control methods for the chosen inverter are discussed and problem of the unequal device conduction periods of LSPWM technique is addressed. The PSPWM carrier modulation is more suitable for D-STATTCOM application but for unbalanced currents the capacitor voltage balancing method is required.

The investigation of the performance of a 1.2-kV, 100-KVA single phase CHB based transformerless PWM D-STATCOM for power quality improvement has been given CHAPTER 3. In this chapter, the two capacitor voltage balancing methods are focused and the control theory's suitable for reference generator for single phase D-STATCOM is discussed. Further, simulation results are provided to verify the steady-state and dynamic performance of the compensator with different load and utility voltage conditions.

The investigation of the performance of an 2.2-kV, 1-MVA SSBC based transformerless PWM D-STATCOM for power quality improvement in 3P3W systems with PSPWM carrier has been given CHAPTER 4. In this chapter, a systematic design procedure, selection of passive components and generation of reference currents for D-STATCOM are given in detail. The two current controller methods are discussed and the cluster voltage balancing method for SSBC D-

STACOM is discussed. Further, simulation results are provided to verify the steady-state and dynamic performance of the compensator with different load and utility voltage conditions.

CHAPTER 5 is dedicated to the Voltage control mode of operation for single phase and three phase SSBC based D-STACOM. In this chapter the control strategy required to maintain the voltage at PCC is focused. Simulation results are provided to verify the steady-state and dynamic performance of the compensators with different utility voltage conditions.

The detailed discussions for the experimental set-ups have been given in CHAPTER 6. This includes the discussion on the power circuit, dSPACE based controllers, the measuring system and the generation of gating signals for the inverter. The chapter concludes with experimental results and the corresponding discussion.

The main conclusions of the presented work and possible future research have been summarised in this CHAPTER 7.

In the end of thesis, the list of references and publications are given

CHAPTER 2: PWM INVERTERS FOR D-STATCOM

[This chapter describes the available inverter topologies for realization of D-STATCOM and the selection of SSBC based modular multilevel inverter for the power circuit of D-STATCOM. The carrier based PWM techniques suitable for SSBC inverter is presented. The phase shifted pulse width modulation (PSPWM) is advantageous over level shifted pulse width modulation (LSPWM) in terms of uniform conduction period and switching frequency of each device in H-bridge.]

2.1 Introduction

High-performance and cost-effective inverter topology is a prerequisite for the realization of D-STATCOM. With the remarkable progress of gate commutated semiconductor devices, attention has been focused on self-commutated inverters capable of generating or absorbing reactive power without requiring large banks of capacitors or reactors. Depending on the dc-link energy-storage component, several approaches are possible including voltage source inverters (VSI) and current source inverters (CSI). The voltage-source approach shown in Figure 2.1(a) uses a capacitor with a regulated dc voltage, while the CSI, shown in Figure 2.1(b) uses a reactor supplied with a regulated dc current.

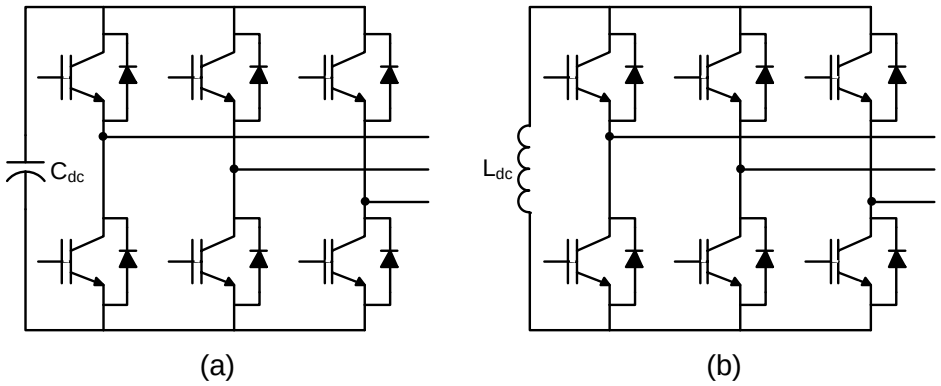


Figure 2.1 Topologies of inverters (a) Voltage source inverter (b) Current source inverter.

A critical comparison of the performance of VSI and CSI when used as the power converter of D-STATCOM is beyond the scope of this thesis. However, one may prefer CSI due to its robustness or the VSI due to its high efficiency, low initial cost, and smaller physical size[4]. Since VSI technology is widely used in industrial applications, this has also been more common in FACTS and Custom power device (CPD) applications and hence, VSI has been considered in this thesis.

2.2 Two-level VSI for High-power, Medium-voltage

The well-known two-level VSI is also used for medium- and high-power applications. To achieve the required voltage level of the converter, semi-conductor switches are connected in series. Thus, an inverter leg is comprised of two groups of active switches, each consisting of two or more switches in series, depending on the dc-link voltage[35], [36]. In addition to this, multiple capacitors in series could be necessary to achieve the desired voltage in dc link. The power circuit of the high-power two-level VSI is shown in Figure 2.2. In this circuit, each switch comprises of three semi-conductor devices connected in series and controlled by the same gating signal.

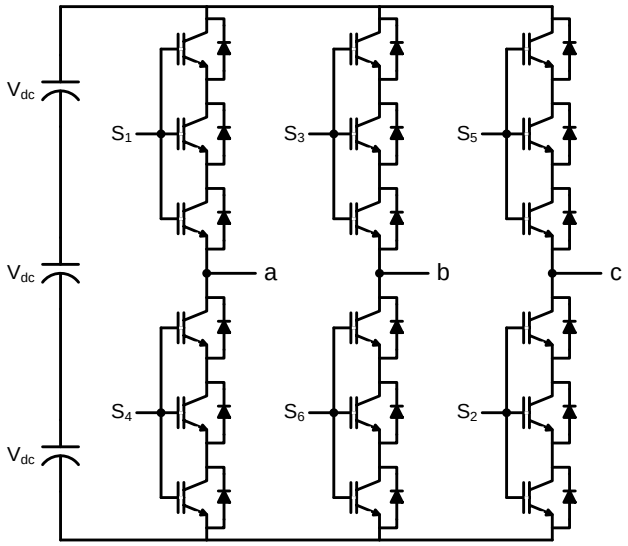


Figure 2.2 Two-level high-power VSI power circuit.

The high harmonic content of the output voltage and increased number of switching devices makes this simple inverter impractical for direct use in high-power applications. Instead of using filters to improve the voltage waveform of the basic two-level VSI, several topologies such as multipulse and multilevel inverters are proposed in the literature for high-power, medium-voltage applications using mature medium-power semiconductor devices.

2.3 VSI Topologies for High power, Medium voltage applications

The different VSI topologies for high-power, medium-voltage applications can be broadly categorized into two groups: multipulse and multilevel type inverters. These inverters have many advantages in comparison to conventional and very well-known two-level VSI. These

advantages are primarily reflected in improvements in the output power quality and increase in the power rating of the inverter.

2.3.1 Multipulse inverters

In multipulse inverters, several six-pulse inverter units are arranged as shown in Figure 2.3, using transformers as magnetic interfaces for achieving high power rating[37] and harmonic neutralization. The higher the number of six-pulse units, the lower is the distortion of the resultant output voltage[6]. For instance, eight six-pulse inverter units can be combined by means of a magnetic interfaces (such as zigzag transformers) to form an equivalent 48-pulse inverter. In this case, the lowest harmonic order is 47^{th} in the ac voltage and 48^{th} in the dc current. The amplitude of the harmonics decreases as the harmonic order increases. In general, combination of N_P six-pulse inverter units gives rise to a $6N_P$ pulse inverter. In this inverter, all harmonic orders except those at $6kN_P \pm 1$ are cancelled in the ac voltage (k is any integer). The corresponding phase difference between two successive inverter units is given by $360°/6N_P$. For transmission line applications, a pulse number of 24 or higher is required to achieve adequate waveform quality without passive filters.

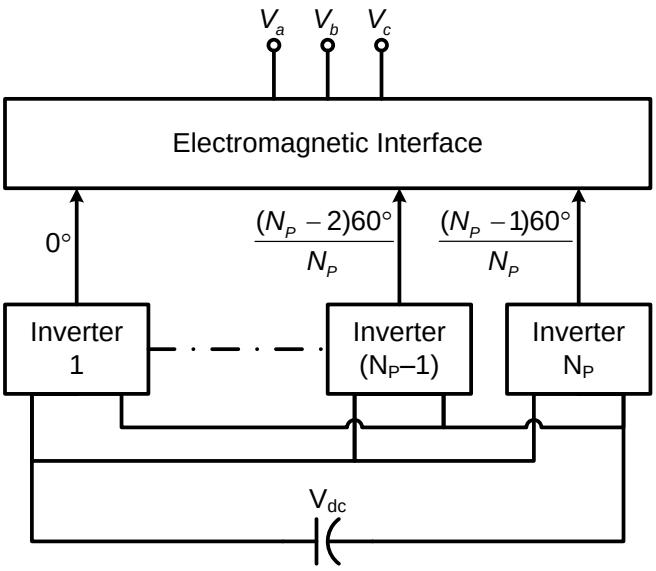


Figure 2.3 General structure of multipulse inverter.

The main advantage with the multipulse inverter is its low switching losses and reduced input-current harmonics[38]. These features are particularly useful in applications with high-voltage, high-power ratings. However, the complex phase shifting transformers have the following drawbacks:

(1) are the most expensive equipments in the overall inverter;

(2) produce about 50% of the total losses of the inverter;
(3) occupy up to 40% of the total real estate requirement of the inverter, which is an excessively large area;
(4) cause difficulties in control due to dc magnetizing and surge overvoltage problems resulting from saturation of the transformers in transient conditions;

To overcome these drawbacks of multipulse inverters, the multilevel inverter topologies have been proposed in the literature.

2.3.2 Multilevel inverters

Multilevel inverters have become increasingly popular in recent years. It uses the concept of aggregating multiple small voltage levels to perform power conversion at an appropriate high-voltage level. Advantages of this approach include good power quality, good electromagnetic compatibility (EMC), low switching losses, and high voltage capability[39]. The output voltage waveform is synthesized by aggregating several levels of capacitor voltages. As the number of levels increases, the synthesized output waveform approaches the sinusoidal wave with the reduced harmonic distortion. However, a large number of levels increase control complexity and introduce voltage imbalance problems. Multilevel inverters are considered today as a very attractive solution for high-power, medium-voltage applications, since they can:

(1) generate output voltages with mature medium-power semiconductor technology with lower distortion and dv/dt ;
(2) draw input current with very low distortion;
(3) generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated;
(4) can operate with a lower switching frequency;
(5) are fault tolerant, less prone to failure and their cost is relatively low;

Because of the above advantages, in the present work, multilevel inverter has been considered over multipulse inverter. The topologies and modulation methods of multilevel inverters are discussed in the next sections.

2.4 Multilevel inverter topologies

At present, there are three benchmark multilevel inverter topologies reported in the literature. They are:

1. Diode Clamped Multilevel Inverter (DCMLI)
2. Flying Capacitor Multilevel Inverter (FCMLI)
3. Cascade Multilevel Inverters (CMLI)

These three could be considered now as the classic or traditional multilevel topologies which were introduced into real industrial products during the last three decades. New multilevel inverter topologies have also been proposed in the literature and most of them are derived from these classical multilevel topologies. However, not so many have made their way to the industry yet. Operating principles, generation of multilevel voltage waveform, characteristics, modulation schemes, applications and other information related to the DCMLI, FCMLI and CMLI can be found from the previous works in [40]–[50]. A brief description of these topologies is given below:

2.4.1 Diode Clamped Multilevel inverter (DCMLI)

The diode clamped multilevel inverter (DCMLI) has been proposed in [51]and can be considered as the first real multilevel inverter. The DCMLI employs clamping diodes and cascaded dc capacitors to produce ac voltage waveforms with multiple levels. The inverter can be generally configured as a three, four, or five-level topology, but only the three-level inverter, often known as neutral-point clamped (NPC) inverter, has found wide application in high-power medium-voltage systems.

Figure 2.4 shows the simplified circuit diagram of a five-level DCMLI. In Figure 2.4, each phase-leg of the inverter is composed of eight active switches (with antiparallel diodes) from S_1 to S'_4. In practice, either IGBT or IGCT can be employed as a switching device. The upper and lower switches of each phase-leg are operated in a complementary manner and the complementary pairs are (S_1, S'_1), (S_2, S'_2), (S_3, S'_3), and (S_4, S'_4).

On the dc side of the inverter, the dc bus capacitor is split into four parts, and provides a neutral point *O*. The voltage across each of the dc capacitors is (V_{dc}), which is normally equal to one fourth of the total dc voltage ($4V_{dc}$). The diodes, connected to the dc bus capacitors are called 'clamping diodes', which will limit the voltage stress across each device to V_{dc}.

The DCMLI are most widely accepted topology in medium-voltage drives and are best suitable for back-to-back regenerative applications[52]. Particularly, three-level DCMLI based applications has become quite popular because of a simple transformer rectifier power circuit structure, with a lower device count and less number of capacitors. Although the DCMLI structure can be extended to higher number of levels, these are less attractive because of higher

losses and uneven distribution of losses in the outer and inner devices. In particular, the clamping diodes, which have to be connected in series to block the higher voltages, introduce more conduction losses and produce reverse recovery currents during commutation that affect the switching losses of the other devices even more[53]. Furthermore, balancing of dc-link capacitor voltage becomes unattainable in higher level topologies with applications such as D-STATCOM, APF and DVR.

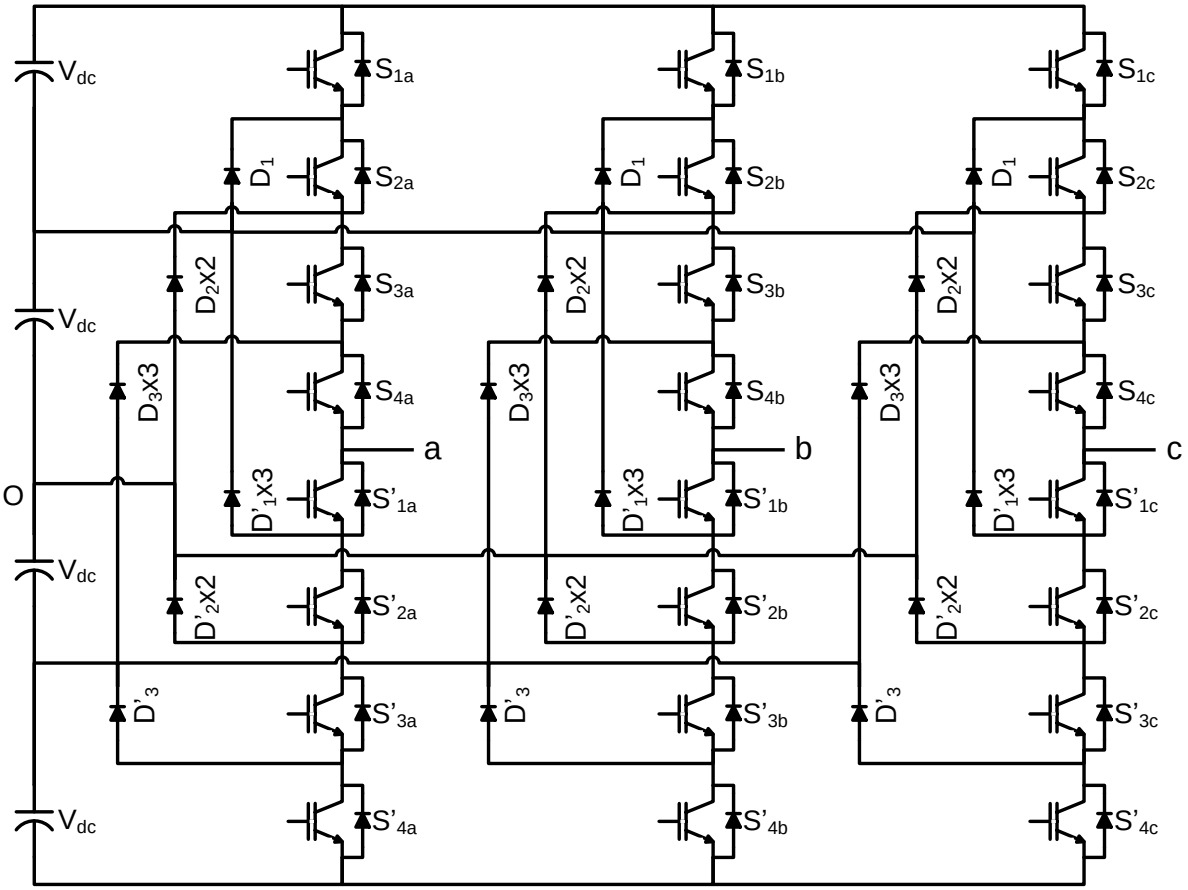


Figure 2.4 A three-phase five-level diode clamped multilevel inverter.

The drawbacks of the DCMLI are the unequal loss distribution and the resulting uneven temperature distribution. Since the semiconductors are cooled with separate heat sinks and cooling systems, it results in an uneven semiconductor-junction temperature distribution, which affects the cooling system design and limits the maximum power rating, output current, and switching frequency of the inverter. The unequal loss distribution can be substantially improved by replacing the neutral clamping diodes with clamping switches. With clamping switches, the current can be forced to go through the upper or lower clamping path. This can be used to control the power loss distribution and overcome the limitations of the DCMLI, enabling substantially higher power rating. These additional devices are called active neutral clamping switches, as shown in Figure 2.5, which gives this inverter its name of active neutral point clamped (ANPC)

or active diode-clamped multilevel inverter (ADCMLI). However, these advantages come at the expense of a more complex circuit structure and the need to control the additional switching devices.

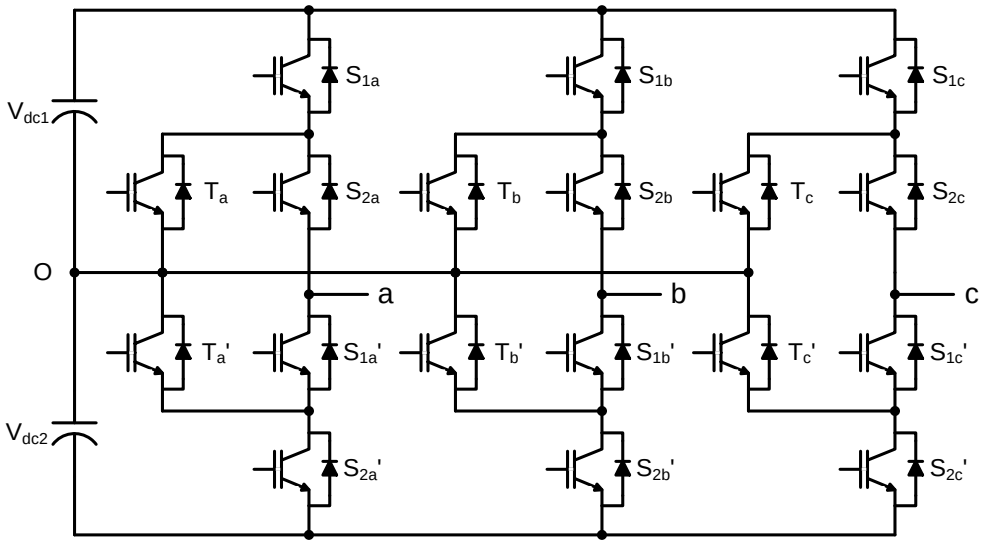


Figure 2.5 A three-phase three-level active diode clamped multilevel inverter.

2.4.2 Flying Capacitor Mulitlevel inverter (FCMLI)

Another fundamental multilevel topology, the flying capacitor inverter, involves a series connection of capacitor switching cells[54]. This topology has several unique and attractive features when compared to the DCMLI. One feature is that clamping diodes as required in DCMLI are not needed. Furthermore, the FCMLI has a switching redundancy within a phase, which can be used to balance the voltages of the flying capacitors (C_F) and equally distribute the switching and conduction losses of the semiconductor switches[55]–[57]. The circuit configuration of a five-level FCMLI is depicted in Figure 2.6. In summary, advantages and disadvantages of a FCMLI converter are as follows.

Advantages:

- Modular in structure and the number of levels can be increased to any arbitrary value.
- Large number of capacitors provide extra ride through capabilities during power outage.
- The switching state redundancy provides a great flexibility for the design of the switching pattern and natural balancing of capacitor voltages.
- Reconfiguration of circuit is possible during fault or under-rated conditions.

Disadvantages:

- An excessive number of storage capacitors are required when the number of inverter levels is high. High-level systems are more difficult to package and more expensive with the required bulky capacitors.
- Capacitors voltages have to be pre-charged at startup to a value which are close to their nominal values.

The above disadvantages make this inverter limited to medium-voltage, high-power applications. However, FCMLI have found particular applications for high bandwidth–high switching frequency applications such as medium-voltage traction drives.

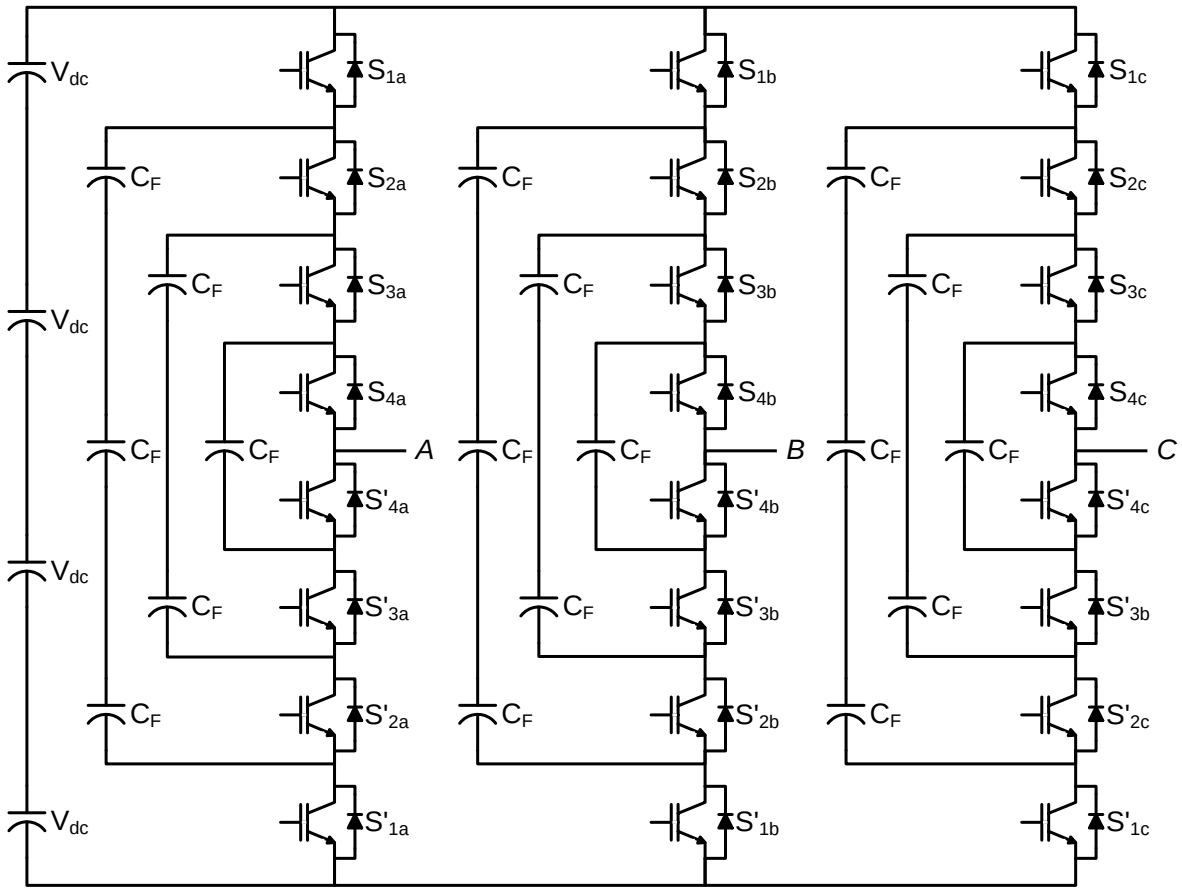


Figure 2.6 A three-phase five-level flying-capacitor multilevel inverter.

2.4.3 Cascaded Multilevel inverters (CMLI)

The CMLI appeared first in 1988, matured during the 1990s and gained more attention after 1997. The CMLI family is characterized by cascade connection of modular chopper-cells or H-bridge cells to form each cluster or arm[58]. This brings flexibility to circuit design, and results in low-voltage steps. The CMLI with H-bridge cells are known as Cascade H-bridge (CHB) multilevel inverters and on the other hand, CMLI composed with bidirectional chopper cells are known as Modular Multilevel Inverters (MMI). However, the common concepts hidden in the

family members are both “modular” structure and “cascade” connection. These concepts allow power electronics engineers to use the common term “Modular Multilevel Cascade Inverter (MMCI)” as a family name[59]. Hereafter in this thesis cascaded multilevel inverters are referred as modular multilevel cascade inverters.

The MMCI is one of the next-generation multilevel Inverters intended for high or medium-voltage power conversion without line-frequency transformers[60]. The family of MMCI consists of following members:

1. Single-star bridge cells (SSBCs)
2. Single-delta bridge cells (SDBCs)
3. Double-star chopper cells (DSCCs)
4. Double-star bridge cells (DSBCs).

The particular advantages of MMCI are:

- They can achieve high or medium-voltage power levels with mature low-voltage semi-conductor devices.
- They can easily expand to higher number of levels with easy construction, flexibility in converter design.
- A direct connection to the system is possible by eliminating the line-frequency transformer. This is particularly advantageous as the existence of the transformer makes the converter heavy and bulky, and also induces a dc magnetic flux deviation during single-line-to-ground faults[61].

Among the members of MMCI, SSBC and SDBC are particularly suitable for applications such as Static Synchronous Compensator (STATCOM), Battery Energy Storage System (BESS), and Dynamic Voltage Restorer (DVR).

In SSBC and SDBC based inverters, each cell includes a single-phase H-bridge cell, and an independent or isolated voltage source provided by floating capacitors or transformer secondaries or batteries. The resulting phase voltage is synthesized by the addition of the voltages generated by the different H-bridge inverters. Figure 2.7 and Figure 2.8 show the following two circuit configurations, respectively: the single-star bridge cells (SSBC) and the single-delta bridge cells (SDBC). The reason for such nomenclature is that both are based on three strings of multiple H-bridge cells with either star or delta connection.

The number of levels (m) in phase-to-ground voltage of a SSBC or SDBC based inverter with N number of H-bridge cells per phase leg can be found from eq.(2.1)

$$m = 2N + 1 \tag{2.1}$$

For MMCI, *m* is always an odd number while in other multilevel topologies such as DCMLI and FCMLI, it can be either an even or odd number.

Table 2-1 lists all the voltage levels and their corresponding switching states to synthesize five-level voltages across *a*–phase and *M*. It should be noted that some voltage levels can be obtained by more than one switching combination.

More recently, SSBC inverters with unequal dc source, also known as hybrid or asymmetric cascaded inverters have been introduced. The circuit configuration of the topology for a five-level SSBC inverter with unequal dc sources is very similar to the regular SSBC shown in Figure 2.7, the difference is that the isolated dc sources have different values. When choosing unequal dc sources, some switching-state redundancies are avoided, and more different output-voltage levels are generated with the same number of power cells. This reduces the size and cost of the inverter and improves reliability. An additional advantage is that the inverter can be controlled appropriately to reduce the switching losses, which is very important in high-power applications.

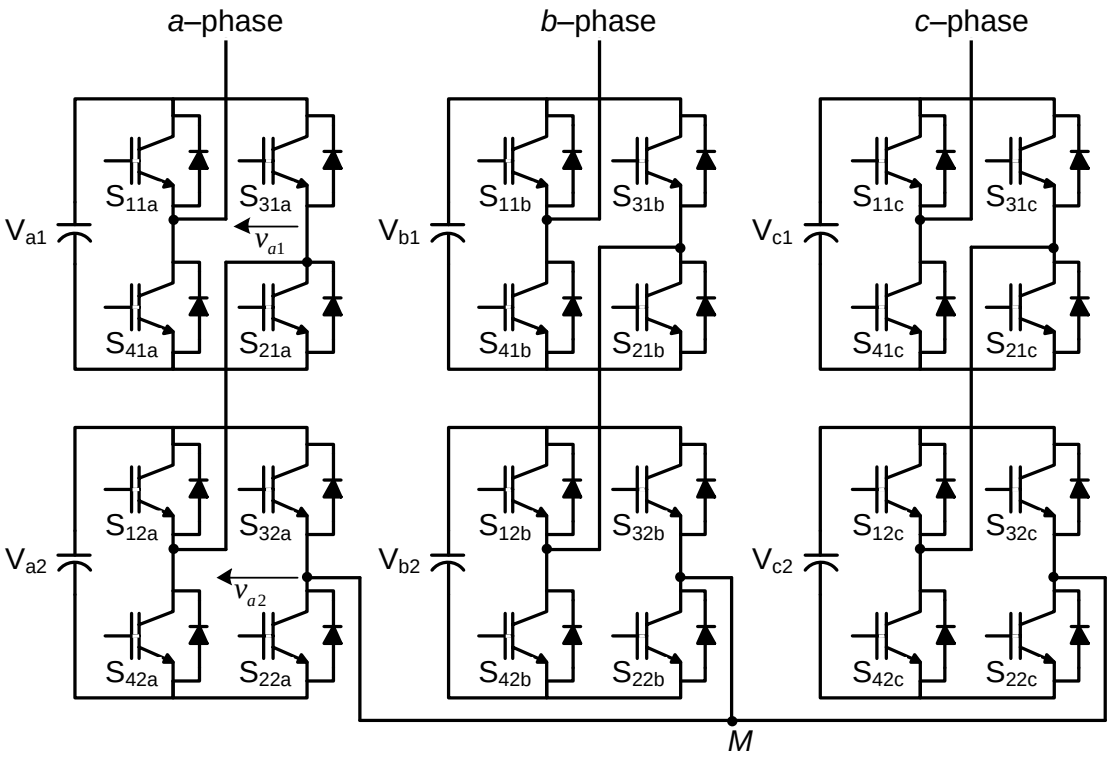


Figure 2.7 A three-phase five-level SSBC based modular multilevel inverter topology.

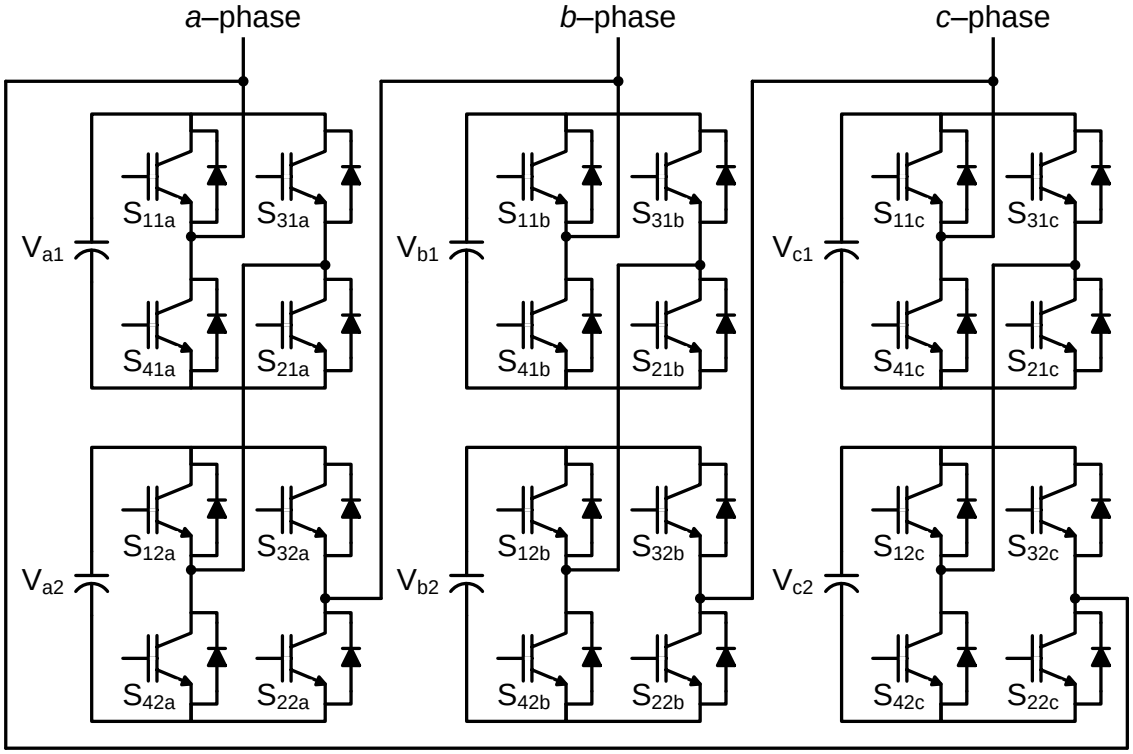


Figure 2.8 A three-phase five-level SDBC based modular multilevel inverter topology.

Table 2-1 Voltage levels and their corresponding switch states for a five-level SSBC or SDBC based inverter.

Output Voltage	Switch State (1 means switch is ON and 0 means OFF)							
	S_{11}	S_{31}	S_{12}	S_{32}	S_{41}	S_{21}	S_{42}	S_{22}
$V_{AM} = +2V_{DC}$	1	1	1	1	0	0	0	0
$V_{AM} = +V_{DC}$	1	1	1	0	0	0	0	1
	0	1	1	1	1	0	0	0
	1	0	1	1	0	1	0	0
	1	1	0	1	0	0	1	0
$V_{AM} = 0$	1	1	0	0	0	0	1	1
	0	0	1	1	1	1	0	0

	1	0	0	1	0	1	1	0
	0	1	1	0	1	0	0	1
	1	0	1	0	0	1	0	1
	0	1	0	1	1	0	1	0
$V_{AM} = -V_{DC}$	1	0	0	0	0	1	1	1
	0	1	0	0	1	0	1	1
	0	0	1	0	1	1	0	1
	0	0	0	1	1	1	1	0
$V_{AM} = -2V_{DC}$	0	0	0	0	1	1	1	1

The main drawback of this inverter is the fact that the modularity and switching redundancy of the inverter are lost, since the different power ratings of the cells force special design for each power cell (even different power-device families could be needed). In addition, no input-current harmonic cancellation can be achieved, since the power asymmetry disables the multipulse rectifier and transformer function. In summary, advantages and disadvantages of a SSBC or SDBC based inverters are as follows.

Advantages:

- Requires the least number of components among all multilevel inverter configurations to achieve the same number of voltage levels.
- Modularized circuit layout and packaging is possible because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors.
- Provides switch combination redundancy for a natural voltage balancing of capacitors.
- Reconfiguration of circuit is possible during under-rated or fault conditions.

Disadvantages:

- Needs separate dc sources for power conversions.

2.5 Comparative evaluation of multilevel converters for D-STATCOM

The selection of individual inverter topologies for D-STATCOM applications depends on their performance, cost, size, and implementation factors. Table 2-2 gives the comparison of power component required per phase-leg for the above discussed multilevel inverter topologies. From Table 2-2, it can be observed that the SSBC or SDBC inverter requires least number of power components[62].

Table 2-3 gives the comparison of multilevel inverter topologies based on their implementation factors. Although FCMLI have a natural voltage balancing operation and modular structure, but its application as a D-STATCOM is limited due to the requirement of large number of capacitors and their initialization process (pre-charge).

Table 2-2 Comparison of power component requirements per phase-leg among multilevel inverter topologies.

Power component	Inverter topology		
	DCMLI	FCMLI	SSBC or SDBC
Main switching devices	$2(m-1)$	$2(m-1)$	$2(m-1)$
Anti-parallel diodes	$2(m-1)$	$2(m-1)$	$2(m-1)$
Clamping diodes	$(m-1)(m-2)$	0	0
DC bus capacitors	$(m-1)$	$(m-1)$	$\frac{(m-1)}{2}$
Flying capacitors	0	$\frac{(m-1)(m-2)}{2}$	0

Table 2-3 Comparison of multilevel inverter topologies based on implementation factors.

Implementation factor	Inverter topology		
	DCMLI	FCMLI	SSBC or SDBC

Specific requirements	Clamping diodes	Additional capacitors and their initialization	Isolated dc sources
Modularity	Low	High	Very high
Design and implementation complexity	Low	Medium	Least (with transformer-less applications)
Control concerns	Voltage balancing	Voltage setup	Power sharing
Fault tolerance	Difficult	Easy	Easy
Applications	CSDs, ASDs, conveyors, marine applications, and regenerative applications such as mining and renewable energy.	ASDs, medium-voltage traction drives.	FACTS, CSDs, High-power ASDs, electric and hybrid vehicles, photovoltaic power conversion, uninterruptible power supplies, and magnetic resonance imaging.
Cost	Low (3-level), high (>= 4-level).	Medium (3-level), high (>= 4-level).	Very low (transformer-less applications), high (input transformer applications).
Available commercial ratings	2.3 to 6.6 kV, 3.7 to 44 MVA.	2.3 to 4.16 kV, 2.24 to 8 MVA.	2.3 to 13.8 kV, 6.2 to 120 MVA.

On the other hand, the SSBC, SDBC and DCMLI topologies seem to be the most suited for D-STATCOM applications. But, the requirement of large number of power components and voltage unbalance problem at higher levels limits the DCMLI for low power rating applications. The requirement of least number of component, modular structure, high fault tolerance ability and absence of complex input transformer as well as non-initialization of the capacitor voltages makes SSBC and SDBC best suited for D-STATCOM and other custom power applications. SSBC and SDBC can reach higher output voltage and power levels (13.8 kV, 30 MVA) and achieves higher level of reliability due to its modular topology[49], [61]. Table 2-4 summarizes the comparisons among SSBC and SDBC based inverters from various points of view[62].

Table 2-4 Comparison of SSBC and SDBC topologies.

Terminology	SSBC	SDBC

Main objectives	Positive-sequence reactive and/or active power	Negative-sequence reactive and/or active power
Cell-count ratio	1	$\sqrt{3}$
Circulating current	No	One degree of freedom
Grid inductor	Yes	Yes
Motor drives	No, but limited expectations exist	No, but limited expectations exist
Grid applications	STATCOM, Battery energy storage system, DVR, APF	STATCOM (flicker compensation), Battery energy storage system
Practicability	+++++	++

The "cell-count ratio" in the third row of Table 2-4 means the ratio of the cell count of each MMCI member to that of the SSBC under the following assumptions: the IGBTs used in the four MMCI members have the same blocking voltage, and both members have the same power and voltage ratings. As a result, the IGBTs have different current ratings because the count of the IGBTs is different in SSBC and SDBC. The "practicability" in the last row ofTable 2-4 includes technical aspects as well as the market size of each member. From Table 2-4 it is observed that applications of the SSBC can be made at the lowest cost because SSBC has fewer cell count ratio than SDBC.

The SDBC has the capability to control negative-sequence reactive power and has recently found some dominant applications in arc furnace industries. However, the circulating current and high cell-count ratio restricted the SDBC applications for controlling positive-sequence leading and lagging reactive power as well as real power. But, on the other hand, the SSBC seems to be the best choice for controlling positive-sequence leading and lagging reactive power as well as real power. As this thesis is devoted for positive-sequence reactive power compensation, a SSBC based inverter has been considered as a power circuit of the D-STATCOM.

2.6 Carrier based PWM schemes

The carrier based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations[35], [40], [63]–[66]. These two techniques are the natural extensions of carrier-based sinusoidal PWM technique used for two level inverters and both modulation schemes can be applied to the SSBC based inverters.

2.6.1 Phase shifted pulse width modulation (PSPWM)

In this scheme, every pair of switches has a carrier signal which has a phase difference with the other carrier signals. In general, a multilevel inverter with *m* voltage levels, requires (*m*–1) triangular carrier signals. In this method all the triangular carrier signals have the same frequency and the same peak-to-peak amplitude, but there is a phase shift (φ_{cr}) between any two adjacent carrier signals, given by

$$\varphi_{cr} = \frac{360°}{(m-1)} \tag{2.2}$$

The modulating signal is usually a three-phase sinusoidal wave with adjustable amplitude and frequency. The gate signals are generated by comparing the modulating signal with the carrier signals. When the modulating signal is more than the carrier signal, the upper switch is on and when it is less than carrier signal, the lower switch is on.

In this technique, the fundamental-frequency component in the inverter output voltage can be controlled by amplitude modulation index (m_a), which is defined as,

$$m_a = \frac{V_m}{V_{cr}} \tag{2.3}$$

Where V_m and V_{cr} are the peak values of the modulating and carrier signals, respectively. The frequency modulation index (m_f) is defined by,

$$m_f = \frac{f_{cr}}{f_m} \tag{2.4}$$

Where f_m and f_{cr} are the frequencies of the modulating and carrier signals, respectively.

Figure 2.9 shows the principle of the phase-shifted modulation technique for a five-level SSBC based inverter (shown in Figure 2.7), where four triangular carrier signals are required with a 90° phase displacement between any two adjacent carrier signals. In this figure only the phase-*a* modulating procedure is shown for simplicity. Four carrier signals are used to generate gating signals for the switches S_{11a}, S_{12a}, S_{22a}, and S_{21a} respectively of phase leg-*a*. The gating signals for the other switches in the H-bridge cells of phase leg-*a* are not shown since these switches are operated in a complementary manner with respect to their corresponding upper/lower switches.

One of the main advantages with the PSPWM modulation strategy is that it maintains the duty cycles of the cells approximately equal and therefore maintains a uniform power distribution

among H-bridge cells which naturally balances the capacitor voltages of the inverter. This feature makes the PSPWM as a dominant PWM method for SSBC inverters.

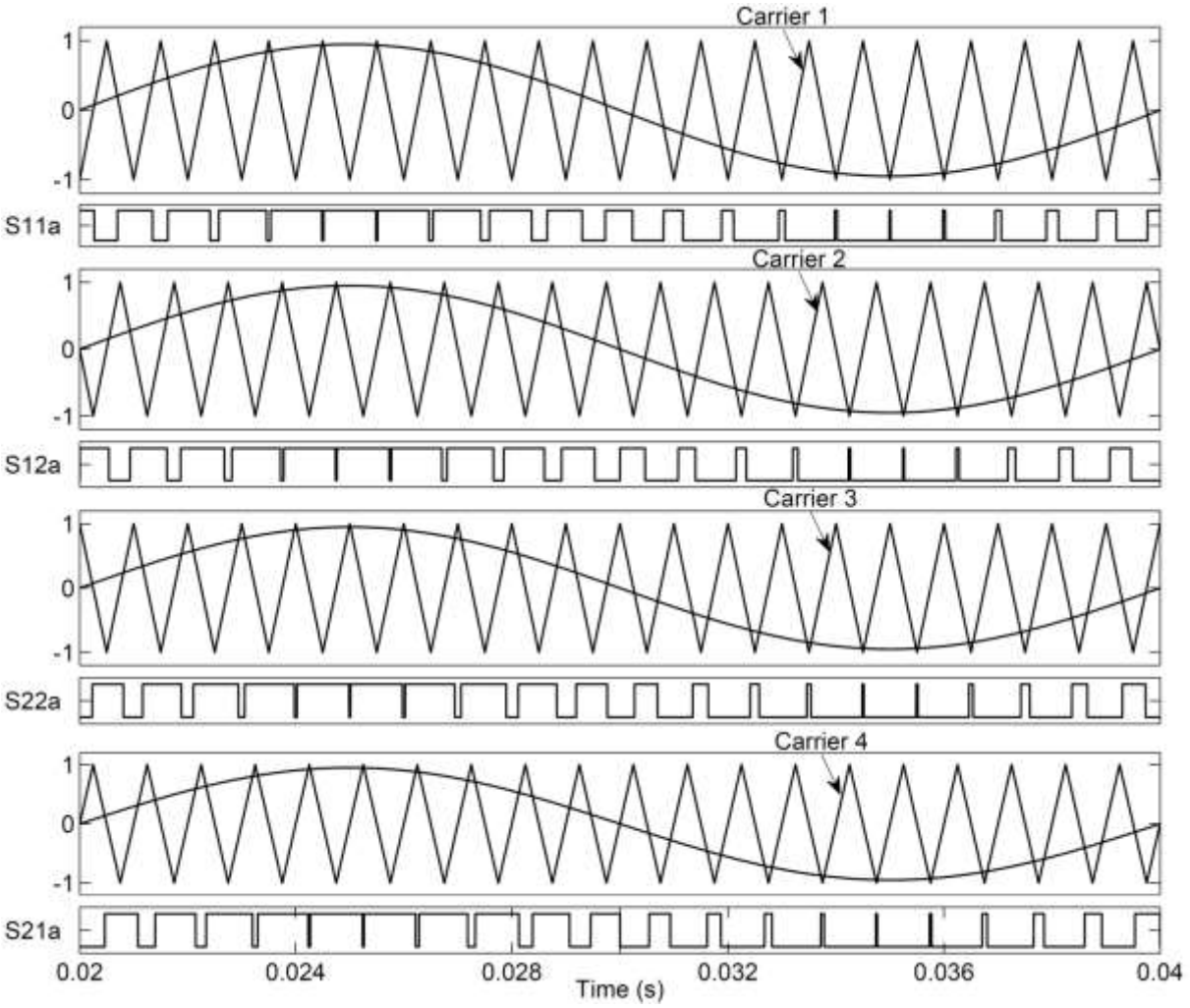


Figure 2.9 PSPWM technique for a five-level SSBC based multilevel inverter.

2.6.2 Level shifted pulse width modulation (LSPWM)

Similar to the phase-shifted modulation, an *m*-level inverter using level-shifted multicarrier modulation scheme requires (*m*–1) triangular carrier signals, all having the same frequency and peak-to-peak amplitude. The (*m*–1) triangular carrier signals are vertically disposed such that the bands they occupy are contiguous. The frequency modulation index (m_f) remains same as that for the phase-shifted modulation scheme whereas the amplitude modulation index (m_a) is defined as:

$$m_a = \frac{V_m}{V_{cr}(m-1)} \tag{2.5}$$

Depending upon the phase relation between individual carrier signals, there are three variants of LSPWM technique.

1. In-phase disposition (All the carriers are in phase)
2. Alternative phase opposite disposition (All carriers are alternatively in opposite disposition)
3. Phase opposite disposition (All carriers above the zero reference are in phase but in opposition to those below reference axis)

Among these three variants, in-phase disposition (IPD) strategy gives rise to the lowest harmonic distortion for the voltage waveform and as a result, this strategy has been referred as LSPWM in this thesis.

Figure 2.10 shows the principle of the In-phase disposed level-shifted modulation technique for a five-level SSBC inverter (shown in Figure 2.7), where four triangular carriers are level-shifted from each other. In this figure only the phase-*a* modulating procedure is shown for simplicity. Four carrier signals are used to generate gating signals for the switches S_{11a}, S_{12a}, S_{22a}, and S_{21a} of phase leg-*a*. The gating signals for the other switches in the H-bridge cells of phase leg-*a* are not shown since these switches are operated in a complementary manner with respect to their corresponding upper/lower switches.

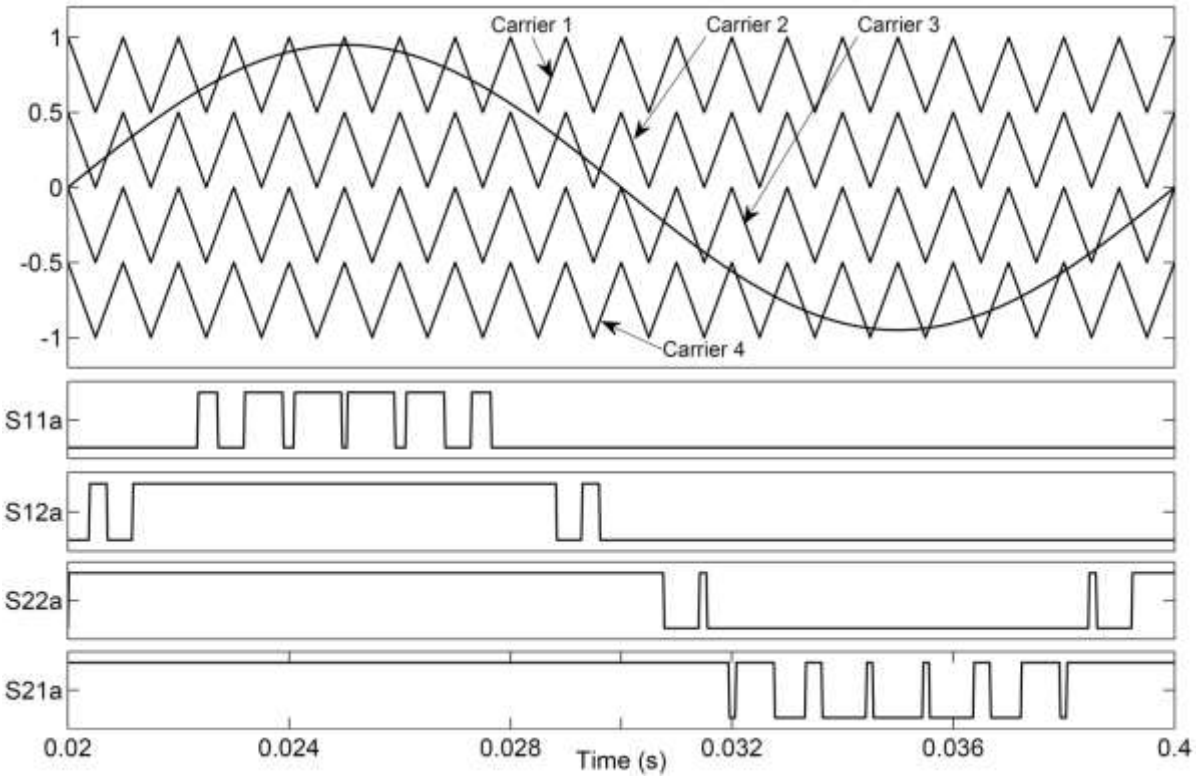
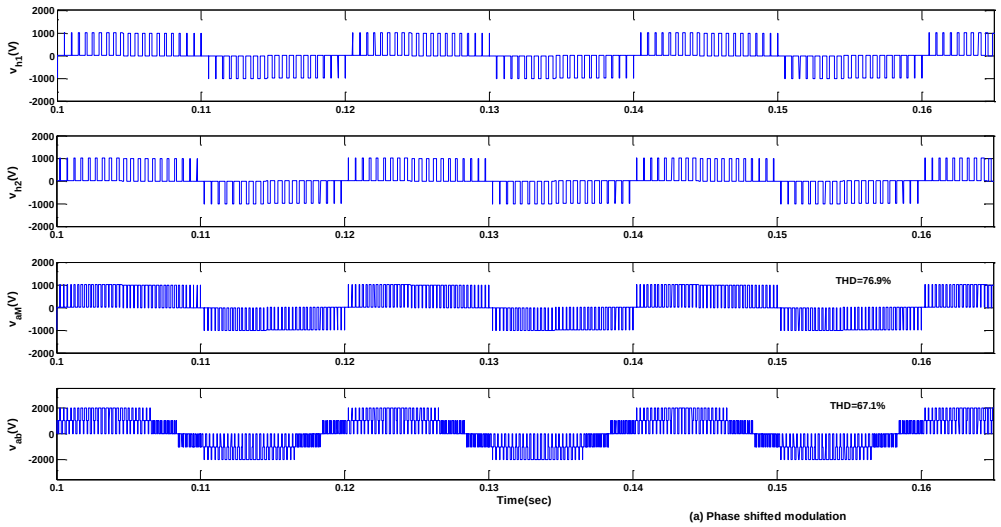


Figure 2.10 LSPWM technique for a five-level SSBC based multilevel inverter.

2.7 Comparison of carrier based PWM Schemes

To compare the performance of phase and level shifted modulation schemes, it is assumed that the average switching frequency of the IGBT switches is the same for both the schemes and the capacitors of SSBC inverter shown in Figure 2.7 are replaced by DC sources. Figure 2.11 shows the output voltage waveforms of a five level SSBC inverter operating with a device switching frequency of 1 KHz and modulation index of 0.4. The differences in the output of the two modulation schemes can be easily distinguished. The H-bridge output voltages v_{h1} and v_{h2}, produced by the phase shifted modulation are almost identical except a small phase displacement among them. All the devices operate at the same switching frequency and conduction time. However, v_{h1} produced by the level-shifted modulation is zero and thus no switching occurs in the H1-bridge. The devices in H2-bridge switch at the carrier frequency of 2 KHz. The inverter phase voltage produced by both the modulation appear to be similar. It contains only three levels instead of five due to the low modulation index. The voltage levels of the inverter line-line voltage (v_{ab}) are reduced accordingly. Furthermore THD of line-line voltage (v_{ab}) produced by the phase shifted modulation is 67.1% and for the level-shifted modulation it is 42.05%. This is mainly caused by the waveform differences in the center portion of the positive and negative half-cycles of line-line voltage (v_{ab}).



(a) Phase shifted modulation

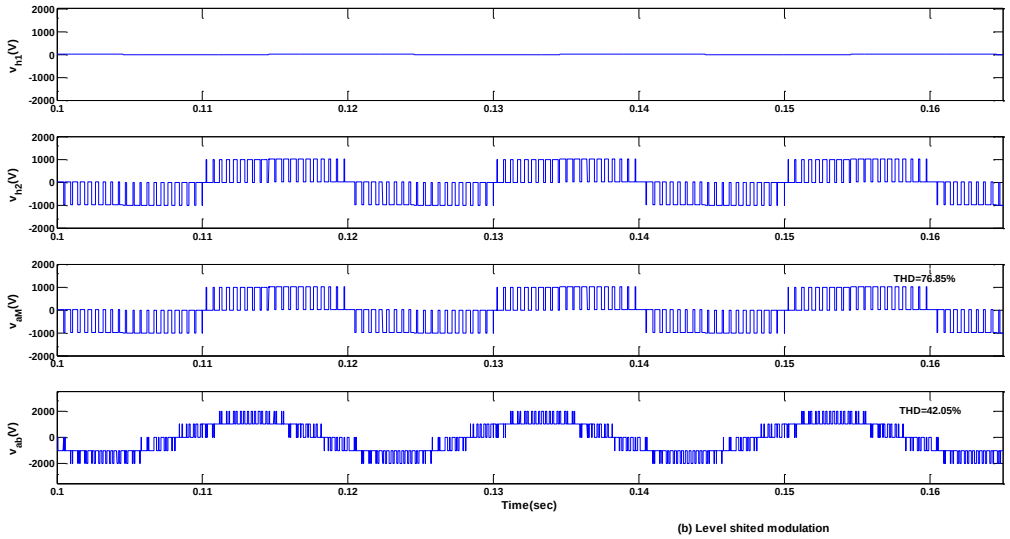


Figure 2.11 Output voltage waveforms of the five level inverter operating at a low modulation index (a) phase siftwed PWM (b) level shifted PWM.

Figure 2.12 shows the THD profile of the line-to-line voltage V_{ab} modulated by the phase and level shifted schemes as a function of modulation index m. It can be observed from this Figure 2.12 the THD of level shifted PWM is better compared to Phase shifted PWM but at higher modulation index the THD difference of the two modulation techniques is small.

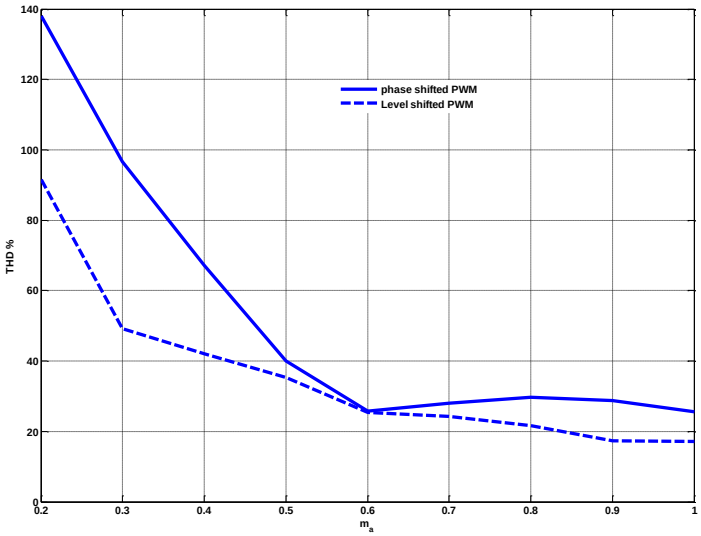


Figure 2.12 Line voltage THD produced by five level SSBC inverter with phase and level shifted modulation schemes.

Table 2-5 comparision between the phase and level shifted PWM schemes.

Comparison	Phase-Shifted modulation (PSPWM)	Level-shifted Modulation (LSPWM)
Device switching frequency	Same	Different
Device conduction period	Same	Different
Line-Line THD	Good	Better
Capacitor balancing	Excellent	poor

A summary of the carrier-based modulation schemes for the SSBC multilevel inverters is given in Table 2-5. For the phase shifted pulse width modulation the device switching frequency and conduction period are same compared to the level shifted pulse width modulation. These uneven losses in the SSBC inverter can create the voltage imbalance in the DC capacitors when this inverter is employed for D-STATCOM application. The capacitor voltage balancing algorithm for SSBC inverter by using the PSPWM is focused in further chapters.

2.8 Scheme for calculating switching and conduction losses

The current flowing through the IGBT and freewheeling diode are separated in order to calculate the losses independently in these two components. The loss calculation procedure is given in flowchart Figure 2.13, this procedure is repeated after every sampling interval (T_S). For high power IGBT modules it is necessary to provide a suitable heat sink, otherwise, it may go into the thermal runaway. The summation of losses occurred in IGBT and freewheeling diode is given to a thermal model. The thermal capacitance of the device junction as well as its junction-to-case thermal resistance are represented by a one-cell cauer network modeled with a Simulink State-space block. The Thermal Network Simscape blocks from the thermal foundation library are used to build a one-cell cauer network based on the thermal capacitances (case and heat sink) and resistances (case-to-sink and sink-to-ambient). The output of this one-cell cauer network is the junction temperature.

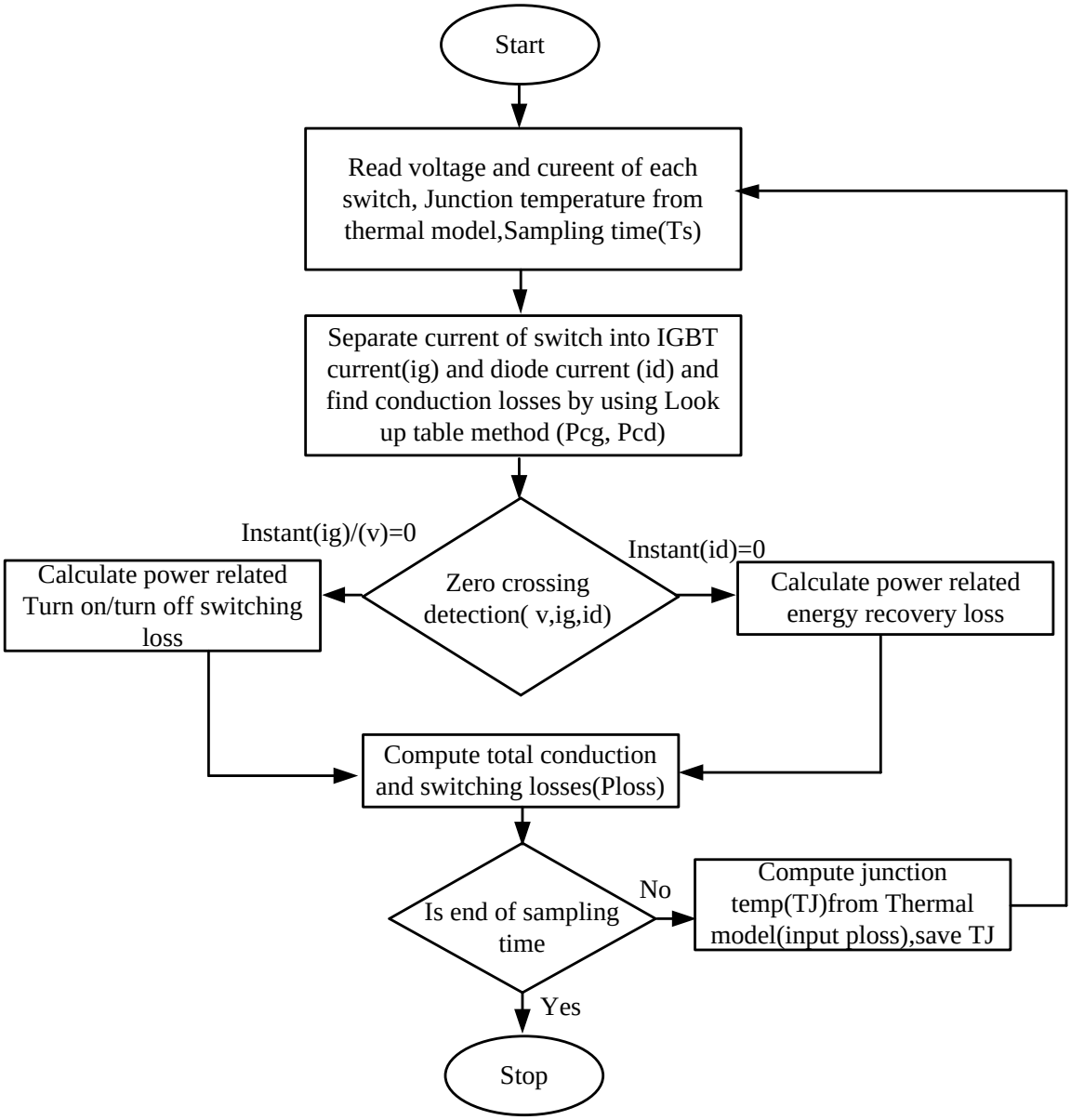


Figure 2.13 Procedure to caliculate the losses in a switch.

2.8.1.1 Conduction loss:

The conduction loss for IGBT and diode are calculated by look up table method. The procedure to find both of the losses is given below. Value of the current (ig/id) flowing in the IGBT/diode and its junction temperature (T_J) determine what would be the saturation voltage (V_{on}) across the IGBT/diode by using a 2-D look-up table shown in Figure 2.14. This V_{on} is then multiplied by ig/id to obtain the conduction losses which are injected into the thermal network. The separate look up tables are prepared for IGBT and diode. The 2-D look-up table is prepared in SIMULINK considering data sheet of manufacturer for IGBT and diode. For example the V-I characteristics of ABB are given in Figure 2.15 and Figure 2.16 for diode and IGBT respectively. Two inputs (I_c/ I_f & T_J) of these two figures considering some data points and the output is

specified at that points. The look up table in a MATLAB/SIMULINK uses a linear interpolation method when the inputs are with-in the range otherwise a linear extrapolation method is used.

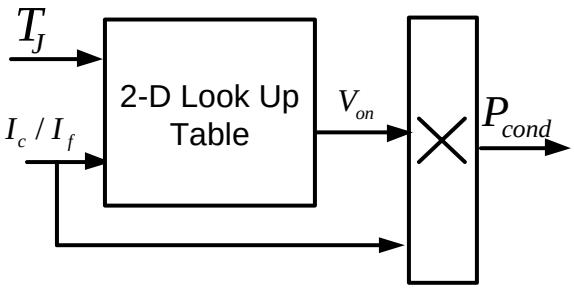


Figure 2.14 Calculation of conduction loss of IGBT/Diode.

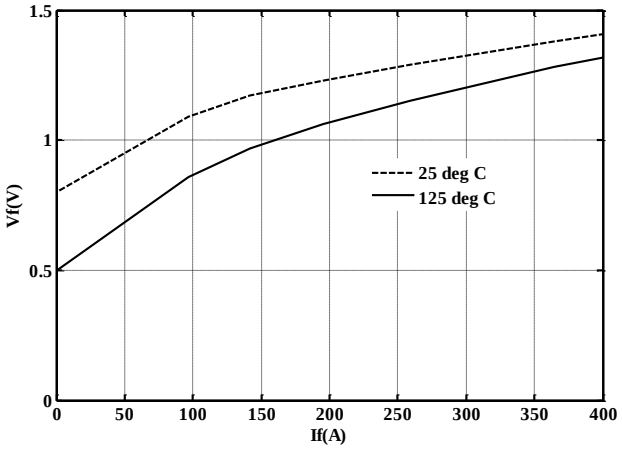


Figure 2.15 Diode on state charecteristics.

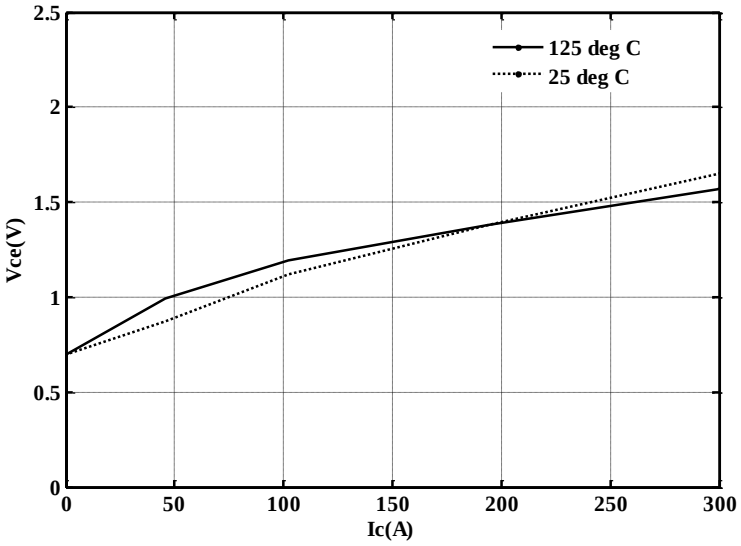


Figure 2.16 IGBT on-state Characteristics.

2.8.1.2 Turn-on/off switching loss and Diode Reverse recovery loss:

Pre-switching value of the voltage across the device, post-switching value of the current flowing into the device, and the junction temperature are used to determine the energy losses with the help of a 3-D lookup table. The separate 3-D lookup tables are prepared for determining the switching on /off losses of an IGBT and recovery loss of diode. The 3-D lookup is prepared in SIMULINK considering data sheet of manufacturer. For example the ABB characteristics is given in Figure 2.18 and Figure 2.19, three inputs (I_c, T_J &V_{cc}) of this figure considering some data points and the E_{on}/ E_{off} / E_{rec} is specified at these points. This energy is converted into a power pulse which is shown in Figure 2.17. The switching on signal is detected and monostable generator generates a pulse of height unity with a duration of ΔT dividing with a pule width of ΔT generates a pulse signal with a unity of sec^{-1} that is multiplied with either energy E_{on}/ E_{off}/ E_{rec} to get a switching on power loss this is injected into the thermal network.

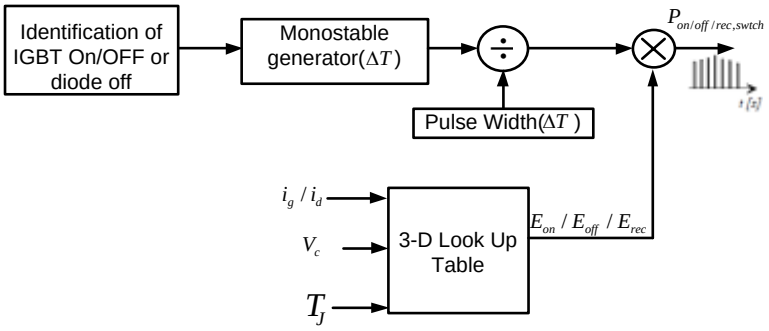


Figure 2.17 Calculation of switching loss.

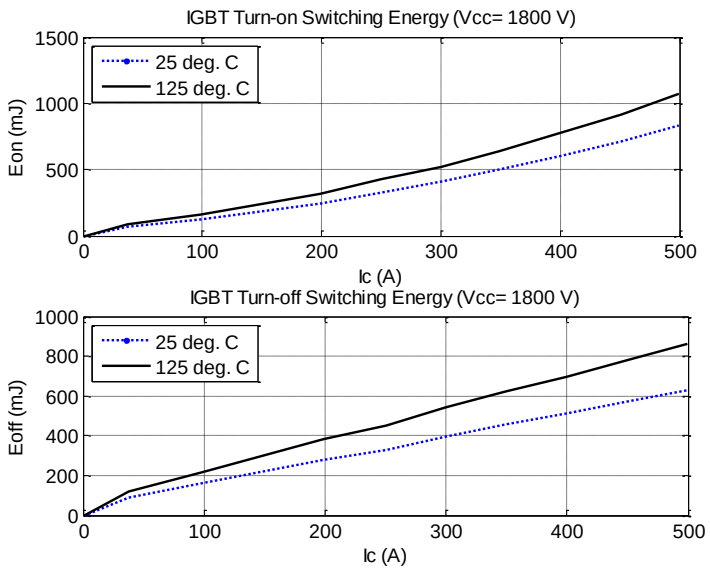


Figure 2.18 Energy loss during turn on and turn off of IGBT switch.

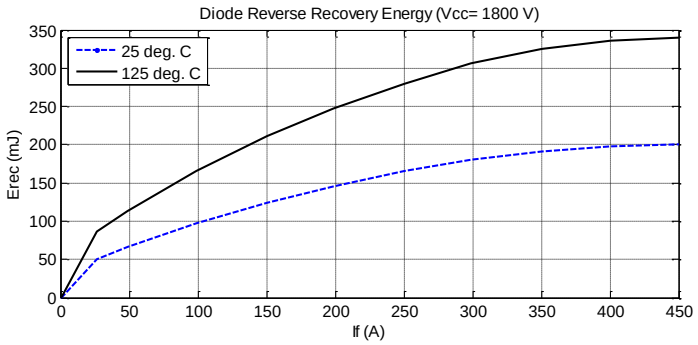


Figure 2.19 Energy recovery loss of diode.

2.9 Power loss calculation in five level SSBC inverter

The three phase five level SSBC inverter is shown in Figure 2.7 the capacitors are replaced with the dc sources. In case of the Phase shifted pulse width modulation, it is observed that conduction period and switching frequency of each switch in H-bridge is the same. In this section a quantification of losses in each H-bridge is calculated for the SSBC inverter in a closed loop current controller mode of operation. The function of the inverter current controller is to force the actual current to follow the reference currents as closely as possible. The currents measured at the output of this inverter are compared with the reference currents and the error signals are processed in a PI current controller to generate the corresponding modulating signal.

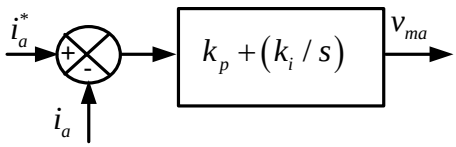


Figure 2.20 Current controller for phase-a.

The current controller realization for phase-a is shown in Figure 2.20, the same realization is implemented for remaining two phases. The parameters *kp* and *ki* of the PI current controller affect the steady state error and the transient response of the control. The output of the current controller is compared with phase shifted triangular carrier waves and firing pulses of the switches are generated as discussed in section 2.6.1. The unbalanced reference currents considered for simulation are given by eq.(2.6).

$$\left.\begin{aligned} i_a &= 200\sqrt{2}\sin(\omega t)+\frac{200\sqrt{2}}{5}\sin(5\omega t)+\frac{200\sqrt{2}}{7}\sin(7\omega t) \\ i_b &= 160\sqrt{2}\sin(\omega t-2\pi/3)+\frac{200\sqrt{2}}{5}\sin(5\omega t+2\pi/3)+\frac{200\sqrt{2}}{7}\sin(7\omega t-2\pi/3) \\ i_c &= 183.3\sqrt{2}\sin(\omega t+13\pi/18)+\frac{200\sqrt{2}}{5}\sin(5\omega t-2\pi/3)+\frac{200\sqrt{2}}{7}\sin(7\omega t+2\pi/3) \end{aligned}\right\} \quad (2.6)$$

Table 2-6 Simulation parameters for power loss calculation.

Parameter	**Value**
DC source voltage	1.2 kV
Load	R_L = 0.2 Ω, L_s = 10 mH
Carrier frequency	1.8 kHz
PI current controller parameters	K_p = 0.02, K_i = 0.04
Energy to power conversion	ΔT =5µsec
Thermal Resistance [case to sink sink to ambient]	[0.02K/W 0.072K/W]
Thermal Capacitance[case sink]	[0.1J/K 0.5J/K]
Sampling time	50µsec
Device data sheets	ABB 5SNE0800M170100 FUJI 2MBI15012A060

The Figure 2.21 shows the simulated performance of inverter for a reference current given in eq.(2.6), when all the H-bridges are employed with ABB IGBT switches. The figure shows the actual current, modulating signal and the losses over a fundamental period in each H-bridge. It is observed that losses occurred in each H-bridge for a phase a, b and c are 1750W, 1440, 1580W respectively. The total loss occurred in two H-bridges of phase-a is 1750*2=3500W, phase-b 1440*2=2880W and similarly for phase-c are 1580*2=3160W.

The Figure 2.22 shows the performance of inverter for a reference current given by eq.(2.6) When one of the H-bridge in each phase is realized with the manufacture ABB and the other with Fuji. The figure shows the actual current, modulating signal and the losses over a fundamental period in each H-bridge of each phase. It can be observed loss occurred in each H-bridge are different. The losses occurred in two H-bridges of phase-a are 1750W, 1210W and for phase-b 1440W, 820W similarly for phase-c 1580W, 1020 W.

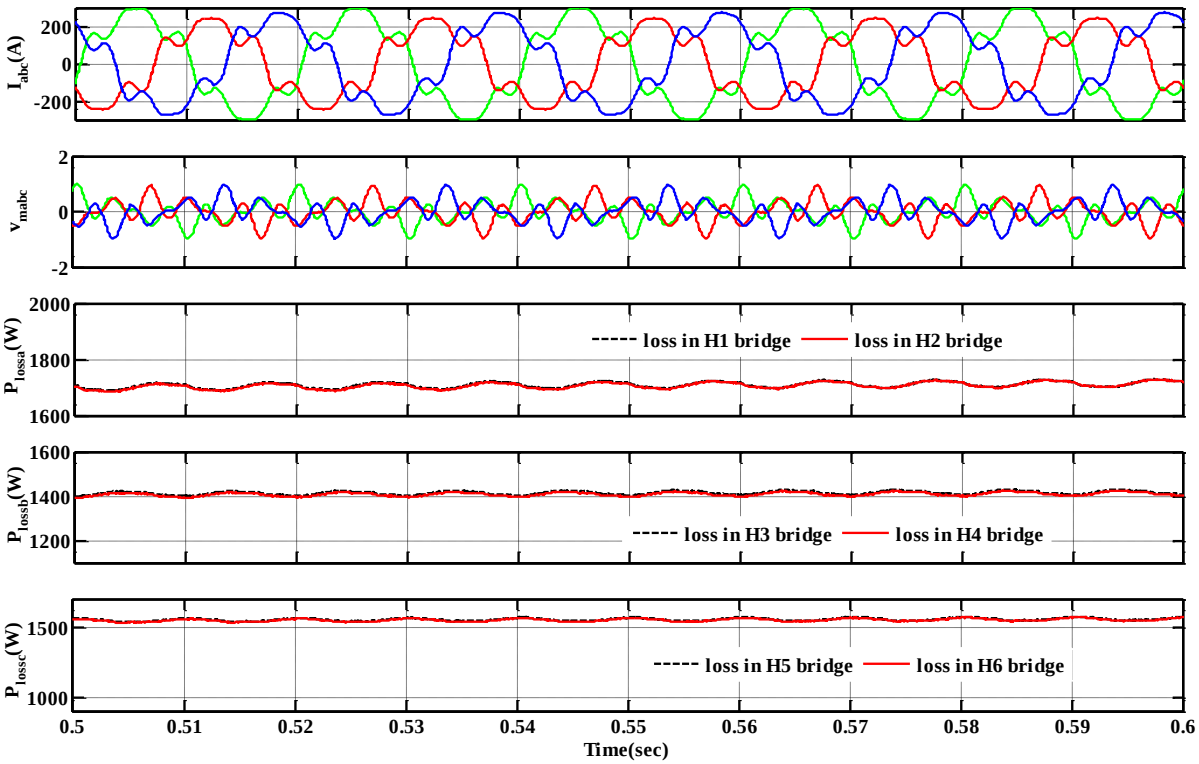


Figure 2.21 Perormance of SSBC inverter with reference unbalanced currents and at the same device charecteristics.

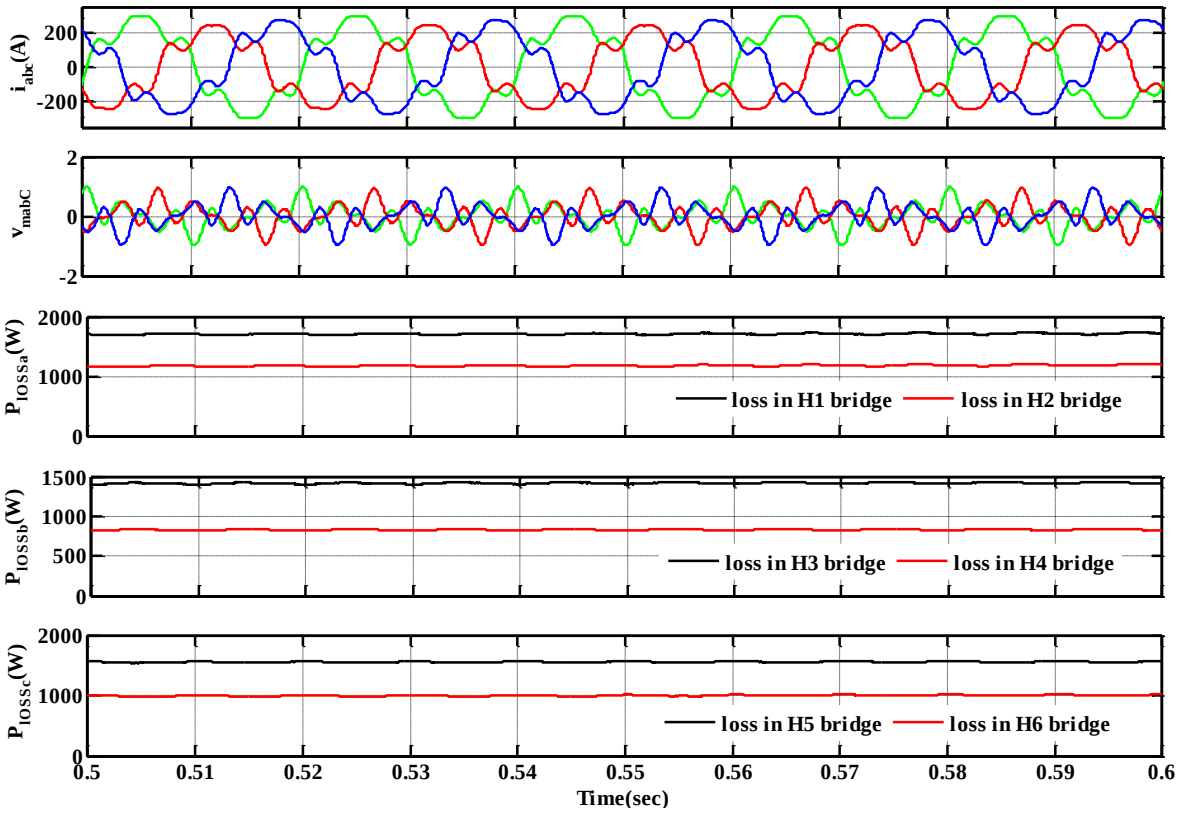


Figure 2.22 Perormance of SSBC inverter with reference unbalanced currents and at the different device charecteristics.

The unequal losses produced in each H-bridge will create the voltage imbalance for the DC capacitors when this inverter is used for D-STATCOM. Therefore, the DC capacitor voltage balancing is need to be address with in the phase (individual voltage balancing) and as well as in between the phases (cluster voltage balancing).

2.10 Conclusion

In this chapter the selection of SSBC inverter topology suitable for D-STATCOM application is discussed. The difference between phase shifted and level shifted pulse width modulation has been brought out in terms of device switching frequency and output voltage THD. The detailed simulation has been carried out by developing MATLAB models for power loss calculation. The effect of inverter unbalance currents and/or mismatched device characteristics on the H-bridge losses are discussed.

CHAPTER 3: CASCADED H-BRIDGE BASED SINGLE PHASE D-STATCOM

[This chapter presents the single phase cascaded H-bridge D-STATCOM used for reactive power compensation, harmonic elimination. The 1-ϕ pq *control theories required to generate the reference currents for D-STATCOM are discussed. The asymmetries in the device characteristics among the H-bridges leads to the deviation in the capacitor voltages. The two capacitor voltage balancing methods namely improved modulating signals method (IMS) and active voltage superposition method (AVS) are discussed.]*

3.1 Introduction

Ideal D-STATCOM has no power loss and it would either supply or absorb the reactive power. In such a case, the amount of capacitor charging and discharging in a cycle would be the same so that DC capacitor voltages will be balanced. However, the switch conduction loss, their asymmetries, and non-ideal passive components cause unequal power dissipation leading to capacitor voltage unbalance. This problem becomes more severe when the D-STATCOM is used for the power factor improvement of highly inductive loads. The methods available in the literature for capacitor voltage balancing can be classified into two categories- optimal PWM technique and Modified control strategy. The optimal PWM technique makes use of switching redundancies, selective harmonic elimination[67]–[72], and model predictive control[73]. The disadvantage of this method is that a central switching controller is required for the system and the pulse width modulator (PWM) generator is not modular. In the second method, the control strategy for DC capacitor voltage uses a phase shifted pulse modulator for each H-bridge with hierarchical control. An individual voltage balancing (IVBS) has been proposed in [74] to realize independent modulation control for each H-bridge in which an active power component is superposed on AC voltage of H-bridge. The scheme of [74] claims to use the same power factor angle for all the H-bridges in its control scheme but it is found to be different in this simulation study. The active voltage superposition method (AVS) is proposed in [75], where the error of the DC voltage is multiplied by the current along with a scaling factor, which is difficult to tune. The main control strategy and auxiliary control for individual DC capacitor balancing are perfectly decoupled in [76]. The power factor angle is computed for each H-bridge by a combination of PLL and Fourier series. The individual capacitor balancing control adjusts the modulating control signal of each H-bridge such that the each H-bridge handles equal reactive

power. Further, the active power requirement of each H-bridge is maintained at desired level to achieve capacitor voltage balancing. The simulation based comparison study is done for both the methods, with a aim to further improve the performance of PWM scheme.

3.2 System configuration and pulse width modulation

Figure 3.1shows the circuit configuration of single phase cascaded H-bridge D-STATCOM consisting of two H-bridges. A coupling inductor (L_c) is connected to the grid and D-STATCOM. The power loss in the H-bridges is represented with an equivalent resistor R_{L1} and R_{L2}. The equations that describe the single phase CHB D-STATCOM are given by eq.(3.1)-(3.5) . Equations (3.1)-(3.2)represent the AC voltages generated by H-bridge which are controlled by the respective modulating signals (m_{h1}, m_{h2}). The D-STATCOM current dynamics is represented by eq.(3.3). Since the source voltage and coupling inductor being constant, the current magnitude and its shape and phase are controlled by the vector sum of the AC voltages developed by two H-bridges. The voltage dynamics of the DC capacitors are given by eq. (3.4)-(3.5). The instantaneous power input to H-bridge is equal to the sum of the instantaneously stored power and loss power across the equivalent resistors.

$$v_{a1} = m_{h1} v_{c1} \tag{3.1}$$

$$v_{a2} = m_{h2} v_{c2} \tag{3.2}$$

$$v_p = L\frac{di_c}{dt} + v_{a1} + v_{a2} \tag{3.3}$$

$$v_{a1} i_c = C\frac{d}{dt}\left(\frac{v_{c1}^2}{2}\right) + \frac{v_{c1}^2}{R_{L1}} \tag{3.4}$$

$$v_{a2} i_c = C\frac{d}{dt}\left(\frac{v_{c2}^2}{2}\right) + \frac{v_{c2}^2}{R_{L2}} \tag{3.5}$$

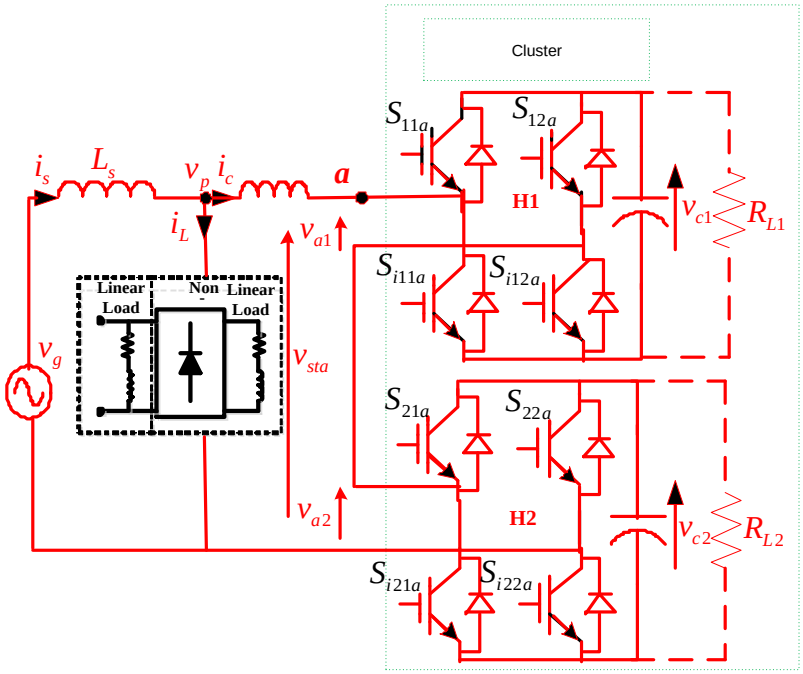


Figure 3.1 Circuit configuration of single phase cascaded H-bridge D-STATCOM.

Each H-bridge is having an isolated DC capacitor and the each leg, the switches are triggered complementarily such that the possible outputs are $+V_{dc}$, 0, and $-V_{dc}$ (for the capacitor reference voltage V_{dc}) providing two non-zero voltages and one zero voltage. Two H-bridges connected in series so that five levels in the output voltage of D-STATCOM are produced. The switching pulses for D-STATCOM can be generated with the two modulating signals (m_{h1}, m_{h2}) and two phase shifted triangular carrier waves. The logic circuit for the generation of switching pulses of the D-STATCOM with the SIMULINK blocks is given in Figure 3.2. In Figure 3.2 the two different colours are used to indicate the switching pulses of two H-bridges in D-STATCOM, the modulating signals (m_{h1}, m_{h2}) are different for the two H-bridges, whereas the triangular carrier wave for H2-bridge is phase shifted by 90^0. Each modulating signal is compared with the triangular carrier to generate a switching signal for H- bridge devices.

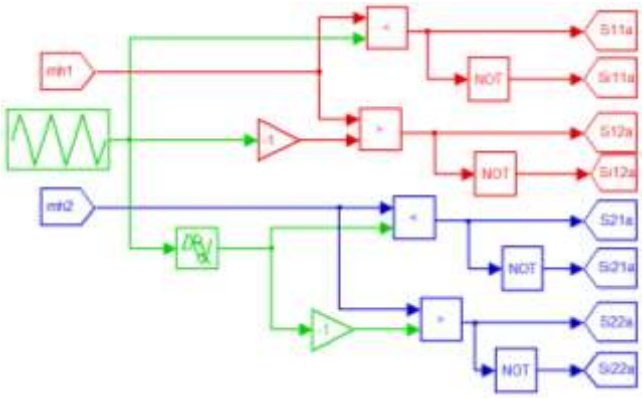


Figure 3.2 Phase shift pulse width modulation.

3.3 Design of 1-phase 1.2 KV 100 KVA five level CHB based D-STATCOM

To design a single phase five level CHB based D-STATCOM, let N be the cascaded number, i.e. the number of H-bridges in CHB inverter, in this particular case N=2. Now, according to[77], the voltage (V_{dc}) required to be maintained in each capacitor of the H-bridge cell for proper operation given as,

$$V_{dc} = k\frac{V_g}{N} \tag{3.6}$$

Where, V_g is the rms value of grid voltage and k is the design parameter. The minimum value of K is $\sqrt{2}$ but, for optimal performance K ranges from the range 1.5 to 2.5.

3.3.1 Selection of interface inductor and DC capacitance

Based on the specific application, operating requirements, system configurations and control strategies, ratings of various components of system such as DC capacitor and inductance of coupling reactors have been selected.

The design of these components is based on the following assumptions:

1. The grid voltage is sinusoidal.
2. Grid side current distortion is assumed to be less than 5% after compensation with D-STATCOM having integrated shunt APF capability.
3. Fixed capability of reactive power compensation of D-STATCOM.
4. Modulation scheme for the CHB inverter is assumed to operate in the linear modulation mode.
5. The coupling inductor resistance, R is neglected.

3.3.1.1 Selection of DC Capacitors

The energy exchange (Δe) in joules between each H-bridge cell of D-STATCOM and load can be expressed as,

$$\Delta e = \frac{1}{2}C_{dc,i}\left(V_{c\max}^2 - V_{c\min}^2\right) \tag{3.7}$$

Where $C_{dc,i}$ is the DC-link capacitor of i^{th} H-bridge cell

Where $V_{c\max}$ and $V_{c\min}$ (in volts) are the maximum and minimum capacitor voltages, respectively. From the principle of energy transformation eq. (3.7) can be written as[22], [78]:

$$\frac{1}{2}C_{dc,i}\left(V_{ref,i}^2 - V_{dc,\min}^2\right) = V(aI)t \tag{3.8}$$

In eq.(3.8),

$C_{dc,i} =$ Capacitance of the capacitor of each H-bridge cell (in farads),

$V_{dc,Min} =$ Minimum voltage level of the DC bus voltage of H-bridge cell,

$V =$ AC voltage of the each H-bridge cell (in rms) $= \frac{V_g}{2}$,

$I =$ Rated current of D-STATCOM,

$t =$ Response time of the D-STATCOM,

$a =$ Over loading factor.

Considering $V_{dc,\min} = 1200V$ (considering 4% ripple in DC capacitor voltages), $V = \frac{1200}{2}V = 600V$, $I = 83.33A$, t = 300 μsec, and $a = 1.2$, the calculated value of $C_{dc,i}$ is 293 μF.

3.3.1.2 Selection of Coupling Inductor

D-STATCOM generates undesirable current harmonics around the switching frequency and its multiples. If the switching frequency of the PWM based D-STATCOM is sufficiently high, these undesirable current harmonics can be easily filtered out by the coupling inductor[79]. The filter inductor (L_c) is one of the key components which determine the performance of the D-STATCOM. The connection of the coupling inductor to the PCC point is shown in Figure 3.1.The selection of the AC inductance depends on the current ripple $i_{c,(P-P)}$ and switching frequency of the CHB inverter, f_{sw}. The approximate value of the ac inductance is given as[22]:

$$L_{inv} = \frac{m_a V_C}{12af_{sw}i_{c,(p-p)}} \tag{3.9}$$

Considering 5% peak-to-peak current ripple $i_{c,(P-P)}$ to be 2.5 A (rms), the switching frequency of the CHB inverter $f_{sw} = 2Nf_{cr} = 2 \times 2 \times 2$ kHz = 8 kHz, amplitude modulation index m_a=1, phase output voltage of the D-STATCOM *Vc*=2500V and overload factor a=1.2, the value is calculated to be 8.6 mH. For a better harmonic cancellation and reactive power compensation a higher value

of inductance is preferable. However, on the other hand, a very high value of inductance will result in slow dynamic response of the D-STATCOM and it would not be possible to compensate some of the load harmonics.

3.4 Control scheme for load compensation

In general, the current drawn by load from the source can be divided into following three parts,

i_{Lp} : Active Power Component

i_{Lq} : Reactive Power Component

i_{Lh} : Harmonic Component

The reference current generator has the task of calculating these components of current that has to be generated by the D-STATCOM. The grid voltage (v_{sa}), DC-link capacitor voltages (v_{c1},v_{c2}), and load current (i_L) are measured to obtain reference compensating current (i_{ref}). One of the key points for proper estimation of (i_{ref}) is to use a reliable estimation method. The original 1-ϕ pq theory[80], [81] is discussed for estimating the reference compensating current (i_{ref}). The instantaneous pq theory is one of the well accepted theories for the estimation of reference compensating current for D-STATCOM. The 1-ϕ pq theory is based on a set of instantaneous powers defined in the time domain.

Let the 1-ϕ grid voltage be given as,

$$V_g = V_m \sin \omega t \tag{3.10}$$

and the non-linear load current drawn at point of common coupling (PCC) is given as,

$$i_{_L} = \sum i_{Ln} \sin\left((n\omega t) + \phi_g\right) \tag{3.11}$$

The 1-ϕ pq theory starts with the transformation of source voltage and currents into $\alpha\beta$ – stationary reference frame. The 1-ϕ grid voltage and load current representation in $\alpha\beta$ – coordinates with a $\pi / 2$ lead is given by,

$$\begin{bmatrix} v_{g\alpha}(\omega t) \\ v_{g\beta}(\omega t) \end{bmatrix} = \begin{bmatrix} v_g(\omega t) \\ v_g\left(\omega t + \frac{\pi}{2}\right) \end{bmatrix} \tag{3.12}$$

$$\begin{bmatrix} i_{L\alpha}(\omega t) \\ i_{L\beta}(\omega t) \end{bmatrix} = \begin{bmatrix} i_L(\omega t + \phi_g) \\ i_L\left(\omega t + \phi_g + \frac{\pi}{2}\right) \end{bmatrix} \tag{3.13}$$

The instantaneous active power (p) and the instantaneous reactive power (q) are defined from instantaneous grid voltages and load currents on the $\alpha\beta-$axes as,

$$p_L(\omega t) = v_{g\alpha}(\omega t) i_{L\alpha}(\omega t) + v_{g\beta}(\omega t) i_{L\beta}(\omega t) \tag{3.14}$$

$$q_L(\omega t) = -v_{g\beta}(\omega t) i_{L\alpha}(\omega t) + v_{g\alpha}(\omega t) i_{L\beta}(\omega t) \tag{3.15}$$

Equations (3.14) and (3.15) can be written in matrix form as,

$$\begin{bmatrix} p_L(\omega t) \\ q_L(\omega t) \end{bmatrix} = \begin{bmatrix} v_{g\alpha}(\omega t) & v_{g\beta}(\omega t) \\ -v_{g\beta}(\omega t) & v_{g\alpha}(\omega t) \end{bmatrix} \begin{bmatrix} i_{L\alpha}(\omega t) \\ i_{L\beta}(\omega t) \end{bmatrix} \tag{3.16}$$

The Instantaneous active (p) and reactive (q) powers can be decomposed into an average (DC) and an oscillatory component (AC) as,

$$p_L(\omega t) = \bar{p}(\omega t) + \tilde{p}(\omega t) \tag{3.17}$$

$$q_L(\omega t) = \bar{q}(\omega t) + q(\omega t) \tag{3.18}$$

The above power components can be defined as,

$\bar{p}(\omega t) =$ DC component of the instantaneous power $p(\omega t)$, which is related to the conventional fundamental active current.

$\tilde{p}(\omega t) =$ AC component of the instantaneous power $p(\omega t)$ having zero average value, which is related to the harmonic currents caused by the AC component of the instantaneous real power.

$\bar{q}(\omega t) =$ DC component of the imaginary instantaneous power $q(\omega t)$, which is related to the reactive power generated by the fundamental components of voltages and currents.

$\tilde{q}(\omega t) =$ AC component of the instantaneous imaginary power $q(\omega t)$, which is related to the harmonic currents caused by the AC component of instantaneous reactive power.

Once the calculated real and reactive powers of the load are separated into their average and oscillating parts, the undesired portions of the real and imaginary powers of the load that should be compensated by D-STATCOM can be selected.

Let p_C and q_C be the powers to be generated by the D-STATCOM to compensate the harmonic and reactive power of the load, then the compensating currents can be calculated in αβ reference frame as,

$$\begin{bmatrix} i^*_{C\alpha}(\omega t) \\ i^*_{C\beta}(\omega t) \end{bmatrix} = \begin{bmatrix} v_{g\alpha}(\omega t) & v_{g\beta}(\omega t) \\ v_{g\beta}(\omega t) & -v_{g\alpha}(\omega t) \end{bmatrix}^{-1} \begin{bmatrix} p_C(\omega t) \\ q_C(\omega t) \end{bmatrix} \tag{3.19}$$

As the D-STATCOM has to absorb small amount of active power to meet losses as well as to supply the reactive power demand by the load, hence the above eq. (3.19)can be expressed as,

$$\begin{bmatrix} i^*_{C\alpha} \\ i^*_{C\beta} \end{bmatrix} = \frac{1}{v^2_{g\alpha} + v^2_{g\beta}} \begin{bmatrix} v_{g\alpha} & v_{g\beta} \\ v_{g\beta} & -v_{g\alpha} \end{bmatrix} \begin{bmatrix} -\tilde{p} + p_{loss} \\ -q_L \end{bmatrix} \tag{3.20}$$

Therefore, the reference current for D-STATCOM in the single phase system with unity power factor requirement is,

$$i^*_{C\alpha} = \frac{1}{v^2_{g\alpha} + v^2_{g\beta}} \left[-v_{g\alpha} \cdot \tilde{p} + v_{g\alpha} \cdot p_{loss} - v_{g\beta} \cdot q_L \right] \tag{3.21}$$

the term p_{loss} represents the total amount of active power absorbed from grid to meet the losses in the inverter. The reference current for D-STATCOM given by eq.(3.21) is dependent on the source voltage. If the source voltage is distorted then it will affect the compensation characteristics. Alternatively a modified 1-ϕ pq theory[82], a PLL is for distorted source voltage, the output of the PLL is $V_m sin(\omega t)$ and $V_m cos(\omega t)$ corresponding to the distorted source voltage.

$$\begin{bmatrix} v_{g\alpha}(\omega t) \\ v_{g\beta}(\omega t) \end{bmatrix} = \begin{bmatrix} V_m \sin(\omega t) \\ V_m \cos(\omega t) \end{bmatrix} \tag{3.22}$$

The voltages obtained from PLL is given by eq.(3.22), these voltage are substituted in eq.(3.20) ,the resultant reference current by modified 1-ϕ pq theory is given by eq.(3.23)

$$i^*_{C\alpha} = \frac{1}{V_m} \left[-\sin(\omega t) \cdot \tilde{p} + \sin(\omega t) \cdot p_{loss} - \cos(\omega t) \cdot q_L \right] \tag{3.23}$$

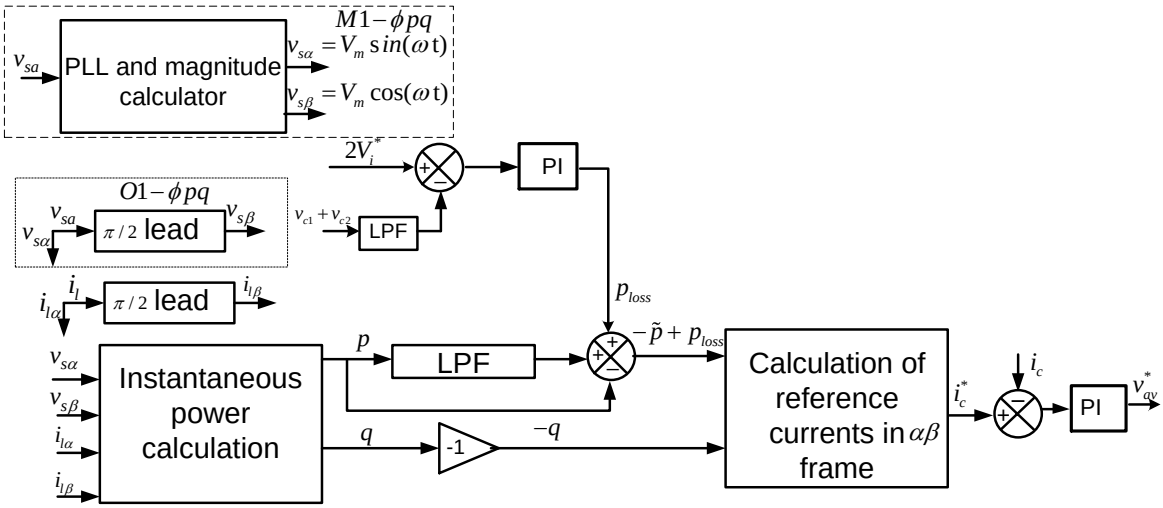


Figure 3.3 Block diagram of single phase D-STATCOM for harmonic and reactive power compensation.

The control theory's so far discussed in this section for generation of reference current for D-STATCOM, to compensate the load harmonics and reactive power required is presented in the block diagram of Figure 3.3. The two control theories with original single phase pq and modified single phase pq theorys are shown in this Figure. The active voltage superposition method is used at the end to generate the modulating signals. The main control loop generates a voltage v_{av}^* if this signal is given as a modulating signal to the H-brides then the capacitor voltage may deviate from reference. The reason is that the active power generated with the average signal to the H-bridge may not be the desired active power for that H-bridge. In this situation in order to modify the modulating signal the authors [75] have proposed this active voltage superposition (AVS) method. In this method the average modulating signal for H1-bridge is changed to new location in the direction of compensating current and a independent modulating signal for each H-bridge is generated. The phasor diagram to modify the modulating signal for H1-bridge is shown in Figure 3.4(a) and its implementation is shown in the Figure 3.4(b).

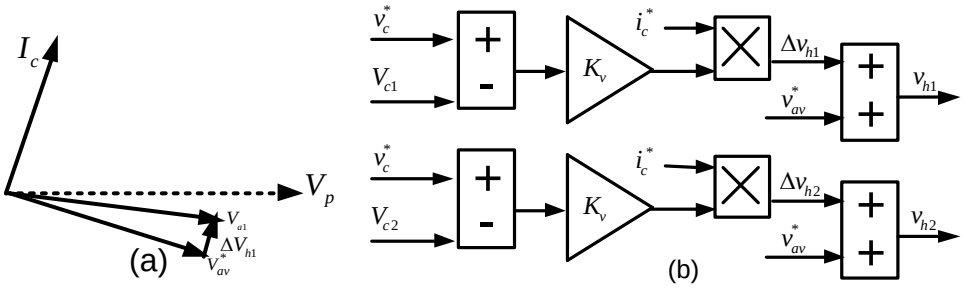


Figure 3.4 Phasor diagram for active voltage superposition for H1-bridge (b) implementation of AVS method.

3.5 Simulation results of single phase D-STATCOM for load compensation

The control theories so far discussed in the above section are used to study the compensation characteristics for single phase CHB D-STATCOM with both linear and nonlinear load for non-sinusoidal grid voltage. The entire system along with control theories are modelled in MATLAB/Simulink. The distorted grid voltage which is the input voltage considered for simulation is shown in Figure 3.5 with a THD of 9.34%. The system parameters used in the simulation study are given in Table 3-1.

Table 3-1 System parameters for simulation study

Parameter	**Value**
Single phase AC line voltage	1.2 kV, 50 Hz
Source impedance	R_s = 0.1 Ω, L_s = 0.1 mH
Coupling inductor of D-STATCOM	L_c = 8.6 mH
DC bus reference voltage	1250 V (for each capacitor in the H-bridge cell)
DC bus capacitance	330 uF (for each capacitor in the H-bridge cell)
Carrier frequency	2 kHz
PI controller parameters	For DC voltage controller: K_p = 0.08, K_i = 0.1
Load	Single-phase uncontrolled rectifier, R_{dc} = 40 Ω, L_{dc} = 50 mH; Linear load (R=5 Ω, L=34 mH).

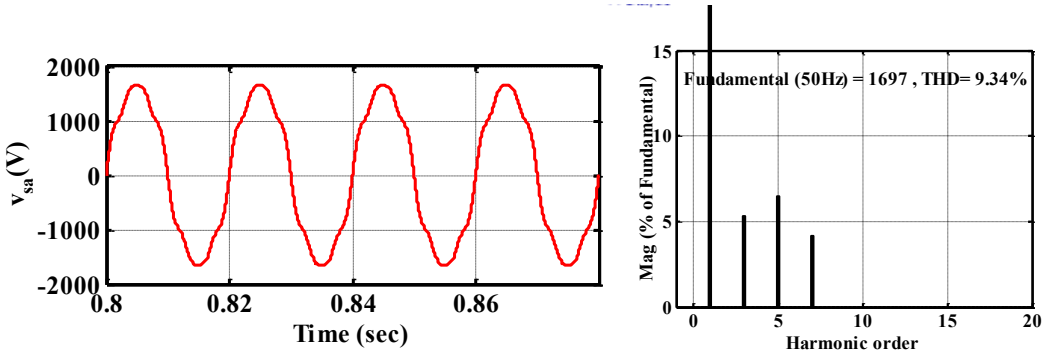


Figure 3.5 Source voltage waveform and its THD.

3.5.1 Linear RL load

Figure 3.5 shows the source voltage waveform and its harmonic spectrum having a THD of 9.34% while Figure 3.6 shows the load current waveform and its harmonic spectrum with a THD of 2.43%. The THD in linear load is arise because of the distortion in supply voltage.

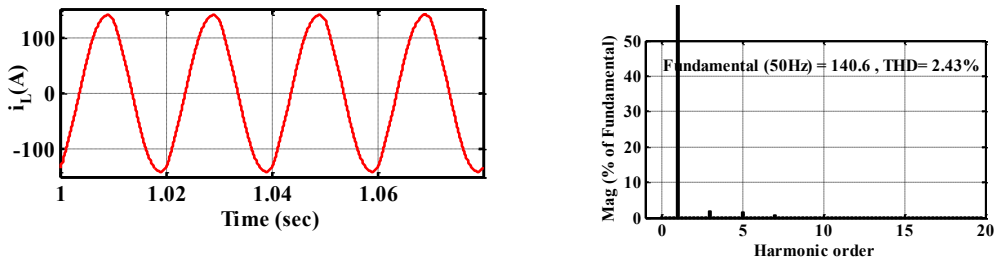


Figure 3.6 Linear load current waveform and its THD.

Figure 3.7(a) and all the subsequent figures in this section shows the similar simulation waveforms, the quantities shown (from top to bottom) as follows:

Trace 1: source phase voltage (v_{Sa}),

Trace 2: load current (i_L),

Trace 3: D-STACOM current (i_C),

Trace 4: source current (i_S),

Trace 5: downscaled source voltage and current of phase-a, and

Trace 6: total dc link voltage(v_{totdc}).

From the Figure 3.7 and Figure 3.8 the following observations are made

1. The THD of the source current for original pq theory is 7.36% and that of the modified pq theory is 1.42%

2. The reason can be seen in the calculation of instantaneous active and reactive powers with original pq theory, the instantaneous source voltage and load currents are taken, the source voltage harmonics along with load current harmonics leads to the oscillating power. The D-STATCOM is operated to cancel this oscillating powers. The reference D-STACOM currents is seen in Figure 3.7(d) can be observed to have distortion.
3. After compensation with D-STATCOM, the source current is in phase with the source voltage and confirms the compensation of reactive power. The power factor and input displacement factor is close to unity in both of the cases.
4. The rms value of the load current is 99.4A and that of the source current 42.94A, 42.71A with original and modified pq theories. The reduction in the source current is due to the compensation of reactive power of the load.
5. The regulation of the capacitor voltages is carried at the DC voltage controller. The total dc voltage is 2500V and it is having a second harmonic ripple which can be clearly seen in both the figures having a ripple voltage of 10V.

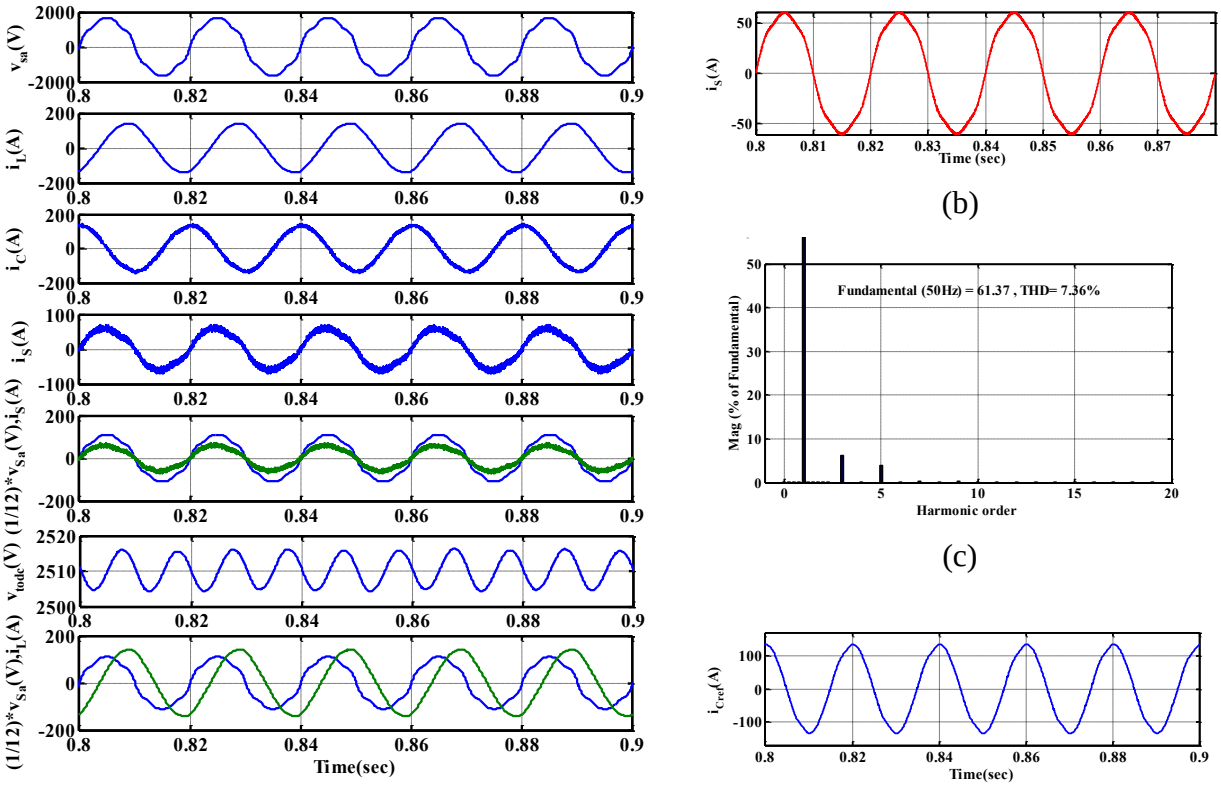
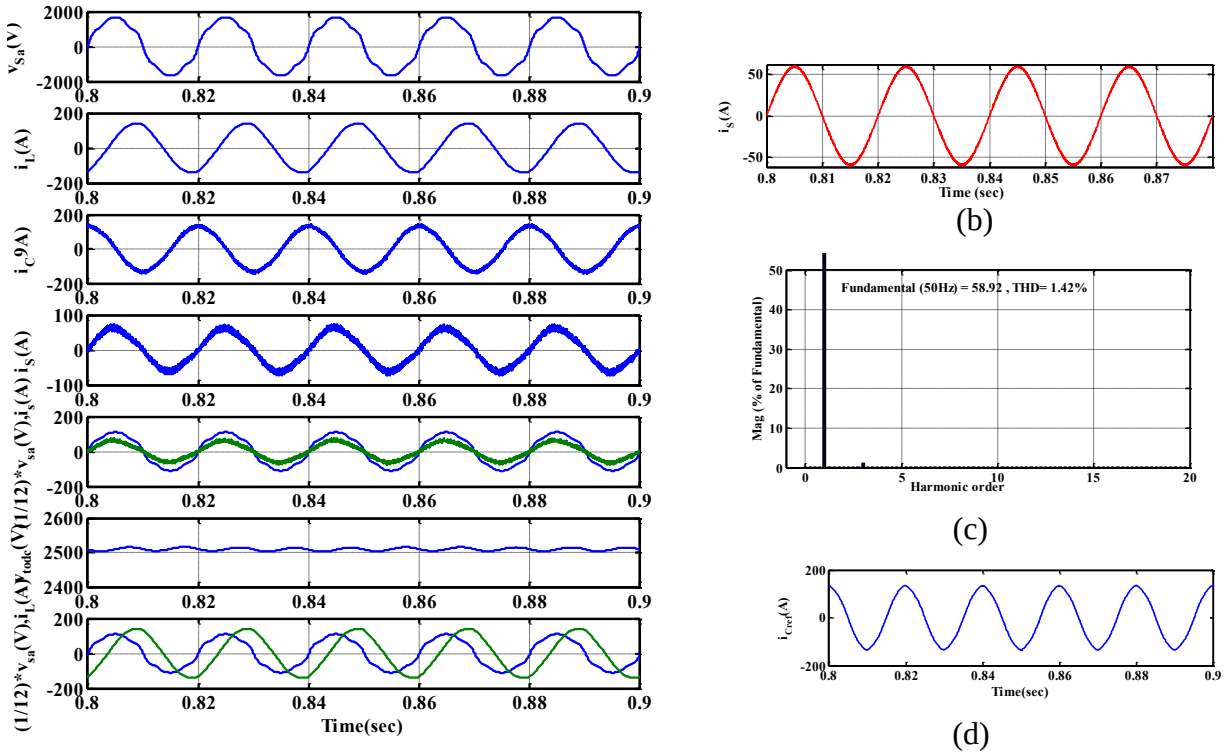


Figure 3.7 Performance of D-STATCOM for linear load using original pq theory.



(a) (b) (c) (d)

Figure 3.8 Performance of D-STATCOM for linear load using modified pq theory.

3.5.2 Uncontrolled rectifier load

A 1-phase uncontrolled rectifier with RL element at the dc side has been considered as a non-linear load in this case. Figure 3.10 and Figure 3.11 shows the simulated waveforms with original and modified pq theories respectively. Figure 3.5 shows the source voltage waveform and its harmonic spectrum having a THD of 9.34% while Figure 3.9 shows the load current waveform and its harmonic spectrum with a THD of 16.23%. In order to compensate this nonlinear current having a THD of 16.23% and also with supply voltage distortion the single phase five level CHB D-STATCOM is used as a compensator in this situation. The original and modified pq theories are used to generate the reference compensating currents. From the Figure 3.10 and Figure 3.11 the following observations are made

1. The THD of the source current with original pq theory is 6.61% and that of the modified pq theory is 3.6%
2. The reason can be seen in the calculation of instantaneous active and reactive power by original pq theory, the instantaneous source voltage and load currents are taken the source voltage harmonics along with load current harmonics leads to the oscillating powers the D-STATCOM is operated to cancel this oscillating powers. The reference D-STACOM currents seen in Figure 3.10(d) can be observed to have this distortion

3. After compensation with D-STATCOM, the source current is in phase with the source voltage and confirms the compensation of reactive power. The power factor and input displacement factor is close to unity in both of the cases.
4. The regulation of the capacitor voltages can be done by the DC voltage controller. The total dc voltage is 2500V and having a second harmonic ripple which can be clearly seen in both the figures having a ripple voltage of 30V

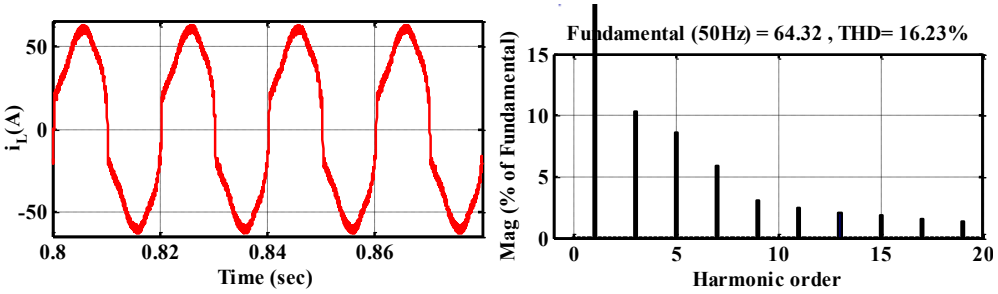


Figure 3.9 Non-linear load current waform and its THD.

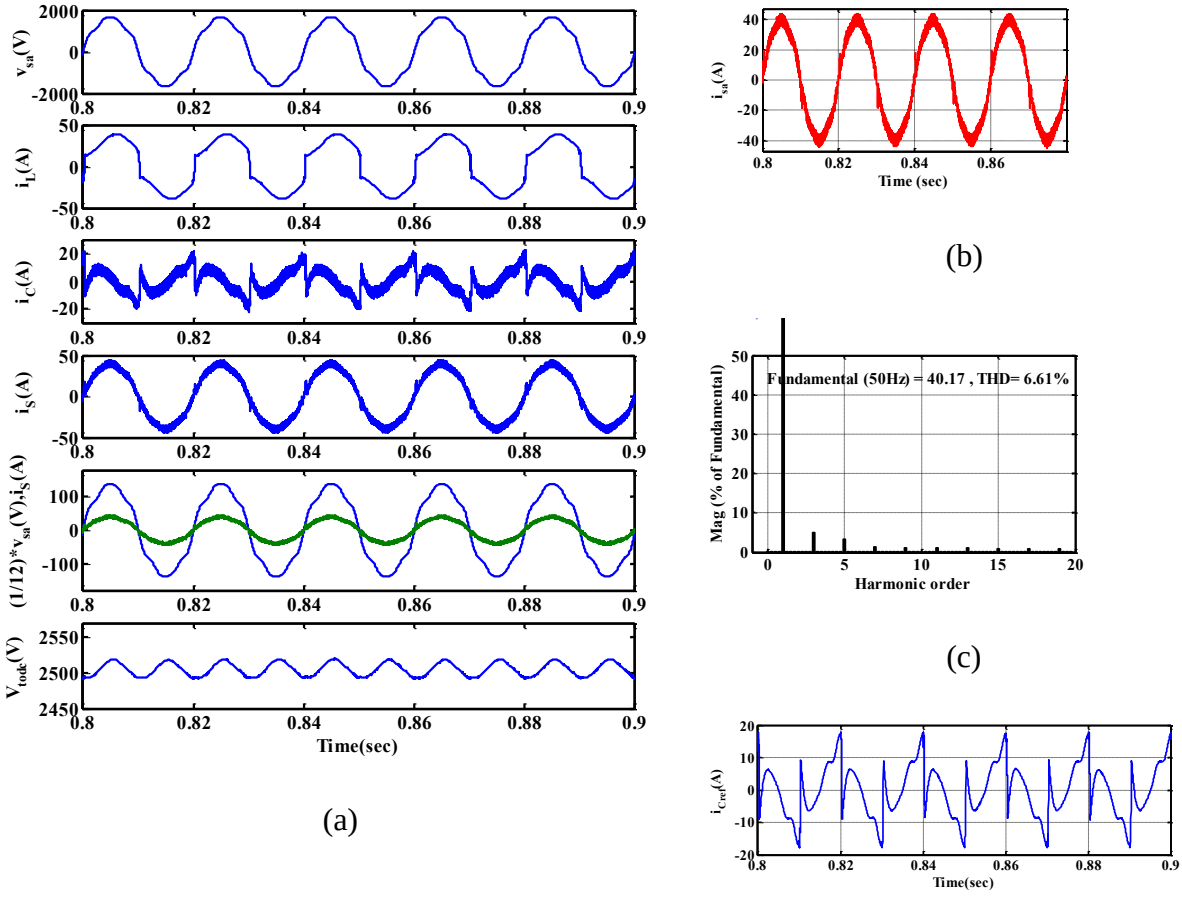
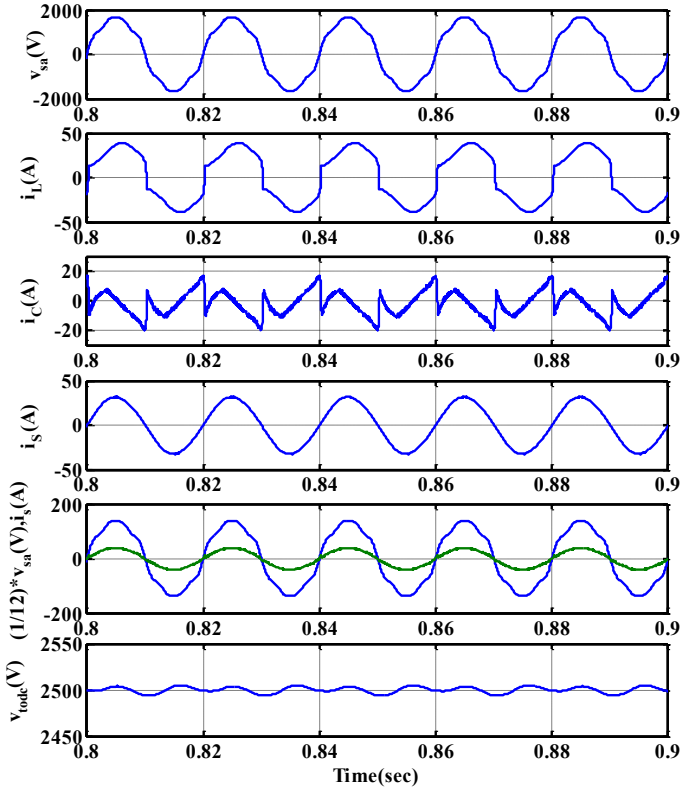
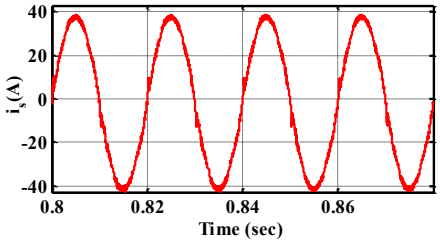


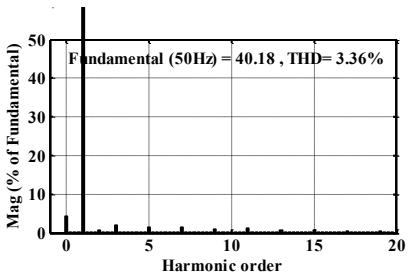
Figure 3.10 Performance of D-STATCOM for nonlinear load using original pq theory.



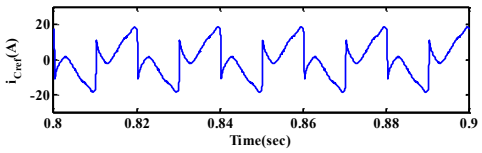
(a)



(b)



(c)



(d)

Figure 3.11 Performance of D-STATCOM for non-linear load using modified pq theory.

3.5.3 Comparison of performance of D-STACOM with load

Table 3-2 THD comparison for different control theories.

Control theory	Linear RL Load			Non-Linear Load		
	v_S THD%	i_L THD%	i_S THD%	v_S THD%	i_L THD%	i_S THD%
Original pq theory	9.34	2.43	7.36	9.34	16.23	6.61
Modified pq theory			1.42			3.36

Table 3-2 gives the summary for the performance of single phase D-STATCOM with different control theories. It is clear from this table that the modified pq theory gives improved results and

it is possible to achieve the source current THD much lower than the source voltage THD. So the modified pq theory should be used when the source voltage is non-sinusoidal.

3.6 Reactive Power Compensation Control scheme for D-STATCOM

The individual H-bridge active power can be calculated by a PI controller. The mathematical equations (3.4)-(3.5) decide the active power required by the individual H-bridge. The equations (3.24)-(3.25) are rewritten as the by introducing the variables shown in eq.(3.26), which are the equations of linear time invariant systems and can be used to calculate the active power of the H-bridges, PI controller can be used.

$$p_1 = C\frac{dg_1}{dt} + \frac{2g_1}{R_{L1}} \tag{3.24}$$

$$p_2 = C\frac{dg_2}{dt} + \frac{2g_2}{R_{L2}} \tag{3.25}$$

$$\left.\begin{aligned} g_1 &= \frac{V_{c1}^2}{2} \\ g_2 &= \frac{V_{c2}^2}{2} \end{aligned}\right\} \tag{3.26}$$

The main control loop comprises of active power computation block and current controller, which are shown in Figure 3.12. For the active power calculation, the square of the actual capacitor voltage is subtracted from the square of reference capacitor voltage and processed in a PI controller to determine the active power requirement of an H-bridge. The sum of two active power components is the total active power required by the D-STATCOM. Figure 3.12 shows the current controller in which the actual source current is subtracted from the reference source current and passed to a PI controller to get the reference D-STATCOM voltage. The source current reference consists of two components as shown in Figure 3.12 the total active current required by D-STATCOM is multiplied by sine template which is in phase with source voltage and the second component is the desired reactive current multiplied with the unit cosine component which is in quadrature with the source voltage[83]. The output of the current PI controller is the average modulating signal which is used in an auxiliary control loop to generate separate modulating signal generated for each H-bridges.

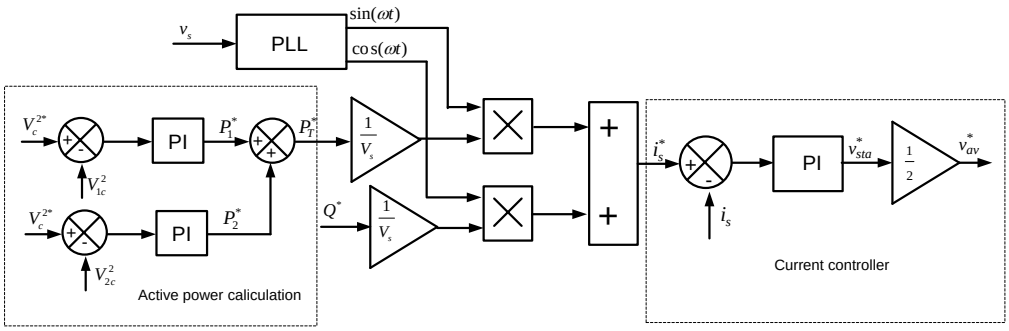


Figure 3.12 Active power calculation and Current controller.

3.7 DC capacitor voltage balancing

The aim of designing an auxiliary loop is to maintain the dc capacitor of each H-bridge at its reference value. The individual modulating signal for each H-bridge is generated by the auxiliary loop. The auxiliary control loop proposed i.e improved modulating signal method (IMS) is investigated and this method is compared to Active voltage superposition method (AVS). The procedure for development of two modulating signals for each H-bridge from the average modulating signal generated by the main control loop is described in this section while the AVS implementation is discussed in section 3.4.

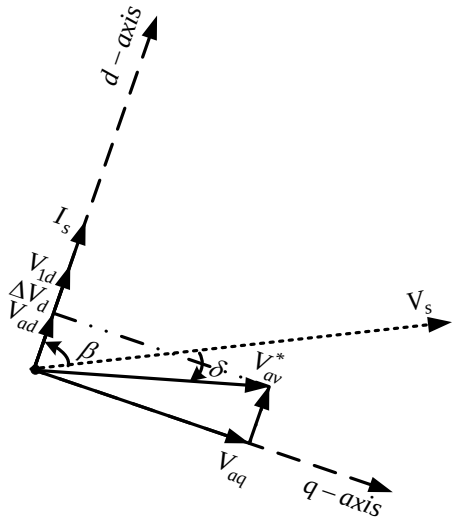


Figure 3.13 Phasor diagram with the average modulating signal.

The steady state operation of D-STATCOM is shown in the phasor diagram of Figure 3.13. This figure shows that source current is leading the source voltage and in order to consume the active power the average modulating signal should be lagging behind the source voltage. A reference frame is chosen in Figure 3.13 with the source current as the direction of reference, the d-axis is

in phase with the source current and q-axis is 90^0 lagging behind. The phase angle of source current and average modulating signal with respect to source voltage is further required to be determined. Fourier series analysis is used to calculate these phase angles. As shown in Figure 3.14, the source voltage PLL circuit gives sine and cosine template, which are used for calculation of Fourier coefficients for source current and average modulating signals. Finally, phase angles are found from these coefficients.

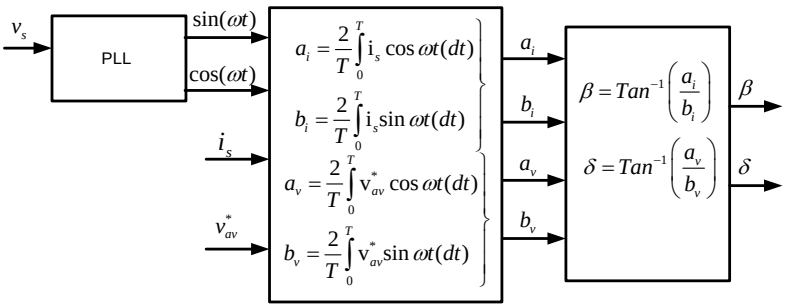


Figure 3.14 Calculation of phase angle of source current and average modulating signal.

The average modulating signal v_{av}^* is divided into d-axis and q-axis components V_{ad} and V_{aq} as given in eq.(3.27)

$$\left.\begin{aligned} V_{ad} &= V_{av}\cos\left(\beta+\delta\right) \\ V_{aq} &= V_{av}\sin\left(\beta+\delta\right) \end{aligned}\right\} \tag{3.27}$$

The average active and reactive powers are determined by eq.(3.28):

$$\left.\begin{aligned} P_{av} &= V_{ad} I_s \\ Q_{av} &= V_{aq} I_s \end{aligned}\right\} \tag{3.28}$$

To take care of unequal power loss in Two H- Bridges, change in d-axis voltage is calculated by eq. (3.29)

$$\Delta V_{1d} = \frac{P_1^* - \frac{P_T^*}{2}}{I_s} \tag{3.29}$$

The improved value of V_{1d} is then given by eq. (3.30)

$$\left.\begin{aligned} V_{1d} &= V_{ad} + \Delta V_{1d} \\ V_{1q} &= V_{aq} \end{aligned}\right\} \tag{3.30}$$

However, there is no change in q-axis voltage

The Figure 3.15(a) shows the phasor diagram for H1-bridge, the resultant modulating signal is shown i.e the addition of direct axis and quadrature axis voltage of H1 bridge. The Figure 3.15(a) shows that modulating signal of H1-bridge is lagging with source voltage, and the instantaneous modulating signal for H1-bridge can be found from eq.(3.31)

$$\left.\begin{aligned} V_1 &= \sqrt{\left(V_{1d}^2 + V_{aq}^2\right)} \\ \delta_1 &= \beta - \theta_1 = \beta - \tan^{-1}\left(\frac{V_{1d}}{V_{aq}}\right) \\ v_{a1} &= \sqrt{2}V_1 \sin\left(\omega t + \delta_1\right) \end{aligned}\right\} \tag{3.31}$$

To take care of unequal power loss in two H- Bridges, change in d-axis voltage for H2-bridge is calculated with eq. (3.32)

$$\Delta V_{2d} = \frac{P_2^* - \frac{P_T^*}{2}}{I_s} \tag{3.32}$$

The improved value of V_{2d} is then given by eq. (3.33)

$$\left.\begin{aligned} V_{2d} &= V_{ad} + \Delta V_{2d} \\ V_{2q} &= V_{aq} \end{aligned}\right\} \tag{3.33}$$

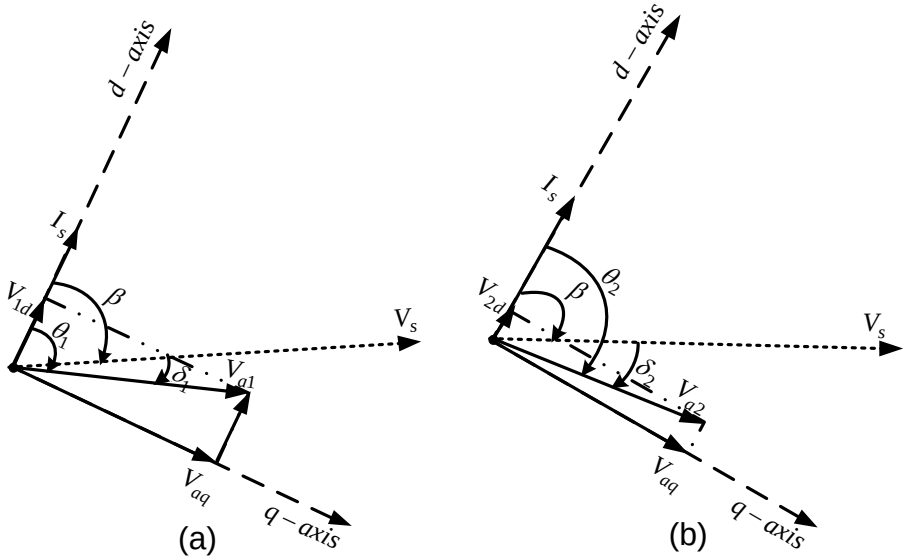


Figure 3.15 Phasor diagram for modulating the signal for (a) H1-bridge (b) H2-bridge.

The Figure 3.15(b) shows the modulating signal for H2-bridge, the resultant modulating signal is shown i.e the addition of direct axis and quadrature axis voltage of H2-bridge. The Figure 3.15(b) shows the modulating signal of H2-bridge is lagging with the source voltage, and the instantaneous modulating signal for H2-bridge can be found from eq.(3.34).

$$\left.\begin{aligned} V_2 &= \sqrt{\left(V_{2d}^2 + V_{aq}^2\right)} \\ \delta_2 &= \beta - \theta_2 = \beta - \tan^{-1}\left(\frac{V_{2d}}{V_{aq}}\right) \\ v_{a2} &= \sqrt{2}V_2 \sin\left(\omega t + \delta_2\right) \end{aligned}\right\} \tag{3.34}$$

3.8 Simulation results

The simulated performance of cascaded H-bridge D-STATCOM is presented while using IMS and AVS methods as discussed above. A five level-cascaded H-bridge converter is connected to a 1200V source with a coupling inductance of 8.6mH. The cascaded H-bridge converter, phase shifted pulse width modulation, and the control strategy is modeled in MATLAB-SIMULINK to obtain its performance, which is discussed below. Here in this section the reference reactive power of a D-STATCOM is chosen directly without considering the load.

3.8.1 Performance of D-STATCOM with average modulating signal:

Figure 3.16 shows the response of D-STATCOM, if both the H-bridges are driven by an average modulating signal generated from the main control loop. Here the results are in terms of source voltage and current, D-STATCOM output voltage, DC link cluster voltage, and individual DC capacitor voltages. The reference reactive power (leading) demand of D-STATCOM is set at 68 KVAR and the corresponding current has a peak value of 80 A. The reference DC capacitor voltage of each H-bridge is set at 1250V to meet above reactive power compensation.

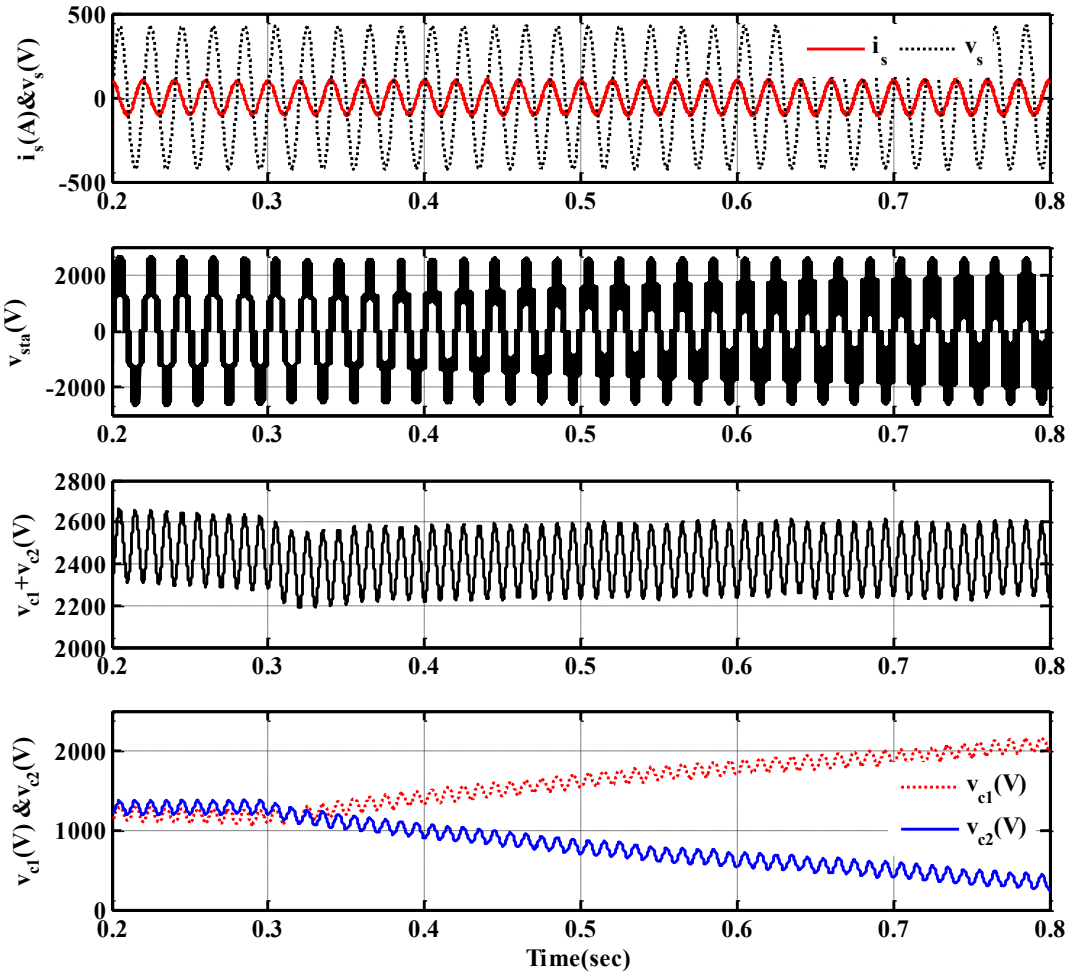


Figure 3.16 Response of D-STATCOM with the average modulating signal.

Initially, loss in each H-bridge is modeled in the form of equal resistances R_{L1}=R_{L2}=250Ω. At t=0.3 sec, the loss in H1-bridge is set at zero (R_{L1} =∞) while H2 bridge remains the same (R_{L2}=250Ω). The response in terms of source current, D-STATCOM output voltage, DC cluster voltage, and individual capacitor voltages is shown in Figure 3.16. The DC capacitor voltages start to change with V_{c1} in H1-bridge increasing and V_{c2} in H2-bridge decreasing linearly. In the meantime, the D-STATCOM output voltage is also seen to change from 5 level to 3 level. Even though the capacitor voltage V_{c1} and V_{c2} are changing, the DC cluster voltage i.e., the summation of DC capacitor voltages remain 2500 V. The overcharging of DC capacitor of H1-bridge can damage the switches.

3.8.2 Performance with improved modulating signal (IMS):

Error! Reference source not found. shows the source voltage and current, D-STATCOM output voltage, DC link cluster voltage, and individual DC capacitor voltages with improved modulating signal. The reference reactive power (leading) demand of D-STATCOM is set at 68

KVAR with peak reactive current of 80 A. The reference DC capacitor voltage of each H-bridge is again set at 1250V.

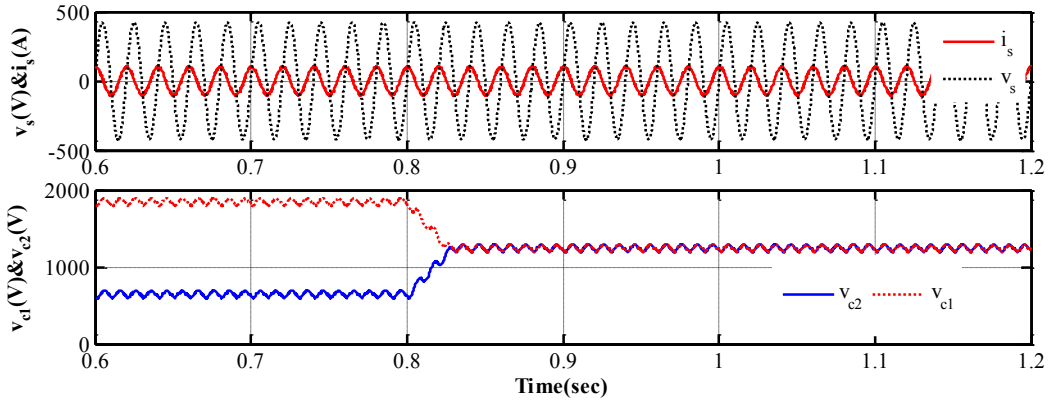


Figure 3.17 Response of D-STATCOM with the average and improved modulating signals.

The loss for H1-bridge is modeled with R_{L1} =250 Ω and for H2-bridge with R_{L2} =62.5 Ω. In the time interval upto 0.8sec because of unequal power loss, the DC capacitor voltage of H1-bridge and H2-bridge are deviated. At t=0.8 sec with the same situation of unequal losses, the auxiliary control loop (IMS) is activated and the DC capacitor voltages are now seen to converge at the DC reference voltage.

3.8.3 Performance with Active voltage superposition (AVS):

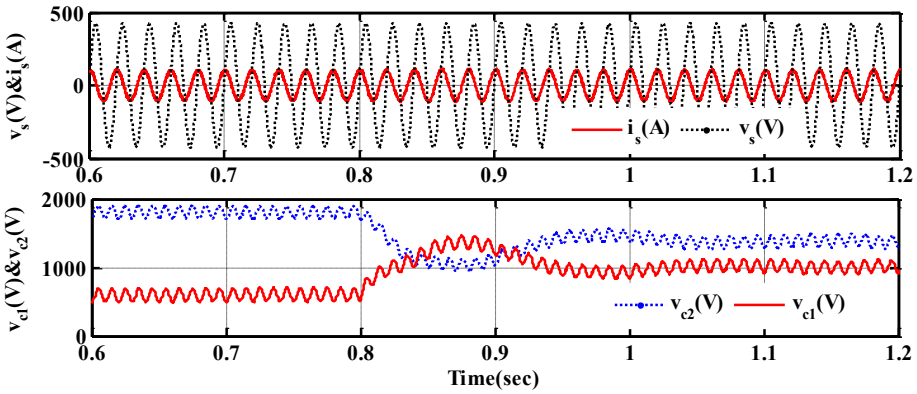


Figure 3.18 Response of D-STATCOM with active voltage superposition.

The Figure 3.18 shows the response of D-STATCOM with the active voltage superposition method where the source voltage, current and individual DC capacitor voltages waveforms have been shown. The reference reactive power (leading) is set at 68 KVAR with corresponding peak reactive current of 80 A. The reference DC capacitor voltage of each H-bridge is chosen as 1250V.

The loss for H1-bridge is modeled with R_{L1} =250 Ω and for H2-bridge with R_{L2} =62.5 Ω. Until t=0.8 sec, main control loop is active and it is observed that the capacitor voltages have large deviation in this interval. At t=0.8 sec, auxiliary control loop with active voltage superposition method is activated, it can be seen that the capacitor voltages start converging towards the reference with a steady state error.

3.8.4 Comparison of IMS and AVS methods:

The performance of these two methods namely IMS and AVS, for auxiliary control loop, is compared by varying the losses of the two H-bridges while the reference DC capacitor voltage is set at 1200 V. The steady state DC capacitor voltages under varying loss is simulated and the results are presented in the Table 3-3. When the active power loss is same for both the H-bridges then the DC capacitor voltage is same as the reference voltage even when the auxiliary control loop is not activated. However, with unequal power loss, the capacitor voltages are seen to have large difference under this condition. With introduction of auxiliary control loop, the capacitor voltages follow the reference value for IMS method where as for AVS method a steady state error of $\pm$100 V is present. Therefore, the proposed IMS method is seen to be capable of capacitor voltage balancing for wide range of loss variation in H bridges.

Table 3-3 Comparison of IMS and AVS methods.

Variation of active power loss on H-bridges by changing resistances [R_{L1}, R_{L2}]	Steady state Capacitor voltages of H-bridges in volts [v_{c1},v_{c2}]		
	With-out auxiliary loop	With auxiliary loop	
		Proposed IMS method	AVS method
[250Ω, 250Ω]	[1200,1200]	[1200,1200]	[1200,1200]
[250Ω, 62.5Ω]	[1800,600]	[1200,1200]	[1400,1000]
[250Ω, 125Ω]	[1450,950]	[1200,1200]	[1300,1100]
[250Ω, ∞]	[0, 2400]	[1200,1200]	[1100,1300]

3.9 Conclusion

The performance of D-STATCOM along with linear/nonlinear is studied with original and modified 1-ϕ pq control theories. The modified 1-ϕ pq theory produces much lower source current THD when compared to the source voltage THD. In cascaded H-bridge D-STATCOM, the difference in switching power loss in individual H-bridge is responsible for deviation of capacitor voltages. Under extreme conditions, when these losses differ too much, the AC output loses its multilevel character. The developed algorithm uses an auxiliary control loop, which employs improved modulating signals produced through combination of PLL and Fourier series. The effectiveness of improved modulating signals for two H-bridges is investigated with simulation studies. The proposed method is compared with the existing AVS method and found to give perfect capacitor voltage balancing even under extreme disparity in switching power loss.

CHAPTER 4: CASCADED H-BRIDGE BASED THREE PHASE D-STATCOM

[The design of a 2.2 KV, 1MVA transformer less SSBC based D-STATCOM for load balancing, harmonic elimination and reactive power compensation in 3P3W distribution system is presented in this chapter. The two current controller schemes namely PI and PI with resonant controllers are designed for SSBC based D-STATCOM. The capacitor balancing is also focussed. Exhaustive simulation results are presented to investigate the performance of D-STATCOM during transients and as well as in steady state for variety of loads.]

4.1 Introduction

The three-phase, three-wire (3P3W) distribution systems are normally used to deliver electrical supply for high-power loads such as adjustable speed drives, traction, arc furnaces, and other industrial applications. In these systems load unbalancing, harmonic and/or reactive current components contribute to the power quality problems in current waveform. For compensation of harmonics, load balancing and reactive power in these systems a 3P3W D-STATCOM is used. The complete compensator scheme of the D-STATCOM for 3P3W distribution system is shown in Figure 4.1. The D-STATCOM consists of two distinct main circuits: (a) PWM inverter; (b) D-STATCOM controller. The former one is responsible for power processing in synthesizing the compensating current that should be drawn from the power system and the later one is responsible for signal processing in determining the compensating reference currents in real-time and forcing the inverter to draw these currents from the system. The control algorithm implemented in the controller of the D-STATCOM determines its compensation characteristics. Detailed description of the controller for the D-STATCOM is given in the next section.

4.2 Control of D-STATCOM

The D-STATCOM controller consists of two functional control blocks:

1. Reference current generator
2. Current controller

The reference current generator has the task of detecting the harmonic and reactive currents which are to be compensated by the D-STATCOM. The source voltages, dc capacitor voltages, and load currents are measured to obtain these reference compensating currents. Once the

reference compensating currents are calculated, these currents are given as reference signals to the inner PWM current controller. The two current controllers are studied in this chapter namely PI and PI with resonant controller. The comparative study is carried out for choosing which current controller can reproduce accurately the compensating currents. The switching operation of the power electronics devices in the inverter automatically forces the D-STATCOM currents to follow the reference compensating currents. The detailed description for each controller is given below.

4.2.1 Reference current generator

One of the key points for proper implementation of a D-STATCOM is to use an appropriate method for current reference generation. Currently, there is a large variety of practical implementations supported by different theories, the performances of which are continuously debated while ever-better solutions are proposed. There are numerous published references that describe different algorithms used for simultaneous filtering of reactive power and harmonics[84]–[86]. The classification of the reference current detection methods can be done depending on the mathematical algorithms involved[84], [87], [88]. Thus, two approaches are described here: the frequency-domain and the time-domain harmonic detection methods. The frequency-domain methods mainly use Fourier analysis for calculating the reference currents as fast as possible with a reduced number of computations, which allows real-time implementation[84]. The commonly used frequency-domain methods are discrete Fourier transform (DFT) [89], recursive discrete Fourier transform (RDFT) [90]and fast Fourier transform (FFT)[91]. The common drawbacks of the Fourier analysis based harmonic detection methods are: proper design of the antialiasing filter, careful synchronization between sampling time and fundamental frequency of the inverter, large memory requirements to store the aquired samples, large computation burden on DSP, and imprecise results in transient conditions[84]. But on the other side, the time-domain methods offer increased speed, ease of implementation, and fewer calculations compared to the frequency-domain methods[84]. There are numerous time-domain approaches reported in the literature, and some of these are Fryze, Buchholz, and Depenbrock method[92]–[96], instantaneous symmetrical components based method[97], synchronous reference frame (SRF) theory[98], instantaneous reactive power (IRP) theory[99], fundamental load current algorithm[100], Adaline based control algorithm[85], Model reference adaptive control (MARC)[101], use of wavelet filtering for compensation of rapidly changing harmonics[102] and a scheme based on neural network techniques[103].

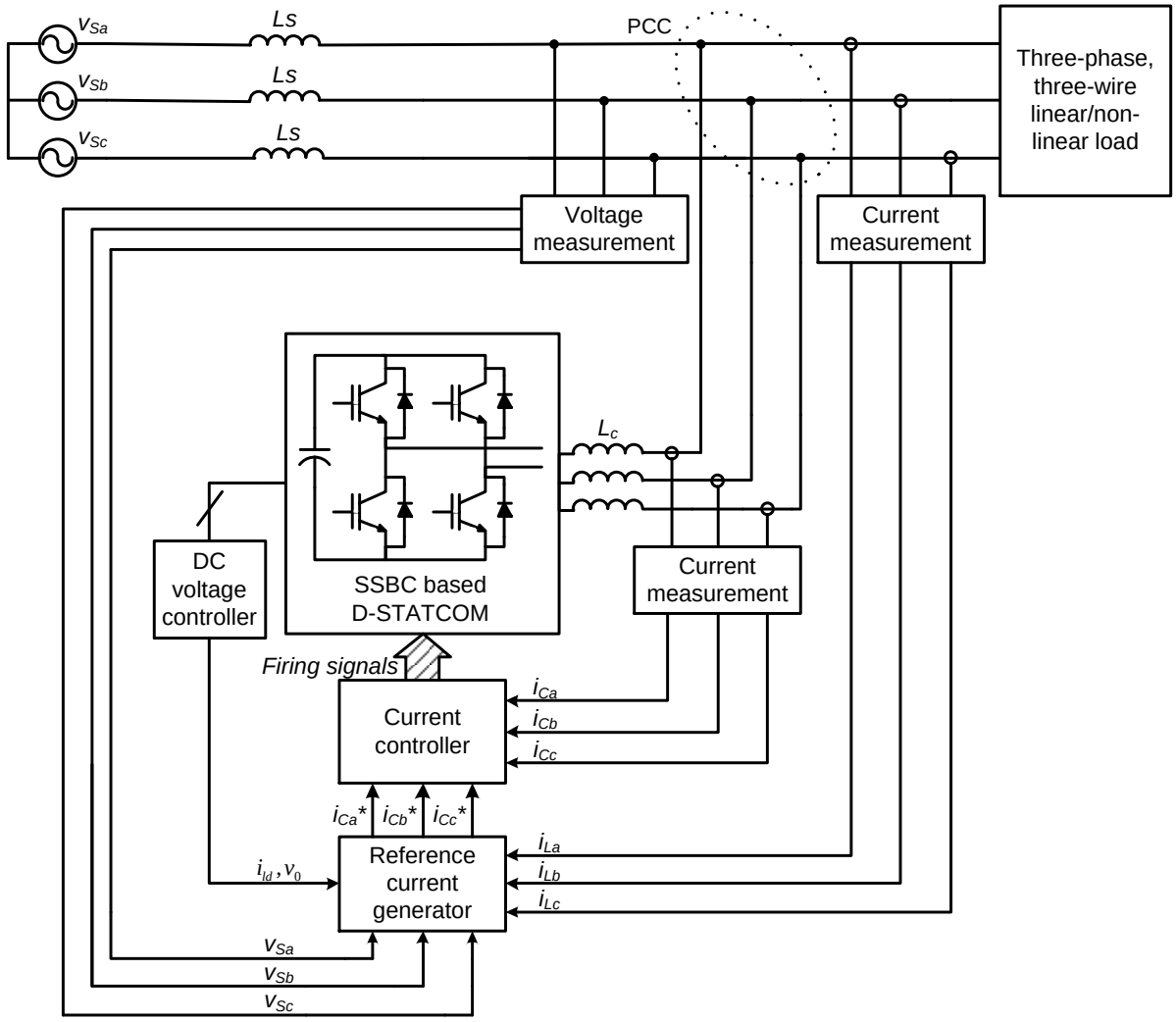


Figure 4.1 Schematic diagram of the 3P3W system with shunt connected D-STATCOM.

Among these control schemes, IRP and SRF theories are most widely used. However, in this thesis SRF theory is used because of its ease of implementation. The step-by-step procedure for implementing the SRF theory based reference current generator for D-STATCOM controller is given below.

4.2.1.1 Implementation of SRF theory

The synchronous reference frame (SRF) method of harmonic extraction is a more direct application of the coordinate transformation given by eq.(4.1). The three phase load currents are referred to a synchronously rotating reference frame. The transformation matrix is given by eq.(4.1) requires six sinusoidal signals which are locked with PCC voltage, at a fixed phase angle at every instant of time. Realization of this matrix requires a complex phase locked loop[104] (PLL) arrangement.

$$K_r = \sqrt{\frac{2}{3}}\begin{bmatrix} \cos(\omega_s t) & \cos(\omega_s t-(2\pi/3)) & \cos(\omega_s t+(2\pi/3)) \\ \sin(\omega_s t) & \sin(\omega_s t-(2\pi/3)) & \sin(\omega_s t+(2\pi/3)) \end{bmatrix} \tag{4.1}$$

If the load currents are of linear unbalanced in a three wire system as given by eq.(4.2) these currents are converted into the synchronous frame ($\omega = \omega_s$)with the help of the transformation matrix into the currents in dq frame are given by eq.(4.3). It is seen from eq.(4.3) that the fundamental positive sequence current can be observed as a dc quantity while the fundamental negative sequence current is observed as a harmonic oscillating with a frequency twice that of the supply frequency.

$$\left.\begin{aligned} i_{la} &= \sqrt{2}I_p\cos(\omega t+\delta_p)+\sqrt{2}I_n\cos(\omega t+\delta_n) \\ i_{lb} &= \sqrt{2}I_p\cos(\omega t+\delta_p-(2\pi/3))+\sqrt{2}I_n\cos(\omega t+\delta_n+(2\pi/3)) \\ i_{lc} &= \sqrt{2}I_p\cos(\omega t+\delta_p+(2\pi/3))+\sqrt{2}I_n\cos(\omega t+\delta_n-(2\pi/3)) \end{aligned}\right\} \tag{4.2}$$

$$\left.\begin{aligned} i_{ld} &= \sqrt{3}I_p\cos(\delta_p)+\sqrt{3}I_n\cos(2\omega t+\delta_n) \\ i_{lq} &= \sqrt{3}I_p\sin(\delta_p)+\sqrt{3}I_n\sin(2\omega t+\delta_n) \end{aligned}\right\} \tag{4.3}$$

The load current drawn by a six pulse thyristor controlled bridge rectifier (three phase) contains the fundamental, harmonics of the order (6n±1; n=1,2,3..). The (6n-1)th harmonics are of negative sequence type, whereas the (6n+1)th harmonics are of the positive sequence type. These line currents are given by eq.(4.4). These load currents are converted into synchronous frame, the resultant currents are given by eq.(4.5). It can be observed from eq.(4.5) that the fundamental current is a dc quantity while the harmonics of the order (6n±1; n=1,2,3..) are observed as a harmonic oscillating with a frequency $6n\omega$ (n=1,2,3..).

$$\left.\begin{aligned} i_{la} &= \sqrt{2}I_1\cos(\omega t+\alpha)+\sum_{n=1}^{\infty}\sqrt{2}I_n\cos((6n+1)\omega t+\delta_p)+\sum_{n=1}^{\infty}\sqrt{2}I_n\cos((6n-1)\omega t+\delta_n) \\ i_{lb} &= \sqrt{2}I_1\cos(\omega t+\alpha-(2\pi/3))+\sum_{n=1}^{\infty}\sqrt{2}I_n\cos((6n+1)\omega t+\delta_p-(2\pi/3))+\sum_{n=1}^{\infty}\sqrt{2}I_n\cos((6n-1)\omega t+\delta_n+(2\pi/3)) \\ i_{lc} &= \sqrt{2}I_1\cos(\omega t+\alpha+(2\pi/3))+\sum_{n=1}^{\infty}\sqrt{2}I_n\cos((6n+1)\omega t+\delta_p+(2\pi/3))+\sum_{n=1}^{\infty}\sqrt{2}I_n\cos((6n-1)\omega t+\delta_n-(2\pi/3)) \end{aligned}\right\} \tag{4.4}$$

$$\left.\begin{aligned} i_{ld} &= \sqrt{3}I_1\cos(\alpha)+\sum_{n=1}^{\infty}\sqrt{3}I_n\cos(6n\omega t+\delta_p)+\sum_{n=1}^{\infty}\sqrt{3}I_n\cos(6n\omega t+\delta_n) \\ i_{lq} &= \sqrt{3}I_1\sin(\alpha)+\sum_{n=1}^{\infty}\sqrt{3}I_n\sin(6n\omega t+\delta_p)+\sum_{n=1}^{\infty}\sqrt{3}I_n\sin(6n\omega t+\delta_n) \end{aligned}\right\} \tag{4.5}$$

In general each current in dq frame are having two parts the dc quantity and oscillating quantity given by eq.(4.6). Low pass filters acting on i_{ld},i_{lq} gives the dc components I_{ld},I_{lq} respectively. Subsequently I_{ld},I_{lq} are subtracted from i_{ld},i_{lq} to obtain oscillating components without any phase error. Once these components are separated the undesired portions of the load currents are chosen and these currents are compensated with D-STATCOM.

$$\left.\begin{aligned} i_{ld} &= I_{ld} + \tilde{i}_{ld} \\ i_{lq} &= I_{lq} + \tilde{i}_{lq} \end{aligned}\right\} \tag{4.6}$$

Simplification of transformation matrix given by eq.(4.1) is done by splitting the transformation into two steps.

In the first step eq.(4.7) is applied to transform the load currents to their stationary equivalents. Because of three wire there is no zero sequence components.

$$\begin{bmatrix} i_{l\alpha} \\ i_{l\beta} \end{bmatrix} = \sqrt{\frac{3}{2}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & -\sqrt{3}/2 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} \tag{4.7}$$

$$\begin{bmatrix} i_{ld} \\ i_{lq} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} i_{l\alpha} \\ i_{l\beta} \end{bmatrix} \tag{4.8}$$

In the next step this stationary variables are converted to their d-q equivalents using eq.(4.8). It can be seen that this transformation uses two basic signals $\sin(\omega t)$ and $\cos(\omega t)$. The complexity of the transformation matrix is greatly reduced.

4.2.1.2 Compensation for D-STATCOM losses

Ideally, there is no loss in the D-STATCOM circuit; therefore, there is no active power exchange between it and the power system and the capacitor voltages remain constant. However, in practice, the D-STATCOM has switching losses associated with the PWM operation of its semiconductor switches. If this energy is supplied by the dc link capacitor(s), the capacitors will gradually discharge and their voltages would progressively reduce thereby adversely affecting the performance of the D-STATCOM.

In order to maintain the dc link voltage at a constant value, a small amount of active current (i_{lossd}) must be drawn continuously from the system to supply switching and ohmic losses in the PWM inverter. This can be done by adding a dc voltage regulator to the control strategy. The dc

voltage controller has a task of determining the real component of the current to be drawn by the D-STATCOM to compensate for the power losses in the inverter thereby maintaining the voltages(s) of the capacitor(s) at their reference value. In dc voltage controller, the reference and the actual dc bus voltages are compared and the error is processed in a PI controller. The output of the PI controller gives the required active current for the compensation of losses in the D-STATCOM.

4.2.1.3 Calculation of reference D-STATCOM currents

The i_{cd}^{*}, i_{cq}^{*} are the reference D-STATCOM currents in synchronous (dq) frame. The D-STATCOM can be operated in different modes

1. Unity power factor mode (UPF): For compensation of reactive power along with the harmonics, the currents $\tilde{i}_{ld}$ and i_{lq} must be compensated as given in eq. (4.9) . This means that all the undesired current components of the load are being eliminated.

$$\left.\begin{aligned} i_{cd}^{*} &= -\left(\tilde{i}_{ld} + i_{lossd}\right) \\ i_{cq}^{*} &= -\left(i_{lq}\right) \end{aligned}\right\} \tag{4.9}$$

   The reason for including negative signs in the compensating powers is to emphasize the fact that the D-STATCOM should draw a compensating current that produces the exact negative of the undesirable powers drawn by the non-linear/reactive load. As a result, the compensated source current is sinusoidal, which produces a constant real power, and does not generate any reactive power. The combination of non-linear load and the D-STATCOM forms an ideal, linear, and purely resistive load. Hence, the source current has a minimum rms value that transfers the same energy as the original load current producing the average real power.
2. Harmonic elimination mode (HEM): For compensation of harmonics generated by the non-linear load, the currents $\tilde{i}_{ld}$ and $\tilde{i}_{lq}$ must be compensated given by eq.(4.10). This means that the harmonic currents of the non-linear load are eliminated.

$$\left.\begin{aligned} i_{cd}^{*} &= -\left(\tilde{i}_{ld} + i_{lossd}\right) \\ i_{cq}^{*} &= -\left(\tilde{i}_{lq}\right) \end{aligned}\right\} \tag{4.10}$$

This kind of compensation is applicable when harmonic elimination is the most important issue. The resulting power drawn from the source is the average real power and reactive power in this mode.

3. Zero voltage regulation mode (ZVR): The amplitude of AC terminal voltage at PCC is controlled to its reference voltage V_p* using the PI voltage controller. The output of the PI voltage controller is considered as the reactive current i_{pq} for zero voltage regulation at PCC. In this control mode of operation the AC voltage regulation at PCC can be controlled, harmonic elimination and load balancing can be achieved.

$$\left.\begin{aligned} i_{cd}^{*} &= -\left(\tilde{i}_{ld} + i_{lossd}\right) \\ i_{cq}^{*} &= -i_{lq} + i_{pq} \end{aligned}\right\} \tag{4.11}$$

Depending on the mode of operation the reference current for a D-STATCOM is chosen in the dq frame. The reference D-STATCOM currents in the abc frame can be found from the eq. (4.12) -(4.13).

$$\begin{bmatrix} i_{c\alpha}^{*} \\ i_{c\beta}^{*} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} i_{cd}^{*} \\ i_{cq}^{*} \end{bmatrix} \tag{4.12}$$

$$\begin{bmatrix} i_{ca}^{*} \\ i_{cb}^{*} \\ i_{cc}^{*} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & -\sqrt{3}/2 \\ -1/2 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{c\alpha}^{*} \\ i_{c\beta}^{*} \end{bmatrix} \tag{4.13}$$

4.3 Design of 2.2 KV 1 MVA Transformer less D-STATCOM for three phase-three wire system

The SSBC based PWM D-STATCOM for medium-voltage application has attracted the attention of power electronics researchers/engineers working in reactive power compensation and/or harmonic compensation. To design a voltage-source PWM inverter based D-STATCOM for medium or high-voltage system, the inverter must be equipped with a transformer for galvanic isolation and voltage matching between the industrial/utility distribution system voltage and the inverter voltage. However, weight and size of the transformer is more than 50% of the overall weight and size of the power converter[105]. To address this issue, a new type of transformer based on power electronics circuits has been presented in [61] for voltage transformation, galvanic isolation, and power quality enhancements. However, this method

requires additional power electronic circuits and adds to the cost of the converter. To alleviate this problem, the focus of this research is to design a SSBC based D-STATCOM without any line frequency transformer.

For design of SSBC based PWM D-STATCOM without any line frequency transformer, let N be the cascade number, i.e. the number of cascaded voltage source H-bridge converters in each phase. Now, according to [106], the voltage (V_{dc}) required to be maintained in each capacitor of the H-bridge cell for proper operation of D-STATCOM is given as,

$$V_{dc} = k\frac{V_S}{N\sqrt{3}} \tag{4.14}$$

where, V_s is the system voltage (line-to-line) and k is the design parameter.

The value of k should be properly selected as the performance of the D-STATCOM is highly dependend on it. The minimum value of k is $\sqrt{2}$ but, for optimal performance k is selected from the range 1.5 to 2.5[107].

4.3.1 Selection of interface inductor and DC capacitance

Based on the specific applications, operating requirements, system configurations and control strategies, ratings of various components of D-STATCOM such as dc capacitor and inductance of coupling reactors are selected[108][22].

The design of these components is based on the following assumptions:

1. The AC source voltage is balanced and sinusoidal.
2. AC side line current distortion is assumed to be less than 5% after compensation with D-STATCOM.
3. Fixed capability of reactive power compensation of D-STATCOM.
4. PWM inverter is assumed to operate in the linear modulation mode (i.e. $0 \leq m_a \leq 1$, m_a = amplitude modulation index).
5. The coupling inductor resistance R_c is neglected.

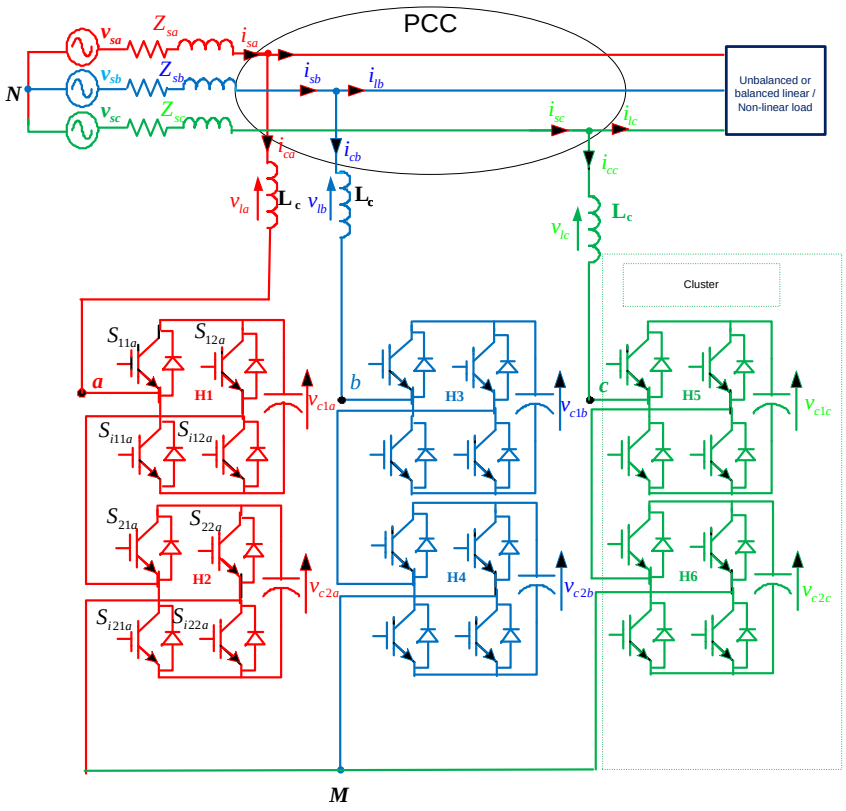


Figure 4.2 A five level SSBC based D-STATCOM.

4.3.1.1 Selection of DC capacitors

The capacitance of the capacitor *C* (in farads) gives its available energy *W* (in joules) as follows:

$$W = \frac{1}{2}C\left(V_{C\max}^2 - V_{C\min}^2\right) \tag{4.15}$$

Where V_{Cmax} and V_{Cmin} are (in volts) are the maximum and minimum capacitor voltages, respectively. From the principles of energy transformation eq. (4.15) can be written as[22][108]:

$$\frac{1}{2}C_{dc}\left(V_{ref,i}^2 - V_{dc,\min}^2\right) = V(al)t \tag{4.16}$$

$$C_{dc} = 2\frac{V(al)t}{\left(V_{ref,i}^2 - V_{dc,\min}^2\right)} \tag{4.17}$$

In eq. (4.17),

C_{dc} = Capacitance of the capacitor of each H-bridge cell (in farads),

$V_{dc,min}$ = Minimum voltage level of the dc bus voltage of H-bridge cell,

V = AC voltage of the each H-bridge cell (in rms) $= V_S \big/ \left(N\sqrt{3} \right)$,

I = Rated phase current of the converter,

t = Response time of the D-STATCOM [52, 55],

a = Over loading factor [52, 55].

Considering $V_{dc,min}$ = 1152 V (considering 4% ripple in dc capacitor voltages), $V = \dfrac{2.2 \times 10^3}{2 \times \sqrt{3}}$ V = 635 V, $I = \dfrac{1 \times 10^6}{\sqrt{3} \times 2.2 \times 10^3}$ A = 262.43 A, t = 0.03 msec, $V_{ref,i}$ =1200 V and a = 1.2, the calculated value of C_{dc} is 0.109 μF.

4.3.1.2 Selection of coupling inductor

PWM converters generate undesirable current harmonics around the switching frequency and its multiples. If the switching frequency of the PWM converter is sufficiently high, these undesirable current harmonics can be easily filtered out by the coupling inductor. The coupling inductor (L_c) is one of the key components which determine the performance of the D-STATCOM. The connection of the coupling inductor to the AC system is shown in Figure 4.2.

The selection of the ac inductance depends on the current ripple $i_{cr,(p-p)}$ and switching frequency of the converter (f_c). The approximate value of the ac inductance is given as[22]:

$$L_C = \frac{\sqrt{3} m_a V_c}{12 a f_c i_{cr,(p-p)}} \tag{4.18}$$

Here, switching frequency of the converter (f_c) depends on the PWM method used for controlling the converter. For carrier rotation based level-shifted PWM technique with carrier signal frequency f_{cr}, f_c can be calculated as:

$$f_c = 2Nf_{cr} \tag{4.19}$$

Considering 5% peak-to-peak current ripple $\left(i_{cr,(p-p)} \right)$ to be 2.6 A rms, the switching frequency of the converter ($2Nf_{cr}$) = 2 × 2 × 2 kHz = 8 kHz, amplitude modulation index (m_a) = 1, phase-to-neutral or cluster voltage of the inverter (V_c) = $N \times V_{ref,i}$ = 2.4 kV and overload factor (a) = 1.2, the value is calculated to be 14.5 mH.

4.3.2 Modelling of modular SSBC D-STATCOM

From Figure 4.2 the KVL voltage equations at the point of common coupling and the cascaded H-bridge converter is given by eq. (4.20). Applying the synchronous dq transformation[109] for eq.(4.20), the differential equations in this synchronous frame are given by eq.(4.21) Where R_c, L_c are leakage resistance, coupling inductances, ω is the speed of the rotation frame, v_{pd} , v_{pq} are the point of common coupling direct axis voltage and a quadrature component, v_{cd} , v_{cq} are the direct and quadrature component of the converter output voltage. The eq.(4.22) gives the dynamic response of the D-STATCOM currents with the inputs to the converter as v_{cd} , v_{cq} and outputs are i_{cd} , i_{cq} . In order to decouple the dq axis currents seperate controllers are to be used[110]. The eq.(4.21) is rearranged with eq.(4.23) with controller outputs are u_{cd} and u_{cq} . After getting the controller outputs, the D-STATCOM output voltage is determined by eq.(4.22) .The Figure 4.3 represents the current controlled D-STATCOM in synchronous d-q reference frame where the cross coupling terms are avoided by means of current controllers[111]–[113]. The current controller's output is a modulating voltage which is compared with the triangular carrier waves to generate firing pulse for the switches. The controller mentioned in the Figure 4.2 is realized with PI controller only[114] and PI with harmonic current controller.

$$\begin{bmatrix} v_{paN} - v_{aM} \\ v_{pbN} - v_{bM} \\ v_{pcN} - v_{cM} \end{bmatrix} = R_c \begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \end{bmatrix} + L_c \frac{d}{dt} \begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \end{bmatrix} \tag{4.20}$$

$$\begin{bmatrix} L_c \dfrac{di_{cd}}{dt} \\ L_c \dfrac{di_{cq}}{dt} \end{bmatrix} = \begin{bmatrix} -R_c & -\omega L_c \\ \omega L & -R_c \end{bmatrix} \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} + \begin{bmatrix} v_{pd} - v_{cd} \\ v_{pq} - v_{cq} \end{bmatrix} \tag{4.21}$$

$$\left.\begin{aligned} L_c \frac{di_{cd}}{dt} &= -R_c i_{cd} + u_{cd} \\ L_c \frac{di_{cq}}{dt} &= -R_c i_{cq} + u_{cq} \end{aligned}\right\} \tag{4.22}$$

$$\left.\begin{aligned} v_{cd} &= u_{cq} + \omega L_c i_{cq} + v_{pd} \\ v_{cq} &= u_{cq} - \omega L_c i_{cd} + v_{pq} \end{aligned}\right\} \tag{4.23}$$

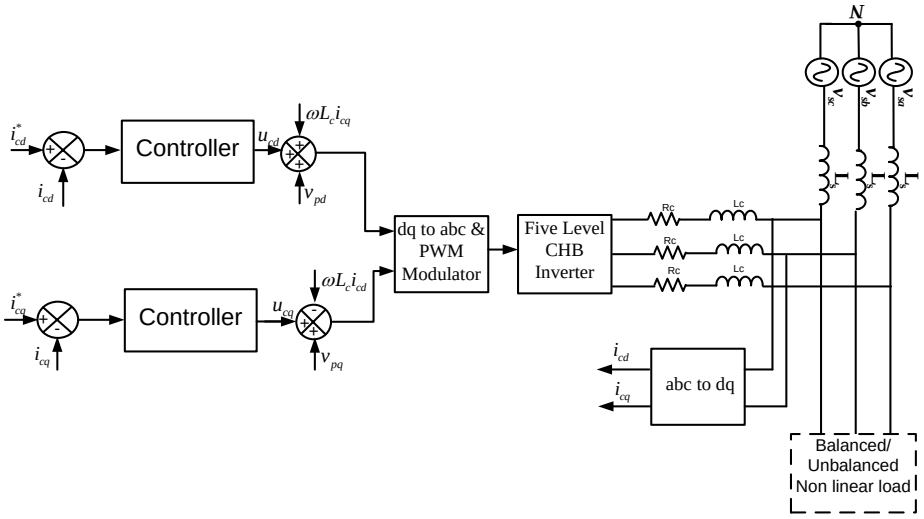


Figure 4.3 Modelling of current controlled D-STATCOM.

4.3.3 PI current controller

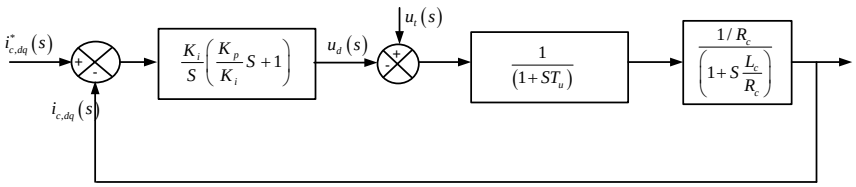


Figure 4.4 Block diagram representation for PI control.

To design PI controller, the system shown in Figure 4.3 is represented in the block diagram as shown in Figure 4.4. In Figure 4.4 each block is represented with the transfer function, PWM modulator is taken as a first order lag element and CHB is represented with unity block, up to the point of common coupling the first order plant transfer function is considered. If the PS-PWM is implemented practically with the digital signal processor in order to update the reference modulating signal and the carrier for a hold on period of switching signal the Tu=1/(4Nfsw) is used for all cell update method[115]. The open loop transfer function of the Figure 4.4 is given by eq.(4.24) and this transfer function having two finite poles, PWM modulator delay pole and plant pole. The pole-zero cancellation method is used to design the controller parameters. The dominant pole is the plant pole and this pole should by cancelled with controller zero in order to have the faster response speed. After the pole-zero cancellation, the resultant transfer function is given by eq .(4.25). The condition for pole-zero cancellation is given by eq.(4.26), which forms relation of controller parameters is framed. In order to find the absolute values of controller

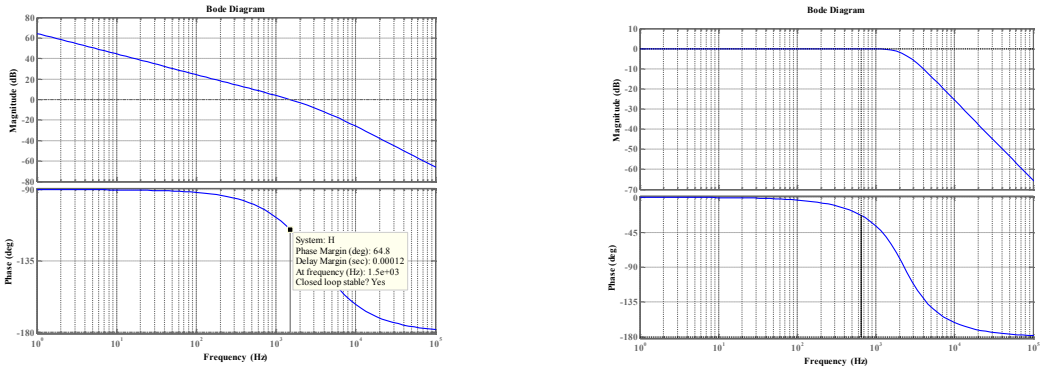
parameters, the bandwidth of the controller is to be fixed. The current controller is designed to compensate the highest harmonic current of the bridge rectifier non-linear load. The highest harmonic order to be processed is chosen as 19. The safety margin is also considered and the bandwidth is to be fixed here it is chosen as f_b (1500 Hz). At this bandwidth frequency the magnitude of the eq.(4.25) is to unity. Thus the controller parameters are found from eq.(4.27). With this controller parameters, the stability of the open loop transfer function is verified with the bode plot as shown in Figure 4.5 and closed loop bode plot is plotted in Figure 4.5 (b).

$$G_{opi} = \frac{K_i}{S}\left(\frac{K_p}{K_i}S+1\right)\left(\frac{1}{T_u S+1}\right)\left(\frac{1/R_c}{\frac{L_c}{R_c}S+1}\right) \tag{4.24}$$

$$G_{opi} = \frac{K_i}{R_c S}\left(\frac{1}{T_u S+1}\right) \tag{4.25}$$

$$\frac{K_p}{K_i} = \frac{L_c}{R_c} \tag{4.26}$$

$$\left.\begin{aligned} K_i &= 2\pi f_b R_c \sqrt{\left(2\pi f_b T_u\right)^2+1} \\ K_p &= \frac{L_c}{R_c} K_i \end{aligned}\right\} \tag{4.27}$$



(a) (b)

Figure 4.5 Bode plot of the (a) open loop (b) closed loop transfer function with PI controller.

Table 4-1 closed loop gain and phase for PI controller at harmonic order.

Harmonic order(n)	Harmonic frequency(Hz)	$\lvert G_{ck}(\omega)\rvert\lvert\underline{G_{ck}(\omega)}$
6	300	$1\lvert\underline{-9.97^0}$
12	600	$1\lvert\underline{-22^0}$
18	900	$1\lvert\underline{-30.5^0}$

The following observations can be made for the PI controller from Table 4-1;

1. Actual D-STATCOM current lags the reference current.
2. Magnitude of D-STATCOM current is equal to the reference current.

Ideally the controller has to be designed such that the actual D-STATCOM current should track its reference in magnitude and with zero phase lag.

4.3.4 PI with resonant current controller

The integral part of the PI controller goes to infinite for a dc variable such a characteristic leads to a desirable zero error for dc variables. However for AC variables there is no term in the PI controller that tends to infinite, so in order to achieve the zero error, for AC variables the resonant controller is used. The harmonic spectrum of bridge rectifier non-linear load contain in harmonic of order 5,7,11,13,17,19 in stationary reference frame are reflected as 6,6,12,12,18,18 harmonics respectively in dq frame rotating at fundamental speed. The fundamental positive sequence is observed as the dc quantities in dq frame rotating at fundamental speed. The PI controller is used for dc quantities. The resonant controllers in dq frame to implement for 6, 12, 18 means that the fundamental and harmonic order upto 19 can efficiently track the reference compensation currents. The block diagram of PI control and the unbalanced harmonic current controller is given in Figure 4.6. The PI controller parameters are found from using eq.(4.27). The gain of the resonant controller is chosen to be sufficiently high such that at the corresponding frequency it introduces a high magnitude such that the error at this frequency is zero. By considering the controller parameters and the resonant controller gain the stability of the open loop transfer function is verified with bode plot and it is shown in Figure 4.7(a) and closed loop bode plot is plotted in Figure 4.7(b).

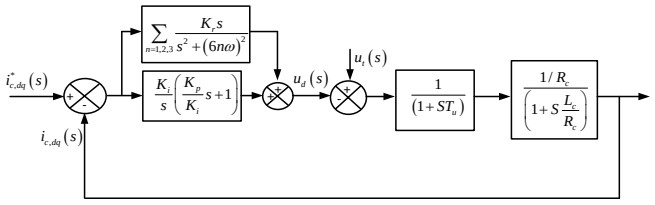
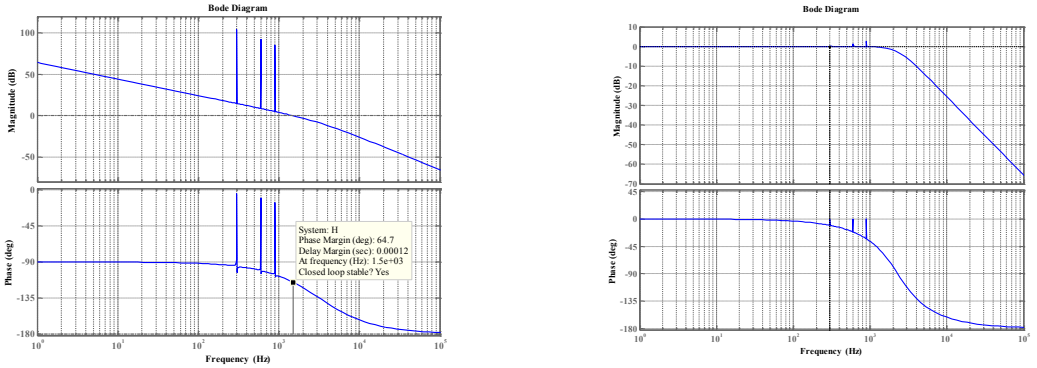


Figure 4.6 Block diagram representation for PI and Resonant current control.



(a) (b)

Figure 4.7 Bode plot of the (a) open loop (b) closed loop transfer function with PI and Resonant current controller.

Table 4-2 closed loop gain and phase for PI and resonant controller at harmonic order.

Harmonic order(n)	Harmonic frequency(Hz)	$\lvert G_{ck}(\omega)\rvert \underline{\lvert G_{ck}(\omega)}$
6	300	$1\underline{\lvert -0.23^0}$
12	600	$1\underline{\lvert -1.86^0}$
18	900	$1\underline{\lvert -0.05^0}$

From Table 4-2 it is observed that PI with resonant controller is tracking the reference current with unity magnitude and with zero phase lag.

4.3.5 DC voltage regulation

Figure 4.8-Figure 4.9 shows the controller for dc voltage regulation for a five level SSBC based D-STATCOM to control the voltages of the 6 floating dc capacitors. The DC capacitor voltage balancing control can be classified into "cluster voltage balancing control" between the three clusters and "individual voltage balancing control" between the two H-bridges in each cluster.The DC capacitors in Cascaded H-bridge D-STATCOM are isolated in phase and the capacitor voltage balancing issue is focused in [116]–[120]. The DC capacitor voltage balancing method with the negative sequence current is proposed in [117] but it does not handle large unbalance in the power system voltage. The energy transfer between the phases of Cascaded H-bridge D-STATCOM is achieved by injecting zero sequence voltage [121], [122]. The zero sequence voltage injection concept is used in [123], [124] for maintaining the DC capacitor voltage balance, when the STATCOM is used for reactive power compensation. The DC capacitor voltage balancing in the presence of unbalanced load with unity power factor mode and zero voltage regulation mode for SSBC D-STATCOM is investigated in this work.

4.3.5.1 Individual DC capacitor voltage balancing

The modulating signals (i.e. v_{aM}^{*} , v_{bM}^{*} , and v_{cM}^{*}) generated by the current control loop are averaged and if given directly as a modulating signal to each H-bride then the capacitor voltage may deviate. The reason is that the active power generated with this average modulating signal in the H-bridge may not be the desired active power for that H-bridge. In this situation, in order to modify the modulating signal, the active voltage superposition (AVS) method is used. In AVS method, the average modulating signal for each H-bridge is changed to a new location in the direction of D-STATCOM current and an independent modulating signal for each H-bridge is generated. The actual DC voltage of an H-bridge is subtracted from the reference voltage and processed in a proportional controller and the output is multiplied with a D-STACOM phase current. The phasor diagram to modify the modulating signal for H1-bridge in phase-a of the D-STATCOM is shown in Figure 4.8(a) and its implementation of modulating signals for two H-bridges in phase-a is shown in the Figure 4.8(b). The remaining modulating signals in other phases are generated in a similar manner.

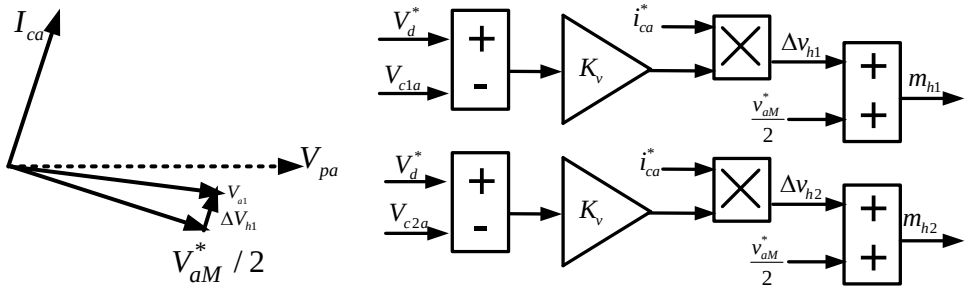


Figure 4.8 Phasor diagram for active voltage superposition for H1-bridge (b) Individual DC capacitor voltage balancing method.

4.3.5.2 Cluster voltage balancing

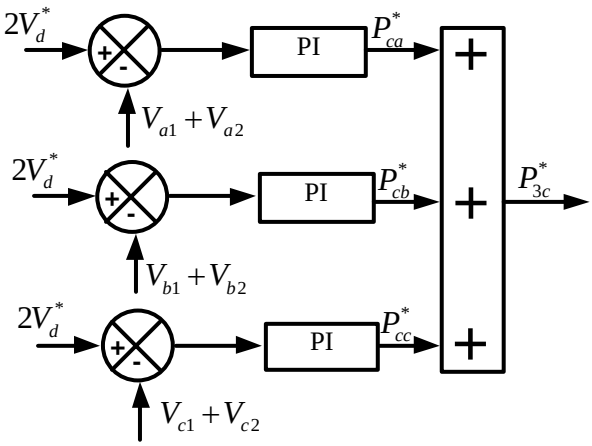


Figure 4.9 Calculation of Compensator powers.

The zero sequence voltage is calculated based on the unbalanced power in the D-STATCOM phases. The phase active power reference of the D-STATCOM can be determined from a PI controller as shown in Figure 4.9. The actual cluster voltage is subtracted from the reference cluster voltage and the error is processed in a PI controller. The output of this controller is treated as desired active power required for that particular phase. The three phase compensator power is the sum of desired active power required by each phase. The unbalanced compensator power is raised because of the unbalanced load on the AC line. The zero sequence voltage is injected such that the desired active power of a phase is equal to the addition of zero sequence power and the average three-phase compensator power. The power in phase-a and phase-b with the zero sequence voltage injection can be found from eq.(4.28)–(4.29). Where in eq.(4.28) –(4.29), $I_{ca}\underline{|\phi_{ca}}$, $I_{cb}\underline{|\phi_{cb}}$ are the known reference D-STATCOM currents, V_0 and Ψ_{v0} are the unknown quantities, these can be determined by solving these two equations and as given in Figure 4.10. The instantaneous zero sequence voltage to be injected is also shown in the block diagram of Figure 4.10 with the necessary computation.

$$P_{ca}^{*}=\frac{P_{3c}^{*}}{3}+V_{o}I_{ca}\cos\left(\psi_{vo}-\phi_{ca}\right) \tag{4.28}$$

$$P_{cb}^{*}=\frac{P_{3c}^{*}}{3}+V_{o}I_{cb}\cos\left(\psi_{vo}-\phi_{cb}\right) \tag{4.29}$$

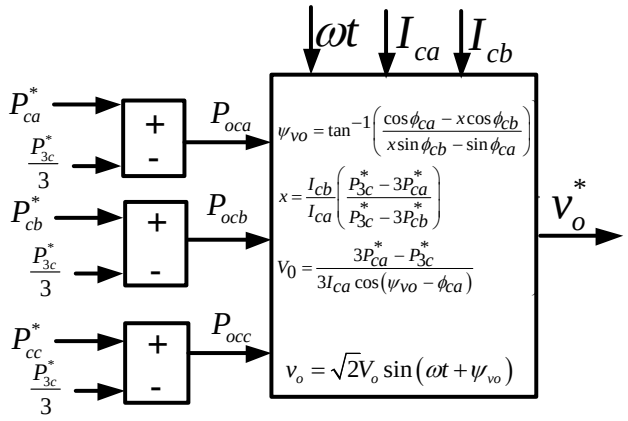


Figure 4.10 Calculation of zero sequence voltage.

4.4 Simulation Results

MATLAB simulation studies under different load conditions have been made to verify the performance of five level SSBC based D-STTACOM for load balancing, harmonic elimination and reactive power compensation in 3P3W distribution system. The simulation studies are used to compare two types of current controllers i.e., PI and PI with resonant controllers for non-linear load. The DC capacitor voltage balancing in the presence of unbalanced linear load for unity power factor mode and zero voltage regulation mode is also investigated.

4.4.1 D-STATCOM Current controller performance with Non-linear load

The control algorithm for the D-STACOM has also been modelled in MATLAB/Simulink. The reference D-STACOM currents have been derived from the synchronous reference frame theory discussed and the unity power factor mode is activated for performance study of this current controller. The parameters used in the simulation are given in Table 4-3.A balanced non-linear load considered is here, so a single DC voltage controller is sufficient for the DC link capacitor voltage balancing. The current controller performance is studied for the uncontrolled and

controlled bridge rectifier with RL and RC loads. In order to study the transient and steady state performance of current controllers, an additional load 50% is connected at t=0.5 sec.

Table 4-3 System parameters for simulation study for current controller performance

Parameter	**Value**
AC line voltage	Three-phase, three-wire, 2.2 kV, 50 Hz
Source impedance	$R_s = 0.1\ \Omega$, $L_s = 0.1$ mH
Coupling inductor of D-STATCOM	$L_c = 14.5$ mH
Commutation inductance	$L_{ac} = 2$ mH
DC bus reference voltage	1200 V (for each capacitor in the H-bridge cell)
DC bus capacitance	110 mF (for each capacitor in the H-bridge cell)
Commutation inductance	$L_{ac} = 2$ mH
Carrier frequency	2 kHz
PI controller parameters	For DC voltage controller: $K_p = 0.08$, $K_i = 0.1$
Load	Three-phase uncontrolled rectifier, $R_{dc} = 500\ \Omega$, $L_{dc} = 500$ mH; Three-phase uncontrolled rectifier, $R_{dc} = 500\ \Omega$, $C_{dc} = 450\ \mu$F; Three-phase phase-controlled rectifier, $R_{dc} = 500\ \Omega$, $L_{dc} = 500$ mH; Three-phase phase-controlled rectifier, $R_{dc} = 500\ \Omega$, $C_{dc} = 450\ \mu$F.

4.4.1.1 Uncontrolled rectifier with RL load

A 3-phase uncontrolled rectifier with RL element on dc side has been considered as a non-linear load in this case. Figure 4.11 and Figure 4.12 shows the simulated waveforms with PI current controller and PI with resonant controller respectively. In Figure 4.11(a) and Figure 4.12(a) and all the subsequent figures in this section shows the similar simulation waveforms, the quantities shown (from top to bottom) as follows:

Trace 1: three phase source voltage (v_{Sabc}),

Trace 2: three phase load current (i_{Labc}),

Trace 3: three phase D-STACOM current (i_{Cabc}),

Trace 4: three phase source current (i_{Sabc}),

Trace 5: downscaled source voltage and current of phase-a, and

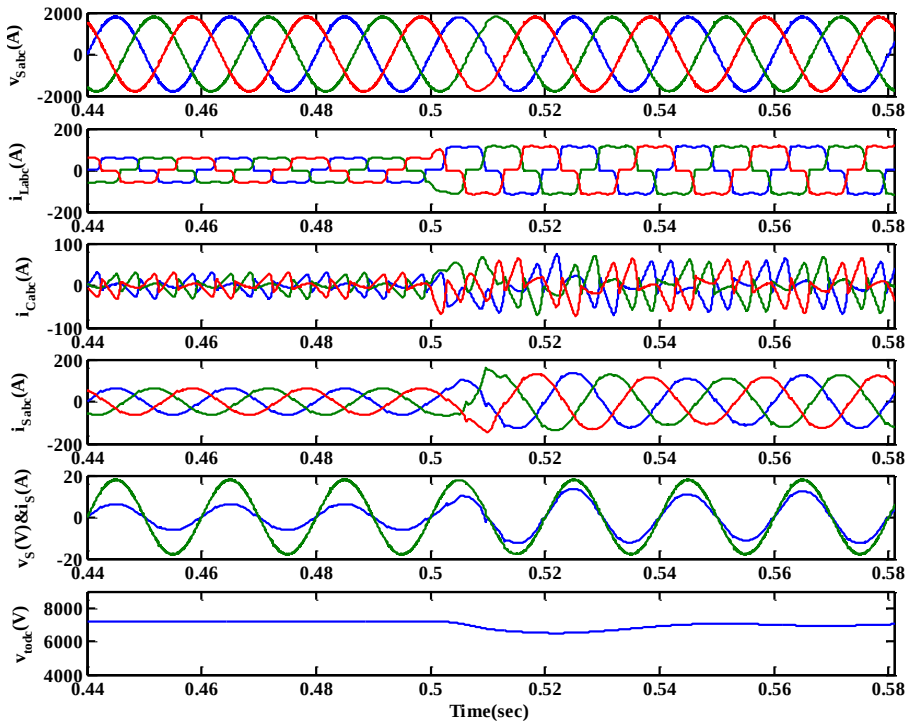
Trace 6: total dc link voltage.

Figure 4.11(b) and Figure 4.12 (b) shows the reference and actual currents of D-STATCOM in synchronous frame. While Figure 4.11(c)-(d), Figure 4.12(c)-(d) shows the harmonic spectrum of load and source currents respectively with PI current controller and with PI and resonant

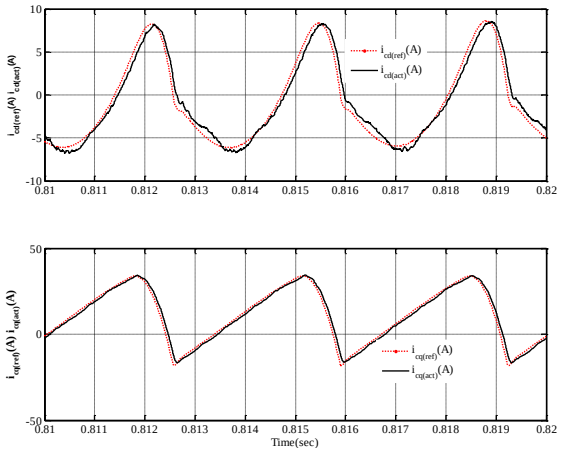
controller. As a three phase balanced load has been considered, the harmonic spectrum of a-phase is shown and the total DC voltage in the SSBC inverter is shown.

From the Figure 4.11 and Figure 4.12 the following observations are made

1. The THD of load current is 25.8% but the source current THD for PI controller is 3.76% and resonant controller is 1.61%
2. The reason can be seen in the harmonic spectrum source currents in the Figure 4.11(d), Figure 4.12(d) it can be seen that the lower order THD for the harmonics the magnitude is reduced this leads to the reduction of THD.
3. The D-STATCOM reference and actual currents in synchronous frame for PI and resonant controller it can be observed that, these currents are fallowed without any phase lag while with PI current controller is having some phase lag which can be clearly seen.
4. After compensation with D-STATCOM, the source current is in phase with the source voltage and confirms the compensation of reactive power. The power factor and input displacement factor is almost unity in both of the cases.
5. The rms value of the load current is 46.45A and that of the source current 44.51A, 44.47A with PI controller and PI with resonant controller. The reduction in the source current is due to the compensation of reactive power of the load.
6. At the instant t=0.5 sec, when the load changes the DC capacitor voltage changes from its reference value to compensate for the enhancement in the load current. This causes a drop in the capacitor voltages which is restored in 1-2 cycles. The regulation of the capacitor voltages can be done by the DC voltage controller.
7. In both the cases, the steady state is reached for the total dc capacitor voltages of all the H-brides with 1-2 cycles with smooth buildup of capacitor voltages with a voltage dip of 50V.
8. At t=0.5 sec, load current is increased to 115A (peak) the corresponding transient change in the compensated and source current has been observed to be very smooth in both of the current controllers and steady state is reached with in one cycle.



(a)



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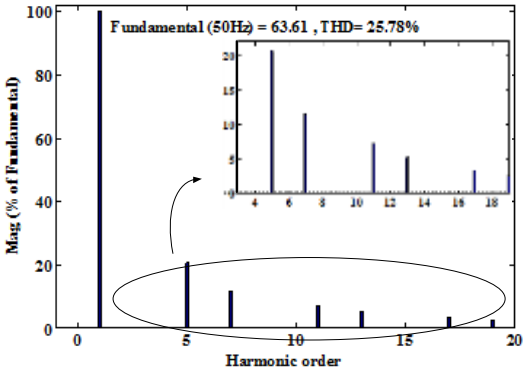
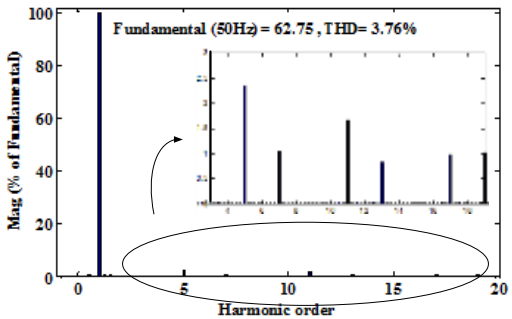
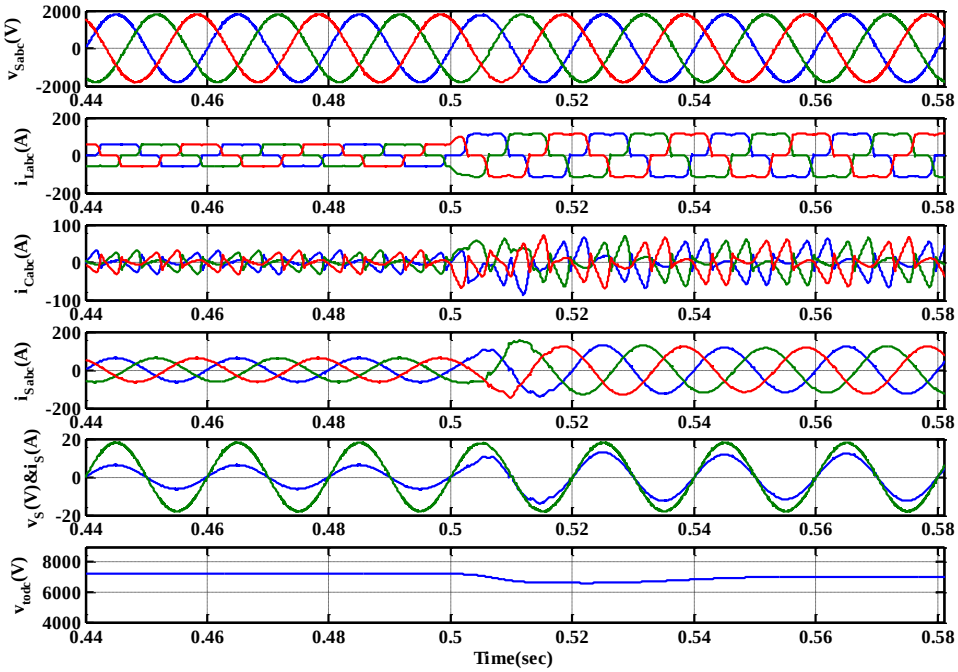


(c)

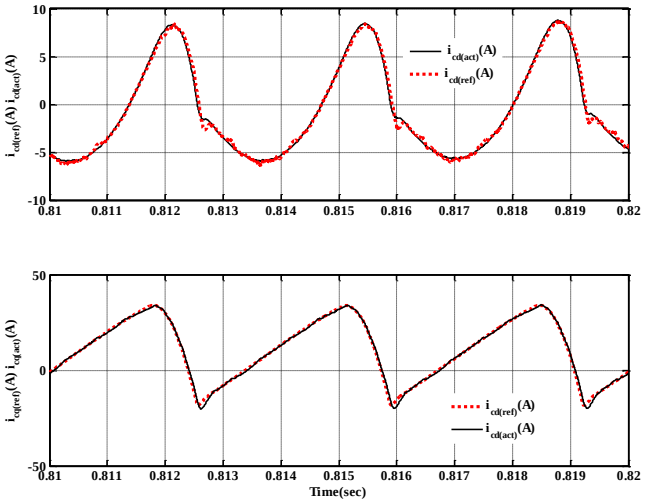


(d)

Figure 4.11 Performance of D-STATCOM for an RL load on the dc side of an uncontrolled rectifier with PI current controller.



(a)



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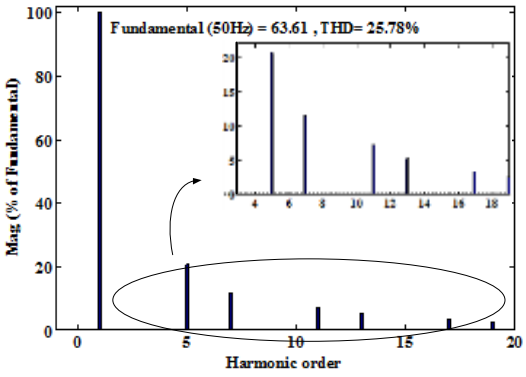

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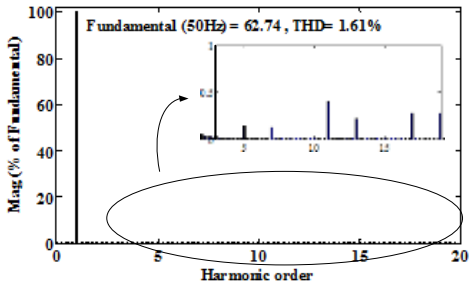


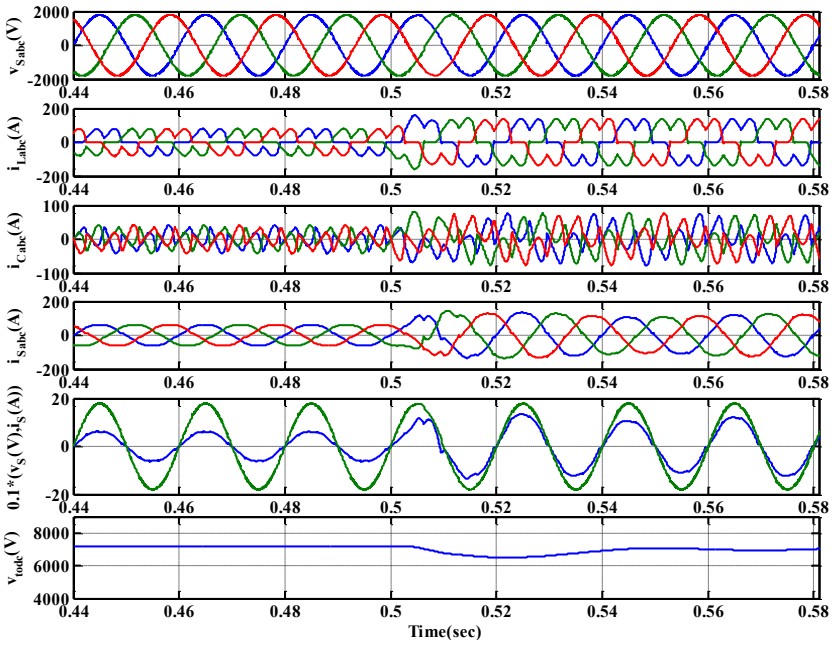
(d)

Figure 4.12 Performance of D-STATCOM for an RL load on the dc side of an uncontrolled rectifier with PI and resonant current controller.

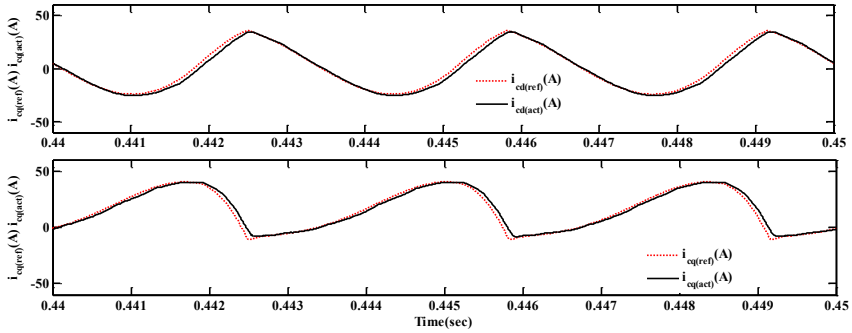
4.4.1.2 Uncontrolled rectifier with RC load

From the Figure 4.13 and Figure 4.14 the following observations are made

1. The THD of load current is 41.31% but the source current THD for PI controller is 5.02% and resonant controller is 1.81%.
2. The reason can be seen in the harmonic spectrum source currents in the Figure 4.13(d),Figure 4.14(d) it can be seen that the lower order THD for the harmonics the magnitude is reduced this leads to the reduction of THD.
3. The D-STATCOM reference and actual currents in synchronous frame for PI and resonant controller it can be observed that, these currents are fallowed without any phase lag while with PI current controller is having some phase lag which can be clearly seen.
4. After compensation with D-STATCOM, the source current is in phase with the source voltage and confirms the compensation of reactive power. The power factor and input displacement factor is almost unity in both of the cases.
5. The rms value of the load current is 49.05A and that of the source current 44.50A, 44.45A with PI controller and PI with resonant controller. The reduction in the source current is due to the compensation of reactive power of the load.
6. At the instant t=0.5 sec, when the load changes the DC capacitor voltage changes from its reference value to compensate for the enhancement in the load current. This causes a drop in the capacitor voltages which is restored in 1-2 cycles. The regulation of the capacitor voltages can be done by the DC voltage controller.
7. In both the cases, the steady state is reached for the total dc capacitor voltages of all the H-brides with 1-2 cycles with smooth buildup of capacitor voltages with a voltage dip of 50V.
8. At t=0.5 sec, load current is increased to 135A (peak) the corresponding transient change in the compensated and source current has been observed to be very smooth in both of the current controllers.



(a)



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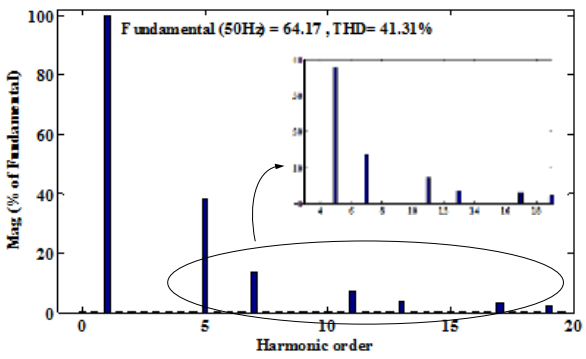

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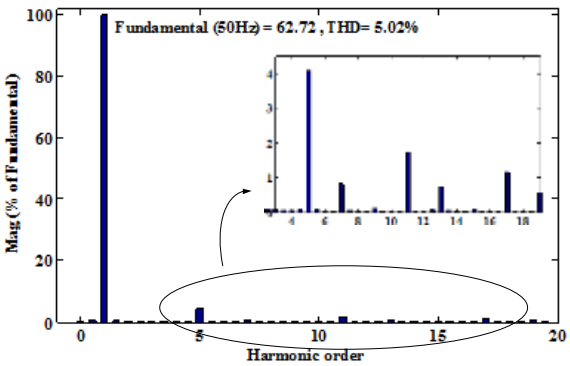
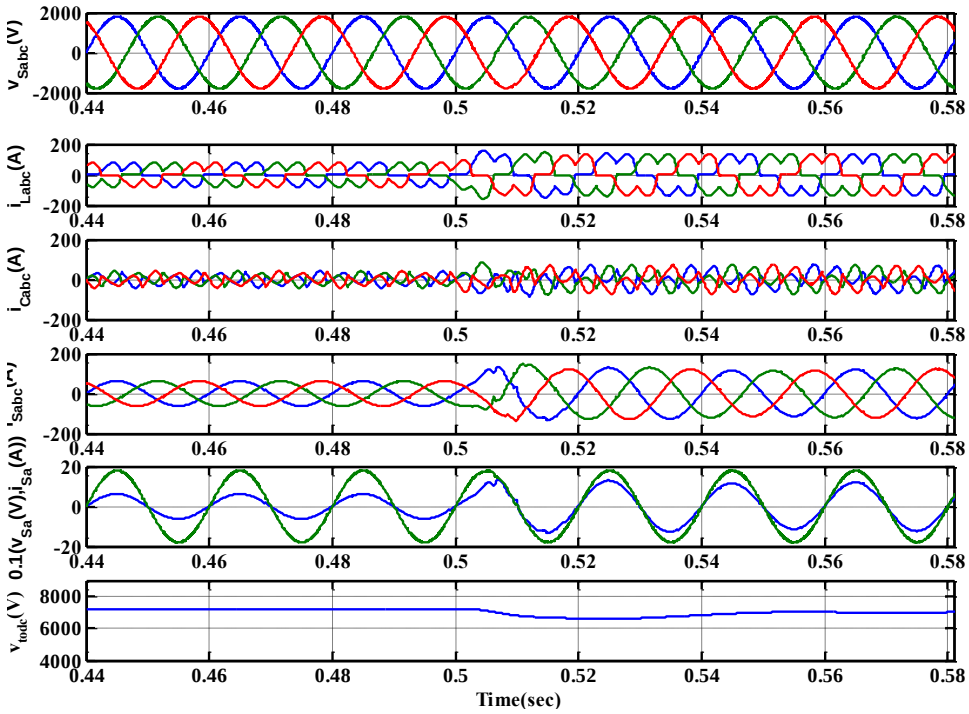
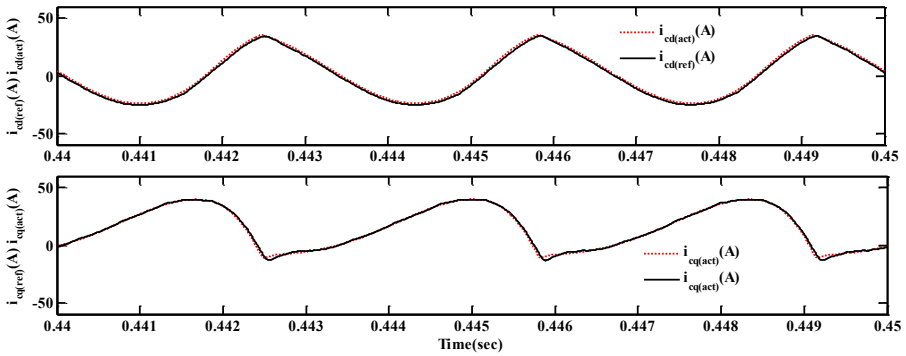


(d)

Figure 4.13 Performance of D-STATCOM for an RC load on the dc side of an uncontrolled rectifier with PI current controller.



(a)



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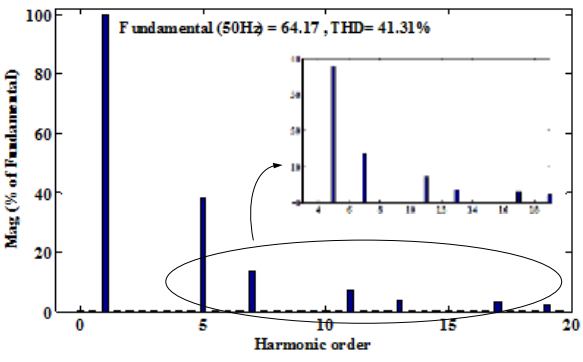

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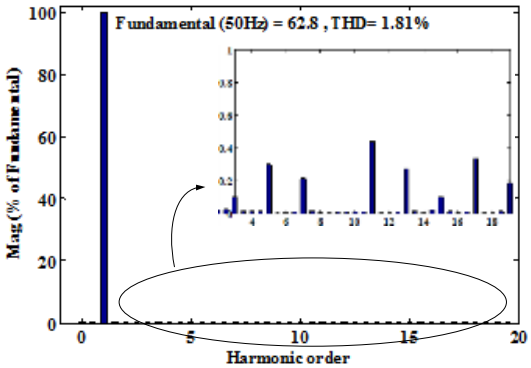


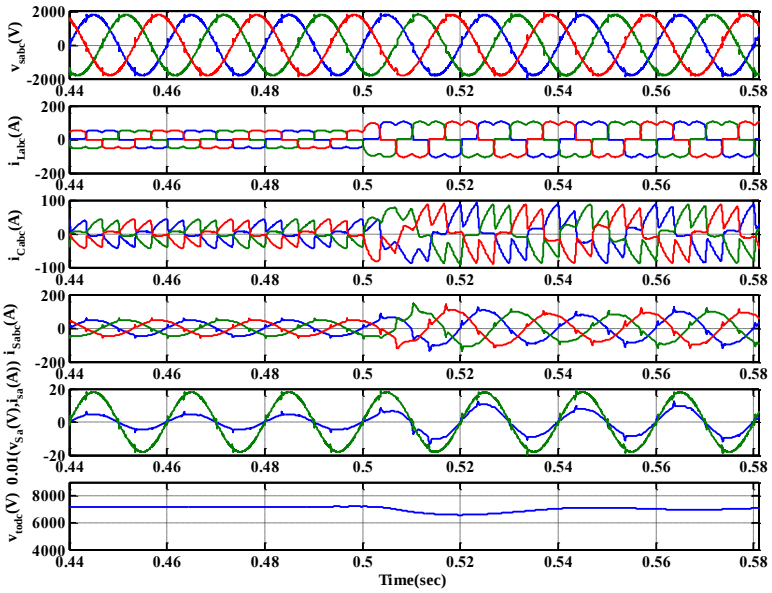
(d)

Figure 4.14 Performance of D-STATCOM for an RC load on the dc side of an uncontrolled rectifier with PI and resonant current controller.

4.4.1.3 Controlled rectifier with RL load

From the Figure 4.15 and Figure 4.16 following observations are made

1. The THD of load current is 28.76% but the source current THD for PI controller is 6.04% and resonant controller is 1.83%
2. The reason can be seen in the harmonic spectrum source currents in the Figure 4.15(d), Figure 4.16(d) it can be seen that the lower order THD for the harmonics the magnitude is reduced this leads to the reduction of THD.
3. The D-STATCOM reference and actual currents in synchronous frame for PI and resonant controller it can be observed that, these currents are fallowed without any phase lag while with PI current controller is having some phase lag which can be clearly seen.
4. After compensation with D-STATCOM, the source current is in phase with the source voltage and confirms the compensation of reactive power. The power factor and input displacement factor is almost unity in both of the cases.
5. The rms value of the load current is 41.18A and that of the source current 34.18A, 34.11A with PI controller and PI with resonant controller. The reduction in the source current is due to the compensation of reactive power of the load.
6. At the instant t=0.5 sec, when the load changes the DC capacitor voltage changes from its reference value to compensate for the enhancement in the load current. This causes a drop in the capacitor voltages which is restored in 1-2 cycles. The regulation of the capacitor voltages can be done by the DC voltage controller.
7. In both the cases, the steady state is reached for the total dc capacitor voltages of all the H-brides with 1-2 cycles with smooth buildup of capacitor voltages with a voltage dip of 50V.
8. At t=0.5 sec, load current is increased to 105A (peak) the corresponding transient change in the compensated and source current has been observed to be very smooth in both of the current controllers.



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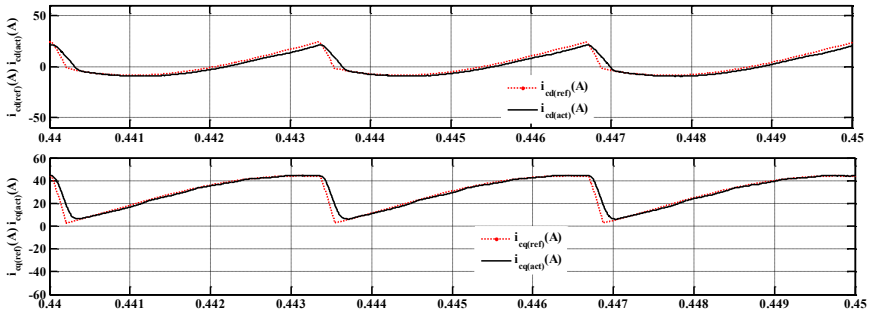

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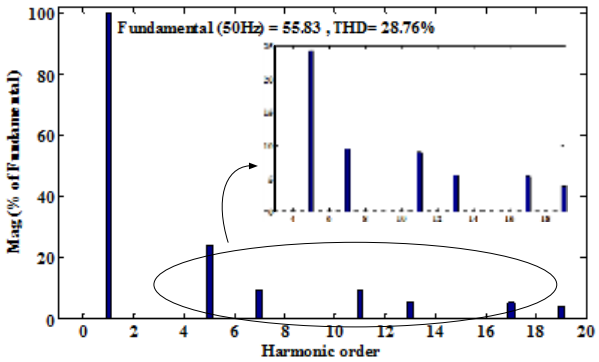

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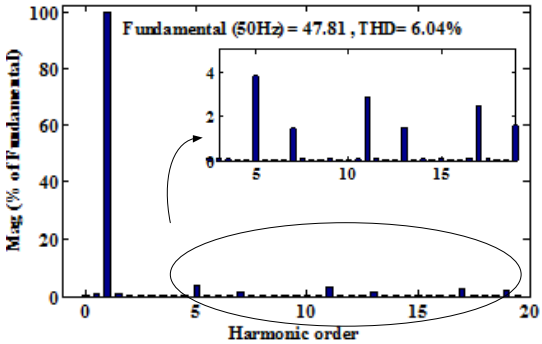
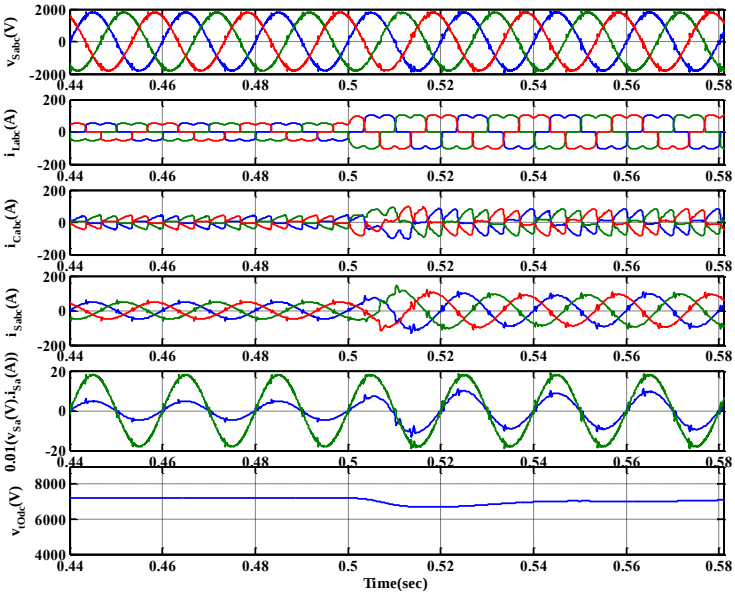
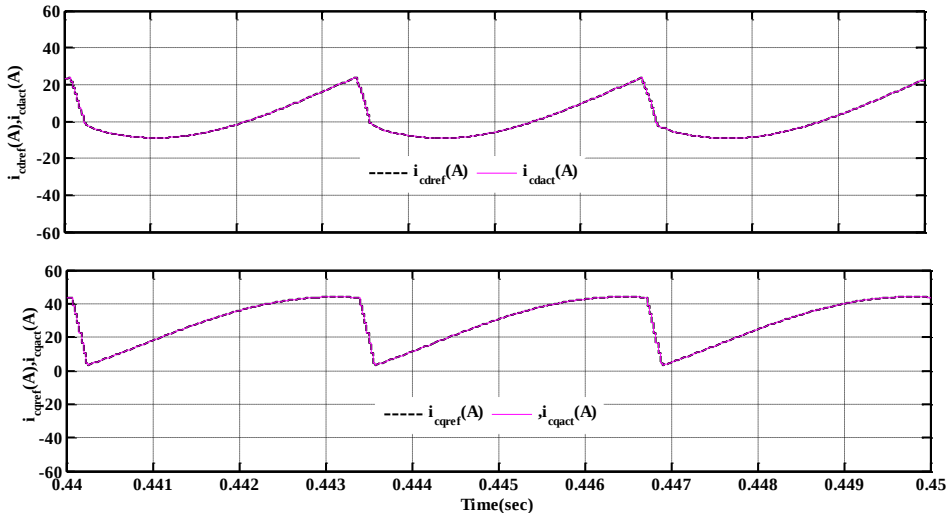


(d)

Figure 4.15 Performance of D-STATCOM for an RL load on the dc side of a controlled rectifier operating at a firing angle of 30^0 with PI current controller.



(a)



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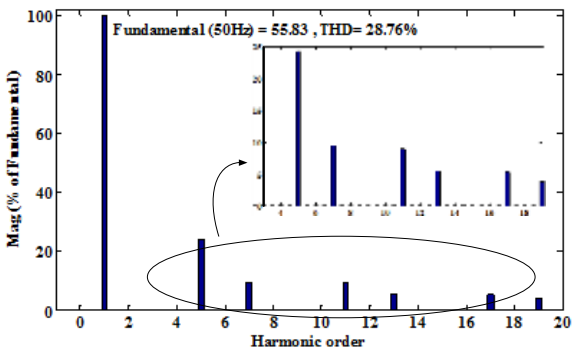

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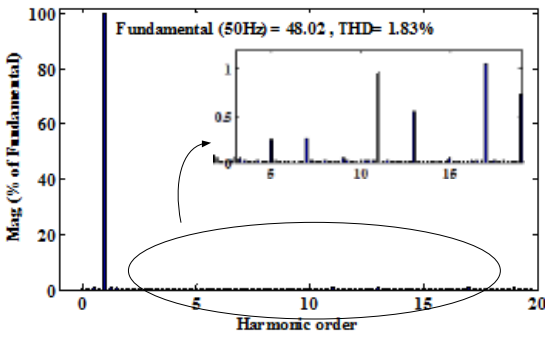


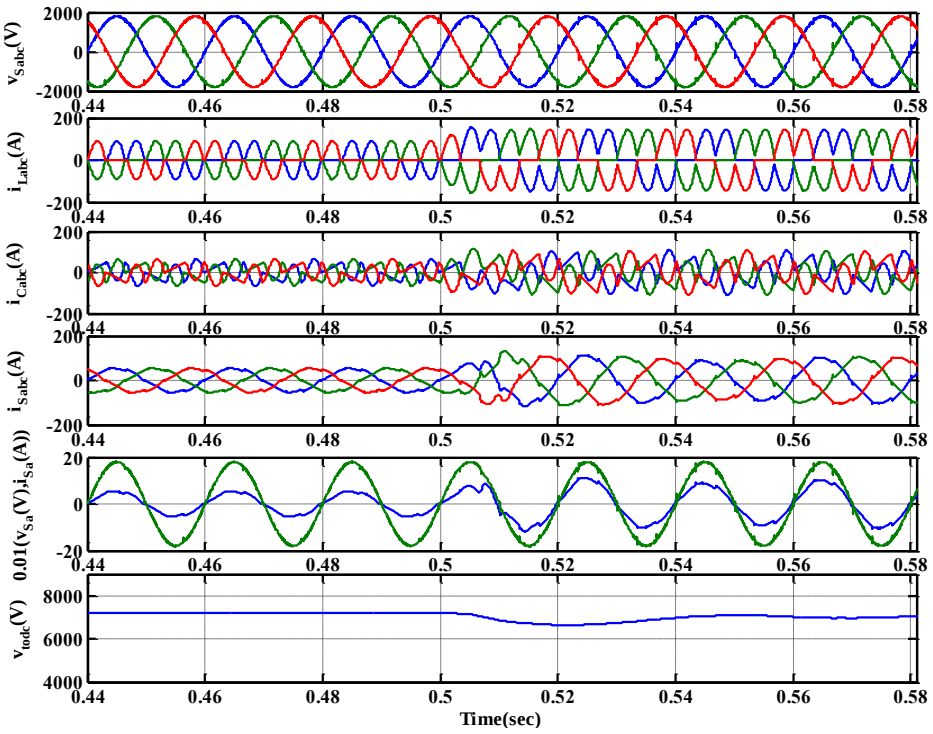
(d)

Figure 4.16 Performance of D-STATCOM for an RL load on the dc side of a controlled rectifier operating at a firing angle of 30^0 with PI and resonant current controller.

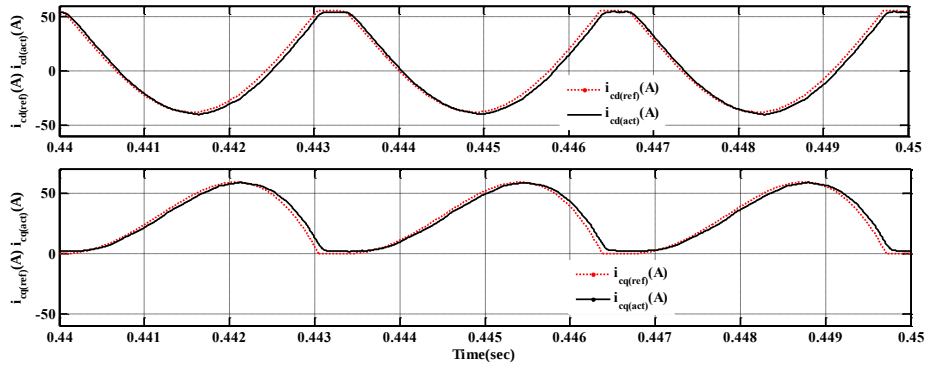
4.4.1.4 Controlled rectifier with RC load

From the Figure 4.17 and Figure 4.18 the following observations are made

1. The THD of load current is 65.17% but the source current THD for PI controller is 5.81% and resonant controller is 1.97%
2. The reason can be seen in the harmonic spectrum source currents in the Figure 4.17(d),Figure 4.18(d) it can be seen that the lower order THD for the harmonics the magnitude is reduced this leads to the reduction of THD.
3. The D-STATCOM reference and actual currents in synchronous frame for PI and resonant controller it can be observed that, these currents are fallowed without any phase lag while with PI current controller is having some phase lag which can be clearly seen.
4. After compensation with D-STATCOM, the source current is in phase with the source voltage and confirms the compensation of reactive power. The power factor and input displacement factor is almost unity in both of the cases.
5. The rms value of the load current is 50.76A and that of the source current 38.09A, 37.97A with PI controller and PI with resonant controller. The reduction in the source current is due to the compensation of reactive power of the load.
6. At the instant t=0.5 sec, when the load changes the DC capacitor voltage changes from its reference value to compensate for the enhancement in the load current. This causes a drop in the capacitor voltages which is restored in 1-2 cycles. The regulation of the capacitor voltages can be done by the DC voltage controller.
7. In both the cases, the steady state is reached for the total dc capacitor voltages of all the H-brides with 1-2 cycles with smooth buildup of capacitor voltages with a voltage dip of 50V.
8. At t=0.5 sec, load current is increased to 145A (peak) the corresponding transient change in the compensated and source current has been observed to be very smooth in both of the current controllers.



(a)



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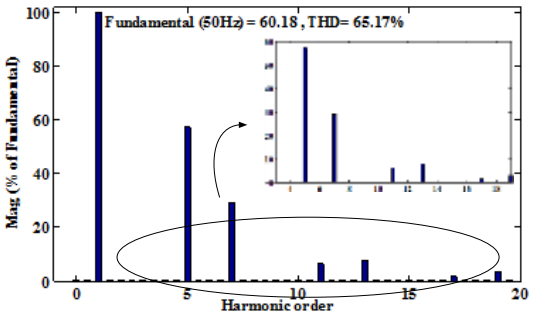

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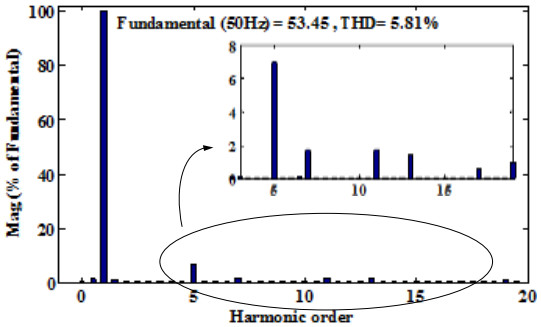
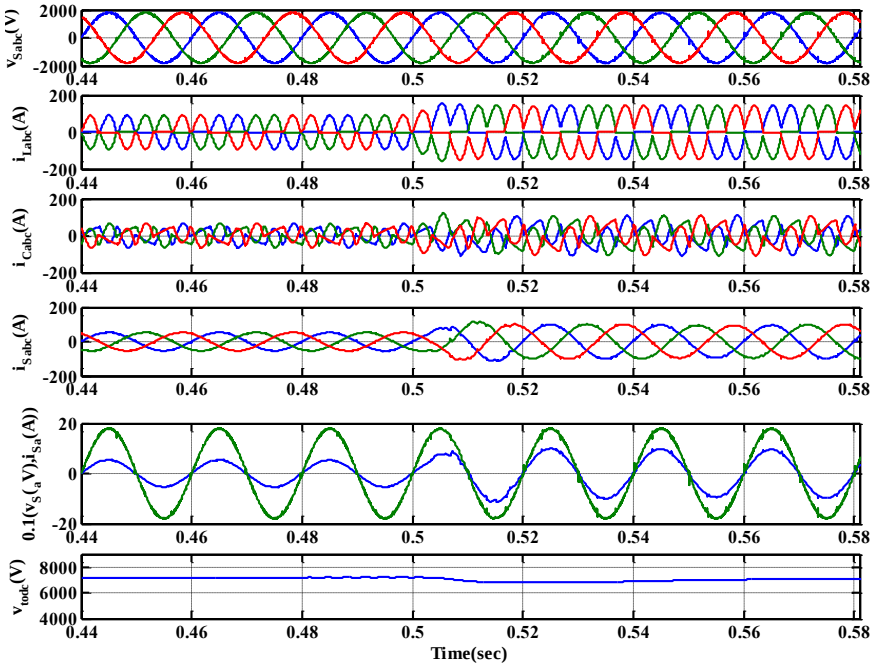
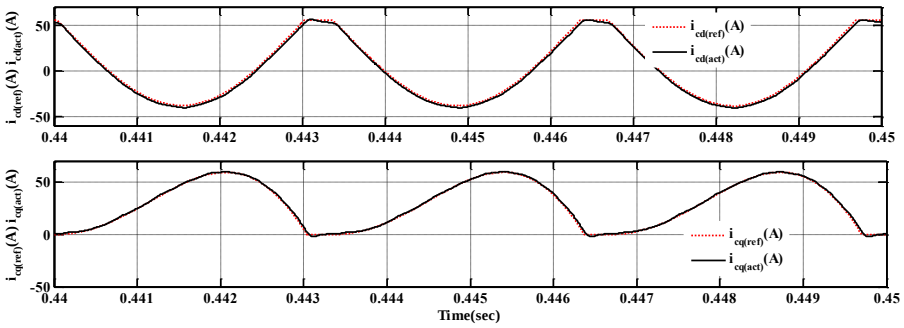


(d)

Figure 4.17 Performance of D-STATCOM for an RC load on the dc side of a controlled rectifier operating at a firing angle of 30^0 with PI current controller.



(a)



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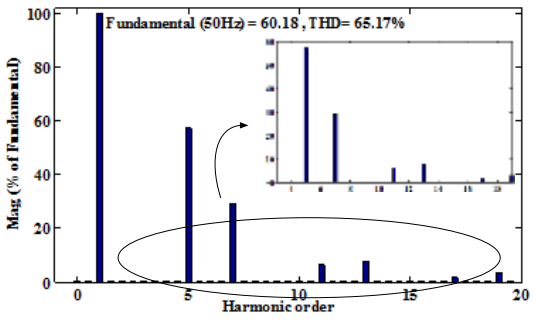

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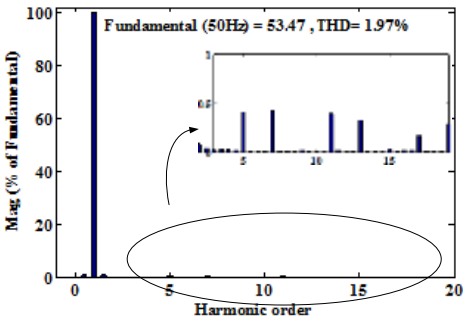


(d)

Figure 4.18 Performance of D-STATCOM for an RC load on the dc side of a controlled rectifier operating at a firing angle of 30^0 with PI and resonant current controller.

4.4.1.5 Comparison of current controllers

Table 4-4 summarize the comparison of the two current controller namely PI and PI with resonant controller for compensation of the reactive/ non-linear loads under ideal source voltage conditions.

Table 4-4 Comparison of two current controller with different non-linear loads.

Parameter	PI controller				PI with resonant Controller			
Reactive/Non-linear load	Diode bridge with RL	Diode bridge with RC	Thyristor bridge with RL	Thyristor bridge with RC	Diode bridge with RL	Diode bridge with RC	Thyristor bridge with RL	Thyristor bridge with RC
% THD of load current	25.78	41.31	28.76	65.17	25.78	41.31	28.76	65.17
% THD of source current after compensation	3.76	5.02	5.04	5.81	1.61	1.81	1.83	1.97
Source power factor before compensation	0.954	0.914	0.8149	0.7454	0.954	0.914	0.8149	0.7454
Source power factor after compensation	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
RMS value of Load current (A)	46.45	49.05	41.18	50.76	46.46	49.07	41.17	50.77
RMS value of Source current after compensation (A)	44.51	44.50	34.18	38.09	44.47	44.45	34.11	37.97

The THD of source current with-out compensation is exceeds the THD limit under IEEE-519 standard. In order to put the THD in acceptable limits the D-STATCOM is used, the two controllers the PI controller only and PI with harmonic current controller is used. From Table 4-4 it can be concluded that current controller with PI and resonant has a relatively superior compensating characteristics when compared with PI current controller. The THD of source current with PI and harmonic current controller is less than 5% this value is accepted under IEEE-519 harmonic standard.

4.4.2 Performance of D-STATCOM under unbalanced linear load

The performance of D-STATCOM for load balancing is presented in this section. In this process of compensation the D-STATCOM has to draw the unbalanced current, this will deviate the capacitor voltages. In order to regulate the dc capacitor voltage to its reference value the cluster

balancing (zero sequence voltage injection) and individual voltage balancing is implemented. The complete system is modelled in the MATLAB-SIMULINK.

Table 4-5 System parameters for simulation study.

Parameter	**Value**
AC line voltage	Three-phase, three-wire, 2.2 kV, 50 Hz
Source impedance	Zsa= Zsb = Zsc =2+j5Ω
DC bus reference voltage	1200 V (for each capacitor in the H-bridge cell)
DC bus capacitance	110 mF (for each capacitor in the H-bridge cell)
Coupling inductor of D-STATCOM	L_c = 14.5 mH
Commutation inductance	L_{ac} = 2 mH
Carrier frequency	2 kHz
PI controller parameters	For DC voltage controller: K_p = 0.08, K_i = 0.1
Unbalanced linear Load	Z_{la}=10+j8 Ω, Z_{lb}=18+j25 Ω, Z_{lc}=10+j22 Ω

4.4.2.1 Load balancing and Zero voltage regulation mode (ZVR)

The unbalanced linear load and other system parameters are given in Table 4-5. Figure 4.19 shows the simulated results with the injection of zero sequence voltage i.e. 3-phase current waveforms of load, D-STATCOM, source along with the capacitor voltages of phase-a, b, and c. From Figure 4.19 it is observed at t=1 sec the ZVR mode of D-STATCOM is activated before to this time interval the source current is seen to be unbalanced. After ZVR mode is activated even though the load current is unbalanced with a peak value of 62 A, 64 A, 76 A, the source currents are balanced with a peak value of 56 A in each phase. The D-STATCOM supplies unbalanced currents with a peak value of 95 A, 80 A, 105 A. To supply these unbalanced currents from D-STATCOM, the capacitor voltages should be properly regulated. When this zero sequence voltage is used in the control strategy, the DC capacitor voltage waveforms are observed in Figure 4.19 to be closely regulated and closely follow the voltage reference value of 1200V.

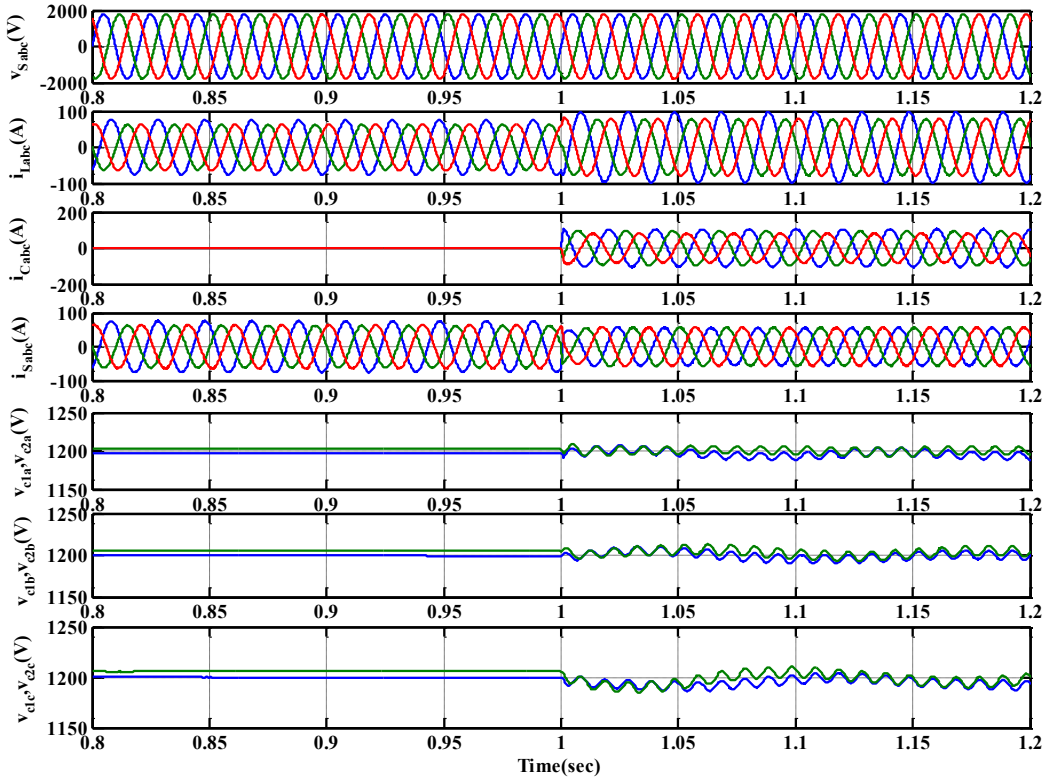


Figure 4.19 Response of D-STATCOM under ZVR mode of operation.

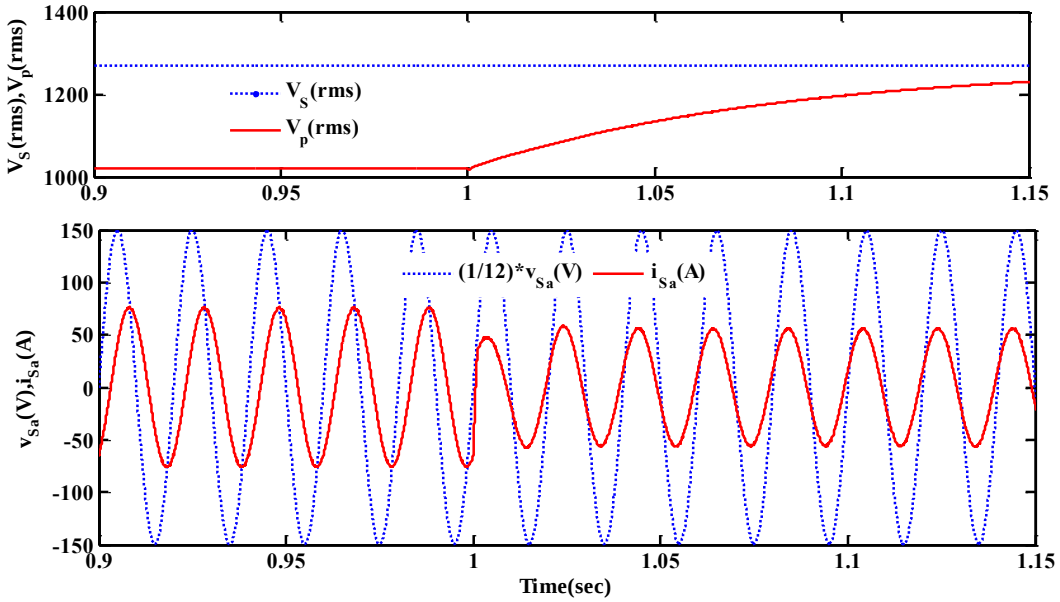


Figure 4.20 Source phase voltage and phase current under ZVR mode.

Figure 4.20 shows the amplitude of source voltage, PCC voltage and waveforms of source voltage and current. At t=1 sec the ZVR mode of D-STATCOM is activated, before this time interval the PCC voltage is found is 1020 V (RMS) which is less than the source voltage of 1270 V (RMS). The voltage drop is attributed to source impedance. After activation of ZVR mode,

the D-STATCOM injects additional reactive power so as to make source current leading and compensate for drop in source impedance.

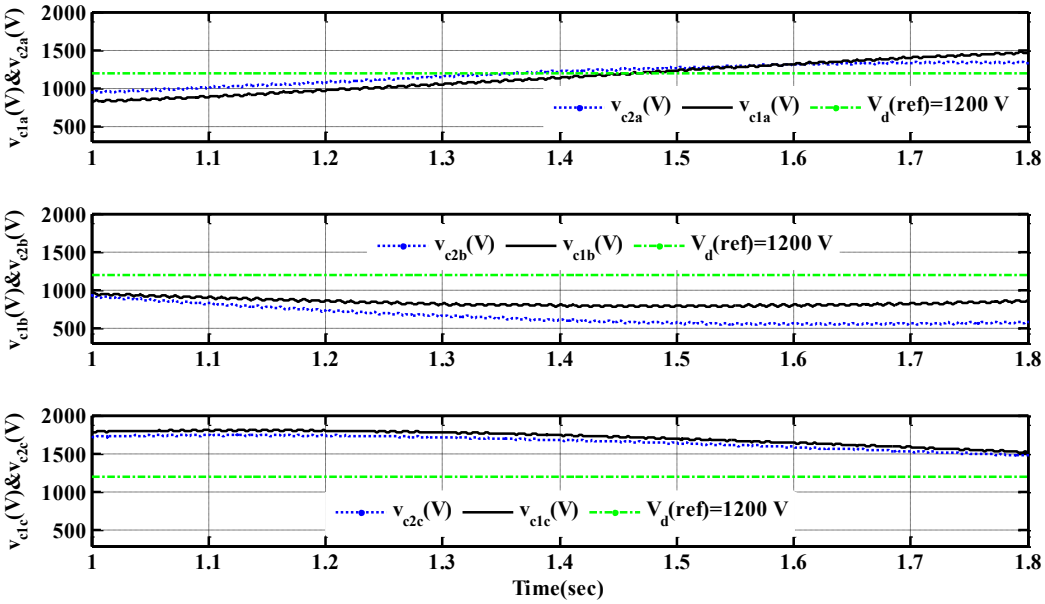


Figure 4.21 DC Capacitor voltages without injection of zero sequence voltage.

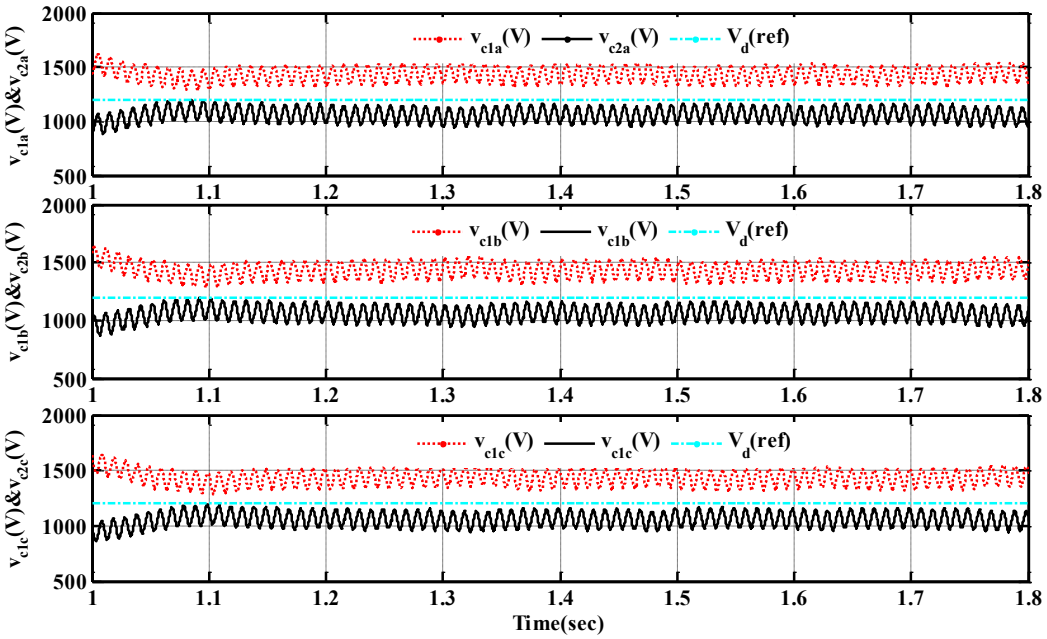


Figure 4.22 DC Capacitor voltages with injection of zero sequence voltage.

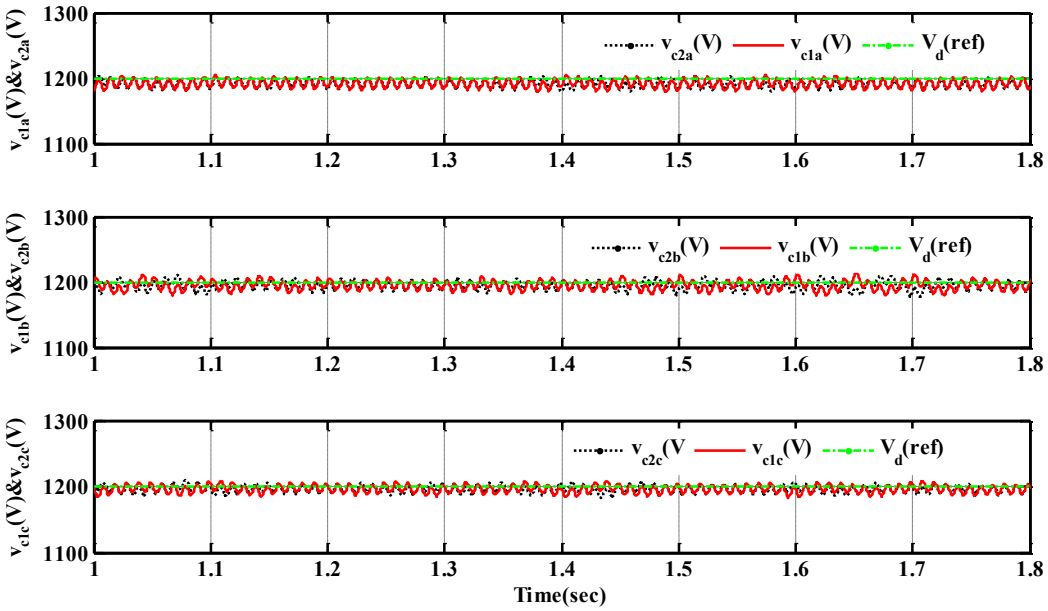


Figure 4.23 DC Capacitor voltages after the injection of zero sequence voltage and individual voltage balancing method.

The Figure 4.21-Figure 4.23 show the capacitor voltage dynamics. Figure 4.21 shows variation of capacitor voltages without the injection of zero sequence voltage and individual voltage balancing method. It can be observed that the capacitor voltages donot converge to the reference the over voltage can damage the IGBT switches of the H-bridge. Figure 4.22 shows the variation of capacitor voltages with the injection of zero sequence voltage the capacitor voltages are nearly steady but they deviate from the reference value of 1200 V. The Figure 4.23 shows the variation of capacitor voltages with the injection of zero sequence voltage and individual balancing method. It is observed that the capacitor voltages converge to the reference voltage of 1200V, which helps in maintaining/tracking reference compensating currents.

4.4.2.2 Load balancing in unity power factor mode

The unbalanced linear load and other system parameters are given in Table 4-5. Figure 4.24 shows the simulated results with the injection of zero sequence voltage i.e. 3-phase current waveforms of load, D-STATCOM, source along with the capacitor voltages of phase-a, b, and c. From Figure 4.24 it is observed at t=1 sec the UPF mode of D-STATCOM is activated before to this time interval the source current is seen to be unbalanced. After UPF mode is activated even though the load current is unbalanced with a peak value of 78 A, 79 A, 98 A, the source currents are balanced with a peak value of 50 A in each phase. The D-STATCOM currents supplies unbalanced currents with a peak value of 71A, 57 A, 80 A. To supply these unbalanced currents from D-STATCOM, the capacitor voltages should be properly regulated. When this zero sequence voltage is used in the control strategy, the DC capacitor voltage waveforms are

observed in Figure 4.24 to be closely regulated and closely follow the voltage reference value of 1200V.

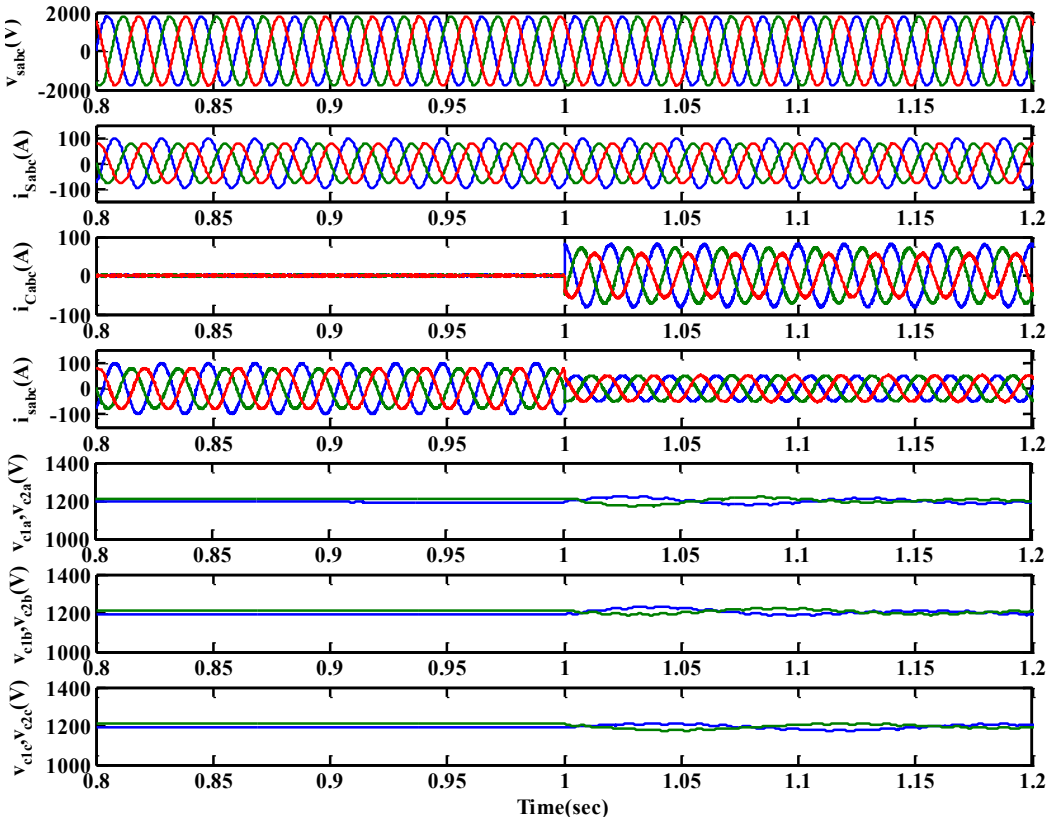


Figure 4.24 Performance of D-STATCOM under UPF mode.

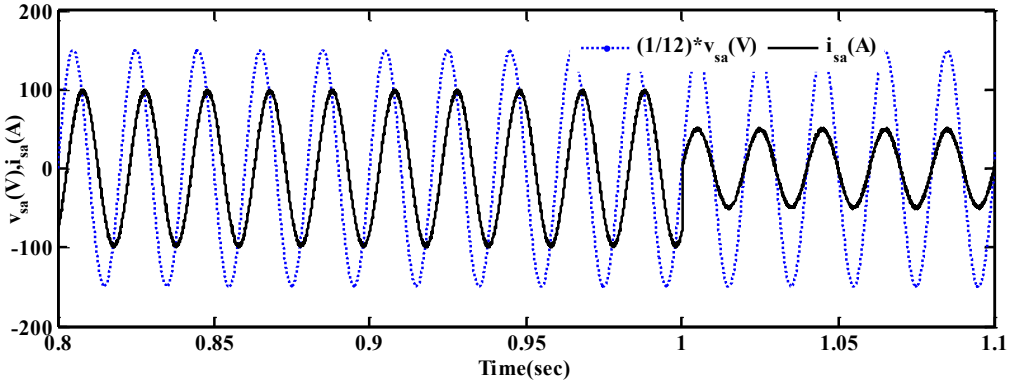


Figure 4.25 Source phase voltage and phase current under UPF mode.

Figure 4.25 shows the waveforms of source voltage and current, at t=1 sec the UPF mode of D-STATCOM is activated resulting that the source phase voltage and current are in phase.

4.5 Conclusion

In this chapter a 2.2 KV, 1MVA five level SSBC based transformerless D-STATCOM has been investigated. As the D-STATCOM is directly connected to the distribution systems, the bulky heavy and costly line frequency transformer can be eliminated. The control algorithm presented

to control the D-STATCOM is not only able to compensate the reactive and harmonics generated by the load but also able to keep the dc voltages of H-bridges controlled in steady state. The PI with resonant controller shows superior performance over to a PI current controller in case of non-linear loads. The dc capacitor voltages are maintained at its reference value in case of compensation for unbalanced linear loads with the help of individual voltage and cluster voltage balancing algorithm.

CHAPTER 5: D-STATCOM OPERATION IN VOLTAGE CONTROL MODE

[This chapter presents the single phase and three phase SSBC based D-STATCOM operating in voltage control mode. The asymmetries in the device characteristics among the H-bridges leads to the deviation in the capacitor voltages. The improved modulating signal method is investigated for single phase D-STATCOM in voltage control mode for capacitor voltage balancing. The zero sequence voltage injection method for capacitor voltage balancing of three phase SSBC based D-STATCOM in voltage control mode is investigated.]

5.1 Introduction

Voltage control of weak distribution grid is a challenging problem, particularly when it is not economical to upgrade the network. D-STATCOM's offer an attractive alternative with potential to provide both steady state and transient voltage compensation with limited capital investment. In the present chapter, the problem of voltage compensation by reactive current injection, at the end of a distribution line, is investigated. In a weak distribution system voltage correction can demand a source current with a leading power factor. The proper operation of the D-STATCOM under unbalanced grid voltage condition is a challenging control issue [120], [125]–[147]. However, the injection of a proper set of unbalanced currents can balance the voltage at the point of common coupling (PCC). In this chapter a control strategy to regulate and balance the voltage at a PCC for single phase and three phase D-STATCOM is developed.

The ideal D-STATCOM has no power loss and it would only supply or absorb the reactive power. In such a case, the amount of capacitor charging and discharging in a cycle would be the same so that DC capacitor voltages will be balanced. However, the switch conduction loss, their asymmetries, and non-ideal passive components cause unequal power dissipation leading to unbalance in capacitor voltage. In this chapter a voltage control mode along with the DC capacitor voltage is investigated for a D-STATCOM connected to a weak grid. The operation of D-STATCOM in voltage control mode is discussed in [132] it is shown that the D-STATCOM can maintain the voltage against any unbalance and distortion either in the load or supply side. An individual voltage balancing (IVBS) has been proposed[74] in a current controlled D-STATCOM to realize independent modulation control for each H-bridge in which an active power component is superposed on AC voltage of H-bridge. The scheme of [74] claims to use the same power factor angle for all the H-bridges in its control scheme but it is found to be

different in this simulation study. The power angle calculation between the two level D-STATCOM voltage and PCC is given in[132] and the voltage controller is realized with dead beat algorithm, here a resonant controller is used for a five level D-STATCOM shown in Figure 5.1.

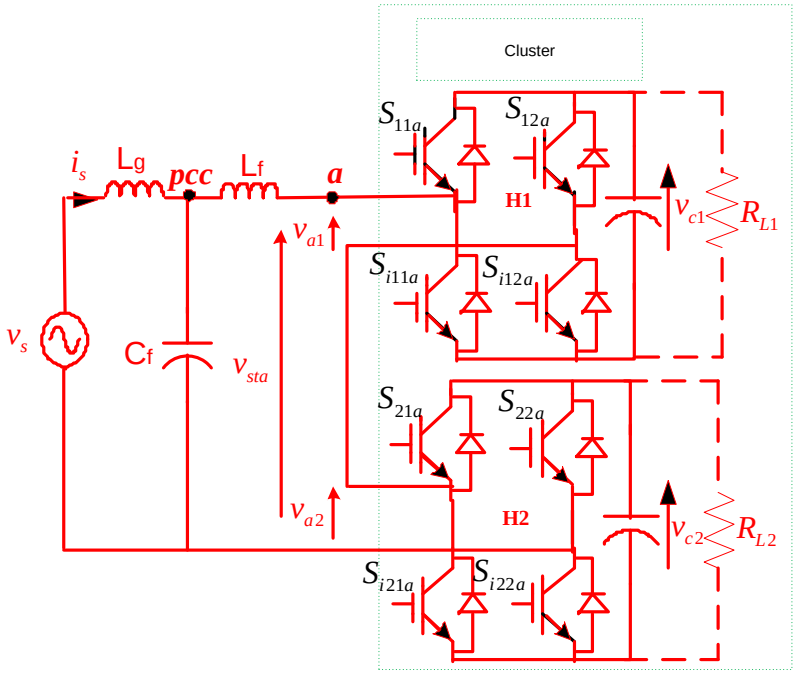


Figure 5.1 Single phase CHB based D-STACOM.

5.2 Voltage control mode for single phase D-STATCOM

The control strategy developed for D-STATCOM operation is based on equal division of reactive power demand between two H-bridges and also on the determination of active power requirement of each H-bridge as per its power loss. It is implemented through two controllers namely- Main control loop and auxiliary control loop. The main control is designed based on the voltage control mode of operation. The output of these two control loops are the modulating signals, the main control loop output is an average modulating signal responsible for the average active power flow and auxiliary control loop gives the modulating signal for individual active power reference, which is responsible for capacitor voltage balancing.

A. Main control loop

The main control loop comprises of active power computation block and voltage controller, which are shown in Figure 5.2. The desired DC capacitor voltage of each H-bridge is V_c^*, the deviation of actual capacitor voltage from its reference is a indication of the losses in the H-bridge. The actual DC capacitor voltage contains of the switching frequency components. Therefore, comparing with the instantaneous value with the reference result in a large error in

the control process, instead here the average of capacitor voltage is used.

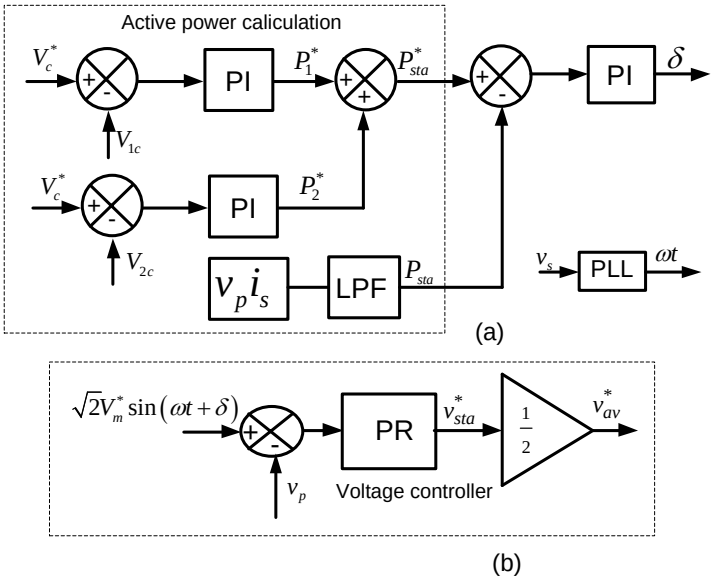


Figure 5.2 (a) Active power calculation and (b) voltage controller.

The active power calculation in Figure 5.2, the actual capacitor voltage is subtracted from the reference capacitor voltage and processed in a PI controller to determine the active power requirement of an H-bridge. The sum of two active power components of the H-bridges is the reference total active power required by the D-STATCOM. The power angle δ which is the phase angle between the source and PCC voltage is calculated so as to ensures the D-STATCOM draws an amount of power P_{sta} that is close to P^*_{sta}. To achieve this a PI controller is used, the output of which is the power angle δ, which is given by eq.(5.1).

$$\delta = k_{p\delta}\left(P^*_{sta} - P_{sta}\right) + k_{i\delta}\int\left(P^*_{sta} - P_{sta}\right)dt \tag{5.1}$$

The reference PCC voltage is given by eq. (5.2), where desired PCC voltage is the reference and its phase angle is calculated based on the power balancing theory.

$$v^*_p = \sqrt{2}V^*_m \sin\left(\omega t + \delta\right) \tag{5.2}$$

The Figure 5.2(b) shows the voltage controller where the actual PCC voltage is subtracted from the reference voltage and error is passed through a proportional resonant (PR) controller to get the reference D-STATCOM voltage. The PR controller transfer function is given by the eq.(5.3) Where ω_0 is the grid frequency, k_p and k_i are the proportional and integral gain.

$$G_c\left(s\right) = k_p + \frac{k_i 2\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{5.3}$$

The cascaded H-bridge D-STATCOM is connected at the PCC with the help of LC filter, so that the transfer function of the plant is given by eq.(5.4)

$$G_p(s) = \frac{sC_f r + 1}{s^2 L_f C_f + sC_f r + 1} \tag{5.4}$$

The controller gains are designed based on the loop shaping techniques, the proportional gain is chosen based on the required closed loop bandwidth and the integral gain is chosen based on the steady state error allowed at the frequency ω_0.The output of the PR controller is the average modulating signal which is used in an auxiliary control loop to generate separate modulating signal generated for each H-bridges.

B. Auxiliary control loop

The aim of designing an auxiliary loop is to maintain the dc capacitor of each H-bridge at its reference value. The individual modulating signal for each H-bridge is generated by the auxiliary loop. The auxiliary control loop i.e improved modulating signal method (IMS) is investigated and this scheme has been discussed in section 3.5.

5.2.1 Simulation results in voltage control mode for single phase D-STATCOM

A five level-cascaded H-bridge converter is connected to a 1050V source with a filter inductance of 1.22mH and a filter capacitor 18μF. The cascaded H-bridge converter, phase shifted pulse width modulation, and the control strategy is modeled in MATLAB-SIMULINK and the results obtained are discussed below.

5.2.1.1 Performance of D-STATCOM with average modulating signal

The STATCOM is operated in voltage control mode of operation to keep the PCC voltage of 1200V even the source voltage is 1050V while the reference DC capacitor voltage is 1250 V. The Figure 5.3 (a)-(d) shows the response of STATCOM, if both the H-bridges are driven by an average modulating signal generated from the main control loop.

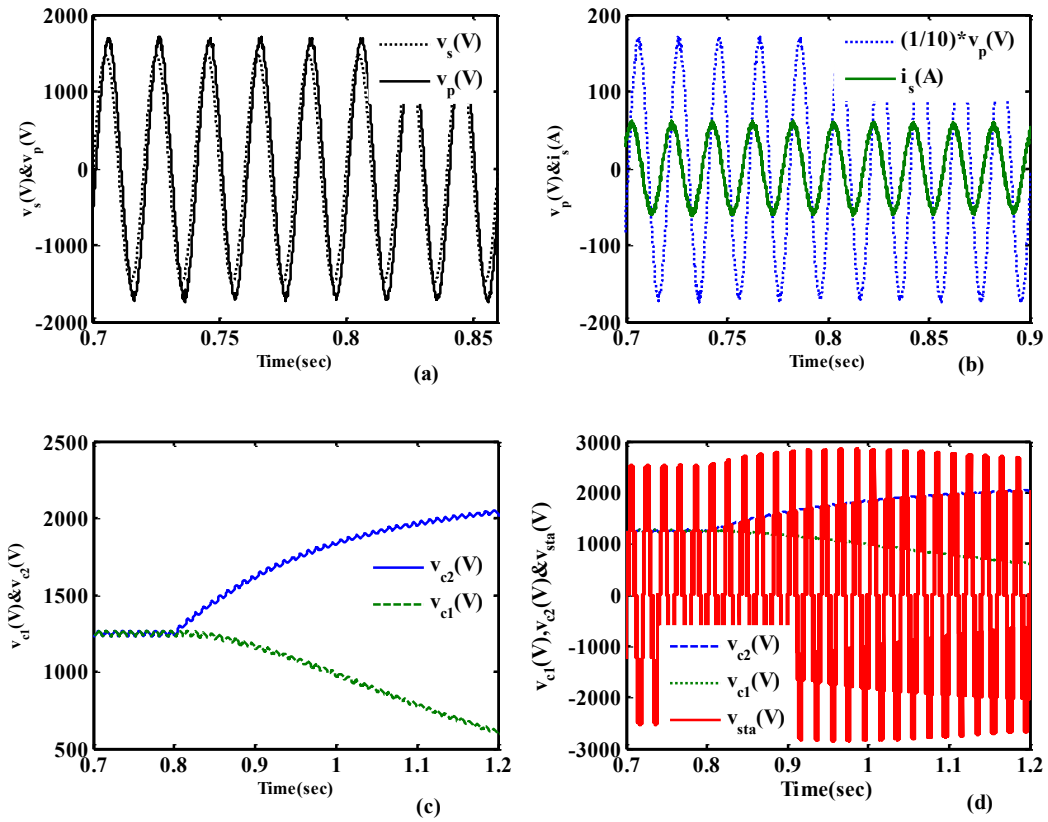


Figure 5.3 Response of D-STATCOM with the average modulating signal.

The Figure 5.3(a) shows the source voltage and PCC voltage, the PCC voltage tracks its reference magnitude of 1200V however it is lagging with source voltage indicating that D-STATCOM is absorbing of active power. The Figure 5.3(b) shows the source current is leading the PCC voltage indicating the STACOM is delivering the reactive power. The Figure 5.3(c)-(d) shows the effect of switching losses on the dc capacitor voltages and the D-STATCOM voltage. Initially, loss in each H-bridge is modelled in the form of equal resistances $R_{L1}=R_{L2}=250\Omega$. At t=0.8 sec, the loss in H1-bridge is set to remains the same ($R_{L1}=250\Omega$) while loss in H2 bridge at zero ($R_{L2}=\infty$). The DC capacitor voltages start to change with V_{c1} in H1-bridge decreasing and V_{c2} in H2-bridge increasing. In the meantime, the D-STATCOM output voltage is also seen to change from 5 level to 3 level in Figure 5.3(d). The overcharged voltage of DC capacitor of H2-bridge can damage the switches. This is the main draw back if unequal losses taken place among the H-bridges, the overcharged dc capacitor voltage can damage the switches.

5.2.1.2 Performance with improved modulating signal (IMS)

The STATCOM is operated in voltage control mode of operation to keep the PCC voltage of 1200V even the source voltage is 1050V while the reference DC capacitor voltage is 1250 V. The Figure 5.4(a)-(d) shows the response of D-STATCOM, if both the H-bridges are driven by

improved modulating signal (IMS) generated from the main control loop.

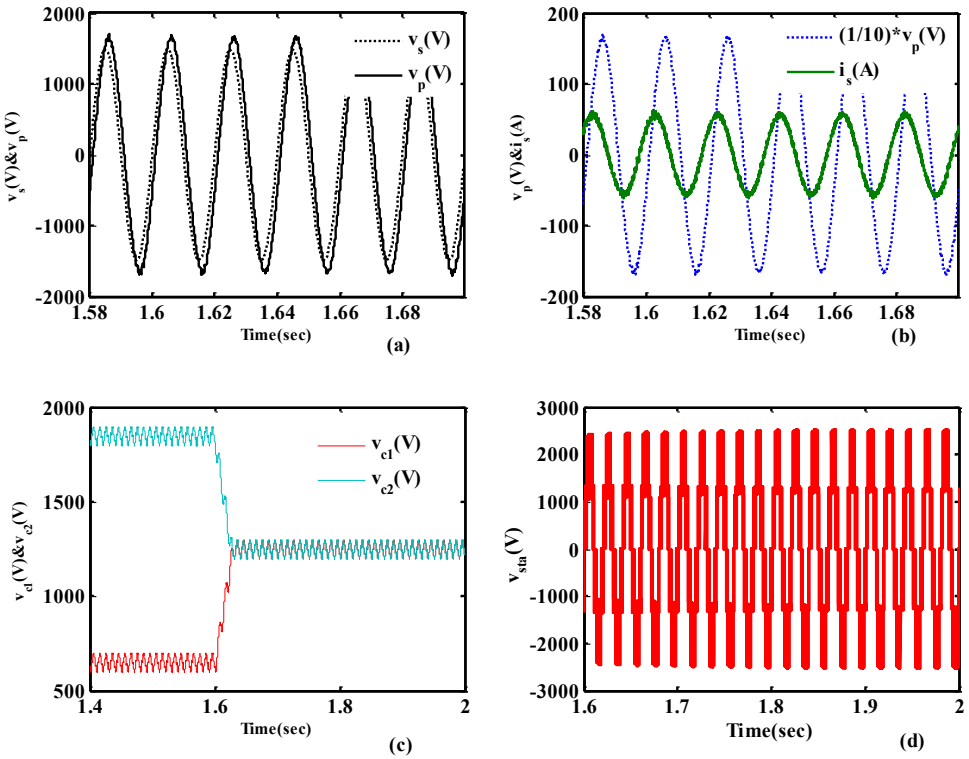


Figure 5.4 Response of D-STATCOM with the improved modulating signals.

The Figure 5.4(a) shows the source voltage and PCC voltage, the PCC voltage tracks its reference magnitude of 1200V however it is lagging behind the source voltage. The Figure 5.4(b) shows the source current is leading the PCC voltage, indicating the D-STATCOM is delivering the reactive power. The Figure 5.4(c)-(d) shows the effect of switching losses on the dc capacitor voltages and the D-STATCOM voltage. Initially, loss in each H-bridge is modelled in the form of unequal resistances R_{L1}=250Ω and R_{L2} =62.5 Ω. At t=1.6 the auxiliary control loop (IMS) is activated, the DC capacitor voltages are now seen to converge at the reference voltage of 1250Vand the D-STATCOM output voltage has five levels as seen in Figure 5.4(d).

5.3 Voltage control mode for three-phase D-STATCOM

The control strategy of D-STATCOM is designed with three objectives (i) Balancing the PCC voltage i.e regulating the positive sequence voltage component to the desired value (ii) Negative sequence component of the PCC voltage is reduced to zero and (iii) The DC capacitor voltage balancing by injection of zero sequence voltage. The control strategy is divided into following three parts:

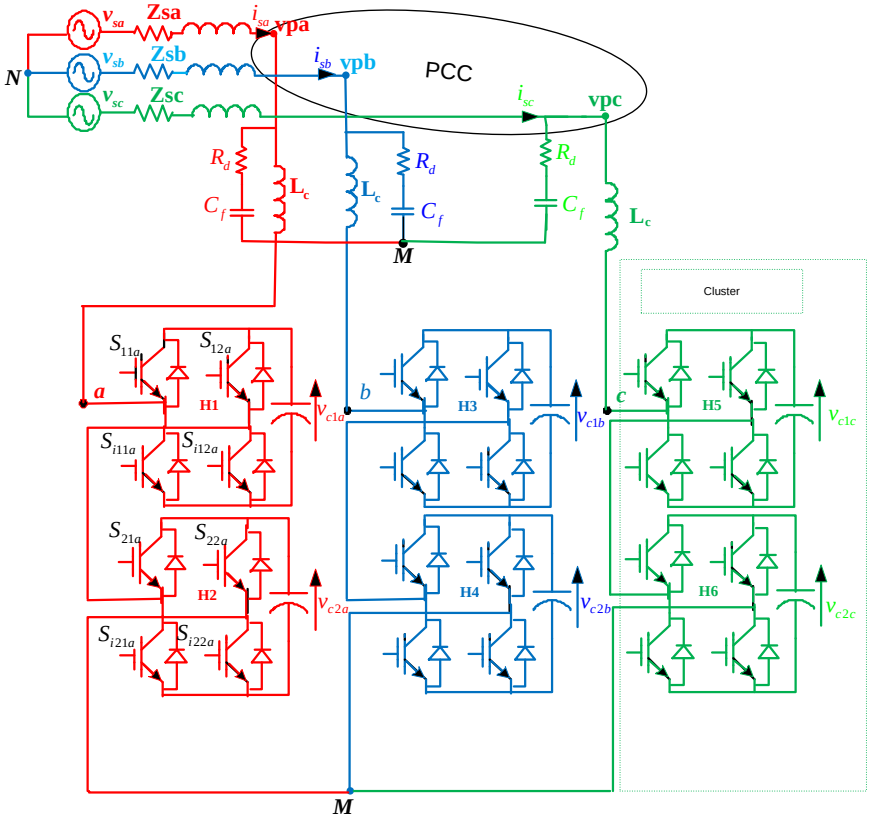


Figure 5.5 SSBC based D-STATCOM.

5.3.1 Generation of reference D-STATCOM currents

The Figure 5.6 shows the generation of reference currents for D-STATCOM in which the sensed PCC voltage is converted into positive and negative reference frames by using parks transformation. The sum of DC cluster voltage is subtracted from the reference capacitor voltage, the result is passed to a PI controller, for determining the positive reference frame direct axis current. The magnitude of PCC voltage is maintained at the desired value (V_p^*) by injecting a suitable reactive current obtained from a PI controller as shown in Figure 5.6. In order to balance the PCC voltage, the negative reference frame direct and quadrature axis voltage are made to zero. Separate PI controller are used to reduce the negative reference frame direct and quadrature axis voltages to zero and the output of the controller decide the negative sequence current to be injected.

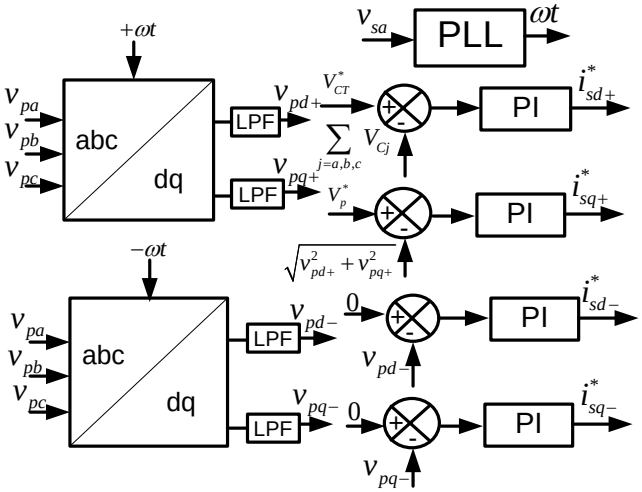


Figure 5.6 Generation of reference currents for D-STATCOM.

5.3.2 Calculation of zero sequence voltage

The zero sequence voltage is injected such that the desired active power of a phase is equal to the addition of zero sequence power and the average three-phase compensator power. The magnitude and angle of D-STATCOM currents $I_{sa}\angle\phi_{sa}$, $I_{sb}\angle\phi_{sb}$ are calculated by taking the instantaneous currents which are converted into positive and negative sequence frame. The magnitude and angles of positive and negative sequence currents can be found from eq. (5) and the phasor quantities of D-STATCOM currents are calculated from eq.(5.6). The power in phase-a and phase-b with the zero sequence voltage injection can be found from eq.(5.7)-(5.8), where in eq.(5.7) $I_{sa}\angle\phi_{sa}$, $I_{sb}\angle\phi_{sb}$ are D-STATCOM currents, V_0 and Ψ_{v0} are the unknown quantities, which can be determined by solving these two equations and shown in Figure 5.7. The instantaneous zero sequence voltage to be injected is also given in the block diagram of Figure 5.7 with the necessary computation.

$$\left.\begin{aligned} |I_{sp}| &= \sqrt{\left(I_{sd+}^2 + I_{sq+}^2\right)} \\ \phi_{sp} &= Tan^{-1}\left(\frac{I_{sq+}}{I_{sd+}}\right) \\ |I_{sn}| &= \sqrt{\left(I_{sd-}^2 + I_{sq-}^2\right)} \\ \phi_{sn} &= Tan^{-1}\left(\frac{I_{sq-}}{I_{sd-}}\right) \end{aligned}\right\} \qquad (5.5)$$

$$\begin{bmatrix} I_{sa}\angle\phi_{sa} \\ I_{sb}\angle\phi_{sb} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1\angle 4\pi/3 & 1\angle 2\pi/3 \end{bmatrix} \begin{bmatrix} I_{sp}\angle\phi_{sp} \\ I_{sn}\angle\phi_{sn} \end{bmatrix} \tag{5.6}$$

$$P_{ca} = \frac{P_{sh}}{3} + V_0 I_{sa} \cos(\psi_{v0} - \phi_{sa}) \tag{5.7}$$

$$P_{cb} = \frac{P_{sh}}{3} + V_0 I_{sb} \cos(\psi_{v0} - \phi_{sb}) \tag{5.8}$$

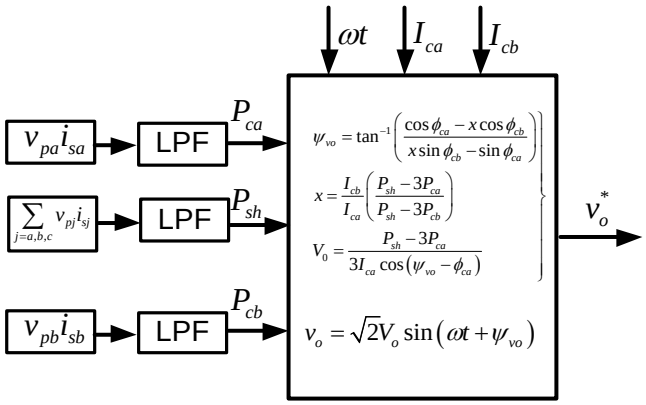


Figure 5.7 Calculation of zero sequence voltage.

5.3.3 Double Synchronous Reference Frame Current Controller (DSRF)

The most effective way to control a reference currents consisting of positive and negative sequence components is to use a current controller based on two synchronous frame rotating at the fundamental grid frequency in the positive and negative directions respectively. The Figure 5.8 shows a dual current controller in which the measured currents are sensed and converted into positive and negative reference frames by using parks transformation. In order to attenuate the effects of the 2ω oscillations in the measured currents notch filters (NF) are used which are tuned at 2ω. In the positive SRF, the actual positive sequence currents are subtracted from the reference currents and this error is processed to a PI controller to which the decoupling terms are added as shown in Figure 5.8 to give the resultant modulating signal. The direct, quadrature and zero sequence modulating signals are converted into abc frame. In the negative SRF, the actual negative sequence currents are subtracted from the reference currents and this error is processed to a PI controller to which the decoupling terms are added to give the resultant modulating signal. The direct, quadrature and zero sequence modulating signals are converted into abc frame.

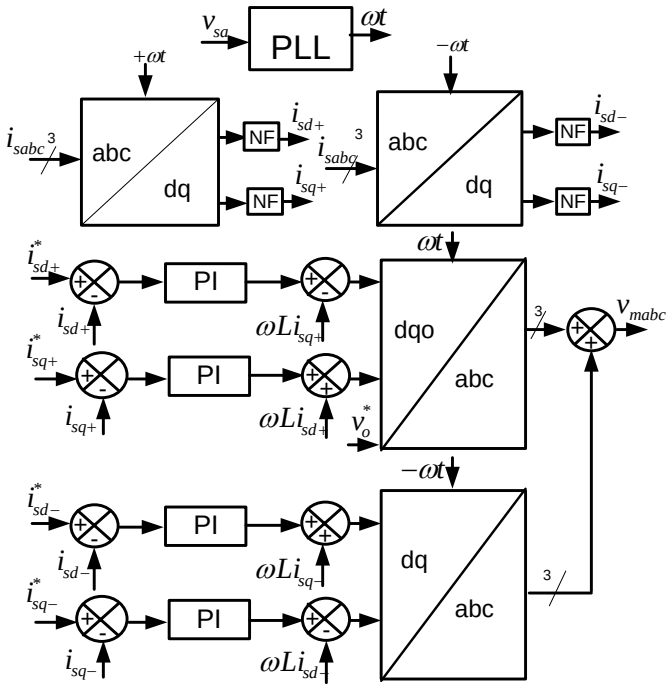


Figure 5.8 Dual current controller for D-STATCOM.

5.3.4 PCC voltage and current controller

The PCC voltage can be balanced at a desired magnitude by injecting appropriate unbalanced current. Hence a relation between PCC voltage magnitude and current injected has been derived. From Figure 5.5 applying KVL, equation (5.9) is obtained.

$$\begin{pmatrix} v_{sa} \\ v_{\mathrm{sb}} \\ v_{\mathrm{sc}} \end{pmatrix} - \begin{pmatrix} v_{p\mathrm{a}} \\ v_{p\mathrm{b}} \\ v_{p\mathrm{c}} \end{pmatrix} = L_s \begin{pmatrix} \frac{di_{sa}}{dt} \\ \frac{di_{sb}}{dt} \\ \frac{di_{sc}}{dt} \end{pmatrix} + R_s \begin{pmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{pmatrix} \tag{5.9}$$

The transformation matrix in positive sequence reference frame is

$$\left(C_s^+\right) = \frac{2}{3} \begin{pmatrix} \sin\left(\theta^+\right) & \sin\left(\theta^+ - \frac{2\pi}{3}\right) & \sin\left(\theta^+ + \frac{2\pi}{3}\right) \\ \cos\left(\theta^+\right) & \cos\left(\theta^+ - \frac{2\pi}{3}\right) & \cos\left(\theta^+ + \frac{2\pi}{3}\right) \end{pmatrix} \tag{5.10}$$

The transformation matrix in negative sequence reference frame is

$$\left(C_s^-\right)=\frac{2}{3}\begin{pmatrix}-\sin\left(\theta^+\right) & -\sin\left(\theta^+-\frac{2\pi}{3}\right) & -\sin\left(\theta^++\frac{2\pi}{3}\right)\\ \cos\left(\theta^+\right) & \cos\left(\theta^++\frac{2\pi}{3}\right) & \cos\left(\theta^+-\frac{2\pi}{3}\right)\end{pmatrix} \tag{5.11}$$

Multiply equation (5.9) with equation (5.10) , and applying Laplace transform

$$\begin{pmatrix}v_{pd}^+(s)\\ v_{pq}^+(s)\end{pmatrix}=\begin{pmatrix}sL_s+R & -\omega L_s\\ \omega L_s & sL_s+R\end{pmatrix}\begin{pmatrix}i_{sd}^+(s)\\ i_{sq}^+(s)\end{pmatrix} \tag{5.12}$$

Where v_{pd}^+ and i_{sd}^+ are d-axis components of PCC voltage and compensator current in positive sequence synchronous reference frame. v_{pq}^+ and i_{sq}^+ are q-axis components of PCC voltage and compensator current in positive sequence synchronous reference frame. Multiply equation (5.9) with equation (5.11) and apply Laplace transform

$$\begin{pmatrix}v_{gd}^-(s)\\ v_{gq}^-(s)\end{pmatrix}=\begin{pmatrix}sL_s+R & \omega L_s\\ -\omega L_s & sL_s+R\end{pmatrix}\begin{pmatrix}i_{sd}^-(s)\\ i_{sd}^-(s)\end{pmatrix} \tag{5.13}$$

Where v_{pd}^- and i_{sd}^- are d-axis components of PCC voltage and compensator current in negative sequence synchronous reference frame. v_{pq}^- and i_{sq}^- are q-axis components of PCC voltage and compensator current in negative sequence synchronous reference frame.

$$\frac{v_{pq}^+(s)}{i_{sd}^+(s)}=-\omega L_s,\frac{v_{pd}^-(s)}{i_{sq}^-(s)}=\omega L_s,\frac{v_{pq}^-(s)}{i_{sd}^-(s)}=-\omega L_s \tag{5.14}$$

Equation (5.14) shows variation of PCC voltages due to the currents injected by D-STATCOM in fundamental positive and negative sequence reference frames. Figure 5.6 shows a basic control strategy for regulating the voltage at PCC. There are three outer loop voltage regulators which maintain the magnitude and balance of the PCC voltage, these regulators are realized with a PI controller. This control loop is tuned to achieve a response time of one to two cycles. The outer loop controller is sensitive to the external grid impedance as well as interaction between the control loops. Hence tuning of this controller to achieve good performance under varying system conditions while maintaining a stable response requires proper design of controller. The tuning and design procedure of one of the controller is given below similar procedure is repeated for other controllers.

Assuming that the current controller is having larger bandwidth, the control block diagram of PCC voltage controller is shown in the Figure 5.9, where G_{vcpos} is plant transfer function, H_{vcpos} is PI controller and G_{vlpf} is low pass filter.

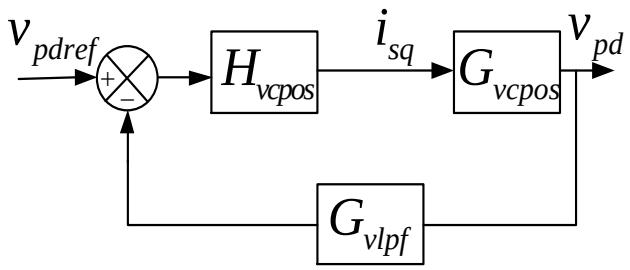


Figure 5.9 PCC voltage control loop

The plant transfer function G_{vcpos} for one of the loop is given by equation (5.15)

$$G_{vcpos}(s) = \frac{v_{pd}(s)}{i_{sq}(s)} = -\omega L_s \tag{5.15}$$

The transfer function of the controller H_{vcpos} is to be designed

$$H_{vcpos}(s) = K_{pvc} + \frac{K_{ivc}}{s} \tag{5.16}$$

In a practical situation, the sensed PCC voltage will not be constant on the account of several reasons. Some of the possible sources of noise are given below

- The PCC voltages carry a small unbalance. Any negative sequence voltage introduces a second harmonic component
- Any PCC voltage harmonic at frequency ω_h introduces an oscillatory component at frequency $\omega_h \pm \omega$

Hence a low pass filter is required during practical implementation. The transfer function of low pass filter G_{vlpf} is

$$G_{vlpf}(s) = \frac{\omega_{vlpf}}{s + \omega_{vlpf}} \tag{5.17}$$

Where ω_{vlpf} is corner frequency of low pass filter. Lower the corner frequency ω_{vlpf} of low pass filter slower is the response PCC voltage controller.

The loop gain G_{vcloop} is

$$G_{vcloop} = G_{vcpos}(s) H_{vcpos}(s) G_{vlpf}(s) \tag{5.18}$$

The closed loop transfer function is

$$G_{clloop} = \frac{v_{gd}(s)}{v_{gdref}(s)} = \frac{G_{vcpos}(s) H_{vcpos}(s)}{1 + G_{vcpos}(s) H_{vcpos}(s) G_{vlpf}(s)} \tag{5.19}$$

Controller design objective for the above system is to achieve a first order unity gain closed loop system for the frequency range of interest. The closed system should also have the required bandwidth. The controller transfer function $H_{vcpos}(s)$ is selected so that the overall loop gain is given by eq.(5.20), where ω_b is the bandwidth of PCC voltage controller. The unknown controller parameters can be found by equating both of the equations and the values are given by eq.(5.21).

$$G_{vcloop} = \frac{\omega_b}{s} \tag{5.20}$$

$$\left\{ \begin{array}{l} K_{pvc} = \dfrac{\omega_b}{\omega L_s \omega_{vlpf}} \\ K_{ivc} = \dfrac{\omega_b}{\omega L_s} \end{array} \right\} \tag{5.21}$$

From Figure 5.10, it is observed that as corner frequency of low pass filter decreases, bandwidth and phase margin of the system decreases. As bandwidth decreases, settling time of the system increases.

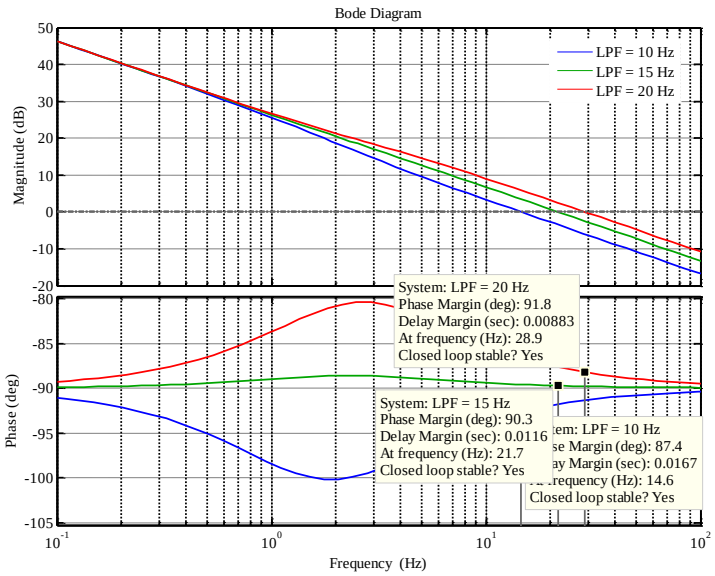


Figure 5.10 Bode plot of voltage controller loop gain.

To maintain a good filtering performance, the resonance frequency of LCL filter should be placed outside the operating bandwidth. The bandwidth of loop gain (G_{Loopk}) is taken as 1100Hz. For sufficient switching harmonic suppression, the desired switching frequency (f_{sw}) of the converter can be set 2.5 times larger than the controller bandwidth. The plant transfer function $G_{LCL,dq}$, with this assumption can be derived from equivalent circuit diagram shown in Figure 5.12.

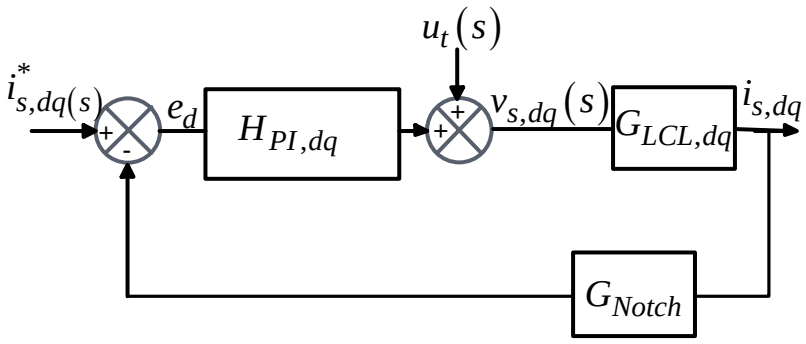


Figure 5.11 : Closed loop current control.

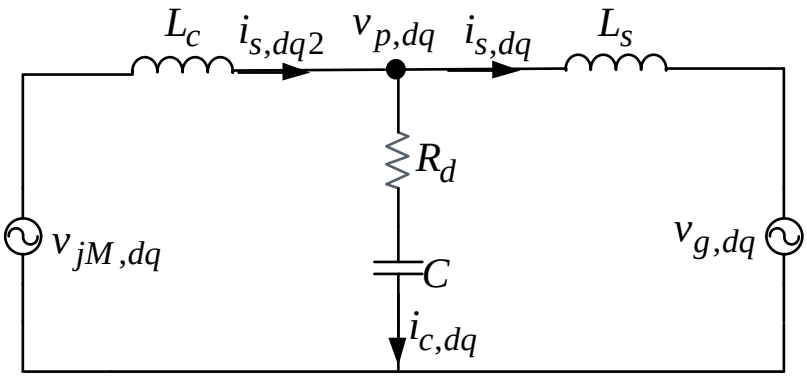


Figure 5.12 : Single phase equivalent circuit diagram.

$$G_{LCL,dq}=\frac{i_{s,dq}}{v_{s,dq}}=\frac{1+sCR_d}{s^3L_sL_cC+s^2(L_s+L_c)CR_d+s(L_s+L_c)} \tag{5.22}$$

The controller $H_k(s)$ is designed through loop shaping method. The controller is designed such that current loop bandwidth is 1100Hz and phase margin is 84°.The controller $H_{PI,dq}(s)$ designed, is given by,

$$H_{PI,dq}(s)=300+\frac{400}{s} \tag{5.23}$$

The generalized current control loop with feed forward term is shown in Figure 5.11. The loop gain ($G_{Loop,dq}$) is given by eq.(5.24). The corresponding loop gain plot is shown in Figure 5.13 and the stability is verified.

$$G_{Loop,dq}=G_{LCL,dq}*H_{PI,dq}(s) \tag{5.24}$$

The transfer function of notch filter is

$$H_{notch}(s)=\frac{s^2+(2\omega)^2}{s^2+2K_n\omega s+(2\omega)^2} \tag{5.25}$$

Where K_n decides the band and its value is taken as 1.414

The loop gain G_{Loopk} of the current controller with the inclusion of notch filter changes to

$$G_{Loop,dq}=G_{LCL,dq}*H_{PI,dq}(s)*H_{notch}(s) \tag{5.26}$$

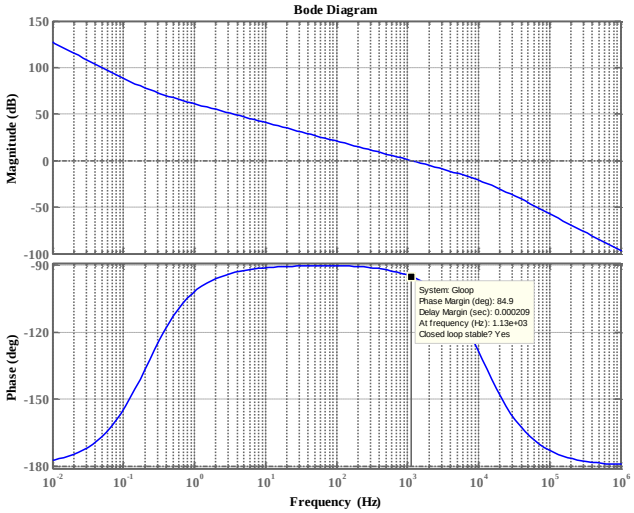


Figure 5.13 Bode plot of loop gain of current controller excluding the notch filter.

The bode plot of loop gain $G_{Loop,dq}(s)$ is shown in Figure 5.14.The attenuation at 100Hz with the inclusion of notch filter is -140dB and system is stable with bandwidth of 1100Hz and phase margin 92.2 degrees.

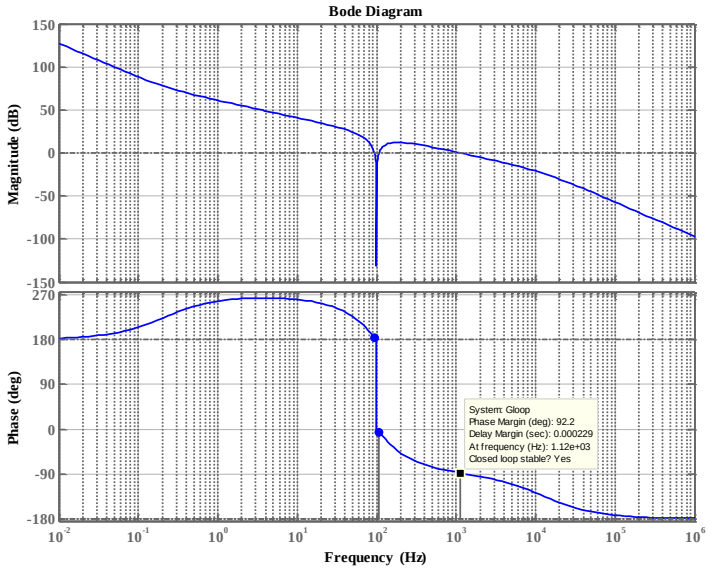


Figure 5.14 Bode plot of loop gain of current controller after the inclusion of notch filter.

5.3.5 Simulation results

The performance of zero sequence voltage injection for voltage control mode to maintain balanced voltage line voltage at PCC is verified by simulation. The complete system is modelled in the MATLAB-SIMULINK to validate the effectiveness of voltage control mode of D-STATCOM. In this section, the simulation results will be presented for regulating the line voltage (balanced) at PCC irrespective of a balanced dip or unbalanced in the supply voltage.

Table 5-1 System parameters for the simulation study.

Rating of D-STATCOM	2.5 KV(line-line), 500KVA
DC capacitors	4700µF each
Reference DC capacitor voltage reference (V^*_d)	1500V
Reference PCC (line-line)voltage	2.44 KV
filter inductor (L_C), filter capacitor (C_f)	2 mH, 20µF
Source impedance(Z_S)	$Z_{sa}= Z_{sb} = Z_{sc} =0.2+j13\Omega$
PCC loop controller gains	Kp=0.018,ki=20

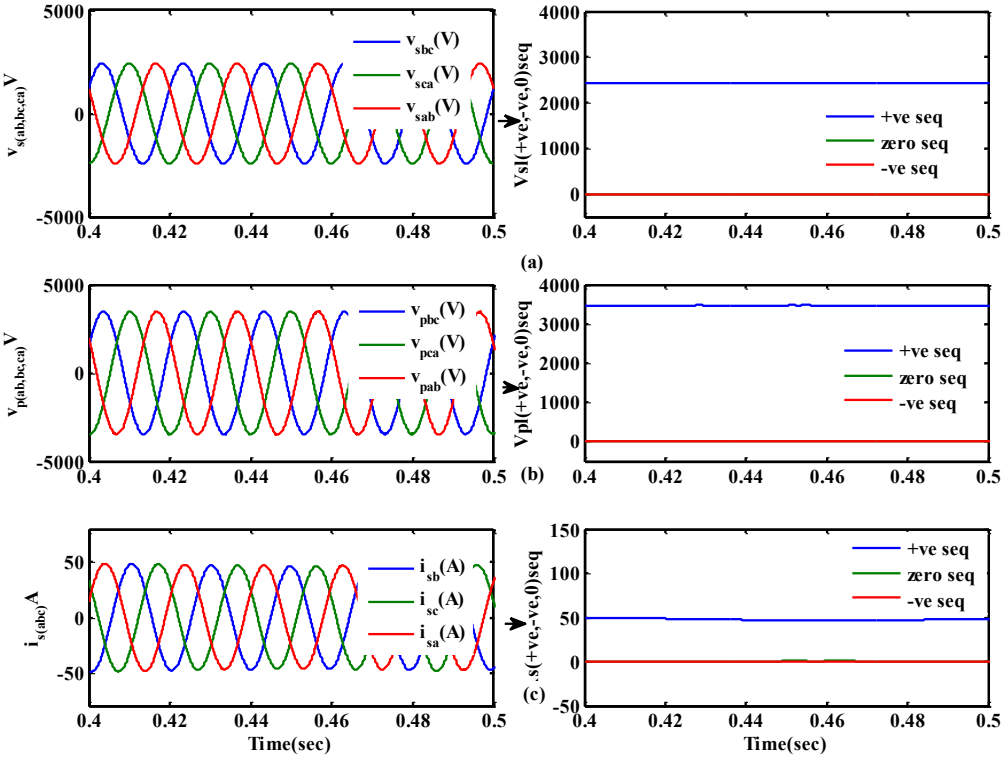


Figure 5.15 (a) Source line voltage and its sequence components (b) PCC line voltage and its sequence components (c) Source current and its sequence components.

The line voltage of source and its sequence components are shown in Figure 5.15(a) it can be observed that the source voltage is balanced with a peak value of 2.42 KV but it is desired to keep the balanced line voltage at PCC to be 3.46 KV. The D-STATCOM is operated in a voltage

control mode in order to track the line voltage at PCC to a reference value of 3.46 KV as shown in Figure 5.15(b) the source current flowing in this situation is 50 A(peak) which is seen in Figure 5.15(c).

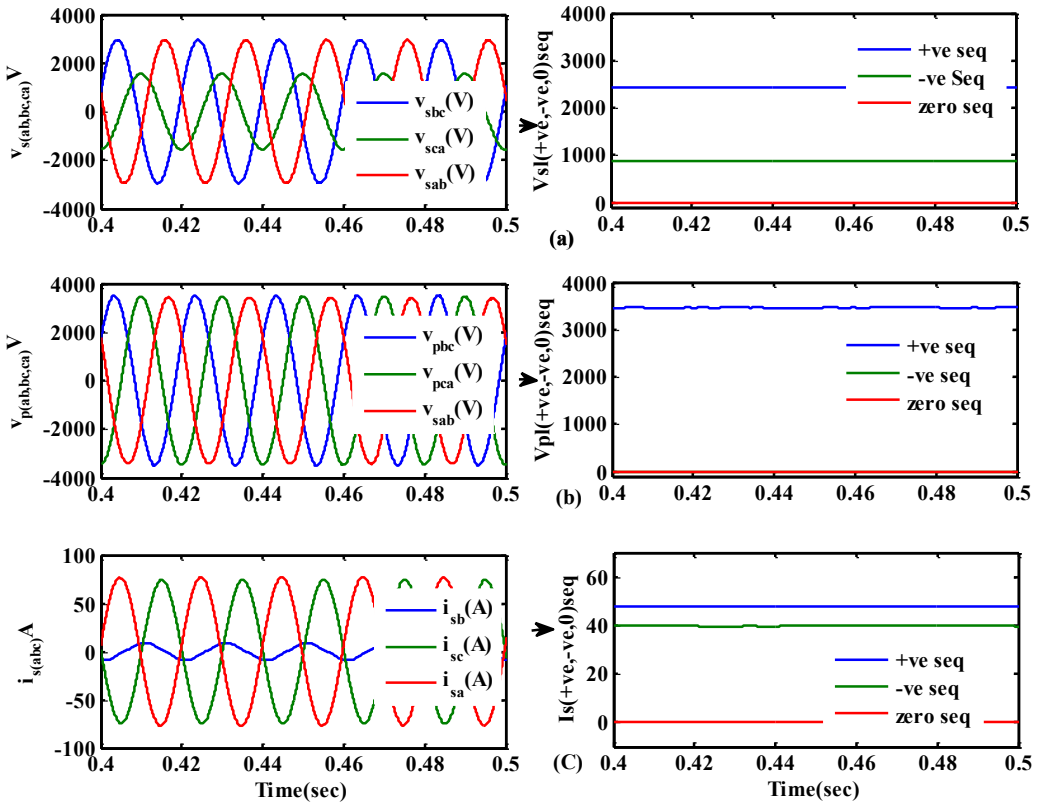


Figure 5.16 (a) unbalanced Source line voltage and its sequence components (b) PCC line voltage and its sequence components (c) Source current and its sequence components.

The source line voltage of source are unbalanced and its sequence components are shown in Figure 5.16(a) it is observed that the source voltage is unbalanced with a positive and negative sequence component value of 2.42 KV and 0.86KV respectively, but it is desired to keep the balanced line voltage at PCC to be 3.46 KV. The D-STATCOM is operated in a voltage control mode for driving the negative sequence component toward to zero and to track the line voltage at PCC to a reference value of 3.46 KV as shown in Figure 5.16(b) and the source current flowing in this situation is unbalanced with a positive and negative sequence component value of 47.7 A and 39.6 A respectively, which is seen in Figure 5.16(c). This unbalanced current can deviate the DC capacitor voltage so a zero sequence voltage is injected to balance this and the capacitor voltages can be observed in Figure 5.17. In order to put the line voltage at PCC to a reference value of 3.46 KV the source currents are of unbalanced, this leads to the capacitor voltages deviation in order to make the capacitor voltages to fallow the reference value of 1500 V the zero sequence voltage is need to be injected.

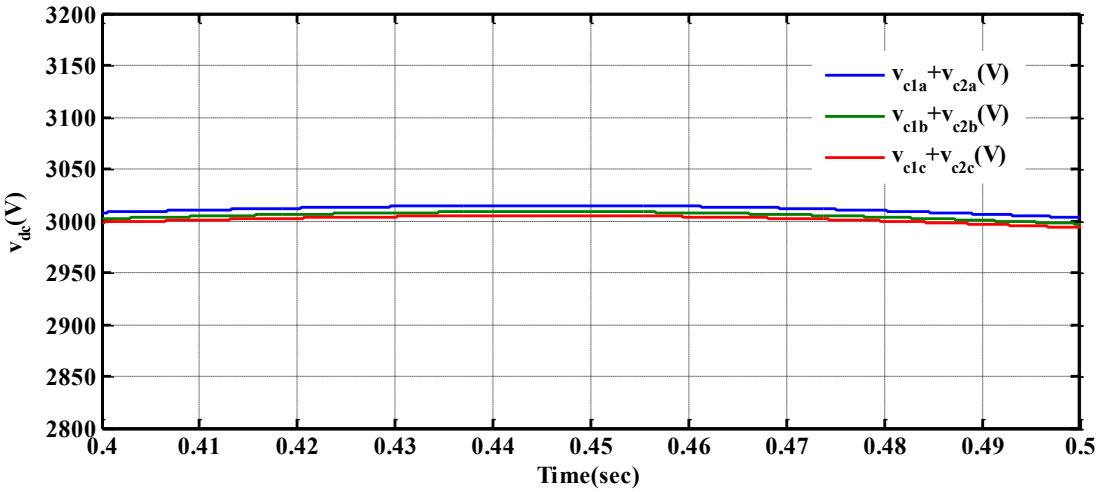


Figure 5.17 DC capacitor voltages after injection of zero sequence voltage.

5.4 Conclusion

The effectiveness of improved modulating signals for two H-bridges is investigated for voltage control mode of operation for single phase D-STATCOM. With the help of three phase D-STATCOM, it is shown that unbalance in line voltages can be taken care at PCC by injection of suitable currents to get balanced line voltages at PCC. While dealing with such situations it found that capacitor voltage vary over wide range, this problem is resolved by introducing zero sequence voltage in each phase. The effectiveness of this method is validated by detailed simulations results. The injected zero sequence voltage maintains the DC capacitor voltage in the SSBC converter to its reference value.

CHAPTER 6: SYSTEM DEVELOPMENT AND EXPERIMENTATION

[The system hardware, dSPACE–DS1006 interfacing and experimentation for the laboratory prototype models of the five-level CHB based D-STATCOM for single phase and 3P3W systems have been described in detail to validate the simulation results presented in previous chapters.]

6.1 Introduction

To verify and test different D-STATCOM systems as discussed in previous chapters, the following major issues are tested on the prototypes which have been developed in the laboratory.

1. Load compensation and DC capacitor voltage balancing in single-phase D-STATCOM.
2. Current controller performance of three-phase five-level SSBC based D-STATCOM.
3. Zero voltage regulation (ZVR) and unity power factor mode of D-STATCOM with unbalanced load.

A downscaled modular multilevel inverter rated at 100 V, 5 kVA has been designed and fabricated to verify the control objectives of D-STATCOM. It is important to note that the control algorithm developed in the earlier chapter is independent of the number of H-bridges. The power circuit of the SSBC based inverter consists of 24 switching devices having same voltage and current ratings. These 24 switching devices are used to realise 6 H-bridge cells and each cell is equipped with a galvanically isolated and floating dc capacitor without any power source. These 6 H-bridge cells are connected to form a three-phase inverter. As a result, it produces a five-level line-to-neutral and 9-level line-to-line voltage waveform. In this set-up, MOSFET (IRFP 460) have been used as the switching devices for realising the inverter. The other hardware components as required for the operation of the experimental set-up such as pulse amplification circuit, isolation circuit, dead-band circuit, voltage and current sensor circuits, non-linear/reactive loads have been designed and developed in the laboratory. The complete schematic diagram for the development of 3P3W D-STATCOM is shown in Figure 6.1 similarly for single phase D-STATCOM, 12 switching devices are used to realise 2 H-bridge cells and each cell is equipped with a galvanically isolated and floating dc capacitor.

A Digital Signal Processor (DSP) DS1006 of dSPACE has been used for the real-time simulation and implementation of control algorithm. By using the Real-Time Workshop (RTW) of MATLAB and Real-Time Interface (RTI) feature of dSPACE–DS1006, the Simulink models of

the various controllers of the prototypes have been implemented. The control algorithm is first designed in the MATLAB/Simulink software. The RTW of MATLAB generates the optimized C-code for real-time implementation. The interface between MATLAB/Simulink and Digital Signal Processor (DSP, DS1006 of dSPACE) allows the control algorithm to be run on the hardware. The master bit I/O is used to generate the required gate pulses and 20 Analog to Digital Converters (ADCs) are used to interface the sensed line currents, supply voltages and dc-bus capacitor voltages. An opto-isolated interface board is also used to isolate the entire DSP master bit I/O.

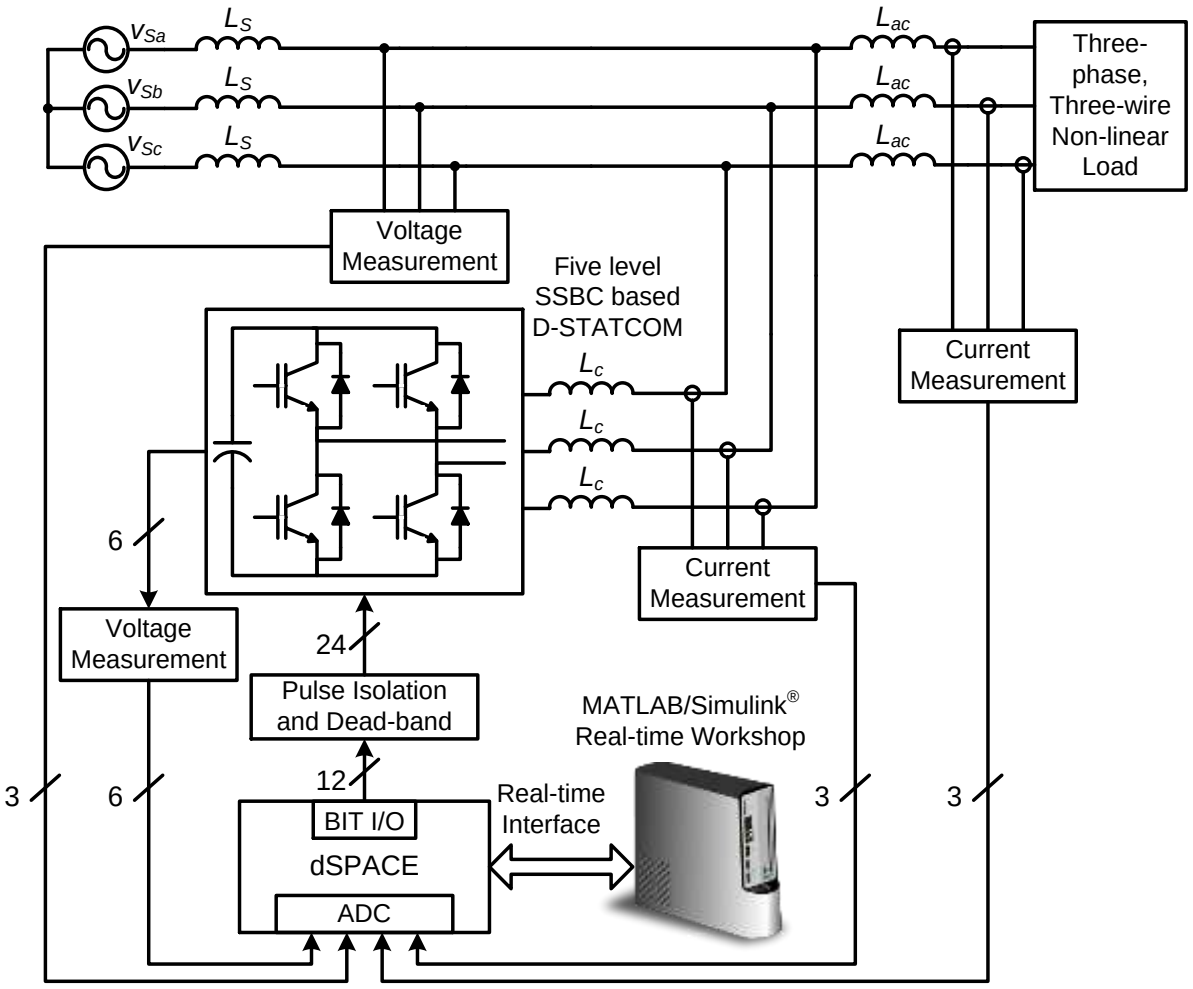


Figure 6.1 Schematic diagram for hardware implementation of SSBC based D-STATCOM.

6.2 Development of System Hardware

The developed experimental prototype comprises of the following parts:

1. Power circuit of 5- level single phase and three phase inverter
2. Measurement circuits

- Voltage measurement
- Current measurement

3. System software
4. Control hardware
    - MOSFET driver circuit for Isolation and Amplification
    - Dead-band circuit

6.2.1 Development of Power Circuit

A single-phase and three phase five level inverters which have been developed in the laboratory uses MOSFETs (IRFP460) switching device. To protect each switching device, a suitably designed snubber circuit is connected across it. The snubber comprises of a resistor and a capacitor connected across a Metal-Oxide Varistor (MOV). The devices are mounted on heat sinks to ensure proper heat dissipation.

6.2.2 Measurement Circuits

For the accurate and reliable operation of a system in closed loop, measurement of various system parameters and their conditioning is required. The measurement system must fulfil the following requirements:

- High accuracy
- Galvanic isolation with power circuit
- Linearity and fast response
- Ease of installation and operation

With the availability of Hall-effect current sensors and isolation amplifiers, these requirements are fulfilled to a large extent. In order to implement the control algorithm in closed loop, current and voltage need to be sensed.

6.2.2.1 Sensing of AC Current

The current have been sensed using the PCB-mounted Hall-effect current sensors (TELCON HTP50). The HTP50 is a closed loop Hall effect current transformer suitable for measuring currents up to 50 A. The current sensing circuit is shown in Figure 6.2.

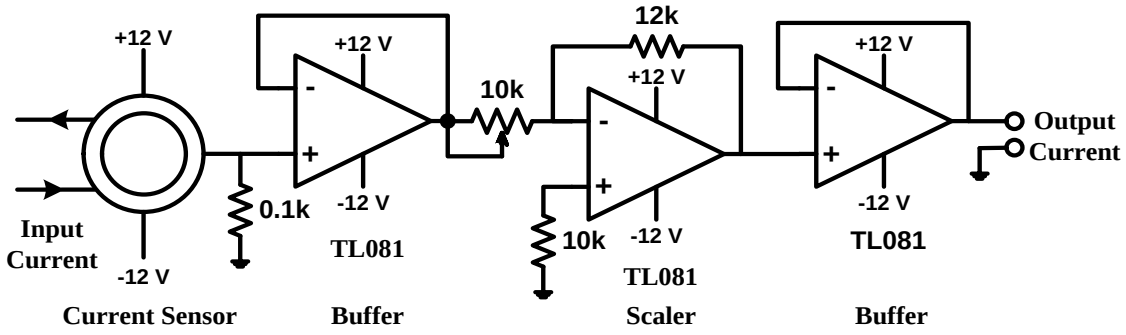


Figure 6.2 Current sensing circuit.

This device provides an output current into an external load resistance. These current sensors provide the galvanic isolation between the high voltage power circuit and the low voltage control circuit and require a nominal supply voltage of the range ±12V to ±15V. It has a transformation ratio of 1000:1 and thus, its output is scaled properly to obtain the desired value of measured current.

6.2.2.2 Sensing of Voltage

The voltages are normally sensed using isolation amplifiers and among them, AD202 is a general purpose, two-port, transformer-coupled isolation amplifier that can be used for measuring both AC and DC voltages. The other main features of the AD202 isolation amplifier are:

1. Small physical size
2. High accuracy
3. Low power consumption
4. Wide bandwidth
5. Excellent common-mode performance

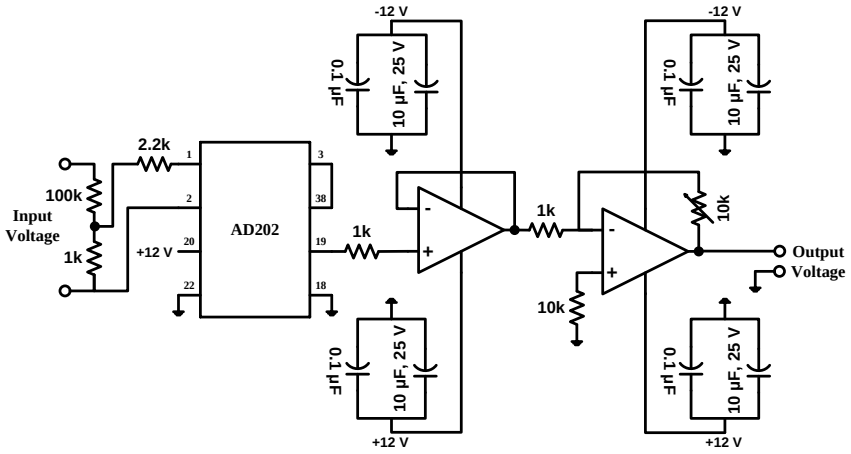


Figure 6.3 AC/DC voltage sensing circuit.

This voltage sensor can sense voltages in the range of ±1 kV (peak) and it requires a nominal supply voltage range of ±12V to ±15V. Figure 6.3 shows the circuit diagram for the voltage sensing scheme, which uses AD202 isolation amplifier. The voltage (AC or DC) to be sensed is applied between the terminals 1 and 2 (across a voltage divider comprising of 100 kΩ and 1 kΩ) and the voltage input to the sensor is available at the pins 1 and 2 of AD202 via a resistance of 2.2 kΩ. The isolated sensed voltage is available at the output terminal 19 of AD202. The output of voltage sensor is scaled properly to meet the requirement of the control circuit and is fed to the dSPACE via its ADC channel for further processing.

6.2.3 Development of System Software

Historically, control software were developed using assembly language. In recent years, industry began to adopt MATLAB/SIMULINK and Real-Time Workshop (RTW) platform based method, which provides a systematic approach to develop control software. Figure 6.4 shows the Total Development Environment (TDE) of dSPACE and its major component blocks are explained as below.

- MATLAB is widely used as an interactive tool for modeling, analysis and visualization of systems, which itself contains more than 600 mathematical functions and supports additional toolboxes to make it more comprehensive.
- Simulink is a MATLAB add-on software that enables block diagram based modeling and analysis of linear, nonlinear, discrete, and continuous and hybrid systems.
- RTW is Simulink add-on software that enables automatic C-code generation from the Simulink model. The generated optimized code can be executed on PC, microcontrollers, and signal processors.
- Real Time Interface (RTI) is add-on software of dSPACE which provides block libraries for I/O hardware integration of DS1006 R&D controller and generates optimized code for master and slave processors of the board.
- dSPACE's control desk is a software tool interfacing with real-time experimental setup and provides easy and flexible analysis, visualization, data acquisition and automation of the experimental setup. The major feature of real-time simulation is that the simulation has to be carried out as quickly as the real system would actually run, thus allowing to combine the simulation and the inverter (real plant).

The DSP DS1006 R&D controller board of dSPACE is a standard board that can be plugged into Peripheral Component Interconnect (PCI) slot of a desktop computer. The DS1006 is specially designed for the development of high-speed multivariable digital controllers and real-

time simulations for various applications. It is a complete real-time control system based on an AMD Opteron™ processor running at 2.6 GHz. It has 256 MB DDR-400 SDRAM local memory for the application and dynamic application data and 128 MB SDR SDRAM global memory for host data exchange. DS1006 R&D controller is a very good platform for the development of dSPACE prototype system for cost-sensitive RCP applications.

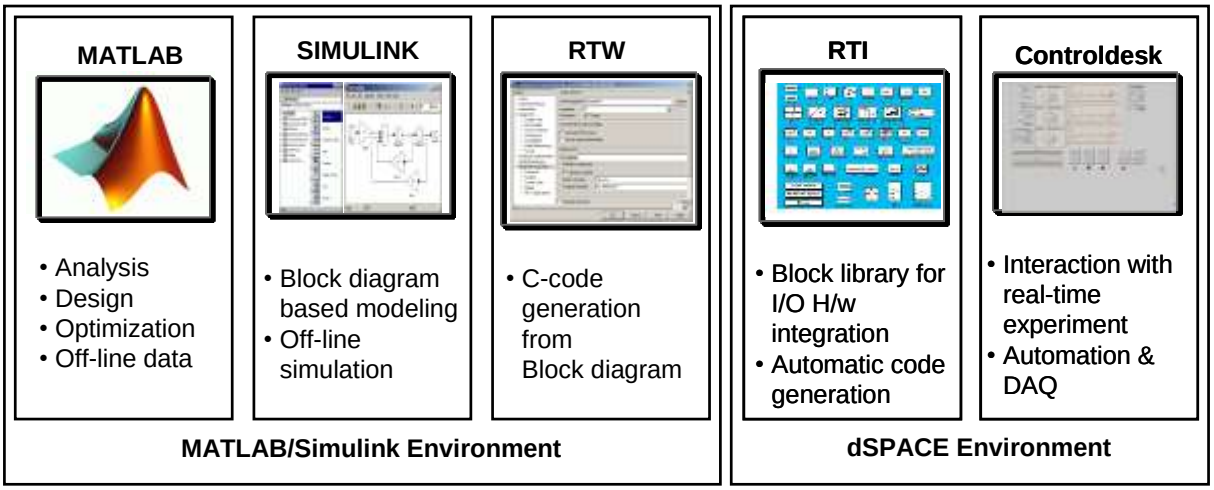


Figure 6.4 Total development environment of dSPACE with MATLAB.

It is used for the real-time simulation and implementation of the control algorithm in real-time. The sensed AC and DC voltages are fed to the dSPACE Multi-I/O Board (DS2201) of DS1006 via the available ADC channels on its connector panel. In order to add an I/O block (such as ADCs and master bit I/Os in this case) to the Simulink model, the required block is dragged from the dSPACE I/O library and dropped into the Simulink model of the SSBC based D-STATCOM system. In fact, adding a dSPACE I/O block to a Simulink model is almost like adding any Simulink block to the model. The master bit I/Os configured in the output mode, are connected to the model for issuing a gate pulse signal to the MOSFETs. In addition to that ADCs are connected to the model for giving different sensed parameter as input to the DSP hardware. Total development environment of dSPACE with MATLAB is presented in Figure 6.4.

The sensed signals of each topology are used for the processing in the designed control algorithm. The vital aspect for real-time implementation is the generation of real-time code of the controller to link the host computer with the hardware. For dSPACE systems, Real-Time Interface (RTI) carries out this linking function. Together with RTW from the Mathworks®, it automatically generates the real-time code from Simulink models and implements this code on the dSPACE real-time hardware. This saves the time and effort considerably as there is no need to manually convert the Simulink model into another language such as ‘C’. RTI carries out the necessary steps needing only addition of the required dSPACE blocks (I/O interfaces) to the

Simulink model. In other words, RTI is the interface between Simulink and various dSPACE platforms. It is basically the implementation software for single-board hardware and connects the Simulink control models to the I/O of the board. In the present case, the optimized C-code of the Simulink model of the control algorithm is automatically generated by the RTW of MATLAB in conjunction with RTI of dSPACE.

The generated code is then automatically downloaded into the dSPACE hardware where it is implemented in real-time and the gating signals are generated. The gating pulses for the power switches of the converter are issued via the Master-bit I/Os available on the dSPACE board. The DS2201 Connector/LED combo panel provides easy-to-use connections between DS1006 board and the devices to be connected to it. The panel also provides an array of LEDs indicating the states of digital signals (gating pulses). The gating pulses are fed to various power devices driver circuits via dead-band and isolation circuits. Figure 6.5 shows the schematic diagram of dSPACE-DS1006 board interfaced with the host computer and the real-world plant (power circuit of SSBC based inverter system). Sensed signals are fed to the ADCs and generated gating pulses are given at Master bit I/Os.

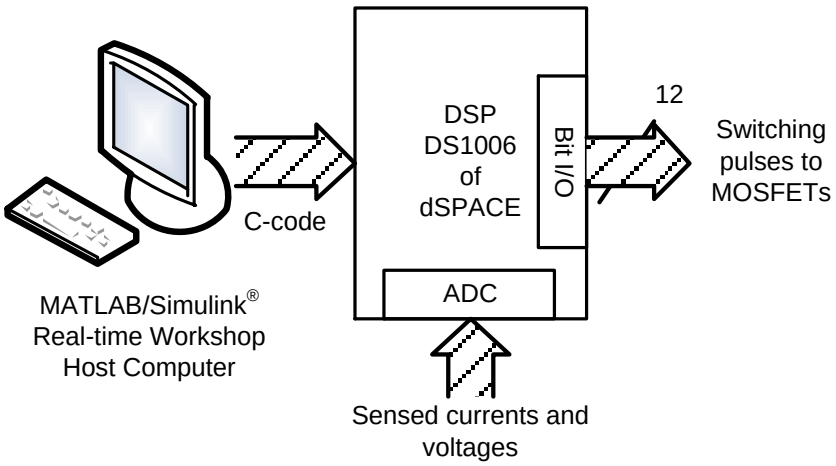


Figure 6.5 DSP (dSPACE-DS1006) circuit board interfacing.

6.2.4 Development of Control Hardware

The control algorithm is designed and built into the MATLAB/Simulink software and the control pulses for the power switches of SSBC based D-STATCOM system are generated by real-time simulation using the DSP of dSPACE. The optimized C-code of the Simulink model of control algorithm is generated with the help of Real-Time Workshop (RTW) of MATLAB. The RTW of MATLAB and the Real-Time Interface (RTI) of dSPACE result in the real-time simulation of the model. The control pulses are generated at the various Master-bit I/Os of the dSPACE which are interfaced with the MOSFET driver circuits through isolation and dead-band circuits.

This ensures the necessary isolation of the dSPACE hardware from the power circuit that is required for its protection. Figure 6.6 shows the basic schematic diagram of interfacing firing pulses from the dSPACE board to switching devices of inverter. From Figure 6.6, it can be observed that the following hardware circuits are required for interfacing of inverter with dSPACE board.

1. Dead-band circuit
2. MOSFET driver circuits for isolation and amplification

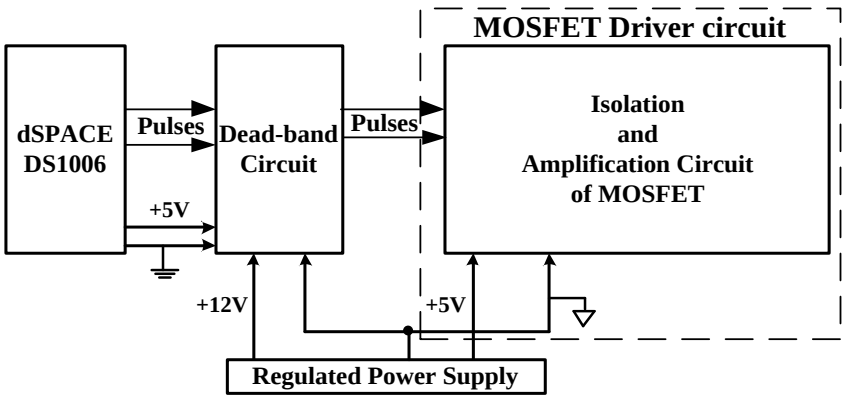
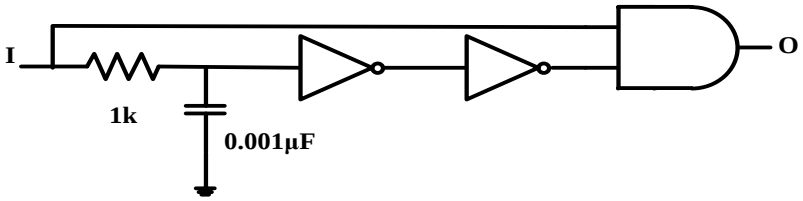


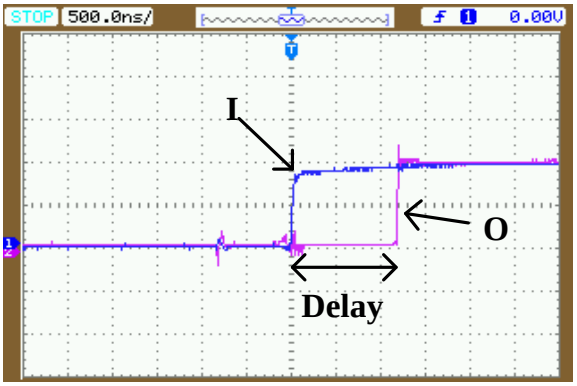
Figure 6.6 Schematic diagram of interfacing firing pulses from dSPACE controller board to switching devices.

6.2.4.1 Dead-band Circuit

A dead-band (dead-time or delay) circuit is employed to provide a delay time (of about 1 μs) between the switching pulses to the devices connected in the same output leg of the inverter. This is required to avoid the short circuit of devices in the same leg of the output phase due to simultaneous conduction. The delay time circuit is shown in Figure 6.7.



(a)

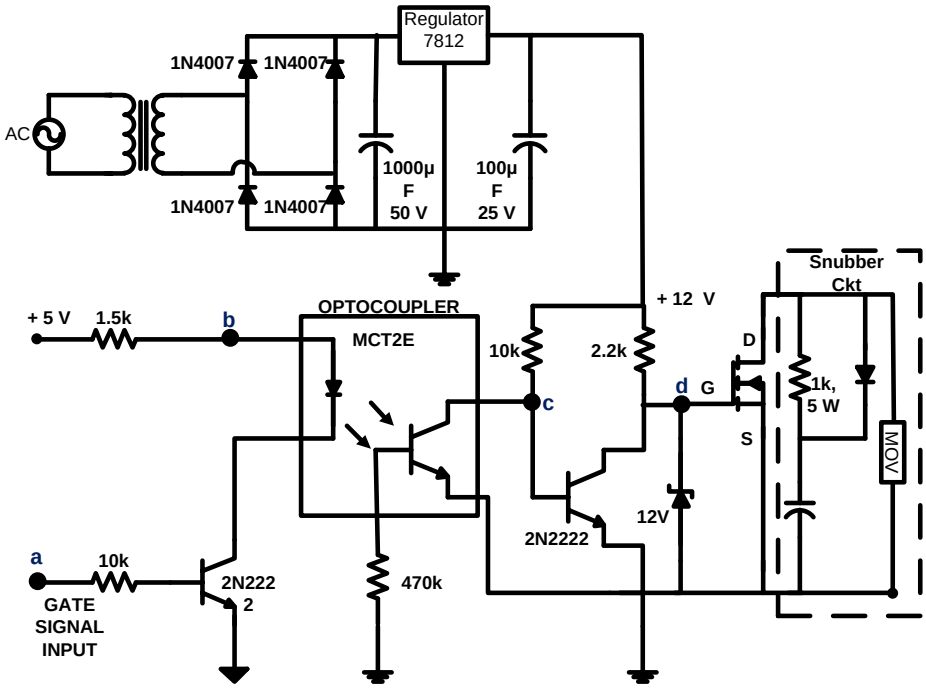


(b)

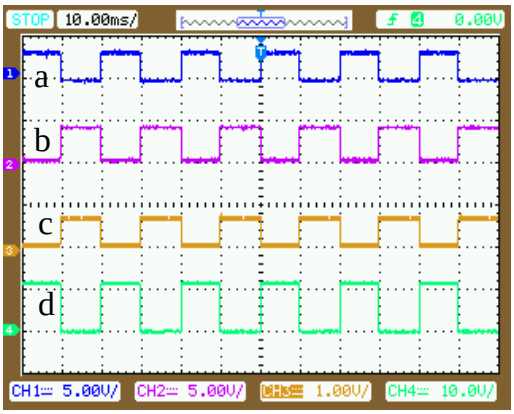
Figure 6.7(a) Dead-band circuit (b) Input-output waveform.

6.2.4.2 MOSFET Driver Circuit

The MOSFET driver circuit is used for pulse amplification and isolation purposes. The control pulses generated from dSPACE unit are not efficient to drive the switching devices. Thus, these signals are further amplified by using proper amplifier circuit. Figure 6.8 (a) shows a circuit diagram of pulse isolation and amplifier circuit for MOSFET driver circuit. For isolation between power circuit and a control circuit, an opto-coupler (MCT2E) is used.



(a)



(b)

Figure 6.8 (a) MOSFET driver circuit (b) Waveform at points a (channel 1), b (channel 2), c (channel 3) and d (channel 4).

Although common + 5V, regulated DC power supply is used at the input side of the opto-coupler, but individual regulated DC power supply of +12V is used to connect the output side of opto-coupler. When the input gating is +5V level, the transistor saturates, the LED conducts and the light emitted by provided by the output amplifier transistor 2N2222. In order to test the MOSFET driver, a PWM signal is applied at point 'a' of Figure 6.8 (a) and waveforms at different points (a, b, c and d) are recorded as shown in Figure 6.8 (b). It is observed that the waveform at point 'd' is similar to the PWM it falls on the base of the phototransistor, thus forming its base drive. The pulse amplification is signal applied at point 'a', but its amplitude is increased to 12 V which is used to drive the MOSFET.

6.3 Experimental validation of single phase D-STATCOM

The power circuit prototype made with MOSFET switches is shown in Figure 6.9, this model have been tested in the laboratory to experimentally validate the simulation results. Each MOSFET shown in this prototype is associated with driver and snubber circuit as shown in Figure 6.8(a).The experimental analysis consists of the following two sections includes the comparison of control theories under source voltage distortion and the improved modulating signal method for capacitor voltage balancing.

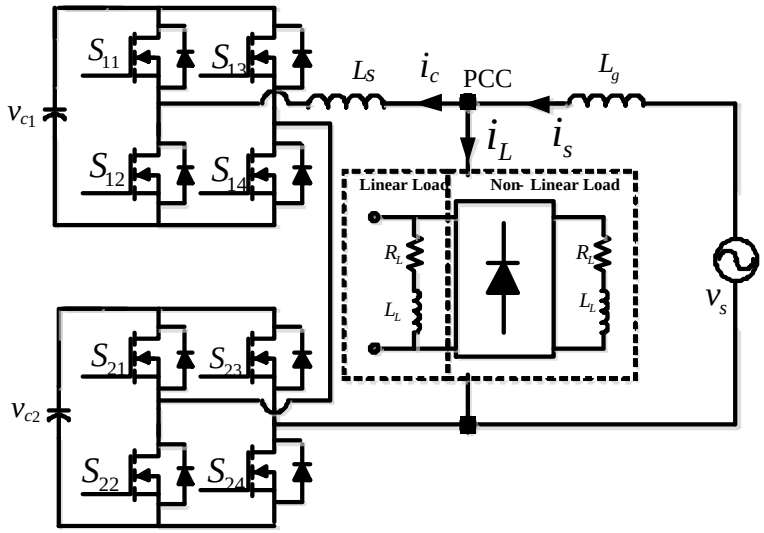


Figure 6.9 Schematic of experimental prototype for Single phase D-STATCOM.

6.3.1 Performance of single phase D-STATCOM for load compensation

The performance of the modified and original single phase pq theories is tested with linear RL and non-linear load, under distorted supply voltage. The distortion in the voltage is introduced by connecting an inductive impedance in the line fallowed by a non-linear load, and the voltage available at this point is then considered as the supply voltage for the single phase D-STATCOM with a THD of 21%. The generation of reference currents by using modified and original single phase pq theories is discussed in the chapter-3. Here experimental results are verified with the downscaled simulation results with the parameters given in Table 6-1.

Table 6-1 Prameters used for experimental validation for Single phase D-STATCOM

Parameter	**Values used in experimentation**
Source voltage	25V,50 Hz
DC bus reference voltage of D-STATCOM	25 V (for each capacitor in the H-bridge cell)
DC bus capacitance of D-STATCOM	2200 μF
D-STATCOM coupling inductor	L_c =2 mH
Commutation inductance	L_f = 1 mH
PWM switching frequency	2 kHz
PI controller parameters for voltage controller	Kp=0.8, Ki=10
Load	R=10 Ω L=10 mH
Sampling time	T_s = 80 μs.

Figure 6.10 and all the subsequent figures in this section shows the similar waveforms the part (a) of each figure consists of four traces namely

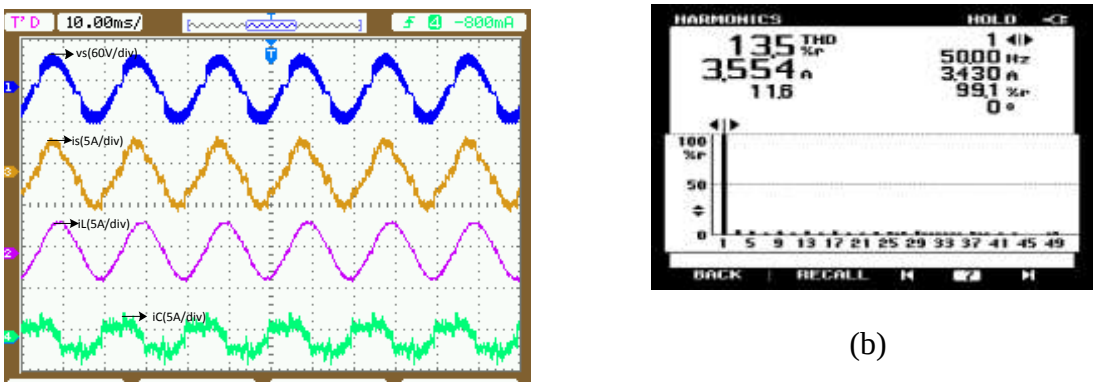
Trace 1: source phase voltage (v_s)

Trace 2: Source current (i_S)

Trace 3: load current (i_L)

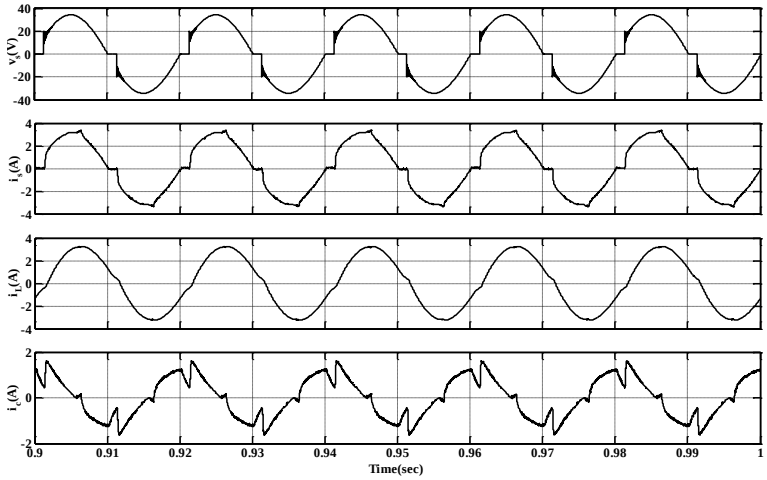
Trace 4: D-STATCOM current (i_C)

and part (b) consist of harmonic spectrum of source current. Figure 6.10-Figure 6.13 shows the performance of D-STATCOM for a linear load with modified and original single phase pq theories. Here the load current is slightly distorted because of the distortion in the source voltage. The experimental waveforms are in good agreement with the simulation results, however there is slight variation in the THD results of the source current. The source current THD with modified pq theory is (3.5 % in experimentation and 1.44% in simulation) is much lower compared to original pq theory (13.5 % in experimentation and 10.64% in simulation).

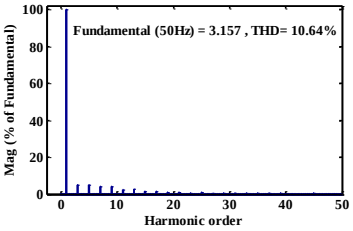


(a) (b)

Figure 6.10 Experimental Performance of single phase D-STATCOM for linear load compensation with orginal 1-phase pq theory.

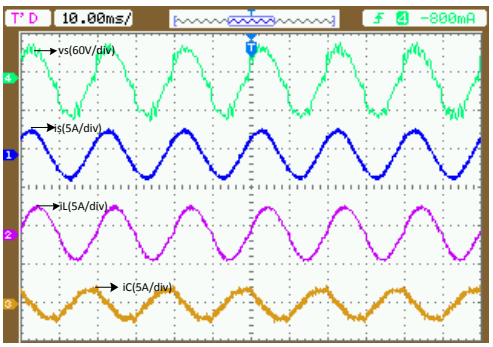


(a)

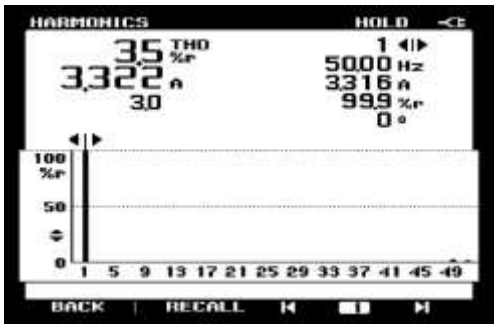


(b)

Figure 6.11 Simulation result of single phase D-STATCOM for linear load compensation with original 1-phase pq theory.

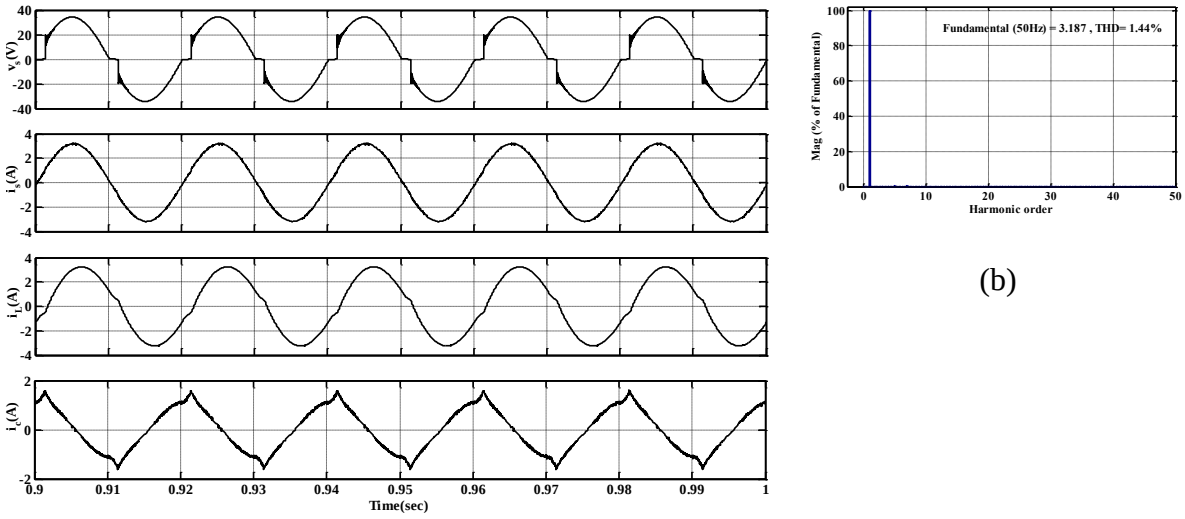


(a)



(b)

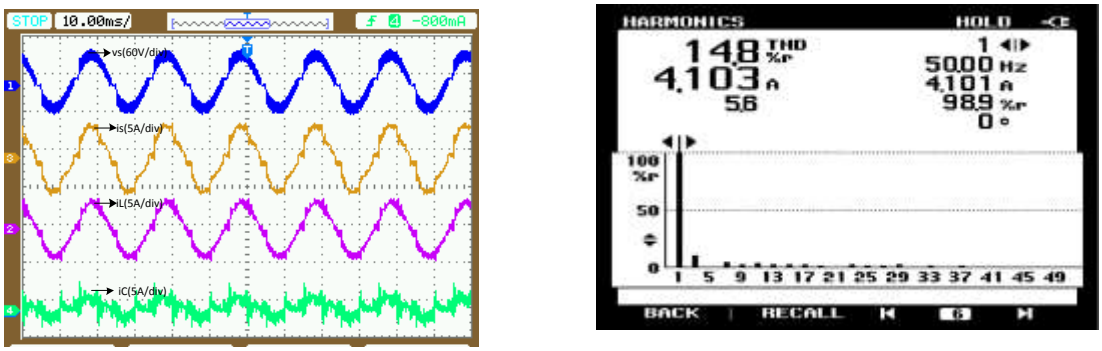
Figure 6.12 Experimental Performance of single phase D-STATCOM for linear load compensation with modified 1-phase pq theory.



(a) (b)

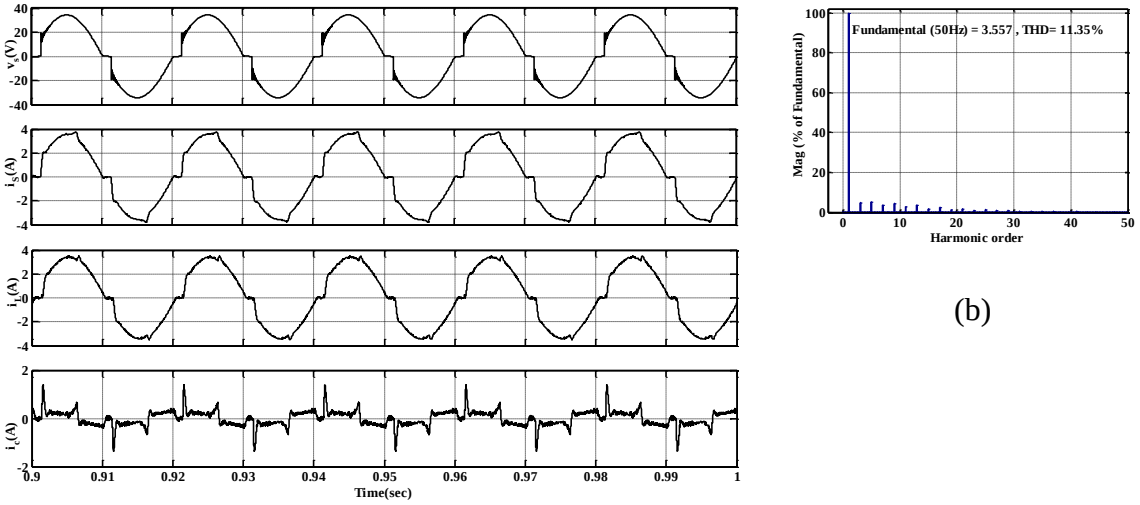
Figure 6.13 Simulation result of single phase D-STATCOM for linear load compensation with modified 1-phase pq theory.

Figure 6.14-Figure 6.17 shows the performance of D-STATCOM for a nonlinear load with modified and original single phase pq theories. The nonlinear load is realized in the laboratory with bridge rectifier feeding resistive load. The load current is having distortion. The experimental waveforms are in good agreement with the simulation results, however there is slight variation in the THD results of the source current. The source current THD with modified pq theory (4.7 % in experimentation and 2.61% in simulation) is much lower compared to original pq theory (14.8 % in experimentation and 11.35% in simulation).



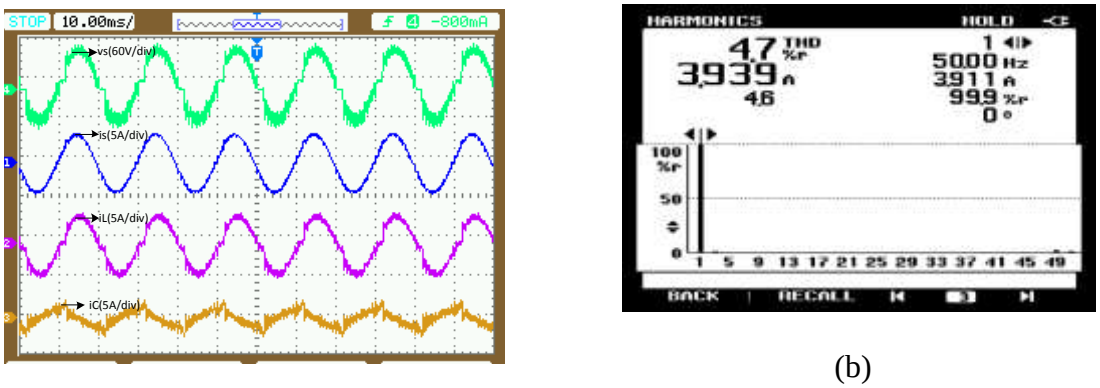
(a) (b)

Figure 6.14 Experimental Performance of single phase D-STATCOM for non-linear load compensation with original 1-phase pq theory.



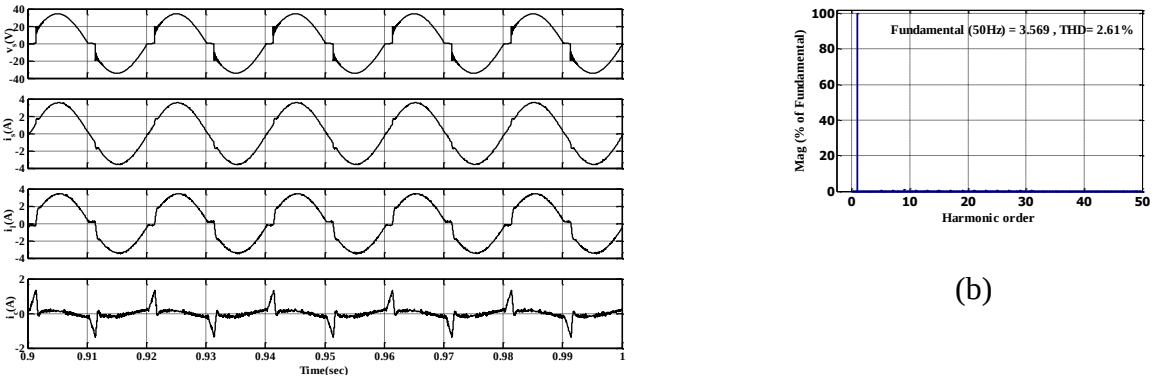
(a) (b)

Figure 6.15 Simulation result of single phase D-STATCOM for non-linear load compensation with original 1-phase pq theory.



(a) (b)

Figure 6.16 Experimental Performance of single phase D-STATCOM for non-linear load compensation with modified 1-phase pq theory.



(a) (b)

Figure 6.17 Simulation result of single phase D-STATCOM for non-linear load compensation with modified 1-phase pq theory.

Table 6-2 Source current THD(%) in simulation and experimentation with orginal and modified single phase control theories.

		Source current THD in (%)	
		Original single phase pq theory (OSPQ)	Modified single phase pq theory (MSPQ)
Linear load	Simulation	10.64	1.44
	Experimentation	13.9	3.5
Non-linear load	Simulation	11.35	2.61
	Experimentation	14.8	4.7

Table 6-2 gives the summary for the performance of single phase D-STATCOM with different control theories. It is clear from this table that the modified pq theory gives improved results and it is possible to achieve the source current THD much lower than the source voltage THD. So the modified pq theory should be used when the source voltage is non-sinusoidal.

6.3.2 Performance of improved modulating signal method

To validate the effectiveness of improved modulating technique for capacitor voltage balancing a hardware prototype is developed. From device safety point of view, the results have been obtained at reducing grid voltage 25V with a coupling inductance of 3 mH and DC voltage reference of each H-bridge is set at 25 V. The phase shifted pulse width modulation is used as a PWM technique with a carrier frequency of 2 KHz. Four AD202JN voltage sensors are used in the experimentation to sense a grid voltage, two DC capacitor voltages, and CHB output voltage. One current sensor TELCON HTP-25 is used to sense the source current. The uneven power loss situation is created by connecting a resistance of 80 Ω across the H1-bridge. Figure 6.19(a) shows the DC capacitor voltages, grid voltage and grid current with the auxiliary control loop current (5 A peak) leading the grid voltage (25 V). The waveforms of STATCOM capacitor voltages of both the H-bridges are seen to follow the reference voltage when improved modulating signals obtained from auxiliary loop are used. Figure 6.19(b)-(c) show the capacitor voltage dynamics of the H-bridges with removal and application of auxiliary loop respectively. In, Figure 6.19(b) initially the auxiliary control loop is active and it is deactivated at other instant of time. The capacitor voltages are observed to be moving away from the reference value, which

clearly demonstrates the effectiveness of proposed auxiliary control loop. Similarly, Figure 6.19(c) shows the effect of application of auxiliary control loop, where the capacitor voltages start to converge towards the reference value of 25V. The Figure 6.19(d)-(e) show the effect of capacitor voltage unbalance on the D-STATCOM output voltage. In Figure 6.19(d), as the capacitor voltages start to deviate from the reference value, the five-level D-STATCOM output voltage becomes three level. The zoomed out portion of output voltage waveform is also shown in the same figure. In Figure 6.19(e), when the capacitor voltages are balanced, the output of D-STATCOM has five levels, which is clearly seen in lower trace of the same figure. The experimental results of this improved modulating signal method are found to match with the downscaled simulation result of Figure 6.18.

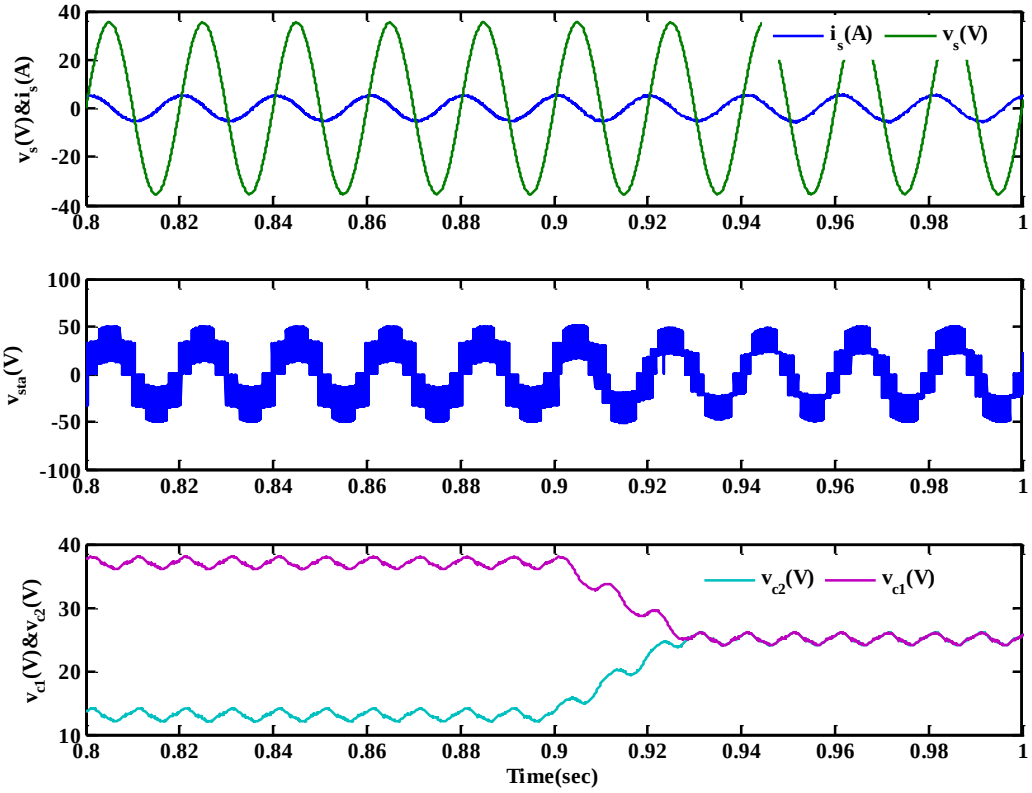
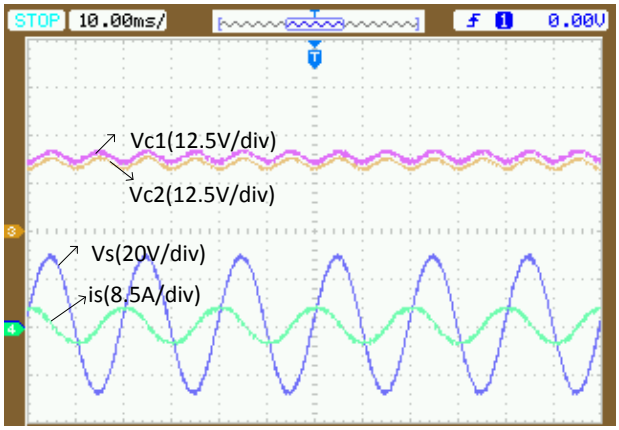
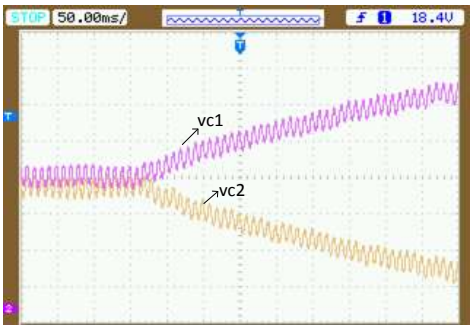


Figure 6.18 Simulation result of the performance of improved modulating signal method.



(a)



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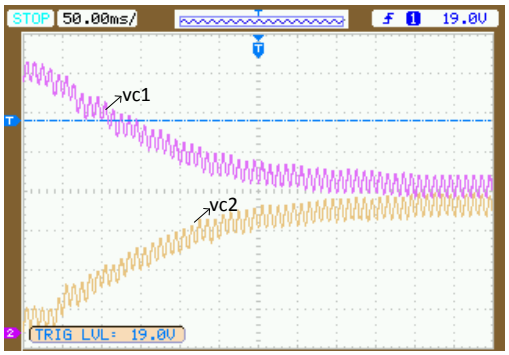

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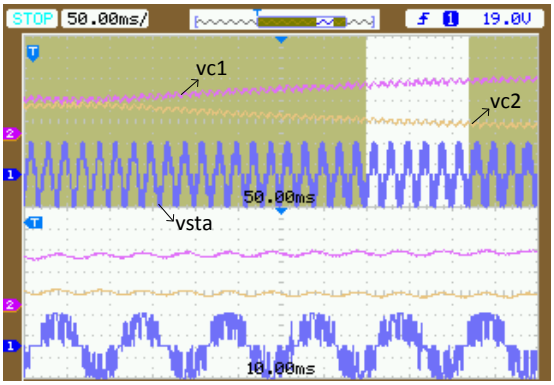

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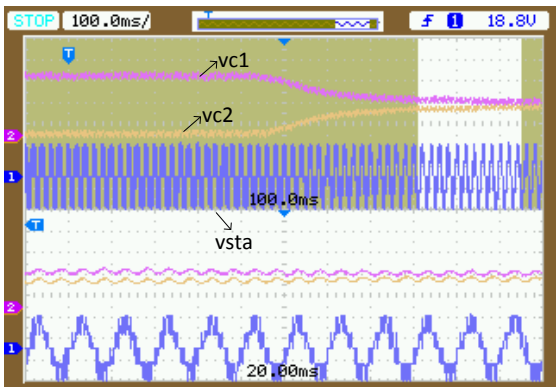


(e)

Figure 6.19 Performance of single phase D-STATCOM with improved modulating signal method

6.4 Three-phase modular D-STATCOM current controller performance

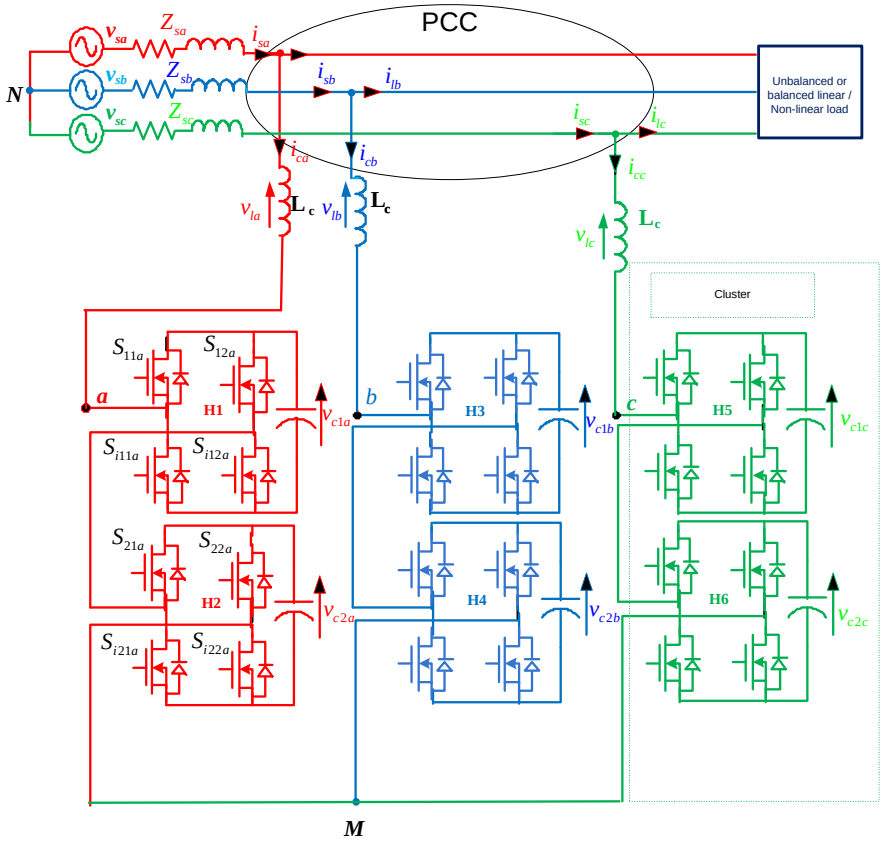
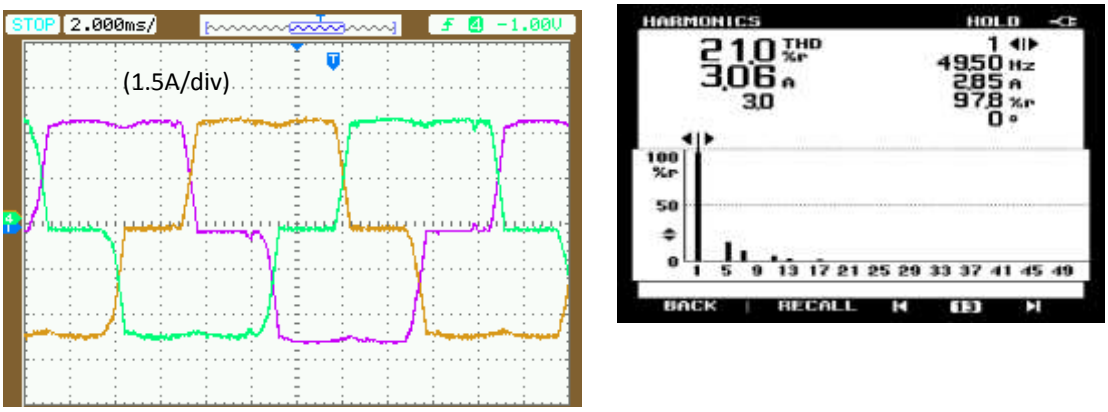


Figure 6.20 Schematic of experimental prototype for SSBC based D-STATCOM

In this experimental study the developed prototype inverter as shown in Figure 6.20 has been used as a D-STATCOM, to verify the current controller performance for harmonic elimination of a bridge rectifier load. In D-STATCOM implementation, each H-bridge cell is equipped with a floating dc capacitor. D-STATCOM is connected to the PCC with series connected coupling inductor in each output phase of the inverter. The synchronous reference frame (SRF) based PI, PI with resonant controller of the D-STATCOM has been implemented in dSPACE.The uncontrolled rectifier with *RL* elements on their dc side have been used as a nonlinear load. For this purpose, a three-phase uncontrolled diode bridge rectifier have been developed in the laboratory. A snubber circuit is also connected across each device for protection of semiconductor devices. Each device has been mounted on suitably designed heat sink to ensure proper heat dissipation. The parameters used for experimental validation are given in Table 6-3. The relevant discussions for these experimental and simulation studies are given below. Figure 6.21(a) shows the typical three-phase load currents drawn by this rectifier.

The currents drawn by the rectifier are non-sinusoidal. The harmonic spectrum of the phase–*a* load current is shown in Figure 6.21(b), which contains significant amounts of 5^{th}, 7^{th}, 11^{th} and 13^{th} order harmonics with resulting THD of 21%.



(a) (b)

Figure 6.21Performance of uncontrolled rectifier with RL-load on its dc side: (a) Three-phase load currents; (b) Harmonic spectrum of phase–a load current.

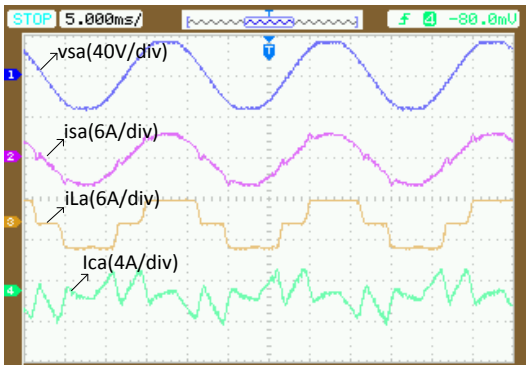
Table 6-3 Parameters used for the experimental validation of 3P3W D-STATCOM.

Parameter	**Values used in experimentation**
AC line parameters (phase voltage)	25V,50 Hz
DC bus reference voltage of D-STATCOM	25 V (for each capacitor in the H-bridge cell)
DC bus capacitance of D-STATCOM	2200 µF
D-STATCOM coupling inductor	L_c = 3 mH
Commutation inductance	L_f = 1 mH
PWM switching frequency	2 kHz
PI controller parameters for voltage controller	Kp=0.8, Ki=10
Current PI controller, Resonant controller	Kp=100, Ki=400, Kr=600
Load	Three-phase uncontrolled rectifier with *RL* load
Sampling time	T_s = 80 µs.

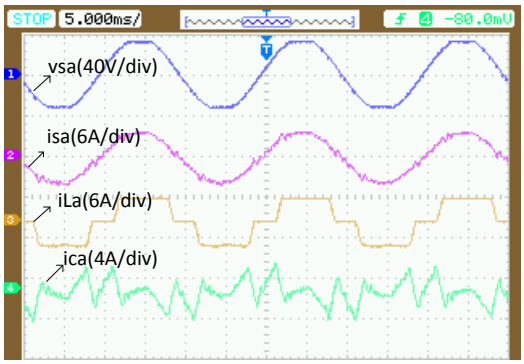
The developed D-STATCOM has been tested to eliminate the harmonics produced by this nonlinear load. The current controller is realized with PI and PI with resonant controller, the experimental waveforms under steady state condition with normal source voltage are shown in Figure 6.22. The source voltage, source current after compensation, load current and compensating currents for phase–*a* with PI and PI with resonant controller are shown in Figure 6.22(a) and Figure 6.22(b) respectively. As a three-phase balanced load has been considered, the results corresponding of only phase–*a* are shown here only. The harmonic spectra of source

currents after compensation with PI and PI with resonant controller are shown in Figure 6.22(c) and Figure 6.22(d) respectively. The experimental results presented in Figure 6.22 are observed to be in good agreement with downscaled simulation results shown in Figure 6.23. From Figure 6.22 the following quantitative observations have been made:

After compensation with D-STATCOM, the load current having 21% THD, the source current THD is reduced to 5.9% and 4% with PI and PI with resonant controller respectively. These %THD values of source currents after compensation are well within the limits of IEEE–519–1992 standard. At the similar conditions of experimental values the simulation results are shown in Figure 6.23, it is observed that the steady state waveforms of both the experimental and simulation results with PI and PI with resonant controllers are similar but the THD of source current is different. The results of THD are given in Table 6-4, where it is observed that in case of PI with resonant controller source current THD is lower both for simulation and experiment over to a PI controller.



(a)



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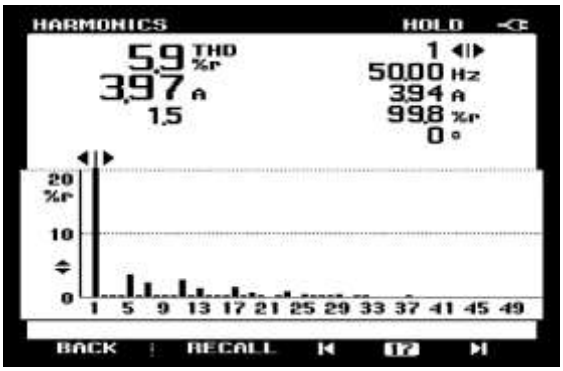

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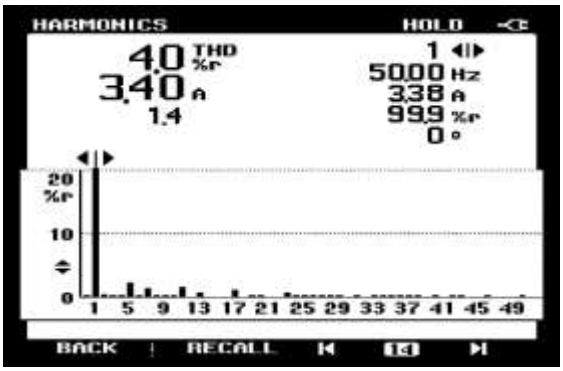


(d)

Figure 6.22 Experimental results of 3P3W D-STATCOM for an RL-load on the dc side of an uncontrolled rectifier with PI and PI with resonant current controller.

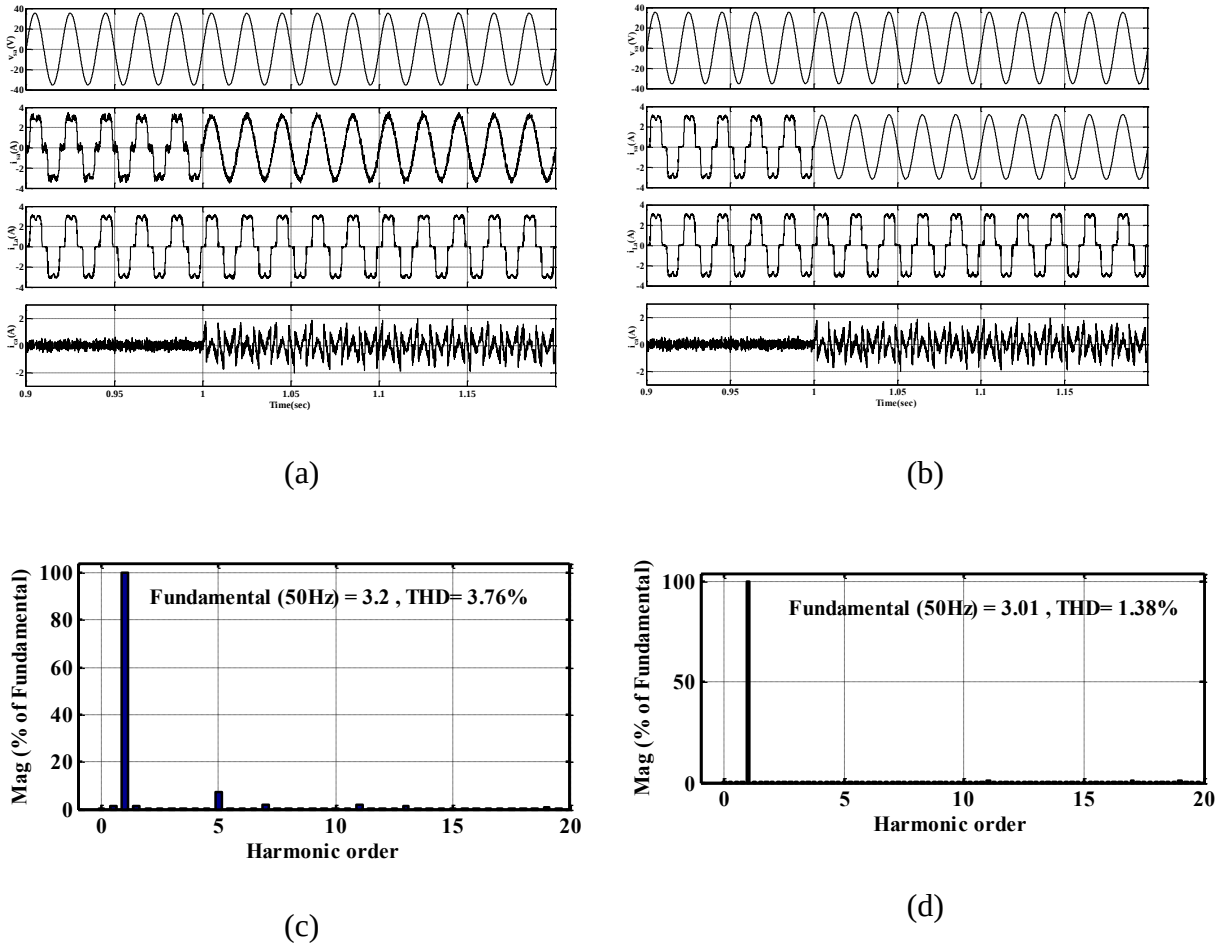


Figure 6.23 Dounscaled simulation results of 3P3W D-STATCOM for an RL-load on the dc side of an uncontrolled rectifier with PI and PI with resonant current controller.

Table 6-4 Source current THD(%) in simulation and experimentation with PI and PI with resonant controller.

	Source current THD (%)	
	PI	PI with resonant controller
Simulation	3.76	1.38
Experimentation	5.97	4.0

6.5 Experimental verification of UPF and ZVR modes of D-STATCOM

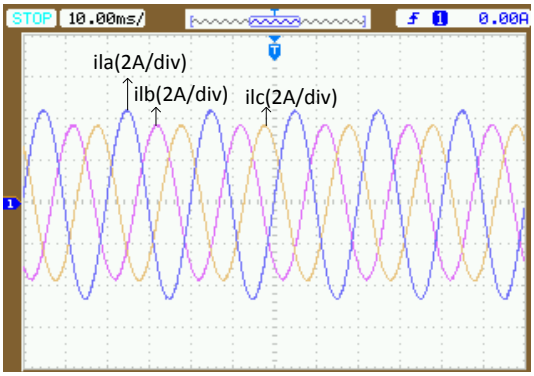
The developed D-STATCOM has been tested for zero voltage regulation mode and unity power factor mode. The three phase load considered here a unbalanced linear load. The individual and zero sequence voltage injection algorithm are developed along with the operating mode of D-

STATCOM, the experimental waveforms under transient and steady state condition with normal source voltage are shown in Figure 6.24 and Figure 6.26. The Experimental parameters are given in Table 6-5.

Table 6-5 System parameters for Experimental study.

Parameter	**Value**
AC line parameters	Three-phase, three-wire, 50 V, 50 Hz
DC bus voltage of D-STATCOM	40 V (for each capacitor in the H-bridge cell)
DC bus capacitance of D-STATCOM	2200 μF, 450 V (for each capacitor in the H-bridge cell)
Source impedance	Zs= j5Ω(ZPF), Ls=1mH
D-STATCOM coupling inductor	L_c = 2 mH
PWM switching frequency	2 kHz
PI controller parameters for voltage controller	Kp=0.8,Ki=10
Current PI controller	Kpi=100, Kii=400
Unbalanced linear Load	Z_a=5+j4Ω, Z_b=9+j12Ω, Z_c=5+j11 Ω.
Sampling time	T_s = 80 μs.

Figure 6.24(a)-(e) shows the experimental results with the injection of zero sequence voltage and after the activation of UPF mode. The Figure 6.24 (a)-(c) shows 3-phase current waveforms for load, D-STATCOM and source respectively. Figure 6.24(a) it is observed that even though the load current is unbalanced in UPF mode with a peak value of 4.5 A, 3.5 A, 3.5 A, the source current are balanced with a peak value of 2.5 A in each phase as shown in Figure 6.24(c). The D-STATCOM currents are also unbalanced with a peak value of 3.6 A, 3.5 A, 2.8 A shown in Figure 6.24(b). These unbalanced D-STATCOM currents are generated by the control strategy to balance the source currents. To supply these unbalanced currents from D-STATCOM, the capacitor voltages should be properly regulated, for which a zero sequence voltage is injected. When this zero sequence voltage is used in the control strategy, the DC capacitor voltage waveforms as seen in Figure 6.24(e) are to be closely regulated and follow the reference value of 40V. The Figure 6.24(d) shows the response of phase voltage and source current when the UPF mode is activated, the source current is in-phase with the source voltage. With the same experimental parameters simulation results are shown in Figure 6.25 it is observed that these results are exactly matched with the experimental results of Figure 6.24.



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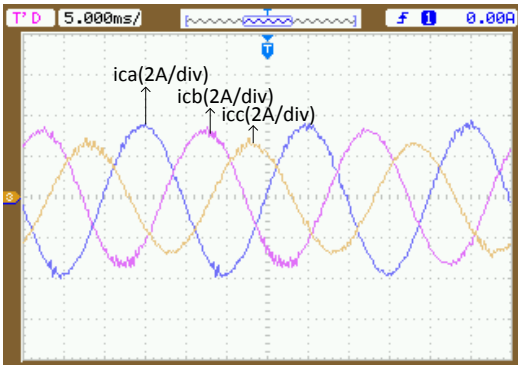

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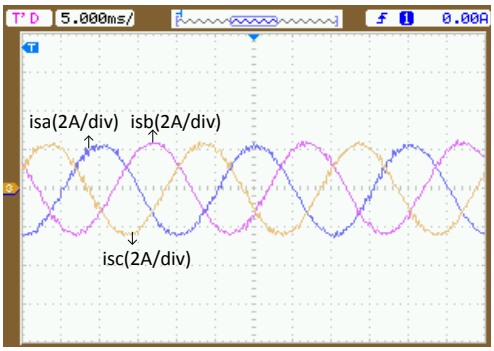

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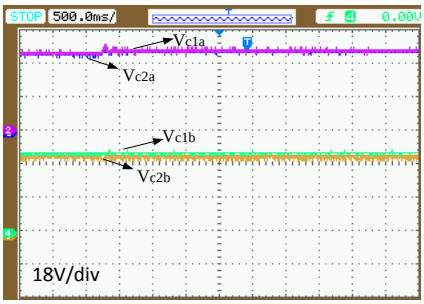


(e)

Figure 6.24 Performance of D-STATCOM under UPF mode with individual voltage balancing and zero sequence voltage injection.

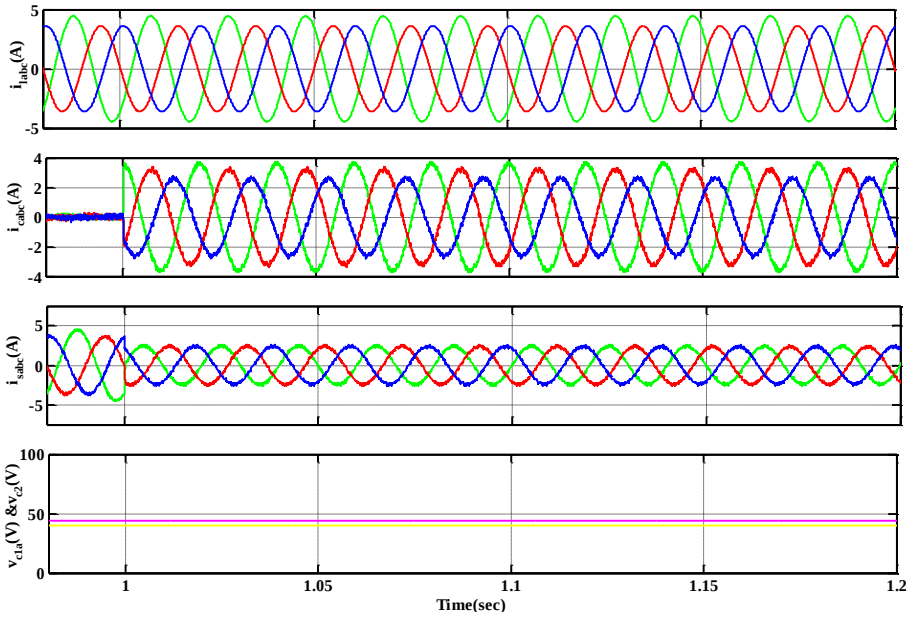
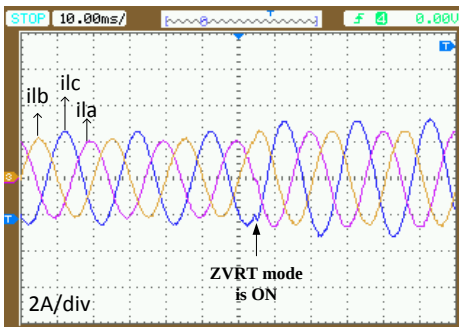
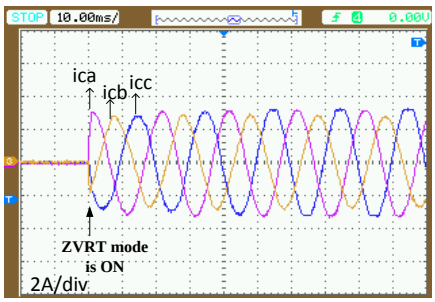


Figure 6.25 Simulation result of D-STATCOM for UPF mode.

Figure 6.26(a)-(e) shows the experimental results with the injection of zero sequence voltage and after the activation of ZVR mode. The Figure 6.26(a)-(c) shows 3-phase current waveforms load, D-STATCOM and source respectively. Figure 6.26(a) it is observed that even though the load current is unbalanced after ZVR mode is activated with a peak value of 4.5 A, 3.5 A, 3.5 A, the source current are balanced with a peak value of 4.5 A in each phase as shown in Figure 6.26(c). The D-STATCOM currents are also unbalanced with a peak value of 5.5 A, 5 A, 4.2 A shown in Figure 6.26(b). These unbalanced D-STATCOM currents are generated by the control strategy to get the source current leading for zero voltage regulation. To supply these unbalanced currents from D-STATCOM, the capacitor voltages should be properly regulated. For regulating the capacitor voltages, a zero sequence voltage is injected. When this zero sequence voltage is used in the control strategy, the DC capacitor voltage waveforms are observed in Figure 6.26(e) to be closely regulated and follow the voltage reference value of 40V. The Figure 6.26(d) shows the response of phase voltage and source current when the ZVR mode is activated, the source current is leading the source voltage and PCC voltage is tracks the rated source voltage. With the same experimental parameters simulation results are shown in Figure 6.27 it is observed that this results are exactly matched to the experimental results of Figure 6.26.



(a)



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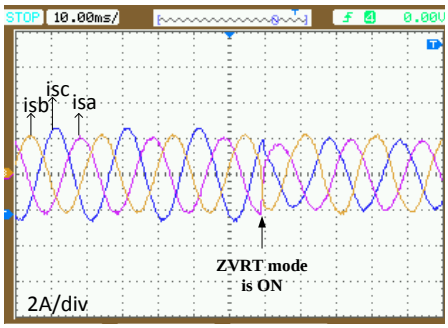

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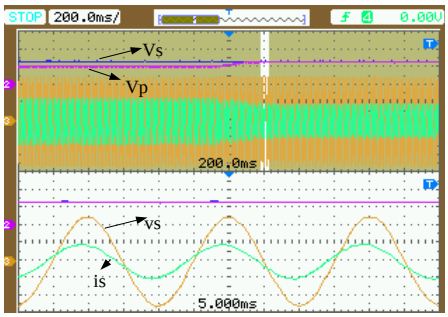

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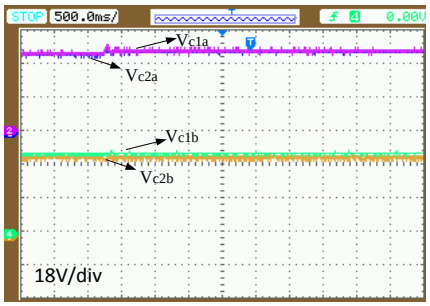

(e)

Figure 6.26 Performance of D-STATCOM under ZVR mode with individual voltage balancing and zero sequence voltage injection.

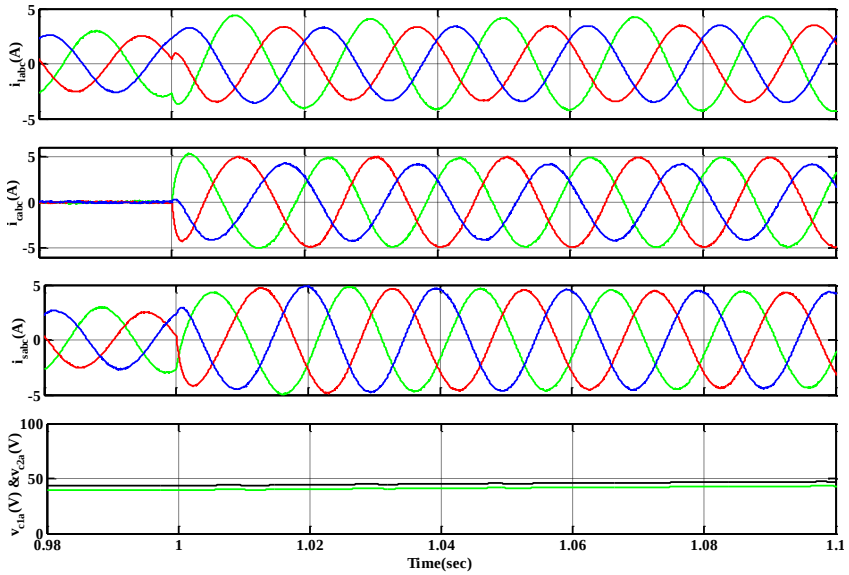

Figure 6.27 Simulation result of D-STATCOM under ZVR mode of operation.

6.6 Conclusion

In this chapter, the detailed descriptions for the design and development of laboratory prototype D-STATCOMs have been given. For the developed D-STATCOM the power circuit is made with MOSFET as a switching devices. A DSP DS1006 of dSPACE has been used for the real-time implementation of various control algorithms of D-STATCOM in MATLAB/Simulink environment. The different hardware components as required for the proper operation of experimental set-ups such as pulse amplification, isolation and dead-band circuits, voltage and current sensor circuits, non-linear/reactive loads have been designed, developed and interfaced with dSPACE. The developed prototype for single phase D-STATCOM has been tested for reactive power compensation and the improved modulation signals for capacitor voltage balancing. The harmonic elimination for different loads with original and modified single phase pq theory under source voltage distortion is validated. The developed prototype has further been tested with three phase D-STATCOM for reactive power compensation and harmonic elimination with different loading conditions. The steady-state performances of the D-STATCOM have been found to be satisfactory with PI and resonant current controller. A smooth control of dc voltages of H-bride cells has ensured the effectiveness of the dc voltage controller by individual voltage balancing and zero sequence algorithm in case of unbalanced load compensation.

CHAPTER 7: CONCLUSIONS AND FUTURE SCOPE

[The main conclusions of the work presented in this thesis and possible future research have been summarized in this chapter.]

7.1 Conclusions

In this thesis, digitally controlled single phase and 3P3W D-STATCOM have been investigated to improve the power quality of the source current waveform and to compensate the load reactive power in distribution systems. Even though, conclusion has been given at the end of each chapter, the following is concluded with respect to the objectives.

- **Evaluation of Multilevel PWM techniques for CHB D-STATCOM**

The performance of SSBC inverter is simulated with Level Shifted PWM (LSPWM) and Phase Shifted PWM (PSPWM) methods. Even though, the THD of output voltage is lower with LSPWM, but the losses in H bridges are unequal. On the other hand PSPWM method results in equal losses in each H-bridge, but at slightly higher THD. Since the difference in loss in H bridges is going to cause capacitor voltage unbalance leading to loss of multilevel operation. Therefore, throughout this work PSPWM technique is used for both single phase as well as three phase D-STATCOM. During unbalance operation of D-STATCOM employing devices of different manufacturers, the losses in H bridges will become more significant. The performance of D-STATCOM comprising of ABB and Fuji switches is simulated to show serious mismatch in the losses.

- **Reference current generation and current controller performance**

For single phase D-STATCOM, two methods (based on original pq and modified pq control theories) are used to generate the reference current. The performance of D-STATCOM is compared when the source voltage is distorted. The modified pq theory is shown to produces much lower source current THD in such situation.

For three phase D-STATCOM, synchronous reference frame (SRF) theory is used for reference currents generation. Two current controllers (PI and PI with resonant) are tested for performance evaluation. The later has shown to give improved performance compared to a PI controller for different types of non-linear loads. After D-STATCOM compensation, the source currents have been observed to be sinusoidal and their corresponding THDs have also been observed to be well within the limits of IEEE–519–1992 recommended value of 5%.

- **Voltage regulation**

The loads on a distribution line cause voltage fluctuations at the point of common coupling (PCC). To make the source current balanced in the case of an unbalanced load and also to keep the magnitude of PCC voltage constant, the D-STATCOM is operated in Zero voltage regulation (ZVR) mode.

In a weak distribution system the D-STATCOM is operated in voltage control mode, it is shown that unbalance in source voltage can be taken care at PCC by injection of suitable currents to get balanced line voltages at PCC.

- **Capacitor voltage balancing**

The unequal power loss due to asymmetries in device characteristics leads to capacitor voltage deviation. It has been shown that it will lead to widening difference in capacitor voltages of H bridges. Two methods namely, improved modulating signal (IMS) and active voltage superposition (AVS) are used to achieve capacitor voltage balance. It has been shown that IMS method gives improved results compared to AVS method.

When D-STATCOM is compensating for unbalance in currents, dc voltage balancing control is done with (a) cluster voltage balancing control and (b) individual voltage balancing control. The former calculates the zero sequence voltage for balancing the total DC voltages in phases and the later one modifies the individual modulating signal for floating dc capacitors to follow their corresponding reference values in each H-bridge.

7.2 Future Scope

This work can be extended for the future research work as briefly pointed below. The research work presented in this thesis discloses a number of issues that could be further investigated.

1. Practical implementation of multilevel inverters for high power applications is still an active area of research. The development of high power inverters involves higher number of levels, large number of devices, complex control, large size and higher cost. Intensive research needs to be done on developing new multilevel inverter topologies with reduced number of components, low THD and high reliability.
2. Development of new modulation techniques for high power inverters with reduced power losses and natural balance of capacitor voltages is a potential area of research.
3. The conventional PI controller of the D-STATCOM control system can be replaced by soft computing techniques such as fuzzy logic, neural network, and genetic algorithm to further improve the transient response of the system.

4. Design of the controller of the D-STATCOM using advanced control techniques such as model predictive control is another area of research.
5. Another interesting topic could be the research on the combination of D-STATCOM and passive harmonic filters. This research could include the selection of topology, inspection of compensating characteristics, losses, cost and rating of the individual and overall compensator.
6. Determination of size and location of D-STATCOM in the distribution network is also potential area of research.

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PHOTOGRAPH OF THE EXPERIMENTAL SETUP

LIST OF PUBLICATIONS

List of Journal Papers

1. **Srinivasa Rao Y** and Mukesh Kumar Pathak, "*A Zero Sequence Voltage Injection Method for Cascaded H-bridge D-STATCO*M" Journal of Power Electronics, Vol. 17, No. 4, PP. 1088-1096, July 2017.
2. **Srinivasa Rao Y**, Mukesh Kumar Pathak, "*SRF based PI and Harmonic current controller for modular D-STATCOM*", International Journal of Pure and Applied Mathematics Vol.114, No.7, PP.99-109, 2017.
3. **Srinivasa Rao Y**, Mukesh Kumar Pathak, "A capacitor voltage balancing scheme for a single-phase cascaded H-bridge STATCOM" Electric Power Components and Systems (Submitted after 1st revision).
4. **Srinivasa Rao Y**, Mukesh Kumar Pathak, "Model Predictive Control for three level Cascaded H-bridge D-STATCOM" IETE Journal of Research-Taylor & Francis (Submitted after 1st revision).

Conference Paper

1. **Srinivasa Rao Y**, Mukesh Kumar Pathak, "Modular D-STATCOM based PCC Voltage Balancing" IEEE Conference on Innovative Technologies in Engineering at Osmania University, Hyderabad (to be presented in April 2018).