ANALYSIS AND MODELLING OF SPACER BASED GATE-ALL-AROUND RECONFIGURABLE DEVICE

Ph.D. THESIS

by

ABHISHEK BHATTACHARJEE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE,
ROORKEE-247 667, INDIA
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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **"ANALYSIS AND MODELLING OF SPACER BASED GATE-ALL-AROUND RECONFIGURABLE DEVICE"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electronics and Communication Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from July, 2014 to March, 2018 under the supervision of Dr. Sudeb Dasgupta, Associate Professor, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institution.

(ABHISHEK BHATTACHARJEE)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

(Sudeb Dasgupta)
Supervisor

Date: **12th March 2018**

The Ph. D Viva-Voce Examination of Mr. **Abhishek Bhattacharjee**, Research Scholar, has been held on **14th August 2018**.

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Signature of Supervisor **Head of the Department**

Date: **14th August 2018**

ABSTRACT

As the scaling limit is gradually reaching its ultimatum, the devices with multiple functionalities such as TFET, multi gate FiNFET, Silicon nanowire FET are been thoroughly investigated. Silicon nanowire-field-effect transistors (SiNWFETs) are among those devices which can replace the planar as well as fin-shaped field-effect transistors (FinFETs). One of the major drawbacks of the conventional CMOS technology is the inability to reconfigure it. To deal with this problem nanoscale technology with flexible configurability has recently gained a lot of attention in the device research community.

An axial silicon nanowire transistor which can be programmed dynamically as n- or p-FET by externally tuning the applied gate voltage forms the modern day reconfigurable field effect transistor (RFET). This device mainly exploits the interesting and unique properties of metal-silicide Schottky junctions to tune the polarity of charge carriers. In a RFET apart from the three electrodes which are common in any field effect transistor, a fourth one acts as an external electric signal to select the desired FET characteristics.

This new technology also provides a lot of advantages in terms of fabrication ease using the traditional bottom-up approach. The channel is almost doping free which leads to lesser short channel effects (SCE's) and the S/D contacts are also metallic which aids its possibility to become a lean technology in upcoming days. Enhanced electrical performance in terms of extremely low gate leakage makes it highly desirable for future low power digital applications. Noteworthy maturity in complex logic and circuit implementation with fewer numbers of transistors than usual has also been recently portrayed using this novel platform.

Unlike any other field effect transistor dependent on band to band tunneling (BTBT) for its on-current generation like tunnel field effect transistor (TFET), RFETs too suffer from various challenges and one of them is lower current drive and higher subthreshold swing (S/S) as compared to other planar devices. In view of these drawbacks, modification to the existing RFET architecture leading to a new device concept is necessary.

The objective of this thesis is many folds, firstly, to design for the first time a source/drain (S/D) spacer based *underlap* ambipolar silicon nanowire field-effect transistor device structure which shows enhanced electrical performance over the existing ambipolar topologies. The main reason behind these improvements is the ability of S/D spacers to

terminate the fringe field lines in to the Schottky contact more nicely which increases the junction electric field and hence the BTBT rate is boosted. The next aim is optimization of various device aspects like spacer material type and length of spacer (L_{sp}), gate dielectric and its thickness (t_{ox}) and inters gate distance (d_{G1G2}) using rigorous coupled 3-D Technology Computer Aided Design (TCAD) numerical device simulations. A systematic investigation of the impact of these critical design parameters on the vital device performance parameters, such as ON current, on to off current ratio, Subthreshold swing (S/S), threshold voltage, and transconductance generation factor was done. It was observed that higher spacer lengths, gate and spacer dielectric constants improves the device performance mainly because of better electrostatic coupling between metal gates and Schottky junctions and also due to increase in density of fringe field lines near the metal/semiconductor interface. To acquire a deeper understanding of various physical details behind spacer based performance enhancements over the conventional *non-underlap* RFET architecture through device level optimizations, the impact of variation in the *gate channel underlap* (L_{GCU}) and *spacer channel underlap* region (L_{SCU}) on the device behaviour was also studied. The main aim of shifting to a high-κ gate dielectric is to lower the equivalent oxide thickness (EOT) without making a trade off with the gate leakage. So, the role of gate oxide EOT and scaling properties of the proposed device was also investigated.

Since the subthreshold drain current of a RFET depends upon thermionic emission which is itself a temperature dependent phenomenon, the work was further extended to study the temperature dependence of the digital/analog parameters and RF figure of merits of the spacer based RFET and compare the same with the existing RFET topology and other devices which depend on band to band tunneling (BTBT) for their on current generation. Having a better thermal stability over TFET and sufficiently lesser V_{th} roll-off, the proposed device portrays orders of magnitude reduction in parasitic gate capacitances and intrinsic delay as compared to gate-all-around (GAA) and heterogeneous gate dielectric gate all around (HD GAA) TFET devices over the considered range of temperature, thus ensuring higher switching speed for digital applications. It is found to have a comparatively better analog performance than SiGe and full silicon TFETs with increased values of g_m, g_m/I_d and A_v in the considered range of temperature mainly because of BTBT dependent drive current and superior gate control over the silicon channel. Temperature variation of various

important RF parameters like higher order transconductance coefficients, cut-off frequency (f_T), gain bandwidth product (GBW), transit time (τ_t), device figures of merits (FOMs) VIP2, the third-order intercept point (IIP3) and the third-order intermodulation distortion (IMD3) was shown and the results were also compared with conventional RFET, Si abrupt TFET and SiGe TFET. For most of these metrics, the proposed device shows superior RF performance as compared to its counterparts. The device FOMs were also found to be less sensitive to temperature variations making it more suitable for applications where temperature fluctuation is a major concern.

Finally, a physics based compact model was developed for surface potential and drain current for a dual gate (DG) source/drain (S/D) spacer based silicon nanowire reconfigurable field effect transistor. The models were derived by dividing the active portion of the device into several regions based on positioning of the gates, spacers and the metal-silicide Schottky junctions. A charge density expression was first developed and the 2-D Poisson's equation was self consistently solved for various sub-regions of the device. By using the charge density expression, a single-piece-approximation of the long channel surface potential was developed. Then it was added to the potential distribution at the Schottky junctions which is then solved by using a quasi-2D approach. The drain current was modeled by first finding the barrier height required for the carriers to overcome the maximum potential barrier induced in the silicon channel by the control gate near the source end of the device which was then used to find out the current through the Schottky barriers. This was equated based on the principle of current continuity with the drift diffusion current in the channel obtained by using the earlier derived charged density expression to generate a final drain current expression. The accuracy of the derived results was tested using 3-D numerical TCAD simulations. This work was lastly concluded by developing a Verilog-A model of the device under consideration for investigating the spacer induced performance improvements over the conventional *non-underlap* RFET with respect to delay reduction mainly in logic applications.

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Date: (Abhishek Bhattacharjee)

To

my beloved parents

and all my cousins

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LIST OF ABBREAVATIONS

DG	Double Gate
SBH	Schottky Barrier Height
DIBL	Drain Induced Barrier Lowering
FIBL	Fringe Induced Barrier lowering
eV	Electron Volt
VLSI	Very Large Scale Integration
EOT	Equivalent Oxide Thickness
CMOS	Complementary Metal Oxide Semiconductor
SiNWFET	Silicon Nanowire Field Effect Transistor
FOM	Figure Of Merit
TCAD	Technology Computer Aided Design
SS	Subthreshold Slope
RFET	Reconfigurable Field Effect Transistor
RF	Radio Frequency
ITRS	International Technology Roadmap for Semiconductors
Si	Silicon
S/D	Source/Drain
GAA	Gate-All-Around
TFET	Tunnel Field Effect Transistor
SiGe	Silicon germanium
TIG	Three Independent Gate
SOC	System-On-Chip
0-D	Zero Dimensional

1-D	One Dimensional
2-D	Two Dimensional
3-D	Three Dimensional
CNT	Carbon Nano Tube
BJT	Bipolar Junction Transistor
NW	Nano Wire
BTBT	Band to Band Tunneling
FET	Field Effect Transistor
SBFET	Schottky Barrier FET
WKB	Wentzel-Kramers-Brillouin
SRH	Shockley-Read-Hall
IC	Integrated Circuit
SCE	Short Channel Effect
SOI	Silicon On Insulator
eDensity	Electron Density
hDensity	Hole Density
HEMT	High Electron Mobility Transistor
NMOS	n-Channel MOSFET
PMOS	p-Channel MOSFET
FinFET	Fin Field Effect Transistor
TAT	Trap Assisted Tunneling
HD GAA	Heterogeneous gate dielectric gate all around
VTC	Voltage Transfer Characteristics
NMH	High level noise margin
NML	Low level noise margin
GBW	Gain bandwidth product

IMD3	Third order intermodulation
IIP3	Third-order intercept point
K	Kelvin

LIST OF SYMBOLS

V_{DD}	Drain Voltage
V_{DS}	Drain to Source Voltage
HfO_2	Hafnium dioxide
SiO_2	Silicon dioxide
t	time
T	Temperature
ε_r	Relative dielectric constant
ε	Permittivity
ε_{ox}	Permittivity of Oxide
N_A	Acceptor concentration
N_D	Donor concentration
L_{sp}	Spacer length
t_{sp}	Spacer width
V_{bi}	Built in Potential
t_{ox}	Oxide thickness
q	Electronic charge
n_i	Intrinsic carrier concentration
I_{ON}	ON state current
I_{OFF}	OFF state leakage current
f_T	Cut off frequency
g_m	Transconductance
g_d	Output Conductance
A_v	Intrinsic voltage gain

d_{G1G2}	Inter gate separation
τ_d	Intrinsic delay
g_{m2}	Second order transconductance coefficient
τ_t	Transit time
V_{FB}	Flatband voltage
C_{GS}	Gate to source capacitance
C_{GD}	Gate to drain capacitance
$\Psi(x, y)$	Potential distribution along x, y direction
TiO_2	Titanium dioxide
E_{FN}	Electron quasi fermi energy level
E_{FP}	Hole quasi fermi energy level
V_n	Electron quasi fermi potential
V_p	Hole quasi fermi potential

Chapter 1

Introduction

1.1 Introduction

Since the past forty years, due to continuous scaling in gate length, gate oxide thickness and supply voltage, the transistor performance has seen a lot of potential improvement [1-4]. The more a device is down scaled, the higher is its packing density, the higher its circuit speed, and lower its power dissipation. However, as CMOS dimensions have started to approach the sub nanometer regime (<100 nm), we observe a change in the device performance. To maintain the rate of improvement in device performance with continued down scaling, modifications to device designs and fabrication techniques are required. Advanced MOSFET structures like ultra thin-body (UTB) FET, Dual-gate FET, FinFET, TriGate FET and Gate All Around (GAA) FET offer the opportunity to continue scaling beyond the bulk because they provide reduced short channel effects (SCE's), a sharper subthreshold slope (S/S) and better carrier transport as channel doping is reduced. Silicon Nanowire Field Effect Transistor (SiNWFET) is a promising candidate [1] for future CMOS device for further scaling. The Gate All around structure enhances the Gate length scalability because the electrostatic control is improved. Moreover threshold voltage variations due to random dopant fluctuations are minimized because it enables the use of an undoped channel [2].

Over the past few decades of dominance of CMOS devices in electronic applications, combining n- and p-FET to reduce power dissipation and silicon area, recently a demonstrable concept was provided for universal transistor which can be configured as n-FET/p-FET by application of appropriate potentials in an axial nanowire heterostructure [Metal-Insulator-Metal (M-i-M)] with independent Schottky junctions. This latest modification in SiNWFET technology is to provoke the concept of ambipolarity in these devices i.e. tuning the polarity allowing the device to act as an n-FET or a p-FET by mere application of voltage with the help of two or three metal gates. The concept to make ambipolar devices using Si is thought to be a modification to next generation FinFET as well as GAAFET and their physics is very much similar to Tunnel Field Effect Transistors

(TFETs). With the help of one control gate and another polarity gate it is possible to make one type of carrier (either e^-'s or holes) to tunnel from Drain to Source end and block the flow of other type of carrier. FinFETs have successfully shown that short channel effects (SCEs) can be minimized to a great extent due to better electrostatic control. To acquire a more superior gate control, Silicon NanoWire FETs (SiNWFETs) having gate-all-around structures have proven to be an ideal replacements to FinFETs. The Schottky metallic contacts at the source and drain junctions creates Schottky junctions that can be tuned electrically to invoke the reconfigurable behaviour. The logic architectures that are impossible to implement with CMOS intrinsically can be developed using ambipolar DG in a compact form.

For reduction of the overall leakage power dissipation of circuits in current CMOS technology, multi threshold voltage (multi-V_t) design is used widely. In the critical paths low-V_t devices are used so that the timing constrains are met, while in the slack paths, high-V_t devices with low-leakage are used. However, to implement the multi-V_t circuits additional technological steps are required to create devices with multiple threshold voltages, which affects the regularity in layout and also increases the process costs compared to single-V_t circuits. Ambipolar SiNWFETs having dual V_t are expected to deliver better performance with smaller consumption of leakage power as compared to low standby power FinFET's.

This chapter introduces the work carried out in this thesis. Section 1.2 describes the background and motivation behind the research topic. Section 1.3 presents a brief discussion on the importance and expectations with SiNWFETs. The major problems with the GAA devices at the current technology node are highlighted in section 1.4. Section 1.5 presents the objectives of this thesis. In section 1.6 the main focus and outline of the work is presented. Finally, the chapter wise organization of the thesis in a compact form is provided in section 1.7.

1.2 Motivation behind the Research

1.2.1 Moore's Law and MOS transistors

After the invention of Bipolar junction transistor (BJT) in 1948 by William Shockley, Walter Houser Brattain and John Bardeen researchers across the globe were looking to overcome various shortcomings of this device such as low thermal stability, higher noise,

low switching frequency, complex base control resulting in the requirement of skillful handling, predominant radiation affect etc. In search for other alternatives, the initial research on present day MOS transistors was started many years ago. In 1965 an observation was made by Intel co-founder Gordon Moore which is also known as Moore's law [3]. It states that after every two years the number of transistors in a dense integrated circuit will get doubled. This law remained unchanged over the next thirty years after this famous observation. It may be noted that at the time of Gordon Moore, the number of transistors in a particular integrated circuit were not more than 32 but now a day's almost 20 billion transistors are integrated on a single chip which clearly shows how important his observation was thus leading to the scaling of transistors. At present the general consensus that has been accepted by the microelectronics industry is that the number of transistors per chip gets doubled every 18 months. There are several implications of Moore's law on the semiconductors over the last several decades. The number of logic transistors in a chip defines its functionality. In the same chip, if more and more components are integrated, then the functionality per chip increases which reduces the delay of data flow and also increases the overall density of transistors per chip area. The next most important implication of Moore's law is the reduction in the cost of manufacturing per function in an integrated circuit along with increasing the functionality per chip. The third implication of this law is improving the speed of a particular microprocessor which is also known as performance factor. The density of transistors in a logic circuit is inversely proportional to the total chip area and directly proportional its overall speed and performance.

1.2.2 Scaling techniques and Short Channel Effects

The initial constant field scaling law for MOS transistors was propped by Robert. H. Dennard [4] in one of his research papers in which gate length of 10 μm was demonstrated. After that an approximate reduction of 15% in gate length of MOSFET is registered every year and currently we have reached 22nm in 2014. By downscaling the MOSFET dimensions, using the constant field scaling theory deteriorate the electrical performance of the transistor. This is due to various SCE's which influence the output characteristics of the device and degrades its performance. There is another type of scaling mechanism known as the constant voltage scaling. In this approach the supply voltage of the transistor is kept

constant. This results in an increase in the electric field which in turn introduces hot carrier effects (HCEs) in the device. The constant voltage scaling is largely adopted in the industry because the rate of reduction in channel length of the MOS transistors with every technology generation [5] is not same as that of the supply voltage scaling (V_{DD}). Moreover, constant field scaling yields the largest reduction in the power-delay product of a single transistor and the disadvantage of constant voltage scaling is that the electric field increases as the minimum feature length is reduced. Though there are a lot of potential improvements in a transistor's performance with continuous downscaling [6-11] in feature size such as increase in operating speed and packing density along with reduction in power dissipation but as we have entered into the sub nanometer regime (<100nm) various other unwanted problems are causing serious hindrance in maintaining the improvement rate. Such problems are collectively called SCEs [12-14]. It consists of a group of phenomenon like V_{th}-roll off, drain-induced-barrier-lowering (DIBL), punch through, channel length modulation, impact ionization etc. Threshold voltage roll off refers to the fact that in short channel devices where the distance between source and drain is nearly equal to the depletion region width of the MOSFET in vertical direction, a part of the charge which is supposed to be controlled by the gate is actually shared between source and the drain. As a result, the gate voltage required to create a particular level of inversion decreases due to a reduction in effective charge being masked by the gate. It may cause serious problems for circuit designers because there is variation in V_{th} due to process variations and with every technology node new techniques are needed to be found out for adequate control of threshold voltage. Another short channel effect known as drain-induced–barrier-lowering (DIBL) occurs when the height of the potential barrier between channel and source gets lowered at higher drain biases resulting in an enhanced drain current and as a result of which threshold voltage (V_{th}) gets lowered. When the drain voltage is increased, the depletion layer width at the drain side may increase and the channel may actually become pinched-off (finished) at the drain side. This may reduce the overall channel length and increase the drain current and is termed as channel length modulation or CLM. This results in a decrease in the effective channel length. At a very high drain to source voltage, especially in small channel devices with low-doped substrates the depletion region under the drain and source can actually merge into a single depletion layer and under this conditions the field beneath the gate becomes a strong function

of drain to source voltage V_{DS}. This may led into an uncontrolled drain current which is undesirable and may decrease the output conductance. Other unwanted effect which occurs especially in n-channel MOSFET is impact ionization. This may lead into increase of subthreshold current at larger drain voltages. Apart from the above mentioned short-channel-effects due to thinning of gate oxide following the constant field scaling approach the gate oxide tunneling current also increases exponentially and poses serious threats to further scaling of the device [13] as it becomes comparable to the drain current (I_{ON}) at an oxide thickness of about 1nm. One of the main aim of technology scaling is to lower the dynamic power dissipation but at the same time since V_{DD} is scaled down and is approaching V_{th}, the static or standby power increases as the transistor size becomes small. For an enhanced higher circuit operation, higher on-current is desirable. Higher drive current is important in view of reduction of delay time in a circuit which depends upon the charging time of next stage capacitance and since the intrinsic delay determines the maximum frequency of operation of any logic circuit, it is one of the most important factors for circuit designers. On the other hand, in the operation of CMOS we find that when there is a change in the input logic state, the total load capacitance of next stage gets changed. Under steady state condition, only one of either NMOS or PMOS is in on-state and the other one remains off. So, under steady state conditions the only current which flows is the off state leakage current and thus for the reduction of total steady state or waiting power consumption, curtailment of off state leakage is very important.

1.2.3 Introduction to Gate All Around (GAA) Devices

After the invention of MOSFET revolutionized the computer industry, the researchers were now focussing on developing new device structures which could further enhance the device performance. An idea was proposed to increase the number of gates to form multi gate transistors to enhance the electrostatic controllability of the channel as compared to single gate bulk SOI MOSFET thus reducing SCE and increase on current. It was found that a double gate (DG) MOSFET scaling can be done more aggressively and short cannel effects are further suppressed because of better effective gate control. Quite a number of double gate FET structures were proposed in the research community out of which the fin shaped field effect transistor or FiNFET emerged as the most popular one [15]. The speciality of this

structure is that the channel region consists of a vertical fin around which the gate is wrapped from the three sides. A few more GAA device structures such as tri gate and omega shaped gated FETs were also proposed. In comparison to tri gate structure an effective fourth gate extends into the substrate from one of the sides in the omega shaped one which makes it better in terms of device performance as the gate control is further improved. But the ultimate scaling options for a MOS transistor were actually provided by semiconductor nanowires which are cylindrical two dimensional crystal structures with few nanometres of diameter. Since the gate actually wraps the channel from all sides, a complete GAA structure was actually possible with this in contrary to all the above mentioned device architectures and the best performance in terms of short channel effects was also achieved with them.

1.3 Silicon Nanowires as Future Nanoscale Devices

1.3.1 Importance of Nanowire Based Devices

Silicon nanowires are quasi one dimensional nanostructures having diameter less than 100nm. Over the last few years silicon nanowires have received considerable attention as chemical as well as biological sensors, photovoltaic as well as nanoelectronics devices [16-26]. Though planar and tri gate device proved their usefulness in various fields of technological applications with silicon as well as other materials [27-45], the small diameter of nanowires has proved to be highly advantageous as it results in a high surface to volume ratio which is an important requirement in sensor based applications because with even a very small input signal the nanowire potential can be effectively controlled. Moreover, their superior sensitivity in chemical surface processes also lies in the fact that one or more of their physical dimensions is always less than the charge screening length or the Debye length. When it comes to applications like photovoltaic solar cells, these nanowire structures are found to be more efficient than Li-ion batteries to collect the incoming solar radiation. In comparison to III-V semiconductors, the quantum confinement of carriers is visible only at large diameters; it is predicted to be substantial only at diameters below 3nm in silicon nanowires. For this reason the behaviour of silicon nanowires are often referred to as quasi 1-D. This quasi 1-D behaviour of silicon nanowires proves to be essential in devices in various ways. With nanowires having diameter below 10nm, the band structure also gets modified in a quiet interesting manner. It is observed that there is an increase in band gap for smaller

diameters and at sufficiently small diameters a direct band gap can be obtained. When it comes to field effect devices, silicon nanowire field effect transistors (SiNWFETs) have achieved the class of most important devices to investigate and optimize the electronic properties of nanowires. An optimum geometric gate coupling can be provided to the active area of the device because the gate is completely wrapped around the nanowire [21-24]. The best scaling performance can be achieved if the silicon thickness is quiet small to allow a full depletion at lower gate voltages. The fact that silicon nanowire field effect transistors is proposed and also studied nowadays by a lot of researchers across the globe lies in many of their superior features which make them a perfect candidate to become the building blocks for future nanoelectronics [23-25]. Some of these features are discussed here. They can be produced in huge quantities with electronic properties that are reproducible which is highly essential for very-large-scale-integrated (VLSI) systems. Moreover, they provide the ease of processing and ability for integration with conventional fabrication techniques which include the conventional bottom up approach to synthesize ultra thin nanowires with well controlled channel width which is not possible with the conventional lithography techniques. It is easier to maintain the electrical integrity of nanowire based electronics even if the gate length is scaled aggressively because their diameters can be controlled well below 10nm which is becoming increasingly difficult to achieve in conventional MOSFETs. Apart from the superior gate control, they are also able to provide radial and axial heterostructures which can reduce scattering and result in higher carrier mobility. By keeping the silicon film thickness same as that of the gate length subthreshold swing less than 75mV/dec and DIBL less than 50mV/V can be achieved using these GAA structures. But, reliability issues such as self heating effect (SHE) can affect the performance of these devices. It arises mainly due to difficulty in evacuating the generated heat due to electron phonon scattering in these structures. Furthermore, surface roughness and spatial confinement can further increase the self heating phenomenon. But through improved fabrication techniques and reduced variability most of the reliability issues can be controlled up to a great extent.

1.3.2 Quest for a Universal CMOS Switch

The computer industry has relied upon n-type and p-type transistors for the implementation of computing circuits over the last four decades. The alternative switching of

n and p FETs is because of the different polarity of the charge carriers. Due to aggressive scaling of the dimensions of transistors, it is becoming increasingly difficult to accurately control the doping distribution in modern 3-D structures. To achieve the energy efficient CMOS operation, it is mandatory that the performance of the n and p-transistors have to be comparable. This means that they must have almost equal on-currents, threshold voltages and inverse subthreshold slopes. The larger channel width requirement in silicon to align on-currents is due to the significantly lower hole mobility compared to that of electrons. For modern 3-D CMOS devices, it is quite difficult to adjust the channel width freely without affecting the device electrostatics. To double the number of p-channels connected in parallel is one possible solution to adjust the current in such cases. The reconfigurable technology can provide solutions to both these problems [46-51], i.e. the difficulty to control the dopant distribution and dissimilar sizing of p and n FETs and hence can reduce the intricacy to build CMOS logic circuits. The channel is kept intrinsic in these devices to allow n and p conduction from the same channel and to avoid impact of doping. After the successful demonstration of field programmable FPGA in 1984, reprogrammable nanowire FPGA matrices have been developed in 2003 and programmable circuits for nano-processors in 2011 by Lieber et. al. [52]. Finally, Schottky barrier engineering technique is adopted to selectively inject electrons and holes into the intrinsic channel from the source and drain electrodes to form the so called reconfigurable FET (RFET) which are discussed later.

1.4 Problem Statement

In light of the existing literature survey, the major problems we have encountered with the various GAA devices at the current technology node are listed below:

i) Since, separate n- and p-transistors are required the layout area is basically large.

ii) The fabrication process is relatively complex and costly.

iii) Increased short channel effects due to scaling.

iv) The drive current is degraded due to various scattering mechanisms which are resulted from heavy doping in the channel region.

1.5 Objectives of the Thesis

The objectives of this thesis are enumerated below.

(a) To design for the first time a source/drain (S/D) spacer based *underlap* ambipolar silicon nanowire field-effect transistor device structure and optimize various device aspects like spacer material type and length of spacer length (L_{sp}), gate dielectric and its thickness (t_{ins}) and inter gate distance (d_{G1G2}) using rigorous coupled 3-D Technology Computer Aided Design (TCAD) numerical device simulations. A systematic investigation of the impact of these critical design parameters on the vital device performance parameters, such as I_{ON}, I_{ON}/I_{OFF}, Subthreshold swing (*S/S*), V_t, and g_m/I_d is proposed to be undertaken.

(b) To acquire a deeper understanding of various physical details behind spacer based performance enhancements over the conventional *non-underlap* RFET architecture through device level optimizations, the impact of variation in the *gate channel underlap* (L_{GCU}) and *spacer channel underlap* region (L_{SCU}) on the device behaviour is also studied. So, the role of gate oxide EOT and scaling properties of the proposed device is also investigated.

(c) Since the subthreshold drain current of a RFET depends upon thermionic emission which is itself a temperature dependent phenomenon, it is proposed to further extend the study as the temperature dependence of the digital/analog parameters and RF figure of merits of a spacer based RFET. The same are proposed to be compared with the existing RFET topology and other devices which depend on band to band tunneling (BTBT) for their on current generation. Having a better thermal stability over TFET and sufficiently lesser V_{th} roll-off, the proposed device portrays orders of magnitude reduction in parasitic gate capacitances and intrinsic delay as compared to GAA and HD GAA TFET devices over the considered range of temperature, thus enduring higher switching speed for digital applications. The device is proposed to be more stable under temperature variations.

(d) To develop a physics based compact model is developed for surface potential and drain current for a dual gate (DG) source/drain (S/D) spacer based silicon nanowire reconfigurable field effect transistor. The models are derived by dividing the active

portion of the device into several regions based on positioning of the gates, spacers and the metal-silicide Schottky junctions. A charge density expression is first developed and the 2-D Poisson's equation is self consistently solved for various sub-regions of the device, to model the drain current and surface potential. The accuracy of the derived results is tested using 3-D numerical TCAD simulations. This work is concluded by investigating the spacer induced performance improvements over the conventional *non-underlap* RFET with respect to delay reduction mainly in logic and digital circuit applications.

1.6 Outline of the Work

The focus of the thesis is to propose a novel ambipolar FET architecture in which many of the limitations of the current *non-underlap* RFET is overcome. This is done by bringing into focus the *underlap* RFET device using the source/drain spacer technology. The inherent device physics behind the spacer induced performance enhancements and the effects of variation in various device attributes on the behaviour of the proposed RFET are discussed in details. Looking at the fact that the device on current is partially dependent on thermionic emission, the temperature dependence of the DC, analog and RF performance of the device is also illustrated. Finally, a charge based compact analytical model of the device under consideration is developed and in addition it is also shown that how S/D spacers can be useful in delay reduction in case of few digital circuit applications. In total the thesis has seven chapters. At the beginning of each chapter there is a brief introduction along with the motivation about the concerned problem. In addition, the simulation methodology, results and analysis are discussed in a comprehendible way.

1.7 Thesis Organization

Chapter 1 introduces the entire thesis. It provides the motivation and outline behind this research and the agenda for choosing the objectives of the work. Problem statement, objectives of the thesis and the thesis organization is presented in this chapter.

Chapter 2 provides a comprehensive literature review on RFET devices and work done by various research groups across the world so far. Starting from the basic single gate

ambipolar transistor, we gradually move into dual and triple gate RFET architectures. The device physics, advantages and the technological challenges are also discussed.

Chapter 3 introduces the new device concept in details. For the very first time the effect of source/drain spacer oxide on the performance of a dual gate ambipolar silicon nanowire field effect transistor are portrayed using extensive 3-D TCAD simulations. We show discusses the impact of various physical attributes of the device under consideration such as spacer length, spacer material, gate oxide material along with its thickness and inter gate distance on vital performance parameters of the device such as I_{ON}, $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$, Subthreshold swing (*S/S*), V_t and g_m/I_d along with their optimization for achieving best device performance.

Chapter 4 discuses the appropriate designing of the gate/spacer channel underlap region to maximize the I_{ON} and $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio and the inherent device physics behind the performance enhancements is also illustrated in details. It further elucidates the role of gate oxide equivalent oxide thickness (EOT) on the performance of the proposed RFET along with which the scaling properties of this device are also reported.

Chapter 5 illustrates the temperature dependence of the digital/analog parameters and RF figure of merits (FOMs) of the proposed RFET and compares the same with the existing RFET topology and other devices which depend on band-to-band tunneling (BTBT) for their on-current generation. Since the on-current of a RFET depends on thermionic emission phenomenon as well which is itself temperature dependent, it is highly interesting to study the temperature dependence of the device characteristics for this unique nanotransistor because though the impact of temperature on the device performance for tunnel field effect transistor (TFET) has been reported earlier by various groups, such an investigation has not yet been presented so far in case of an RFET.

Chapter 6 begins with the development of a physics based compact model for surface potential and drain current for the device under consideration which can be used can be used to study the behavior of ambipolar FETs having S/D spacers for varying device dimensions and also can be utilized for the future design of memory devices and circuits using spacer based RFETS. The model includes the effects of drain voltage, nanowire radius, temperature and Schottky barrier height. The accuracy of the derived results is tested using 3-D numerical

TCAD simulations. The chapter ends with the illustration of how the spacer technology can be useful in digital logic applications.

The conclusions of the thesis are drawn based on the obtained results in **Chapter 7**. The thesis ends with future scopes related to this work and a complete bibliography.

Chapter 2

Reconfigurable Field Effect Transistor-Device Physics, Challenges and Applications: A Literature Review

2.1 Introduction

As the state of art CMOS technology is reaching its scaling limits, sub threshold leakage is becoming a big threat at the current 22nm node technology. Various methods have been tried in the past to resolve this problem. Use of high-κ gate dielectrics is one of such methods [53]. Moreover, multi V_t design has gained immense popularity in designing modern complex logic architectures. Nearly, five decade old research in CMOS based IC's portrays the use of combination of n- and p-FET devices [5-30]. But, exact control of doping are required in these devices and changing their electrical characteristics is very tough. Among the futuristic devices, CNT FETs and various tunneling based transistors has gained immense attention from various device researchers In recent years [54-84], one such class of device is the reconfigurable Gate All Around (GAA) SiNWFET which is of immense interest because of their negligible random dopant fluctuation, lower series resistance, excellent electrostatic integrity, low thermal budget and higher on to off current ratio at a given supply voltage. Moreover the ease of fabrication with the conventional bottom up approach has made them as one of the potential competitors for future CMOS logic technologies. Recent research by Zhang et. al. [46], have shown that ambipolar SiNWFET can be immensely useful in the design of complex logic architectures. This chapter presents a detailed study on this current topic of research i.e Ambipolar SiNWFETs, history of development, their operation, method of fabrication and their application from digital logic design point of view. After an extensive literature survey, the chapter ends with outlining the current technical gaps.

2.2 Nanowire FET Classification

Depending on the materials by which they are made, nanowire can be broadly classified as semiconductor nanowires, metallic nanowires and molecular nanowires. They can also be categorized as metal nitride, metal carbide and metal oxide nanowires [21]. Among the various types of nanowire Si/SiO_2 based nanowires having a stable semiconductor/oxide interface have gained immense popularity. Examples of elemental

nanowires include Ge, B, In, Sn nanowires whereas metal oxide nanowires include SnO_2, GeO_2, SiO_2 nanowires. Further, metal carbide and metal nitride nanowires consists of BC, SiC and BN, AlN nanowires respectively.

2.2.1 Properties and Applications of SiNWFETs

Nanowires can also be defined as structures with certain length and thickness or diameter limited to tens of nanometer or even less. In nanowires with diameter less than 15nm mobility of electrons is found to behave in a different manner mainly due to quantum confinement as compared to its bulk counterpart. Kotlyar et. al. [85] had shown that as wire size reduces, phonon-limited electron mobility decreases. Jin et. al. [86] stated that there is an enhancement in total electron mobility at high transverse field due to volume inversion. When the material size is smaller than de Broglie wavelength, electrons and holes are confined spatially leading to the formation of electric dipoles. Moreover, in all materials discrete electronic energy levels are formed. The energy separation between adjacent levels increases with decreasing dimension. The electron Density of States (DOS) depends largely on the dimensions of structures in nanoscale. For bulk systems, there is a square-root dependence of energy, discrete features are seen in zero dimensional (0D) quantum dots, in one dimensional (1D) quantum wires spikes are observed and for two dimensional (2D) quantum well structures the behaviour is more like a staircase. V. K. Arora [87] described that ballistic transport mechanism is an important phenomenon that takes place in nanowires. It generally takes place if device length is smaller than the mean-free path of electrons. With respect to ballistic transport is that there is neither any elastic scattering nor energy dissipation in the process of conduction. Impurities and defects should be there for scattering to take place. The transmission coefficients will be reduced when elastic scattering takes place.

2.3 Tunneling Based FETs

2.3.1 Theory of Tunneling

When the probability of transition of carriers through a barrier is non-zero, tunneling takes place. The rate of tunneling can be found if this probability is calculated and multiplied with the number of electrons in a a given space L. Keldysh [88] provided one of the basic

expressions for tunneling probability calculation E. Kane [89] had simplified the approach and had given amore simpler expression later on based on the time independent Schrodinger equation. Tunneling is basically of two types, direct tunneling and phonon assisted tunneling. Direct tunneling takes place mainly in direct band gap semiconductors where the maxima of valence band and minima of conduction band lie at the same k value. In indirect bandgap semiconductors a change in momentum is acquired by the tunneling particle by emitting a phonon, which is termed as phonon assisted tunneling mechanism.

2.3.2 Brief History of Planar and GAA Tunneling Transistors

T. Baba [90] described one of the initial tunneling devices called the surface tunnel transistor which could operate in room temperatures in structures having gate length less than 100nm. The modern day tunneling field effect transistor (TFET) was proposed by T. Baba [90] in the form of a p-i-n device similar to a lubistor which required higher source/drain doping. Omura [91] described that the working of a TFET is more like a PN diode in reverse bias where the tunneling is controlled by the applied gate bias. A prediction was made that a broader gate oxide may increase the subthreshold swing. To achieve a steeper subthreshold slope, Padilla et. al. [92] proposed a device known as feedback FET with under lapped gate electrode. Cao et. al. [93] proposed a new TFET architecture with a n-layer near the tunneling junction. Rahi et. al. [94] brought into limelight the junctionless TFET device with different isolated gates having different work functions which provide higher tunneling current and less variability as compared to MOSFET. For more efficient switching asymmetric junctionless transistor was proposed later on by Shih and Chien [95]. The double gate TFET architecture with an added metal gate for better drive current was described by Ionescu [96] which was further modified as a dual material gate TFET by Kumar et. al. [97]. The concept of vertical TFET with a very small S/S was elucidated by Han et. al. [98]. Bjork et. al. [99] demonstrated TFETs based on silicon nanowires. Ghosh et. al. [100] tried to improve the characteristics of a Ge TFET by using an underlap portion at the drain side of the device and a p+ pocket implant at the source periphery. Fischer et. al. [101] demonstrated a vertical structure of Si TFET with tunneling in line with the field of gate. Choi et. al. [102] showed a steep subthreshold slope of 60 mV/dec for TFETs for the first time which was further reducible through proper scaling. Kim et. al. [103] brought into limelight L-shaped

TFETs in which the direction of BTBT and current flow are perpendicular to each other. Significant contribution had also been made in analytical modeling of both planar as well as nanowire TFETs by Vishnoi [104]. Nevertheless, all these TFET devices suffer from many drawbacks. The heavy doping in the channel region leads to various short channel effects. Moreover, in TFETs ambipolarity is suppressed and therefore the same device cannot be reconfigured to behave both as a n- and p-FET and hence a large layout area is required.

2.4 Concept of Ambipolarity in SiNWFETs

Ambipolarity is basically the implementation of the same FET as both n and p type by varying the gate voltage and tuning the source and drain contacts. Research on reconfigurable Schottky barrier MOSFETs and silicon nanowire GAA transistors [106-110] is going on for a considerable amount of time [2, 46, 47]. Now a day's researchers are trying to propose new design approaches for making use of the phenomenon of ambipolarity rather than suppressing it. L. Chua [71] first illustrated the concept of an ambipolar device in the form of 'memristor'. After a lot of research the modern day reconfigurable dual gate device was proposed by A. Heinzig et. al. [2]. Later on, Zhang et. al. [46] also proposed the tri gate ambipolar device architecture.

2.4.1 Device structure

The explanation of the device structure for both dual and triple gate ambipolar SiNWFETs will be given in this section. The dual gate structure [2] is shown in Fig. 2.1. The device consists of a Silicon core which is intrinsic. SiO_2 is used as gate dielectric. $NiSi_2$ metal contacts are present at the source and drain Schottky junctions to form an abrupt metal silicide junction. The work function was chosen to be 0.66 eV because it has been experimentally found that the fermi energy level of $NiSi_2$ and intrinsic Silicon gets aligned at a work function of 0.66eV. SiO_2 was chosen as gate dielectric, mainly because it is experimentally proven that lower trap densities are present at the interface of Si and thermally grown SiO_2 [2]. A Schottky barrier of 0.66 eV for electrons and 0.46 eV for holes arises after the formation of $NiSi_2$-Si junction at source and drains contacts. The working of this FET as an ambipolar device largely depends upon the proper tuning of the Schottky junctions with appropriate application of gate voltage [2, 50].

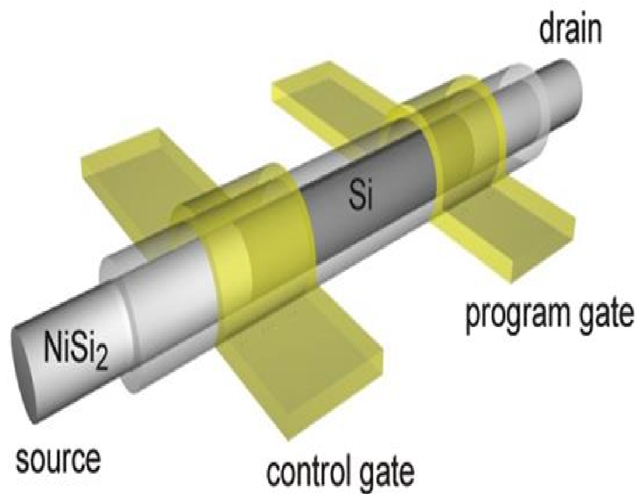


Figure 2.1. Dual gate ambipolar SiNWFET [2].

One of the major difference of this architecture with that of the conventional FET's is that two separate gates are present at drain and source junctions out of which the control gate is used to form the channel with desired carrier type and the polarity gate blocks the injection of alternate carrier [2].

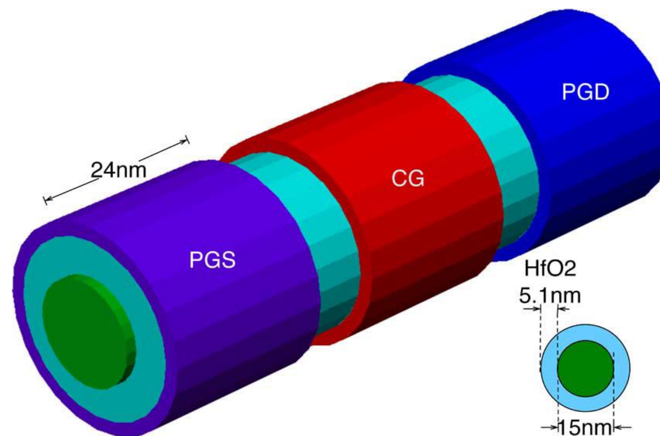


Figure 2.2. Tri gate ambipolar SiNWFET [46].

Similarly, it was demonstrated by Zhang et. al. [46] that with 3 independent gates it is also possible to design ambipolar SiNWFET s [Fig. 2.2].

The tri gate ambipolar device is similar in both design and operation to the dual gate RFET. In contrast to the dual gate structure the tri gate one consists of one more polarity Gate. $NiSi_2$

is used to make the source and drain Schottky junctions to invoke the bend bending [46, 47, 48].

2.4.2 Fabrication of Ambipolar SINWFETs

The conventional Vapor liquid solid (VLS) technique can be used to grow undoped silicon nanowires as depicted by Weber et. al [2]. Si with crystal orientation <112> were chosen. SiO_2 coating of desired thickness was formed by thermal oxidation technique. Nickel reservoirs were deposited at drain and source ends to create the Schottky barriers. After this step annealing was done, following which there is a chance of axial diffusion of Ni into the SiO_2 coated nanowire and Si is transformed into metallic, $NiSi_2$ nanowire segments. After, the successful completion of this step $NiSi_2$/intrinsic−Si/$NiSi_2$ NW heterostructures were obtained surrounded by a shell of SiO_2 of desired thickness. Scanning Electron Microscopy (SEM) can be employed to determine the positions of the $NiSi_2$/Si Schottky contacts. The resulting device as reported by Weber et. al. has a post fabricated nanowire diameter of 20 nm and length 680 nm, above which there is a SiO_2 shell [2, 50].

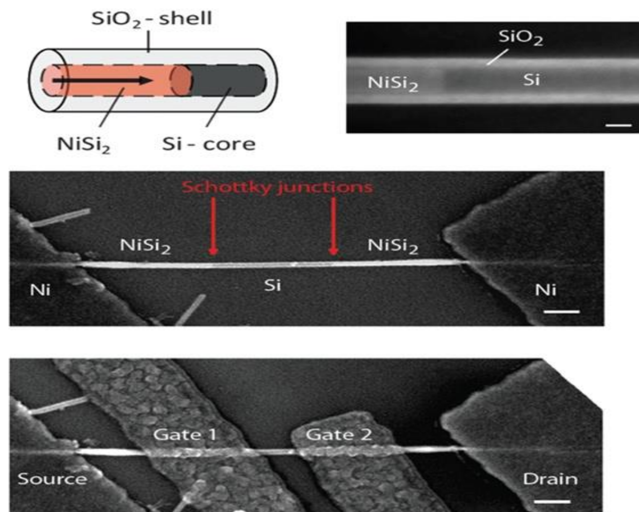


Figure 2.3. SEM images showing fabricated dual gate SiNWFETs [2].

In a similar way fabrication of TIG SINWFET can be done as depicted by Zhang et. al. [46]. The nanowire stack was obtained by the process of Deep Reactive Ion Etching (DRIE). The control gates were patterned in a self aligned manner after patterning the polarity gates. For structure isolation purpose Silicon nitride spacers were employed [2, 46, 48]. To form the

NiSi source/drain contacts a nickel layer was deposited followed by annealing. After the contacts were formed, unreacted nickel was removed by selective etching technique. The SEM image of the tri gate structure as obtained from the literature is given below [46].

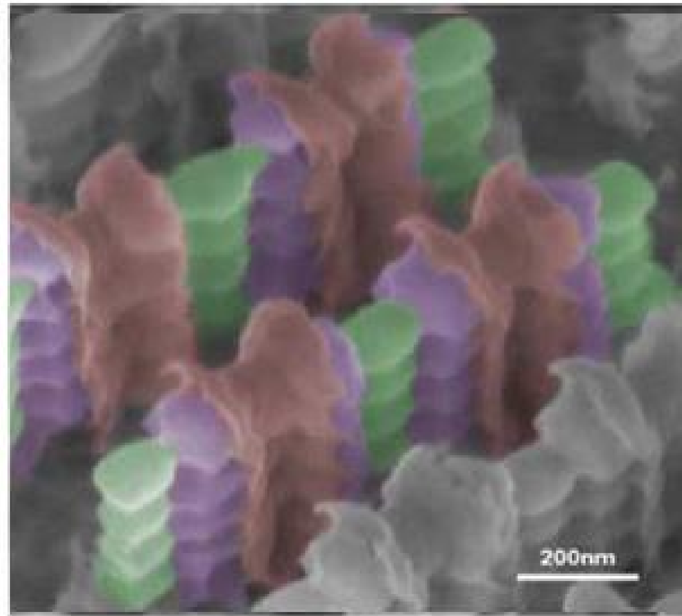


Figure 2.4. SEM images showing fabricated tri gate SiNWFETs [46].

2.4.3 Associated physics and modes of operation

First of all the explanation of the dual gate device is given followed by the tri gate one. Band bending at the two Schottky contacts is the main controlling factor for the flow of a particular carrier type into the Si core channel area and blocking the movement of the other type during alternate application of bias. In the figure given on the next page the left diagram depicts the band bending when the device is behaving as a p-FET and the right diagram shows the band bending when the device is behaving as a n-FET [2]. To program the device to behave as a p-FET, V_{G2} was set to −3 V and V_{DS} to −1 V (Fig. 2.5 left column). The potential applied to V_{G2} blocks injection of electrons at the drain end. V_{G1} was swept from negative to positive values. When V_{G1} potential is negative, injection of holes takes place into the core region at the source end because the band bending is upwards. Similarly, to make the device behave as a n-FET, V_{G2} is biased to 3V and V_{DS} is kept constant at 1V.

Under this biasing arrangement hole injection is stopped at the drain end. At positive values of V_{G1} electrons flow is initiated because of the downward band bending [2].

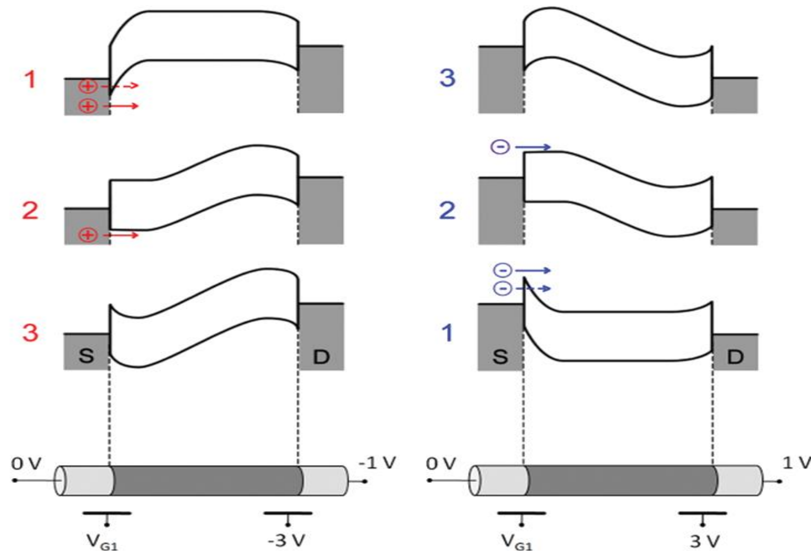


Figure 2.5. Band bending at different biases applied during p-FET and n-FET operation [2].

In Fig. 2.6 there are 3 regions of operation depicted for both p and n FET behaviour. If we start the explanation by taking the n-FET case (the right side curve of Fig. 2.6), region 1 attributes to the highest current as achieved during n-mode operation. This is due to the combined effects of both quantum mechanical tunneling and thermionic emission phenomenon for electrons at this region of operation. Slowly, as the voltage became less positive we can see there is a sharp decrease in the n–FET drain current because of the reduction in the tunneling effect which can be clearly seen in region 2 of the mentioned curve. Lastly, in region 3 we can see that the n-FET current almost became zero because the barrier for is too high for electrons to cross in this case. Similarly, if we want to explain the operation during p-FET case similar physics applies here as well. The left hand side curve of Fig. 2.6 shows that the holes find it easy to tunnel and cross the barrier when the gate bias is higher on the negative side in region 1 of operation for holes. As, the voltage gradually shifts from negative to positive biases we can see that tunneling effect for holes comes down and it results to a reduced p-FET current in region 2 and finally the p-FET drain current becomes almost zero in region 3. The I_d-V_d characteristic is given in Fig. 2.7 for p-FET operation. It

can be seen that the drain current increases as the drain voltage is increased from lower to higher potentials in negative direction [2].

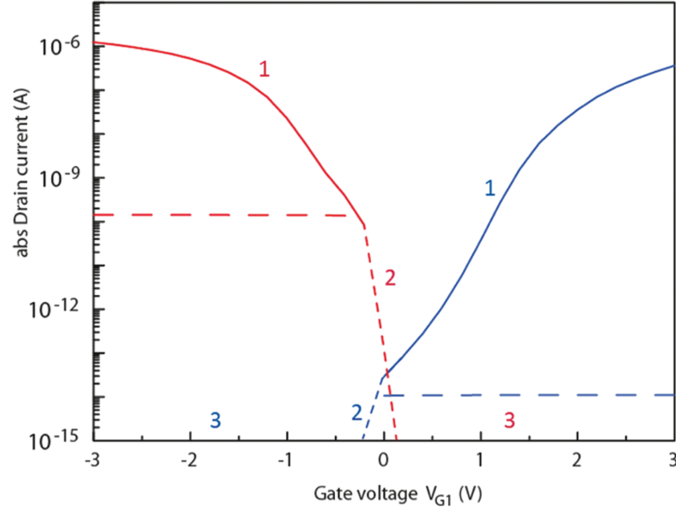


Figure 2.6. Ambipolar behaviour in dual gate SiNWFET [2].

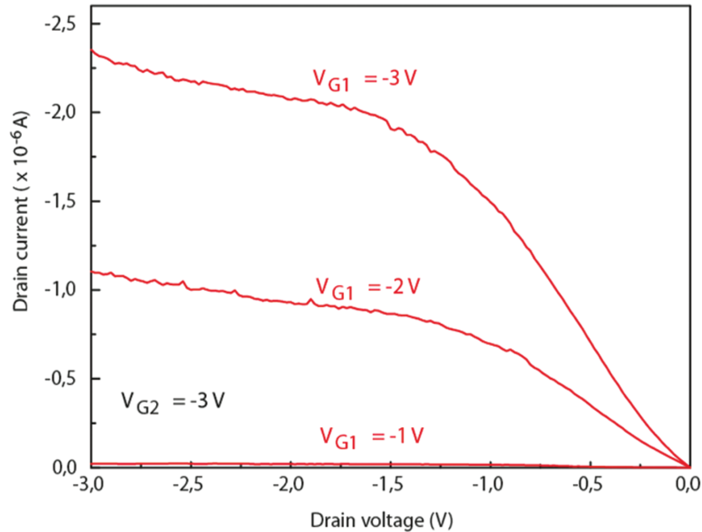


Figure 2.7. Output characteristic during p-FET operation [2].

Now, explanation of the operation and associated physics in triple gate ambipolar SiNWFETs as discussed by Zhang et. al. [46] is given. As, already mentioned in the device structure section, there are 3 mid gap work function metal gates and 2 $NiSi_2$/Si Schottky junctions at the drain and source end. The device can have 2^n states of operation, where n is the number of gates. Since, it is a tri gate device it has 8 states of operation [46]. It has 2 on states (i.e) one as p-FET and one as n-FET under the condition PGS=PGD=CG. Apart from

this, there are 4 different off states and 2 states whose operation is not certain. The 3 metal gates were biased independently to either GND (‘0’) or VDD (‘1’). In Fig. 2.8 the band diagrams corresponding to the 6 states of operation in the tri gate device (except the 2 unused states) are shown.

1) **ON states**: When, we apply PGS=PGD=CG, both for opposite bias we can achieve alternate operation modes for the device. For example when we apply equal positive voltage in both the control and polarity gates the barrier is less for electrons due to the downward band bending and n-FET operation is obtained. Similarly, during the application of equal negative biases at control and polarity gates we get p-FET operation because the up shift in band edge supports the hole tunneling into the nanowire channel. (Fig. 2.8 a and b).

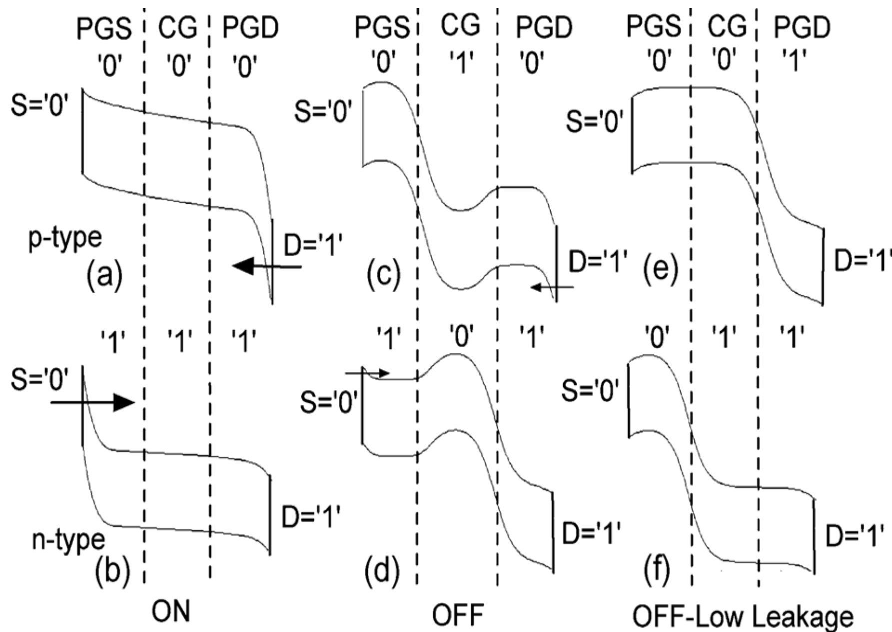


Figure 2.8. Various modes of operation and their corresponding band edge shifts [46].

2) **OFF states**: Now, if the biasing arrangements are reversed i.e. for example we provide high voltage at the control gate and low voltage at both the polarity gates and vice versa, then the device is said to be in standard OFF state. (Fig. 2.8 b and c).

3) **OFF states with negligible leakage**: When we apply opposite biases to drain and source polarity gates, making sure that the source side polarity gate is always at ground potential. For example the control gate is biased at ground (0V) and the source side polarity gate

voltage is also 0V but the drain side polarity gate voltage is V_{dd} or source side polarity gate is at 0V and control gate is at V_{dd} and drain side polarity gate is also at V_{dd} carriers could not tunnel at both source and drain ends due to thick barriers leading to minimum leakage in the device which is termed by Weber et. al. as **"Low Leakage OFF State".** (Fig. 2.8 e and f).

4) **Uncertain states**: Now, if source side polarity gate is biased at higher potential and drain side polarity gate is biased at lower potential the current flow may be ceased due to an unexpected barrier in the inner region resulting into states which we can't predict or **"Uncertain States".** (Not shown in Fig. 2.8).

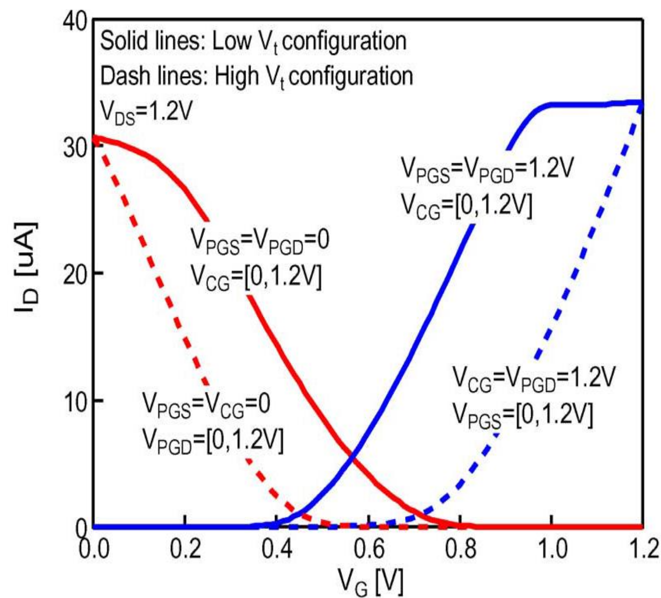


Figure 2.9. I_d-V_g of the triple gate ambipolar FET showing the dual threshold [46].

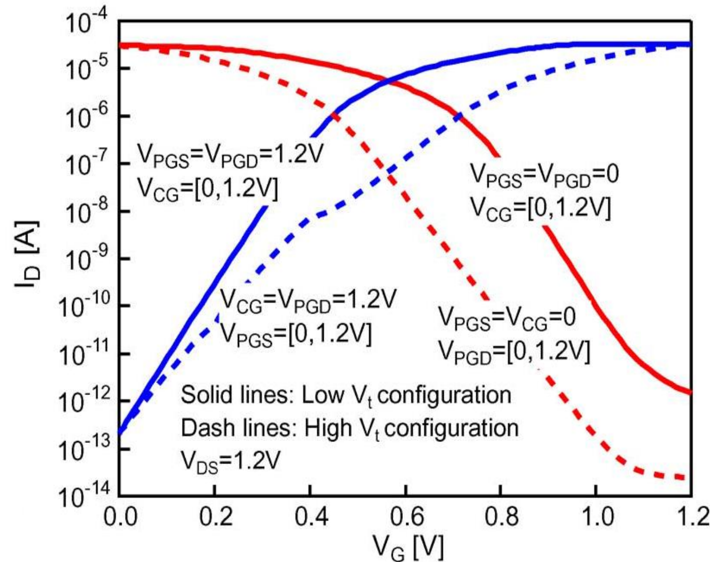


Figure 2.10. Transfer characteristic of TIG SINWFET in log scale [46].

2.4.4 Dual Threshold behaviour and its advantages

Dual threshold is a popular design technique for modern CMOS circuit designer's. This technique can efficiently be applied to control the gate leakage in modern high density ULSI chips. In the critical paths, low V_t devices are applied and in slack paths the device with higher V_t and lower gate leakage are used.

The 3 gate device can have 2 low/2 high V_t n-FET and 2 low/2 high V_t p-FET (Fig. 2.9 and 2.10):-

1) **Low-V_t p-FET**: The voltage applied on both the drain side and source side polarity gates are 0V (GND).

2) **Low-V_t n-FET**: The voltage applied on both the drain side and source side polarity gates are high (V_{dd}).

3) **High-V_t pFET** : When both the control gate and source side polarity gate are at 0V (GND), and drain side polarity gate voltage is varied.

4) **High-V_t nFET** : VDD When both the control gate and drain side polarity gate are at V_{dd} (GND), and the source side polarity gate voltage is varied.

2.4.5 Suitability in Complex Logic Architectures

Logic function mapping using the triple gate RFET as proposed by Zhang et. al. [46] is discussed now. Mapped functions are (a) AOI gate and (b) XOR gate. Both low and high V_t configurations under different connection schemes were taken into account.

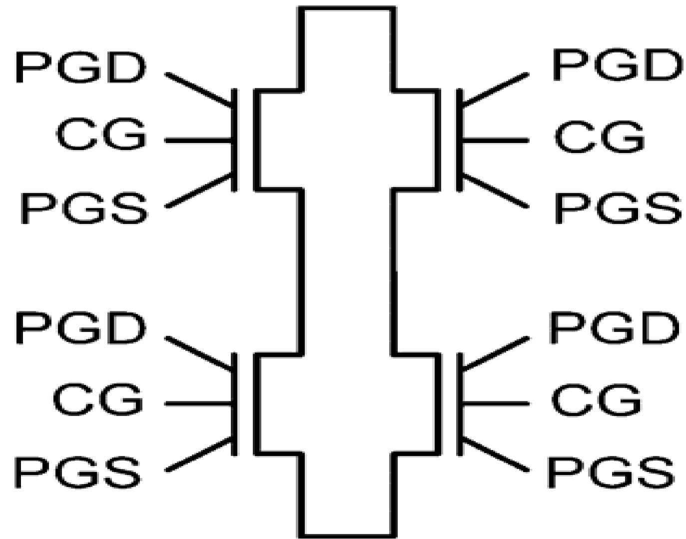


Figure 2.11. Uncommitted Logic Gate Pattern [46]

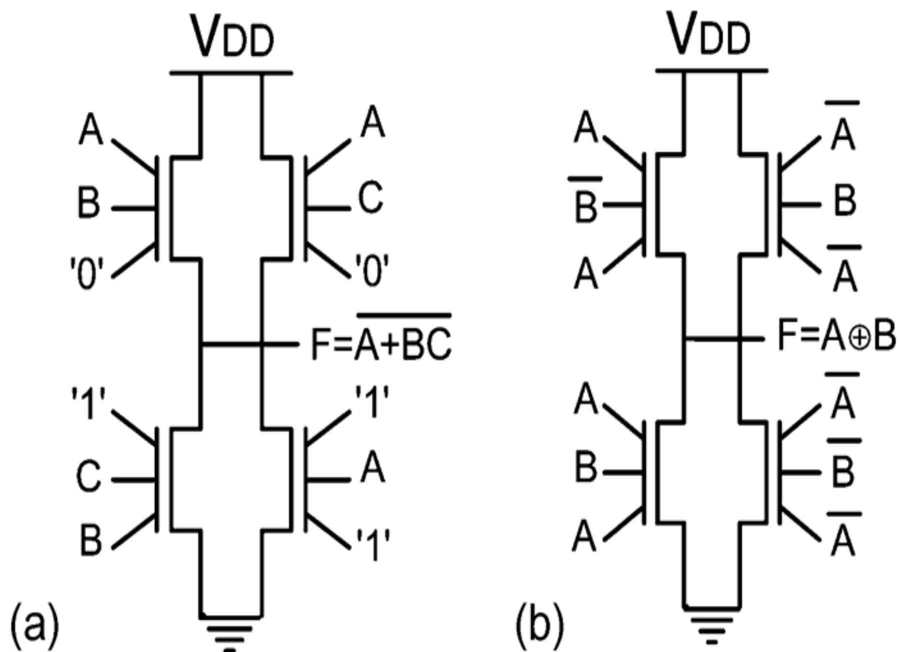


Figure 2.12. AOI and XOR Gates using pattern proposed by Zhang et. al [46]

The 4-T pattern of logic gate into which mapping is done is shown in Fig. 2.11. **Combinational Elements**: Fig. 2.12 shows the AOI implementation. Since it is designed using LVT n-FET and 2 series p-FETs/n-FETs, only 4 transistors are required in this case, and for MOSFET it is 6. In Fig. 2.12 (b), mapping of XOR gate is shown using the same technique.

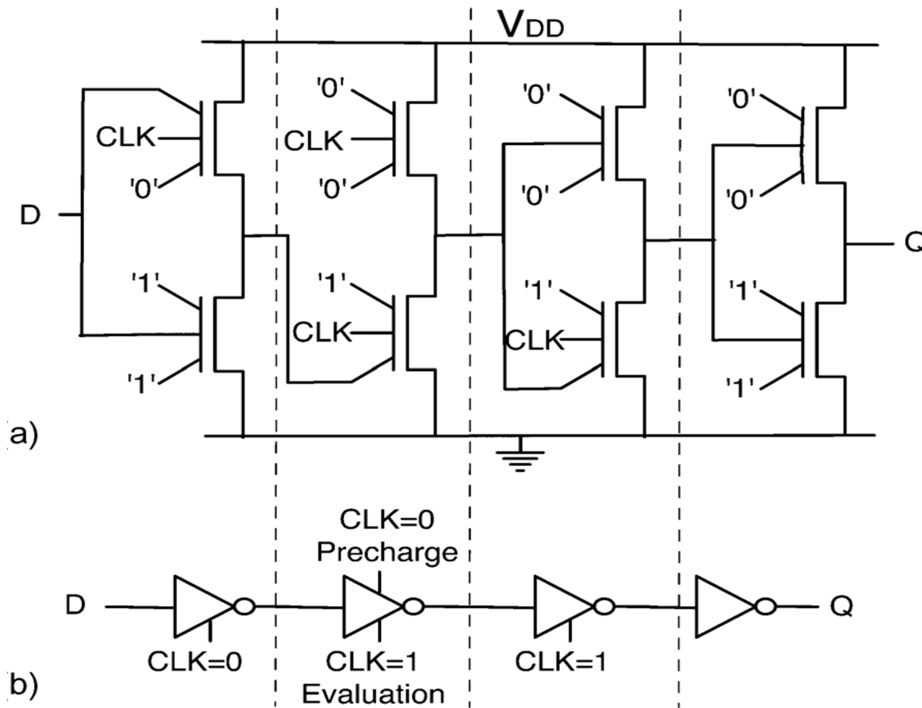


Figure 2.13. TSPC DFF and equivalent Gate level circuit proposed by Zhang et. al. [46]

Sequential Elements: For synchronous logic circuits True-Single-Phase-Clock D-Flip-Flop is a vital block for storing data [46]. Depending upon the configurations of Triple gate ambipolar FET, the flip flop is put on the desired gate pattern [Fig. 2.13 (a)]. It may be noted that less number of transistors than planar CMOS is required in this case. Equivalent circuit of the logic is given in Fig. 2.13 (b). Moreover, in this gate pattern, only one series transistor is present in a single path. Since, an internal node capacitance is not there, switching speed of circuit becomes better. Logic gate delay can also be modulated by applying LVT and HVT configurations of Triple gate SiNWFET as can be seen in Fig. 2.14 [46].

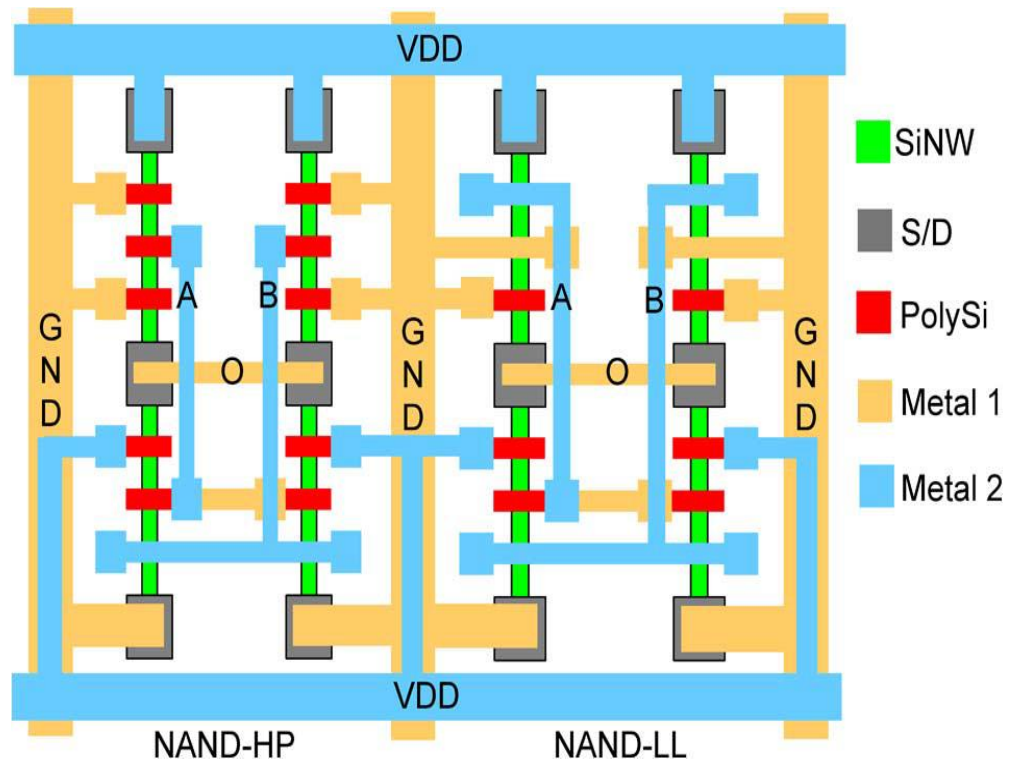


Figure 2.14. NAND gate connection technique [46].

2.4.6 Advantages of RFETs over other Classical and Non-Classical Devices

The increase in off-state leakage current (I_{off}) mainly relates to shrinkage of physical dimensions of devices due to continuous miniaturization over the past several decades, which have increased the short channel effects (SCEs) up to a great extent. Due to the intrinsic nanowire channel used in the reconfigurable FETs, they are free up to a great extent form various SCEs especially from mobility degradation from carrier-carrier scattering. The reported values of off state leakage is in the order of ~10^{-14} resulting in a very high on-off current ratio of 10^9 which make these devices stand apart from various other planar classical device structures. The fabrication complexities are also quiet low as the conventional bottom-up approach is adopted in most of the literatures. From circuit design point of view it is reported that these devices provide the opportunity to minimize the number of transistors while designing complex logic architectures. For example in design of exclusive OR (XOR) and NAND gate it is depicted that only 4 transistors is enough in contrary to 8 transistors in case if planar devices (MOSFET). The same is shown below [48].

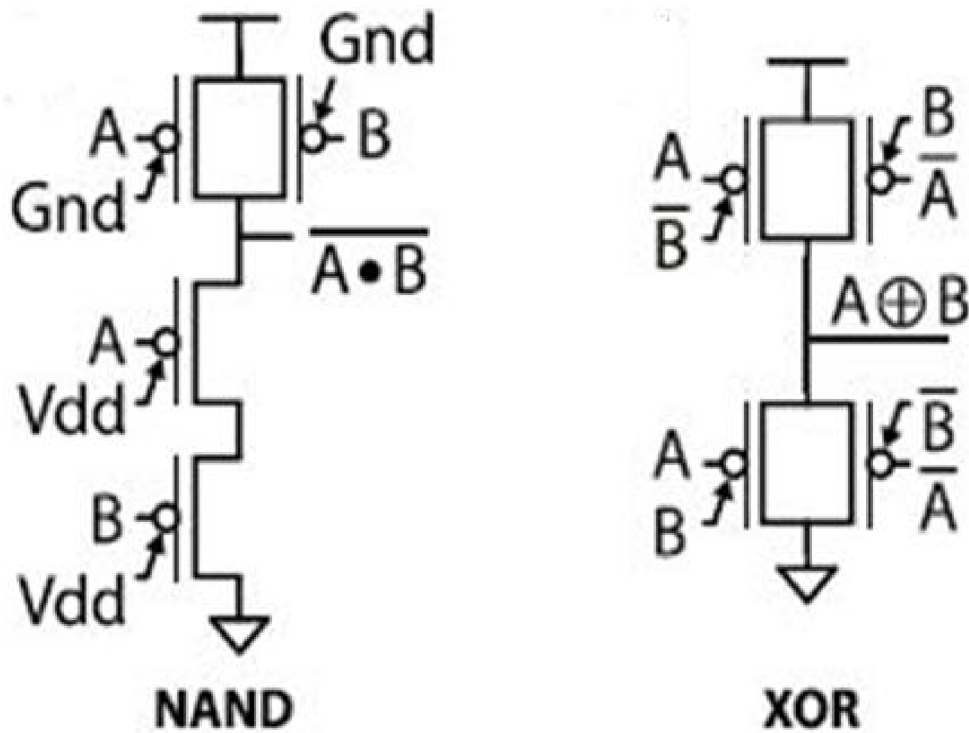


Figure 2.15. Implementation of complex architectures with reduced number of gates [48].

2.5 Technical Gaps

Based on the literature survey, it is observed that device researchers across the globe are showing immense interest towards this newly proposed reconfigurable FET technology which can become an ideal replacement to the conventional planar and Fin shaped FETs. Like any upcoming technology, RFETs also have their own set of limitations and challenges. The following research gaps have been observed based on the literature review:

a) The ambipolar devices reported so far have low on-currents like other devices which are dependent on BTBT for their on-current generation like tunnel FETs (TFETs). Though a lot of device architectures have been proposed in case of TFETs, very little is reported in the literature so far about reconfigurable FETs regarding this problem. Research can be done to improve the current drive in this kind of devices.

b) It is an well established fact that use of spacer oxide has led to the improvement in device performance in case of devices like TFETs, FiNFETs etc. It will be very interesting to study

the effect of spacer technology in this kind of devices with an aim to enhance the device performance and also in reducing the leakage current.

c) Extensive circuit analysis using ambipolar device has not been done yet to account for the reduction in silicon area. To achieve this high fan-out and high I_{ON} is required.

d) Co-design of both analog and digital circuits has not been studied yet.

e) Though dual-threshold behavior has been reported using these devices using a tri gate device but a robust dual threshold technology is yet to be reported. Moreover, dual threshold characteristics using a dual gate RFET is not yet reported in any literature.

f) Development of a compact analytical model for ambipolar devices is still not available. It is important as well as interesting for further understanding of the device physics.

h) Effect of temperature on device performance is yet to be studied. Since the subthreshold current of the device is dependent on thermionic emission phenomenon, which is in turn temperature dependent, it would be of great interest to study the thermal performance of the device.

Chapter 3

Source/Drain (S/D) Spacer Based Dual Gate (DG) RFET and its Optimization

3.1 Introduction

One of the major drawbacks of conventional CMOS technology is the inability to reconfigure it. Over many decades, circuits which are reconfigurable are used for providing various functions as desired after manufacturing. By mainly two different approaches, the reconfigurability of logic function is implemented. The information required is transmitted pathways to various destination units in the older method which is also known as the coarse grain approach. An example of this method is the reconfigurable FPGA, programmable nanoprocessor circuits etc. reported by the Lieber research group [52].

When the logic functions are being programmed at each constituting block of the circuit, the approach is known as fine grain. The major advantage of this technique is that more complex circuits can be designed in compact form as in case of a memristor. The main drawback from which a memristor suffers is that every single time before the targeted logic function can be actually implemented, we must program the electrical behaviour of the same by using a voltage pulse and thus an extra functional unit is required for this reason. Thus the main necessity from the point of view of circuit application is to develop a transistor the polarity of which can be tuned as desired just by changing the external gate bias. After many years of research the nanotransistor proposed by Heinzig et. al. in 2012 [2] is found to be capable in providing unipolar conduction for both carrier types and is able to fulfill all the above mentioned criterions. The concept of reconfigurability in this device relies on controlling the transport of charge carriers over the metal-semiconductor Schottky contacts. Moreover, since it is possible to implement this device in complementary logic, it proved to be an additional advantage over various Schottky barrier FETs (SBFETs) discussed previously in the literature. The nanowire geometry is important in view of the electrostatic coupling required between the metallic contacts and the semiconductor. The metallic junctions should be such that the hetrojunction interface to silicon within the nanowire is of high quality possessing atomic level sharpness and a Schottky barrier should arise naturally for electrons (and holes). The vertical electric field resulted due to the gate voltage applied

exactly peaks at the Schottky junctions, which further improves the control of gate over the nanowire channel and turns out to be an extra benefit provided by the geometry of the device. The functioning of this nano structure as a classical ambipolar device is based on blocking a particular type of carrier to change the conductance from one to the other. This is done by controlling the energy band bending in the nanowire active region. The device concept caught the attention of many device researchers across the globe because of its straight forward operation over all the top gated combinations for reconfigurability available previously in literature and also due to the relative ease of fabrication by the conventional bottom up process. In the next few years, keeping this device as a motivation, other research groups also proposed various reconfigurable transistor architectures having almost the same device physics and principle of operation. One of those is the tri gate RFET device implemented by Zhang et. al [46]. It was shown that dual threshold configurable circuits and combinational logic blocks with less number of transistors than planar CMOS is achievable using this geometry. The implemented dual V_t circuits were found to overcome various drawbacks such as requirement of additional process steps affecting the fabrication cost and regularity of overall layout as exhibited by state of the art multi threshold designs which are achieved by using conventional techniques like adaptive body biasing and gate work function engineering by using various gate materials.

Apart from all the advantages it provides, unlike any other newly proposed device concept, it has got various limitations too. The reported current drive when the device operates in saturation is not as high as other tunneling transistors such as tunnel field effect transistors (TFETs). Moreover, reduction of gate leakage is extremely important not only for circuit applications but also for having a higher on-off current ratio. Since an additional metal gate is required in the tri gate architecture, the implementation of dual threshold design using a DG RFET is also a challenge.

Keeping all of these points in mind a modified DG RFET architecture having source/drain spacers is proposed in this work to make this reconfigurable device concept fully compatible to today's mainstream low power digital design. The remaining part of this chapter is organized as follows. Section 3.2 describes the proposed device structure and its operation along with the simulation methodology used in this work. Section 3.3 discusses the calibration of our simulation set up with that of the experimental device and also illustrates

the inherent device physics behind the spacer induced performance enhancements. Moreover, in this section the impact of spacer material on device performance is also discussed and the same is benchmarked with that of the experimental conventional DG RFET and TIG SiNWFET. In section 3.4 the optimization of various important device parameters such as spacer length (L_{sp}), spacer material type, gate dielectric and its thickness (t_{ins}) and integrate gate distance (d_{G1G2}) is discussed in details. The chapter concludes with a summary in section 3.5.

3.2 Proposed S/D Spacer DG RFET, Operation and Simulation Framework

3.2.1 Proposed Device Structure and Simulation Methodology

The proposed source drain spacer based device structure is shown in Fig. 3.1. The experimental Schottky barrier FET (SBFET) of [2] is used as a reference device for this research. Since, the Si/$NiSi_x$ junction is not kept inside the gate, the proposed architecture is thus termed as the *underlap* device architecture. The part of the channel which not in cover of the gate near the source and drain junctions is termed as the gate channel underlap region (L_{GCU}) and the part of the gate channel underlap region where high κ spacer is absent is termed as the spacer channel underlap region (L_{SCU}) as shown in Fig. 3.1. This is one of the major architectural dissimilarities of the proposed device with that of the conventional *non-underlap* RFET device architecture. TiO_2 in Rutile phase (having dielectric constant in the range of 50-80) [53] is chosen as the most suitable gate oxide to replace SiO_2 [2] for a better performance in the off-state and improving the electrostatics of the device. To keep intact the high quality interface properties, a thin layer of SiO_2 may be deposited beneath the high κ dielectric while the device is fabricated. The device consists of a lightly p-doped (10^{15} cm^{-3}) silicon nanowire which has a length of 680nm and diameter 20nm surrounded by a 10nm shell of TiO_2 (EOT=0.67nm). $NiSi_2$-Si Schottky junctions with Schottky barrier height (SBH) of 0.66eV for electrons and 0.44eV for holes are present at the source and drain ends. On each side of 200nm midgap metal gates (work function=4.2eV) with inter gate separation (d_{G1G2}=270nm), HfO_2 spacers of length (L_{sp}) 2nm and thickness (t_{sp}) 10nm (same as that of gate dielectric) are present. Gate G_1 acts as the control gate which controls the formation of the channel with desired carrier type, and gate G_2 acts as the polarity gate which blocks the injection of alternate carrier. It may be noted that, for incorporating the thin spacer layer, the

Schottky contact in the proposed device is kept away from the gate intentionally at a distance of 5nm unlike as in [2]. To model the impact of air spacer in TCAD simulations and describe the interaction between gate and Schottky contact correctly, a low-κ spacer (ε_r=1) is placed in

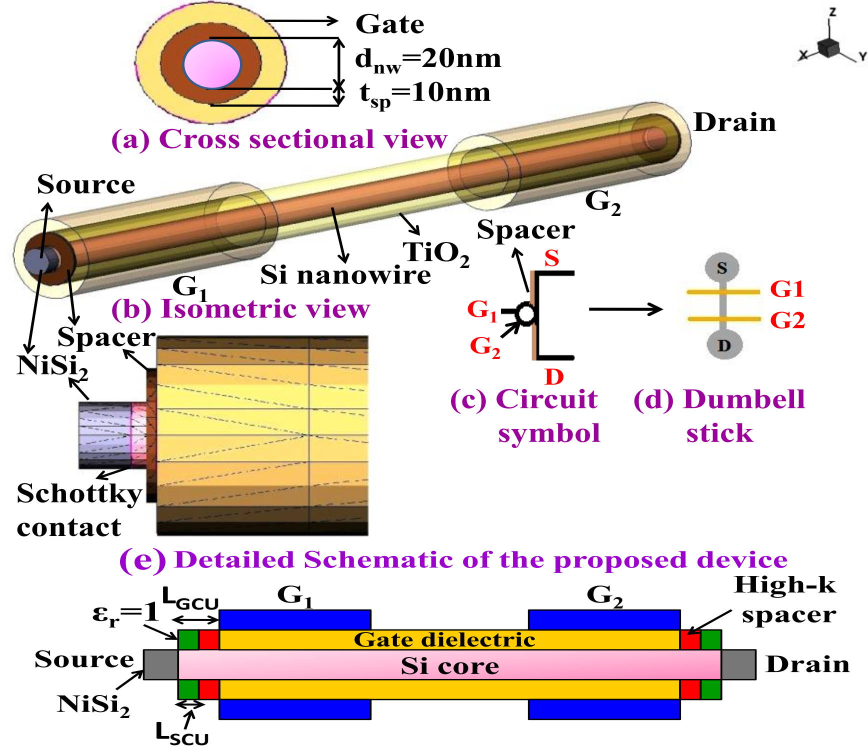


Figure 3.1. (a) Cross sectional view (b) Isometric view showing the position of S/D spacers and mid-gap metal gates along with zoomed view from one side to illustrate the position of Schottky contact (c) Circuit symbol (d) Dumbell-stick diagram (e) Detailed Schematic of the proposed device.

between S/D electrodes and high-κ spacer. A room temperature drift diffusion model is applied within the silicon core and both barrier tunneling and barrier lowering models (Wentzel-Kramers-Brillouin approximation) along with thermionic emission model (because the subthreshold current is controlled by thermionic emission phenomenon [2, 46]) are applied at S/D junctions to take into account charge transport of carrier and 2-D quantum confinement effects. Philips unified mobility model (PhuMob) is used to describe mobility degradation due to carrier-carrier scattering mechanisms and a field dependent mobility model having high field corrections is used to consider velocity saturation of carriers at higher electric fields. Electron and hole tunneling masses are chosen as 0.19 m_o and 0.16 m_o

respectively which is accordance with the literature [47]. The recombination terms include the Shockley-Read-Hall (SRH) expression for recombination (both temperature and doping dependent), recombination via band-to-band tunneling and Auger effects. The device dimensions are matched with experimental device [2] and the setup is implemented in *Synopsys Sentaurus 3-D TCAD* [105] tool.

3.2.2 Working Principle

The device operates on alternative usage of control gate (G_1) and polarity gate (G_2) [refer to Fig. 3.1 (e)]. G_1 controls the formation of channel by injecting a particular carrier type and G_2 blocks the alternate carrier injection into the nanowire active region. Fig. 3.2 (a) and (b) show lateral band diagrams of the device for both n and programs at various polarity gate voltages with control gate voltage fixed at + 3V for n-type and -3V for p-type device. Since the barrier is steeper in the drain side, so we require a larger polarity gate voltage to stop the ambipolar currents.

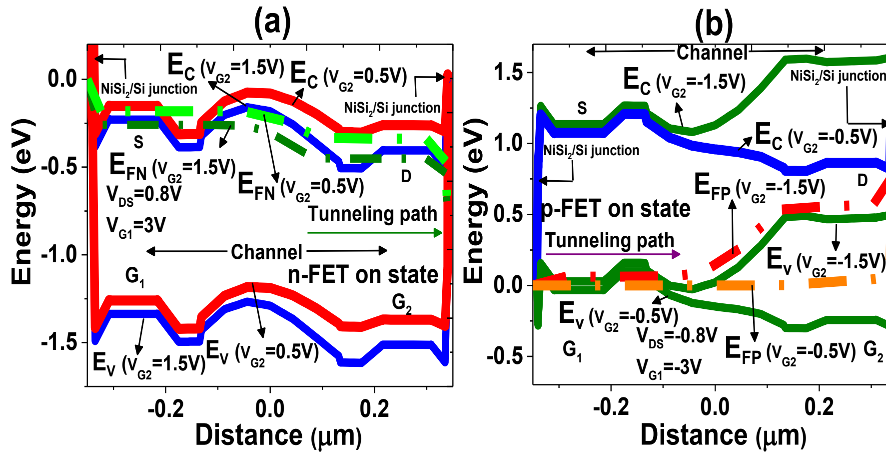


Figure 3.2. Band diagrams of the device in lateral direction for various gate voltages for (a) n-FET on state (b) p-FET on state.

It may be noted that the portion at which all (valence and conduction) band edges merge together is the point of formation of $NiSi_2$/Si Schottky (metallic) junctions. The electrons tunnel from the source end of the device which is therefore be referred as the tunnel source, towards the drain end which is thus referred to as the tunnel destination. To make the device act as a n-FET, both drain and polarity gate (G_2) are kept at fixed positive voltages

and control gate bias (V_{G1}) is swept to higher positive values which results in downward band bending, thereby allowing the electrons to tunnel from source side into the nanowire core region. With alternate biasing arrangements, upward band bending can be initiated, which assist hole tunneling and the device thereby acts as a p-FET. When positive potential is applied at the control gate during n-program, a large number of empty states are actually separated by a huge number of filled states separated by a steep tunneling junction which is a favourable condition for BTBT to take place. Due to the combined influence of drain and polarity gate voltage the band edge near the drain end is pinned down further [Fig. 3.2 (a)] which blocks the tunneling of electrons from drain to source. Similar explanations also hold true for the p-program with alternate biasing.

3.3 Simulation Calibration and Spacer Induced Performance Enhancements

3.3.1 Calibration with Experimental Data

To verify the correctness of our simulation set up we have calibrated it against the experimental data of [2] at T=300 K as shown in Fig. 3.3.

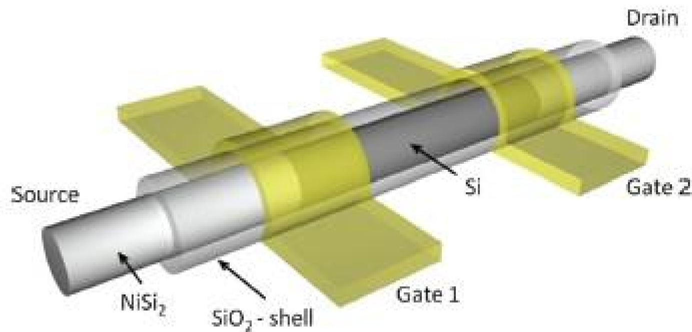


Figure 3.3. Experimental device with length 680nm and gate length 200nm [2].

Experimental Device [2]	Length of nanowire (nm)	Gate length (nm)	Oxide thickness (nm)	Nanowire radius (nm)
V_{DD} (V)	680	200	10	10

To calibrate the simulation results with the experimental data, the same device dimensions as mentioned for the experimental RFET are reproduced in *Sentaurus 3-D TCAD* tool.

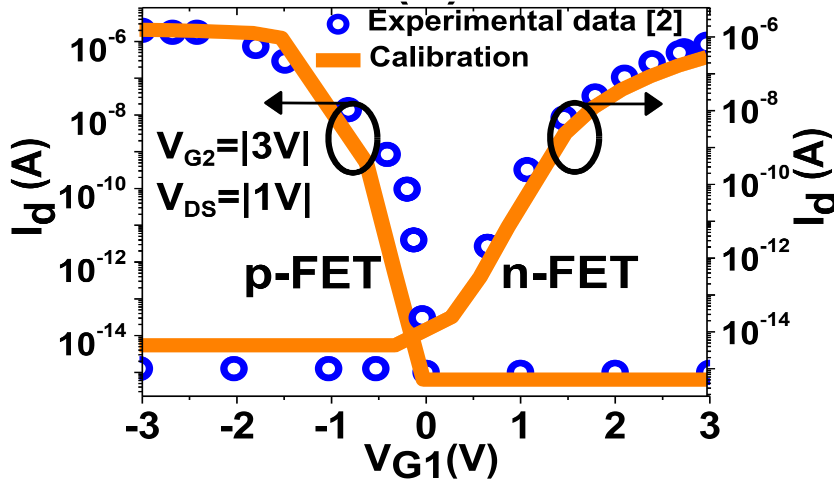


Figure 3.4. Calibration of I_D-V_{G1} characteristics with experimental device [2].

The physical parameters adjusted for calibration are electron and hole tunneling mass (m_{te} and m_{th}), electron and hole Schottky barrier height (φ_{bn} and φ_{bh}), gate metal work function (φ_{ms}), $NiSi_2$ work function. Moreover, the device parameters like gate oxide thickness (t_{ins}), silicon film thickness (t_{si}) and channel length (L_{si}) are also kept unaltered to successfully produce the transfer characteristics of the experimental RFET [2]. It can be seen from Fig. 3.3 that the simulated transfer characteristics for both n- and p-FET match the experimental one with great accuracy at V_{DS}=1V and V_{G2}=3V, validating the accuracy of our simulation set up and different models used by us. The threshold voltage obtained from calibration for n (p-FET) is 0.435V (-0.476V).

3.3.2 Physical Explanations behind the Performance Improvements

Fig. 3.4 shows the comparison of extracted I_D-V_{G1} characteristics of the proposed device with experimentally reported device [2]. It may be seen from the figure that the proposed RFET shows higher on-current for both n- and p-configurations as compared to the traditional RFET topology.

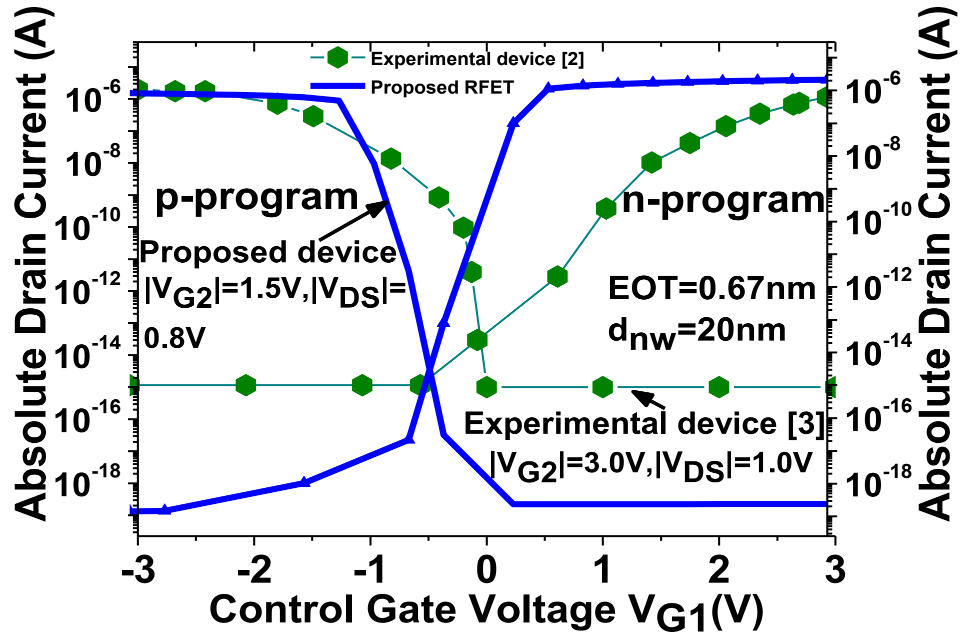


Figure 3.5. Comparison of typical simulated I_D-V_{G1} characteristics (lines) of proposed device with that of experimental device [2] (dotted).

The improvement in ON current attributes to rise in electric flux by 0.22 MV/cm (0.08 MV/cm) within the high-κ spacer leading to 35.2% (12.3%) up (down) shift in conduction band edge for n (p-FET) as can be seen from Fig. 3.5 (a), (b), (c), (d). The shift in band edge for electrons is near source end of the device since electron tunnels from source to drain. Similarly, for holes the band edge shift is near the drain edge. This eventually increases tunneling probability for both carrier types through the thin barriers at ON state. As a result of this, more number of electrons (or holes) tunnel from their respective tunnel source towards their tunneling destination. The peak value of the electric field is obtained at the metal silicide Schottky junctions as expected. The excess field is mainly due to external fringe field emanating from outer gate periphery and terminating into $NiSi_2$/Si Schottky contacts.

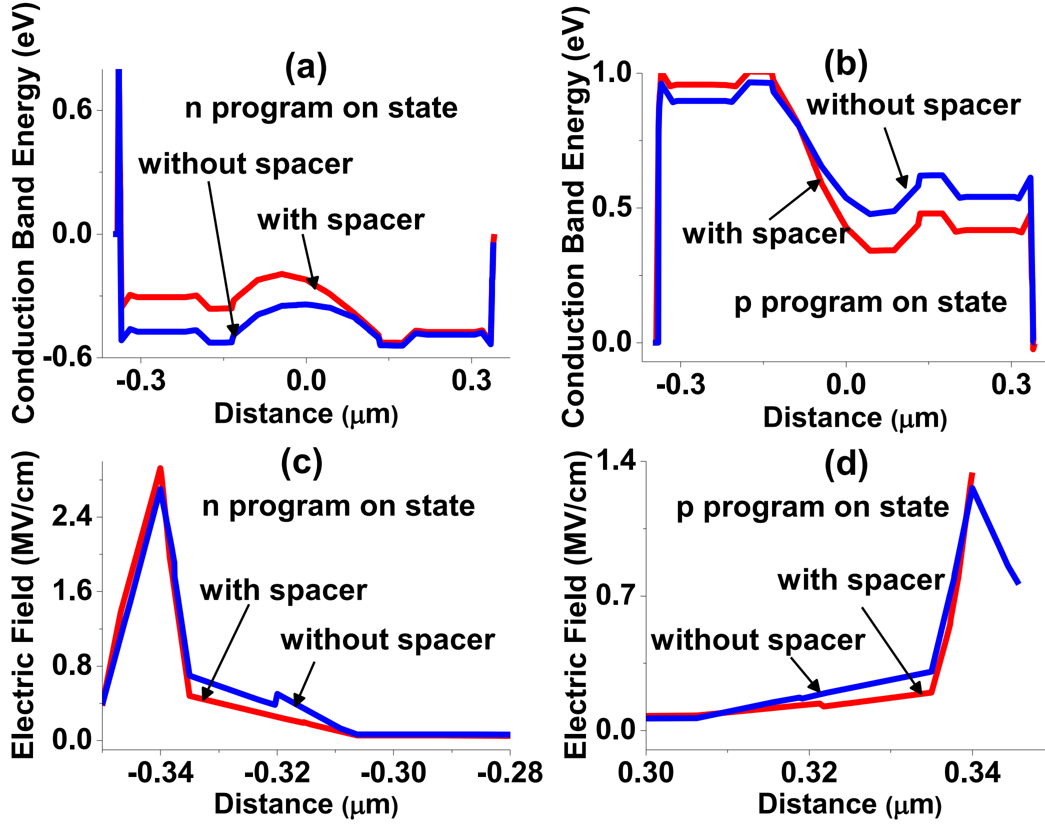


Figure 3.6. (a) Conduction band edge for n-program (b) Conduction band edge for p-program (c) Electric field variation for n-program (source side) (d) Electric field variation for p-program (drain side) in ON state for proposed device along the lateral direction (with and without HfO_2 spacer).

Maximum transconductance of 0.14 μS and 0.03 μS is obtained for n and p-FET respectively. The subthreshold current for n (p-FET) is found to be 2.16×10^{-17} A (3.09×10^{-17} A), as compared to 4×10^{-15} A for both configurations in [2]. The substantial reduction in gate leakage current cannot be explained by enhanced electrostatic integrity due to HfO_2 spacers alone. The ability of high-κ gate dielectric (TiO_2) to combat OFF-state leakage better than SiO_2 with a same physical thickness should also be taken into consideration. This is one of the major advantages of using TiO_2 as a replacement gate dielectric to SiO_2. Performance improvements of the device with high κ spacer are summarised in Table 3.1.

Table 3.1 Device performance with and without spacer

Performance parameters	Device	
	With spacer	Without spacer
I_{ON} n(p-FET) (×10^{-6} A)	2.13 (0.826)	0.328 (0.608)
I_{OFF} n(p-FET) (×10^{-17} A)	2.16 (3.09)	1.94 (3.10)
I_{ON}/I_{OFF} (×10^{11}) n(p-FET)	0.986	0.169 (0.196)
S/S n(p-FET) (mV/dec)	78.9 (91.50)	118.35
Schottky Barrier Height n(p-FET) (eV)	0.897	1.263 (0.9744)

Integrate distance (d_{G1G2}) of the RFET, i.e. the space between two gates has large impact on device parasitic and hence also on the device performance. But unfortunately its impact has not yet been studied for RFETs in any of the literature. The inter-gate distance (d_{G1G2}) scaling performance of the device for n (p-FET) is shown in Fig. 3.6 (a) and (b). It may be noted that reconfigurability is maintained for large variations in d_{G1G2} for both n- and p-programs of the proposed RFET. A significant reduction in I_{ON} for both n- and p-FET with increasing distance between control and polarity gates which is clearly reflected from the figure is mainly because of an increase in the parasitic resistance with an increased distance between gates. The same also holds true for the slight increase in S/S for p-FET although for n-FET the S/S remains almost unchanged over the entire variation in d_{G1G2}. Impact of spacer material on device behaviour is also shown for reference in Table 3.2. The various spacer materials used are SiO_2 (κ=3.9), Si_3N_4 (κ=8), HfO_2 (κ=25) and TiO_2 (κ=60). It is seen that although TiO_2 as spacer material improves the ON current, it provides a degraded I_{ON}/I_{OFF} ratio as compared to HfO_2 due to increase in OFF state current. This relates to the convergence of fringe electric filed lines back on to the gate at higher κ_{sp} value. On the other hand, though I_{ON}/I_{OFF} is highest for Si_3N_4 spacer, the ON current is almost 50% that in case of HfO_2. So looking at both on current and on-off current ratio TiO_2 gives the best performance among all the spacer materials we have taken into consideration.

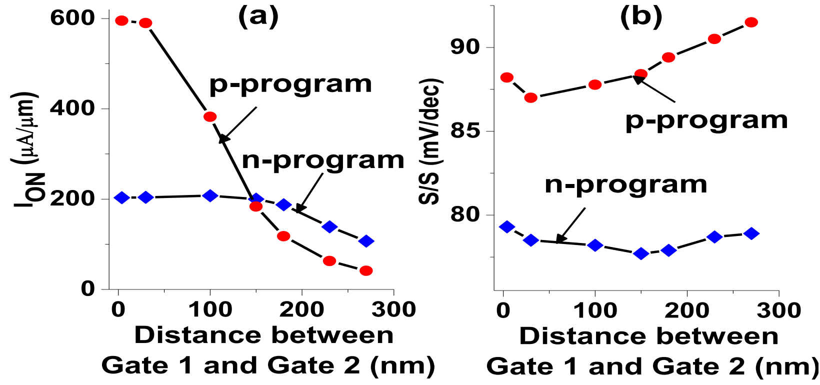


Figure 3.7. (a) I_{ON} versus inter-gate distance (d_{G1G2}) for n (p-FET) (b) S/S versus inter-gate distance (d_{G1G2}) for n (p-FET).

Table 3.2 Variation in device performance with spacer material

Spacer material	I_{OFF} n (p-FET) ($\times 10^{-17}$ A)	I_{ON} n (p-FET) ($\times 10^{-6}$ A)	I_{ON}/I_{OFF} ($\times 10^{11}$)
SiO_2	1.18 (3.1)	0.829 (0.736)	0.702 (0.237)
Si_3N_4	0.478 (3.11)	1.29 (0.778)	2.69 (0.25)
HfO_2	2.16 (3.09)	2.13 (0.826)	0.986 (0.267)
TiO_2	4.89 (3.1)	2.7 (0.853)	0.552 (0.275)

The dual threshold behavior of the proposed device is portrayed in Fig. 3.7. In order to portray the dual-V_t property for the first time using 2 independent gates instead of 3 as in [55], similar biasing arrangement as [55] is adopted except G_1 resembling biasing of polarity gate (PGS) and G_2 matching that of control gate (CG) for n-FET (HV_T and LV_T), whereas in case of p-FET (HV_T and LV_T) biasing of G_1 and G_2 correspond to control gate (CG) and polarity gate (PGD) respectively. With reduced number of gates less number of power supplies are required for maintaining ambipolarity, which results in low power application.

We obtained 64.10 % and 62.96% reduction in subthreshold slope for LV_T n (p-FET) whereas the off current reduces by 0.87×10^6 (49.4×10^3) for HV_T n (p-FET) and 20.6 (103.8) for LV_T n (p-FET) respectively, as compared with (TIG) SiNWFET reported in [55] for similar explanations given earlier.

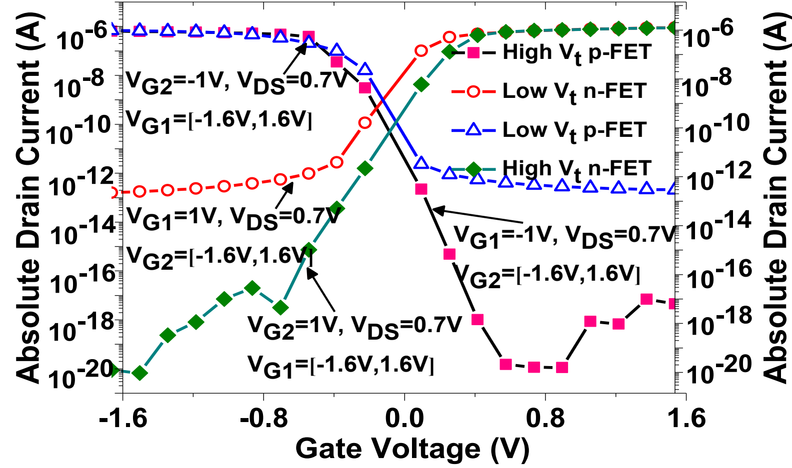


Figure 3.8. Transfer characteristics of the proposed device in logarithmic scale illustrating the dual V_t property.

The difference in threshold voltage between the low and high V_t configurations for n (p-FET) is reduced by 53.48% (58.33%) compared to [55], implying more robust circuit design. It is interesting to note that the LV_T mode with earlier turn-on can provide higher operating speed. However, a trade off must be made with increased gate leakage in comparison to HV_T configurations. The proposed device performance is benchmarked with dual gate RGFET [2] and TIG SINWFET [55] and the performance improvements are summarized in Table 3.3.

Table 3.3. Performance comparison of dual gate RGFET [2], TIG SiNWFET [55] and proposed device

Device	Dual gate RGFET [2]	TIG SiNWFET [55]	Proposed
V_{DD} (V)	1	2	0.8
I_{ON} n (p-FET)	5.3 (94)	10.3 (5.9)	107 (41.3)
I_{OFF} n (p-FET)	4×10^{-15} (4×10^{-15})	1×10^{-12} (315×10^{-15}) (HV_T)	2.16×10^{-17} (3.09×10^{-17})
I_{ON}/ I_{OFF} n (p-FET)	6×10^{7} (1×10^{9})	3×10^{5} (6×10^{5})	0.986×10^{11} (0.267×10^{11})
S/S n (p-FET)	220 (90)	207 (155)	78.9 (91.50)

It is observed that, apart from considerable reduction in I_{OFF}, the device offers V_{dd} scaling of 60% (20%) along with 64.1% reduction in S/S for n-FET and 61.8% (40.9%) for n (p-FET)

compared to [2] and [55] respectively.

3.4 Parameter Optimization for the Proposed Device

3.4.1 Spacer Length (L_{sp}) Optimization

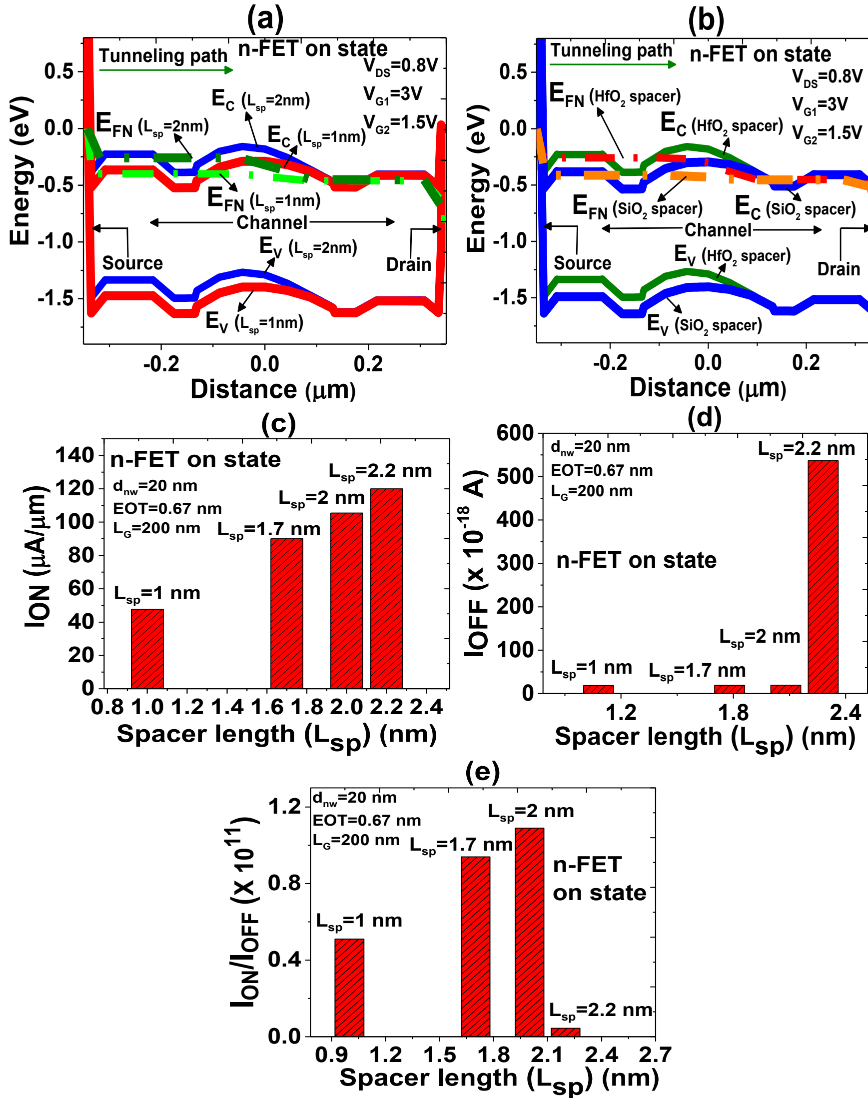


Figure. 3.9. Impact of variation in (a) spacer length (L_{sp}) and (b) spacer material on lateral band diagram of the device (c) I_{ON} vs spacer length (L_{sp}) (d) I_{OFF} vs spacer length (L_{sp}) (e) I_{ON}/I_{OFF} vs spacer length (L_{sp}) for n-FET on state.

We have shown the variation in band edge for the following cases: varying spacer length (L_{sp}) and varying spacer-κ at fixed gate and drain biases for n-FET ON state [Fig. 3.8

(a) and (b)]. The band overlap is now between channel and drain regions [see Fig. 3.8 (a), (b)] because the polarity gate voltage is kept fixed. As L_{sp} is increased from 1nm to 2nm the device displays 50.01% higher carrier velocity which relates to the improved electrostatic coupling near the Schottky junction at higher spacer length values. The 33.33% up-shift in band diagram with increase in spacer length from 1nm to 2nm is mainly due to an increase in lateral fringe lines concentration near the Schottky junction at higher L_{sp} because of better coupling between the source and the gate metal through the spacer which is in consistence with the findings of Chattopadhyay et. al. [54] showing the impact of spacer oxide on another class of transistor, tunnel FETs (TFETs). The shift in band edge in turn reduces the minimum tunneling width and allows more electrons to tunnel from source to drain resulting in 72.25 μA/μm increase in normalized on current with L_{sp} increase from 1nm to 2.2nm as shown in Fig 3.8 (c). To have a better physical insight into this phenomenon we have plotted the fringe field contour plots of the device near the source side for L_{sp}=1nm and 2nm respectively as shown in Fig. 3.9 (a) and (b). It can be observed from the figure that the concentration of fringe electric lines are more dense for 2nm spacer length with a 16.10% rise in E_{max} resulting an increase in carrier tunneling rate near the $NiSi_2$/Si Schottky junction which is clear from the simulated BTBT rates in Fig. 3.9 (c). Similar explanations can also be given for 36.8% and 27.27% up-shift in band edge in case of HfO_2 spacer as compared to SiO_2 and Si_3N_4 as observed from Fig. 3.8 (b). Due to higher κ value, HfO_2 spacer can terminate the outer fringe field lines (those emanating from outer edge of the gate electrode and terminating into $NiSi_2$/Si Schottky interface through the spacer material) better as compared to SiO_2 and Si_3N_4, resulting in more upward band bending near the tunnel source. It is worth mentioning that though higher spacer lengths facilitate increase in current drive, but beyond L_{sp}=2nm (which is used as optimum in this work) the I_{OFF} can be seen to increase significantly [Fig. 3.8 (d)] causing I_{ON}/I_{OFF} ratio to deteriorate [Fig. 3.8 (e)]. This accounts to the parasitic injection of electrons at drain contact at higher L_{sp}. Table 3.4 shows the 2-D electron velocity comparison in the silicon nanowire core at V_{G1}=3V, V_{G2}=1.5V and V_{DS}=0.8V as a function of spacer length, thickness and spacer material type. With increase in L_{sp} from 1nm to 2nm the device shows 50.01% higher carrier velocity which relates to the

Table 3.4 Variation in electron velocity with spacer attributes

Performance parameter	Variation with spacer attributes	
Maximum Electron velocity (cm/sec)	**L_{sp}=1nm**	**L_{sp}=2nm**
	3.9×10^6	7.803×10^6
	t_{sp}=7nm	**t_{sp}=10nm**
	6.7×10^6	7.803×10^6
	Spacer κ=3.9	**Spacer κ=25**
	3.7×10^6	7.903×10^6

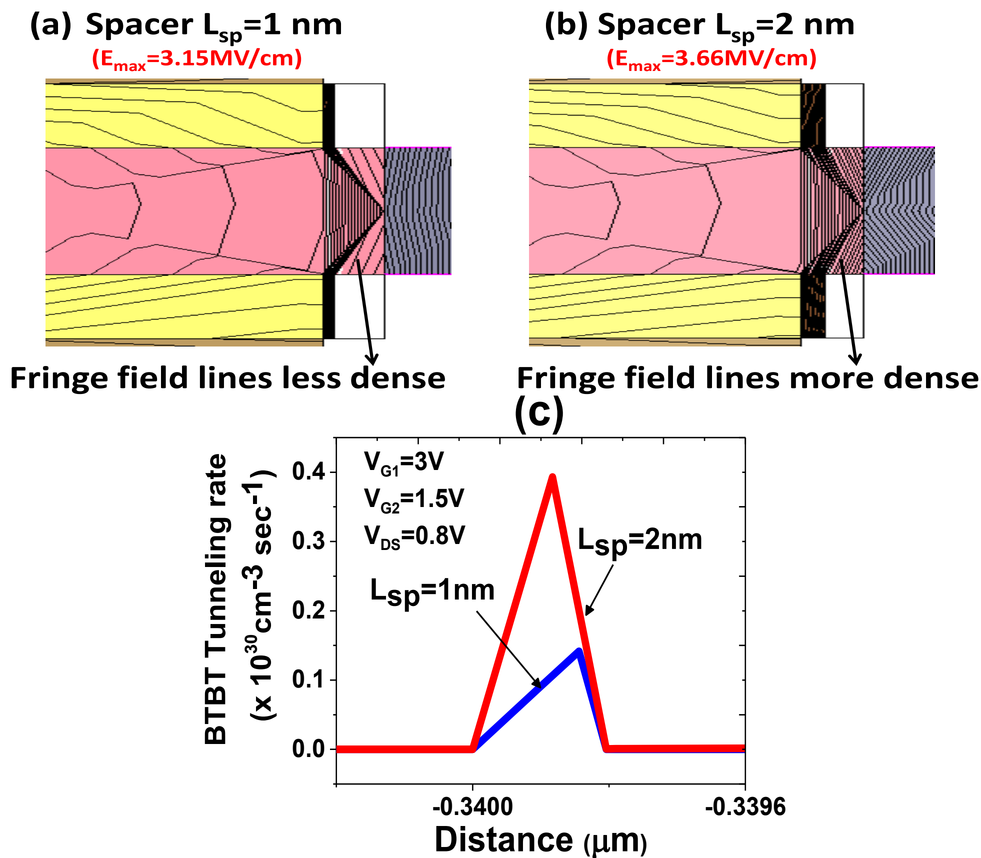


Figure. 3.10. Fringe field coupling through the spacer for (a) L_{sp}=1nm (b) L_{sp}=2nm (c) BTBT rate comparison for L_{sp}=1nm and 2nm.

improved electrostatic coupling near the Schottky junction at higher spacer lengths. As a result of increase in electric flux concentration, electrons entering the channel from source

end, experience higher field strength which enhances their velocity. Similar observations can also be seen when spacer width is changed from 7nm to 10nm, though the improvement obtained in peak velocity is only ~13.04%. This shows that coupling does not increase significantly with increase in spacer width because of the physical distance and lesser impact of t_{sp} on outer fringe lines. Finally, ~72% increase in V_{max} with the inclusion of high-κ (HfO_2) spacer relates to a huge rise in concentration of the fringing electric field near the $NiSi_2$/Si Schottky contact.

3.4.2 Optimization of Gate Dielectric Constant

We now show the comparison of device performance for various gate dielectrics in Fig. 3.10 (a), (b), (c), (d) and (e).

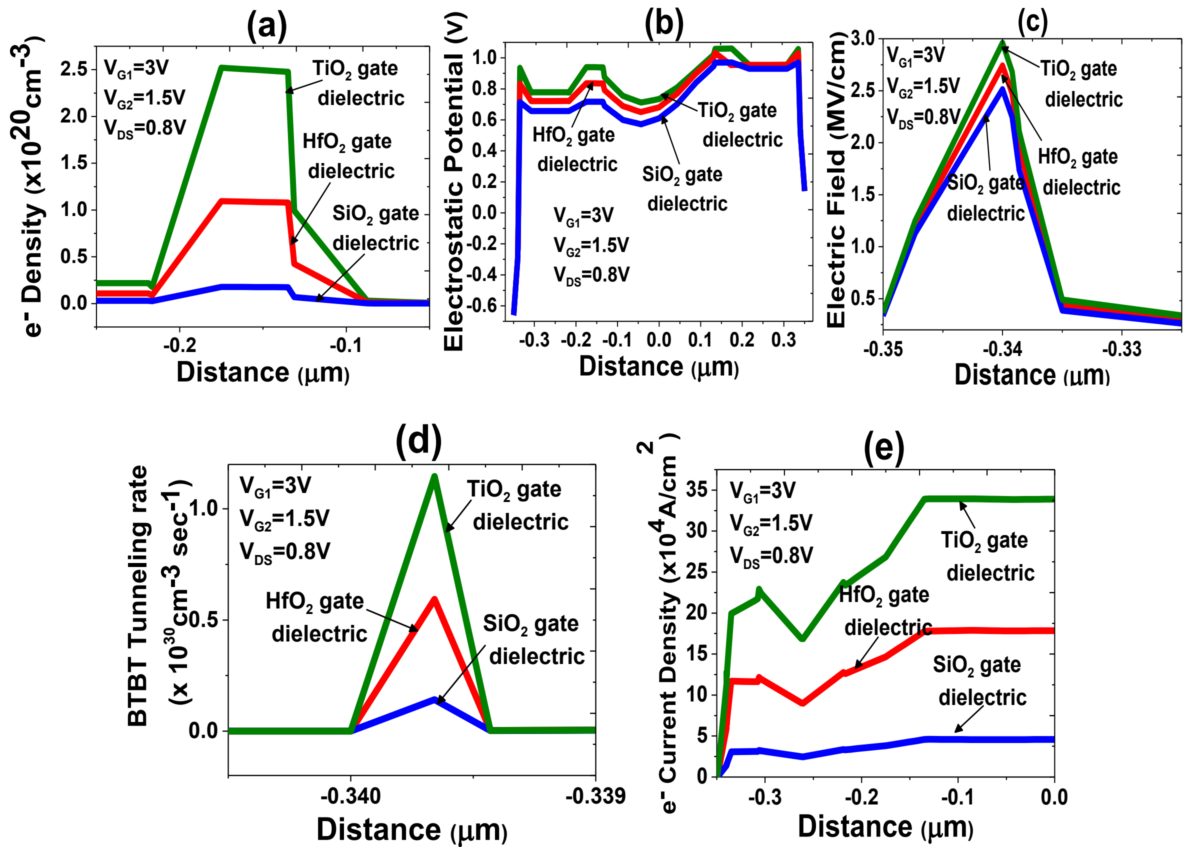


Figure. 3.11. Impact of TiO_2 as gate dielectric as compared to SiO_2 and HfO_2 on (a) electrostatic potential (b) electric field (c) electron density (d) BTBT rate (e) electron current density.

The EOT is kept fixed in each case to 0.67nm and 3 different cases are considered viz. SiO_2

(with κ=3.9) [2, 55] HfO_2 (with κ=25) [46] and TiO_2 [present work] (with κ=60). With TiO_2 gate oxide the peak electron density increases by ~1.5×10^{20} cm^{-3} and ~2.2×10^{20} cm^{-3} at a distance of 0.19 μm from the source electrode [Fig. 3.10 (a)] in comparison to HfO_2 and SiO_2 respectively. This can be explained by the following model. The fringe field lines emanated from the gate and terminating into the Schottky junction through the gate dielectric may be termed as internal and that terminating through the spacer can be termed as external. When there is an enhancement in the internal fringe field due to a higher κ value of gate dielectric (TiO_2) than that of the spacer, the applied gate potential is mainly coupled through the gate oxide, and results in the increase in carrier densities at the designated places [56]. This also increases the number of electrons tunneling from source to channel resulting in higher density of carriers at source side causing an 17.8% rise in electrostatic potential and 15.2% increase in peak electric field (E_{max}) when we switch to TiO_2 from SiO_2 as gate dielectric [Fig. 3.10 (b) and (c)].

The highest gradient of electric field takes place at the Schottky junction. From the analytical expression of tunneling probability through the Schottky barriers at source and drain derived by using the WKB model of a triangular barrier [50], it is found that higher value of electric field across the interface results in an increased tunneling rate near the Schottky junction which is evident from Fig. 3.10 (d). Since, the tunneling current at a constant bias is dependent exponentially on strength of the field [57]; a rise in the electron current density can also be observed in Fig. 3.10 (e).

3.4.3 Optimization of Spacer Dielectric Constant (κ_{sp})

The impact of variation in κ of the spacer material on device performance is now depicted. The various spacer dielectric constants used are 3.9, 6, 25 and 60. It may be noted that the width of the spacer (t_{sp}) is kept unaltered at 10nm in this entire analysis. With an increase in spacer dielectric constant there is an improvement in all the performance metrics of the device [Fig. 3.11 (a)-(e)].

The aforementioned observations can be explained qualitatively by using the energy band diagram in Fig. 3.8 (b) and fringing field of the device near the source edge for various κ_{sp} values as shown in Fig. 3.12. It is evident from Fig. 3.8 (b) that as the spacer κ is increased it results in more upward band bending near the source channel region. It may be noted from

Fig. 3.12 that the fringing field in the source side near the gate electrode is denser for a device having high-κ spacer (κ=60) than that of a low-κ (κ=3.9) one.

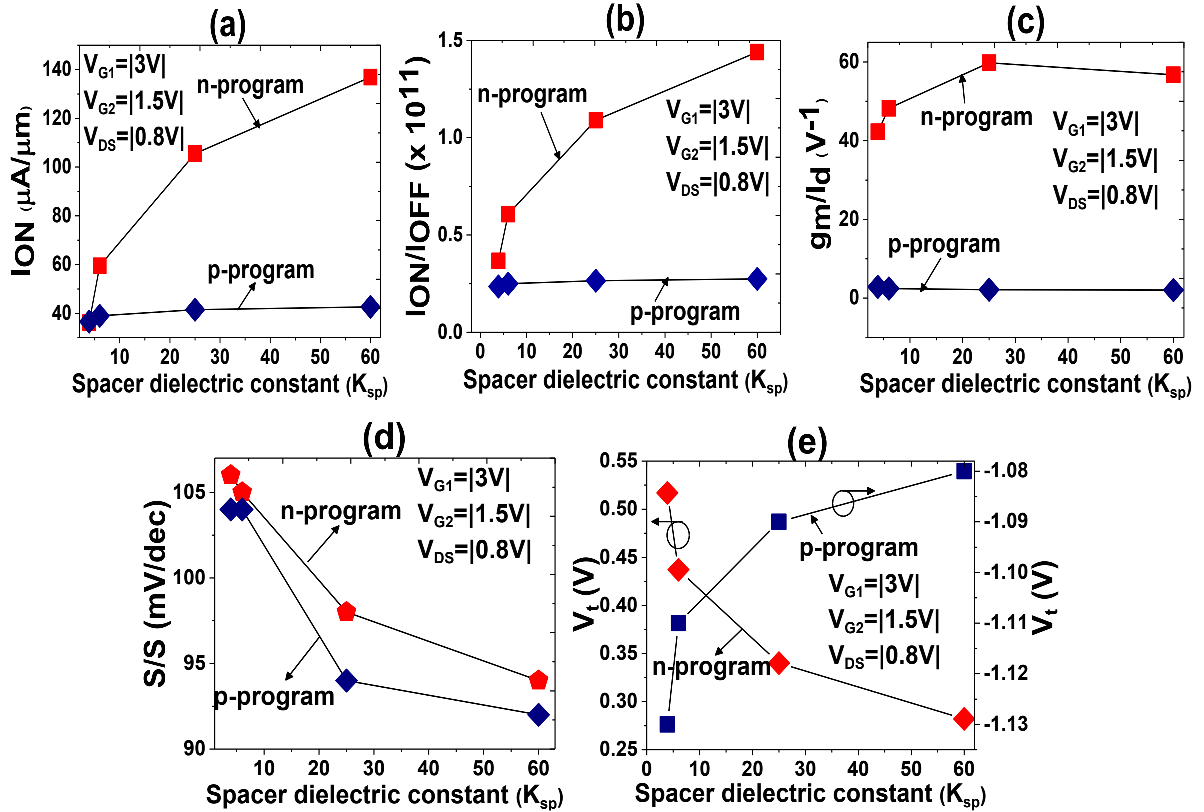


Figure. 3.12. Impact of spacer dielectric constant on (a) normalized I_{ON} (b) I_{ON}/I_{OFF} (c) g_m/I_d (d) S/S (e) V_t for n and p-FET on state.

This confirms the fact that the band bending in Fig. 3.8 (b) is due to fringe field lines which arises out of the spacer. The upward band bending increases the BTBT rate at on-state due to reduction in minimum tunneling width as reported in [2], thereby causing an 100.7 μA/μm (6.05 μA/μm) rise in ON current for n (p-FET) [Fig. 3.11 (a)] which also leads to a significant improvement in on-off current ratio [Fig. 3.11(b)] when κ of the spacer is switched from 3.9 to 60. Though the Transconductance-Generation-Factor (T.G.F) i.e. g_m/I_d shows small variation for both n and p-FET's with an increase in spacer κ value [Fig 3.11 (c)], there is a 45.45% (4.42%) decrease in V_t for n (p-FET) with $κ_{sp}$ increase [Fig 3.11 (e)] which relates to the increase in electric lines of force at the Schottky junctions as compared to the total amount of field lines which results in lowering of the barrier which is also known as Fringe induced barrier lowering (FIBL) [58]. In our calculations, the evaluation of

threshold voltage (V_t) is done through a constant current criterion ($I_d=10^{-7}$ A×W/L).

Since the inverse subthreshold slope (S/S) is directly proportional to V_T [59], we find a sharp decrease in S/S for both programs with reduction in threshold voltage upto κ_{sp} =25 [Fig 3.11 (d)], though after that, there is a slight increase in this parameter which accounts to increase in device parasitic effects. All the observations mentioned here are similar to the findings presented by Virani et. al. [56] for another class of device based on tunneling phenomenon (TFETs).

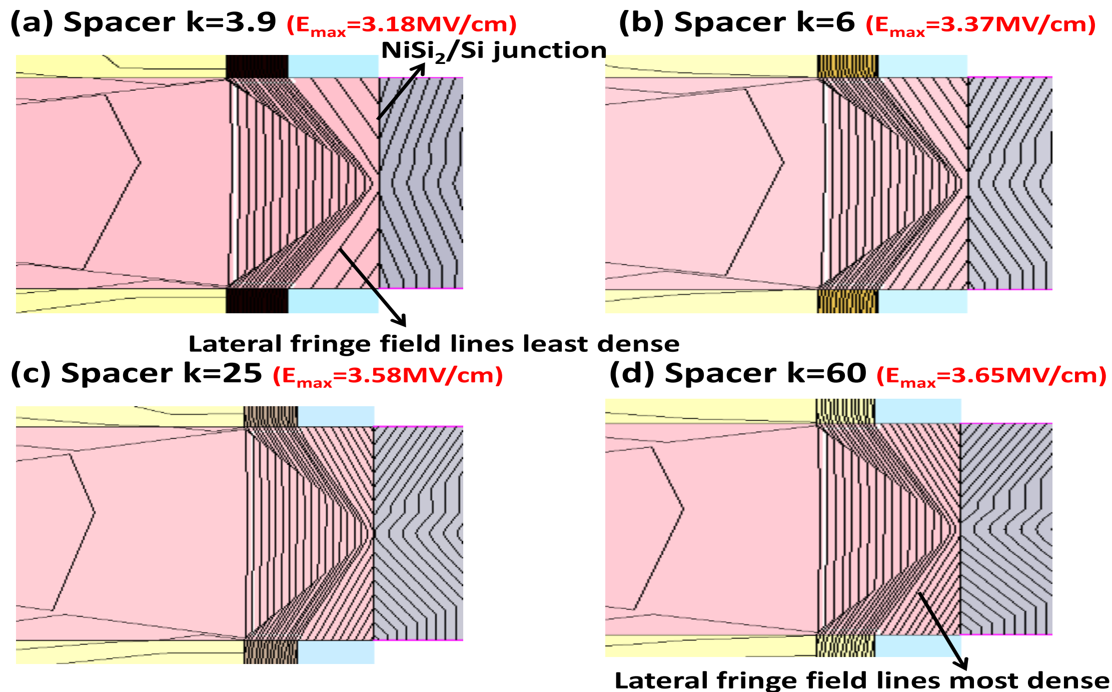


Figure. 3.13. Fringe field coupling through the spacer at source end for the four cases shown in Fig. 6 with varying spacer dielectric constant.

3.4.4 Optimization of Gate Dielectric Thickness (t_{ins})

Fig. 3.13 (a)-(c) show a series of simulation results depicting the impact of variation in gate dielectric thickness (t_{ins}~7nm-10nm) on device performance (it is useful to mention that in all the cases the spacer thickness is also scaled in contrast to the thickness of gate oxide). The improvement in on/off current ratio with t_{ins} increase [Fig. 3.13 (a)] mainly attributes to reduction of direct tunneling current through the gate oxide and a lower Schottky junction resistance at higher t_{ins} causing an enhancement in gate dielectric properties [2] and reduction

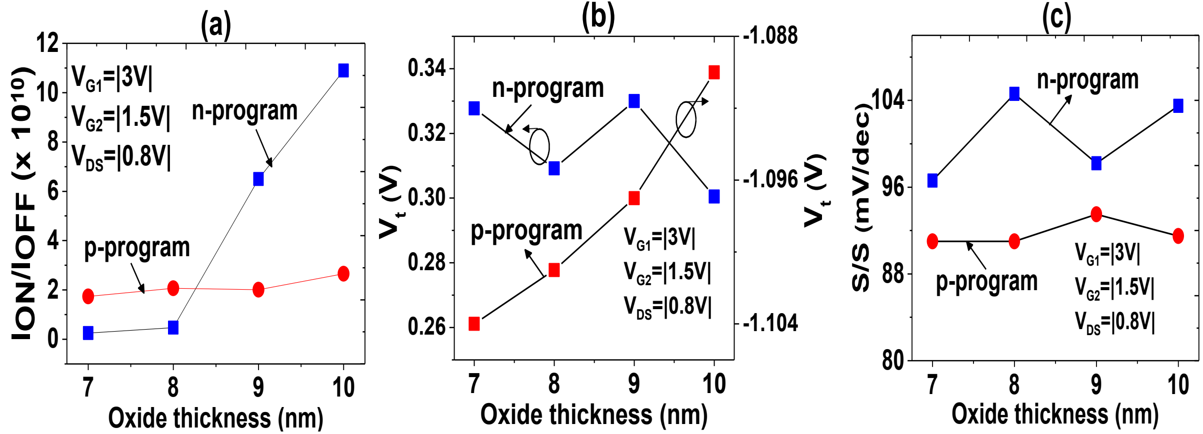


Figure. 3.14. Impact of t_{ins} scaling on (a) I_{ON}/I_{OFF} (b) V_t (c) S/S for n and p-program on state.

in off-state leakage, thereby resulting in an overall modulation increase. The reduction in V_t for n-FET [Fig. 3.13 (b)] is due to increase in gate control over channel potential at higher gate oxide thickness. It is interesting to note that performance gains obtained with a thicker gate oxide does not cause a significant deterioration in S/S for both n (p-FET) which is evident from Fig. 3.13 (c). The performance comparison of the proposed spacer based RFET with various reconfigurable topologies is shown in Table 3.5. It can be seen that apart from having a very low off state leakage current, the proposed device shows enhancements in performance in terms of ON current and S/S at a scaled supply voltage as compared to its counterparts.

3.4.5 Inter gate Distance (d_{G1G2}) Scaling Performance

The simulations are performed at various separations between control gate (G_1) and polarity gate (G_2) [4nm, 30nm, 150nm, 180nm, 230nm and 270nm (which is used in the current work)]. With HfO_2 spacer there is a significant increase in normalized I_{ON} from 105.35 µA/µm (41.45 µA /µm) to 202.3 µA/µm (620 µA/µm) for n (p-FET) with d_{G1G2} scaled down from 270nm to 4nm which is mainly due to decrease in parasitic resistance at smaller inter gate separation. This effect is less predominant in SiO_2 spacer case because of its lower κ value which is evident from a relatively lesser increase in on-current for n (p-FET)] [Fig 3.14 (a) and (b)]. Same reasons hold true for a slight increase in S/S for p-program for both kind of spacers at higher d_{G1G2} [Fig 3.14 (c) and (d)]. In case of n-program the S/S is found to

Table 3.5 Performance comparison of various RFETs proposed in literature with our proposed device

Parameters \ Device	DGRFET [2]		Ambipolar FET [61]		TIG SiNWFET [55]		Proposed	
	n-FET	p-FET	n-FET	p-FET	n-FET	p-FET	n-FET	p-FET
I_{ON} (× 10^{-6} A)	0.11	1.9	0.3	0.3	0.310	0.177	2.11	0.829
I_{OFF} (×10^{-16} A)	40	40	100	100	10000 (HV_T)	3150 (HV_T)	0.192	0.312
I_{ON}/I_{OFF}	10^9	6×10^7	$>3\times10^7$	$>3\times10^7$	3×10^5	6×10^5	1.09×1	0.265×10^{11}
S/S (mV/dec)	220	90	240	230	217 (LV_T)	155 (LV_T)	98	94
V_{DD} (V)	1		2		2		0.8	

* HV_T and LV_T correspond to low V_T and high V_T configurations of dual V_T implementation [55].
** The average current between the gate voltages, at which I_D begins to increase, is used to calculate S/S.

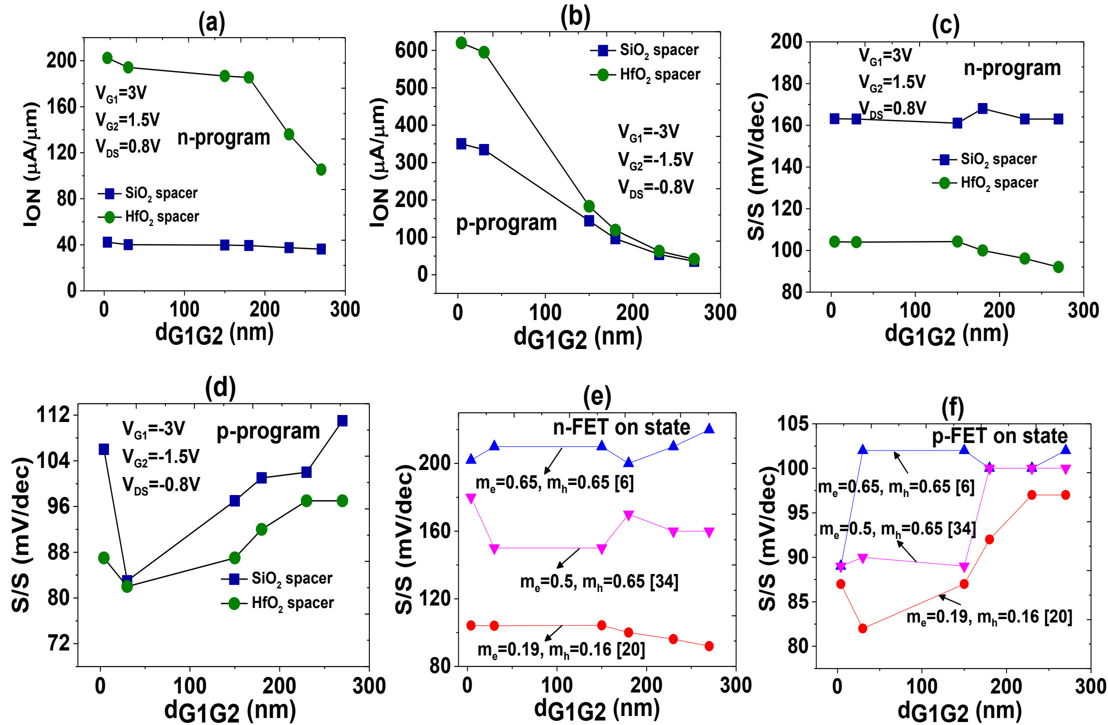


Figure. 3.15. Impact of d_{G1G2} scaling on (a) I_{ON} for n-FET (b) I_{ON} for n-FET (c) S/S for n-FET (d) S/S for p-FET for SiO_2 (blue lines) and HfO_2 (green lines) spacer material. (e) S/S vs d_{G1G2} with varying m_n, m_p [56, 47, 69] for n-FET (f) S/S vs d_{G1G2} with varying m_n, m_p for p-FET. Note the biasing arrangements in all the cases are for on-state of the respective program.

be almost independent of variation in d_{G1G2} which is mainly because of the higher effective tunneling mass of electrons than that of holes. The variation in S/S with d_{G1G2} is also shown

for various values of tunneling masses reported in literature [Fig. 3.14 (e) and (f)]. It is interesting to note that with increase in electron tunneling mass, S/S is found to degrade significantly for both n and p-FET devices which account to reduced BTBT probability near the tunneling junction at on state for higher tunneling mass values. It can be seen from Fig. 3.15 (a) and (b) that the performance gains achieved at lower d_{G1G2} is offset by higher capacitive coupling due to 92.8 aF and 89.6 aF rise in the total inter gate capacitance (C_{G1G2}) for HfO_2 and SiO_2 spacers for n-FET and 614 aF and 623.6 aF for p-FET which will in turn degrade the circuit performance.

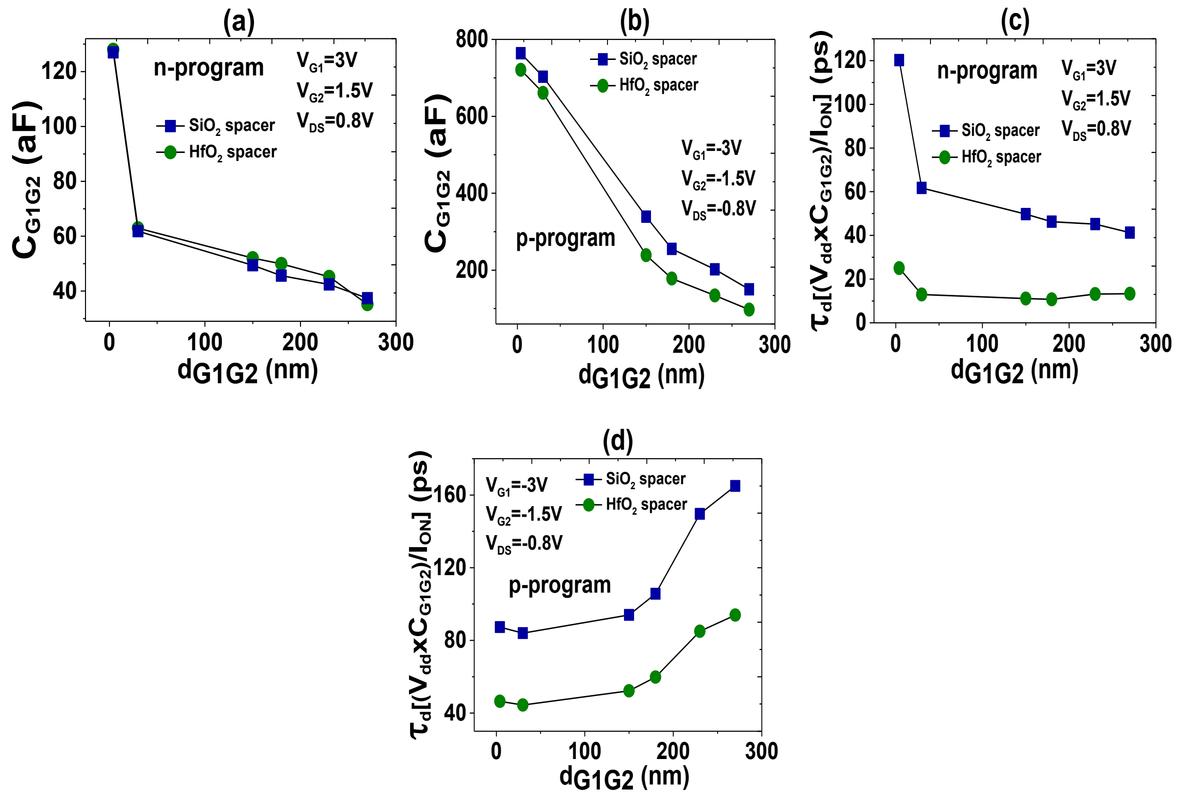


Figure. 3.16. Impact of d_{G1G2} scaling on (a) I_{ON} for n-FET (b) I_{ON} for n-FET (c) S/S for n-FET (d) S/S for p-FET for SiO_2 (blue lines) and HfO_2 (green lines) spacer material. Note the biasing arrangements in all the cases are for on-state of the respective program.

The average propagation delay τ_d ($C_{G1G2}\times V_{dd}/I_{ON}$) which is an known measure of suitability of a device for high speed logic applications [59] is estimated following the $V_{DD}\times C_{G1G2}/I_{ON}$ metric, where C_{G1G2} is the inter gate coupling capacitance. It is found to degrade by 11.7 ps and 78.9 ps with scaling inter gate distance in case of n-FET for both

SiO_2 and HfO_2 spacers. But in case of p-FET the effect of rise in coupling capacitance is actually offset by substantial increase in drive current for which the delay (τ_d) is found to increase by 47.4 ps and 77.7 ps for SiO_2 and HfO_2 spacers at higher d_{G1G2} [Fig. 3.15 (c) and (d)].

3.5 Summary

In summary, it can be stated that a novel RFET device concept is elucidated for improving the performance of a dual gate ambipolar FET using high-κ S/D spacers. The proposed device is benchmarked with the existing reconfigurable device architectures which shows that the proposed device have enhanced electrical characteristics like higher I_{ON}/I_{OFF} and lower S/S along with significant reduction in subthreshold leakage current, which makes it highly suitable for low power digital applications. A detailed investigation of the impact of variation in critical design parameters like spacer length (L_{sp}) and spacer material type, gate dielectric and its thickness (t_{ins}) and inter gate distance on the performance of the proposed device is also carried out. It is observed that the concentration of lateral fringe lines arising from outer edge of the gate increases at higher L_{sp} values which lead into a shift in the conduction band edge thus resulting in higher on current. It is also observed that increasing the dielectric constant of the gate oxide may result in further improvement in device performance by increasing the BTBT rate and carrier densities at on state due to an enhancement in internal fringing field. In addition the qualitative nature of fringing field is found to be strongly dependent on the spacer dielectric constant. The fringing field of the device near the source tunneling junction becomes denser at higher κ_{sp} values causing a reduction in minimum tunneling width due to upward band bending. This eventually leads to higher carrier tunneling rate causing an improvement in S/S and I_{ON}. Scaling the thickness of gate dielectric is actually found to deteriorate the device performance because of higher gate oxide tunneling current and Schottky junction resistance at lower t_{ins}. Finally, it is also observed that although inter gate distance (d_{G1G2}) scaling may result in a boosted I_{ON} and lower S/S due to an increase in the parasitic effects of the device, still we anticipate degradation in terms of circuit performance due to an increase in inter gate coupling capacitance causing a rise in intrinsic delay (τ_d).

Chapter 4

Impact of Gate/Spacer Channel Underlap, Gate Oxide EOT and Scaling on the Device performance of DG-RFET

4.1 Introduction

We have introduced, spacer induced enhancement in device performance (in terms of I_{ON}, I_{ON}/I_{OFF} ratio and S/S) using a novel *underlap* RFET device architecture and optimization of various important device parameters for best performance. But since the device is relatively new in terms of development and maturity, the overall physics of the device and several physical mechanisms regarding its operation are not yet clearly understood. To make the proposed spacer based reconfigurable FET a robust device and achieve the best possible performance, more research needs to be performed to fully understand the underlying physical principles to clearly know how the source/drain spacers prove to be highly useful in amplifying the performance parameters and their close connection with the metal/silicide Schottky contacts. Some of the important issues which need physical insight not only for a better understanding of the operation of the device but also for its future analytical modeling include the impact of variation in the underlap region between gate, spacer and silicon channel, influence of high-κ gate dielectric and its scaling properties. Keeping these above mentioned goals in mind, a rigorous investigation of the role of EOT of the gate oxide on the device performance of the proposed DG-RFET is carried out. In this chapter the impact of variation in the gate/spacer-channel underlap and scaling on the device properties are also studied. Moreover, it is also depicted that we can achieve the same performance gains using a single supply voltage for control gate, polarity gate and drain, thus providing a simpler operation, other than using multiple supply voltages unlike as in [2, 47, 50]. To make a better connection to the state of the art CMOS technology, a scaled down device architecture is considered by us for the entire analysis. Device dimensions as shown in Fig. 4.1 (a) are used in our simulations.

The chapter comprises of six sections including the current introductory section. A brief description of device structure and optimization of high-κ spacer length is provided in section

4.2. The impact of variation in gate channel underlap region for fixed and varying spacer channel underlap is investigated in section 4.3. Section 4.4 analyzes the effects of variation in gate oxide EOT on the performance of the proposed RFET. Both the cases of fixed and varying EOT are considered by us. Since scaling properties of such a device is not yet investigated in any of the literature, section 4.5 focuses on the impact of scaling nanowire length, gate length, nanowire diameter, L_{GCU} and L_{SCU} on the performance of the device under consideration. Conclusions are drawn based on the results obtained in section 4.6.

4.2 Underlap RFET Device and High-κ Spacer Optimization

The considered underlap device architecture is shown in Fig. 4.1.

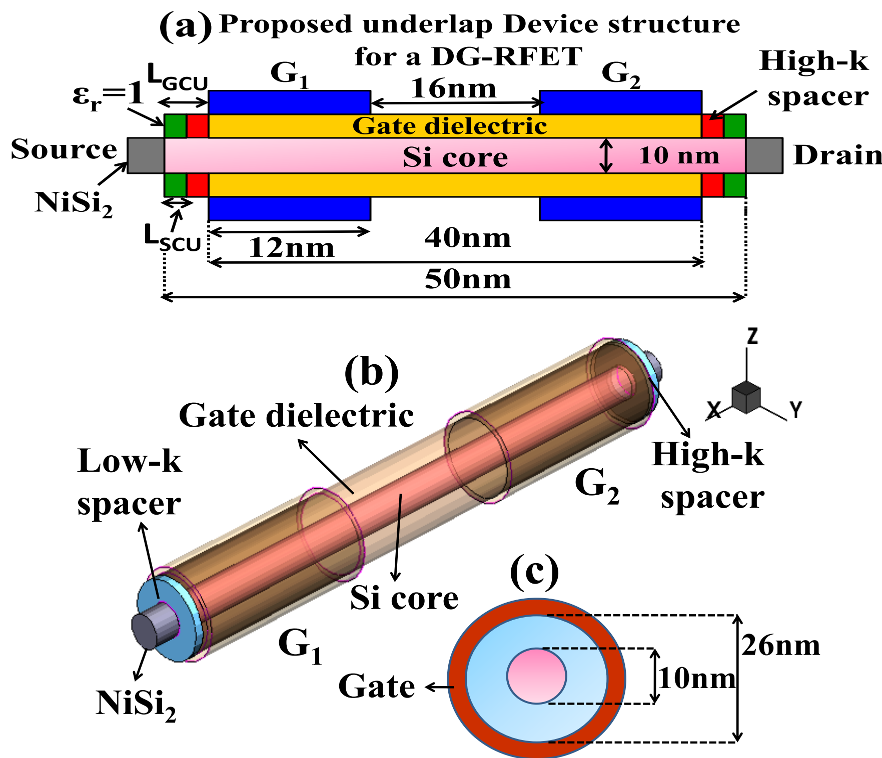


Figure. 4.1. Schematic representation (b) 3-D isometric view (c) Cross-sectional view of the target RFET.

As mentioned in the previous chapter also, to optimize the high-κ spacer length we have performed a series of TCAD simulations for various spacer lengths (3nm, 3.5nm, 4nm, 4.2nm and 4.5nm) of the device under study as shown in Fig. 4.2 (c) taking I_{ON}/I_{OFF} ratio as

the performance metric for evaluation.

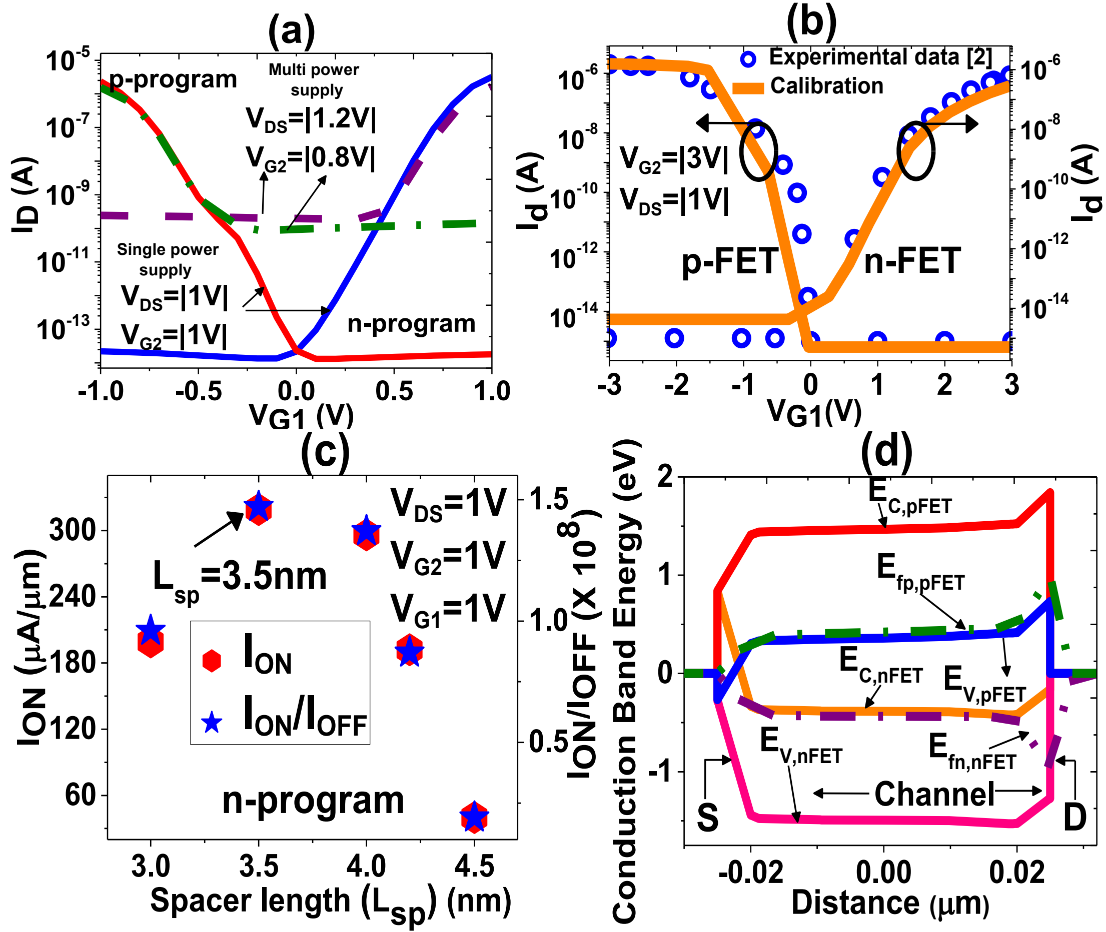


Figure. 4.2. (a) Transfer characteristics comparison for single and multi stage power supply for both n and p-programs (b) Calibration of BTBT model against experimental data [2] (c) Optimization of high-κ spacer length (d) Simulated energy band diagrams for n- and p-program on-state of the proposed RFET.

It can be seen from the figure that though increasing the length of high-κ spacer results in an improvement in drive current I_{ON}, but after reaching a certain L_{sp} (in this case 3.5nm), there is degradation in I_{ON}/I_{OFF} ratio. Initially, when the length of high-κ spacer is increased, from 3nm to 3.5nm there is an increase in the drive current I_{ON}. This is because of an up-shift in band edge with increase in spacer length. As the spacer length is more increased there is an enhancement of lateral electric field at the Schottky junction due to an increased coupling between source and gate metal through spacer. The shift in energy band in turn reduces the minimum tunneling width which allows more electrons to tunnel from source to drain. On

the other hand, after reaching an L_{sp} of 3.5nm, the off state leakage current increases gradually which results in degradation in the I_{ON}/I_{OFF} ratio. A possible explanation to this observation includes parasitic tunneling which implies tunneling of carriers in the reverse direction than that of the normal tunneling path which is from source electrode (tunneling source) to drain electrode (tunneling destination) of the device because of reduced *gate-channel underlap* (L_{GCU}) [please refer to Fig. 4.1 (a)] length. We want to again highlight this point that this trend is slightly dissimilar from any other single gated device dependent on BTBT for on-current generation such as TFET which is primarily because of different geometrical architecture, charge transport behavior and device physics of the proposed ambipolar FET. As mentioned earlier, a low-κ material (ε_r=1) is used in the *spacer-channel underlap* region (L_{SCU}) (the region between the high-κ spacer and $NiSi_2$/Si Schottky junction) [Fig. 4.1(a)] to correctly model the impact of air spacer in TCAD simulations. Results related to only the n-RFET are shown for simplicity. Similar results are also expected for the p-program with alternate biasing arrangements.

4.3 Impact of Variation of the Gate-Channel Underlap (L_{GCU})

4.3.1 Varying Spacer Channel Underlap (L_{SCU})

We investigate the impact of variation in the length of gate-channel underlap region (L_{GCU}) on the performance of the device for varying spacer-channel underlap (L_{SCU}) [please refer to Fig. 4.1 (a) for exact locations of the two regions]. It may be noted that for varying the spacer-channel underlap the outer edge of both control and polarity gates (along with the gate dielectric) is shifted towards the device centre by keeping the high-κ spacer length (3.5nm) and gate length (12nm) unaltered (in the process the gate-channel underlap length also gets modulated). We have used four different values of the spacer-channel underlap, 1.5nm (i.e., 3.5nm length of the high-κ spacer and 5nm gate-channel underlap), 4.5nm (L_{GCU}=8nm), 6.5nm (L_{GCU}=10nm) and 8.5nm (L_{GCU}=12nm). The transfer characteristics for different values of the spacer-channel underlap devices at V_{DS}=1V are shown in Fig. 4.3 (a).

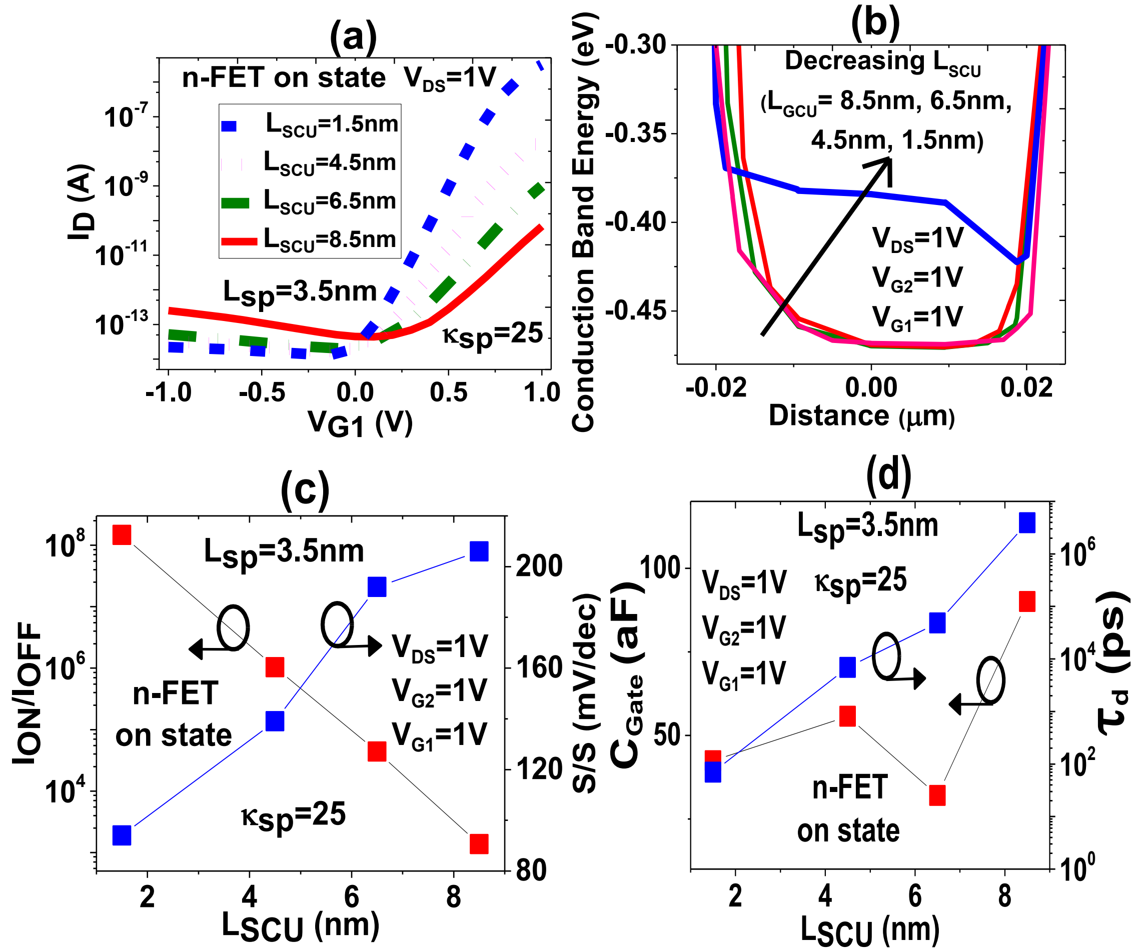


Figure. 4.3. (a) Transfer characteristics (b) Simulated energy band diagrams (c) I_{ON}/I_{OFF} ratio and S/S (d) Total gate capacitance and intrinsic gate delay for n- program on-state of the proposed RFET at V_{G1}=1V, V_{G2}=1V and V_{DS}=1V for varying spacer-channel underlap (L_{SCU}).

It can be observed that the subthreshold characteristics of the device (mainly thermionic emission dependent) as well as the on state current (mainly BTBT dependent) of depend heavily upon the length of the spacer-channel underlap region. From the plot of I_{ON}/I_{OFF} ratio and S/S for different values of spacer-channel underlaps as shown in Fig. 4.3 (c), it is evident that an increase in the spacer-channel underlap results in performance degradation in terms of both S/S and I_{ON}/I_{OFF}.

In order to get an insight, the electric field and BTBT rates contour plots at the source side are shown in Fig. 4.4 for 1.5nm and 8.5nm spacer-channel underlap devices at V_{G1}=1V,

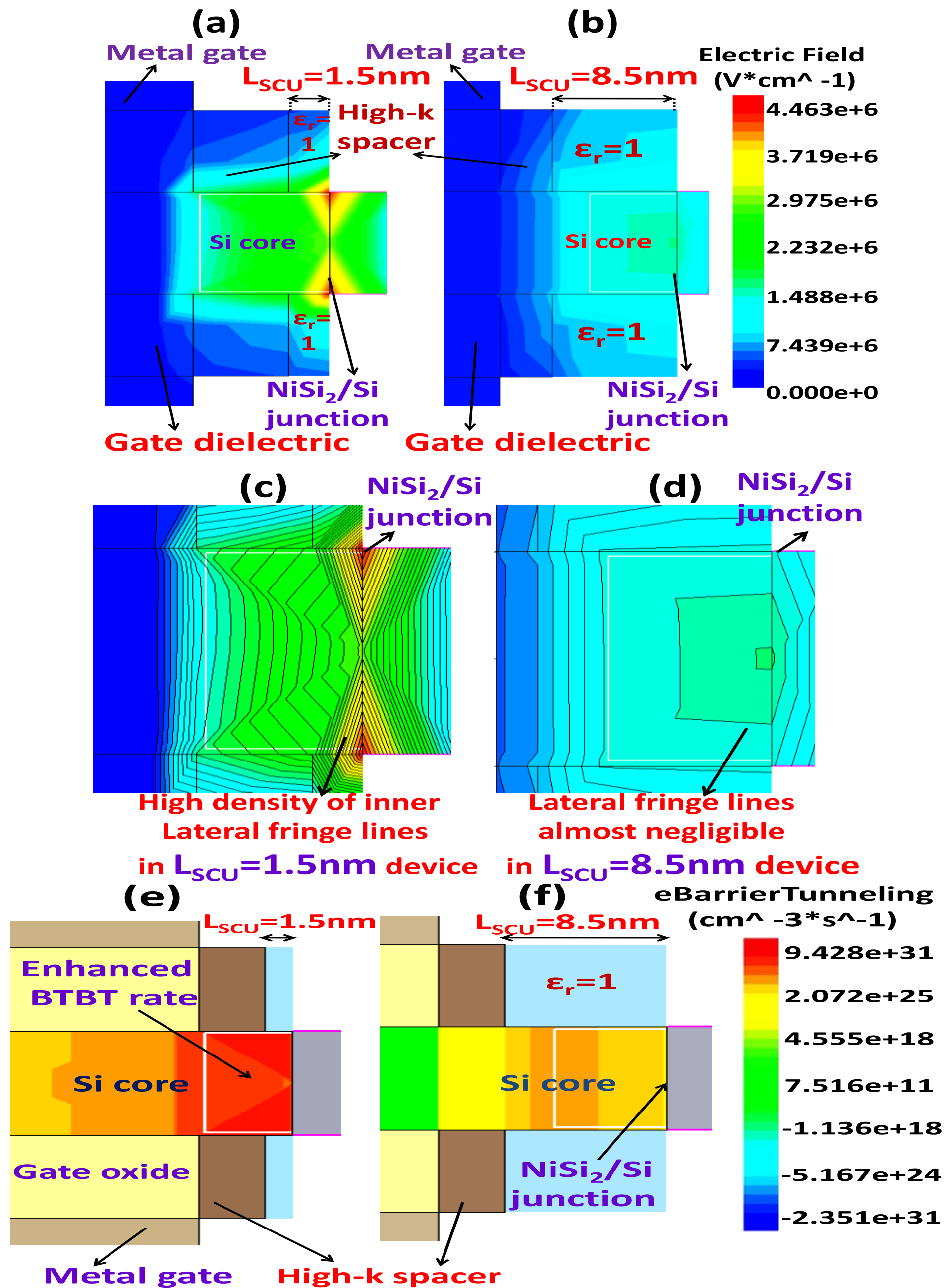


Figure. 4.4. (a) Electric field contour for L_{SCU}=1.5nm (b) Electric field contour for L_{SCU}=8.5nm (c) Magnified electric field plot showing the lateral fringe field coupling through the spacer for L_{SCU}=1.5nm (d)) Magnified electric field plot showing the lateral fringe field coupling through the spacer for L_{SCU}=8.5nm (e) BTBT contour for L_{SCU}=1.5nm (f) BTBT contour for L_{SCU}=8.5nm at source end for n-program on-state of the proposed RFET at V_{G1}=1V, V_{G2}=1V and V_{DS}=1V for varying spacer-channel underlap (L_{SCU}).

V_{G2}=1V and V_{DS}=1V. It can be seen that spacer-channel underlap has a significant impact on the electric field as well as BTBT rates near the source side Schottky tunneling junction.

Along with 1.32 MV/cm enhancement in peak electric field near the junction [Fig. 4.4 (a), (b)], a notable BTBT happens at the $NiSi_2$/Si Schottky interface for 1.5nm underlap device (~$9.5\times10^{31}$$cm^{-3}$/sec), although it decreases manifold for the 8.5nm underlap device ($2.2\times10^{25}$$cm^{-3}$/sec) [Fig. 4.4 (e), (f)]. It is also seen from the fringe field contour comparison plots that between the two devices as shown in Fig. 4.4 (c), (d) that the density of lateral fringe lines at the tunneling source periphery is significantly higher for lower gate-channel underlap device and becomes almost negligible for the higher one. This is mainly related to the fact that when the high-κ spacer as well as outer gate edge is shifted away from metal-semiconductor interface for 8.5nm underlap device, there is a reduction in the electrostatic coupling between the gate, high-κ spacer and the tunneling junction, because of which less number of electric lines of force get linked with the metal silicide Schottky junction, which eventually reduces the peak electric field strength near the interface. This ultimately causes a noteworthy deterioration in the ON current for higher underlap devices causing the on-off current ratio to fall drastically thus affecting the average subthreshold swing [Fig. 4.3(c)]. To further verify this fact, we have also shown in Fig. 4.3 (b), the simulated energy band diagrams in the lateral direction at V_{G1}=1V, V_{G2}=1V and V_{DS}=1V for the 1.5nm, 4.5, 6.5nm and 8.5nm underlap devices. Due to the increasing fringing field arising out of a high-κ spacer, the bands are pushed up in energy (~0.053 eV, going from 8.5nm to 1.5nm underlap device), causing a reduction in the tunneling width for a device with a lower spacer-channel underlap, compared to that having a higher one. As a result degradation in device performance is observed in Fig. 4.3 (a), (c) when L_{SCU} is increased from 1.5nm to 8.5nm. The rise in S/S with an increase in underlap length in this case is again slightly different from that of a single gated device and is mainly because of the fact that as the length of spacer-channel underlap (L_{SCU}) is increased [Fig. 4.3 (c)] the high-κ spacers are actually shifted away from the $NiSi_2$/Si Schottky contact although their length is kept unchanged. As such, there is a reduction in the electrostatic coupling between the gate, high-κ spacer and the tunneling junction, as a result of which lower number of electric lines of force get linked with the metal silicide Schottky junction, which ultimately reduces the peak electric field strength near the junction and eventually causes the average subthreshold swing (S/S) to increase. The

retarded on-current performance is also reflected in orders of magnitude rise in intrinsic delay τ_d for 8.5nm underlap device as compared to the 1.5nm one [Fig. 4.3 (d)]. We would like to mention that τ_d is calculated by following the $C_{GG}V_{DD}/I_{EFF}$ method, where I_{EFF} is calculated from the relation $R_{SW}=V_{DD}/2I_{EFF}$. To calculate switching resistance R_{SW}, device level mixed mode simulations have been performed using *Sentaurus TCAD* tool to obtain the transient responses with a peak-to-peak voltage of 1 V and a rise time (t_r) of 50 ps, fall time (t_f) of 50 ps, delay (t_d) of 10 ps, on time (t_{on}) of 1000 ps and a load capacitance of 10 aF. Then R_{SW} is calculated from the slope of the fall delay versus load capacitance (C_L) plot in the same way as mentioned in [68].

4.3.2 Fixed Spacer Channel Underlap (L_{SCU})

In order to study the impact of varying gate-channel underlap (L_{GCU}) on the device performance by keeping the spacer-channel underlap (L_{SCU}) constant, we have carried out device simulations for four RFET structures with gate-channel underlap of 5nm, 7nm, 9nm and 10nm respectively [with L_{SCU} fixed at 1.5nm in all the cases]. This is done to see the impact of relative separation between the outer gate edge and the Schottky junction on the electrostatic integrity of the device and its performance. Unlike as done in the previous section, here we have only shifted the control and polarity gate outer edges towards the center of the device and kept the relative positions of the high-κ spacer and gate dielectric unchanged. All other device dimensions and parameters including gate length (L_g) are kept same as shown in Fig. 4.1(a). It can be seen from Fig. 4.5 (a) that as the gate-channel underlap length is decreased from 10nm to 5nm there is an improvement of the device performance with increase in normalized I_{ON} and reduction in V_t [extracted using the constant current (10^{-7}A × W/L) method]. To get an insight into the aforementioned observations, the simulated energy band diagrams in the lateral direction for different values of L_{GCU} are shown in Fig. 4.5 (b) at V_{DS}=1V. It is seen that a gradual decrease in the underlap length from 10nm to 5nm results in upward silicon band movement, thereby causing a reduction in the minimum tunnel width which can be verified from the simulated BTBT plot as a function of L_{GCU} as shown in Fig. 4.5 (c). This condition, in turn causes better transmission of electrons across the thin barriers at on state, resulting a rise in current conduction at lower L_{GCU} as can be verified from Fig. 4.5 (a).

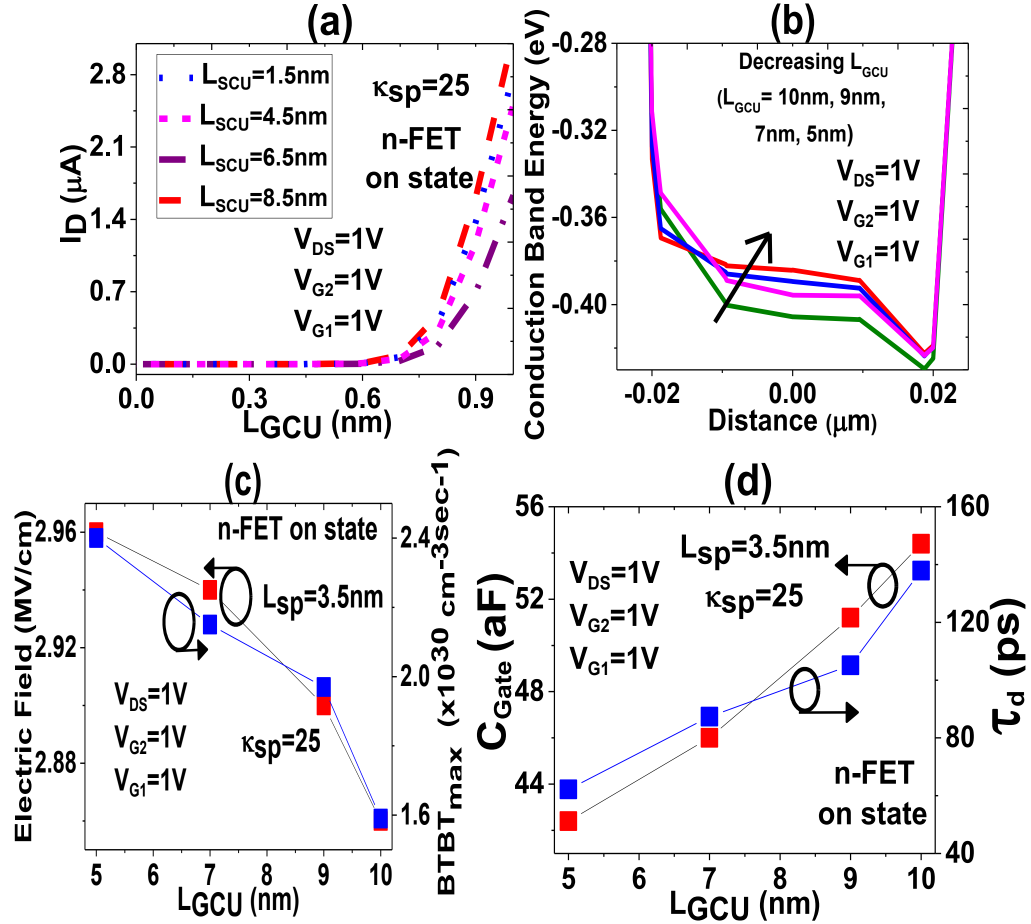


Figure. 4.5. (a) I_{ON} and V_t (b) Simulated energy band diagrams (c) Electric field and BTBT rate (d) Total gate capacitance and intrinsic gate delay for n- program on-state of the proposed RFET at V_{G1}=1V, V_{G2}=1V and V_{DS}=1V for varying gate-channel underlap (L_{GCU}) at fixed spacer-channel underlap (L_{SCU}).

The obtained device performance improvements at lower gate-channel underlap lengths mainly relates to the improved electrostatic coupling between the metal gate and $NiSi_2$/Si junction at lower L_{GCU} values. We believe that as the gates are moved away from the metal-semiconductor interface there is a reduction in the fringe field lines emanating from the outer gate edge and terminating into the Schottky contact through the high-κ spacer which is evident from 0.102 MV/cm reduction in peak electric field at the junction for the 10nm underlap device as compared to the 5nm one [Fig. 4.5 (c)]. It is interesting to note that unlike as in the previous case a drastic deterioration in the current performance of the device is not observed in this case at higher gate-channel underlap lengths, which confirms the fact

that the influence of gate on the density of fringing electric lines of force near the tunneling interface is minimal as compared to that of the high-κ spacer.

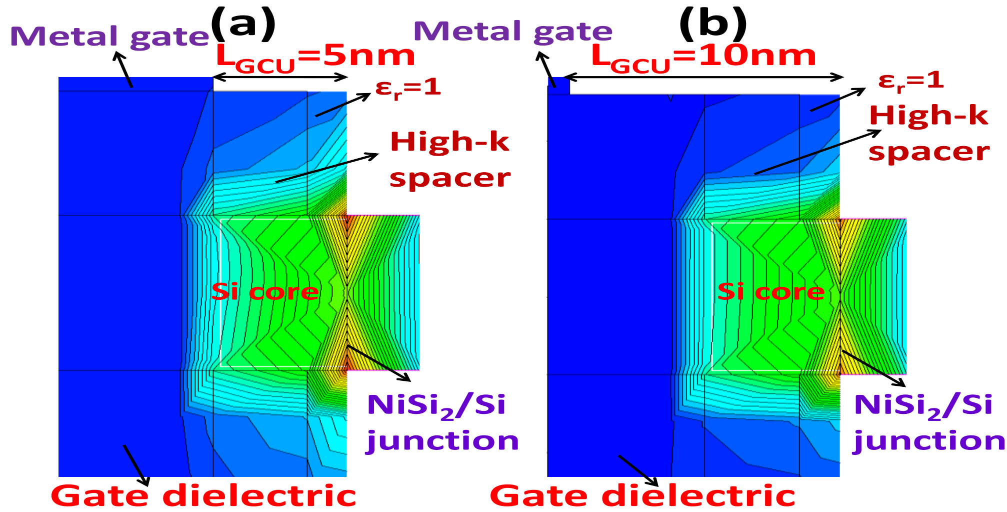


Figure. 4.6. (a) Fringe field contour plot showing the lateral fringe field coupling through the spacer for L_{GCU}=5nm device (b)) Fringe field contour plot showing the lateral fringe field coupling through the spacer for L_{GCU}=5nm device at source end for n-program on-state of the proposed RFET at V_{G1}=1V, V_{G2}=1V and V_{DS}=1V for varying gate-channel underlap (L_{GCU}).

To further validate this assumption the fringe field contours for 5nm and 10nm L_{GCU} devices is shown in Fig. 4.6. It can be seen from the figure that only a slight enhancement in the peak electric field and density of lateral fringe lines is observed in the 5nm underlap device as compared to the 10nm one. It is further observed that there is deterioration in device performance both in terms of total gate capacitance (C_{Gate}) and intrinsic delay (τ_d) for devices having larger gate-channel underlap lengths [Fig. 4.5 (d)]. Whereas, 12 aF increase in C_{Gate} for the 10nm L_{GCU} device as compared to the 5nm one relates to the higher capacitive coupling between the control and polarity gate metal at lower inter gate separation (16nm for the 5nm underlap device and 6nm for the 10nm underlap device), 75 ps rise in τ_d is due to the combined effect of higher gate capacitance and lower ON current at higher values of L_{GCU}.

4.4 Influence of Gate Oxide EOT on the Device performance

4.4.1 Fixed EOT

We now investigate the impact of using various gate dielectric materials with fixed EOT on the performance of the proposed RFET. The device structure in Fig. 1 is simulated for five different κ values of the gate dielectric as 3.9, 8, 12, 25 and 60 for a same EOT of 0.52nm.

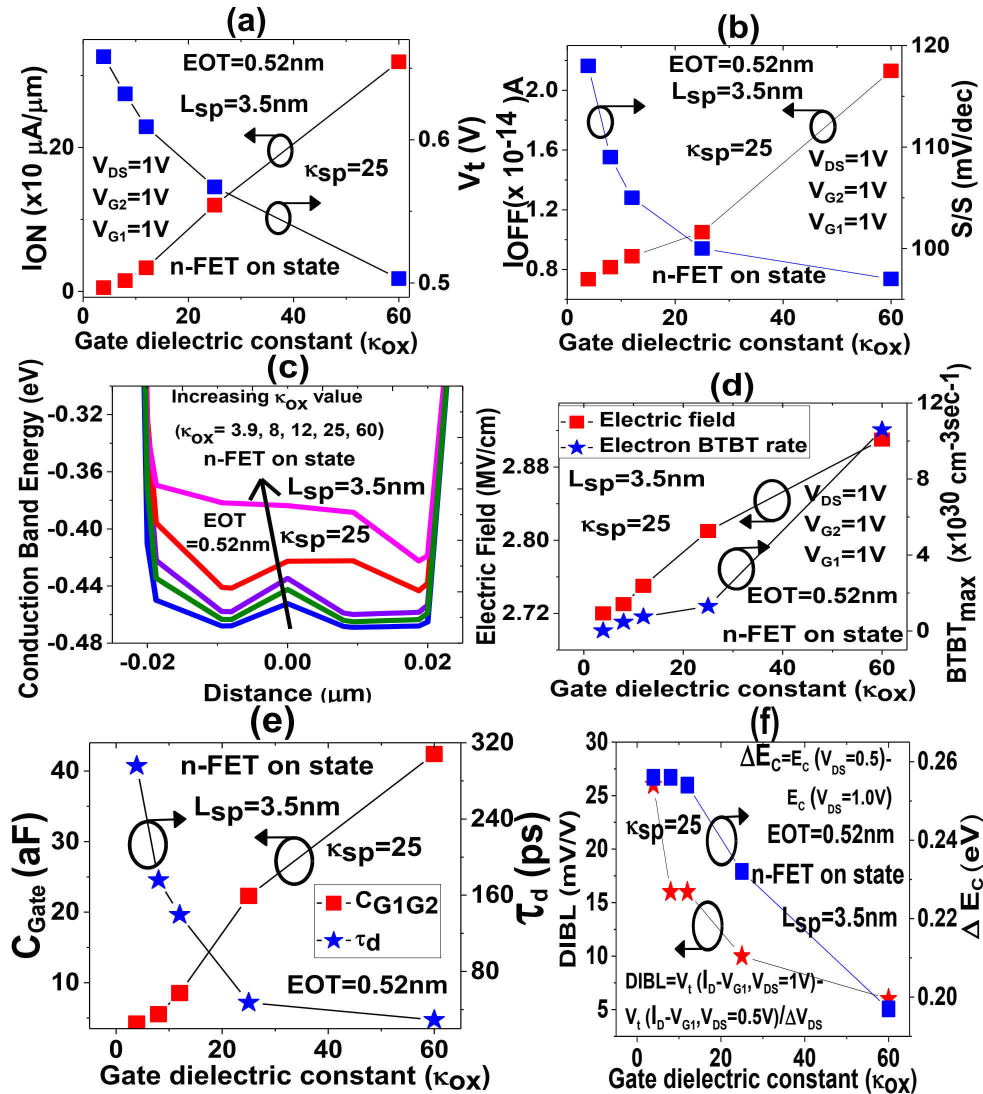


Figure. 4.7. (a) Normalized I_{ON} and V_t (b) I_{OFF} and S/S (c) Simulated energy band diagram (d)Electric field and electron BTBT rate (e)Total gate capacitance and intrinsic gate delay (f) DIBL as a function of of gate dielectric constant (κ_{ox}) gate dielectric constant (κ_{ox}) for varying κ_{ox} and a fixed V_{DS} for n-FET on-state of the proposed device for a fixed EOT of 0.52 nm.

It may be noted that the width of high-κ spacer material is also varied according to that of the gate dielectric to maintain symmetry between gate height, oxide and spacers. All other device dimensions and parameters are kept unaltered as shown in Fig. 4.1. It is seen from Fig. 4.7 (a) that an increase in κ_{ox} value from 3.9 to 60 leads to 313.73 μA/μm rise in normalized I_{ON} and 0.155V reduction in V_t but at the same time I_{OFF} is not significantly affected in this case as can be seen from Fig. 4.7 (b) which is mainly because of the lesser impact of varying physical thickness of the gate oxide on thermionic emission phenomenon controlling the subthreshold characteristics. To get an insight into it, the simulated energy band diagrams biased at V_{DS}=1V, V_{G2}=1V and V_{G1}=1V are shown in Fig. 4.7 (c) for various κ values of the gate dielectric. 17.77% up shift in energy band is observed near the tunnel source region when κ_{ox} is increased from 3.9 to 60. A physical explanation of this observation can be given as follows. With an increase in the dielectric constant of the gate dielectric at fixed EOT, the vertical internal fringing field lines that emanate from the gate and terminate into the Schottky junction through the gate oxide, perpendicular to the silicon channel near the tunneling junction becomes a dominant factor which can be verified from 6.98% rise in peak electric field at the source end of the RFET which in turn starts to influence the channel potential below the gate, causing energy bands of the tunnel source adjacent to the tunneling junction to move upward. As a result there is a reduction in the electron tunneling barrier and a rise in the maximum BTBT rate [Fig. 4.7 (d)] with increasing κ_{ox}, thereby yielding an improvement in device performance as evident in Fig. 4.7 (a). The κ_{ox} dependencies of C_{Gate} and τ_d at fixed EOT are plotted in Fig. 4.7 (e). It can be observed that although low-κ gate dielectric (κ=3.9) exhibits 38.20 aF lower total gate capacitance as compared to the high-κ one (κ=60), because of the lower permittivity of gate oxide, the intrinsic delay (τ_d) is found to reduce by 266 ps due to the rise in on current when κ_{ox} is switched from 3.9 to 60.

It may be noted that unlike other planar devices like MOSFETs and FiNFETs the performance gains achieved with increasing κ_{ox} at a fixed EOT does not affect the subthreshold characteristics like S/S and DIBL in case of a RFET as can be seen from Fig. 4.7 (b) and (f). This can be explained as follows. With an increase in κ_{ox} at a fixed EOT, due to an increase in the physical thickness of the gate oxide a lateral drain field is introduced which degrades characteristics like S/S and DIBL for various planar as well as cylindrical

devices [36] but in case of a RFET the metal silicide Schottky energy barriers on either side of the channel [refer Fig. 4.1 (a)] actually act as an insulating layer and does not allow the lateral drain field to significantly affect the tunneling junction at the source end (tunnel source).

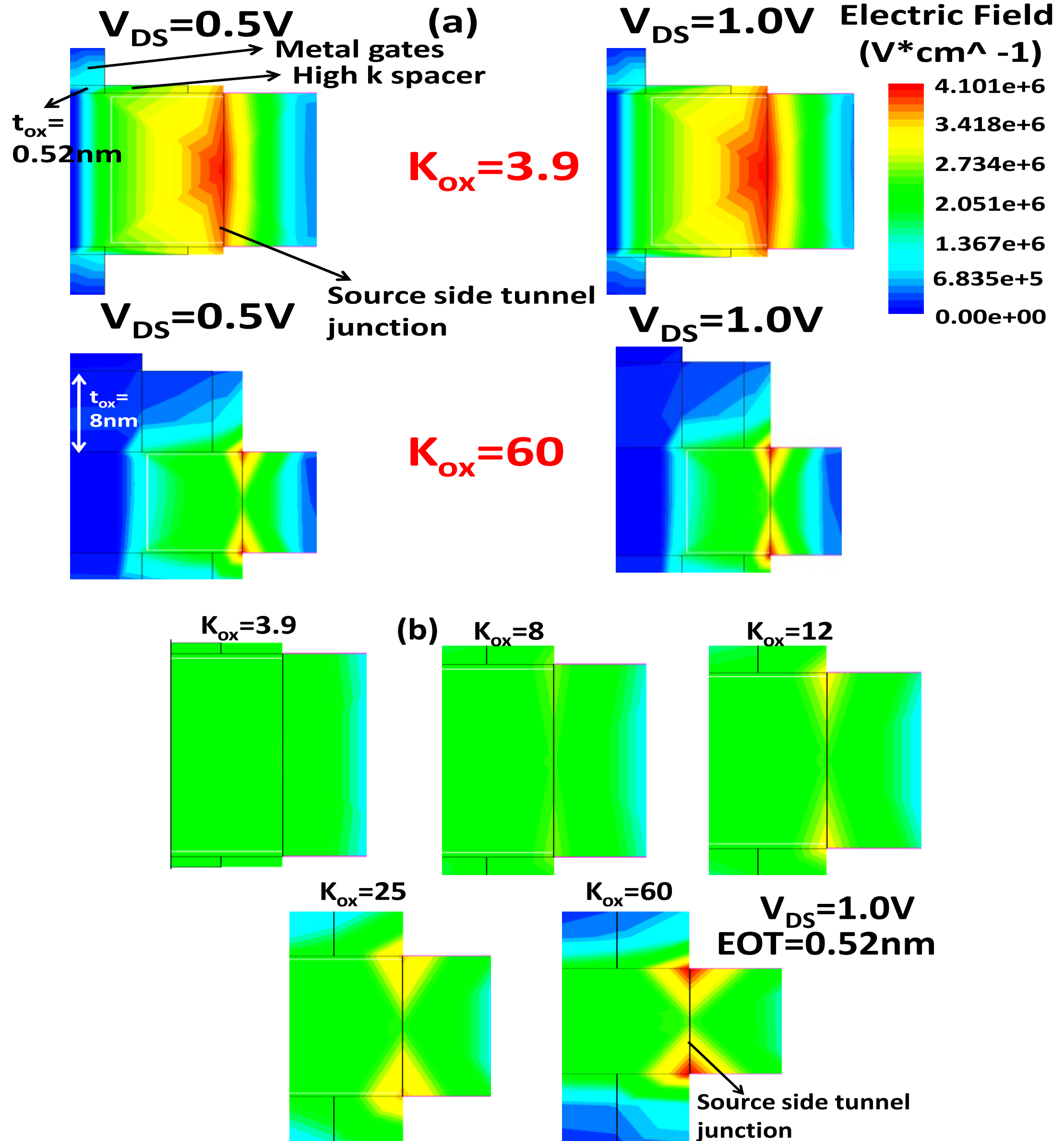


Figure. 4.8. (a) Electric field contours for varying κ_{ox} and a varying V_{DS} (b) Electric field contours for varying κ_{ox} and a fixed V_{DS} for n-FET on-state of the proposed device for a fixed EOT of 0.52nm.

This can be verified from the electric field contours plots shown at the source end for κ_{ox}=3.9 and 60 for V_{DS}=0.5V and 1V respectively [Fig. 4.8 (a)]. Furthermore, it is clearly mentioned in [70] that the effect of lateral drain field which results in a deteriorated short channel behaviour can be ascribed to a 2-D effect related to a stronger capacitive coupling between the drain and the channel region and is only dominant in those Gate All Around (GAA) devices having channel length less than 20nm. Moreover, with an increase in the κ_{ox} value there is a significant increase in the vertical fringing electric field at the source side. This can be verified from the electric flux contour plots (at the source end) at a fixed V_{DS}=1V for varying κ_{ox} values as shown in Fig. 4.8 (b). The increase in electric flux concentration with increasing t_{ins} at fixed V_{DS} causes the bands to move up in energy [Fig. 4.7 (c)], leading to lower tunnel width and higher electron tunneling rate [Fig. 4.7 (d)], and thus results in a better gate control over the channel causing reduced change in V_{GS} for same change in drain current I_d due to which S/S is found to improve by 17.70 % with increasing κ_{ox} from 3.9 to 60 [Fig. 4.7 (b)]. The reason behind the reduction in DIBL from 26mV/V to 6mV/V [Fig. 4.7 (f)] as κ_{ox} is increased from 3.9 to 60 is twofold. Firstly, due to higher electric flux concentration underneath the gate [Fig. 4.7 (d) and Fig. 4.8 (b)] with κ_{ox} increase, the control of gate over the channel as compared to drain becomes better which results in reduced DIBL for higher κ_{ox} values. Secondly, we have also calculated the ΔE_C (difference between the conduction band edge at V_{DS}=1V and V_{DS}=0.5V) near the tunnel source of the device. It has been seen that ΔE_C decreases with increasing κ of the gate dielectric. This is due to the fact that the rate of up shift in the conduction band edge at V_{DS}=1V is higher near the source end with increasing gate oxide κ as compared to V_{DS}=0.5V. This causes in higher reduction in threshold voltage at V_{DS}=1V as compared to V_{DS}=0.5V. In other words the difference in threshold voltages i.e. (V_{th} at V_{DS}=1V-V_{th} at V_{DS}=0.5V) becomes smaller and hence DIBL decreases with increasing κ_{ox}. [Fig. 4.7 (f)].

4.4.2 Varying EOT

To study the impact of using various high-κ gate dielectrics of constant physical thickness (t_{ins}) on the performance of the device under consideration, we have performed device simulations at a fixed t_{ins} of 8nm with varying κ value of the gate dielectric (κ_{ox}). All other device dimensions and parameters (including spacer dielectric constant of 25) are kept

unchanged as shown in Fig. 4.1.

The various values of κ_{ox} used are 3.9, 8, 12, 25 and 60. It is seen from Fig. 4.9 (a) that with increasing κ value of the gate dielectric 3.9 to 60, there is 303.50 μA/μm rise in normalized I_{ON} and 0.202V reduction in V_t.

To explain these observations, we have plotted the simulated energy band diagrams of the device at V_{DS}=1V, V_{G2}=1V and V_{G1}=1V for different gate dielectric constants as shown in Fig. 4.9 (b). It may be seen that the impact of κ_{ox} increase is more dominant at the source side of the device (which is the tunnel source) than the drain end (which is the tunnel destination). This is because of the fact that a higher κ gate oxide will increase the oxide capacitance at same physical thickness, resulting in an enhancement of tunneling probability T(E) as given in [67]. This can be verified from the plot of BTBT rate as a function of κ_{ox} given in Fig. 4.9 (c). Now, due to the presence of high-κ insulator, there is an increase in the concentration of fringe field lines emanating from the outer gate edge and terminating into the Schottky interface through the gate oxide as compared to those terminating through the spacer.

As a direct consequence, almost the entire voltage applied on the gate is coupled through the gate dielectric causing a rise in the surface electric field just underneath the edge of the control gate near the $NiSi_2$/Si junction [Fig. 4.9 (c)]. As a result larger impact of the high-κ dielectric is seen near the source end of the device and there is almost no movement at the drain end [Fig. 4.9 (b)]. The same is also responsible for the improvement of device performance with increasing κ value of spacer [Fig. 4.9 (a)]. We have also examined the total gate capacitance (C_{Gate}) and intrinsic gate delay (τ_d) performance of the device with varying κ_{ox} as shown in Fig. 4.9 (d). C_{Gate} increases by 37.76 aF and the CV/I speed metric improves by 231 ps for κ_{ox}=60 as compared to κ_{ox}=3.9 [Fig. 4.9 (d)] which is expected because of the enhancement in gate dielectric permittivity.

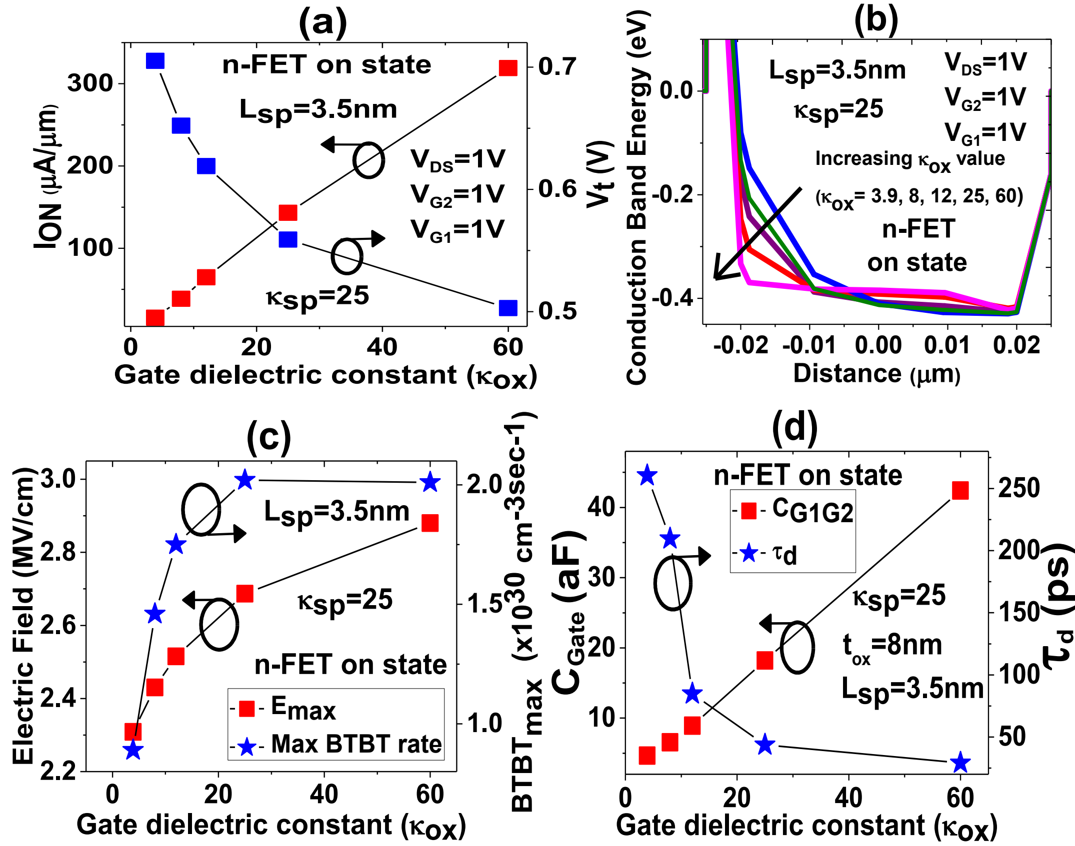


Figure. 4.9. (a) Normalized I_{ON} and V_t (b) Simulated energy band diagrams (c) Electric field and max^m BTBT rate (d) Total gate capacitance and intrinsic gate delay as a function of gate dielectric constant (κ_{ox}) at fixed t_{ins} for n-FET on-state of the proposed device at V_{DS}=1V, V_{G2}=1V and V_{G1}=1V.

4.5 Impact of Scaling Nanowire Length, Gate Length, Nanowire Diameter, L_{GCU} and L_{SCU}

To study the silicon nanowire length (L_{Si}) scaling properties of the device, simulations are done for four different values of L_{Si}, namely 36nm, 40nm, 42nm and 50nm against an inter gate separation between 2nm (for L_{Si}=36nm) and 16nm (for L_{Si}=50nm) [Fig. 4.10 (a)]. All other dimensions and parameters are kept same, as in previous sections, except that scaled metallic $NiSi_2$ S/D segments are used in all the devices same as done in [62].

It is clear from Fig. 4.10 (a) that the device characteristics are less sensitive for variations in nanowire length with a mere 18.59% and 2.66% increase (decrease) in I_{ON} (V_t) with L_{Si} scaled down from 50nm to 36nm. The robustness of the device behavior against

variation in L_{Si} is mainly because the ON current in these devices are controlled mainly through direct probing of the gated barrier, with injection of charge carriers mainly through the source Schottky junction as the main on-state current limiting factor which can be experimentally verified from [65].

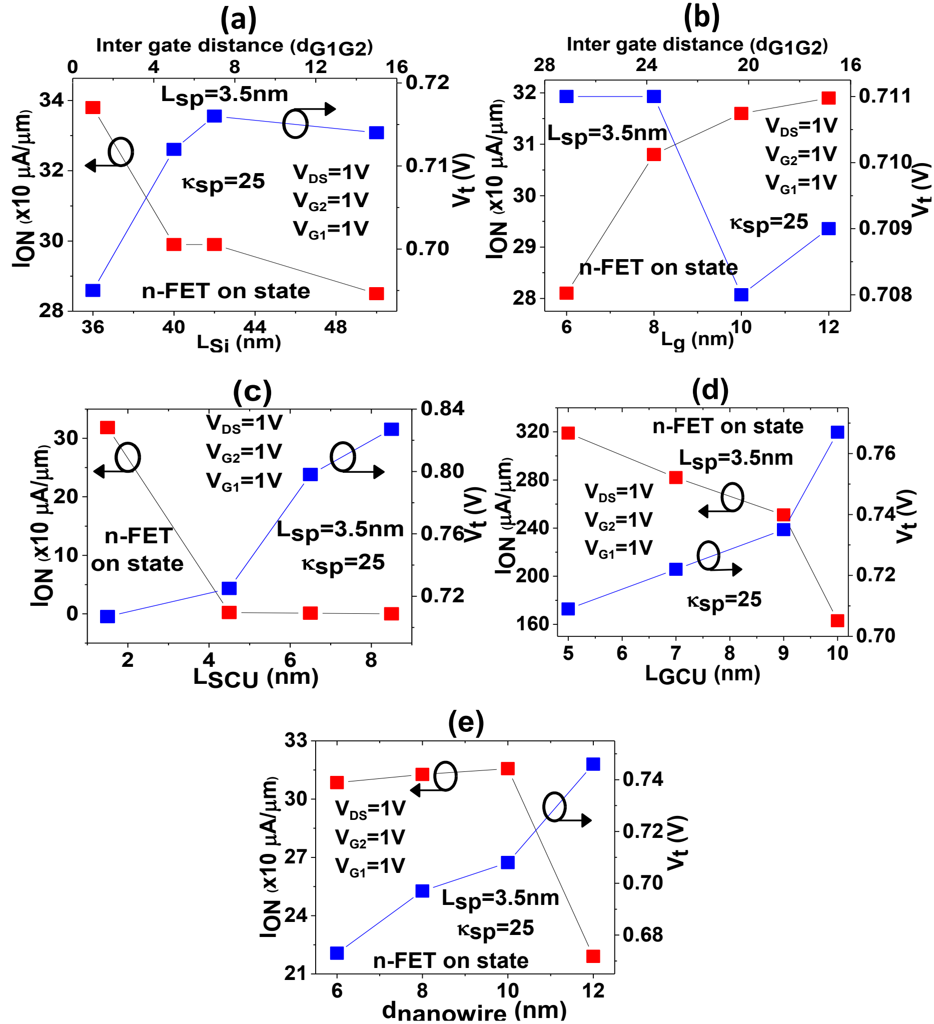


Figure. 4.10. (a) Normalized I_{ON} and V_t as a function of silicon nanowire length (L_{Si}) (b) Normalized I_{ON} and V_t as a function of gate length (L_g) (c) Normalized I_{ON} and V_t as a function of L_{SCU} (d) Normalized I_{ON} and V_t as a function of L_{GCU} (e) Normalized I_{ON} and V_t as a function of nanowire diameter ($d_{nanowire}$) for n-FET on-state of the proposed device at V_{DS}=1V, V_{G2}=1V and V_{G1}=1V.

For studying the impact of L_g scaling on device performance, device simulations are carried out for four different values of gate length, viz. 6nm, 8nm, 10nm and 12nm

respectively against an inter gate separation between 28nm and 16nm [Fig. 4.10 (b)]. It is found that the device shows 38 μA/μm rise in the normalized on current at L_g = 12nm as compared to L_g = 6nm with threshold voltage remaining almost same. The slight improvement in current drive attributes to the lowering in the parasitic channel resistance at smaller inter gate spacing (16nm at L_g =12nm) as compared to the larger one (28nm at L_g =6nm).

Whereas, the drastic improvement of device performance with L_{SCU} scaling [Fig. 4.10 (c)] is mainly because of the rise in peak electric field near the $NiSi_2$/Si Schottky junction because of the shift in outer gate edge towards the nanowire centre at fixed gate and spacer lengths; 156 μA/μm increase in normalized I_{ON} and 7.56% reduction in V_t with L_{GCU} scaling [Fig. 4.10 (d)] from 10nm to 5nm relates to up shift of the conduction band edge, thereby causing a reduction in the electron tunneling width and improved coupling between the $NiSi_2$/Si junction and metal gates at lower L_{GCU} values.

Finally, the slight improvement in I_{ON} and V_t with scaling of nanowire diameter from 12nm to 6nm [Fig. 4.10 (e)] is because of the increase in vertical electric field due to enhancement in electrostatic gate control at lower silicon film thickness.

4.6 Summary

An extensive investigation of the impact of gate/spacer-channel underlap on the device characteristics of a DG-RFET structure has been made. It is found that, the gate/spacer channel underlap has a strong impact on the BTBT dependent on-state current of the device as well as its subthreshold characteristics where thermionic emission is the dominant phenomenon. It is important because by proper designing of the gate-channel and spacer-channel underlap the I_{ON} and I_{ON}/I_{OFF} ratio of the device can be improved by orders of magnitude. A significant reduction in BTBT rate near the source end of the proposed RFET is found to take place when spacer channel underlap is increased which in turn degrades the drive current of the device drastically. Similarly, for smaller values of gate channel underlap at fixed spacer channel underlap, both current conduction and delay properties of the device is found to improve mainly because of better electrostatic coupling between gate and the Schottky junctions. Moreover, it is seen that though for a fixed EOT a higher-κ gate

dielectric can lead to better capacitive coupling, still it is expected to be beneficial from circuit performance point of view due to a reduction in intrinsic gate delay. It is also found that, though ON current improves by L_{Si}, L_g and $d_{nanowire}$ scaling but the increase is small as compared to other tunneling dependent short channel devices. On a whole, we may conclude that apart from scaling the overall nanowire dimensions, smaller gate/spacer channel underlap lengths and higher gate dielectric constant must be used for achieving the best optimized performance for the proposed S/D spacer based DG RFET.

Chapter 5

Temperature Dependence of the DC, Analog and RF Performance of the S/D Spacer Based DG-RFET

5.1 Introduction

For more than four decades of circuit implementation using CMOS technology, separate n- and p-type transistors having different dimensions are used to achieve symmetrical transfer characteristics, mainly because holes have lower mobility than that of electrons [40-70]. After the concept of a reconfigurable device first brought into limelight by L. Chua in 1971 [71] in the form of a two terminal *non-volatile* device known as *memristor* which was later on successfully demonstrated by *Hewlett Packard* in 2008, the search for a reprogrammable device concept in which the switching behavior can be tuned electrically without any modifications to the data path led to the development of today's ambipolar transistor which can provide unipolar n and p-FET behavior in a single switch. By setting the polarity gate to a particular voltage, the polarity of this device can be changed at the time of operation. This new device concept also offers a number of keynote advantages in terms of fabrication ease using the conventional bottom-up approach. It has a channel region which is nearly undoped, thus leading to reduced short channel effects (SCE's) and metallic S/D contacts [61, 46, 62] which facilitates its potential to become a lean technology in upcoming days. Circuit maturity and complex logic implementation with lesser number of transistors as required in case of planar CMOS have also been depicted in literature using this novel nanowire platform [63]. One such example is the 4-T XOR implementation (instead of 8-T as required in case of MOSFET) demonstrated recently by Marchi et. al. [63]. It is demonstrated that since polarity of the RFET can be dynamically tuned, several digital logic functions such as NOR, NAND, XOR, full adder (with merely 8 transistors) can be implemented by configuring a particular circuit having rigid polysilicon lines containing 4 similar transistors, just by altering the metal connections present at the back-end. Taking the fabricated RFET demonstrated by Heinzig et. al. [2] which shows enhanced electrical performance in terms of substantially high I_{ON}/I_{OFF} ~10^9 and extremely low gate leakage ~10^{-14} as the starting framework we have demonstrated a new source/drain spacer based *underlap* RFET

architecture in the earlier chapters which shows enhanced electrical characteristics over the *non-underlap* one. As compared to other tunneling transistors the device physics of RFET is relatively complex. The on current of the RFET depends upon BTBT and the subthreshold current is mainly thermionic emission dependent. Since thermionic emission is a strongly temperature dependent phenomenon, it is obvious that the temperature dependence of the device characteristics of the RFET cannot be neglected. Although the impact of temperature on the device performance for another class of tunneling transistors i.e. TFET has been earlier reported by various groups in [67] and [72], such an investigation has not yet been presented so far in case of a RFET. Moreover, since BTBT is a weakly temperature dependent phenomenon, the device characteristics of TFET is more or less immune to temperature variations, but in case of a RFET the same is not expected. Thus it would be highly interesting to study the temperature dependence of the device characteristics for this unique nanotransistor. Hence in this chapter, we investigate the influence of temperature using a numerical device simulator on the DC, analog and RF characteristics of an S/D spacer based DG-RFET and compare the same with other devices of the same class such as GAA, HD GAA, SiGe, full silicon TFETs and the conventional *non-underlap* RFET. For comparison purpose, we have taken data from various literatures dealing with the temperature dependence of other devices. It may be noted that in this study, we have focused more on the general trends and orders of magnitude because our primary goal is not to accurately predict the current values but to qualitatively explain the obtained results based on device electrostatics.

The rest of the chapter is organized as follows. Section 5.2 explores the impact of temperature on the DC characteristics of the proposed RFET. Apart from discussing the temperature effect on the drain current of the device, subthreshold swing (S/S), V_{th} shifts etc, we have also illustrated the thermal variation of mobility, Fermi Dirac distribution and intrinsic carrier density of the device. In section 5.3 we have investigated the temperature dependence of the analog behaviour of the device under consideration and compared the same with $Si_{1-x}Ge_x$ and 100% Si with abrupt profile (silicon at the source) TFET devices [73]. The main analog parameters used in our investigation are transconductance (g_m) Output Conductance (g_d) transconductance generation factor (g_m/I_d) and intrinsic voltage gain (A_v). The impact of temperature on the intrinsic gate capacitances and CV/I metrics for the

proposed ambipolar FET and its comparison with gate all around TFET (GAA TFET) [74] and Hetero Gate dielectric gate all around TFET (HD GAA TFET) [74] is shown in section 5.4. Intrinsic capacitances of the device such as C_{GS}, C_{GD} and C_{GG} as well as intrinsic delay τ are taken into consideration. Section 5.5 portray the effect of temperature on the RF performance of the proposed DG-RFET and compare it with the conventional *underlap* RFET device structure, described in [61] having similar device dimensions and $Si_{1-x}Ge_x$ and 100% Si with abrupt profile TFET devices [73]. For the RF analysis the various parameters used by use are the higher order transconductance coefficients, cut-off frequency (f_T), gain bandwidth product (GBW), transit time (τ_t), device figures of merits (FOMs) VIP2, the third-order intercept point (IIP3) and the third-order intermodulation distortion (IMD3). The entire study is done in between temperature minima and maxima of 250K and 450K respectively. Section 5.6 concludes this chapter with a summary.

5.2 Impact of Temperature on DC Characteristics

The device structure used in this analysis is shown in Fig. 5.1 (a). The nanowire channel has a length (L) of 220 nm and a thickness (t_{Si}) of 12 nm. Source and drain contacts are made of $NiSi_2$ having work function 4.64 eV, and both control as well as polarity gates (length=70 nm) are made of a metal whose work function (ϕ_m) is 4.6 eV. The *gate-channel-underlap* length (L_{GCU}) is kept as 5 nm [Fig. 5.1 (a)]. An equivalent oxide thickness (EOT) of 0.52 nm is considered for the gate dielectric. It can be observed from Fig. 5.1 (b) that symmetrical transfer characteristics are obtained for both the programs at T=300K. The energy band diagrams for n- and p-FET on as well as off states are shown in Fig. 5.1 (c) and (d) respectively. The models used in the simulations and optimization technique for high-κ spacers followed by us are same as mentioned in the previous chapters. The transfer characteristics of the proposed RFET with varying temperature are shown in Fig. 5.2 (a). The subthreshold current is mainly dependent on thermionic emission [2]. Since thermionic emission itself is a temperature dependent phenomenon, it gives rise to a strong temperature dependence of the subthreshold current at lower value of electric fields. It is interesting to note that the BTBT dependent ON current of the device varies weakly with temperature because the impact of temperature on BTBT is small [Fig. 5.2 (a)]. From Fig. 5.2 (b) we find

that the difference between valence and conduction band of the device (the energy band gap) reduces with increasing temperature.

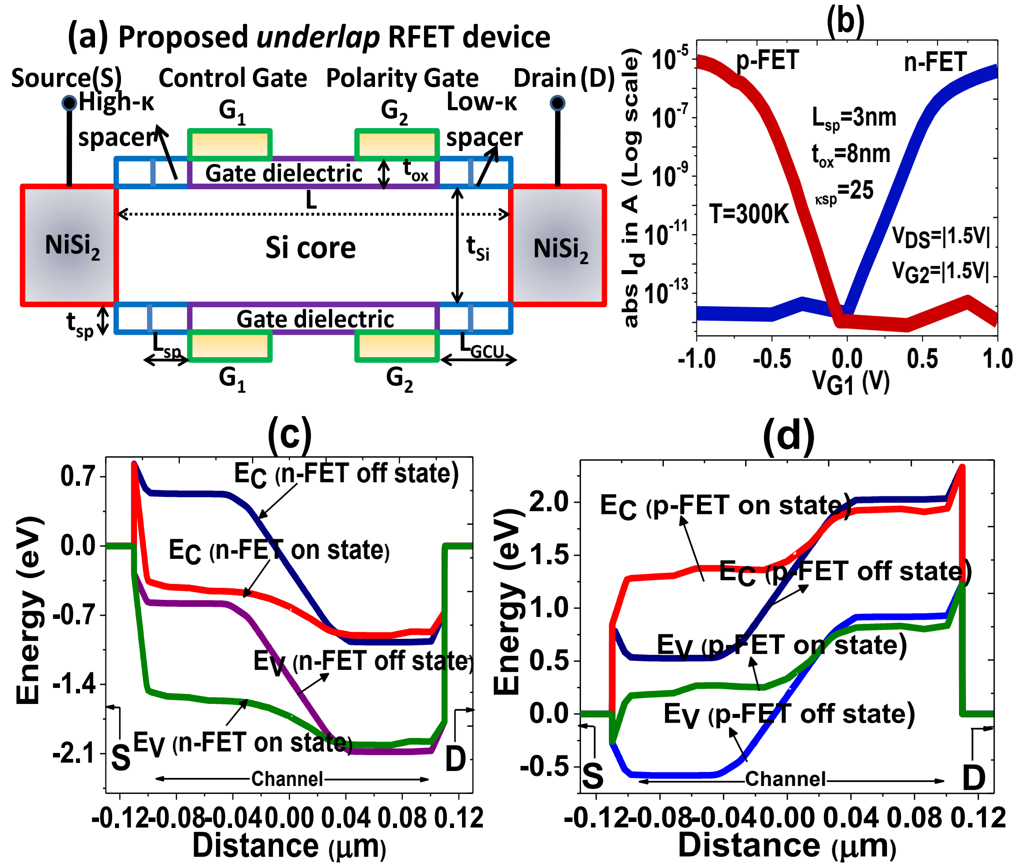


Figure. 5.1. (a) Schematic representation of the proposed device (b) Transfer characteristics for both n and p-programs (c) Energy band diagrams for n-FET on and off states (c) Energy band diagrams for p-FET on and off states.

This can be explained as follows. Energy bandgap has an inverse dependence on the tunneling current [72]. Since the tunneling current increases with an increase in temperature we find a decreasing trend in the bandgap energy with a rise in temperature. The reduction in energy bandgap is further reflected in the increase in normalized ON current with rise in temperature [Fig. 5.2 (c)]. It is interesting to note that at very high temperature beyond 350K, there is a decreasing trend in I_{ON} with increase in temperature. The slight decrease in I_{ON} beyond 350K is because of the reduction in the temperature dependent channel mobility at elevated temperatures due to enhanced scattering.

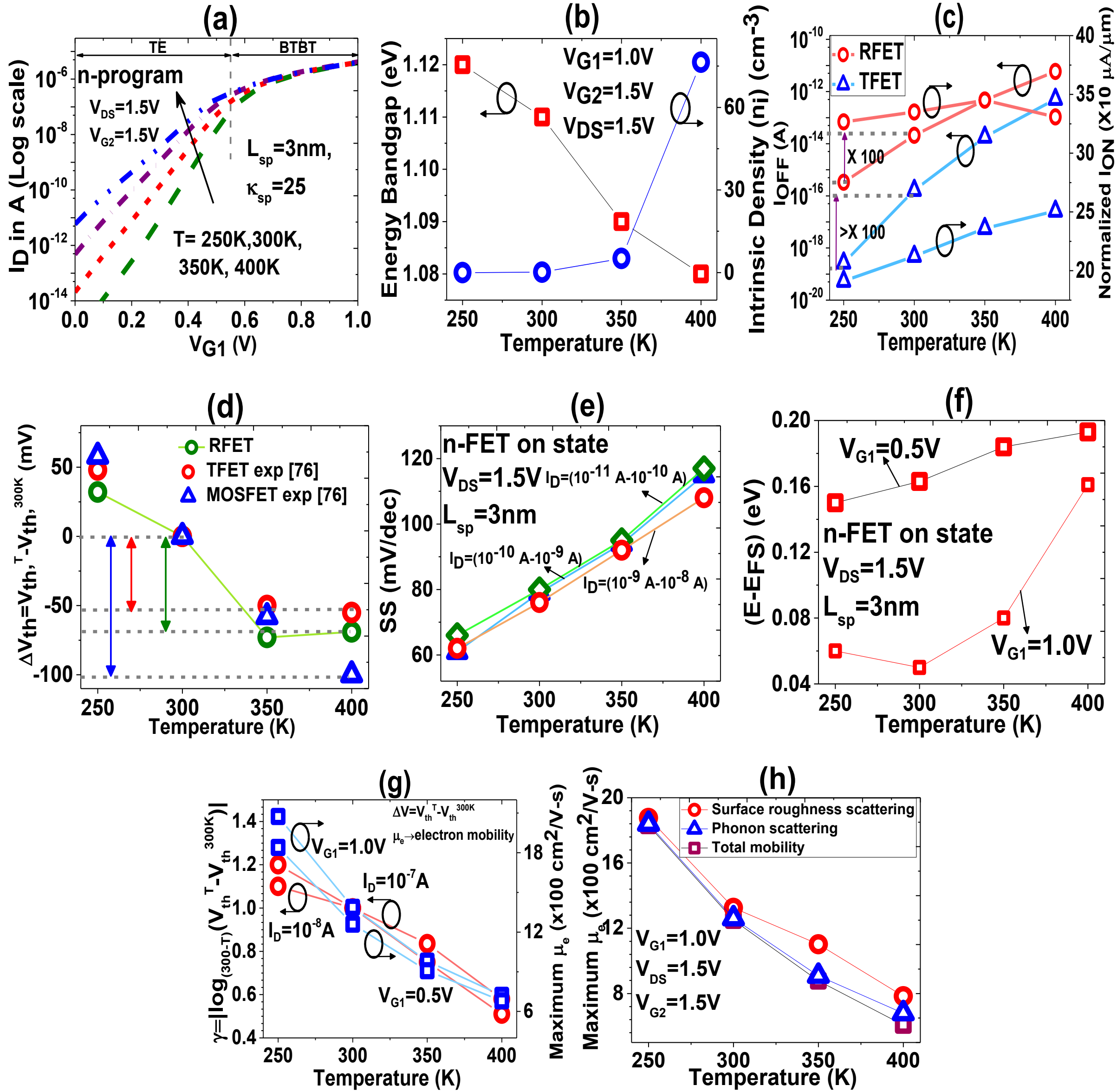


Figure. 5.2. Variation of (a) I_D (log scale) vs. V_{G1} (b) Energy bandgap and intrinsic density (c) I_{OFF} and normalized I_{ON} (d) ΔV_{th}(e) S/S (f) E-E_{FS} (g) γ and maximum mobility (h) Maximum mobility contribution due to phonon and surface roughness scattering for n-FET on state at V_{DS}=1.5V with temperature.

On the other hand, since more thermal energy is available for EHP generation due to breaking of bonds, the intrinsic carrier concentration n_i, which is proportional to exp (-Eg/2kT) (where *k* is the Boltzman constant) increases at higher temperature [Fig. 5.2 (b)]. This ultimately causes an increase in the SRH dominated gate leakage (I_{OFF}) [67] as evident from Fig. 5.2 (c). Further, it may be noted that the normalized I_{ON} of the proposed RFET rises at higher temperatures in

contrast to TFET and also the I_{OFF} increment in RFET is only two orders whereas it is more than this in case of a TFET [Fig. 5.2 (c)]. This shows the proposed RFET has better temperature stability over TFET.

The temperature dependences of V_{th} shifts in RFET and experimental TFET [76] and MOSFET [76] are shown in Fig. 5.2 (d). We have taken V_{th} values at 300K as a standard in all the calculations. Despite the fact that the common origin of V_{th} shift in all of the three devices is the bandgap narrowing with temperature [Fig. 5.2 (b)], the amount of V_{th} shifts in these devices are not equal. The dissimilarity in the amount of V_{th} shifts with respect to temperature arises mainly due to the difference in the mechanism of current flow which is primarily BTBT in case of TFET/RFET and predominantly drift in that of a MOSFET. The variation of subthreshold swing (S/S) is shown in Fig. 5.2 (e). The SS shown in Fig. 5.2 (e) is slightly larger as compared to other devices but we would like to highlight the fact that apart from all the performance gains of a RFET, the SS obtained in case of all the experimental RFET devices present in literature are always in the range of 60 mV/dec-90 mV/dec as mentioned in [2]. It may be noted that at drain current range (I_d~10^{-9}A - I_d~10^{-8}A) the S/S of the proposed RFET shows almost linear variation with temperature having a positive slope of 0.32mV/dec/K. The ΔS/S is approximately of the order of ~15mV/dec for every 50K increase in temperature. But this behavior is slightly non-linear when the device goes into nearly off state at drain current range (I_d~10^{-11}A - I_d~10^{-10}A). The slope also becomes slightly less positive in the range of 0.30mV/dec/K [Fig. 5.2 (e)] and a ΔS/S of ~14mV/dec at 250K-300K and a ΔS/S of ~22mV/dec for 350K-400K. This unusual trend can be explained from the point of view of current conduction of the device in on state and subthreshold and is mainly because of the fact that when the device gradually enters into the on state there is a dominance of BTBT phenomenon which is weakly temperature dependent and drift becomes the main carrier transport process in the silicon channel. On the other hand, it is mainly diffusion when the RFET is in near off state and the current mainly depends on thermionic emission which has strong temperature dependence. Moreover, since mobility degrades with temperature increase, S/S is found to deteriorate with temperature for all current values. The reason behind this is that at a higher temperature, more gate voltage is required to bring the same decade change in drain current. To understand this variation in subthreshold slope with temperature we have also plotted the energy difference between the source side conduction band and Fermi level

with temperature in Fig. 5.2 (f). Note that with increasing temperature the Fermi level is pinned further down (energy difference is increasing), as a result of which the probability of the Fermi function f(E) existing above the Fermi level becomes higher and the Fermi tail cut off by the band gap becomes larger and larger. At very low current levels this cut off becomes almost negligible which eventually gives rise to the decreasing slope of S/S versus T since the temperature dependence of the tunneling current comes mostly from the Fermi-Dirac distribution. Moreover, to depict the thermal dependence of the threshold voltage more uniquely we have introduced a parameter γ. The non linear shift in the threshold voltage with temperature [Fig. 5.2 (d)] (which is smaller than the MOSFET) can be captured in this single parameter γ. Since, $\Delta V_{th}=V^{T}-V^{300K}$, using an arbitrary fitting parameter γ we can write $\Delta V_{th}=(300-T)^{\gamma}$, or in other words $\gamma=\log_{(300-T)}(V^{T}-V^{300K})$. It is seen that γ is found to be greater than 1 and shows significant variation with temperature [Fig. 5.2 (g)], thus providing a concrete way to characterize the temperature dependence of V_{th}.

Finally, the maximum mobility is found to degrade above room temperature (300K) [Fig. 2 (g)]. This can be explained from the fact that the device mobility is limited by phonon scattering [Fig. 5.2 (h)] in that temperature range. It may also be noted that on a whole the mobility is mainly dictated by the surface roughness. To make this point more clear we have also shown the temperature variation due to phonon boundary scattering (using the ConstantMobility model in *Sentaurus TCAD*) and surface roughness scattering (using the Enormal model in *Sentaurus TCAD*). It may be noted that the *TCAD* tool mobility model is unable to fully capture the correct device physics related to phonon boundary scattering at higher temperature values and due to phonon confinement and diffused scattering of phonon modes, the carrier phonon scattering rates may get enhanced at higher temperatures. The electron phonon scattering rate as obtained from *Sentaurus TCAD* using the ConstantMobility model is about 4.67 arb. units. We have also calculated the temperature coefficients for phonon boundary scattering as well as surface roughness scattering. The temperature coefficient α [obtained using the formula $\Delta\mu=\mu_o(1+\alpha\Delta T)$, where μ_o the mobility of silicon at 273K and taken approximately as 1568 $cm^2/V\text{-}s$] for phonon boundary scattering is found to be 0.0034 $cm^2/V\text{-}s\ K$ and for surface roughness scattering it is found to be 0.0040 $cm^2/V\text{-}S\ K$.

5.3 Temperature Influence on the Analog Performance

We have plotted the transconductance (g_m) as a function of temperature in Fig. 5.3 (a). Although no major change is noticed as the temperature rises, there is clearly a slight positive impact on the transconductance values for the RFET as compared to SiGe TFET device [73] and almost 1 order of magnitude difference with the full silicon transistor [73] configuration. This is mainly due to the BTBT dominated current conduction in the former cases and trap assisted tunneling (TAT) dominance in the latter. Fig. 5.3 (b) shows the variation of output conductance (g_d) for the 3 devices following the same temperature variation. Even if all of the devices show positive temperature coefficient, the BTBT dominated devices again show higher values due to larger drain voltage impact. This can be verified from Fig. 5.3 (c) which clearly shows that the maximum BTBT rate for the proposed RFET increases with increasing drain bias for all temperatures which is mainly because of the reduction in minimum tunnel width due to an up shift in conduction band edge near the source side (which is also the tunnel source) of the device as shown in Fig. 5.3 (d). Fig. 5.3 (e) illustrates the temperature impact on the transconductance generation factor (g_m/I_d) for the 3 device configurations. A decrease is noticed in the peak g_m/I_d values at higher temperatures which relates to the difference in transport mechanism which is TAT for SiGe [73], full silicon TFETs [73] and thermionic emission for RFET in the subthreshold region (g_m/I_d peak) and BTBT in the superthreshold (high I_d) for all the 3 cases. The intrinsic voltage gain susceptibility to the temperature is displayed in Fig. 5.3 (f).

In spite of the fact that all the devices show a negative trend with temperature under BTBT dominance affirming a degrading performance at higher temperatures, the proposed RFET is expected to be more suitable for analog applications at room temperature because of the higher values of A_v. Table 5.1 summarizes the comparison data for various analog performance parameters with temperature variation for the 3 device instances mentioned above.

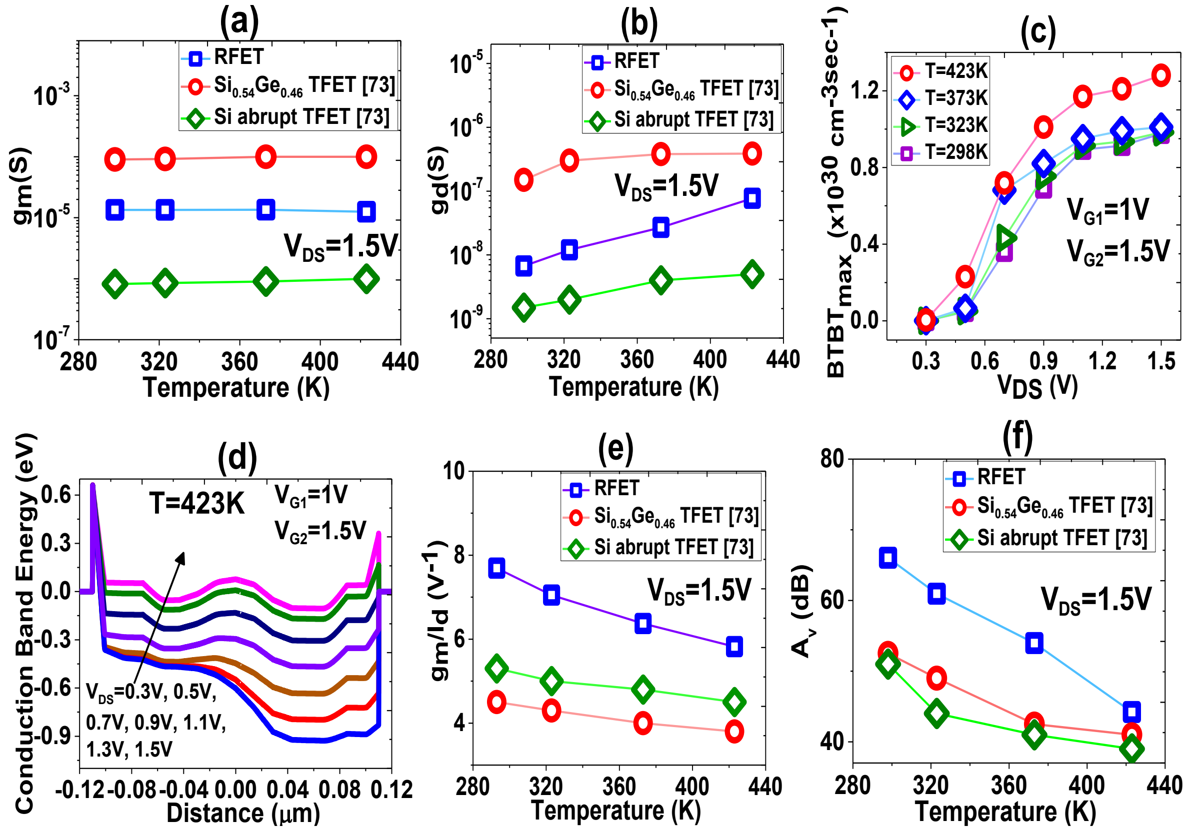


Figure. 5.3. Variation of (a) Transconductance (g_m) (b) Output Conductance (g_d) (c) BTBT max (d) Conduction band energy (e) Transconductance generation factor (g_m/I_d) (f) Intrinsic voltage gain (A_v) for the proposed RFET, experimental $Si_{0.54}Ge_{0.46}$ TFET [73] and Si abrupt TFET [73] for n-FET on state at V_{DS}=1.5V with temperature.

Table 5.1 Performance Analog Performance Comparison with Temperature Variation for Proposed RFET, $Si_{0.54}Ge_{0.46}$ TFET [73] and Si abrupt TFET [73]

Analog Parameters	Proposed RFET	$Si_{0.54}Ge_{0.46}$ TFET [73]	Si abrupt TFET [73]
g_m (S/K)	7.2×10^{-9}	8×10^{-8}	1.44×10^{-9}
g_d (S/K)	5.624×10^{-10}	1.88×10^{-9}	2.8×10^{-11}
g_m/I_d ($V^{-1}K^{-1}$)	0.01496	0.0056	0.0064
A_v (dB/K)	0.17456	0.092	0.096

5.4 Effect of Temperature on Capacitive Behavior

The extraction of various capacitances in this entire analysis is done through AC small signal analysis at a frequency of 1MHz.

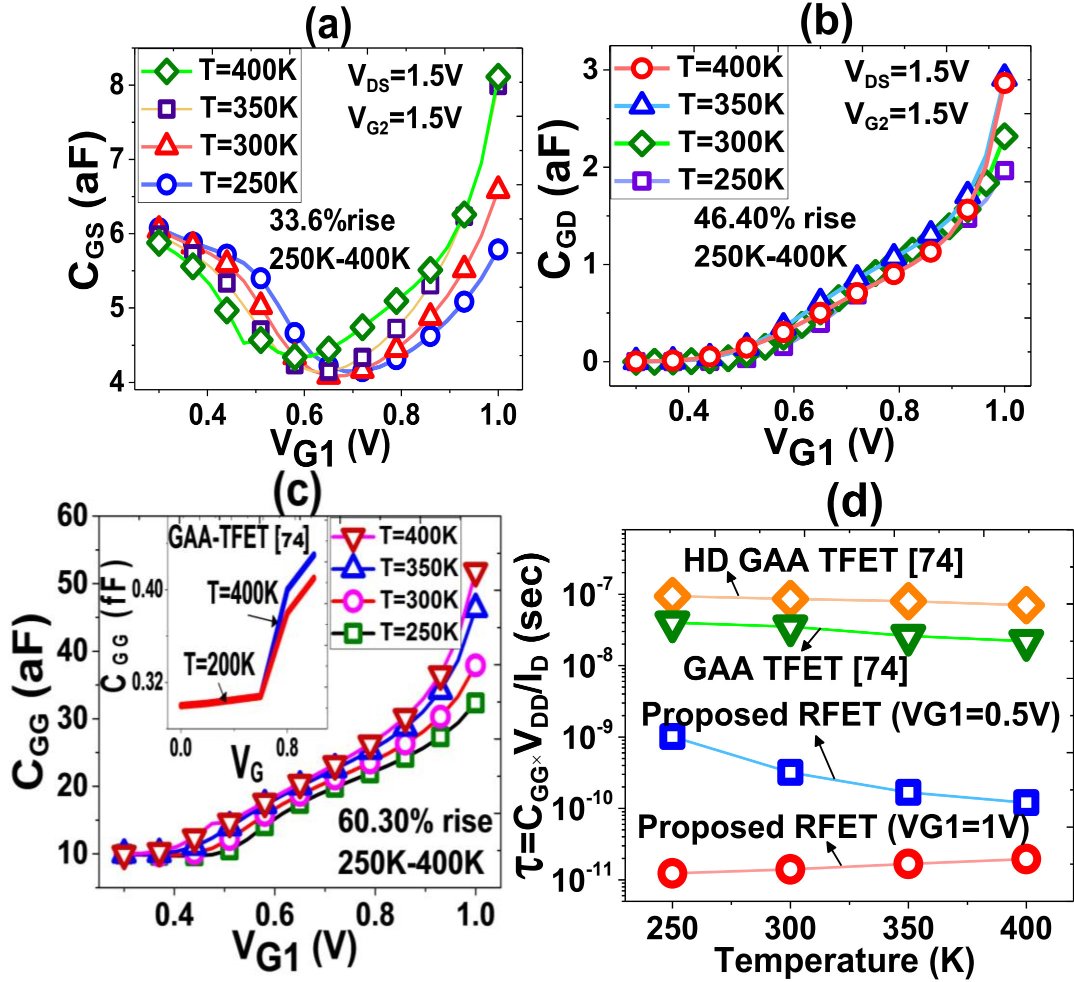


Figure. 5.4. Variation of (a) Gate to source capacitance (C_{GS}) with V_{G1} for varying temperature (b) Gate to drain capacitance (C_{GD}) with V_{G1} for varying temperature (c) Total gate capacitance (C_{GG}) with V_{G1} for varying temperature (d) Intrinsic delay for proposed RFET (n-FET on state), HDD TFET [74] and GAA TFET [74] with temperature.

It is well known that the intrinsic capacitances depend upon the operating region of the device. It is clearly observed from Fig. 5.4 (a), (b) and (c) that for the proposed device, C_{GS}, C_{GD} and C_{GG} increase with V_{G1} until saturation, with the increase being dominating at higher temperature. It is calculated that the peak values of the above mentioned parasitic capacitances increase by 33.65, 46.4% and 60.3% respectively with an increase in

temperature from 250K to 400K. The physical mechanism behind this behavior can be explained as follows. With increase in V_{G1}, the control gate (near the source side $NiSi_2$/Si junction) electrostatically induces charges of the desired carrier type (electrons for n-program and holes for p-program) into the channel region of the nanowire which causes C_{GS} and C_{GD} to increase and reach the maximum just at the onset of saturation. With an increase in the temperature there is a rise in the flatband voltage (V_{FB}) due to higher intrinsic carrier concentration (n_i) and a reduction in the threshold voltage (V_{th}) resulting in positive temperature coefficients of C_{GS} and C_{GD}. At higher gate biases, the values of capacitances are determined by the onset of quasi-saturation. Since the quasi-saturation current (the drain current just at the onset of saturation) increases with temperature rise, the peak values of capacitances also increases [75].

It may be noted from Fig. 5.4 (c) that the total gate capacitance C_{GG} of the RFET is almost 3 orders of magnitude lower than GAA TFET [74]. The reason behind this is twofold. Firstly, the channel region in case of RFET is almost intrinsic (and even if doping is done it is in very light in the order of 10^{15} cm^{-3}), whereas in case of TFET the channel is highly doped in the order of 10^{19} cm^{-3}. Secondly, in TFET the potential drop is negligible near the drain-channel junction due to a larger reverse bias leading to a comparatively large gate-drain capacitance (C_{GD}). Now, since C_{GG} is contributed almost equally by C_{GS} and C_{GD} in case of a GAA TFET, even a comparatively smaller increase in C_{GS} actually leads into an enhanced C_{GG}. From Fig. 5.4 (d) it is clear that there is also a considerable reduction in intrinsic gate delay (τ) in case of RFET as compared to GAA TFET [74] and HD GAA TFET [74] which can be a detrimental factor deciding the operating speed of the device. Quantitatively at V_{G1}=1V, τ reduces by 10^{-3} s in comparison with GAA TFET and by 10^{-4} s for HD GAA TFET respectively for the entire temperature range. This reduction is mainly due to an enhanced I_{ON} in case of the proposed device as compared to its other counterparts. Note that the trend of delay is slightly different for the RFET at V_{G1}=0.5V and 1V which is mainly because the difference in the values of total gate capacitance (C_{GG}) and drain current (I_d) at these two gate biases. We would like to highlight the fact that that τ plays a critical role in benchmarking a transistor's performance for digital logic applications and the switching speed of any device depends upon the intrinsic capacitances, the smaller values of intrinsic delay and parasitic capacitances make the proposed RFET more reliable for low as well as

high temperature applications.

5.5 Temperature Dependence of the RF Characteristics

The various metrics used in this study are higher order transconductance coefficients, cut-off frequency (f_T), gain bandwidth product (GBW), transit time (τ_t), device figures of merits (FOMs) VIP2, the third-order intercept point (IIP3) and the third-order intermodulation distortion (IMD3). f_T is the parameter which is computed as the frequency at which the short circuit current gain drops to unity. The variation in f_T with temperature at V_{DS}=1.5V can be seen from Fig. 5.5 (a). The device under study reflects its superior performance in terms of higher f_T. The difference in f_T values between the proposed and conventional RFET and TFET devices is mainly due to the difference in the values of g_m and C_{GS}. Though the conventional device shows almost no variation in cut-off frequency with temperature, the slight decrease in f_T in case of the proposed RFET is mainly due to an increase in C_{GS} with temperature rise [Fig. 5.4 (a)]. Moreover, we would like to state that the range of capacitances in case of both SiGe TFET [73] and Si TFET [73] is in the order of fF which in turn results in a lower f_T in their case as compared to the proposed RFET in which the gate capacitance is in aF range [Fig. 5.4]. Similar explanation also holds true for the variation of gain-bandwidth product (GBW) with temperature as shown in Fig. 5.5 (b). Although the figure clearly reflects an enhancement in GBW for the proposed device, a degradation at higher temperature relates to an increase in total gate capacitance C_{GG}. The higher f_T values of the spacer based RFET is also reflected in almost two orders of magnitude reduction in the transit time (τ_t) [Fig. 5.5 (c)] as compared to other devices which is a decisive factor in determining the speed of any device. Another important RF figure of merit is the VIP2 which decides the distortion characteristics for various dc parameters. A larger value of VIP2 is demanded for a distortionless operation and high linearity performance. The variation of VIP2 with temperature for all the devices is shown in Fig. 5.5 (d). It is observed from the figure that the proposed architecture is quite immune to variation in VIP2 with respect to temperature and corresponds to a higher value of VIP2 as compared to the conventional one

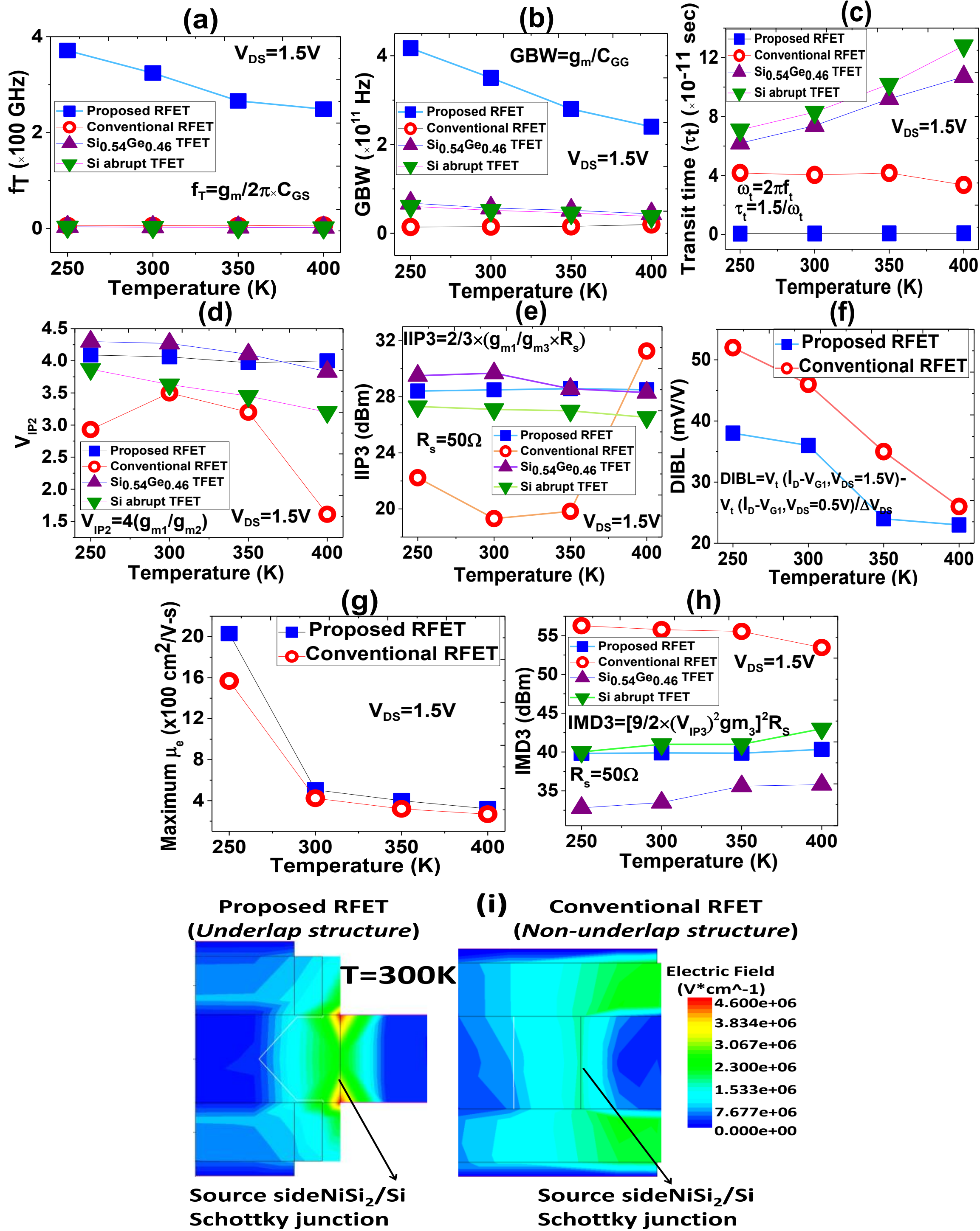


Figure. 5.5. Variation of (a) Cut-off frequency (f_T) (b) Gain bandwidth product (GBW) (c) Transit time (τ_t) (d) V_{IP2} (e) IIP3 (f) IMD3 (g) DIBL (h) Maximum mobility (i) Electric Field contour with temperature for the proposed RFET (n-FET on state), conventional RFET described in [61], with similar device dimensions, $Si_{0.54}Ge_{0.46}$ TFET [73] and Si abrupt TFET [73].

and slightly lower value as compared to SiGe TFET because it has a higher g_{m1} as compared to the conventional RFET but lower than that of SiGe TFET. The degradation in VIP2 value for the conventional device is mainly because of an increase in the second order transconductance coefficient (g_{m2}) with temperature. Fig. 5.5 (e) displays the variation of third-order intercept point (IIP3) with temperature which is a crucial FOM required for optimizing the bias point for RFIC design. A comparatively higher carrier transport efficiency and hence a superior gate control over the channel as compared to the conventional RFET are the main reasons due to which the *underlap* RFET device portrays an improvement in IIP3 and almost a similar performance trend like SiGe TFET, although even in this case the variation with temperature is quite negligible. To justify this statement we have also shown the comparison of DIBL and electron mobility along with the electric field contours between the proposed and conventional RFET devices in Fig. 5.5 (f), (g) and (i) respectively. It can be observed that due to better electrostatic coupling between the high-κ spacer and the $NiSi_2$/Si Schottky junction owing to the *underlap* device architecture the proposed RFET shows enhancement in the lateral electric field at the Schottky junction [Fig. 5.5 (i)] as compared to the *non-underlap* conventional RFET device. Moreover, because of higher electric flux concentration below the gate, the control of gate over the channel as compared to drain becomes better for the proposed RFET which results in reduced DIBL [Fig. 5.5 (f)]. A better gate control and higher carrier transport efficiency of the device under consideration is further reflected in higher channel mobility as can be seen from Fig. 5.5 (g). Finally, Fig. 5.5 (h) shows the variation of third order intermodulation (IMD3) distortion as a function of temperature for all the devices. IMD3 mainly arises from the nonlinearity displayed by the static characteristics of any device, thus causing signal distortion in wireless networks. On an average a 15-20 dB reduction in the third order harmonics is exhibited by the proposed reconfigurable topology over the entire range of temperature [Fig. 5.5 (h)]. This relates to the enhancement of device power and hot carrier immunity, hence causing lowering of distortion.

5.6 Summary

A comprehensive study regarding the temperature effects on the device performance of a spacer based RFET and its comparison with other relevant tunneling based devices has done. With orders of magnitude lesser V_{th} roll-off as compared to MOSFET, the proposed device is found to have a better thermal stability over TFET owing to a smaller I_{OFF} increment and larger ON current at higher temperatures which would be a strong motivation for using this device in various low power applications requiring strict V_{th} control. The device under consideration also shows excellent analog performance with higher values of g_m, gm/I_d and A_v over the considered temperature range as compared to SiGe and full silicon TFETs mainly because of better tunneling barrier properties which give rise to a dominant BTBT current and better controllability of gate over the channel. Orders of magnitude reduction in C_{GS}, C_{GD}, C_{GG} and hence intrinsic delay (τ_d) is observed for all temperatures in case of the proposed ambipolar FET as compared to GAA and HD GAA TFET owing to a different device geometry and nearly undoped channel. Finally, superior RF performance and lower third order harmonics is shown by the *underlap* RFET device for low as well as high temperatures as compared to the conventional reconfigurable topology, SiGe and full silicon TFETs which guarantees a linear operation with low signal distortion and higher input power. Apart from its distinguished overall performance, its RF/analog FOMs are found to be immune to fluctuations in temperature which make it a strong contender for applications demanding rapid temperature variations.

Chapter 6

Modeling of S/D Spacer Based DG-RFET and its Verilog-A Model Development for Digital Applications

6.1 Introduction

We have discussed how the reconfigurable nanowire field effect transistors (RFETs) are excellent candidates in this era of continuous downscaling of nanotransistor. The concepts of ambipolar FETs have also been studied at device level by using various semiconductors other than silicon such as graphene. Nevertheless, the implementation of a fully operational polarity controllable device by using an extra gate to electrostatically tune the Schottky junctions working equally well both at device and circuit levels is only achieved using silicon in the form of today's RFET device as mentioned here. There are various device modeling works on SiNWFETs with Schottky junctions. But to the best of our knowledge till now, a physics based compact model is not illustrated for ambipolar SiNWFETs in any of the literature. Most of the modeling of Schottky barrier FETs (SBFETs) are done either using Non-Equilibrium Green's function (NEGF) or relatively easier semi classical method [80, 81]. The former method is accurate but time consuming as well as on rigorous quantum mechanical based computations are required. Due to the complex calculations involved in this approach, it is very tough to make simpler spontaneous illustrations and design devices based on physical understanding of the device physics. Moreover, it provides insufficient insight from circuit applications point of view. On the other hand, semi-classical methods can be computed easily and efficiently. Moreover, they are based on core device physics and can be easily parameterized making it easier for design engineers. Up to a channel length of 10 nm a semi-classical approach can be applied for DG MOSFET, FiNFET and other planar devices [82]. But we cannot avoid a quantum mechanical approach for devices like SBFETs which rely on modulating the tunneling probability through source/drain metallic contacts by changing the applied gate bias. The available models for SBFETs, mainly rely on semi-classical techniques in addition to quantum mechanics for calculating the tunneling probability at Schottky junctions. Though some of the models described earlier in were more effective than NEGF methods, but were incapable for simulations which were needed for

circuit design engineers because of 2 complex computational steps: (i) tunneling probability calculation at the Schottky barriers and (ii) evaluating the surface potential in the channel self-consistently. By taking SBFETs in the quantum capacitance range only, efforts have also been made in to eradicate the necessity for self-consistent solution and make them computationally efficient. The main drawback of this technique is that they can be applied only for ultra scaled parasitic free devices. Models using ballistic transport phenomenon and lumped capacitances are also discussed in [82], [83]. The more simplifications are incorporated, the more it becomes a question whether the device performance and its transient response will be affected or not. The use of integral functions as described in [82] and [83] involves rigorous mathematical calculations which make its use in various circuit simulators such as HSPICE almost impossible. One of the techniques to improve the runtime is the polynomial fitting approach described in [84], but when device parameters are changed the performance evaluation of GAA SBFET becomes difficult. For a SBFET with undoped channel and tunneling at S/D contacts, the published models for conventional GAAFET's are not enough to fully examine the complex electrostatic and short channel effects (for very small channel lengths) on both on current and effective gate capacitance. To evaluate the SBFET performance from circuit point of view with a higher level of accuracy, a SBFET-device model with a higher degree of circuit-compatibility which also incorporates the typical device level nonidealities is essential. Unlike any other tunneling based silicon nanowire FET, thus the main thirst for RFET is also to develop a physical model which is not only easy to understand but also can be easily parameterized so that it can become highly useful for design engineers too. Although some of the aspects of this device has been studied through numerical simulations, but a compact analytical model which is required for future circuit design and further understanding of this device functioning and also able to describe the SCE's completely is yet to be developed. Thus the objective of this chapter is to develop an analytical surface potential and drain current model for the S/D spacer based DG-RFET by solving both drift diffusion in the silicon channel and carrier tunneling at the $NiSi_2$/Si Schottky contacts.

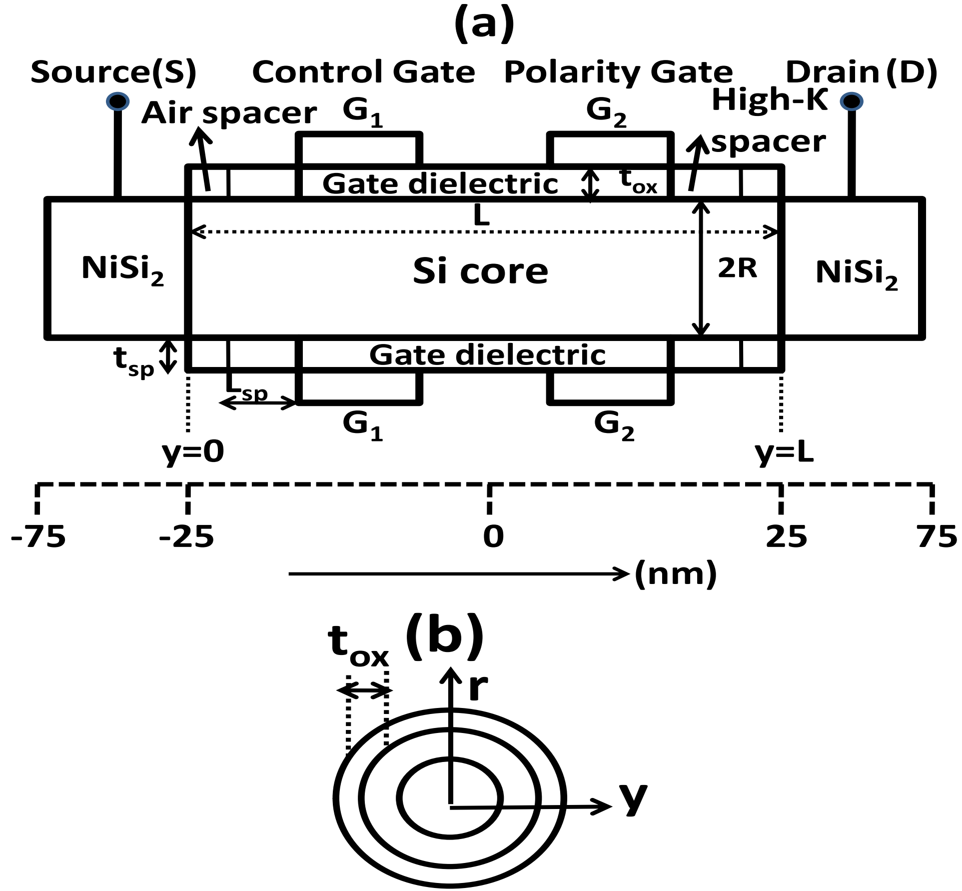


Figure. 6.1. (a) Schematic representation (drawn not to scale) (b) Cross sectional view of the target S/D spacer based RFET.

Fig. 6.1 (a) and (b) show the schematic and cross sectional view of the proposed dual gate reconfigurable SiNWFET (silicon nanowire field effect transistor) with S/D spacers placed on either side of the gate electrode (length, L_G=12 nm) having mid-gap workfunction of 4.6 eV. The nanowire channel is lightly p-doped ($10^{15}cm^{-3}$) and a room temperature drift diffusion (DD) formulation is considered in it. Quantum mechanical tunneling model (Wentzel-Kramers-Brillouin approximation) with electron and hole tunneling masses as 0.3 m_o and 0.2 m_o respectively [61] along with thermionic emission model is applied at the $NiSi_2$/Si Schottky contacts. Schottky barrier height for electrons (ϕ_{Bn}) is taken as 0.59 eV [61]. The Philips unified mobility model (PhuMob) is used to describe mobility degradation due to carrier-carrier scattering mechanisms. The recombination terms include the conventional Shockley-Read-Hall (SRH) expression (to account for recombination via traps),

recombination via band-to-band tunneling and Auger effects. Length (L_{ch}) and diameter ($d_{nanowire}$) of the lightly p-doped (10^{15} cm^{-3}) silicon nanowire channel is kept as 50 nm and 12 nm respectively. The *gate-channel underlap* (L_{GCU}) region (the space in between the outer gate edge and Schottky junctions) is kept as 5 nm on either side of the midgap metal gates to incorporate the HfO_2 spacers of length, L_{sp}=3.5 nm and thickness, t_{sp}=8 nm, where L_{sp} is the length and t_{sp} is the thickness of the high-κ spacers. The optimization of the high-κ spacer length is done through a series of TCAD simulations for various spacer lengths of the device under study taking I_{ON}/I_{OFF} ratio as the performance metric for evaluation (as shown previously in chapter 3). A low-κ material (ε_r=1) is used in the region between the high-κ spacer and $NiSi_2$/Si Schottky junction [Fig. 1(a)] to correctly model the impact of air spacer in TCAD simulations. Thickness of the gate dielectric is kept as 8nm (EOT=0.52 nm). To dynamically switch the device polarity between n- and p-type, metallic source and drain contacts made up of $NiSi_2$ (work function=4.64 eV) are present [Fig. 6.1 (a)] which facilitate the formation of $NiSi_2$/Si Schottky contacts. Drift-diffusion transport and a coupled Poisson's equation is self consistently solved within the silicon channel and WKB approximation is used to calculate the tunneling at Schottky junctions. Quantum mechanical effects are not considered in our simulations since the thickness of the silicon film in this case is greater than 10nm (R>10 nm). However, one has to consider quantum confinement for films thinner than 10nm as it leads to an increase in threshold voltage and reduction in the channel charge density [79].

The device polarity can be electrically tuned by alternatively using control gate (G_1) and polarity gate (G_2). To make the device act as a n-FET, control gate voltage (V_{G1}) is swept from negative to positive values keeping both drain and polarity gate (G_2) at fixed positive biases, initiating downward bending of the conduction band edge which makes it easier for the electrons to tunnel from source side into the nanowire channel region [Fig. 6.2 (b)]. For p-FET operation, alternate biasing is applied to polarity gate as well as drain which initiates upward band bending, assisting hole tunneling from the source side towards the drain end of the device [Fig. 6.2 (b)]. Fig. 6.2 (c) shows the I_D-V_{G1} characteristics of the device at V_{G2} and V_{DS} both kept at 1V. It offers a high I_{ON}/I_{OFF} ratio (> 10^8) and a normalized on-current (normalization done with respect to nanowire diameter) of 181.67 μA/μm (150 μA/μm) for n (p-FET). From the surface potential plot as shown in Fig. 6.2 (d) we can see that most of the

potential actually drops across the nearly intrinsic channel region of the nanowire as expected, mainly

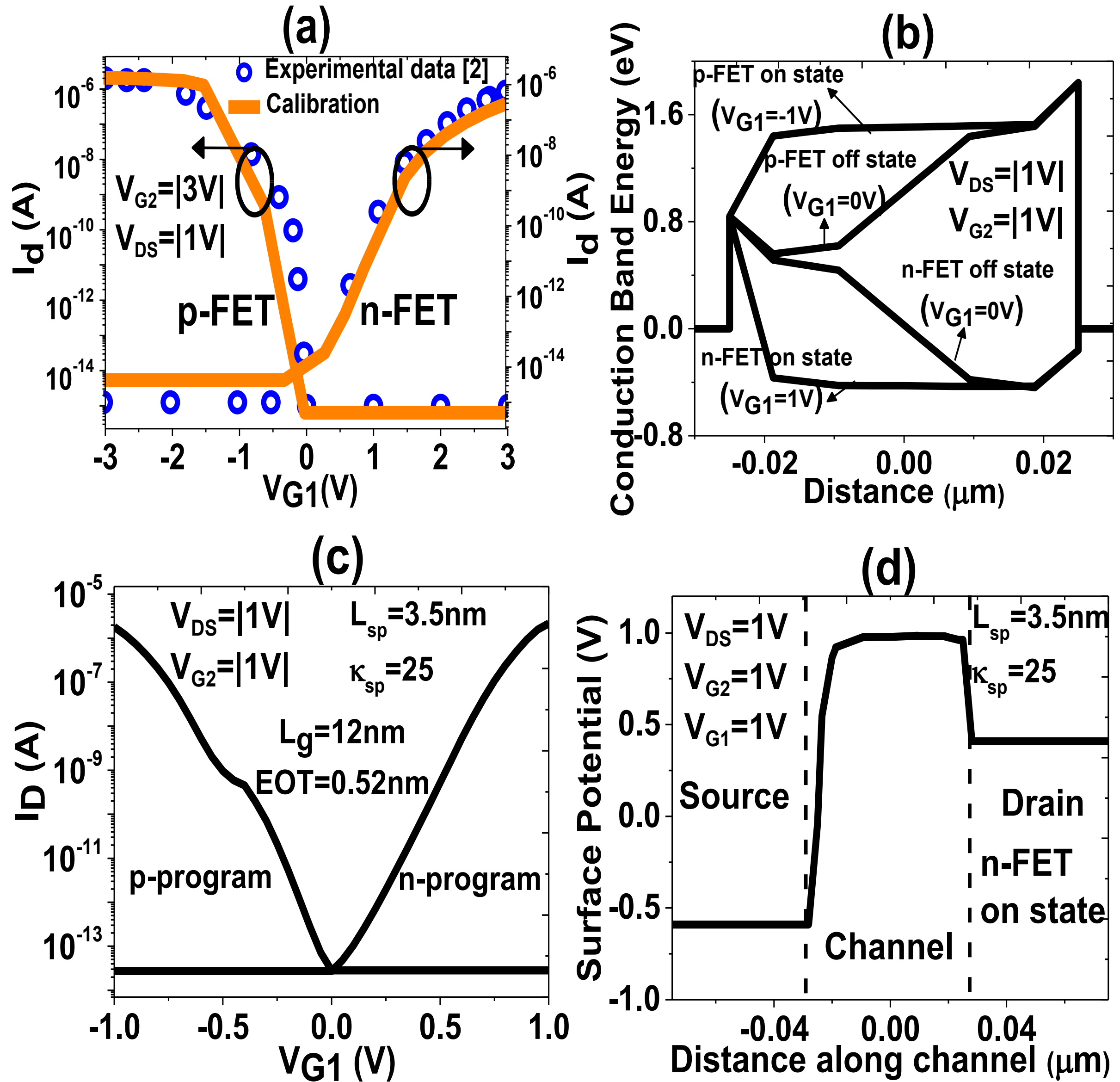


Figure. 6.2. (a) Reproduction of experimental results in [2] using TCAD simulations (b) Simulated conduction band profiles for n-FET and p-FET on and off-states (c) Transfer characteristics at V_{G2}=|1V|, V_{DS}=|1V| (d) Surface potential for n-type device at V_{G1}=1V, V_{G2}=1V, V_{DS}=1V of the proposed RFET.

because it is almost depleted of mobile charge carriers.

In this chapter, we initially develop a charge density expression, which was subsequently used to model the surface potential and drain current. The values of the quasi fermi potentials for electrons and holes for various regions of the device are obtained by

solving the current continuity equation rigorously. The potential modeling is done by generating a single-piece-approximation of the long channel surface potential by using the charge density expression and solving the 2-D Poisson equation in the silicon channel. Then it is added to the potential distribution at the Schottky contacts which is solved by using a quasi-2D approach. Finally, to model the drain current, we first find the barrier height required for the carriers to overcome the maximum potential barrier induced in the channel by the control gate near the source end of the device. Then we use the same to find out the current through the Schottky barriers. This is further equated based on the principle of current continuity with the drift diffusion current in the channel which is obtained using the earlier derived charged density model to generate a final drain current expression.

The validation of the developed potential profile and current characteristics is done by comparing the same with 3-D numerical TCAD simulations. To ensure the correctness of our simulation set up, we have calibrated the BTBT model and other tunneling parameters as shown in Fig. 6.2 (a) to accurately reproduce the experimental results reported in [2], with same device dimensions as used in this work.

6.2 Model Development

6.2.1 Surface Potential Model

We start with the Poisson's equation for an undoped silicon nanowire taking into account the gradual channel approximation (GCA) considering the variation of potential along the r direction only fixed in y direction,

$$\frac{d^2\psi(r)}{dr^2}+\frac{1}{r}\frac{d\psi(r)}{dr}=\frac{kT}{q}\delta e^{\frac{q(\psi(r)-V)}{KT}} \tag{6.1}$$

where, $\delta=q^2n_i/kT\varepsilon_{Si}$, n_i is the intrinsic concentration of carriers, q is the charge of electron, ε_{Si} is the permittivity of silicon, V is the quasi fermi potential of the carriers (electrons or holes) and ψ is the electrostatic potential. Since, here we have to consider both electron and hole transport, Eq. (6.1) is re-written as,

$$\frac{d^2\psi(r)}{dr^2}+\frac{1}{r}\frac{d\psi(r)}{dr}=\frac{kT}{q}\delta\left[e^{\frac{q(\psi(r)-V_n)}{KT}}-e^{\frac{q(V_p-\psi(r))}{KT}}\right] \tag{6.2}$$

where, V_n and V_p are the electron and hole quasi fermi potentials respectively. We would like to mention in the context of this chapter that we have assumed the quasi fermi potentials of electrons to be constant within each sub region of the device and labeled them as $V_{n,(p),G1SS}$, $V_{n,(p),G2SD}$, $V_{n,(p),G1G2}$, $V_{n,(p),SS,S}$, $V_{n,(p),SD,D}$ and the surface potentials are also labeled as ψ_{G1SS}, ψ_{G2SD}, ψ_{G1G2}, $\psi_{SS,S}$, $\psi_{SD,D}$ where G_1SS, G_2SD, G_1G_2, SS,S and SD,D refer to control gate-source side spacer, polarity gate-drain side spacer, region between two gates, source side spacer and source and drain side spacer and drain respectively.

The necessary boundary conditions required to solve Eq. (6.2) are:

$$\frac{d\psi}{dr}(r=0)=0, \psi(r=R)=\psi_S \tag{6.3}$$

ψ_S being the surface potential.

Again, the total charge per unit gate area is given as, $Q = C_{ox}(V_{gate}-\psi_S)$, where C_{ox} is the oxide capacitance per unit area and can be written as $\varepsilon_{ox}/(R\ \ln(1+t_{ins}/R))$. Now, from Gauss's law we can write,

$$C_{ox}\left(V_{gate}-\psi_S\right)=Q=\varepsilon_{Si}\frac{d\psi}{dr}\Big|_{r=R} \tag{6.4}$$

Where, V_{gate} is the applied gate bias. Considering current flow in the y-direction and assuming quasi fermi potentials to be constant along the direction of nanowire radius r, the surface potential ψ_S is first solved analytically for electrons from Eq. (6.2) using a similar approach as in [79] yielding,

$$\psi_{S,n}(r)=V_n+\frac{kT}{q}\ln\left(\frac{-8A_n}{\delta\left(1+A_n r^2\right)^2}\right) \tag{6.5}$$

for n-FET, if $V_{gate}>>(V_n+V_p)/2$ and

$$\psi_{S,p}(r)=V_p-\frac{kT}{q}\ln\left(\frac{-8A_p}{\delta\left(1+A_p r^2\right)^2}\right) \tag{6.6}$$

for p-FET, if $V_{gate}<<(V_n+V_p)/2$.

Here, A_n and A_p are constants. Using second boundary condition of Eq. (6.4) constants A_n and A_p are evaluated as,

$$A_n = -\frac{Q_n}{(Q_n + \frac{4\varepsilon_{Si}}{R}\frac{kT}{q})R^2},$$

$$A_p = -\frac{Q_p}{(Q_p + \frac{4\varepsilon_{Si}}{R}\frac{kT}{q})R^2} \quad (6.7)$$

Using $\psi_{S,n}(r)$ from Eq. (6.5) in (6.4) we solved for electrons,

$$C_{ox}\left(V_{gate} - V_n - \frac{kT}{q}\ln\left(\frac{-8A_n}{\delta(1+A_n r^2)^2}\right)\right) = \varepsilon_{Si}\frac{d[V_n + \frac{kT}{q}\ln\left(\frac{-8A_n}{\delta(1+A_n r^2)^2}\right)]}{dr}\Big|_{r=R} \quad (6.8\text{ a})$$

or, $$\frac{q(V_{gate} - V_{x,n})}{kT} - \ln\left(\frac{8}{\delta R^2}\right) = n(1-\alpha) - \ln\alpha^2 + \gamma(\frac{1-\alpha}{\alpha}) \quad (6.8b)$$

or, $$\ln(1-\alpha) - \ln\alpha^2 + \gamma(\frac{1-\alpha}{\alpha}) + \ln\left(\frac{8}{\delta R^2}\right) = \frac{q(V_{gate} - V_{x,n})}{kT} \quad (6.8c)$$

Similarly for holes we obtain,

$$\ln(1-\alpha) - \ln\alpha^2 + \gamma(\frac{1-\alpha}{\alpha}) + \ln\left(\frac{8}{\delta R^2}\right) = \frac{q(V_{x,p} - V_{gate})}{kT} \quad (6.8d)$$

where, x denotes the applied bias dependent quasi fermi level with x_{min}=0 and x_{max}= the maximum source-drain voltage applied. $\gamma=4\varepsilon_{Si}/C_{ox}R$ and $\alpha\equiv1+AR^2$ ($A=A_n$ for electrons and A_p for holes) is a constant in term of nanowire radius and can be solved from Eq. (6.8) as a function of $V_{x,n(p)}$ for a particular V_{gate}.

Now, differentiating Eq. (6.5) and substituting r=R we get,

$$\frac{d\psi}{dr}\Big|_{r=R} = 4\frac{kT}{q}\left(\frac{1-\alpha}{\alpha}\right) \quad (6.9)$$

Substituting the above relation obtained in Eq. (6.9) in Eq. (6.4) we obtain charge/area as,

$$Q = \left(\frac{4\varepsilon_{Si}}{R}\right)\left(\frac{kT}{q}\right)\left(\frac{1-\alpha}{\alpha}\right) \quad (6.10)$$

If we assume Q′=(4ε$_{Si}$/R)(kT/q), we can write Q=Q′(1-α)/α. In other words, α=Q′/Q′+Q. Now, putting this value of α in Eq. (6.8) we obtained for electrons,

$$\ln\left[\frac{8(Q_n^2+Q_nQ')}{\delta R^2 Q'^2}\right]+\frac{q}{kT}\frac{Q_n}{C_{ox}}=\frac{q(V_{gate}-V_{x,n})}{kT} \tag{6.11}$$

and for holes,

$$\ln\left[\frac{8(Q_p^2+Q_pQ')}{\delta R^2 Q'^2}\right]+\frac{q}{kT}\frac{Q_p}{C_{ox}}=\frac{q(V_{x,p}-V_{gate})}{kT} \tag{6.12}$$

where Q_n and Q_p are the carrier densities of electrons and holes. But it is only possible to solve (6.11) and (6.12) numerically as they do not have any exact analytical solution. But an approximate explicit expression of Q which agrees very well with the numerical solutions of (6.11) and (6.12) both at sub and post threshold without any fitting parameters is written as,

$$Q=C_{ox}\left(-\frac{2C_{ox}V_{th}^2}{Q'}+\sqrt{\left(\frac{2C_{ox}V_{th}^2}{Q'}\right)^2 4V_t^2\ln^2\left|\left(\frac{V_{gate}-V_t+\Delta V_t-V_x}{2V_t}\right)\right|}\right) \tag{6.13}$$

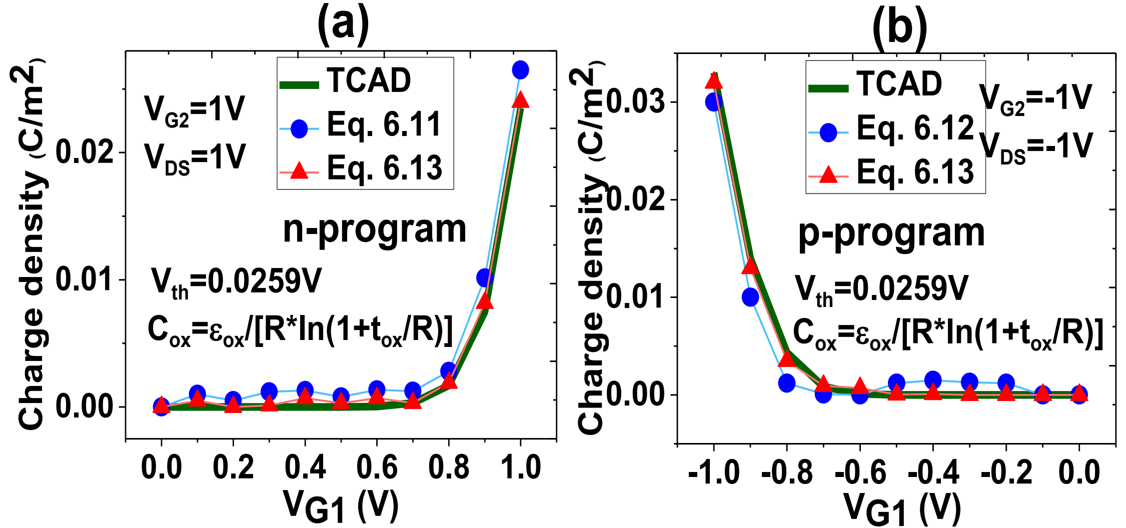


Figure. 6.3. (a) Carrier density for n-program (b) Carrier density for p-program.

where, $Q=Q_n(Q_p)$ and $V_x=V_{x,n}$ ($V_{x,p}$) for electrons (holes), V_{th} is the thermal voltage and $\Delta V_t=2C_{ox}V_{th}^2/Q'$ above V_t and $\Delta V_t=(2C_{ox}V_{th}^2/Q'^2)(C_{ox}(V_{gate}-\varphi_{gate}-(kT/q)\ln(8/\delta R^2)-V_x))$below V_t, φ_{gate} being the work function of gate metal. As it can be seen from Fig. 6.3 that although Eq. (6.11) and (6.12) are slightly less accurate for calculating the carrier densities but the unified explicit expression of (6.13) agrees very well with the numerical TCAD solution.

An overall expression for the channel surface potential ψ_{so} (r) valid for all bias conditions is now written from Eq. (6.5) and (6.6) using complementary smoothing functions such that the regional solutions approach zero outside their regions of validity,

$$\psi_{so}(r) = \frac{(1+\tanh\beta)}{2}\psi_{s,n}(r) + \frac{(1-\tanh\beta)}{2}\psi_{s,p}(r) \tag{6.14}$$

where, $\beta=q(2V_{gate}-V_n-V_p)/2kT$. Please note for n-program, tanh (β) tends to 1 since β tends to infinity owing to a positive V_{gate} which is much greater than the quasi fermi potentials and so the second part of the summation actually cancels out leaving only $\psi_{s,n}$ (r). Similarly, for p-program tanh (β) tends to -1 since β tends to minus infinity. Now, to have a complete surface potential model for the proposed RFET. We solve for the quasi 2-D surface potentials (independent of r) near the $NiSi_2$/Si Schottky junctions [77] apart from the long channel surface potential ψ_{so} of (6.14). To do this the necessary boundary conditions required are,

$$\psi_S(y=0) = V_{bi} + V_{source}, \psi_S(y=L) = V_{bi} + V_{drain} \tag{6.15}$$

Where, V_{bi} is the built in voltage of $NiSi_2$/Si junction and V_{source}, V_{drain} are source and drain voltages respectively.

If $\xi_{s,s}$ (y, r) and $\xi_{s,d}$ (y, r) represents the bias dependent potential profiles at the source and drain ends of the device, we can write using [77],

$$\xi_{s,s}(y,r) = \frac{\sinh((L-y)/\lambda_s)}{\sinh\frac{L}{\lambda_s}}(V_{bi} + V_{source} - \psi_{so}(r)) \tag{6.16}$$

$$\xi_{s,d}(y,r) = \frac{\sinh(y/\lambda_s)}{\sinh\frac{L}{\lambda_s}}(V_{bi} + V_{drain} - \psi_{so}(r)) \tag{6.17}$$

where, length of each metallic gate is defined as L, λ_S is the characteristic length of the device and is given as $\sqrt{\varepsilon_{Si}R/2C_{ox}}$, V_{bi} is the built-in potential due to the source (drain) to channel work function difference

The overall expression for surface potential ψ_S (r, y) is thereby obtained as,

$$\psi_s(r,y) = \psi_{so}(r) + \xi_{s,s}(y,r) + \xi_{s,d}(y,r) \tag{6.18}$$

6.2.2 Drain Current Model

To model the drain current, the Schottky contacts and the channel are modeled separately. We start with the calculation of tunneling probability at the S/D Schottky barriers. To do this a similar approach as given in [78] is followed by us. The source side Schottky barrier between the fermi level of the metal ($NiSi_2$) and the conduction band of the nanowire is replaced by an effective Schottky barrier height $\psi_{SB,source}^{eff}$. If the energy at some point is above this barrier height, then the barrier is assumed to be lower than a fitting parameter d_{tunnel}, and the carriers thereby can reach the channel through thermionic emission and the tunneling probability in this case is assumed to be unity. On the other hand, the carriers having energy below the effective barrier height are reflected and hence the tunneling probability for them is zero. The same procedure is applied for effective drain side Schottky barrier height $\psi_{SB,drain}^{eff}$. Now, to find out the effective Schottky barrier heights for electrons and holes we solve (6.18) for $y=d_{tunnel}$ and $y=L-d_{tunnel}$ and obtain,

$$\psi_{SB,n}^{eff} = \left(1 - e^{-\frac{d_{tunnel}}{\lambda_s}}\right)(\psi_{SB,n} - \psi_{SS,S} + V_{bi} + V_{source}) \tag{6.19}$$

$$\psi_{SB,p}^{eff} = \left(1 - e^{-\frac{d_{tunnel}}{\lambda_s}}\right)(\psi_{SB,p} - V_{bi} - V_{drain} + \psi_{SD,D}) \tag{6.20}$$

where, $\Psi_{SB,n}$ and $\Psi_{SB,p}$ are the Schottky barrier heights for electrons and holes and are equal to $\varphi_{Schottky}-\chi$ and $\chi+ E_g/q- \varphi_{Schottky}$ respectively.

The Schottky-diode current voltage relationship is used to calculate the BTBT current for electrons and hole transport across the Schottky barriers considering S as the contact area between source (drain) electrode and the channel and is approximately equal to πR^2, R being the nanowire radius, m^*_n and m^*_p are the effective tunneling masses for electrons and holes, h is the Planck constant and T is the absolute temperature,

$$I_{BTBT,n} = S\frac{4\pi m_n^* k^2 q}{h^3} T^2 \exp^{\left(-\frac{q\psi_{SB,n}^{eff}}{kT}\right)} \tag{6.21}$$

$$I_{BTBT,p} = S\frac{4\pi m_p^* k^2 q}{h^3} T^2 e^{\left(-\frac{q\psi_{SB,p}^{eff}}{kT}\right)} \tag{6.22}$$

Now, in the channel region of the RFET the current is governed by drift-diffusion transport and to find this current the method discussed in [79] is followed by us,

$$I_{DD,n} = \mu \frac{2\pi R}{L_{channel}} \int_{0}^{V_{drain}} Q_n(V_n) dV_n \tag{6.23}$$

Now, differentiating (6.11) considering $V_{x,n}$ as a variable we get,

$$dV_n = \frac{dQ_n}{C_{ox}} + \frac{kT}{q} + \left(\frac{dQ_n}{Q_n} + \frac{dQ_n}{Q_n + Q'} \right) \tag{6.24}$$

writing dV_n as a function of Q_n and dQ_n in (6.23) and integrating between charge at source, $Q_{S,n}$ and charge at drain, $Q_{D,n}$ we get,

$$I_{DD,n} = \mu_n \frac{2\pi R}{L_{channel}} \left[2\frac{kT}{q}\left(Q_{S,n} - Q_{D,n}\right) + \frac{Q_{S,n}^2 - Q_{D,n}^2}{2C_{ox}} + \frac{kT}{q} Q' \ln\left[\frac{Q_{D,n} + Q'}{Q_{S,n} + Q'} \right] \right] \tag{6.25}$$

Following similar approach for holes we obtain,

$$I_{DD,p} = \mu_p \frac{2\pi R}{L_{channel}} \left[2\frac{kT}{q}\left(Q_{S,p} - Q_{D,p}\right) + \frac{Q_{S,p}^2 - Q_{D,p}^2}{2C_{ox}} + \frac{kT}{q} Q' \ln\left[\frac{Q_{D,p} + Q'}{Q_{S,p} + Q'} \right] \right] \tag{6.26}$$

We solve for $Q_{S,n}$, $Q_{D,n}$, $Q_{S,p}$ and $Q_{D,p}$ from (6.11) and (6.12) by putting V_{gate}=V_{G1} along with $V_{x,n(p)}$=$V_{x,n(p),SS,S}$ at source/source side spacer interface and $V_{x,n(p)}$=$V_{x,n(p),SD,D}$ at drain/drain side spacer interface.

Applying current continuity in the channel, we equate I_{BTBT} and I_{DD} for electrons as well as holes (neglecting excess carrier generation and recombination at the junctions as well as in the nanowire active region). We assume $V_{x,n,SS,S}$= $V_{x,n,CG}$ and $V_{x,p,SS,D}$= $V_{x,p,CG}$ since the quasi fermi potentials drops mostly at the drain end for any tunneling based FET. When the carriers reach the other end of the nanowire, the voltage drop between source/drain and source/drain spacers should also be taken into account and (6.21) and (6.22) are correspondingly modeled as,

$$I_n = S\frac{4\pi m_n^* k^2 q}{h^3} T^2 \left(e^{\frac{q\left(V_{drain} - V_{x,n,SD,D} - \psi_{SB,n}\right)}{kT}} - e^{\left(-\frac{q\psi_{SB,n}}{kT}\right)} \right)$$

$$= S\frac{4\pi m_n^* k^2 q}{h^3} T^2 e^{(-\frac{q\psi_{SB,n}}{kT})}\left(e^{\frac{q\left(V_{drain}-V_{x,n,SD,D}-\psi_{SB,n}\right)}{kT}}-1\right) \quad (6.27)$$

$$I_p = S\frac{4\pi m_p^* k^2 q}{h^3} T^2\left(e^{\frac{q\left(V_{x,p,SS,S}-V_{source}-\psi_{SB,p}\right)}{kT}}-e^{(-\frac{q\psi_{SB,p}}{kT})}\right)$$

$$= S\frac{4\pi m_p^* k^2 q}{h^3} T^2 e^{(-\frac{q\psi_{SB,p}}{kT})}\left(e^{\frac{q\left(V_{x,p,SS,S}-V_{source}-\psi_{SB,p}\right)}{kT}}-1\right) \quad (6.28)$$

By combining the drain current expressions in (6.21), (6.22), (6.27) and (6.28) the values of quasi-fermi potentials $V_{x,n(p)}=V_{x,n(p),SS,S}$ and $V_{x,n(p)}=V_{x,n(p),SD,D}$ are obtained as follows,

$$V_{x,n,SD,D} = V_{drain} - \psi_{SB,n} + \psi_{SB,n}^{eff} \quad (6.29)$$

$$V_{x,p,SS,S} = V_{source} + \psi_{SB,p} - \psi_{SB,p}^{eff} \quad (6.30)$$

Putting the values of A_n, A_p, $V_{x,n,SD,D}$ and $V_{x,p,SS,S}$ from (6.7), (6.29) and (6.30) in (6.5) and (6.6) the channel surface potentials [thereby the long channel (6.14) and overall surface potential (6.18)] are obtained as follows,

$$\psi_{S,n}(r) = V_{drain} - \psi_{SB,n} + \psi_{SB,n}^{eff} + \frac{kT}{q}\ln\left(\frac{\left(\frac{8Q_n}{(Q_n+Q')R^2}\right)}{\frac{q^2 n_i}{kT\varepsilon_{Si}}\left(1-\frac{Q_n r^2}{Q_n+Q'}\right)^2}\right) \quad (6.31)$$

$$\psi_{S,p}(r) = V_{source} + \psi_{SB,p} - \psi_{SB,p}^{eff} + \frac{kT}{q}\ln\left(\frac{\left(\frac{8Q_p}{(Q_p+Q')R^2}\right)}{\frac{q^2 n_i}{kT\varepsilon_{Si}}\left(1-\frac{Q_p r^2}{Q_p+Q'}\right)^2}\right) \quad (6.32)$$

6.3 Model Validation

To verify the models developed for surface potential and drain current in section II the RFET device structure with high-κ S/D spacers as shown in Fig. 6.1 is simulated using 3-D simulations by *Sentaurus TCAD* Version 13.12.

We have used Philips unified mobility model (PhuMob) to consider mobility degradation due to carrier-carrier scattering mechanisms along with a field dependent mobility model with high field corrections to account for velocity saturation of carriers at high electric fields. The recombination terms include the SRH (Shockley-Read-Hall) expression (to account for recombination via traps), recombination via band-to- band tunneling and Auger effects. In the simulation of RFETs, the choice of tunneling model plays a vital role. A non local tunneling model is used to consider the availability of states across the $NiSi_2$/Si Schottky interface, otherwise if a local tunneling model is used it may result in a nonzero tunneling current at zero drain voltage because this model integrates the BTBT rate based on the electric field only. Electron and hole tunneling masses are chosen as 0.3 m_o and 0.2 m_o respectively [61]. First of all we verify the electrostatic potential model derived as a numerical solution to Poisson's equation (1). Fig. 6.4 (a) and (b) show the potential distribution along the radial direction with given values of quasi fermi potentials for n- and p-programs at $|V_{G1}|$=0.5 V, 1 V and both $|V_{DS}|$ and $|V_{G2}|$ fixed at 1 V respectively. As can be observed from the figures, the TCAD simulations match well with the model results given by (6.5) and (6.6). It is interesting to note from Fig. 6.4 (a) that there is a high electric field (non zero slope in the potential curve) at the drain end of the device for lower V_{G1} (0.5 V) because the device is relatively less n-type in this case and most of the electrons tunnel from source to drain. Similar observations can also be seen from Fig. 6.4 (b) in case of a p-FET. The surface potential distribution obtained from the simulation along the channel for both n- and p-type configurations is shown in Fig. 6.4 (c) and (d) which shows good agreement with the model (6.18). It may be noted that in our modeling approach we have divided the device into several regions and considered the quasi fermi potentials within each region as constant.

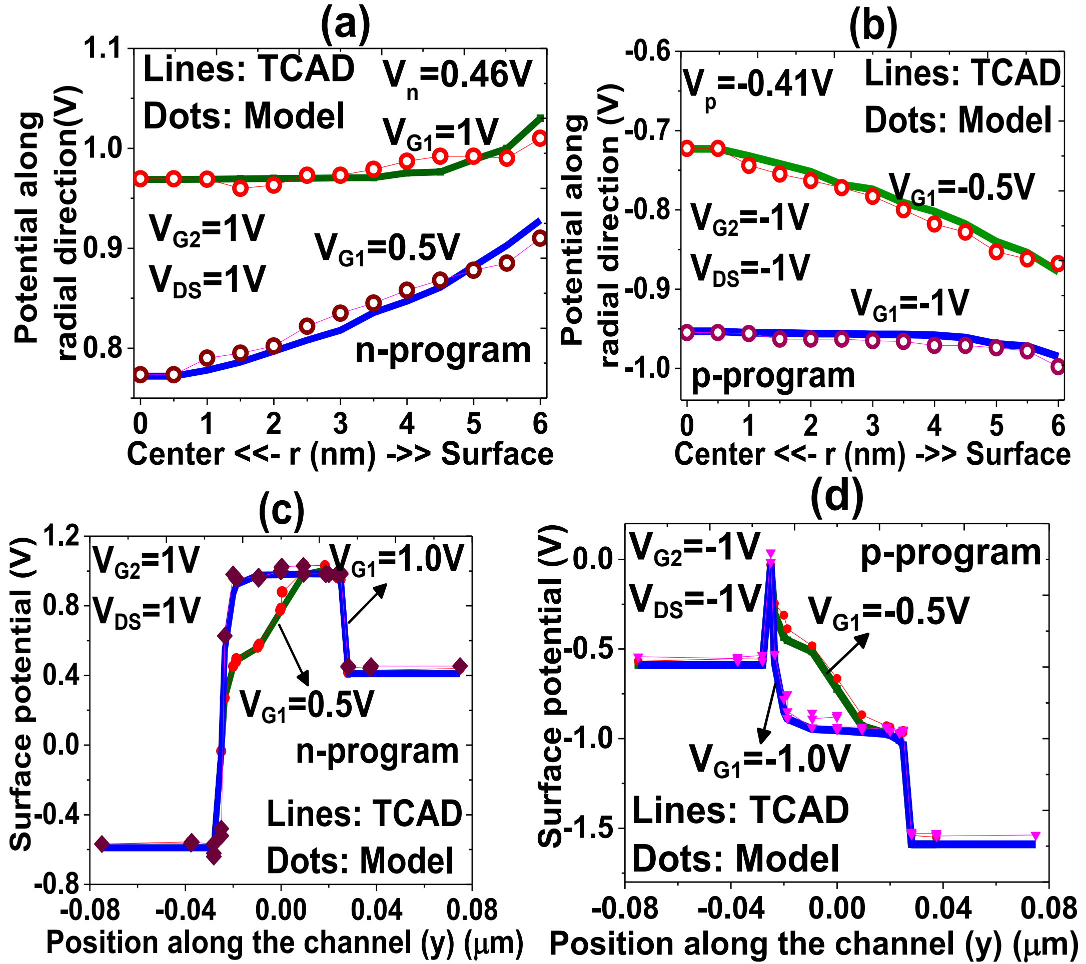


Figure. 6.4. The predicted (a) Potential along radial direction for n-program (taking cutline at y=L) (b) Potential along radial direction for p-program (taking cutline at y=L) (c) Surface potential for n-program (d) Surface potential for p-program (lines: TCAD simulation, dots: model).

.

But when control gate voltage V_{G1} is changed from 0.5 V to 1 V, ψ_{G1SS}, ψ_{G2SD} and ψ_{G1G2} also changes due to a slight change in the quasi fermi potentials which is reflected from Fig. 6.4 (c) and (d). It is observed that the potential drop across the tunneling junction is almost negligible and can be assumed to be constant indicating a high concentration of mobile charge carriers across these regions. A much steeper profile in the potential distribution (high electric field) is observed for both n- and p-programs in the nanowire channel region for lower control gate voltage (V_{G1}=|0.5 V)| as compared to the higher one which is mainly because of the gradient in applied potential between control and polarity gates.

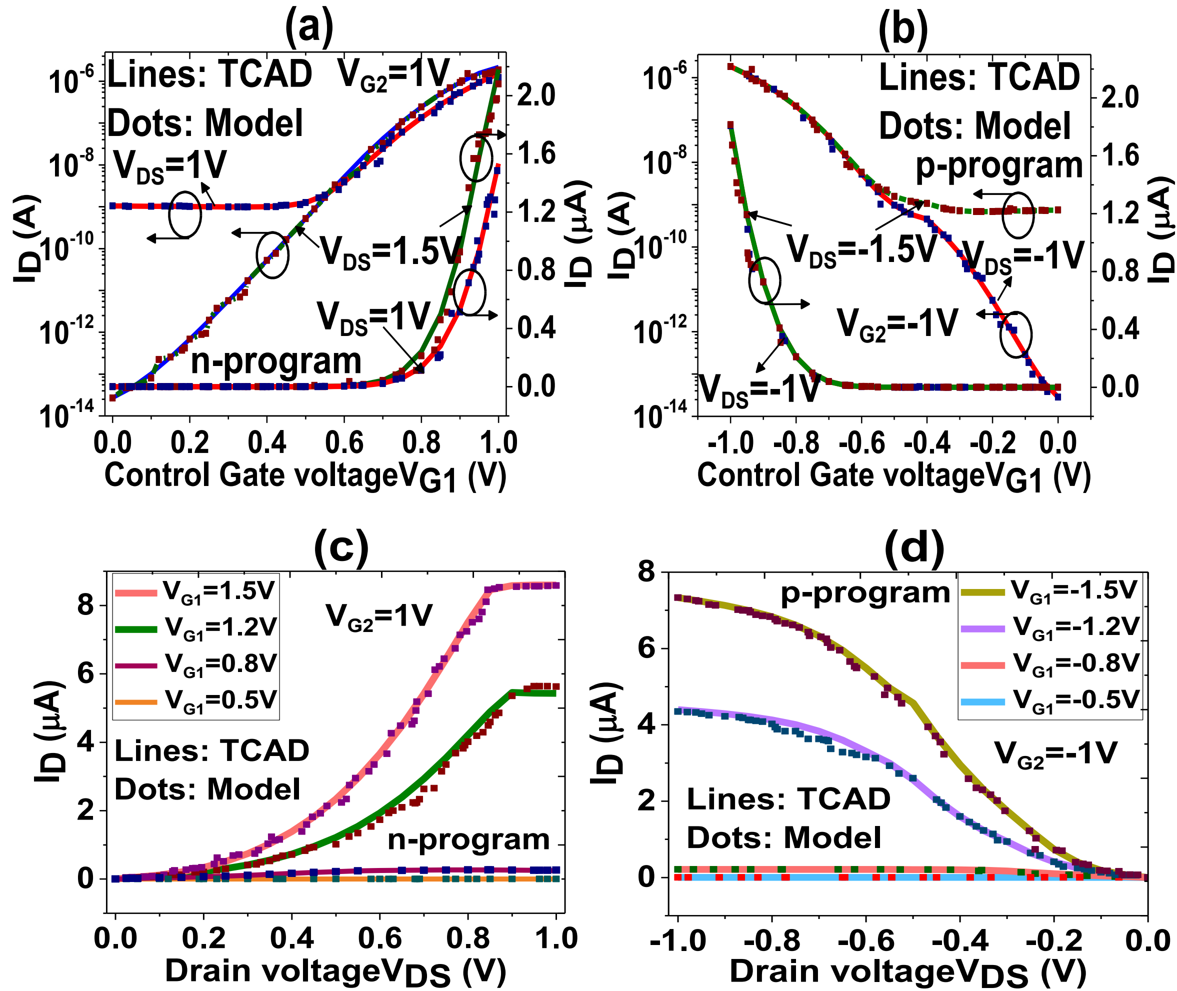


Figure. 6.5. (a) Drain characteristics for varying V_{CG} at a fixed V_{PG} for n program (b) Drain characteristics for varying V_{CG} at a fixed V_{PG} for p-program (c) Drain characteristics for varying V_{DS} at a fixed V_{CG} for n program (d) Drain characteristics for varying V_{DS} at a fixed V_{CG} for p program (lines: TCAD simulation, dots: model).

Fig. 6.5 (a) and (b) show the model results for log as well as linear I_D-V_{G1} curves for the proposed RFET with L_{ch}=50 nm and L_G=12 nm. V_{th} for n (p-FET) is taken as 0.45 V (-0.463 V). The model accurately predicts the drain current for the entire range of V_{G1} and hence can be used for finding the drain current and SS of a RFET. A small mismatch in the I_D-V_{G1} curves above the threshold voltage is mainly because in our calculations we have considered a simple assumption of the device characteristic length λ_S which does not perfectly capture the effect of induced charge carriers. To reduce this discrepancy one can consider the use of a

unified λ_S at turn–on as done in [77]. Fig. 6.5 (c) and (d) shows the output characteristics in linear scale (I_D-V_{DS} curves) for the RFET device under consideration. Over a large range of V_{DS} the current model is in good agreement with the simulations for both n- and p-program. For very small values of drain voltage, the simulated drain current slightly deviates from the model predictions. This is because in this work the saturation drain current is considered to be dominated mainly by the Schottky barriers and the model is less accurate in predicting the average electric field E_{avg} at very small drain biases and further work needs to be done on this.

A comparison between the modeled and TCAD simulated I_d-V_{G1} characteristics for varying channel lengths viz. L=40 nm, 44 nm, 48 nm, 50 nm, 60 nm, 70 nm and 80 nm for both n- and p-programs (on-state) of the proposed RFET is shown in Fig. 6.6 (a) and (b). It may be noted that the inter gate separation (d_{G1G2}) becomes as small as 6 nm at a nanowire length of 40 nm below which there are huge convergence issues in TCAD and as such the lowest nanowire length for which the validity of SCE modeling shown in this paper is 40 nm. As expected the drain current increases for both configurations with length of the channel being scaled down. The model accurately predicts the device drain current for the entire range of applied control gate voltage. Moreover, for a complete validation of the proposed model we have also compared the channel length dependences on subthreshold swing, DIBL and threshold voltage roll-off as shown in Fig. 6.6 (c), (d) and (e). We would like to mention the fact that evaluation of threshold voltage is done using a constant current criterion ($I_d=10^{-7}A\times W/L$). To calculate V_{th} roll off, the threshold voltage in case of the highest channel length (here 80 nm) is taken as V_{th0} and it is subtracted from the threshold voltage for that channel length where it needs to be calculated. As can be observed from the figures all the short channel parameters improve with increasing L and the modeled predicted results

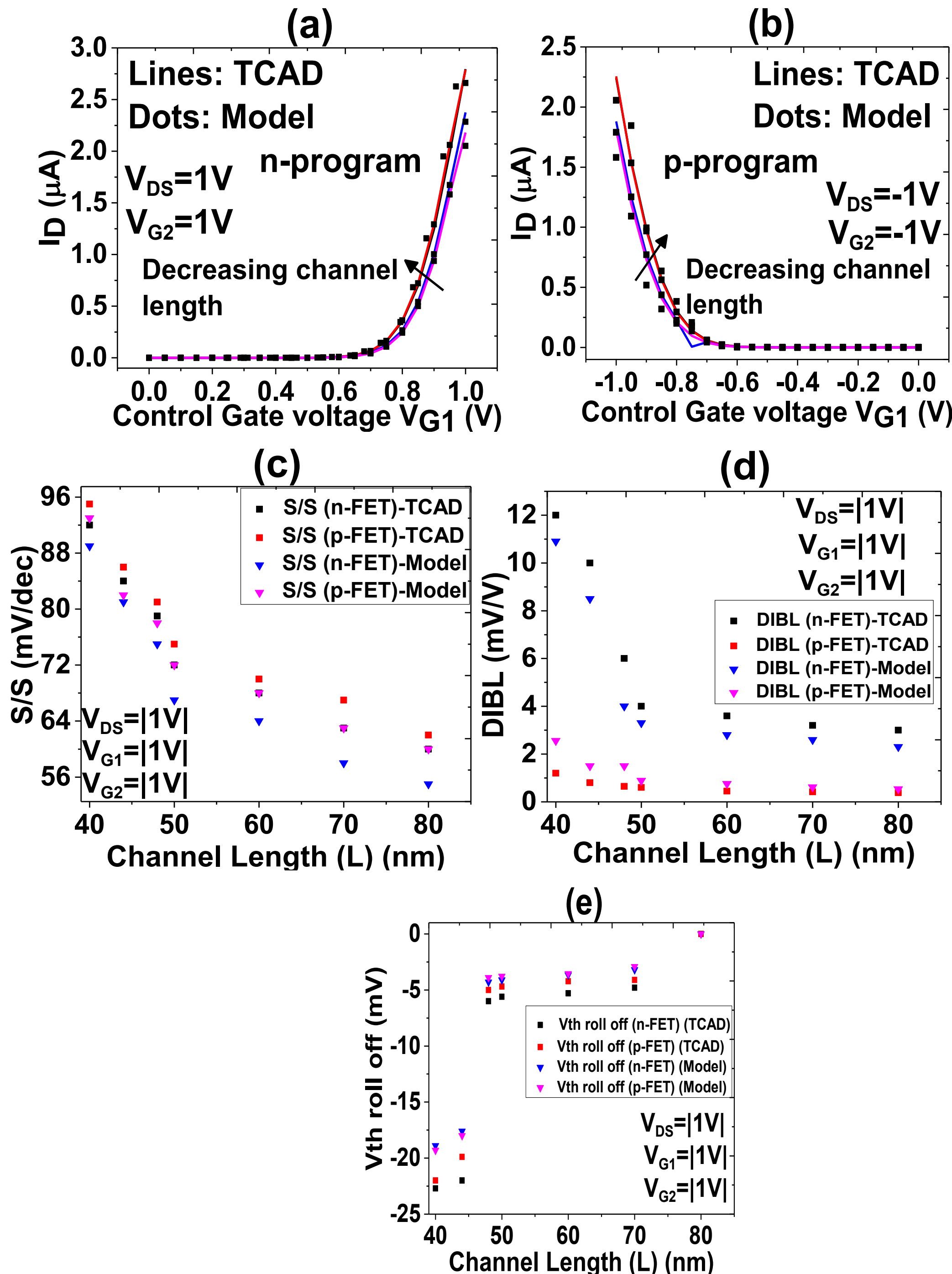


Figure. 6.6. (a) Variation of I_d vs. V_{G1} for n-FET for various channel lengths (Lines-TCAD, Dots-Model) (b) Variation of I_d vs. V_{G1} for p-FET for various channel lengths (Lines-TCAD, Dots-Model) (c) Variation of S/S with channel length for both n- and p-FET (Lines-TCAD, Dots-Model) (d) Variation of DIBL with channel length for both n- and p-FET (Lines-TCAD, Dots-Model) (e) Variation of V_{th} roll off with channel length for both n- and p-FET (Lines-TCAD, Dots-Model).

resemble quite closely with that of the simulated ones for both configurations. The slight discrepancy between the model predicted and simulated on state BTBT current and thereby the SCE's can be further reduced by adjusting the tunneling parameters and calculating the carrier densities at the channel and source (drain)/spacer interface more accurately.

6.4 Verilog-A Model Development

To the best of the author's knowledge, we have developed a Verilog-A model for the proposed RFET. We have used a silicon nanowire of channel length 680nm and diameter 20nm at its core as shown in Fig. 6.7. Source and drain regions are formed by nickel silicide which is present at both ends of the wire and two Schottky junctions are formed at both the interfaces of silicon and nickel silicide. 10nm thick shell of SiO_2 surrounds the nanowire and major portion of nickel silicide. Gating near the junction controls the injection of holes and electrons from source or drain and ungated region does not limit conductance.

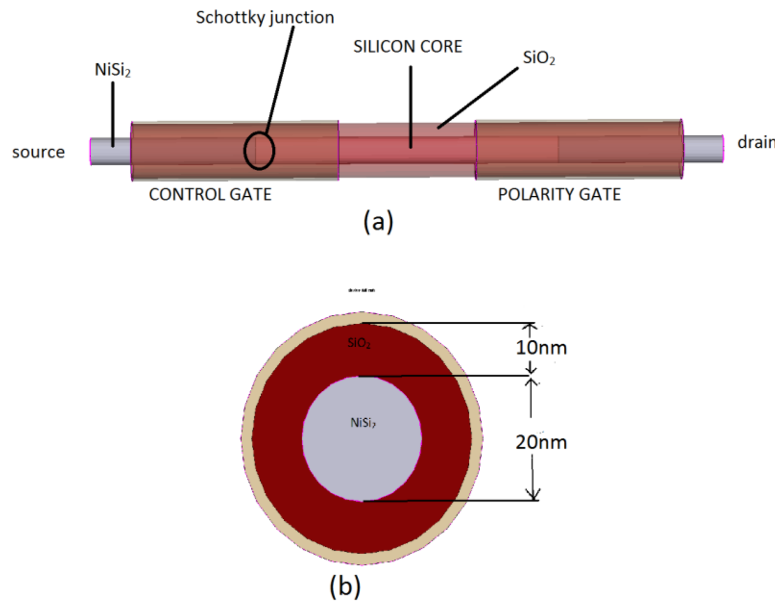


Figure. 6.7. a) 3-D isometric view of dual-gate SiNWFET b) Cross-sectional view.

Current and capacitance characteristics of this device are used to make an inverter in this work. The device under observation is first made in TCAD. But simulations in TCAD

are very time consuming are many a times have convergence issues. To avoid these problems, look-up table based Verilog-A model is used. Verilog-A model of the device mimics its behavior using equations derived from TCAD data. It is up to user to what extent he wants to represent the device's complexity in Verilog-A model. Many a times, current and capacitance characteristics are enough to tell about static and transient behavior of the circuits made using the device. Similar approach has been used in this work. As already mentioned, Technology Aided Computer Design (TCAD) simulations are very time consuming and many a times have convergence issues. With spacer-based device also, convergence issues were there for simulation of an inverter. Thus, Verilog-A model which captures very basic nature of the device is used instead of TCAD [Fig. 6.8]. For doing transient, dc and ac analysis, current and capacitance characteristics are sufficient. For this device, three-dimensional look-up tables with $I_{ds}(V_{pgs}, V_{cgs}, V_{ds})$, $C_{pgs}(V_{pgs}, V_{cgs}, V_{ds})$, $C_{pgd}(V_{pgs}, V_{cgs}, V_{ds})$, $C_{cgd}(V_{pgs}, V_{cgs}, V_{ds})$, $C_{cgs}(V_{pgs}, V_{cgs}, V_{ds})$ characteristics are required to make the Verilog-A model, which is shown in Fig. 6.8. C_{cgs} and C_{cgd} denote the capacitance between control gate and source, drain and C_{pgs}, C_{pgd} denotes the capacitance between polarity gate and source, drain. C_{gg} is the capacitance between the two gates.

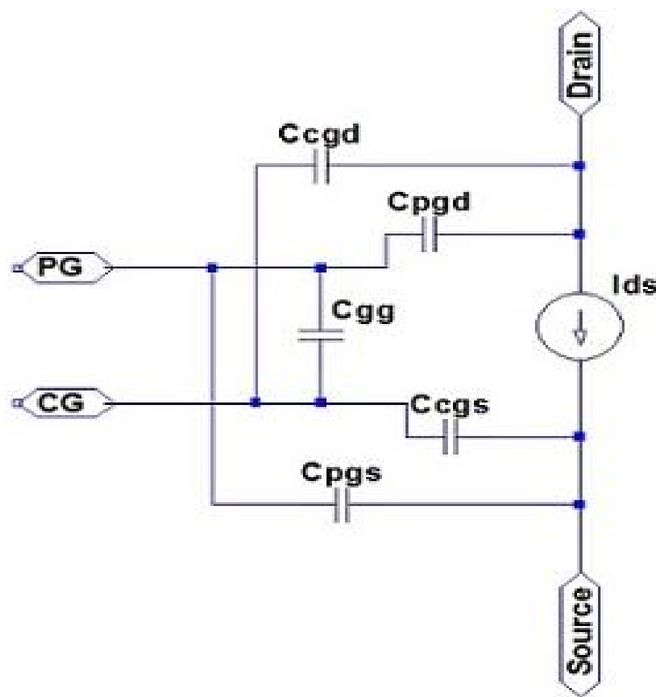


Figure. 6.8. Verliog-A model of the device.

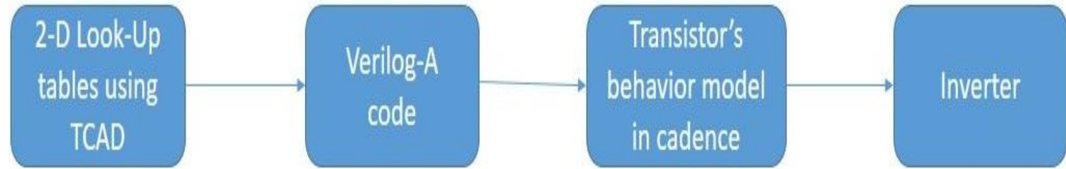


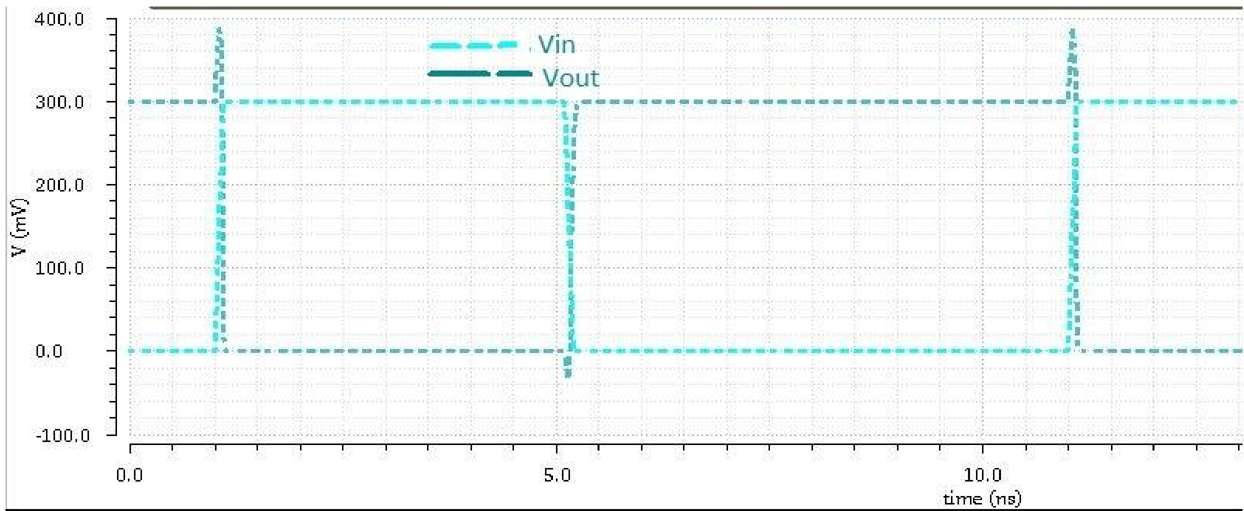
Figure. 6.9. Complete flow from data extraction to making an inverter.

For an inverter only two-dimensional look-up tables (with polarity gate at a constant value) are sufficient. 2D look-up tables are extracted from 3D TCAD simulations. Gate voltage is varied from 0 to 2V for nFET and -2V to 0V for pFET with an increment of 0.02V and drain voltage is varied from -2V to 2V for both nFET and pFET with an increment of 0.02V. They are directly called in the Verilog-A code and the data is linearly interpolated and extrapolated in the code. The code is included in cadence virtuoso and thus we have black boxes which mimic the behavior of the device. An inverter is made using these black boxes in cadence and dc and transient simulations are carried out for it. The complete flow from data extraction to simulation is shown in Fig. 6.9. Prior to including our device's Verilog-A code, the flow is tested on Verilog-A model of Tunnel Field Effect Transistors. Inverter circuit, results of DC and transient analysis for TFET are shown in Fig. 6.10. The t_{PHL}, t_{PLH}, t_P as calculated from Fig. 6.10 (a) are 0.256 ns, 0.278 ns and 0.267 ns respectively. High level noise margin (NMH) as obtained from Fig. 6.10 (b) is 158 mV and low level noise margin (NML) is 154 mV.

6.4.1 Inverter simulation in cadence

Initially, only nFET characteristics were used and pFET characteristics were assumed to be mirror image of them. Fig. 6.11 shows family of curves for nFET and pFET (here mirror image of nFET characteristics) for different values of gate voltage. The drain voltage at which two curves corresponding to same input voltage intersect gives the output voltage corresponding to that input voltage. So, pFET characteristics were used instead of nFET. I_d-V_d curves for pFET are shown in Fig. 6.12 and they are similar to those of MOSFET. Fig. 6.13 shows Voltage Transfer Characteristics for this inverter for varying V_{DD} (0.15 V, 0.17 V, 0.28 V, 0.35 V, 0.5 V, 0.55 V, 0.63 V, 0.78 V, 0.85 V, 1 V). The NMH and NML for V_{DD}=1V are 440 mV and 552 mV respectively. Due to insufficient experimental published

data we could not provide comparison of the inverter characteristics for the *underlap* RFET device with and without spacers. But we anticipate since the spacer based RFET device shows improvements in terms of electrical performance parameters such as I_{ON}, S/S, I_{ON}/I_{OFF} as shown by us in the previous chapters, the logic performance of the spacer based RFET will also get improved.



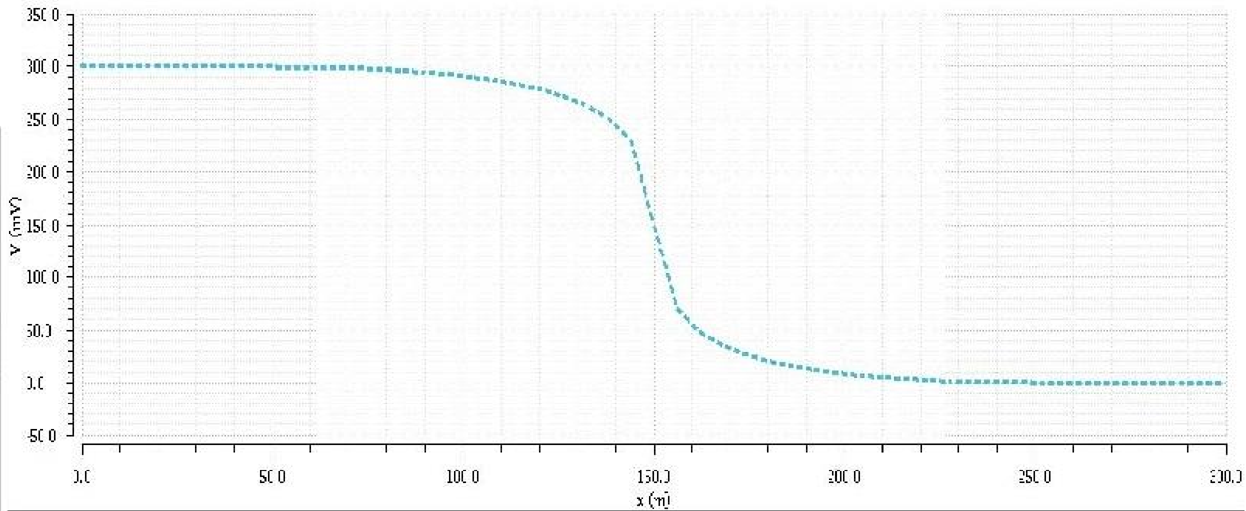


Figure. 6.10. a) Transient analysis b) Voltage Transfer Characteristics for inverter made using TFET.

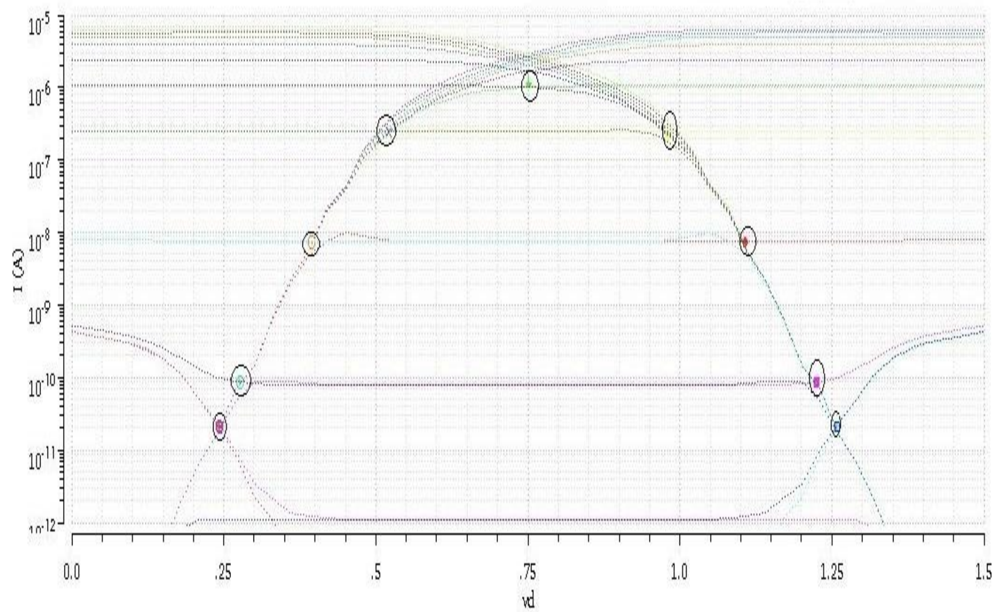


Figure. 6.11. Family of curves for nFET and its mirror image (here pFET).

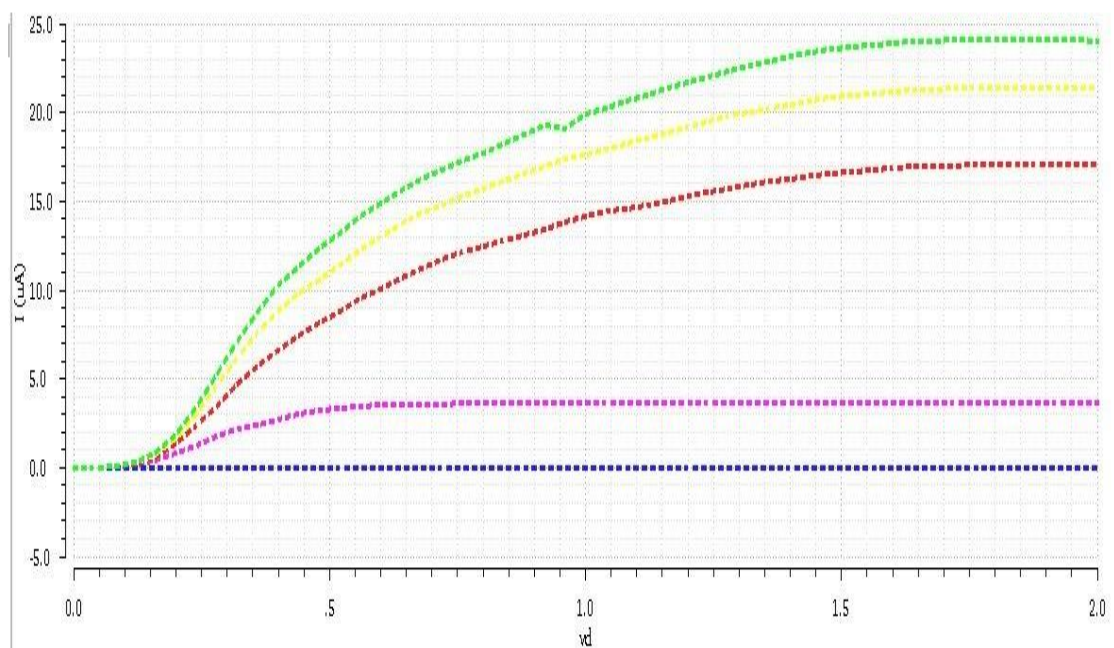


Figure. 6.12. I_d-V_d characteristics of p-programmed transistor (mirrored about x and y axis).

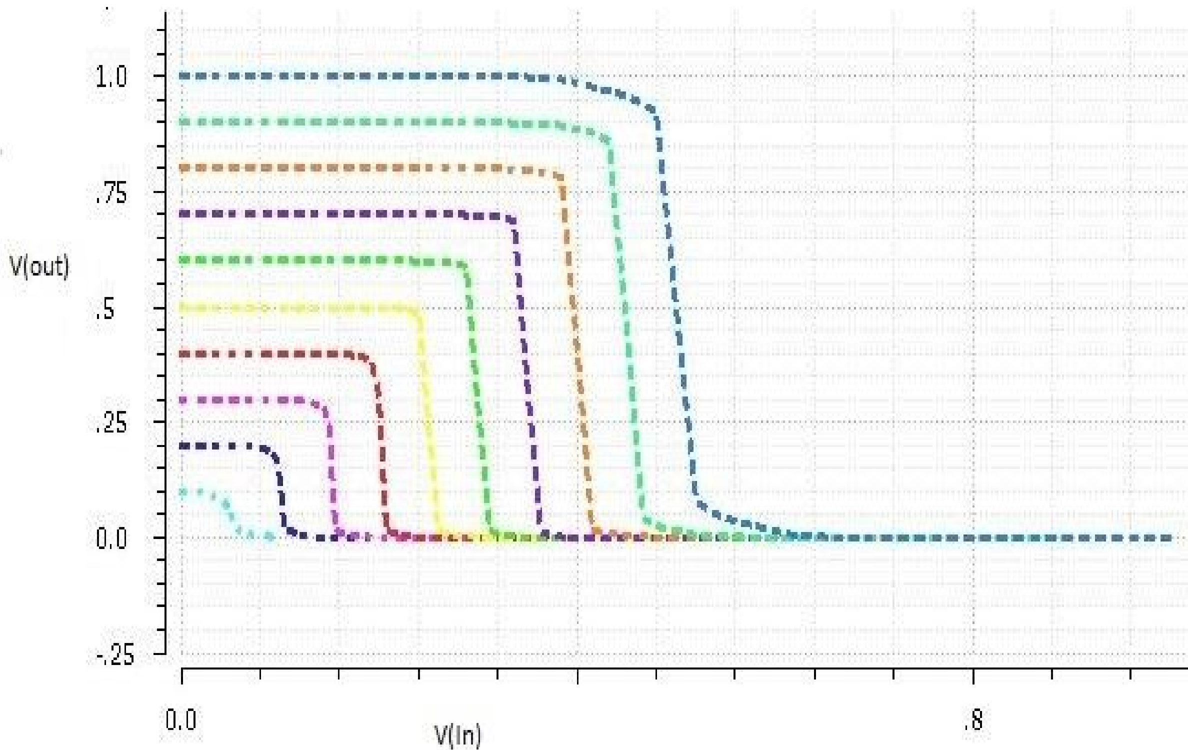


Figure. 6.13. Voltage Transfer Characteristics of inverter obtained using pFET characteristics for various V_{DD}.

After DC analysis, transient analysis was done with nFET characteristics only and it had convergence problems. After doing intense investigation in cadence, it was found that capacitances extracted were causing unexpected contribution to currents. Moreover it was observed that admittance matrix obtained by ac analysis in TCAD was not symmetric. Considering the I_d-V_d characteristics of nFET and capacitance characteristics of nFET and pFET, a strong need was felt to make some changes in device's meshing strategy and Physics models applied while doing device simulation.

6.5 Summary

As a summary we have developed a compact physics based model for the surface potential and drain current of a spacer based DG-RFET. In this model we have included the effects of drain voltage, nanowire radius, temperature and Schottky barrier height. The model uses a carrier charge density expression to find the surface potential and the drain current of the proposed RFET. To find out the values of quasi fermi potentials for electrons and holes

the current continuity equation is rigorously solved for various regions of the device. The results of our model are compared with numerical TCAD simulations and calibrated with experimental results. It may be pointed that for very low drain biases our model results in slight mismatch with the simulations. So, further research needs to be performed to refine the models in the low current regime. In order to further improve the accuracy of the derived surface potential and drain current, one can integrate complex electrostatics related to Schottky junctions and more advanced physical phenomenon associated with silicon nanowire in this proposed framework.

Verilog-A model has also been created and successfully used in cadence. But, poor I_d-V_d characteristics of n-programmed transistor gave poor Voltage Transfer Characteristics of inverter. I_d-V_d characteristics for pFET are similar to MOSFET and VTCs obtained with them are acceptable. Convergence problems are observed in transient analysis and it is possible to do transient analysis for t_{fall}/t_{rise} greater than 5ms, which was of no practical use.

Chapter 7

Conclusions and Future Scope

In this thesis, a detailed study on spacer based RFET, its advantages on the conventional *non-underlap* ambipolar structure, the core device physics behind all the performance enhancements, its temperature dependence, numerical modeling and possible advantages one may get form logic applications point of view is presented. The starting chapters of this thesis provides a comprehensive literature review on the work done till date on reconfigurable devices by various research groups across the globe and also introduces the S/D spacer based RFET concept and optimization of various design parameters to achieve best performance. The chapters at the end of the thesis depict the temperature dependence of the DC, RF and analog characterizes of the device. A compact physics based model was developed and how improvements obtained from spacer engineering may be highly useful in digital logic is also illustrated.

7.1 Conclusions

In the first phase of this work a novel reconfigurable device concept with high-κ S/D spacers was introduced. The Schottky junction between metal and semiconductor was kept outside the gate unlike to the existing *non-underlap* device configuration. It was found that the proposed device shows significant improvement in electrical characteristics like I_{ON}, I_{ON}/I_{OFF} ratio, S/S etc. The main reason behind these performance enhancements is that the S/D spacers were able to terminate the fringe electric field lines better in to the Schottky contact which increased the electric field and hence resulted in higher BTBT rate. Various vital device parameters such as spacer length, spacer material type, gate oxide thickness, gate length and integrate distance were optimized to achieve the best possible performance out of the proposed device.

To explore the device physics further and for a better understanding of all the performance gains the second phase of the work deals with the impact of gate/spacer channel underlap on the proposed device performance and also on proper gate oxide designs. It was observed that the gate/spacer channel underlap has a significant effect on the device drive current and also on the subthreshold current. It was shown that the I_{ON} and I_{ON}/I_{OFF} ratio of

the spacer based RFET can be improved manifold by appropriate designing of the gate-channel and spacer-channel underlap. Furthermore, it was observed that although using a higher-κ gate dielectric can result into larger capacitive coupling at a fixed gate oxide EOT, still it was found to improve intrinsic gate delay which may prove to be highly beneficial from circuit application point of view. It was also observed that, the improvement in I_{ON} achieved by scaling L_{Si}, L_g and $d_{nanowire}$ is quite less as compared to other devices which depends on tunneling for their on current generation.

In the third phase of the work a detailed investigation of the effect of temperature on the performance of the proposed RFET is carried out and compared it with other devices based on tunneling. It is found to have superior analog performance with increased values of g_m, g_m/I_d and A_v in the range temperature range as compared to SiGe and full silicon TFETs due to better BTBT dominated ON current and gate control over the channel. Intrinsic gate capacitances such as C_{GS}, C_{GD} and C_{GG} are also reduced many orders of magnitude, which results in a reduction in intrinsic delay (τ_d) as compared to GAA and HD GAA TFET. The RF/analog FOMs are also found to be immune to fluctuations in temperature for the entire range.

The fourth phase of the work discusses about a compact physics based model for the proposed DG-RFET. The effects of drain voltage, nanowire radius, temperature and Schottky barrier height are included in this model. The values of quasi fermi potentials for electrons and holes are found by solving the current continuity equation for various sub regions of the device. We have also compared the obtained results of our model with TCAD simulations. Finally, a Verilog-A model has been successfully created and used in cadence for the first time. The inverter characteristics can be further improved if more symmetric curved for both n- and p-FET can be achieved. But qualitatively better results for all logic applications are expected because of higher current drive than the *non-underlap* RFET device.

7.2 Major Contributions of this Work

A novel S/D spacer based *underlap* RFET architecture was proposed. Apart from improvement in ON current, 2 orders of magnitude reduction in off state leakage current and 64.1% improvement in subthreshold slope (S/S) for n-FET and 61.8% (40.9%) for n (p-FET) was observed as compared to experimental dual and tri gate ambipolar devices. The

improvement in drive current mainly resulted from the enhancement in electric field by 0.22 MV/cm (0.08 MV/cm) within the high-κ spacer material which in turn resulted in 35.2% (12.3%) up (down) shift in conduction band edge for n (p-FET).

The various physical parameters of the proposed device were optimized for best performance. 72.25 μA/μm increase in normalized I_{ON} for n-FET is seen with L_{sp} increase from 1nm to 2.2nm because of 33.33% up-shift in band edge thus reducing the minimum tunneling width. Increase in gate as well as spacer dielectric constant is not only found to boost the ON current and transconductance generation factor but also reduce S/S and V_t. This is mainly because of an increase in the fringe electric field lines near the Schottky junction at higher spacer κ. For HfO_2 spacers the current drive is found to improve from 105.35 μA/μm (41.45 μA /μm) to 202.3 μA/μm (620 μA/μm) for n (p-FET) with d_{G1G2} scaled down from 270nm to 4nm mainly because of a decrease in parasitic resistance at smaller gate separation but the performance gains is partially offset by higher capacitive coupling which may deteriorate circuit performance. Moreover, smaller values of gate/spacer channel underlap is found to improve the device performance drastically in terms of I_{ON}, I_{ON}/I_{OFF} ratio and intrinsic delay due to better electrostatic coupling between the Schottky junction and gate metal causing an enhancement in peak electric field and BTBT rate of electrons from source to drain.

Temperature dependence of the proposed device was portrayed and compared with other tunneling based devices. It was found that although the ON current of the proposed RFET increases with temperature, a slight decrease beyond 350K is mainly due to reduction in channel mobility at higher temperatures. The I_{OFF} increment in the proposed RFET with temperature is only two orders which is less than that of a TFET. The reduction in intrinsic capacitances for the device under consideration is mainly because of an intrinsic channel region and a negligible potential drop near the drain-channel junction. This ultimately results in reduction of τ by 10^{-3} s in comparison with GAA TFET and by 10^{-4} s for HD GAA TFET at V_{G1}=1V. Most of the analog and RF performance parameters of the proposed spacer based RFET is also found to be superior as compared to SiGe and Si abrupt TFET and are also quite immune to temperature fluctuations.

To model the drain current and surface potential of the proposed ambipolar device a charge density expression was first developed and the quasi fermi potentials of various sub

regions of the device were calculated by solving the current continuity equation. A single-piece-approximation of the long channel surface potential was developed by using the charge density expression and 2-D Poisson equation was rigorously solved in the silicon channel. Then it was added to the potential distribution at the Schottky contacts which was then solved by using a quasi-2D technique. The drain current was modeled by first finding the barrier height required for the carriers to overcome the maximum potential barrier induced in the channel by the control gate near the source end of the device which was then used to find out the current through the Schottky barriers. This was equated based on the principle of current continuity with the drift diffusion current in the channel which is obtained using the earlier derived charged density expression to generate a final expression for drain current. The validation of the developed model was done by comparing the obtained results with numerical 3D TCAD simulations and was found to match closely for various range of gate voltages. Finally, a Verilog-A model of this device was developed and logic simulations were performed by extracting various capacitances of the device using the TCAD tool. It is expected that due to the obtained performance enhancements the S/D spacers based DG RFET will also show a superior logic performance as compared to the conventional *non-underlap* RRFET architecture.

7.3 Future Scope

The fabrication of the proposed spacer based RFET and experimental verification of the results is the next most important thing to be done from futuristic point of view. It is essential that the results must be verified for the enhancements in performance presented here for S/D spacer based through TCAD simulations. Apart from this, other important problems that can be used for research in future are as follows:

1. More advanced designs with spacer based RFETs can be tried such as dual κ spacer, asymmetric spacer etc. .

2. Apart from silicon other materials like germanium and grapheme can also be utilized in designing future RFETs so that advantages related to all these semiconductors over silicon can also be availed.

3. More sophisticated compact model including all the advanced effects related to Schottky junctions can be developed.

4. Complex circuit applications related to spacer based RFETs can also be implemented.

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LIST OF PUBLICATIONS

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1. **A. Bhattacharjee**, and S. Dasgupta, "A Compact Physics-Based Surface Potential and Drain Current Model for an S/D Spacer Based DG-RFET," *IEEE Trans. Electron Devices,* vol. 65, no.2, pp. 448-455, Jan. 2018.

2. **A. Bhattacharjee**, M. Saikiran, and S. Dasgupta, "A First Insight to the Thermal Dependence of the DC, Analog and RF Performance of a S/D Spacer Engineered DG-Ambipolar FET," *IEEE Trans. Electron Devices,* vol. 64, no.10, pp. 4327-4334, Oct. 2017.

3. **A. Bhattacharjee**; S. Dasgupta, "Impact of Gate/Spacer-Channel Underlap, Gate Oxide EOT, and Scaling on the Device Characteristics of a DG-RFET," *IEEE Trans. Electron Devices,* vol. 64, no.8, pp. 3063-3070, Aug. 2017.

4. **A. Bhattacharjee** and S. Dasgupta, "Optimization of Design Parameters in Dual-κ Spacer-Based Nanoscale Reconfigurable FET for Improved Performance," *IEEE Trans. Electron Devices,* vol. 63, no.3, pp. 1375-1382, Mar. 2016.

5. **A. Bhattacharjee**, M. Saikiran, A. Dutta, Bulusu. A and S. Dasgupta 'Spacer Engineering-Based High-Performance Reconfigurable FET with Low OFF Current Characteristics', *IEEE Electron Device Letters*, vol. 36, no.5, pp. 520-522, May. 2015.

International Conferences

1. **A. Bhattacharjee**, M. Saikiran and S. Dasgupta 'S/D Spacer Effects on the Performance of a Silicon nanowire Ambipolar FET', *18th International Workshop on Physics of Semiconductor Devices (IWPSD 2015)* organized by Indian institute of Science, Bangalore, Karnataka, December, 2015 (Conference proceedings only).