DEVICE-CIRCUIT INTERACTIONS IN TUNNEL FET: AN ANALOG DESIGN PERSPECTIVE

Ph.D. THESIS

by

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OCTOBER, 2018

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A THESIS

Submitted in partial fulfilment of the requirements for the award of the degree
of

DOCTOR OF PHILOSOPHY

in

NANOTECHNOLOGY

by

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OCTOBER, 2018

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **"DEVICE-CIRCUIT INTERACTIONS IN TUNNEL FET: AN ANALOG DESIGN PERSPECTIVE"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Centre of Nanotechnology of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from January, 2015 to October, 2018 under the supervision of Dr. Anand Bulusu, Associate Professor, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(ABHISHEK ACHARYA)

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ABSTRACT

The static-power constrained applications have promoted the research on the steep slope transistor based analog/digital circuits. The prime objective is to overcome the problem of the MOSFET's ever-increasing leakage current while maintaining the performance. Therefore, the transistors with a steep subthreshold swing (SS) are being extensively investigated by the device research community. Among the emerging transistors, Tunnel FET (TFET) is one of the most promising by virtue of its ultra-low leakage current and MOSFET compatible fabrication processes. There are two kinds of TFETs, point and line TFET which are differentiated as per the direction of tunneling with respect to the gate. The steep slope of these devices makes them suitable for the sensing and other low power applications. However, the biasing schemes and the impact of device design parameters on the analog circuit performance have not been discussed in depth for TFETs. Bearing the above facts in mind, the biasing strategies and the small signal model for TFET need to be examined in detail. In addition, the drain current saturation voltage (V_{DSAT}) and the body bias saturation voltage (V_{BSAT}) are extremely important from the perspective of analog design.

We investigated for the first time, a method to extract V_{DSAT} for the point and line TFETs. The saturation in output characteristics of a point TFET is attained when the difference in the conduction band energy of the channel and drain is a few K_BT. As the drain voltage (V_{DS}) increases, the device initially enters in a *soft* saturation state and subsequently into *deep* saturation. The onset of *soft* and *deep* saturation happens for a constant difference in the gate-drain bias (V_{GD}). We have also validated our results with the published experimental data. A *soft* saturation state in L-TFET is attained when the electron density in the epitaxial layer over the source saturates with the drain bias (V_{DS}) and the conduction band energy gets pinned. In addition, at the onset of *deep* saturation, the electron density in the epitaxial layer over the channel drops below its doping level and the conduction band energy becomes invariant of any further increase in V_{DS}. The transconductance and output resistance abruptly increases when the device enters in the *soft* saturation regime and attains a maximum in the *deep* saturation. The difference V_{GD} is found to be a constant at the onset of saturation and remains independent of the gate-source overlap length (L_{OV}). A shift in V_{DSAT} and V_{GD} is also observed with a change in

the thickness and doping of the epitaxial layer. Further, a nominal change of ~ 5% in the voltage gain of a common source amplifier is observed when the *n*-device is either biased in *soft* or *deep* saturation regime, without any trade-off in the bandwidth. The proposed method is suitable for the analog design as V_{DSAT} varies linearly with V_{GS}.

The impact of body bias (V_{BS}) and gate-source overlap on the device-circuit analog performance of the epitaxial layer based L-TFETs is reported for the first time. The occupancy probability within the valence band of the source determines the modulation of I_D with V_{BS}. An increase of 40-60 % in I_D with the reverse V_{BS} is observed, while the forward V_{BS} does not significantly alter the drain current. The reverse V_{BS} at which I_D attains the maximum value is defined as V_{BSAT}, which changes almost linearly with V_{GS}. We also proposed a mathematical model to determine V_{BSAT}, bsed on the electrostastics of the gate-source overlap region. V_{BSAT} increases with the gate-source overlap length (L_{OV}) and decreases with the thickness of epitaxial layer. The intrinsic gain and unity gain cut-off frequency increase with the reverse V_{BS} and remain nearly constant with the forward V_{BS}.

In general, the device width is being used to improve the drive capability in circuit design. We investigated that an increase in the gate-source overlap can also substantially enhance the analog performance of L-TFETs. Thus, we propose L_{OV} variation-aware small signal model for L-TFETs based analog circuit design. This model can be used for appropriate sizing of the transistor for a target amplifier performance. The drain current initially increases linearly with L_{OV}, and then exhibits a non-linear behavior. This is due to reduced effect of the lateral electric field at the far end of the gate-source overlap region. It is observed than an increase of 2.5× in L_{OV} results in ~2.33× increase in the voltage gain without any significant penalty in the bandwidth. Therefore, L_{OV} can be used as an important design parameter in the analog circuit design, as it does not significantly change the output resistance and the gate-drain capacitance of the device.

ACKNOWLEDGMENTS

वक्रतुण्ड महाकाय सूर्यकोटि समप्रभ । निर्विघ्नं कुरु मे देव सर्वकार्येषु सर्वदा ॥

I have been very blessed to pursue my PhD studies under the esteemed guidance of **Dr. Anand Bulusu**, Associate Professor, Department of Electronics and Communication Engineering, IIT Roorkee, Roorkee. With his continuous guidance and encouragement, I could be motivated to explore a heterogeneous array of topics in the device/circuit engineering. I am extremely thankful to him for the meticulous care with which he examined my work and a multitude of other reasons, which made it possible for this thesis to take its present shape.

I deeply value the insights and advice received from the faculty members of Microelectronics & VLSI Group, IIT Roorkee on a wide variety of topics. My conversations with them and their students have been a fantastic learning experience for me. I'd also like to thank the members of my Student Research Committee for sparing their precious time to carefully review my progress and providing critical suggestions to improve the work. I sincerely thank Naveen Sir for his support in dealing with the workstations, tools, licenses, and internet related issues.

I am also thankful to my parent organization *Government Engineering College Bikaner* for sponsoring me for this noble cause and *Quality Improvement Programme Centre*, *IIT Roorkee* for providing all the necessary logistic arrangement, during this tenure. Special thanks to my fellow colleague, brother, and good friends Alok Acharya and Ajay Choudhary. It was always cool hanging out with you guys in the mother tongue.

I have been fortunate to be part of a lab filled with fellow students who have been great teachers (and co-learners), colleagues, and friends. I have learned much from and enjoyed to know all of my labmates over the years, including Navjeet, Shashank, Neeraj, Lalit, Deepak, Rahul, Inder, Govinda, Shivam Sir, Arvind Sir, Om Sir, and Bhattacharjee. My graduate experience would be unimaginable without the deep discussions and time frittered away in their company. Prabhat Dubey has been a constant sounding board and debate partner on just about every topic imaginable. Abhishek Solanki was an able and willing helper during his free time in our lab. Outside of our group, I have similarly benefited and drawn inspiration from continual discussions with many other fellow students. Out of so many educational and entertaining

conversation partners, I've benefited in particular from knowing, and talking the ears off of Vikas, Anant, Sanjay, Gyanendra, and Amit. I've spent a lot of time with them and the memories that bring smile on my face. The never ending tea sessions with them at different corners of the campus were magical to vaporize my fatigues. There are no words to describe my gratitude towards my fellow colleagues Kunal, Jyoti, Rahul and Lomash for their unconditional encouragement and inspiration. There all are pillar of support guiding through the thick and thin of time.

Most or all of the materials presented in Chapters 3, 4, 5, and 6 have been either published or communicated in assorted IEEE journals and conferences; they are reproduced here with the minor modifications in accord with the author rights agreements for the respective publications.

Thanking my family is both essential and inadequate in the face of all the experiences we've been through together. There are no words to describe gratitude towards my family members for their unconditional love, trust, inspiration, and encouragement. I would like to express my great appreciation to my late grandfather, late father, mother, wife and my lovely daughter, for their patience and sacrifice to my selfish dream.

I know that all things work together for the good of those who love God. May my life and work be in accord with His will and glorify His name.

(Abhishek Acharya)

To

My Family

& Friends

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

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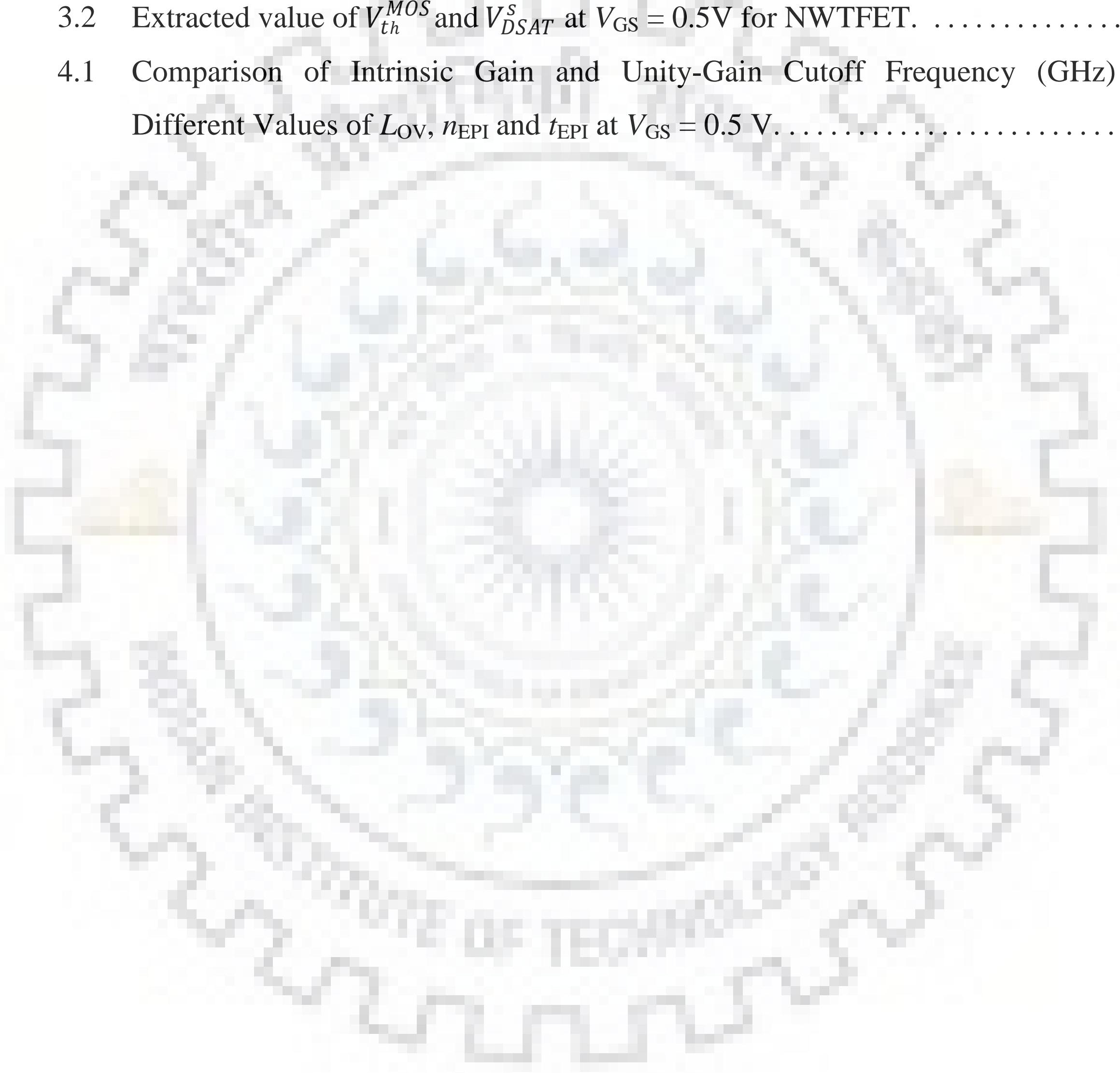


Chapter 1

Introduction

The modern semiconductor devices have established a new dimension in the handheld consumer and healthcare electronics such as tablet PC, smartphones, and sensors. This requires an electronic device that consumes less power with a minimum supply voltage and OFF-state leakage current (I_{OFF}) [1]. The reduction in power dissipation turns out to be essential as CMOS technologies grow. This demands for a new transistor based switch which works at the lower operating voltages and maintains a reduced level of the leakage current. In this manner, the opportunities and challenges emerge from the quantum mechanical transport. A novel tunnel transistor can essentially operate at significantly lower voltages than MOSFETs by employing band-to-band tunneling as the main conduction mechanism with the small subthreshold slopes (SS) [2].

1.1 Fundamental Limitation of CMOS: Tunnel FETs

A reduction in the power consumption of MOSFETs is primarily because of the lowering of the supply voltage. However, keeping this trend by employing the CMOS technology scaling, gives diminishing results due to an increase in the OFF-state leakage current. Consequently, the total power consumption also increases. The MOSFET devices suffer from a fundamental limitation of the lower bound o subthreshold slope and thus also the OFF-state leakage current. The complementary MOSFETs are not suitable for the circuit operation below 0.5 V supply voltage because of their SS limitation, which is not possible to scale below 60 mV/decade at the room temperature, as shown in Fig. 1.1(a) [3]. As per the scale length theory of MOSFETs, the threshold voltage can be reduced by the same scale as of the supply voltage [4]. This results in a net increase in the gate overdrive voltage and I_{OFF}. Beyond 65 nm technology node, the leakage is very high and static power dominates, as shown in Fig. 1.1(b) [5]. Therefore, the fundamental bottleneck with the MOSFET based technologies is the non-scalability of SS. In conventional MOSFETs, the lower bound of 60 mV/decade is because the subthreshold current

is driven by the 'Boltzmann tail' of the source carrier population, with the energies greater than the top of the barrier in the channel. In addition, this 'Boltzmann tail' becomes more significant because of the drain induced barrier lowering (DIBL), which is a major challenge for the short channel MOSFETs of the present era.

At the room temperature, $SS = \frac{dV_{GS}}{d\log_{10} I_D} = \frac{2.3\mathrm{m}\,\mathrm{K_B}\,\mathrm{T}}{\mathrm{q}}$, and $m = 1 + \frac{C_{DEP}}{C_{OX}}$ indicates the voltage drop across the channel effectively. Here, m, K_B, T, C_{DEP} and C_{OX} are the mass of electron, the temperature, Boltzmann's constant, depletion and oxide capacitance respectively. This fundamental limitation necessitates a very small supply voltage for operating the MOSFET devices. In addition, the voltage scaling also hampers by the increased variability of the scaled devices owing to the random dopant fluctuations [6].

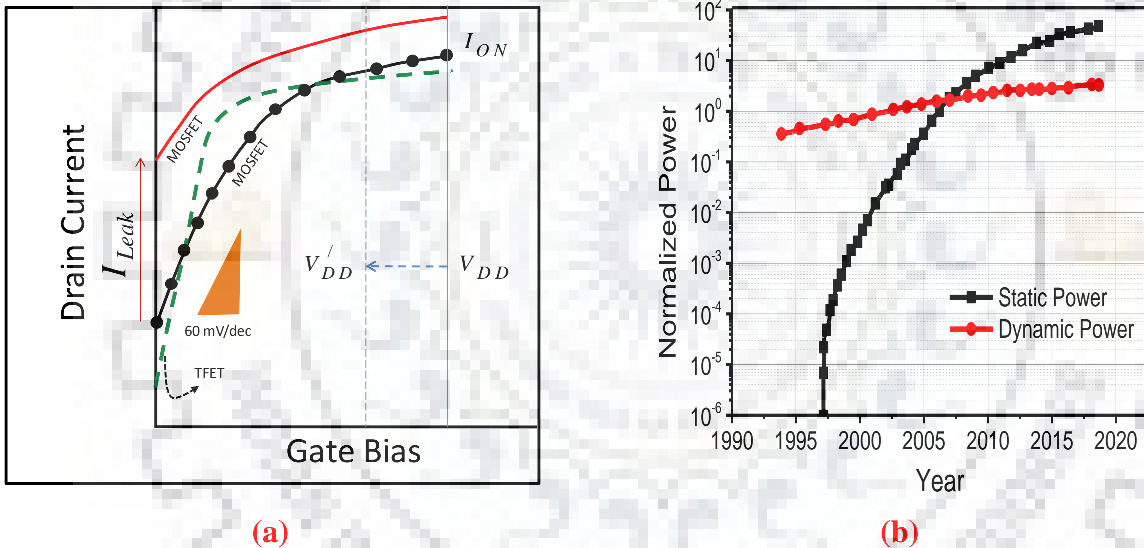


Figure 1.1: (a) Transfer characteristics of MOSFET indicating an exponential increase in the leakage current with a decrease in the threshold voltage (V_{TH}) due to the technology scaling. (b) Trends of the dynamic and static CMOS power show that static power consumption has become a serious problem [5].

To prevail over these fundamental constraints, a new carrier injection mechanism must be employed instead of the drift and diffusion of carriers. This has initiated the research in so-called "steep slope" transistors which can have SS < 60 mV/decade. Therefore it is possible to achieve a good $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio at the lower voltages. Many such devices have been proposed to achieve the steep slopes [6], [137] as follows:

- ***Impact Ionization MOS (IMOS)*** is based on the avalanche breakdown principle and requires a high reverse bias voltage. The steep slope is achieved by the process of impact ionization in the high-field region (drain junction) when the device operates in the saturation regime. Hole current generated due to impact ionization (for an *n*-channel device) enhances the potential of the transistor body near the channel region. This decreases the threshold voltage and increases the drive current [137]. The increase in current further increases the rate of impact ionization. By the process a positive feedback loop is completed. Consequently, the drain current latches rapidly from the OFF state to the ON state and SS < 60 mV/decade can be observed [138]. However, these devices suffer from serious scalability issues.
- ***Nano-Electro-Mechanical Switches (NEMS)*** are fabricated with mechanical contacts. The gate electrode remains in contact with the gate dielectric during the OFF state, thus, the short-channel effects are efficiently suppressed. In addition, the gate electrode gets separated from the gate dielectric during the ON state, hence. This dynamically lowers the threshold voltage and the drive current of transistor is enhanced, along with the elimination of the gate leakage. The NEMFETs are likely to meet the performance specifications for the low power applications, even at 25 nm gate length, and is attractive choice for scaled supply voltage operation [139]. These devices are having a lower speed and also suffer from the reliability issues.
- ***Negative Capacitance FETs (NCFETs)*** are based on the ferroelectric concept. The concept of NCFET was recently demonstrated by Salahuddin *et al.* in 2008, using a negative differential capacitance [140]. Theoretical NCFET projections were reported using HfZrO2 as anti-ferroelectric material and it was shown that a minimum SS ~ 23 mV/decade can be achieved [141]. NCFETs having ferroelectric and organic material in their gate stack have been also experimentally demonstrated with SS ~ 18 mV/decade [142]. A minimum SS ~ 8.5 mV/decade for FinFET based negative capacitance device was experimentally measured with wide hysteresis [143]. Ferroelectric HfZrOx FET was experimentally reported with a small hysteresis window shift (<0.1 V), reverse SS ~ 28 mV/dec, and forward SS ~ 42 mV/dec. These devices are primarily used for energy harvesting applications [144]. It is found that ferroelectric damping effect results in large short circuit power and delay, which in turn limits the high frequency operation [145]. Ferroelectric

thickness should be properly tuned in order to get saturated output characteristics. In addition, these devices suffer from the lower speed, and the interface states also pose fabrication complexity.

- ***Hyper FET*** is a recent addition to the plethora of steep slope device, also popularly known as Phase Transition FET. In these devices the source terminal is attached to the phase transition correlated material. The steep slope of the Hyper-FET is due to the collective carrier dynamics of the correlated material. During the transistor operation, these materials experience selective phase switching. Correlated materials show a strong correlation among their inherent electrons. Consequently, they have striking electronic and magnetic properties such as spin–charge separation, metal–insulator transitions, and half-metallicity [147]. Few examples of these materials are vanadium dioxide, doped chalcogenide, Cu-doped HfO2 etc which have highly nonlinear electric behavior. The functionalities of Hyper-FETs have already been shown experimentally with the discrete and monolithic incorporation of the correlated material with the transistor. In addition, SS ~ 8 mV/decade has been measured in the monolithically integrated Hyper-FET [137].
- ***Tunnel FETs*** are based on the band-to-band tunneling transport mechanism and exhibit steep turn-on characteristics. This device will be discussed in the rest of the thesis comprehensively. The above mentioned steep slope devices are helpful in the analog applications to realize:
    - Shorter discharging time for a node capacitor.
    - Better analog switch with linear ON state resistance having lower value.
    - Differential amplifier with larger voltage amplification for small signal.
    - Current mirror with more precise current transfer.

Among all these devices, band-to-band tunneling (BTBT) transistors have emerged as one of the most promising because of their potential for low voltage operation and fabrication compatibility with CMOS technology [7].

1.2 Working Principle of Tunnel FET

In essence, TFET works as a gated *p-i-n* structure where the carrier transport takes place by BTBT between the source and channel, as shown in Fig. 1.2 [2]. In order to remain consistent with the MOSFET technology, names of the terminals are selected such that the voltages are

applied in an analogous way for TFET operation. The n^+ region of a TFET is denoted as its drain, and the source is made up of p^+ region for an *n*-type device. For an *n*-type device to be in the OFF-state, the conduction band energy of the channel is higher than the valence band energy of the source, therefore, preventing the tunneling to occur [Fig. 1.2]. With the increased gate bias, the conduction band edge of the channel is pulled below the valence band edge of the source, such that BTBT occurs and the device becomes turn-on. In a similar fashion, the *p*-type device can be realized by just reversing the doping polarity of the *n*-type device. The carrier injection from the source is a strong function of the range of energies over which tunneling can occur. Besides, the high-energy Boltzmann tail of the source distribution does not append to the tunneling current at the low bias.

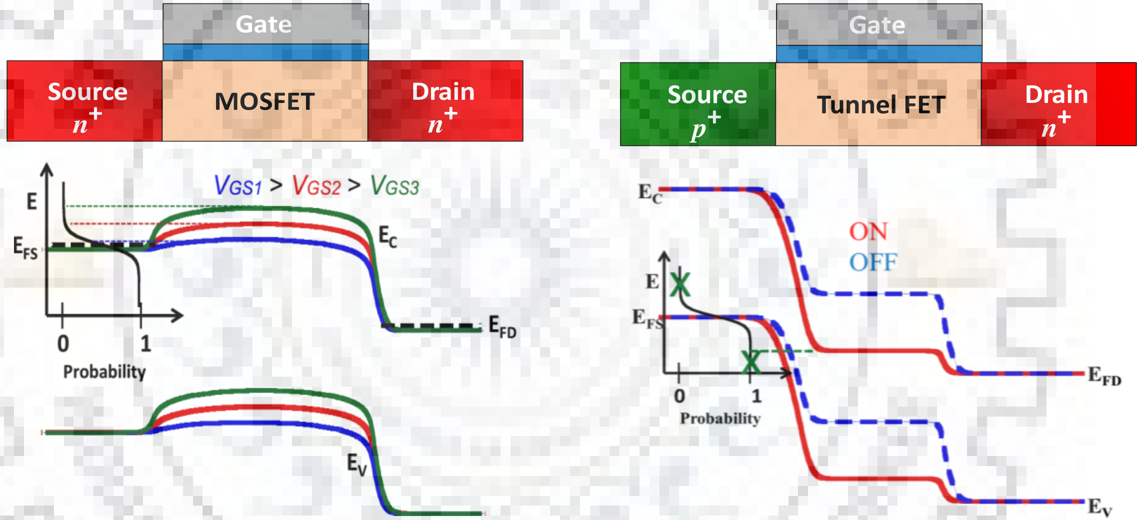


Figure 1.2: Comparison of working mechanism between MOSFET and TFET. E_C, E_V, and E_F are the conduction band, valence band, and Fermi energy respectively.

Therefore theoretically, it is possible for TFETs to attain the subthreshold swings appreciably below $ln(10)K_BT/q$ mV/decade with a lower value of I_{OFF}. [8]. The tunneling probability, T and tunneling current I_{BTBT} can be calculated using WKB approximation as:

$$I_{BTBT} \propto T \approx \exp\left(\frac{-4\lambda\sqrt{2m^*}\,Eg^{3/2}}{3\hbar(\Delta\Phi + Eg)}\right) \quad (1.1)$$

Here, E_g is the energy bandgap at tunnel junction, λ is the screening length, m^* is the tunneling mass and $\Delta\Phi$ is the range of energy over which tunneling can occur. Therefore, the important conditions for the band-to-band tunneling to take place are:

- Available states to tunnel from
- Available states to tunnel to
- The energy barrier that is sufficiently narrow for the tunneling to take place
- Conservation of momentum.

Tunnel FETs suffer from the low drive currents in spite of their steep slope. Further, the steep slope also depends upon the interface quality at the tunneling junctions.

Point and Line TFETs: Tunneling Direction

Tunnel FETs can be classified into two categories according to the direction of tunneling. The first one is Point TFET, in which the tunneling occurs at the edge of source-channel junction. The contribution of this tunneling is dominant in the small localized area. The second category is the Line TFET, in which the directional of tunneling is orthogonal or perpendicular to the gate. Line TFETs exhibit one dimensional nature of the band-to-band tunneling unlike point tunneling where two dimensional picture of band-to band tunneling is present. The line TFETs have increased area of cross-section for tunneling, hence the driving capability of such devices are always higher than their point tunneling counterparts.

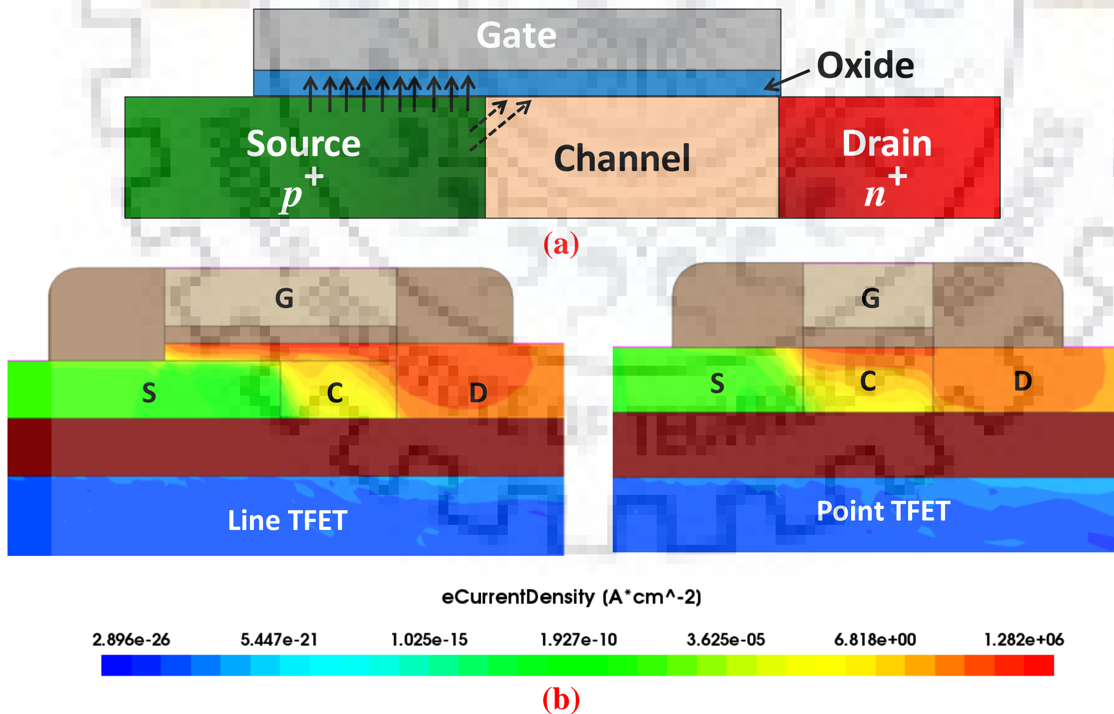


Figure 1.3: (a) Classification of TFETs as per the direction of tunneling. Solid arrows indicate the Line tunneling and dashed arrows indicate the Point tunneling. (b) Current Density in the Line and Point TFET devices obtained through our numerical TCAD simulation two devices.

It is observed from the numerical TCAD simulations, that the current flow lines are almost similar for these two devices. However, the current density is higher in the case of Line TFET devices due to the increased area of cross-section for the tunneling, as shown in Fig. 1.3(b).

1.3 Motivation

The fabrication of TFET devices is compatible with the state-of-art CMOS technologies and the OFF-state leakage of TFET is appreciably lower than the MOSFET. The potential of TFET to implement ultra-low power analog/digital applications have also been verified by the several simulation and experimental studies. However, currently reported TFETs offer a low drive current which limits their speed performance, a relevant use can be found in the power-constrained applications, such as Internet of Thing (IoT) sensors. These sensors catch each and every single event coming whenever. Thus, it is not feasible for the circuits to remain turn-off very often, consequently, the static power consumption increase. TFETs are being extensively explored for the power constrained analog and digital applications (IoT), owing to their steep slope, lower I_{OFF}, and higher output resistance. This encourages us to determine the dependence of TFET analog performance on the bias voltages and the device design parameters. It has been established as a fact that the proper biasing of the analog circuit is essential; hence a detailed study on the drain current saturation is also required. The saturation of drain current in TFET is very unique in nature. It occurs at a constant difference between the gate and drain bias. This necessitates the understanding of the physics behind drain current saturation in TFETs. Therefore, it is also required to extract the drain current saturation voltage (V_{DSAT}) for both the line and point TFETs, in order to bias them properly in the analog circuits. The impact of body bias on the device performance is very critical as it modulates the drive capability of the device, so there is a need to model such effects. In addition, the variation in gate-source overlap length modulates the drive capability of the epitaxial layer based line TFETs, and hence it can be used as an important design parameter for the analog circuit design. Furthermore, a device design guideline is also required to obtain the optimum device-circuit analog performance.

1.4 Objectives

In this work, the physics behind the saturation in the drain current of the point and line tunnel FET is explained from the perspective of analog design. Thereafter, a method to extract

the V_{DSAT} is also proposed for the first time for these devices. The impact of body bias and gate-source overlap on the line tunneling devices is also examined in this work. This is accomplished by the following objectives:

- To explain the physics behind the drain current saturation in the point and line TFETs.
- To propose a method to extract the drain current saturation voltage (V_{DSAT}) for the point and line TFETs.
- To demonstrate the device-circuit analog performance in the *soft* and *deep* saturation regimes based on the proposed methods.
- To establish a device design guideline to obtain an optimum device/circuit analog performance using TFETs.
- To model the impact of body bias on the line TFETs and explain its implications to the analog design. A method to extract body bias saturation voltage (V_{BSAT}) is also discussed.
- To propose a gate-source overlap variation-aware small signal model for the line TFETs to determine the analog device-circuit performance.

1.5 Outline of Work in this Thesis

This thesis is based on the objectives discussed above. This thesis consists of a total seven chapters. Each chapter begins with the introduction, problem statement, and motivation behind the respective study. Thereafter, the simulation framework is discussed in details. This is followed by the analysis and interpretation of results. The novelty of the work is also drawn in the conclusion section.

Chapter 1 provides the need of steep slope devices for the low power application. This chapter outlines the basic working principle and the potential application area of TFETs. The definition of line and point TFET is also introduced. Thereafter, a summary of each chapter is presented at the end.

Chapter 2 presents an extensive literature review of TFETs, starting from its origin to the recent advancements. This also elucidates that how the junction and material engineering are the major driving force for obtaining the steep slope in TFET devices. The physics and analytical models of TFETs are presented with their significance. The potential applications and limitations of TFETs are also discussed at the end of this chapter.

Chapter 3 deals with the thorough explanation of the physics behind the drain current saturation in the point tunneling based TFETs. A well-calibrated simulation deck is used to carry out the numerical simulations using Sentaurus TCAD tool of Synopsys Inc. An approach to define the *soft* and *deep* saturation condition is also presented. We proposed a systematic methodology to identify the *soft* and *deep* saturation voltages of the device, and then a method to extract the V_{DSAT} is also presented for the first time. Consecutively, this facilitates the analog designer to bias the analog circuit in the appropriate regime. A common source amplifier biased in the *soft* and *deep* saturation regime is also demonstrated. Further, the impact of the device design parameters on V_{DSAT} is also presented with the new physical insights. The validation of the proposed method is also done against the experimentally measured data.

Chapter 4 explains the saturation in drain current for the line TFETs. The device under consideration is an epitaxial layer based TFET, whereby the tunneling occurs normal to the gate. The physics of saturation is different from the point tunneling devices, as the tunneling mechanism is different. As compared to point TFET, the area of the cross-section for tunneling is effectively increased in the line TFETs. Further, a method to extract the V_{DSAT} for the line TFETs is also proposed for the first time. We also figured out the device design guidelines for the line TFETs based analog circuit. The variation of V_{DSAT} with the vital device design parameters like overlap length, doping, and thickness of the epitaxial layer, is also presented with the physical insights.

Chapter 5 presents a comprehensive study about the impact of body biasing on the epitaxial layer based line TFETs. The modulation of drain current with the body bias is mainly due to the modulation of the available states for tunneling. An explanation based on the physics for the above said effect, is also validated by a mathematical model proposed by us. The variation in V_{BSAT} (the voltage at which the drain current maximize) with the gate and drain bias is also explained with our model. The variation in V_{BSAT} with device design parameters is also presented. The behavior of vital analog performance parameters with the reverse and forward body bias is also examined in detail. Further, the impact of body biasing on V_{DSAT} is also investigated from the perspective of analog circuit design.

Chapter 6 demonstrates L_{OV} variation-aware semi-empirical small signal model for L-TFETs based analog circuit design. We report a comprehensive physics behind the drain current dependence on the gate-source overlap length (L_{OV}) in the line TFETs. Thereafter, the influence of L_{OV} on the vital small signal parameters is also discussed for the first time. It is

observed that the increase in drain current with the increasing L_{OV} exhibits a nonlinear behavior. The proposed semi-empirical small signal model is based on the electrostatics of the gate-source overlap region. Further, the advantage of L_{OV} variation over the device width in the analog circuit design is also examined.

Chapter 7 presents the major findings of the thesis. The conclusions are drawn on the basis of results obtained through the numerical TCAD simulations and physics based models. The future scope of the current study is also proposed for the prospective readers of the device/circuit research community.

Chapter 2

Literature Survey

An increased leakage current, and hence the power budget is a primary setback for the nano-scale integrated circuits. In general, the supply voltage scaling shrinks the energy required for switching, however, the transistors in present era integrated circuits, require more than 60 mV of the gate bias to augment the drive current by one order of magnitude at the room temperature. TFETs overcome this limit by employing the quantum-mechanical tunneling rather than the thermionic injection, to inject the charge carriers into the channel of the device. TFETs based on nano-wires or ultrathin semiconductor films can attain around hundred times power reduction over the CMOS technology [9]. Therefore, an integration of TFETs with CMOS technology can elucidate the problem associated with the low-power integrated circuits.

2.1 Initial work on Tunnel Device

The concept of tunnel transistor has a long history, going back to the realization of tunnel diode based on inter-band quantum mechanical tunneling followed by a three terminal tunnel device by Banerjee *et al.* in 1987 based on Zener effect [10]. Further, the idea of inter-band tunneling was many times rediscovered and the first experimental demonstration of the surface tunnel transistor (STT) was submitted by T. Baba in 1992 having n^+-i-p^+ structure with an insulated gate over the intrinsic region [11]. The first silicon surface tunnel transistor [12] was experimentally presented, based on the lateral BTBT and there was no punch through effect.

2.2 The Promise and Status of Tunnel FETs

Perhaps, the first sign of the massive potential of TFET came into the picture in 2004, with the experimental observations of inverse subthreshold swing (SS) in carbon nanotube based transistor biased to induce BTBT [13]. The current flow was controlled by modulating the conduction and conduction band edges of the channel and source respectively. Therefore, *SS* of 40 and 65 mV/decade was observed for *n* and *p*-type device respectively. Meanwhile, the sub

60 mV/decade swing in Silicon TFET having vertical process flow using the simulation [14] was proposed. They reported optimized TFET characteristics by including a δp^+ *SiGe* layer to increase the tunneling probability along with the scaling issues.

2.2.1 Quench of Steep Slope and High Drive Current

Till date, several experimental and simulation based studies have been conducted to realize SS of sub 60 mV/decade using TFET for both *n*- and *p*-type devices, considering various structures and material system. Since, the fundamental idea is to increase the tunneling current by keeping SS and leakage as small as possible. The tunneling can be modulated by changing the bandgap of material, tunneling mass of material and by controlling the electric field at tunnel junction [15]. Choi *et al.* experimentally demonstrated SS of 52.7 mV/decade [16]. It was suggested to use low bandgap material like *SiGe* and *Germanium* source, abrupt doping profile and the lower equivalent oxide thickness (EOT). The double-gate TFET with a high drive current of 300 μA/μm and SS of 50 mV/decade by employing the concept of strained *Germanium* was experimentally demonstrated [17]. It was suggested to use asymmetric doping along with the degenerately doped source. Gahndhi *et al.* demonstrated Silicon nanowire based TFET using a CMOS compatible vertical gate-all-around process flow [18]. SS and DIBL of the said device were 30 mV/decade and 70 mV/V respectively without any ambipolar effect. Recently, *GeSn* based TFET is proposed for energy efficient design, wherein both *n*- and *p*-TFETs are having comparable drive currents [19], [20].

So far, we have reviewed about group-IV (*Si*, *Ge*, *SiGe,* and *GeSn*) semiconductors based TFET devices. Since group-IV semiconductors are having relatively higher effective masses and indirect band gaps. Thus, these semiconductors are liable to suppress the tunneling probability and hence limit the expected drive current, and hence hinder any obvious technology advantages in terms of CMOS compatibility. To prevail over these limitations, TFETs based on III-V materials and/or hetero-junctions have become more widely explored owing to their smaller and tunable direct bandgap and effective masses, which significantly increase the tunneling probability. Experimentally, many studies have shown higher on-currents in all III-V TFETs compared to silicon, but most have failed to confirm steep SS [7], due to less steep impurity profiles and high density of defects at the source channel junction. Most of the studies were based on *InAs*, *InGaAs* and *GaSb-InGaAs* based material system along with certain modifications in the fabrication process. Perhaps, the most promising experimental

reports have come in *InGaAs*-based TFETs which achieved a minimum subthreshold swing of 60 mV/decade [21] and 64 mV/decade. Several *InGaAs/Si* or *InAs/Si* hetero-junction TFETs with steep SS (as low as 30 mV/decade at very low currents) have also appeared, though, invariably with little on-currents [22]. *InP/GaAs* hetero-structure nanowire TFET has also been measured to have SS below 50 mV/decade, though the strong temperature dependence of SS in the device suggests that the subthreshold current may be due to something other than direct band-to-band tunneling [23]. All such III-V semiconductor devices suffered from high leakage current originating from material issues, complications due to random dopant fluctuation, traps, and inadequately optimized tunnel junction electrostatics because of less steep doping gradients [24], [25], [24]. Recently, *p*-type TFET with hetero-junction of III-V material with *GeSn* is reported showing promising current-voltage characteristics [26].

From the above literature, it is important to note that the group-IV based TFETs are having a low drive current and steep slope, whereas, group III-V based TFETs are having gradual SS along with higher drive current. Therefore, in addition to the material system, structural modifications in TFETs have also been explored, beyond the lateral tunneling structure [27]–[29]. A gate-source overlap is used to improve the drive current by lining up the gate field to the tunneling direction. This, in turn, increases the tunneling cross-section area. Although some experimental devices have adopted this configuration, surface field-induced quantization and fabrication complexity pose possible significant challenges. The gate-drain underlap structures [Fig. 2.1 (a)] have also been exercised to suppress the ambipolar effects in TFETs [30].

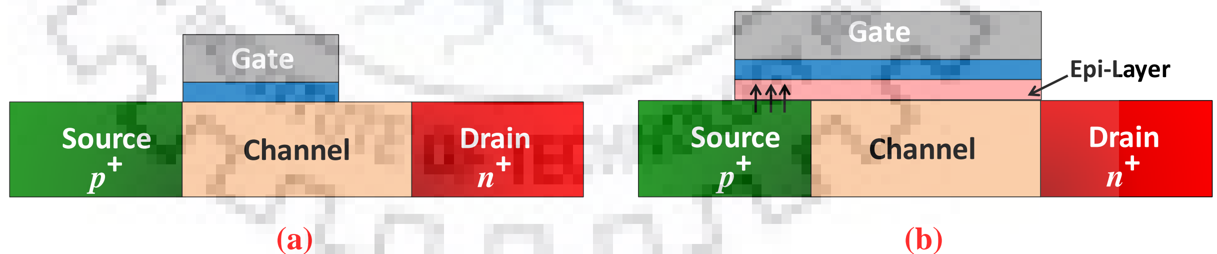


Figure 2.1: Tunnel FET structures (a) gate-drain underlap (b) epitaxial layer based TFET with increased cross-section area of BTBT.

Further, the line tunneling structures are also being explored in quench of higher drive current and steep slope, whereby the tunneling area is increased by the insertion of an epitaxial layer of over the source [27], [29], [31], [32], as shown in Fig. 2.1(b). However, the quantum

confinement issues are important for such devices. The concept of bi-layer TFET [33] is also being explored, whereby electrostatic doping is realized by the back gate biasing and thus, eliminating the need of abrupt junctions [34] . The gate work functions were tuned carefully for such devices.

2.2.2 Current Fabrication Status of Tunnel FETs:

By comparing the theoretical and experimental studies on TFETs, it seems that there exists a large gap between the two. The results presented by Lu *et al.* [7] clearly indicate that highest ON state current for *n*-TFET is 10^{-2} A/μm for the *n*-type device and 10^{-4} A/μm for the *p*-type device was observed till 2014. A few devices with *Si/SiGe/Ge* material system were also reported with SS < 60 mV/decade, having I_D of 10^{-7} to 10^{-5} A/μm. Most of the devices with III-V hetero-structure and broken energy bandgap exhibited I_D as per the projection of ITRS, however, with SS > 60 mV/decade. In 2015, Brijesh *et al.* experimentally reported the complementary $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ near broken bandgap TFET with I_{ON} ~ 275 μA/μm and sub-60 mV/decade for *n*-type TFET, and I_{ON} ~ 10 μA/μm and 115 mV/decade minimum SS for p-type TFET [148]. In 2016, Pandey *et al.* benchmarked $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ and $Ge/Ge_{0.93}Sn_{0.07}$ hetero-junction *p*-type TFET, and reported that $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ TFETs exhibit lower phonon-assisted tunneling then the other one [26]. Recently, a vertical pillar based TFET structure was experimentally demonstrated by Glass *et al.* [135], which has a counter doping in the channel (*Si* is sandwiched between two *SiGe* layer) to improve SS. Negative capacitance InGaAs TFETs [149] and Phase Change TFETs [150] were also reported recently for the analog and digital applications. In addition, quantum engineering is also being explored for 2D material based TFETs [151].

To form the abrupt junctions in TFET, researchers are using Selective Epitaxial Growth (SEG) at high temperature. In addition, to prevent the dopant diffusion into SEG region, *HfO2-TiN* gate stack is being employed by using atomic layer deposition. Traditional hetero-epitaxy suffers from lattice mismatch, which results in defective layers. The art of hetero epitaxy is to reduce and confine the defective layer close to the substrate, such as to keep defects away from the device layer. This may be accomplished by the nucleation and buffer layers, annealing strategies, and/or the use of masked substrates. The monolithic integration of various III-V compounds on *S*i using template-assisted selective epitaxy (TASE) is also being used for electronic devices.

2.3 Tunnel FET Device Physics and Modeling

In this section, the fundamental of TFET device physics will be discussed. The device shows unique ambipolar behavior and the super-linear onset of the drain current. A variety of compact analytical models for TFETs have been presented for the current-voltage and the capacitance-voltage modeling. A few SPICE level models have also been introduced for the circuit design.

2.3.1 Device Physics

There is a precise physical definition of the threshold voltage (V_{TH}) for MOSFETs, whereas no such well-defined characterization exists in TFETs. For all such novel devices, V_{TH} can be extracted at an arbitrarily chosen constant current, as of CMOS experience. It has been reported that TFET exhibits dual threshold voltage: First in terms of the gate voltage and the second in terms of drain voltage [35], [36]. The notorious ambipolar behavior of TFET is defined as the conduction for the high positive and negative gate biases, while the drain is kept polarized in one direction only, for the *n*- and *p*-device respectively [37]. In addition to this, it was investigated that merely increasing the drive current of TFET is not sufficient to outperform the MOSFET, because a unique drain barrier voltage leads to a higher delay in the TFET based circuits. The saturation voltage in TFET is also much higher when compared to MOSFET [38]. The perfect saturation in the output characteristics of TFET was observed, hence the output resistance and intrinsic gain of the device is appreciable [39], [40]. V_{DSAT} for the point TFET was arbitrarily defined as the voltage V_{DS} at which I_D attains 90-95 % of its maximum value. The impact of field-induced quantum confinement in TFET has been also reported by several researchers [41]. Since BTBT is a quantum mechanical phenomenon, it is suggested to consider the multiple valleys of holes and electrons to precisely analyze the behavior of the tunnel device [42].

A dominant nature of the direct BTBT is observed when the *Germanium* mole fraction increases in the $Si_{1-x}Ge_x$ material system [43]. The impact of variation in the process conditions and geometrical parameter on TFET were carried out [44], [45]. It was shown the TAT affects the onset voltage of the device and degrades the subthreshold swing [46]–[48]. Dutta *et al.* [49] has comprehensively reviewed the reliability aspects of III-V TFETs and suggested a few applications of TFET for energy efficient computing. Device-circuit co-design was also

explained by using a look-up table based Verilog-A model. It was established that TFET based circuits show better efficiency for $V_{DD} \leq$ 0.5V. The channel in TFET is inverted due to the injection of electrons from the drain, and at higher V_{DS} the channel charge reduces significantly due to the barrier at drain-channel junction [50], [51].

The degradation of SS due to degenerately doped source and the poor driving capability of TFET was investigated [52]. It was suggested to jointly consider the occupancy function and tunneling probability. It was also highlighted that driving current can be boosted by tunneling probability, if and only if there are available states in source and empty states in the channel over a range of energy. Moreover, for sub-20 nm, the length of the channel and drain must satisfy some minimum criterion to sustain reverse bias drain voltage. A relatively low doping of drain enables the distribution of drain voltage drop across the drain and channel so that the penetration of the electric field can be reduced and hence the leakage current can be controlled [53], [54]. It was explained that the drain has an important role in influencing the potential profile at source when the channel length (L) is reduced to below twice the thickness (t_{Si}) of the device ($L < 2t_{Si}$). It was also reported for the short channel lengths, the source depletion is coupled with the channel potential through the continuity of field at the junction interface [55], [56]. The impact of body bias on the point TFET results in an increase in the drain current due to increase in the electric field at the tunnel junction [57], [58]. It was demonstrated using the experimental results and the device simulation that the drain current increases sub-linearly with gate-source overlap [27], [31], [59] for the epitaxial layer based line TFETs.

2.3.2 Tunnel FET Device Modeling

It is almost a decade or more, TFETs are being widely explored by the research community through experimentations and simulations, but a circuit level model of TFET is yet to be investigated. Most of the analytical models are based on the semi-analytical explanations of the Poisson's equation to determine the surface potential and charge of the channel, in order to obtain the drain current. Further, most of these models are structure specific and very complex expressions of the drain current are derived for them. In most of the cases, the tunneling current density is calculated by employing WKB model [15].

Vandenberghe *et al.* [60] explained the impact of drain bias on I_D and tunneling probability through the analytical model for both the line and point tunneling. It was concluded that the super-linear onset is due to the exponential dependence of the drain current on the tunnel

length. Prior to this work, researchers used to explain the tunneling current as a function of gate bias only, this was the first time, when both V_{GS} and V_{DS} dependence of tunneling current was addressed [61], [62]. A physics based analytical model by incorporating Landauer formalism to evaluate the drive current for SOI-TFET was also presented [63]. The saturation of I_D in the output characteristics was explained [40] using an analytical model and TCAD simulations for the homo/hetero-junction III-V TFETs. It was observed that the saturation in output characteristics of TFET is quite dissimilar from MOSFET owing to the super-linear onset. V_{DSAT} was arbitrarily defined as the gate voltage at which drain current falls to 95% of its maximum value. The delayed saturation further degrades the performance of inverter and other logic circuits, as reported. The dual modulation effects in the surface potential of TFET due to the gate and drain bias for different operating regimes were explained [64]. A few models for the nanowire TFETs are also presented [62], [65], [66].

Lu *et al*. described the current-voltage characteristics of TFETs using Kane-Sze formula [67], [68]. This model includes the super-linear onset in the output characteristics and the ambipolar behavior of TFETs. A set of scaling rules for the sub-10 nm channel length was highlighted for TFETs considering the ambipolar effects and the role of effective mass [69]. The tunneling current was estimated by Franz's two band *E(k)* relationship. SPICE level circuit and analytical models for TFETs by considering source depletion [70]–[72] was presented by Zhang *et al*. A closed form and charge based model for capacitance estimation in TFETs is reported for the point tunneling devices [73]. A review and comparison of various models for TFETs are nicely discussed by Esseni *et al.* [74].

2.4 Tunnel FET for Analog and Digital Circuits

In most of the literature discussed above, it is highlighted that the TFETs are the most suitable candidate to replace CMOS for low power low voltage applications. Lot of circuit level solutions for TFETS is presented in the last few years. Most of them were developed using Verilog–A based lookup table approach, in which I_D-V_{GS}-V_{DS} and C-V_{GS}-V_{DS} characteristics of the device are captured using TCAD simulations. Then the circuit simulations are performed using Cadence and HSPICE platform [75], [76]. This is because of the fact that in the mixed-mode, the device-circuit simulation takes a lot of processing time in TCAD environment. The main downside of this approach is that the current-voltage characteristics of the *p*-TFETs are taken as a mirror image of *n*-TFETs. Nevertheless, this method is still widely adopted due to

the unavailability of SPICE level models of [67], [77], [78]. The gate capacitance of TFET and its impact on the transient behavior of the inverter were discussed [79], and a large overshoot in the output of an inverter was observed due to Miller capacitance (gate-drain capacitance C_{gd}) of TFETs. Further, the gate-source capacitance (C_{gs}) was found to be negligible due to the tunnel barrier at the source-channel junction.

TFET based inverter consumes ~10^4 times less static power than that of a 65 nm low performance CMOS technology node [80]. It is reported [54] that HTFET based ring oscillator shows 9-19 times dynamic power reduction when compared to 45 nm CMOS technology [81]. Esseni *et al.* presented a comprehensive comparison between TFET and MOSFET for ultra-low power applications for $V_{DD} \leq 0.5$ V [77], [82]–[84]. Although, *n*- and *p*-type MOSFETs exhibit equal I_{OFF}, however, *n*- and *p*-type TFETs do not show such behavior. Therefore, the work functions are tuned to achieve equal I_{OFF}. Besides, the extensive research suggests that III-V TFETs are prominent than FinFET for low power digital design [85].

TFETs exhibit higher value of the intrinsic gain than MOSFET [39]. This happens as the output resistance is high owing to a near perfect saturation in the output characteristics. Although, the gain bandwidth product of MOSFET is better than TFET, due to the severe Miller effect in TFET device. The ultra-low-power sensors have wide applications in areas such as healthcare devices, environmental monitoring devices etc. [86], [87]. Differential amplifiers and current mirrors using TFET are also compared with FinFET [86]–[89]. It was emphasized that III-V semiconductors based TFETs are more promising for energy harvesting applications. A less temperature sensitive pre-amplifier stage using TFET based operational transconductance amplifier (OTA) was successfully demonstrated [90], [91].

Sedighi *et al.* [92] presented analog design aspects of TFET based circuits. It was demonstrated that 14 nm III-V hetero-junction TFET based OTA shows 5× reduction in the power dissipation when compared with the FinFET of the same dimension. Furthermore, analog performance as a function of temperature and source compositions ($Si_{1-x}Ge_x$) is also studied experimentally. It has been shown that the drive current increases with increasing *Germanium* content, however, the noise level degrades and hence the devices with *Silicon* source are still favorable for application where minimum $1/f$ noise is required [102], [94]. Recently, TFET for energy efficient computing is benchmarked for the analog [104], [105] and digital [97], [98] circuits.

2.5 Technical Gaps

It is observed that the TFET devices have emerged as a very promising candidate for beyond CMOS technologies. In light of the extensive literature survey, this thesis work explains the drain current saturation in both the point and line TFETs and extraction method of V_{DSAT} is also presented for the same. The prediction of V_{DSAT} under the variation of device design parameter is challenging for the analog designers in order to bias the circuit properly. In addition, the body bias modulates the tunneling generation in L-TFETs, hence it is necessary to model this phenomenon. After the sufficient literature survey, the following technical gaps emerged:

- Several analog circuit applications have been presented using TFETs for energy efficient computing [39], [92], [95], [96], their biasing strategies have not been discussed. It is well known that the drain current saturation voltage (V_{DSAT}) for TFET plays an important role in biasing the analog circuits. V_{DSAT} extraction method based on physics is yet to be explored, to determine the suitable bias range for the analog circuits, as the existing methods are either not consistent with device physics or arbitrary in nature [40], [92]. We propose a model to extract V_{DSAT} for both the point and line TFETs, which is also validated against the experimentally measured data. Thereafter, we will demonstrate the utility of this analysis for analog circuit design.
- Impact of device design parameters on the analog and digital performance of the device has been reported by some research groups. These parameters include the optimization of the gate length, film thickness, spacers, source/drain doping, and lateral straggle parameters [95], [96], [99], [100]. But, a systematic guideline has not been presented so far for the circuit designers. It would be imperative to study the impact of variation in the device design parameters on V_{DSAT} of TFET and analog circuits. Further, the analog circuit performance of the epitaxial layer based line TFETs has not been systematically discussed. We first time propose device design guidelines for obtaining optimum device/circuit performance.
- The impact of body biasing on the performance of epitaxial layer based L-TFET is not reported in the existing literature. It has been stated that the body bias will modulate the drive capability of the point TFET to a certain extent due to an increase in the junction electric field only [57], [58]. However, the role of occupancy functions and hence the available states for tunneling were not reported in the modulation of drive current with

body bias. The value of body bias (V_{BSAT}) at which drain currents attains a maximum is also required to be calculated for presenting circuit design guideline. The device design parameters may also affect the value of V_{BSAT}, which also need to be addressed. We address all these aspects and propose a mathematical model to determine V_{BSAT}.

- Few researchers have reported that the drain current increases sub-linearly with increasing the gate-source overlap length [30], [35], [59]. However, analytical models suggest that I_D-L_{OV} characteristics exhibit a linearly increasing trend [61]. We investigate the physics behind this phenomenon. The gate-source overlap length is supposed to be an important design parameter for amplifier design. It increases the drive current without significantly changing the gate capacitances. On contrary to this, an increase in the device width results in significant increase in the terminal capacitances. A mathematical model to predict the change in analog parameters with change in device design parameter is not presented till date. This issue is also addressed by proposing a semi-empirical small signal model based on the electrostatics of the gate-source overlap.

In this thesis, we will address the above mentioned technical gaps.

Chapter 3

V_{DSAT} Extraction Method for Tunnel FETs and its Implication to Analog Design

This chapter investigates for the first time, a method to extract the saturation drain voltage for TFETs. The saturation in output characteristics of a TFET is found to take place when the difference in conduction band energy (ΔE_C) of the channel (E_{CC}) and drain (E_{CD}) is a few K_BT. As the drain voltage (V_{DS}) increases, it is found that the device initially enters in a *soft* saturation state and subsequently into *deep* saturation. For any given value of gate voltage (V_{GS}), the onset of *soft* and *deep* saturation happens for a constant difference in V_{GS} and V_{DS}. We propose a novel method to extract this voltage difference V_{GD}, which is explained using a phenomenological approach. We have also validated our results with published experimental data. It is found that, the output resistance (r_o), transconductance (g_m) and intrinsic gain ($g_m \times r_o$) increase when the device enters in a *soft* saturation and attains a maximum value in *deep* saturation regime. Furthermore, a common source amplifier biased in *soft* saturation is also demonstrated to have a comparable voltage gain and bandwidth to the one biased in *deep* saturation.

3.1 Introduction

Tunnel FETs have recently been gaining interest for analog and RF circuits due to their low operating voltage and high output resistance [91], [92], [101], [102], [103]. Few experimental demonstrations of the improved circuit performance using TFETs and several simulation based studies have also been conducted to demonstrate the analog performance of TFET at device levels[93], [95], [104]. It is well known that the saturation in output characteristics is a key factor in analog circuit design. Although, the drain current saturation mechanism of double gate TFETs has been discussed in [39], [38], [40], a technique to extract the saturation drain voltage V_{DSAT} has been ambiguously presented. The definitions of V_{DSAT} presented in [51], [100], [128],

[105] are either not consistent for a wide range of bias voltages, or are not readily usable from the perspective of analog circuit design.

Therefore, this chapter, while addressing the problem raised above, proposes for the first time, a new method to extract the onset of saturation in the lateral tunneling based TFET devices. For this study, we consider *SiGe/Si* hetero-junction NWTFET as a target device. This ultimately enables the circuit designer to estimate the suitable terminal bias voltages for analog design. We divide the saturation regime into two sub-regimes: "*Soft*" saturation and "*Deep*" saturation. In *soft* saturation regime, transistor level analog parameters are reasonably good, whereas, in the *deep* saturation regime, these parameters settle at their best values. We discuss the physical origin of these two sub-regimes and thereafter methods to extract the values of V_{DSAT} for both of these sub-regimes. We have shown that the presented V_{DSAT} models exhibits linear relationships between V_{DSAT} and V_{GS} and are quite useful for analog circuit design in estimating the onset of saturation. The validation of the obtained results is done with the help of *Sentaurus* 3-D TCAD simulations and with experimentally measured characteristics published in [19].

3.2 Device Structure and Simulation Framework

Our self-consistent numerical simulations have been performed by using Synopsys *Sentaurus* TCAD [106]. Fig. 3.1(a) shows 3-D view and 2-D schematic of the simulated nanowire device having a diameter of 25 nm and a channel length of 50 nm. An interfacial layer of 1 nm SiO_2 along with 3 nm HfO_2 is used as gate dielectric and the $Si_{0.5}Ge_{0.5}$ material is used as a source, as in [93]. High-κ gate dielectric is used to enhance the electrostatic integrity of the device. The doping concentration of source (*p*-type), drain (*n*-type) and channel (*p*-type) is kept at 10^{20}, 5×10^{18} and 10^{16} cm^{-3}, respectively.

The simulation setup is well calibrated with [107] and includes non-local band-to-band tunneling, bandgap narrowing, mobility models, SRH recombination, and the Fermi-Dirac statistics, as shown in the inset of Fig. 3.1(a). The nonlocal band-to-band tunneling model is activated across all the semiconductor regions to emulate the tunneling phenomenon. This model uses Wentzel-Kramer-Brillouin (WKB) approximation along with two band dispersion model to capture tunneling across all possible junctions and interfaces. For further reading, the details of this model can be obtained from the *Sentaurus SDevice* user manual [106] of Synopsys Inc.

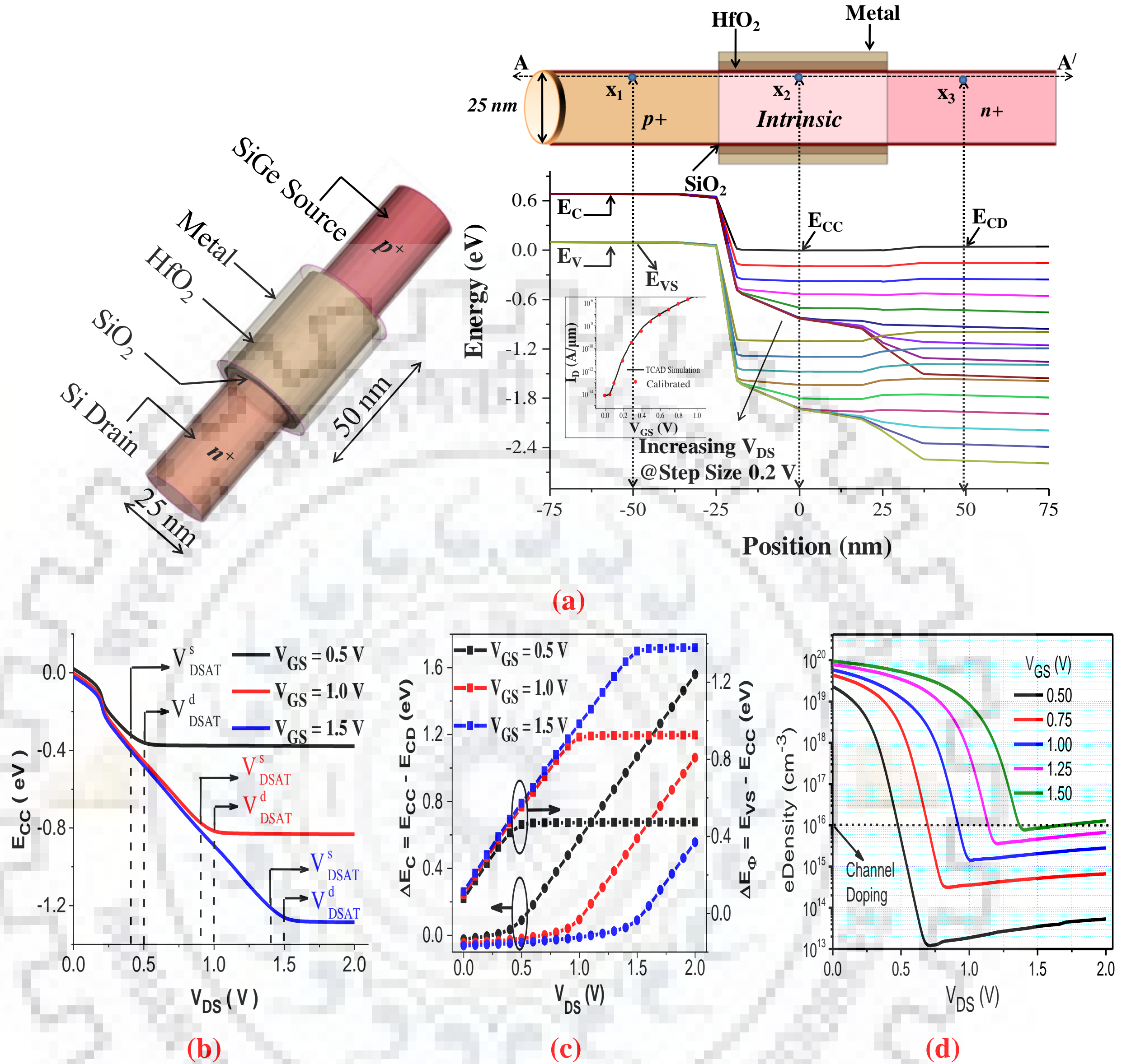


Figure 3.1: (a) 3-D view and 2-D schematic of the target device and its simulated energy band diagram for V_{GS}=1V and V_{DS} varying from 0-1.6 V. ΔE_C is the difference between conduction band energy of channel (E_{CC}) and drain (E_{CD}) and ΔE_{Φ} is the difference between valence band energy of source (E_{VS}) and E_{CC}. (E_{VS}, $E_{CC,}$ and E_{CD} are measured 1 nm below the oxide-semiconductor interface at points x_1, x_2, x_3 respectively along the line AA$^{/}$). Inset shows calibration of I_D-V_{GS} characteristics with [107]. Inset shows the calibration of models. Variation in (b) $E_{CC,}$ (c) ΔE_C and ΔE_{Φ} (d) electron density (charge distribution) with V_{DS}. Please note that, the value of ΔE_C may vary along the lateral distance of the device and also depends upon source/drain doping along with the device structure, but the underlying physics remains same.

A fine nonlocal mesh is also defined for the same. This approach calculates the local wave numbers, and then the tunneling probability is calculated using WKB approximation. Trap-assisted-tunneling (TAT) has been reported as critical modeling parameter in TFET simulation. The effect of TAT is captured by SRH recombination model along with field enhanced Schenk TAT model.

Further, Philips unified mobility and bandgap narrowing models take care of the doping dependence. The bandgap narrowing models and Fermi distributions are also used to capture carrier action in the device under consideration. The calibrated values of the barrier tunneling model parameters with and without quantum corrections (QC) are borrowed from [34], as it results in a shifting of the onset voltage for tunneling [49], [134]. The impact of non-ideal effects such as gate leakage and strain are ignored in this Chapter, as in [127]. We have not incorporated the influence of contact resistance external to the device (due to metal contacts) in our study, as the source and drain doping is sufficiently high.

3.3 Proposed V_{DSAT} Extraction Technique

In this section, the proposed technique to extract V_{DSAT} and its relation with terminal bias voltages of the device is qualitatively discussed, with the example of an *n*-type hetero-junction NWTFET. It may be noted that the results discussed here also hold good for other TFET structures such as a single/double gate, homo-junctions, gate underlap etc. Before proceeding further, we define $\Delta E_C = E_{CC} - E_{CD}$ and $\Delta E_\Phi = E_{VS} - E_{CC}$, where E_{CC}, E_{CD}, and E_{VS} are as depicted in Fig. 3.1(a).The output current saturation in TFET is discussed with new physical insights in the subsequent subsections.

3.3.1 Definition of *Soft* and *Deep* Saturation in Tunnel FET

Fig. 3.1(c) shows a plot of the conduction band energy difference ΔE_C as a function of V_{DS}. It is discussed later, that the analog parameters are a strong function of ΔE_C. For a given value of V_{GS}, with V_{DS} increasing, initially the energy bands E_{CC} and E_{CD} remain aligned and the drain current (I_D) keeps on increasing, as shown in Fig. 3.1(a) and 3.2(a). When the value of V_{DS} reaches to V_{DSAT}^s (V_{DSAT} for the onset of *soft* saturation), a misalignment of E_{CC} and E_{CD} ($\Delta E_C = K_BT$, where K_BT is thermal energy) occurs as shown in Fig. 3.1(c), and thereby I_D begins to saturate as shown in Fig. 3.2(a); this is the condition for *soft* saturation ($V_{GS} - V_{DSAT}^s =$

Constant). This is because, initially the value of E_{CC} decreases with an increase in the drain voltage, as shown in Fig. 3.1(b), which is consistent with [51]. After the onset of *soft* saturation, when V_{DS} increases beyond V_{DSAT}^{s} for a given value of V_{GS}, the channel charge begins to decrease as the drain starts to sweep the channel charges [Fig. 3.1(d)]. Once the channel charge is very close to the value of channel doping, any further increase in V_{DS} does not significantly alter the channel charge (hence channel potential Ψ_S), resulting in an increase in ΔE_C as shown in Fig. 3.1(c). This eventually results in a weak dependence of ΔE_Φ on V_{DS}, thereby, R_o and $g_m \times R_o$ increase beyond V_{DSAT}^{s} [Fig. 3.2(b)]. Incidentally, the value of V_{GS} for which the channel charge is very close to the value of channel doping, is also the threshold voltage of the gate-channel-drain MOS system of NWTFET.

As V_{DS} increases to V_{DSAT}^{d} and beyond (hence there is an increase in ΔE_C), most of the channel charges are swept out by the drain terminal. Here, V_{DSAT}^{d} is the value of drain voltage at the onset of *deep* saturation condition. For $V_{DS} = V_{DSAT}^{d}$, results in an almost flat band condition in the channel (therefore, $V_{GS} = V_{DS}$). Since V_{GS} is kept constant, and the channel charge drops below the channel doping value [Fig. 3.1(d)], therefore, the channel potential (Ψ_S) remains constant for any further increase in V_{DS}. Thus, only the value of E_{CD} decreases and E_{CC} remains almost pinned to a value as shown in Fig. 3.1(b). This results I_D to attain a maximum value and remaining invariant to any further increase in V_{DS}. This is the condition for *deep* saturation ($\Delta E_C = 3K_BT$ and $V_{GS}- V_{DSAT}^{d} = 0$). For $V_{DS} < V_{DSAT}^{s}$, E_{CC} and E_{CD} remains aligned, and height of the tunneling window (ΔE_Φ)gets affected by drain bias unlike the situation when $V_{DS} \geq V_{DSAT}^{d}$, and ΔE_Φ is no more affected due to E_{CC} getting pinned to a constant value, as confirmed in Fig. 3.1(a) and (c). Furthermore, it is to be noted that the value of ΔE_Φ is affected by V_{DS} before the onset of *soft* saturation, because the *drain* can thermally inject carriers into the channel.

Please note that ΔE_Φ becomes almost independent of V_{DS} after the onset of deep saturation. Therefore, a perfect saturation is observed in NWTFET, and the values of r_o and $g_m \times r_o$ attain a maximum beyond V_{DSAT}^{d} [Fig. 3.2(b)], which is also consistent with the reported results in [40],[39] for other TFET structures. It is noteworthy to mention here that for sub-20 nm channel length TFETs, the impact of drain-induced barrier thinning (DIBT) is significant [108], and hence the value of E_{CC} is not pinned, rather it gradually decreases with an increase in V_{DS} beyond V_{DSAT}^{d}. It is observed from our TCAD simulations that the impact of DIBT does not affect the value of $V_{DSAT}^{s,d}$. This is because the depletion in channel charge is a strong function of

small changes in E_{CC} only. The degraded saturation, however, results in a reduced value of r_o and $g_m \times r_o$ at sub–20 nm channel lengths.

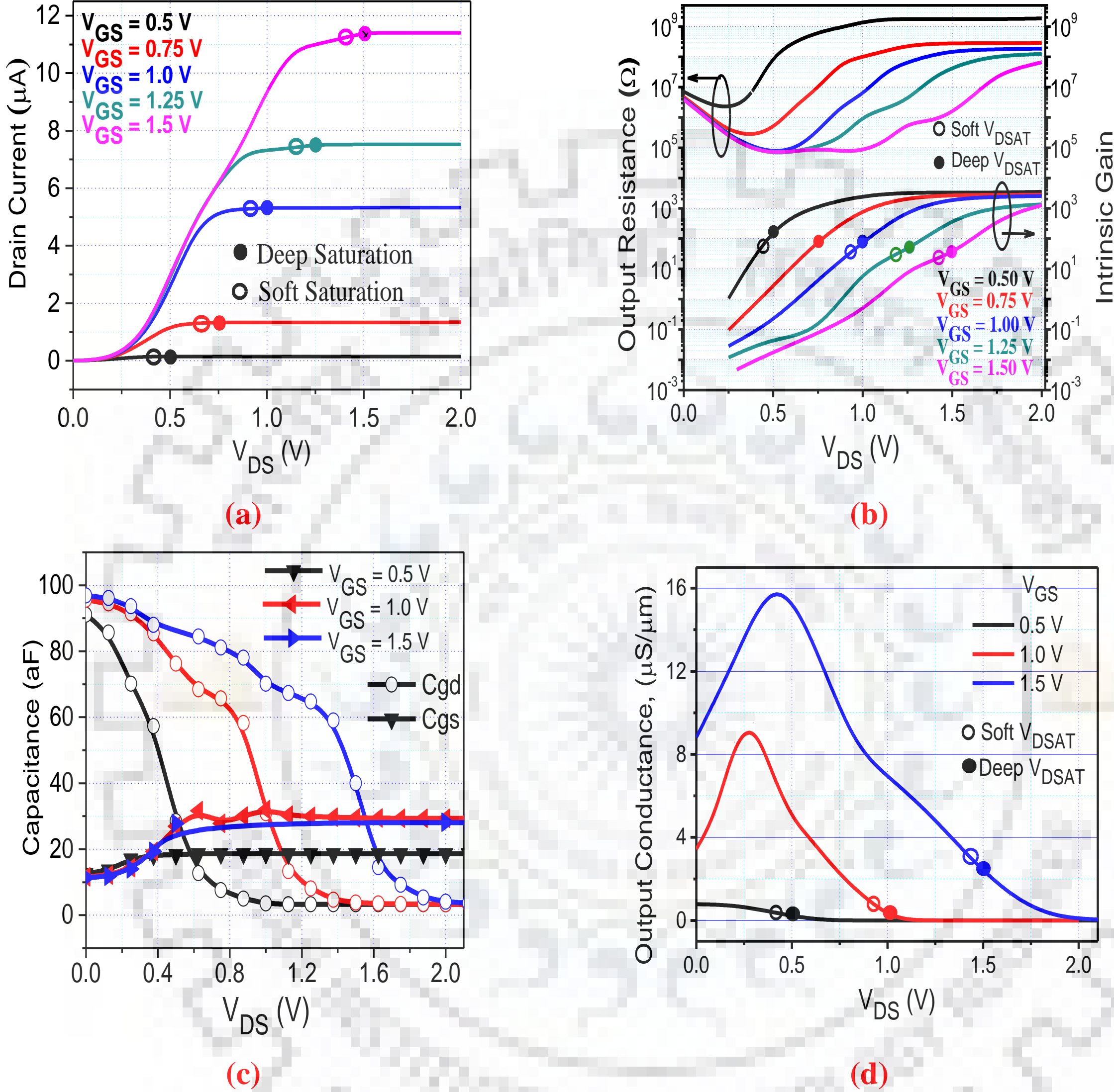


Figure 3.2: Variation in (a) drain current (b) output resistance and intrinsic gain (c) gate capacitance (d) output conductance with V_{DS}. The extracted values of *soft* and *deep* saturation voltages for measured characteristics of hetero-junction NWTFET are marked with empty and filled circles respectively.

3.3.2 A Novel Technique to Extract V_{DSAT}

The above discussion reveals that the voltage differences V_{GS}- $V_{DSAT}^{s,d}$, remain constant with V_{GS} for both the *soft* and *deep* saturation conditions (as determined by ΔE_C and ΔE_Φ). The values of V_{DSAT} from previous works [40], [92], [105] are not consistent with I_D-V_{DS}

characteristics, as can be seen from Table 3.1 and Fig. 3.2(a). The methods of extraction of V_{DSAT} in [40], [92], [105] are empirical and need to be repeated for each value of V_{GS}. B. Rajamohan *et al.* [40] stated that V_{DSAT} can be defined as the drain bias where I_D attains 95% of its maximum value. The contribution of drain threshold voltage due to a super linear onset in the output characteristics of TFET was considered in the calculation in the V_{DSAT} [92]. The method proposed in [105] is valid for the small geometry MOSFETs only. Though [51] also proposes a constant value of V_{GD} at the onset of saturation, its method of extraction of V_{DSAT} is empirical and lacks in physical explanation.

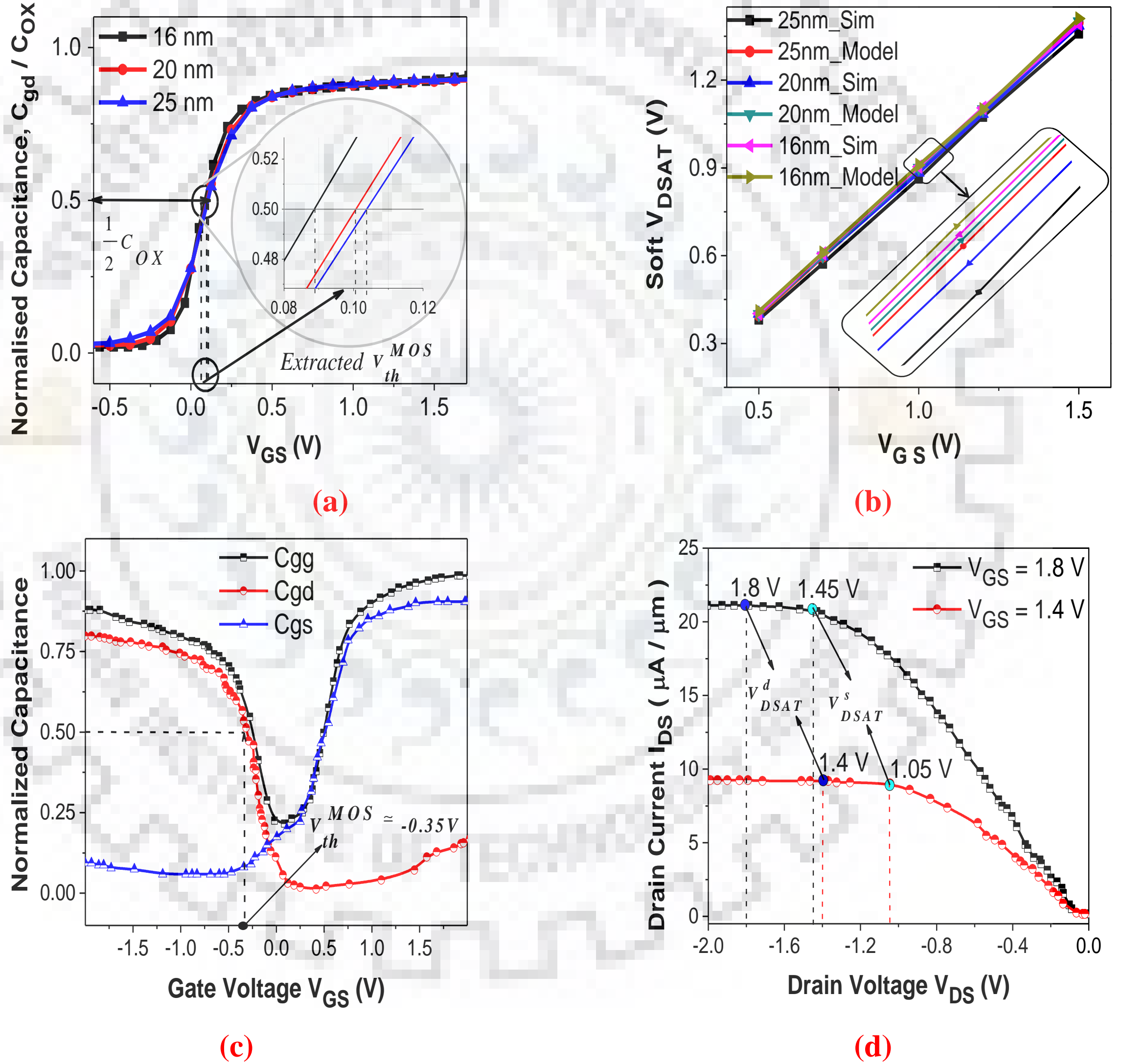


Figure 3.3: (a) Extraction of V_{th}^{MOS} from C_{gd}–V_{GS} curve for V_{DS} = 0 V. Inset shows V_{th}^{MOS} for different NWTFET diameters. Validation of the proposed method with the (b) Numerical TCAD simulations and experimentally measured (c) C–V_{GS} (d) I_D–V_{DS} curve of a *p*-type device show a good match between the proposed and the experimental data.

As discussed in the previous sub-section, the constant voltage difference V_{DSAT}^{s} is actually the threshold voltage of the gate-channel-drain MOS system in the NWTFET. In order to extract the accurate value of drain voltage (V_{DSAT}^{s}) at the onset of *soft* saturation, a fundamental phenomenological explanation ($\Psi_S + V_{OX} = V_{GS}$) of the threshold voltage for the MOS system [110] is used, where V_{OX} is the drop across oxide. It states that Ψ_S and V_{OX} are the specific fractions of V_{GS} when strong inversion is reached in the channel. The first derivative of the term $\Psi_S + V_{OX} = V_{GS}$ with respect to the applied gate bias is always unity.

The term $\frac{dVox}{dVGS}$ dominates in the relation $\frac{d\Psi s}{dVGS} + \frac{dVox}{dVGS}$=1, after the attainment of strong inversion. This directly translates into the fact that the TFET gate-drain capacitance (C_{gd}) can be expressed as a specific fraction of the oxide capacitance (C_{OX}) when the strong inversion is reached in the channel of TFET. We have found that the gate bias for which strong inversion is attained (V_{th}^{MOS}) in the channel of a TFET, can be extracted from C_{gd}–V_{GS} characteristics at zero drain bias, as shown in Fig. 3.3(a).

We also observe that the constant voltage difference V_{GD}^{s} is equal to the value of V_{GS}, when C_{gd} becomes half of C_{OX}. This is also the threshold voltage MOS system (V_{th}^{MOS}) [Fig. 3.3(a)]. Therefore, V_{GD}^{s} is found to be equal to V_{th}^{MOS}; $V_{GD}^{s} = V_{GS} - V_{DSAT}^{s}$. Furthermore, *deep* saturation condition in the target device is attained when V_{DS} becomes equal to V_{GS}, and hence the constant voltage difference V_{DSAT}^{d} remains always zero [Table 3.1]. It may be noted here that C_{gd} is always a dominating component of total gate capacitance in lateral tunneling based TFETs [39], [51].

Table 3.1 verifies the aforesaid observations that V_{DSAT} varies linearly with V_{GS}. Further, the voltage difference V_{GD} always remains constant with V_{GS} at the onset of both *soft* and *deep* saturation regimes [Fig. 3(b)]. Therefore, our method is readily usable for biasing an analog circuit using TFETs, as discussed later in Section 3.5. The proposed method for calculating V_{DSAT} for a TFET in this study is also consistent for other nanowire diameters [Fig. 3.3(a)-(b)] and homo-junction TFETs. The close agreement of our modeled data with numerically simulated TCAD results [Fig. 3.3(b)], assures the accuracy of our V_{DSAT} extraction method.

For completeness of work, our results are also validated against the experimentally measured characteristics of a *p*-type $Ge_{0.958}Sn_{0.042}$ TFET [19], as shown in Fig. 3.3(c)-(d). It is found that our method accurately calculates the values of V_{DSAT} for the set of measured data, as depicted in Fig. 3.3(d). Please note that the model and the definitions of *soft/deep* saturation

advanced in this chapter are general in nature. As discussed in the next section, if the drain (source) doping is increased, the *soft* saturation voltage increases (negligibly decreases) for the TFET device. Further, an increase in the gate-drain underlap also reduces the V_{DSAT} values. The doping and gate underlap dependence of V_{DSAT} is due to the modulation of channel charge.

TABLE 3.1

COMPARISON OF THE PROPOSED TECHNIQUE WITH REF. [92], [40] AND [105]

V_{GS} (V)	**Ref.[92]**	**Ref. [40]**	**Ref. [105]**	***Soft* Sat.**	***Deep* Sat.**
	$V_{DSAT}(V_{GD})$	$V_{DSAT}(V_{GD})$	$V_{DSAT}(V_{GD})$	$V_{DSAT}(V_{GD})$	$V_{DSAT}(V_{GD})$
0.5	0.45(0.05)	0.364(0.136)	0.38 (0.12)	0.396(0.104)	0.50(0)
0.75	0.82(-0.07)	0.568(0.182)	0.50 (0.25)	0.646(0.104)	0.75(0)
1.0	1.2(-0.2)	0.716(0.282)	0.75 (0.25)	0.896(0.104)	1.00(0)
1.5	1.7(-0.2)	1.123(0.377)	1.125(0.375)	1.376(0.104)	1.50(0)

3.4 Impact of device design parameters on V_{DSAT}

After having discussed physics based understanding of the output current saturation in TFETs, this section elaborates the impact of various device design parameter on V_{DSAT}. These parameters include channel length, gate-drain underlap, nanowire diameter, and source/drain doping. This study is important from the perspective of TFET based circuit design, as the saturation voltages may change with the device design parameters.

3.4.1 Impact of short channel length on V_{DSAT}

The drive currents in TFETs are almost independent of the channel lengths. At extremely short channel lengths (sub-20 nm), the drain-induced barrier thinning (DIBT) is more pronounced in TFETs. It degrades the saturation in the output characteristics [108]. The physics behind this phenomenon is similar to DIBL in MOSFETs and resulting due to the influence of the V_{DS} on the source-channel tunnel junction. Therefore, at sub-20 nm channel length, an increase in V_{DS} results in a very gradual decrease in the conduction band energy of channel (E_{CC}) beyond its *deep* saturation point ($V_{DSAT}^{d} = V_{GS}$). The value of E_{CC} does not effectively pin to a specific value, as shown in Fig. 3.4(a). Furthermore, the height of tunneling window is also affected by drain bias beyond deep saturation.

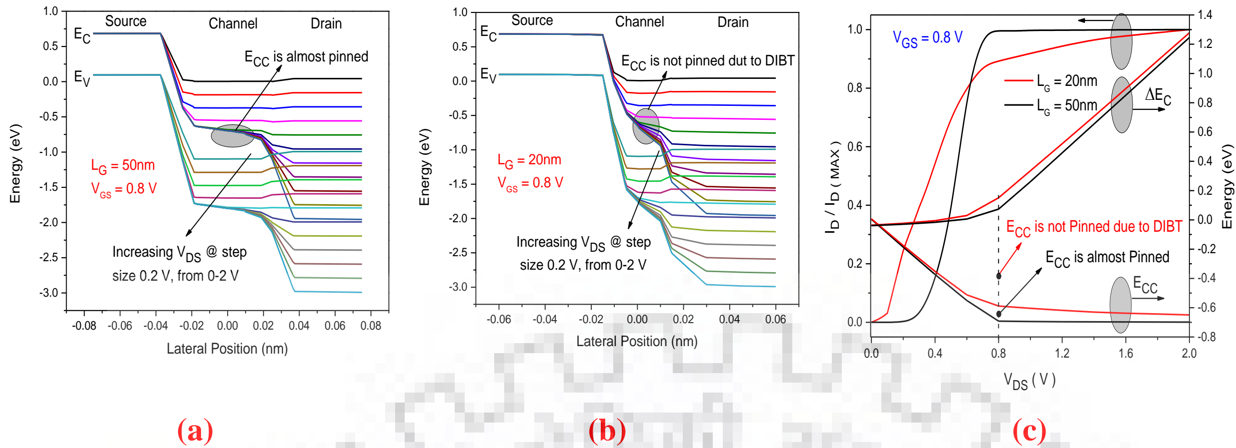


Figure 3.4: Energy band for *SiGe/Si* hetero-junction Nanowire Tunnel FET (a) 50 nm channel length (b) 20 nm channel length. It is shown that E_{CC} decreases gradually with increase in V_{DS} even after *deep* saturation condition for short channel TFETs. (c) Imperfect saturation results in short channel TFETs due to pronounced effect of DIBT.

However, as with the long channel TFETs, in short channel TFETs too, ΔE_C becomes non-zero at the onset of saturation and increases for further increase in V_{DS}. However, DIBT does not affect the value of V_{DSAT}; rather this phenomenon is impacted only by the relative change in the channel's potential and hence it is similar for the long as well as short channel lengths. In addition, for the shorter channel TFETs, the saturation in output characteristics is worsened [Fig. 3.4(c)], thereby the output resistance and intrinsic gain also degrades. It may be noted that short channel (sub-20 nm) TFETs are suitable for digital applications, while long channel TFETs are most suitable for the analog design due to the reduced impact of DIBT, therefore the benefits in terms of output resistance and intrinsic gain can be fully exploited.

3.4.2 Impact of gate-drain underlap on V_{DSAT}

The gate-drain underlap [Fig. 2.1 (a)] is a promising technique to suppress the ambipolar behavior in TFETs [111], [112] due to a reduction in the drain side tunneling. However, C_{gd} is reduced when a gate-drain underlap is used, therefore, the value of V_{th}^{MOS} increases from 104 mV to 187 mV (as measured from our method). This happens as the electrostatic control of the gate becomes weaker over the underlap portion of the channel, thus, a higher gate bias is required to achieve the strong inversion in the channel. Further, the onset of *soft* saturation happens in advance (V_{DSAT}^{S} = 0.813 V), when compared to V_{DSAT}^{S} (0.9 V) without gate-drain

underlap. The value of V_{DSAT} in the *deep* saturation is still equal to the gate bias due to the reasons explained in the last section.

3.4.3 Impact of source/drain doping on V_{DSAT}

The source doping is one of the key device design parameters in TFETs. The validity of our proposed method for V_{DSAT} extraction against the variation in source/drain doping is also studied. Three different devices D_1, D_2, and D_3 with *p*-type source (*n*-type drain) doping values of 10^{20} (5×10^{18}), 4×10^{20} (5×10^{18}) and 10^{20} (10^{20}) respectively are considered. Please note that all other parameters are kept same as explained in Section 3.2, other than the doping values. A high source doping results in a source degeneracy and an increase in the junction electric field [113], [114], which eventually increases the drain current. It is interesting to note that the value of V_{DSAT}^{s} is not much affected by changing the source doping, as V_{th}^{MOS} of TFET is independent of the source doping [Fig 3.5(a)]. However, it increases the drive capability of the device.

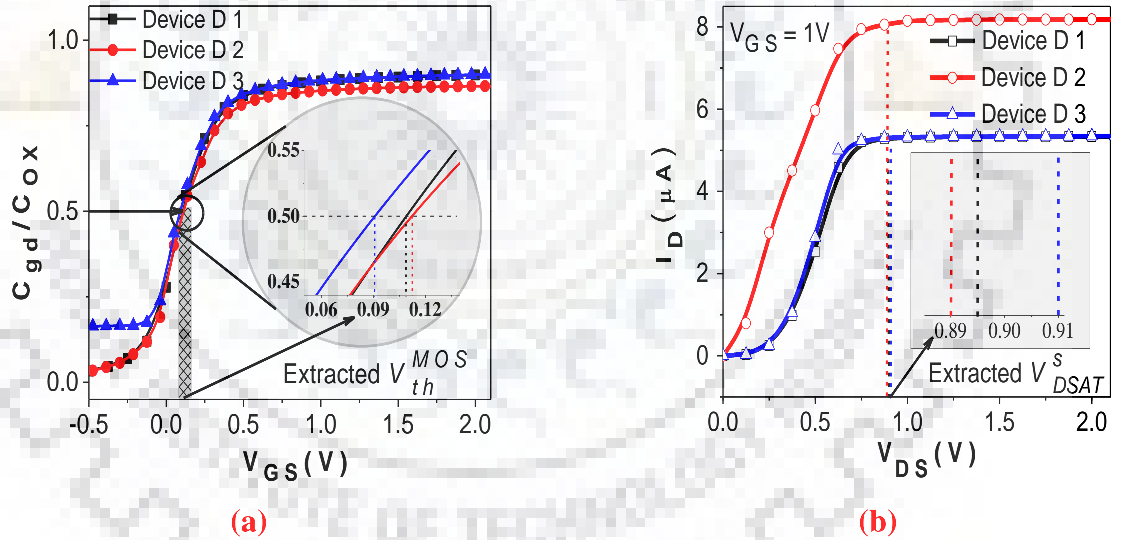


Figure 3.5: (a) Variation in gate-drain capacitance with V_{GS} for V_{DS} = 0V. The dotted line shows the extracted values of V_{th}^{MOS} for device $D1$, $D2$ and $D3$. (b) I_D-V_{DS} characteristics show the value of *soft* and *deep* V_{DSAT}.

Unlike the higher source doping, a higher drain doping results in I_D remaining essentially unchanged because the tunneling current remains almost unaffected [40]. However, V_{DSAT}^{s} increases (or V_{th}^{MOS} reduces) as more inversion carriers diffuse from the drain to channel [Fig.

3.5(b)]. As explained above, a delayed saturation happens due to the decrease in V_{th}^{MOS} when drain doping is increased. Further, there is no change in V_{DSAT}^{d} since it is caused by the attainment of a *flatband* condition in the gate-channel-drain MOS system [Section 3.3].

3.4.4 Impact of nanowire diameter on V_{DSAT}

As the diameter of the nanowire is reduced, the electrostatic control of the gate over the channel is enhanced. This is due to the penetration of vertical electric field into the channel. Further, the gate voltage required for the strong inversion in the channel of the nanowire is also reduced for small nanowire diameter. In turn, this increases the onset of the *soft* saturation in TFETs. This is because a higher V_{DS} is required to deplete the channel charge for a given V_{GS}. Hence, the pinning of E_{CC} in 20 nm diameter occurs at the higher V_{DS} than 25 nm diameter. As a consequence, the value of ΔE_C remains low for the smaller nanowire diameter. This also causes a delay in the output current saturation in TFETs. The *deep* saturation is always defined as flat band voltage when $V_{DS} = V_{GS}$ and $V_{GD} = 0$. The early onset of *soft* saturation is always desirable from the analog design point of view, as discussed in Section 3.5. Table 3.2 discloses the important conclusions about the variation in nanowire diameter on the output current saturation.

TABLE 3.2

EXTRACTED VALUE OF V_{th}^{MOS} AND V_{DSAT}^{s} AT $V_{GS} = 0.5$V FOR NWTFET

NW Diameter	Si Source		$Si_{0.5}Ge_{0.5}$ Source	
	V_{th}^{MOS} (V)	V_{DSAT}^{s} (V)	V_{th}^{MOS} (V)	V_{DSAT}^{s} (V)
25 nm	0.111	0.389	0.104	0.396
20 nm	0.108	0.392	0.100	0.400
16 nm	0.100	0.400	0.89	0.411

3.4.5 Impact of hetero/homo-junctions on V_{DSAT}

The source material engineering is one of the prominent design parameter in TFETs based circuit design. Please note that *Silicon* homo-junction based devices suffer from the low drive currents. From last few couples of year, *SiGe*, *Ge,* and *GeSn* based group IV material are widely exploited as source material apart from group III-V based materials. In this study, only the source material is changed from $Si_{0.5}Ge_{0.5}$ to *Si*. We observe that the homo-junction based

TFET saturates relatively in advance than the *SiGe-Si* hetero-junction. The strong inversion in the channel of homo-junction TFETs occur at relatively higher gate voltage than the hetero-junction TFETs. This is due to fact that there is an abrupt decrease in the bandgap of *SiGe-Si* based hetero-junction. Furthermore, there is a prominent effect of direct and indirect BTBT in *Germanium* based devices [43]. Nevertheless, the value of drive current always increases with increasing *Germanium* content in the source due to the favorable energy bands for tunneling.

3.5 Implications of Proposed V_{DSAT} Extraction Technique to the Analog Circuit Design

This section investigates suitable bias conditions to design an active load Common Source (CS) amplifier, based on our proposed method, using 3D-TCAD *mixed-mode* simulations. As it is shown in Fig. 3.2 (b)-(c), that $g_m \times r_o$ (C_{gd}) increases (decreases) in *soft* saturation regimes and attains a maximum (minimum) value beyond *deep* saturation voltage. When $V_{DS} \geq V_{DSAT}^{d}$ ($\Delta E_C \geq 3K_BT$), E_{CC} remains pinned while E_{CD} keeps on moving down, resulting in an increase in the drain channel barrier. This causes $g_m \times r_o$ (C_{gd}) to attain a maximum (minimum) value in *deep* saturation [Fig. 3.2].

We now discuss the importance of the above observations on the biasing of a CS amplifier [inset of Fig. 3.6(b)]. The device structure and doping profiles for the *p*-device is kept same as that of the *n*-device except that an opposite doping is used for different regions of the *p*-device. The drive currents of both the *n* and *p*-type devices are adjusted to be equal by tuning the work function of the gate metal. Fig. 3.6(a) shows the voltage transfer characteristics (VTC) for different value of the gate bias of *p*-type load transistor (V_{bias}). The boundaries for the onset of the *soft* and *deep* saturation regimes are determined from the V_{DSAT} extraction method discussed in the Section 3.3.

The value of maximum voltage gain (A_V) increases with an increasing value of V_{bias}. This happens as both the transistors are operating in the saturation regimes for a wider range of the output voltage. Thus, the r_o of the load transistor increases with increasing value of V_{bias}. It is evident [Fig 3.6(a)] that the gain can be maximized through an appropriate selection of bias voltages which would ensure that both the transistors operate in *deep*/*soft* saturation regime simultaneously. Therefore, an estimation of V_{DSAT}^{s} is important from the point of view of amplifier biasing.

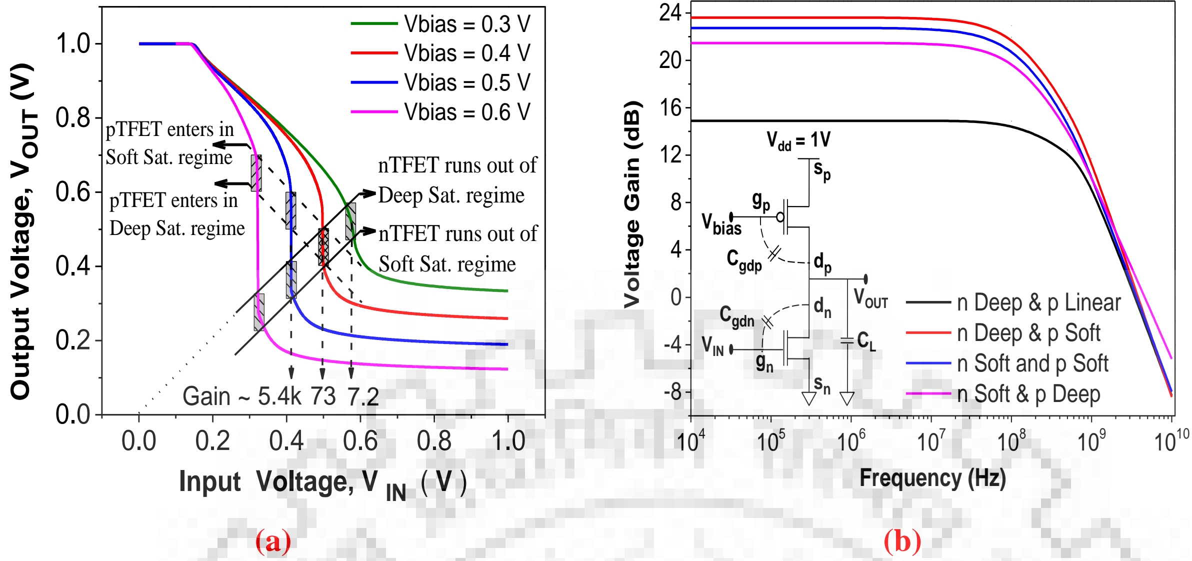


Figure 3.6: (a) VTC for different values of V_{bias}. Shaded areas on VTC show the boundaries for the *soft* and *deep* saturation regimes for *n* (*p*) device. The value of maximum voltage gain corresponding to each VTC is also shown. (b) The frequency response of a CS amplifier for a fixed V_{bias} (0.4 V), and the value of C_L is selected as 5×10^{-17} F. Inset shows schematic of Common Source amplifier.

Finally, the frequency response of a common source amplifier is plotted in Fig. 3.6(b). It is clearly shown that the maximum value of voltage gain is achieved when both the devices are either in *soft* or *deep* saturation regimes and hence their output resistance is maximized. The common source amplifier offers a maximum A_V of 23.62 dB when *n* (*p*) device is biased in the *deep* (*soft*) saturation regime, whereas the almost similar value of the maximum voltage gain (22.74 dB) is obtained when both the devices are biased in *soft* saturation regimes. In contrast to this, the value of maximum voltage gain (14.9 dB) reduces significantly when the *p*-device is biased in the linear regime (hence the output resistance decreases), as evident from Fig. 3.6 (b).

Moreover, it is interesting to note that the bandwidth of the common source amplifier remains almost same (~2×10^{8} Hz) when both the devices are biased either in the *soft* or *deep* saturation regimes because the C_{gd} attains a minimum and r_o attains a maximum value. Therefore, both the gain and bandwidth are optimized in the *soft* saturation regime. It may be noted that the common source amplifier offers a higher bandwidth (~6×10^{8} Hz) [Fig. 3.6(b)] when the *p*-type load is biased in the linear region, where it exhibits a lower value of R_o and higher value of C_{gd}.

3.6 Conclusion

We have proposed a novel V_{DSAT} extraction method to estimate the onset of *soft* and *deep* saturation voltages for the lateral tunneling based hetero/homo-junction TFETs. The proposed method is further validated through the numerical 3D-TCAD simulations and experimental data. It is found that V_{GD} remains constant in both the *soft* and *deep* saturation regimes. Furthermore, a detailed investigation regarding the influence of ΔE_C on the analog performance of the device is performed with an in-depth explanation of the inherent physical mechanisms. The total gate capacitance remains at a minimum in the *soft*/*deep* saturation and hence a high bandwidth is expected for the amplifier. The impact of various device design parameters on V_{DSAT} is also examined. The design space for a common source amplifier reveals that the amplifier exhibits acceptable values of the voltage gain and bandwidth in the *soft* saturation regimes like the one observed in *deep* saturation regime. The physics discussed here is focused on general trends and is useful for developing a future analytical model for the analog circuit design using TFETs.

Chapter 4

Drain Current Saturation in Line Tunneling based TFETs: an Analog Design Perspective

In the previous chapter, an extraction method of V_{DSAT} was discussed for the point tunneling devices. This chapter highlights the output current saturation in a line tunneling based Tunnel FET (L-TFET). Thereafter, a novel method to extract the onset of saturation voltage (V_{DSAT}) for L-TFET is proposed for the first time. A *soft* saturation state is attained when the electron density in the epitaxial layer over the source (EoS) region saturates with the drain bias (V_{DS}) and the conduction band energy (E_C) gets pinned. In addition, at the onset of *deep* saturation, the electron density in the epitaxial layer over the channel (EoC) region drops below its doping level and E_C becomes invariant for any further increase in V_{DS}. The difference between gate-drain biases (V_{GD}) is found to be a constant at the onset of saturation and remains independent of the gate-source overlap lengths (L_{OV}). A shift in V_{DSAT} and V_{GD} is also observed with a change in the thickness and doping of the epitaxial layer. The transconductance and output resistance are reasonably good in the *soft* saturation regime. Furthermore, a nominal change of ~ 5% in the voltage gain (A_V) of a Common Source (CS) amplifier is observed when the *n*-device is either biased in *soft* or *deep* saturation regime, without any trade-off in the bandwidth.

4.1 Introduction

The journey of Tunnel FET for improving the drive current and the subthreshold swing has led to the proposal of many novel device architectures [115]. An optimization of the device structure and the source/channel material are strongly being pursued. The line tunneling structures with the gate overlapping the low band gap source, are notably one of the best candidate in this regard [116], [117]. The term line tunneling is also rephrased by researchers as vertical tunneling or area scaled tunneling [118], [119] whereby, the band-to-band tunneling (BTBT) takes place by the gate normal electric field. Therefore, the effective cross-section area

for BTBT is increased. In spite of the high ON-state current (I_{ON}) and small subthreshold swing (SS), the gate overlapping the source structures suffer from the delayed onset of tunneling [32], [124]. Thus, a higher gate bias (V_{GS}) is required to initiate the tunneling process within the source region. Recently, epitaxial layer and counter doped source pocket L-TFETs are being explored [30], [32], [35], [124]–[127]. These enable tunneling at low V_{GS} and are more suitable for low power / low voltage applications.

Further, it has been established as a fact that the doping (n_{EPI}) and thickness (t_{EPI}) of the epitaxial layer/source pocket are vital parameters in the line tunneling for low voltages operation ($V_{DD} \leq 0.5$). The impact of quantum confinement and interface traps on the line tunneling are also reported in some studies [124]–[126]. TFETs for the analog applications are also being investigated by the research community for last few years [98], [109]. Although the drain current saturation in point tunneling based TFETs has been discussed [68], [114], [115], [131], [132]. However, those explanations cannot be applied to L-TFET, by virtue of its different tunneling mechanism and gate capacitances, as discussed in subsequent sections. Therefore, The saturation of drain current (I_D) with V_{DS} for L-TFETs and the performance of analog parameters in the saturation regime, are yet to be discussed systematically.

This chapter, while addressing the problem discussed above, investigates the physics behind the onset of saturation in the line tunneling based TFET structures. In addition, we also propose a novel method to extract the saturation drain voltage (V_{DSAT}) for L-TFETs. The output current saturation in L-TFET is attributed by the saturation of electron density in the epitaxial region under the gate with increasing value of V_{DS} as discussed later in detail. Therefore, in the L-TFETs, the carrier action at the gate overlapped source region is fairly important. Moreover, this work is also intended towards the impact of V_{DS} on analog matrices like the transconductance (g_m), output resistance (r_o), intrinsic gain, and gate capacitances (C_{gd}, C_{gs}). Besides, this work also quantifies the analog device/circuit performance and presents optimization guidelines for L-TFETs, by considering the impact of device design parameters. The significance of our V_{DSAT} formulae for the *soft*/*deep* saturation regimes, and the improved circuit performance while using these, are also discussed. The voltage gain of an amplifier, when the L-TFET is biased in the *soft* saturation regime, is merely 5% smaller than that in the *deep* saturation regime, while the bandwidth (BW) is almost unaffected. The design of L-TFET amplifiers biased in *soft* saturation regime and thus increasing the signal swings is also enabled through this work.

This chapter is organized as follows. In Section 4.2, the device structure, simulation framework, and calibration approach are presented. The physics of saturation in L-TFETs along with V_{DSAT} extraction is explained in Section 4.3. The impact of variation in the device design parameters on the saturation is discussed in Section 4.4. The device design guidelines and design space for a CS Amplifier are presented in Section 4.5. Section 4.6 discloses the impact of device design parameters on the device/circuit analog performance, followed by the conclusion in Section 4.7.

4.2 Device Structure and Simulation Framework

The device structure under consideration [Fig. 4.1(a)] is based on a recent and improvised Si/SiGe based hetero-junction [27]. It consists of a 3 nm epitaxial layer thickness (t_{EPI}) of Silicon over the source and channel. The source material is chosen as Si_XGe_{1-X} to obtain a high drive current as per ITRS norms [117]. The *germanium* content is kept at 50% to assure a defect free source region [28]. A high-κ metal gate stack with a dielectric layer of 3 nm $HfO_2$is selected for better electrostatic control of the gate over the tunnel junctions. The work function of gate electrode is tuned to 4.15 eV [27]. The length of the channel (L_C) and epitaxial layer is 20 nm and 40 nm, respectively. The gate-source overlap length (L_{OV}) of 20 nm is considered in this Chapter to enable line tunneling between the source and epitaxial regions. The doping concentration of source (*p*-type), drain (*n*-type), channel (*p*-type) and epitaxial layer (*n*-type) is kept at 2×10^{20}, 5×10^{19}, 10^{16} cm^{-3} and 2×10^{18} respectively, unless otherwise stated. Our self-consistent numerical simulations are performed using Sentaurus TCAD tool. The details of various physical models and their description are same, as mentioned in the Chapter 3.

4.3 Insights of the Output Current Saturation and Proposed V_{DSAT} Extraction Method

This section explains the physics behind the output current saturation in *n*-type L-TFETs. Thereafter, a method to extract the V_{DSAT} for L-TFET is proposed for the first time. The saturation in output characteristics is governed by the electrostatics of two distinct regions in the device. First is the epitaxial layer over the heavily doped *p*-type source (EoS) and the other is epitaxial layer over the intrinsic channel (EoC). The physics discussed here also holds for the *p*-type L-TFET and the other line tunneling based TFET structures. Please note that the values

of band energies, surface potential, and electron density may vary with the position of x_1, x_2 and x_3, but the underlying physics remains the same.

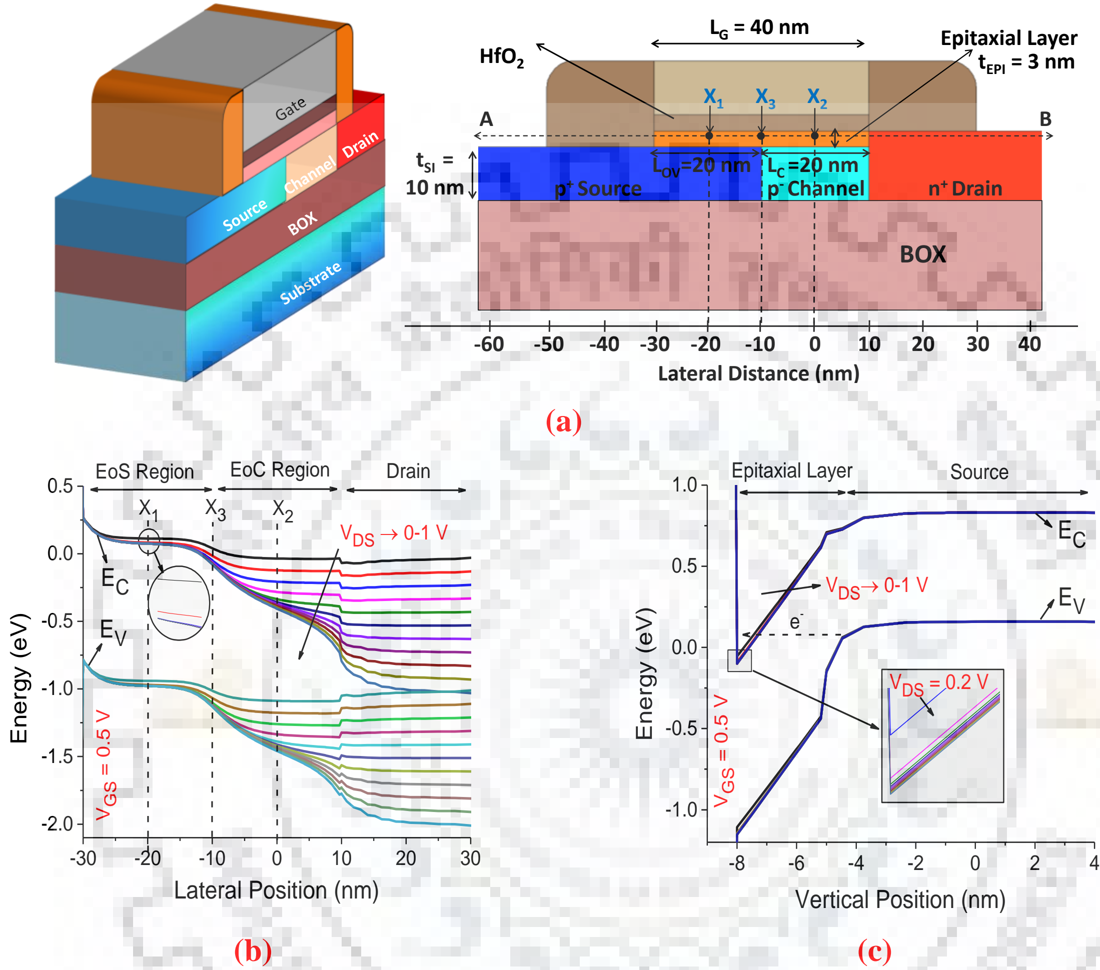
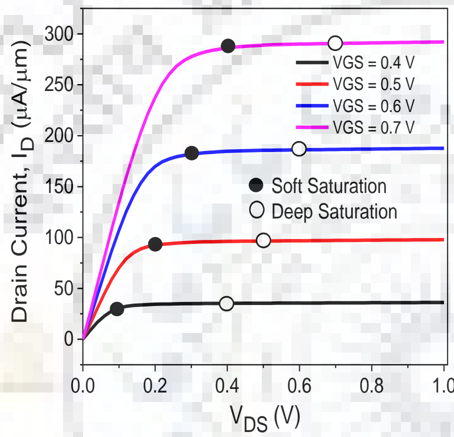


Figure 4.1: (a) 3-D view and 2-D schematic of the target device. (b) Lateral energy bands across the line AB. (c) Vertical energy bands across the EoS region show the tunneling at point x_1. The points x_1, x_2, and x_3 are kept at 1 nm below the oxide-semiconductor interface along the line AB as depicted by dotted lines.

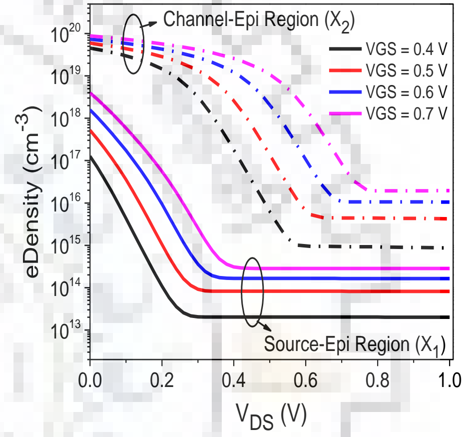
4.3.1 Output current saturation mechanism

The output characteristics for the target device are shown for different gate biases [Fig. 4.2(a)]. It is evident from Fig. 4.2(a) that a near perfect saturation is observed in the device. The output current saturation depends upon the variation of E_C (and hence Ψ_S) with V_{DS}. For a given value of V_{GS}, when V_{DS} increases, initially the electron density decreases in the EoS region (point x_1 [Fig. 4.1(a)]). After certain V_{DS}, this becomes independent of any further

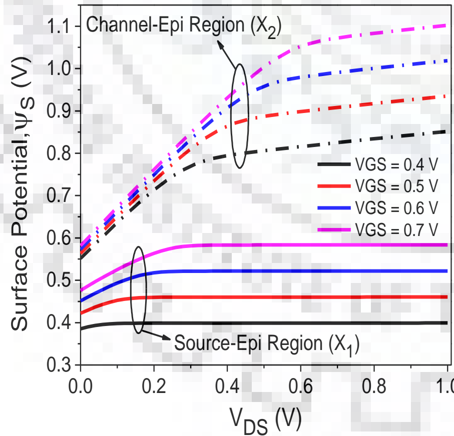
increase in V_{DS}, as shown in Fig. 4.2(b). This voltage is called the *soft* saturation voltage (V^{s}_{DSAT}). This happens because E_C of the EoS region gets pinned to a specific value with increasing V_{DS}, beyond the *soft* saturation voltage [Fig. 4.1(b)-(c)]. This pinning is because of an almost complete depletion of the EoS region, resulting from a reverse bias at the EoS junction (np^+-junction). Thus, Ψ_S also gets pinned, as shown in Fig. 4.2(c). Moreover, the tunneling distance starts to saturate and becomes almost independent of any further increase in V_{DS}, as depicted in Fig. 4.2(d). Consequently, the difference between the gate and drain bias at the onset of *soft* saturation (V^{s}_{GD}) corresponds to a constant value, as discussed later.



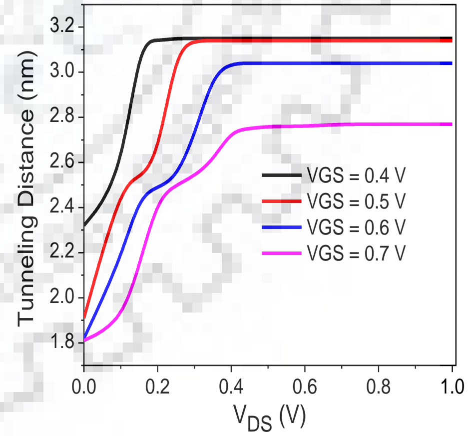
(a)



(b)



(c)



(d)

Figure 4.2: (a) I_D-V_{DS} characteristics showing near perfect saturation in L-TFETs. *Soft* and *deep* saturation voltages are marked for different V_{GS} (b) Electron density and (c) Surface potential in the epitaxial region at points x_1 and x_2. (d) Tunneling distance is extracted from TCAD simulations, and measured between the junction formed by source and epitaxial layer.

It is worthy to mention here, that the *soft* saturation condition in the device depends upon the carrier action in the EoS region. In addition, after the onset of *soft* saturation, V_{DS} loses its control over the EoS region. Although, a negligible influence of V_{DS} can be seen beyond V_{DSAT}^{s} (0.2 V) on the E_C of the EoS region [inset Fig. 4.1(c)], due to small change in the electric field. Therefore, I_D increases with a retarded tempo with the increasing V_{DS}, as shown in Fig. 4.2(a). As V_{DS} is increased beyond V_{DSAT}^{s}, the electron density in the EoC region (point x_2 [Fig. 4.1(a)]) continuously decreases. Then, it reaches below the doping level of the epitaxial region, i.e. this region is depleted of the carriers, as shown in Fig. 4.2(b). Besides, the electron concentration near the drain end is greatly reduced at this point, as confirmed by the band diagrams of Fig. 4.1(b). This voltage is defined as the *deep* saturation voltage (V_{DSAT}^{d}). Beyond V_{DSAT}^{d}, the electron density rapidly drops and then saturates [Fig. 4.1(c)]. This happens because E_C in the EoC region (points x_2 and x_3) gets almost independent of V_{DS} [Fig. 4.1(b)] and hence Ψ_S also gets pinned, as shown in Fig 4.2(c). It may be noted that the tunneling distance remains invariant with V_{DS} in *deep* saturation region as depicted in Fig. 4.2(d). At the onset of *deep* saturation, the pinning of E_C in the EoC region leads to an almost zero difference between the gate and drain bias voltages, as the pinning starts to occur at $V_{GS} \approx V_{DS} = 0.5$ V [Fig. 4.1(b)]. It is also evident from the trends of electron density and Ψ_S, that V_{DS} effectively loses its control on these parameters after the attainment of *deep* saturation condition in the device.

4.3.2 Proposed V_{DSAT} extraction technique for L-TFET

This section explains an extraction method of V_{DSAT} for the line tunneling based TFETs. As discussed in the previous subsection, the gate-drain bias (V_{GD}) has unique constant values at the onset of both the *soft* and *deep* saturation conditions. We observe from rigorous simulations, that this constant value of V_{GD} remains invariant with changes in L_{OV}. In other words, V_{DS} at which the depletion in the EoS region beings to occur does not modify with the varying L_{OV}, as shown in Fig. 4.3(a). This is because the potential drop in the EoS region remains constant, resulting in a constant potential at point x_3 (Fig. 4.1(a)) with respect to V_{GS}. Since, the EoC region has a higher carrier concentration; the potential of the point x_3 is determined by V_{DS}. Therefore, the depletion of EoS region starts at a constant V_{GD}. Accordingly, E_C and Ψ_S in the EoS region also remain almost independent of any change in L_{OV} after the onset of *soft* saturation [Fig. 4.4(a)]. The gate-drain capacitance C_{gd} is determined by the gate control of the

charges in the EoS as well as EoC regions. After the onset of *soft* saturation, the contribution of the EoS region to this capacitance becomes negligible. As a consequence, the value of C_{gd} for different values of L_{OV} remains equal after the onset of *soft* saturation, for a given value of V_{GS} [Fig. 4.3(a) and 4.9(d)].

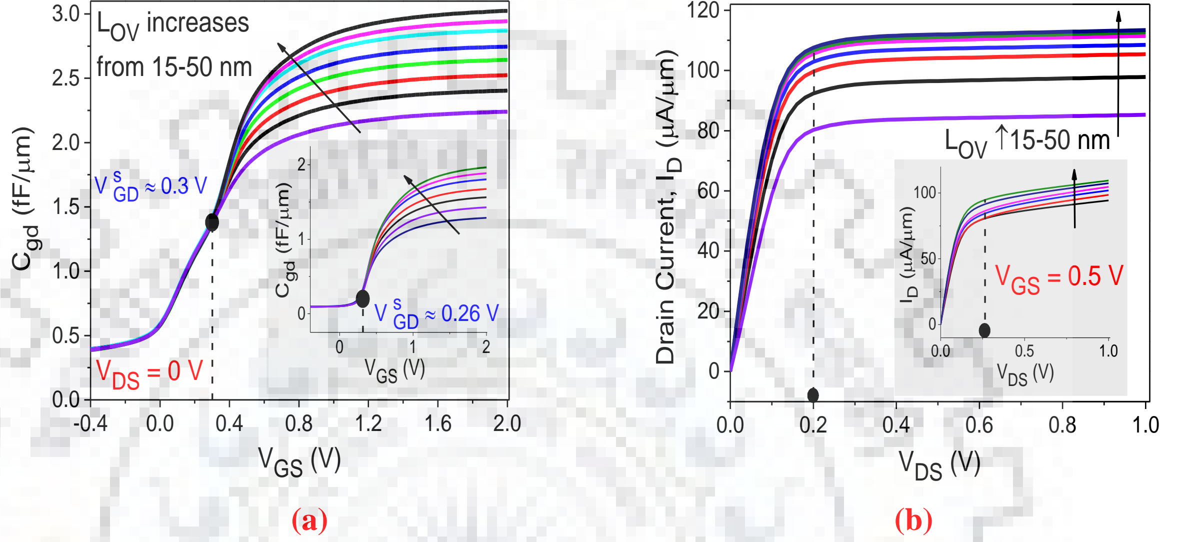


Figure 4.3: (a) Extraction of V_{GD}^{s} from C_{gd}-V_{GS} curve at V_{DS} = 0 V. V_{GD}^{s} remains constant with the increasing L_{OV} from 15-50 nm at the step size of 5 nm. Inset shows C_{gd}-V_{GS} curve for the device having non-gated ($L_G = L_{OV}$) intrinsic region. (b) The output characteristics show that the value of $V_{DSAT}^{s,d}$ is invariant of the overlap lengths L_{OV}. Device without gate-channel overlap shows slight distortion in saturation characteristics [Inset of (b)].

Next, the constant value of V_{GD} at the onset of *soft* saturation (V_{GD}^{s}) can be extracted as follows: Keeping V_{DS} = 0, if V_{GS} is increased, initially the carrier (electron) concentration in the EoC region increases while the EoS region remains depleted. This results in a value of C_{gd}, which is independent of L_{OV} till $V_{GS} = V_{GD}^{s}$ [Fig. 4.3(a)]. Therefore, for $V_{GS} \leq V_{GD}^{s}$, the values of C_{gd} at different values of L_{OV} remain equal with varying V_{GS}. After this voltage (V_{GD}^{s}), when the electron concentration in the EoS region becomes significant, C_{gd} for the different values of L_{OV} separates out. This value of V_{GD}^{s} can be extracted by obtaining C_{gd}-V_{GS} characteristics for various values of L_{OV} at V_{DS} = 0, as shown in Fig. 4.3 (a). The value of V_{DS} at the onset of *soft* saturation is defined as $V_{DSAT}^{s} = V_{GS} - V_{GD}^{s}$. It is worth highlighting here, that the maximum value of C_{gd} in the L-TFET is less than the oxide capacitance, as also pointed out in [127]. This is because the electron density in the EoS region is limited by its np^{+}-junction, unlike that in the

EoC region (np^- junction) as shown in Fig. 4.2(b). In contrary to this, the maximum value of C_{gd} in point tunneling based TFETs almost equals the oxide capacitance at $V_{DS} = 0$, whereas, C_{gs} is negligibly small. Further, the onset of *deep* saturation is defined as the amount of V_{DS} required to deplete the EoC region, as discussed in previous subsection. It occurs when V_{DS} is almost equal (slightly less than) the value of V_{GS} [Fig. 4.1(b)]. Therefore quantitatively, $V_{DSAT}^{d} \approx V_{GS}$ and V_{GD}^{d} remains almost zero. Please note that these values of $V_{DSAT}^{s,d}$ are least affected by the inclusion of contact resistances.

The validation of our method is done against the numerically simulated data obtained from Sentaurus TCAD. It is observed that V_{GD}^{s} obtained using our physics based method exhibits a good match with the simulation results [Fig. 4.2(a)-(d)]. In addition, the method explained above is also experimentally feasible, because the variation in L_{OV} can be easily controlled with suitable mask lengths. Thus, the on-chip measurement of V_{GD}^{s} (and hence V_{DSAT}^{s}) from C_{gd}-V_{GS} curve for different values of L_{OV} is straightforward [Fig. 4.3], and is useful for analog designers. Our method is also applicable for the non-gated devices [gate does not overlap intrinsic p^- region, i.e. $L_G = L_{OV}$ and L_C is the length of the non-gated in Fig. 4.1(a)], as shown in the inset of Fig. 4.3(a)-(b). The values of V_{DSAT}^{s} get slightly changed with the change in the length of the non-gated region. This is attributed to the modification in C_{gd} and the channel resistance of the non-gated region which actually modulates with varying length of this non-gated region. It is suggested to keep the non-gated length to a moderate value (20-25 nm), so that a suitable value of both I_{OFF} and I_{ON} can be obtained. However, the saturation characteristics worsen with increasing the length of non-gated region [Fig. 4.3(b)].

4.4 Impact of L-TFET Structural Variation on V_{DSAT}

This section explains the impact of variation in the device design parameters of L-TFET, viz. L_{OV}, n_{EPI}, and t_{EPI} on the drain current saturation (and hence on V_{DSAT}). These parameters have been widely explored to optimize the device for obtaining the higher values of I_{ON} and smaller SS.

4.4.1 Impact of the gate-source overlap length (L_{OV})

In this study, L_{OV} is changed, while keeping all the other parameters same as mentioned in Section 4.2. An increase in L_{OV} increases the effective cross-section area for BTBT, and hence I_{ON} also increases. However, the onset of *soft* saturation remains invariant with increasing L_{OV},

as shown in Fig. 4.3(a)-(b). As explained in the previous subsection, the depletion in devices with different L_{OV} takes place for an equal value of V_{GD} [Fig. 4.4(a)]. Thereafter, the carrier density in EoS region settles to negligible and a minimum value [Fig. 4.4(a)]. Thus, the pinning of Ψ_S occurs at same V_{DS} for L-TFETs having different L_{OV}. This causes V_{DSAT}^{s} to remain invariant with L_{OV} as shown in Fig. 4.4(b).

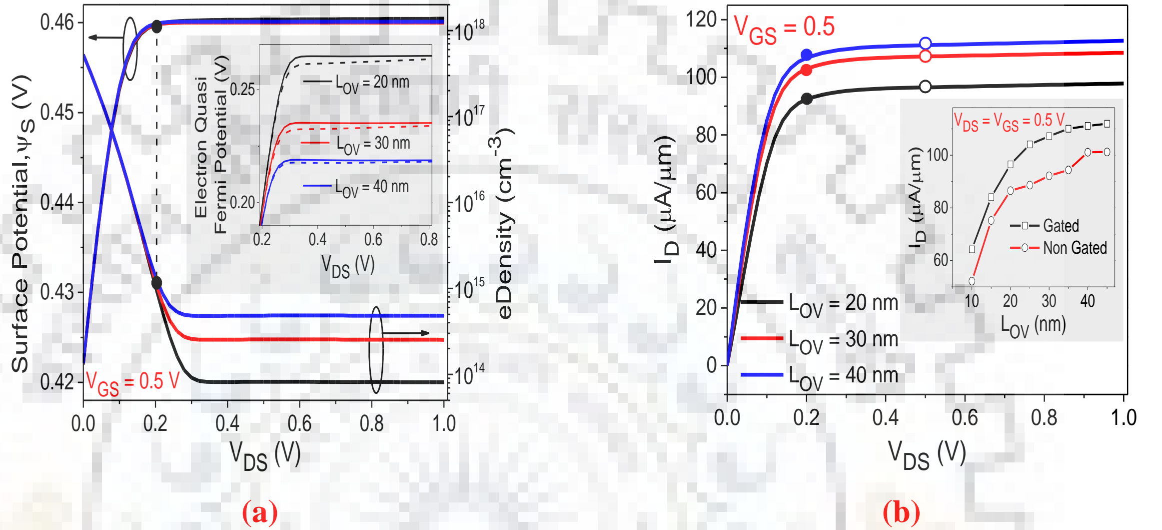


Figure 4.4: (a) Trends of surface potential and electron density (at point x_1) show the common saturation voltages for increased overlap lengths. The solid circle shows the onset of *soft* saturation. Inset shows the electron quasi-Fermi potential for gated and non-gated devices at point x_1. (b) I_D-V_{DS} characteristics exhibit a similar onset of saturation voltage for different L_{OV}. As L_{OV} is increased, the value of $V_{GD}^{s,d}$ remains the same, and hence $V_{DSAT}^{s,d}$. Inset of (b) shows the saturation of I_D with increasing L_{OV} for gated and non-gated devices.

In addition, I_D exhibits saturation for higher values of L_{OV}, as shown in the inset of Fig. 4.4(b). This is owing to an increase in the channel resistance with increasing L_{OV}[123]. It is worth highlighting that the *soft* saturation voltage for the non-gated device slightly differs from, the gated one [Fig 4.3(a)-(b)]. This is attributed by the higher resistance of non-gated region, thereby, the effective V_{DS} at tunnel junction is reduced (a slight reduction in the electron quasi-Fermi potential for the non-gated device is observed as well [inset of Fig. 4.4(a)]). The value of C_{gd} also decreases with increasing the length of the non-gated region, thus a shift in V_{DSAT}^{s} is expected. Eventually, this also causes the saturation characteristics to degrade, and hence the output resistance of the device reduces.

4.4.2 Impact of the epitaxial layer doping (n_{EPI})

The doping of epitaxial layer is also a key design parameter in L-TFETs. Merely increasing n_{EPI} not only increases the ON-state current, but also the OFF-state current [31]. At the onset of *soft* saturation, the entire EoS region is depleted and (free) electron concentration is negligible as compared to the dopant ion concentration. As the value of n_{EPI} increases, the free electron concentration (when depletion occurs within the EoS region) also increases, as shown in Fig. 4.5(a). The electron quasi-Fermi level (F_n) is almost unaltered from EoC (electron rich) to EoS (depleted) region with increasing n_{EPI} [inset of Fig. 4.5(a)].

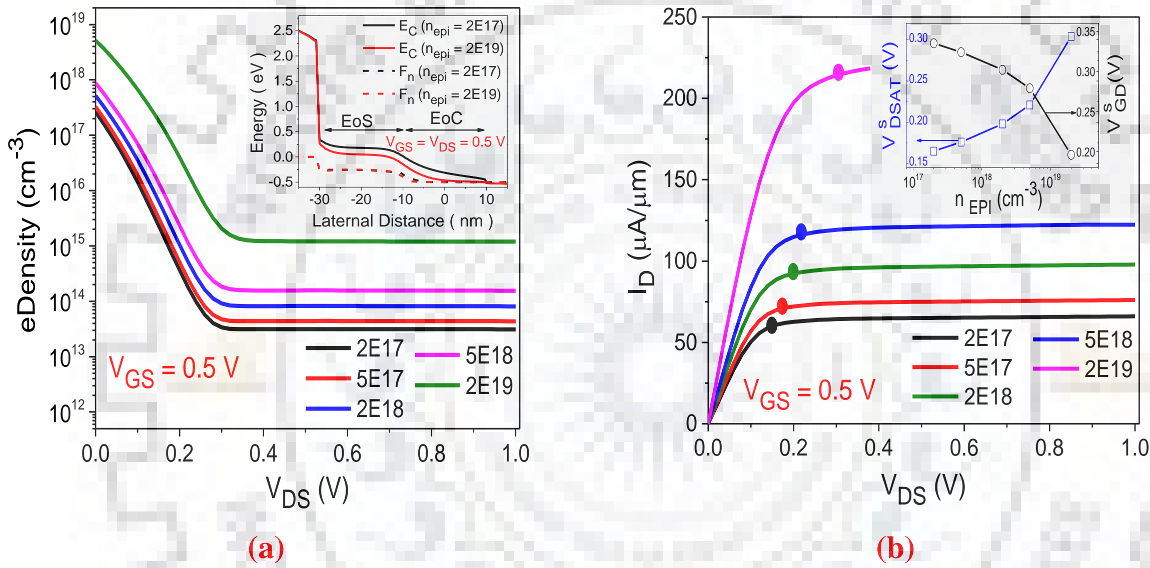


Figure 4.5: (a) Trends of electron density with varying n_{EPI} reveal a shift in the onset of *soft* saturation voltage. Inset shows that the difference E_C-F_n reduces with increasing n_{EPI}. (b) Output characteristics are marked with *soft* saturation voltage. Inset shows an increase in V_{DSAT}^{s} with the increasing value of n_{EPI}.

However, as the value of electron concentration in EoS region increases with n_{EPI}, the difference $E_C - F_n$ reduces. This further reduces the potential drop from EoC to EoS regions, thereby decreasing V_{GD} and increasing V_{DSAT}^{s}. We observe, if the value of n_{EPI} is raised from 2×10^{17} to 2×10^{19}, the value of V_{DSAT}^{s} increases about 0.2 to 0.33 V (for V_{GS} = 0.5 V), as shown in the inset of Fig. 4.5(b). It is also interesting to note that there is a sudden shoot up in I_D beyond n_{EPI} of 5×10^{18} cm^{-3}. This is attributed to a heavily doped p^+n^+-junction between the source and epitaxial layer.

4.4.3 Impact of epitaxial layer thickness (t_{EPI})

The third engineering parameter is the thickness of epitaxial layer. The thickness of epitaxial layer should be low in order to reduce the tunneling width. However, at very small t_{EPI} (< 2 nm), the conduction band and valence bands are not aligned, thereby, the tunneling rate decreases. Conversely, at higher t_{EPI}, the control of gate over the tunneling junction weakens by the virtue of a reduced surface electrical field, thereby, the voltage drop across the EoS region increases. Therefore, I_D exhibits a fast saturation with V_{GS} [Fig. 4.6 (b)], which is also consistent with [27], [123].

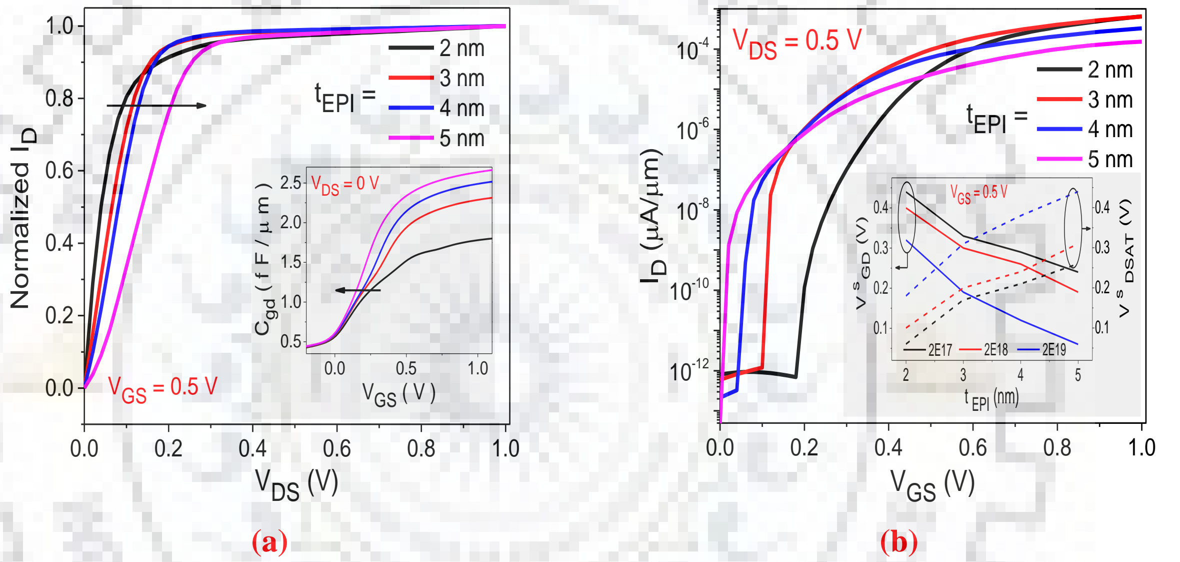


Figure 4.6: (a) I_D is normalized by its maximum value. Normalized I_D-V_{DS} curves show the delayed saturation with increasing t_{EPI} at fixed n_{EPI} of 2×10^{18}. The values of V_{GD}^{s} increases with decreasing t_{EPI} [Inset of (a)]. (b) I_D-V_{GS} for different values of t_{EPI}. Inset of (b) shows the trends of V_{GD}^{s} and V_{DSAT}^{s} with a change in n_{EPI} and t_{EPI}.

The saturation voltages in LT-TEFTS devices are also very sensitive to the value of t_{EPI}. As the value of t_{EPI} increases, the depletion in device happens at higher V_{DS} for a given value of V_{GS} as shown in Fig. 4.6(a). A shift in C_{gd} with the change in t_{EPI} clearly shows a notable change in the values of V_{DSAT}^{s} [inset of Fig. 6(a)]. It is worth highlighting here, for a change of 2 nm in the t_{EPI} (3 nm to 5 nm), the values of V_{GD}^{s} and V_{DSAT}^{s} swing by 0.2-0.3 V [inset of Fig. 4.6(b)]. Moreover, a delayed onset of *soft* saturation worsens the analog parameters for low voltage operation (<0.5V). For instance, at t_{EPI} of 5 nm, the intrinsic gain and bandwidth both

are degraded, as discussed later in detail. Therefore, the selection of t_{EPI} and n_{EPI} are very critical for obtaining optimal analog performance.

4.5 Implications of Proposed Method to Analog Design

This section reveals the performance of an *n*-type L-TFET through a discussion on vital analog parameters, viz. g_m, r_o, C_{gd}, C_{gs}, intrinsic gain ($G = g_m \times r_o$) and unity-gain cutoff frequency ($f_T = g_m/2\pi C_{gg}$), in the *soft/deep* saturation regime. We also discuss the terminal voltages to optimize the performance of L-TFET based CS amplifier biased in the *soft/deep* saturation regime.

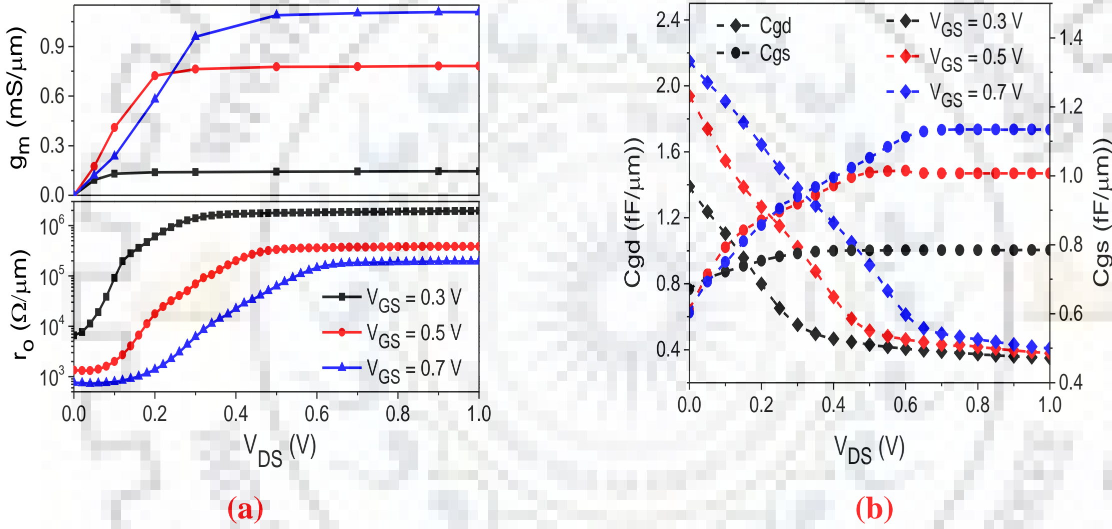


Figure 4.7: Variation in (a) transconductance (g_m) and output resistance (r_o) (b) gate-drain capacitance (C_{gd}) and gate-source capacitance (C_{gs}) with the gate and drain bias

4.5.1 Analog parameters in the *soft/deep* saturation regime

The transconductance increases with increasing V_{GS} for a given V_{DS} due to an increase in I_D, as shown in Fig. 4.7(a). Further, g_m increases in the *soft* saturation regime and then attains a maximum in the *deep* saturation regime, similar to the point tunneling TFETs, as discussed in [21]. This happens because for $V_{DS} \geq V_{DSAT}^{s}$, the E_C and hence Ψ_S gets pinned in the EoS region and I_D starts to saturate, as discussed in Section 4.3. Similar to the trends of g_m, the output resistance becomes a maximum in the *deep* saturation regime. We observe 4× increment in r_o, when V_{DS} is increased from $V_{DSAT}^{s} \rightarrow V_{DSAT}^{d}$ (at V_{GS} = 0.5 V), as shown in Fig. 4.7(a). The output

resistance of L-TFET can be increased by increasing the channel length (for gated device), because the impact of drain-induced barrier modulation decreases [127], thus an improved saturation characteristics are observed. Further, r_o decreases with increasing V_{GS} even when the device doesn't enter linear regime, due to the increased current levels [Fig. 4.6(a)].

The gate capacitances for L-TFETs are shown in Fig. 4.7(b). Unlike the point tunneling TFET (whereby, C_{gd} dominates in C_{gg}), L-TFETs show a significant contribution of both C_{gd} and C_{gs} in C_{gg} [123]. This behavior is attributed to an effective increase in the area of cross-section for tunneling in the later case. As V_{DS} reaches toV_{DSAT}^{s}, the value of C_{gd} (C_{gs}) decreases (increases), thereafter at V_{DSAT}^{d}, attains a minimum (maximum). The minimum value of C_{gd} in the deep saturation is attributed to the increased difference between E_C of the EoC region and the drain [Fig. 4.1(b)]. Consequently, most of the charges are swept out by the drain and hence the EoC region remains depleted. Instead, C_{gs} increases in saturation owing to the increased tunneling at EoS-source junction. Thereafter, it becomes a maximum as the tunnel junction is not much affected by V_{DS} beyond V_{DSAT}^{d}, as depicted in Fig. 4.1(b)-(c).

4.5.2 Implications of V_{DSAT} extraction to analog circuit design

The significance of above observations is also discussed for biasing of a common source amplifier. Here *p*-type L-TFET is used as current source load with its gate terminal connected to V_{bias}, as shown in Fig. 4.8(b). For a *p*-type L-TFET, *SiGe* is kept in the epitaxial layer in order to obtain the CMOS compatible drive currents [119]. An opposite and equal doping of *n*-type L-TFET is used in the different regions of *p*-type L-TFET. Fig. 4.8(b) shows the voltage transfer characteristics (VTC) of the CS amplifier, for different gate bias (V_{bias}) of *p*-type current source load transistor. The shaded region [Fig. 4.8(a)] shows of the boundaries for the *soft* and *deep* saturation regimes, determined by our V_{DSAT} extraction method [Section 4.3.2]. The pink and green color shaded region on each VTC indicates the onset of *soft*/*deep* saturation voltages for *n*- and *p*-type L-TFETs, respectively.

The exterior triangular region on VTC signifies that both the transistors are operated either in the *soft* or in the *deep* saturation regimes. Within this exterior triangle on VTC, grey and purple shaded region identify that both the devices are operated in the *deep* and *soft* saturation regimes respectively, for the given value of V_{bias}. These boundaries provide us with the range of input voltage for which the amplifier should be biased. Further, the voltage gain can be maximized by appropriate selection of the bias voltages for the *n*- and *p*-type L-TFETs.

Therefore, the correct estimation of the boundaries for the *soft/deep* saturation regimes is important from the perspective of the analog circuit design.

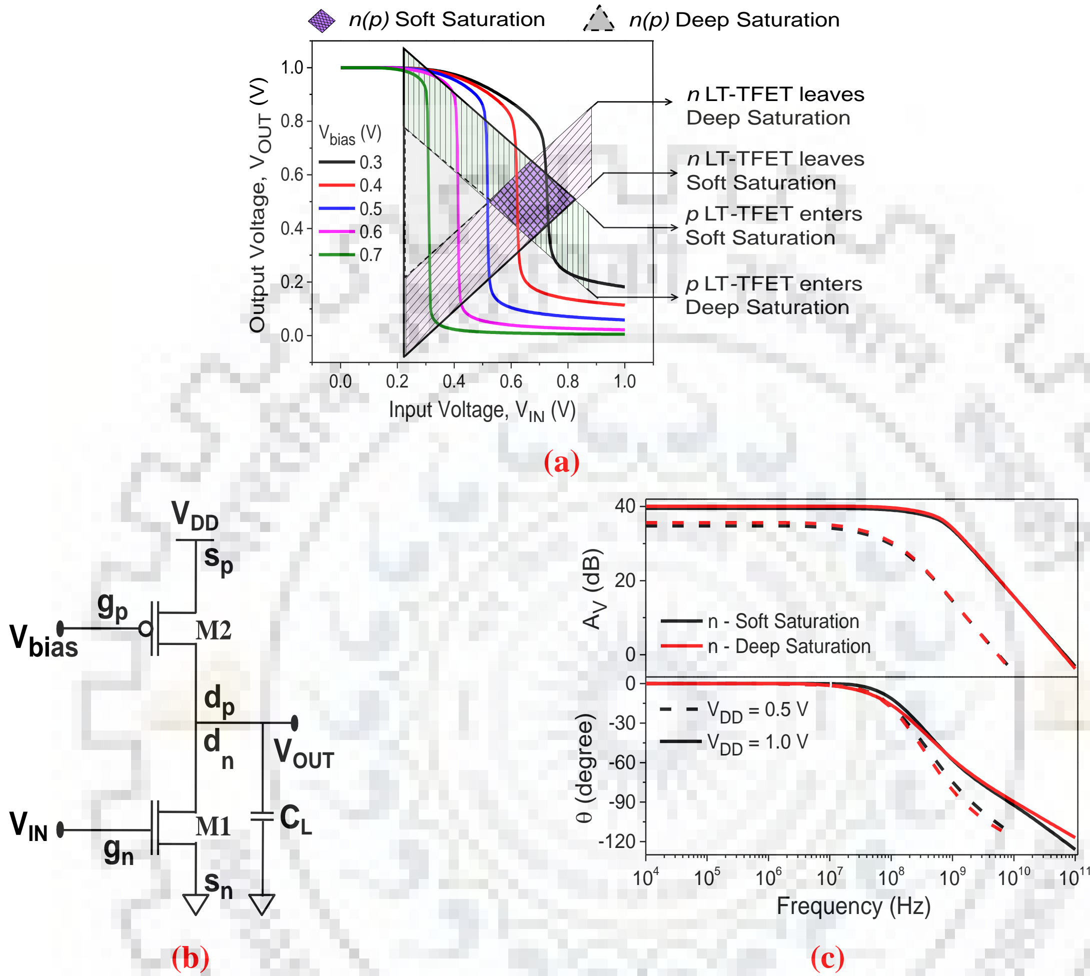


Figure 4. 8: (a) VTC of the L-TFETs based CS amplifier. (b) Schematic of the current source load CS Amplifier. (c) The voltage gain (phase) v/s frequency plot of the CS amplifier shows almost similar response in the *soft* and *deep* saturation regimes, even at $V_{DD} = 0.5$ V.

Finally, the frequency response of the CS amplifier is plotted in Fig. 4.8(c). It is also evident from the figure that the voltage gain (A_V) of a CS amplifier remains almost equal when the *n*-type L-TFET is either biased in the *soft* (39.5 dB) or *deep* (40.1 dB) saturation regime, without any trade-off in the bandwidth (~7×10^8 Hz). In addition, the phase (θ) response is also similar for both the cases, which confirms the advantage of biasing in the *soft* saturation regime. Thus the estimation of$V_{DSAT}^{s,d}$ facilitates the designer to take benefit of the full output voltage swing in the analog circuit design. Furthermore, *A*v and *BW* decrease at lower V_{DD}

owing to a decrease in the drive currents of device [Fig. 4.7(b)]. Nevertheless, the performance of a CS amplifier biased in the *soft* and *deep* saturation regime remain invariably same, even at lower V_{DD} also.

4.6 Impact of Device Design Parameters on the Device-Circuit Analog Performance

This section comprehensively explores the impact of device design parameters on the device/circuit analog performance of L-TFETs. Thereafter, we discuss the device design guideline to the TFET research community, in order to obtain the optimum analog performance. Please note that here we explicitly discuss the device/circuit analog performance for the *soft* saturation regime (V_{DS} = 0.3 V) and the *deep* saturation regime (V_{DS} = 0.5 V) at V_{GS} = 0.5 V. These *soft* and *deep* saturation regimes are determined from our proposed V_{DSAT} extraction formulae, as explained in Section 4.3.

4.6.1 Influence of L_{OV}, n_{EPI}, and t_{EPI} on the analog parameters

As shown in Fig. 4.9 (a), the output resistance exhibits a negligible change with gate-source overlap length. This is attributed to the similar onset of saturation for the devices with different L_{OV}, as discussed in Section 4.3. The drain current saturates with the increasing L_{OV} due to the reduced effect of the lateral electric field at the far end of gate-source overlap region (More details is presented in the Chapter 6). This in turn, also causes a slight modulation (ignorable) of the output resistance with increasing L_{OV}. For $L_{OV} \leq$ 10 nm, the drive current capability of device hinders, owing to the reduced area of cross-section for the BTBT. Hence it is suggested to keep $L_{OV} \geq$ 20 nm to take benefit of the drive current of L-TFETs.

The value of transconductance always increases with the increasing gate-source overlap length as of I_D [Fig. 4.9(a)]. For higher L_{OV}, transconductance tends to saturate because of the saturation in the drain current, as discussed in Section 4.4 [Fig. 4.4]. Further, the variation in transconductance with V_{DS} is not significant, once the device enters in the saturation state. A notable reduction in r_o is observed at the higher doping values of the epitaxial layer, as depicted in Fig. 4.9(b).

This happens as the onset of saturation in I_D occurs at a higher V_{DS} for increasing values of n_{EPI}, (since the depletion in EoS region occurs at higher V_{DS}). Thus, increasing n_{EPI} reduces r_o

to a great extent due to the increased influence of V_{DS}. It may be noted that I_D (I_{ON}, I_{OFF}) also decreases with the decreasing n_{EPI}. Therefore, moderate doping dose (5×10^{17} - 5×10^{18} cm^{-3}) in the epitaxial layer gives optimum results in terms of the gain and bandwidth. Next, g_m always increases with increasing n_{EPI} due to the increased junction electric field and thus more tunneling takes place [Fig. 4.9(b)]. The trends of r_o with the change in t_{EPI} are atypical. For excessively thin t_{EPI} (< 2 nm), the BTBT is suppressed [59], as E_V of the source is not adequately raised to align with the E_C of the epitaxial layer. This eventually results in the small change in I_D with V_{DS}, so the offered r_o remains high [Fig. 4.9(c)]. On the other hand, with increasing t_{EPI}, the control of drain over the tunneling junction weakens, which in turn increases r_o. In general, the value of r_o increases with the increasing t_{EPI} (except t_{EPI} = 2 nm). On the other hand, g_m always decreases with increasing t_{EPI}, by the virtue of a reduced control of the gate, as shown in Fig. 4.9(c). The optimum thickness is also determined by the doping of the epitaxial layer.

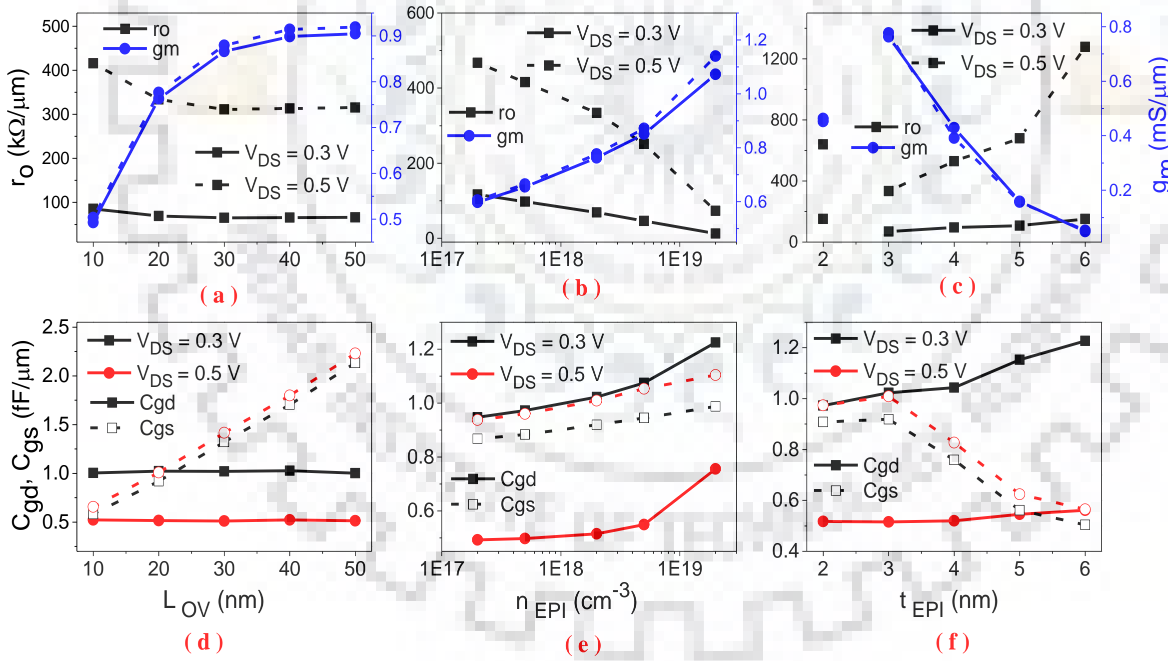


Figure 4.9: Variation in transconductance (g_m) and output resistance (r_o) with (a) L_{OV}. (b) n_{EPI}. (c) t_{EPI}. Variation in gate-drain capacitance (C_{gd}) and gate-source capacitance (C_{gs}) with (d) L_{OV}. (e) n_{EPI}. (f) t_{EPI}.

The gate-drain capacitance (C_{gd}) is determined by the gate control of the charges in the EoS

and EoC regions. After the onset of *soft* saturation, the contribution of the EoS region to C_{gd} becomes negligible [Section 4.3]. As a consequence, C_{gd} remains invariant of L_{OV} after the onset of *soft* saturation, as shown in Fig. 4.9(d). While, C_{gs} increases almost linearly with L_{OV}, because of a larger cross-section of the tunneling. It may be noted from Fig. 4.9(e), that both C_{gd} and C_{gs} increases with the increasing n_{EPI}. The higher n_{EPI} create a p^+n^+- junction between the source and epitaxial layer, which raises the value of C_{gs}. This also results in a strong coupling of the EoC region with the drain, hence increasing C_{gd}. Besides, C_{gs} significantly decreases with the increasing t_{EPI} due to a suppressed BTBT, while C_{gd} is not much affected, as depicted in Fig. 4.9(f).

TABLE 4.1

COMPARISON OF INTRINSIC GAIN AND UNITY-GAIN CUTOFF FREQUENCY (GHZ) FOR DIFFERENT VALUES OF L_{OV}, N_{EPI} AND T_{EPI} AT V_{GS} = 0.5 V

L_{OV}	V_{DS} = 0.3 V		V_{DS} = 0.5 V		n_{EPI}	V_{DS} = 0.3 V		V_{DS} = 0.5 V		t_{EPI}	V_{DS} = 0.3 V		V_{DS} = 0.5 V	
(nm)	G	f_T	G	f_T	(cm^{-3})	G	f_T	G	f_T	(nm)	G	f_T	G	f_T
10	42.02	49.4	209.35	67.9	2×10^{17}	69.92	52.4	283.15	67.5	2	68.19	38.3	296.02	49.4
20	52.66	62.6	259.06	81.1	5×10^{17}	63.80	56.2	276.77	72.7	3	52.66	62.5	259.06	81.1
30	56.54	58.9	273.89	72.7	2×10^{18}	52.66	62.5	259.06	81.1	4	40.93	38.0	207.31	46.3
40	59.01	52.4	286.55	62.7	5×10^{18}	39.49	67.1	219.36	86.6	5	9.83	14.8	106.22	21.3
50	59.76	46.0	289.75	53.4	2×10^{19}	13.39	77.0	83.28	97.6	6	7.39	4.50	67.27	7.45

Table 4.1 compares the intrinsic gain and unity-gain cutoff frequency for the different device design parameters. The intrinsic gain increases with an increasing L_{OV} as it is dictated by g_m (r_o is fairly constant). However, f_T decreases as the impact of C_{gs} becomes more pronounced at higher L_{OV}. Therefore it is advisable to keep L_{OV} in the range of 20-40 nm for optimum performance. The intrinsic gain degrades at higher n_{EPI}, as r_o gets worse. In addition, f_T gets improved at higher n_{EPI} as a result of the raised g_m. Thus, n_{EPI} should be kept in the range of 5×10^{17}- 5×10^{18} cm^{-3}. Both G and f_T decrease at the higher t_{EPI}, because g_m gets reduced, [Fig. 4.8(c), (f)]. Further, t_{EPI} should not be kept below 3 nm, because the drive capability gets deprived. The optimization of t_{EPI} is critical, as its best possible value may also depend upon n_{EPI}. However, we observe that t_{EPI} of 3-4 nm gives the optimum results for n_{EPI} of 2×10^{18} cm^{-3}.

4.6.2 Impact of L_{OV}, n_{EPI}, and t_{EPI} on the Common Source Amplifier

The impact of device design parameters on the performance of CS Amplifier is discussed in this section. For all the amplifiers, the values of V_{bias} and V_{OUT} are kept at $V_{DD}/2$, and V_{IN} is set accordingly. In this study, the values of the device design parameters are kept equal for both *n*- and *p*-type L-TFETs. The cut-off frequency (f_{3dB}) and A_V and of the CS amplifier can be expressed as [129]:

$$A_V = \frac{V_{out}}{V_{in}} \approx \frac{-g_{m1}}{g_{ds1} + g_{ds2}} \tag{4.1}$$

$$f_{3dB} \approx \frac{g_{ds1} + g_{ds2}}{2\pi(C_{gd1} + C_{gd2} + C_L)} \tag{4.2}$$

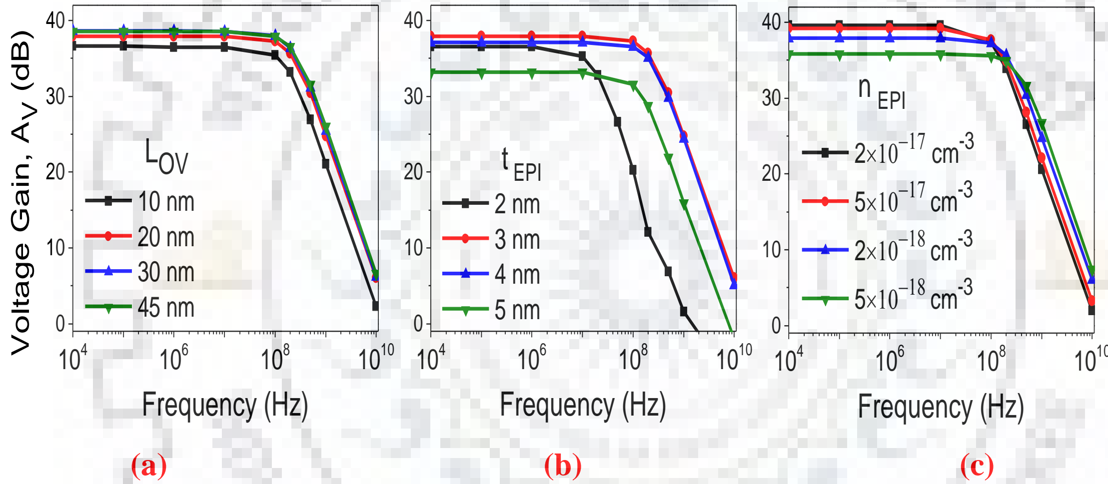


Figure 4.10: (a) Frequency response of CS amplifier with varying device design parameters (a) L_{OV}. (b) n_{EPI}. (c) t_{EPI}. Please note that for all the amplifiers, $V_{bias} = V_{OUT} = V_{DD}/2$.

It is obvious from Fig. 4.10(a), the voltage gain of the CS amplifier increases with increasing L_{OV}. An increase in A_V of 37.9 dB to 39.6 dB is observed when L_{OV} is raised from 20 nm to 45 nm. A_V does not increase beyond 40 nm overlap length due to the increased value of drift resistance. It can also be seen from Fig. 4.9(a), the output conductance ($g_{ds} = 1/r_o$) and C_{gd} remain almost independent of overlap length for $L_{OV} \geq 20$ nm. For $L_{OV} < 20$ nm, A_V and *BW* suffer, as both g_m and g_{ds} decrease. A_V (*BW*) for a CS amplifier decreases (increases) with increasing value of n_{EPI} [Fig. 4.10(b)]. This happens as g_{ds} increases with increasing n_{EPI}. We observe merely a change of around 39.5–35.4 dB and 200–500 MHz in A_V and *BW* respectively, when n_{EPI} is raised from 5×10^{17}–5×10^{18} cm^{-3}. For excessively lower doping, *BW*

remains very small, albeit the higher values of A_V. An almost equal value of A_V and BW for the CS amplifier is observed at t_{EPI} of 3–4 nm, as shown in Fig. 4.10(c). Beyond this range, either A_V or BW suffers. It is also observed that the bandwidth drastically reduces for $t_{EPI} < 3$ nm due to the extremely high output resistances.

4.7 Conclusion

We presented a comprehensive physics based explanation of the output current saturation and an extraction method of V_{DSAT} for the line tunneling based TFETs. Subsequently, we also discussed the significance of estimating V_{DSAT}^{s} for biasing a CS amplifier. Our results show that a comparable voltage gain and bandwidth are obtained when the driver transistor of a CS amplifier is either biased in the *soft* or *deep* saturation regime, which necessitates the correct estimation of $V_{DSAT}^{s,d}$. The experiments carried out in this Chapter show that, increasing the values of L_{OV} does not impact the saturation voltage of L-TFET. Further, V_{GD} also remains a constant at the onset of *soft* and *deep* saturation conditions. The validation of the proposed method is done against the numerically obtained TCAD results. A change in the values of t_{EPI} and n_{EPI} significantly shift the onset of *soft* saturation condition in the L-TFETs, which in turn, impact the analog performance. Although, the gain and bandwidth are the best in the *deep* saturation regime, nevertheless, they also exhibit good values in the *soft* saturation regime. Overall results indicate that our method adequately allows determining the optimal terminal voltages for biasing L-TFETs based analog circuits in the *soft* and *deep* saturation regimes. Finally, the optimization guidelines to quantify the device/circuit analog performance are also presented for the TFET research community by considering the impact of device design parameters.

Chapter 5
Impact of Body Bias on the Line TFETs and its Implications to Analog Design

This chapter reports the impact of body bias (V_{BS}) on the performance of the epitaxial layer based Line Tunneling FETs (L-TFET) for the first time. The drain current (I_D) initially increases with the reverse body bias and then it saturates. This happens as the occupancy probability (and hence the band-to-band tunneling generation) increases with the reverse body bias, and then remains invariant of any further increase in V_{BS}. Thus the occupancy probability in the source valence band plays a vital role in determining the modulation of I_D with V_{BS}. The reverse V_{BS} at which the drain current attains a maximum is defined as V_{BSAT}, and changes almost linearly with the gate bias (V_{GS}). A novel physics based model is also proposed to investigate the dependence of V_{BSAT} on V_{GS}. In fact, an increase of 40–60% in I_D with the increasing reverse V_{BS} is also observed. Forward V_{BS} does not significantly alter the value of occupancy probability and I_D. The magnitudes of V_{BSAT} increases with the gate-source overlap lengths and decreases with the thickness of epitaxial layer. Further, V_{DSAT} slightly reduces with an increase in the reverse V_{BS}. The intrinsic gain and unity gain cut-off frequencies increases with the reverse V_{BS} and remains almost unaltered with the forward V_{BS}.

5.1 Introduction

The steep subthreshold characteristics of tunnel FETs are being extensively explored by the research community for the ultra-low power VLSI design applications [92], [97], [98]. However, the major challenge for TFETs is its poor drive capability. Thanks to the advancement in the junction and material engineering, which have significantly improved the drive current of TFETs [19], [118], [130]. The epitaxial layer/source pocket based line TFETs are also gaining interest, whereby the source region is overlapped by the metal gate [27], [29], [116], [122], [123]. In these devices, the area of cross-section for BTBT is large, hence I_D

increases. Recently, the potential of L-TFETs for the analog circuits and Internet of Things (IoT) applications have also been discussed [94]. In addition, the benefits of body biasing (V_{BS}) to improve the device/circuit performance has been reported by several researchers for *deep* sub-micrometer CMOS technologies [3]. The improvement in the I_D with V_{BS} has been also reported for point tunneling devices [57], [58]. Besides the potential to improve TFET performance, the body biasing also provides additional flexibility to the circuit designer. However, to the best of our knowledge, the impact of V_{BS} on the line TFETs with epitaxial layer/source pocket has never been discussed.

In this work, we report for the first time that the body bias has a significant impact on the L-TFETs with epitaxial layers. We discover, that I_D initially increases with reverse V_{BS} and then saturates. The purpose of this study is also to propose a novel physics based extraction method and explanation of V_{BSAT}. The body bias modulates the electrostatics in the thin epitaxial layer over the channel and source. In turn, this modifies the carrier concentration and the gate oxide induced electric field. Particularly, we found that the reason behind the enhancement in I_D is owing to the modulation of electron quasi-Fermi energy (and thus the occupancy probability) in the valence band of the source with the body bias. This changes the availability of the carriers at the initial tunneling point and empty states at the end of the tunnel path. Thus, the impact of body bias on the epitaxial layer based L-TFET is distinct when compared with the body bias effect on the point TFETs. The impact of V_{BS} on the I_D-V_{DS} characteristics and analog performance is also examined

5.2 Device Structure and Simulation Framework

A 2D schematic of the target device is shown in Fig. 5.1 (a). The device under consideration is one of the most established L-TFET [27]. It consists of a 3 nm epitaxial layer thickness (t_{EPI}) of *Silicon* over the source and channel. The source material is selected as $Si_{0.5}Ge_{0.5}$ to obtain a high drive current [28]. The high-κ metal gate stack with a dielectric layer of 3 nm HfO_2 is selected along with a channel length of (L_{CH}) 20 nm. The doping concentration of source (*p*-type), drain (*n*-type), channel (*p*-type) and epitaxial layer (*n*-type) is kept at 2×10^{20}, 5×10^{19}, 1×10^{16} and 2×10^{18} cm^{-3} respectively, unless otherwise stated. The thickness of BOX region is kept at 10 nm and the body is doped heavily with *p*-type dopants. Our self-consistent numerical simulations are performed using Sentaurus TCAD tool (*version K-2015-06*) of Synopsys Inc. The dynamic nonlocal band-to-band tunneling model is activated across

all the semiconductor regions to emulate the tunneling phenomenon. This model utilizes the nonlocal generation of the electrons of holes caused by the direct and phonon-assisted BTBT process. The generation rate is calculated from the nonlocal path integration. The theoretically calculated values of BTBT model parameters for *Silicon* (A = 3.29 × 10^{15} $cm^{-3}·s^{-1}$, B = 2.38 × 10^{7} V cm^{-1}) and $Si_{0.5}Ge_{0.5}$ (A = 2.27 × 10^{15} $cm^{-3}·s^{-1}$, B = 1.55 ×10^{7} V cm^{-1}) are borrowed from [43]. The detailed descriptions of various other physical models are same as mentioned in Chapter 3.

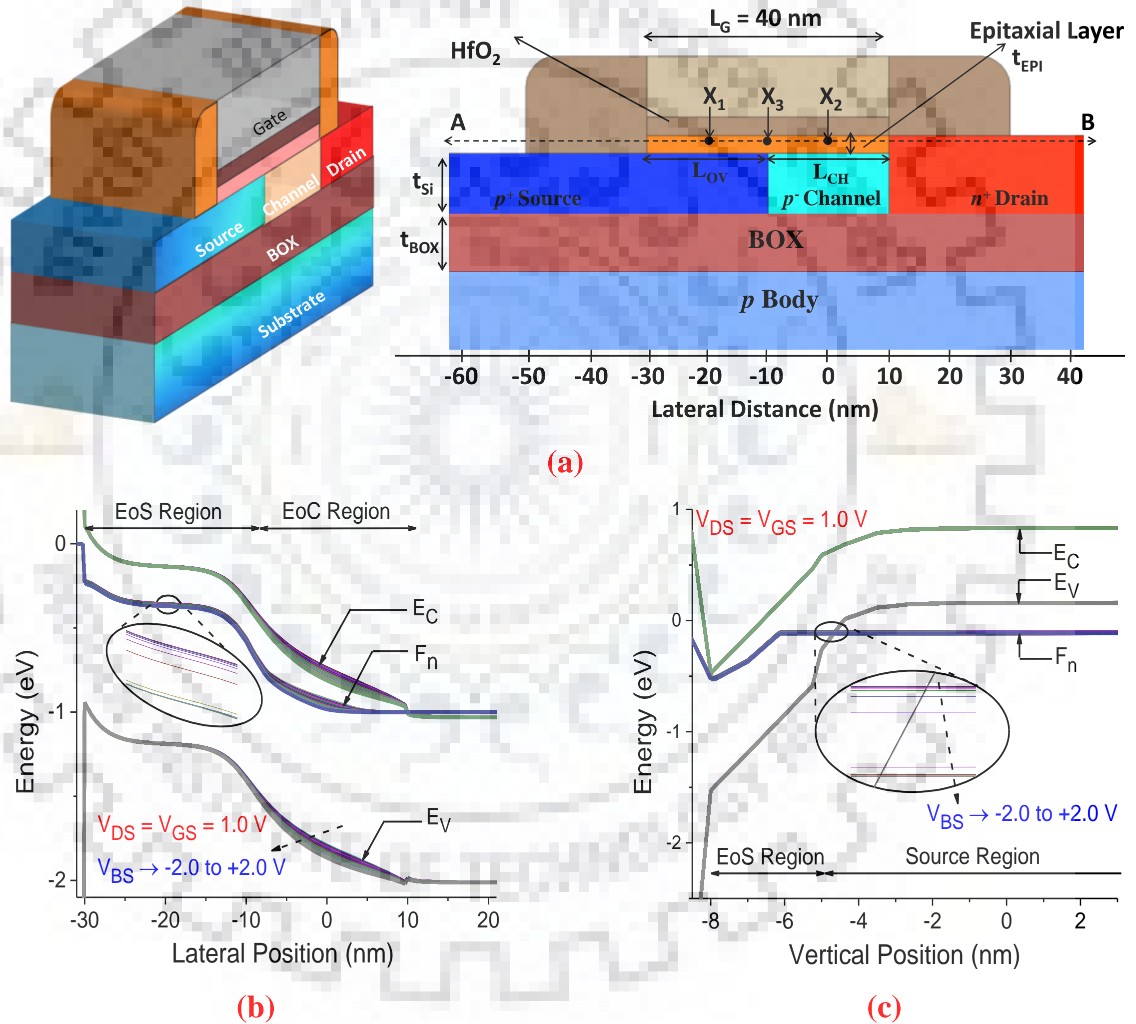


Figure 5.1: (a) 3-D view and 2-D schematic of the target device. Please note that t_{Si} = t_{BOX} = 10 nm for all simulations. (b) Lateral energy bands across the line AB. (c) Vertical energy bands across the EoS region show the tunneling at point x_1. The points x_1, x_2, and x_3 are kept at 1 nm below the oxide-semiconductor interface along the line AB. The values of band energies may vary with the position of line AB, however, the underlying physics will remain the same.

5.3 Impact of Body Bias on Line TFETs

This section investigates the influence of the reverse and forward body bias on the drain current of the epitaxial layer based L-TFETs. The drain current initially increases with the increasing reverse V_{BS}, thereafter it attains a maximum value, as shown in Fig. 5.2(a)-(b). A similar trend of the electron BTBT generation is also observed from the numerical TCAD simulations [Fig. 5.2(c)]. This happens because the reverse V_{BS} increases the available carriers for tunneling at the EoS/source junction underneath the high-κ metal gate [Fig. 5.1(a)]. Further, it also increases the average vertical electric field across the EoS region to a little extent. An improvement of more than 50% in I_D can be achieved with the appropriate selection of body bias. Please note that L-TFET is assumed to be operated in the saturation region ($V_{GS} \leq V_{DS}$) unless otherwise stated.

5.3.1 Reverse body bias and V_{BSAT}

Initially, with the increasing reverse V_{BS}, the depletion charges in the substrate and channel region continuously increase. Thus, the band energy (E_C, E_V) of the channel and epitaxial region over the channel (EoC) increase with reverse body bias as depicted in Fig. 5.1(b). For the smaller values of reverse V_{BS}, the electron concentration in the channel reduces marginally. This signifies that the difference E_C-F_n is almost constant, so F_n also moves with E_C (for smaller reverse V_{BS}). We observe a very small change in the E_C/E_V of EoS region [Fig. 5.1(c)], when compared to the change in F_n. This happens as the heavily doped p^+-source region shields the EoS region.

In addition, the potential in the EoS region is mostly governed by the gate to source vertical electric field. Thus V_{BS} does not directly change the $E_{C,\ V}$ of the EoS region. However, the reverse V_{BS} causes a shift in the electron/hole quasi-Fermi level ($F_{n/p}$) of the EoS and source region, as shown in the inset of Fig. 5.2(d). The reason is as follows: Since the EoS region is fully depleted of electrons, thus F_n of the EoS and EoC regions are tightly bound. Therefore, any change in F_n of the EoC region results in a similar change in F_n of the EoS region. The band bending across the tunnel junction is not much affected by the reverse V_{BS}. It is worth highlighting here, that an increase in F_n increases the occupancy energy levels in the valence band of the source region [Fig. 5.1(c)]. This increases the number of carriers available for tunneling, which is also confirmed by the increased rate of BTBT generation [Fig. 5.2(c)].

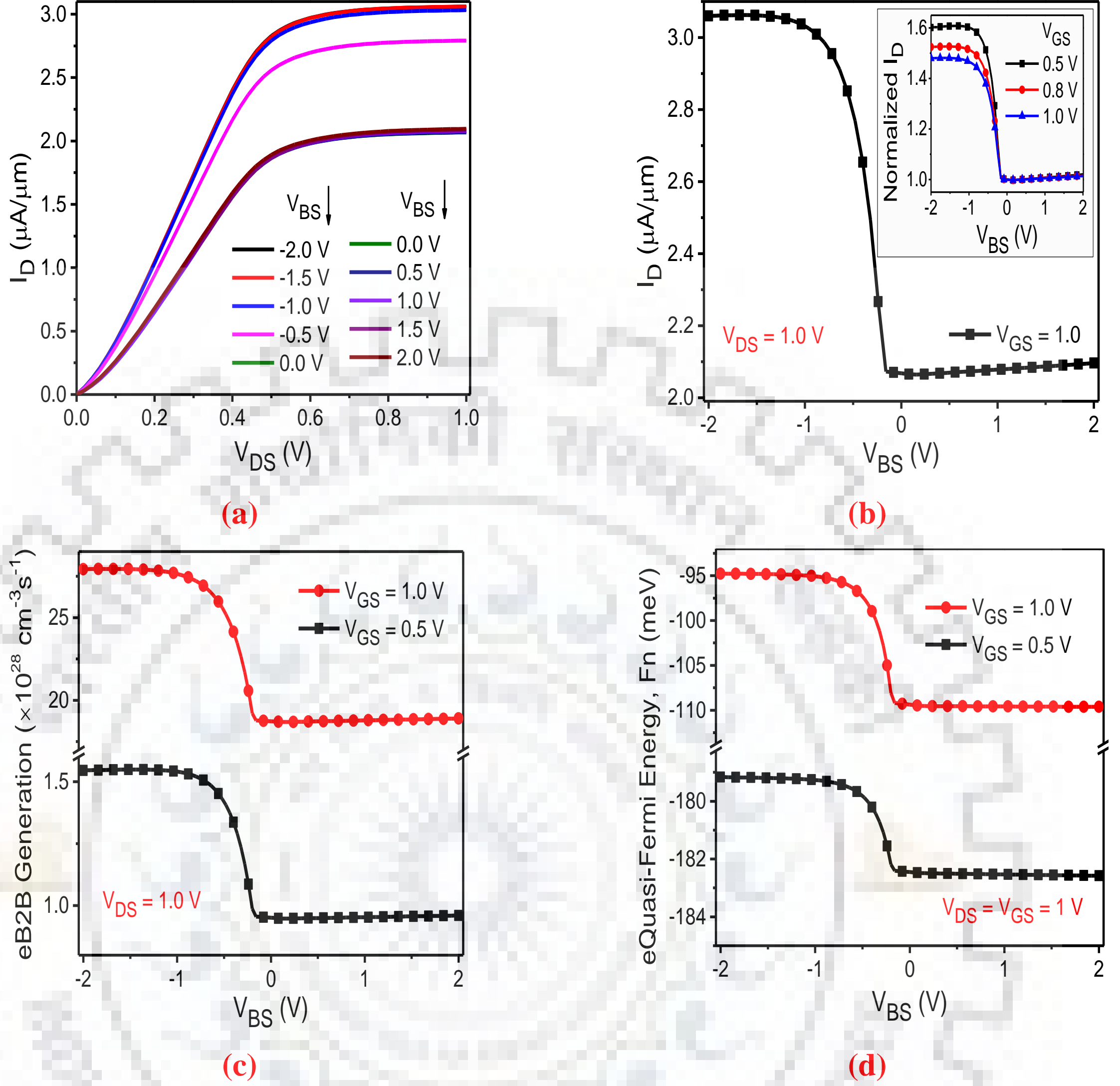


Figure 5.2: (a) Output characteristics of the target device. Here negative (positive) values of V_{BS} correspond to reverse (forward) body bias. (b) Saturation in I_D is observed with reverse body bias, while, I_D does not significantly change with the forward body bias. Normalized values of I_D show the modulation efficiency for different V_{GS} [Inset of (b)]. Trends of (c) Electron band-to-band generation rate at point x_1 (d) Electron quasi-Fermi energy with V_{BS} for different V_{GS} at EoS/source junction along the line x_1 for different gate biases.

As per Esaki's theory of tunneling, the drain current, I_D is proportional to:

$$I_D \propto \int_{CB_{EoS_min}}^{VB_{S_max}} P(E)\left[f_S(E) - f_{EoS}(E)\right]dE \tag{5.1}$$

Here, f_S and f_{EoS} are the occupancy functions of the source and EoS region respectively, and *P(E)* is the tunneling probability which depends on the electric field. With the increasing

reverse V_{BS}, F_n of the EoC/channel region increases, hence F_n of the EoS/source region also increases, whereas $E_{C,V}$ of the EoS/source region changes to a very small extent. Since, the source is degenerate, so F_n lies within the valence band of the source. Therefore, the occupancy probability of the valence band of the source also increases with increasing F_n. In fact, a small change in $F_{n/p}$ causes the available states to change drastically. This consecutively changes the availability of carriers and empty states at the tunneling path. Therefore, the overall tunneling current increases with the reverse V_{BS}.

With a further increase in the reverse V_{BS}, the EoC region gets completely depleted of electrons thus F_n of the EoC region does not significantly change its position [Fig. 5.1(b)]. Therefore, the difference E_C-F_n in the EoC region increases with an increase in the reverse V_{BS}, and F_n gets saturated in the EoC and EoS regions. This also causes the tunneling current to saturate with the reverse V_{BS} [Fig. 5.2(a)]. Next, we also observe that the tunneling distance [which depends upon the position of F_n within source] slightly decreases with reverse V_{BS} and then it becomes independent of V_{BS}. This also confirms that I_D saturates for $V_{BS} \geq V_{BSAT}$. Here V_{BSAT} is the reverse body bias for which the I_D attains a maximum. A negligible drop in I_D beyond V_{BSAT} is due to the slight increase in $E_{C,V}$ in the EoS region with the increasing reverse V_{BS}. Although this change is very small, still beyond V_{BSAT} the difference E_C-F_n is dictated by the values of $E_{C/V}$ only, thus a small decrease in I_D is expected. It is worth highlighting here that the change in E_C/E_V with reverse V_{BS} is more dominating in the channel than the source. This is due to a decrease in the electron density of the channel with the reverse V_{BS}.

In addition, the reverse V_{BS} is more influential at the lower gate biases [inset of Fig. 5.2(b)]. Here the normalization of I_D is calculated as, $I_D(V_{BS})/I_D(V_{BS}=0)$. The maximum I_D modulation efficiency for V_{GS} = 0.5 V is 61% when compared to 48% at V_{GS} = 1.0 V. This happens because at a higher V_{GS}, E_C and F_n of EoC/channel region shift downward. This also results in a downward shifting in F_n of the source valence band [Fig. 5.1(b)-(c)], consequently, a reduced BTBT modulation efficiency is observed. The value of V_{BSAT} can be extracted as the reverse bias voltage where the first derivative of I_D becomes zero, i.e.$\partial I_D/\partial V_{BS} = 0$, for the given V_{GS} and V_{DS}. These values of V_{BSAT} change almost linearly with V_{GS} [Fig. 5.3(a)]. This is owing to the fact that the surface potential in the EoC region varies linearly with V_{GS} at the onset of $V_{BS} \geq V_{BSAT}$. Please note, Fig. 5.3(c) can be realized as a linear capacitive network, so the depletion charge in the silicon film does not change with V_{GS} in the saturation regime, i.e. $V_{GS} \leq V_{DS}$. Since E_C of the EoS region remains almost independent of the reverse V_{BS},

therefore, the difference ΔE_C also changes linearly with the V_{GS} at the onset of the body saturation, as shown in Fig. 5.3(b). We observe a change in $V_{BSAT} \approx 0.32$ V when V_{GS} changed from 0.5 V → 1.0 V. After the onset of $V_{BS} \geq V_{BSAT}$, the L-TFET devices exhibit a negative conductance ($\partial I_D/\partial V_{BS}$), because of a slight decline in I_D beyond V_{BSAT}. Here, ΔE_C is the difference between the conduction band energies of the EoS and EoC region.

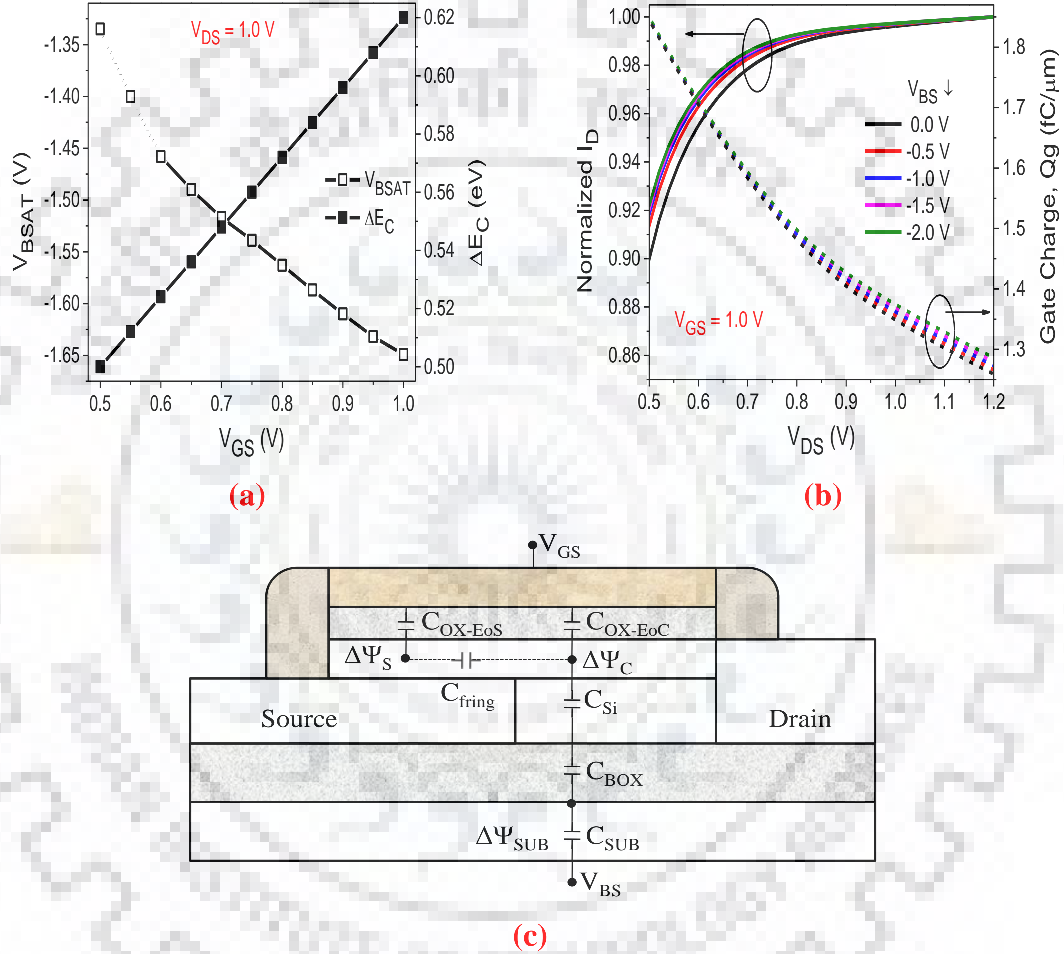


Figure 5.3: (a) The variation of V_{BSAT} and ΔE_C with the gate bias. The change in slope of V_{BSAT} is due to the change in the channel and substrate charge with V_{GS}. (b) A small shift in the V_{DSAT} due to V_{BS} is observed, which is confirmed by the change in gate charge. (c) Gauss law is applied from body to gate terminal to obtain the potential balance equation for L-TFET device.

To gain a better insight into this phenomenon, we use a potential balance equation based on the capacitance division approach [3], as shown in Fig. 5.3(c).

$$V_{GS} - V_{BSAT} = V_{FB} + \Psi_{Sub} + V_{BOX} + V_C + V_{OX} \tag{5.2}$$

$$V_C = \int_0^{t_{Si}} \left[\varepsilon_{C-Sub} + \frac{qN_a x}{\varepsilon_{Si}} \right] dx = \frac{Q_{Sub}}{\epsilon_{Si}} t_{Si} + \frac{qN_a t_{Si}^2}{2} \tag{5.3}$$

Here V_{FB}, Ψ_{Sub}, V_{BOX}, V_C and V_{OX}, are the *flatband* voltage, the surface potential of the substrate, the potential drop in the BOX region, the potential drop in the channel region and the voltage drop in the gate oxide respectively. ε_{C-Sub} is the electric field in the silicon film, caused by the gate to substrate charges. Eq. (5.2) can be simplified as:

$$V_{GS} - V_{BSAT} = V_{FB} + \Psi_C + V_{OX} \tag{5.4}$$

$$\text{Where } \Psi_C = \Psi_{Sub} + V_{BOX} + V_C \tag{5.5}$$

Since Fig. 5.3(a) is a linear capacitive network, so the change in voltage is always linearly related. Thus $\Delta\Psi_{Sub}$ and $\Delta\Psi_C$ are proportional to each other, i.e. $\Psi_C = 0$, if $\Psi_{Sub} = 0$. It is the substrate charge which actually changes with change in V_{GS}, therefore V_{BSAT} also changes with the same. By taking the depletion approximation, (5.4) becomes:

$$V_{GS} - V_{BSAT} = V_{FB} + \Psi_C + k_1\sqrt{\Psi_C} \tag{5.6}$$

As discussed above, the surface potential changes linearly with the gate bias, so without any loss of generality, (5.6) can be written as:

$$V_{GS} - V_{BSAT} = V_{FB} + a + bV_{GS} + k\sqrt{a + bV_{GS}} \tag{5.7}$$

Eq. (5.6)-(5.7) are valid under the depletion approximation; otherwise, the substrate charges exhibit an exponential dependence on the $\Delta\Psi_{Sub}$ (V_{GS}) [3]. Any change in the surface potential of the EoS region ($\Delta\Psi_S$) with V_{GS} and V_{BS} corresponds to a change in the gate-to-source fringing electric field of the EoS region, as per (5.3). At the onset of $V_{BS} \geq V_{BSAT}$, the ratio $\Delta\Psi_S/\Delta\Psi_C$ remains constant with V_{GS}. That is why ΔE_C varies linearly with V_{GS} at the onset of $V_{BS} \geq V_{BSAT}$ [Fig. 5.3(a)]. Moreover, any change in V_{GS} causes the gate-to-source fringing electric field (hence C_{fringe}) to change, thus both $\Delta\Psi_S$ and $\Delta\Psi_C$ get changed. This change is compensated by the reverse V_{BS}, i.e. V_{BSAT} also changes accordingly. Thus, we observe an increase in V_{BSAT} with any substantial increase in V_{GS}, as shown in Fig 5.3(a). It may be noted from Fig. 5.3 (a), that initially V_{BSAT} changes sub-linearly with V_{GS} ($\leq$ 0.6 V). This is because the depletion charge in the EoC and substrate region remains almost unchanged below 0.6 V, then it starts to drop significantly with increasing V_{GS} (since the electron density increases with V_{GS}). The change in depletion corresponds to change in *charge* in (5.3), hence the linear dependence of Ψ_S on V_{GS} deviates. Please note that the model is not valid for forward V_{BS}.

5.3.2 Forward body bias

The drain current remains almost steady with the forward V_{BS}, because the electron band-to-band generation rate does not change significantly with the positive values of V_{BS} [Fig. 5.2(c)]. The difference E_C-F_n in the EoC/channel region decreases with an increase in the forward V_{BS}. Thus the electron density in the channel region increases with the forward V_{BS}. Besides, the change in $F_{n/p}$ of the epitaxial layer/source region is negligibly small with the forward V_{BS}, as shown in Fig. 5.2(d). Therefore, the occupancy probability and hence the available states for tunneling remain almost unaltered. In particular, the source potential increases with the forward body bias, so F_n should move toward intrinsic energy level. On the other hand, F_n of the channel/EoC region decreases with the forward V_{BS}, so the overall effect is compensated. Thus, F_n of the EoS/source region remains almost invariant of the forward V_{BS}. This also causes the tunneling current to remain almost invariant of the forward V_{BS}.

5.3.3 Impact of body bias on V_{DSAT}

The saturation in I_D with V_{DS} is mainly determined by the electron density and the surface potential of the EoS/EoC region, as explained in Chapter 4. As V_{DS} increases, initially, the electron density in the EoS region decreases and then becomes independent of V_{DS}. This happens as Ψ_S of EoS region gets pinned after the onset of the *soft* saturation. For a given gate and drain bias, when reverse V_{BS} increases, the electron density in the EoS region increases. This is because of a decrease in E_C-F_n with the reverse V_{BS}, as shown in Fig 5.1(b)-(c). Since, Ψ_S of EoS region is slightly affected by the reverse V_{BS}, as a result, a minimal change in V_{DSAT} with the reverse V_{BS} is also expected. This can also be confirmed from the change in gate charge due to the reverse V_{BS} in the saturation region, as shown in Fig. 5.3(b). The reverse body bias advances the onset of saturation, i.e. V_{DSAT} reduces to a little extent. We observe a reduction of around 20 mV in V_{DSAT} when the reverse V_{BS} is increased from 0 to 2 V.

5.4 Impact of Device Design Parameters on V_{BSAT}

This section investigates the impact of device design parameters of L-TFET on its I_D-V_{BS} characteristics. The vital device design parameters in L-TFETs are gate-source overlap length (L_{OV}), epitaxial layer thickness (t_{EPI}), epitaxial layer doping (n_{EPI}) and channel length. The detailed description of each parameter is as follows:

5.4.1 Gate-source overlap length (L_{OV})

The gate-source overlap length is a widely used parameter to modulate the drive capability of L-TFETs. As we scale up L_{OV}, the drain current increases due to an increase in the cross-section area of tunneling, as shown in Fig. 5.4 (a). The onset of V_{BSAT} in L-TFETs also increases for the given gate/drain bias. This is because the impact of the fringing electric field reduces with increasing L_{OV}. As a result, $\Delta\Psi_S$ of the EoS region also increases. From the capacitance model [Fig. 5.3(c)], it is obvious that a higher reverse V_{BS} is required to compensate for this change in $\Delta\Psi_S$ due to increased L_{OV}, hence V_{BSAT} increases, as shown in Fig. 5.4(b). We observe that V_{BSAT} changes from -1.65 V to - 2.12 V when L_{OV} is raised from 20 nm to 200 nm.

On contrary to above, when the channel length (L_C) is increased from 20 nm to 30 nm, V_{BSAT} changes from -1.65 V to -1.53 V. This reduction in V_{BSAT} can also be explained from the capacitance model. As we increase L_C, the value of $\Delta\Psi_C$ increases and the ratio $\Delta\Psi_S/\Delta\Psi_C$ decreases, thus less reverse V_{BS} is required to compensate for the same. Further, the modulation of I_D with V_{BS} is slightly affected by the increase in L_{OV}, as shown in Fig. 5.4(b). The percentage change in I_D with V_{BS} initially increases due to an increase in the tunneling. Thereafter, a decline is observed because of an increase in the resistance of the EoS region with increasing gate-source overlap region.

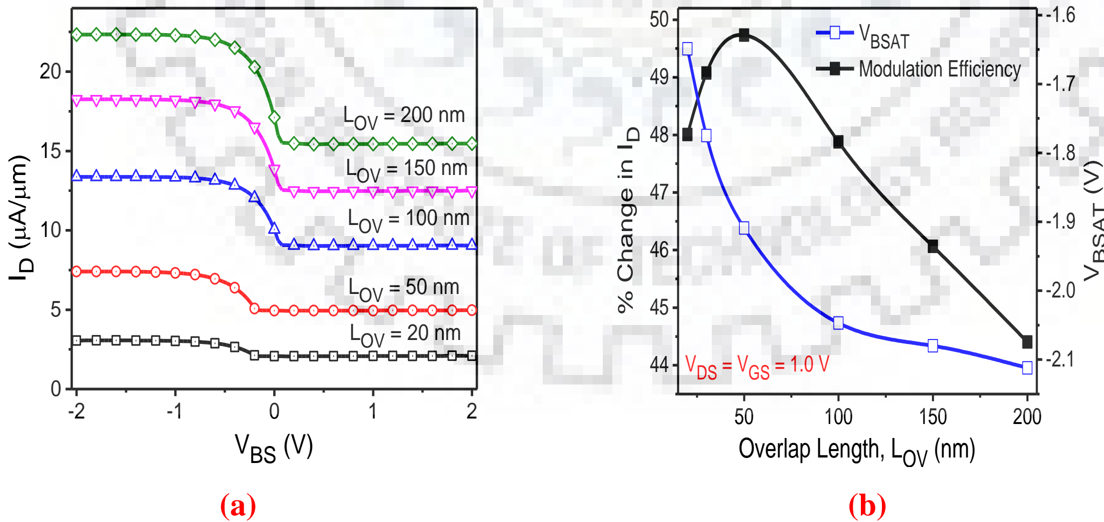


Figure 5.4: (a) I_D-V_{BS} characteristics for the different values of L_{OV}, whereby I_D increases almost linearly with L_{OV}. (b) Modulation of I_D by V_{BS} is almost independent of L_{OV}, while the magnitude of V_{BSAT} increases with L_{OV}.

5.4.2 Thickness of epitaxial layer (t_{EPI})

The second engineering parameter is the thickness of epitaxial layer. The optimum value of thickness also depends upon the doping of the epitaxial layer. The drain current drops with increasing t_{EPI} as the tunnel junction moves away from the gate, hence the vertical electric field at tunneling junction reduces [Fig. 5.5(a)]. Further, the value of V_{BSAT} becomes less negative with increasing t_{EPI} as shown in Fig. 5.5(a). This is due to the reduced electrostatic control of the gate over the channel. Thus, a small reverse V_{BS} is sufficient to maximize the drain current for a given gate-drain bias.

Moreover, extremely thin t_{EPI} has a stronger gate control, whereas the extremely thick t_{EPI} has a weaker gate control. Thus the control of reverse V_{BS} becomes more dominating at the thicker epitaxial layer. Once the depletion charge in the channel starts to drop with V_{GS}, the slope of V_{BSAT} starts to change linearly [Fig. 5.5(b)], as modeled in (5.3)-(5.4). For thicker t_{EPI} ($\geq$ 5 nm), the channel remains depleted even at lower V_{GS}, thus V_{BSAT} is always linear with V_{GS}. On contrary, the channel depletes at higher V_{GS} for excessively thinner t_{EPI} ($\leq$ 3 nm). As a result, V_{BSAT} exhibit sub-linear trend at the lower V_{GS} and becomes linear at the higher V_{GS} [Fig. 5.5(b)]. It is worth highlighting that influence of the forward V_{BS} becomes pronounced for higher t_{EPI} due to the reduced gate control [Fig. 5.5(a)].

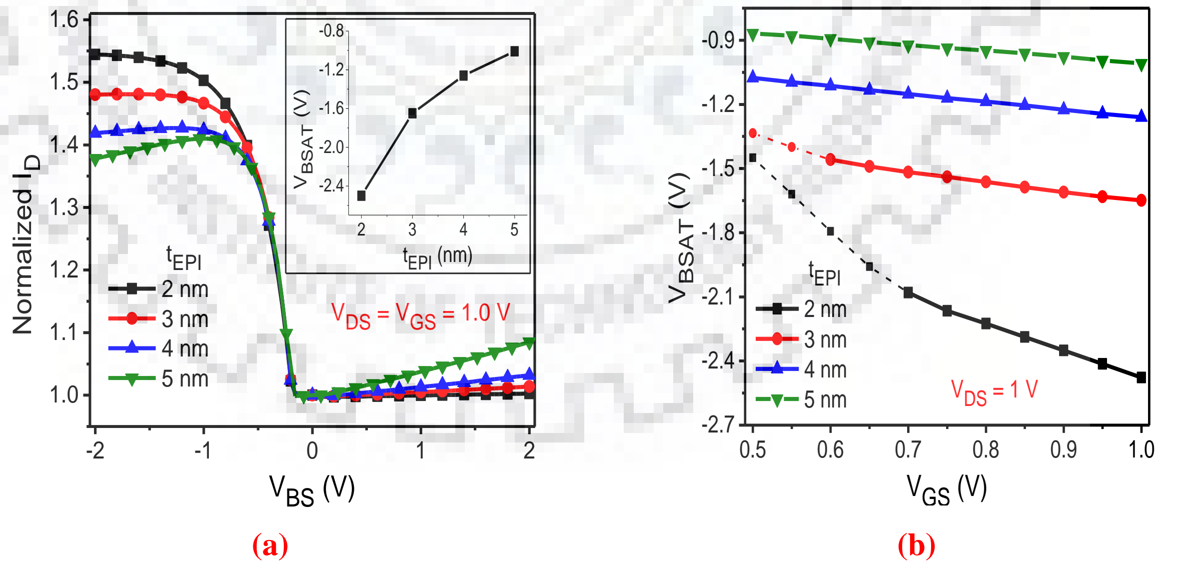


Figure 5.5: (a) Normalized I_D for different epitaxial layer thicknesses. Here I_D is normalized by its value at V_{BS} = 0 V. Inset shows the variation of V_{BSAT} with t_{EPI}. (b) Linear dependence of V_{BSAT} on V_{GS} is justified by the simulations and the model presented in Eq. (5)

5.4.3 Doping of epitaxial layer (n_{EPI})

The epitaxial layer doping is another design parameter for improving the drive current. As we increase n_{EPI}, electron BTBT generation across the degenerately doped p^+n^+ junction increases, [Fig. 5.6(a)]. The impact of reverse V_{BS} on the drain current modulation slightly decreases [Fig. 5.6(b)] with increasing n_{EPI}. This is due to a reduction in the modulation of F_n with increasing doping [Fig. 5.6(b)]. However, V_{BSAT} changes only to a small extent (-1.62 V to -1.65 V) when the doping is raised from 10^{16} cm^{-3} to 10^{19} cm^{-3}. This is because the change in depletion charge of the channel does not significantly change with a change in n_{EPI}. Therefore, the dependence of V_{BSAT} on V_{GS} is negligible, which can also be confirmed by the model discussed in subsection 5.3.1.

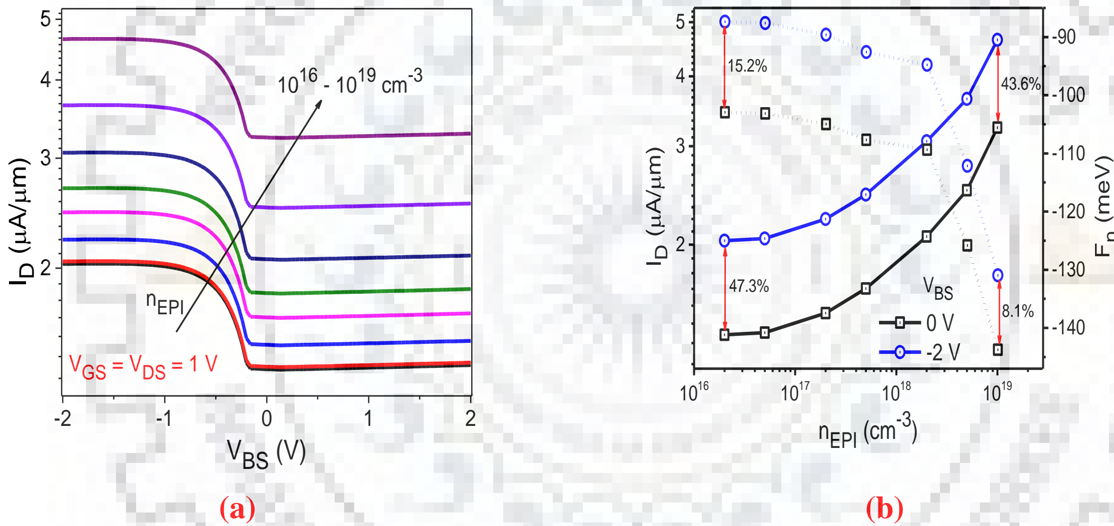


Figure 5.6: (a) Drain current for different values of n_{EPI}. (b) Comparison of percentage change in I_D and F_n for different values of n_{EPI} with and without reverse V_{BS}.

5.5 Impact of Body Biasing on the Analog Performance

This section explains the impact of body biasing on the vital analog parameters viz. transconductance (g_m), output resistance (r_o), gate capacitances (C_{gs}/C_{gd}) and intrinsic gain ($g_m \times r_o$) etc. of L-TFETs. The transconductance increases with the reverse V_{BS} and then attains a maximum as shown in Fig 5.7(a). This happens as the tunneling current increases with the reverse V_{BS} and then saturates. Further, g_m remains almost constant with the forward V_{BS} because BTBT does not change significantly, as explained in Section 5.3.2. Please note that the increment in g_m at higher V_{GS} is due to increased rate of tunneling. The output resistance

initially reduces (V_{BS} < 1 V) with the reverse V_{BS}, as the change in I_D is significant. When ΔI_D is small, r_o starts to increase with reverse V_{BS} as shown in Fig. 5.7(b). The forward V_{BS} reduces r_o as I_D continuously increases, to a small extent. The intrinsic gain in effect increases with reverse V_{BS} because of increasing behavior of g_m, while it remains almost unchanged with the forward V_{BS} [Fig. 5.7(b)].

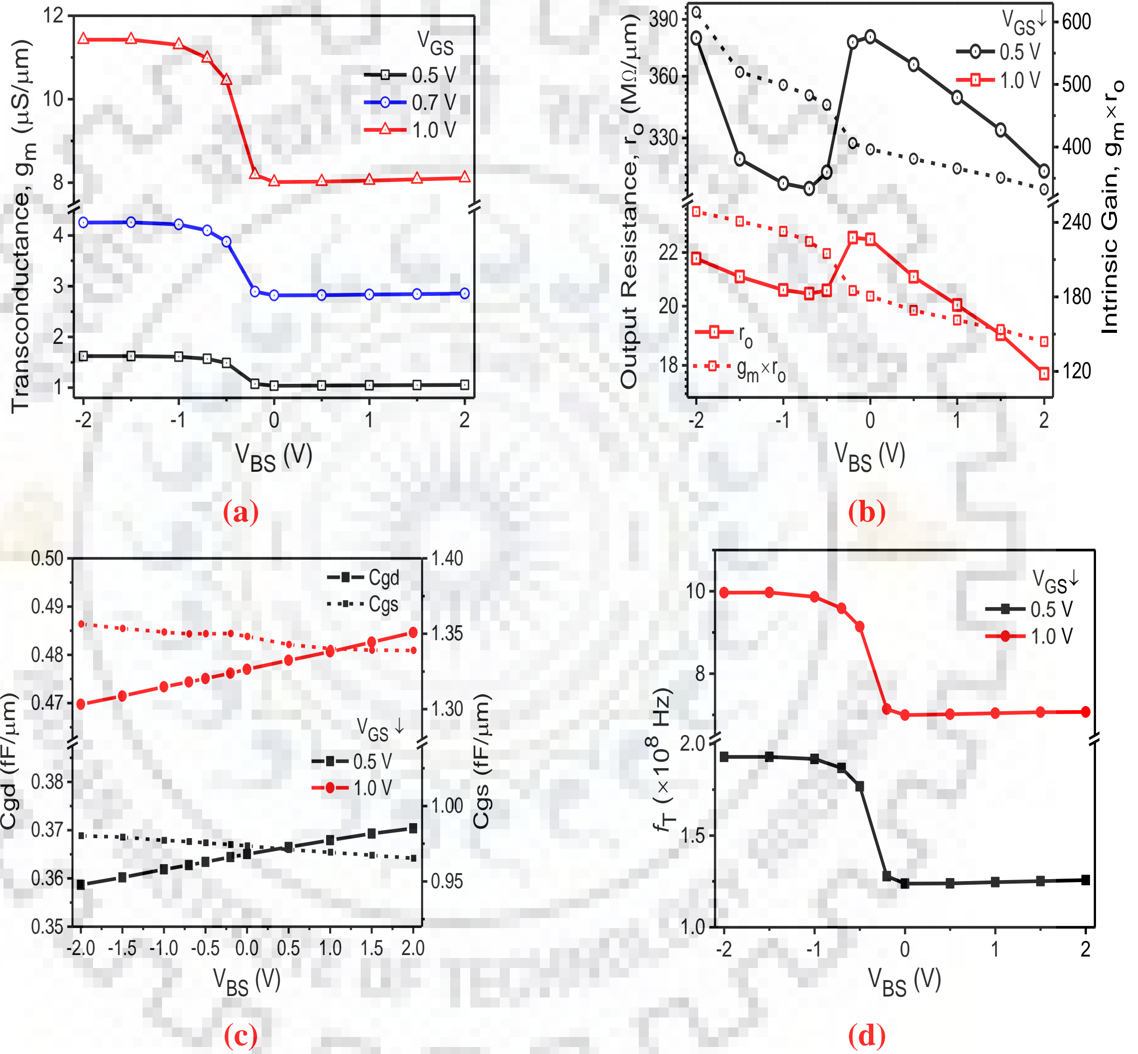


Figure 5.7: Performance of analog parameters under the forward and reverse body biasing at V_{DS} = 1.0 V: (a) Transconductance (b) Output resistance and intrinsic gain (c) Gate capacitances (d) Unity gain cut-off frequency

The variation in C_{gd} of L-TFET with V_{BS} is attributed to the change in depletion charge of the channel. Moreover, the channel electron density decreases with the reverse V_{BS} and

increases with the forward V_{BS}. In addition, C_{gs} is augmented to a little extent with reverse bias due to increased tunneling charge across the EoS/source junction, as depicted in Fig. 5.7(c). It is worthwhile to mention that a significant change in C_{gs} is observed with varying V_{GS}, as the BTBT generation increases to a great extent. Finally, the unity gain cut-off frequency (f_T) of the device under consideration is shown in Fig. 5.7(d). The trend of f_T is dominated by the device transconductance. This is because the device's total capacitances exhibit a negligible change (~1%) with reverse V_{BS}, when compared to the transconductance (40-60%). Therefore, the reverse body bias is essentially useful for the analog designer to adjust the gain and bandwidth of the circuit.

5.6 Conclusion

In this work, we presented strong arguments so as to why, the drain current of L-TFETs modulates with the body bias. We also proposed a physics based model for V_{BSAT}. As per the trends of electron quasi-Fermi energy levels in the valence band of the source, I_D-V_{BS} characteristics assume different shapes. This is by virtue of the fact that the occupancy probability changes with the body bias. In fact, our study reveals that the reverse V_{BS} has a notable influence on I_D compare to the forward V_{BS}. Further, the linear dependence of V_{BSAT} on V_{GS} is also confirmed by our numerical TCAD simulations and proposed model. This is owing to the fact that both ΔE_C and Ψ_C are linear with V_{GS}. We also investigated that the change in V_{DSAT} with body bias is not symptomatic. However, V_{BSAT} fluctuates with the change in epitaxial layer thickness, channel length, and the gate-source overlap length. Finally, we demonstrated that the intrinsic gain and unity gain cut-off frequency are significantly improved with reverse body biasing. This improvement is dictated by the enhanced transconductance of L-TFETs, while keeping the gate capacitances almost independent of the body bias. The superior drive capability and analog performance due to the body bias can be further explored in L-TFETs based circuit design.

Chapter 6

Impact of Gate-Source Overlap Length on Small Signal Parameters of Line TFETs

In the previous chapters, the impact of the gate, drain, and body bias on the TFET device-circuit performance was investigated in detail. In this chapter, the impact of gate-source overlap on L-TFETs is examined. The gate-source overlap length (L_{OV}) in the L-TFET can be used as a design parameter to improve the analog circuit performance. In this chapter, we modeled the drain current (I_D) dependence on L_{OV} considering the electrostatics of the gate-source overlap region. It is observed that an increase in I_D with the increasing L_{OV} exhibits a nonlinear behavior. This happens as the impact of lateral electric field at the far end of the tunnel junction reduces, thereby reducing the tunneling rate. Based on our semi-empirical physics based I_D-L_{OV} model a novel L_{OV} variation-aware small signal model for L-TFET is also presented. The output resistance (r_o) and the gate-drain capacitance (C_{gd}) remain almost independent of L_{OV} in the saturation regime. The gate-source capacitance (C_{gs}) and the transconductance (g_m) linearly increase with L_{OV}. A common source amplifier is demonstrated with ~ 2.4 × increase in the voltage gain when L_{OV} is increased from 20 nm to 50 nm, with a penalty of ~ 10% in the bandwidth. We observe that it is not possible to achieve the gain similar to one obtained using 2.5× increase in L_{OV} even after increasing the device width 5 times. However, the bandwidth reduces 30% at such width owing to an increase in the gate capacitances.

6.1 Introduction

The research on TFETs over the last decade has shown the potential of this device for energy efficient computing [2], [131]. In this context, tremendous efforts have been made to improve the drive current and subthreshold swing of TFETs. The optimization of TFETs from the process to material engineering have been extensively discovered [132]. The benchmarking of TFETs for the low power low voltage analog and digital application are also being explored

rigorously [95], [133], [134]. Recently, on-chip implementation of line-TFET based analog circuits has increased the interest of in such devices [88], [96]. In this context, an experimental demonstration of L-TFET devices for the Internet of Thing (IoT) applications has also been reported [94].

In general, the width of the device is used to improve the drive capability. However, an increase in the device width also results in the increased gate capacitances and decreased output resistance. The overlap lengths of L-TFETs can also be employed in the circuits to increase the drive current, without much affecting its r_o. Further, it has been established as a fact that the gate-source overlap length is an important design parameter in L-TFETs [29]. Thus, this parameter may provide an additional degree of freedom to the analog designer to adjust the gain and bandwidth of the circuit. It is observed through the numerical simulations that the drain current varies sub-linearly with L_{OV} [27], [31], [123]. However, the existing analytical models assume that I_D should increase linearly with L_{OV}, by virtue its increased area of the cross-section for band-to-band tunneling (BTBT) [61]. Thus, there is a need to quantify the change in drain current as a function of L_{OV} for the circuit designers.

Therefore, in this work, while addressing the problem cited above, a physics based explanation of the dependence of I_D on L_{OV} in the saturation regime is presented comprehensively. The drain current initially increases linearly with L_{VO}, thereafter, a sub-linear trend is observed. This happens as the impact of lateral electric field diminishes at the far end of the gate-source overlap region. The impact of L_{OV} on vital analog performance parameters is also discussed while explaining the underlying physics of them. This facilitates the analog designer to predict the gate-source overlap length aware small signal model for L-TFETs based circuits. This model is also validated against the numerically simulated results. Finally, the advantage of L_{OV} variation over the width is also examined for the common source amplifier. It is interesting to note that the pillar based L-TFET with a vertical process flow [135] does not exhibit such a non-linear behavior, as discussed later in Section 6.3.3.

The rest of the Chapter is organized as follows: Section 6.2 describes the device structure and the simulation framework. The dependence of I_D on L_{OV} is explained in Section 6.3. A mathematical approach is also presented to model such an effect. Section 6.4 presents the influence of L_{OV} on the analog parameters and also provides a physics based semi-empirical model for the same. Impact of L_{OV} variation on the analog circuit design is discussed in Section 6.5. Lastly, the important results and conclusions are drawn in Section 6.6.

6.2 Device Design and Simulation Framework

The device under consideration is an epitaxial layer based line tunneling FET [27] as shown in Fig. 6.1(a). Epitaxial layer/source pockets are significant to improve the turn-on characteristics of the device [120]. The device consists of a 3 nm epitaxial layer of *Silicon* and a low bandgap $Si_{1-X}Ge_X$ source is used to improve the drive capability of the device. The content of *Germanium* in the source is kept at 50% in order to achieve a defect-free interface [27]. The length of the channel is chosen as 20 nm unless otherwise stated. A high-κ metal gate stack with a dielectric layer of 3 nm HfO_2 is selected for better electrostatic control of the gate. The gate-source overlap length is kept varying in order to carry out our study. A heavily doped substrate is used along with a 10 nm thick BOX region of SiO2, as shown in Fig. 6.1(a). The doping of drain, channel, source, and epitaxial region are 5×10^{19} (n-type), 1×10^{16} (p-type), 2×10^{20} (p-type) and 2×10^{18} (n-type) respectively, as done in Chapter 5.

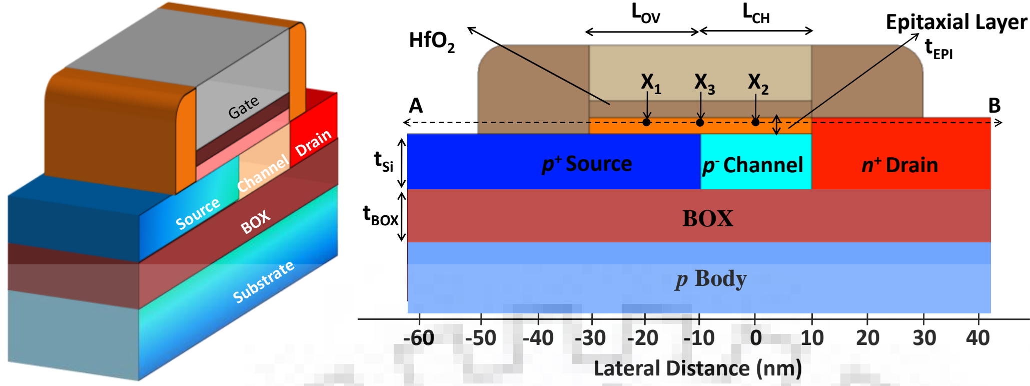
Next, to perform 2D numerical simulations, Sentaurus TCAD tool of Synopsys Inc. is used in this work. The dynamic nonlocal path tunneling model is used to capture the band-to-band tunneling generation rate at all possible interface. This model utilizes the nonlocal generation of the electrons and holes caused by the direct and phonon-assisted BTBT process. The generation rate is calculated from the nonlocal path integration. The Kane-Keldish formula used in the numerical simulation for the calculation of BTBT is as under [106]:

$$R_{net} = A\left(\frac{E}{F_O}\right)^P \exp\left(-\frac{B}{E}\right) \tag{6.1}$$

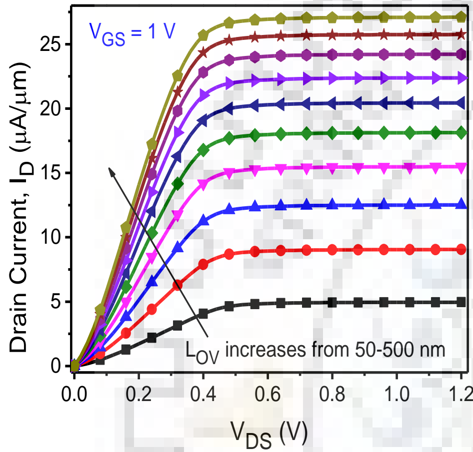
Here, the prefactor A and exponential factor B are the constants of Kane-Keldish model, and E is the electric field. These constants depend upon the reduced masses of the electron and hole. Rests of the physical models are same as mentioned in Chapter 3.

6.3 Dependence of I_D on L_{OV}: Physical Insights

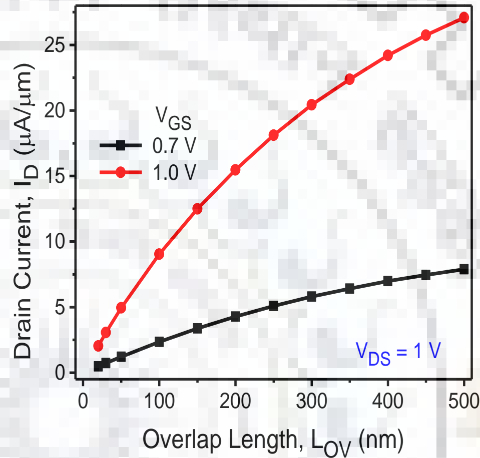
This section explains the behavior of drain current with the variation in gate-source overlap lengths. This will be used in analyzing L-TFET small signal parameters for the analog circuit design. It may be noted that I_D always increases with L_{OV}, due to the increased area of cross-section for BTBT generation, however the rate of increment changes with the variation in L_{OV}. First, the cause of nonlinear increase in I_D with L_{OV} is explained with a physical insight, followed by a semi-empirical model for the drain current.



(a)



(b)



(c)

Figure 6.1: (a) 3-D view and 2-D schematic of the target device. (b) The variation in drain current with increasing L_{OV}. (c) The non-linear trend of I_D with L_{OV} extracted from (b).

6.3.1 Why I_D increases sub-linearly with L_{OV}

As shown in Fig. 6.1(b), the drain current increases almost linearly for $L_{OV} \leq 200$ nm. It is worth highlighting here, that almost 5× increase in I_D is found when L_{OV} is raised from 20 nm to 100 nm as shown in Fig. 6.1(c). Afterward, a sub-linear increase in I_D with L_{OV} is noticed. For instance, when L_{OV} is raised from 100 nm to 500 nm, merely an increase of 3× is found in I_D. The physics behind this phenomenon is as follows: the potential within the epitaxial region over the source (EoS) varies with increasing the overlap length, as depicted in Fig. 6.2(a). It is clear from Fig. 6.1(a) that the gate voltage is uniformly applied to the overlap region. Therefore, the gate normal electric field is assumed to be uniform across the epitaxial region underneath the gate. However, the potential reduces exponentially with the increasing L_{OV}. This change in the potential is due to the lateral component of the electric field, which continuously

changes at the junction between the source and the epitaxial layer, as shown in Fig. 6.2(b). In addition, the EoS region is fully depleted and the space charge is uniform owing to the uniform doping of the region.

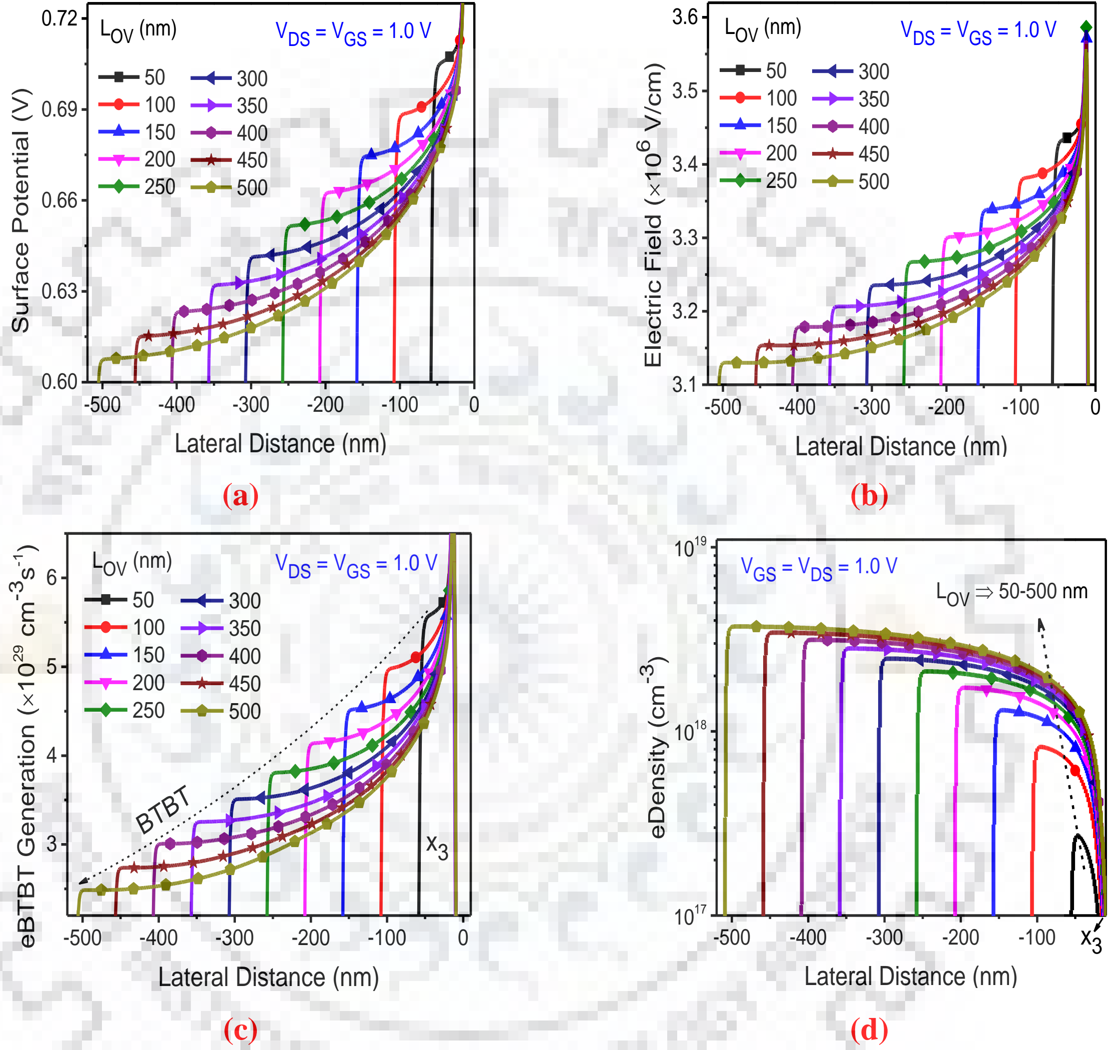


Figure 6.2: (a) Potential profile along the line AB within EoS region [Fig. 6.1(a)]. (b) The magnitude of the electric field at the source-EoS junction. (c) Variation in the electron band-to-band generation and (d) electron density along the line AB [Fig. 6.1(a)].

Thus, two dimensional Poisson's equation can be applied to estimate the potential profile (Ψ) of the EoS region underneath the gate [3]:

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = -\frac{\rho}{\epsilon_{si}} \tag{6.2}$$

$$\frac{\partial E}{\partial x} + \frac{\partial E}{\partial y} = -\frac{\rho}{\in_{Si}} \tag{6.3}$$

Here, ρ is the space charge in the EoS region and E is the electric field. The general solution of the above said equations can be represented as:

$$\psi = A_1 \exp(\alpha x) + A_2 \exp(-\alpha x) = A_2 \exp(-\alpha x) \tag{6.4}$$

Where, $x = 0$ at the point x_3 and $x = L_{OV}$ at x_n, and α is a fitting parameter. The constant $A_1 = 0$, otherwise the value of Ψ becomes infinite when $x \rightarrow \infty$. The potential of EoS region exponentially decreases as we move away from the source-channel junction (x_3) towards the far end of the gate-source overlap (x_n) [i.e. as L_{OV} is increased] according to (6.4). The electric field can be represented as:

$$E = -\frac{d\psi}{dx} = \alpha A_2 \exp(-\alpha x) = \alpha A_2 (1 - \alpha x + \ldots) \tag{6.5}$$

Therefore, the electric filed at the EoS/source junction also reduces exponentially. It may be noted that the change in the electric field with L_{OV} is small enough [Fig. 6.2(b)]. Thus, a linear approximation of the electric field can also be considered by neglecting the higher order terms, as in (6.5). This approximation is justified as the vertical electric field is constant and this change in total electric field is only due to lateral component.

BTBT at the point x_n is found to be different than x_3 [Fig. 6.2(c)]. It is observed that BTBT at the far end (x_n) drops to 2×10^{29} $cm^{-3}s^{-1}$, when compared to 6×10^{29} $cm^{-3}s^{-1}$ at the point x_3, for L_{OV} of 500 nm. However, the electron density at the far end is slightly more owing to a reduced potential (4), as shown in Fig. 6.2(d). Further, the difference E_C-F_n within the EoS region also decreases as one move towards the cut plane C1 to C6 [Fig. 6.3(a)]. It is noteworthy to mention here, the overall I_D remains always high at the increased L_{OV}, due to the increased area of the cross-section for BTBT.

To get further insights into the above observations, we performed the numerical simulations on L-TFET device having L_{OV} = 300 nm [Fig. 6.3(a)]. Next, the vertical energy bands at the source epitaxial layer junction are obtained for various cross-sections C1-C6 at the regular intervals (from point x_3), as shown in Fig. 6.3(a). This enables us to find the change in tunneling distance at the source-EoS junction with the increasing overlap lengths. Interestingly, an increase in the tunneling distance is observed between the cross section C1 and C6 [Fig. 6.3(b)]. In fact, the reduced electric field causes BTBT to reduce at the far end of the overlap

region (x_n). Therefore, we may confirm that, a sub-linear increase in the I_D is caused by the phenomenon just explained above. Hence, there must be a decaying factor associated to the drain current at higher gate-source overlap lengths, apart from its linearly increasing trend. We also observe similar effects in a recently reported pillar structure based line TFET [135], however, these effects are only prominent at very high L_{OV}, as discussed later in subsection 6.3.3.

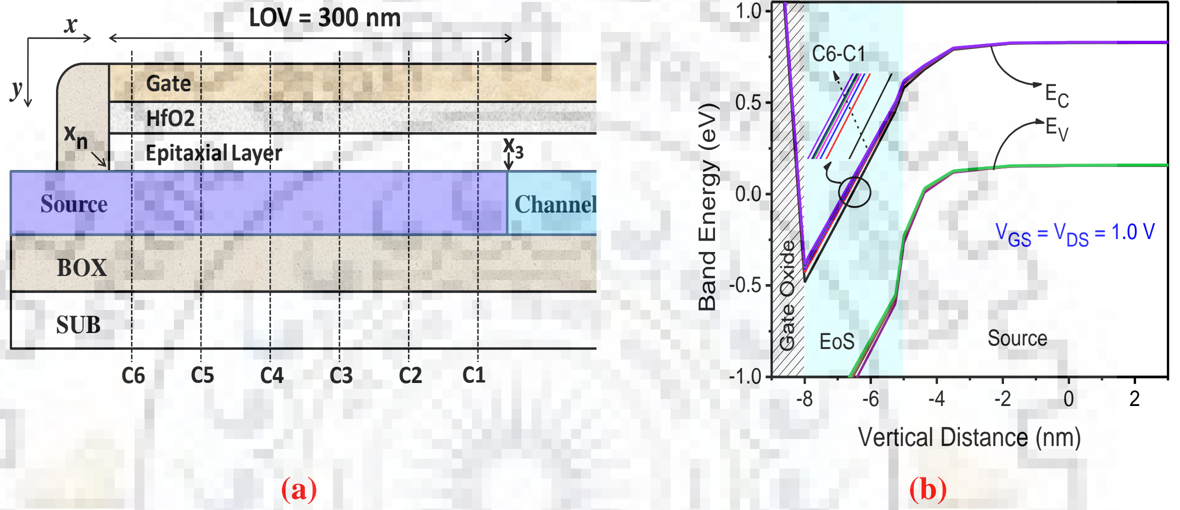


Figure 6.3: (a) Cross section of L-TFET underneath the gate. Equi-distant vertical cut planes are indicated using $C1$-$C6$. Please note that the starting point of gate-source overlap region is x_3, whereas far end is denoted by x_n. (b) Band energies for cut planes $C1$-$C6$ are plotted to find the tunneling distance.

6.3.2 Semi-empirical model for I_D-L_{OV} characteristics

The existing analytical model assumes that I_D increases linearly with the increasing L_{OV} [i.e. $I_D \propto L_{OV}$] for L-TFETs [60]. On the contrary, several experimental and simulation results clearly indicate a non-linear relation between I_D and L_{OV} [27], [31], [59], [139]. We also observe a sub-linear increase in I_D with an increase in L_{OV} [Fig. 6.1(c)]. Therefore, the drain current should be predicted by considering the exponential potential profile within the EoS region (6.4)-(6.5). In order to calculate I_D, BTBT generation rate of (6.1) can be integrated over the overlap length, assuming the variation in other dimensions is negligible:

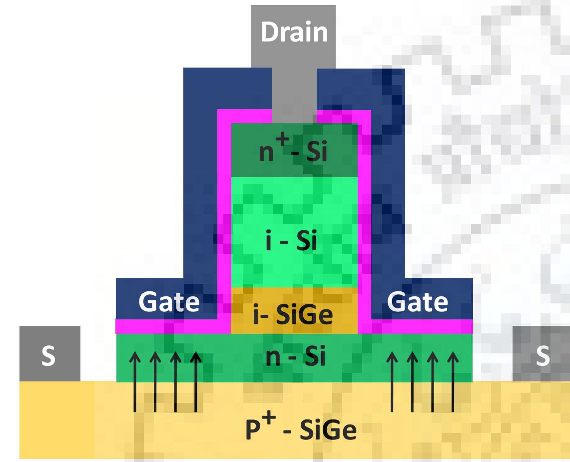
$$I_D = \int R_{net} dv \tag{6.6}$$

Substituting (6.1), (6.4) and (6.5) into (6.6), I_D becomes:

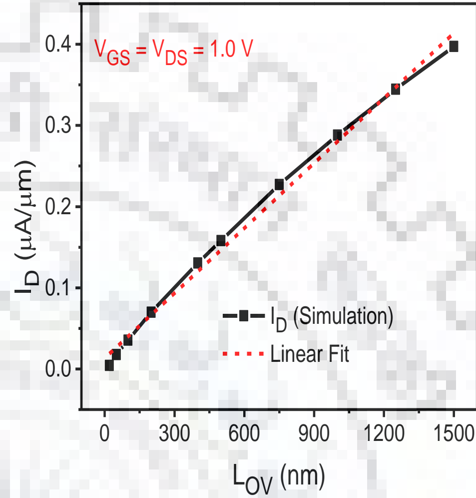
$$I_D = \int_0^{L_{OV}} A\left(\frac{\alpha A_2(1-\alpha P x)}{F_O}\right)\exp\left(\frac{-B}{\alpha A_2(1-\alpha x)}\right)dx \tag{6.7}$$

After simplifying and rearranging (6.7), we get:

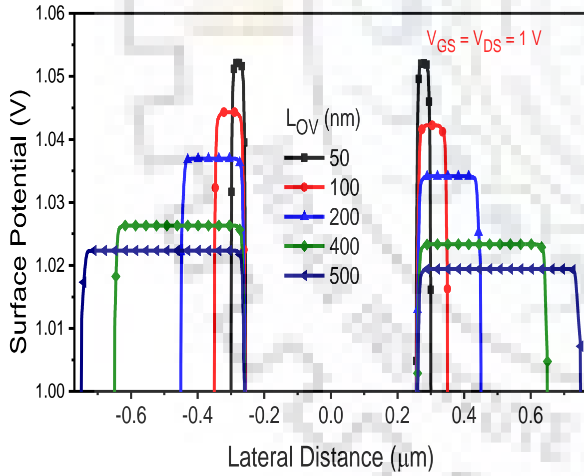
$$I_D \propto L_{OV}\exp(-\beta L_{OV}) \tag{6.8}$$



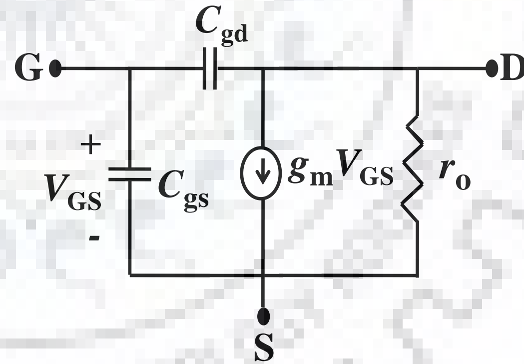
(a)



(b)



(c)



(d)

Figure 6.4: (a) 2D schematic of pillar based line TFET with vertical process flow [135]. (b) Drain current changes almost linearly with L_{OV}. (c) Potential profile within the EoS region. (d) Small signal model for L-TFET.

Eq. (6.8) indicates that I_D increases linearly for the smaller gate-source overlap, whereas, I_D starts to increase sub-linearly for the higher values of L_{OV}. The proposed semi-empirical model is also validated against the simulation results of Fig. 6.2(c). With an appropriate selection of

the constant β, a perfect fit between simulated and modeled data can be obtained.

6.3.3 Impact of device geometry on I_D-L_{OV} characteristics

We observe that the geometry of the device strongly influences the nature of I_D-L_{OV} characteristics. For instance, a recently reported pillar based L-TFET has vertical process flow is depicted in Fig. 6.4(a). It is to be noted, the drain is not laterally aligned with the source, whereas the drain remains always aligned with the source in the target device [Fig 6.1(a)]. This device exhibits almost linear dependence on L_{OV} up to 1500 nm gate-source overlap [Fig. 6.4(b)]. This is owing to the fact that the drain terminal has very little influence on the potential underneath the gate terminal as confirmed by Fig. 6.4(b). Thus the lateral electric field due to the drain is not going to affect the potential profile of the gate-source overlap region. Therefore, the potential of the gate-source overlap region remains almost flat with any further increase in L_{OV}, as shown in Fig. 6.4(c). On the contrary, the device shown in Fig. 6.1(a) has a more influence of the drain on the potential within EoS region [Fig. 6.2(a)] by virtue of its lateral drain to source alignment.

6.4 Dependence of Small Signal Parameters on L_{OV}

This section discusses the performance of vital analog parameters with the variation in L_{OV} when the device operates in the saturation regime. A gate-source overlap length variation-aware small signal model for L-TFETs is also presented, as shown in Fig. 6.4(d). The transconductance (g_m) follows the trend of I_D, hence increases with L_{OV} [Fig. 6.5(a)], g_m can be represented as:

$$g_m \propto L_{OV} \exp(-\beta L_{OV}) \tag{6.9}$$

It is interesting to note that g_m will increase linearly with L_{OV} for the pillar based structure owing to a linear I_D-L_{OV} behavior, as shown in Fig. 6.4(b). The output resistance (r_o) is high for the smaller gate-source overlap ($L_{OV} \leq 50$ nm) owing to the reduced BTBT (i.e. the drive current is small). Afterward, it decreases slightly and attains an almost constant value. It can be observed that r_o remains fairly constant for $L_{OV} \geq 100$ nm, as shown in Fig. 6.5(a). This happens as the EoS region is almost fully depleted, and the change in charge is not significant. Further, a change in the potential due to V_{DS} is prominent near the point x_3 of the EoS region. Besides, the influence of the drain on the far end of the tunneling junction gets diminished, as

the gate-source overlap is increased, resulting in r_o to remain almost invariant at the larger L_{OV}.

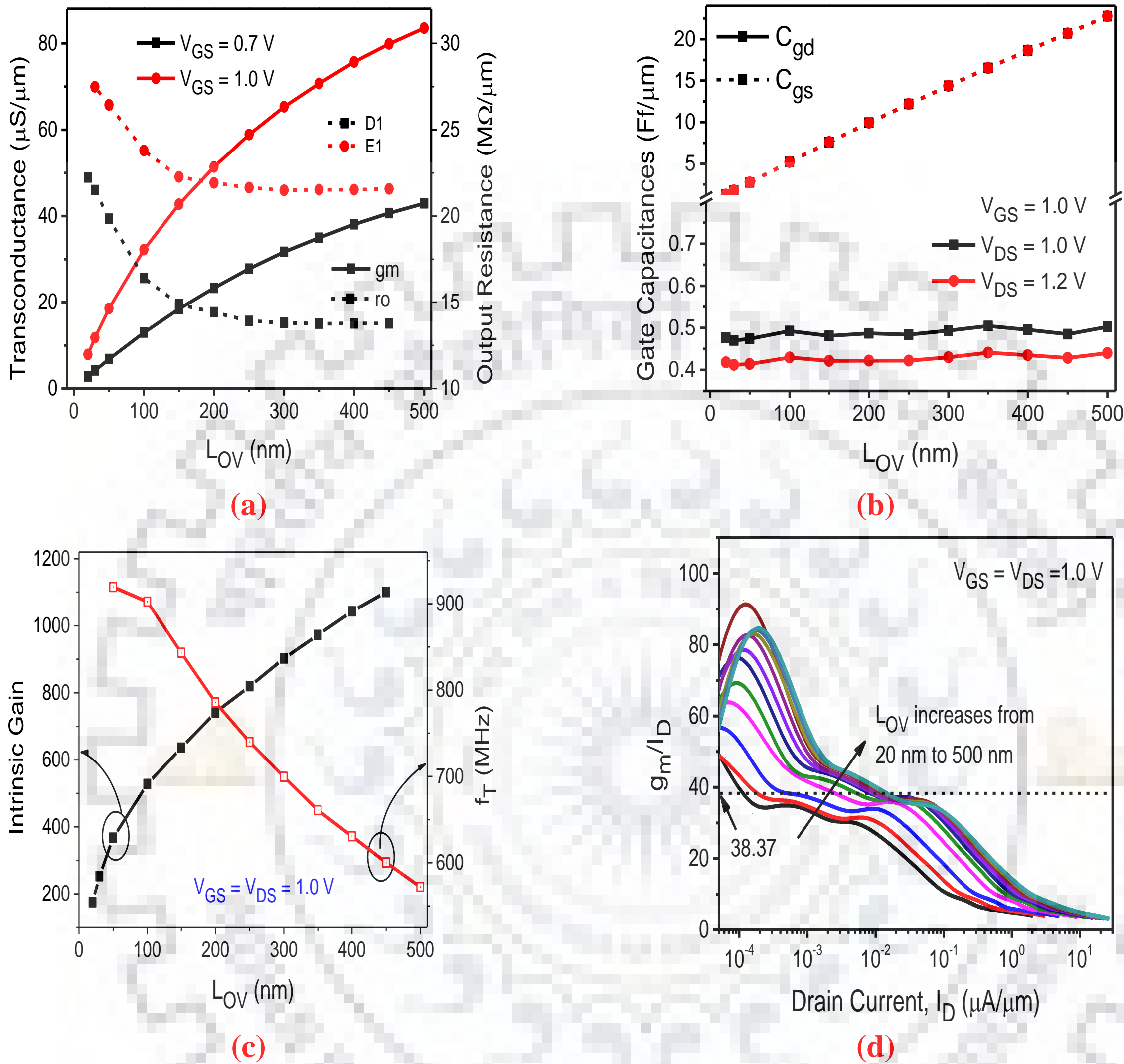


Figure 6.5: Performance of analog parameters with the gate-source overlap lengths (a) Transconductance and output resistance (b) Gate capacitances (c) Intrinsic gain and unity gain cutoff frequency. (d) Variation in g_m/I_D with drain current.

It worth highlighting, a decrease of ~ 30 % is observed in r_o when L_{OV} is increased from 20 nm to 100 nm. Whereas, less than 10 % decrease in r_o is found when L_{OV} is increased from 100 nm to 500 nm. These results can also be justified by carefully examining the variation of the surface potential and electron BTBT along the gate-source overlap of 500 nm [Fig. 6.2(a)-(c)]. A sharp decrease in the potential and electron BTBT is observed up to the overlap segment of 100 nm. Thereafter, a sluggish response of these physical quantities is expected, as discussed

above. This distinct feature of r_o-L_{OV} relation can be explored in circuit design. For instance, the voltage gain of an amplifier can be adjusted with an appropriate selection of L_{OV}, without much affecting its r_o and bandwidth. In contrast, an increase in the width to improve the drive capability of the device will result in a degraded bandwidth and outputresistance owing to the fact that the influence of drian will remain same. Initially, r_o exhibits an exponentially decaying relation with L_{OV}, and then attains a constant value, as shown in Fig. 6.5(a), and can be approximated as:

$$r_o = R_1 - R_2 \exp(-\omega L_{OV}) \qquad 6.10$$

Where, R_1, R_2, and ω are the fitting constants. However, for $L_{OV} \geq 100$ nm, r_o can be considered independent of L_{OV} for the small signal modeling, as r_o is almost constant.

The variation of the gate capacitance with L_{OV} is shown in Fig. 6.5(b). The gate-drain capacitances (C_{gd}) are almost invariant of L_{OV} in the saturation regime. This is owing to the fact that the channel is almost depleted in the saturation, thus the overlap lengths will not affect C_{gd}. However, the gate-source capacitance (C_{gs}) increases linearly with L_{OV}, due to an increase in the cross section area of tunneling. Therefore, C_{gs} is found to be proportional to L_{OV} in the saturation regime. The first order modeling of the capacitances in the saturation regime is straightforward and can be represented as:

$$C_{gd} \neq f(L_{OV}) \qquad 6.11$$

$$C_{gs} \propto L_{OV} \qquad 6.12$$

The basic small signal model for L-TFET is shown in Fig. 6.4(d). The intrinsic gain always increases with L_{OV}, as the transconductance increases. These increasing trends are sub-linear as in the case of I_D and g_m. However, a reduction in unity gain bandwidth [Fig. 6.5(c)] is observed due to the increased gate-source capacitance. It may be noted that almost L_{OV} independent nature of C_{gd} is useful in many circuits, as the miller capacitance will not change with L_{OV}. The value of, g_m/I_D [Fig. 6.5(d)] in subthreshold region can be formulated as:

$$\frac{g_m}{I_D} = \frac{\ln(10)}{SS} \qquad 6.13$$

For FDSOI and FinFET technologies at the room temperature, SS > 60 mV/decade, due to the thermionic emission of the carriers and it cannot be scaled down further. Therefore, g_m/I_D is always less than 38.37 for FDSOI and FinFET technology [Eq. 6.13]. However, g_m/I_D is sufficiently high for TFETs because of their inherent BTBT transport mechanism.

6.5 Impact of L_{OV} on the Analog Circuit Design

As explained in the previous section, L_{OV} is an important design parameter for the analog circuits. Therefore, this section explores the significance of L_{OV} variation over the width variation for designing a common source amplifier. Here, *p*-type L-TFET is used as a current source load with its gate terminal connected to V_{bias}, as shown in Fig. 6.6(a). For a *p*-type L-TFET, *SiGe* is kept in the epitaxial layer in order to obtain the CMOS compatible drive currents. An opposite and equal doping of *n*-type L-TFET is used in the different regions of *p*-type L-TFET. The saturation voltages are determined by our V_{DSAT} extraction method [136]. To perform the circuit simulations, electrical characteristics (*I-V* and *C-V*) of L-TFET are extracted using numerical TCAD simulations for the finely varying gate and drain voltages. Next, a Verilog-A based look-up table approach is used to interpolate these data [92]. These Verilog-A models are used to predict the gain and bandwidth of CS amplifier in SPICE environment

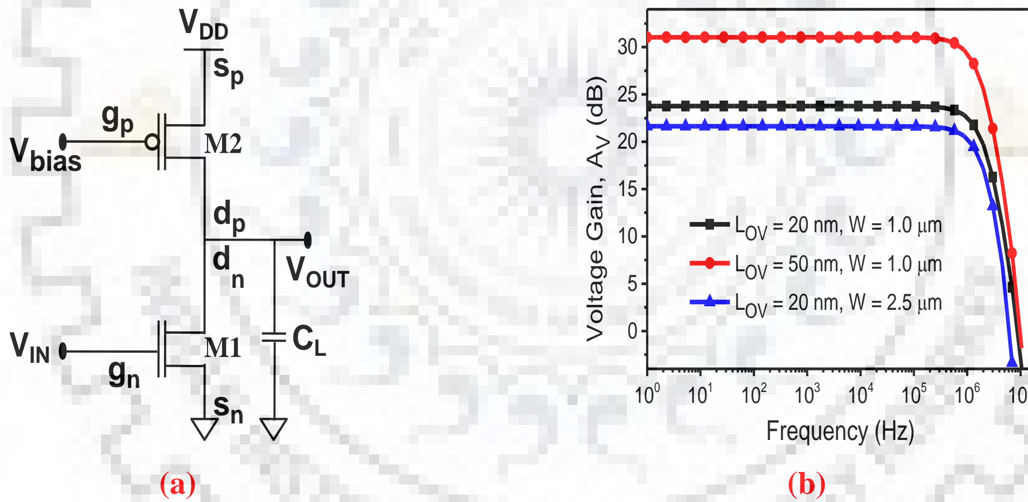


Figure 6.6: (a) Schematic of Common Source Amplifier (b) Frequency response of the common source amplifier. The DC output voltage is kept $V_{OUT} = V_{DD}/2$ for all the cases, where $V_{DD} = 0.6$ V. Please note that width and L_{OV} of *n*-LTFET (M1) are varied while keeping the parameters of *p*-LTFET (M2) unchanged.

First, we design a CS amplifier with L_{OV} = 20 nm for both *n*- and *p*-L-TFETs. The output voltage (DC operating point) of the CS amplifier is adjusted to be $V_{DD}/2$ for all the experiments. The voltage gain and bandwidth of the said amplifier are measured as ~23 dB and ~2.67 MHz respectively, as shown in Fig. 6.6(b). Next, L_{OV} of *n*-L-TFET is increased to 50 nm without

affecting the other parameters. This provides a voltage gain (bandwidth) of ~31 dB (~2.3 MHz), because of an almost 2.5× increase the transconductance of *n*-L-TFET. This also matches with our L_{OV} variation-aware semi-empirical small signal model [Eq. (6.8)]. Therefore, our proposed model can be used for the analog design. With a 2.5× increase in L_{OV}, the bandwidth decreases by almost 10 % because C_{gs} increases linearly with L_{OV} [Fig. 6.5(b)]. On the contrary, we observe an almost 2.4× improvement in A_V when L_{OV} is raised from 20 nm to 50 nm. In addition, for a similar (2.5×) increase in the device width, merely 21.6 dB of gain is observed with a bandwidth of ~2.6 MHz. This is because of the fact that the device capacitances increase and the output resistance decreases with the increasing device width. Besides, it is very difficult to achieve A_V of ~31 dB by merely increasing the device width. We obtain a maximum A_V ~28 dB and bandwidth of ~1.9 MHz, with a 5× increase in the device width. Therefore, we strongly believe that L_{OV} variation in L-TFETs can be used as an important design parameter in the analog circuits.

6.6 Conclusion

In this chapter, the dependence of small signal parameters on L_{OV} is illustrated with a mathematical model. We explained a reason behind the sub-linear dependence of the drain current on the gate-source overlap lengths for L-TFETs. This happens as the impact of the lateral electrical field due to drain diminishes at the far end of the gate-source overlap. The exponentially decaying potential profile in the gate-source overlap region is obtained from the two dimensional Poisson's equation. This also confirms a sub-linear trend of I_D-L_{OV} characteristics. Therefore, a semi-empirical model for I_D-L_{OV} relation is established for the device under consideration. Further, a linear dependence of the drain current on L_{OV} can be obtained using pillar based L-TFETs, whereby, the influence of drain bias is not significant on the tunneling junction. An increase in L_{OV} causes g_m to increase, whereas, r_o remains almost unaltered at the higher L_{OV}. The value of C_{gd} is almost independent of L_{OV}, while C_{gs} increases linearly. Finally, the gate-source overlap variation-aware small signal model is also presented for L-TFETs. The voltage gain of the CS amplifier increases from 23 dB to 31 dB without any significant decrease in the bandwidth, when L_{OV} is increased from 20 nm to 50 nm. Therefore, the parameter L_{OV}, when compared to the variation in the device width, provides an additional degree of freedom to the circuit designer.

Chapter 7

Conclusions and Future Scope

In this chapter, we conclude the major findings and the novelty of our work. TFETs are most suitable for the ultra-low power analog applications, such as IoT sensors. In this thesis, the biasing strategies and the small signal models are examined to obtain the optimal analog circuit performance. A physical insight of the drain current saturation in TFET is comprehensively presented and an extraction method to determine their V_{DSAT} is also illustrated. The impact of body bias and the gate-source overlap length on the epitaxial layer based line TFETs are also discussed. L_{OV} is an important design parameter in the analog circuit design; therefore, L_{OV} variation-aware small signal model is derived in this work. Moreover, the analog design aspects of TFETs are discussed using the device/circuit interactions. The physics discussed here is focused on the general trends and is immensely useful for developing the future analytical model for analog circuit design using TFETs.

7.1 Conclusions

We have proposed a novel V_{DSAT} extraction method to estimate the onset of *soft* and *deep* saturation voltages for the point TFET using a phenomenological approach. It is found that V_{GD} remains constant in both the *soft* and *deep* saturation regimes. The extracted value of the *soft* saturation voltage is $V_{DSAT}^{s} = V_{GS} - V_{TH}^{MOS}$ and for the *deep* saturation voltage is $V_{DSAT}^{d} = V_{GS}$, where V_{TH}^{MOS} is the voltage at which the strong inversion in the channel of TFET is attained. V_{DSAT} varies linearly with V_{GS}, hence it is feasible for the circuit designers to estimate the bias points accurately. The proposed method is further validated through the numerical TCAD simulations and the experimental data. The total gate capacitance remains at minimum in the *soft*/*deep* saturation; hence a large bandwidth is expected for the amplifier. A common source amplifier biased in *soft* saturation is demonstrated to have a comparable voltage gain and bandwidth to the one biased in *deep* saturation. Further, a detailed investigation regarding the

influence of device design parameters on V_{DSAT} and the analog performance of the device is performed with an in-depth explanation.

We presented a comprehensive physics based explanation of the output current saturation and an extraction method of V_{DSAT} for the line tunneling based TFETs, for the first time. The experiments carried out in this work show that V_{DSAT} of L-TFET does not change with L_{OV}. The values of V_{DSAT} are extracted from the capacitance-voltage characteristics, measured for the different gate-source overlap lengths. A change in the values of t_{EPI} and n_{EPI} significantly shift the onset of *soft* saturation condition in the L-TFETs, consequently, this also impact the analog performance. Overall results indicate that our method adequately allows determining the optimal terminal voltages for biasing L-TFETs based analog circuits in the *soft* and *deep* saturation regimes. A nominal change of ~ 5 % in the voltage gain is observed when the driver transistor of the common source amplifier is either biased in the *soft* or *deep* saturation regime, without any significant change in the bandwidth. This confirms the necessity of the correct estimation of $V_{DSAT}^{s,d}$ for the appropriate biasing of circuits. Finally, the optimization guidelines to quantify the device/circuit analog performance are also presented for the TFET research community by considering the impact of device design parameters.

We presented strong arguments for the modulation of the drain current of L-TFETs with the body bias. An increase of 40-60 % in the drain current of L-TFET is observed with the change in V_{BS}. As per the trends of electron/hole quasi-Fermi energy levels, I_D-V_{BS} characteristics assume different shapes. A mathematical model to determine V_{BSAT} is proposed for the circuit designers. The linear dependence of V_{BSAT} on V_{GS} is also confirmed by simulations and mathematical models. This happens as both ΔE_C and Ψ_C are linear with V_{GS}. We investigated that the change in V_{DSAT} with the body bias is not symptomatic. However, V_{BSAT} fluctuate with the change in epitaxial layer thickness, channel length, and the gate-source overlap length. We demonstrated that the intrinsic gain and unity gain cut-off frequency are significantly improved with the reverse V_{BS}. This improvement is dictated by the enhanced g_m, while the gate capacitances are almost independent of V_{BS}. The superior drive capability and analog performance due to the body bias can be further exploited in the L-TFETs based circuit design.

Finally, L_{OV} variation-aware semi-empirical small signal model for the L-TFET based analog circuit design is figured out. We explained a reason behind the sub-linear dependence of the I_D on L_{OV} for L-TFETs. This is because the impact of lateral electric field on the far end of the gate-source overlap region diminishes. The exponentially decaying potential profile in the

gate-source overlap region is obtained from the two dimensional Poisson's equation. Thereafter, a semi-empirical model for I_D-L_{OV} relation is established for the device under consideration. An increase in L_{OV} causes g_m to increase, whereas, r_o remains almost unaltered at the higher L_{OV}. The value of C_{gd} is almost independent of L_{OV}, while C_{gs} increases linearly. The performance of common source amplifier is predicted using our model and also validated with the numerical TCAD simulations. The voltage gain of the CS amplifier increases from 23 dB to 31 dB without any significant decrease in the bandwidth, when L_{OV} is increased from 20 nm to 50 nm. On the other hand, it is not feasible to achieve a gain of 31 dB while increasing the device width. Therefore, L_{OV} provides an additional degree of freedom to the circuit designers, when compared to the variation in the device width. Furthermore, a linear dependence of I_D on L_{OV} is obtained using the pillar based L-TFETs, whereby, the influence of lateral electric field is not significant on the tunneling junction.

7.2 Future Scope

In this section, we present the problems which we could not address during this tenure. Some of the left over interesting problems are as under:

- There is a strong need to develop a compact analytical model for the epitaxial layer based line TFETs to accurately capture the physics of the device.
- In most of our work, we have not considered the non-ideal effects, i.e. strain in the device, gate leakages, and interface traps. These parameters may affect the saturation voltages and the analog performance of the device. Thus, these aspects may be addressed in the future work.
- A bias-dependent small signal model for both line and point TFET is required to be developed, which should be aware of the variation in vital device design parameters viz. source/drain/epitaxial layer doping, channel/epitaxial layer thickness and channel lengths.
- The body bias and gate-source overlap significantly improves the drive capability of the device. The impact of V_{BS} and L_{OV} on the L-TFET based ultra-low power analog/digital circuits is yet to be explored.

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LIST OF PUBLICATIONS

Journal Publications

[1] **Abhishek Acharya**, Sudeb Dasgupta and Bulusu Anand, "A Novel V_{DSAT} Extraction Method for Tunnel FETs and its Implication to Analog Design", *IEEE Trans. on Electron Devices*, vol. 64, no. 2, pp. 629-633, Feb. 2017.

[2] **Abhishek Acharya**, Abhishek B. Solanki, Sudeb Dasgupta and Bulusu Anand, "Drain Current Saturation in Line Tunneling based TFETs: An Analog design Perspective", *IEEE Trans. on Electron Devices*, vol. 65, no. 1, pp. 322-330, Jan. 2018.

[3] **Abhishek Acharya**, Sudeb Dasgupta and Bulusu Anand, "Physical Modeling of Body Bias in Line TFETs and it implication to Analog Design Parameter", *IEEE Trans. on Electron Devices*, Mar. 2019. [Under Review: TED-2019-03-0530-R]

[4] **Abhishek Acharya**, Abhishek B. Solanki, S. Glass, Q. T. Zhao, and Bulusu Anand, "Impact of gate-source overlap on Device/Circuit Analog Performance of Line TFETs", *IEEE Trans. on Electron Devices*, Mar. 2019. [Under Review: TED-2019-03-0395-R]

Conference Publications

[5] **Abhishek Acharya**, Sudeb Dasgupta and Bulusu Anand, "Impact of Device Design Parameters on V_{DSAT} and Analog Performance of TFETs", in *proceeding of the Silicon Nanoelectronics Workshop, VLSI Symposium on Technology and Circuits*, 4-5 Jun. 2017, pp. 53-54, Kyoto, Japan.

[6] **Abhishek Acharya**, Sudeb Dasgupta and Bulusu Anand, "Understanding Drain Current Saturation and V_{DSAT} Extraction in Tunnel FETs: Analog Design Outlook", in *PhD Forum*, *International Conference on VLSI Design,* 6-10 Jan. 2018, Pune, India.

[7] **Abhishek Acharya** and Bulusu Anand, "Influence of Body-Bias and Gate-Source Overlap Length on the Analog Performance of Epitaxial Layer Enabled Area Scaled Tunneling FETs", in *PhD Forum*, *International Conference on VLSI Design,* 5-9 Jan. 2019, New Delhi, India.