PERFORMANCE INVESTIGATIONS OF LOW VOLTAGE HIGH CURRENT POWER SUPPLY

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RAKESH MAURYA

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE – 247667 (INDIA)
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ROORKEE

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in this thesis entitled **"PERFORMANCE INVESTIGATIONS OF LOW VOLTAGE HIGH CURRENT POWER SUPPLY"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electrical Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from July, 2010 to December, 2013 under the supervision of Dr. S. P. Srivastava, Professor and Dr. Pramod Agarwal, Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(**RAKESH MAURYA**)

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(Pramod Agarwal)
Supervisor

(S. P. Srivastava)
Supervisor

Date: _____

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ABSTRACT

As bulk of electrical power is extensively utilized in the form of A.C., but contemporary, DC power has also gained significant importance due to wide applications of electronic devices. Some of the industrial processes where controlled DC is required are electroplating, electrolysis, anodizing, and metal refining, electronic welding, plasma torch applications, battery charging, electrical traction, telecommunication and computer industry. There are several applications which require high power at reduced DC voltage power because high voltage cannot be applied due to the system requirements. These applications include telecommunication, computer server system, electrochemical processes, DC arc furnaces, Large Hadran Collider (LHC), and nuclear fusion research of magnetic confinement etc. The power supply installed in aforesaid applications is named as Low Voltage High Current (LVHC) power supply.

In light of the variety of the aforementioned applications, several power converters are reported in literature which could be employed for low, medium and high power applications. Keeping in view of high power applications at low output voltage, the use of transformer is essential for voltage scaling, electrical isolation and safety. Based on electrical isolation, the existing topologies are broadly classified in two groups namely line frequency transformer based converter and high frequency transformer based converter. These groups of power converters are normally compared from the viewpoint of size and weight, location of transformer and DC-DC converter in order to search for suitable power circuit for providing high current at low output voltage.

The majority of high-power rectifier manufacturers around the world inevitably use line frequency transformer based power converter due to low cost and well-established technique. Invariably, these converters consist of a power conditioning system which comprises of phase shift transformers and multiple AC-DC converters that transfers power to load in single-stage conversion. The phase shifting transformer is essential to provide desired phase shift in input voltages of converters and is achieved by different connections of three-phase and single phase transformers. Additionally, phase shifting transformer provides electrical isolation and reduction in voltage to achieve high current at low voltage. Although such multipulse converters help in achieving reduction in DC voltage ripples and harmonics in input current simultaneously, but they are quite bulky and more weight due to line frequency operation. Further, the efficiency of such system is low to deliver same power at reduced voltage.

To comply harmonics regulation set by IEEE Standard 519-1992, the line frequency transformer based converter requires additional filters at the input which further increases size , weight and cost.

In light of the above limitations, the high frequency transformer based power converters are selected in which power conditioning system consists of two stages namely AC –DC and DC-DC power conversion. The most common practice for AC-DC conversion is to use 1-phase/3-phase diode bridge rectifier followed by a large capacitor to obtain ripple free DC voltage. As a result, the line current becomes non-sinusoidal and has several undesired effects on both the utility and consumer sides such as losses and overheating in transformer, shunt capacitors, power cables, reduced power factor and distortion of the line voltage due to the line impedance drop. Hence, PFC pre-regulator are used to ensure power quality issues at utility sides. The output DC voltage obtained by PFC pre-regulator from $1-\phi$, 230 V, 50Hz / $3-\phi$, 415 V, 50 Hz AC power supply varies from 400-1000V DC.

In order to meet demand of large current at low output voltage, the survey of power converter topologies for the second stage of power conversion (DC-DC) is extremely important. Keeping in view the requirement of low output voltage from high input DC voltage, high conduction losses, and controller design, the performance of the following DC-DC converters are evaluated.

- Isolated DC-DC Converter
- Inter-Connected Converter
- Three-phase DC-DC Converter

Isolated DC-DC converters in its basic forms i.e. forward, fly-back, push-pull, half and full bridge for the second stage of implementation face the problem of high voltage stress on the switching devices of front end converter and it has become a major concern in designing converter. Conventionally, in order to reduce voltage/current stress, each power devices are replaced by two or more series/parallel connected switches respectively. In practice, the devices are not identical but have forward dropping characteristics within a narrow band. In addition, the parasitic elements significantly influence the unequal voltage and current sharing by the switching devices. Alternatively, the modular approach for designing LVHC DC-DC converter be adopted in which low rating DC-DC converter modules are integrated in series or parallel, both at input side as well as output side to achieve desired input and output specifications. Among four possible inter-connections namely input-parallel-output-parallel (IPOP), input-parallel–output-series (IPOS), input-series–output-parallel (ISOP), and input-series–output-series (ISOS), the ISOP connection is preferred for low voltage high current applications due to better voltage stress at front end converter and current stresses at load end converter, increase power processing capability, improved reliability because of more even distribution of stresses, ease of expansion and repair.

Keeping this in mind, the performance of two identical modules of push-pull converters is investigated. The effect of parasitic elements such as effective series resistance of

capacitors and output inductors, leakage and magnetizing reactances of transformers and with inter-connected in series at input side and in parallel at output side are included. The converter modules of same rating cannot be identical i.e. any mismatch in circuit parameters leads to unequal sharing of power by individual converter modules i.e. the module which supplies more power suffers more stress and the probability of its failure increases. In order to share equal power by two push-pull converters, three controllers namely common output voltage controller, inner current controller and input voltage controller are employed. A stable feedback system is designed to regulate the output voltage. A systematic development of a small-signal linear dynamic model of proposed converter is carried out using State-Space Averaging (SSA) technique. The transfer functions of different control blocks of converter are obtained. Furthermore, stability analysis of control loops is carried out to ensure closed loop operation. The Simulink model of proposed converter is developed using MATLAB/ SimPowerSystem^{TM} and the simulation results are presented. For high power applications, a large number of small rating modules are connected in ISOP connection and to ensure equal power sharing, several controllers are to be employed. Therefore, on account of more number of components, controllers, system reliability decreases and furthermore design of controllers becomes complex.

A three-phase DC-DC converter is proposed as an alternative for high power applications. It has several advantages over the single-phase DC-DC converter such as ease of power device (MOSFETs) selection due to reduced current rating, reduction of size and weight of passive components due to increased effective switching frequency by a factor of 3 compared to single-phase DC-DC converter and reduction in transformer size due to better transformer core utilization.

This work presents mathematical modelling, analysis, design, simulation and experimental results of three-phase, high frequency isolation transformer based DC-DC converters suitable for low voltage and high current applications. A high-frequency isolated three-phase LLC resonant DC-DC converter with centre-tapped secondary windings of trasnformer is proposed which consists of three units of single-phase half bridge LLC DC-DC converter and operated in interleaved manner to feed high power load. The proposed topology with interleaved control technique increases the effective frequency of operation without increase in switching frequency of switches and hence reduces the size and weight of passive components. However, operation with higher frequency leads to increase in switching losses and EMI problems. The performance of proposed topology is further improved by implementation of Zero Voltage Switching (ZVS) making use of snubber capacitance, leakage and magnetizing inductances of transformer (LLC resonant tank) and hence reduced switching losses in front end converter, and better current sharing at load end converter can be achieved. The mathematical modeling of LLC resonant tank network is

developed and its design curves are plotted against variation of normalized frequency for different values of load. Based on the design curves, the Simulink model of converter is developed using MATLAB/SimPowerSystems™ and simulation study is carried out to investigate its performances for low voltage high current applications. To validate simulation results, a prototype model of 75W, 1.5V/50A is built and its performance is investigated under various operating conditions.

For high-current applications, the rectifier configuration of current-doubler converter is preferred over the centre-tapped converter for a number of reasons. First, in the current-doubler converter the inductor currents and the transformer secondary current are lower than the corresponding currents in the centre-tapped converter. As a result, the current-doubler converter exhibits lower conduction losses than the centre-tapped converter. Second, the current-doubler converter minimizes the number of high-current interconnections that further simplify the secondary layout and reduces the layout-related loss. On the basis of secondary side load sharing, transformer design and thermal heat dissipation, the three-phase high frequency isolated DC-DC converter with three-phase rectification is proposed. It consists of three main parts: front end converter, high frequency transformer and load end converter. The front end converter comprises of *N* legs and each leg consists of two power switches. The midpoints of each leg are connected to one end of the primary winding of single-phase high frequency transformers and other ends of the primary winding of transformers are connected at one point. The load end converter of three-phase rectification is similar to three-phase full diode bridge in which upper diodes are replaced by inductors. The performance of proposed converter is investigated under symmetrical and asymmetrical phase shifted PWM control methods with fixed frequency operation. The steady state operation of the converter is discussed in detailed using operating waveforms and its equivalent circuits during different modes. A Simulink model of proposed converter is developed using MATLAB/ SimPowerSystems™ and its simulation results are presented under various operating conditions. To validate the simulation results of proposed topology, a scaled prototype model is developed and experimentally tested under different operating conditions. The comparative evaluation of proposed converter under symmetrical and asymmetrical control method is carried out with respect to various parameters such as duty cycle control, voltage gain, transformer secondary winding current, voltage and current of rectifier diodes, thermal stress and ZVS and ZCS implementation. It is concluded that under symmetrical control method, all the power switches conduct uniformly unlike to asymmetrical control and hence uniform heat distribution is achieved with symmetrical control. Implementation of asymmetrical control technique requires dead band circuits as compared to symmetrical control. Furthermore, reduction in secondary side losses can be done by employing self driven synchronous rectifier replacing rectifier power diodes.

Many industrial applications such as welding, plasma cutting, and surface hardening require large DC current at low voltage. In such applications, the rating of power supply varies from several kilowatts to hundreds of kilowatts. The power supply employs in such applications particularly in arc welding process is expected to operate from open-circuit (no-load) to short-circuit (when the electrode sticks to the workpiece for a short span of time) quickly and also the transients occur during the striking of the arc, rapid arc length changes and metal transfer across the arc. The power supply must respond to these changes rapidly. In the present work, a multi-phase high frequency isolated DC-DC converter is proposed which is well suited for aforementioned applications. The proposed converter comprises of front end converter, two units of three-phase high frequency transformers and multi-phase rectifier stage at load end converter. In proposed topology, one three-phase transformer is configured in *Yd*1 and other transformer is configured in*Yd*11 to provide phase shift for interleaved operation. The performance of proposed converter has been investigated under symmetrical and asymmetrical phase shifted PWM control methods with fixed frequency operation. In comparison with conventional welding machine employed in many industries, the size and weight, efficiency and dynamic response of proposed converter is improved significantly. The simulation and experimental results are obtained under different operating conditions and presented.

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(Rakesh Maurya)

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A,B,C	Averaged state space matrices
A_i,B_i,C_i,E_i,F_i	State space matrices in i^{th} mode; $i = 1,2,3,....8$
Ac	Core cross-sectional area
Aw	Winding wire area
$a_{w1,}a_{w2}$	Area of wire
B_m	Maximum value of flux density
C_1,C_2 ....C_N	Input capacitors
C_o	Output capacitor
C_s	Resonant capacitor
D	Duty cycle
$\tilde{d}$	Perturbation in duty cycle
d_i	Duration of i^{th} mode of ISOP connected converter
D_1,D_2,D_3,D_4,D_5,D_6	Rectifier diodes of multi-phase DC-DC converter
$D_{11},D_{12},D_{22},D_{21},D_{31},D_{32}$	Rectifier diodes of centre-tapped converter based rectification stage
ΔI_L	Inductor current ripple
f_{sw}	Switching frequency
i	Mode of operation
i_A,i_B,i_C,i_D,i_E,i_F	Line current at primary side of transformer
i_a,i_b,i_c,i_d,i_e,i_f	Line current at load end converter
$i_{D1},i_{D2},i_{D3},i_{D4},i_{D5},i_{D6}$	Current through rectifier diodes
$i_{D11},i_{D12},i_{D21},i_{D31},i_{D32}$	Current through rectifier diodes in centre-tapped converter
i_L, $i_{L1},i_{L2},i_{L3},i_{L4},i_{L5},i_{L6}$	Current through output filter inductors
I_{L1max},I_{L1min}	Max and min value of current of each inductor
i_m,i_{m1},i_{m2}	Magnetizing current of transformer
I_o	Load current
i_{in1},i_{in2}	Input current at each DC-DC module
i_{ph}, i_{ph1}	Phase current and fundamental component of phase current
$i_{sa},i_{sb},i_{sc},i_{sd},i_{se},i_{sf}$	Secondary side winding current of transformer
J	Current density
K	Waveform coefficient
K_i	Integral constant
K_p	Proportional constant

L_1,L_2,L_3,L_4,L_5,L_6	Output filter inductor
L_{lk1},L_{lk2}	Leakage inductance of transformer
L_m,L_{m1},L_{m2}	Magnetizing inductance
L_p,L_s	Equivalent reactance measured at primary side with Secondary side open and shorted respectively
m_1,m_2,m_3,m_4	Slope of current at different time interval
$M_{12},M_{13},M_{21},M_{22},M_{31},M_{32}$	Mutual inductance between output filter inductor
N	No of modules
N_1,N_2,n_1,n_2	Number of turns in primary and secondary windings of transformer
n	Turns ratio, $n=\frac{n_1}{n_2}=\frac{N_1}{N_2}$
p	Differential operator
P_t	Apparent power
Q	Quality factor
R	Load resistance
r_C	Equivalent series resistance output capacitor
$r_{C1},r_{C2,.....}r_{CN}$	Equivalent series resistance input dividing capacitor
$r_{L1},r_{L2},r_{L3,.....}r_{LN}$	Equivalent series resistance output filter inductor
$s=j\omega$	Laplace operator
$S_1,S_2,S_3,S_4,S_5,S_6,.....S_N$	Power switches of multi-phase topology
$S_{11},S_{12},S_{21},S_{22}$	Power switches of push-pull converter
T	Time period
T_0	Instantaneous time
$t_0,t_1,t_2,t_3,t_4,t_5,t_6,t_7,t_8$	Instantaneous time
T_a,T_b,T_c,T_d,T_e,T_f	Transformer
T_{r1},T_{r2},T_{r3}	Saw-tooth waveform
$\bar{T}_{r1},\bar{T}_{r2}\&\bar{T}_{r3}$	Phase-shift saw-tooth waveform
u	Input matrix
v_1,v_2	e.m.f. induced in two winding of transformer
v_A,v_B,v_C,v_D,v_E,v_F	Potential at mid points (A,B,C,D,E & F) of legs of front end converter
v_a,v_b,v_c,v_d,v_e,v_f	Potential at mid points (a, b, c, d, e & f) of legs of load end converter
$v_{A1A2},v_{B1B2},v_{C1C2},v_{D1D2},v_{E1E2},v_{F1F2}$	Voltage across high voltage windings of transformer
$v_{a1a2},v_{b1b2},v_{c1c2},v_{d1d2},v_{e1e2},v_{f1f2}$	Voltage across low voltage windings of transformer

v_{AB}, v_{BC}, v_{CA}	Output line voltage of front end converter
$v_{ph,}\ v_{An},\ v_{Bn},\ v_{Cn},\ v_{Dn},\ v_{En},\ v_{Fn}$	Output phase voltage of front end converter
v_{C1}, v_{C2}…….v_{CN}	Voltage across output capacitor
$v_{Control}$	Control voltage
$v_{DS1}, v_{DS2}, v_{DS3}, v_{DS4}, v_{DS5}, v_{DS6}$	Drain to source voltage across switches (S_1-S_6) of front end converter
$v_{GS1}, v_{GS2}, v_{GS3}, v_{GS4}, v_{GS5}, v_{GS6}$	Gate to source voltage across switches (S_1-S_6) of front end converter
V_{in}	Input DC voltage
$\tilde{v}_{in}$	AC ripple in input DC voltage
v_{in1}, v_{in2}	Input voltage of individual DC-DC converter module
$v_L, v_{L1}, v_{L2}, v_{L3}, v_{L4}, v_{L5}, v_{L6}$	Voltage across output filter inductor
V_o	Output voltage of converter
v_{o1}, v_{o2}	Output voltage of individual DC-DC converter module
$v_{p11}, v_{p12}, v_{p21}, v_{p22}$	Voltage of primary windings of transformer
v_{s1}, v_{s2}, v_{s3}	Voltage of secondary windings of transformer
$v_{s11}, v_{s12}, v_{s21}, v_{s22}$	Voltage across switches of ISOP connected push-pull converter
$v_{sw}, v_{sw1}, v_{sw2}, v_{sw3}, v_{sw4}, v_{sw5}, v_{sw6}, v_{sw7}, v_{sw8}$	Voltage across switches
x	State variable of converter
$\tilde{x}, \tilde{y}$	Perturbation in state variable x, y
y	Output matrix
Z_{in}	Input impedance of per phase converter model

[This chapter describes some of the applications which require high power at reduced DC voltage. The literature on converter topologies, control techniques suitable for low voltage high current applications is reviewed. Based on study, inter-connected modular DC-DC converter and multi-phase DC-DC converters are proposed. Finally scope of work, author's contribution and thesis outlines are presented.]

1.1 Introduction

The field of power supply is concerned with the processing of electrical power as desired by applications. As bulk of electrical power is extensively utilized in the form of A.C., but contemporary, DC power has also gained significant importance in recent times. Some of the industrial processes where controlled DC is required includes electroplating, electrolysis, anodizing, metal refining, electronic welding, plasma torch applications, battery charging, electrical traction, telecommunication and computer industry [1-3]. There are several applications which require high power at reduced DC voltage as due to constraint of system requirements high voltage cannot be applied. These applications include telecommunication, computer server system, electrochemical processes, DC arc furnaces, Large Hadran Collider (LHC), and nuclear fusion research of magnetic confinement etc. The power supply installed in aforesaid applications is named as Low Voltage High Current (LVHC) power supply.

A schematic diagram of Low Voltage High Current power supply is shown in Fig.1.1. It consists of phase shifting transformer having low turns ratio (N_s/N_p) and multiple AC-DC converters connected in parallel to provide very high current at low voltage as desired by load. The phase shifting transformer is essential to provide desired phase shift in input voltages of AC-DC converters by different connections of three-phase transformer. These connections include Delta/Delta-Wye, Delta/ Wye-Delta, Delta/ Zigzag, Delta/polygon and Zigzag/ Wye [4-6]. Additionally, the phase shifting transformer provides electrical isolation and reduction in voltage to achieve high current at reduce voltage. These configurations help in achieving reduction in DC voltage ripple and harmonics in input current simultaneously, but they have several drawbacks:

- The transformer's size and weight varies inversely with frequency, thus line frequency transformers, which operate at 50Hz, are large in size and weight.
- Locations of the transformers at the primary stage of power conversion system, cause lower efficiency because to deliver same power at reduced voltage, the subsequent circuits would draw large currents.
- The semiconductor switches connected in parallel do not share equal load current.
- The requirement of inter phase transformers (IPTs) increases the size, weight and cost and reduces the efficiency.

To comply harmonics regulation set by IEEE Standard 519-1992, line frequency transformer based converter requires additional filters at the input which further increases size , weight and cost.

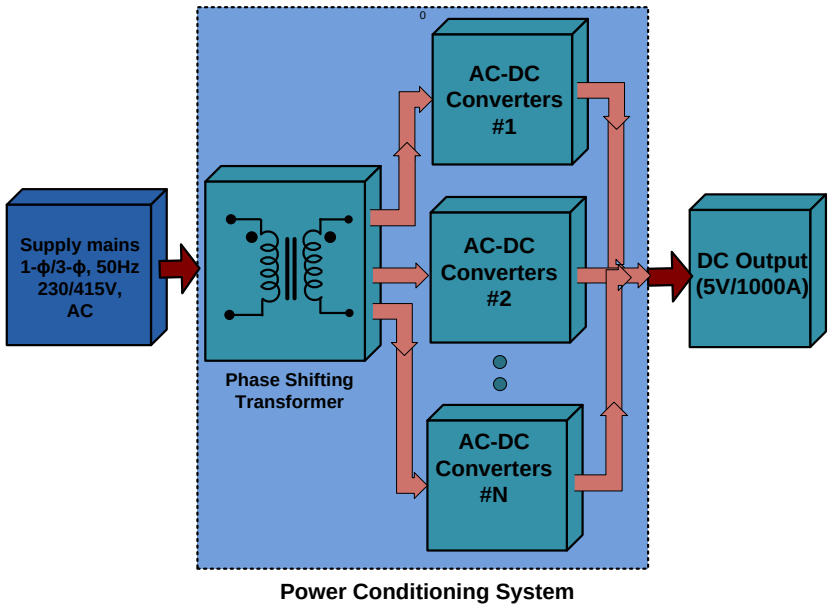


Fig.1.1 Schematic diagram of low voltage high current power supply.

In the past few years, the need of efficient and light weight low-voltage high-current regulated DC power supplies for low, medium and high power loads, has stimulated considerable interest in the power supply industry. Looking to the drawbacks of conventional LVHC power supply, designer has to pay special attention towards design of ripple free DC output voltage, efficient secondary side circuit, harmonic contamination in line currents, devices rating and their interconnections and switching frequency.

1.2 Applications of Low Voltage High Current Power Supply

The choice of rectification technology is governed by the application requirements. Fig.1.2 shows the classification of LVHC applications based on voltage and power demand by the applications. Therefore, the applications of LVHC power supply and their characteristics need to be reviewed to select a power supply for an application.

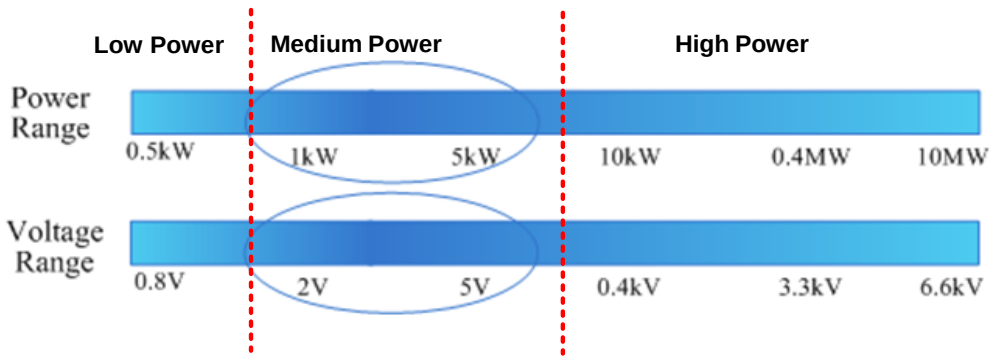


Fig.1.2 Voltage and power rating of LVHC applications

1.2.1 Low Power Applications

The LVHC power supply is widely used in low power applications such as data processing and telecommunications equipment. Due to drastic increase in use of Internet, advancements in telecommunication, high-speed data computing and communication systems such as, phone exchange, internet server, router, desktop, laptop and all other types of telecommunication systems require high performance power DC supply.

Initially, The Centralized Power Architecture (silver box) provides 5V-12V and feeds power to memory chip, video card and other parts as well as to microprocessor load through VRMs (point-of-load (POL) converter). To meet the pace of fast developing microprocessor, The Centralized Power Architecture (CPA) based power supply is no longer practical and hence Distributed Power Architecture (DPA) had been adopted as shown in Fig.1.3. The DPA has a common intermediate DC bus voltage, nominal at 12 V, which supports the entire system. Because each communication board requires a specific voltage lower than the bus voltage, a point-of-load (POL) converter is used. The POL converter converts the intermediate bus voltage to the required microprocessor core voltage ranging from 0.8 to 3.3V and also provides isolation with the bus voltage.

The vast majority of today's servers supplied from single phase ac lines employ the LV DC-bus architecture as shown in Fig.1.3 .

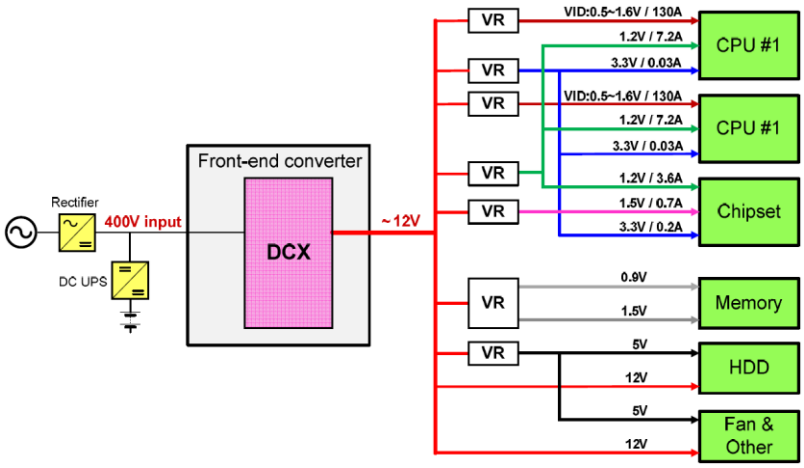


Fig.1.3 Power architecture in computer server system [7]

1.2.2 Medium Power Applications

Medium power applications of LVHC power supply includes battery charging and starting process of aircraft/vehicles. Several charging methods are practiced for rechargeable batteries such as Constant Voltage (CV) charging, Constant Current (CC) charging, Taper Current Charging, Trickle current charging, automatic charging, high-rate or Boost charging and diagnostic charging. In CC charging, battery is charged at a preset rate of constant current. In taper current charging method as the voltage increases, the current decreases or tapers off to a minimum. Boost chargers provide high charging current (40 to 250 A) for quick

recharging or boosting a battery or assist in starting a vehicle. Trickle chargers are basically manual small current chargers used to maintain a battery at its full state of charge over a long period of time. Diagnostic chargers additionally include circuitry to detect a good or a bad battery. Essentially, all charging methods need a CC power supply to pump required current into a discharged battery.

The battery charging sets developed by Anode Converter Works with different specifications as follows:

- Automatic –control rectifying sets consisting of semiconductor diodes and controlled by means of magnetic amplifiers. They are rated at 125A-500A at 72V and 125A at 48,110 and 220V, respectively. They serve primarily as supply sources for postal exchanges, but are also used for charging of power house and transformer-station standby batteries and similar installation for floating operation and trickling charging.
- Rectifier set with 400A or 200A current rating at 110 or 65V are developed for battery charging.
- Silicon-diode battery- charging set with semi-automatc control serves for the charging of lower–capacity batteries of 20-30 ampre-hours. These rectifiers are rated for 100, 50 and 30 A at rated voltages of 6, 12 and 40V respectively. These power supplies are developed for taper current charging.
- A multipurpose power supply unit, including battery charging at 6, 12 and 24 V and maximum current of 150A, motor vehicle starting at 12 and 24V and 1200A current, welding at 12 and 24V with 40-300A current rating and galvanizing at 12 or 24V with current rating 200A.

All aforementioned rectifier sets consist of line frequency isolated transformer, diodes/ thyristors and magnetic amplifier. The major disadvantages of these systems are large size and weight, less efficiency and poor thermal heat management.

1.2.3 High Power Applications

Electrochemical plants, in particular those producing aluminium, zinc, chlorine, and hydrogen, are the biggest consumers of electrical power. These electrochemical processes need direct current of 3-300kA at 50-1000V, depending on the electrolysis equipment employed. High power rectifier equipment supplying industrial electrolysis's incorporates silicon diodes almost exclusively now a days. The voltage and current ranges are fairly broad, depending on the specific applications. For instance, equipment delivering 60-140kA at 400-1000V has been built for aluminium smelters, whereas diaphragm-cell chlorine electrolysis require 25-40kA at 400-700V and mercury cell chlorine electrolyses use equipment delivering 150-300kA at 75-400V.

Power involved, indicated by the aforementioned figures render the efficiency of the rectifying equipment, is a prime consideration. Electrochemical processes operate continuously at constant rates of power consumption and hence, in countries like India where electrical energy is not readily available and price of kilowatt-hour is high, a little / slight improvement in design, control and operations will cause great saving of electrical power. Typical ratings for the dc current and voltage for high power applications are given in Table 1.1.

Table 1.1 High Power Application Processes

Sr. No.	Rectification Application	Current (Amps)	Voltage (DC)
1.	Chemical electrolysis	5,000-150,000A	40-1,000V
2.	Aluminium Potline	10,000-300,000	<1,300 V
3.	DC Arc Furnace	50,000-130,000A	600-1,150V
4.	Graphitizing Furnaces	20,000-120,000A	50-250V
5.	Copper Refining	10,000-15,000A	40-350V
6.	Traction substation	1,000-5,000 A	500-1,500 V
7.	Battery chargers	25 to 2000A	50-1000V

In addition to above applications, some specific applications such as DC compound pump in nuclear reactor, Large Hadron Collider (LHC) and DC fused quartz furnace etc also require high power at reduced DC voltage. For example DC compound pumps require low voltage high current power source for its operation. The power source should be able to provide low voltage of 2 volts and a minimum current upto 3000A. The power supply is required to operate from three-phase 415V with $\pm 10\%$ variations, 50 Hz supply. The ripple should be less than $\pm 1\%$ and it should be designed for continuous duty with natural cooling. Indira Gandhi Centre for Atomic Research (IGCAR), Kalpakkam (T.N.) India is currently having one power supply for supplying the DC Compound pump. Present power supply source uses autotransformers and diodes which makes it of higher size and more weight. The physical diemension of this power supply system is $2215(H)\times 1730(W)\times 1030(D)mm^3$ and its weight is $1325 Kgs$.

The Large Hadron Collider (LHC) is the world's largest and most powerful particle accelerator consisting of a 27-kilometre ring of superconducting magnets in which two high-energy particle beams travel at close to the speed of light before they are made to collide. The beams travel in vacuum and opposite directions in separate beam pipes and guided around the accelerator ring by a strong magnetic field maintained by superconducting electromagnets. For this purpose, a total 176 power converters of 8V/6kA and 24 power converter of 8V/8kA rating are required for supplying power to superconducting magnets.

These converters are made using modular concept where three to four high-current converter [2kA, 8V]) are connected in parallel and they are expected to exhibit a very high level of performance in all operating conditions.

Fused quartz furnace is an industrial furnace used to purify quartz by heating. A $30V / 2000A$ DC power supply unit includes three-phase AC voltage regulator circuit, rectifier transformer, and rectifier circuit of double reverse-star with inter-group reactor. Although double reverse-star rectifier circuit with inter-group reactor make the power supply bulky and slow, but it has several advantages:

- The output voltage waveform of the double reverse-star rectifier circuit is the same as the waveform of the six-phase half-wave rectifier circuit, and the pulsation of the output voltage is smaller than the three-phase half-wave circuit.
- The magnetic circuit of transformer is balanced, so there is no DC magnetization problem.
- Compared with the six-phase half-wave rectifier circuit, the utilization of the transformer secondary winding is doubled and therefore the capacity of the transformer is smaller than the six-phase half-wave rectifier circuit.
- Since each rectifier contributes 50% of the load current, the ability to withstand the load is improved.

Due to high load current, the conduction losses in rectifier are more and hence this circuit requires high current rating diodes and windings conductor on secondary side.

1.3 Literature Review

Prior to the advent of power semiconductor devices such as diode, thyristor, gate turned off thyristor (GTO), power MOSFETS, Insulated Gate bipolar transistor and Integrated Gate Commutated Thyristor (IGCT), the LVHC DC power supply was accomplished using a motor-generator set in which induction motor or synchronous motor is mechanically coupled with DC generator. The major problems associated with motor-generator set was low efficiency, high cost, large size & weight and frequent requirement of maintenance. New era of DC supply was started with the development of high current power diodes and thyristor in 1960 and 1970 respectively. Conventionally, three-phase full bridge rectifiers fed from three-phase transformer with on tap load changer (OTLC) had been used for high power applications as shown in Fig.1.4. To meet increasing demand of high power, each power switch of Fig.1.4 is replaced by the parallel combination of power devices [8,9]. Theoretically, the current divides equally among identical symmetrically placed devices, but in practice, the devices are not identical and have their forward dropping characteristics within a narrow band. In addition, the parasitic elements significantly influence the sharing of current in

individual diodes connected in parallel. Therefore, such system have high conduction losses, high working temperature and are inefficient and of large size and weight.

In most of the applications, the front end converter is used with either diode bridge rectifier or phase controlled rectifier, which draws significant harmonics and reactive power from AC mains and hence unable to comply power quality requirements recommended by IEEE 519-1992 [10].

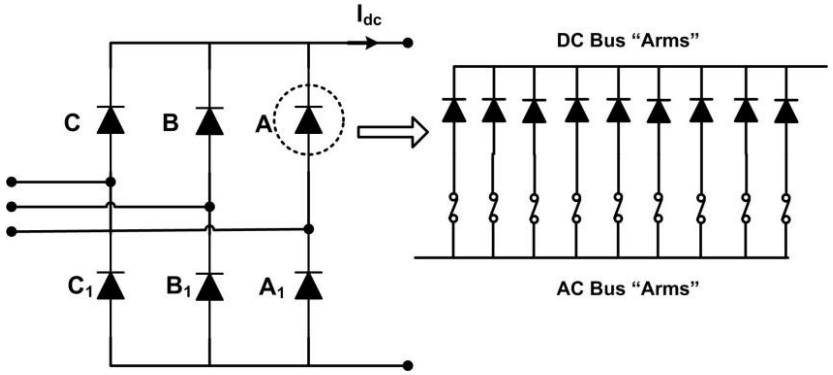


Fig.1.4 Conventional high power rectifier

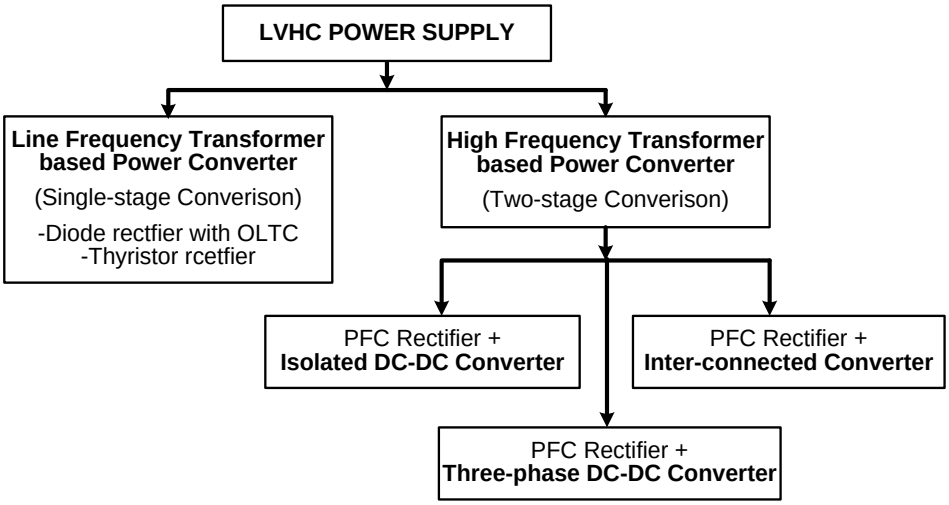


Fig.1.5 Generalized classification of LVHC power supply

Keeping in view of high power applications at low voltage output, the use of transformer is essential for voltage scaling, electrical isolation and safety. Based on electrical isolation, the topologies reported in literature are broadly classified in two groups namely line frequency transformer based converter and high frequency transformer based converter as illustrated in Fig.1.5. The major high-power rectifier manufacturers around the world inevitably use line frequency transformer based power converter because of low cost and well-established techniques [3,11-15]. Invariably, these converters consist of power conditioning system which comprise of phase shift transformers and multiple AC-DC converters, feeding power to load in single-stage conversion as shown in Fig.1.6(a). The phase shifting transformers are required to provide desired phase-shift in converter input

voltage by different three-phase connections of transformers. Additionally, phase shifting transformer provides electrical isolation and reduction in voltage to achieve high current at low voltage. Although these group of converters help in achieving reduction of DC voltage ripple and harmonics in input current simultaneously, but they have several drawbacks as discussed in section-1.1. Furthermore, to comply harmonics regulation set by IEEE Standard 519-1992, line frequency transformer based converter requires complex windings connections of phase shifting transformer and several inter-phase transformers which further increases size, weight and cost.

P. A. Dahono in [5] proposed a family of low voltage high current rectifier intended to use in cathodic protection system. These rectifiers reduce the conduction losses by providing minimum number of power devices in forward path of secondary side current and do not require complex input transformer [6]. It is observed that current in secondary windings of transformer contains a DC components and only one secondary winding carries current at particular time. The primary windings must be connected in delta connection to eliminate the DC components from the line current.

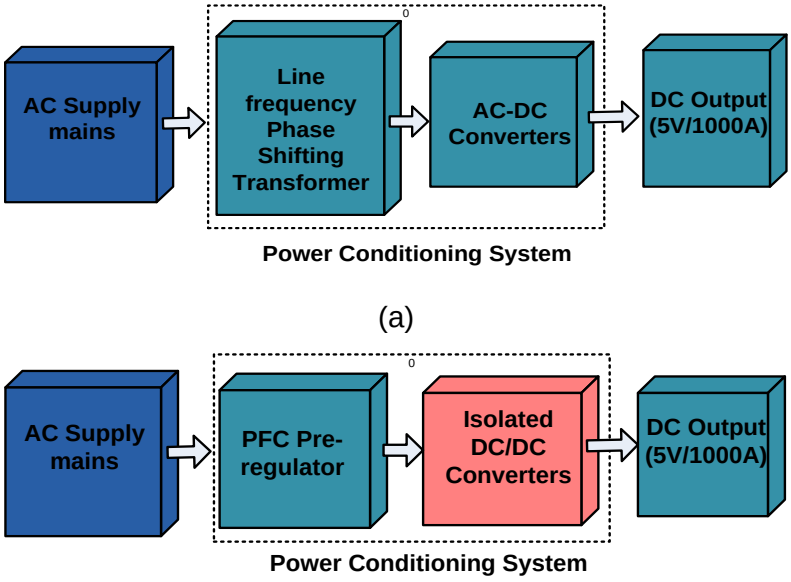


Fig.1.6 Block diagram of power converter (a) Line frequency isolation (b) High frequency isolation

In light of limitations of line frequency transformer based converter, the high frequency transformer based power converters are reviewed in which power conversion takes place mainly in two stages: AC–DC and DC-DC conversion [16-19]. The block diagram of high frequency based power converter is represented in Fig.1.6(b). Normally, for AC-DC conversion 1-ϕ / 3-ϕ diode bridge rectifier followed by large capacitor is used to obtain ripple free DC voltage. As a result, the line current becomes non-sinusoidal and adversely effects the utility and consumers. Therefore, enhanced AC-DC converter (PFC pre-regulator, PWM

rectifier etc.) are used to provide ripple-free DC voltage and meet the utility side power quality requirements in terms of harmonic contents and unity power factor operation [12, 20-25]. The output DC voltage obtained by PFC pre-regulator from 1-ϕ, 230 V, 50Hz / 3-ϕ, 415 V, 50 Hz ac power supply varies from 400-1000V. Therefore, power switches of second stage of conversion (DC-DC) experience high voltage stress.

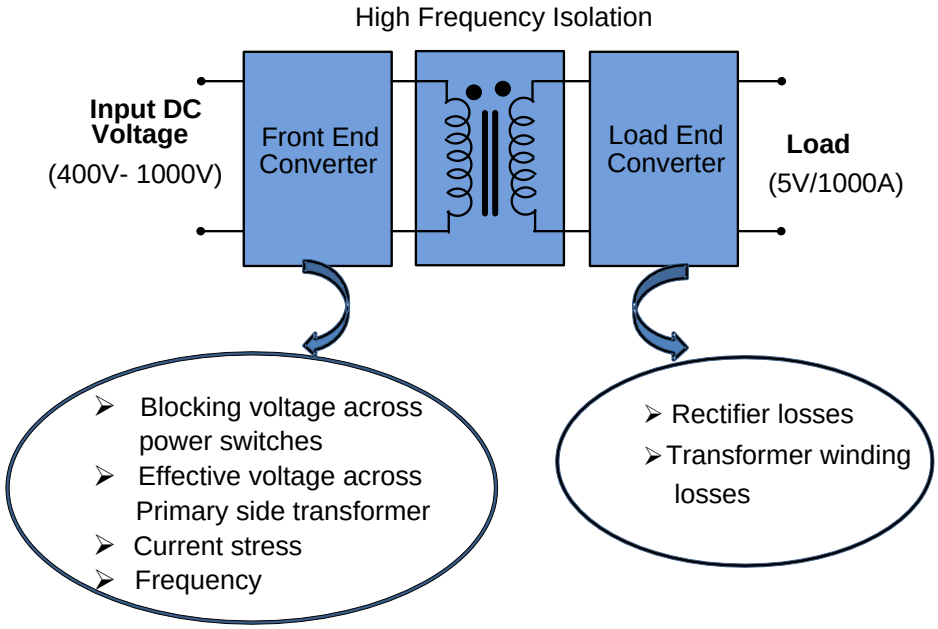


Fig.1.7 High frequency isolated DC-DC power converter

1.3.1 Topologies of DC-DC Power Converters

In order to meet demand of high current at low output voltage for an application, the survey of power converter topologies for second stage of power conversion (DC-DC) is important. Therefore, literature on isolated DC-DC converters are analyzed with respect to the desire features incorporated in different parts of converters as shown in Fig.1.7. The desired features for front end converter includes high blocking voltage and low current rating of switching devices, low effective voltage across primary side of transformer, high frequency operation, and ease of ZVS/ZCS switching implementations. On the other hand, desired features in load end converter include reduced rectifier losses, less high current nodes, and transformer winding losses. Keeping in view of large input voltage, low output voltage, high conduction losses and controller design, various types of DC-DC converters have been proposed in literature which are classified in following three groups as shown in Fig.1.5.

- Isolated DC-DC Converter
- Inter-Connected Converter
- Three-phase DC-DC Converter

The front end converter of single–phase isolated DC-DC converters namely: fly-back and forward are widely used in low power applications. The power switches of these topologies experience high voltage stresses when employed for medium and high power

applications [26-29]. The most commonly used topologies of front end converter in single-phase isolated DC-DC converters include push-pull, half-bridge, full-bridge, hybrid-bridge and full-bridge three-level configuration. These topologies are evaluated on the bases of blocking voltage, switch current and primary winding voltage as illustrated from Fig. 1.10 to Fig. 1.13 and comparative study with respect to desired parameters are tabulated in Table 1.2. Out of these topologies, half-bridge circuit configuration is most suitable because of reduced voltage stress, lesser switching devices, and lesser turn's ratio of transformer.

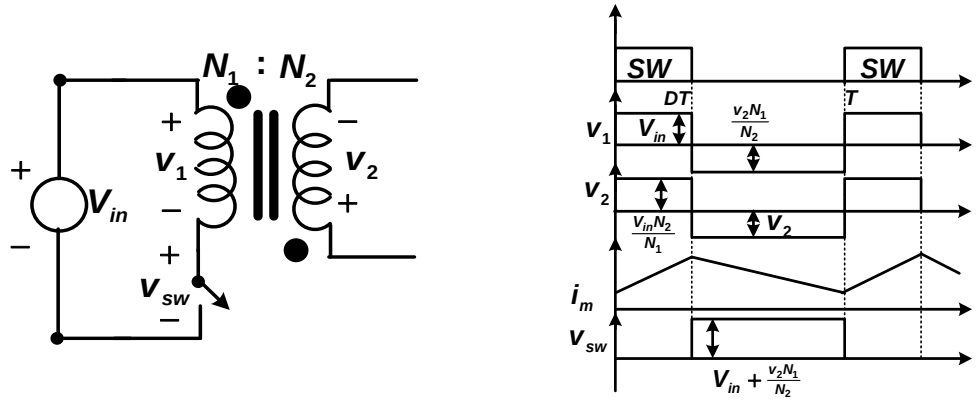


Fig. 1.8 Fly-back converter (a) Power circuit (b) Voltage & current waveforms

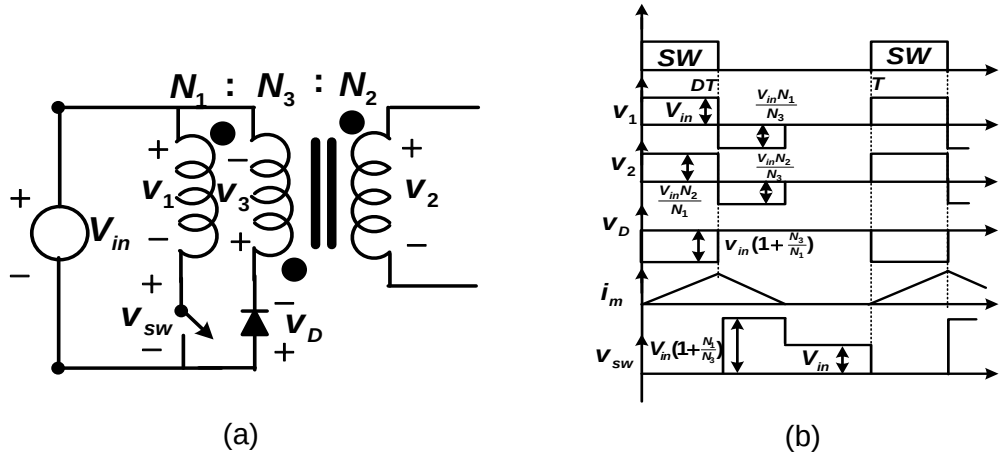
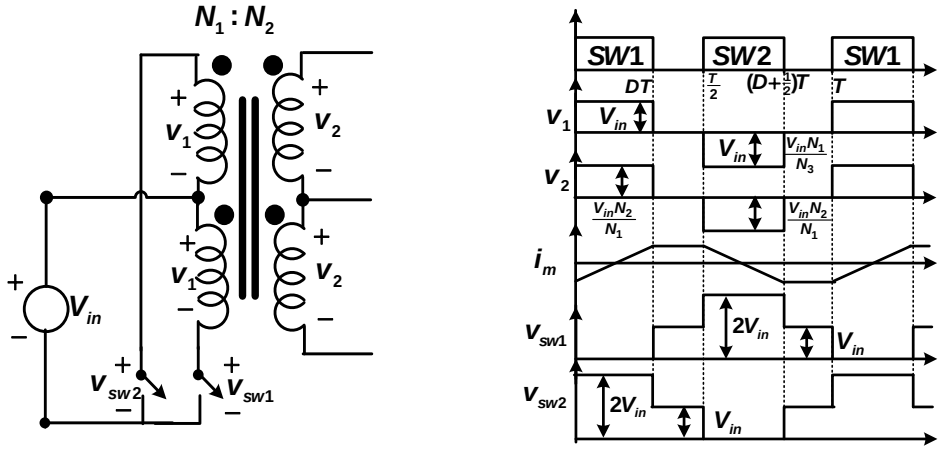
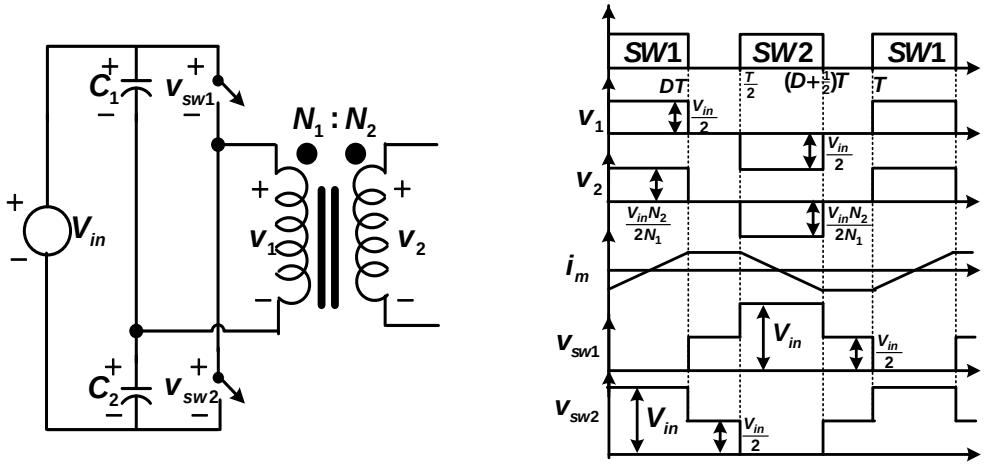


Fig. 1.9 Forward converter (a) Power circuit (b) Voltage & current waveforms



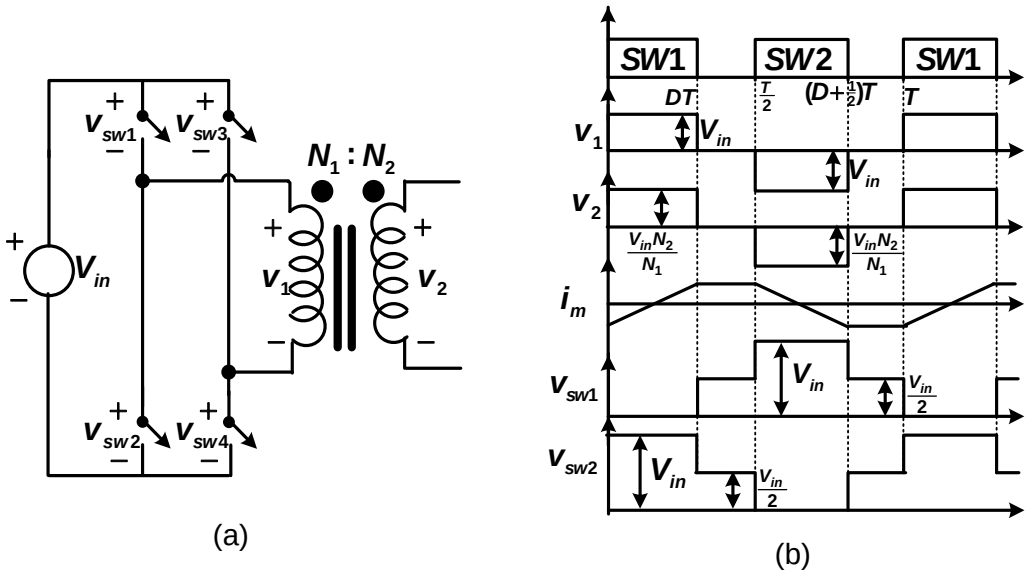
(a) (b)

Fig. 1.10 Push-Pull converter (a) Power circuit (b) Voltage & current waveforms



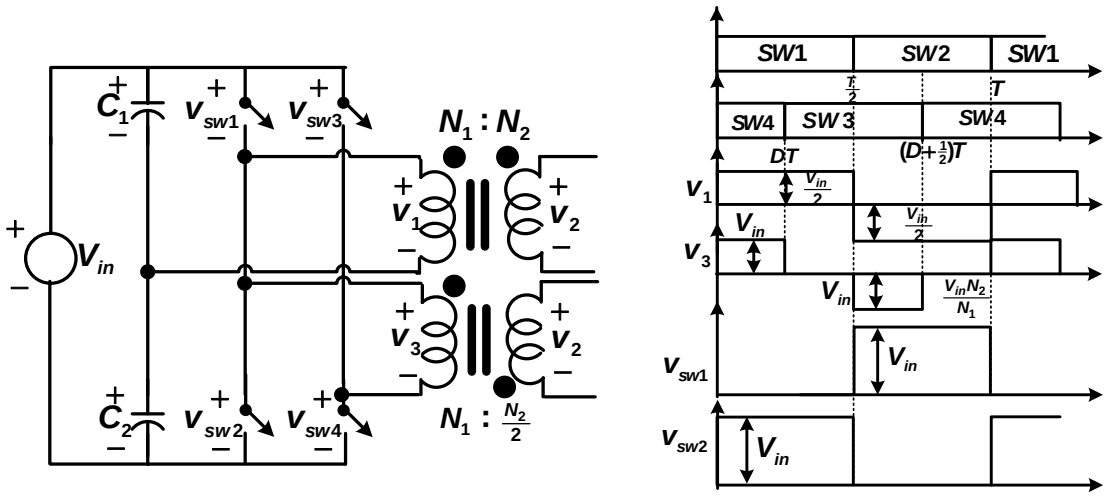
(a) (b)

Fig. 1.11 Half-Bridge converter (a) Power circuit (b) Voltage & current waveforms



(a) (b)

Fig. 1.12 Full-Bridge converter (a) Power circuit (b) Voltage & current waveforms



(a) (b)

Fig. 1.13 Hybrid converter (a) Power circuit (b) Voltage & current waveforms

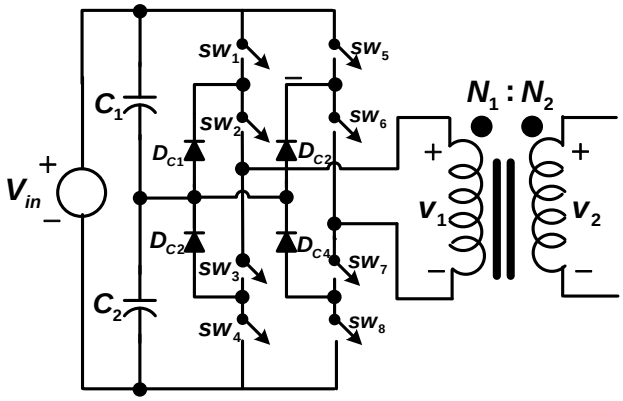


Fig. 1.14 Full bridge three-level converter

Table 1.2 Single-phase front end converter topology

Parameters	Front End Converter				
	Push Pull	Half-bridge	Full-bridge	Hybrid Bridge	Full bridge TL
Topology	Fig.1.10	Fig.1.11	Fig.1.12	Fig.1.13	Fig.1.14
Blocking Voltage (v_{SW1})	$2V_{in}$	V_{in}	V_{in}	V_{in}	$\frac{V_{in}}{2}$
Switch Current $i_1(t)$	I_1	$2I_1$	I_1	$3I_1$	-
Primary voltage (v_1)	V_{in}	$\frac{V_{in}}{2}$	V_{in}	V_{in}	-

Proper selection of load end converter ensures desired efficiency because this portion of converter carries high current and therefore, conduction losses in LVHC converters are dominant. In order to choose suitable topology for LVHC applications the following points need to be considered:

- Reduction of rectifier losses: the rectifier loss mainly depends on selection of topology, power devices and current in various parts of load end converter.
- Transformer windings losses: this loss can be reduced by selection of transformer winding geometry of low resistance, and suitable topology which requires low transformer winding currents particularly at low voltage secondary winding.

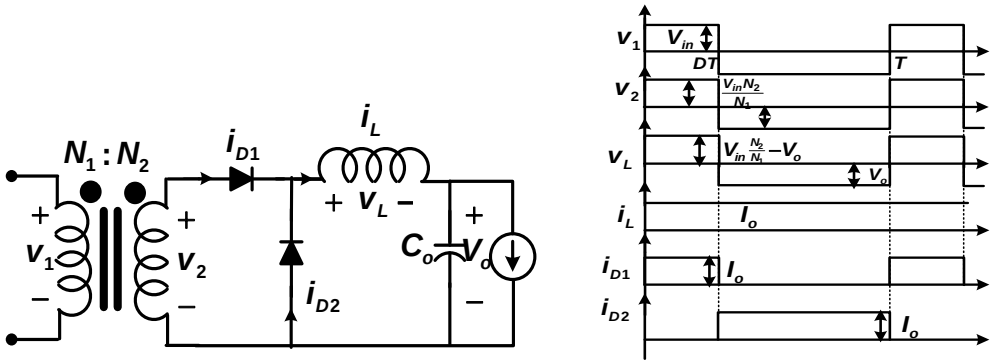
The topologies reported in literature [30-32] are analyzed in view of current in different parts of rectifer stage and its suitability for low voltage high current applications. The analysis of topologies shown in Fig.1.15 to Fig.1.18 is carried out and their comparative study has been made with respect to aforesaid points as tabulated in Table 1.3. The forward converter illustrated in Fig.1.15 has the simplest structure and requires a larger filter inductance and exhibits higher rectification losses than other rectifier circuits. Therefore, it is least suitable for LVHC applications. In the centre-tapped converter shown in Fig.1.16, the frequency of the output-filter-inductor voltage waveform is twice the switching frequency, while in the forward converter it is equal to the switching frequency as illustrated in Fig.1.16(b). As a result, the filter inductance in the centre-tapped converter is significantly smaller than that in the forward converter. On the other hand, the disadvantage is the large transformer winding current and winding losses and high current tapping in low voltage windings.

The Current Doubler converter requires one secondary winding that eliminates high current tapping unlike centre-tapped topology and hence avoids centre tapping shown in Fig.1.17(a). The current through the secondary winding is about half of the total average output current and thus reduced secondary winding current rating and losses. The major drawbacks are the pulsating current through the components in the primary side that increases the conduction losses, and also presents the possibility of current unbalance through the filter inductors when the inductances are different.

A novel Current-Tripler converter is proposed for high current applications [31]. Basically, an additional inductor is added in the current doubler rectifier to share one-third of the load current by each inductor as illustrated in Fig.1.18 . As a result, it has better power dissipation than the conventional centre-tapped and current doubler topologies, leading to better thermal management and potentially improved power density. In addition, compared to the centre-tapped rectifier, transformer secondary winding utilization is also improved and the transformer winding conduction loss is reduced significantly. Keeping in view the size, weight, and ease of transformer design, the centre-tapped converter and current doubler converter are considered in the present work.

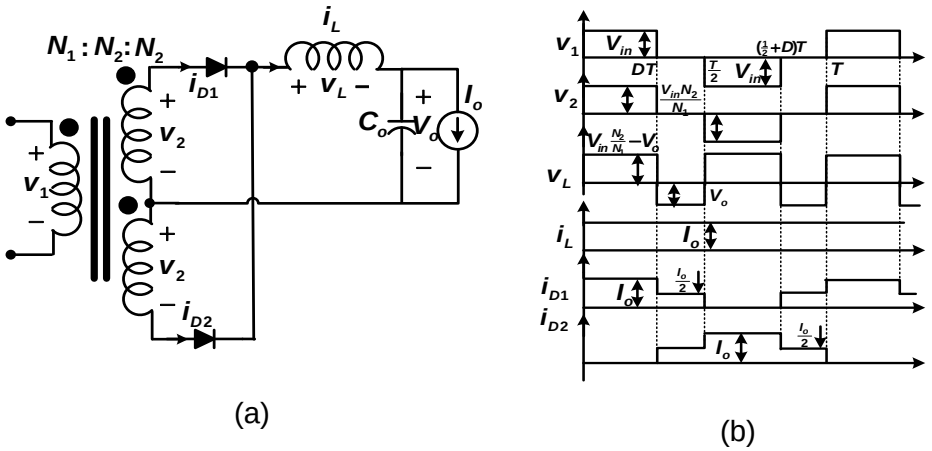
Although in recent years, the improvement of voltage and current rating of self commutated devices, particularly MOSFET and IGBT, and contemporary improvements in magnetic core have brought the possibility to explore their use in high power applications, but it would be difficult to meet high power demand using individual power switch. Therefore,

reduction of voltage and current stresses in power switches is done through device integration to reduce voltage stress in front end converter and current stress in load end converter [9, 33].



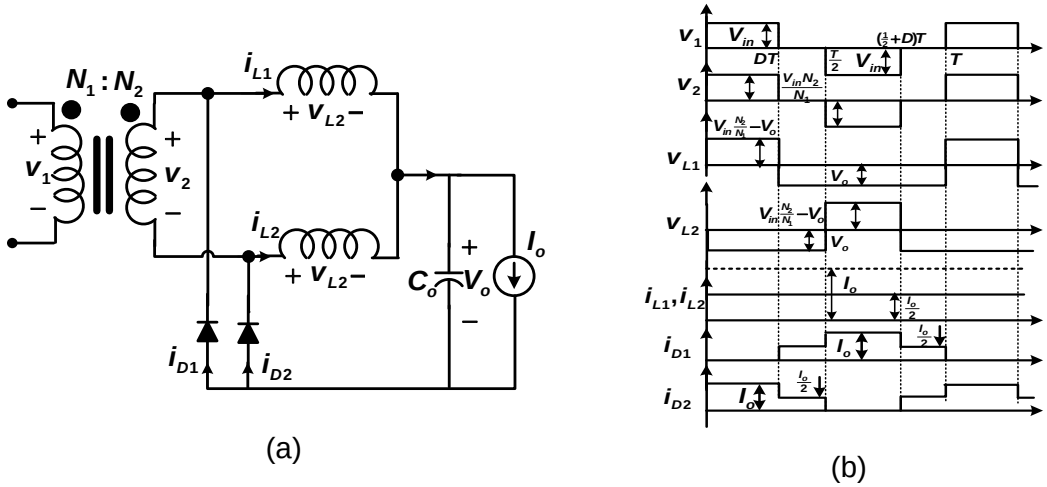
(a) (b)

Fig.1.15 Forward converter (a) Power circuit (b) Voltage & current waveforms



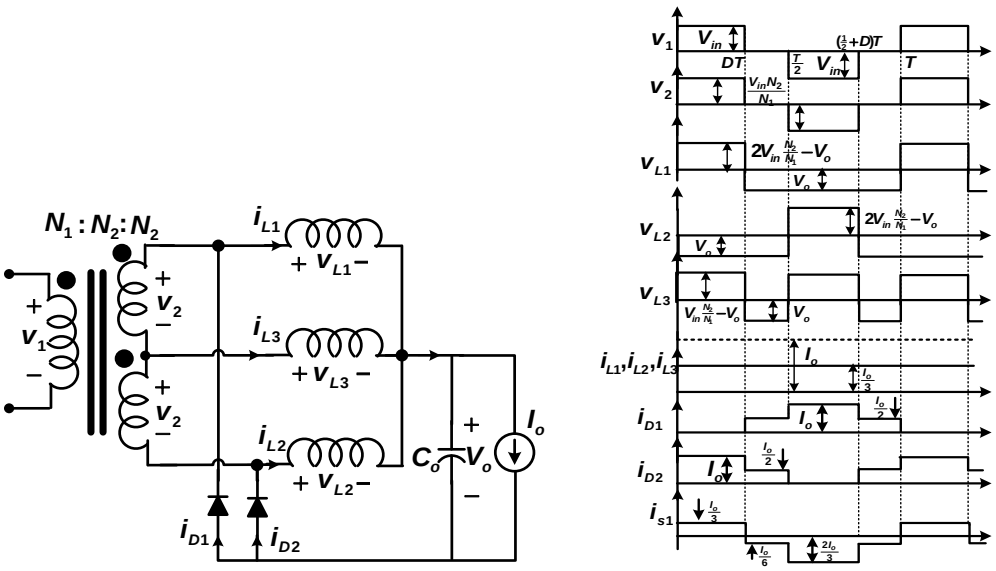
(a) (b)

Fig.1.16 Centre-Tapped converter (a) Power circuit (b) Voltage & current waveforms



(a) (b)

Fig.1.17 Current Doubler converter (a) Power circuit (b) Voltage & current waveforms



(a) (b)

Fig.1.18 Current Tripler converter (a) Power circuit (b) Voltage & current waveforms

Table 1.3 Single-phase load end converter topology

Parameters	Load End Converter			
	Forward type	Centre-Tapped	Current Doubler	Current Tripler
Topology	Fig.1.15	Fig.1.16	Fig.1.17	Fig.1.18
Transformer structure	Two –windings	Centre- tapped	Two windings	Centre-tapped
RMS diode Current (I_{D1},I_{D2})	$I_o\sqrt{D}$, $I_o\sqrt{(1-D)}$	$I_o\sqrt{\frac{1}{4}+\frac{D}{2}}$, $I_o\sqrt{\frac{1}{4}+\frac{D}{2}}$	$I_o\sqrt{\frac{1}{4}+\frac{D}{2}}$, $I_o\sqrt{\frac{1}{4}+\frac{D}{2}}$	$I_o\sqrt{\frac{1}{4}+\frac{D}{2}}$, $I_o\sqrt{\frac{1}{4}+\frac{D}{2}}$
Inductor Current (I_{L1},I_{L2},I_{L3})	I_0	I_0	$\frac{I_o}{2},\frac{I_o}{2}$	$\frac{I_o}{2},\frac{I_o}{2},\frac{I_o}{2}$
Transformer sec.current	$I_o\sqrt{D}$	$I_0\sqrt{\frac{1}{4}+\frac{D}{2}}$	$I_o\sqrt{\frac{D}{2}}$	$I_0\sqrt{\frac{1}{36}+\frac{D}{2}}$

The modular approach of designing second stage of LVHC converter is normally adopted in which low power low voltage DC-DC converter modules are integrated in any combination, series or parallel, both at input side as well as output side to achieve desired specifications. This approach helps in reducing voltage and current stresses on devices over single high power centralized power converter [34, 35]. There are four possible connections of DC-DC converter modules namely Input-parallel-output-parallel (IPOP), input-parallel–output-series (IPOS), input-series–output-seriesl (ISOS), and input-series–output-parallel (ISOP) as shown in Fig.1.19. In IPOP and IPOS connected systems as shown in Fig.1.19(a)-(b), the modules are connected in parallel at the input side, and thus the input voltage of each module are equal by virtue of its connection. Therefore, the module output currents are made equal for IPOP systems and the output module voltages are made equal

for IPOS systems respectively. For ISOP and ISOS systems of Fig.1.19(c)-(d), the modules are connected in series at the input side and therefore input voltage to each module is to be controlled. To ensure equal output power sharing by each module, the output current and output voltage for ISOP and ISOS systems are to be controlled by controller respectively. Input and output side circuit parameters to be controlled for various interconnection of small DC-DC converter modules are tabulated in Table 1.4.

The ISOP connection of DC-DC converter modules is preferred for low voltage high current applications due to reduce voltage stress at front end converter and reduced current stresses at load end converter, increase power processing capability, improved reliability because of more even distribution of stresses, ease of expansion and repair.

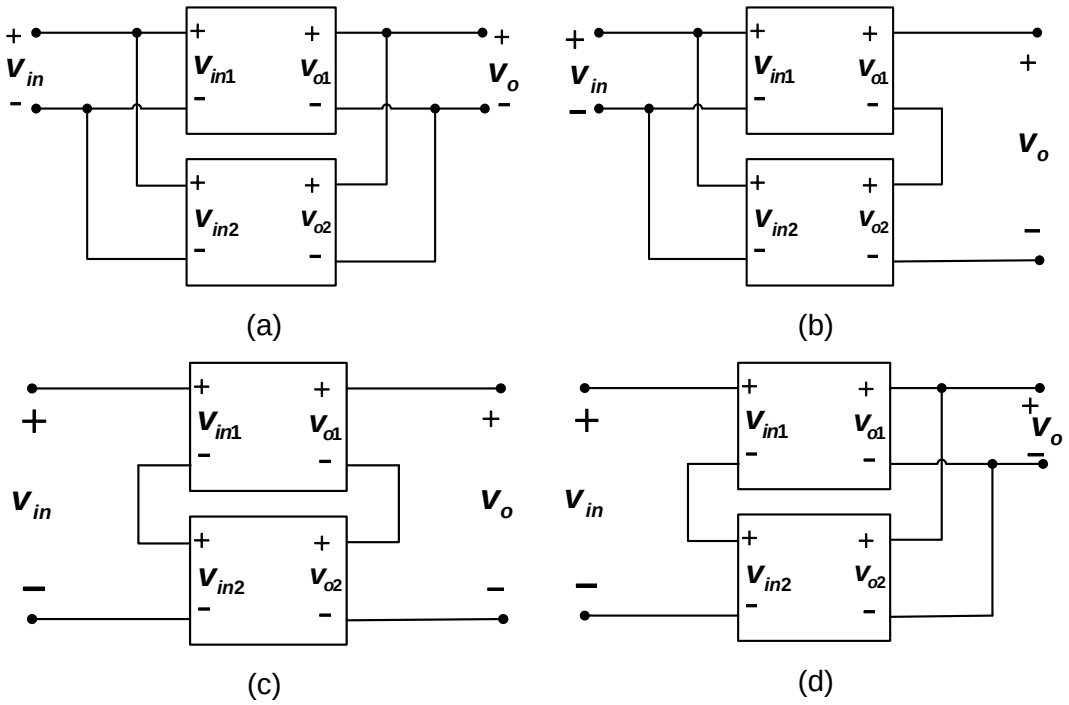


Fig.1.19 Interconnection of multiple DC-DC converters (a) IPOP (b) IPOS (c) ISOS (d) ISOP

Xinbo Ruan et al. [35-39] have presented basic classification scheme for paralleling of DC-DC converters and general control problems of DC-DC converters connected in ISOP and ISOS connections. In this approach any mismatch in circuit parameters leads to unequal sharing of power by individual converter module and hence suffers more stress so the probability of its failure increases. Therefore, to share equal power by each module, different controllers are employed. Furthermore, relationship between input voltage sharing (IVS) and output current sharing (OCS) of the constituent modules has been developed by power balance theory to reduce the number of controllers.

Ned Mohan et al. [40-42] have proposed a common control scheme using one current mode or voltage mode controller to ensure active voltage sharing and load current sharing of ‘n’ DC-DC converters, connected in series at the input and parallel at the output by applying

a common duty ratio. Furthermore, a three-loop control scheme, consisting of a common output voltage loop, individual inner current loops, and individual input voltage loops, has been reported to achieve input voltage and load current sharing.

Single-phase isolated DC-DC converters specially forward converter [43-45], Phase Shifted Full Bridge Converter [36, 46, 47] and half bridge are generally designed with ISOP connection to meet desired specifications.

Table 1.4 Interconnection of small DC-DC converter modules

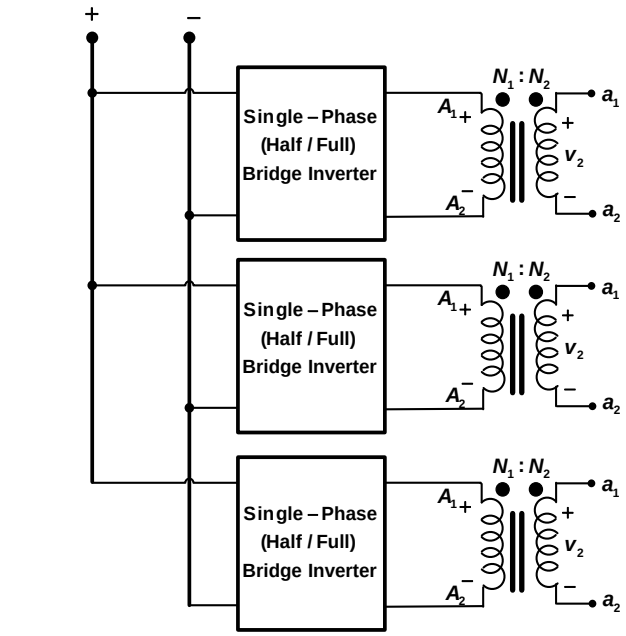
<table>
<tr><td rowspan="2">Connection</td><td colspan="2">Input side</td><td colspan="2">Output side</td></tr>
<tr><td>Input voltages</td><td>Input currents</td><td>Output voltages</td><td>Output currents</td></tr>
<tr><td>IPOP</td><td rowspan="2">Equal by connection</td><td rowspan="2">Equal sharing achievable by Control</td><td>Equal by connection</td><td>Equal sharing achievable by Control</td></tr>
<tr><td>IPOS</td><td>Equal sharing achievable by Control</td><td>Equal by connection</td></tr>
<tr><td>ISOS</td><td rowspan="2">Equal sharing achievable by Control</td><td rowspan="2">Equal by connection</td><td>Equal sharing achievable by Control</td><td>Equal by connection</td></tr>
<tr><td>ISOP</td><td>Equal by connection</td><td>Equal sharing achievable by Control</td></tr>
</table>

As power rating of converters increases, more number of small DC-DC converter modules are integrated in ISOP connection to achieve desired specification. To ensure equal power sharing by each converter module, individual controller is required for ensuring equal voltage at input side and and equal current sharing at output side. Therefore, on account of more number of converter modules and controllers, the system reliability decreases and furthermore design of controllers becomes complex.

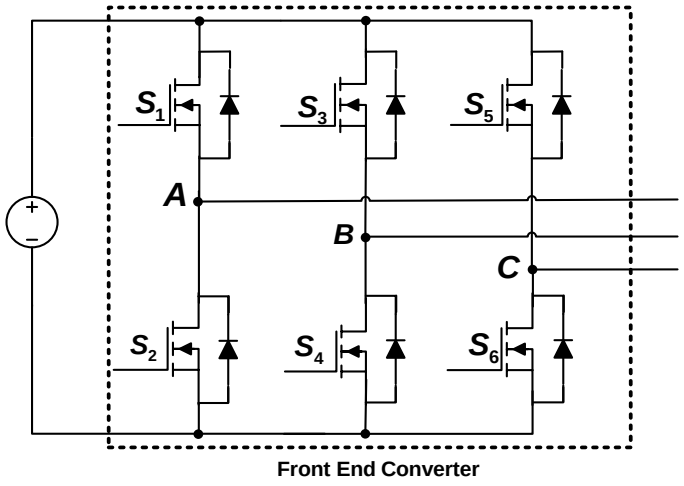
Single-phase isolated topologies are very popular and often used in low power applications. These converters experience high voltage stresses when fed from high input voltage of the order of 400V-1000V DC and employed for high power applications. On the other hand modular approach of realizing power supply, particularly ISOP connection for low voltage high current applications is very popular. But on account of increased number of components & controllers, system reliability decreases and design of controllers also becomes complex [48]. An alternate solution is proposed in [49, 50] in which high frequency link is incorporated using a three-phase inverter and three-phase high frequency transformer.

For high power application, the front end converter comprises of three units of single-phase half or full–bridge inverters connected in parallel and the gating signals for each inverter is phase shifted by 120^0 with respected to each other to generate three ac voltages. These ac voltages are identical and phase shifted by 120^0 to each other and appear as input to three single-phase high frequency transformers as illustrated in Fig.1.20(a). The primary

windings must be isolated from each other, whereas the secondary windings may be connected in Wye or Delta. The transformer secondary windings are normally connected in delta to eliminate triplen harmonics.This arrangement requires three single-phase transformers, 12 power switches and 12 diodes.



(a)



(b)

Fig.1.20 Three-phase front end converter (a) Three units of single-phase inverter (b) Three-phase inverter

Alternatively, three-phase balanced ac voltages can be generated by three-phase bridge inverter comprises of six power switches as shown in Fig.1.20(b). The three-phase output voltages of this topology are fed to primary of three-phase high frequency transformer. A set of symmetrical control signals are employed to control the power switches of each leg. The three legs of inverter operate with interleaved phase shifted manner. The interleaved operation of switches of front end converter enables in reduction of filter size and reduces

RMS current of power switches and hence ease their thermal managements. Furthermore, if three-phase high frequency transformer is used in place of three single-phase high frequency transformers, reduction in transformer core size & weight and losses can be achieved. Additionally, voltage scaling can also be done in addition to turns ratio with proper three-phase connection of windings of transformer.

As load end converter deals with high current, therefore it plays a major role in improving efficiency and thermal heat management. The topology of Fig.1.21(a) offers large conduction losses due to large number of devices in forward path of current, high working temperature and bulky in size & weight. This topology is widely used in PV cell applications. These drawbacks are addressed by providing lesser number of active devices in forward path of current as shown in Fig.1.21(b-f).

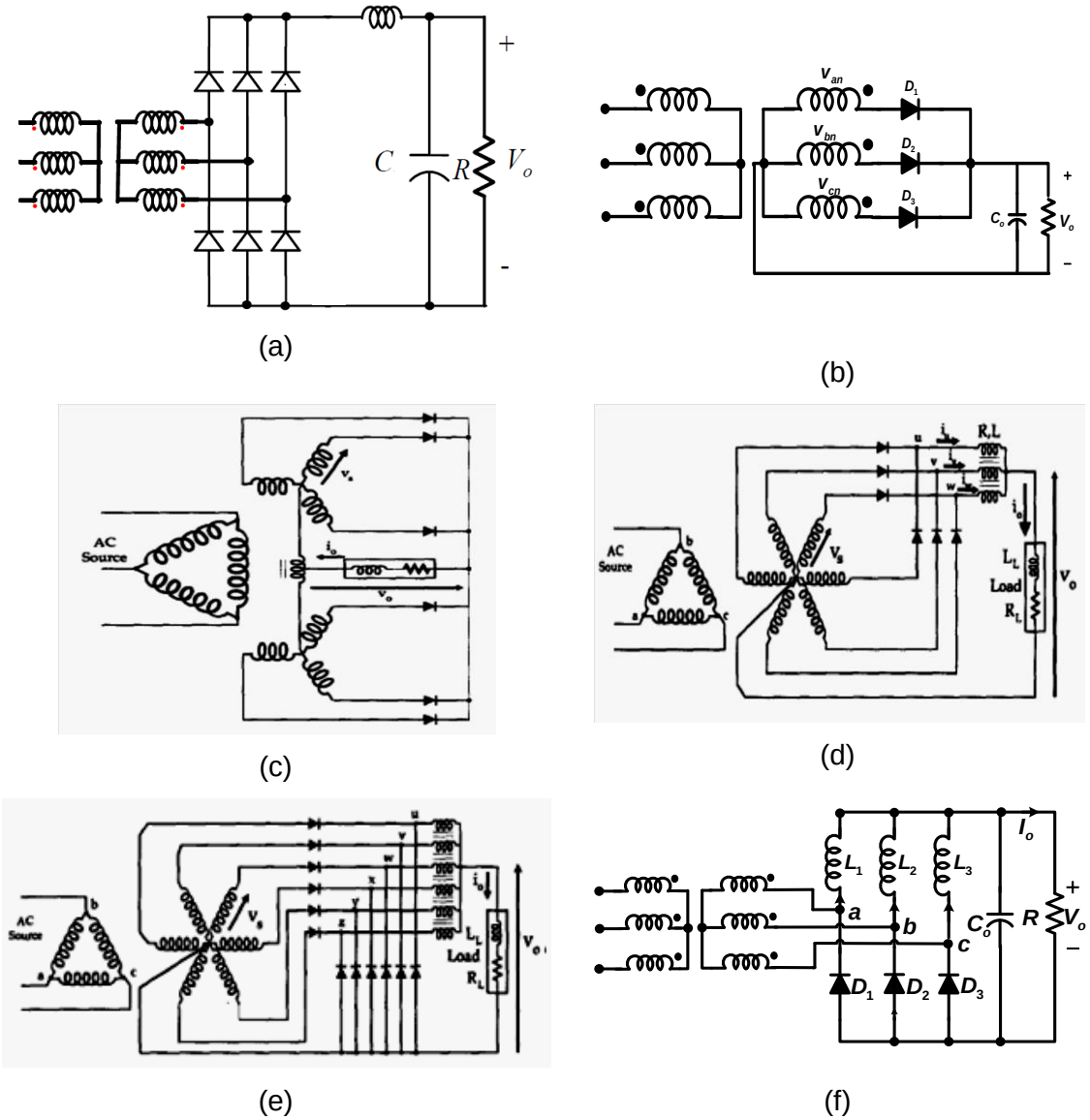


Fig.1.21: Three-phase load end converter topologies[5]

Table 1.5 Summary of three-phase load end converter topologies

Parameters	Topology			
	Fig.1.21(b)	Fig.1.21(c)	Fig.1.21(d)	Fig.1.21(e)
RMS diode current (I_{D1}, I_{D2})	$I_o\sqrt{D}$, $I_o\sqrt{(1-D)}$	$\boldsymbol{I_o\sqrt{\frac{1}{4}+\frac{D}{2}}}$, $\boldsymbol{I_o\sqrt{\frac{1}{4}+\frac{D}{2}}}$	$\boldsymbol{I_o\sqrt{\frac{1}{4}+\frac{D}{2}}}$, $\boldsymbol{I_o\sqrt{\frac{1}{4}+\frac{D}{2}}}$	$\boldsymbol{I_o\sqrt{\frac{1}{4}+\frac{D}{2}}}$, $\boldsymbol{I_o\sqrt{\frac{1}{4}+\frac{D}{2}}}$
Inductor Current (I_{L1}, I_{L2}, I_{L3})	I_0	I_0	$\frac{I_O}{2}, \frac{I_O}{2}$	$\frac{I_0}{2}, \frac{I_0}{2}, \frac{I_0}{2}$

In Fig.1.21(b), it is observed that secondary winding currents contains a DC components and only one secondary winding carries current at particular time. The primary windings must be connected in delta connection to eliminate the DC components in input side. Fig.1.21(c) shows the two Wye connected secondary windings with their neutral connected through inter-phase reactor to prevent the circulating currents between the windings and connected in parallel to provide high output current. However, the design of transformers and inter-phase reactor becomes complex and may lead to circulating currents.

Topology of Fig.1.21(d) can be considered as three single-phase centre-tapped rectifiers that are connected in parallel through three output inductors. Each rectifier is supplied by one of the three centre-tapped secondary windings of transformer. Because of the 120^0 phase among transformer secondary voltages, the full-wave output voltage of each rectifier will be displaced 60^0 among others. Topology shown in Fig.1.21(e) can be considered as six single-phase half wave rectifiers that are connected in parallel through a six-phase output inductor. Each single-phase rectifier is supplied by one phase of secondary windings of the three-phase transformer that is connected as a three-phase to six-phase converter. The total output voltage of the rectifier can be considered as superposition of the output voltage of six single phase half-wave rectifiers.

In order to overcome the problems of large conduction losses, the three-phase version of single-phase current doubler is proposed by D.S. Oliveira and I.Barbi in [51]. The rectifier stage is similar to three-phase, full diode bridge in which upper diodes are replaced by inductors (L_1, L_2, L_3) as shown in Fig.1.21(f) and it is well suitable for high power application at very low voltage.

The front end converter consists of three single-phase full-bridge converter as shown in Fig.1.20(a) and load end converter comprises of three phase full-bridge diode rectifier of Fig.1.21(a). The high frequency isolation is provided through a set of three single-phase transformers, whose secondary windings are connected in a Wye configuration as given in [52, 53]. The Wye connected secondary windings of transformer increases the input primary

winding voltage by $\sqrt{3}$ time in addition to turn ratio. This topology has several disadvantages such as poor heat dissipation, large number of devices in front end converter and poor efficiency.

S.R. Moon et al. in [53], proposed the converter consists of six switches to form three half-bridge phase-legs as shown in Fig.1.20(b), three transformers in Y-Y configuration, a three-phase full-bridge rectifier, and LC filter. In this topology, the output voltage is regulated through symmetrical control PWM signals for switches of front end converter which cause high switching losses due to hard switching. In practice, due to presence of line inductance and leakage inductance of transformer, the converter experiences high circulating and conduction losses. Therefore, soft switching of three-phase resonant pulse-width modulation controlled DC-DC converter with Wye/Wye transformer connection is introduced in [54]. A 1.5 kVA experimental prototype model of three-phase DC resonant PWM DC-DC converter has been implemented with the following circuit parameters: 110V, 12.5 A input, 100V, 12.5A output and 90.9% efficiency. In this topology, duty cycle of each power switch of three-phase bridge inverter requires to vary from 16.67% to 33.33% in order to produce zero to full output voltage. This topology not only shows low efficiency but also suffers from high voltage and current stresses on devices and hence increases the devices rating. Furthermore, Wye/Wye connections of transformer does not provide path of third harmonics current.

A noval three-phase series resonant converter for high power application is given in [55]. The resonant tank is created by external series capacitors and stray inductances of primary and secondary windings of three-phase transformer. All the switches of three-phase front end converter is realised with power MOSFETs and gated with six phase shifted signal of duty ratio 50%. A 5kW prototype model of 400V input, 400V output at 100 kHz is built. The operation of converter was discussed with switching frequency equal and higher to resonant frequency. It was found that the optimum point of operation can be achieved at ZVS and not at ZCS. At ZVS highest efficiency is achieved and the EMI is reduced [56].

A three-phase voltage-fed DC-DC converter is proposed in [57]. The upper and lower switches of each leg are operated with asymmetrical (complementary) switching to regulate the output voltage. Interleaved PWM control of three legs of front end converter are used, which results in increased effective switching frequency. A 1.5 kW prototype of the proposed converter has been built with following specifications: 25-35V DC input, 400V DC output, 50 kHz. The Δ-Y transformer has been constructed with three single-phase transformers. The maximum efficiency of 95.5% was measured at 700W load and its efficiency decreases sharply as the load increases over 700W. This topology is applicable for PV application.

A 1kW prototype model with 400V DC input, 48V DC output, 200 kHz switching frequency, has been developed based on novel current doubler [58]. A 48-V/1.0-V, 100-A, 300-kHz prototype, three-phase version of this topology is implemented in [59, 60] and

achieve 87% efficiency at full load. The use of these rectifiers improve the efficiency of the converter significantly because only three diodes are associated in the secondary side for the conduction losses. Besides, the current in the secondary side of the transformer is also reduced. Therefore, this converter offers improved efficiency as compared to full bridge, forward and centre-tapped rectifier converter and hence well suited for future microprocessors and telecommunications systems. A new non-isolated zero-voltage switching (ZVS) current tripler converter is proposed in [61]. In order to reduce the current stress of the transformer secondary windings and current doubler rectifier, a new rectification converter for high-current isolated converters is proposed in [62]. In this topology, an additional inductor is used to share the load currents other than two inductors in the current doubler structure. The proposed rectification technique has good thermal management and well-distributed power dissipation, and low copper loss for inductors and transformer due to the fact that the load current is better distributed in inductors and the rms current in transformer windings is reduced. However, the concern of this topology is that the current stress of the synchronous rectifier (SR) is not reduced, and consequently, the high-current conduction losses of SRs are not reduced.

1.3.2 Pulse Width Modulation Control

In general, output voltage of DC-DC converter can be controlled in two different ways: variable frequency control and fixed frequency control[63]. In variable frequency control, the time period of switch is allowed to vary keeping either (i) ON-time constant or (ii) OFF-time constant. On the other hand, in fixed frequency operation, ON- time of switch is allowed to vary keeping time period constant. As width of pulse is modified to control output voltage, therefore this method named as Pulse Width Modulation (PWM). The variable frequency operation has some disadvantages as compared to constant frequency operation as given below:

- The switching frequency has to be varied over a wide range for the control of output voltage and therefore, filter design for such wide frequency variations is quite difficult.
- For control of duty cycle, frequency variation would be wide. Therefore, there may be possibility of interference with signalling and telephone lines.
- The large OFF-time may lead to discontinuous mode of operation which is undesirable.

In light of aforesaid limitation of variable frequency operation, the fixed frequency operation is subject of interest for controlling converter.

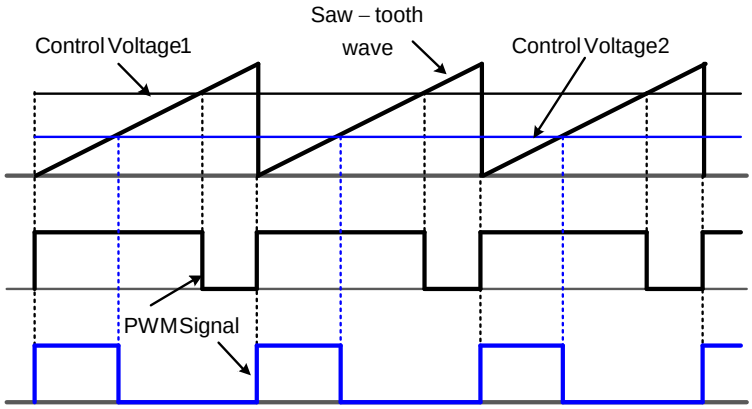


Fig.1.22 Conventional PWM control

(a) Conventional PWM Control

In the conventional PWM control, the PWM signals for the switches of DC/DC converter are generated by controller block in which difference of reference voltage and feedback voltage is fed to PI controller to generate control voltage and further saw-tooth waveform of fixed frequency and magnitude is compared with the control voltage and yields PWM signal as illustrated in Fig.1.22. In order to regulate the output voltage, the control voltage is allowed to vary which results in variable pulse width as shown in Fig.1.22. The PWM signal with two different control voltages where switch is ON for the intervals, where the control voltage is higher than the saw-tooth voltage, and the switch is OFF otherwise is shown in Fig.1.22.

(b) Phase-Shifted PWM Control

The DC-DC converters such as push-pull, half-bridge, full-bridge and multiphase topology comprised of more than one power switch in which power switches are conducted in definite manner. To achieve desired switching pattern for aforementioned converters deliberately phase delay is to be introduced. In this control method, two saw-tooth waveforms with phase delay of ϕ (saw-tooth1, saw-tooth2) are compared with control voltage of constant magnitude of half of the peak value of saw-tooth waveform. Hence, all of the switches have the same duty cycle of 50%, ideally. The compensated error voltage is converted to the phase angle (ϕ) between the two saw-tooth voltage waveforms and hence, in Phase-Shift PWM control method, instead of the control voltage, the phase angle (ϕ) is utilized as the control variable.

As an example, the PWM signals for the switches $(SW1-SW4)$ of full-bridge converter of Fig. 1.12(a) can be generated using two saw-tooth waves and compared with control voltage as depicted in Fig.1.23. As phase delay (ϕ) between two saw-tooth waveforms are allowed to vary, the voltage (V_1) appears across primary windings of transformer is changed.

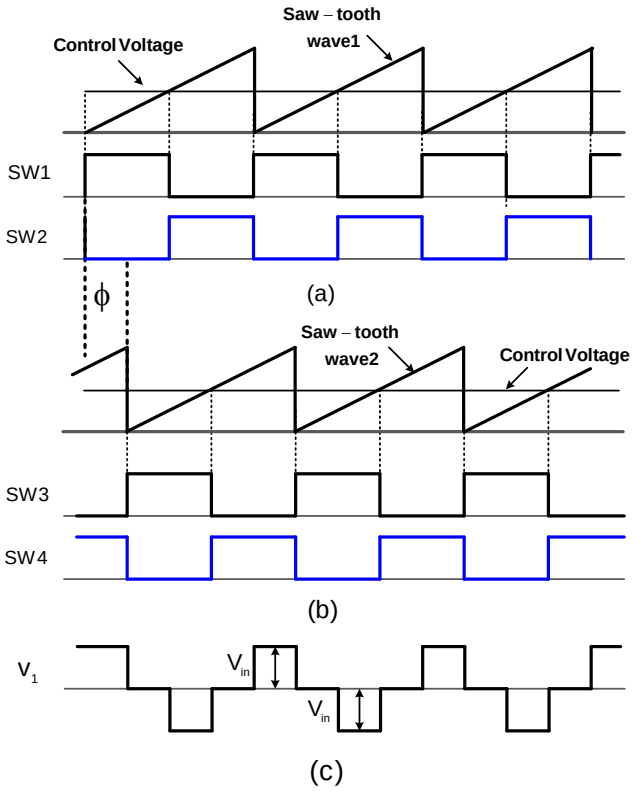


Fig.1.23 Phase-Shift PWM control of full bridge converter of Fig.1.12 (a) Switching signals for SW1&SW2 (b) Switching signals for SW3 &SW4 (c) Waveform of primary voltage

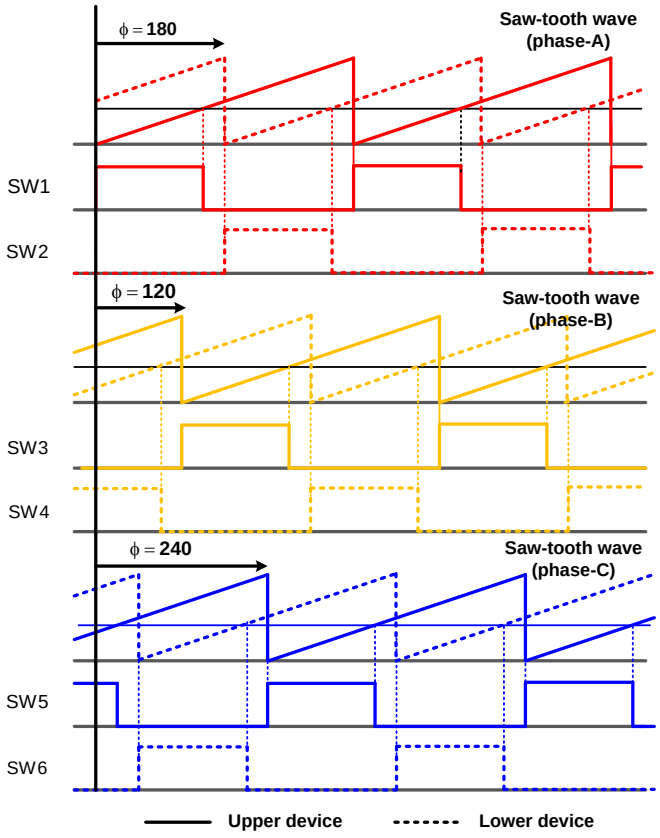


Fig. 1.24 Interleaved PWM Control for three-phase front end converter of Fig.1.20(b): Switching signals for SW1 to SW6

(c) Interleaved PWM Control

Normally, this technique is used in multi-phase DC-DC converter where multiple DC-DC converters are connected in parallel to share large load. In this technique, switching pattern of each module are equally phase-shifted over one switching cycle so that ripples in load current are reduced significantly and hence size and weight of output filter becomes small. Fig. 1.24 shows the interleaved control methods used to generate switching pulses for front end converter shown in Fig.1.20(b). In this topology, three different legs are symmetrically operated with phase delay of 120^0 and the duty cycle of power switches of each leg is limited to 50% to avoid direct short circuit. For low-voltage high-current applications, the power converters must possess compact size, low conduction losses and fast transient response to achieve an accurate output regulation. The transient response can be improved by selecting this control technique which further reduces the output filter inductance.

1.4 Scope of Work and Motivation

On the basis of literature review in area of power supply design for low voltage high power applications, it is found that extensive efforts are being made to meet the challenges face by isolated converters toward design of DC-DC power converters with input voltage ranges from 48V to 300 V DC. However, following issues attract to carry out further research to develop highly efficient, cost effective power supply in LVHC applications.

(a) Line frequency based transformer converters are popular in high power applications, but suffer from several drawbacks such as large size and weight, high conduction losses, low efficiency, relatively small turns ratio, poor sharing of load current among semiconductor switches.

(b) Isolated DC-DC Converters in its primitive forms i.e. Forward, Fly-back, Push-Pull, Half Bridge, Full Bridge, and Hybrid FB (H-FB) experience high voltage stresses when they are fed from large input voltage (400V-1000V).

(c) Three-Level (TL) PWM converter is reported that reduces the voltage stress of the switches to half of the input voltage. This approach worked well and very attractive for medium and high power dc-to-dc conversion fed from large input voltage, but the equipment cost, complexity and reliability suffer due to large components count.

(d) The major losses take place in the rectification stage because of high current and therefore it is necessary to reduce the losses particularly at secondary side by following ways:

- Selecting suitable secondary side Configuration.
- Replacing schottky rectifiers with synchronous rectifiers.
- Employing ZVS/ZCS switching condition.

(e) Normally, magnetic integration methods are used to reduce size and weight. However, in high current applications magnetic stress and thermal management become vital issues. Therefore instead of using a big piece of magnetic core, the bulk magnetic component can be distributed into several small pieces, which have a lower profile, better electrical, mechanical, thermal characteristics.

(f) In high power applications, single phase DC-DC converters experience high stress on devices, and therefore multiphase topology could be the better alternative.

1.5 Proposed Topology for Low Voltage High Current Power Converters

In light of comparative evaluation of power converter topologies subjected to large input DC voltage, high current output, and very low output voltage as discussed above, the modular approach is used to realize LVHC power supply.

The modular approach of designing LVHC power supply includes interconnection of *n* low rating standard modules of DC-DC converter with their inputs in series and outputs in parallel as shown in Fig.1.25. The advantages of modular input series output parallel connected converters includes-

(a) Reduced cost and manufacturing time due to standardization

(b) Increased efficiency due to use of lower voltage MOSFET devices

(c) Lower conversion ratios for low output voltage applications

(d) Reduced switch stress in high input voltage applications

(e) Reduced filtering requirements due to interleaving

As per ISOP connection features, each converter module delivers equal load current of $\left(I_1 = I_2 = ... = I_n = I_o/n\right)$ subjected to each module of the same specifications and fed from same input DC voltage $\left(V_{in}/n\right)$. The input capacitors $\left(C_1, C_2, ...C_n\right)$ are used to divide input DC voltage into n equal voltages $\left(V_{in1} = V_{in2} = ... = V_{inn} = V_{in}/n\right)$ which appeared at the input of each converter module. As each module is connected in parallel at output side and therefore, their output voltages are equal by connection i.e. $\left(V_{o1} = V_{o2} = V_{o3} .... = V_{on} = V_o\right)$. If output current of each module is made equal by current controller i.e. $\left(I_{o1} = I_{o2} = I_{o3} .... = I_{on} = I_o/n\right)$, then equal sharing of power by each module can be maintained subjected to equal input voltage appeared to each module. Therefore, there is a need to make input voltage and output current of each converter module equal. Additionally, to regulate output voltage against parameters variations, output voltage control is needed.

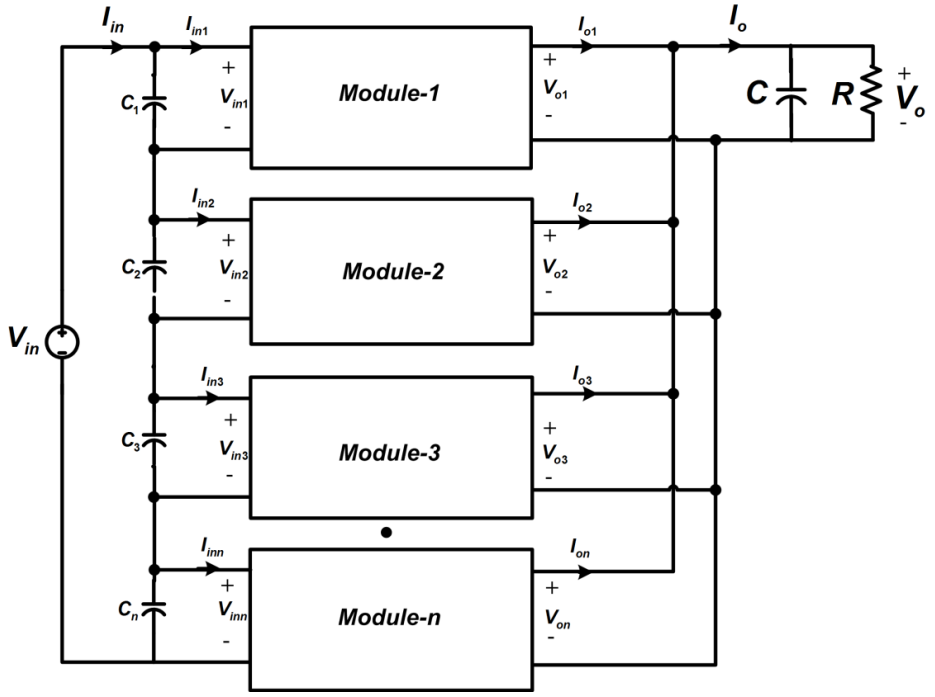


Fig.1.25 Modular approach :ISOP connected multiple DC-DC converter modules

For high power applications, several small rating modules are to be employed in modular approach and to ensure equal power sharing, large number of controllers are required. Therefore, on account of more number of components, controllers, system reliability decreases and furthermore design of controllers becomes complex. Based on study of single-phase front end converter and load end converter, the half-bridge circuit configuration as front end converter and centre-tapped configuration as load end converter offers reduced voltage stress, lesser switching devices, and lesser turn's ratio of transformer, reduced size and weight of filter inductance. Thus, three-phase, high frequency isolated, LLC resonant DC-DC power converter with centre-tapped secondary windings is proposed as shown in Fig.1.26.

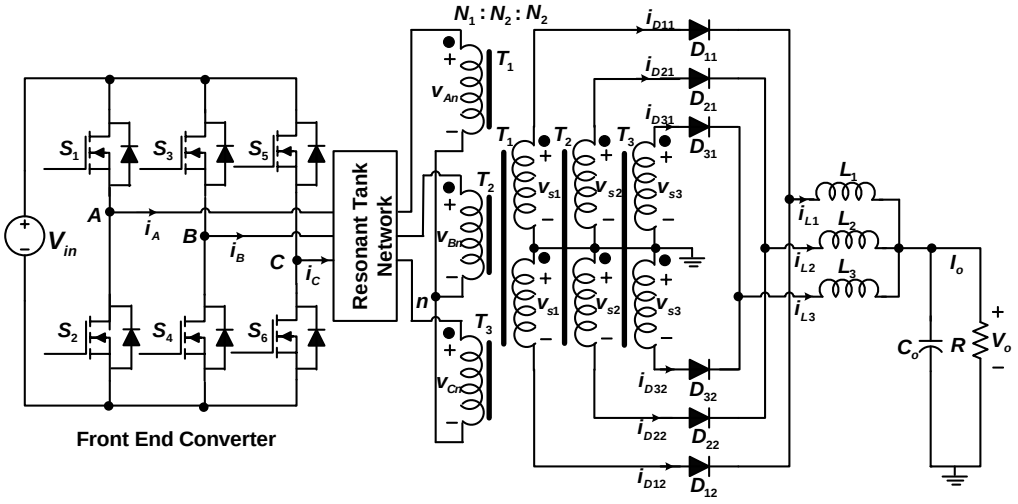
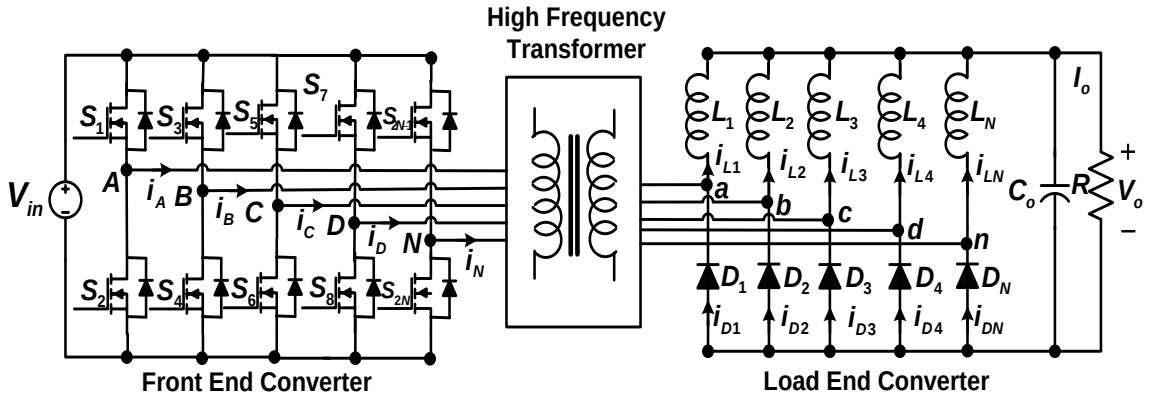


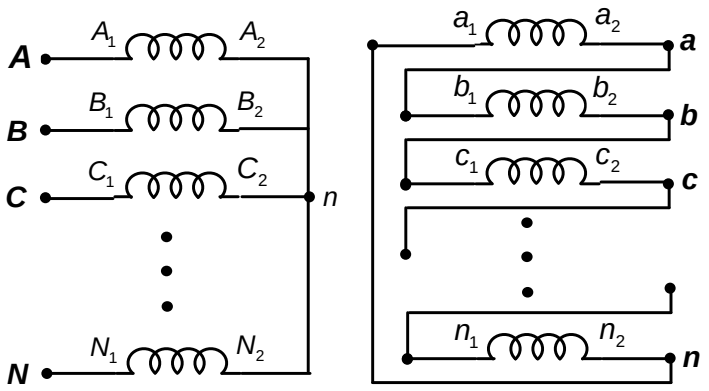
Fig.1.26 Three-phase, high frequency isolated, LLC resonant DC-DC power converter with centre-tapped secondary windings

The modeling, control and design of proposed converter is carried out with symmetrically controlled interleaved PWM control method. This is well suited for medium power applications. The benefits of this topology includes reduced primary voltage, lesser turns ratio, simple self-driven synchronous rectification for wide input voltage range, and reduced size & weight of output inductor due interleaving.

The proposed multi-phase high frequency isolated DC-DC converter consists of three main parts: front end converter, high frequency transformer and load end converter as shown in Fig. 1.27(a). The front end converter comprises of *N* legs and each leg consists of two power switches. The midpoints of each leg are connected to one end of the primary winding of single-phase high frequency transformers and other ends of the primary winding of transformers are made common to form wye-connections as shown in Fig. 1.27(b). On the basis of secondary side load sharing, transformer design and thermal heat dissipation, the load end converter of multi-phase full diode bridge is selected in which upper diodes are replaced by inductors $(L_1, L_2, L_3, ...L_N)$ as shown in Fig. 1.27.



(a)



(b)

Fig. 1.27 Multi-phase high frequency isolated DC-DC converter (a) Power circuit (b) Winding connection of n single-phase high frequency transformer

Keeping in view of low voltage high current applications particularly for industrial processes, three-phase DC-DC converter may not be efficient because of high current stress on devices of load end converter and design of high current output inductors. To cater need of industrial applications, the six-phase version of proposed converter with reduced hardware components in front end converter is proposed as shown in Fig.1.28 which consists of two unit of three-phase high frequency transformer to provide high frequency isolation, voltage scaling and phase shift. One three-phase transformer is connected in $Yd1$ and other transformer is connected in $Yd11$ i.e. primary side of both transformers are connected in wye (*Y*) and secondary windings of both transformers are connected in delta (*d*1) and delta (*d*11) as shown in Fig.1.28.

The proposed converter topology of low voltage high current is simulated, developed and investigated in the present work.

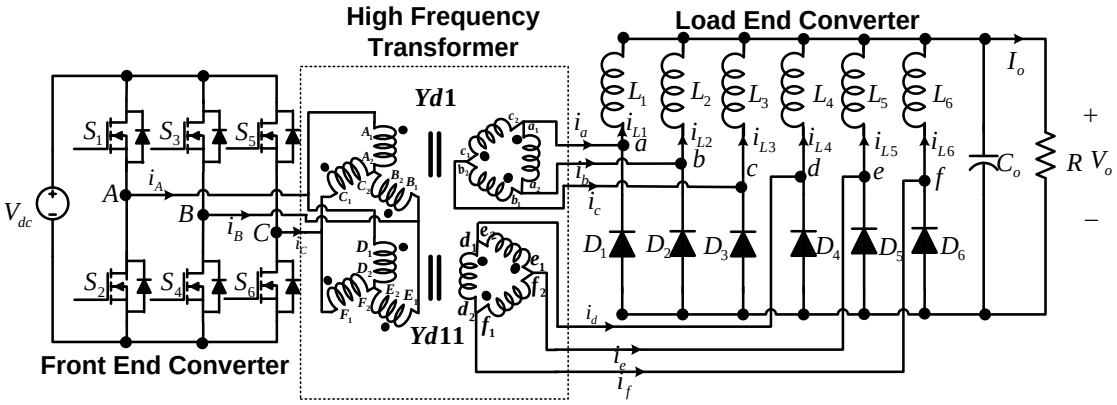


Fig.1.28 Six-phase version of proposed converter with reduced component

1.6 Author's Contribution

The main contributions of the author are as follows-

(a) To begin with, the survey of power converter topologies suitable for low voltage high current applications is carried out. On the basis of literature survey, the high frequency transformer based power converter is selected in which electrical power is processed at two stages namely AC-DC and DC-DC power conversion. In order to meet the requirement of high current at low output voltage, the second stage of power conversion (DC-DC) is developed using following two methods:

- Modular approach based ISOP connected Converter
- Multi-phase technology based converter

(b) Simulation study of the modular approach based ISOP connected multiple converters-

- A 0.5kW, 5V/100A, Simulink model of ISOP connected two push-pull converter is developed which can be extended to 5kW, 5V/1000A by ISOP connection.
- In order to investigate the performance, the effect of parasitic elements such as effective series resistance of capacitors and output inductors, leakage and

magnetizing reactance of transformers are considered. Further to share equal power by constituent push-pull converters, three controllers namely common output voltage controller, inner current controller and input voltage controller are employed and a stable feedback system is designed to regulate output DC voltage.

- A systematic development of a small-signal linear dynamic model of proposed converter is carried out using State-Space Averaging (SSA) technique and transfer functions of different control blocks of converter are obtained. Furthermore, stability analysis of control loops is carried out to ensure closed loop operation.

(c) Design and development of three-phase, high frequency isolated, LLC resonant DC-DC converter with centre-tapped secondary winding of the transformer-

- A 5kW, 5V/1000A simulink model of proposed converter is developed using Simulink and SimPowerSystem^{TM} of MATLAB software for simulation study and its performances are investigated with fixed frequency, symmetrical phase-shift Pulse Width Modulation control method under various operating conditions.
- Improved performance of the converter is achieved by employing Zero Voltage Switching (ZVS) and Zero Current Swicthing (ZCS) condition for the power switches.
- To verify the simulation studies, a downscaled prototype model (75W, 1.5V/50A) is developed and tested under various operating conditions.
- Experimental results are obtained with different operating conditions, during transient as well as steady state.

(d) Design and development of multi-phase, high frequency isolated, DC-DC converter with multi-phase rectification for high power applications-

- A 5kW, 5V/1000A simulink model of three-phase, high frequency isolated, DC-DC converter with three-phase rectification is developed using Simulink and SimPowerSystem^{TM} of MATLAB software for simulation study. The performance of converter is investigated with symmetrical and asymmetrical phase-shift Pulse Width Modulation control method with fixed frequency operation under various operating conditions.
- To verify the simulation studies, a downscaled prototype model rated at 75W 1.5V/50A is developed and tested under various operating conditions with both aforementioned PSPWM control methods.
- Experimental results are obtained with different operating conditions, during transient as well as steady state.

- The performance of the converter with aforementioned PSPWM control methods are compared.

(e) Reduction in hardware components of six-phase version of multi-phase, high frequency isolated, DC-DC converter with multi-phase rectification using phase-shifting transformer-

- For simulation study, a 5kW, 5V/1000A simulink model of three-phase, high frequency isolated, DC-DC converter with multi-phase rectification is developed using Simulink and SimPowerSystem^{TM} of MATLAB software and its performance is investigated with symmetrical and asymmetrical phase-shift Pulse Width Modulation control method with fixed frequency operation under various operating conditions.
- To verify the simulation studies, a downscaled prototype model rated at 150W, 1.5V/100A is developed and tested with both aforementioned PSPWM control method under various operating conditions.
- Various experimental results are obtained under different operating conditions during transient as well as steady state.

1.7 Organization of the Thesis

The thesis is organized in the seven chapters and work described in each chapter is briefly outlined below:

Chapter-1 presents a brief overview of applications which require high power at reduced DC voltage. It also includes the review of converter topologies and control technique suitable for low voltage high current applications. Based on study, the modular approach is used to realise LVHC power supply. Keeping this in mind, the inter-connected modular DC-DC converter and multi-phase DC-DC converters are proposed. Finally scope of work, author's contribution and thesis outlines are presented.

Chapter-2 presents the modular approach of designing low voltage high current power supply using inter-connection of multiple DC-DC modules in which low-power, low-voltage, individual DC-DC modules are connected in series at the input side and parallel at the output side, to realize given system specifications. In this chapter, the simulink model of ISOP connected push-pull converters with interleaved control method is developed and its performance is investigated under steady-state and dynamic conditions.

Chapter-3 includes the design of system hardware for prototype models of three-phase LLC resonant DC-DC power converter and multi-phase high frequency isolated DC-DC converter with multi-phase rectifications. In this chapter design of basic parts such as power circuit, control circuit and measurement circuits are discussed. A dSPACE-DS1104 is used

for implementation of the control circuit and real-time generation of control pulses for all the power switches of the converter.

Chapter-4 presents high-frequency isolated three-phase LLC resonant DC-DC converter which is suitable for medium power applications. It provides high current at low output voltage, isolation, good regulation against load and line disturbances, and fast dynamic response. In this chapter, the modelling, control and design of proposed converter are carried out under symmetrical control with fixed frequency operation and its steady-state analysis has been presented according to the description of the operational stages of the converter. In order to investigate the performance, the simulation study in carried out using the Simulink and SimPowerSystem^{TM} of MATLAB software. Based on mathematical analysis, a 1.5V/ 50A prototype model is built and tested under various operating conditions.

Chapter-5 deals with modelling, control and design of three-phase, high frequency isolated, DC-DC converter operated under symmetrical control and asymmetrical control with fixed frequency operation. In this chapter, steady state analysis is presented according to the description of the operational stages of the converter. In order to investigate the performance, the simulation study is carried out using Simulink and SimPowerSystem^{TM} of MATLAB software and a prototype model is developed and tested under various operating conditions.

In the chapter-6, high frequency isolated multi-phase DC-DC converter with multi-phase rectification is proposed which is well suited for Industrial applications such as welding, plasma cutting, and surface hardening require high power at reduced DC voltage. In these applications, the rating of power supply varies from few kilowatts to hundreds of kilowatts. In comparison with conventional welding machine employed in many industries, the performance of proposed converter is improved significantly in terms of size and weight, efficiency and dynamic response. The simulation and experimental studies of proposed converter are carried output and obtained results under different operating conditions are presented.

The main conclusion of the work and possible future research are summarized in Chapter-7. At the end, the list of references and appendices are provided.

CHAPTER 2: INTER-CONNECTED MULTIPLE DC-DC CONVERTER

[This chapter deals with a modular approach of designing Low Voltage High Current power supply using interconnection of multiple DC-DC modules where low-power, low-voltage, individual modules can be connected in series at the input side and parallel at the output side, to realize system specifications.The effect of parasitic elements such as effective series resistance(ESR) of capacitor and output inductors, leakage and magnetising reactance of transformers are included while system modelling. A systematic development of a small-signal linear dynamic model of proposed converter is carried out using State-Space Averaging (SSA) technique and the transfer functions of different control blocks of converter are obtained. Furthermore, stability analysis of control loops is carried out to ensure closed loop operation. The simulink model of proposed converter is developed using MATLAB Simulink and SIM Power System tool box.The performance of two modules of push-pull converters with ISOP connection under interleaved control technique is investigated under steady state and dynamic conditions].

2.1 Introduction

AC-DC conversion using Power- Factor-Correction (PFC) converters typically provide high DC voltage to downstream DC-DC converter. For instance, In $3-\phi$ PFC converter with line voltage 415V, 50 Hz supply, the output DC voltage can be as high as 800V-1000V. Such large DC voltage, imposed high voltage stresses to devices of DC-DC converters that are connected to it. Furthermore, the choice of devices that can withstand such high DC voltage stresses is limited, and their cost is usually very high. Therefore, it is necessary to reduce the voltage stresses of the switching devices by proper choice of topologies and/or the use of appropriate switching techniques. Multilevel converters have been used to reduce voltage stresses[64-66], but their effectiveness relies on the use of a sufficient number of "levels," which is often restricted by relatively large quantity of additional clamping diodes or flying capacitors and the increased complexity of the associated control. On the other hand, inter-connection of multiple DC-DC converter, particularly, ISOP connection is a better choice to reduce voltage stresses on devices. In ISOP connection, low-power, low-voltage module of single-phase DC-DC converters are integrated with series at input side and parallel at ouput side [35,43,67]. This modular approach of design power converter exhibit several merits as follows:

- Reduced voltage stress in each module as multiple low-power converters are used to achieve the total power demand.
- Simple design due to standard modules and reduced power level of individual modules.

- Reduced output current ripples due to application of an appropriate interleaving technique.
- Changes in power specification and voltage level with changes in the number of modules, rather than designing a new converter system.
- Easy to repair such systems since on-line replacement of faulty modules is possible.
- High efficiency, low voltage conversion ratio and cost, reduced output filtering requirements, and less manufacturing time.

In view of above merits, ISOP connection is used in LVHC power supply [44].

2.2 System Configuration and Control Scheme

2.2.1 Power Circuit

Fig. 2.1 shows n modules of DC-DC converter inter-connected in series at input side and in parallel at output side (ISOP) to reduce voltage stress on devices and to share high output current. The converter modules of same rating may not be identical and therefore, any mismatch in circuit parameters lead to unequal sharing of power by individual converter module. The module which supplies more power than other, suffers more stress so the probability of its failure increases. In order to provide stable operation of proposed system, each constituent converter modules must be identical, i.e. they have identical topology and specifications and share equal power. If the efficiency of each converter module is assumed to be 100%. Then for power conversion, we have

$$\begin{aligned} &V_{in1}I_{in1} = V_{o1}I_{o1},\ V_{in2}I_{in2} = V_{o2}I_{o2},\ V_{in3}I_{in3} = V_{o3}I_{o3} \\ &.,.,V_{inn}I_{inn} = V_{on}I_{on} \end{aligned} \tag{2.1}$$

As per ISOP connection features, each converter module delivers equal load current of $\left(I_1 = I_2 = ... = I_n = I_o/n\right)$ subjected to each module of the same specifications and fed from same input DC voltage $\left(V_{in}/n\right)$. The input capacitors $\left(C_1, C_2, ...C_n\right)$ are used to divide input DC voltage into n equal voltages $\left(V_{in1} = V_{in2} = ... = V_{inn} = V_{in}/n\right)$ which appeared at input of each converter module. As each module is connected in parallel at output side and therefore, all the output voltages are equal by connection i.e. $\left(V_{o1} = V_{o2} = V_{o3} .... = V_{on} = V_o\right)$. If output current of each module is made equal by current controller i.e. $\left(I_{o1} = I_{o2} = I_{o3} .... = I_{on} = I_o/n\right)$, then from equation (2.1), the equal sharing of power by each module can be maintained subjected to equal input voltage appeared to each module. Therefore, input voltage and output current of each converter module needs to make equal. Additionally, to regulate output voltage against parameters variations, output voltage control is needed.

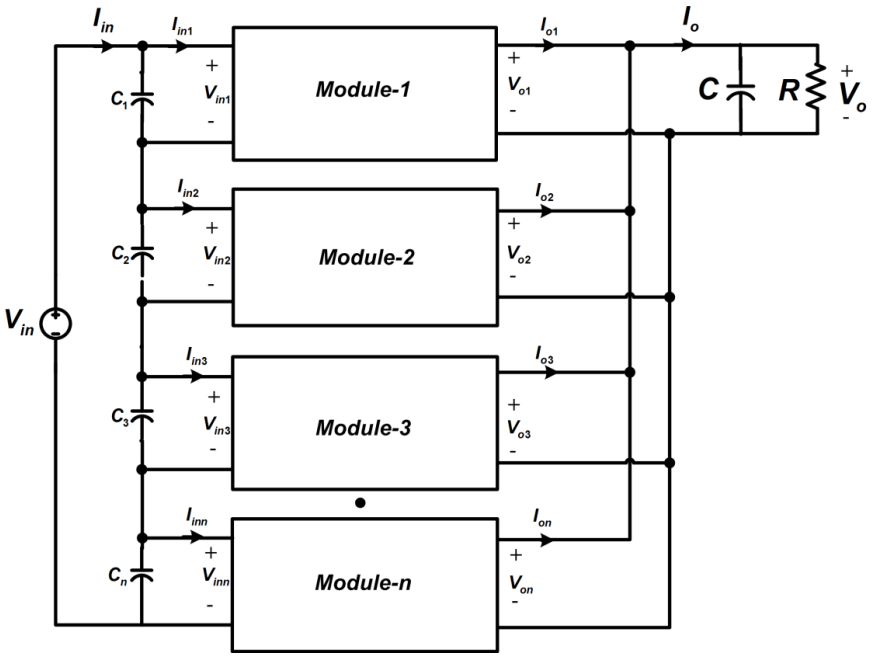


Fig. 2.1 ISOP connected multiple DC-DC converter modules

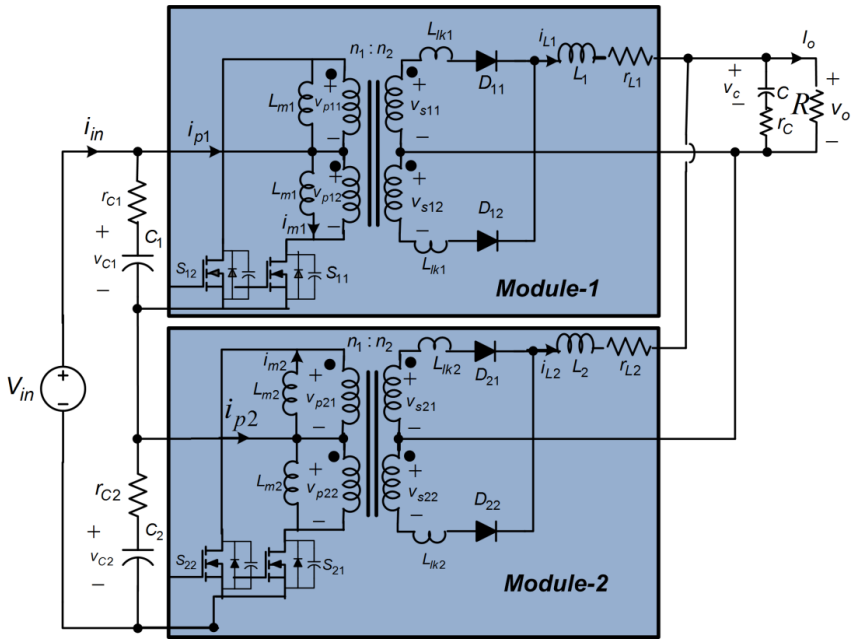
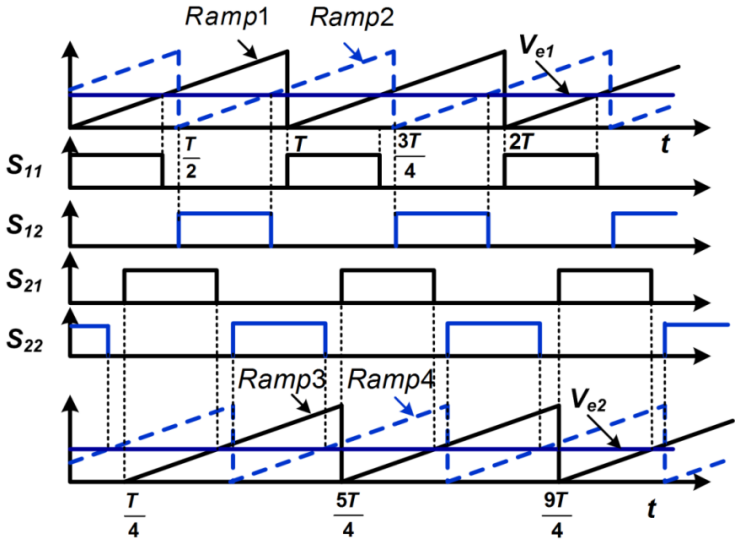


Fig.2.2 Power circuit of ISOP connected push-pull converters

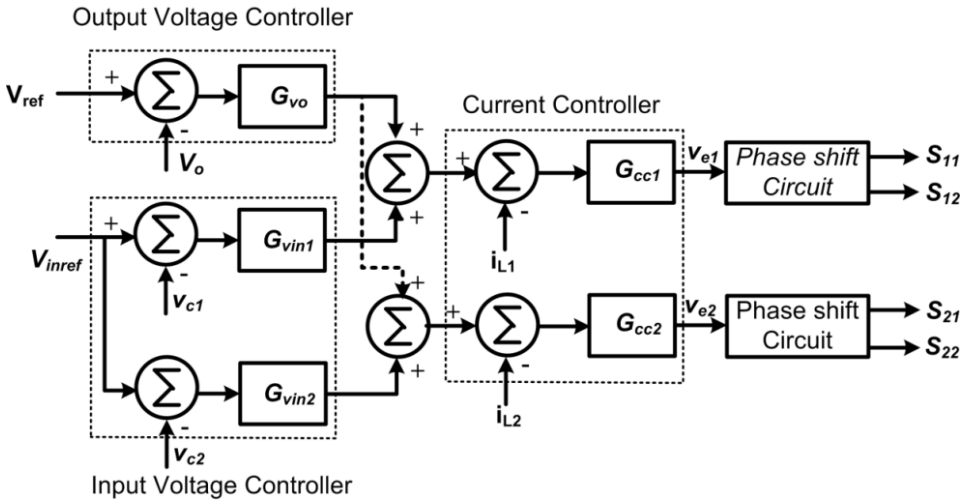
As an illustration, two identical modules of push-pull converters are connected in series at input and in parallel at output as shown in Fig.2.2. It consists of power switches $(S_{11},S_{12},S_{21},S_{22})$, rectifier power diodes $(D_{11},D_{12},D_{21},D_{22})$, centre-tapped transformers, input capacitors (C_1,C_2) and output inductors (L_1,L_2). To investigate its in-depth performance, effect of parasitic elements such as effective series resistance (ESR) of capacitor and output inductors, leakage and magnetizing reactance of transformers are also considered as shown in Fig.2.2.

2.2.2 Control Strategy

The power switches of both modules are controlled by switching signals as shown in Fig.2.3(a). Using this switching pattern, the ripple in output-filter-capacitor get reduced due to the ripple cancellation effect. Additionally the effective ripple frequencies of the output-filter-capacitor current and the input current are increased with increase in number of interleaved modules. As a result, the size of the output filter capacitor gets reduced significantly.



(a)



(b)

Fig.2.3 Control scheme of ISOP connected push-pull converters

(a) Switching waveforms (b) Schematic of diagram of controller

To establish stable closed loop control of converter the output voltage (V_o), individual inductor currents (i_{L1}, i_{L2}) and input capacitor voltage (v_{C1}, v_{C2}) are sensed and fed to concerned points of common output voltage controller, individual inner current controller and individual input voltage controller as shown in Fig.2.3 (b). The output signals $(V_{e1} \& V_{e2})$ of current controllers are fed to two phase-shift circuit. Each phase-shift circuits comprises of

two saw-tooth waveforms (*Ramp1 & Ramp2*) and (*Ramp3 & Ramp4*). The saw-tooth waveforms (*Ramp1 & Ramp2)* are phase shifted by 180^0 between each other and compared with v_{e1} to generate switching signals for power switches (S_{11}, S_{12}). Similarly, the saw-tooth waveforms (*Ramp3 & Ramp4*) are phase shifted by 180^0 between each other and compared with v_{e2} to generate switching signals for power switches (S_{21}, S_{22}). The switching pattern of switches of these two modules is phase shifted by 90^0 to ensure interleaved operation as shown in Fig.2.3(a).

2.3 Operation, Modeling and Analysis of the Converter

Based on switching state of switches $(S_{11}, S_{12}, S_{21}, S_{22})$, the operation of the ISOP connected push-pull converters is divided into mainly eight different operating modes (mode-1 to mode-8) over one full switching cycle as shown in Fig.2.4. The switching state of power switches under different modes of operation is tabulated in Table 2.1. The steady state analysis of the converter under fixed frequency, interleaved PWM control is carried out and operating waveforms of key parameters are shown in Fig.2.4.

Table 2.1 Operational table

		Figure	Time Interval	Duration	State of switching devices			
					S_{11}	S_{12}	S_{21}	S_{22}
Mode-1		Fig.2.5(a)	$t_0 \le t \le t_1$	$(2D-1)T/4$	ON	OFF	OFF	ON
Mode-2	T_1	Fig.2.6(a)	$t_1 \le t \le t_1 + T_o$	$(1-D)T/2$	ON	OFF	OFF	OFF
	T_2	Fig.2.6.(b)	$t_1 + T_o \le t \le t_2$		ON	OFF	OFF	OFF
Mode-3		Fig.2.5(c)	$t_2 \le t \le t_3$	$(2D-1)T/4$	ON	OFF	ON	OFF
Mode-4	T_1	Fig.2.5(d)	$t_3 \le t \le t_3 + T_o$	$(1-D)T/2$	OFF	OFF	ON	OFF
	T_2		$t_3 + T_o \le t \le t_4$		OFF	OFF	ON	OFF
Mode-5		Fig.2.5(e)	$t_4 \le t \le t_5$	$(2D-1)T/4$	OFF	ON	ON	OFF
Mode-6	T_1	Fig.2.5(f)	$t_5 \le t \le t_5 + T_o$	$(1-D)T/2$	OFF	ON	OFF	OFF
	T_2		$t_5 + T_o \le t \le t_6$		OFF	ON	OFF	OFF
Mode-7		Fig.2.5(g)	$t_6 \le t \le t_7$	$(2D-1)T/4$	OFF	ON	OFF	ON
Mode-8	T_1	Fig.2.5(h)	$t_7 \le t \le t_7 + T_o$	$(1-D)T/2$	OFF	OFF	OFF	ON
	T_2		$t_7 + T_o \le t \le t_8$		OFF	OFF	OFF	ON

As there are eight operating modes of operation and power switches conducting during first half-period and second half-period are symmetrical, therefore, detailed operation of converter during first half-period are discussed below:

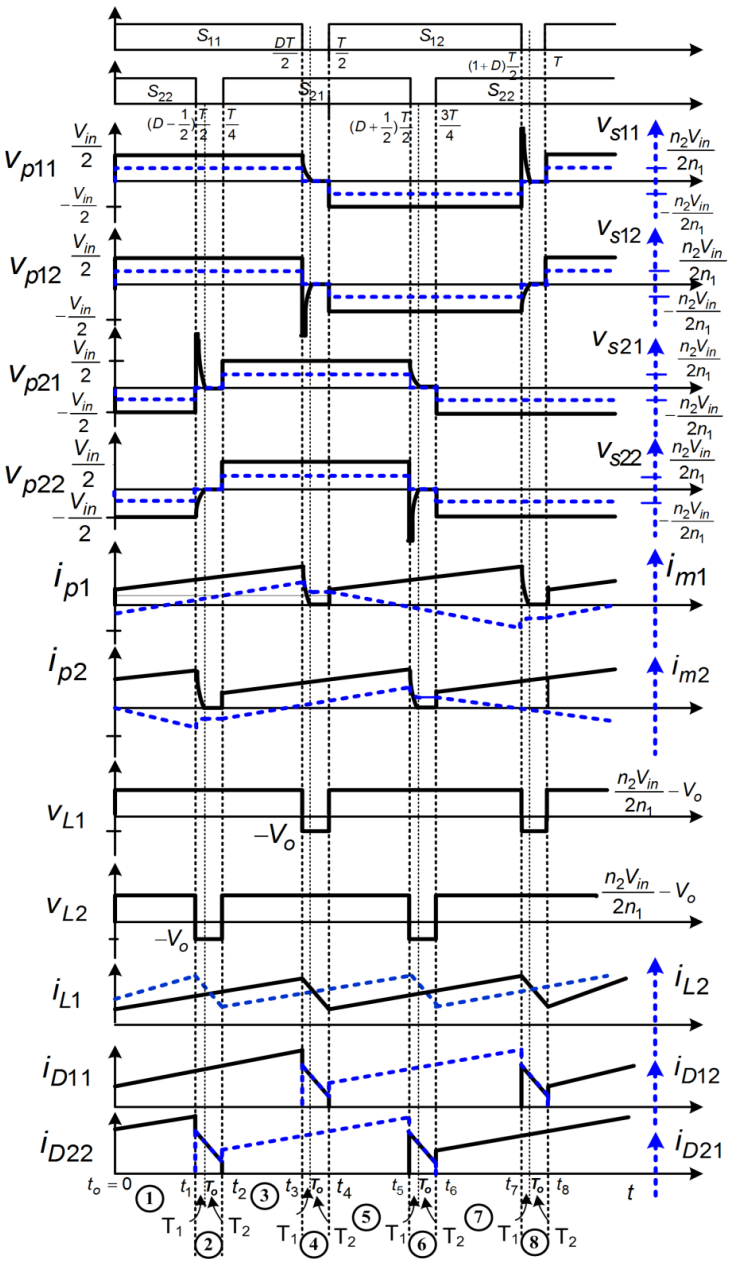
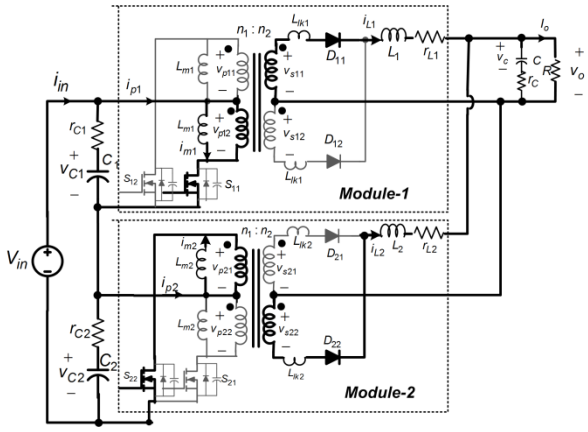
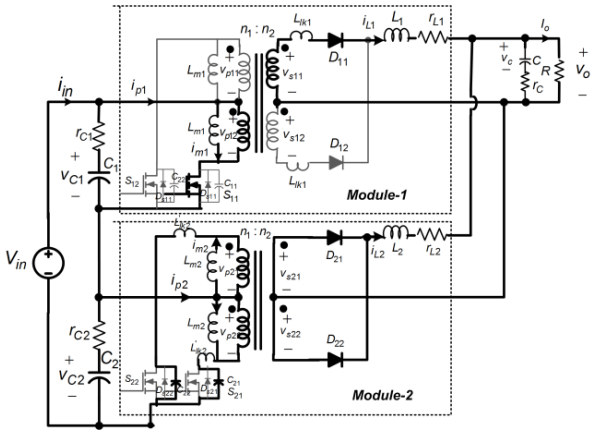


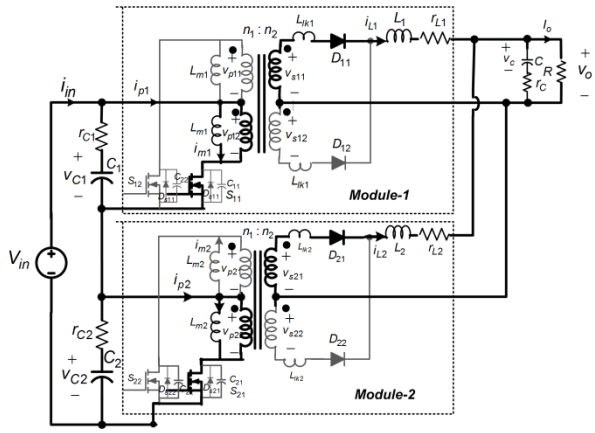
Fig.2.4 Steady-state voltage and current waveforms



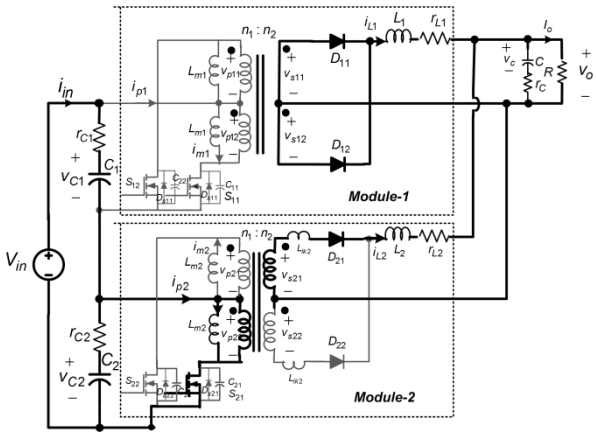
(a) mode-1



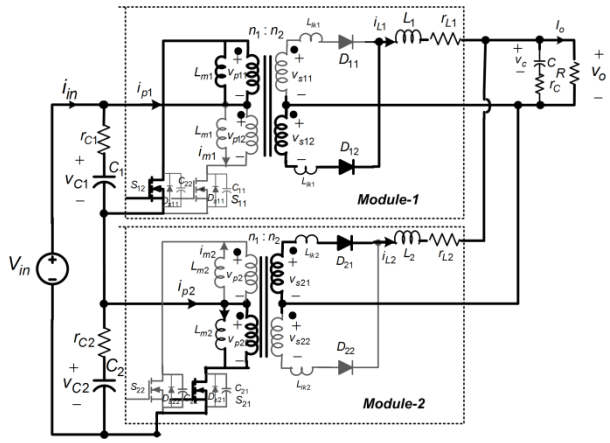
(b) mode-2



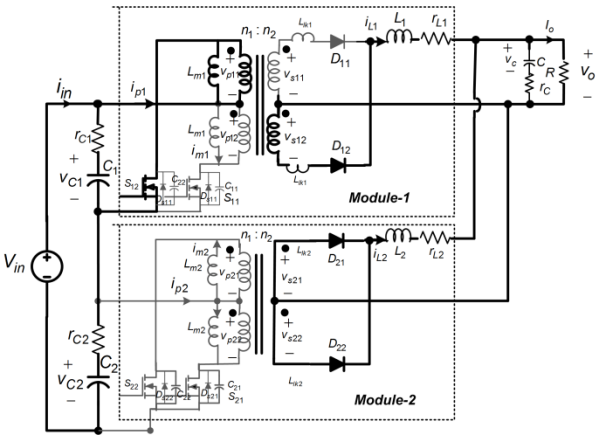
(c) mode-3



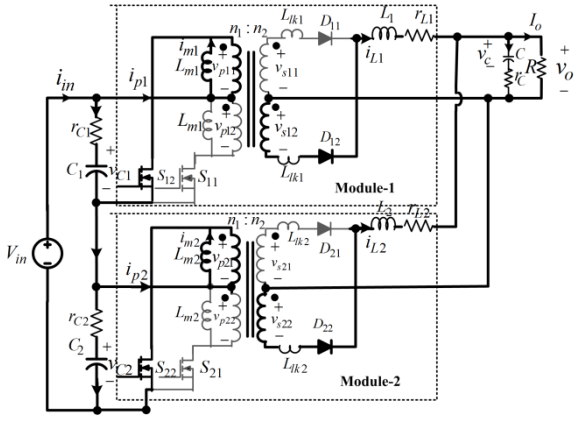
(d) mode-4



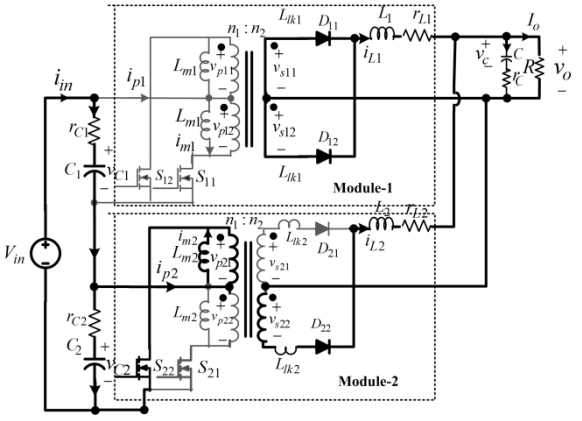
(e) mode-5



(f) mode-6



(g) mode-7



(h) mode-8

Fig. 2.5 Equivalent circuits under various modes of operation (a) mode-1 (b) mode-2 (c) mode-3 (d) mode-4 (e) mode-5 (f) mode-6 (g) mode-7 (h) mode-8

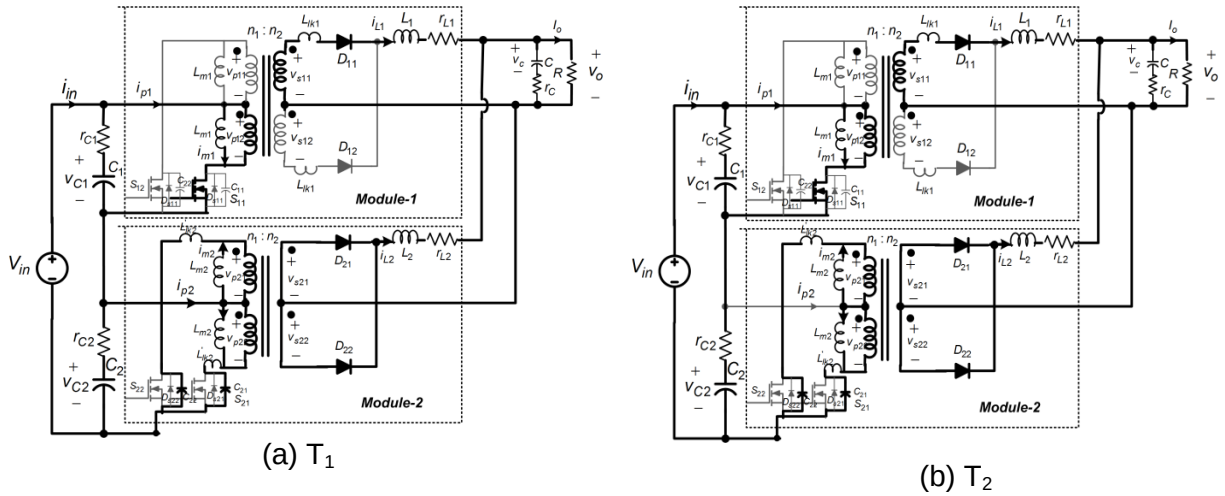
(a) Mode-1 $(t_o \le t \le t_1)$

During this mode, power switches $(S_{11} \& S_{22})$ are ON and switches $(S_{12} \& S_{21})$ are OFF. The equivalent circuit during this mode is given in Fig. 2.5 (a) with conducting path marked with bold line. Under steady state condition, the input DC voltage $\left(V_{in}/2\right)$ is applied to one half of primary windings of both transformers and only one half of secondary winding of both the transformers feed the load through rectifying diodes $(D_{11} \& D_{22})$ as illustrated in Fig. 2.5 (a). The voltage and current associated with different parts of converter during this mode of operation is tabulated in Table 2.2. The mode-1 terminates with turning OFF of power switch (S_{22}).

(b) Mode-2 $(t_1 \le t \le t_2)$

This mode starts with turning OFF of S_{22} at instant $t = t_1$. The switch S_{11} continues to conduct same as in mode-1 as shown in Fig.2.4. The operation of converter in this mode can be further subdivided in two sub-intervals $(T_1 \& T_2)$ as illustrated in Fig.2.6.

Referring to Fig.2.4, each power switch of modules is subjected to at least twice the DC voltage that appears across half of the primary winding (V_{C1}, V_{C2}) of transformer. However, the maximum stress is somewhat more than twice of (V_{C1}, V_{C2}).The excess voltage stress is caused due to leakage inductance. Referring to Fig.2.6(a), at the instant $(t = t_1)$, when S_{22} is turned OFF, switch current (i_{P2}) falls rapidly and causes a positive spike in input voltage of transformer primary (v_{p21}) due to leakage inductance drop of transformer. Subinterval (T_1) is over when i_{p2} becomes zero.



(a) T_1 (b) T_2

Fig.2.6 Equivalent circuits of sub-intervals of mode-2 (a) T_1 (b) T_2

During subinterval (T_2) as shown in Fig.2.6(b) only magnetizing currents of lower transformer remain in circuit. At $t = t_1 + T_o$, the voltage across primary windings of transformer become zero and output inductor L_2 forces rectifier D_{21} to conduct a long with D_{22}.Thus, both rectifier diodes (D_{21},D_{22}) conduct simultaneously and the transformer secondary is shorted as shown in Fig.2.6(b). These sub-intervals appear during switching of each switch as given in Table 2.1.

(c) Mode-3 $(t_2 \le t \le t_3)$

This mode starts at $t = t_2$ with turning ON of S_{21}. Switch S_{11} remains in conducting state as in mode-1. The equivalent circuit during this mode is given in Fig. 2.5 (c) with conducting path marked with bold line. It is observed that half of input DC voltage appears across one half of primary winding of both modules which induce voltage in secondary windings. The induced secondary winding voltages force rectifier diodes $(D_{11} \& D_{21})$ to conduct and deliver energy to load. The voltage and current associated with different parts of converter during this mode of operation is tabulated in Table 2.2. This mode terminates with turning OFF of power switch (S_{11}) at instant $t = DT/2$.

(d) Mode-4 $(t_3 \le t \le t_4)$

At the beginning of this mode, switch (S_{11}) is turned OFF at time instant $t = DT/2$, and power switch (S_{21}) remain conducting as in mode-3. Similar to mode-2, in this mode also, There are two sub-intervals $(T_1 \& T_2)$. Referring to Fig. 2.5(d), at the instant $(t = t_3)$, when switch S_{11} is turned OFF, the switch current (i_{P1}) falls rapidly and causes a negative spike in input voltage of transformer primary (v_{p12}) due to leakage inductance drop of transformer. Subinterval (T_1) comes to end with i_{p1} becoming zero. During subinterval (T_2) as shown in Fig.2.4 only magnetizing currents of upper transformer remain in circuit. At $t = t_3 + T_o$, The voltage across primary windings of transformer become zero and output inductor L_1 forces rectifier D_{11} to conduct a long with D_{12}.Thus, both rectifier diodes (D_{11},D_{12}) conduct simultaneously and the transformer secondary windings is shorted.

Similarly, remaining operating modes of second half-period can be explained. The parameters associated with transformers, output filter inductors, rectifier diodes under different operating modes are tabulated in Table 2.2 and equivalent circuits during each operating mode indicating current conduction path with bold line are shown in Fig. 2.5.

Table 2.2 Summary of circuit parameters

	Mode of Operation							
	1	2	3	4	5	6	7	8
v_{p11}	$\frac{V_{in}}{2}$	$\frac{V_{in}}{2}$	$\frac{V_{in}}{2}$	0	$-\frac{V_{in}}{2}$	$-\frac{V_{in}}{2}$	$-\frac{V_{in}}{2}$	0
v_{p12}	$\frac{V_{in}}{2}$	$\frac{V_{in}}{2}$	$\frac{V_{in}}{2}$	0	$-\frac{V_{in}}{2}$	$-\frac{V_{in}}{2}$	$-\frac{V_{in}}{2}$	0
v_{p21}	$-\frac{V_{in}}{2}$	0	$\frac{V_{in}}{2}$	$-\frac{V_{in}}{2}$	$\frac{V_{in}}{2}$	0	$-\frac{V_{in}}{2}$	$-\frac{V_{in}}{2}$
v_{p22}	$-\frac{V_{in}}{2}$	0	$\frac{V_{in}}{2}$	$-\frac{V_{in}}{2}$	$\frac{V_{in}}{2}$	0	$-\frac{V_{in}}{2}$	$-\frac{V_{in}}{2}$
v_{s11}	$\frac{n_2}{n_1}\frac{V_{in}}{2}$	$\frac{n_2}{n_1}\frac{V_{in}}{2}$	$\frac{n_2}{n_1}\frac{V_{in}}{2}$	0	$-\frac{n_2}{n_1}\frac{V_{in}}{2}$	$-\frac{n_2}{n_1}\frac{V_{in}}{2}$	$-\frac{n_2}{n_1}\frac{V_{in}}{2}$	0
v_{s12}	$\frac{n_2}{n_1}\frac{V_{in}}{2}$	$\frac{n_2}{n_1}\frac{V_{in}}{2}$	$\frac{n_2}{n_1}\frac{V_{in}}{2}$	0	$-\frac{n_2}{n_1}\frac{V_{in}}{2}$	$-\frac{n_2}{n_1}\frac{V_{in}}{2}$	$-\frac{n_2}{n_1}\frac{V_{in}}{2}$	0
v_{s21}	$-\frac{n_2}{n_1}\frac{V_{in}}{2}$	0	$\frac{n_2}{n_1}\frac{V_{in}}{2}$	$-\frac{n_2}{n_1}\frac{V_{in}}{2}$	$\frac{n_2}{n_1}\frac{V_{in}}{2}$	0	$-\frac{n_2}{n_1}\frac{V_{in}}{2}$	$-\frac{n_2}{n_1}\frac{V_{in}}{2}$
v_{s22}	$-\frac{n_2}{n_1}\frac{V_{in}}{2}$	0	$\frac{n_2}{n_1}\frac{V_{in}}{2}$	$-\frac{n_2}{n_1}\frac{V_{in}}{2}$	$\frac{n_2}{n_1}\frac{V_{in}}{2}$	0	$-\frac{n_2}{n_1}\frac{V_{in}}{2}$	$-\frac{n_2}{n_1}\frac{V_{in}}{2}$
v_{L1}	$\frac{n_2}{n_1}\frac{V_{in}}{2}-V_o$	$\frac{n_2}{n_1}\frac{V_{in}}{2}-V_o$	$\frac{n_2}{n_1}\frac{V_{in}}{2}-V_o$	$-V_o$	$\frac{n_2}{n_1}\frac{V_{in}}{2}-V_o$	$\frac{n_2}{n_1}\frac{V_{in}}{2}-V_o$	$\frac{n_2}{n_1}\frac{V_{in}}{2}-V_o$	$-V_o$
v_{L2}	$\frac{n_2}{n_1}\frac{V_{in}}{2}-V_o$	$-V_o$	$\frac{n_2}{n_1}\frac{V_{in}}{2}-V_o$	$\frac{n_2}{n_1}\frac{V_{in}}{2}-V_o$	$\frac{n_2}{n_1}\frac{V_{in}}{2}-V_o$	$-V_o$	$\frac{n_2}{n_1}\frac{V_{in}}{2}-V_o$	$\frac{n_2}{n_1}\frac{V_{in}}{2}-V_o$
i_{L1}	$m_1 t + I_{L1\min}$	$m_1(t-t_1)$ $+I_{L1}(t_1)$	$m_1(t-t_2)$ $+I_{L1}(t_1)$	$m_3(t-t_3)$ $+I_{L1\max}$	$m_1(t-t_4)$ $+I_{L1\min}$	$m_1(t-t_5)$ $+I_{L1}(t_5)$	$m_1(t-t_6)$ $+I_{L1}(t_6)$	$m_3(t-t_7)$ $+I_{L1\max}$
i_{L2}	$m_2 t + I_{L2\min}$	$m_4(t-t_1)$ $+I_{L2\max}$	$m_2(t-t_2)$ $+I_{L2\min}$	$m_2(t-t_3)$ $+I_{L2}(t_3)$	$m_2(t-t_4)$ $+I_{L2}(t_4)$	$m_4(t-t_5)$ $+I_{L2\max}$	$m_2(t-t_6)$ $+I_{L2\min}$	$m_2(t-t_7)$ $+I_{L2}(t_7)$
i_{D11}	$m_1 t + I_{L1\min}$	$m_1(t-t_1)$ $+I_{L1}(t_1)$	$m_1(t-t_2)$ $+I_{L1}(t_1)$	$0.5m_3(t-t_3)$ $+I_{L1\max}$	0	0	0	$0.5m_3(t-t_7)$ $+I_{L1\max}$
i_{D12}	0	0	0	$0.5m_3(t-t_3)$ $+I_{L1\max}$	$m_1(t-t_4)$ $+I_{L1\min}$	$m_1(t-t_5)$ $+I_{L1}(t_5)$	$m_1(t-t_6)$ $+I_{L1}(t_6)$	$0.5m_3(t-t_7)$ $+I_{L1\max}$
i_{D21}	0	$0.5m_4(t-t_1)$ $+I_{L2\max}$	$m_2(t-t_2)$ $+I_{L2\min}$	$m_2(t-t_3)$ $+I_{L2}(t_3)$	$m_2(t-t_4)$ $+I_{L2}(t_4)$	$0.5m_4(t-t_5)$ $+I_{L2\max}$	0	0
i_{D22}	$m_2 t + I_{L2\min}$	$0.5m_4(t-t_1)$ $+I_{L2\max}$	0	0	0	$0.5m_4(t-t_5)$ $+I_{L2\max}$	$m_2(t-t_6)$ $+I_{L2\min}$	$m_2(t-t_7)$ $+I_{L2}(t_7)$

where, $m_1 = \frac{\frac{n_2}{n_1}\frac{V_{in}}{2}-V_o}{L_1}$, $m_2 = \frac{\frac{n_2}{n_1}\frac{V_{in}}{2}-V_o}{L_2}$, $m_3 = \frac{-V_o}{L_1}$, $m_4 = \frac{-V_o}{L_2}$

2.4 Design of Power Circuit Parameters

Power circuit design of proposed converter includes selection of mainly four components: input capacitors, output filter inductors, output filter capacitor and high frequency transformer with centre-tapped primary and secondary windings.

2.4.1 Input voltage divider

The capacitors (C_1, C_2) are used to divide input DC voltage (V_{in}) into equal voltages $(V_{in1} = V_{in2} = V_{in}/2)$ at steady state conditions which is to be appeared as input to each converter module as shown in Fig. 2.7.

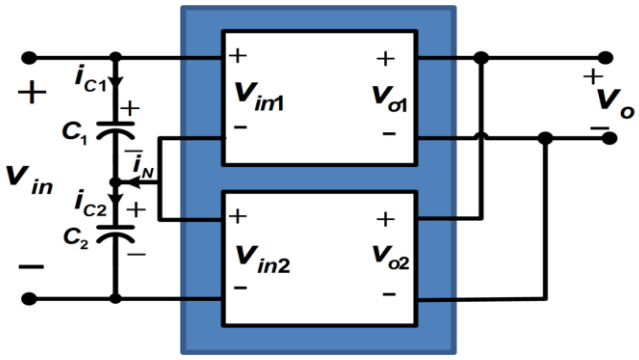


Fig. 2.7 Input voltage divider using capacitors

Refering to Fig. 2.7, the following equations associated with input capacitors are derived:

$$v_{in1} + v_{in2} = V_{in} \tag{2.2}$$

$$\Delta v_{in1} + \Delta v_{in2} = 0 \tag{2.3}$$

$$i_{C1} + i_{C2}\left(\frac{C_1}{C_2}\right) = 0 \tag{2.4}$$

$$i_{C2} = i_{C1} + i_N \tag{2.5}$$

Solving equations (2.4) and (2.5), the capacitor currents $i_{C1}, \& i_{C2}$ can be obtained as below:

$$i_{C1} = -\left(\frac{C_1}{C_1 + C_2}\right) i_N \tag{2.6}$$

$$i_{C2} = \left(\frac{C_2}{C_1 + C_2}\right) i_N \tag{2.7}$$

From equation (2.2) to (2.7), yields equations (2.8) and (2.9)

$$v_{in1} = \frac{V_{in}}{2} - \left(\frac{i_N}{C_1 + C_2}\right) T \tag{2.8}$$

$$v_{in2} = \frac{V_{in}}{2} + \left(\frac{i_N}{C_1 + C_2}\right) T \tag{2.9}$$

$$\Delta v_{in} = v_{in1} - v_{in2} = -\left(\frac{2i_N}{C_1 + C_2}\right)T \tag{2.10}$$

From equation(2.10), it is observed that difference in voltage across input dividing capacitors (Δv_{in}) is function of C_1, C_2, f_{sw} & i_N. Under steady state condition and for large value of C_1, C_2, the voltages at the input of each converter modules are same $\left(V_{in1} = V_{in2} = \frac{V_{in}}{2}\right)$. Therefore, large capacitors are selected for balanced capacitor voltages.

2.4.2 Output Filter Inductor

The output filter inductor of each converter module is designed based on peak-to-peak variation in the inductor current. Refering voltage and current waveform of each inductor in Fig.2.4, the following design equations can be derived.

$$V_o = \frac{n_2}{2n_1} D V_{in} \tag{2.11}$$

$$\Delta i_{L1} = \frac{\frac{n_2}{n_1}\frac{V_{in}}{2} - V_o}{L_1}\frac{DT}{2} \tag{2.12}$$

Equation (2.12) can be combined with equation (2.11) to determine the value of inductance (L_1) for a specified peak-to-peak inductorcurrent (Δi_{L1}) for continuous-current operation:

$$L_1 = \frac{(1-D)V_o}{\Delta i_{L1} 2 f_{sw}} \tag{2.13}$$

2.4.3 Output Filter Capacitor

The ISOP connected modules are operated in interleaved manner such that equal phase shifted between inductor currents (i_{L1}, i_{L2}) is obtained. The current entering at node of the output capacitor and load resistance is the sum of two inductor currents (i_{L1}, i_{L2}), which has a smaller peak-to-peak variation with higher frequency than individual inductor currents. This results in a smaller peak-to-peak variation in capacitor current than would be achieved with a single converter, requiring less capacitance for the same output ripple voltage.

2.5 Dynamic Modelling of Converter with State-Space Averaging (SSA) Technique

A number of ac modelling technigues are reported in the literature, including the current injection approach, circuit averaging, and state-space averaging technique [Erickson, 2001 #253][Moussa, 1990 #254]. The state space averaging technique represents the small signal behavior of converters in terms of a set of linear time invariant state equations driven by a

continuous duty ratio function. This technique offers more compact representation of equations and through this method small signal linear equivalent model for the converter is obtained. From the small signal linear model, it is possible to obtain the input and control transfer functions of the converter. The assumptions for the validity of the state space averaging is that the natural time constants of the converter are much longer than the switching period of operation.

The following steps are followed to reveal the insight of converter's dynamic behaviour as well as providing a stable feedback control design:

Step-1: Determination of state-space equations of the converter for each operating mode.

The equations governing the dynamics of the converter are derived under all operating modes over one switching cycle. In mode-1 $(t_o \le t \le t_1)$, power switches (S_{11}, S_{22}) are ON and (S_{12}, S_{21}) are OFF. The equivalent circuit in this mode is shown in Fig. 2.5(a) and various circuit equations are derived as follows:

$$V_{in} = r_{C1}C_1\frac{dv_{C1}(t)}{dt} + v_{C1}(t) + r_{C2}C_2\frac{dv_{C2}(t)}{dt} + v_{C2}(t) \tag{2.14}$$

$$C_1\frac{dv_{C1}(t)}{dt} + i_{m1}(t) + \frac{i_{L1}(t)}{a} = C_2\frac{dv_{C2}(t)}{dt} + i_{m2}(t) + \frac{i_{L2}(t)}{a} \tag{2.15}$$

Substituting $C_1\frac{dv_{C1}(t)}{dt}$ from equation (2.15) to the equation(2.14), yields equation(2.16):

$$\begin{aligned}\frac{dv_{C2}(t)}{dt} &= \frac{r_{C1}}{a(r_{C1}+r_{C2})C_2}i_{L1}(t) - \frac{r_{C1}}{a(r_{C1}+r_{C2})C_2}i_{L2}(t) - \frac{1}{(r_{C1}+r_{C2})C_2}v_{C1}(t)\\ &- \frac{1}{(r_{C1}+r_{C2})C_2}v_{C2}(t) + \frac{r_{C1}}{(r_{C1}+r_{C2})C_2}i_{m1}(t) - \frac{r_{C1}}{(r_{C1}+r_{C2})C_2}i_{m2}(t) + \frac{1}{(r_{C1}+r_{C2})C_2}V_{in}\end{aligned} \tag{2.16}$$

Substituting $\frac{dv_{C2}(t)}{dt}$ from equation (2.16) to equation(2.15), we evaluate for $\frac{dv_{C1}(t)}{dt}$ as given below:

$$\begin{aligned}\frac{dv_{C1}(t)}{dt} &= -\frac{r_{C2}}{a(r_{C1}+r_{C2})C_1}i_{L1}(t) + \frac{r_{C2}}{a(r_{C1}+r_{C2})C_1}i_{L2}(t) - \frac{1}{(r_{C1}+r_{C2})C_1}v_{C1}(t)\\ &- \frac{1}{(r_{C1}+r_{C2})C_1}v_{C2}(t) - \frac{r_{C2}}{(r_{C1}+r_{C2})C_1}i_{m1}(t) + \frac{r_{C2}}{(r_{C1}+r_{C2})C_1}i_{m2}(t) + \frac{1}{(r_{C1}+r_{C2})C_1}V_{in}\end{aligned} \tag{2.17}$$

$$L_{m1}\frac{di_{m1}(t)}{dt} = v_{C1}(t) + r_{C1}C_1\frac{dv_{C1}(t)}{dt} \tag{2.18}$$

$$L_{m2}\frac{di_{m2}(t)}{dt} = v_{C2}(t) + r_{C21}C_2\frac{dv_{C2}(t)}{dt} \tag{2.19}$$

Using equation(2.16) to equation(2.19), we get $\frac{di_{m1}(t)}{dt}, \frac{di_{m2}(t)}{dt}$ as given in equations(2.20) & equation(2.21):

$$\frac{di_{m1}(t)}{dt} = -\frac{r_{C1}r_{C2}}{a(r_{C1}+r_{C2})L_{m1}}i_{L1}(t) + \frac{r_{C1}r_{C2}}{a(r_{C1}+r_{C2})L_{m1}}i_{L2}(t) + \frac{r_{C2}}{(r_{C1}+r_{C2})L_{m1}}v_{C1}(t)$$
$$-\frac{r_{C1}}{(r_{C1}+r_{C2})L_{m1}}v_{C2}(t) - \frac{r_{C1}r_{C2}}{(r_{C1}+r_{C2})L_{m1}}i_{m1}(t) + \frac{r_{C1}r_{C2}}{(r_{C1}+r_{C2})L_{m1}}i_{m2}(t) \quad (2.20)$$
$$+\frac{r_{C1}}{(r_{C1}+r_{C2})L_{m1}}V_{in}$$

$$\frac{di_{m2}(t)}{dt} = \frac{r_{C1}r_{C2}}{a(r_{C1}+r_{C2})L_{m2}}i_{L1}(t) - \frac{r_{C1}r_{C2}}{a(r_{C1}+r_{C2})L_{m2}}i_{L2}(t) - \frac{r_{C2}}{(r_{C1}+r_{C2})L_{m2}}v_{C1}(t)$$
$$+\frac{r_{C1}}{(r_{C1}+r_{C2})L_{m2}}v_{C2}(t) + \frac{r_{C1}r_{C2}}{(r_{C1}+r_{C2})L_{m2}}i_{m1}(t) - \frac{r_{C1}r_{C2}}{(r_{C1}+r_{C2})L_{m2}}i_{m2}(t) + \frac{r_{C2}}{(r_{C1}+r_{C2})L_{m2}}V_{in} \quad (2.21)$$

$$v_o(t) = v_C(t) + \left\{ i_{L1}(t) + i_{L2}(t) - \frac{v_o(t)}{R} \right\} r_C \quad (2.22)$$

Rearrange the equation(2.22), we obtain $v_o(t)$ as given in equation(2.23):

$$v_o(t) = \frac{Rr_C}{R+r_C}i_{L1}(t) + \frac{Rr_C}{R+r_C}i_{L2}(t) + \frac{R}{R+r_C}v_C(t) \quad (2.23)$$

$$C\frac{dv_C(t)}{dt} = i_{L1}(t) + i_{L2}(t) - \frac{v_o(t)}{R} \quad (2.24)$$

using equation(2.23) and equation(2.24), we get equation(2.25):

$$\frac{dv_C(t)}{dt} = \frac{R}{(R+r_C)C}i_{L1}(t) + \frac{R}{(R+r_C)C}i_{L2}(t) - \frac{1}{(R+r_C)C}v_C(t) \quad (2.25)$$

$$\frac{v_{C1}(t)}{a} + \frac{r_{C1}C_1}{a}\frac{dv_{C1}(t)}{dt} = i_{L1}(t)r_{L1} + (L_1 + L_{lk1})\frac{di_{L1}(t)}{dt} + v_o(t) \quad (2.26)$$

Substituting equation(2.17) and equation(2.23) in equation(2.26), yields equation(2.27):

$$\frac{di_{L1}(t)}{dt} = -\left\{ \frac{r_{L1} + R \,||\, r_C + \frac{r_{C1} \,||\, r_{C2}}{a^2}}{(L_1 + L_{lk1})} \right\} i_{L1}(t) + \left\{ \frac{-R \,||\, r_C + \frac{r_{C1} \,||\, r_{C2}}{a^2}}{(L_1 + L_{lk1})} \right\} i_{L2}(t) - \frac{R}{(R+r_C)(L_1+L_{lk1})}v_C(t)$$
$$+\frac{r_{C2}}{a(r_{C1}+r_{C2})(L_1+L_{lk1})}v_{C1}(t) - \frac{r_{C1}}{a(r_{C1}+r_{C2})(L_1+L_{lk1})}v_{C2}(t) - \frac{r_{C1} \,||\, r_{C2}}{a(L_1+L_{lk1})}i_{m1}(t) \quad (2.27)$$
$$+\frac{r_{C1} \,||\, r_{C2}}{a(L_1+L_{lk1})}i_{m2}(t) + \frac{r_{C1}}{a(r_{C1}+r_{C2})(L_1+L_{lk1})}V_{in}$$

Where $R \,||\, r_C = \frac{Rr_C}{R+r_C}, r_{C1} \,||\, r_{C2} = \frac{r_{C1}r_{C2}}{r_{C1}+r_{C2}}$

$$\frac{v_{C2}(t)}{a} + \frac{r_{C2}C_2}{a}\frac{dv_{C2}(t)}{dt} = i_{L2}(t)r_{L2} + (L_2 + L_{lk2})\frac{di_{L2}(t)}{dt} + v_o(t) \quad (2.28)$$

Substituting equation (2.16) and equation(2.23) in equation(2.28), yields equation(2.29):

$$\frac{di_{L2}(t)}{dt} = \frac{-R \,||\, r_C + \frac{r_{C1} \,||\, r_{C2}}{a^2}}{(L_2 + L_{lk2})} i_{L1}(t) - \frac{r_{L2} + R \,||\, r_C + \frac{r_{C1} \,||\, r_{C2}}{a^2}}{(L_2 + L_{lk2})} i_{L2}(t) - \frac{R}{(R + r_C)(L_2 + L_{lk2})} v_C(t)$$
$$- \frac{r_{C2}}{a(r_{C1} + r_{C2})(L_2 + L_{lk2})} v_{C1}(t) + \frac{r_{C1}}{a(r_{C1} + r_{C2})(L_2 + L_{lk2})} v_{C2}(t) + \frac{r_{C1} \,||\, r_{C2}}{a(L_2 + L_{lk2})} i_{m1}(t) \quad (2.29)$$
$$- \frac{r_{C1} \,||\, r_{C2}}{a(L_2 + L_{lk2})} i_{m2}(t) + \frac{r_{C2}}{a(r_{C1} + r_{C2})(L_2 + L_{lk2})} V_{in}$$

Above dynamic equations of the converter obtained for mode-1, can also be expressed in state space equations: $\frac{dx}{dt} = A_i x + B_i u$ and $y = C_i x + E_i u$ form.

where $i = 1,2,3,3...8$ be the modes of operation,

A_i, B_i, C_i, E_i are of the state space matrix

State variables $x = \begin{bmatrix} i_{L1}(t) & i_{L2}(t) & v_C(t) & v_{C1}(t) & v_{C2}(t) & i_{m1}(t) & i_{m2}(t) \end{bmatrix}^T$,

$u = [V_{in}]$,

$y = \begin{bmatrix} v_o(t) & i_{p1}(t) & i_{p2}(t) \end{bmatrix}^T$

From equations(2.16) to equation(2.29), the state space matrixes can be developed as given below:

$$A_1 = \begin{bmatrix}
-\frac{r_{L1} + R \,||\, r_C + \frac{r_{C1} \,||\, r_{C2}}{a^2}}{(L_1 + L_{lk1})} & \frac{-R \,||\, r_C + \frac{r_{C1} \,||\, r_{C2}}{a^2}}{(L_1 + L_{lk1})} & -\frac{R}{(R + r_C)(L_1 + L_{lk1})} & \frac{r_{C2}}{a(r_{C1} + r_{C2})(L_1 + L_{lk1})} & -\frac{r_{C1}}{a(r_{C1} + r_{C2})(L_1 + L_{lk1})} & -\frac{r_{C1} \,||\, r_{C2}}{a(L_1 + L_{lk1})} & \frac{r_{C1} \,||\, r_{C2}}{a(L_1 + L_{lk1})} \\
\frac{-R \,||\, r_C + \frac{r_{C1} \,||\, r_{C2}}{a^2}}{(L_2 + L_{lk2})} & -\frac{r_{L2} + R \,||\, r_C + \frac{r_{C1} \,||\, r_{C2}}{a^2}}{(L_2 + L_{lk2})} & -\frac{R}{(R + r_C)(L_2 + L_{lk2})} & -\frac{r_{C2}}{a(r_{C1} + r_{C2})(L_2 + L_{lk2})} & -\frac{r_{C1}}{a(r_{C1} + r_{C2})(L_2 + L_{lk2})} & \frac{r_{C1} \,||\, r_{C2}}{a(L_2 + L_{lk2})} & -\frac{r_{C1} \,||\, r_{C2}}{a(L_2 + L_{lk2})} \\
\frac{R}{(R + r_C)C} & \frac{R}{(R + r_C)C} & -\frac{1}{(R + r_C)C} & 0 & 0 & 0 & 0 \\
-\frac{r_{C2}}{a(r_{C1} + r_{C2})C_1} & \frac{r_{C2}}{a(r_{C1} + r_{C2})C_1} & 0 & -\frac{1}{(r_{C1} + r_{C2})C_1} & -\frac{1}{(r_{C1} + r_{C2})C_1} & -\frac{r_{C2}}{(r_{C1} + r_{C2})C_1} & \frac{r_{C2}}{(r_{C1} + r_{C2})C_1} \\
\frac{r_{C1}}{a(r_{C1} + r_{C2})C_2} & -\frac{r_{C1}}{a(r_{C1} + r_{C2})C_2} & 0 & -\frac{1}{(r_{C1} + r_{C2})C_2} & -\frac{1}{(r_{C1} + r_{C2})C_2} & \frac{r_{C1}}{(r_{C1} + r_{C2})C_2} & -\frac{r_{C1}}{(r_{C1} + r_{C2})C_2} \\
-\frac{r_{C1} \,||\, r_{C2}}{aL_{m1}} & \frac{r_{C1} \,||\, r_{C2}}{aL_{m1}} & 0 & \frac{r_{C2}}{(r_{C1} + r_{C2})L_{m1}} & -\frac{r_{C1}}{(r_{C1} + r_{C2})L_{m1}} & -\frac{r_{C1} \,||\, r_{C2}}{L_{m1}} & \frac{r_{C1} \,||\, r_{C2}}{L_{m1}} \\
\frac{r_{C1} \,||\, r_{C2}}{aL_{m2}} & -\frac{r_{C1} \,||\, r_{C2}}{aL_{m2}} & 0 & -\frac{r_{C2}}{(r_{C1} + r_{C2})L_{m2}} & \frac{r_{C1}}{(r_{C1} + r_{C2})L_{m2}} & \frac{r_{C1} \,||\, r_{C2}}{L_{m2}} & -\frac{r_{C1} \,||\, r_{C2}}{L_{m2}}
\end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{r_{C1}}{a(r_{C1} + r_{C2})(L_1 + L_{lk1})} & \frac{r_{C2}}{a(r_{C1} + r_{C2})(L_2 + L_{lk2})} & 0 & \frac{1}{(r_{C1} + r_{C2})C_1} & \frac{1}{(r_{C1} + r_{C2})C_2} & \frac{r_{C1}}{(r_{C1} + r_{C2})L_{m1}} & \frac{r_{C2}}{(r_{C1} + r_{C2})L_{m2}} \end{bmatrix}^T$$

$$C_1 = \begin{bmatrix} \frac{Rr_C}{R + r_C} & \frac{Rr_C}{R + r_C} & \frac{R}{R + r_C} & 0 & 0 & 0 & 0 \\ \frac{1}{a} & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & \frac{1}{a} & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

Similarly, dynamic equations for remaining operating modes (mode-2 to mode-8) can be derived referring Fig.5(b) to Fig.5(h) and the state space matrices $(A_i, B_i, C_i \,\&\, E_i)$ can be obtained.

Step-2: Determination of averaged state-space matrices $(A,B,C\ \&\ E)$.

The averaged state space matrices can be evaluated using equation(2.30).

$$A=\sum_{i=1}^{8}A_i d_i, B=\sum_{i=1}^{8}B_i d_i, C=\sum_{i=1}^{8}C_i d_i, \& E=\sum_{i=1}^{8}E_i d_i \tag{2.30}$$

The following averaged state space matrices are derived:

$$A=\begin{bmatrix}
A_{11} & A_{12} & A_{13} & \frac{r_{C2}}{a(r_{C1}+r_{C2})(L_1+L_{lk1})}D & -\frac{r_{C1}}{a(r_{C1}+r_{C2})(L_1+L_{lk1})}D & -\frac{r_{C1}\|r_{C2}}{a(L_1+L_{lk1})}D & \frac{r_{C1}\|r_{C2}}{a(L_1+L_{lk1})}(2D-1)\\
A_{21} & A_{22} & A_{23} & -\frac{r_{C2}}{a(r_{C1}+r_{C2})(L_2+L_{lk2})}D & -\frac{r_{C1}}{a(r_{C1}+r_{C2})(L_2+L_{lk2})}D & \frac{r_{C1}\|r_{C2}}{a(L_2+L_{lk2})}(2D-1) & -\frac{r_{C1}\|r_{C2}}{a(L_2+L_{lk2})}D\\
\frac{R}{(R+r_C)C} & \frac{R}{(R+r_C)C} & -\frac{1}{(R+r_C)C} & 0 & 0 & 0 & 0\\
-\frac{r_{C2}}{a(r_{C1}+r_{C2})C_1}D & \frac{r_{C2}}{a(r_{C1}+r_{C2})C_1}D & 0 & -\frac{1}{(r_{C1}+r_{C2})C_1} & -\frac{1}{(r_{C1}+r_{C2})C_1} & -\frac{r_{C2}}{(r_{C1}+r_{C2})C_1}D & \frac{r_{C2}}{(r_{C1}+r_{C2})C_1}D\\
\frac{r_{C1}}{a(r_{C1}+r_{C2})C_2}D & -\frac{r_{C1}}{a(r_{C1}+r_{C2})C_2}D & 0 & -\frac{1}{(r_{C1}+r_{C2})C_2} & -\frac{1}{(r_{C1}+r_{C2})C_2} & \frac{r_{C1}}{(r_{C1}+r_{C2})C_2}D & -\frac{r_{C1}}{(r_{C1}+r_{C2})C_2}D\\
-\frac{r_{C1}\|r_{C2}}{aL_{m1}} & \frac{r_{C1}\|r_{C2}}{aL_{m1}}(2D-1) & 0 & \frac{r_{C2}}{(r_{C1}+r_{C2})L_{m1}}D & -\frac{r_{C1}}{(r_{C1}+r_{C2})L_{m1}}D & -\frac{r_{C1}\|r_{C2}}{L_{m1}}D & \frac{r_{C1}\|r_{C2}}{L_{m1}}D\\
\frac{r_{C1}\|r_{C2}}{2aL_{m2}}(2D-1) & -\frac{r_{C1}\|r_{C2}}{2aL_{m2}} & 0 & -\frac{r_{C2}}{2(r_{C1}+r_{C2})L_{m2}} & \frac{r_{C1}}{2(r_{C1}+r_{C2})L_{m2}} & \frac{r_{C1}\|r_{C2}}{2L_{m2}}(2D-1) & -\frac{r_{C1}\|r_{C2}}{L_{m2}}
\end{bmatrix}$$

$$B=\begin{bmatrix}\frac{r_{C1}}{a(r_{C1}+r_{C2})(L_1+L_{lk1})}D & \frac{r_{C2}}{a(r_{C1}+r_{C2})(L_2+L_{lk2})}D & 0 & \frac{1}{(r_{C1}+r_{C2})C_1} & \frac{1}{(r_{C1}+r_{C2})C_2} & \frac{r_{C1}}{(r_{C1}+r_{C2})L_{m1}}D & \frac{r_{C2}}{2(r_{C1}+r_{C2})L_{m2}}\end{bmatrix}^T$$

$$C=\begin{bmatrix}
\frac{Rr_C}{R+r_C} & \frac{Rr_C}{R+r_C} & \frac{R}{R+r_C} & 0 & 0 & 0 & 0\\
\frac{1}{a}D & 0 & 0 & 0 & 0 & D & 0\\
0 & \frac{1}{a}D & 0 & 0 & 0 & 0 & D
\end{bmatrix}$$

Where

$$A_{11}=-\frac{r_{L1}+R\,\|\,r_C+\frac{r_{C1}\|r_{C2}}{a^2}}{(L_1+L_{lk1})}D-\frac{r_{L1}+R\,\|\,r_C}{L_1}(1-D);$$

$$A_{12}=-\frac{R\,\|\,r_C}{(L_1+L_{lk1})}D-\frac{R\,\|\,r_C}{L_1}(1-D)+\frac{r_{C1}\|r_{C2}}{a^2(L_1+L_{lk1})}(2D-1);$$

$$A_{13}=-\frac{R}{(R+r_C)(L_1+L_{lk1})}D-\frac{R}{(R+r_C)L_1}(1-D);$$

$$A_{21}=-\frac{R\,\|\,r_C}{(L_2+L_{lk2})}D-\frac{R\,\|\,r_C}{L_2}(1-D)+\frac{r_{C1}\|r_{C2}}{a^2(L_2+L_{lk2})}(2D-1);$$

$$A_{22}=-\frac{r_{L2}+R\,\|\,r_C+\frac{r_{C1}\|r_{C2}}{a^2}}{(L_2+L_{lk2})}D-\frac{r_{L2}+R\,\|\,r_C}{L_2}(1-D);$$

$$A_{23}=-\frac{R}{(R+r_C)(L_2+L_{lk2})}D-\frac{R}{(R+r_C)L_2}(1-D);$$

Step-3: Determination of the linear small-signal state-space equations.

Consider the input duty cycle (d), input voltage (V_{in}) are varying around their quiescent operating points D and V_{in}, as $d=D+\hat{d}$; $v_{in}=V_{in}+\hat{v_{in}}$ respectively. These time varying inputs produce perturbations in the dynamic variables $x=X+\hat{x}$ and $y=Y+\hat{y}$ which contain DC,

linear and non-linear terms. The effect of the non-linear terms will be small on the overall response and hence may be neglected as perturbations in input voltage (V_{in}) is small. Therefore, linear small-signal state-space equations can be obtained as given in equation(2.31).

$$\frac{d}{dt}\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\\ \hat{v}_C\\ \hat{v}_{C1}\\ \hat{v}_{C2}\\ \hat{i}_{m1}\\ \hat{i}_{m2}\end{bmatrix}=\begin{bmatrix}a_{11}&a_{12}&a_{13}&a_{14}&a_{15}&a_{16}&a_{17}\\ a_{21}&a_{22}&a_{23}&a_{24}&a_{25}&a_{26}&a_{27}\\ a_{31}&a_{32}&a_{33}&a_{34}&a_{35}&a_{36}&a_{37}\\ a_{41}&a_{42}&a_{43}&a_{44}&a_{45}&a_{46}&a_{47}\\ a_{51}&a_{52}&a_{53}&a_{54}&a_{55}&a_{56}&a_{57}\\ a_{61}&a_{62}&a_{63}&a_{64}&a_{65}&a_{66}&a_{67}\\ a_{71}&a_{72}&a_{73}&a_{74}&a_{75}&a_{76}&a_{77}\end{bmatrix}\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\\ \hat{v}_C\\ \hat{v}_{C1}\\ \hat{v}_{C2}\\ \hat{i}_{m1}\\ \hat{i}_{m2}\end{bmatrix}+\begin{bmatrix}\frac{r_{C1}}{a(r_{C1}+r_{C2})(L_1+L_{lk1})}D\\ \frac{r_{C2}}{a(r_{C1}+r_{C2})(L_2+L_{lk2})}D\\ 0\\ \frac{1}{(r_{C1}+r_{C2})C_1}\\ \frac{1}{(r_{C1}+r_{C2})C_2}\\ \frac{r_{C1}}{(r_{C1}+r_{C2})L_{m1}}\\ \frac{r_{C2}}{(r_{C1}+r_{C2})L_{m2}}\end{bmatrix}\hat{v}_{in}+\begin{bmatrix}d_1\\ d_2\\ d_3\\ d_4\\ d_5\\ d_6\\ d_7\end{bmatrix}\hat{d} \tag{2.31}$$

$$\begin{bmatrix}\hat{v}_0\\ \hat{i}_{p1}\\ \hat{i}_{p2}\end{bmatrix}=\begin{bmatrix}R\,||\,r_C & R\,||\,r_C & \frac{R}{R+r_C} & 0 & 0 & 0 & 0\\ \frac{1}{a}D & 0 & 0 & 0 & 0 & D & 0\\ 0 & \frac{1}{a}D & 0 & 0 & 0 & 0 & D\end{bmatrix}\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\\ \hat{v}_C\\ \hat{v}_{C1}\\ \hat{v}_{C2}\\ \hat{i}_{m1}\\ \hat{i}_{m2}\end{bmatrix}+\begin{bmatrix}0\\ \frac{1}{a}I_{L1}+I_{m1}\\ \frac{1}{a}I_{L2}+I_{m2}\end{bmatrix}\hat{d} \tag{2.32}$$

where,

$$a_{11}=-\frac{r_{L1}+R\,||\,r_C+\frac{r_{C1}\,||\,r_{C2}}{a^2}}{(L_1+L_{lk1})}D-\frac{r_{L1}+R\,||\,r_C}{L_1}(1-D)\;;\; a_{12}=-\frac{R\,||\,r_C}{(L_1+L_{lk1})}D-\frac{R\,||\,r_C}{L_1}(1-D)+\frac{r_{C1}\,||\,r_{C2}}{a^2(L_1+L_{lk1})}(2D-1);$$

$$a_{13}=-\frac{R}{(R+r_C)(L_1+L_{lk1})}D-\frac{R}{(R+r_C)L_1}(1-D)\;;\; a_{14}=\frac{r_{C2}}{a(r_{C1}+r_{C2})(L_1+L_{lk1})}D;$$

$$a_{15}=-\frac{r_{C1}}{a(r_{C1}+r_{C2})(L_1+L_{lk1})}D;a_{16}=-\frac{r_{C1}\,||\,r_{C2}}{a(L_1+L_{lk1})}D\;;\; a_{17}=\frac{r_{C1}\,||\,r_{C2}}{a(L_1+L_{lk1})}(2D-1);$$

$$a_{21}=-\frac{R\,||\,r_C}{(L_2+L_{lk2})}D-\frac{R\,||\,r_C}{L_2}(1-D)+\frac{r_{C1}\,||\,r_{C2}}{a^2(L_2+L_{lk2})}(2D-1);\; a_{22}=-\frac{r_{L2}+R\,||\,r_C+\frac{r_{C1}\,||\,r_{C2}}{a^2}}{(L_2+L_{lk2})}D-\frac{r_{L2}+R\,||\,r_C}{L_2}(1-D);$$

$$a_{23}=-\frac{R}{(R+r_C)(L_2+L_{lk2})}D-\frac{R}{(R+r_C)L_2}(1-D);a_{24}=-\frac{r_{C2}}{a(r_{C1}+r_{C2})(L_2+L_{lk2})}D;\; a_{25}=\frac{r_{C1}}{a(r_{C1}+r_{C2})(L_2+L_{lk2})}D;$$

$$a_{26}=\frac{r_{C1}\,||\,r_{C2}}{a(L_2+L_{lk2})}(2D-1)\;a_{27}=-\frac{r_{C1}\,||\,r_{C2}}{a(L_2+L_{lk2})}D;\; a_{31}=a_{32}=\frac{R}{(R+r_C)C};\; a_{33}=-\frac{1}{(R+r_C)C};$$

$$a_{41}=-a_{42}=-\frac{r_{C2}}{a(r_{C1}+r_{C2})C_1}D;\ a_{43}=0;a_{44}=a_{45}=-\frac{1}{(r_{C1}+r_{C2})C_1};\ a_{46}=-a_{47}=-\frac{r_{C2}}{(r_{C1}+r_{C2})C_1}D;$$

$$a_{51}=-a_{52}=\frac{r_{C1}}{a(r_{C1}+r_{C2})C_2}D;\ a_{53}=0;\ a_{54}=a_{55}=-\frac{1}{(r_{C1}+r_{C2})C_2};\ a_{56}=-a_{57}=\frac{r_{C1}}{(r_{C1}+r_{C2})C_2}D;$$

$$a_{61}=-\frac{r_{C1}\,||\,r_{C2}}{aL_{m1}};\ a_{62}=\frac{r_{C1}\,||\,r_{C2}}{aL_{m1}}(2D-1);\qquad a_{63}=0;\ a_{64}=\frac{r_{C2}}{(r_{C1}+r_{C2})L_{m1}}D;\ a_{65}=-\frac{r_{C1}}{(r_{C1}+r_{C2})L_{m1}}D;$$

$$a_{66}=-\frac{r_{C1}\,||\,r_{C2}}{L_{m1}}D;\ a_{67}=\frac{r_{C1}\,||\,r_{C2}}{L_{m1}}(2D-1);a_{71}=\frac{r_{C1}\,||\,r_{C2}}{2aL_{m2}}(2D-1);\ a_{72}=-\frac{r_{C1}\,||\,r_{C2}}{2aL_{m2}};\ a_{73}=0;$$

$$a_{74}=-\frac{r_{C2}}{2(r_{C1}+r_{C2})L_{m2}};\ a_{75}=\frac{r_{C1}}{2(r_{C1}+r_{C2})L_{m2}};a_{76}=\frac{r_{C1}\,||\,r_{C2}}{2L_{m2}}(2D-1);\ a_{77}=-\frac{r_{C1}\,||\,r_{C2}}{2L_{m2}};$$

$$d_1=\left\{-\frac{r_{L1}+R\,||\,r_C+\frac{r_{C1}\,||\,r_{C2}}{a^2}}{(L_1+L_{lk1})}+\frac{r_{L1}+R\,||\,r_C}{L_1}\right\}I_{L1}+\left\{-\frac{R\,||\,r_C}{(L_1+L_{lk1})}+\frac{R\,||\,r_C}{L_1}+2\frac{r_{C1}\,||\,r_{C2}}{a^2(L_1+L_{lk1})}\right\}I_{L2}+\left\{-\frac{R}{(R+r_C)(L_1+L_{lk1})}+\frac{R}{(R+r_C)L_1}\right\}V_C$$
$$+\frac{r_{C2}}{a(r_{C1}+r_{C2})(L_1+L_{lk1})}V_{C1}-\frac{r_{C1}}{a(r_{C1}+r_{C2})(L_1+L_{lk1})}V_{C2}-\frac{r_{C1}\,||\,r_{C2}}{a(L_1+L_{lk1})}I_{m1}+2\frac{r_{C1}\,||\,r_{C2}}{a(L_1+L_{lk1})}I_{m2}+\frac{r_{C1}}{a(r_{C1}+r_{C2})(L_1+L_{lk1})}V_{in}$$

$$d_2=\left\{-\frac{R\,||\,r_C}{(L_2+L_{lk2})}+\frac{R\,||\,r_C}{L_2}+2\frac{r_{C1}\,||\,r_{C2}}{a^2(L_2+L_{lk2})}\right\}I_{L1}+\left\{-\frac{r_{L2}+R\,||\,r_C+\frac{r_{C1}\,||\,r_{C2}}{a^2}}{(L_2+L_{lk2})}+\frac{r_{L2}+R\,||\,r_C}{L_2}\right\}I_{L2}+\left\{-\frac{R}{(R+r_C)(L_2+L_{lk2})}+\frac{R}{(R+r_C)L_2}\right\}V_C$$
$$-\frac{r_{C2}}{a(r_{C1}+r_{C2})(L_2+L_{lk2})}V_{C1}-\frac{r_{C1}}{a(r_{C1}+r_{C2})(L_2+L_{lk2})}V_{C2}-2\frac{r_{C1}\,||\,r_{C2}}{a(L_2+L_{lk2})}I_{m1}-\frac{r_{C1}\,||\,r_{C2}}{a(L_2+L_{lk2})}I_{m2}+\frac{r_{C2}}{a(r_{C1}+r_{C2})(L_2+L_{lk2})}V_{in}$$

$$d_3=0\ \ d_4=\frac{r_{C2}}{(r_{C1}+r_{C2})C_1}\left(-\frac{1}{a}I_{L1}+\frac{1}{a}I_{L2}-I_{m1}+I_{m2}\right);d_5=\frac{r_{C1}}{a(r_{C1}+r_{C2})C_2}\left(\frac{1}{a}I_{L1}-\frac{1}{a}I_{L2}+I_{m1}-I_{m2}\right);$$

$$d_6=2\frac{r_{C1}\,||\,r_{C2}}{aL_{m1}}I_{L2}+\frac{r_{C2}}{(r_{C1}+r_{C2})L_{m1}}V_{C1}-\frac{r_{C1}}{(r_{C1}+r_{C2})L_{m1}}V_{C2}-\frac{r_{C1}\,||\,r_{C2}}{L_{m1}}I_{m1}+2\frac{r_{C1}\,||\,r_{C2}}{L_{m1}}I_{m2};$$

$$d_7=\frac{r_{C1}\,||\,r_{C2}}{aL_{m2}}I_{L1}+\frac{r_{C1}\,||\,r_{C2}}{L_{m2}}I_{m1};$$

The mathematical model of linearized small signal model of ISOP converter is presented in matrix form which contains parasitic elements of circuits such as r_{C1}, r_{C2} & r_C effective series resistances of input and output capacitor, r_{L1} filter inductor resistance and leakage , magnetizing inductance of the transformer $(L_{lk1}, L_{lk2}, L_{m1}, L_{m2})$. In summary, the nonlinear averaged equations of switching converter can be linearized about quiescent operating point and nonlinear terms are neglected because of sufficiently small as variations in magnitude. Therefore, the obtained small –signal ac model of the converter has certain limitations:

The accurate modelling of practical system having more nonlinear components are more complex and hence, neglecting higher order terms to linearized model results in undesired response.

Step-4: Derivation of open loop transfer functions.

Taking Laplace Transform of equation(2.31) and equation(2.32) and after simplification, the output voltage $V_o(s)$ can be obtained.

$$V_o(s)=\frac{R\{r_C(s-a_{33})-a_{31}\}\left[\begin{array}{l}\{(a_{14}+a_{24})s+(a_{12}-a_{11})a_{24}\}V_{C1}(s)+\{(a_{15}+a_{25})s+(a_{12}-a_{11})a_{25}\}V_{C2}(s)\\+\dfrac{D}{a(r_{C1}+r_{C2})}\left\{\dfrac{r_{C1}s}{(L_1+L_{lk1})}+\dfrac{r_{C2}(s-a_{11}+a_{12}}{(L_2+L_{lk2})}\right\}V_{in}+\{(d_1+d_2)s+(a_{12}-a_{11})d_2\}d(s)\end{array}\right]}{(R+r_C)\left[(s-a_{33})\{(s-a_{11})(s-a_{21})-a_{12}a_{21}\}-a_{31}\{(a_{13}+a_{23})s+(a_{12}-a_{11})a_{23}\}\right]} \quad (2.33)$$

$$V_o(s)=\frac{R\{r_C(s-a_{33})-a_{31}\}\left[\begin{array}{l}\{(a_{14}+a_{24})s+(a_{12}-a_{11})a_{24}\}V_{C1}(s)+\{(a_{15}+a_{25})s+(a_{12}-a_{11})a_{25}\}V_{C2}(s)\\+\dfrac{D}{a(r_{C1}+r_{C2})}\left\{\dfrac{r_{C1}s}{(L_1+L_{lk1})}+\dfrac{r_{C2}(s-a_{11}+a_{12}}{(L_2+L_{lk2})}\right\}V_{in}+\{(d_1+d_2)s+(a_{12}-a_{11})d_2\}d(s)\end{array}\right]}{(R+r_C)\left[(s-a_{33})\{(s-a_{11})(s-a_{21})-a_{12}a_{21}\}-a_{31}\{(a_{13}+a_{23})s+(a_{12}-a_{11})a_{23}\}\right]} \quad (2.34)$$

Substituting initial conditions in equation(2.34), the open loop transfers can be obtained as given below:

$$G_{voc1}(s)=\left.\frac{V_o(s)}{V_{C1}(s)}\right|_{V_{C2}(s)=0,V_{in}(s)=0,d(s)=0}=\frac{R\{r_C(s-a_{33})-a_{31}\}\{(a_{14}+a_{24})s+(a_{12}-a_{11})a_{24}\}}{(R+r_C)\left[(s-a_{33})\{(s-a_{11})(s-a_{21})-a_{12}a_{21}\}-a_{31}\{(a_{13}+a_{23})s+(a_{12}-a_{11})a_{23}\}\right]}$$

$$G_{voc2}(s)=\left.\frac{V_o(s)}{V_{C2}(s)}\right|_{V_{C1}(s)=0,V_{in}(s)=0,d(s)=0}=\frac{R\{r_C(s-a_{33})-a_{31}\}\{(a_{15}+a_{25})s+(a_{12}-a_{11})a_{25}\}}{(R+r_C)\left[(s-a_{33})\{(s-a_{11})(s-a_{21})-a_{12}a_{21}\}-a_{31}\{(a_{13}+a_{23})s+(a_{12}-a_{11})a_{23}\}\right]}$$

$$G_{vod}(s)=\left.\frac{V_o(s)}{d(s)}\right|_{V_{C1}(s)=0,V_{C2}(s)=0,V_{in}(s)=0}=\frac{R\{r_C(s-a_{33})-a_{31}\}\{(d_1+d_2)s+(a_{12}-a_{11})d_2\}}{(R+r_C)\left[(s-a_{33})\{(s-a_{11})(s-a_{21})-a_{12}a_{21}\}-a_{31}\{(a_{13}+a_{23})s+(a_{12}-a_{11})a_{23}\}\right]}$$

Similarly, the open loop transfer function of current controller $G_{cc1d}(s)=\left.\frac{I_{L1}(s)}{d(s)}\right|$, $G_{cc2d}(s)=\left.\frac{I_{L2}(s)}{d(s)}\right|$ with initial conditions $V_{C1}(s)=0$, $V_{C2}(s)=0$, $V_{in}(s)=0$ can be derived.

Fig. 2.8 shows system block diagram comprises of two inner current loops and outer voltage control loop. The voltage loop controller is designed for narrow bandwidth and slow dynamics whereas the inner current loop has wide bandwidth and fast dynamics and therefore, in the voltage loop design, the inner current loop dynamics can be neglected. The inner current control loop consists of two PI controllers and two modulators having the same frequency (25 kHz) and amplitude but phase shifted by 180^o. Therefore, design of the control loops are given separately.

Fig. 2.9 gives the bode plot of the voltage control loop and current control loop of uncompensated and compensated system with PI controller. Beyond corner frequency, in the lower frequency range where the impedance of output capacitor (C) is much greater than its effective series resistance (ESR), the only effective impedance is that of output capacitor only. In this frequency range, the gain falls similar to gain without ESR as shown in Fig. 2.9(a). At higher frequencies, where the impedance of output capacitor (C), is less than its ESR, the effective impedance is that of its ESR only. Hence in that frequency range the gain curve falls with different slope than that of without ESR as shown in Fig. 2.9(a). The

transition of slope of gain curve with ESR is mainly dependent on ESR of output capacitor. The phase margin (PM) of 45^0 is achieved at the desired crossover frequency of 5 kHz using proper tuning of controller and compensation network, thus, low frequency gain is improved.

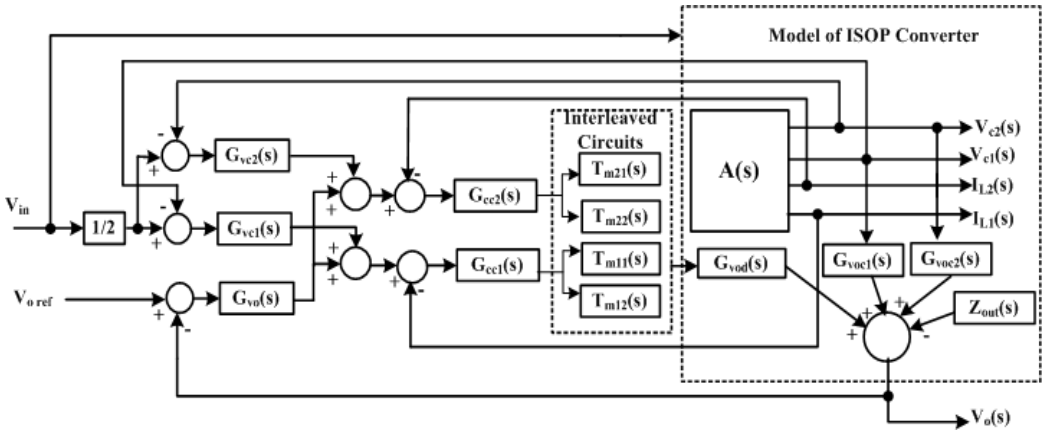
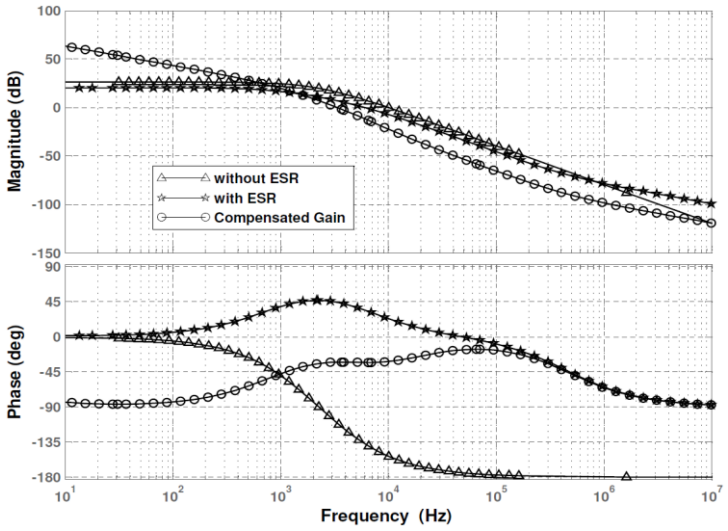
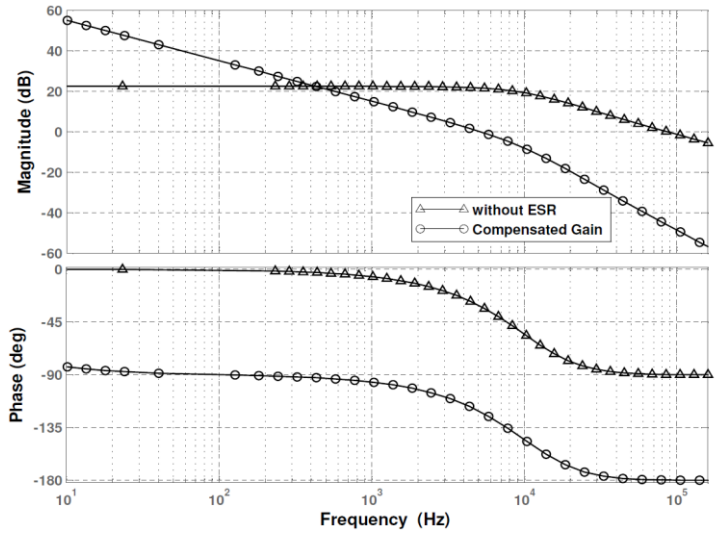


Fig. 2.8 System block diagram of ISOP converter with IVS and OCS control strategy.



(a)



(b)

Fig. 2.9 Bode plot of uncompensated and compensated control loop (a) Output voltage control loop (b) Current control loop

2.6 System Modeling

A Simulink model of proposed ISOP power converter is developed with Simulink and SimPowerSystem™ of MATLAB software which consists of two modules of push-pull converters with identical specifications as given in Table 2.3. These modules are connected in series at input side and in parallel at load side as illustrated Fig.2.2. The input source is modeled with controlled DC voltage source where its output voltage is controlled by step signal. System parameters like currents through different parts of circuit and input & output voltage are measured.

A simulink block of the control system that ensures equal input-voltages and load current sharing between two converters is shown in Fig. 2.10. The proposed control method consists of multi feedback loops through which closed loop controls are accomplished to regulated the output voltage against disturbances in input voltage and/or in the load current. In addition, feedback systems are stable. As shown in Fig. 2.10, the actual output voltage is compared with reference voltage and error signal is processed through PI controller (PI_1). PI Controllers (PI_2, PI_3) are used to control equal input voltage between two converter modules. In order to deliver equal load current by converters, the inner feedback loop consisting of PI controllers (PI_4, PI_5) are implemented. The control voltage obtained from PI controllers (PI_4, PI_5) are fed to phase-shift circuit to generate control signals for power switches $(S_{11}, S_{12}, S_{21} \& S_{22})$.

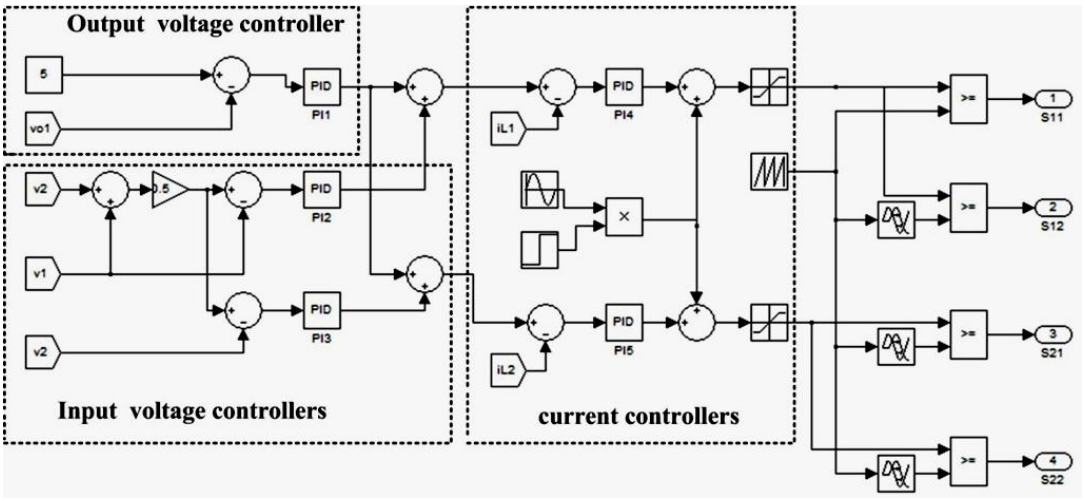


Fig. 2.10 Simulink model of controller for ISOP converter

To obtain the open loop frequency response of converter, the time domain simulation is performed with sinusoidal signal of various frequencies ranging from 10 Hz to 10MHz. This signal is added into duty cycle $d(t)$ at summing junction of PI controllers (PI_4, PI_5) output as shown in Fig. 2.10, such that $d(t) = D + D_m \sin \omega_m t$; where D_m are constants, $|D_m| \ll D$, and ω_m modulating frequency. The Fast Fourier Transformation technique is applied to extract the

fundamental frequency components (magnitude and phase). Subsequently, a single frequency response of V_o/d (*gain* and *phase* response) is stored. This process repeats for the various frequency range (10Hz to 10MHz).

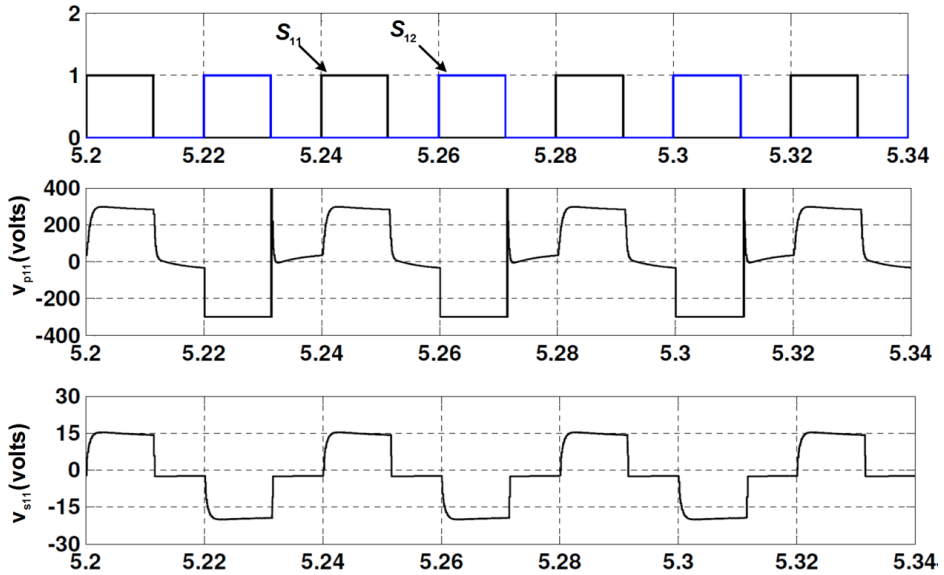
Table 2.3 Specification of each power modules

Particulars	Specification
DC input voltage (V_{in})	$300V \pm 10\%$
Output power (V_o, I_o)	$5V, 100A$
Centre-tapped high frequency transformer	$1-\phi, 250VA, 25kHz, 300V / 20V,$ $r_p = 0.5\Omega, r_s = 0.1\Omega, L_{lkp} = L_{lkp} = 10\mu H,$ $L_{lks1} = L_{lks2} = 0.2\mu H, R_m = 50\Omega, L_m = 250\mu H$
Output filter inductor $(L_1 = L_2, r_{L1} = r_{L2})$	$15\mu H, 25m\Omega$
Output capacitor (C, r_C)	$660\mu F, 10m\Omega$
Input capacitor $(C_1 = C_2, r_{C1} = r_{C2})$	$4 * 660\mu F, 10m\Omega$
Output voltage ripple, $\Delta v_o / v_o$	0.5%
Switching Frequency, f_{sw}	$25kHz$

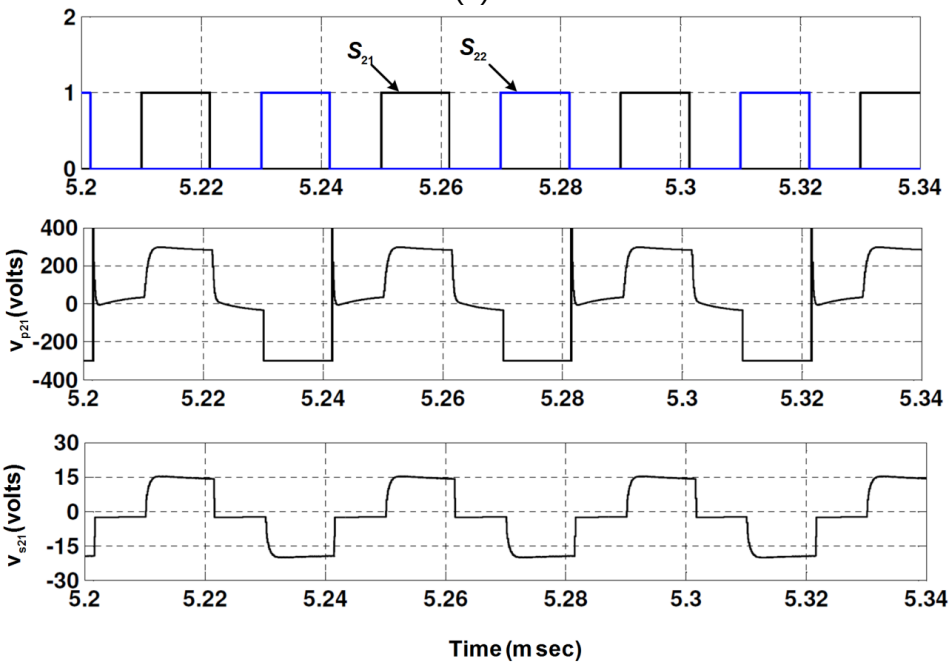
2.7 Simulation Results and Discussion

To investigate the performances of proposed ISOP connected DC-DC converter with interleaved PWM control, extensive simulation studies are carried out with specifications given in Table 2.3. The entire system is modelled in MATLAB/ Simulink environment using power system block set. The modelled system is studied for input voltage and load current sharing, effect of parastics component of converter under various operating conditions and some of the results are discussed below.

Fig.2.11 shows the voltage waveforms appear across primary and secondary windings of transformer for modue-1 and module-2. It is observed that the large spike in voltages are due to transformer leakage drop at the instant of switching OFF of power switches and this spike is severe for higher value of leakage inductance as shown in Fig.2.12. Leakage inductance also limits the rate of reversal of current in the primary and secondary circuit. Higher value of leakage inductance means more energy is available to discharge the device output capacitance and snubber capacitance. Furthermore, it was observed that secondary voltages of transformer are zero for certain duration, which indicates output filter inductor of concerned module freewheel though its rectifier diodes.



(a)



(b)

Fig.2.11 Switching pulse, primary and secondary windings voltage waveforms

(a) module-1 (b) module-2

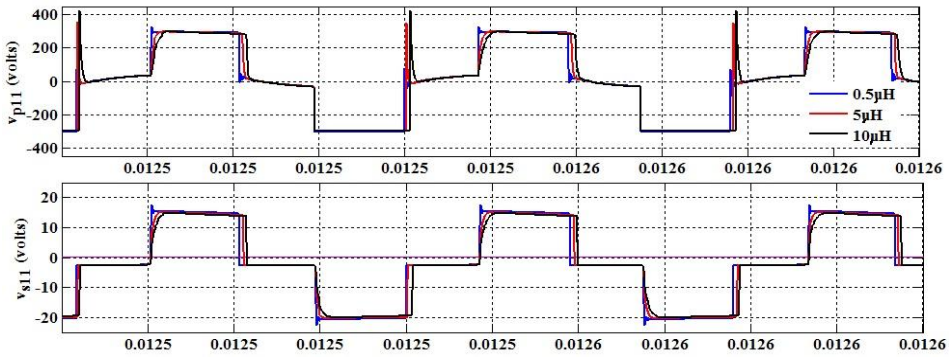


Fig.2.12 Primary & secondary voltages of module-1 indicating the effect of leakage inductance

Fig. 2.13 shows the waveforms of input currents (i_{p1}, i_{p2}) of two converter modules. It is observed that average value of both currents are equal whereas their instantaneous values are phase-shifted due to interleave operation. Therefore, source current (i_{in}) becomes constant and ripple-free.

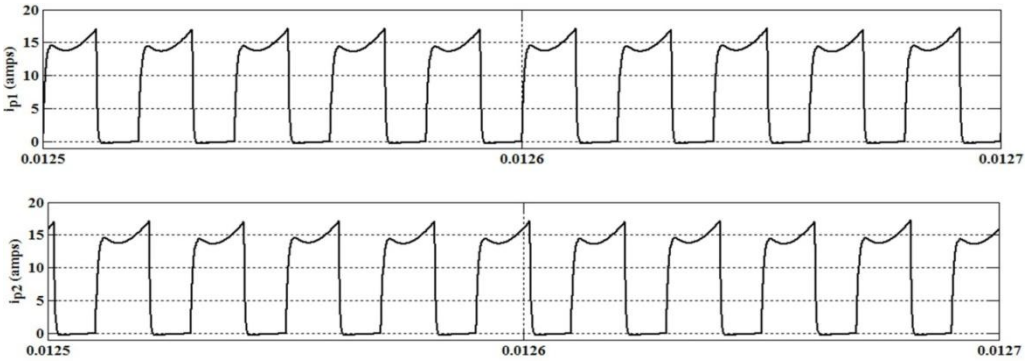


Fig. 2.13 Input current waveforms of each module

Fig. 2.14 shows steady state voltage and current waveform of output filter inductors which share equal current i.e half of the loads current. Due to interleaved operation, the load current contains lesser ripple as compare to individual inductor ripple current. It is observed in Fig. 2.14 that output inductor current (i_{L1}, i_{L2}) share equal current during input voltage and load current variations.

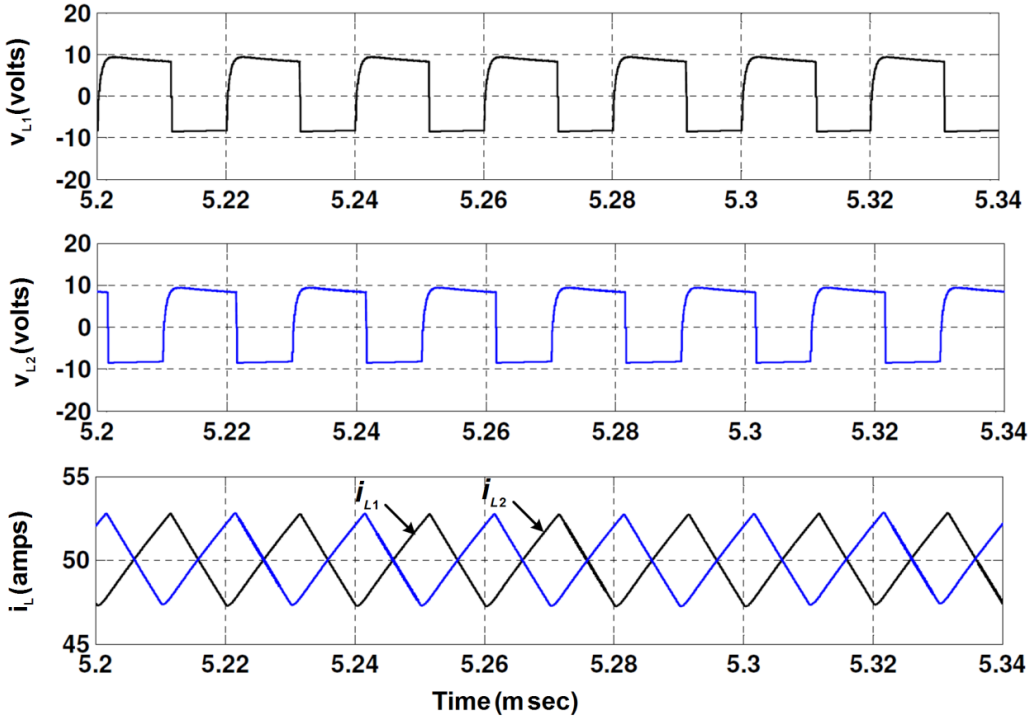


Fig. 2.14 Voltage and current waveforms of output filter inductor

Fig. 2.15 shows steady state waveform of rectifier diodes currents $(i_{D11}, i_{D12}, i_{D21} \& i_{D22})$. It is observed that each module delivers power through individual rectifier diode follow by freewheeling period. During freewheeling period, both rectifier diodes of same module are conducting . Therefore, average value of rectifier diode current is reduced significantly, thus there is significant reduction of heat dissipation in secondary side. In all these waveforms, duty cycle of power switches is adjusted by controller to keep output terminal voltage constant against input voltage and load variations.

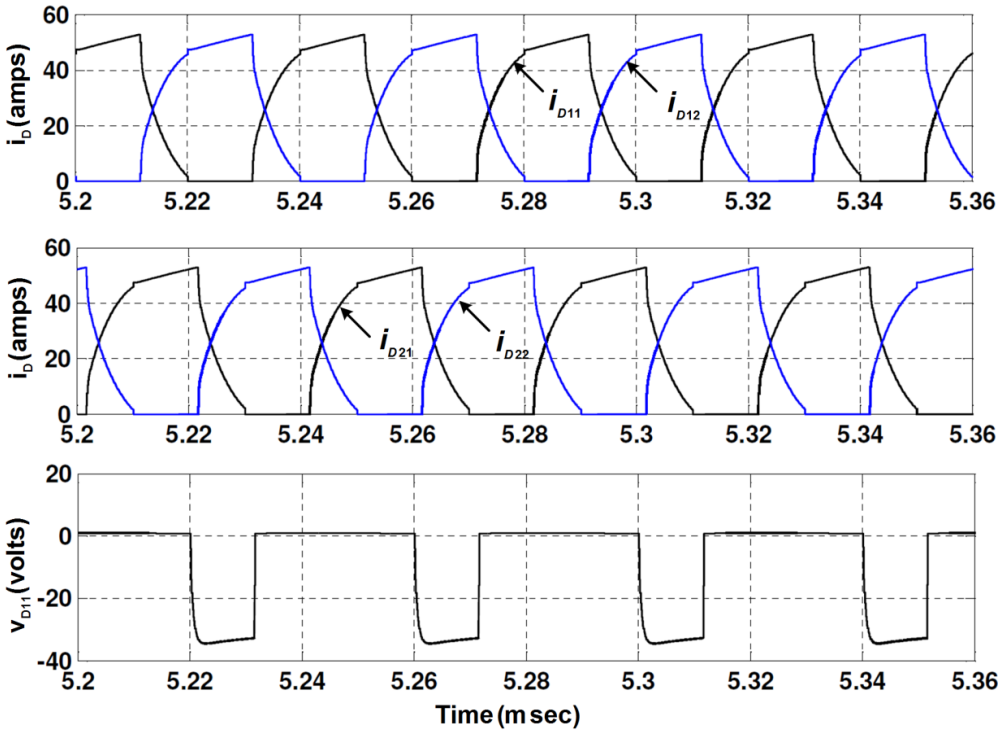


Fig. 2.15 Current and voltage waveforms of rectifier diodes

To study the dynamic behaviour of converter against input voltage sudden change in input voltage from 600V to 450V at $t = 8m$sec and 450V to 550V at $t = 18m$sec is made and it is observed that output voltage remains unchanged irrespective of these variations. Further to investigate performance of converter with load variations, load from full load of 100A to 80A at $t = 12m$sec and 80A to 90A at $t = 20m$sec are introduced and response against these variations is observed in Fig. 2.16. The output inductor current sharing against aforementioned input voltage and load variations also depicted in Fig. 2.17 and it has been observed that under all operating conditions inductor current shares equal current.

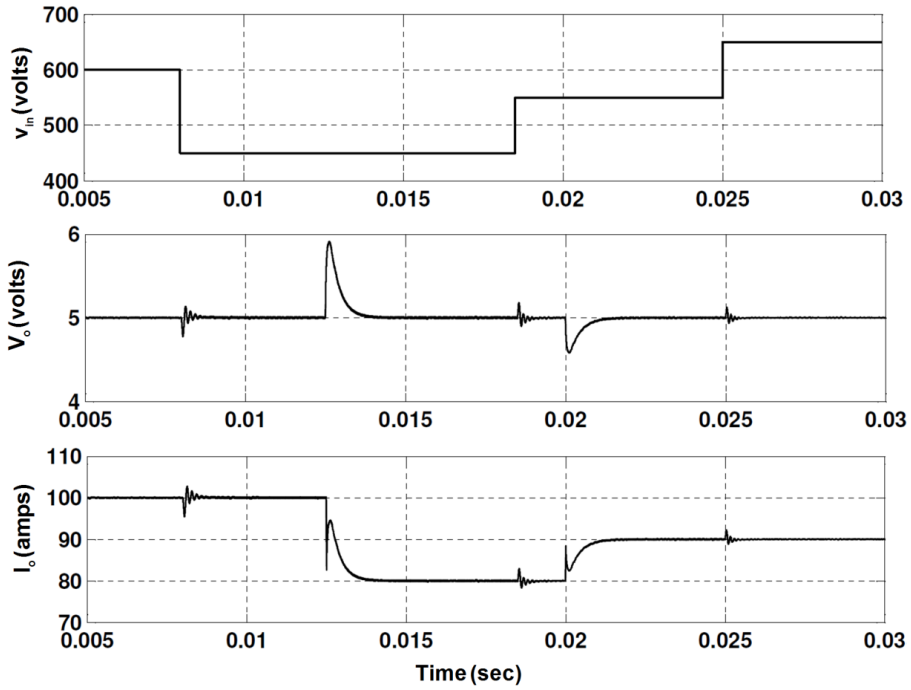


Fig. 2.16 Transient response of converter under different operating conditions (voltage decreased from 600V to 450V DC at 8 msec, load decreased from 100A to 80A at 0.0125 sec, voltage increased from 450V to 550V DC at 18msec and load increased from 80A to 90A at 0.02 sec)

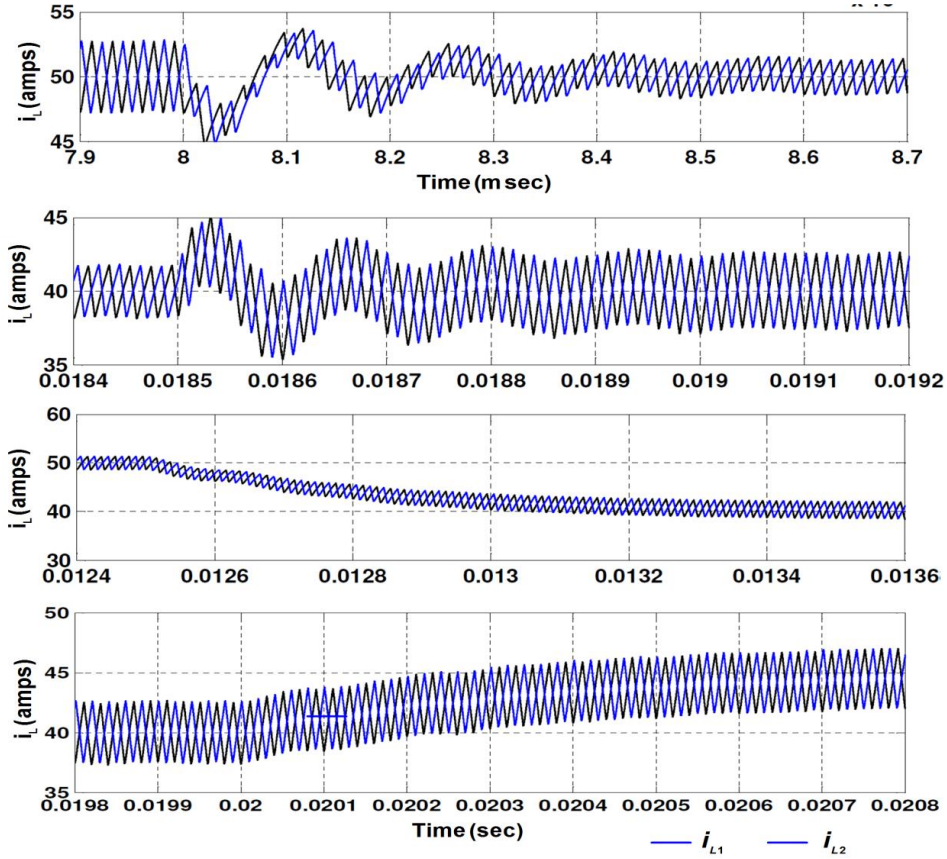


Fig. 2.17 Output inductor currents during various operating conditions of Fig.2.16

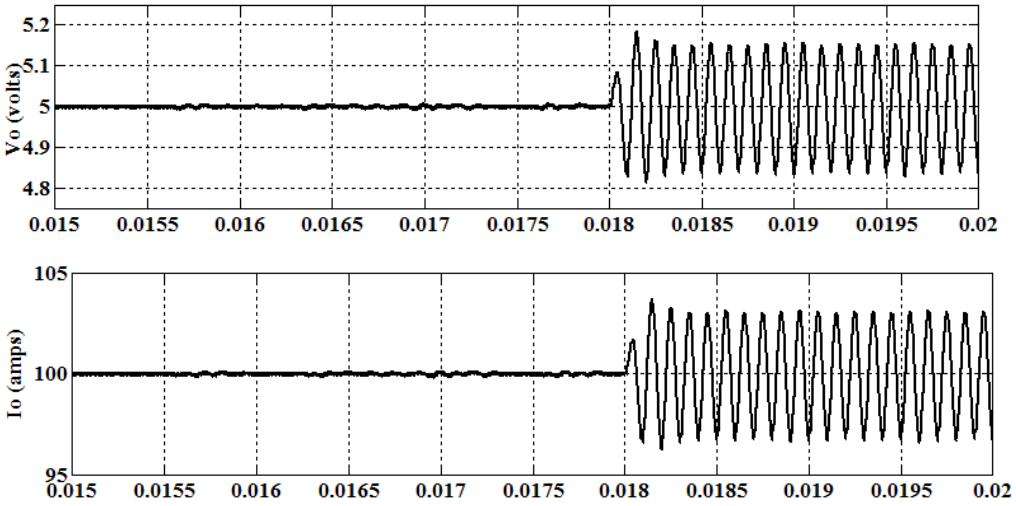
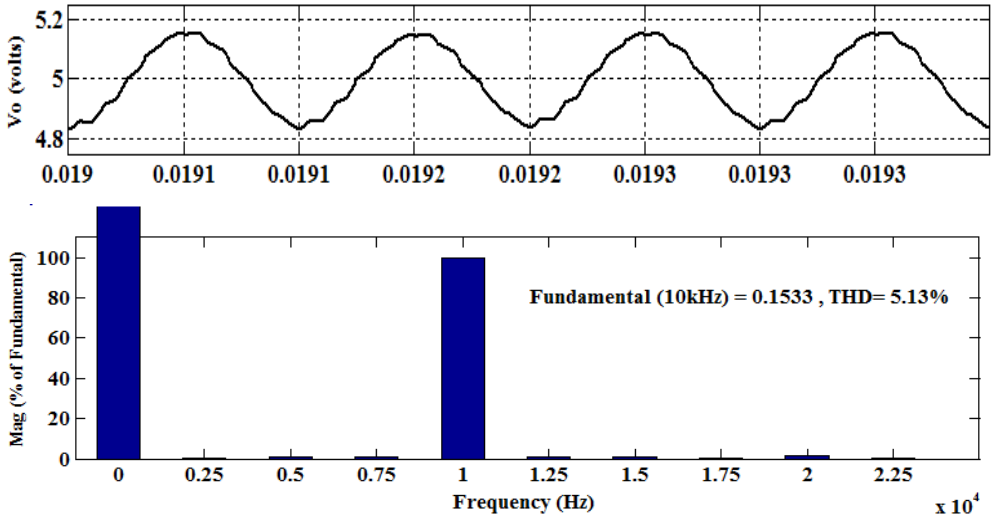
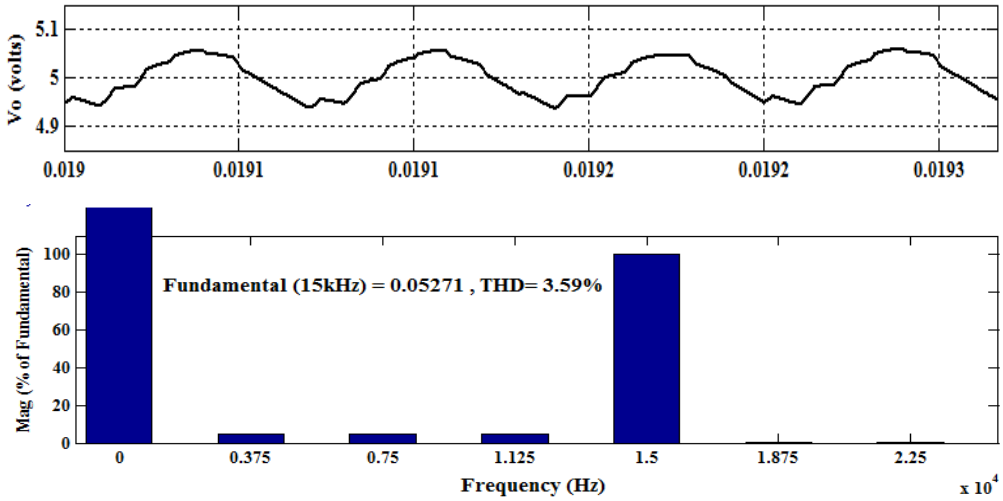


Fig. 2.18 Load voltage & current waveforms with small ac perturbation in duty cycle of 10kHz at 0.18 sec



(a) 10kHz



(b) 15kHz

Fig. 2.19 Output voltage waveform and its FFT under perturbed condition in duty cycle of (a) 10kHz (b) 15kHz

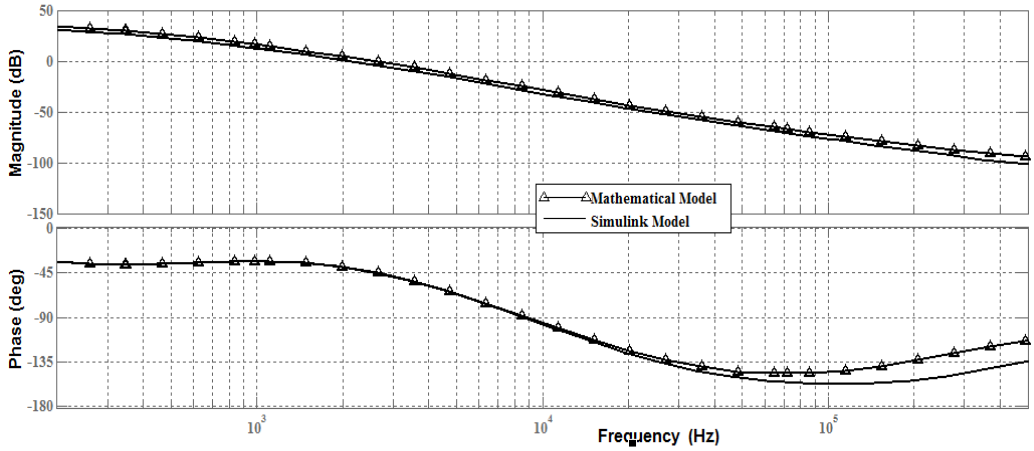


Fig. 2.20 Bode plot of converter controller

A small perturbation in duty cycle of different frequency is introduced and its effect on output voltage is observed as shown in Fig. 2.18. Additionally FFT analysis of output voltage is carried out as shown in Fig. 2.19. To validate the derived mathematical model with Simulink model, frequency response of loop gain and phase are plotted and it is found almost identical as illustrated in Fig. 2.20.

2.8 Conclusion

In this chapter, modular approach for designing LVHC power supply using inter-connection of multiple converters, particularly ISOP connected modules is studied. The multi-feedback loops is used to control the output voltage against various disturbances. The interleaved control technique is adopted to control switches of proposed converter. A mathematical modelling of ISOP connected two modules of Push Pull converter including all parasitic elements are carried out under steady-state and dynamic-state. A Simulink model of two push-pull converters with ISOP connection is developed using SimPower System™. The simulation results are presented for both steady–state and transient conditions with input voltage and load variations. Furthermore, small ac perturbation in duty cycle at different frequencies was injected to study frequency response. From the FFT analysis of output voltage, it is found that voltage contains a low frequency component at modulating frequency.

This approach offers several features such as high efficiency, low devices voltage/current stress, and low cost for low voltage high current applications. For high power applications, a large number of small rating modules are to be connected in ISOP connection and to ensure equal power sharing, several controllers are to be employed. Therefore, on account of more number of components, controllers, system reliability decreases and furthermore design of controllers becomes complex.

[This chapter presents the design of system hardware for prototype models of three-phase LLC resonant DC-DC power converter, multi-phase high frequency isolated DC-DC converter with multi-phase rectifications. The system hardware comprises of power circuit, control circuit and measurement circuits. A dSPACE-DS1104 is used for implementation of the control circuit and real-time generation of control pulses for all the power switches of the converter.]

3.1 Introduction

To validate the simulation results, the downscaled prototype models of the following are developed for experimentation:

- Three-phase LLC resonant DC-DC power converter.
- Multi-phase high frequency isolated DC-DC converter with multi-phase rectifications.
- Six-phase version of multi-phase high frequency DC-DC converter with multi-phase rectification.

A three-phase LLC resonant DC-DC power converter of Fig.1.26 and a three-phase high frequency isolated DC-DC converter with three-phase rectification of Fig. 1.27, both rated at 75 W, 1.5V/50A, as well as a six–phase version of multi-phase high frequency DC-DC converter with multi-phase rectification as shown in Fig.1.28, rated for 150 W, 5 V/100A, are designed and developed to validate its viability and effectiveness to LVHC applications. In order to implement the control algorithum, the DC output voltage is sensed and then compared with a reference value. The error signal is processed through PI controller. The output of PI controller is fed to Phase-Shift PWM block through saturation block as shown in Fig. 3.1. The Phase-Shift PWM block is used to generate switching pulses by implementation of symmetrical and asymmetrical control scheme. These switching pulses are fed to switching devices of front end converter through proper isolation and amplification. A Digital Signal Processor (DSP) DS1104 of dSPACE is used for the real time simulation and implementation of these control algorithum.

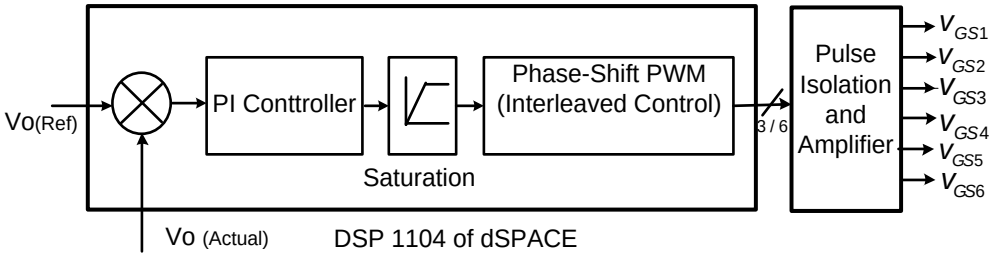


Fig. 3.1 Schematic diagram of realization of control scheme

The system hardware of above topologies is developed mainly in three stages:

- Development of power circuit,
- Development of control circuit,
- Measurements of system parameters,

3.2 Development of power circuit

In general, the power circuits of above mentioned topologies include front end converter, high frequency transformer and load end converter. The development of these parts are discussed in the following subsection.

3.2.1 Design of Front End Converter

The power circuit of front end converter consists of six self-commutated semi-conductor switches $(S_1 - S_6)$ with anti-parallel diodes and RC series circuit as shown in Fig. 3.2. These switches can be practically realized using power transistors, MOSFETs and IGBTs based on the rating of the converter. In the prototype models developed in the laboratory, six power MOSFETs, IRF460A (20A, 500A, 0.27Ω), are used as switching devices. A suitably designed snubber circuit is connected across each device for its protection and is mounted on a heat sink to ensure proper heat dissipation [68, 69].

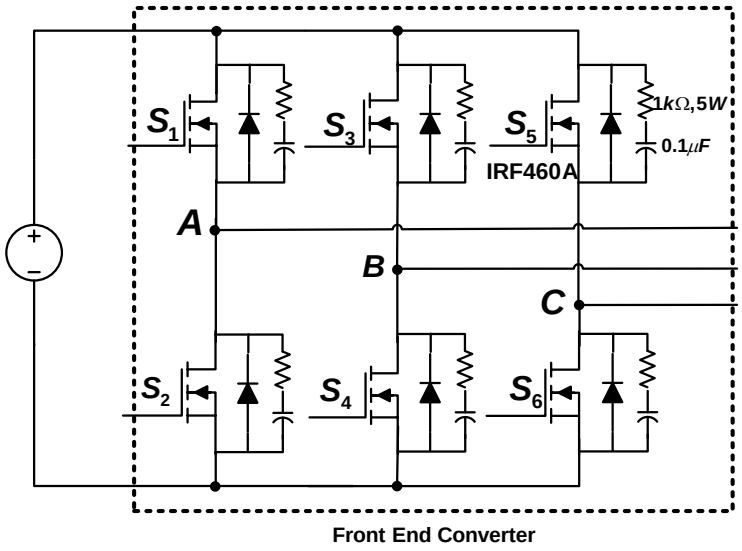


Fig. 3.2: Power circuit of front end converter

3.2.2 Design of High Frequency Transformer

In most of the isolated DC-DC converters, high frequency transformer is used to provide electrical isolation, voltages scaling, and reduction of switch stresses. Two units of three-phase transformers for developing multi-phase high frequency isolated DC-DC converter with multi-phase rectification are used. Further, three units of single-phase transformer with centre-tapped secondary windings for three-phase LLC resonant DC-DC

power converter are used. For practical implementation, three units of single-phase transformers are used due to easy availability of ferrite core, flexible connection and simple design. In this section, single-phase high frequency two windings transformer and single-phase high frequency transformer with centre-tapped secondary windings are designed and developed. The value of apparent power handling by transformer may vary by a factor ranging from 2 to 2.828 times of input power, depending upon the type of circuit in which the transformer is employed [70,71].

These transformers are fabricated using EE65 ferrite core, primary winding of 209 turns with 19 SWG Cu wire and secondary windings of 12-12 turns with 17 SWG Cu-wire. The leakage inductance and magnetizing inductance of transformer are expressed in terms of inductances (L_p, L_s). Practically, the values of L_p and L_s can be measured on primary side keeping secondary side winding open circuited and short circuited respectively. Thus measurement of inductances (L_p, L_s) for designed and developed single phase high frequency transformer (Fig.A.3) is carried out. Further desired values of L_p and L_s can be achieved by providing suitable air-gap length between magnetic core. The measured values of L_p and L_s with respect to various air-gap length are depicted in Table 3.1.

Table 3.1 Measured values of L_p, L_s for developed transformer

Air-Gap Length *(mm)*	Primary side Inductance	
	$L_p\,(mH)$	$L_s\,(mH)$
0.054	*26.76*	*2.754*
0.048	***29.51***	***2.812***
0.036	*36.44*	*2.854*
0.024	*45.98*	*2.891*
0.018	*62.00*	*3.013*
No gap	*304.2*	*3.102*

The polarlity test on fabricated transformers is conducted to identify the polarity of windings as shown in Fig. 3.3. Using dotted terminal of each transformer, the winding connections for three-phase high frequency transformer is made as shown in Fig. 3.4. The polarity test of single-phase transformer with centre-tapped secondary winding is also conducted. The voltage waveforms of primary & secondary winding are shown in Fig. 3.5. The winding connections of transformer for three-phase LLC resonant DC-DC power converter is shown in Fig. 3.6.

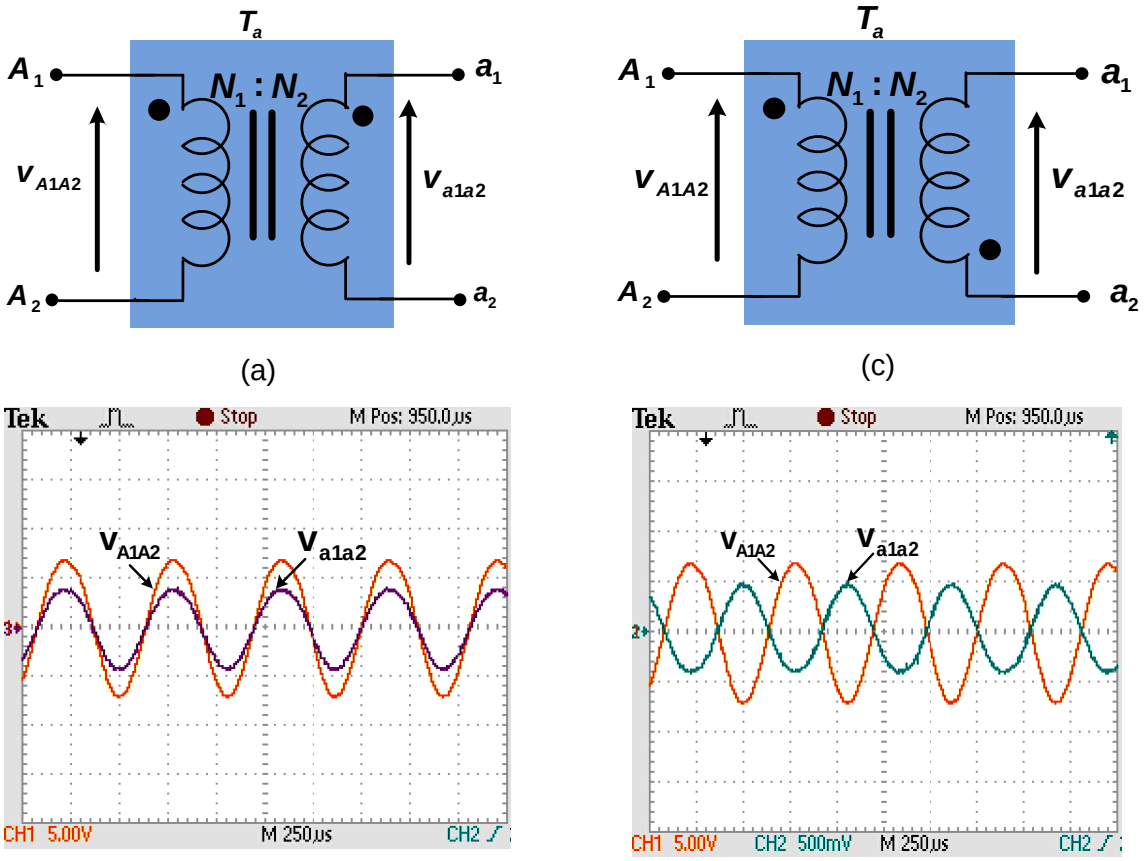


Fig. 3.3 Polarity test of two winding transformer (a) & (c) Single-phase transformer indicating polarity (b) Primary and secondary voltage waveforms of Fig. 3.4(a) (d) Primary and secondary voltage waveforms of Fig. 3.4(a)

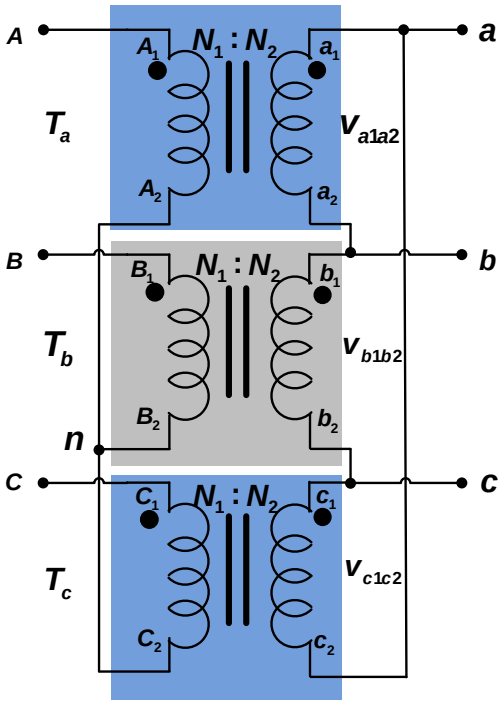
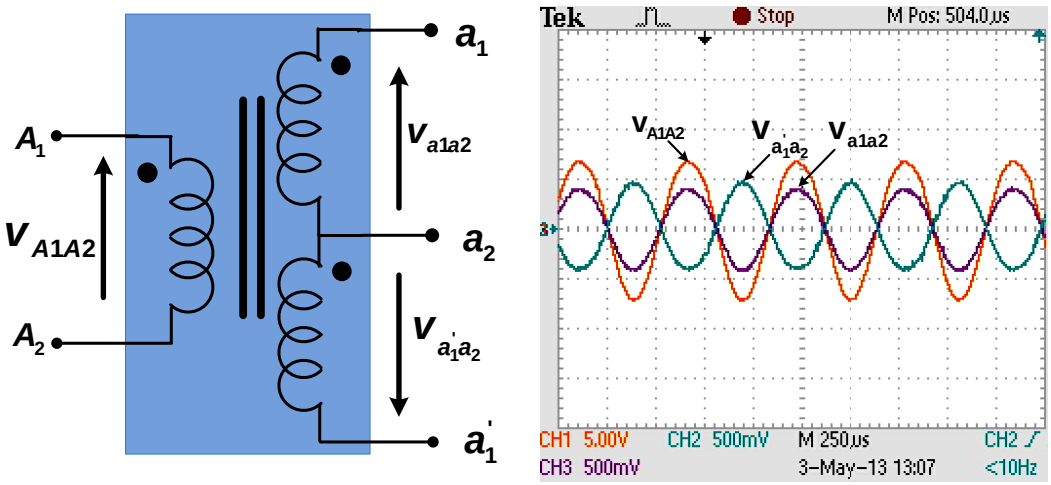


Fig. 3.4 Three-phase high frequency transformer



(a) (b)

Fig. 3.5 Polarity test of transformer with centre-tapped secondary winding transformer (a) Single-phase transformer indicating polarity (b) Primary and secondary voltage waveforms

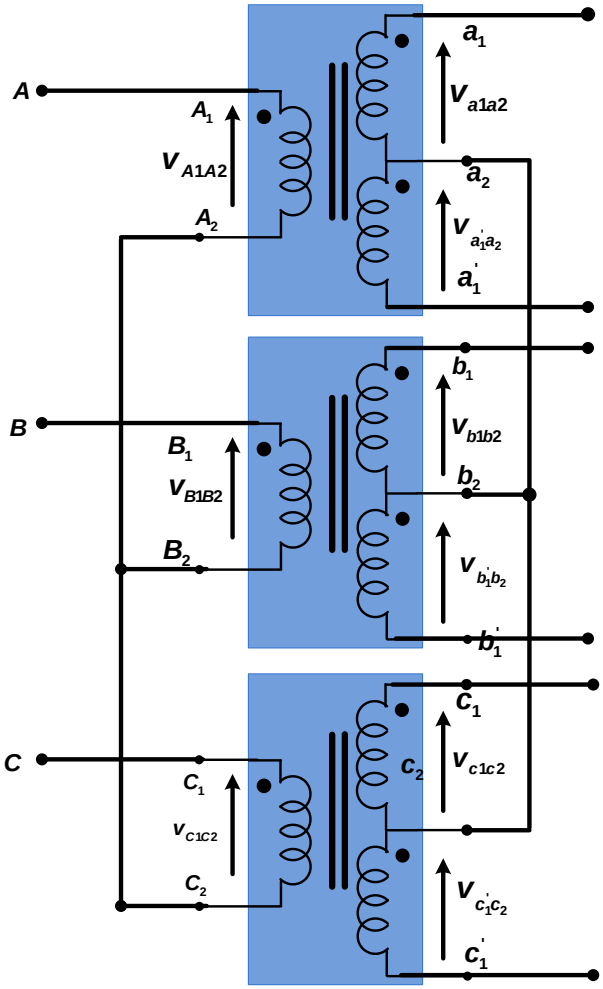


Fig. 3.6 Transformer connections for three-phase LLC resonant DC-DC resonant converter

3.3 Development of Control Circuit

The control algorithm is designed and built in MATLAB/Simulink software and the control pulses for six MOSFETs of front end converter are generated by real-time simulation using the DS-1104 of dSPACE. In case of symmetrical control method, All the control pulses for six MOSFETs are generated using DS-1104 of dSPACE, whereas in asymmetrical control methods, only three control pulses are generated using dSPACE and remaining three are complementary of generated pulses. In fact, the optimized C-code of the Simulink model of control algorithm is generated with the help of Real-Time Workshop of MATLAB. The Real-Time Workshop (RTW) of MATLAB and the Real-Time Interface (RTI) of dSPACE result in the real-time simulation of the model. The control pulses are generated at the various Master–bit I/Os of the dSPACE which are interfaced with the MOSFETs driver circuits through isolation boards. This ensures the necessary isolation of the dSPACE hardware from the power circuit which is necessary for its protection.

3.3.1 MOSFET Driver Circuits

The MOSFET driver circuits are used for pulse amplification and isolation purposes. The control pulses generated from dSPACE unit are not efficient to drive the switching devices. Thus, these signals are further amplified by using proper amplifier circuit. Fig.3.7 shows circuit diagram of pulse isolation and amplifier circuit for MOSFET driver circuit. For isolation between power circuit and control circuit, an opto-isolator (MCT2E) is used. Although common +5V, regulated DC power supply may be used at input side of opto-coupler, but individual regulated DC power supplies of +12V is used to connect output side of opto-coupler. In order to test the MOSFET driver, a PWM signal is applied at point ‘a’ of Fig.3.7 (a) and waveforms at different points (b, c and d) are recorded as shown in Fig.3.7 (b). It is observed that waveform of point ‘d’ is similar to PWM signal applied at point ‘a’, but it’s amplitude is increased to 12V which is used to drive the MOSFET. An identical circuit is used for each device.

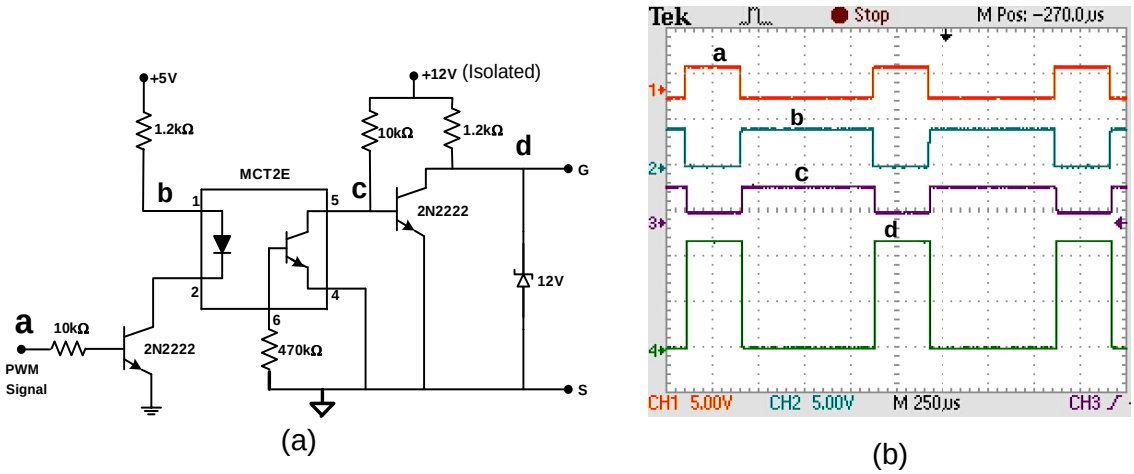
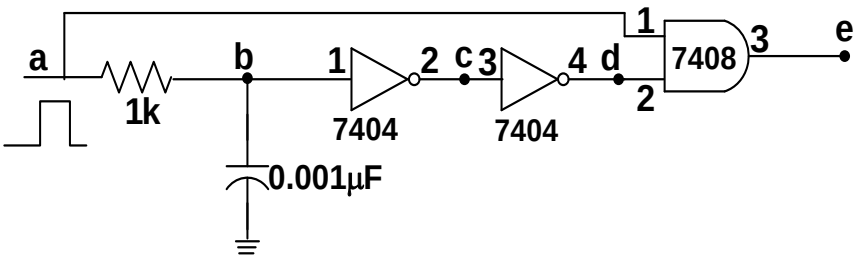


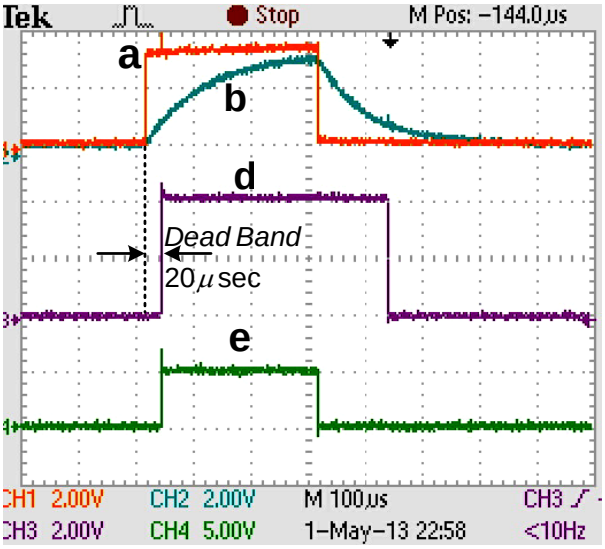
Fig.3.7 Pulse isolation & amplifier circuit (a) Circuit diagram (b) Waveforms at different points

3.3.2 Dead-Band Circuit

A dead-band circuit is used to provide finite time delay between two switching signals for switches of the same leg of front end converter topology when they are operated in a complementary manner. This circuit is required to avoid direct short circuit between two terminals of the input DC source which occurs due to simultaneous conduction of switches of same leg. The time delay between switching pulses of same leg is introduced with a R-C circuit and logic gates as shown in Fig.3.8(a). An identical dead-band circuit is used for each leg of front end topology of converter when it is operated under asymmetrical control method. Test waveforms recorded at different of circuit is shown in Fig.3.8(b).



(a)



(b)

Fig.3.8 Dead band circuit (a) Circuit diagram (b) Waveforms at different points

3.3.3 DS1104 DSP (dSPACE) hardware board

The DSP DS1104 R&D Controller Board of dSPACE is a standard board that can be plugged into Peripheral Component Interconnect (PCI) slot of a desktop computer. The DS1104 is specifically designed for the development of high-speed multivariable digital controllers and real-time simulations in various fields. It is a complete real-time control system based on an AMD optern™ processor running at 2.6 GHz. For advanced I/O purposes, the board includes a slave-DSP subsystem based on the TMS320F240 DSP

microcontroller. For the purposes of rapid control prototyping (RCP), specific interface connectors and connector panels provide easy access to all input and output signals of the board. Thus, the DS1104 R&D Controller Board is very good hardware for the dSPACE prototype development system for cost-sensitive RCP applications. It is used for the real-time simulation and implementation of the control algorithm in real-time.

In real-time simulation, the real plant (converter) is controlled by the controller (PI) that is simulated in real time. The sensed voltages and currents are fed to the dSPACE board via the available ADC channels on its connector panel. In order to add an I/O block (like ADCs and master bit I/Os in this case) to the simulink model, the required block is dragged from the dSPACE I/O library and dropped into the simulink model of the controller.

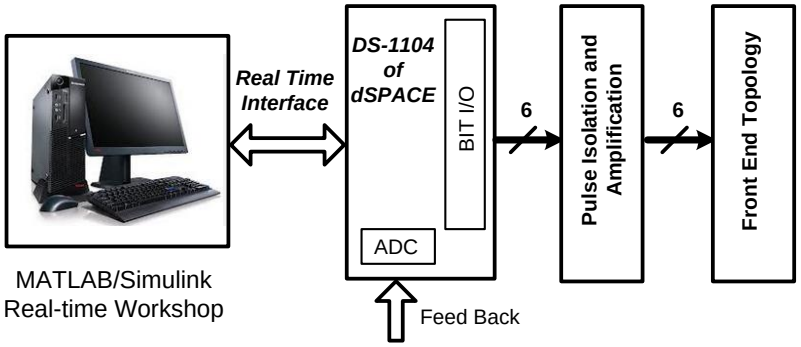


Fig. 3.9 DSP (dSPACE-DS1106) circuit board interface

In fact, adding a dSPACE I/O block to a simulink model is almost like adding any simulink block to the model. Depending on the number of signals to be taken out, the master bit I/Os, configured in the output mode, are connected to the model. In addition, ADCs are connected to the model for inputting the feedback voltage signals. These sensed signals are used for processing in the designed control algorithm. Because real-time simulation is such a vital aspect for control engineering, the same is true for the automatic generation of real-time code, which can be implemented on the hardware. For dSPACE systems, Real-Time Interface (RTI) carries out this linking function. Together with Real-Time Workshop from the Mathworks, it automatically generates the real-time code from simulink models and implements this code on dSPACE real-time hardware. This saves the time and effort twice as there is no need to manually convert the simulink model into another language such as C and one need not to be concerned about a real-time program frame and I/O function calls, or about implementing and downloading the code onto the dSPACE hardware. RTI carries out these steps and we just need to add the required dSPACE blocks (I/O interfaces, etc.) to our simulink model. In other words, RTI is the interface between Simulink and various dSPACE platforms. It is basically the implementation software for single-board hardware and connects the simulink control model to the I/O of the board. In the present case, the optimized C-code of the simulink model of control algorithm is automatically generated by the Real-Time Workshop of MATLAB in conjunction with dSPACE Real-Time Interface (RTI). The

generated code is then automatically downloaded into the dSPACE hardware where it is implemented in real-time and the gating pulses are generated. The gating pulses for the power switches of converter are outputted via the master-bit I/Os available on the dSPACE board. The CLP1104 Connector/LED Combi panel provides easy-to-use connections between DS1104 board and the devices to be connected to it. The panel also provides an array of LEDs indicating the states of digital signals (gating pulses). The gating pulses are fed to various MOSFET driver circuits via the opto-isolation circuit boards. Fig. 3.9 shows the schematic of the dSPACE (DS1104) board interfaced with the Host PC and the real-world plant. Sensed signals are fed to the ADCs and generated gating pulses are outputted at master bit I/Os.

3.4 Measurements of System Parameters

For accurate and reliable operation of a system in closed loop, the measurement of various system parameters and their conditioning is required, which must fulfill the following requirements-

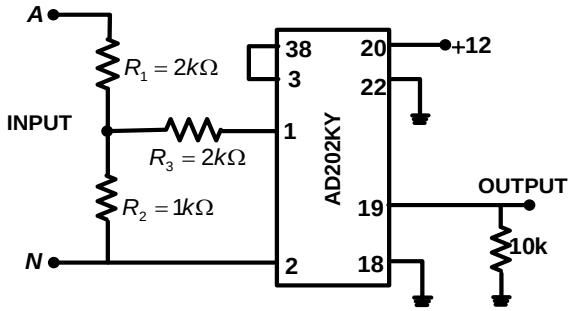
- High accuracy,
- Galvanic isolation between high and low voltage side,
- Ease of installation and operation,
- Linearity and fast response, etc.

With the availability of Hall-effect current sensors(TELCON HTP 25) and isolation amplifiers(AD202KY), these requirements are fulfilled to a greater extent. In order to implement the control algorithm in the closed loop operation of converters, the output DC voltage is sensed and for processing and signal conditioning low pass filter is designed. Thus, for measurement of various circuit parameters, voltage and current sensors are designed as discussed below:

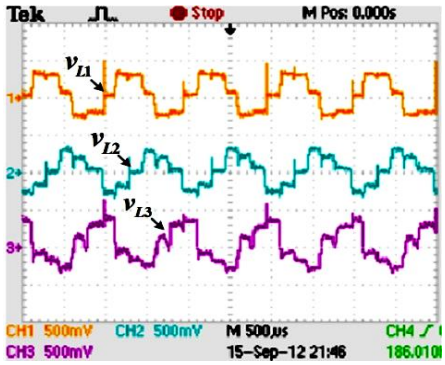
3.4.1 Voltage Sensing

The actual output voltage is to be sensed and made available for comparison at voltage controller. This voltage is sensed using an isolation amplifier (AD202KY). It is a general-purpose, two-port, transformer-coupled isolation amplifier used to measure the voltages and transmits the same for processing without a galvanic connection between input and output stages of the isolation amplifier through the use of internal transformer coupling. The other main features of the isolation amplifier are a bipolar ±5V output range, an adjustable gain range from 1 V/V to 100 V/V, ±0.025% maximum nonlinearity, 130dB of CMR and lower power consumption. This voltage sensor can sense voltages in the range of ±1000V (peak). Fig. 3.10(a) shows the circuit diagram for the voltage sensing scheme, using an AD202 KY isolation amplifier.

The voltage to be sensed is applied between the terminals A and N (across a voltage divider comprising of R_1 and R_2) and the voltage input to the sensor is available at the pins 1 and 2 via a resistance R_3. The isolated sensed voltage is available at the output terminal 19. The output of voltage sensor is scaled properly to meet the requirement of the control and is fed to the dSPACE via its ADC channel for further processing. It requires a nominal supply voltage range of ±12V to ±15V. Fig. 3.10(b) shows the response of sensed voltages.



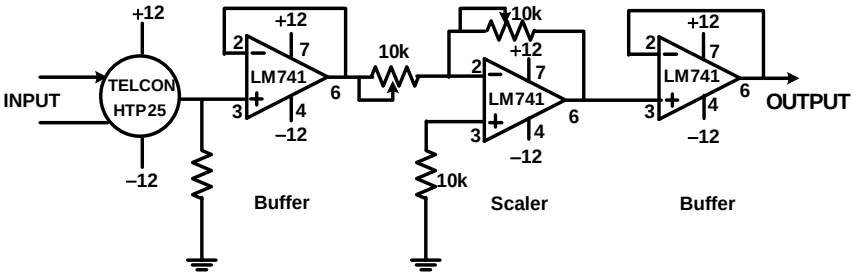
(a)



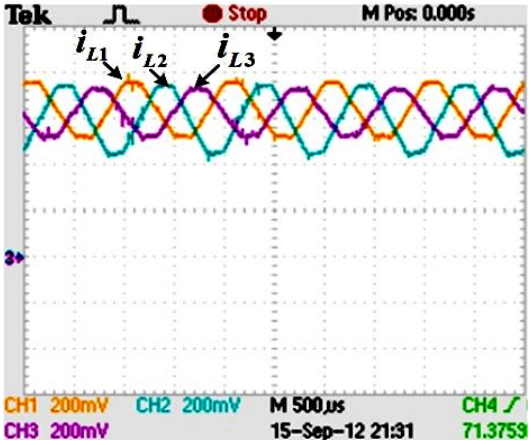
$(v_{L1}, v_{L2} \& v_{L3} : 5V/div, X-axis : 500\mu s/div)$

(b)

Fig. 3.10 (a) Voltage sensing circuit (b) Sensed voltage waveforms $(v_{L1}, v_{L2} \& v_{L3})$



(a)



$(i_{L1}, i_{L2} \& i_{L3} : 3A/div, X-axis : 500\,\mu s/div)$

(b)

Fig. 3.11 (a) Current sensing circuit (b) Sensed current waveforms $(i_{L1}, i_{L2} \& i_{L3})$

3.4.2 Current Sensing

The AC and DC currents are sensed using the PCB-mounted Hall-effect current transformer type sensor (TELCON HTP 25) suitable for measuring current upto 25A. These current sensors provide the galvanic isolation, ease of assembly, high reliability and require a nominal supply voltage of the range ±12V to ±15V DC. It has a transformation ratio of 1000:1 and hence its output is scaled properly to obtain the desired value to meet the control requirements. The circuit diagram of the current sensing scheme for AC and DC measurements is shown in Fig. 3.11(a). The response of current sensors is shown in Fig. 3.11(b). It is observed that waveform of inductor currents are phase shifted by 120^0. The inductor current (i_{L2}) is of higher value as compared to i_{L1} & i_{L3}, because of unequal scaling of current sensor. This error is corrected by adjusting the scaler at later stage.

3.5 Conclusion

In this chapter, the design and development of system hardware for prototype model of three-phase LLC resonant DC-DC converter and multi-phase high frequency isolated DC-DC converter are given. The main points of this chapter include the following:

- The front end converter of prototype models of three-phase LLC resonant DC-DC power converter and multi-phase high frequency isolated DC-DC converter with multi-phase rectifications are developed using six power MOSFETs with anti-parallel diodes and RC series circuit.
- Single-phase high frequency transformer is designed and developed and its leakage and magnetizing inductance are determined with different air-gaps.
- The polarity test on manufactured transformers are conducted and winding connection of the three-phase transformer is carried out.
- Test waveforms of different points of MOSFET driver circuit, dead band circuit are presented.
- Voltage and current sensing circuits are designed for measurement of various circuit parameters.

CHAPTER 4: THREE-PHASE LLC RESONANT DC-DC POWER CONVERTER WITH CENTRE-TAPPED TRANSFORMER

[This chapter deals with high-frequency isolated three-phase LLC resonant DC-DC converter suitable for medium power applications which demand high current at low output voltage, isolation, good regulation against load and line disturbances, and fast dynamic response. The modeling, control and design of proposed converter are carried out under symmetrical control with fixed frequency operation and its steady state analysis has been presented according to the description of the operational stages of the converter. Mathematical modeling of LLC resonant tank network is carried out and its design curves are plotted against variation of normalized frequency for different value of the load. In order to investigate the performance, the simulation study in carried out using the SimPowerSystems™ and Simulink toolbox of MATLAB software. Based on mathematical analysis, a 1.5V/ 50A prototype model is built and tested under various operating condition.]

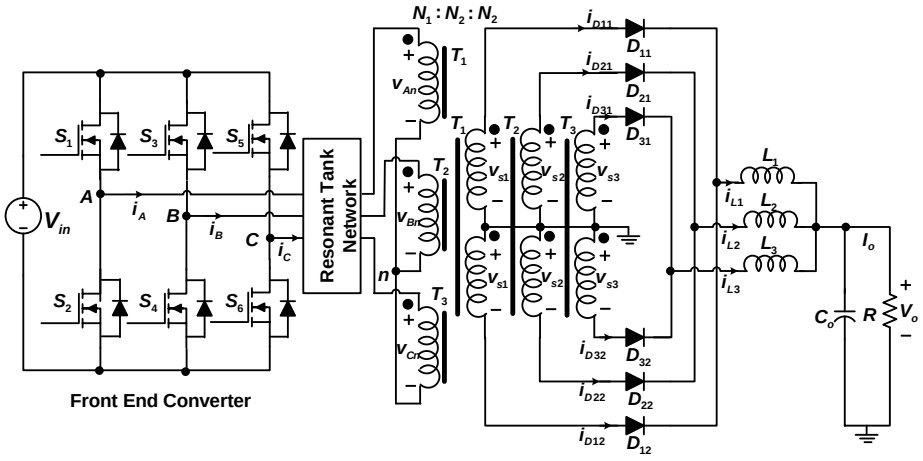
4.1 Introduction

The increasing demand of DC power supply in various electronics equipments such as data processing and telecommunication equipment, and to comply the issues like losses, device stresses, thermal heat management, size & weight and safety, the isolated DC-DC converters are widely used. Most of these converters, are rated upto few kWs and single-phase high frequency transformer is employed for isolation and voltage scaling [Prasad, 1988#255][72-78]. Due to increase in usages of internet, advances in telecommunication and high-speed data computing systems, the need of high power at low DC voltage has been increased. In view of LVHC applications, single-phase half bridge resonant DC-DC converter has several merits but face severe components stresses when employed for medium and high power applications. Therefore, as an alternative, three-phase high frequency isolated converter is proposed. It consists of three units of half bridge DC-DC converter and operated with interleaved control techniques. It offers following advantages over existing converter:

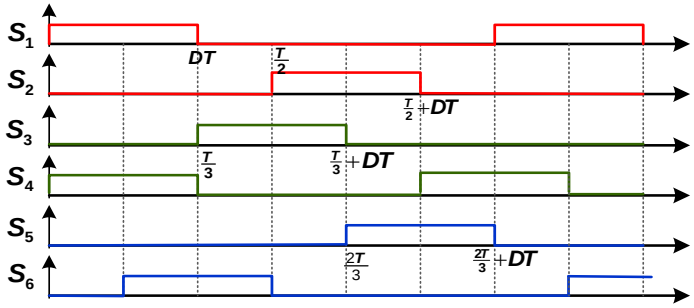
- Increase in frequency of input current and output voltage ripple due to interleaved operation.
- Lower RMS current through the switches of front end converter i.e higher power transfer for the same switch current and voltage stresses.
- Reduction in size of reactive (filter) components.
- Better transformer core and winding utilization.

To reduce size and weight of passive components, the proposed converter is operated at high switching frequency. Therefore, switching losses in front end converter of proposed converter become more due to hard switching of devices. The Zero Voltage Switching (ZVS) for switches of front end converter is used to reduce the switching losses. Implementation of

ZVS condition for switches is carried out using resonant tank network. In most of the practical design, the resonant tank network comprises of LC series circuit and shunt inductor. The elements of LLC resonant tank is implemented by making use of snubber capacitance, leakage and magnetizing inductance of the transformer (LLC resonant tank) [79]. The proper values of series and shunt inductor may be implemented by introducing suitable airgap length in magnetic core.



(a)



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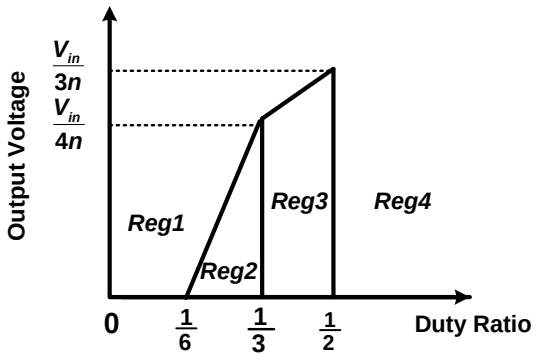


(c)

Fig. 4.1 Three-phase high frequency isolated LLC DC-DC resonant converter
(a) Power Circuit (b) Switching signals for symmetrical control (c) Operating regions

4.2 System Configuration and Control Scheme

4.2.1 Power Circuit

Fig. 4.1(a) shows the power circuit of three-phase, LLC resonant DC-DC power converter with centre-tapped transformer. It consists of four main parts: front end converter, resonant tank network, high frequency transformers , and load end converter (centre-tapped rectifier stage, output filter). The front end converter of converter is similar to a three-phase full bridge inverter which consists of six power switches $(S_1 - S_6)$ that may be practically realized by MOSFET with body diode and RC snubber depending on rating of converter. The three units of single phase high frequency transformer with centre-tapped secondary windings are used for isolation and scaled down the voltage to an appropriate level. These transformers are configured in Wye connection at primary side and centre-tapped secondary windings with rectifier diodes $(D_{11}, D_{12}, D_{21}, D_{22}, D_{31}, D_{32})$ are connected in parallel to feed energy to load through output filters $(L_1, L_2, L_3 \,\&\, C_o)$. As three single-phase half bridge DC-DC converter are operated in an interleaved manner to share high load current, the switching signals of each converter are 120^0 phase-shifted over a switching period which reduces the ripple in output capacitor due to the ripple cancellation effect as depicted in Fig. 4.1(b). The duty ratio of each switch is restricted to 0.5, to avoid saturation of transformer core and short circuit of source. The output inductors share one third of load current, and hence low value inductors are used to reduce ripples in individual inductor current. The ripples in total current (i_{L1}, i_{L2}, i_{L3}) are reduced significantly using interleaved technique. The suitable configuration of the resonant tank network has been derived without adding external components in circuits. Its function is to pass a fundamental component of current which lags with a fundamental component of resonant tank input voltage over a wide range of load.

4.2.2 Control Strategy

The power switches of front end converter are to be controlled to regulate output DC voltage against disturbances. The variable frequency control method is adopted to regulate the output voltage of the converter by many researchers [80-82]. The main drawback of this technique is the size and magnetic loss of passive components as it is selected on the basis of minimum frequency of operation. On the other hand, fixed frequency phase shift pulse width modulated control is used [13, 32].The proposed converter operates under symmetrical control method with fixed frequency operation, in which duty ratio of the upper group of power switches (S_1, S_3, S_5) in three-phase bridge inverter is same as that of lower group of power switches (S_2, S_4, S_6) as shown in Fig. 4.1(b). The power switches in the same inverter leg operate for same duty ratio and phase shifted by 180^0. The operation of each inverter leg

is same but gating signals are phase shifted by 120^0 to produce balanced high frequency AC voltages for primary windings of the transformer.

In order to control the converter output voltage, the duty ratio of power switches varies which mainly depends on the turn's ratio of transformer, supply voltage and load. Based on duty ratio, whole operating region has been classified in four regions: Reg1$\left(0 \le D \le \frac{1}{6}\right)$, Reg2$\left(\frac{1}{6} \le D \le \frac{1}{3}\right)$, Reg3 $\left(\frac{1}{3} \le D \le \frac{1}{2}\right)$ and Reg4$\left(\frac{1}{2} \le D\right)$ as shown in Fig. 4.1(c). If the converter operates in Reg1, at any instant only one switch turns on which makes incomplete current path in the primary side of transformers and hence, yields zero output voltage. Further operation of converter in Reg4 is prohibited to avoid direct short circuiting of DC voltage. Therefore, allowable regions for converter operation are Reg2 and Reg3. Finally, selection of the turn's ratio of transformer is one of the major factors in deciding the duty ratio of power switches and hence, restricts converter operation in particular operating region. The sequence of power switches of the front end converter in conduction varies with region of operation as tabulated in Table 4.1.

Table 4.1 Operational Table

Mode	Power switches in conduction	
	Reg2	*Reg3*
1	S_4,S_1	S_5,S_4,S_1
2	S_1	S_4,S_1
3	S_1,S_6	S_4,S_1,S_6
4	S_6	S_1,S_6
5	S_6,S_3	S_1,S_6,S_3
6	S_3	S_6,S_3
7	S_3,S_2	S_6,S_3,S_2
8	S_2	S_3,S_2
9	S_2,S_5	S_3,S_2,S_5
10	S_5	S_2,S_5
11	S_5,S_4	S_2,S_5,S_4
12	S_4	S_5,S_4

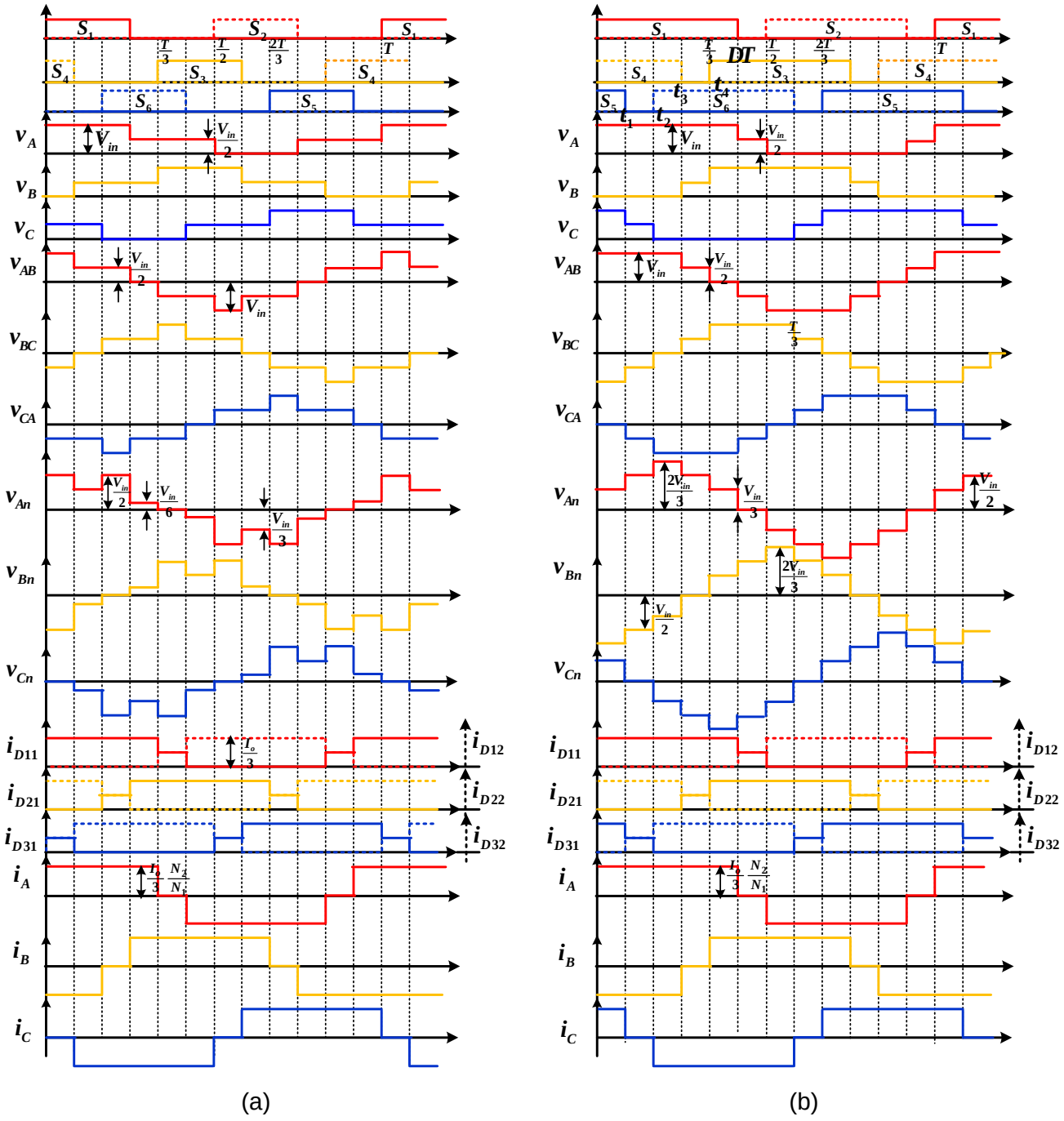


Fig.4.2 Voltage and current waveforms of three-phase LLC resonant DC-DC converter (a) Reg2$\left(\frac{1}{6}\le D\frac{1}{3}\right)$; (b) Reg3$\left(\frac{1}{3}\le D\frac{1}{2}\right)$.

4.3 Operation, Modeling and Analysis of the Converter

The model of the converter needs to be developed for its performance evaluation. To carry out steady state analysis, the following assumptions are made:

- The power switches and passive components are considered to be ideal.
- The input and output DC voltage ripples is negligibly small and hence it is to be considered constant.
- The output inductors are large enough to ensure continuous mode of operation and inductor currents are constant and ripple-free.
- Three-phase circuit is balanced.
- The leakage inductances and magnetizing inductance of high frequency transformer are to be included as a part of resonant tank.

Based on the duty ratio of power switches twelve main operating modes are identified in both regions (Reg2 & Reg3). The operating waveform of key parameters under these regions of operation is shown in Fig.4.2. The converter operations from operating mode-1 to mode-6 are complementary of mode-7 to mode-12 respectively. Thus operating mode-1 to mode-6 of proposed converter has been explained in subsequent section.

4.3.1 Operation of Converter

The steady state operation of the proposed converter with fixed frequency, symmetrically controlled PWM methods, operated in the region (Reg3), is presented. The gate signals require for power switches $(S_1 - S_6)$ of converter in region (Reg3) and operating waveforms of key parameters of three-phase LLC resonant DC-DC converter are shown in Fig.4.2(b). As shown in Fig.4.2(b), switches of each inverter-leg are conducted for equal duration and phase shift of 120^0 between each inverter-leg are provided for interleaved operation. Based on state (ON and OFF) of power switches, the potential of midpoint (v_A, v_B, v_C) of each inverter leg is calculated with respect to the negative terminal of input DC voltage and further, line and phase voltages applied to the primary side of transformers are drawn which are symmetrically phase shifted by 120^0. The detailed operation of the converter (in Reg3) is explained as follows:

(a) Mode-1

In this mode power switches S_1, S_4 and S_5 are ON and remaining switches are OFF. The current paths in the primary and secondary side of the circuit are shown by the bold line in Fig. 4.3(a) and simplified equivalent circuit during mode-1 is shown in Fig. 4.3(b). The voltages appearing across primary and secondary winding of transformers are as follows:

$$v_{AB} = V_{in},\ v_{BC} = -V_{in},\ v_{CA} = 0,\ v_{An} = \tfrac{V_{in}}{3},\ v_{Bn} = -\tfrac{2V_{in}}{3},\ v_{Cn} = \tfrac{V_{in}}{3},\ V_{s1} = \tfrac{V_{in}}{3}\tfrac{N_2}{N_1} = V_{s3},\ V_{s2} = -\tfrac{2V_{in}}{3}\tfrac{N_2}{N_1}$$

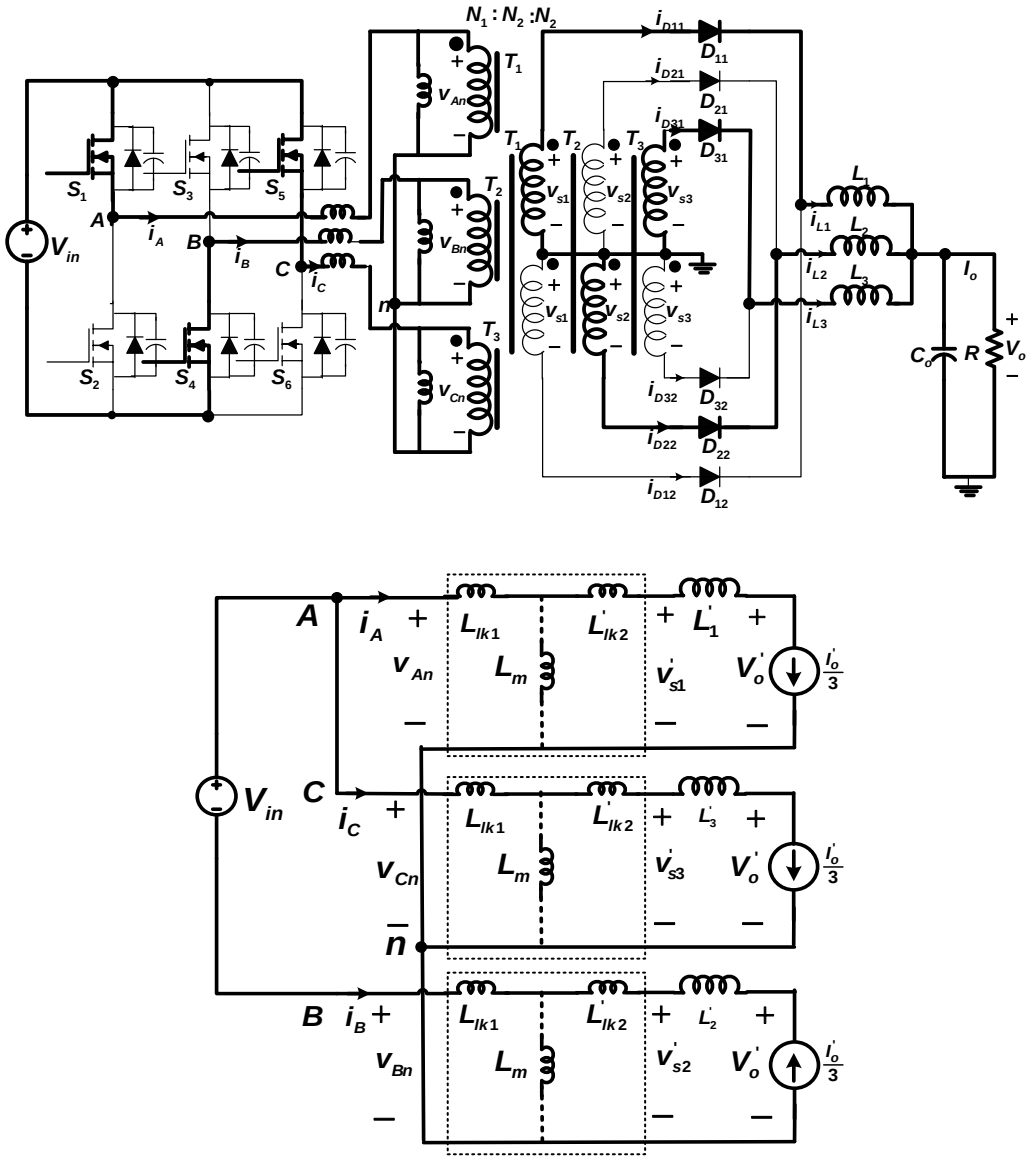


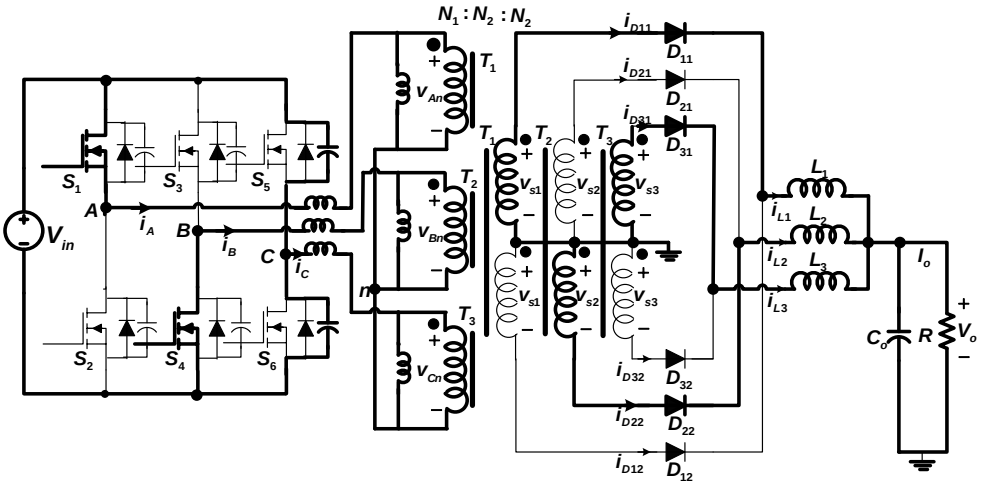
Fig. 4.3 Circuit diagram and equivalent circuit of three-phase LLC resonant DC-DC converter operated in mode-1

The secondary voltage of transformer forward biases the rectifier diodes (D_{11}, D_{22}, D_{31}) and feed energy to load through output inductors (L_1, L_2, L_3). The magnetizing inductance (L_m) of transformer is much larger than leakages inductances $(L_{lk1} + L'_{lk2})$ and connected in parallel, thus neglected as shown by dotted line in Fig. 4.3(b). Further leakage inductances are significantly smaller than primary referred output filter inductance (L'_1, L'_2, L'_3). The primary currents (i_A, i_c) increase with slope $\left(\frac{\frac{V_{in}}{3} - V'_o}{L'_1}\right)$ and i_C increases with negative slope of $\left(\frac{\frac{2V_{in}}{3} - V'_o}{L'_3}\right)$.

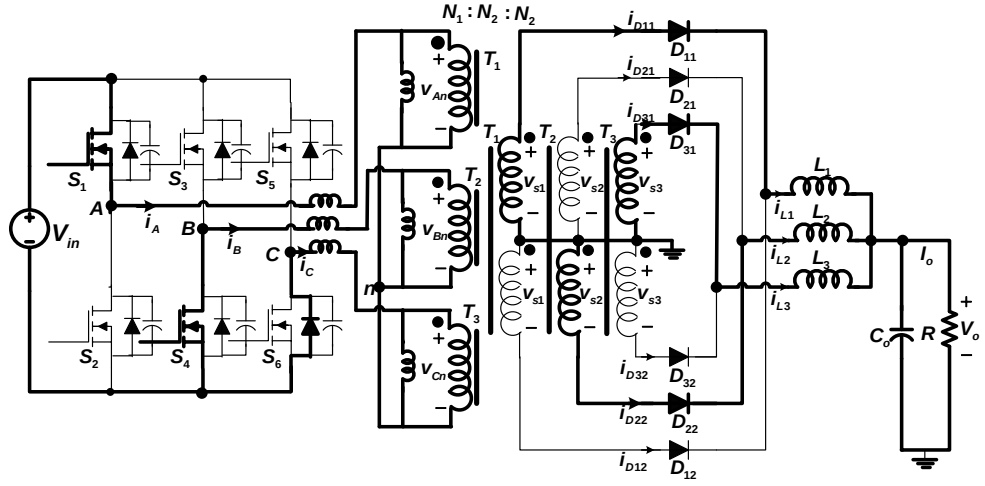
The simplified current equations are given below:

$$i_A = \frac{\frac{V_{in}}{3} - V'_o}{L'_1} \approx \frac{I_o}{3}\frac{N_2}{N_1}, i_B = -\frac{I_o}{3}\frac{N_2}{N_1}, i_C = \frac{I_o}{3}\frac{N_2}{N_1}, i_{D11} = i_{D22} = i_{D31} = \frac{I_o}{3}, \; i_{D12} = i_{D21} = i_{D32} = 0, i_{L1} = i_{L2} = i_{L3} = \frac{I_o}{3}$$

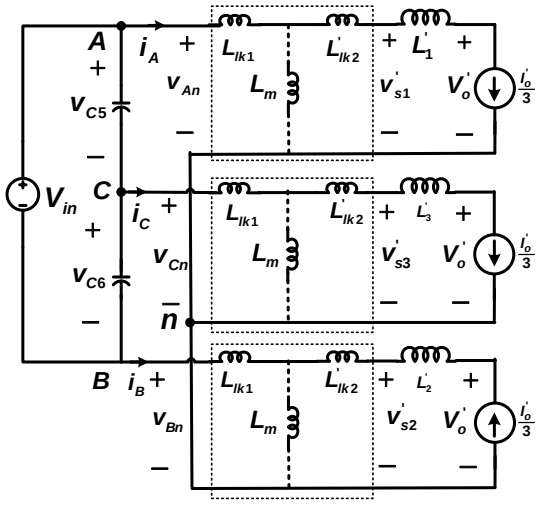
The mode-1 ends with the time instant when the power switch S_5 turns OFF.



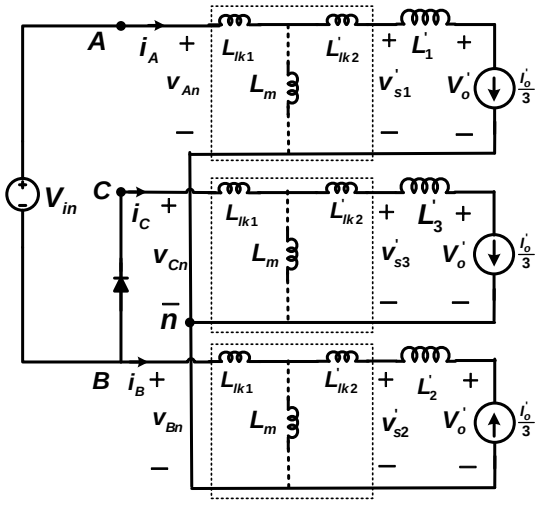
(a)



(b)



(c)



(d)

Fig.4.4 Equivalent circuit of three-phase LLC resonant DC-DC converter (a) Capacitor charging and discharging interval (b) Body diode conduction interval; Simplified equivalent circuit during: (c) Capacitor charging and discharging interval and during (d) Body diode conduction interval

(i) Capacitor charging and discharging Interval

This mode starts with turning OFF of S_5 and power switches (S_1, S_4) are conducting. The primary current (i_C) starts to flow through the parasitic capacitor (C_5, C_6) of S_5, S_6 as shown in Fig.4.4(a). During this mode, C_5 charges and C_6 discharges linearly with the half of i_C. Total energy to charge C_5 and discharge C_6 are supplied from leakage resistance and output filter inductors as shown in Fig.4.4(c). At the end of this mode C_5 is charged to V_{in} and C_6 is discharged to zero. This mode of operation takes places place for a very short duration and thus secondary side current paths are same as mode-1. The voltage across S_6 decreases from V_{in} to zero in time interval $(t_1^+ - t_1^-)$ and hence gate signal should be given to switch S_6 beyond this point to achieve Zero Voltage Switching (ZVS). The charging time interval $(t_1^+ - t_1^-)$ is inversely proportional of load current and hence to achieve a ZVS condition for power switches, this is calculated based on minimum load current.

(ii) Body diode conduction interval

As the capacitor C_6 is discharged to zero, the body diode of power switch S_6 starts conducting and carry primary current i_C as shown in Fig.4.4(b). The simplified equivalent circuit during this mode is shown in Fig.4.4(d). Beyond this point onward gate signal can be applied to S_6 to satisfy ZVS condition. In this interval primary current i_C decreases with slope $\left(-\frac{\frac{V_{in}}{3}-V_o'}{L_3'}\right)$ through body diode of S_6. As i_C becomes zero this mode ends.

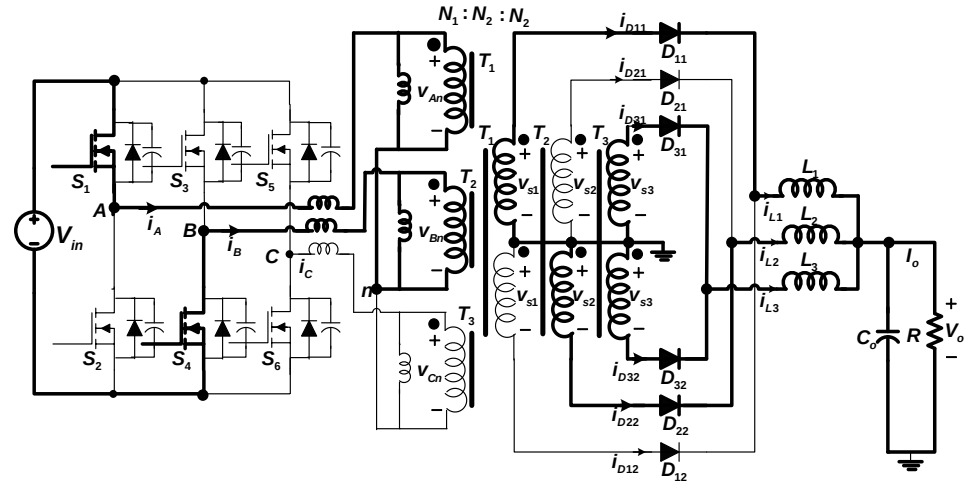
(b) Mode-2

In this mode of operation, power switches S_1 and S_4 are conducting and remaining power switches are OFF. During this mode, the voltage $\left(\frac{V_{in}}{2}\right)$ appears across primary windings of transformer (T_1,T_2) and voltage across the primary winding of transformer (T_3) is zero which forces both rectifier diodes (D_{31}, D_{32}) to free-wheel through both centre-tapped secondary windings of T_3 as depicted in Fig. 4.5(a). The secondary winding voltages of T_1 and T_2 make rectifier diodes D_{11}, D_{22} in forward biased. The voltages and currents during this mode can be evaluated with the help of simplified equivalent circuit shown in Fig. 4.5 (c) and given below:

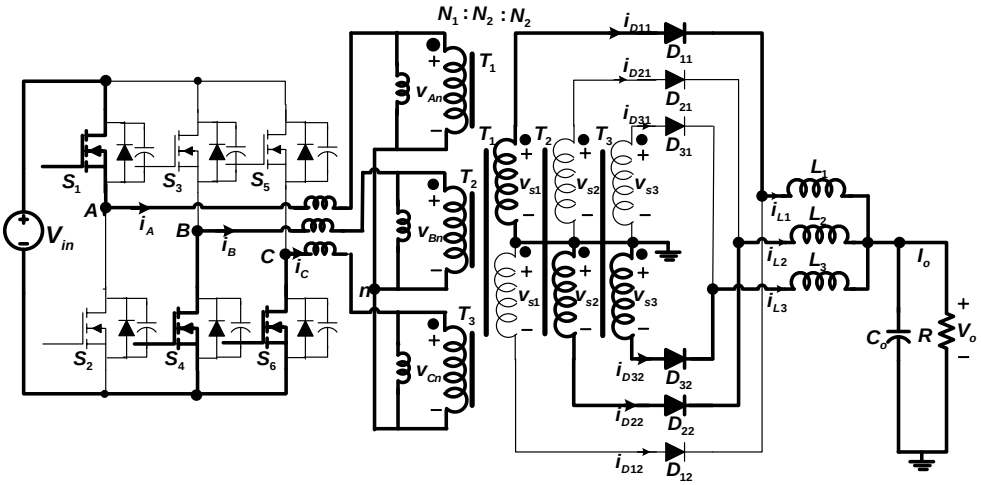
$$v_{AB} = V_{in},\ v_{BC} = \tfrac{V_{in}}{2}, v_{CA} = -\tfrac{V_{in}}{2}, v_{An} = \tfrac{V_{in}}{2}, v_{Bn} = -\tfrac{V_{in}}{2}, v_{Cn} = 0,\ v_{s1} = \tfrac{V_{in}}{2}\tfrac{N_2}{N_1}, v_{s2} = -\tfrac{V_{in}}{2}\tfrac{N_2}{N_1}, v_{s3} = 0,$$

$$i_A = \tfrac{\frac{V_{in}}{2}-V_o'}{L_1'} \approx \tfrac{I_o}{3}\tfrac{N_2}{N_1}, i_B = -\tfrac{I_o}{3}\tfrac{N_2}{N_1}, i_C = 0,\ i_{D11} = i_{D22} = \tfrac{I_o}{3}, i_{D31} = i_{D32} = \tfrac{I_o}{6}, i_{D12} = i_{D21} = 0,$$

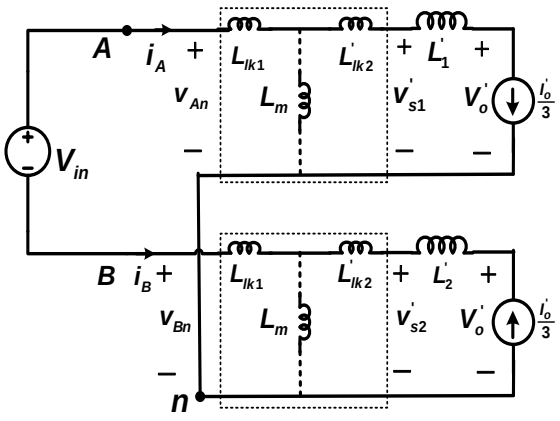
In this mode, current through the power switch S_6 is zero and gating signal is applied to S_6 and hence satisfying ZCS conditions.



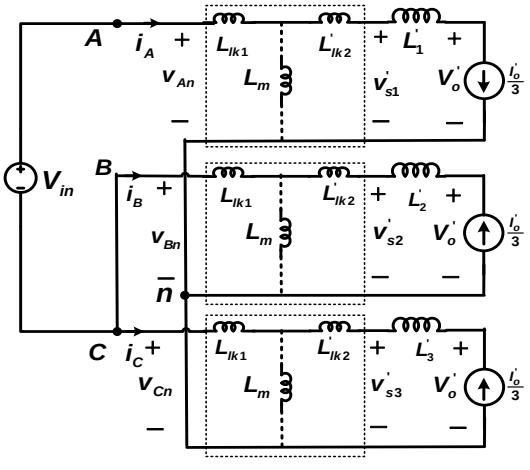
(a)



(b)



(c)



(d)

Fig. 4.5 Equivalent circuit of three-phase LLC resonant DC-DC converter in (a) mode-2 and (b) mode-3; Simplified equivalent circuit (c) mode-2 and (d) mode-3

(c) Mode-3

During this mode switches S_1, S_4, and S_6 are conducting and remaining power switches are OFF. Referring to Fig. 4.5(b) and Fig. 4.5(d), the voltages and currents in different parts of the circuit can be obtained as given below:

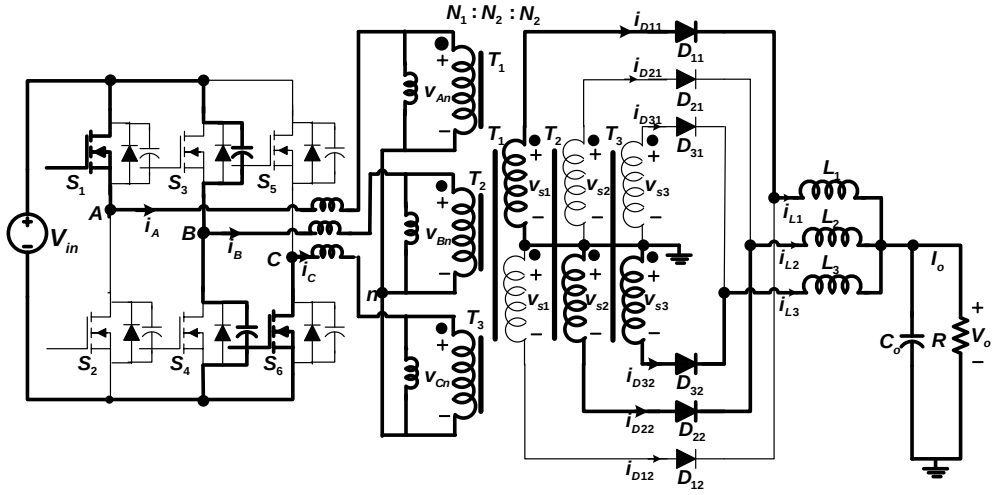
$$v_{AB} = V_{in},\ v_{BC} = 0, v_{CA} = -V_{in}, v_{An} = \frac{2V_{in}}{3}, v_{Bn} = -\frac{V_{in}}{3}, v_{Cn} = -\frac{V_{in}}{3},\ v_{s1} = \frac{2V_{in}}{3}\frac{N_2}{N_1}, v_{s2} = -\frac{V_{in}}{3}\frac{N_2}{N_1} = v_{s3}$$

$$i_A = \frac{\frac{2V_{in}}{3} - V_o'}{L_1'} \approx \frac{I_o}{3}\frac{N_2}{N_1}, i_B = -\frac{I_o}{3}\frac{N_2}{N_1}, i_C = -\frac{I_0}{3}\frac{N_2}{N_1}, i_{D11} = \frac{I_o}{3}, i_{D22} = \frac{I_o}{3}, i_{D32} = \frac{I_o}{3}, i_{D12} = 0,\ i_{D21} = 0,$$

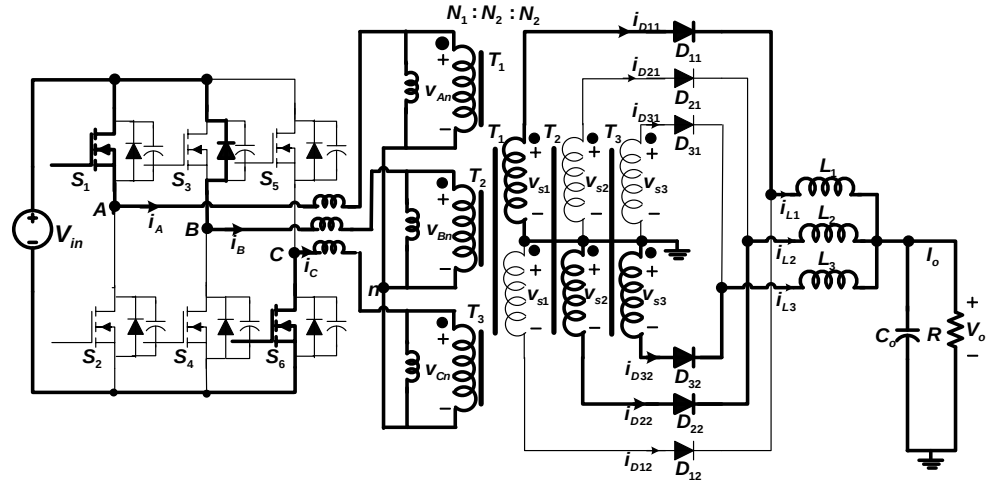
$$i_{D31} = 0,\ i_{L1} = \frac{I_o}{3}, i_{L2} = \frac{I_o}{3}, i_{L3} = \frac{I_o}{3}$$

The voltages v_{An}, v_{Bn} and v_{Cn} appear at primary windings of transformers T_1, T_2 and T_3 respectively and transferred to respective secondary windings of transformers. The induced secondary side voltages v_{s1}, v_{s2} and v_{s3} make rectifier diodes D_{11}, D_{22} and D_{32} in forward biased respectively.

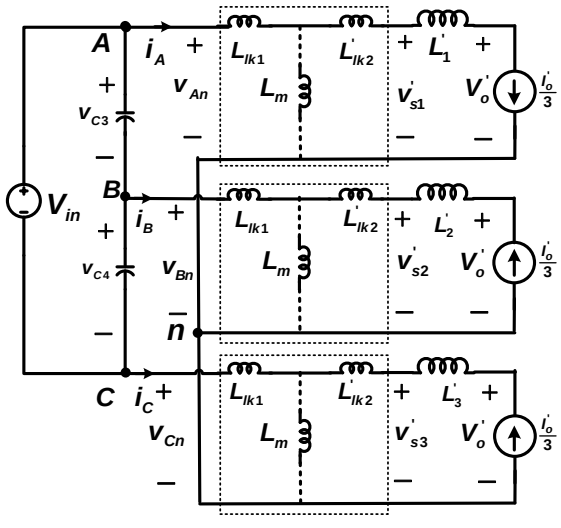
At instant t_3 this mode terminates with switching OFF switch S_4 .As soon as S_4 turned OFF, primary current i_B starts to flow through parasitic capacitors (C_3, C_4) of switches S_3 and S_4 respectively as shown in Fig. 4.6 (a). The charging of C_4 and discharging of C_3 can be explained in the similar ways as that of C_5 and C_6 discussed in capacitor charging interval of Fig.4.4(b). When capacitor C_3 is discharged to zero, body diode (D_3) of switch S_3 starts to conduct and carries primary current i_B as shown in Fig. 4.6 (b). As long as diode D_3 conduct conducts, ZVS condition is achieved. When current i_B becomes zero as shown in Fig. 4.6 (b), the diode stop conducting and creating ZCS for power switch, S_3.



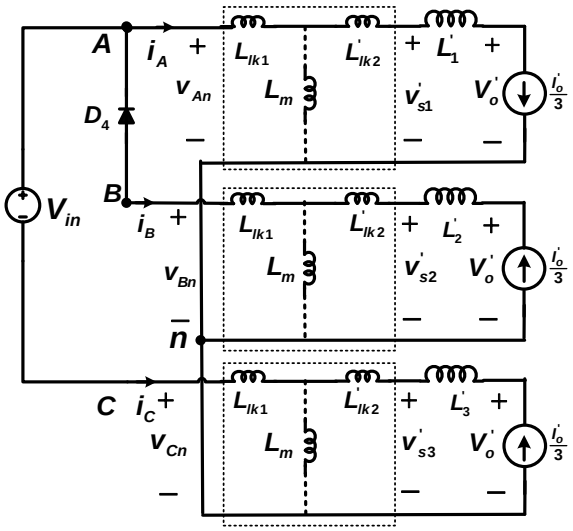
(a)



(b)



(c)



(d)

Fig. 4.6 Circuit diagram and equivalent circuit of three-phase LLC resonant DC-DC converter (a) C_4 charging and C_3 discharging interval (b) body diode (D_4) conduction interval; (c) & (d) Simplified equivalent circuit of operating interval (a) and (b) respectively

(d) Mode-4

As primary current i_B becomes zero, body diode D_3 of power switch S_3 turns OFF and switches S_1 and S_6 remain conducting. The equivalent circuit in this mode is shown in Fig. 4.7(a). The input voltage across primary winding of transformer (T_2) is zero which induced zero voltage in corresponding secondary windings $(v_{s2}=0)$. Thus secondary current of transformer (T_2) free wheels through rectifier diodes (D_{21},D_{22}). Referring simplified equivalent circuit of converter during mode-3 as shown in Fig. 4.7(c), the voltage and current equations in different part of circuit are evaluated as given below:

$$v_{AB}=\tfrac{V_{in}}{2},\ v_{BC}=-\tfrac{V_{in}}{2},v_{CA}=-V_{in},v_{An}=\tfrac{V_{in}}{2},v_{Bn}=0,v_{Cn}=-\tfrac{V_{in}}{2}$$

$$v_{s1}=\tfrac{V_{in}}{2}\tfrac{N_2}{N_1},v_{s2}=0,V_{s3}=-\tfrac{V_{in}}{2}\tfrac{N_2}{N_1}\quad,\quad i_A=\tfrac{\frac{V_{in}}{2}-V_o'}{L_1'}\approx\tfrac{I_o}{3}\tfrac{N_2}{N_1},i_B=0,i_C=-\tfrac{I_0}{3}\tfrac{N_2}{N_1},i_{D11}=\tfrac{I_o}{3},i_{D21}=i_{D22}=\tfrac{I_o}{6},$$

$$i_{D32}=\tfrac{I_o}{3},i_{D12}=0,\ i_{D31}=0\ i_{L1}=\tfrac{I_o}{3},i_{L2}=\tfrac{I_o}{3},i_{L3}=\tfrac{I_o}{3}$$

(e) Mode-5

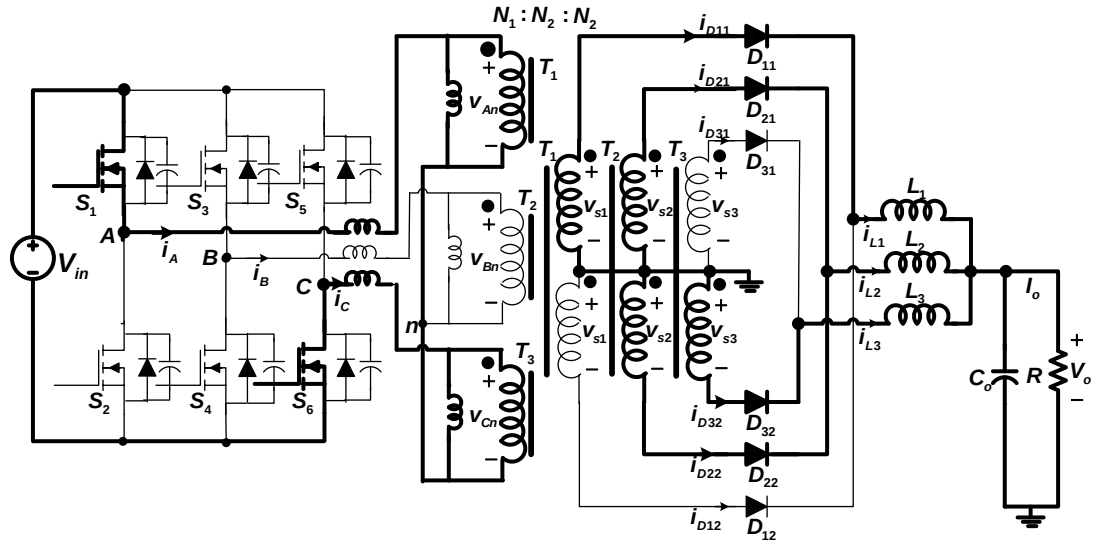
In this mode switch S_3 turns ON at ZCS conditions as discussed during mode-3, primary current, i_B is always zero and S_1, S_6 are already conducting from mode-3. The power switches S_2, S_4 and S_5 are OFF as shown in Fig. 4.7 (b). The voltage and current in different part of circuit are given below:

$$v_{AB}=0,\ v_{BC}=V_{in},v_{CA}=-V_{in},v_{An}=\tfrac{V_{in}}{3},v_{Bn}=\tfrac{V_{in}}{3},v_{Cn}=-\tfrac{2V_{in}}{3},\ v_{s1}=\tfrac{V_{in}}{3}\tfrac{N_2}{N_1},v_{s2}=-\tfrac{V_{in}}{3}\tfrac{N_2}{N_1},$$

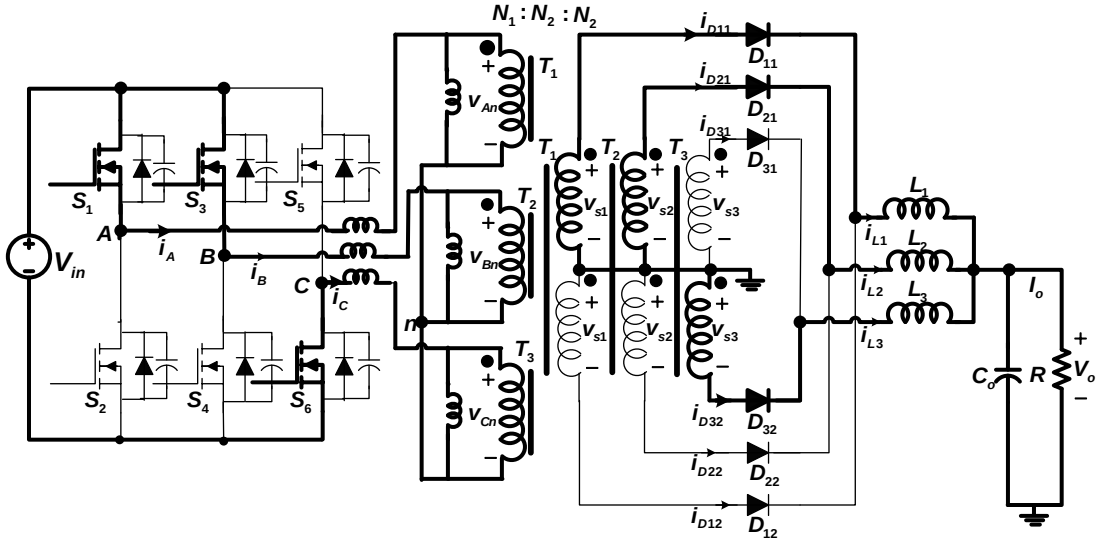
$$V_{s3}=-\tfrac{2V_{in}}{3}\tfrac{N_2}{N_1}\quad,\quad i_A=\tfrac{\frac{V_{in}}{3}-V_o'}{L_1'}\approx\tfrac{I_o}{3}\tfrac{N_2}{N_1},i_B=\tfrac{I_o}{3}\tfrac{N_2}{N_1},i_C=-\tfrac{I_0}{3}\tfrac{N_2}{N_1},i_{D11}=\tfrac{I_o}{3},i_{D21}=\tfrac{I_o}{3},i_{D32}=\tfrac{I_o}{3},i_{D12}=0,$$

$$i_{D31}=0,i_{D22}=0,\ i_{L1}=\tfrac{I_o}{3},i_{L2}=\tfrac{I_o}{3},i_{L3}=\tfrac{I_o}{3}$$

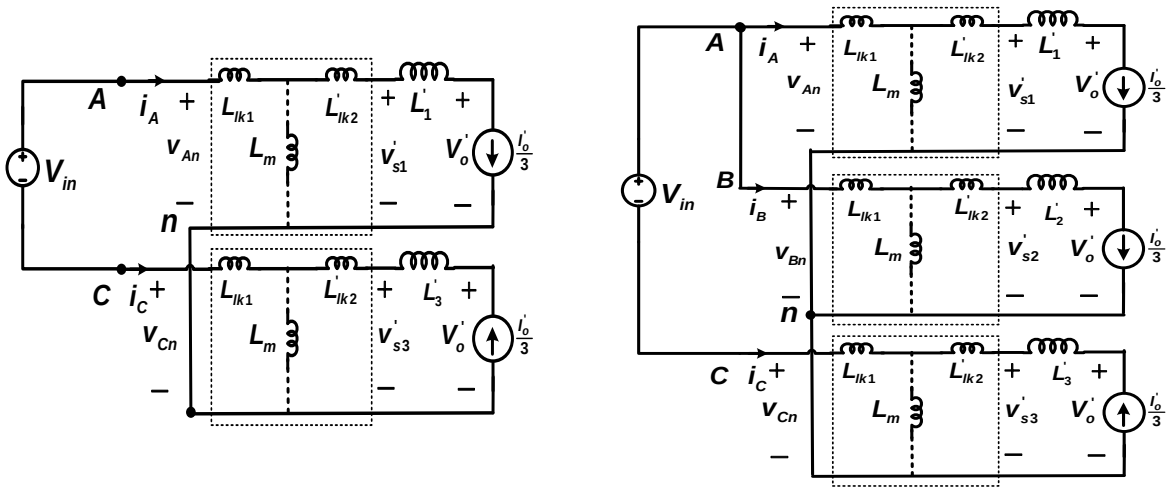
At instant $t= DT$, switch S_1 turns OFF and primary current i_A is diverted through C_1. Thus C_1 starts charging and C_2 starts discharging at same rate as shown in Fig. 4.8 (a). In a very short time interval, C_1 gets charged to V_{in} and C_2 gets discharged to zero. When voltage across C_2 decreases to zero, body diode D_2 of switch S_2 starts conduct and creating ZVS condition for switch S_2 as shown in Fig. 4.8 (b).



(a)

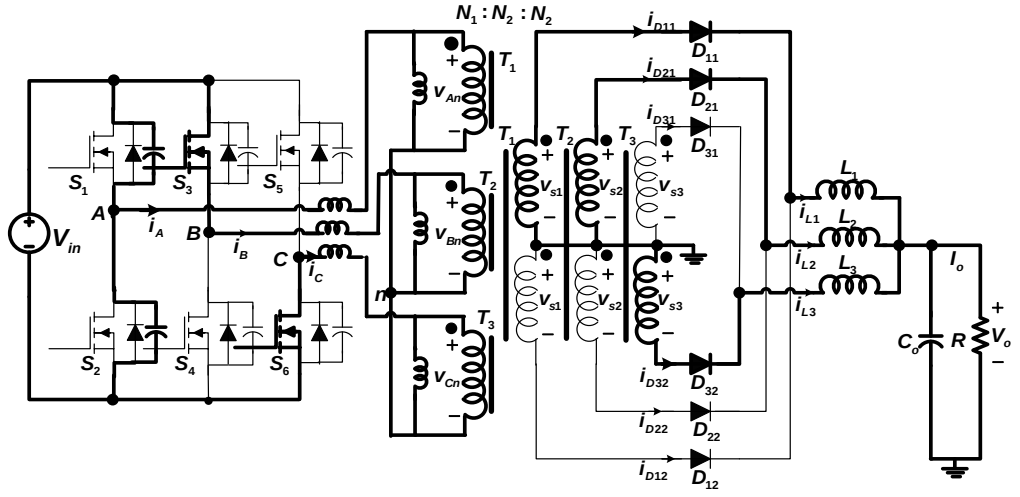


(b)

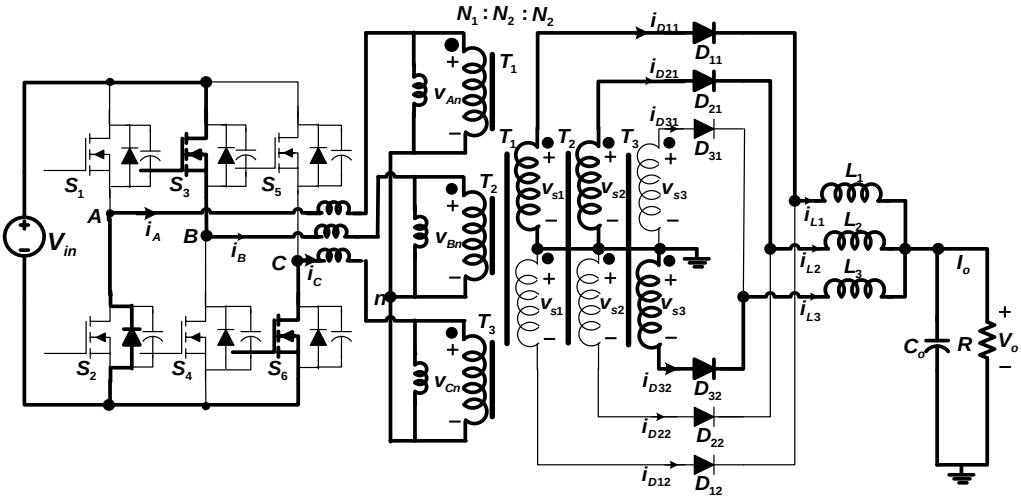


(c) (d)

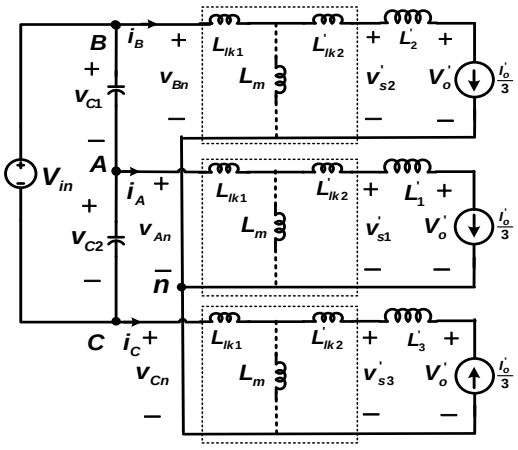
Fig. 4.7 Equivalent circuit of three-phase LLC resonant DC-DC converter (a) mode-4 and (b) mode-5; Simplified equivalent circuit in (c) mode-4 and (d) mode-5



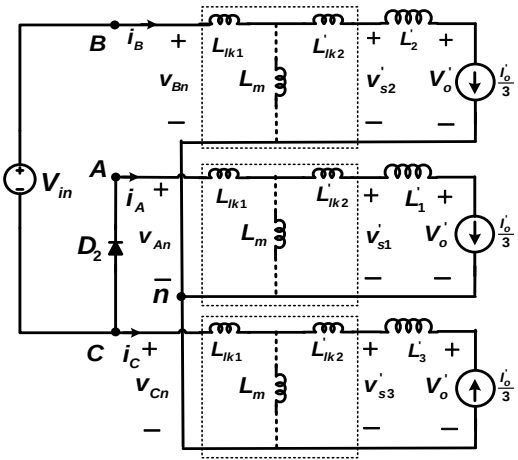
(a)



(b)



(c)



(d)

Fig. 4.8 Circuit diagram and equivalent circuit of three-phase LLC resonant DC-DC converter (a) C_1 charging and C_2 discharging interval (b) Body diode (D_2) conduction interval (c)& (d) Simplified equivalent circuit of operating interval (a) & (b) respectively

(f) Mode-6

As primary current, i_A becomes zero, body diode D_2 stops to conduct. In this mode switches S_3 and S_6 are in conduction. The secondary current of transformer T_1 free-wheel through rectifier diodes D_{11} and D_{12} because induced secondary voltage is zero $(v_{s1}=0)$ as shown in Fig. 4.9(a). The voltage and current in different part of circuit are given below:

$$v_{AB}=0,\ V_{BC}=V_{in}, v_{CA}=-\tfrac{V_{in}}{2}, v_{An}=0, v_{Bn}=\tfrac{V_{in}}{2}, v_{Cn}=-\tfrac{V_{in}}{2},\ V_{s1}=0, v_{s2}=\tfrac{V_{in}}{2}\tfrac{N_2}{N_1}, V_{s3}=-\tfrac{V_{in}}{2}\tfrac{N_2}{N_1},$$

$$i_A=0, i_B=\tfrac{I_o}{3}\tfrac{N_2}{N_1}, i_C=-\tfrac{I_0}{3}\tfrac{N_2}{N_1}, i_{D11}=\tfrac{I_o}{6}, i_{D21}=\tfrac{I_o}{3}, i_{D32}=\tfrac{I_o}{3},$$

$$i_{D12}=\tfrac{I_o}{6},\ i_{D31}=0, i_{D22}=0,\ i_{L1}=\tfrac{I_o}{3}, i_{L2}=\tfrac{I_o}{3}, i_{L3}=\tfrac{I_o}{3}$$

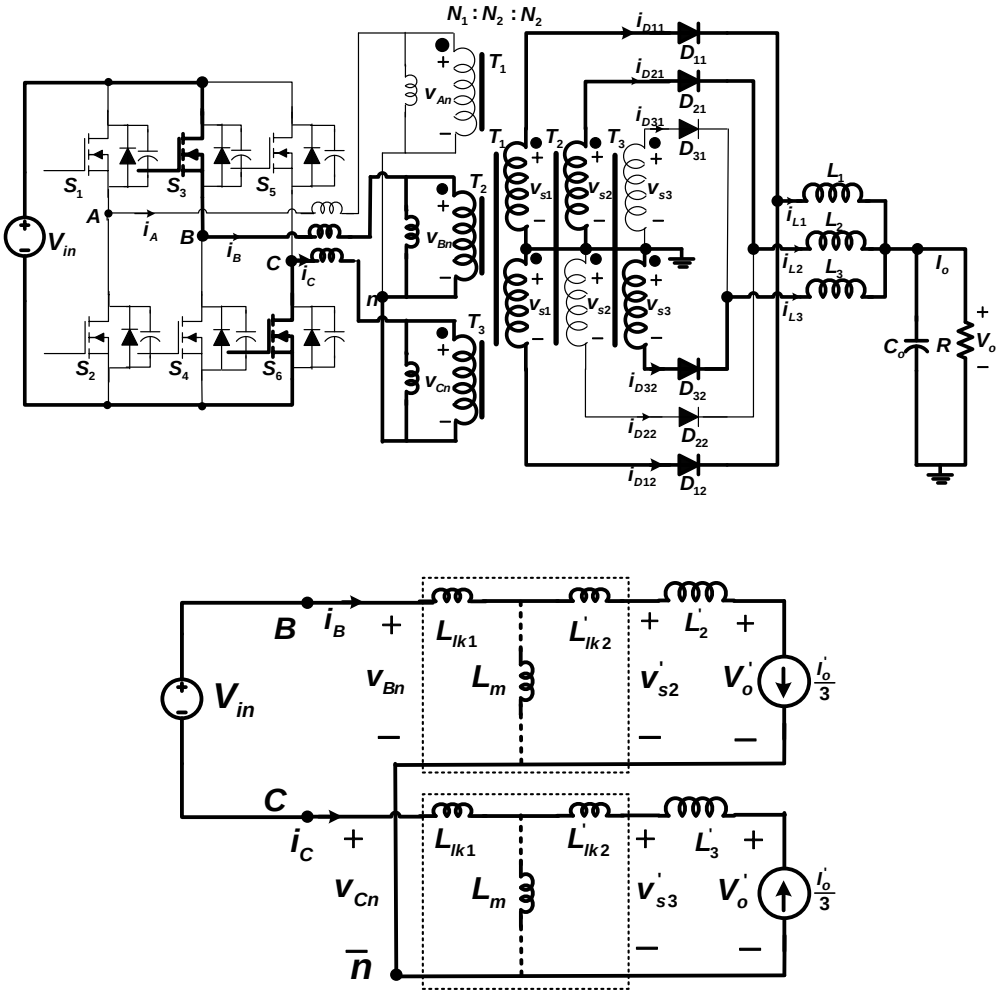


Fig. 4.9 Equivalent circuit & simplified equivalent circuit of three-phase LLC resonant DC-DC converter in mode-6

4.3.2 Modeling of LLC Resonant Tank

The objective of resonant tank is to pass fundamental component of current which lags the fundamental component of input voltage to resonant tank. The output voltage of three-phase bridge inverter appears as an input to resonant tank. The per phase model of three-phase LLC resonant converter can be represented as in shown Fig. 4.10(a). Classical ac circuit analysis approach can be used for its analysis. The following steps are to be followed:

***Step-1**: Derivation of RMS value fundamental component of phase voltages* $\left(V_{ph1}\right)$.

The phase voltage $\left(V_{ph}\right)$ of three-phase full bridge inverter operated in region (*Reg3*) is shown in Fig. 4.10(c). The waveform of v_{ph} is odd and quarter wave symmetry about y-axis (shown in dotted line) at $t=0$. This waveform can be expressed in terms of input dc voltage and duty ratio using Fourier series. The Fourier Coefficients $\left(a_o=0;a_n=0\right)$; as v_{ph} odd and quarter wave symmetric and b_n can be evaluated as follows:

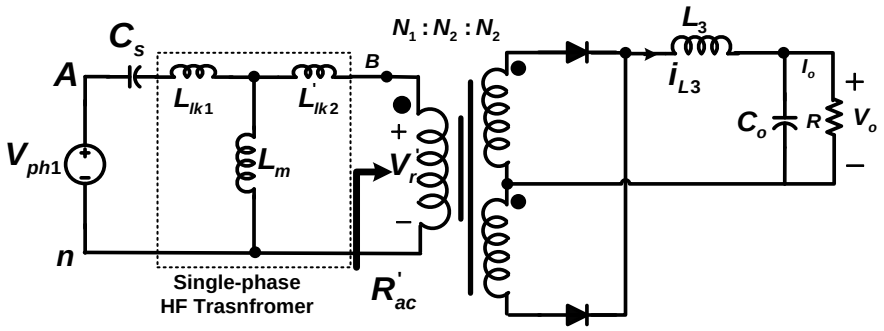
$$
\begin{aligned}
b_n &= \frac{8}{T}\int_0^{\frac{T}{4}} v_{ph}(t)\sin(n\omega t)dt \\
&= \frac{8}{T}\left[\int_{\left(\frac{1}{4}-\frac{D}{2}\right)T}^{\left(\frac{D}{2}-\frac{1}{12}\right)T}\frac{V_{in}}{3}\sin(n\omega t)dt + \int_{\left(\frac{D}{2}-\frac{1}{12}\right)T}^{\left(\frac{5}{12}-\frac{D}{2}\right)T}\frac{V_{in}}{2}\sin(n\omega t)dt + \int_{\left(\frac{5}{12}-\frac{D}{2}\right)T}^{\frac{T}{4}}\frac{V_{in}}{3}\sin(n\omega t)dt\right] \\
&= \frac{8}{T}V_{in}\left[\frac{1}{3}\left\{-\frac{\cos(n\omega t)}{n\omega}\right\}\Bigg|_{\left(\frac{1}{4}-\frac{D}{2}\right)T}^{\left(\frac{D}{2}-\frac{1}{12}\right)T} + \frac{1}{2}\left\{-\frac{\cos(n\omega t)}{n\omega}\right\}\Bigg|_{\left(\frac{D}{2}-\frac{1}{12}\right)T}^{\left(\frac{5}{12}-\frac{D}{2}\right)T} + \frac{2}{3}\left\{-\frac{\cos(n\omega t)}{n\omega}\right\}\Bigg|_{\left(\frac{5}{12}-\frac{D}{2}\right)T}^{\frac{T}{4}}\right] \\
&= \frac{8}{n\omega T}V_{in}\begin{bmatrix}\frac{1}{3}\left\{\cos\left(n\omega T\left(\frac{1}{4}-\frac{D}{2}\right)\right)-\cos\left(n\omega T\left(\frac{D}{2}-\frac{1}{12}\right)\right)\right\}+\\ \frac{1}{2}\left\{\cos\left(n\omega T\left(\frac{D}{2}-\frac{1}{12}\right)\right)-\cos\left(n\omega T\left(\frac{5}{12}-\frac{D}{2}\right)\right)\right\}+\\ \frac{2}{3}\left\{\cos\left(n\omega T\left(\frac{5}{12}-\frac{D}{2}\right)\right)-\cos\left(n\omega\frac{T}{4}\right)\right\}\end{bmatrix} \\
b_n &= \frac{8}{n\pi}V_{in}\begin{bmatrix}\frac{1}{3}\sin\left(\frac{n\pi}{6}\right)\sin n\pi\left(D-\frac{1}{3}\right)+\frac{1}{2}\sin\left(\frac{n\pi}{3}\right)\sin n\pi\left(-D+\frac{1}{2}\right)\\ +\frac{2}{3}\sin n\pi\left(-\frac{D}{2}+\frac{2}{3}\right)\sin n\pi\left(\frac{D}{2}-\frac{1}{6}\right)\end{bmatrix} \qquad (4.1)
\end{aligned}
$$

Substitute $n=1$, in equation(4.1), yields

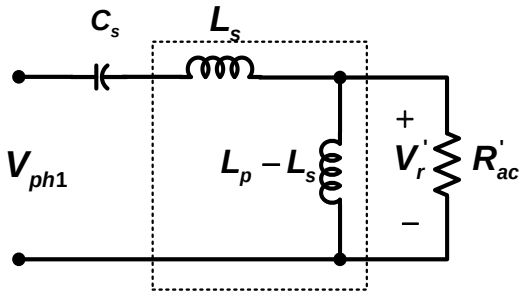
$$
\begin{aligned}
b_1 &= \frac{8}{\pi}V_{in}\begin{bmatrix}\frac{1}{3}\sin\left(\frac{\pi}{6}\right)\sin\pi\left(D-\frac{1}{3}\right)+\frac{1}{2}\sin\left(\frac{\pi}{3}\right)\sin\pi\left(-D+\frac{1}{2}\right)\\ +\frac{2}{3}\sin\pi\left(-\frac{D}{2}+\frac{2}{3}\right)\sin\pi\left(\frac{D}{2}-\frac{1}{6}\right)\end{bmatrix} \qquad (4.2) \\
&= \frac{2V_{in}}{\pi}\sin(\pi D)
\end{aligned}
$$

Therefore, RMS value of fundamental voltage of the three-phase bridge inverter can be represented in terms of dc input voltage and duty ratio**,** is given by;

$$V_{ph1}=\frac{\sqrt{2}V_{in}}{\pi}\sin(\pi D) \qquad (4.3)$$



(a)



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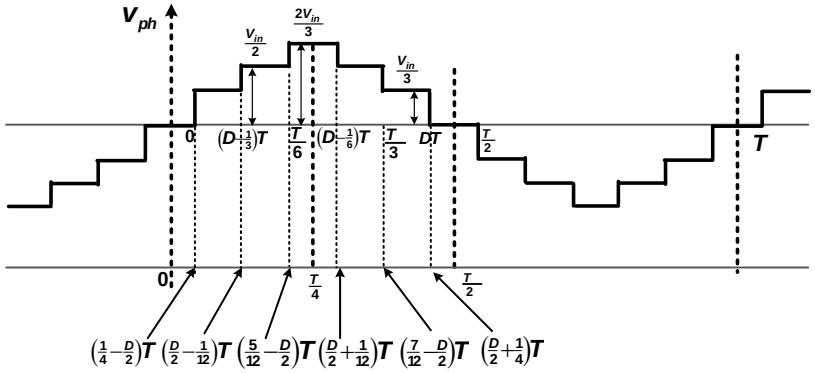


(c)

Fig. 4.10 Per phase LLC Resonant DC-DC Converter (a) AC equivalent model (b) Resonant network(c) Phase voltage of three-phase bride inverter operated in *Reg3*

Step-2: *Modifying resonant tank as per practical design*

The elements of LLC tank may be integrated with transformer as shown in Fig. 4.10(a) and the parameters L_p and L_s are related to leakage inductances (L_{lk1}, L_{lk2}) and magnetizing inductance (L_m) of single-phase high frequency transformer as follows:

$$L_p = L_{lk1} + L_m \simeq L_m \qquad ; \; L_m \gg L_{lk1}$$

$$L_s = L_{lk1} + \frac{L_m L'_{lk2}}{L_m + L'_{lk2}} \simeq 2L_{lk1} \quad ; \; L_m \gg L_{lk1}, \; L_{lk1} = L'_{lk2}$$

Thus, inductances (L_p, L_s) of resonant tank network can be practically calculated using leakage inductances and magnetizing inductance of high frequency transformer. If leakage inductances are not sufficient then external series inductance may be added.

Step-3 *Derivation of equivalent ac load resistance referred to primary side.*

The input current (i_{ph}) of centre-tapped rectifier shown in Fig. 4.11(a) is illustrated in Fig. 4.11(b). The waveform of i_{ph} is even and half wave symmetric about y-axis (shown as dotted line) with only the odd harmonics of cosine terms present as follows:

$$\begin{aligned} a_n &= \frac{4}{T}\left[\int_{-\frac{DT}{2}}^{\frac{DT}{2}} \frac{I_o}{3}\frac{N_2}{N_1}\cos(n\omega t)\,dt\right] \\ &= \frac{4N_2 I_o}{3N_1 T}\left[\frac{\sin(n\omega t)}{n\omega}\Bigg|_{-\frac{DT}{2}}^{\frac{DT}{2}}\right] \\ &= \frac{4N_2 I_o}{3n\omega N_1 T}\left[\sin\left(n\omega\tfrac{DT}{2}\right)-\sin\left(-n\omega\tfrac{DT}{2}\right)\right] \\ &= \frac{8N_2 I_o}{3n\omega N_1 T}\sin\left(n\omega\tfrac{DT}{2}\right) \\ &= \frac{4I_o}{3n\pi}\frac{N_2}{N_1}\sin(n\pi D) \end{aligned}$$

$$i_{ph}(t) = \sum_{n=1,3,5,..}^{\infty} \frac{4I_o}{3n\pi}\frac{N_2}{N_1}\sin(n\pi D)\cos(n\omega t) \tag{4.4}$$

Substituting $n = 1$ in equation(4.4) yields fundamental phase current and its RMS value can be evaluated as

$$I_{ph1} = \frac{2\sqrt{2}I_o}{3\pi}\frac{N_2}{N_1}\sin(\pi D) \tag{4.5}$$

Average value of rectified fundamental voltage:

$$\begin{aligned} V_o &= \frac{2}{T}\left[\int_0^{\frac{T}{2}} \frac{V_p N_2}{N_1}\sin(\omega t)\,dt\right] = \frac{2}{T}\frac{V_p N_2}{N_1}\left(\frac{-\cos(\omega t)}{\omega}\right)\Bigg|_0^{\frac{T}{2}} \\ &= \frac{2}{T}\frac{V_p N_2}{N_1\omega}\left(1-\cos\left(\tfrac{\omega T}{2}\right)\right) = \frac{2V_p}{\pi}\frac{N_2}{N_1} \end{aligned}$$

$$V_o = \frac{2V_p}{\pi}\frac{N_2}{N_1} \tag{4.6}$$

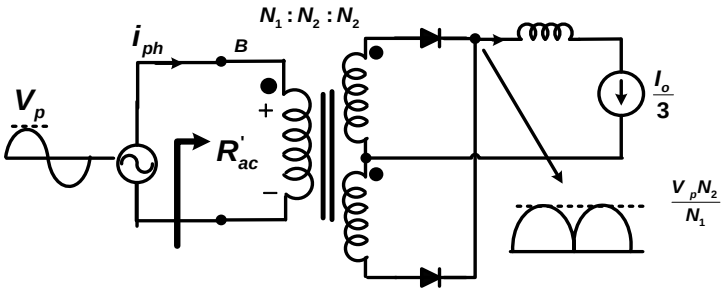
Therefore, the RMS value of input voltage to the centre-tapped rectifier can be represented as

$$V_r' = \frac{\pi}{2\sqrt{2}}\frac{N_1}{N_2}V_o \tag{4.7}$$

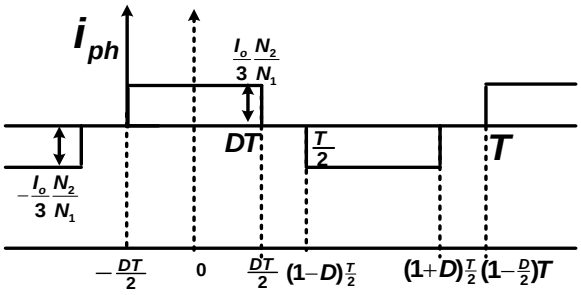
The equation(4.5),(4.6) and equation(4.7), yields equivalent ac resistance ($R_{ac}^{'}$), as follows

$$R_{ac}^{'} = \frac{V_r^{'}}{I_{ph1}} = \frac{3\pi^2}{8}\frac{N_1^2}{N_2^2}\frac{1}{\sin(\pi D)}R \tag{4.8}$$

Where $R = \frac{V_o}{I_o}$ be the actual load resistance as shown in Fig. 4.10(a).



(a)



(b)

Fig. 4.11 Equivalent AC load as derived by rectifier load (a) Centre-tapped converter (b) Input current waveform

The voltage gain of converter can be derived as follows:

$$Z_{in}(s) = \frac{1}{sC_s} + sL_s + \frac{s(L_p - L_s)R_{ac}^{'}}{R_{ac}^{'} + s(L_p - L_s)}$$

$$= \frac{R_{ac}^{'} + s(L_p - L_s) + s^2L_sC_s\left\{R_{ac}^{'} + s(L_p - L_s)\right\} + s^2C_s(L_p - L_s)R_{ac}^{'}}{sC_s\left(R_{ac}^{'} + s(L_p - L_s)\right)}$$

$$= \frac{R_{ac}^{'} + s(L_p - L_s) + s^2R_{ac}^{'}L_pC_s + s^3L_sC_s(L_p - L_s)}{sC_sR_{ac}^{'} + s^2C_s(L_p - L_s)}$$

$$Z_{in}(s) = \frac{R_{ac}^{'} + s(L_p - L_s) + s^2R_{ac}^{'}L_pC_s + s^3L_sC_s(L_p - L_s)}{sC_sR_{ac}^{'} + s^2C_s(L_p - L_s)} \tag{4.9}$$

$$I_{ph1} = \frac{V_{ph1}(s)}{Z_{in}(s)} = \frac{\frac{\sqrt{2}V_{in}}{\pi}\sin(\pi D)\left\{sC_sR_{ac}^{'} + s^2C_s(L_p - L_s)\right\}}{R_{ac}^{'} + s(L_p - L_s) + s^2R_{ac}^{'}L_pC_s + s^3L_sC_s(L_p - L_s)} \tag{4.10}$$

Substitute $s = j\omega$ in equation(4.10), we get

$$I_{ph1} = \frac{\frac{\sqrt{2}V_{in}}{\pi}\sin(\pi D)\left\{-\omega^2 L_s C_s\left(\frac{L_p}{L_s}-1\right)+j\omega C_s R_{ac}^{'}\right\}}{R_{ac}^{'}-\omega^2 R_{ac}^{'} L_p C_s + j\omega L_s\left\{\left(\frac{L_p}{L_s}-1\right)-\omega^2 L_s C_s\left(\frac{L_p}{L_s}-1\right)\right\}}$$

$$= \frac{\sqrt{2}V_{in}}{\pi}\sin(\pi D)\frac{\left\{-\frac{\omega^2}{\omega_o^2}(m-1)+j\frac{\omega}{\omega_o}\frac{1}{Q}\right\}}{R_{ac}^{'}\left(1-\frac{\omega^2}{\omega_p^2}\right)+j\frac{\omega}{\omega_o}\omega_o L_s\left\{m-1-\frac{\omega^2}{\omega_o^2}(m-1)\right\}}$$

$$I_{ph1} = \frac{\sqrt{2}V_{in}}{\pi}\sin(\pi D)\frac{\left\{\frac{\omega}{\omega_o}Q(m-1)-j\right\}}{\frac{\omega_o}{\omega}\sqrt{\frac{L_s}{C_s}}\left(\frac{\omega^2}{\omega_p^2}-1\right)+jQ\sqrt{\frac{L_s}{C_s}}(m-1)\left(\frac{\omega^2}{\omega_o^2}-1\right)} \tag{4.11}$$

Where

$$\omega_o = \frac{1}{\sqrt{L_s C_s}},\ \omega_p = \frac{1}{\sqrt{L_p C_s}},\ m = \frac{L_p}{L_s},\ Q = \sqrt{\frac{L_s}{C_s}}\frac{1}{R_{ac}^{'}}$$

Referring Fig. 4.10(b), voltage gain can be calculated as follows:

$$V_r^{'} = I_{ph1}.\frac{j\omega L_s\left(\frac{L_p}{L_s}-1\right)R_{ac}^{'}}{R_{ac}^{'}+j\omega L_s\left(\frac{L_p}{L_s}-1\right)}$$

$$V_r^{'} = I_{ph1}.\frac{j\frac{\omega}{\omega_o}(m-1)\sqrt{\frac{L_p}{L_s}}}{1+j\frac{\omega}{\omega_o}(m-1)Q} \tag{4.12}$$

Substituting equations(4.11),(4.12) in equation (5.13) , yields

$$\frac{V_o}{V_{in}} = \frac{4}{\pi^2}\frac{N_2}{N_1}\frac{(m-1)\sin(\pi D)}{\left(m-\frac{\omega_o^2}{\omega^2}\right)+jQ(m-1)\left(\frac{\omega}{\omega_o}-\frac{\omega_o}{\omega}\right)} \tag{4.13}$$

Similarly, the expression of voltage stresses across inductor and capacitor can be derived.

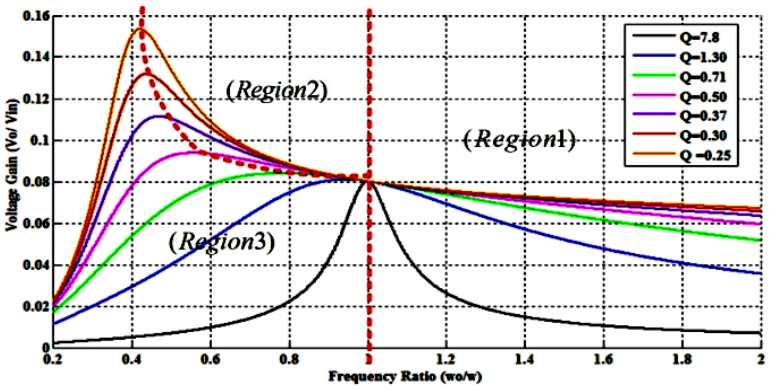
$$\frac{V_{Ls}}{V_{in}} = \frac{\sqrt{2}}{\pi}\sin(\pi D)\frac{\frac{\omega^2}{\omega_o^2}\left\{1+jQ(m-1)\frac{\omega}{\omega_o}\right\}}{\left(\frac{\omega^2}{\omega_p^2}-1\right)+jQ(m-1)\frac{\omega}{\omega_o}\left(\frac{\omega^2}{\omega_o^2}-1\right)} \tag{4.14}$$

$$\frac{V_{Cs}}{V_{in}} = \frac{\sqrt{2}}{\pi}\sin(\pi D)\frac{\frac{\omega^2}{\omega_o^2}\left\{Q(m-1)\frac{\omega}{\omega_o}-j\right\}}{-Q(m-1)\frac{\omega}{\omega_o}\left(\frac{\omega^2}{\omega_p^2}-1\right)+j\left(\frac{\omega^2}{\omega_p^2}-1\right)} \tag{4.15}$$

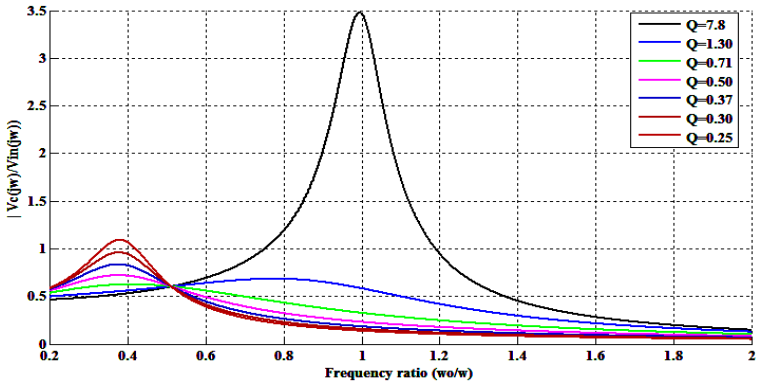
Based on ac classical analysis, design equations of inductor current (i_{Ls}), converter voltage gain $\left(\frac{V_o}{V_{in}}\right)$, voltage stress across resonant inductor $\left(\frac{V_{Ls}}{V_{in}}\right)$, and voltage stress across resonant capacitor $\left(\frac{V_{Cs}}{V_{in}}\right)$ are derived as given by equations(4.11),(4.13),(4.14) and equation

(4.15). With the help of these equations, the design curves of LLC resonant tank network are plotted against normalized frequency for different values of *Q*-factor as shown in Fig.4.12.

The voltage gain characteristic of converter is divided into three regions as shown in Fig.4.12(a). For this converter, there are two resonant frequencies $\left(\omega_0 \,\&\, \omega_p\right)$. One is determined by the resonant components L_S and C_s. The other is determined by (L_p-L_s), C_s and load condition. As load increases, the resonant frequency shifts to higher frequency. The operation of converter in region-2 of voltage gain characteristic is restricted by ratio $\left(\frac{L_s}{L_p - L_s}\right)$ with change in output voltage of bridge inverter. If converter is designed to operate with rated voltage at $\frac{\omega}{\omega_o}$, then with decrease load current, the converter automatically enters in the lagging power factor mode. There are three possible modes of operation based on ratio of switching frequency (ω) to resonant frequency (ω_o). The operation below resonant frequency exhibits large peak current in circuits and therefore, results high conduction losses, high VA rating of reactive components. The operation of converter above resonant frequency has several advantages such as use of internal body diode and output capacitance of MOSFET, reduces size of reactive and high frequency transformer and no need to limit rate of change of current.



(a)



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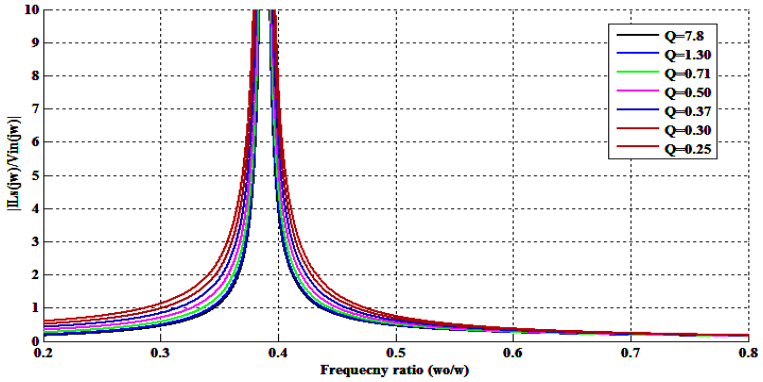

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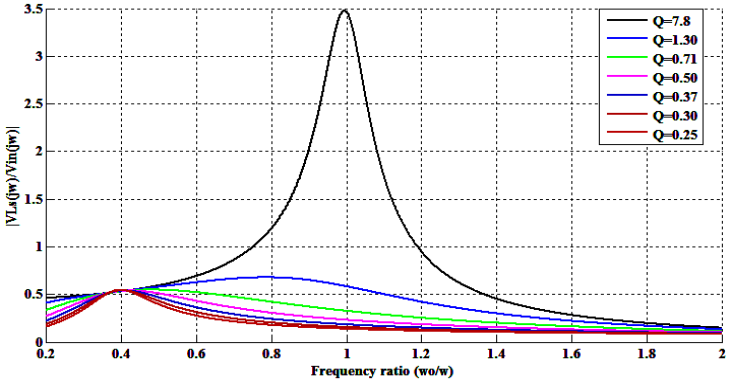


(d)

Fig.4.12 Design curves for LLC resonant tank (a) $\frac{V_o}{V_{in}}$ (b) $\frac{V_{Cs}}{V_{in}}$ (c) $\frac{I_{Ls}}{V_{in}}$ (d) $\frac{V_{Ls}}{V_{in}}$ Versus $\frac{\omega}{\omega_o}$

4.3.3 Converter Design

Design of converter includes selection of mainly three parameters namely output filter inductor design, output filter capacitor and selection of operating switching frequency. Fig.4.12(a) shows that maximum converter voltage gain lies between two frequencies (ω_p) and (ω_o) in design curve. As load increases operating frequency shifted to frequency ω_o and as load decreases operating frequency shifted to ω_p. Selection of operating frequency should be taken as ω_o for full load conditions and maximum duty cycle. Design of resonant circuit parameters is based on equations for $\omega_o, \omega_p, m \& Q$ which is developed in sub-section 4.3.2.

The design of output filter components are based on the following assumptions-

- All the output filter inductors are identical.
- The rate of change of inductor current is linear.
- The duty cycle of switches is assumed to be 50% in worst case design (minimum input DC voltage and full load condition).

(a) Output filter design relation

Fig. 4.13 shows the voltage and current associated with output filter inductor and it is observed that inductor current varies linearly with different slopes in different time intervals. The inductor current in various time intervals is given below:

Time interval $(t_o < t \le t_1)$; $t_1 - t_o = DT - \frac{T}{3}$

$$v_{L1}(t) = \frac{V_{in}}{3n} - V_o \tag{4.16}$$

$$i_{L1}(t) = \left(\frac{\frac{V_{in}}{3}\frac{N_2}{N_1} - V_o}{L_1} \right)(t - t_o) + i_{L1}(t_o)$$

$$i_{L1}(t) = m_1(t - t_o) + I_{L1\min} \tag{4.17}$$

At the end of this interval, inductor current $i_{L1}(t)$ can be written as

$$i_{L1}(t_1) = m_1(t_1 - t_o) + I_{L1\min} \tag{4.18}$$

Where $m_1 = \frac{\frac{V_{in}}{3}\frac{N_2}{N_1} - V_o}{L_1}$, $i_{L1}(t_o) = I_{L1\min}$

Time interval $(t_1 < t \le t_2)$; $t_2 - t_1 = \frac{T}{2} - DT$

$$v_{L1}(t) = \frac{V_{in}}{2n} - V_o \tag{4.19}$$

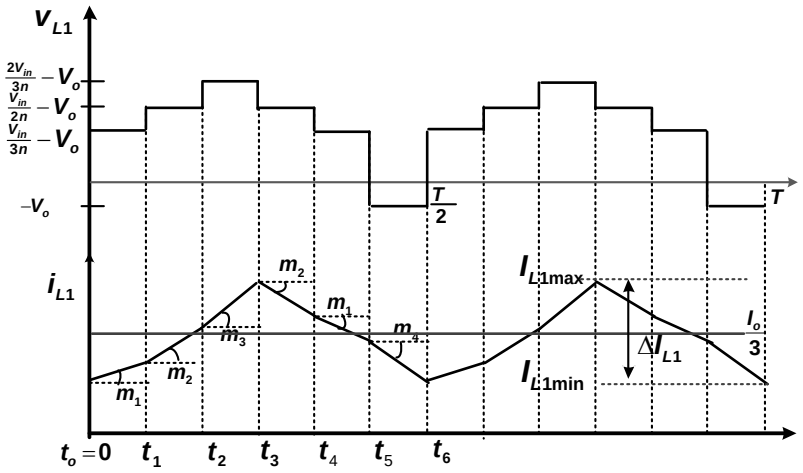


Fig. 4.13 Voltage and current waveforms of output inductor (L_1)

$$i_{L1}(t)=\left(\frac{\frac{V_{in}}{2}\frac{N_2}{N_1}-V_o}{L_1}\right)(t-t_1)+i_{L1}(t_1)$$

$$i_{L1}(t)=m_2(t-t_1)+m_1(t_1-t_o)+I_{L1\min} \tag{4.20}$$

Where $m_2=\frac{\frac{V_{in}}{2}\frac{N_2}{N_1}-V_o}{L_1}$

At the end of this time interval, inductor current $i_{L1}(t)$ can be written as

$$i_{L1}(t_2)=m_2(t_2-t_1)+m_1(t_1-t_o)+I_{L1\min} \tag{4.21}$$

Time interval $(t_2<t\le t_3)$; $t_3-t_2=DT-\frac{T}{3}$

$$v_{L1}(t)=\frac{2V_{in}}{3n}-V_o \tag{4.22}$$

$$i_{L1}(t)=\left(\frac{\frac{2V_{in}}{3}\frac{N_2}{N_1}-V_o}{L_1}\right)(t-t_2)+i_{L1}(t_2)$$

$$i_{L1}(t)=m_3(t-t_2)+m_2(t_2-t_1)+m_1(t_1-t_o)+I_{L1\min} \tag{4.23}$$

Where $m_3=\frac{\frac{2V_{in}}{3}\frac{N_2}{N_1}-V_o}{L_1}$, $i_{L1}(t_3)=I_{L1\max}$

At the end of this time interval, inductor current $i_{L1}(t)$ can be written as

$$i_{L1}(t_3)=m_3(t_3-t_2)+m_2(t_2-t_1)+m_1(t_1-t_o)+I_{L1\min} \tag{4.24}$$

The inductor current at the end of the switching cycle be the same as that of the beginning under steady - state operation and therefore the net change in inductor current over one period is zero.

$$\left(\sum_{t=0}^{t_6}\Delta i_{L1}\right)_{T/2}=0 \tag{4.25}$$

Converter voltage gain can be obtained as follows:

$$\left(\frac{V_{in}}{3}\frac{N_2}{N_1}-V_o\right)\{(t_1-t_o)+(t_5-t_4)\}+\left(\frac{V_{in}}{2}\frac{N_2}{N_1}-V_o\right)\{(t_2-t_1)+(t_4-t_3)\}$$
$$+\left(\frac{2V_{in}}{3}\frac{N_2}{N_1}-V_o\right)(t_3-t_2)+-V_o(t_6-t_5)=0$$

$$\frac{V_o}{V_{in}}=\frac{1}{3}\frac{N_2}{N_1}\left(2D+\frac{1}{3}\right) \tag{4.26}$$

The ripple in an inductor can be evaluated from equation(4.24) and substituting values of slopes (m_1, m_2 and m_3) and time duration of time intervals as follows:

$$\Delta I_{L1}=I_{L1\max}-I_{L1\min}=m_3(t_3-t_2)+m_2(t_2-t_1)+m_1(t_1-t_o)$$
$$=\frac{\left(\frac{2V_{in}}{3}\frac{N_2}{N_1}-V_o\right)}{L_1}\left(DT-\frac{T}{3}\right)+\frac{\left(\frac{V_{in}}{2}\frac{N_2}{N_1}-V_o\right)}{L_1}\left(\frac{T}{2}-DT\right)+\frac{\left(\frac{V_{in}}{3}\frac{N_2}{N_1}-V_o\right)}{L_1}\left(DT-\frac{T}{3}\right)$$
$$=\frac{V_oT}{L_1}\frac{(6D-1)(7-12D)}{12(6D+1)}$$

$$\Delta I_{L1}=\frac{V_oT}{L_1}\frac{(6D-1)(7-12D)}{12(6D+1)} \tag{4.27}$$

The average current of each inductor must be one third of the average current in the load resistor, since the average capacitor current must be zero for steady-state operation.

$$I_{L1}=I_{L2}=I_{L3}=\frac{V_o}{3R} \tag{4.28}$$

The maximum and minimum values of the inductor current can be computed from Fig. 4.13

$$I_{L1\min}=\frac{V_o}{3R}-\frac{\Delta I_{L1}}{2}$$
$$=\frac{V_o}{3R}-\frac{1}{2}\frac{V_oT}{L_1}\frac{(6D-1)(7-12D)}{12(6D+1)} \tag{4.29}$$

$$I_{L1\max}=\frac{V_o}{3R}+\frac{\Delta I_{L1}}{2}$$
$$=\frac{V_o}{3R}+\frac{1}{2}\frac{V_oT}{L_1}\frac{(6D-1)(7-12D)}{12(6D+1)} \tag{4.30}$$

In order to ensure continuous inductor current, the value of $I_{L1\min}$ must be positive. Therefore, substituting $I_{L1\min}=0$ in equation (4.29) to find the critical value of output filter inductor.

$$L_{crit}=\frac{(6D-1)(7-12D)R}{8(6D+1)f_{sw}} \tag{4.31}$$

Where L_{crit} is minimum value of inductance for a given D, f_{sw}, and R, below which converter operates in discontinuous conduction mode of operation. Normally, the actual value of the inductor is selected 10 to 20 times higher than L_{crit}.

(b) Design of output capacitor

The interleaved operation of converter is useful for reducing the size of filter components. The current $\left(i_{L1}+i_{L2}+i_{L3}\right)$ enters at node of output capacitor and load resistance which has a smaller ripple and its frequency is three time of frequency of individual inductor currents / six time of switching frequency as shown in Fig.4.14. This yields a smaller peak-to-peak variation in output capacitor current than would be achieved without interleaved operation,and hence lesser value of capacitor is required for the same output ripple voltage.

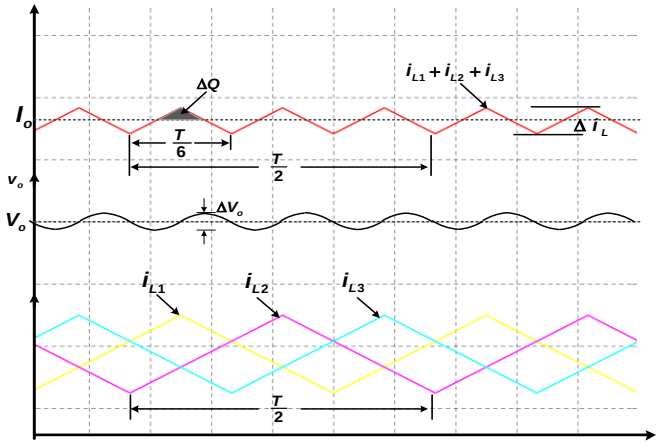


Fig.4.14 Voltage and current waveforms of output filter inductor during interleaved operation

The variation in output voltage & output voltage ripples is computed from the voltage-current relationship of the capacitor. The current in the capacitor is

$$i_{C_o}(t)=i_{L1}(t)+i_{L2}(t)+i_{L3}(t)-I_o \tag{4.32}$$

The change in charge ΔQ is the area of the triangle shown in the shaded portion of Fig.4.14,

$$\Delta Q=\frac{1}{2}\left(\frac{T}{12}\right)\left(\frac{\Delta i_L}{2}\right)=\frac{\Delta i_L T}{48} \tag{4.33}$$

When capacitor current is positive, the capacitor is charging. From the definition of capacitance,

$$Q=CV_o; \qquad \Delta Q=C\Delta V_o$$

$$\Delta V_o=\frac{\Delta Q}{C} \tag{4.34}$$

Substituting equation(4.33) in equation(4.34), yields

$$\Delta V_o=\frac{\Delta i_L T}{48C} \tag{4.35}$$

Simplifying equation(4.35), we get

$$\frac{\Delta V_o}{V_o}=\frac{T^2}{48CL_1}\frac{(6D-1)(7-12D)}{12(6D+1)} \tag{4.36}$$

In design, it is useful to rearrange the equation(4.36) to express required capacitance in terms of specified voltage ripple:

$$C = \frac{(6D-1)(7-12D)}{576L_1(6D+1)\frac{\Delta V_o}{V_o}f_{sw}^2} \tag{4.37}$$

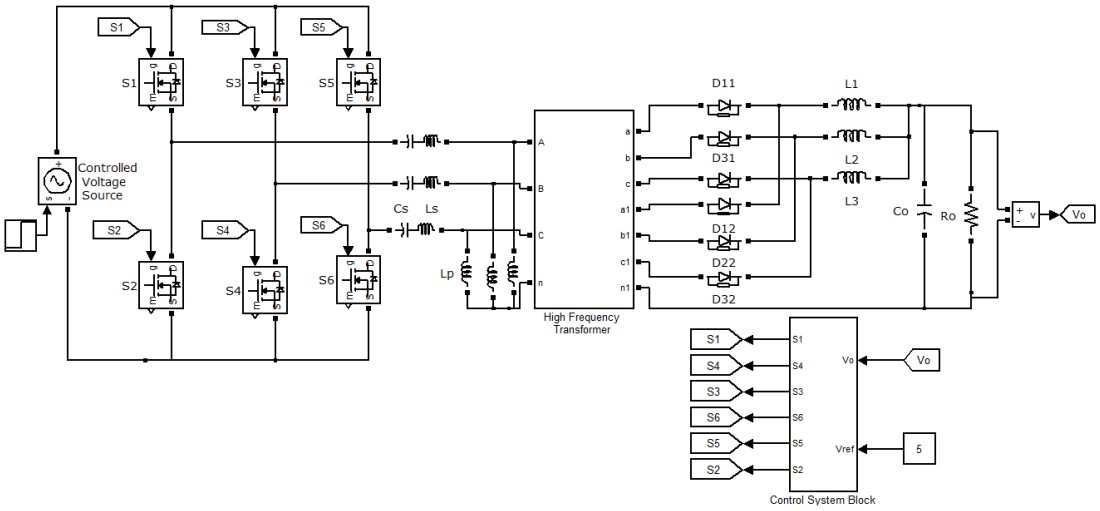
If the output voltage ripple is not large, the assumption of a constant output voltage is reasonable and the preceding analysis is essentially valid.

4.4 Simulation Studies

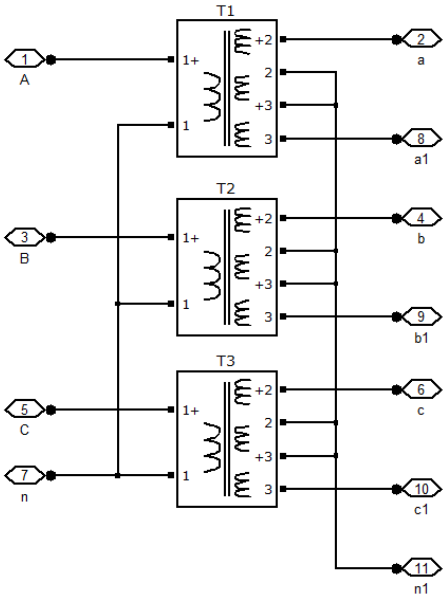
A Simulink model of three-phase isolated LLC DC-DC converter is developed with Simulink and SimPowerSystem^{TM} of MATLAB software. The system model consists of three main parts: input dc source, power circuit and control circuit as shown in Fig. 4.15. The input DC source is modelled with controlled voltage source of SIM power system toolbox library which converts the simulink input signal into an equivalent voltage source. The generated voltage of input DC source is driven by the input signal of the block. The three-phase inverter bridge is made of six MOSFETs and its internal body in parallel with the RC snubber circuit. Three units of two-winding transformer with centre-tapped secondary windings are connected as shown in Fig. 4.15(b). The six units of rectifier diodes(D_{11},D_{12},D_{21},D_{22},D_{31} and D_{32}) are connected as per connections shown in Fig. 4.15(a).

The output voltage controller is implemented for closed loop operation for the converters as in shown in Fig. 4.15(c) in which the converter output DC voltage is sensed and subtracted from an external reference voltage to obtain an error signal which is further processed through PI controller and the saturation block to obtain control voltage. The saturation block limits the control voltage less than 0.5 to avoid direct short circuit at the input side. The control voltage is compared with two saw-tooth waveforms which are phase shifted by 180^0 to generate gating pulses for two MOSFETs (S_1 and S_2). In order to generate gating signals for S_3 and S_4, the same control voltage is compared with two saw-tooth waveforms which are phase shifted by 120^0 and 300^0 with respect to first saw-tooth wave form. Similarly, gating signals for MOSFETs(S_5 and S_6) are derived as shown in Fig. 4.15(c).

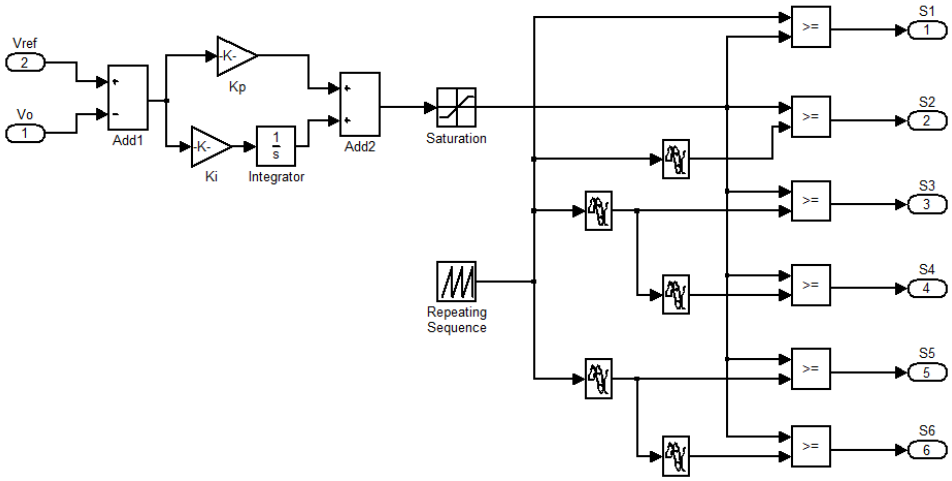
Thus, the voltage-mode control provides good regulation against variations in the load. The line regulation (regulation against variations in the input voltage) is, however, delayed because changes in the input voltage must first manifest themselves in the converter output before they can be corrected.



(a)



(b)



(c)

Fig. 4.15 Simulink model of three-phase LLC resonant DC-DC converter (a) Power circuit (b) Subsystem of HF transformer (c) Subsystem of control system block

Table 4.2 Parameters for Simulation Study

Parameters		Specification
Input voltage	V_{in}	660V, DC
Single-phase transformer	(T_1, T_2, T_3)	2000 VA, 400/25V ,10kHz, $R_m = 32k\Omega$, $L_m = 400\mu H$
Filter inductor	(L_1, L_2, L_3)	5μH
Output capacitor	C_o	1000μF
Resonant tank parameter	(L_s, L_p, L_{m1})	$L_s = 100\mu H$, $C_s = 100\mu F$ $L_{m1} = 250\mu H$
Switching Frequency	f_{sw}	10kHz
External Reference Voltage	$V_o(ref)$	5V
Voltage PI Controller	(K_p, K_i)	$K_p = 0.0125$, $K_i = 120$

4.4.1 Simulation Results & Discussion

A 5kW, 5V/1000A simulink model of three-phase, high frequency isolated LLC resonant DC-DC converter is developed using Simulink and SimPowerSystem™ of MATLAB software and its performance is studied under different operating conditions. Based on analysis of the converter, various circuit parameters are selected for simulation studies of converter as given in Table 4.2.

The simulation results obtained for three-phase, high frequency isolated LLC resonant DC-DC converter at different loads(100%, 90% and 60% of full load) with input DC voltage varies from 550V to 650V are shown in Fig.4.16 to Fig. 4.26. The output voltages $(v_{AB}, v_{BC}, \& v_{CA})$ of front end converter with input DC voltage $V_{in} = 600V$ are shown in Fig.4.16. it is observed that these voltages are symmetrically phase shifted by 120^0. Fig.4.17 shows steady state waveforms of phase voltages $(v_{An}, v_{Bn} \& v_{Cn})$ and primary side line currents $(i_A, i_B \& i_C)$ of front end converter, when it operates in region (Reg3) and delivers full load with the input DC voltage, $V_{in} = 600V$. It is observed that the primary currents lag with concerned voltages and hence ensures conduction of body diode of power switches prior to turning ON of switches. Fig.4.18 shows the steady state waveforms of currents $(i_{D11}, i_{D12}, i_{D21}, i_{D22}, i_{D31} \& i_{D32})$ through rectifier diodes which indicates that the peak current is one third of the full load current. It is further observed that two rectifier diodes connected to centre-tapped secondary windings of same transformer are conducting simultaneously, when voltage appears across its primary winding is zero. Thus, during this period, concerned

output inductor freewheels through these diodes and hence rate of rise of current reduced considerably.

Fig.4.19 illustrates the voltage across the output filter inductors under steady state conditions. The ringing in voltage waveforms of inductors are due to leakage inductance of transformer and output inductors. From Fig. 4.20, it is observed that each inductor shares one third of load current and individual inductor current ripple is large. The ripple content in load current is significantly reduced due to equal phase shift PWM control of converter, as shown in Fig. 4.20.

The performance of converter is investigated in view of application requirements such as accurate and stable output voltages, better line and load regulation, fast transient response, and safety measures. To investigate the performance of the converter with respect to line and load variations, the step change in load current from 600A to 900A at instant $t = 0.06$ sec and from 1000A to 600A at $t = 0.03$ sec ; furthermore, step change in input DC voltage (V_{in}) from 600V to 650V at $t = 0.015$ sec and from 650V to 550V at $t = 0.08$ sec, are incorporated. From Fig. 4.21 and Fig. 4.22, it is observed that output inductors $(L_1, L_2 \& L_3)$ share one-third of load current irrespective of line and load variations. Though, small disturbance in inductor currents is observed which die out in less than 0.001 sec. It is further observed that irrespective of variations in input voltage and load, the output DC voltage of converter resumes its reference voltage of *5V* after few disturbances as depicted in Fig. 4.26. The output DC voltage waveform of converter with various controller parameters has been simulated and it is observed that delay in elimination of disturbances can also be optimized by proper tuning of controller parameters. The transient response of converter under aforementioned line and laod variations with one set of controller parameter($K_P = 0.0125$, $K_I = 120$) are shown in Fig. 4.23 to Fig. 4.26. It is observed that output DC voltage resumes its reference voltage in less than 0.001 sec. The performance of the converter is found to be as per design and satisfactory.

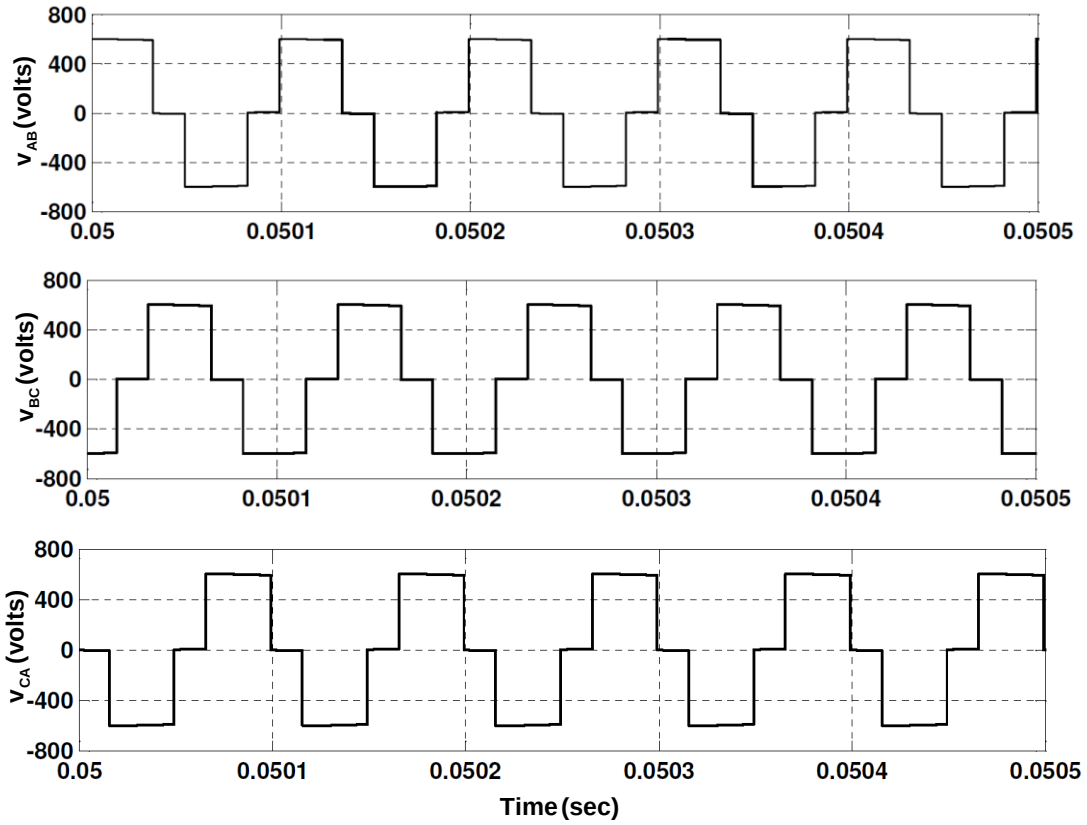


Fig.4.16 Output line voltages $(v_{AB}, v_{BC} \& v_{CA})$ of front end converter with $V_{in} = 600V$

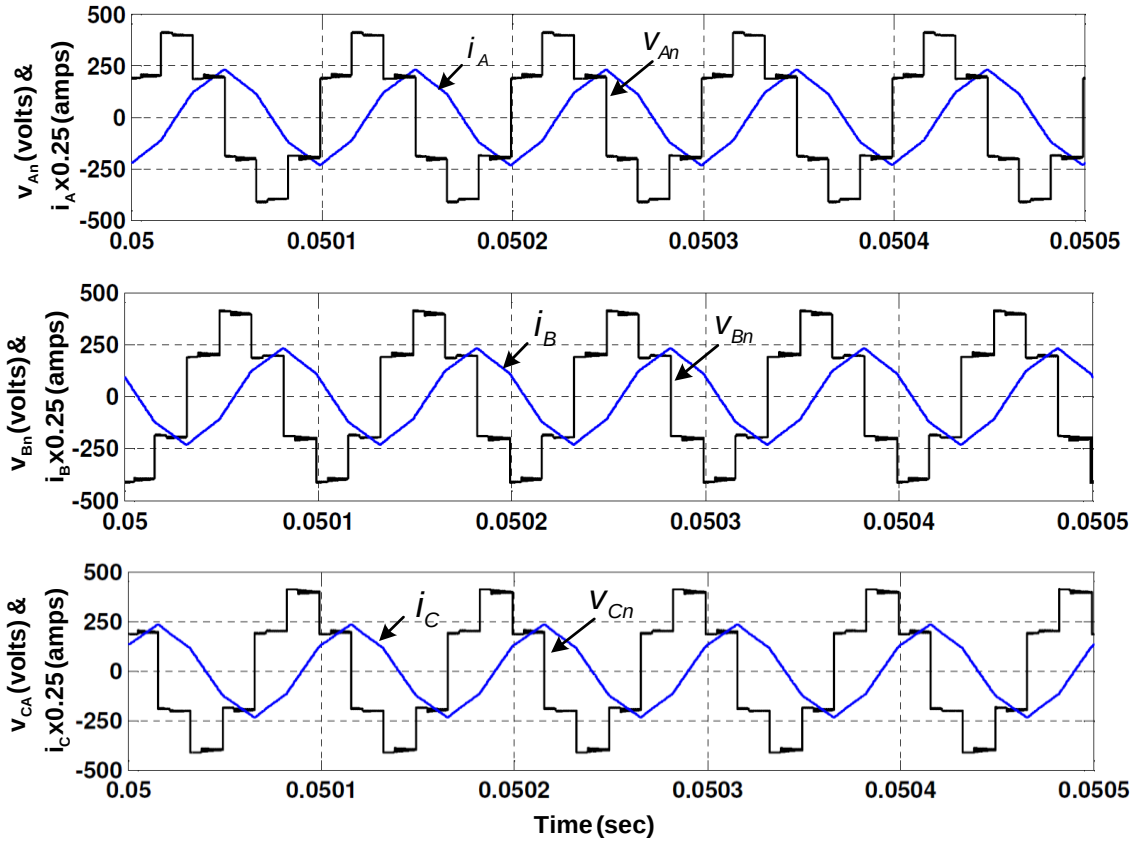


Fig.4.17 Phase voltages $(v_{An}, v_{Bn} \& v_{Cn})$ and primary line currents $(i_A, i_B \& i_C)$ with input DC voltage $V_{in} = 600V$

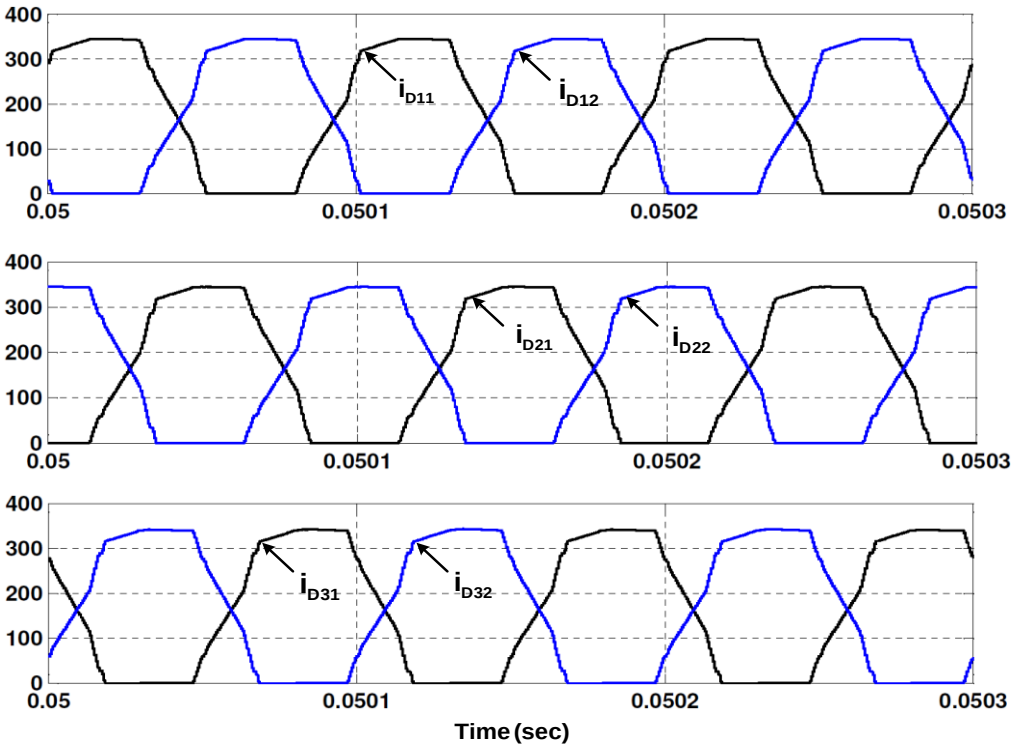


Fig.4.18 Rectifier diode currents waveforms $i_{D11}, i_{D12}, i_{D21}, i_{D22}, i_{D31}$ & i_{D32} (*amps*) at full load

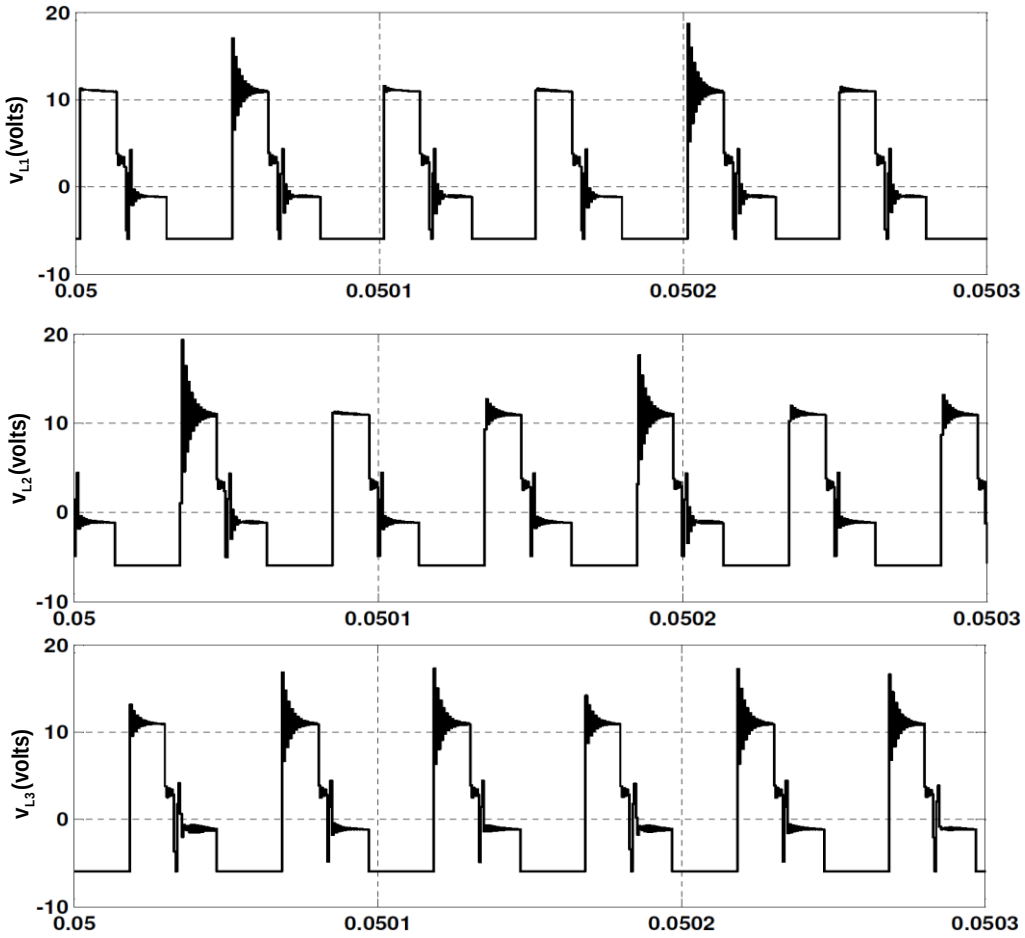


Fig.4.19 Voltage waveforms of output filter inductor $(v_{L1}, v_{L2}$ & $v_{L3})$

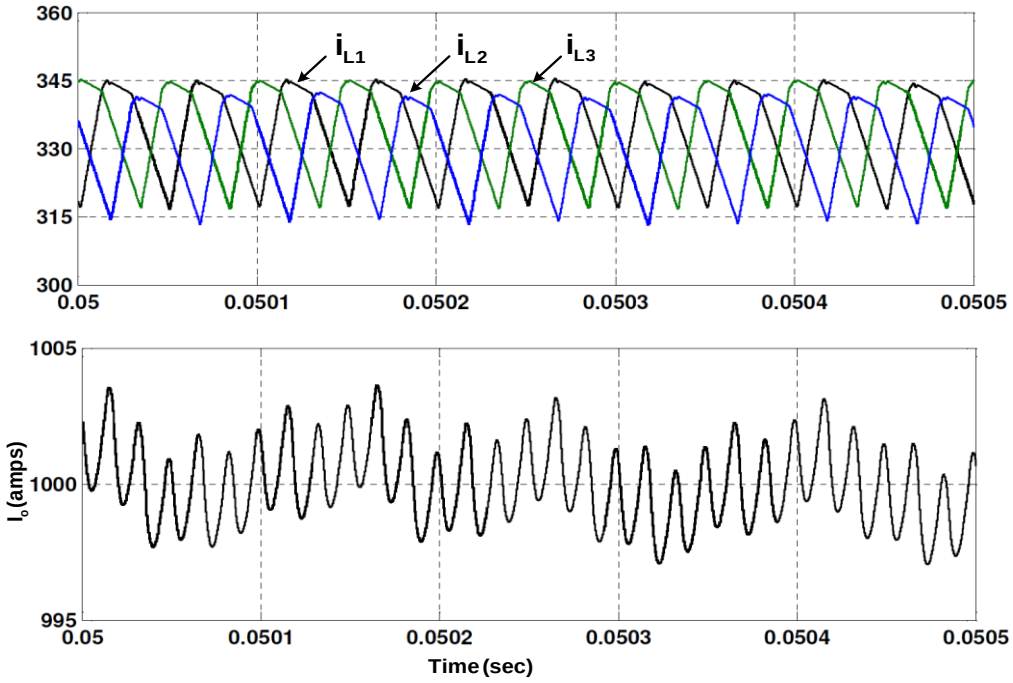


Fig. 4.20 Output filter inductor currents i_{L1}, i_{L2} & $i_{L3}(amps)$ and load current (I_o) waveforms

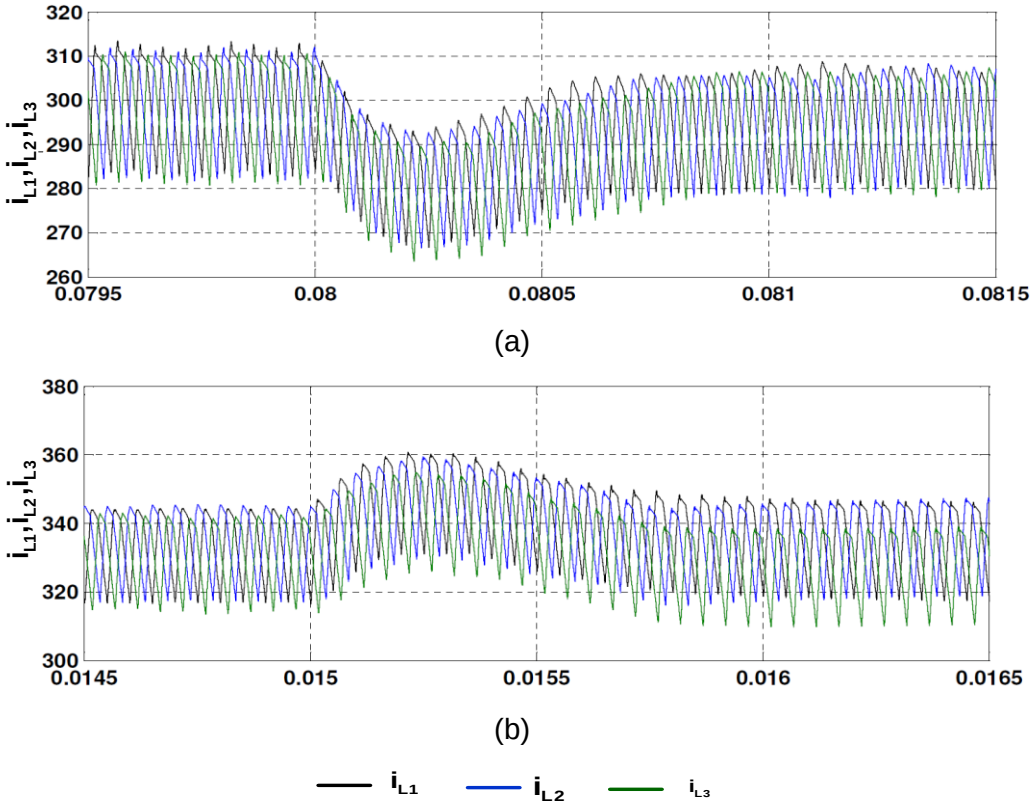
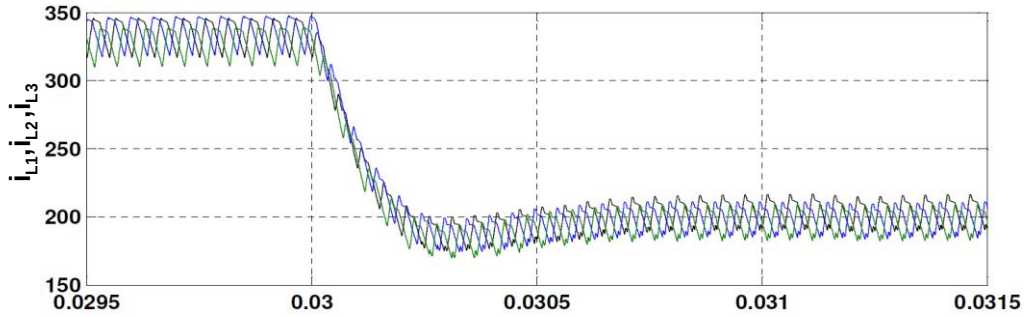


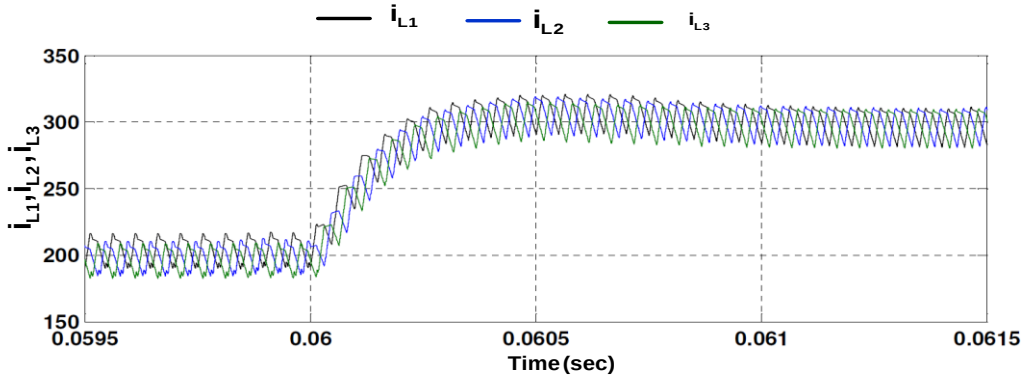
Fig. 4.21 Output inductor current waveforms during input voltage variations

(a) Decrease in voltage from 650V to 550V at 0.008 sec

(b) Increase in voltage from 600V to 650V at 0.015 sec



(a)



(b)

Fig. 4.22 Output filter inductor current against load variations

(a) Decrease in load current from 1000A to 600A at 0.03 sec

(b) Increase in load current from 600A to 900A at 0.06 sec

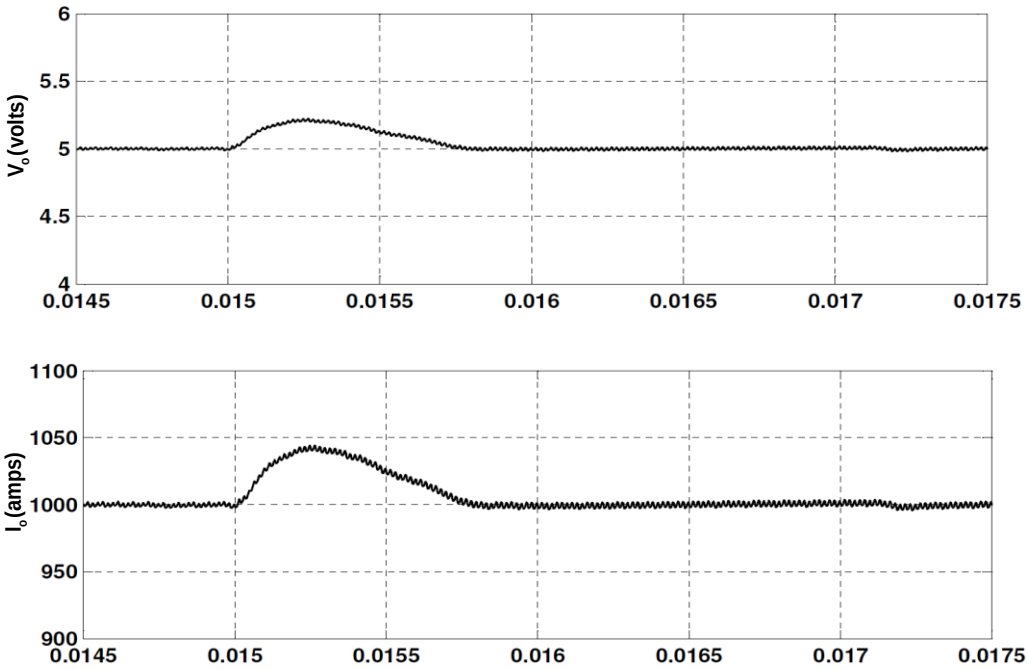


Fig. 4.23 Output voltage and load current variations against increased in input voltage from 600V to 650V at 0.015 sec

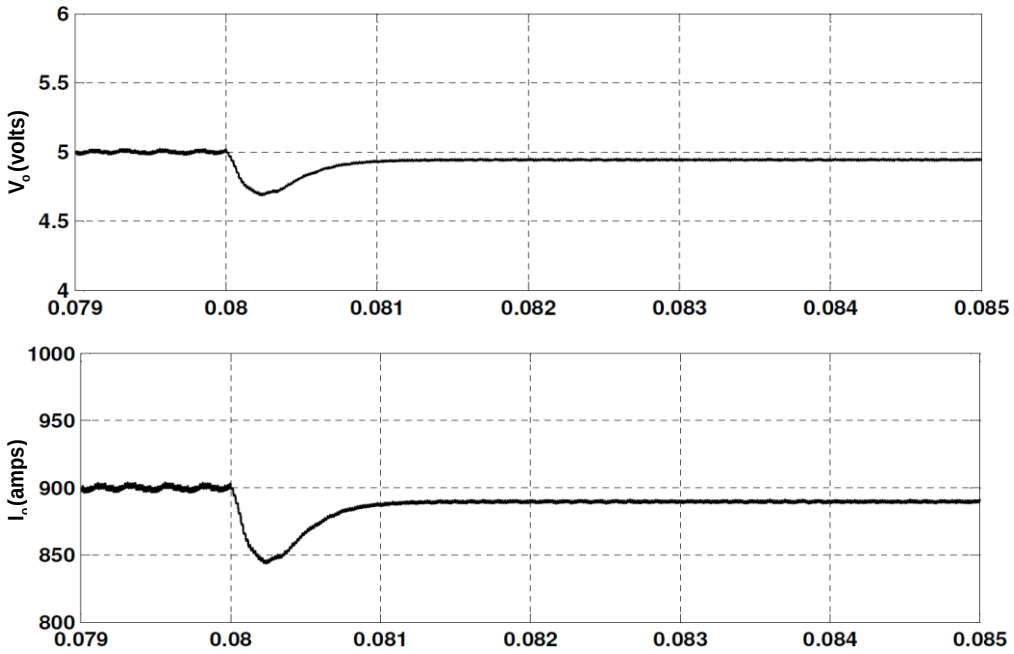


Fig. 4.24 Output voltage and load variations against decreased in input voltage from 650V to 550V at 0.008 sec

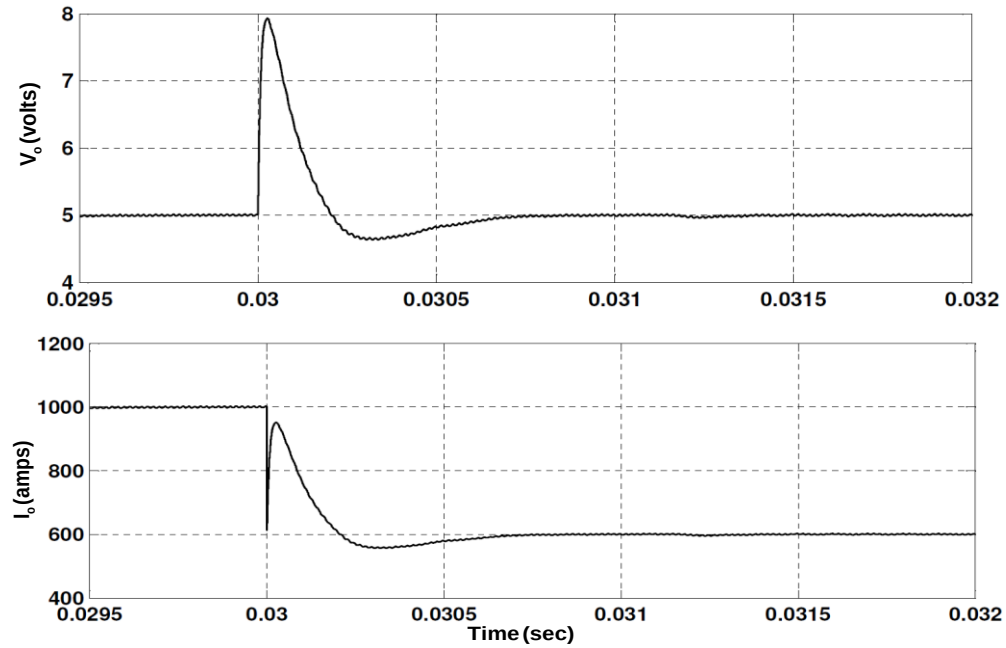
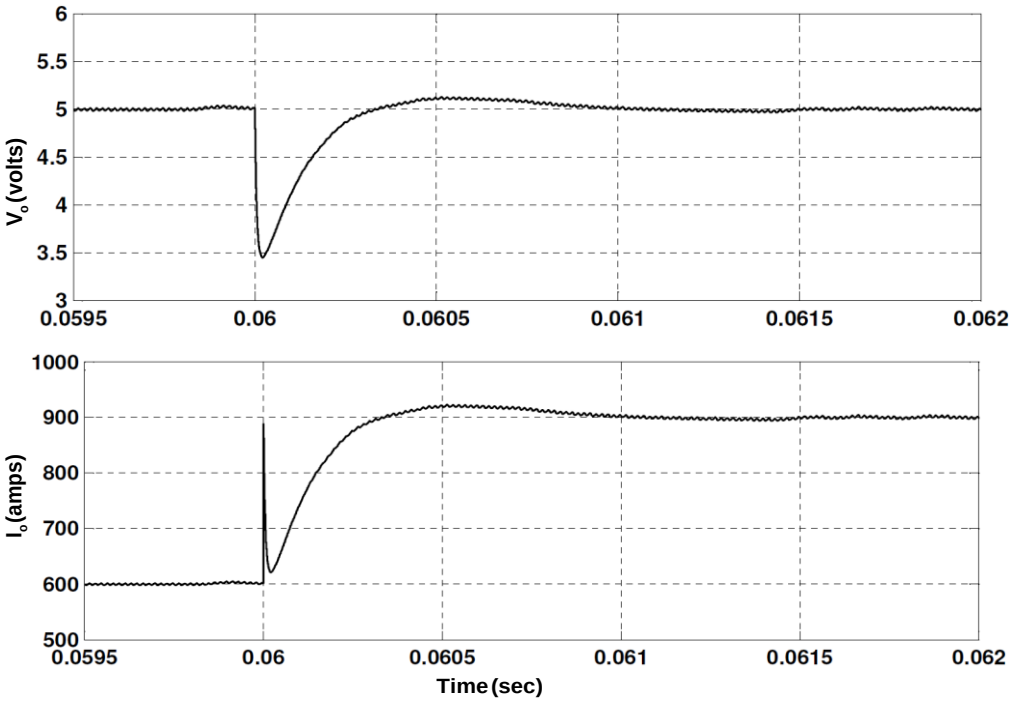


Fig. 4.25 Output voltage and load current variations against decreased in load current from 1000A to 600A at 0.03 sec



(b)

Fig. 4.26 Output voltage and load current variatons against increased in load current from 600A to 900A at 0.06 sec

Table 4.3 Components used in Prototype Model (75W, 1.5V/50A)

Parts	Items	Quantity	Components /Rating
Input voltage	V_{in}	1	220V, DC
Power switches	$(S_1 - S_6)$	6	IRFP 460A
Rectifier diodes	$(D_1 - D_6)$	6	25D40R
Single-phase Transformer	(T_1, T_2, T_3)	3	250 VA, E65ferrite core, Turns ratio-209/12/12,
Filter inductor	(L_1, L_2, L_3)	3	EE65 ferrite core, 5mH
Output capacitor	C_o	1	Electrolyte, 1000µF, 50V
Digital Signal Processor	-	1	DSP DS1104

4.5 Experimental Validation

4.5.1 A Prototype Model of Proposed Converter

In simulation studies presented in previous section, three-phase high frequency isolated LLC resonant DC-DC converter, rated at 5 kW, 5V/1000A is realised with symmetrical PS-PWM method. But due to the practical constraints, a 75 W, 1.5V/50A prototype proposed model is built with the specifications given in Table 4.3. As the experimental studies are conducted at a reduced rating of converter, for validating the experimental results, the simulation studies are also carried out with reduced rating of converter. The power circuit of front end converter consists of six switches $(S_1 - S_6)$ with anti-parallel diodes. The MOSFETs IRFP460A with built-in fast recovery diodes are used as switching devices with protected by designed snubber circuits. The three units of single-phase transformers with centre-tapped secondary windings are fabricated using EE65 ferrite core, primary winding of 209 turns with 19 SWG Cu wire and secondary windings of 12-12 turns with 17 SWG Cu-wire. The leakage inductance and magnetizing inductance of transformer are selected with maintaining suitable air-gap length in magnetic core so-that the designed value of resonant tank parameters can be achieved. The output filter inductors (L_1, L_2, L_3) and output capacitor (C_o) should be large enough to smooth out ripples at switching frequency (1kHz) and maintaining continuous current conduction. Interleaved symmetrical controlled method is employed to reduce size of filter components to maintain same amount of ripple.

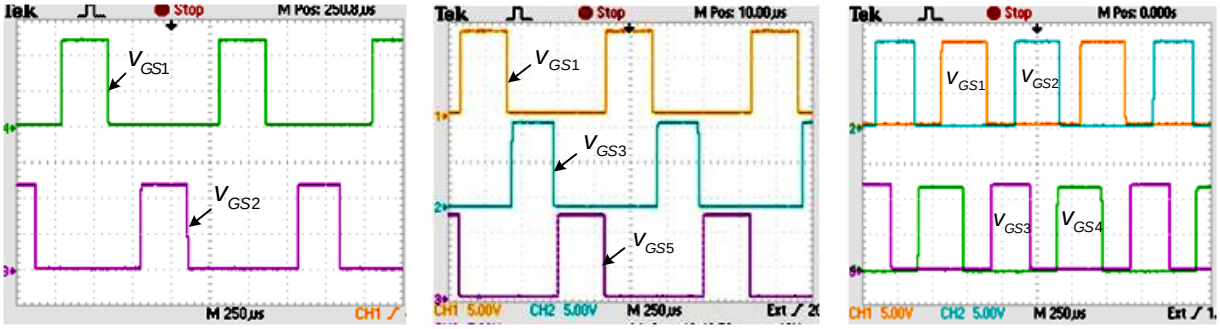
A DSP DS1104 of dSPACE is used for the real-time implementation of control algorithms. The control algorithm is first designed in the MATLAB SIMULINK software and the Real-Time Workshop of MATLAB automatically generates the optimized C-code for real-time implementation. The interface between MATLAB and Digital Signal Processor (DSP, DS1104 of dSPACE) allows the control algorithm to run on the hardware, which is an MPC8240 processor. The master bit I/O is used to generate the required six gate pulses and one analog to digital converter (ADC) to implement close loop control. Switching signals obtained from the controller are given to the driver circuit of power MOSFETs $(S_1 - S_6)$.

4.5.2 Experimental Results and Discussions

A *75W*, 1.*5V*/50*A* prototype high frequency isolated LLC DC-DC converter is built with specifications: input DC source $(V_{in} = 220V \pm 10\%)$, three units of single-phase high frequency transformer $(250VA, 150V / 15 - 15V)$ with centre-tapped secondary windings and tested under various operating conditions.

(a) Steady State Performance

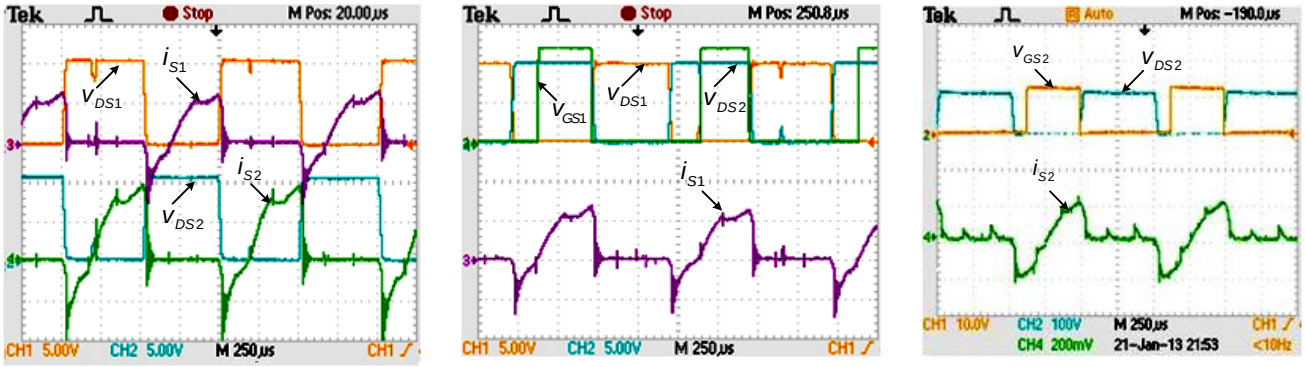
The Simulink model of the symmetrical PS-PWM control scheme for converter is implemented using dSPACE-DS1104 controller. The generated firing pulses are given to corresponding semiconductor devices of front end converter through pulse isolation and amplifier circuit in real-time. The experimentally obtained firing signals (gate to source voltage) across MOSFETs $(S_1 - S_6)$ are shown in Fig. 4.27, which indicates that each of front end converter operates in interleaved manner.



(a) (b) (c)

$(v_{GS}: 5V/div, X-axis: 250\,\mu s/div)$

Fig. 4.27 Gate to source voltages of MOSFETs (a) v_{GS1}, v_{GS2}, (b) v_{GS1}, v_{GS3}, & v_{GS5} (c) v_{GS1}, v_{GS2}, v_{GS4},& v_{GS3}.



(a) (b) (c)

$(v_{DS1}\&v_{DS2}: 100V/div, i_{S1}\&i_{S2}: 2A/div, v_{GS1}\&v_{GS2}: 5V/div, X-axis: 250\,\mu s/div)$

Fig. 4.28 Voltage and current of power switches of front end converter (a)v_{DS1}, v_{DS2}, i_{S1},& i_{S2}, (b) v_{DS1},v_{DS2}, i_{S1},& v_{GS1},(c) v_{GS2}, v_{DS2}, & i_{S2}

Fig. 4.28 shows the experimentally obtained voltage and current associated with MOSFETs (S_1, S_2) of front end converter which indicates that prior to turn ON either S_1 or S_2, the concerned body diode of S_1, S_2 are conducted and hence zero voltage switching for these switches are achieved, which can also be validated through simulation results of reduced raing of converter as shown in Fig.4.29 : scale for switch current: i_{sw} x0.1.

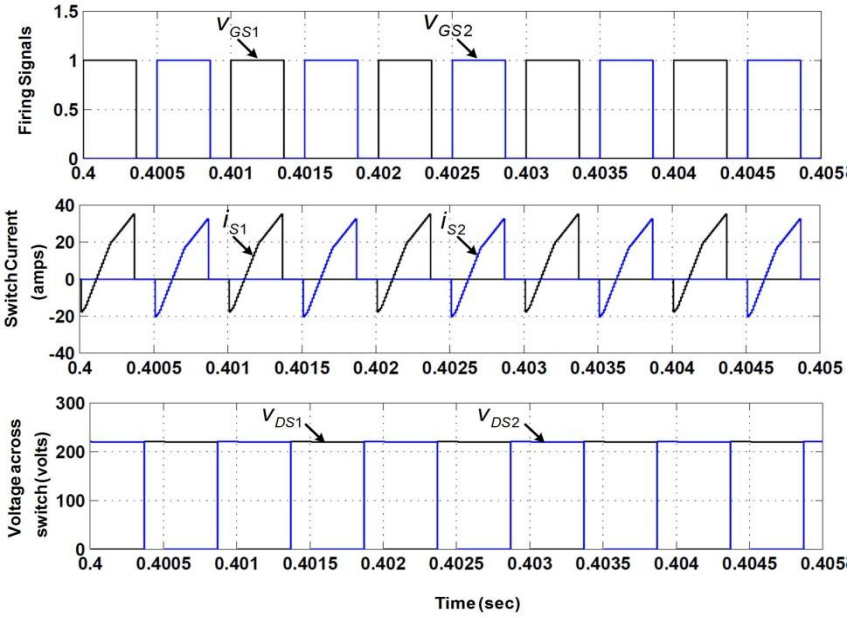
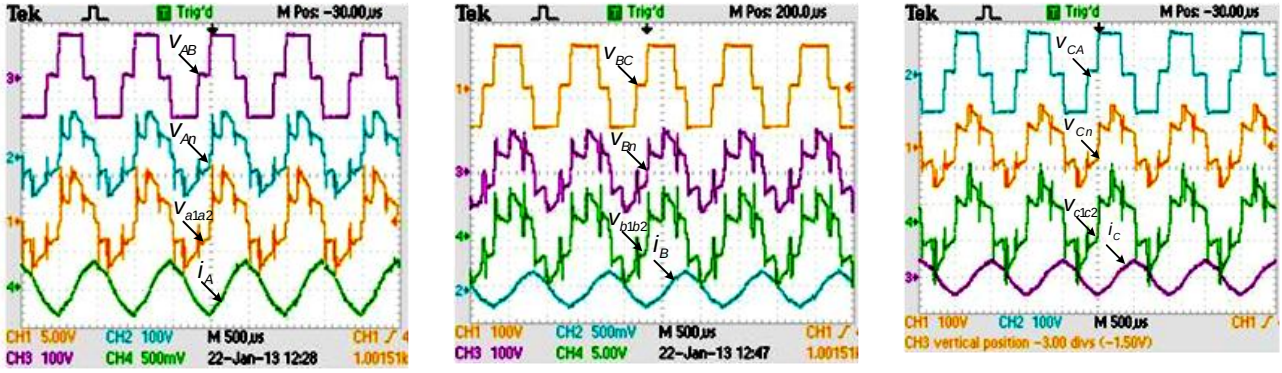


Fig.4.29 Simulated voltage and current waveforms of power switches (S_1, S_2)

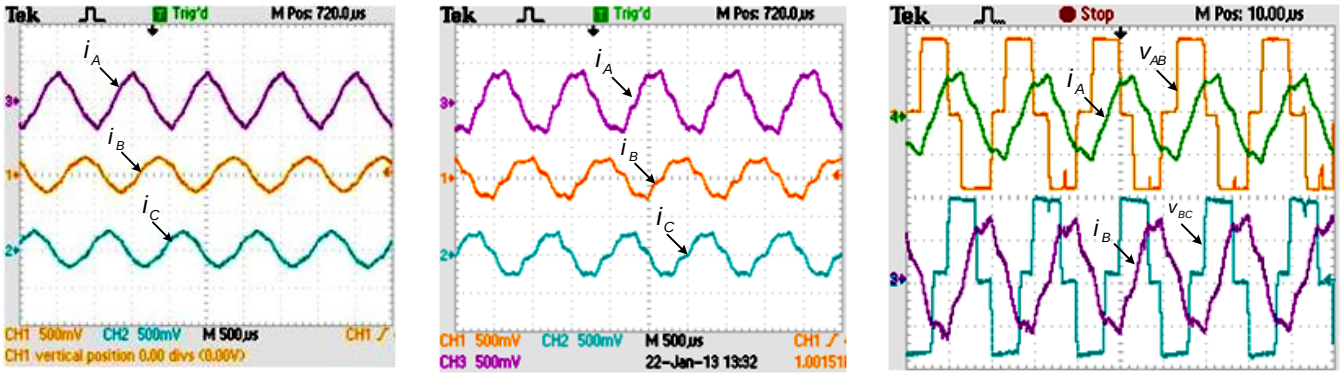
Fig.4.30 to Fig.4.32 illustrate the experimentally obtained line to line voltages (v_{AB}, v_{BC}, v_{CA}) , line to neutral volatges (v_{An}, v_{Bn}, v_{Cn}), centre-tapped secondary-side voltages (v_{a1a2}, v_{b1b2} &v_{c1c2}) and primary side line currents (i_A, i_B, i_C) with 20% and 50% of full load current. The most notably, the primary voltages are phase-shifted by 120^0 and currents $(i_A, i_B \,\&\, i_C)$ are sinusoidal over a wide range of load as depicted in Fig.4.31 and Fig.4.32.



(a) (b) (c)

$(v_{AB}, v_{BC} \,\&\, v_{CA} : 100V/div, i_A, i_B \,\&\, i_C : 2A/div, v_{a1a2}, v_{b1b2}, \&\, v_{c1c2} : 10V/div, X-axis : 500\,\mu s/div)$

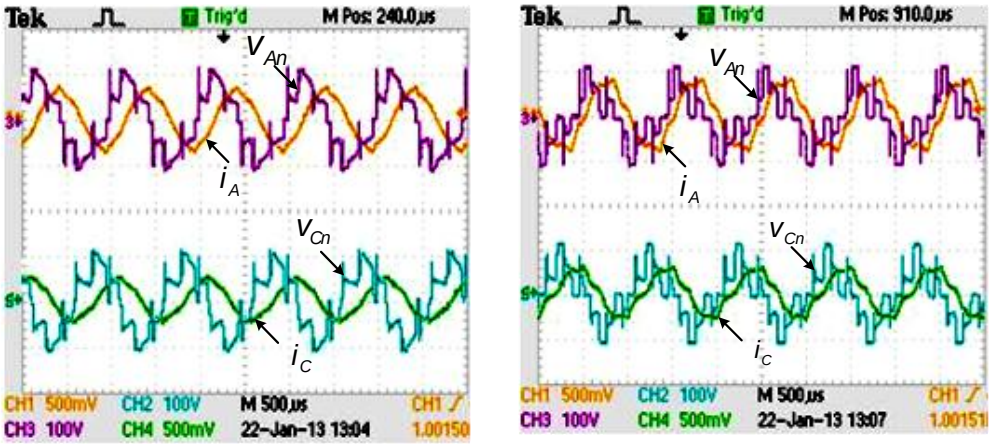
Fig.4.30 Voltage and current waveforms of transformer (a) v_{AB} ,v_{An} ,v_{a1a2} & i_A (b) v_{BC},v_{Bn},v_{b1b2}, & i_B (c) v_{CA},v_{Cn},v_{c1c2}, & i_C



(a) (b) (c)

$$(v_{AB}, v_{BC} \& v_{CA} : 100V/div, i_A, i_B \& i_C : 2A/div, X-axis : 500\,\mu s/div)$$

Fig.4.31 Primary side line current(i_A, i_B, i_C) waveforms of transformer at (a) 20% load (b) 50% load (c) line voltage & current at 50% load conditions

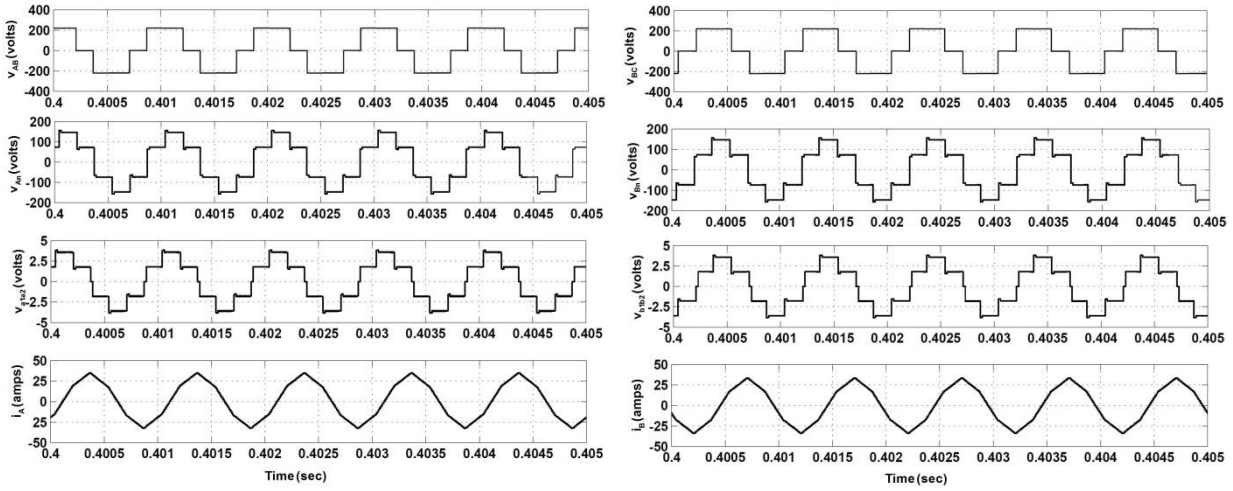


(a) (b)

$$(v_{An}, v_{Bn} \& v_{Cn} : 100V/div, i_A, i_B \& i_C : 2A/div, X-axis : 500\,\mu s/div)$$

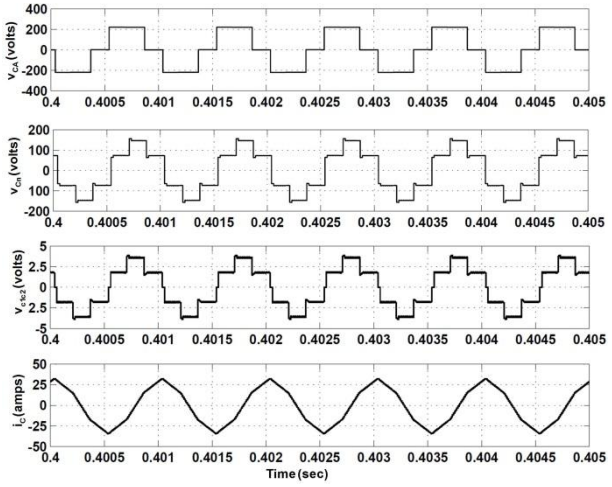
Fig.4.32 Primary side phase voltage (v_{An}, v_{Cn}) and line current (i_A, i_C) waveforms at (a) 20% load (b) 75% load

Furthermore, it is observed that the primary side line currents lag with the respective phase voltages of the transformers over a wide range of load variations, and hence ZVS condition is ensured for a wide range of load variation. For validation, the simulation results obtained with simulink model of reduced rating of converter are shown in Fig. 4.33.

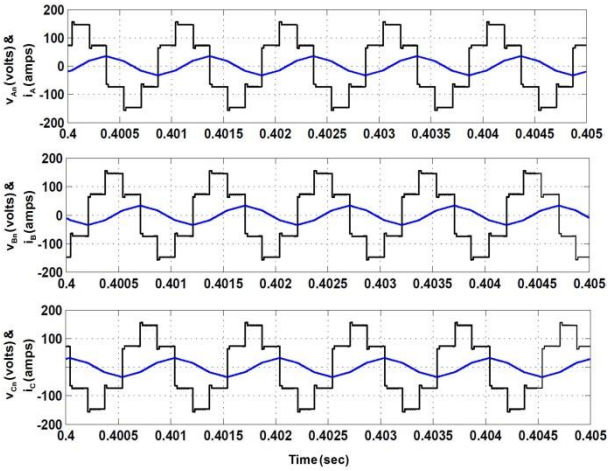


(a)

(b)



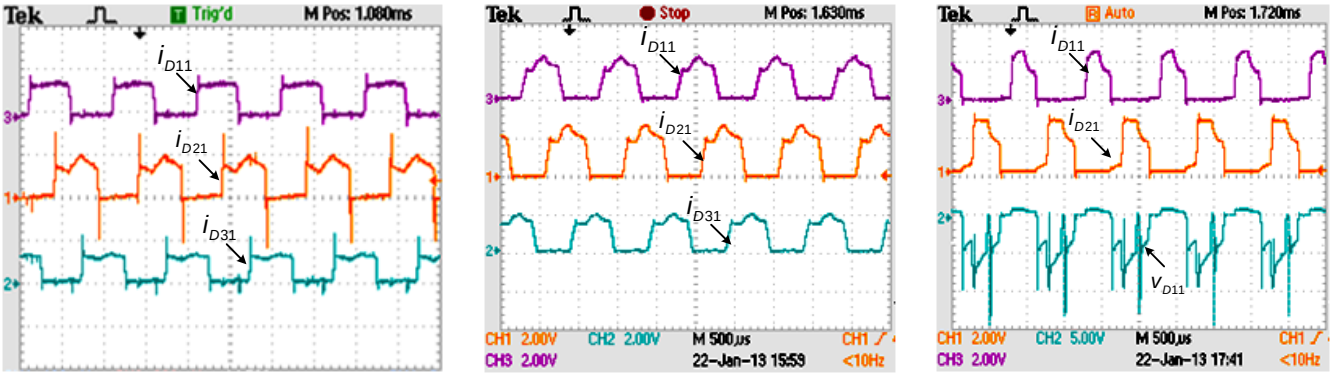
(c)



(d)

Fig. 4.33 Simulation results of three-phase high frequency isolated LLC resonant DC-DC converter (a) v_{AB} ,v_{An} ,v_{a1a2} & i_A (b) v_{BC},v_{Bn},v_{b1b2}, & i_B (c) v_{CA},v_{Cn},v_{c1c2}, & i_C (d) phase voltages (v_{An},v_{Bn}& ,v_{Cn}) and line current (i_A , i_B & i_C)x0.1

Fig. 4.34 and Fig. 4.35 show experimental and simulation waveforms of rectifier diode currents, which indicate that peak current is reduced to 1/3 times of full load and average current of rectifier diodes is reduced significantly. As current in rectifier diodes is reduced, it helps in better thermal heat dissipation. Fig. 4.36 illustrates the voltage and current associated with output filter inductors which indicates that ripple content in each inductor current is large.



(a) (b) (c)

$(v_{D11}: 20V/div, i_{D11}, i_{D21} \& i_{D31}: 8A/div, X-axis: 500\,\mu s/div)$

Fig. 4.34 Rectifier diodes current (i_{D11},i_{D21},& i_{D31}) waveforms at (a) 20% load (b) 50% load (c) voltages across the diode (v_{D11})

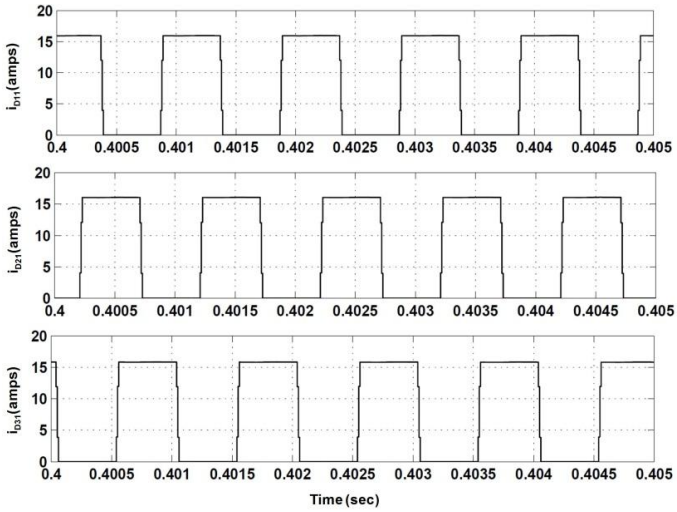
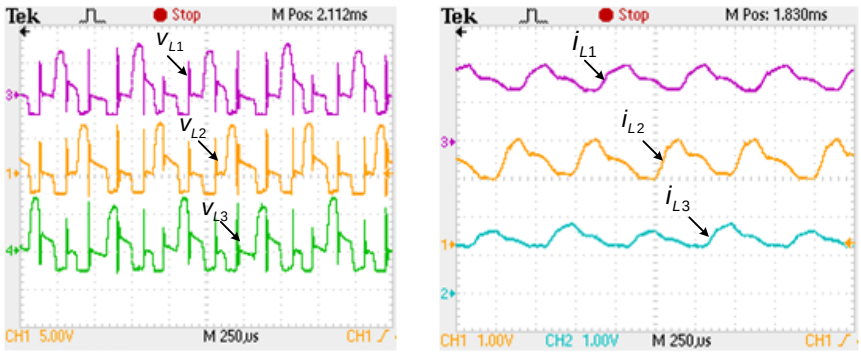


Fig. 4.35 Simulated rectifier diode currents $(i_{D11}, i_{D21} \& i_{D31})$ with reduced equivalent model of converter

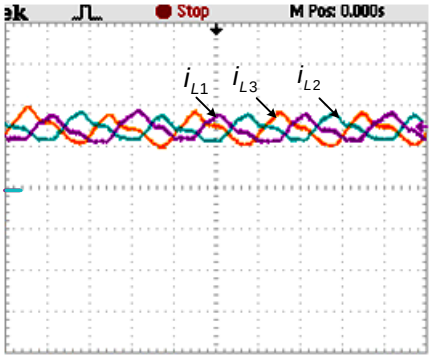


(a) (b)

$(v_{L1}, v_{L2} \& v_{L3}: 50V/div, i_{L1}, i_{L2} \& i_{L3}: 8A/div, X-axis: 250\,\mu s/div)$

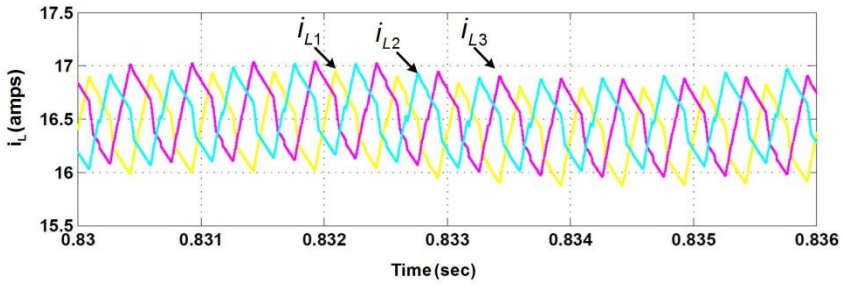
Fig. 4.36 Voltage and current waveforms of output filter inductors (a) v_{L1}, v_{L2},& v_{L3} (b) i_{L1},i_{L2},& i_{L3}

But, due to interleaved operation, the ripple in load current of converter is reduced by the ripple cancellation and hence size of output capacitive filter is reduced. This can also be validated in inductor current waveform obtained with simulink model of reduced rating of converter.



$(i_{L1}, i_{L2} \& i_{L3} : 8\,A/div\,, X-axis : 250\,\mu s/div)$

(a)



(b)

Fig. 4.37 Output inductor current waveforms (a) Experimental (b) Simulation

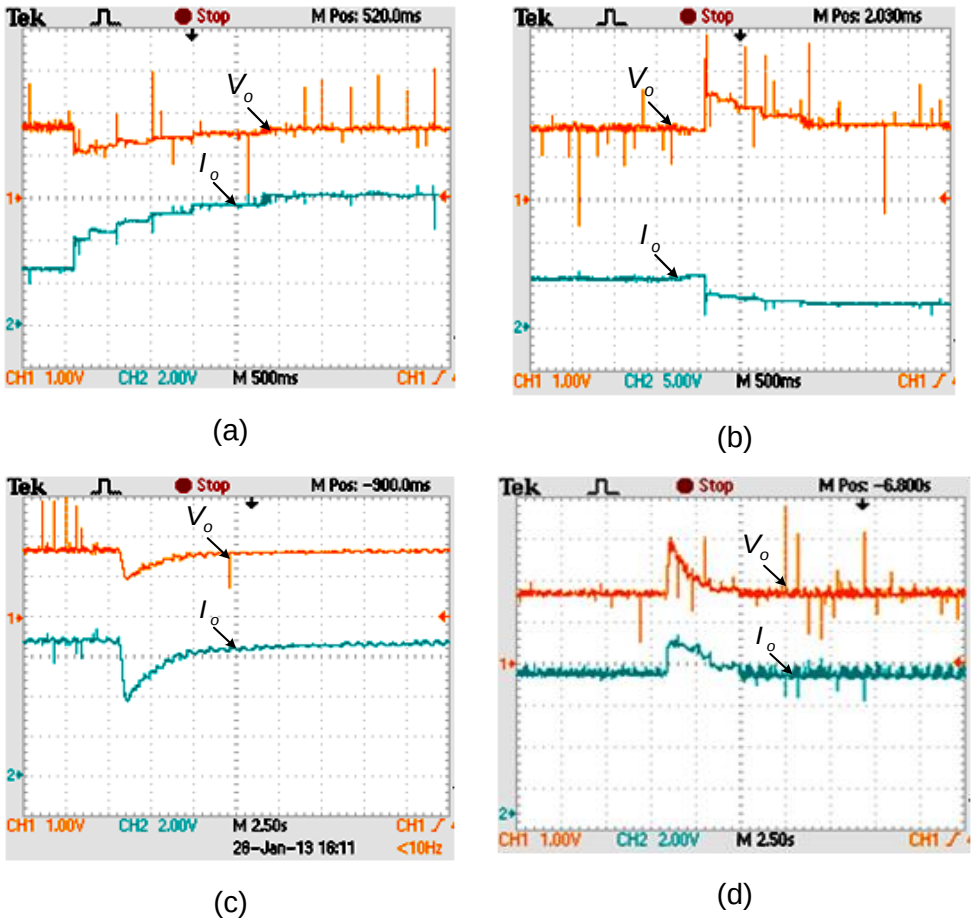
(b) Transient Performance

The transient performance of the prototype model is studied with step increase and decrease in input voltage and load current.

Fig. 4.38 shows the experimental results of output voltage and load current with different step change in input voltage and load current. In Fig. 4.38(a) the load current is increased from 20% to 50% of full load current with input voltage 220V, the corresponding change in ouput voltage is observed. It is also observed that output voltage resumes its previous value of 1.5V after 2.5 sec. In Fig. 4.38(b), the load current is decreased from 20% to 10% of full load and corresponding change in output is observed. It is observed that output voltage retains its reference value irrespective of load variation. To validate the performanace under transient conditions, similar study change in the reduced rating of Simulink model of converter has been and obtained simulation results are presented in Fig. 4.39 (a) and (b).

To investigate the performance under input voltage variations, sudden decrease from 220V to 170V and sudden increase from 200V to 220V are done and corresponding change

in output voltagein is observed as shown in Fig. 4.38 (c) and Fig. 4.38(d). It is found that irrespective of input voltage variations, the output voltage of converter remains its reference value after some delay from the point of disturbance. It is observed that this disturbances can be reduced with proper tuning of PI controller. To validate the performance of converter against input voltage variations, the input voltage is increased from 200V to 220V at $t = 0.45$ sec and decreased from 220V to 180V at $t = 0.75$ sec and corresponding change in output voltage of Simulink model are observed and obtained simulation results are presented in Fig. 4.39 (c) and Fig. 4.39(d). The comparison of experimental and simulation results under different operating conditions are summarized in Table 4.4.



$(V_o : 1V/div, I_o : 8A/div)$

Fig. 4.38 Transient response of converter (a) Increase in load from 20% to 50 % of full load (b) Decrease in load from 20% to 10 % of full load (c) Decrease in supply from 200V to 170V DC (d) Increase in supply from 200V to 220V

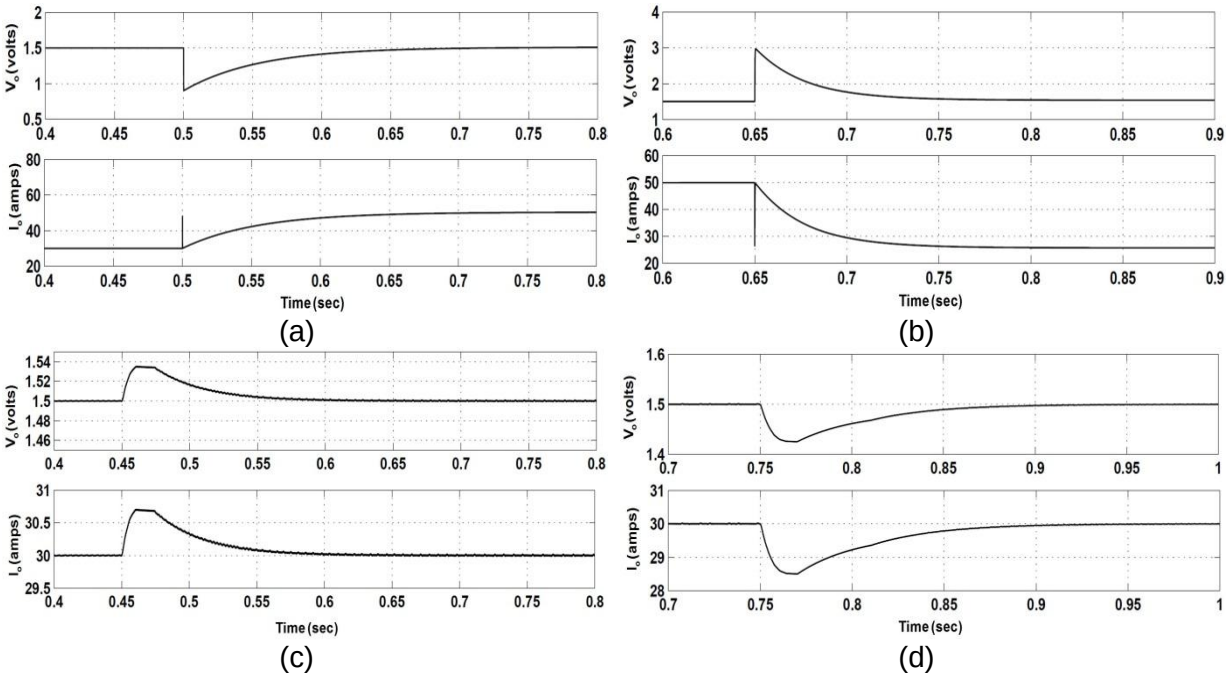


Fig. 4.39 Simulation results under various perturbations (a) increase in load from 60% to 100 % of full load (b) decrease in load from 100% to 50 % of full load (c) increase in V_{in} from 200V to 220V DC (d) decrease in V_{in} from 220V to 180V

Table 4.4 Comparison of experimental and simulation results with different operating conditions

Parameter		25% of full load		50% of full load		100% of full load	
		Exp.	Simulation	Exp.	Simulation	Exp.	Simulation
Output voltage (volts)		1.5	1.5	1.5	1.5	1.5	1.5
Load current (amp)		12.5	12.5	25	25	50	50
Output Inductor current (amps)	I_{L1}	4.1	4.16	8.21	8.33	16.64	16.71
	I_{L2}	4.0	4.16	8.15	8.33	16.64	16.64
	I_{L3}	3.9	4.16	8.20	8.33	16.63	16.65
Rectifier diode current (amps)	I_{D11}	2.15	2.20	4.40	4.40	8.30	8.35
	I_{D21}	2.15	2.20	4.15	4.15	8.31	8.35
	I_{D31}	2.15	2.20	4.04	4.04	8.32	8.35
Settling time (sec)		-	0.15	-	0.15	-	0.15
% Rise/ Fall in V_o during change in V_{in} from 220V to 180V & vice-versa		-	6.67%	-	6.67%	44.44%	6.67%
Sampling time		30 µsec	1µsec	30 µ sec	1µsec	30 µ sec	1 µsec

4.6 Conclusion

In this chapter three-phase, high frequency isolated LLC resonant DC-DC converter is proposed. To study the performance, a 5 kW, 5V/1000A Simulink model of proposed converter is developed and operated under interleaved PWM control. This chapter is summarized as follows:

- A three-phase, high frequency isolated resonant DC-DC converter is proposed which suitable for medium power applications such as telecommunication and computer industries.
- The mathematical modelling of proposed converter is carried out under different operating modes.
- The parameters of the LLC resonant tank are derived from per phase model of the proposed converter and its design equations: converter voltage gain, voltage stress across resonant inductor, voltage stress across resonant capacitor and inductor current are derived and design curves are plotted against normalized frequency for various loading conditions(Q).
- Based on mathematical analysis, the designed values of LLC resonant tank, output filter inductors and capacitor are selected. The parameter of leakage and magnetizing inductances of transformers are adjusted using airgap length to match with designed values of LLC resonant tank. It is observed that leakage and magnetizing inductances of transformers along with snubber capacitances are sufficient to achieve ZVS for power switching device over a wide range of load variations.
- To investigate the performance of proposed converter, extensive simulation studies with 5kW, 5V/1000A Simulink model under symmetrical interleaved PWM control method are carried out and simulation results are presented under steady-state and transient conditions.
- Based on mathematical analysis, a prototype model of reduced rating is developed and tested under various operating conditions in laboratory. Experimental results under steady state and transient state are presented. To validate the experimental results, Simulink model of proposed converter of reduced equivalent rating is developed and simulation results are presented.
- Output DC voltage of converter resumes its reference value (1.5V) during input voltage and load variations after 5 sec and 2.5 sec respectively.
- The measured efficiency of the converter with full load condition is found to be 85%.
- The issues of over current cause by overload or short circuit condition, or the inrush current during startup are to be addressed so that the power converter can be well protected against damage under those conditions.

CHAPTER 5: THREE-PHASE ISOLATED DC-DC CONVERTER WITH THREE-PHASE RECTIFICATION

[This chapter deals with modeling, control and design of three-phase, high frequency isolated, DC-DC converter operated under symmetrical control and asymmetrical control with fixed frequency operation. The steady state analysis is presented according to the description of the operational stages of the converter. In order to investigate the performance, the simulation study is carried out using the SimPowerSystem™ and Simulink toolbox of MATLAB software. Based on mathematical analysis, a prototype model is developed and tested under various operating conditions.]

5.1 Introduction

The load end converter of low voltage high current power supply plays an important role to improve the performances of converter in terms of size, weight, losses and cost [72, 83]. In chapter-4, three-phase high frequency resonant DC-DC converter with centre-tapped rectifier based load end converter has been analysed and found suitable for medium power applications. In centre-tapped rectifier based load end converter, the secondary windings of transformer are designed for large DC current which are equal to current rating of rectifier diodes/ output filter inductor [32,83]. The load end converter comprises of current doubler configuration offers several advantages over centre-tapped configuration and hence, it is preferred over the centre-tapped configuration for a number of reasons for single-phase power circuit [28, 32]:

- There is no need of centre-tapped secondary windings which makes transformer structure simple.
- The current through the output inductor and the transformer secondary winding are two times lower than the corresponding currents in the centre-tapped converter. As a result, the current-doubler converter exhibits lower conduction losses than the centre-tapped converter.
- The current-doubler configuration minimizes the number of high-current inter-connections that simplify the secondary layout and its layout-related loss.
- The transformer and the filter inductors in the current-doubler converter can be integrated on a single magnetic core, which simplifies the packaging of the components and reduce the overall size of the magnetic.

The current doubler converter has been combined with single-phase front end topologies such as the forward, half-bridge, push–pull, and the full-bridge converter topology [30, 72, 75]. These single-phase high frequency isolated DC-DC converters face severe stresses when employed for high power applications (over power rating of 5kWs). Therefore, three-phase HF isolated DC-DC converters have been proposed in [54, 57, 59, 84-87]. They

have several advantages over single-phase high frequency isolated converters such as lesser turn ratio of the transformer, reduced size of passive filters etc. In all these isolated DC-DC converters, first input DC voltage is converted into high frequency balanced AC voltages via front end converter and then voltage scaling, isolation are provided through high frequency transformer. Finally, the high frequency AC voltage is converted into DC through load end converter.

In view of above mentioned advantages of the current doubler converter, the multi-phase high frequency isolated DC-DC converter with multi-phase load end topology is introduced in which load end converter is extended version of current doubler converter topology. The performance of proposed converter is investigated under symmetrical and asymmetrical controlled phase shifted PWM control methods with fixed frequency operation.

5.2 System Configuration and Control Scheme

5.2.1 Power Circuit

The schematic diagram of multi-phase high frequency isolated DC-DC converter is shown in Fig.5.1. It consists of three main parts: front end converter, high frequency transformer and load end converter. The front end converter comprises of *N* legs and each leg consists of two power switches. The midpoints of each leg are connected to one end of the primary winding of single-phase high frequency transformers and other ends of the primary winding of transformers are connected together at point '*n*' to form wye-connections. The high frequency transformer consists of *N* units of single phase high frequency transformer in which primary and secondary winding connections for three-phase, four-phase, five and six-phase configurations are illustrated in Fig.5.2 . On the basis of secondary side load sharing, transformer design and thermal heat dissipation, the load end converter of multi-phase full diode bridge is selected in which upper diodes are replaced by inductors $(L_1, L_2, L_3, ...L_N)$ as shown in Fig.5.1.

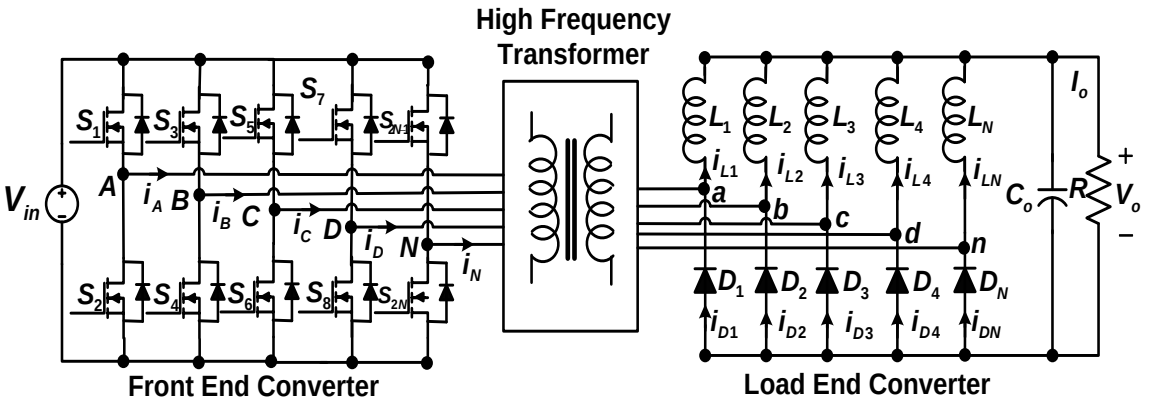
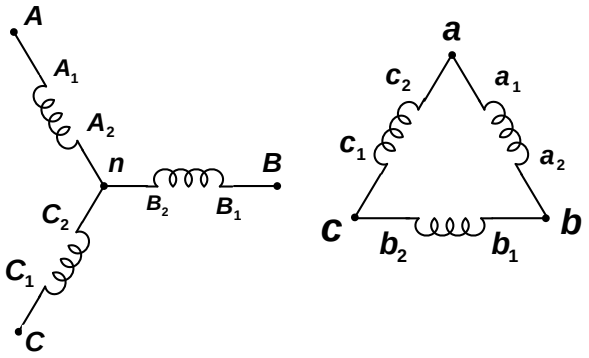
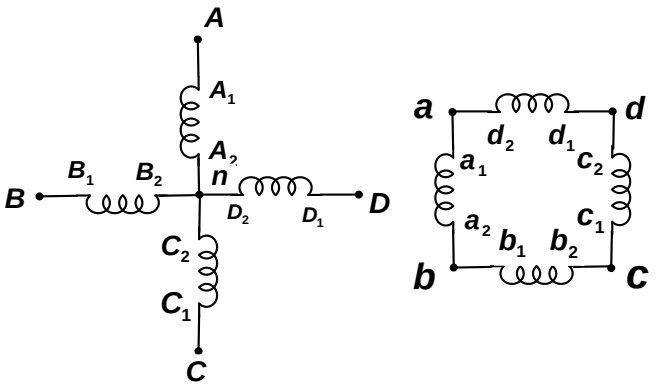


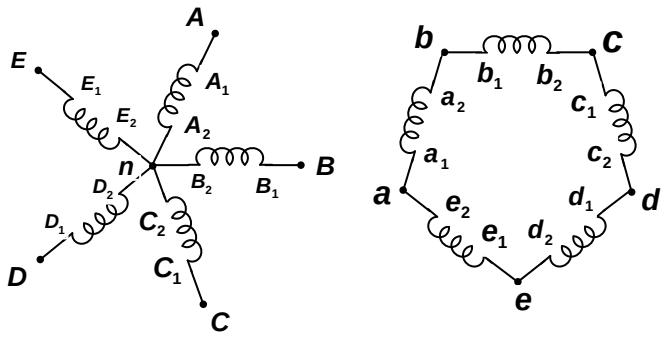
Fig.5.1 Multi-phase high frequency isolated DC-DC converter



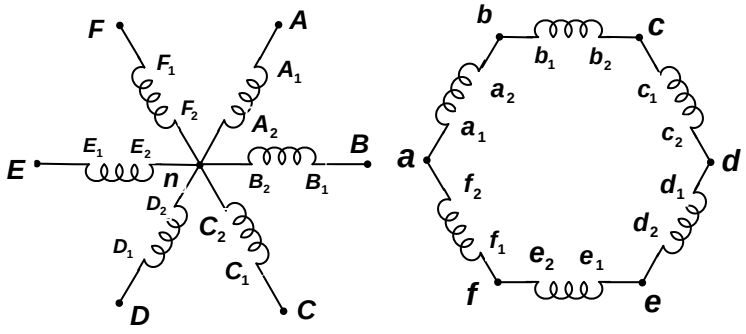
(a)



(b)



(c)



(d)

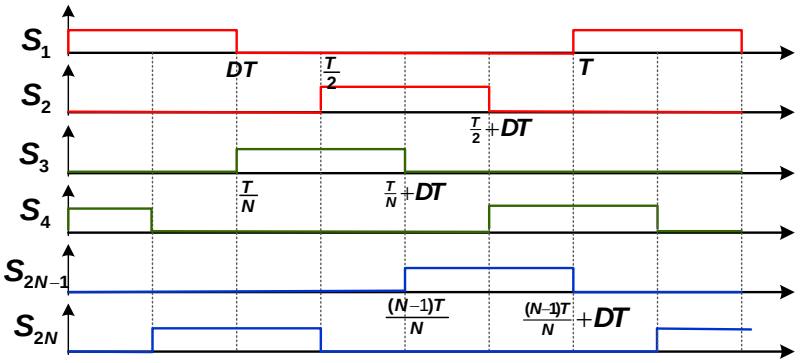
Fig.5.2 Winding connection of high frequency transformer (a) Three-phase (b) Four-phase (c) Five-phase (d) Six-phase

5.2.2 Control Strategy

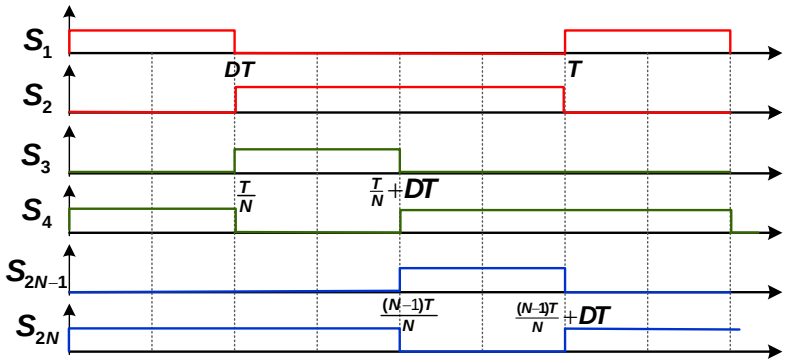
In fixed frequency operation, the width of PWM signals for the power switches of the front end converter is to be varied to regulate the output voltage against variations of input DC voltage and load. Based on the duty cycle of power switches, two PS-PWM control methods namely symmetrical and asymmetrical control methods are proposed.

In the symmetrical control method, the duty ratio of the upper group of power switches $(S_1, S_3, S_5, \ldots S_{2N-1})$ is same as that of the lower group of power switches $(S_2, S_4, S_6, \ldots S_{2N})$ as shown in Fig.5.3 (a). In other words, all the power switches operate for same durations. The phase shift between PWM signals of two switches of the same leg differs by $(T/2)$ and that of different legs differs with (T/N) as shown in Fig.5.3 (a).

In the asymmetrical control method, the duty cycle of the upper group of power switches differs with lower group of switches. The power switches of the same legs operate in a complementary manner as shown in Fig.5.3 (b). The PWM signals for power switches of different legs are advanced or delayed by T/N with respect to each leg to obtain multi-phase balanced output voltages from front end converter.



(a)



(b)

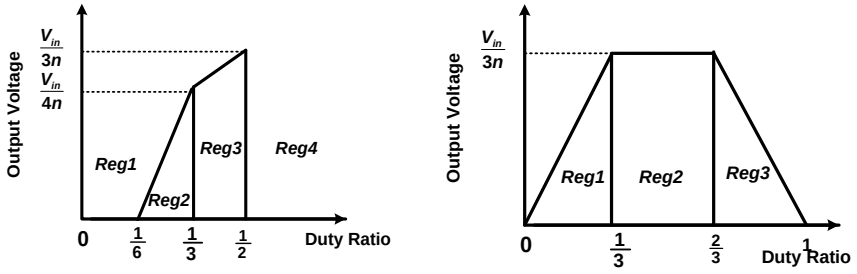
Fig.5.3 Switching signals in phase-shifted PWM control (a) Symmetrical (b) Asymmetrical

5.3 Operation, Modeling and Analysis of the Converter

In this section three-phase high frequency isolated DC-DC converters are discussed in detail where front end converter consists of three legs and its midpoints $(A,B\,\&\,C)$ are connected to three single-phase transformers as shown in Fig.5.2 (a). On the other hand secondary windings of transformers are connected in delta configuration and its terminals $(a,b\,\&\,c)$ are connected to the mid points of three legs of load end converter. The power switches associated with different legs of front end converter operate with a phase shift of $\left(\frac{T}{3}=120^0\right)$ under both aforementioned control methods.

In the symmetrical control method, based on duty cycle variations, the complete operating region is classified in four regions: Reg1 to Reg4 as shown in Fig. 5.4 (a). In Reg1$\left(0\le D\le\frac{1}{6}\right)$, at any instant only one power switch conducts which makes no current to flow through front end converter due to its incomplete current path. When the duty cycle exceeds beyond, $\left(D\ge\frac{1}{2}\right)$ i.e. Reg4, shoot through conditions occurs which leads to direct short circuit of the input DC source. Thus the output voltage of converter operated in regions (Reg1 and Reg4) is zero. Therefore, under this control method converter is allowed to operate mainly in Reg2$\left(\frac{1}{6}\le D\le\frac{1}{3}\right)$ and Reg3$\left(\frac{1}{3}\le D\le\frac{1}{2}\right)$. In both operating regions (Reg2, Reg3), the output voltage increases linearly with different slope as shown in Fig. 5.4 (a).

In the asymmetrical control method, duty cycle allows to vary between 0 and 1. In this case three operating regions: Reg1$\left(0\le D\le\frac{1}{3}\right)$, Reg2 $\left(\frac{1}{3}\le D\le\frac{2}{3}\right)$ and Reg3$\left(\frac{2}{3}\le D\le 1\right)$ are identified. In region Reg1, output voltage increase from 0 to $\left(\frac{V_{in}}{3}\frac{N_1}{N_2}\right)$ linearly with duty ratio. During operation in Reg2, the output voltage remains constant$\left(\frac{V_{in}}{3}\frac{N_1}{N_2}\right)$, irrespective of duty cycle variations and as duty cycle varies between $\frac{2}{3}$ to 1, output voltage decreases from $\left(\frac{V_{in}}{3}\frac{N_1}{N_2}\right)$ to 0. It has been observed that the output voltage can be controlled in Reg1 and Reg3, however design of controller for converter operated in Reg3 is uncommon practice and therefore converter is allowed to operate in Reg1 to regulate output voltage.



(a) (b)

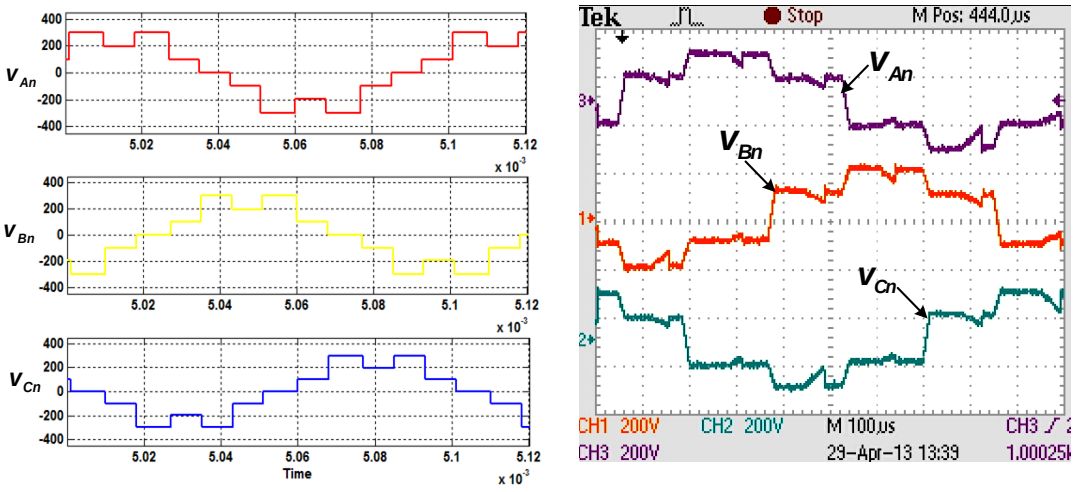
Fig. 5.4 Output voltage versus duty ratio (a) Symmetrical Control (b) Asymmetrical Control

Table 5.1 Conduction of switches of front end converter

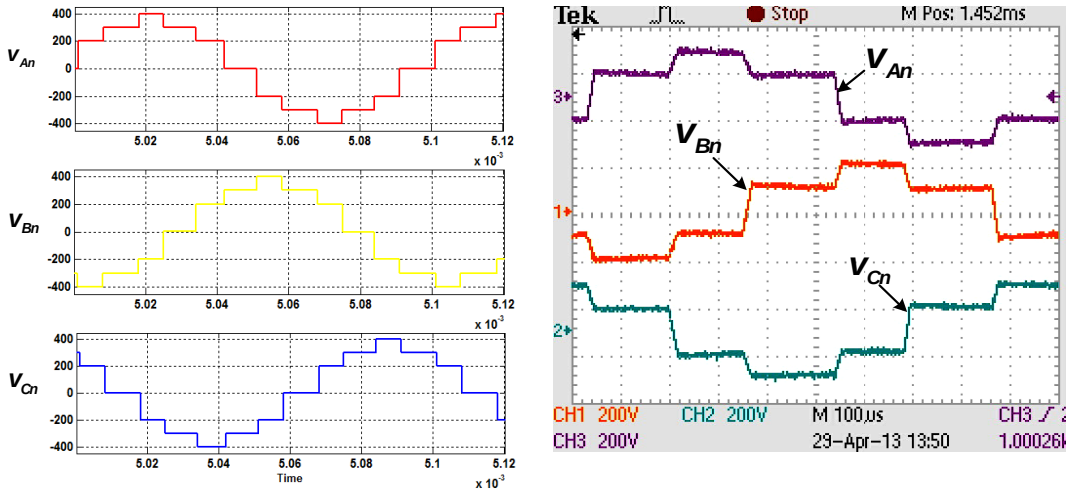
Symmetrical control method			Asymmetrical control method		
Modes	Reg2$\left(\frac{1}{6} \le D \le \frac{1}{3}\right)$	Reg3$\left(\frac{1}{3} \le D \le \frac{1}{2}\right)$	Modes	Reg1$\left(0 \le D \le \frac{1}{3}\right)$	Reg2 $\left(\frac{1}{3} \le D \le \frac{2}{3}\right)$
1	S_4, S_1	S_5, S_4, S_1	1	S_6, S_4, S_1	S_5, S_4, S_1
2	S_1	S_4, S_1	2	S_2, S_4, S_6	S_1, S_4, S_6
3	S_1, S_6	S_4, S_1, S_6	3	S_2, S_3, S_6	S_1, S_3, S_6
4	S_6	S_1, S_6	4	S_2, S_4, S_6	S_2, S_3, S_6
5	S_6, S_3	S_1, S_6, S_3	5	S_2, S_4, S_5	S_2, S_3, S_5
6	S_3	S_6, S_3	6	S_2, S_4, S_6	S_2, S_4, S_5
7	S_3, S_2	S_6, S_3, S_2			
8	S_2	S_3, S_2			
9	S_2, S_5	S_3, S_2, S_5			
10	S_5	S_2, S_5			
11	S_5, S_4	S_2, S_5, S_4			
12	S_4	S_5, S_4			

The conduction of power switches of front end converter under aforementioned control methods mainly depends on region of operation. Sequence of switches operate in different regions are tabulated in Table 5.1.

Fig.5.5 and Fig.5.6 show the experimental and simulation waveforms of phase voltages $\left(v_{An}, v_{Bn} \,\&\, v_{Cn}\right)$ of symmetrical and asymmetrical controlled front end converter in different operating regions. It is observed that simulated phase voltage waveforms are in confirmty with experimental waveform. As operating mode changes, the step variations in voltages are observed as per Table 5.1 in simulation results whereas linear variations in voltages are observed in experimental waveform which are due to gradual charge and discharge of snubber capacitors of power switches.

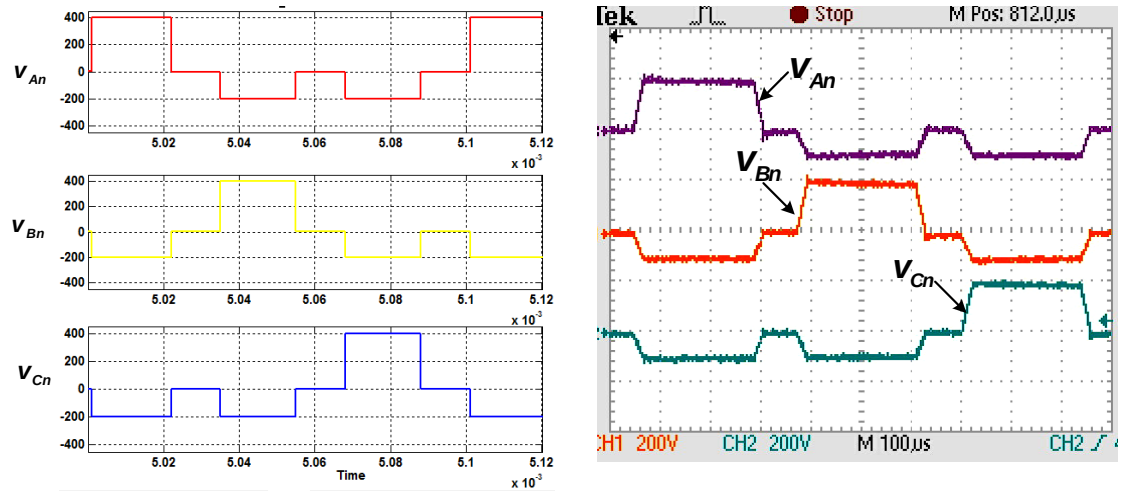


(a)

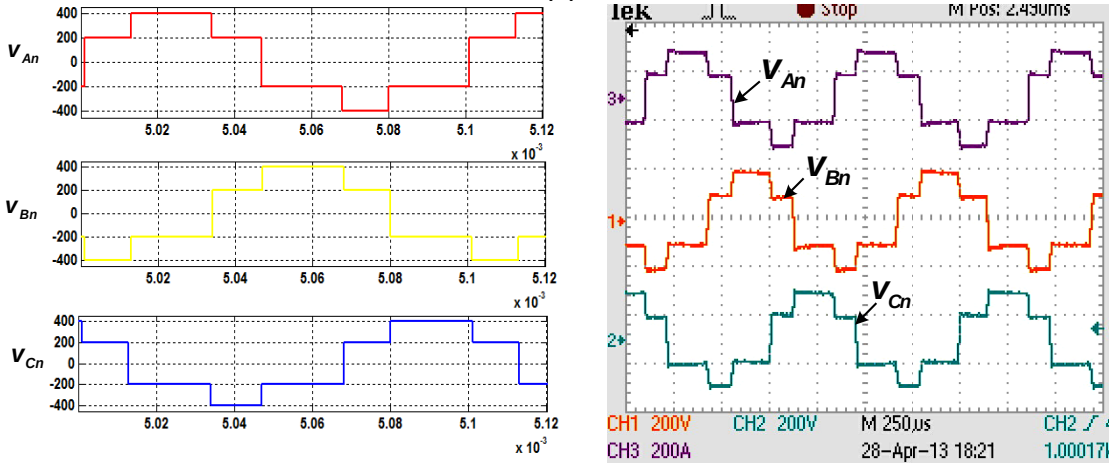


(b)

Fig.5.5 Simulation and experimental waveforms of phase voltages of symmetrically controlled front end converter operated in (a) Reg2 (b) Reg3



(a)



(b)

Fig.5.6 Simulation and experimental waveforms of phase voltages of asymmetrically controlled front end converter operated in (a) Reg1 (b) Reg2.

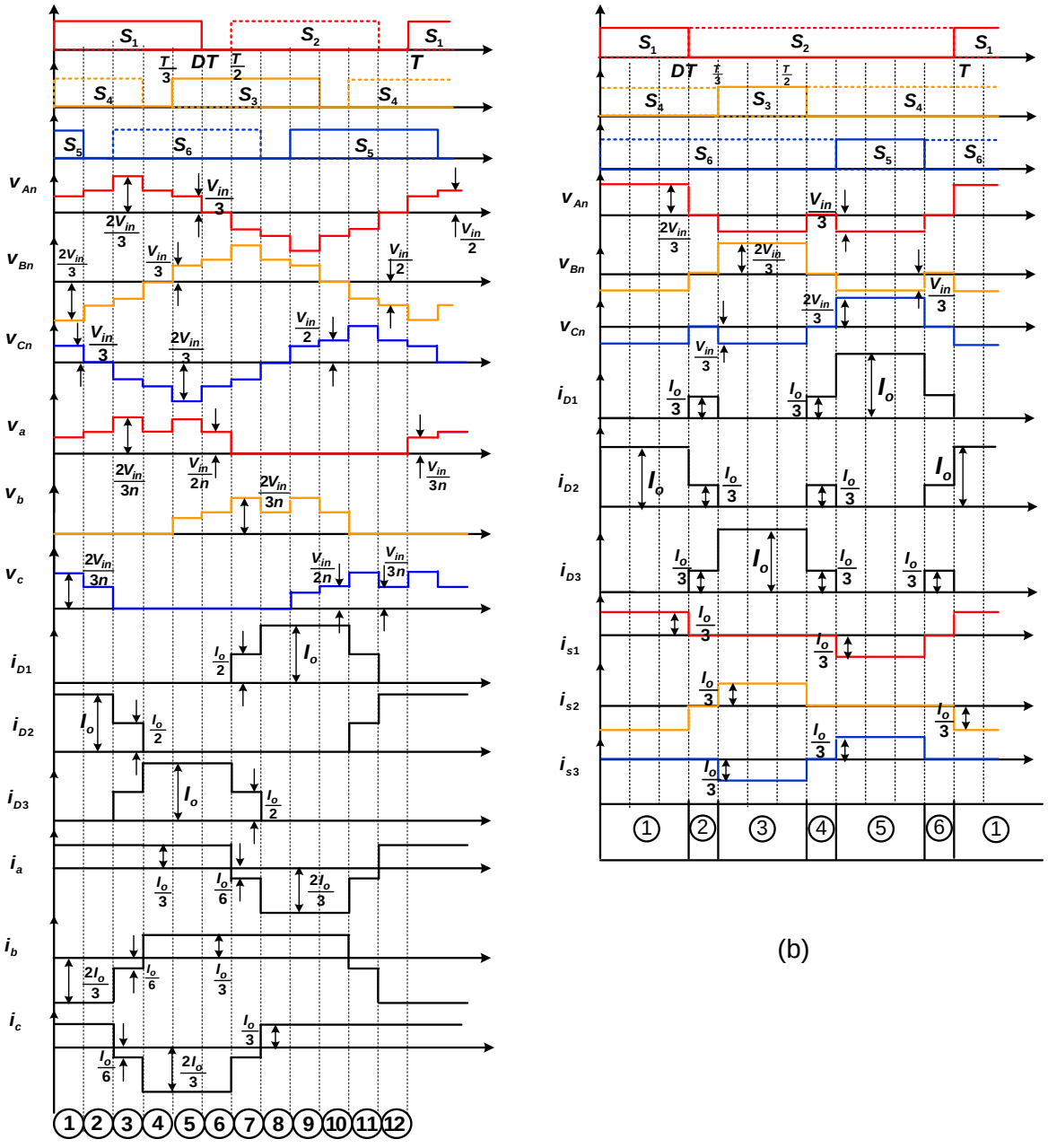
In order to simplify the steady state analysis of proposed converter, the following assumptions are made:

- Power switching devices and passive components are lossless.
- The input and output voltages are constant and ripple-free.
- The output inductors are large enough to ensure continuous current operation and the currents are constant and ripple-free.
- Three-phase circuits are balanced.
- Effects on snubber circuit are neglected.

The switches of each leg of front end converter are symmetrical / asymmetrically controlled and 120^0 phase shifted between each leg for interleaved operation as shown in Fig. 5.7. In worst case deisgn, the proposed converter will operate in region Reg3 under symmetrical control method and in Reg2 under asymmetrical control method to deliver full load current with minimum input voltage. The operation of converter in these regions are explained in following subsection.

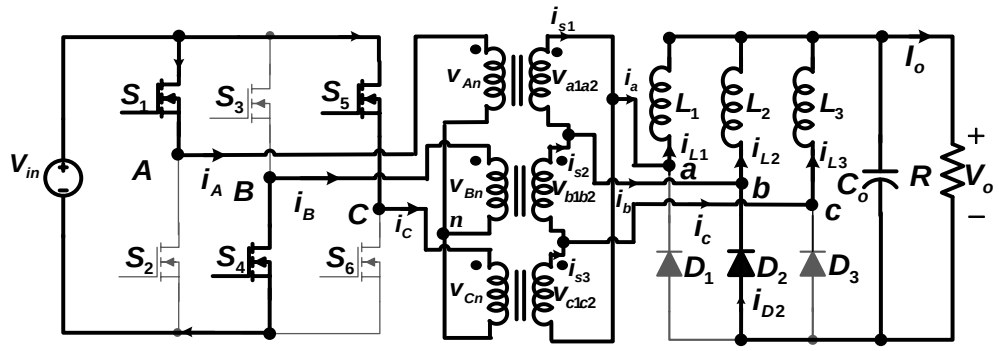
5.3.1 Operation of Converter under Symmetrical Control Method

The steady state waveforms of various circuit parameters of converter operated under symmetrical control method in region Reg3 is shown in Fig. 5.7(a). Based on the state of power switches twelve operating modes are identified as tabulated in Table 5.1. It is observed that power switches of front end converter conducted during mode-1 to mode-6 are complementary with mode-7 to mode-12 respectively. Therefore, operation of the converter during mode-1 to mode-6 is discussed and mode-wise equivalent circuits are shown in Fig. 5.8. The operation of converter is explained below by referring Fig. 5.7 and Fig. 5.8 simultaneously.

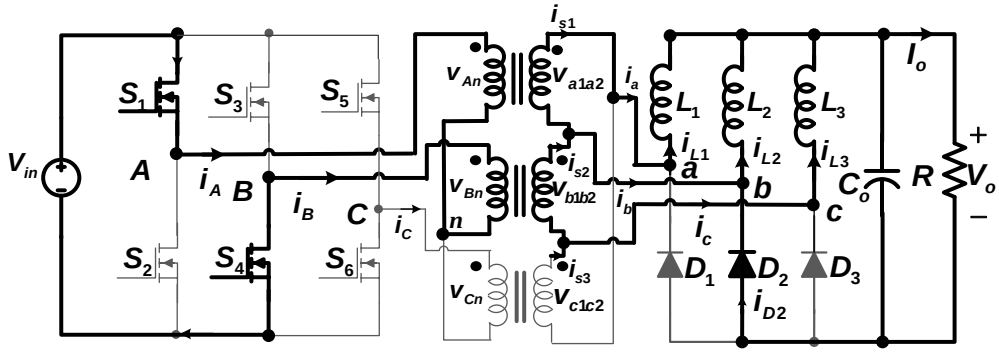


(a) (b)

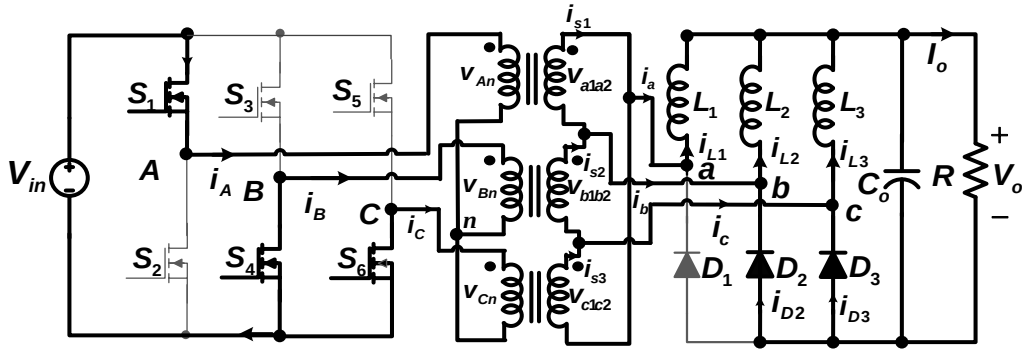
Fig. 5.7 Steady-state waveforms of voltage and current (a) Symmetrical control (b) Asymmetrical control


i_{s1}
v_{An}
v_{a1a2}
i_a
L_1
L_2
L_3
I_o
S_1
S_3
S_5
V_{in}
A
i_A B
i_B
C
i_C
i_{s2}
v_{Bn}
v_{b1b2}
i_b
i_{L1}
i_{L2}
i_{L3}
a
b
c
C_o
R
V_o
n
i_c
S_2
S_4
S_6
v_{Cn}
i_{s3}
v_{c1c2}
D_1
D_2
D_3
i_{D2}

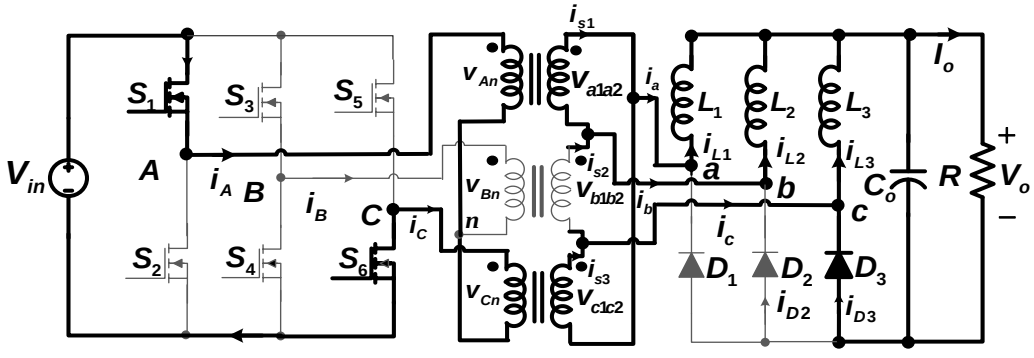
(a)


i_{s1}
v_{An}
v_{a1a2}
i_a
L_1
L_2
L_3
I_o
S_1
S_3
S_5
V_{in}
A
i_A B
i_B
C
i_C
i_{s2}
v_{Bn}
v_{b1b2}
i_b
i_{L1}
i_{L2}
i_{L3}
a
b
c
C_o
R
V_o
n
i_c
S_2
S_4
S_6
v_{Cn}
i_{s3}
v_{c1c2}
D_1
D_2
D_3
i_{D2}

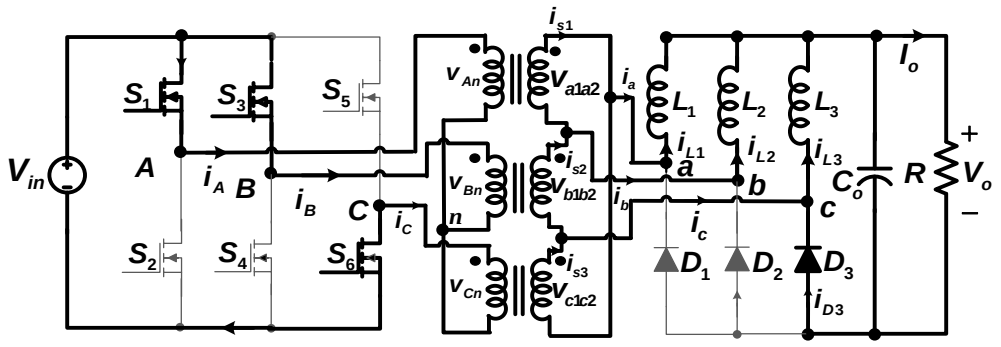
(b)


i_{s1}
v_{An}
v_{a1a2}
i_a
L_1
L_2
L_3
I_o
S_1
S_3
S_5
V_{in}
A
i_A B
i_B
C
i_C
i_{s2}
v_{Bn}
v_{b1b2}
i_b
i_{L1}
i_{L2}
i_{L3}
a
b
c
C_o
R
V_o
n
i_c
S_2
S_4
S_6
v_{Cn}
i_{s3}
v_{c1c2}
D_1
D_2
D_3
i_{D2}
i_{D3}

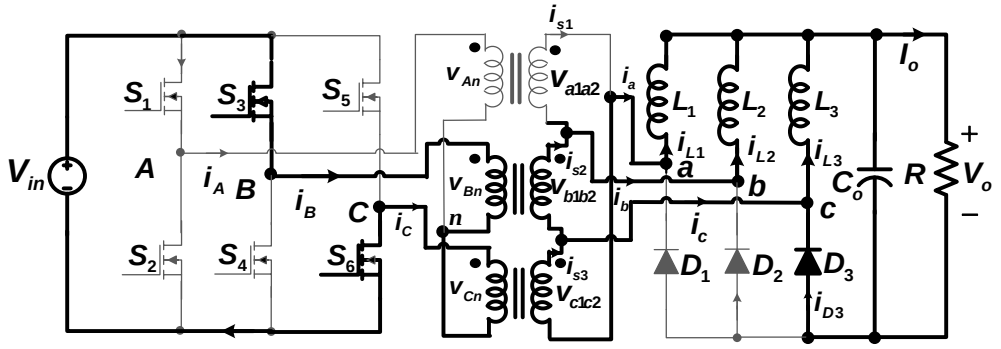
(c)


i_{s1}
v_{An}
v_{a1a2}
i_a
L_1
L_2
L_3
I_o
S_1
S_3
S_5
V_{in}
A
i_A B
i_B
C
i_C
i_{s2}
v_{Bn}
v_{b1b2}
i_b
i_{L1}
i_{L2}
i_{L3}
a
b
c
C_o
R
V_o
n
i_c
S_2
S_4
S_6
v_{Cn}
i_{s3}
v_{c1c2}
D_1
D_2
D_3
i_{D2}
i_{D3}

(d)



(e)



(f)

Fig. 5.8 Equivalent circuits of the symmetrically controlled converter in (a) mode-1 (b) mode-2 (c) mode-3 (d) mode-4 (e) mode-5 (f) mode-6

(a)Mode-1

In this mode, switches S_1, S_4 and S_5 are ON and remaining switches are OFF as shown in Fig. 5.8(a). The voltages : $v_{An} = \frac{V_{in}}{3}, v_{Bn} = -\frac{2V_{in}}{3}, v_{Cn} = \frac{V_{in}}{3}, v_{a1a2} = \frac{V_{in}}{3n}, v_{b1b2} = -\frac{2V_{in}}{3n}, v_{c1c2} = \frac{V_{in}}{3n}$ appear across primary and secondary windings of transformers as shown in Fig. 5.7(a). where n is turns ratio. The potential of mid-points (a,b,c) of load end converter : $v_a = \frac{V_{in}}{3n}$, $v_b = 0, v_c = \frac{V_{in}}{3n}$ are determined with respect to negative terminal of load which forward biases the rectifier diode D_2. The currents in different parts of load end converter are $i_a = \frac{I_o}{3}$, $i_b = -\frac{2I_o}{3}$, $i_c = \frac{I_o}{3}, i_{D1} = 0, i_{D2} = I_o, i_{D3} = 0, i_{s1} = \frac{4I_o}{9}, i_{s2} = -\frac{2I_o}{9}, i_{s3} = \frac{I_o}{9}$ as shown in Fig. 5.8(a). This mode terminates with turning OFF of power switch S_5.

(b)Mode-2

During this mode switches (S_1, S_4) are ON and remaining switches are OFF as shown in Fig. 5.8(b). The voltages and current equations during this mode are given below:

$$v_{An}=\frac{V_{in}}{2},v_{Bn}=-\frac{V_{in}}{2},v_{Cn}=0,v_{a1a2}=\frac{V_{in}}{2n},v_{b1b2}=-\frac{V_{in}}{2n},v_{c1c2}=0,\ v_a=\frac{V_{in}}{2n},v_b=0,v_c=\frac{V_{in}}{2n},$$

$$i_a=\frac{I_o}{3},i_b=-\frac{2I_o}{3},i_c=\frac{I_o}{3},i_{D1}=0,\ i_{D2}=I_o,i_{D3}=0,i_{s1}=\frac{I_o}{3},i_{s2}=-\frac{I_o}{3},i_{s3}=0.$$

The potential of mid-point b is lower than points $a\&c$. Therefore, rectifier diode, D_2 remain in conduction. This mode terminates at $t=\frac{T}{6}$ when S_6 turned ON.

(c) Mode-3

In this mode power switches (S_1,S_4,S_6) are ON and remaining switches are OFF as shown in Fig. 5.8(c). The voltage and current equations during this mode are given below:

$$v_{An}=\frac{2V_{in}}{3},v_{Bn}=-\frac{V_{in}}{3},v_{Cn}=-\frac{V_{in}}{3},v_{a1a2}=\frac{2V_{in}}{3n},v_{b1b2}=-\frac{V_{in}}{3n},v_{c1c2}=-\frac{V_{in}}{3n},v_a=\frac{2V_{in}}{3n},v_b=0,$$

$$v_c=0,i_a=\frac{I_o}{3},i_b=-\frac{I_o}{6},i_c=-\frac{I_o}{6},i_{D1}=0,i_{D2}=\frac{I_o}{2},i_{D3}=\frac{I_o}{2},i_{s1}=\frac{I_o}{18},i_{s2}=-\frac{I_o}{9}\ i_{s3}=-\frac{5I_o}{18}$$

As points $b\&c$ of load end converter are at least potential, therefore during this mode rectifier diodes (D_2,D_3) are forward biased and carry half of the load current as shown in Fig. 5.7(a). This mode ends with switch S_4 turned OFF.

(d) Mode-4

In this mode switches (S_1,S_6) are ON and remaining switches are OFF as shown in Fig. 5.8(d). The voltage and current equations during this mode are given below:

$$v_{An}=\frac{V_{in}}{2},v_{Bn}=0,v_{Cn}=-\frac{V_{in}}{2},v_{a1a2}=\frac{V_{in}}{2n},v_{b1b2}=0,v_{c1c2}=-\frac{V_{in}}{2n},v_a=\frac{V_{in}}{2n},v_b=0,v_c=0,$$

$$i_a=\frac{I_o}{3},i_b=\frac{I_o}{3},i_c=-\frac{2I_o}{3},i_{D1}=0,i_{D2}=0,i_{D3}=I_o$$

During this mode, the rectifier diode D3 carries the load currents and other diodes (D_1,D_2) are reverse biased.

(e) Mode-5

During this mode switches (S_1,S_3,S_6) are ON and remaining switches are OFF and its associated voltages and current are given below. The equivalent circuit during this mode is given in Fig. 5.8(e).

$$v_{An}=\frac{V_{in}}{3},v_{Bn}=\frac{V_{in}}{3},v_{Cn}=-\frac{2V_{in}}{3},v_{a1a2}=\frac{V_{in}}{3n},v_{b1b2}=\frac{V_{in}}{3n},v_{c1c2}=-\frac{2V_{in}}{3n},v_a=\frac{2V_{in}}{3n},v_b=0$$

$$v_b=\frac{V_{in}}{3n},v_c=0,\ i_a=\frac{I_o}{3},i_b=\frac{I_o}{3},i_c=-\frac{2I_o}{3},i_{D1}=0,i_{D2}=0,i_{D3}=I_o$$

This mode terminates with turning OFF of switch S_1.

(f) Mode-6

During this mode switches (S_3, S_6) are ON and remaining switches are OFF as shown in Fig. 5.8(f). The voltage and current equations during this mode are given below:

$$v_{An} = 0, v_{Bn} = \frac{V_{in}}{2}, v_{Cn} = -\frac{V_{in}}{2}, v_{a1a2} = 0, v_{b1b2} = \frac{V_{in}}{2n}, v_{c1c2} = -\frac{V_{in}}{2n}, v_a = \frac{V_{in}}{2n}, v_b = \frac{V_{in}}{2n}, v_c = 0$$

$$i_a = \frac{I_o}{3}, i_b = \frac{I_o}{3}, i_c = -\frac{2I_o}{3}, i_{D1} = 0, i_{D2} = 0, i_{D3} = I_o$$

5.3.2 Operation of Converter under Asymmetrical Control Method

To investigate the performance, the mathematical modelling of the proposed converter under asymmetrical control method is carried out. The proposed converter operates in six operating modes under this control method in both operating regions (Reg1,Reg2) as tabulated in Table 5.1. The operation of converter in region (Reg1) is explained by referring Fig. 5.7(b) and Fig.5.9 simultaneously. The equivalent circuits during different modes of operation indicating current paths with bold line are illustrated in Fig.5.9.

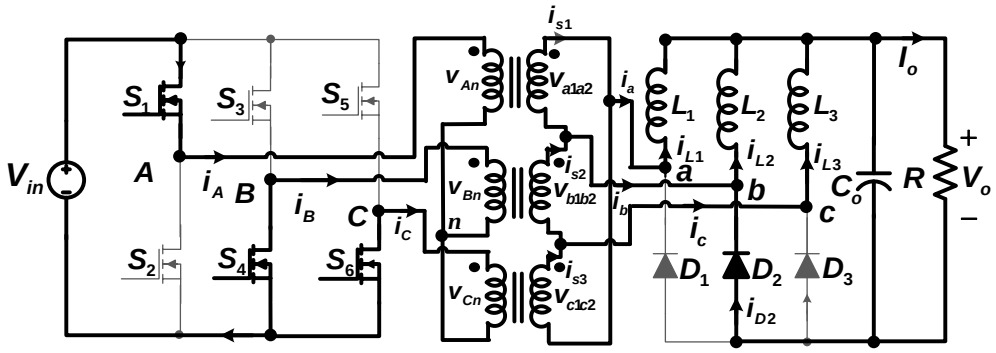
(a) Mode-1$(0 < t < DT)$: In this mode, power switches (S_1, S_4, S_6) are ON and remaining switches are OFF as shown in Fig.5.9(a). The voltages: $v_{An} = \frac{2V_{in}}{3}, v_{Bn} = -\frac{V_{in}}{3}, v_{Cn} = -\frac{V_{in}}{3}$, $v_{a1a2} = \frac{2V_{in}}{3n}, v_{b1b2} = -\frac{V_{in}}{3n}, v_{c1c2} = -\frac{V_{in}}{3n}$ appear across primary and secondary windings of transformers which forward biases rectifier diode D_2 as shown in Fig. 5.7(b). The current in different parts of load end converter are $i_a = \frac{I_o}{3}, i_b = -\frac{2I_o}{3}, i_c = \frac{I_o}{3}, i_{D1} = 0$, $i_{D2} = I_o, i_{D3} = 0$ as shown in Fig.5.9(a). The mode-1 ends with turning OFF of power switch S_1.

(b) Mode-2$(DT < t < \frac{T}{3})$: At $t = DT$ power switch (S_2) turns ON and it starts conducting along with previous conducting switches (S_4, S_6). The equivalent circuit during this mode is shown in Fig.5.9 (b). All output inductors freewheel through rectifier diodes. The voltage and current in different parts of circuits are given below:

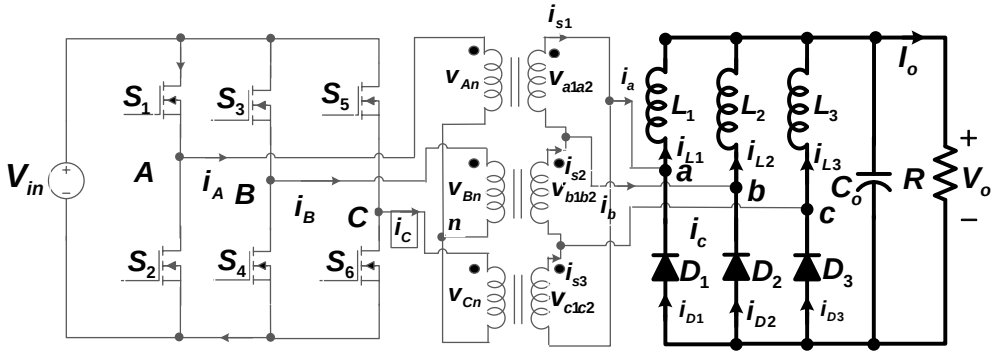
$$v_{An} = 0, v_{Bn} = 0, v_{Cn} = 0, v_{a1a2} = 0, v_{b1b2} = 0, v_{c1c2} = 0, i_{D1} = i_{D2} = i_{D3} = \frac{I_o}{3},$$

The operation of converter in mode-4$(\frac{T}{3} + DT < t < \frac{2T}{3})$ and mode-6$(\frac{2T}{3} + DT < t < T)$ are similar to mode-2.

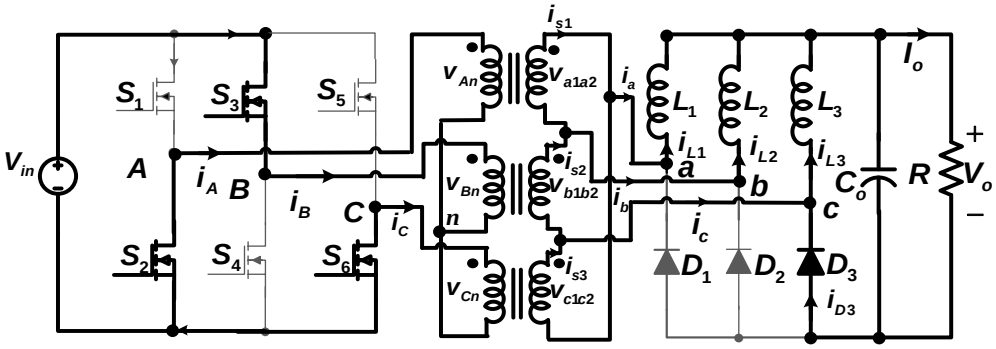
(c) Mode-3$(\frac{T}{3} < t < \frac{T}{3} + DT)$*:* During this mode power switches (S_2, S_3, S_6) are in operation as shown in Fig.5.9(c). The voltages $v_{An} = -\frac{V_{in}}{3}, v_{Bn} = \frac{2V_{in}}{3}, v_{Cn} = -\frac{V_{in}}{3}$ appear at primary winding and induced voltage in secondary winding of each transformer. The rectifier diode D_3 is forward biased and carries whole load current.



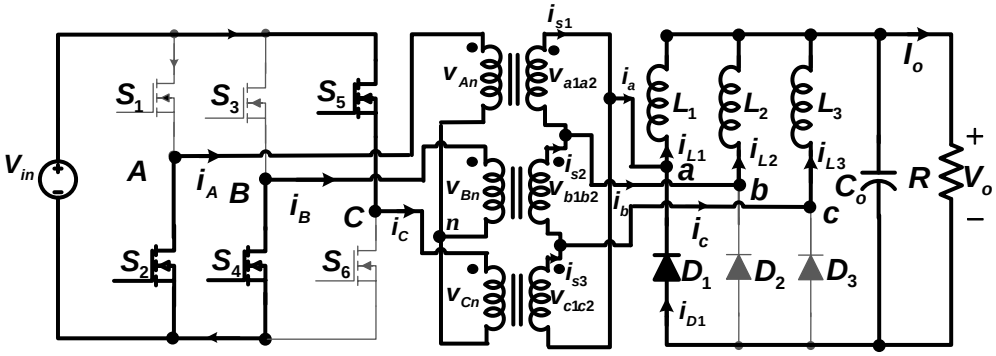
(a)



(b)



(c)



(d)

Fig.5.9 Equivalent circuits of asymmetrically controlled converter (a) Mode-1 (b) Mode-2, 4, 6 (c) Mode-3 (d) Mode-5.

(e) Mode-5 $\left(\frac{2T}{3} < t < \frac{2T}{3} + DT\right)$*:* During this mode, switches (S_2, S_4, S_5) are in conduction as shown in Fig.5.9(d). The voltage and current equations during this mode are given below:

$$v_{An} = -\frac{V_{in}}{3}, v_{Bn} = -\frac{V_{in}}{3}\ v_{Cn} = \frac{2V_{in}}{3}, V_{a1a2} = -\frac{V_{in}}{3n}, v_{b1b2} = -\frac{V_{in}}{3n}, v_{c1c2} = \frac{2V_{in}}{3n}, i_a = -\frac{2I_o}{3}, i_b = \frac{I_o}{3},$$

$$i_c = \frac{I_o}{3}, i_{D1} = I_o, i_{D2} = i_{D3} = 0$$

5.4 Design of Output Filter Inductor

The proposed converter is operated with interleaved PS-PWM control technique to reduce output ripples in voltage and current. In this scheme effective output ripple frequency is increased without increasing switching frequency of power switches. The following voltage equations can be written from the load end converter shown in Fig.5.1.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} r_{L1} + L_1 p & M_{12} p & M_{13} p \\ M_{21} p & r_{L2} + L_2 p & M_{23} p \\ M_{31} p & M_{32} p & r_{L3} + L_3 p \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \end{bmatrix} + \begin{bmatrix} v_o \\ v_o \\ v_o \end{bmatrix} \tag{5.1}$$

Where v_a, v_b and v_c are potential of mid points (a, b& c) of load end converter with reference to negative dc output voltage respectively, $r_{L1} = r_{L2} = r_{L3} = r_L$ be the effective resistance of output filter inductors $(L_1 = L_2 = L_3 = L)$ and mutual inductance between filter inductors be $M_{12} = M_{21} = M_{23} = M_{32} = M_{13} = M_{31} = M$ and $p = \frac{d}{dt}$. If the voltages and currents are separated into the average (capital case) and ripple components (small case with cap) then equation (5.1) can be written as follow:

$$\begin{bmatrix} V_a + \hat{v}_a \\ V_b + \hat{v}_b \\ V_c + \hat{v}_c \end{bmatrix} = \begin{bmatrix} r_{L1} + L_1 p & M_{12} p & M_{13} p \\ M_{21} p & r_{L2} + L_2 p & M_{23} p \\ M_{31} p & M_{32} p & r_{L3} + L_3 p \end{bmatrix} \begin{bmatrix} I_{L1} + \hat{i}_{L1} \\ I_{L2} + \hat{i}_{L2} \\ I_{L3} + \hat{i}_{L3} \end{bmatrix} + \begin{bmatrix} V_o + \hat{v}_o \\ V_o + \hat{v}_o \\ V_o + \hat{v}_o \end{bmatrix} \tag{5.2}$$

Equating average and ripple components on the left- and right-hand sides of equation(5.2), the following equations can be obtained

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} r_{L1} I_{L1} + V_o \\ r_{L3} I_{L2} + V_o \\ r_{L3} I_{L3} + V_o \end{bmatrix} \tag{5.3}$$

$$\begin{bmatrix} \hat{v}_a \\ \hat{v}_b \\ \hat{v}_c \end{bmatrix} = \begin{bmatrix} r_{L1} + L_1 p & M_{12} p & M_{13} p \\ M_{21} p & r_{L2} + L_2 p & M_{23} p \\ M_{31} p & M_{32} p & r_{L3} + L_3 p \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{i}_{L3} \end{bmatrix} + \begin{bmatrix} \hat{v}_o \\ \hat{v}_o \\ \hat{v}_o \end{bmatrix} \tag{5.4}$$

The ripple voltage across resistance is usually very small and hence can be neglected. The LC filter is also designed in such way so that all the units are identical and the output voltage ripple is small, with these assumptions, equation(5.4) can be simplified as

$$\begin{bmatrix} \hat{v}_a \\ \hat{v}_b \\ \hat{v}_c \end{bmatrix} = \begin{bmatrix} Lp & Mp & Mp \\ Mp & Lp & Mp \\ Mp & Mp & Lp \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{i}_{L3} \end{bmatrix} \tag{5.5}$$

Using equation(5.5), the inductor currents can be evaluated using following equation.

$$\begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{i}_{L3} \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} L^2 - M^2 & M(M-L) & M(M-L) \\ M(M-L) & L^2 - M^2 & M(M-L) \\ M(M-L) & M(M-L) & L^2 - M^2 \end{bmatrix} \begin{bmatrix} \int (v_a - V_a)dt \\ \int (v_b - V_b)dt \\ \int (v_c - V_c)dt \end{bmatrix} \tag{5.6}$$

Where, $\Delta = L^3 - 3M^2L + 2M^3$

Total ripple components of inductor current is

$$\hat{i}_L = \hat{i}_{L1} + \hat{i}_{L2} + \hat{i}_{L3} \tag{5.7}$$

From equation (5.5) and equation(5.6), we obtain

$$\hat{i}_L = \frac{(L-M)^2}{\Delta} \int \hat{v}_L dt \tag{5.8}$$

Where $\hat{v}_L = v_a + v_b + v_c - V_a - V_b - V_c$

Referring Fig. 5.7(a), the average value of v_b can be derived as

$$V_b = \frac{1}{T} \left[\begin{array}{l} \frac{V_{dc}}{3n}\left(DT - \frac{T}{3}\right) + \frac{V_{dc}}{2n}\left\{\left(\frac{T}{2} - DT\right) + \left(\frac{2T}{3} - \frac{T}{6} - DT\right) + \left(\frac{5T}{6} - \frac{T}{3} - DT\right)\right\} \\ + \frac{2V_{dc}}{3n}\left\{\left(\frac{T}{6} + DT - \frac{T}{2}\right) + \left(\frac{T}{3} + DT - \frac{2T}{3}\right)\right\} \end{array} \right]$$

$$V_b = \frac{V_{dc}}{n}\left(\frac{D}{6} - \frac{7}{36}\right) \tag{5.9}$$

Where *D* be the duty cycle which restricted in the operating region (*Reg3)*. Because, three legs of the inverter bridge operate symmetrically with same duty cycle, & hence $V_a = V_b = V_c$.

The equation for $\hat{v}_L$ can be express as follows with the help of Fig. 5.7(a):

$$\hat{v}_L = \frac{V_{dc}}{3n} + 0 + \frac{2V_{dc}}{3n} - 3\frac{V_{dc}}{n}\left(\frac{D}{6} - \frac{7}{36}\right) = \frac{V_{dc}}{n}\left(\frac{19}{12} - \frac{D}{2}\right) \quad \text{for } 0 \le t \le DT - \frac{T}{3}$$

Thus, $\hat{v}_L$ can be summarized as follows

$$\hat{v}_L = \begin{cases} \frac{V_{dc}}{n}\left(\frac{19}{12}-\frac{D}{2}\right); 0 \le t \le \frac{T}{6}, \frac{V_{dc}}{n}\left(\frac{5}{4}-\frac{D}{2}\right); \frac{T}{6} \le t \le DT - \frac{T}{6} \\ \frac{V_{dc}}{n}, \left(\frac{13}{12}-\frac{D}{2}\right); DT - \frac{T}{6} \le t \le \frac{T}{3} \end{cases} \quad (5.10)$$

Using equation (5.10) and equation(5.8), the expression of current ripple can be obtained.

If the output capacitor is quite large then almost all the ripple component of total inductor current is flowing through the capacitor. With this assumption, capacitor current ripple can be approximated as inductor ripple current. Thus the analysis of ripple current is useful to determine the ripple component of capacitor voltage. Finally, inductor current ripple and the output voltage capacitor ripple can be reduced if coupled inductor with positive mutual inductance is used. Finally, output filter inductors (L_1, L_2, L_3) are designed so that the operation remains in continuous mode until the load current falls in its specified minimum value. The output capacitor that holds the output voltage constant/ specified voltage ripple is designed. As the number of interleaved phase's increases, output capacitor become optional.

5.5 Simulation Studies

To investigate the performances of three-phase isolated DC-DC converter under symmetrical and asymmetrical control methods, a 5kW, 5V/1000A model is developed using Simulink and SimPowerSystem™ of MATLAB Tool Box. Parameters selected for simulation studies for 5kW, 5V/1000A power converter are as follows-

Source voltage ,V_{in}= 600VDC, 10 -20% variations

Switching frequency, f= 10kHz

Single-phase HF Transformer, 2kVA, 400V/40V

L_{lkp}=140nH,L_{lks}= 1nH,L_m = 250 μ H, R_m = 500kΩ

Output filter inductor, L_1=L_2=L_3 = 25 μ H

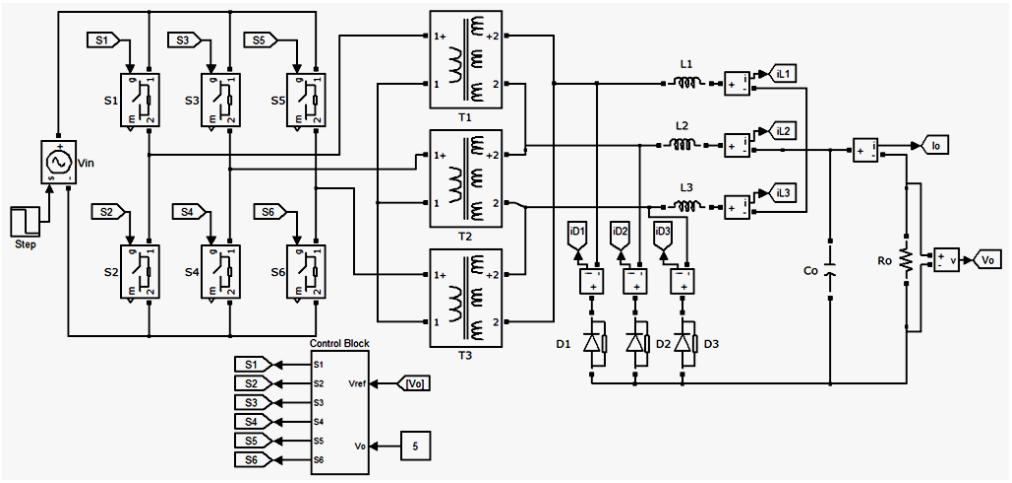
Output filter capacitor, C_o=1000 μ F

Output voltage ripple, ΔV_o = 0.5%

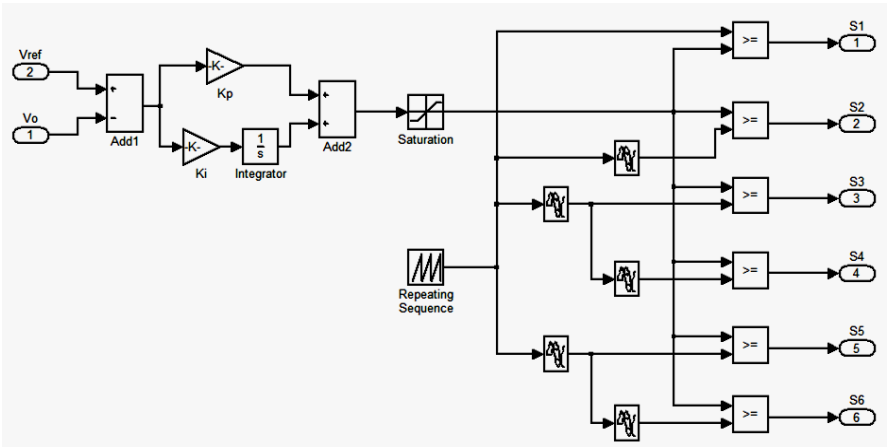
Inductor current ripple, ΔI_L = 7.5%

The system model consists of three main parts: input DC source, power circuit and control circuit as shown in Fig.5.10. The input DC source is modelled with controlled voltage source of SIM power system toolbox library which converts the simulink input signal into an equivalent input voltage source. The generated voltage is driven by the input signal of the block. The power circuit includes front end converter, transformer and load end converter. The front end converter is made of six MOSFETs with anti-parallel power diode and RC snubber circuit is connected in parallel with each MOSFET as shown in Fig.5.10 (a). Three units of two-winding transformer with their primary windings connected in Wye and

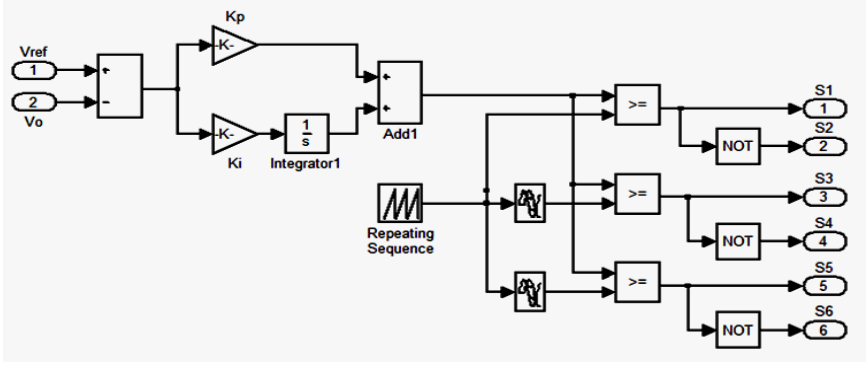
secondary windings in Delta as shown in Fig.5.10(a). The load end converter is similar to three-phase full bridge diode rectifier with upper group of diodes are replaced by output inductor as shown in Fig.5.10(a).



(a)



(b)



(c)

Fig.5.10 Simulink model of three-phase isolated DC-DC converter
(a) power circuit (b) subsystem of symmetrical control system block
(c) subsystem of asymmetrical control block

The control system block generates six switching signals for the power switches of three-leg front end converter. The output voltage is sensed and compared with a reference signal to obtain an error signal which is further processed through PI controller and saturation block to generate the control voltage. The control voltage is limited to less than 0.5 to avoid direct short circuit of input DC voltage. Based on symmetrical / asymmetrical control methods, control logic is built as shown in Fig.5.10(b) and Fig.5.10(c).

Fig.5.10(b) shows subsystem on the symmetrical control block in which control voltage obtained from a PI controller is compared with two saw-tooth waveforms which are phase shifted by 180^0 to generate PWM pulses for two MOSFETs (S_1 and S_2) of the same leg. In order to generate PWM signals for S_3 and S_4, the same control voltage is compared with two saw-tooth waveforms which are phase shifted by 120^0 and 300^0 with respect to first saw-tooth waveform. Similarly, switching PWM signals for MOSFETs (S_5 and S_6) are derived as shown in Fig.5.10 (b).

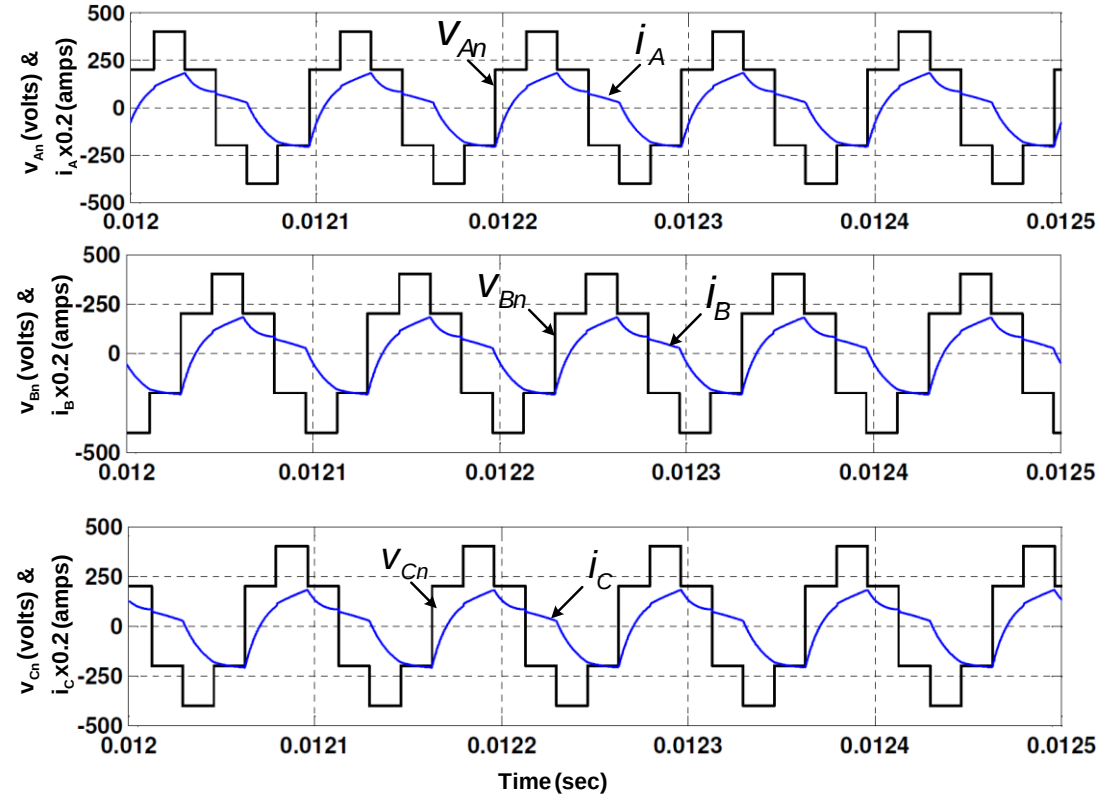
Fig.5.10(c) shows the subsystem of the asymmetrical control block, in which switching PWM signals for S_1, S_3 and S_5 are generated by comparing control voltage obtained from PI controller with three saw-tooth waves which are phase-shifted with 120^0 between each other. The switching PWM singals for S_2, S_4 and S_6 are generated with the help of NOT gate as shown in Fig.5.10(c).

5.5.1 Simulation Results and Discussions

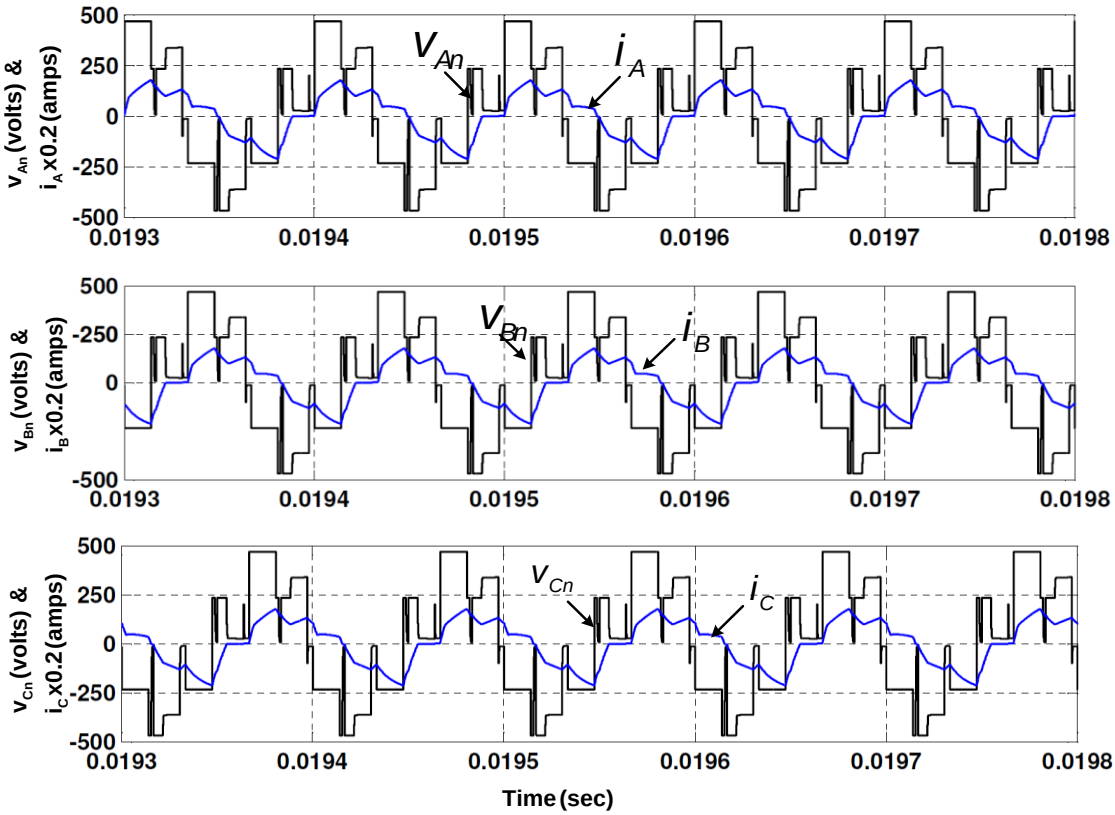
The performance of 5kW, 5V/1000A simulink model of three-phase high frequency isolated DC-DC converter is investigated under symmetrical and asymmetrical control methods. The simulink model of converter is developed as per aforementioned specifications and simulation results obtained with both control methods are discussed as follows:

(a) Performance with Symmetrical Control Method

Fig. 5.11(a) shows the steady state phase voltages (v_{An},v_{Bn},v_{Cn}) and primary side line currents (i_A,i_B,i_C) waveforms of front end converter, when converter operates in *Reg3* under symmetrical control on full load with source voltage, V_{in} = 600V DC. As the DC source voltage, V_{in} increases to 700V, the duty cycle of power switches reduces to provide same load and hence converter operation shifted from *Reg3* to *Reg2*. The phase voltages and primary side line current waveforms in *Reg2* are shown in Fig. 5.11(b). Fig. 5.12 shows the primary current (i_A), secondary winding current (i_{s1}) and secondary side line current (i_a) associated with transformer (T_1). It is observed from Fig. 5.12 that windings current (i_{s1}) of transformer is reduced as compare to line current (i_a) unlike three-phase high frequency isolated LCC resonant DC-DC converter and hence reduces current rating of secondary winding conductors.



(a)



(b)

Fig. 5.11 Phase voltages (v_{an},v_{Bn} & v_{Cn}) and primary line currents (i_A,i_B &i_C) waveforms with input voltage (a) V_{in}= 600V at full load (b) V_{in}= 700V at full load

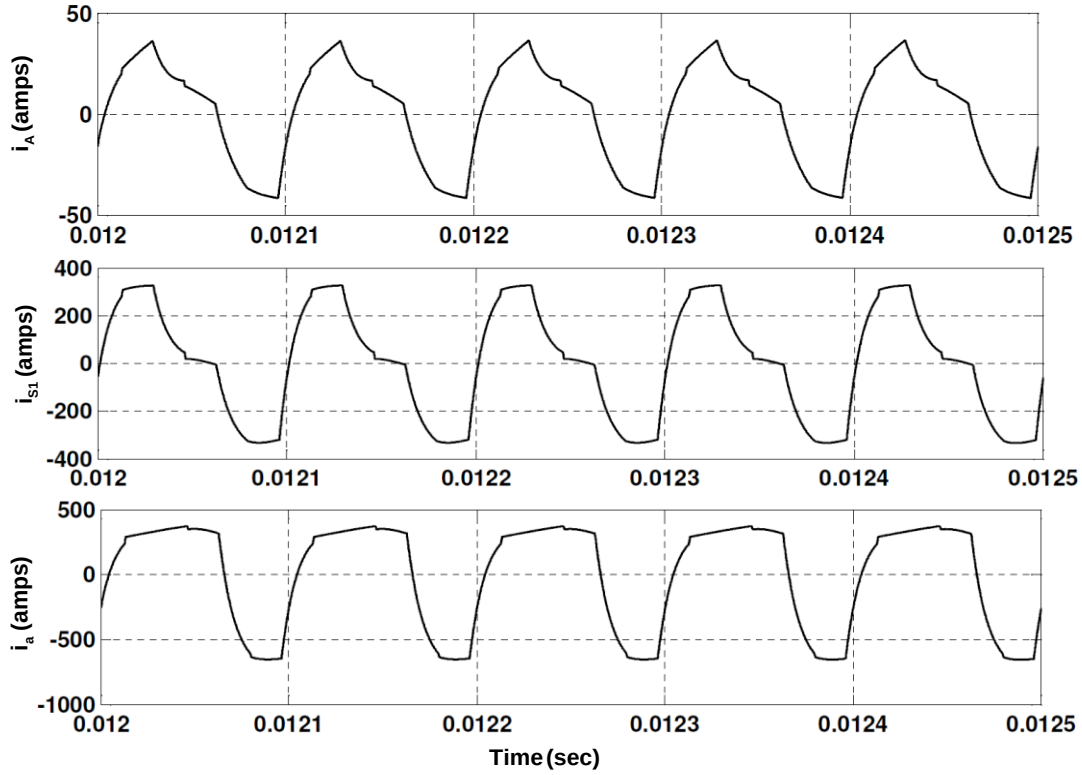


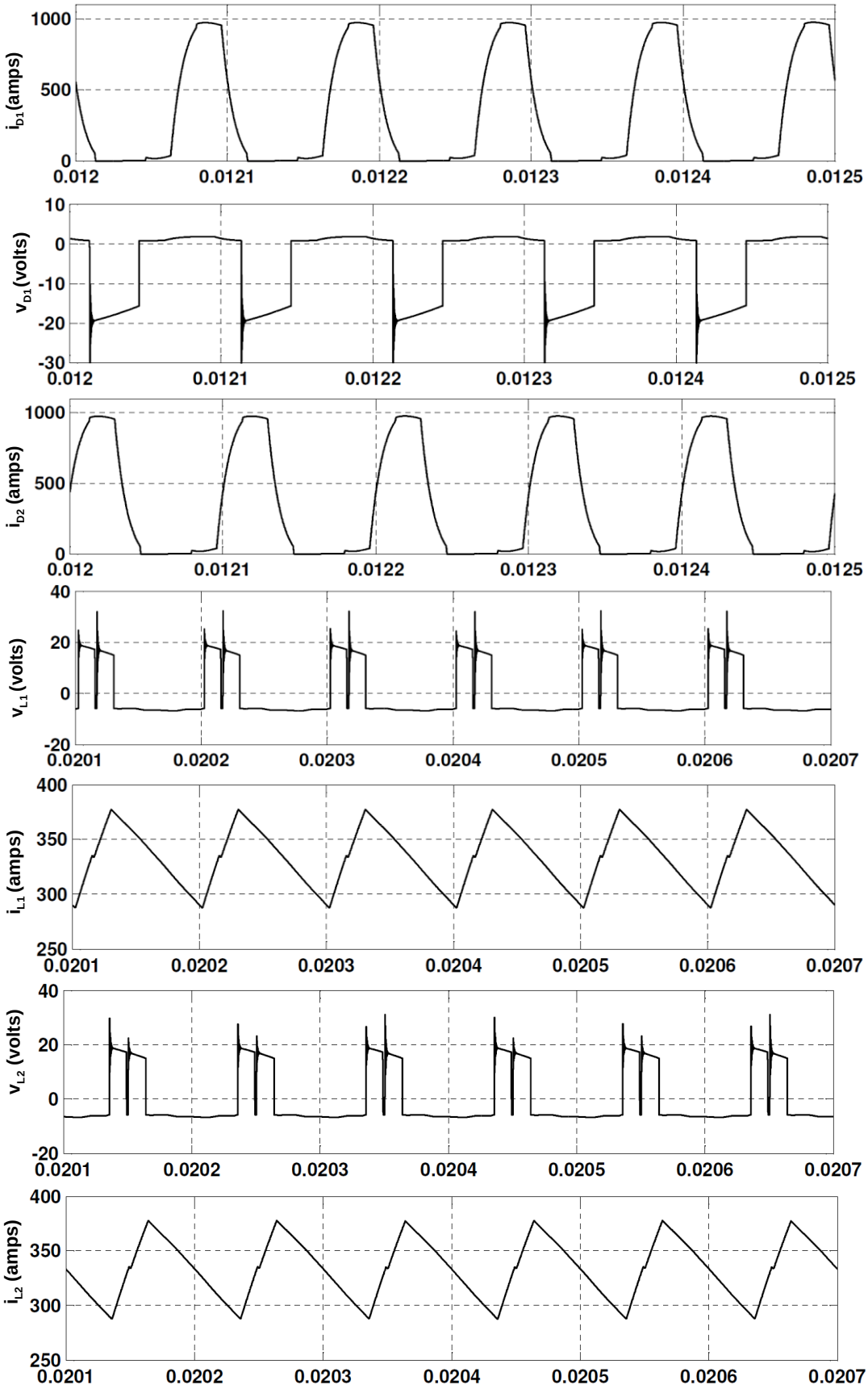
Fig. 5.12 Winding currents (i_A, i_{s1}) and secondary line current (i_a) waveforms of transformer (T_1)

Fig. 5.13 illustrates voltage and current of output filter inductors at steady state conditions. It is observed that inductor shares one third of load current and individual inductor current ripple is large. Due to interleaved PWM control operation of converter, the ripple content in load current is reduced. Therefore, the size of output filter capacitor is reduced consierably.

Fig. 5.14 shows the voltage across the rectifier diodes (v_{D1}, v_{D2}, v_{D3}) and current (i_{D1}, i_{D2}, i_{D3}) which indicate that the peak current is same as that of the load current and during change over two rectifier diodes are conducting simultaneously. Therefore, power devices of lower on state resistance are to be chosen to reduce the conduction losses.

The transient performance of proposed converter is investigated with step change in input voltage and load. In Fig. 5.15, the load current is increased from 800A to 1000A at $t = 0.005$ sec and it further decreased from 1000A to 700A at $t = 0.021$sec and corresponding change in output voltage are observed. To study the performance of converter with input voltage variation, the input DC voltage V_{in} is increased from 600V to 700V at $t = 0.015$ sec and corresponding change in output voltage is observed in Fig. 5.15. It is further observed that currents sharing by output filter inductors under all above perturbations are found satisfactory as shown in Fig. 5.16.

Over all, It is observed that irrespective of various disturbances such as input voltage and load, the output voltage resumes *5V* quickly as depicted in Fig. 5.15. The response time can also be optimized by proper tuning of controller parameters.


i_{D1}(amps)
1000
500
0
0.012
0.0121
0.0122
0.0123
0.0124
0.0125
v_{D1}(volts)
10
0
-10
-20
-30
i_{D2} (amps)
v_{L1}(volts)
40
20
-20
0.0201
0.0202
0.0203
0.0204
0.0205
0.0206
0.0207
i_{L1}(amps)
400
350
300
250
v_{L2} (volts)
i_{L2} (amps)

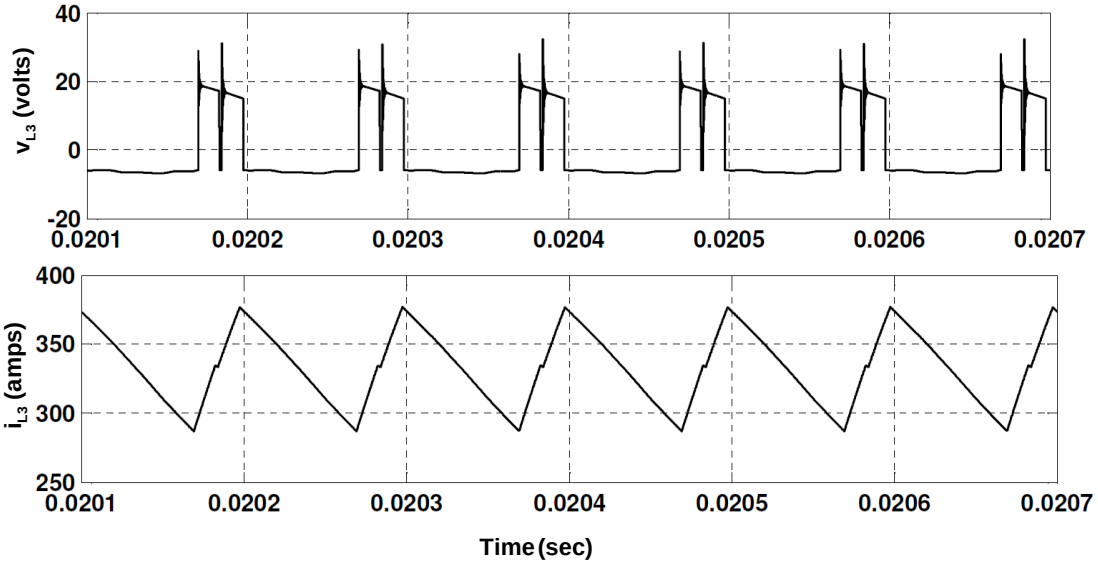


Fig. 5.13 Voltages (v_{L1},v_{L2},v_{L3}) and currents (i_{L1},i_{L2},i_{L3}) waveforms associated with output filter inductors with full load

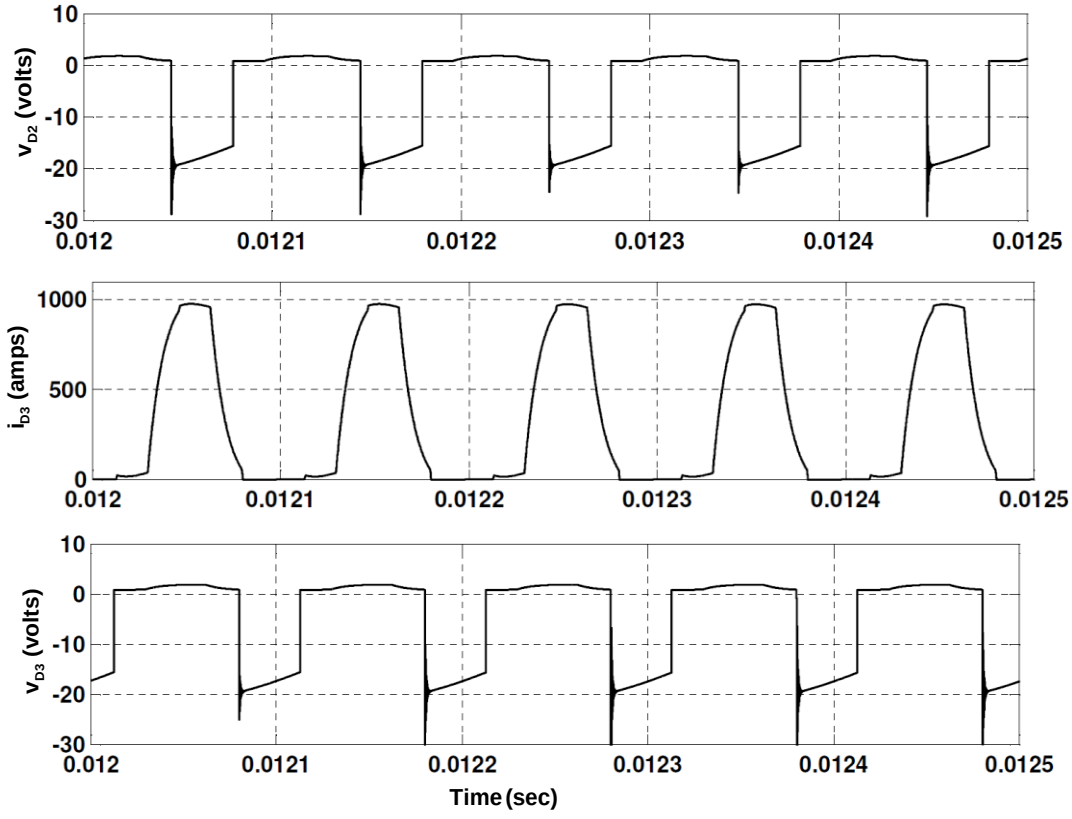


Fig. 5.14 Voltage (v_{D1},v_{D2},v_{D3}) and current (i_{D1},i_{D2},i_{D3}) waveforms of rectifier diodes with full load

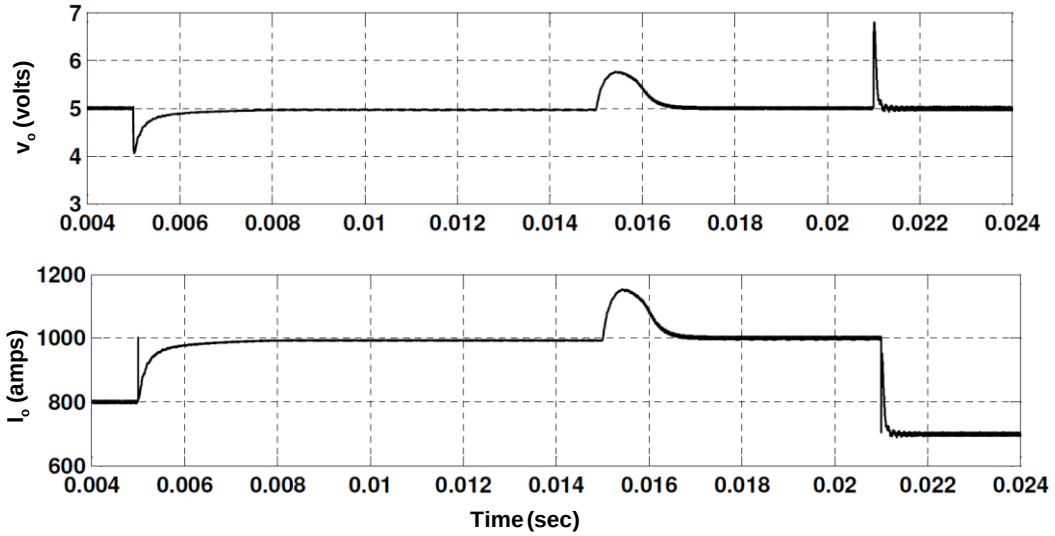


Fig. 5.15 Output voltage V_o (volts) and load current I_o (amps) during load perturbation at 0.005 sec and 0.021 sec and source perturbation at 0.015 sec.

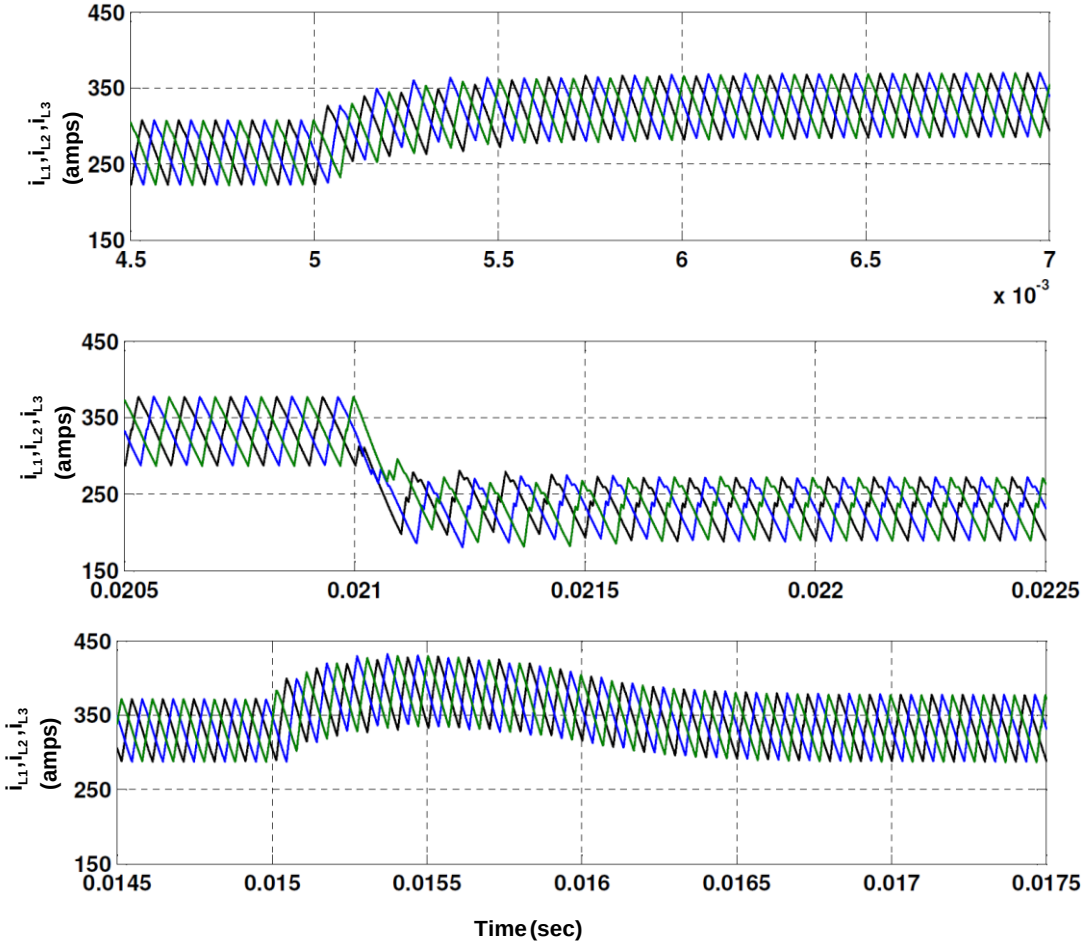
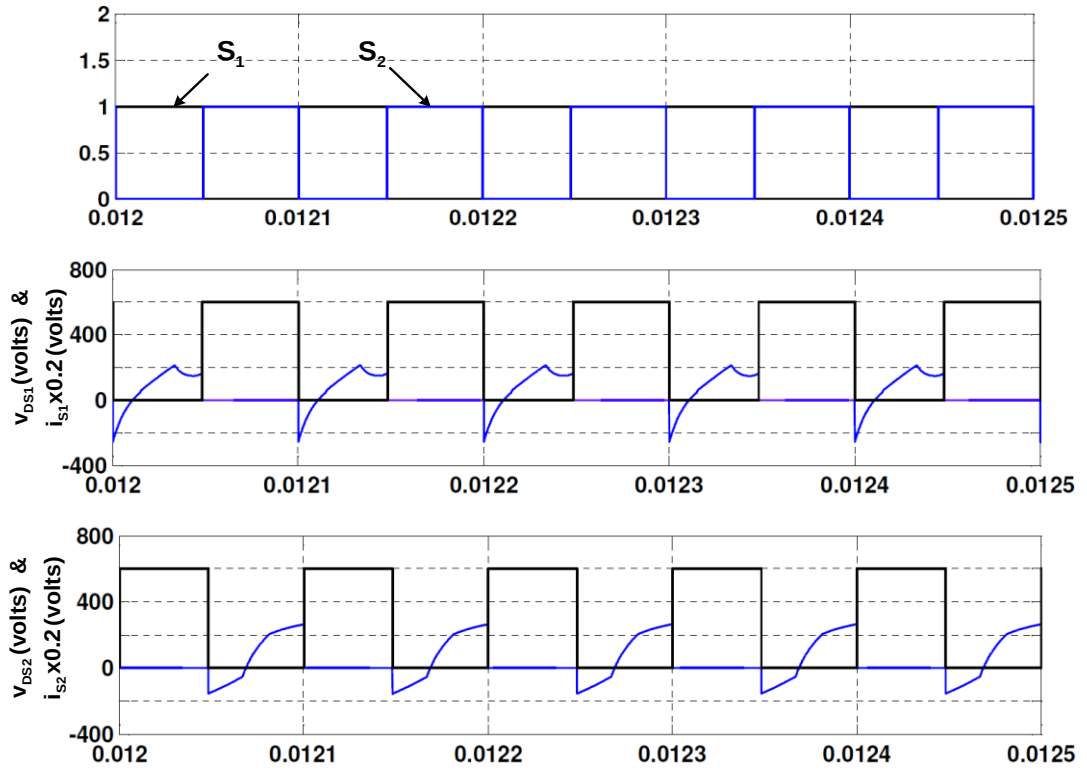


Fig. 5.16 Output filter inductor current during load perturbation at 0.005 Sec and 0.021 search and source perturbation at 0.015 sec.

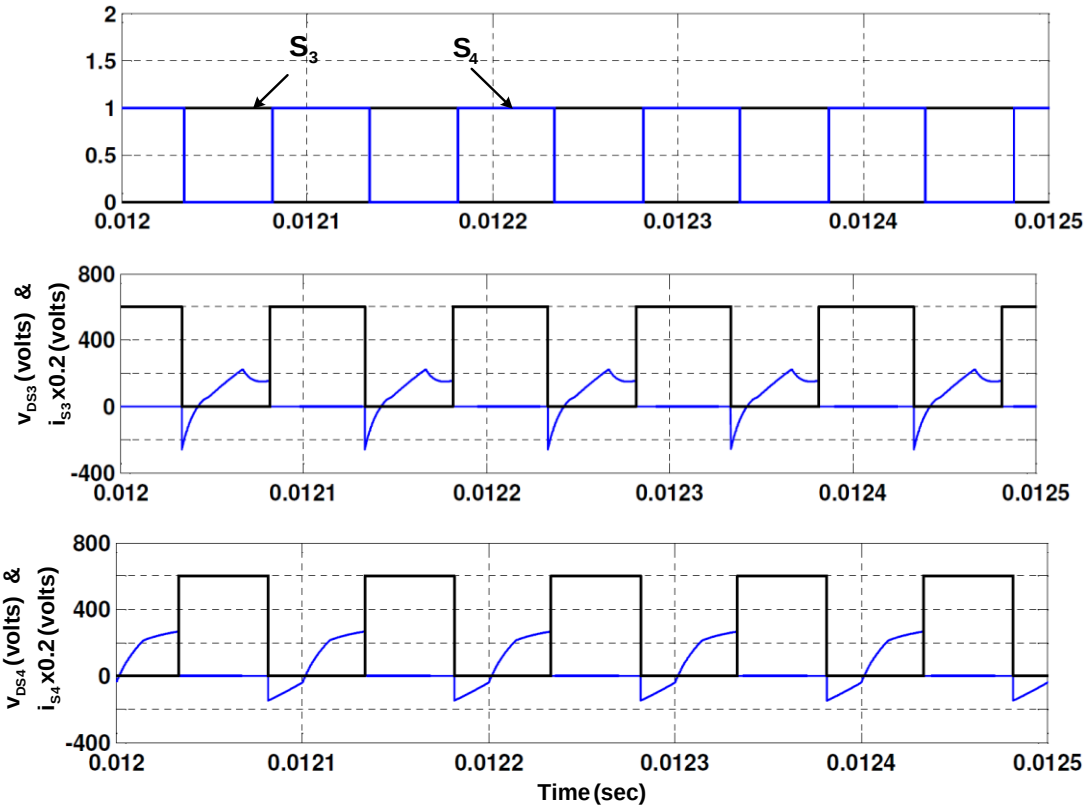
(b) Performance with Asymmetrical Control Method

The simulation studies of proposed converter with asymmetrical PWM control methods are carried output and obtained simulation results are presented in Fig. 5.17 to Fig. 5.22. Fig. 5.17 shows the switching PWM signals, drain to source voltage, and switch current for switches of front end converter which consists of three legs namely left, middle and right leg. The power switches (S_1, S_2), (S_3, S_4) and (S_5, S_6) are associated with left, middle and right leg respectively. It is observed that negative switch current flows through the body diode of switch and hence creating zero voltage switching condition for all switches over wide range of load. The three-phase phase voltages (v_{An},v_{Bn},v_{Cn}) of front end converter with two different input DC voltages (V_{in}= 600V, 700V) are depicted in Fig. 5.18. Fig. 5.18(a) shows waveforms of output phase voltage of front end converter, when converter operates in region (Reg2) with input DC voltage of 600V and delivers load current of 1000A at 5V. As input voltage is increased to 700V, the duty cycle of switches of front end converter reduces to deliver same load current. The phase voltages (v_{An},v_{Bn},v_{Cn}) of front end converter in Reg1 with V_{in} =700V are shown in Fig. 5.18(b). Fig. 5.19 and Fig. 5.20 show the steady-state waveforms of voltage across rectifier diodes (v_{D1}, v_{D2}, v_{D3}) and diode currents (i_{D1}, i_{D2}, i_{D3}) at 100% and 70% of full load. As the three legs of front end converter, operate in interleaved manner, each output filter inductor carries one-third of the load current as shown in Fig. 5.21. It is observed that ripple content in each inductor current is large, but ripple content in total current $(i_{L1} + i_{L2} + i_{L3})$ is reduced significantly due to equal phase-shifted operation.

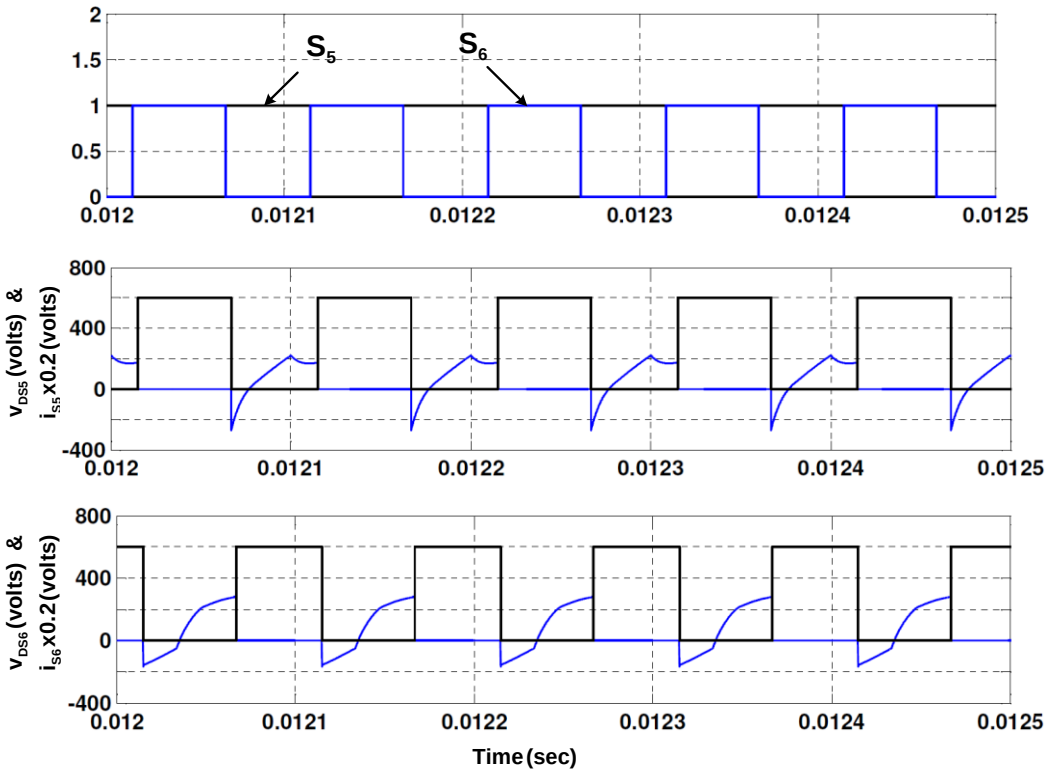
In addition to the steady-state waveforms, the performance of proposed converter under asymmetrical control method is also investigated under transient conditions. In Fig. 5.22, the step change in load from 800A to 1000A at $t = 0.005$ sec and from 1000A to 700A at $t = 0.021$ sec are done and corresponding change in output voltage is observed. Furthermore, the variation in input DC voltage is introduced at $t = 0.015$ sec and output voltage of converter is observed as shown in Fig. 5.22. It is observed that the output voltage resumes its reference value after some delay from the point of disturbance and its dynamic response can be improved by proper selection of controller parameters.


S1
S2
2
1.5
1
0.5
0
0.012
0.0121
0.0122
0.0123
0.0124
0.0125
800
400
0
-400
vDS1(volts) & iS1x0.2(volts)
vDS2(volts) & iS2x0.2(volts)

(a)


S3
S4
2
1.5
1
0.5
0
0.012
0.0121
0.0122
0.0123
0.0124
0.0125
800
400
0
-400
vDS3(volts) & iS3x0.2(volts)
vDS4(volts) & iS4x0.2(volts)
Time(sec)

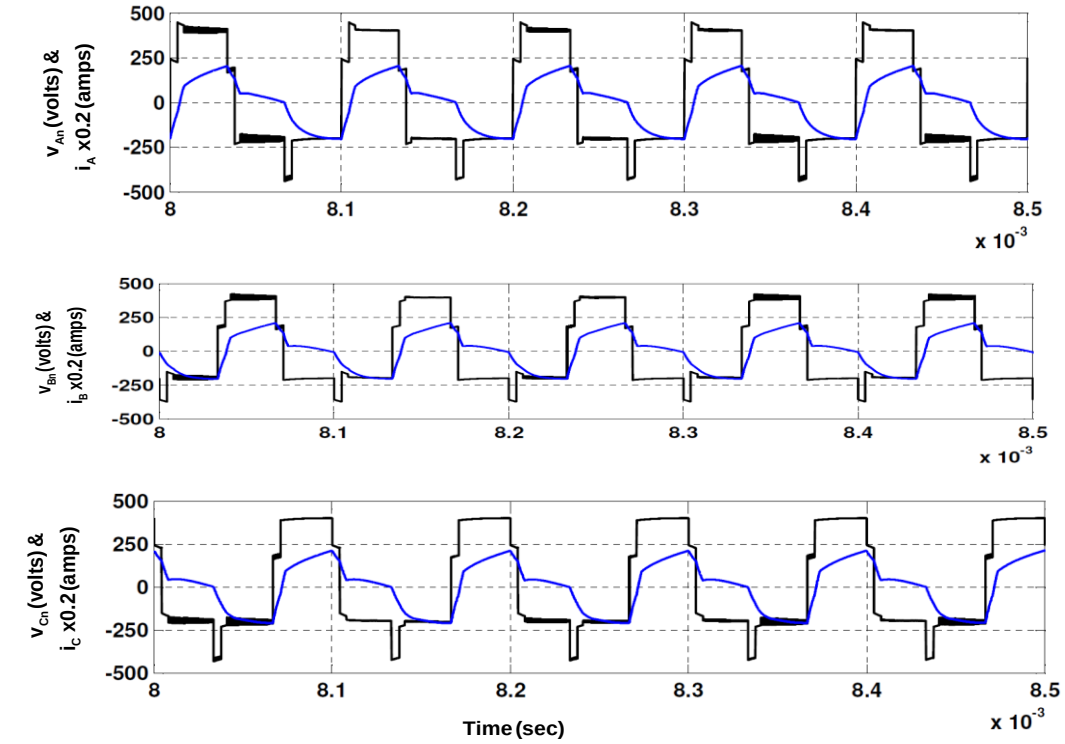
(b)



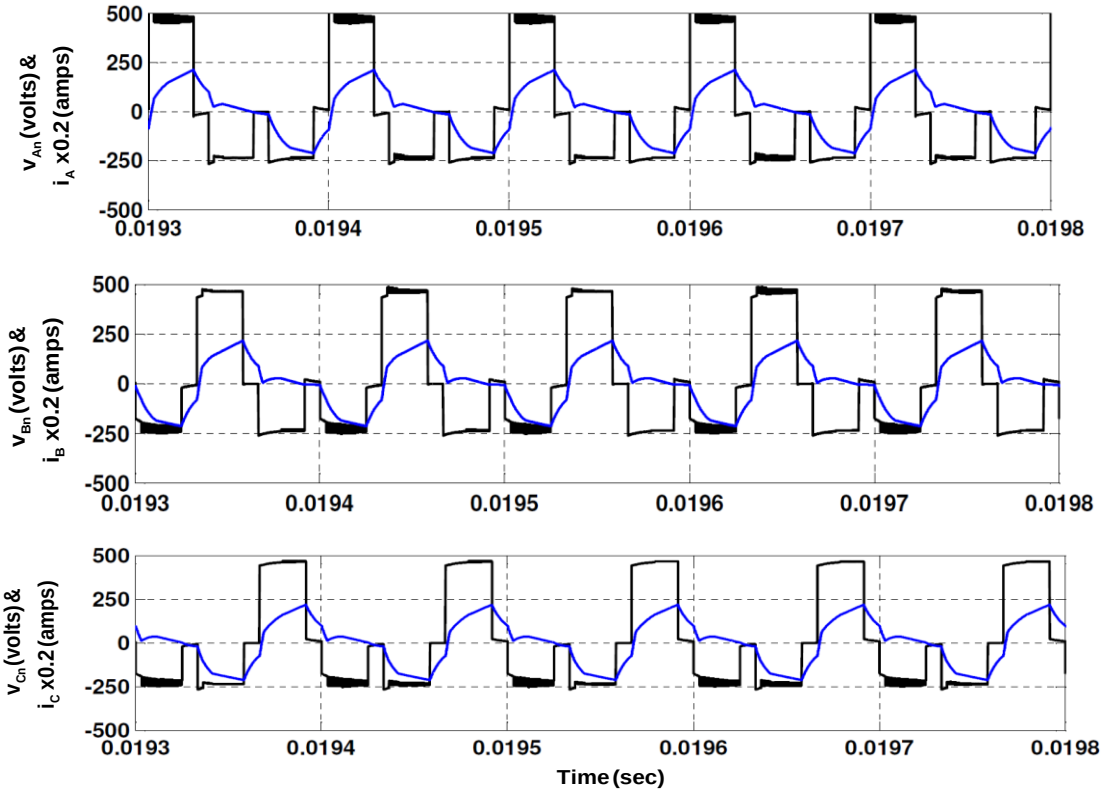
(c)

Fig. 5.17 Voltage and current waveforms of switches of front end converters

(a) left leg (b) middle leg (c) right leg



(a)



(b)

Fig. 5.18 Phase voltages (v_{an},v_{Bn} & v_{Cn}) and primary line currents (i_A,i_B &i_C) with source voltage (a) V_{in}= 600V at full load(b) V_{in}= 700V at full load.

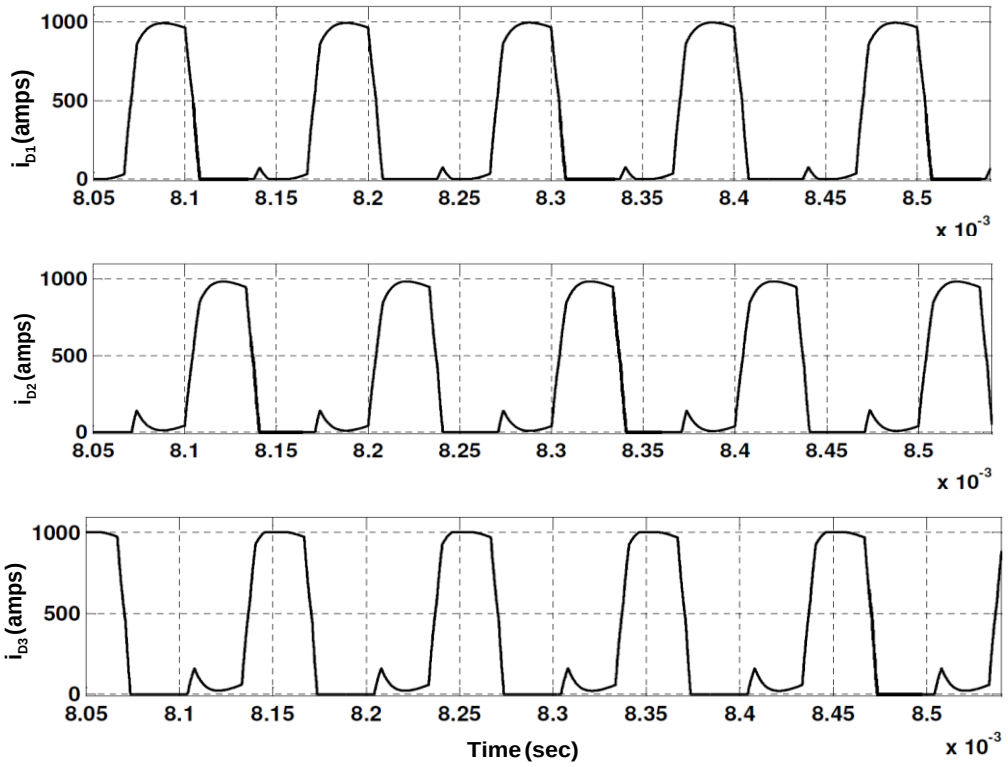


Fig. 5.19 Waveform of rectifier diode currents (i_{D1},i_{D2}& i_{D3}) at full load

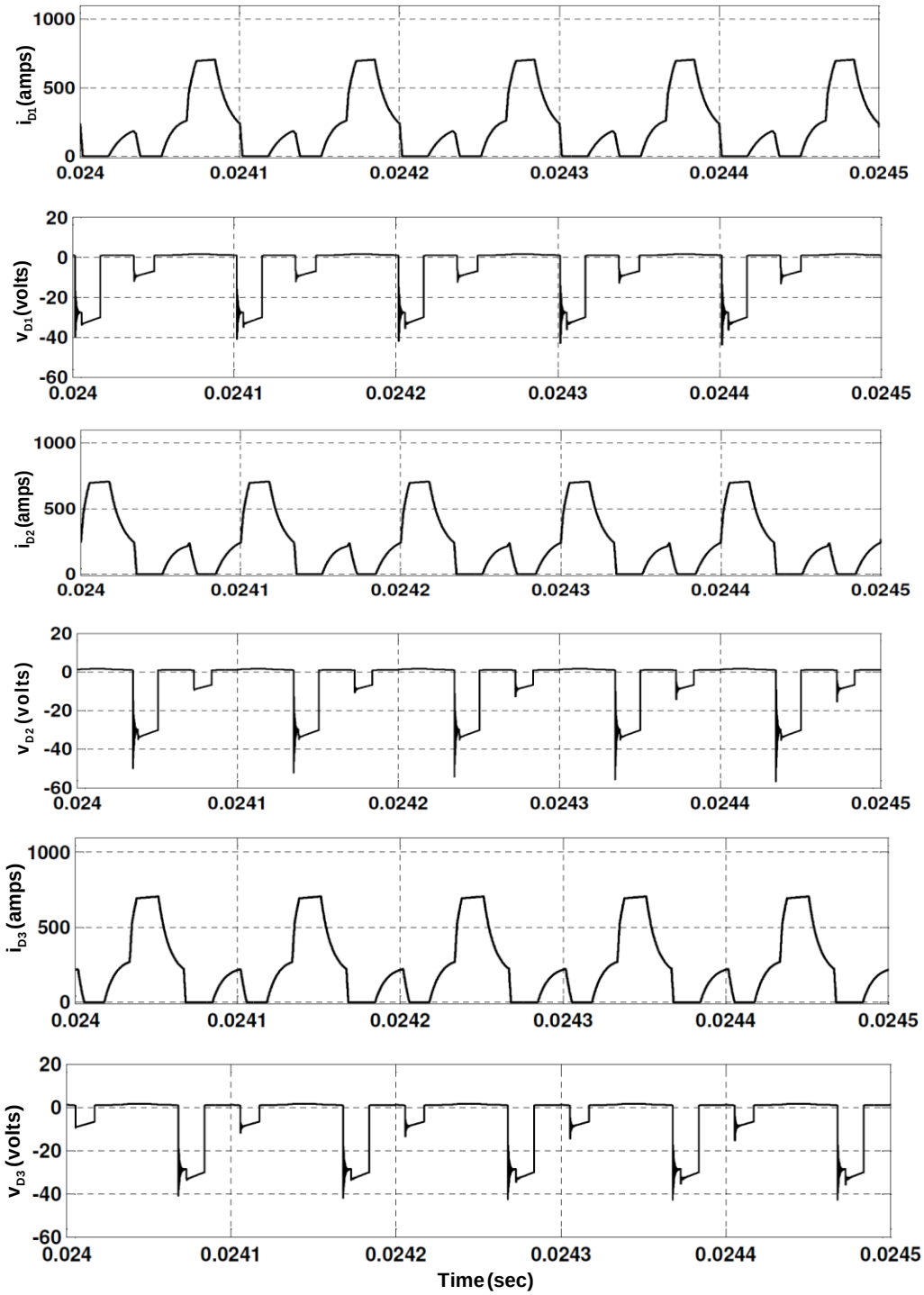


Fig. 5.20 Voltages (v_{D1},v_{D2},v_{D3}) and currents (i_{D1},i_{D2}& i_{D3}) waveforms of rectifier diodes at 70% of full load

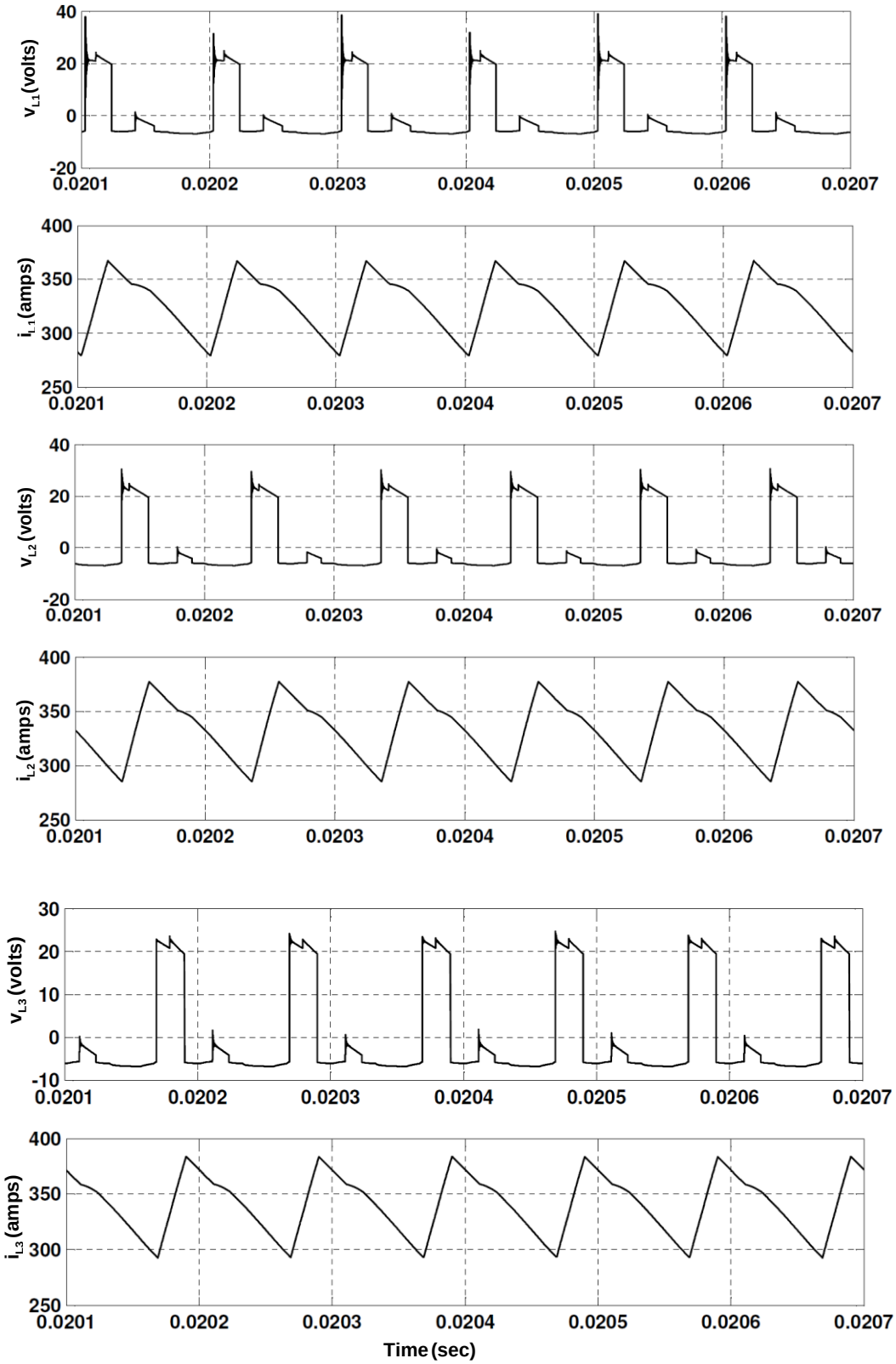


Fig. 5.21 Voltage and currents waveforms of output filter inductors

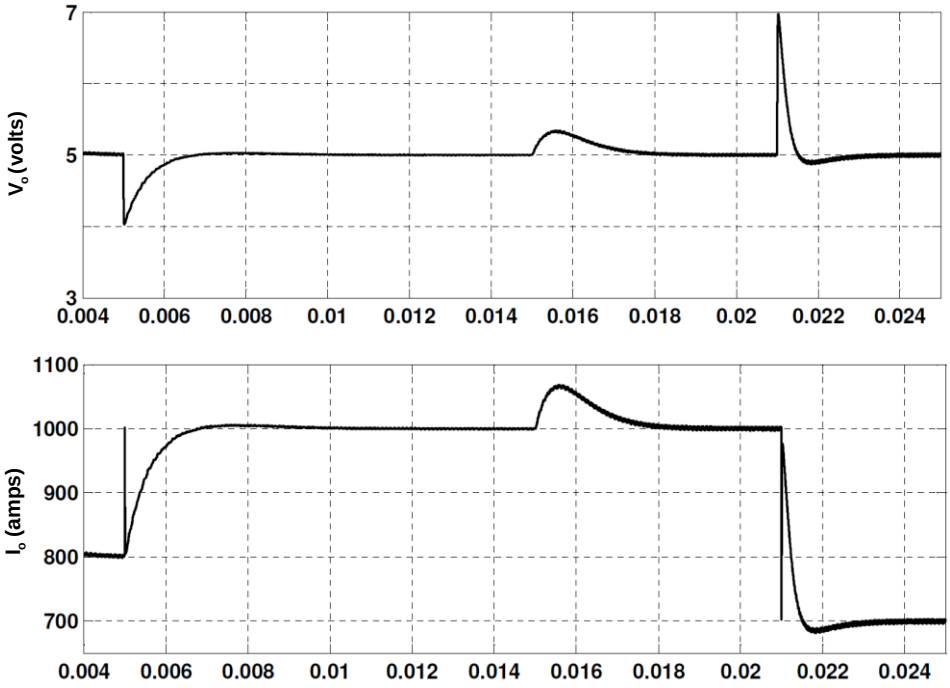
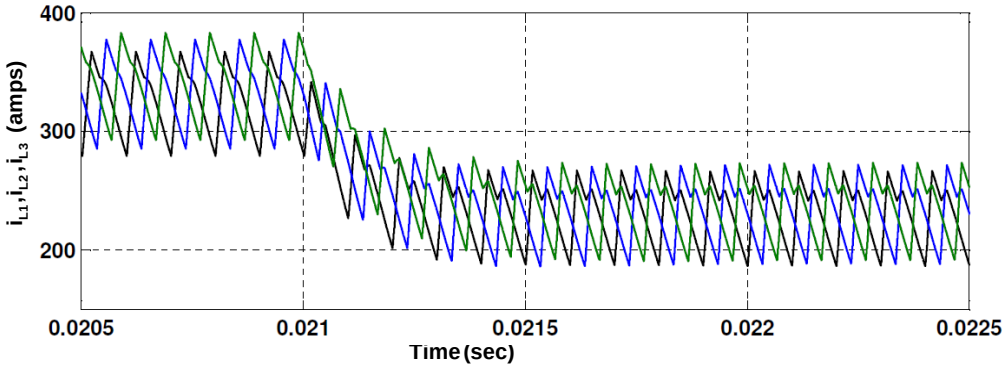
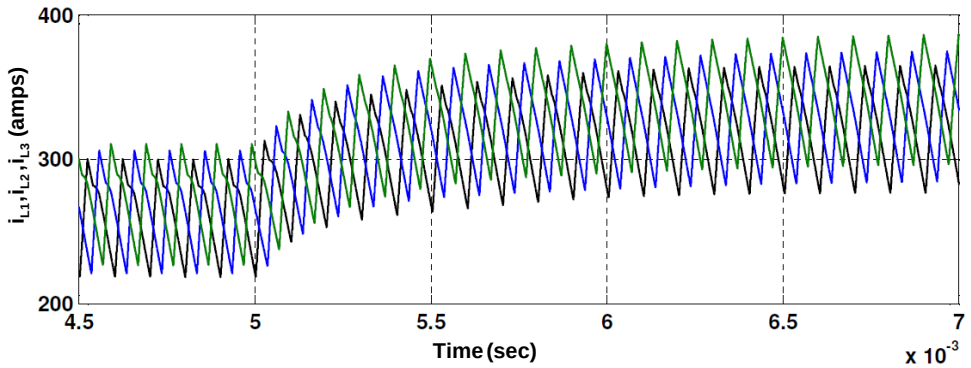


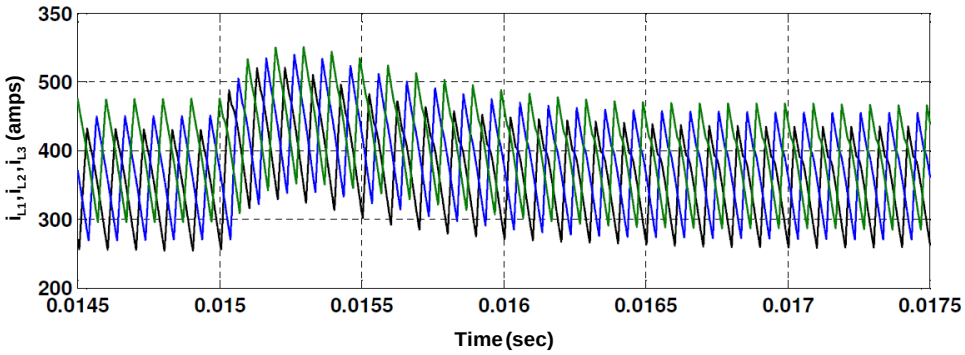
Fig. 5.22 Variation of output voltage (V_o) with load variation from 800A to 1000A at 0.005 sec and from 1000A to 700A at 0.021 sec and source voltage variation from 600V to 700V DC at 0.015 sec.



(a)



(b)



(c)

Fig. 5.23 Transient response of output inductor currents (i_{L1},i_{L2}& i_{L3}) with (a) load perturbation at 0.021 sec from 100% to 70% load (b) load perturbation at 0.005 sec from 80% to 100% load (c) perturbation in source voltage 600V to 700V at 0.015 sec.

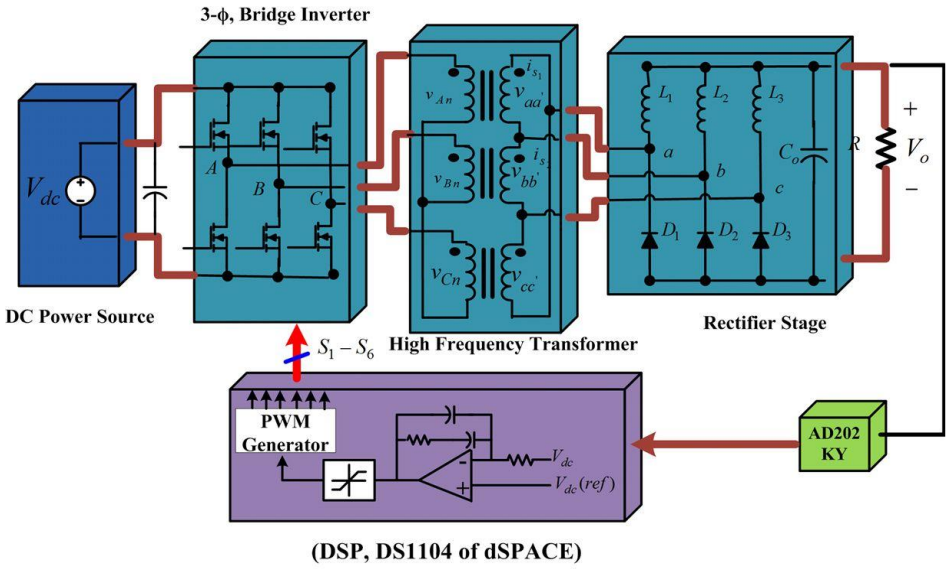


Fig. 5.24 Schematic diagram of three-phase high frequency isolated DC-DC converter

Table 5.2 Specification of hardware components

Parameter	Specifications
Input voltage	220V, DC
Output power	1.5V, 50A
Switching frequency	1kHz
Power switches $(S_1 - S_6)$	IRFP460A, 500V, 20A
Rectifier diodes (D_1, D_2, D_3)	25D40R
High frequency transformer (3 units)	1-Φ,250VA,150/25V, $\frac{N_s}{N_p} = 0.1667$, E65 ferrite $L_p = 26.76 - 304.2\mu H$ $L_s = 2.754 - 3.0102\mu H$
Filter inductor (3units)	5mH
Output capacitor	1000 µF,50V

5.6 Experimental Validation

5.6.1 A Prototype Model

In simulation studies of proposed three-phase high frequency isolated DC-DC converter, rated at 5 kW, 5V/1000A is realised with symmetrical and asymmetrical PS-PWM method. But, due to the practical constraints, a 75 W, 1.5V/50A prototype proposed model is built with the specifications given in Table 5.2. As the experimental studies are conducted at a reduced rating of converter, for validating the experimental results, the simulation study at reduced equivalent rating of converter is also carried out. The complete system hardware consists of power circuit and control circuit and its schematic diagram is shown in Fig. 5.24.

The power circuit of the proposed converter comprises of six power MOSFETs $(S_1 - S_6)$ of front end converter, a set of three high frequency transformers, and load end converter consisting of rectifier power diodes $(D_1 - D_3)$ and output filters $(L_1, L_2, L_3 \,\&\, C_o)$ as shown in Fig. 5.24.

A DSP DS1104 of dSPACE is used for the real-time simulation and implementation of control algorithms. The control algorithm is first designed in the MATLAB SimPowerSystem tools software and the Real-Time Workshop of MATLAB automatically generates the optimized C-code for real-time implementation. The interface between MATLAB and Digital Signal Processor (DSP, DS1104 of dSPACE) allows the control algorithm to be run on the hardware, which is an MPC8240 processor. The master bit I/O is used to generate the required six gate pulses and one analog to digital converters (ADCs) to implement close loop control. Switching signals obtained from controller are given to the power MOSFETs $(S_1 - S_6)$ after proper isolation and amplification.

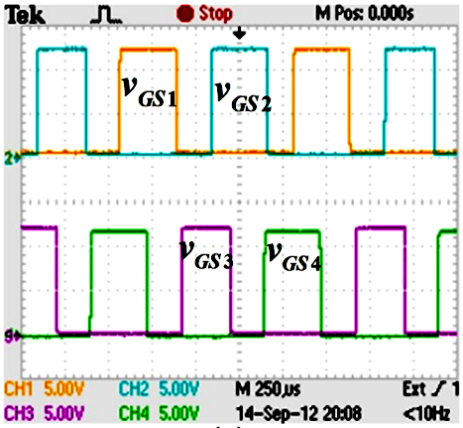
5.6.2 Experimental Results and Discussions

A prototype model of 75W, 1.5V/50A is built with the aforementioned specifications tabulated in Table 5.2. The developed converter is tested under different operating conditions with symmetrical and asymmetrical control methods and obtained results are presented in Fig.5.25 to Fig.5.34. To validate the experimental result of proposed three-phase isolated DC-DC converter under both control methods, simulation results of same rating simulink model are also presented along with experimental results.

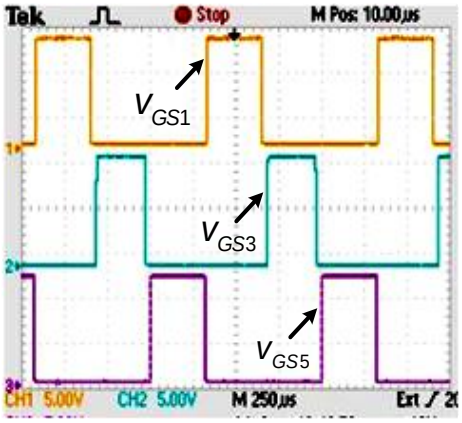
(a) Steady-State Performance of Converter with Symmetrical Control

The experimental results presented in Fig.5.25 to Fig. 5.29 are associated with proposed converter under symmetrical controlled method. Fig.5.25 shows experimentally obtained switching pulses across gate to source terminal of switches $(S_1 - S_6)$ under symmetrical control methods. Fig.5.26 shows gate to source voltage, drain to source voltage

and switch current associated with power switches (S_1, S_2) of front end converter. In Fig.5.26(a), it is observed that when switching signal, v_{GS1} appears across S_1, the positive current (i_{S1}) start flowing from drain to source and during this period darin to source voltage appears across S_2 is input voltage $(v_{DS2} = V_{in})$. It is further observed that prior to switching signal, the current through switches i_{S1} becomes negative for small duration, indicating that anti-parallel diode of switch is conducting. Therefore, Zero Voltage Switching is achieved. In waveforms of v_{DS1} & v_{DS2} in Fig.5.26(b), small distortion is observed which is because of failure of ZVS condition at certain load. This happens due to crossing of line current waveforms to zero value before start of new switching cycle.



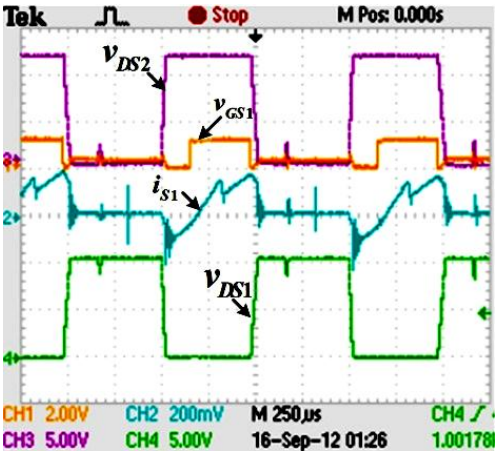
(a)



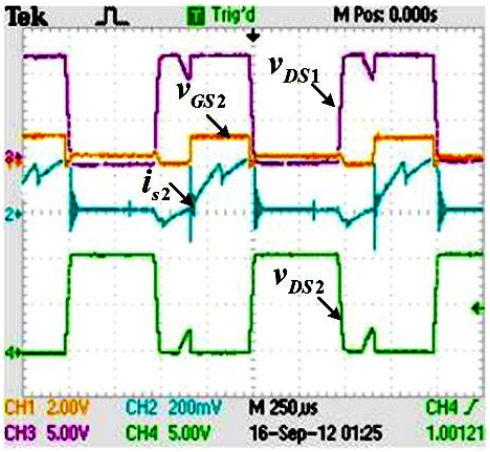
(b)

$(v_{GS}: 5V/div, X-axis: 250\,\mu s/div)$

Fig.5.25 Switching signals of switches $(S_1 - S_6)$ (a) $v_{GS1}, v_{GS2}, v_{GS3}$ & v_{GS4} (b) v_{GS1}, v_{GS3} & v_{GS5}



(a)

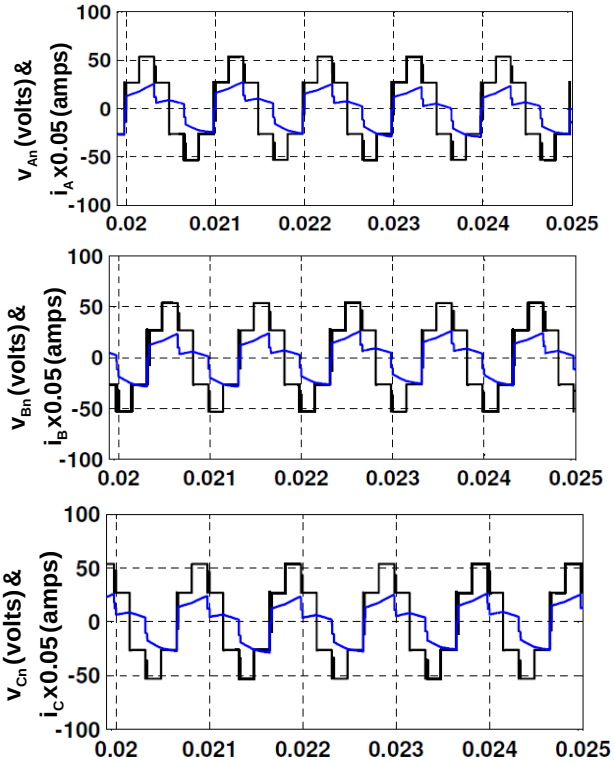


(b)

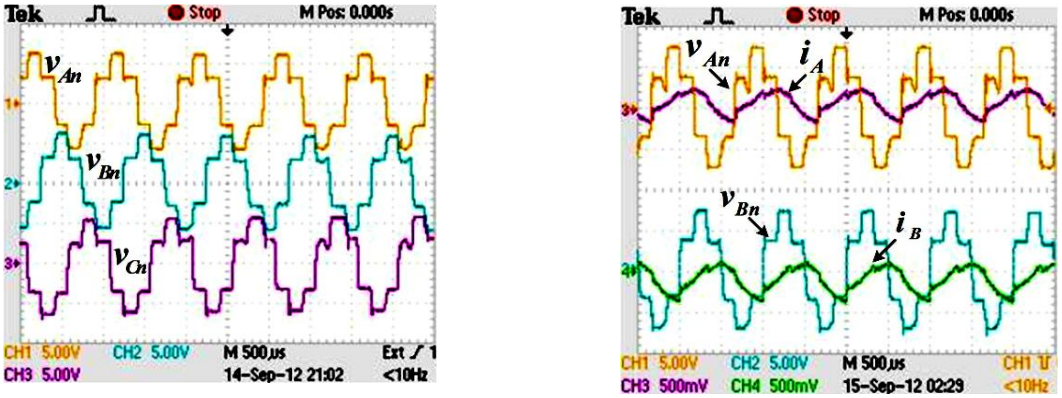
$(v_{DS1}$ & $v_{DS2}: 50V/div, i_{S1}$ & $i_{S2}: 2A/div, v_{GS1}$ & $v_{GS2}: 20V/div, X-axis: 250\,\mu s/div)$

Fig.5.26 Voltage & current waveforms of switches S_1, S_2 (a) $v_{GS1}, v_{DS1}, v_{DS2}$ & i_{S1} (b) $v_{GS2}, v_{DS1}, v_{DS2}$ & i_{S2}

Fig. 5.27 shows the steady-state waveform of phase voltage (v_{An}, v_{Bn}, v_{Cn}), primary currents (i_A, i_B), with input dc voltage, $V_{in} = 110V$ under symmetrically controlled converter. In this case, proposed converter operates in operating region(Reg3) and experimental results obtained of phase voltages are symmetrical about time-axis and phase-shifted by 120^0.



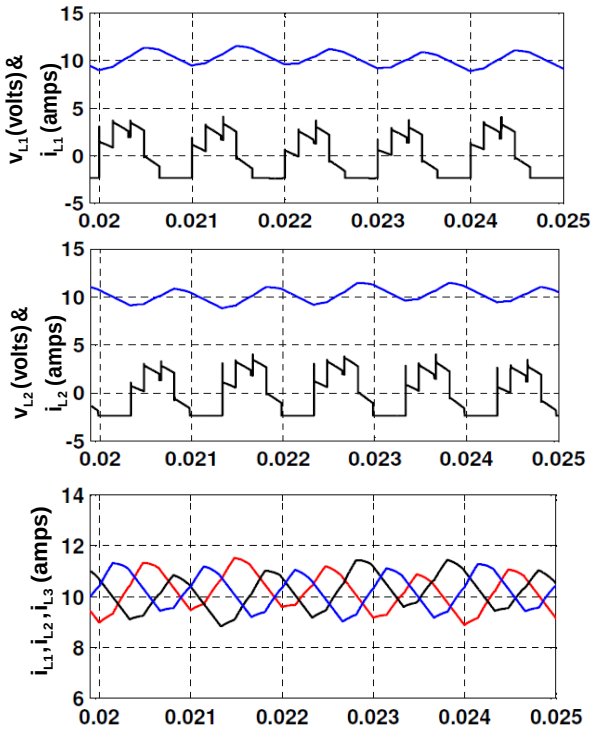
(a)



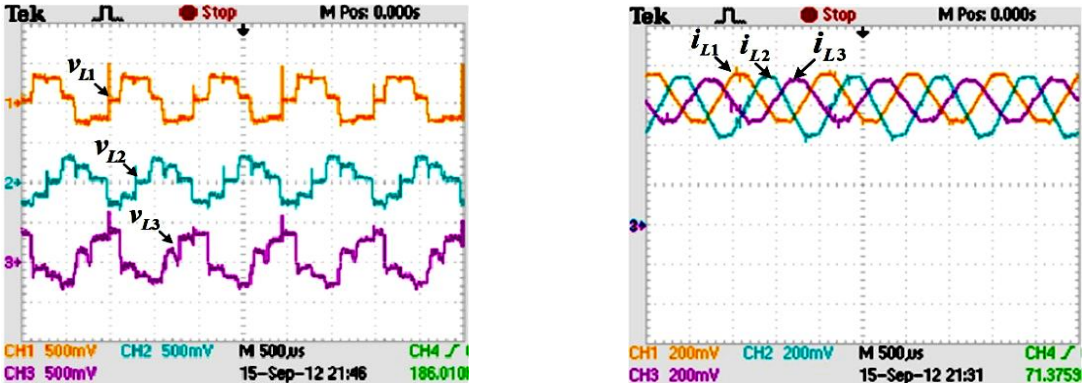
(b)

$(v_{An}, v_{Bn} \& v_{Cn} : 50V/div, i_A \& i_B : 2A/div)$

Fig. 5.27 Phase voltages (v_{An}, v_{Bn}, v_{Cn}) and primary currents (i_A, i_B, i_C) waveforms of front end converter (a) Simulation (b) Experimental



(a)

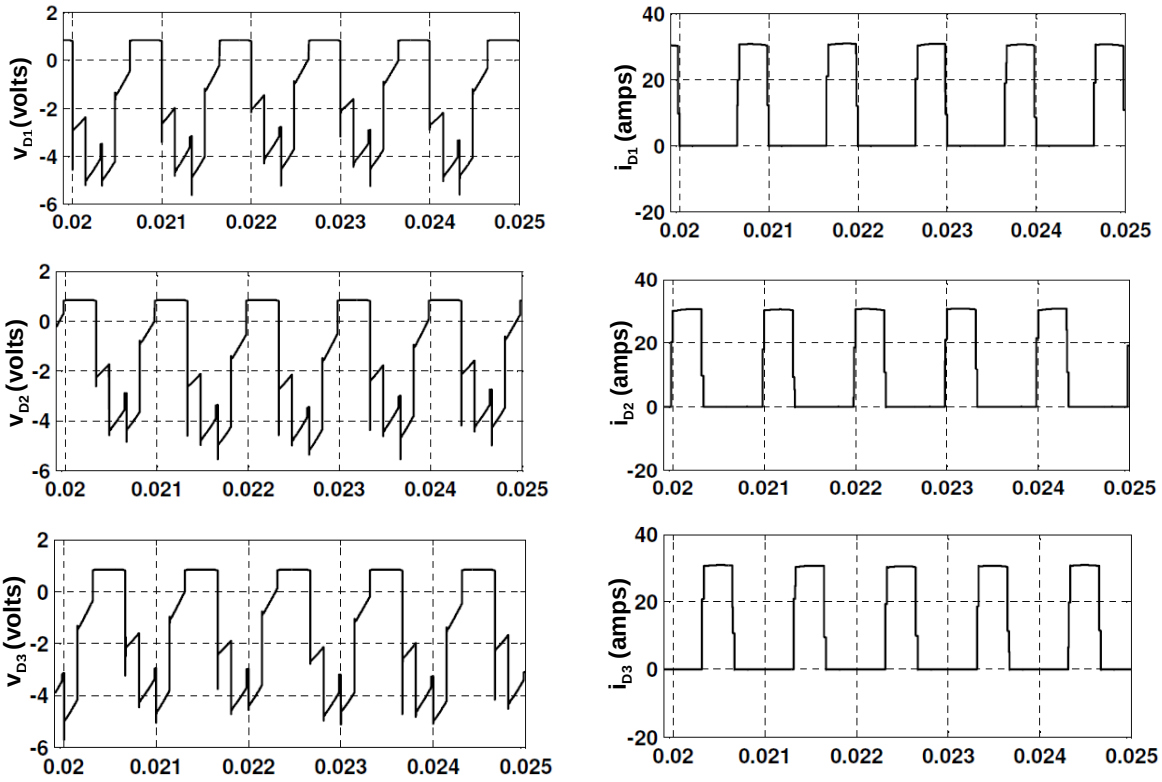


(b)

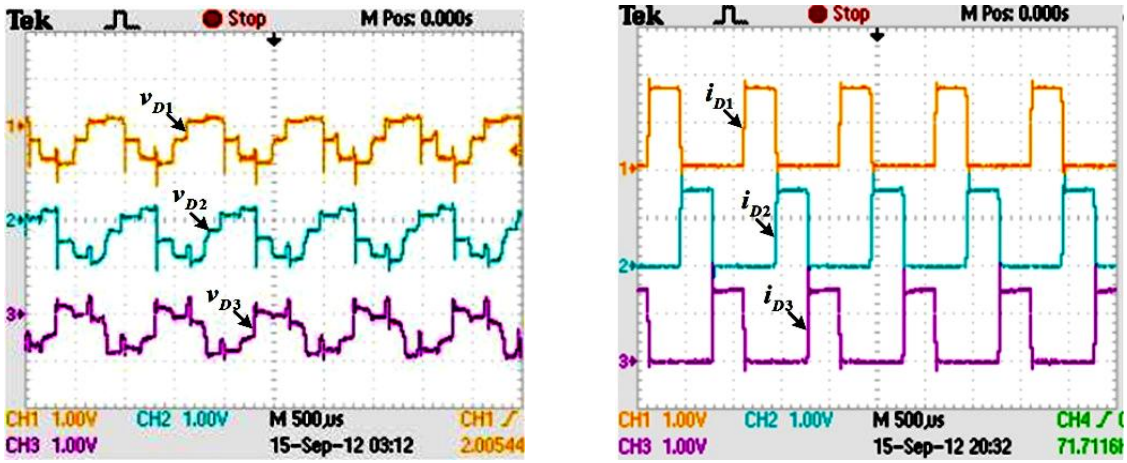
$(v_{L1}, v_{L2} \& v_{L3}: 5V/div, i_{L1}, i_{L2} \& i_{L3}: 3A/div)$

Fig. 5.28 Voltage $(v_{L1}, v_{L2} \& v_{L3})$ and currents (i_{L1}, i_{L2}, i_{L3}) waveforms of output filter inductors

(a) Simulation (b) Experimental



(a)



$(v_{D1}, v_{D2} \& v_{D3}: 5V/div, i_{D1}, i_{D2} \& i_{D3}: 15A/div)$

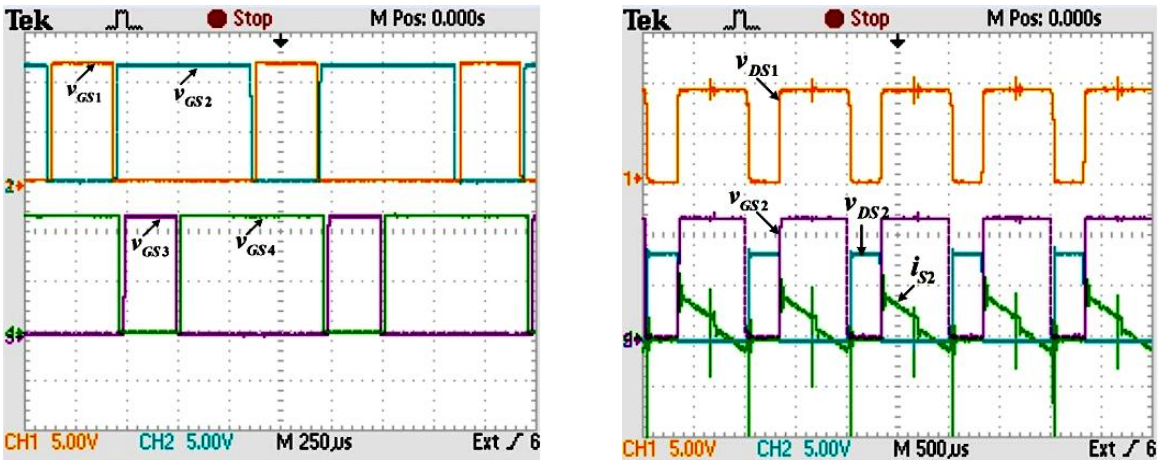
(b)

Fig. 5.29 Voltages (v_{D1}, v_{D2}, v_{D3}) and currents (i_{D1}, i_{D2}, i_{D3}) waveforms associated with rectifier diodes (a) Simulation (b) Experimental

The output filter inductors share one third of load current and individual inductor current ripple is large, but ripple content in total current $(i_{L1} + i_{L2} + i_{L3})$ is reduced significantly due ripple concellation as shown in Fig. 5.28. Fig. 5.29 shows the voltage and current associated with rectifier diodes, which indicates that average value of rectifier diode is reduced, thus there is significant reduction of heat dissipation in secondary side.

(b) Steady-State Performance of Converter with Asymmetrical Control

The performance of proposed three-phase high frequency isolated DC-DC converter is also investigated using asymmetrical interleaved control methods. For validating the experimental results, simulation results of reduced equivalent rating of converter are also presented. Fig.5.30(a) shows experimentally obtained switching signals for switches $(S_1 - S_4)$ of front end converter in which switches of same leg are operated in complementary manner. Fig.5.30(b) shows drain to source voltage of switches (S_1, S_2), gate to source voltage and current associated with switches (S_2).

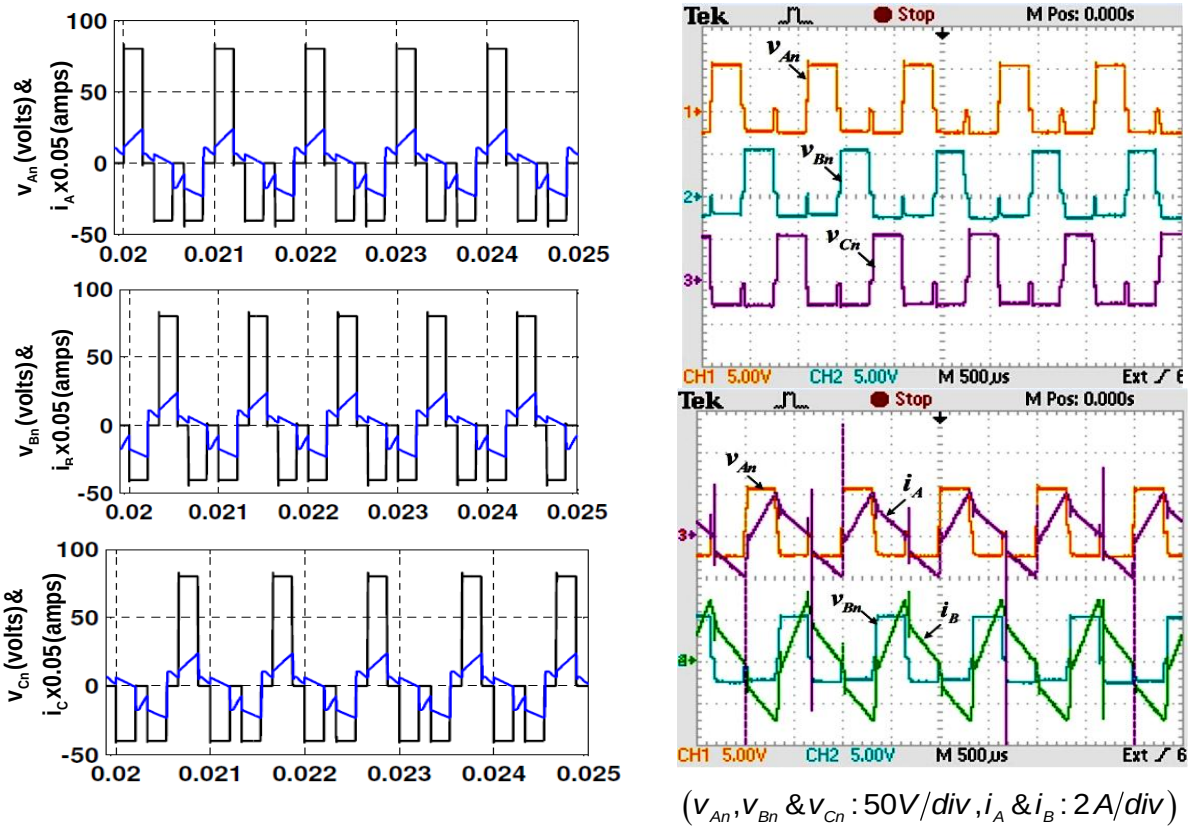


(a) (b)

$(v_{DS1} \& v_{DS2} : 50V/div, i_{S1} \& i_{S2} : 2A/div, v_{GS1} \& v_{GS2} : 5V/div)$

Fig.5.30 Voltage & current waveforms of power switches $(S_1 - S_4)$ (a) $v_{GS1}, v_{GS2}, v_{GS3} \& v_{GS4}$ (b) $v_{DS1}, v_{DS2}, v_{GS2} \& i_{S2}$

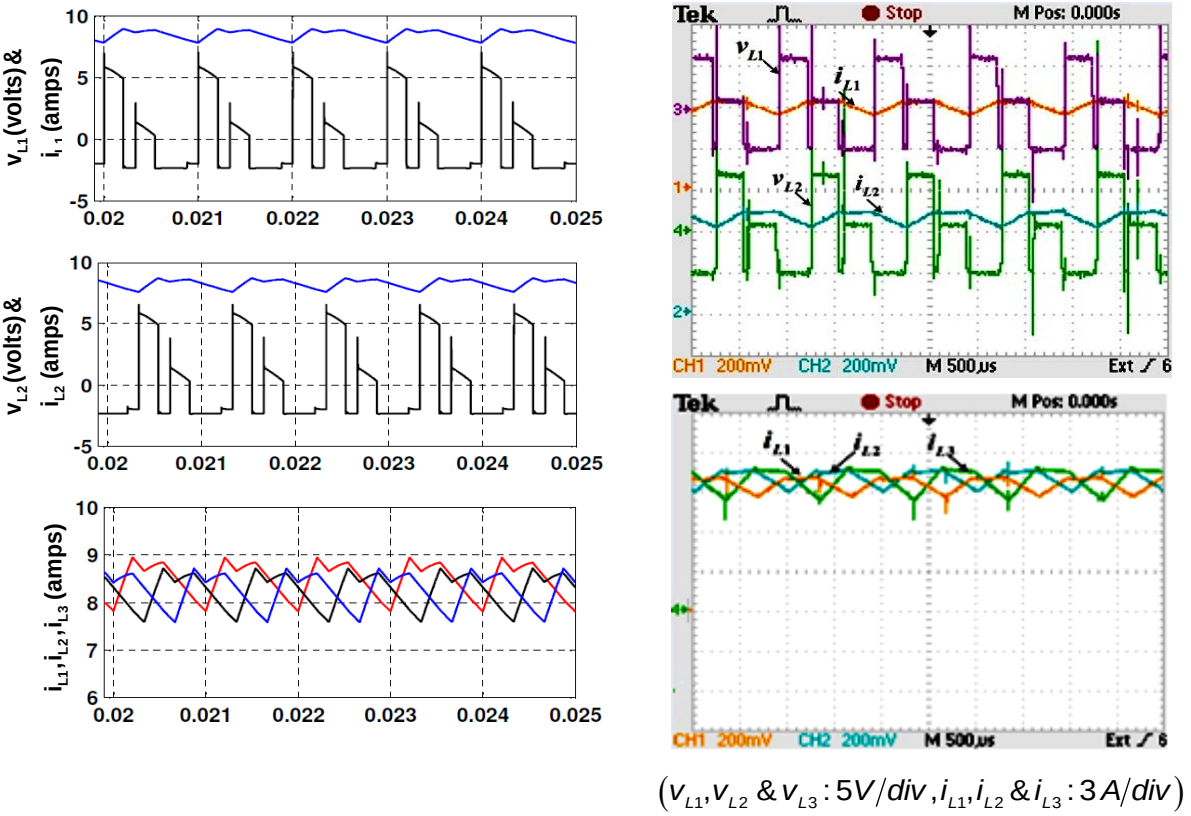
The steady-state waveforms of phase voltage (v_{An}, v_{Bn}, v_{Cn}) and currents (i_A, i_B) of front end converter obtained from Simulink model and prototype model are depicted in Fig.5.31. It is observed that wavefroms obtained from both model are similar and converter operates in operating region (Reg1). In Fig.5.32, simulation and experimental results of voltage across output filter inductors and current through inductors are psesented. In this case also each output inductors share one third of load current and ripple content in individual inductor current is large, but lesser than that of symmetrical control method. The ripple content in total current $(i_{L1} + i_{L2} + i_{L3})$ is reduced significantly due to ripple concellation effect. Fig.5.33 shows voltage and current of rectifier diodes. The spikes observed in voltage and current waveforms of various circuit parameters are due to hard switching of power switching devices and rectifier diodes. These spikes in voltage and current waveforms can be eliminated through proper design of snubber circuit of devices and implementation of soft switching techniques.



$(v_{An}, v_{Bn} \& v_{Cn} : 50V/div, i_A \& i_B : 2A/div)$

(a) (b)

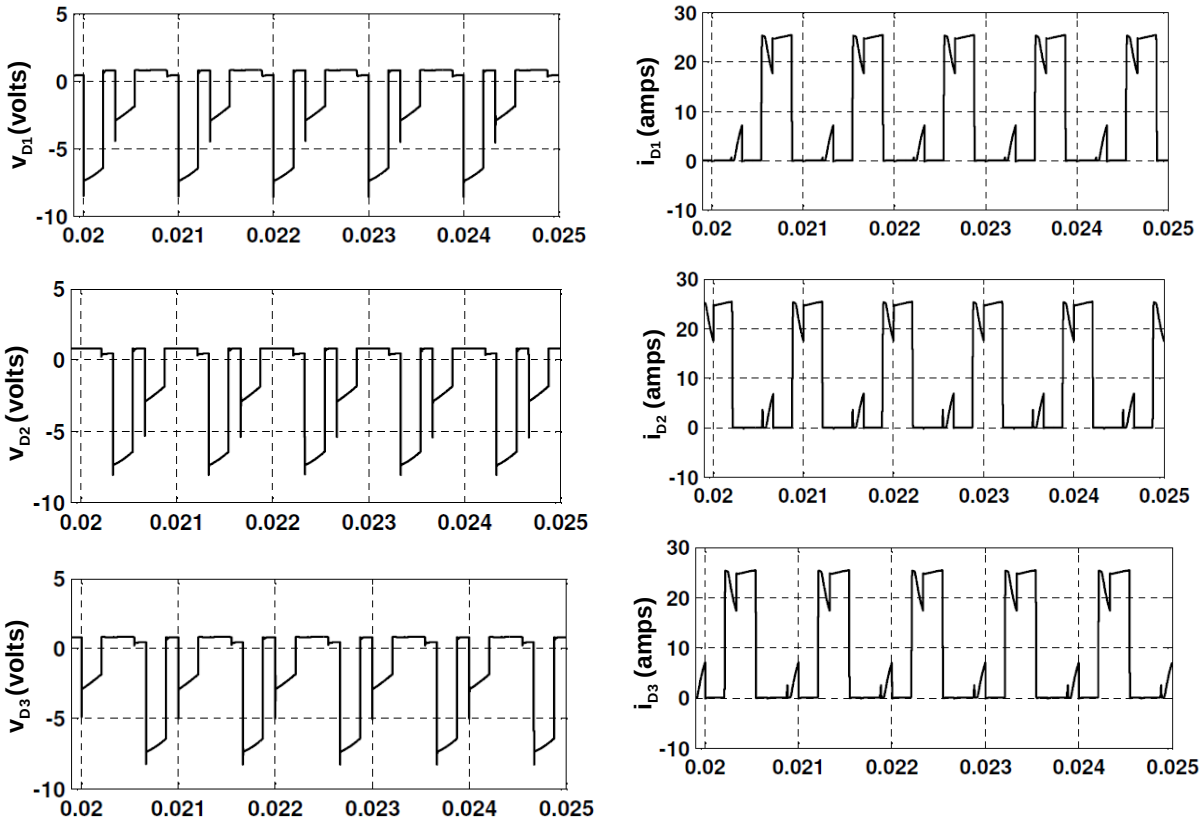
Fig.5.31 Phase voltages (v_{An}, v_{Bn}, v_{Cn}) and currents (i_A, i_B, i_C) (a) Simulation (b) Experimental



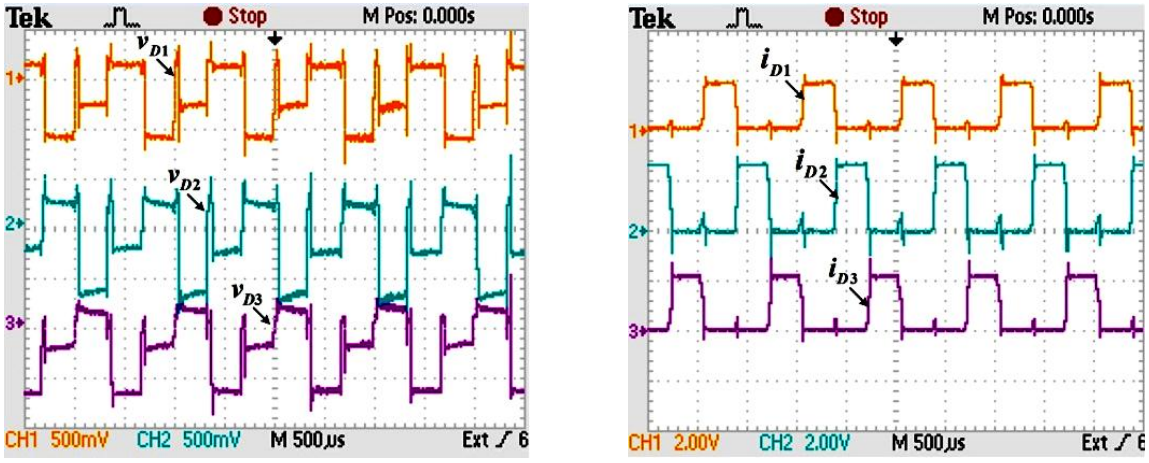
$(v_{L1}, v_{L2} \& v_{L3} : 5V/div, i_{L1}, i_{L2} \& i_{L3} : 3A/div)$

(a) (b)

Fig.5.32 Voltage (v_{L1}, v_{L2}) & currents (i_{L1}, i_{L2}, i_{L3}) waveforms of output filter inductors (a) Simulation (b) Experimental



(a)



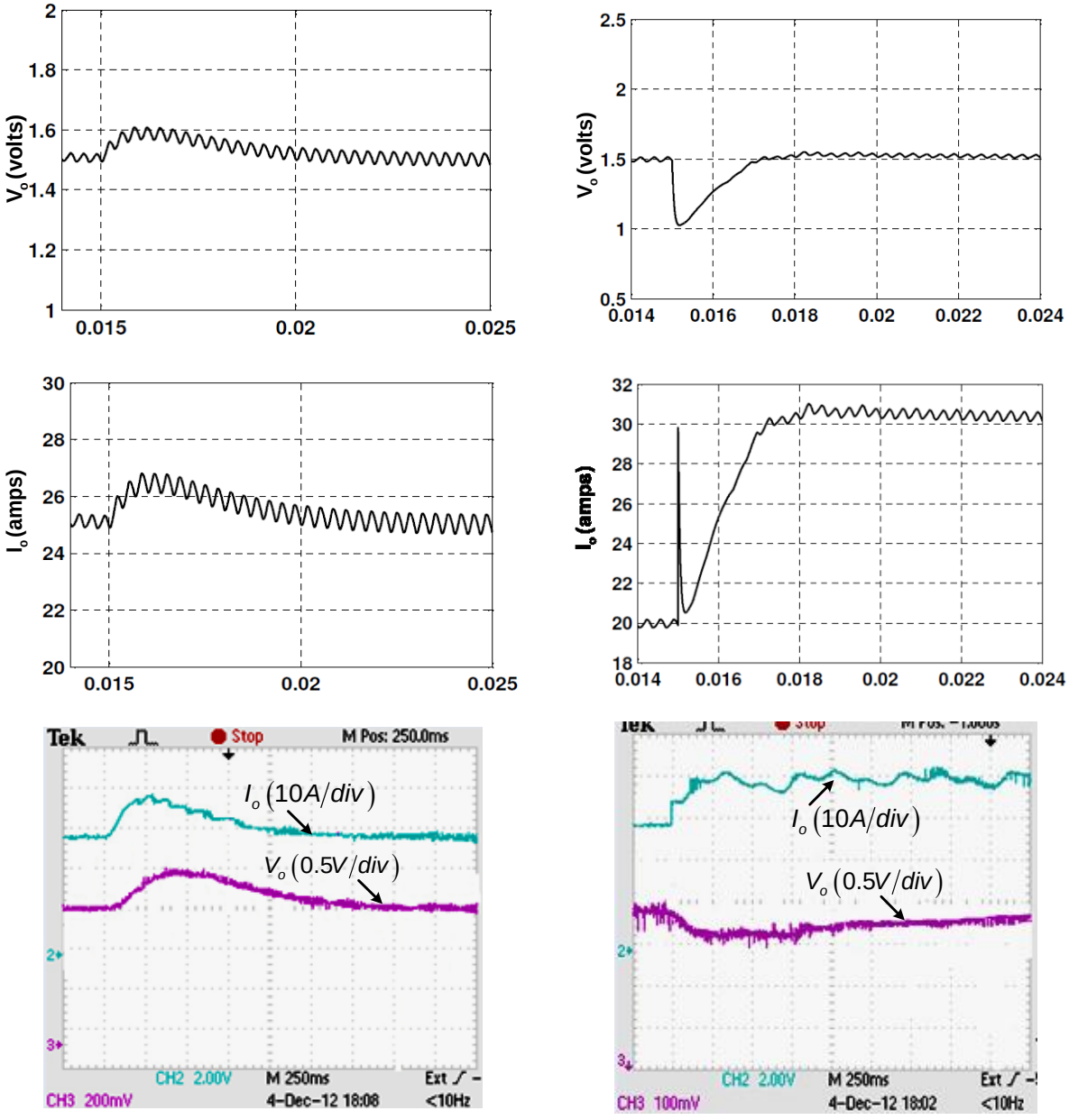
$(v_{D1}, v_{D2} \& v_{D3} : 5V/div, i_{D1}, i_{D2} \& i_{D3} : 25A/div)$

(b)

Fig.5.33 Voltages (v_{D1}, v_{D2}, v_{D3}) and currents (i_{D1}, i_{D2}, i_{D3}) waveforms of rectifier diodes (a) Simulation (b) Experimental

(c) Trasient Performance of Converter

The transient response of proposed converter under both control methods are also studied. Simulation and experimental results are given in Fig.5.34. In simulation results of Fig.5.34(a), the input voltage is increased at $t = 0.015$ sec and corresponding change in output voltage is observed. The similar change in input voltage is incorporated in prototype model and obtained experimental results is depicted in Fig.5.34(a). Thus, it is observed that output voltage variation in both models of proposed converters are similar. Furthermore, output voltage variation against increase in load is also depicted in Fig.5.34(b). It is found that output voltage resumed its reference value after some time delay from the point of disturbance. In all these variations, duty cycle of power switches is adjusted by controller to keep output terminal voltage constant against input voltage and load variations.



(a) (b)

Fig.5.34 Dynamic response of converter under input voltage and load variations

Table 5.3 Comparison of experimental and simulation results of proposed converter with different operating conditions

Parameter		25% of full load		50% of full load		100% of full load	
		Exp.	Simulation	Exp.	Simulation	Exp.	Simulation
Output voltage (volts)		1.5	1.5	1.5	1.5	1.5	1.5
Load current (amp)		12.5	12.5	25	25	50	50
Output Inductor current (amps)	I_{L1}	4.1	4.17	8.21	8.33	16.64	16.71
	I_{L2}	4.0	4.17	8.15	8.33	16.64	16.64
	I_{L3}	3.9	4.17	8.20	8.33	16.63	16.65
Rectifier diode current (amps)	I_{D1}	4.16	4.17	8.20	8.33	16.64	16.65
	I_{D2}	4.15	4.17	8.16	8.33	16.63	16.65
	I_{D3}	4.15	4.17	8.18	8.33	16.64	16.65
Settling time (sec)		-	0.010	-	0.015	-	0.015
% Rise/ Fall in V_o during change in V_{in} from 220V to 180V & vice-versa		-	6.67%	-	6.67%	44.44%	6.67%
Sampling time		30 µsec	1µsec	30 µ sec	1µsec	30 µ sec	1 µsec

5.7 Performance Comparison

In order to evaluate performance of three-phase, high frequency isolated, DC-DC converter with three-phase rectification, the simulation and experimental studies are carried out with symmetrical and asymmetrical PWM control methods. Keeping in view of high power applications at relatively low voltage, the converter has to provide high output current and therefore, achieving high conversion efficiency is challenging task. The conduction interval, number of power devices in conduction and losses in different parts of the converter, mainly depend on type of control methods are to be employed and duty ratio of swicthes. Therefore, comparative evaluation of proposed converter based on mathematical modeling and experimental studies for proposed converter under aforesaid control methods are summarized in Table 5.4. In symmetrical control method, the duty cycle of switches of converter is allowed to vary between $\frac{1}{6}$ to $\frac{1}{2}$ whereas in asymmetrical control method, that of between 0 to $\frac{2}{3}$. Therefore, the range of duty cycle to vary the output voltage is larger in asymmetrical control method as compare to symmetrical control method.

The conduction period of each power switch of front end converter is same i.e. DT in symmetrical control method and that of DT for upper group and $(1-D)T$ for lower group in asymmetrical control. This results in uniform heat distribution in power circuit with symmetrical control method. Therefore, thermal stress in power circuit is more in asymmetrical control methods as compare to symmetrical control method because of unequal conduction of swicthes.

In asymmetrical control method, switches of each leg of front end converter are operated in complementary manner. In order to implement in hardware, a deal band circuit for each device is required to avoid direct short circuiting of input DC voltage. This control method facilitate ease implementation of ZVS/ZCS condition as compare to symmetrical control method.

Table 5.4 Comparative evaluation of isolated three-phase DC-DC converter

Parameter	Symmetrical Control		Asymmetrical Control	
Duty cycle control	$\left(\frac{1}{6} < D < \frac{1}{2}\right)$		$(0 < D < 1)$	
Output voltage control	small		wide	
Thermal stress	less		more	
DC voltage gain $\left(\frac{V_o}{V_{in}}\right)$	$\frac{(6D-1)}{2n}$	$\left(\frac{1}{6} < D < \frac{1}{3}\right)$	$\frac{DV_{dc}}{n}$	$\left(0 < D < \frac{1}{6}\right)$
	$\frac{(6D+1)}{12n}$	$\left(\frac{1}{3} < D < \frac{1}{2}\right)$	$\frac{V_{dc}}{3n}$	$\left(\frac{1}{3} < D < \frac{2}{3}\right)$
Transformer sec. winding current	$\frac{I_o}{6}\sqrt{2D+1}$		$\frac{I_o}{3}\sqrt{2D}$	
Diode voltage stress	$\frac{V_{dc}}{2n}$ $\frac{V_{dc}}{2n}$		$\frac{2V_{dc}}{3n}$	
Diode RMS current	$\frac{I_o}{2}\sqrt{\frac{6D+1}{3}}$		$\frac{I_o}{3}\sqrt{6D+1}$	
Inductor current	$\frac{I_o}{3}$		$\frac{I_o}{3}$	
ZVS /ZCS implementation	difficult		ease	
Devices losses	small		more	

5.8 Conclusion

In view of high power applications at reduced output voltage, a Multi-phase high frequency isolated DC-DC converter with Multi-phase rectification is proposed. As an illustration a three-phase version of DC-DC converter is discussed in detail. This chapter is summarized as follows:

The steady-state operation, modelling and control of three-phase high frequency isolated DC-DC converter under symmetrical and asymmetrical control methods are carried out. Based on mathematical analysis, 5 kW, 5V/1000A Simulink model is developed and its performance is studied with symmetrical and a symmetrical control methods. Due to practical

constraints, reduced rating of 1.5V/ 50A prototype model is developed. As experimental studies are carried out at reduced system parameters, for validating the experimental results, Simulink model with reduced system parameters is developed. The prototype model and reduced Simulink model are tested under various operating conditions and experimental and simulation results are presented for comparative study. The performance of converter during steady-state and transient conditions is found as per design and satisfactory. During input voltage and load variations, output voltage resumes its reference value (1.5V) within 2.5 sec after disturbance. Therefore, it exhibits improved response.

Based on simulation and experimental study, the comparative study of proposed converter under symmetrical and asymmetrical control method is carried out. It is concluded that under symmetrical control method, all the power switches conduct uniformly unlike to asymmetrical control method and hence uniform heat distribution is achieved.

On the other hand, implementation of asymmetrical PWM control method requires dead band circuits for each power switch to avoid short circuiting of input DC voltage, whereas in symmetrical control method, dead band circuits for switches are not neceassry. Furthermore, reduction in secondary side losses can be done by employing self driven synchronous rectifier by replacing rectifier power diodes.

CHAPTER 6: THREE-PHASE HIGH FREQUENCY ISOLATED DC-DC CONVERTER WITH MULTI-PHASE RECTIFICATION

[Industrial applications such as welding, plasma cutting, and surface hardening require high power at reduced DC voltage. In these applications, the rating of power supply varies from few kilowatts to hundreds of kilowatts. The power supply employs in such applications particularly in arc welding process is operated from open-circuit (no-load) to short-circuit (when the electrode sticks to the work-piece for a short span of time) quickly and also the transients occur during the striking of the arc, rapid arc length changes and metal transfer across the arc. The power supply must respond to these changes rapidly. In this chapter, high frequency isolated multi-phase DC-DC converter with multi-phase rectification is proposed which is well suited for aforementioned applications. In comparison with conventional welding machine employed in many industries, the performance of proposed converter is improved significantly in terms of size and weight, efficiency and dynamic response. The simulation and experimental studies of proposed converter are carried output and obtained results under different operating conditions are presented.]

6.1 Introduction

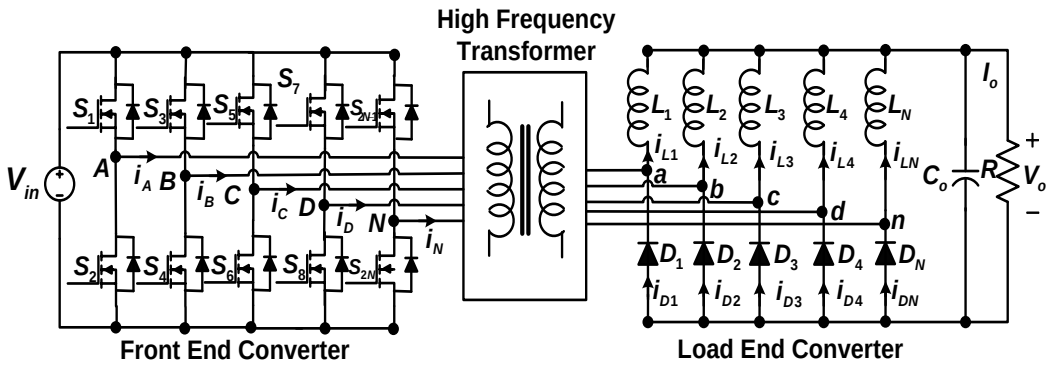
There are many industrial applications such as electroplating, electrolysis, welding, plasma cutting, and surface hardening require high power at reduced DC voltage because of system requirements[11, 88, 89]. In such applications, the rating of power supply varies from few kilowatts to hundreds of kilowatts. Conventionally, the line frequency isolated transformer followed by diode rectifier, thyristor rectifier and diode/chopper hybrid rectifier are employed in many industries [2, 6, 90] in which large output filter inductance is required to limit the rate of the output current rise to prevent the rapid load changes. These machines are too bulky, inefficient and poor dynamic response.

With the advancement in power switching, devices, magnetic core and sophisticated controller, high frequency isolation based power supply is getting popularity in wide variety of applications and catering the need of most of aforesaid applications. Modern welding machines generally utilize single-phase full-bridge DC/DC converter based power supplies, due to high power handling capability and better utilization of the transformer and switches, among all the others DC/DC converters [76, 91]. Although, three-phase converters have been also reported in literature [23, 82, 92, 93]. As demand of power increases, more efforts are being made in research to cater the need of different nature of applications. The following features are desirable in the converter for aforesaid applications:

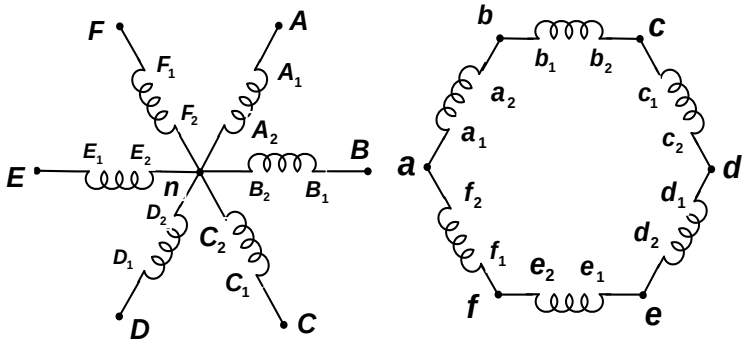
- Capability to deliver high current at reduced DC voltage
- Electrical isolation via transformer for safety issues
- Fast dynamic response

- Better heat managements
- Compact size etc.

In chapter-5, multi-phase high frequency isolated DC-DC converter with multi-phase rectification has been proposed. Keeping in view of low voltage high current applications, particularly for industrial processes, three-phase DC-DC converter may not be efficient because of high current stress on devices of load end converter and design of high current output inductors. Therefore, to cater the need of industrial processes, the six-phase, high frequency isolated DC-DC is studied in which front end converter consists of six legs with each leg comprises of two switches as shown in Fig.6.1. The mid points $(A,B,C,D,E\,\&\,F)$ of each leg in front end converter are connected to one terminal of each primary winding of transformers and other terminals of primary winding of each transformer are connected to point 'n' as shown in Fig.6.1(b). The points $(a,b,c,d,e\,\&\,f)$ of mesh-connected secondary windings of transformers are connected to points $(a,b,c,d,e\,\&\,f)$ of load end converter as shown in Fig.6.1(b). As shown in figure, the front end converter comprises of twelve power switches and its associated PWM signals to generate six phase voltages $(v_{An},v_{Bn},v_{Cn},...v_{Fn})$. Due to large number of switching devices in front end converter and its gate drive circuits, its complexity increases many fold and hence, reliability of system decreases. Furthermore, there are too many high current terminal connections on secondary side.



(a)



(b)

Fig.6.1 Schematic diagram of multi-phase high frequency isolated DC-DC converter (a) Power circuit (b) Winding connections of high frequency transformer

In view of these issues, few modification in high frequency transformer connections is proposed in aforementioned topology which produces six ac voltages $(v_{An}, v_{Bn}, v_{Cn}, ...v_{Fn})$ without addition of switches in three-phase version of front end converter. Furthermore, high current connecting terminals in secondary are also reduced. The six-phase version of multi-phase high frequency isolated DC-DC converter with multi-phase rectification is discussed detail.

6.2 System Configuration and Control Scheme

6.2.1 Power Circuit

As shown in Fig.6.2, the proposed multi-phase high frequency isloated DC-DC converter includes six MOSFETs at front end converter, two units of three-phase high frequency transformers and multi-phase rectifier stage at load end converter. The operation of front end converter is similar to three-phase, isolated DC-DC converter as discussed in chapter-5. The three-phase transformer could be configured in various connections $\Delta/\Delta, \Delta/Y, Y/Y \& Y/\Delta$. Out of these connections, Y/Δ connection offers several advantages:

- Low turns ratio: $1/\sqrt{3}$ time reduction in turns ratio and hence mitigates problems associated with large inductances.
- Lesser primary & secondary winding currents: This reduces kVA rating of transformer, size of primary and secondary winding conductors.

The proposed topology of converter as shown in Fig.6.2, consists of two unit of three-phase high frequency transformer to provide high frequency isolation, voltage scaling and phase shift. one three-phase transformer is connected in *Yd*1 and other transformer is connected in *Yd*11 i.e. primary side of both transformers are connected in wye (*Y*) and secondary windings of both transformers are connected in delta (*d*1) and delta (*d*11) as shown in Fig.6.3(a) and Fig.6.3(b) respectively. Here capital and small case indicate high voltage and low voltage windings. For *Yd*1, *Yd*11 connections, high voltage wye connected winding will lead, lag the low voltage delta connected winding by 30^0 respectively as illustrated in Fig.6.3(c). Thus secondary winding voltages $(v_{a1a2}, v_{b1b2}, v_{c1c2}, v_{d1d2}, v_{e1e2}, v_{f1f2})$ are 60^0 phase shifted as shown in Fig.6.3(c). These ac voltages are further rectified through load end converter which comprises of six legs which are made of six rectifier diodes $(D_1 - D_6)$ and output filter inductors $(L_1 - L_6)$ as shown in Fig.6.2.

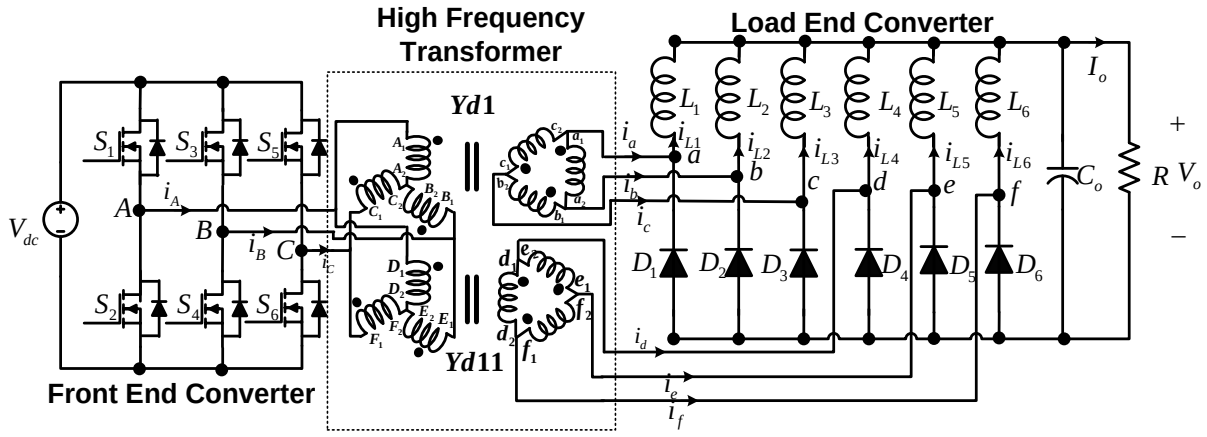


Fig.6.2 Schematic diagram of multi-phase DC-DC converter with reduced components

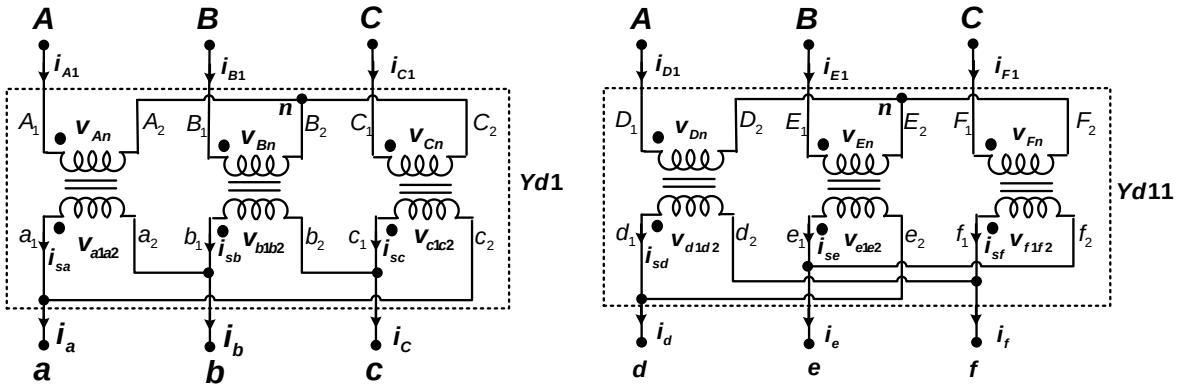


Fig.6.3 Three-phase electrical connections of high frequency transformer (a) *Yd*1 (b) *Yd*11 (c) Vector diagrams

6.2.2 Transformer winding currents and voltages

In order to represent winding currents $(i_{sa}, i_{sb}, i_{sc}, i_{sd}, i_{se}$ & $i_{sf})$ in terms of secondary side line current, $(i_a, i_b, i_c, i_d, i_e$ & $i_f)$, the Kirchhoff's current law is applied at points(a,b,c,d,e,&f) of Fig.6.3(a) and Fig.6.3(b) and yields following current equations

$$i_{sa} - i_{sc} = i_a \tag{6.1.1}$$

$$i_{sb} - i_{sa} = i_b \tag{6.1.2}$$

$$i_{sc} - i_{sb} = i_c \tag{6.1.3}$$

$$i_{sd} - i_{se} = i_d \tag{6.2.1}$$

$$i_{se} - i_{sf} = i_e \tag{6.2.2}$$

$$i_{sf} - i_{sd} = i_f \tag{6.2.3}$$

Solving equation(6.1.1) to equation(6.2.3) with $i_{sa} + i_{sb} + i_{sc} = 0$ and $i_{sd} + i_{sf} + i_{sf} = 0$, we get equation(6.3.1) to equation(6.3.3) and equation(6.4.1) to equation (6.4.3) as follows :

$$i_{sa} = \frac{1}{3}(i_a - i_b) \tag{6.3.1}$$

$$i_{sb} = \frac{1}{3}(i_b - i_c) \tag{6.3.2}$$

$$i_{sc} = \frac{1}{3}(i_c - i_a) \tag{6.3.3}$$

$$i_{sd} = \frac{1}{3}(i_d - i_f) \tag{6.4.1}$$

$$i_{se} = \frac{1}{3}(i_e - i_d) \tag{6.4.2}$$

$$i_{sf} = \frac{1}{3}(i_f - i_e) \tag{6.4.3}$$

If N_1 and N_2 be the number of turns in primary and secondary windings of each transformer. The reflected secondary windings currents in primary side are evaluated as follows:

$$i_{A1} = \frac{N_2}{N_1}\frac{1}{3}(i_a - i_b) \tag{6.5.1}$$

$$i_{B1} = \frac{N_2}{N_1}\frac{1}{3}(i_b - i_c) \tag{6.5.2}$$

$$i_{C1} = \frac{N_2}{N_1}\frac{1}{3}(i_c - i_a) \tag{6.5.3}$$

$$i_{D1} = \frac{N_2}{N_1}\frac{1}{3}(i_d - i_f) \tag{6.6.1}$$

$$i_{E1} = \frac{N_2}{N_1}\frac{1}{3}(i_e - i_d) \tag{6.6.2}$$

$$i_{F1} = \frac{N_2}{N_1}\frac{1}{3}(i_f - i_e) \tag{6.6.3}$$

The primary side currents $(i_A, i_B \,\&\, i_C)$ can be evaluated as

$$i_A = i_{A1} + i_{D1} \tag{6.7.1}$$

$$i_B = i_{B1} + i_{E1} \tag{6.7.2}$$

$$i_C = i_{C1} + i_{F1} \tag{6.7.3}$$

The line voltages of secondary side of high frequency transformer can be evaluated from Fig.6.3(a) and Fig.6.3(b) as follows:

$$V_{ab} = V_{a1a2} \tag{6.8.1}$$

$$V_{bc} = V_{b1b2} \tag{6.8.2}$$

$$V_{ca} = V_{c1c2} \tag{6.8.3}$$

$$V_{de} = V_{d1d2} + V_{f1f2} \tag{6.9.1}$$

$$V_{ef} = V_{e1e2} + V_{d1d2} \tag{6.9.2}$$

$$V_{fd} = V_{f1f2} + V_{e1e2} \tag{6.9.3}$$

6.2.3 Control Strategy

The switches of front end converter are controlled to regulate the output voltage against input voltage and load variations. Thus, the output voltage can be varied by controlling duty ratio of switches. Three saw-tooth waves $(T_{r1}, T_{r2} \,\&\, T_{r3})$ with phase shifted of $\left(T/3\right)$ between each other are required to operate in interleaved manner. These saw-tooth wavefroms are compared with control voltage (v_C) to generate PWM signals for switches of front end converter. The duty ratio of the switches is function of control voltage and thus to control output voltage of converter, the control voltage is to be varied.

Based on the duty ratio, two phase-shifted PWM control techniques namely symmetrical and asymmetrical control are illustrated in Fig.6.4.

In symmetrical control method, six saw-tooth waves $\left(T_{r1}, T_{r2}, T_{r3}, \bar{T}_{r1}, \bar{T}_{r2}, \&\, \bar{T}_{r3}\right)$ are compared with control voltage (v_C). The phase shift of $\left(T/2\right)$ is made between two saw-tooth waves $\left(\bar{T}_{r1}, T_{r1}\right), \left(\bar{T}_{r2}, T_{r2}\right) \& \left(\bar{T}_{r3}, T_{r3}\right)$ to operate converter in symmetrical manner over one switching cycle. As shown in Fig.6.4(a), the PWM signals of switches (S_1, S_2) are

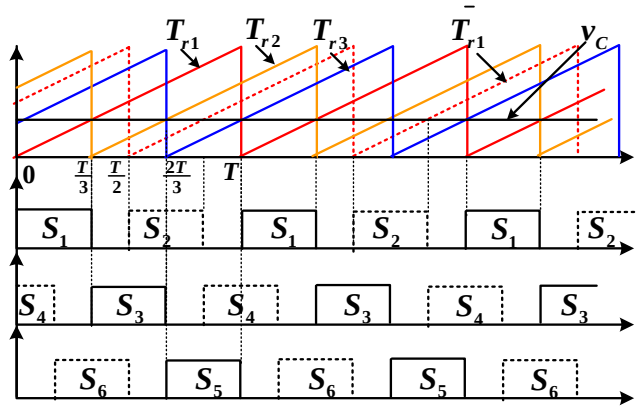
generated by comparing saw-tooth waves $\left(T_{r1},\bar{T}_{r1}\right)$ with control voltage (v_C) and figure indicates that S_1 is ON for duration of duty cycle (DT). At the end of duty cycle, S_1 turned OFF and both switches (S_1,S_2) are OFF for duration $\left(T/2-DT\right)$. In the middle of time period, the switch (S_2) is ON and operates in same manner as previously. For generating PWM signals for S_3,S_4 saw-tooth waves $\left(T_{r2},\bar{T}_{r2}\right)$ and for S_5,S_6 saw-tooth waves $\left(T_{r3},\bar{T}_{r3}\right)$ are compared with control voltage (v_C) and resulting PWM signals are shown in

Fig.6.4(a). As duty ratio varies from 0 to 1, the converter operates in various distinct regions. In symmetrical control method, four regions are identified as Reg1$\left(0<D<\frac{1}{6}\right)$,Reg2 $\left(\frac{1}{6}\le D\le\frac{1}{3}\right)$,Reg3$\left(\frac{1}{3}\le D\le\frac{1}{2}\right)$ and Reg4$\left(\frac{1}{2}\le D\le 1\right)$. The operation of converter in Reg1 and Reg4, are stricted to aviod incomplete current path and direct short circuit of input DC voltage respectively. In regions Reg2, Reg3 output voltage increases from 0 to $\frac{V_{in}}{4n}$ and $\frac{V_{in}}{4n}$ to $\frac{V_{in}}{3n}$ as duty cycle increases from $\frac{1}{6}$ to $\frac{1}{3}$ and $\frac{1}{3}$ to $\frac{1}{2}$ respectively as shown in Fig.6.5(a). Therefore converter operation is restricted in Reg2 and Reg3 only.

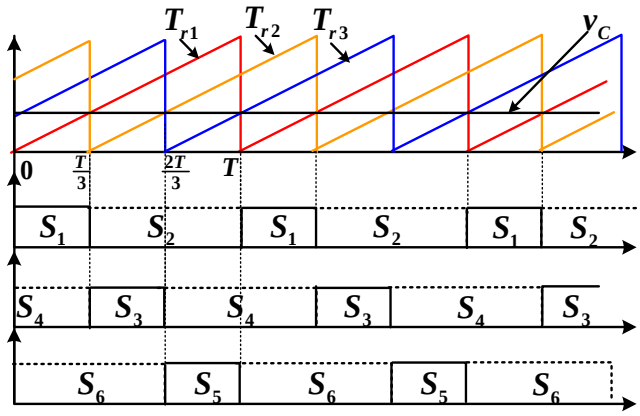
In asymmetrical control method, three saw-tooth waveforms$(T_{r1},T_{r2},\&T_{r3})$ are compared with control voltage(v_C) and the PWM signals for upper group of switches (S_1,S_3,S_5) are generated. As shown in Fig.6.4(b), upper group of switches are ON for the duration of duty cycle (DT) and bottom group of switches are ON for the period of $(1-D)T$. In other words, one and only one switch of each leg is ON at a time. To generate PWM signal for S_1, saw-tooth wave (T_{r1}) is compared with control voltage(v_C) and PWM signal for S_2 is generated by complementing PWM signal of S_1 as shown in

Fig.6.4(b). The PWM signals for switches(S_3,S_5) are generated in similar manner with saw-tooth waves$(T_{r2}\,\&\,T_{r3})$ and PWM signals for switches(S_4,S_6) are obtained through complementing PWM signals of S_3,S_5 as illustrated in Fig.6.4(b). In asymmetrical control method, as duty cycle varies from 0 to 1, three operating regions: Reg1 $\left(0<D<\frac{1}{3}\right)$, Reg2$\left(\frac{1}{3}<D<\frac{2}{3}\right)$, Reg3$\left(\frac{2}{3}<D<1\right)$ are identified in Fig.6.5(b). In region (Reg1), output voltage increase linearly from 0 to $\frac{V_{in}}{3n}$, as duty cycle increases varies from 0 to $\frac{1}{3}$. In region (Reg2), converter provides constant voltage in spite of change in duty cycle. In region (Reg3), output voltage decrease to 0 as duty cycle increases from $\frac{2}{3}$ to 1. Thus, operation of

converter in Reg1 and Reg3 are same, whereas in Reg3 output volatge decreases with increase in duty ratio , which makes control design is different than Reg1. Therefore, duty cycle of converter is restricted to less than 0.5 and hence allow operation in Reg1 and Reg2 only.



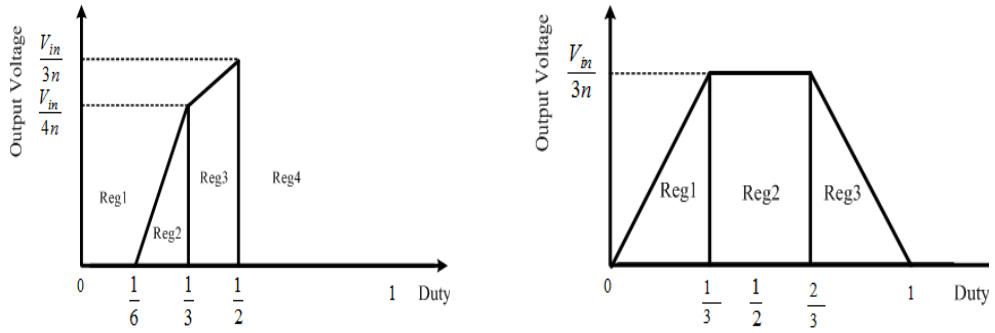
(a)



(b)

Fig.6.4 Switching signals in phase-shifted PWM control

(a) Symmetrical control (b) Asymmetrical Control



(a) (b)

Fig.6.5 Output voltage versus duty ratio (a) Symmetrical Control (b) Asymmetrical Control

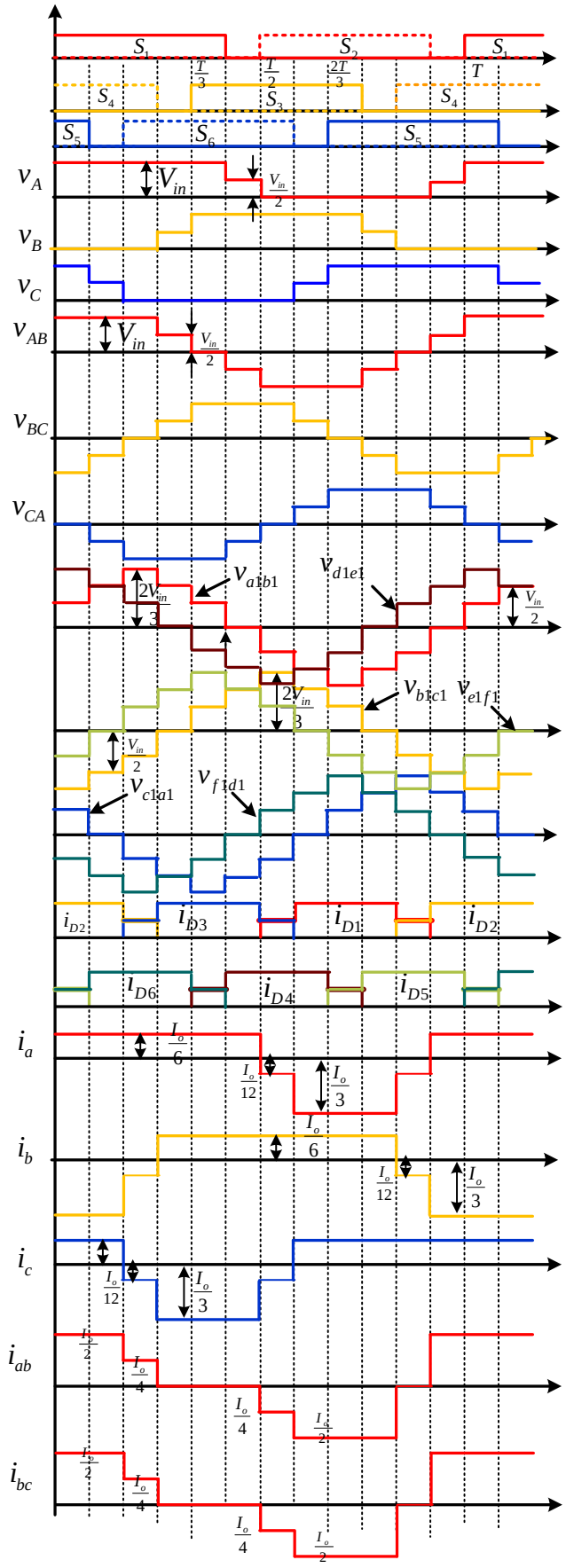


Fig. 6.6 Steady- state voltage and current waveforms of multi-phase high frequency isolated DC-DC converter

6.3 Operation, Modeling and Analysis of the Converter

In order to simplify the steady state analysis of proposed converter, the following assumptions are made:

- Power switching devices and passive components are lossless.
- The input and output voltages are constant and ripple-free.
- The output inductors are large enough to ensure continuous current mode of operation, and then currents are constant and ripple-free.
- Effects of snubber circuit are neglected.

The switches of each leg of front end converter are symmetrically/ asymmetrically controlled and each leg is operated with 120^0 phase shift for interleaved operation as shown in Fig.6.4. Based on state of power switches various operating modes are identified as tabulated in Table-6.1. The steady state operation of converter with symmetrical control in region Reg3 and with asymmetrical control in region Reg1 are discussed in the following sections:

6.3.1 Operation of Converter under Symmetrical Control Method

The operation of proposed converter in region (Reg3) under symmetrical control method consists of twelve operating modes. The switches of front end converter are conducting during mode-1 to mode-6 and are complementary with mode-7 to mode-12 respectively. Therefore, operations of converter during mode-1 to mode-6 are discussed and its mode-wise equivalent circuit are shown in Fig. 6.7 to Fig. 6.9. The operation of converter is explained below:

(a) Mode-1: In this mode power switches S_1, S_4 and S_5 are conducting and remaining switches are OFF. The current paths in primary and secondary side of circuit are shown by bold line in Fig. 6.7(a). The voltage across primary and secondary windings of transformer are as follows:

$$v_{AB} = V_{in},\ v_{BC} = -V_{in}, v_{CA} = 0, v_{An} = v_{Dn} = \tfrac{V_{in}}{3}, v_{Bn} = v_{En} = -\tfrac{2V_{in}}{3}, v_{Cn} = v_{Fn} = \tfrac{V_{in}}{3}$$

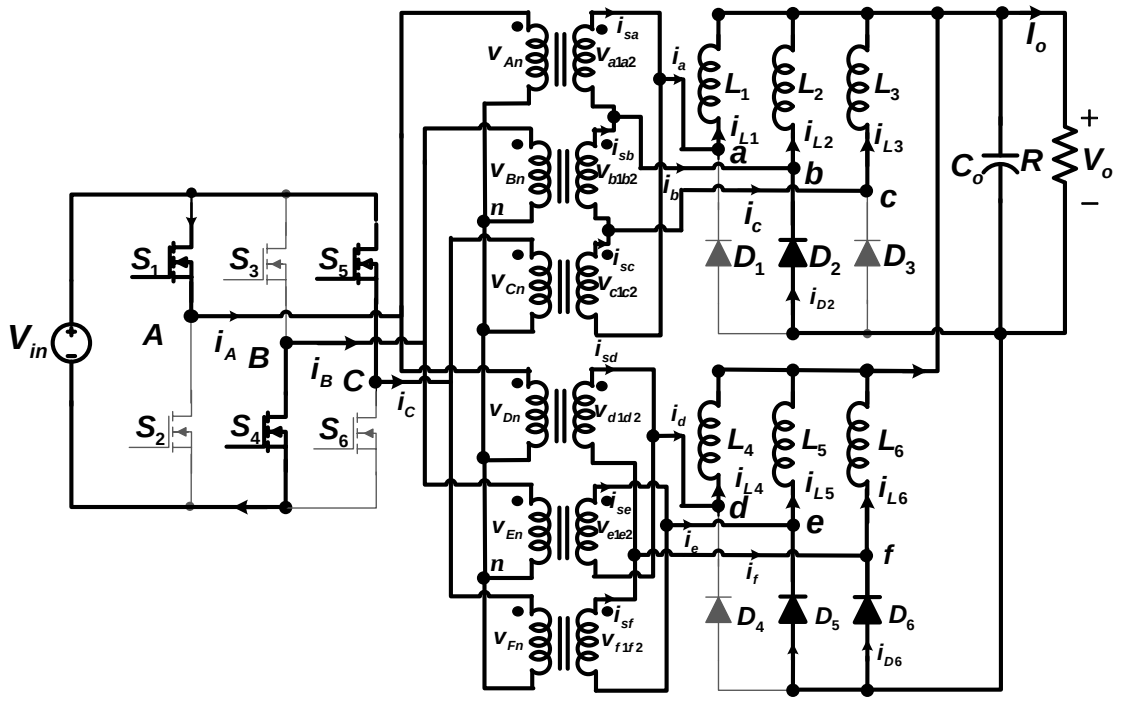
$$V_{a1b1} = \tfrac{V_{in}}{3}\tfrac{N_2}{N_1}, V_{b1c1} = -\tfrac{2V_{in}}{3}\tfrac{N_2}{N_1}, V_{c1a1} = \tfrac{V_{in}}{3}\tfrac{N_2}{N_1}, V_{d1e1} = \tfrac{2V_{in}}{3}\tfrac{N_2}{N_1}, V_{e1f1} = -\tfrac{V_{in}}{3}\tfrac{N_2}{N_1}, V_{f1d1} = \tfrac{V_{in}}{3}\tfrac{N_2}{N_1}$$

The secondary voltages of transformer forward biases the rectifier diodes (D_2, D_5, D_6) and feed energy to load through output inductors $(L_1 - L_6)$. The current thought different parts of circuit are as follows:

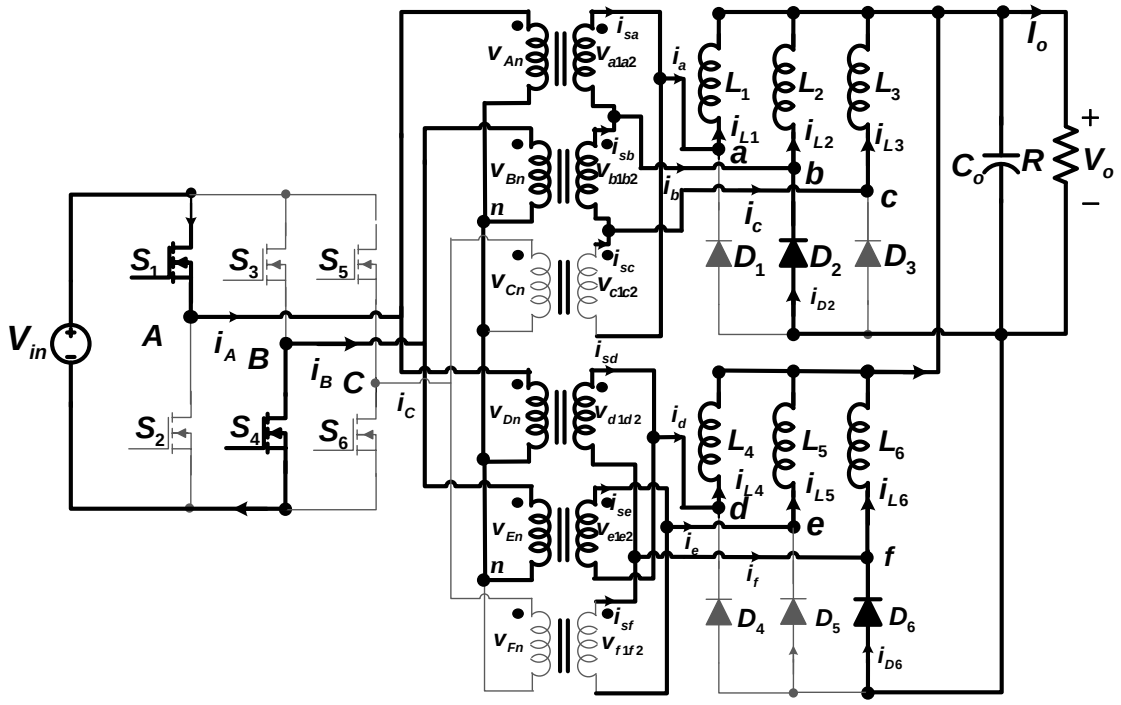
$$i_A = \tfrac{\frac{V_{in}}{3} - V_o'}{L_1'} \approx \tfrac{I_o}{3}\tfrac{N_2}{N_1}, i_B = -\tfrac{I_o}{3}\tfrac{N_2}{N_1}, i_C = \tfrac{I_o}{3}\tfrac{N_2}{N_1}, i_{D2} = \tfrac{I_o}{2}, i_{D5} = \tfrac{I_o}{4}, i_{D6} = \tfrac{I_o}{4}, i_{D1} = i_{D3} = i_{D4} = 0,$$

$$i_{L1} = i_{L2} = i_{L3} = \tfrac{I_o}{6}, i_{L4} = i_{L5} = i_{L6} = \tfrac{I_o}{6}, i_a = i_c = i_d = \tfrac{I_o}{6}, i_b = -\tfrac{I_o}{3}, i_e = i_f = -\tfrac{I_o}{12}$$

The mode-1 ends with time instant when power switch S_5 turns OFF.



(a) mode-1



(b) mode-2

Fig. 6.7 Equivalent circuit of converter under (a) mode-1 and (b) mode-2

(b) Mode-2

During this mode switches S_1 and S_4 are conducting and remaining other power switches are OFF. Referring to Fig. 6.7(b) the voltages and currents in different parts of circuit can be obtained as below:

$$v_{AB} = V_{in},\ v_{BC} = -\frac{V_{in}}{2}, v_{CA} = -\frac{V_{in}}{2}, v_{An} = v_{Dn} = \frac{V_{in}}{2}, v_{Bn} = v_{En} = -\frac{V_{in}}{2}, v_{Cn} = v_{Fn} = 0;$$

$$v_{a1b1} = v_{d1e1} = \frac{V_{in}}{2}\frac{N_2}{N_1}, v_{b1c1} = -\frac{V_{in}}{2}\frac{N_2}{N_1}, v_{c1a1} = 0, v_{d1e1} = \frac{2V_{in}}{3}\frac{N_2}{N_1}, v_{e1f1} = 0, v_{f1d1} = -\frac{V_{in}}{2}\frac{N_2}{N_1};$$

$$i_A = \frac{\frac{2V_{in}}{3} - V_o'}{L_1'} \approx \frac{I_o}{3}\frac{N_2}{N_1}, i_B = -\frac{I_o}{3}\frac{N_2}{N_1}, i_C = -\frac{I_o}{3}\frac{N_2}{N_1}, i_{D2} = \frac{I_o}{2}, i_{D5} = 0, i_{D6} = \frac{I_o}{2}, i_{D1} = i_{D3} = i_{D4} = 0,$$

$$i_{L1} = i_{L2} = i_{L3} = \frac{I_o}{6}, i_{L4} = i_{L5} = i_{L6} = \frac{I_o}{6}, i_a = i_c = i_d = i_e = \frac{I_o}{6}, i_b = i_f = -\frac{I_o}{3}$$

Induced secondary voltages of transformers forward biases the rectifier diodes(D_2 & D_6) with result output filter inductors (L_1,L_3, L_4 & L_5) feed energy to load. At the same time currents of output filter inductors (L_2 & L_6) freewheel through rectifier diodes (D_2 & D_6) as shown in Fig. 6.7(b).

(c) Mode-3

In this mode switches S_1,S_6 &S_4 are conducting and remaining power switches are OFF. Referring to Fig. 6.8(a) the voltages and currents in different parts of circuit can be obtained as below:

$$v_{AB} = V_{in},\ v_{BC} = 0, v_{CA} = -V_{in}, v_{An} = v_{Dn} = \frac{2V_{in}}{3}, v_{Bn} = v_{En} = -\frac{V_{in}}{3}, v_{Cn} = v_{Fn} = -\frac{V_{in}}{3};$$

$$v_{a1b1} = \frac{2V_{in}}{3}\frac{N_2}{N_1}, v_{d1e1} = \frac{V_{in}}{3}\frac{N_2}{N_1}, v_{b1c1} = -\frac{V_{in}}{3}\frac{N_2}{N_1}, v_{c1a1} = 0, v_{e1f1} = \frac{V_{in}}{3}\frac{N_2}{N_1}, v_{f1d1} = -\frac{V_{in}}{2}\frac{N_2}{N_1};$$

$$i_A = \frac{\frac{2V_{in}}{3} - V_o'}{L_1'} \approx \frac{I_o}{3}\frac{N_2}{N_1}, i_B = -\frac{I_o}{3}\frac{N_2}{N_1}, i_C = -\frac{I_o}{3}\frac{N_2}{N_1}, i_{D2} = i_{D3} = \frac{I_o}{4}, i_{D5} = 0, i_{D6} = \frac{I_o}{2},$$

$$i_{D1} = i_{D3} = i_{D4} = 0, i_{L1} = i_{L2} = i_{L3} = \frac{I_o}{6}, i_{L4} = i_{L5} = i_{L6} = \frac{I_o}{6}, i_b = i_c = -\frac{I_o}{12}, i_f = -\frac{I_o}{3}$$

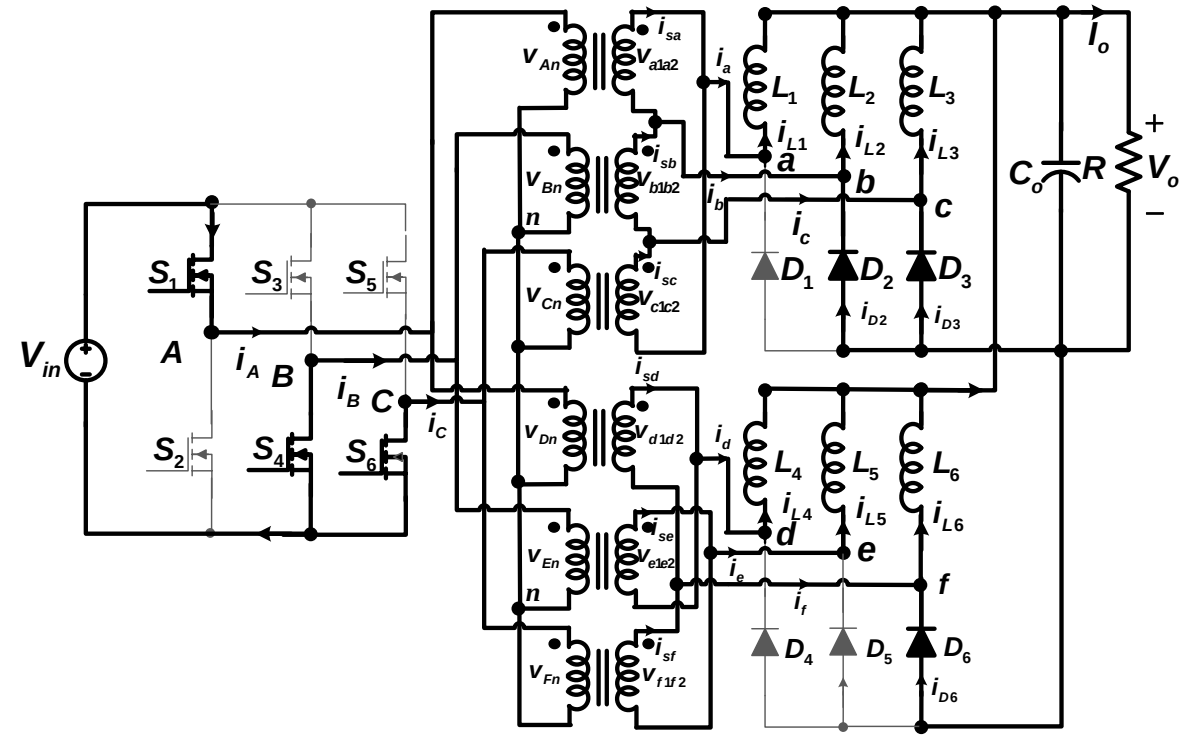
Induced secondary voltages of transformers forward biases the rectifier diodes (D_2, D_3 & D_6) with the results output filter inductors (L_1, L_4 & L_5) feed energy to load through their respective secondary windings. The currents of output filter inductors (L_2, L_3 & L_6) freewheel through rectifier diodes (D_2, D_3 & D_6) as shown in Fig. 6.8(a).

(d) Mode-4

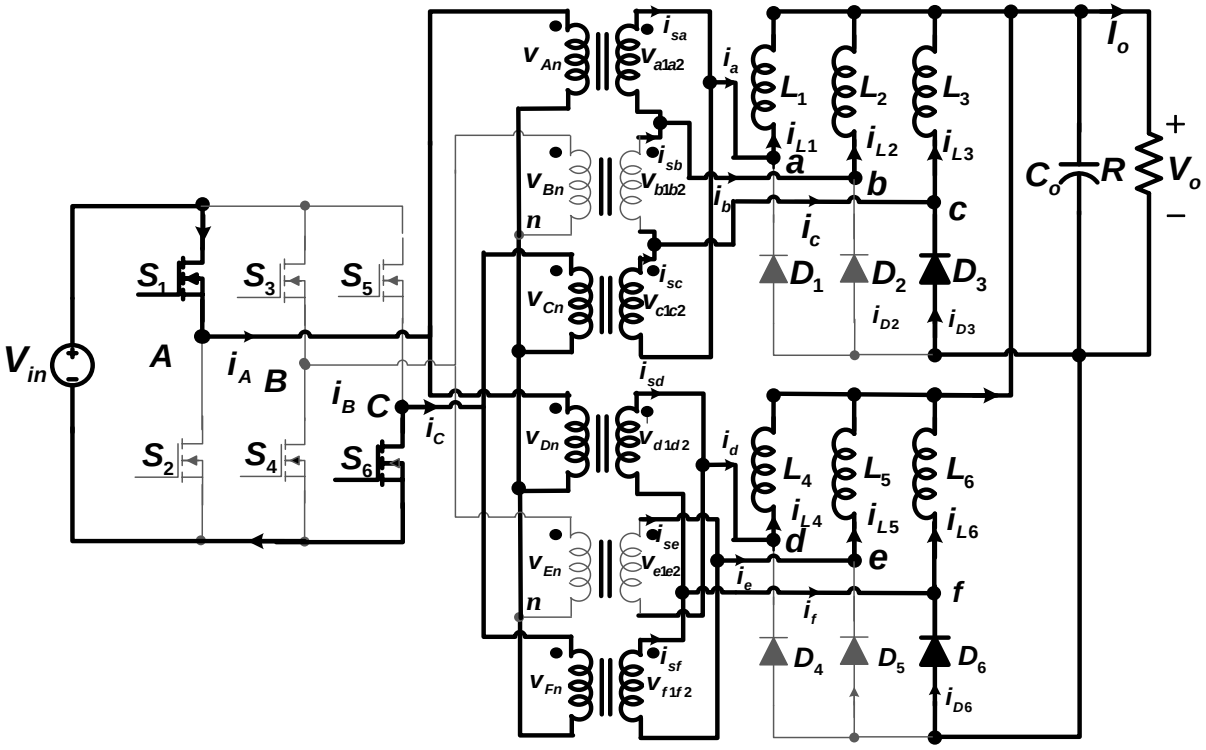
In this mode, switches S_1 and S_6 are conducting and other switches are OFF as shown in Fig. 6.8(b). The voltage and current in different parts of circuits can be obtained as below:

$$V_{AB} = \frac{V_{in}}{2},\ v_{BC} = \frac{V_{in}}{2}, v_{CA} = -V_{in}, v_{An} = v_{Dn} = \frac{V_{in}}{2}, v_{Cn} = v_{Fn} = -\frac{V_{in}}{2}, v_{Bn} = v_{En} = 0;$$

$$v_{a1b1} = \frac{V_{in}}{2}\frac{N_2}{N_1}, v_{d1e1} = 0, v_{b1c1} = 0, v_{c1a1} = v_{f1d1} = -\frac{V_{in}}{2}\frac{N_2}{N_1}, v_{e1f1} = \frac{V_{in}}{2}\frac{N_2}{N_1},$$



(a) mode-3



(b) mode-4

Fig. 6.8 Equivalent circuit of converter under (a) mode-3 (b) mode-4

$$i_A = \frac{\frac{2V_{in}}{3} - V_o'}{L_1'} \approx \frac{I_o}{3}\frac{N_2}{N_1}, i_B = -\frac{I_o}{3}\frac{N_2}{N_1}, i_C = -\frac{I_o}{3}\frac{N_2}{N_1}, i_{D3} = \frac{I_o}{2}, i_{D5} = 0, i_{D6} = \frac{I_o}{2}, i_{D1} = i_{D2} = i_{D4} = 0,$$

$$i_{L1} = i_{L2} = i_{L3} = \frac{I_o}{6}, i_{L4} = i_{L5} = i_{L6} = \frac{I_o}{6}, i_b = i_c = -\frac{I_o}{12}, i_f = -\frac{I_o}{3}$$

It is observed that rectifier diodes (D_3 & D_6) are forward biased and hence the current freewheels through output filter inductors (L_3 & L_6).

(e) Mode-5

In mode-5 switches (S_1,S_3 and S_6) are in conduction state and remaining switches are in OFF state. Switch S_3 starts conducting at $t = \frac{T}{3}$. The voltage $\left(\frac{V_{in}}{3}\right)$ appears across primary windings (A_1A_2, B_1B_2, D_1D_2 & E_1E_2) and voltage $\left(-\frac{2V_{in}}{3}\right)$ appears at primary windings (C_1C_2 & F_1F_2) of transformers. Theses voltages induce voltage in secondary windings which force rectifier diodes (D_3, D_4 & D_6) to conduct. Voltage and current in different parts of circuit can be evaluated from Fig. 6.9(a) as below:

$$V_{AB} = 0,\ V_{BC} = V_{in}, V_{CA} = -V_{in}, v_{An} = v_{Dn} = \frac{V_{in}}{3}, v_{Cn} = v_{Fn} = -\frac{2V_{in}}{3}, v_{Bn} = v_{En} = \frac{V_{in}}{3};$$

$$V_{a1b1} = \frac{V_{in}}{3}\frac{N_2}{N_1}, V_{d1e1} = -\frac{V_{in}}{3}\frac{N_2}{N_1}, V_{b1c1} = \frac{V_{in}}{3}\frac{N_2}{N_1}, V_{c1a1} = -\frac{2V_{in}}{3}\frac{N_2}{N_1}, V_{f1d1} = -\frac{V_{in}}{3}\frac{N_2}{N_1}, V_{e1f1} = \frac{2V_{in}}{3}\frac{N_2}{N_1},$$

$$i_A = \frac{\frac{2V_{in}}{3} - V_o'}{L_1'} \approx \frac{I_o}{3}\frac{N_2}{N_1}, i_B = -\frac{I_o}{3}\frac{N_2}{N_1}, i_C = -\frac{I_o}{3}\frac{N_2}{N_1}, i_{D3} = \frac{I_o}{2}, i_{D4} = \frac{I_o}{4}, i_{D6} = \frac{I_o}{4}, i_{D1} = i_{D2} = i_{D5} = 0,$$

$$i_{L1} = i_{L2} = i_{L3} = \frac{I_o}{6}, i_{L4} = i_{L5} = i_{L6} = \frac{I_o}{6}, i_a = \frac{I_o}{6},\ i_b = \frac{I_o}{6}, i_c = -\frac{I_o}{3}, i_e = -\frac{I_o}{3}, i_d = i_f - \frac{I_o}{12}$$

(f) Mode-6

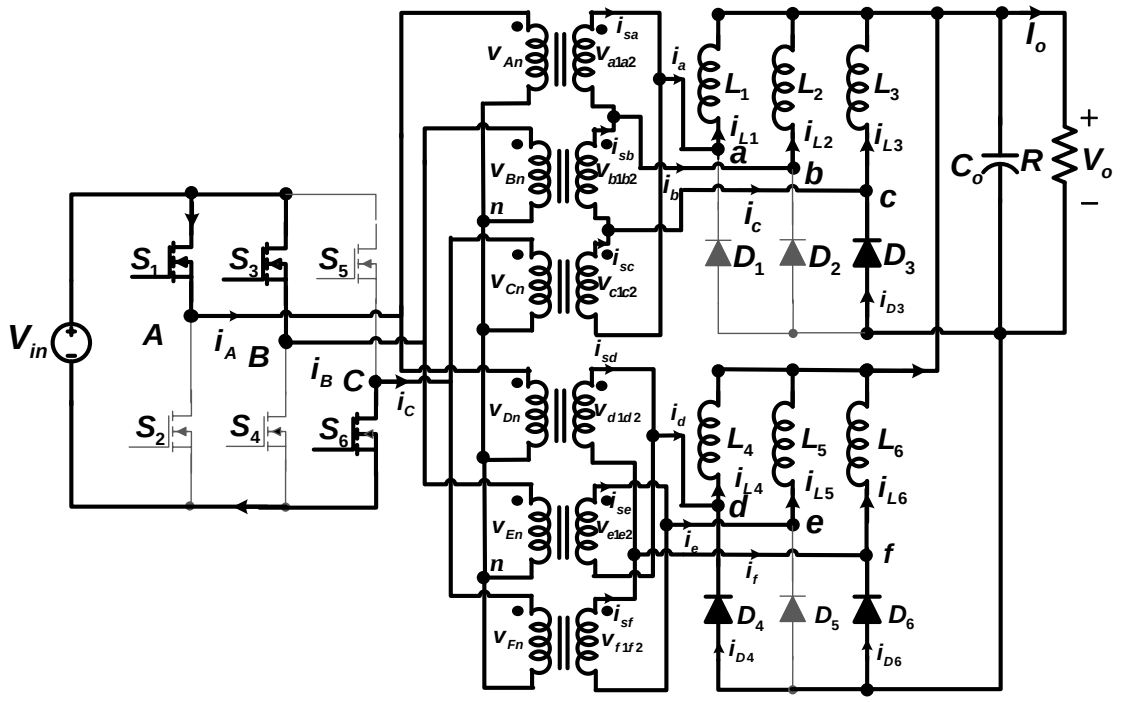
In mode-6 switches (S_3 and S_6) are in conduction state and remaining switches are in OFF state. The voltage $\left(\frac{V_{in}}{2}\right)$ appears across primary windings (B_1B_2 & E_1E_2) and voltage $\left(-\frac{V_{in}}{2}\right)$ appears at primary windings (C_1C_2 & F_1F_2) of transformers. Theses voltages induce voltage in secondary windings which force rectifier diodes (D_3& D_4) to conduct. Voltage and current in different parts of circuit can be evaluated from Fig. 6.9(b) as below:

$$V_{AB} = -\frac{V_{in}}{2},\ V_{BC} = V_{in}, V_{CA} = -\frac{V_{in}}{2}, v_{An} = v_{Dn} = 0, v_{Cn} = v_{Fn} = -\frac{V_{in}}{2}, v_{Bn} = v_{En} = \frac{V_{in}}{2};$$

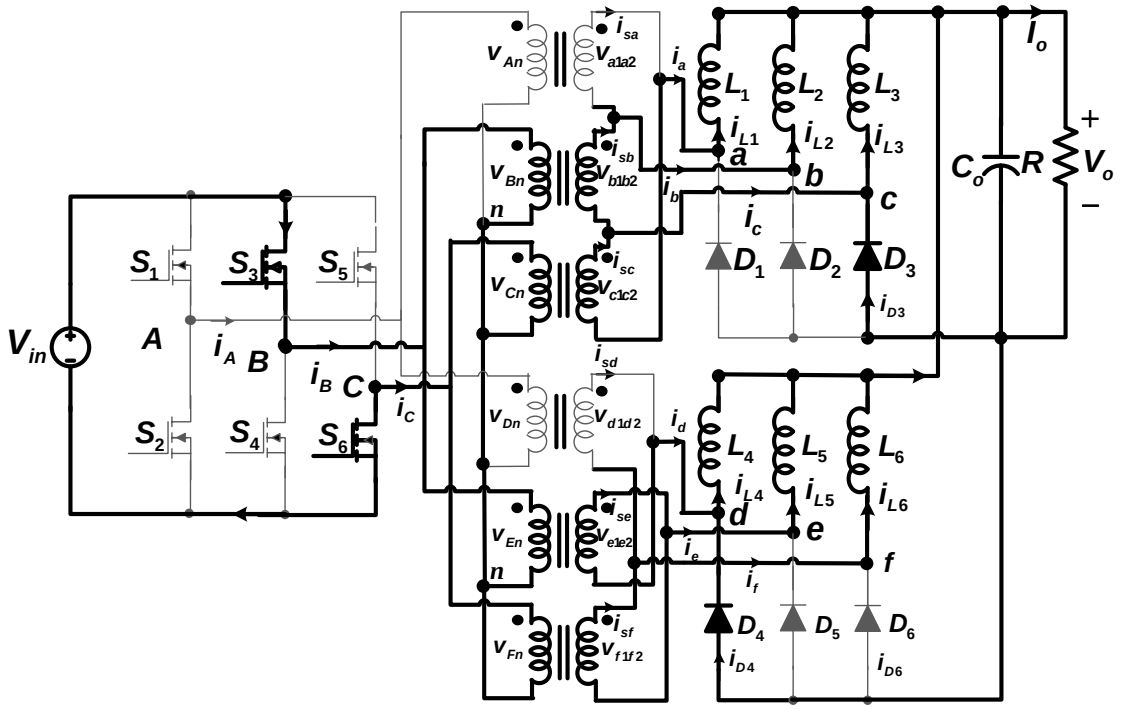
$$V_{a1b1} = 0, V_{d1e1} = -\frac{V_{in}}{2}\frac{N_2}{N_1}, V_{b1c1} = \frac{V_{in}}{2}\frac{N_2}{N_1}, V_{c1a1} = -\frac{V_{in}}{2}\frac{N_2}{N_1}, V_{f1d1} = 0, V_{e1f1} = \frac{V_{in}}{2}\frac{N_2}{N_1},$$

$$i_A = \frac{\frac{2V_{in}}{3} - V_o'}{L_1'} \approx \frac{I_o}{3}\frac{N_2}{N_1}, i_B = -\frac{I_o}{3}\frac{N_2}{N_1}, i_C = -\frac{I_o}{3}\frac{N_2}{N_1}, i_{D3} = \frac{I_o}{2}, i_{D4} = \frac{I_o}{2}, i_{D6} = 0, i_{D1} = i_{D2} = i_{D5} = 0,$$

$$i_{L1} = i_{L2} = i_{L3} = \frac{I_o}{6}, i_{L4} = i_{L5} = i_{L6} = \frac{I_o}{6}, i_a = \frac{I_o}{6},\ i_b = \frac{I_o}{6}, i_c = -\frac{I_o}{3}, i_e = -\frac{I_o}{3}, i_d = i_f = \frac{I_o}{6}$$



(a)



(b)

Fig. 6.9 Equivalent circuit of converter under (a) mode-5 (b) mode-6

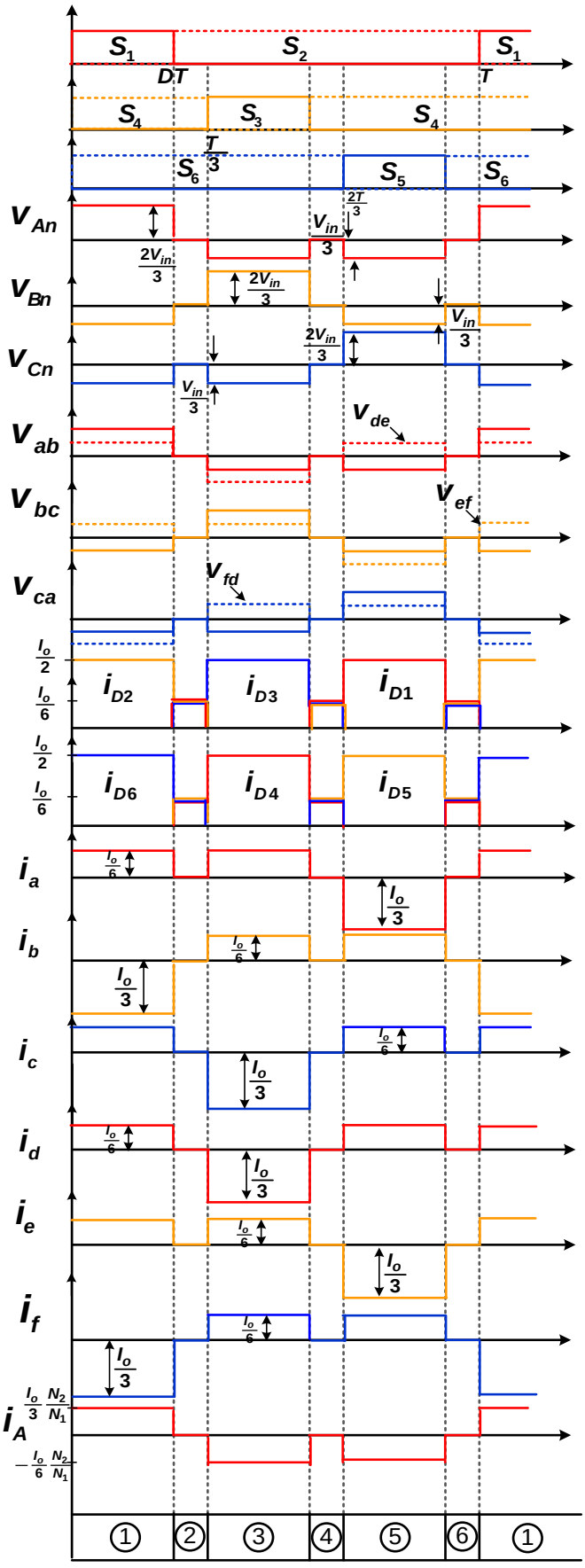


Fig. 6.10 Voltage & current waveforms of proposed converter under asymmetrical control method

6.3.2 Operation of Converter under Asymmetrical Control Method

As duty ratio of switches varies, the proposed converter operates in both regions (Reg1, Reg2) under asymmetrical control method. The operation in the region (Reg2) under asymmetrical control is similar to operation of converter in the region (Reg3) under symmetrical control. Therefore, the operation of the converter only in the region (Reg1) is explained. The six operating modes are identified based on ON and OFF state of switches and steady state waveform of voltage and current of the circuit is illustrated in Fig. 6.10. The equivalent circuit of converter in each operating mode with bold solid line indicating current paths is illustrated in Fig. 6.11.

(a) Mode-1$\left(0 < t < DT\right)$: In this mode, power switches $\left(S_1, S_4, S_6\right)$ are ON and remaining switches are OFF and equivalent circuit during this mode is shown in Fig. 6.11(a). The voltages and currents in different parts of circuit can be obtained as given below:

$$v_{An} = v_{Dn} = \frac{2V_{in}}{3}, v_{Bn} = v_{En} = v_{Cn} = v_{Fn} = -\frac{V_{in}}{3},\ v_{a1b1} = \frac{2V_{in}}{3}\frac{N_2}{N_1},\ v_{d1e1} = \frac{V_{in}}{3}\frac{N_2}{N_1}$$

$$v_{b1c1} = v_{c1a1} = -\frac{V_{in}}{3}\frac{N_2}{N_1}, v_{e1f1} = -\frac{V_{in}}{3}\frac{N_2}{N_1}, v_{f1d1} = \frac{2V_{in}}{3}\frac{N_2}{N_1}, i_A = \frac{I_o}{3}\frac{N_2}{N_1}, i_{D2} = i_{D6} = \frac{I_o}{2},$$

$$i_{D1} = i_{D3} = i_{D4} = i_{D5} = 0,\ i_b = i_f = -\frac{I_o}{3}, i_a = i_c = i_d = i_e = \frac{I_o}{6},$$

$$i_{L1} = i_{L2} = i_{L3} = i_{L4} = i_{L5} = i_{L6} = \frac{I_o}{6}$$

The mode-1 ends with turning OFF of power switch S_1.

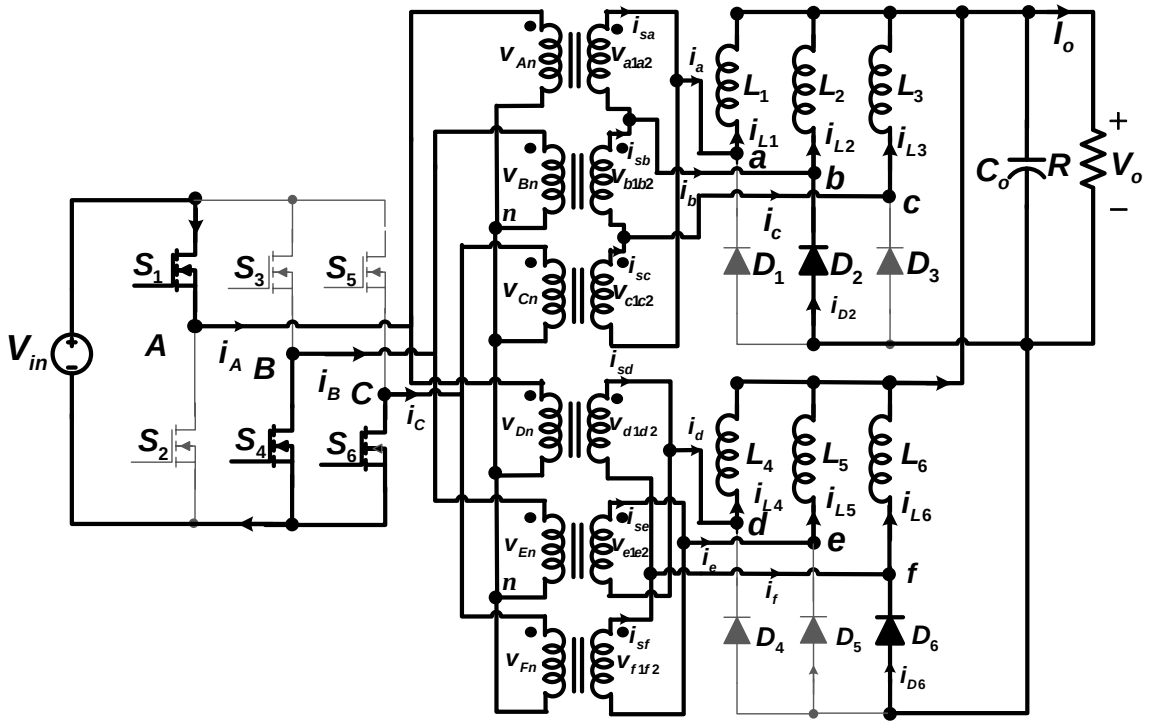
(b) Mode-2$\left(DT < t < \frac{T}{3}\right)$: At $t = DT$ power switch $\left(S_2\right)$ turns ON and it starts conducting along with previous conducting switches $\left(S_4, S_6\right)$. The equivalent circuit during this mode is shown in Fig. 6.12(b). The inductor currents freewheel through rectifier diodes. The voltage and current in different parts of circuits are given below:

$$v_{An} = 0, v_{Bn} = 0, v_{Cn} = 0, v_{a1a2} = 0, v_{b1b2} = 0, v_{c1c2} = 0, i_{D1} = i_{D2} = i_{D3} = \frac{I_o}{6},$$

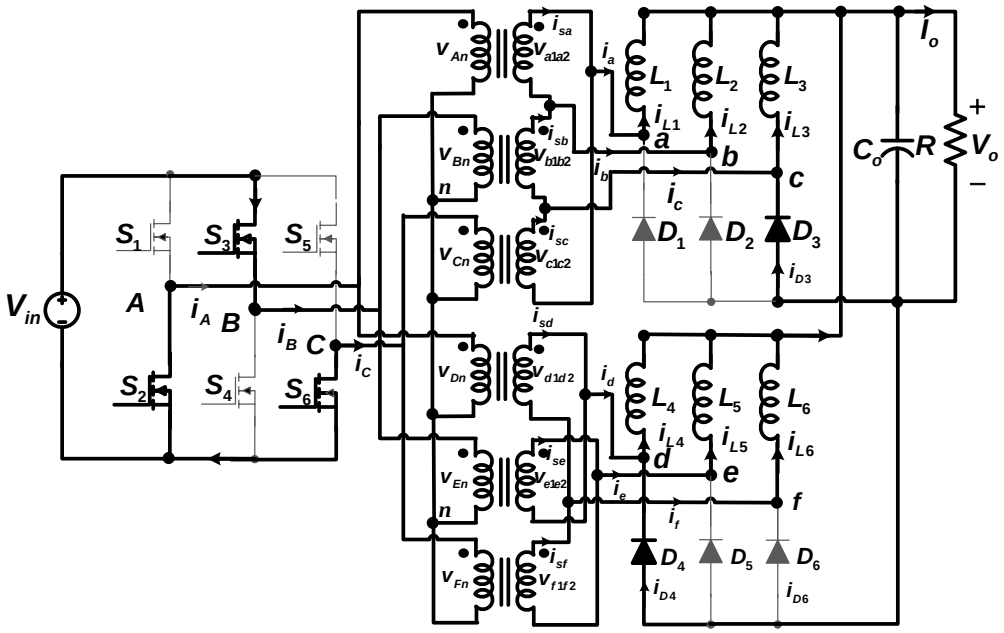
The operation of converter in mode-4$\left(\frac{T}{3} + DT < t < \frac{2T}{3}\right)$ and mode-6$\left(\frac{2T}{3} + DT < t < T\right)$ are similar to mode-2.

(c) Mode-3 $\left(\frac{T}{3} < t < \frac{T}{3} + DT\right)$: In this mode power switches $\left(S_2, S_3, S_6\right)$ are ON and remaining switches are OFF as shown in Fig. 6.11(b). The voltages $v_{An} = v_{Cn} = v_{Dn} = v_{Fn} = -\frac{V_{in}}{3}$, $V_{Bn} = V_{En} = \frac{2V_{in}}{3}$, appear at primary winding of each transformer. The rectifier diodes D_3, D_4 are conducting and carriy half of total load current. The remaining rectifier diodes are OFF.

$$v_{a1b1} = -\frac{V_{in}}{3}\frac{N_2}{N_1},\ v_{d1e1} = -\frac{2V_{in}}{3}\frac{N_2}{N_1}, v_{b1c1} = \frac{2V_{in}}{3}\frac{N_2}{N_1},\ v_{e1f1} = \frac{V_{in}}{3}\frac{N_2}{N_1}, v_{c1a1} = -\frac{V_{in}}{3}\frac{N_2}{N_1},\ v_{f1d1} = \frac{V_{in}}{3}\frac{N_2}{N_1}$$

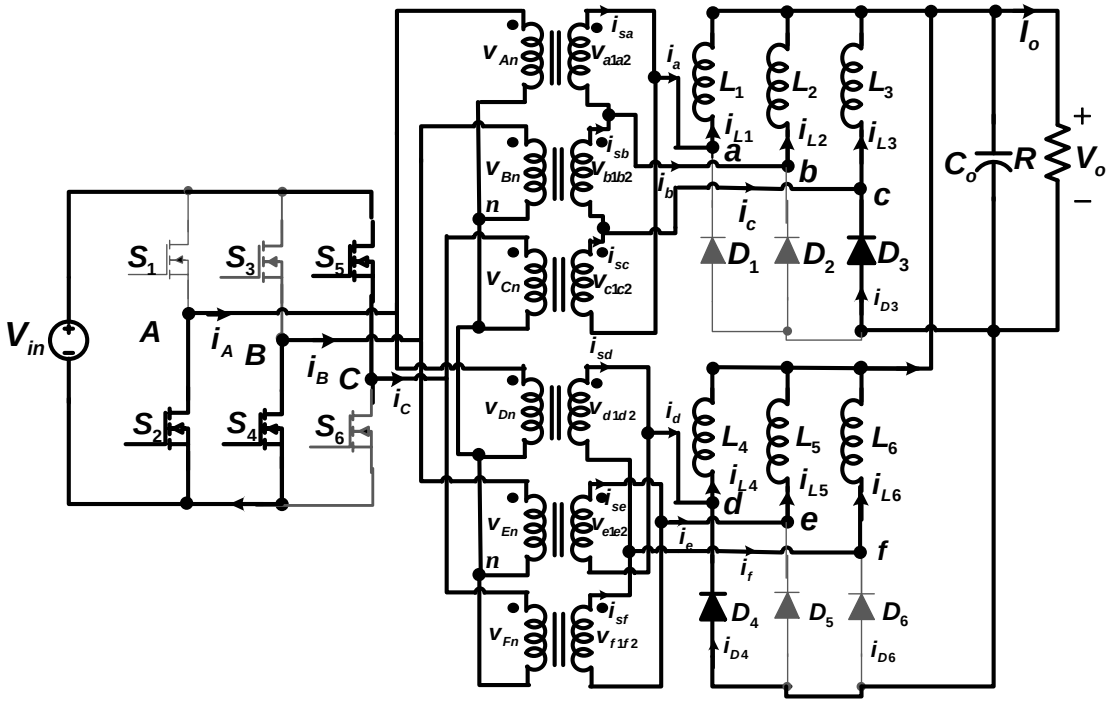


(a) mode-1

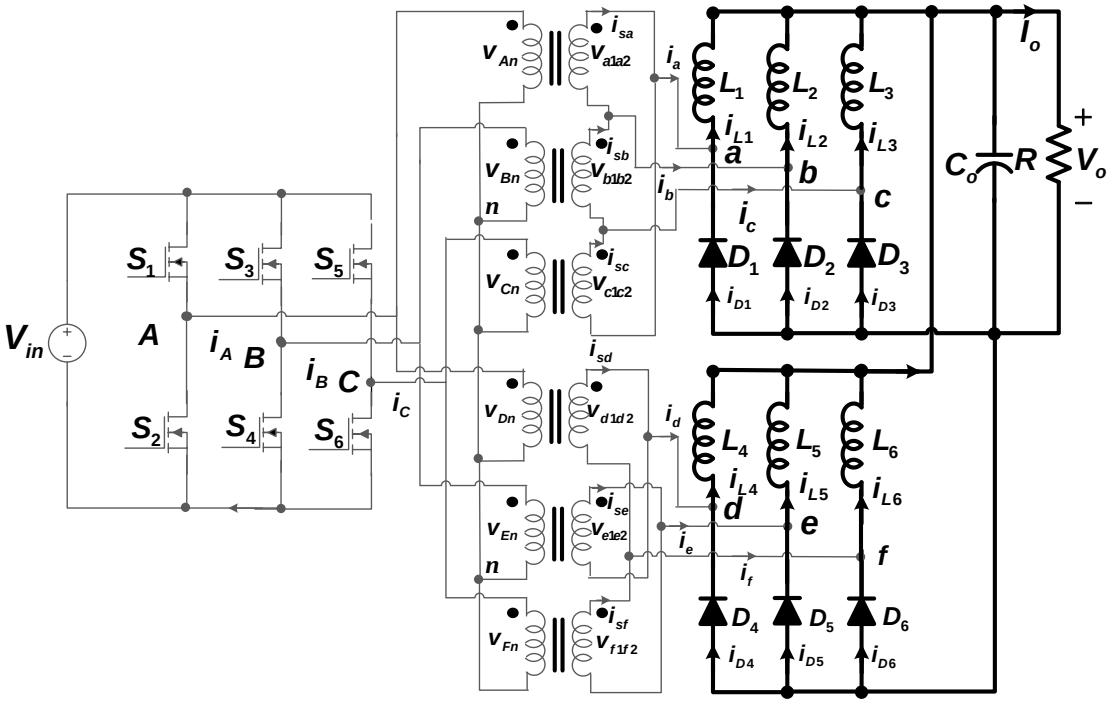


(b) mode-3

Fig. 6.11 Equivalent circuit of multiphase converter under asymmetrical control methods (a) mode-1 (b) mode-3



(a) mode-5



(b) mode-2,4,6

Fig. 6.12 Equivalent circuit of multiphase converter under asymmetrical control methods (a) mode-5 (b) mode-2,4,6

(e) Mode-5 $\left(\frac{2T}{3} < t < \frac{2T}{3} + DT\right)$*:* During this mode, switches (S_2, S_4, S_5) are ON and remaining switches are OFF as shown in Fig. 6.12(a). The voltage and current equations during this mode are depicted in Fig. 6.10.

6.4 Simulink Model for Simulation Studies

A 5kW, 5V/1000A simulink model of multi-phase high frequency isolated DC-DC converter with multi-phase rectification is developed using SimPowerSystem™ and Simulink of MATLAB software for experimentation. To verify the mathematical analysis the simulation study of proposed converter under symmetrical and asymmetrical control methods is carried out. Simulation results are presented in both steady-state and transient-state, with different loading conditions. Various parameters selected for simulation studies for 5kW, 5V/1000A proposed converter are as follows:

Input voltage , V_{in}= 600V DC with 10 -20% variations

Switching frequency, f= 10kHz

Single-phase HF Transformer, 2kVA,400V/40V

L_{lkp}= L_{lks}=0.05 μ H , L_m = 250 μ H, R_m = 500k ohms

Output filter inductor, L_1=L_2=L_3 = 25 μ H

Output filter capacitor, C_o=1000 μ F

Output voltage ripple, ΔV_o = 0.5%

Inductor current ripple , ΔI_L = 0.5%

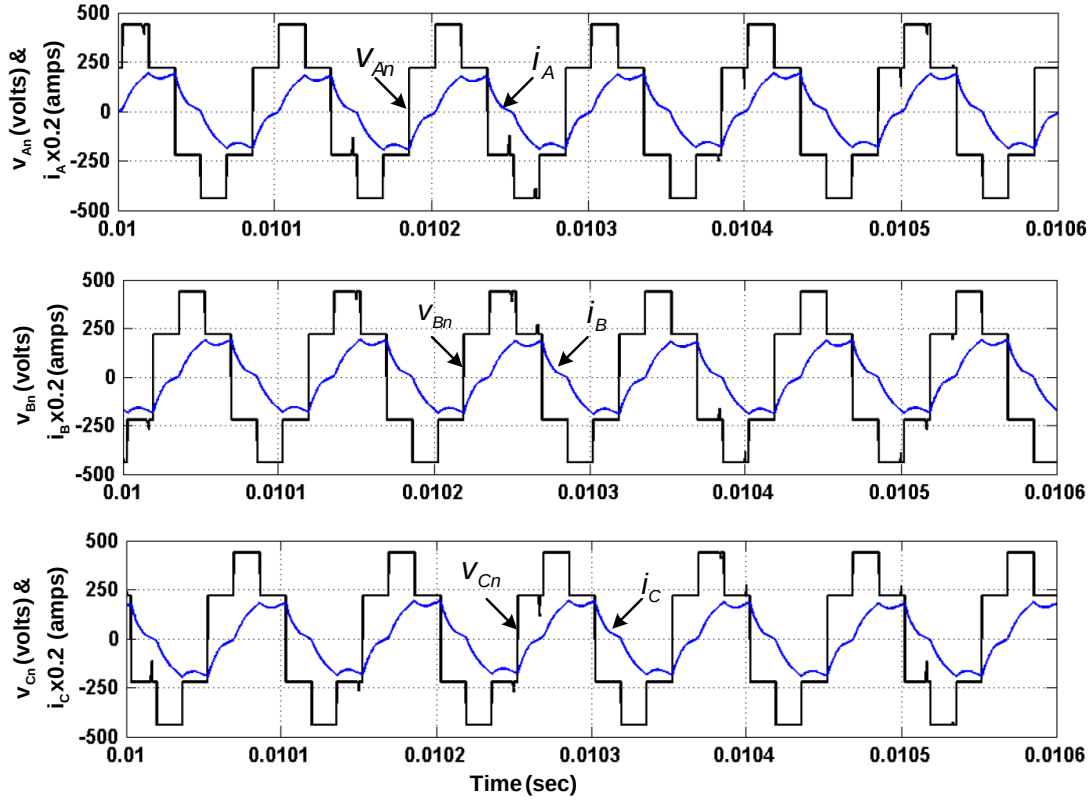
6.4.1 Simulation Results & Discussion

To investigate the performance of proposed converter, the simulation studies are carried out under symmetrical and asymmetrical control method. The steady-state and dynamic behaviour of proposed converter is also investigated under different operating conditions.

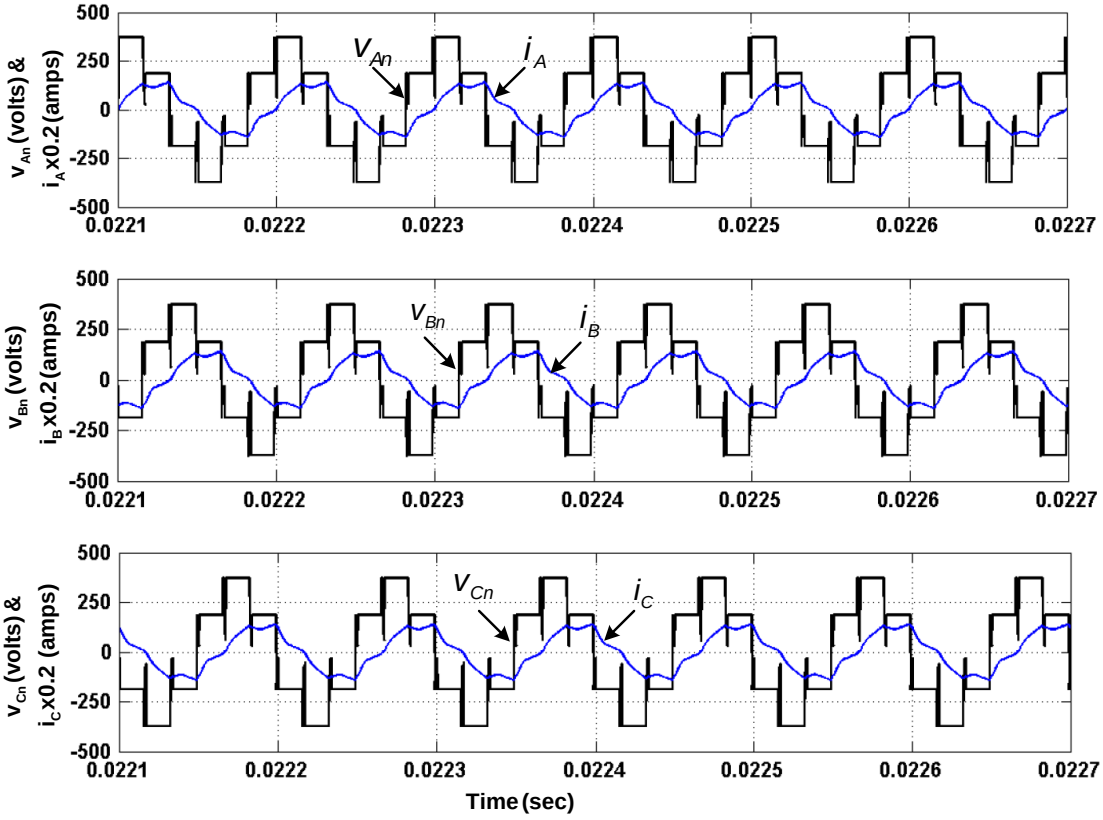
(a) Performance under Symmetrical Control

The simulation waveforms of phase voltages $(v_{An}, v_{Bn} \& v_{Cn})$ and line currents $(i_A, i_B \& i_C)$ at front end converter with input DC voltage $(V_{in} = 600V)$ at 120% of full load and input voltage $(V_{in} = 560V)$ at 80% of full load are given in Fig. 6.13. In these waveforms, duty ratio of switching devices is to be varied to regulate the output voltage against input voltage and load variations. In worst case design, converter operates with minimum input voltage $(V_{in} = 560V)$ to supply full load in region (Reg3) with duty ratio 0.45. As load decreased to 80% of full load or input voltage increase to high value, the operating region of converter is shifted in region (Reg2).

Fig. 6.14 and Fig. 6.15 show the primary side line current waveforms and its frequency spectrum which indicate the improvement in current waveform of i_A as compare to i_{A1} and i_{D1} over wide range of load.



(a)



(b)

Fig. 6.13 Phase voltage $(v_{An}, v_{Bn} \& v_{Cn})$ & line current $(i_A, i_B \& i_C)$ at front end converter with (a) $V_{in} = 600V$ at 120% of full load (b) $V_{in} = 560V$ at 80% of full load

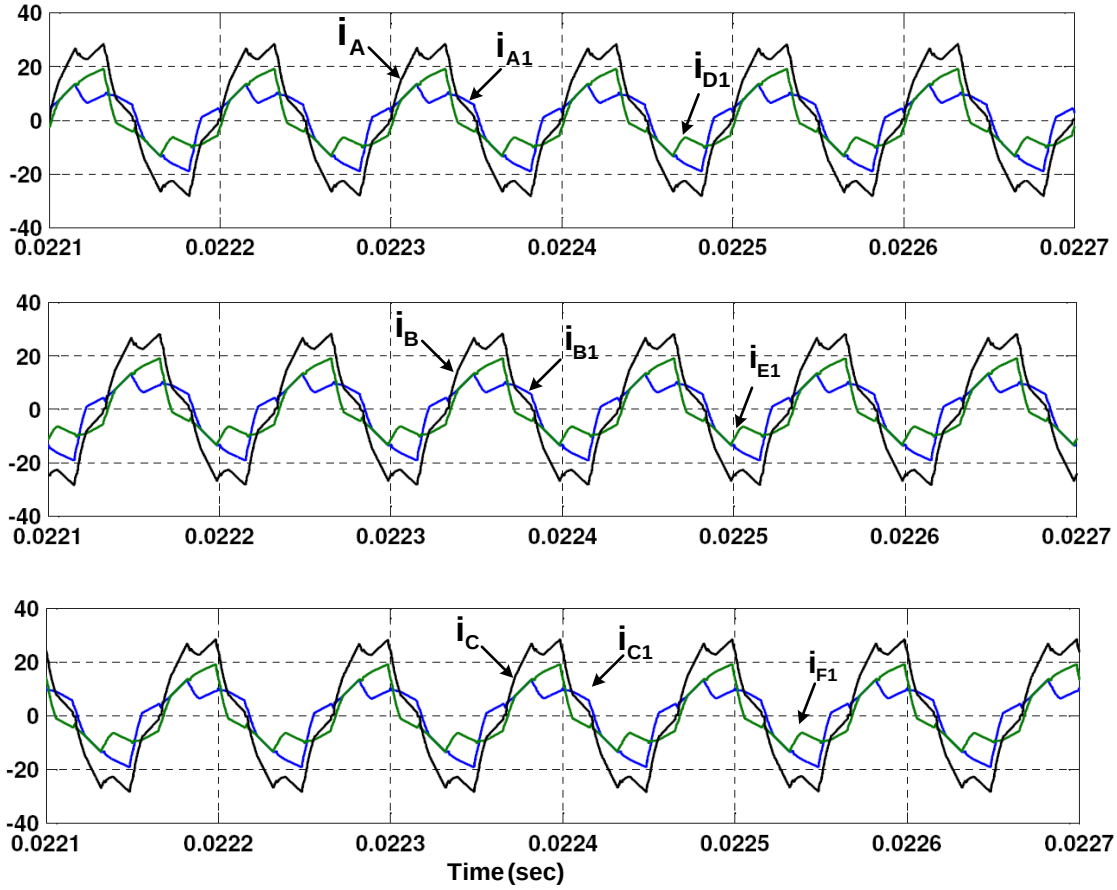


Fig. 6.14 Waveform of line currents $(i_A, i_B \,\&\, i_C)$ and primary winding currents $(i_{A1}, i_{B1}, i_{C1}, i_{D1}, i_{E1} \,\&\, i_{F1})$ of transformers

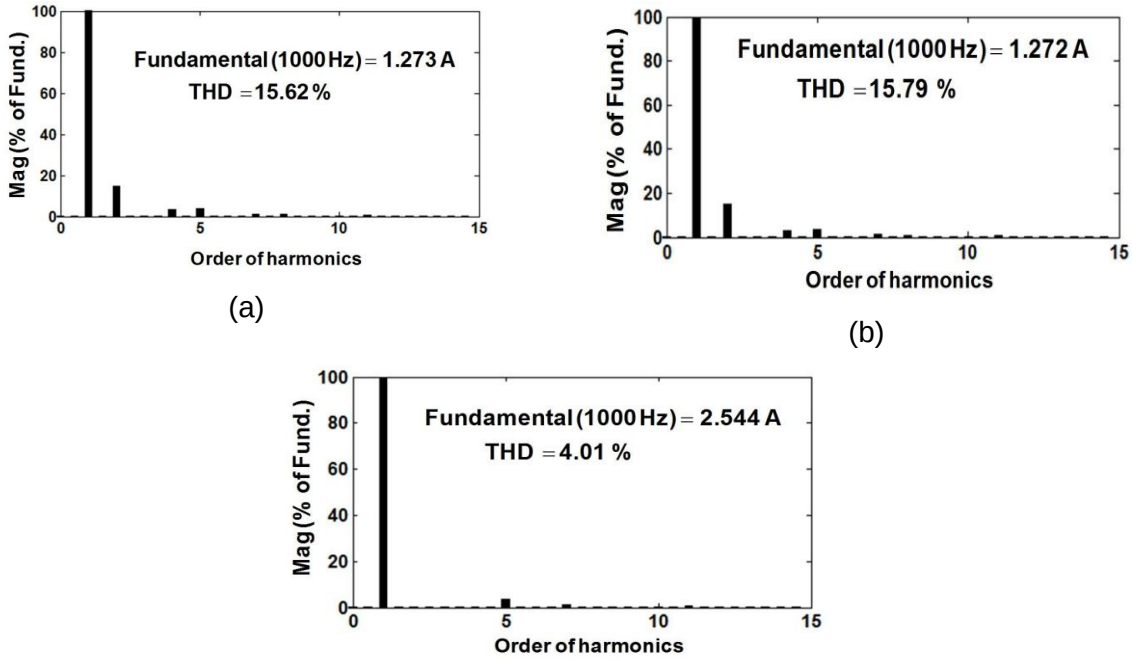
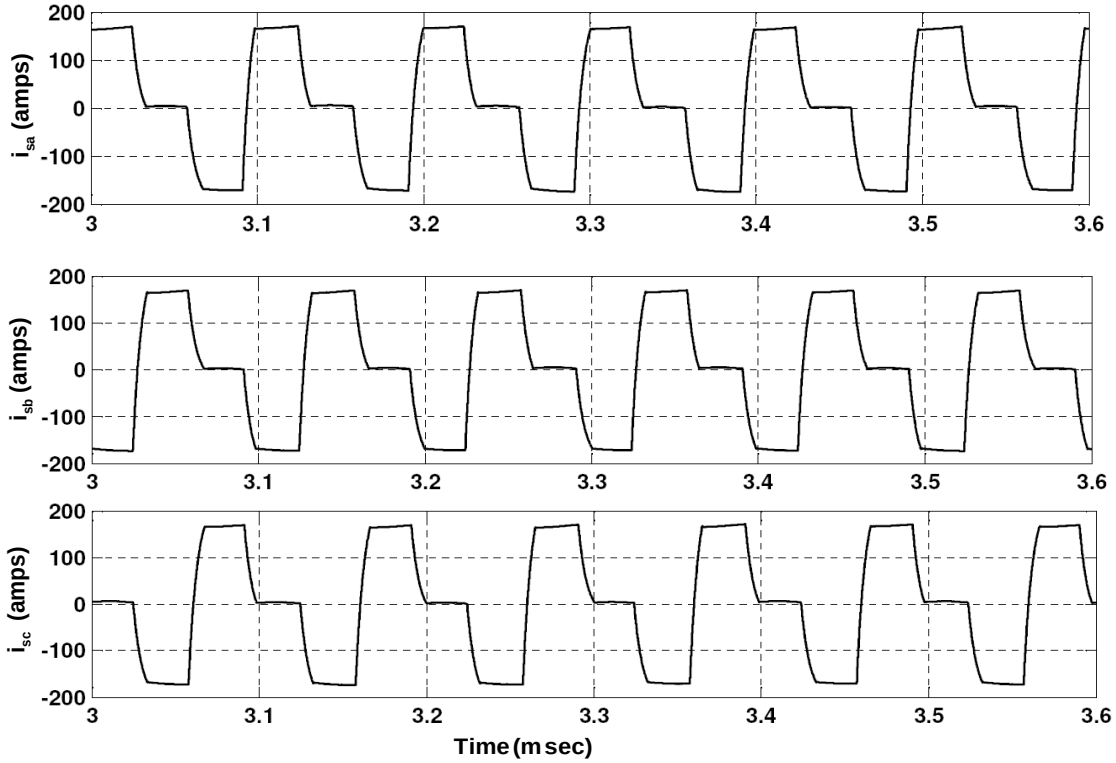
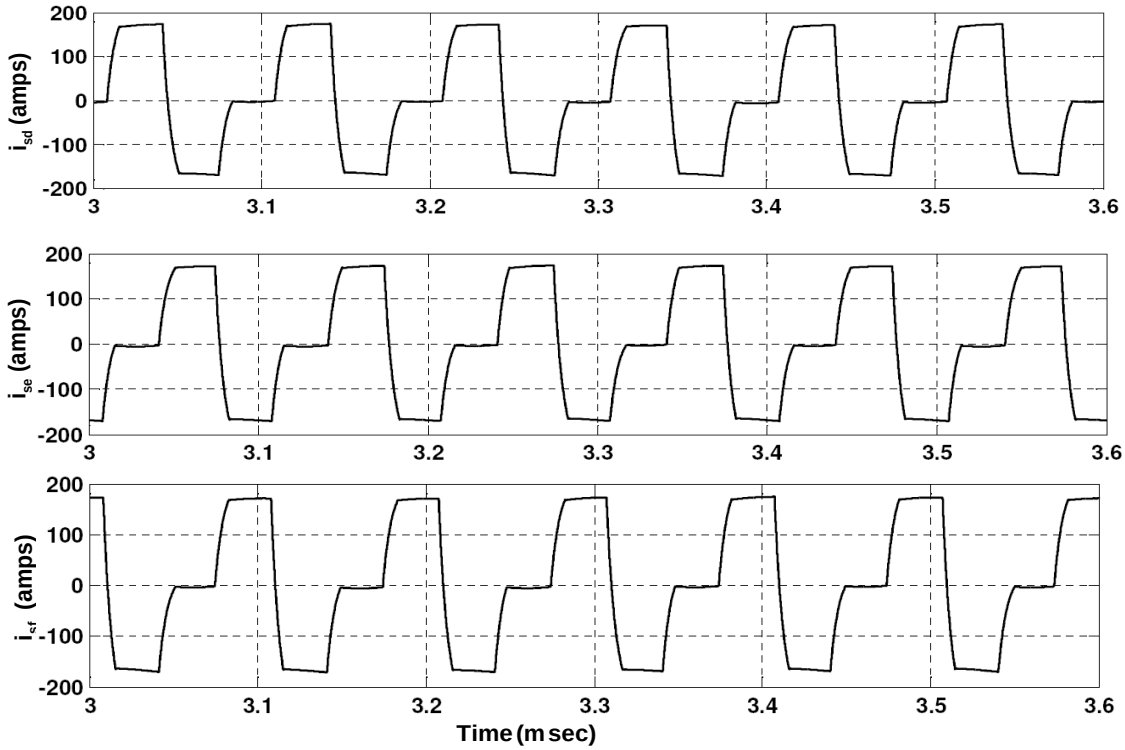


Fig. 6.15 Frequency spectrum of primary currents of transformer (a) i_{A1} (b) i_{D1} (c) i_A

Fig. 6.16 shows six winding currents $(i_{sa}, i_{sb}, i_{sc}, i_{sd}, i_{se}, \& i_{sf})$ of delta connected secondary windings of transformers which indicate that current in these windings is reduced and hence the conduction losses in transformer is reduced.



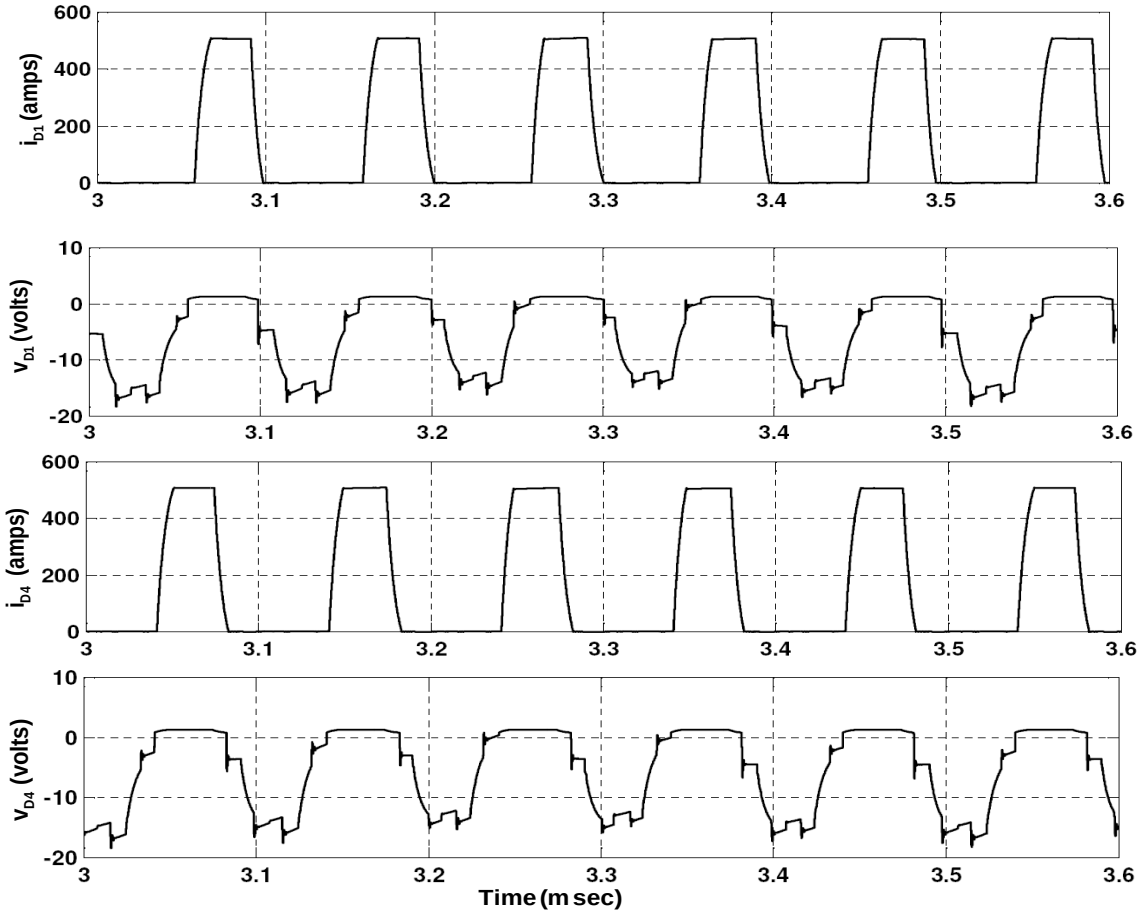
(a) YD1



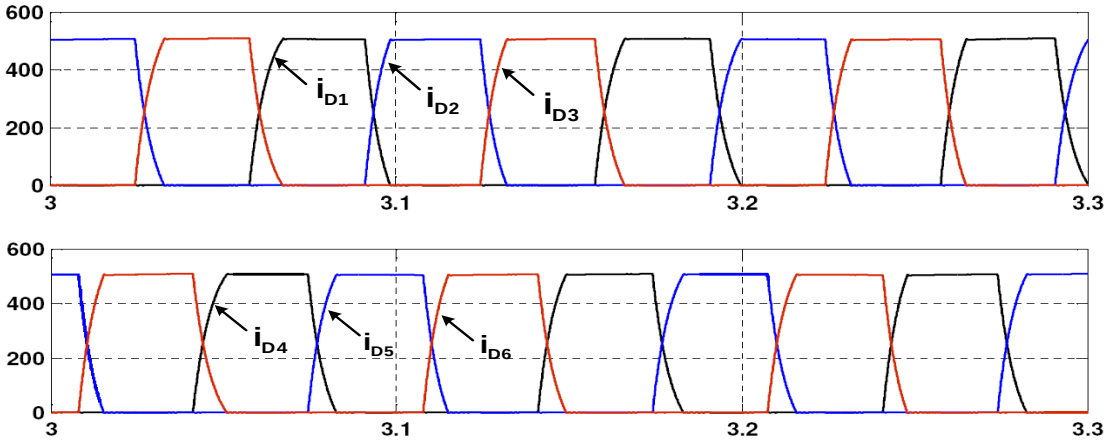
(b)YD11

Fig. 6.16 Secondary side winding currents in transformer (a) YD1 connection (b) YD11 connection

Fig.6.17(a) shows the voltage across rectifier diodes (v_{D1},v_{D4}) and current (i_{D1},i_{D4}) which indicate that peak current is half of full load current and during change over two rectifier diodes are conducting simultaneously. Thus, average current though each diode reduces and better thermal heat management is achieved. Fig.6.17(b) illustrates current through rectifier diodes at full load.



(a)



(b)

Fig.6.17 Voltage & current waveforms of rectifier diodes at full load with input voltage $(v_{in} = 600V)$ (a) diode currents (i_{D1},i_{D4}) and voltages (v_{D1},v_{D4}) (b) diode currents $(i_{D1},i_{D2},i_{D3},i_{D4},i_{D5}\ \&\ i_{D6})$

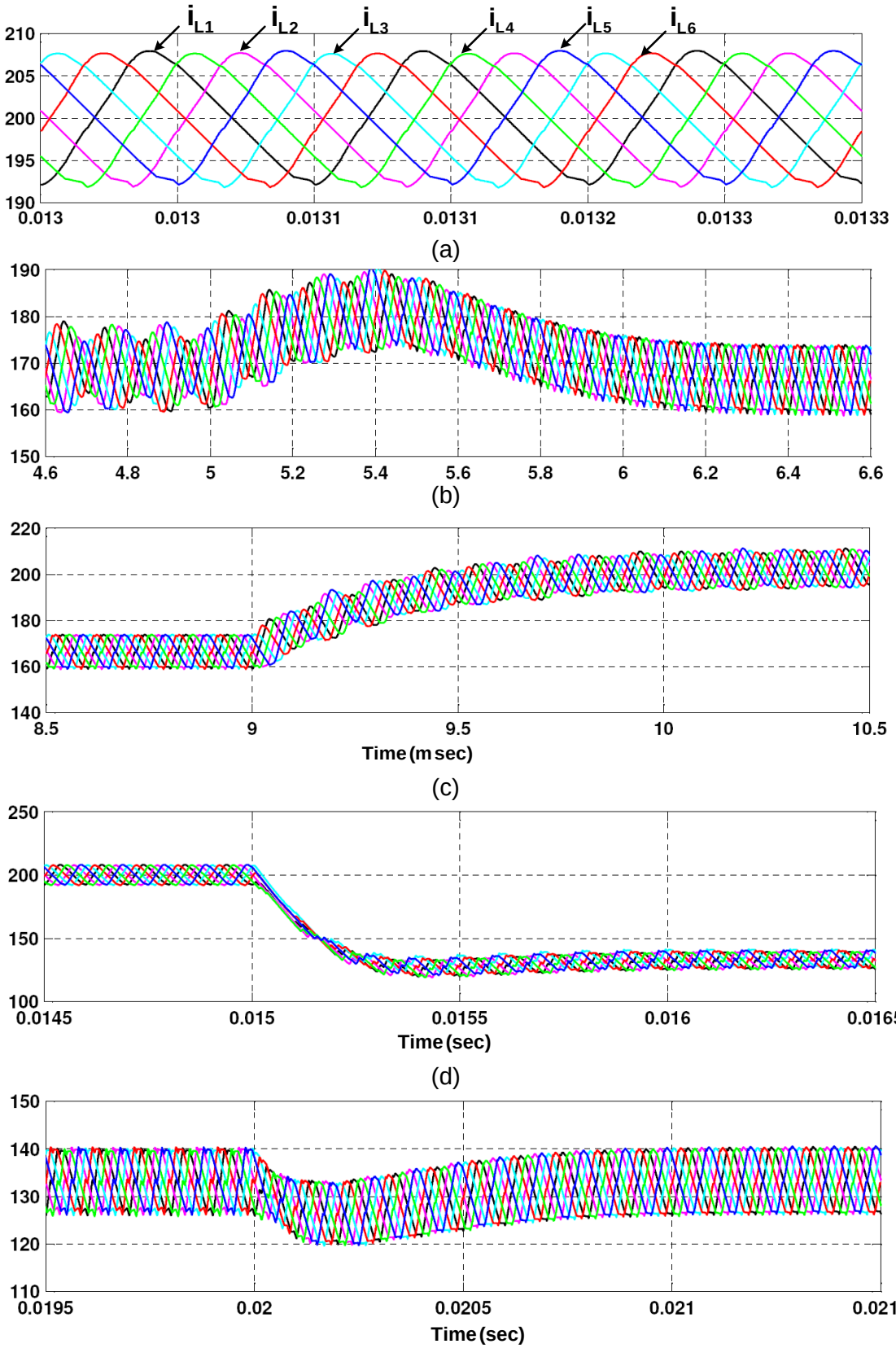
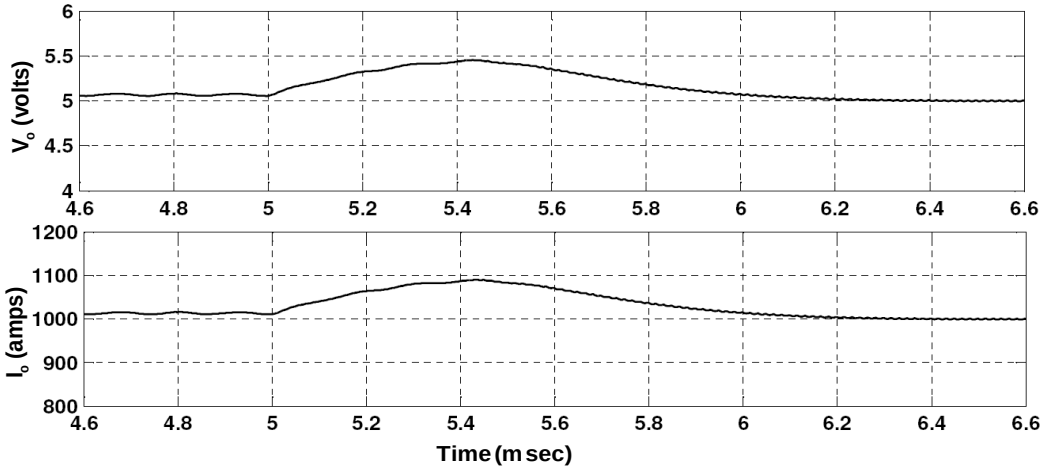


Fig. 6.18 Output inductor current sharing under different operating conditions (a) steady state (b) 10% increase in input voltage at $t = 5 m\,\text{sec}$ (c) 20% increase in full load current at $t = 9 m\,\text{sec}$ (d) 60% of full load current at $t = 0.015\,\text{sec}$ (e) 6% decrease in input voltage at $t = .02\,\text{sec}$

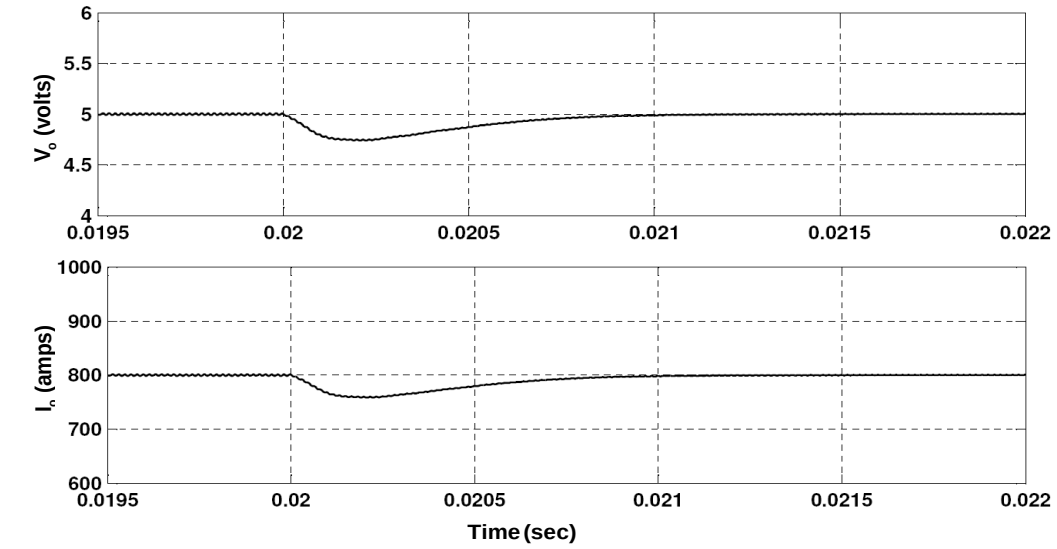
Fig. 6.18 illustrates current shared by output filter inductors under various operating conditions both at steady-state and transient-state. It is observed in Fig. 6.18(a) that each inductor shares one sixth of load current and ripple in individual inductor current is large, but due to equal phase-shifted PWM control (i.e. interleaved operation), the ripple content in load current is significantly reduced. Furthermore, for investigation the current shared by each inductor during transient conditions, the step change in input DC voltage and load current is carried outas below:

10% increase in input voltage at $t = 5m\sec$, 6% decrease in input voltage at $t = 0.02\sec$, 20% increase in full load current $t = 9m\sec$ and 60% of full load current $t = 0.015\sec$ are incorporated and corresponding change in inductor currents are shown in Fig. 6.18(b) to Fig. 6.18(e). It is concluded that inspite of several change in input voltage and load current, equal sharing of currents by each output inductor is maintained.

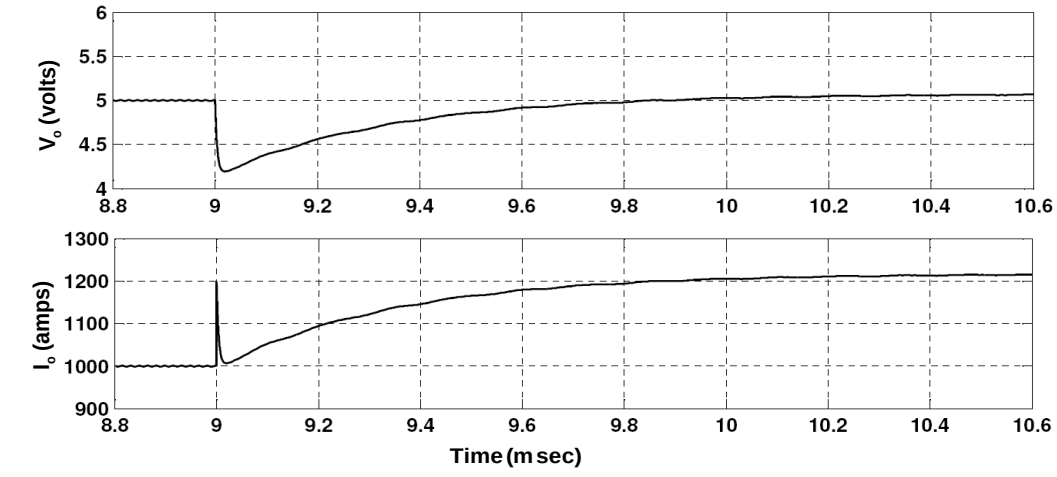
The transient response of proposed converter under symmetrical control method is investigated with variations in input DC voltage and load. The 10% step increase and 6% step decrease from nominal input voltage are introduced at instant $t = 5m\sec$ and $t = .02\sec$ respectively and corresponding variations in output voltage are shown in Fig. 6.19. It is observed that output voltage resumes its reference value i.e. $V_{ref} = 5V$ quickly after few disturbances from instant of disturbances. Furthermore, to study transient behaviour of converter against load variations, 20% sudden increase in full load current at $t = 9m\sec$ and sudden reduction of load current to 60% of full load current at $t = 0.015\sec$ are done and corresponding change in output voltage and load current are depicted in Fig. 6.19(c) to Fig. 6.19(d).



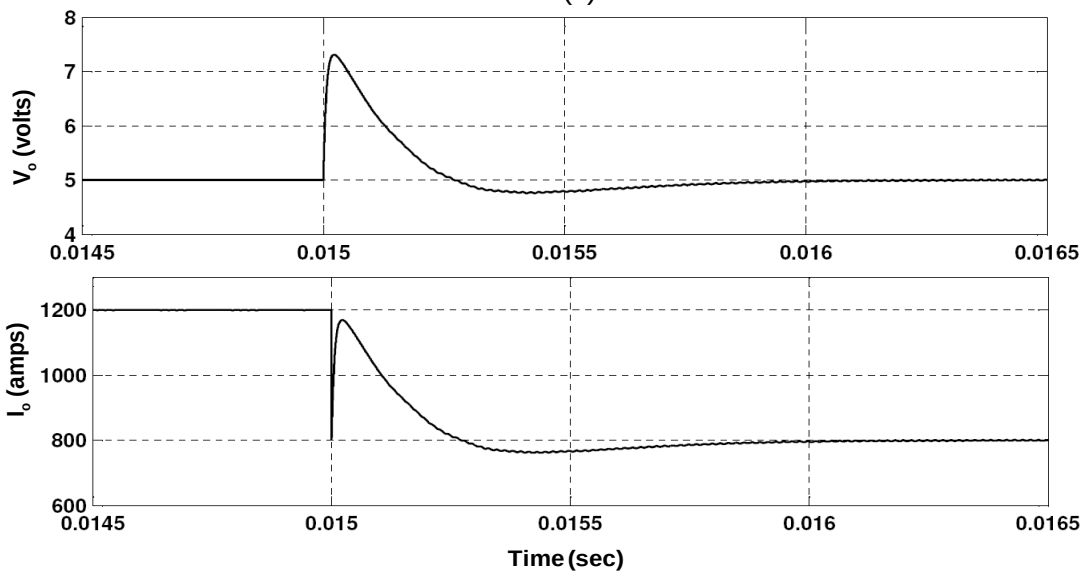
(a)



(b)



(c)



(d)

Fig. 6.19 Output voltage waveforms under different perturbations (a) 10% increase in input voltage at $t = 5m\sec$ (b) 6% decrease in input voltage at $t = .02\sec$ (c) 20% increase in full load current at $t = 9m\sec$ (d) 60% of full load current at $t = 0.015\sec$

(b) Performance under Asymmetrical Control

The simulation studies of proposed converter are carried out under asymmetrical control methods and obtained simulation results are discussed in this section. Fig.6.20 shows the line-line voltage appears across primary windings of transformers at steady-state. It is observed that sum of voltages at any instant is zero i.e $(v_{AB}+v_{BC}+v_{CA}=0)$ which indicates that magnetic structure of core can be simplified with magnetic core of three legs similar to core of three-phase transformer. This compact core size reduces the core losses in transformer.

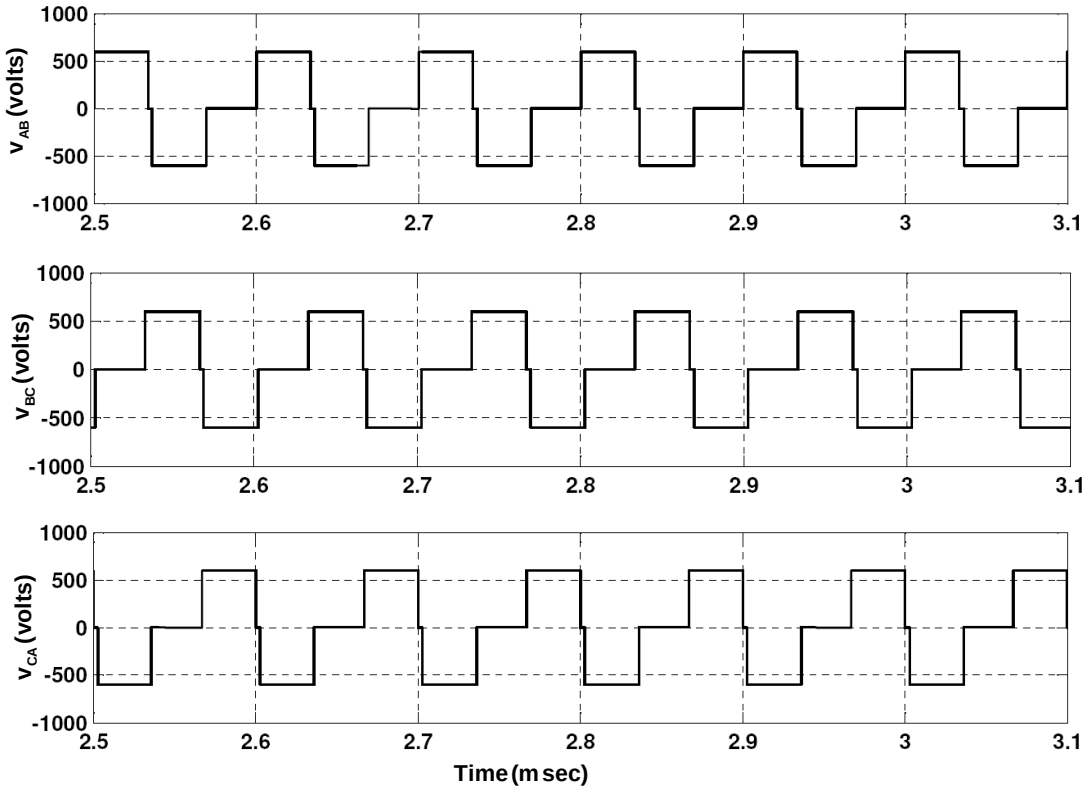
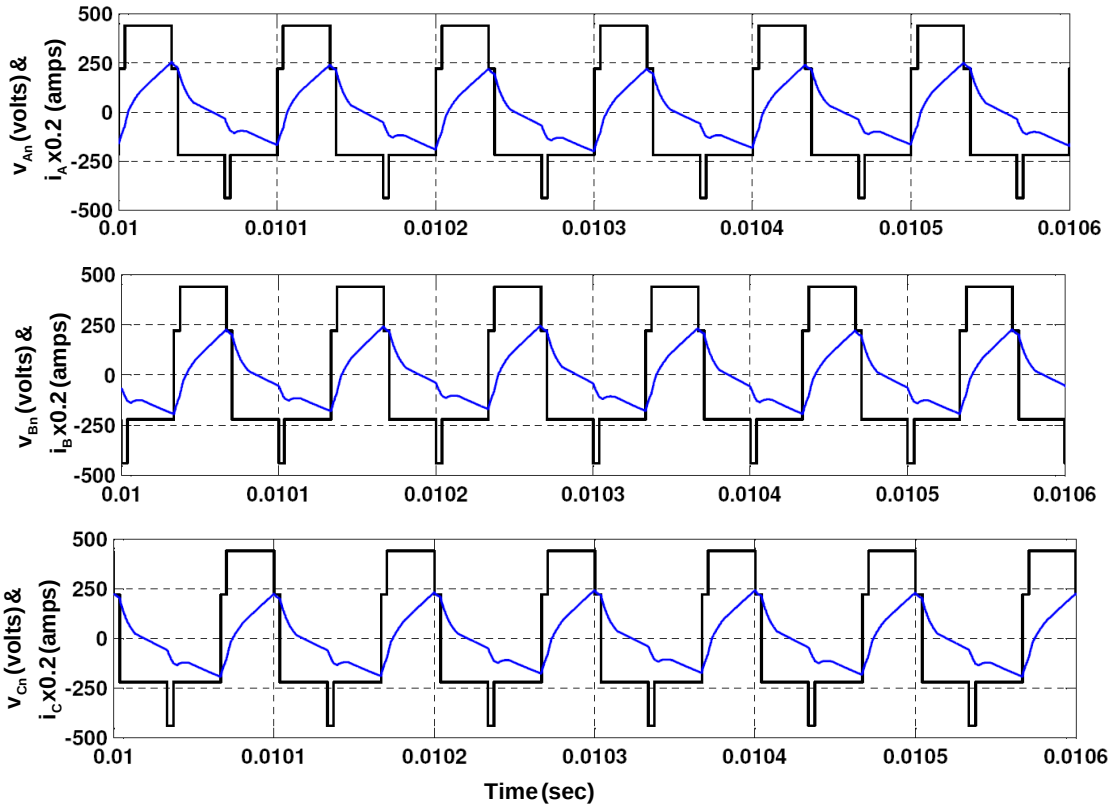


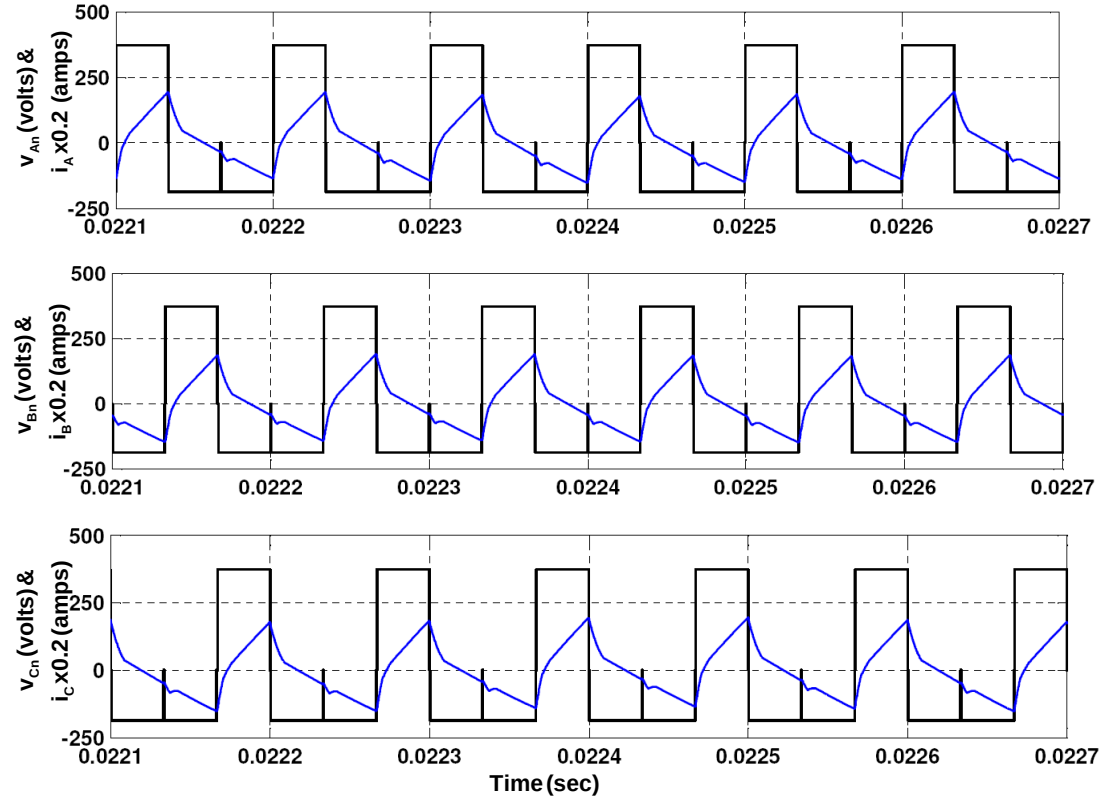
Fig.6.20 Line-line voltages (v_{AB}, v_{BC}, v_{CA}) applied to primary windings of transformer under asymmetrical control methods

Fig. 6.21(a) and Fig. 6.21(b) show the phase voltage appears across primary windings of transformers and line currents. It is observed that voltage waveforms mainly depend on converters operating regions (Reg1 and Reg2).

Fig. 6.22 and Fig. 6.23 are associated with primary windings currents and its frequency spectrum. It is observed that there is not much improvement in THD of current (i_A) when converter operates in region (Reg1). The currents in secondary windings of transformers are reduced as compared to other three-phase connections as shown in Fig. 6.24.



(a) Reg2



(b) Reg1

Fig. 6.21 Waveforms of input phase voltages $(v_{An} = v_{Dn}, v_{Bn} = v_{En}, v_{Cn} = v_{Fn})$ of transformers and line currents (i_A, i_B, i_C)

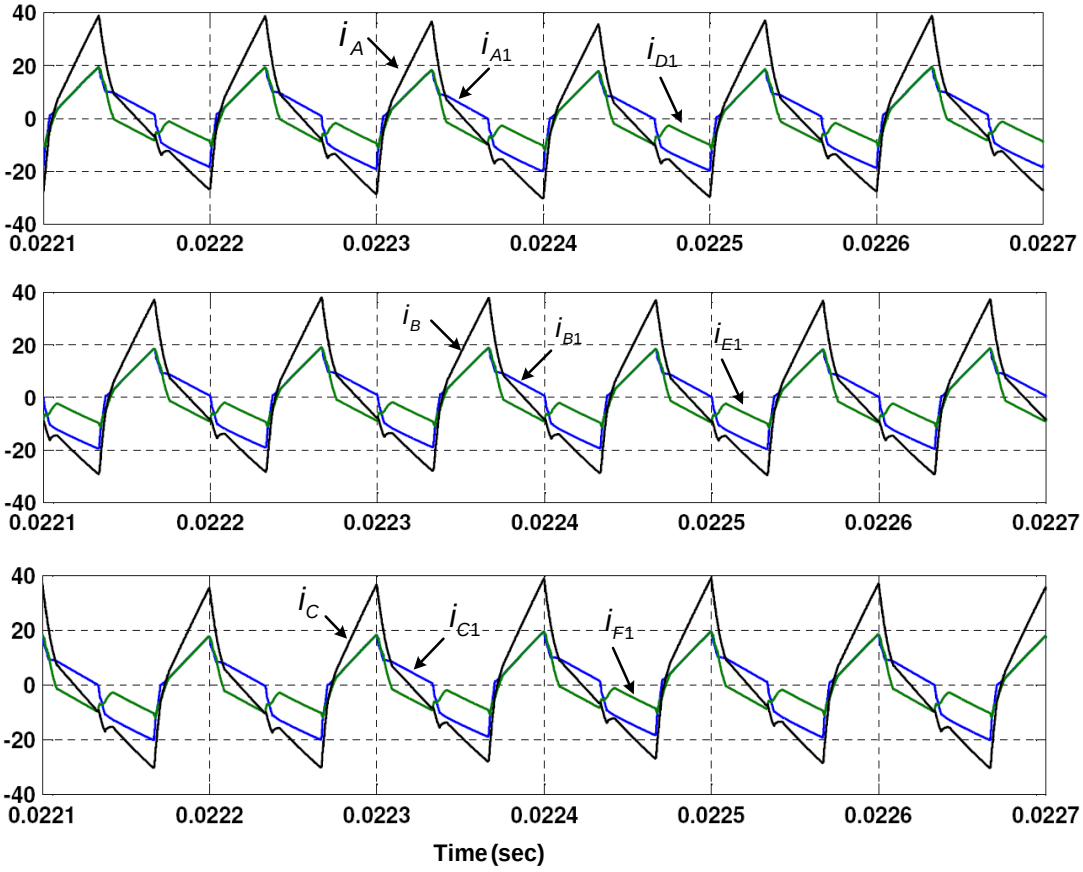
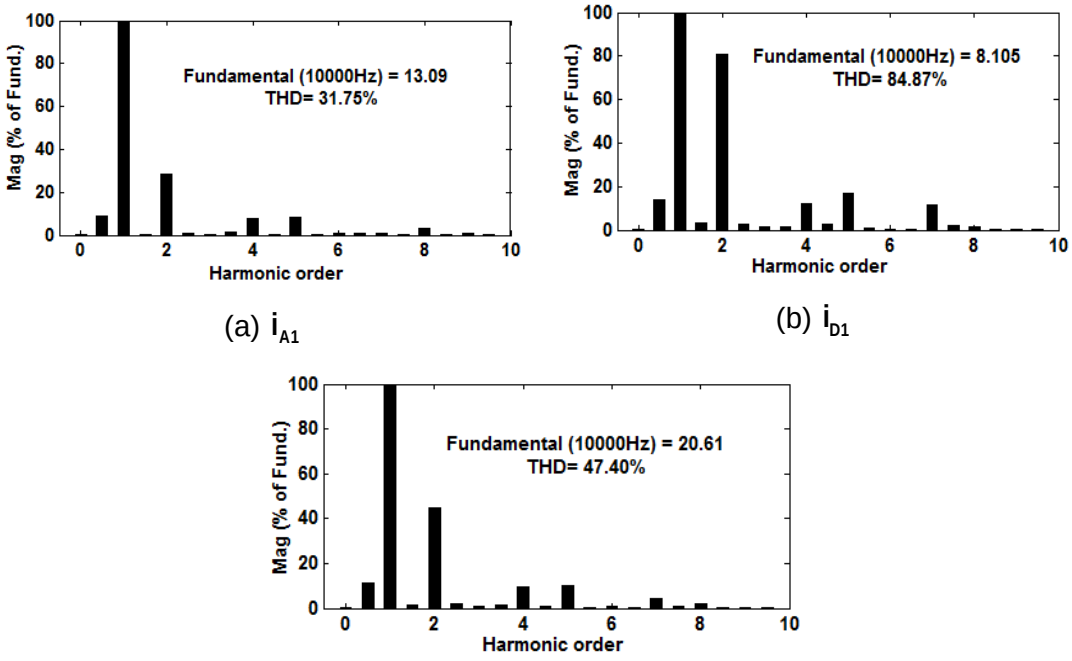


Fig. 6.22 Waveform of line currents $(i_A, i_B \& i_C)$ and primary winding currents $(i_{A1}, i_{B1}, i_{C1}, i_{D1}, i_{E1} \& i_{F1})$ of transformer

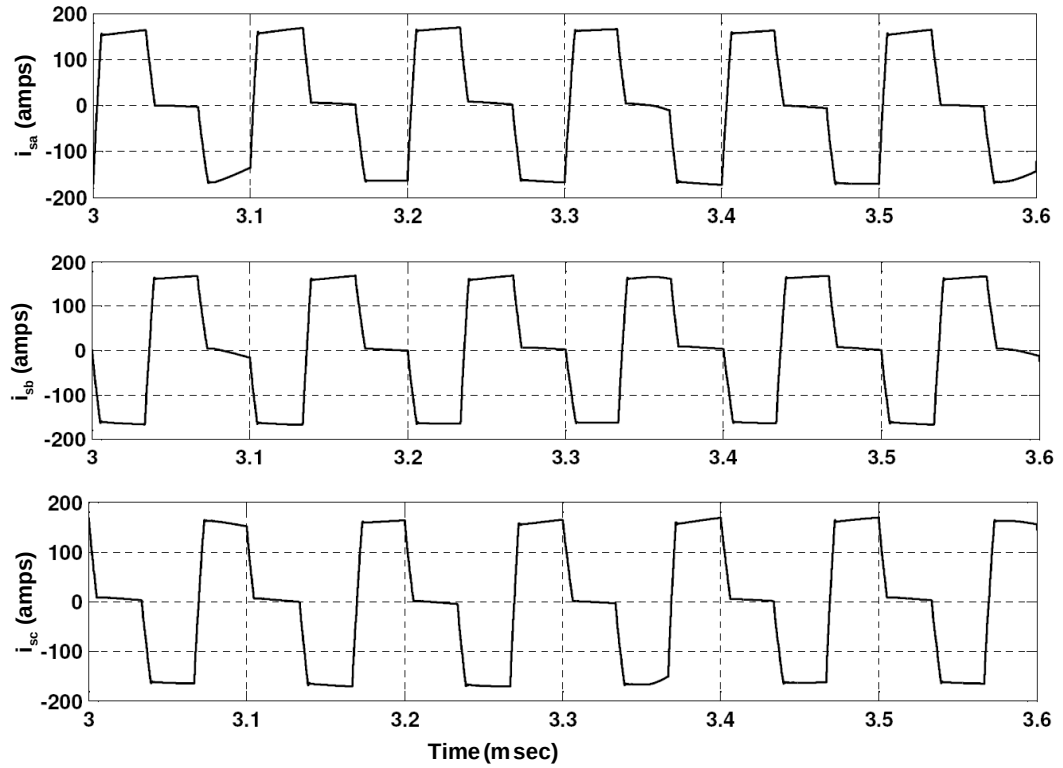


(a) i_{A1}

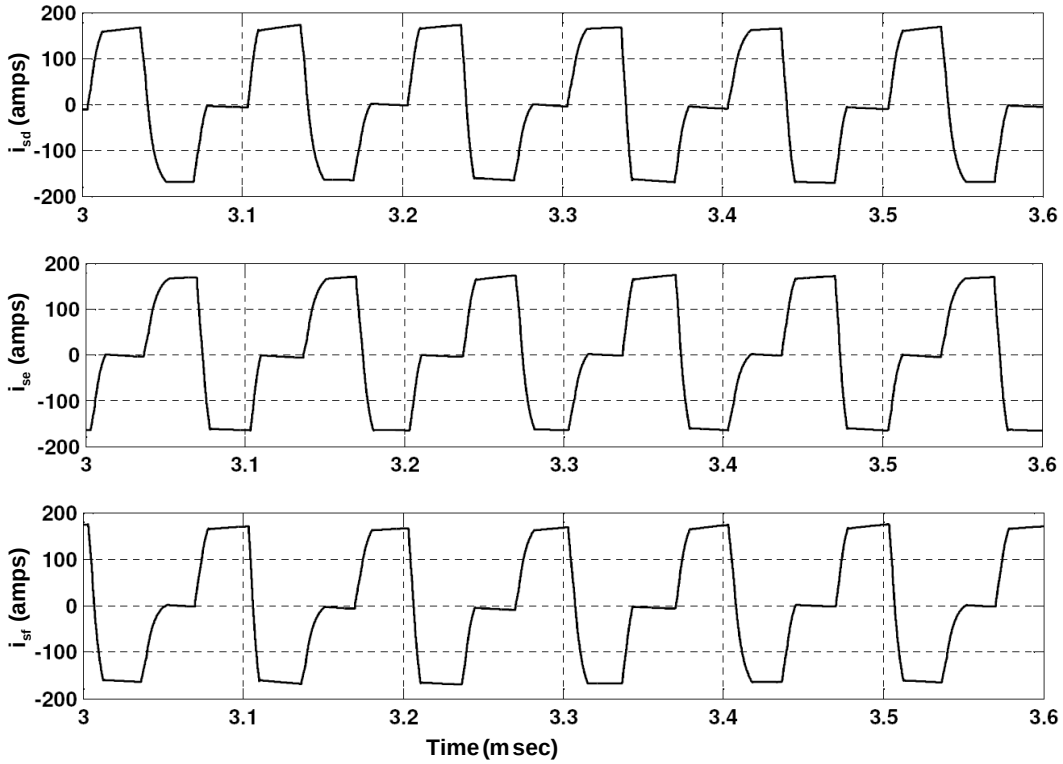
(b) i_{D1}

(c) i_A

Fig. 6.23 Frequency spectrum of primary currents (i_A, i_{A1}, i_{D1}) of transformers

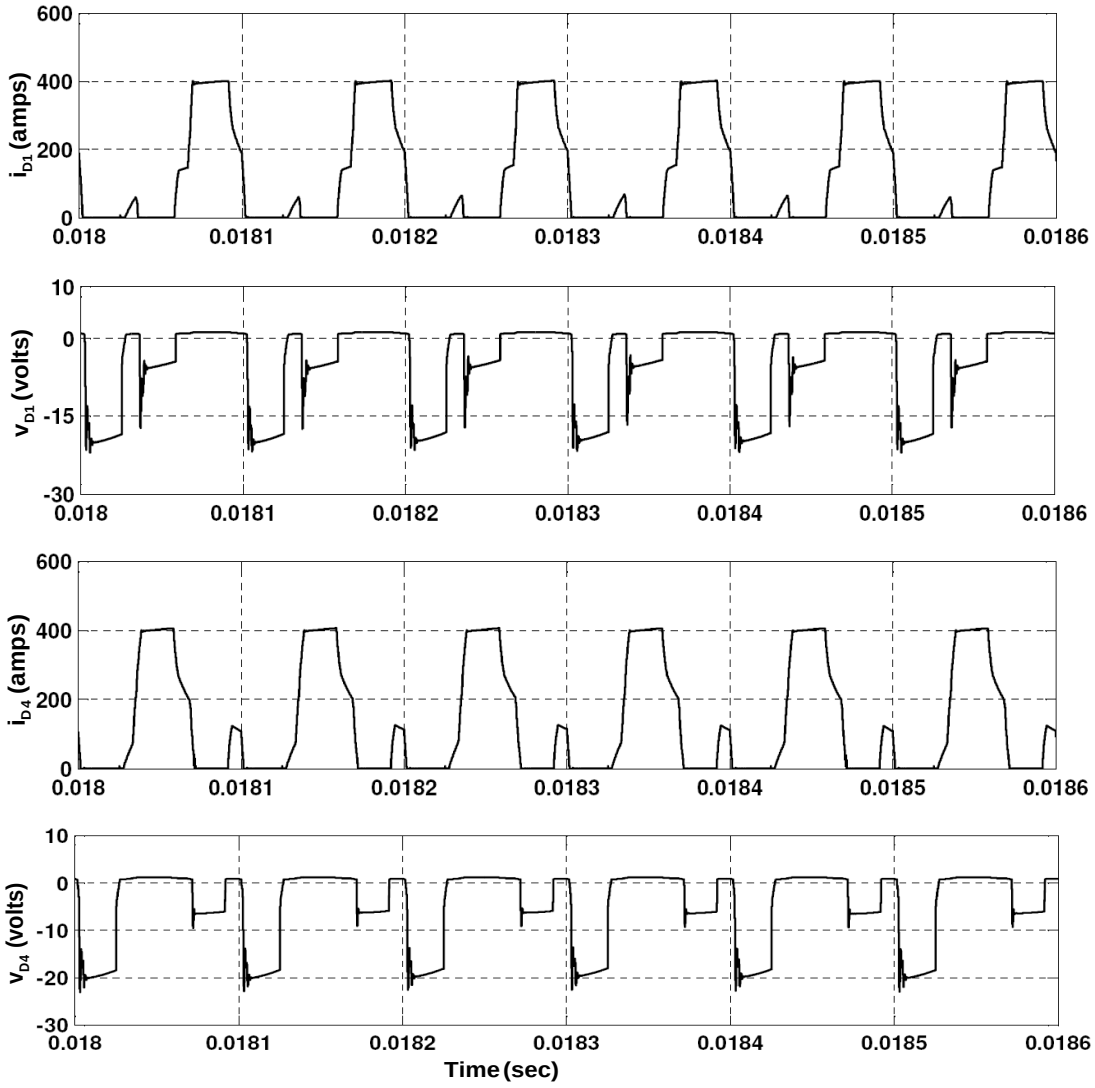


(a) YD1

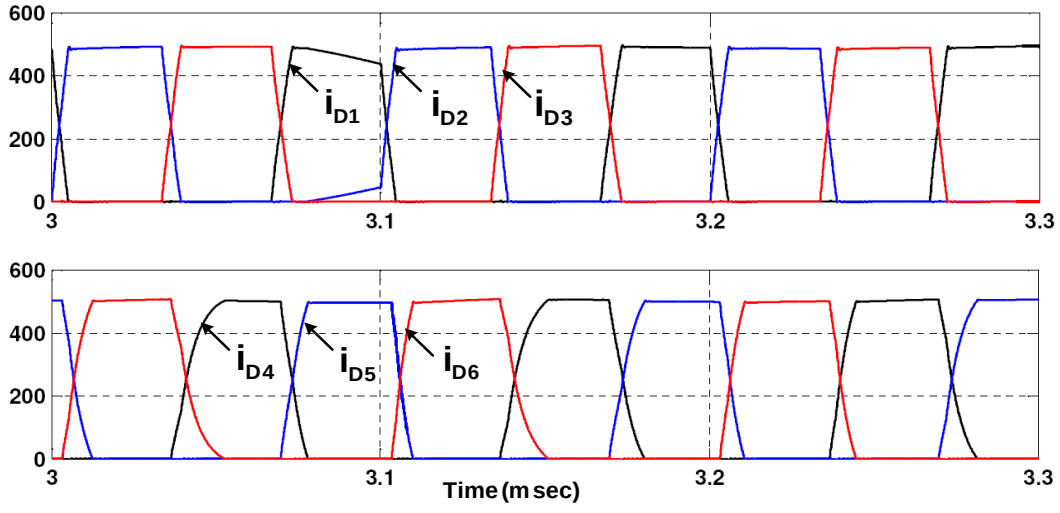


(b)YD11

Fig. 6.24 Secondary side winding currents in transformer (a) YD1 connection (b) YD11 connection



(a)



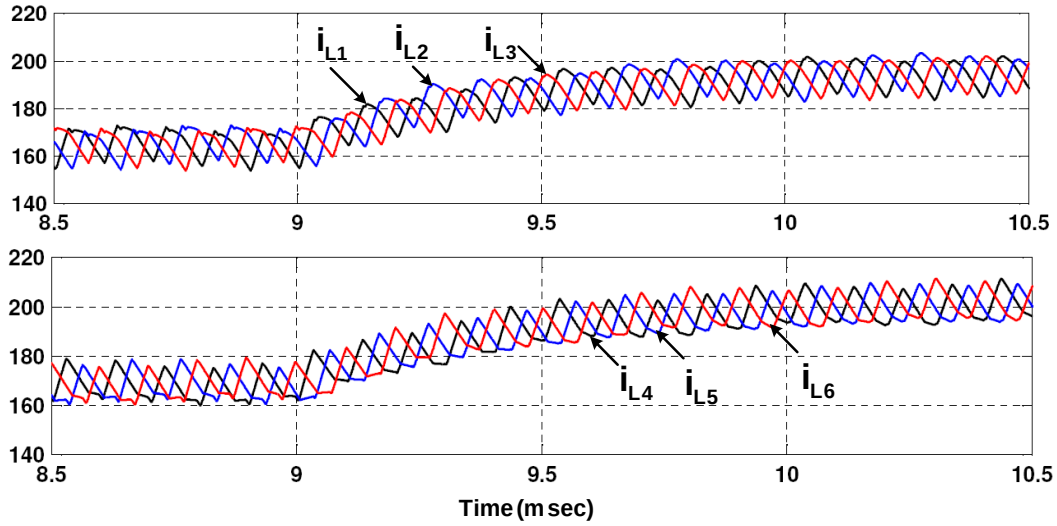
(b)

Fig. 6.25 Voltage and current waveforms of rectifier diodes at (a) load current of 800A (b) load current of 1000A

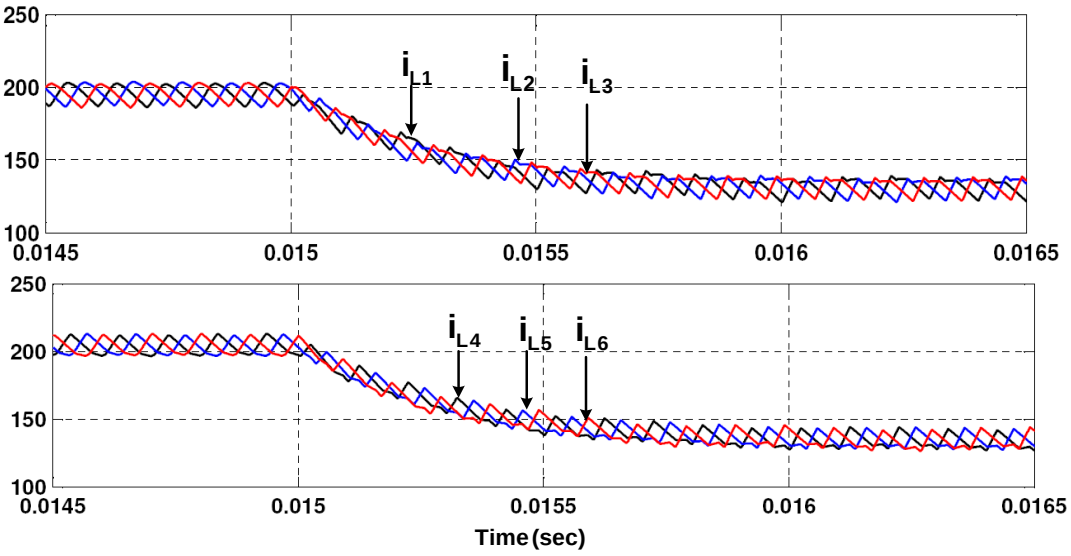
Fig. 6.25(a) shows the voltage across rectifier diodes (v_{D1},v_{D4}) and current (i_{D1},i_{D4}) when converter supplies full load current of 800A which indicate that peak current is 400A i.e. half of full load current and during change over two rectifier diodes are conducting simultaneously. Thus, average current though each diode reduces and better thermal heat management can be done. As load is increased to full load value, the operation of converter is shifted to region (Reg2) which is similar to operation of converter in region (Reg3) under symmetrical control method. The currents through rectifier diodes at full load with asymmetrical control method are shown in Fig. 6.25(b) which are similar to rectifier diode currents obtained under symmetrical control method as shown in Fig.6.17.

Fig.6.26 illustrates current shared by output inductors under various operating conditions both at steady-state and transient conditions. It is observed that each inductor shares one sixth of load current and ripple content in individual inductor current is large, but due to equal phase shifted PWM control (i.e. interleaved operation), the ripple content in load current is significantly reduced. To demonstrate current sharing by each inductor during transient conditions, the step change: 10% increase in input voltage at $t = 5m\sec$ and 6% decrease in input voltage at $t = 0.02\sec$, 20% increase in full load current $t = 9m\sec$ and 60% of full load current $t = 0.015\sec$ are incorporated and obtained simulation results are shown in Fig.6.26(a) to Fig.6.26(c). It is concluded that under all aforementioned variations, the output inductors share equal current similar to operation of converter under symmetrical control method.

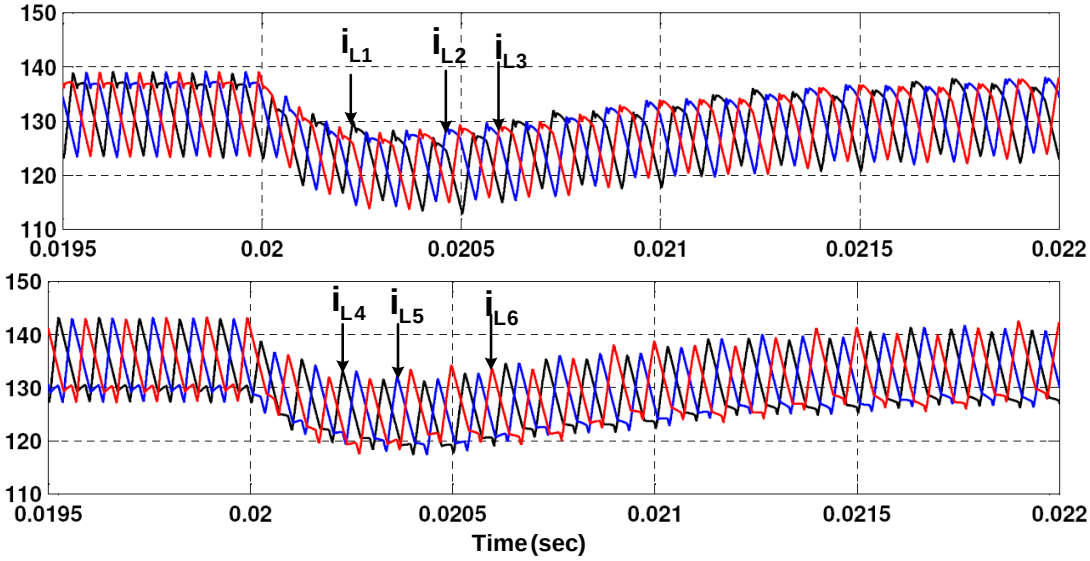
In order to investigate the performance of converter under input voltage variations: 10% step increase and 6% step decrease from nominal input voltage are introduced at instant $t = 5m\sec$ and $t = 0.02\sec$ respectively. The corresponding variation in output voltage is shown in Fig. 6.27. It is observed that output voltage settles to its reference value i.e. $V_{ref} = 5V$ quickly even less than 1.6 sec . Furthermore, to study transient behaviour of converter against load variations, 20% increase in full load current at $t = 9m\sec$ and reduction of load current to 60% of full load current at $t = 0.015\sec$ has been done and obtained simulation results are depicted in Fig. 6.27 (c) to Fig. 6.27(d).



(a)

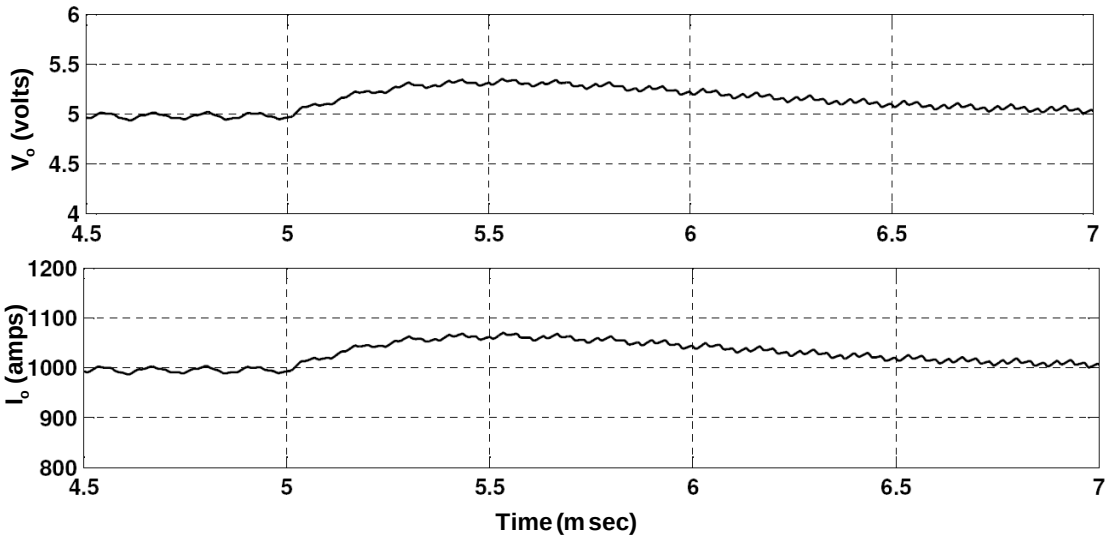


(b)

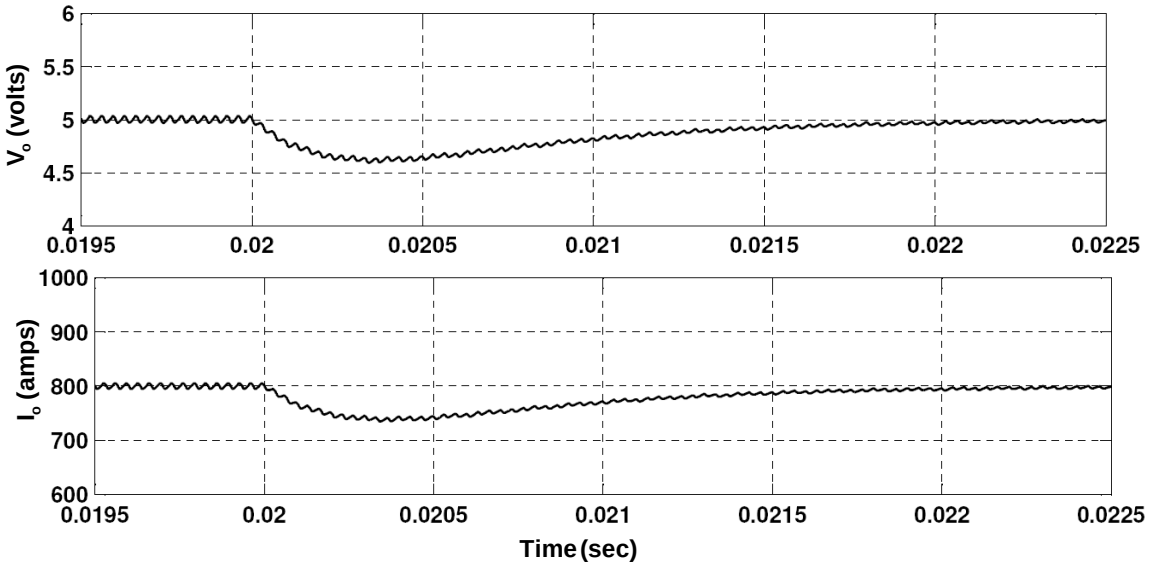


(c)

Fig.6.26 Output inductor current sharing under different operating conditions (a) 20% increase in full load current at $t = 9 m\,\text{sec}$ (b) 60% of full load current at $t = 0.015\,\text{sec}$ (c) 6% decrease in input voltage at $t = 0.02\,\text{sec}$

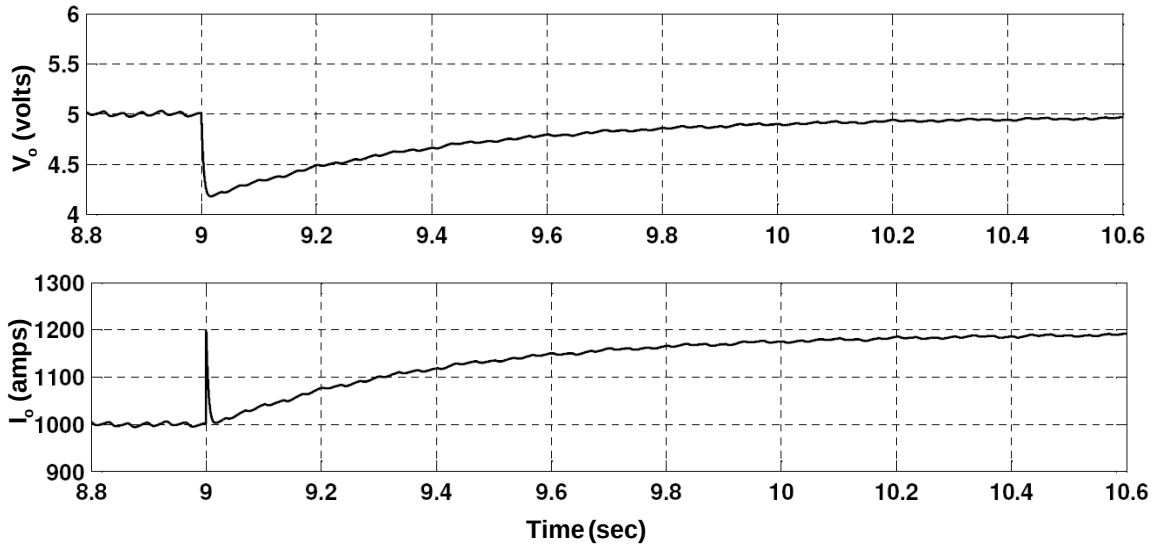


(a)

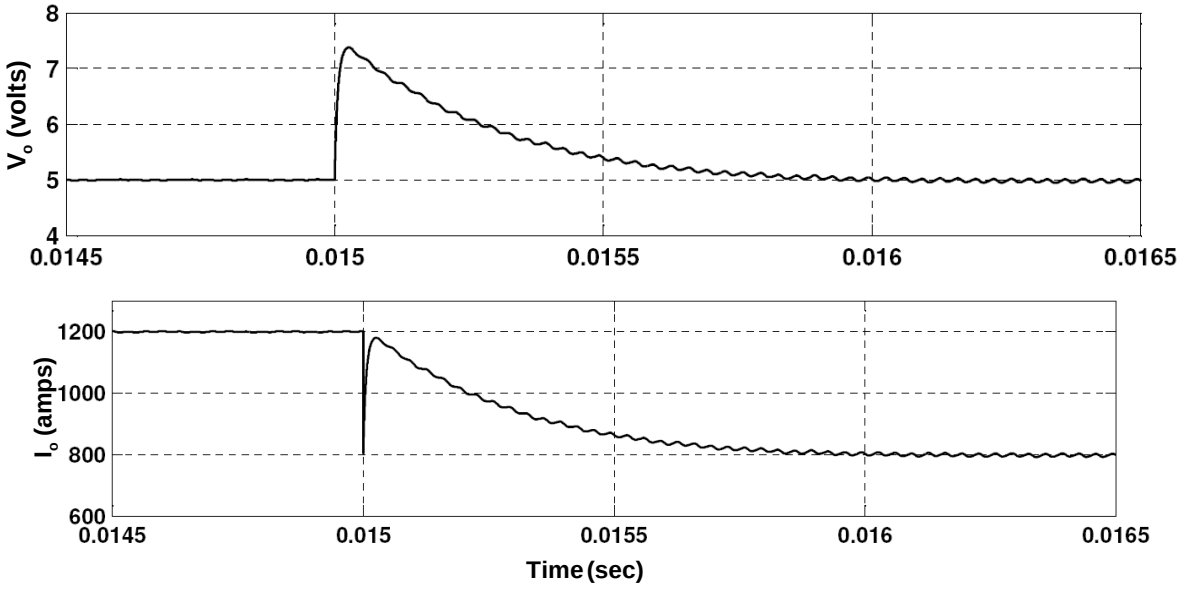


(b)

Fig. 6.27 Waveform of output voltage (V_o) variation with (a) 10% increase in input voltage at $t = 5m\sec$; (b)) 6% decrease in input voltage at $t = 0.02\sec$



(a)



(b)

Fig. 6.28 Waveform of output voltage (V_o) variation with (a) 20% increase in full load current at $t = 9m\sec$ (b) 60% of full load current at $t = 0.015\sec$

6.5 Experimental Validation

In the simulation studies presented in previous section, multi-phase isolated DC-DC converter with multi-phase rectification is developed with rating 5 kW, 5V/1000A, but due to constraints of practical limitations, the experimental studies are conducted at a reduced rating. As experimental studies are conducted at reduced rating of proposed converter, for validating the experimental results, the simulation studies are also carried out with reduced rating of converter.

6.6 Prototype model

A 1.5V/100A prototype model of multi-phase isolated DC-DC converter with multi-phase rectification is built in the laboratory with specifications tabulated in Table 6.1 and its schematic diagram is shown in Fig.6.29. The system hardware is developed in three stages namely the development of power circuits, control circuits and protection circuits as given in chapter-3. The power circuit of proposed converter consists front end converter, high frequency transformer and multi-phase rectifier stage. Six MOSFETs (IRFP460A) with protected by well designed snubber circuits are used to form three-legs of front end converter. Two units of three-phase transformers are practically implemented with six unit of single-phase transformer fabricated using EE65 ferrite core, primary winding of 209 turns with 19 SWG Cu wire and secondary windings of 24 turns with 17 SWG Cu-wire. The leakage inductance and magnetizing inductance are adjusted with maintaining suitable air-gap so-that the designed value of resonant tank parameters can be achieved. The output filter inductors $(L_1 - L_6)$ and output capacitor (C_o) are large enough to smooth out ripples at switching frequency (1kHz) and maintaining continuous current conduction.

A DSP DS1104 of dSPACE is used for the real-time simulation and implementation of control algorithms. The control algorithm is first designed in the MATLAB Sim Power System tools software and the Real-Time Workshop of MATLAB automatically generates the optimized C-code for real-time implementation. The interface between MATLAB and Digital Signal Processor (DSP, DS1104 of dSPACE) allows the control algorithm to be run on the hardware, which is an MPC8240 processor. The master bit I/O is used to generate the required six gate pulses and one analog to digital converters (ADCs) to implement close loop control. Switching signals obtained from controller are given to the power MOSFETs $(S_1 - S_6)$ after proper isolation and amplification.

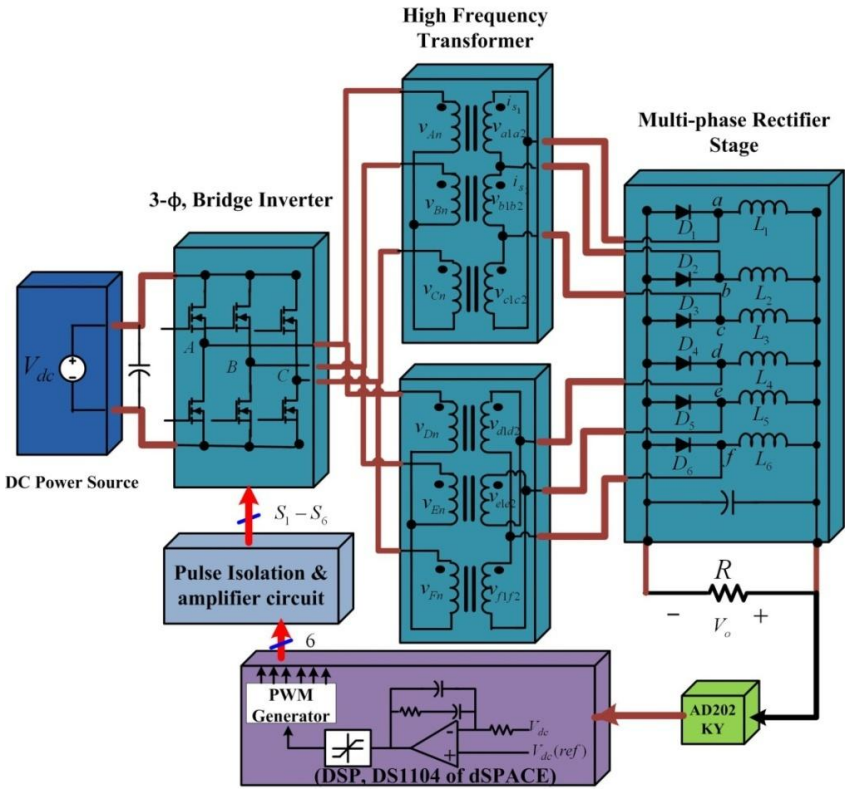


Fig.6.29 Schematic diagram of multi-phase DC-DC Converter with multi-phase rectification

Table 6.1 Specifications of hardware components used

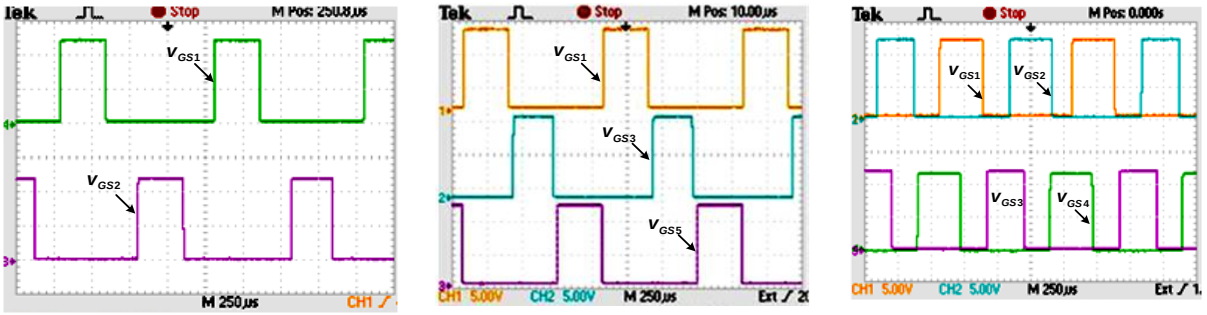
Parts	items	Quantity	Components /Rating
Input voltage	V_{in}	1	220V, DC
Power switches	$(S_1 - S_6)$	6	IRFP 460A
Rectifier diodes	$(D_1 - D_6)$	6	25D40R
Single-phase Transformer	$(T_a - T_f)$	6	250 VA, E65ferrite core, Turns ratio-209/24
Filter inductor	$(L_1 - L_6)$	6	EE65 ferrite core, 5mH
Output capacitor	C_o	1	Electrolyte, 1000µF, 50V
Digital Signal Processor	-	1	DSP DS1104

6.6.1 Experimental Results and Discussions

The performance of prototype model of proposed converter with symmetrical and asymmetrical control methods is investigated under different operating conditions. The experimental results obtained are discussed below:

(a) Performance under symmetrical control method

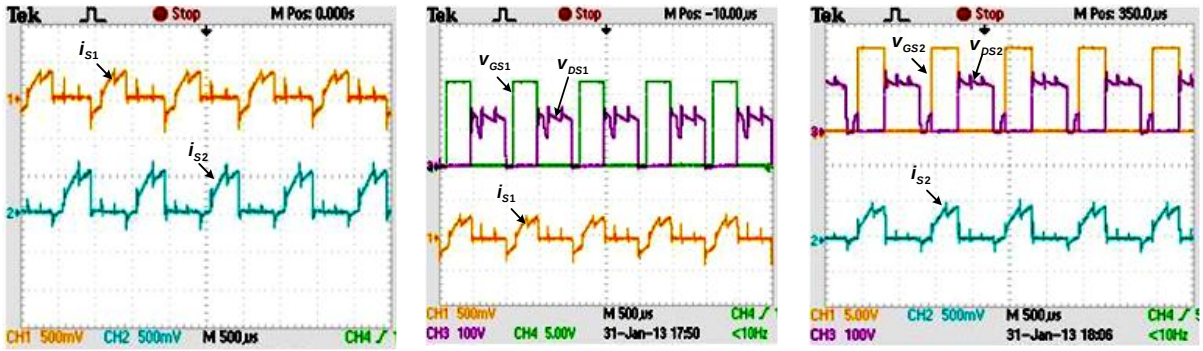
A prototype model of multi-phase high frequency isolated DC-DC converter rated at 1.5/100A is built and tested under symmetrical control methods with various operating conditions. The experimental results depicted in Fig. 6.30 show the gate to source voltages of switching devices which indicate that switches of front end converter are operated in symmetrical manner. Fig. 6.31 shows voltages (v_{DS1}, v_{DS2}) and currents (i_{S1}, i_{S2}) of power switches(S_1,S_2) of one leg of front end converter. The negative portion of switch currents (i_{S1}, i_{S2}) indicates that anti-parallel body diode of switches(S_1,S_2) are conducting and hence creating zero voltage switching condition. For validating the experimental results of Fig. 6.31, the simulation results of voltage and current switches of simulink model with reduced equivalent rating are shown in Fig.6.32.



(a) (b) (c)

$(v_{GS}: 5V/div, X-axis: 250\,\mu s/div)$

Fig. 6.30 Gate to source voltages of MOSFETs (a) v_{GS1}, v_{GS2} (b) v_{GS1}, v_{GS3}, v_{GS5} (c) v_{GS1}, v_{GS2}, v_{GS4}, v_{GS3}



(a) (b) (c)

$(v_{DS1} \& v_{DS2}: 200V/div, i_{S1} \& i_{S2}: 2A/div, v_{GS1} \& v_{GS2}: 5V/div, X-axis: 500\,\mu s/div)$

Fig. 6.31 Voltage and current aasociated with power switches (S_1,S_2) of front end converter (a) i_{S1}, i_{S2} (b) v_{GS1}, v_{DS1}, i_{S1} (c) v_{GS2}, v_{DS2}, i_{S2}

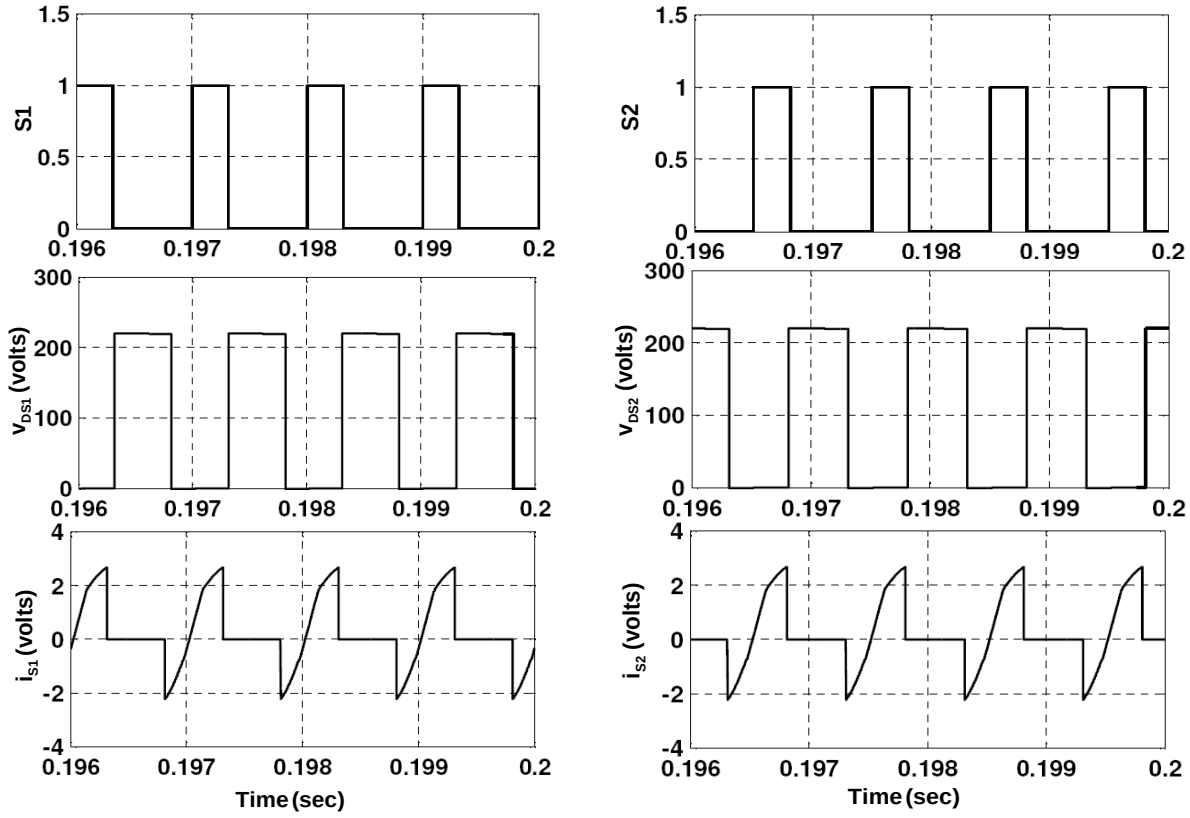
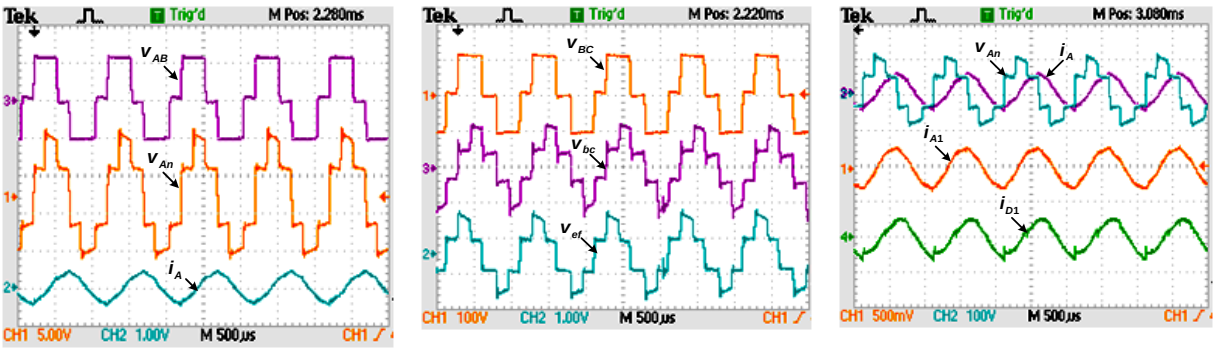
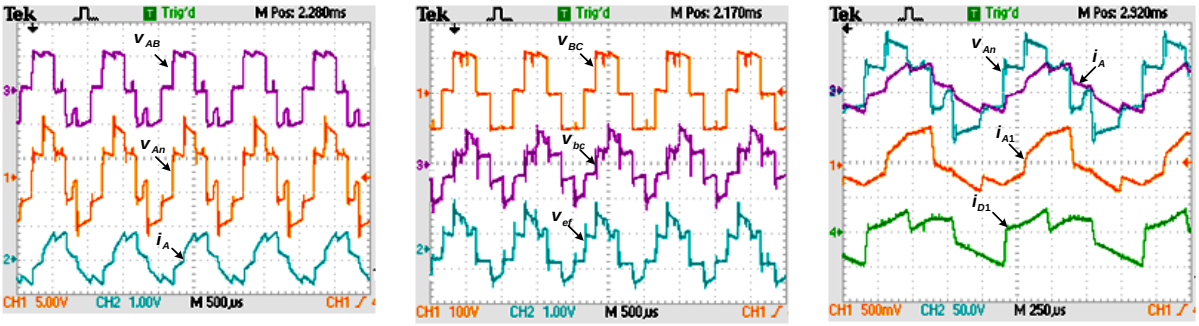


Fig.6.32 Simulated voltage and current waveforms of power switches (a) switching pulses of S_1, v_{DS1}, i_{S1} S_1 and (b) S_2, v_{DS2}, i_{S2}

Fig. 6.33 presents line to line voltage (v_{AB}), phase voltage (v_{An}) and current (i_A) at primary side of transformer, when converter delivers 20% and 50% of full load. It is observed that line current distorted with increase in load. A phase shift of 60^0 is observed between line to line voltages (v_{bc}, v_{ef}) at secondary side of transformer because of the three-phase connections (Yd1 and Yd11). The experimental waveforms of $i_A, i_{A1} \& i_{D1}$ are shown in Fig. 6.33 and Fig. 6.36 which indicate that line currents i_{A1} & i_{D1} are distorted as compare to i_A. Fig. 6.35 presents simulation waveform of the primary side line current $(i_A, i_{A1} \& i_{D1})$ and its frequency spectrum, indicating total harmonic distortion. It is observed that current waveform of i_A contains 4.01% THD as compared to that of i_{A1} and i_{D1} (15.62%THD). Therefore, waveform of current i_A improved as compared to i_{A1} and i_{D1} over wide range of load. Fig. 6.36 presents secondary side line currents $(i_a, i_b \& i_c)$ and line to line voltages (v_{a1b1}, v_{d1e1}).



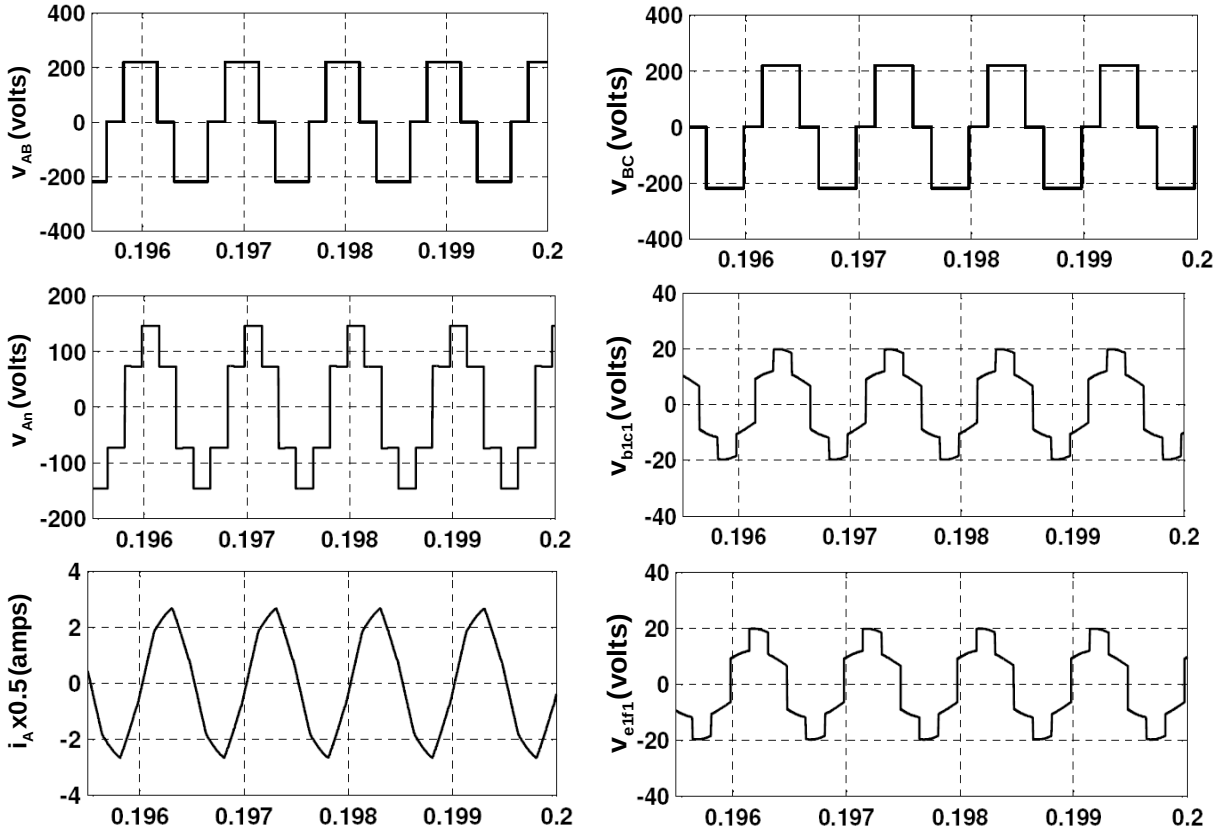
(a)



(b)

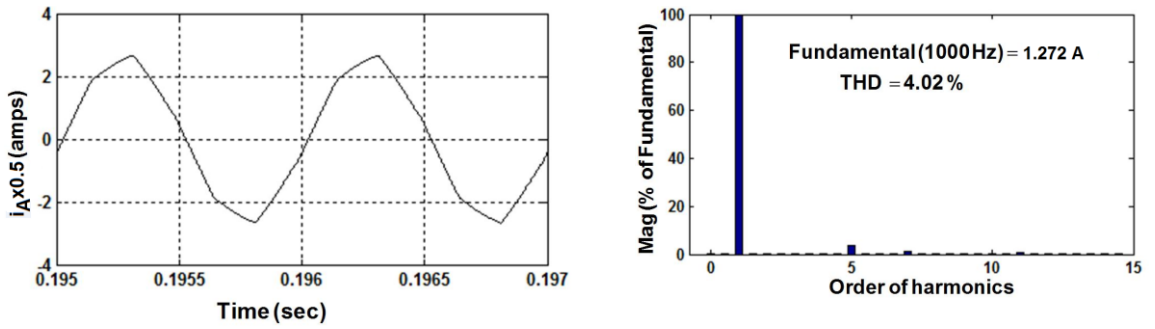
$(v_{AB}, v_{BC} \& v_{CA} : 200V/div, v_{An}, v_{Bn} \& v_{Cn} : 100V/div, i_A, i_{A1} \& i_{D1} : 2A/div, v_{bc} \& v_{ef} : 20V/div)$

Fig. 6.33 Voltage and current waveforms of primary side of transformer at (a) 20% load (b) 50% load

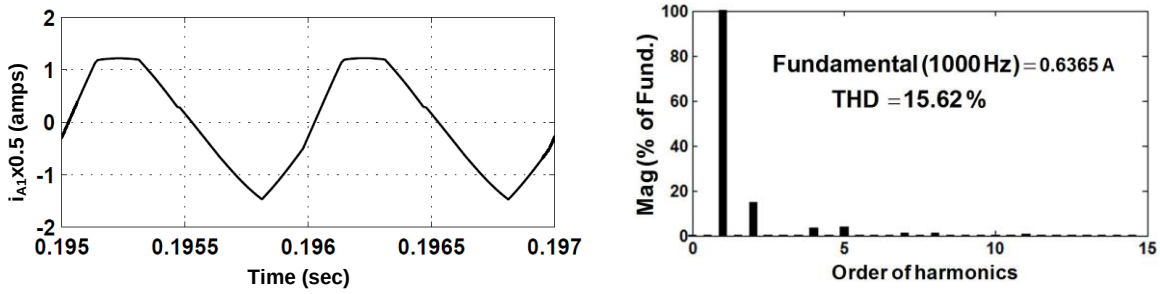


(a) (b)

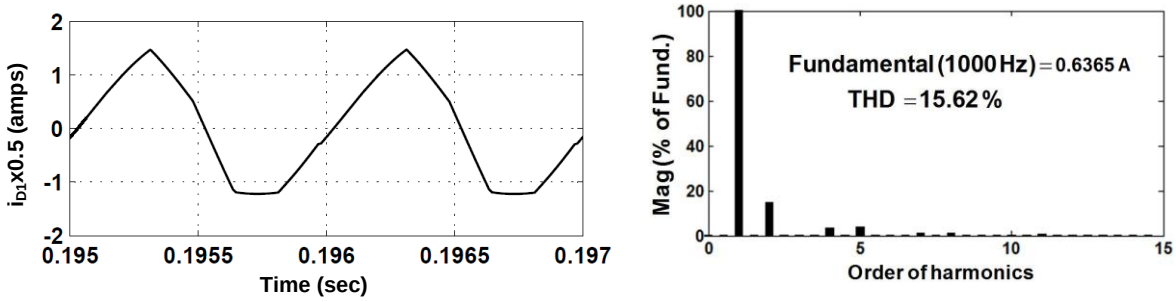
Fig. 6.34 Simulated voltage and current waveforms of primary side of transformer



(a)

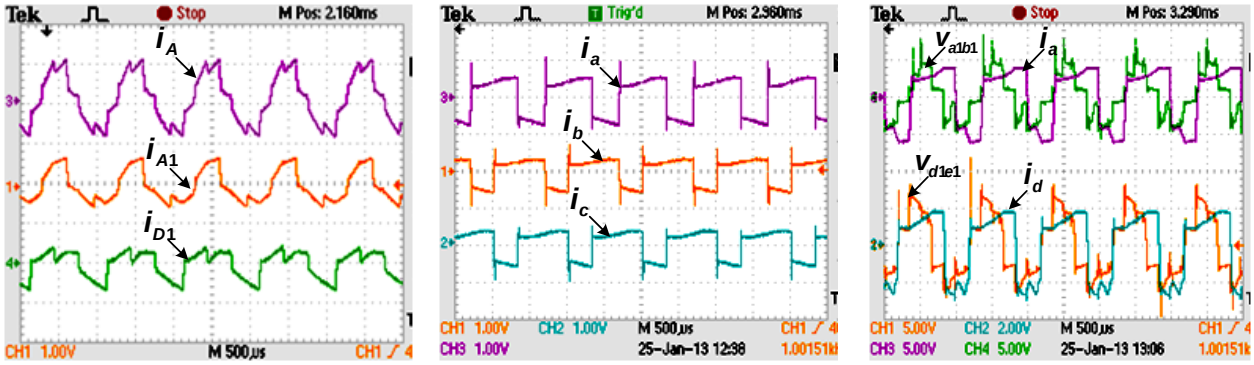


(b)



(c)

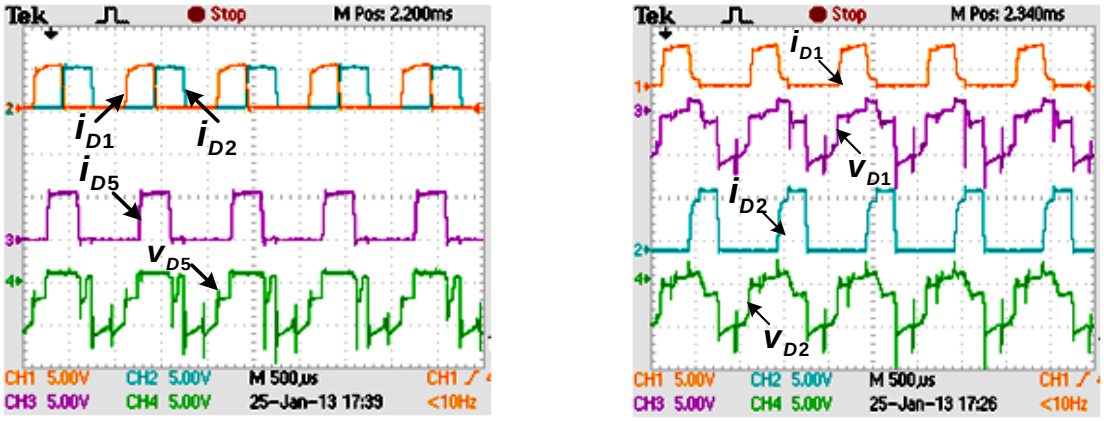
Fig. 6.35 Frequency spectrum of primary side current of transformers (a) i_A(b) i_{A1}(c) i_{D1}



$$(i_A, i_{A1} \& i_{D1} : 2A/div, i_a, i_b, i_c \& i_d : 8A/div, v_{a1b1} \& v_{d1e1} : 20V/div)$$

Fig. 6.36 Currents and voltage waveforms of primary and secondary windings of transformer

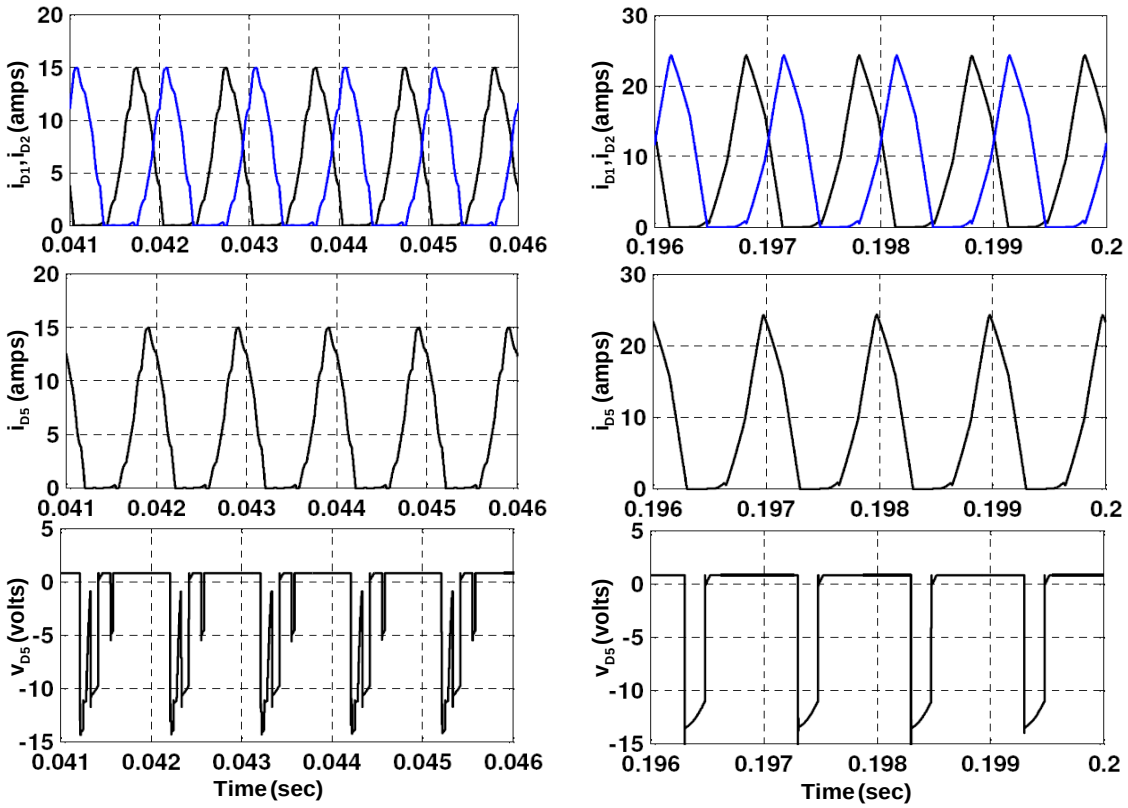
Fig. 6.37 and Fig. 6.38 present experimental and simulation waveforms of voltage and current of rectifier diodes. It is observed that average current though each diode reduces and better thermal heat management is acheived.



(a) (b)

$(v_{D1}, v_{D2} \& v_{D3} : 10V/div, i_{D1}, i_{D2} \& i_{D3} : 15A/div)$

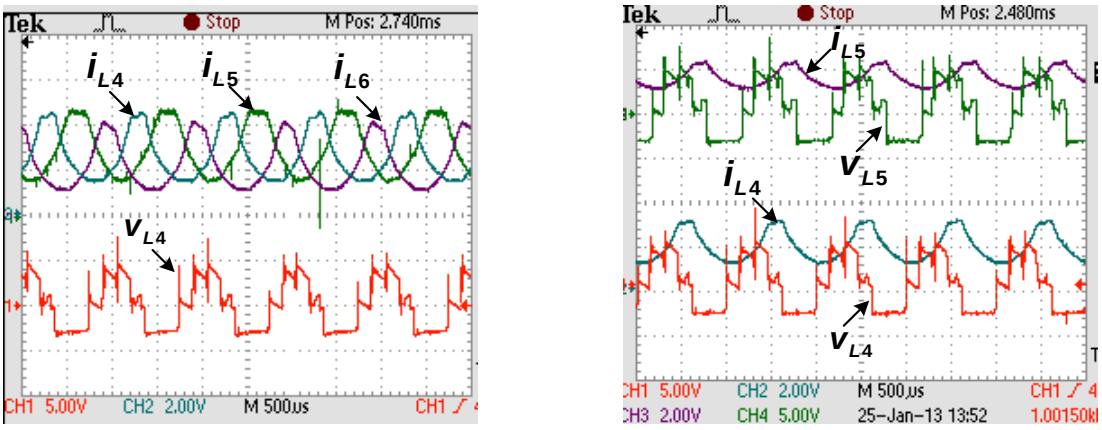
Fig. 6.37 Voltage and current waveforms of rectifier diodes



(a) 20% of Full load (b) 50% of Full load

Fig. 6.38 Simulated voltage and current waveforms of associated with rectifier diodes

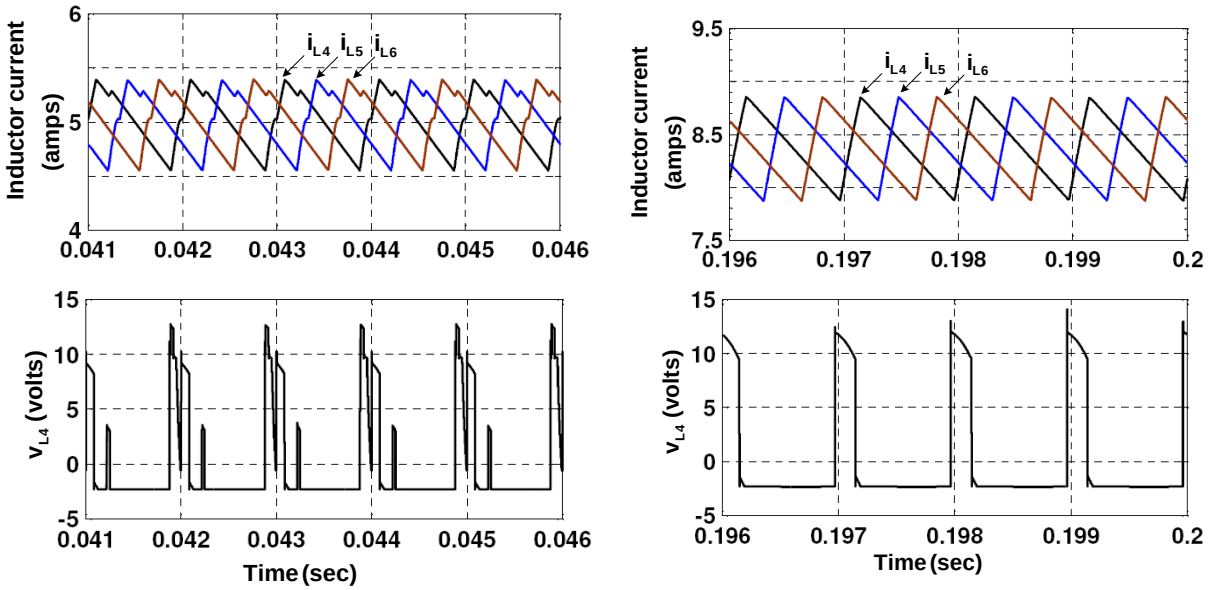
It is observed from Fig. 6.39 to Fig.6.41 that each inductor shares one sixth of load current and individual inductor current ripple is large, but due to equal phase shifted PWM control (i.e. interleaved operation), the ripple content in load current is considerably reduced. Therefore, size of output filter capacitor is reduced.



(a) (b)

$(v_{L4}\ \&\ v_{L5}: 10V/div, i_{L4}, i_{L5}\ \&\ i_{L6}: 8A/div, X-axis: 500\,\mu s/div)$

Fig. 6.39 Voltage and current waveforms of output filter inductors



(a) 20% of Full load (b) 50% of Full load

Fig. 6.40 Simulated voltage and current waveforms of output filter inductors

In order to investigate the sharing of current by each output inductor of proposed converter under transient conditions, input DC voltage is increased by 10% from its nominal value at $t = 0.1$sec and corresponding change in inductor currents are observed as shown in Fig.6.41(b). Furthermore, simulation results of inductor currents with respect to step increase in load current at $t = 0.15$sec is shown in Fig.6.41(c). It is observed that output inductors share equal current during steady-state and transient conditions.

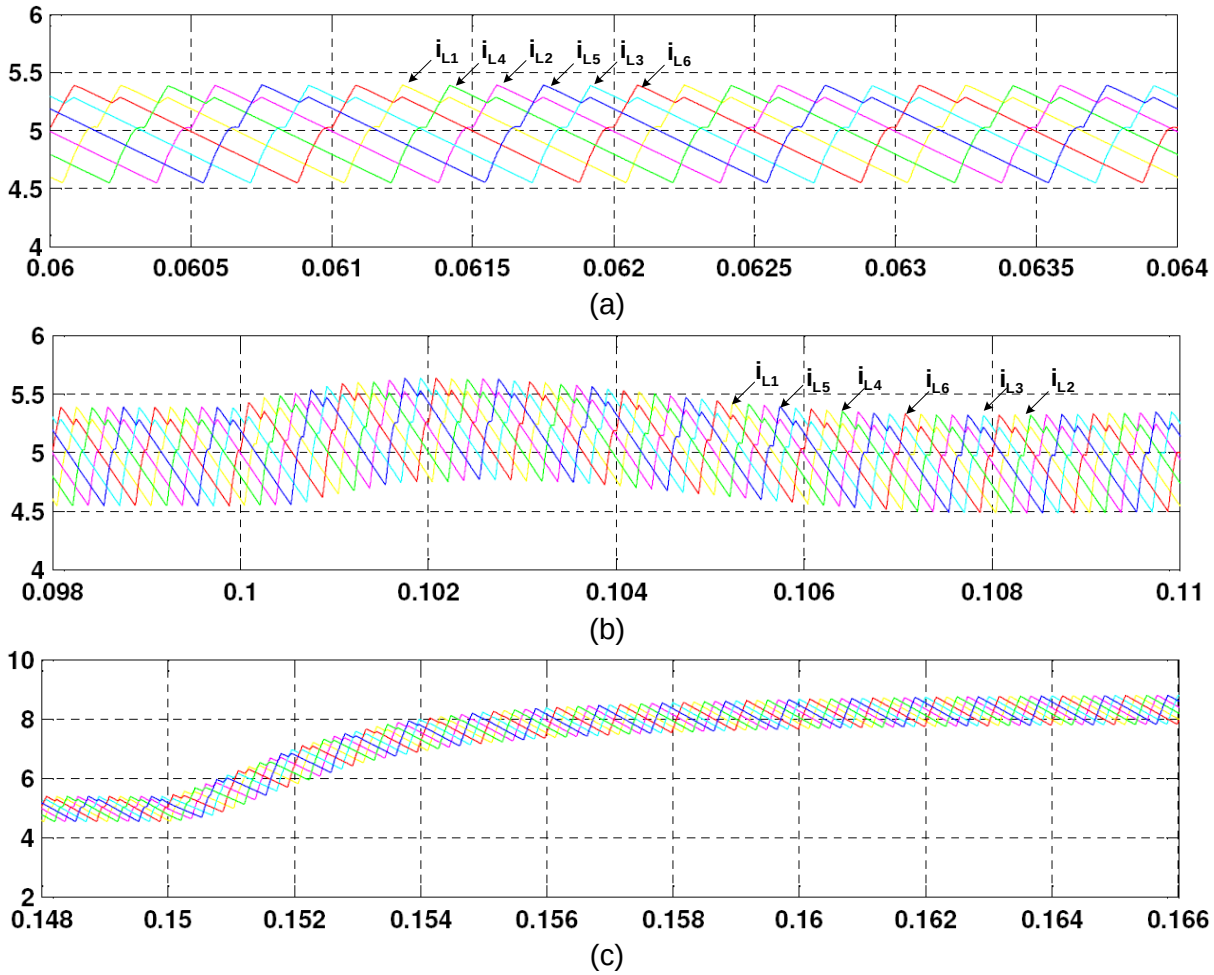


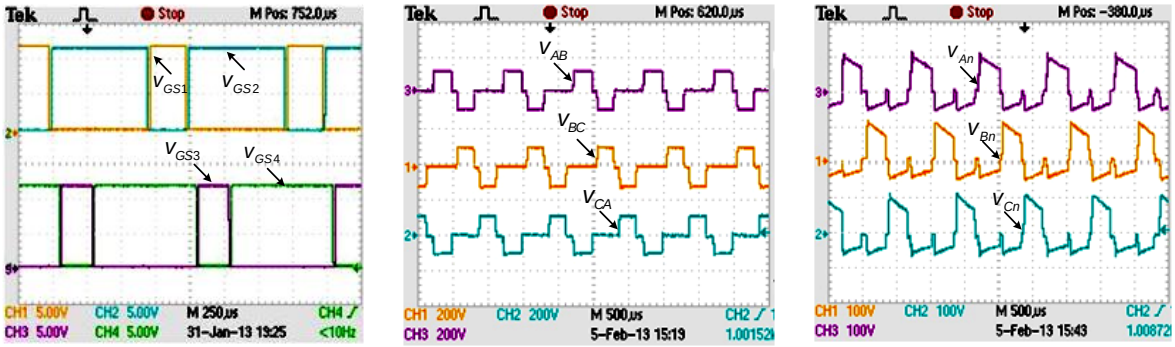
Fig.6.41 Output inductor current waveforms under different operating conditions

(a) Steady state; (b) 10% increase in input voltage at $t = 0.1\text{sec}$

(c) 30 % increase in load at instant $t = 0.15\,\text{sec}$

(b) Performance under asymmetrical control

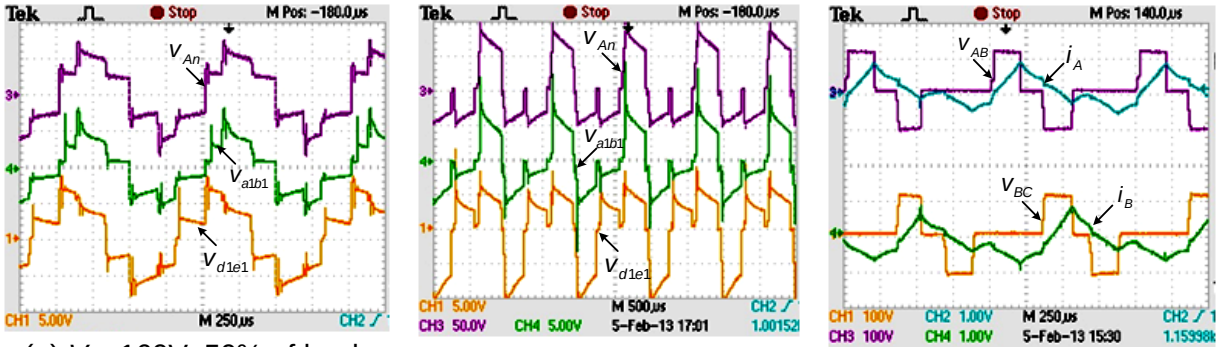
A prototype model of multi-phase high frequency isolated DC-DC converter is also tested under asymmetrical control method under various operating conditions. The experiment results obtained are shown in Fig. 6.42 to Fig. 6.44. The experimental results depicted in Fig. 6.42(a) shows the gate to source voltages of switching devices which indicate that switches of front end converter are operated in complimentary manner. Fig. 6.42(b) and Fig. 6.42(c) show the line to line voltage and phase voltage output of front end converter. Fig. 6.43(a) presents voltage appears across transformer windings, when converter operates in Reg2 with input voltage (160V,DC) and delivers 50% of full load. The secondary voltages $\left(v_{a1b1}, v_{d1f1}\right)$ are phase shifted by 60^0 as shown in Fig. 6.43(a) which indicates both three-phase trasnformers are connected in YD1 and YD11. As input voltage increased to 220V and load is reduced to 20% of load, then converter operation take place in Reg1 and obtained results for voltage appears across transformer windings are shown in Fig. 6.43(b).



(a) (b) (c)

$$(v_{GS}:5V/div, v_{AB}, v_{BC} \& v_{CA}:200V/div, v_{An}, v_{Bn} \& v_{Cn}:100V/div)$$

Fig. 6.42 Voltage and current waveforms of front end converter (a) v_{GS1},v_{GS2},v_{GS3} & v_{GS4}, (b)v_{AB}, v_{BC} & v_{CA} (c) v_{An},v_{Bn}, & v_{Cn}

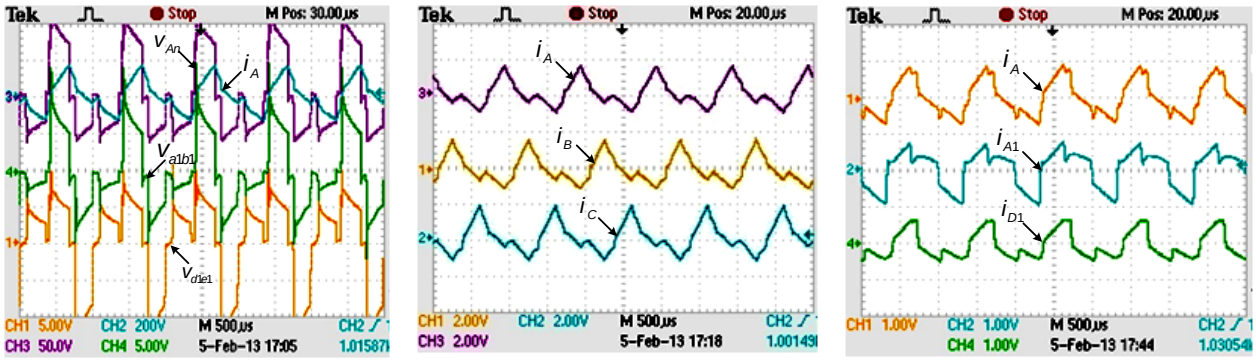


(a) V_{in}=160V, 50% of load (b) V_{in}=220V, 20% of load (c)

$$(v_{An}, v_{Bn} \& v_{Cn}:100V/div, i_A \& i_B:2A/div, v_{a1b1} \& v_{d1e1}:20V/div)$$

Fig. 6.43 Voltage and primary line current waveforms of transformer

Fig. 6.44 shows waveform of the primary side line currents $(i_A, i_{A1} \& i_{D1})$ which indicates that the improvement in current waveform of i_A as compare to i_{A1} and i_{D1} at light load. As load current increased to 50% of full load, the waveform of i_A get distorted.

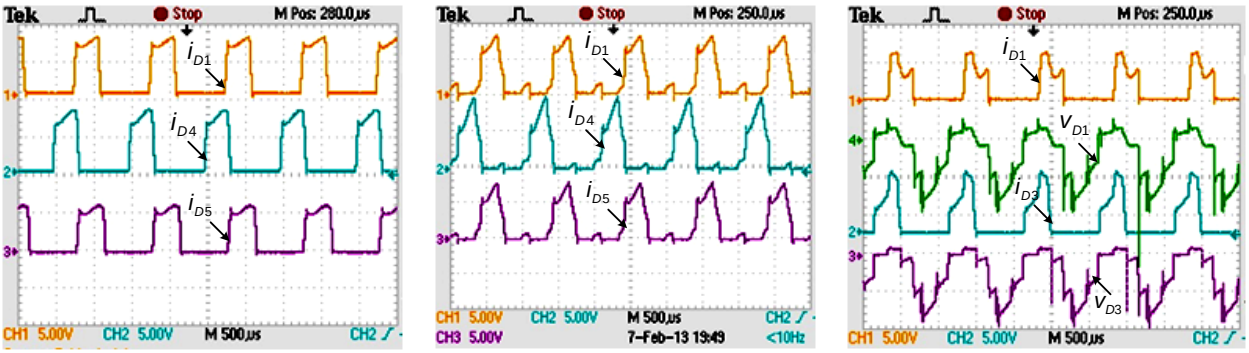


(a) @ V_{in}=120V (b) (c)

$$(v_{An}, v_{Bn} \& v_{Cn}:100V/div, i_A, i_B, i_C, i_{A1} \& i_{D1}:2A/div, v_{a1b1} \& v_{d1e1}:20V/div)$$

Fig. 6.44 Primary winding voltage and current waveforms of transformer

Fig. 6.45 shows the waveform of rectifier diodes, when converter delivers 50% load and 20%load with input voltage (V_{in} = 160V, DC). The variations in current waveform of rectifier diodes are shown in Fig. 6.45(a) and Fig. 6.45(b) are due to change in operating regions.

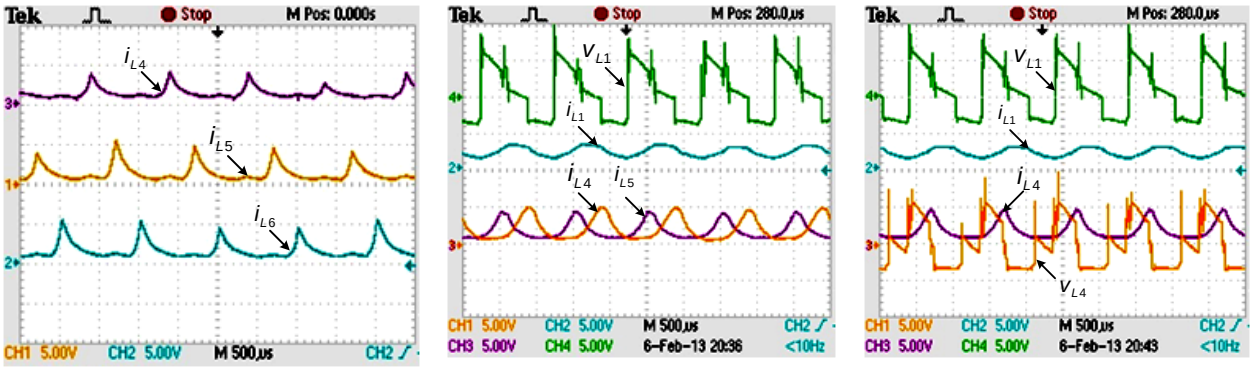


(a) @ 50% load (b) @ 20% load (c)

$$(v_{D1}, v_{D2} \& v_{D3} : 10V/div, i_{D1}, i_{D2} \& i_{D3} : 15A/div)$$

Fig. 6.45 Voltage and current waveforms of rectifier diodes $(D_1 - D_6)$

It is observed from Fig. 6.46 that each inductor shares one sixth of load current and individual inductor current ripple is large but due to phase shifted PWM control operation, the ripple content in load current is considerably reduced which is similar to operation of converter under symmetrical control method.



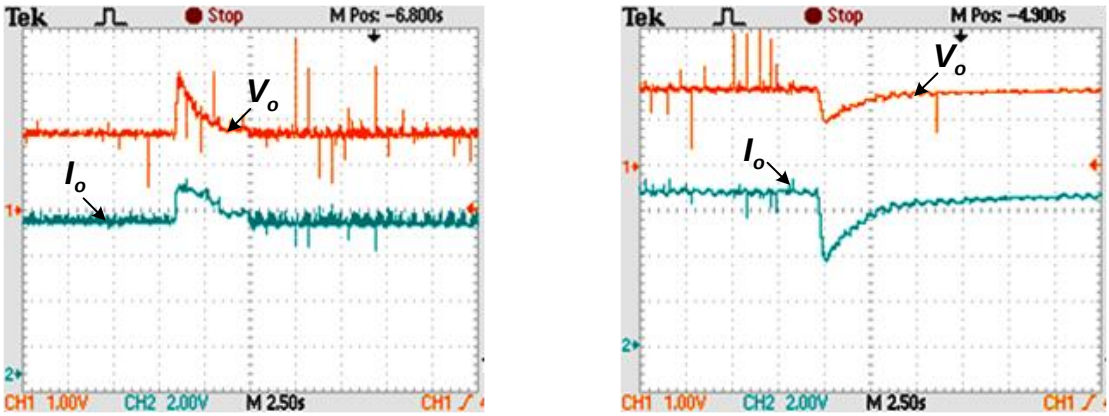
(a) (b) (c)

$$(v_{L4} \& v_{L5} : 10V/div, i_{L4}, i_{L5} \& i_{L6} : 10A/div, X - axis : 500\,\mu s/div)$$

Fig. 6.46 Voltage and current waveforms of output filter inductors $(L_1 - L_6)$

In order to investigate the performance of proposed converter under trasnent conditions, input voltage variations: 10% step increase and 10% step decrease from its nominal input voltage are introduced and corresponding variations in output voltage are shown in Fig. 6.47 and Fig. 6.48. It is observed that output voltage resumes its reference value i.e. $V_{ref} = 1.5V$ quickly after few disturbances from instant of disturbances being introduced. Furthermore, to study transient behaviour of converter against load variations, 40% increase in full load current and reduction of load current to 20% of full load current has

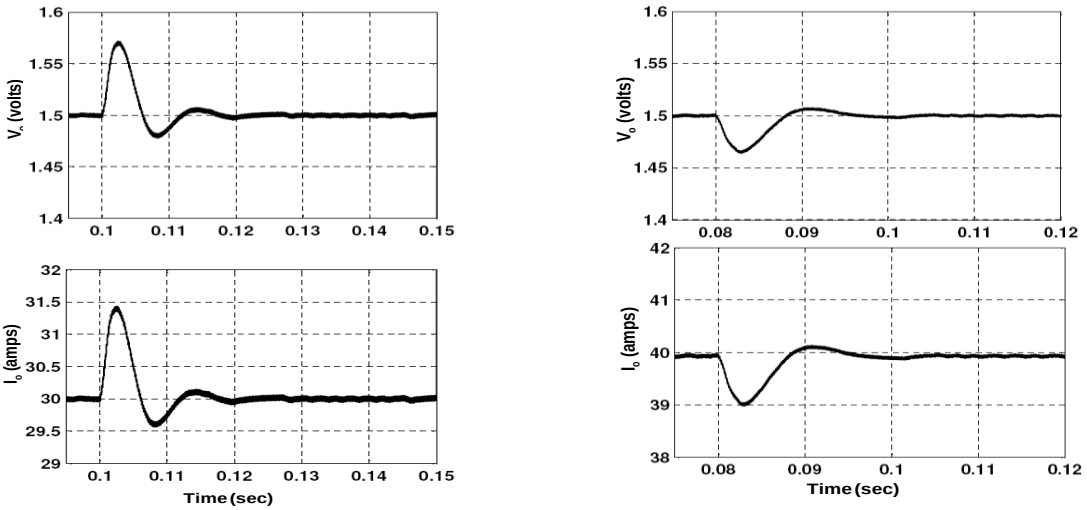
been done and obtained results are depicted in Fig. 6.49 and Fig. 6.50. It is summarized that converter exhibit improved dynamic response with respect to input DC voltage and load variations.



(a) (b)

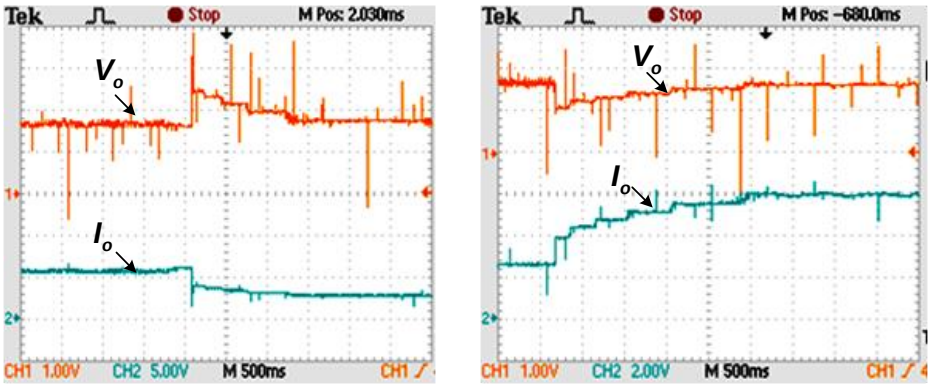
$(V_o : 1V/div, I_o : 8A/div)$

Fig. 6.47 Output voltage variation against input voltage perturbations (a) 10 % increase in V_{in} (b) 10 % decrease in V_{in}



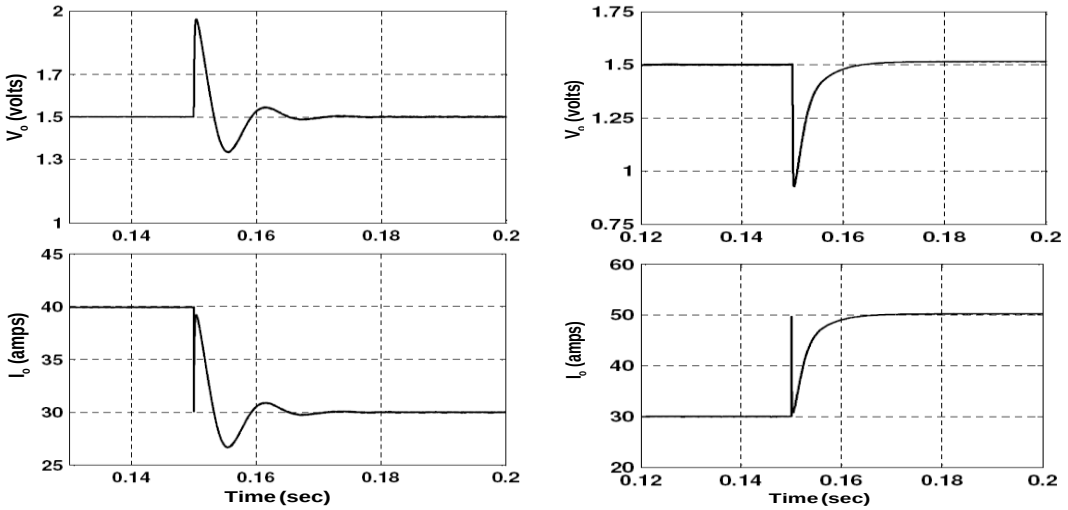
(a) (b)

Fig. 6.48 Simulated output voltage and load current waveforms against input voltage perturbations (a)10 % increase in V_{in} (b) 10 % decrease in V_{in}



(a) (b)

Fig. 6.49 Variations of output voltage against load perturbations (a) 20% decrease from nominal values (b) 40% increase from nominal load



(a) (b)

Fig. 6.50 Simulated output voltage and load current waveforms against load perturbations (a) 20% decrease from nominal values (b) 40% increase from nominal load

Table 6.2 Comparison of experimental and simulation results of proposed converter with different operating conditions

Parameter		25% of full load		50% of full load		100% of full load	
		Exp.	Simulation	Exp.	Simulation	Exp.	Simulation
Output voltage (volts)		1.5	1.5	1.5	1.5	1.5	1.5
Load current (amp)		25	25	50	50	-	100
Output Inductor current (amps)	I_{L1},I_{L4}	4.1	4.17	8.21	8.33	16.64	16.67
	I_{L2},I_{L5}	4.0	4.17	8.15	8.33	16.64	16.67
	I_{L3},I_{L6}	3.9	4.17	8.20	8.33	16.63	16.67
Rectifier diode current (amps)	I_{D1},I_{D4}	4.16	4.17	8.20	8.33	16.64	16.65
	I_{D2},I_{D5}	4.15	4.17	8.16	8.33	16.63	16.65
	I_{D3},I_{D6}	4.15	4.17	8.18	8.33	16.64	16.65
Settling time (sec)		-	0.020	-	0.02	-	0.02
% Rise/ Fall in V_o during change in V_{in} from 220V to 180V & vice-versa		-	6.67%	-	6.67%	44.44%	6.67%
Sampling time		30 µsec	1µsec	30 µ sec	1µsec	30 µ sec	1 µsec

6.7 Performance Comparison

The performance of multi-phase, high frequency isolated, DC-DC converter with reduced system hardware operating under symmetrical and asymmetrical PWM control methods are investigated. The simulation and experimental studies are carried out for comparison. Keeping in view of industrial requires of high power at relatively low voltage, the converter has to provide high output current and therefore, achieving high conversion efficiency is challenging task. The conduction interval, number of power devices in conduction and losses in different parts of the converter, mainly depend on type of control methods are to be employed and duty ratio of power switches.

The conduction period of each power switch of front end converter is same i.e. DT in symmetrical control method and that of DT for upper group and $(1-D)T$ for lower group in asymmetrical control like three-phase, high frequency isolated DC-DC converter discussed in chapter-5. This results in uniform heat distribution in power circuit with symmetrical control method. Therefore, thermal stress in power circuit is more in asymmetrical control methods as compare to symmetrical control method because of unequal conduction of swicthes.

In asymmetrical control method, switches of each leg of front end converter are operated in complementary manner. In order to implement in hardware, a deal band circuit for each device is required to avoid direct short circuiting of input DC voltage. This control method facilitates easy implementation of ZVS/ZCS as compared to symmetrical control method.

6.8 Conclusion

The following points are summarized from this chapter-

- The six-phase version of multi-phase high frequency isolated DC-DC converter with multi-phase rectification is suitable for industrial applications.
- In this converter switching legs of front end converter is reduced from six-legs to three-legs. The hardware components associated with front end converter such as number of switching legs, devices and driver circuits, switches losses in front end devices etc are reduced.
- In proposed converter, each rectifier diode and inductor carries 16.6A while delivering full load current of 100A. Thus, better current sharing at load end converter is achieved. The individual ripple current is 6.6% of full load.
- Simulation study of proposed converter is carried out under both control methods and the results are validated through prototype model of converter. The performance is also investigated under various operating conditions.

- Improvement in current waveforms is achieved at front end converter over wide range of load variations.
- With respect to input voltage and load variation, output DC voltage resumes its reference value (1.5V) within 1.5 sec which shows faster dynamic response.

CHAPTER 7: CONCLUSIONS AND FUTURE SCOPE OF RESEARCH

[The main conclusions of the presented work and possible research in future are summarised in this chapter.]

7.1 Conclusion

Low Voltage High Current DC power supplies are required in several applications such as electroplating, electrolysis, anodizing, metal refining, electronic welding, plasma torch applications, battery charging, electrical traction, telecommunication and computer industry where high voltage DC power is not applied due to system requirements. In this thesis, high frequency isolation based converters for low voltage high current power applications are proposed which have improved performances in terms of reduced size and weight, reduced losses, improved efficiency and dynamic response. Power conditioning in these LVHC power converters take place in two stages namely AC-DC and DC-DC conversion. Keeping in view the applications of low voltage high current power supply and the requirements associated with DC-DC conversion stage, modular approach based ISOP connected converter and multi-phase technology based converter are seen as viable alternative over exsiting methods for performance improvement.

In this thesis modular approach of designing DC-DC converter is proposed using input series-output parallel connection of multiple converters with interleaved control technique. In view of above, two identical modules of push-pull converters with their inter-connection in series at input and in parallel at output is simulated. In order to investigate the performance of the power supply, the effect of parasitic elements such as effective series resistance of capacitor and output filter inductors, leakage and magnetizing inductance of transformer are included and it is observed that ESRs of passive elements have major effect on dynamic response and load sharing. As two converter modules can not be identical and therefore to share equal power by each converter module, individual voltage and current controllers are employed. In addition to these controller, common voltage controller is also used to regulate output voltage against line and load variations. For simulation studied, 5V/100A Simulink model of proposed converter is developed using SimPowerSystem tool box of MATLAB and its performance is analyzed against line and load variations. A systematic development of a small-signal linear dynamic model of proposed converter is carried out using State-Space Averaging (SSA) technique. Transfer functions of different control blocks of converter are obtained. Small perturbation in duty cycle at different frequencies are introduced. It was observed that FFT of output voltage contains a low frequency component at modulating frequency. Furthermore, stability analysis of control loops is carried out to ensure closed loop operation.

The proposed topology can be extended to high power e.g. 5kW, 5V/1000A. Large number of small rating modules are connected in ISOP connection and to ensure equal power sharing, several controllers are to be needed. Therefore, due to more number of components & controllers, design of controllers becomes complex. It also reduces the system reliability.

Exhaustive simulation study is carried out to investigate the performance of single phase, isolated DC-DC converter and it's suitablity for low voltage high current applications. These converters experienced high stresses when employed for high power applications. Therefore, a three-phase high-frequency isolated LLC resonant DC-DC converter is proposed which is suitable for medium and high power applications. The design and modelling of proposed converter is carried out under symmetrical control with fixed frequency operation and its detailed steady state analysis is carried out for different operational stages of the converter. The parameters of the LLC resonant tank are derived from per phase model of the proposed converter and the modelling of LLC resonant tank network is carried out. Design curves of proposed converter are plotted against variation of normalized frequency for different value of the load. Based on the designed values of LLC resonant tank, the parameter of leakage and magnetizing inductances of transformers are adjusted. It is observed that leakage and magnetizing inductances of transformers along with snubber capacitances are sufficient to achieve ZVS for power switching device over a wide range of load variations.

In order to investigate the performance, the simulation study is carried out using the SimPowerSystem^{TM} and Simulink toolbox of MATLAB software. A prototype model rated for 1.5V/50A is built and tested under different operating condition and obtained experimental results are presented. It is observed that under symmetrical control method, all the power switches conduct uniformly unlike to asymmetrical control and hence thermal heat distribution improved. The size of reactive element can be reduced by employing ZVS condition for power devices. In view of high current at reduced voltage, the center-tapped rectifier based load end converter, carries high DC current and therefore secondary windings of centre-tapped transformers are designed for DC current rating equal to current rating of each rectifier diode which leads to complex design and high conduction losses in transformer.

Multi-phase high frequency isolated DC-DC converter with multi-phase load end converter is proposed and it's performance is investigated with fixed frequency, symmetrical and asymmetrical controlled phase shifted PWM control methods. For simulation studies, 5kW, 5V/1000A Simulink Model of three-phase high frequency isolated DC-DC converter with three-phase load end converter is developed using SimPowerSystem^{TM} and Simulink toolbox of MATLAB software. To investigate the performance of proposed converter, a

prototype model rated for 1.5V/50A is built and tested under different operating conditions and furthermore, simulation results of 1.5V/50A Simulink model are presented which are validated using prototype model. It is observed that under symmetrical control method, all the power switches of front end converter conduct uniformly unlike to asymmetrical control and hence better management of heat distribution is done. Although results of individual inductor current ripple are large, but ripple content in total inductor current is reduced significantly, due to ripple concealation effect and hence, size of output capacitor is reduced considerably. On the other hand converter operation with asymmetrical control method offers Zero Voltage Switching on front end converter over wide range of load variations.

In many industrial applications such as welding, plasma cutting, and surface hardening require high power at reduced DC voltage where the rating of LVHC power supply varies from few kilowatts to hundreds of kilowatts. Three-phase version of proposed converter may not be efficient because of high current stress on devices of load end converter and design of output filter inductors of high DC current are difficult. Therefore, to cater the need of aforementioned applications, multi-phase high frequency isolated DC-DC converter with reduced hardware of six-phase high frequency isolated DC-DC converter with six phase rectification is proposed. Performance comparison of multi-phase high frequency isolated DC-DC converter with multi-phase rectification is carried out with symmetrical and asymmetrical control method. In proposed converter, each rectifier diode and inductor carries 16.6A while delivering full load current of 100A under steady state condition. Thus, better current sharing at load end converter is achieved. Although individual ripple current is 6.6% of full load, but ripples in load current is reduced significantly. With respect to input voltage and load variation, output DC voltage resumes its reference value (1.5V) within 1.5 sec which shows faster dynamic response. Keeping in view of high power applications at reduced DC voltage, this converter offers reduced switches in front end converter, better magnetic core utilization, better sharing of load current and reduction in high current connections.

7.2 Future Scope of Research

Research is a continuous process. An end of a research project is led to start of several other avenues for future work. Following suggestions for further research in this area are summarized below:

- The operation and performance evaluation of the ISOP connected push-pull converter modules has to be experimentally verified.
- Further reduction in losses at rectification stage would be done by replacing Schottky rectifiers with synchronous rectifiers.
- Dynamic response may be further improved by employing mutual coupled output filter inductors.

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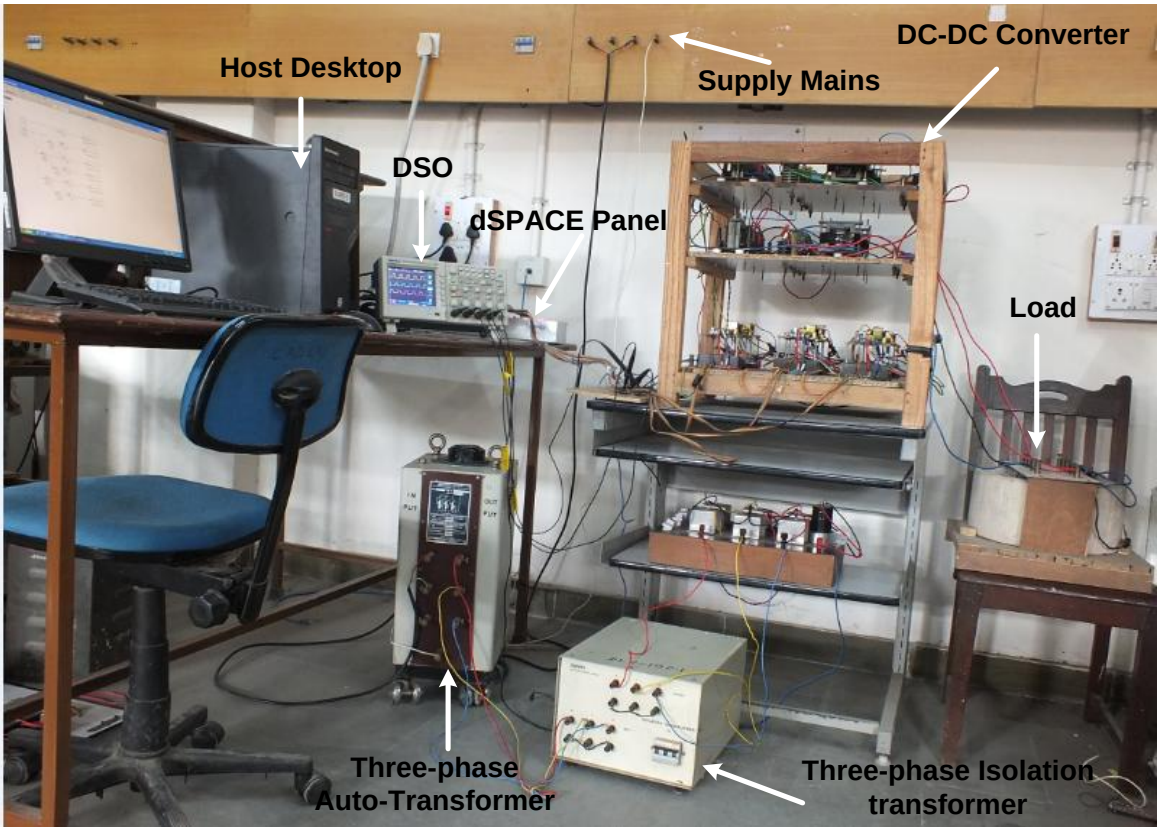

Fig.A.1 Experimental set-up

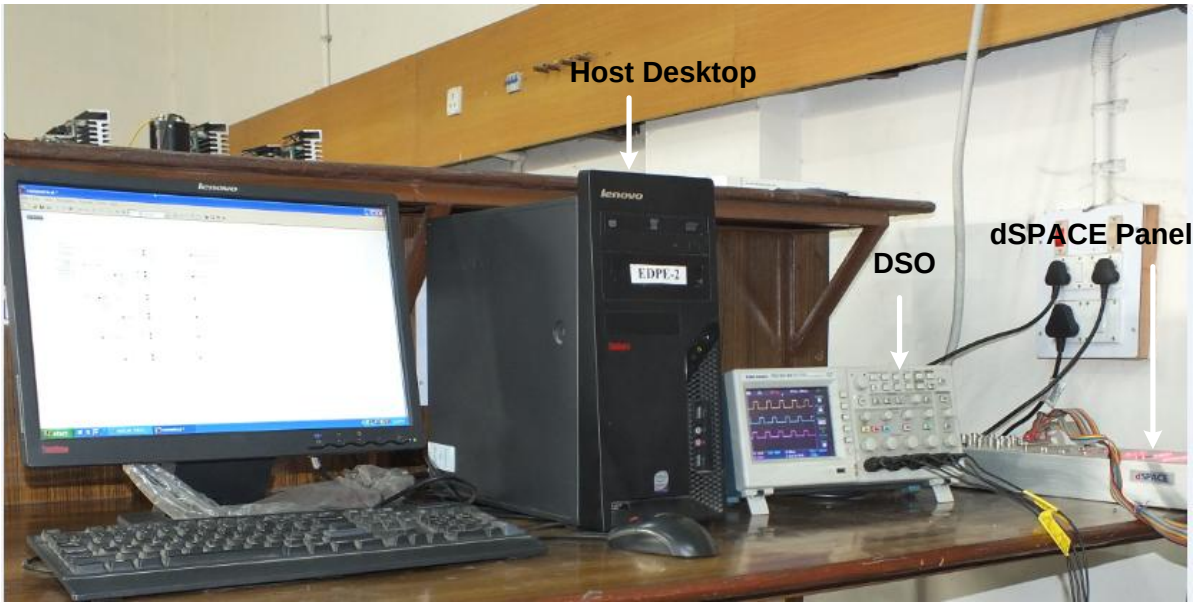

Fig.A.2 Host desktop with dSPACE panel

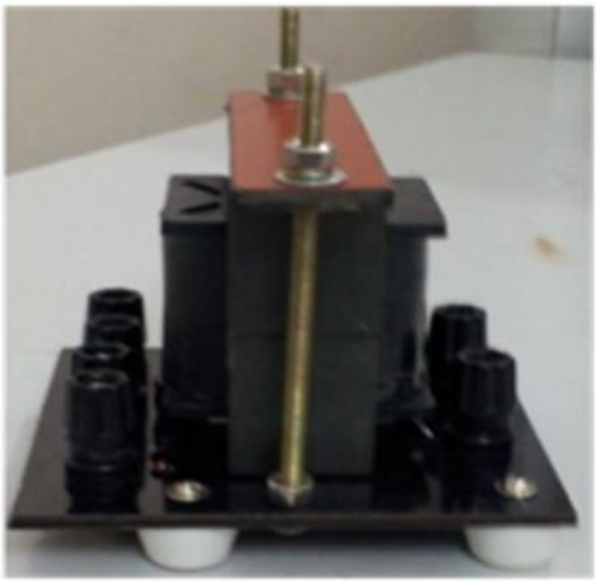

Fig.A.3 Fabricated high frequency transformer

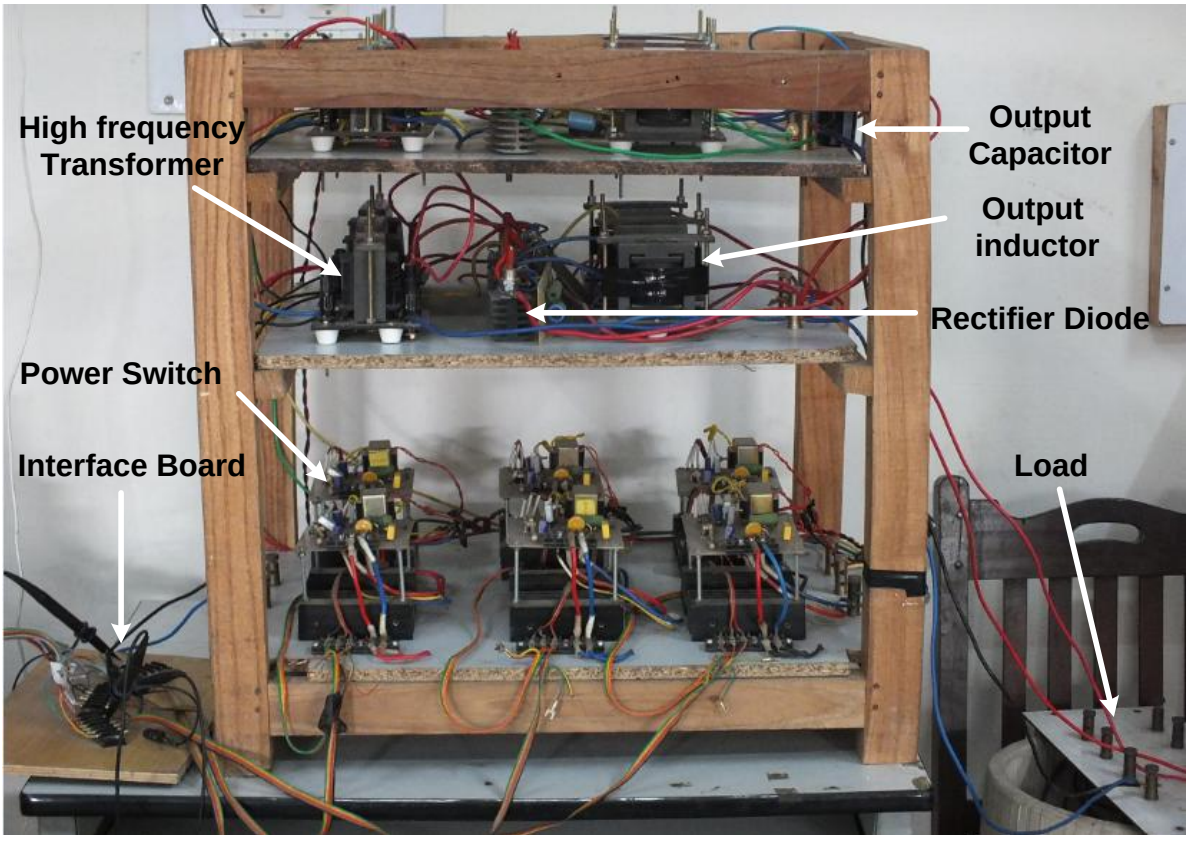

Fig.A.4 High frequency Isolated DC-DC converter

Nominal Diameter (mm)	Wire Size (SWG)	Outer Diameter (mm)	Resistance (Ω/ Km)	Area (mm^2)
0.025	50	0.036	34026	0.000506
0.030	49	0.041	23629	0.000729
0.041	48	0.051	13291	0.001297
0.051	47	0.064	8507	0.002027
0.061	46	0.074	5907	0.002919
0.071	45	0.086	4340	0.003973
0.081	44	0.097	3323	0.005189
0.091	43	0.109	2626	0.006567
0.102	42	0.119	2127	0.008107
0.112	41	0.132	1758	0.009810
0.122	40	0.142	1477	0.011675
0.132	39	0.152	1258	0.013701
0.152	38	0.175	942.5	0.018242
0.173	37	0.198	735.9	0.02343
0.193	36	0.218	589.1	0.02927
0.213	35	0.241	482.2	0.03575
0.234	34	0.264	402.0	0.04289
0.254	33	0.287	340.3	0.05067
0.274	32	0.307	291.7	0.05910
0.295	31	0.330	252.9	0.06818
0.315	30	0.351	221.3	0.07791
0.345	29	0.384	183.97	0.09372
0.376	28	0.417	155.34	0.1110
0.417	27	0.462	126.51	0.1363
0.457	26	0.505	105.02	0.1642
0.508	25	0.561	85.07	0.2027
0.559	24	0.612	70.30	0.2452
0.610	23	0.665	59.07	0.2919
0.711	22	0.770	43.40	0.3973
0.813	21	0.874	33.23	0.5189
0.914	20	0.978	26.26	0.6567
1.016	19	1.082	21.27	0.8107
1.219	18	1.293	17.768	1.167
1.422	17	1.501	10.850	1.589
1.626	16	1.709	8.307	2.075
1.829	15	1.920	6.564	2.627
2.032	13	2.129	5.317	3.243
2.337	12	2.441	4.020	4.289
2.946	11	3.068	2.529	6.818
3.251	10	3.383	2.077	8.302
3.658	9	3.800	1.640	10.51
4.064	8	4.219	1.329	12.97