DUAL-*k* SPACER ENGINEERED DEVICES FOR HIGH PERFORMANCE DIGITAL CIRCUIT/SRAM APPLICATIONS

Ph.D. THESIS

by

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **"DUAL-*k* SPACER ENGINEERED DEVICES FOR HIGH PERFORMANCE DIGITAL CIRCUIT/SRAM APPLICATIONS"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electronics and Communication Engineering of the Indian Institute of Technology Roorkee is an authentic record of my own work carried out during a period from July, 2011 to November, 2015 under the supervision of Dr. S. Dasgupta, Associate Professor and Dr. B. K. Kaushik, Associate Professor, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(PANKAJ KUMAR PAL)

This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

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Date: 20th Nov. 2015

ABSTRACT

FinFET technology has emerged as a major milestone in the field of nano-electronics after the announcement by leading semiconductor industry to use the tri-gate transistors commercially in the 22 nm technology node. In order to keep pace with Intel and TSMC, 10 nm and 14 nm FinFET process nodes are rapidly emerging as preferred choice amongst other semiconductor industries/foundries in near future. However, similar to the problems faced by any new technology, FinFET with sub-20 nm feature size also faces several design challenges. Most of these challenges arise due to technological restriction that can deteriorate the short channel characteristics. This necessitates the use of undoped underlap regions that otherwise increases the channel resistance and reduces the drive current. In the past decade, high permittivity (*k*) spacer materials act as key enabler in enhancing the device performance that provides strong field coupling between the gate and the undoped underlap region and hence reduces the raised source/drain series resistance. However, it has limited applicability in high-performance circuit/SRAM applications. The limitations are imposed due to exorbitant increase in fringe capacitance that in turn worsens the dynamic performance. The other two inherent challenges associated with FinFET are higher magnitude of parasitic (due to its 3D nature) and fin width quantization. Therefore, the digital circuit designers need to adapt their designs taking into account these critical issues so as to improve overall performance in terms of device/circuit parameters such as I_{ON}, I_{OFF}, noise-immunity, and the switching speed etc. Process variability has emerged as one of the major concern in sub-20 nm gate lengths. The random variability in device increases sharply with reduced feature size that can fail out any design both in digital as well as analog domain. Therefore, it is necessary to thoroughly investigate novel device architectures with their circuit/SRAM suitability and tolerance to random statistical variations.

In this thesis, we primarily focus towards the novel device architecture abbreviated as dual-*k* spacer FinFET that intelligently uses the high permittivity spacer targeting for high-performance device-circuit co-design and its immunity to random statistical and structural variations. The dual-permittivity spacer concept and the optimization strategy are presented for the tri-gate FinFET device under study. We

also describe the proposed symmetric and asymmetric dual-*k* architectures, their fabrication methodology and superior ON- and OFF-state electrostatics over the conventional (single/low-*k* spacer) as well as the purely high-*k* spacer underlap FinFET structure. It is observed that the carrier concentration increases with an increase in the inner high-*k* spacer length (L_{hk}) till it reaches an optimum value. Beyond this optimum point, the fringing-field lines do not affect much the laterally diffused S/D region that already has very high carrier concentration. Therefore, there is no need to place high-*k* spacers above the highly doped laterally diffused area that may otherwise lead to higher parasitic capacitances. Consequently, beyond an optimal L_{hk}, the device performance starts degrading. The difference in spacer permittivity at high-*k*/low-*k* interface region changes the electric field path that results in better electrostatics in both ON and OFF-state. We also physically interpret the ON/OFF state electrostatics associated with dual-*k* structure with an increase in inner spacer *k* value. From this, an important observation is made that the conduction band energy barrier (in ON-state) directly under the gate is significantly affected in proposed dual-*k* architectures which otherwise remains same in purely high-*k* device even though the inner spacer permittivity is increased substantially. In addition, a detailed TCAD comparative analysis between symmetric and asymmetric architectures is demonstrated that clearly presents the competing effects of high permittivity spaces on device electrostatics. It is observed from the obtained results that the source side spacer mainly governs the charge transport from source to drain, however, the drain side spacer helps to enhance the current magnitude.

We also comprehensively study the role of fringe capacitances associated with proposed dual-*k* architectures that demonstrates the suitability of high-*k* spacer materials for improving noise-margin and delay performances, simultaneously. Although, the dual-*k* structures also exhibits larger fringe capacitances in comparison to conventional FinFET, but with an optimized inner spacer length, the proposed SymD-*k* and AsymD-*k*S architectures shows better inverter/RO3 delay performances. This superior delay performance is due to the increased gate-to-source capacitance component. On the other hand, the inverter delay worsens in AsymD-*k*D device because of the high value of Miller capacitance. For AsymD-*k*S and SymD-*k* architectures, it is observed that the gate-to-source capacitance increases sharply up to an optimum point and thereafter decreases marginally. However, for AsymD-*k*D

architecture, it remains low and almost constant. Moreover, an important and novel observation is made that the delay performance improvement is more pronounced with higher permittivity of the spacers in dual-*k* spacer technology that otherwise worsen in case of purely high-*k* architectures.

Motivated by the superior device/circuit electrostatics, we further explore the possibility of proposed symmetric and asymmetric dual-*k* architectures for augmenting the SRAM design metrics such as SNM, read/write access time, and the total leakage power. Furthermore, we investigate the tolerance of symmetric and asymmetric dual-*k* spacer architectures and its SRAM performance by random statistical and structural parametric variations. In addition to the superior device electrostatics and better static/dynamic circuit performance, it is observed that both the symmetric and asymmetric dual-*k* tri-gate FinFET structures also exhibits better device and circuit immunity to random variations and lesser sensitivity to key structural parameters in comparison to the conventional FinFET based circuits.

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ABBREVIATIONS AND SYMBOLS

2D	two-dimensional
3D	three-dimensional
6T	six-transistors
AsymD-*k*	asymmetric dual-*k* structure either at source or drain side
AsymD-*k*D	asymmetric dual-*k* at drain-side only
AsymD-*k*S	asymmetric dual-*k* at source-side only
BL	bit-line
BLB	bit-line bar/complement
BOX	buried oxide layer
BTBT	band-to-band tunneling current
CBE	conduction band energy
C_{fr}	total fringe capacitance
C_{GC}	gate-to-channel capacitance
C_{GD}	gate-to-drain capacitance
C_{GG}	total gate capacitance
C_{GS}	gate-to-source capacitance
C_{if}	inner fringe capacitance
CMOS	complementary metal oxide semiconductor
C_{of}	outer fringe capacitance
CR	cell-ratio
DG	double-gate
DIBL	drain induced barrier lowering
DSDT	direct source-to-drain tunneling current
DSL	dopant segregation length
eDensity	electron-density
EOT	equivalent oxide thickness
ETSOI	extremely thin-film SOI
eV	electron volt
FDSOI	fully-depleted SOI

FET	field effect transistor
FinFET	fin- field effect transistor
GAA	gate-all-around
G-S/D	gate to source/drain
H_{fin}	fin height
HP	high-performance
IC	integrated chips
I_{EDT}	edge direct tunneling current
$I_{EDT\text{-}OFF}$	edge direct tunneling current at (V_{GS}=0, V_{DS}= V_{DD})
$I_{EDT\text{-}ON}$	edge direct tunneling current at (V_{GS}=V_{DD}, V_{DS}=0)
IFM	impedance field method
IG	independent-gate
I_G	total gate tunneling current
$I_{G,ON}$	ON-state gate tunneling current
I_{GC}	gate-to-channel tunneling current
$I_{G\text{-}OFF}$	OFF-state gate tunneling current
I_{OFF}	total leakage current
I_{ON}	drive current/ON-state current
I_{SUB}	sub-threshold current
ITRS	International technology roadmap for semiconductors
k	dielectric permittivity
L_{eff}	effective channel length
L_{EXT}	gate edge to source/drain extension length
L_G	physical gate length
L_{hk}	inner high-k spacer length
L_{lk}	outer low-k spacer length
L_{un}	undoped underlap length
MOSFET	metal oxide semiconductor field-effect transistor
N_A	acceptor concentration
N_D	donor concentration
NM	noise-margin of an inverter

NMOS	*n*-channel MOSFET
PA_L, PA_R	access-transistors (left and right) in 6T SRAM cell
PD_L, PD_R	pull-down transistors (left and right) in 6T SRAM cell
PMOS	*p*-channel MOSFET
PR	pull-up ratio
PU_L, PU_R	pull-up transistors (left and right) in 6t sram cell
RDF	random dopant fluctuations
RO3	three-stage ring-oscillator
$R_{S/D}$	total source/drain series resistance
SG	shorted-gate
SINM	static current noise margin
SNM	static noise margin
SOI	silicon-on-insulator
SPNM	static power noise margin
SRAM	static random access memory
SS	subthreshold-slope
SVNM	static voltage noise margin
SymD-*k*	symmetric dual-*k* spacer architecture
T	time-period of the oscillations
TCAD	technology computer-aided design
T_{fin}	fin thickness
T_G	gate-electrode thickness
TG	tied-gate
T_{hk}	high-*k* gate dielectric thickness
TOX	oxide roughness variations
TSMC	Taiwan semiconductor manufacturing company
V_{DD}	supply voltage
V_{DS}	voltage difference between gate and drain terminal
V_{GS}	voltage difference between gate and source terminal
VTC	voltage transfer characteristics
V_{th}	threshold voltage

W	total width of FinFET
WFV	Metal-grain oriented work-function variations
WL	word-line
WTI	write-trip current
WTP	write-trip power
WTV	write-trip voltage
σ_{L}	segregation length
σ	standard deviation

CHAPTER 1

Introduction

1.1 Introduction

Eversince the first integrated chip (IC) [KilbJ'64] and the complementary MOS technology [WanlF'67] were demonstrated in 1958 and 1963, respectively, the aggressive downscaling has continued that has actually fuelled the rapid growth of micro/nano-electronics industries. In April 1965, Gordon Moore predicted that the number of transistors in an IC would double and the manufacturing cost would be reduced by half in every one and half years [MoorG'65]. This trend had set a baseline for International Technology Roadmap for Semiconductors (ITRS) to discover or manufacture smaller and faster transistors that enable the inventions of countless novel applications available to the community such as high speed microprocessors and compact mobile phones (Fig. 1.1).

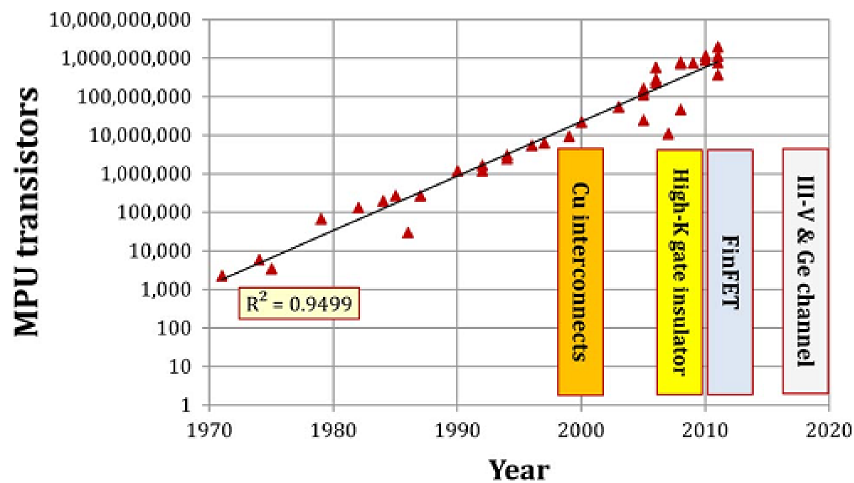


Figure 1.1. The number of transistors per microprocessor chip *vs.* time [CaviR'12].

This chapter introduces the work carried out in this thesis. Section 1.2 describes the background and motivation behind the research work carried out. Section 1.3 presents the brief history of FinFET and its merits/demerits. Section 1.4 discusses some of the major challenges and issues faced by FinFET in designing digital circuit/SRAM. Further, section 1.5 deals with the problem statement and section 1.6 present the outline of this thesis. Finally, a brief summary of this chapter is drawn in section 1.7.

1.2 Background and Motivation

After Moore's prediction, the microelectronic devices have evolved rapidly in terms of size, cost and performance. The advances in the development of microelectronic materials and device architectures in the past few years have ushered a new era of devices and circuits. While some of these new technologies are still in the developmental stages, many of them are on the way to become mainstream workhorses for the coming few years. Current physical gate length of transistors used in high performance integrated circuits are around 22 nm [ShorJ'12] and will possibly go further down to 7-10 nm by mid of 2017, according to projections made in recent ITRS trends [ITRS]. However, there are numerous challenges ahead for the semiconductor industries in its effort to track Moore's law beyond the sub-20 nm nodes. The main challenges in this regime are twofold: (a) reduction of leakage currents, and (b) reduction in device variability to increase the yield [XionW'02].

1.2.1 Scaling and its Challenges

Reducing the device dimensions not only results in a higher packing density but also lead to faster switching speed, lower power consumption and lower manufacturing cost. Therefore in 1974, Dennard *et al.* [DennR'74] reported the constant field scaling method to shrink the structural parameters of a device (horizontally as well as vertically) by a constant factor. However, as the gate length is shortened to enhance the operating speed and the chip density, the so-called short-channel effect (SCE) arises. Therefore, the scaling is limited by various physical/electrical parameters such as V_{th} roll-off, drain induced barrier lowering (DIBL), velocity saturation, and sub-threshold swing (SS) degradation, etc. [TaurY'09]. These effects have started plaguing the device characteristics mainly because of the reduced gate electrostatic control over the channel.

In general, a MOS transistor is said to be short channel device when the effective channel length is comparable to the sum of the source/drain junction depletion-layer widths [TsucT'98]. In short channel MOSFETs, the electric-field lines that originate from the source/drain regions strongly influence the channel potential and govern the barrier [NguyT'81]. Ideally, the barrier was controlled by the applied gate field. To enhance the gate control over the channel, the gate dielectric layer must be made thinner and channel doping must be increased as suggested by the classical scaling

rules [DennR'74]. Although, this approach has been followed over the decades, but in recent years this has given rise to a series of undesirable effects such as higher parasitic, increased gate tunnelling current, mobility degradation, and random statistical variations such as RDF.

When the gate oxide thickness is reduced below 2-3 nm, the gate direct tunnelling current increases exponentially and therefore increases the standby power dissipation. In sub-100 nm technology nodes, the gate oxide thickness has been reduced to the point where the power dissipated due to gate leakages is equivalent to the power for switching the circuit [KimN'03]. Moreover, in highly doped MOSFETs, the existence of large number of dopant ions obstructs the carrier motion because of Coulomb scattering and hence the mobility degrades [KittC'76]. Additionally, higher channel doping increases the surface electric field for a given inversion level which results in reduced carrier mobility due to surface scattering [TakaS'94]. The high surface electric field confines the carriers in a narrow potential well resulting in quantum confinement effects [SterF'67]. Further, a high gate oxide field depletes the poly-silicon gate with appreciable amount of potential drop thus reducing the effective gate bias [LuCY'89]. Quantum confinement [TaurY'09, VasiD'97] and poly-silicon depletion [ArorN'95] leads to a threshold voltage shift and decreases the overall gate capacitance. On the other hand, the random dopant fluctuation (RDF) originates due to the discrete dopant ions in the channel region. This effect is more prominent at smaller geometry because the total numbers of dopant ions are very small that results in large statistical fluctuations. RDF also alters the transistor properties, especially threshold voltage and drive current [AsenA'98]. High body doping increases the electric field in the reverse biased source/drain-to-body junction which significantly enhances the junction band-to-band tunnelling (BTBT) current [TaurY'97b].

1.2.2 Multi-gate FETs and its Advantages

In order to improve the short-channel characteristics in classical devices, several methods such as super-steep retrograde profile [JacoJ'95], source/drain extension region, halo implants [TomiT'09] and so on were suggested. In an aggressively scaled MOS architecture, the S/D-to-bulk capacitances are becoming a major issue that can be significantly minimized using SOI (silicon-on-insulator) technology. In extremely-thin SOI (ETSOI) platforms, [also called as fully-depleted SOI (FDSOI) or ultra-thin body (UTB) SOI] the gate control over the channel is significantly enhanced in

comparison to the planar bulk technology. It is primarily due to thinner silicon film (T_{fin}) than the channel depletion depth. However, the use of SOI as an alternative to bulk technology remained confined only to the specific sectors and applications. The majority of the commercial market uses bulk process, championed by the foundries, including Intel, TSMC, UMC and GlobalFoundries. An alternative way to improve the gate electrostatic control, various multi-gate architectures can be used such as double-gate, FinFET, Si-nanowire and gate-all-around and so on. Such architectures can be implemented on SOI and bulk substrate as well.

Recently, multi-gate FETs are seen as a better alternative for pushing the CMOS scaling under sub-20 nm gate lengths [FranD'01]. The primary advantage of the multi-gate MOSFET is the excellent control of SCEs [ColiJ’08, HaenW'06] without relying on channel doping that makes it potentially scalable to the end of the ITRS roadmap. Having more than one gate around the channel improves the electrostatic integrity (EI) that is the measure of electric field lines originated from the source/drain and influencing the channel region. Various flavours of alternative device structures having multiple gates have been proposed to replace the classical planar MOSFET and extend the channel length scalability into the sub-22 nm regime.

1.3 Evolution of Double/Tri-gate FinFETs

Among the multi-gate architectures, double-gate/tri-gate FinFET have been proven to be a strong candidate for the future CMOS technology [KuhnK'11]. Therefore, Intel already started its production at 22 and 14 nm technology nodes as shown in Fig. 1.2 [AuthC'12].

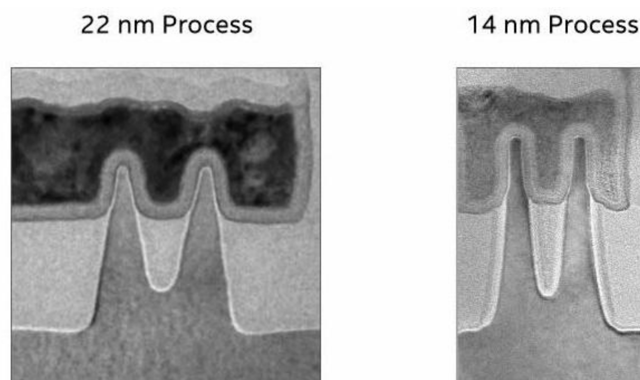


Figure 1.2. Microscopic images of Intel’s tri-gate FinFET design for 22 and 14 nm process nodes.

The concept of the first planar double-gate transistor evolved in the late 80s by Balestra *et al.* [BaleF’87] and Hisamoto *et al.* [HisaD'91]. Besides the advantage of

doubling the drive current by the presence of two channels, additional interest existed in the possibility of volume inversion for thin-film devices. In volume inversion, the charge carriers are concentrated in the middle of the channel instead of SiO_2/Si interfaces and this can be modulated by the front and back gate voltages [ColiJ'90]. Although, the concept of the planar double-gate transistor appeared very promising, but it was very challenging to fabricate such devices with perfectly aligned front and back gates. Early success was achieved by the gate-all-around (GAA) transistors [SimoE'95]. But the main breakthrough of the double-gate transistors came in 1999, with the concept of the self aligned FinFET. In this technology, the planar arrangement was abandoned for a vertical one and the top channel was replaced by two sidewall channels, wrapped around a silicon fin as shown in Fig. 1.3 [HisaD'00, KedzJ'01, ChoiY'02a].

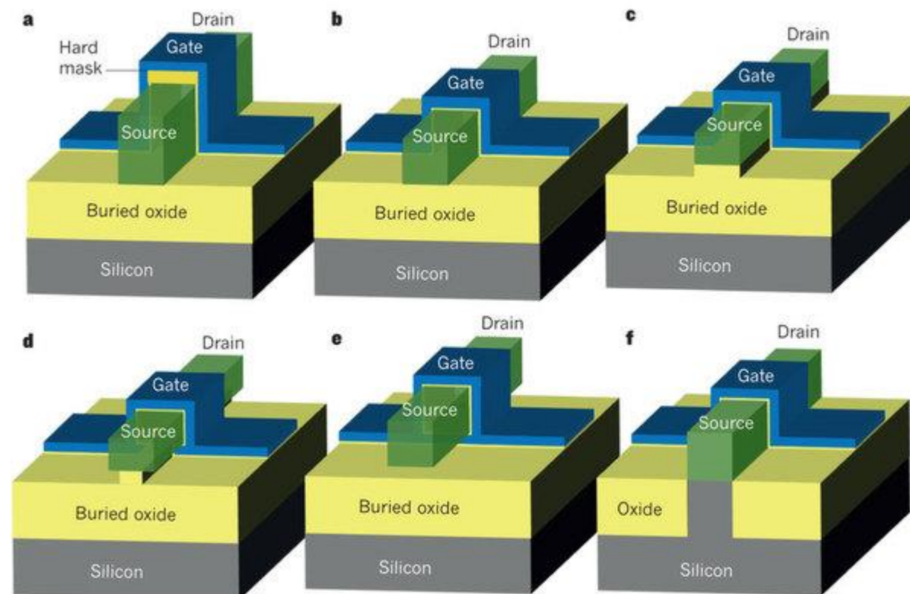


Figure 1.3. Various versions of FinFET structures: (a) double-gate SOI FinFET, (b) tri-gate SOI FinFET, (c) π-gate, (d) Ω-gate, (e) quadruple-gate/gate-all-around, and (f) tri-gate bulk FinFET.

FinFET offer increased immunity to small-geometry effects, a near-ideal subthreshold slope, and certain other advantages like the increased mobility associated with lightly doped channel. Lower doping results in less electric field that further reduces the surface carrier scattering and gate tunnelling. The use of an undoped or lightly doped body also provides immunity to threshold voltage and drive current variation due to statistical dopant fluctuations. For planar MOSFETs, the high substrate doping that used to control the SCEs also enabled threshold voltage adjustment. However, the freedom of threshold voltage adjustment was lost in case of

FinFET due to the absence of channel doping. In FinFET, the required V_{th} was usually set by using tuneable work-function metal gate [LiuY'06]. The undoped/lightly-doped channel increases the carrier mobility due to reduced Coulomb scattering. Thus, the FinFET architectures offer the potential for maintaining the scalability of the CMOS technology as it approaches the “end of the road-map” phase of its development [KuhnK'11].

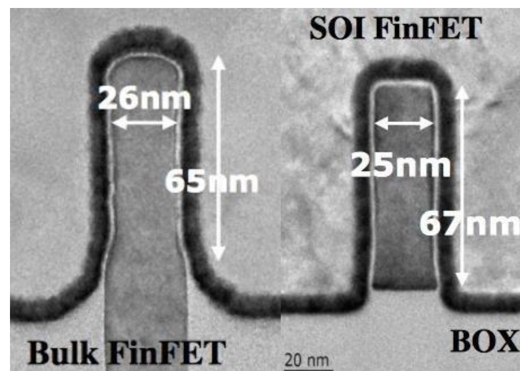


Figure 1.4. Microscopic images of fabricated bulk and SOI FinFETs.

Depending upon the type of substrate used, FinFET can be broadly classified as a bulk or SOI type as shown in Fig. 1.4. Both types of FinFETs have merits associated with their structure. The main advantage of bulk FinFET was its process compatibility with planar MOS technology and reduced self-heating. However, the SOI FinFETs are benefited from a lesser amount of junction capacitances. Apart from their merits/demerits, the choice between the bulk and SOI substrate is decided by the fabrication cost and ease of integration in the present technology setup. Typically, the body thickness is small compared to its height. Therefore, the two side gates have prominent effect in controlling the channel inversion in comparison to the top gate. Also, the top gate influence on the channel reduces when top gate oxide is thicker than the side gate oxide. Since the FinFET mainly controlled by two side gates, it is called as double-gate (DG) FinFET. Nevertheless, when the body thickness and top gate oxide are comparable to its height and side gate oxide, respectively, the presence of top gate cannot be neglected. Such a device is called as tri-gate FinFET [KavaJ'06].

When the top gate is removed, the result is an independent-gate FinFET that can be controlled separately. The IG FinFET are primarily used to dynamically control the threshold voltage. Structurally, DG-FinFET can also be differentiated as symmetric or asymmetric based on dielectric material, thickness, and gate work-function. Apart

from the double-gate/tri-gate FinFET, various other versions of the FinFET have been reported such as π-gate, Ω-gate, and quadruple-gate (shown in Fig. 1.3).

1.4 FinFET Design Challenges and Issues

More recently, the FinFET concept has been translated to bulk Si-substrates [ParkT’03], whereby the fins are now defined by Shallow Trench Isolation (STI) regions. Bulk FinFET allow fabrication on standard Si-substrates without a major overhaul of fabrication line-up. The scaling advantages of the FinFET architecture can be combined resulting in the adoption of these devices by Intel at the 22 nm CMOS technology node [JanCH'12]. Foundries such as TSMC followed the suit for 16 nm technology node [TSMC'13] and other majors such as Samsung and GlobalFoundries collaborated to produce their 14 nm FinFETs [Tech’14].

Over the past few years, considerable research have been done in FinFET directed towards numerous active areas such as device modelling [PrasN'15, MukhS’05], parasitic extraction [KumaM'05, KumaM'06, BhojA'13c, BansA’04, BindB'07] and so on. Most of the researchers have investigated the suitability of FinFETs in designing digital [RasoS'09, RasoS'10, PaulB'06, NaraR'12] and analog/RF circuits [GhosS'15, KoleK'15, KollS'07, KundA'14]. FinFET based SRAMs have also been demonstrated by few authors [MoraF'09, AnanH'06, BhojA'14]. Over the last 3-4 years, random/PVT variations in FinFET have gained significant attention [YangY'14, RaoR'10, DadgH'10, MahmH'05]. Despite the advantages of double/tri-gate structures, there are several challenges that need to be taken care off.

1.4.1 High-permittivity Materials as Spacer

As FinFET shrinks down continuously, electrostatic control reduces that gives rise to SCEs. Moreover, fabricating a precisely controlled and well-defined doping profile in sub-20 nm technology nodes is very difficult that degrade the device performance. Therefore, the undoped underlap region is unavoidable in devices with gate length 20 nm or less [YangJ'07]. Although, the underlap region helps in reducing SCEs but at the expense of drive current (I_{ON}). As the underlap length (L_{un}) further increases, the series resistance ($R_{S/D}$) starts dominating and hence gate-source/drain (G-S/D) barrier restricts the carriers to flow from source-to-drain, even at high bias. Introducing high-*k* spacers can provide strong field coupling between the gate and the underlap region

that reduces $R_{S/D}$ [TrivV'05]. However, it also increases the fringe capacitance (C_{fr}) that worsens the digital circuit performance in terms of delay and access-time.

1.4.2 Parasitic Resistances and Capacitances

From a device point of view, one of the biggest challenges is the larger parasitic resistances and capacitances due to its own three-dimensional structure. For good short channel control, a thin fin must be used. This results in a larger parasitic source/drain series resistance ($R_{S/D}$) due to the small cross sectional area of the fin extension. In order to minimize $R_{S/D}$, a raised source/drain structure is often used. The raised source/drain is formed by a selective epitaxial growth process, which creates a non-rectangular raised source/drain cross section. Another important parasitic component is the outer fringe capacitances (C_{of}) that becomes significantly higher after raising the source and drain.

1.4.3 SRAM Design Challenges

A 6T SRAM cell has the most critical design consideration in terms of leakage power, delay and noise-margins. Over the past 5-6 years, FinFET emerged as a very promising substitute to conventional MOSFET for sub-22 nm technology nodes due to its excellent electrostatic control and reduced SCEs. Furthermore, it is possible to operate FinFET at lower supply voltages because of lower (intrinsic) channel doping and larger effective channel width. Therefore, less dynamic power is achieved in SRAM circuits. Moreover, superior electrostatic control due to double/tri-gate also reduces the standby power consumption. Although, the FinFET offer some advantages in SRAM design, but also poses several new challenges due to its novel 3D architecture. The most important and inherent design challenge associated with FinFET is the width quantization effect that becomes more critical for circuits like SRAM wherein transistor sizing has significant effect on its functionality. Moreover, the read/write conflict in 6T SRAM cell aggravates the challenge posed by width quantization. Therefore, to design a power efficient, dense and stable SRAM using FinFET architecture is a major concern nowadays.

1.5 Problem Statement

Based on the challenges presented in previous sections, this work addresses the issues of high-permittivity spacer materials and FinFETs for achieving simultaneous improvement in device and circuit performance. The aim of this research work is to

comprehensively explore the suitability of high-*k* spacer technology for high-performance digital applications. The entire thesis work is divided into four parts:

- Introduction to proposed dual-*k* spacer technology and its detailed ON/OFF electrostatics, fabrication methodology and merits.
- An in-depth analysis of fringe capacitances for symmetric and asymmetric dual-*k* spacer FinFET and its impact on basic CMOS logic circuits (using inverter and a 3-stage ring-oscillator)
- Implementation of proposed dual-*k* spacer structures in the conventional 6T-SRAM cell to mitigate read/write conflict, enhance access time and leakage power as well.
- Statistical variability and sensitivity analysis of proposed symmetric and asymmetric dual-*k* spacer FinFET devices/SRAMs.

1.6 Thesis Organization

This thesis primarily focuses toward the novel spacer engineered device architecture that intelligently uses the high permittivity spacer while targeting high-performance device-circuit co-design (from the device level to circuit/SRAM perspective) and its immunity to random statistical and structural variations. The thesis consists of seven chapters. Each chapter begins with a brief introduction pertaining to the concerned problem and motivation behind the study. Moreover, the results are summarized and discussed at the end of the each chapter. A brief discussion of each chapter is presented below:

Chapter 1 provides the overview and evolution of novel MOS based tri-gate device, *i.e.* FinFET architectures, design challenges and the current research scenario of semiconductor industries/foundries. The chapter also includes the motivation of taking up the specific problem in the present research work. Furthermore, it presents the outline of the complete thesis work.

Chapter 2 presents an extensive literature review of double/tri-gate FinFET technology, gate-source/drain underlap and overlap architectures, advancement of high permittivity materials as either gate-dielectric or spacer. Furthermore, the technological restriction of high permittivity spacers that limits its usage in high-performance circuit/SRAM applications is thoroughly illustrated.

Chapter 3 introduces the dual-permittivity (*k*) spacer concept and the optimization strategy for the FinFET under study. It describes the proposed symmetric and asymmetric architectures, their fabrication methodology and superior ON- and OFF-state electrostatics over the conventional (single/low-*k* spacer) as well as the purely high-*k* spacer underlap FinFET structure. This chapter also physically interprets the ON/OFF state electrostatics associated with dual-*k* structure with an increase in inner spacer *k* value. In addition, it is necessary to analyze symmetric and asymmetric architectures that present clear understanding to distinguish the competing effects of symmetric and asymmetric dual-*k* spacer structures.

Chapter 4 describes the role of fringe capacitances associated with proposed architectures that demonstrates the suitability of high-*k* spacer materials for high-performance logic circuits improving noise-margin and delay performances. The circuit performances are evaluated based on the static and dynamic characteristics of a CMOS inverter and a three-stage ring oscillator. This chapter also presents the effect of power supply scalability on CMOS inverter based on dual-*k* FinFETs.

Chapter 5 explores the possibility of symmetric and asymmetric dual-*k* architecture for augmenting the SRAM design metrics. Cell performance is evaluated based on SNMs (hold, read, and write), read/write access times, and total leakage power. We also demonstrate the effect of underlap length and power supply scalability on dual-*k* based SRAM cells.

Chapter 6 investigates the tolerance of symmetric and asymmetric dual-*k* spacer architectures and its SRAM performance by random statistical and structural parametric variations. In addition to the superior device electrostatics and better static/dynamic circuit performance, it is observed that both the symmetric and asymmetric dual-*k* tri-gate FinFET structures also exhibit better device and circuit immunity to random variations and lesser sensitivity to key structural parameters in comparison to the conventional FinFET based circuits.

Chapter 7 concludes this research work. Conclusions are drawn based on the obtained results and major outcomes. The future scope of the work is also presented in this chapter.

The thesis ends with a complete bibliography.

1.7 Summary

This chapter presented a brief introduction of FinFET, its advantages and some challenges that need to be addressed. It concludes by providing a brief research plan and organization of the thesis. The outcome of the present work is expected to help future VLSI/ULSI designer to develop such integration schemes that will not only enhance the performance criterion in terms of speed but also reduce the overall leakage power dissipation.

CHAPTER 2

FinFET Device and Circuit Design: A Literature Review

2.1 Introduction

In the past few decades, the semiconductor industry has grown consistently to meet the performance and computing requirements of various sectors ranging from medical applications to high performance microprocessors. In recent years, the evolution of conventional silicon MOS based integrated circuits (ICs) has made it possible to integrate greater functionality and complexity on a single chip. Today, ICs serve different needs ranging from low-power mobile applications, highly reliable military applications to high performance computing applications. However, with the advent of new technology generations, there is a demand for increasing functionality within same silicon area. This serves as the driving force towards the miniaturization of the transistors.

Traditionally, bulk-MOSFETs are used in digital ICs and their scaling has been studied in detail. However, in deep sub-micron regime, bulk MOSFETs are approaching the physical limits. With the reduction in geometric dimensions, devices are increasingly suffering from short channel effect (SCE), high leakage power dissipation, increasing parasitic capacitances and resistances, large process variations, dominating interconnect delay and so on. Most of these issues pertain to the inherent device structures. In conventional bulk MOSFETs, as channel length shrinks below 100 nm, channel doping engineering such as super halo [TaurY'97a] or asymmetric channel profile [BansA'05b] are required to achieve desired threshold voltage and to reduce SCE. The high doping concentration increases the vertical electrical field resulting in mobility degradation and worsens sub-threshold swing (SS). To improve the SS, gate oxide thickness can also be reduced, that however, results in increased gate direct tunnelling current. Also, as the dimensions reduce, dopant atoms are confined in a very small volume. Therefore, their placement in the channel region affects the device electrical characteristics. Because of process fluctuations, the placement of dopant atoms is random [FranD'99] resulting in poor yield. Thus, bulk-MOSFETs are not suitable for the extreme scaling. To overcome the bulk MOSFET scaling limitations, fully-depleted thin-body silicon-on-insulator (FD-SOI) transistor

structures have been proposed [ITRS]. Because of thin body, drain field is inhibited from penetrating deep into the channel. This gives more gate control over the channel resulting in improved SCE and near ideal sub-threshold slope [FranD’92]. Improved SCE also relax the need of extreme scaling of gate dielectric thickness, thus reducing the gate direct tunneling leakage. To increase the drive current and to provide more gate control over the channel, several multi-gate structures such as planar double-gate [WongH’97], FinFET [HisaD’00], tri-gate [ChauR’02] and omega-FET [YangF’02] have been proposed.

2.2 Multi-gate MOSFETs (MugFETs)

In a continuous effort to increase the drive current and also to control SCEs, SOI transistors have evolved from classical, planar, single-gate devices into three-dimensional devices with a multi-gate structure (*i.e.* double, triple or quadruple-gate). Multi-gate FETs offer certain advantages over the conventional single-gate MOSFETs.

One of the most important advantages is the excellent gate control over the electrostatic charges. This increased charge control in the channel translates into improved short channel effects [ColiJ’04a]. Since the channel is controlled electrostatically by the gate from multiple sides, the channel is better-controlled by the gate than in the conventional transistor structure. Unwanted leakage components are reduced and a small transistor can be used to continue the cost reduction through miniaturization. Improved gate control also provides the lower output conductance. This provides greater voltage gain, which is beneficial to RF/analog circuits as well as to the noise tolerance of digital circuits.

Another distinct characteristic of MugFETs are the increased ON-current and therefore faster circuit speed [MRSP'03]. One of the main advantages of using multiple-gate device is the highly improved electrical characteristic in the sub-threshold regime [ColiJ’04b]. The drain induced barrier lowering (DIBL) characteristic of a fully depleted multiple-gate transistor is much improved over a normal single-gate (SG) MOS transistor. The volume inversion is a phenomenon observed only in multiple-gate architectures. A device is said to be operating in volume inversion if there is a strong coupling between two conducting channels [BaleF’87]. In multiple gate devices, the use of a very thin film allows to downscale

the devices without the need of using high channel doping densities and gradients [ChoiY'00]. In fact, undoped films can be used wherein the fully depleted thin film prevents the punch-through mechanism. Besides this, the absence of dopant atoms in the channel increases the mobility by suppressing impurity scattering [ChoiJ'95].

Multi-gate nanoscale devices have many advantages in circuit performance. A very high packaging density is possible because of the smaller size of these devices that have short channel and thin film. Because of the higher mobility, transconductance can be higher, which gives more current gain and allows a higher operating frequency. Therefore, multiple gate nanoscale devices are potential candidate for RF and microwave applications [SohnC'12, MokuN'10]. The analog performance of these devices is also superior. Moreover, the voltage gain is much higher than the gain of conventional bulk MOSFETs, especially in moderate inversion region. In this section, we present a brief overview of planar DGFETs and FinFETs technology.

2.2.1 Planar Double-gate (DG) MOSFETs

The first article on the double-gate MOS transistor was published by Sekigawa and Hayashi in 1984 [SekiT'84]. The device was called XMOS because of its cross-section that looks similar to the Greek letter Ξ *(Xi)*. These double-gate transistors demonstrated significant reduction of SCEs by the configuration wherein the drain-source channel was sandwiched between two independently fabricated gate/gate-oxide stacks as shown in Fig. 2.1.

Figure 2.1. Planar double-gate MOSFET.

The double-gate FET can be thought of as an enhanced version of an FD SOI transistor with a very thin buried oxide (same thickness as the gate oxide). Only now, the back substrate is heavily doped and electrically connected to the top gate. Since there is no capacitive potential division between the top and bottom gate, *i.e.* both of them drive the substrate together, the gate to substrate coupling is perfect and the long

channel SS is nearly 60mV/decade. In addition, the short channel effect control is very good by virtue of a thin fully depleted body and gate shielding of drain electric field lines from both sides. Due to the action of two gates, the device can now be scaled to shorter gate lengths for the same body (and oxide) thickness.

Depending upon the structure, materials or applied gate voltages, DG MOSFETs may be categorized to symmetric and asymmetric. Symmetric DG-MOSFET are obtained when both the gates have same work-function, oxide thickness, dielectric material and common input voltages applied to the gates, whereas an asymmetric DG MOSFET is created by introducing asymmetry through input voltage, work functions, thickness, gate-dielectrics, materials etc.

Planar DGFETs had been extensively researched during the initial phase of evolution of multi-gate transistors. Although, the DG-MOS device offers significant advantages over single-gate (SG) devices, but it has not played a significant role in the CMOS technology front till date. The reason is that the planar DGFETs are difficult to fabricate [NowaE’04]. There are problems in aligning the top and bottom gates as well as in building a low resistance contact to the bottom gate [YinC'05]. Manufacturing a self-aligned double-gate MOSFET has been the holy-grail for device engineers and researchers ever since it was proposed. The alignment of the top and bottom gates to each other as well to S/D diffusion is crucial, as any misalignment can result in parasitic capacitance. This problem is resolved in the FinFET, which has a self-aligned triple-gate structure.

2.2.2 FinFET Technology

The next major step forward in the electronics industry has been the introduction of FinFET technology. A FinFET is a new type of multi-gate 3D transistor that offers significant performance improvements and power reduction compared to existing planar CMOS devices. In a FinFET, the gate of the device wraps over the conducting drain-source channel as shown in Fig. 2.2. This results in better electrical properties, providing lower threshold voltages and better performance as well as reductions in both leakage and dynamic power.

The first fabricated self-aligned double-gate SOI structure was published in 1989, by D. Hisamoto *et al.* [HisaD’89]. Initially the transistor was named as DELTA *i.e.* fully **DE**pleted **L**ean-channel **T**r**A**nsistor. This was renamed as FinFET by researchers

of University of California, Berkeley in 1999 [HuanX'99]. ITRS considers it as the potential candidate to replace classical MOSFETs due to the benefits of multi-gate transistor and relatively easier fabrication technique [ITRS]. The processes to fabricate DG-FinFET device options can be found in the literature [MathL'04, MasaM'06]. Thereafter, extensive research has been carried out on FinFET/tri-gate technology from the device performance optimization and methodology to the circuit design.

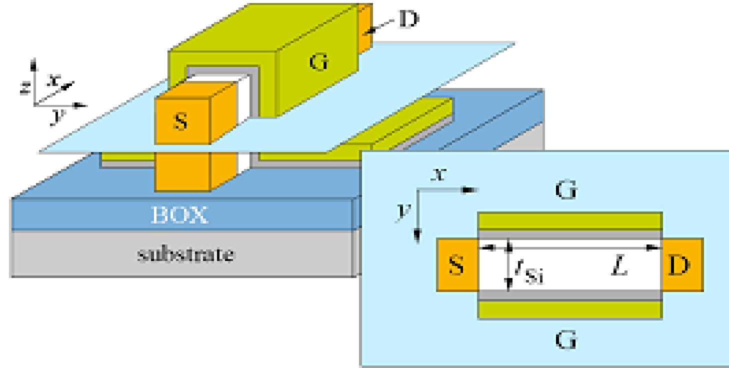


Figure 2.2. A cross-sectional view of FinFET structure.

In FinFET devices, the width of the silicon film (T_{fin}) is much smaller than its height (H_{fin}) that resembles to the fin of a fish. The two side gates mostly control the device operation, and according to an empirical scaling rule T_{fin}, which defines the separation between the two side gates must be less than one-third of channel length to suppress SCE. As is evident, the electrical width of a triple-gate FinFET is $W=2H_{fin}+T_{fin}$. In many cases, T_{fin} is small in order to have acceptably small SCE. Moreover, in a DG-FinFET, the top gate is anyway ineffective. As a result, W is approximately $2H_{fin}$. As a result, the physics of a FinFET becomes largely similar to that of a DGFET. Thus, most of the literature that discuss compact model development for DGFETs can be applied to FinFETs with a minor parameter (H_{fin}) adjustment.

FinFET can be fabricated with their channel along different directions in a single die. Fabrication of planar MOSFET channels along any crystal plane other than ⟨100⟩ is difficult due to process variations and interface traps [MishP'10b, ChngL'04]. However, the FinFETs can be fabricated along the ⟨110⟩ plane as well. This results in enhanced hole-mobility. The ⟨110⟩ oriented FinFETs can be fabricated by simply rotating the transistor layout by 45° in the plane of a ⟨100⟩ wafer [KangM'10]. Thus, *n*-FinFETs implemented along ⟨100⟩ and *p*-FinFETs along ⟨110⟩ lead to faster logic

gates since this gives designers an opportunity to combat the inherent mobility difference between electrons and holes. However, this multi-orientation scheme has an obvious drawback of increased silicon area [KangM’10].

2.3 FinFETs Classification

FinFETs have attracted increasing attention over the past one and half decade because of the degrading short-channel characteristics of conventional MOSFETs [ReddG'05, OrouA'06, KumaS'14]. It was the most researched device technology by the leading foundries/industries as well as academia [SharR'09, MajuK'10a, MajuK'10b]. Therefore, the FinFET technology comes with various flavours (as shown in Fig. 2.3) depending upon their usage in device/circuit perspectives such as double-gate or tri-gate FinFET, symmetric and asymmetric FinFET, tied-gate and independent gate FinFET, and bulk/SOI FinFET. This section will briefly discuss the various classifications and capabilities offered by the FinFET.

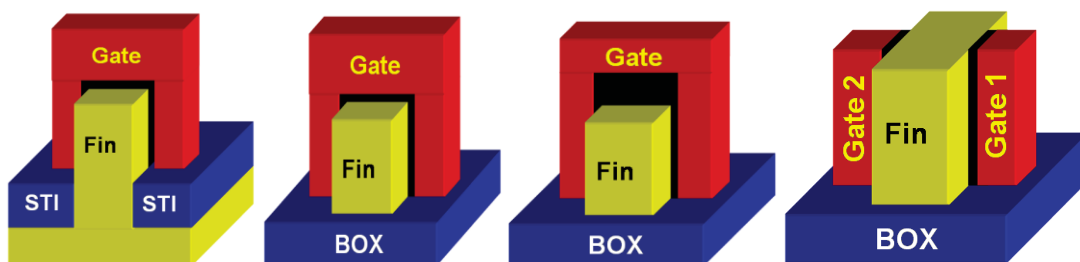


Figure 2.3. (a) Tri-gate bulk FinFET, (b) tri-gate SOI FinFET, (c) double-gate SOI FinFET, and (d) independent double-gate FinFET.

2.3.1 Bulk and SOI FinFETs

FinFET can be made on both bulk or SOI substrates known as bulk FinFET [Fig. 2.3(a)] and SOI FinFETs [Fig. 2.3(b-d)], respectively [ParkTS’06, KawaH’06, KimSY’05]. However, the FinFETs implemented on SOI wafers are very popular and researched extensively. Unlike bulk FinFETs, where all fins share a common Si substrate (also known as the bulk), fins in SOI FinFETs are physically isolated. From industrial point of view, most of the foundries would prefer the bulk technology because it is much easier to migrate to bulk FinFETs from conventional bulk MOSFETs. However, FinFETs on both types of wafers are quite comparable in terms of cost, performance, and yield.

2.3.2 Double-gate and Tri-gate FinFETs

In general, FinFET can also be categorized as a tri-gate [Fig. 2.3(a-b)] and double-gate FinFETs [Fig. 2.3(c-d)]. Both are the variant of a FinFET family. With an active third-gate on top of the Si-channel [as shown in Fig. 2.3(a-b)], the FinFET architectures are abbreviated as tri-gate or triple-gate FinFETs. In triple-gate FinFETs, both the side surfaces and the top surface conduct current. The top gate also helps for self-alignment between the two side gates.

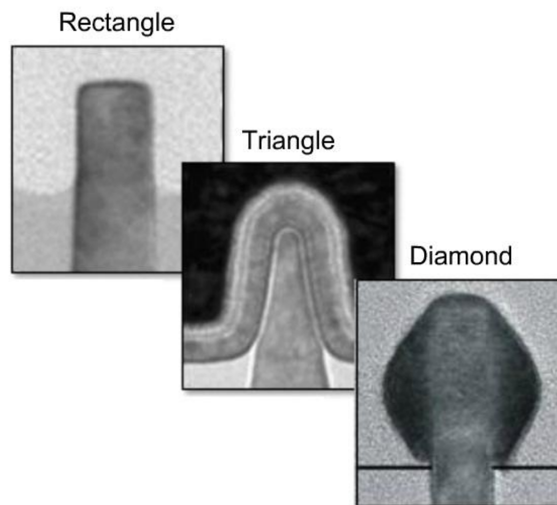


Figure 2.4. TEM cross-sections of the fin shapes of different foundries.

In tri-gate FETs, the thickness of the dielectric on top of the fin is similar to that of the side-gate oxide thickness in order to activate the third gate. Due to the presence of the third gate, the thickness of the fin also adds to the channel width. Hence, tri-gate FinFETs enjoy slightly higher width advantage over the double-gate FinFETs. However, depending upon the process flow of the respective foundries, the fin shape can be rectangular [WuCC'10], triangular [AuthC'12] and diamond shape.

Recently, Intel announced a big change in the electronic switches at the heart of its CPU. They introduced tri-gate FETs at the 22 nm node in the Ivy-Bridge processor in 2012 [AuthC'12, MarkJ'11]. Going forward, the firm announced commercial usage of the three-dimensional transistors (triangular FinFET) instead of long-used planar MOS architecture because of their superior attributes at advanced technology nodes. In particular, FinFET demonstrates better performance leakage and dynamic power, intra-die variability, and retention voltage for SRAMs.

For double-gate FinFET, either the top-gate can be disabled by fabricating a thick hard-mask oxide layer (served as a tied double-gate FinFET) or the top-gate is etched out and the two gates can be controlled independently. Therefore, the top surface of the fin does not conduct current in double-gate FinFET. Yang *et al.* compared the tri-gate with double-gate FinFET and argued that the double-gate FinFET are superior to tri-gate FET in the long run [YangJ'05]. They showed that although the undoped tri-gate FET enjoy more relaxed body thickness, they are not competitive with double-gate FinFET in SCE metrics. When trying to achieve comparable SCE metrics, tri-gate FET lose the scaling advantage and suffer from significant layout area disadvantage. However, with new triangular architecture, it is premature to declare a clear winner between double and tri-gate FinFET [BhatD'14].

2.3.3 Tied-gate and Independent-gate FinFETs

Based on the number of terminals, FinFET can be categorized either as the tied-gate (TG) [Fig. 2.3(a-c)] or independent-gate (IG) [Fig. 2.3(d)] configurations. TG FinFETs are also known as shorted-gate (SG) or three-terminal (3T) FinFETs and IG FinFETs as four-terminal (4T) are commonly known as double-gate FinFETs. In TG configuration, the two side gates are connected through the top-gate to form a three-terminal device. Initially, the top gate was used for the perfect alignment of the two-side gates. Thus, in TG FinFETs, both gates are jointly used to control the electrostatics of the channel. Hence, TG FinFETs show higher on-current (I_{ON}) compared to those of IG FinFETs. In independent-gate configuration, the two side gates are separated and can be independently biased which can be achieved by removing the top portion of the gate of a regular FinFET using chemical mechanical polishing (CMP).

Because of the four terminals, IG FinFETs offer the flexibility of applying different voltages to their two gates that enables the use of the back-gate bias to modulate the V_{th}. This additional advantage of IG FinFET proves it as a possible solution of width-quantization. Over the past decade, IG-mode FinFETs have been extensively researched from circuit perspectives [GuptS'11, EndoK'08]. IG FinFETs suffer from high area penalty due to the need for placing two separate gate contacts and the comparatively higher parasitic (due to more interconnect lines). In a later section, these techniques will be discussed and how they improved the circuit/SRAM performance metrics is also covered.

2.3.4 Symmetric and Asymmetric FinFETs

From device perspective, FinFETs can be further categorized as symmetric and asymmetric architectures. Symmetric FinFET architecture is perfectly symmetrical or similar with respect to source/drain terminal as well as front and back gates. Most of the reported symmetric architecture that claimed for better device/circuit performance uses some performance booster such as high-*k* gate dielectric or spacer [ZhaoH'08]. Rest of the symmetrical structure uses variations in key process and structural parameters such as dopant segregation, S/D extension length *etc.* Contrastingly, most of the asymmetric FinFET architectures targeted some specific device/circuit applications such mitigation of the read/write conflict in 6T SRAM cell.

Asymmetry in FinFET structures can be introduced from several ways. Initially in double-gate MOSFETs, the asymmetries were incorporated by applying different potential on both gates, using different work-function material gates, and by fabricating different front and back-gate oxide material or thickness. However, over the past 3-4 years, several researchers have introduced asymmetries with respect to source and drain terminal as well [GuptS'11, MoraF'11, SalaS'13a]. Although, these types of asymmetries restrict the conventional interchangeable source drain concept, but is useful for the applications having pass transistors. These asymmetric architectures will be discussed in detail later in this chapter.

2.4 FinFET Fabrication

In order to improve the short channel characteristics of FinFET, low fin thickness are required [CollN'05]. Typically, the fin thickness is equal to approximately half the gate length or lower that achieves good electrostatics in FinFETs [TawfS'09]. Since the minimum feature size associated with a technology is defined by lithography for the gate length, the fabrication of FinFET requires sub-lithographic patterning technology for the formation of fins. Some examples of sub-lithographic patterning techniques include resist washing followed by oxide hard mask trimming [AsanK'01] and spacer lithography [ChoiY'02a]. There are several techniques for fabrication of FinFETs but we will discuss only the spacer patterning technique.

In this sub-section, we focus towards spacer lithography and describe the features of this technique. Fig. 2.5 shows the fabrication process for FinFETs using spacer patterning. A sacrificial layer of $Si_{0.4}Ge_{0.6}$ is deposited and patterned using

lithography. Phospho-silicate glass (PSG) spacer is deposited around the SiGe sacrificial layer. PSG layer is etched out from the top of SiGe so that the PSG layer remains only on the side of SiGe. Next, the SiGe sacrificial layer is etched out. The PSG layer that remains after the etching of the sacrificial layer serves as the mask for the formation of fins. Thus, the fin thickness is determined by the thickness of the PSG spacer layer and is not limited by lithography. In this manner, fins with low thickness can be formed by controlling the thickness of the PSG spacer layer deposited around the sacrificial layer.

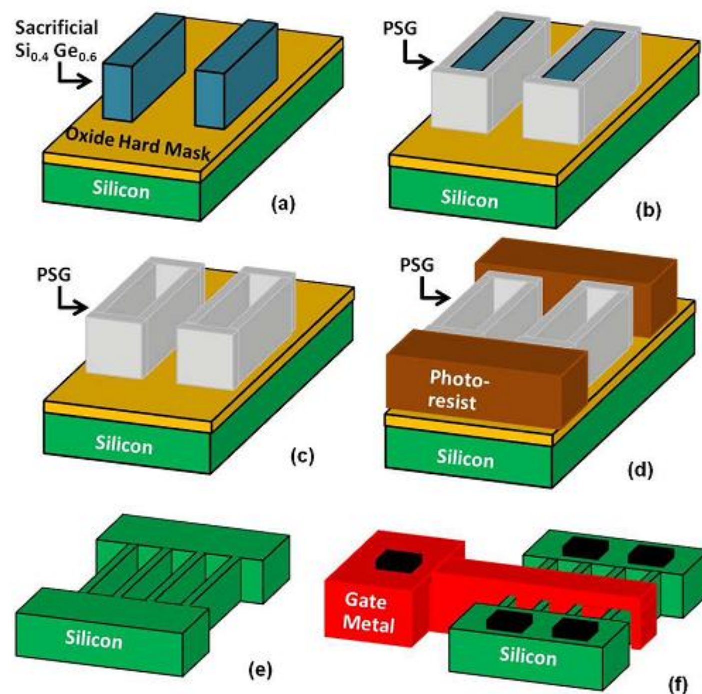


Figure. 2.5. Fabrication of FinFETs using spacer patterning/lithography technique: (a) Deposition and patterning of sacrificial $Si_{0.4}Ge_{0.6}$ layer (b) deposition of phosphosilicate glass (PSG) spacer layer around $Si_{0.4}Ge_{0.6}$ and etching of PSG from the top of $Si_{0.4}Ge_{0.6}$ (c) etching of $Si_{0.4}Ge_{0.6}$ (d) formation of photo-resist mask for source/drain (e) formation of fins and source/drain using PSG and photo-resist as masks and (f) deposition of gate dielectric, gate metal and contacts and doping of source/drain to obtain the FinFET structure [ChoiY'02].

After the etching of the sacrificial layer, a photo-resist is deposited and patterned for forming the raised source and drain [ChoiY'02]. Note that the raised source/drain (S/D) is often used for FinFET structures in order to reduce the S/D resistance [VegaR'09]. With the photo-resist and the PSG spacers acting as the masks, fins with raised S/D are formed. The gate dielectric and gate metal/poly are deposited and patterned. This is followed by the formation of the gate spacers and doping of S/D.

Finally, gate and S/D contacts are formed to obtain a FinFET. It may be mentioned that FinFETs can be fabricated on silicon-on-insulator (SOI) [HisaD'00] or on a silicon substrate (body-tied) [ParkT'03]. The main difference between the two structures is that in SOI FinFETs, the body is floating while in BT FinFETs; the body potential can be controlled using a substrate contact. It can be observed from Fig. 2.5 that due to formation of spacer on both sides of the sacrificial layer, fins are formed in pairs in spacer lithography technology. Thus, the density of fins is doubled compared to a lithography based technique for fin formation. If odd number of fins is desired, one fin has to be etched away. In other words, FinFETs with $2i$ and $2i$-1 fins (where i is a natural number) have the same device footprint [ChoiY'02].

2.5 Challenges and Issues of FinFET Technology

Like any other new technology, FinFETs also poses several device/circuit co-design challenges. Custom designers who are closely working with standard cells, and analog designers working on IP blocks, noticed some challenging issues associated with the FinFET technology. In particular, some of the design strategies such as the flexibility in width adjustment that have been used in the past for conventional/planar MOSFET will not work for FinFETs and the other multi-gate architectures such as cylindrical gate/nano-wires *etc*. This is because the intrinsic device characteristics of FinFETs are very different from the planar MOSFETs.

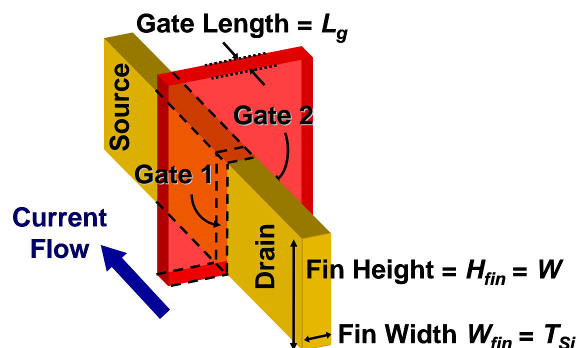


Figure 2.6. 3D FinFET architecture showing the self-aligned gate wrapped on the Si-channel.

Fig. 2.6 shows a FinFET structure in which a gate is wrapped on the silicon-channel. The channel in planar MOSFET is horizontal whereas the FinFET channel (also known as the fin) is vertical. Hence, the height of the channel (H_{fin}) determines the width (W) of the FinFET. With planar transistors, standard cell designers can arbitrarily change transistor width in order to manage drive current. However, with

FinFETs, designers cannot do the same. For this, designer can only add or subtract fins to change the drive current. In other words, the FinFET width must be a multiple of H_{fin}, that is, widths can be increased by using multiple fins. Also the fins come in discrete increments thus, arbitrary FinFET widths are not possible *i.e.* we can't add three-quarters of a fin. This issue is commonly known as "width quantization". Although smaller fin heights offer more flexibility, but they lead to multiple fins, which in turn lead to more silicon area. On the other hand, taller fins lead to less silicon footprint, but may also result in structural instability. Typically, the fin height is determined by the process engineers and is kept below four times the fin thickness [AlioM'11, CollN'05].

There are several other issues also related to FinFETs but have not gained much importance as the width quantization has gained over the years. For example, body biasing will generally be impractical in FinFETs in comparison to the planar MOSFETs. Moreover, in order to modify the device threshold voltage by bulk biasing in16/14nm processes, one requires a very large voltage supply since the distance of the top of the fin (the active part) from the bulk is very large. This high supply voltage is neither feasible nor efficient enough in terms of power dissipation.

The long and narrow portion of the fin that is not under the gate is called the extension region. This region is technologically unavoidable, because it is not possible to have a steep lateral doping gradient, starting from a highly doped source/drain and ending at a lightly doped channel region. A lightly doped body is often preferred because it helps in reducing corner effects [FossJ'03b], random dopant fluctuations and mobility degradation effects. As a result, FinFETs typically have a relatively large parasitic series resistance and capacitance. These parasitic resistance and capacitance represent another challenging area for the custom designer.

As the device shrinks further on the horizontal plane, and at the same time the top gate dimension increases, a new coupling to neighbouring elements appear and create additional parasitic capacitances. Starting at 20 nm, C_{GS} (gate-to-source capacitance) and C_{GD} (gate-to-drain capacitance) effects become a larger concern and it contribute to the Miller effect that feeds the output of a circuit back into its input through the parasitic capacitances. Also, additional parasitic resistances in the source/drain area affect the device performance.

Clearly, it is observed that introduction of FinFETs comes with several new design challenges. Most of these challenges are related to their effective usage while deriving maximum benefit of their characteristics. Nowadays, advanced TCAD/EDA tools can provide assistance in resolving these challenges that certainly help in finding the best designs using FinFETs.

2.6 FinFET Device/Circuit Performance Analysis

Over the past decade, FinFET architecture is the most researched and mature amongst all the multiple-gate technologies. Therefore, an extensive work has been carried out and reported on FinFET technology from the device performance optimization to the circuit/memory design perspectives. This section will review the state-of-the-art FinFET device, circuit design, various optimization strategies and performance metrics.

2.6.1 Device Structure and Performance Optimization

As the FinFET dimensions shrink, the SCEs and leakage currents continues to dominate that degrades the device performance. Therefore, most of the recent research works have been focused towards the device optimization considering various FinFET structures. Similar to the planar MOS devices, FinFETs also have overlap and underlap regions. The concept of “non-overlapped” gate-source/drain (G-S/D) with low-doped channel was suggested [TrivV'05] to facilitate the scaling of bulk-Si MOSFETs to 20 nm gate lengths. However, the difficulty in fabricating precisely controlled and well-defined doping profile necessitates the usage of undoped underlap regions. In underlap structure, the effective channel length (L_{eff}) is significantly longer than the physical gate length (L_G) in weak inversion, while L_{eff} is comparable to L_G in strong inversion [FossJ’03a, YangJ'07]. As a result, SCEs can be suppressed while maintaining the current driving capability. Previous studies have shown enhanced current drivability with an optimized G-S/D underlap structure [ShenR’03, SchuT’04, BalaS’03]. However, they have not considered the parasitic capacitance that strongly affects the switching speed in deeply scaled FinFETs.

On device level, several researchers have focused on the integration of high-*k* materials to enhance the device performance [ShahD'09, AgraS'10, AgraS'08]. The fringing-field phenomenon through these high-*k* gate dielectrics have been studied by few researchers from circuit perspectives [ManCR’07, MohaN’03]. A high-*k* gate

dielectric could offer additional advantages such as significant enhancement in the performance and scalability [VellG'07]. The possible high-k advantages include thinner effective oxide thickness (EOT), which implies higher gate capacitance (C_{GG}) and ON-state current (I_{ON}). Also, the larger physical thickness (T_{hk}) of the high-k dielectric reduces the parasitic gate-source/drain (G-S/D) outer-fringe capacitance [KimSH'06, ManCR'07]. However, these merits come hand in hand with certain disadvantages. The larger T_{hk} results in the fringe induced barrier lowering (FIBL) effect that significantly degrades the SCE control [ManCR'07, MohaN'03]. Moreover, the channel mobility tends degrade significantly due to poor quality of the Si/high-k dielectric interface [ZhuW'04] and long-range scattering from optical phonons inherently present in high-k insulators [FiscM'01]. Further, the integration of a high-k dielectric into the CMOS process presents alarmingly large technological challenges [LeeJC'05, SongS'06]. Manoj *et al.* [ManCR'07] did a simulation-based study of the impact of high-k dielectrics on nanoscaled FinFET design and its performance. They compared L_G=32 nm devices having different gate dielectric constants (k). They have maintained the same OFF-state current (I_{OFF}) in each device by reducing T_{fin} with increasing k to suppress FIBL. They simulated CMOS ring-oscillator, giving good insights, and reported a modest performance enhancement for an optimized permittivity of k~20, relative to counterpart CMOS with SiO_2 gate dielectric [AgraS'10].

Introduction of high-k spacers can provide strong field coupling between the gate and undoped underlap region that reduces $R_{S/D}$ [TrivV'05]. This effect is commonly known as gate fringe induced barrier lowering (GFIBL) that enhances the digital performance during strong inversion regime [SachA'08]. Increasing S/D extension length (L_{EXT}) will increase the undoped/low-doped portion of L_{EXT} near to gate edge of underlap FinFET. Therefore, restricting high-k dielectric to the gate side wall can enhance the gate sidewall fringing fields that in turn can raise the barrier to conduction at weak/moderate inversion regime. Ever since the devices have been scaled in the sub-micrometer regime, the parasitic capacitances have been a significant part of the gate capacitance that increases much faster as the scaling continues [BansA'05a]. Trivedi *et al.* [TrivV'05] first reported the effect of gate fringing field in double-gate MOSFET on total gate capacitances using numerical simulation while discussing the effect of abrupt and underlapped gate profile. Bansal

et al. [BansA'05a] investigated the effect of fringing-field component from the gate sidewall to the source through spacer in double-gate MOSFET using conformal mapping. In 2010, Manoj *et al.* [ManCR'10] reported an enhanced fringe capacitance in FinFETs at 22 nm node compared to the equivalent planar MOSFETs. It is noted that the high-k spacers increases the fringe capacitance (C_{fr}) that worsens the circuit delay in digital applications. To the best of our knowledge, none of the research works have ever explored the direct impact of fringe field in enhancing the dynamic circuit performance in high-k spacer devices. Therefore, a comprehensive study of three-dimensional (3D) fringing field due to high-k spacers on both device and circuit performance is still critically required.

2.6.2 Circuit Design Applications

This sub-section focuses on the critical issues of FinFET circuit designing. In this, we review the merits and demerits of reported FinFET based circuits in terms of leakage power and functionality of analog/digital circuits and high performance SRAM cells. Several authors investigated the potential of FinFET technology in digital circuits for high performance digital applications [BhojA'13a, BhojA'13b, BhojA'13c] and SRAM memory design [BansA'07]. Regarding digital circuit design, most of the work has been based on independent gate configurations [DattA'07]. It has been reported that an independent control of front and back gates (as dynamically adjustment of the V_{th}) can be exploited either to reduce standby power or to merge parallel transistors that reduces dynamic power through the reduction of parasitic capacitance. Cakici *et al.* [CakiT'07] defined and presented different device as well as circuit design possibilities of DG-FinFETs. For example, authors in [WuXW'06, NirmD'13] describe the suitability of double-gate MOSFETs in sub-threshold circuits to achieve ultralow power consumption when speed is not of utmost importance. Chiang *et al.* [ChiaM'06], proposed a novel logic-circuit technique by employing independent-gate DGFET device. Using tied-gate configuration, Landsiedel *et al.* [LandD'09] showed the benefit of the multiple-gate inverter leading either to a lower leakage power at the same speed or to a higher speed at the same leakage as in case of conventional MOSFET. Independent-gate operation advantages in various circuits such as Schmitt triggers, dynamic logic circuits, sense amplifiers, and static random-access memory (SRAM) bit-cells have been shown in [MahmH'04]. Multi-threshold based FinFET sequential circuits with independent-gate bias, work-function

engineering, and gate-drain/source underlap engineering techniques are demonstrated in [TawfS'11]. Lacord *et al.* [LacoJ'12] compared planar and vertical FinFET structures from circuit perspectives in terms of propagation delays for inverter and NAND gate chain. Also, they investigated the impact of the width under several design rules for different FinFET configurations. Low-power multi-gate circuit design has been explored from device/circuit point of view in [PachC'07]. In [MuttA'07, RostM'11], logic styles leveraging the tied and independent-gate modes of FinFET operation have been investigated. FinFET latches and flip-flops have been studied in [TawfS'08a]. Due to small dimensions, a FinFET is expected to suffer from the process and temperature variations. Metal-gate work-function variation is shown to be the most important contributor to the variation in V_{th} for FinFETs. FinFETs with asymmetric gate work-functions in the form of n^+/p^+ poly-silicon gates have been engineered and investigated in [KedzJ'01].

FinFET offers lot of interesting device features that are potentially good for RF/analog applications. In past half a decade, many research groups focused towards the FinFETs applications in analog/RF circuits design. In [WambP'07], authors demonstrated the combination of a new gate stack in FinFET architecture that outperforms the comparable circuit realizations in planar bulk CMOS for low to moderate speed. In the microwave and millimetre-wave frequency region, planar bulk CMOS are still superior. The primary challenge for the FinFET structure in the coming years is the improvement of maximum cut-off frequency beyond 100 GHz. Flude *et al.* [FuldM'07] demonstrated benefits of FinFET in analog circuit applications and claimed that the introduction of novel gate stack materials (*e.g.* metal gate, high-*k* dielectric) and modified device architectures (*e.g.* fully depleted, undoped fins) can significantly affect the analog device properties. Also, the resulting benefits for speed, accuracy and power trade-off in analog circuit design were presented. Thereafter, several device design engineering and optimization strategies have been applied to FinFETs to enhance performance metrics in analog/RF domain. For example, Mohankumar *et al.* [MokuN'10] investigated the influence of channel and gate engineering on the analog/RF performance of DG FinFETs. Also, the analog and RF performance of a single halo double gate MOSFET implemented with dual-material gate (DMG) technology is investigated in [MokuN'09]. Recently, some papers reported the analog/RF performance enhancement of underlap DGFETs with

high-k spacers for low power applications [KranA'07]. Sohn *et al.* [SohnC'12] proposed some guidelines for FinFET based RF/analog applications in terms of fin height and fin spacing.

2.6.3 SRAM/Memory Applications

FinFET is an emerging technology and the ITRS predicted that by the end of year 2016, the memory circuits would occupy 94% area of a total chip [ITRS]. Therefore, it is very important to have an overall literature review to understand the progress of FinFET based SRAM cells considering the device, circuit, and technological issues.

Designing a power efficient, area efficient and robust SRAM cell is a major concern. Furthermore, there are several important trade-offs also that need to be considered to find an optimized design for SRAM. Most of the time the large SRAM cell array remains idle; therefore, the static power consumption is a big issue for memory circuits. To reduce the leakage, there are two techniques that can be followed. The use of longer channel length is one of the two techniques, but it further affects the area, capacitance, access time and active power. Another technique is to use higher threshold voltage that in turn affects the access time. The larger size transistors ensure larger design margins, therefore it offers enhanced device performance but at the cost of area. To reduce the area, lower supply-voltage can be used that also reduce the leakage power consumption. In addition, it degrades the static noise margin (SNM). The increase in gate leakages and decrease in I_{ON}/I_{OFF} current ratio also affects the SNMs. Access time is an important parameter for SRAM cell design and it is dependent on the successful read/write operation [ZhenG'10, ZhenG'05, TawfS'08b]. Due to less channel doping and larger effective channel width, it is possible to achieve lower operating voltage therefore less dynamic power in FinFET SRAM circuits. The better control over the channel due to double-gate allows us to achieve better SCEs with low static power consumption.

As we already discussed, the fin width can only be increased in quanta of fin height. Therefore, the width quantization became a major issue for FinFET based SRAM circuits. As the SRAM circuits require proper transistor sizing for robust performance which could be achieved through width optimization in planar technology, but is not an available in FinFET. Moreover, the conflicting design requirements in 6T SRAM cell for achieving high read and write stabilities make the

situation even more complicated. Considering these facts, Fossum *et al.* [KimSH'07] reported the design optimization and performance projections of double-gate FinFETs with gate-source/drain underlap for SRAM applications.

2.6.3.1 Source/Drain Asymmetric FinFET based SRAM Cells

In reported literature, several radical departures such as S/D asymmetry, back-gate biasing, and usage of some performance boosters in FinFET have been proposed earlier that claimed to mitigate read-write stability conflict. A substantial volume of research focused on the independent-gate configurations for threshold (V_{th}) adjustment [MasaM'07, GuptS'11, EndoK'08], while several others proposed asymmetric S/D device architectures [GoelA'11, MoraF’11] that enhanced the process as well as circuit complexity. Although, the S/D asymmetry helps in altering the pull-up (PR) and cell-ratio (CR) exploiting the bidirectional current flow to augment the SNMs but in turn adversely affects the cell-area, leakage power and access-times. In this sub-section, we analyze the concept of introducing asymmetry in FinFET device and the way it affects the SRAM cell performance and robustness.

Goel *et al.* [GoelA'11] presented an asymmetric drain spacer extension (ADSE) that introduced a gate underlap only on the drain side using an extended spacer. Compared to conventional FinFET SRAM, asymmetric FinFET exploits the magnitude of currents for positive and negative drain-to-source voltages. Authors have claimed to achieve 57% decrease in leakage, 11% improvement in read static noise margin and 6% improvement in write margin. However, it suffered from degraded access-time (7%) and cell area (7%). Similarly, Moradi *et al.* [MoraF’11] proposed an asymmetrically doped (AD) FinFET in which asymmetry in the device is achieved by unequal source/drain doping of FinFETs. Based on this, authors designed a FinFET SRAM cell that would simultaneously improve read and write margin and also mitigate the read/write conflict. Using AD FinFET, they achieved superior short channel characteristics, lower cell leakage, improved read SNM, write-margin, write time, and hold SNM. This AD based SRAM cell is also able to resolve the read-write conflict as the strength of the access transistors varies with the storage node voltage. The improvements reported in read and write SNM are 7.3% and 23%, respectively. However, these improvements also come at the cost of an excessively increased access time of 42% because the access transistor becomes weak during a read operation. Recently, Sachid *et al.* [SachA'12] proposed a stable SRAM cell structure

by fabricating multiple fin-heights that might be a better solution to width quantization but with an increased process complexity.

Ebrahimi *et al.* [EbraB'12] studied the different characteristics of 6T and 4T SRAM cells based on asymmetric FinFET structures. Recently, Salahuddin *et al.* [SalaS'13a] proposed two novel 6T FinFET SRAM cells based on asymmetrical gate underlap technique under process parameter fluctuations. In first design, they constructed the cell with asymmetrically gate overlap/underlap engineered FinFET-OU. In this design, the right side of the device is underlapped and the left side is overlapped. In this SRAM-OU cell, the underlapped sides of asymmetrical FinFET-OU are connected to the data storage nodes and the overlapped sides are connected to the bit-lines. In their second design [SalaS'13b], they proposed a memory cell based on asymmetrically gate underlap engineered FinFET-AU. Here, the longer underlapped sides of asymmetrical FinFET-AUs are connected to the data storage and the shorter underlapped sides are connected to the bit-lines. As the direction of the current flow is reversed, the strengths of the asymmetrical bit-line access transistors are weakened during read operations and enhanced during write operations. Therefore, the conflicting design requirements of achieving read/write stability can be mitigated. Both the proposed asymmetrical designs provide much better read SNM of around 70% compared to symmetrical gate underlap based design. However, the leakage power was reduced with the second design compared to the first one. Hu *et al.* [HuVP'10] reported that the asymmetric source-underlap access transistors can improve read SNM but can degrade write-margin. They observed that the FinFET SRAM cell based on asymmetric source/drain underlap access and pull-up transistors (at V_{DD}=1 V) can improve the RSNM by 20.5% with comparable WSNM, 10% reduction in cell read access time and 36% improvement in write-time as compared to symmetrical FinFET SRAM cell. However, due the worse electrostatic integrity caused by the underlap, it is not possible to further improve the RSNM by using source/drain-underlap access transistors as the V_{DD} reduced below 0.6 V.

2.6.3.2 Independent Gate-based FinFET SRAMs

As the circuit designs with FinFETs offer some unique features to explore, the independent-gate FinFET is likely to be the most important one. For the independent gate based FinFET designs, one gate can be used for driving/switching and the other gate can be used for threshold voltage control. It allows the dynamic threshold voltage

control due to electrical coupling of both the front and back gates. The modulation of front-gate threshold voltage can be achieved by applying back-gate voltage biasing. Therefore, it offers more stable SRAM circuits. Also, it is possible to reduce the trade-offs between read and write margin by applying this technique. Thus, the improved device performance, reduced leakage current, stability improvement can be easily achieved by using independent gate FinFET. Cakici *et al.* [CakiT'07] showed that further control on leakage can be achieved by using sleep transistor based source biasing technique with independent gate-based FinFET SRAM. Theoretically, it is preferred that the back-gate devices should be asymmetrically built. Joshi *et al.* [JoshR'07] described the area-efficient row-based back gate biasing scheme for asymmetrical double-gate FinFET. Based on the comparisons, they proved that the FinFET based back-gate biasing to control the V_{th} of device was better than the CMOS body/well biasing. Later on, Kanj *et al.* [KanjR'08] presented a column decoupled SRAM design and revealed the statistical evaluation and yield. Two novel independent-gate FinFET based SRAM cells have been presented by Tawfik *et al.* [TawfS'07]. In their first design, the pull-down transistors are tied-gate transistors, whereas the pull-up transistors and the access transistor are independent-gate FinFETs. By this approach, a 50% enhancement in static noise margin has been reported compared to tied-gate FinFET SRAM cell. In the second design, the technique of V_{th} modulation has been explored by using independent gate access transistor by dynamically tuning the read/write strength. For read and write operation, they proposed two separate data access. The back-gate of access transistors are controlled by a separate write signal (W) and the front-gate is controlled by a read/write (R/W) signal. The threshold voltage of the access transistor is dynamically adjusted by using this technique. The read static noise margin has been enhanced by 92% with this approach. The leakage power reduction is reported as 36% using this IG approach compared to tied-gate approach. Liu *et al.* [LiuZ'08], reported a 17.5% reduction in area compared to tied-gate FinFET using minimum sized independent-gate transistors without affecting the data stability. Endo *et al.* [EndoK'08] proposed a row-by-row V_{th} control for an independent gate based SRAM array. In this design, back gate control lines parallel to the word lines are used to control the V_{th}. In stand-by mode, the threshold voltage of the transistors was increased to reduce the leakage current. During a read or write-access, the threshold voltage was decreased to ensure high drive current. The voltages for the control lines are supplied by level shifters by

converting a row decoder output signal. Endo *et al.* [EndoK'08] fabricated FinFET based SRAM array and reported a drastic reduction in leakage power consumption along with dynamic power consumption by efficiently controlling the back gate.

2.6.3.3 Fin-Thickness, Fin-Height, and Fin-Ratio Optimization

FinFET offers several improvements in SRAM performance, but one need to address many challenges also that arise due to inherently different device architecture. This sub-section discusses the effect of fin thickness and fin height on drain induced barrier lowering (DIBL), threshold voltage, write ability, and read stability of the SRAM cell. For superior circuit/SRAM performance, it is very important to choose the correct/optimized fin configuration. Here, fin configuration means fin height, thickness, fin pitch and the number of fins etc. The SRAM are interconnect dominated circuits; therefore the increase in drive current would be beneficial for memory circuits. It is possible to increase the effective channel width and drive current by increasing the fin height of FinFET. In a joint optimization study of $V_{DD,}$ fin height, and V_{th} on SRAM performance, Ananthan *et al.* [AnanH'06] achieved 87% lower sub-threshold leakage, 50% lower gate leakage, 25% lower dynamic energy, 13% higher static noise margin by using 69% taller fins, 8% lower V_{DD} and 35% higher V_{th}. Furthermore, they reported that increase in fin thickness (T_{fin}) lowers the read stability of FinFET SRAM cell. However, larger T_{fin} increases the yield of write ability or word-line trip voltage. On the other hand, the read stability decreases as the fin height (H_{fin}) increases, but if the T_{fin} is small then the H_{fin} does not have a significant impact on read stability [LeeJ'12]. In one of the studies, Dobrovolny *et al.* [DobrP'12] analyzed the impact of inter-die fin height variations on the SRAM cell wherein they reported that the inter-die fin height variations dominate the overall intra-die variation and both inter-die variation and intra-die variation affect the SRAM cell SNM and write-trip point. Another study [ChenMC'13] reported that a multiple fin-height SRAM cell demonstrates a 25% better static noise margin than single fin-height cell. They used tall fin in pull-down transistor and short fin in pass gate transistor. Cheng *et al.* [ChngH'10] reported that a multi-fin and larger aspect ratio SRAM showed better electrical characteristics than single fin and smaller aspect ratio FinFET. Also, multi-fin FinFET reduces the random dopant fluctuations because of uniform surface potential. On the other hand, Kang *et al.* [KangM'10] demonstrated that two-fin pass gate consumed larger dynamic energy due to the effectively larger gate and drain

capacitances. Therefore, one-fin pass gate would be a suitable choice for SRAM designing with proper surface orientation. Another study on process variation impact on FinFET SRAM reported that the stability of the cell was most susceptible to the fin thickness variation of the access transistor [ShimY'08]. They demonstrated that using multiple fins in pull-down transistor might improve the read SNM under worst case. Sohn *et al.* [SohnC'13] stated that the parasitic capacitance can be lowered by using taller and denser fins. Also, the static power consumption was much larger with taller fins due to higher off-current. Rasouli *et al.* [RasoS'09] reported that the fin thickness below 10 nm (for 22 nm technology) can induce quantum mechanical effect such as structural confinement. Matsukawa *et al.* [MatsT'09] demonstrated that the parasitic resistance is greatly influenced by T_{fin} fluctuations and can be reduced by optimizing the extension doping. An optimization for stability of SRAM has been discussed through silicon fin thickness and fin ratio in [LeksD'07] where they demonstrate that the silicon thickness constraint can be relaxed without affecting the stability of the cell and can reduce the process variability. Also, it has been reported that the reduction of the fin-to-fin variability can be achieved by increasing the number of fins. Besides this, a penalty in terms of 25% increase in area is paid on increasing the number of fins is increased by one or two in access or pull-down transistors.

2.6.3.4 Fabrication Level Optimization

In preceding sub-sections, it is clearly seen that the performance metrics of FinFET based SRAMs can be improved by various device and circuit level approaches. In this sub-section, we focus towards the fabrication level optimization techniques. Kawasaki *et al.* [KawaH'09] discussed the fabrication related challenges and solutions in SRAM cells for 22 nm node and beyond. They reported that the sidewall image transfer (SIT) is an important technique to achieve narrower fin formation. Furthermore, this technique can be advantageous for SRAM circuits to achieve lower line edge roughness (LER). The authors in [KawaH'09] preferred to use plasma doping or solid-phase doping to reduce the threshold voltage mismatch in SRAMs. As we have discussed earlier that the reduction in parasitic resistance is a key factor in improving FinFET device performance. Therefore, the authors [KawaH'09] proposed Source/Drain merged FinFET with diamond shaped epi to improve the parasitic resistance issue. A high-performance 25 nm gate length SRAM cell has been fabricated in [ChngC'09] by optimizing fin extension and embedded

SiGe Source/Drain. The optimized implant and anneal conditions can be used to reduce the extension resistance that in turn improves the fin quality and short-channel effects as well. Liu *et al.* [LiuY'06] reported that the TiN wet etching technique is good to obtain sub-30 nm gate length, taller fins of around 100 nm and symmetrical threshold voltages. Veloso *et al.* [VeloA'09] demonstrated FinFET based SRAM cell by using advanced single-patterning process with full-field EUV and immersion lithography. To achieve good electrical characteristics at V_{DD} down to 0.4 V, the *W* metallization for contact holes and epitaxial raised source/drain (SEG) with double spacer and ultra-thin silicide were also demonstrated. In their later work, Horiguchi *et al.* [HoriN'10] reported that the single gate patterning approach produced weak yield in FinFET SRAM and had a problem in gate pitch control. Therefore, they demonstrated the double gate patterning approach to improve the yield of FinFET SRAM. Kawasaki *et al.* [KawaH'08] demonstrated a single sided ion implantation scheme to reduce threshold voltage variation in FinFET based SRAM. Also, they reported that an undoped channel FinFET based SRAM shows lesser threshold voltage variation compared to the halo-doped FinFET SRAM. Basker *et al.* [BaskV'10] demonstrated a FinFET SRAM cell operating at 0.4 V with good performance metrics. Although, they have used the conventional optical lithography, but managed to aggressively scale fin pitch (40 nm) and gate pitch (80 nm) by using a double-expose, double-etch SIT process. Besides this, they have also used the epitaxial films for conformal doping and reported that it reduces the external resistance by 30%.

2.6.4 Process Variations

Reduced feature size and limited photolithographic resolution cause statistical fluctuations in nano-scaled devices. These fluctuations cause variations in device as well as circuit performance parameters, such as V_{th}, I_{ON}, I_{OFF}, SNM and so forth. These process variations can be inter-die or intra-die, correlated or uncorrelated depending on the fabrication process. This lead to mismatched device strengths and degraded the yield of the die. That is why continued scaling of planar MOSFETs has become so difficult. Therefore, the authors in [DimiS'87, StojN'83a, StojN'83b] have reviewed the failure physics of ICs and their influence on device reliability in early days of scaling.

In planar MOSFETs, a sufficient number of dopants must be inserted in the channel to tackle the SCEs. However, this highly doped channel gave rise to random dopant fluctuations (RDF) that further lead to significant variation in V_{th}. Since FinFETs enable better SCE performance due to the presence of the second gate, they do not need a high channel doping to ensure a high V_{th}. Hence, designers have to keep the thin channel (fin) at nearly intrinsic levels (~10^{15}cm^{-3}). This reduces the statistical impact of RDF on V_{th}. The desired V_{th} is obtained by engineering the work function of the gate material. Undoped/lightly doped channel also ensures better carrier mobility inside the channel. Thus, FinFETs emerged as superior to planar MOSFETs by overcoming a major source of process variation. However, due to its complicated structure and lithographic limitations, FinFET do suffer from other process variations such as gate-edge roughness (GER), fin-edge roughness (FER), grain dependent work-function variations (WFV), interface trap-charges fluctuations (ITC), gate oxide thickness, gate underlap and positive/negative bias temperature instability (P/N-BTI) [WangX'11, MishP'10a, MatsT'09, ChauS'14]. In sub-20 nm technology nodes, process variability has become one of the major concerns in FinFET that can fail-out any circuit/SRAM. Xiong *et al.* [XionS'03] studied the sensitivity on performance parameters to various physical variations in devices designed with a nearly intrinsic channel. Choi *et al.* [ChoiJ'07] studied the temperature variations in FinFET based logic circuits under key structural parametric variations. They showed that even under moderate process variations in gate length and body thickness (T_{fin}), more than 15% thermal runaway was possible in an IC, when primary input switching activity is 0.4. The effect of temperature variation is more severe in SOI FinFETs because the oxide layer under the fin has poor thermal conductivity. The heat generated within the fin cannot easily dissipate in SOI FinFETs. Bhoj *et al.* [BhojA'13a] evaluated the symmetric and asymmetric FinFETs under temperature variation and observed that the asymmetric tied gate FinFET remained best and retained a 100× advantage over the symmetric one at higher temperature. They also plotted the distribution of I_{OFF} under process variations for the symmetric and asymmetric FinFETs. By optimization and/or modelling techniques, statistical variability in SRAM cell has been carried out by many researchers in [EbraB'11, KangM'10, HuVP'11].

2.7 Technical Gaps

Based on the above literature survey, it has been observed that the FinFET devices have emerged as one of the promising devices among the other multi-gate architectures for sub-20 nm nodes. However, the Intel announcement to commercially use the tri-gate FinFET below 22 nm nodes started a race to develop high performance FinFET device/circuits with some performance boosters. After extensive literature survey, the following technical gaps have emerged:

a) As the underlap length is reduced beyond ~10 nm, the relative ON-OFF advantage saturates because of increased S/D series resistance that degrades I_{ON}. Many researchers reported that the use of high-*k* spacers reduces $R_{S/D}$ but it also increases parasitic capacitance. So, there is a strong trade-off between fringe capacitance (C_{fr}) and $R_{S/D}$. Therefore, it is necessary to intelligently use high permittivity spacers that optimize the C_{fr} and $R_{S/D}$ trade-off so as to improve the device performance.

b) Introduction of high-*k* spacers can provide strong fringing-field coupling between the gate and the undoped underlap region that improves the device performance. However, it also increases the fringe capacitance that worsens the circuit delay in digital applications. Therefore, an in-depth analysis of fringe capacitances in high-*k* spacer devices and its impact on basic CMOS logic circuits (inverter and 3-stage ring-oscillator) is critically required.

c) SRAM cells are traditionally one of the most critical circuit components in a SoC and therefore, considerable efforts must be spent to achieve read/write robustness, reduce access time and low power consumption without any cell area penalty. So, it is necessary to explore the proposed spacer engineered architectures for mitigating the read/write conflict in 6T SRAM cell that also improves cell performance metrics.

d) Process variability has emerged as one of the major concerns in sub-20 nm gate lengths. The random variability in device/circuit increases sharply with reduced feature size that can fail out any design. Therefore, it is necessary to explore the device and circuit performance under process variations such as random discrete dopant induced fluctuations (RDF), oxide roughness variations (TOX), and metal grain dependent work-function variations (WFV).

2.8 Summary

In this chapter, an existing literature review of double/tri-gate FinFET devices and its circuit/SRAM performances are discussed. This literature survey helped to identify various technical gaps in this area of research. Through the work presented in subsequent chapters, an attempt has been made to bridge these technical gaps in order to have better device in sub-22 nm technology nodes that fits well for high-performance circuit/memory applications.

CHAPTER 3

Dual-*k* Spacer Device Architecture and its Electrostatics

3.1 Introduction

As FinFET devices are drastically scaled, SCE and leakage currents continue to dominate and affect device performance. Therefore, the large drive current projected by the ITRS for sub-20 nm FinFET devices has not been achieved yet [ITRS]. In sub-20 nm regime, suppression of SCEs can be achieved by incorporating gate-source/drain (G-S/D) underlap regions. In an underlap structure, the dynamic effective channel length (L_{eff}) is significantly longer than the physical gate length (L_G) in weak inversion, while L_{eff} is comparable to L_G in strong inversion [FossJ'03a]. Although, the underlap region helps in reducing SCEs, but at the expense of drive current (I_{ON}) [YangJ'07]. This is primarily because of the increased underlap resistance that starts dominating the total source/drain series resistance ($R_{S/D}$) with an increase in the underlap length (L_{un}). Consequently, the G-S/D barrier restricts the flow of carriers from source-to-drain, even at high gate/drain bias.

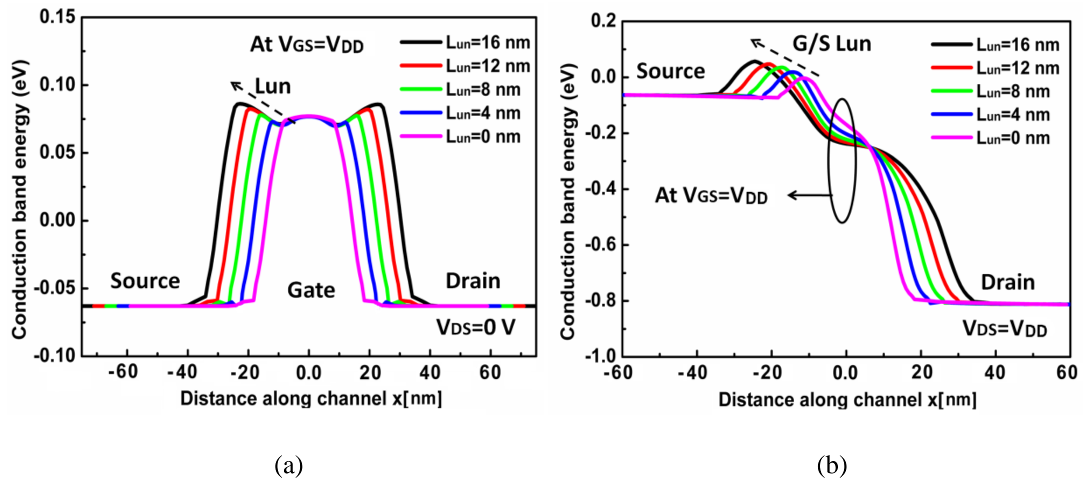


Figure 3.1. Conduction band profile along the channel with increasing underlap lengths (a) at V_{DS}= 0, and (b) V_{DS}=V_{DD}, when V_{GS}=V_{DD}.

Spacer engineering plays a significant role in describing the electrostatics and charge dynamics of the underlap devices. The undoped underlap region increases the total source/drain series resistance that in other words creates barrier (near the gate edges) in OFF-state. This barrier is more prominent with an increase in underlap length as shown in Fig. 3.1(a). With an increase in the drain potential, the underlap barrier on

the drain side reduces without affecting much on the source side (G/S) underlap barrier as shown in Fig. 3.1(b). In large underlap device, this source-side underlap barrier is prominently high that actually restricts the carriers to flow from source to drain in ON-state.

In the past decade, high permittivity (k) spacer materials act as key enabler in enhancing the device performance that provides strong field coupling *i.e.* gate fringe induces barrier lowering (GFIBL) between the gate and the undoped underlap region and hence reduces the raised source/drain series resistance [SachA'08]. This results in a better gate control and improved device performance. However, replacing low-k spacer material with high-k spacer originates two foremost problems related to trap charges and parasitic capacitance that significantly affects the device performance. In general, the high permittivity spacer materials have limited applicability in high-performance digital circuits [ZhaoH'08]. This limitation is imposed due to excessive increase in fringe capacitance (C_{fr}) that in turn worsens the circuit delay/access-time. The other problem is associated with interfacing of high-k material to silicon body which induces trapped charges that severely degrades the carrier mobility due to increased Coulomb scattering at the Si/spacer interface [ColiJ'08]. As k value increases, the mobility degradation will be much higher due to enhanced trap charges. Therefore, it is necessary to diligently use high permittivity spacer so that the electric fringe-field only converges toward the high energy barrier which can help in reducing the extra $R_{S/D}$. This also helps in improving the device and circuit performance in digital domain.

At device level, several researchers have focused towards the integration of high permittivity materials as a gate-oxide and/or spacers [AgraS'08, KoleK'15, JanCH'12, ChenQ'05]. The fringe field phenomenon through the high-k gate dielectric *i.e.* FIBL has been studied by few researchers from device and circuit perspectives as well [MohaN'02, ManCR'07, NirmD'13, RaoVR'04]. There is continuous reduction in dimensions of the device due to scaling which motivates for a comprehensive study of three-dimensional (3D) fringing field due to high-k spacers on both device as well as circuit performance. To the best of our knowledge, none of the research works have ever explored the direct impact of 3D fringe-field in enhancing the dynamic circuit performance using high-k spacers. Moreover, there are no studies which trace the electric flux across spacers of various dielectric constants.

This chapter presents a comprehensive analysis of the effect of high permittivity spacers on underlap tri-gate FinFET. This study helps designer to make effective use of such spacer engineered devices for enhanced performance. Section 3.2 introduces the dual-permittivity (*k*) spacer concept within device. Section 3.3 presents the optimization strategy for proposed symmetric (SymD-*k*) and asymmetric dual-*k* spacer (AsymD-*k*) tri-gate architectures and the simulation methodology adopted to explore the benefits of employing high-*k* spacers in symmetric and asymmetric devices. Section 3.4 provides the proposed methodology of fabricating symmetric and asymmetric dual-*k* spacer FinFETs. The superior ON/OFF-state electrostatics and merits of dual-*k* FinFET over the conventional (single/low-*k* spacer) as well as the purely high-*k* spacer underlap FinFET structure is discussed in section 3.5. An extensive three dimensional (3D) TCAD device simulation examines both ON and OFF-state electrostatics with high permittivity sidewall spacers to reveal the effects of 3D fringing field phenomenon that in turn modulates charge dynamics inside the channel. Furthermore, this section also physically interprets the ON/OFF state electrostatics associated with dual-*k* structure with an increase in inner spacer *k* value. Moreover, section 3.6 distinguishes the competing effects of symmetric and asymmetric dual-*k* spacer structures. This study helps in understanding the favourable field dynamics of their respective electrostatics and its influence on high performance circuit applications. Finally, section 3.7 briefly summarizes this chapter.

3.2 Dual-*k* Spacer Architecture and TCAD Simulation Setup

The optimized dual-*k* spacers can effectively reduce the G-S/D underlap barriers by concentrated fringing field. Apparently, the drain-side barrier in any underlap device inherently reduces by drain bias in ON-state. However, the source-side underlap barrier is almost unaffected by drain bias that in turn restricts the carrier flow from source to drain [as shown in Fig. 3.1(b)]. Therefore, the optimum high-*k* spacer can be effectively used, either on both side (abbreviated as SymD-*k*) to maintain the device symmetry or towards the source-side only to selectively reduce the source-side underlap barrier *i.e.* in form of AymD-*k*S architecture. Due to the limited usage of high permittivity material only on one side, the AsymD-*k*S architecture further helps in reducing the overall trap charges, Miller capacitance (C_{GD}) and the high-*k* mobility degradation in comparison to the symmetric device (SymD-*k*). However, in certain applications where biasing changes dynamically such as pass transistor logic and

SRAM cell, the bidirectional current characteristics of AsymD-*k*S architecture needs equal attention.

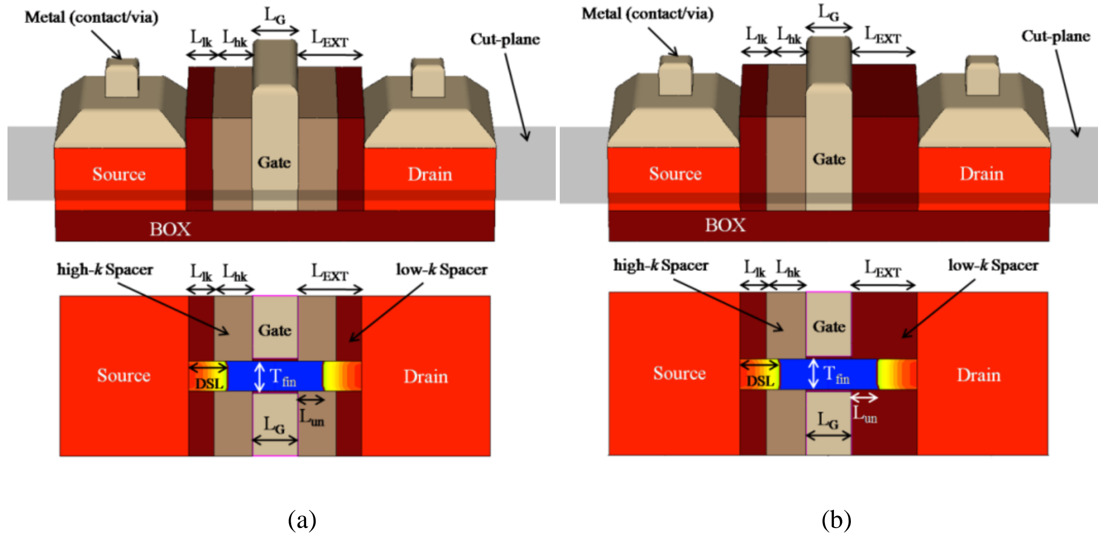


Figure 3.2. 3D and top (2D) view of proposed (a) symmetric, SymD-*k* and (b) asymmetric dual-*k* spacer (AsymD-*k*S) tri-gate FinFETs.

A three-dimensional and top (2D) view of an optimized symmetric and asymmetric dual-*k* spacer tri-gate structures are shown in Figs. 3.2(a) and (b), respectively. These structures are in contrast to the conventional one where a single/low-*k* spacer material is used all over the extension region *i.e.* from the gate edge to S/D edges. Because of the co-existence of both high-*k* and low-*k* spacers in extension region, the architecture is abbreviated as dual-*k* architecture. It consists of an inner high permittivity and an outer low permittivity spacer material. Similarly, the asymmetric structure is termed as AsymD-*k* which has dual-*k* spacer material either at the source or drain side. The asymmetry is introduced with respect to the source and drain terminals. Depending on applied bias condition, the AsymD-*k* structure is further categorized as “AsymD-*k*S” and “AsymD-*k*D”. If a positive potential (for *n*-type FinFET) is applied at the dual-*k* side terminal with respect to the low-*k* side terminal, the structure is called as "AsymD-*k*D" and if the higher potential is applied at the low-*k* side terminal, then the structure is known as "AsymD-*k*S". The "*D*" and "*S*" letter used in device nomenclature stands for drain and source, respectively for reason that higher potential terminal (in *n*-type) act as a drain.

For the sake of comparison, the silicon dioxide (SiO_2, k=3.9) is adopted as a spacer throughout the G-S/D extension region and it is termed as the “conventional” device. On the other hand, if high-*k* material replaces the SiO_2 in the conventional

device, then the device is called as "purely high-k" device. To analyze the effect of high permittivity spacers on underlap FinFET, the inner high-k spacer length (L_{hk}) is varied from the gate edge to source/drain edges with a step of 4 nm for a fixed underlap length (L_{un}) of 8 nm. Note that in SymD-k structure, L_{hk} of 0 nm and 20 nm corresponds to the conventional single/low-k and purely high-k structures, respectively. All the considered architectures in this thesis are summarized in Table 3.1. For high-k spacer materials, Si_3N_4 (k=7.5), HfO_2 (k=22) and TiO_2 (k=40) are considered throughout the work. Except for the spacer permittivity variations presented in this thesis, HfO_2 is taken as the high-k spacer material due to its advanced technology that makes it more feasible from the fabrication point of view.

TABLE 3.1

NOMENCLATURE FOR VARIOUS DEVICE ARCHITECTURES AND THEIR CHARACTERIZATION

Architectures	Characterization
Conventional	Single/low-k spacer throughout G-S/D extension region
SymD-k	Symmetric dual-k spacer
AsymD-k	Asymmetric dual-k spacer either at source or drain side
AsymD-kS	Dual-k spacer at source-side only
AsymD-kD	Dual-k spacer at drain-side only
High-k	Single/high-k spacer throughout G-S/D extension region

The physical and electrical parameters are calibrated to meet the specifications according to the ITRS projections for 14 nm physical gate length (L_G) as summarized in Table 3.2 [ITRS]. Accordingly, the fin thickness (T_{fin}), fin height (H_{fin}) and equivalent oxide thickness (EOT) are adopted as 9.4 nm, 20 nm and 0.72 nm, respectively. The metal-gate work functions are tuned to 4.45 eV for n-type and 4.77 eV for p-type to achieve a requisite threshold (V_{th}) of ~230 mV at a supply voltage of 750 mV. S/D extension region uses Gaussian-doping profiles followed by a lateral doping gradient of 3nm/decade, such that the dopant-segregation length (DSL) is 12 nm. The S/D extension length (L_{EXT}) is taken as 20 nm (*i.e.* greater than the physical gate length). The channel and underlap region are lightly doped with a concentration of 1×10^{16} cm^{-3} to reduce random dopant fluctuations (RDF) [ColiJ'08]. The raised

source/drain regions have been formed to reduce the parasitic resistance associated with thin fins. Moreover, to consider the gate-to-source/drain capacitance, metal contacts are taken. The gate-electrode thickness (T_G) is nearly twice the L_G value [YangJ'07]. The inner high-*k* spacer (L_{hk}) and outer low-*k* spacer length (L_{lk}) are tuned to 12 and 8 nm, respectively for L_{un} of 8 nm. The thickness of buried-oxide (BOX) layer is taken as 50 nm.

TABLE 3.2

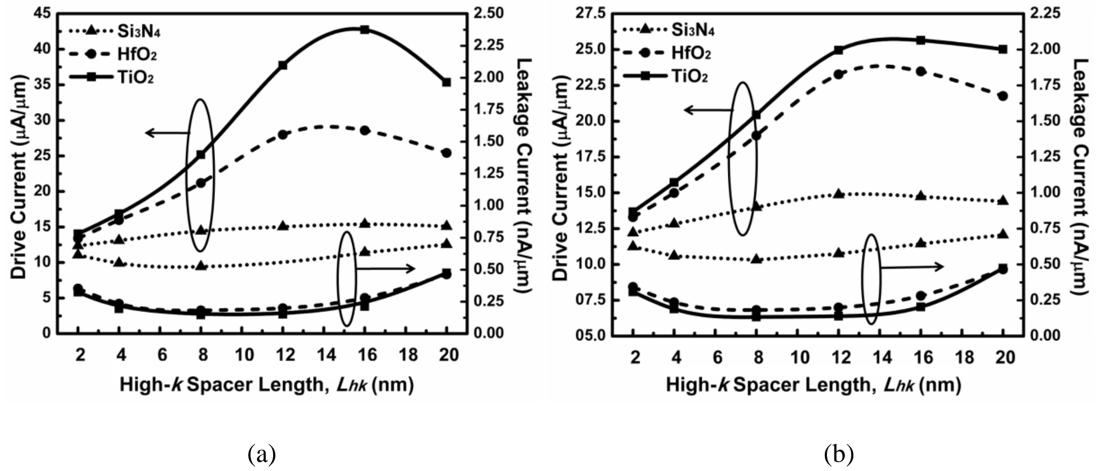
ITRS PROJECTIONS (2012) FOR HIGH PERFORMANCE DEVICE IN YEAR 2017 [ITRS]

Device Parameters	Abbreviations	ITRS Projections Value
Physical Gate Length	L_G	14 nm
Eq. Oxide Thickness	*EOT*	0.72 nm
Fin Thickness	T_{fin}	9.4 nm
Fin Height	H_{fin}	20 nm
Supply Voltage	V_{DD}	0.75 V
Channel Doping	N_A	1×10^{16} cm^{-3}
Source/Drain Doping	N_D	1×10^{20} cm^{-3}
Threshold Voltage	V_{th}	~230 mV

For 3D device realization and extensive mixed-mode circuit simulations, Synopsys TCAD is used [TCAD]. To include the quantum confinement of carriers in thin silicon channel, the quantum potential model is adopted instead of only drift-diffusion. The direct tunneling model is included that considers all the gate leakages including the edge-gate direct tunneling current. The Philips unified mobility model is enabled that accounts for both impurity and carrier–carrier scattering mechanisms. Besides this, the high-*k* Lombardi mobility model has been activated to account high-*k* mobility degradation at the Si/spacer interface at high transverse electric field. In ultra-scaled devices at high electric field, the carrier drift velocity is no longer proportional to the electric field, instead, the velocity saturates to a finite speed v_{sat}. Therefore, the *Canali* model is enabled to account for the same.

3.3 Inner High-k Spacer Length Optimization

For an underlap structure, introduction of high permittivity (k) spacer material modulates the charge dynamics in the underlap regions. For an abrupt junction, the inner high-k spacer extends up to the junction [NandA'12] but such a profile is unrealistic from the fabrication point of view. Moreover, the variability issues with low straggle have also become prominent. For Gaussian lateral extension of S/D, the device performance in tri-gate FinFET largely depends on the underlap length and lateral doping straggle (σ_L) [ZhaoH'08]. If high permittivity materials are used as spacers to enhance the device performance, then its permittivity and length should be carefully optimized. This section demonstrates the optimization strategy of inner high-k spacer length to maximize the proposed device performance.



(a) (b)

Figure 3.3. Effect on drive and sub-threshold leakage current in (a) SymD-k and (b) AsymD-kS device structures as a function of L_{hk} with different high-k permittivity materials.

Fig. 3.3 (a) and (b) plots the drive and sub-threshold leakage current in SymD-k and AsymD-kS architectures, respectively as a function of high-k spacer permittivity and length varied from gate edge (L_{hk}= 0 nm) to source and/or drain edges ($L_{hk} = L_{EXT}$ = 20 nm) for a fixed L_{un} of 8 nm. It is observed that in both the SymD-k and AsymD-kS architecture, the I_{ON} increases with an increase in L_{hk} until an optimal point of 12 nm is reached. Beyond this point, I_{ON} starts degrading. The behavior can be easily understood by the two-dimensional electron-density variations in silicon film as a function of inner high-k spacer length as shown in Fig. 3.4. In this, the L_{hk} is also varied from the gate edge to S/D edge with a step of 4 nm.

It is observed from the conventional device [Fig. 3.4(a), L_{hk} = 0 nm] that the

underlap and its nearby laterally diffused regions have low carrier concentration hence an energy barrier is formed. This barrier restricts the carrier flow from source to drain that necessitates the usage of high-k spacer material. The energy barrier is reduced by gate induced fringe field lines that enhance the drive current. Figs. 3.4(b-d) depicts that the carrier concentration increase beneath the spacer interface with an increase in L_{hk} till this length reaches a value of 12 nm. The increase in I_{ON} (shown in Fig. 3.3) is due to this modulation of carrier concentration in the underlap and its nearby lightly doped region. The fringe-field lines originate from the gate and travels through the inner high-k spacer. Due to the difference in spacer permittivity (inner/outer spacer k values), the field lines converge at the interface and terminate underneath the high-k/low-k spacer interface region. Hence, more charges accumulates under the inner/outer-spacer interface that leads to reduction in underlap barrier, thereby resulting in higher I_{ON}. As the inner spacer permittivity increases, more convergence of field lines occurs and thereby increases the charge density under the dual spacer interface. Therefore, higher field beneath interface results in higher carrier concentration and hence a higher ON current.

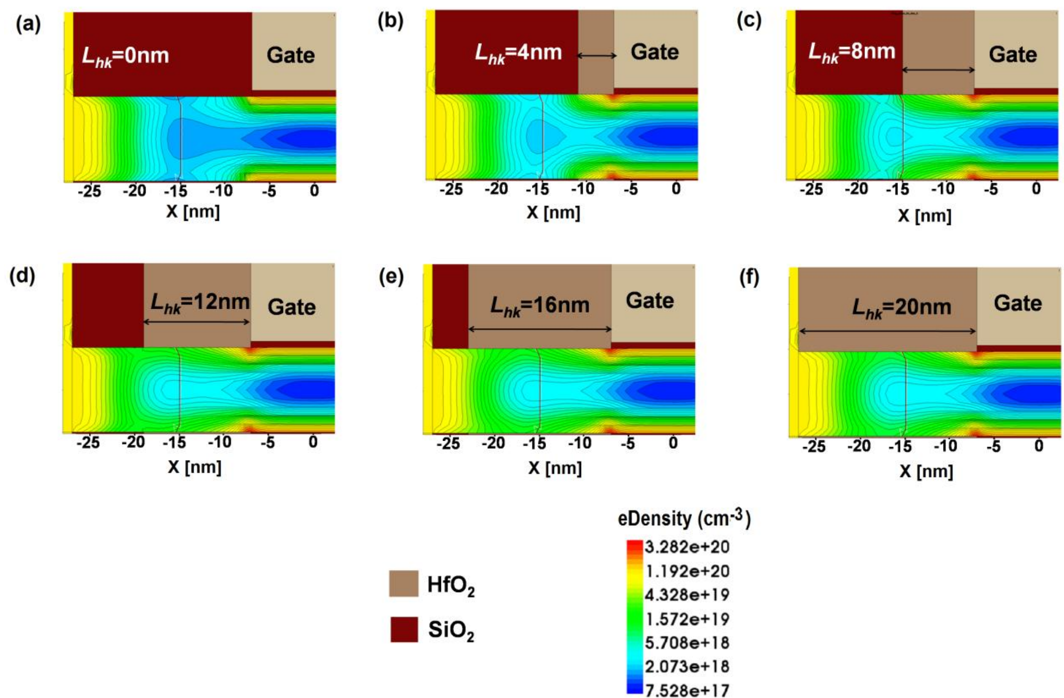


Figure 3.4. Variation of electron-density at the Si/spacer interface (source side) for $V_{\mathrm{GS}} = V_{\mathrm{DD}}$ and $V_{\mathrm{DS}} = 0$ V as a function of L_{hk}.

However, beyond an optimum value of L_{hk}= 12 nm, the I_{ON} starts decreasing due to spreading of fringing field lines. These fringing-field lines now falls on laterally

diffused S/D region that already has very high carrier concentration. Hence, the intensity of fringing-field lines on underlap and its nearby lightly doped region is comparatively reduced. Therefore, the carrier density slightly reduces that result in lower I_{ON} in comparison to the drive current at the optimum point. The measured electron-density values ($\times 10^{18}$ cm^{-3}) at high/low-*k* interface (at $x = \pm 19$ nm) are 3.24, 15.58 and 11.2 for L_{hk} of 0 [Fig. 3.4(a)], 12 [Fig. 3.4(d)], and 20 nm [Fig. 3.4(f)], respectively. Therefore, placement of high-*k* spacers beyond the highly doped laterally diffused area is not required that may otherwise lead to higher trap charges and unnecessarily higher fringe capacitances. The difference in spacer permittivity at interface region changes the electric field path that results in superior electrostatics in OFF state as well.

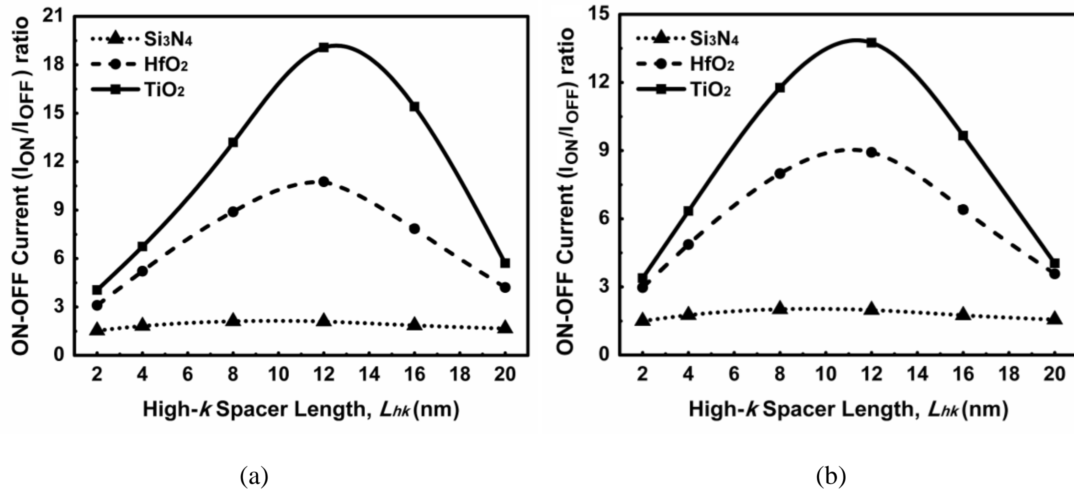
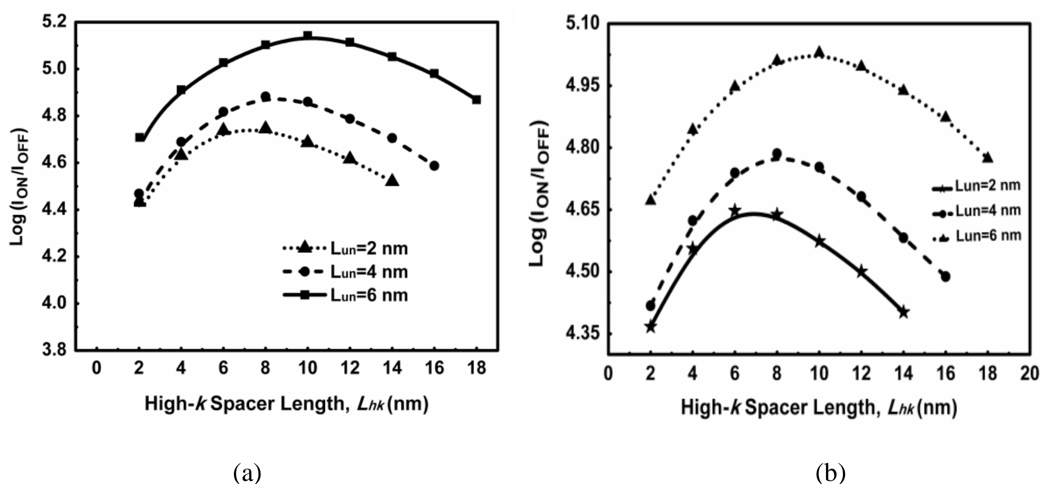


Figure 3.5. Effect on I_{ON}/I_{OFF} ratio in (a) SymD-*k*, and (b) AsymD-*k*S device structures normalized with respect to conventional as a function of L_{hk} with different high-*k* permittivity materials.

Fig. 3.5(a) and (b) plots the I_{ON}/I_{OFF} current ratio variations in SymD-*k* and AsmD-*k*S architectures, respectively as a function of L_{hk} for with different spacer permittivity materials. Similar to the ON and OFF characteristics, it is also observed that the I_{ON}/I_{OFF} current ratio increases sharply with L_{hk} upto an optimal point of 12 nm with an increase in inner spacer permittivity and beyond this it starts decreasing. The I_{ON}/I_{OFF} trends of proposed dual-*k* architectures are mainly due to the I_{ON} characteristics. Therefore, to obtain best performance, the dimensions of inner high-*k* spacer (L_{hk}) and outer low-*k* spacer length (L_{lk}) are optimized to 12 nm and 8 nm, respectively. In other words, for a fixed value of σ_L and L_{un}, a maximum I_{ON}/I_{OFF} can be achieved by having an extended high-*k* spacer length of 4 nm than the underlap length. It is also observed that both SymD-*k* and AsymD-*k*S structure outperforms the

purely high-k structure (*i.e.* SymD-k device when L_{hk} = 20 nm).

Fig. 3.6 shows the variation of I_{ON}/I_{OFF} with L_{hk} for different L_{un}. It is observed that the dual-k spacer concept (for both symmetric and asymmetric) and its optimization strategy holds good for smaller underlap lengths also. It shows the I_{ON}/I_{OFF} ratio trends for L_{un} = 2 nm, 4 nm and 6 nm keeping all the other parameters constant. It is observed from the obtained trends that for different underlap lengths; only the inner high-k spacer length has to be changed. For optimal point in L_{un} of 2, 4 and 6 nm, the L_{hk} should be 6, 8 and 10 nm, respectively that suggests L_{hk} to be 4 nm more than the underlap length. As the underlap length increases, the I_{ON}/I_{OFF} ratio will increase with an improved DIBL and subthreshold-swing (SS).



(a) (b)

Figure 3.6. Shifting of maximum I_{ON}/I_{OFF} point with different underlap values.

3.4 Fabrication Methodology of SymD-k and AsymD-kS FinFETs

This section briefly provides the proposed methodology of fabricating dual-k spacer architectures under study. The key process steps involved in fabricating the proposed SymD-k and AsymD-kS device architectures are the dual-k spacer technology for creating an underlap region at S/D as depicted in [AndeB'06] and the high-k dielectric spacer patterning as used in [XionZ'04]. Both the SymD-k and AsymD-kS tri-gate FinFET fabrication flow starts with either bulk or SOI wafers for fins formation with required thickness and height. Thereafter, channel doping is performed by using a masked ion-implantation and a sacrificial oxidation is employed prior to gate oxidation to eliminate etch damages. Next, the gate dielectric is grown and metal gate is deposited with requisite work-function. It is appropriate to tune the threshold voltage of the structure by using a gate material that has proper work

function. After gate formation, high-k (preferably HfO_2) offset spacers are formed on both sides, to achieve symmetric doping profiles and underlap lengths. Thereafter, S/D extension regions are formed after the high-k offset spacer using low-energy implantation. Subsequently in SymD-k structure, the raised S/D region is grown by using selective epitaxial growth. It helps to reduce the parasitic resistance associated with thin fins. The thermal anneals are used for dopant activation. At last, the silicidation and metallization is carried out.

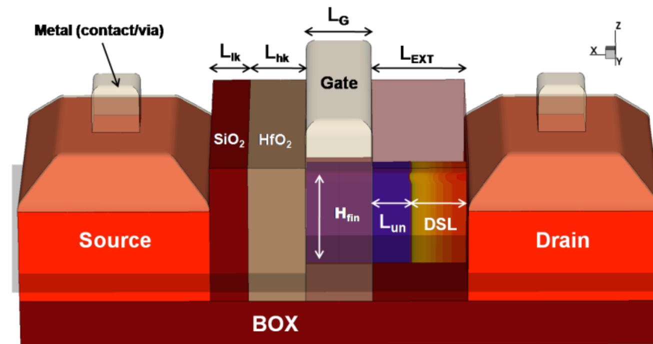


Figure 3.7. 3D view of asymmetric dual-k spacer at source (AsymD-kS) tri-gate FinFET.

Because of symmetric nature, the SymD-k architecture is quite simpler to fabricate than its asymmetric counterpart. Asymmetric dual-k spacer tri-gate (AsymD-kS) FinFET architecture consists of an optimized inner high-k and an outer low-k spacer material only at the source-side, as shown in Fig. 3.7. Therefore, the major fabrication challenges associated with the AsymD-kS device is to form asymmetric dual-k spacer along with the symmetrical underlap regions on both sides. Several researchers over the past years have proposed the method used for fabricating single and/or double dielectric asymmetric spacers [ChngK'11], but it is intentionally used to form unequal Source/Drain (S/D) underlap regions. Symmetrical S/D underlap regions can only be formed by using symmetrical spacers that provide an offset of dopant implant. Fig. 3.8 illustrates the proposed process flow of introducing two spacers only on one of the source or drain sides with equal underlap regions on both sides.

After the gate formation, high-k spacers are formed on both sides that provide the offsets. S/D extensions are formed using tilt angle implants to achieve symmetric doping profiles and underlap values. Thereafter, a photo resist layer is formed over the structure. This photo resist mask and the gate structure shield the source side inner high-k spacer from damage by the angled ion-implant [LeeBH'04]. The angled ion-implant is the key technology to selectively damage the unprotected high-k spacer so

as to subsequently fabricate inner high-*k* spacer at source-side [WeiA'08]. Then the damaged spacer (*i.e.* drain-side high-*k* spacer) is subsequently removed by reactive ion etching (RIE). Now, we have a source-side high-*k* spacer with equal underlap lengths. The low-*k* (SiO_2) spacers are formed over the remaining portions and then, the raised S/D region is grown by selective epitaxial growth. Thereafter, the annealing, salicidation and metallization steps are performed.

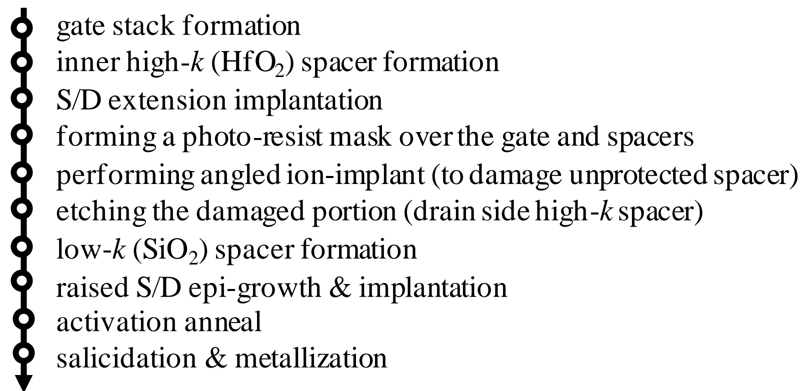


Figure 3.8. The proposed fabrication flow for AsymD-*k*S tri-gate FinFET structure.

3.5 Electrostatics and Merits of Dual-*k* spacer FinFETs

For an underlap structure, introduction of optimum high permittivity (*k*) spacer material modulates the charge dynamics in the underlap and channel as well. This section demonstrates the unique properties, merits and electrostatics associated with the proposed symmetric (SymD-*k*) and asymmetric dual-*k* (AsymD-*k*S) FinFET structures. The proposed dual-*k* device architectures have interface region (high-*k*/low-*k*) that makes it different from the conventional single/low-*k* and purely high-*k* structures. This interface region mainly improves the electrostatics of the proposed architectures as discussed in section 3.3. The difference in spacer permittivity at interface region changes the electric field path that results in superior electrostatics in both ON and OFF-state. To better understand both the symmetric and asymmetric dual-*k* architectures, it is necessary to first analyze them separately. Thereafter, both the proposed SymD-*k* and AsymD-*k* architectures are compared to distinguish the competing effects of high permittivity spacers amongst them.

3.5.1 Symmetric Dual-*k* (SymD-*k*) Tri-gate Architecture

The optimized symmetric dual-*k* spacer architecture, abbreviated as “SymD-*k*” consists of an inner high-*k* and an outer low-*k* spacer material on both source and

drain sides. The TCAD drawn schematic of the same is shown in Fig. 3.9. It sharply differs from the architecture of "conventional" and "high-*k*" structure; where a single low-*k* and high-*k* spacer material, respectively is used throughout the extension region.

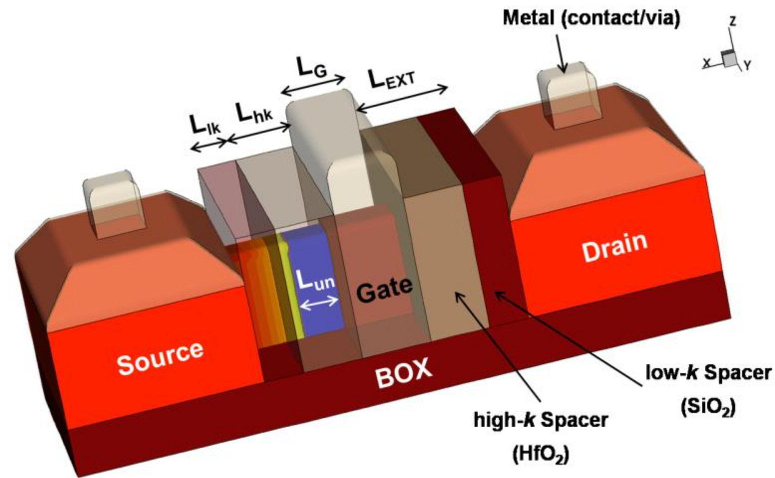


Figure 3.9. 3D-view of symmetric dual-*k* spacer (SymD-*k*) tri-gate FinFET.

This sub-section demonstrates the brief electrostatics and merits associated with the SymD-*k* FinFET over the conventional and purely high-*k* structures considering HfO_2 as inner high-*k* spacer material. In comparison to the conventional and high-*k* spacer FinFETs; the SymD-*k* FinFET structure displays a higher conduction band edge under the gate region at V_{GS}=0 as observed in Fig. 3.10. It is because of the subdued influence of drain electric field on the channel that substantially reduces the sub-threshold leakage current.

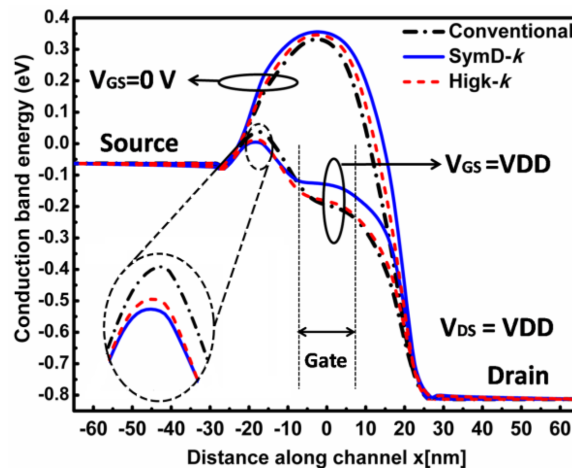


Figure 3.10. Conduction band profile along the channel for conventional, high-*k* and SymD-*k* *n*-FinFET structures at V_{GS} = 0 and V_{DD} when V_{DS} = V_{DD}.

To better understand the superior OFF-state electrostatics, Fig. 3.11 presents the electric-field contours at $V_{DS} = V_{DD}$, $V_{GS} = 0$ V in SymD-*k* and high-*k* structures. It clearly demonstrates that when the SymD-*k* device is in OFF-state (V_{DS}=V_{DD}, V_{GS}=0 V), most of the electric field lines terminates at/near the interface (high/low-*k* spacer) region and thereafter the field intensity reduces as one move towards the channel region. While in purely high-*k* device, the drain-field intensity in the underlap and channel region is larger than the proposed SymD-*k* device thereby influencing the channel region to a greater extent. Furthermore in the channel region of SymD-*k*, it is observed that the influence of drain-field reduces even more with a further increase in inner-spacer permittivity. This results in higher conduction band edge (CBE) in OFF-state for SymD-*k* device than high-*k* device.

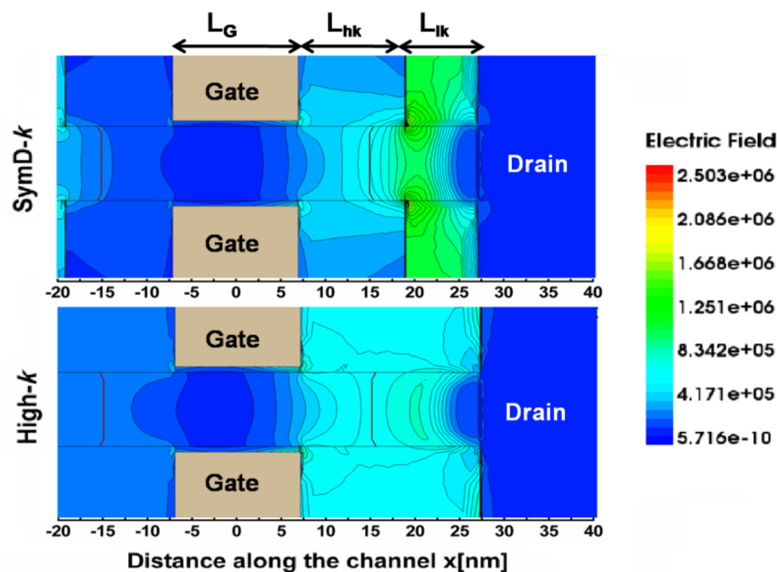
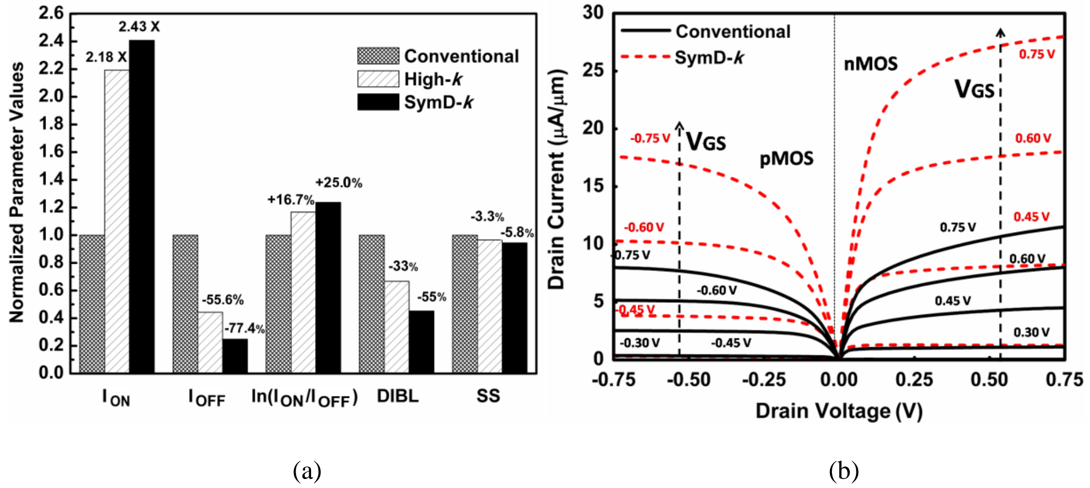


Figure 3.11. The electric-field contours (*xy*-plane cutting at H_{fin}=10 nm) in OFF-state that demonstrates the influence of drain-field on underlap and channel region in SymD-*k* (top) and high-*k* devices (bottom).

Moreover, in ON-state (V_{GS}=V_{DS}=V_{DD}), the increased fringing-field produces an accumulation of carriers in the underlap region through the inner high-*k* spacer that evidently lowers the series resistance. This barrier lowering permits slightly higher injection of charge carriers into the channel. Furthermore, the barrier directly under the channel is lowered to a lesser extent by the drain bias in SymD-*k* than in the conventional; hence the electrostatic integrity increases that reduce SCE. In addition, the lower drain-field influence on the underlap and channel region results in reduced DIBL. Influence of drain field reduction depends upon the type of inner high-*k* spacer

used. With a higher inner spacer permittivity, the difference in underlap barrier for SymD-*k* and high-*k* devices is even more significant that will be discussed later in this chapter. Further, it is observed that the CBE barrier which is directly under the gate increases with an increasing inner spacer *k* value, but it does not affect the I_{ON} unless it is significantly higher than the underlap barrier. Once the carriers cross the G-S underlap barrier, they can be easily transported to the drain end.



(a) (b)

Figure 3.12. (a) Design metrics comparison among conventional, high-*k* and SymD-*k* *n*-FinFETs. (b) I_D-V_{DS} comparison between conventional and SymD-*k* FinFET structure with increasing V_{GS}.

Fig. 3.12(a) examines the device performance parameters to reveal the effects of fringing-fields through the inner high-*k* spacer. For SymD-*k* FinFET (with HfO_2 as inner high-*k* spacer), the drive current increases 2.4 ×, with an OFF-state leakage current (I_{OFF}) reduction of nearly 77% as compared with the conventional one. Moreover, the SymD-*k* structure shows 25% improvement in $\log_{10}(I_{ON}/I_{OFF})$, with reduced DIBL (~55%) and sub-threshold swing (~5.8). It is also observed from Fig. 3.12(a) that the proposed SymD-*k* device outperforms purely high-*k* spacer device in terms of all the performance metrics. The output characteristics of the proposed device compared with the conventional structure is plotted in Fig. 3.12(b). The results depict that, the drain current for a given V_{GS} in saturation region is almost constant for SymD-*k* device compared to the conventional and hence larger output impedance (or, lower output conductance) is achieved.

3.5.2 Asymmetric Dual-*k* (AsymD-*k*) Tri-gate Architecture

In asymmetric dual-*k* spacer (AsymD-*k*) architecture, the optimal inner high-*k* spacer material is used only at the source-side targeting to reduce the G-S underlap

barrier. The asymmetric characteristics are measured by applying the bias on both the terminals as discussed earlier in section 3.2. To implement CMOS logic gates, the asymmetry with respect to S/D does not affect its functionality, although the power and delay metrics might get affected. Asymmetry introduced with respect to S/D terminals could be beneficial in circuits that uses pass transistors such as 6T SRAM cell that faces a trade-off between read and write stabilities. Therefore, the proposed asymmetric dual-*k* spacer architecture helps in mitigating the read/write conflict. This sub-section describes the unique electrostatics and properties associated with the AsymD-*k* structure. Various advantages of the AsymD-*k*S over the conventional single-*k* spacer FinFET are also discussed.

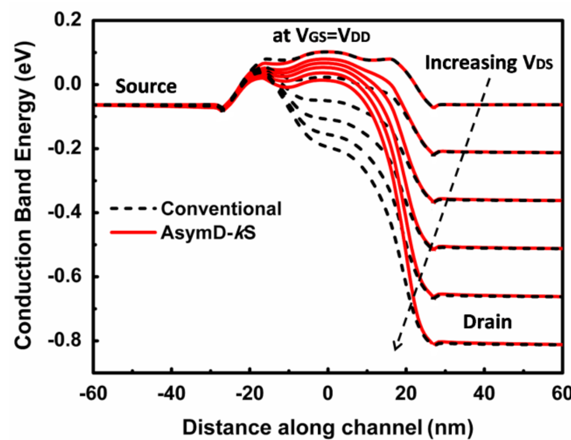


Figure 3.13. CBE profile of the conventional and AsymD-*k*S devices with increasing V_{DS} at V_{GS}=V_{DD}.

Fig. 3.13 shows the conduction band energy with increasing drain to source potential (V_{DS}) of conventional and AsymD-*k*S FinFET structures at V_{GS}=V_{DD}. It is observed that the CBE barrier directly under the gate is lowered to a lesser extent by the drain bias in AsymD-*k*S than conventional, hence the electrostatic integrity increases. In AsymD-*k*S structure, the increased source coupling competes with the gate to keep the channel potential near zero volts, illustrating how source-side injection governs the drain current in short device and reduces the effect of drain potential directly under the channel [KencD'00]. In other words, the gate voltage accumulates electrons (holes) in the *n*-type (*p*-type) device on the source-side through the inner high-*k* spacer. This evidently lowers the source series resistance and accounts for the injection of carriers into the channel. Reduced influence of drain field depends on the type of inner high-*k* spacer used at the source side. The barrier directly under the gate increases with increasing source side inner spacer *k* value while maintaining low-*k* spacer on the drain side.

Fig. 3.14 shows the variation of CBE profile along the channel for conventional, AsymD-*k*S and AsymD-*k*D *n*-FinFET structures at V_{GS}=0 and V_{DD} when V_{DS}=V_{DD}. It is clear from the CBE profile that AsymD-*k*S structure displays the highest conduction band edge under the gate region at V_{GS}=0 that substantially reduces the sub-threshold leakage. When potential is applied to the gate terminal, conduction band edge of the channel near the source (under G-S interface) reduces more in AsymD-*k*S as compared to the other two structures, hence ON-current increases. Less barrier lowering is observed throughout the channel region that means better electrostatic control of the gate over channel and hence helps in reducing SCEs.

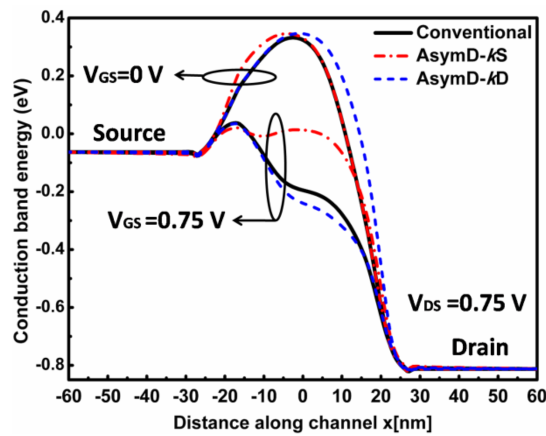


Figure 3.14. Variation of CBE along the channel for conventional, AsymD-*k*S and AsymD-*k*D *n*-FinFET structures at V_{GS}=0 and V_{DD} when V_{DS}=V_{DD}.

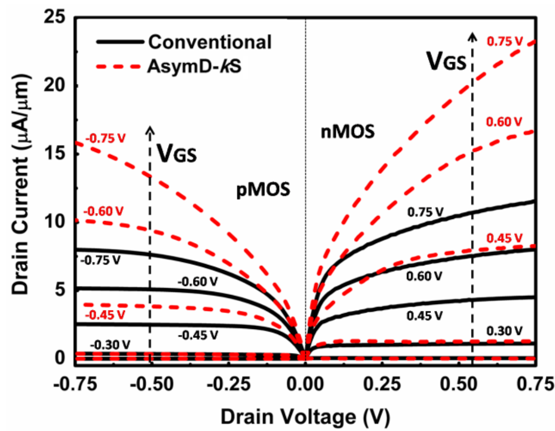


Figure 3.15. I_{DS}-V_{DS} comparison between conventional and AsymD-*k*S FinFET structure with increasing V_{GS}.

AsymD-*k*D FinFET also presents marginally better results than the conventional one. The output characteristics of the proposed AsymD-*k*S device compared with the conventional structure is shown in Fig. 3.15 at different V_{GS} ranging from 0 V-0.75 V (V_{DD}) with a step of 0.15 V.

3.5.3 Dual-*k* FinFETs with Different Spacer Permittivity

It is explained earlier in section 3.3 that the high-*k* spacer length should be limited only upto a region where the strong fringe field lines are able to generate higher carrier density especially in underlap and nearby lightly doped region. Increasing the high-*k* spacer length further will not derive any benefit in terms of carrier density; instead it will increase the fringe-associated capacitance ($C_{if,}$ C_{of}). Thus, L_{hk} should be optimized in such a way that the fringe-field lines concentrates only on the underlap barrier. This can help in reducing both the $R_{S/D}$ and the C_{fr} component of total gate capacitance in comparison to the purely high-*k* device (where $L_{lk} = 0$, $L_{hk} = L_{EXT}$) that can result in better device and in turn circuit delay performance.

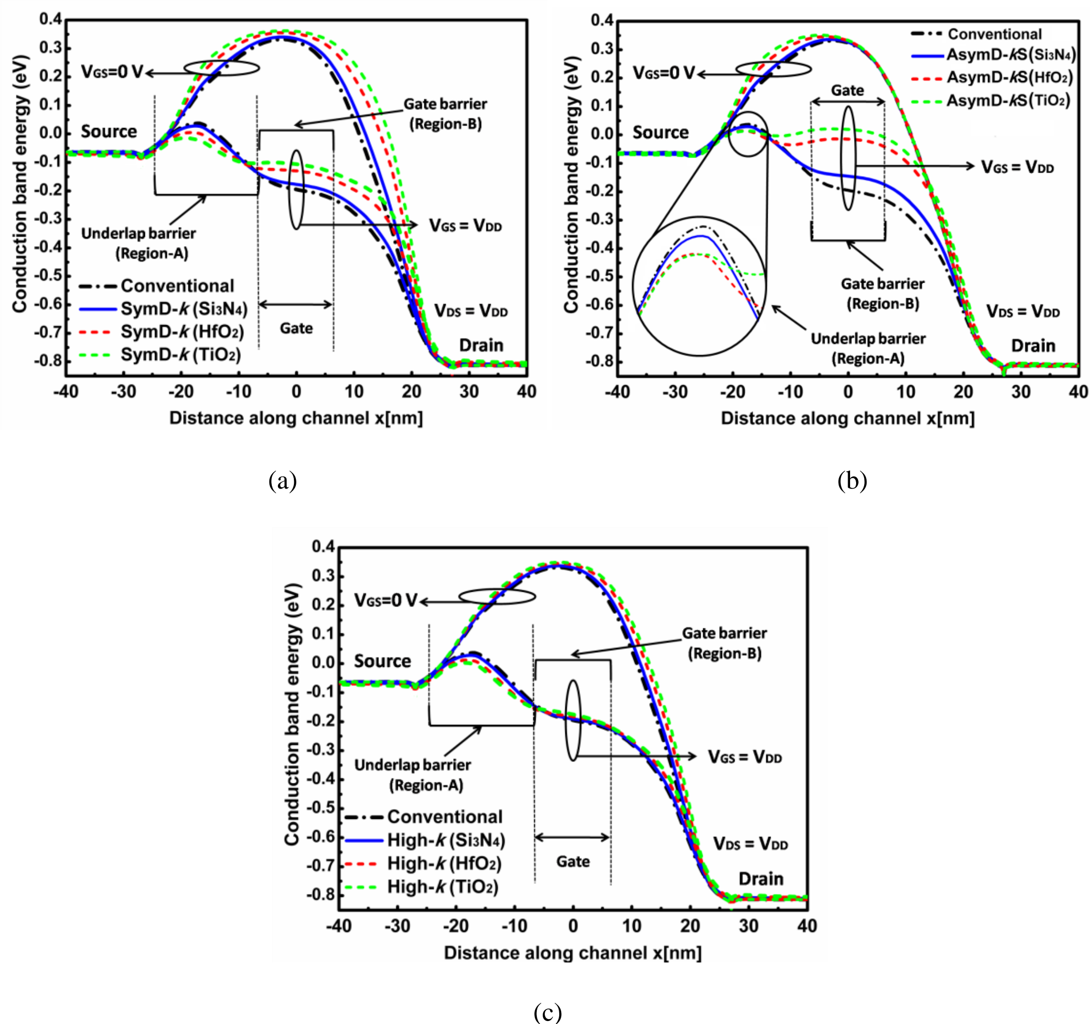


Figure 3.16. CBE profile along the channel (*xy*-plane cut at H_{fin}=10 nm) for (a) SymD-*k*, (b) AsymD-*k*S, and (c) high-*k* FinFET structures in ON and OFF-state with increasing spacer permittivity.

In general, the high permittivity (*k*) spacer material modulates the underlap barrier [SachA'08]. While in proposed dual-*k* spacer, the fringing field modulates not only the

underlap barrier but it also affects the charge dynamics within the channel. This section demonstrates the brief electrostatics, merits, and the current characteristics associated with the dual-*k* spacer FinFET architectures with an increase in inner spacer permittivity. In comparison to the conventional one, Fig. 3.16 shows the conduction band energy profile along the channel of SymD-*k*, AsymD-*k*S, and purely high-*k* device architectures with different inner high-*k* spacer materials at a *xy*-plane cutting H_{fin}=10 nm. As expected, in OFF-state (when V_{GS} = 0 V, V_{DS} = V_{DD}), the conduction band edge is increasing with an increase in inner spacer permittivity that reduces the sub-threshold leakage current. Moreover, in ON-state, the gate fringing field lines through the inner high-*k* spacer reduces the underlap barrier that leads to a higher I_{ON}. Similar to purely high-*k* device, it is observed that the underlap barrier (Region-A) decreases in both SymD-*k* and AsymD-*k*S device architectures with an increase in inner spacer permittivity. On the other hand, the conduction barrier (in ON-state) directly under the gate (Region-B) increases in both SymD-*k* and AsymD-*k*S [shown in Fig. 3.16(a) and (b)] which otherwise remains same in high-*k* device [SachA'08] even though the inner spacer permittivity is increased substantially [Fig. 3.16(c)]. It is because of the favorable field dynamics at the interface of source-side high-*k*/low-*k* spacer regions spacer that effectively subdued the influence of drain electric field on the channel that improves the short channel characteristics.

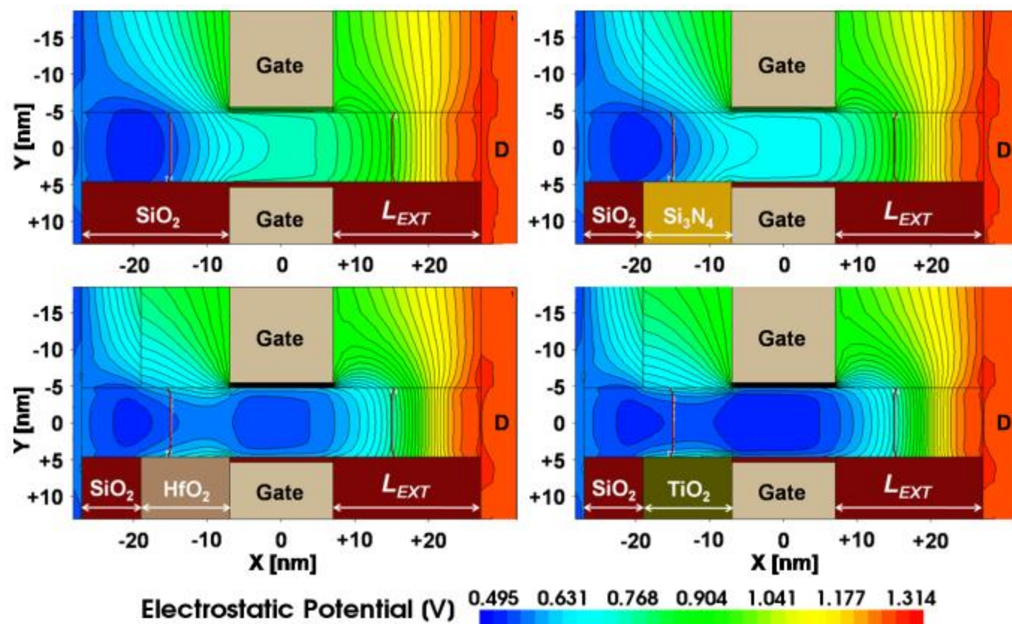
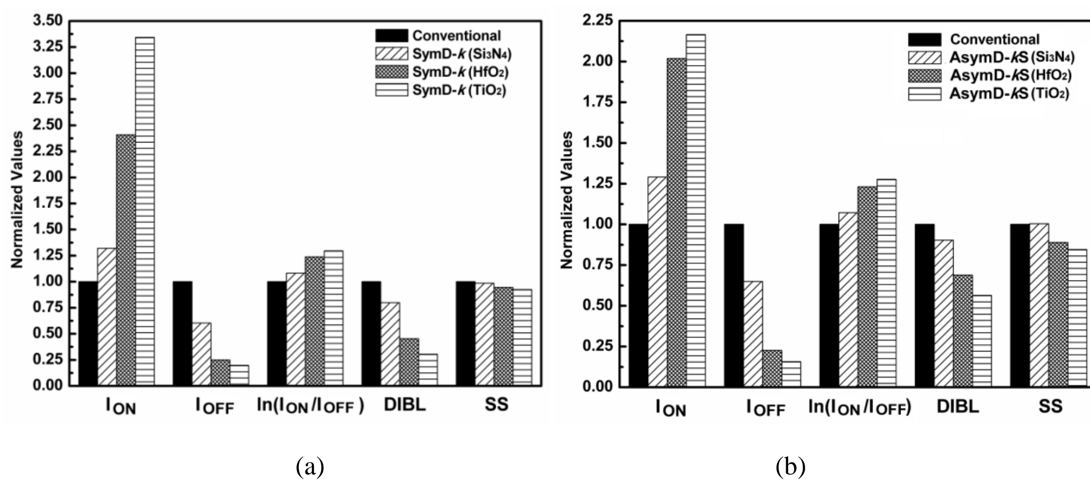


Figure 3.17. The variation of electrostatic potential at the spacer interface and inside the channel (in ON-state) with increasing high-*k* spacer permittivity.

To better understand this, Fig. 3.17 shows the variation of electrostatic potential at the source-side spacer interface and inside the channel (in ON-state) with increasing spacer permittivity. It is observed that the equi-potential lines deviates at the spacer interface in ON-state. As the inner-spacer permittivity increases, the concentration of equi-potential lines at the interface of inner spacer and channel region increases that ultimately results in an increase of I_{ON}. However, the inner spacer permittivity can be increased only upto a level wherein the Region-B barrier does not attain a level above Region-A level *i.e.* satisfying the following condition:

$$Barrier\ (Region\text{-}B) \leq Barrier\ (Region\text{-}A)$$



(a) (b)

Figure 3.18. (a) SymD-*k*, and (b) AsymD-*k*S device performance improvement in comparison to conventional FinFET with different inner spacer permittivity.

The improvement in digital performance metrics using SymD-*k* and AsymD-*k*S structures over the conventional FinFET with increasing spacer permittivity is shown in Fig. 3.18(a) and (b), respectively. Compared to the conventional one, SymD-*k* (AsymD-*k*S) FinFET shows 1.3-3.3 × (1.3-2.2 ×) improvement in drive current with an almost 40-80% [35-84%] reduction in OFF-state leakage current (I_{OFF}) when inner spacer permittivity (*k*) is varied from 7.5 to 40. Moreover, the SymD-*k* (AsymD-*k*S) structure with TiO_2, k =40 shows upto 29.6% (27.7%) improvement in $\log_{10}(I_{ON}/I_{OFF})$, with a reduced DIBL and sub-threshold slope of 69% (43.5%) and 7.5% (15.4%), respectively. Therefore, SymD-*k* and AsymD-*k*S devices with higher inner-spacer permittivity comprehensively outperform the conventional, high-*k* and dual-*k* devices with lower inner spacer permittivity.

3.6 A Comparative Analysis between SymD-*k* and AsymD-*k*S Architectures

This section provides an in-depth analyses of the various competing effects of high-*k* spacer (HfO_2) implemented on source and/or drain side. Fig. 3.19 compares the CBE profile along the channel among the conventional, SymD-*k*, AsymD-*k*S, and AsymD-*k*D *n*-FinFET structures in ON and OFF-states.

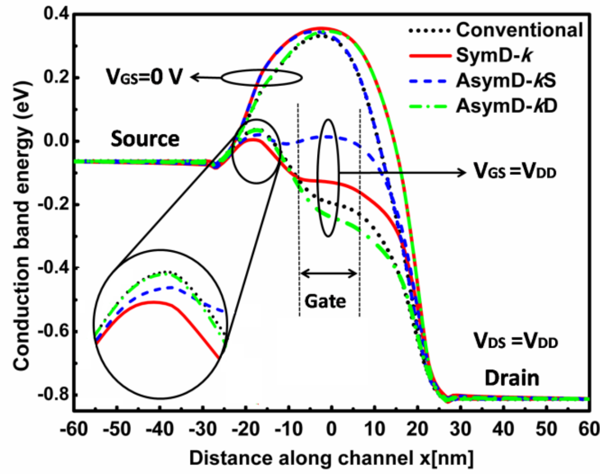


Figure 3.19. Conduction band profile along the channel for conventional, SymD-*k*, AsymD-*k*S and AsymD-*k*D *n*-FinFET structures at V_{GS}=0 and V_{DD} when V_{DS}=V_{DD}.

It is observed that all the considered dual-*k* spacer devices (symmetric as well as asymmetric) exhibits higher CBE barrier in OFF-state over the conventional single/low-*k* device that encouragingly results in lower sub-threshold current. Both SymD-*k* and AsymD-*k*S device exhibits almost same improvement in terms of OFF-state electrostatics. The major differences in CBE profile among the considered structures are observed under the gate region in ON-state. The CBE profile or charge density is prominently affected within the channel. This is due to the spacer placement and the field dynamics at high/low-*k* spacer interface.

From this, an important observation is made that the CBE barrier (in ON-state) of AsymD-*k*S directly under the gate is much higher in comparison to other devices that signifies a subdued influence of drain field. Similarly, the drain influence in AsymD-*k*D structure increases as the gate fringe lines couples with drain fringe lines and therefore, strengthens the vertical electric field at G-D edge. Consequently, the drain field completely controls the channel thereby, reducing the gate electrostatic control in comparison to the conventional device that is not often preferable by device

engineers. The combinational effect of the two asymmetric structures can be observed in SymD-*k* architecture wherein the gate control increases that reduces the underlap barrier resulting in increased drive current.

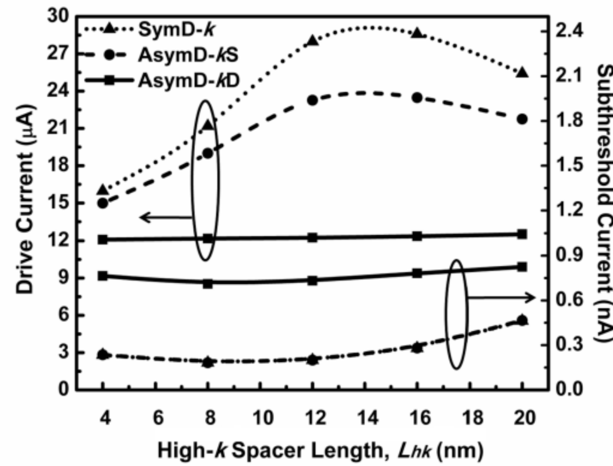
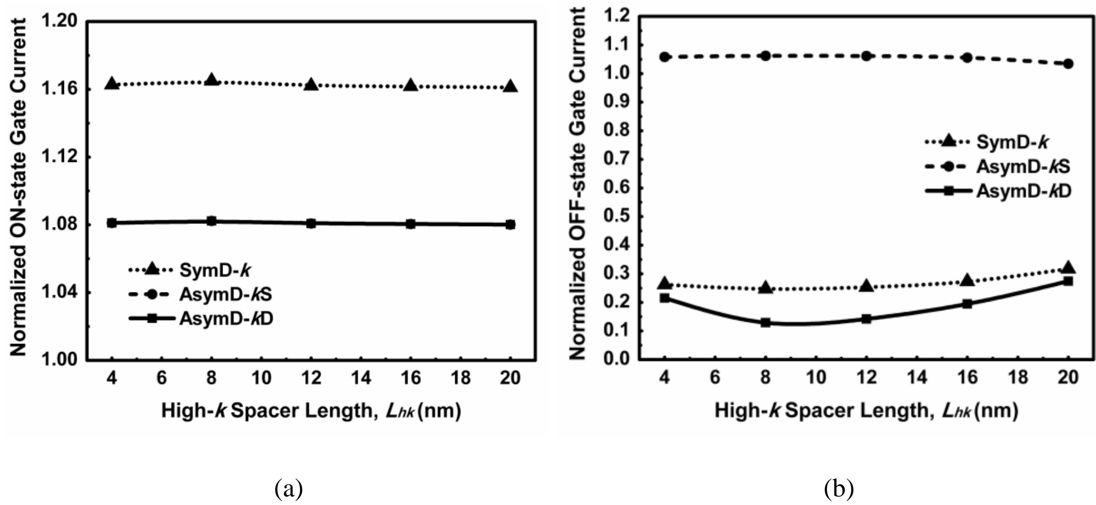


Figure 3.20. Effect on drive current and subthreshold current in SymD-*k*, AsymD-*k*S and AsymD-*k*D device structures as function of L_{hk} considering HfO_2 as inner spacer permittivity materials.

This section is also devoted towards performance evaluation of devices using parameters such as drive current, gate leakage current, sub-threshold current and short channel parameters. Furthermore, several effects due to source and drain side spacers and their combined effect on symmetric device is also investigated. Fig. 3.20 plots the drive current and sub-threshold current component as a function of high-*k* spacer length varied from gate edge (L_{hk}=0 nm) to source and/or drain edges (L_{hk} = L_{EXT} = 20 nm). It is observed that, the drive current in both the SymD-*k* and AsymD-*k*S devices increases with an increase in L_{hk} up to an optimal point of 12 nm beyond which it starts decreasing. However, in AsymD-*k*D device structure, it is throughout constant, when L_{hk} is extended from gate edge to drain edge. It is also observed from Fig. 3.20 that the AsymD-*k*D device leads to a higher subthreshold leakage current in comparison to its counterpart AsymD-*k*S device. However, both SymD-*k* and AsymD-*k*S structure shows overlapped leakage current behavior. The sub-threshold leakage component in all the considered structures are lesser than the conventional one because of better electrostatic integrity. It is observed from the obtained results that the source side spacer mainly governs the charge transport from source to drain, however, the drain side spacer helps to enhance the current magnitude in SymD-*k* compared to AsymD-*k*S.

Apart from the sub-threshold leakage current (I_{SUB}), the gate tunneling current (I_G)

are considered to be a dominant leakage current component that may affect the device performance. The gate leakage current is further composed of the gate-to-channel tunneling current (I_{GC}) and the edge direct tunneling current (I_{EDT}). When the device operates in ON-state (V_{GS}=V_{DD}), the I_{GC} dominates due to the direct tunneling of carriers from the channel to the gate. However, the I_{EDT} appears through the gate and drain/source extension region, both in the ON-state [I_{EDT-ON} at (V_{GS}=V_{DD}, V_{DS}=0)] and OFF-state [$I_{EDT-OFF}$ at (V_{GS}=0, V_{DS}= V_{DD})]. The $I_{EDT-OFF}$ component is much smaller than I_{EDT-ON} Therefore, the total gate-tunneling current (I_{G-ON}) in ON-state is the sum of I_{GC} and 2×I_{EDT-ON} [BansA'04].



(a) (b)

Figure 3.21. Effect on (a) ON-state gate tunneling current, and (c) OFF-state gate tunneling current as function of L_{hk} in SymD-*k*, AsymD-*k*S and AsymD-*k*D device structures.

Fig. 3.21(a) and (b) shows the variations of ON and OFF state gate tunneling current, respectively with L_{hk} for the three considered dual-*k* structures normalized with respect to the conventional one. As expected, both the AsymD-*k*S and AsymD-*k*D architectures shows same I_{G}-ON with almost overlapping values at different spacer lengths. Moreover, around 8% increase in I_{G-ON} is observed in both asymmetric architectures as compared to the conventional one. Since the gate dielectric material and the thickness are same in all the devices, the I_{GC} component is almost constant and hence, the difference in I_{G-ON} is mainly due to the increase in I_{EDT-ON} due to the incorporation in high-*k* spacers. It is well known that the I_{EDT-ON} flows only near the gate edges therefore; an increase in L_{hk} does not reflect any change in it. The combined effect of spacers on both sides in SymD-*k* device results in a constant I_{G-ON} that is nearly 16% higher than the conventional one. On the other side, the $I_{EDT-OFF}$ current in OFF state (V_{GS}=0, V_{DS}= V_{DD}) reduces in both the SymD-*k* and AsymD-*k*D

structures while it remains same and marginally high in AsymD-*k*S device as compared to the conventional one. Fig. 3.22 shows the normalized I_{ON}/I_{OFF} variation with L_{hk} in three considered architectures. For both SymD-*k* and AsymD-*k*S devices, the maximum I_{ON}/I_{OFF} is obtained at the high permittivity spacer length L_{hk} of 12 nm because of the superior ON and OFF-state electrostatics. While in case of AsymD-*k*D structure, it remains constant.

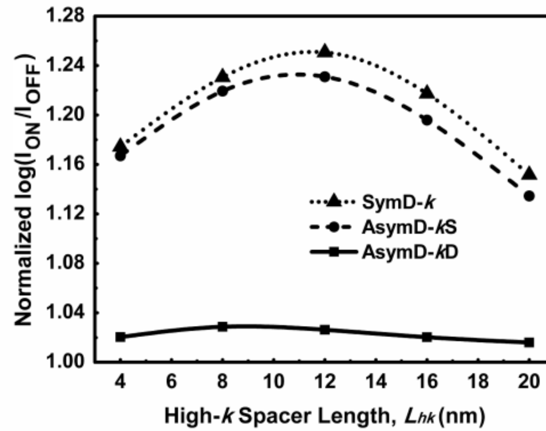
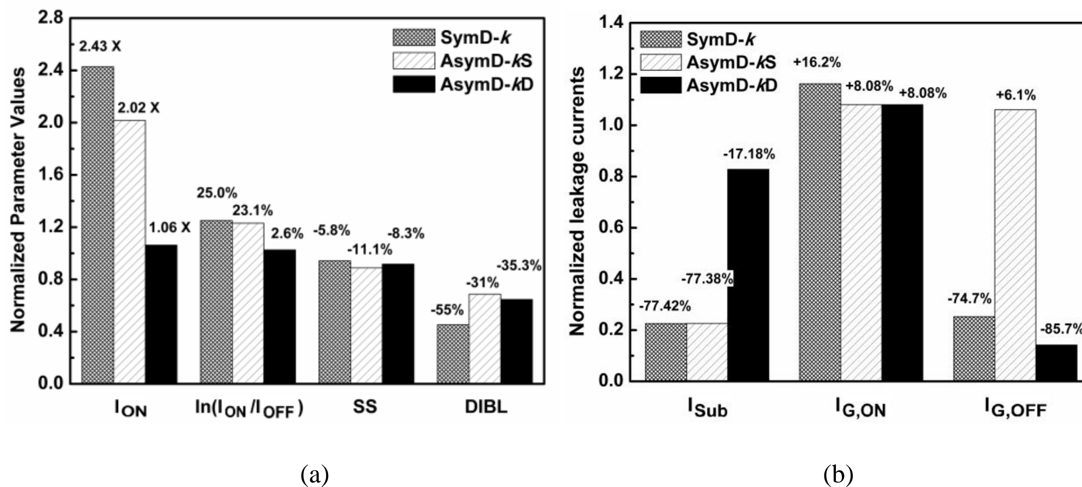


Figure 3.22. Variations in normalized log(I_{ON}/I_{OFF}) ratio as function L_{hk} for different dual-*k* spacer devices.



(a) (b)

Figure 3.23. (a) Design metrics and (b) leakage currents comparison among SymD-*k*, AsymD-*k*S and AsymD-*k*D device structures normalized with respect to the conventional one.

Fig. 3.23 examines the improvement observed in the device structures at an optimized inner high-*k* spacer length of 12 nm normalized with respect to the conventional one. For SymD-*k* and AsymD-*k*S FinFET, the drive current increases by 2.43 × and 2.02 ×, respectively while a marginal (~6%) improvement is observed in AsymD-*k*D structure over its conventional counterpart. Almost same increment *i.e.*

~25% is observed in $\log_{10}(I_{ON}/I_{OFF})$ for SymD-*k* and AsymD-*k*S in comparison to conventional one with an improved DIBL and SS. Although, the AsymD-*k*D perform better in terms of short channel characteristics but it shows marginal improvement in ON and OFF currents as compared to the conventional structure.

3.7 Summary

This chapter introduces the dual-*k* spacer concept that uses an optimal high-*k* spacer length for enhancing the device performance of an underlap FinFET. Current characteristics and SCE metrics of the proposed symmetric and asymmetric dual-*k* spacer devices are presented and compared with conventional single/low-*k* as well as purely high-*k* FinFET structures. To evaluate the optimal high-*k* point, the effect on drive current, leakage current and their ratio are discussed with respect to high-*k* spacer length and spacer material. Due to the fringing field through the spacer in dual-*k* architectures, not only the underlap region is affected but the charge density within the channel is also modulated significantly. The favorable field dynamics and charge modulation due to high-*k*/low-*k* spacer interface of the device are analyzed to evaluate their overall performance. It also demonstrates the electrostatics and merits associated with the proposed SymD-*k* and AsymD-*k*S FinFET structures over the conventional with varying inner high-*k* spacer permittivity. From this, an important and novel observation is made that the CBE barrier (in ON-state) directly under the gate increases in dual-*k* architectures which otherwise remains same in high-*k* device even though the inner spacer permittivity is increased substantially. A detailed comparative analysis helps to examine the ON- and OFF-state electrostatics with high permittivity sidewall spacers to reveal competing effects among the symmetric and asymmetric dual-*k* spacer devices. It is observed that the source side spacer mainly governs the charge transport from source to drain, however, the drain side spacer helps to enhance the current magnitude in SymD-*k* compared to AsymD-*k*S. Overall, the proposed SymD-*k* and AsymD-*k*S architectures exhibits excellent device performance that would anticipate better circuit/SRAM performance.

CHAPTER 4

Capacitive Analysis and Dual-*k* FinFET based Digital Circuit Design

4.1 Introduction

Double/tri-gate FinFET transistors are recognized as one of the most promising successors of conventional bulk MOS devices in the sub-20 nm regime due to their excellent short channel characteristics and reduced leakage currents [ColiJ'08]. However, in addition to the advantages offered by FinFET in device level, it also offers some new challenges to handle from circuit perspectives. The two main inherent challenges associated with FinFET are the higher magnitude of parasitic due to its three-dimensional architecture and the fin width quantization that limits its applicability in high-performance circuit applications due to conflicting design requirements. In conventional MOS devices, digital designers considered width, length, and area as parameters for evaluating the trade-off between transistor configuration and electrical performance. The nature of FinFET design could dramatically change all that.

In an underlap device, the source/drain series resistance ($R_{S/D}$) starts dominating that limits the device drive-current (I_{ON}). Incorporating high-*k* spacers can provide strong field coupling between the gate and the undoped underlap region that reduces $R_{S/D}$ [TrivV'05]. Previous studies have shown device performance with an optimized underlap structure [ShenR'03, SchuT'04]. However, they have not considered the fringe capacitance (C_{fr}) that strongly affects the switching speed in deeply scaled FinFETs. Therefore, the digital circuit designers need to adapt their designs taking into account these critical issues so as to improve overall performance in terms of device and circuit parameters such as I_{ON}, I_{OFF}, noise-immunity, and the switching speed.

Most of the previous work on FinFET devices has been done at the device and process level [SharR'11, MajuK'11, Dey'08]. At the CAD and circuit level, only few researchers have looked into the FinFET design issues. Several researchers have focused on the integration of high-*k* materials as a gate-dielectric and/or spacers from device level [ShahD'09, AgraS'10, VellG'07]. A high-*k* gate dielectric could offer

additional advantages such as thinner effective oxide thickness (EOT), which implies higher gate capacitance (C_{GG}) and I_{ON}. Also, the larger high-*k* dielectric thickness reduces the parasitic gate-source/drain (G-S/D) outer-fringe capacitance [KimSH'06, ManCR'07]. The fringing field phenomenon through this high-*k* gate dielectric has been studied by few researchers from circuit perspectives in [AgraS'10, MohaN'02]. Agrawal *et al.* [AgraS'10] simulated a CMOS ring-oscillator using high-*k* gate dielectric and reported a modest performance enhancement for an optimized permittivity of *k*~20, relative to counterpart CMOS with SiO_2 gate dielectric. Several research works have reported the impact of gate-sidewall fringe-field in enhancing the device performance using high-*k* spacers. However, a comprehensive study of 3D fringing field due to high permittivity spacers on circuit performance is still critically required. In addition, most of the reported data from circuit perspective are based on 2D device/circuit simulations. As the FinFET is three-dimensional device, therefore, the 2D structures remains susceptible to error. Therefore, to fully capture the effect of 3D fringing field, the 3D tri-gate device geometry should be considered.

This chapter investigates the effect of the optimized symmetric and asymmetric dual-*k* structures for better logic circuit performance. This work demonstrates the suitability of high-*k* spacer materials for high-performance logic circuits improving noise-margin and delay, simultaneously. The analysis presented in this chapter proves that the circuit delay reduces sharply with an increase in inner spacer permittivity that otherwise worsens for purely high-*k* structures. This chapter comprises of two major sections. Section 4.2 describes the role of fringe capacitances associated with the proposed SymD-*k* and AsymD-*k*S architectures. Thereafter, the impact of capacitance on circuit performance with different inner high-*k* spacer materials and length is investigated in section 4.3. The circuit performances are evaluated based on the static and dynamic characteristics of a CMOS inverter and a three-stage ring oscillator. Furthermore, the effect of power supply scalability on dual-*k* based circuits is investigated in section 4.4. Finally, section 4.5 presents a brief summary of this chapter.

4.2 Impact of Fringe Capacitance on Dual-*k* FinFETs

Fringe capacitance plays a dominant role in describing the circuit behavior. It is clear from the discussion presented in the preceding chapter that the performance among the conventional, high-*k* and dual-*k* architectures are mainly dependent on the

role of fringe-capacitances. Incorporation of high permittivity spacers, length and its placement, modulates the charge concentration and the electrostatics of the proposed architectures in comparison to conventional and high-*k* architectures.

In an underlap device, total gate capacitance (C_{GG}) includes gate-to-channel (C_{GC}), and fringe capacitance (C_{fr}) components. The C_{GC} component is almost same amongst the three considered structures. Introduction of high-*k* spacers enhance the fringe capacitance components of the structure. The total fringe capacitance consists of outer (C_{of}) and inner (C_{if}) fringe components. Since, in the strong inversion operation, C_{if} is screened by the channel, therefore, the outer fringe capacitance mainly affect the carrier modulation in underlap and channel region in dual-*k* spacer architectures. In general, the dynamic circuit performance of high-*k* spacer device degrades due to very high parasitic capacitances. Therefore, before going deeper into the circuit analysis, this section first explores the capacitive behavior of dual-*k* spacer architecture in comparison to the conventional single/low-*k* and purely high-*k* architectures.

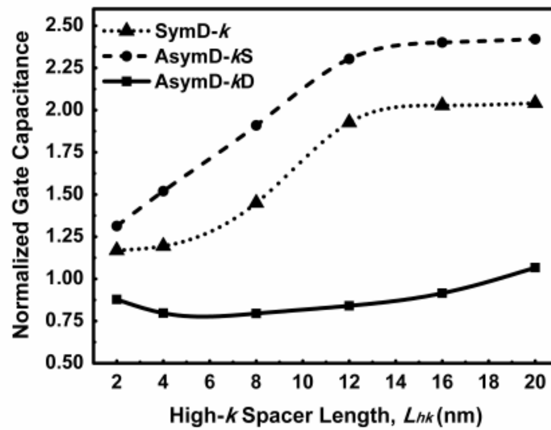
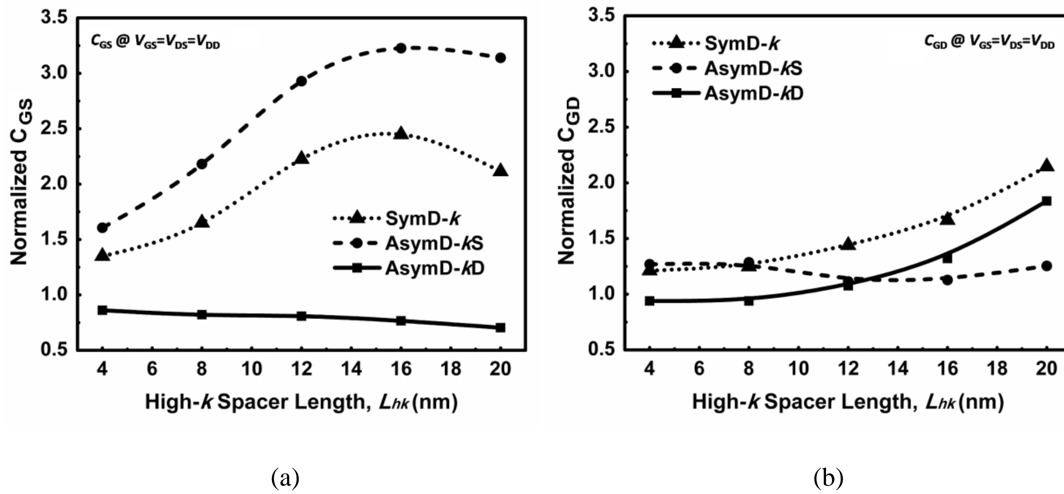


Figure 4.1. Effect of increasing L_{hk} on total gate capacitance (C_{GG}) in SymD-*k*, AsymD-*k*S and AsymD-*k*D device structures normalized with respect to the conventional.

Fig. 4.1 depicts the change in total gate capacitance (C_{GG}) in proposed SymD-*k*, AsymD-*k*S and AsymD-*k*D architectures normalized with respect to the conventional (considering HfO_2 as spacer material) as function of L_{hk}. It is observed that both SymD-*k* and AsymD-*k*S demonstrate similar capacitive behavior. As L_{hk} is increased towards S/D edge (or towards source-edge only in case of AsymD-*k*S), the outer fringe component dominates the overall gate capacitance. To better understand the role of individual capacitances and its impact on device performance; the C_{GG} is further divided into gate-to-source (C_{GS}) and gate-to-drain capacitance (C_{GD}).

Fig. 4.2(a) and 4.2(b) presents the contribution of C_{GS} and C_{GD}, respectively in overall C_{GG} with an increasing inner high-k spacer length. For AsymD-kS and SymD-k architectures, it is observed from Fig. 4.2(a) that the C_{GS} increases sharply up to L_{hk} = 12 nm as expected and thereafter, decreases marginally. However, for AsymD-kD architecture, although the C_{GS} component slightly decreases, but retains much lower values that are comparable to the conventional one. In AsymD-kD architecture, the inner high-k spacer is placed only on the drain side while, the source-side has the same low-k spacer throughout the gate-edge to source-edge. Therefore, if only the outer fringe component is considered then the C_{GS} component should be constant irrespective of the change in inner high-k spacer length at drain-side. However, it is observed that although the overall C_{GS} component has smaller values but it continuously decreases even though the source-side spacer is unchanged. This is due to the drain-side electric field that influences the channel as shown in Fig. 4.3.



(a) (b)

Figure 4.2. Effect of increasing L_{hk} on (a) C_{GS} and (b) C_{GD}, in SymD-k, AsymD-kS and AsymD-kD structures normalized with respect to the conventional.

Note that the overall C_{GG} is divided into C_{GS} and C_{GD} from the centre of the gate (at [x] =0 nm point as shown in Fig. 4.3). It is observed that with an increase in L_{hk} at drain-side, the charge density within the channel region (towards source and drain sides) also modulates and hence it can be said that the drain influences the channel directly under the gate. The modulated charge directly under the gate (towards the source side) reduces the inner fringe component and therefore, the overall C_{GS}. For shorter gate length, this effect becomes more prominent. Similarly, it is observed from Fig. 4.2(b) that the C_{GD} component slightly fluctuates with an increase in L_{hk} of AsymD-kS architecture. However, it has uniformly higher value than the conventional

device because the charge modulation directly under the gate is more in case of AsymD-*k*S architecture than the AsymD-*k*D [shown in Fig. 3.20]. It is also observed from the Fig. 4.2(b) that the C_{GD} component in both the SymD-*k* and AsymD-*k*D increases steeply that would enhance the Miller capacitance and degrade the dynamic performance of a circuit/SRAM.

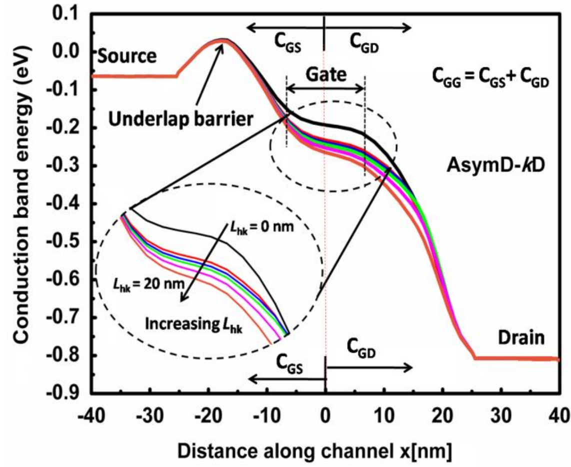
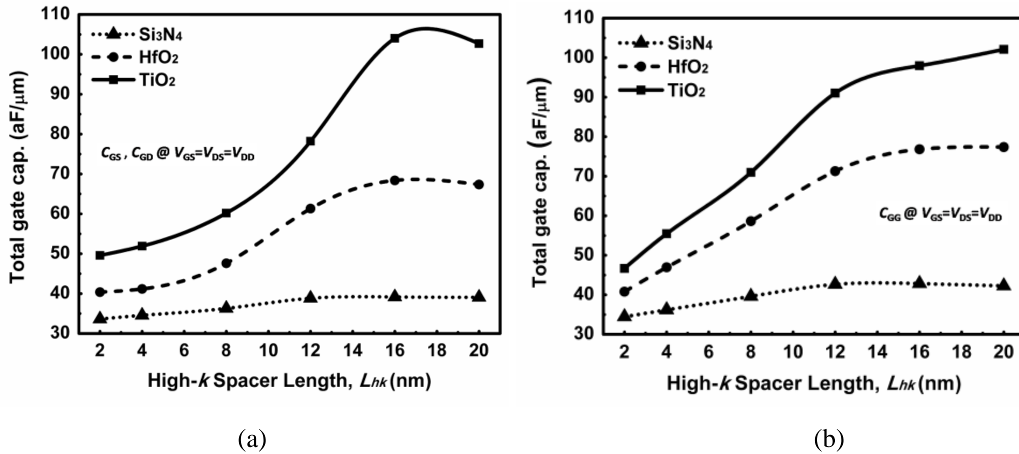


Figure 4.3. CBE profile along the channel for conventional and AsymD-*k*D *n*-FinFET structures with increasing L_{hk} at $V_{GS}=V_{DS}=V_{DD}$.

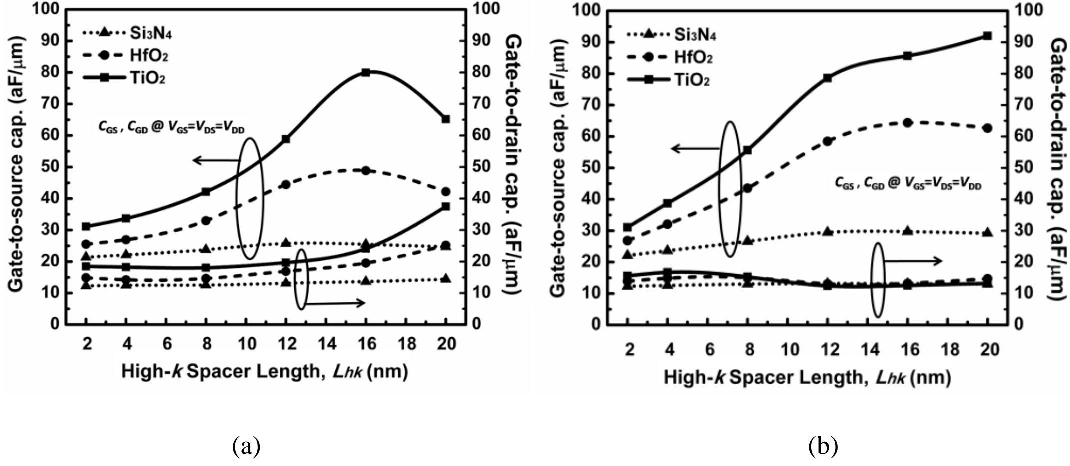


(a) (b)

Figure 4.4. Effect of increasing L_{hk} on total gate capacitance in (a) SymD-*k* and (b) AsymD-*k*S structure for different *k* normalized with respect to the conventional.

To comprehensively analyze the impact of fringe capacitances with different spacer permittivity; Fig. 4.4(a) and 4.4(b) shows the C_{GG} variations with L_{hk} in SymD-*k* and AsymD-*k*S considering Si_3N_4, HfO_2 and TiO_2 as inner high-*k* spacer dielectric. In addition to the C_{GG} increment with L_{hk}, it is also observed that the fringe component excessively increases with an increase in the spacer permittivity values ranging from 7.5 to 40. Very large fringe capacitance associated with the high-*k* spacer device (L_{hk}= 20 nm) degrades the device performance. For TiO_2 (*k*=40) spacer

materials, the total gate capacitances in SymD-*k* and AsymD-*k*S structures are nearly 2.1× and 3.2×, respectively than the conventional structure with SiO_2 spacer.



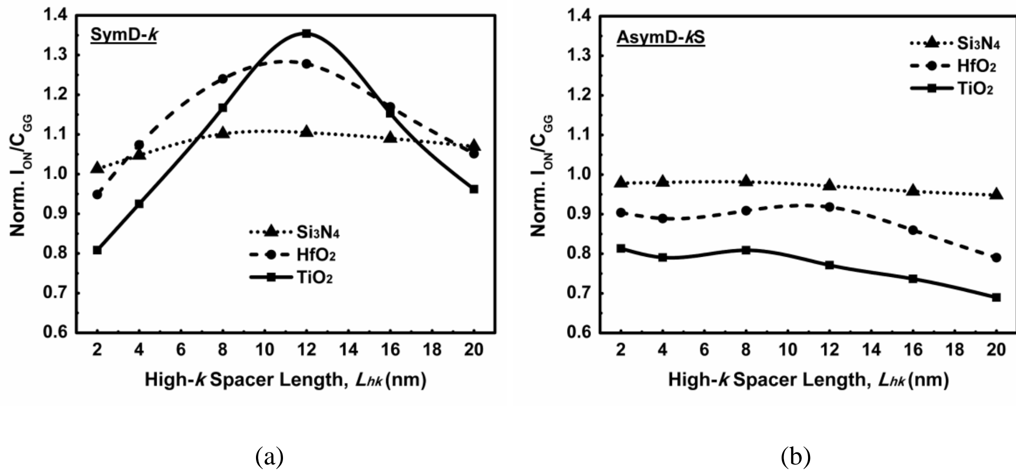
(a) (b)

Figure 4.5. Effect of increasing L_{hk} on C_{GS} and C_{GD}, for different spacer permittivity materials in (a) SymD-*k* and (b) AsymD-*k*S FinFET structure.

Fig. 4.5(a) and 4.5(b) shows the variations of C_{GS} and C_{GD} in SymD-*k* and AsymD-*k*S devices, respectively with increasing inner spacer length for different spacer materials. It is observed that the C_{GD} component in symmetric and asymmetric structures contributes much lesser than the C_{GS} component in the total gate-capacitance. For higher permittivity (*k*) in SymD-*k* structure, the C_{GS} increases rapidly with L_{hk} that result in higher ON-current trends (as shown in Fig 3.3). However, the delay performance of a logic circuit is directly dependent on the Miller component of C_{GD}. A higher value of C_{GD} in the high-*k* device severely degrades the delay and switching performance. Interestingly in SymD-*k* device, C_{GD} remains almost constant up to an optimal L_{hk} and then starts increasing because of stronger gate-drain coupling. Whereas, the C_{GD} component remain almost same throughout the L_{hk} in AsymD-*k*S device structure (due to the absence of drain side high-*k* spacer). Therefore, AsymD-*k*S structure would show better delay performances in comparison to SymD-*k* structure that will be dealt in next section.

For digital applications, the device performance in terms of circuit delay depends on the relative rate of change of I_{ON} and C_{GG} [SachA'08]. Therefore, in most of the literature, the circuit delay performance is usually predicted by the relative rate of change of I_{ON} and C_{GG}. For achieving substantial reduction in delay, I_{ON}/C_{GG} should be high enough.

Fig. 4.6 shows the variations of normalized I_{ON}/C_{GG} as a function of L_{hk} for different k value. For SymD-k FinFET, it is observed that an optimum I_{ON}/C_{GG} is obtained with L_{hk} ranging from 8 to 12 nm for different high-k spacer materials that strongly impacts the delay of a circuit. However, in case of AsymD-kS FinFET, the I_{ON}/C_{GG} is continuously decreases with an increase in L_{hk} as shown in Fig. 4.6(b). This anticipates that the proposed AsymD-kS structure is not suitable for logic circuit applications in achieving better delay performances. Conversely, it is observed that the AsymD-kS structure outperforms the SymD-k and conventional in terms of delay performance. Even the circuit delay reduction is more prominent with an increase in spacer permittivity. Note that the intrinsic advantages of FinFET become not visible if a simple $C_{GG}V_{DD}/I_{ON}$ delay metric is used for circuit performance evaluation. For a first-hand approximation, it helps to roughly anticipate the device dynamic performance in symmetrical architectures only. However, it may fail in predicting the dynamic performance for S/D asymmetric architectures.



(a) (b)

Figure 4.6. Normalized I_{ON}/C_{GG} in (a) SymD-k and (b) AsymD-kS structures for different spacer material as function of L_{hk}.

4.3 Dual-*k* Spacer based Circuit Performance: Stability and Speed

The primary goal in CMOS logic circuit is to maximize stability and switching speed, simultaneously. However, it is observed from the device analysis that the high-k structure with higher spacer permittivity could be beneficial in enhancing stability but at a cost of exorbitant increase in fringe capacitance that in turn degrades the delay performance. Therefore, most of the researchers have been forced to design logic circuits with low permittivity spacers. To the best of our knowledge, no published material exists that designs and analyzes logic circuits with high-k spacer

device demonstrating improvement in noise-margin and delay performances, simultaneously. Considering these facts, this research work targeted for improvements in noise margin and delay using high permittivity spacers.

Motivated by the superior electrostatics of symmetric and asymmetric dual-*k* spacer FinFETs, this section describes the suitability of SymD-*k* and AsymD-*k*S device for high-performance circuit applications for improving the static and dynamic performances. To evaluate the FinFET logic circuit performance, mixed mode circuit simulations of a FinFET inverter and the three-stage ring-oscillator (RO3) circuits have been carried out. The *p*-type to *n*-type width ratio of a FinFET inverter is tuned to 2:1 to obtain symmetrical voltage transfer characteristics (VTC) and to maximize the noise-margins. Static and dynamic characteristics of FinFET logic circuits based on the conventional, dual-*k* and purely high-*k* structures are compared.

4.3.1 Static Characteristics

This sub-section discusses the voltage transfer characteristics (VTC) of the SymD-*k* and AsymD-*k*S based CMOS inverter with an increase in inner spacer permittivity. It is observed from Fig. 4.7, that the slope in the transition region increases with an increase in inner-spacer permittivity. A sharp transition region improves the noise-margins (NM_H, NM_L) of an inverter that in turn enhances stability. Accordingly, Fig. 4.8 shows the improvement in maximum voltage gain achieved with SymD-*k*, AsymD-*k*S and high-*k* based inverters in comparison to the conventional one.

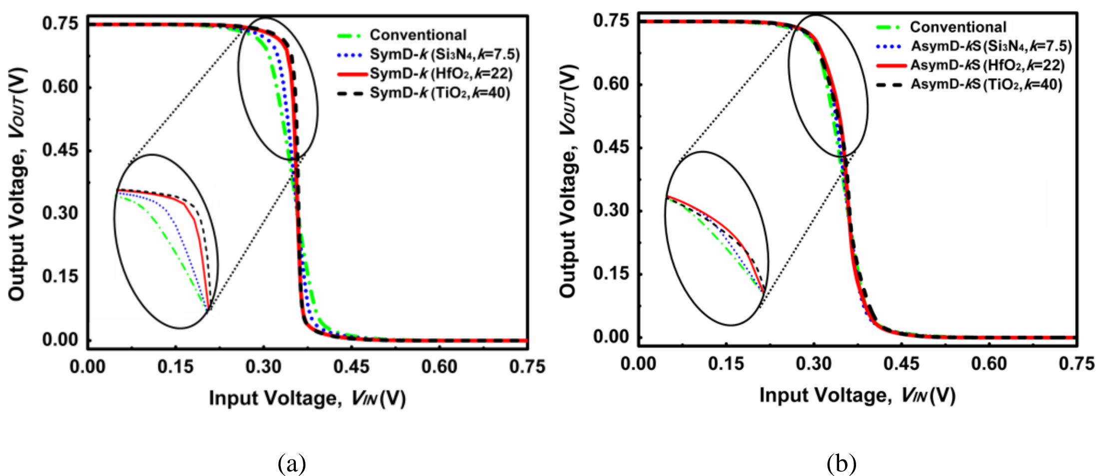


Figure 4.7. Voltage transfer characteristics comparison of (a) SymD-*k* and (b) AsymD-*k*S structure for different spacer permittivity.

It is observed that for lower spacer permittivity (Si_3N_4, k=7.5), both high-k and SymD-k based inverter shows similar improvement. However, with higher spacer permittivity materials, SymD-k not only outperforms the conventional and high-k but the AsymD-kS as well. In comparison to the conventional one, SymD-k based CMOS inverter shows an improvement by a factor of 4.1 and 7.6 in maximum voltage-gain with an inner spacer permittivity of HfO_2 and TiO_2, respectively. These improvements are attributed to the very high drive current and better SCE control. The transition region slope is also dependent on the DIBL and sub-threshold swing of a device. Therefore, the SymD-k structure performs better on all these grounds. Generally, it appears that the circuit stability has a negative correlation with DIBL [SongX'10]. Moreover, it is observed from the analysis carried out that the spacer permittivity (k) has a direct correlation with the inverter stability. In agreement to this, the *NM*s are considerably improved using higher inner permittivity in dual-k structures.

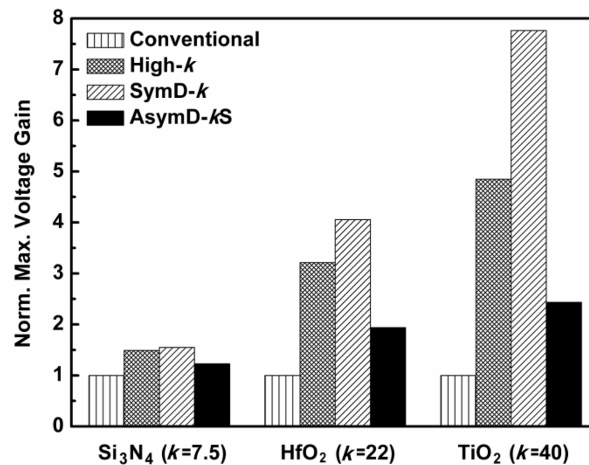


Figure 4.8. The maximum voltage gain comparison among SymD-k, AsymD-kS and high-k structure for different spacer permittivity (k) normalized with respect to the conventional one.

4.3.2 Dynamic Characteristics

This section describes the delay metric outcomes based on the choice of the high-k spacer material and its length in FinFET logic circuits applications. To evaluate the dynamic performance, a mixed-mode circuit simulation of the CMOS inverter and a three-stage ring oscillator (RO3) circuit has been carried out. Fig. 4.9 shows the inverter delay of symmetric and asymmetric dual-k structures normalized with respect to the conventional one as a function of L_{hk} (with HfO_2 as spacer permittivity material). It is clearly observed that both the proposed SymD-k and AsymD-kS architectures shows better inverter delay performances with an optimized L_{hk} of 12

nm even though, both the structures also exhibits larger fringe capacitances. This superior delay performance is primarily due to the optimized high-*k* spacer length and its placement that modulates the field dynamics and hence, electrostatics of the architecture.

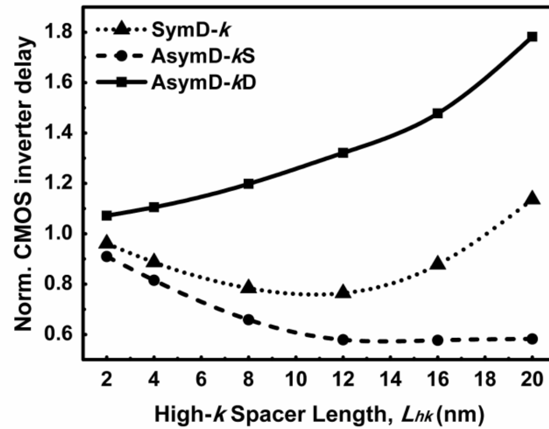


Figure 4.9. CMOS inverter delay for symmetric and asymmetric dual-*k* architectures as function of L_{hk}, normalized with respect to conventional counterpart.

It is discussed in the previous section that the SymD-*k* structure exhibits better static characteristics than the AsymD-*k*S. However, in terms of dynamic performance, the AsymD-*k*S outperform SymD-*k* architecture due to higher C_{GS} and smaller C_{GD} values. In SymD-*k* device, the C_{GD} component sharply increases beyond an optimum L_{hk} of 12 nm, moreover, the C_{GS} reduces that degrades the delay performance. On the other hand, the inverter delay worsens in AsymD-*k*D device because of the lower C_{GS} and a high value of C_{GD}. Because of inferior performance, the subsequent sections will not deal with AsymD-*k*D device.

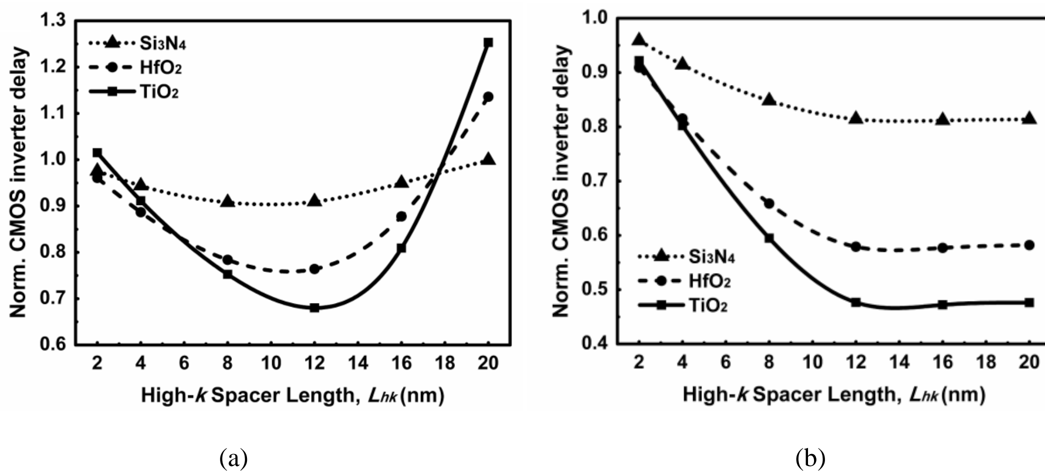


Figure 4.10. CMOS inverter delay for (a) SymD-*k* and (b) AsymD-*k*S architectures as function of L_{hk} normalized with respect to conventional one.

Fig. 4.10 (a) and (b) plots the SymD-*k* and AsymD-*k*S, based inverter delay, respectively normalized with respect to the conventional one as a function of L_{hk} with different spacer permittivity materials. It is observed from Fig. 4.10(a) that the inverter delay reduces with an increase in L_{hk} upto an optimal value of 12 nm, thereafter, it starts increasing sharply. For purely high-*k* device (at L_{hk} = 20 nm), the inverter delay worsens by 15% and 27%, whereas in contrast to this, the SymD-*k* based inverter (L_{hk}= 12 nm) speeds up by 24% and 32% for spacer materials of HfO_2 and TiO_2, respectively. As discussed earlier, the worst delay performance shown by high-*k* device is because of the increased Miller capacitance (C_{GD}) beyond L_{hk}=12 nm. Furthermore, it is also observed that the rate of decrement (or increment) in inverter delay in the vicinity of L_{hk}=12 nm sharply increases with an increase in inner spacer permittivity.

Contrastingly, in AsymD-*k*S structure [shown in Fig. 4.10(b)], the inverter delay sharply reduces with an increase in L_{hk} at source side upto an optimal value of 12 nm, and thereafter, it saturates. In comparison to the conventional one, the AsymD-*k*S based inverter (at L_{hk} = 12 nm) speeds up by 42% and 54.4% for spacer materials HfO_2 and TiO_2, respectively. For similar delay improvement, AsymD-*k*S can also be considered with L_{hk} equals to L_{EXT} *i.e.* 20 nm that also simplifies the process complexity. But it will slightly deteriorate the device as well as SRAM performance. Therefore, a better circuit performance of symmetric and asymmetric dual-*k* structures in terms of inverter delay and stability is obtained at L_{hk}=12 nm with higher spacer permittivity.

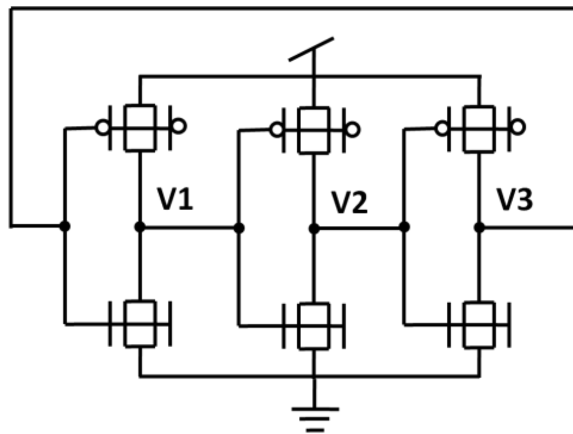


Figure 4.11. Schematic of CMOS based three-stage ring-oscillator circuit.

For the accurate delay assessment, the suitability of the SymD-*k* and AsymD-*k*S

FinFET are also investigated by realizing a three stage-ring oscillator (RO3) circuit and it further compared with the conventional and purely high-*k* based RO3 delay. The schematic of a tied-gate RO3 circuit is shown in Fig. 4.11 wherein each stage of a RO3 is a static FinFET inverter. The V_1, V_2 and V_3 represent the output node voltages of the corresponding inverters. The output waveform of the conventional, SymD-*k* and AsymD-*k*S based RO3 (Fig. 4.12) shows the stable frequency oscillations. The output frequency of a 3-inverter stage ring oscillator is obtained as 1/(6×inverter delay). Thus, the propagation delay of an inverter circuit is obtained by measuring the time period (T) of the oscillator.

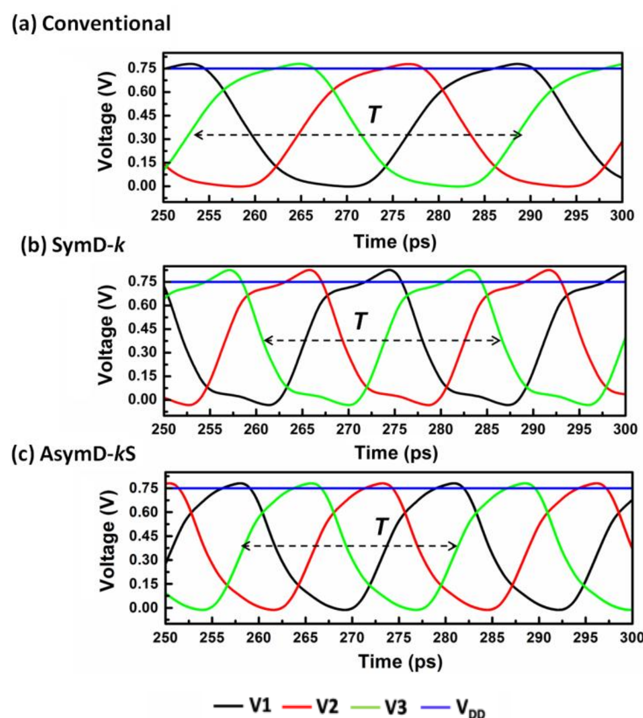


Figure 4.12. Output waveforms of the (a) conventional, (b) SymD-*k* and (c) AsymD-*k*S FinFET based three stage ring oscillator.

Fig. 4.13 shows the percentage improvement in RO3 delay/stage for SymD-*k*, AsymD-*k*S and high-*k* with respect to the conventional one for different spacer permittivity materials. In comparison to the conventional one, SymD-*k* based RO3 demonstrates a delay reduction of 8%, 20% and 27% for an inner high-*k* spacer material of Si_3N_4, HfO_2 and TiO_2, respectively. However, the AsymD-*k*S based RO3 demonstrates a delay reduction upto 41% for an inner spacer permittivity ranging from 7.5 to 40. This performance benefit is due to the combined effect of higher drive current, higher C_{GS} and lower C_{GD} in comparison to a purely high-*k* device. Although, the high-*k* based logic circuits demonstrates better stability with respect to

conventional one, but its delay performance is the worst among all. Similar to the inverter delay results, the RO3 delay proves that the dynamic performance improvement using dual-*k* spacer architectures are more pronounced with higher permittivity of the inner spacers.

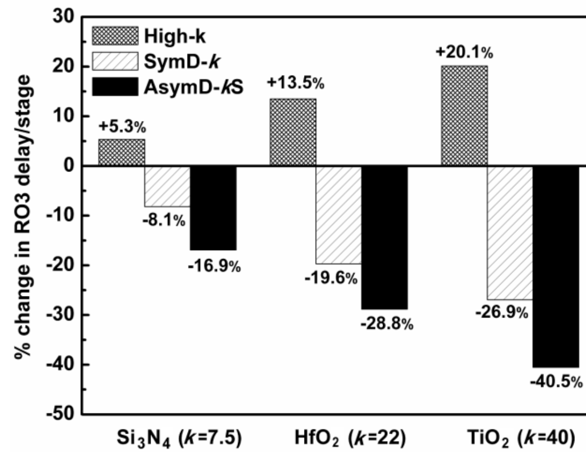


Figure 4.13. Percentage change in RO3 delay/stage using SymD-*k*, AsymD-*k*S and purely high-*k* structures with different spacer material normalized to the conventional one.

Energy consumption in digital circuits is another important concern that needs to be addressed. The higher capacitance and higher current would lead to higher energy consumption of a circuit. Fig. 4.14 shows the spacer engineering effect on the energy consumption of an inverter. It is observed that the dynamic energy of an inverter circuit significantly increases with an increase in inner high-*k* spacer length. As the AsymD-*k*S shows highest capacitance among all the considered dual-*k* architectures, therefore AsymD-*k*S based inverter shows highest dynamic energy consumption as compared to others.

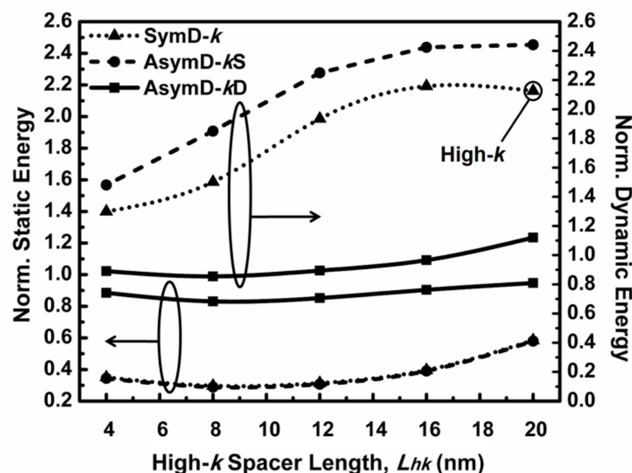


Figure 4.14. Static and dynamic energy consumption of an inverter with varying L_{hk}.

Similarly, AsymD-*k*D shows almost same dynamic and static energy in comparison to the conventional case because of its reduced capacitance as well as current characteristics. It is also observed that the proposed symmetric dual-*k* (SymD-*k*) tri-gate based inverter also consumes lesser dynamic energy in comparison to purely high-*k* devices. Moreover, from the static energy perspective, dual-*k* architectures outperform not only the high-*k* devices but also the conventional one due to the significantly lower leakage currents. It is a well-known fact that with higher device density, lower supply and threshold voltages, the energy optimization focus has shifted from dynamic to leakage (static) energy while maintaining sufficient speed characteristics. The leakage energy is now dominating in the dense cache memories that occupies major portion of a die. Therefore, we believe that for highly dense memories, the proposed SymD-*k* and AsymD-*k*S architectures would outperform both the conventional and purely high-*k* structures in terms of overall energy consumption.

4.4 Effect of Supply Voltage on Dual-*k* based Circuits

The power supply scalability is an important metric that needs to be explored from circuit perspectives. Fig. 4.15 presents the effect of lowering the V_{DD} on VTC. The insets in the Fig. 4.15 shows the voltage-gain comparisons of dual-*k* FinFET based CMOS inverter over the conventional one. Compared to the conventional, the SymD-*k* based inverter shows prominent improvement in voltage gain with scaling of supply voltage. However, it is observed that, the VTC of AsymD-*k*S based inverter degrades at higher V_{DD}.

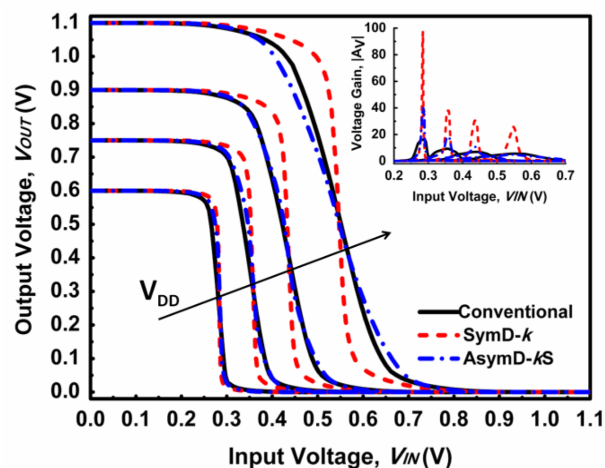


Figure 4.15. Effect of V_{DD} scaling on CMOS inverter VTC and voltage gain.

It is because of the enhanced GFIBL effect at higher V_{DD} that significantly reduces the G/S underlap barrier. Therefore, the CBE barrier (in ON-state) directly under the gate becomes prominent (instead of underlap barrier) that limiting the drive current in AsymD-*k*S and hence the static performance.

4.5 Summary

This chapter comprehensively analyzed the role of fringe capacitances associated with proposed dual-*k* architectures that advocates for high-*k* spacer materials for improving noise-margin and delay performances, simultaneously. Although, the dual-*k* structures exhibit larger fringe capacitances, but with an optimized inner spacer length of 12 nm, both the SymD-*k* and AsymD-*k*S architectures show better inverter delay performances. This superior delay performance is primarily due to the diligent usage of high-*k* spacer length and its placement that modulates the field dynamics and hence, electrostatics of the architecture. The AsymD-*k*S outperforms the other architectures in terms of dynamic performances due to higher C_{GS} and smaller C_{GD} values. Moreover, an important and novel observation is made that the delay performance improvement is more pronounced with higher permittivity of the spacers in dual-*k* spacer technology that otherwise worsen in case of purely high-*k* architecture. Furthermore, this chapter also investigated the effect of power supply scalability on dual-*k* based circuits.

CHAPTER 5

Design Metric Improvement of Dual-*k* based SRAM Cell

5.1 Introduction

The continuous increase in the dataset size and wide gap between the speed of processor and main memories has led to an ever-increasing demand for large cache memories. In modern processors, the caches account for a significant fraction of the chip area as well as the power consumption. Recently, the ITRS predicted that by the end of year 2016, the memory circuits would occupy 94% area of a chip [ITRS]. Traditionally, SRAM has been the workhorses for realizing cache memories due to its robustness, relatively lower read/write access times and process compatibility. Most of the time the large SRAM cell array remains idle; therefore, static power consumption is a big issue for memory circuits. However, exorbitantly high leakage currents and short channel effects such as V_{th} roll-off, DIBL, and sub-threshold slope, places several significant challenges to SRAM design. To tackle the leakage problem and to improve SRAM stability, earlier research efforts have explored a number of different device and circuit level techniques such as multi-V_{th} and multi-t_{ox} transistors [RostM’11], body/back-gate biasing [GiraB’09], write assist [YangY'12], 8T/10T bit-cells [KanjR'08], and so on. However, as the technology scales down to sub-20 nm nodes, extremely small channel lengths and close proximity between highly doped source and drain region introduces newer leakage components such as the direct source to drain tunneling (DSDT) leakage in addition to sub-threshold thermionic leakage and gate leakages [VegaR'10]. This leads to very high leakage currents as well as degradation of the transistor I_{ON}/I_{OFF} ratio, which impacts the leakage and access time of the cell. The other major design concern is the read/write conflict, wherein a transistor sizing to enhance the read-stability degrades the write-ability and vice-versa. To enhance read stability, a cell-ratio (CR) must be increased either by increasing pull-down transistor width or by increasing access transistor length. Both options degrade write-ability, area as well as power dissipation [GiraB'08]. Similarly, to enhance write-ability, a pull-up ratio (PR) must be decreased. So, the main conflict arises due to the current driving capability of the access transistor.

As FinFET offers some unique features, solutions can be achieved by exploiting

these features. Several radical departures from conventional design have been discussed earlier in section 2.6.3 that claimed to mitigate read-write stability conflict, improved noise-margins, and access times. A substantial volume of research focused on independent-gate configurations for threshold (V_{th}) adjustment [GiraB'09] that also enhanced the circuit complexity. Recently, many innovative source/drain asymmetric architectures have been proposed to mitigate read/write conflict and improve SRAM cell metrics. Source/drain asymmetry helps in adjusting the PR and CR to augment the stability but in turn adversely affects the cell-area, leakage power and access-times. Goel *et al.* [GoelA'11] proposed asymmetric structure that enhances read/write stability and reduce leakage at the expense of higher access time and cell-area. Moradi *et al.* [MoraF'11] proposed an asymmetrically doped (AD) FinFET structure that reported an improvement in SNMs and cell leakage but with a higher access time penalty. Recently, Sachid *et al.* [SachA'12] proposed stable SRAM cell structure by fabricating multiple fin height (H_{fin}) that is possibly a better solution to width quantization but it is an application specific approach with an increased process complexity. Moreover, all these structures would require setting up of new design rule constraints, thus limiting their applications.

Motivated by the superior device electrostatics and circuit performance, this chapter investigates the proposed symmetric (SymD-*k*) and asymmetric dual-*k* (AsymD-*k*) architectures in 6T-SRAM cell. It is observed that the proposed SymD-*k* based SRAM cell helps in improving the hold, read and write noise-margins, read/write speed (access-time), and standby leakage power without affecting PR and CR. Moreover, the AsymD-*k* based SRAMs also enhance stabilities, write-delay and leakage power without cell-area and read delay penalties. Rest of the chapter is organized as follows. Section 5.2 presents the brief introduction of basic SRAM architecture and bit-cell, its read/write operations, and the performance evaluation metrics such as SNM, access-time and standby leakage power. Thereafter, section 5.3 explores the proposed symmetric and asymmetric dual-*k* configurations, its merits and demerits over the conventional and purely high-*k* architectures. In section 5.4, the effect of supply voltage on dual-*k* based SRAM cells are investigated. Section 5.5 compares both the proposed dual-*k* based SRAM cells on common platform by evaluating power margins. At last, section 5.6 draws a brief summary and the major outcomes of this chapter.

5.2 Basic Operation of an SRAM Memory Cell

An SRAM cache consists of an array of bi-stable memory bit cells along with the address (row and column) decoders, sense amplifiers, write drivers and bit-line pre-charge circuits commonly known as the peripheral circuitry. Peripheral circuitry helps in reading from and writing into the array. A conventional SRAM array is composed of millions of identical cells. For example, a 32 Mb cache memory is composed of 33,554,432 cells. Each cell circuit is capable of storing single bit of information. Therefore, a small improvement in reliability, performance and saving in static power will strongly impact the entire processor. As most of the chip area in a cache is covered by the bit-cell component, therefore, several researchers targeted to improve SRAM cell performance from past four decades [AnanH'06, BansA'07, BhatD'14, ChenB'07, GiraB'09].

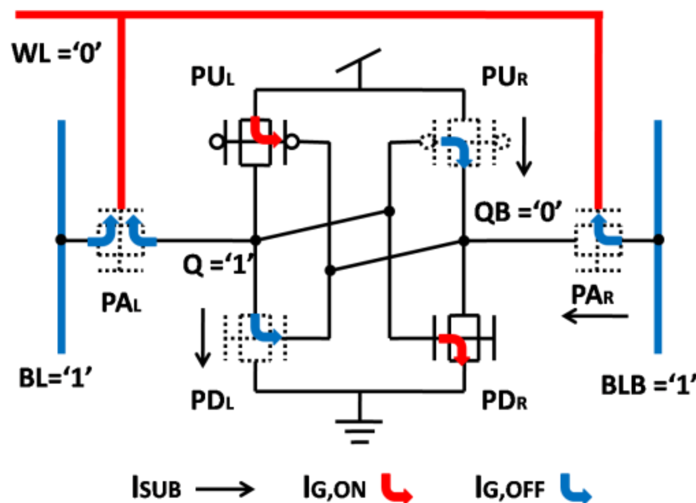


Figure 5.1. A standard tied-gate 6T SRAM cell schematic with different leakage current contributions.

A standard tied-gate 6T SRAM cell consists of two cross coupled inverters and two access transistors connected to each data storage node. The schematic circuit of the same is shown in Fig. 5.1 with different leakage current contributions. The inverter pair forms a latch and holds the binary information. The data in SRAM cell is stored as long as the power is ON. The cross-coupled inverters are connected to two bit-lines, commonly known as BL (bit-line) and BLB (bit-line bar/complement), through access transistors PA_L and PA_R, respectively. The access transistors are controlled by the word-line (WL) voltage. The SRAM cell has three modes of operation: read, write and standby. In other words, it can be in three different states such as reading, writing or standby. In the standby or hold mode, WL is kept low

(V_{WL}= 0 V), thus turning OFF the access transistors and isolating the bit-lines from the cross-coupled inverter pair.

In a read operation, prior to the word-line being selected (V_{WL} raised from 0 to V_{DD}); both the bit-lines are precharged to V_{DD} via low-impedance path. Then, the selected word-line is enabled (V_{WL}=V_{DD}), activating the access transistors of the desired row. By turning ON the access transistors of a row, a small difference voltage is generated between each bit-line pair, connected to it. This small voltage difference is detected and amplified by the sense amplifiers connected to the bit-lines. At the end of the read operation, the word-line is turned OFF, thus isolating the cell from the bit-lines and allowing data nodes to return to their standby values before the read cycle. Proper design needs be exercised to ensure that the values on storage nodes are not flipped during the read operation. However, in a write operation, appropriate write voltages are applied to the bit-lines to force the cell into the intended logical state. A write operation starts by applying a voltage at bit-line that corresponds to the data to be stored in the cell. Then, the word-line is enabled and the memory cell flips to the state corresponding to the voltage difference. The write operation is completed by turning OFF the word-line by column decoder. Throughout the chapter, the cell performance is mainly evaluated on the basis of SNMs (hold, read and write), read/write access time and the standby leakage power. The traditional measure to find the stability of an SRAM cell during the different modes of operation is the Static Noise Margin (SNM).

The SNM is defined as the maximum amount of DC noise voltage that can be tolerated by the cross-coupled inverter pair such that the cell retains its data [SheeE'87]. Both the hold and read SNM is extracted from the voltage transfer characteristics (VTC) in hold and read operation, respectively. During the hold/retention mode, nodes Q and QB store logic "1" and "0", respectively and word-line is OFF. Hold-SNM defines the stability in retaining the stored data. However, during a read operation, the word-line access transistors are ON after bit-lines are precharged. The read VTC can be measured by sweeping the voltage at the data storage node Q (or QB) with both bit-lines (BL, BLB) and word-line (WL) biased at V_{DD} while monitoring the node voltage at QB (or Q). For higher read stability, access transistor strength must be low. The access time in read mode is another important metric, which depends on read cell current through the access and pull-down

transistors. Similarly, write-margin and write access time are calculated for write operation. The write access time is measured between the time when WL reaches to 50% of V_{DD} and node QB reaches switching threshold voltage of the other inverter.

5.3 Dual-*k* FinFET based SRAM Cell Configurations

This section describes the design metric outcome of SymD-*k* and AsymD-*k* tri-gate FinFET based 6T SRAM cells. Fig. 5.1 shows the schematic of a tied-gate 6T SRAM cell with all leakage current components. The thick line is used to represents the large line capacitances associated with the word-line (WL) and bit-lines (BL and BLB). The PMOS pull-up transistors (PU_L and PU_R) and NMOS access transistors (PA_L and PA_R) are of minimum size (single fin) to set a low pull-up ratio value. All the analysis and comparisons are drawn (considering HfO2 as inner high-*k* spacer) based on the simulations performed for a cell-ratio of two by modulating fin-pitch and hence, current driving capability of pull-down transistors (PD_L and PD_R).

5.3.1 Symmetric Dual-*k* (SymD-*k*) FinFET based SRAM Cell

This sub-section presents the SRAM metrics enhancement using SymD-*k* FinFET structure in comparison to the conventional and high-*k* FinFET based SRAMs. The primary goal in SRAM cell includes maximizing stabilities and minimizing access times besides achieving minimum leakages. In general, the read and write stability depends on the resistive divider action of PA-PD and PU-PA transistors, respectively. The storage node voltage is charged or discharged through the access transistor. To prevent cell from the read-failure, the storage node voltages must be less than the inverter trip voltage. Therefore, the PDs must be stronger than PAs. For reliable write operations, the PA transistor strength must be larger than the PU transistor strength. This contradictory sizing requirement of access transistor raises read/write conflict. Therefore, it is necessary to use improved architecture that exhibits superior device performance while mitigating read/write conflict with improved access times. To the best of our knowledge, none of the published material exists that collectively improve the stabilities, access-time as well as standby leakage power; without affecting the design ratios (CR and PR) and cell area.

The noise-margin (SNM) comparisons of proposed SymD-*k* based SRAM cell with respect to the conventional and high-*k* based SRAM in all three possible modes of operations (hold, read and write) are shown in Fig. 5.2. The hold, read and write

margins are improved by 8.7%, 9.4% and 10.4%, respectively compared to conventional SRAM cell. These improvements in SNMs are attributed to the enhanced electrostatic control that increases noise-margins (NM_H and NM_L) and voltage-gain of an inverter (discussed in section 4.3.1). Also, the read/write stability is not directly dependent on the absolute value of I_{ON} [KimSH'07]. Apparently, SNM has a negative correlation with DIBL [SongX'10]. In agreement to this, it is observed that the SNMs are considerably improved using proposed SymD-*k* architecture without affecting the design ratios *i.e.* CR and PR and cell area penalty.

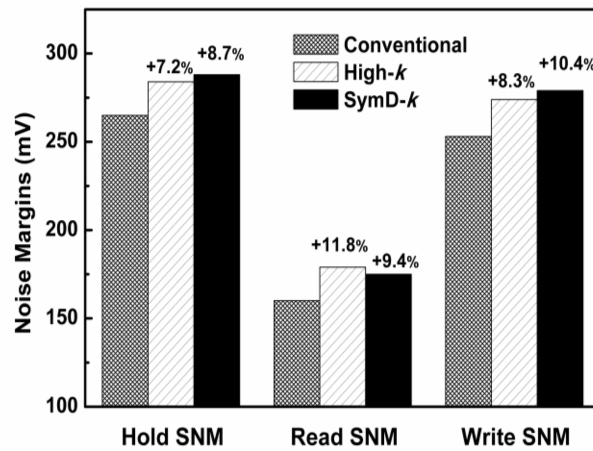


Figure 5.2. Comparison of hold SNM, read SNM and write margin among the conventional, purely high-*k* and SymD-*k* based 6T SRAM cells.

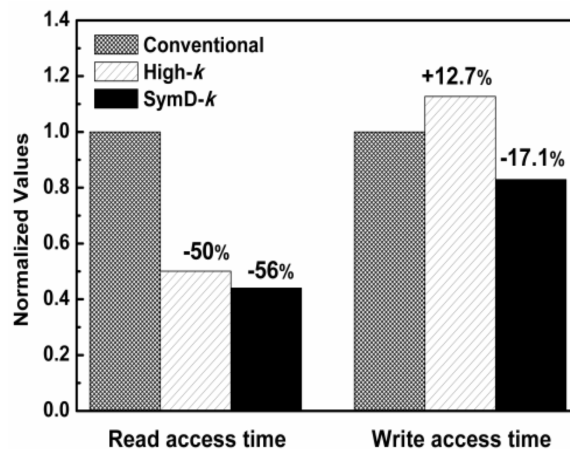


Figure 5.3. Comparison of read and write access time in purely high-*k* and SymD-*k* based 6T SRAM cells normalized with respect to the conventional one.

Furthermore, around 2.31× and 1.22× reductions in read and write access times, respectively compared to conventional one is depicted in Fig. 5.3. The read access time depends on the read cell current through the PA transistors therefore SymD-*k* cell outperform the other two cells. It is also observed that the purely high-*k* SRAM

cell proves to be better than the conventional in all respect except for the 12.7% increase in write access-time. The optimal high-*k* spacer length in SymD-*k* structure increases the I_{ON}/C_{GG} that helps in reducing write access time; however, the purely high-*k* based SRAMs shows worst write-delay among all. Although, the purely high-*k* based SRAM cell helps in stability enhancement and reduces read access time. But, it lacks in terms of write access-time and leakage power in comparison to the proposed SymD-*k* SRAM cell.

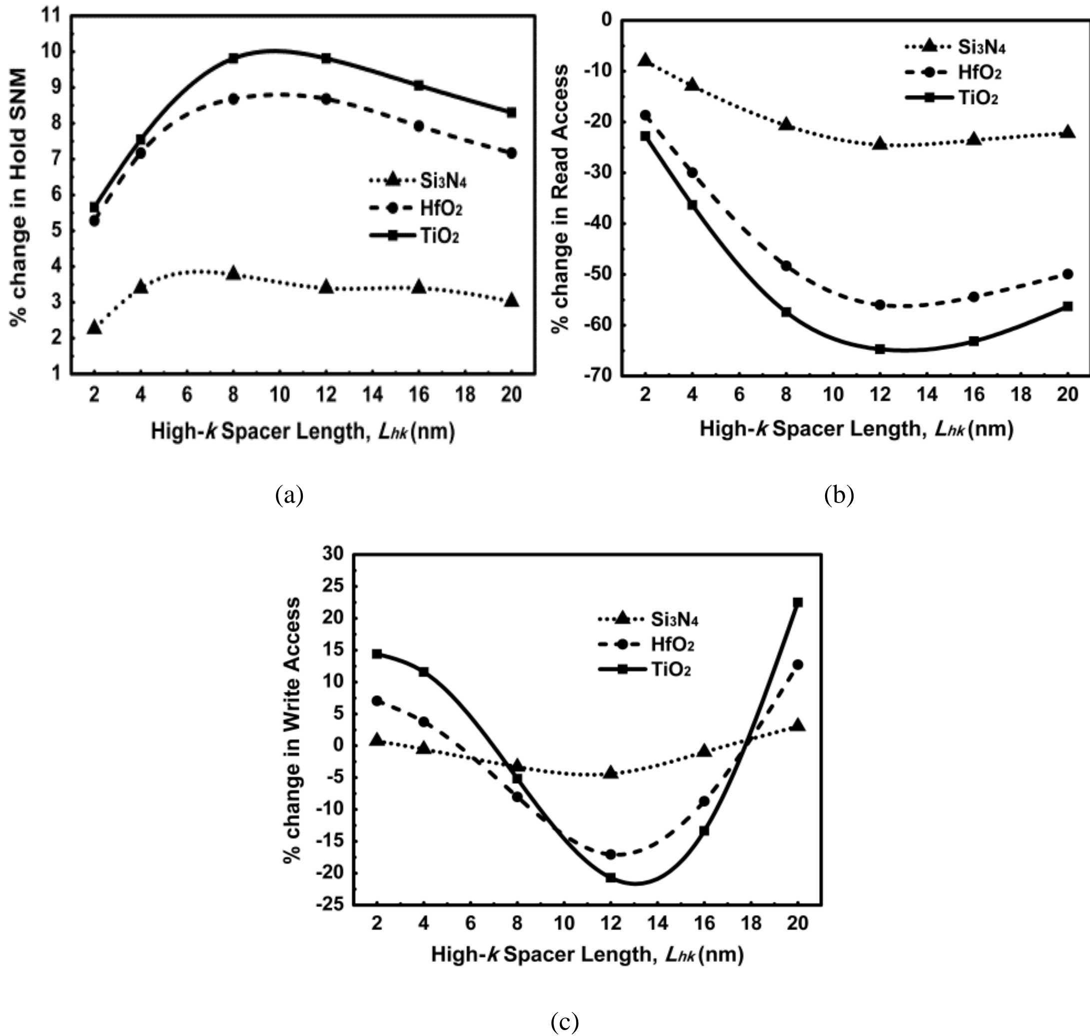


Figure 5.4. Percentage change in (a) hold SNM, (b) read access time, and (c) write-access time with respect to conventional FinFET based SRAM for different high-*k* values as function of L_{hk}.

Fig. 5.4(a)-(c) shows the percentage change in hold-SNM, read and write access time, respectively as a function of inner high-*k* spacer permittivity and length. It is observed that the reduced read/write access time and enhanced SNMs can be achieved by using an inner spacer length ranging from 8-12 nm for L_{un}= 8 nm, however, beyond this range the read-access and hold SNM slightly degrades. On the other hand,

increasing the value of *k* for L_{hk} outside the range of 10-15 nm degrades the write access-time more rapidly due to the higher C_{GD} [BansA'07]. Thus, the SymD-*k* device structure would be a better option for an overall improvement.

5.3.2 Asymmetric Dual-*k* (AsymD-*k*) FinFET based SRAM Cell

This sub-section describes AsymD-*k* architecture to enhance SRAM metrics in comparison to the conventional FinFET based SRAM. This asymmetric architecture exploiting the unequal source/drain currents that helps in modulating SRAM design ratios (cell-ratio and pull-up ratio) to improve read/write noise margins. There are two possible configurations based on asymmetric dual-*k* architecture that are AsymD-*k*S and AsymD-*k*D SRAM cells.

5.3.2.1 The AsymD-*k*D FinFET SRAM Configuration

In AsymD-*k*D cell configuration, the terminal having dual-*k* spacer of PU and PD transistors are connected to the storage nodes for implementing cross-coupled inverters. The access transistor (PA) terminal with dual-*k* spacer is connected to the bit-line and the other terminal with low-*k* is connected to the storage node. In this configuration, use of asymmetric current driving capability helps to enhance the hold, read SNM as well as write margin. The write-ability depends on the resistive divider action of PU and PA, and the access transistor strength must be larger than the PU transistor strength. During write operation, the terminal having a dual-*k* spacer of PA_R is at higher voltage; therefore the access transistor acts as AsymD-*k*S device with very high-current driving capability than PU_R (that operates as AsymD-*k*D structure with comparatively lower drive strength), resulting in higher write-ability.

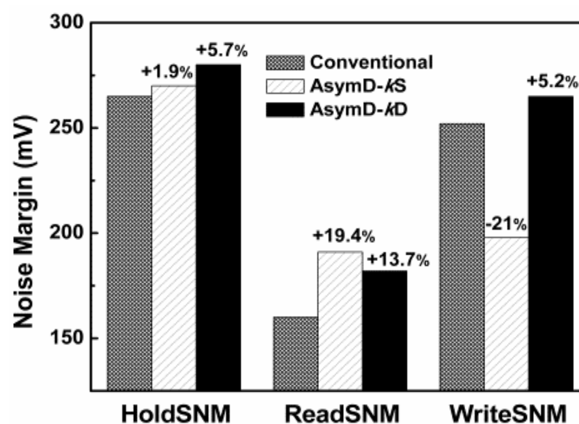


Figure 5.5. Comparison of hold, read and write margin amongst the conventional, AsymD-*k*S and AsymD-*k*D based 6T SRAM cells.

Similarly, the read stability depends upon the resistive divider action of PA and PD transistors. The storage node voltage is charged through the access transistor, and it must be less than the inverter threshold voltage to prevent cell from the read-failure. So, the pull-down transistor must be stronger than access transistor. It is also observed that the read stability is considerably improved using proposed AsymD-*k*D cell configuration. Moreover, it also mitigates the read/write conflict. Fig. 5.5 shows the comparison of noise margins to the conventional SRAM in all three possible modes of operation. The hold, read and write margins increase by 5.66%, 13.75% and 5.16%, respectively. Fig. 5.6 shows 14.38% reduction in write access time due to stronger access transistor during write mode and same read access time in comparison to the conventional FinFET based SRAM.

5.3.2.2 The AsymD-*k*S FinFET SRAM Configuration

In this SRAM cell configuration, AsymD-*k*S FinFET structure is used. The terminals having dual-*k* spacer of pull-up and pull-down transistors are connected to V_{DD} and GND, respectively to implement cross-coupled inverters. The access transistor terminal with low-*k* spacer is connected to the storage node and the terminal with dual-*k* is connected to the bit-line.

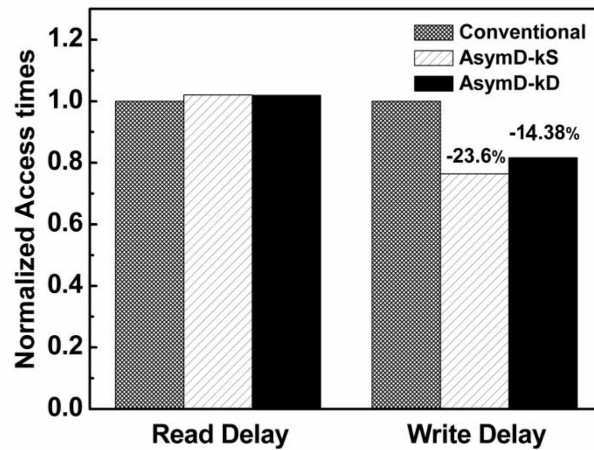


Figure 5.6. Comparison of read and write access time in AsymD-*k*S and AsymD-*k*D based 6T SRAM cell normalized with respect to the conventional.

Compared to the conventional SRAM, this configuration marginally increases hold SNM by 2%, due to better short channel characteristics [BansA'07]. During read mode, the access transistor terminal having dual-*k* spacer is on high potential whereas pull-down transistor terminal with dual-*k* spacer is at ground. So, PD_L strength increases more as compared to PA_L that in turn increases CR and hence read stability.

The asymmetry between access and pull-down transistors almost doubles the CR that enhances read stability by 19.35%. However, nearly 20% decrement in write-margin is observed due to the increased pull-up transistor strength as compared to access transistor, which increases PR (even greater than that of conventional SRAM cell).

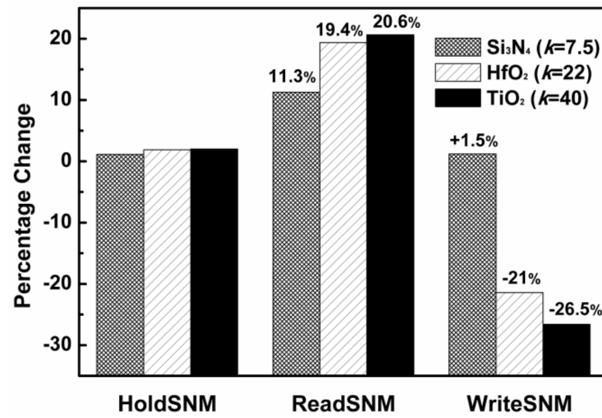


Figure 5.7. Percentage change in SNM (hold, read and write modes of operation) as a function of inner high-*k* spacer material in AsymD-*k*S SRAM cell configuration.

Fig. 5.7 shows the percentage change in SNM as a function of high-*k* spacer material. It is observed that with an increase in inner spacer permittivity, both the hold and read SNM increases however, the write-margin degrades. This reduced write-margin can be overcome by using an inner spacer of dielectric value ranging from 7-15, but it slightly degrades read SNM as well. Moreover, without affecting the read SNM in AsymD-*k*S SRAM cell; the write-margin can also be improved by using write-assist circuitry. For almost same read delay, the write delay is substantially reduced by 23.63% due to better drive current of stronger PA_R and PU_R.

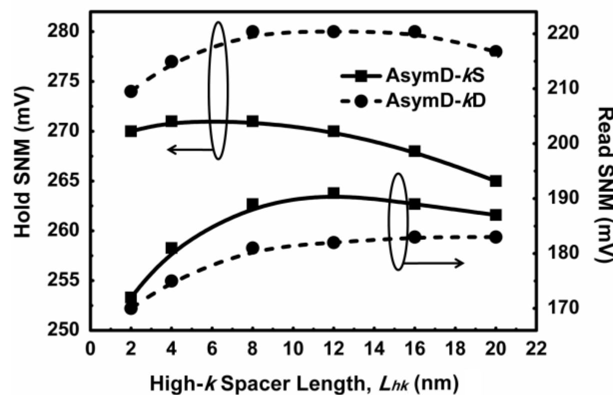


Figure 5.8. Effect on hold and read SNM as function of L_{hk}.

Fig. 5.8 compares the hold and read SNM of AsymD-*k* cell configurations. It is observed that both SNMs are at peak for the optimum L_{hk} and thereafter, it reduces.

The asymmetry in terms of I_{ON} between the AsymD-*k*S and AsymD-*k*D structures are maximum at the optimal point (L_{hk}=12 nm) (as observed from Fig. 3.20), thus the enhancement in CR and read SNM is maximum at this point.

5.4 Effect of Supply Voltage on Dual-*k* based SRAM Cells

Reducing leakage in SRAM is critical for overall reduction of static power consumption in nano-regime [GiraB'09]. Supply voltage reduction is a technique for lowering leakages but reduction in noise immunity limits the supply voltage lowering [VataE'08]. Therefore, V_{DD} scalability on SRAM design metrics needs to be explored.

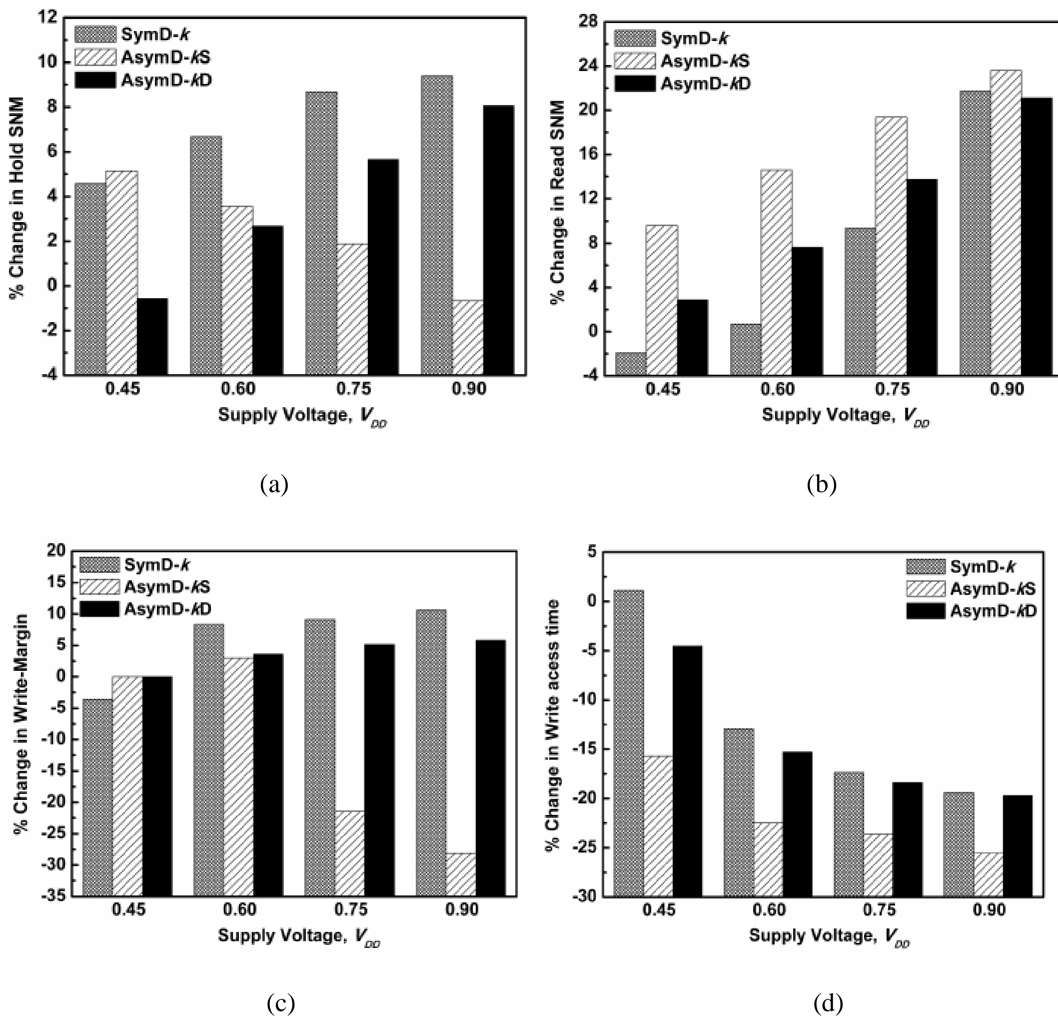


Figure 5.9. Percentage change in (a) hold, (b) read, (c) write SNM, and (d) write-access time as function V_{DD} for SymD-*k* and AsymD-*k*S, AsymD-*k*D SRAM cell with respect to the conventional cell.

Fig. 5.9(a-d) presents the effect of lowering the V_{DD} on SNMs (in hold, read and write mode) and write-access time, respectively. Compared to the conventional cell, SymD-*k* FinFET based SRAM configuration shows an improvement of 4.5-9.4% in

hold SNM; and up to 21.7% in read stability for supply voltage ranging from 0.45-0.9 V. Consequently, the write-margin enhances upto 10.6% and write access time reduces by 19.4%. In contrast to this, AsymD-*k*D FinFET based SRAM configuration shows 2.8-21.2% improvement in read SNM, 3.6-5.82% in write-margin, 2.6-8.0% increase in hold SNM and 4.5-19.7% reduction in write access time. Furthermore, AsymD-*k*S based SRAM demonstrates 5.3-23.6% higher read SNM and a marginally higher hold SNM at the expense of 15.8-21.5% write-margin. Similar to the inverter VTC (as shown in Fig. 4.15), it is observed that the hold SNM in AsymD-*k*S cell also reduces with an increase in supply voltage. Conversely, SymD-*k* and AsymD-*k*D SRAM cell performs better in above-threshold region and shows significant improvement with higher V_{DD}. The obtained results show that the proposed SymD-*k* and AsymD-*k*D based SRAM configurations are not viable candidate in sub-threshold region of operation. The percentage improvement metrics decreases with scaling down of supply voltage. This is due to the reduction in gate fringe coupling through inner high-*k* spacer that increases series resistance with reduced V_{DD}.

5.5 Symmetric and Asymmetric Dual-*k* SRAM Cell Comparison

The robustness of an SRAM cell is commonly evaluated by the SNMs during hold and functional operations of read and write. These three metrics (hold SNM, read SNM, and write SNM) are widely used for design and performance analysis of SRAM cell.

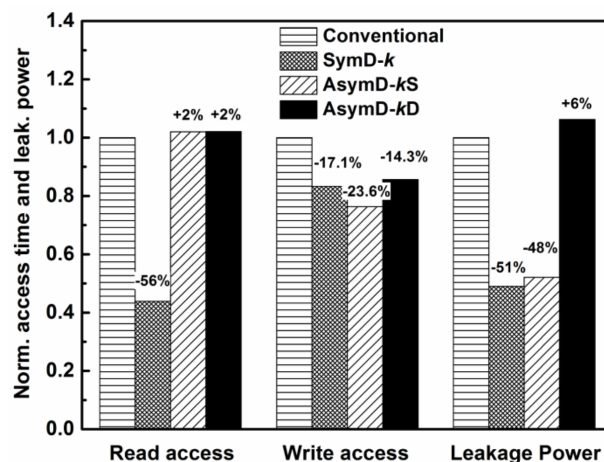


Figure 5.10. Comparison of read/write access time and cell leakage power in symmetric and asymmetric dual-*k* spacer based SRAM cells normalized with respect to the conventional one.

Fig. 5.10 compares the read/write access time and 1-bit SRAM cell leakage power amongst the conventional, SymD-*k*, AsymD-*k*S and AsymD-*k*D based SRAM cells.

For SymD-*k* cell, around 56% and 17% reductions in read and write access time, respectively are achieved in comparison to the conventional cell as depicted in Fig. 5.10. However, nearly 24% improvement in write access time is observed in AsymD-*k*S with a marginal loss in read access time by 2%. The write access times in 6T SRAM cell using the symmetric dual-*k* architecture is significantly reduced due to their higher I_{ON}/C_{GG}. Primarily, the read access time depends on the read cell current through the access transistors therefore SymD-*k* outperforms the rest structures.

Standby leakage power in SRAM is another critical concern that seriously impacts the battery life. The sub-threshold current (I_{SUB}) current and the gate tunneling current (I_G) are considered as the dominant leakage current components to evaluate the total leakage current in an SRAM cell [BansA'07]. Fig. 5.10 shows the estimated leakage power of 1-bit SRAM cell normalized with respect to the conventional FinFET based cell. In OFF-state, I_{SUB} and $I_{EDT\text{-}OFF}$ (or, $I_{G\text{-}OFF}$) dominate the total leakage current and both reduce with an increase in L_{un} [MukhS'05]. The sub-threshold leakage component in SymD-*k* and AsymD-*k*S structures are much lesser than the conventional because of better electrostatic integrity. Therefore, nearly 50% reduction in cell leakage power is observed for SymD-*k* and AsymD-*k*S based SRAM cell with respect to the conventional. Although, the AsymD-*k*D based SRAM cell mitigates read/write conflict, but its total leakage power is almost double than AsymD-*k*S based SRAM cell. It is due to the higher sub-threshold current in AsymD-*k*D structure.

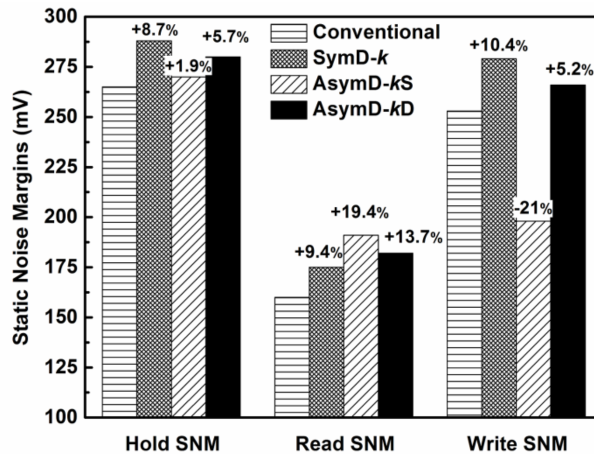


Figure 5.11. Comparison of hold SNM, read SNM and write-margin amongst the conventional, symmetric and asymmetric dual-*k* spacer based SRAM cells.

Fig. 5.11 compares the SNMs (extracted from the conventional butterfly curves) amongst the conventional, SymD-*k* and AsymD-*k* based SRAM cells. It is observed

that the hold margin in SymD-*k* and AsymD-*k*S SRAMs are increased by 8.6% and 1.2%, respectively, because of the improved drive current. In comparison to the conventional SRAM bit cell, the improvement observed in read SNM of AsymD-*k*S based cell is much higher (19.4%) than the SymD-*k* based cells (9.4%). This read SNM improvement in AsymD-*k*S based SRAM cell is due to its asymmetric nature that helps in adjusting the PR and CR to augment the stability. Contradictorily, the improvement in SymD-*k* cell is attributed to the enhanced electrostatic integrity that increases SNM without affecting PR and CR. Therefore, it is not justified to directly compare the cell by using only voltage margins *i.e.* SNMs.

For a suitable comparison among the architectures, it is necessary to explore the architectures on a common metric that clearly distinguish their superiority in SRAM applications. The N-curve [WannC'05] metric provides an alternative approach for both current and voltage stability analysis that also satisfies our requirement of comparing SRAM performance on a common platform. As an attractive approach, N-curve also contains information for both read stability and write stability. The extracted N-curve has three intersection points A, B, and C wherein points A and C correspond to stable state points while point B is a meta-stable point [SingJ'13].

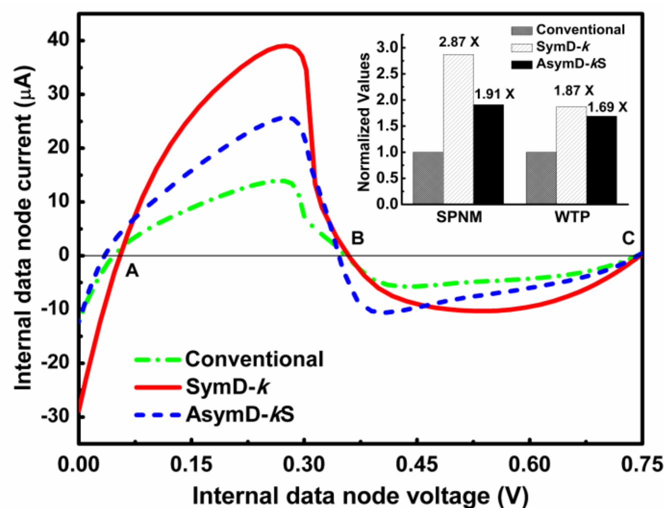


Figure 5.12. N-curves and the read/write power margins of conventional, SymD-*k* and AsymD-*k*S based 6T SRAM cells.

The stability metrics derived from the N-curve are based on the combined voltage and current information for a SRAM cell [SingJ'13]. The static voltage noise margin (SVNM) is defined as a maximum tolerable DC noise voltage at internal nodes of the cell before its content flips and it is measured as a voltage difference between points

B and A. Similarly, static current noise margin (SINM) can be defined as a maximum tolerable DC noise current injected at internal nodes of the cell before its content changes and it is measured as a peak current located between points A and B. These two metrics SVNM and SINM are used to characterize the cell read stability. Similarly, the write stability can be characterized with the help of write-trip voltage (WTV) and write trip-current (WTI). The WTV is the minimum voltage drop needed to change the internal nodes of the cell, which can be measured as a difference between points C and B. The WTI is defined as a minimum amount of the current needed to write the cell, which can be measured as a negative current peak between points C and B. An overlap of points A and B means that the cell is at the edge of stability loss, as a result, destructive read operation can easily occur. Similarly, overlapping of points B and C may lead to failure in write operation.

It is observed from the N-curves shown in Fig. 5.12 that the SymD-*k* cell shows better SINM because of high current driving capability and slightly reduced SVNM (due to same cell-ratio) as compared to its asymmetric counterpart AsymD-*k*S SRAM cell. Contrastingly, the AsymD-*k*S cell has higher SVNM due to increase in cell-ratio and lower SINM. Therefore, in case of these contradictory results, it would be beneficial to derive the power margins [*i.e.* static power noise margin (SPNM) and write trip power (WTP)] that include both voltage and current information for read/write stability. The SPNM is defined as the maximum tolerable DC noise power by the internal data storage nodes of a cell before its content changes and it is measured as the area under the curve between points A and B. Similarly, the WTP characterizes the write stability of a cell that is measured as the area bounded by the curve and *x*-axis between points B and C. The inset in Fig. 5.12 shows the power margin comparisons of SymD-*k* and AsymD-*k*S based 6T SRAM cell normalized with respect to the conventional one. For SymD-*k* cell, it is observed that the SPNM and WTP increase by 2.87 × and 1.87 ×, respectively, whereas, SPNM and WTP increase by 1.91 × and 1.69 ×, respectively for AsymD-*k*S based cell. The percentage change in SINM with respect to SVNM is more in case of SymD-*k* than AsymD-*k*S. Hence, the higher power margins (or area under the curves) observed in case of SymD-*k* cell as compared to the AsymD-*k*S cell. Based on the observations of read/write power margins, SymD-*k* structure outperforms the AsymD-*k*S for SRAM applications.

5.6 Summary

This chapter investigated the proposed SymD-*k* and AsymD-*k* architectures for high performance memory application. The proposed dual-*k* based SRAM cell yields a large reduction in leakage power, improved noise margins and reduced access time. For SymD-*k* cell, around 56% and 17% reductions in read and write access time, respectively are achieved in comparison to the conventional cell. Further, nearly 24% improvement in write access time is observed in AsymD-*k*S with a marginal loss in read access time by 2%. In terms of power margins, the SPNM and WTP in SymD-*k* cell increase by 2.87 × and 1.87 ×, respectively, whereas, SPNM and WTP increase by 1.91 × and 1.69 ×, respectively for AsymD-*k*S based cell. Moreover, there are no cell area penalties associated with proposed configurations because the device dimensions are same in all respects. Thus, the proposed dual-*k* SRAM configurations prove to be better than the conventional memory cell in terms of voltage, current and power margins.

CHAPTER 6

Statistical Variability and Sensitivity Analysis of Dual-*k* FinFETs

6.1 Introduction

Process variability has emerged as one of the major concerns in sub-20 nm gate lengths. Primarily, process variations can be classified as *systematic* and *random*. The systematic variations are predictable in nature and it depends on various deterministic factors such as layout structure and surrounding topological environment [OrshM'00, MehrV'00]. On the other hand, random variations are totally unpredictable and are caused by random uncertainties in the fabrication process such as microscopic fluctuations in the number and location of dopant atoms in the channel region [TangX'97]. Random variations are harder to characterize and can have a negative effect on the yield of critical modules in a design. Random variations can cause a significant mismatch in neighboring devices and hence are largely responsible for the poor yield in complex circuits such as SRAMs [ChenB'04].

As memory will continue to consume a large fraction of the area in future ICs, scaling of memory density must continue to track the scaling trends of logic. Due to the technology scaling, process variations is a critical issue for SRAM stability [ChenB'04]. There are various statistical variability sources for FinFET based SRAM that affects the stability and these issues are required to be addressed. Random discrete dopant fluctuations RDF), gate oxide roughness variations (TOX), and metal-grain dependent work-function variations (WFV) increase the spread in threshold voltage and thus the ON- and OFF- currents as the device is scaled down in the nanoscale regime. Increased transistor leakage and parameter variations present the biggest challenges for the scaling of 6T SRAM memory arrays. Therefore, for an optimized FinFET SRAM design, solutions are needed to address these issues. Moreover, the control of key structural dimensions such as L_G, T_{fin} *etc.* continues to be very difficult, due to technological (lithographic and etching) restrictions.

The significance of random variability and sensitivity of key structural parameters in nano-scaled tri-gate transistors increases sharply with the downscaling of device dimensions below 20 nm gate lengths that can fail out any design. Therefore, it is

necessary to investigate the proposed dual-k devices and its circuit performance under process variations. This chapter briefly presents a comparison amongst the conventional, SymD-k and AsymD-kS tri-gate architectures based on device/SRAM parameters such as V_{th}, I_{ON}, I_{OFF}, and SNMs under random (specifically RDF, TOX, WFV) and parametric (T_{fin}, L_{hk}, DSL) variations.

6.2 Impendence Field Method (IFM) and TCAD Simulation Setup

As transistor scaling continues, self-averaging of device properties for individual devices becomes less effective and, therefore, the statistical variability of device properties becomes more prominent. For the investigation of variability in single transistors, so called "atomistic" approaches have been proposed to investigate the variability for MOSFETs [ChenB'07]. Such methods rely on 3D TCAD simulations of a large number of independent randomized 3D realizations of the device structure. The computational resources needed for the "atomistic" approach are directly proportional to the number of randomized device structures in the statistical sample. Such an approach is therefore naturally limited to smaller devices with simplified geometries [ChenB'07].

The application of atomistic methods to 3D six-transistor (6T) SRAM cells with realistic geometries seems to be extremely difficult. For the exploration of random variability in SRAM cells, quite a large number of theoretical- and simulation-based approaches were reported [BhavA'01, HuVP'11, HiraT'11]. In [BhavA'01], analytic approximations are used. In [HiraT'11], the SRAM cell is modeled using SPICE-type simulations where transistors are represented as compact models. In [HuVP'11], 3D technology computer-aided design (TCAD) simulations for an entire SRAM cell are presented, where the cell geometric and doping profiles are defined analytically.

Recently, the statistical impedance field method (IFM) is reported as a viable alternative to atomistic and SPICE-based approaches. The IFM in TCAD provides a fast, convenient, and accurate alternative for statistical variability analysis [SayeK'12b]. The basic concept behind the IFM is to treat randomness as a perturbation of a reference device. Rather than solving the full nonlinear Poisson and drift-diffusion equations for a large number of random device realizations, the 3D TCAD solution is obtained only once for the reference device. Then, the current fluctuations at the device terminals caused by these random perturbations are

computed. These computations are based on linear response theory using Green's function technique [BonaF'98, WettA'03]. The IFM can be applied to different kinds of perturbations, including geometric fluctuations and work function fluctuations. The most prominent advantage of the IFM method is that it is applicable to large device structures and can also readily handle realistic geometries. Statistical IFM also can be used for more complex applications, such as the investigation of the static noise margin variability of SRAM cells [SayeK'12a]. The computational resource requirements depend weakly on the number of randomized devices included in the statistical sample.

The random device-circuit variability of proposed SymD-*k* and AsymD-*k*S architectures are investigated in terms of random discrete dopant (RDF) induced variations, gate oxide roughness variations (TOX), and metal grain dependent work-function variations (WFV). The doping profile is randomized according to the Sano's method [SanoN'02]. To obtain statistical samples, the doping is spatially uncorrelated and that the number of dopants in a given volume follows a Poisson distribution, with an average number of dopants in the volume.

To study the WFV, gate metals TiN and MoN are used for *n*-type and *p*-type, respectively [RasoS'14]. TiN metal exhibits random positional dependency of two possible grain orientations, *i.e.* <200> and <111>, of 4.6 and 4.4 eV work-function values, with 60%, and 40% probabilities of occurrences, respectively. Similarly, MoN exhibits 5.0 and 4.4 eV for grain orientations of <110> and <112>, with 60% and 40% probabilities of occurrences, respectively. The average grain sizes for TiN and MoN metals are 22 nm and 17 nm, respectively. For gate oxide roughness (TOX), a procedure similar to the WFV is used. Here, in each "grain" along the surface, the oxide thickness is modified. In this chapter, all the random variability simulations using IFM are carried out at a supply voltage of 1 V.

6.3 Results and Discussions

This section briefly presents the comparison amongst conventional, SymD-*k* and ASymD-*k*S FinFET architectures based on the performance parameters such as I_{ON}, I_{OFF}, V_{th}, inverter delay and SRAM static noise margin (SNM) under random statistical and parametric variations.

6.3.1 Statistical Variability of SymD-*k* and AsymD-*k*S Structures

The random device-circuit variability of both the SymD-*k* device and the conventional device are investigated in terms of RDF, TOX, and metal grain dependent WFV. The numerical comparison of the standard deviations and the relative variation for V_{th}, I_{ON}, and I_{OFF} is summarized in Table 6.1 and their total impact is shown in Fig. 6.1.

TABLE 6.1

STANDARD DEVIATION AND ITS RELATIVE VARIATION (IN %) OF DEVICE PARAMETERS IN CONVENTIONAL, SYMD-*K* AND ASYMD-*K*S TRI-GATE FINFET ARCHITECTURES

		V_{th} (mV)			I_{ON} (μA)			I_{OFF} (pA)		
		Conv	**SymD-*k***	**AsymD-*k*S**	**Conv**	**SymD-*k***	**AsymD-*k*S**	**Conv**	**SymD-*k***	**AsymD-*k*S**
RDF	σ	4.61	4.38	4.11	1.60	2.50	1.56	8.93	6.48	4.62
	%	1.91	1.60	1.65	8.58	5.73	4.23	11.01	12.21	11.66
TOX	σ	6.39	1.84	4.11	0.82	1.45	0.79	34.29	7.75	15.44
	%	2.65	0.67	1.65	4.40	3.33	2.14	42.39	20.52	29.49
WFV	σ	17.95	16.10	17.70	0.38	0.73	0.38	37.68	16.98	24.20
	%	7.43	5.87	7.12	2.06	1.68	1.04	46.36	44.86	46.22
Total	σ	19.58	16.79	18.67	2.14	2.99	1.79	45.87	18.12	26.96
	%	8.11	6.12	7.51	9.67	6.85	4.86	56.69	47.89	51.61

It is observed that both SymD-*k* and AsymD-*k*S structures are more immune to random variations as compared to their conventional counterpart. As the channel and underlap region is lightly doped in all considered structures, therefore a reduced threshold (V_{th}) fluctuation *i.e.* ~1.6-1.9% is observed under RDF induced variations. The σV_{th} due to oxide thickness variations in SymD-*k* and AsymD-*k*S are observed as 1.84 and 4.11 mV, respectively in comparison to 6.39 mV in conventional device. However, the effect of work-function on σV_{th} is significantly higher due to enhanced grain oriented work-function difference. Overall, the SymD-*k* architecture

demonstrates reduced V_{th} variations to their mean values due to its superior electrostatic and enhanced gate controllability over the channel in comparison to the AsymD-*k*S and conventional devices.

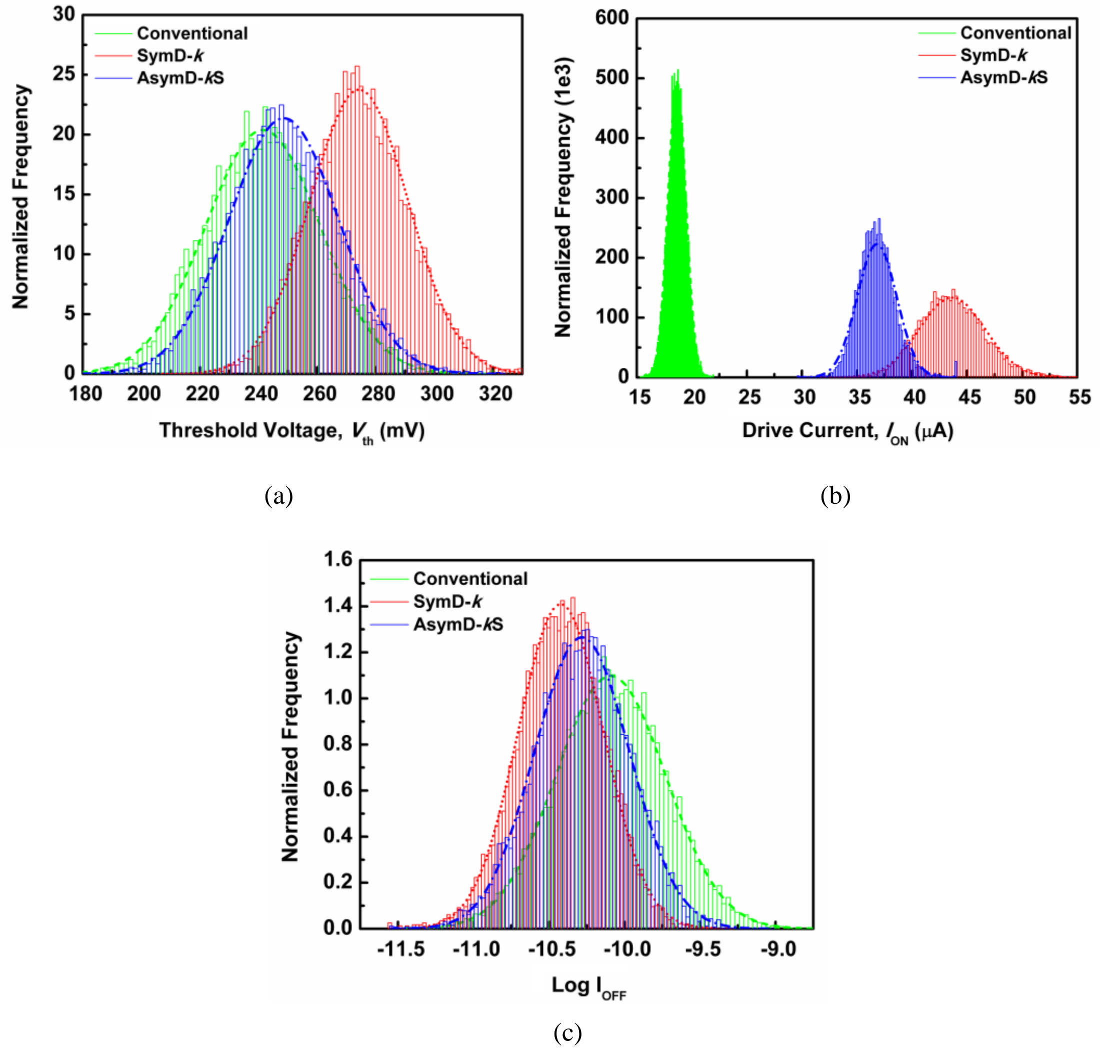


Figure 6.1. Total statistical variability's of (a) threshold voltage, (b) drive current and (c) Log I_{OFF} of conventional, SymD-*k* and AsymD-*k*S considering RDF, TOX and WFV.

On the other hand, it is observed that the AsymD-*k*S device outperform the other architectures in terms of I_{ON} variation. In AsymD-*k*S device, an ON -current deviation with RDF is relatively lower than the other architectures. It is because of the highly concentrated carriers near the G/S surface and enhanced fringing field that in turn establishes immunity to I_{ON}. It is observed that the current distribution (σI_{ON}) and percentage variation ($\sigma I_{ON}/<I_{ON}>$) in ON-state are less affected due to TOX and WFV as compared to RDF variations. Contrastingly, the σI_{OFF} and ($\sigma I_{OFF}/<I_{OFF}>$) are highly affected by TOX and WFV as compared to RDF variations.

The percentage variations due to TOX and WFV obtained in I_{OFF} for SymD-k structure are much better than the AsymD-kS and its mean value ($<\sigma I_{OFF}>$) is more than 2× lower than the conventional one. Percentage variations of all parameters are found to be much lower (except for a marginally higher I_{ON}) in SymD-k based device compared to the AsymD-kS and conventional devices. The WFV induced variations on I_{ON} are comparable for both the devices, given that the mean value ($<I_{ON}>$) for SymD-k is 2.4× higher than the conventional one.

6.3.2 Statistical Variability of SymD-*k* and AsymD-*k*S based SRAM cells

There is an emerging need of robust and high performance SRAMs since memories occupy most of the die area in processors [ITRS]. Semiconductor memories have large number of transistors wherein a small variation in device parameter leads to failure of read/write operations. Variations in device dimensions can severely affect the balance of transistors ratio that often degrades the read/write stability. This sub-section describes the design metric outcome and statistical variations of SymD-k and AsymD-kS FinFET based SRAM cells in comparison to the conventional one.

TABLE 6.2

STANDARD DEVIATION AND ITS RELATIVE VARIATION OF HOLD/READ-SNM IN CONVENTIONAL, SYMD-*K* AND ASYMD-*K*S BASED SRAM CELLS

		Hold SNM			**Read SNM**		
		Conv.	SymD-*k*	AsymD-*k*S	Conv.	SymD-*k*	AsymD-*k*S
RDF	Std. dev (mV)	37.07	10.16	7.73	35.16	12.94	17.97
	% variations	11.58	2.98	2.53	21.55	6.25	8.77
TOX	Std. dev (mV)	0.90	0.75	0.50	1.97	1.27	1.45
	% variations	0.27	0.22	0.16	1.11	0.59	0.68
WFV	Std. dev (mV)	16.39	13.93	16.28	14.50	11.82	15.67
	% variations	5.06	4.12	5.43	8.65	5.71	7.71

From SRAM perspectives, both the SymD-*k* and AsymD-*k*S based 6T cells yield improved noise margins and reduced access times, without affecting the cell area. Compared to the conventional SRAM cell, SymD-*k* cell improves read SNM by 5%, 9.4%, and 10.6% for spacer material of Si_3N_4, $HfO_{2,}$ and TiO_2 respectively. Moreover, the write-access time substantially reduces by 4.4%, 17.1%, and 20.7% for spacer material of Si_3N_4, $HfO_{2,}$ and TiO_2 respectively. It is due to the improved current/capacitive behavior at an optimum L_{hk} of 12nm. As the read-access time primarily depends on the current driving capability of an access transistor, hence a large improvement of ~24-64% is observed for spacer permittivity ranging from 7.5-40.

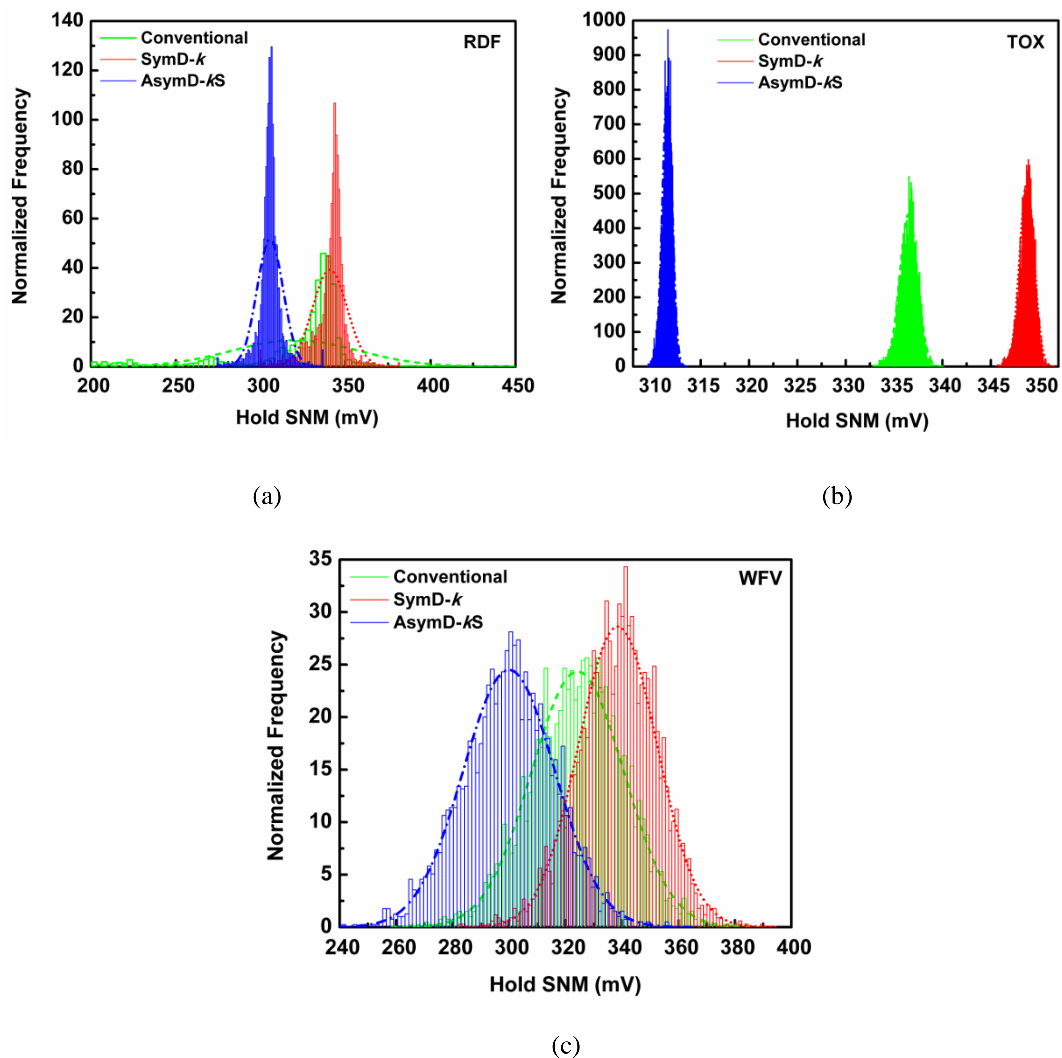


Figure 6.2. Statistical variability of Hold SNM of conventional, SymD-*k* and AsymD-*k*S based 6T SRAM cells as a function of (a) RDF, (b) TOX and (c) WFV.

The improvement observed in SymD-*k* and AsymD-*k*S device parameters and its relative variations in turn improves SRAM variability also. The random variability

effects on hold and read SNMs are shown in Fig. 6.2 and 6.3, respectively using conventional, SymD-*k* and AsymD-*k*S structures. Moreover, the relative variations (in %) and standard deviations for hold and read SNMs are shown in Table 6.2. The relative variations in SRAM performances are found to be much lower using SymD-*k* device in comparison to the conventional FinFET.

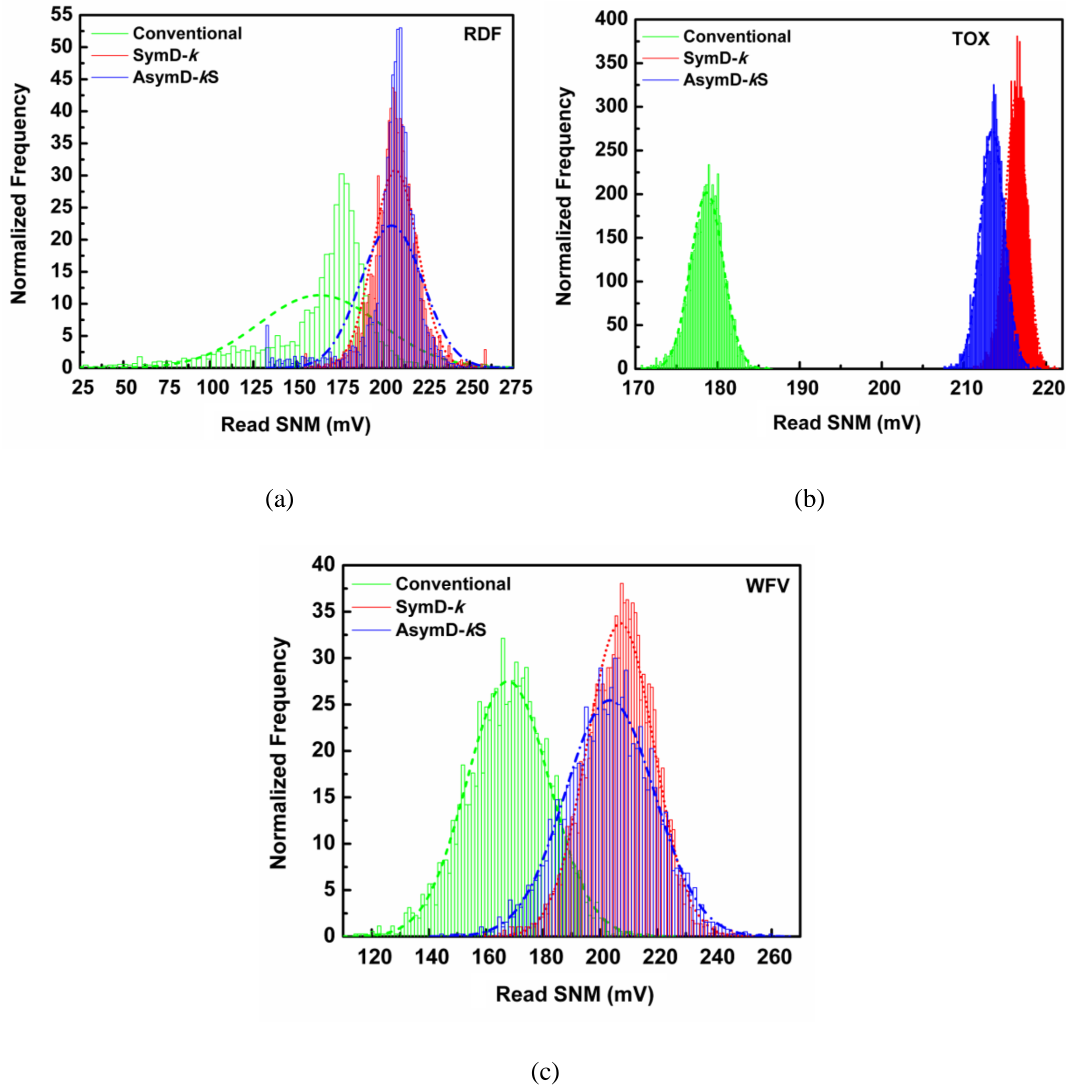


Figure 6.3. Statistical variability of Read SNM of conventional, SymD-*k* and AsymD-*k*S based 6T SRAM cells as a function of (a) RDF, (b) TOX and (c) WFV.

6.3.3 Sensitivity Analysis

The sensitivity analysis provides a relative significance of each device parameter on the performance metrics. The sensitivity metric on a parameter (p) is defined as:

$$S(M) = 100 \times \left[\frac{(\delta M / M)}{(\delta p / p)} \right]$$

Where, M is the performance parameter that depends on device parameters (p), such as silicon film thickness (T_{fin}), inner high-k spacer length (L_{hk}), and dopant segregation length (DSL).

TABLE 6.3

SENSITIVITY (IN PERCENTAGE) OF CONVENTIONAL, SYMD-k AND ASYMD-kS STRUCTURE CONSIDERING ±20% STRUCTURAL VARIATIONS

Sensitivity (%)	Conv.		SymD-k			AsymD-kS		
	T_{fin}	DSL	T_{fin}	DSL	L_{hk}	T_{fin}	DSL	L_{hk}
V_{th}	28	5	14	2	2	20.9	4	1.9
I_{ON}	44	67	23	64	44	37.5	56.2	26.9
I_{OFF}	560	76	368	58	32	448.3	72.8	25.5
C_{GG}	36	14	17	23	64	18	27	57.5
SS	20	5	14	4	1	15.2	4.98	0.7
Inverter delay	19	31	9	23	11	7.6	19	13.3

Table 6.3 compares the performance of SymD-k and AsymD-kS devices with the conventional one by considering ±20% variation in key structural parameters. It is observed that the inverter delay in SymD-k (AsymD-kS) structure is nearly 2.1× (2.5×) and 1.34× (1.63×) lesser sensitive to the T_{fin} and DSL variation, respectively in comparison to its conventional counterpart. Both the SymD-k and AsymD-kS inherently introduce an additional source of structural sensitivity *i.e.* inner high-k spacer length (L_{hk}) that actually favors the charge dynamics in the channel. Due to an optimized L_{hk}, the fringe capacitance component is much higher in case of dual-k, consequently, the overall gate capacitance is more responsive to L_{hk}. In both the proposed dual-k architectures, the optimization of L_{hk} depends on DSL; therefore, the inverter delay is more sensitive to L_{hk} and DSL as compared to T_{fin}. The silicon film thickness marginally affects the dynamic performance of circuit while it highly amends the short channel characteristics such as I_{OFF} and sub-threshold slope.

6.4 Summary

This chapter analyzed the random variability and structural sensitivity of proposed SymD-*k* and AsymD-*k*S architecture. In comparison to the conventional one, SymD-*k* (AsymD-*k*S) architecture improves the random variations of V_{th}, I_{ON}, and I_{OFF} by 24.5% (7.39%), 29.16% (49.74%), and 15.5% (8.96%), respectively. Furthermore, the SymD-*k* based SRAM cell also exhibits more immunity to hold and read SNMs. It is also observed that the inverter delay in SymD-*k* structure shows lesser sensitivity, nearly 2.1× (2.5×) and 1.34× (1.63×) to the T_{fin} and DSL, respectively. Overall, both dual-*k* architectures exhibit least sensitivity to random variations in comparison to their conventional counterpart that prove them to be the suitable candidates for high-performance device/circuit applications in sub-20 nm nodes.

CHAPTER 7

Conclusions and Future Scope

This chapter concludes the major research work carried out in this thesis. It summarizes the major outcomes and the contributions of this study in enhancing the spacer engineered device/circuit co-design performance in sub-20 nm technology nodes.

7.1 Conclusion

The research work presented in this thesis primarily focuses on the novel spacer engineered FinFET architectures that smartly use the high-permittivity materials targeting high-performance device-circuit co-design (from device to circuit/SRAM perspective) and its immunity to random statistical and structural variations. Overall, this research work is broadly divided into four major parts. The first part dealt with the device level analysis wherein the dual-permittivity (*k*) spacer concept and the optimization strategy of the same were introduced. It also described the proposed symmetric (SymD-*k*) and asymmetric dual-*k* (AsymD-*k*) architectures, their fabrication methodology and the superior ON- and OFF-state electrostatics over the conventional (single/low-*k* spacer) as well as purely high-*k* spacer underlap FinFET structure. It is observed that the high-*k* spacer length should be optimized to underlap and its nearby lightly doped area so that the fringe-field line converges only towards the high energy barrier which helps in reducing the extra $R_{S/D}$. It is observed that the carrier concentration increases with an increase in the inner high-*k* spacer length till it reaches a value of 12 nm. Beyond this optimum point, the fringing-field lines do not affect much the laterally diffused S/D region that already has very high carrier concentration. Therefore, there is no need to place high-*k* spacers above the highly doped laterally diffused area that may otherwise lead to higher parasitic capacitances and trap charges. Consequently, beyond an optimal L_{hk} of 12 nm (for an underlap length, L_{un} = 8 nm), the device performance starts degrading. The proposed symmetric and asymmetric dual-*k* structures have high-*k*/low-*k* spacer interface regions that make it different from the conventional and purely high-*k* structure. This interface region actually improves the device electrostatics of the proposed architectures. The difference in spacer permittivity at interface region modifies the electric field path that

results in superior electrostatics in both ON and OFF-state. We have also physically interpreted the ON/OFF state electrostatics associated with dual-*k* structure with an increase in inner spacer *k* value. From this, an important and novel observation was made that the conduction band energy (CBE) barrier (in ON-state) directly under the gate increases in proposed architectures which otherwise remains same in high-*k* device even though the inner spacer permittivity is increased substantially. Furthermore, the symmetric and asymmetric dual-*k* architectures are analyzed to observe the competing effects of spacer engineering. It is observed that the source-side spacer mainly governs the charge transport from source to drain in underlap devices; however, the drain side spacer helps to slightly enhance the current magnitude in SymD-*k* compared to AsymD-*k*S.

In second part of this work, the role of fringe capacitances associated with the proposed architectures is described that also demonstrated the suitability of high-*k* spacer materials for high-performance logic circuits improving noise-margin and delay, simultaneously. The circuit performances are evaluated based on the static and dynamic characteristics of a CMOS inverter and a three-stage ring oscillator. A purely high-*k* device could be beneficial in enhancing stability but at the cost of exorbitant increase in fringe capacitance, that in turn worsens the delay performance. Although, the proposed dual-*k* structures exhibit larger fringe capacitances than the conventional one, but with an optimized L_{hk} of 12 nm, both proposed SymD-*k* and AsymD-*k*S architectures shows better inverter delay performances. This superior delay performance is due to the high C_{GS} component that increases the carrier density resulting in higher ON-current. The AsymD-*k*S outperforms SymD-*k* architecture due to higher C_{GS} and smaller C_{GD} values. Beyond an optimum L_{hk} of 12 nm in SymD-*k* device, the C_{GD} component sharply increases and the C_{GS} reduces that degrades the delay performance. On the other hand, the inverter delay worsens in AsymD-*k*D device because of the lower C_{GS} and a higher value of Miller component of C_{GD}. For AsymD-*k*S and SymD-*k* architectures, it is observed that the C_{GS} increases sharply up to L_{hk}= 12 nm and thereafter it decreases marginally. However, for AsymD-*k*D architecture, it remains low and almost constant. Moreover, an important observation is made that the delay performance improvement was more pronounced with higher permittivity of the spacers in dual-*k* spacer technology. The effect of power supply scalability on dual-*k* FinFET based inverter/RO3 is also presented.

Motivated by the superior device electrostatics and circuit performance, the third part of this thesis explored the possibilities of symmetric and asymmetric dual-*k* architecture for augmenting the SRAM design metrics. SRAM cell performances are evaluated in terms of SNMs (hold, read, and write), read/write access times, and total cell leakage power. Implementation of proposed dual-*k* spacer structures in conventional 6T SRAM cell also mitigate read/write conflict and enhance read/write access time, simultaneously. It is observed that the performance improvement in AsymD-*k* based SRAM cell is due to its S/D asymmetric current that helps in adjusting the pull-up (PR) and cell-ratio (CR) to augment the voltage margins. Contradictorily, the improvements in SymD-*k* cell are attributed to the enhanced electrostatic (or current margins) that increase SNMs without affecting PR and CR. Therefore, to compare both the device architecture on a common platform, the power margins are also considered. The result shows that the SymD-*k* based SRAM cell outperforms the other architectures in terms of overall read/write power margins, read/write access times and standby leakage power.

Furthermore, the last section of this thesis investigated the tolerance of symmetric and asymmetric dual-*k* spacer architectures and its SRAM performance by random statistical and key structural parametric variations. In addition to the superior device electrostatics and better static/dynamic circuit/SRAM performance, it is observed that both the symmetric and asymmetric dual-*k* tri-gate structures also exhibit better device and circuit immunity to random variations and lesser sensitivity to key structural parameters in comparison to the conventional and purely high-*k* FinFET based device/circuits.

7.2 Scope for Future Research

The work carried out during this research demonstrated the optimum usage of high-permittivity spacer materials to enhance the tri-gate FinFET device and digital circuit performance using extensive 3D TCAD simulations. However, following work can be undertaken to further explore the dual-*k* spacer concept:

1. The source/drain series resistance and parasitic fringe capacitance plays crucial role in determining the performance of dual-*k* spacer technology. Therefore, it is important to further investigate the inner and outer fringe components using charge based analytical modelling.

2. It is observed that the performance improvement in dual-*k* spacer technology is primarily due to the change in electric-field path at the high-*k*/low-*k* spacer interface. Therefore, it is suggested to quantitatively study the potential and charge distribution under the spacer interface. Modelling high-*k*/low-*k* spacer interface effects would be of great significance.
3. Recently, the strain engineering has been played a crucial role in device/circuit performances in sub-20 nm technology nodes. High-*k* gate-dielectric and spacer material introduces strain that further modulates the device/circuit performance. Therefore, it would be interesting to analyze the strain effect in dual-*k* based circuit/SRAMs.
4. In addition to high-performance digital circuit/SRAM applications, the dual-*k* spacer concept should be investigated for analog and mixed-mode circuits such as current mirror, differential amplifiers, ADC and DAC *etc.* In TCAD, large mixed-mode circuit simulation is a time consuming process that is further marred by convergence issues. Therefore, either a BSIM or Verilog-A model have to be developed for further investigation of large mixed-mode circuits such as a complete SRAM array with all its peripheral circuitry.
5. Although, the immunity of dual-*k* spacer technology under some random and structural variations such as WFV, RDF and TOX are demonstrated in this thesis. However, FinFET in sub-20 nm nodes suffer from several other variations such as line edge roughness, interface roughness, NBTI and so on. Therefore, it would be imperative to study its effect on dual-*k* architectures.
6. It is important to fabricate the proposed dual-*k* architectures that truly demonstrate its suitability for high-performance device/circuit applications in presence of the actual interface trap charges and other quantum mechanical (QM) effects. Also, it would be very interesting to experimentally analyze the effect of random variations on dual-*k* FinFET.

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2. **Pankaj Kr. Pal**, B. K. Kaushik, and S. Dasgupta, "Investigation of symmetric dual-*k* spacer trigate FinFETs from delay perspective," *IEEE Trans. on Electron Devices*, vol.61, no.11, pp.3579-3585, Nov. 2014. **(*Impact factor: 2.512*)**
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Books:

1. **Pankaj Kr. Pal**, B. K. Kaushik, and S. Dasgupta, "Spacer-engineered FinFET architectures for high-performance digital circuit applications," *CRC Press, Taylor and Francis.* **(*Proposal accepted*)**