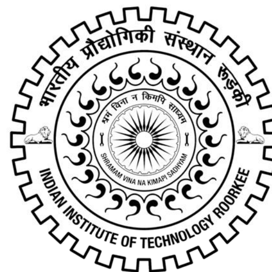
MODELING OF CROSSTALK EFFECTS IN CMOS GATE DRIVEN ON-CHIP INTERCONNECTS USING FDTD TECHNIQUE

Ph.D. THESIS

by

RAMESH KUMAR VOBULAPURAM



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
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MODELING OF CROSSTALK EFFECTS IN CMOS GATE DRIVEN ON-CHIP INTERCONNECTS USING FDTD TECHNIQUE

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Submitted in partial fulfilment of the requirements for the award of the degree

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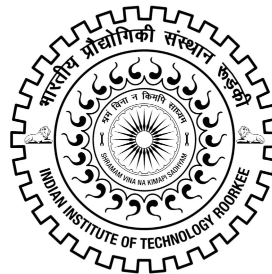
by

RAMESH KUMAR VOBULAPURAM



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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **"MODELING OF CROSSTALK EFFECTS IN CMOS GATE DRIVEN ON-CHIP INTERCONNECTS USING FDTD TECHNIQUE"** in partial fulfillment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electronics and Communication Engineering of the Indian Institute of Technology Roorkee is an authentic record of my own work carried out during a period from December, 2011 to November, 2015 under the supervision of Dr. B. K. Kaushik, Associate Professor and Dr. A. Patnaik, Associate Professor, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee.

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

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This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

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Dated: 2nd March 2016

ABSTRACT

Advancement in very large scale integration (VLSI) technology offers gigascale integrated circuits in a system on-chip. In these circuits, interconnects play a key role in determining circuit performance, such as time delay and power consumption. At high operating frequencies, the closely packed interconnects produce transient crosstalk. The crosstalk noise strongly influences the signal propagation delay and causes the logic or functional failure.

Over the years, several mathematical models have been proposed for the analysis of CMOS gate driven coupled on-chip interconnects. However, most of these crosstalk noise models approximately considered the non-linear CMOS driver as a linear resistor. This approximation is not valid for on-chip interconnects because during the input and output transition states the transistor operates in cutoff, linear and saturation regions. The transistor operating time in the saturation region is about 50% during the transition period. Thus, assuming that the transistor operates in the linear region leads to severe errors in the performance estimation of the driver-interconnect-load system. Therefore, it is necessary to develop an accurate model that appropriately considers the non-linear effects of CMOS driver and accurately measures the crosstalk induced performance parameters of on-chip interconnects.

This thesis presents an accurate and time efficient model of CMOS gate driven coupled on-chip interconnects for crosstalk induced performance analysis. The proposed model successfully incorporates the non-linear effects of CMOS driver. The model is developed using the finite-difference time-domain (FDTD) technique for coupled on-chip interconnects, whereas, the CMOS driver is modeled by either n-th power law or modified alpha power law model. The model is validated by comparing the results with HSPICE simulations. It is observed that the results of the proposed model closely matches with that of HSPICE simulations. Encouragingly, the FDTD model is highly time efficient than the HSPICE.

The conventional copper interconnect suffers from low reliability with down scaling of interconnect dimensions. The reliability of Cu reduces due to the electromigration induced problems such as hillock and void formations. Moreover, with highly scaled dimensions the resistivity of Cu increases due to electron-surface

scattering and grain-boundary scattering. Therefore, researchers are forced to find an alternative material for on-chip interconnects. Carbon nanotubes (CNTs) have been proposed as a promising interconnect material. A portion of this thesis is focused towards the modeling of multi-walled CNT (MWCNT) interconnects. An accurate FDTD model is presented while incorporating the quantum effects of nanowire and non-linear effects of CMOS driver. To reduce the computational effort required for analyzing the CMOS driver, a simplified but accurate model is employed, named as, modified alpha power law model. The crosstalk noise is comprehensively analyzed by examining both functional and dynamic crosstalk effects.

Graphene nanoribbon (GNR), a strip of ultra-thin width graphene layer, has also been considered aggressively by the researchers as a potential alternative material for realizing on-chip interconnects. Most of the physical and electrical properties of GNRs are similar to that of CNTs; however, the major advantage of GNRs over CNTs is that both transistor and interconnect can be fabricated on the same graphene layer, thus avoiding the metal-graphene contact problems. This thesis presents an accurate model for the analysis of multi-layer GNR (MLGNR) interconnects. In a more realistic manner, the model incorporates the width dependent mean free path that helps in accurately estimating the crosstalk induced performance in comparison to the conventional models.

The stability of the FDTD technique is constrained by the Courant-Friedrichs-Lewy (CFL) stability condition. Hence, beyond the CFL condition, the FDTD technique is unstable and within it, the technique is inefficient. The efficiency improvements in FDTD technique can be addressed, if the CFL stability condition is removed. To improve the efficiency of FDTD technique, an unconditionally stable FDTD (US-FDTD) technique is presented for the analysis of on-chip interconnects. It is observed that the stability of the proposed model is not constrained by the CFL condition and is therefore unconditionally stable. The accuracy of the proposed model is validated against the conventional FDTD model. It is observed that the US-FDTD model is highly time efficient while being as accurate as the conventional FDTD. Moreover, a comparative analysis of crosstalk induced performance is presented among Cu, MWCNT and MLGNR interconnects. It is observed that the MLGNR and MWCNT interconnects outperform the Cu interconnect.

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This thesis is dedicated to my parents and my loving family.

Dated: 2nd March 2016 **(V. Ramesh Kumar)**

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LIST OF SYMBOLS

C — Capacitance

C_d — Driver capacitance

C_L — Load capacitance

c_c — Coupling capacitance between the interconnects

c_e — Electrostatic capacitance

c_q — Quantum capacitance

d_1 — Innermost shell diameter of MWCNT

d_i — Diameter of ith shell in MWCNT

d_N — Outermost shell diameter of MWCNT

E_F — Fermi energy level

E_g — Energy gap

E_i — The lowest (or highest) energy level of the ith-conduction (or valence) subband

ê E — Energy gap between the subbands

e — Electron charge

F_m — Metallic to semiconducting ratio

H — Distance between the interconnect and the ground plane

h — Planckøs constant

I_{DSAT} — Drain saturation current

k_B — Boltzmann constant

I_n — NMOS current

I_p — PMOS current

L — Inductance

l_e — Magnetic inductance

l_k — Kinetic inductance

l_m — Mutual inductance between the shells/layers

N — Number of shells/layers in MWCNT/MLGNR

$N_{ch,i}$	Number of conducting channels of ith shell/layer
N_C	Number of carbon atoms across the GNR width
P	Backscattering probability
R	Resistance
R_{eq}	Driver resistance
R_{lump}	Lumped resistance
R_{MC}	Contact resistance
R_Q	Quantum resistance
r_s	Scattering resistance
T	Temperature
t	Interconnect thickness
V_{DD}	Supply voltage
V_{DSAT}	Drain saturation voltage
V_S	Input voltage
v_F	Fermi velocity
w	Interconnect width
τ	Time delay
σ	Drain conductance parameter
δ	Inter-shell/inter-layer distance
λ_{mfp}	Mean free path
λ_d	Mean free path due to defects
λ_n	Mean free path due to edge roughness
λ_{eff}	Effective mean free path
θ	Chirality angle
ε	Permittivity
μ	Permeability
Δt	Time step size
Δz	Space step size

LIST OF ABBREVIATIONS

ac	Armchair
ADI	Alternating Direction Implicit
CFL	Courant-Friedrichs-Lewy
CMOS	Complementary Metal Oxide Semiconductor
CN	Crank-Nicolson
CNT	Carbon Nano Tube
DIL	Driver Interconnect Load
ESC	Equivalent Single Conductor
FDTD	Finite-Difference Time-Domain
FET	Field Effect Transistor
FSV	Feature Selective Validation
GDM	Global Difference Measure
GNR	Graphene Nano Ribbon
HSPICE	Hewlett Simulation Program with Integrated Circuit Emphasis
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
LER	Line Edge Roughness
MFP	Mean Free Path
MLGNR	Multi Layer Graphene Nano Ribbon
MNA	Modified Nodal Analysis
MOS	Metal Oxide Semiconductor
MTL	Multi-conductor Transmission Line
MWCNT	Multi Walled Carbon Nano Tube
p.u.l.	Per Unit Length

RC	Resistance Capacitance
RLC	Resistance Inductance Capacitance
RLCG	Resistance Inductance Capacitance Conductance
SLGNR	Single Layer Graphene Nano Ribbon
SWCNT	Single Walled Carbon Nano Tube
TB	Tight Binding
TEM	Transverse Electro-Magnetic
US-FDTD	Unconditionally Stable FDTD
VLSI	Very Large Scale Integration
zz	Zigzag
1D	One Dimensional
2D	Two Dimensional
3D	Three Dimensional

Chapter 1

Introduction

1.1 Introduction

Advancement of technology in the nanometer regime considers high speed and high density very large scale integration (VLSI) circuits. It is desirable to use multilayer interconnections in three or more levels to achieve higher packing densities and smaller footprint [1, 2]. Based on the length and cross-sectional dimensions, the on-chip interconnects can be broadly characterized into three categories: local, intermediate and global interconnects. Local interconnects consist of very thin lines, used to connect gates and transistors in a functional block. Intermediate interconnects are wider and longer than local interconnects, provide low resistance signal paths in a functional block. The global interconnects provide long distance communication between the functional blocks and have a large cross-sectional area to minimize the resistance [3]. The global interconnects are placed at the higher level of the chip and can be as long as 1-2 cm in current high-performance integrated circuits [1].

In early days, the operating speed of an integrated circuit was limited by the speed of a logic gate. Interconnects between the gates were considered as ideal conductors, where the signal propagates instantaneously. Therefore, the interconnects had little effect on circuit operation. However, after the introduction of submicron semiconductor devices, the ideal behavior of interconnects no longer remains adequate. In fact, the performance of the chip is primarily determined by the interconnect line rather than the device [4].

At high operating frequencies, the closely packed interconnects produce transient crosstalk [5-7]. The undesired effect created on one line due to a signal transmitted on another line is defined as crosstalk. The crosstalk noise strongly influences the signal propagation delay and causes the circuit malfunction or functional failure. Based on the switching transitions in the coupled lines, crosstalk can be broadly classified into functional and dynamic crosstalks. When the victim line is quiescent, a voltage spike appearing on it due to switching in an adjacent line is

referred as the functional crosstalk. Dynamic crosstalk appears when the adjacent lines are simultaneously switching either in-phase or out-phase. A change in logic value and propagation delay can be experienced under functional and dynamic crosstalks, respectively. Moreover, the crosstalk noise causes signal overshoot, undershoot and ringing effects. Therefore, accurate estimation of performance parameters, under the effect of crosstalk, gained importance for the design of high performance on-chip interconnects.

1.2 Evolution of Interconnect Materials

Aluminium had been used for a long time to form interconnect lines because of its compatibility with silicon. However, as device dimensions scale down the reliability decreases due to increasing current density that may lead to electromigration induced problems [2]. In 1997, IBM announced plans to replace aluminium with copper, a metal with lower resistivity than aluminum [2]. Copper provides high current density (10^7 A/cm^2) leading to the electromigration effect being less significant [8]. Later on, it was realized that even Cu was not able to fulŁll the demands of high-speed interconnects due to the following reasons:

i) The reliability decreases with down scaling of interconnect dimensions due to increase in current density.

ii) The resistivity increases at lower dimensions, due to grain-boundary scattering and surface scattering.

iii) The resistivity increases rapidly due to Joule heating.

iv) The conductivity reduces at high operating frequencies, due to the skin effect.

Therefore, the copper interconnect material is unable to meet the requirements of future technology needs. The widening gap between the requirements of future on-chip interconnect material and the presently used copper material has compelled researchers and designers to look out for novel material solutions. Graphene based nano interconnects have been proposed as a promising solution for the future on-chip interconnects [9-15]. Encouragingly, graphene nano interconnects demonstrate longer mean free paths in the order of several micrometers, higher current densities in excess of 10^9 A/cm^2, and higher thermal stability than copper. These properties create lots of

interest among researchers to use these materials as VLSI interconnects [16, 17]. Graphene nano interconnects can be classified into carbon nanotubes (CNTs) and graphene nanoribbons (GNRs).

1.2.1 Carbon Nanotubes (CNTs)

Carbon nanotubes are single layer of graphene sheets rolled up into cylinders with diameters ranging from 1 nm to 5 nm. The electron transport in metallic CNTs is ballistic that results in movement of electrons without scattering along the nanotube axis and enables a long mean free path in the range of micrometers [18-22]. Contrastingly, the mean free path of electrons in Cu is limited to a few nanometers. Due to the large mean free path and small diameter, the electrons do not scatter as often in CNTs that results in low resistance. This low resistance ensures that the energy dissipated in CNTs is incredibly small. Thus, the problem of dissipated power density can be properly addressed. Moreover, the 1D structure of CNT offers many electrical properties, such as

i) High quality CNTs have long mean free path (MFP) ranging from 1-5 μm that results in ballistic transport phenomenon.

ii) The strong sigma bonds are useful for high mechanical strength and pi bonds are useful for high conductivity.

iii) Higher electron mobility (~ 10^5 $cm^2/(V\cdot s)$) in comparison to Cu (~ 10^3 $cm^2/(V\cdot s)$) that results in high drift velocity.

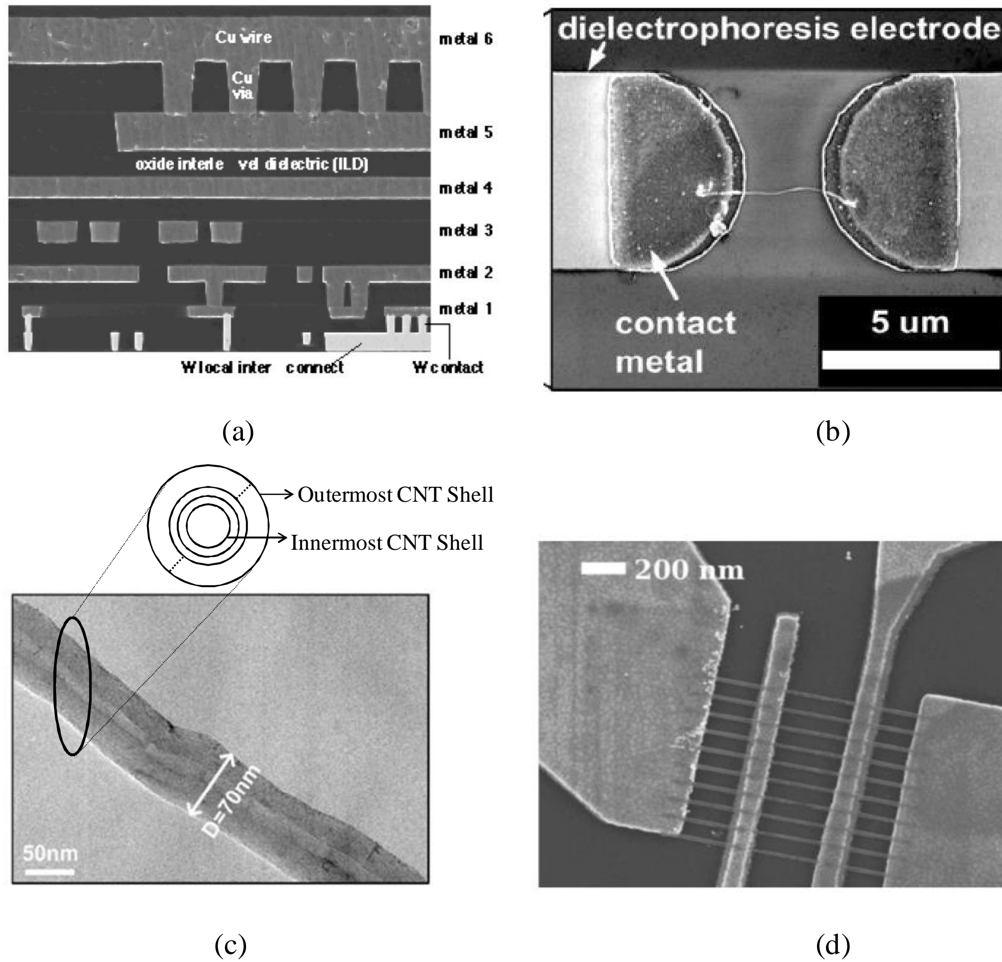
iv) Larger current densities (10^9 A/cm^2) in comparison to Cu (10^7 A/cm^2) that results in lower electromigration effect.

Depending on the number of concentrically rolled up graphene sheets, CNTs are categorized as single-walled CNTs (SWCNTs) and multi-walled CNTs (MWCNTs) [23, 24]. SWCNT is a single-layer sheet of graphite rolled up into a cylinder. The primary drawback of SWCNT bundle is the non-controllability of its chirality. The metallic and semiconducting properties of CNTs are primarily dependent on their chirality. Statistically, one-third of the CNTs in a bundle are considered to be conducting (*i.e.*, metallic) while the remaining behaves as semi-conductors. Morris [25] observed that the SWCNTs with random chiralities do not show any advantage over the conventional interconnect materials. This problem can

be rectified by using MWCNTs that consist of multiple layers of graphene sheets arranged in co-axial configuration with the diameters ranging from 2 nm to several tens of nanometers. Due to the large diameters, the MWCNT shells are conductive even if they are of semiconducting chirality because the energy gap is inversely proportional to the shell diameter. For a semiconducting CNT having a diameter greater than 20 nm, the gap between the conduction band and the Fermi level is observed to be smaller than 0.0258 eV, which can be smeared by the environmental temperature [26].

1.2.2 Graphene Nanoribbons (GNRs)

Graphene nanoribbon, a strip of ultra-thin width graphene layer, has also been considered aggressively by the researchers as a potential alternative material for realizing on-chip interconnects [27, 28]. Most of the physical and electrical properties of GNRs are similar to that of CNTs, however, the major advantage of GNRs over CNTs is that both transistors and interconnects can be fabricated on the same graphene layer [29]. Therefore, one of the manufacturing difficulties regarding the formation of metal-nanotube contact can be avoided. Depending on the number of stacked graphene sheets, GNRs are classified as single-layer GNRs (SLGNRs) and multi-layer GNRs (MLGNRs). Due to the lower resistivity and easy fabrication process, the MLGNRs are often preferred over SLGNRs as interconnect material. However, the MLGNRs fabricated till date have displayed some level of edge roughness [30, 31]. The electron scattering at the rough edges, reduces the mean free path (MFP) that substantially lowers the conductance of the MLGNRs. This fundamental challenge limits the performance of MLGNR interconnects. The SEM images of Cu, MWCNT and MLGNR interconnects are shown in Figure 1.1. Figure 1.1 (a) shows the Cu interconnect structure with different interconnect levels. The MWCNT structure with 80-CNT shells is shown in Figure 1.1 (b) and the close-up view is shown in Figure 1.1 (c). The MLGNR interconnect structure with 10-GNR layers is shown in Figure 1.1 (d).



(a) (b)

(c) (d)

Figure 1.1. (a) Cross-sectional view of Cu interconnect architecture with 6 levels [6], (b) fabricated structure of an MWCNT between two metal contacts, (c) close-up view of MWCNT, consisting of 80 shells [19] and (d) fabricated structure of MLGNR, consists of 10 layers [27].

1.3 Modeling of On-chip Interconnects

Historically, interconnects were modeled as a lumped capacitor [1]. With the advancement of technology, the cross-sectional area of interconnects were scaled down, due to which the line resistance became significant and therefore, the interconnect line was represented as lumped resistance-capacitance (RC) [32]. However, later these interconnect parasitic elements were not treated as lumped elements. To improve the accuracy, a distributed RC model was considered [33]. Currently, the parasitic inductance has started to play an important role in an on-chip interconnect performance due to the adoption of low resistive interconnect materials, and high operating switching frequencies. Therefore, the on-chip interconnects must

be treated as distributed *RLC* lines or as transmission lines to estimate the performance accurately [34]. Agarwal *et al.* [4] proposed a model considering the transmission line effects of coupled on-chip interconnects driven by a linear resistor. Kaushik *et al.* extended this model to a non-linear complementary metal-oxide semiconductor (CMOS) driver using alpha-power law model and analyzed functional crosstalk effects in [35] and dynamic crosstalk effects in [36]. The models reported in [4], [35] and [36] are based on even-odd modes and hence limited to purely two coupled interconnect lines. Furthermore, the transient analysis was carried out for lossless lines, which is impractical.

The modeling of distributed *RLC* lines along with non-linear CMOS driver suffers from frequency/time domain conversion problem. This problem arises because the transmission lines were traditionally solved in the frequency domain by using the partial differential equations, whereas the CMOS driver is modeled in the time domain. Therefore, to avoid this conversion problem, most of the researchers [4, 5], [37] replace the non-linear CMOS driver by the linear resistive driver that severely affects the accuracy of the model. In the present research work, to avoid the conversion problem, finite-difference time-domain (FDTD) technique is used to solve the transmission line equations in the time domain. Using the FDTD method, the voltage and current values can be correctly estimated at any particular point on the interconnect line. Moreover, the FDTD model can be extended to *n* coupled interconnect lines with low computational cost.

In past, FDTD techniques were used to analyze the transmission lines, which are excited and terminated by resistive driver and resistive load, respectively [38-40]. Including the frequency dependent losses, Orlandi *et al.* [41] proposed the FDTD model for the analysis of multiconductor transmission lines terminated in arbitrary loads using the state-variable formulation. However, the models proposed in [38-40] analyses the transmission lines with resistive drivers and hence not valid for the accurate study of on-chip interconnects performance, which are actually excited and terminated by the CMOS inverters. Based on the FDTD technique, Li *et al.* [42] proposed a model for the transient analysis of CMOS gate-driven distributed *RLC* interconnects. Coupled interconnects were analyzed at global interconnect length using 180 nm technology node where the non-linear CMOS drivers were modeled by

the alpha power law model. This model is not accurate under the conditions when the technology is scaled down beyond 180 nm, due to the ignorance of the finite drain conductance parameter. Therefore, it is necessary to develop an accurate model that appropriately considers the non-linear effects of CMOS drivers and accurately measures the crosstalk induced performance parameters of on-chip interconnects. This thesis presents an accurate and time efficient model of CMOS gate driven coupled interconnects for crosstalk induced performance analysis. The model is developed using the FDTD technique for coupled on-chip interconnects, whereas the CMOS driver is modeled by either n-th power law or modified alpha power law model by considering the finite drain conductance parameter. The model is validated by comparing the results with HSPICE simulations.

1.4 Problem Definition

Over the years, several mathematical models have been proposed for the analysis of CMOS gate driven coupled interconnect lines [4-7], [21], [37]. However, most of these crosstalk noise models consider the non-linear CMOS driver as a linear resistor. In actual practice, this approximation is not valid, since during the signal transition states the MOSFET operates in cutoff, linear and saturation regions. The MOSFET operating time in the saturation region is about 50% during the transition period. Thus, assumption of the non-linear transistor as a linear resistor leads to severe errors in the performance estimation of on-chip interconnects. The aim of this research work is to incorporate the non-linear effects of CMOS driver in the modeling of different on-chip interconnects. The time/frequency domain conversion problem is addressed by analyzing the interconnect lines in time domain using the FDTD technique. The entire work is divided into four parts:

i) FDTD modeling of CMOS gate driven Cu interconnects for comprehensive crosstalk analysis, including functional and dynamic crosstalk effects.

ii) Development of a numerical model for the crosstalk induced performance analysis of MWCNT interconnects by incorporating the quantum effects of a nanowire.

iii) Accurate crosstalk noise modeling of MLGNR interconnects by including the width dependent MFP.

iv) Development of a novel unconditionally stable FDTD model to increase the efficiency of the conventional FDTD model.

1.5 Outline of the Work

The thesis consists of seven chapters. A brief discussion of each chapter is presented below:

Chapter 1 introduces the challenges associated with the modeling of on-chip interconnects. This chapter also introduces the evolution of graphene interconnect materials and the challenges associated with them. The motivation for taking the specific problem for the purpose of the present research work is demonstrated. Furthermore, it presents the outline of the complete thesis work.

Chapter 2 reviews the Cu based on-chip interconnect modeling. The structures, properties and characteristics of graphene based on-chip interconnects are discussed. Depending on the physical configuration, equivalent electrical models of MWCNT and MLGNR interconnect lines are also introduced. An extensive review on performance analysis of on-chip interconnects is presented. This chapter brings forward various technical gaps based on vast literature review.

Chapter 3 deals with the modeling of Cu based on-chip interconnects. The model considers the non-linear effects of CMOS driver as well as the transmission line effects of interconnect line. The CMOS driver is represented by the n-th power law model and the coupled-multiple interconnect lines are modeled by the FDTD technique. The model is validated by the industry standard HSPICE simulator. It is observed that the results of the proposed model closely matches with that of HSPICE simulations. Encouragingly, the proposed model is highly time efficient than the HSPICE.

Chapter 4 introduces an equivalent single conductor (ESC) model of MWCNT interconnects. Based on the ESC model, this chapter presents an accurate FDTD model of MWCNT while incorporating the quantum effects of nanowire and non-linear effects of CMOS driver. To reduce the computational effort required for analyzing the CMOS driver, a simplified but accurate model is employed named as modified alpha power law model.

Chapter 5 analyzes the performance of coupled MLGNR interconnects using the FDTD technique. In a more realistic manner, the proposed model incorporates the width dependent MFP parameter of the MLGNR while taking into account the edge roughness. This helps in accurate estimation of the crosstalk induced performance in comparison to the conventional models. The crosstalk noise is comprehensively analyzed by examining both functional and dynamic crosstalk effects.

Chapter 6 introduces a novel unconditionally stable FDTD (US-FDTD) model for the performance analysis of on-chip interconnects. It is observed that the stability of the proposed US-FDTD model is not constrained by the CFL condition and is therefore unconditionally stable. The accuracy of the proposed model is validated against the conventional FDTD model. It is observed that the US-FDTD model is as accurate as the conventional FDTD model while being highly time efficient. Moreover, the performance of Cu interconnect is compared with MWCNT and MLGNR interconnects under the influence of crosstalk.

Chapter 7 concludes the thesis. Conclusions are made based on the obtained results. The future scope of the work is also presented in this chapter.

The thesis ends with a complete list of references along with the list of publications based on the research work carried out.

Chapter 2

Review of Cu, MWCNT and MLGNR Interconnect Models

2.1 Interconnect Modeling Approaches

In the early days of VLSI design, the crosstalk induced signal integrity effects were negligible because of relatively low integration density and slow operating speed. However, with the introduction of technology scaling of below 0.25   m, there were many significant changes in the structure and electrical characteristics [43, 44]. The interconnect lines started to be a dominating factor for chip performance and robustness. The line parasitic elements have a major impact on the electrical behavior of the interconnect model. These models vary from simple to very complex depending upon the effects that are being studied and the required accuracy. There are three different types of approaches available in literature for modeling Cu based on-chip interconnects.

2.1.1 Lumped Model with CMOS Driver

This approach focuses on the CMOS gate modeling while the interconnect line is approximately considered as a lumped circuit. Alpha-power law model [45] has been widely used for representation of short-channel transistor that includes the velocity saturation effects. Based on the alpha-power law model, delay formulas were developed for CMOS gate driven lumped capacitance modeled interconnect line [46, 47]. Bisdounis *et al.* [48] extended the model to include the influences of short-circuit current and gate-to-drain coupling capacitance. With the resistive component of interconnect becoming comparable to the gate output impedance, the line resistance R of interconnect line needs to be considered. Considering the line resistance, the modeling of CMOS gate driven resistor-capacitor (RC) line was presented in [49-51]. The representation of CMOS gate driven lumped RC load is shown in Figure 2.1. Alder and Friedman [52] derived the delay equations for repeater insertion of a CMOS buffer design with RC interconnects. They developed a closed form expression for the timing analysis of CMOS gate driven RC load. They also derived an expression for the short-circuit power dissipation of the driver-interconnect-load system. However, all these approaches [45-52], lumped the total wire resistance of

each segment into one single R and similarly combined the global capacitance into a single capacitor C. This lumped RC model is inaccurate for long interconnect wires, which are more adequately represented by a distributed RC model. Moreover, due to high operating frequencies and wider interconnect dimensions, interconnects exhibit inductance effects and should be included in the delay and crosstalk noise models. Hence, the analytical models that considered only RC were no longer accurate [45-52].

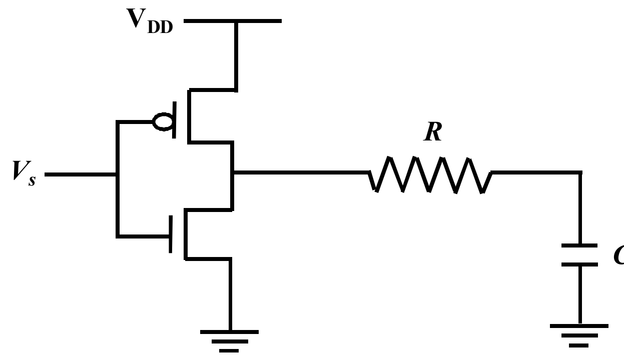


Figure 2.1. A CMOS gate driven *RC* load.

2.1.2 Distributed Model with Resistive Driver

In the distributed model with resistive driver, the driver-interconnect-load system is analyzed by simplifying the CMOS gate driver as a resistive driver [53]. Using the linear driver approximation, Elmore delay model was initially developed for RC lines [54] and then extended to RLC lines [55, 56]. The distributed RLC line with linear driver is shown in Figure 2.2, where R_d and C_L represent driver resistance and load capacitance, respectively; r, l and c represent per-unit-length line resistance, inductance and capacitance, respectively. Considering the nonlinearity of the driver, Bai *et al.* [57] improved the linear driver model by calculating the effective resistance. Davis and Meindl proposed closed-form delay expressions for the analysis of distributed RLC lines by considering the single transmission line effects in [58] and a crosstalk noise model of coupled transmission lines in [59].

Based on even-odd mode technique, the crosstalk noise model was developed by Agarwal *et al.* [4] for coupled-two lossless lines and then modified for low-loss lines to analyze crosstalk induced noise peak voltage. They investigated that at high operating frequencies, inductive coupling effects are significant and should be

included for accurate crosstalk-noise analysis. Using the coupled transmission line theory, the authors developed a crosstalk noise model that is useful to guide noise-aware physical design optimizations. A closed form analytical transient response model was derived for resistance/capacitance loads by solving semi-finite transmission line equations [60]. However, all these models [4], [53-60] consider the non-linear CMOS driver as a linear driver that limits the accuracy of the models.

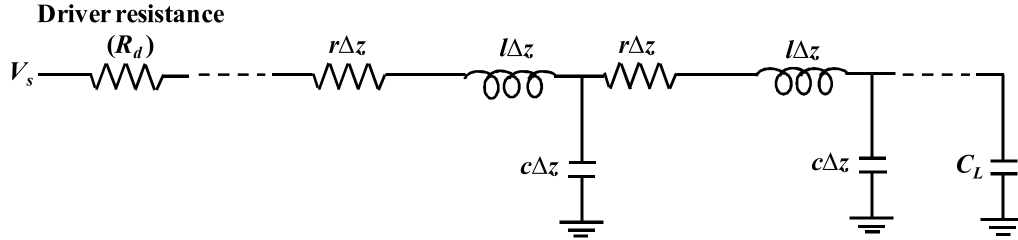


Figure 2.2. A distributed *RLC* interconnect line driven by a resistive driver.

2.1.3 Distributed Model with CMOS Driver

The distributed model with CMOS driver approach co-simulates the nonlinear CMOS gate and the distributed interconnect. The CMOS gate driven distributed *RLC* interconnect line is shown in Figure 2.3. Based on the even-odd modes, Kaushik *et al.* proposed a simple analytical model for functional crosstalk analysis in [61] and dynamic crosstalk analysis in [36] of CMOS gate-driven two coupled interconnect lines. The model was developed based on the alpha power law model of MOS transistors and transmission line theory of interconnects. There the authors have observed that the non-linear effects of the CMOS inverter should be incorporated in a valid crosstalk noise modeling. Moreover, it was noticed that the use of resistive driver model presented a pessimistic view on the performance analysis of on-chip interconnects. However, these models [36], [61] were based on the even-odd modes and hence limited to two coupled interconnect lines. Later on, Li *et al.* [42] proposed an FDTD method for the transient analysis of CMOS-gate driven lossy transmission lines including frequency dependent losses and observed the effect of functional crosstalk. However, the model ignored the finite drain conductance parameter in the modeling of CMOS driver and hence not useful for nano-scaled devices.

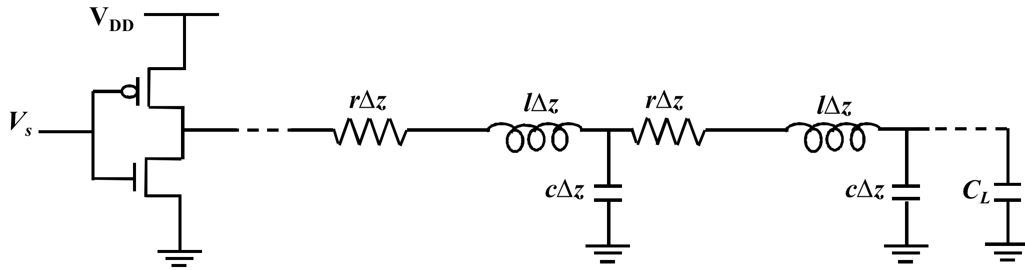


Figure 2.3. A CMOS gate driven distributed *RLC* interconnect line.

2.2 Carbon Nanotubes

Until mid-1980øs, diamond and graphite were the only two known forms of carbon allotropes. In 1985, Kroto *et al.* [62] were able to synthesize new allotrope of carbon, C_{60}. They used a high pulse of laser light to vaporize a sample of graphite. The vaporized graphite was sent to a mass spectrometer with the help of helium gas. The mass spectrometer detected the presence of $C_{60,}$ a molecule consisting of 60 carbon atoms. The C_{60} had the shape of a soccer ball with 12 pentagon faces and 20 hexagonal faces. The easy synthesis of C_{60} led the group to propose the existence of another allotrope of carbon named as õbuckyballö due to its soccer ball shaped structure. The shape of the new allotrope of carbon did not end at the soccer shaped structures and long cylindrical tube like structures were also reported, which are known as carbon nanotubes (CNTs).

CNTs have fascinated the research world due to their extraordinary physical, electrical and chemical properties. Many of the properties defy the conventional trends and scientists are still discovering the unique properties and constantly making efforts to understand and explain the phenomenon for such distinctive behavior. One of the remarkable physical properties of CNT is its ability to scale down its thickness to a single atomic layer. Another interesting physical property observed in CNTs is when two slightly different structured CNTs are joined together; the resultant junction formed can be used as an electronic device. The properties of the device formed are dependent on the type of CNTs used for their formation.

2.2.1 Basic Structure of CNTs

A single-walled carbon nanotube can be assumed as a structure formed when a single graphene sheet is rolled into a cylindrical shape (Figure 2.4). Depending on the shape of the circumference, CNTs can be classified as armchair (ac), zigzag (zz) or chiral CNTs as shown in Figures 2.4 (a), (b), and (c), respectively. The terms zigzag and armchair are inspired from the pattern in which the carbon atoms are arranged at the edge of the nanotube cross-section. Graphene consists of sp^2-hybridized atoms of carbon that are arranged in a hexagonal pattern. The hexagonal carbon rings should join coherently when placed in contact to adjacent carbon atoms. Accordingly, in an SWCNT tube, all the carbon atoms (except at the edges) form hexagonal rings and are therefore equally spaced from one another. Xu *et al.* [63] reported the fabrication of vertically grown CNT bundles with an average diameter of 50 m and a pitch of 110 m.

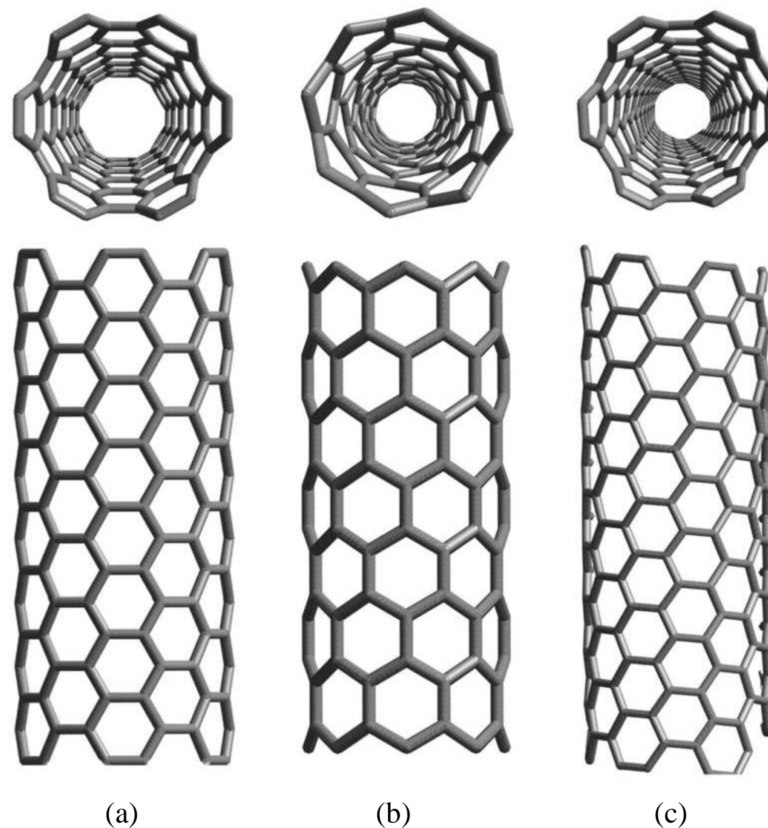


Figure 2.4. Sketches of three different SWCNT structures (a) armchair nanotube, (b) zigzag nanotube and (c) chiral nanotube [64].

In spite of the hexagonal aromatic rings, SWCNT is considered to be more reactive than planar graphene. It is due to the fact that the hybridization in SWCNTs is not purely sp^2 and some degree of sp^3 hybridization is also present. It has been observed that with the decrease in SWCNT diameter, the degree of sp^3 hybridization increases [65]. This phenomenon causes variable overlapping of energy bands that results in SWCNTs obtaining versatile and unique electrical properties. It was studied that beyond the diameter of é 2.5 nm, the SWCNT tube collapses into a two-layer ribbon [65]. Moreover, a CNT with smaller diameter results in higher stress on the structure, although SWCNTs of é 0.4 nm diameter have been produced [66]. It is therefore natural to consider that a diameter of é 1 nm is the most suitable value with regards to energy consideration of SWCNTs. Encouragingly, there are no such restrictions on the length of the SWCNTs. The length is dependent on the processes and methods used for synthesis of the SWCNTs. SWCNTs of length ranging from micrometers to millimeters can be commonly observed. Considering the diameter and length of an SWCNT, it is easy to intuitively conclude that SWCNT structures have exceptionally high aspect ratios.

A graphene sheet can be rolled in a number of different ways (see Figure 2.4). The mathematical expression that can be used to represent the various ways of rolling graphene into the tubes is shown below [10]:

$$PX = \boldsymbol{C}_{\mathrm{h}} = p\boldsymbol{b}_1 + q\boldsymbol{b}_2 \qquad (2.1)$$

where $\boldsymbol{C}_{\mathrm{h}}$ is chirality vector, p and q are integers. The unit vectors $\boldsymbol{b}_1$ and $\boldsymbol{b}_2$ are defined as

$$\boldsymbol{b}_1 = \frac{b\sqrt{3}}{2}\boldsymbol{x} + \frac{b}{2}\boldsymbol{y} \text{ and } \boldsymbol{b}_2 = \frac{b\sqrt{3}}{2}\boldsymbol{x} - \frac{b}{2}\boldsymbol{y} \qquad (2.2)$$

where $b = 2.46$ Å and $\cos\theta = \frac{2p+q}{2\sqrt{p^2+q^2+pq}}$

The vector PX is normal to the CNT tube axis and θ is chirality angle. The diameter, d of a nanotube is dependent on $\boldsymbol{C}_{\mathrm{h}}$ by the following relation

$$d = \frac{|C_h|}{\pi} = \frac{b_{C-C}\sqrt{3\left(p^2+q^2+pq\right)}}{\pi} \qquad (2.3)$$

where $1.41\text{Å}\left(graphene\right) \le b_{C-C} \le 1.44\text{Å}\left(C_{60}\right)$

The C-C bond length in the hexagonal ring structure of SWCNT slightly increases from the C-C bond length in graphene due to the curved structure of SWCNT. The degree of curvature in an SWCNT cannot exceed the degree of curvature in C_{60} molecule, resulting in the upper limit of C-C bond length in SWCNTs. Similarly, the degree of curvature in an SWCNT cannot be less than the curvature in a flat graphene structure, resulting in lower limit of C-C bond length in SWCNTs. Moreover, it can be observed that $\boldsymbol{C}_h$, θ and d can be expressed in terms of p and q. Since SWCNTs can be identified by $\boldsymbol{C}_h$, θ and d values, it is sufficient to define SWCNTs through p, q values by denoting them as (p, q). The p and q values for a particular SWCNT can be easily obtained by counting the number of hexagonal rings separating the margins of $\boldsymbol{C}_h$ vector following $\boldsymbol{b}_1$ first and then $\boldsymbol{b}_2$ [67]. Based on the (p, q) representation, zz SWCNTs can be denoted as (p, 0) and having $\theta = 0^0$; ac SWCNTs can be denoted as (p, p) and having $\theta = 30^0$; chiral SWCNTs can be denoted as (p, q) and having $0 < \theta < 30^0$.

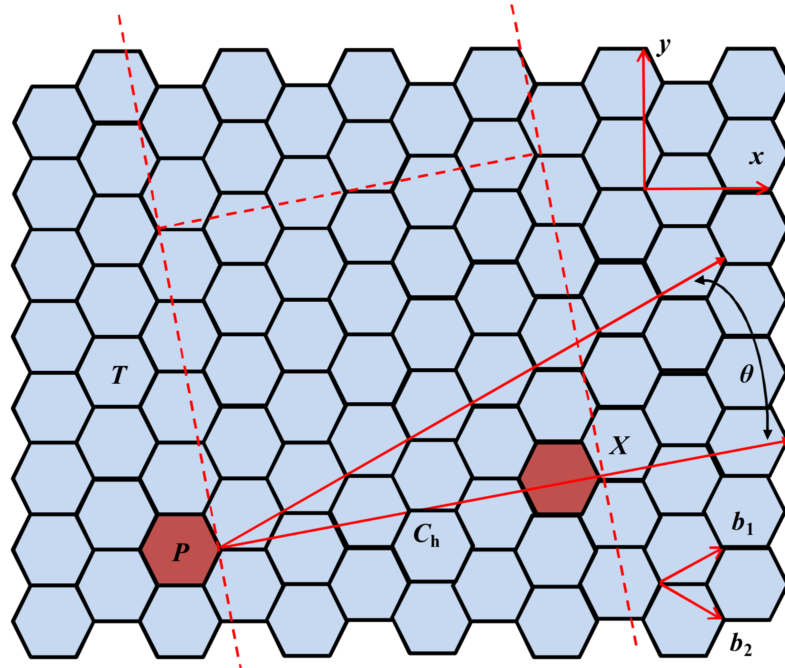


Figure 2.5. Sketch representing the procedure to obtain an CNT, starting from a graphene sheet.

From Figure 2.5, it can be observed that having $\boldsymbol{C}_h$ direction perpendicular to any carbon bond directions results in zz SWCNT ($\theta = 0^0$), while having $\boldsymbol{C}_h$ direction parallel to any carbon bond directions will result in ac SWCNT ($\theta = 30^0$). In chiral SWCNTs, $0 < \theta < 30^0$ due to hexagonal rings in graphene sheet.

An MWCNT is a bit more intricate in structure compared to an SWCNT. Unlike a single graphene shell in an SWCNT, there are multiple graphene shells in an MWCNT. The MWCNTs have two or more numbers of CNT shells that are concentrically rolled up. The structure of MWCNT between the two contacts is shown in Figure 2.6, wherein the inset figure shows its cross-sectional view. The inter-shells are separated by the van der Waals gap, $\delta \sim 0.34$ nm. The diameter of outermost CNT shell can be varied from a few nanometers to several tens of nanometers. The diameter of outermost and innermost shells are denoted by d_N and d_1. The ratio of d_1/d_N varies in different MWCNTs, the values between 0.3-0.8 have been observed in [68-70]. The density of $10^6/\text{cm}^2$ has been obtained in [68] with a d_1/d_N of 0.5. The current carrying capabilities of MWCNTs are similar to the SWCNT bundles, however, the MWCNTs are easier to fabricate [71]. Close *et al.* [19] reported the fabrication of MWCNTs with 80 shells based on a versatile method that is ideally suited for fabricating MWCNT interconnects with extensive electrical properties.

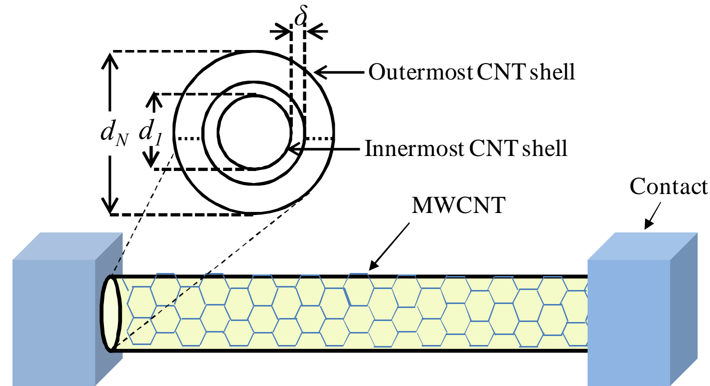


Figure 2.6. The structure of MWCNT placed between the two contacts.

2.2.2 Semiconducting and Metallic CNTs

CNTs can act as semiconducting or metallic based on the pattern of CNT circumference. The armchair CNTs always act as metallic, whereas the zigzag CNTs act as either metallic or semiconducting depending on the chiral indices. This section presents the behavior of zz CNTs and their dual nature.

Since CNT is a rolled-up sheet of graphene, an appropriate boundary condition is required to explore the band structure. If CNT can be considered as an infinitely long cylinder, there are two wave vectors associated with it: 1) the wave vector parallel to CNT axis, $k_{\|}$, that is continuous in nature due to the infinitely long length

of CNTs and 2) the perpendicular wave vector, $k_\perp$, that is along the circumference of the CNT. These two wave vectors must satisfy a periodic boundary condition [10]

$$k_\perp . C_\mathrm{h} = \pi d k_\perp = 2\pi m \quad (2.4a)$$

where m is an integer. The quantized values of allowed $k_\perp$ for CNTs are obtained from the boundary condition. The cross-sectional cutting of the energy dispersion with the allowed $k_\perp$ states results in the 1D band structure of graphene as shown in Figure 2.7 (a). This is called zone folding scheme of obtaining the band structure of CNTs. Each cross-sectional cutting gives rise to 1D sub-band. The spacing between allowed $k_\perp$ states and their angles with respect to the surface Brillouin zone determine the 1D band structures of CNTs. The band structure near the Fermi level is determined by allowed $k_\perp$ states that are close to the K points. When the allowed $k_\perp$ states pass directly through the K points as shown in Figure 2.7 (c), the energy dispersion has two linear bands crossing at the Fermi level without a bandgap. However, if the allowed $k_\perp$ states miss the K points as shown in Figure 2.7 (b), there would be two parabolic 1D bands with an energy bandgap. Therefore, two different kinds of CNTs can be expected depending on the wrapping indices, firstly, the semiconducting CNTs with bandgap as in Figure 2.7 (b) and secondly, the metallic CNTs without bandgap as in Figure 2.7 (c) [10].

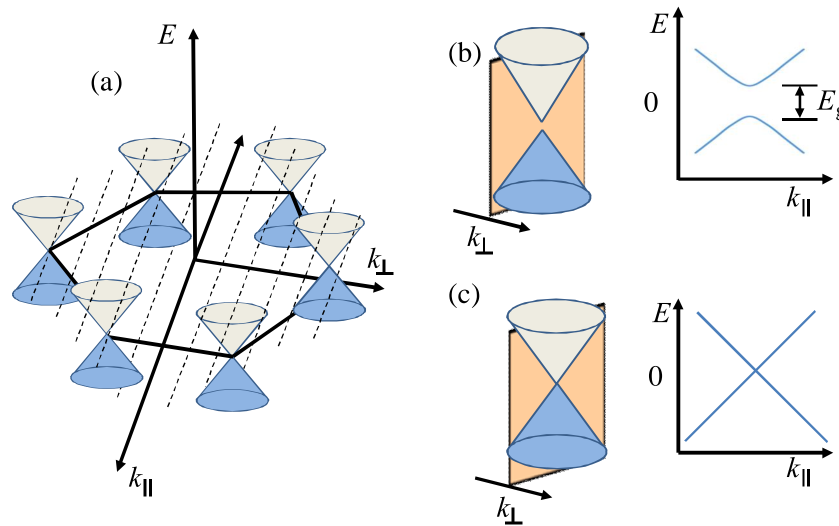


Figure 2.7. Band structures of CNT shell (a) first Brillouin zone of graphene with conic energy dispersions at six K points. The allowed $k_\perp$ states in CNT are presented by dashed lines. The band structure of the CNT is obtained by the cross-sections as indicated. Close view of the energy dispersion near one of the K points are schematically shown along with the cross-sections by allowed $k_\perp$ states and resulting 1D energy dispersions for (b) a semiconducting CNT and (c) a metallic CNT.

Using the approach of 1D sub-bands discussed in previous sub-section, the 1D sub-band closest to the K points for zigzag CNTs is investigated here. Based on the chiral indices, the zigzag CNTs can show metallic/semiconducting property. Since the circumference is $\bar{p}b$ ($C_h = \bar{p}b_1$), the boundary condition in Eq. (2.4a) becomes

$$k_x \bar{p} b = 2\pi m \tag{2.4b}$$

There is an allowed k_x that coincides with K point at (0, 4 /3b). This condition arises when $\bar{p}$ has a value in multiple of 3 ($\bar{p} = 3\bar{q}$, where $\bar{q}$ is an integer), Therefore, by substitution in Eq. (2.4b) [10]

$$k_x = \frac{2\pi m}{\bar{p}b} = \frac{3Km}{2\bar{p}} = \frac{Km}{2\bar{q}} \tag{2.5}$$

There is always an integer m (= $2\bar{q}$) that makes k_x pass through K points and these types of CNTs (with $\bar{p} = 3\bar{q}$) are always metallic without bandgap as shown in Figure 2.7 (c). There are two cases when p is not a multiple of 3. If $\bar{p} = 3\bar{q}+1$, the k_x is closest to the K point at $m = 2\bar{q}+1$ (as in Figure 2.7 (b)).

$$k_x = \frac{2\pi m}{\bar{p}b} = \frac{3Km}{2\bar{p}} = \frac{3K(2\bar{q}-1)}{2(3\bar{q}+1)} = K + \frac{K}{2}\frac{1}{3q+1} \tag{2.6}$$

Similarly, for $\bar{p} = 3\bar{q}$ ó1, the allowed k_x closest to K is when $m = 2\bar{q}$ ó1, hence

$$k_x = \frac{2\pi m}{\bar{p}b} = \frac{3Km}{2\bar{p}} = \frac{3K(2\bar{q}-1)}{2(3\bar{q}-1)} = K - \frac{K}{2}\frac{1}{3\bar{q}-1} \tag{2.7}$$

In these two cases, allowed k_x misses the K point by

$$\Delta k_x = \frac{K}{2}\frac{1}{3\bar{q}\pm 1} = \frac{2}{3}\frac{\pi}{\bar{p}b} = \frac{2}{3}\frac{\pi}{\pi d} = \frac{2}{3d} \tag{2.8}$$

From Eq. (2.8), it is inferred that the smallest misalignment between an allowed k_x and a K point is inversely proportional to the diameter. Thus, from the slope of a cone near K points (Eq. (2.4a)), the bandgap E_g can be expressed as

$$E_g = 2\times\left(\frac{\partial E}{\partial k}\right)\times\frac{2}{3d} = 2\hbar v_F\left(\frac{2}{3d}\right) \approx 0.7\text{eV}/d\ (\text{nm}) \tag{2.9}$$

Therefore, semiconducting CNTs (d = 0.8ó3 nm) exhibit bandgap ranging from 0.9ó 0.2 eV. Depending on the value of $\bar{p}$, where $\bar{p}$ is the remainder when p and q is divided by 3, SWCNTs (represented by (p, q)) can be of three types:

$\overline{p} = 0$; metallic with linear sub-bands crossing at the K points.

$\overline{p} = 1, 2$; semiconducting with a bandgap, $E_g \sim 0.7\text{eV}/d$ (nm).

Similar treatment can also be applied for armchair CNTs ($\overline{p}, \overline{p}$), arriving at the conclusion that they are always metallic.

2.2.3 Properties and Characteristics of CNTs

The atomic arrangements of carbon atoms are responsible for the unique electrical, thermal and mechanical properties of CNTs [72, 73]. The sp^2 bonding delivers the high conductivity and mechanical strengths to the CNTs. The unique properties of CNTs are discussed below:

2.2.3.1 Strength and Elasticity

Due to the sp^2-hybridization, each carbon atom in a single sheet of graphite is connected via strong sigma bonds to three neighboring atoms. Thus, CNTs exhibit the strongest basal plane elastic modulus and hence are expected to be the ultimate high-strength fiber. The elastic modulus of CNT is much higher than steel that makes the CNT as a strongest material. Although forcing on the tip of nanotube will cause it to bend, the nanotube returns to its original state as soon as the force is removed. This property makes CNTs extremely useful as probe tips for high-resolution scanning probe microscopy. Although, the current Youngøs modulus of SWCNT is about 1 TPa, but a much higher value of 1.8 TPa has also been reported [74]. For different experimental measurement techniques, the values of Youngøs modulus vary in the range of 1.22 TPa to 1.26 TPa depending on the size and chirality of the SWCNTs [73]. It has been observed that the elastic modulus of CNTs is not strongly dependent on the diameter. Primarily, the moduli of CNTs correlate to the amount of disorder in the nanotube walls [75].

2.2.3.2 Thermal Conductivity and Expansion

CNTs can exhibit superconductivity below 20 K (-253°C) due to the strong in-plane sigma bonds in between carbon atoms. The sigma bond provides exceptional strength and stiffness against axial strains. Moreover, the larger inter-plane and zero in-plane thermal expansion of SWCNTs results in high flexibility against non-axial strains.

Due to their high thermal conductivity and large in-plane expansion, CNTs exhibit exciting prospects in nanoscale molecular electronics, sensing and actuating devices, reinforcing additive fibers in functional composite materials, etc. Recent experimental measurements suggest that the CNT-embedded matrices are stronger in comparison to bare polymer matrices [76]. Therefore, it is expected that the nanotube may also significantly improve the thermo-mechanical and the thermal properties of the composite materials.

2.2.3.3 Field Emission

Under the application of strong electric field, tunnelling of electrons from the metal tip to vacuum results in the phenomenon of field emission. Field emission results from the high aspect ratio and small diameter of CNTs. The field emitters are suitable for the application in flat-panel displays. For multi-walled CNTs, the field emission properties occur due to the emission of electrons and light. Without applied potential, the luminescence and light emission occur through the electron field emission and visible part of the spectrum, respectively.

2.2.3.4 Aspect Ratio

One of the exciting properties of CNTs is the high aspect ratio, which infers that a lower CNT load is required compared to other conductive additives to achieve similar electrical conductivity. The high aspect ratio provides unique electrical conductivity in CNTs in comparison to the conventional additive materials such as chopped carbon fiber, carbon black, or stainless steel fiber.

2.2.3.5 Absorbent

Carbon nanotubes and CNT composites have been emerging as perspective absorbing materials due to their light weight, larger flexibility, high mechanical strength and large surface area. Therefore, CNTs emerge out as ideal candidates for use in gas, air and water filtration. The absorption frequency range of SWCNT-polyurethane composites broaden from 6.4 - 8.2 (1.8 GHz) to 7.5 - 10.1 (2.6 GHz) and to 12.0 - 15.1 GHz (3.1 GHz) [77]. A lot of research has already been carried out for replacing the activated charcoal with CNTs for certain ultra-high purity applications [78].

2.2.3.6 Conductivity

CNTs are assumed to be the most electrically conductive materials. However, it is quite difficult to control the chirality of the SWCNT shells and therefore statistically only 1/3rd of the CNTs in a bundle are assumed to be conducting and the rest of them are semiconducting. However, because of large diameters, the CNT shells of MWCNTs would be conductive even if they are of semiconductor characteristics. The energy gap between the conduction band edge and the Fermi level of a CNT shell is defined as [68]

$$\boldsymbol{E}_g = \frac{v_0 p_{C-C}}{d} \tag{2.10}$$

where d is the CNT diameter, v_0 is the nearest-neighboring tight-binding parameter and $p_{C\text{-}C}$ is the nearest neighbor C-C bond length, which is ~ 0.142 nm. From Eq. (2.10), it can be observed that the bandgap is inversely proportional to the diameter. Therefore, the semiconducting CNT shells with larger diameter are conductive. The detailed conductivity comparison between MWCNTs and SWCNTs will be discussed in the following sections.

2.2.4 Conductivity Comparison

The performance of interconnect primarily depends on the conductivity of the interconnect filler material. The conductivity comparison among Cu, SWCNT and MWCNT is analyzed in this section.

2.2.4.1 SWCNT Conductivity

The conductivity of SWCNT [9], [26] can be expressed as

$$\sigma_{SWCNT} = \frac{4G_0 l_0 d F_m}{\sqrt{3}(d+\delta)^2} \frac{l}{(l + l_0 d)} \tag{2.11}$$

where l, d, F_m are the interconnect length, shell diameter, fraction of metallic CNTs in the bundle, respectively, l_0 is 10^3, δ is 0.34 nm, G_0 is the quantum conductance equal to $2e^2/h$, e is the charge of an electron and h is the Planckøs constant.
For $l > l_0 d$, Eq. (2.11) can be expressed as

$$\sigma_{SWCNT} \approx \frac{4G_0 l_0 d F_m}{\sqrt{3}(d+\delta)^2} \tag{2.12}$$

From Eq. (2.12), it can be observed that for longer interconnects, the conductivity of SWCNT is independent of length.

2.2.4.2 MWCNT Conductivity

The conductivity of MWCNT [79] can be expressed as

$$\sigma_{MWCNT} = \frac{G_0 l}{2\delta}\left[\left(1-\frac{d_{min}^2}{d_{max}^2}\right)\frac{a}{2}+\left(b-\frac{l}{l_0}a\right)\times\left(\left(\frac{1}{d_{max}}-\frac{d_{min}}{d_{max}^2}\right)-\frac{l}{d_{max}^2 l_0}\ln\frac{d_{max}+\frac{l}{l_0}}{d_{min}+\frac{l}{l_0}}\right)\right] \quad (2.13)$$

where d_{max} and d_{min} are the outermost and the innermost shell diameters of an MWCNT, respectively; a and b are constants and the values are 0.0612 nm^{-1} and 0.425, respectively [80]. From Eq. (2.13), it can be observed that for $l > (l_0 b / a)$, the conductivity increases with an increase in d_{max}.

The conductivity comparison plot among Cu, SWCNT bundles and MWCNT is shown in Figure 2.8. It can be observed that for shorter interconnect length, the conductivity of SWCNT bundle is higher than MWCNT, whereas for longer lengths, MWCNTs can potentially have conductivities several times larger than that of copper or even SWCNT, which is essential for interconnect applications. It is worth noting that the best case scenario is considered for SWCNTs, wherein they were densely packed so that highest conductivity is obtained. However, in contrast to this, an average case scenario was considered for MWCNTs wherein the innermost diameter is half of the outermost shell diameter. The innermost diameters were considered as 5, 15, 35, 50 nm for respective outer diameters of 10, 30, 70, 100 nm. However, the best case scenario for MWCNTs would have been when the innermost diameter had been 1 nm. But still, for longer interconnects, the performance of the MWCNTs was better than the SWCNTs.

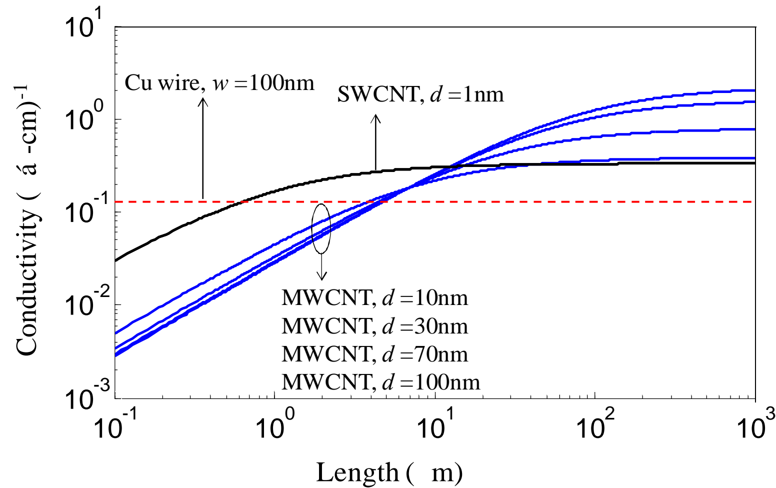


Figure 2.8. The conductivity comparison among Cu, SWCNT and MWCNT.

2.2.5 MWCNT Interconnect Modeling

MWCNTs have recently acquired importance for VLSI on-chip interconnect material due to their high current carrying capabilities. For the first time, Burke [81] proposed an electrical equivalent model for the analysis of carbon nanotube interconnects based on the Lüttinger liquid theory. The model considered the quantum effects of a nano wire by including the quantum resistance, kinetic inductance and quantum capacitance. The electrical equivalent model was further explained by Avouris *et al.* [82] through extensive study of electronic structure and transport properties of CNTs. Depending on the analysis, a bottom-up approach was demonstrated by Li *et al.* [83] to integrate MWCNTs into multilevel interconnects in silicon-integrated circuits. Ngo *et al.* [84] reported the mechanism of electron transport across metal CNT interface. The authors analyzed this mechanism for two different MWCNT architectures, horizontal or side-contacted MWCNTs and vertical or end-contacted MWCNTs. Later, Miano and Villone [85] extended the fluid theory model for frequency domain to describe the electromagnetic response of three dimensional (3D) structures formed by metallic CNTs and conductors within the framework of classical electrodynamics.

Xu and Srivastava [15] presented a semi-classical one-dimensional (1D) electron fluid model that took into account the electron-electron repulsive force. Based on the 1D electron fluid theory, the authors presented a transmission line model of metallic CNT interconnects using classical electrodynamics. However, the authors neglected the inter-CNT tunnelling phenomenon. Later, Li *et al.* [26] presented a multiconductor transmission line (MTL) model for the MWCNT. The authors considered the tunnelling effect between the adjacent shells in MWCNT and neighboring CNTs in a bundle. However, using the MTL model, the analysis of MWCNT with N number of tubes leads to the solution of differential equations with the system dimensional of $2N$, which can be computationally expensive. For this reason, the equivalent single conductor (ESC) model was proposed in [86]. The ESC model is based on the assumption that voltages at an arbitrary cross-section along MWCNT are the same, such that all nanotubes are connected in parallel at both ends. The accuracy of the ESC model in comparison to MTL model has been reported by several researchers [86, 87]. It was observed that the transient responses to a pulse

input of MTL model and ESC model are in good agreement. The MTL and ESC models are briefly described in the next section.

2.2.5.1 MTL and ESC models of MWCNT Interconnect

The electrical equivalent models of MWCNT interconnect are discussed in this section. The schematic cross-sectional view of MWCNT interconnect is shown in Figure 2.9. The MWCNT bundle interconnect line is positioned over a ground plane at a distance, H and placed in a dielectric medium with dielectric constant, ε. The MWCNT interconnect consists of N number of tubes with intershell distance, δ; inner shell diameter, d_1 and outer shell diameter, d_N. The total number of CNTs in an MWCNT can be expressed as

$$N = 1 + \text{int}\left[\frac{(d_N - d_1)}{2\delta}\right] \tag{2.14}$$

where int[.] represents an integer value. The number of conducting channels in a CNT can be derived by adding all the sub-bands contributing to the current conduction. Using Fermi function, it can be expressed as

$$N_{ch,i} = \sum_{\text{subbands}} \frac{1}{\exp\left(\left|E_i - E_F\right|/k_B T\right) + 1} \tag{2.15}$$

where T is the temperature, k_B is the Boltzmann constant, and E_i is the lowest (or highest) energy for the sub-bands above (or below) the Fermi level, E_F.

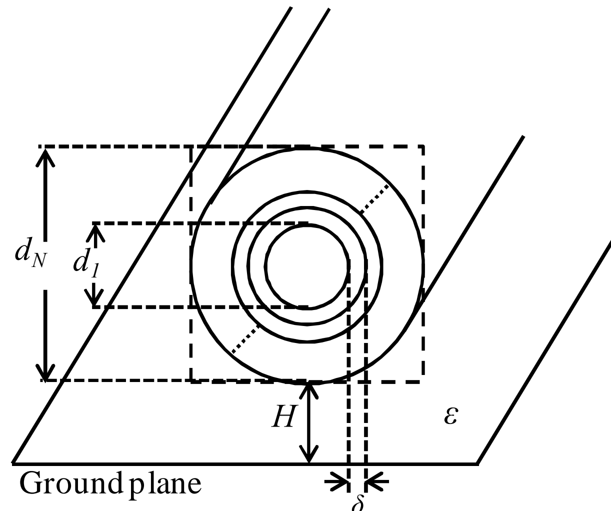
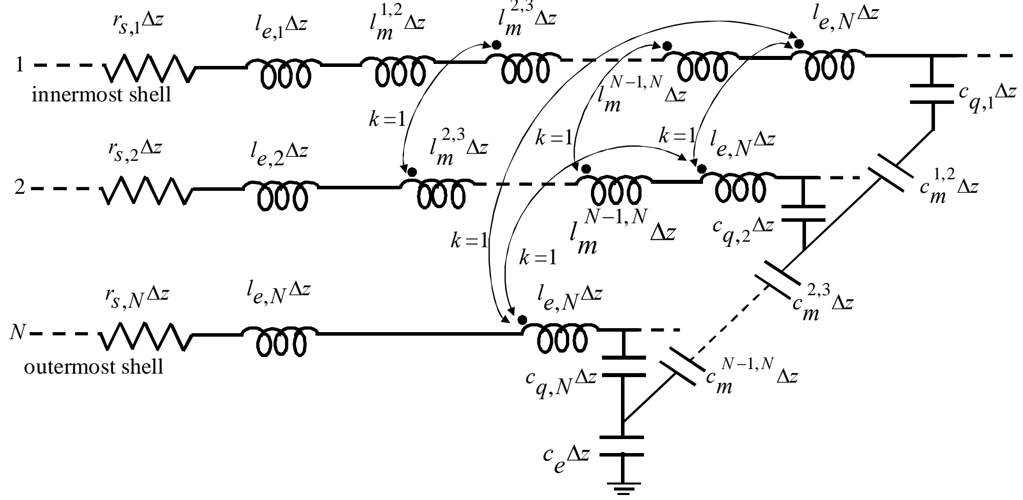
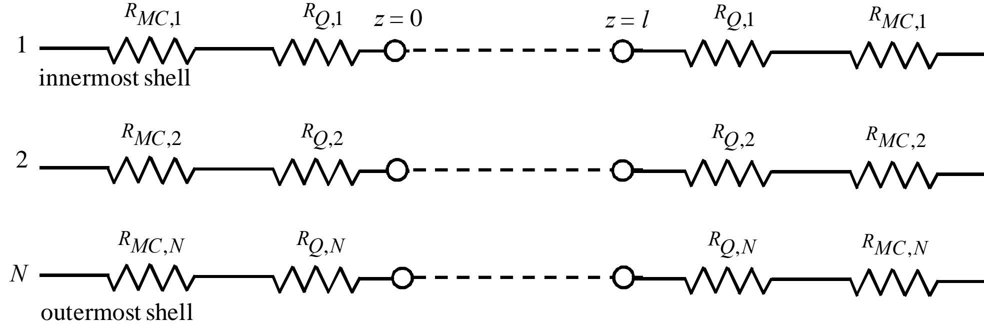


Figure 2.9. Geometry of an MWCNT with N shells above a ground plane.



(a)



(b)

Figure 2.10. Multiconductor transmission line model of MWCNT (a) section of infinitesimal length ê *z,* where k = 1 represents perfect magnetic coupling (b) nanotube of length l including terminal resistance.

The multiconductor transmission line (MTL) model of MWCNT interconnect is described in Figure 2.10, where $R_{MC,i}$ and $R_{Q,i}$ represent the imperfect metal contact resistance and quantum resistance of ith shell, respectively; $r_{s,i}$, $l_{k,i}$ and $c_{q,i}$ represent the p.u.l. scattering resistance, kinetic inductance and quantum capacitance, respectively. The parasitics $R_{Q,i}$, $r_{s,i}$, $l_{k,i}$ and $c_{q,i}$ can be expressed as

$$R_{Q,i} = \frac{h}{4e^2 N_{ch,i}} \tag{2.16a}$$

$$r_{s,i} = \frac{h}{2e^2 \lambda_{mfp,i} N_{ch,i}} \tag{2.16b}$$

$$l_{k,i} = \frac{h}{4e^2 v_F N_{ch,i}} \tag{2.16c}$$

$$c_{q,i} = \frac{4e^2 N_{ch,i}}{h v_F} \tag{2.16d}$$

where h, e λ_{mfp} and v_F represent the Planckøs constant, electron charge, mean free path and Fermi velocity, respectively.

In Figure 2.10, $l_{e,i}$ is p.u.l. magnetic inductance of the ith shell and c_e is p.u.l. electrostatic capacitance, $c_m^{i,i+1}$ and $l_m^{i,i+1}$ are the p.u.l. coupling capacitance and mutual inductance between the shells, respectively. These parasitics can be expressed as

$$l_{e,i} = \frac{\mu_0 \mu_r}{2\pi} \cosh^{-1}\left[\left(\frac{d_i + 2H}{d_i}\right)\right] \tag{2.16e}$$

$$c_e = \frac{2\pi\varepsilon_0\varepsilon_r}{\cosh^{-1}\left[\left(\frac{d_N + 2H}{d_N}\right)\right]} \tag{2.16f}$$

$$c_m^{i,i+1} = \frac{2\pi\varepsilon_0}{\ln(d_{i+1}/d_i)},\ i = 1,2,\cdots\cdots, N\text{-}1 \tag{2.16g}$$

$$l_m^{i,i+1} = \frac{\mu}{2\pi} \ln\left(d_{i+1}/d_i\right),\ \ i = 1,2,\cdots\cdots, N\text{-}1 \tag{2.16h}$$

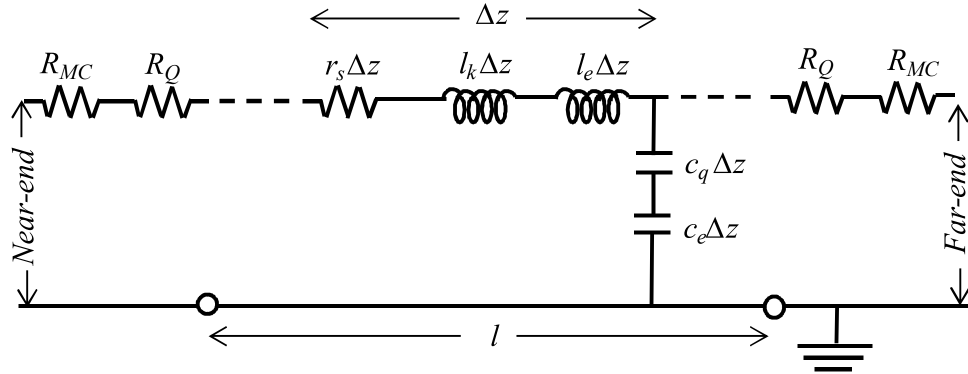


Figure 2.11. Equivalent single conductor model of MWCNT.

To reduce the complexity of the MTL model, a simplified equivalent single conductor model was proposed in [86]. The equivalent single conductor model is shown in Figure 2.11. This model was developed based on the assumption that voltages at an arbitrary cross-section along MWCNT are the same. Thus, all the

scattering resistances, $r_{s,i}$ are in parallel and can be replaced by an equivalent resistance ($r_{s,ESC}$). The $r_{s,ESC}$ can be expressed as

$$r_{s,ESC} = \frac{h/e^2}{\sum_{i=1}^{N} 2N_{ch,i}\lambda_{mfp,i}} \tag{2.17a}$$

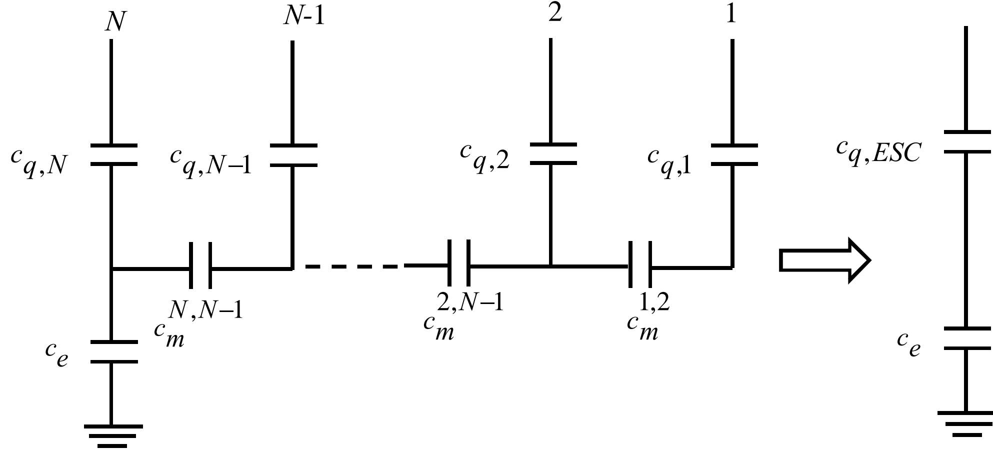


Figure 2.12. Per unit length capacitance network of the MWCNT.

Referring to Figure 2.12, the distributed MWCNT capacitance, $c_{q,ESC}$ is expressed in terms of quantum capacitance and coupling capacitance between shell to shell.

$$c_{equ,1} = c_{q,1} \tag{2.17b}$$

$$c_{equ,i} = \left(\frac{1}{c_{equ,i-1}} + \frac{1}{c_m^{i-1,i}}\right)^{-1} + c_{q,i},\ i = 2, 3, \cdots\cdots, N \tag{2.17c}$$

$$c_{q,ESC} = c_{equ,N} \tag{2.17d}$$

The inductance equations can be written in a similar form. The ESC model of MWCNT interconnect is thoroughly discussed in Section 4.2.

2.2.6 MWCNT Performance Analysis

The performance analysis of MWCNT interconnects was analyzed by using both the MTL and ESC models in [88]. The voltage response of two coupled MWCNT interconnects of 14 and 22 nm technologies was computed to a pulse input. It was observed that both models are in good agreement. The same agreement was achieved in the estimation of 50% time delay as well. The validity of the ESC model was also verified experimentally in [86]. Based on the ESC model, Lamberti *et al.* [89] compared the performance of MWCNTs with SWCNTs. The propagation delay

time was analyzed at three different technologies 15, 21, and 32 nm by means of interval analysis. It was observed that for global interconnect lengths, the time delay obtained for MWCNT interconnects is less than 1 ns for the most severe configuration, *i.e.*, for 15 nm technology node at a length of 250 m, whereas for SWCNTs the delay is as large as 7.87 ns.

The estimation of performance parameters under the crosstalk influence is an important design concern in modern VLSI interconnects. The crosstalk analysis of MWCNTs has been studied by several researchers. Liang *et al*. [90] analyzed the crosstalk noise effects with lengths ranging from 10 to 1000 µm at 22 and 14 nm technology nodes. Moreover, the performance of MWCNTs was compared with the Cu interconnects. They observed that the MWCNT interconnects showed better performance for longer wire lengths and smaller technology nodes. Das *et al*. [12] analyzed the crosstalk effects in Cu, SWCNT and MWCNT interconnects. They observed that the MWCNT based interconnects are more suitable for VLSI interconnects. Furthermore, the authors analyzed the power supply voltage drop for Cu and MWCNT based interconnects in [91]. It was observed that the CNT based interconnects have significantly less power drop in comparison to that of Cu based interconnects for semi-global and global lengths. Based on the ESC model, Liang *et al*. [21] investigated the crosstalk effects in Cu and MWCNT interconnects. They reported that the crosstalk induced time delays in MWCNT interconnects are much smaller than those in the Cu interconnects. Sahoo and Rahaman [92] developed an analytical closed form of delay expression for both Cu and MWCNT interconnects. They observed that the performance of MWCNT interconnects over copper interconnects is improved by 90% for 200 µm long interconnect. In 2015, Tang *et al.* [93] proposed a fast transient simulation technique based on the ESC model for the crosstalk induced performance analysis of MWCNT interconnects. They observed that the proposed method and HSPICE are very similar to each other with an average relative error of 1.54%. However, most of the researchers [21, 90, 92, 93] used the resistive driver in the performance analysis of MWCNT interconnects that leads to severe errors in the performance estimation of the driver interconnect load (DIL) systems.

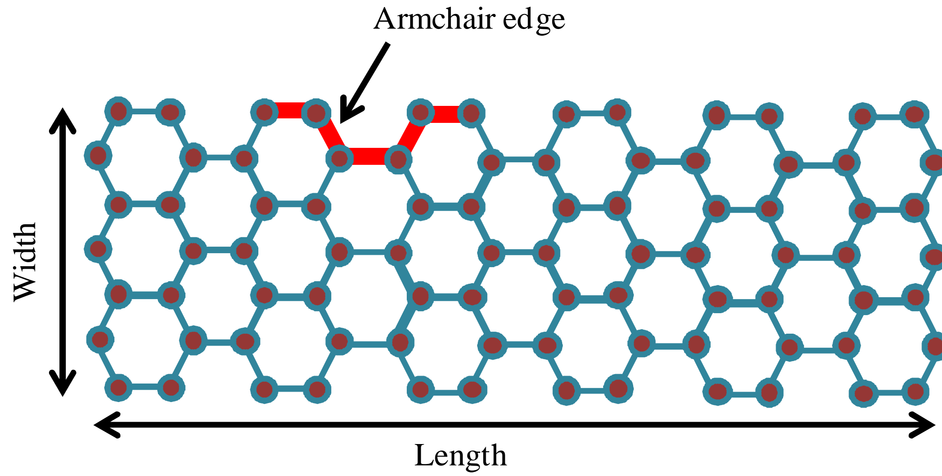
2.3 Graphene Nanoribbons

In 1996, Mitsutaka Fujita and his group provided a theoretical model of graphene nanoribbons (GNRs) to observe the edge and nanoscale dimension effect in graphene [94, 95]. Recent developments in GNRs have aroused a lot of research interest of their potential applications in the area of interconnects and field effect transistors [96-98]. A monolithic system can be constructed using the single layer GNR for both transistors and interconnects. For nanoscale device dimensions, Cu based interconnects are mostly affected by grain boundaries and sidewalls scatterings. It has been predicted that GNRs will outperform the Cu interconnects for smaller widths [99]. In a high quality GNR sheet, the mean free path is ranging from 1-5   m. GNRs can carry large current densities of more than 10^8 A/cm^2. They also offer high carrier mobility that can reach up to 10^5 cm^2/(V·s) [100].

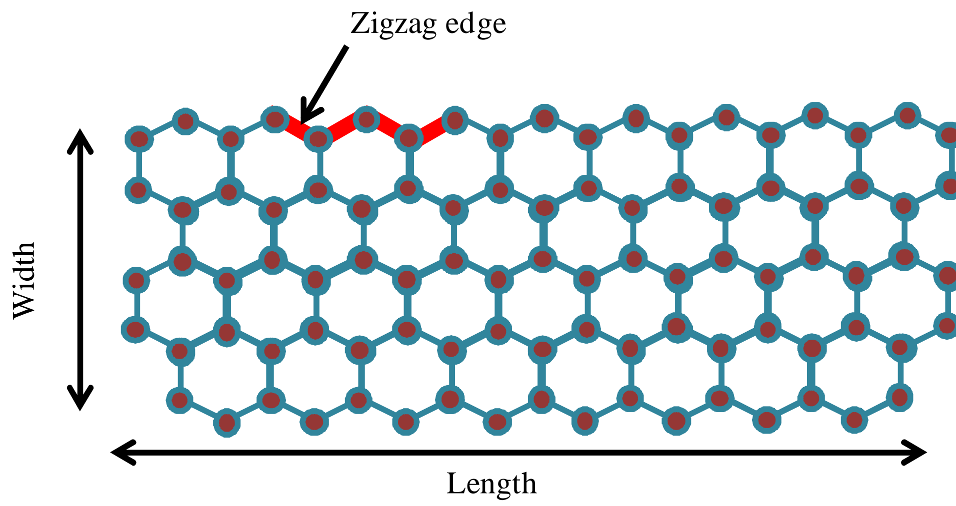
2.3.1 Basic Structure of GNRs

A graphene nanoribbon is a single sheet of graphene layer, which is extremely thin and limited in width, such that it results in a one-dimensional structure [101]. As a result, GNRs can be considered as an unrolled version of CNTs. The electronic properties of GNRs are similar to that of CNTs. Depending on termination of their width, GNRs can be divided into chiral and nonchiral GNRs. The chiral GNRs can be further classified as armchair (ac) or zigzag (zz) GNRs as shown in Figures 2.13 (a) and (b), respectively. It can be noted that the terms õarmchairö and õzigzagö are used for both GNRs and CNTs. However, these nomenclatures are used in opposite ways. For GNRs the terms armchair and zigzag indicate the pattern of the GNR edge, whereas for CNTs the same terms indicate the CNT circumference. Therefore, the unrolled armchair CNT can be visualized as a zigzag GNR and vice-versa.

Depending on the stacked graphene sheets, GNRs are classified as single-layer GNR (SLGNR) or multi-layer GNR (MLGNR). The most promising interconnect solution for VLSI interconnect is MLGNR due to its higher current carrying capability than SLGNR. The geometric structure of an MLGNR is shown in Figure 2.14. The MLGNR interconnect consists of N number of layers, with interlayer distance, δ width, w and thickness, t.



(a)



(b)

Figure 2.13. Structure of GNR (a) armchair and (b) zigzag.

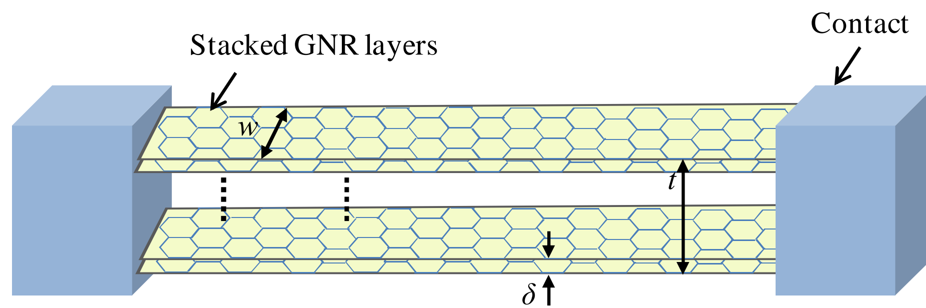


Figure 2.14. The geometric structure of an MLGNR interconnect.

From the fabrication point of view, it is evident that the growth of the GNRs can be more easily controlled than that of the CNTs because of their planar structure. This makes them compatible with the conventional lithography techniques [30]. Using the electron beam lithography technique, Murali *et al.* [27] fabricated an MLGNR interconnect with ten layers. The higher electrical conductivity in MLGNR can be obtained either by enhancing the carrier mobility or by increasing the number of carriers. The carrier mobility can be increased by intercalation doping of arsenic pentafluoride (AsF_5) vapor. Using the AsF_5 doping, the conductivity of MLGNR can be increased up to 3.2×10^5 S/cm, which is almost 1.5 times higher than the copper interconnects [102]. Additionally, the easier fabrication process of MLGNRs makes them as promising candidates for interconnect material.

2.3.2 Semiconducting and Metallic GNRs

GNRs can act as either semiconducting or metallic based on the pattern of the GNR edge. The zigzag edge patterned GNR always act as metallic, whereas the armchair edge patterned GNRs can act as either metallic or semiconducting depending on the number of carbon atoms present across the width of the GNR. This section presents the behaviour of armchair GNRs and its dual nature.

The typical structure of armchair GNR is shown in Figure 2.13 (a), where the number of carbon atoms across its width, $N_C = 7$. For understanding the metallic/semiconducting behaviour of GNRs, it is necessary to analyze the electronic band structures. The band structures of GNRs are obtained using a tight binding (TB) model [103]. Using the TB approach, the band structures of 23- and 24- atom wide armchair GNRs are shown in Figures 2.15 (a) and (b), respectively. It can be observed that the metallic GNR has zero band gap, whereas the semiconducting GNR has 0.2 eV band gap. The ac GNR acts as metallic, if $N_C = 3a+2$ and acts as semiconducting, if $N_C = 3a+1$ or 3, where a is an integer. The zz GNRs are always metallic, independent of the value of N_C [103].

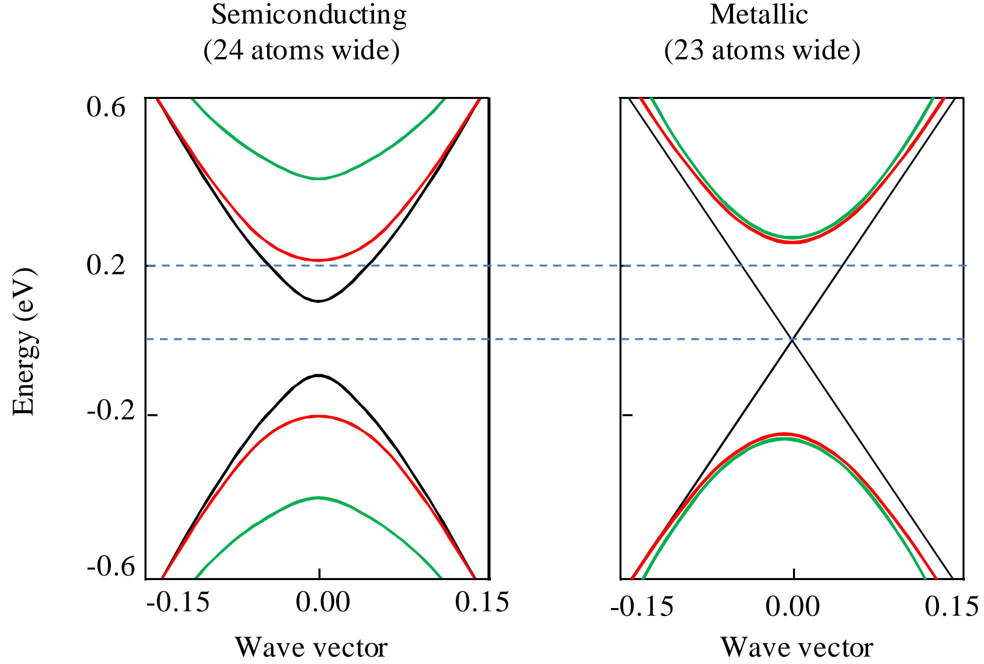


Figure 2.15. Band structures of (a) semiconducting and (b) metallic armchair GNRs whose widths are 6.02 nm (24 atoms wide) and 5.78 nm (23 atoms wide), respectively [103].

2.3.3 Properties and Characteristics of GNRs

Most of the physical and electrical properties of GNRs are similar to that of CNTs. However, compared to CNTs, the growth of the GNRs is considered to be more controllable due to their planar structure. Moreover, the major advantage of GNRs over CNTs is that both transistor and interconnect can be fabricated on the same continuous graphene layer, which unlike CNTs, are free from Stone-Wales defects [104]. Therefore, one of the manufacturing difficulties regarding the formation of metal-nanotube contact can be avoided. Due to the lower resistivity, the MLGNRs are often preferred over SLGNRs as suitable on-chip interconnect material. However, the MLGNRs fabricated till date, have displayed some level of edge roughness [30], [31]. The electron scattering at the rough edges reduces the mean free path that substantially lowers the conductance of the MLGNR. This fundamental challenge limits the performance of MLGNR based interconnects. The value of MFP primarily depends on the level of edge roughness. The following sections discuss the effect of edge roughness on the MFP.

2.3.3.1 Mean Free Path of GNR

The effective MFP of GNR, λ_{eff}, depends on the scattering effects due to phonons, λ_{ph}, defects, λ_d and edge roughness, λ_n. Using Matthiessenøs rule, the λ_{eff} can be expressed as

$$\frac{1}{\lambda_{eff}} = \frac{1}{\lambda_d} + \frac{1}{\lambda_n} + \frac{1}{\lambda_{ph}} \tag{2.18}$$

For the interconnect applications (low bias), the MFP corresponding to λ_{ph} is observed as extremely large, *i.e.*, tens of micrometers, and therefore, its effect can be neglected for the modeling of GNR scattering resistance [103]. Consequently, λ_d and λ_n dominate the overall value of λ_{eff}.

According to the experimental measurements reported in [31], the MFP corresponding to λ_d is about 1   m for a single layer GNR, which is width independent. However, in multilayer GNR, the MFP reduces due to the inter-sheet electron hopping [105]. The λ_d of MLGNR can be extracted by measuring the in-plane conductivity of GNR. Using the in-plane conductivity of $G_{sheet} = 0.026$ (á -cm)$^{-1}$ [106], layer spacing of 0.34 nm and $E_F = 0$ of a neutral MLGNR, the λ_d is extracted as 419 nm by solving equation (2.19) [106]

$$G_{sheet} = \frac{2q^2}{h} \cdot \frac{\pi\lambda_d}{hv_f} \cdot 2k_B T \, ln\left[2\cosh\left(\frac{E_F}{2k_B T}\right)\right] \tag{2.19}$$

To increase the conductivity of MLGNR, AsF_5 intercalated graphite can be used. The in-plane conductivity, $G_{sheet} = 0.63$ (µá -cm) ^{1} and carrier concentration, $n_p = 4.6\times10^{20}$ cm^{-3} are observed for the AsF_5 intercalated graphite [107]. Using the simplified TB model, the E_F can be expressed as

$$E_F = hv_F \left(\frac{n_p \cdot \delta}{4\pi}\right)^{1/2} \tag{2.20}$$

where $\delta = 0.575$ nm is the average layer spacing between adjacent graphene layers. Using the expressions (2.19) and (2.20), E_F and λ_d are expressed as 0.6 eV and 1.03 µm, respectively.

The MFP corresponds to diffusive scattering at the edges is a function of edge backscattering probability, P and the average distance by an electron travels along the

length before hitting the edge. The mean free path for n^{th} sub-band due to edge scattering can be expressed as [99]

$$\lambda_n = \frac{w}{P}\sqrt{\left(\frac{E_F/\Delta E}{n}\right)^2 - 1} \tag{2.21}$$

where ê E is the gap between the sub-bands.

2.3.4 Conductivity Comparison

The performance of the interconnect line is primarily depends on the conductivity of the material. This section discusses the conductivity of various interconnect materials. Figure 2.16 shows the conductivity of Cu, SWCNT bundle, MWCNT and MLGNR interconnects. The fully specular edge MLGNR interconnects are analyzed for two different doped conditions [108]. Firstly, the Fermi energy level of 0.3 eV is considered and secondly, the level of 0.6 eV is considered. The SWCNT diameter is chosen to be 1 nm with a metallic to semiconducting ratio (F_m) of 1/3. For MWCNTs, the outer diameter of CNT shell is considered as 15 nm. From Figure 2.16, it can be observed that the conductivity of MLGNR increases with the Fermi energy. Moreover, at highly doped condition (E_F = 0.6 eV) the conductivity of MLGNR is observed to be higher than MWCNT interconnects.

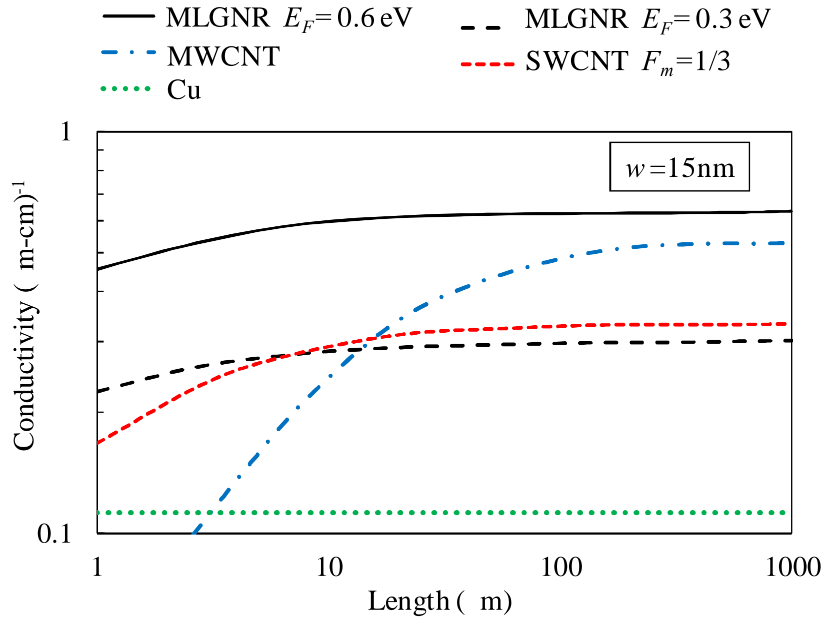


Figure 2.16. Conductivity comparison among Cu, SWCNT bundle, MWCNT and MLGNR interconnects.

2.3.5 MLGNR Interconnect Modeling

This section presents an electrical equivalent model of the MLGNR interconnect line. An MLGNR of width, w and thickness, t is placed above the ground plane at a distance, H as shown in Figure 2.17. The permittivity of the medium between the bottommost layer of MLGNR and the ground plane is represented by ε. The total number of layers (N_{layer}) can be expressed as

$$N_{layer} = 1 + \text{int}\left[\frac{t}{\delta}\right] \tag{2.22}$$

The interlayer distance, δ is considered to be 0.575 nm and 0.34 nm for doped and neutral MLGNRs [106], respectively.

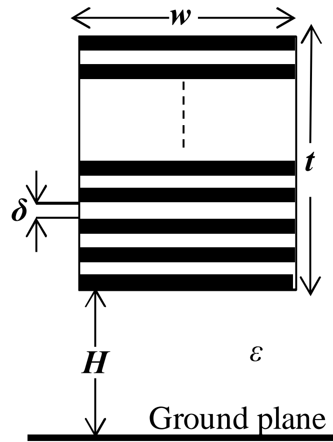


Figure 2.17. Geometry of MLGNR above ground plane.

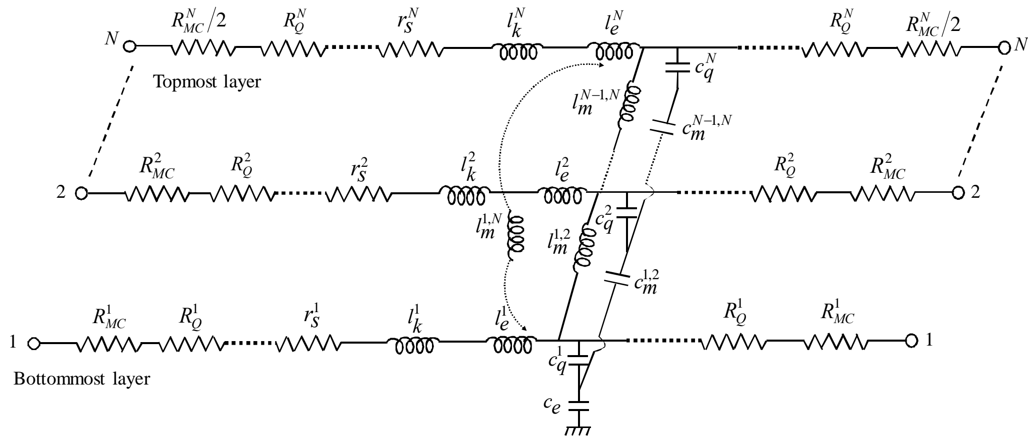


Figure 2.18. Equivalent *RLC* model of MLGNR interconnect.

The equivalent electrical model of MLGNR interconnect is presented in Figure 2.18, wherein the parasitics are primarily dependent on the number of conducting channels (N_{ch}) of each layer in MLGNR. The N_{ch} takes into account the effect of spin and sub-lattice degeneracy of carbon atoms and primarily depends on the width, Fermi energy (E_F), temperature (T) and can be expressed as [109]

$$N_{ch} = \sum_{n=0}^{n_C} \left[e^{(E_i - E_F)/kT} + 1 \right]^{-1} + \sum_{n=0}^{n_V} \left[e^{(E_i + E_F)/kT} + 1 \right]^{-1} \tag{2.23}$$

where k, n_C and n_V represent the Boltzmann constant, number of conduction and valence bands, respectively. E_i is the lowest/highest energy of ith sub-band in conduction/valence band [109].

Depending on the current fabrication process, the imperfect metal-MLGNR contact resistance (R_{MC}) has a typical value ranging from 1 k to 20 k [37]. Each layer of MLGNR exhibits lumped quantum resistance (R_Q) that is due to the quantum confinement of carriers across the interconnect width. The quantum resistance of jth layer (R_Q^j) can be expressed as

$$R_Q^j = \frac{h}{4e^2 . N_{ch}} \tag{2.24}$$

For longer interconnects, scattering resistance, r_s appears due to the static impurity scattering, defects, line edge roughness scattering (LER), etc. [17], [110, 111]. The r_s primarily depends on the effective MFP of electrons (λ_{eff}) and can be expressed as

$$r_s^j = \frac{h}{2e^2 . N_{ch} . \lambda_{eff}} \tag{2.25}$$

Using the Matthiessen's rule, the λ_{eff} of each sub-band can be expressed from (2.18). Each layer in MLGNR comprises of kinetic inductance (l_k) and quantum capacitance (c_q) that represent the mobile charge carrier inertia and the density of electronic states, respectively. The l_k and c_q of any layer j can be expressed as

$$l_k^j = \frac{l_{k0}}{2N_{ch}} \text{; where } l_{k0} = \frac{h}{2e^2 v_F} \tag{2.26}$$

$$c_q^j = 2c_{q0} \cdot N_{ch}\text{; where } c_{q0} = \frac{2e^2}{hv_F} \tag{2.27}$$

where v_F é 8×10^5 m/s represents the Fermi velocity of carriers in graphene [37]. The kinetic inductance per channel is 8 nH/ m, that is verified by the experimental observations also [14]. The electrostatic capacitance (c_e) is due to the electric field coupling between the bottom most layer of MLGNR and the ground plane. Therefore, the c_e is primarily dependent on the MLGNR width (w) and the distance (H) from the ground plane. Apart from this, the magnetic inductance (l_e) of MLGNR interconnect is due to the stored energies of carriers in the magnetic field. The l_e and c_e can be expressed as

$$l_e^j = \frac{\mu_0 \mu_r H}{w} \text{ and } c_e = \frac{\varepsilon_0 \varepsilon_r w}{H} \tag{2.28}$$

The inter-layer mutual inductance (l_m) and coupling capacitance (c_m) are mainly due to the magnetic and electric field coupling between the adjacent layers. The l_m and c_m can be expressed as

$$l_m^{j-1,j} = \frac{\mu_0 \delta}{w}\ ,\ j = 2, 3, \cdots\cdots, N \tag{2.29a}$$

$$c_m^{j-1,j} = \frac{\varepsilon_0 w}{\delta},\ \ j = 2, 3, \cdots\cdots, N \tag{2.29b}$$

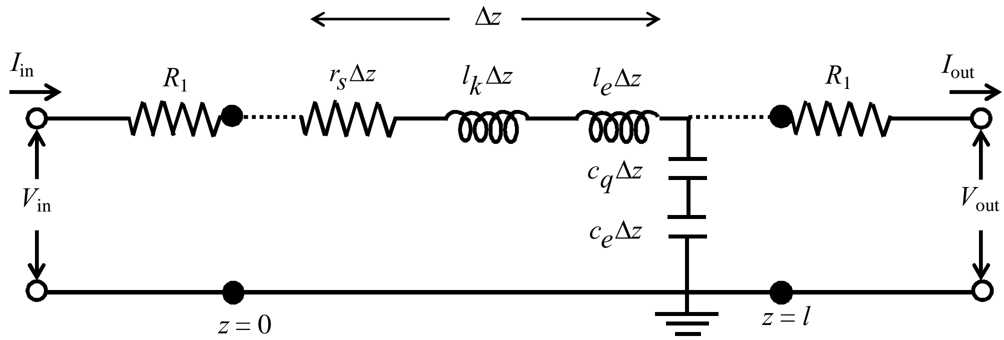


Figure 2.19. Equivalent single conductor (ESC) model of MLGNR interconnect.

The analysis of signal propagation along an MLGNR with N_{layer} leads to the solution of a 2N dimensional system of differential equations that can be highly time consuming. For this reason, the equivalent *RLC* model of Figure 2.18 is simplified to an ESC model shown in Figure 2.19, wherein all the layers are assumed to be parallel.

The value of $R_1 = (R_{MC} + R_Q)$ is equally divided between the two contacts on either side of the interconnect line. The detailed explanation of ESC model of MLGNR interconnect line is provided in Section 5.2.

2.3.6 MLGNR Performance Analysis

The performance of an MLGNR interconnect is generally evaluated by means of an electrical equivalent model. The equivalent model considers all the parasitic parameters based on the quantum effects of the nanowire, and its electrostatic and magnetostatic characteristics. Sarto *et al.* proposed an electrical equivalent transmission model to represent the MLGNR interconnect [112]. They compared the performance between MWCNT and MLGNR interconnects and observed that the MLGNR interconnect has higher current carrying capability than the MWCNT interconnect. Xu *et al*. [106] derived the conductance model of MLGNR interconnect using the tight binding approach and the Landauer formula. The conductance of the MLGNR compared among Cu, W and CNTs. They observed that the conductance of MLGNR is much higher than the Cu, W and CNTs when proper intercalation doped MLGNRs are used. Nishad *et al*. [113] presented the analytical time domain models for the performance analysis of top contact and side contact MLGNR interconnects. Based on the analytical models, they designed an optimum top contacted MLGNR interconnect that exceeds the performance of Cu and optical interconnects.

The crosstalk induced signal transmission analysis of MLGNR interconnects was performed by Cui *et al*. [37] based on the transmission line model. The authors obtained the output response of driver-interconnect-load system using the transfer function. The impact of Fermi level on the signal transmission was also investigated. In 2014, Zhao *et al*. [108] performed the comparative study on MLGNR interconnects with SWCNT, MWCNT and Cu interconnects. They observed that even with the maximum crosstalk impacts considered, the advantage of MLGNR interconnects over other interconnect materials can still be maintained. The impact of MLGNR line resistance variations on the crosstalk induced performance parameters were investigated in [114]. The simulations were performed for 11 and 8 nm technology nodes for both intermediate and global interconnect lengths. They observed that irrespective of technology node, the perfectly doped fully specular MLGNR interconnects are better than Cu interconnects as far as the line resistance tolerance

was concerned. However, the existing crosstalk noise models [37], [108], [114] analyzed the performance of MLGNR interconnects with resistive drivers that limits the accuracy of the models. Moreover, the authors considered the mean free path parameter independent of width by assuming perfectly smooth edges of MLGNRs.

2.4 Technical Gaps

Based on the literature survey, it is observed that the analysis of distributed transmission lines in the presence of nonlinear elements (CMOS driver) suffers from the mixed frequency/time domain problem. This problem arises from the fact that transmission lines are described by partial differential equations that are traditionally solved in the frequency domain, whereas the nonlinear elements are described only in the time domain. Accordingly, in the crosstalk noise models of Cu [4], [6], [59], MWCNT [5], [21], [93] and MLGNR [37], [108], [114] interconnects, the non-linear CMOS drivers were approximately considered as resistive drivers that limits the accuracy of the models. Therefore, an efficient crosstalk noise model is utmost required to accurately analyze the performance of different on-chip interconnects. The following research gaps are noticed from the literature survey on the crosstalk noise modeling of on-chip interconnects:

- Most of the existing crosstalk noise models of Cu interconnect approximately considered the non-linear CMOS driver as a linear resistor [4], [6], [59]. This approximation is not valid for on-chip interconnects, since it has been observed that during the transition time transistor operates in the linear region as well as the saturation region. The percentage of time in saturation region is about 50%. It is known that the driver has a significant effect on delay and crosstalk noise measurements. Thus, assuming that the transistor operates in the linear region during the transition region leads to severe errors in estimating performance parameters such as propagation delay and peak voltage. The reported CMOS gate driven interconnect models are based on the even and odd modes and hence limited to only two coupled interconnects. Moreover, the performance analysis that was carried out for lossless lines, which is impractical.
- The multi-walled carbon nanotubes (MWCNTs) have drawn much attention in scientific research due to their unique physical and electrical properties. The MWCNT can support large current densities up to 10^9A/cm^2 and have long mean

free paths in the range of several micrometers. Previously, several researchers [5], [21], [93] performed the crosstalk noise of MWCNT interconnects, but they approximately considered the non-linear CMOS driver as a linear resistor. Therefore, it is important to develop a model that correctly models the effect of MWCNT interconnects while incorporating the non-linear effects of CMOS driver.

- During the recent past, the multi-layer graphene nanoribbon interconnects have also been considered aggressively by the researchers as a potential alternative material for realizing on-chip interconnects. The great advantage of GNRs compared to CNTs is the possibility of forming õmonolithicö device interconnect structures. Using the proper combinations of metallic and semiconducting regions the entire circuit can be seamlessly formed out of one patterned graphene sheet [104]. Using the equivalent transmission line model, the crosstalk effects of coupled MLGNR have been studied in [37], [108], [114]. However, the researchers used resistive driver in the analysis of MLGNR interconnects. Moreover, the authors considered the mean free path parameter independent of width by assuming perfectly smooth edges. However, in reality the GNRs fabricated till date, exhibit edge roughness [30], [31]. Due to these rough edges, the electrons backscatter, thereby decreasing the overall MFP. At lower widths, the MFP is predominantly dependent on the edge roughness. Therefore, it is essential to incorporate width-dependent MFP while modeling the CMOS gate driven MLGNR interconnects.
- It would be interesting to analyze the crosstalk effects of complete driver-interconnect-load system for different on-chip interconnects such as Cu, MWCNT and MLGNR interconnects. The performance parameters such as propagation delay, crosstalk noise voltage, and its timing instances are highly affected by crosstalk and it is very much essential to develop a mathematical model to analyze the crosstalk effects in CMOS gate driven on-chip interconnects. For the accurate analysis, the non-linear CMOS driver effects must be incorporated in the model. Unfortunately, there is no existing model to meet these requirements.

This thesis presents the accurate numerical models for the crosstalk induced performance analysis of different on-chip interconnects such as Cu, MWCNT and

MLGNR interconnects. The time/frequency domain conversion problem is addressed by analyzing the interconnect lines in time domain using the FDTD technique. In a more realistic manner, the proposed model includes the effect of width-dependent MFP of the MLGNR while taking into account the edge roughness.

Chapter 3

FDTD Model for Crosstalk Analysis of CMOS Gate-Driven Coupled Copper Interconnects

3.1 Introduction

Traditionally, non-linear CMOS driver has been modeled as a linear resistor in the performance analysis of a driver-interconnect-load system [4], [6], [59]. This approximation is not valid for on-chip interconnects because during the input and output transition states the MOSFET operates in cutoff, linear and saturation regions [1], [115-117]. The value of change in resistance in saturation region is much higher than the linear region. Especially, the PMOS operates in the saturation region for more than 60% of time and in the linear region for less than 5% of time [35]. Thus, assuming that the transistor operates in the linear region, leads to severe errors in the performance estimation of the driver-interconnect-load system.

The modeling of distributed *RLC* lines along with non-linear CMOS driver suffers with frequency/time domain conversion problem. This problem arises because the transmission lines were traditionally solved in the frequency domain by using the partial differential equations, whereas the CMOS driver elements appeared in the time domain. A direct way to avoid this conversion problem is the use of the FDTD technique to solve the transmission line equations. Using the FDTD technique, the analysis of transmission lines for the resistive load and resistive driver was proposed in [39]. Including the frequency dependent losses, Orlandi *et al.* [41] proposed FDTD model for the analysis of multiconductor transmission lines terminated in arbitrary loads using the state-variable analysis. FDTD-like techniques are also available to solve coupled transmission lines namely, latency insertion method [118], and alternating direction explicit-latency insertion method [119]. However, the models proposed in [39], [41], [118, 119] analyses the transmission lines with resistive loads and not valid for the on-chip interconnects performance, which are actually excited and terminated by the CMOS inverters.

Based on the FDTD technique, Li *et al.* [42] proposed a model for the analysis of CMOS gate-driven distributed *RLC* interconnects. Interconnect lines were analyzed at global interconnect length using 180 nm technology node. However, this model ignores the finite drain conductance parameter (σ). Therefore, using [42], the estimated current is higher than the actual value and also assumes that the MOS drain current in the saturation region (I_{dsat}) is independent of drain voltage (V_{ds}), which is not applicable in actual practice. Moreover, the analysis in [42] is limited to functional crosstalk wherein only one of the lines is switching. As the dynamic crosstalk occurs frequently in the coupled interconnect lines, its analysis is essential for current technology nodes. The proposed model considers all these effects appropriately and measures the crosstalk induced performance parameters accurately.

This chapter presents an accurate model for comprehensive crosstalk analysis of coupled-multiple interconnects, including the functional and dynamic crosstalk effects. The proposed model considers the non-linear effects of the CMOS driver as well as the transmission line effects of interconnect line that includes coupling capacitance and mutual inductance effects. The CMOS driver is represented by the *n*-th power law model [120], and the coupled-multiple interconnect lines are modeled by FDTD with second order accuracy. The results demonstrate that the proposed model has high accuracy with respect to HSPICE.

The rest of the chapter is organized as follows: Section 3.2 describes the motivation behind this work. In Section 3.3, the FDTD technique combined with *n*-th power law model is developed for coupled-two lines that can be extended to multiple lines. Section 3.4 is devoted to the validation of proposed model for coupled-two lines and Section 3.5 confirms the validation of model for extended coupled lines. Finally, Section 3.6 concludes this chapter.

3.2 Motivation

Most of the researchers perform the analysis of the CMOS gate-driven on-chip interconnects by representing the non-linear CMOS driver with a resistive driver [4], [6], [59]. The equivalent resistance (R_{eq}) value is obtained by averaging the resistance values at the endpoints of the transition region. Using the Taylor expansion, R_{eq} is expressed as [1]

$$R_{eq} = \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\sigma V_{DD}\right) \tag{3.1}$$

where I_{DSAT} is drain saturation current and σ is the finite drain conductance parameter.

Coupled-two interconnects driven by CMOS inverter and resistive driver are shown in Figures 3.1 and 3.2, respectively, where R, L, and C are per unit length (p.u.l.) line resistance, line inductance and ground capacitance, respectively. The coupling capacitance and mutual inductance are represented respectively by C_{12} and L_{12} and the values are obtained in p.u.l.

To justify the motivation, the transient response is compared between the two structures using HSPICE simulations. For symmetric operations of CMOS inverter, the ratio of PMOS to NMOS width is chosen as 2 [1]. The input transition time is chosen as 10 ps. Using the above-mentioned setup, the signal integrity analysis is carried out at the global level interconnect length of 1 mm for 32 nm technology and 0.9 V of V_{DD}. The width of interconnect is assumed to be equal to the space between the two interconnects, and the thickness of the line is assumed to be equal to height from the ground plane. The resistivity of the copper material and the relative permittivity of the inter layer dielectric medium are chosen as 2.2 (á -cm) and 2.2, respectively. Using 0.22 µm line width and an aspect ratio of 3 [121], the associated parasitic values are listed in Table 3.1. The load capacitance C_L is chosen as 2 fF. The device and interconnect dimensions are corresponding to 32 nm technology node and can be mapped to a real integrated circuit.

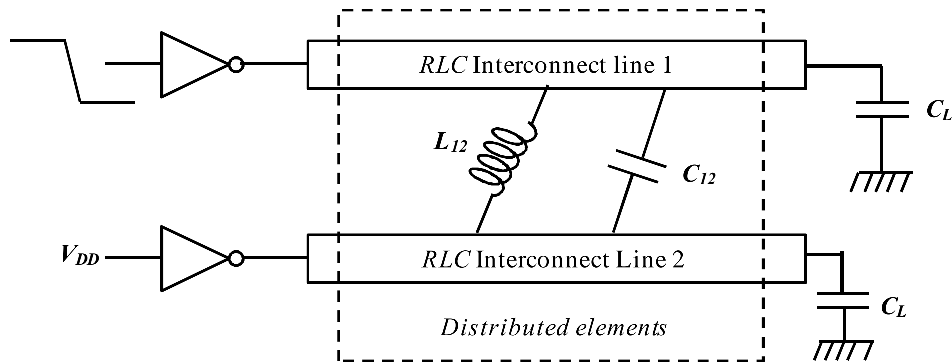


Figure 3.1. Coupled-two interconnects driven by CMOS inverter.

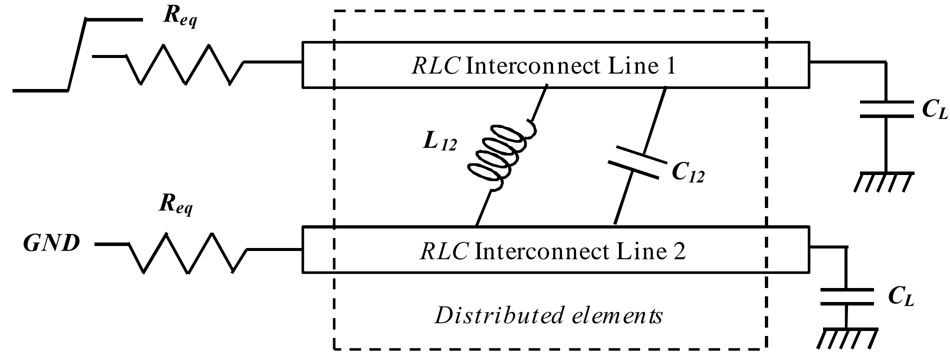


Figure 3.2. Coupled-two interconnects driven by resistive driver.

Table 3.1 Interconnect parasitics

Line resistance R **(kΩ/m)**	**Line inductance** L **(μH/m)**	**Mutual inductance** L_{12} **(μH/m)**	**Line capacitance** C **(pF/m)**	**Coupling capacitance** C_{12} **(pF/m)**
150	1.645	1.484	15.11	98.59

The transient response comparison between CMOS driver and resistive driver for functional, dynamic in-phase, dynamic out-phase crosstalk conditions are shown in Figures 3.3, 3.4 and 3.5, respectively. A large deviation in propagation delay, peak voltage, and its timing instances can be observed from the figures. For instance, the percentage error while comparing the worst-case propagation delay during the dynamic out-phase switching is about 68% and peak voltage during the functional crosstalk switching is about 53%. This corroborates the earlier observations in [35], [36], and [42], that the resistive driver model presents a pessimistic view on the performance analysis of on-chip interconnects.

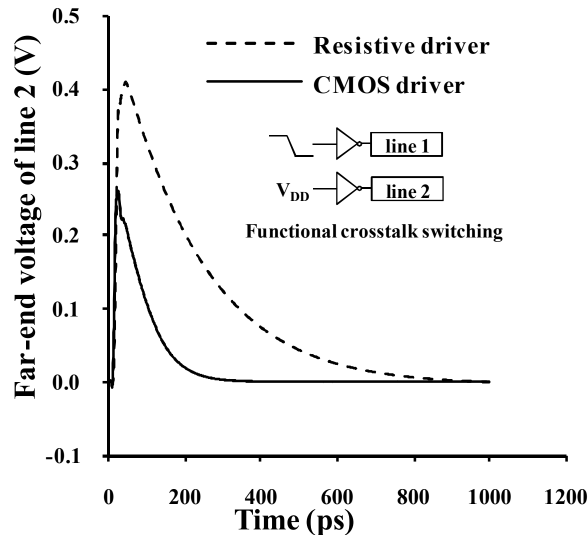


Figure 3.3. Transient response comparison during the functional crosstalk.

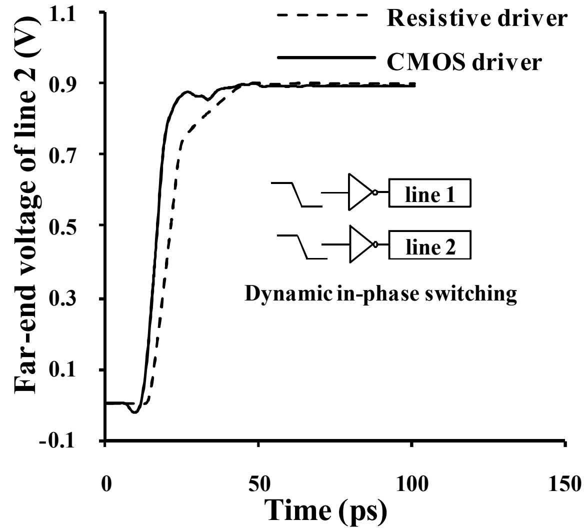


Figure 3.4. Transient response comparison during the dynamic in-phase crosstalk.

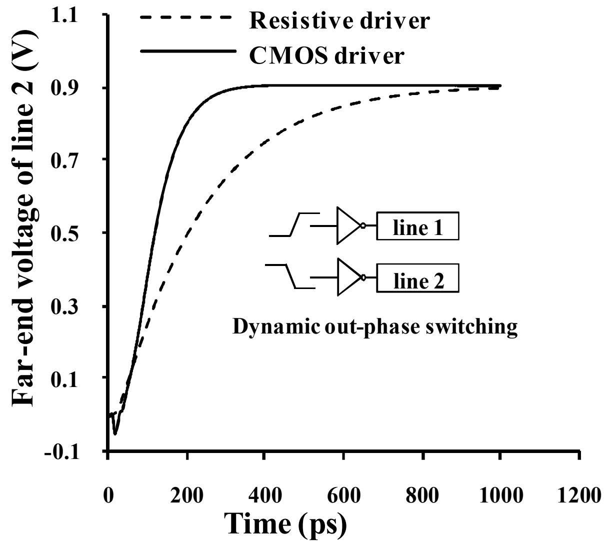


Figure 3.5. Transient response comparison during the dynamic out-phase crosstalk switching.

3.3 FDTD Model of CMOS Gate-driven Cu Interconnects

The FDTD technique is used to model the coupled distributed *RLC* interconnect lines [39]. The interconnect lines are driven by the CMOS inverter and terminated by a capacitive load. The short-channel transistors in the CMOS driver are represented by n-th power law model that includes the velocity saturation effect and finite drain conductance parameter [120].

3.3.1 FDTD Model of Interconnects

The structure of CMOS gate driven coupled Cu interconnect lines is shown in Figure 3.6, where R_1, R_2 are the line resistances, L_1, L_2 are the line inductances, C_1, C_2 are the line capacitances, and C_{L1}, C_{L2} are the load capacitances of line 1 and line 2, respectively. All these values are mentioned in p.u.l. C_{12} and L_{12} are the p.u.l. coupling capacitance and mutual inductance, respectively. The position along the interconnect line, and time are denoted as z and t, respectively.

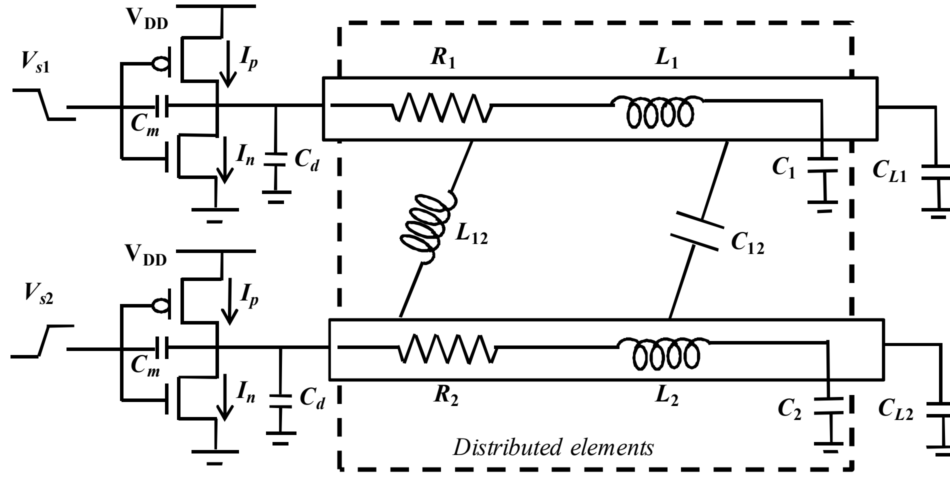


Figure 3.6. Coupled-two interconnect lines driven by CMOS inverter.

For uniform coupled-two transmission lines, the telegrapher's equations in the transverse electro-magnetic (TEM) mode are

$$\frac{\partial}{\partial z}V_1(z,t)+L_1\frac{\partial}{\partial t}I_1(z,t)+L_{12}\frac{\partial}{\partial t}I_2(z,t)+R_1I_1(z,t)=0 \tag{3.2a}$$

$$\frac{\partial}{\partial z}V_2(z,t)+L_2\frac{\partial}{\partial t}I_2(z,t)+L_{12}\frac{\partial}{\partial t}I_1(z,t)+R_2I_2(z,t)=0 \tag{3.2b}$$

$$\frac{\partial}{\partial z}I_1(z,t)+(C_1+C_{12})\frac{\partial}{\partial t}V_1(z,t)-C_{12}\frac{\partial}{\partial t}V_2(z,t)=0 \tag{3.2c}$$

$$\frac{\partial}{\partial z}I_2(z,t)+(C_2+C_{12})\frac{\partial}{\partial t}V_2(z,t)-C_{12}\frac{\partial}{\partial t}V_1(z,t)=0 \tag{3.2d}$$

Equations (3.2a)-(3.2d) can be represented in the matrix form as

$$\frac{d}{dz}\boldsymbol{V}(z,t)+\boldsymbol{RI}(z,t)+\boldsymbol{L}\frac{d}{dt}\boldsymbol{I}(z,t)=0 \tag{3.2e}$$

$$\frac{d}{dz}\boldsymbol{I}(z,t)+\frac{d}{dt}\boldsymbol{C}\boldsymbol{V}(z,t)=0 \tag{3.2f}$$

where $\boldsymbol{V}$ and $\boldsymbol{I}$ are 2×1 column vectors of line voltages and currents, respectively. The line parasitic elements are obtained in 2×2 per unit length matrix form *i.e.*,

$$\boldsymbol{V}=\begin{bmatrix}V_1\\V_2\end{bmatrix},\ \boldsymbol{I}=\begin{bmatrix}I_1\\I_2\end{bmatrix},\boldsymbol{R}=\begin{bmatrix}R_1 & 0\\0 & R_2\end{bmatrix},\boldsymbol{L}=\begin{bmatrix}L_1 & L_{12}\\L_{12} & L_2\end{bmatrix}\text{and } \boldsymbol{C}=\begin{bmatrix}C_1+C_{12} & -C_{12}\\-C_{12} & C_2+C_{12}\end{bmatrix}$$

Central difference approximation is used to analyze the first-order differential equations (3.2e) and (3.2f). Using the FDTD method, the analysis of telegrapher's equations has shown better accuracy if the voltage and current points are chosen as alternate in space location and separated by one-half of the position discretization, *i.e.*, $\Delta z/2$. In the same manner, the solution time for $\boldsymbol{V}$ and $\boldsymbol{I}$ should also be separated by $\Delta t/2$ as shown in Figure 3.7.

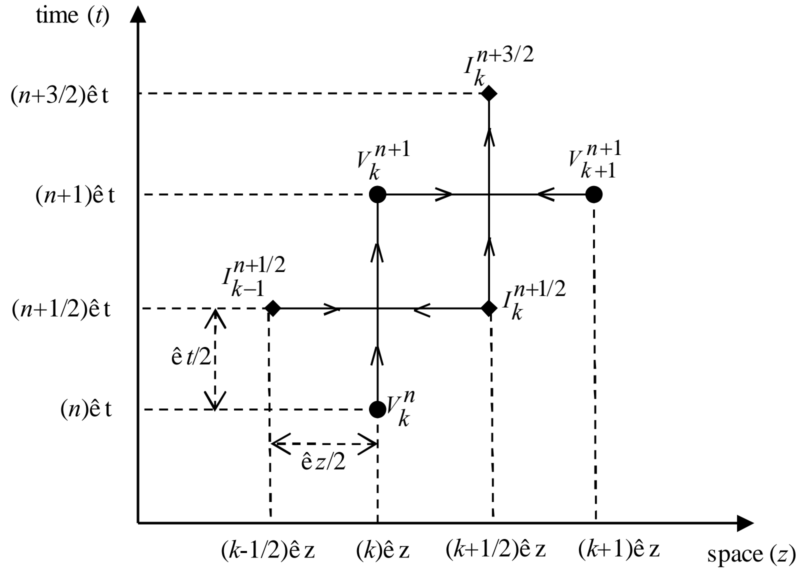


Figure 3.7. The relation between spatial and time discretization to achieve second order accuracy.

The interconnect line of length, l is driven by a CMOS inverter at $z = 0$ and terminated by a capacitive load at $z = l$. The line is discretized into Nz uniform segments of length $\Delta z = l/Nz$. The voltage and current solution points are discretized along the line as shown in Figure 3.8.

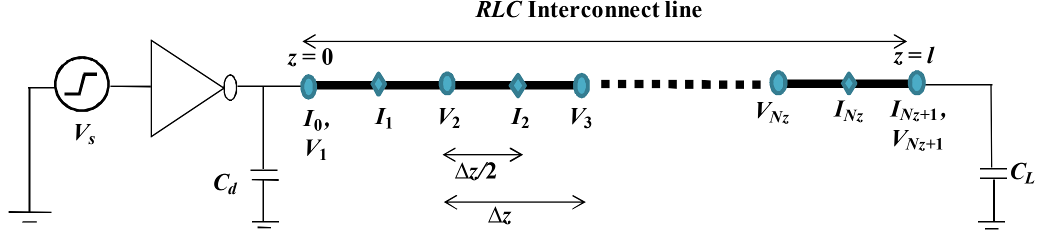


Figure 3.8. Illustration of space discretization of line for FDTD implementation.

Applying finite difference approximations to (3.2e) and (3.2f) results in

$$\frac{\boldsymbol{V}_{k+1}^{n+1}-\boldsymbol{V}_{k}^{n+1}}{\Delta z}+\boldsymbol{L}\frac{\boldsymbol{I}_{k}^{n+3/2}-\boldsymbol{I}_{k}^{n+1/2}}{\Delta t}+\boldsymbol{R}\frac{\boldsymbol{I}_{k}^{n+3/2}+\boldsymbol{I}_{k}^{n+1/2}}{2}=0 \tag{3.3a}$$

$$\boldsymbol{I}_{k}^{n+3/2}=\boldsymbol{BDI}_{k}^{n+1/2}+\boldsymbol{B}\left(\boldsymbol{V}_{k}^{n+1}-\boldsymbol{V}_{k+1}^{n+1}\right) \quad \text{for } k=1, 2, \cdots\cdots, Nz \tag{3.3b}$$

where $\boldsymbol{B}=\left[\frac{\Delta z}{\Delta t}\boldsymbol{L}+\frac{\Delta z}{2}\boldsymbol{R}\right]^{-1}$, $\boldsymbol{D}=\left[\frac{\Delta z}{\Delta t}\boldsymbol{L}-\frac{\Delta z}{2}\boldsymbol{R}\right]$

$$\frac{\boldsymbol{I}_{k}^{n+1/2}-\boldsymbol{I}_{k-1}^{n+1/2}}{\Delta z}+\boldsymbol{C}\frac{\boldsymbol{V}_{k}^{n+1}-\boldsymbol{V}_{k}^{n}}{\Delta t}=0 \tag{3.4a}$$

$$\boldsymbol{V}_{k}^{n+1}=\boldsymbol{V}_{k}^{n}+\boldsymbol{A}\left(\boldsymbol{I}_{k-1}^{n+1/2}-\boldsymbol{I}_{k}^{n+1/2}\right) \text{for } k=2, 3, \cdots\cdots, Nz \tag{3.4b}$$

where $\boldsymbol{A}=\left[\frac{\Delta z}{\Delta t}\boldsymbol{C}\right]^{-1}$

Here, it can be noticed that the calculations are interleaved in both space and time. For example, in (3.4b) the new value of $\boldsymbol{V}$ is calculated from the previous value of $\boldsymbol{V}$ and the most recent values of $\boldsymbol{I}$. For integer values of i and j, $\boldsymbol{V}$ and $\boldsymbol{I}$ vectors are denoted as

$$\boldsymbol{V}_{i}^{j}=\boldsymbol{V}\left[i\Delta z, j\Delta t\right], \quad \boldsymbol{I}_{i}^{j}=\boldsymbol{I}\left[(i+1/2)\Delta z, j\Delta t\right] \tag{3.5}$$

3.3.2 Incorporation of Boundary Constraints

The voltage and current points at the near end terminal are represented by $\boldsymbol{V}_1$ and $\boldsymbol{I}_0$, respectively. As indicated in Figure 3.8, it is observed that to apply the

boundary conditions in (3.4b), ê z is replaced by $\Delta z/2$. Therefore, at $k = 1$ equation (3.4b) becomes

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{V}_1^{n} + 2\boldsymbol{A}\left[\boldsymbol{I}_0^{n+1/2} - \boldsymbol{I}_1^{n+1/2}\right] \tag{3.6a}$$

The source current $\boldsymbol{I}_0$ at $(n+(1/2))$ time interval is obtained by averaging the source current at (n) and $(n+1)$ time intervals, then the equation (3.6a) becomes

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{V}_1^{n} + 2\boldsymbol{A}\left[\frac{\boldsymbol{I}_0^{n+1}+\boldsymbol{I}_0^{n}}{2} - \boldsymbol{I}_1^{n+1/2}\right] \tag{3.6b}$$

here, $\boldsymbol{I}_0$ is the CMOS driver current. Applying Kirchhoff's current law at near-end terminal, $\boldsymbol{I}_0$ can be expressed as

$$\boldsymbol{I}_0 = \boldsymbol{C}_m\left[\frac{d(\boldsymbol{V}_S-\boldsymbol{V}_1)}{dt}\right] + \boldsymbol{I}_p - \boldsymbol{I}_n - \boldsymbol{C}_d\frac{d\boldsymbol{V}_1}{dt} \tag{3.7}$$

where $\boldsymbol{C_m}$ is the drain to gate coupling capacitance, $\boldsymbol{C_d}$ is the drain diffusion capacitance of CMOS inverter, $\boldsymbol{I_p}$ and $\boldsymbol{I_n}$ are the PMOS and NMOS currents, respectively. Using the n-th power law model, MOS currents are represented by [120]

$$\boldsymbol{I_p} = \begin{cases} 0 & V_S \geq V_{DD} - \left|V_{Tp}\right| \quad (cutoff) \\ \boldsymbol{I}_{DSATp}\left(1+\sigma_p(V_{DD}-\boldsymbol{V}_1)\right)\left(2-\dfrac{V_{DD}-\boldsymbol{V}_1}{\boldsymbol{V}_{DSATp}}\right)\dfrac{V_{DD}-\boldsymbol{V}_1}{\boldsymbol{V}_{DSATp}} & \boldsymbol{V}_1 > V_{DD} - \boldsymbol{V}_{DSATp} \quad (lin) \\ \boldsymbol{I}_{DSATp}\left(1+\sigma_p(V_{DD}-\boldsymbol{V}_1)\right) & \boldsymbol{V}_1 \leq V_{DD} - \boldsymbol{V}_{DSATp} \quad (sat) \end{cases} \tag{3.8a}$$

$$\boldsymbol{I}_n = \begin{cases} 0 & V_S \leq V_{Tn} \quad (cutoff) \\ \boldsymbol{I}_{DSATn}\left(1+\sigma_n\boldsymbol{V}_1\right)\left(2-\dfrac{\boldsymbol{V}_1}{\boldsymbol{V}_{DSATn}}\right)\dfrac{\boldsymbol{V}_1}{\boldsymbol{V}_{DSATn}} & \boldsymbol{V}_1 < \boldsymbol{V}_{DSATn} \quad (lin) \\ \boldsymbol{I}_{DSATn}\left(1+\sigma_n\boldsymbol{V}_1\right) & \boldsymbol{V}_1 \geq \boldsymbol{V}_{DSATn} \quad (sat) \end{cases} \tag{3.8b}$$

where V_{DSATp}, V_{DSATn} are the drain saturation voltages; I_{DSATp}, I_{DSATn} are drain saturation currents; V_{Tp}, V_{Tn} are the threshold voltages under no body bias condition; σ_p, σ_n are the finite drain conductance parameters of PMOS and NMOS, respectively. The drain saturation voltage of PMOS and NMOS are obtained from

$$\boldsymbol{V}_{DSATp} = K_p \left(V_{DD} - \boldsymbol{V}_S - \left| V_{Tp} \right| \right)^{m_p} \tag{3.8c}$$

$$\boldsymbol{V}_{DSATn} = K_n \left(\boldsymbol{V}_S - V_{Tn} \right)^{m_n} \tag{3.8d}$$

The drain saturation current of PMOS and NMOS are obtained from

$$\boldsymbol{I}_{DSATp} = \frac{W_p}{L_{eff}} B_p \left(V_{DD} - \boldsymbol{V}_S - \left| V_{Tp} \right| \right)^{s_p} \tag{3.8e}$$

$$\boldsymbol{I}_{DSATn} = \frac{W_n}{L_{eff}} B_n \left(\boldsymbol{V}_S - V_{Tn} \right)^{s_n} \tag{3.8f}$$

The parameters B_p, s_p and B_n, s_n control the saturation region while K_p, m_p and K_n, m_n control the linear region characteristics of PMOS and NMOS, respectively. The width of PMOS and NMOS is represented by W_p and W_n, respectively, L_{eff} is an effective channel length. The model parameters are computed from the method proposed in [120], and the values are listed in Table 3.2.

Table 3.2 Model parameters for 32 nm node

Parameter	PMOS	NMOS
m	0.087	0.211
s	1.07	0.915
B	0.801×10^{-5}	3.55×10^{-5}
K	0.316	0.369
σ	3.11	0.867
V_T	0.366	0.36

In order to use the equation (3.7) in (3.6b), the source current $\boldsymbol{I}_0$ must be represented in discretized form as:

$$\boldsymbol{I}_0^{n+1} = C_m \frac{\boldsymbol{V}_S^{n+1} - \boldsymbol{V}_S^n}{\Delta t} + \boldsymbol{I}_p^{n+1} - \boldsymbol{I}_n^{n+1} - (\boldsymbol{C}_m + \boldsymbol{C}_d) \frac{\boldsymbol{V}_1^{n+1} - \boldsymbol{V}_1^n}{\Delta t} \tag{3.9}$$

Using (3.9) and (3.6b)

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{V}_1^n + \boldsymbol{EA}\left[\frac{\boldsymbol{C}_m}{\Delta t} (\boldsymbol{V}_S^{n+1} - \boldsymbol{V}_S^n) + \boldsymbol{I}_0^n \right] - 2\boldsymbol{EAI}_1^{n+1/2} + \boldsymbol{EA}\left(\boldsymbol{I}_p^{n+1} - \boldsymbol{I}_n^{n+1} \right) \tag{3.10}$$

where $\boldsymbol{E} = \left[\boldsymbol{U} + \frac{\boldsymbol{A}}{\Delta t} (\boldsymbol{C_m} + \boldsymbol{C_d}) \right]^{-1}$ and $\boldsymbol{U}$ is the 2×2 identity matrix.

The objective is to derive the voltage expression at k = Nz+1. At k = Nz+1 the equation (3.4b) becomes

$$\boldsymbol{V}_{Nz+1}^{n+1} = \boldsymbol{V}_{Nz+1}^{n} + 2\boldsymbol{A}\left(\boldsymbol{I}_{Nz}^{n+1/2} - \frac{\boldsymbol{I}_{Nz+1}^{n+1} + \boldsymbol{I}_{Nz+1}^{n}}{2} \right) \tag{3.11}$$

The output current ($\boldsymbol{I}_{Nz+1}$) of the capacitive load is defined as

$$\boldsymbol{I}_{Nz+1} = \boldsymbol{C}_L \frac{d}{dt} \boldsymbol{V}_{Nz+1} \tag{3.12a}$$

where $\boldsymbol{C}_L$ is the load capacitance, the load current $\boldsymbol{I}_{Nz+1}$ can be discretized as

$$\boldsymbol{I}_{Nz+1}^{n+1} = \boldsymbol{C}_L \frac{\left(\boldsymbol{V}_{Nz+1}^{n+1} - \boldsymbol{V}_{Nz+1}^{n} \right)}{\Delta t} \tag{3.12b}$$

Using (3.11) and (3.12b)

$$\boldsymbol{V}_{Nz+1}^{n+1} = \boldsymbol{V}_{Nz+1}^{n} + 2\boldsymbol{F}\boldsymbol{A}\left[\boldsymbol{I}_{Nz}^{n+1/2} - \frac{\boldsymbol{I}_{Nz+1}^{n}}{2} \right] \tag{3.13}$$

where $\boldsymbol{F} = \left[\boldsymbol{U} + \frac{\boldsymbol{A}\boldsymbol{C}_L}{\Delta t} \right]^{-1}$

These equations are evaluated in a bootstrapping fashion. Initially, the voltages along the line are evaluated for a specific time from equations (3.10), (3.4b) and (3.13) in terms of the previous values of voltage and current values. Thereafter, the currents are evaluated from (3.3b) in terms of these voltage and previous current values. The analysis starts with a quiescent line having zero voltage and current values. Nevertheless, the FDTD method provides an exact solution if the CFL stability condition, $\Delta t \leq \Delta z/v$, is satisfied. This implies to a condition that the time step must not be greater than the propagation time over each cell [39]. If this condition is translated to a per cell basis, the relation becomes $\Delta t < \sqrt{LC}$ referred as causality condition [118]. However, since the boundary conditions (3.10) and (3.13) have the explicit forms derived from the implicit equations, there is no stability problem at the two boundaries. Therefore, the stability of the system is only determined by the transmission line portion of the system. For a coupled-multiple interconnect lines, these equations remain valid except for the few changes in the matrix notation. For instance, in a coupled-three interconnect line system the parasitics of interconnect line, CMOS driver and load capacitance elements become 3×3 matrices, and the voltage and current values are calculated in a 3×1 column vector form.

3.4 Validation of the Model

The proposed model is validated by comparing it with HSPICE simulations. The coupled-two interconnect line structure is considered for the validation of the model as shown in Figure 3.1. Using the simulation setup described in Section 3.2, the parasitic matrices are obtained as

$$R = \begin{bmatrix} 150 & 0 \\ 0 & 150 \end{bmatrix} \frac{k\Omega}{m},\ L = \begin{bmatrix} 1.645 & 1.484 \\ 1.484 & 1.645 \end{bmatrix} \frac{\mu H}{m},\ \text{and}\ C = \begin{bmatrix} 113.7 & -98.59 \\ -98.59 & 113.7 \end{bmatrix} \frac{pF}{m}$$

Using the line parasitic values, the mode velocities for a lossless case are calculated as $v_{m1} = 1.4543\times10^{8}$ m/s and $v_{m2} = 1.7105\times10^{8}$ m/s. The space discretization (Δz) is less than 4.57×10^{-4} m while considering a break frequency of 3.18×10^{10} Hz and smaller mode velocity v_{m1}. Using the value of Δz and CFL stability condition, the time discretization (Δt) is obtained to be less than 2.67×10^{-12} s, for a larger mode velocity, v_{m2} that ensures a stable system [39]. The grid size is calculated using $_{\min}$/(10-20), where $_{\min}$ is the smallest electromagnetic wavelength.

In the coupled-two line system, line 1 and line 2 are considered as aggressor and victim lines, respectively. The propagation delay, peak voltage, and peak voltage timing are analyzed on victim line 2 [122]. The input signal rise and fall transition times are chosen as 10 ps. Using the simulation setup described in Section 3.2, transient waveforms are compared at the far end terminal on the victim line 2.

The crosstalk effects are studied for two different cases. First case considers the functional crosstalk, which is analyzed by switching the aggressor and keeping the victim line in quiescent mode. Dynamic crosstalk effect is considered in the second case, by simultaneously exciting the aggressor and victim lines with both in-phase and out-phase manner. Figures 3.9, 3.10 and 3.11 show the transient waveform comparison of the proposed model, HSPICE simulations, and the model suggested in [42] of coupled-two interconnect lines. The waveforms generated using the proposed model closely matches with HSPICE results. The model of [42] is not accurate under the conditions when the technology is scaled down, due to the ignorance of σ. Therefore, using [42], the estimated current is high, that results in rise (or fall) of the output signal quickly as observed in Figures 3.10 and 3.11.

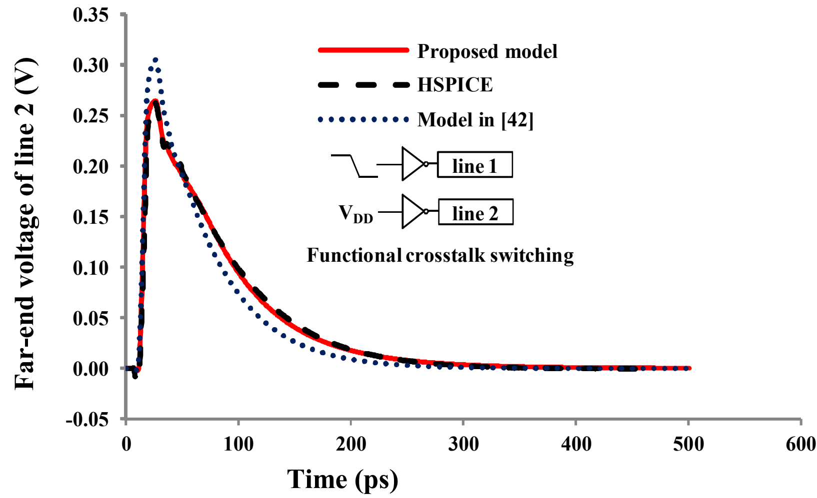


Figure 3.9. Transient response of quiescent line 2 during the functional crosstalk switching.

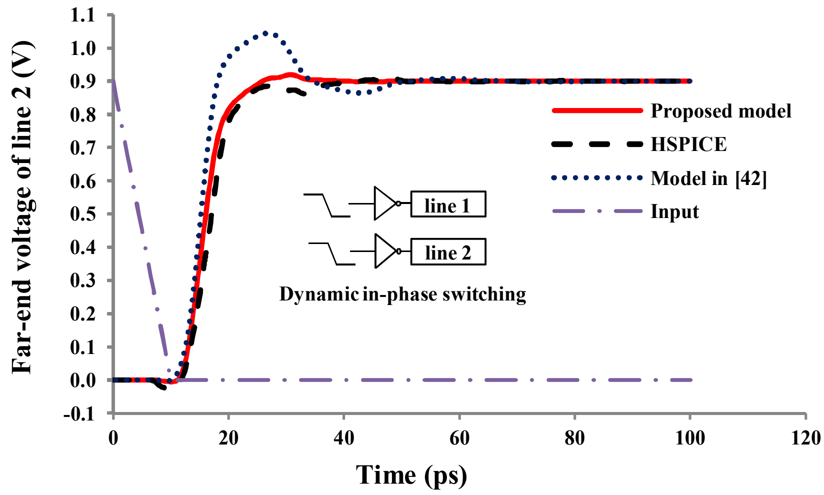


Figure 3.10. Transient response of line 2 during the dynamic in-phase crosstalk switching.

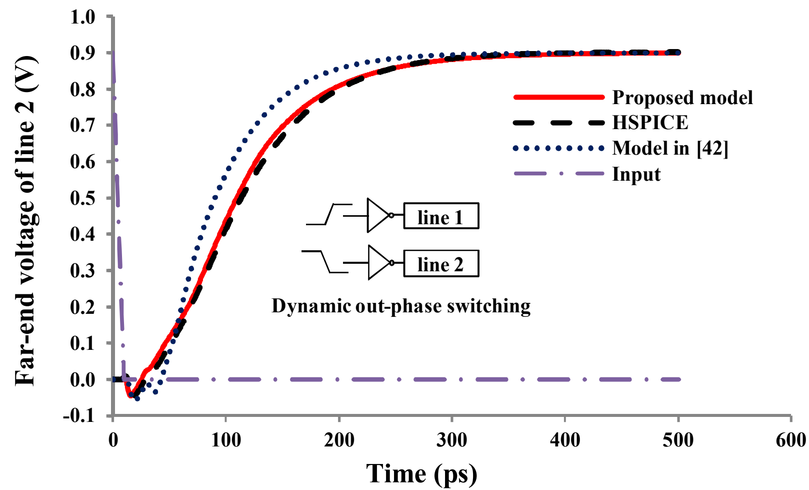


Figure 3.11. Transient response of line 2 during the dynamic out-phase crosstalk switching.

Table 3.3 presents the computational error involved in predicting the crosstalk induced peak voltage on quiescent victim line 2, using the proposed model and the model suggested in [42], with respect to HSPICE simulations. The computational error for the crosstalk induced peak voltage timing is shown in Table 3.4. For evaluating the robustness of the model, the analysis is performed at different input transition times. It is observed that using the proposed model the average error in estimation of crosstalk peak voltage is only 1.7%, whereas, using [42] the average error can be as large as 16%. The peak voltage timing is also well predicted by the proposed model. The average error using proposed model and [42] is 1.5% and 9.7%, respectively.

Table 3.3 Computational error involved in peak noise voltage

Input transition time (T_r) (ps)	**Peak voltage**				
	HSPICE (V)	**Proposed model (V)**	**Li *et al.* model [42] (V)**	**% error Proposed model**	**% error [42]**
10	0.26	0.26	0.30	0.00	-15.38
30	0.24	0.25	0.29	-4.17	-20.83
50	0.22	0.23	0.27	-4.55	-22.73
70	0.21	0.21	0.24	0.00	-14.29
90	0.20	0.20	0.22	0.00	-10.00

Table 3.4 Computational error involved in peak voltage timing

Input transition time (T_r) (ps)	**Peak voltage timing**				
	HSPICE (ps)	**Proposed model (ps)**	**Li *et al.* model [42] (ps)**	**% error Propoposed model**	**% error [42]**
10	25.74	25.90	26.40	-0.62	-2.56
30	40.89	39.30	28.80	3.89	29.57
50	60.39	59.10	58.40	2.14	3.30
70	79.39	78.80	75.70	0.74	4.65
90	98.89	98.70	90.10	0.19	8.89

The propagation delay comparison during the in-phase and out-phase transition on victim line 2 is shown in Figure 3.12 for different input transition timings. The propagation delay during the out-phase transition is observed to be high due to Miller capacitance effect. It is observed that the proposed model accurately

predicts the propagation delay in both in-phase and out-phase transitions. The average error using the proposed model is found to be 4% and 2% during the in-phase and out-phase switching, respectively, whereas the average error is 16% and 19% in case of the model suggested in [42]. The size of the repeater is considered as 100 times to its length. However, in common practice to use multiple repeaters of varying sizes while driving long interconnects. The effect of repeater size variation can be incorporated in the proposed model by using different model parameters that are calculated using [120].

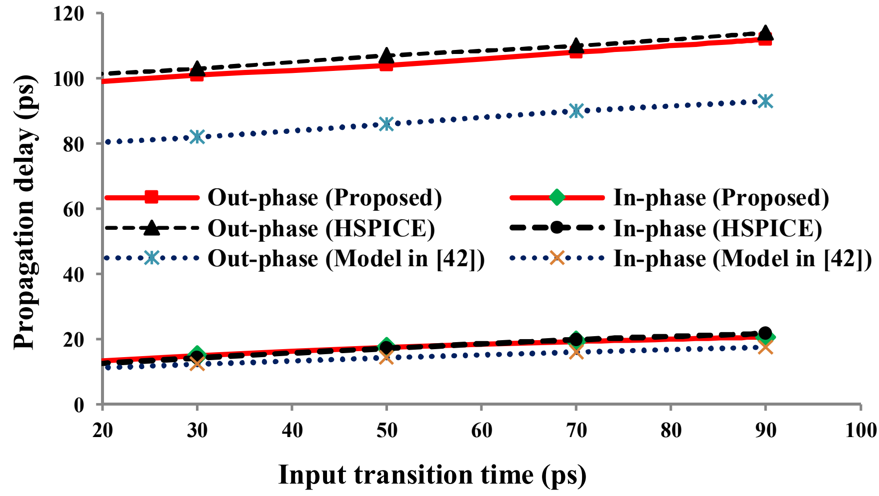


Figure 3.12. Variation of propagation delay with respect to transition time.

3.5 Extensions and Observations

The previous section demonstrated that the proposed model can accurately analyze the coupled-two interconnects. In this section, the interconnect line model is extended to three lines as shown in Figure 3.13 and is validated with HSPICE simulations. The input transition time and the load capacitance are chosen as 10 ps and 2 fF, respectively. Using the dimensions described in Section 3.2, the following interconnect parameters are used in the crosstalk analysis of coupled-three lines. The coupling capacitance between line 1 and line 3 can be safely neglected because of large spacing distance [59].

$$R = \begin{bmatrix} 150 & 0 & 0 \\ 0 & 150 & 0 \\ 0 & 0 & 150 \end{bmatrix} \frac{k\Omega}{m}, \quad L = \begin{bmatrix} 1.645 & 1.484 & 1.264 \\ 1.484 & 1.645 & 1.484 \\ 1.264 & 1.484 & 1.645 \end{bmatrix} \frac{\mu H}{m}, \text{ and}$$

$$C = \begin{bmatrix} 113.7 & -98.59 & 0 \\ -98.59 & 212.29 & -98.59 \\ 0 & -98.59 & 113.7 \end{bmatrix} \frac{pF}{m}$$

The authors in [42], considered the diagonal elements within the capacitance matrix to be equal for a symmetrical coupled-multiple interconnect structure. However, the diagonal elements in the symmetric capacitance matrix cannot be equal. For instance, in a coupled-three line system, the total capacitance of line 2 is higher than line 1 and line 3. These effects have been considered into account in the present model.

The transient response comparison between the proposed model, HSPICE, and the model in [42] are shown in Figure 3.14. Considering lines 1 and 3 as aggressors and line 2 as victim, different input switching cases are analyzed, and the transient responses are compared on victim line 2. It is observed that for all cases of input switching, the proposed model matches accurately with the simulation results. In addition to that, the proposed model is time efficient than the HSPICE.

Table 3.5 provides the computational error involved in the estimation of crosstalk induced propagation delay on victim line 2 with respect to HSPICE. Using the proposed model, the average error is observed to be less than 4%, whereas, using [42] the average error is as large as 24%. It is also observed that the crosstalk induced delay increases with the increasing case mode as shown in Table 3.5. This fact can be realized by the effect of Miller capacitance that highly influences the signal propagation when two wires (aggressor and victim) transits in opposite direction. Consequently, for a victim line 2, case-5 transition must be the worst-case delay in high-speed on-chip interconnects.

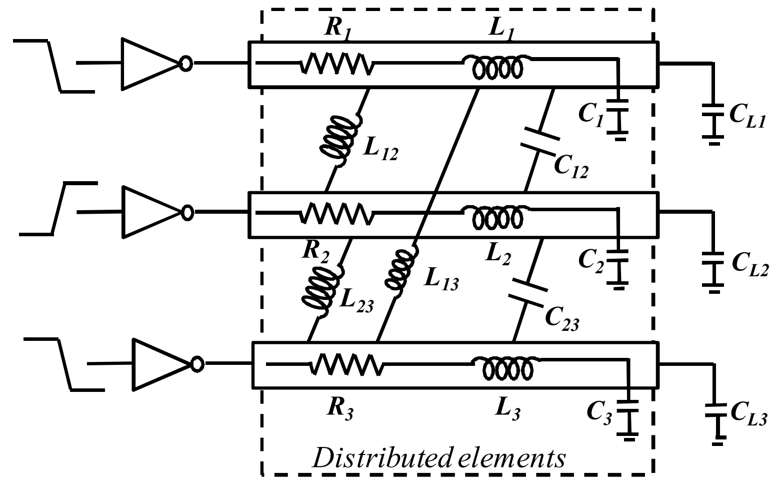
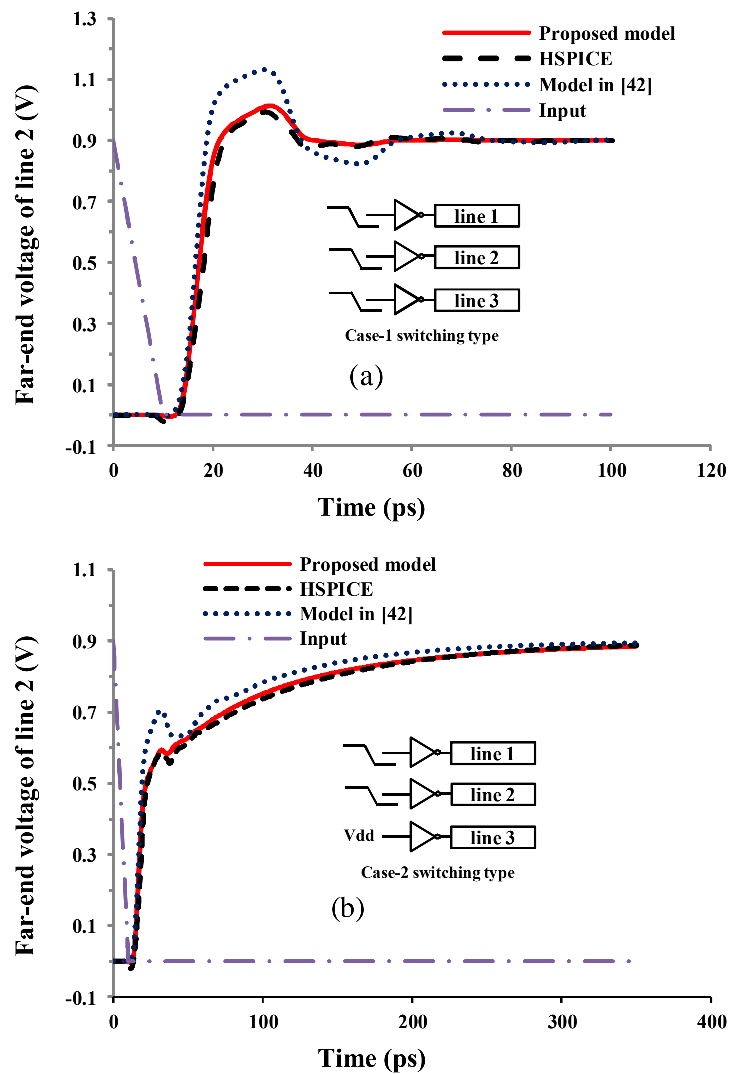
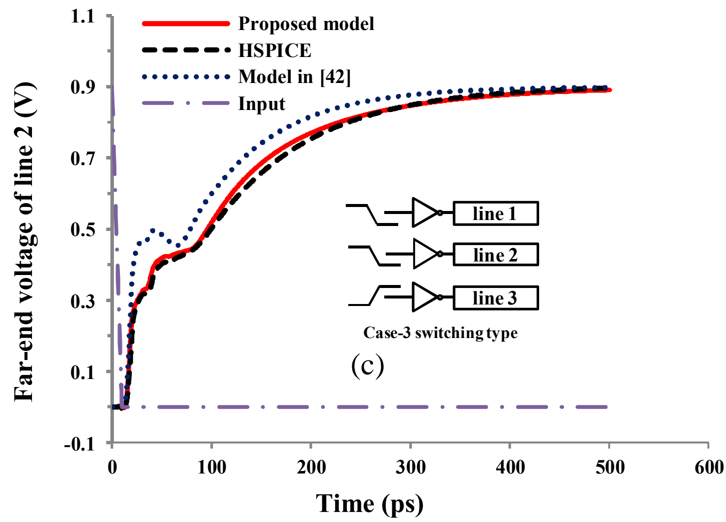
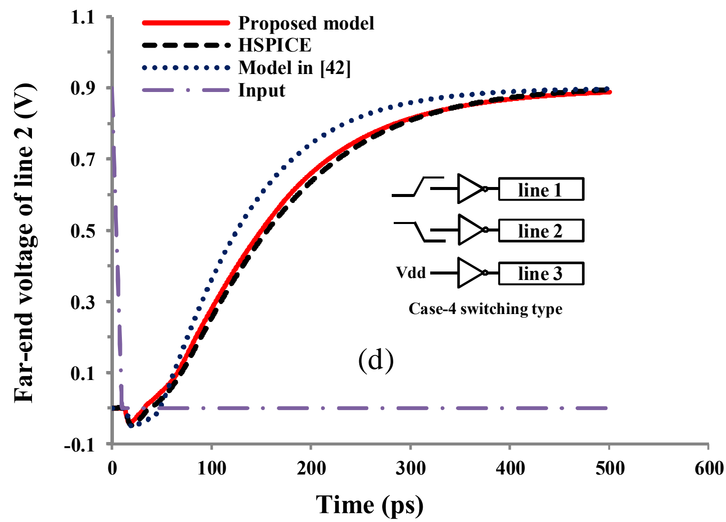


Figure 3.13. Coupled-three interconnect lines driven by CMOS inverter.







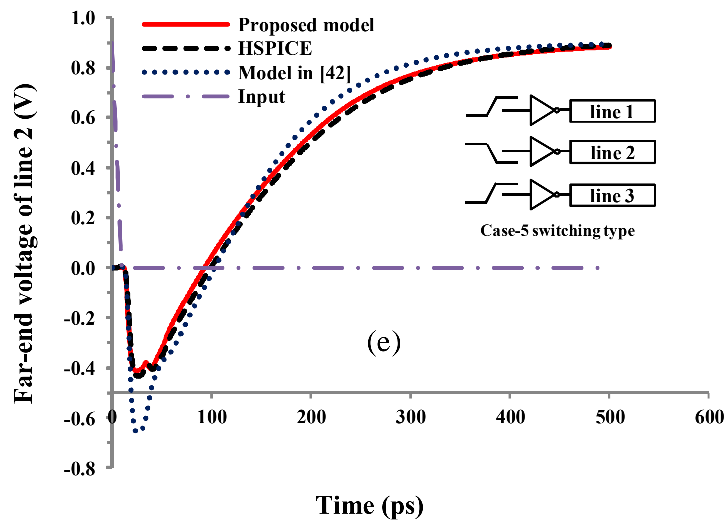


Figure 3.14. Transient response comparison on victim line 2 (a) case-1, (b) case-2, (c) case-3, (d) case-4, and (e) case-5 input switching modes.

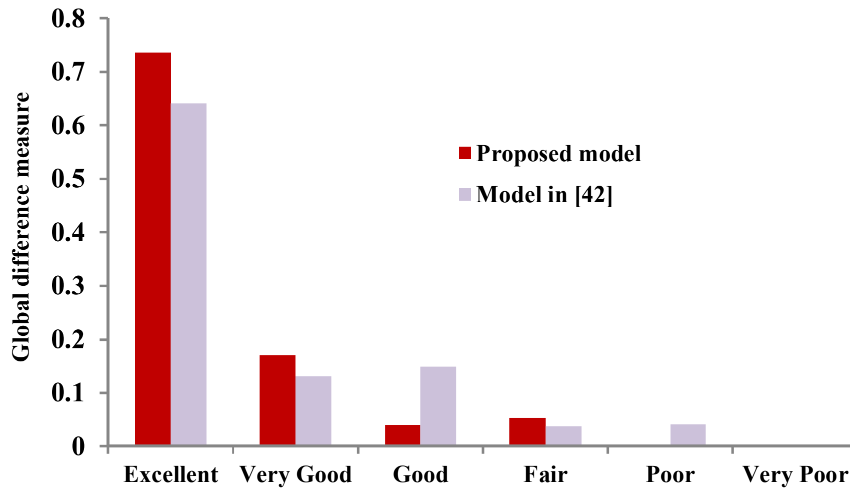


Figure 3.15. Histogram form the datasets of Figure 3.14(a) using FSV tool.

Table 3.5 Computational error involved for propagation delay on victim line2

Input switching modes				**Propagation delay on victim line 2**				
Case-mode	**Line 1**	**Line 2**	**Line 3**	**HSPICE (ps)**	**Proposed model (ps)**	**Li *et al.* model [42] (ps)**	**% error Proposed model**	**% error [42]**
Case-1	1 0	1 0	1 0	12.7	12.1	11.5	4.7	9.4
Case-2	1 0	1 0	Vdd	15.7	15	13.8	4.4	12.1
Case-3	1 0	1 0	0 1	79.6	78.1	20.9	1.8	73.7
Case-4	0 1	1 0	Vdd	138.4	133	111	3.9	19.8
Case-5	0 1	1 0	0 1	181.4	174.9	164.7	3.5	9.2

In order to make a simple decision about the quality of the comparison, the datasets of Figure 3.14(a) are converted into natural language descriptor (excellent, very good, good, fair, poor, and very poor). Using the feature selective validation (FSV) tool [123]-[125], the histogram of the global difference measure (GDM) is generated and shown in Figure 3.15. The results convincingly demonstrate that the proposed model excellently matches with HSPICE simulations in comparison to that of [42]. Moreover, the proposed is also validated with the post-layout simulator. The post-layout simulations and proposed model results are compared using the 32 nm

technology and shown in Figure 3.16. It can be observed that the proposed model results are close to the post-layout simulation results.

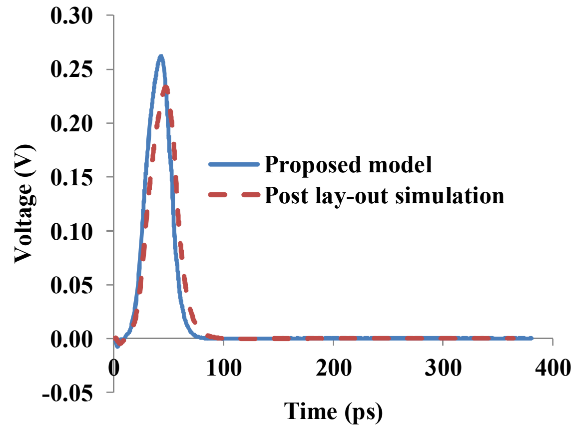


Figure 3.16. Transient response comparison between proposed model and post lay-out simulations.

3.6 Summary

This chapter presented an accurate model to analyze the crosstalk effects in CMOS gate-driven coupled-multiple on-chip interconnects. CMOS driver is analyzed using the n-th power law model and coupled RLC interconnect line has been modeled using the FDTD method. Crosstalk effects are analyzed in coupled two and three interconnect lines. It has been observed that the results are in good agreement with HSPICE simulations. The proposed model can be extended to coupled n-lines and the voltage signal at any particular point on the interconnect line can be quickly and accurately obtained with minimum computational effort. Moreover, it is observed that representing the non-linear CMOS driver with a resistive driver gives erroneous results and no longer useful for accurate estimation of crosstalk induced performance parameters. Furthermore, the existing CMOS gate-driven RLC interconnect models are also unable to estimate the performance parameters, especially at lower technology nodes. The proposed model meets these requirements very well, and is therefore, extremely useful in evaluating the signal integrity issues of next-generation on-chip interconnects.

Chapter 4

FDTD Model for Crosstalk Analysis of Multiwall Carbon Nanotube (MWCNT) Interconnects

4.1. Introduction

The conventional interconnect copper material is unable to meet the requirements of future technology needs, since it suffers from low reliability with down scaling of interconnect dimensions. Moreover, the resistivity of copper increases, due to electron-surface scattering and grain-boundary scattering with smaller dimensions. Therefore, researchers are forced to find an alternative material for global VLSI interconnects. Carbon nanotubes have been proposed to be one of the potential candidates for VLSI interconnects due to their unique physical properties, such as extraordinary mobility, large mean free path, and high current carrying capability [88], [100], [126-131].

Carbon nanotubes can be classified into single-walled carbon nanotube (SWCNT) and multi-walled carbon nanotube (MWCNT) [132-135]. The promising interconnect solution for global interconnect lengths are MWCNTs due to their high current carrying capabilities than SWCNT bundles. Naeemi *et al.* observed that for longer interconnects, MWCNTs can have conductivities several times greater than SWCNT bundles [135]. Hence, many researchers consider the MWCNTs as a potential solution for global interconnect material. The experimental and theoretical investigations of MWCNTs as an interconnect material have been presented in [68] and [86], respectively.

The performance of an MWCNT interconnect line is generally evaluated by means of an equivalent transmission line model. Li *et al.* proposed a multi-conductor transmission line (MTL) model to represent the MWCNT interconnect [26]. However, the analysis of MWCNT using the MTL model can be computationally expensive. For this reason, the equivalent single conductor (ESC) model was proposed in [86], [88], using the assumption that voltage at an arbitrary cross-section along MWCNT are the same, such that all nanotubes are connected in parallel at the both ends. The accuracy

of the ESC model has been verified by several researchers [87, 88]. They observed that the transient responses of ESC model and MTL model and are in good agreement.

The FDTD technique has been used widely to analyze the transmission lines due to their better accuracy [38]. However, incorporation of different boundary conditions in the FDTD models is a challenging task. Previously, Paul [39, 40] incorporated the boundary conditions to analyze the transmission lines for resistive driver and resistive load boundaries. However, these studies were focused only on copper interconnects and hence, not suitable for next generation graphene based nano interconnects. The quantum and contact resistances at the near-end and far-end terminals of a nano interconnect line results in complex boundary conditions. For the first time Liang *et al*. [21], proposed a crosstalk noise model for the analysis of MWCNT interconnects using FDTD technique. However, the authors represented the nonlinear CMOS driver by a resistive driver, thus limiting the accuracy of their model. Moreover, they did not validate their proposed model with respect to HSPICE. Therefore, a more accurate model is required that allows a better crosstalk induced performance estimation of MWCNT interconnects.

The fabrication technique of MWCNT bundles was reported in [63], using thermal chemical vapor deposition technique. The authors have demonstrated the feasibility of growing perfectly aligned carbon nanotube bundles. Recently, Wang *et al.* [136] fabricated the MWCNTs arrays by using microwave plasma chemical vapor deposition on Si substrate with inter-digital electrodes. This method is able to control the thickness of MWCNT arrays based on the growth time. Although, the controlled growth of MWCNTs with high CNT density is realizable, but, the researchers are still facing some challenges in terms of large imperfect metal-nanotube contact resistance, poor control on number of shells, chirality and orientation, higher growth temperature during the fabrication process. However, efforts are underway to fabricate MWCNTs for interconnect applications.

This chapter presents an accurate numerical model for comprehensive crosstalk analysis of coupled MWCNT interconnects based on FDTD method. Using this method, the voltage and current can be accurately estimated at any particular point on the interconnect line. Since the proposed model requires less number of

assumptions, the accuracy is very high. The non-linear CMOS driver effects are incorporated using the modified alpha power law model with suitable boundary conditions. Using the proposed FDTD method, the functional and dynamic crosstalk analysis is carried out. The results demonstrate that the proposed model has high accuracy that matches closely with the HSPICE results. In addition to this, the proposed model is highly time efficient than the HSPICE. Although, this chapter demonstrate the crosstalk effects on two coupled interconnect lines, but the model can be extended to *N*-lines.

The rest of the chapter is organized as follows: Section 4.2 describes the ESC model of an MWCNT. In Section 4.3, the FDTD method is developed for coupled MWCNT interconnect lines. Section 4.4 is devoted to the validation of proposed model for coupled-two lines. In Section 4.5, the sensitivity analysis is performed to evaluate the validity of the assumptions associated with the proposed model. Finally, Section 4.6 concludes this chapter.

4.2. Equivalent Single Conductor Model of the MWCNT Interconnect

This section presents an equivalent *RLC* model of an MWCNT interconnect line. Consider a horizontal MWCNT bundle interconnect line positioned over a ground plane at a distance, *H* and placed in a dielectric medium with dielectric constant, . The geometry of an MWCNT interconnect is shown in Figure 4.1. The coupling parasitics between the two MWCNT interconnects is shown in Figure 4.2, where s is the spacing between the interconnect lines, l_{12} and c_{12} represent the mutual inductance and coupling capacitance between the interconnect lines, respectively. The MWCNT interconnect consists of N number of tubes

$$N = 1 + \text{int}\left[\frac{(d_N - d_1)}{2\delta}\right] \tag{4.1}$$

where δ, d_1 and d_N represent inter-shell distance, innermost shell diameter and outermost shell diameter, respectively.

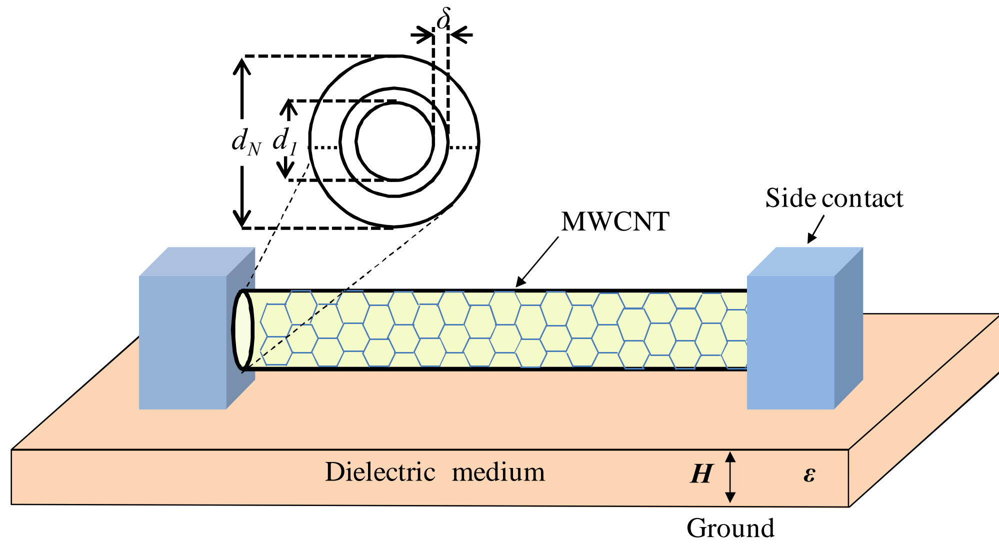


Figure 4.1. Geometry of an MWCNT interconnect above the ground plane.

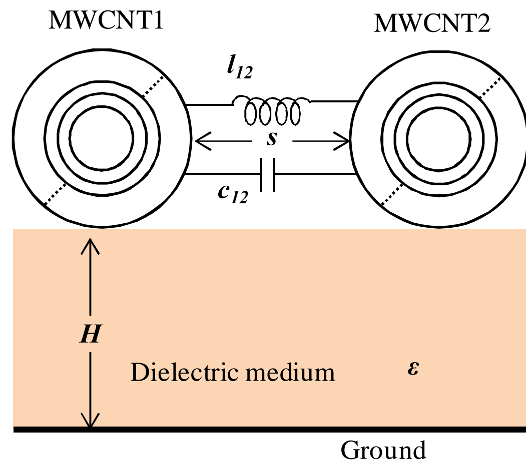


Figure 4.2. Cross-sectional view and coupling parasitics between MWCNTs.

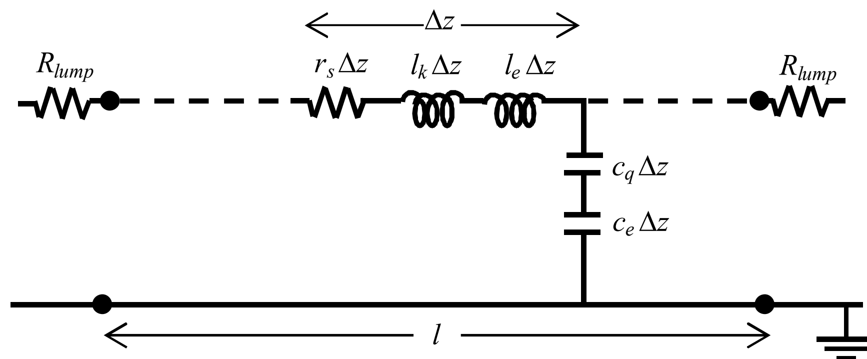


Figure 4.3. Electrical equivalent model of an MWCNT interconnect.

The MWCNT interconnect has been represented by an equivalent single conductor (ESC) model as shown in Figure 4.3 [86]. The *RLC* parasitics of an MWCNT interconnect are primarily dependent on the number of conducting channels. The number of conducting channels in a CNT can be derived by adding all the subbands contributing to the current conduction. Using Fermi function, it can be expressed as

$$N_{ch,i} = \sum_{\text{subbands}} \frac{1}{\exp(|E_i - E_F|/k_B T) + 1} \tag{4.2a}$$

where T is the temperature, k_B is the Boltzmann constant, and E_i is the lowest (or highest) energy for the subbands above (or below) the Fermi level, E_F.

A simplified form of expression (4.2a) is [135]:

$$\begin{aligned} N_{ch,i} &\approx k_1 T d_i + k_2 \qquad && d_i > d_T / T \\ &\approx 2/3 && d_i < d_T / T \end{aligned} \tag{4.2b}$$

where d_i represents the diameter of CNT in an MWCNT, k_1 and k_2 are curve fitted constants. The value of d_T (=1300 nm·K) is determined by the gap between the subbands and the thermal energy of electrons. The *RLC* parasitics can be extracted a follows:

4.2.1 Resistance

Each shell in the MWCNT primarily demonstrates three different types of resistances: 1) quantum resistance (R_Q) due to the finite conductance value of quantum wire if there is no scatterings along the length; 2) imperfect metal-nanotube contact resistance (R_{MC}) that exhibits a value ranging from zero to few kilo-ohms depending on the fabrication process [9], [15], [137]; and 3) scattering resistance (r_s) due to acoustic phonon scattering and optical phonon scattering that occurs when the nanotube lengths exceeds the mean free path of electrons. The scattering resistance is appeared as per unit length distributed resistance along the line, whereas 1) and 2) are considered as lumped resistances placed at the contacts of near-end and far-end terminals. The overall effective lumped resistance at the near-end/far-end terminals of the MWCNT can be expressed as

$$R_{lump,ESC} = \frac{1}{2}\left[\sum_{i=1}^{N}\left(\frac{R_Q}{2N_{ch,i}} + R_{MC,i}\right)^{-1}\right]^{-1} \quad \text{where } R_Q = \frac{h}{e^2} \approx 25.8\ \text{K}\Omega \tag{4.3a}$$

The p.u.l. scattering resistance of an MWCNT can be expressed as

$$r_{s,ESC} = \frac{h/e^2}{\sum_{i=1}^{N} 2N_{ch,i}\lambda_{mfp,i}} \text{ where } \lambda_{mfp,i} = \frac{10^3 d_i}{(T/T_0)-2}, T_0 = 100\text{ K} \tag{4.3b}$$

where h and e represent the Planckøs constant and the charge of an electron, respectively.

4.2.2 Inductance

The MWCNT demonstrates two different types of inductances:

1) Magnetic inductance: The magnetic inductance (l_e) is due to the magnetic field generation around a current carrying conductor. In the presence of ground plane, the p.u.l. magnetic inductance of a CNT shell shown in Figure 4.4 is given by [81]

$$l_e = \frac{\mu}{2\pi}\cosh^{-1}\left(\frac{d+2H}{d}\right) \tag{4.4a}$$

where d and H represent the shell diameter and height from the ground plane, respectively. Additionally, the inter-shell mutual inductance (l_{m}) is mainly due to the magnetic field coupling between the adjacent shells in an MWCNT. The p.u.l. l_m can be expressed as [26]

$$l_m = \frac{\mu}{2\pi}\ln\left(\frac{d_i}{d_{i-1}}\right) \tag{4.4b}$$

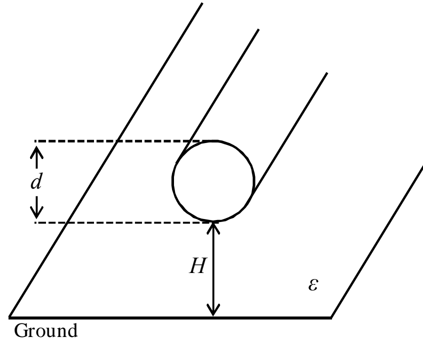


Figure 4.4. A single CNT shell above a ground plane.

2) Kinetic inductance: The kinetic inductance (l_k) is mainly due to the kinetic energy of electrons. By equating kinetic energy stored in each conducting channel of a CNT shell to the effective inductance, the kinetic inductance of each conducting channel ($l_k^{'}$) in a CNT can be expressed as [81]

$$l_k' = \frac{h}{2e^2 v_F} \tag{4.4c}$$

where v_F is the Fermi velocity ≈ 8×10^5 m/s [138].

By adopting a recursive approach proposed in [86], the equivalent inductance ($l_{k,ESC}$) of Figure 4.3 can be expressed as

$$l_{equ,1} = l_{k,1} \tag{4.4d}$$

$$l_{equ,i} = \left(\frac{1}{l_{equ,i-1} + l_m^{i-1,i}} + \frac{1}{l_{k,i}} \right)^{-1}, \ i = 2,3, \cdots\cdots, N \tag{4.4e}$$

$$l_{k,ESC} = l_{equ,N} \tag{4.4f}$$

where $l_m^{i-1,i} = \frac{\mu}{2\pi} \ln\left(d_i / d_{i-1} \right), \ \ i = 2,3, \cdots\cdots, N$ (4.4g)

$$l_{k,i} = \frac{1}{2N_{ch,i}} \frac{h}{2e^2 v_F} \qquad 1 \le i \le N \tag{4.4h}$$

4.2.3 Capacitance

The MWCNT interconnect consists of two types of capacitances:

1) Electrostatic capacitance: It represents the electrostatic field coupling between the CNT and the ground plane. The electrostatic capacitance (c_e) of MWCNT appears between the external shell and the ground plane, as external shell shields the internal ones. The p.u.l. c_e of a CNT shell shown in Figure 4.4 can be expressed as [81]

$$c_e = \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{d + 2H}{d} \right)} \tag{4.5a}$$

Additionally, the inter-shell coupling capacitance (c_m) is mainly due to the potential difference between adjacent shells in MWCNT. The p.u.l. c_m can be expressed as [26]

$$c_m = \frac{2\pi\varepsilon}{\ln\left(\frac{d_i}{d_{i-1}} \right)} \tag{4.5b}$$

2) Quantum capacitance: It originates from the quantum electrostatic energy stored in a CNT shell when it carries current. According to the Pauli exclusion principle, it is only possible to add extra electrons into the CNT shell at an available state above the Fermi level. By equating this energy to the effective capacitance energy, the quantum capacitance of each conducting channel ($c_q^{'}$) in a CNT can be expressed as

$$c_q^{'} = \frac{2e^2}{hv_F} \tag{4.5c}$$

The distributed line capacitance, $c_{q,ESC}$ is expressed in terms of quantum capacitance (c_q) and coupling capacitance (c_m) between shells

$$c_{equ,1} = c_{q,1} \tag{4.5d}$$

$$c_{equ,i} = \left(\frac{1}{c_{equ,i-1}} + \frac{1}{c_m^{i-1,i}} \right)^{-1} + c_{q,i}, \; i = 2, 3, \cdots\cdots, N \tag{4.5e}$$

$$c_{q,ESC} = c_{equ,N} \tag{4.5f}$$

where $c_m^{i-1,i} = \frac{2\pi\varepsilon}{\ln(d_i/d_{i-1})}, \; i = 2, 3, \cdots\cdots, N$ (4.5g)

$$c_{q,i} = 2N_{ch,i} \frac{2e^2}{hv_F} \qquad 1 \le i \le N \tag{4.5h}$$

4.3. FDTD Model of MWCNT Interconnect

The FDTD method is used to model the coupled MWCNT interconnect lines. The coupled-two interconnect lines are analyzed in this section; however, the model can be extended to coupled-N lines with a low computational cost.

4.3.1 The MWCNT Interconnect Line

The coupled-two MWCNT interconnect line structure is shown in Figure 4.5, where r_{s1}, r_{s2} are the scattering resistances; l_{k1}, l_{k2} are the kinetic inductances; l_{e1}, l_{e2} are the magnetic inductances; c_{q1}, c_{q2} are the quantum capacitances; c_{e1}, c_{e2} are the electrostatic capacitances; and C_{L1}, C_{L2} are the load capacitances of line 1 and line 2, respectively where all these values are mentioned in p.u.l. The parameters c_{12} and l_{12} are the p.u.l. coupling capacitances and mutual inductances, respectively [139-149]. The position along the interconnect line, and time are denoted as z and t, respectively.

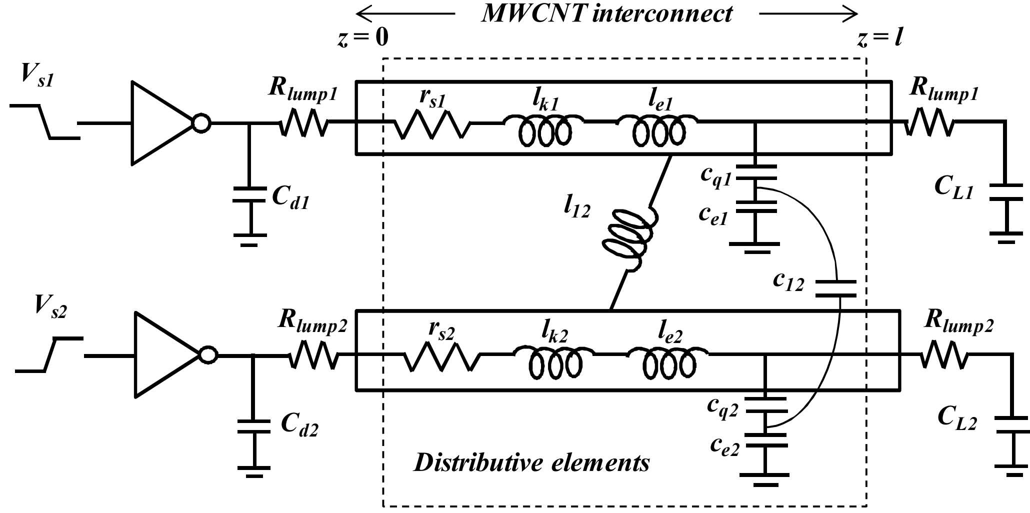


Figure 4.5. Coupled MWCNT interconnect lines.

For uniform coupled-two transmission lines the telegrapher's equations in the transverse electro-magnetic (TEM) mode [38] are represented as

$$\frac{d}{dz}\boldsymbol{V}(z,t)+\boldsymbol{RI}(z,t)+\boldsymbol{L}\frac{d}{dt}\boldsymbol{I}(z,t)=0 \tag{4.6a}$$

$$\frac{d}{dz}\boldsymbol{I}(z,t)+\boldsymbol{C}\frac{d}{dt}\boldsymbol{V}(z,t)=0 \tag{4.6b}$$

where $\boldsymbol{V}$ and $\boldsymbol{I}$ are 2×1 column vectors of line voltages and currents, respectively. The line parasitic elements are obtained in 2×2 per unit length matrix form, *i.e.*,

$$\boldsymbol{V}=\begin{bmatrix}V_1\\V_2\end{bmatrix},\ \boldsymbol{I}=\begin{bmatrix}I_1\\I_2\end{bmatrix},\ \boldsymbol{R}=\begin{bmatrix}r_{s1}&0\\0&r_{s2}\end{bmatrix},\boldsymbol{L}=\begin{bmatrix}l_{k1}+l_{e1}&l_{12}\\l_{12}&l_{k2}+l_{e2}\end{bmatrix}\text{ and}$$

$$\boldsymbol{C}=\begin{bmatrix}\left(1/c_{q1}+1/c_{e1}\right)^{-1}+c_{12}&-c_{12}\\-c_{12}&\left(1/c_{q2}+1/c_{e2}\right)^{-1}+c_{12}\end{bmatrix}$$

Central difference approximation is used to analyze the first-order differential equations (4.6a) and (4.6b) by neglecting the higher order terms. This assumption results in a negligibly small loss of accuracy in the estimation of the transient response, since the value of time segment Δt is limited by CFL condition [150]. Using the FDTD method, the analysis of telegrapher's equations shows better accuracy, if the voltage and current points are chosen at the alternate space location and separated by one-half of the position discretization, *i.e.*, $\Delta z/2$ [39]. In the same manner, the solution time for $\boldsymbol{V}$ and $\boldsymbol{I}$ should also be separated by $\Delta t/2$.

The interconnect line of length l is driven by a resistive driver at $z = 0$ and terminated by a capacitive load at $z = l$. The line is discretized into Nz uniform segments of length $\Delta z = l/Nz$. The voltage and current solution points are discretized along the line as shown in Figure 4.6.

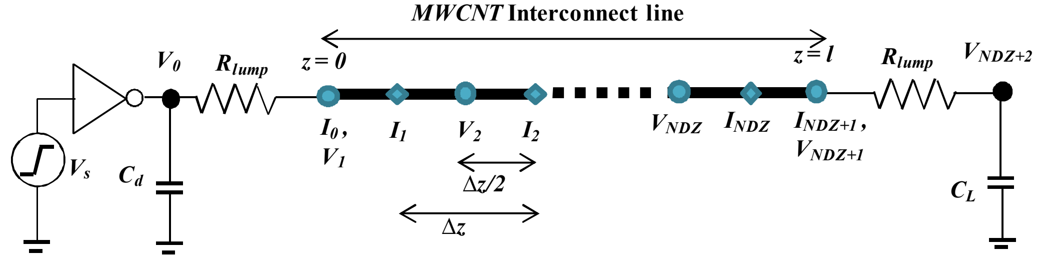


Figure 4.6. Illustration of space discretization of line for FDTD implementation.

Applying finite difference approximations to (4.6a) results in

$$\frac{\boldsymbol{V}_{k+1}^{n+1}-\boldsymbol{V}_{k}^{n+1}}{\Delta z}+\boldsymbol{L}\frac{\boldsymbol{I}_{k}^{n+3/2}-\boldsymbol{I}_{k}^{n+1/2}}{\Delta t}+\boldsymbol{R}\frac{\boldsymbol{I}_{k}^{n+3/2}+\boldsymbol{I}_{k}^{n+1/2}}{2}=0 \tag{4.7a}$$

$$\boldsymbol{I}_{k}^{n+3/2}=\boldsymbol{EFI}_{k}^{n+1/2}+\boldsymbol{E}\left[\boldsymbol{V}_{k}^{n+1}-\boldsymbol{V}_{k+1}^{n+1}\right] \text{ for } k = 1, 2, \cdots\cdots, Nz \tag{4.7b}$$

where $\boldsymbol{E}=\left[\frac{\Delta z}{\Delta t}\boldsymbol{L}+\frac{\Delta z}{2}\boldsymbol{R}\right]^{-1}$, $\boldsymbol{F}=\left[\frac{\Delta z}{\Delta t}\boldsymbol{L}-\frac{\Delta z}{2}\boldsymbol{R}\right]$

Applying finite difference approximations to (4.6b) results in

$$\frac{\boldsymbol{I}_{k}^{n+1/2}-\boldsymbol{I}_{k-1}^{n+1/2}}{\Delta z}+\boldsymbol{C}\frac{\boldsymbol{V}_{k}^{n+1}-\boldsymbol{V}_{k}^{n}}{\Delta t}=0 \tag{4.8a}$$

$$\boldsymbol{V}_{k}^{n+1}=\boldsymbol{V}_{k}^{n}+\boldsymbol{D}\left[\boldsymbol{I}_{k-1}^{n+1/2}-\boldsymbol{I}_{k}^{n+1/2}\right] \text{ for } k = 2, 3,\cdots\cdots, Nz \tag{4.8b}$$

where $\boldsymbol{D}=\left[\frac{\Delta z}{\Delta t}\boldsymbol{C}\right]^{-1}$

4.3.2 Boundary Condition at Near-end Terminal

The voltage and current points at the near end terminal are represented by $\boldsymbol{V}_1$ and $\boldsymbol{I}_0$, respectively. As indicated in Figure 4.6, it is observed that to apply the boundary conditions in (4.8b), êz is replaced by $\Delta z/2$. Therefore, at $k = 1$ equation (4.8b) becomes

$$\boldsymbol{V}_{1}^{n+1}=\boldsymbol{V}_{1}^{n}+2\boldsymbol{D}\left[\boldsymbol{I}_{0}^{n+1/2}-\boldsymbol{I}_{1}^{n+1/2}\right] \tag{4.9a}$$

The source current $\boldsymbol{I}_0$ at $(n+1/2)$ time interval is obtained by averaging the source current at (n) and $(n+1)$ time intervals. Then the equation (4.9a) becomes

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{V}_1^{n} + 2\boldsymbol{D}\left[\frac{\boldsymbol{I}_0^{n+1}+\boldsymbol{I}_0^{n}}{2} - \boldsymbol{I}_1^{n+1/2}\right] \tag{4.9b}$$

where $\boldsymbol{I}_0$ is the driver current. Applying Kirchhoff's current law (KCL) at near-end terminal, $\boldsymbol{I}_0$ can be written as

$$\boldsymbol{V}_0^{n+1} = \boldsymbol{V}_0^{n} + \boldsymbol{A}\left[\frac{\boldsymbol{C}_m}{\Delta t}(\boldsymbol{V}_s^{n+1} - \boldsymbol{V}_s^{n}) + \boldsymbol{I}_p^{n+1} - \boldsymbol{I}_n^{n+1} - \boldsymbol{I}_0^{n}\right] \tag{4.9c}$$

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{B}\boldsymbol{V}_1^{n} + 2\boldsymbol{B}\boldsymbol{D}\left[\frac{\boldsymbol{V}_0^{n+1}}{2\boldsymbol{R}_{lump}} + \frac{\boldsymbol{I}_0^{n}}{2} - \boldsymbol{I}_1^{n+1/2}\right] \tag{4.9d}$$

$$\boldsymbol{I}_0^{n+1} = \frac{1}{\boldsymbol{R}_{lump}}\left[\boldsymbol{V}_0^{n+1} - \boldsymbol{V}_1^{n+1}\right] \tag{4.9e}$$

where $\boldsymbol{A} = \left[\frac{\boldsymbol{C}_m+\boldsymbol{C}_d}{\Delta t}\right]^{-1}$, $\boldsymbol{B} = \left[\boldsymbol{U} + \frac{\boldsymbol{D}}{\boldsymbol{R}_{lump}}\right]^{-1}$

$\boldsymbol{C}_m$ is the drain to gate coupling capacitance, $\boldsymbol{C}_d$ is the drain diffusion capacitance of CMOS inverter, $\boldsymbol{I}_p$ and $\boldsymbol{I}_n$ are the PMOS and NMOS currents, respectively. The modified alpha power law model that includes the drain conductance parameter is used to express the NMOS current as

$$\boldsymbol{I}_n = \begin{cases} 0 & V_S \le V_{tn} \quad (off) \\ \boldsymbol{K}_{ln}(\boldsymbol{V}_S - \boldsymbol{V}_{tn})^{\alpha_n/2}\boldsymbol{V}_0 & \boldsymbol{V}_0 < \boldsymbol{V}_{DSATn} \quad (lin) \\ \boldsymbol{K}_{sn}(\boldsymbol{V}_S - \boldsymbol{V}_{tn})^{\alpha_n}(1+\sigma_n \boldsymbol{V}_0) & \boldsymbol{V}_0 \ge \boldsymbol{V}_{DSATn} \quad (sat) \end{cases} \tag{4.9f}$$

where K_{ln}, K_{sn}, V_{tn}, α_n and σ_n are the linear region transconductance parameter, saturation region transconductance parameter, threshold voltage, velocity saturation index and drain conductance parameter of NMOS, respectively. In a similar manner, the PMOS current can be expressed as

$$\boldsymbol{I}_p = \begin{cases} 0 & V_S \ge \boldsymbol{V}_{DD} - |V_{tp}| \quad (off) \\ \boldsymbol{K}_{lp}\left(\boldsymbol{V}_{DD} - \boldsymbol{V}_S - |\boldsymbol{V}_{tp}|\right)^{\alpha_p/2}(\boldsymbol{V}_{DD} - \boldsymbol{V}_0) & \boldsymbol{V}_0 > \boldsymbol{V}_{DD} - \boldsymbol{V}_{DSATp} \quad (lin) \\ \boldsymbol{K}_{sp}\left(\boldsymbol{V}_{DD} - \boldsymbol{V}_S - |\boldsymbol{V}_{tp}|\right)^{\alpha_p}\left(1+\sigma_p\left(\boldsymbol{V}_{DD} - \boldsymbol{V}_0\right)\right) & \boldsymbol{V}_0 \le \boldsymbol{V}_{DD} - \boldsymbol{V}_{DSATp} \quad (sat) \end{cases} \tag{4.9g}$$

4.3.3 Boundary Condition at Far-end Terminal

Here the objective is to derive the voltage expression at $k = Nz+1$, and $Nz+2$. At $k = Nz+1$, the equation (4.8b) becomes

$$\boldsymbol{V}_{Nz+1}^{n+1} = \boldsymbol{V}_{Nz+1}^{n} + 2\boldsymbol{D}\left(\boldsymbol{I}_{Nz}^{n+1/2} - \frac{\boldsymbol{I}_{Nz+1}^{n+1} + \boldsymbol{I}_{Nz+1}^{n}}{2}\right) \tag{4.10a}$$

Applying KCL at far-end terminal, the output current ($\boldsymbol{I}_{Nz+1}$) can be expressed as

$$\boldsymbol{V}_{Nz+1} - \boldsymbol{V}_{Nz+2} = \boldsymbol{R}_{lump}\boldsymbol{I}_{Nz+1} \tag{4.10b}$$

The discretized form of (4.10b) is

$$\boldsymbol{I}_{Nz+1}^{n+1} = \frac{1}{\boldsymbol{R}_{lump}}\left[\boldsymbol{V}_{Nz+1}^{n+1} - \boldsymbol{V}_{Nz+2}^{n+1}\right] \tag{4.10c}$$

Using (4.10a) and (4.10c) the far-end voltage $\boldsymbol{V}_{Nz+1}$ can be expressed as

$$\boldsymbol{V}_{Nz+1}^{n+1} = \boldsymbol{B}\boldsymbol{V}_{Nz+1}^{n} + 2\boldsymbol{B}\boldsymbol{D}\left[\frac{\boldsymbol{V}_{Nz+2}^{n+1}}{2\boldsymbol{R}_{lump}} + \boldsymbol{I}_{Nz}^{n+1/2} - \frac{\boldsymbol{I}_{Nz+1}^{n}}{2}\right] \tag{4.10d}$$

and the load voltage $\boldsymbol{V}_{Nz+2}$ is

$$\boldsymbol{V}_{Nz+2}^{n+1} = \boldsymbol{V}_{Nz+2}^{n} + \frac{\Delta t}{\boldsymbol{C}_L}\boldsymbol{I}_{Nz+1}^{n} \tag{4.10e}$$

These equations are evaluated in a bootstrapping fashion. Initially, the voltages along the line are evaluated for a specific time from equations (4.9c), (4.9d), (4.8b), (4.10e), and (4.10d) in terms of the previous values of voltage and current. Thereafter, the currents are evaluated from (4.9e), (4.7b), and (4.10c) in terms of these voltages and previous current values.

4.4. Validation of the Model

The coupled MWCNT interconnects are analyzed using the actual CMOS driver. The proposed model is implemented with the MATLAB. The industry standard HSPICE simulations are used for the validation of the results. The HSPICE simulations are carried out using the subcircuit model with 50 distributed segments for interconnect and using BSIM4 technology model for MOSFET. A symmetric CMOS driver is used to drive the interconnect load. The equivalent resistance of the driver is evaluated by averaging the resistance value over an interval when the input is between V_{DD} and $V_{DD}/2$ [1]. The signal integrity analysis is carried out at the global interconnect length of 1 mm for 32 nm technology and 0.9 V of V_{DD}. The interconnect

dimensions are based on the ITRS data [121]. The interconnect width and height from the ground plane and are 48 and 110.4 nm, respectively. The spacing between the two interconnects is 48 nm. The relative permittivity of the inter layer dielectric medium is 2.25. The load capacitance and input transition time are 2 fF and 20 ps, respectively. The following *RLC* parasitics are used in the experiments [151-158]

$$\boldsymbol{R}=\begin{bmatrix}653.67 & 0\\ 0 & 653.67\end{bmatrix}\frac{k\Omega}{m},\ \boldsymbol{L}=\begin{bmatrix}14.83 & 0.61\\ 0.61 & 14.83\end{bmatrix}\frac{\mu H}{m}\ \text{and}\ \boldsymbol{C}=\begin{bmatrix}93.33 & -71.50\\ -71.50 & 93.33\end{bmatrix}\frac{pF}{m}$$

In the interconnect system, lines 1 and 2 are considered as aggressor and victim lines, respectively. For the above-mentioned setup, the transient response is analyzed at the far-end terminal of the victim line using the proposed model, resistive driver based model [21], and HSPICE simulations using CMOS driver. From Figure 4.7, it can be observed that the model presented in [21] is unable to capture the timing waveform accurately. However, the proposed model is able to successfully capture the HSPICE waveform characteristics.

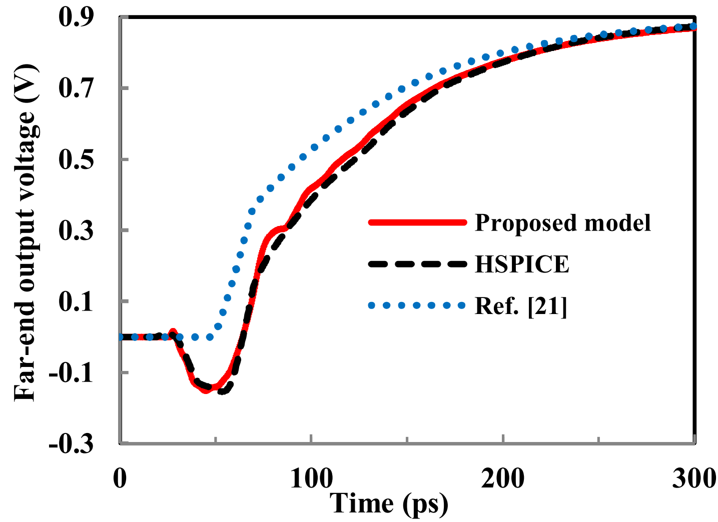


Figure 4.7. Transient response at the far-end terminal of the victim line when the aggressor and victim lines are switched out-of-phase.

The crosstalk induced delay is analyzed under two different cases. First case considers out-phase delay where the input signals of aggressor and victim lines are switched out-of-phase. Second case considers in-phase delay where the input signals of aggressor and victim lines are switched in-phase. Figures 4.8 (a) and (b), shows out-phase and in-phase delay comparison, respectively for different interconnect

lengths. It can be clearly observed that the model proposed in [21], fails to estimate the crosstalk induced delay for all interconnect lengths. The model proposed in [21] underestimates the delay for both out-phase and in-phase switching by average errors of 27.2% and 35.3%, respectively.

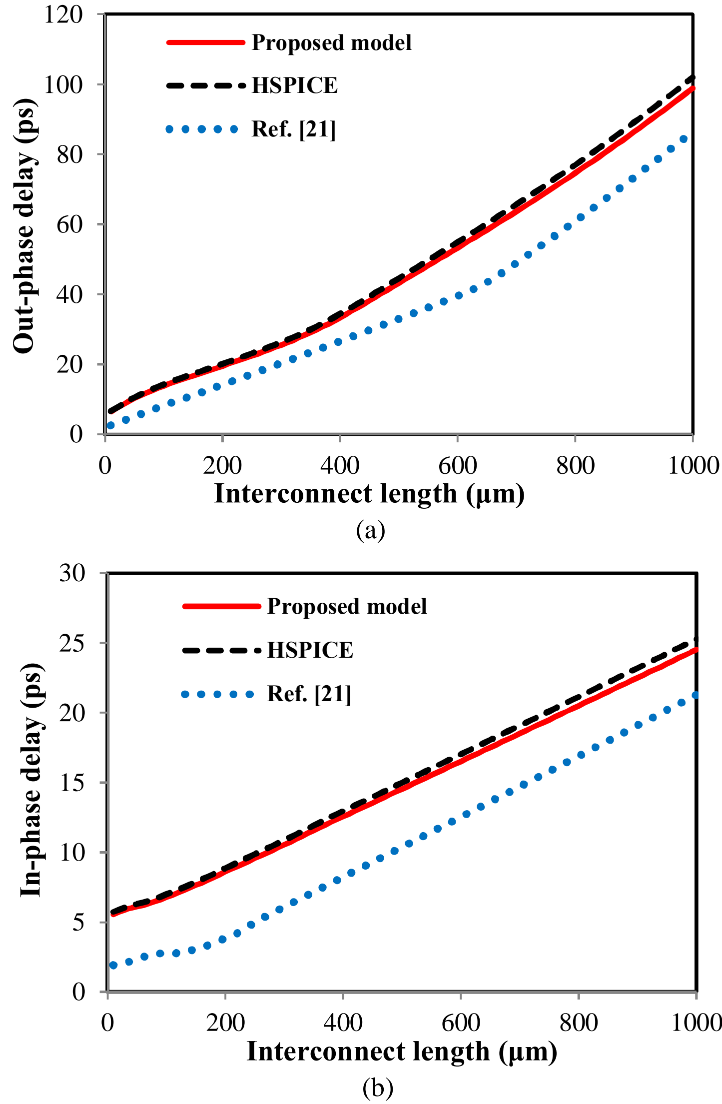


Figure 4.8. Crosstalk induced delay comparison (a) out-phase delay and (b) in-phase phase delay with the variation of interconnect length.

The functional crosstalk noise is analyzed when the aggressor line is switched and the victim line is kept in quiescent mode. Figure 4.9 depicts the noise peak voltage comparison on the victim line. It can be observed that the resistive driver model [21] overestimates the noise peak voltage, wherein the average error is observed to be 15%.

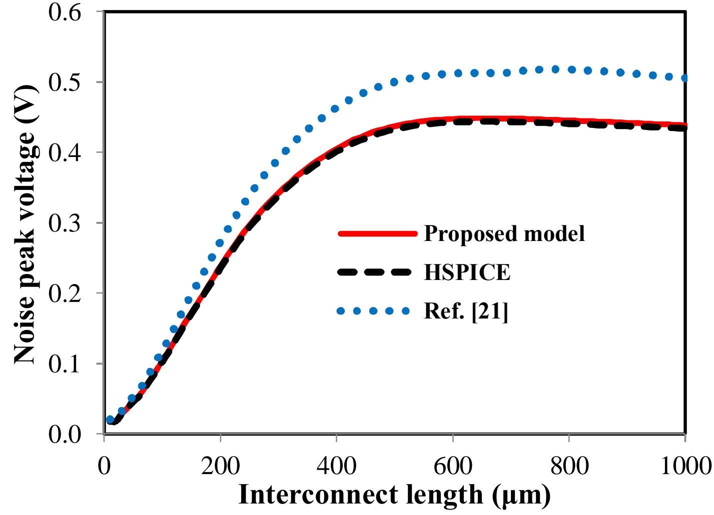


Figure 4.9. Noise peak voltage comparison of victim line 2 with the variation of interconnect length.

To test the robustness, the proposed model is examined at different input transition times. The interconnect length is considered as 500 µm. Figure 4.10 depicts the computational error involved in predicting the crosstalk induced propagation delay. It can be observed that the proposed model accurately predicts the delay for both out-phase and in-phase transitions. The average error involved is only 1.4% and 1.5% during in-phase and out-phase switching, respectively. Contrastingly, with the resistive driver model [21], the average error involved is 38.6% and 25.1% for in-phase and out-phase switching, respectively.

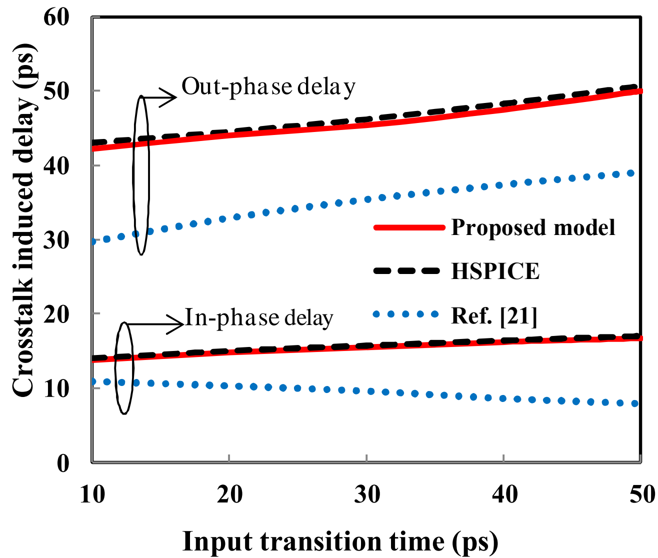


Figure 4.10. Crosstalk induced delay comparison on victim line 2 with the variation of input transition time.

Modified nodal analysis (MNA) is the core approach used in SPICE to formulate the system equations. Applying the Kirchhoff's current law and following the energy conversion principle, the MNA generates the set of matrix equations. The order of the matrix is determined by the number of nodes and unknown variables in the circuit. The unknown variables are solved after the inversion of the matrix and therefore require more computational time. However, the FDTD operator is matrix free and therefore fast and memory efficient as compared to HSPICE simulations.

The efficiency of the proposed model is examined under different test cases. The analysis is carried out by varying the space segment while keeping the time segment constant for coupled interconnects. Using a PC with Intel Dual Core CPU (2.33 GHz, 4 GB RAM), the comparison results are provided in the Table 4.1. Using the proposed model, it is observed that the CPU runtime reduces by an average of 91% in comparison to HSPICE simulations. Additionally, the proposed model is compared with the HSPICE simulations using the same modified alpha-power law model. It is observed that the average CPU runtime reduces by 88% in comparison to HSPICE simulations.

Table 4.1 CPU runtime comparison between proposed model and HSPICE with 1000 time segments

Number of space segments	HSPICE (s)	Proposed model (s)	% reduction in runtime
1	0.14	0.02	85.71
10	0.68	0.06	91.17
50	2.97	0.23	92.25
100	6.04	0.31	94.86

4.5. Sensitivity analysis

The primary assumptions made in the proposed work are for: 1) number of conducting channels; and 2) contact resistance. This sub-section presents the sensitivity analysis to evaluate the validity of these assumptions.

4.5.1 Sensitivity analysis for number of conducting channels

The number of conducting channels in a CNT can be obtained from expression (4.2b), which is an approximated form of (4.2a). Table 4.2 shows the variations in parasitics and crosstalk induced performance parameters using equations (4.2a) and

(4.2b). The average percentage change in parasitics and performance parameters are just 2.3% and 2%, respectively. It can be inferred that the parasitics and crosstalk induced performance parameters are almost insensitive to the usage of approximated expression for obtaining N_{ch}.

Table 4.2 Variation between (4.2a) and (4.2b) on parasitics and crosstalk induced performance parameters

Variation between (4.2a) and (4.2b)	Parasitic parameter				Performance parameter		
	Lumped resistance (Ω)	**Scattering resistance (Ω)**	***C* (fF)**	***L* (pH)**	**Noise peak voltage (V)**	**In-phase delay (ps)**	**Out-phase delay (ps)**
From Eqn (4.2a)	11.79	675.10	21.84	15.28	0.433	26.0	64.3
From Eqn (4.2b)	11.43	653.67	21.83	14.83	0.424	25.3	63.6
% change	3.05	3.17	0.04	2.94	2.1	2.6	1.1

Table 4.3 Variation of performance parameters due to change in R_{MC}

Parasitic parameter		Performance parameter			
R_{MC} (per shell) (kΩ)	**Lumped resistance ($R_{lump,ESC}$) (Ω)**	**Noise peak voltage (V)**	**Noise peak timing (ps)**	**In-phase delay (ps)**	**Out-phase delay (ps)**
0	11.20	0.425	54.5	25.1	63.5
2	11.3	0.425	54.4	25.3	63.5
4	11.49	0.424	54.4	25.3	63.6
6	11.63	0.424	54.4	25.4	63.6
8	11.77	0.424	54.4	25.4	63.8

4.5.2 Sensitivity analysis for contact resistance

The value of imperfect metal contact resistance can range from the best case value of zero to the worst case value of few kilo-ohms depending on the fabrication process. As reported earlier [9], the R_{MC} value is considered as 3.2 ká per shell. However, a sensitivity analysis on parasitic $R_{lump,ESC}$ and crosstalk induced performance parameters for R_{MC} varying from 0 to 8 ká is carried out and the results are presented in Table 4.3. A maximum variation of 5% in $R_{lump,ESC}$ and almost no

change in the crosstalk performance are noticed with the change in R_{MC}. This is due to the fact that the crosstalk induced performance parameters are primarily depends on the scattering resistance and almost insensitive to the change in R_{MC}.

4.5.3 Sensitivity analysis for PVT variations

The uncertainties and variations in geometrical processes may produce a remarkable alteration in crosstalk induced performance. Therefore, it is not sufficient to analyze the nominal value of the parameters and the observed performance. Using the process voltage temperature (PVT) variations a range of values are required to consider for effective and reliable design of interconnects. Monte Carlo approach is adopted in order to study the impact of PVT variation. The process induced parameters are varied by ±10% of its nominal value. Based on the PVT variations, the different parasitic values are used to analyze the power/delay/crosstalk, for which two new parameters N+ and N- are introduced that can be defined as

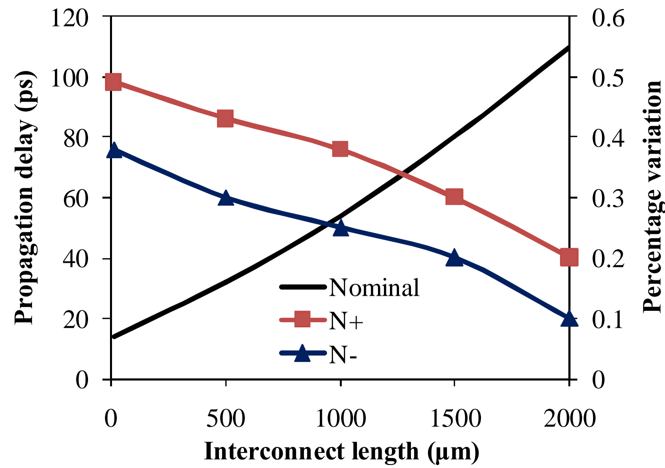
N+ = (Maximum value - Nominal value) / Nominal value

N- = (Nominal value - Minimum value) / Nominal value

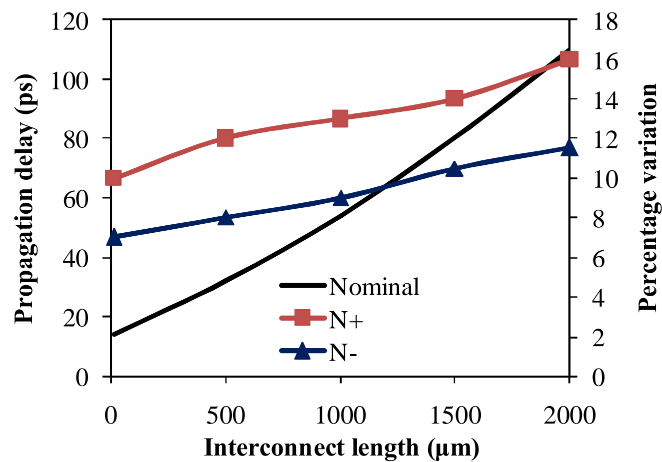
In device the impact of sub-threshold process parameters such as threshold voltage/oxide-thickness/channel-length has been analyzed and observed that the average deviation in N+ and N- is less than 1% for process induced device parameters. It is due to the fact that in driver-interconnect-load system, the overall performance is primarily determined by the interconnect line rather than device. Similarly, the power results are also observed to be less than 1% variations. The change in propagation delay due to device threshold process induced variation is shown in Figure 4.11 (a).

Interconnect process induced variations such as width, thickness and separation between the two interconnect lines are analyzed. It is observed that the average deviation in N+ and N- is almost 2% for interconnect width and 12% for interconnect thickness and 6% for interconnect spacing. Moreover, it is observed that the variation is much higher in thickness as compared to width and spacing of the interconnects. The power variations are also observed to be higher for thickness process variation due to its larger dimensional value compared to width and spacing. The change in propagation delay due to interconnect thickness variation is shown in Figure 4.11 (b). In addition to the device and interconnect variations, the supply and

temperature variations are also performed. It has been observed that the effect of supply voltage is higher than temperature variation.



(a)



(b)

Figure 4.11. Propagation delay with different interconnect lengths for process induced variations on (a) device threshold and (b) interconnect thickness.

4.6. Summary

This chapter presented an accurate model to analyze the crosstalk effects in coupled MWCNT interconnect lines. The CMOS driver and the coupled MWCNT interconnect are modeled by modified alpha power law model and FDTD method, respectively. It has been observed that the results of the proposed model exhibit a good agreement with HSPICE simulations. Over the random number of test cases, the average error in the propagation delay measurement is observed to be less than 2%. Moreover, the sensitivity analysis is performed based on the assumptions used in the

proposed model. It is observed that the percentage change in parasitic elements and performance parameters are almost negligible with respect to the assumptions associated with the model. This analysis suggests that, with continuous advancements in FDTD technique the proposed model would play a significant role in performance analysis of MWCNT on-chip interconnects and would be potentially incorporated in TCAD simulators.

Chapter 5

Crosstalk Modeling with Width Dependent MFP in MLGNR Interconnects Using FDTD Technique

5.1. Introduction

In the first four decades of the semiconductor industry, system performance was entirely dependent on the transistor delay and power dissipation [1]. The technology scaling had an adverse effect on *RLC* delay of complex VLSI circuits as the resistivity increased for the small-dimensional metal interconnects made up of Cu [159-164]. The reduced cross-sectional area of Cu interconnects resulted in higher resistivity under the effects of enhanced grain and surface scattering. Moreover, with thinner interconnects and higher operating frequency, electromigration induced problems gained more attention. Presently, at GHz range of frequencies, issues like skin effect, stability, operational bandwidth and crosstalk severely affect the performance of Cu interconnects [165, 166]. Therefore, researchers are forced to find an alternative to Cu material for high-speed global VLSI interconnects [167-173].

During the recent past, graphene nanoribbons (GNRs) have rapidly gained importance as an emerging material that potentially forms a monolithic system for field effect devices and interconnects [29], [104]. GNR is a sheet of graphite wherein carbon atoms are tightly packed in honeycomb lattice structures [106]. High quality GNR sheets have long mean free path (MFP) ranging from 1-5 μm that results in ballistic transport phenomenon. Due to the large MFP, GNRs have higher carrier mobility of 10^5 $cm^2/(V{\cdot}s)$ and larger current densities, of 10^9 A/cm^2 in comparison to Cu [100]. Due to high intrinsic resistance of single layer GNR, researchers often prefer multi-layer GNR (MLGNR) as potential interconnect material [174-177]. Moreover, intercalation doping can increase the in-plane conductivity of MLGNR up to twenty times that involves insertion of one dopant layer between each pair of adjacent graphene layers [106]. Intercalation doping can also increase the MFP due to an increase in spacing between the adjacent layers. Additionally, the easier fabrication process of MLGNR makes it a promising candidate for VLSI interconnect material. The comparison between the performance of MLGNR and Cu has been studied in

[108], where the authors observed that MLGNR interconnect demonstrates the smaller propagation delay than Cu interconnect.

Using the equivalent transmission line model, the crosstalk effects of coupled MLGNR have been studied in [37], where the authors considered the MFP parameter independent of width by assuming perfectly smooth edges of MLGNR. However, in reality all GNRs exhibit edge roughness [30, 31]. Due to these rough edges, the electron scattering increases, thereby decreasing the overall MFP and increasing the resistivity [99]. At lower widths, the MFP is predominantly dependent on the edge roughness. Therefore, it is essential to incorporate width-dependent MFP while modeling the performance of MLGNR based interconnects.

This chapter accurately analyzes the performance of MLGNR interconnects based on the finite-difference time-domain (FDTD) technique. In a more realistic manner, the proposed model includes the effect of width-dependent MFP of the MLGNR while taking into account the edge roughness. Moreover, a non-linear CMOS driver is used to drive the MLGNR interconnect line. At different interconnect widths, the crosstalk induced propagation delay is compared among proposed model, HSPICE and the existing crosstalk noise model.

The organization of this chapter is as follows: Section 5.1 introduces the importance of MLGNR interconnects in current research scenario and briefs about the work carried out. Based on the multiconductor transmission line theory, an equivalent single conductor (ESC) model of MLGNR interconnects is described in Section 5.2. Using a driver-interconnect-load system, a comparative analysis of transient response of MTL and ESC models is also presented in this section. Section 5.3 brief the FDTD model for the MLGNR interconnects. The validation of the proposed model is discussed in Section 5.4 along with the performance comparison between Cu and MLGNR interconnects. Section 5.5 concludes this chapter.

5.2. Equivalent Single Conductor Model of the MLGNR Interconnect

The proposed model is developed for MLGNR interconnect line positioned over a ground plane at a distance H with a dielectric medium sandwiched between GNRs as shown in Figure 5.1. The MLGNR consists of N number of layers

$$N_{layer} = 1+\mathrm{int}[t/\delta] \tag{5.1}$$

where w, t and δ are width, thickness and interlayer spacing, respectively. The number of conducting channels per layer can be expressed as

$$N_{ch} = \sum_{i=0}^{n_c} \left[1+e^{(E_i - E_F)/k_B T}\right]^{-1} + \sum_{i=0}^{n_v} \left[1+e^{(E_i + E_F)/k_B T}\right]^{-1} \tag{5.2a}$$

where the first and second summations represent the contributions of the n_c conduction subbands and n_v valence subbands, respectively, T is the temperature, k_B is the Boltzmann constant, E_F is the Fermi level, and E_i is the lowest (highest) energy of the ith conduction (valence) subband. In general, the value of E_F is set to zero for neutral GNR [106]. However, some charge usually gets trapped at the interface of graphene and the substrate. This is due to the planar structure of graphene and also due to the work function difference between the graphene and substrate. Alternatively, the number of conduction channels is also derived from the following approximated expression [109]

$$N_{ch} = \begin{cases} a_0 + a_1 w + a_2 w^2 + a_3 E_F + a_4 w E_F + a_5 E_F^2 & \text{for } E_F > 0 \\ b_0 + b_1 + b_2 w^2 & \text{for } E_F = 0 \end{cases} \tag{5.2b}$$

For metallic GNR at T = 300 K, the fitting parameters a_0-a_6 and b_0-b_2 are given in Table 5.1 and Table 5.2, respectively [109].

Table 5.1 Fitting parameters (a_0-a_6) for calculating the N_{ch} of $E_F > 0$

Fitting parameters					
a_0	a_1	a_2	a_3	a_4	a_5
1.244	-1.696×10^{-2}	7.517×10^{-5}	-5.031	1.225	5.122

Table 5.2 Fitting parameters (b_0-b_3) for calculating the N_{ch} of $E_F = 0$

Fitting parameters		
b_0	b_1	b_2
1.94	2.97×10^{-4}	2.29×10^{-4}

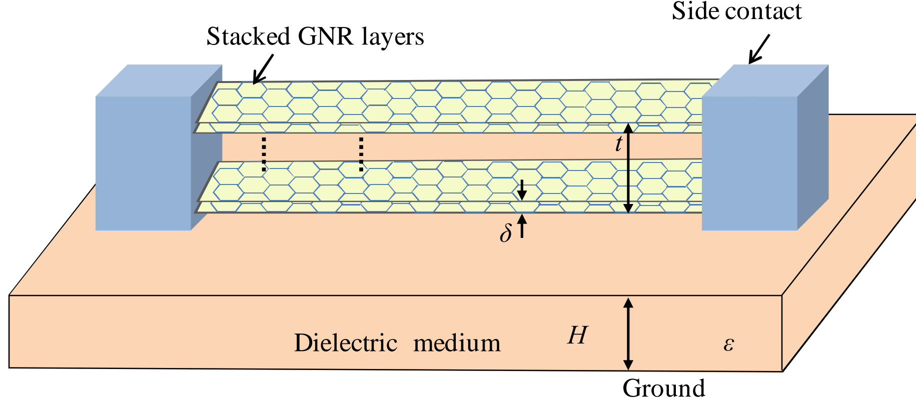


Figure 5.1. The geometric structure of MLGNR.

The typical ESC model of an MLGNR is shown in Figure 5.2, where R_{MC}, R_Q, and r_s are the imperfect metal contact, quantum and scattering resistances, respectively; l_k and l_e are the kinetic and magnetic inductances, respectively; c_q and c_e are the quantum and electrostatic capacitances, respectively. The R_{lump} represents the average value of metal contact resistance and quantum resistance.

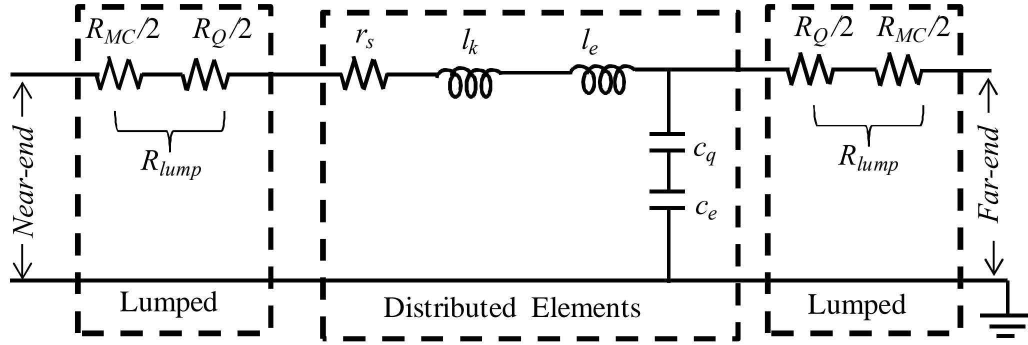


Figure 5.2. Equivalent single conductor model of an MLGNR interconnect.

The resistances R_{lump} and r_s are expressed as

$$R_{lump} = \frac{1}{2}\left[\frac{h/2e^2}{N_{ch}N_{layer}} + \frac{R_{MC}}{N_{layer}}\right] \tag{5.3}$$

$$r_{s,ESC} = \left(h/2e^2 N_{layer}\right)\left(\sum_n \left(\frac{l}{\lambda_{eff_n}}\right)^{-1}\right)^{-1} \tag{5.4}$$

where h, e, N_{layer}, n, l and λ_{eff} represent the Planckøs constant, electron charge, number of GNR layers, number of subbands, length, and overall effective MFP, respectively.

The λ_{eff} of nth subband is expressed as

$$\frac{1}{\lambda_{eff_n}} = \frac{1}{\lambda_d} + \frac{1}{\lambda_n} \tag{5.5}$$

where λ_d and λ_n represent the MFP corresponding to the scattering effects due to defects and edge roughness, respectively. The value of λ_d is considered as 419 nm and 1.03 m for neutral and doped MLGNRs, respectively. The λ_n for n^{th} subband is expressed as [99]

$$\lambda_n = \frac{w}{P}\sqrt{\left(\frac{2wE_F}{nhv_F}\right)^2 - 1} \tag{5.6}$$

where P is the backscattering probability, lies in the range 0 to 1 and v_F is the Fermi velocity.

The quantum capacitance and kinetic inductance of an MLGNR can be expressed as

$$c_{q,ESC} = N_{ch} N_{layer} \frac{2 \times 2q^2}{hv_F} \tag{5.7}$$

$$l_{k,ESC} = \frac{1}{N_{ch} N_{layer}} \frac{h}{2 \times 2q^2 v_F} \tag{5.8}$$

The values of $l_{e,ESC}$ and $c_{e,ESC}$ can be obtained using the electromagnetic field solvers.

5.2.1 Transient Analysis of MTL and ESC Models

The ESC model of MLGNR is validated with respect to the MTL model by performing transient analysis of DIL system. The CMOS gate driven MLGNR interconnect line is shown in Figure 5.3. The number of stacked GNR layers is considered as 20. The interconnect line is excited and terminated by a CMOS driver and capacitive load, respectively. The symmetric CMOS inverter is used and the load capacitance is considered as 250 aF. To maintain good accuracy, the number of distributed segments is considered as 20. For different interconnect lengths ranging from 100 m to 1000 m, Figure 5.4 shows the far-end voltage waveforms of MLGNR interconnects. It is observed that the output voltage waveforms of the ESC model are in good agreement with the MTL model for all interconnect lengths.

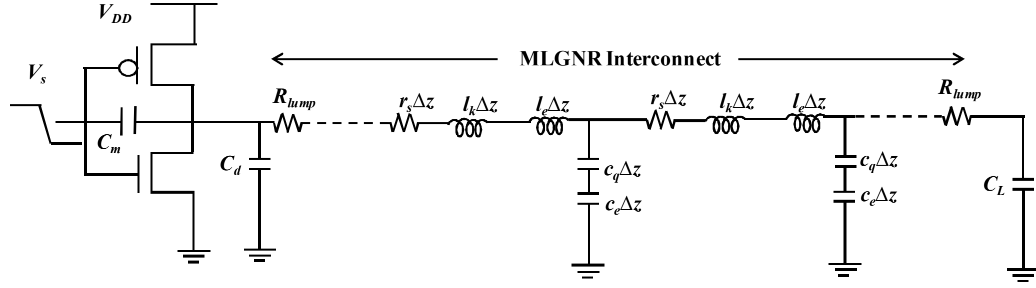


Figure 5.3. Driver-interconnect-load (DIL) structure, wherein R_{lump} is placed at near-end and far-end terminals of the interconnect line due to the effect of quantum and imperfect contact resistances.

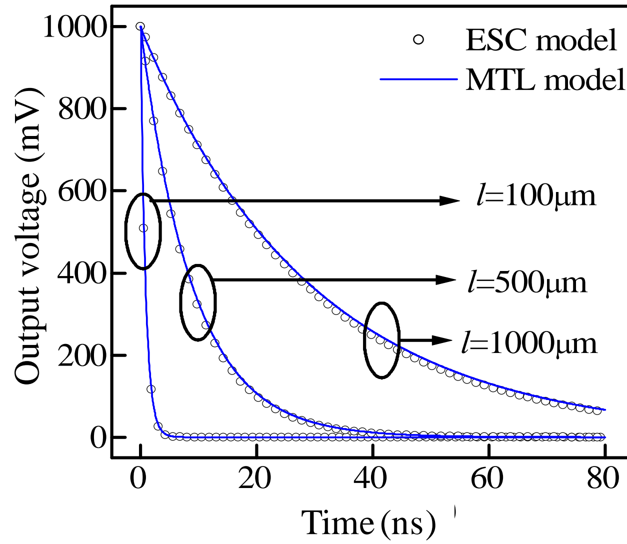


Figure 5.4. Transient waveforms of the output voltages of MLGNR (N_{layer} = 20) interconnect.

5.3. FDTD Model of the MLGNR Interconnect

The MLGNR interconnect of length l is driven by a CMOS inverter at near end and terminated by a capacitive load at far-end. The total interconnect length is discretized into Nz uniform segments of space step Δz and the total simulation time is discretized into n uniform segments of time step Δt. The value of n can be determined by dividing the total simulation time by êt. The time step, êt is determined by the Courant stability condition. The maximum time step that can be allowed for the stable operation is $\Delta t_{max} = \Delta z/v_{\text{max}}$, where v_{max} is the maximum phase velocity. The voltage and current solution points are discretized along the line as shown in Figure 5.5.

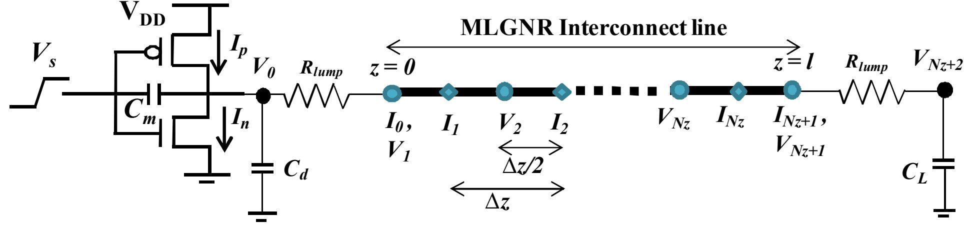


Figure 5.5. Illustration of space discretization of line for FDTD implementation.

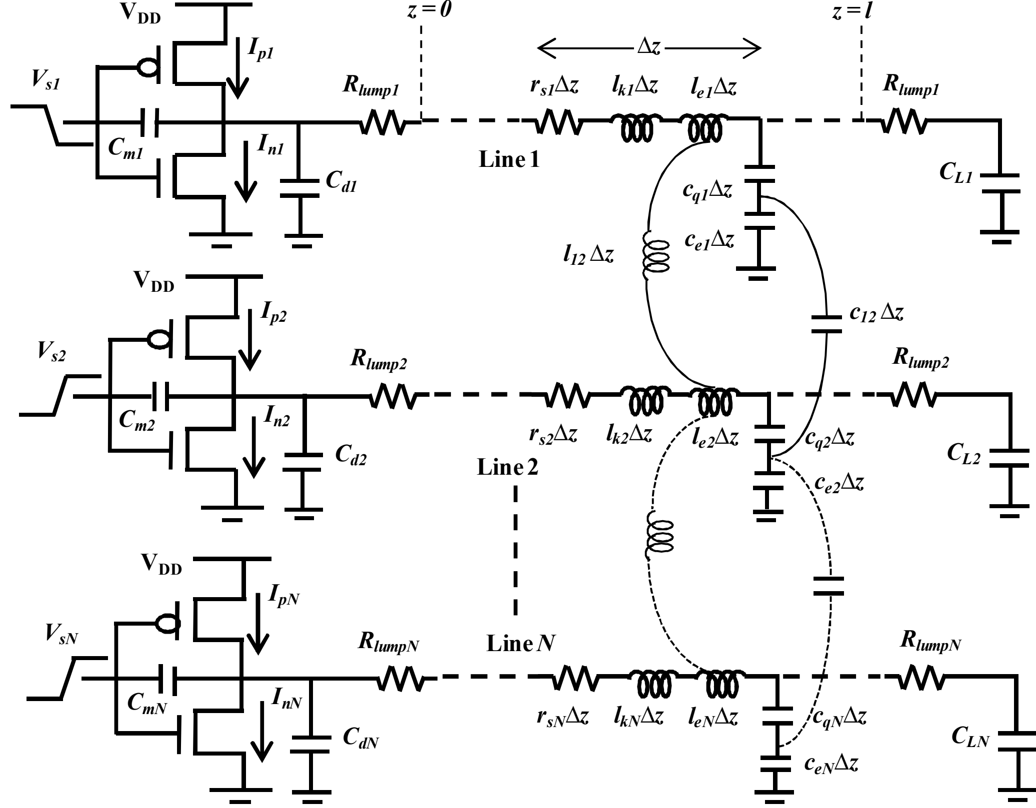


Figure 5.6. Coupled MWCNT interconnect lines driven by CMOS inverter.

The CMOS gate-driven coupled MWCNT interconnects are shown in Figure 5.6. The telegrapher's equations are

$$\frac{d}{dz}\boldsymbol{V}(z,t)+\boldsymbol{RI}(z,t)+\boldsymbol{L}\frac{d}{dt}\boldsymbol{I}(z,t)=0 \tag{5.9a}$$

$$\frac{d}{dz}\boldsymbol{I}(z,t)+\frac{d}{dt}\boldsymbol{CV}(z,t)=0 \tag{5.9b}$$

where $\boldsymbol{V}$ and $\boldsymbol{I}$ are $N\times1$ column vectors and the line parasitic elements are obtained in $N\times N$ matrix form. For instance, the voltage $\boldsymbol{V}$ is $\begin{bmatrix}V_1 & V_2 & . & . & . & V_{N-1} & V_N\end{bmatrix}^T$,

resistance $\boldsymbol{R}$ and inductance $\boldsymbol{L}$ matrices are $\begin{bmatrix} r_{s1} & 0 & 0 & . & . \\ 0 & r_{s2} & 0 & . & . \\ 0 & 0 & r_{s3} & . & . \\ . & . & . & . & . \\ . & . & . & 0 & r_{sN} \end{bmatrix}$ and $\begin{bmatrix} l_{k1}+l_{e1} & l_{12} & l_{13} & . & . \\ l_{21} & l_{k2}+l_{e2} & l_{23} & . & . \\ l_{31} & l_{32} & l_{k3}+l_{e3} & . & . \\ . & . & . & . & . \\ . & . & . & l_{N-1,N} & l_{kN}+l_{eN} \end{bmatrix}$, respectively, where r_{sN} is the scattering resistance of line N, and $l_{N\text{-}1,N}$ is the mutual inductance between the lines N-1 and N.

Applying finite difference approximations to (5.9a) and (5.9b) the line voltages and currents can be determined, whereas using Kirchhoff's law at near-end and far-end boundaries the terminal voltage and current can be determined as

$$\boldsymbol{V}_0^{n+1} = \boldsymbol{V}_0^n + \boldsymbol{A}\left[\frac{\boldsymbol{C}_m}{\Delta t}(\boldsymbol{V}_s^{n+1} - \boldsymbol{V}_s^n) + \boldsymbol{I}_p^{n+1} - \boldsymbol{I}_n^{n+1} - \boldsymbol{I}_0^n\right] \tag{5.10}$$

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{B}\boldsymbol{V}_1^n + 2\boldsymbol{B}\boldsymbol{D}\left[\frac{\boldsymbol{V}_0^{n+1}}{2\boldsymbol{R}_{lump}} + \frac{\boldsymbol{I}_0^n}{2} - \boldsymbol{I}_1^{n+1/2}\right] \tag{5.11}$$

$$\boldsymbol{V}_k^{n+1} = \boldsymbol{V}_k^n + \boldsymbol{D}\left[\boldsymbol{I}_{k\text{-}1}^{n+1/2} - \boldsymbol{I}_k^{n+1/2}\right] \text{ for } k = 2, 3, \cdots\cdots, Nz \tag{5.12}$$

$$\boldsymbol{V}_{Nz+2}^{n+1} = \boldsymbol{V}_{Nz+2}^n + \frac{\Delta t}{\boldsymbol{C}_L}\boldsymbol{I}_{Nz+1}^n \tag{5.13}$$

$$\boldsymbol{V}_{Nz+1}^{n+1} = \boldsymbol{B}\boldsymbol{V}_{Nz+1}^n + 2\boldsymbol{B}\boldsymbol{D}\left[\frac{\boldsymbol{V}_{Nz+2}^{n+1}}{2\boldsymbol{R}_{lump}} + \boldsymbol{I}_{Nz}^{n+1/2} - \frac{\boldsymbol{I}_{Nz+1}^n}{2}\right] \tag{5.14}$$

$$\boldsymbol{I}_0^{n+1} = \frac{1}{\boldsymbol{R}_{lump}}\left[\boldsymbol{V}_0^{n+1} - \boldsymbol{V}_1^{n+1}\right] \tag{5.15}$$

$$\boldsymbol{I}_k^{n+3/2} = \boldsymbol{E}\boldsymbol{F}\boldsymbol{I}_k^{n+1/2} + \boldsymbol{E}\left[\boldsymbol{V}_k^{n+1} - \boldsymbol{V}_{k+1}^{n+1}\right] \text{for } k = 1, 2, \cdots\cdots, Nz \tag{5.16}$$

$$\boldsymbol{I}_{Nz+1}^{n+1} = \frac{1}{\boldsymbol{R}_{lump}}\left[\boldsymbol{V}_{Nz+1}^{n+1} - \boldsymbol{V}_{Nz+2}^{n+1}\right] \tag{5.17}$$

where $\boldsymbol{A} = \left[\frac{\boldsymbol{C}_m + \boldsymbol{C}_d}{\Delta t}\right]^{-1}$, $\boldsymbol{B} = \left[\boldsymbol{U} + \frac{\boldsymbol{D}}{\boldsymbol{R}_{lump}}\right]^{-1}$, $\boldsymbol{D} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{C}\right]^{-1}$, $\boldsymbol{E} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{L} + \frac{\Delta z}{2}\boldsymbol{R}\right]^{-1}$, $\boldsymbol{F} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{L} - \frac{\Delta z}{2}\boldsymbol{R}\right]$, $\boldsymbol{C}_m$ is the drain to gate coupling capacitance, $\boldsymbol{C}_d$ is the drain

diffusion capacitance of CMOS inverter, $\boldsymbol{I_p}$ and $\boldsymbol{I_n}$ are the PMOS and NMOS currents, respectively [120].

The expressions (5.10)-(5.17) are evaluated in a bootstrapping fashion. The process can be demonstrated with the flowchart shown in Figure 5.7. The proposed model can be easily extended to bigger circuits with more number of coupled lines by changing the dimensions of the parasitic, voltage and current matrices. To optimize the calculation time in the FDTD flow, the value of ê t must be considered as ê $t_{\max}$, so that the number of time steps can be minimized.

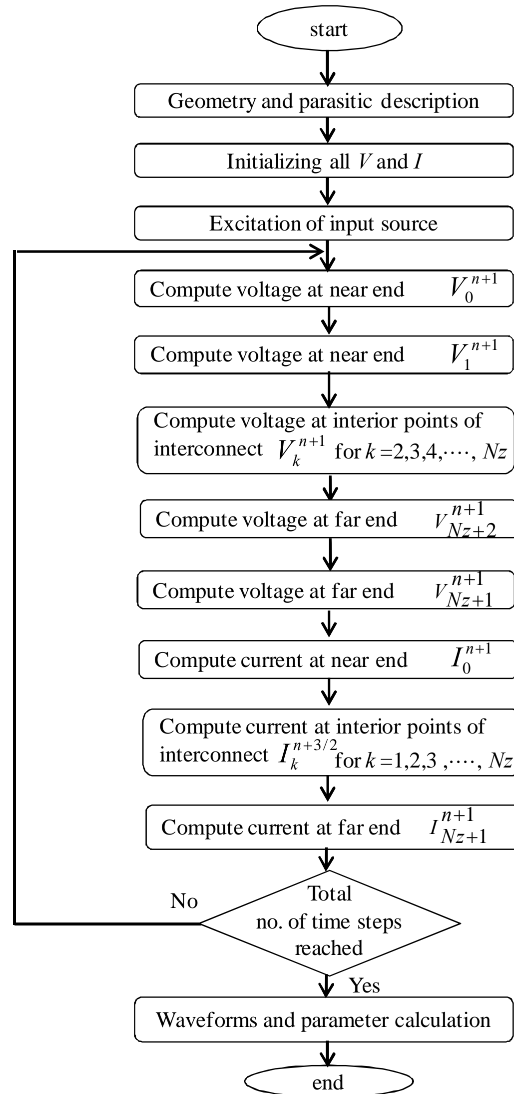


Figure 5.7. Flowchart for evaluation of voltage and current using the proposed FDTD technique.

5.4. Results and Discussion

The effective mean free path, resistance, propagation delay and the crosstalk induced delay of an MLGNR are analyzed by incorporating the width dependent MFP. Moreover, the performance of MLGNR interconnect is compared with Cu interconnect.

5.4.1 Analysis of Mean Free Path, Resistance and Propagation Delay with Rough Edges

The fundamental issue in GNR is the presence of edge roughness that substantially reduces the effective MFP. For rough edges, the electrons scatter at the edges, and hence, the effective MFP becomes width dependent. Therefore, width dependent MFP should be incorporated in the model of MLGNR resistance. Based on the improved model, this section demonstrates the impact of edge roughness on the performance of MLGNR interconnects.

The effective MFP, λ_{eff} is analyzed by considering the width dependent MFP for different values of edge roughness probabilities of MLGNR. The MFP due to defects and Fermi level are assumed to be 419 nm and 0.2 eV, respectively. The values of λ_{eff} are calculated using Eq. (5.5) and the results are shown in Figure 5.8. It is observed that the edge roughness reduces the MFP by more than one order of magnitude, particularly for narrow widths. However, the reduction of MFP is highly dependent on the back scattering probability (P).

The scattering resistance of MLGNR can be expressed as

$$r_{s,ESC} = \frac{h}{2e^2 N_{layer}} \left[\sum_{n} \left(\frac{l}{\lambda_{eff_n}} \right)^{-1} \right]^{-1} ;\ 0 < P \leq 1 \text{(rough edges)} \tag{5.18a}$$

$$r_{s,ESC} = \frac{h}{2e^2 N_{layer} N_{ch}} \left(\frac{l}{\lambda_d} \right);\ P = 0 \text{ (smooth edges)} \tag{5.18b}$$

Using (5.18a) and (5.18b), the scattering resistance of MLGNR for different widths and edge roughness probabilities is shown in Figure 5.9. The thickness and interconnect length are 56.9 nm and 100 m, respectively. The variation in the resistance is higher at narrow widths due to the dominating effect of edge scattering.

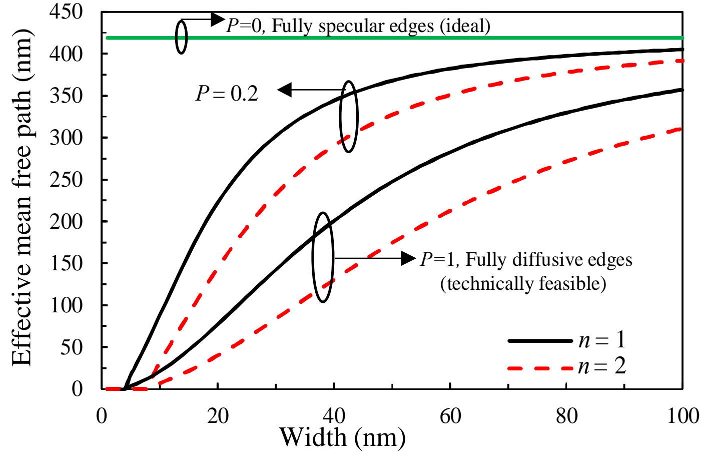


Figure 5.8. MFP of MLGNR for first two lowest sub-bands at different widths.

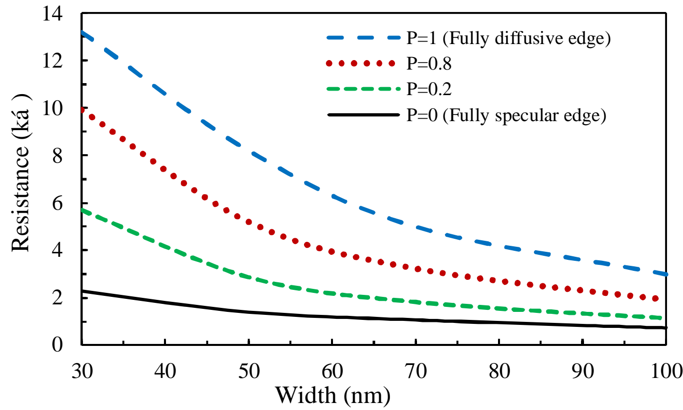


Figure 5.9. Resistance of MLGNR for different interconnect widths.

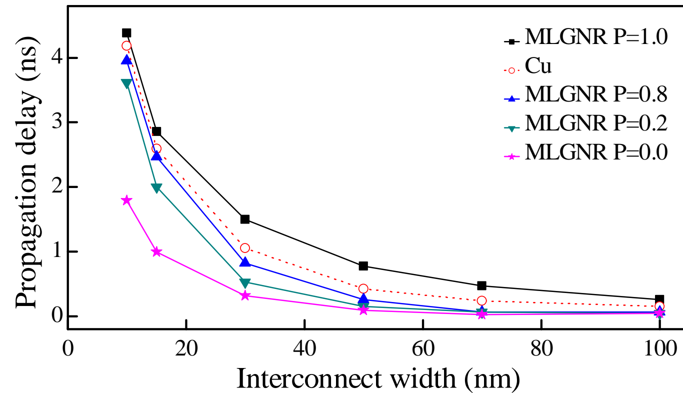


Figure 5.10. Propagation delay of MLGNR and Cu at t = 56.9 nm and l = 100 m.

For different values of P, the propagation delay of MLGNR and Cu at different interconnect widths is shown in Figure 5.10. It is observed that for wider MLGNR interconnects, the delay is almost constant for different edge roughness probabilities. It is due to a small variation in the scattering resistance for wider interconnects. It can also be observed that the propagation delay of MLGNR is higher than Cu for fully diffusive edge (P = 1).

5.4.2 Crosstalk Induced Delay

The coupled MLGNR interconnects performance is analyzed using the proposed model and the outcome is compared with the previously reported model [37], where the MFP is considered as independent of width. An industry standard HSPICE simulator is used for model validation. Considering the width dependent and width independent MFPs, the variation of crosstalk induced propagation delay with interconnect width during in-phase and out-phase transitions is shown in the Figures 5.11 (a) and (b), respectively. The dynamic crosstalk is analyzed by switching both lines in-phase and out-phase. The input signal rise and fall transition times are considered as 20 ps. For an interconnect length of 10 m, the interconnect width is varied from 10 nm to 60 nm, while keeping the thickness and spacing between the interconnect lines as 22 nm, and distance from the ground plane as 44 nm.

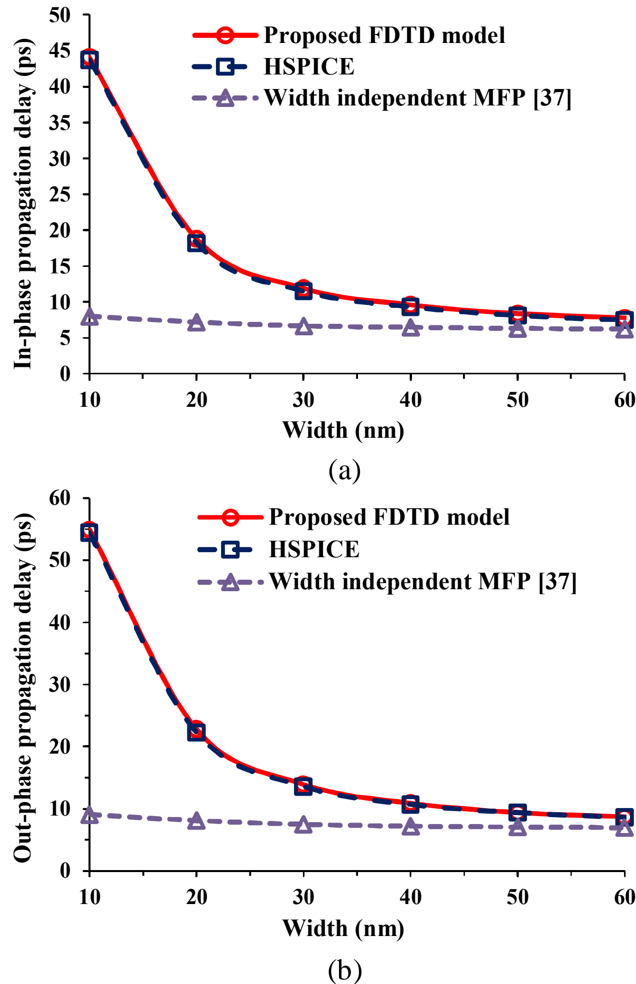


Figure 5.11. Crosstalk-induced propagation delay performance with change in interconnect width under (a) in-phase switching, and (b) out-phase switching.

From Figure 5.11, it can be observed that the width independent MFP model presented in [37] underestimates the propagation delay by 32%. Moreover, it is observed that this margin increases substantially for technology nodes having narrower interconnect widths. This is due to the prominent effect of edge scattering at smaller dimensions. Therefore, it is strongly recommended to include width dependent MFP for accurately modeling the crosstalk noise in MLGNR interconnects.

To further verify the robustness of the proposed model, the propagation delay comparison under in-phase and out-phase transitions on victim line 2 is observed in Figure 5.12 for different input transition times. It can be observed that the proposed model matches accurately with HSPICE simulations for all transition times. Moreover, the propagation delay during the out-phase transition is higher due to Miller capacitance effect.

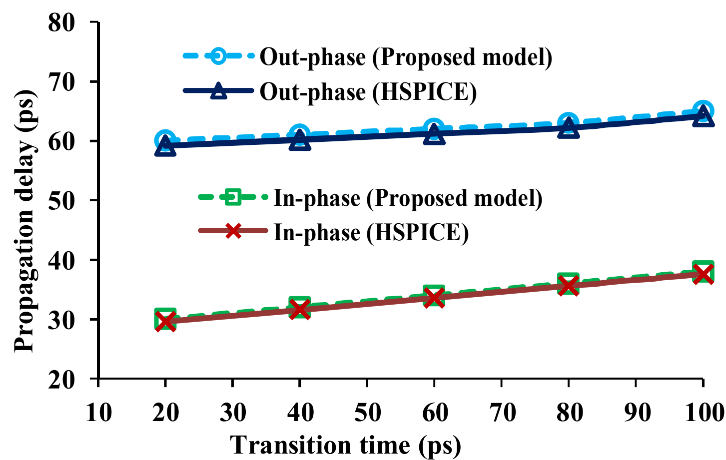


Figure 5.12. Variation of propagation delay with respect to input transition time.

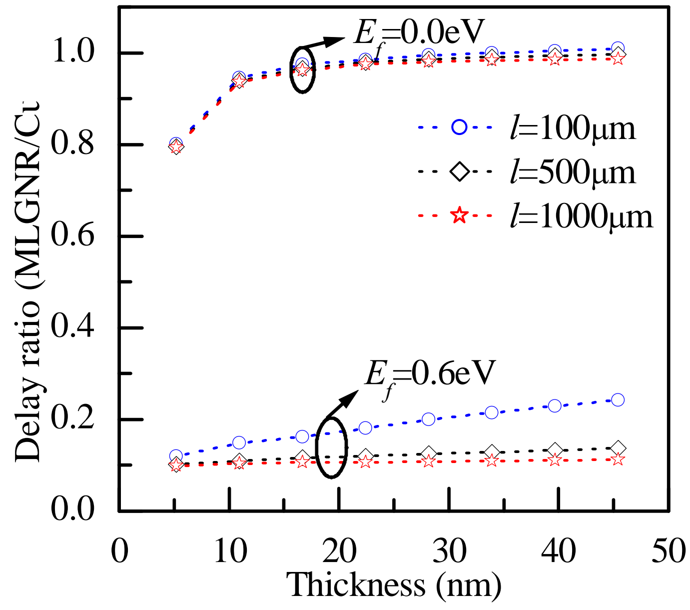
Using a PC with Pentium Dual Core CPU (2.33 GHz, 4 GB RAM), the runtime of the proposed model is compared with the HSPICE simulation time. Using the proposed model, it is observed that the CPU runtime reduces by an average of 95% in comparison to HSPICE simulations. For an interconnect length of 200 μm with 100-space and 1000-time segments, the runtime using proposed model is 0.36 s against 7.26 s using HSPICE.

5.4.3 Performance Comparison between Cu and MLGNR Interconnects

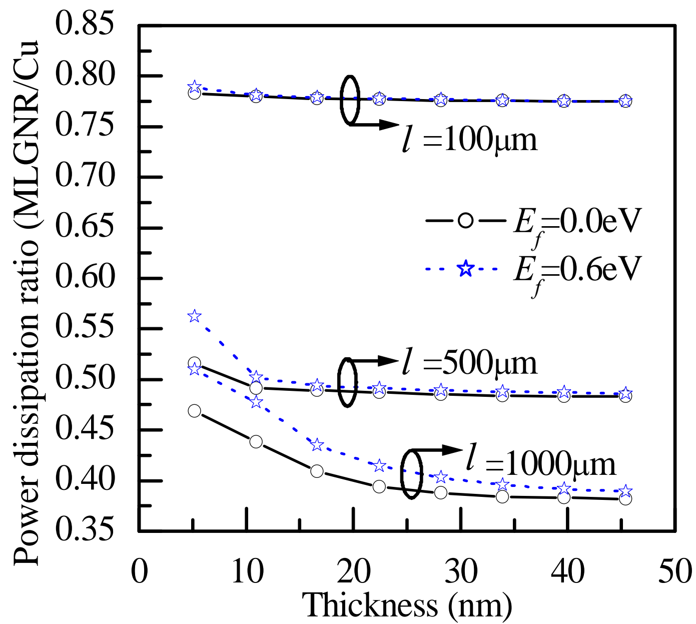
The propagation delay and power dissipation of MLGNR (neutral and doped) and Cu are analyzed for similar interconnect length, width and thickness. The mean free path, λ_d of neutral MLGNR is considered as 419 nm with in-plane conductivity of 0.026 (μ .cm)$^{-1}$, whereas an AsF_5 doped MLGNR can exhibit λ_d of 1.03 μm with in-plane conductivity of 0.63 (μ .cm)$^{-1}$ [106]. Figure 5.3 shows the DIL system wherein the interconnect line is represented by the ESC model of MLGNR. The *RLC* distributed model is used for analyzing the conventional Cu interconnects [4], [7], [178]. A CMOS driver with supply voltage of 0.9 V is used to drive the interconnect line that is terminated by a load capacitance of 10 fF. Using this setup, propagation delay and power dissipation are analyzed for different global interconnect lengths ranging from 100 μm to 1000 μm.

The propagation delay and power dissipation are proportional to the resistive and capacitive parasitics of interconnect. For different interconnect thickness, the MLGNR (neutral and doped) to Cu delay and power dissipation ratio are shown in Figures 5.13 (a) and 5.13 (b), respectively. It is observed that a thicker doped MLGNR demonstrates substantial reduction in delay and power dissipation compared to Cu interconnects. In doped MLGNR, the higher carrier concentration in each layer substantially increases the number of conducting channels that in turn drastically reduces the resistive parasitic ($r_{s,ESC}$) compared to Cu interconnects. Although, more number of conducting channels in doped MLGNR increases the quantum capacitance ($c_{q,ESC}$), but the equivalent capacitance (c_{ESC}) remains almost constant due to the dominating effect of ($c_{e,ESC}$) factor. Therefore, the cumulative effect of $r_{s,ESC}$ and c_{ESC} of doped MLGNR reduces the overall delay and power dissipation in comparison to Cu interconnects.

Table 5.3 summarizes the percentage reduction in propagation delay and power dissipation of doped MLGNR in comparison to Cu at different interconnect lengths. The reduction is more pronounced for longer interconnects due to a comparatively higher reduction in the line resistance. The overall delay and power dissipation of doped MLGNR are reduced by 86.13% and 43.72%, respectively, in comparison to the Cu interconnects.



(a)



(b)

Figure 5.13. MLGNR to Cu (a) delay and (b) power dissipation ratio at different interconnect thicknesses.

Table 5.3 Percentage reduction in propagation delay and power dissipation for doped MLGNR with respect to Cu interconnects

Thick-ness (nm)	% reduction in propagation delay of MLGNR *w.r.t.* Cu for interconnect lengths of			% reduction in power dissipation of MLGNR *w.r.t.* Cu for interconnect lengths		
	100 m	500 m	1000 m	100 m	500 m	1000 m
5.75	88.01	89.79	90.11	49.39	50.61	54.04
11.50	85.13	88.97	89.61	50.93	52.98	57.17
17.25	83.78	88.44	89.42	51.12	54.17	59.14
23.00	81.91	87.98	89.27	51.32	55.82	60.61
28.75	80.05	87.53	89.15	51.47	57.31	61.21
34.50	78.46	87.10	89.04	51.57	58.02	61.57
40.25	77.11	86.67	88.92	51.66	58.99	61.72
46.00	75.76	86.25	88.82	51.69	60.13	61.81

5.5. Summary

This chapter analyzed the performance of MLGNR as a potential candidate to replace the Cu for future VLSI interconnects. Based on the multiconductor transmission line theory, the ESC model of MLGNR is presented. In a more realistic manner, the proposed model incorporates the width dependent MFP parameter that helps in accurately estimating the crosstalk induced performance in comparison to the conventional model. The proposed ESC model is validated by comparing its transient response with respect to the response of MTL model.

The FDTD model is presented to analyze the crosstalk effects in coupled MLGNR interconnect lines. The results of the proposed model closely matches with that of HSPICE simulations. The average error in the propagation delay measurement is observed to be less than 2%. Moreover, it has been noticed that the width dependent MFP should be incorporated in a valid crosstalk noise modeling. In addition, the efficiency of the proposed model has also been demonstrated. It is observed that the model requires at an average only 5% of HSPICE simulation time. Based on the comparative study, it is observed that the MLGNR is the better suitable on-chip interconnect material than the Cu.

Chapter 6

An Efficient US-FDTD Model for Crosstalk Analysis of On-chip Interconnects

6.1 Introduction

The shrinking size of the transistors has resulted in gate delays being overshadowed by larger interconnect delays [7, 8]. Therefore, the overall chip performance is primarily dependent on the interconnect performance. The close proximity of interconnects in miniaturized microelectronic devices leads to crosstalk noise. The crosstalk noise may result in logic failure, circuit malfunction, change in signal propagation and unwanted power dissipation [12]. Therefore, accurate modeling of crosstalk noise has emerged as vital design criteria in microelectronics.

The FDTD technique is widely used to solve electromagnetic wave problems. It is a fast, accurate and robust technique, which involves discretization of electromagnetic fields in both space and time domains [43], [179, 180]. Recently, the application of this versatile technique has been extended to high-speed interconnect domain [181]. However, in the FDTD technique to ensure a stable operation, the time step size (Δt) is limited by the Courant-Friedrichs-Lewy (CFL) stability condition *i.e.*, ê $t \leq$ ê t_{max}, where ê t_{max} = ê z/v_{max}, the terms ê z and v_{max} represent the space step size and the maximum phase velocity, respectively [182, 183]. Consequently, the conventional FDTD techniques [21], [42], [181] consume large memory space and power due to the enormous number of iterations required for the analysis. Hence, beyond the CFL condition, the FDTD technique is unstable and within it, the technique is not efficient.

The improvements in FDTD technique can be easily addressed if the CFL stability condition is removed. Recently, several researchers have proposed various modified FDTD techniques to overcome the CFL stability criteria based on different algorithms, such as alternating direction implicit (ADI)-FDTD [184, 185], split-step FDTD [186, 187], Crank-Nicolson (CN)-FDTD [188, 189] and others [190-192]. All these techniques [184-192] were developed for transmission lines that are usually

excited and terminated by resistive drivers and resistive loads, respectively. However, the VLSI interconnects are driven and terminated by the non-linear CMOS drivers and capacitive loads, respectively. Therefore, the existing unconditionally stable FDTD techniques are not suitable to analyze the performance of CMOS gate driven VLSI interconnects.

In this chapter, a novel model is proposed that successfully implements an unconditionally stable FDTD (US-FDTD) technique to analyze the comprehensive crosstalk effects of coupled VLSI interconnects. The interconnect lines are driven by the non-linear CMOS driver that are modeled by the modified Alpha power law model, which includes the drain conductance parameter. The crosstalk induced performance parameters such as noise peak voltage, noise width and delay are analyzed. The proposed model is compared against the conventional FDTD model for accuracy, efficiency and stability.

The remaining chapter is organized as follows: Section 6.2 details the implementation of the US-FDTD technique for coupled interconnect lines. Moreover, the unconditional stability of the model is also scrutinized. Section 6.3 analyzes the crosstalk noise and validates the accuracy and efficiency of the proposed model. Moreover, to verify the unconditional stability of the proposed model the transient analysis is carried out at different values of time step. The performance of Cu, MWCNT and MLGNR interconnects is compared in Section 6.4. Finally, Section 6.5 concludes the chapter.

6.2 Development of Proposed US-FDTD Model

This section deals with the development of US-FDTD model for the coupled on-chip interconnects. The interconnect lines are coupled capacitively and inductively. In a more realistic manner, the CMOS drivers are considered for accurate performance analysis. The interconnect lines are terminated by capacitive loads. The schematic view of coupled interconnect lines is shown in Figure 6.1, where the line x and the line y represent the aggressor and victim lines, respectively.

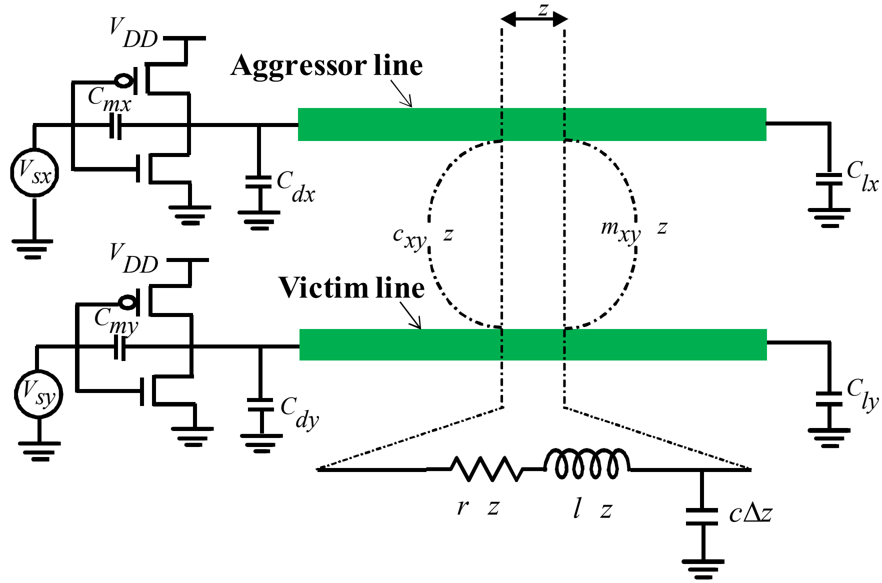


Figure 6.1. Schematic view of coupled interconnects driven by CMOS drivers.

6.2.1 Modeling of Coupled On-chip Interconnects

The interconnect lines are represented by the transmission lines that are coupled capacitively, c_{xy} and inductively, m_{xy}. The telegrapherøs equations in the transverse electro-magnetic mode of coupled lines, at any point z along the line, is represented as

$$\frac{\partial v_x(z,t)}{\partial z} + r_x i_x(z,t) + l_x \frac{\partial i_x(z,t)}{\partial t} + m_{xy} \frac{\partial i_y(z,t)}{\partial t} = 0 \tag{6.1a}$$

$$\frac{\partial v_y(z,t)}{\partial z} + r_y i_y(z,t) + l_y \frac{\partial i_y(z,t)}{\partial t} + m_{xy} \frac{\partial i_x(z,t)}{\partial t} = 0 \tag{6.1b}$$

$$\frac{\partial i_x(z,t)}{\partial z} + c_x \frac{\partial v_x(z,t)}{\partial t} + c_{xy} \frac{\partial v_x(z,t)}{\partial t} - c_{xy} \frac{\partial v_y(z,t)}{\partial t} = 0 \tag{6.1c}$$

$$\frac{\partial i_y(z,t)}{\partial z} + c_y \frac{\partial v_y(z,t)}{\partial t} + c_{xy} \frac{\partial v_y(z,t)}{\partial t} - c_{xy} \frac{\partial v_x(z,t)}{\partial t} = 0 \tag{6.1d}$$

Representing equations (6.1a) and (6.1b) in matrix form results in

$$\frac{\partial \boldsymbol{v}(z,t)}{\partial z} + \boldsymbol{r}\boldsymbol{i}(z,\mathrm{t}) + \boldsymbol{l} \frac{\partial \boldsymbol{i}(z,t)}{\partial t} = \mathbf{0} \tag{6.2a}$$

where v and i are evaluated in 2×1 matrix form as $v = [v_x, v_y]^{\mathrm{T}}$, $i = [i_x, i_y]^{\mathrm{T}}$, r and l are evaluated in 2×2 matrix form as

$$\boldsymbol{r} = \begin{pmatrix} r_x & 0 \\ 0 & r_y \end{pmatrix}, \ \boldsymbol{l} = \begin{pmatrix} l_x & m_{xy} \\ m_{xy} & l_y \end{pmatrix}$$

Representing equations (6.1c) and (6.1d) in matrix form results in

$$\frac{\partial \boldsymbol{i}(z,t)}{\partial z} + \boldsymbol{c}\frac{\partial \boldsymbol{v}(z,t)}{\partial t} = \boldsymbol{0} \tag{6.2b}$$

where c is evaluated in 2×2 matrix form as $\boldsymbol{c} = \begin{pmatrix} c_x + c_{xy} & -c_{xy} \\ -c_{xy} & c_y + c_{xy} \end{pmatrix}$

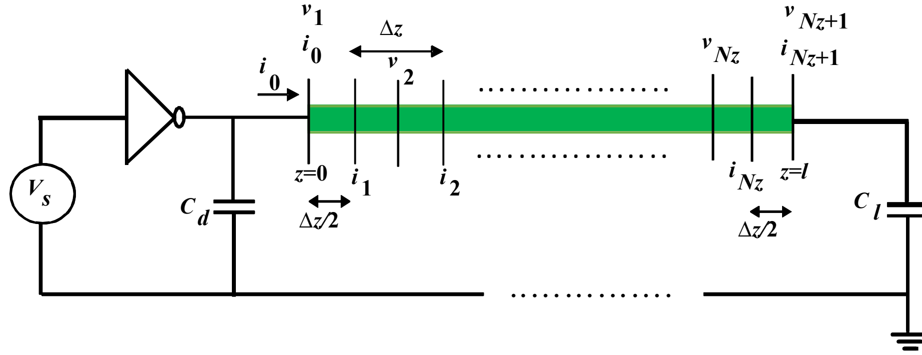


Figure 6.2. Representation of space discretization of an interconnect line for unconditionally stable FDTD technique. The total interconnect length is divided into N_z number of sections, each with a uniform length of Δz.

Figure 6.2 represents the space discretization of an interconnect line. Using the forward difference approximation in space domain, equation (6.2a) results in

$$\frac{\boldsymbol{v}_{k+1} - \boldsymbol{v}_k}{\Delta z} = -\boldsymbol{r}\boldsymbol{i}_k - \boldsymbol{l}\frac{\partial \boldsymbol{i}_k}{\partial t} \tag{6.3a}$$

For $k = 1, 2, \cdots\cdots, N_z$, equation (6.3a) can be rearranged as

$$\boldsymbol{v}_{k+1} - \boldsymbol{v}_k + \boldsymbol{r}\ \ z\boldsymbol{i}_k + \boldsymbol{l}\Delta z\frac{\partial \boldsymbol{i}_k}{\partial t} = \boldsymbol{0} \tag{6.3b}$$

Using the backward difference approximation in space domain, equation (6.2b) results in

$$\frac{\boldsymbol{i}_k - \boldsymbol{i}_{k-1}}{\Delta z} = -\boldsymbol{c}\frac{\partial \boldsymbol{v}_k}{\partial t} \tag{6.4}$$

For k = 1 and k = Nz+1, the space segment is replaced by $\Delta z/2$ (Figure 6.2).

For k = 1, equation (6.4) results in

$$\boldsymbol{i}_1 - \boldsymbol{i}_0 + \frac{\boldsymbol{c}\ \ z}{2}\frac{\partial \boldsymbol{v}_1}{\partial t} = \boldsymbol{0} \tag{6.5a}$$

For $k = Nz+1$, equation (6.4) results in

$$\boldsymbol{i}_{Nz+1} - \boldsymbol{i}_{Nz} + \frac{\boldsymbol{c}\Delta z}{2} \frac{\partial \boldsymbol{v}_{Nz+1}}{\partial t} = \boldsymbol{0} \tag{6.5b}$$

For $k = 2, 3, \cdots\cdots, Nz$, equation (6.4) results in

$$\boldsymbol{i}_k - \boldsymbol{i}_{k-1} + \boldsymbol{c}\Delta z \frac{\partial \boldsymbol{v}_k}{\partial t} = \boldsymbol{0} \tag{6.5c}$$

Equations (6.5a) and (6.5b) are further modified after applying the boundary conditions, as illustrated in the following sub-sections 6.6.2 and 6.6.3.

6.2.2 Modeling of CMOS Driver

The CMOS drivers are modeled by modified alpha power law model that incorporates the effect of velocity saturation along with the finite drain conductance parameter. As shown in Figure 6.1, the parasitic capacitances C_m and C_d represent gate to drain coupling capacitance and drain diffusion capacitance, respectively. The NMOS and PMOS transistors can operate in either cutoff, linear or saturation regions depending on the input voltage signal [193] as depicted in Figure 6.3.

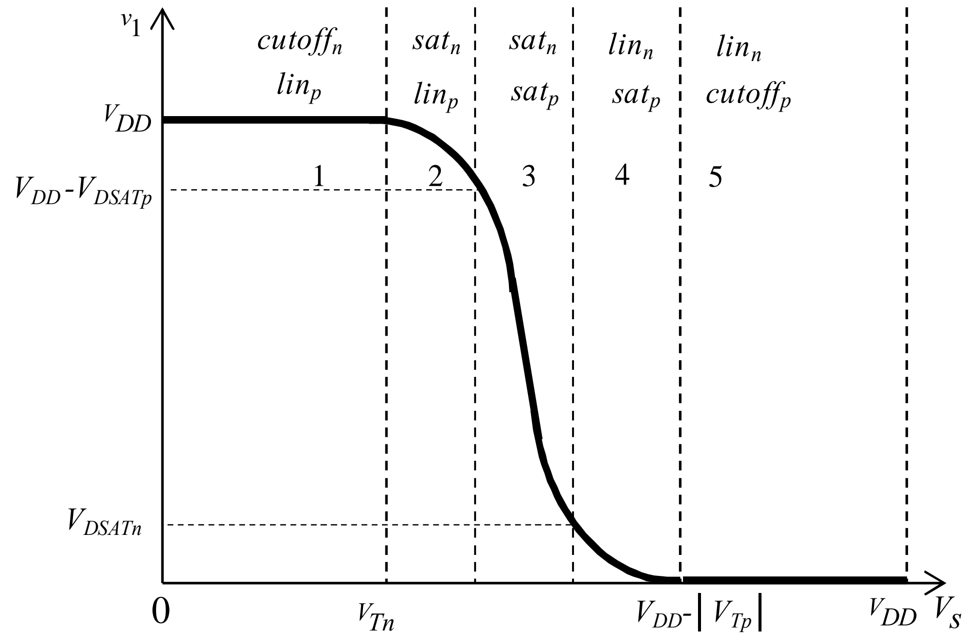


Figure 6.3. The five regions of operation of a CMOS inverter. The subscripts *n* and *p* denote NMOS and PMOS, respectively.

The current equations of the MOS transistors are

$$\boldsymbol{I}_n = \begin{cases} \mathbf{0} & (cutoff) \\ \boldsymbol{M}_{Ln}\left(\boldsymbol{V}_S - \boldsymbol{V}_{Tn}\right)^{\alpha_n/2} \boldsymbol{v}_1 & (lin) \\ \boldsymbol{M}_{Sn}\left(\boldsymbol{V}_S - \boldsymbol{V}_{Tn}\right)^{\alpha_n}\left(\boldsymbol{U} + \sigma_n \boldsymbol{v}_1\right) & (sat) \end{cases} \tag{6.6}$$

$$\boldsymbol{I}_p = \begin{cases} \mathbf{0} & (cutoff) \\ \boldsymbol{M}_{Lp}\left(\boldsymbol{V}_{DD} - \boldsymbol{V}_S - \left|\boldsymbol{V}_{Tp}\right|\right)^{\alpha_p/2}\left(\boldsymbol{V}_{DD} - \boldsymbol{v}_1\right) & (lin) \\ \boldsymbol{M}_{Sp}\left(\boldsymbol{V}_{DD} - \boldsymbol{V}_S - \left|\boldsymbol{V}_{Tp}\right|\right)^{\alpha_p}\left(\boldsymbol{U} + \sigma_p(\boldsymbol{V}_{DD} - \boldsymbol{v}_1)\right) & (sat) \end{cases} \tag{6.7}$$

where $\boldsymbol{U}$ is a 2×2 identity matrix, M_{Ln} (M_{Lp}), M_{Sn} (M_{Sp}), α_n (α_p), σ_n (σ_p) and V_{Tn} (V_{Tp}) are the linear region transconductance parameter, saturation region transconductance parameter, velocity saturation index, drain conductance parameter and the threshold voltage of NMOS (PMOS), respectively. The model parameters of NMOS/PMOS transistor at 32 nm technology node are listed in Table 6.1.

Table 6.1 Model parameters for 32 nm node

Parameter	**PMOS**	**NMOS**
M_L	0.006	0.007
M_S	0.875105×10^{-3}	1.944973×10^{-3}
α	1.0788	0.91503
σ	2.685	0.876
V_T	0.36	0.35

6.2.3 Modeling of Driver-Interconnect-Load

In this sub-section, the near-end and far-end interconnect terminal conditions are incorporated in the current equations. At the near-end terminal (k = 1), applying Kirchhofføs current law, the source current i_0 can be expressed as

$$\boldsymbol{i}_0 = \boldsymbol{I}_p - \boldsymbol{I}_n + \boldsymbol{C}_m\left(\frac{d(\boldsymbol{V}_S - \boldsymbol{v}_1)}{dt}\right) - \boldsymbol{C}_d\frac{d\boldsymbol{v}_1}{dt} \tag{6.8}$$

Incorporating equation (6.8) in equation (6.5a) results in

$$\boldsymbol{i}_1 - \boldsymbol{I}_p + \boldsymbol{I}_n - \boldsymbol{C}_m\left(\frac{d(\boldsymbol{V}_S - \boldsymbol{v}_1)}{dt}\right) + \boldsymbol{C}_d\frac{d\boldsymbol{v}_1}{dt} + \frac{\boldsymbol{c}\Delta z}{2}\frac{\partial \boldsymbol{v}_1}{\partial t} = \mathbf{0} \tag{6.9}$$

At the far-end terminal ($k = Nz+1$), the load current i_{Nz+1} can be expressed as

$$\boldsymbol{i}_{N_z+1} = \boldsymbol{C}_l \frac{\partial \boldsymbol{v}_{Nz+1}}{\partial t} \tag{6.10}$$

Incorporating equation (6.10) in (6.5b) results in

$$\boldsymbol{i}_{Nz} - \left(\frac{\boldsymbol{c}\Delta z}{2} + \boldsymbol{C}_l \right) \frac{\partial \boldsymbol{v}_{Nz+1}}{\partial t} = \boldsymbol{0} \tag{6.11}$$

Representing equations (6.9), (6.5c) and (6.11) together in the matrix form results in

$$\boldsymbol{PI} + \boldsymbol{GV} + \boldsymbol{C} \frac{\partial \boldsymbol{V}}{\partial t} = \boldsymbol{I}_s + \boldsymbol{X}_r \frac{\partial \boldsymbol{V}_r}{\partial t} \tag{6.12}$$

where $\boldsymbol{P} = \begin{pmatrix} \boldsymbol{U} & \boldsymbol{0} & \cdots & \boldsymbol{0} & \boldsymbol{0} \\ -\boldsymbol{U} & \boldsymbol{U} & \cdots & \boldsymbol{0} & \boldsymbol{0} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \boldsymbol{0} & \boldsymbol{0} & \cdots & -\boldsymbol{U} & \boldsymbol{U} \\ \boldsymbol{0} & \boldsymbol{0} & \cdots & \boldsymbol{0} & -\boldsymbol{U} \end{pmatrix}_{2(Nz+1)\times 2Nz}$, $\boldsymbol{G} = \begin{pmatrix} \boldsymbol{E}_1 & \boldsymbol{0} & \cdots & \boldsymbol{0} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{0} & \ddots & \vdots & \boldsymbol{0} \\ \vdots & \ddots & \ddots & \boldsymbol{0} & \boldsymbol{0} \\ \boldsymbol{0} & \ddots & \ddots & \boldsymbol{0} & \vdots \\ \boldsymbol{0} & \boldsymbol{0} & \cdots & \boldsymbol{0} & \boldsymbol{0} \end{pmatrix}_{2(Nz+1)\times 2(Nz+1)}$,

$$\boldsymbol{C} = \begin{pmatrix} \frac{\boldsymbol{c}\Delta z}{2} + \boldsymbol{C}_d + \boldsymbol{C}_m & \boldsymbol{0} & \boldsymbol{0} & \cdots & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{c}\Delta z & \ddots & \ddots & \boldsymbol{0} \\ \vdots & \boldsymbol{0} & \ddots & \boldsymbol{0} & \vdots \\ \boldsymbol{0} & \vdots & \ddots & \boldsymbol{c}\Delta z & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{0} & \cdots & \boldsymbol{0} & \frac{\boldsymbol{c}\Delta z}{2} + \boldsymbol{C}_l \end{pmatrix}_{2(Nz+1)\times 2(Nz+1)},$$

$\boldsymbol{I}_s = \begin{pmatrix} \boldsymbol{E}_2 \\ \boldsymbol{0} \\ \vdots \\ \vdots \\ \boldsymbol{0} \end{pmatrix}_{2(N_z+1)\times 1}$, $\boldsymbol{I} = \begin{pmatrix} \boldsymbol{i}_1 \\ \boldsymbol{i}_2 \\ \vdots \\ \vdots \\ \boldsymbol{i}_{Nz} \end{pmatrix}_{2Nz\times 1}$, $\boldsymbol{V}_r = \begin{pmatrix} \boldsymbol{V}_s \\ \boldsymbol{0} \\ \vdots \\ \vdots \\ \boldsymbol{0} \end{pmatrix}_{2(Nz+1)\times 1}$, $\boldsymbol{V} = \begin{pmatrix} \boldsymbol{v}_1 \\ \boldsymbol{v}_2 \\ \vdots \\ \vdots \\ \boldsymbol{v}_{Nz+1} \end{pmatrix}_{2(Nz+1)\times 1}$,

$$\boldsymbol{X}_r = \begin{pmatrix} \boldsymbol{C}_m & \boldsymbol{0} & \cdots & \cdots & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{0} & \ddots & \ddots & \boldsymbol{0} \\ \vdots & \vdots & \ddots & \ddots & \vdots \\ \vdots & \vdots & \ddots & \ddots & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{0} & \cdots & \boldsymbol{0} & \boldsymbol{0} \end{pmatrix}_{2(Nz+1)\times 2(Nz+1)},$$

The values of E_1 and E_2 are dependent on the operating region of CMOS inverter and can be obtained from Table 6.2.

Table 6.2 E_1 and E_2 for different regions of operation

Region	$\boldsymbol{E_1}$	$\boldsymbol{E_2}$
1	$\boldsymbol{M}_{Lp}\left(V_{DD}-V_s-\lvert V_{Tp}\rvert\right)^{\alpha_p/2}$	$\boldsymbol{M}_{Lp}\left(V_{DD}-V_s-\lvert V_{Tp}\rvert\right)^{\alpha_p/2}V_{DD}$
2	$\boldsymbol{M}_{Lp}\left(V_{DD}-V_s-\lvert V_{Tp}\rvert\right)^{\alpha_p/2}+$ $\sigma_n\boldsymbol{M}_{Sn}\left(V_s-V_{Tn}\right)^{\alpha_n}$	$\boldsymbol{M}_{Lp}\left(V_{DD}-V_s-\lvert V_{Tp}\rvert\right)^{\alpha_p/2}V_{DD}-$ $\boldsymbol{M}_{Sn}\left(V_s-V_{Tn}\right)^{\alpha_n}$
3	$\sigma_p\boldsymbol{M}_{Sp}\left(V_{DD}-V_s-\lvert V_{Tp}\rvert\right)^{\alpha_p}+$ $\sigma_n\boldsymbol{M}_{Sn}\left(V_s-V_{Tn}\right)^{\alpha_n}$	$\boldsymbol{M}_{Sp}\left(V_{DD}-V_s-\lvert V_{Tp}\rvert\right)^{\alpha_p}+$ $\sigma_p\boldsymbol{M}_{Sp}\left(V_{DD}-V_s-\lvert V_{Tp}\rvert\right)^{\alpha_p}V_{DD}-$ $\boldsymbol{M}_{Sn}\left(V_s-V_{Tn}\right)^{\alpha_n}$
4	$\boldsymbol{M}_{Ln}\left(V_s-V_{Tn}\right)^{\alpha_n/2}+$ $\sigma_p\boldsymbol{M}_{Sp}\left(V_{DD}-V_s-\lvert V_{Tp}\rvert\right)^{\alpha_p}$	$\boldsymbol{M}_{Sp}\left(V_{DD}-V_s-\lvert V_{Tp}\rvert\right)^{\alpha_p}+$ $\sigma_p\boldsymbol{M}_{Sp}\left(V_{DD}-V_s-\lvert V_{Tp}\rvert\right)^{\alpha_p}V_{DD}$
5	$\boldsymbol{M}_{Ln}\left(V_s-V_{Tn}\right)^{\alpha_n/2}$	0

Representing equation (6.3b) in matrix form results in

$$\boldsymbol{QV}+\boldsymbol{RI}+\boldsymbol{L}\frac{\partial \boldsymbol{I}}{\partial t}=\boldsymbol{0} \tag{6.13}$$

where $\boldsymbol{Q}=\begin{pmatrix} -\boldsymbol{U} & \boldsymbol{U} & \boldsymbol{0} & \boldsymbol{0} & \cdots & \boldsymbol{0} \\ \boldsymbol{0} & -\boldsymbol{U} & \boldsymbol{U} & \ddots & \ddots & \boldsymbol{0} \\ \vdots & \ddots & \ddots & \ddots & \boldsymbol{0} & \vdots \\ \boldsymbol{0} & \ddots & \ddots & -\boldsymbol{U} & \boldsymbol{U} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{0} & \cdots & \boldsymbol{0} & -\boldsymbol{U} & \boldsymbol{U} \end{pmatrix}_{2Nz\times 2(Nz+1)}$, $\boldsymbol{R}=\begin{pmatrix} \boldsymbol{r}\Delta z & \boldsymbol{0} & \cdots & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{r}\Delta z & \ddots & \vdots \\ \vdots & \ddots & \ddots & \boldsymbol{0} \\ \boldsymbol{0} & \cdots & \boldsymbol{0} & \boldsymbol{r}\Delta z \end{pmatrix}_{2Nz\times 2Nz}$,

$$\boldsymbol{L}=\begin{pmatrix} \boldsymbol{l}\Delta z & \boldsymbol{0} & \cdots & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{l}\Delta z & \ddots & \vdots \\ \vdots & \ddots & \ddots & \boldsymbol{0} \\ \boldsymbol{0} & \cdots & \boldsymbol{0} & \boldsymbol{l}\Delta z \end{pmatrix}_{2Nz\times 2Nz}$$

Applying finite difference in time domain to equations (6.12) and (6.13)

$$\boldsymbol{P}\frac{\boldsymbol{I}^{n+1}+\boldsymbol{I}^{n}}{2}+\boldsymbol{G}\frac{\boldsymbol{V}^{n+1}+\boldsymbol{V}^{n}}{2}+\boldsymbol{C}\frac{\boldsymbol{V}^{n+1}-\boldsymbol{V}^{n}}{\Delta t}=\frac{\boldsymbol{I}_s^{n+1}+\boldsymbol{I}_s^{n}}{2}+\boldsymbol{X}_r\frac{\boldsymbol{V}_r^{\,n+1}-\boldsymbol{V}_r^{\,n}}{\Delta t} \tag{6.14}$$

$$\boldsymbol{Q}\frac{\boldsymbol{V}^{n+1}+\boldsymbol{V}^{n}}{2}+\boldsymbol{R}\frac{\boldsymbol{I}^{n+1}+\boldsymbol{I}^{n}}{2}+\boldsymbol{L}\frac{\boldsymbol{I}^{n+1}-\boldsymbol{I}^{n}}{\Delta t}=\boldsymbol{0} \tag{6.15}$$

Solving equations (6.14) and (6.15) results in

$$\boldsymbol{V}^{n+1} = \boldsymbol{K}_1 \left(\frac{\boldsymbol{I}_S^{n+1} + \boldsymbol{I}_S^n}{2} + \boldsymbol{X}_r \frac{\boldsymbol{V}_r^{n+1} - \boldsymbol{V}_r^{n}}{\Delta t} - \boldsymbol{K}_2 \boldsymbol{V}^n - \boldsymbol{K}_3 \boldsymbol{I}^n \right) \tag{6.16}$$

$$\boldsymbol{I}^{n+1} = -\boldsymbol{K}_4 \left(\boldsymbol{K}_5 \boldsymbol{I}^n + \boldsymbol{K}_6 \left(\boldsymbol{V}^{n+1} + \boldsymbol{V}^n \right) \right) \tag{6.17}$$

where $\boldsymbol{K}_1 = \left(\left(\frac{\boldsymbol{G}}{2} + \frac{\boldsymbol{C}}{\Delta t} \right) - \frac{\boldsymbol{P}}{4} \boldsymbol{K}_4 \boldsymbol{Q} \right)^{-1}$, $\boldsymbol{K}_2 = \left(\left(\frac{\boldsymbol{G}}{2} - \frac{\boldsymbol{C}}{\Delta t} \right) - \frac{\boldsymbol{P}}{4} \boldsymbol{K}_4 \boldsymbol{Q} \right)$, $\boldsymbol{K}_3 = \left(\frac{\boldsymbol{P}}{2} - \frac{\boldsymbol{P}}{2} \boldsymbol{K}_4 \boldsymbol{K}_5 \right)$,

$\boldsymbol{K}_4 = \left(\frac{\boldsymbol{R}}{2} + \frac{\boldsymbol{L}}{\Delta t} \right)^{-1}$, $\boldsymbol{K}_5 = \left(\frac{\boldsymbol{R}}{2} - \frac{\boldsymbol{L}}{\Delta t} \right)$, $\boldsymbol{K}_6 = \frac{\boldsymbol{Q}}{2}$

Initially, the voltage and current values of interconnect line are set to zero. After exciting the input voltage source, the voltages along the line are evaluated for a specific time using (6.16) in terms of the previous values of voltage and current. Thereafter, the currents are evaluated using (6.17), in terms of these voltages and previous current values. The process is continued till the final time step is reached. This procedure can be demonstrated with the flowchart shown in Figure 6.4.

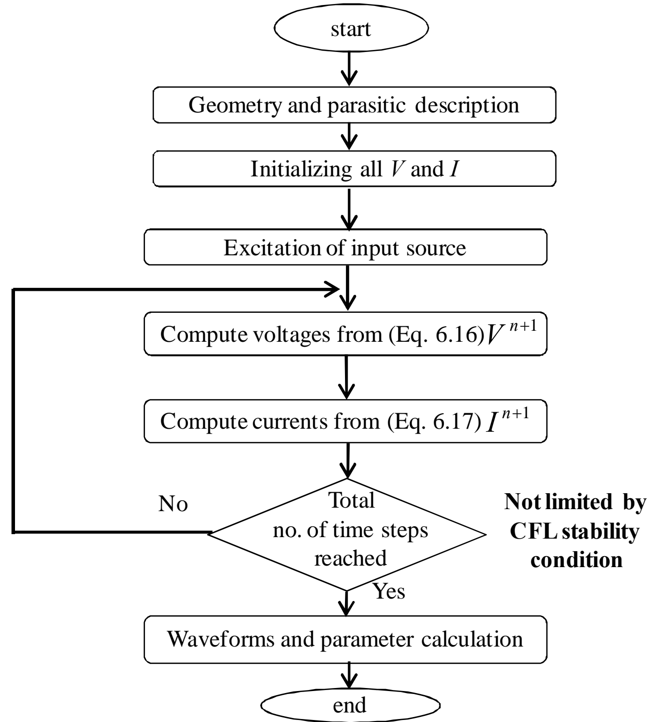


Figure 6.4. Flowchart for evaluation of voltage and current using the proposed US-FDTD technique.

From equations (6.16) and (6.17), it can be observed that these equations are in implicit form and hence free from stability condition. Moreover, the conductance parameter (***g***) can be incorporated in the proposed model without affecting the unconditional stability criteria.

6.2.4 Stability Analysis

This sub-section analytically demonstrates that the proposed US-FDTD model is not limited by the CFL stability condition and is unconditionally stable. Representing equations (6.12) and (6.13) together in matrix form results in

$$\boldsymbol{A}\boldsymbol{M} + \boldsymbol{B}\frac{\partial \boldsymbol{M}}{\partial t} = \tilde{\boldsymbol{I}}_s + \tilde{\boldsymbol{X}}_r \frac{\partial \tilde{\boldsymbol{V}}_r}{\partial t} \qquad (6.18)$$

where $\boldsymbol{A} = \begin{pmatrix} \boldsymbol{G} & \boldsymbol{P} \\ \boldsymbol{Q} & \boldsymbol{R} \end{pmatrix}$, $\boldsymbol{B} = \begin{pmatrix} \boldsymbol{C} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{L} \end{pmatrix}$, $\tilde{\boldsymbol{I}}_s = \begin{pmatrix} \boldsymbol{I}_s \\ \boldsymbol{0} \end{pmatrix}$, $\tilde{\boldsymbol{X}}_r = \begin{pmatrix} \boldsymbol{X}_r \\ \boldsymbol{0} \end{pmatrix}$, $\tilde{\boldsymbol{V}}_r = \begin{pmatrix} \boldsymbol{V}_r \\ \boldsymbol{0} \end{pmatrix}$, $\boldsymbol{M} = \begin{pmatrix} \boldsymbol{V} \\ \boldsymbol{I} \end{pmatrix}$

Performing finite difference in time domain, the equation (6.18) results in

$$\boldsymbol{A}\frac{\boldsymbol{M}^{n+1} + \boldsymbol{M}^{n}}{2} + \boldsymbol{B}\frac{\boldsymbol{M}^{n+1} - \boldsymbol{M}^{n}}{t} = \frac{\tilde{\boldsymbol{I}}_s^{n+1} + \tilde{\boldsymbol{I}}_s^{n}}{2} + \tilde{\boldsymbol{X}}_r \frac{\tilde{\boldsymbol{V}}_r^{n+1} - \tilde{\boldsymbol{V}}_r^{n}}{t} \qquad (6.19a)$$

After rearranging, equation (6.19a) results in

$$\boldsymbol{M}^{n+1} = \boldsymbol{X}\boldsymbol{M}^{n} + \left(\frac{\boldsymbol{A}}{2} + \frac{\boldsymbol{B}}{\Delta t}\right)^{-1}\left(\frac{\tilde{\boldsymbol{I}}_s^{n+1} + \tilde{\boldsymbol{I}}_s^{n}}{2} + \tilde{\boldsymbol{X}}_r \frac{\tilde{\boldsymbol{V}}_r^{n+1} - \tilde{\boldsymbol{V}}_r^{n}}{t}\right) \qquad (6.19b)$$

where $\boldsymbol{X} = \left(\frac{\boldsymbol{A}}{2} + \frac{\boldsymbol{B}}{\Delta t}\right)^{-1}\left(\frac{\boldsymbol{B}}{\Delta t} - \frac{\boldsymbol{A}}{2}\right)$

The matrix X is known as the amplification matrix of equation (6.19b). The model is stable if $\rho(X)$ Ö 1, where $\rho(X)$ represents the spectral radius of X and can be expressed as [194]

$$\rho(\boldsymbol{X}) = \max(|\, eigen(\boldsymbol{X}) \,|) \qquad (6.20)$$

With the increase in time step size, beyond the CFL limit, the conventional FDTD techniques [21], [42], [181] results in instability. However, for the proposed model the value of (6.20) is always less than 1 for all values of time step. Considering the worst case of the time step size, tending to infinity, the amplification matrix of the proposed US-FDTD model tends to identity matrix that has spectral radius of 1. Therefore, the proposed model is stable for any value of the time step size and hence, unconditionally stable.

The stability of the proposed model is analyzed based on the value of $\rho(X)$, which is calculated from equation (6.20). Figure 6.5 shows the comparison of $\rho(X)$ between the proposed US-FDTD model and conventional FDTD model, at different time steps. It is observed that when Δt is greater than the CFL limit ($\Delta t_{\max}$), for the conventional FDTD model, $\rho(X) > 1$, whereas for the proposed US-FDTD model, $\rho(X) < 1$. Therefore, the proposed model is stable beyond the CFL stability condition as well. The numerical example that demonstrates the unconditional stability of the proposed model is provided in section 6.3.3.

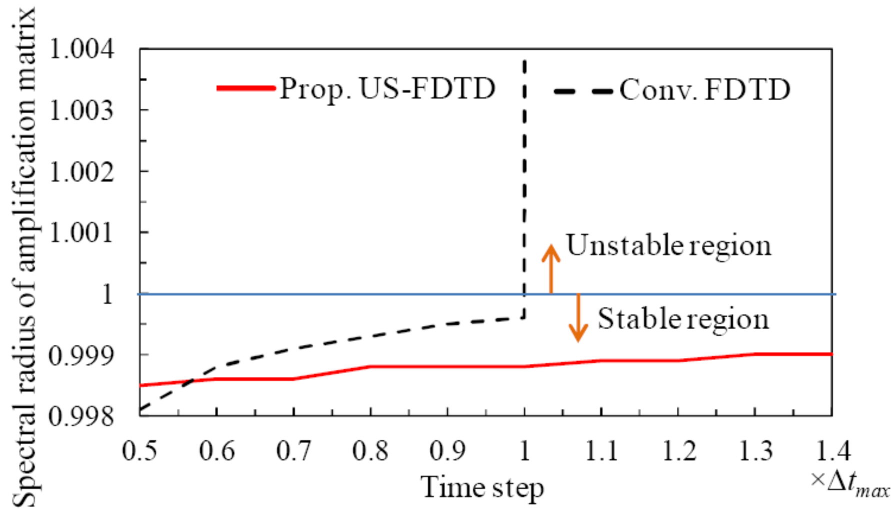


Figure 6.5. Comparison of spectral radius of amplification matrix between proposed US-FDTD and conventional FDTD model.

6.3 Simulation Setup and Results

The proposed US-FDTD model is validated with the conventional FDTD model. Using the 32 nm technology, the width and thickness of the interconnect line are considered as 48 nm and 112.32 nm, respectively, with an aspect ratio of 2.34. The spacing between the interconnect lines and the height from the ground plane are assumed to be equal to the width and thickness, respectively. The interlevel metal insulator dielectric constant, load capacitance and length of the line are 2.78, 2 fF and 0.5 mm, respectively. The line capacitive and inductive parasitics are extracted from the electrostatic and magnetostatic field solvers, respectively [195, 196]. The symmetric CMOS drivers are used to drive the coupled interconnect lines [197]. The input to the aggressor line is a falling ramp signal from 0.9 V to 0 V with a transition time of 50 ps.

The interconnect line supports two different modes of propagation *i.e.*, even and odd modes in coupled lines. For given line parasitics, the corresponding even and odd mode velocities are evaluated as $v_1=1.49\times10^8$ m/s and $v_2=0.49\times10^8$ m/s, respectively. To maintain high accuracy, the line discretization value (êz) is considered as 0.5×10^{-5} m. Based on the CFL stability condition, the maximum time step size ($\Delta t_{\max}$) while ensuring stable operation is 0.33×10^{-13} s.

6.3.1 Transient Analysis

The comprehensive crosstalk noise is analyzed at the far-end of the line 2 using proposed US-FDTD and conventional FDTD. The transient responses of functional, dynamic in-phase and dynamic out-phase crosstalk switching are shown in Figures 6.6, 6.7 and 6.8, respectively. The input switching of interconnect lines is shown in the inset. For functional crosstalk, line 1 (aggressor) makes a transition from ground to V_{DD} while line 2 (victim) is at ground level. During dynamic in-phase crosstalk, both line 1 and line 2 switch from ground to V_{DD}. Finally, for dynamic out-phase crosstalk, line 1 and line 2 make the transition from ground to V_{DD} and from V_{DD} to ground, respectively. From Figures 6.6-6.8, it is observed that in all the three cases the proposed US-FDTD model accurately estimates the timing response with respect to the conventional FDTD model.

6.3.2 Crosstalk Induced Noise Peak, Width and Delay Analysis

When the generated noise has a peak voltage above the threshold voltage and attains a width above the threshold pulse width of the receiving gate, it leads to the generation of a glitch that may result in logical failure of the circuit [162]. Therefore, noise peak voltage and pulse width are the two important parameters for crosstalk noise analysis. Consequently, these parameters are estimated using the proposed US-FDTD model and conventional FDTD model. Table 6.3 shows the functional crosstalk noise peak voltage and pulse width at different load capacitances. The average percentage error is observed to be less than 1% for noise peak voltage and noise width. It is also observed that as the load capacitance increases, the noise peak voltage decreases, whereas the noise width increases. This is because of the increase in time constant with the increase in load capacitance.

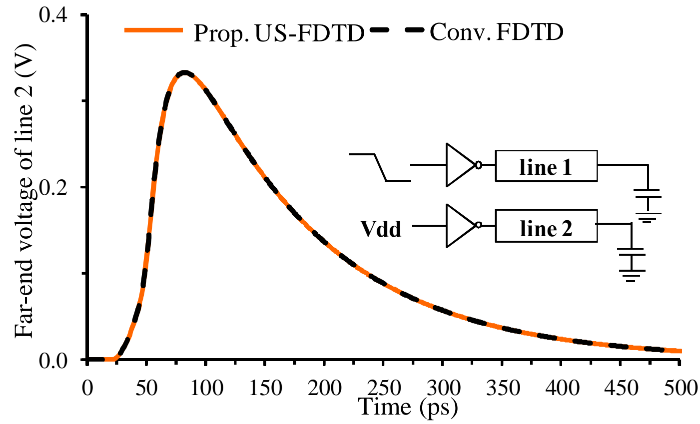


Figure 6.6. Transient response comparison during the functional crosstalk.

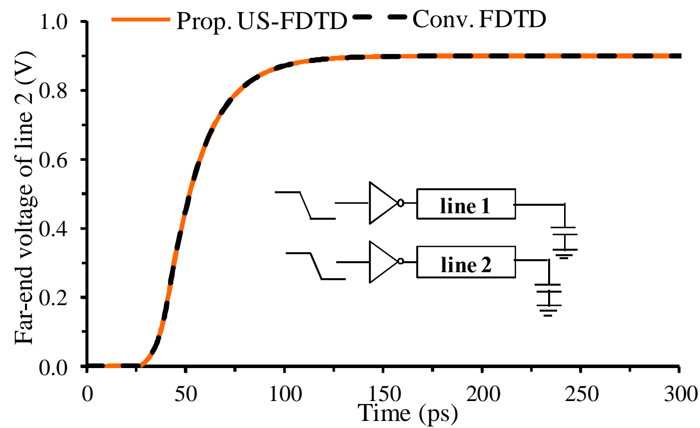


Figure 6.7. Transient response comparison during the dynamic in-phase crosstalk.

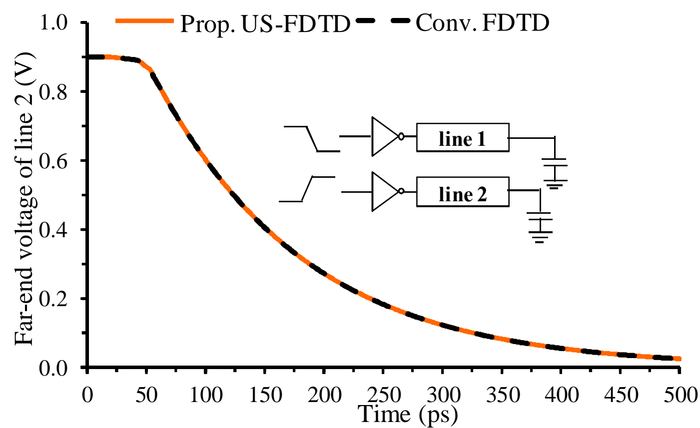


Figure 6.8. Transient response comparison during the dynamic out-phase crosstalk.

Table 6.3 Noise peak voltage and noise width comparison between proposed US-FDTD and conventional FDTD simulations

Load capacitance (fF)	Peak voltage			Noise width		
	Proposed US-FDTD (V)	Conv. FDTD (V)	Error (%)	Proposed US-FDTD (ps)	Conv. FDTD (ps)	Error (%)
5	0.287	0.289	0.69	150.151	148.280	0.58
10	0.249	0.249	0	176.614	175.655	0.54
15	0.222	0.223	0.45	202.112	201.003	0.55
20	0.197	0.198	0.50	231.621	229.707	0.62

To further verify the accuracy of the proposed model, the dynamic in-phase and out-phase crosstalk induced delay are analyzed at different interconnect lengths. From Figure 6.9, it can be observed that the proposed model accurately estimates the crosstalk induced propagation delay for all interconnect lengths, with an average error of less than 1%. It is also observed that the out-phase delay is higher than the in-phase delay. This is due to the fact that the Miller capacitance strongly influences the signal propagation during the out-phase switching, whereas it is ineffective during the in-phase switching.

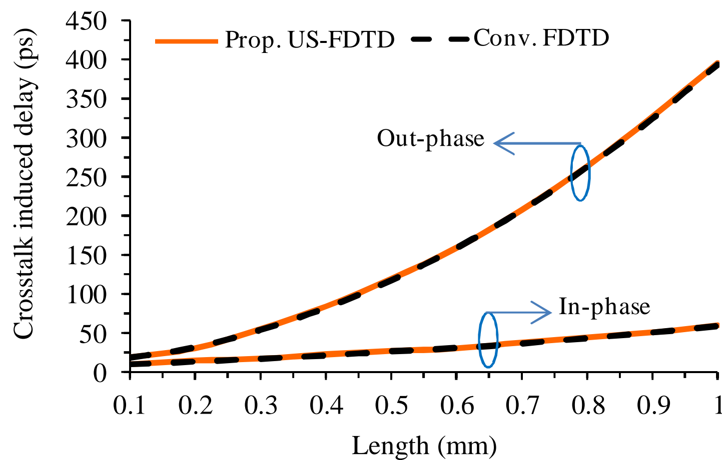


Figure 6.9. Comparison of crosstalk induced propagation delay between proposed US-FDTD model and conventional FDTD model.

6.3.3 Unconditional Stability of the Proposed Model

The stability of the proposed model is verified through a numerical example demonstrating the dynamic in-phase transient response. The transient response is analyzed at different time steps using both conventional and proposed US-FDTD.

The stability of the proposed model is analyzed in the following two cases:

1) Within the CFL condition ($\Delta t = \Delta t_{max}$), from Figure 6.10 (a) it can be observed that both conventional FDTD and proposed US-FDTD models provide stable outputs;

2) Beyond the CFL condition ($\Delta t > \Delta t_{max}$), from Figure 6.10 (b) it can be observed that the conventional FDTD model is unstable at $\Delta t = 2\Delta t_{max}$, whereas the proposed model is stable and sufficiently accurate, even when $\Delta t = 100t_{max}$ (Figure 6.10 (a)). Although, at $\Delta t = 300\Delta t_{max}$ the proposed model output is stable but the accuracy reduces due to the lower resolution in temporal space. The stability of the proposed model is not limited by the CFL condition and is therefore unconditionally stable.

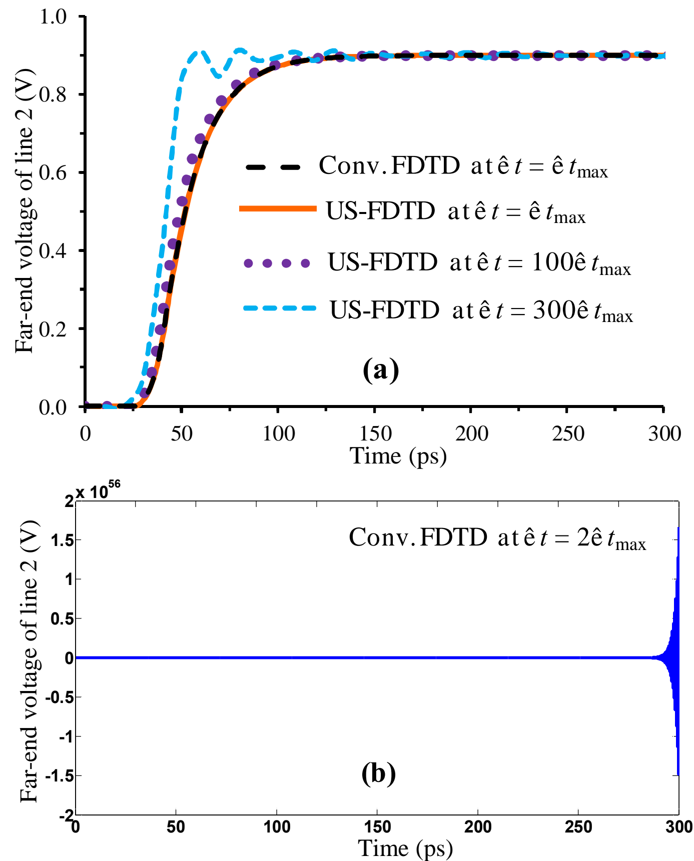


Figure 6.10. Dynamic in-phase crosstalk analysis at different time steps (a) stable output of conventional FDTD and proposed US-FDTD and (b) unstable output of conventional FDTD due to the violation of CFL condition.

6.3.4 Efficiency of the Proposed Model

Using a PC with Intel Core i7 CPU (3.4 GHz, 8 GB RAM), the runtime of the proposed model is compared with the conventional FDTD. The computational effort for the transient analysis of dynamic in-phase crosstalk at different time steps is shown in Table 6.4. For Δt Ö Δt_{max}, the proposed US-FDTD model requires 89% of the time utilized by the conventional FDTD model. It is worth noting that because the proposed model is unconditionally stable, it allows to consider larger time step, well beyond Δt_{max}. This further reduces the number of iterative steps required for analysis and consequently, reduces the computational run-time. As observed in Table 6.4, at $\Delta t = 100\Delta t_{max}$, where the conventional model results in unstable output, the proposed model requires only 0.9% of the time required by conventional model at $\Delta t = \Delta t_{max}$. Therefore, depending on the time step size the proposed model can be up to 100 times faster than the conventional FDTD.

Table 6.4 Comparison of computational efforts

Time Step Size, ê *t*	No. of Iterations		CPU Time (s)	
	Conventional FDTD Model	Proposed US-FDTD Model	Conventional FDTD Model	Proposed US-FDTD Model
$0.5\Delta t_{max}$	18182	18182	4.124	3.651
$1\Delta t_{max}$	9091	9091	2.056	1.824
$2\Delta t_{max}$	×	4545	×	0.914
$10\Delta t_{max}$	×	909	×	0.191
$50\Delta t_{max}$	×	182	×	0.037
$100\Delta t_{max}$	×	91	×	0.019

÷×ø represents the invalid instances since the conventional FDTD model becomes unstable for $\Delta t > \Delta t_{max}$.

6.3.5 Comparison with 3D Simulations

The validity of the proposed model is further verified by the 3D simulations. Sentaurus TCAD simulator is used for the 3D simulations [198]. The interconnect width and spacing between the interconnect lines are equally considered as 48 nm, the thickness and height from the ground plane are equally considered as 112.32 nm. The interlevel metal insulator dielectric constant, load capacitance and length of the line

are 2.78, 0.2 fF and 5   m, respectively. The structure of the coupled interconnect line is shown in Figure 6.11. The transient response at the far-end voltage of line 2 is observed during the functional crosstalk switching and shown in Figure 6.12. It can be observed that the accuracy of the results via the proposed model is in good agreement with the 3D simulations. The average error between the proposed model and 3D simulation is less than 3%. The CPU run time and memory required by the proposed model are 0.02 s and 602 MB, respectively, whereas the 3D simulations require 964 s and 3066 MB, respectively.

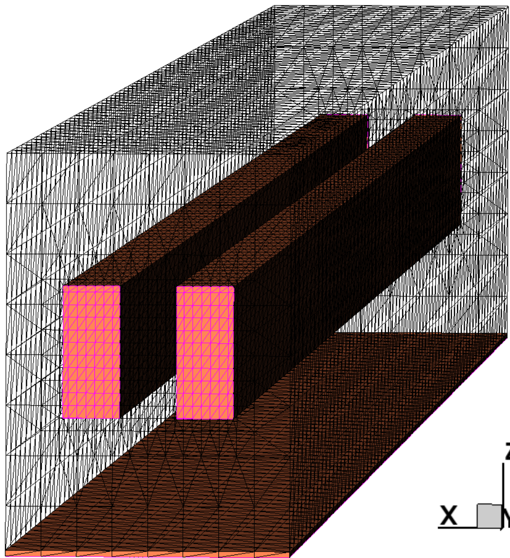


Figure 6.11. Structure of two coupled interconnects.

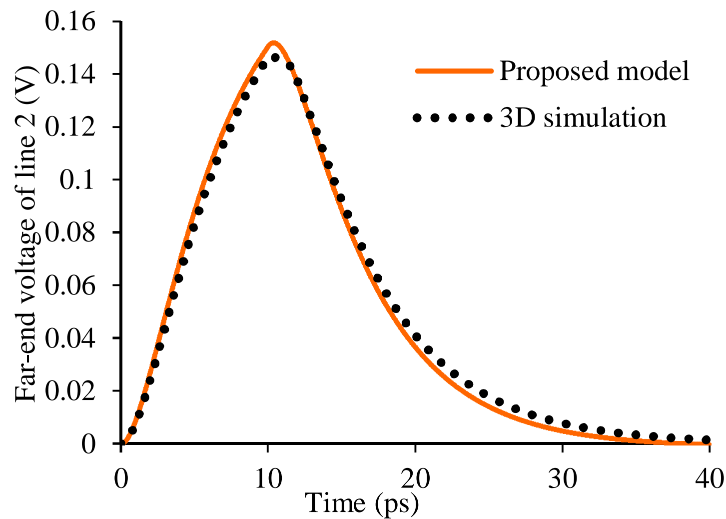


Figure 6.12. Transient response comparison between the proposed US-FDTD model and 3D simulations at the far-end terminal of line 2 during the functional crosstalk switching.

6.4 Performance Comparison of Cu, MWCNT and MLGNR Interconnects

In this sub-section, the propagation delay under the influence of crosstalk is analyzed among Cu, MWCNT and MLGNR interconnects. The simulations have been carried out using the US-FDTD method. The coupled interconnect line structures considered for the performance comparison of Cu/MWCNT/MLGNR is shown in Figure 6.13. A CMOS driver with supply voltage V_{DD} = 0.9 V is used to drive the interconnect line. The relative permittivity of the inter layer dielectric medium is considered as 2.25. The width and spacing between coupled interconnects is equal to 48 nm and the distance from the ground plane is 86.4 nm.

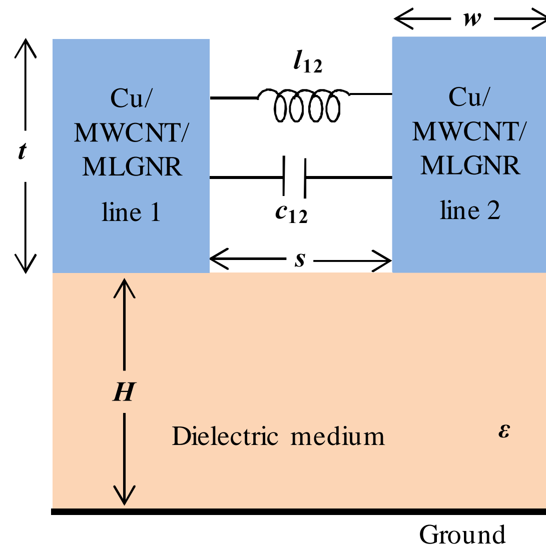


Figure 6.13. Structure of two coupled interconnects.

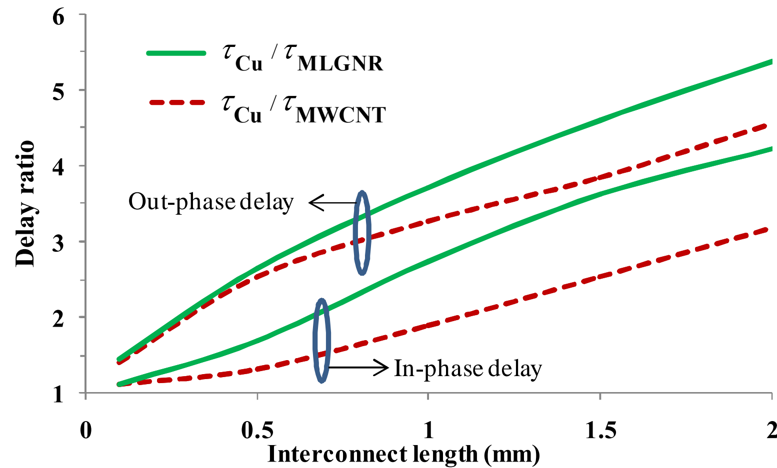


Figure 6.14. Performance delay comparison among Cu, MWCNT and MLGNR interconnects.

The crosstalk induced delay ratios of Cu to MLGNR (τ_{Cu}/τ_{MLGNR}) and MWCNT (τ_{Cu}/τ_{MWCNT}) are shown in Figure 6.14. The AsF_5 doped MLGNR interconnect is used with intercalation doping density of E_F = 0.4 eV and back scattering probability of 0.2. The comparison plot shows that the crosstalk induced delay of MWCNT and MLGNR substantially reduces in comparison to the conventional Cu interconnect. This reduction is more prominent for out-phase switching due to the considerable reduction in coupling capacitance of MWCNT/MLGNR than Cu interconnects. Additionally, the crosstalk induced delay of MLGNR is smaller in comparison to MWCNT interconnects. The primary reason behind this reduced delay is the availability of more number of conduction channels in MLGNR than MWCNT. Therefore, the superior electrical properties and the fabrication compatibility with conventional lithography techniques make the MLGNR intrinsically more suitable material for on-chip interconnect realization. However, the intercalation doping of MLGNR with low back scattering probability is the primary challenge in designing a high performance MLGNR interconnect.

6.5 Summary

This chapter proposed a novel model based on US-FDTD technique, to analyze the crosstalk effects of coupled VLSI interconnects. It is analytically and numerically demonstrated that the proposed model is not limited by the CFL condition and is unconditionally stable. Using the proposed model, a comprehensive crosstalk analysis is performed and the results are in good agreement with the conventional FDTD model. The average percentage error is observed to be less than 1% for the estimation of crosstalk induced performance parameters. Moreover, it is observed that the proposed model is highly time efficient than the conventional FDTD model. Depending on the time step size, the proposed model can be up to 100× faster than the conventional FDTD. Moreover, the performance comparison of Cu, MWCNT and MLGNR interconnects is also presented. It is observed that the MLGNR is the better suitable on-chip interconnect material than the Cu and MWCNT.

Chapter 7

Conclusions and Future Scope

This thesis focused on the modeling of CMOS gate driven on-chip interconnects, where the time/frequency domain conversion problem is addressed by analyzing the interconnect lines in time domain using the FDTD technique. Based on the FDTD technique, the performance of Cu and graphene based on-chip interconnects has been investigated. Moreover, to improve the efficiency of the conventional FDTD technique, a novel unconditionally stable FDTD technique is introduced. This chapter summarizes the major contributions and the important outcomes of the proposed work. In addition, it also presents some directions for future research work.

7.1 Conclusions

The first phase of the work demonstrated the FDTD modeling for the crosstalk induced performance analysis of Cu interconnects. In a more realistic manner, the nonlinear CMOS drivers have been considered to drive the interconnect lines. The CMOS drivers are represented by the n-th power law model and the interconnect lines are represented as transmission lines that are coupled capacitively and inductively. The boundary conditions are derived from the interfacing equations without using any approximations. The stability of the proposed model is strictly followed by the CFL stability time step condition. The propagation delay, peak crosstalk voltage, and peak voltage timing on the victim line of coupled-multiple lines have been observed and compared to HSPICE simulation results for the global interconnect length. The numerical results demonstrate that the proposed model accurately estimates the performance parameters of the driver interconnect load system. Encouragingly, the FDTD model is highly time efficient than the HSPICE. The model is useful for the evaluation of signal integrity, issues of electromagnetic interference (EMI) and electromagnetic compatibility (EMC) of Cu interconnects.

In the second phase, the MWCNT interconnects have been considered for the crosstalk induced performance analysis. Based on the equivalent single conductor

(ESC) model, an accurate FDTD model of MWCNT is presented. The proposed model considers the quantum effects of nanowire and non-linear effects of CMOS driver. To reduce the computational effort required for analyzing the CMOS driver, a simplified but accurate model is employed, named as, modified alpha power law model. The developed model can be essentially used to analyze the functional and dynamic crosstalk effects of coupled MWCNT interconnect lines. Crosstalk induced propagation delay and peak voltage are measured using the proposed model and validated by comparing it to the HSPICE simulations. Over a random number of test cases, it is observed that the average error in estimating the noise peak voltage on a victim line is less than 2%. Moreover, it is observed that using the proposed model, the CPU runtime reduces by an average of 91% in comparison to HSPICE simulations. The presented model is extremely useful for accurate estimation of crosstalk induced performance parameters of MWCNT interconnects. The analysis suggests that, with continuous advancements in FDTD technique the proposed model would play a significant role in performance analysis of MWCNT on-chip interconnects and would be potentially incorporated in TCAD simulators.

The third phase of the work is directed towards the modeling and performance analysis of multi-layered GNR (MLGNR). In a more realistic manner, the proposed model considered the effect of width-dependent MFP while taking into account the edge roughness. Using the width dependent MFP, the effective MFP of an MLGNR is evaluated and it has been observed that the edge roughness reduces the MFP by more than one order of magnitude, particularly for narrow widths. Based on the FDTD technique, the crosstalk induced propagation delay of an MLGNR is analyzed. It is observed that the results exhibit a good agreement with HSPICE simulations. Moreover, it is observed that the conventional models are not useful for accurate estimation of crosstalk induced performance parameters. It has been noticed that the width dependent MFP should be incorporated in a valid crosstalk noise modeling. In addition, the performance of MLGNR is compared with the Cu interconnects. It is observed that the overall delay and power dissipation of doped MLGNR are reduced by 86% and 43%, respectively, in comparison to the Cu interconnects.

The last phase of the work focused on the efficiency of the FDTD model. It is noticed that the efficiency of the conventional FDTD is limited by the CFL condition.

The improvements in FDTD technique can be easily addressed if the CFL stability condition is removed. Therefore, to improve the efficiency of the FDTD model an unconditionally stable FDTD (US-FDTD) model is proposed for the performance analysis of on-chip interconnects. The accuracy of the US-FDTD model is validated against the conventional FDTD model. It is observed that the proposed model is as accurate as the conventional FDTD. It is also observed that the stability of the proposed model is not constrained by the CFL stability condition. Depending on the time step size, the US-FDTD model can be up to 100× faster than the conventional FDTD. Moreover, the performance of MWCNT and MLGNR interconnects is compared with the Cu interconnects. Based on the comparative study, it is observed that the MLGNR and MWCNT interconnects outperform the Cu interconnect.

7.2 Future Work

In this thesis, an exhaustive study on the modeling of Cu, MWCNT and MLGNR interconnects has been carried out, but still there is enough scope for further research work. Some of these works are briefly mentioned below:

1. The performance analysis of non uniform interconnects can be attempted as an extension of this research work.
2. At high operating frequencies, the frequency dependent parameters can be incorporated in the proposed FDTD models, for better accuracy.
3. In a more realistic manner, the developed models can be extended for 3 dimensional structures.
4. Temperature and stress effects can be incorporated in the modeling of interconnects.
5. The full wave structural simulations for nano-structured materials can be developed to validate the interconnect models.
6. The proposed FDTD technique can be applied for the performance analysis of through silicon vias (TSVs).

References

[1] Rabaey, J. M.; Chandrakasan, A.; Nikolic*,* B. õDigital integrated circuits: A design perspective,ö 2nd Edition, Prentice-Hall, **2003**.

[2] Goel, A. K. õHigh-speed VLSI Interconnections,ö 2nd Edition, Wiley-IEEE Press, **2007.**

[3] Rabindra, K.; Srivastava, P.; Sharma, G. K. õNetwork-on-chip: On-chip communication solution,ö *International Review on Computers and Software* **2010**, 5(1), 22-33.

[4] Agarwal, K.; Sylvester, D.; Blaauw, D. õModeling and analysis of crosstalk noise in coupled RLC interconnects,ö *IEEE Trans. Comput. Aided Des. Integrated Circuits Syst*. **2006**, 25(5), 892ó901.

[5] Sahoo, M.; Ghosal, P.; Rahaman, H. õModeling and analysis of crosstalk induced effects in multiwalled carbon nanotube bundle interconnects: An ABCD parameter-based approach,ö *IEEE Trans. Nanotechnology* **2015**, 14(2), 259-274.

[6] Edelstein, D.; Heidenreich, J.; Goldblatt, R.; Cote, W.; Uzoh, C.; Lustig, N.; Roper, P.; McDevitt, T.; Motsiff, W.; Simon, A.; Dukovic, J.; Wachnik, R.; Rathore, H.; Schulz, R.; Su, L.; Luce, S.; Slattery, J. õFull copper wiring in a sub-0.25µm CMOS ULSI technology,ö Proc. *Inter. Electron Dev. Meeting Tech. Digest*, USA, **1997**, 773-776.

[7] Zhang, J.; Friedman, E. G. õCrosstalk modeling for coupled *RLC* interconnects with application to shield insertion,ö *IEEE Trans. VLSI Syst.* **2006**, 14(6), 641-646.

[8] Koo, K. H. õComparison study of future on-chip interconnects for high performance VLSI applications,ö Ph.D. thesis, Stanford University, United States, **2000**.

[9] Srivastava, A.; Xu, Y.; Sharma, A. K. õCarbon nanotubes for next generation very large scale integration interconnects,ö *J. Nanophotonics.* **2010**, 4(1), 1 ó 26.

[10] Javey, A.; Kong, J. õCarbon nanotube electronics,ö Springer, **2009**.

[11] Xu, Y. õCarbon nanotube interconnect modeling for very large scale integrated circuits,ö PhD Dissertation, Louisiana State University, USA, **2011**.

[12] Das, D.; Rahaman, H. õAnalysis of crosstalk in single- and multiwall carbon nanotube interconnects and its impact on gate oxide reliability,ö *IEEE Trans. Nanotechnol.* **2011**, 10(6), 1362-1370.

[13] Tamburrano, A.; D'Aloia, A. G.; Sarto, M. S. õBundles of multiwall carbon nanotube interconnects: RF crosstalk analysis by equivalent circuits,ö Proc. *IEEE International Symposium on Electromagnetic Compatibility (EMC),* Pittsburgh, **2012**, 434-439.

[14] Plombon, J. J. õHigh-frequency electrical properties of individual and bundled carbon nanotubes,ö *Applied Physics Lett.* **2007**, 90(6), 063106-1ó063106-3.

[15] Xu, Y.; Srivastava, A. õA model for carbon nanotube interconnects,ö *Int. J. Circuit Theory Appl.* **2009**, 38(6), 559 ó 575.

[16] Berber, S.; Kwon, Y. K.; Tomanek, D. õUnusually high thermal conductivity of carbon nanotubes,ö *Phys. Rev. Lett.* **2000**, 84(20), 4613ó4616.

[17] Areshkin, D. A.; Gunlycke, D.; White, C. T. õBallistic transport in graphene nanostrips in the presence of disorder: Importance of edge effects,ö *Nano Lett.* **2007**, 7(1), 204ó210.

[18] Avorious, P.; Chen, Z.; Perebeions, V. õCarbon-based electronics,ö *Nat. Nanotechnol.* **2007**, 2(10), 605-613.

[19] Close, G. F.; Wong, H. S. P. õAssembly and electrical characterization of multiwall carbon nanotube interconnects,ö *IEEE Trans. Nanotechnol.* **2008**, 7(5), 596 ó 600.

[20] Collins, P. G.; Arnold, M. S.; Avouris, Ph. õEngineering carbon nanotubes and nanotube circuits using electrical breakdown,ö *Science* **2001**, 292(5517), 706ó709.

[21] Liang, F.; Wang, G.; Lin, H. õModeling of crosstalk effects in multiwall carbon nanotube interconnects,ö *IEEE Tran. on Electromagnetic Compatibility* **2012**, 54(1), 133ó139.

[22] Narasimhamurthy, K. C.; Paily, R. õImpact of bias voltage on inductance of carbon nanotube interconnects,ö Proc. *22nd International Conference on VLSI Design*, New Delhi, **2009**, 505-510**.**

[23] Majumder, M. K.; Pandya, N. D.; Kaushik, B. K.; Manhas, S. K. õAnalysis of MWCNT and bundled SWCNT Interconnects: Impact on crosstalk and area,ö *IEEE Electron Device Lett.* **2012**, 33(8), 1180-1182.

[24] Majumder, M. K.; Kaushik, B. K.; Manhas, S. K. õAnalysis of delay and dynamic crosstalk in bundled carbon nanotube interconnects,ö *IEEE Trans. Electromagn. Compat.* **2014**, 56(6), 1666-1673.

[25] Morris, J. E. õThe proof is in the nanopacking,ö *IEEE Nanotechnol. Mag.* **2008**, 2(4), 25-27.

[26] Li, H.; Yin, W. Y.; Banerjee, K.; Mao, J. F. õCircuit modeling and performance analysis of multi-walled carbon nanotube interconnects,ö *IEEE Trans. Electron Devices* **2008**, 55(6), 1328-1337.

[27] Murali, K. H.; Brenner, K.; Yang, Y.; Beck, T.; Meindl, J. D. õResistivity of graphene nanoribbon interconnects,ö *IEEE Electron Device Lett.* **2009,** 30(6), 611-613.

[28] Tanachutiwat, S.; Liu, S.; Geer, R.; Wang, W. õMonolithic graphene nanoribbon electronics for interconnect performance improvement,ö Proc. *IEEE Int. Symp. on Circuits and Systems,* Taipei. **2009**, 589-592.

[29] Naeemi, A.; Meindl, J. D. õElectron transport modeling for junctions of zigzag and armchair graphene nanoribbons (GNRs),ö *IEEE Electron Device Lett.* **2008**, 29(5), 497ó499.

[30] Avouris, P. õGraphene: Electronic and photonic properties and devices,ö *Nano Lett.* **2010**, 10(11), 4285ó4294.

[31] Berger, C.; Song, Z.; Li, X.; Wu, X.; Brown, N.; Naud, C.; Mayou, D.; Li, T.; Hass, J.; Marchenkov, A. N.; Conrad, E. H.; First, P. N.; Heer, W. A. õElectronic conŁnement and coherence in patterned epitaxial graphene,ö *Science* **2006**, 312(5777), 1191ó1196.

[32] Bothra, S.; Rogers, B.; Kellam, M.; Osburn, C. M. õAnalysis of the effects of scaling on interconnect delay in ULSI circuits,ö *IEEE Trans. Electron Devices*, **1993**, 40(3), 591ó597.

[33] Bakoglu, H. B. õCircuits, interconnections and packaging for VLSI,ö Addison-Wesley Publishing Company, **1990**.

[34] Ismail Y. I.; Friedman, E. G. õEffects of inductance on the propagation delay and repeater insertion in VLSI circuits,ö *IEEE Trans. Very Large Scale Integration (VLSI) Systems* **2000**, 8(2), 195ó206.

[35] Kaushik, B. K.; Sarkar, S. õCrosstalk analysis for a CMOS-gate-driven coupled interconnects,ö *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst*. **2008**, 27(6), 1150-1154.

[36] Kaushik, B. K.; Sarkar, S.; Agarwal, R. P.; Joshi, R. C. õAn analytical approach to dynamic crosstalk in coupled interconnects,ö *Microelectron. J*. **2010**, 41(2), 85-92.

[37] Cui, J.; Zhao, W.; Yin, W.; Hu, J. õSignal transmission analysis of multilayer graphene nano-ribbon (MLGNR) interconnects,ö *IEEE Trans. Electromagnetic Compat*. **2012**, 54(1), 126ó132.

[38] Paul, C. R. õAnalysis of multiconductor transmission lines,ö IEEE Press, **2008**.

[39] Paul, C. R. õIncorporation of terminal constraints in the FDTD analysis of transmission lines,ö *IEEE Trans. Electromagnetic Compat*. **1994**, 36(2), 85ó91.

[40] Paul, C. R. õDecoupling the multi conductor transmission line equations,ö *IEEE Trans.on Microwave Theory and Techniques* **1996**, 44(8), 1429ó1440.

[41] Orlandi, A.; Paul, C. R. õFDTD analysis of lossy, multiconductor transmission lines terminated in arbitrary loads,ö *IEEE Trans. on Electromagnetic Compat.* **1996**, 38(3), 388ó399.

[42] Li, X. C.; Ma, J. F.; Swaminathan, M. õTransient analysis of CMOS gate driven *RLGC* interconnects based on FDTD,ö *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **2011**, 30(4), 574-583.

[43] Livshits, P.; Sofer, S., õAggravated electromigration of copper interconnection lines in ULSI devices due to crosstalk noise,ö *IEEE Trans. Device and Materials Reliability*, **2012**, 12(2), 341-346.

[44] Moll, F.; Roca, M.; Rubio, A. õInductance in VLSI interconnection modeling,ö *IEEE Proc. Circuits Devices Syst*. **1998**, 145(3), 175-179.

[45] Sakurai, T.; Newton, R. õAlpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas,ö *IEEE Jr. Solid-State Circuits* **1990**, 25(2), 584ó594.

[46] Bowman, K. A.; Austin, B. L.; Eble, J. C.; Xingha, T.; Meindl, J. D. õA physical alpha-power law MOSFET model,ö *IEEE J. Solid State Circuits* **1999**, 34(10), 1410-1414.

[47] Dutta, S.; Shetti, S. S. M.; Lusky, S. L. õA comprehensive delay model for CMOS inverters,ö *IEEE J. Solid-State Circuits* **1995**, 30(8), 864ó871.

[48] Bisdounis, L.; Nikolaidis, S.; Koufopavlou, O. õAnalytical transient response and propagation delay evaluation of the CMOS inverter for short-channel devices,ö *IEEE J. Solid-State Circuits* **1998**, 33(2), 302ó306.

[49] Qian, J.; Pullela, S.; Pillage, L. õModeling the effective capacitance for the RC interconnect of CMOS gates,ö *IEEE Trans. Comput.-Aided Des*. **1994**, 13(12), 1526ó1535.

[50] Hafed, M.; Oulmane, M.; Rumin, N. C. õDelay and current estimation in a CMOS inverter with an RC load,ö *IEEE Trans. Comput.-Aided Des.* **2001**, 20(1), 80ó89.

[51] Chatzigeorgiou, A.; Nikolaidis, S.; Tsoukalas, I. õModeling CMOS gates driving RC interconnect loads,ö *IEEE Trans. Circuits Syst. II: Analog Digital Signal Process* **2001**, 48(4), 413ó418.

[52] Adler, V.; Friedman, E. G.; õRepeater design to reduce delay and power in resistive interconnect,ö *IEEE Tran. on Circuits and Systems II: Analog and Digital Signal Processing*, **1998**, 45(5), 607ó616.

[53] Bakoglu, H. B.; Meindl, J. D. õOptimal interconnection circuits for VLSI,ö *IEEE Trans. on Electron Devices* **1985**, 32(5), 903ó909.

[54] Rubinstein, J.; Penfield, P.; Horowitz, M. A. õSignal delay in RC tree networks,ö *IEEE Trans. Comput.-Aided Des.* **1983**, 2(3), 202ó211.

[55] Kahng, A.; Muddu, S. õAn analytical delay model for RLC interconnects,ö *IEEE Trans. Comput.-Aided Des*. **1997**, 16(2), 1507ó1514.

[56] Ismail, Y. I.; Friedman, E. G.; Neves, J. L. õEquivalent elmore delay for RLC trees,ö *IEEE Trans. Comput.-Aided Des*. **2000**, 19(1), 83ó97.

[57] Bai, X.; Chandra, R.; Dey, S.; Srinivas, P. V. õInterconnect couplingaware driver modeling in static noise analysis for nanometer circuits,ö *IEEE Trans. Comput.-Aided Des.* **2004**, 23(8), 1256ó1263.

[58] Davis J. A.; Meindl, J. D. õCompact distributed RLC models, part I: Single line transient, time delay, and overshoot expressions,ö *IEEE Trans. Electron Devices* **2000**, 47(11), 2068ó2077.

[59] Davis, J. A.; Meindl, J. D. õCompact distributed RLC models, part II: Coupled line transient expressions and peak crosstalk in multilevel networks,ö *IEEE Trans. Electron Devices* **2000**, 47(11), 2078ó 2087.

[60] Liu, T.; Kuo, J.; Zhang, S. õA closed-form analytical transient response model for on-chip distortion less interconnect,ö *IEEE Trans. Electron Devices* **2012**, 59(12), 3186ó3192.

[61] Kaushik, B. K.; Sarkar, S. õCrosstalk analysis for a CMOS gate driven inductively and capacitively coupled interconnects,ö *Microelectronics Journal* **2008**, 39(12), 1834-1842.

[62] Kroto, H. W.; Heath, J. R.; OøBrien, S. C.; Curl, R. F.; Smalley, R. E. õC60: Buckminsterfullerene,ö *Nature*, **1985**, 318,162-63.

[63] Xu, T.; Wang, Z.; Miao, J.; Chen, X.; Tan, C. M. õAligned carbon nanotubes for through-wafer interconnects,ö *Appl. Phys. Letts.* **2007**, 91(4), 042108-1 - 042108-3.

[64] Scarselli, M.; Castrucci, P.; Crescenzi, M. õElectronic and optoelectronic nano-devices based on carbon nanotubes,ö *Journal of Physics: Condensed Matter* **2012**, 24(31), 313202-1ó313202-36.

[65] Monthioux, M.; Serp, P.; Flahaut, E. ÷Introduction to carbon nanotubes. In: Handbook of nano-technology,*"* ed. B. Bhushan, New York: Springer, **2010**.

[66] Wang, N.; Tang, Z. K.; Li, G. D.; Chen., J. S. õSingle-walled 4 Å carbon nanotube arrays,ö *Nature* **2000**, 408, 50ó51.

[67] Hamada, N.; Sawada, S. I.; Oshiyama., A. õNew one-dimensional conductors, graphite microtubules,ö *Phys. Rev. Lett*. **1992**, 68, 1579ó81.

[68] Li, H. J.; Lu, W. G.; Li, J. J.; Bai, X. D.; Gu., C. Z. õMultichannel ballistic transport in multiwall carbon nanotubes,ö *Phys. Rev. Lett.* **2005**, 95(8), 86601.

[69] Nihei, M.; Kondo, D.; Kawabata, A.÷Low-resistance multi-walled carbon nanotube vias with parallel channel conduction of inner shells,ö Proc. *IEEE Int. Interconnect Technology Conference* **2005,** 234ó36.

[70] Forró, L.; Schönenberger, C. õPhysical properties of multi-wall nanotubes in topics in applied physics, carbon nanotubes: synthesis, structure, properties and applications,ö ed. M.S. Dresselhaus, G. Dresselhaus, P. Avouris. Berlin, Germany: Springer-Verlag, **2000.**

[71] Wei, B. Q.; Vajtai, R.; Ajayan, P. M. õReliability and current carrying capacity of carbon nanotubes,ö *Appl. Phys. Lett.* **2001**, 79(8), 1172-1174.

[72] Shah, T. K.; Pietras, B. W.; Adcock, D. J.; Malecki, H. C.; Alberding. M. R. õComposites comprising carbon nanotubes on fiber,ö US Patent, US8585934 B2, **2013**.

[73] Dresselhaus, M.; Dresselhaus, G.; Avouris, Ph. õCarbon nanotubes: Synthesis, structure, properties and applications,ö Topics in applied research 80, Springer, **2001**.

[74] Hsieh, J. Y. L.; Huang, J. M.; Hwang, C. C. õTheoretical variations in the Youngøs modulus of single-walled carbon nanotubes with tube radius and temperature: A molecular dynamics study,ö *Nanotechnology* **2006,** 17, 3920ó24.

[75] Forro, L.; Salvetat, J. P.; Bonard, J. ÷Electronic and mechanical properties of carbon nanotubes. In science and application of nanotubes,ö ed. Tománek, and Enbody, 297ó320 New York: Plenum Publishers, **2002**.

[76] Wei, C.; Srivastava, D.; Cho., K. õThermal expansion and diffusion coefficients of carbon nanotube-polymer composites,ö *Nano Lett.* **2002,** 2(6), 647ó50.

[77] Wang, Z.; Zhao., G. L. õMicrowave absorption properties of carbon nanotubes-epoxy composites in a frequency range of 2-20 GHz,ö *Open J. Compos Mater* **2013**, 3(2), 17ó 23.

[78] Ifeanyi, H. N.; John, I. E.; Zhou W., Diola, B., Guang-Lin Z. õMicrowave absorption properties of multi-walled carbon nanotube (outer diameter 20ó30 nm)óepoxy composites from 1 to 26.5 GHz,ö Diamond and Related Materials, **2015**, 52, pp. 66-71.

[79] Naeemi, A.; Meindl, J. D. õCompact physical models for multiwall carbon-nanotube interconnects,ö *IEEE Electron Device Lett.* **2006**, 27(5), 338-340.

[80] Naeemi, A.; Sarvari, R.; Meindl, J. D. õPerformance comparison between carbon nanotube and copper interconnects for gigascale integration (GSI),ö *IEEE Electron Device Lett.* **2005**, 26(2), 84-86.

[81] Burke, P. J. õLüttinger liquid theory as a model of the gigahertz electrical properties of carbon nanotubes,ö *IEEE Trans. Nanotechnol.* **2002**, 1(3), 129-144.

[82] Avouris, P.; Appenzeller, J.; Martel, R.; Wind, S. J. õCarbon nanotube electronics,ö *Proc. of IEEE* **2003**, 91(11), 1772-1784.

[83] Li, J.; Ye, Q.; Cassell, A.; Ng, H. T.; Stevens, R.; Han, J.; Meyyappan, M. õBottom-up approach for carbon nanotube interconnects,ö *Appl. Phys. Lett.* **2003**, 82(15), 2491ó2493.

[84] Ngo, Q.; Petranovic, D.; Krishnan, S.; Cassell, A. M.; Ye, Q.; Li, J.; Meyyappan, M.; Yang, C. Y. õElectron transport through metalómultiwall carbon nanotube interfaces,ö *IEEE Trans. Nanotechnol.* **2004**, 3(2), 311-317.

[85] Miano, G.; Villone, F. õAn integral formulation for the electrodynamics of metallic carbon nanotubes based on a fluid model,ö *IEEE Trans. Antennas Propag.* **2005**, 54(10), 2713-2724.

[86] Sarto, M. S.; Tamburrano, A. õSingle conductor transmission-line model of multiwall carbon nanotubes,ö *IEEE Trans. Nanotechnol.* **2010**, 9(1), 82-92.

[87] Tang, M.; Lu J.; Mao J. õStudy on equivalent single conductor model of multi-walled carbon nanotube interconnects,ö Proc. *IEEE Asia Pacific Microwave Conference*, Taiwan, **2012**, 1247ó1249.

[88] DøAmore, M.; Sarto, M. S.; Tamburrano, A. õFast transient analysis of next-generation interconnects based on carbon nanotubes,ö *IEEE Trans. Electromagn. Compat.* **2010**, 52(2), 496 ó 503.

[89] Lamberti, P.; Tucci, V. õImpact of variability of the process parameters on CNT-based nanointerconnects performances: A comparison between SWCNTs bundles and MWCNT,ö *IEEE Trans. Nanotechnol.* **2012**, 11(5), 924-933.

[90] Liang, F.; Lin, H.; Wang, G. õPrediction of crosstalk effects in future multiwall carbon nanotube (MWCNT) interconnects,ö Proc. *IEEE Symposium on Antennas Propagation and EM Theory (ISAPE),* Guangzhou*,* **2010**, 1031-1034.

[91] Das, D.; Rahaman, õIR drop analysis in single- and multi-wall carbon nanotube power interconnects in sub-nanometer designs,ö Proc. *IEEE Asia Symposium on Quality Electronic Design (ASQED)*, **2011**, pp.174-183.

[92] Sahoo, M.; Rahaman, H. õPerformance analysis of multiwalled carbon nanotube bundles,ö *In Electronics and Nanotechnology (ELNANO), IEEE XXXIII International Scientific Conference* **2013,** 200-204.

[93] Tang, M.; Mao, J. õModeling and fast simulation of multiwalled carbon nanotube interconnects,ö *IEEE Trans. Electromagnetic Compatibility.* **2015,** 57(2), 232-240.

[94] Fujita, M.; Wakabayashi, K.; Nakada, K.; Kusakabe, K. õPeculiar localized state at zigzag graphite edge,ö *Journal of the Physics Society Japan* **1996**, 65(7), 1920-23.

[95] Nakada, K.; Fujita, M.; Dresselhaus, G.; Dresselhaus, M. S. õEdge state in graphene ribbons: Nanometer size effect and edge shape dependence,ö *Physical Review* **1996**, 54(24), 17954-61.

[96] Echtermeyer, T. J.; Lemme, M. C.; Baus, M.; Szafranek, B. N.; Geim, A. K.; Kurz, H. õNonvolatile switching in graphene field-effect devices,ö *IEEE Electron Device Lett.* **2008**, 29(8), 952-54.

[97] Lemme, M. C.; Echtermeyer, T. J.; Baus, M.; Kurz, H. õA graphene field-effect device,ö *IEEE Electron Device Lett.* **2007**, 28(4), 282-84.

[98] Rawat, B.; Paily, R**.** õAnalysis of graphene tunnel field-effect transistors for analog/RF applications,ö *IEEE Transactions on Electron Devices* **2015**, 62(8), 2663-2669.

[99] Naeemi, A.; Meindl, J. D. õConductance modeling for graphene nanoribbon (GNR) interconnects,ö *IEEE Electron Device Lett*. **2007**, 28(5), 428ó431.

[100] Li, H.; Xu, C.; Srivastava, N.; Banerjee, K. õCarbon nanomaterials for next-generation interconnects and passives: Physics, status and prospects,ö *IEEE Trans. Electron Devices* **2009**, 56(9), 1799-182.

[101] Kan, E. ; Li, Z.; Yang. J. õGraphene nanoribbons: geometric electronic and magnetic properties,ö In *Physics and Applications of Graphene- Theory*, *INTECH,* ed. S. Mikhailov, Chapter 16, **2011.**

[102] Dresselhaus, M. S.; Dresselhaus, G. õ Intercalation compounds of graphite,ö *Advances in Physics* **2002**, 51(1), 1ó186.

[103] Naeemi, A.; Meindl, J. D. õCompact physics-based circuit models for graphene nanoribbon interconnects,ö *IEEE Trans. Electron Devices* **2009,** 56(9), 1822ó33.

[104] Stan, M. R.; Unluer, D.; Ghosh, A.; Tseng, F., õGraphene devices, interconnect and circuits ô challenges and opportunities,ö Proc. *IEEE International Symposium on Circuits and Systems (ISCAS),* Taipei, **2009**, 69-72.

[105] Benedict, L. X.; Crespi, V. H.; Louie, S. G.; Cohen, M. L. õStatic conductivity and superconductivity of carbon nanotubesô Relations between tubes and sheets,ö *Phys. Rev. B, Condens. Matter* **1995**, 52(20) 14935ó40.

[106] Xu, C.; Li, H.; Banerjee, K. õModeling, analysis, and design of graphene nanoribbon interconnects,ö *IEEE Trans. Electron Devices* **2009**, 56(8), 1567-1578.

[107] Hanlon, L. R.; Falardeau, E. R.; Fischer, J. E. õMetallic reł ectance of AsF_5-graphite intercalation compounds,ö *Solid State Commun*. **1977**, 24(5), 377ó81.

[108] Wen-Sheng Zhao; Wen-Yan Yin, õComparative study on multilayer graphene nanoribbon (MLGNR) interconnects,ö *IEEE Transactions Electromagnetic Compatibility* **2014**, 56(3), 638-645.

[109] Nasiri, S. H.; Faez, R.; Moravvej-Farshi, M. K. õCompact formulae for number of conduction channels in various types of grapheme nanoribbons at various temperatures,ö *Mod. Phys. Lett. B* **2012**, 26(1), 1150004-1 - 115004-5.

[110] Hwang, E. H.; Adam, S.; Sarma, S. D. õCarrier transport in two-dimensional graphene layers,ö *Phys. Rev. Lett.* **2007**, 98(18), 186806-1-186806-4.

[111] Yan, J.; Zhang, Y.; Kim, P.; Pinczuk, A. õElectric field effect tuning of electron-phonon coupling in graphene,ö *Phys. Rev. Lett.* **2007**, 98(16), 166802-1-166802-4.

[112] Sarto, M. S.; Tamburrano, A. õComparative analysis of TL models for multilayer graphene nanoribbon and multiwall carbon nanotube interconnects,ö Proc. *IEEE Int. Symp.on Electromagn. Compat.,* Fort Lauderdale, FL, USA, **2010**, 212-217.

[113] Nishad, A. K.; Sharma, R. õAnalytical time-domain models for performance optimization of multilayer GNR interconnects,ö *IEEE J. Select. Topics in Quantum Electronics* **2014**, 20(1), pp. 3700108-1ó3700108-8.

[114] Sahoo, M.; Rahaman, H. õImpact of line resistance variations on crosstalk delay and noise in multilayer graphene nano ribbon interconnects,ö Proc. *International Symposium on Electronic System Design (ISED),* **2014**, 94-98.

[115] Jacob M.; Christos C. H.; Jit, S. õElectronic Devices and Circuits,ö 3rd Edition, Tata McGraw-Hill Publishing Company Limited, **2010**.

[116] Sarvesh, D.; Mirgender, K.; Kumar, T.; Jit, S. õAnalytical modeling of threshold voltage of short-channel strained-Si on Silicon-Germanium-on-Insulator (SGOI) MOSFETs with localized charges,ö *Journal of Computational and Theoretical Nanoscience* **2014**, 11(1), 165-172.

[117] Rawat, B.; Paily, R. õPerformance comparison between graphene based conventional MOSFET and TFET for analog circuits,ö Proc. *Conference on Transport Properties in Low Dimensional Systems: Experiment and Simulation* (TransLES-2014), IASST, Guwahati, **2014**, 11-13.

[118] Schutt-ainé, J. E. õLatency insertion method (LIM) for the fast transient simulation of large networks,ö *IEEE Trans. Circuits and Systems-I: Fundamental Theory and Applications* **2001**, 48(1) 81ó89.

[119] Kurobe, H.; Sekine, T.; Asai, H. õAlternating direction explicit-latency insertion method (ADE-LIM) for the fast transient simulation of transmission lines,ö *IEEE Trans. Components, Packaging, and Manufacturing Technology* **2012**, 2(5), 783ó792.

[120] Sakurai, T.; Newton, A. R. õA simple MOSFET model for circuit analysis,ö *IEEE Trans. Electron Devices* **1991**, 38(4), 887ó894.

[121] International Technology Roadmap for Semiconductors, 2013. [Online]. Available: http://public.itrs.net

[122] Krishnamurthy, R.; Sharma, G. K. õAn area efficient wide range on-chip delay measurement architecture,ö Proc. *Springer VLSI Design and Test* (*VDAT 2013*), Jaipur, **2013**, 49-58.

[123] IEEE Standard P1597, õ Standard for validation of computational electromagnetics computer modeling and simulation ó Part 1,ö 2 2008.

[124] Duffy, A. P.; Martin, A. J. M.; Orlandi, A.; Antonini, G.; Benson, T. M.; Woolfson, M. S. õFeature selective validation (FSV) for validation of computational electromagnetics (CEM). Part I ó The FSV method,ö *IEEE Trans. Electromagnetic Compat*. **2006**, 48(3), 449ó459.

[125] Orlandi, A.; Duffy, A. P.; Archambeault, B.; Antonini, G.; Coleby, D. E.; Connor, S. õFeature selective validation (FSV) for validation of computational electromagnetics (CEM). Part II ó Assessment of FSV performance,ö *IEEE stad.* **2006**, 48(3), 460ó467.

[126] Kumar, M. J. Special issue on õNanoelectronic devices and technology,ö Guest editorial, **2006**, *IETE Journal of Research,* 52 (5).

[127] Mittal, A.; Kumar, M. J. õElectrochemical double layer capacitors featuring carbon nanotubes,ö *Encyclopedia of Nanoscience and Nanotechnology*, 2nd Edition, 13, 263-271, (Edited by H.S.Nalwa), American Scientific Publishers, CA, USA, **2011**.

[128] Chaturvedi, P.; Chouksey, A.; Naik, A.; Kumar, A.; Singh, V.; Rawat, J. S.; Chaudhury, P. K.; Kumar, M. J. õControlled deposition of aligned carbon nanotubes by floating electrodes dielectrophoresis,ö Proc. *IEEE Int. Conf. Emerging Electronics (ICEE2012),* Bombay, India, **2012**, 1-4.

[129] DøAmore, M.; Sarto; M. S.; D'Aloia, A. G. õSkin-effect modeling of carbon nanotube bundles: The high-frequency effective impedance,ö Proc. *IEEE International Symposium on Electromagnetic Compatibility (EMC)*, Fort Lauderdale, **2010**, 847-852.

[130] Sarto, M. S.; Tamburrano, A.; DøAmore, M. õNew electron-waveguide-based modeling for carbon nanotube interconnects,ö *IEEE Trans. Nanotechnol.* **2009**, 8(2), 214 ó 225.

[131] Xu, Y.; Srivastava, A.; Sharma, A. K. õEmerging carbon nanotube electronic circuits, modeling and performance,ö *VLSI Design*, *Hindawi* **2010**, 864165, 1-8.

[132] Sahoo, M.; Rahaman, H. õModeling of crosstalk delay and noise in single-walled carbon nanotube bundle interconnects,ö Proc. *Annual IEEE India Conference* (*INDICON 2013*), Mumbai, India, **2013**, 1-6.

[133] Das, D.; Rahaman, H. õTiming analysis in carbon nanotube interconnects with process, temperature, and voltage variations,ö Proc. *IEEE Int. Symp. Electronic Design* (*ISED 2010*), Bhubaneshwar, India, **2010**, 27-32.

[134] McEuen, P. L.; Fuhrer, M. S.; Park, H. õSingle-walled carbon nanotube electronics,ö *IEEE Trans. Nanotechnol.* **2002**, 1(1), 78-85.

[135] Naeemi, A.; Meindl, J. D. õCarbon nanotube interconnects,ö *Annual Review of Materials Research* **2009**, 39(1), 255ó275.

[136] Wang, Z.; Chen, X.; Zhang, J.; Tang, N.; Cai, J. õFabrication of sensor based on MWCNT for NO_2 and NH_3 detection,ö Proc. *IEEE Conf. on Nanotechnology*, Beijing, **2013**, 2202-2214.

[137] Somvanshi, D; Jit, S. õEffect of ZnO Seed layer on the electrical characteristics of Pd/ZnO thin film based Schottky contacts grown on n-Si substrates,ö *IEEE Trans. Nanotechnology* **2014**, 13(6), 1138-1144.

[138] Park , J. Y.; Rosenblatt , S.; Yaish, Y.; Sazonova , V.; Üstünel, H.; Braig , S.; Arias, T. A.; Brouwer, P. W.; McEuen, P. L. õElectron phonon scattering in metallic single-walled carbon nanotubes,ö *Nano Letters* **2004**, 4(3), 517ó520.

[139] Harris, P. J. F. õCarbon nanotubes and relayed strucrues: New materials for 21st century,ö Cambridge, United Kingdom: Press syndicate of the university of cambridge, **1999**.

[140] Collins, P. G.; Hersam, M.; Arnold, M.; Martel, R.; Avouris, Ph. õCurrent saturation and electrical breakdown in multiwalled carbon nanotubes,ö *Phys. Rev. Lett.* **2001**, 86(14), 3128ó3131.

[141] Li, H.; Banerjee, K. õHigh-frequency analysis of carbon nanotube interconnects and implications for on-chip inductor design,ö *IEEE Trans. Electron Devices* **2009**, 56(10), 2202 ó 2214.

[142] Naeemi, A.; Meindl, J. D. õPhysical modeling of temperature coefficient of resistance for single- and multi-wall carbon nanotube interconnects,ö *IEEE Electron Device Lett.* **2007**, 28(2), 135 ó 138.

[143] Naeemi, A.; Meindl, J. D. õPerformance modeling for single- and multiwall carbon nanotubes as signal and power interconnects in gigascale systems,ö *IEEE Trans. Electron Devices* **2008**, 55(10), 2574 ó 2582.

[144] Maffucci, A.; Miano, G.; Villone, F. õA new circuit model for carbon nanotube interconnects with diameter-dependent parameters,ö *IEEE Trans. Nanotechnol.* **2009**, 8(3), 345 ó 354.

[145] Nieuwoudt, A.; Massoud, Y. õEvaluating the impact of resistance in carbon nanotube bundles for VLSI interconnect using diameter-dependent modeling techniques,ö *IEEE Trans. Electron Devices* **2006**, 53(10), 2460-2466.

[146] Kim, W.; Javey, A.; Tu, R.; Cao, J.; Wang, Q.; Dai, H. õElectrical contacts to carbon nanotubes down to 1 nm in diameter,ö *Appl. Phys. Lett.* **2005**, 87(17), 173101.

[147] Nieuwoudt, A.; Massoud, Y. õUnderstanding the impact of inductance in carbon nanotube bundles for VLSI interconnect using scalable modeling techniques,ö *IEEE Trans. Nanotechnol.* **2006**, 5(6), 758-765.

[148] Nieuwoudt, A.; Massoud, Y. õPerformance implications of inductive effects for carbon-nanotube bundle interconnect,ö *IEEE Electron Device Lett.* **2007**, 28(4), 305 ó 307.

[149] Raychowdhury, A.; Roy, K. õModeling of metallic carbon-nanotube interconnects for circuit simulations and a comparison with Cu interconnects for scaled technologies,ö *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **2006**, 25(1), 58-65.

[150] Courant, R.; Friedrichs, K.; Lewy, H. õOn the partial difference equations of mathematical physics,ö *IBM J. of Research and develop*. **1967,** 11(2), 215-234.

[151] Agrawal, S.; Raghuveer, M. S.; Ramprasad, R.; Ramanath, G. õMultishell carrier transport in multiwalled carbon nanotubes,ö *IEEE Trans. Nanotechnol.* **2007**, 6(6), 722-726.

[152] Nieuwoudt, A.; Massoud, Y. õOn the optimal design, performance, and reliability of future carbon nanotube-based interconnect solutions,ö *IEEE Trans. Electron Devices* **2008**, 55(8), 2097 ó 2110.

[153] Maffucci, A.; Miano, G.; Villone, F. õPerformance comparison between metallic carbon nanotube and copper nano-interconnects,ö *IEEE Trans. Adv. Packag.* **2008**, 31(4), 692 ó 699.

[154] Fathi, D.; Forouzandeh, B.; Mohajerzadeh, S.; Sarvari, R. õAccurate analysis of carbon nanotube interconnects using transmission line model,ö *Micro & Nano Lett.* **2009**, 4(2), 116 ó 121.

[155] Lim, S. C.; Jang, J. H.; Bae, D. J.; Han, G. H.; Lee, S.; Yeo, I., S.; Lee, Y. H. õContact resistance between metal and carbon nanotube interconnects: Effect of work function and wettability,ö *Appl. Phys. Lett.* **2009**, 95(26), 264103-1 ó 264103-3.

[156] Koo, K., H.; Cho, H.; Kapur, P.; Saraswat, K., C. õPerformance comparison between carbon nanotubes, optical and Cu for future high-performance on-chip interconnect applications,ö *IEEE Trans. Electron Devices* **2007**, 54(12), 3206 ó 3215.

[157] Bellucci, S.; Onorato, P. õThe role of the geometry in multiwall carbon nanotube interconnects,ö *J. Appl. Phys.* **2010**, 108(7), 073704-1 - 073704-9.

[158] Rossi, D.; Cazeaux, J. M.; Metra, C.; Lombardi, F. õModeling crosstalk effects in CNT bus architecture,ö *IEEE Trans. Nanotechnol*. **2007**, 6(2), 133ó145.

[159] Eo, Y.; Eisenstadt, W. R.; Jeong, J. Y.; Kwon, O., K. õA new on-chip interconnect crosstalk model and experimental verification for CMOS VLSI circuit design*," IEEE Trans. Electron Devices* **2000**, 47(1),129ó140.

[160] Arvind, M.; Bhardwaj, A. õPower reduction in on-chip interconnection network by serialization,ö Proc. *IEEE Int. Conf. Symp. on Low Power Electronics Design (ISLPED 2008),* Bangalore, **2008**, 201-204.

[161] Mezhiba, A. V.; Friedman, E. G. õInductive properties of high-performance power distribution grids,ö *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2002**, 10(6), 762ó776.

[162] Kahng, A. B.; Muddu, S.; Vidhani, D. õNoise and delay uncertainty studies for coupled RC interconnects,ö Proc. *IEEE International ASIC/SOC Conference*, Washington, DC, **1999**, 3-8.

[163] Nagpal, R.; Bharadwaj, A.; Madan, A. õINTACTE: An interconnect area, delay, and energy estimation tool for microarchitectural explorations,ö Proc. *International Conference on Compilers, Architecture, and Synthesis for Embedded systems*, 2007, 238-247.

[164] Sharma, R.; Chakravarty, T.; Bhattacharyya, A. B. õAnalytical modeling of microstrip-like interconnects in presence of ground plane aperture,ö *IET Microwaves, Antennas and Prop*. **2009**, 3(1), 14-22.

[165] Yi, M.; Swaminathan, M.; Qian, Z.; Aydiner, A. õSkin effect modeling of interconnects using the Laguerre-FDTD scheme,ö Proc. *21st Conference on Electrical Performance of Electronic Packaging and Systems* (EPEPS), Tempe, **2012**, 236-239.

[166] Mezhiba, A. V.; Friedman, E. G. õImpedance characteristics of power distribution grids in nanoscale integrated circuits,ö *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2004**, 12(11), 1148-1155.

[167] Nasiri, S. H.; Moravvej-Farshi, M. K.; Faez, R. õTime domain analysis of graphene nanoribbon interconnects based on transmission line model,ö *Iranian Journal of Electrical & Electronic Engineering* **2012**, 8(1), 37-44.

[168] Nasiri, S. H.; Moravvej-Farshi, M. K.; Faez, R. õStability analysis in graphene nanoribbon interconnects,ö *IEEE Electron Device Lett*. **2010**, 31(12), 1458ó1460.

[169] Bhattacharya, S.; Das, S.; Das, D.; Rahaman, H. õElectrical transport in graphene nanoribbon interconnect,ö Proc. *International Conference on Devices, Circuits and Systems (ICDCS),* Combiatore*,* **2014**, 1-4.

[170] Das, D.; Rahaman, H., õSimultaneous switching noise and IR drop in graphene nanoribbon power distribution networks,ö Proc. *IEEE Conference on Nanotechnology (IEEE-NANO),* **2012**, 20-23.

[171] Araneo, R.; Burghignoli, P.; Lovat, G.; Hanson, G. W. õModal propagation and crosstalk analysis in coupled graphene nanoribbons,ö *IEEE Transactions Electromagnetic Compatibility* **2015**, 57(4), 726-733.

[172] Nandy, T.; Dutta, A.; Haque, M. A.; Mahmood, Z. H. õHigh frequency compatibility of doped multilayer graphene nanoribbon in VLSI interconnect with respect to skin depth

effect and layer width variation,ö Proc. *International Conference on Informatics, Electronics & Vision (ICIEV),* **2014**, 23-24.

[173] Morris, J. E. õNanotechnology materials for electronics reliability,ö Proc. *IEEE 31st Int. Spring Seminar on Electronics Technology*, Budapest, **2008**, 211-215.

[174] Fang, Y.; Zhao, W. S.; Wang, X.; Jiang, F.; Yin, W. Y. õCircuit modelling of multilayer graphene nanoribbon (MLGNR) interconnects,ö Proc. *IEEE Asia-Pacific Symp. on Electromagn. Compat. (APEMC)*, Singapore, **2012**, 625-628.

[175] Kumar, P.; Singh, A.; Garg, A.; Sharma, R. õCompact models for transient analysis of single-layer graphene nanoribbon interconnects,ö Proc. *IEEE Int. Conf. Computer Modelling and Simulation (UKSim2013)*, Cambridge, **2013**, 809-814.

[176] Xu, C.; Li, H.; Banerjee, K. õGraphene nano-ribbon (GNR) interconnects: A genuine contender or a delusive dream?,ö Proc. *IEEE Int. Electron Devices Meeting* (IEDM 2008), San Francisco, CA, USA, **2008**, 1-4.

[177] Moon, J. S.; Gaskill, D. K. õGraphene: Its fundamentals to future applications,ö *IEEE Trans. Microw. Theory Tech*. **2011**, 59(10), 2702ó 2708.

[178] Bandyopadhyay, T.; Han, K. J.; Chung, D.; Chatterjee, R.; Swaminathan, M.; Tummala, R. õRigorous electrical modeling of through silicon vias (TSV) for MOS capacitance effects,ö *IEEE Trans. Compon. Packag. Manuf. Technol.* **2011**, 1(6), 893-903.

[179] Jiang, L. L.; Mao, J. F.; Wu, A. L. õSimplistic finite-difference time domain method for Maxwell equations,ö *IEEE Trans. Magn.* **2006**, 42(8), 1991ó1995.

[180] Bawa, S.; Sharma, G. K. õA parallel transitive closure computation algorithm for VLSI test generation,ö Proc. *6th Int. Conf. Applied Parallel Computing Advanced Scientific Computing*, London, UK, **2002**, 243-252.

[181] Farahat, N.; Raouf, H.; Mittra, R. õAnalysis of interconnect lines using the finite-difference time-domain (FDTD) method,ö *Microw. Opt. Technol. Lett.* **2002**, 34(1), 6ó9.

[182] Taflove, A. õComputational Electrodynamics,ö Norwood, MA: Artech House, **1995**.

[183] Strikwerda, J. C. õFinite difference schemes and partial differential equations,ö Pacific Grove, CA: Brooks/Cole, **1989**.

[184] Lee, Y. M.; Chen, C. õPower grid transient simulation in linear time based on transmission line-modeling alternating-direction implicit method,ö Proc. *IEEE Int. Conf Computer Aided Design (ICCAD)*, USA, **2001**, 75-80.

[185] Namiki, T. õA new FDTD algorithm based on alternating-direction implicit method,ö *IEEE Trans. Microwave Theory and Techniques* **1999**, 47(10), 2003ó2007.

[186] Wang, W.; Liu, P.G.; Qin, Y.J. õAn unconditional stable 1D-FDTD method for modeling transmission lines based on precise split-step scheme,ö *Progress In Electromagnetics Research* **2013**, 135, 245ó260.

[187] Kong, Y.; Chu, Q.; Li, R. õTwo efficient unconditionally-stable four-stages split-step FDTD methods with low numerical dispersion,ö *Progress in Electromagnetics Research B* **2013**, 48, 1ó22.

[188] Sun, C.; Trueman, C. W. õUnconditionally stable CrankóNicolson scheme for solving two-dimensional Maxwellφs equations,ö *Electron. Lett.* **2003**, 39(7), 595ó597.

[189] Tan, E. L. õEfficient algorithms for Crank-Nicolson-based finite difference time-domain methods,ö *IEEE Trans. Microwave Theory and Tech.* **2008**, 56(2), 408ó413.

[190] Tang, M.; Mao, J. F. õA precise time-step integration method for transient analysis of lossy nonuniform transmission lines,ö *IEEE Trans. Electromagn. Compat.* **2008**, 50(1), 166ó174.

[191] Afrooz, K.; Abdipour, A. õEfficient method for time-domain analysis of lossy nonuniform multiconductor transmission line driven by a modulated signal using FDTD technique,ö *IEEE Trans. Electromag. Compat.* **2012**, 54(2), 482ó494.

[192] Jia, L.; Shi, W.; Guo, J. õArbitrary-difference precise-integration method for the computation of electromagnetic transients in single-phase nonuniform transmission line,ö *IEEE Trans. Power Delivery* **2008,** 23, 1488-1494.

[193] Kang, S. M.; Leblebici, Y. õCMOS digital integrated circuits: Analysis and design,ö 3rd ed. Tata McGraw-Hill, **2003**.

[194] Kantartzis, V. N.; Tsiboukis, T. D. õModern EMC analysis techniques volume I: Time-domain computational schemes,ö *Synth. Lectures Comput. Electromagn.*, 1st ed., **2008**, 1ó 224.

[195] Maxwell 2D student version, Ansoft Corp., Pittsburgh, PA., **2005**.

[196] FastHenry version 3.32, http://www.fastfieldsolvers.com, **2011**

[197] Tan, M. L. P., Arora, V. K.; Saad, I.; Ahmadi, M., T.; Ismail, R. õThe drain velocity overshoot in an 80 nm metal-oxide-semiconductor field-effect transistor,ö *Journal of Applied Physics* **2009**, 105(7) 074503-1 ó 074503-7.

[198] Sentaurus user manuals, Synopsys, Inc., Mountain View, CA, USA, **2015**.

List of Publications

Journals/Magazines

[1] **V. Ramesh Kumar**, A. Alam, B. K. Kaushik, and A. Patnaik, õAn unconditionally stable FDTD model for crosstalk analysis of VLSI interconnects,ö *IEEE Transactions Components, Packaging and Manufacturing Technology*, vol. 5, no. 12, pp. 1810-1817, Dec. 2015. (Thomson Reuters Impact Factor: 1.18).

[2] **V. Ramesh Kumar**, M. K. Majumder, N. R. Kukkam, and B. K. Kaushik, õTime and frequency domain analysis of MLGNR interconnects,ö *IEEE Transactions Nanotechnology*, vol. 14, no. 3, pp. 484-492, May 2015 (Thomson Reuters Impact Factor: 1.825).

[3] **V. Ramesh Kumar**, B. K. Kaushik, and A. Patnaik, õAn accurate FDTD model for crosstalk analysis of CMOS-gate-driven coupled RLC interconnects,ö *IEEE Transactions Electromagnetic Compatibility*, vol. 56, no. 5, pp. 1185-1193, Oct. 2014 (Thomson Reuters Impact Factor: 1.297).

[4] **V. Ramesh Kumar**, M. K. Majumder, and B. K. Kaushik, õGraphene based on-chip interconnects and TSVs ó prospects and challenges,ö *IEEE Nanotechnology Magazine*, vol. 8, no. 4, pp. 14-20, Nov. 2014.

[5] B. K. Kaushik, M. K. Majumder, and **V. Ramesh Kumar**, õCarbon nanotube based 3-D interconnects - A reality or a distant dream,ö *IEEE Circuits and Systems Magazine*, vol.14 no. 4, pp. 16-35, Nov. 2014 (Thomson Reuters Impact Factor: 2.517).

[6] M. K. Majumder, J. Kumar, **V. Ramesh Kumar**, and B. K. Kaushik, õPerformance analysis for randomly distributed mixed carbon nanotube bundle interconnects,ö *IET Micro & Nano Letters*, vol. 9, no. 11, pp. 792-796, Dec. 2014 (Thomson Reuters Impact Factor: 0.853).

[7] **V. Ramesh Kumar**, B. K. Kaushik, and A. Patnaik, õCrosstalk noise modeling of multiwall carbon nanotube (MWCNT) interconnects using Łnite-difference time-domain (FDTD) technique,ö *Microelectronics Reliability* (*Elsevier*), vol. 55, no. 1, pp. 155-163, Jan. 2015 (Thomson Reuters Impact Factor: 1.433).

[8] **V. Ramesh Kumar**, B. K. Kaushik, and A. Patnaik, õImproved Crosstalk Noise Modeling of MWCNT Interconnects Using FDTD Technique,ö *Microelectronics Journal* (*Elsevier*) vol. 46, no. 12, pp. 1263-1268, Dec. 2015, (Thomson Reuters Impact Factor: 0.836).

[9] **V. Ramesh Kumar**, B. K. Kaushik, and A. Patnaik, õAn accurate model for dynamic crosstalk analysis of CMOS gate driven on-chip interconnects using FDTD method,ö *Microelectronics Journal* (*Elsevier*), vol. 45, no. 4, pp. 441-448, April 2014 (Thomson Reuters Impact Factor: 0.836).

[10] **V. Ramesh Kumar**, M. K. Majumder, A. Alam, N. R. Kukkam, and B. K. Kaushik, õStability and delay analysis of multi-layered GNR and multi-walled CNT interconnects,ö *Journal of Computational Electronics* (Springer), vol. 14, no. 2, pp. 611-618, June 2015 (Thomson Reuters Impact Factor: 1.520).

[11] M. K. Majumder, P. K. Das, **V. Ramesh Kumar**, and B. K. Kaushik õCrosstalk induced delay analysis of randomly distributed mixed CNT bundle interconnect,ö *Journal of Circuits, Systems and Computers*, vol. 24, no. 10, pp. 1550145-1−1550145-15, Dec. 2015 (Thomson Reuters Impact Factor: 0.33).

<u>Conferences</u>

[1] **V. Ramesh Kumar**, B. K. Kaushik, and A. Patnaik, õModeling of crosstalk effects in coupled MLGNR interconnects based on FDTD method,ö in *Proc. IEEE Electronic Components and Technology Conference* (ECTC), Florida, USA, pp. 1091-1097, May 2014.

[2] A. Alam, M. K. Majumder, A. Kumari, **V. Ramesh Kumar,** and B. K. Kaushik, õPerformance analysis of single- and multi-walled carbon nanotube based through silicon vias,ö in *Proc. IEEE Electronic Components and Technology Conference* (ECTC), Marina San Diego, USA, pp. 1834-1839, May 2015.

[3] **V. Ramesh Kumar**, B. K. Kaushik, and A. Patnaik, õDynamic crosstalk analysis of CMOS driven RLC interconnects using FDTD method,ö in *Proc. IEEE Radio Science Meeting AP-S/USNC-URSI*, Florida, USA, p.80, July 2013.

[4] **V. Ramesh Kumar**, B. K. Kaushik, and A. Patnaik, õCrosstalk modeling with width dependent MFP in MLGNR interconnects using FDTD technique,ö in *Proc. IEEE Conference on Electron Devices and Solid-State Circuits*, Singapore, pp. 138-141, June 2015.

[5] M. K. Majumder, A. Kumari, A. Alam, **V. Ramesh Kumar** and B. K. Kaushik õSignal integrity improvement with peripherally placed MWCNTs in mixed CNT bundle based TSVs,ö in *Proc. IEEE Conference on Electron Devices and Solid-State Circuits*, Singapore, pp. 649-652, June 2015.

[6] **V. Ramesh Kumar**, B. K. Kaushik, and A. Patnaik, õPerformance comparison of multilayer graphene nanoribbon and copper based VLSI interconnects,ö *Presented in Nano India 2013*, Trivandrum, Feb. 2013.

Books

[1] **V. Ramesh Kumar**, M. K. Majumder, A. Alam and B. K. Kaushik, õThrough Silicon Vias ó Materials, Models, Design and Performance,ö *CRC Press, Taylor & Francis* (In-Press).

[2] **V. Ramesh Kumar**, B. K. Kaushik and A. Patnaik, õCrosstalk in Modern On-Chip Interconnects: A FDTD Approach,ö *Springer Briefs in Applied Sciences and Technology* (In-Press).