SIMULATION AND MODELLING OF MULTIGATE MOSFETS FOR ANALOG APPLICATIONS

Ph.D. THESIS

by

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INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **"SIMULATION AND MODELLING OF MULTIGATE MOSFETS FOR ANALOG APPLICATIONS"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electronics and Communication Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from July, 2010 to April, 2015 under the supervision of **Dr. S. Dasgupta**, Associate Professor and **Dr. A. K. Saxena**, Professor, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

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This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

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ABSTRACT

Complementary metal oxide semiconductor (CMOS) integrated circuits (ICs) have seen overwhelming growth in electronic industry with gadgets for entertainment, communication, computing, signal processing and other applications. Low power consumption, reduced area, increased speed and lower production cost per chip etc., are some advantages of CMOS technology that have opened the door for integration of millions of transistors on a single chip. It is also believed that, with technology scaling, the trend of rapid improvements in performance of CMOS ICs will continue in near future. Advancement in CMOS technology in modern times has further ensured not only higher packing density but also improved performance in digital, analog and mixed signal circuit design.

However, as the number of transistors that are integrated per chip is increased, the problems of leakage currents, thermal management, reliability etc. have also been pronounced. These problems are posing great threat to circuit designer in recent years, because of increasing use of battery operated portable electronic gadgets in various spectrum of life. Starting from micro environmental sensors and radio frequency identification to personal digital assistants like laptops, cell phones, cameras etc., the demand for ultra low power consumption and prolonged battery life is increasing day by day. Therefore, single gate bulk CMOS devices scaled below 100nm gate length are practically losing its credibility with pronounced increase in short channel effects (SCEs) that degrades the battery run time in these portable devices. Multi-gate (MG) MOSFETs such as double gate (DG), triple gate (TG) and gate all around (GAA) MOSFETs etc., on the other hand, posses good properties like, near ideal subthreshold slope, improved threshold voltage roll-off and drain induced barrier lowering (DIBL).

More importantly, due to better channel control, the channel region of MG MOSFETs can be left undoped or lightly doped. This leads to enhanced carrier mobility and lower random doping fluctuation (RDF) effects that are some added advantages of MG MOSFETs.

Digital/analog circuits design with MOSFETs operating in subthreshold and weak/moderate inversion regime have gained wide interest these days due to their suitability for battery operated portable applications requiring ultra low power consumption, high gain with low/moderate frequency of operation. One of the major concerns for circuit design at this operation regime of device is its increased sensitivity to process, voltage and temperature variations. In addition, gate length scaling in nano-meter regime worsens various short channel effects (SCEs) that are posing serious threats to both digital and analog performance of the device. Considerable attention has been given for analyzing super threshold circuit behavior with progressive technology scaling, but no such attention has been given to subthreshold or weak/moderate inversion circuits, particularly using MG MOSFETs with circuit co-design techniques.

Volume inversion in MG MOSFET is one of the important properties in this regard that has to be used effectively for performance improvement. The volume inverted carriers are confined at the center of the channel rather than at Si-SiO_2 interface. This results in (i) Higher current due to great increase in number of minority carriers (ii) Reduction in surface scattering and interface defects (iii) Higher carrier mobility due to use of thick volume inversion as compared to narrow surface inversion and (iv) Higher transconductance. Secondly, for channel thickness between 5nm to 20nm, the volume inversion mobility of minority carriers are improved substantially at low temperature than at room temperature. These special features enhance the current

drive, transconductance, subthreshold slope and speed of the device. Secondly, use of high-*k* gate dielectric material is beneficial in expanding design space due to possible use of thicker gate dielectric that can reduce the gate tunneling leakage while the device dimensions are scaled down in nano-meter regime. Nevertheless, fringe induced barrier lowering (FIBL) is fast becoming a major concern that can worsen SCEs, enhances off current and introduces threshold voltage roll–off because of loss of gate electrostatic control over the channel region. Third, Fin type FET (FinFET) has almost all advantages of MG MOSFETs in addition to lesser design related issues because of its self aligned gates. Providing sufficient underlap to the FinFET can enhance the digital performance because of variation in effective gate length in strong and weak inversion regime of operation of device. The analog performance of this kind of underlap FinFET is enhanced at subthreshold/weak inversion regime due to higher effective gate length. Nevertheless, introducing high-*k* spacer dielectric in underlap section of FinFET can enhance the digital performance because of gate fringe induced barrier lowering (GFIBL) effect. Dual-*k* spacer based underlap FinFET is another option for suppressing direct source to drain tunneling (DSDT) and short channel effects due to effective increase in gate fringing fields near gate edges of device via inner high-*k* spacer dielectric.

This issue is addressed as first part of the work with detailed analysis of the impact of dual-*k* spacer on analog and short channel performance of device. The length of inner high-*k* spacer dielectric is optimized in terms of these performances. Suitable fin thickness is selected to account for the volume inversion effect too. From the study, we conclude that dual-*k* spacer formation in underlap FinFET is an attractive option in controlling DSDT, SCEs and improving analog figures of merit (FOM). The transconductance and output conductance improves in all extension lengths

irrespective of doping gradient. Use of optimized inner high-k spacer length can compensate the increase in capacitance by transconductance improvement which can produce almost the same cutoff and maximum oscillation frequency as compared to low-k FinFET, in addition to a large increase in intrinsic gain. Transconductance-to-current ratio and early voltage are also observed to improve by formation of dual-k spacer in underlap FinFET. More so, pronounced effect of barrier modulation result in improved frequencies (f_T and f_{max}) and intrinsic gain as the devices are scaled in nano-meter regime. In the second part of the work, detailed analysis of the effect of variations on crucial device parameters like gate oxide thickness (T_{ox}), fin width (W_{fin}), lateral straggle (X_j) of source drain doping profile etc., are carried out to formulate a guideline for dual-k spacer underlap FinFET design in analog domain. The process induced variations in these parameters are becoming more prominent with shrinking device dimensions causing negative impact on the inter device variability and, in turn, degrading the mismatch parameter. More so, the effect of alternative inner high-k spacer dielectric materials on analog performance of the device is studied in detail. It is shown that, for an optimum aspect ratio (fin height/fin width), the FOM of dual-k N/P-FinFETs are considerably higher and posses lesser variation to fin width, oxide thickness and S/D lateral straggle which, in turn, can improve the lithographic limitations at process level. Subsequently, the work has been extended to study the effect of spatial variations in critical transistor attributes, T_{ox} and X_j of underlap FinFET, on single stage operational transconductance amplifier (OTA) performance. It is observed that, improved and variation less threshold voltage and mobility of dual-k FinFET are crucial in improving analog FOM like A_{DM}, A_{CM} and CMRR of the OTA.

The analog performance of the device can be enhanced at low temperature environment because of improved threshold voltage due to increase in fermi potential and improved carrier mobility due to volume inversion, subband splitting, reduced phonon scattering and enhanced velocity overshoot effect at liquid nitrogen range (≥77K). Therefore, in third part of our work, extensive study of low temperature operation of underlap FinFET is carried out. It is shown that, as the temperature is lowered to 100K, the percentage improvements in analog FOM of dual-*k* FinFET are enhanced further because of improvement in mobility and threshold voltage. Secondly, scaling down the gate length of dual-*k* FinFET to 10nm seems feasible at 100K temperature range, which can target A_{V0}, f_T and f_{max} of ~44dB, 242GHz and 302GHz respectively.

Fourth part of the work deals with development of analytical models for double gate underlap FinFET. The change in electric field line path between two different dielectric interfaces (ε_h and ε_l) of underlap section and its effect, is the part that have been modeled for the first time. Each underlap section has been divided into two parts low-*k* and high-*k* section. Modelling of inner high-*k* section is carried out by conformal mapping technique where as modeling of outer low-*k* section has been carried out by solving continuity equations in two different (low-*k*/high-*k*) dielectric interface and considering change in effective gate heights for the elliptical field lines at dielectric interface. It is shown that, the proposed model captures well the effect of inner high-*k* spacer on change in electric field lines at dielectric interface and its subsequent effect on potential profile of dual-*k* spacer based underlap FinFET. Furthermore, the model matches well with TCAD sentaurus device simulation results with variation in crucial device dimensions such as, gate oxide thickness, inner high-*k* spacer length and its dielectric constant.

With lightly doped channel, the source/drain dopant species can intrude into the channel region when rapid thermal processing step following the high temperature annealing is performed to activate the dopant species. Therefore, final part of our work deals with generation of compact model for DG MOSFET that considers the effect of lateral straggle of source/drain gaussian profile. It has been observed that, increase in lateral straggle of source/drain gaussian profile facilitates propagation of lateral electric field which, in turn, lowers the threshold voltage and effective channel length of the device. These two effects will alter the current drive and change crucial parameters like transconductance, output conductance and, in turn, intrinsic gain of the device. Finally conclusions are drawn based on the findings of the research. Future scope of the work is also enumerated.

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Date:

Place: (Ashutosh Nandi)

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LIST OF SYMBOLS

e_h	Eccentricity of High-*k* Dielectric
e_l	Eccentricity of Low-*k* Dielectric
f_{max}	Maximum Oscillation Frequency
f_T	Cutoff Frequency
g_{ds}	Output Conductance
g_m	Transconductance
g_m/I_{ds}	Transconductance-to-current Ratio
k	Boltzmann's Constant
l_d	Channel Length Modulation Factor
n_i	Intrinsic Carrier Density of Semiconductor
$n_{i,eff}$	Effective Intrinsic Carrier Density of Semiconductor
q	Electronic Charge
s_D	Spin Degeneracy Factor
t	Time
v_t	Thermal Voltage
x	Channel Length Direction
y	Body Thickness Direction
Al_2O_3	Silicon Oxide
A_{CM}	Common Mode Gain
A_{DM}	Differential Mode Gain
A_{V0}	Intrinsic DC Gain
C_d	Depletion Capacitance per Unit Area
C_{gg}	Total Gate Oxide Capacitance per Unit Area
C_{gd}	Gate to Drain Capacitance per Unit Area
C_{if}	Inner Fringe Capacitance per Unit Area

C_{of}	Outer Fringe Capacitance per Unit Area
C_{ox}	Gate Oxide Capacitance per Unit Area
C_{si}	Silicon Body Capacitance per Unit Area
D_{eff}	Effective Drain End
E_{eff}	Effective Electric Field
$E(e_x)$	Elliptical Integral
E_g	Silicon Band Gap Energy
$E_{g,eff}$	Effective Band-gap Energy
E_i	Ionization Energy
E_{i0}	Ionization Energy of Undoped Silicon
E_x	X Directional Electric Field
E_y	Y Directional Electric Field
E_z	Z Directional Electric Field
E_C	Critical Electric Field
E_D	Donor Level Energy
E_F	Fermi Level Energy
H_{fin}	Fin Height
HfO_2	Hafnium Oxide
$I_{D,lin}$	Linear Drain Current
$I_{D,sat}$	Total Saturation Drain Current
I_{off}	‘off’ State Leakage Current
I_{on}	‘on’ State Driving Current
I_{sub}	Sub-threshold Leakage Current
I_{CBO}	Gate Lekage Current
L_{arch}	Elliptical Arc Length of High-*k* Dielectric
L_{arcl}	Elliptical Arc Length of Low-*k* Dielectric
$LaAlO_3$	Lanthanum Aluminate

L_{eff}	Effective Channel Length
L_{elec}	Electrical Length
L_{ext}	Spacer Extension Length
L_g	Channel Length
$L_{sp,lk}$	Low-*k* Spacer Extension Length
$L_{sp,hk}$	High-*k* Spacer Extension Length
L_{un}	Channel Underlap Length
N_a	Channel Acceptor Doping Concentration
N^-_a	Ionized Acceptor Concentration
N_d	Channel Donor Doping Concentration
N^+_d	Ionized Donor Concentration
N_{de}	Degenrated Doping Concentration
$NdGaO_3$	Neodymium Gallate
$N_{SD}(p)$	Peak Doing Concentration of Source/Drain Doping Profile
$N^+_{SD}(x)$	Ionized Source/Drain Donor Doping Concentration
$N_{SD}(x)$	Lateral Source/Drain Doping Profile
Q_b	Bulk Charge
Q_{DEP}	Depletion Charge
Q_{INV}	Inversion Charge
S_{eff}	Effective Source End
Si_3N_4	Silicon Nitride
SiO_2	Silicon Dioxide
SS	Sub-threshold Slope Factor
T	Temperature
T_g	Gate Height
TiO_2	Titanium Dioxide
T_{ox}	Gate Oxide Thickness

T_{si}	Channel Thickness of Multigate Device
V_{bi}	Built in Potential
V_{dd}	Supply Voltage
V_{fb}	Flat- Band Voltage
V_{th}	Threshold Voltage
V_{DS}	Drain to Source Voltage
$V_{DS,sat}$	Drain to Source Saturation Voltage
V_{EA}	Early Voltage
V_{GS}	Gate to Source Voltage
W	Channel Width
W_{fin}	Fin Thickness
ΔE_g	Change in Band-gap Energy
ΔI_D	Shift in Drain Current
ΔV_{th}	Shift in Threshold Voltage
ε_h	Permittivity of High-*k* Dielectric
ε_l	Permittivity of Low-*k* Dielectric
ε_{ox}	Permittivity of Silicon Dioxide
ε_{si}	Permittivity of Silicon
ϕ	Fermi Potential
λ	Natural Length
λ_a	Velocity Overshoot Effect Factor
μ	Channel Carrier Mobility
μ_n	Electron Mobility
Ψ (x, y)	2D Potential along x, y Directions
Ψ_b (x)	Body Potential along x Direction
Ψ_f (x)	Front Surface Potential along x Direction

$\Psi_{tsi}(x)$	Back Surface Potential along x Direction
σ	Doping Gradient of Source/Drain Doping Profile
σ_L	Lateral Straggle of Source/Drain Doping Profile

LIST OF ABBREVIATIONS

ACF	Auto Correlation Function
AR	Aspect Ratio
BG	Back Gate
BJT	Bipolar Junction Transistor
BOX	Buried Oxide
BTBT	Band-to-Band Tunneling
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
DG	Double Gate
DG-FinFET	Double Gate Fin Field Effect Transistor
DG MOSFET	Double gate Metal Oxide Field Effect Transistor
DIBL	Drain Induced Barrier Lowering
DMDG	Dual Metal Double Gate
DRAM	Dynamic Random Access Memory
DSDT	Direct Source to Drain Tunneling
DSS	Dopant Segregated Schottky
EDGE	Enhance Data rate for GSM Evolution
EI	Electrostatic Integrity
EOT	Equivalent Oxide Thickness
FD	Fully Depleted
FET	Field Effect Transistor
FG	Front Gate
FIBL	Fringe Induced Barrier Lowering
FinFET	Fin Field Effect Transistor
FOM	Figures of Merit

FSB	First Sub-Band
GAA	Gate-All-Around
GAA MOSFET	Gate-All-Around MOSFET
GFIBL	Gate Fringe Induced Barrier Lowering
GIDL	Gate Induced Drain Leakage
GSM	Global System for Mobile
HDD	Highly Doped Drain
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
LER	Line Edge Roughness
LNA	Low Noise Apmlifier
LSI	Large Scale Integration
LWR	Line width Roughness
MLDA	Modified Local Density Approximation
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MUG	Masson’s Unilateral Gain
N-FinFET	n-Channel FinFET
NMOS	n-Channel MOSFET
OPAMP	Operational Amplifier
OTA	Operational Transconductance Amplifier
OTV	Oxide Thickness Variation
PAI	Pre Amorphization Implant
PD-SOI	Partially Depleted Silicon-on-Insulator
P-FinFET	p-Channel FinFET
PMOS	p-Channel MOSFET
PPM	Parts per Million

RIE	Reactive Ion Etching
RTP	Rapid Thermal Processing
SCE	Short Channel Effect
S/D	Source/Drain
SG	Single Gate
SG-SOI	Single Gate Silicon-on-Insulator
SIMS	Secondary Ion Mass Spectrometry
SoC	System-on-Chip
SOI	Silicon on Insulator
SOI MOSFET	Silicon on Insulator MOSFET
SNWT	Silicon Nano Wire Transistor
SRAM	Static Random Access Memory
SRH	Shockley–Read–Hall
TCAD	Technology Computer Aided Design
TED	Transient Enhance Diffusion
TFET	Tunnel Field Effect Transistor
TG	Tripple Gate
TG MOSFET	Tripple Gate MOSFET
USJ	Ultra Shallow Junction
VLSI	Very Large Scale Integration

Chapter 1

Introduction

1.1 Introduction:

Moore's law proposed at least twofold increase in number of devices on a single chip every two years since the invention of complementary metal oxide semiconductor (CMOS) [1]. This increase in number of transistors per chip combined with decreasing average cost of production has lead to possible high speed and complex designs [2]. Present day electronic gadgets are so small and so economical that billions of basic functions can be performed by a hand held system. Since early 1990's, academia and researchers from various semiconductor companies have teamed up for accurate prediction of the future of semiconductor industries. Their initiatives resulted in a well organized body "International Technology Roadmap for Semiconductors (ITRS)" [3]. ITRS issues a yearly basis report, which serve as a benchmark for various semiconductor industries and academic institutions around the world. ITRS has predicted that in the near future, the semiconductor devices will achieve the gate length down to 20nm and below, in order to target low power and high performance device operation. Complementary metal oxide semiconductor (CMOS) technology has played a major role in down-scaling the device dimensions, so that realization of compact high performance digital/analog circuits becomes a reality. But when the device dimensions are scaled to this extent, several mulfunctions in device operation start to crop up [4-5]. Therefore, reliability of CMOS technology has become one of the major bottlenecks in the evolution of next generation systems.

Stojadinovic et al. [6] have emphasized the failure physics of integrated circuits and their influence on device reliability. The work is further elaborated in [7], which systematizes different failure modes in integrated circuits. Important tests are enumerated for enhancing

different failure modes and a relationship between failure modes and respective tests for their detection is discussed. This, in turn, raises the instabilities and reliability issues in CMOS integrated circuits. Stress induced instabilities in CMOS can be introduced due to positive gate bias affecting gate dielectric and surface state charges in CMOS transistors [8]. This leads to development of various methods to separate and calculate gate dielectric and surface state charges for effective analysis of instabilities in CMOS integrated circuits [9]. There will be phenomenal influence of these gate oxide charges and interface trap charges on threshold voltage and gain factor of CMOS transistors leading to introduction of fluctuation mechanism in semiconductor devices [10]. Presence of small signal noise in semiconductor devices enhances the fluctuation mechanism further. Therefore, proper guidelines need to be developed for effective small signal noise modelling techniques while opting for numerical simulation of semiconductor devices considering different kinds of fluctuation mechanisms [11]. Subsequently, various authors have reviewed large signal operation of semiconductor devices by physics based numerical simulation in presence of noise that led to evolution of various techniques to measure frequency conversion and noise under this large signal operation [12-13]. Secondly, random doping fluctuations in channel region of device are one of the important causes of variability in nano-scale device. Masoero et al. [14] have evaluated the statistical current fluctuation property, induced by this kind of random doping fluctuations. A linear perturbation theory is adopted to determine the total current fluctuations. Subsequently, a surface potential model that considers this random doping fluctuations effect in device channel had been developed where green's function formulation of external device parameters is used for an efficient circuit level sensitivity analysis [15]. Therefore, when the technology is scaled to nano-meter regime, several device level sensitivity issues are required to be addressed to avoid possible malfunction in device that can possibly hamper circuit operation [4-5].

Some of these major sensitive issues that affect the performance of nano-scale MOSFET are:

- V_{th} roll-off
- Gate Oxide and Interface Trap Charges
- Drain Induced Barrier Lowering (DIBL)
- Increased Subthreshold Source/Drain (S/D) leakage
- Gate Induced Drain Leakage (GIDL)
- Gate direct tunneling and hot carrier effect
- Random Dopant fluctuation
- Controlling junction and depletion depths
- Quantum mechanical tunneling of charge carriers from source to drain and from drain to body of MOSFET
- Control of density and location of dopant atoms in channel and source/drain region of MOSFET to provide a high on/off current ratio
- Interconnect resistance and capacitance

Power consumption and hot carrier effects can be reduced by reducing supply voltage V_{DD} but at the cost of performance degradation. The performance can be improved by lowering threshold voltage; however source/drain leakage is increased with reduction in threshold voltage. Oxide thickness reduction is an approach to reduce DIBL and enhance adequate channel control by gate electrode. However, reducing oxide thickness increases the gate leakage [16]. Therefore, it is quite a challenge to design nano-scale MOSFET that can address all the instability issues in addition to performance improvement.

1.2 Background and Motivation:

The motivation behind this research work is to provide alternative device design to engineers that can address most of the scaling issues as well as performance improvement at compact low power environment in order to satisfy overwhelming demand of present day battery operated

portable devices. Noticeable applications of such devices are in the field of cellular phones, biomedical instruments, wireless sensor networks, ambient intelligent systems and others [17-19]. Elementary digital/analog circuits such as CMOS logic gates, reference circuits, SRAM cells, current mirrors, operational amplifiers are basic building blocks of these battery operated portable gadgets. The semiconductor devices that are used to realize these digital/analog circuits demand low power, high gain and low/moderate frequency of operation. Subthreshold/weak inversion regime of operation of semiconductor devices achieves this target [3], [20-22].More so, subthreshold operation of MOSFET has performance advantages such as better linearity and output impedance in addition to low power consumption and better tolerance to temperature variation. These additional features of the device are most suited while designing signal conditioning circuitry required for environmental sensors [23]. Short channel effects (SCEs) are of serious concern in nano-scaled devices affecting both digital and analog performance. Increasing off state leakage current is another major concern due to pronounced increase in source to drain lateral electric field that deteriorates the gate electrostatic integrity (*EI*). Analog operation of device is another key performance area that is affected most by this loss of *EI*. Therefore, better short channel effect (SCE) immunity and increased gate electrostatic control are of paramount importance in order to pursue scaling at nano-scale regime without deteriorating the performance.

1.2.1 Multigate advantages:

With better channel control and reduced short channel effects, the multi-gate MOSFET is considered to be the successor to planner MOSFET [24-25]. Various multigate MOSFETs are reported recently that have superior scalability because of better short channel immunity and performance improvement. Few examples are, source engineered double gate vertical strained SiGe MOSFET [26] for better I_{on}/I_{off} ratio, gate work function engineered full depleted silicon-on-insulator (FDSOI) MOSFET [27-28], single halo dual material double gate (DMDG)

MOSFET [29-31] for better analog performance, tunneling source MOSFET [32-34] for better SCE and intrinsic gain, novel bottom spacer based FinFET [35] for better power delay and self heating performance etc. Among the multigate family, FinFET is emerging as a promising candidate that can be a suitable alternative to conventional single gate (SG) technologies [36-40]. Larger gate area of FinFET increases drive current of the device while sub-threshold leakage is minimized through reduced channel doping [41]. Further, it has sharper subthreshold slope, which allows better switching in the device. Also, the threshold voltage is controlled without the use of heavy channel doping in fin. Therefore, the effects of random doping fluctuations (RDF) are eliminated [42]. This lightly doped fin reduces the mobility degradation phenomenon due to scattering and can reduce the drain to body band-to-band (BTBT) leakage currents. Secondly, single lithography and etch step in fabrication is an attractive feature of FinFET due to its self aligned gates [43-45]. More so, FinFET is becoming a popular device of choice among mutigate FET that can address scaling and process variation challenges which are generally present in the SG technologies [46]. **Fig. 1.1** shows the schematic of a FinFET. The gate wraps over the thin silicon fin type channel resulting in a quasi-planar symmetrical FinFET structure. All three gates, front and back and top are made up of same material and have same work function. The top and front gate insulators are marked as T_{ox1} and T_{ox2} whereas, T_{ox3} is adjacent to back gate. Various definitions of geometrical parameters of the device shown in the figure are as follows, L_g: effective channel length of FinFET estimated by the metallurgical junction, H_{fin}: height of Si fin defined as the distance between top gate (*TG*) and buried oxide, T_{fin}: thickness of Si fin defined by the distance between front gate (*FG*) and back gate (*BG*) oxides, *W*: geometrical channel width defined as [47]: $W = 2H_{fin} + T_{fin}$.

The main features of FinFET are:

(a) An ultra-thin silicon fin type channel for suppressing short channel effects

(b) Single lithography and etch step in fabrication is possible due to its self aligned gates

(c) Raised source/drain structure for reducing parasitic resistance

(d) Gate last process compatible with low temperature and high-*k* gate dielectrics

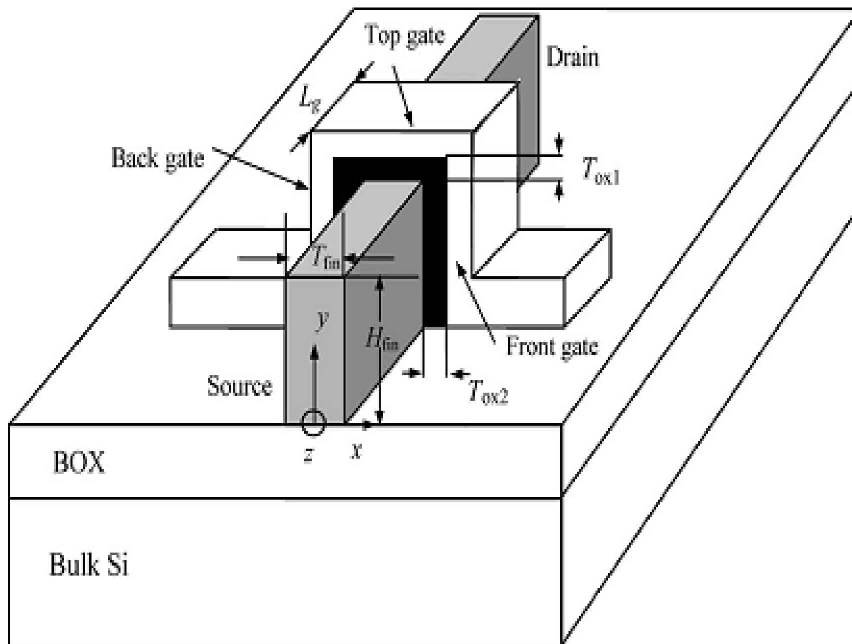

Fig. 1.1. Schematic of FinFET.

Integration of high-*k* dielectric material is an added advantage. It is reported that, titanium oxide (TiO_2) can be used as alternative storage dielectrics for DRAM applications [48-49] due to its high permittivity and excellent step coverage. TiO_2 based MOS capacitors are preferable because only schottky emission effect dominates the current conduction mechanism at low electric field [50]. Similarly, due to larger bandgap and thermodynamic compatibility to interface with silicon, hafnium oxide (HfO_2) can be used as gate material in reducing ever increasing tunneling current and reliability issues while oxide thickness are scaled down in nano meter regime [51]. Manoj et al. [52] have studied the impact of high-*k* gate dielectric material on FinFET short channel effects and its digital circuit performance. Nevertheless, the short channel effects worsen with increasing dielectric constant of gate dielectrics. Various approaches such as gate work function engineering, fin width scaling and doping adjustment in

fin are studied in order to deduce an optimum dielectric constant value so that an acceptable subthreshold leakage current can be targeted [52].

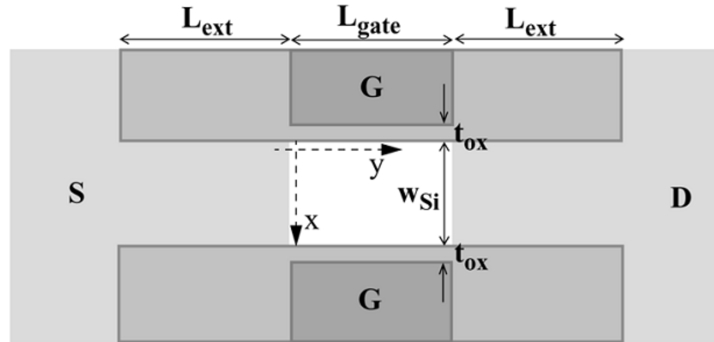

Fig. 1.2. Top cross-sectional view of FinFET [53].

Considerable attention has been paid on underlap FinFET because of its variable gate length in strong and weak inversion [53-54]. As shown in **Fig. 1.2**, the source and drain ends are at considerable distance from the gate edges. This distance is termed as extension length (L_{ext}) of the device. At strong inversion underlap extension portion is fully inverted with high electron concentration providing effective channel length $L_{eff} \approx L_g$. At subthreshold/weak inversion regime of operation, on the other hand, low electron concentration allows the source and drain extension lengths (L_{ext_S}/L_{ext_D}) to add to the actual channel length resulting in effective gate length $L_{eff} \approx L_{ext_S}+L_g+L_{ext_D}$. Therefore, in addition to suppressing short channel effects (SCEs) and reducing off current, it also serves in providing higher on current. Some of the striking features of underlap FinFET are as follows [53-57]:

(a) Increase in effective channel length in off state to control SCE.

(b) High I_{on}/I_{off} ratio.

(c) Reduction of gate edge direct tunnel leakage

(c) Reduction of gate sidewall fringe capacitance

(d) GIDL is reduced due to undoped body

(e) Intrinsically doped channel region avoids random dopant effects and improves carrier mobility

As per aforementioned properties, underlap FinFET operating at subthreshold/weak inversion, has the potential to suppress short channel effects and, in turn, can enhance the performance.

1.2.2 Analog performance:

The analog figures of merit (FOM) such as transconductance (g_m), output conductance (g_{ds}), early voltage ($V_{EA} = I_{ds}/g_{ds}$), transconductance-to-current ratio (g_m/I_{ds}), intrinsic dc gain ($A_{V0} = g_m/g_{ds}$) and cutoff frequency ($f_T = g_m/2\Pi C_{gg}$) are affected by short channel effects and, in turn, depend upon the effectiveness of gate electrostatic integrity (*EI*) over channel region [58-59]. With scaling down of gate length, it is reported that for a fixed gate and drain overdrive voltages, both unity gain cut-off frequency (f_T) and non-quasi-static transition frequency (f_{NQS}) increase monotonically as $1/L^2_{eff}$ [60]. However, aggressive scaling of supply voltages can result in turnaround of both f_{NQS} and f_T beyond 100nm regime. This kind of performance degradation at scaled gate lengths can be attributed to lower mobility at reduced gate overdrive voltages [60].

A halo implanted MOSFET has been reported to enhance the analog FOM of bulk MOSFETs in subthreshold region of operation [61]. The authors further show that adopting dual material single gate structure for conventional MOSFET can enhance the analog FOM too at subthreshold regime of operation of device. 70% improvement in intrinsic voltage gain is observed as compared to the gain of single material based MOSFET [22]. Subsequently, it is shown that single halo dual material double gate (DMDG) MOSFET has superior scalability because of better short channel immunity and improved analog performance [29]. Higher electron mobility and velocity at surface of the device are crucial parameters of DMDG MOSFET that accounts for better performance and noise immunity [30]. The advantage of DMDG structure over channel engineered devices is further studied in detail [31]. FinFET is

emerging as a popular choice because of reduced SCE and superior RF performance. Sengupta et al. [62] have reported that the drive current and peak cut-off frequency of n-FinFET improves with higher implantation energy and reduced channel implantation dose. Subsequently, high frequency noise parameters in FinFETs have been studied and different models are deduced for extraction of minimum noise figure, equivalent noise resistance and optimum source admittance [63].

With an increase in both source and drain extension lengths (L_{ext}) of underlap FinFET the analog FOM are reported to improve further [20-21]. Similarly, a drain extended FinFET has been proposed for high voltage and high speed (or RF) applications. The device shows a better on resistance vs break down voltage tradeoff [64]. More so, downscaling of FinFET is beneficial to analog performance by improving gate electrostatic control although losses due to series parasitic increase [65]. However, quantum mechanical effects are of serious concern in multigate devices when silicon fin thickness is scaled to 5nm or below [66-67]. This would affect both digital and analog performance.

Furthermore, use of high-*k* dielectric in underlap section of FinFET can enhance the fringing field coupling. This effect is known as gate fringe induced barrier lowering (GFIBL) capability of high-*k* spacer that enhances the digital performance at strong inversion regime of operation of device [68]. Increasing L_{ext} length will increase the undoped/low-doped portion of L_{ext} near to gate edge of underlap FinFET. Therefore, restricting high-*k* dielectric to the gate side wall only, can enhance the gate sidewall fringing fields and, in turn, can raise the barrier to conduction at weak/moderate inversion regime of operation. Vega et al. [69-70] has reported that this kind of dual-*k* spacer based underlap FinFET can improve the gate electrostatic integrity ($EI \alpha 1/L_{elec}$) and, in turn, can control direct source to drain tunneling (DSDT) and short channel effects. Virani et al. [71-72] has also analyzed the implications of dual-*k* spacer in improving performance of Tunnel FET with underlap. Subsequently, dual-*k* spacer based

FinFET has the potential to shift the influence of drain potential away from the gate edge toward drain and, in turn, can enhance the analog performance of the device.

1.2.3 Design Issues in Multigate Devices:

Harish et al. [73] have proposed a methodology for modeling the process variation effects on delay performance of digital circuits. The variations in implant dose and energy, processing techniques such as oxidation and high temperature annealing etc. are categorized under extrinsic variations to device. Whereas, variations such as, random dopant fluctuation in channel, gate dielectric thickness and its permittivity, interface and oxide charges etc. are categorized under intrinsic variations of device dimensions. It is reported that this kind of severe process related variations in deep sub-micrometer regime cannot be adequately produced by deterministic circuit design approach. Therefore, it becomes imperative to adopt statistical circuit design approach that can account any number of process related variability issues [73].

Dadgour et al. [74] have modeled the threshold voltage fluctuation effect due to work function variability in emerging devices like FDSOI MOSFET, FinFET etc. The source of variability is identified as defects in grain orientations of metal. TiN and WN materials show lower V_{th} fluctuations. Furthermore, FinFET is less affected by work function variations due to its larger gate area. Nevertheless, few VLSI circuits can show degraded performance and reliability issue due to V_{th} fluctuation [75]. Subsequently, an accurate physical model has been developed that considers the effect of the work function variation for ultra short channel MOSFETs [76]. More so, the model has the advantages of capturing work function variation effects of 3-D device by using 2-D device simulation. This results in a significant lower simulation time as compared to the simulation time of 3-D device. Quantum mechanical effect and width quantization are two important properties that need to be accounted for characterization of FinFET even in subthreshold regime. In addition, work function variation results in quantum mechanical confinement. Therefore, a reliable design framework has to be targeted that considers the width

quantization effect [77-78]. Secondly, sources of variability such as random doping fluctuation in source/drain extension regions, line edge and line width roughness (LER/LWR) etc., need to be studied in detail for characterization and optimization of CMOS in nano-meter regime [79-80]. These studies are crucial considering their effect on threshold voltage and on current of the device [81-83].

Better electrostatic control over channel is of paramount importance for performance improvement at nano-scale regime. Tall and narrow fin formation, oxide thickness reduction and doping profile control are crucial aspects of device design that can target better *EI* [84-86]. However, unique manufacturing challenge while incorporating tall and narrow fins (high aspect ratio), and process induced variations in the fins and oxide thickness are pronounced with shrinking device dimensions [87-93]. Similarly, formation of ultra shallow junction (USJ) for controlling doping profile is governed by defect formation and junction leakage in addition to associated manufacturing challenge and cost effectiveness [94-100]. These important manufacturing factors are causing negative impact on the inter device variability and, in turn, degrade the mismatch parameter in nano-scale devices. Furthermore, the mismatch in critical device attributes can limit the accuracy of digital as well as analog circuits. For comparators and operational amplifiers, the mismatch has serious implications on offsets. For analog to digital converter it can affect the bit accuracy, whereas power supply noise and common mode rejection ratio of differential amplifier are two important parameters that are affected by this mismatch [101]**.** This culminates in designing FinFET with excellent *EI* so that the performance is less immune to parametric variations and inter-device variability considering the aforementioned process challenges.

Low temperature operation of field effect transistors (FETs), on the other hand, have some excellent properties like: improved switching speed due to increase in saturation velocity and carrier mobility, improved reliability, reduced thermal noise, higher packing density, lower

power dissipation etc. [102-106]. Secondly, high transconductance and velocity overshoot effects in NMOS devices are added incentive when the device is cooled to liquid nitrogen temperature [107]. More so, the volume inversion property of multigate device is enhanced at low temperature than at room temperatures results in substantial improvement in mobility of minority carriers [108]. Therefore, further scaling down of device dimensions in low temperature environment is possible because of improved subthreshold slope, lower leakage current, improved gate electrostatic integrity and, in turn, enhanced analog performance [107-114].

1.2.4 Compact Mathematical Model Generation:

Simple compact mathematical models of MOS transistors are needed for high speed computation of device characteristics that can be used in computer-aided circuit simulators in order to design and optimize the performance of integrated circuits containing millions of transistors on single silicon chip [115]. Surface potential model approach of channel region of MOS device is one of the simple, compact and accurate mathematical analysis that is widely accepted by researchers [116-118]. In addition, the equations derived from these surface potential models are continuous in all three operation regions of device. Therefore, the current can be accurately determined using these models which are often needed for VLSI circuit simulation [119-120]. Several authors have proposed analytical models of threshold voltage, DIBL, subthreshold slope and subthreshold current using the surface potential model approach [121-124]. Therefore, this kind of approach is familiar in device characterization of most of the present day MOSFETs starting from bulk MOSFET to FDSOI MOSFET, DG MOSFET, triple gate (TG) MOSFET and gate all around (GAA) MOSFET etc. Furthermore, the mathematical computation is easier while solving wide range of poisson equations governing 2-D, 3-D and cylindrical co-ordinate systems. In addition, inclusion of short channel and narrow width effects are also possible while deducing models for short channel MOSFETs.

For underlap FinFET, on the other hand, the gate fringing field effects in underlap region cannot be captured by adopting the conventional double gate MOSFET model approach. The electric flux continuity expressions of underlap regions will be different, as the effective oxide thickness between gate side wall and Si-SiO_2 interface is not constant due to fringing fields. Conformal mapping technique has been used by Bansal et al. [125] to model the gate fringing field of DG underlap FinFET. As the underlap surfaces are not equipotential surfaces, the fringing field can be solved self-consistently with the surface potential using Poisson equation in order to generate a compact analytical model [125-127]. Subsequently, modelling of threshold voltage of the device can be carried out by equating the electron concentration at minimum potential point in the channel region with the channel doping concentration that satisfies the inversion condition. Using the threshold voltage model, the drain current in linear and saturation region of DG MOSFET can be deduced by following the approach as suggested by Suzuki et al. [128]. In addition, effects like impact ionization and parasitic BJT effects have to be included while modeling conduction current considering high lateral electric filed in saturation region of operation of device [129]. More importantly, the non local effects such as channel length modulation [130], velocity overshoot effect [131] and drain induced barrier lowering (DIBL) [132] are also required to be included in current model as the device dimensions are scaled down to nano-meter regime [133].

Second aspect of model formulation should capture the effect of heavily doped source/drain (S/D) region on channel region of device. Heavily doped S/D region is usually preferred to control the device parasitics in order to avoid performance deterioration [44]. However, when rapid thermal processing step following the high temperature annealing is performed to activate the dopant species of both channel and S/D region, the heavily doped S/D dopant species can easily intrude into the lightly doped channel region. This effect will enhance the lateral spread of S/D electric field and, in turn, will deteriorate short channel effects (SCEs) and performance

of multigate MOSFETs, especially when the device dimensions are scaled into nano-meter regime. Adoption of advanced junction process technologies can target ultra shallow junction (USJ) formation in order to control this ever increasing lateral S/D electric field spread via dopant species and to avoid deterioration in SCE and performance of nano-scaled devices [134]. However, formation of USJs is achieved by additional process complexity and efficient temperature control step in fabrication [94-100]. Therefore, while deriving compact models for nano-scale MOSFET, it is pertinent to include the effect of this lateral S/D profile on channel electrostatics.

1.3 Problem Description:

The proposed work during the period of research addresses the analog performance and variability issues of nano-scale multigate FETs. It is felt that, as the multigate FETs are scaled into nanometer regime, various issues pertaining to the gate electrostatic integrity and, in turn, analog performance are not studied in detail. Effective uses of high-*k* dielectric at underlap section of multigate FETs are not fully explored. To the best of our knowledge, compact analytical modelling of double dielectric spacer based underlap FinFET has not yet been developed. Effect of source and drain lateral gaussian profile on analog performance of multigate FETs is another concern that has not been fully explored. In view of these observations, the whole work during the period of research has been divided primarily into four phases.

I. Analog performance study of double dielectric spacer based underlap FinFET by extensive 'Technology Computer Aided Design' (TCAD) simulations. Optimization of inner high-*k* spacer dimension and addressing subsequent performance improvement related issues.

II. Exploring options to mitigate gate length scaling as well as variability issues at nano-meter regime of device operation.

III. Circuit implementation of the developed optimized devices.

IV. Development of mathematical models to accurately predict the characteristics of multigate FETs and subsequent verification by TCAD simulations.

Initially, the effect of underlap extension length on FinFET analog performance has been studied by extensive TCAD simulations. The study has been extended to dual-*k* spacer based underlap FinFET in order to optimize the inner high-*k* spacer length. Suitable variations in underlap extension length and doping gradient of S/D doping profile are provided to optimize the inner high-*k* spacer length in accordance with analog performance comparison with conventional low-*k* FinFET. In the second phase of the research, we have addressed the design related issues of FinFET at scaled gate lengths. Variations in crucial device dimensions such as, fin height (H_{fin}), fin width (W_{fin}), oxide thickness (T_{ox}) and lateral straggle (σ_L) of S/D doping profile are studied to target the optimum analog FOM and address its variability aspect in terms of performance. The effect of frequently available alternative high-*k* inner spacer material on analog performance of dual-*k* underlap FinFET is studied too. Subsequently, a single stage OTA is designed in third phase of the research, to further address the effect of local variation in crucial device dimensions over circuit performance. More so, low temperature operation of underlap FinFET is explored to maximize the analog FOM that can address the possible scaling issues.

In the fourth phase of the research, a mathematical model has been formulated to accurately predict the behavior of dual-*k* underlap FinFET. The results so obtained have been verified by extensive TCAD simulations. Crucial device attributes such as, gate oxide thickness, inner high-*k* spacer length and its dielectric constant are varied to validate our model under variable

device attributes. To the best of our knowledge, for the first time this kind of model for dual-*k* underlap FinFET has been developed. Secondly, as the lateral gaussian profile of S/D region plays a crucial role in deciding analog FOM of the device, therefore for the first time, we have included this effect while deriving a compact mathematical model of conventional DG MOSFET. The work is further validated by varying crucial device attributes such as lateral straggle of S/D gaussian profile, oxide thickness, channel thickness and gate length of the DG MOSFET. The analytical results have been further verified by extensive TCAD simulations.

1.4 Thesis Organization:

This thesis is organized into 8 chapters as follows:

Chapter 1: Deals with analog performance analysis of multigate FETs, need for dual-*k* spacer formation at underlap section of FinFET, problem definition etc. This chapter also introduces methods to develop compact model in presence of optimized high-*k* inner spacer dielectric. Modelling the effect of lateral source/drain gaussian profile on analog performance is also introduced in this chapter.

Chapter 2: This chapter reviews the state of the art issues regarding analog performance of multigate FETs. Various technical gaps that are identified based on the review are summarized in this chapter. The chapter also provides a detailed review of related works on advantages of introducing inner high-*k* spacer near the gate edge of underlap section of FinFET. Variation aware design and analysis in analog environment is reviewed in detail. In addition, advantages of low temperature operation of underlap FinFET to address the analog performance as well as device scaling issues are also reviewed. Furthermore, the review work is extended to develop a compact analytical model of double dielectric spacer based underlap FinFET and to include the effect of source and drain lateral gaussian profile on analog performance of multigate FETs.

Chapter 3: This chapter deals with the study of the effect of extension length on mobility, electric field and, in turn, analog performance of underlap FinFET. Subsequently, feasibility study of introduction of high-*k* inner spacer dielectric at underlap section is studied and a fabrication step is outlined. Device physics pertaining to the inner high-*k* spacer is explored with variation in its length. Furthermore, this high-*k* spacer length is optimized to develop a suitable ratio between inner and outer spacer length for optimum analog performance.

Chapter 4: This chapter primarily presents design and analysis of underlap FinFET so that the performance is less immune to parametric variations and inter-device variability considering the process challenge issues. Tall and narrow fin formation, oxide thickness reduction and doping profile control are some crucial aspects that are analysed in terms of analog performance of the device. A single stage OTA is designed to further study the effect of local variation in crucial device dimensions over the circuit performance.

Chapter 5: This chapter targets low temperature operation of underlap FinFET. The analog performance of the device is enhanced at low temperature environment because of improved threshold voltage (V_{th}) and carrier mobility at liquid nitrogen range (≥77K). It is observed that, dual-*k* spacer based underlap FinFET improves the analog FOM because of further improvement in mobility and threshold voltage and, in turn, analog FOM as compared to conventional low-*k* FinFET. Secondly, scaling down the gate length of dual-*k* FinFET at 100K temperature range is also studied in detail.

Chapter 6: This chapter deals with development of a compact potential model of dual-*k* underlap FinFET that includes the effect of inner high-*k* spacer (ε_h) on device performance. The S/D underlap portion are divided into two sub-sections so that underlap length $L_{un} = L_h + L_l$, where L_h is the length of the inner high-*k* spacer and L_l is the length of the outer low-*k* spacer. The section defined by L_l is modelled via effective gate height reduction by elliptical field line expressions and taylor series solution to 2D potential equations. Subsequently, the expression

for threshold voltage and drain current model is deduced. Furthermore, the effect of inner high-k spacer over analog figures of merit such as g_m, g_{ds} and A_{V0} is studied.

Chapter 7: This chapter presents a simple, yet effective compact potential model for 2D DGMOSFET that includes the effect of source/drain lateral gussian profile on analog performance of the device. For generating a compact model, the effect of S/D profile is introduced in terms of ionised dopant species, effective S/D ends and effective channel length calculation considering dopant degeneracy effects. Subsequently, the expression of threshold voltage and drain current model is deduced. Furthermore, the effect of σ_L over output conductance (g_{ds}), transconductance (g_m) and intrinsic gain (A_{V0}) is studied.

Chapter 8: Finally, summary of the work with conclusions of the thesis is presented. This chapter ends with the further scope for extending the present work.

Chapter 2

Literature Review

2.1 Introduction:

Improving performance of nano-scale MOSFETs have been studied for several decades in order to address the overwhelming increase in short channel effects and performance deterioration with aggressive scaling of gate lengths into nano-meter regime. Source to drain lateral spread of electric field plays major role in deciding the performance of nano-scale devices. Of particular importance are analog applications where various figures of merit (FOM) of the device, deteriorate with unrestricted spread of this lateral electric field. The estimation of this field spread via various critical transistor attributes, is a mandatory step to get an insight about its impact on device performance and reliability. Nevertheless, controlling this lateral field near the gate edges of the device is a complex task that is continually posing serious challenges to design engineers. With each change in the underlying technology, new effects appear and old designing practice must be revised in order to cope with additional challenges that crop up. Secondly, change in device design technology at scaled gate lengths has profound implications on circuit performance in both digital and analog domain.

For conventional CMOS devices, the gate overlap is indeed a scalable parameter that needs to be scaled properly along with channel length in order to target better performance at circuit level [135]. It is reported that, if this gate overlap is not optimized properly, it will not only hamper the functionality of inverter delay, sample and hold application etc. but also enhance serious hot carrier reliability issue. In addition, as compared to lower overlap length, the circuit performance of higher overlap length based device is very sensitive to process tolerance [135]. Subsequently, Srinivasan et al. [136] have deduced an optimized overlap length in order to target minimum noise figure and maximum gain for low noise amplifier circuit (LNA). A

second device design approach is to extend the source/drain region away from the gate edge, resulting in an underlap region adjacent to gate edge [53]. Increasing this underlap extension length has the capability to suppress source to drain lateral electric field and, in turn, allow the gate electric field to take control of most of this underlap area adjacent to gate edge. This process will improve gate electrostatic integrity, reduce short channel effects and enhance performance of multigate MOSFETs [20-21], [54].

In this chapter, we present an extensive literature review related to various state of the art issues in multigate devices. Various research papers, books and monographs are referred that take care of various aspects such as, underlap FinFET advantages, variability aspect of underlap FinFET in analog domain, scaling issues and modeling of multigate devices in order to understand the timeliness of the work being carried out as well as to understand the various technical gaps in the area of analog device and circuit design. Section 2.2; covers the literature on major scientific developments made in the area of underlap FinFETs. Section 2.3; deals with a survey of efforts made to understand the variations in critical transistor attributes and its effect on device and circuit performance, Section 2.4; describes the review of low temperature advantages of multigate devices in analog domain, Section 2.5; enumerates the research done to develop analytical models for predicting characteristics of underlap FinFET. The literature survey through various research papers for developing compact analytical model that can include the effect of source/drain lateral doping spread into the channel region has been presented in Section 2.6. Finally the chapter concludes with Section 2.7 which enumerates various technical gaps identified based on the literature survey.

2.2 Survey of Underlap FinFETs:

This section covers literature survey regarding advantages of underlap FinFET that can suppress short channel effects and enhance digital/analog performance of the device. Major issues such as, metal gate advantage, problems in use of high-*k* material as gate dielectric,

leakage phenomenon, dual-k spacer formation in underlap section of FinFET and its advantage in improving performance of the device are highlighted.

Special attention has been paid in designing underlap FinFET in recent years, where an underlap extension length (L_{ext}) is defined between gate and source/drain of FinFET [53]. With increase in underlap extension length, the source to drain lateral electric field is suppressed and most of the area adjacent to gate edge comes under direct control of gate. Subsequently, the effective underlap section helps in providing a bias-dependent longer effective channel length (L_{eff}) at subthreshold and weak inversion regime of device operation. Therefore, significant relaxation in fin-thickness requirement for controlling short-channel effects (SCEs) can be addressed. Fossum et al. [54] have reported that, gate to source bias (V_{GS}) modulates the electric potential (φ) and electron density (n) in these undoped underlap regions. This kind of modulation is a consequence of gate-induced electrons moving into the extension regions and modification of the source to drain lateral electric field that affect a perturbed drift-diffusion detailed balance in the direction of channel current. Consequently, L_{eff} is longer in weak inversion whereas it approaches the physical gate length in strong inversion. The long $L_{eff(weak)}$ tends to suppress SCEs and limit off state current (I_{off}), and the short $L_{eff(strong)}$ can yield high on state current (I_{on}).

High-k gate dielectric materials are preferred in device design to reduce the ever increasing gate tunneling leakage (I_g) while the device dimensions are scaled down into nano-meter regime [137-139]. Secondly, the high-k gate dielectric is beneficial in expanding design space due to possible use of thicker dielectric. However, when the dimension of thick gate dielectric becomes comparable to the gate length of underlap FinFET, there would be increased fringing fields from gate to source/drain regions, thereby the electric fields from source/drain to channel is enhanced. As a consequence, the gate control over the channel region is degraded and the short-channel performance is worsened [52], [139]. Chen et al. [140] have termed this effect as

fringe induced barrier lowering (FIBL). FIBL is fast becoming a major concern while trading off the thickness of high-*k* gate dielectric with SCE. Its effect worsens SCEs, enhances I_{off} and introduces threshold voltage (V_{th}) roll–off because of loss of gate electrostatic control over the channel region. More so, Dutta et al. [141] have reported that, use of high-*k* gate dielectric will result in degradation of I_{on} and transconductance of the device, because of degradation in mobility at the high-*k*/Si interface. Increasing the gate thickness (T_G), the electric field coupling between the gate terminal and underlap extension region increases. This effect lowers the barrier in the source underlap extension region and, in turn, more carriers from source side are allowed to enter into the channel region which subsequently increases the on current (I_{on}) of the device. The phenomenon is known as gate fringe induced barrier lowering (GFIBL) and is restricted to the undoped underlap regions [68]. Use of high-*k* spacer dielectric in underlap region will further enhance GFIBL effect. I_{on} increase is similar to what reported by Chang et al. [142] in case of bulk MOSFETs. Unlike FIBL, GIFBL does not degrade threshold voltage, subthreshold slope and I_{off} as GIFBL is restricted to undoped underlap region.

Poly-silicon depletion effects, boron penetration effects and incompatibility of polysilicon with high-*k* gate dielectric materials are few severe limitations that make the use of polysilicon gates difficult in nanoscale regime. Use of metal gates, can avoid these problems effectively. Additionally, low resistance and tunable work function of metal compounds are some attractive properties of metal gate for its use as alternative gate material. This kind of work function tuning is a better technique for threshold voltage setting of device rather than modifying the channel doping [143-144]. Therefore, the combination of undoped body and metal gate with work function close to midgap is an attractive option in scaling the multigate devices down to 10nm to meet ITRS targeted requirements.

Poiroux et al. [38] have reported that, scaling the gate length of underlap FinFET will have similar effect as reported by bulk devices. Oxide thickness scaling will improve SCEs,

transconductance and I_{on} / I_{off} due to better gate electrostatic control. This will increase the leakage current too [145]. Scaling fin thickness will reduce I_{on} because of reduction in number of carriers in a thinner fin. Secondly, the structural quantum confinement in the thin fin causes the minimum energy of electrons in the potential well to rise to non-zero values as the silicon fin becomes thinner. This effectively increases the threshold voltage (V_{th}) of the device as carriers must now populate a higher energy subband [38], [145]. Quan et al. [146] have reported that image force at oxide silicon interface will induce a positive charge on the interface which acts like an image charge within the layer. This effect leads to a reduction of the barrier height for both electrons and holes. Subsequently, the gate leakage will increase.

With scaling down of technology into nano-meter regime, the effective gate capacitance lowers, resulting in better performance and reduced power consumption in a circuit. In sub-100nm technologies, however, the gate capacitance reduction is not significant as it was predicted by ITRS [3]. This is because, the parasitic fringe capacitance starts dominating the effective gate capacitance with technology scaling which hardly reduce as effectively as the oxide capacitance scales with technology [147]. In the absence of overlap capacitance, these fringe capacitances are more dominant in underlap FinFET. Therefore, the FIBL effect is more pronounced in underlap FinFET [52], [68]. The fringe capacitances consist two parts, inner and outer. Agrawal et al. [148] have reported that at weak inversion both inner and outer fringe capacitance will be present. In strong inversion, on the other hand, the inner fringe capacitance (C_{if}) is shielded by channel, because lateral direction electric field contributing to C_{if} is screened out by free carriers in the body. Therefore, only outer fringe capacitance C_{of} is required to be modeled [148]. At weak inversion C_{if} directly depends upon the effective underlap defined by the lateral source/drain doping whereas, C_{of} depends on the length of the gate underlap region and hence indirectly on effective underlap. These two weak capacitances can be modeled by applying gauss law and poisson equation at the underlap region [148-150]. At strong inversion C_{of} is

calculated using conformal mapping techniques where, the arc shaped electric field lines are mapped into an equivalent parallel plate system [57].

Secondly, Quan et al. [146] have reported that, with scaling down of oxide thickness, the quantum effects on the silicon body capacitance (C_{Si}) cannot be neglected. This is mainly because of the quantum nature of two-dimensional electrons in the inversion layer, which has major contribution to C_{Si} in strong inversion [146]. The C_{Si} results from the depletion charge (Q_{DEP}) and induced electron charge (Q_{INV}). The inversion charge consists of two dimensional (2D) electrons induced in the subbands. In the strong inversion region, the contribution from the induced electron charges dominate C_{Si} and more than 90% of the induced electrons fall into first subband [151]. The first subband (FSB) approximation of Q_{INV} holds good because it greatly simplifies the mathematics with practically no errors incurred [152]. In depletion region of device, less than 90% of the induced charges reside in first subband. Nevertheless, the amount of induced electron charge is much lower than the depletion charge, so that its effect on C_{Si} is completely masked by the depletion charge [151-152].

Increase in underlap extension length (L_{ext}) improves gate controllability with reduced SCEs because of shift in lateral electric field from gate edge toward drain. Therefore, analog figures of merit such as transconductance (g_m), output conductance (g_{ds}), transconductance-to-current ratio (g_m / I_{ds}), early voltage ($V_{EA} = I_{ds} / g_{ds}$), intrinsic dc gain ($A_{V0} = g_m / g_{ds}$) and unite gain cutoff frequency ($f_T = g_m / 2\Pi C_{gg}$) is reported to improve [20-21]. Reduction of g_{ds} is due to of reduced dopant concentration at gate edge with increase in underlap extension length, whereas reduction in C_{gg} is due to increase in distance between gate and drain/source electrodes which makes the fringing fields difficult to screen out. Increase in g_m can be attributed to high increase in electron mobility (μ_n) as $g_m \alpha \mu_n$. This is because of so called volume inversion effect in narrow fin multigate SOI MOSFETs [24]. Volume inversion carriers experience lesser scattering at Si-SiO_2 interface than the carriers present in surface inversion layer. As a result

considerable increase in mobility and, in turn, transconductance is observed in multigate devices at low gate biases [153]. This effect is pronounced with increase in underlap extension lengths because of lesser influence of drain potential on the channel.

Raskin et al. [154] have shown that, at low gate overdrive, the charge carriers are well spread out across the thin silicon film indicating presence of VI regime. There will be equal amount of charge concentrations present at the surface as well as at the center of the film, which is considerably higher than the channel doping. As the overdrive increases, the charge carriers at the Si-SiO_2 surface will screen out the carriers present at the center of the silicon film. This, in turn, results in linear increase in the potential at the fin surface following the gate overdrive whereas the potential at the center of the film almost saturates and cannot follow the overdrive. This kind of potential imbalance can enhance the rate of increase in electron concentration at the surface of the film as compared to the concentration at the center of the film. Therefore, although there will be higher mobility at the center of the film due to reduced effect of vertical electric field, the surface charge carriers will dominate the current conduction at higher gate overdrive. Subsequently, the dominant current flow is due to the carriers located at the center of the film attributed to weak inversion regime of operation of device due to lower gate overdrive. In strong inversion region, on the other hand, the current conduction mechanism is shifted to the surface of the film. In terms of analog perspective, low gate overdrive is termed as VI regime with high g_m for multiple-gate devices. As the overdrive increases, the VI regime becomes less effective because of increasing carrier concentration at the Si-SiO_2 interface which promotes a screening effect on the carrier concentrated at the center of the film. Subsequently, reduction in the charge concentration at the center of the silicon film results in reduced current drive and, in turn, lowers transconductance of the device [153-154].

Gate fringe induced barrier lowering (GFIBL) is enhanced in undoped underlap FinFETs with increase in dielectric constant of spacer region (L_{ext}) as discussed by Sachid et al. [68]. The

barrier to lateral drain electric field is lowered in strong inversion because of increase in coupling of gate fringing fields to undoped underlap portion of FinFET resulting in higher on current (I_{on}). Consequently, higher I_{on}/C_{gg} ratio can be obtained with increase in spacer dielectric constant, thereby reducing the propagation delay of digital circuits. With increase in doping gradient of N_{sd} doping profile, the lateral drain field intrudes into the channel and reduces the effect of gate fringing fields near the gate edges. Therefore, I_{on}/C_{gg} ratio cannot be improved with increase in spacer dielectric constant when sufficient undoped underlap portion is not present in the device. This envisages that restricting the high-*k* dielectric to undoped/low-doped underlap portion ($L_{sp,hk}$) can strengthen the gate sidewall fringing fields. These fringing fields are virtually normal to the underlap region; therefore, the lateral electric fields from drain to source can be shifted away from gate edge toward drain by strengthening these fringing fields [155].

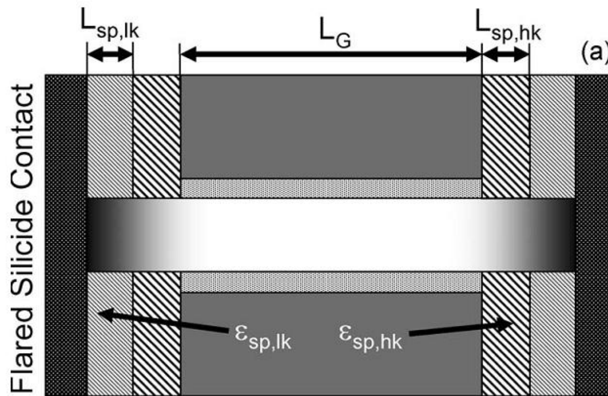

Fig. 2.1. Cross section of dual-*k* spacer based dopant segregated schottky (DSS) MOSFET [69].

Increasing length of L_{ext} will increase the undoped/low-doped portion of L_{ext} near to gate edge of underlap FinFET. Restricting, high-*k* dielectric to the gate side wall can enhance the gate sidewall fringing fields in this low-doped/undoped area which, in turn, can raise the energy barrier at weak/moderate inversion regime of operation. This kind of barrier modulation capability of gate fringing fields can increase the electrical length (L_{elec}) by depleting the silicon region beyond gate edge of the device [69-70]. Subsequently, it will improve the gate

electrostatic integrity ($EI \alpha 1/L_{elec}$) and short channel immunity of the device [69], [156]. Increasing spacer length of inner high-*k* spacer can improve the short channel immunity further. **Fig. 2.1** shows a dual-*k* spacer based dopant segregated schottky MOSFET where, $L_{sp,hk}$ is length of inner high-*k* spacer and $L_{sp,lk}$ is length of outer low-*k* spacer [69].

The improvement in gate electrostatic integrity can improve transconductance (g_m), output conductance (g_{ds}), early voltage ($V_{EA} = I_{ds}/g_{ds}$) and transconductance-to-current ratio (g_m /I_{ds}) of the device. Transconductance-to-current ratio (g_m /I_{ds}) is a measure of transconductance generation efficiency of the device. Silveira et al. [157] have demonstrated that, g_m /I_{ds} is a better criterion to assess device performance as it expresses the capability of FinFET to amplify a signal under certain dissipated power (I_{ds}). Kranti et al. [153] have reported that, multigate device exhibit higher values of g_m /I_{ds} due to improved charge control resulting from enhanced coupling between its multiple gates. This fact is attributed to absence of body effect in multigate device as compared to its single gate counterpart.

2.3 Process Parameter Related Design Issues:

Tall and narrow fins are typically required for high drive current, better SCE immunity and matching the current drivability [158]. Secondly, taller fins can improve f_T and f_{max} of multi-fin devices when the same channel width of the device is distributed over less number of taller fins as compared to the distribution over larger number of shorter ones [85]. Kilchytska et al. [86] have investigated the effect of fin width on analog performance of 50nm gate length FinFET. It is reported that, both digital and analog performance are degraded at higher fin width because of partially depleted fins. However, when the fin width is scaled down to narrowest possible value, the device enters into fully depletion regime of operation. Subsequently, super high value of early voltage and, in turn, intrinsic gain is reported in these devices due to suspected presence of volume inversion [86]. More so, Parvais et al. [84] have discussed few additional advantages of FinFETs designed using ultra thin body. The need of channel doping can be

eliminated in ultra thin devices which, in turn, will (1) reduce parametric spread due to doping fluctuations and (2) reduce junction leakage currents due to high electric fields (3) lower coulomb scattering resulting in higher mobility. Secondly, higher gate electrostatic integrity will lead to lesser threshold voltage mismatch, higher transconductance and voltage gain [84]. On the other hand, thicker fin width or oxide thickness will reduce the *EI* factor and degrade the analog FOM and aggravate SCE [89], [159]. Most importantly, the demand of ultra shallow junction (USJ) formation is fast becoming a crucial requirement for nano-scale MOSFET in order to control the lateral electric field spread into the channel region [134].

Therefore, tall and narrow fin formation, oxide thickness reduction and doping profile control are crucial aspects of performance improvement at nano-scale regime due to of resulting excellent electrostatic control over channel [84-86]. From industrial point of view, high aspect ratio (AR = Fin height / Fin width) fins are typically preferred because of reduced manufacturing cost resulting from smaller substrate area requirements. However, the requirement of this kind of tall and narrow fin presents unique challenges at manufacturing environment [91]. Various mechanical stresses a typical narrow fin encounters during manufacturing process are (1) inertial forces during substrate movement (2) fluid forces during cleaning steps. The fin can fracture and, in turn, the transistor can become in-operative with increase in these forces on the narrow fin. Secondly, manufacturing of high aspect ratio (*AR*) fins are susceptible to fracture because their relatively narrow base will be exposed to their heavier height induced internal stresses in addition to the forces due to substrate movement and cleaning steps [91], [93]. Subramanian et al. [92] have pointed out that narrow fins do suffer from surface roughness and series resistance related problems. This, in turn, can result in higher noise and mismatch parameters. The series resistance of narrow fin device increases drastically due to current crowding effect that can reduce the drive current and transconductance as a result. In addition, process induced variations in the fins and oxide thickness become more prominent with shrinking device dimensions causing negative impact on the inter device

variability and, in turn, degrading the mismatch parameter [87-92].

Secondly, due to line edge roughness (LER), where random variations along the channel width direction is considerably higher, the short channel immunity and performance of the device can be degraded in addition to enhanced device to device variability [88], [90], [92]. Linton et al. [88] have shown that, the effect of LER is enhanced at shorter gate length resulting in pronounced increase in off current and random variations in device current across a single die. Asenov et al. [87] have studied the LER effect using a fourier synthesis technique and demonstrated that, LER can deteriorate I_{on}/I_{off} ratio and dominate the fluctuation mechanism at shorter gate lengths. Therefore, stringent control of critical dimension and improved gate line edge quality must be challenged simultaneously to meet ITRS requirement [90].

Similarly, oxide thickness variation (OTV) becomes important when the device dimensions become comparable to correlation length of Si-SiO_2 and gate-SiO_2 interface. Asenov et al. [87] have introduced a gussian co-relation function accounting for this fluctuation in T_{ox}. Fluctuation in threshold voltage is observed due to oxide thickness variation resulting from the interface roughness. More importantly, this V_{th} fluctuation is comparable to the V_{th} fluctuation due to random discrete dopants. Evidently, fluctuation along the structure is more pronounced at smaller oxide thickness. Xiong et al. [159] have studied the sensitivity of 20nm double gate and FinFET device due to crucial process parameter variations such as, channel thickness, oxide thickness, gate length etc. Device performance in terms of on current, off current, threshold voltage and SCEs etc. are reported to fluctuate with the device electrical parameters. Moreover, these variations are pronounced as the feature sizes approach the size of atoms or the usable light wavelength required for patterning lithography masks [159]. Therefore, variations in these critical transistor attributes are becoming major threats in transistor design. Drennan et al. [89] have highlighted most of the physical basis for mismatch. It is reported that, accurate mismatch modeling based on physical process parameters are required to calculate parametric yield loss

over design. Subsequently, the study reveals that, analog circuits are of particular importance, where the device level performance variations can substantially alter the specification of the particular circuit from its desired value [89]. In a 3D-TCAD simulation study, Laxmi et al. [160] have reported that the cutoff frequency (f_T) of FinFET is more sensitive to gate length, underlap extension length, gate dielectric thickness, doping of source/drain pads and corner radius. Sachid et al. [161] have shown that variations in gate length, gate dielectric and channel thickness posses serious threat to SRAM cells. An undoped high-*k* spacer based underlap FinFET has been proposed to address the process variation issues of sub-20nm FinFET.

Second aspect of design consideration is controlling doping profile. These day designers are aiming for ultra shallow junction (USJ) formation in order to control the lateral electric field spread into the channel region [134]. However, formation of USJ is governed by defect formation and junction leakage, temperature control, equipment maturity, process control, cost effectiveness etc. [94-100]. More so, USJ formation is even more difficult in case of P-FinFET because of annealed limited transient enhanced diffusion (TED) in boron [94-98]. This culminates in designing FinFET with excellent *EI* so that the performance is less immune to parametric variations and inter-device variability considering the aforementioned process challenges.

Precision analog circuit design is possible by thoroughly understanding the matching behavior of independent devices available in any given technology. Shyu et al. [162] have derived an explicit formula for random errors that affect MOS capacitance and current ratios. The random error differs from device to device in MOS integrated circuit, and therefore it is almost impossible to correct it completely by matching techniques. Four random error effects due to local and global variations in different MOS transistor attributes are considered. These are (1) Random edge effect attributed to variations in ideally straight edges of MOS capacitor (2) Random surface charge effect due to surface as well as ion implanted charges (3) Random

oxide effect due to fluctuations in oxide thickness and permittivity (4) Random mobility effect due to impurity and lattice scattering mechanisms [162]. These variations will affect threshold voltage, gain factor and drain current of the device. More importantly, it is pointed out that, all local random variation effects can be minimized by adopting larger device size.

Lakshmikumar et al. [163] have provided a comprehensive understanding of various causes of mismatch in large and small geometry based p/n-channel devices. An analytical model is developed that relate crucial electrical parameter mismatch to variations in device dimensions. The drain current matching is found to be depended upon both device dimension and operating point. Subsequently, the study focuses local variations or mismatch behavior of drain current in adjacent devices. Threshold voltage (V_{th}) and transconductance factor ($K = \mu C_{ox}(W/L)$) are reported as two crucial parameters that affect the drain current matching [163]. Subsequently, it is concluded that mismatch in V_{th} can be due to variations in different charge quantities, whereas, mismatch in K can be attributed to variations in device dimensions, mobility in channel and gate oxide capacitance per unit area resulting from oxide thickness and permittivity fluctuations. Kinget et al. [101] have pointed out that, the impact of V_{th} mismatch is a dominant term in deciding performance accuracy of CMOS. In addition, between thermal noise and transistor mismatch, the effect of later term on the power consumption is most important while designing high speed and accurate analog building blocks. Subsequently, this problem of low voltage and mismatch study has been extended to analog low power design of switched opamp circuit which is a possible alternative to switched capacitor circuit that is fast becoming in-operative at low power environment [164]. Kinget has demonstrated a fixed bandwidth-accuracy-power tradeoff imposed by minimal device area requirements for improved inter device matching while designing accurate analog circuits such as, current mirror and operational transconductance amplifier [165].

Therefore, it is imperative to study the impact of local variations in threshold voltage (V_{th}) and

mobility (μ), with crucial process induced variations like, T_{ox} and X_j, that are two important aspect of analog circuit design at smaller processing nodes [162-163]. Secondly, the circuit level variations will be pronounced at smaller technology node, if the variations in V_{th} and μ are not controlled at device level [101], [164-166].

2.4 Low Temperature Operation and Scaling Issue:

Infrared detectors, space applications, medical diagnostics, satellite communications, terrestrial applications, cryogenic instrumentation and superconductive magnetic energy storage systems are few application areas of low temperature electronics [109], [167-168]. Due to reduced current gain, it is not feasible for bipolar transistors to operate at low temperatures [106]. Field effect transistors (FETs), on the other hand, have some excellent properties while operating at low temperature environment. These are: improved switching speed due to increase in saturation velocity and carrier mobility, improved reliability, reduced thermal noise, higher packing density, lower power dissipation etc. [102-106]. Sai-Halasz et al. [107] have reported high transconductance and velocity overshoot effects, when 0.1μm gate length fabricated NMOS devices are cooled to liquid nitrogen temperature.

Subsequently, volume inversion MOS transistors have been reported on the basis of confinement of minority carriers at the center of the channel rather than at Si-SiO_2 interface [24]. The advantages of volume inversion are (i) Higher current due to great increase in number of minority carriers (ii) Reduction in surface scattering and interface defects (iii) Higher carrier mobility due to use of thick volume inversion as compared to narrow surface inversion and (iv) Enhanced effective mobility and, in turn, higher transconductance [24]. These special features will enhance current drive, transconductance, subthreshold slope and speed of the device. Ge et al. [110] have extended this analysis to double gate MOSFETs. It is reported that, carrier mobility of symmetrical DG MOSFET is most enhanced under moderate volume inversion. For intra-subband scattering, reduced ground state form factor is main reason behind this mobility

enhancement. The mobility is also enhanced at strong inversion for an optimal channel thickness (t_{si}). However, for very thin t_{si}, the enhancement tends to be restricted by surface scattering resulting from strong structural confinement [110]. Nevertheless, volume inversion and subband splitting are two main factors for mobility increase in optimally designed DG MOSFETs due to lesser structural confinement [24], [110]. Gamiz et al. [108] have studied volume inversion effect in DG SOI MOSFET at low temperature environment. It is reported that, for 5nm $< t_{si} <$ 20nm, the volume inversion mobility of minority carriers are improved substantially at low temperatures than at room temperature. Quantitatively, volume inversion mobility higher than 1700 cm^2/V.s has been predicted to occur when temperature of thin film DG SOI MOSFET is lowered to 25K [108]. Secondly, reduced electric field in thin-fin devices also contributes to high mobility values. Similar mobility enhancement has been reported in thin film trigate SOI MOSFETs [111]. Subsequently, Colinge et al. [112] have reported that the average surface mobility of trigate SOI MOSFET improves almost linearly as the temperature is lowered from 400K to 100K. Below 100K, on the other hand, the average surface mobility improvement is restricted. This is attributed to the fact that, for temperatures above 100K, the mobility is largely limited by phonon scattering whereas below 100K it is limited by surface scattering [112]. Furthermore, the subthreshold slope improves linearly in the temperature range of 400K to 100K.

Liquid nitrogen can be used as a cryogenic coolant to lower the temperature up to 77K so that low temperature environment for electronic circuits can be targeted. Yu et al. [169] have fabricated CMOS transistors with scaled gate lengths up to 45nm. Negligible impact on SCEs such as DIBL, V_{th} roll-off in addition to lower subthreshold leakage, enhanced threshold voltage and carrier mobility are reported due to cooled operation. Reduction in subthreshold leakage of short channel device can be attributed to decrease in number of carriers with enough energy for impact ionization, whereas latchup free operation is possible because of reduced bipolar gain at lower temperatures resulting in enhanced performance at compact low power

environment [169]. Elbuluk et al. [168] have discussed that, operating at low temperatures, the majority carrier devices can show low leakage current and minimal latch-up susceptibility in addition to improved carrier mobility and saturation velocity leading to high speed circuit designs [113], [170-171]. More importantly, because of improved subthreshold slope, lower leakage current and improved gate electrostatic integrity, further scaling down of device dimensions can become a reality in low temperature environment [109], [112]. Secondly, because of improved threshold voltage (V_{th}), carrier mobility and enhanced velocity overshoot effect, the analog performance of the device can be enhanced at liquid nitrogen temperature environment (≥77K) [107-114].

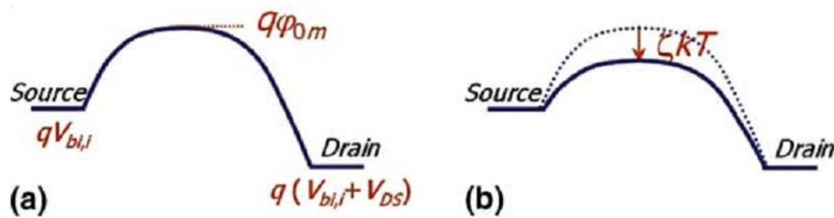

Fig. 2.2. Conduction band energy along the channel of the device (a) with low gate dielectric material (b) with high gate dielectric material of same EOT. Fringe induced barrier lowering effect (FIBL) is denoted in (b) by ζkT amount [140].

It is a standard practice to introduce thick and high dielectric constant (high-*k*) based gate dielectric material in MOSFET technology in order to alleviate the ever increasing tunneling current while scaling down the device dimensions in sub 100nm regime. However, recent studies have shown that, use of this kind of thicker high-*k* gate dielectric material can exacerbate short channel effects (SCE) in double gate and multigate structures [140], [172]. This is because due to thicker gate dielectric, the gate electrostatic control over the channel region will be reduced when same equivalent oxide thickness (EOT) is considered. **Fig. 2.2** shows this kind of fringe induced barrier lowering effect where the conduction band energy is

lowered by an amount of ζkT due to use of thick high-*k* gate dielectric that weaken the gate control over the channel of device [140]. The parameter ζ depends upon device geometry and dielectric constant of gate material. Lowering of potential barrier will enhance the propagation of source to drain (S/D) lateral electric field and, in turn, allow unopposed flow of charge carrier in channel direction which would have been otherwise controlled by the vertical gate electric field. Subsequently, there will be deterioration in threshold voltage, leakage current and performance of the device.

Lowering the temperature of operation can be a solution to restore the loss of gate electrostatic integrity (*EI*) because of decrease in number of carriers will raise the conduction band energy [169]. Nevertheless, as the dielectric constant of gate material increases, lowering the operating temperature hardly helps in controlling the ever-increasing lateral electric field when the gate length is scaled down to 16nm and beyond, posing serious threat for analog applications. In this regard, dual-*k* spacer based underlap FinFET is emerging as a strong contender to multigate devices. This is because of better screening of virtually normal fringing field via inner high-*k* spacer can control the lateral S/D electric field spread into the channel region, thereby improving the gate electrostatic integrity. Subsequently, direct source to drain tunneling (DSDT) and short channel effects can be controlled and digital/analog performance can be improved [21] [69-70]. The effective screening of dominant fringing field can be enhanced with gate length scaling and increasing the dielectric constant of inner high-*k* spacer. This would result in improved threshold voltage and channel carrier mobility. With scaling down the operating temperature of dual-*k* FinFET, there will be pronounced increase in threshold voltage and channel carrier mobility and, in turn, greater percentage improvement in analog FOM.

2.5 Analytical Modeling:

Accurately predicting the behavior of fabricated devices using device models and simulators saves time and money. As a result, modeling is an ongoing topic of research for many engineers

and device physicists. Simple analytical models of MOS transistors are needed for computer-aided design of several integrated circuits containing millions of transistors on single silicon chip [115]. The purpose of modeling is to derive fast, accurate and simple mathematical representation of various electrical characteristics of the device. DC characteristics, switching characteristics, small signal characteristics etc. are part of these terminal properties of the device that are addressed via analytical expressions. These analytical models are required to compute the device characteristics, at enough speed, for its use in circuit simulators in order to design and optimize the performance of integrated circuits containing millions of similar and/or dissimilar transistors. These analytical models define the terminal behavior of the device in terms of capacitance-voltage (C-V) and current-voltage (I-V) characteristics in addition to their carrier transport process happening within the device [118]. More so, these models describe the behavior of device in all operation regions.

Surface potential model often referred as charge sheet model is one of the simple and compact mathematical model widely used by researchers [116-117]. More importantly, the equations derived from these models are continuous in all three operation regions of device. Therefore, the current can be accurately determined using these models which are often needed for VLSI circuit simulation [119-120]. Baishya et al. [122] have presented an analytical subthreshold potential model that includes variations in channel depletion depth and source/drain depletion layers which are few crucial parameters of short channel MOSFETs. The model is further extended to evaluate subthreshold current of MOSFET [122]. Katti et al. [121] have developed a threshold voltage expression for fully depleted silicon-on-insulator (FDSOI) MOSFET by solving three dimensional (3-D) poisson’s equation in channel region. Variable separation technique with appropriate boundary conditions has been used to solve this kind of 3-D poisson’s equation. Short channel and narrow width effects are also accounted for in the model [121]. The analytical model is further extended to deduce threshold voltage and subthreshold

current models of FinFET [123], subthreshold slope and subthreshold current models of asymmetric three terminal and four terminal DG MOSFETs [124].

Similar surface potential modeling can be adopted to model the underlap FinFET behavior. However, Bansal et al. [125] have described that, the gate fringing field effects in underlap region cannot be captured by the conventional double gate MOSFET model approach because of different potential distribution function in overlap and underlap regions [125]. The underlap surfaces are not equipotential surfaces, therefore, the fringing fields need to be solved self-consistently with the surface potential using poisson equation. Secondly, Young et al. [173] have pointed out that, subthreshold potential modeling can be carried out without the mobile charge term in poisson equation for determining subthreshold behavior, such as threshold voltage and subthreshold slope with minimum computation. Subsequently, parabolic potential distribution along vertical direction can be adopted for developing the model [173-176]. After obtaining the parabolic potential distribution function, the poisson equation is solved to obtain the front surface potential in silicon channel. However, the electric flux continuity expressions of underlap regions will be different as the effective oxide thickness between gate side wall and Si-SiO_2 interface is not same due to of fringing fields.

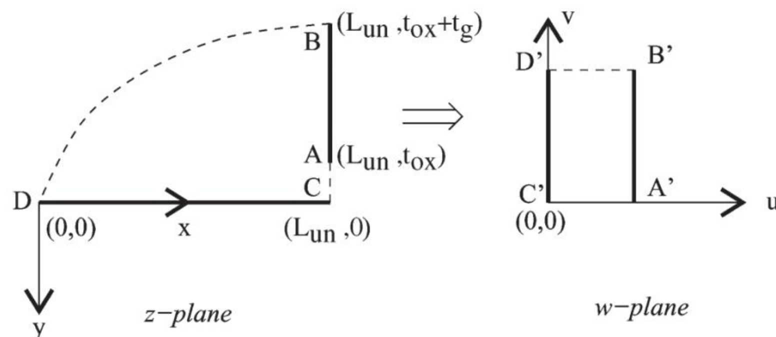

Fig. 2.3. Conformal mapping technique. The left gate edge AB and Si-SiO_2 interface CD of *z*-plane is converted to AB' and CD' in *w*-plane [125].

Kuo et al. [126] have provided guidelines of conformal mapping techniques of gate misaligned DG MOSFET. Same conformal mapping technique has been extended by Bansal et al. [125] to model the gate fringing field of DG underlap FinFET as shown in **Fig. 2.3**. Subsequently, the fringing field can be solved self-consistently with the surface potential using poisson equation excluding the mobile charge term, in order to generate a compact analytical model [125-127]. Nevertheless, the available analytical model of underlap DG device cannot be directly applied to dual-*k* spacer based underlap device [125], [127] because of change in electric field line path between two different dielectric interfaces (ε_h-ε_l) of underlap section. The continuity equations governing two different dielectric materials have been described by Hyat et al. [177]. Therefore, Modeling of electric field lines in underlap section can be carried out by considering the continuity of electric flux at the ε_h-ε_l interface. The poisson's equations in Si-SiO_2 interface can be deduced using the derived flux density expressions, continuity equations and parabolic potential expressions in channel region. The solution to the poisson's equation with appropriate boundary conditions in different region will result in potential expression of DG underlap FinFET.

Modeling threshold voltage of the device can be carried out by finding the electron concentration at minimum potential point in the channel region and equating the same with the channel doping concentration that satisfies the inversion condition. Rao et al. [178] have derived an analytical threshold voltage model for dual metal single gate fully depleted silicon-on-insulator (FDSOI) MOSFET. Variable separation method with appropriate boundary conditions has been used to deduce the threshold voltage for various non-uniform channel doping profiles. Subsequently, the model has been extended to study the effect of random dopant fluctuations in silicon channel [179]. Suzuki et al. [128] have reported drain current expressions of both linear and saturation region of DG MOSFET that is deduced using the threshold voltage model. Similar approach can be followed to model the drain currents of DG underlap FinFET. The double gate structure is a parallel combination of two transistors.

Secondly, channel mobility suffers from both surface roughness and phonon scattering. Therefore, Matthiessen's rule can be adopted to compute effective mobility resulting from these two factors [128].

Impact ionization and parasitic BJT effects have large contribution towards current conduction of the device in saturation region when electric field is normally much larger [129]. Drifting of electrons at oxide-silicon interface in inversion layer will have significant channel current. When drain electric field is much higher, these drifting electrons will collide with lattice and generate electron hole pairs. Due to presence of lateral electric field, the electrons will move toward drain terminal whereas, holes will move toward source terminal of the device. This results in the impact ionization current. Parasitic BJT effects will be pronounced for short channel SOI MOSFET when drain acts as a collector and source acts as a source, allowing a large portion of the impact ionisation current flowing through the source terminal. The thin film acts as a reservoir of holes leading to activation of a parasitic bipolar transistor. As soon as the bipolar device is activated, there will be recombination of electrons and holes at the base region of device. As the vertical electric field of the bipolar device is higher, there will be a collector current component mainly due to of electrons. These electrons will further collide with the lattice, consequently generating electron hole pair [129]. This envisage in three crucial current components: impact ionisation current, channel current and collector current of bipolar transistor that results from impact ionisation and parasitic BJT effects. These effects will not be present before onset of saturation. Therefore, modeling of linear region is straight forward without impact ionisation and parasitic BJT effects.

As the device dimensions are scaled down to nano-meter regime, the non local effects become more prominent in deciding transistor currents. Channel length modulation [130], velocity overshoot effect [131] and drain induced barrier lowering (DIBL) [132] are few of these non local effects that cannot be overlooked [133]. Velocity overshoot is one of the most crucial

issues since it has large impact on drive current and transconductance of the device [107], [180-182]. This effect arises from the fact that, the electron velocity can overshoots from its saturation value for a time period shorter than its energy relaxation time. Increasing longitudinal electric filed will empower the electron gas to be in non-equilibrium with its lattice. These non-equilibrium electrons can now be accelerated to a higher velocity from its saturation value for channel lengths below 150nm [133]. Therefore, while modeling linear and saturation drain currents, these non-local effects such as channel length modulation, velocity overshoot and DIBL are required to be introduced in the models.

2.6 Mathematical Modeling Considering S/D Lateral Gaussian Profile:

Due to close proximity of multiple gates, gate electrostatic control of multigate MOSFET is much better as compared to single gate MOSFET. This results in better threshold voltage control without conventional method of heavy channel doping. However, source/drain (S/D) region of the device is usually heavily doped to control the device parasitics so that the performance is not deteriorated [44]. With lightly doped channel, the dopant species from heavily doped S/D region can easily intrude into the channel region when rapid thermal processing step following the high temperature annealing is performed to activate the dopant species. This kind of dopant spread into the channel region deteriorates short channel effects (SCEs) and performance of multigate MOSFETs, when the device dimensions are scaled into nano-meter regime. ITRS predicts adoption of advanced junction process technologies for ultra shallow junction (USJ) formation in order to control the lateral S/D electric field spread via dopant species and, in turn, to avoid deterioration in SCE and performance of nano-scaled devices [134]. Kranti et al. [20] have reported combined effect of doping gradient (σ) of S/D profile and underlap extension length (s) on analog performance of underlap FinFET. As shown in **Fig. 2.4**, the analog performance of underlap FinFET is deteriorated when the underlap extension length (s) is reduced from $1.25L_g$ to $0.5L_g$ and the doping gradient (σ) is increased

from 3nm/dec to 7nm/dec due to intrusion of lateral S/D electric field into the channel region of the device via lower *s* and higher σ [20].

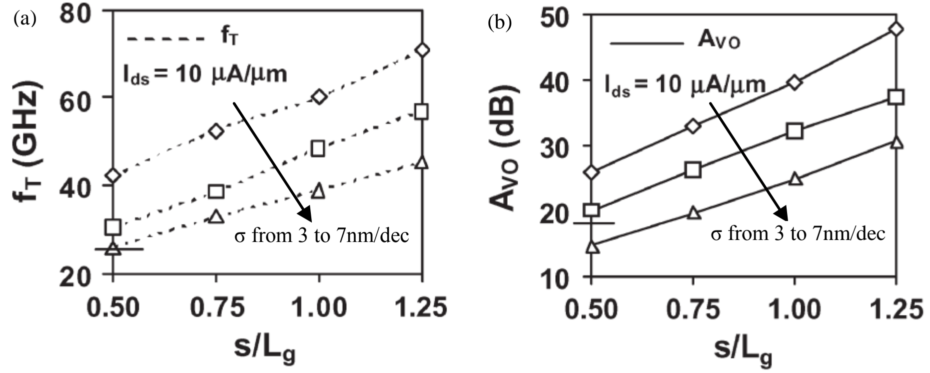

Fig. 2.4. Variation of (a) cutoff frequency (f_T) and (b) intrinsic gain (A_{V0}) with ratio of underlap spacer length to gate length (s/L_g) [20].

Formation of USJs, on the other hand, is achieved by additional process complexity and efficient temperature control step in fabrication. Ion channeling and transient enhanced diffusion (TED) are few such process challenges [96]. Conventionally, germanium or silicon is used as pre-amorphization implants (PAIs) to minimize ion channeling. Upon annealing, silicon pre-amorphization often leads to end-of-range (EOR) defects. Secondly, diffusion of boron in silicon undergoes interstitial mechanism resulting in TED. Various authors suggest use of co-implantation such as, carbon, fluorine, nitrogen etc. to reduce TED of boron atoms [183-184]. Shima et al. [94] have reported a self-limiting laser thermal process for formation of USJ. The process self controls the heating process and enhances the laser exposure window beyond the conventional limit of 300mJ/cm^2. The effectiveness of the process is verified in 50nm CMOS node and drain current improvement has been demonstrated with laser fluence. Improvements in V_{th} roll-off and subthreshold characteristics are reported because of box-like dopant distribution that can target USJ between 20 to 30nm (σ_L ~ 5nm) attributed to self limiting laser process [94]. Lerch et al. [95] have demonstrated an advanced rapid thermal processing (RTP)

which can target USJ formation. USJ close to 20nm can be targeted for p^+ MOS devices using this kind of diffusion-less flash assisted RTP. Gelpey et al. [97] have reported that with optimization of flash lamp-based ms annealing and advanced doping techniques, very shallow and abrupt USJ close to 11nm (σ_L ~ 2nm) can be targeted. Therefore, spike annealing, flash annealing, laser annealing, excimer laser annealing etc. with low-energy dopant implants are few alternatives that have been developed so far, to reduce the impact of TED and to satisfy the shallow junction requirements. But challenges like accurate temperature control and equipment maturity limits adoption of these annealing techniques [97], [155]. Moreover, Do et al. [98] have reported that, crystal defect formation cannot be completely removed even after adopting these advanced annealing techniques. In addition, USJ formation requires very shallow implant and, in turn, depends upon low implant energy. However, requirement of low implant energy is governed by ion implantation problems like low beam current and, in turn, low throughput. Few alternative doping techniques such as plasma doping, advanced plasma doping, infusion doping and molecular implants are have been proposed in literature to overcome the limitations of this implantation problem [96-98]. However, in-depth analysis with regard to device performance, cost effectiveness and process control compatibility with conventional beam-line implantation techniques are few key issues required to be studied before effective use of these doping techniques in semiconductor industry [96-98].

Recently, Santos et al. [99] have proposed molecular implant and cold implant techniques for USJ formation that can address defect removal issues in future Si devices. Different, atomistic simulation techniques are adopted for damage generation study due to amorphization of substrate during these implants. Amorphous region due to molecular implants are generated due to of an energy spike near the impact point region whereas, in case of cold implants the amorphization is caused by damage accumulation due to low temperatures which helps in extending life time of generated defects. Subsequently, a model has been developed that includes energy spike effects which can help in optimization of implant related fabrication

issues [99]. Similarly, Yang et al. [100] have demonstrated benefits of cryogenic S/D extension implants for 28nm NMOS device. It is proposed that, such integration benefit of cryo-implantation technique via damage engineering and supplemented dopant halo activation can improve SCE, DIBL and crucial device performance such as static random access memory improvement [100]. Summarizing the above discussion it can be stated that, formation of USJ is governed by defect formation and junction leakage, temperature control, equipment maturity, process control, cost effectiveness etc. [94-100].

Therefore, while deriving compact models for DG-MOSFET it is pertinent to include the effect of lateral S/D profile on channel electrostatics. The gaussian S/D profile that intrude into the channel region can be modeled as $N_{SD}(x) = N_{SD(p)}e^{-x^2/2\sigma_L^2}$ where, $N_{SD}(p)$ is the peak of gaussian profile. Due to mathematical complexity in solving equations involving this type of gaussian term, the S/D profile can be approximated by its absolute value at the each point of the channel. Subsequently, the effect of S/D profile can be introduced in terms of ionized dopant species, effective S/D ends and effective channel length calculation considering dopant degeneracy effects. For weak-inversion/ subthreshold operation of device, the 2-D poisson equation at Si-SiO_2 interface should include the ionized donor concentration ($N^+_{SD}(x)$) of S/D doping profile in addition to ionized acceptor concentration (N^-_a) [173]. Moreover, the mobile charge term in poisson equation can be neglected as suggested by Young et al. [173]. Sze et al. [185] have represented this ionized donor concentration as a function of peak doping concentration ($N_{SD(p)}$) that decays with a lateral straggle (σ_L) along the channel direction. Furthermore, factors like spin degeneracy factor (s_D), Fermi level $\left(E_F = \left(E_g/2\right) + kT\ln\left(N_{SD}(x)/n_{i,eff}\right)\right)$ and donor level $\left(E_D = E_{g,eff} - E_i\right)$ of $N_{SD}(x)$ profile need to be calculated correctly, for accurate prediction of $N^+_{SD}(x)$.

M. S. Tyagi [186] has demonstrated the many body effects, involving donor-electron interaction due to coulomb screening of donor ions by charge carriers, will reduce the donor

ionization energy (E_i). Subsequently, $E_i = E_{i0}\left(1-\sqrt[3]{N_{SD}(x)/N_{de}}\right)$ provides correct representation of ionization energy of arsenic in silicon as per experimental measurements. Where, E_{i0} is ionization energy of lightly doped substrate and the degenerated doping value N_{de} is the critical carrier concentration at which E_i will vanish. In accordance with the experimental results as explained by Morin et al. [187], the E_{i0} and N_{de} of arsenic can be set to 0.054eV and 2.7×10^{19} cm^{-3} respectively. Slotboom et al. [188] have demonstrated relations for calculation of effective intrinsic concentration as $n_{i,eff} = \sqrt{n_i^2 e^{\Delta E_g/kT}}$ and effective band gap $E_{g,eff} = E_g - \Delta E_g$, where, E_g and n_i represent bandgap and carrier density of intrinsic semiconductor. Calculation of effective S/D ends and effective channel length can be carried out considering dopant degeneracy effect of S/D doping concentration as soon as it reaches the critical value of N_{de}.

Subthreshold potential model of DG MOSFET, considering the S/D gaussian profile effect in channel region, can be derived using these effects like ionized dopant species, effective S/D ends and effective channel length calculation considering dopant degeneracy effects. Potential modeling in subthreshold regime of operation is useful in deducing crucial parameters like threshold voltage, DIBL and subthreshold slope of the device. Parabolic potential distribution along vertical direction can be assumed for model development, whose coefficients can be determined from boundary conditions, continuity of electric flux at front and back Si-SiO_2 interface and effective S/D end calculations [173-176]. The poisson equation can be subsequently solved using the potential distribution function to obtain the front surface potential and, in turn, deriving threshold voltage expression of the device. The drain current in linear and saturation region can be deduced using the threshold voltage as suggested by Suzuki et al. [128]. Due to large electric filed in saturation region of nano-scale devices, impact ionization and parasitic BJT effects are also required to be included while modeling saturation current of the device [129]. As these effects will not be present before onset of saturation, modeling of linear region can be carried out without including these effects. More so, non local

effects such as, Channel length modulation [130], velocity overshoot effect [131] and drain induced barrier lowering (DIBL) [132] are also need to be included in derivation of current models, since these effects are more prominent in deciding transistor currents and transconductance, when the device dimensions are scaled in nano-meter regime [107], [180-182]. The transconductance and output conductance of the device can be derived from the slope of I_{DS}-V_{DS} and I_{DS}-V_{GS} curve of linear and saturation currents, which can be further used to calculate the intrinsic DC gain.

2.7 Technical Gaps:

After an extensive literature survey, various technical gaps are pinpointed for current research work. These are stated as:

1. Recent works have shown that, the underlap FinFET is attainting an overwhelming response from the researchers in the field of low power and high performance digital/analog circuits in order to address the increase in demand of battery operated portable gadgets in various fields. Particularly in analog domain, where the FOM like g_m, g_{ds}, V_{EA}, g_m/I_{ds}, A_{V0}, f_T and f_{max} largely depend upon the length of the underlap section. Thus, it would be imperative to study and understand the effect of underlap extension length on these FOM and deduce an optimum underlap length subsequently.

2. Dual-*k* spacer formation in underlap section of FinFET is emerging as a viable option at shorter gate length in order to restore the loss of gate electrostatic integrity. This is because, the inner high-*k* spacer strengthens the virtually normal fringing field from gate edge and, in turn, controls the lateral spread of source to drain electric field. However, the effect of this kind of dual-*k* spacer on analog performance of FinFET has not yet been studied in detail. Since, controlling of source to drain lateral electric field will surely affect the analog FOM, therefore, further insights are required for optimum performance of dual-*k* spacer based underlap FinFET.

3. Tall and narrow fin formation, oxide thickness reduction and doping profile control are crucial aspects of analog performance improvement at nano-scale regime. However, precise dimensional requirements and process challenges are major hurdles at nano-scale regime resulting in device-to-device variability and performance variations. Designing dual-*k* spacer underlap FinFET with excellent electrostatic integrity can control this kind of performance variations due to inter device variability. Due to continuous down scaling of device dimensions, it becomes necessary to investigate this kind of dual-*k* spacer underlap FinFET and its further circuit performance through TCAD simulations.

4. Higher mobility and smaller subthreshold slope are some attractive features of low temperature operation of FinFETs at scaled gate lengths. However, very little effort has been made to enhance the analog performance of device at lower gate lengths. More importantly, most of the studies indicate further scaling down of device dimensions that can become a reality because of low leakage current, reduced latchup susceptibility and improved gate electrostatic integrity. To the best of our knowledge, very few research papers deal with the 3D TCAD simulation of underlap FinFET for analog performance study at scaled gate lengths.

5. Most of the reported papers deal with analytical models of double gate MOSFET with and without underlap. The surface potential model is deduced to further model the threshold voltage and short channel effects like DIBL and subthreshold slope. Whereas, very few papers are reported that derive analog FOM from current models that use the threshold voltage deduced from surface potential model. To the best of our knowledge, no paper deals with Modeling the dual-*k* spacer based underlap FinFET. Therefore, it is imperative to develop analytical model to accurately predict threshold voltage and drain current of dual-*k* spacer underlap FinFET. Further, the drain current model can be used to derive analog FOM like g_m, g_{ds} and A_{V0}.

6. One of the most important aspects while deriving the analytical model for MOSFET is lateral spreading of S/D dopants into the channel region. As the MOSFET is scaled into nano-scale

regime, this kind of dopant spread into the channel region will facilitate the lateral electric field spread into the channel and, in turn, deteriorate the gate electrostatic integrity. The short channel effects and performance are aggravated with increase in lateral straggle of S/D gaussian profile. To the best of our knowledge, inclusion of lateral straggle while deducing models for double gate MOSFET has not been reported yet. Hence analysis of existing models in order to include this lateral straggle term while deriving analog FOM is necessary.

Chapter 3

Impact of Dual-*k* Spacer Formation on Analog Performance of Underlap FinFET

3.1 Introduction:

Subthreshold/weak inversion regime of operation of semiconductor devices can fulfill overwhelming demand of low power, high gain and low/moderate frequency of operation, for battery operated portable devices in the field of cellular phones, wireless receivers, biomedical instruments etc [3], [20-21]. However, when the semiconductor devices are scaled into nano-meter regime, various short channel effects (SCEs) are posing serious threats to devices design aspects which, in turn, affect both digital and analog performance of the device. Among the family of multigate structures, FinFET has potential to suppress short channel effects, thereby enhancing the performance. Secondly, single lithography and etch step in fabrication is an attractive feature of FinFET due to its self aligned gates [43-44], [189]. In addition, FinFETs with source/drain underlap has the potential to enhance the performance further [45], [53-54].

The analog figures of merit (FOM) such as transconductance (g_m), output conductance (g_{ds}), early voltage (V_{EA}), transconductance-to-current ratio (g_m / I_{ds}), intrinsic dc gain (A_{V0}), cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) are affected by short channel effects and, in turn, depend upon the effectiveness of gate electrostatic integrity (*EI*) over channel region. With an increase in the extension length (L_{ext}) of underlap FinFET, these FOM are reported to improve further [20-21]. More so, downscaling of FinFET is beneficial to analog performance by improving gate electrostatic control although losses due to series parasitic increase [65]. Secondly, high

dielectric (high-k) spacers in underlap section of FinFET are reported to modulate the barrier in undoped underlap length of FinFETs [68]. The barrier modulation is a direct consequence of increase in gate fringing field which shifts the lateral electric field at the gate edge towards drain. This electric field shifting increases transconductance (g_m) and reduces output conductance (g_{ds}), thereby improves intrinsic dc gain ($A_{V0} = g_m/g_{ds}$) [20-21]. With an increase in the underlap extension length (L_{ext}), the doping profile becomes low at the gate edges. This, in turn, will restrict the lateral spread of S/D electric field into the channel region. Vega et al. [69-70] have reported that increase in source/drain extension length (L_{SDE}) of dopant segregated schottky (DSS) DG MOSFET will improve the gate electrostatic integrity (EI) as EI is inversely proportional to electrical length L_{elec} as shown in **Fig. 3.1**.

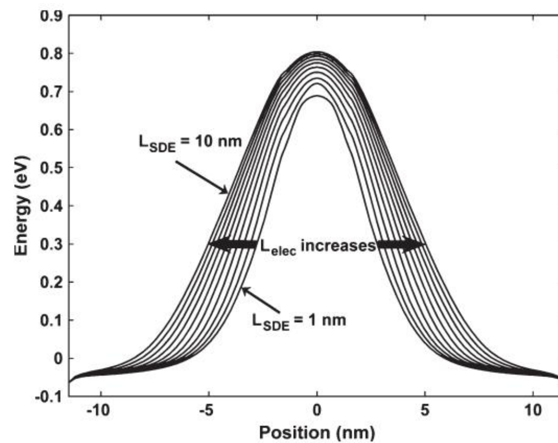

Fig. 3.1. OFF-state conduction band profile of dopant segregated schottky MOSFET for different source/drain extension length (L_{SDE}) [69].

It is also demonstrated that, the gate electrostatic integrity can be further improved by introducing high-k spacer in undoped/low-doped region created by increase in L_{SDE}. This results in dual-k spacer based DSS DG MOSFET which is a better alternative in controlling direct source to drain tunneling (DSDT) and SCEs that limit the device

scaling in nano-meter regime [69-70]. This is because lower portion of the gate sidewall is effectively coupled to source drain extension regions, thereby increasing the gate electrostatic integrity. Subsequently, Virani et al. [71-72] have analyzed the implications of dual-*k* spacer in improving performance of Tunnel FET with underlap.

In this chapter, we have analyzed the effect of gate fringing fields on device analog performance and SCEs by introducing high-*k* spacer near the gate edges. We have shown that optimized dual-*k* spacer based underlap FinFETs have potential to offer almost same cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) as compared to the single low dielectric spacer (low-*k*) FinFETs in addition to high increase in intrinsic DC gain (A_{V0}).

The primary contributions in this chapter are as follows:

1. Study of potential advantages of underlap section on performance of underlap FinFET.
2. Effect of double dielectric (dual-*k*) spacer formation on underlap section of FinFET and subsequent device physics study.
3. Optimization of inner high-*k* spacer length ($L_{sp,hk}$) of resulting dual-*k* underlap FinFET.
4. Comparison of analog figures of merit (FOM) of conventional low-*k* and optimized dual-*k* underlap FinFET and further study of gate length scaling issues.
5. Study of short channel effects in low-*k* and dual-*k* underlap FinFET.

This chapter is organized as follows: Section 3.2 of the manuscript deals with device structure and simulation method used. Section 3.3 discusses the advantages of underlap section on performance of underlap FinFET. Effect of dual-*k* spacer formation on underlap section of FinFET is studied in Section 3.4. Optimization of inner high-*k* spacer

length is taken up in Section 3.5. Subsequently, Section 3.6 compares the analog FOM of conventional low-*k* FinFET with that of optimized dual-*k* FinFET whereas comparisons of SCEs are carried out in section 3.7. Finally, section 3.8 concludes the chapter.

3.2 Device Structure and Simulation Setup:

Fig. 3.2 (a) shows a 3-D underlap FinFET structure whereas; **Fig. 3.2 (b)** shows its 2D view along the cut plane. The specifications of the device are as follows: p-type SOI layer doping (N_a) = 10^{16} cm^{-3}, peak of doping profile (N_{sd}) = 10^{20} cm^{-3}, gate oxide thickness (T_{ox}) = 1.1nm, fin thickness (W_{fin}) = 8nm, fin height (H_{fin}) = 40nm.

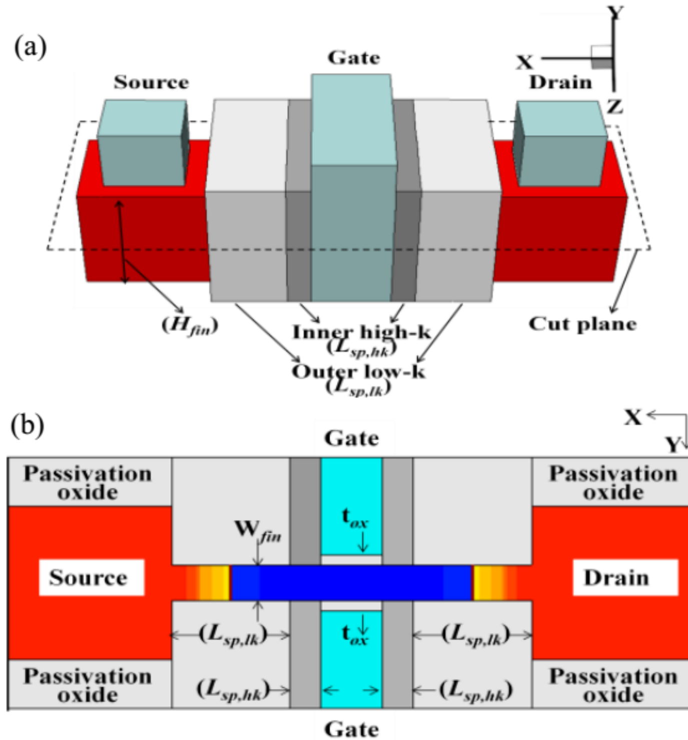

Fig. 3.2. (a) 3-D Schematic of underlap FinFET (b) 2-D view along cut plane.

Metal gate with 4.5eV gate work function is used to enhance the performance through elimination of poly-Si depletion, higher carrier mobility, higher transconductance and lower gate leakage [190-191]. Gate length (L_g) is selected as 16nm. SiO_2 is used as single low-*k* spacer ($L_{sp,lk}$) dielectric in conventional FinFET, whereas TiO_2 (k = 40) as high-*k*

inner spacer ($L_{sp,hk}$) and SiO_2 as outer spacer ($L_{sp,lk}$) are used in dual-k spacer based FinFET structures [69]. The spacer extension length ($L_{ext} = L_{sp,lk} + L_{sp,hk}$) is varied from 12nm (= 0.75 L_g) to 24 nm (= 1.5 L_g) and source/drain doping gradient (σ) = $|d \log (N_{sd}(x))/dx|^{-1}$ is varied from 3 to 7nm/dec as shown in **Fig. 3.3**. Cutoff frequency (f_T) is extracted from current gain (h_{21}) through an extrapolation of -20 dB/decade slope, whereas maximum oscillation frequency (f_{max}) is extracted from Mason's unilateral gain (MUG) [192] through an extrapolation of -20 dB/decade slope. The maximum oscillation frequency is a figure of merit related to the capability of the device to provide maximum available power gain at large frequency [192].

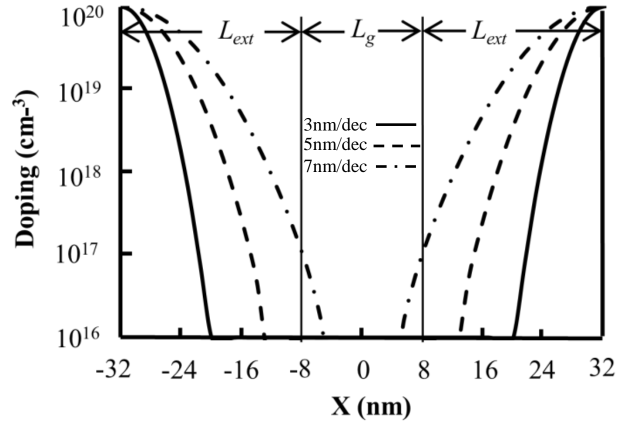

Fig. 3.3. Lateral S/D doping profile (N_{sd}) along the center of the channel showing various doping gradients (σ).

3D device simulation is carried out using TCAD mixed-mode sentarus device simulator including fin depended parasitics calculated from [44] and [65]. For calculation of S/D parasitics, contact length of 150nm, nickel silicide resistivity of 3×10^{-7} Ω.cm^2 with 23nm of SEG thickness are used as per experimental value [44]. For calculation of gate parasitics, silicide resistivity of 7.5 Ω /sq and contact resistivity of 7 Ω.μm^2 are used [65]. Suitable saturation velocity and empirical parameter β are selected to calibrate the drift diffusion transport model as per [193] and [194], to correctly couple the carrier transport

phenomena at scaled gate length. Furthermore, modified local density approximation (MLDA) quantization model, Lombardi mobility model, shockley–read–hall (SRH) recombination/generation model, band to band auger recombination and old slotboom bandgap narrowing phenomenon are also included in simulation setup [195]. Heavily doped raised source/drain regions are opted for low parasitic resistance [43-44]. However, these parasitic do not affect the device performance significantly at such low drive currents [20]. Gate height is chosen to be double of H_{fin} in accordance with effective spacer formation step [43]. Simulated and experimental [196] I_{ds}-V_{gs} characteristics of N/P FinFETs at low (50 mV) and high (1V) drain biases are shown in **Fig. 3.4**. This analysis forms the basis of our simulation setup.

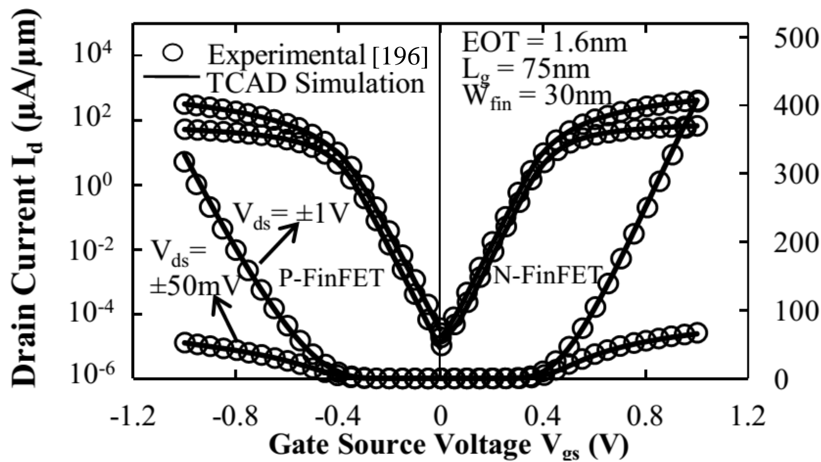

Fig. 3.4. Simulated and Experimental I_{ds}-V_{gs} characteristics of N/P-FinFETs at low (50 mV) and high (1V) drain biases.

Fabrication step of this kind of symmetric FinFET structure is similar to a standard FinFET as discussed in [43-44] and [189], with an additional steps of introducing underlap with low-k outer spacer dielectric ($L_{sp,lk}$) at both source and drain sides. The methods like asymmetric spacer formation or tilt ion implantation can be used for this kind of additional spacer formation [197-198]. Goel et al. [199] have proposed this kind

of extra asymmetric spacer formation at drain side by depositing a spacer material with a mask on source side to prevent any material from depositing on source side. Then using reactive ion etching (RIE) vertically, spacer material can be etched for required S/D (Source/Drain) doping. In case of symmetric dual-*k* spacer based design, on the other hand, the inner high-*k* spacer ($L_{sp,hk}$) can be formed and etched for required dimensions using usual steps [43], [189]. Then low-*k* outer spacer ($L_{sp,lk}$) can be formed by similar technique, without any mask at source side. RIE has to be used twice, which is same as the case of asymmetric design, before required S/D doping profile formation.

3.3 Underlap Advantages:

Increase in underlap extension length (L_{ext}) improves gate controllability with reduced SCEs because of shift in lateral electric field from gate edge toward drain. Gate edge is shown at ±8nm in **Fig. 3.3**. Therefore, analog figures of merit such as transconductance (g_m), early voltage ($V_{EA} = I_{ds}/g_{ds}$), transconductance-to-current ratio (g_m/I_{ds}), intrinsic dc gain (A_{V0}), cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) are reported to improve [20-21]. **Fig. 3.5** shows the variation of C_{gg}, g_m and g_{ds} with L_{ext}, normalized to the values obtained at extension length of 12nm. Reduction of g_{ds} is due to reduced dopant concentration at gate edge with increase in the underlap extension length, whereas reduction in C_{gg} is due to increase in the distance between gate and drain/source electrodes which makes the fringing field difficult to screen out. We observe that an increase in g_m can be attributed to high increase in electron mobility (μ_n) as g_m is directly proportional to μ_n. **Fig. 3.6** shows the variation of electron mobility along lateral direction in the channel. It can be seen that the mobility within any point in the channel increases with extension length. The increase in the mobility is due to (1) increase in undoped/low doped region towards source/drain end (2) reduction in electric field at gate edge towards

drain (as shown in the inset of **Fig. 3.6**) and resulting reduced surface scattering thereof [20], [24], [153].

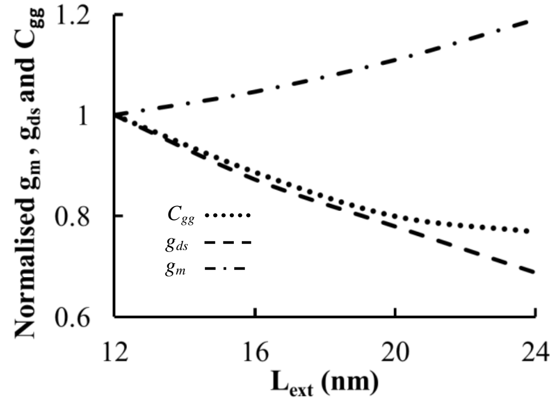

Fig. 3.5. Variation of normalised g_m, g_{ds} and C_{gg} with extension length (L_{ext}) simulated at 10μA/μm. L_g = 16nm, σ = 3nm/dec, V_{ds}=1.1V.

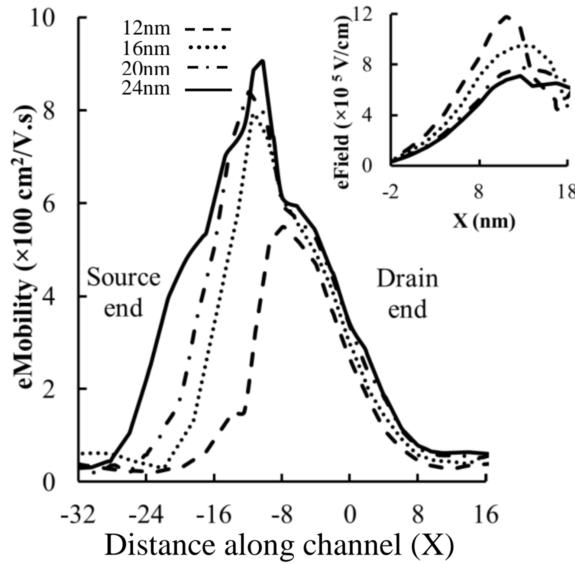

Fig. 3.6. Electron mobility and electric field at center of channel extracted at 10μA/μm for various L_{ext} based low-*k* FinFET. Simulated with σ = 3nm/dec, V_{ds} = 1.1V.

3.4 Effect of Dual-*k* on Performance:

Gate fringe induced barrier lowering (GFIBL) is observed in undoped underlap FinFETs with an increase in the dielectric constant of spacer region (L_{ext}) [68]. The barrier to

lateral drain electric field is lowered in strong inversion because of increase in the coupling of gate fringing fields to undoped underlap portion of FinFET. In weak to moderate inversion however, we observe that restricting the high-*k* dielectric to undoped/low-doped underlap portion ($L_{sp,hk}$) can strengthen the gate sidewall fringing field. These fringing fields are virtually normal to the underlap region which makes the lateral electric field from drain to source shift away from gate edge toward drain. 3-D poisson equation governing the device physics of low doped p-type fin is [155]:

$$\frac{dE_x}{dx}+\frac{dE_y}{dy}+\frac{dE_z}{dz}=\frac{q}{\varepsilon_{Si}}(p-n+N_d^+-N_a^-) \tag{3.1}$$

The fringing electric fields contribute towards increasing E_y and E_z components of eq. 3.1. Thereby, the lateral electric field E_x is reduced as the sum total of charges at the right hand side of eq. 3.1 is constant throughout the device. Larger portion of L_{ext} near the gate edge of underlap FinFET remain undoped/low-doped with an increase in its length. High-*k* dielectric used as inner spacer ($L_{sp,hk}$) can enhance the gate sidewall fringing fields in this low-doped/undoped area. **Fig. 3.7 (a)** shows the shift in lateral electric field at the gate edge toward the drain with increase in $L_{sp,hk}$. This helps in modulating the energy barrier to drain potential and in fact raises the energy barrier at weak/moderate inversion regime of operation. The GIFBL concept remains same at strong inversion because of ease in propagation of lateral electric fields at high electron concentration. This envisages the barrier modulation capability of dual-*k* spacer based underlap FinFET devices. At weak/moderate inversion regime of operation of devices, the barrier modulation capability of gate fringing fields can broaden the energy band profile by depleting the silicon layer beyond the gate edges of FinFET. The electrical length (L_{elec}) is a measure of this energy barrier broadening phenomenon. Unlike effective channel length (L_{eff}) defined at constant doping level, electrical length (L_{elec}) is defined at constant energy level. Thus effective increase in L_{elec}, due to depleted silicon region beyond gate edge, will improve

the electrostatic integrity ($EI\ \alpha\ 1/L_{elec}$) and, in turn, short channel effects are improved [69]. We observe that, this L_{elec} increases with increase in the screening of gate side wall fringing fields. The variation of L_{elec} with increase in inner spacer length $L_{sp,hk}$ is shown in **Fig. 3.7 (b)**. As the spacer length is increased, more and more fringing fields are coupled to the underlap portion, thereby improving short channel effects at low electron energies.

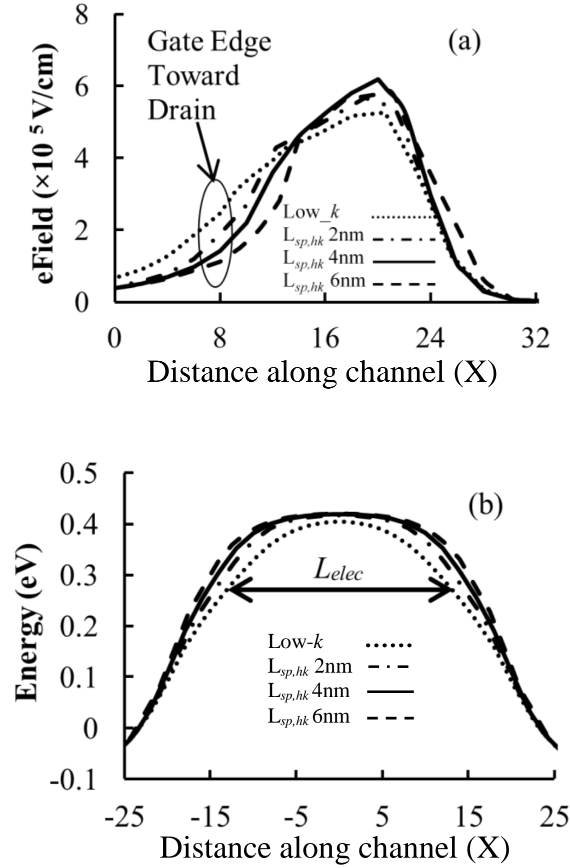

Fig. 3.7. (a) Lateral electric field at the center of the body simulated with V_{gs} = 0.3V and V_{ds} = 1.1V (b) OFF-state lateral conduction band profile at the center of the body simulated with $V_{gs} = V_{ds} = 0$V.

The improvement in short channel effects transforms into better gate electrostatic integrity and, in turn, lead to an increase in transconductance (g_m) and lowering of output conductance (g_{ds}). This increases the early voltage ($V_{EA} = I_{ds}/g_{ds}$) and transconductance-to-current ratio (g_m/I_{ds}) of the device, thereby increasing the intrinsic DC gain A_{V0} with an

increase in current as $A_{V0} = (g_m / I_{ds}) \times V_{EA}$. Furthermore, the influence of lateral drain field can degrade the gate stack reliability of nano-scale device which is of serious concern at current technologies. The reliability issues such as time dependent dielectric breakdown, bias temperature instability, channel hot carrier degradation etc. are aggravated due to of intrusion of lateral electric field into the channel region [200]. Dual-*k* spacer has potential to control the lateral electric field and can enhance the gate stack reliability issues thereby.

3.5 Inner High-*k* Spacer Length Optimisation

Fringing field screening is pronounced with an increase in length of $L_{sp,hk}$. This decreases the g_{ds} and increases g_m, gate to drain capacitance (C_{gd}) and total gate capacitance (C_{gg}). With lower value of $L_{sp,hk}$ the g_m increase can supersede the increase in C_{gg}, therefore, providing higher f_T (= $g_m/2\Pi C_{gg}$). The combined effect of improved f_T and g_{ds} can result in higher f_{max} (f_{max} is inversely proportional to $\sqrt{g_{ds} + 2\pi f_T C_{gd}}$) [20]. However, while the improvement in both f_T and f_{max} is not significant at $L_{sp,hk}$ = 2nm, the gain improvement is limited to ≈ 6dB as shown in **Fig. 3.8**. At $L_{sp,hk}$ = 4nm ($L_{ext}/6$), we have observed that, the increase in C_{gg} is almost compensated by g_m increase, therefore f_T and f_{max} of both low-*k* and dual-*k* FinFETs are almost equal wherein A_{V0} is increased by 7.73dB (≈2.5times). With further increase in $L_{sp,hk}$ (>$L_{ext}/6$), there is a tradeoff between increase in A_{V0} and decrease in both f_T and f_{max} of dual-*k* FinFET as compared to conventional low-*k* FinFET.

Further analysis is carried out by varying L_{ext} from 12nm to 24nm, σ from 3nm/dec to 7nm/dec and with $L_{sp,hk} = L_{ext}/6$ in order to observe the improvement in gain without sacrificing f_T and f_{max}. It is observed that the A_{V0} is enhanced by more than 100% (> 6dB) for all extension lengths irrespective of doping gradient as enumerated in **Table 3.1**. With doping gradient (σ) of 3nm/dec and L_{ext} = 24nm, f_T, f_{max} and A_{V0} of dual-*k* spacer based

FinFET is observed to be 110GHz, 202.4 GHz and 41.56dB respectively. Furthermore, it is observed that improvement in f_T, f_{max} and A_{V0} varies linearly with L_{ext}.

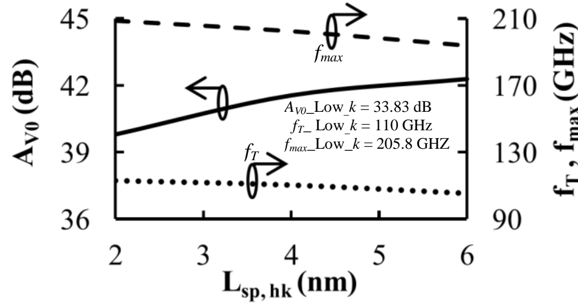

Fig. 3.8. Variation of A_{V0}, f_T and f_{max} extracted at 10 μA/μm drain current with different inner spacer length $L_{sp,hk}$. L_g = 16nm, σ = 3nm/dec, L_{ext} = 24nm, V_{ds}=1.1V.

TABLE 3.1

SIMULATED VALUES OF A_{V0}, F_T AND F_{MAX} WITH VARIATION IN DOPING GRADIENTS AND EXTENSION LENGTHS

σ (nm/dec)	L_{ext} (nm)	A_{V0} (dB)		f_T (GHz)		f_{max} (GHz)	
		Low-k	Dual-k	Low-k	Dual-k	Low-k	Dual-k
7	12	23.36	29.62	52.44	50.49	102.3	101.4
	16	26.77	34.48	68.58	67.22	130.6	129.8
	20	29.74	37.2	83.39	80.64	156.6	151.1
	24	32.29	40.48	99.46	94.34	184.5	174.6
5	12	25.77	32.57	63.63	62.67	117.7	117.2
	16	29.84	36.4	77.8	78.3	145.7	143.8
	20	31.05	38.92	93.33	94.73	174.8	169.3
	24	33.19	41.03	107.1	104.9	197.9	190.5
3	12	29.1	35.14	71.57	73.62	135	132.3
	16	30.63	37.52	83.95	86.2	157.1	158.8
	20	32.13	39.46	98.77	99.84	183.5	180.5
	24	33.83	41.56	110	110.4	205.8	202.4

3.6 Analog Performance Comparison:

The most crucial aspect of barrier modulation is lowering of g_{ds}. Variation of g_{ds} and g_m is shown in **Fig. 3.9 (a)** for doping gradient of 3nm/dec. It is observed that g_{ds} of dual-*k* spacer FinFET is reduced by 41.83% at L_{ext} = 12nm to 51.55% at L_{ext} = 24nm. g_{ds}

improvement increases early voltage (V_{EA}) due to weaker influence of lateral electric field (E_x) on the channel and is a measure of enhanced vertical gate coupling of dual-k based FinFET structure. This large increase in V_{EA} is combined with improvement in g_m to produce high increase in A_{V0}. The dual-k spacer increases C_{gg} by 13.37% at L_{ext} = 12nm to 12.04% at L_{ext} = 24nm. Increase in g_m tends to nullify the C_{gg} increase, thereby producing almost same cutoff frequency for both low-k and dual-k spacer based FinFET structures as shown in **Table 3.1**. Secondly, as f_{max} is inversely proportional to $\sqrt{g_{ds} + 2\pi f_T C_{gd}}$, the second term $2\pi f_T C_{gd}$ is compensated by g_{ds} improvement. This results in negligible reduction in f_{max} for dual-k FinFETs as compared to low-k FinFETs. The variation of C_{gg} and C_{gd} with L_{ext} are shown in **Fig. 3.9 (b)**.

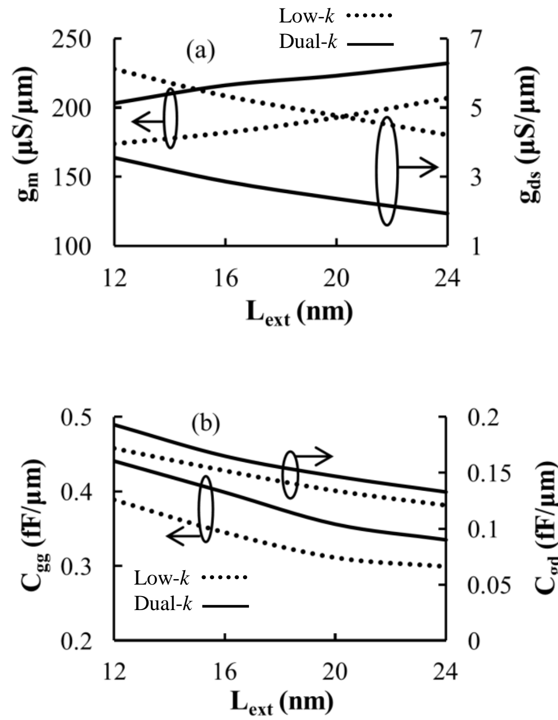

Fig. 3.9. (a) Variation of g_m and g_{ds} (b) Variation of C_{gg} and C_{gd} with extension length (L_{ext}). L_g = 16nm, σ = 3nm/dec, $L_{sp,hk} = L_{ext}/6$, V_{ds}=1.1V.

Another important factor in deciding A_{V0} at different current levels is transconductance-to-current ratio (g_m / I_{ds}) and is a measure of transconductance generation efficiency of the

device. This expresses the capability of FinFET to amplify a signal under certain dissipated power (I_{ds}). Infact, g_m /I_{ds} is a better criterion than g_m or I_{ds} to assess device performance as it represents the efficiency of the device to convert DC power into AC frequency and gain performance [157]. More so, multigate device exhibit higher values of g_m/I_{ds} due to improved charge control resulting from enhanced coupling between its gates, which leads to reduced body effect as compared to single gate device [153]. As $A_{V0} = (g_m/I_{ds}) \times V_{EA}$ therefore increase in both g_m/I_{ds} and V_{EA} increases A_{V0} at different current level. **Fig. 3.10** represents these two factors with normalized drain currents ($I_{ds}/(W_g/L_g)$).

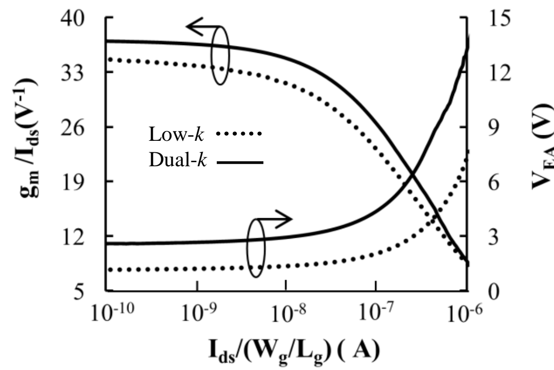

Fig. 3.10. Variation of g_m/I_{ds} ratio and V_{EA} with normalized drain current $I_{ds}/(W_g/L_g)$. L_{ext} = 24nm, L_g = 16nm, σ = 3nm/dec, $L_{sp,hk} = L_{ext}/6$, V_{ds}=1.1V.

We have further varied the gate lengths keeping $L_{ext} = 1.5\times L_g$ and $L_{sp,hk}=L_{ext}/6$ to observe the effects of barrier modulation. **Fig. 3.11** shows the variation of analog FOM with varying gate lengths. We observe that f_T and f_{max} of dual-*k* spacer FinFETs are lower than low-*k* FinFETs at higher gate lengths. With scaling of gate lengths beyond 16nm both f_T and f_{max} of dual-*k* spacer FinFETs become higher than low-*k* FinFETs. This is the case when g_m increase supersedes the increase in C_{gg}. We also observe that the intrinsic gain at L_g =12nm is up by 8.8dB as compared to 6.8dB increase at L_g = 20nm. Overall decrease of frequencies and gain with L_g, for both low-*k* and dual-*k* FinFET, is due to lower dimensional value of L_{ext} (=1.5×L_g). Nevertheless, these parameters can be improved

further with increase in L_{ext} as the gate lengths are scaled to L_g=12nm. Considering a typical case of L_g=12nm, L_{ext}=2×L_g and $L_{sp,hk} = L_{ext}/6$, we observe f_T, f_{max} and A_{V0} of dual-*k* FinFET as 114GHz, 206 GHz and 39.5 dB respectively, which are comparable to the values obtained at L_g=16nm as discussed in **Table 3.1** for the same values of L_{ext} and $L_{sp,hk}$. As compared to low-*k* FinFET the increase in these f_T, f_{max} and A_{V0} at L_g=12nm are found to be 12GHz, 8GHz and 10.5dB respectively. The improvements in both intrinsic gain and frequencies at lower gate lengths indicate the pronounced barrier modulation effect with device scaling. This envisages that, with scaling down of technology, formation of dual-*k* spacer is advantageous to single low-*k* spacer design in all aspects.

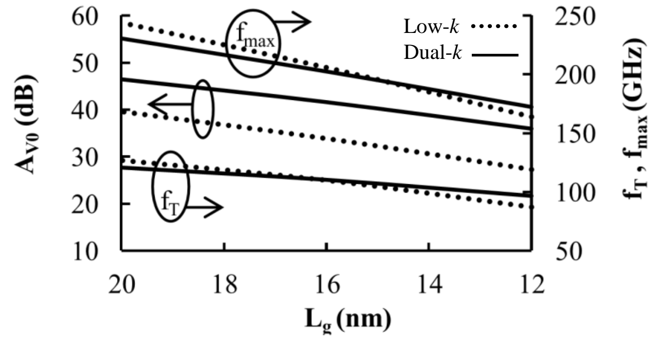

Fig. 3.11. Variation of f_T, f_{max} and A_{V0} with gate length (L_g). σ = 3nm/dec, L_{ext} = 1.5×L_g, $L_{sp,hk} = L_{ext}/6$, V_{ds}=1.1V.

3.7 Short Channel Effects Study:

Drain induced barrier lowering (DIBL) and subthreshold slope (SS) are two important factors of SCE improvement, that are addressed in this section. Doping gradient plays an important role in facilitating the lateral S/D electric field and deteriorating the SCEs. Secondly, as achieving lower doping gradient has many process related challenges, therefore, an attempt has been made to address the SCE issue by relaxing the doping gradient itself. As shown in **Table 3.2** for dual-*k* N-FinFET the improvement in DIBL is found to be enhanced from 50.27% to 54.44% and that in SS from 2.91mV/dec to

5.48mV/dec when doping gradient is increased from 3nm/dec to 9nm/dec. For P-FinFET symmetrical improvement in DIBL from 46.35% to 54.27% and SS from 4.1mV/dec to 7.57mV/dec are observed.

TABLE 3.2
DIBL AND SUBTHRESHOLD SLOPE (SS) OF N AND P CHANNEL FINFETS

Doping Gradient (nm/dec)	DIBL (mV/V)		SS (mV/dec)		DIBL (mV/V)		SS (mV/dec)	
	Low-k	Dual-k	Low-k	Dual-k	Low-k	Dual-k	Low-k	Dual-k
	N-FinFET				P-FinFET			
3	16.49	8.2	65.33	62.42	18.68	10.02	68	63.9
5	17.62	8.68	65.45	62.7	21.46	11.05	68.29	63.95
7	22.26	10.06	67.8	63.46	26.7	12.86	69.74	64.58
9	33.34	15.19	70.58	65.1	40.92	18.71	75.39	67.82

3.8 Summary:

The primary conclusions from this chapter are as follows:

Feasible dual-*k* spacer formation in underlap FinFET is an attractive option in controlling DSDT, SCEs and improving analog FOM. The transconductance and output conductance improves in all extension lengths irrespective of doping gradient. The most crucial aspect of SCE improvement is reduction of output conductance, thereby improving the intrinsic dc gain by more than 100% (> 6dB) for all extension lengths. With an optimized $L_{sp,hk} = L_{ext}/6$, the increase in capacitance of dual-*k* FinFET is compensated by transconductance improvement, thereby producing almost same cutoff and maximum oscillation frequency as compared to low-*k* FinFET in addition to high increase in intrinsic gain. Transconductance-to-current ratio and early voltage are two important parameters in deciding the intrinsic gain at different current levels. We observed that these two parameters improve by formation of dual-*k* spacer in underlap FinFET. More so, pronounced effect of barrier modulation is observed as the devices are scaled in nano-

scale regime. This would result in improved frequencies (f_T and f_{max}) and better percentage improvement in intrinsic gain of dual-*k* FinFET as compared to low-*k* FinFET.

Chapter 4

Design and Analysis of Analog Performance of Underlap FinFET and its circuit performance study

4.1 Introduction:

In this chapter, we have carried out TCAD simulation studies of various 3D underlap FinFET structures and its performance optimization in operational transconductance amplifier (OTA). Our aim is to study these structures for optimum underlap length, fin height and width, oxide thickness and lateral straggle, in terms of analog FOM as well as the parametric variation issues affecting the performance. Subsequently, crucial spatial variations like oxide thickness and lateral straggle that affect the OTA performance are addressed in detail. We have started with device physics study of conventional low-*k* as well as proposed dual-*k* underlap FinFET that affect the analog FOM at scaled gate lengths.

Power efficient, area efficient and cost-efficient heterogeneous System-on-chip (SoC) integration are key factors in modern IC design to address the overwhelming increase in battery operated portable devices. Typical examples are GSM/EDGE baseband processors for cellular phones [19], medical instruments [20], wireless sensor networks and ambient intelligent systems [18]. Elementary digital/analog circuits such as CMOS logic gates, SRAM cells, reference circuits, current mirrors, operational amplifiers are basic building blocks of SoC IC design. Subthreshold/weak inversion regime of operation of advanced MOS devices can meet the targeted low power, high gain and low/moderate frequency environment to realize the aforementioned digital/analog circuits [3], [20-22]. Improved short channel effect (SCE) immunity and increased gate electrostatic control are of

paramount importance in order to pursue scaling at nano-scale regime without deteriorating the performance.

However, at channel length of < 20nm, unavoidable non zero lateral straggle (σ_L) of source/drain (S/D) doping profile facilitate the drain potential to strongly influence the channel potential due to ease in propagation of lateral S/D electric field, leading to inability of the gate to switch off the channel current and reducing the gate electrostatic integrity (*EI*). This loss of gate controllability over the channel region, considered as short channel effects (SCEs), is of serious concern in nano-scaled devices affecting both digital and analog performance. Therefore, in order to pursue scaling at nano-scale regime, alternative multi-gate architectures such as FinFET is emerging as a strong contender, offering better immunity to SCEs and increased gate electrostatic control. This is because of better screening of longitudinal electric field at the source end of the device due to close proximity of multiple gates, resulting in reduced drain induced barrier lowering (DIBL) and improved subthreshold swing (SS), the important factors of SCEs [201]. In addition, the need of channel doping can be eliminated due to use of ultra thin silicon film which, in turn, can reduce (i) parametric spread resulting from dopant fluctuations and (ii) junction leakage current due to high electric fields [84]. Recent studies show that providing sufficient underlap in FinFET structure can restrict the S/D junction formation to underlap section rather than channel region [45], [53-54]. The result is higher effective channel length (L_{eff}) of the device, possibly greater than the physical length (L_g), and, in turn, better SCE immunity. The analog figures of merit (FOM) such as g_m, g_{ds}, V_{EA}, g_m/I_{ds}, A_{V0}, f_T and f_{max} are affected by the effectiveness of gate electrostatic integrity (*EI*) over channel region. Therefore, tall and narrow fin formation, oxide thickness reduction and doping profile control are crucial aspects of performance improvement at nano-scale regime due to of resulting excellent electrostatic control over channel [84-86]. However,

incorporating tall and narrow fins (high aspect ratio) into a small area of the substrate poses unique manufacturing challenge. Because, in addition to various mechanical stresses encountered during manufacturing, the height of the tall and heavier fin may concentrate larger internal stresses in its relatively narrow base. The larger the forces, the greater are the chances of fin becoming susceptive to fracture and causing failure in transistor operation. [91-93]. In addition, process induced variations in the fins and oxide thickness become more prominent with shrinking device dimensions causing negative impact on the inter device variability and, in turn, degrading the mismatch parameter [87-90], [92]. Second aspect of design consideration is controlling doping profile. These days, designers are aiming for ultra shallow junction (USJ) formation in order to control the lateral electric field spread into the channel region [134]. Nevertheless, USJ formation is governed by various process related issues such as, defect formation and junction leakage, temperature control, equipment maturity, effective process control, cost effectiveness etc. [94-100]. This culminates in designing FinFET with excellent *EI* so that the performance is less immune to parametric variations and inter-device variability considering the aforementioned process challenges.

Vega et al. [69] have reported recently that, dual-*k* spacer formation in underlap FinFET is a better alternative in improving digital performance, controlling direct source to drain tunneling (DSDT) and SCEs. Subsequently, dual-*k* spacer based FinFET has the potential to enhance the analog performance of the device by shifting the lateral electric field at the gate edge toward drain. Secondly, the effect is pronounced with gate length scaling, because of resultant increase in fringing fields. In the first part of this chapter, we have focused on variation of fin height (H_{fin}), fin width (W_{fin}), oxide thickness (T_{ox}) and lateral straggle (σ_L) of S/D doping profile and studied its effect on analog performance of conventional low-*k* and dual-*k* spacer based underlap SOI FinFETs. As these design

parameters decide the *EI* as well as processing challenges, therefore, study about the same is crucial considering the reduction in device dimensions.

Another objective of this chapter is to study the impact of local variations in threshold voltage (V_{th}) and mobility (μ), with crucial process induced variations in T_{ox} and X_j, that are two important aspect of analog circuit design at smaller processing nodes [162-163]. The effect of μ will alter the transconductance factor $\mu C_{ox}(W/L)$, whereas, the combined effect of V_{th} and μ will affect transconductance (g_m), output conductance (g_{ds}), transconductance-to-current ratio (g_m /I_{ds}) and intrinsic dc gain (A_{V0}) at device level. This would translate into large variations in crucial circuit level FOM such as, common mode gain (A_{CM}), differential mode gain (A_{DM}) and common mode rejection ratio (*CMRR*) [101], [164-166]. More so, the circuit level variations will be pronounced at smaller technology node, if the variations in V_{th} and μ are not controlled at device level. Device mixed mode simulations are required to be carried out to analyze these effect on important analog building blocks such as, differential amplifier or operational transconductance amplifier (OTA).

The primary contributions of this chapter are as follows:

1. Device physics study of dual-*k* spacer based underlap FinFET in terms of conduction band energy and subsequent performance evaluation at analog domain.
2. Design and analysis of conventional and dual-*k* underlap FinFET in terms of:
   (i) Aspect ratio (H_{fin}/W_{fin})
   (ii) Fin width (W_{fin})
   (iii) Oxide thickness (T_{ox})
   (iv) Lateral straggle (σ_L)
3. Study of possible alternative high-*k* material for dual-*k* spacer design.

4. Single stage OTA design and its performance study.
5. Spatial variation study in terms T_{ox} and σ_L, its effect on V_{th} and μ of the affected device and its subsequent effect on circuit performance of OTA.
6. Study of gate length scaling issue on OTA performance.

This chapter is organized as follows. Study of device physics and, in turn, analog performance related issue is carried out in Section 4.2. Section 4.3 presents design related issues in underlap FinFET in terms of analog performance. This section also covers studies related to possible use of alternative high-*k* material for dual-*k* spacer design. Section 4.4 analyzes the circuit performance of single stage OTA which is further extended to study the effects of spatial variations on performance. More so, gate length scaling issues on OTA performance is also included in this section. Finally, the major conclusions are drawn in Section 4.5.

4.2 Dual-*k* underlap FinFET Device Physics Study:

Fig. 4.1 (a) shows a 3-D dual-*k* underlap FinFET structure with the following specifications: SiO_2 as gate oxide with EOT of 1.1nm throughout the analysis (except when T_{ox} is changing), channel doping (N_a/N_d) = 10^{16} cm^{-3}, peak of doping profile (N_{sd}) = 10^{20} cm^{-3}, gate length (L_g) = 12nm, SOI layer thickness = 150nm. SiO_2 is used as single low-*k* spacer ($L_{sp,lk}$) dielectric in conventional FinFET, whereas TiO_2 (k = 40) as high-*k* inner spacer ($L_{sp,hk}$) (except when *k* is changing) and SiO_2 as outer spacer ($L_{sp,lk}$) are used in dual-*k* spacer based FinFET structures. Metal gate work functions are set as 4.6eV and 4.7eV for N and P-FinFETs, respectively. S/D doping profile has been modeled as N(x) = N_{sd} exp ($-$ $x^2/2\sigma_L^2$) as shown in **Fig. 4.1 (b)**. Since g_m plays a major role in deciding important FOM such as A_{V0} and f_T, therefore, the spacer extension length (L_{ext}) of low-*k* underlap FinFET has been selected as 18nm considering limited g_m improvement

after this length as shown in **Fig. 4.1 (c)**. Consequently, same spacer extension length (L_{ext} = $L_{sp,lk}$ + $L_{sp,hk}$) is selected for dual-*k* FinFET with optimised $L_{sp,hk}$ = L_{ext}/6 for analysis purpose as discussed in chapter 3.

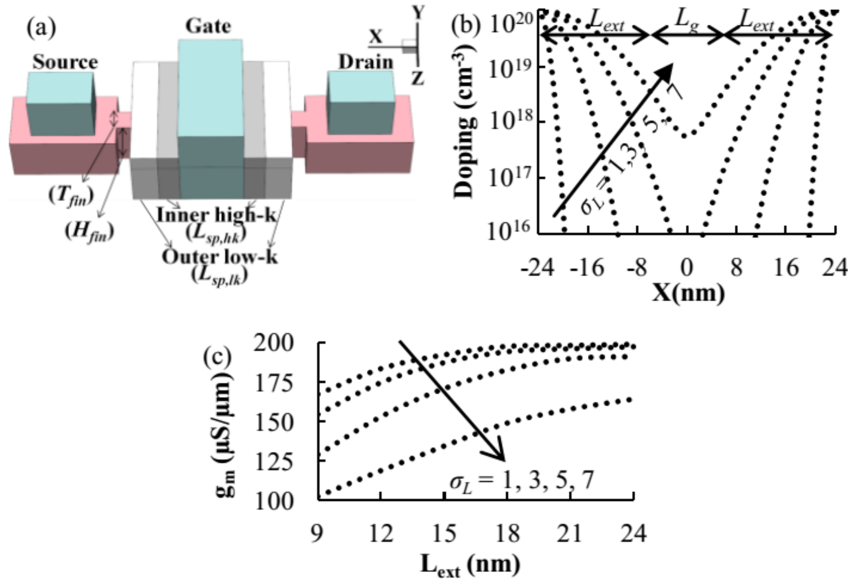

Fig. 4.1. (a) 3-D Schematic of dual-*k* underlap FinFET. (b) Variation of lateral source/drain doping profile N(x) for various lateral straggle (σ_L) values along the center of the channel (c) g_m variation with L_{ext} extracted at 10µA/µm.

Due to gate fringe induced barrier lowering (GFIBL) the barrier to lateral drain electric field is lowered in strong inversion because of an increase in the coupling of gate fringing fields to undoped underlap portion of FinFET [68]. In chapter 3, we observe that, by strengthening these virtually normal fringing fields, the lateral electric field from drain to source can be shifted away from gate edge toward drain at weak/moderate inversion regime of operation. This helps in raising the energy barrier as shown in **Fig. 4.2**. The electrical length (L_{elec}), defined at constant energy level, will improve due to depleted silicon region beyond gate edge and, in turn, improves the electrostatic integrity ($EI\ \alpha\ 1/L_{elec}$) [69]. The improvement in *EI* can lead to an increase in g_m and lowering g_{ds}. The decrease in g_{ds} is a direct consequence of decrease in drain control over the channel and

reduced channel length modulation. This will improve the quality of the device as a constant current source. In addition, the improvements in early voltage ($V_{EA} = I_{ds}/g_{ds}$) and transconductance-to-current ratio (g_m/I_{ds}) of the device raises the intrinsic DC gain (A_{V0}) with an increase in current as $A_{V0} = (g_m /I_{ds}) \times V_{EA}$. The g_m/I_{ds} ratio is a measure of transconductance generation efficiency of the device which expresses the capability of FinFET to amplify a signal under certain dissipated power (I_{ds}) [157]. **Fig. 4.3** represents g_m/I_{ds} and V_{EA} with respect to normalised drain currents ($I_{ds}/(W_g/L_g)$).

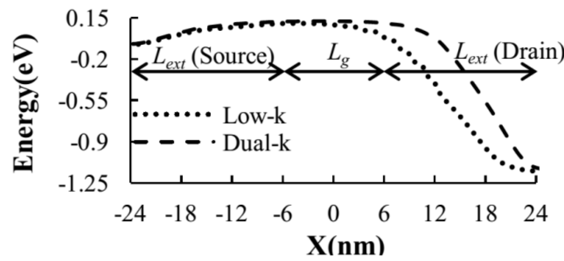

Fig. 4.2. Variation of conduction band energy as a function of X for low-*k* and dual-*k* FinFET. Simulated with $AR = 5$, $W_{fin} = 0.6L_g$, $T_{ox} = 1.1$nm, $\sigma_L = 3$nm, V_{ds}=1.1V and V_{gs} = 0.35V.

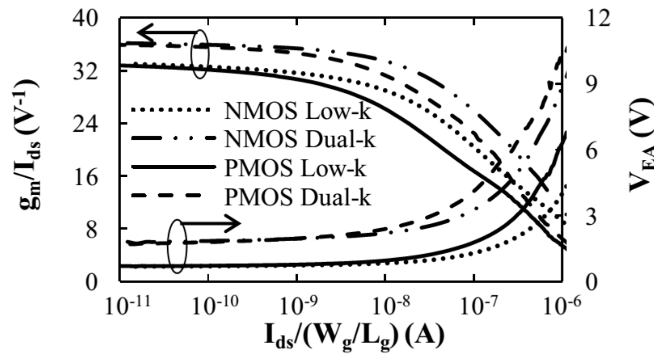

Fig. 4.3. Variation of g_m/I_{ds} ratio and V_{EA} with respect to normalised drain current $I_{ds}/(W_g/L_g)$. Simulated with $AR = 5$, $W_{fin} = 0.6L_g$, $T_{ox} = 1.1$nm, $\sigma_L = 3$nm and V_{ds} = 1.1V.

4.3 Design and Analysis:

Major design parameters that decide the gate electrostatic integrity (*EI*) of underlap FinFET are: aspect ratio (*AR*), L_{ext}, W_{fin}, T_{ox} and σ_L of S/D profile. In previous chapter, we have addressed the issues related to L_{ext} variation. Therefore, we have selected a fixed L_{ext} of 18nm (1.5L_g) with TiO_2 as inner high-*k* spacer ($L_{sp,hk}$) and varied W_{fin}, *AR*, T_{ox} and σ_L to study the effects of gate electrostatic integrity and, in turn, its effect on variation of analog FOM of both N/P-FinFETs. More so, the dielectric constant (*k*) of $L_{sp,hk}$ has also been varied to study the effect of various high-*k* dielectric on analog FOM. The FOM are extracted at $I_{ds} = 10\ \mu A/\mu m$ targeting weak/moderate inversion regime of operation.

4.3.1 Performance Variation with Aspect Ratio (AR):

Taller fins are required for high drive current and matching the current drivability, whereas narrow fins ensure better SCE immunity. Secondly, taller fins can improve f_T and f_{max} of multi-fin devices when the same channel width of the device is distributed over less number of taller fins as compared to the distribution over larger number of shorter fins [85]. However, manufacturing challenges and associated mechanical stresses are few major concerns of taller fin devices. With increasing *AR* of the device, the height may induce larger internal stresses in its relatively narrow base causing mechanical fracture and, in turn, operational failure [91-93]. **Fig. 4.4** plots the analog FOM of both N/P-FinFETs with varying aspect ratio (*AR*). It is observed that, g_m, g_{ds}, C_{gg} and C_{gd} reduces almost linearly with increasing *AR*. The intrinsic gain (A_{V0}) of dual-*k* N/P-FinFETs are increased by more than 3 times (≈ 10dB) as compared to their low-*k* counterpart and both the designs produces almost constant gain (slightly increasing). The increase in f_T and f_{max} with *AR* are linear for both designs. However, the improvements are not significant after *AR* = 5. This is, because the contribution from top gate is limited after

AR = 5, resulting in reduced transconductance and limited reduction in capacitance. As $f_T = g_m/2\Pi C_{gg}$, the limited reduction in capacitance is further counteracted by g_m reduction. Similarly, as f_{max} is inversely proportional to $\sqrt{g_{ds} + 2\pi f_T C_{gd}}$ [21], therefore, f_T increase tends to compensate reduction in C_{gd} and g_{ds}. Secondly, f_T and f_{max} of dual-k design tend to saturate earlier as compared to low-k design due to limited capacitance reduction. But the improvement at AR ~ 5, considering the top gate contribution, is still a good option.

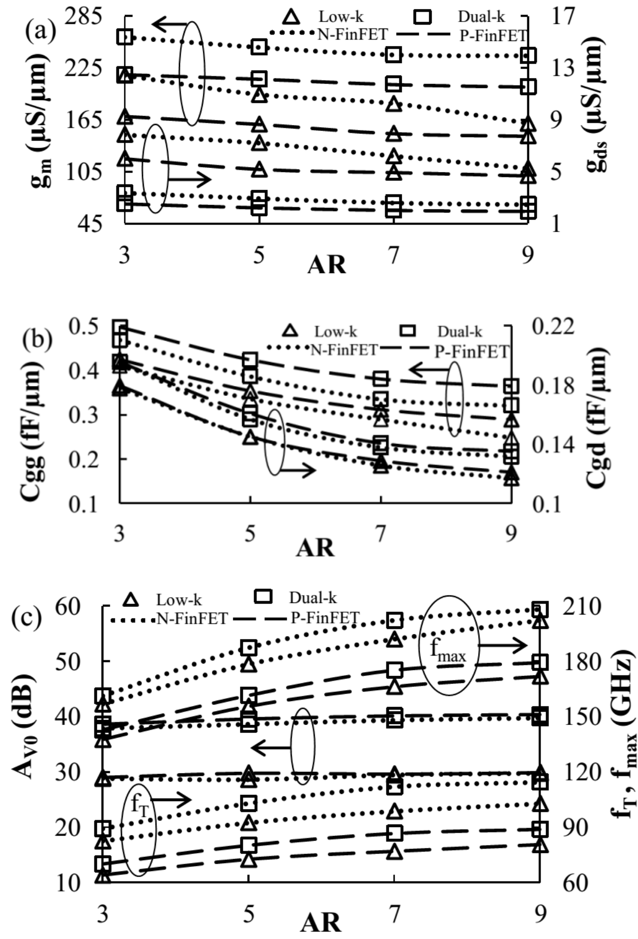

Fig. 4.4. Variation of (a) g_m and g_{ds} (b) C_{gg} and C_{gd} (c) A_{v0}, f_T and f_{max} of N/P-FinFETs with aspect ratio (AR). Simulated with $W_{fin} = 0.6L_g$, $T_{ox} = 1.1$nm, $\sigma_L = 3$nm and $V_{ds} = 1.1$V.

At AR = 5 we have observed that, f_T and f_{max} of dual-k N-FinFET are higher by 11% and 5%, respectively, as compared to low-k N-FinFET in addition to high increase in A_{V0}. These frequency improvements are restricted to 8.5% and 2.5% for P-FinFET because of

lower g_m resulting from poor mobility. Interestingly, g_{ds} too suffers from poor mobility, therefore, overall intrinsic gain of P-FinFETs are higher. Considering the manufacturing challenges and limited performance improvements of taller fins ($AR > 5$), it is desirable to aim for dual-k spacer based N/P-FinFETs with shorter fins ($AR \sim 5$) that outperforms the low-k designs in all aspect.

4.3.2 Performance Variation with Fin Width:

Due to close proximity of multiple gates, at smaller W_{fin}, the longitudinal electric field at the source end of the device can be easily screened out which increases the EI [201]. However, as the transistors are scaled down, variations in critical transistor attributes such as W_{fin} and T_{ox} are becoming major issues in transistor design. Moreover, these variations are pronounced as the feature sizes approach the size of atoms or the usable light wavelength required for patterning lithography masks [159]. Subsequently, the study reveals that, analog circuits are of particular importance, where the device level performance variations can substantially alter the specification of the particular circuit from its desired value [89]. In addition, variation along the channel width direction better known as line edge roughness (LER) can degrade the short channel immunity and performance in addition to device-to-device variability [88]. In the present work, however, we have only studied the effects of W_{fin} variation on analog performance. Although this simplistic approach does not fully capture the LER effect, but will definitely explore the device physics associated with W_{fin} variation with/without LER.

Fig. 4.5 shows the variation of analog FOM with W_{fin}. At the aforementioned technology node, Huang et al. [202] have reported that, W_{fin} of the order of $0.7L_g$ is required for improved performance and better SCE immunity. Therefore, we have varied the W_{fin} from $0.5L_g$ to $0.8L_g$. It is observed that, A_{V0}, f_T and f_{max} of both low-k and dual-k N/P-FinFETs

decrease linearly with W_{fin}. The gain improvement factor of dual-k FinFET is almost constant till $W_{fin} = 0.7L_g$, after which it tends to decrease due to higher percentage increase in g_{ds}. At $W_{fin} = 0.8L_g$, however, it is observed that A_{V0} of dual-k N/P-FinFETs are higher by 8.8/8.7dB respectively as compared to low-k N/P-FinFETs. Nevertheless, percentage improvement in f_T and f_{max} of dual-k N/P-FinFETs is enhanced at higher W_{fin}. Secondly, lesser g_{ds} variation of dual-k FinFET with W_{fin} is an attractive feature from analog circuit design point of view particularly when the device is used as constant current source.

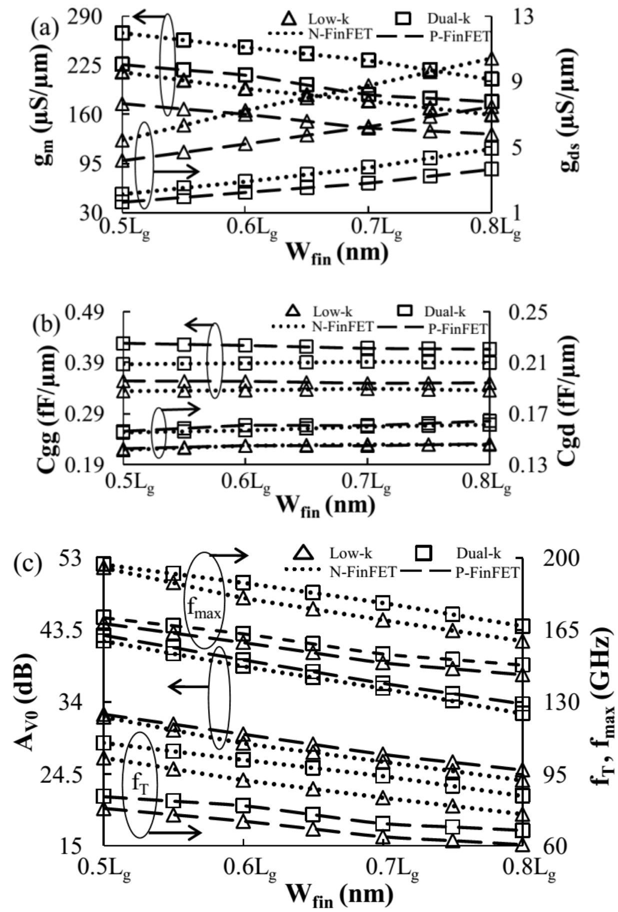

Fig. 4.5. Variation of (a) g_m and g_{ds} (b) C_{gg} and C_{gd} (c) A_{v0}, f_T and f_{max} of N/P-FinFETs with fin width (W_{fin}). Simulated with H_{fin} = 36nm, T_{ox} = 1.1nm, σ_L = 3nm and V_{ds} = 1.1V.

In addition, the percentage improvements in f_T and f_{max} of dual-k N/P-FinFETs are limited below $W_{fin} = 0.5L_g$. This may be attributed to the fact that, the effective screening of gate fringing fields is improved with W_{fin} scaling, thereby increasing the gate capacitance. Therefore, designing dual-k N/P-FinFETs with AR ~ 5 and $0.5L_g \leq W_{fin} \leq 0.7L_g$ is a better option as compared to low-k N/P-FinFETs.

4.3.3 Performance Variation with Oxide Thickness:

Variation in oxide thickness is another limiting factor at nano-scale devices with shrinking device dimensions. Thicker T_{ox} or W_{fin} will reduce the EI factor and degrade the analog FOM and aggravate SCE [159].

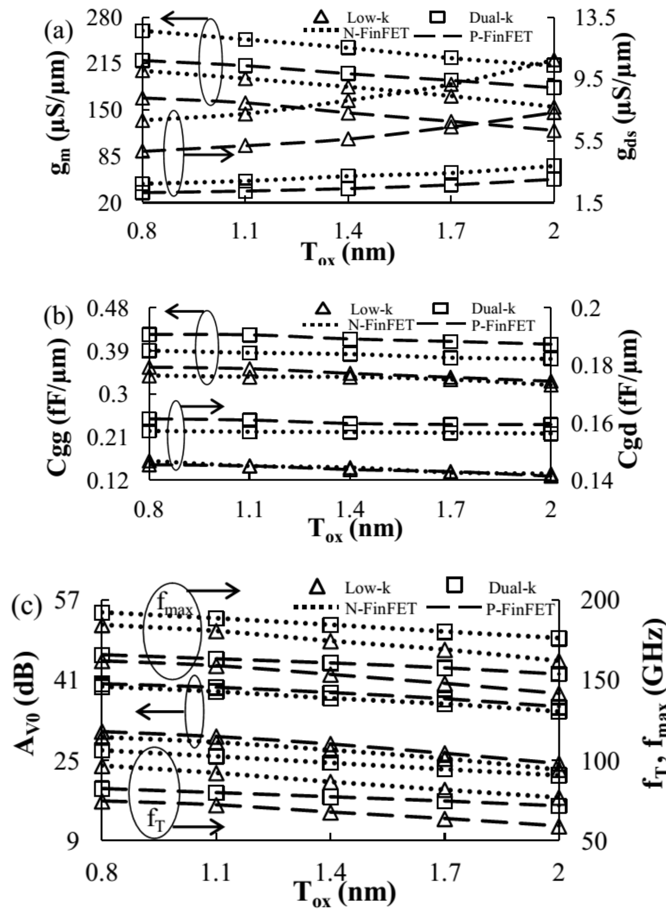

Fig. 4.6. Variation of (a) g_m and g_{ds} (b) C_{gg} and C_{gd} (c) A_{v0}, f_T and f_{max} of N/P-FinFETs with oxide thickness (T_{ox}). Simulated with $AR = 5$, $W_{fin} = 0.6L_g$, σ_L = 3nm and V_{ds} = 1.1V.

Fluctuation in threshold voltage is observed due to oxide thickness variation resulting from interface roughness [87]. Evidently, fluctuation is more pronounced at smaller T_{ox} resulting in pronounced analog FOM variation. **Fig. 4.6** plots the variation of analog FOM with oxide thickness. As can be seen, the g_m of dual-k N/P-FinFETs does not vary as much as g_m of low-k N/P FinFETs does. The g_{ds} variation is even lesser for dual-k N/P-FinFETs. Although both of these parameters reduce with T_{ox} for all designs, but the improvement in A_{V0} for dual-k N/P-FinFETs is better (~11.5dB) at T_{ox} = 2nm as compared to the improvement (~10dB) at T_{ox} = 0.8nm, thereby reducing the A_{V0} variation to T_{ox} in contrast to low-k designs. Furthermore, the variation in f_T and f_{max} of dual-k designs are also less than those of low-k designs. This is attributed to 18% (8%) improvement in f_T (f_{max}) of dual-k N-FinFET and 21% (9%) improvement in f_T (f_{max}) of dual-k P-FinFET as compared to low-k design at T_{ox} = 2nm. Higher percentage improvements in both g_m and g_{ds} with T_{ox} are key factors in maintaining these FOM variations to lesser value.

For dual-k design, the equivalent oxide thickness (EOT) of inner high-k section can be calculated by integrating the outer fringing field line path between the smaller of T_g (gate height) plus T_{ox} and $L_{sp,hk}$ as [203]:

$$EOT_{hk} = \left(\frac{\varepsilon_{lk}}{\varepsilon_{hk}}\right)\int_{L_{sp,hk}}^{T_g+T_{ox}}\left(\frac{dx}{x}\right) = \left(\frac{\varepsilon_{lk}}{\varepsilon_{hk}}\right)\ln\left(\frac{T_g+T_{ox}}{L_{sp,hk}}\right) \tag{4.1}$$

where, the ratio ($\varepsilon_{lk}/\varepsilon_{hk}$) is introduced so that EOT_{hk} is inversely proportional to k. Considering T_g ~ 5nm and T_{ox} =1.1nm, the EOT_{hk} with 3nm of inner TiO_2 will be ~ 0.069nm which is considerably smaller than the EOT directly under the gate (being 1.1nm). This indicates that, the inner high-k spacer will strengthen the fringing fields and facilitate its better screening at source/drain ends of underlap section resulting in better EI and improved FOM. With an increase in T_{ox} to 1.4nm the EOT_{hk} becomes ~ 0.074nm

increasing merely by ~ 0.005nm. Therefore, the FOM improvement of dual-*k* design is enhanced at higher T_{ox} as shown in **Fig. 4.6**.

4.3.4 Performance Variation with Lateral Straggle:

As the devices are scaled to nano-scale regime, formation of USJ can control the lateral electric field spread into the channel region [134].

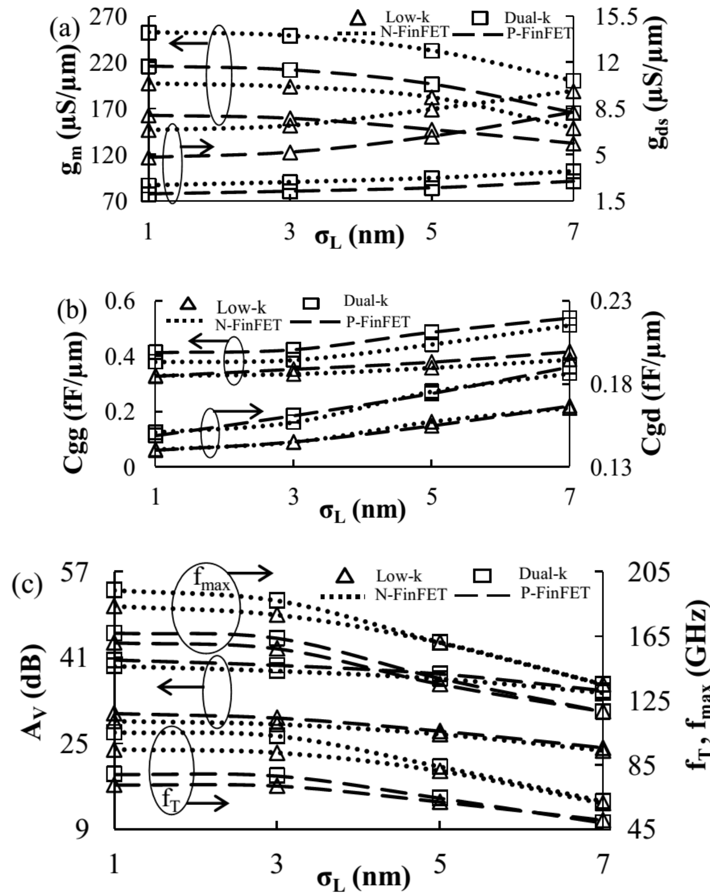

Fig. 4.7. Variation of (a) g_m and g_{ds} (b) C_{gg} and C_{gd} (c) A_{v0}, f_T and f_{max} of N/P-FinFETs with lateral straggle (σ_L) of S/D profile. Simulated with $AR = 5$, $W_{fin} = 0.6L_g$, $T_{ox} = 1.1$nm and $V_{ds} = 1.1$V.

However, formation of USJ is governed by defect formation and junction leakage, temperature control, equipment maturity, process control, cost effectiveness etc. More so, USJ formation is even more difficult in case of P-FinFET because of annealed limited

transient enhanced diffusion (TED) in boron [95]. Considering the above facts, till now we have simulated the devices with a reasonable junction depth (X_j) of ~ 13nm (σ_L = 3nm). Nevertheless, this section varies the lateral straggle (σ_L) from 1nm (X_j ~ 5nm) to 7nm (complete overlap structure). **Fig. 4.7** plots the variation of analog FOM with σ_L. The gain improvement is observed to be almost constant for both dual-*k* N/P-FinFETs whereas improvement in f_T and f_{max} reduces with increasing σ_L resulting in a higher variation of f_T and f_{max}. This trend is attributed to the fact that the fringing field screening via inner high-*k* spacer is more pronounced when the underlap portion near gate edges remain undoped/lowly doped. At σ_L = 7nm however, the achievable gain of both dual-*k* N/P-FinFETs is ~35 dB without f_T and f_{max} degradation, a fact which is still attractive in designing circuitry for battery operated portable devices. In addition, the percentage improvement in g_{ds} with increasing σ_L is more suitable for designing ideal current mirrors. With advancement in junction technology, these FOM can be improved further.

4.3.5 Selecting Alternate High-*k* Material as Inner Spacer:

Dielectric constant of inner high-*k* spacer has a direct impact on analog FOM. Screening of fringing fields will be limited by reducing *k* value of inner high-*k* spacer and, in turn, will reduce A_{V0}, f_T and f_{max} linearly as shown in **Fig. 4.8**. This is because the EOT_{hk} will increase by reducing *k* in accordance to eq. 4.1, while the length of $L_{sp,hk}$ is kept constant. We have observed that with k = 22 (HfO_2) the EOT_{hk} calculated from eq. 4.1 will be ~ 0.126nm, thereby limiting improvements in A_{V0}, f_T and f_{max} to 2.35 times (7.4dB), 6% and 2%, respectively, as compared to low-*k* design. It should be noted that an attempt to increase $L_{sp,hk}$ to reduce EOT_{un} to ~ 0.069nm (to match with EOT_{un} of dual-*k* TiO_2) will deteriorate f_T and f_{max} further. Nevertheless, with HfO_2 as inner high-*k* spacer, the improvements in A_{V0}, f_T and f_{max} as compared to low-*k* designs are still better for its use in place of TiO_2, where improvements are 3times (10dB), 11% and 5%, respectively.

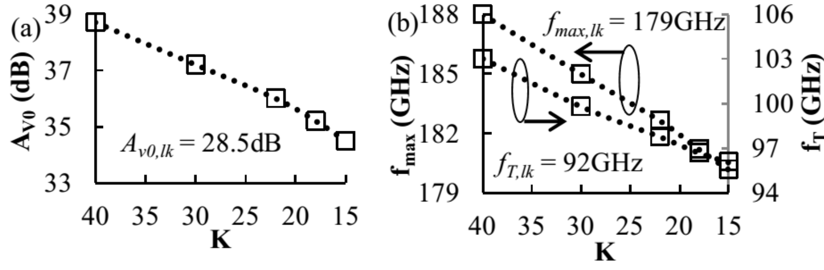

Fig. 4.8. Variation of (a) A_{V0} (b) f_T and f_{max} of dual-k N-FinFETs with spacer dielectric constant (k). Simulated with $AR = 5$, $W_{fin} = 0.6L_g$, σ_L = 3nm and V_{ds} = 1.1V.

4.4. Circuit Performance Study of Single stage OTA:

In this section, results are extracted for spatial variations in major parameters of single stage OTA through 3D mixed simulations.

Increasing demand of miniaturized battery operated portable devices, leads to scaling down the semiconductor device dimensions into nano-meter regime. However, problems like SCE and performance deterioration are crucial issues that are needed to be addressed at device level in order to target optimum circuit performance. Most important is the fluctuation in performance of analog circuits due to local variations in critical transistor attributes such as T_{ox} and X_j. Lakshmikumar et al. [163] have reported that, threshold voltage (V_{th}) and transconductance factor ($K = \mu C_{ox}(W/L)$) are two crucial parameters that can affect the drain current matching. Subsequently, Kinget et al. [101] have pointed out that, the impact of V_{th} mismatch is a dominant term in deciding performance accuracy of CMOS. Therefore, threshold voltage (V_{th}) and mobility (μ) are two important aspect of device design that are affected due to process induced variations in T_{ox} and X_j. Variation in oxide thickness is a lithography step generated limiting factor at nano-scale devices with shrinking device dimensions [87], [204]. Whereas, formation of ultra shallow

junction (USJ) is governed by various process related issues as discussed in last section. [94-100]. Evidently, fluctuation in T_{ox} and X_j are pronounced at lower technology nodes.

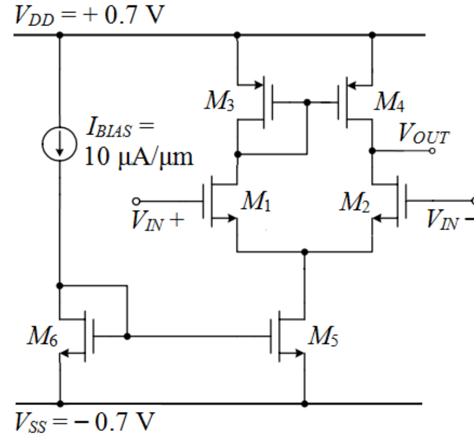

Fig. 4.9. Schematic of single stage OTA circuit.

TABLE 4.1

DEVICE SPECIFICATIONS

Attributes	Low-*k*		Dual-*k*	
	N-FinFET	P-FinFET	N-FinFET	P-FinFET
σ_L (nm)	2	2	2	2
T_{ox} (nm)	1	1	1	1
Φ_m (eV)	4.69	4.61	4.69	4.61
V_{th} (V)	0.3861	- 0.3790	0.4146	- 0.4038
I_{OFF}	10pA/μm	12pA/μm	2.6pA/μm	2.1pA/μm
10μA/μm @V_{GS} =	0.4516V	- 0.4508V	0.4762	- 0.4719V

Fig. 4.9 shows a single stage OTA whereas, **Table 4.1** lists out important attributes that are matched for subsequent analog circuit design. Device specifications that are used for the analysis are: L_g = 16nm, L_{ext} = 1.5× L_g, T_{ox} = 1nm, σ_L = 2nm, W_{fin} = 8nm, AR = 5. However, while parameters like W_{fin} and AR are kept constant throughout the analysis, suitable variations in T_{ox} and σ_L are selected for spatial variation study. Secondly, L_g is constant throughout the spatial variation analysis except in last part of the study that addresses the scaling issues.

Dual-*k* spacer architecture in underlap section of FinFET will strengthen the virtually

normal gate edge fringing fields via inner high-*k* spacer. This would control the lateral S/D electric field spread into the channel region and improve *EI*. More so, the *EI* of dual-*k* FinFET is less affected by thicker T_{ox} and higher X_j that can enhance the spreading of lateral S/D electric field. Subsequently, V_{th} and μ of dual-*k* FinFET are less affected by spatial change in dimensions of T_{ox} and X_j.

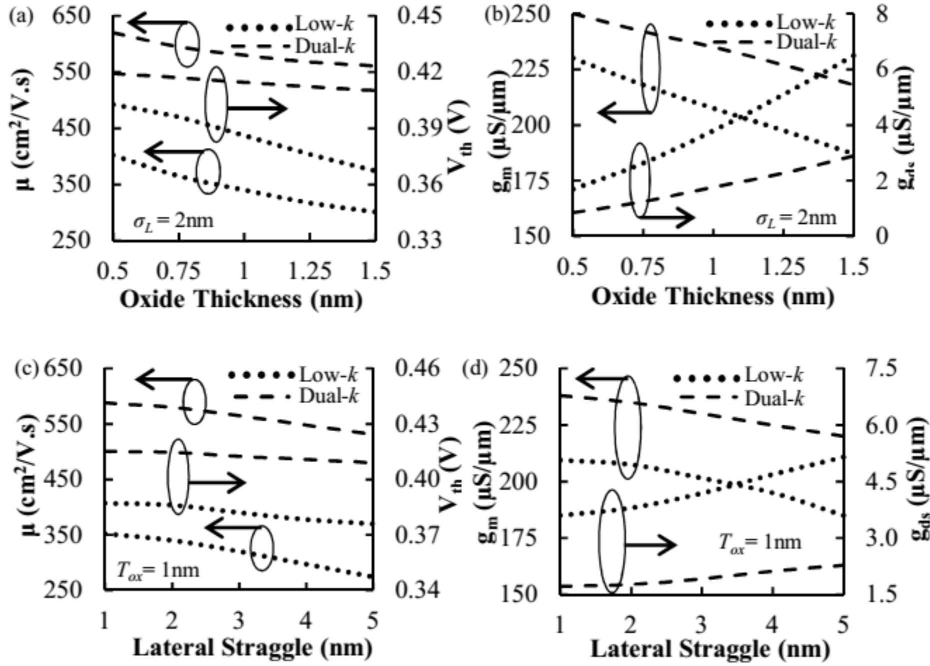

Fig. 4.10. Variation of (a) mobility and V_{th} (b) g_m and g_{ds} of N-FinFET with T_{ox} (c) mobility and V_{th} (d) g_m and g_{ds} of N-FinFET with σ_L of S/D profile.

Fig. 4.10 (a) shows the variation in V_{th} and μ of both conventional low-*k* and dual-*k* FinFET with thickness of gate dielectric T_{ox} at a constant lateral straggle σ_L = 2nm (X_j ~ 9nm). It is observed that, variations in V_{th} and μ with T_{ox} of dual-*k* FinFET are much lesser as compared to low-*k* FinFET. This is attributed to improvements in V_{th} and μ of dual-*k* FinFET by 43mV and 86% at T_{ox} = 1.5nm against the improvements of 17mV and 54% at T_{ox} = 0.5nm, as compared to V_{th} and μ of low-*k* FinFET at corresponding T_{ox}. This translates into improvements in g_m (g_{ds}) by 17% (56%) at T_{ox} = 1.5nm and 9% (50%) at T_{ox} = 0.5nm as shown in **Fig. 4.10 (b)**. Improved and variation less g_m and g_{ds} are two

important factors that translate into better A_{DM}, A_{CM} and CMRR at circuit level [205]. **Fig. 4.10 (c)** shows the variation in V_{th} and μ of both low-*k* and dual-*k* FinFET with σ_L of S/D doping profile. The σ_L is varied from 1nm to 5nm corresponding to junction depth X_j of ~5nm to ~22nm. The improvement in V_{th} (μ) of dual-*k* FinFET is 34mV (94%) at σ_L = 5nm and 27mV (67%) at σ_L = 1nm as compared to V_{th} (μ) of low-*k* FinFET at corresponding σ_L. This translates into improvements in g_m (g_{ds}) by 19% (56%) at σ_L = 5nm and 13% (52%) at σ_L = 1nm as shown in **Fig. 4.10 (d)** which, in turn, minimizes variations in g_m and g_{ds} at device level.

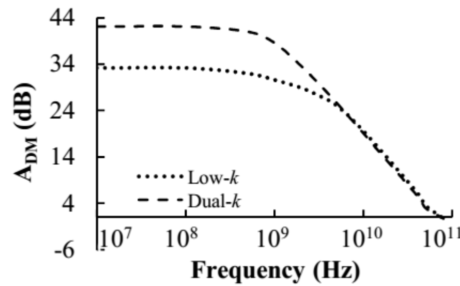

Fig. 4.11. Gain vs. frequency variation of single stage OTA circuit.

Fig. 4.11 shows the frequency response of single stage OTA circuit at 10μA/μm bias current. It is observed that, the unit gain bandwidths of both low-*k* and dual-*k* FinFET based OTA are 78GHz and 72GHz respectively, whereas, 3dB bandwidths are close to 1.1GHz and 0.85GHz, respectively. Negligible reduction in bandwidth of dual-*k* FinFET based OTA is attributed to increase in overall capacitance due to use of high-*k* inner dielectric spacer at underlap section of the device. Nevertheless, higher transconductance tend to reduce the effect of higher capacitance, thereby, producing almost similar bandwidth as compared to low-*k* FinFET based OTA. In the following two sub-sections, we have shown the effect of spatial variations in T_{ox} and σ_L on the analog FOM of single stage OTA. A common mode signal of 10mV peak-to-peak has been applied to analyse common mode gain (A_{CM}).

4.4.1 Spatial Variations in Transistors M1 and M2

Fig. 4.12 shows variations in crucial analog figures of merit (FOM) such as differential mode gain (A_{DM}), common mode gain (A_{CM}) and common mode rejection ratio (CMRR) of both low-*k* and dual-*k* FinFET based OTA with respect to variations in T_{ox} and σ_L of input transistor M1. For ± 0.5nm variation in T_{ox} of M1, it is observed that, maximum variations in A_{DM} and A_{CM} of low-*k* and dual-*k* FinFET based OTA are -5.2dB (-1.1dB) and +28.2dBm (+30.6dBm), respectively, as shown in **Fig. 4.12 (a)**.

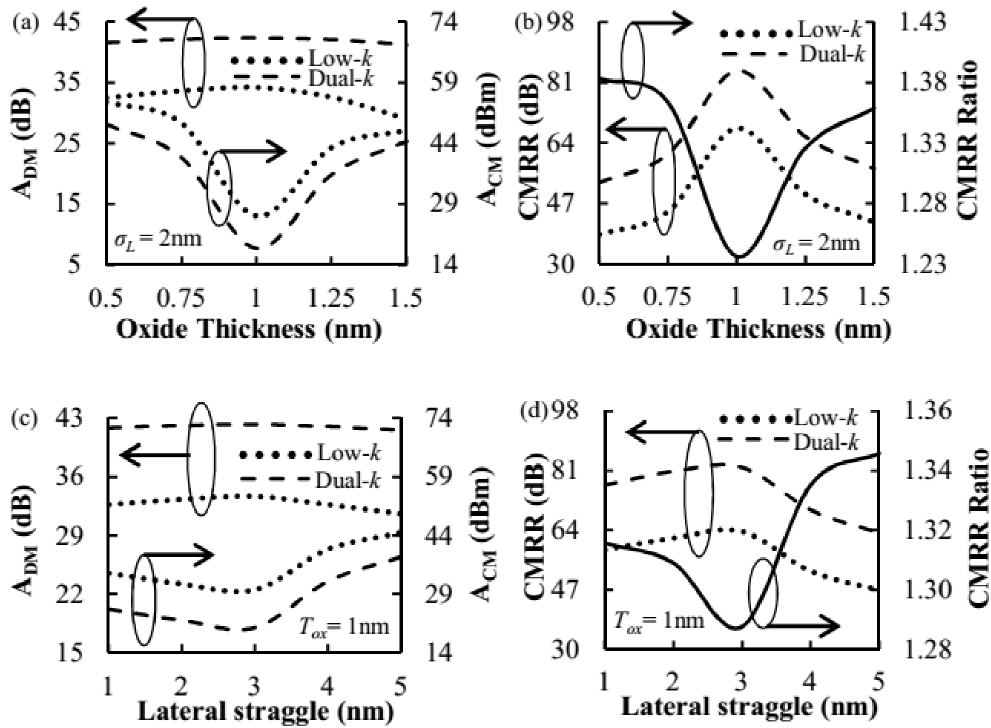

Fig. 4.12. Variation of (a) A_{DM}, A_{CM} (b) CMRR and CMRR Ratio of OTA with ± 0.5nm variation in T_{ox} of M1. Variation of (c) A_{DM}, A_{CM} (d) CMRR and CMRR ratio of OTA with ± 2nm variation in σ_L of S/D profile of M1.

Negligible increase in A_{CM} of dual-*k* FinFET based OTA can be attributed to the fact that the change in current ΔI_{D1} is multiplied by $(1/g_{m3}) \parallel (1/g_{ds3})$ yields $\Delta I_{D4} = g_{m4}\,[(1/g_{m3}) \parallel (1/g_{ds3})]\,\Delta I_{D1}$. This, in turn, produces additional current $\Delta I_{D4} - \Delta I_{D2}$ to flow through output

impedance of ($1/g_{ds4}$) [205]. As the output impedance of dual-k FinFET is higher but the change in current ΔI_{D1} is not significant, therefore, the additional factor of A_{CM} is negligible. Subsequently, the percentage improvements in CMRR of dual-k FinFET based OTA is much higher as compared to CMRR of low-k FinFET based OTA in presence of ± 0.5nm variation in T_{ox} of M1. CMRR ratio has been defined as the ratio of CMRR of dual-k and low-k OTA as shown in **Fig. 4.12 (b)**. It is observed that the maximum CMRR improvement is approximately 1.38 times (38%). **Fig. 4.12 (c)** plots variations in A_{DM} and A_{CM} of OTA for ± 2nm variation in σ_L of S/D profile of M1. It is observed that, maximum variations in A_{DM} and A_{CM} of low-k and dual-k FinFET based OTA are -2dB (-0.7dB) and +14.6dBm (+18dBm) respectively. In a similar fashion, the additional current $\Delta I_{D4} - \Delta I_{D2}$ flows through output impedance ($1/g_{ds4}$) and deteriorates A_{CM} of both low-k and dual-k FinFET based OTA. Subsequently, due to limited deterioration in A_{CM}, the percentage improvements in CMRR of dual-k FinFET based OTA is much higher as compared to CMRR of low-k FinFET based OTA in presence of ± 2nm variation in σ_L of S/D profile of M1. As shown in the CMRR ratio plot of **Fig. 4.12 (d)**, the maximum CMRR improvement is ~34%.

Fig. 4.13 (a) plots variations in A_{DM} and A_{CM} of OTA for ± 0.5nm variation in T_{ox} of M2. It is observed that, maximum variations in A_{DM} and A_{CM} of low-k and dual-k FinFET based OTA are -6.8dB (-2.2dB) and +27dBm (+31.3dBm), respectively. The change in current ΔI_{D2} will directly result from T_{ox} change in M2 which also affect g_{ds2}. Subsequently, the difference between $\Delta I_{D4} - \Delta I_{D2}$ flowing through output impedance ($1/g_{ds4}$) will be larger. These two effects will lead to largest variation in A_{DM} of both low-k and dual-k FinFET based OTA. Nevertheless, due to limited variations in g_{ds2} and ΔI_{D2}, the dual-k spacer based OTA will experience lesser variation in A_{DM}. Subsequently, the percentage improvement in CMRR of dual-k spacer based OTA is maximum (40%), as

shown in **Fig. 4.13 (b)**. For ± 2nm variation in σ_L of S/D profile of M2, it is observed that maximum variations in A_{DM} and A_{CM} of low-*k* and dual-*k* FinFET based OTA are -3.5dB (-1dB) and +12dBm (+15.5dBm) respectively as shown in **Fig. 4.13 (c)**. Similarly, maximum percentage improvement in CMRR of dual-*k* spacer based OTA is ~35% as shown in **Fig. 4.13 (d)**.

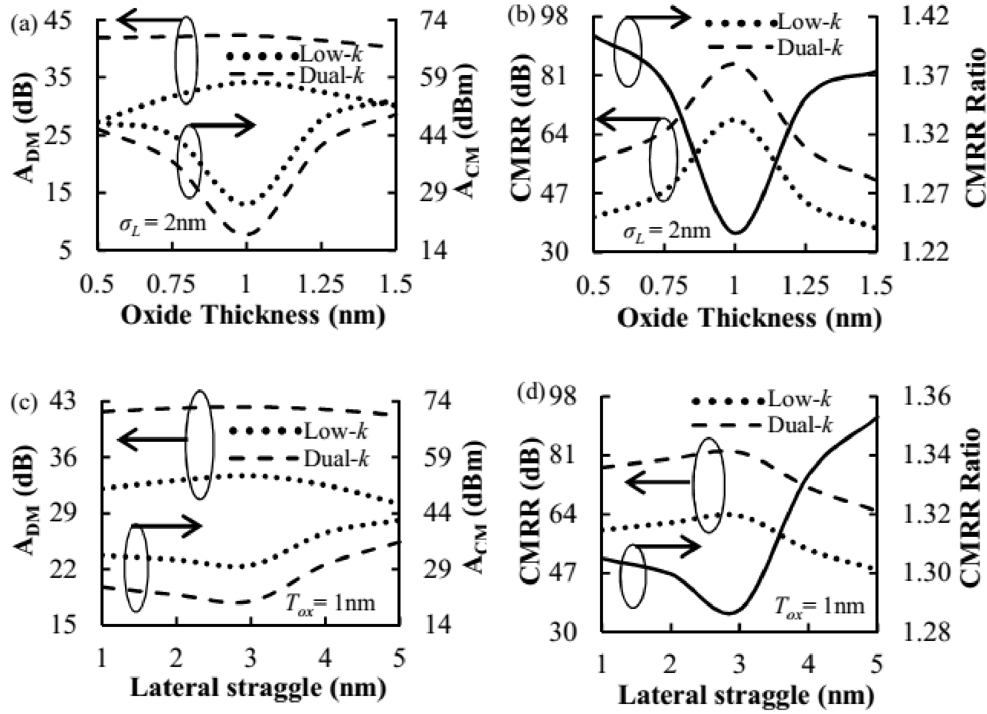

Fig. 4.13. Variation of (a) A_{DM}, A_{CM} (b) CMRR and CMRR Ratio of OTA with ± 0.5nm variation in T_{ox} of M2. Variation of (c) A_{DM}, A_{CM} (d) CMRR and CMRR ratio of OTA with ± 2nm variation in σ_L of S/D profile of M2.

4.4.2 Spatial Variations in Transistors M3 and M4:

For ± 0.5nm variation in T_{ox} of load transistor M3, it is observed that, maximum variations in A_{DM} and A_{CM} of low-*k* (dual-*k*) FinFET based OTA are -3.6dB (-0.7dB) and +23.7dBm (+26.8dBm), respectively, as shown in **Fig. 4.14 (a)**. Negligible increases in A_{CM} of dual-*k* FinFET based OTA can be attributed to limited variations in g_{m3}, g_{ds3} and, in turn, change in current ΔI_{D1} and ΔI_{D4}. As the output impedance ($1/g_{ds4}$) of dual-*k*

FinFET is higher but the change in current ΔI_{D4} is not significant, therefore, the additional factor of A_{CM} is negligible [205]. Subsequently, the percentage improvements in CMRR of dual-k FinFET based OTA is much higher as compared to CMRR of low-k FinFET based OTA in presence of ± 0.5nm variation in T_{ox} of load transistor M3. As shown in **Fig. 4.14 (b)**, the maximum CMRR improvement is observed to be ~32.5%. Similarly, maximum variations in A_{DM} and A_{CM} of low-k and dual-k FinFET based OTA are -1.2dB (-0.55dB) and +10.6dBm (+12.7dBm), respectively, for ± 2nm variation in σ_L of S/D profile of M3 as plotted in **Fig. 4.14 (c)**. This leads to maximum CMRR improvement of dual-k FinFET based OTA as ~32% as shown in **Fig. 4.14 (d)**.

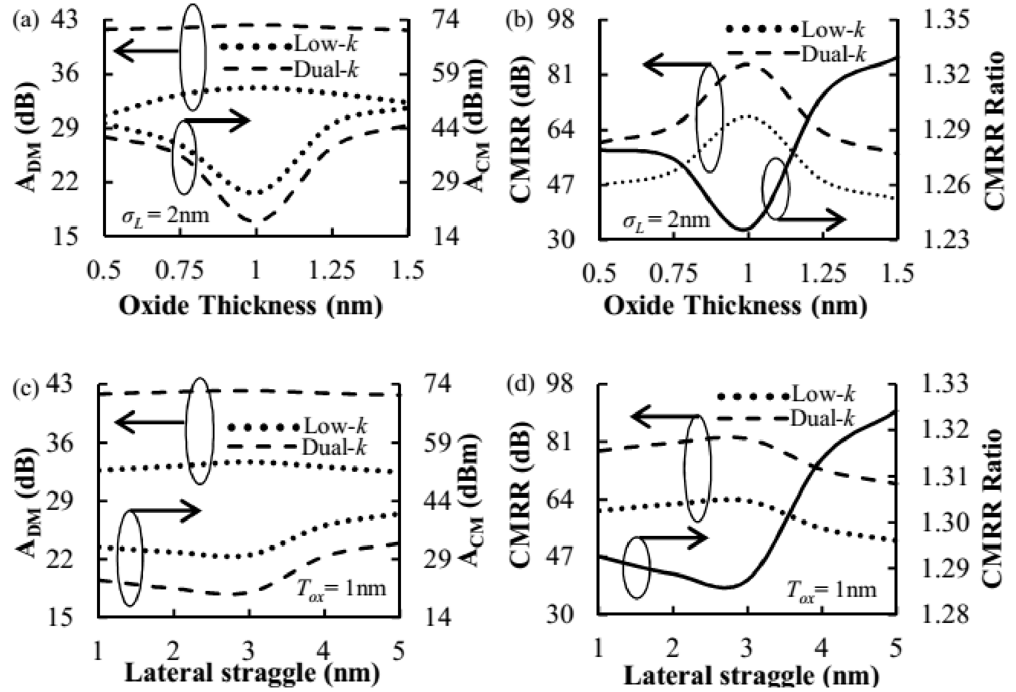

Fig. 4.14. Variation of (a) A_{DM}, A_{CM} (b) CMRR and CMRR Ratio of OTA with ± 0.5nm variation in T_{ox} of M3. Variation of (c) A_{DM}, A_{CM} (d) CMRR and CMRR ratio of OTA with ± 2nm variation in σ_L of S/D profile of M3.

Fig. 4.15 (a) plots variations in A_{DM} and A_{CM} of OTA for ± 0.5nm variation in T_{ox} of load transistor M4. It is observed that, maximum variations in A_{DM} and A_{CM} of low-k (dual-k)

FinFET based OTA are -3.5dB (-1.7dB) and +25.7dBm (+26.5dBm), respectively. Since load impedance ($1/g_{ds4}$) changes directly by ± 0.5nm variation in T_{ox}, variation in A_{DM} of both low-*k* and dual-*k* FinFET based OTA will be greater. Subsequently, limited deterioration in A_{CM} of dual-*k* FinFET based OTA leads to maximum CMRR improvements of 35.5% as shown in **Fig. 4.15 (b)**. Similarly, for ± 2nm variation in σ_L of S/D profile of load transistor M4, it is observed that, maximum variations in A_{DM} and A_{CM} of low-*k* and dual-*k* FinFET based OTA are -1.4dB (-0.6dB) and +11.5dBm (+12.2dBm) respectively. This leads to maximum CMRR improvements of ~36% as plotted in **Fig. 4.15 (d)**.

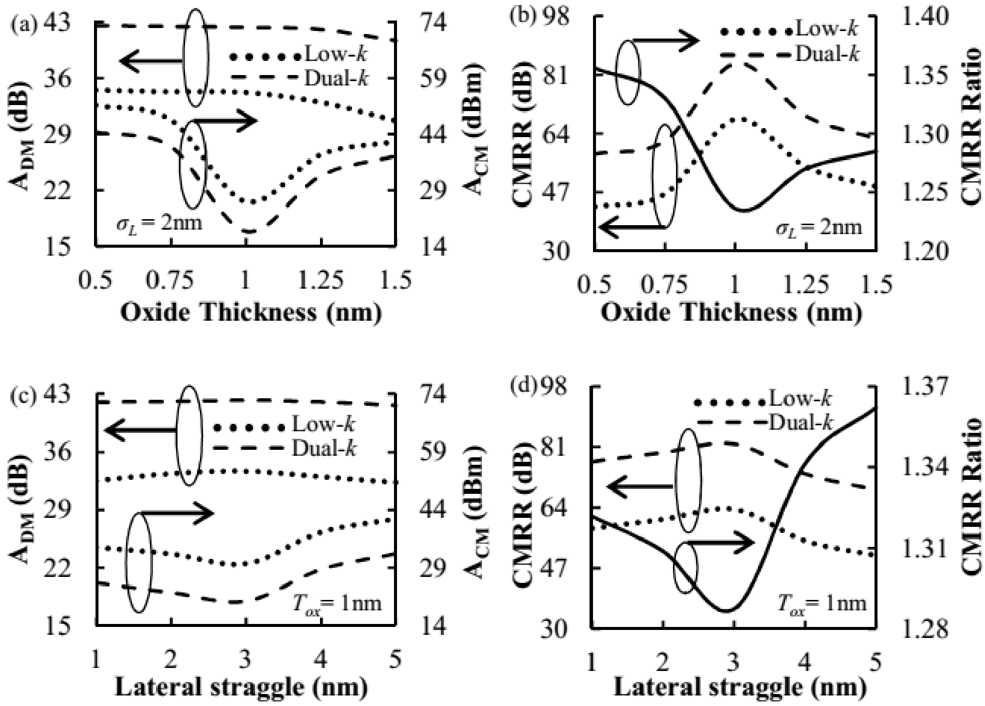

Fig. 4.15. Variation of (a) A_{DM}, A_{CM} (b) CMRR and CMRR Ratio of OTA with ± 0.5nm variation in T_{ox} of M4. Variation of (c) A_{DM}, A_{CM} (d) CMRR and CMRR ratio of OTA with ± 2nm variation in σ_L of S/D profile of M4.

4.4.3 Gate Length Scaling:

Source to drain lateral electric field spread into the channel region is enhanced as the gate length is scaled down in nanometer regime, leading to deterioration in gate electrostatic integrity. This, in turn, aggravates SCE and would result in reduced transconductance, increased output conductance and subsequent deterioration of crucial analog FOM. We observe g_m and g_{ds} of low-*k* underlap FinFET are deteriorated by 22% and 92% respectively, as the gate length is scaled down from 16nm to 12nm. On the other hand, deterioration of g_m and g_{ds} of dual-*k* FinFET are limited to 9% and 62%, respectively.

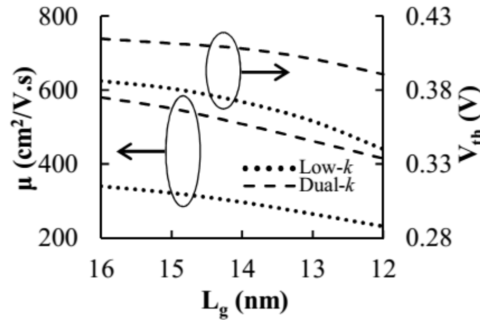

Fig. 4.16. Variation of (a) threshold voltage (b) mobility with gate length (L_g).

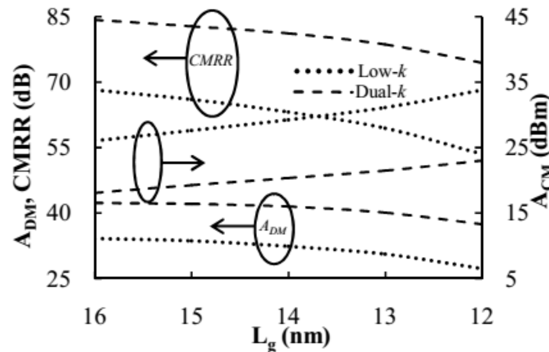

Fig. 4.17. Variation of A_{DM}, A_{CM} and CMRR of OTA with gate length scaling.

As discussed earlier, V_{th} and carrier mobility (μ) are two crucial parameters that determine these improved analog FOM at lower gate lengths. As shown in **Fig. 4.16**, due to of excellent *EI*, V_{th} and μ of dual-*k* FinFET are enhanced by 50.6mV and 45% at L_g = 12nm

as compared to low-*k* FinFET. Consequently, A_{DM}, A_{CM} and CMRR of dual-*k* FinFET based OTA are much better, when gate lengths are scaled from 16nm to 12nm. It is observed that, the deterioration in A_{DM}, A_{CM} and CMRR of low-*k* (dual-*k*) FinFET based OTA with gate length scaling are -7.2dB (-4.8dB), +7.7dBm (+4.9dBm) and -14.6dB (-9.8dB) respectively, as shown in **Fig. 4.17**. This is attributed to improvement in A_{DM}, A_{CM} and CMRR of dual-*k* FinFET OTA by 37%, 32% and 39% respectively at L_g = 12nm, as compared to the values extracted for low-*k* FinFET OTA. More importantly, due to excellent *EI*, the fluctuations in V_{th}, μ and analog FOM due to spatial variation in T_{ox} and X_j (or σ_L) of dual-*k* FinFET are controlled even at lower gate lengths. **Table 4.2** list out the maximum variations in analog FOM of low-*k* and dual-*k* FinFET OTA at L_g = 12nm, with spatial variations in T_{ox} (±0.5nm) and σ_L (±2nm) of individual transistors.

TABLE 4.2

MAXIMUM VARIATIONS IN ANALOG FOM OF OTA DESIGNED AT LG = 12NM

Attributes	Transistors	ΔA_{DM} (dB)		ΔA_{CM} (dB)		Max. *CMRR* Ratio
		Low-*k*	Dual-*k*	Low-*k*	Dual-*k*	
T_{ox}	M1	-6.4	-1.60	+31.5	+33.8	1.43
	M2	-8.7	-3.10	+29.6	+34.1	1.42
	M3	-5.1	-0.88	+27.4	+30.8	1.37
	M4	-5.8	-2.81	+28.8	+30.0	1.41
σ_L	M1	-3.3	-0.85	+16.8	+19.4	1.38
	M2	-4.9	-1.49	+15.2	+17.9	1.40
	M3	-2.4	-0.66	+14.5	+16.1	1.37
	M4	-2.9	-0.93	+13.9	+14.7	1.42

4.5 Summary:

The primary conclusions from this chapter are as follows:

Dual-*k* spacer based N/P-FinFETs are attractive option in designing circuitry for low power battery operated portable devices because of improved analog FOM. As compared to conventional low-*k* N/P-FinFETs, the improvements in FOM of dual-*k* N/P-FinFETs

are much better for devices with lower aspect ratio (~ 5) and fin width in the range of 0.5 L_g to 0.7L_g, a fact that is crucial in designing circuitry at this compact low power environment. More so, for a constant fin height, the FOM of dual-*k* N/P-FinFETs are considerably higher and posses lesser variation to fin width and oxide thickness, thereby improving the lithographic limitations at process level. The improvement in analog FOM is better at lower σ_L because of better screening of gate side wall fringing fields via undoped/lowly doped underlap portion near gate edges. This requirement of undoped/lowly-doped underlap portion can be achieved by providing sufficient underlap extension length and/or adopting better annealing techniques. Nevertheless, dual-*k* N/P-FinFETs are capable of providing excellent voltage gain with almost same f_T and f_{max} even at σ_L = 7nm. Secondly, improved and less variable g_{ds} to W_{fin}, T_{ox} and σ_L is more suitable for designing analog circuits such as current mirrors. We further observe that reducing *k* value of inner high-*k* spacer will linearly decrease the FOM improvements of dual-*k* FinFET as compared to low-*k* design.

Crucial analog FOM like A_{DM}, A_{CM} and CMRR of OTA largely depend upon spatial variations in critical transistor attributes T_{ox} and X_j. The variations in analog FOM is posing major threats to circuit designer, especially when the gate lengths are scaled into lower processing nodes because of unavoidable process limited steps. In this regard, dual-*k* spacer formation at underlap section of FinFET is immerging as an attractive option to improve the *EI* at lower gate lengths. Subsequently, improved and variation less V_{th}, μ and analog FOM can be achieved at device level which, in turn, improves circuit performance. It is observed, that the spatial variation of T_{ox} and X_j of input transistor M2 leads to worst case change in A_{DM} and A_{CM} of dual-*k* FinFET based OTA by -2.2dB and +31.3dBm at L_g = 16nm. This leads to CMRR improvements of 37% at this worst case condition as compared to CMRR of low-*k* FinFET OTA. Scaling the gate length to 12nm

results in -3.1dB and +34.1dBm deterioration in A_{DM} and A_{CM} of dual-*k* FinFET based OTA, whereas the CMRR improves to 42% at this condition as compared to CMRR of low-*k* FinFET OTA.

Chapter 5

Enhancing Low Temperature Analog Performance of Underlap FinFET

5.1 Introduction:

Recently, electronic circuits operating at low temperatures have found widespread applications in various fields such as, infrared detectors, space applications, medical diagnostics, satellite communications and terrestrial applications which include magnetic levitation transportation systems, cryogenic instrumentation and superconductive magnetic energy storage systems etc. [109], [167-168]. Basic building blocks of most of the aforementioned applications are elementary digital/analog circuits such as CMOS logic gates, reference circuits, current mirrors, SRAM cells, operational amplifiers etc. that are realized using advanced semiconductor devices. Gaensslen et al. [106] have discussed that it is not feasible for bipolar transistors to operate at low temperatures because of reduced current gain. On the other hand, operating at low temperatures, the field effect transistors (FETs) exhibit (i) improved switching speed due to an increase in the saturation velocity and enhanced carrier mobility resulting in reduced drain-to-source electrical resistance, (ii) improved reliability issues because of exponential reduction in various thermally activated process like diffusion, chemical reaction and electro-migration during fabrication, (iii) reduced thermal noise and, in turn, improved noise behavior and finally (iv) elimination of heating elements will lead to higher packing density. Moreover, lower power dissipation attributed to sharper turn-on characteristics of FETs and requirement of lower thermal energies can lead to aggressive scaling down of power supplies at low temperature environment [102-106].

Secondly, added incentive like high transconductance and velocity overshoot effects in NMOS devices have been reported by Sai-Halasz et al. [107], when the device is cooled to liquid

nitrogen temperature. These features will further allow device miniaturization at nano-scale regime. The performance is enhanced further by volume inversion effect reported in MOS transistor due to carrier confinement at the center of the channel rather than at Si-SiO_2 interface [24]. Higher current, reduced surface scattering and interface defects, higher carrier mobility and, in turn, higher transconductance are few added advantages of volume inversion effects in single as well as multigate MOSFETs [110]. It is reported that, channel thickness (t_{si}) optimization can avoid surface scattering from strong structural confinement, in order to target mobility enhancement [110]. Therefore, volume inversion and subband splitting are two main factors for mobility increase in optimally designed DG MOSFETs [24], [110]. More so, the volume inversion mobility of minority carriers of DG SOI MOSFET is improved substantially at low temperatures than at room temperature [108]. Reduced electric field in thin-fin devices also contributes to high mobility values. It is reported that the phonon scattering limited average surface mobility of trigate SOI MOSFET improves almost linearly as the temperature is lowered from 400K to 100K whereas, improvement in surface scattering limited average surface mobility is restricted when the temperature is lowered below 100K [111-112]. Yu et al. [169] have reported that, when the CMOS transistor is cooled to low temperature, it will have negligible impact on short channel effects such as DIBL, threshold voltage roll-off in addition to lower subthreshold leakage, enhanced threshold voltage and carrier mobility. Several authors have extended this argument to majority carrier devices in order to design high speed circuit because of superior carrier mobility and saturation velocity [113], [168], [170-171]. Therefore, further scaling down of device dimensions in low temperature environment is possible because of improved subthreshold slope, lower leakage current and improved gate electrostatic integrity [109], [112].

The analog performance of the device can be enhanced at low temperature environment because of improved threshold voltage (V_{th}) due to increase in fermi potential and improved carrier mobility due to volume inversion, subband splitting, reduced phonon scattering and

enhanced velocity overshoot effect at liquid nitrogen range (≥77K) [107-114]. Secondly, introduction of thicker high-*k* gate dielectric is a standard practice in sub 100nm regime to alleviate ever increasing tunneling current. Recently it is reported that this kind of thick high-*k* dielectric can exacerbate short channel effects (SCE) in double gate and multigate structures because of ease in propagation of source to drain (S/D) lateral electric fields resulting from reduced gate electrostatic control [140], [172]. The loss of gate electrostatic integrity (*EI*) can be restored up to certain extent when the temperature is lowered to 100K because of decrease in number of carriers with enough energy for impact ionization, resulting in raised conduction band energy, lower subthreshold leakage and hot carrier degradation [169]. Nevertheless, for thick high-*k* gate dielectric based multigate devices, it is still a challenge to control the ever-increasing lateral electric field as the gate length is scaled down to 16nm and beyond, posing serious threat for analog applications in all temperature ranges. The analog figures of merit (FOM) such as, g_m, g_{ds}, g_m /I_{ds}, A_{V0}, f_T and f_{max} are affected severely by gate length scaling even though temperature is lowered to 100K.

In this regard, dual-*k* spacer based underlap FinFET is emerging as a strong contender because of better screening of virtually normal fringing field via inner high-*k* spacer, thereby controlling the lateral S/D electric field spread into the channel region and, in turn, improves performance and SCE immunity [20], [69-70]. The effective screening of dominant fringing field is enhanced with gate length scaling resulting in improved threshold voltage and channel carrier mobility. At low temperature environment, the pronounced increase in threshold voltage and channel carrier mobility of dual-*k* FinFET can be useful in improving the analog FOM further.

The primary contributions in this chapter are as follows:

1. Analysis of high-*k* gate dielectric based underlap FinFET for analog applications.
2. Analysis of dual-*k* spacer based underlap FinFET.
3. Addressing gate length scaling issues for analog domain.

This chapter is organized as follows. Section 5.2 covers the simulation method used. Analysis of conventional underlap FinFET under different gate dielectric material has been presented in Section 5.3. Section 5.4 gives insight into analog performance of dual-*k* underlap FinFET with variation in device temperature. Gate length scaling under different temperature is taken up in Section 5.5. Finally, the major conclusions are drawn in Section 5.6.

5.2 Simulation Setup:

This section of the chapter focuses on suitable device physics models that are taken up for simulation setup. Fin depended parasitics calculated from [44] and [65] are included in the TCAD mixed-mode sentaurus device simulator. Non stationary effects such as velocity overshoot are introduced by selecting suitable saturation velocity and empirical parameter β as per [193] and [194], to correctly couple the carrier transport phenomena at nanometer regime. Secondly, the impact ionization has been introduced by activating Okuto-Crowell model and carrier temperature dependent impact ionization model. The mobility models that are used in simulation setup comprises of (1) Philips unified mobility model that account, the temperature dependency, electron–hole scattering, screening of ionized impurities by charge carriers and clustering of impurities (2) Electron and hole high field saturation model that account, the actual mobility model, velocity saturation model and driving force model (3) Lombardi mobility model for normal field dependent mobility at Si-SiO_2 and Si-high-*k* interface, which also includes remote coulomb scattering and remote phonon scattering. Furthermore, MLDA quantization model, SRH recombination/generation model, band to band auger recombination and old slotboom bandgap narrowing phenomenon are also included in simulation setup [195]. Device specifications that are used for the analysis are: L_g = 16nm, L_{ext} = 24nm, $L_{sp,hk} = L_{ext}/6$, EOT = 1.1nm, σ_L = 2nm, W_{fin} = 8nm, AR = 5. SiO_2 as gate oxide with equivalent oxide thickness (EOT) of 1.1nm is used throughout the analysis except in section 5.3, where different dielectric materials such as Al_2O_3 (k = 9.5), $NdGaO_3$ (k = 22), $LaAlO_3$ (k = 24) and TiO_2 (k =

40) with EOT of 1.1nm are used. Temperature coefficient of dielectric constants of these materials are selected as +110 ppm/^{0}K (Al_2O3), +1250 ppm/^{0}K ($LaAlO_3$), +2600 ppm/^{0}K ($NdGaO_3$) and -24 ppm/^{0}K (TiO_2) [206-208]. Secondly, L_g is constant throughout the analysis except in last part of the study that addresses the scaling issues. The analog FOM is extracted at I_{ds} = 10 $\mu A/\mu m$ keeping constant drain to source voltage V_{ds} = 1.1V.

5.3 Variation of Gate Dielectric Constant:

This section analyses analog performance of conventional underlap FinFET designed using different gate dielectric materials. Use of thick high-*k* gate dielectric can exacerbate SCE and deteriorates gate electrostatic integrity because of ease in propagation of source to drain lateral electric fields [140], [172]. Chen et al. [140] have reported that the conduction band energy is lowered by an amount of ζkT due to use of high-*k* gate dielectric, where the parameter ζ depends upon device geometry and dielectric of gate material.

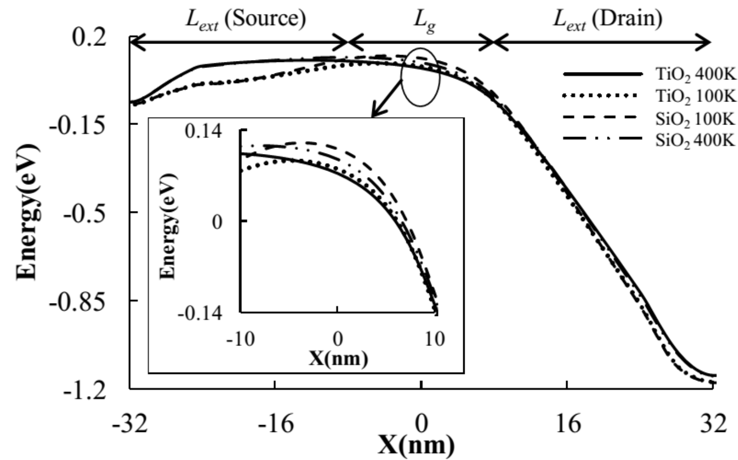

Fig. 5.1 . Variation of conduction band energy as a function of lateral direction (X) for various gate dielectric based underlap FinFETs. Simulated with V_{ds} = 1.1V and V_{gs} = 0.4V.

As the temperature is lowered to 100K there will be a decrease in the number of carriers with enough energy for impact ionization, resulting in a raised conduction band energy, lower subthreshold leakage and hot carrier degradation [169]. **Fig. 5.1** shows the variation of

conduction band energy (CBE) within the device with lateral distance (X) for different gate oxide material. As can be seen the conduction band energy of SiO_2 based N-FinFET is improved as the temperature is lowered to 100K. For high-*k* gate dielectric, on the other hand, reduction in *EI* is more dominant than decrease in number of carriers. Therefore, the improvement in conduction band energy at the centre of the channel is negligible as the temperature is lowered to 100K. Consequently, with increase in dielectric constant of gate oxide, there will be pronounced barrier lowering at low temperature as shown in **Fig. 5.1**.

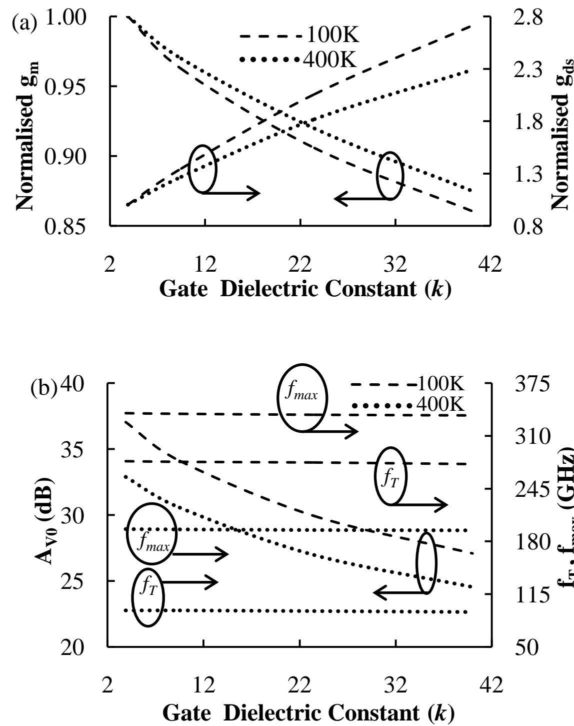

Fig. 5.2. Variation of (a) Normalised g_m and g_{ds} (b) A_{V0}, f_T and f_{max} of conventional underlap N-FinFET with gate dielectric constant (*k*).

Pronounced barrier lowering due to loss of gate electrostatic integrity will deteriorate the analog performance of the device. **Fig. 5.2 (a)** plots normalised g_m and g_{ds} with respect to dielectric constant *k* of gate oxide where, the g_m and g_{ds} are normalised to the extracted value of SiO_2 gate oxide based N-FinFET. It is observed that both g_m and g_{ds} are deteriorated with an increase in the dielectric constant *k* of gate oxide. As predicted, the deterioration is more pronounced at 100K temperature range. Therefore at 100K, we observe almost 10dB drop in

intrinsic gain (A_{V0}) as opposed to 8.3dB drop at 400K when k is varied from 3.9 (SiO_2) to 40 (TiO_2). **Fig. 5.2 (b)** plots the analog FOM of N-FinFET with varying dielectric constant k of gate oxide. The f_T and f_{max} will improve at low temperature because of a steep increase in the mobility and, in turn, transconductance. However, we observe that increasing k will result in almost constant f_T and f_{max} (slightly decreasing) for all temperature ranges, because of lower gate capacitance resulting from lesser screening of longitudinal electric field of thicker gate dielectric.

5.4 Analysis of Dual-*k* Spacer Based Underlap FinFET:

The digital performance of underlap FinFET operating in strong inversion is enhanced because of gate fringe induced barrier lowering (GFIBL) effect [68]. However, operating in low/moderate inversion regime, the conduction band energy can be raised by opting dual-k spacer design in underlap section of FinFET. This would enhance the analog performance of the underlap FinFET because of shift in source to drain lateral electric field from gate edge towards drain which will raise the threshold voltage and carrier mobility at the centre of the device. We observe that the shift in lateral electric field is pronounced as the device is cooled down to 100K temperature range. **Fig. 5.3** shows the conduction band energy of both low-k and dual-k based design at temperature range of 100K and 400K. As can be seen, the improvement in conduction band energy of dual-k design is much better when the device is cooled to 100K. It is also observed that at 100K, the conduction band energy of both low-k and dual-k FinFETs are low at source side of the device as compared to the energy at 400K. This will not aggravate the SCE of the device under study, as the lateral electric field is controlled at gate edge toward drain side of the device. Secondly, the minimum potential point still lies near the centre of the channel (X = 0nm) as can be observed from **Fig. 5.3**. Lowering of conduction band energy at source side of the device might pose serious concern for extremely scaled devices with smaller gate length and/or smaller extension length, where the source side conduction band energy can

possibly affect the minimum potential point of channel. Due to presence of higher conduction band energy and subsequently minimum potential point at the centre of the channel, the device under study posses higher threshold voltage (V_{th}) for both low-*k* and dual-*k* FinFETs when cooled down to 100K as shown in **Fig. 5.4 (a)**. This will certainly improve immunity of the device to SCE, by suppressing off current of the device. In addition to V_{th}, the carrier mobility (μ) at center of the channel extracted at $I_{ds} = 10\ \mu A/\mu m$, is also included in **Fig. 5.4 (a)**.

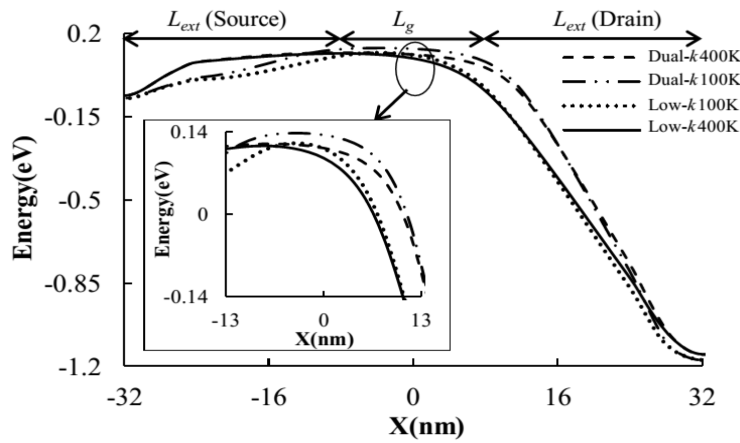

Fig. 5.3. Variation of conduction band energy as a function of lateral direction (X) for low-*k* and dual-*k* spacer based underlap FinFET. Simulated with $V_{ds} = 1.1$V and $V_{gs} = 0.4$V.

Due to a better gate electrostatic integrity, the V_{th} of dual-*k* FinFET is improved by ~20mV at 100K as compared to low-*k* design. This improvement is restricted to ~12mV at 400K. We also observe ~81% improvement in carrier mobility of dual-*k* FinFET at 100K against ~60% at 400K as compared to low-*k* FinFET. Improvement in mobility at lower temperature may be attributed to enhanced volume inversion, subband splitting, velocity overshoot effect and reduced phonon scattering [107-114]. For a constant current, combined improvement in carrier mobility and V_{th} will enhance the transconductance (g_m) of the device [205]. Subsequently, we investigate the g_m/I_{ds} ratio which is a measure of transconductance generation efficiency of the device [21], [157]. **Fig. 5.4 (b)** represents g_m/I_{ds} with respect to normalised drain currents ($I_{ds}/(W_g/L_g)$) at different temperature range. It is observed that, lowering temperature to 100K

will enhance the percentage improvement in g_m/I_{ds} ratio.

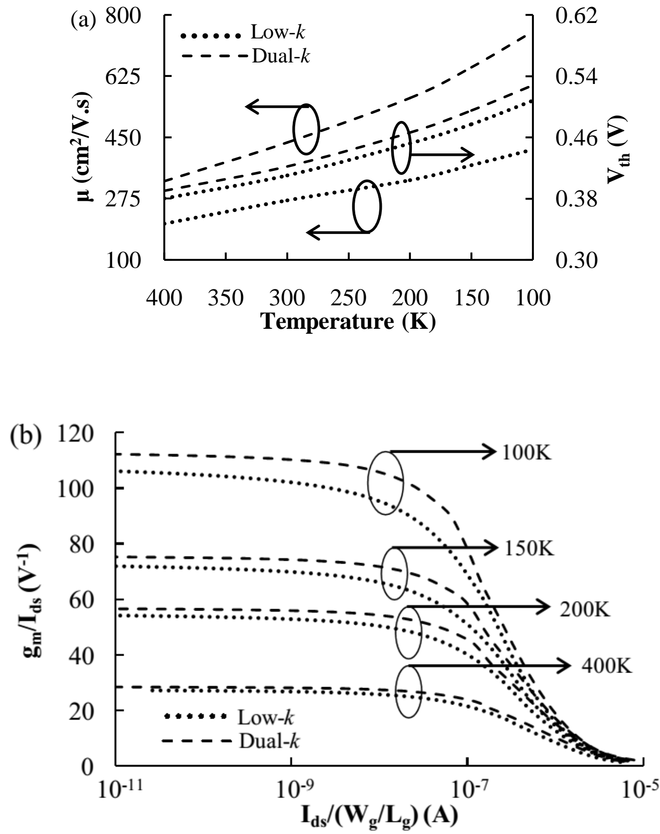

Fig. 5.4. Variation of (a) mobility and threshold voltage with temperature (b) g_m/I_{ds} ratio with respect to normalised drain current $I_{ds}/(W_g/L_g)$. The V_{th} is extracted by second derivative method.

Crucial analog figures of merit (FOM) such as A_{V0}, f_T and f_{max} are extracted at I_{ds} = 10 $\mu A/\mu m$ targeting weak/moderate inversion regime of operation as shown in **Fig. 5.5**. Due to an improved conduction band energy, the percentage improvement in g_m, g_{ds} and, in turn, A_{V0} of dual-*k* FinFET is enhanced at 100K. This improvement in A_{V0} is observed to be ~11.5dB at 100K as compared to ~7.3dB at 400K. It should be noted that, at I_{ds} = 10 $\mu A/\mu m$ the effect of source resistance resulting from lower g_{ds} of dual-*k* FinFET will have negligible effect on transconductance and, in turn, f_T and f_{max} of the device. Secondly, as the g_m of dual-*k* FinFET is enhanced due to improved mobility and V_{th}, it is observed that the f_T and f_{max} are improved by 10GHz and 9GHz respectively at 100K.

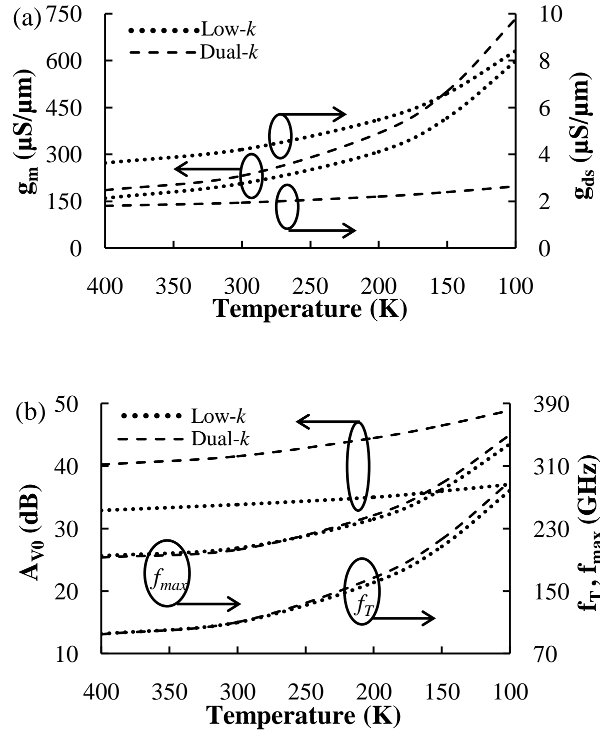

Fig. 5.5. Variation of (a) g_m and g_{ds} (b) A_{V0}, f_T and f_{max} of N-FinFET with temperature.

5.5 Gate Length Scaling Issues:

Scaling down of gate length in nanometer regime will enhance the source to drain lateral electric field penetration into the channel region, thereby deteriorating the gate electrostatic integrity. This would result in reduced transconductance and increased output conductance would deteriorate crucial analog FOM such as A_{V0}, f_T and f_{max}. At 400K temperature range we observe g_m and g_{ds} of low-*k* underlap FinFET are deteriorated by 24% and 96% as the gate length is scaled down from 16nm to 10nm, respectively. On the contrary, due to excellent *EI*, the deterioration in g_m and g_{ds} of dual-*k* underlap FinFET are limited to 6.5% and 67% respectively. This would translate into ~10.5dB improvement in A_{V0} at 10nm gate length as compared to ~7.3dB improvement at L_g = 16nm. Reduction in f_T and f_{max} of both low-*k* and dual-*k* design is limited with gate length scaling because of reduced gate capacitances. More so, the improvements in f_T and f_{max} of dual-*k* design as compared to low-*k* design are enhanced at

lower gate lengths because of limited g_m and g_{ds} deterioration. **Fig. 5.6** plots the analog FOM of low-*k* and dual-*k* underlap FinFET with gate length scaling at 400K temperature range.

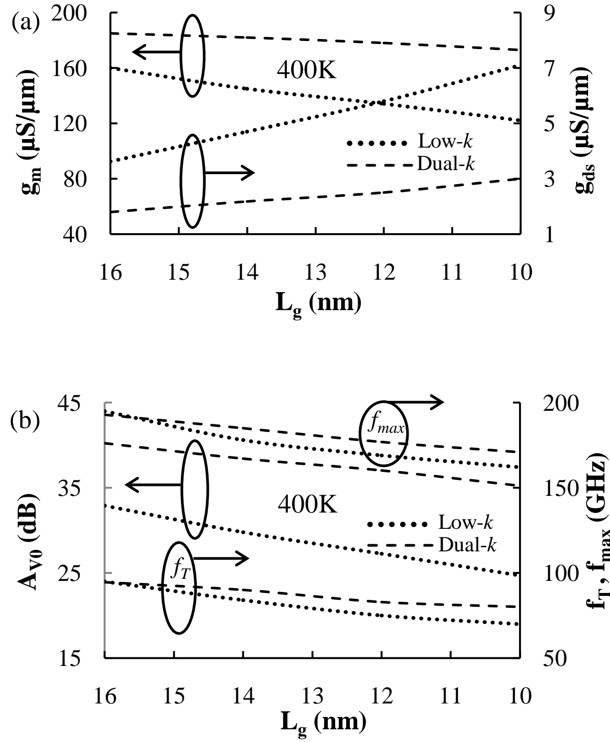

Fig. 5.6. Variation of (a) g_m and g_{ds} (b) A_{V0}, f_T and f_{max} of N-FinFET with gate length (L_g) at 400K.

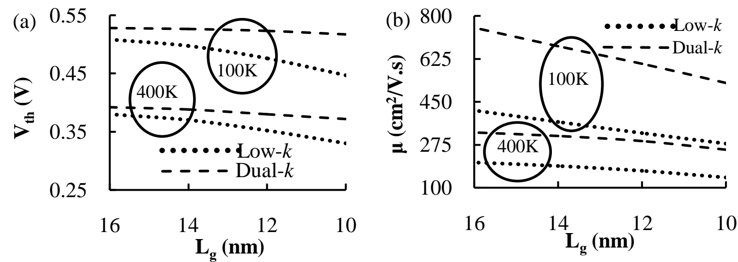

Fig. 5.7. Variation of (a) threshold voltage (b) mobility with gate length (L_g). The V_{th} is extracted by second derivative method.

As discussed in earlier section, threshold voltage and carrier mobility are two crucial parameters that determine the improved analog FOM of dual-*k* FinFET at L_g = 10nm. We observe that, V_{th} and carrier mobility of dual-*k* FinFET at 400K are enhanced by 42mV and 81% at L_g = 10nm as compared to low-*k* FinFET as shown in **Fig. 5.7**.

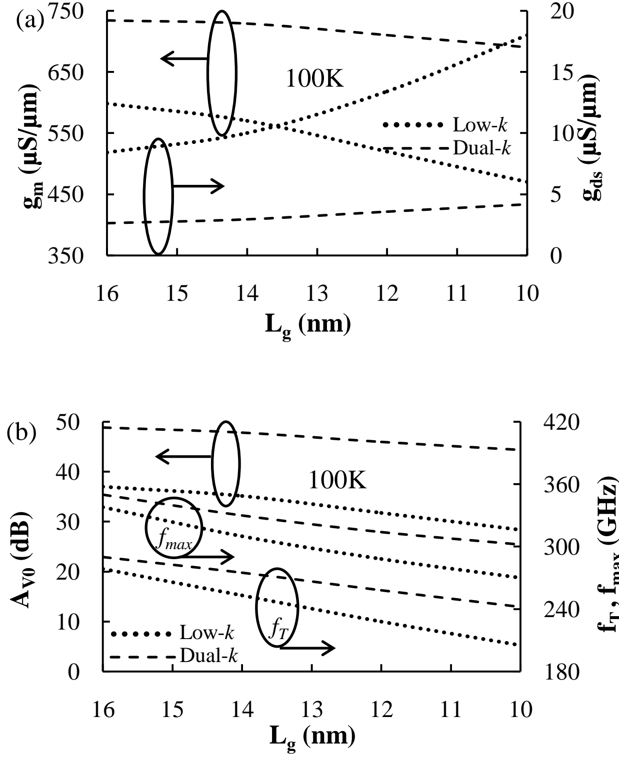

Fig. 5.8. Variation of (a) g_m and g_{ds} (b) A_{V0}, f_T and f_{max} of N-FinFET with gate length (L_g) at 100K.

More importantly, as the temperature is lowered down to 100K we observe that these two factors are improved by 70mV and 88% at same gate length. As stated earlier, higher mobility can be due to enhanced volume inversion, subband splitting, velocity overshoot effect and reduced phonon scattering [107-113]. Whereas, higher threshold voltage can be attributed to an increase in the fermi potential, low leakage current, reduced latchup susceptibility and improved gate electrostatic integrity [109], [168-169] at lower temperature and lower gate lengths. Therefore, at 100K temperature range and L_g = 10nm, we observe overwhelming improvement in g_m and g_{ds} of dual-*k* underlap FinFET as compared to low-*k* underlap FinFET as shown in **Fig. 5.8(a)**. Consequently, we observe ~16dB improvements in A_{V0} at 10nm gate length as compared to ~11.5dB improvement at L_g = 16nm as shown in **Fig. 5.8(b)**. More importantly, due to excellent g_m and g_{ds}, the capacitances offered from higher dielectric inner spacer of dual-*k* underlap FinFET are mitigated to a large extent. This results in lesser

reduction in f_T and f_{max} with gate length scaling at 100K temperature range. At 10nm gate length, the dual-*k* underlap FinFET has the capacity to offer A_{V0}, f_T and f_{max} of ~44dB, 242GHz and 302GHz respectively. As compared to low-*k* design the f_T and f_{max} are increased by 40GHz and 32GHz at this gate length.

5.6 Summary:

The primary conclusions from this chapter are as follows:

Use of high-*k* gate dielectric exacerbates short channel effects and gate electrostatic integrity, resulting in deterioration of analog FOM. As the temperature is lowered from 400K to 100K, the deterioration is more pronounced. On the other hand, dual-*k* spacer formation at underlap section of FinFET is an attractive option to improve the FOM. As the temperature is lowered to 100K, the percentage improvements in analog FOM of dual-*k* FinFET are enhanced further because of improvement in mobility and threshold voltage. Higher mobility can be due to enhanced volume inversion, subband splitting, velocity overshoot effect and reduced phonon scattering. Whereas, higher threshold voltage can be attributed to increase in fermi potential, low leakage current, reduced latchup susceptibility and improved gate electrostatic integrity at lower temperatures. Secondly, scaling down the gate length of dual-*k* FinFET to 10nm is feasible at 100K temperature range, which can target A_{V0}, f_T and f_{max} of ~44dB, 242GHz and 302GHz respectively. Considering the fact that at L_g = 10nm, A_{V0} of low-*k* FinFET is merely 25dB and 28dB at 400K and 100K respectively, the device scaling of dual-*k* FinFET to this gate length is still an attractive option. Therefore, dual-*k* underlap FinFET would pose as a serious contender among multigate MOSFETs for circuit design at compact low power and low temperature environment.

Chapter 6

Analytical Modelling of Dual-*k* Spacer Based Double Gate (DG) Underlap FinFET

6.1 Introduction:

Surface potential modeling is one approach to model the underlap FinFET behavior. However, the potential modelling in underlap FinFET is not straight forward as is the case in double gate MOSFET. This is because of gate fringing field effects in underlap region. Therefore, the potential distribution is different for overlap and underlap regions [125]. Since underlap surfaces are not equipotential surfaces, therefore, the fringing fields are solved self-consistently with the surface potential using Poission equation. Young et al. [173] have discussed that the mobile charge term in Poisson equation can be ignored for subthreshold potential modeling with acceptable error. This will help in determining subthreshold behavior such as threshold voltage and subthreshold slope with minimum computation overheads. Parabolic potential distribution along vertical direction is most widely used assumption for developing the model [173-176]. The coefficients of the parabolic potential distribution are determined from boundary condition and continuity of electric flux at front and back Si-SiO_2 interface. In case of symmetric structure, the front and back surface potential are equal. After obtaining the parabolic potential distribution function, the Poisson equation can be solved to obtain the front surface potential. The electric flux continuity expressions in case of underlap region is different from that of overlap region, since the effective oxide thickness between gate side wall and Si-SiO_2 interface is not constant due to fringing fields. The fringing field can be modeled using a conformal mapping technique [125-126]. Thereafter, the fringing field can be solved self-consistently with the surface potential using Poisson equation.

Fig. 6.1 shows the schematic of dual-*k* spacer based DG underlap FinFET where ε_h (high-*k*) and ε_l (low-*k*) are two dielectric constants of underlap sections. Available analytical model [125], [127] of underlap DG device cannot be directly applied to dual-*k* spacer based DG underlap device because of change in electric field line path between two different dielectric interfaces (ε_h and ε_l) of underlap sections. Secondly, use of inner high-*k* spacer will result in enhanced bunching of electric field lines near gate edges of underlap section. For modeling of region II/IV and I/V, this effect will change the effective gate heights for the elliptical field lines, emanating from gate edge and diverging at ε_h-ε_l interface. Therefore, to model this kind of dual-*k* spacer based DG underlap FinFET, we have divided the S/D underlap portion into two sub-sections so that underlap length $L_{un} = L_h+L_l$, where L_h is the length of the inner high-*k* spacer and L_l is the length of the outer low-*k* spacer as shown in **Fig. 6.1**.

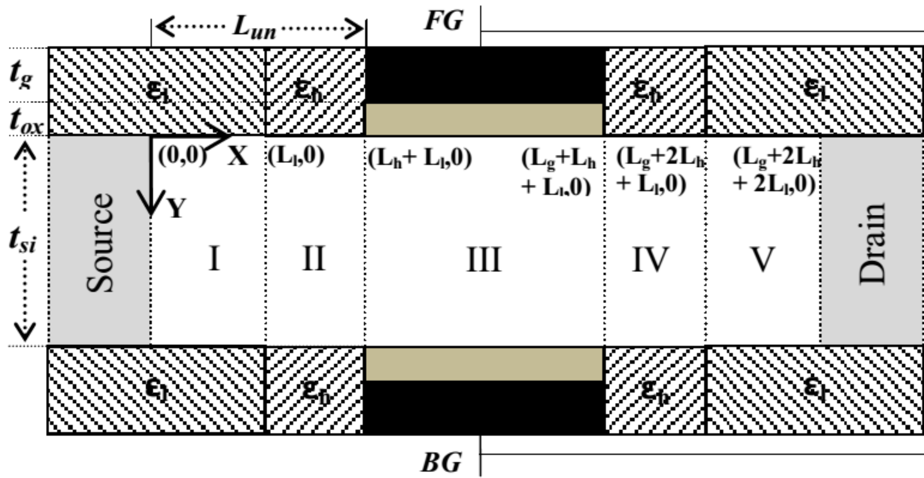

Fig. 6.1. Schematic of dual-*k* spacer based DG underlap FinFET.

Device specifications that are used for the analysis of nano-scale DG underlap FinFET design are: gate length (L_g) = 16nm, high-*k* extension length (L_h) = 2nm, low-*k* extension length (L_l) = 2nm, oxide thickness (t_{ox}) = 1nm, gate height (t_g) = 15nm, channel thickness (t_{si}) = 8nm, channel doping (N_a) = 10^{16} cm^{-3}. Furthermore, important device parameters like ε_h, L_h and t_{ox} are varied to validate our model as well as to deduce an expression for optimum L_h length.

Modelling of electric field lines in underlap section can be carried out by considering the continuity of electric flux at the ε_h-ε_l interface [177]. This will help in deriving overall flux density expressions of field lines from gate edge to silicon surface. Using the flux density expressions, the continuity equations and parabolic potential expressions in channel region, we can deduce the Poisson's equations in Si-SiO_2 interface. Subsequently, the Poisson's equations can be solved for surface potential expressions by Taylor series method and can be suitably converted to their body potential expressions as explained by Bansal et al. [125]. After deducing body potential expressions of all five regions of dual-*k* spacer based DG underlap FinFET, a compact potential model can be derived by application of suitable boundary conditions. The minimum potential point of the channel region gives us the inversion condition required to derive the threshold voltage of the device. Using the threshold voltage model, the drain current in linear and saturation region can be deduced by following the approach as suggested by Suzuki et al. [128]. Furthermore, since DG structure is a parallel combination of two transistors, Matthiessen's rule has been adopted to compute effective mobility in channel that suffers from both surface roughness and phonon scattering [128].

In addition, since lateral electric filed is normally much larger in saturation region of operation of device, effects like impact ionization and parasitic BJT effects have to be included while modeling conduction current in this region [129]. More so, the electric field in saturation region increases exponentially with gate length scaling and so is the impact ionization current and resulting parasitic BJT. However, these effects will not be present before onset of saturation. Therefore, modeling of linear region is straight forward where impact ionisation and parasitic BJT effects can be neglected. More importantly, as the device dimensions are scaled down to nano-meter regime, the non local effects such as channel length modulation [130], velocity overshoot effect [131] and drain induced barrier lowering (DIBL) [132] become more prominent in deciding transistor currents [133]. Out of which velocity overshoot is one of the most crucial issue where the electron velocity overshoots from its saturation value for a time

period shorter than its energy relaxation time and, in turn, impact the drive current and transconductance of the device [107], [180-182]. Reddy et al. [133] have pointed out that, as the channel length is scaled below 150nm, the electric filed will increase at a higher rate with pronounced increase in velocity overshoot effect. Therefore, while modeling linear and saturation drain currents these non-local effects are required to be introduced in the models.

The transconductance and output conductance are derived from the slope of I_{DS}-V_{DS} and I_{DS}-V_{GS} curve. Finally, the intrinsic DC gain is obtained from transconductance and output conductance ratio. The effect of inner high-*k* spacer over output conductance, transconductance and intrinsic gain is studied via analytical model that matches well with TCAD sentaurus device simulation results [195] for a range of inner high-*k* dielectric constant, high-*k* spacer length and oxide thickness.

In particular, this chapter makes the following contributions:

1) To the best of authors' knowledge, for the first time a compact analytical model for this kind of double dielectric spacer based underlap FinFET has been deduced that considers the change in the electric field line path between these two different dielectric spacers;

2) The effect of ε_h, L_h and t_{ox} on the electric field line path has been studied in order to exploit its impact on device performance;

3) A surface potential model is derived using the electric field analysis within underlap region of the device;

4) A compact threshold voltage model is formulated using the derived potential model that considers most of the design parameters to show the robustness of the proposed model;

5) Drain current model of linear and saturation region is deduced using this threshold voltage and including major non-local effects such as channel length modulation,

velocity overshoot, DIBL and secondary effects such as impact ionization and parasitic BJT effects;

6) Finally, the analog FOM such as output conductance (g_m), transconductance (g_{ds}) and intrinsic gain (A_{V0}) are extracted from the slope of I_{DS}-V_{DS} and I_{DS}-V_{GS} curve.

The rest of this chapter has been organized as follows. In Section 6.2, we have deduced an elliptical field line model of underlap section that includes the change in electric field lines in spacers. Section 6.3 deals with generating a potential model of the dual-*k* spacer based underlap FinFET. The potential model is further extended to develop a compact threshold voltage model in Section 6.4. Linear and saturation region drain currents are modeled in Section 6.5. These current models are further used for calculation of g_m, g_{ds} and A_{V0} in Section 6.6 which is further validated by variation of inner high-*k* dielectric constant, high-*k* spacer length and oxide thickness. Finally, Section 6.7 summarizes the chapter.

6.2 Elliptic Field Line model:

Modeling of section I and V is complicated because the elliptic electric field lines passes through two different dielectrics, high-*k* (ε_h) dielectric adjacent to gate edge and low-*k* (ε_l) dielectric at outer underlap section, before terminating at S/D ends as shown in **Fig. 6.2 (a)**. The field lines mapping are shown in **Fig. 6.2 (b)** where, the dotted lines corresponds to $\varepsilon_h = \varepsilon_l$ and continuous lines corresponds to $\varepsilon_h > \varepsilon_l$. Larger portion of field lines will terminate near to gate edges with increase in ε_h, resulting in reduced effective gate height (P_1) at ε_h-ε_l interface. Considering the field lines originating from the gate edge makes an angle θ with the normal at ε_h-ε_l interface, we write the continuity of electric flux at this interface as [177]:

$$\varepsilon_h E_h \cos\theta = \varepsilon_l E_l \cos\phi \tag{6.1}$$

$$E_h \sin\theta = E_l \sin\phi \tag{6.2}$$

where, E_h and E_l are field lines at high-k and low-k underlap section, respectively and ϕ is the diverging field angle at ε_h-ε_l interface.

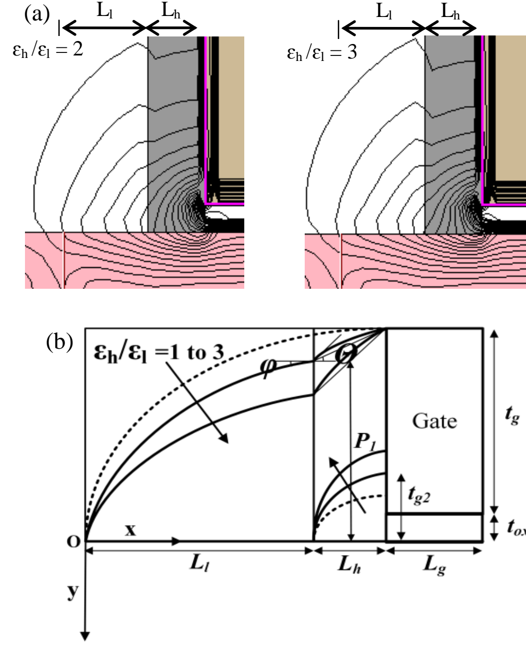

Fig. 6.2. (a) TCAD Simulated electric field lines through ε_h-ε_l interface (b) Electric field line mapping of dual-k spacer based DG underlap FinFET.

Reduction in height of P_1 with increase in ε_h will increase the incident angle θ at the ε_h-ε_l interface. Resulting θ_1 $(>\theta)$ is required to be calculated from the electric field lines originating from point (L_h+L_l, t_g+t_{ox}). Starting with an initial approximation that the diverging field angle ϕ_o for any ε_h to be equal and terminating at (0, 0) we write θ_1 as:

$$\theta_1 = \tan^{-1}[(\varepsilon_h/\varepsilon_l)\tan(\phi_o)] \tag{6.3}$$

where, using the equation of ellipse at (x -L_h-L_l, y) with minor and major axis being L_h+L_l and t_g+t_{ox}, respectively ϕ_o is calculated from the tangent at $x = L_l$ as:

$$\phi_0 = \tan^{-1}\left[\frac{L_h}{\sqrt{1-e_0^2}\sqrt{(L_h+L_l)^2-L_h^2}}\right] \tag{6.4}$$

e_0 is the eccentricity of the elliptic field line from point (L_h+L_l, -t_g-t_{ox}) to (0, 0) calculated as:

$$e_0 = \sqrt{1-[(L_h+L_l)/(t_g+t_{ox})]^2} \tag{6.5}$$

Now we write the expression for P_1 as:

$$P_1 = t_g + t_{ox} - L_h \tan(\theta_1) \tag{6.6}$$

Since the equation of incident field lines are unpredictable, we assume that, traversing from (L_l,0) to (0,0) will change the incident angle linearly from 90^0 to θ_1 at ε_h-ε_l interface. Therefore, the incident angle θ as a function of x is written as:

$$\theta = \theta_1 + \left(x \frac{(\pi/2) - \theta_1}{L_l} \right) \tag{6.7}$$

From which the final divergence angle ϕ can be written as:

$$\phi = \tan^{-1}\left[(\varepsilon_l / \varepsilon_h) \tan\theta \right] \tag{6.8}$$

6.3 Potential model:

For potential modeling we have assumed the parabolic potential distribution along the vertical direction as [173-176]:

$$\psi_i(x, y) = a_i(x) + b_i(x) y + c_i(x) y^2 \tag{6.9}$$

where a_i (x), b_i (x) and c_i (x) are to be determined using boundary conditions and continuity of electric flux at the S_i-spacer interface and ε_h-ε_l interface [177] as:

$$\psi_i(x,0) = \psi_f(x) = a_i(x) \tag{6.10}$$

$$\psi_i(x, t_{si}) = \psi_b(x) = a_i(x) + b_i(x) t_{si} + c_i(x) t_{si}^2 \tag{6.11}$$

$$E_h = \frac{\left(V'_{GS} - \psi_{\text{int}}(x) \right)}{L_{arch}} \tag{6.12}$$

$$E_l = \frac{\left(\psi_{\text{int}}(x) - \psi_f(x) \right)}{L_{arcl}} \tag{6.13}$$

where, L_{arch} and L_{arcl} are arc length of inner high-*k* and outer low-*k* spacer, $\psi_f(x)$ is potential at silicon front surface and $\psi_{\text{int}}(x)$ is potential at ε_h-ε_l interface. $V'_{GS} = V_{GS} - V_{fb}$, V_{GS} is the applied gate potential, V_{fb} is the flat band voltage. Finally, we write the overall flux density expression of field lines from gate edge to silicon surface as:

$$\varepsilon_h E_h \cos\theta = \frac{\left(V'_{GS} - \psi_f(x)\right)}{\frac{L_{arch}}{\varepsilon_h \cos\theta} + \frac{L_{arcl}}{\varepsilon_l \cos\phi}} \quad (6.14)$$

Considering the incident angle at S_i-spacer interface to be 90^0 as shown in **Fig. 6.2 (a)**, we write the continuity equation as:

$$\left.\frac{\partial\psi(x,y)}{\partial y}\right|_{y=0} = \frac{1}{\varepsilon_{si}\cos\theta}\frac{\left(\psi_f(x) - V'_{GS}\right)}{\frac{L_{arch}}{\varepsilon_h \cos\theta} + \frac{L_{arcl}}{\varepsilon_l \cos\phi}} = b_i(x) \quad (6.15)$$

Similarly, considering $\psi_{tsi}(x)$ as back surface potential we write

$$\left.\frac{\partial\psi(x,y)}{\partial y}\right|_{y=t_{si}} = \frac{1}{\varepsilon_{si}\cos\theta}\frac{\left(V'_{GS} - \psi_{t_{si}}(x)\right)}{\frac{L_{arch}}{\varepsilon_h \cos\theta} + \frac{L_{arcl}}{\varepsilon_l \cos\phi}} = b_i(x) + 2t_{si}c_i(x) \quad (6.16)$$

Using the symmetry condition $\psi_f(x) = \psi_{tsi}(x)$ and solving eq. (6.15) and (6.16) we get

$$c_i(x) = -b_i(x)/t_{si} \quad (6.17)$$

We have calculated the elliptical lengths of incident and diverging field lines from their eccentricity as [209]:

$$L_{arch} = \frac{L_h}{\sqrt{1-e_h^2}}E(e_h),\; L_{arcl} = \frac{(L_l - x)}{\sqrt{1-e_l^2}}E(e_l) \quad (6.18)$$

Where, complete elliptic integral $E(e_x)$ and the eccentricity e_h and e_l are calculated as:

$$E(e_x) = \int_0^{\pi/2}\sqrt{1 - e_x^2\sin^2\theta}\,d\theta \quad (6.19)$$

$$e_l = \sqrt{1 - \left(L_l/P_1\right)^2},\; e_h = \sqrt{1 - \left(L_h/t_{g_2}\right)^2} \quad (6.20)$$

The major axis can be expressed as: $t_{g_2} = \frac{L_h}{\sqrt{1-e_0^2}} + L_h\tan(\theta_1)$ (6.21)

The first part of R. H. S of eq. (6.21) is calculated from the concentric ellipse with eccentricity e_0 whereas the second part is an additional increase in height of major axis as shown in **Fig. 6.2 (b)**, considering the fact that more electric filed lines, from higher portion of gate side wall, are confined to inner high-*k* section with increase in ε_h.

For weak inversion operation the 2-D Poisson equation at Si-SiO_2 interface can be written as:

$$\frac{\partial^2\psi_i(x,y)}{\partial x^2} + \frac{\partial^2\psi_i(x,y)}{\partial y^2} = \frac{qN_a}{\varepsilon_{Si}} \quad (6.22)$$

where, N_a is channel concentration and potential distribution in channel ψ_i (x, y) can be deduced by putting the value of $a_i(x)$, $b_i(x)$ and $c_i(x)$ in eq. (6.9). Subsequently, eq. (6.22) can be re-arranged for the front surface potential (at y = 0) as:

$$\frac{d^2\psi_f(x)}{dx^2}+2\left(\frac{1}{t_{si}\varepsilon_{si}\cos\theta}\frac{V'_{GS}-\psi_f(x)}{\frac{L_{arch}}{\varepsilon_h\cos\theta}+\frac{L_{arcl}}{\varepsilon_l\cos\phi}}\right)=\frac{qN_a}{\varepsilon_{Si}} \tag{6.23}$$

No elementary solution to above differential equation exists. Therefore, neglecting the right hand side undoped body channel which is negligible in subthreshold condition [125] and using Taylor series approximation we get the surface potential equation in region I as:

$$\psi_1(x)=\psi_1(0)+x\psi_1'(0)+(1/2)x^2m_2(\psi_1(0)-V'_{GS})$$
$$+\frac{1}{6}x^3m_2\left(\frac{((\pi/2)-\theta_1)\tan(\theta_1)(\psi_1(0)-V'_{GS})}{L_l}-\frac{m_3(\psi_1(0)-V'_{GS})}{m_1}+\psi_1'(0)\right) \tag{6.24}$$

Where, $$m_1=\frac{\varepsilon_l E(e_h)L_h\sec(\theta_1)}{\varepsilon_h\sqrt{1-e_h^2}}+\frac{E(e_l)L_l\sqrt{\varepsilon_l^2\tan^2(\theta_1)+\varepsilon_h^2}}{\varepsilon_h\sqrt{1-e_l^2}} \tag{6.25}$$

$$m_2=\frac{2\varepsilon_l\sec(\theta_1)}{m_1 t_{\mathrm{si}}\varepsilon_{\mathrm{si}}} \tag{6.26}$$

and $$m_3=\frac{((\pi/2)-\theta_1)\varepsilon_l E(e_h)L_h\tan(\theta_1)\sec(\theta_1)}{\sqrt{1-e_h^2}\,\varepsilon_h L_l}$$

$$-\frac{E(e_l)\sqrt{\varepsilon_l^2\tan^2(\theta_1)+\varepsilon_h^2}}{\varepsilon_h\sqrt{1-e_l^2}}+\frac{((\pi/2)-\theta_1)\varepsilon_l^2E(e_l)\tan(\theta_1)\sec^2(\theta_1)}{\varepsilon_h\sqrt{1-e_l^2}\sqrt{\varepsilon_l^2\tan^2(\theta_1)+\varepsilon_h}} \tag{6.27}$$

The constants $\psi_1(0)$ and $\psi_1'(0)$ can be obtained by solving the boundary conditions. A similar expression can be obtained at region V with constants $\psi_5(2L_h+2L_l+L_g)$ and $\psi_5'(2L_h+2L_l+L_g)$ with $x=(x-(2L_h+2L_l+L_g))$.

Potential modeling of region II and IV is determined by solving the Poisson equation as explained in [125]

$$\psi_2(r_1)=c_3\left(1-\frac{r_1^2}{2}\right)+c_4\left(r_1-\frac{\alpha r_1^3}{6}\right)+V'_{GS} \tag{6.28}$$

$$\psi_4(r_2) = c_7\left(1-\frac{r_2^2}{2}\right)+c_8\left(r_2-\frac{\alpha r_2^3}{6}\right)+V'_{GS} \tag{6.29}$$

where, constants c_3, c_4, c_7, c_8 are calculated from boundary conditions. Whereas,

$$r_1 = \eta\frac{L_h+L_l-x}{t_{ox}} \tag{6.30}$$

$$r_2 = \eta\frac{x-(L_h-L_l-L_g)}{t_{ox}} \tag{6.31}$$

and $\eta = \left(\frac{t_{ox}}{L_{un}}\right)\sinh\left(\cosh^{-1}\left(\frac{t_{g2}}{t_{ox}}\right)\right)$ (6.32)

Similarly, modeling of region III is determined as [128]:

$$\psi_3(x) = c_5\,\mathrm{e}^{\frac{(x-L_{un})}{\lambda}}+c_6\,\mathrm{e}^{\frac{-(x-L_{un})}{\lambda}}-\frac{qN_a\lambda^2}{\varepsilon_{Si}}+V'_{GS} \tag{6.33}$$

where, natural length $\lambda = \sqrt{\frac{t_{\mathrm{ox}}t_{\mathrm{si}}\varepsilon_{\mathrm{si}}}{2\varepsilon_{\mathrm{ox}}}\left(\frac{\varepsilon_{\mathrm{ox}}t_{\mathrm{si}}}{4t_{\mathrm{ox}}\varepsilon_{\mathrm{si}}}+1\right)}$ (6.34)

Finally we convert the surface potential equation of all five regions to its body potential equation as explained in [125]

$$\psi_{bi}(x) = \psi_i(x)\left(\frac{\varepsilon_{\mathrm{ox}}t_{\mathrm{si}}}{4t_{\mathrm{ox}}\varepsilon_{\mathrm{si}}}+1\right)-\frac{V'_{\mathrm{GS}}\varepsilon_{\mathrm{ox}}t_{\mathrm{si}}}{4t_{\mathrm{ox}}\varepsilon_{\mathrm{si}}} \tag{6.35}$$

6.3.1 Boundary Conditions:

The final expressions for potential in all five regions (i.e., constants $\psi_1(0)$, $\psi_1'(0)$, c_3, c_4, c_5, c_6, c_7, c_8, $\psi_5(2L_h+2L_l+L_g)$ and $\psi_5'(2L_h+2L_l+L_g)$) are computed by applying the continuity of the potential and its lateral gradient as the boundary conditions between regions. The boundary conditions are as follows:

$$\psi_{b1}(0) = V_{bi} \tag{6.36}$$

$$\psi_{b1}(L_l) = \psi_{b2}(L_l) \tag{6.37}$$

$$\psi_{b2}(L_l+L_h) = \psi_{b3}(L_l+L_h) \tag{6.38}$$

$$\psi_{b3}(L_l + L_h + L_g) = \psi_{b4}(L_l + L_h + L_g) \quad (6.39)$$

$$\psi_{b4}(L_l + 2L_h + L_g) = \psi_{b5}(L_l + 2L_h + L_g) \quad (6.40)$$

$$\psi_{b5}(2L_l + 2L_h + L_g) = V_{bi} + V_{DS} \quad (6.41)$$

$$\left.\frac{d\psi_{b1}(x)}{dx}\right|_{x=L_l} = \left.\frac{d\psi_{b2}(x)}{dx}\right|_{x=L_l} \quad (6.42)$$

$$\left.\frac{d\psi_{b2}(x)}{dx}\right|_{x=L_l+L_h} = \left.\frac{d\psi_{b3}(x)}{dx}\right|_{x=L_l+L_h} \quad (6.43)$$

$$\left.\frac{d\psi_{b3}(x)}{dx}\right|_{x=L_l+L_h+L_g} = \left.\frac{d\psi_{b4}(x)}{dx}\right|_{x=L_l+L_h+L_g} \quad (6.44)$$

$$\left.\frac{d\psi_{b4}(x)}{dx}\right|_{x=L_l+2L_h+L_g} = \left.\frac{d\psi_{b5}(x)}{dx}\right|_{x=L_l+2L_h+L_g} \quad (6.45)$$

The computed constant values are as follows:

$$c_3 = c_5 + c_6 \quad (6.46)$$

$$c_4 = \left(\frac{t_{ox}}{\eta}\right) \times \left(\frac{c_6 - c_5}{\lambda}\right) \quad (6.47)$$

$$c_5 = \lambda\left(\frac{p_1 + p_2}{p_3 + p_4}\right) \quad (6.48)$$

$$c_6 = \frac{2n_3 t_{\mathrm{ox}}^2 \left(2h_2 L_l^3 - h_1^2 L_l^4 - 3\right) \times \left(V_{bi} e^{\frac{L_g}{\lambda}} + V_{bi} + V_{DS}\right)}{n_1\left(e^{\frac{2\mathrm{L_g}}{\lambda}} - 1\right) + \lambda n_2\left(e^{\frac{2\mathrm{L_g}}{\lambda}} + 1\right)} \quad (6.49)$$

$$c_7 = c_5\,\mathrm{e}^{\frac{L_g}{\lambda}} + c_6\,\mathrm{e}^{-\frac{L_g}{\lambda}} \quad (6.50)$$

$$c_8 = \frac{t_{ox}}{\eta}\frac{c_5\,\mathrm{e}^{\frac{L_g}{\lambda}} - c_6\,\mathrm{e}^{-\frac{L_g}{\lambda}}}{\lambda} \quad (6.51)$$

$$h_1 = \left(\frac{m_2}{2}\right) \quad (6.52)$$

$$h_2 = -\frac{h_1 m_3}{m_1} + \frac{\left((\pi/2) - \theta_1\right) h_1 \tan(\theta_1)}{L_l} \quad (6.53)$$

$$p_1 = -i_1 q_1\left(V_{bi} + \left(V_{bi} + V_{DS}\right)e^{\frac{L_g}{\lambda}}\right) - i_2 q_1\left(V_{bi} - \left(V_{bi} + V_{DS}\right)e^{\frac{L_g}{\lambda}}\right) \quad (6.54)$$

$$p_2 = i_1 q_1 V'_{\mathrm{GS}}\left(e^{\frac{L_g}{\lambda}} + 1\right) - i_2 q_1 V'_{\mathrm{GS}}\left(e^{\frac{L_g}{\lambda}} - 1\right) \quad (6.55)$$

$$p_3 = i_1\left(e^{\frac{L_g}{\lambda}} + 1\right) - i_3\left(e^{\frac{L_g}{\lambda}} - 1\right) \quad (6.56)$$

$$p_4 = i_1\left(e^{\frac{L_g}{\lambda}} - 1\right) - i_3\left(e^{\frac{L_g}{\lambda}} + 1\right) \quad (6.57)$$

$$q_1 = 2t_{\mathrm{ox}}^2\left(h_1^2 L_l^4 - 2h_2 L_l^3 + 3\right) \quad (6.58)$$

$$i_1 = \alpha\eta^2 L_h^3\left(h_1 L_l^2 + 1\right) + \alpha\eta^2 h_1 L_h^2 L_l^3 + 3\alpha\eta^2 L_h^2 L_l - 6L_h t_{\mathrm{ox}}^2\left(h_1 L_l^2 + 1\right) - 2h_1 L_l^3 t_{\mathrm{ox}}^2 - 6L_l t_{\mathrm{ox}}^2 \quad (6.59)$$

$$i_2 = -3\alpha\eta^2 h_1 \lambda L_h^2 L_l^2 - 2\alpha\eta^2 \lambda L_h L_l\left(h_1 L_l^2 + 3\right) + 6h_1 \lambda L_l^2 t_{\mathrm{ox}}^2 - 3\alpha\eta^2 \lambda L_h^2 + 6\lambda t_{\mathrm{ox}}^2 \quad (6.60)$$

$$i_3 = -i_2 + 12\lambda t_{\mathrm{ox}}^2 \quad (6.61)$$

$$\psi'_1(0) = \frac{1}{2t_{\mathrm{ox}}^3\left(h_1 L_l^2 + 1\right)}\left[2t_{ox}\alpha c_3 \eta^2 L_h + \mathrm{c}_4\left(\alpha\eta^3 L_h^2 - 2\eta\, t_{\mathrm{ox}}^2\right) - \psi_1(0)\left(2h_2 L_l^2 t_{\mathrm{ox}}^3 + 4h_1 L_l t_{\mathrm{ox}}^3\right)\right] \quad (6.62)$$

$$\psi'_5(2L_l + 2L_h + L_g) = \frac{1}{2t_{\mathrm{ox}}^3\left(h_1 L_l^2 + 1\right)}\left[-2t_{ox}\alpha c_7 \eta^2 L_h + c_8\left(2\eta t_{\mathrm{ox}}^2 - \alpha\eta^3 L_h^2\right) - 2h_2 V'_{\mathrm{GS}} L_l^2 t_{\mathrm{ox}}^3 - 4h_1 V'_{\mathrm{GS}} L_l t_{\mathrm{ox}}^3\right.$$

$$\left. + \psi_5\left(2L_h + 2L_l + L_g\right) \times \left(2h_2 L_l^2 t_{\mathrm{ox}}^3 + 4h_1 L_l t_{\mathrm{ox}}^3\right)\right] \quad (6.63)$$

$$n_1 = 2\alpha^2\eta^4 L_h^5 L_l\left(h_1^2 L_l^4 + 4h_1 L_l^2 + 3\right) + \eta^4 L_h^6\left(\alpha + \alpha h_1 L_l^2\right)^2 + 4\alpha\eta^2 L_h^3 L_l\left(h_1^2 L_l^4 + 4h_1 L_l^2 + 3\right) \times \left(3\alpha\eta^2\lambda^2 - 4t_{ox}^2\right)$$

$$+ \alpha\eta^2 L_h^4\left(\alpha\eta^2\left[3h_1\left(3h_1\lambda^2 + 2\right)L_l^4 + 9\left(2h_1\lambda^2 + 1\right)L_l^2 + h_1^2 L_l^6 + 9\lambda^2\right]\right.$$

$$\left. - 12\left(h_1 L_l^2 t_{\mathrm{ox}} + t_{\mathrm{ox}}\right)^2\right) + 24 L_h L_l t_{\mathrm{ox}}^2\left(h_1^2 L_l^4 + 4h_1 L_l^2 + 3\right)\left(t_{\mathrm{ox}}^2 - \alpha\eta^2\lambda^2\right)$$

$$+ 4L_h^2\left(t_{\mathrm{ox}}^2 - \alpha\eta^2\lambda^2\right) \times \left[9\left(h_1 L_l^2 t_{\mathrm{ox}} + t_{\mathrm{ox}}\right)^2 - \alpha\eta^2 L_l^2\left(h_1 L_l^2 + 3\right)^2\right]$$

$$+ 4t_{\mathrm{ox}}^4\left[3h_1\left(3h_1\lambda^2 + 2\right)L_l^4 + 9\left(2h_1\lambda^2 + 1\right)L_l^2 + h_1^2 L_l^6 + 9\lambda^2\right] \quad (6.64)$$

$$n_2 = 2\left(5\alpha^2\eta^4 L_h^4 L_l\left(h_1^2 L_l^4 + 4h_1 L_l^2 + 3\right) + 3\eta^4 L_h^5\left(\alpha + \alpha h_1 L_l^2\right)^2\right.$$

$$- 2\alpha\eta^2 L_h^3\left[12\left(h_1 L_l^2 t_{\mathrm{ox}} + t_{\mathrm{ox}}\right)^2 - \alpha\eta^2 L_l^2\left(h_1 L_l^2 + 3\right)^2\right]$$

$$-24\alpha\eta^2 L_h^2 L_l t_{ox}^2\left(h_1^2 L_l^4+4h_1 L_l^2+3\right)+12L_l t_{ox}^4\left(h_1^2 L_l^4+4h_1 L_l^2+3\right)\Big)$$

$$+4L_h t_{ox}^2\left[9\left(h_1 L_l^2 t_{ox}+t_{ox}\right)^2-\alpha\eta^2 L_l^2\left(h_1 L_l^2+3\right)^2\right] \tag{6.65}$$

$$n_3=\alpha\eta^2 L_h^2\left(h_1 L_l^3-3h_1\lambda L_l^2-3\lambda+3L_l\right)+\alpha\eta^2 L_h^3\left(h_1 L_l^2+1\right)+2L_h\left[\alpha\eta^2\lambda L_l\left(h_1 L_l^2+3\right)+3t_{ox}^2\left(h_1 L_l^2+1\right)\right]$$

$$-2t_{ox}^2\left(h_1 L_l^3-3h_1\lambda L_l^2-3\lambda+3L_l\right) \tag{6.66}$$

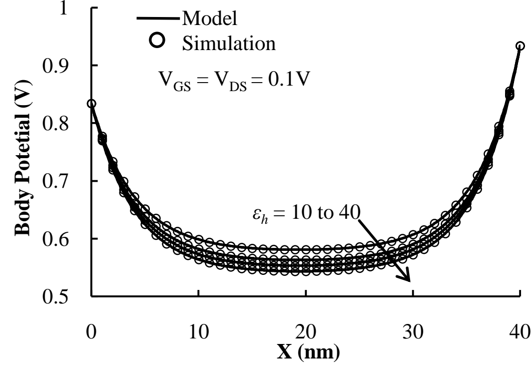

Fig. 6.3. Body potential (y = $t_{si}/2$) variation along the channel for different inner high- *k* spacer values.

Considering bandgap narrowing effect, the built in potential (V_{bi}) can be approximated as

$$V_{bi}=v_t\ln\left(N_a N_d/n_{i,eff}^2\right) \tag{6.67}$$

where, v_t is the thermal voltage and $n_{i,eff}=\sqrt{n_i^2 e^{\Delta E_g/kT}}$ [188]. The model predicted and TCAD device simulated body potential profiles are shown in **Fig. 6.3**. The reduction in potential profile with an increase in ε_h is attributed to the increase in conduction band energy with ε_h.

6.4 Threshold voltage model:

The minimum potential point $x_{min}=L_{un}+(\lambda/2)\ln(c_6/c_5)$ is calculated by equating

$$\partial\psi_{b3}(x)/\partial x=0 \tag{6.68}$$

The threshold voltage is defined as the gate voltage when the channel electron densities at the minimum potential point reach the channel doping density. i. e.

$$\left(n_i^2/N_a\right)e^{\left(\psi_{b3}(x_{min})/v_t\right)}=N_a \tag{6.69}$$

This yields the expression for threshold voltage as:

$$V_{th} = V_{fb} + 2\phi - \left(1 + \frac{C_{ox}}{4C_{Si}}\right) \times \left(c_5 e^{\frac{(x_{\min} - L_{un})}{\lambda}} + c_6 e^{\frac{-(x_{\min} - L_{un})}{\lambda}} - \frac{Q_{Si}}{2}\left(\frac{1}{4C_{Si}} + \frac{1}{C_{ox}}\right)\right) \tag{6.70}$$

where, $\phi = v_t \ln\left(\frac{N_a}{n_i}\right)$, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$, $C_{Si} = \frac{\varepsilon_{Si}}{t_{Si}}$, $Q_{Si} = qN_a t_{Si}$

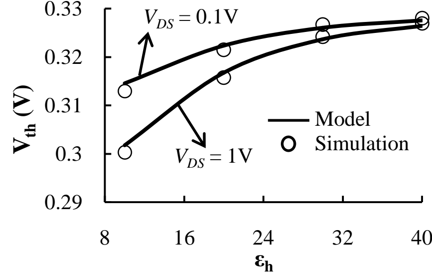

Fig. 6.4. Variation of V_{th} with ε_h for high and low V_{DS}.

As shown in **Fig. 6.4**, the threshold voltage (V_{th}) increases with an increasing ε_h. This is attributed to an increase in gate electrostatic integrity because of enhanced screening of gate side wall fringing fields, which effectively increases the V_{GS} requirement for creating inverted channel electron density. With an increase in the V_{DS}, the lateral electric field intrudes more into the channel region and reduces the V_{GS} requirement for creating inversion charges. However, due to pronounced increase in *EI* at higher ε_h, the effect of V_{DS} on threshold voltage variation is limited as shown in **Fig. 6.4**. This improved drain induced barrier lowering (DIBL), calculated as change in V_{th} with V_{DS}, plays a major role in deciding analog performance. The model predicted V_{th} and DIBL are in good agreement with TCAD simulation results extracted at 1.127 × (W/L_{eff}) µA [153].

6.5 Drain current model:

The linear and saturation drain current models of DG MOSFET can be derived using the proposed threshold voltage model. Secondly, the non-local effects such as channel length modulation [130], velocity overshoot [131] and DIBL [132] are required to be introduced in the current models. As the device dimensions are scaled in nanometer regime, these factors are

becoming more crucial in increasing current drive and transconductance of device [133]. Including all these effects, the linear ($I_{D,lin}$) and saturation ($I_{ch,sat}$) drain currents are given by [131-133]

$$I_{D,lin} = \left(\frac{2W\mu_{neff}C_{ox}}{\left(L_{eff} - l_d + \frac{V_{DS}}{E_C} \right)} + \lambda_a \frac{2WC_{ox}}{\left(L_{eff} - l_d \right)^2} \right) \times \left[\left(V_{GS} - V'_{th} \right) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \tag{6.71}$$

$$I_{ch,sat} = \left(\frac{2W\mu_{neff}C_{ox}}{\left(L_{eff} - l_d + \frac{V_{DS,sat}}{E_C} \right)} + \lambda_a \frac{2WC_{ox}}{\left(L_{eff} - l_d \right)^2} \right) \times \left[\left(V_{GS} - V'_{th} \right) V_{DS,sat} - \frac{1}{2} \left(V_{DS,sat} \right)^2 \right] \tag{6.72}$$

Where, the effective channel length (L_{eff}) is calculated as $L_{eff} = L_g + (2 \times L_{un})$. This is because the analysis is carried out at overdrive voltage (V_{GS}-V_{th}) of ≤ 200mV to target low/moderate inversion regime of operation [20], so that performance such as high gain of DG structure is explored. The pre-factor 2 before width W account for the fact that, the DG structure is a parallel connection of two transistors [128]. Width $W = 2h_{fin}+t_{si}$ [44], where fin height (h_{fin}) is the third dimension of the simulated device set as 1µm. $V'_{th} = V_{th}$ - DIBL and l_d is the channel length modulation factor as discussed in [130], [133]. $\lambda_a = 25\times10^{-5}$ cm^3/Vs accounts for velocity overshoot effect [131]. The critical electric field E_C at which electron velocity saturates is described in [128]. Whereas, saturation voltage ($V_{DS,sat}$) is given by

$$V_{DS,sat} = \frac{V_{GS} - V'_{th}}{1 + \left(V_{GS} - V'_{th} \right) / \left(L_{eff} E_C \right)} \tag{6.73}$$

Furthermore, the impact ionization and parasitic BJT effects are added to the final saturation current model to account for large lateral electric field at nano-scale devices [129]. Finally, the total drain current in saturation is written as:

$$I_{D,sat} = GI_{ch,sat} + HI_{CBO} \tag{6.74}$$

where, the parameters G, H and leakage current (I_{CBO}) are described in [129]. **Fig. 6.5** plots I_{DS}-

V_{DS} plots of the proposed model which is in good agreement with the TCAD simulation results.

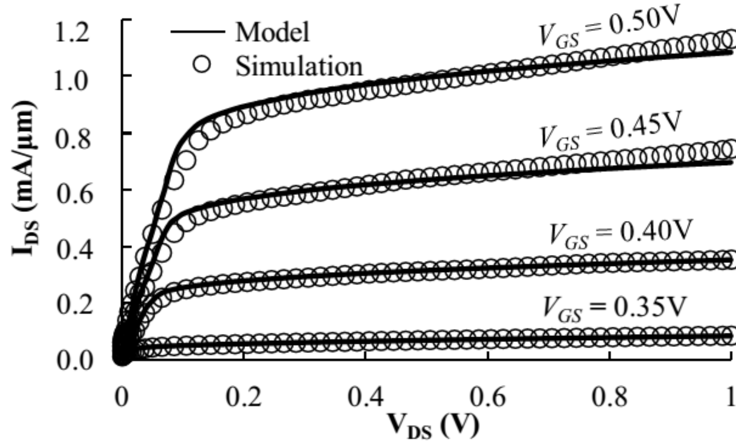

Fig. 6.5. I_{DS}-V_{ds} characteristics of DG underlap FinFET with ε_h =20.

6.6 Analog parameter extraction:

Fig. 6.6 (a) and **(b)** show the variation of g_{ds} and g_m with ε_h. The output conductance (g_{ds}) is extracted from the slope of I_{DS}-V_{DS} between V_{DS} = 0.5 V and V_{DS} = 1V at V_{GS} = 0.4V while the transconductance (g_m) is extracted from the slope of I_{DS}-V_{GS} between V_{GS} = 0.4 V and V_{GS} = 0.45V at V_{DS} = 1V for both model predicted and simulation value. The g_m and g_{ds} are expected to decrease at higher ε_h because of increase in threshold voltage. However, the intrinsic gain (A_{V0} = g_m/g_{ds}) will increase at higher ε_h because of pronounced decrease in g_{ds} [133]. **Fig. 6.6 (c)** plots A_{V0} with increase in ε_h. We observe ~10dB increase in A_{V0} when ε_h is varied from 10 to 40. We further validate our model by varying two important parameters L_h and t_{ox} as shown in **Fig. 6.7**. We observe that, improvement in V_{th} and, in turn, A_{V0} is limited after L_h = L_{un}/6 = 2nm. More so, with increase in L_h (> L_{un}/6), the cutoff and maximum oscillation frequency tend to deteriorate due to increase in gate capacitances. Therefore, L_h = L_{un}/6 is the optimum length to be considered while designing dual-*k* FinFET structure. Secondly, variation in A_{V0} with t_{ox} is almost linear as lower t_{ox} enhances better coupling of gate

side wall fringing fields, thereby increasing the gate electrostatic integrity and, in turn, analog FOM.

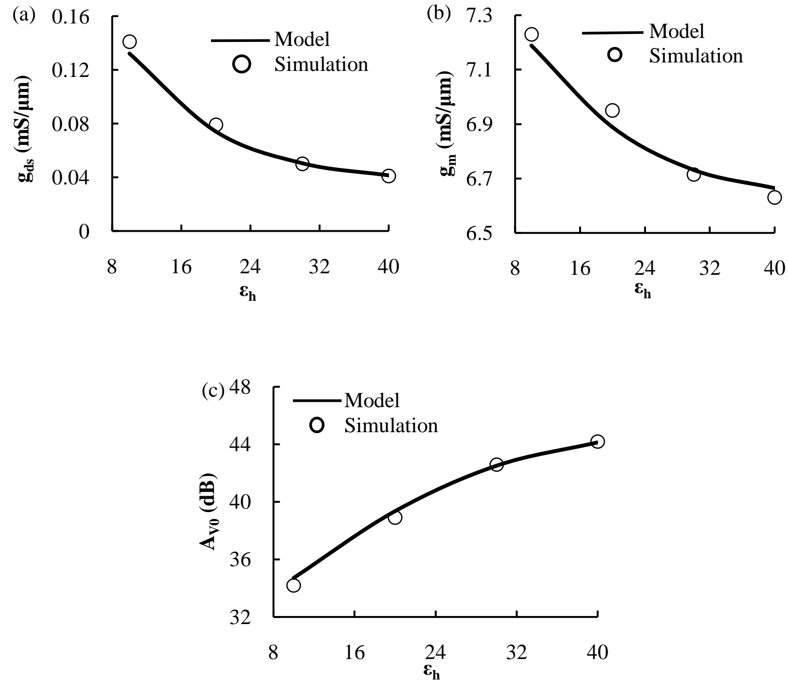

Fig. 6.6. Variation of (a) g_{ds} (b) g_m (c) A_{V0} with ε_h.

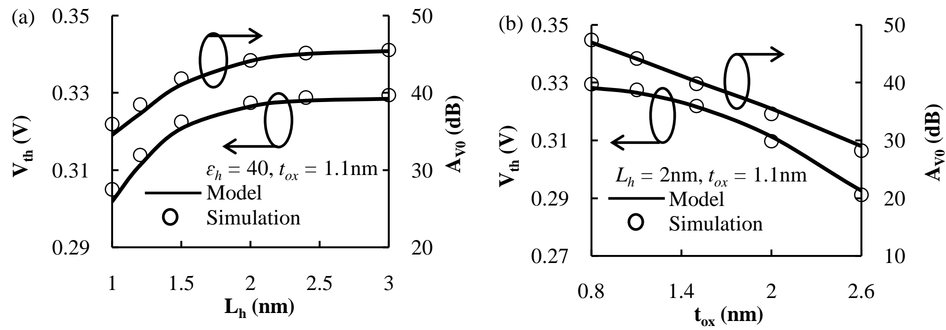

Fig. 6.7. Variation of V_{th} and A_{V0} with (a) L_h (b) t_{ox}.

6.7 Summary:

The proposed model captures well the effect of inner high-*k* spacer on change in electric field lines at low-*k*/high-*k* dielectric interface and its subsequent effect on potential profile of dual-*k* spacer based underlap FinFET. Due to better gate electrostatic integrity, the conduction band energy will increase and the minimum potential will be lowered with an increase in the

dielectric constant of inner high-*k* spacer. This, in turn, will increase the threshold voltage and reduce the effect of drain bias on threshold voltage variation. Subsequently, the short channel and analog performance of the device will be improved. The model matches well with TCAD device simulation [195] results with variation in crucial device dimensions such as, inner high-*k* spacer dielectric constant, inner high-*k* spacer length and gate oxide thickness. We observe that, the improvement in A_{V0} is almost linear with reducing gate oxide thickness whereas, the improvement is almost limited for $L_h > L_{un}/6$. Therefore, $L_h = L_{un}/6$ has to be considered as optimum length while designing dual-*k* FinFET structure.

Chapter 7

Analytical Modelling of DG MOSFET Considering Source/Drain Lateral Gussian Doping Profile

7.1 Introduction:

One of the most critical fabrication steps is rapid thermal processing following the high temperature annealing of dopant species in channel and source/drain region of the device. Rapid thermal processing is required for dopant activation process so that the desired electronic contribution from impurity ions are achieved and charge carriers can be effectively controlled by gate and channel bias voltages. In case of double gate and multigate MOSFETs, the gate electrostatic control is much better due to close proximity of multiple gates. This, in turn, controls the threshold voltage of the device without use of heavy channel doping and/or channel stop implants. Nevertheless, heavily doped raised source/drain structure is usually preferred to control the device parasitics so that the performance is not deteriorated [44]. With lightly doped channel, this kind of heavily doped source/drain dopant species can intrude more into the channel region when rapid thermal processing step following the high temperature annealing is performed to activate the dopant species. As the technology is scaled down into nano-meter regime, this kind of dopant spread into the channel region plays a major role in aggravating short channel effects (SCEs) and deteriorating performance of multigate MOSFETs.

Recent years has seen tremendous increase in advanced junction processes for ultra shallow junction formation at the cost of added process complexity. This is because; formation of ultra shallow junction (USJ) allows control of lateral electric field spread via dopant species into the channel region [134]. However, USJs are achieved by additional process complexity such as: defect formation and junction leakage, temperature control, equipment maturity, process control, cost effectiveness etc. [94-100]. Improvements in annealing techniques however,

promise formation of USJ from 20-30nm (σ_L ~ 5nm) [94-95] to ~ 11nm (σ_L ~ 2nm) [97]. **Fig. 7.1** shows secondary ion mass spectrometry (SIMS) doping profiles under different techniques.

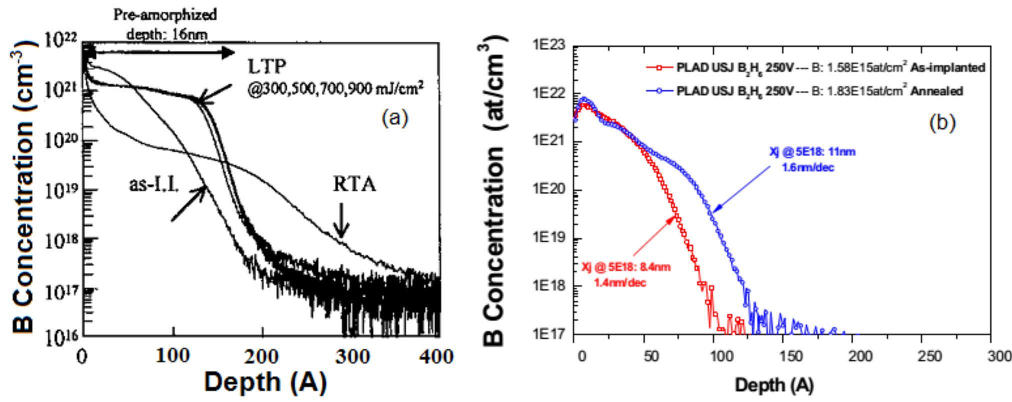

Fig. 7.1. SIMS profile showing dopant distribution (a) Shima et al. [94] (b) Gelpey et al. [97].

This envisages the inclusion of lateral S/D profile effect while deriving compact models for DG-MOSFET. Nevertheless, the exact computation involving gaussian like S/D profile is mathematically very complex. Therefore, instead of solving the potential equation involving gaussian term, we have approximated it by its absolute value at each point of the channel. For generating a compact model, the effect of S/D profile is introduced in terms of ionised dopant species, effective S/D ends and effective channel length calculation considering dopant degeneracy effects.

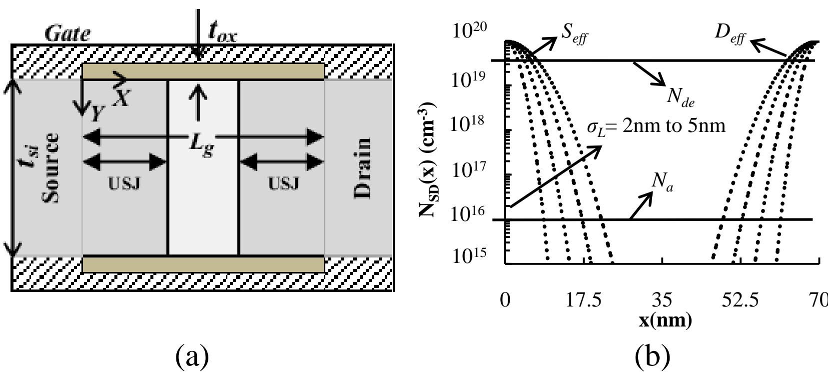

Fig. 7.2. (a) Schematic of DG-MOSFET (b) S/D Doping profile. L_g, t_{si} and t_{ox} are gate length, channel thickness and oxide thickness respectively.

Fig. 7.2 (a) shows the schematic of a DG MOSFET with non-zero lateral straggle (σ_L), where

USJ is formed in the channel region which is sufficiently away from S/D ends. The gaussian profile in the channel region is modeled as $N_{SD}(x) = N_{SD(p)} e^{-x^2/2\sigma_L^2}$ where, $N_{SD}(p)$ is the peak of gaussian profile, set as 1×10^{20} cm^{-3}. The gate work function is set as 4.6eV. **Fig. 7.2 (b)** shows various S/D gaussian profile corresponding to different σ_L. The degenerated doping value N_{de} is set as 2.7×10^{19} cm^{-3} in accordance with experimental results as explained by Morin et al. [187].

Subthreshold modeling of DG MOSFET is useful in deducing crucial parameters like threshold voltage, DIBL and subthreshold slope of the device. The mobile charge term in Poisson equation can be neglected to develop a simpler yet effective subthreshold potential model [173]. Parabolic potential distribution along vertical direction can be assumed for model development [173-176]. The coefficients of the parabolic potential distribution are determined from boundary conditions, continuity of electric flux at front and back Si-SiO_2 interface and effective source/drain end calculations. After obtaining the parabolic potential distribution function, the Poisson equation is solved to obtain the front surface potential. The minimum surface potential point of the channel region gives us the inversion condition required to derive the threshold voltage of the device. Using the threshold voltage model, the drain current in linear and saturation region can be deduced by following the approach as suggested by Suzuki et al. [128].

Secondly, impact ionization and parasitic BJT effects have large contribution towards current conduction in saturation region of the device [129]. Therefore, these effects are included while modeling conduction current in this region. As these effects will not be present before onset of saturation, hence, modeling of linear region is carried out without considering these effects. Secondly, non local effects such as, Channel length modulation [130], velocity overshoot effect [131] and drain induced barrier lowering (DIBL) [132] become more prominent in deciding transistor currents when the device dimensions are scaled in nano-meter regime. Velocity

overshoot is one of the most crucial issues since it has large impact on drive current and transconductance of the device [107] [180-182].

After deriving the expressions for linear and saturation region of device, the transconductance and output conductance are derived from the slope of I_{DS}-V_{DS} and I_{DS}-V_{GS} curve. Finally, the intrinsic DC gain is obtained from transconductance and output conductance ratio. The effect of lateral straggle over output conductance, transconductance and intrinsic gain is studied using analytical model that matches well with TCAD sentaurus device simulation results [195] for a range of lateral straggle, gate length, channel and oxide thickness.

In particular, this chapter makes the following contributions:

1) To the best of authors' knowledge, for the first time, a compact model has been deduced that considers the effect of lateral straggle (σ_L) of S/D doping profile;

2) The effect of S/D profile is introduced in terms of ionised dopant species, effective S/D ends and effective channel length calculation;

3) A compact surface potential model is derived using these ionised dopant species, effective S/D ends and effective channel length;

4) A compact threshold voltage model is deduced using the derived potential model;

5) Drain current model of linear and saturation region is deduced using the derived threshold voltage and including the non-local effects such as channel length modulation, velocity overshoot and DIBL, in addition to secondary effects such as impact ionization and parasitic BJT effects;

6) Finally, the analog FOM such as output conductance (g_m), transconductance (g_{ds}) and intrinsic gain (A_{V0}) are extracted from the slope of I_{DS}-V_{DS} and I_{DS}-V_{GS} curve.

The rest of this chapter has been organized as follows. In Section 7.2, we have deduced a surface potential model of DG-MOSFET that includes the effect of lateral straggle (σ_L) of S/D doping profile. Section 7.3 deals with modeling threshold voltage of the DG-MOSFET using

the derived potential model. Linear and saturation region drain currents are modeled in Section 7.4. These current models are further used for calculation of g_m, g_{ds} and A_{V0} in Section 7.5 which is further validated by variation of gate length, oxide and channel thickness. Finally, Section 7.6 summarizes the chapter.

7.2 Surface Potential model:

We have assumed the parabolic potential distribution along the vertical direction as [173]:

$$\psi(x,y) = a(x) + b(x)y + c(x)y^2 \tag{7.1}$$

Where $a(x)$, $b(x)$ and $c(x)$ are to be determined using boundary conditions and continuity of electric flux at the Si-SiO_2 interfaces as:

$$\psi(x,0) = \psi_f(x) = a(x) \tag{7.2}$$

$$\psi(x,t_{si}) = \psi_b(x) = a(x) + b(x)t_{si} + c(x)t_{si}^2 \tag{7.3}$$

$$\left.\frac{\partial \psi(x,y)}{\partial y}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\left(\psi_f(x) - \left(V_{GS} - V_{fb}\right)\right)}{t_{ox}} = b(x) \tag{7.4}$$

$$\left.\frac{\partial \psi(x,y)}{\partial y}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\left(\left(V_{GS} - V_{fb}\right) - \psi_{t_{si}}(x)\right)}{t_{ox}} = b(x) + 2t_{si}c(x) \tag{7.5}$$

where, V_{GS} is the applied gate potential, V_{fb} is the flat band voltage, whereas $\psi_f(x)$ and $\psi_{t_{si}}(x)$ are front and back surface potential respectively. Using the symmetry condition $\psi_f(x) = \psi_{t_{si}}(x)$ and solving eq. (7.4) and (7.5) we get

$$c(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{si}} \frac{\left(\left(V_{GS} - V_{fb}\right) - \psi_f(x)\right)}{t_{ox}} \tag{7.6}$$

The 2-D Poisson equation at Si-SiO_2 interface, considering lateral source drain profile or weak inversion operation, as shown in **Fig. 7.2**, can be written as:

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = \frac{qN_a^-}{\varepsilon_{Si}} - \frac{qN_{SD}^+(x)}{\varepsilon_{Si}} \tag{7.7}$$

where, N_a is ionized acceptor concentration and $N^+_{SD}(x)$ is the ionized donor concentration represented as [185]:

$$N^+_{SD}(x) = \left(N_{SD(p)} e^{\frac{-x^2}{2\sigma_L^2}} + N_{SD(p)} e^{\frac{-(L_g - x)^2}{2\sigma_L^2}} \right) \Big/ \left(1 + s_D e^{((E_F - E_D)/kT)}\right) \tag{7.8}$$

where, E_F is the Fermi level and E_D is the donor level of $N_{SD}(x)$ profile calculated as,

$$E_F = (E_g/2) + kT \ln(N_{SD}(x)/n_{i,eff}) \tag{7.9}$$

$$E_D = E_{g,eff} - E_i \tag{7.10}$$

The ionization energy E_i considering many body effects involving ionized donor-electron interaction is [186],

$$E_i = E_{i0}\left(1 - \sqrt[3]{N_{SD}(x)/N_{de}}\right) \tag{7.11}$$

For arsenic E_{i0} is 0.054eV and degenerated doping value N_{de} is set as 2.7×10^{19} cm^{-3} in accordance with the experimental results [187]. s_D is the spin degeneracy factor. The effective intrinsic concentration $n_{i,eff} = \sqrt{n_i^2 e^{\Delta E_g/kT}}$ and effective band gap $E_{g,eff} = E_g - \Delta E_g$ are calculated from [188], where, E_g and n_i represent bandgap and carrier density of intrinsic semiconductor.

Using the potential expression of eq. (7.1) and the values of $a(x)$, $b(x)$ and $c(x)$, the Poisson eq. (7.7) can be written as:

$$\frac{\partial \psi_f(x)}{\partial x^2} - \frac{\psi_f(x)}{\lambda^2} = \frac{q\left(N_a^- - N^+_{SD}(x)\right)}{\varepsilon_{Si}} - \frac{\left(V_{GS} - V_{fb}\right)}{\lambda^2} \tag{7.12}$$

where, the natural length

$$\lambda = \sqrt{(\varepsilon_{si} t_{si} t_{ox})/(2\varepsilon_{ox})} \tag{7.13}$$

The solution of eq. (7.12) can be carried out by calculating its complimentary function (*CF*) and particular integral (*PI*) [127]. The *PI* of first gaussian term of eq. (7.12), without considering the denominator factor of eq. (7.8), will be of form $\left(1-(\lambda D)^2\right)^{-1}\left(k_1 e^{-x_1^2}\right)$, where $x_1 = x/\left(\sqrt{2}\sigma_L\right)$, $k_1 = \left(\lambda^2 q/\varepsilon_{Si}\right) N_{SD(p)}$. Series expansion of $\left(1-(\lambda D)^2\right)^{-1}$ is one way of solving this kind

of PI. After which it can be rewritten as $\left(1+(\lambda D)^{2}+(\lambda D)^{4}+(\lambda D)^{6}+......+(\lambda D)^{2n}\right)\left(k_1 e^{-x_1^2}\right)$ and can be further simplified as: $\left(k_1 e^{-x_1^2}\right)+\sum(\lambda D)^{2n}\left(k_1 e^{-x_1^2}\right)$ [209]. Calculation of $(\lambda D)^{2n}\left(k_1 e^{-x_1^2}\right)$ is mathematically very complex to implement in a compact model, even though the gussian term can be expanded by power series method or by curve fitting approach. However, for smaller value of x_1, this term will have some contribution towards the potential profile in channel. For high x and/or small σ_L, the x_1 value becomes larger and the potential contribution from this term will be negligible. Therefore, we have approximated the PI by considering the absolute value of gaussian profile $e^{-x_1^2}$ at each point of the channel. Consequently, the solution to eq. (7.12) is approximated as:

$$\psi_f(x) \approx c_1 e^{-x/\lambda} + c_2 e^{x/\lambda} + PI \tag{7.14}$$

$$PI = \left(V_{GS} - V_{fb}\right) - \frac{\lambda^2 q\left(N_a^- - N_{SD}^+(x)\right)}{\varepsilon_{Si}} \tag{7.15}$$

where, c_1, c_2 are calculated using boundary condition at effective S/D ends as, $\psi_f\left(S_{eff}\right)=V_{bi}$, $\psi_f\left(D_{eff}\right)=V_{bi}+V_{DS}$ as shown in **Fig. 7.2(b)**. The effective S/D ends are calculated when S/D doping concentration reaches the critical value of N_{de}. Subsequently,

$$S_{eff} = \sqrt{\ln\left(N_{de}/N_{SD(p)}\right)\times\left(-2\sigma_L^2\right)} \tag{7.16}$$

$$D_{eff} = L_g - S_{eff} = S_{eff} + L_{eff} \tag{7.17}$$

$$L_{eff} = L_g - 2\times S_{eff} \tag{7.18}$$

$$c_1 = \left(\frac{v_{bi} - c_2 e^{S_{eff}/\lambda} - PI}{e^{-S_{eff}/\lambda}}\right) \tag{7.19}$$

$$c_2 = \left(\frac{\left(v_{bi} - PI\right)\times\left(1-\left(e^{-D_{eff}/\lambda}\Big/e^{-S_{eff}/\lambda}\right)\right)+V_{DS}}{e^{D_{eff}/\lambda} - \left(e^{S_{eff}/\lambda}\Big/e^{-S_{eff}/\lambda}\right)e^{-D_{eff}/\lambda}}\right) \tag{7.20}$$

The built in potential (V_{bi}) can be approximated as:

$$V_{bi} \approx v_t \ln\left(N_{de} N_a / n_{i,eff}^2\right) \tag{7.21}$$

where, $v_t = kT/q$ is the thermal voltage. The model predicted and TCAD device simulated surface potential profiles are shown in **Fig. 7.3**.

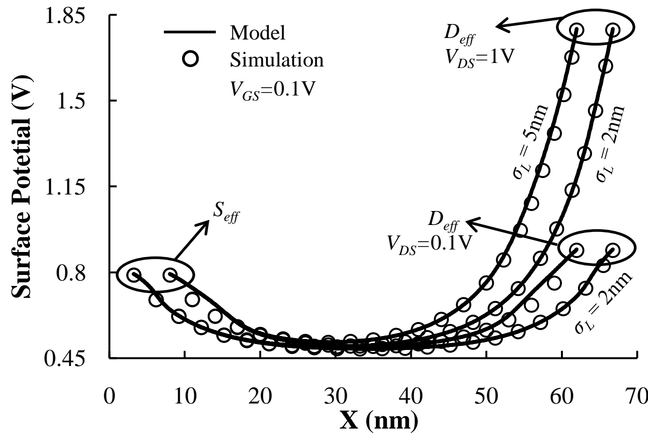

Fig. 7.3. Surface potential variation along the channel. L_g = 70nm, t_{si} = 20nm, t_{ox} = 2nm.

7.3 Threshold voltage model:

The minimum potential point $x_{\min} = (\lambda/2)\ln\left((c_1/c_2)_{\max}\right)$ is calculated by equating $\partial\psi_f(x)/\partial x = 0$. The threshold voltage is defined as the gate voltage when the channel electron densities at the minimum potential point reach the channel doping density. i. e.

$$\left(n_i^2/N_a\right)e^{\left(\psi_f(x_{\min})/v_t\right)} = N_a \tag{7.22}$$

This yields the expression for threshold voltage as:

$$V_{th} = V_{fb} + 2\phi - c_{1\max} e^{\frac{-x_{\min}}{\lambda}} - c_{2\max} e^{\frac{x_{\min}}{\lambda}} + \frac{\lambda^2 q\left(N_a^- - N_{SD}^+(x_{\min})\right)}{\varepsilon_{Si}} \tag{7.23}$$

where, $\phi = v_t \ln\left(N_a/n_i\right)$.

As shown in **Fig. 7.4**, the threshold voltage (V_{th}) is reduced with increasing σ_L. This is attributed to an increase in the spreading of donor impurity into the channel region which effectively reduces V_{GS} required for creating lesser inverted electron density in accordance with eq. (7.22). Secondly, with an increase in the V_{DS}, the lateral electric field intrudes more into the channel

region via higher σ_L. This will further reduce V_{th} and deteriorate the drain induced barrier lowering (DIBL), calculated as change in V_{th} when V_{DS} is varied from 0.1V to 1V. The model predicted that V_{th} and DIBL are in good agreement with TCAD simulation results extracted at $1.127 \times (W/L_{eff})$ μA [153]. **Fig. 7.4** also includes the abrupt threshold voltage values for different V_{DS}. For a practical device with non-zero lateral straggle, this abrupt threshold voltage and DIBL will result in incorrect prediction of drain current, transconductance, output conductance and intrinsic gain.

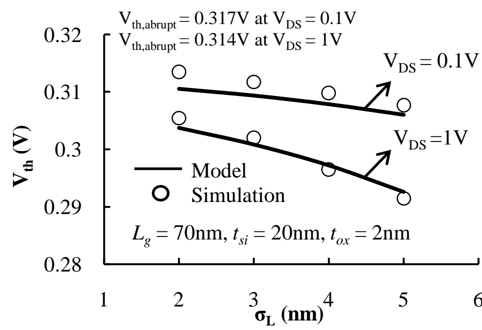

Fig. 7.4. Variation of threshold voltage with σ_L for high and low V_{DS}.

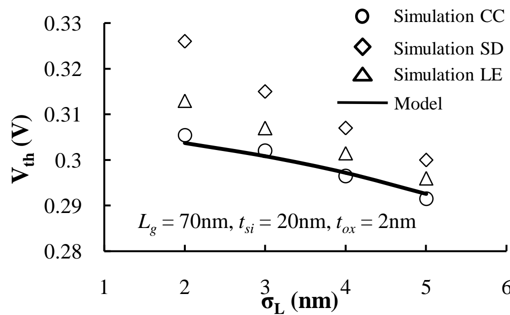

Fig. 7.5. Threshold voltage comparison with several extracted methods.

The model predicted V_{th} is compared against the extracted V_{th} via rigorous simulation techniques such as constant current (CC), second derivative (SD) and linear extrapolation (LE) methods as shown in **Fig. 7.5** [211]. We observe slight mismatch in our model predicted and extracted threshold voltages for later two cases. This is because we have assumed the conventional definition of threshold voltage, which is considered to be the gate voltage when

the surface potential is twice the fermi potential (2ϕ). Although few researchers suggest to improve this conventional definition of V_{th} by adding an empirical term to 2ϕ for a range of doping concentration and oxide thickness [212], however, as can be seen in **Fig. 7.5**, it would be pertinent to define a range of correction terms corresponding to each σ_L value. Therefore, we have considered 2ϕ as the pinning value of V_{th} for drain current model. With addition of empirical term at each σ_L value, the accuracy of the model will be improved further.

7.4 Drain current model:

The linear and saturation drain current models of DG MOSFET can be derived using the proposed threshold voltage model and considering the non-local effects such as channel length modulation [130], velocity overshoot [131] and DIBL [132] as discussed in chapter 6. Subsequently, the linear ($I_{D,lin}$) and saturation ($I_{ch,sat}$) drain currents are given by [131-133]

$$I_{D,lin} = \left(\frac{2W\mu_{neff}C_{ox}}{\left(L_{eff} - l_d + \frac{V_{DS}}{E_C} \right)} + \lambda_a \frac{2WC_{ox}}{\left(L_{eff} - l_d \right)^2} \right) \times \left[\left(V_{GS} - V'_{th} \right) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \tag{7.24}$$

$$I_{ch,sat} = \left(\frac{2W\mu_{neff}C_{ox}}{\left(L_{eff} - l_d + \frac{FV_{DS,sat}}{E_C} \right)} + \lambda_a \frac{2WC_{ox}}{\left(L_{eff} - l_d \right)^2} \right) \times \left[\left(V_{GS} - V'_{th} \right) FV_{DS,sat} - \frac{1}{2} \left(FV_{DS,sat} \right)^2 \right] \tag{7.25}$$

The parameter F in eq. (7.25), before $V_{DS,sat}$ is the smoothing function ensuring smooth transition between linear and saturation region. It is given by [130]

$$F = 1 - \frac{\ln\left(1 + e^{A(1 - V_{ds}/V_{dsat})}\right)}{\ln\left(1 + e^{A}\right)} \tag{7.26}$$

where, constant A = 3 has been found a good fitting parameter. Furthermore, the impact ionization and parasitic BJT effects are added to the final saturation current model so that:

$$I_{D,sat} = GI_{ch,sat} + HI_{CBO} \tag{7.27}$$

Fig. 7.6 and **Fig. 7.7** plots I_{DS}-V_{DS} and I_{DS}-V_{GS} plots of the proposed model which is in good agreement with the TCAD simulation results. Lower V_{th} and L_{eff} are the reason for an increase in the drain current with increase in σ_L, which facilitate lateral penetration of drain electric field.

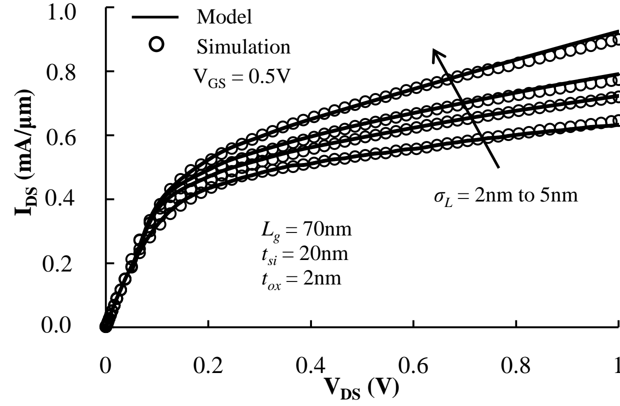

Fig. 7.6. I_{DS}-V_{DS} characteristics of DG MOSFET for various σ_L value.

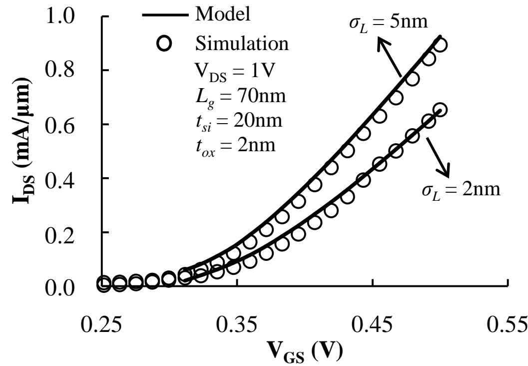

Fig. 7.7. I_{DS}-V_{GS} characteristics of DG MOSFET for various σ_L value.

7.5 Analog parameter extraction:

The **Fig. 7.8(a)** and **(b)** show variation of g_m and g_{ds} with σ_L. The g_{ds} is extracted from the slope of I_{DS}-V_{DS} between V_{DS} = 0.9 V and V_{DS} = 1V at V_{GS} = 0.5V while g_m is extracted from the slope of I_{DS}-V_{GS} between V_{GS} = 0.45 V and V_{GS} = 0.5V at V_{DS} = 1V for both model predicted and simulation values. The analysis is carried out at an overdrive voltage (V_{GS}-V_{th}) of ≤ 200mV to target the high gain operation regime of device. The g_m and g_{ds} are expected to increase at

higher σ_L because of reduction in L_{eff} [133]. However, as shown in **Fig. 7.8(c)**, the A_{V0} will decrease with increase in σ_L because of reduction in threshold voltage as:

$$A_{V0} = \frac{g_m}{g_{ds}} = \frac{K_n(V_{GS} - V_{TH})}{(\lambda/2)K_n(V_{GS} - V_{TH})^2} = \frac{2}{\lambda(V_{GS} - V_{TH})} \tag{7.28}$$

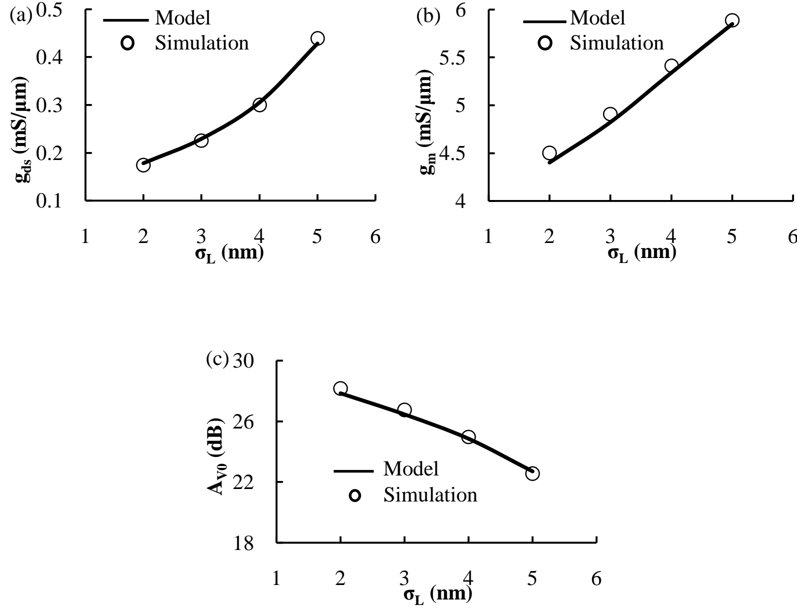

Fig. 7.8. Variation of (a) g_{ds} (b) g_m (c) A_{V0} with lateral straggle. L_g = 70nm, t_{si} = 20nm, t_{ox} = 2nm.

Where, $K_n = \mu_n C_{ox} W/L_{eff}$. We observe ~6dB decrease in A_{V0} when σ_L is varied from 2nm to 5nm. Lower value of the gate length (L_g), higher value of the oxide (t_{ox}) and channel thickness (t_{si}) will aggravate the lateral electric field penetration into the channel region, resulting in further loss of gate electrostatic integrity and, in turn, lower V_{th} and A_{V0}. We observe reduction in V_{th} by ~22mV and A_{V0} by ~ 12dB, when L_g is reduced to 60nm as shown in **Fig. 7.9 (a)**. We have limited our analysis to L_g = 60nm, because of limitation in velocity overshoot model parameter λ_a which will dominate the drain current after this gate length [131]. The variation in V_{th} and A_{V0} with t_{ox} and t_{si} are shown in **Fig. 7.9 (b)** and **(c)**. It is observed that V_{th} and A_{V0} changes by approximately 24mV and 11 dB while t_{ox} changes from 1nm to 3nm, while variation in t_{si} from 10nm to 30nm will reduce V_{th} and A_{V0} by ~24mV and ~ 12dB. Our model predicted values are

slightly lower than the simulated values at lower value of t_{si}. This is attributed to presence of volume inversion effect at lower value of t_{si}, which is not considered in our model, resulting in higher transconductance and, in turn, increased A_{V0} [153].

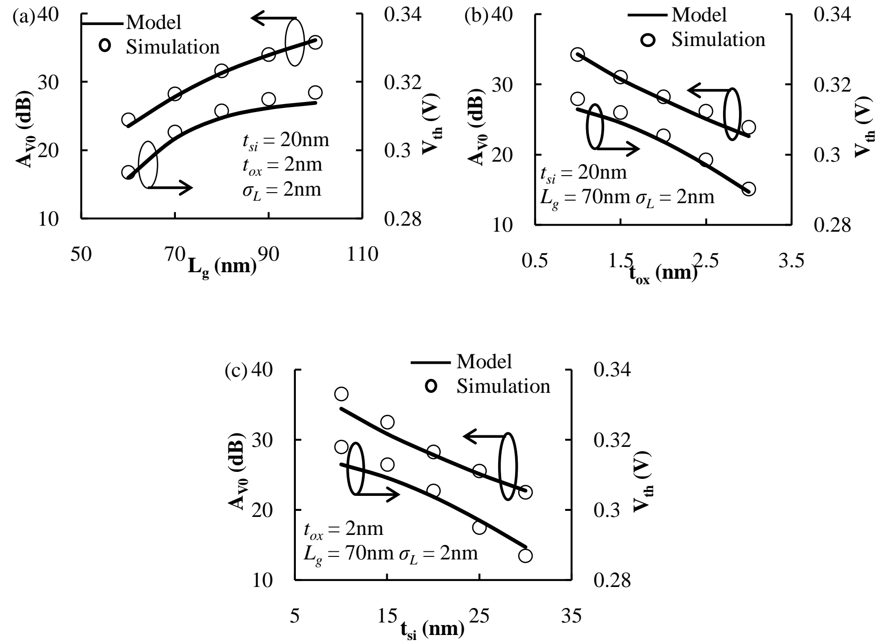

Fig. 7.9. Variation of V_{th} and A_{V0} with (a) L_g (b) t_{ox} (c) t_{si}.

7.6 Summary:

A new analytical potential model has been developed for a DG-MOSFET that includes the effect of lateral gaussian profile of source/drain dopant species. The proposed model captures well the effect of lateral electric field spread via this gaussian profile of dopant species. As exact computation involving gaussian like S/D profile is mathematically very complex, therefore, instead of solving the potential equation involving gaussian term, we have approximated it by its absolute value at the each point of the channel. For generating a compact model, the effect of source/drain gaussian profile is introduced in terms of ionised dopant species, effective source/drain ends and effective channel length calculation considering dopant degeneracy effects.

Increase in lateral straggle of source/drain gaussian profile facilitates propagation of lateral electric field which, in turn, lowers the threshold voltage and effective channel length of the device. These two effects will affect the current drive and change crucial parameters like transconductance and output conductance. The linear and saturation drain current models of DG MOSFET are derived using the proposed threshold voltage model and including the non-local effects such as channel length modulation, velocity overshoot and DIBL. More so, impact ionization and parasitic BJT effects are added to the final saturation current model to account for large lateral electric field at nano-scale devices. The transconductance and output conductance are extracted from the slope of I_{DS}-V_{DS} and I_{DS}-V_{GS} curve. Finally, the intrinsic DC gain is obtained from transconductance and output conductance ratio.

The intrinsic gain is deteriorated with increase in lateral straggle because of loss of gate electrostatic integrity and reduction in threshold voltage. As the device dimensions are scaled in nano-meter regime, the proposed model will become prominent in deciding device characteristics, as the effect of lateral electric field will be pronounced via gaussian like profile of source/drain dopant species. Therefore, to further validate our model, we have varied crucial parameters like gate length, channel and oxide thickness of DG-MOSFET. It is observed that the model agrees well with TCAD sentaurus simulation results for variation in these crucial device dimensions [195].

Chapter 8

Conclusions and Further Scope

In this chapter, a summary of the research work carried out has been reported, along with the conclusions of the work. Specific directions for future research are also indicated.

8.1 Conclusions:

The major contributions and conclusions from this work are summarized below.

The short channel and analog performance analysis of dual-*k* spacer based underlap FinFET is covered in first part of the work. It is concluded that, the use of optimized inner high-*k* spacer is beneficial in controlling DSDT, SCEs and improving analog figures of merit (FOM) such as, transconductance, output conductance, transconductance-to-current ratio, early voltage, cutoff and maximum oscillation frequency. More so, inner high-*k* spacer length optimization improves intrinsic gain of the device in all extension lengths irrespective of doping gradient without sacrificing the frequencies (f_T and f_{max}) as compared to low-*k* FinFET. Subsequently, it is observed that, dual-*k* spacer based underlap FinFET is beneficial in improving analog FOM of the device at scaled gate lengths too. In addition, a detailed analysis of the effect of variations in crucial device parameters like gate oxide thickness (T_{ox}), fin width (W_{fin}), lateral straggle (X_j) of source drain doping profile etc., are carried out to formulate a guideline for dual-*k* spacer underlap FinFET design in analog domain. A guideline for designing dual-*k* FinFET considering alternative inner high-*k* spacer dielectric materials are also studied in detail. It is observed that for an optimum aspect ratio (fin height/fin width), the FOM of dual-*k* FinFETs are considerably higher and posses lesser variation to fin width, oxide thickness and S/D lateral straggle. Subsequently, A_{DM}, A_{CM} and CMRR of dual-*k* FinFET based single stage operational

transconductance amplifier (OTA) are improved, considering spatial variations in critical transistor attributes.

In the second part of the work, extensive study of low temperature operation of underlap FinFET is carried out in order to address the scaling issues in nano-meter regime at low temperatures. It is shown that as the operating temperature is lowered to 100K, pronounced improvement in mobility and threshold voltage of dual-*k* FinFET enhances the analog FOM further. TCAD simulation at 100K temperature shows that, FOM like A_{V0}, f_T and f_{max} of 16nm gate length based dual-*k* FinFET are improved by approximately 11.5dB, 10GHz and 9GHz respectively as compared to the FOM of low-*k* FinFET. Subsequently, scaling down the gate length of dual-*k* FinFET to lower technology node is possible at this operating temperature range, because of overwhelming increase in analog FOM.

In the last part of research work, an analytical model has been developed for dual-*k* spacer based double gate underlap FinFET. To the best of our knowledge, fringing field model between two different dielectric interfaces (ε_h and ε_l) of underlap section has been carried out for the first time. Each underlap section has been divided into two parts low-*k* and high-*k* section. Modelling of inner high-*k* section is carried out by conformal mapping technique where as modeling of outer low-*k* section has been carried out by solving continuity equations in two different (low-*k*/high-*k*) dielectric interface. Analog FOM like, transconductance, output conductance and intrinsic gain has been extracted from the current curves deduced via the proposed threshold voltage model that matches well with TCAD sentaurus device simulation results with variation in crucial device dimensions such as, gate oxide thickness, inner high-*k* spacer length and its dielectric constant. It is observed that dual-*k* FinFETs can improve the intrinsic gain by approximately 10dB when TiO_2 (k = 40) is used as inner high-*k* spacer. This part of research work has been further extended to develop a compact model for DG MOSFET that considers the effect of lateral straggle of source/drain gaussian profile. With lightly doped

channel, the source/drain dopant species can intrude into the channel region when rapid thermal processing step following the high temperature annealing is performed to activate the dopant species. Therefore, it is crucial to consider the effect of source/drain gaussian profile while generating compact model for DG MOSFETs. This effect lowers the threshold voltage and effective channel length of the device and, in turn, alters the current drive and crucial analog FOM. Of particular importance is the intrinsic gain of the device which is observed to decrease by approximately 6dB when the lateral straggle is set to 5nm. Subsequently, the results obtained on the basis of our model were found to be a close match with the TCAD sentaurus simulation results, thus ensuring the accuracy of the model developed.

8.2 Scope for Future Research:

The present research work brings out a small portion of the great potential of the research in the area of analog performance of integrated devices and circuits. To go further, we briefly point out some directions in which we think further research should be carried on:

1. The mathematical model of dual-*k* FinFET that has been developed in this work can be extended to model the inner and outer fringe capacitance (C_{if} and C_{of}) of the device. Since the model captures well the effect of electric field pattern change at different dielectric interface in addition to change in effective gate height at interface as well as in high-*k* section of the device, there is a great potential to carry out the research on computing the charge associated with this fringing electric fields which will be helpful in computing C_{if} and C_{of}. Subsequently, model for gate to source capacitance, gate to drain capacitance and total gate capacitance can be deduced in order to model the frequency components (f_T and f_{max}) of the device. Therefore, modeling C_{if} and C_{of} have good potential for future research work.

2. Modeling of subthreshold slope and subthreshold current are two important aspect of device design that can be extended from the present mathematical model too. There are not many compact models at present that addresses these issues in dual-*k* underlap FinFET and the

studies are only limited to time consuming TCAD mixed mode simulations. Therefore, there is a great need for compact models development for this kind of advanced devices which can be further included in circuit simulators such as HSPICE.

3. Performance of important analog circuits like current mirror, differential amplifier, band gap reference operational amplifier etc., that can be designed using this kind of advanced FinFET, is another important aspect oriented towards future research work. Although it's a time consuming process to go for mixed mode circuit simulation in TCAD environment, nevertheless, evolution of mathematical models can predict the circuit behavior in various advanced modern day tools like Verilog A. More so, the circuit performance of the designed OTA and additional circuits can be studied at low temperature environment that can be included in future scope of work too.

4. TCAD process simulation of dual-*k* spacer based underlap FinFET considering various process induced variations like, line edge and interface roughness, variations in S/D dopant dose and energy etc. is another important aspect of design that can be studied for observing robustness of the device in terms of SCE and analog FOM. Therefore, this kind of study can be a possible future topic of research.

Appendix: Physical Constants and Device Parameters

Description	Symbol	Value and Unit
Electronic Charge	q	1.6×10^{-19} C
Temperature	T	300 K
Boltzmann's Constant	k	1.38×10^{-23} J/K
Intrinsic Carriers Concentration	n_i	1.5×10^{16} m^{-3}
Vacuum Permittivity	ϵ_0	8.85×10^{-12} F/m
Silicon Permittivity	ϵ_{si}	1.04×10^{-10} F/m
Oxide Permittivity	ϵ_{ox}	3.45×10^{-11} F/m
Planck's Constant	h	6.63×10^{-34} J-s
Modified Planck's Constant	$\hbar$	$(h/2\pi)=1.05 \times 10^{-34}$ J.s
Thermal Voltage (T = 300 K)	kT/q	0.0259 V
Angstrom	A^o	$1\ A^o = 10^{-10} m$
Electron Volt	eV	1 eV = 1.6×10^{-19} J
Free Electron Mass	m_o	9.1×10^{-31} kg
Electrons Effective Mass in Si (Transverse)	m_t^*	$0.19m_0$
Electrons Effective Mass in Si (Longitudinal)	m_l^*	$0.98m_0$
Band-gap of Si	E_g	1.12 eV
Bulk Mobility for Un-doped Si	μ_{bulk}	0.1441 m^2/V.s

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List of Publications

Based upon the research work carried out, following papers are published/in press/accepted/under review/communicated for publications to various peer reviewed International Journals and Conferences.

International Journals:

1. **Ashutosh Nandi**, A. K. Saxena and S. Dasgupta, “Impact of Dual-*k* Spacer on Analog Performance of Underlap FinFET,” *Elsevier Microelectronics Journal*, Vol. 43, pp. 883-887, 2012.
2. **Ashutosh Nandi**, A. K. Saxena and S. Dasgupta, “Design and Analysis of Analog Performance of Dual-*k* Spacer Based Underlap N/P-FinFET at 12nm Gate Length,” *IEEE Transactions on Electron Devices*, Vol. 60, No. 5, pp. 1529-1535, May 2013.
3. **Ashutosh Nandi**, A. K. Saxena and S. Dasgupta, “Analytical Modelling of Double Gate MOSFET Considering Source/Drain Lateral Gussian Doping Profile,” *IEEE Transactions on Electron Devices*, Vol. 60, No. 11, pp. 3705-3709, Nov 2013.
4. **Ashutosh Nandi**, A. K. Saxena and S. Dasgupta, “Enhancing Low Temperature Analog Performance of Underlap FinFET at Scaled Gate Lengths,” *IEEE Transactions on Electron Devices*, Vol. 61, No. 11, pp. 3619-3624, Dec 2014.
5. **Ashutosh Nandi**, A. K. Saxena and S. Dasgupta, “Compact Analytical Modelling of Dual-*K* Spacer Based Underlap FinFET,” Under review in *IEEE Transactions on Electron Devices*.
6. **Ashutosh Nandi**, A. K. Saxena and S. Dasgupta, “Oxide Thickness and S/D Junction Depth Based Variation Aware OTA Design Using Underlap FinFET,” Communicated to *Elsevier Microelectronics Reliability*.

International Conference/Workshop:

7. **Ashutosh Nandi**, A. K. Saxena and S. Dasgupta, "Analog Performance Analysis of Dual-*k* Spacer based Underlap FinFET," in 16th *International Symposium on VLSI Design and Test* (VDAT 2012), *Springer LNCS* 7373, pp. 46-51, July 1-4, 2012.