DESIGN AND ANALYSIS OF VERTICAL NANOWIRE CMOS DEVICES AND CIRCUITS

Ph.D THESIS

by

MAHESHWARAM SATISH

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE - 247667, INDIA
DECEMBER, 2014

DESIGN AND ANALYSIS OF VERTICAL NANOWIRE CMOS DEVICES AND CIRCUITS

A THESIS

Submitted in partial fulfilment of the requirements for the award of the degree

of

DOCTOR OF PHILOSOPHY

in

ELECTRONICS AND COMMUNICATION ENGINEERING

by

MAHESHWARAM SATISH

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE – 247 667 (INDIA)

DECEMBER, 2014

©INDIAN INSTITUTE OF TECHNOLOGY ROORKEE, ROORKEE- 2014
ALL RIGHTS RESERVED

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **"DESIGN AND ANALYSIS OF VERTICAL NANOWIRE CMOS DEVICES AND CIRCUITS"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electronics and Communication Engineering of the Indian Institute of Technology Roorkee is an authentic record of my own work carried out during a period from July, 2010 to December, 2014 under the supervision of **Dr. S. Manhas**, Associate Professor and **Dr. B. Anand**, Associate Professor, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(MAHESHWARAM SATISH)

This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

(S. Manhas)
Supervisor

(B. Anand)
Supervisor

Date:_________

ABSTRACT

The continued CMOS scaling has led to the need for introduction of 3-D transistors such as multigate FETs for technology nodes at 22 nm and below replacing planar MOSFETs (Metal Oxide Semiconductor Field Effect Transistors). Of these novel devices, the nanowire (NW) devices have minimum short channel effects (SCE) and allow thicker gate insulator thereby reducing the leakage currents in the device. Further, in NW device family, the Vertical Nanowire FETs (VNWFET) have additional strong advantage of occupying least silicon area due to vertical pillar structure and possibility of stacking devices vertically. This has driven numerous researchers to work on vertical nanowire devices and its circuits. Although there have been studies reporting device level fabrication results for VNW FETs, but due to fabrication challenges and large cost involved in developing technologies, accurate VNW CMOS circuit performance evaluation has not been well demonstrated and thoroughly investigated. The use of TCAD in VNW CMOS development is of high importance, as TCAD can help to reduce design cycles as well as provide critical insight into VNW CMOS behavior and key performance factors. At extremely scaled dimensions, the device and layout parasitics also start to dominate and are of high importance in evaluating circuit performance. The vertical device architecture has several issues like: newer/different kind of parasitic components such as contact overlapping nanowire tip, increased parasitic due to cylindrical structure and asymmetry due to differences in top/bottom electrodes contacts. Thus, the impact of parasitic and electrode asymmetry on device and circuit performance with scaling are important design issues. In this thesis, we investigate the performance of VNW CMOS and its design issues using well calibrated 3D TCAD simulations at 15 nm technology node as test vehicle. The important results are compared with corresponding FinFET/planar devices and circuits.

Using well-calibrated process and device parameters the scaling performance of VNWFET device is performed with respect to channel length (L_G), S/D extension length (S/D_{ext}), gate overlap/underlap length (L_{OV}), gate dielectric thickness (T_{OX}) and nanowire diameter (D_{NW}). The L_G scaling study shows that the VNWFET devices can be easily scaled down to 15 nm with a thicker dielectric of 2 nm as opposed to less than 1 nm dielectric thickness required in planar MOSFETs. From, the S/D_{ext} scaling and S/D asymmetry we find that device drive current can be increased by decreasing S/D_{ext} and source as the bottom electrode has better performance. The optimum device structure parameters for 15 nm node are: L_{OV} = 2 nm, T_{OX} = 2 nm and D_{NW} (NMOS/PMOS) = 10/15 nm. Also, it is shown that n^{th} power law can be used to

obtain device I-V characteristics matching to TCAD simulation results. Next, we develop models for parasitic series resistance and capacitance components which match well with simulation results. It is observed that gate to bottom electrode capacitance is a major contributor to device parasitic capacitance, while the contact and extension resistance are major contributors to device parasitic resistance. Further, the device performance with respect to L_G, S/D_{ext} and S/D asymmetry is explained with the help of modeled parasitic components. These parasitic models are later used in analyzing CMOS circuit performance.

Finally, we study detailed digital and analog circuit performance of VNWFET CMOS. It is observed that due to better SCE, the VNWFET CMOS inverter voltage transfer characteristics (VTC) have sharper transition than planar MOSFET. Also, we note a gradient around the noise margin (NM) extraction point which is attributed to larger series resistance that can be minimized by reducing S/D_{ext}. The CMOS inverter's dynamic performance is carried with respect to L_G scaling and compared to reported FinFET and planar MOSFET inverters. It is found that VNWFET has the better delay, area and power performance when compared to planar or FinFET. The device S/D asymmetry leading to various possible CMOS layouts for a given circuit are investigated, we report new layout rule guidelines for VNWFET based circuit design. Further, it is shown that VNWFET based inverter delay can be improved by reducing S/D_{ext} and by using device with source as bottom electrode provides best circuit performance. The CMOS inverter delay is modeled using the effective current method, which uses the parasitic capacitance model for delay prediction, and the delay model results match well with simulation results. This also explains the circuit performance with respect to S/D_{ext} scaling and S/D asymmetry. Lastly, analog performance of VNWFET device is done and the intrinsic frequency response is compared to an equivalent FinFET. It is found that VNWFET has better gain, 3dB bandwidth and unity gain bandwidth (f_T). Further, the impact of S/D_{ext} length on common source (CS) amplifier is performed and it is seen that with lower source extension length the amplifier has better performance in terms of gain, 3dB bandwidth and f_T.

The overall results obtained in this study demonstrate that VNW CMOS has very high potential for use in CMOS based digital/analog circuits and offers best overall performance for CMOS technology nodes below 22 nm when compared to planar or FinFET. The study of digital/analog circuit design in this thesis highlight new circuit design methodologies and circuit layout rules, which addresses device asymmetry and parasitics. The parasitic models proposed through this work can be used to develop a compact SPICE model for VNWFET, with which circuit design and performance analysis on various standard cells, analog building blocks, SRAM cell and reliability study can be easily performed.

ACKNOWLEDGEMENT

I cannot stop myself from writing a very long acknowledgement as I have to cover almost 6 and 1//2 years of my stay at Indian Institute of Technology, Roorkee, which includes 2 years of M.Tech.

First of all, I would like to thank Dr. Sanjeev Manhas who guided me during M.Tech dissertation and is the real motivation for me to choose Ph.D as my next step in career. I would like to thank my M.Tech batch mates Parag, Nema, Sandeep, Ankit, Atul bhai, NVSS, Sravan, and Vivek ji for the support and encouragement given to me when I was in dilemma regarding choosing Ph.D as my career. All of them along with Dr. Manhas believed that I can do justice to what I have started as my M.Tech dissertation and give it completeness through Ph.D. At this point I would like to thank my parents and sisters for allowing me to enroll for Ph.D program and relieving me from various family responsibilities to pursue research.

Now that I am submitting my thesis, I express my heartfelt gratitude to Dr. Sanjeev Manhas, and Dr. Anand Bulusu, Associate Professors in Department of Electronics and Communication Engineering at Indian Institute of Technology Roorkee, for their valuable guidance, support, encouragement and immense help. I consider myself extremely fortunate for getting the opportunity to learn and work under their able supervision. Working under their guidance will always remain a cherished experience in my memory and I will adore it throughout my life. I would like to thank Dr. Manhas's family, as I have taken a lot of his personal time for my thesis related discussions.

My sincere thanks to the faculty of Microelectronics and VLSI Technology group Department of Electronics and Communication Engineering at Indian Institute of Technology Roorkee, for the technical knowhow and analytical abilities they have imbibed, which have helped me in dealing with the problems I encountered during the thesis. I am thankful to my student research committee which has given critical suggestions and reviewed my progress time to time.

I take this opportunity to thank the lab supervisors Naveen ji and Dinesh ji for their support in providing and maintenance of lab facilities whether it is faster license procurement, high end workstation procurement and networking/internet related issues.

I would also like to remember my seniors and juniors with whom I have spent a lot of time at IITR and memories that bring smile on my face. I am really indebted to Manju mam, Puru sir, Kola, Baljit mam, Anju, and Shivam who have taken care of my appetite with their version of

rasam, sambhar, curries, soya chaap, rotis, and pulao respectively. I am thankful to god for introducing me to Santu, Ron dada, Gaurav bro, Gaurav Kapil, Venu and Ashok who gave constant support, motivation, help even though they were from different departments or groups and spent a lot of time on trips, daily badminton matches and weekend parties. I would like to sincerely thank senior research scholars of Microelectronics and VLSI group Jiten sir, Naushad sir, Rathod sir, Vaddi sir, Gaurav sir and Nandi who have given a lot of their time to clarify my research doubts. I am happy to have known industrious M.Tech juniors Jitano, Swati, Siva, Deepika, Gaurav Bharadwaj, Arvind, Ravisankar, Sarvesh, Raghav, Asheesh, Prateek, Bipin, and Sai with whom I had very long discussions. A special mention of time spent with Durga, Akhil, Sandeep, Sidhu and Sashank on trips to Rohtang pass, Vaishno devi temple and Surkanda devi temple.

I want to thank Dr. Bulusu for giving the opportunity to mentor his Ph.D student Archana. I am really proud to have mentored such hard working and sincere learner. I would like to thank Archana as she made me to learn a lot of new things in order to clarify her doubts. I want to thank Dr. Manhas once again, for giving the opportunity to mentor his students Sakshi (summer intern from NIT Hamirpur), Mohit (M.Tech) and Omdot (Ph.D). I have spent a lot of time with them working on compact modeling of MOSFET devices. I consider these four as my torch bearers, and wish them to take my work to the next level successfully. I wish each one of my juniors a very bright future and a healthy life.

My acknowledgement is incomplete without mentioning thanks to Ministry of Human Resource Development, Govt. of India, who have provided fellowship during my Ph.D.

Finally, I want to thank నాన్న శ్రిషైలం గారు, అమ్మ స్త్యవెని గారు and అక్కలు సునిత, కల్పన, and ఉష for their love and support, without which I wouldn’t have made it this far in my career. I thank god gifted sisters Veenakka, Swa, Meena, Sampada, Reppika, Kanchu, Havi, Sona, ‘Su’dha/ma, Soumya, and friends Rohit, Chandu, Kishore, Puneet, Manasa, Chaitu, Chan, Swe, Pal and Saja, whom I met at different junctures during my life time for their unending support and motivation during my higher education at IITR. I am happy to have them as part of my life as I can talk to them any time and on anything. I am thankful to Bachan and Suru (trekking guides) for showing me the beauty of nature during my trek to Devkhira, in the valley of Har-ki-dun and for allowing me to lead the group during trek of Devban’s snowy peaks. I will end with a mention of regular visitors Parag, Nema, Mona, Baba, and Gullu who forced me to take time out for myself.

Maheshwaram Satish

Ph. D. (MEV)

CONTENTS

ABSTRACT i
ACKNOWLEDGEMENT iii
CONTENTS v
LIST OF FIGURES ix
LIST OF TABLES xiii
ABBREVIATIONS AND SYMBOLS xv
1 CHAPTER 1
INTRODUCTION 1
1.1 Introduction 1
1.2 Motivation 4
1.3 Objectives 5
1.4 Thesis Organization 5
2 CHAPTER 9
LITERATURE SURVEY 9
2.1 Scaling Theory 9
2.2 Device Fabrication 11
2.3 NW Circuit Performance 14
2.4 NW Modeling 15
2.5 Vertical NW Circuit Performance 16
2.6 VNWFET Other Applications 16
2.7 Technical Gaps 17
3 CHAPTER 19
TCAD CALIBRATION 19
3.1 Technology Computer Aided Design: TCAD 19
3.1.1 Process Simulation 20

3.1.2 Device Simulation ... 21
3.2 Calibrated Simulation Setup ... 23
3.3 Device and Simulation Details ... 27
4 CHAPTER ... 29
DEVICE SCALING PERFORMANCE ... 29
4.1 Scaling of Channel Length: L_G ... 30
4.2 Scaling of Extension Length: S/D_{ext} ... 31
4.3 Scaling of Gate Overlap/Underlap Length: L_{OV} ... 32
4.4 Scaling of Gate Dielectric: T_{OX} ... 33
4.5 Scaling of Nanowire Diameter: D_{NW} ... 34
4.6 n^{th} Power Law Modeling ... 34
4.7 Summary ... 37
5 CHAPTER ... 39
PARASITIC MODELING ... 39
5.1 Capacitance Modeling ... 39
5.2 Series Resistance Modeling ... 46
5.3 Summary ... 53
6 CHAPTER ... 55
CIRCUIT PERFORMANCE ... 55
6.1 Digital Performance ... 55
6.1.1 VNW CMOS Inverter Voltage Transfer Characteristics (VTC) Analysis ... 55
6.1.2 Benchmarking of Inverter Transient Response ... 60
6.1.3 VNW CMOS Inverter Delay Analysis ... 61
6.1.4 VNW CMOS Inverter Delay Modeling ... 65
6.2 Analog Performance ... 67
6.3 Summary ... 72
7 CHAPTER ... 75
CONCLUSION & FUTURE SCOPE ... 75

7.1 Conclusion 75
7.2 Future Scope 78
BIBLIOGRAPHY 81
PUBLICATIONS 99
APPENDIX A 101
APPENDIX B 107
APPENDIX C 113

LIST OF FIGURES

Figure 1.1 Evolution of device structure from single-gated to GAA NWFET [25]. 2
Figure 1.2 3D device structure of lateral nanowire supported by source/drain pads at its ends [55]. 3
Figure 1.3 3D isometric view of Vertical Nanowire device [57]. 3
Figure 2.1 Fabrication flow of SGT [76]. 12
Figure 2.2 Process flow of vertical MOSFET [77]. 12
Figure 2.3 Process flow for pillar and transistor formation [78]. 13
Figure 2.4 SEM image of vertical NWFET [78]. 14
Figure 3.1 Finite element grid magnified at gate-drain corner of an NMOSFET [66]. 20
Figure 3.2 2D SOI MOSFET obtained using structure editor [66]. 21
Figure 3.3 Current flow lines in a 0.13-μm NMOSFET at V_{gs} = 1.5 V and V_{ds} = 3.0 V; shading represents current density [66]. 21
Figure 3.4 Drain current as function of drain voltage for a 50-nm NMOSFET at V_{gs} = 0.25, 0.5, 0.75, 1.0, and 1.25 V [66]. 23
Figure 3.5 3D isometric view of Vertical nanowire device [127]. 23
Figure 3.6 I_D-V_{GS} characteristics of VNWFET device with reported dimensions is found to match well with experimentally reported data [57]. 25
Figure 3.7 I_D-V_{GS} characteristics of rectangular nanowire device with reported dimensions is found to match well with experimentally reported data [135]. 26
Figure 4.1 Vertical Nanowire FET structure highlighting important physical dimensions. 29
Figure 4.2 (a) I_{ON} ($V_{GS} = V_{DS} = V_{DD}$) and I_{OFF} (V_{GS} = 0V, $V_{DS} = V_{DD}$) of NMOS and PMOS VNW FET versus L_G. (b) SS and DIBL of NMOS and PMOS VNWFET versus L_G showing marginal presence of SCE when L_G is scaled down to 15 nm. 30
Figure 4.3 I_{ON} ($V_{GS} = V_{DS}$ = 0.8 V) and I_{OFF} (V_{GS} = 0V, V_{DS} = 0.8 V) of (a) n (D_{NW} = 10 nm), (b) p (D_{NW} = 14 nm) VNW FET drive showing excellent scaling performance with S/D_{ext} down to 10nm. SS and DIBL of (c) NMOS and (d) PMOS VNWFET showing marginal presence of SCE when S/D_{ext} =10 nm. 31
Figure 4.4 I_{ON}, I_{OFF} variation with respect to gate overlap/underlap length. 32
Figure 4.5 I_{ON}, I_{OFF} variation with respect to gate dielectric thickness. 33
Figure 4.6 I_{ON}, I_{OFF} variation with respect to nanowire diameter variation. 34
Figure 4.7 Selected points for model parameter extraction of nth power law [67]. 35

Figure 4.8 I-V characteristics of NMOS and PMOS VNWFET (L_G=45nm, S/D_{ext}=30nm, Diameter=15nm) obtained from simulation (solid lines) and obtained from n^{th} power law model (dotted lines) [57]....36
Figure 5.1 VNW FET 3-D isometric view....39
Figure 5.2 VNWFET 2-D view marked with parasitic capacitance components....40
Figure 5.3 *GTof* and *gexT* components are identified for (a) Extension length > gate thickness (b) Extension Length < gate thickness [139]....42
Figure 5.4 Inter electrode capacitances versus V_G for NMOS and PMOS VNWFET (L_G=15 nm, S/D_{ext} = 30 nm and D_{NW}=10/15 nm)....43
Figure 5.5 NMOS (D_{NW}=10nm) simulated (symbol) and modeled (line) parasitic off state capacitances versus (a) L_G (S/D_{ext}=30nm) and (b) S/D_{ex} (L_G=15nm) and individual components contributing to C_{GG} versus (c) L_G and (d) S/D_{ext}....44
Figure 5.6 PMOS (D_{NW}=14/15nm) simulated (symbol) and modeled (line) parasitic off state capacitances versus (a) L_G (S/D_{ext}=30nm) and (b) S/D_{ex} (L_G=15nm) and individual components contributing to C_{GG} versus (c) L_G and (d) S/D_{ext}....45
Figure 5.7 VNW FET 3-D isometric view with individual resistance components identified...46
Figure 5.8 Electron (e) density profile in the device cross section through nanowire centre shown at V_G=V_{DD} and V_D=0.05V to highlight the impact of isolation oxide....49
Figure 5.9 R_{TB} extraction methodology shown for NMOS VNW for L_G = 45 nm and 15 nm, S/D_{ext} = 30nm....49
Figure 5.10 Extracted R_{TB}, R_{ON} versus (a) L_G (S/D_{ext} = 30nm) and (b) S/D_{ext} (L_G = 15nm) and individual resistance components contributing to NMOS R_{TB} versus (c) L_G and (d) S/D_{ext}, where R_{oth} represents the sum of *sh* and *sp* resistances....50
Figure 5.11 Simulated (symbol) and modeled (line) R_T (red) and R_B (blue) versus L_G (a) NMOS (b) PMOS, and with respect to S/D_{ext} (c) NMOS and (d) PMOS....51
Figure 6.1 CMOS VTC for VNW, FinFET and planar MOSFET. FinFET VTC is not symmetric due to mismatch in drives of its NMOS/PMOS Fin devices. Solid line circle highlights the switching transition region and the dotted circles highlights the gradient around the NM extraction point....56
Figure 6.2 (a) Resistive loaded CMOS circuit schematic. (b) Impact of R_D, R_S on VTC of planar CMOS at 45nm. Degradation in NM is highlighted in insets....57
Figure 6.3 Planar NMOS, PMOS I_D-V_{DS} characteristics with 0, 12kΩ series resistance. The vertical down directing arrows indicate the V_{DSsat} points, the double ended arrow represents the switching region of CMOS and the inclined lines represent slope in linear region. 57

Figure 6.4 VNW NMOS, PMOS I_D-V_{DS} characteristics with S/D_{ext} = 10/30nm resistance.......58
Figure 6.5 (a) VNW VTC simulated (lines) and VTC generated using I_D-V_{DS} characteristics (symbols) for L_G=45nm, S/D_{ext} =30/10nm. (b) Gain of inverter for varying S/D_{ext}. (c) NM extraction.......59
Figure 6.6 VNW inverter transient response for L_G=45, 22 nm, S/D_{ext} = 30nm and Diameter = 10/15nm (NMOS/PMOS).......60
Figure 6.7 Benchmarking of VNW, simulated FinFET, experimentally reported FinFET and planar CMOS.......61
Figure 6.8 Topview of S_B inverter (a) L1 layout. (b) L2 layout. F is minimum feature size (15 nm).......62
Figure 6.9 (a) Delay versus $S/D_{ext.}$ (b) Load capacitance (C_L) and circuit speed metric (C_L/I_{ON}) versus S/D_{ext} for S_B VNW CMOS L_G = 15 nm.......62
Figure 6.10 Impact of S/D asymmetry on delay performance and extracted C_L of different layouts.......63
Figure 6.11 Delay and power variation with S/D_{ext} for S_B and S_T inverters.......64
Figure 6.12 Power and power delay product (PDP) variation with S/D_{ext} for S_B and S_T inverters.......64
Figure 6.13 Schematic diagram of two stage inverter chain.......65
Figure 6.14 Delay (T_d) extracted-modeled and power versus S/D_{ext} for S_B and S_T VNW CMOS (L_G=15nm).......66
Figure 6.15 CS amplifier circuit topology.......67
Figure 6.16 CS amplifier V_{out}, gain versus V_{in} for various R_L. VNW device L_G=15nm, S/D_{ext} = 20nm.......68
Figure 6.17 Impact of bias voltage on CS amplifier performance. VNW device L_G=15nm, S/D_{ext} = 20nm.......68
Figure 6.18 Impact of multiple nanowires in VNW on CS amplifier performance. VNW device L_G=15nm, S/D_{ext} = 20nm.......69
Figure 6.19 Frequency response of intrinsic VNW device (L_G=15nm, S/D_{ext}=20nm, Dia=10nm) biased at V_D= 0.8V and V_G = 0.4V.......70
Figure 6.20 Frequency response of intrinsic FinFET device (L_G=16nm, S/D_{ext}=20nm, W_{fin}=10nm, H_{fin}=30nm) biased at V_D= 0.8V and V_G = 0.4V.......70
Figure 6.21 VNW devices with process variation impact on gate position. The device labeled 5nmB corresponds to device where gate position shifted towards bottom side by 5nm. 5nmT corresponds to device where gate position shifted towards top side by 5nm.......71

Figure 6.22 Intrinsic gain of VNW device with variation in gate position................................ 71
Figure 6.23 CS amplifier gain of VNW with variation in gate position.................................... 72
Figure A.1 3D device structure of a VNWFET with typical dimensions and coarse meshing. The isolation oxide is made translucent to see the nanowire and gate regions......................... 106

LIST OF TABLES

Table 2.1 Natural scale length and minimum channel length of different devices. 11
Table 3.1 Device structural parameters used in the thesis. 27
Table 4.1 Extracted n^{th} power model parameters for various VNWFET device. 37
Table 5.1 Parameters used in standard capacitance components. 40
Table 5.2 Parameters used in standard resistance components. 47
Table 6.1 Performance comparison of planar, FINFET and VNW inverters for 45 nm channel length. 60
Table 6.2 Performance of VNW device with increase in number of nanowires and change in S/D_{ext}. 69

ABBREVIATIONS AND SYMBOLS

C_{GB}	Gate to Bottom electrode capacitance
C_{GG}	Total gate parasitic capacitance
C_{GT}	Gate to Top electrode capacitance
C_{load}	Total output node capacitance
C_M	Miller capacitance
CMOS	Complementary MOS
CS	Common Source
CVD	Chemical Vapor Deposition
DG	Double Gate
DIBL	Drain Induced Barrier Lowering
D_{NW}	Nanowire diameter
F	Minimum feature size
FPGA	Field Programmable Gate Array
f_T	Unity gain bandwidth
GAA	Gate-all-around
g_{ds}	Output conductance
g_m	Transconductance
HBT	Heterojunction Bipolar Transistor
HDP	High Density Plasma
HEMT	High Electron Mobility Transistor
IC	Integrated Circuits
ITRS	International Technology Roadmap for Semiconductors
L_G	Channel Length
L_{OV}	Gate-Overlap/Underlap length
MG	Multi-Gate
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NM	Noise Margin
NW	Nanowire
R_B	Bottom electrode series resistance
RO	Ring Oscillator
R_T	Top electrode series resistance

R_{TB}	Total series resistance
S/D	Source/Drain
S/D_{ext}	Source/Drain extension length
S_B	Source as Bottom electrode and drain as top electrode
SCE	Short Channel Effects
SEM	Scanning Electron Microscopy
SGT	Surrounding Gate Transistor
SOI	Silicon on Insulator
SS	Subthreshold Slope
S_T	Source as Top electrode and drain as bottom electrode
STI	Shallow Trench Isolation
TCAD	Technology Computer Aided Design
T_{OX}	Gate dielectric thickness
T_{pHL}	High to Low delay
T_{pLH}	Low to High delay
VLS	Vapor –Liquid-Solid
VNWFET	Vertical Nanowire FET
VTC	Voltage Transfer Characteristics
θ	Mobility degradation parameter
λ	Natural scale length
λ_{CLM}	Channel Length Modulation coefficient

1 CHAPTER

INTRODUCTION

1.1 Introduction

Moore's law [1] has been followed for more than 40 years while scaling down the device dimension of planar/bulk metal oxide semiconductor field effect transistor (MOSFET). To address the scaling related issues, new process technologies such as: lightly doped drain, lateral non-uniformity in channel doping, junctionless device, strained silicon, high-κ dielectrics and metal gates have been introduced in complementary metal oxide semiconductor (CMOS) device architecture [2]–[9]. These improvements in fabrication processes have kept the technology in pace with international technology roadmap for semiconductors (ITRS) guidelines for future technology requirements [10]. However, for deca-nanometer and beyond technology nodes, the conventional MOSFET suffers severely from short channel effects (SCE) [2]. Thus the novel devices with multiple gates or 3D structures (Double Gate FET [11]–[13], Fin-FET [14]–[16], and Nanowire (NW) Gate-all-around (GAA) FET) are researched as potential replacements [2], [17]–[21]. These multiple gate devices have better scalability and electrostatic control over channel [22]–[26]. Recently, Intel corp. has reported introduction of 22 nm FinFET (3D transistor) [27]–[30] in their microprocessors named Ivy Bridge, released in 2013 [31], also Taiwan Semiconductor Manufacturing Corporation has released its production details of 28 nm and below technology node planar MOSFET [32]. Other firms like IBM, Samsung are also planning to implement FinFET below 20 nm technology node. Further for sub-50 nm nodes NWFET has been reported by industrial researchers [33]. This underlies the importance and potential of the 3D/multigate or novel devices to extend existing MOSFET scaling limits.

The evolution of MOSFET from single gate through multi-gate to gate all around (GAA) structure having improvement in electrostatic control is shown in Figure 1.1 [25]. In Figure 1.1, double gate FET has the following salient features 1) better SCE control when compared to single gate planar FET due of presence of two gates, 2) tight electrostatic coupling of the gate with the channel due to thin silicon film. These features provide the advantage of: 1) reduction in SCE, resulting in allowable channel length to be much shorter when compared to planar FET, 2) near ideal value of sub-threshold slope SS (~ 60 mV/dec when compared to > 80

mV/dec for planar FET), which allows gate overdrive to be large for the same off- state current and the same power supply and 3) better carrier transport is observed with reduced channel doping [2].

Among the important 3D or non-planar structure family, the FinFET is considered to be the first member. It is named so, as the silicon channel is etched into the wafer surface like a fin [2]. The fabrication of the FinFET device begins with the formation of a fin obtained by patterning and etching on an SOI/bulk substrate using a hard mask, which is retained throughout the fabrication process. The other derivative devices such as tri-gate, Pi-gate, Ω-gate are similarly produced. It is reported that the drive current of FinFET devices rival those of best conventional planar devices [34]–[40]. Despite the non-planar/unconventional device structure and topology, the presence of more than a single gate leads to increase in electrostatic coupling of gate and channel, thus the minimum gate length achieved is among the shortest [2], [41]–[46].

Due to multiple gates in GAA structure, this device architecture is the most effective for better electrostatic control of the channel charge and is resistant to SCEs [25]. One major problem with scaling of planar CMOS is the requirement to shrink gate oxide thickness, which causes increase in tunneling leakages. It is observed that, NW GAA FET can be scaled without proportionally reducing the gate dielectric thickness [47]. Thus, the NW GAA FET is the best device for deca-nanometer dimensions [48].

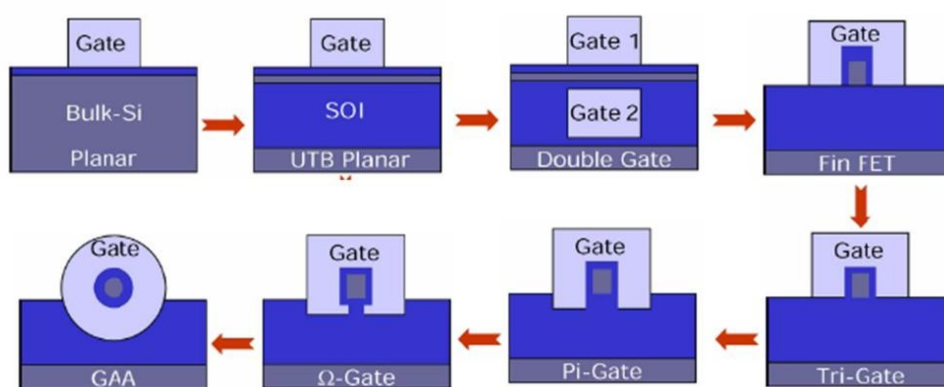

Figure 1.1 Evolution of device structure from single-gated to GAA NWFET [25]**.**

Nanowires can be obtained by two different fabrication approaches namely: the bottom–up approach and the top–down approach [25]. The bottom up approach is a non-lithographic method in which vapor-liquid-solid (VLS) mechanism is employed using a suitable catalyst and chemical vapor deposition process to produce nanowires. However, these nanowires are

randomly distributed and additional processing steps are necessary to assemble them into functional devices. The top-down approach is a CMOS compatible process and is lithographically used to define the orientation and location of nanowire with respect to wafer surface, thus resulting in two types of devices: 1) vertical pillar nanowires and 2) lateral nanowires [25], [49]–[54].

Between the two types based on orientation of nanowire with respect to surface, the lateral nanowire type follows process steps similar to FinFET. But it employs an additional step after the Si fin formation, which is to convert the rectangular fin to a cylindrical wire structure. It is achieved by first etching away a part of the buried oxide or etching the dummy layer (introduced so that the fin can be released in air) and then oxidizing the fin. This is followed by an oxide etching to release the nanowire which is supported at its ends by the source/drain pads as shown in Figure 1.2.

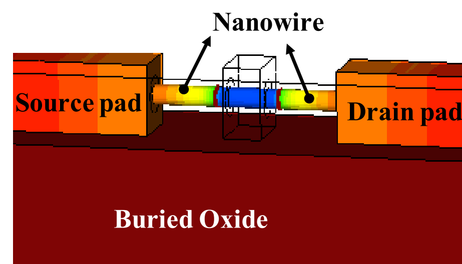

Figure 1.2 3D device structure of lateral nanowire supported by source/drain pads at its ends [55].

Vertical nanowire structure shown in Figure 1.3 follow different process steps than used for lateral nanowire device. The first step involves formation of vertical pillar structure by selective deep etching of silicon with hard mask resist dots [56]. In this device structure substrate acts as source, the nanowire tip acts as drain and channel in between them. Also source and drain electrodes can be interchanged. The gate around the nanowire channel is obtained by special processing steps, which will be presented in detail in next chapter.

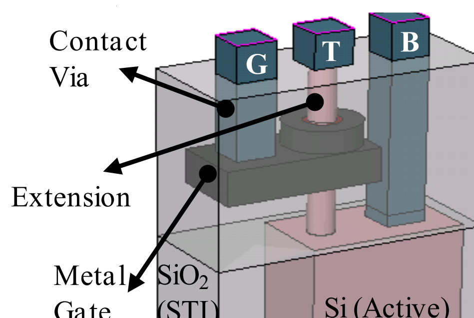

Figure 1.3 3D isometric view of Vertical Nanowire device [57].

In this thesis, the studies on design and analysis of vertical silicon nanowire gate all around FET (NW GAAFET) devices and circuits are presented. The device structure used is a modified version of VNW structure reported by Yang et al. [56].

1.2 Motivation

Among the different 3D device structures discussed in the previous section, the vertical NW GAA FET has the best SCEs performance due to multiple gate structure and also occupies the least silicon wafer area owing to its vertical architecture. Thus, ultra dense integrated circuits (IC) for high performance applications can be obtained using these devices.

Further, the VNW GAA FET devices can be fabricated in vias, which is a step towards reconfigurable logic which can be widely used in field programmable gate arrays (FPGA) and can also be used to introduce logic functions in interconnects [58]. This improves performance in terms of area, delay and power. Furthermore, the VNWs also have good potential to realize high sensitivity chemical [59] or bio sensors [60]–[63], gas sensors [64] and solar cells [65].

From the extensive literature survey presented in chapter 2, we find that the vertical nanowire device performance with respect to various device dimensions is necessary for optimization. The impact of device asymmetry and different layouts arising thereby are not yet studied. Also, the impact of parasitic on device and circuit performance needs to be quantified in terms of various parasitic components, which can be estimated by developing appropriate models.

Thus, the literature gaps/issues and the advantages of VNW GAA FET listed above have motivated us in carrying out detailed device and circuit analysis in this work. The work has been extensively carried using 3D TCAD simulator i.e., Sentaurus (version 2009.10), which is the state of the art virtual fabrication and characterization software package supplied by Synopsys Inc. [66].

The work presented in this thesis addresses optimization of VNW device and presents various circuit design issues when working with VNW devices. This can be used by device and circuit engineers in industry to take a leap forward in developing low power memory applications, digital logic and analog circuit design.

1.3 Objectives

In this thesis, work has been carried out on device and circuit performance of vertical nanowire (VNW) silicon MOSFET compatible with CMOS technology. The study has the following objectives:

1. Thorough analysis of vertical nanowire device in terms of performance parameters (I_{ON}/I_{OFF} ratio, SS, drain induced barrier lowering - DIBL) at sub 45nm channel lengths, where the series source/drain resistance and parasitic capacitances are expected to affect the device performance significantly.

2. To evaluate device performance and process variation, the impact of device parameters such as channel length, wire diameter, source/drain asymmetry and S/D extension region length (S/D_{ext}) on device characteristics.

3. A comprehensive parasitic model for resistance and capacitance, which can take into account the device asymmetry and cylindrical structure is developed for VNW device. Further, the device I-V modeling is realized with n^{th} power law [67].

4. Finally, thorough circuit analysis is carried out, in order to demonstrate the better circuit performance potential of VNW devices. Firstly, performance of digital circuits [68], [69]with the help of CMOS inverter is investigated considering some of the device scaling parameters & the impact of source/drain asymmetry, and different layouts arising thereby. Secondly, the nth power law and parasitic capacitance models are used to analyze the delay trends. Finally, analog performance [70]of VNW device is analyzed using common-source (CS) amplifier to complete the study. We highlight the better performance of VNW CMOS by comparing and benchmarking the results with reported FinFET/planar technologies.

1.4 Thesis Organization

This thesis is organized into different chapters as below:

Chapter 1: In this chapter, introduction is presented with brief highlights of technological advancements in the field of MOSFET devices to date. Further, the motivation arising out of technical gaps/issues and advantages of using VNW devices are presented. Finally the various objectives addressed through this thesis are pointed out along with thesis organization details.

Chapter 2: This chapter provides detailed literature review of MOSFET device evolution along with the need and advantages of VNW device. The technical gaps in the existing literature on VNW device performance, device modeling, digital and analog circuit performance are discussed. The chapter is concludes with a brief summary of technical gaps to be addressed in the thesis.

Chapter 3: In this chapter, TCAD details of implemented VNW MOS structures, simulation models and related tools are discussed. A well calibrated TCAD simulation setup is established. This is carried out by creating an equivalent structure of reported device [56] and [52] to match the I-V characteristics at low and high V_{DS}. This also includes selection of appropriate physical models for carrier transport, velocity saturation, contact resistance, surface and bulk scatterings, along with quantization effects. Finally, the complete details of device and important model parameters, which are used in simulations carried in this thesis work is presented. This is followed by details of simulation setup such as DC sweep parameters, AC parameters for device analysis and transient parameters for circuit analysis.

Chapter 4: This chapter deals with the VNW device performance in terms of I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, SS, DIBL with channel length scaling from 45 to 15nm, for both NMOS and PMOS. Important results, such as $I_{ON}/I_{OFF} > 10^4$, SS ~ 60 – 70 mV/dec and DIBL < 30 mV, highlight greater control of short channel effects due to surrounding gate architecture. For 15nm channel length devices, performance is analysed in terms of wire diameter variations, source/drain asymmetry and S/D_{ext} length. This study highlights importance of achieving matched drive currents for NMOS and PMOS, which differ by a non integral factor (~ 1.4) with the help of single nanowire devices, as opposed to multi nanowire/fins required in lateral novel devices. Finally, the device I-V characteristics are modeled with nth power law, which will be employed later in circuit delay prediction. The chapter concludes with highlights of the important device performance parameters found.

Chapter 5: This chapter focuses on modeling of parasitic resistance and capacitance present in VNW devices. In these models, the inherent device asymmetry and device structural topology such as the cylindrical gate, rectangular vias, gate extension and contact pad overlapping the tip of nanowire are considered. Further, the impact of device scaling on these parasitic components is thoroughly investigated, and emphasis is given on the major parasitic contributors. The results depicts that nearly 50% of the total series resistance is contributed by the metal semiconductor contacts and the total parasitic capacitance is nearly 1.5 to 2 times the channel

capacitance. This chapter ends with the highlights of the important aspects of parasitic modeling and its importance in compact modeling.

Chapter 6: This chapter discusses the circuit performance of VNW devices in detail. The digital circuit performance is carried out with CMOS inverter circuit with device scaling and is benchmarked with existing literature for FinFET and planar CMOS inverters. The results show better performance of VNW based circuits and justify its usefulness in low power applications. For 15nm VNW devices, complete performance analysis of CMOS inverter is presented with respect to S/D extension length, S/D asymmetry and impact of different layouts arising thereby. The results show ~65% better delay performance by devices with drain at top as compared to devices with drain at bottom. Moreover, detailed insight into static characteristics of VNW CMOS inverter and the use of S/D_{ext} as tuning parameter to obtain required gain and noise margin is presented provided.

Further, analog performance of 15nm VNW device are analysed for intrinsic device and common-source amplifier in terms of performance metrics such as gain, 3dB bandwidth and unity gain bandwidth (f_T), and are compared with FinFET technologies at same node. It is observed that VNW devices have nearly 40% higher gain and 66% higher f_T when compared to equivalent FinFET device. In a VNW device the impact of extension length and number of nanowires over gain of intrinsic device and CS amplifier is studied. Also, the position of gate can be used to obtain VNW based amplifier with required gain and f_T. The chapter ends with a summary of important circuit performance metrics and guidelines.

Chapter 7: This chapter concludes the present study and results obtained. Further, recommended research directions for future investigations are also discussed.

2 CHAPTER

LITERATURE SURVEY

In the previous chapter, introduction to the thesis is presented with an emphasis on VNWFET. In this chapter the VNWFET literature is discussed, and research gaps which are investigated in this thesis are identified. The scaling theory of MOSFETs and best scaling performance of NWFETs are briefly described. It is followed by discussion on different fabrication approaches reported in literature for VNWFET. The various silicon data related to NWFET are presented from literature with comparison to state of the art FinFET and planar devices. Further, we briefly highlight different models proposed for NWFET current-voltage and capacitance-voltage characteristics. We then present various circuit performance metrics reported in literature for VNWFET. Then we highlight the advantages of using vertical nanowire structures through various reported applications such as CMOS, tunnel FET, SONOS memory, etc. Finally, the chapter is concluded by identifying research gaps to be addressed through this thesis.

2.1 Scaling Theory

C.P. Auth *et al.,* [71] have presented the scaling theory of GAA MOSFET considering cylindrical form of Poisson's equation, assuming a parabolic potential in radial direction. They have compared scaling theory of cylindrical MOSFET with the double gate (DG) MOSFET [72], and observed nearly 40% improvement in minimum effective channel length for cylindrical MOSFET. The scaling theory of cylindrical MOSFET as proposed by Auth *et al.*, is as follows:

A parabolic solution is assumed for the potential, $\Phi(r,z)$, in cylindrical co-ordinates as:

$$\emptyset(r,z) = c_0(z) + c_1(z)r + c_2(z)r^2 \qquad \textbf{(2.1)}$$

to find the solution of Poisson's equation in cylindrical co-ordinates represented as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\emptyset(r,z)\right) + \frac{\partial^2}{\partial z^2}\emptyset(r,z) = \frac{qN_a}{\varepsilon_{si}} \qquad \textbf{(2.2)}$$

where N_a is the uniform channel doping.

The following three boundary conditions are necessary to obtain a solution:

1) The center potential (Φ_c) is independent of radius term and varies as a function of z

$$\emptyset(0, \mathrm{z}) = \emptyset_{\mathrm{c}}(\mathrm{z}) = \mathrm{c}_0(\mathrm{z}) \tag{2.3}$$

2) Due to cylindrical geometry the electric field in the center of the nanowire is zero

$$\frac{\mathrm{d}}{\mathrm{dr}} \emptyset(\mathrm{r}, \mathrm{z})|_{\mathrm{r}=0} = 0 = \mathrm{c}_1(\mathrm{z}) \tag{2.4}$$

3) Using the gate potential (Φ_{gs}) and surface potential (Φ_s), the electric potential at Si/SiO_2 interface is given as

$$\frac{d}{dr} \emptyset(r, z)|_{r=\frac{t_{si}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \left(\left(\emptyset_{gs} - \emptyset_s(z) \right) / \left(\frac{t_{si}}{2} \ln \left(1 + \frac{2t_{ox}}{t_{si}} \right) \right) \right) = t_{si} c_2(z) \tag{2.5}$$

The solution of potential after eliminating surface potential is given by

$$\emptyset(r, z) = \emptyset_c(z) - \left(\left(2\varepsilon_{ox} r^2 \left(\emptyset_c(z) - \emptyset_{gs} \right) \right) / \left(\varepsilon_{si} t_{si}^2 \ln \left(1 + \frac{2t_{ox}}{t_{si}} \right) + \frac{\varepsilon_{ox} t_{si}^2}{2} \right) \right) \tag{2.6}$$

Using the above potential, solution of the Poisson's equation at the nanowire centre $r = 0$ is given by

$$\frac{\partial^2}{\partial z^2} \emptyset_c(z) - \left(\emptyset_c(z) - \emptyset_{gs} \right) / \lambda^2 = q N_a / \varepsilon_{si} \tag{2.7}$$

where λ is known as the natural scale length and it governs the scaling limit of devices with better sub-threshold behavior and is given by

$$\lambda = \sqrt{\left(2\varepsilon_{si} t_{si}^2 \ln \left(1 + 2\frac{t_{ox}}{t_{si}} \right) + \varepsilon_{ox} t_{si}^2 \right) / 16\varepsilon_{ox}} \tag{2.8}$$

The minimum channel length obtained is given by $L_{min}= 2\alpha\lambda$. The scaling parameter α is kept constant to maintain constant SS and DIBL. For typical values of t_{ox}=1 nm and t_{Si}=5 nm, the values of λ and L_{min} for GAA, silicon on insulator (SOI) and DG SOI [73] devices are tabulated in Table 2.1. It is clear from the table that for given constraints i.e., gate dielectric thickness and silicon thickness, GAA or NW structure can achieve minimum channel length devices.

Hence, scaling theory justifies the ultimate scalability of NW devices and, thus it can address the scaling limitations posed by planar MOSFET.

Table 2.1 Natural scale length and minimum channel length of different devices.

Device	Natural scale length (λ)		α	L_{min}(nm) = 2αλ
SOI [73]	$\lambda = \sqrt{t_{Si}\, t_{ox} \frac{\varepsilon_{Si}}{\varepsilon_{0x}}}$	3.91 nm	5	39
DGSOI [72]	$\lambda = \sqrt{\frac{\epsilon_{Si}}{2\epsilon_{0x}}\left[1 + \frac{\epsilon_{ox}\, t_{Si}}{4\epsilon_{Si}\, t_{ox}}\right] t_{Si}\, t_{ox}}$	3.28 nm	3	20
GAA [71]	$\lambda = \sqrt{\frac{2\epsilon_{Si}\, t_{Si}^2 \ln\left[1+2\frac{t_{ox}}{t_{Si}}\right] + \epsilon_{ox}\, t_{Si}^2}{16\epsilon_{ox}}}$	2.18 nm	2.3	10

2.2 Device Fabrication

GAA devices are classified into two, based on nanowire orientation: 1) Lateral nanowire type and 2) Vertical pillar type. Most of the reported data *Singh et al.* [74], *Jiang et al.* [33], *Yeo et al.* [75], *Singh et al.* [25], and *Rustagi et al.* [53] are for lateral NWFET with better raw materials and fine tuned process steps. Ultra short channel (sub 45nm) lateral NWFET devices have been reported by *Yeo et al.* [75] (Lg = 15nm), and *Jiang et al.* [33] (sub 10nm) with excellent device performance. The devices have exhibited ideal values for SS ~65 and ~70 mV/dec for NMOS and PMOS, respectively. DIBL of less than 50 mV/V proves the minimal presence of SCE's. Also, the I_{ON}/I_{OFF} of ~ 10^6 to 10^7 has been reported. These three device performance parameters satisfy the stringent SCE constraints suggested by *Gnani et al.* [47]. Thus, it is possible to obtain deca-nanometer Vertical NWFET devices with excellent device performance by fabricating the device in epitaxial grown silicon layer and fine tuned process steps.

Vertical NWFET occupies least silicon area due to its vertical architecture when compared to a lateral NWFET which occupies similar area as FinFET or double gate device. The vertical FET has been reported in 1991 by *Takato et al.* [76]. The proposed surrounding gate transistor (SGT) has been implemented using a 1-2 µm height pillar with effective channel length of 0.8 µm and thickness 1 µm. The process steps (shown in Figure 2.1) involved are:

- pillar formation by silicon etching
- wet etching and sacrificial oxidation to remove surface damages

- 20 nm gate oxide growth and polysilicon deposition and patterning
- source/drain implantation and metallization

Takato et. al. [76] reported that, due to vertical topology the device occupies ~ 40-50% lesser silicon area.

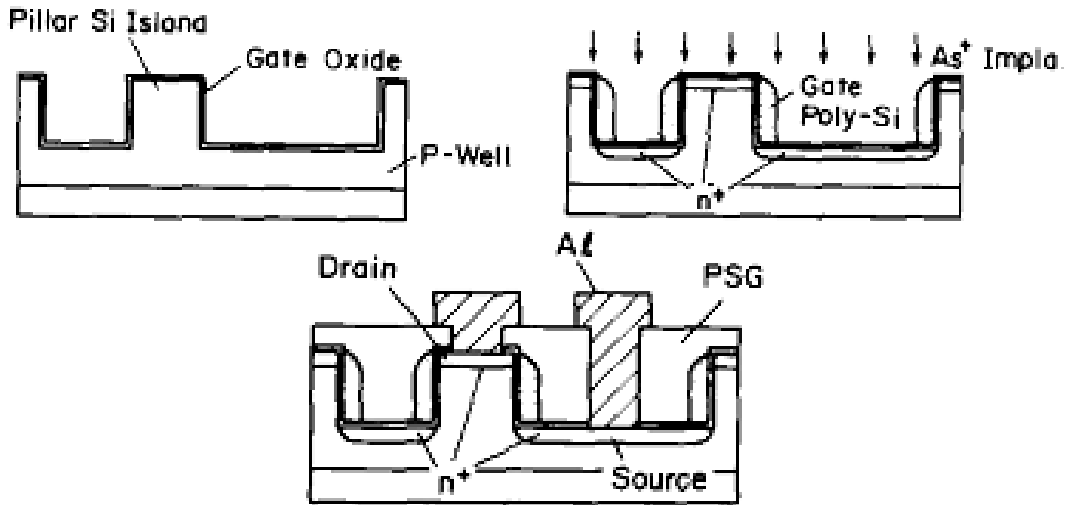

Figure 2.1 Fabrication flow of SGT [76].

Another novel way of obtaining vertical NWFET has been reported by *Jayanarayanan et al.* [77] shown in Figure 2.2. A p type Si wafer is taken as substrate and then source, channel and drain layers were grown through chemical vapor deposition (CVD) process. Subsequently, a reactive ion etch process was used to define the mesa of the vertical MOSFET. Then a 10 nm silicon cap was grown by CVD before growing 4 nm gate oxide by wet oxidation at 750°C. This was followed by 100 nm polysilicon and ion implantation. The rest of steps are similar to planar MOSFET like isolation oxide deposition, contact etching and metallization.

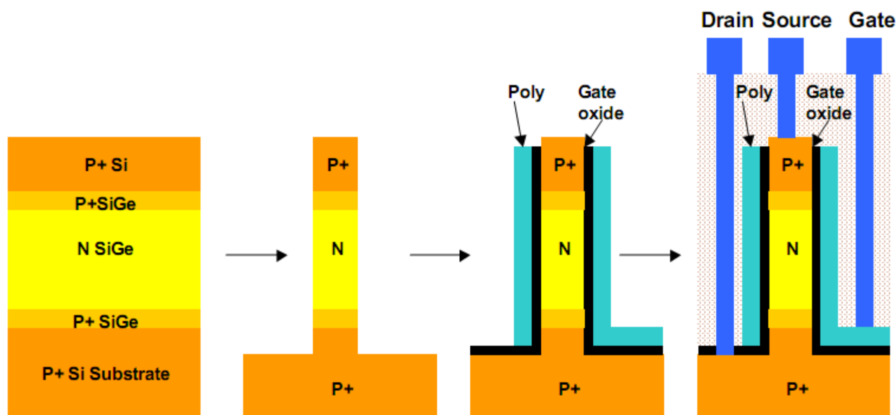

Figure 2.2 Process flow of vertical MOSFET [77].

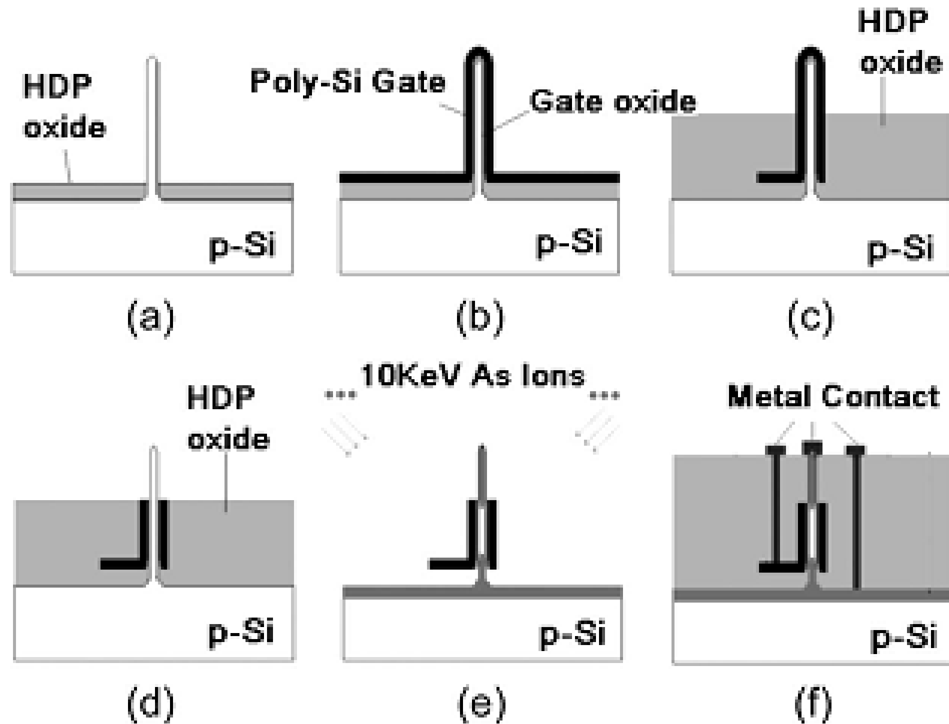

Figure 2.3 Process flow for pillar and transistor formation [78].

The process steps of [76] have been further refined by *Yang et al.* [78] as shown in Figure 2.3 and are as follows: a) patterning circular resist dots of different diameters (from 160 to 600 nm) on the bulk Si wafer followed by 1-µm deep Si etch under hard mask. Oxidation of pillars is done at 1150°C to convert them into nanowires. After vertical nanowire formation the grown oxide is stripped. A high-density plasma (HDP) oxide of 250 nm thick is deposited, followed by wet chemical etch-back. Due to the non conformal deposition a thicker oxide at the bottom surface and thinner oxide along the nanowire sidewalls is obtained. A 150-nm thick oxide is retained covering the foot of vertical wire using wet etch back technique. This process step is done to seperate the gate electrode from source extension pad reducing the gate to source fringing capacitance. b) 5 nm thick gate oxide is thermally grown on the vertical wire surface, followed by 30-nm poly-Si deposition, to serve as the gate electrode. Then the gate pad is patterned and etched under resist mask which covers the nanowire and provide a extension region of poly-Si for gate contact. c) The process of HDP oxide deposition followed by wet etch back is repeated to access the polysilicon on top of nanowire while protecting the gate pad defined earlier. d) Poly-Si is then isotropically etched. e) This is followed by complete removal of oxide through wet etch process and Arsenic is implanted. Due to gate extension pad, shadowing effect is anticipated at the bottom of the pillar. It is found, however that a rapid thermal annealing at 1000°C/10 s is enough for dopants to diffuse across the shadowed region,

effectively eliminating the offset in the shadowed region. f) The fabrication process ends with standard metallization. The detailed structure can be observed in the scanning electron microscope (SEM) image shown in Figure 2.4.

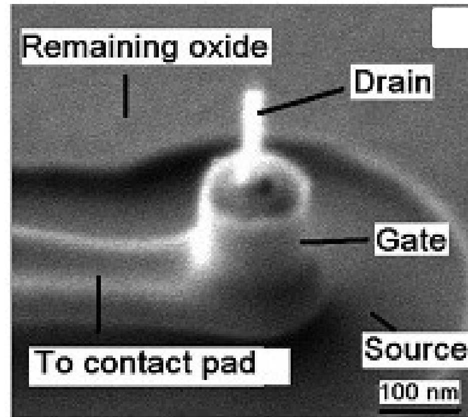

Figure 2.4 SEM image of vertical NWFET [78]**.**

The methods reported by *Takato et al.*[76], and *Yang et al.*[78] result in device where the bottom nanowire extension (nanowire below the gate region) suffers due to the shadowing effect of gate extension during ion implantation. Thus the bottom extension is not optimally doped. This increases the series resistance and results in asymmetric device with respect to source/drain contacts. Also, the other source of asymmetric behavior is due to device parasitic capacitances. We have realized such a device in Sentaurus TCAD simulation tool and analyze the impact of device asymmetry on device and circuit performance.

2.3 NW Circuit Performance

The NWFET device performance rivals the present state of art FinFET and planar devices reported by *Chiarella et al.* [79], *Datta et al.* [80] and *Hoffmann et al.* [81], *Pouydebasque et al.*[82] respectively.

Takato et al. [76] first reported long channel SGFET device performance parameters in comparison to planar MOSFET for similar device dimensions (W=4μm, L=1μm). The obtained I-V characteristics are close to each other. Further it is shown that the SS is 72 and 98 mV/dec for SGFET and planar respectively, with nearly equal threshold voltage. In SGFET it is also

shown that the device performance is not dependent on substrate bias, as observed in planar MOSFETs.

Yang et al. [78] fabricated short channel (120-150nm) Vertical NWFET showing excellent transistor characteristics with large drive current per wire, high Ion/Ioff ratio (~ 10^7), good SS (~ 80mV/dec) and low DIBL (~ 25mV/ V) for both NMOS and PMOS. These devices showed excellent performance. The device asymmetry observed in I-V characteristics was attributed to be arising due to top contact on nanowire and bottom contact on active area acting as source/drain interchangeably.

Le et al. [83] demonstrated inverter with vertical nanowire transistors for the first time. Device with channel length of 90nm and diameter ~30nm have been fabricated with high I_{ON}/I_{OFF} ratio of > 10^6, low SS ~ 100 mV/dec (as the device is made out of polysilicon), and reasonable DIBL ~50 mV/V. The inverter based on the poly-Si NWTFTs (with a dimension ratio between N- and P-NWFETs of 1:1) exhibits excellent performance even with reduced V_{DD} ~0.2 V, showing good transfer characteristics and low switching currents.

2.4 NW Modeling

Evaluation of circuit performance using device model requires current-voltage and capacitance-voltage relations of nanowire device.

Jiménez and *Iñiguez* group [84]–[89], and *Yu et al.* [90] reported current-voltage model for NWFETs, which are applicable for undoped or lightly doped channels. However, in practice NWFET always have a doped body structure due to technology requirements and due to unintentional doping during real fabrication process. *Liu et al.* [91] proposed an implicit model for long-channel SGMOSFETs with intrinsic channels to heavily doped bodies. These models [85], [87], [90], [91] fail to explain SS > 60 mV/dec (due to the presence of interface-trap charges) observed in practical devices. *Yu et al.* [92] proposed an implicit and continuous charge-control model for cylindrical doped n-channel NWFETs that included interface-trap charges. All these models are developed for the gate-channel region of a NWFET without considering the series Source/Drain resistance arising due to narrow nanowire extensions, contact resistance, gate topology, device asymmetry etc.

The capacitance-voltage dependence is used to quantify the parasitic capacitance components (gate-source, gate-drain, and source-drain) present in a device. Two different methodologies

have been used to quantify the parasitic capacitance. *Yu et al.* [90] used charge based approach to model the capacitances. *Zou et al.* [93] proposed models based on 3-D electrostatic calculations for the gate to nanowire extension outer fringing component, the gate to source/drain pads, gate to source/drain sidewall capacitance, the overlap capacitance and the inner fringe component between the end of source/drain extension region and the inner surface of gate. Though these models are good in predicting parasitic device capacitance of NWFET, still they cannot be used for the VNW device which will be analysed in this thesis. This is due to model inability to consider cylindrical gate geometry and the capacitance components arising there by.

2.5 Vertical NW Circuit Performance

The circuit evaluation using vertical NWFET has been reported by many authors. *Hamedi-Hagh et al.* [94] presented design and characterization of vertical nanowire based differential pair amplifier using BSIM-SOI equivalent model. The amplifier provides 5THz bandwidth with a voltage gain of 16 and a distortion better than 3%. *Bindal et al.* [95] used similar equivalent model of undoped vertical NWFET to analyze transient circuit performance, power dissipation and layout area of inverter, 2- and 3-input NAND, NOR, XOR gates, and full adder circuits. The inverter threshold is 410mV which is due to slightly higher drive current in NMOS devices. The worst case delay of an inverter with a load of 200aF is ~16ps. Both [94] and [95] have verified their modeling results with Silvaco's ATLAS device design tool.

2.6 VNWFET Other Applications

Vertical nanowires are not only useful in obtaining a MOS based high density logic circuits, but it is also used to realize various other devices such as III-V vertical NWFET [96]–[108], tunnel FET [109]–[113], DRAM cell [114]–[117] and SONOS memory [118]–[122]. *Chen et al.* [110], and *Gandhi et al.* [109] proposed conversion of vertical NWFET to a Tunneling FET to obtain SS < 60mV/dec. *Endoh et al.* [117], and *Goebel et al.* [115] presented stacked SGFET architecture to realize DRAM memory cells which reduces the area requirement due to vertical stacking of devices. *Sun et al.* [123], and *Chen et al.* [118] have realized flash/SONOS memory cell using vertical Si nanowires.

Further, Sun et al. reported 2bit storage per memory cell. *Huang et al.* [124] experimentally demonstrated current mirrors based on vertical transistors. *Gaillardon et al.* [58] reported an innovative application of vertical nanowire transistors i.e., reconfigurable logic circuits such as FPGAs. In this they have embedded logic functionality in between metal lines, to reduce the routing overhead. Thus, an area saving of 46.2% and delay reduction of 42% are reported.

2.7 Technical Gaps

Based on the literature survey it is observed that the gate-all-around devices are promising devices for deca-nanometer technology nodes. Further, the VNW FET has the added advantage of occupying least Si area for a given functionality in various applications. Hence, it is necessary to carry out comprehensive scaling study to ascertain device and circuit performance using VNWFET. An equivalent model of the device needs to be obtained, which can be used to predict the circuit performance in a smaller amount of time. The following technical gaps are to be addressed:

- Long channel vertical nanowire devices have been reported by many researchers [76], [78], [83]. *The vertical nanowire device performance parameters (I_{ON}/I_{OFF} ratio, SS, DIBL) at sub 45nm channel length where the series source/drain resistance is expected to affect the device performance significantly* is not reported.
- The impact of device parameters such as *channel length, wire diameter variations, source/drain asymmetry and doping, length of S/D extension region on device performance* is not studied extensively.
- The impact of *source/drain asymmetry, source/drain extension length and different layouts* on circuit performance has not been reported.
- Gate-all-around/nanowire device I-V models are reported [85], [87], [90]–[92] without considering the source and drain series resistances. The parasitic capacitance modeling of GAA devices considering circular gate is also lacking. *Hence a comprehensive model which can take into account the asymmetric series resistance in case of device I-V model and parasitic capacitance considering circular gate and asymmetric source-drain electrodes is* needed.
- D*esign and performance of VNWFET based SRAM cell and its comparison with FinFET or Planar technology* is not reported.
- D*esign and performance of VNWFET based analog circuits* is not reported.

- Standard cell library consisting of inverter, NAND, NOR, and SRAM blocks for Vertical nanowire device is not available.

Through this thesis we address most of the major research gaps identified above.

3 CHAPTER

TCAD CALIBRATION

In this chapter, the importance of carrying this study using Sentaurus Technology Computer Aided Design (TCAD) [66] tools is discussed. Then, a well calibrated TCAD simulation setup is established. This is achieved by simulating an equivalent structure of reported device [78] and match the reported I-V characteristics. This also includes selection of appropriate physical models for carrier transport, velocity saturation, contact resistance and surface & bulk scatterings, along with quantization effects. Finally, the complete details of device and important model parameters, which are used in simulations related to the thesis work is presented, followed by a brief discussion on simulation setup for various device and circuit analysis techniques.

3.1 Technology Computer Aided Design: TCAD

Technology Computer-Aided Design (TCAD) software's are used for carrying out simulations on computer for development and optimization of semiconductor processing technologies and devices. TCAD simulation tools solve diffusion and transport equations with inclusion of various physical effects on device geometry discretized through meshing. The physical approach is the reason for accurate results through TCAD simulations and also matches well with actual fabricated device data.

TCAD simulations can be therefore used for reducing the cost and time consumed in test wafer runs while developing or characterizing a new device or technology, speeds up the research and development process. Moreover, semiconductor companies use TCAD for integrated circuits (IC) process variation analysis, by monitoring, analyzing, and optimizing their IC process flows.

TCAD simulations are of two types: process simulation and device simulation.

3.1.1 Process Simulation

In process simulation, a flow of actual fabrication procedure is created with the processes like deposition, etching, oxidation, ion implantation, and thermal annealing [125]. These are then simulated based on the physical equations governing the respective process. Through meshing the simulated part is discretized and represented as a finite-element structure shown in Figure 3.1.

For example, in the simulation of ion implantation followed by annealing the ions are first implanted with specific energy which determines the dopants peak concentration position and dose which determines the peak concentration value. When the annealing process is performed the dopants diffuse and provide required dopant profile. In Figure 3.1 we show the doping profile of source region under the spacer.

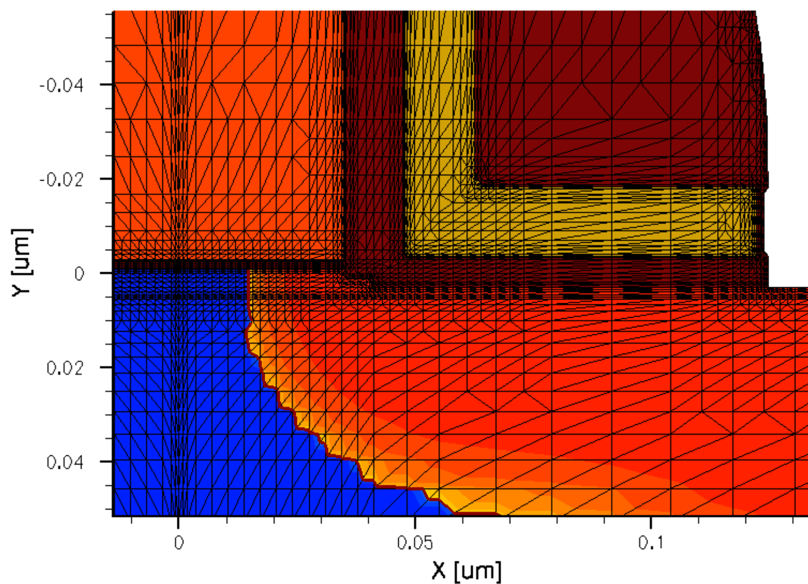

Figure 3.1 Finite element grid magnified at gate-drain corner of an NMOSFET [66].

Sentaurus TCAD has another attractive option to create device structures known as the structure editor. In this a device can be created in no time as there is no process steps actually involved. In this the user splits the device into multiple regions and each region is appropriately placed along with its material type. It is followed by definition of doping properties of each region using constant profile, analytical (Gaussian or error function) profile or user defined profile placement commands. Finally, the device structure is discretized using meshing commands and mesh engine. Figure 3.2 shows a SOI MOSFET device created using the structure editor [66].

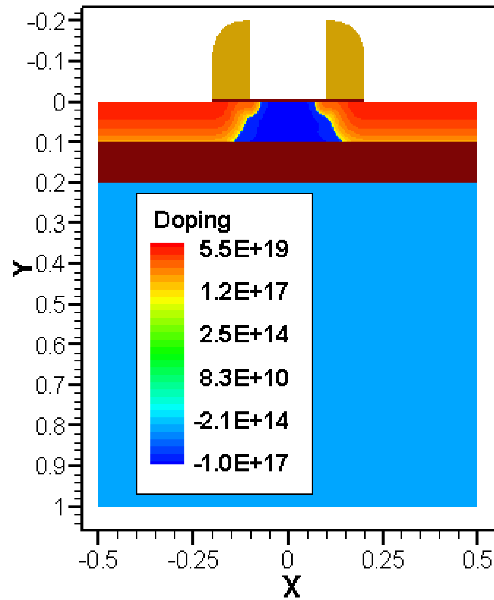

Figure 3.2 2D SOI MOSFET obtained using structure editor [66]**.**

3.1.2 Device Simulation

Device simulations are like virtual measurements of the electrical characteristics of a device, such as a transistor or diode. The device is represented as a meshed finite-element structure. Each node of the device has properties associated with it, such as material type and doping concentration and the properties like the carrier concentration, current densities, electric field, carrier mobility, and so on are computed. Electrodes represent areas on which boundary conditions, such as voltage, contact resistance or workfunction are defined. In Figure 3.3 we show a simulated MOSFET device highlighting the current density in the device for given bias condition [66].

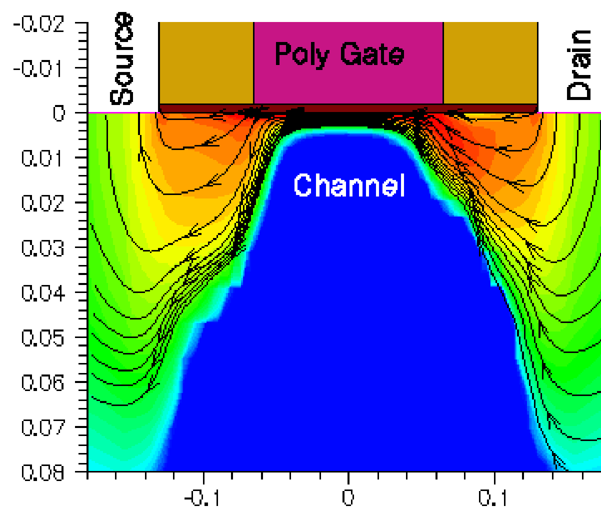

Figure 3.3 Current flow lines in a 0.13-µm NMOSFET at V_{gs} = 1.5 V and V_{ds} = 3.0 V; shading represents current density [66]**.**

The device simulator solves the Poisson equation [66][126], which is:

$$\nabla \cdot \left(\varepsilon \nabla \emptyset + \vec{P}\right) = -q(p - n + N_D - N_A) - \rho_{trap} \quad \textbf{(3.1)}$$

where ε is electrical permittivity, $\vec{P}$ is ferroelectric polarization, q is electronic charge, n and p are electron and hole densities, N_D and N_A are concentration of ionized donors and acceptors, ρ_{trap} is the charge density of fixed charges and traps.

The electron and hole densities are computed from electron and hole quasi-Fermi potentials [66][126]. If Fermi statistics is assumed, the formulas are:

$$n = N_c F_{1/2}\left(\left(E_{F,n} - E_c\right)/kT\right) \quad \textbf{(3.2)}$$

$$p = N_v F_{1/2}\left(\left(E_v - E_{F,p}\right)/kT\right) \quad \textbf{(3.3)}$$

where N_C and N_V are effective densities of states, $E_{F,n}$= $-q\Phi_n$ and $E_{F,p}$= $-q\Phi_p$ are the quasi-Fermi energies for electron and holes, Φ_n and Φ_p are quasi-Fermi potentials of electron and holes and E_C and E_V are the conduction and valence band edges. $F_{1/2}$ is the Fermi integral of order ½. k is Boltzman's constant and T is device temperature in $°K$.

The carrier continuity equations which include the carrier transport models [66][126] for semiconductors are:

$$\nabla \cdot \left(\overrightarrow{J_n}\right) = -qR_{net} + q(\partial n/\partial t) \quad \textbf{(3.4)}$$

$$-\nabla \cdot \left(\overrightarrow{J_p}\right) = qR_{net} + q(\partial p/\partial t) \quad \textbf{(3.5)}$$

where, R_{net} is the net recombination rate, $\overrightarrow{Jn}$ and $\overrightarrow{Jp}$ are the electron and hole current densities.

Based on requirement and device being considering one can choose from four transport models Drift-diffusion, Thermodynamic, Hydrodynamic and Monte Carlo. After solving the Poisson equation along with continuity equation with a particular transport model, the resulting electrical currents at the contacts are extracted as shown in Figure 3.4 [66].

Semiconductor devices can be simulated using Sentaurus device to do electrical, thermal and optical characterization. It is the leading device simulator and handles 1D, 2D, and 3D geometries, mixed-mode circuit simulation with compact models, and numeric devices. Sentaurus Device is used to evaluate and analyse how a device works, to optimize devices, and to extract SPICE models and statistical data early in the development cycle. Applications of Sentaurus Device include very deep submicron silicon, where Sentaurus Device has proven

accuracy to well below 100-nm technology; SOI devices, where Sentaurus Device is known for its robust convergence and accuracy; double-gate and FinFET devices, where quantum transport is a reality; SiGe; thin-film transistors; optoelectronics; heterojunction high electron mobility transistor (HEMTs) and heterojunction bipolar transistor (HBTs), and power and RF semiconductor devices.

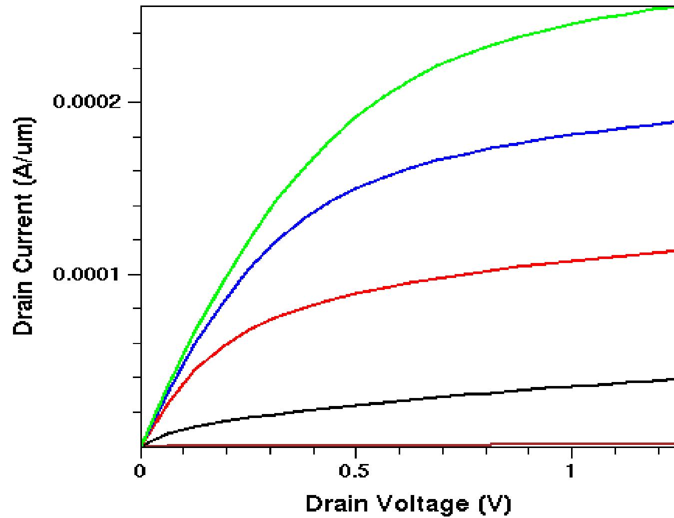

Figure 3.4 Drain current as function of drain voltage for a 50-nm NMOSFET at V_{gs} = 0.25, 0.5, 0.75, 1.0, and 1.25 V [66].

3.2 Calibrated Simulation Setup

In this thesis work the VNWFET device are obtained using the Sentaurus structure editor as shown in Figure 3.5 and a sample of VNWFET structure code is given in Appendix A. First, device is created with reported device dimensions and process details (25 nm diameter NW, 5 nm gate oxide, 150 nm channel length, 150 nm bottom extension and 500 nm top extension)as reported by Yang et.al. [5].

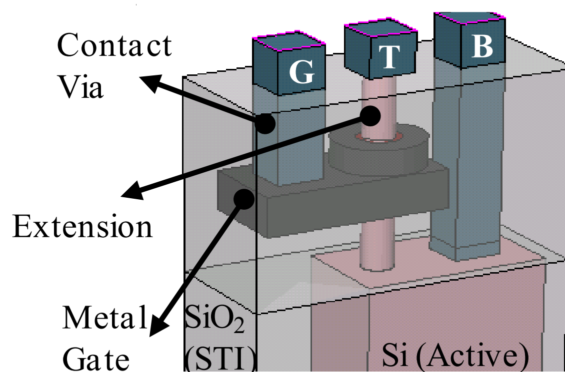

Figure 3.5 3D isometric view of Vertical nanowire device [127].

The following physics models are considered during the simulation: Drift-diffusion transport models as given below, is used along with Poisson and Fermi statistics.

$$\vec{J_n} = \mu_n(n\nabla E_c - 1.5nkT\ \nabla ln m_n) + D_n(\nabla n - n\ \nabla ln\gamma_n) \quad \textbf{(3.6)}$$

$$\vec{J_p} = \mu_p(p\nabla E_v + 1.5pkT\ \nabla ln m_p) - D_p(\nabla p - p\ \nabla ln\gamma_p) \quad \textbf{(3.7)}$$

where μ_n and μ_p are electron and hole mobilities, m_n and m_p are spatial variation of the effective masses, and γ_n and γ_p are obtained from Fermi statistics. The diffusivities D_n and D_p are obtained in terms of mobility using the Einstein relation, D = $kT\mu$.

Further, self heating phenomenon is considered to account for heating in narrow nanowire channel, as it is surrounded by isolation oxide or due to absence of heat conduction path. Sentaurus device computes the spatially dependent lattice temperature where all the temperatures merge into its calculation.

Bandgap narrowing is considered by activating the OldSlotboom [128]–[131] which is:

$$\Delta E_g^0 = E_{ref}\left[\ln\left(\frac{N_{tot}}{N_{reg}}\right) + \sqrt{\left(\ln\frac{N_{tot}}{N_{ref}}\right)^2 + 0.5}\right] \quad \textbf{(3.8)}$$

where, E_{ref} and N_{ref} are material parameters.

For calculation of carrier mobility various models are activated like Phumob [132] which considers majority and minority carrier bulk mobilities, the model takes into account screening of ionized impurities by charge carrier, electron-hole scattering, and clustering of impurities. In presence of high electric fields, the velocity saturates to a finite speed v_{sat} as the carrier drift velocity is no longer proportional to the electric field. To consider the electric field perpendicular to semiconductor-insulator interface Enormal model is enabled.

Recombination models such as doping dependent Shockley–Read–Hall and band2band tunneling are also enabled. At the material interface of semiconductor/gate-dielectric Fowler-Nordheim tunneling and direct tunneling models [133] are enabled.

When the device structure matching to reported VNWFET [5] is created using structure editor and simulated with the models presented earlier, it is observed that after tuning the gate workfunction to match the threshold voltage, a good match of I_D-V_{GS} characteristics is obtained as shown in Figure 3.6 [57].

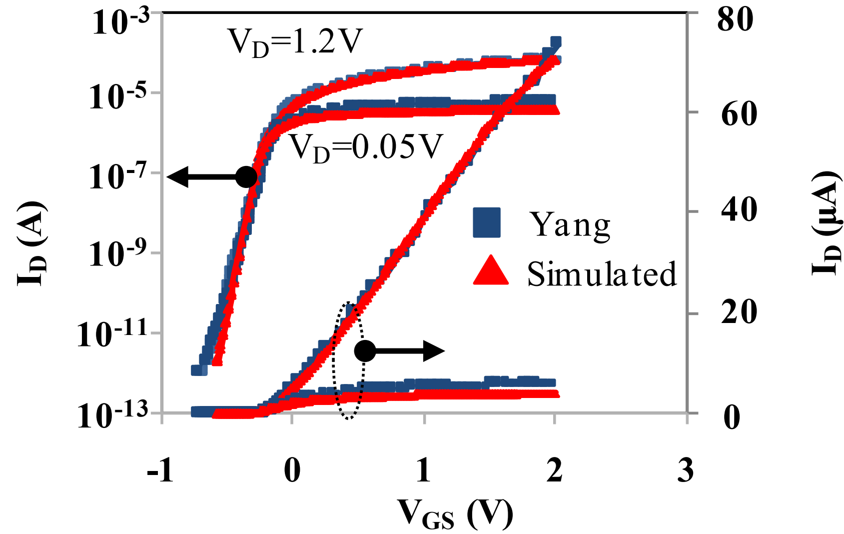

Figure 3.6 I_D-V_{GS} characteristics of VNWFET device with reported dimensions is found to match well with experimentally reported data [57]**.**

As the focus of this thesis is on performance analysis of sub 45 nm VNWFET with nanowire diameter around 10 nm, the devices are expected to suffer from quantization effects and high contact resistance. To account for the contact resistance at the interface of metal-silicon a distributed resistance of 1×10^{-8} $\Omega.cm^2$ is considered [134]. The setup is further calibrated against reported short channel rectangular nanowire devices [135] NMOS (L_G=35nm, NW width = 13.3 nm and height = 20.4 nm, T_{OX}=1.8 nm) and PMOS (L_G=25nm, NW width = 9 nm and height = 13.9 nm), where these devices are also expected to exhibit ballistic transport of carriers. A template of the advanced physics section used in device simulations is provided in Appendix B.

The quantization effect is included as the device dimensions have reached quantum mechanical lengths and the wave nature of electron and holes cannot be neglected. In MOSFETs quantization leads to shift in threshold voltage and reduction of gate capacity. We have considered the van Dort quantization model [136] which is a fast, robust and proven model [66]. The terminal current characteristics are well described by this model, though it does not give correct density distribution in channel. We have considered the quantization parameters which are reported to match with silicon data for electron [136] and hole [137].

Further, Monte Carlo analysis of these devices is carried out following the procedure given in Sentaurus applications [66], [138] to find the carrier velocity under quasi-ballistic mode of transport. The surface scattering ratio is taken as 0.85 for the whole device and surface scattering ratio ballistic is taken as 0.85 for a ballistic window covering the channel and gate-

dielectric regions. The carrier velocity thus obtained are used in velocity saturation model of the device simulation setup [138]. It is observed that NMOS devices with L_G = 35 nm show ballistic velocity of 1.4×10^7 cm/sec and PMOS devices with L_G=25nm show ballistic velocity of 1.2×10^7 cm/sec.

The rectangular nanowire devices matching to reported device dimensions [135] are simulated with quantization, contact resistance, joule heating, modified effective saturation velocity along with earlier calibrated setup. It is found that the simulated characteristics of NMOS and PMOS match well with reported device characteristics as shown in Figure 3.7.

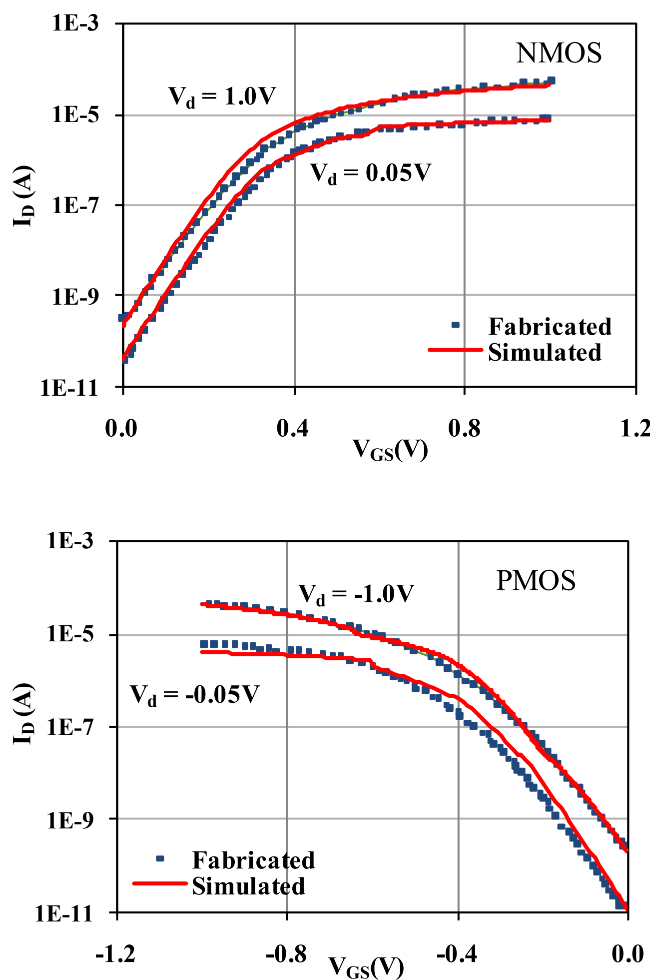

Figure 3.7 I_D-V_{GS} characteristics of rectangular nanowire device with reported dimensions is found to match well with experimentally reported data [135].

These results prove that the simulation setup being considered for the analysis of VNWFET at sub 45 nm technology nodes is well calibrated to reproduce experimental results.

3.3 Device and Simulation Details

In this thesis, VNWFET (shown in Figure 3.5) based device designs and circuit designs have following device dimensions: bottom active area of 3F×F, contact via of F×F, contact to contact spacing of F, variable channel length 45 nm – 15 nm, variable extension length 30 nm to 10 nm, nanowire diameter (D_{NW}) is 10 nm/15 nm (NMOS/PMOS) and the gate workfunction of 4.4 eV/4.85 eV (NMOS/PMOS). The gate dielectric is considered to be SiO_2 and of thickness 2 nm. F is the minimum feature size and is equal to L_G. The contact resistivity of 1×10^{-8} Ωcm^2 is used in all devices for metal-silicon interface. The doping concentrations in different regions are p-substrate with constant doping of 1×10^{16} cm^{-3}, heavily doped active region of fixed doping 1×10^{20} cm^{-3}, constantly doped extension 1×10^{19} cm^{-3}, and channel is 1×10^{16} cm^{-3} doped [57], [127], [139]. We have tabulated important device structural parameters used in the thesis work in Table 3.1.

Table 3.1 Device structural parameters used in the thesis.

p-substrate doping = 1×10^{16} cm^{-3}	L_G = 45 to 15nm
active region doping =1×10^{20} cm^{-3}	Active area = 3F×F
S/D extension doping = 1×10^{19} cm^{-3}	S/D_{ext} = 30 to 10 nm
Channel doping = 1×10^{16} cm^{-3}	Contact via = F×F
Contact resistivity = 1×10^{-8} $\Omega\cdot cm^2$	Contact-contact spacing = F
gate workfunction = 4.4/4.85 eV (NMOS/PMOS)	D_{NW} = 10/15 nm (NMOS/PMOS)
Carrier saturation velocity = $1.8/1.5 \times 10^7$ cm/sec (Electron/Hole)	

In this thesis work, for in depth analysis of VNWFET devices and circuits various simulations are performed such as: DC sweep simulations, AC simulations and transient simulations. The DC simulations are performed on device to find I_D-V_{GS} characteristics for V_{DS} bias of 0.05 V, V_{DD} V and V_{GS} sweep from 0 V to V_{DD} V. It is to be noted that V_{DD} depends on channel length, and is equal to 1 V for 45 nm, 32 nm and 0.8 V for 22 nm, 15 nm devices. From I_D-V_{GS} characteristics device parameters such as I_{ON} (I_{DS} when V_{GS}=V_{DS}=V_{DD}), I_{OFF} (V_{GS}=0 V and V_{DS}=V_{DD}), SS and DIBL. The device I_D-V_{DS} characteristics are done for V_{GS} bias of $V_{DD}/4$, $V_{DD}/2$, $3V_{DD}/4$ and V_{DD} and V_{DS} sweep from 0 V to V_{DD} V. These characteristics will be modeled using the nth power law [67]. Further, DC simulations are performed with CMOS inverter and common-source amplifier to obtain voltage transfer characteristics (VTC), where input voltage of inverter is swept from 0 V to V_{DD} V. From the VTC one can extract gain and noise margin parameters.

The AC simulations are performed at a fixed frequency of 100 kHz on device to find inter-electrode capacitances with respect to gate and drain voltages. For C-V_{GS} characteristics V_{DS} is biased at of 0 V, V_{DD} V and V_{GS} is swept from 0 V to V_{DD} V and for C-V_{DS} characteristics V_{GS} is biased at of 0 V, V_{DD} V and V_{DS} is swept from 0 V to V_{DD} V. The value of the inter-electrode capacitances at V_{GS}=V_{DS}=0 V correspond to parasitic capacitance. Further, AC simulations are performed on device and CS amplifier where V_{GS}, V_{DS} are biased to particular voltage values and frequency is swept from 1 Hz to 100 THz. From these simulation results we can obtain transconductance, output conductance and thus extract gain, 3db bandwidth and unity gain bandwidth (f_T).

Finally, the transient simulations are performed on CMOS inverter to find its delay response for various inverter layouts. In transient analysis a voltage pulse is applied at input node with a rise and fall time of 5 ps and load capacitance equivalent to inverter input capacitance or similar inverter is used as load. Further, from the inverter transient simulation we can extract input capacitance and output capacitance by integrating appropriate nodal currents (to obtain total charge) and divide it by voltage transition difference.

The templates for various device and circuit simulations used in this thesis are provided in Appendix C.

4 CHAPTER

DEVICE SCALING PERFORMANCE

This chapter deals with the VNW device performance in terms of I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, SS, DIBL for both NMOS and PMOS for sub 45 nm channel length devices. Figure 4.1 shows structure of the vertical nanowire FET implemented in 3D device simulator [66], as presented in chapter 3 earlier. The following notation will be used for referring to device structure arising out of S/D asymmetry: the device is referred as source bottom (S_B) if bottom electrode (B) acts as source and top electrode (T) acts as drain, and the device is referred as source top (S_T) if top electrode (T) acts as source and bottom electrode (B) acts as drain. The scaling performance of VNW device is presented in this chapter with respect to S/D_{ext}, D_{NW}, L_{ov}, and T_{ox} which are marked on device structure in Figure 4.1. The nanowire devices are considered as replacement for existing planar devices for sub 22 nm technology nodes, thus this study is performed for 15 nm channel length devices. For 15 nm channel length devices, performance is first analysed with respect to scaling of S/D_{ext} as these devices are expected to suffer from large series resistance due to narrow nanowire extensions. Further, for 15 nm channel length devices with minimum possible extension length, we study the impact of wire diameter, gate overlap/underlap length and gate oxide thickness variations and the impact of source/drain asymmetry on device performance. The device I-V characteristics are modeled with n^{th} power law, which will be employed later in circuit delay prediction.

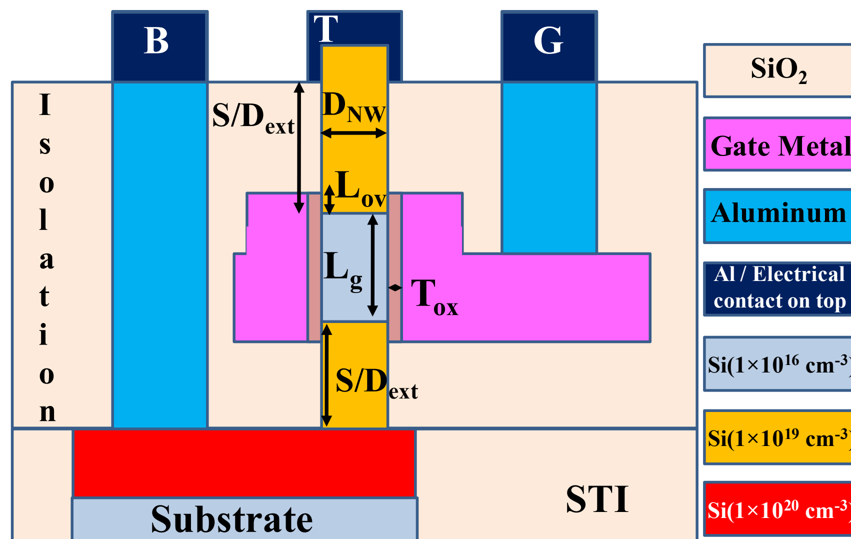

Figure 4.1 Vertical Nanowire FET structure highlighting important physical dimensions.

4.1 Scaling of Channel Length: L_G

VNW device performance with respect to scaling of L_G is shown in Figure 4.2. These devices have same S/D_{ext}=30 nm, diameter of NMOS VNW is 10 nm and PMOS VNW is 15 nm and T_{ox} of 2 nm. For 45 nm, 32 nm devices the V_{DD} is set to 1V and for 22 nm, 15nm devices V_{DD} is set to 0.8V. With decrease in L_G from 45 nm to 32nm and 22 nm to 15 nm there is marginal increase in I_{ON} this is attributed to presence of high series resistance (S/D_{ext} = 30 nm). The drop in I_{ON} when L_G is scaled from 32 nm to 22 nm is due to lower V_{DD} in 22 nm devices. It is observed that these devices show minimal presence of SCE even for 15 nm channel length, without even scaling the gate dielectric thickness. Further, we observe that $I_{ON}/I_{OFF} > 1\times10^4$, SS < 80 mV/dec and DIBL < 50 mV/V. Thus, the VNW MOSFET can replace the existing planar MOSFET at sub 22 nm technology nodes which suffer from severe SCE. Hence, the following work is done for 15 nm channel length to prove that VNW MOSFET is the ideal device to replace planar MOSFET at sub 22 nm technology nodes.

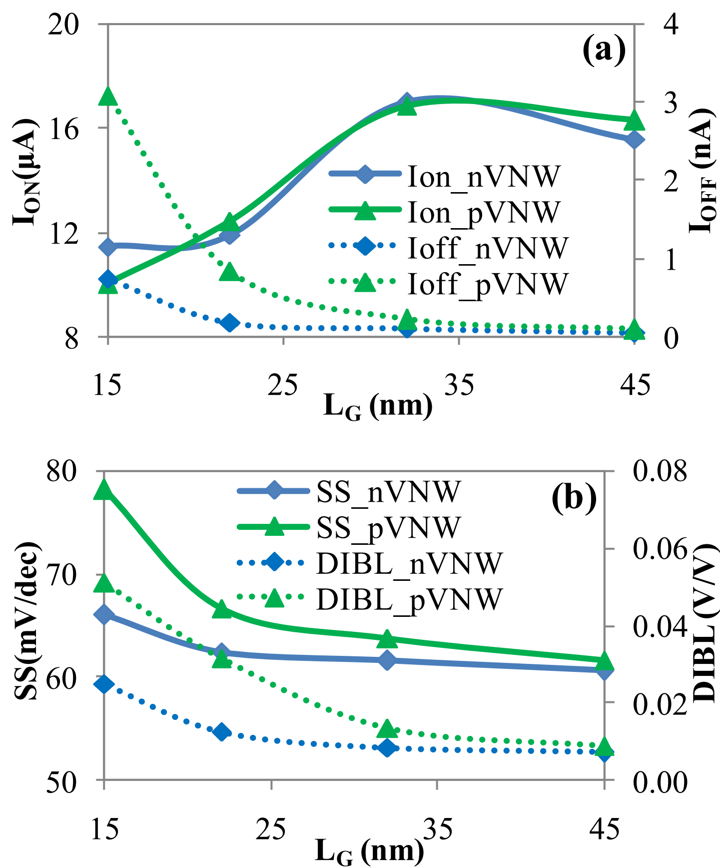

Figure 4.2 (a) I_{ON} ($V_{GS} = V_{DS} = V_{DD}$) and I_{OFF} (V_{GS} = 0V, $V_{DS} = V_{DD}$) of NMOS and PMOS VNW FET versus L_G. (b) SS and DIBL of NMOS and PMOS VNWFET versus L_G showing marginal presence of SCE when L_G is scaled down to 15 nm.

4.2 Scaling of Extension Length: S/D_{ext}

VNW device performance for 15 nm gate length with respect to scaling of S/D_{ext} is shown in Figure 4.3 for S_B and S_T device configuration. It is observed that gate-all-around architecture allows device scaling to L_G=D_{NW} with an appreciable value of I_{ON}/I_{OFF} ratio > 10^4 even when the device have relatively thicker gate oxide (T_{ox}) of 2 nm. This is in contrast to what is required in planar and FinFET devices, where the requirement is to have gate oxide thickness less than 1 nm to control SCE. Thus, it highlights NW CMOS will have inherently low standby power as compared to other device technologies. It is also noted from Figure 4.3 (a) and (b) that the drive currents of NMOS and PMOS are nearly equal, which is due to thicker diameter of nanowire (D_{NW}=14 nm).

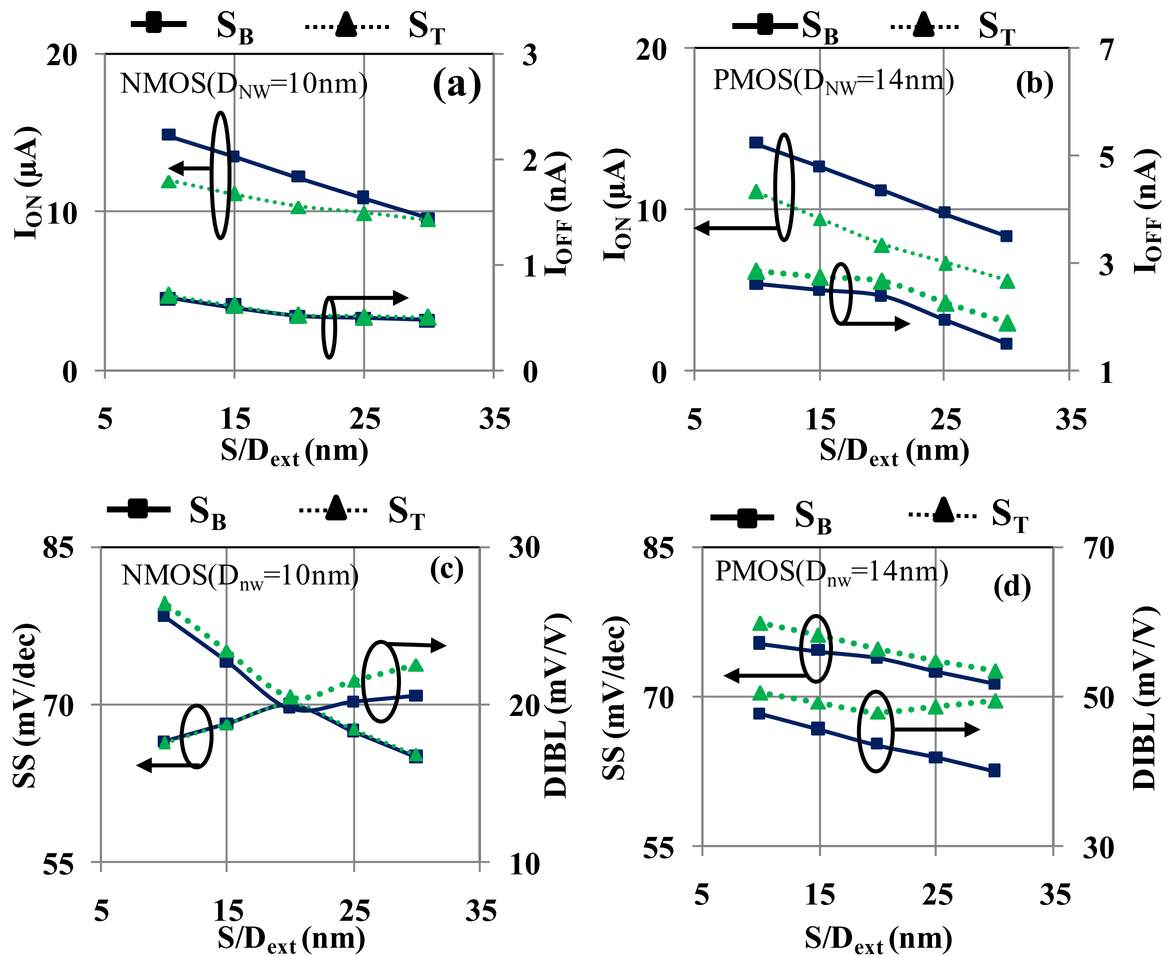

Figure 4.3 I_{ON} (V_{GS} = V_{DS} = 0.8 V) and I_{OFF} (V_{GS} = 0V, V_{DS} = 0.8 V) of (a) n (D_{NW} = 10 nm), (b) p (D_{NW} = 14 nm) VNW FET drive showing excellent scaling performance with S/D_{ext} down to 10nm. SS and DIBL of (c) NMOS and (d) PMOS VNWFET showing marginal presence of SCE when S/D_{ext} =10 nm.

Owing to top/bottom electrode asymmetry, it is expected that the bottom electrode with wider active area will have smaller series resistance (R_B) compared to the top electrode (R_T). Further

due to small dimensions, series resistance is a strong function of S/D_{ext} length. From Figure 4.3 (a)-(b), we note that S_B device has greater I_{ON} ($V_G = V_D = 0.8$ V) compared to S_T device. This can be explained by $R_T > R_B$, since S_T configuration will have lower gate overdrive ($V_{GS} - R_T \times I_D - V_T$) compared to S_B. Thus, the circuit performance depends on whether an S_B/S_T device configuration is used. Further a significant increase in I_{ON} (50 - 60 %) with S/D_{ext} scaling (from 30 to 10 nm) shows the large impact of extension resistance on device performance. It is also observed that I_{OFF} increases marginally when S/D_{ext} is scaled, which indicates controllable SCE even when S/D_{ext} is scaled down to 10 nm. From Figure 4.3 (c) and (d) we infer the same conclusion: that is controllable SCE when S/D_{ext} is 10 nm. It is observed that SS increases from 70 mV/dec by 0.5 mV/dec/nm decrease in S/D_{ext}, and similarly DIBL increases from its value at S/D_{ext} = 30 nm by 0.05mV/V/nm decrease in S/D_{ext}.

From, this analysis we can conclude that, for L_G =15 nm devices the S/D_{ext} can be scaled down to as low as 10 nm (< L_G) without significant degradation in SCE.

4.3 Scaling of Gate Overlap/Underlap Length: L_{OV}

For NMOS devices with L_G = 15 nm, S/D_{ext} =10 nm, T_{OX}=2 nm, and D_{NW} = 10 nm the impact of gate overlap/underlap is carried out. The overlap length is the amount by which gate overlaps the extension region and the underlap length is the distance by which the moderately doped extensions are formed away from gate edge. It is observed from Figure 4.4 that as the overlap length keeps on decreasing or as the underlap length keeps on increasing the I_{ON} current decreases. This is due to increase in series resistance, i.e., lesser overlap of gate with extension or increase in highly resistive lightly doped underlap region.

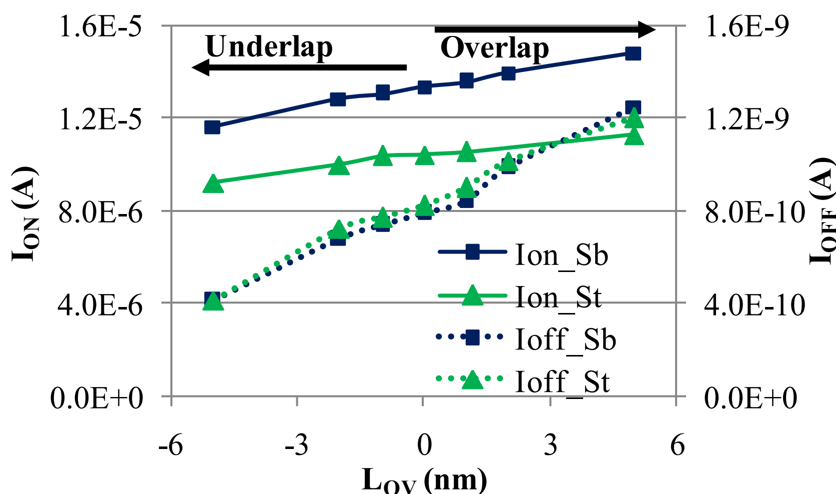

Figure 4.4 I_{ON}, I_{OFF} variation with respect to gate overlap/underlap length.

It is to be observed that with increases in underlap length the I_{OFF} current decrease drastically, this is due to high resistance of underlap regions. For the range of overlap/underlap lengths considered, it is found that SS ~ 65-70 mV/dec and DIBL ~ 20-30 mV/V, which are acceptable values highlighting minimal presence of short channel effects. For the devices used in this thesis work, L_{OV} = 2 - 5 nm are used, as these devices have higher I_{ON} when compared to underlap devices with manageable I_{OFF}.

4.4 Scaling of Gate Dielectric: T_{OX}

For NMOS devices with L_G = 15 nm, S/D_{ext} =10 nm, L_{OV}=2 nm, and D_{NW} =10 nm the thickness of gate dielectric or gate oxide is varied from 1 nm to 2.5 nm. From Figure 4.5 we observe that, with T_{OX} scaling I_{ON} increases linearly and I_{OFF} decreases drastically for both S_B/S_T devices. For T_{OX} scaling from 2.5 nm to 1 nm the device shows SS variation from 70 to 65 mV/dec and DIBL variation from 30 to 10 mV/V. These results highlight the gate insulator scaling can be used for improvement in SCE and device performance.

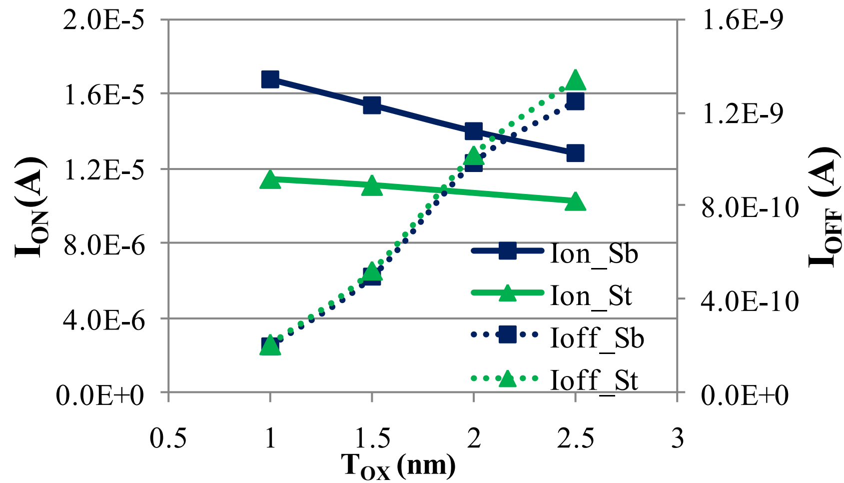

Figure 4.5 I_{ON}, I_{OFF} variation with respect to gate dielectric thickness.

We choose devices in this work with T_{OX}=2 nm, because it minimizes the tunneling and gate leakage currents. Further, these devices have an acceptable value of I_{OFF} current 1 nA and fractionally lower I_{ON} than that obtained at T_{OX} = 1 nm. Moreover, the difference between I_{ON} for S_B/S_T devices is optimal when T_{OX} = 2 nm, thus reducing the device asymmetry.

4.5 Scaling of Nanowire Diameter: D_{NW}

Finally the impact of nanowire diameter variation on device performance is carried for NMOS devices with L_G = 15 nm, S/D_{ext} =10 nm, L_{OV}=2 nm, and T_{OX}=2 nm. It can be observed from Figure 4.6 that as the diameter is increased from 8 to 12 nm there is a linear increase in I_{ON}. This is due to increase in width of device and decrease in series resistance as extension regions cross sectional area also increased. It is further observed that I_{ON} increases at rate of 1.45 μA per 1 nm increase in nanowire diameter. Thus, it can be used as width tuning technique to tune current drive in PMOS devices to match with that of NMOS. Further, I_{OFF} current increases significantly from 0.2 nA to 4 nA. It is observed from device characteristics that the SS degrades from 65 to 75 mV/dec and DIBL increases from 15 to 50 mV/V, when diameter is increased. All these increases in device parameters highlight the presence of SCE in larger diameter device. Further, it can be noted that both S_B/S_T scale proportionately with diameter, which is due to similar change in series resistance.

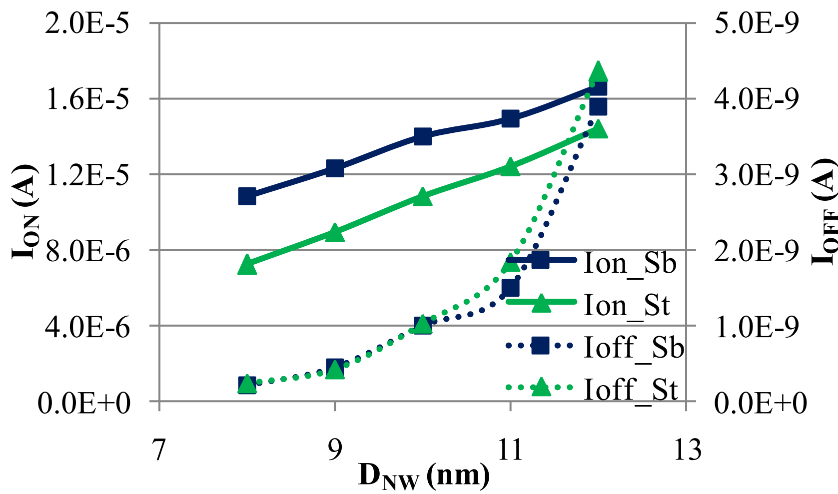

Figure 4.6 I_{ON}, I_{OFF} variation with respect to nanowire diameter variation.

In this work until and unless specified the diameter of nanowire in NMOS devices is 10 nm and PMOS devices is 14/15 nm. For these values of diameters the devices have matched I_{ON} and acceptable I_{OFF} of 1 nA as shown in L_G and S/D_{ext} scaling sections.

4.6 n^{th} Power Law Modeling

Sakurai and Newton [67] have proposed a simple MOSFET model for device and circuit analysis, which is known as the nth power law. The model consists of the following parameters V_{t0}, B, n, K, m and γ, which are extracted from the device I-V characteristics. The inverter

delay can be modeled by using some of these parameters of n and p devices along with C_{load} (the total output node capacitance). The model equations given by Sakurai and Newton [67] are as follows:

$$V_{TH} = V_{T0} + \gamma\left(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F}\right) \quad \textbf{(4.1)}$$

where V_{T0}, γ, φ_F describe threshold voltage and for $V_{BS} = 0$, $V_{TH} = V_{T0}$ which is the case of NW devices .

$$V_{DSAT} = K(V_{GS} - V_{TH})^m \quad \textbf{(4.2)}$$

$$I_{DSAT} = \frac{W}{L_{eff}} B(V_{GS} - V_{TH})^n \quad \textbf{(4.3)}$$

where K, m control the linear region characteristics and B, n determine the saturated region characteristics. The drain current is then defined as:

$$I_D = I_{D5} = I_{DSAT}\,(1 + \lambda_{CLM} V_{DS}) \qquad (V_{DS} \geq V_{DSAT}\ \text{: Saturated region}) \quad \textbf{(4.4)}$$

$$I_D = I_{D3} = I_{D5}\left(2 - \frac{V_{DS}}{V_{DSAT}}\right)\left(\frac{V_{DS}}{V_{DSAT}}\right) \qquad (V_{DS} < V_{DSAT}\ \text{: Linear region}) \quad \textbf{(4.5)}$$

where $\lambda_{CLM} = \lambda_0 - \lambda_1 V_{BS}$, λ_0, λ_1 are related to finite drain conductance in saturated region.

The model parameters are extracted from the device I-V characteristics using the following equations and the data points which are used for extraction are marked on device characteristics as shown in Figure 4.7.

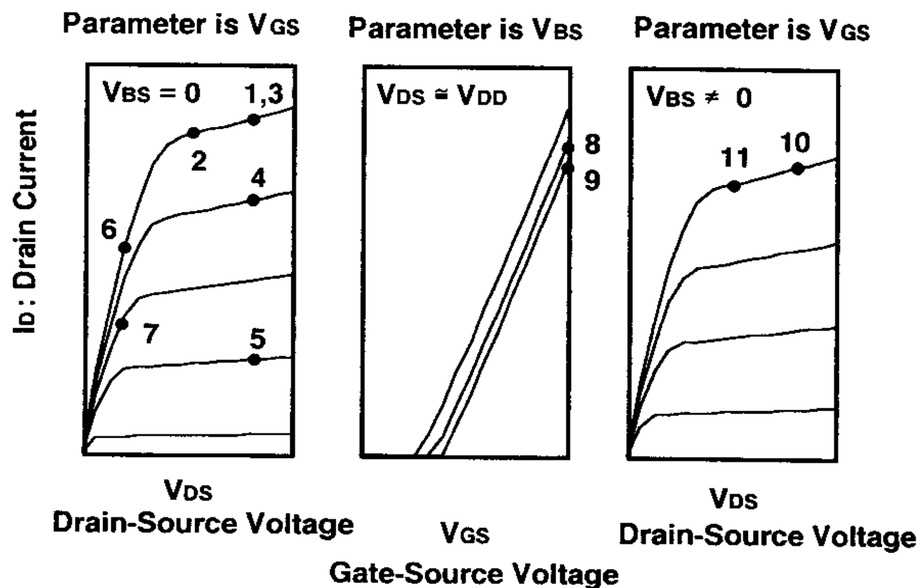

Figure 4.7 Selected points for model parameter extraction of nth power law [67].

$$\lambda_0 = (I_{D,2} - I_{D,1})/(I_{D,1}V_{DS,2} - I_{D,2}V_{DS,1}) \quad \textbf{(4.6)}$$

$$I_{z3} = I_{D,3}/(1 + \lambda_0 V_{DS,3}) \qquad I_{z4} = I_{D,4}/(1 + \lambda_0 V_{DS,4}) \qquad I_{z5} = I_{D,5}/(1 + \lambda_0 V_{DS,5}) \quad \textbf{(4.7)}$$

V_{T0} is obtained by obtaining the solution of the following equation:

$$f_v(V_{T0}) = \log\left(\frac{I_{z3}}{I_{z4}}\right)\log\left[\frac{(V_{GS,4}-V_{T0})}{(V_{GS,5}-V_{T0})}\right] - \log\left(\frac{I_{z4}}{I_{z5}}\right)\log\left[\frac{(V_{GS,3}-V_{T0})}{(V_{GS,4}-V_{T0})}\right] \quad \textbf{(4.8)}$$

The solution for above function is obtained graphically by plotting $f_v(V_{T0})$ with respect to V_{T0}. The other model parameters are obtained using the expression below:

$$n = \log(I_{z3}/I_{z4})/\log[(V_{GS,3} - V_{T0})/(V_{GS,4} - V_{T0})] \quad \text{and} \quad B = I_{z3}/(V_{GS,3} - V_{T0})^n \quad \textbf{(4.9)}$$

$$E_6 = I_{D,6}/\{B[(V_{GS,6} - V_{T0})^n(1 + \lambda_0 V_{DS,6})]\}$$

$$E_7 = I_{D,7}/\{B[(V_{GS,7} - V_{T0})^n(1 + \lambda_0 V_{DS,7})]\} \quad \textbf{(4.10)}$$

$$V_{DSAT,6} = V_{DS,6}\left(1 + \sqrt{1 - E_6}\right)/E_6 \qquad V_{DSAT,7} = V_{DS,7}\left(1 + \sqrt{1 - E_7}\right)/E_7 \quad \textbf{(4.11)}$$

$$m = \log(V_{DSAT,6}/V_{DSAT,7})/\log[(V_{GS,6} - V_{T0})/(V_{GS,7} - V_{T0})]$$

$$K = I_{z3}/(V_{GS,6} - V_{T0})^m \quad \textbf{(4.12)}$$

The above procedure is followed to model the characteristics of VNWFET NMOS and PMOS as shown in Figure 4.8. It is observed that the model characteristics match well with the TCAD simulation results. For different dimensions the nth power law model parameters are extracted and tabulated in Table 4.1. The model parameters thus obtained can be used in estimation of performance of circuits such as inverter, NAND and NOR gates.

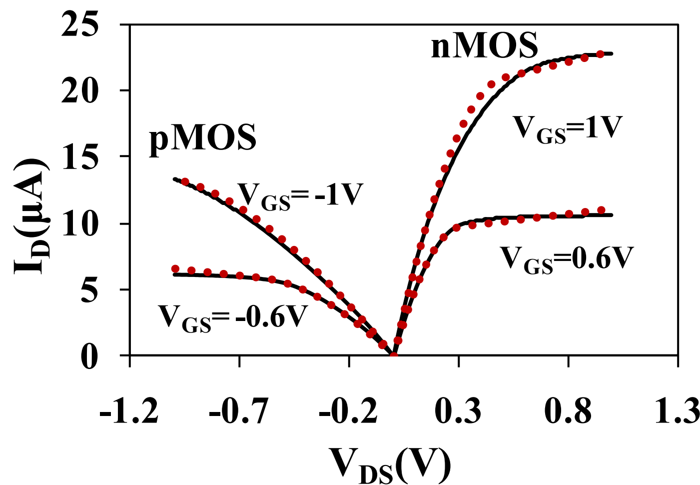

Figure 4.8 I-V characteristics of NMOS and PMOS VNWFET (L_G=45nm, S/D_{ext}=30nm, Diameter=15nm) obtained from simulation (solid lines) and obtained from n^{th} power law model (dotted lines) [57].

Table 4.1 Extracted nth power model parameters for various VNWFET devices.

	n-VNWFET (Dia=15nm)						p-VNWFET (Dia=15nm)					
L(nm)	V_{T0}	K	m	B	n	λ_0	V_{T0}	K	m	B	n	λ_0
250	0.288	0.728	0.728	2.2E-5	1.21	0.14	-0.271	1.366	0.905	1.03E-5	1.38	0.066
45	0.305	0.623	0.576	2.6E-5	0.86	0.21	-0.336	1.254	0.548	1.33E-5	0.76	0.362
32	0.305	0.608	0.270	2.6E-5	0.80	0.18	-0.342	1.184	0.471	1.32E-5	0.68	0.401
22	0.300	0.568	0.478	2.5E-5	0.75	0.22	-0.339	0.966	0.391	1.36E-5	0.62	0.398

4.7 Summary

From the scaling study we observe that S/D_{ext} can be scaled down to 10 nm (< L_G =15nm) with marginal SCE. The other optimum device dimensions which are obtained from the scaling study are L_{OV}=2 nm, T_{OX}=2 nm and D_{NW}(NMOS/PMOS) = 10/15 nm. For the mentioned device dimensions the devices shows good performance such as I_{ON}/I_{OFF} > 10^4, SS ~ 60 – 70 mV/dec and DIBL < 50 mV, which highlight the better control of short channel effects due to surrounding gate architecture. Further, this study highlights the advantage of achieving matched drive currents for NMOS and PMOS, which differ by a non integral factor (~ 1.4 – 1.5) with the help of single nanowire devices, as opposed to multi nanowire/Fins required in lateral devices. Finally, it is shown that nth power law can be used to obtain device I-V characteristics, and the model parameters will be used in circuit performance prediction.

5 CHAPTER

PARASITIC MODELING

As we scale down the device dimensions the parasitic start to dominate. These parasitic play an important role in determining the device performance as presented in chapter 4. This chapter focuses on modeling of parasitic resistance and capacitance present in VNW devices considering cylindrical gate and structural asymmetry. Their impact on circuit performance will be presented in chapter 6. In these models, the inherent device asymmetry and device structural topology such as the cylindrical gate, rectangular vias, gate extension and contact pad overlapping the tip of nanowire are considered. Further, the impact of device scaling on these parasitic is thoroughly investigated and emphasis is given on the major parasitic contributors. These parasitic models will help in estimation of circuit performance (to be presented in next chapter) without actually performing time consuming TCAD simulations.

For device shown in Figure 5.1 a tradeoff between series resistance and capacitance exists, needing optimized S/D_{ext} and also highlights the structural asymmetry in the device, which results in asymmetric parasitics.

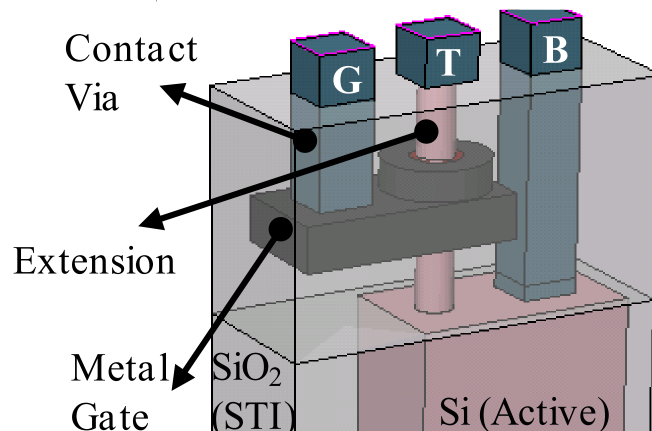

Figure 5.1 VNW FET 3-D isometric view.

5.1 Capacitance Modeling

Figure 5.2 shows various inter-electrode components of device capacitance. It is apparent that the overlap of gate with bottom electrode is large due to the gate extension, while the overlap of cylindrical gate with top electrode is small. Hence, the gate to top electrode (C_{GT}) and gate to

bottom (C_{GB}) electrode capacitances are different. It is important to model these parasitic for accurate evaluation of circuit performance having S_B or S_T configurations. As shown in Figure 5.2, C_{GB}/C_{GT} comprises of parallel plate (*pp*), gate-extension fringe (*gex*), gate-overlap (*ov*), gate-inner fringe (*if*), gate-outer fringe (*of*, Figure 5.3 (a)) components and gate-channel capacitance (*GC*).

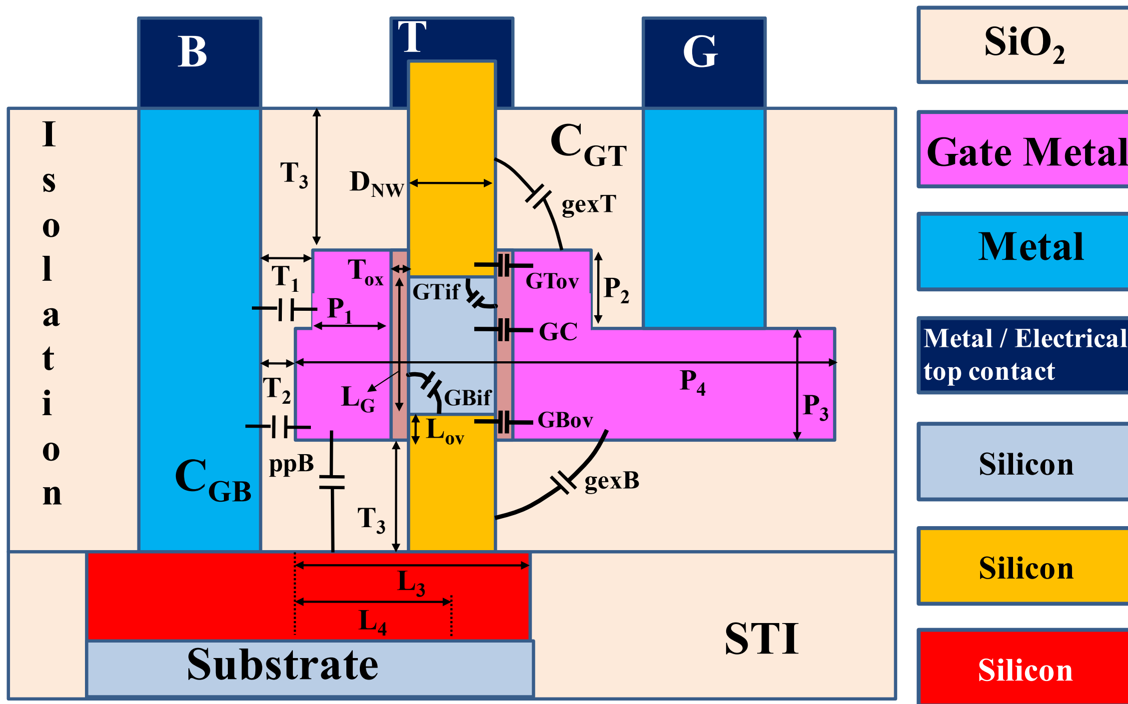

Figure 5.2 VNWFET 2-D view marked with parasitic capacitance components.

Some of the important parameters that will be used in the capacitance models are listed in Table 5.1.

Table 5.1 Parameters used in standard capacitance components.

L_G = Channel Length	***T_{ox}*** = Gate oxide thickness	***D_{NW}***=Nanowire diameter
L_{ov}=Gate-S/D overlap	***ViaThk*** = Metal via thickness	***GaExtWid***= Gate Extension width
T_1, T_2, T_3, L_3, L_4, P_1, P_2, P_3 and P_4 are identified in Figure 5.2		

The standard components in Figure 5.2 like *GC*, *ov*, *if* and *of* are modeled by appropriately modifying existing models available in literature to account for VNW device geometry.

The *GC* capacitance is modelled by standard cylindrical capacitance incorporating inversion layer quantisation effect in the model. Thus, the model given below has effective gate insulator thickness T_{OX_qn} in place of T_{OX}.

$$C_{GC} = 2\pi\varepsilon_{ox} L_G / ln\big(1 + 2\, T_{ox_qn} / D_{nw}\big) \quad \textbf{(5.1)}$$

The *ov* capacitance component is also modeled using the standard cylindrical capacitance formula and is given as (5.2), where L_{OV} denotes overlap length.

$$C_{GBov} = C_{GTov} = 2\pi\varepsilon_{ox} L_{OV} / \ln\big(1 + 2\, T_{ox_qn} / D_{nw}\big) \quad \textbf{(5.2)}$$

The inner fringe capacitance component *if* model can be obtained from an equivalent model proposed for lateral nanowire by Zou et al., [93] and is given as below.

$$C_{GBif} = C_{GTif} = 2\varepsilon_{Si} D_{NW} / \ln(1 + D_{NWn} / 4T_{OX}) \quad \textbf{(5.3)}$$

Parallel plate capacitance component *ppB* between gate bottom surface – active top surface and gate sidewall – bottom electrode via is given by

$$\mathrm{C_{ppB}} = \epsilon_{\mathrm{OX}} \left[\frac{\mathrm{P_2 \times ViaThk}}{\mathrm{T_1}} + \frac{\mathrm{P_3 \times ViaThk}}{\mathrm{T_2}} + \frac{(\mathrm{GaExtWid} \ \times \mathrm{L_3} - \pi(\mathrm{D_{NW}} + \mathrm{T_{OX}})^2)}{\mathrm{T_3}}\right] \quad \textbf{(5.4)}$$

The component *gex* needs to be derived for cylindrical electrodes, and is very important as it modulates the resistance of extension region. The *gexT* is modeled depending on S/D_{ext} dimension as shown in Figure 5.3. Following the approach in [93], [140], to obtain *gexT* component for structure with cylindrical features, we consider *ds1* and *ds2* as two differential area elements on the gate and extension regions. The effective area ds_{eff}, in terms of ds_1 and ds_2 elements is defined as $ds_{eff} = \sqrt{(ds_1 ds_2)} \cong \eta ds_1$; where $\eta = \sqrt{\int ds_2 / \int ds_1}$.

Case 1: When $P_1 \leq T_3 - T_{ox}$ (Figure 5.3(a))

$$\mathrm{S_1} = \pi[(\mathrm{P_1} + 0.5\mathrm{D_{NW}} + \mathrm{T_{OX}})^2 - (0.5\mathrm{D_{NW}} + \mathrm{T_{OX}})^2]$$

$\mathrm{S_2} = \pi\, \mathrm{D_{NW}}\, \mathrm{P_1}$ and $\eta = \epsilon_{OX}\sqrt{D_{NW}/(P_1 + D_{NW} + 2T_{OX})}$

Modifying expression for capacitance between plates at an angle π/2 [140], the capacitance is modeled as,

$$\mathrm{C_{gexT}} = \iint \mathrm{dC} = 4\eta \mathrm{P_1} \quad \text{where} \quad dC = \frac{2\eta}{\pi}\ln(1 + dx/x).(xd\varphi) \quad \textbf{(5.5)}$$

and the integral is performed over surface S_1 with limits as:

$$\varphi : 0 \ to\ 2\pi \quad and \quad x: (0.5D_{NW} + T_{OX})\ to\ (P_1 + 0.5D_{NW} + T_{OX})$$

Case 2: When $P_1 \geq T_3 - T_{ox}$ (Figure 5.3 (b))

$$\eta = \epsilon_{\mathrm{OX}}\sqrt{\mathrm{D_{NW}}/(\mathrm{T_3} + \mathrm{D_{NW}} + 2\mathrm{T_{OX}})} \quad \text{and} \quad \mathrm{C_{gexT}} = 4\eta(\mathrm{T_3} - \mathrm{T_{ox}}) \quad \textbf{(5.6)}$$

Similarly the *gexB* component has two cases. Case 1 ($P_1 < T_3 - T_{ox}$) a square area of gate bottom is considered excluding a part of gate extension. The model [93] for rectangular gate and cylindrical extension is modified for square gate by replacing height and width of gate by L_4 (shown in Figure 5.2), thus resulting in (5.7). For case 2, ($P_1 > T_3 - T_{ox}$) the capacitance component is similar to that of Figure 5.3 (b) with the model given by (5.6).

Case 1: When ($P_1 < T_3 - T_{ox}$)

$$C_{gexB} = \frac{16}{\pi}\epsilon_{OX}\left[(0.5L_4 - 0.5D_{NW} - T_{OX})(3 - 1/\sqrt{2})\right]$$
$$\times\sqrt{[\pi D_{NW}(L_4/\sqrt{2} - 0.5D_{NW} - T_{OX})]/[L_4^2 - \pi(0.5D_{NW} + T_{OX})^2]} \quad \textbf{(5.7)}$$

Case 2: When ($P_1 > T_3 - T_{ox}$)

$$C_{gexB} = 4\epsilon_{ox}(T_3 - T_{OX})\sqrt{D_{NW}/(D_{NW} + T_{OX} + T_3)} \quad \textbf{(5.8)}$$

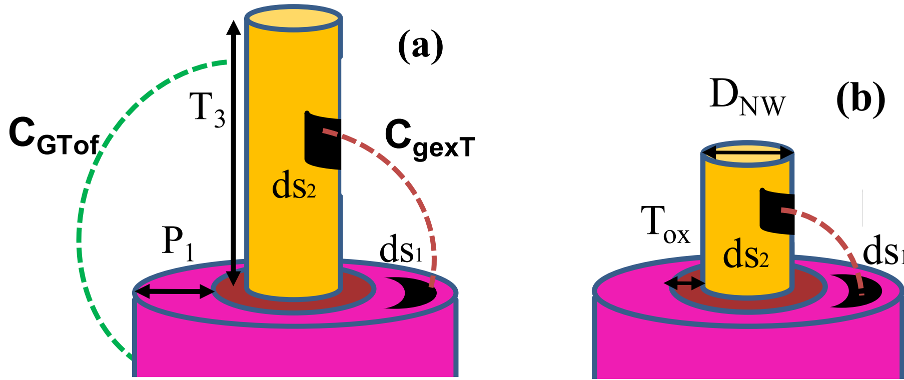

Figure 5.3 *GTof* and *gexT* components are identified for (a) Extension length > gate thickness (b) Extension Length < gate thickness [139]**.**

The model of *GTof* capacitance component is obtained by using modified Suzuki model [141], by taking into account that the metal B/G vias lying on either side of nanowire terminate 50% of the field lines emanating from gate outer surface.

$$C_{GTof} = 0.5D_{NW}\,\varepsilon_{OX}\ln\left[1 + \frac{T_3 - T_{OX} - P_1}{T_{OX} - P_1}\right] \quad \textbf{(5.9)}$$

The model for *GBof* capacitance component is obtained by modifying the model reported in [141], [142], it consists of two components: one between gate extension and active region and the other between gate extension and bottom electrode.

$$C_{GBof} = (\epsilon_{OX}/\pi)(2 \cdot GaExtWid - ViaThk + 2 \cdot L_3) \times \ln\left[(K^2-1)\,(K^2/(K^2-1))^{K^2}\right] + (\epsilon_{OX}/\pi)GaExtWid \times \ln\left[(M^2-1)\,(M^2/(M^2-1))^{M^2}\right] \quad \textbf{(5.10)}$$

where $K = 1 + P_3/T_3$ and $M = (P_4 - L_3)/T_3$.

The individual components given by (5.1) - (5.10) can be further simplified by replacing the physical dimensions such as L_G, *ViaThk*, *GaExtWid*, L_3, L_4, P_4 etc., in terms of minimum feature size F. These capacitance components are then used to obtain the total bottom and top parasitic capacitances as:

$$C_{GB} = C_{GBOV} + C_{GBif} + C_{ppB} + \beta\, C_{gexB} + \beta\, C_{GBof} \quad \textbf{(5.11)}$$

$$C_{GT} = C_{GTOV} + C_{GTif} + \beta\, C_{gexT} + \beta\, C_{GTof} \quad \textbf{(5.12)}$$

where β is a geometric correction factor for non-parallel plates capacitance components and is same for both GT and GB due to similar structures involved in capacitance components. For example considering Figure 5.3 (a)-(b) if $T_3 = P_1+T_{ox}$, then the field lines defining C_{gexT} will be circular ($\beta = 1$) and if $T_3 \neq P_1+T_{ox}$ non-circular field lines exists thus $\beta < 1$ as reported earlier by [142].

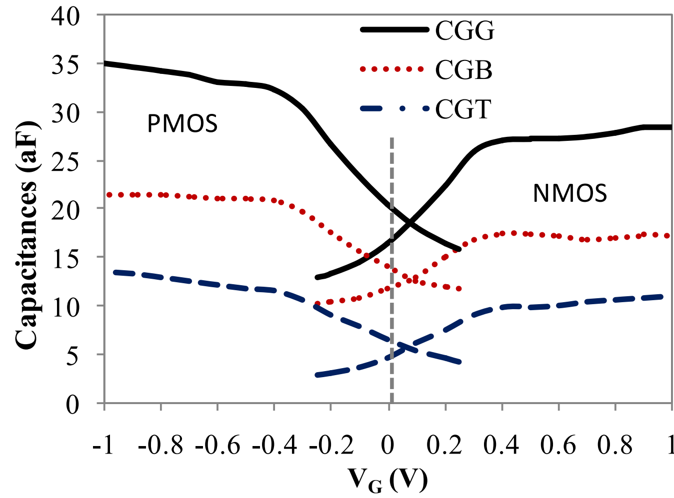

Figure 5.4 Inter electrode capacitances versus V_G for NMOS and PMOS VNWFET (L_G=15 nm, S/D_{ext} = 30 nm and D_{NW}=10/15 nm).

The simulation result of typical variation of inter-electrode capacitance with gate bias (V_D=V_S=0V) is shown in Figure 5.4 and highlights that C_{GB} is larger than C_{GT} [127], which is due to larger overlap of gate bottom with active area. The value of capacitance at V_G=0V is considered as the value of parasitic capacitance.

For NMOS (D_{NW}=10nm), the extracted capacitance (V_G=0V) and model (5.11), (5.12) parasitic capacitances with varying L_G (S/D_{ext} = 30nm) and S/D_{ext} (L_G=15nm) lengths are shown in Figure 5.5 (a)-(b). Figure 5.5 (c)-(d) shows components of the gate capacitance, in which, in addition to other components, top/bottom electrode parasitic capacitances (sum of *pp*, *of*, *gex* components) are labeled C_{paraT}/C_{paraB} respectively. It is observed that with β=0.8 (value is consistent with existing literature [142], the models are found to match well with the simulation results as shown in Figure 5.5. It is seen that parasitic capacitance C_{GB} is about 0.8 to 1.5 times the intrinsic gate capacitance (C_{GC}), while C_{GT} is about 0.2-0.5 times the C_{GC}.

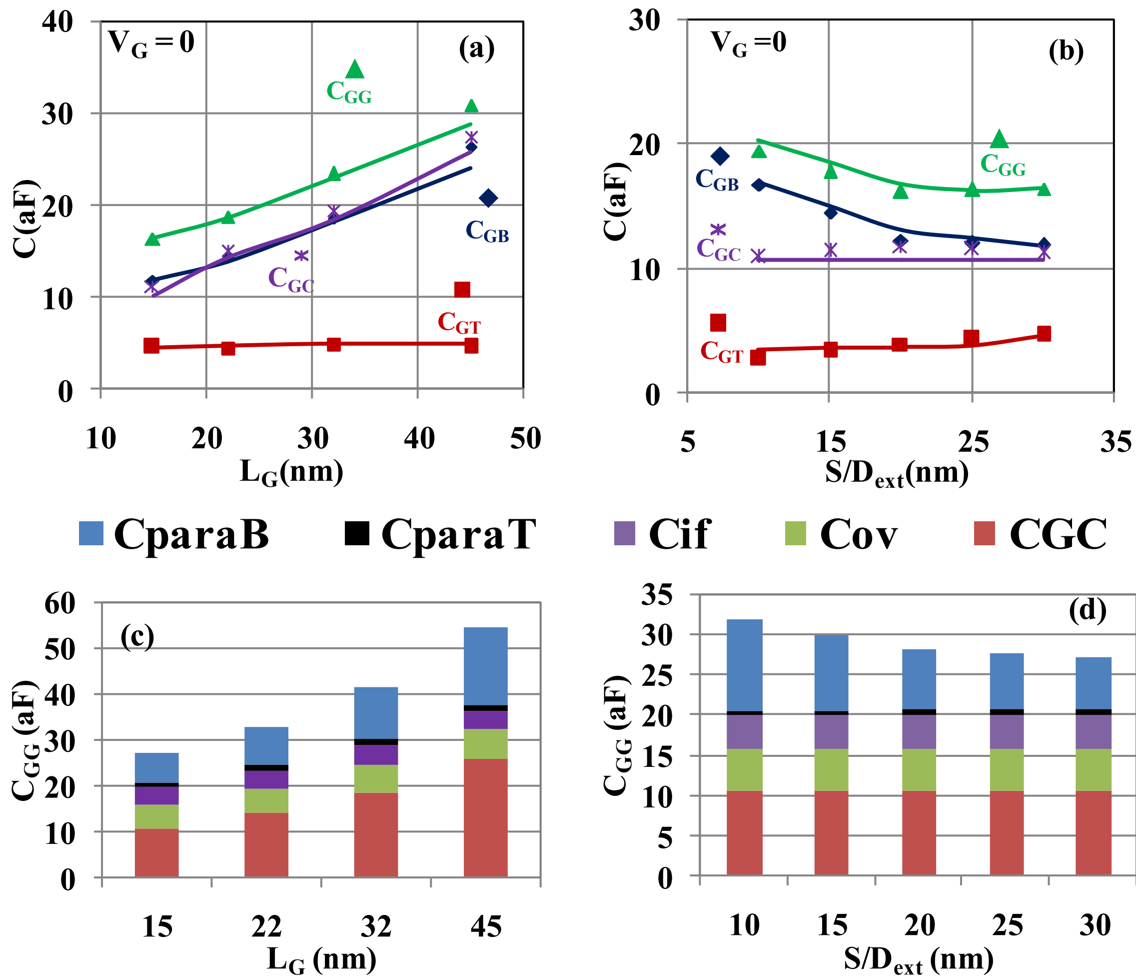

Figure 5.5 NMOS (D_{NW}=10nm) simulated (symbol) and modeled (line) parasitic off state capacitances versus (a) L_G (S/D_{ext}=30nm) and (b) S/D_{ex} (L_G=15nm) and individual components contributing to C_{GG} versus (c) L_G and (d) S/D_{ext}.

Thus total parasitic capacitance is about 1.5 to 2 times C_{GC}, highlighting its importance and role in determining circuit performance. Further, similar behavior and model matching with varying L_G and S/D_{ext} for PMOS (with D_{NW}=15nm is shown in Figure 5.6) is obtained verifying the

inclusion of D_{NW} dependence in model. It is observed that the use of larger D_{NW} in PMOS results in higher capacitance than NMOS.

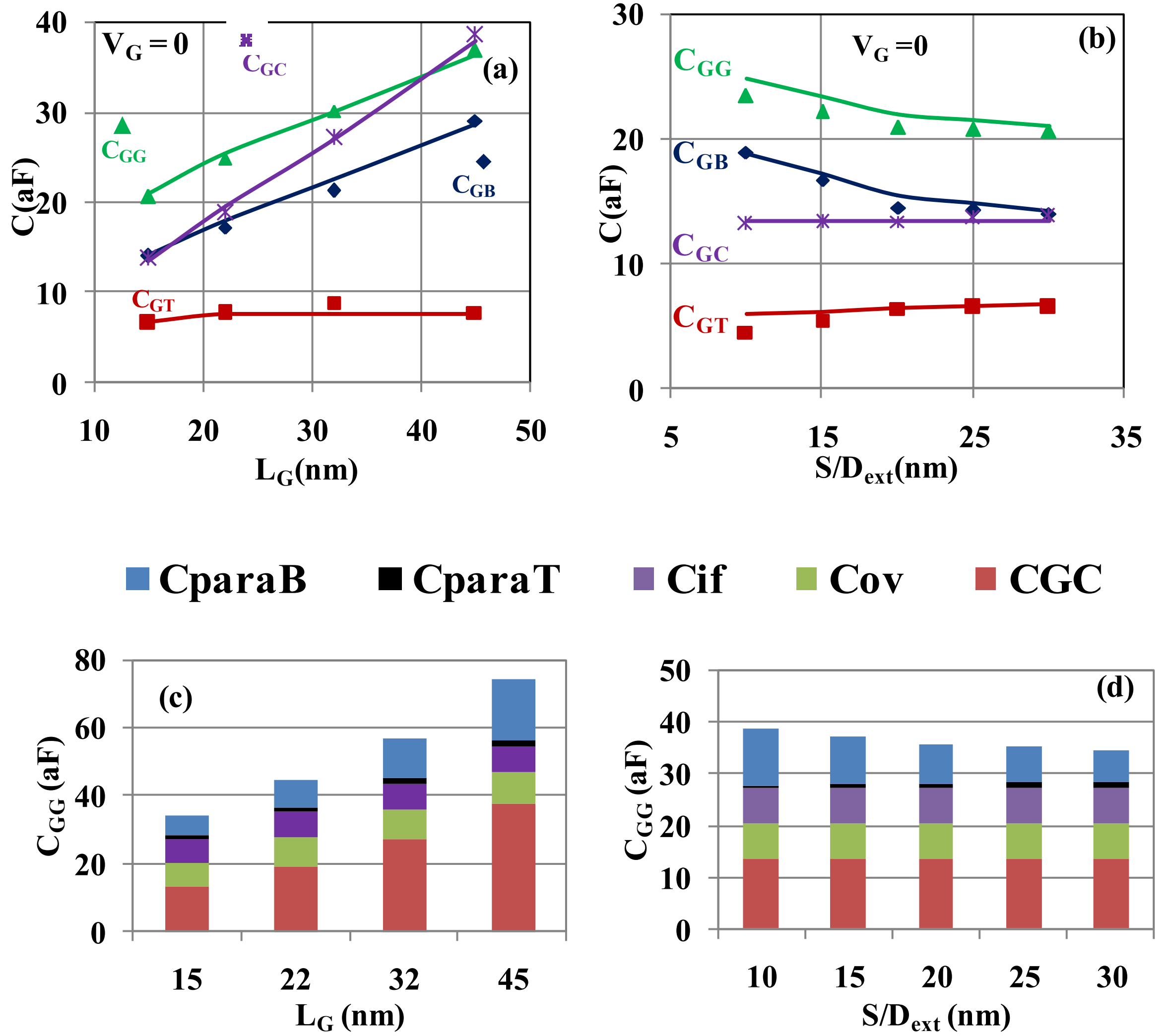

Figure 5.6 PMOS (D_{NW}=14/15nm) simulated (symbol) and modeled (line) parasitic off state capacitances versus (a) L_G (S/D_{ext}=30nm) and (b) S/D_{ex} (L_G=15nm) and individual components contributing to C_{GG} versus (c) L_G and (d) S/D_{ext}.

Figure 5.5 and Figure 5.6 (a), (c) show that with L_G scaling, C_{GC} decreases significantly, while C_{GT}/C_{paraT} capacitance is nearly constant. This is due to fact that, the device structure above gate does not change for varying L_G. However, with L_G scaling, C_{GB}/C_{paraB} capacitance decreases significantly. This can be explained as other device dimensions such as gate extension width/length (*GaExtWid*, P_4 identified in Figure 5.2), via size and active area dimension are also scaled, resulting in reduced overlap area for *ppB* and *of* components (identified in Figure 5.2). However, when S/D_{ext} is scaled the *ppB, gexB and GBof* components increases significantly due to the reduced distance between gate extension and active area (T_3 in

Figure 5.2). Therefore, we see a nearly 20% increase in C_{GB}/C_{paraB} as shown in Figure 5.5 and Figure 5.6 (b), (d). On the other hand, a slight reduction in C_{GT}/C_{paraT} is obtained, which is attributed to a reduction in gate-top electrode overlap (*gexT* component, Figure 5.2). It is observed that for both L_G and S/D_{ext} scaling, the total gate parasitic capacitance (C_{GG}) trend is dominated by the C_{GB}/C_{paraB} component and *if*, *ov* components contribution remains same as the structures defining them do not change.

Other than conventional capacitances (C_{ov}, C_{if}, C_{gex}), gate extension to active area capacitance (C_{ppB}) is significant contributor to parasitic capacitance making C_{GB} much higher (up to three times) than C_{GT}. Thus for similar dimensions the VNW MOSFET will have lower total parasitic capacitance than the planar MOSFET, whose total equivalent parasitic capacitance will be $2\times C_{GB}$. Hence, the VNW's asymmetric capacitance has an important role in determining the circuit performance of S_B and S_T configurations. Modeling of these capacitances through (5.1) - (5.12), enables better understanding in designing and calculating performance of VNW based digital (e.g., inverter with (S_B/S_T) configurations and sizing) and analog circuits.

5.2 Series Resistance Modeling

The series resistance ($R_{T/B}$) affects the drive current by reducing gate source overdrive and drain-source voltage. The effect of series resistance is expected to be more significant because of the reduced cross-sectional areas in nanowire devices.

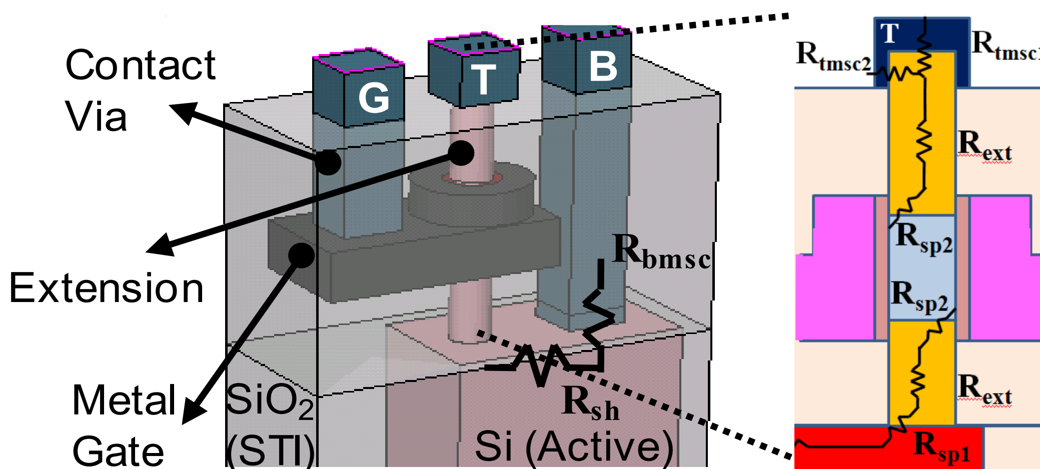

Figure 5.7 VNW FET 3-D isometric view with individual resistance components identified.

Hence, it is important to analyze the contribution of these resistances and their impact on circuit performance. The individual resistance components of top/bottom series resistance (R_T/R_B) are highlighted in Figure 5.7, these include: metal-semiconductor contact (R_{msc}), spreading (R_{sp}), sheet (R_{sh}) and extension (R_{ext}) resistances.

The definition of some of the physical parameters used in modeling of parasitic resistance components are tabulated in Table 5.2.

Table 5.2 Parameters used in standard resistance components.

contOL=contact overlap with nanowire	***contW***=contact width	$\boldsymbol{D_{NW}}$=Nanowire diameter
$\boldsymbol{L_{ext}}$=S/D_{ext} length	$\boldsymbol{L_{ov}}$=Gate-S/D overlap	$\boldsymbol{T_{sub}}$=Active area thickness
$\boldsymbol{\rho_{ext}}$=Extension resistivity	$\boldsymbol{\rho_{sub}}$=Substrate resistivity	$\boldsymbol{\rho_{c}}$=Contact resistivity

The bottom via-semiconductor contact resistance *bmsc* component is modeled using the standard contact resistance formula. With L_G scaling the contact area reduces leading to increase in resistance.

$$R_{bmsc} = \left(\sqrt{\rho_{sub}\,\rho_c}/contW\right)\coth\left(contW\sqrt{\rho_{sub}/\rho_c}\right) \quad \textbf{(5.13)}$$

Substrate sheet resistance component *sh* between via and nanowire, which is of length *F* (minimum feature size) and area $contW{\times}T_{sub}$ is given by standard sheet resistance formula.

$$\mathrm{R_{sh}} = \mathrm{\rho_{sub}} \times \mathrm{F}/(\mathrm{contW} \times \mathrm{T_{sub}}) \quad \textbf{(5.14)}$$

The extension region series resistance component *ext* is obtained by using resistance formula for a cylindrical structure. Due to the narrow circular-cross section it is the highest contributor towards series resistance which will be shown later. The effect of fringe gate field on extension is included as model parameter in (5.20) below.

$$\mathrm{R_{ext}} = 4\mathrm{\rho_{ext}}(\mathrm{L_{ext}} - \mathrm{L_{ov}})/\pi \mathrm{D_{NW}^2} \quad \textbf{(5.15)}$$

Spreading resistance component *sp1* arising due to carriers flowing from active area to narrow nanowire extension is modeled by modifying the model for planar MOSFET [143] to cylindrical structure. The junction depth is replaced by T_{sub}, channel thickness is equal to 0.5 D_{NW} and current flow width is equal to π D_{NW}.

$$\mathrm{R_{sp1}} = [2\mathrm{\rho_{sub}}/(\pi \times \pi \mathrm{D_{NW}})] \times \ln(0.75\,\mathrm{T_{sub}}/0.5\,\mathrm{D_{NW}}) \quad \textbf{(5.16)}$$

Similarly, the spreading resistance component *sp2* arising due to carriers flowing from nanowire extension into channel, which is present on both bottom and top of the channel is

modeled by considering junction depth equal to 0.5 D_{NW}, accumulation layer thickness X_c equal to 2.5/3.2nm for NMOS/PMOS (obtained from TCAD simulation results).

$$R_{sp2} = [2\rho_{ext}/(\pi \times \pi D_{NW})] \times \ln(0.75\, D_{NW}/2\, X_C) \quad \textbf{(5.17)}$$

As shown in Figure 5.5, metal-nanowire top contact resistance (R_{tsmc}) can be divided into two parallel resistance components: top (R_{tsmc1}) and cylindrical surfaces of nanowire (R_{tmsc2}). The model for R_{tmsc1} can be obtained from R_{bmsc} by letting the dimension of current flow as D_{NW}×D_{NW}:

$$R_{tmsc\,1} = \left(\sqrt{\rho_{ext}\,\rho_c}/D_{NW}\right) \times \coth\left(D_{NW}\sqrt{\rho_{ext}/\rho_c}\right) \quad \textbf{(5.18)}$$

The model for R_{tmsc2} can be obtained by modifying definition of transfer length (L_T) to consider 100% overlap of metal over nanowire, instead of 75% considered in [144] as (5.19), where $L_T = \sqrt{(\rho_c D_{NW} / 4\rho_{ext})}$.

$$R_{tmsc\,2} = (4\rho_{ext}\, L_T/(\pi D_{NW}^2)) \times \coth(contOL/L_T) \quad \textbf{(5.19)}$$

It is also noted that, the structure with overlap of top metal with top nanowire, as opposed to non-overlap structure, has a lower contact resistance due to larger circular contact area. So, the overlap structure is a better option in order to reduce the top resistance and decrease the difference with bottom resistance. Using the individual components (5.13) - (5.19), the top and bottom resistances are given by,

$$R_B = \beta_{bmsc}\, R_{bmsc} + \beta_{sh}\, R_{sh} + R_{sp1} + \beta_{ext}\, R_{ext} + R_{sp2} \quad \textbf{(5.20)}$$

$$R_T = (R_{tmsc1}\, R_{tmsc2})/(R_{tmsc1}+R_{tmsc2}) + R_{ext} + R_{sp2} \quad \textbf{(5.21)}$$

where a fitting parameters β_{bmsc} accounts for the carrier density modulation at metal via-semiconductor interface due to gate fringing field, β_{sh} accounts for the effect of gate fringing field on active region carrier concentration, and α, β_{ext} (unequal due to asymmetric structure) are used to consider the dependence of R_{ext} on gate structure and gate voltage. It is observed that the value of β_{ext} is smaller than α, as the bottom extension experiences much larger gate fringing field due to the longer gate extension at bottom. The introduction of fitting parameters to account for gate voltage dependent modulation is justified, as seen in the case of carrier density in the device simulations, for with and without isolation oxide in Figure 5.8.

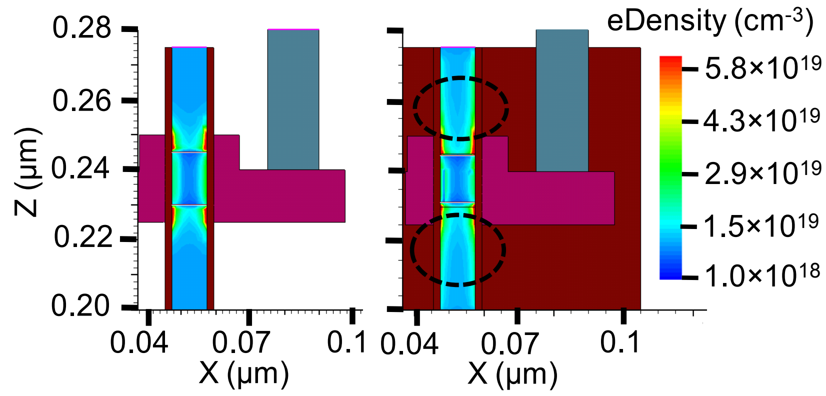

Figure 5.8 Electron (e) density profile in the device cross section through nanowire centre shown at V_G=V_{DD} and V_D=0.05V to highlight the impact of isolation oxide.

We see that the electron density in extension is increased (highlighted by black dotted circle) in presence of isolation oxide, which has enhanced gate field. Similarly, the mobility is reduced in presence of isolation oxide, accounted by gate dependent mobility degradation coefficient (θ) [145]. Thus the actual contribution of R_{ext}, R_{sh} and R_{bmsc} towards total resistance needs to be parameterized to consider the effect of gate fringing field.

Device resistance R_{ON} is calculated as I_{ON}/V_{DD} (where I_{ON} = I_D at V_{DS}=V_{GS}=V_{DD}) and S/D series resistance R_{TB} (R_T+R_B) is extracted by extrapolating the curve of R=V_{DS}/I_{DS} (V_{DS}=50mV) versus $(V_{GS} - V_{th} - V_{DS}/2)^{-1}$ and finding the R intercept as shown in Figure 5.9.

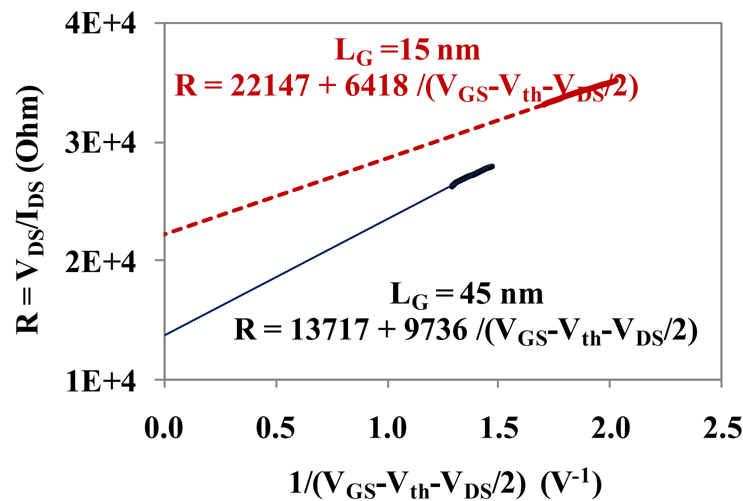

Figure 5.9 R_{TB} extraction methodology shown for NMOS VNW for L_G = 45 nm and 15 nm, S/D_{ext} = 30nm.

Further, the R-intercept corresponds to the value θ×slope + R_{TB}. The value of θ is obtained from simulations of large diameter NW MOSFETs with no extensions, which diminishes extension resistance. Following the same procedure as earlier, the intercept now obtained is only θ×slope

and independent of R_{TB}. The value of θ is obtained as 0.7 V^{-1}, 0.4 V^{-1} for NMOS and PMOS respectively.

Extracted R_{ON} and R_{TB} are shown in Figure 5.10 (a)-(b) for NMOS and PMOS with varying L_G and S/D_{ext} after taking correction parameter θ [145] into account. Moreover, the individual resistances contributing to R_{TB} are shown in Figure 5.10 (c)-(d). The fitting parameters ($\alpha + \beta_{ext}$) dependence on gate voltage can be obtained from plot of R versus $(V_{GS} - V_{th} - V_{DS}/2)^{-1}$. For a typical NMOS device of L_G=45nm, S/D_{ext}=30nm the value of $\alpha + \beta_{ext}$ = 0.72/0.12 corresponding to $(V_{GS} - V_{th} - V_{DS}/2)^{-1}$ = 1.2 V^{-1}/ 0 V^{-1} respectively.

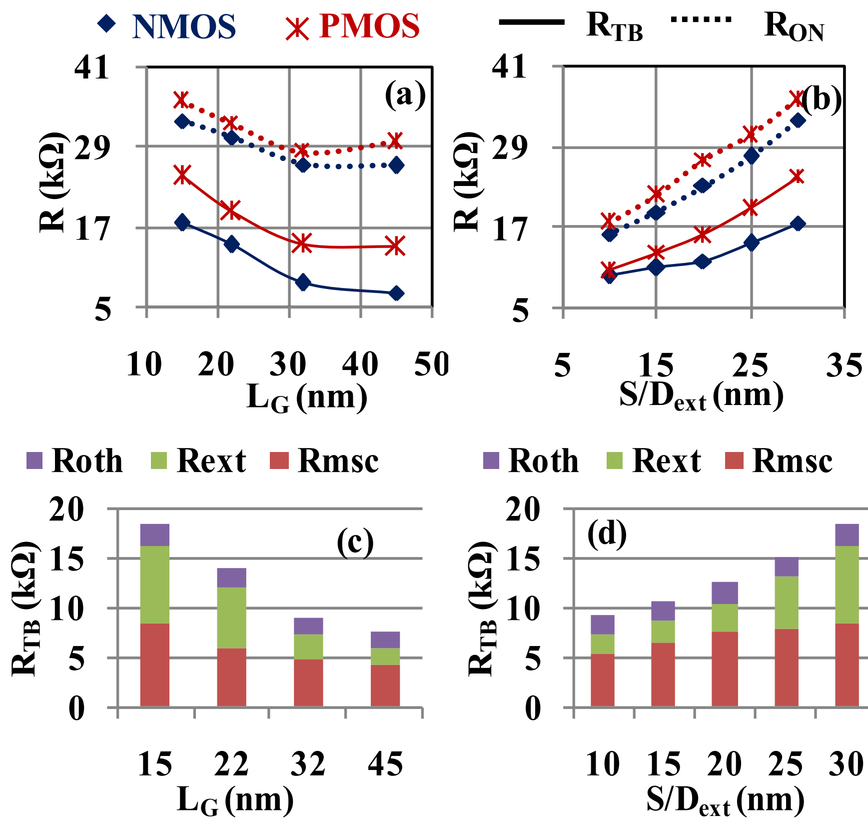

Figure 5.10 Extracted R_{TB}, R_{ON} versus (a) L_G (S/D_{ext} = 30nm) and (b) S/D_{ext} (L_G = 15nm) and individual resistance components contributing to NMOS R_{TB} versus (c) L_G and (d) S/D_{ext}, where R_{oth} represents the sum of *sh* and *sp* resistances.

From Figure 5.10 (a)-(b), we see that R_{ON} of NMOS and PMOS are nearly equal due to drive matching obtained by increasing the D_{NW} of PMOS [57], [127]. Further, it is observed that more than 50% of ON resistance is contributed by R_{TB}, which is predominantly due to the narrow S/D extension regions and high contact resistance. In Figure 5.10 (a), it is seen that R_{TB} and R_{ON} increases with reduction in L_G due to increase in contact resistance (reduced F). The additional rise in R_{ON} for L_G change from 32nm to 22nm is due to different V_{DD} for these nodes i.e., 1V and 0.8V respectively. In Figure 5.10 (b), we observe R_{ON} and R_{TB} drop strongly with

S/D_{ext} due to reduction in R_{ext}, improving *ON* current [127]. Figure 5.10 (c)-(d) show contribution of R_{msc}, R_{ext} and R_{oth} (= R_{sh}+R_{sp}) towards R_{TB}. We note that R_{msc} and R_{ext} contribute nearly equally to the total resistance and make 80-90% of total resistance R_{TB}. From Figure 5.10 (c), it is observed that, with L_G scaling the contact resistance increases due to proportional scaling of contact dimensions. The increase in extension resistance contribution is due to reduced modulation of bottom extension resistance by the gate extension, due to reduction in the dimensions of gate pad (*GaExtWid*, P_4 identified in Figure 5.2) with scaling of L_G. In Figure 5.10 (d), the decrease in R_{msc} component is attributed to the reduced bottom contact proximity to gate, which enhances the carrier concentration in metal-semiconductor interface region. Also the decrease in R_{ext} is due to reduced S/D_{ext} length. The resistance components *sh* (5.14) and *sp* (5.16 – 5.17) do not scale significantly due to weak dependence on L_G and S/D_{ext} dimensions.

Since VNW is asymmetric having different R_T and R_B, we use transconductance (g_m) method [146] along with R_{TB} (Figure 5.10), to extract R_T and R_B separately.

$$R_T - R_B = [g_m(S_B) - g_m(S_T)] / [g_m(S_B) \times g_m(S_T)] \quad \textbf{(5.22)}$$

The effect of substrate or body bias is neglected in (5.22) due to absence of substrate contact in these devices. Figure 5.11 shows R_T and R_B extracted using (5.22) and modeled using (5.20)-(5.21), with L_G and S/D_{ext} scaling.

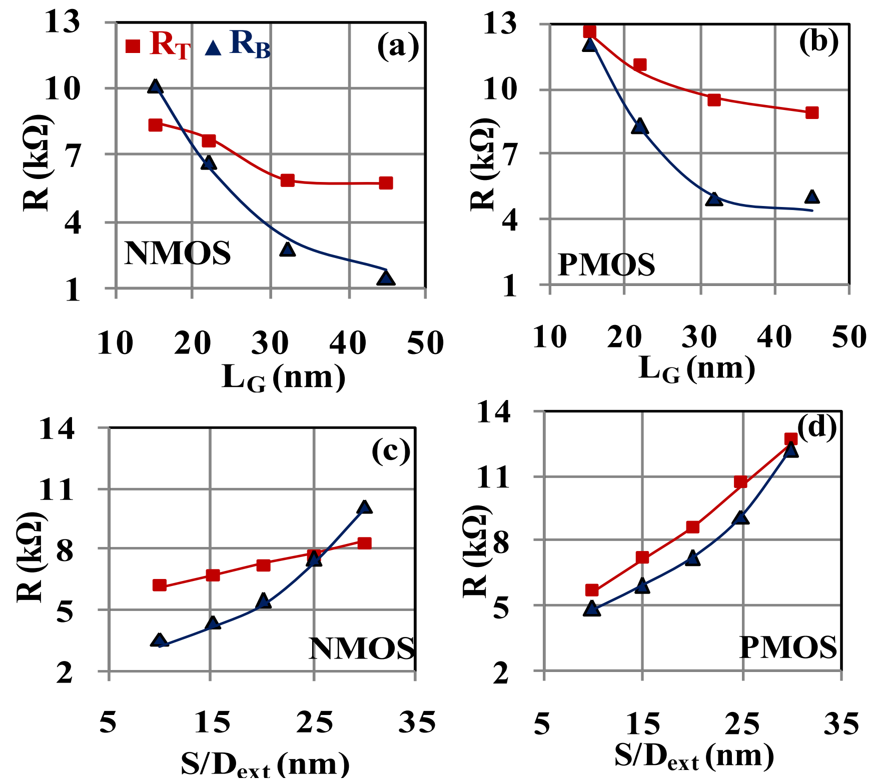

Figure 5.11 Simulated (symbol) and modeled (line) R_T (red) and R_B (blue) versus L_G (a) NMOS (b) PMOS, and with respect to S/D_{ext} (c) NMOS and (d) PMOS.

It is observed that for both NMOS and PMOS the modeled R_T and R_B fit well with the values extracted from simulation, both for L_G and S/D_{ext} scaling. We observe the resistances in PMOS are larger than in NMOS, which can be explained by differences in carrier density (n/p=2), mobility (μ_n/μ_p =1.7) and nanowire cross sectional area (D_{NWp}/D_{NWn} =1.5). These ratios are the typical values obtained from device simulation. By substituting the ratios in the values of the parameters in extension resistance model (5.15), we obtain R_{ext_p} =1.7 R_{ext_n}. Also, we see that R_T is larger compared to R_B due to higher R_{ext} contribution (low gate fringe field) and top contact over narrow nanowire. Thus a S_T device with R_T as the source resistance will have lower drive current (lower gate overdrive), when compared to S_B device [127], [147].

It is to be noted that in Figure 5.11 (a) and (c), when L_G and S/D_{ext} are scaled for NMOS device there is crossover of R_T and R_B resistances at 18 nm and 25 nm respectively, which is not observed for the case of PMOS. This is due to the difference in modulation of nanowire extension regions arising due to different nanowire diameters in NMOS (D_{NW} = 10 nm) and PMOS (D_{NW} = 15 nm). Due to larger diameter in PMOS devices the crossover is observed at 15 nm and 30 nm respectively for L_G and S/D_{ext} scaling.

The L_G scaling (S/D_{ext} = 30nm) in Figure 5.11 (a)-(b) shows that bottom resistance R_B increases significantly due to the diminishing contact size. Also, due to decrease in fringing field lines between gate extension and active region, we find that fitting parameter β_{sh} increases with decreasing L_G. The parameter β_{bmsc} varies from ~1 (nearly no modulation) for 30nm to 0.35 for 10nm extension lengths. We see that the top resistance R_T is less dependent on L_G scaling as the top extension region in device structure above the gate remains same except for the top metal contact overlap over nanowire, which is 30nm, 20nm, 15nm, 10 nm for L_G 45nm, 32nm, 22nm, 15nm respectively. Thus, the decrease in overlap length results in 1-2 kΩ increase in R_T as observed. The crossover of R_T and R_B is observed for different L_G in NMOS and PMOS due to the different nanowire diameters.

As shown in Figure 5.11 (c)-(d), when S/D_{ext} is scaled (L_G=15nm) from 30nm to 10nm nearly 50-60% reduction in series resistance is obtained. We note that R_B decreases rapidly because of combined contribution of reducing R_{ext}, R_{sh} and R_{bmsc}. As S/D_{ext} is reduced, gate fringing field effect on the bottom extension increases (C_{GB} increases with S/D_{ext} scaling as shown in Figure 5.4 (b)), resulting in decrease in value of β_{ext}, reducing R_{ext} and explaining the observed trend. Moreover, the distance between gate bottom to active area and gate bottom to metal via-semiconductor interface also decreases, which are considered in model by reducing value of β_{sh}

and β_{bmsc} with S/D_{ext}. It is observed that R_T varies linearly with S/D_{ext}, which can be explained by proportional decrease in R_{ext} and constant value of α, since the gate fringe field lines between gate top and top extension remain same (C_{GT} is almost constant with S/D_{ext} scaling as shown in Figure 5.4 (b)). Further, it is observed in Figure 5.8 (c)-(d) that the reduction of R_T with S/D_{ext} is larger for PMOS than NMOS, which can be explained by larger nanowire diameter (=15nm) in PMOS devices. Due to the larger D_{NW}, the gate top (disc shape) surface area increases, resulting in increased capacitance ($C_{GTp} > C_{GTn}$). So in PMOS when S/D_{ext} is scaled more gate field lines are confined in small dielectric volume leading to increased R_{ext} modulation. This results in the larger slope of R_T with S/D_{ext} for PMOS than NMOS. Hence the device/circuit performance is dependent on L_G, S/D_{ext}, D_{NW} and *T/B* electrode asymmetry.

5.3 Summary

In this chapter the models for parasitic resistances and capacitances in a vertical nanowire CMOS are presented, and are shown to match well with extracted parasitic from simulations for varying L_G, S/D_{ext} and D_{NW}. The models incorporate the influence of the gate structure and voltage on extension resistance. The results depicts that nearly 90% of the total series resistance is contributed by the metal semiconductor contacts and extension resistance. The parasitic capacitances are well modeled with parallel-plate and cylindrical fringe components with good match to simulations. It is found that the gate-active/extension are dominating contributors to parasitic capacitance. Moreover, the total parasitic capacitance is nearly 1.5 – 2 times the channel capacitance. The combined resistance and capacitance parasitic determine the performance of devices and circuits (delay). Thus, the structural asymmetry will impose layout restrictions in circuit design using VNWFET devices. The parasitic models presented here can be used in SPICE simulators for faster circuit performance analysis of VNW devices.

6 CHAPTER

CIRCUIT PERFORMANCE

This chapter discusses the circuit performance of VNW devices in detail. The analysis of digital circuit performance is carried out using CMOS inverter and is benchmarked with existing literature for FinFET and planar MOSFET inverters. To start with detailed insight of static characteristics of VNW CMOS inverter and the use of S/D_{ext} as tuning parameter to obtain required gain and noise margin is provided. Next, a comparison of dynamic performance of the inverters is shown between their VNW, FinFET and planar MOSFET implementations with respect to channel length scaling, which establishes a better performance of VNW devices. For 15nm VNW MOSFET, complete performance analysis of a CMOS inverter is presented with respect to S/D extension length, S/D asymmetry and impact of different layouts arising thereby. To complete the digital circuit analysis, we present inverter delay prediction with the help of parasitic capacitance models developed in previous chapter along with the effective current delay model [148]. Further, analog circuits with 15nm VNW MOSFET are analysed for device and circuit performance metrics such as transconductance (g_m), output conductance (g_{DS}), gain, 3dB bandwidth and f_T of intrinsic device, common source (CS) amplifier and compared with equivalent FinFET devices at same node.

6.1 Digital Performance

6.1.1 VNW CMOS Inverter Voltage Transfer Characteristics (VTC) Analysis

Figure 6.1 shows the CMOS inverter VTC for different device structures. In VTC, it is important to analyse the regions highlighted by solid line circle and dotted line circles. Inside the solid line circle, we observe sharper transition of multi-gate (MG) CMOS than the planar CMOS. Inside the dotted circle we observe that, around the gain value -1 (used for NM extraction), the MG CMOS have gradual gradient as compared to planar CMOS. To design a CMOS circuit with required noise margins, it is important to understand reason for such behavior.

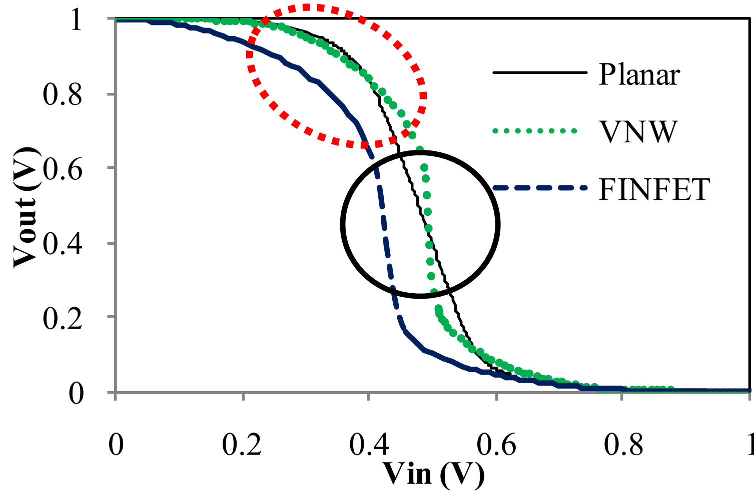

Figure 6.1 CMOS VTC for VNW, FinFET and planar MOSFET. FinFET VTC is not symmetric due to mismatch in drives of its NMOS/PMOS Fin devices. Solid line circle highlights the switching transition region and the dotted circles highlights the gradient around the NM extraction point.

The region of a gradual fall in V_{out} (dotted circle) observed in MG devices can be understood by considering the impact of series resistance on VTC. We perform a pseudo analysis using planar CMOS (L_G=45 nm, PTM SPICE model [149]) with external series resistances. Figure 6.2 shows planar CMOS with series resistances and corresponding VTC characteristics for 45nm devices. It can be observed that when $R_S=R_D=0\Omega$, the inverter has highest NM performance. For the other three cases, when some series resistance is added, it leads to degradation of NM values. Further it can be observed that the degradation with $R_D=12k\Omega$ and $R_S=0\Omega$ is large as compared to the case when $R_S=12k\Omega$ and $R_D=0\Omega$. The worst NM is obtained for the case when $R_S=R_D=12k\Omega$ (denoted by red lines in Figure 6.2). This analysis implies that, the reason for deteriorated VTC highlighted by dotted line circle in Figure 6.1 is due to large drain series resistance of VNW, and it can be improved with reduction in the series source-drain resistance by scaling of S/D_{ext} to lowest possible values.

In order to understand how the series resistance determines the shape of VTC characteristics, we examine the device (NMOS, PMOS) I_D-V_{DS} characteristics. We take this approach, as VTC can be constructed from device I_D-V_{DS} characteristics. For this study, we transfer the PMOS characteristics so that its current is positive and then the voltage axis is right shifted by V_{DD}, so that it overlaps with the NMOS voltage range as shown in Figure 6.3.

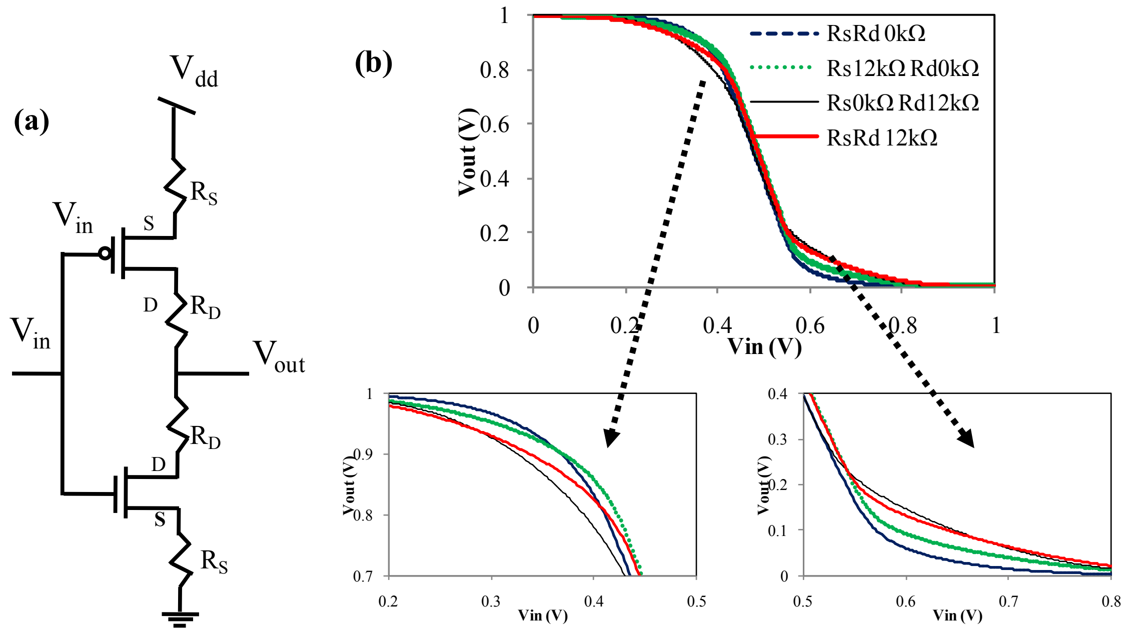

Figure 6.2 (a) Resistive loaded CMOS circuit schematic. (b) Impact of R_D, R_S on VTC of planar CMOS at 45nm. Degradation in NM is highlighted in insets.

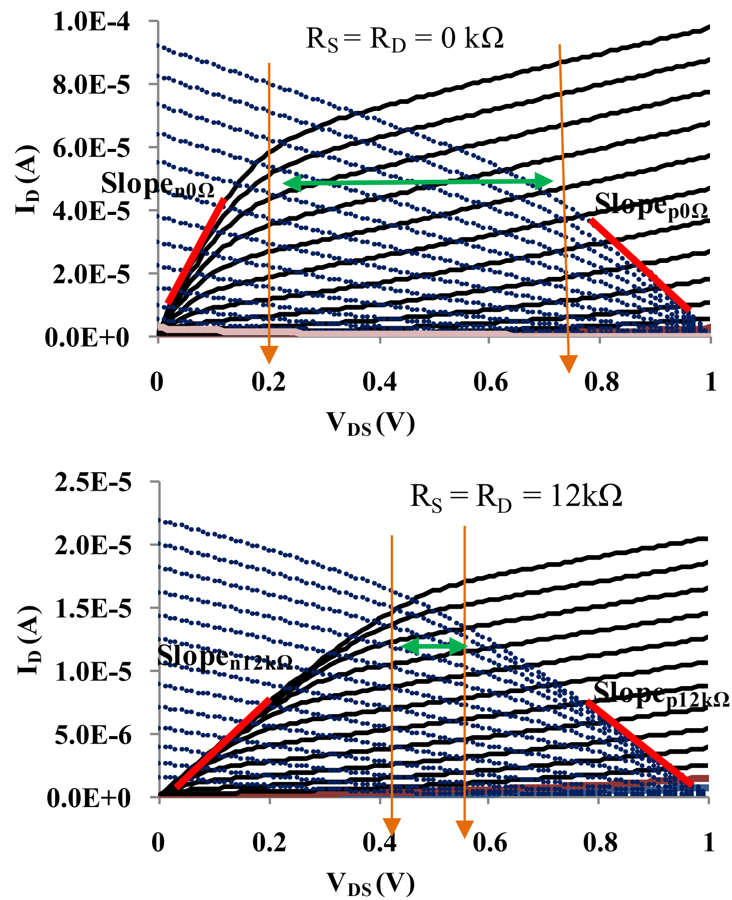

Figure 6.3 Planar NMOS, PMOS I_D-V_{DS} characteristics with 0, 12kΩ series resistance. The vertical down directing arrows indicate the V_{DSsat} points, the double ended arrow represents the switching region of CMOS and the inclined lines represent slope in linear region.

In Figure 6.3, we observe that with increase in series resistance the V_{DSsat} (denoted by vertical down arrows) of devices increases from 0.2V - 0.25 V to ~0.55 V. Further the series resistance decreases the slope (denoted by inclined lines) of device characteristics in the linear region i.e., $Slope_{n0\Omega} > Slope_{n12k\Omega}$. The range of V_{out} over which the PMOS device is in linear region of operation is larger. This is the primary cause for the gradual gradient characteristics highlighted by dotted line circle in Figure 6.1.

Similar study is performed on VNW devices for L_G=45nm and S/D_{ext} = 10/30nm as shown in Figure 6.4. The reasoning explained earlier is applicable for this case also. To clarify further, the VTC of VNW inverter is constructed from the intersection points of NMOS/PMOS I_D-V_{DS} of Figure 6.4, which is found to match well with simulation results as shown in Figure 6.5. In Figure 6.5, the data points denoted with symbols in dotted circles correspond to the linear region of device.

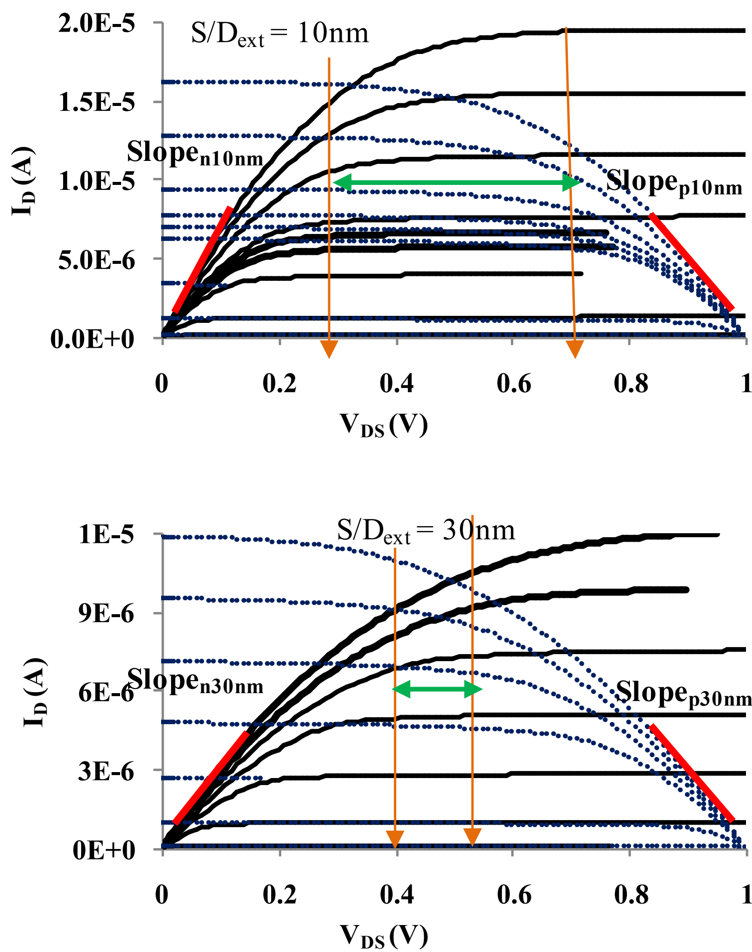

Figure 6.4 VNW NMOS, PMOS I_D-V_{DS} characteristics with S/D_{ext} = 10/30nm resistance.

In order to explain the difference in behavior during transition region of inverter VTC for planar and MG devices (highlighted by solid line circle in Figure 6.1), we consider Figure 6.3 and Figure 6.4. The double-ended arrows correspond to the switching region of CMOS VTC. In this range, the devices are in full saturation and the VNW (Figure 6.4) have low λ_{CLM} (channel length modulation) or minimum short channel effects (SCE), when compared to planar MOS devices with large λ_{CLM} (Figure 6.3). This results in sharper transition and higher gains in VNW (MG) inverter as compared to planar CMOS which has higher λ_{CLM} value.

Further, it is observed that with decrease of S/D_{ext} the gain of inverter almost doubles as shown in Figure 6.5 (b). From the -1 slope points of dV_{out}/dV_{in} (gain), we observe that NM increases by 40-80 mV, when we decrease the S/D_{ext} from 30 to 10nm. The larger value of NM is a result of a smaller value of V_{DSsat} for the VNW device for a smaller value of S/D_{ext}. This shows that S/D_{ext} can be tuned to improve CMOS VTC performance (NM/gain).

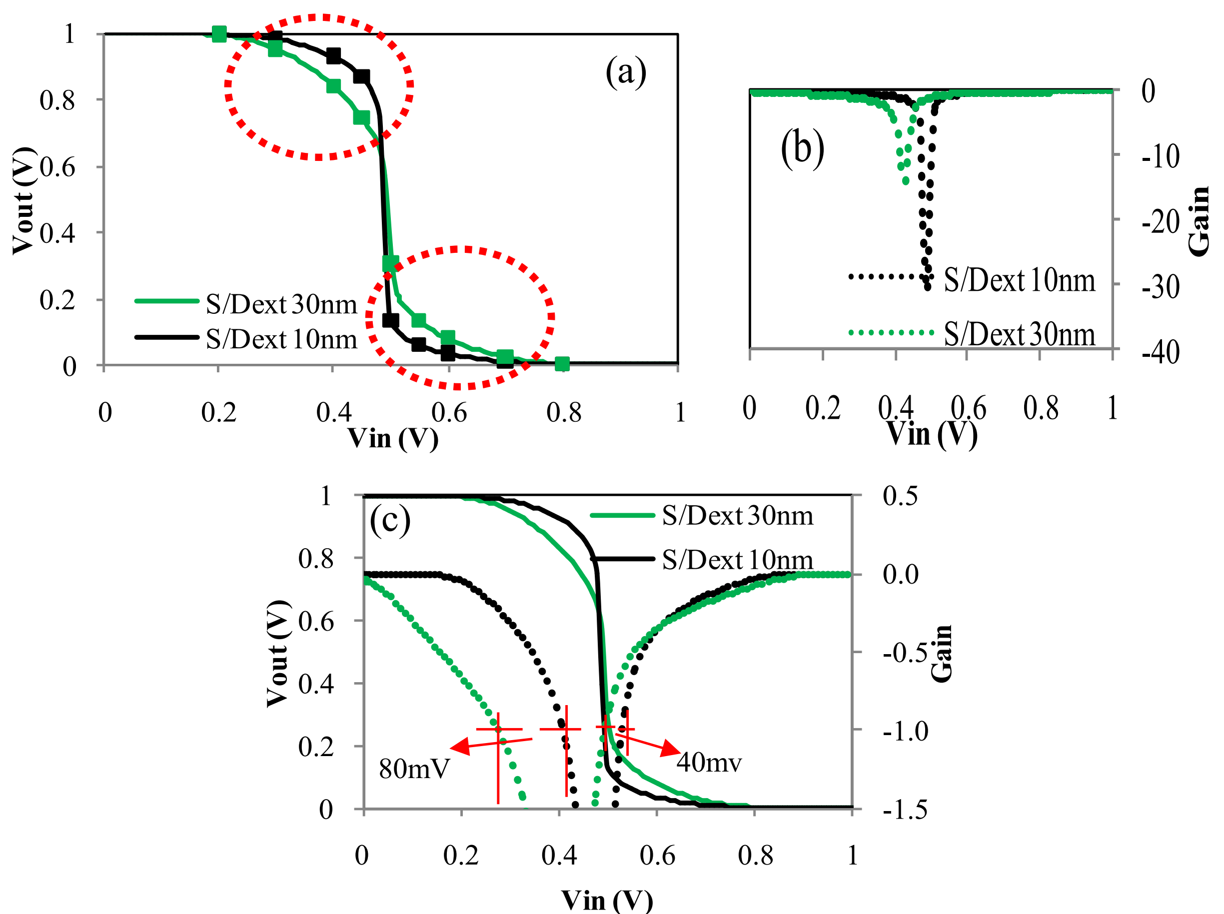

Figure 6.5 (a) VNW VTC simulated (lines) and VTC generated using I_D-V_{DS} characteristics (symbols) for L_G=45nm, S/D_{ext} =30/10nm. (b) Gain of inverter for varying S/D_{ext}. (c) NM extraction.

6.1.2 Benchmarking of Inverter Transient Response

VNW inverter is compared with FinFET [79] and planar [81] based CMOS for layout area, ring oscillator (RO) power/stage ($C_0 V_{DD}^2 f$) and delay/stage as shown in Table 6.1, where F is minimum feature size. It is observed that when compared with planar (FinFET), VNW has 50% (45%) area saving and 65% (50%) lower in delay. Moreover, VNW show ~75% lower power consumption than FinFET (for same L_G and S/D_{ext}) and hence has better overall performance.

Table 6.1 Performance comparison of planar, FINFET and VNW inverters for 45 nm channel length.

Device (L=F=45 nm)	Planar	FinFET	VNW
V_{DD} (V)	1.1	1.0	1
Area	$60F^2$	$55\ F^2$	$30\ F^2$
RO Delay/stage (ps)	17	12	6.0
RO Power/stage (μW)	28.5	26	13.8
RO Power/stage/MHz (pW)	484	312	83

VNW inverter transient analysis for varying L_G is shown in Figure 6.6. It is observed that the high to low delay (T_{pHL}) and low to high delay (T_{pLH}) of VNW inverter are almost equal. This is due to larger diameter nanowire in PMOS used to match the drive current with NMOS. Also, with L_G scaling from 45 nm to 22 nm the delay almost reduces by 40-45%. Further we benchmark the VNW performance as shown in Figure 6.7. The delay variation for fan-out capacitance FO=1, with L_G for VNW CMOS (S/D_{ext} = 30 nm) is benchmarked with simulated 3D FinFET CMOS (with equivalent device dimension T_{ox} = 2 nm, L_{ext} = 30 nm, fin-thickness = 10 nm, fin-height = 30 nm), along with experimentally reported data for FinFET and planar CMOS [79], [82].

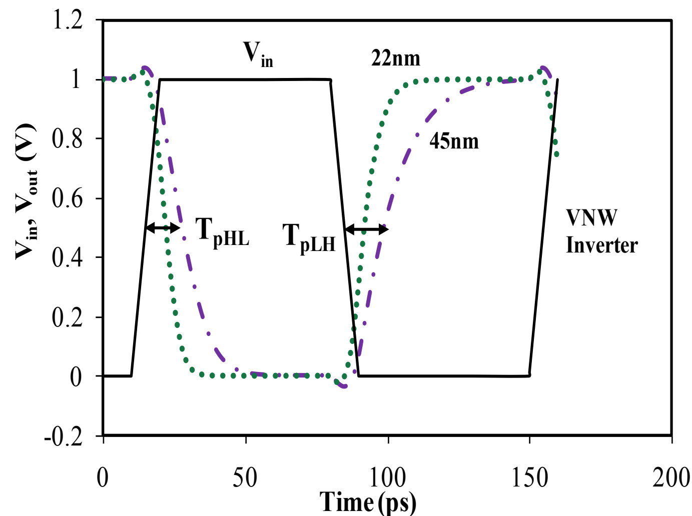

Figure 6.6 VNW inverter transient response for L_G=45, 22 nm, S/D_{ext} = 30nm and Diameter = 10/15nm (NMOS/PMOS).

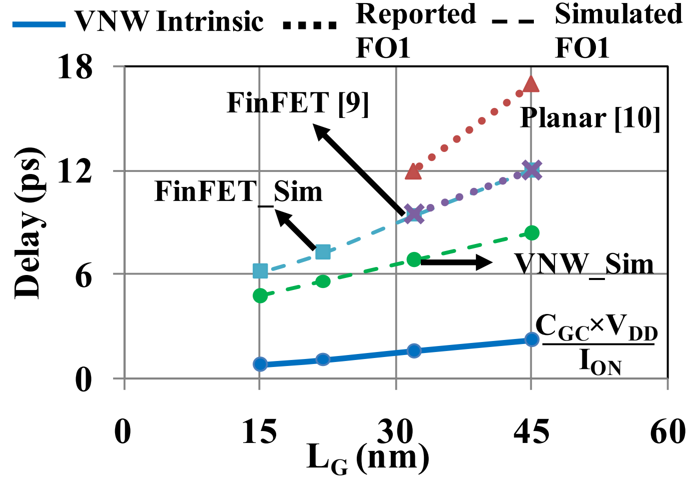

Figure 6.7 Benchmarking of VNW, simulated FinFET, experimentally reported FinFET and planar CMOS.

In Figure 6.7 the intrinsic gate delay of VNW MOSFET is also shown for reference. It is observed that despite large series resistance (S/D_{ext} = 30 nm), VNW CMOS shows better delay performance for different technology nodes and has nearly 40% lower delay than FinFET at 32 nm technology node. The intrinsic gate delay of VNW highlights the minimum gate delay and how additional parasitic contribute to delay when using these devices. From the benchmarking it can be concluded that VNW device based circuits have advantage of occupying least silicon area, consuming low power and provide least delay.

6.1.3 VNW CMOS Inverter Delay Analysis

In this section the performance of VNW CMOS inverter is analysed with respect to S/D asymmetry, S/D_{ext} and different layout schemes. Figure 6.8 (a-b) shows source as bottom electrode - S_B VNW CMOS inverter layout schemes (topview) implemented using drive-matched n and p FETs. To study the effect of within-device (marked 'w/o') parasitic and complete layouts L1, L2 (Figure 6.8 (a), (b)) parasitic, a two stage inverter chain is analysed in terms of its FO1 delay. In Figure 6.8, $IO_{overlap}$ defines input and output-interconnect overlap length, which contributes to layout parasitic. The total input and output interconnect length (IO_{length}) will also contribute to the layout parasitic. With L1 layout, the power rails (V_{DD}, V_{SS}) are in close proximity, which in circuit design will require two metallization layers to avoid shorting of V_{out} and V_{in} lines with V_{DD} and V_{SS} lines while routing. In L2 layout, the power rails can be defined with single metallization layer and are far apart, however at the cost of larger area and higher parasitic.

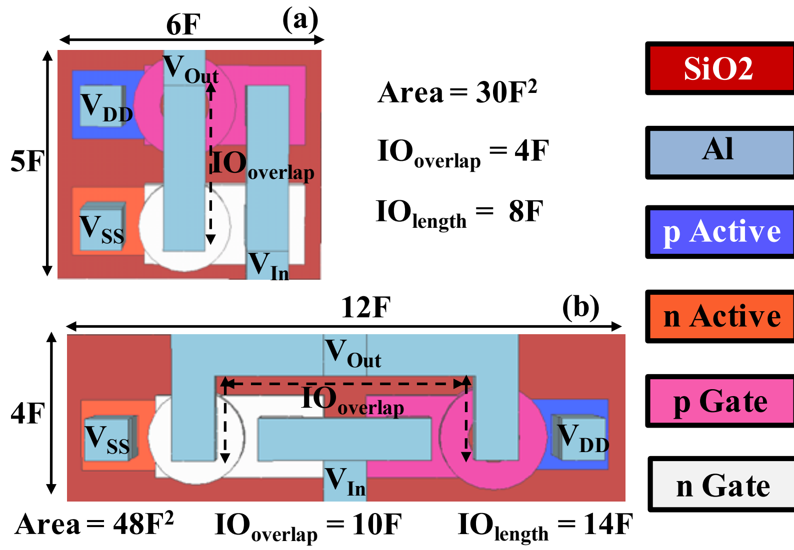

Figure 6.8 Topview of S_B inverter (a) L1 layout. (b) L2 layout. F is minimum feature size (15 nm).

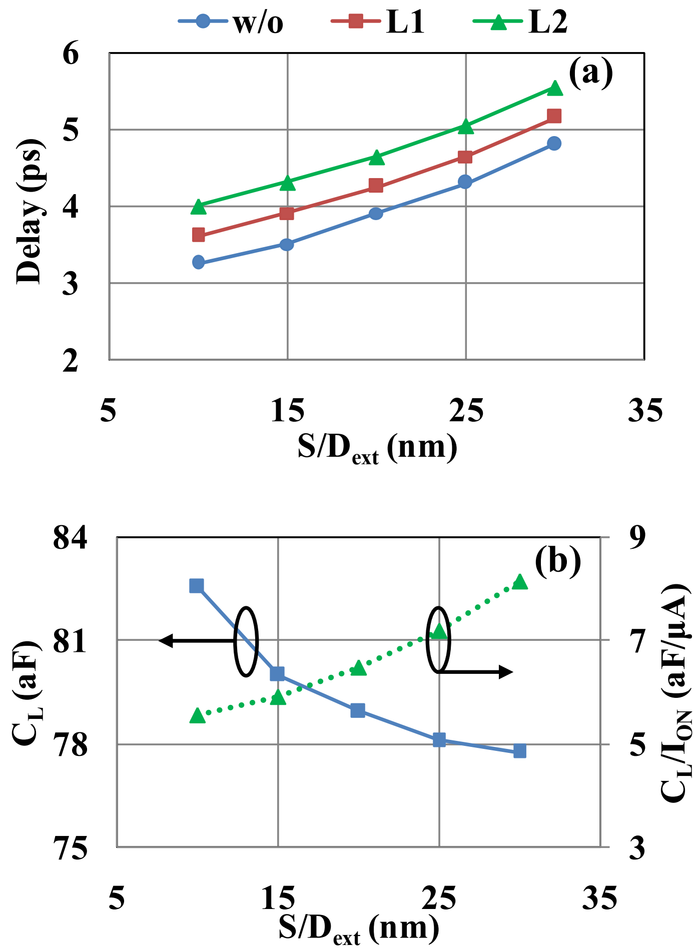

Figure 6.9 (a) Delay versus $S/D_{ext.}$ (b) Load capacitance (C_L) and circuit speed metric (C_L/I_{ON}) versus S/D_{ext} for S_B VNW CMOS $L_G = 15$ nm.

Figure 6.9 (a) shows delay trend with S/D_{ext} length, with delay reduction of 0.77 ps per 10 nm of S/D_{ext} length for w/o (only device parasitic), L1 and L2 layouts. We see that the reduction in delay with S/D_{ext} tends to slow down as S/D_{ext} is reduced. This can be explained by competing effects of increased drive current (reduced series resistance) and increased parasitic capacitance, as seen in larger increase in I_{ON} (~25%/10 nm, Figure 4.2) compared to proportionately smaller increase in extracted load capacitance (3%/10 nm, Figure 6.9 (b)). The same explanation is also borne out by plot of fanout capacitance (C_L) of first stage inverter and circuit speed metric (C_L/I_{ON}). Thus, we see that performance of NW devices is strongly limited by series resistance rather than parasitic capacitance at lowest possible value of 10 nm. Further, we note that the layout related parasitic increase the delay by 0.3 ps (L1) and 0.7 ps (L2), compared to w/o layout circuit. Since L2 inverter has larger layout parasitic ($IO_{overlap}$, IO_{length}) compared to L1 inverter, it has higher delay.

Figure 6.10 shows delay comparison for S_B and S_T (source as top electrode) inverters (10 nm S/D_{ext}). We see that with S_T, the delay is higher by ~65%. The increase in delay for S_T inverter cannot be explained by lower (~20%) drive current alone as seen in Figure 4.2. A contribution from increased parasitic capacitance (~33%, Figure 6.10) due to large gate to bottom (drain) electrode capacitance (C_{GB} or the gate-drain capacitance) enhanced by miller effect also needs to be taken into account. This combined effect of lower drive current and increase in C_L can account for increase in delay. This highlights that when designing VNW CMOS circuits, how tradeoff between layouts due to different routing schemes resulting in S_T/S_B, and speed needs to be taken into consideration. Further, we propose L1 kind of layouts for circuit design to obtain better performance.

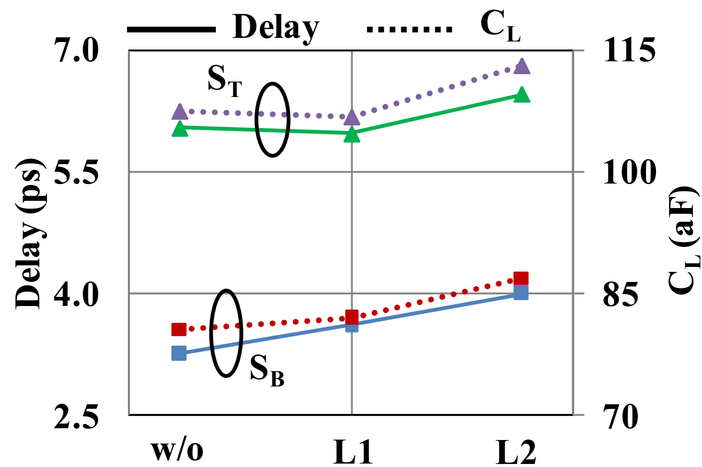

Figure 6.10 Impact of S/D asymmetry on delay performance and extracted C_L of different layouts.

In Figure 6.11, the delay of VNW S_B/S_T inverters is shown with respect to S/D_{ext} variation. It can be observed that the S_T inverters have larger delay than S_B inverters due to reasons stated earlier. The S/D_{ext} scaling in Figure 6.11 shows delay reduction of 0.7ps per 10nm, with reduction slowing down at 10nm. This behavior can be explained by competing effects from reducing R_{ext} and increased parasitic capacitance, with R_{ext} reduction being dominant over increase in parasitic capacitance.

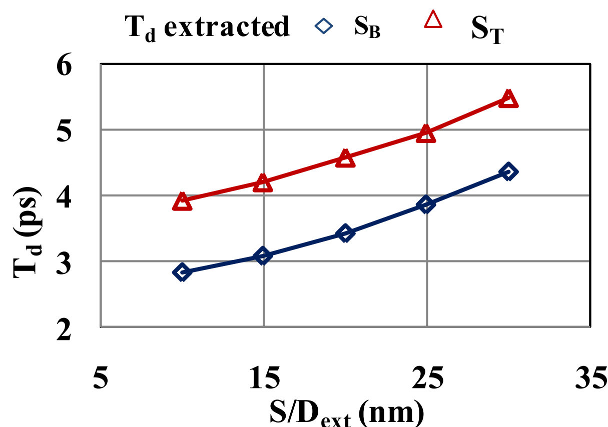

Figure 6.11 Delay and power variation with S/D_{ext} for S_B and S_T inverters.

From Figure 6.12, it is inferred that with S/D_{ext} scaling, power consumption ($C_L V_{DD}^2 f$) increases at a faster rate and the S/D_{ext} for which optimum performance is achieved can be obtained with the help of power delay product (PDP). PDP trends suggest that S_B devices with S/D_{ext} = 10 nm provide the best performance with a marginal increase in PDP when compared to device with larger S/D_{ext}. It is evident that the PDP of S_B is smaller than S_T highlighting the better performance of S_B inverters. Thus, S/D_{ext} is an important design parameter while designing circuits to obtain better performance.

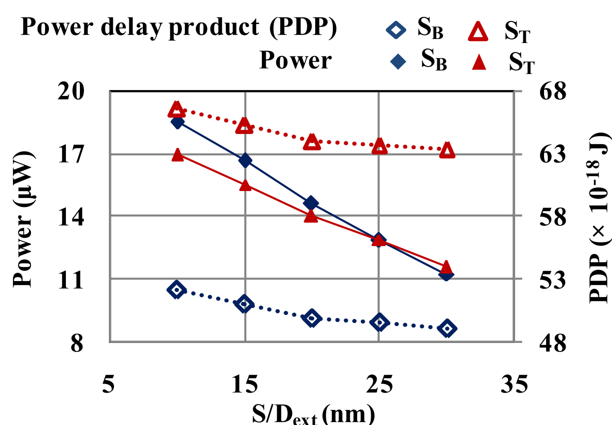

Figure 6.12 Power and power delay product (PDP) variation with S/D_{ext} for S_B and S_T inverters.

6.1.4 VNW CMOS Inverter Delay Modeling

Impact of parasitic on circuit performance is studied for L_G=15nm, VNW CMOS inverter dynamic behavior. We implemented different inverter schemes using drive matched NMOS-PMOS with S_B (source as bottom electrode) and S_T (source as top electrode) devices respectively. A two-stage inverter is built as shown in Figure 6.13, showing important capacitances for studying the effect of S/D_{ext} dependent parasitics on *FO1* delay. For different layout schemes, the input and output interconnect parasitic are also different, which further contribute to the existing asymmetry of device [127].

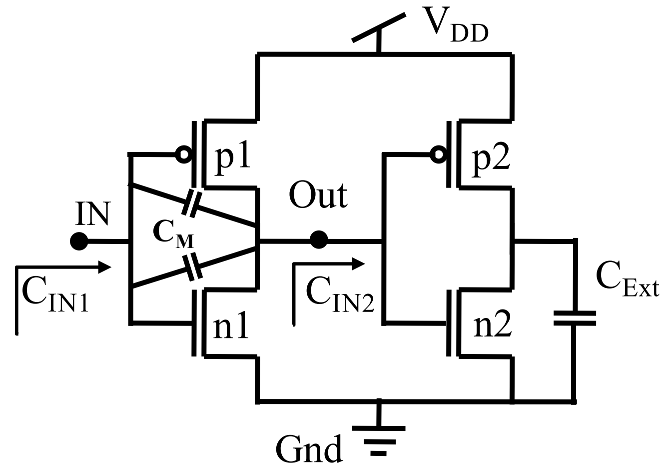

Figure 6.13 Schematic diagram of two stage inverter chain.

Load capacitance (C_L) seen by first stage inverter at node *Out* can be extracted from transient simulation or calculated from 1st stage output parasitic (miller amplified), and 2nd stage input capacitance as (6.1), where, the factor M is miller coefficient and is taken as 1.5 [150]. The input capacitance C_{IN2} is estimated from the weighted contribution of *ON* and *OFF* state capacitances of NMOS and PMOS during input transitions. For example, during the output-rise transition to 50% of V_{DD}, the transistor *p2* changes state from *OFF* to *ON*, and *n2* remains in *ON* state. Thus, *OFF*:*ON* ratio 0.25:0.75 [150] can be used to obtain C_{IN2} as in (6.2).

$$C_L = M \cdot C_M + C_{IN2} \tag{6.1}$$

$$C_{IN2} = 0.25\, C_{G_OFF} + 0.75\, C_{G_ON} \tag{6.2}$$

where $C_{G_OFF} = C_{GBn} + C_{GTn} + C_{GBp} + C_{GTp}$ and $C_{G_ON} = C_{GBn} + C_{GTn} + C_{GCn} - 2\, C_{ifn} + C_{GBp} + C_{GTp} + C_{GCp} - 2\, C_{ifp}$. All these capacitances are modeled in chapter 5. It can be observed in C_{G_ON} the inner fringe parasitic components (C_{if}) are subtracted to account for their absence

when device is ON [150]. Further, the miller capacitance (C_M) for inverter with S_T devices is C_{GBn} + C_{GBp} as the bottom electrodes act as the drain, whereas for inverter with S_B devices it is C_{GTn} + C_{GTp} as the top electrode acts as the drain.

The CMOS inverter delay (T_d) is obtained from transient simulation or calculated using the effective current model [148],

$$T_d = 0.5C_L \times V_{DD}/I_{eff} \quad \textbf{(6.3)}$$

where I_{eff} is average of current at V_G=V_{DD}, V_D=0.5V_{DD} and V_G=0.5V_{DD}, V_D=V_{DD}. The value of C_L can be obtained either from inverter buffer simulation or calculated from (6.1) using capacitance component models presented in section 5.1. Figure 6.14 shows calculated inverter delay fit well (less than ~5% error) with the extracted delay. This highlights the accuracy of the developed parasitic models for the VNW structure.

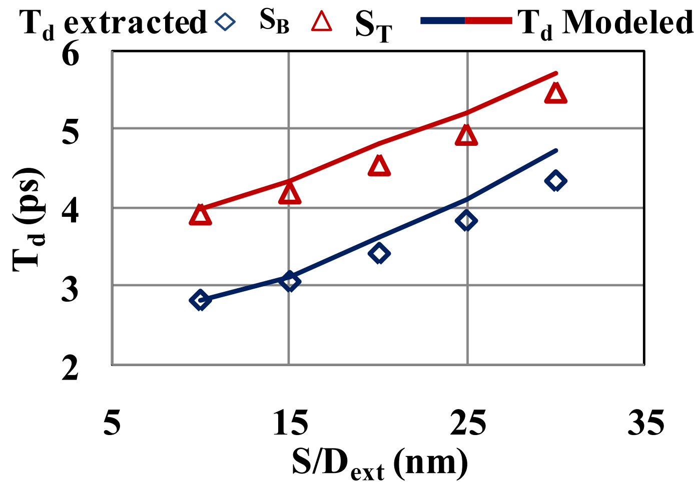

Figure 6.14 Delay (*T_d*) extracted-modeled and power versus *S/D_{ext}* for *S_B* and *S_T* VNW CMOS (*L_G*=15nm).

In Figure 6.14 we also observe that for S_T inverter delay is nearly 50% higher. This increase in delay can be explained by higher source resistance or R_T, which results in lower gate overdrive or drive current. Also a contribution from higher parasitic capacitance is also an important factor. Due to large gate to bottom electrode capacitance (C_{GB} or the gate-drain capacitance) enhanced by miller effect resulting in larger C_L in S_T CMOS. This combined effect of increased series resistance, and increased C_L can explain the increase in delay and is verified using the delay model as seen in Figure 6.14. This emphasizes the importance of parasitic models, when designing and analyzing circuits with different layout schemes arising due to S_T/S_B devices.

6.2 Analog Performance

Multi-gate transistors such as nanowire FETs have gained immense importance due to their immunity to short channel effects and ability to scale device dimensions, below the limits faced by planar MOSFETs. In section 6.1 the studies are carried out to analyze the performance of VNW devices in digital logic circuits and memory cells. The results highlighted that these devices and VNW CMOS has promising future for low power and efficient applications. In this section we study application of VNW CMOS in analog circuits. For the study of basic analog performance we implement single stage common source (CS) amplifier as test vehicle.

Figure 6.15 shows the circuit topology of resistive loaded CS amplifier implemented for analog performance analysis. First, we optimize load resistance R_L by varying its value to see the variation of V_{out} and gain (dV_{out}/dV_{in}) versus V_{in} as shown in Figure 6.16. It is observed that in order to have amplifier behavior i.e, gain > 1 the minimum load required is R_L = 38 kΩ. The large value of R_L required is due to the large $R_{S/D}$ in the VNW devices and is a special characteristic of VNW devices. This minimum R_L is a function of S/D_{ext} of the VNW device and it would also change if parallel VNWs are used to increase drive strength. Such high values of resistances can be obtained by appropriately biasing VNW PMOS devices in diode configuration mode.

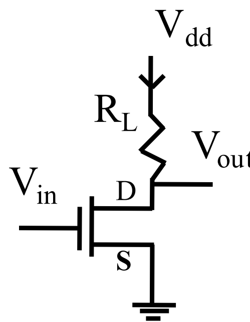

Figure 6.15 CS amplifier circuit topology.

The amplifier performance is studied with respect to variation in bias voltage, which is obtained by varying R_L. The results in Figure 6.17 corresponds to performance of amplifier when the bias voltage is fixed such that peak is observed in gain curves at $V_{in} = V_{out}$ = 0.4 V, 0.3 V, 0.25 V. This is done to understand the gain-load relationship. It is observed that by increasing the bias from 0.25 V to 0.4 V, the gain peak drops from 8 to 2 with a considerable increase in swing. This highlights the tradeoff between gain and swing while designing an amplifier. In amplifier design using planar MOSFET, width of the transistor is tuned to obtain

required gain and swing, while in VNW the equivalent width variation can be obtained by either increasing NW diameter, using multiple NW in parallel or by varying extension, overlap/underlap length.

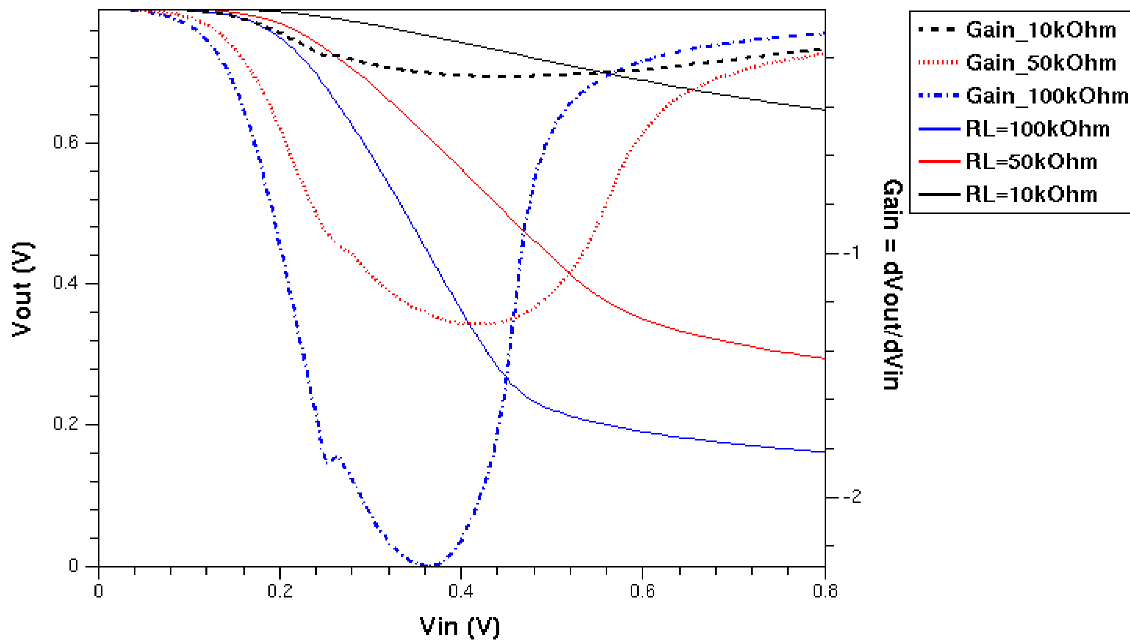

Figure 6.16 CS amplifier V_{out}, gain versus V_{in} for various R_L. VNW device L_G=15nm, S/D_{ext} = 20nm.

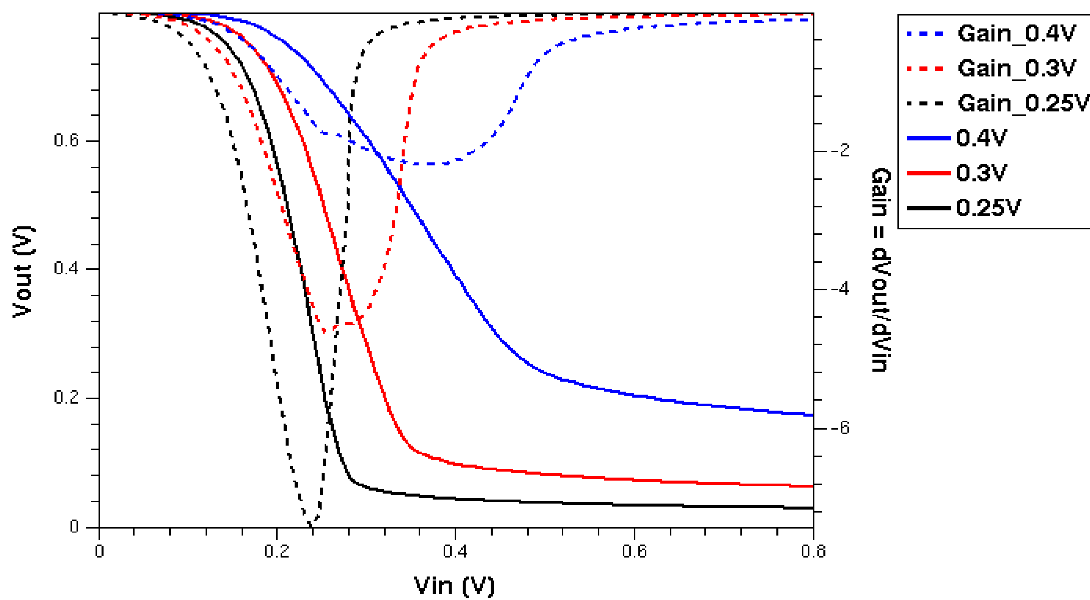

Figure 6.17 Impact of bias voltage on CS amplifier performance. VNW device L_G=15nm, S/D_{ext} = 20nm.

To understand driver-gain behavior the number of nanowires in VNW are increased from 1 to 16 as shown in Figure 6.18. In Figure 6.18 similar behavior is observed, when the nanowires in

VNW device are increased, it leads to increase in the g_m (transconductance), resulting in increase in gain value at the cost of decrease in swing.

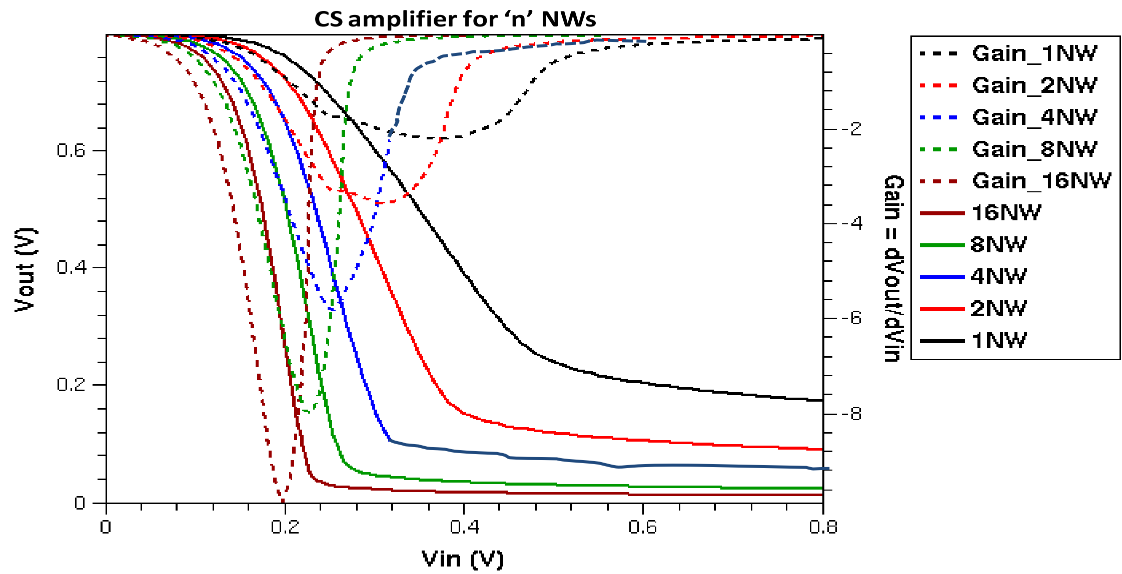

Figure 6.18 Impact of multiple nanowires in VNW on CS amplifier performance. VNW device L_G=15nm, S/D_{ext} = 20nm.

The impact of number of nanowires and the change in S/D_{ext} on intrinsic gain (absolute) of device and gain of amplifier is shown in Table 6.2. In this study, the value of R_L is chosen such that the gain peak is observed at 0.4V for intrinsic and single VNW device. For 2 NW and 4 NW the gain peak is observed at 0.3 V and 0.25 V respectively. For the intrinsic case the gain is higher for longer S/D_{ext}, i.e., lower g_{DS} or large output conductance. But for a resistive loaded CS amplifier, gain is higher for smaller S/D_{ext}. This is due to relatively higher increase in g_m when compared to degradation in output conductance.

Table 6.2 Performance of VNW device with increase in number of nanowires and change in S/D_{ext}.

Gain				
S/D_{ext}	Intrinsic (0.4V)	1nw (0.4V)	2nw (0.3V)	4nw (0.25V)
30nm	260	1.93	3.31	5.52
20nm	240	2.14	3.55	5.89
10nm	120	2.17	3.70	6.00

An amplifier performance is incomplete without its frequency response analysis. Figure 6.19 shows that the intrinsic gain is 47 dB for the given bias, which is 40% high when compared to gain value 34.12 dB obtained in FinFET devices (Figure 6.20). From these results the 3dB bandwidth is extracted to be 160 GHz and 157 GHz respectively for VNW and FinFET. Further

it is observed that the f_T (Gain=0 dB) of VNW device is 814 GHz (~ 66% higher) where as it is 490 GHz for FinFET device. Due to higher gain, nearly equal 3dB bandwidth and higher f_T shown by VNW device, we can conclude the suitability of VNWFET for high performance analog applications.

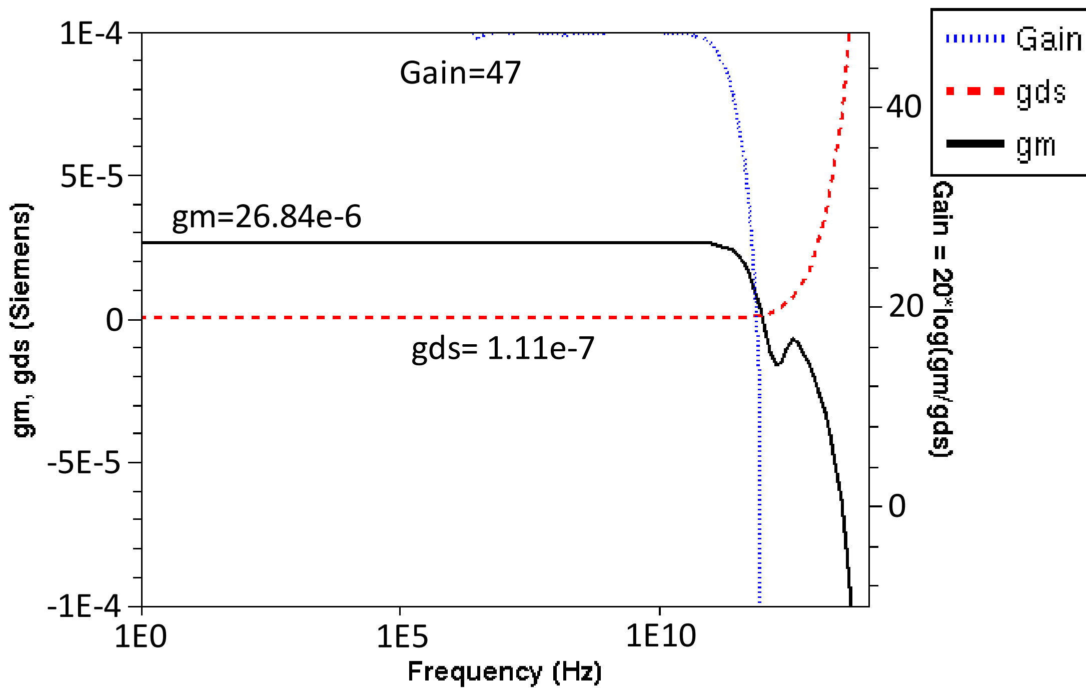

Figure 6.19 Frequency response of intrinsic VNW device (L_G=15nm, S/D_{ext}=20nm, Dia=10nm) biased at V_D= 0.8V and V_G = 0.4V.

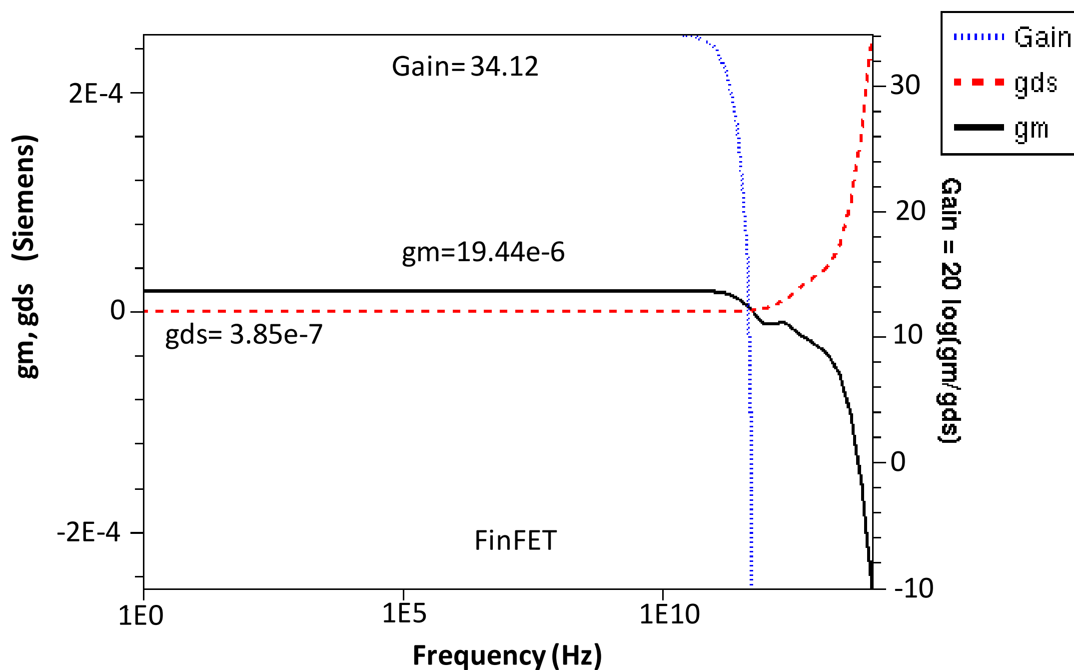

Figure 6.20 Frequency response of intrinsic FinFET device (L_G=16nm, S/D_{ext}=20nm, W_{fin}=10nm, H_{fin}=30nm) biased at V_D= 0.8V and V_G = 0.4V.

Finally, the impact of variability in gate position and resulting asymmetric S/D_{ext} length as a tuning parameter in design CS amplifier is carried out. The resulting devices with different gate positions are shown in Figure 6.21.

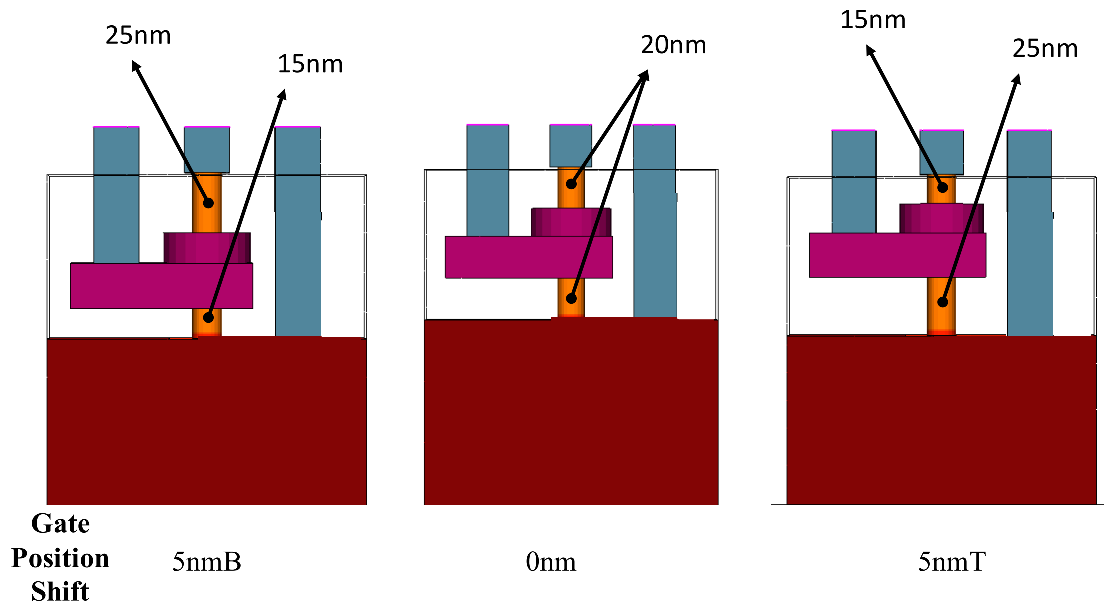

Figure 6.21 VNW devices with process variation impact on gate position. The device labeled 5nmB corresponds to device where gate position shifted towards bottom side by 5nm. 5nmT corresponds to device where gate position shifted towards top side by 5nm.

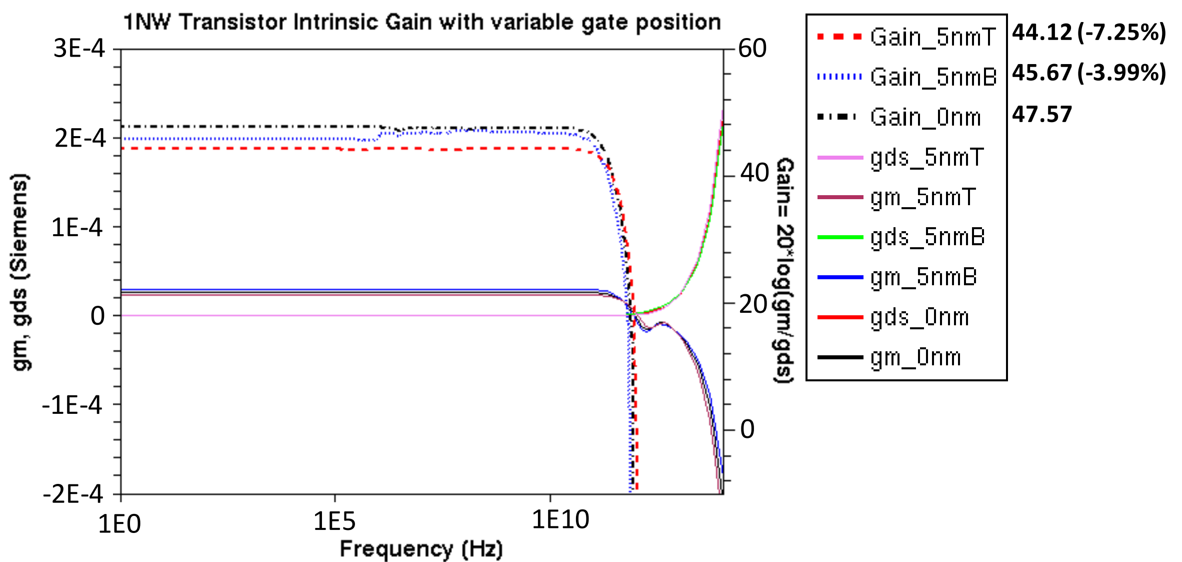

Figure 6.22 Intrinsic gain of VNW device with variation in gate position.

For a ±25% change in gate position, the maximum change in intrinsic gain (20 log (g_m/g_{ds})) is -7.25% as in Figure 6.22. This can be explained as follows, in 5nmT device the extension length towards the source side is longer, contributing to larger series source resistance. It results in large drop across source resistance, hence decrease in effective gate voltage across the channel. Due to this, there is decrease in g_m of the device and hence the gain.

In the case of a resistive loaded CS amplifier, for 5nmB there is increase in gain and for 5nmT there is decrease in gain as seen in Figure 6.23. In 5nmB device there is increase in drain extension length or drain resistance, hence there is increase in output conductance and gain. In 5nmT device there is increase in source extension length or source resistance, hence there is decrease in effective gate voltage across channel or g_m and gain. It is observed that 3dB bandwidth is 316 GHz, 270 GHz, 402 GHz and f_T is 450 GHz, 420 GHz, 560 GHz for 0nm, 5nmB, 5nmT CS amplifiers respectively. Thus with 5nmT device with a marginal decrement in gain (4.1%), we can increase the 3dB bandwidth and f_T by nearly 25%. Thus, extension length tuning can be used to design amplifier with required gain, bandwidth and f_T.

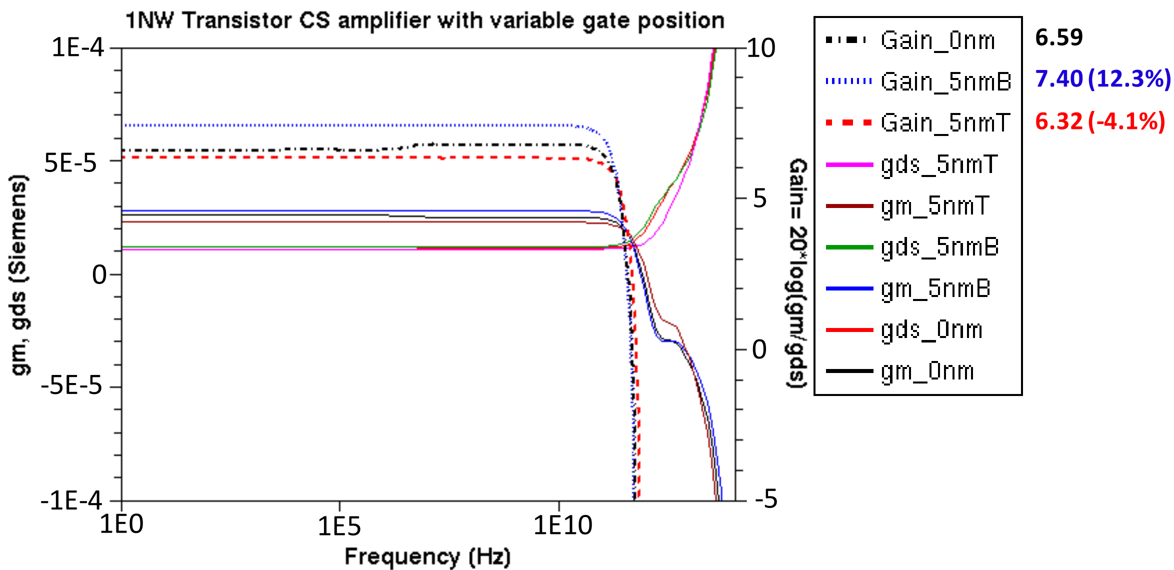

Figure 6.23 CS amplifier gain of VNW with variation in gate position.

6.3 Summary

Benchmarking of VNW CMOS inverter performance with respect to planar and FINFET inverters shows better performance of VNW based circuits and justifies its usage in low power applications. The delay performance analysis of VNW inverter highlights ~65% better delay of

performance by devices with drain at top as compared to devices with drain at bottom. It is shown that the parasitic capacitance models developed in chapter 5 can be used to estimate the FO1 load of CMOS inverter and thus can be used to estimate delay of inverter using the effective current method. Further, we have shown that for analog applications, VNW device is much better than FinFET device in terms of gain, 3dB bandwidth and f_T of intrinsic device. Finally, analysis of the impact of bias voltage, number of nanowires, S/D_{ext} length and variability in gate position on CS amplifier using VNW device is presented. Further, it is observed that changing the position of gate results in change in gain, 3dB bandwidth and f_T. Thus, it can be used as a tuning parameter to design amplifier with required gain, bandwidth and f_T.

7 CHAPTER

CONCLUSION & FUTURE SCOPE

In this chapter, we consolidate the major conclusions of the work carried out on Vertical Nanowire FET as part of this thesis. Further, we present pointers for future work that can be undertaken in investigating VNWFET as the future device for technology nodes smaller than 15 nm.

7.1 Conclusion

Vertical Nanowire MOSFETs are proven to be scalable to shortest possible dimensions due to its gate-all-around architecture and it has added advantage of occupying lowest silicon area and low power applications. In this thesis the VNWFET device and its analog/digital circuit performance are comprehensibly studied and the major results are concluded in this section.

We start with implementation of VNWFETs using TCAD simulation setup which is well calibrated with reported experimental device characteristics. The setup consists of major physical effects observed in short channel devices like: quantization effects, high field effect and scattering effects on carrier mobility, contact resistance, gate tunneling, Joule heating effect and ballistic transport of carriers. We found that for 15 nm channel length NW devices, the ballistic transport observed through device monte-carlo simulations (considering 0.85 as the ratio between specular and diffusive scattering at SiO_2 interface) can be replicated in device drift-diffusion simulations by changing the carrier saturation velocities of electron and hole as 1.8×10^7 cm/sec and 1.5×10^7 cm/sec respectively. These values are part of calibration setup used in device and device-circuit studies done in this thesis.

First, device scaling study of VNWFET is presented with respect to channel length (L_G), source/drain extension length (S/D_{ext}), gate-overlap or underlap length (L_{OV}), gate dielectric thickness (T_{OX}), and nanowire diameter (D_{NW}) scaling. It is shown that VNWFET devices can be easily scaled to 15 nm or below L_G with a thick dielectric when compared to planar MOSFET and has $I_{ON}/I_{OFF} > 1\times10^4$, subthreshold slope-SS < 80 mV/dec and drain induced barrier lowering – DIBL < 50 mV/V, thus proves its immunity to short channel effects (SCE's).

For a device with L_G=15 nm, it is shown that device drive current can be improved at a rate of 0.27μA/nm reduction in S/D_{ext} length, and the device continue to be immune to SCE's for S/D_{ext} = 10nm (< L_G). Further, the impact of S/D asymmetry on device performance is investigated, it is demonstrated that S_B (source as bottom electrode) device configuration has better performance when compared to S_T (source as top electrode) device configuration. Next, the impact of L_{OV} on device performance is studied. It is shown that overlap devices have higher I_{ON}, when compared to underlap devices (due to higher resistance in underlap region) and overlap devices have higher I_{OFF} current but still it is around the acceptable value of 1nA. Thus length and choice of overlap/underlap can be tuned to obtain certain I_{ON}/I_{OFF} performance. Further, the impact of T_{OX} scaling on device performance is carried, and it is seen that I_{ON} increases and I_{OFF} decreases. In further studies we choose T_{OX}=2 nm as the gate dielectric thickness in order to have minimal tunneling and gate leakage current. Finally, the impact of nanowire diameter on device performance is studied, it is seen that with larger diameter the I_{ON} current increases linearly with penalty of increased SCE's. It is concluded that diameter can be used as a tuning parameter to match NMOS and PMOS device drive currents. The device characteristics are modeled using the nth power law and found to match well with simulation results. The model parameters are useful in prediction of circuit performance. From the results of device studies we choose following device for rest of thesis study: L_G = 15 nm, S/D_{ext}=30 nm -10 nm. The other optimum device dimensions, which are obtained from the scaling study, are: L_{OV}=2 nm, T_{OX}=2 nm and D_{NW} (NMOS/PMOS) = 10/15 nm.

Nanowire devices are expected to suffer from parasitic resistances and capacitances due to small device dimensions. So, accurate models for these parasitic resistances and capacitances components are formulated for a VNWFET device (considering the cylindrical gate, gate vias and device asymmetry), which match well with simulation results. These modeled parasitics play an important role in determining the device/circuit performance, without actually doing the time consuming TCAD simulations. It is seen that total parasitic capacitance is nearly 1.5 – 2 times the gate capacitance, and the capacitance components totaling to gate-bottom capacitance C_{GB} are the major contributors of parasitic capacitance. Thus, if the bottom electrode acts as drain in digital circuits, then C_{GB} will account for miller capacitance, resulting in higher delays. In the parasitic resistance modeling, the device structure is taken into account along with influence of voltage applied to gate terminal. It is seen that metal semiconductor contacts and extension regions contribute to 90% of the total series resistance. Further, it is noted that top series resistance (R_T) is greater than bottom series resistance (R_B), thus proving the I_{ON} trends of S_B/S_T device i.e., S_B devices have higher drive current (due to lower source

(R_B) resistance or higher gate over drive). These parasitic models can be incorporated into device I-V models and compact SPICE model for VNWFET can be developed. Finally, using these models we analyse and estimate circuit performance of VNWFET.

In the final chapter detailed analysis of circuits employing VNWFET devices is done. First, digital performance of CMOS inverter is analysed through voltage transfer characteristics (VTC). It is found that the VTC has a sharper transition region as opposed to planar MOSFET, this is due to the full saturation characteristics of VNW device or low channel length modulation/minimum SCE. The observed gradual transition in VTC characteristics around the noise margin extraction points is attributed to the range over which one of the device (NMOS or PMOS) stays in linear region thus delaying onset of VTC transition. Finally, we show how S/D_{ext} can be used as tuning parameter to design an inverter with required gain and noise margins. This is followed by, detailed analysis of VNWFET CMOS inverter dynamic characteristics and its comparison with planar and FinFET based inverters. It is seen that VNWFET devices have 65%(50%) lower delay, occupies 50%(45%) lower silicon area when compared to planar(FinFET) technologies. It is also shown that with change in inverter layout the inter device parasitic changes consequently leading to different delay values and L1 layout (Figure 6.8) has the least delay or best performance. Further, it is shown that S_T devices have 65% higher delay owing to lower drive current (or large R_T acting as source resistance) and higher miller capacitance (or higher C_{GB} acting as the C_{GD} or miller component). The impact of S/D_{ext} scaling on inverters (S_B/S_T) delay and power is shown, which highlights the importance of S/D_{ext} as a design parameter in achieving required digital performance. Finally, the digital performance is concluded by delay prediction of inverter using the proposed parasitic models. The delay model predicts well the delay performance, and is found to match well with simulation results. Also, with the delay modeling the behavior for delay performance of S_B/S_T circuits with S/D_{ext} scaling is explained.

To complete the study, VNWFET analog performance is investigated for intrinsic device and single stage common source (CS) amplifier. The gain-load and driver-gain relationships are investigated for a VNWFET based CS amplifier. It is seen that very high values of load (> 38 kOhm) is required to obtain gain greater that 1 and multiple nanowires in VNWFET can be used to increase the gain at cost of output swing. Through frequency response of intrinsic VNWFET and FinFET it is seen that VNWFET has higher gain, f_T and slightly higher value of 3dB bandwidth. This demonstrates the better performance of VNWFET not only in digital circuits, but also in analog circuits. Finally, the variation in gate position or asymmetric S/D

lengths is investigated as a tuning parameter in designing CS amplifier. It is seen that when source extension length is reduced, the series resistance decreases thus increasing the device transconductance with a marginal change in output conductance, thus resulting in higher gain and slightly lower 3dB bandwidth and f_T.

Hence, with the device scaling study, parasitic modeling, detailed digital and analog circuit performance we conclude that VNWFET is an attractive device for future technology nodes ($\leq$ 15 nm), overcoming limitations of planar/FinFET transistors.

7.2 Future Scope

In this section, we present future work that can be carried out based on this thesis.

1. VNWFET based memory cells is of prime importance due to the fact that it can provide the highest circuit density for a given silicon area. Thus, detailed analysis of VNWFET based 6T SRAM cell need to be carried out. In the SRAM design S/D asymmetry can be used to our advantage by using S_T devices as the low drive access transistors. Further, the diameter of PMOS can be kept equal to NMOS so that the pull-up strength is less than pull-down strength. With this approach there will be no need of width tuning or different dimension device to realize an SRAM cell.

2. The parasitic capacitance and resistance models proposed for VNWFET can be used along with existing nanowire I-V and C-V models to develop a unified compact model of VNWFET, which can then be used in SPICE simulators. With this model, the standard cell library of VNWFET can be created consisting of inverter, ring oscillator, buffer, NAND, NOR, XOR, XNOR, mux and decoder etc.

3. VNWFET devices and circuits can be fabricated following the guidelines presented in this thesis. The characterization of devices/circuits thus obtained can be compared with the simulation results and further analysis can be carried out.

4. Further detailed analysis of VNWFET can be carried out with various analog circuits such as current mirrors, differential amplifiers and other analog circuit blocks.

5. Reliability study of VNWFET can be carried out with respect to radiation effects, hot carrier induced effects, negative/positive bias temperature instability and time to dielectric breakdown, which are of high importance.

6. Further, studies of VNW based devices in applications such as solar cells, NW sensors can be undertaken.

BIBLIOGRAPHY

[1] G. E. Moore, “Cramming More Components Onto Integrated Circuits,” *Proc. IEEE*, vol. 86, no. 1, pp. 82–85, 1998.

[2] H. S. P. Wong, “Beyond the conventional transistor,” *IBM J. Res. Dev.*, vol. 46, no. 2.3, pp. 133–168, 2002.

[3] C. H. Wann, K. Noda, T. Tanaka, M. Yoshida, and H. Chenming, “A comparative study of advanced MOSFET concepts,” *Electron Devices, IEEE Trans.*, vol. 43, no. 10, pp. 1742–1753, 1996.

[4] S. Thompson, P. Packan, and M. Bohr, “MOS Scaling Transistor Challenges for the 21st Century,” *Intel Technol. J.*, vol. Q3, pp. 1–19, 1998.

[5] T. Skotnicki, J. A. Hutchby, K. Tsu-Jae, H. S. P. Wong, and F. Boeuf, “The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance,” *Circuits Devices Mag. IEEE*, vol. 21, no. 1, pp. 16–26, 2005.

[6] P. M. Zeitzoff and J. E. Chung, “A perspective from the 2003 ITRS: MOSFET scaling trends, challenges, and potential solutions,” *Circuits Devices Mag. IEEE*, vol. 21, no. 1, pp. 4–15, 2005.

[7] S. Gundapaneni, S. Ganguly, and A. Kottantharayil, “Enhanced Electrostatic Integrity of Short-Channel Junctionless Transistor With High- κ Spacers,” *Electron Device Lett. IEEE*, vol. 32, no. 10, pp. 1325–1327, 2011.

[8] S. Gundapaneni, M. Bajaj, R. K. Pandey, K. V. R. M. Murali, S. Ganguly, and A. Kottantharayil, “Effect of Band-to-Band Tunneling on Junctionless Transistors,” *Electron Devices, IEEE Trans.*, vol. 59, no. 4, pp. 1023–1029, 2012.

[9] S. Gundapaneni, S. Ganguly, and A. Kottantharayil, “Bulk Planar Junctionless Transistor (BPJLT): An Attractive Device Alternative for Scaling,” *Electron Device Lett. IEEE*, vol. 32, no. 3, pp. 261–263, 2011.

[10] "ITRS." [Online]. Available: http://www.itrs.net/Links/2008ITRS/Home2008.htm.

[11] P. Rakesh Kumar and S. Mahapatra, "Analytical modeling of quantum threshold voltage for triple gate MOSFET," *Solid. State. Electron.*, vol. 54, no. 12, pp. 1586–1591, 2010.

[12] N. Sharan and S. Mahapatra, "Nonquasi-Static Charge Model for Common Double-Gate MOSFETs Adapted to Gate Oxide Thickness Asymmetry," *Electron Devices, IEEE Trans.*, vol. 60, no. 7, pp. 2419–2422, 2013.

[13] N. Sharan and S. Mahapatra, "Continuity equation based nonquasi-static charge model for independent double gate MOSFET," *J. Comput. Electron.*, pp. 1–7, 2013.

[14] M. Shrivastava, B. Verma, M. S. Baghini, C. Russ, D. K. Sharma, H. Gossner, and V. Ramgopal Rao, "Benchmarking the device performance at sub 22 nm node technologies using an SoC framework," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1–4.

[15] M. Shrivastava, H. Gossner, and V. R. Rao, "A Novel Drain-Extended FinFET Device for High-Voltage High-Speed Applications," *Electron Device Lett. IEEE*, vol. 33, no. 10, pp. 1432–1434, 2012.

[16] M. Shrivastava, R. Mehta, S. Gupta, N. Agrawal, M. S. Baghini, D. K. Sharma, T. Schulz, K. Arnim, W. Molzer, H. Gossner, and V. Ramgopal Rao, "Toward System on Chip (SoC) Development Using FinFET Technology: Challenges, Solutions, Process Co-Development & Optimization Guidelines," *Electron Devices, IEEE Trans.*, vol. 58, no. 6, pp. 1597–1607, 2011.

[17] K. J. Kuhn, U. Avci, A. Cappellani, M. D. Giles, M. Haverty, K. Seiyon, R. Kotlyar, S. Manipatruni, D. Nikonov, C. Pawashe, M. Radosavljevic, R. Rios, S. Shankar, R. Vedula, R. Chau, and I. Young, "The ultimate CMOS device and beyond," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 8.1.1–8.1.4.

[18] D. A. Antoniadis and A. Khakifirooz, "MOSFET performance scaling: Limitations and future options," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, 2008, pp. 1–4.

[19] K. Bernstein, R. K. Cavin, W. Porod, A. Seabaugh, and J. Welser, "Device and Architecture Outlook for Beyond CMOS Switches," *Proc. IEEE*, vol. 98, no. 12, pp. 2169–2184, 2010.

[20] A. Agarwal, N. Singh, T. Liow, R. Kumar, N. Balasubramanian, and D. L. Kwong, "Transport Characteristics of Si Nanowires in Bulk Silicon and SOI Wafers," in *Emerging Technologies - Nanoelectronics, 2006 IEEE Conference on*, 2006, pp. 67–70.

[21] S. Thompson and S. Parthasarathy, "Moore's law: the future of Si microelectronics," *Mater. Today*, vol. 9, no. 6, pp. 20–25, 2006.

[22] S. Balakumar, K. D. Buddharaju, B. Tan, S. C. Rustagi, N. Singh, R. Kumar, G. Q. Lo, S. Tripathy, and D. L. Kwong, "Germanium-Rich SiGe Nanowires Formed Through Oxidation of Patterned SiGe FINs on Insulator," *J. Electron. Mater.*, vol. 38, no. 3, pp. 443–448, 2009.

[23] N. Balasubramanian, N. Singh, S. C. Rustogi, K. D. Buddharaju, J. Fu, Z. Hui, S. Balakumar, A. Agarwal, S. K. Manhas, G. Q. Lo, and and D. L. Kwong, "Si Nanowire CMOS Transistors and Circuits by Top-Down Technology Approach," *ECS Trans.*, vol. 13, no. 1, pp. 201–211, 2008.

[24] Y. Jiang, N. Singh, T. Y. Liow, W.-Y. Loh, S. Balakumar, K. M. Hoe, C. H. Tung, V. Bliznetsov, S. C. Rustagi, G.-Q. Lo, D. S. H. Chan, and D.-L. Kwong, "Ge-Rich (70%) SiGe Nanowire MOSFET Fabricated Using Pattern-Dependent Ge-Condensation Technique," *Electron Device Letters, IEEE*, vol. 29, no. 6. pp. 595–598, 2008.

[25] N. Singh, K. D. Buddharaju, S. K. Manhas, A. Agarwal, S. C. Rustagi, G. Q. Lo, N. Balasubramanian, and K. Dim-Lee, "Si, SiGe Nanowire Devices by Top─Down Technology and Their Applications," *Electron Devices, IEEE Trans.*, vol. 55, no. 11, pp. 3107–3118, 2008.

[26] D.-L. Kwong, X. Li, Y. Sun, G. Ramanathan, Z. X. Chen, S. M. Wong, Y. Li, N. S. Shen, K. Buddharaju, Y. H. Yu, S. J. Lee, N. Singh, and G. Q. Lo, "Vertical Silicon Nanowire Platform for Low Power Electronics and Clean Energy Applications," *J. Nanotechnol.*, vol. 2012, 2012.

[27] C. H. Jan, U. Bhattacharya, R. Brain, S. J. Choi, G. Curello, G. Gupta, W. Hafez, M. Jang, M. Kang, K. Komeyli, T. Leo, N. Nidhi, L. Pan, J. Park, K. Phoa, A. Rahman, C. Staus, H. Tashiro, C. Tsai, P. Vandervoorn, L. Yang, J. Y. Yeh, and P. Bai, "A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 3.1.1–3.1.4.

[28] C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. Mcfadden, B. Mcintyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry, "A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors , Self-Aligned Contacts and High Density MIM Capacitors," in *VLSIT*, 2012, vol. m, no. 2003, pp. 131–132.

[29] S. Damaraju, V. George, S. Jahagirdar, T. Khondker, R. Milstrey, S. Sarkar, S. Siers, I. Stolero, and A. Subbiadh, "A 22nm IA Multi-CPU and GPU System-on-Chip," in *ISSCC*, 2012, vol. 44, no. 4, pp. 56–57.

[30] S. Ramey, A. Ashutosh, C. Auth, J. Clifford, M. Hattendorf, J. Hicks, R. James, A. Rahman, V. Sharma, A. S. Amour, and C. Wiegand, "Intrinsic Transistor Reliability Improvements from 22nm Tri-Gate Technology," in *IRPS*, 2013, pp. 4C5.1–4C.5.5.

[31] "Intel." [Online]. Available: http://www.intel.com/technology/architecture-silicon/22nm/index.htm.

[32] "TSMC." [Online]. Available: http://www.tsmc.com/tsmcdotcom/PRListingNewsArchivesAction.do?action=detail&newsid=3041&language=E.

[33] Y. Jiang, T. Y. Liow, N. Singh, L. H. Tan, L. Guo-Qiang, D. S. H. Chan, and K. Dim-Lee, "Nickel Salicided Source/Drain Extensions for Performance Improvement in Ultrascaled (Sub 10 nm) Si-Nanowire Transistors," *Electron Device Lett. IEEE*, vol. 30, no. 2, pp. 195–197, 2009.

[34] A. B. Sachid, P. Paliwal, S. Joshi, M. Shojaei, D. Sharma, and V. Rao, "Circuit Optimization at 22nm Technology Node," in *VLSI Design (VLSID), 2012 25th International Conference on*, 2012, pp. 322–327.

[35] A. B. Sachid, R. Francis, M. S. Baghini, D. K. Sharma, K. H. Bach, R. Mahnkopf, and V. Ramgopal Rao, "Sub-20 nm gate length FinFET design: Can high-κ spacers make a difference?," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, 2008, pp. 1–4.

[36] A. B. Sachid and H. Chenming, "Denser and More Stable SRAM Using FinFETs With Multiple Fin Heights," *Electron Devices, IEEE Trans.*, vol. 59, no. 8, pp. 2037–2041, 2012.

[37] M. Shrivastava, M. S. Baghini, A. B. Sachid, D. K. Sharma, and V. R. Rao, "A Novel and Robust Approach for Common Mode Feedback Using IDDG FinFET," *Electron Devices, IEEE Trans.*, vol. 55, no. 11, pp. 3274–3282, 2008.

[38] F. Moradi, S. K. Gupta, G. Panagopoulos, D. T. Wisland, H. Mahmoodi, and K. Roy, "Asymmetrically Doped FinFETs for Low-Power Robust SRAMs," *Electron Devices, IEEE Trans.*, vol. 58, no. 12, pp. 4241–4249, 2011.

[39] S. K. Gupta, P. Sang Phill, and K. Roy, "Tri-Mode Independent-Gate FinFETs for Dynamic Voltage/Frequency Scalable 6T SRAMs," *Electron Devices, IEEE Trans.*, vol. 58, no. 11, pp. 3837–3846, 2011.

[40] A. Goel, S. K. Gupta, and K. Roy, "Asymmetric Drain Spacer Extension (ADSE) FinFETs for Low-Power and Robust SRAMs," *Electron Devices, IEEE Trans.*, vol. 58, no. 2, pp. 296–308, 2011.

[41] B. Swahn and S. Hassoun, "Gate sizing: finFETs vs 32nm bulk MOSFETs," in *Design Automation Conference, 2006 43rd ACM/IEEE*, 2006, pp. 528–531.

[42] T. Poiroux, M. Vinet, O. Faynot, J. Widiez, J. Lolivier, B. Previtali, T. Ernst, and S. Deleonibus, "Multigate silicon MOSFETs for 45nm node and beyond," *Solid. State. Electron.*, vol. 50, no. 1, pp. 18–23, 2006.

[43] M. V Dunga, L. Chung-Hsun, D. D. Lu, X. Weize, C. R. Cleavelin, P. Patruno, H. Jiunn-Ren, Y. Fu-Liang, A. M. Niknejad, and H. Chenming, "BSIM-MG: A Versatile Multi-Gate FET Model for Mixed-Signal Design," in *VLSI Technology, 2007 IEEE Symposium on*, 2007, pp. 60–61.

[44] J. P. Colinge, "Multi-gate SOI MOSFETs," *Microelectron. Eng.*, vol. 84, no. 9–10, pp. 2071–2076, 2007.

[45] C. R. Manoj, N. Meenakshi, V. Dhanya, and V. Ramgopal Rao, "Device optimization of bulk FinFETs and its comparison with SOI FinFETs," in *Physics of Semiconductor Devices, 2007. IWPSD 2007. International Workshop on*, 2007, pp. 134–137.

[46] Y. Bin, L. Chang, S. Ahmed, W. Haihong, S. Bell, Y. Chih-Yuh, C. Tabery, H. Chau, X. Qi, K. Tsu-Jae, J. Bokor, H. Chenming, L. Ming-Ren, and D. Kyser, "FinFET scaling to 10 nm gate length," in *Electron Devices Meeting, 2002. IEDM '02. International*, 2002, pp. 251–254.

[47] E. Gnani, S. Reggiani, M. Rudan, and G. Baccarani, "Design Considerations and Comparative Investigation of Ultra-Thin SOI, Double-Gate and Cylindrical Nanowire FETs," in *Solid-State Device Research Conference, 2006. ESSDERC 2006. Proceeding of the 36th European*, 2006, pp. 371–374.

[48] N. N. Mojumder and K. Roy, "Band-to-Band Tunneling Ballistic Nanowire FET: Circuit-Compatible Device Modeling and Design of Ultra-Low-Power Digital Circuits and Memories," *Electron Devices, IEEE Trans.*, vol. 56, no. 10, pp. 2193–2201, 2009.

[49] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "High-performance fully depleted silicon nanowire (diameter ≤ 5 nm) gate-all-around CMOS devices," *Electron Device Lett. IEEE*, vol. 27, no. 5, pp. 383–386, 2006.

[50] N. Singh, F. Y. Lim, W. W. Fang, S. C. Rustagi, L. K. Bera, A. Agarwal, C. H. Tung, K. M. Hoe, S. R. Omampuliyur, D. Tripathi, A. O. Adeyeye, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "Ultra-Narrow Silicon Nanowire Gate-All-Around CMOS Devices: Impact of Diameter, Channel-Orientation and Low Temperature on

Device Performance," in *Electron Devices Meeting, 2006. IEDM '06. International*, 2006, pp. 1–4.

[51] N. Singh, W. W. Fang, S. C. Rustagi, K. D. Budharaju, S. H. G. Teo, S. Mohanraj, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "Observation of Metal-Layer Stress on Si Nanowires in Gate-All-Around High- κ/Metal-Gate Device Structures," *Electron Device Lett. IEEE*, vol. 28, no. 7, pp. 558–561, 2007.

[52] K. D. Buddharaju, N. Singh, S. C. Rustagi, S. H. G. Teo, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "Si-nanowire CMOS inverter logic fabricated using gate-all-around (GAA) devices and top-down approach," *Solid. State. Electron.*, vol. 52, no. 9, pp. 1312–1317, 2008.

[53] S. C. Rustagi, N. Singh, W. W. Fang, K. D. Buddharaju, S. R. Omampuliyur, S. H. G. Teo, C. H. Tung, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "CMOS Inverter Based on Gate-All-Around Silicon-Nanowire MOSFETs Fabricated Using Top-Down Approach," *Electron Device Lett. IEEE*, vol. 28, no. 11, pp. 1021–1024, 2007.

[54] J. Fu, N. Singh, K. D. Buddharaju, S. H. G. Teo, C. Shen, Y. Jiang, C. X. Zhu, M. B. Yu, G. Q. Lo, N. Balasubramanian, D. L. Kwong, E. Gnani, and G. Baccarani, "Si-Nanowire Based Gate-All-Around Nonvolatile SONOS Memory Cell," *Electron Device Lett. IEEE*, vol. 29, no. 5, pp. 518–521, 2008.

[55] G. Kaushal, S. K. Manhas, S. Maheshwaram, S. Dasgupta, B. Anand, and N. Singh, "Tuning Source/Drain Extension Profile for Current Matching in Nanowire CMOS Logic," *Nanotechnology, IEEE Trans.*, vol. 11, no. 5, pp. 1033–1039, 2012.

[56] B. Yang, K. D. Buddharaju, S. H. G. Teo, N. Singh, G. Q. Lo, and D. L. Kwong, "Vertical Silicon-Nanowire Formation and Gate-All-Around MOSFET," *Electron Device Lett. IEEE*, vol. 29, no. 7, pp. 791–794, 2008.

[57] S. Maheshwaram, S. K. Manhas, G. Kaushal, B. Anand, and N. Singh, "Vertical Silicon Nanowire Gate-All-Around Field Effect Transistor Based Nanoscale CMOS," *Electron Device Lett. IEEE*, vol. 32, no. 8, pp. 1011–1013, 2011.

[58] P. E. Gaillardon, H. Ben-Jamaa, P. Morel, J. Noel, F. Clermidy, and I. O'Connor, "Can we go towards true 3-D architectures?," in *Design Automation Conference (DAC), 2011 48th ACM/EDAC/IEEE*, 2011, pp. 282–283.

[59] G. Shen, P.-C. Chen, K. Ryu, and C. Zhou, "Devices and chemical sensing applications of metal oxide nanowires," *J. Mater. Chem.*, vol. 19, no. 7, pp. 828–839, 2009.

[60] A. Agarwal, K. Buddharaju, I. K. Lao, N. Singh, N. Balasubramanian, and D. L. Kwong, "Silicon nanowire sensor array using top–down CMOS technology," *Sensors Actuators A Phys.*, vol. 145–146, no. 0, pp. 207–213, 2008.

[61] Z. Gao, A. Agarwal, A. D. Trigg, N. Singh, C. Fang, C.-H. Tung, Y. Fan, K. D. Buddharaju, and J. Kong, "Silicon Nanowire Arrays for Label-Free Detection of DNA," *Anal. Chem.*, vol. 79, no. 9, pp. 3291–3297, 2007.

[62] A. Agarwal, I. K. Lao, K. Buddharaju, N. Singh, N. Balasubramanian, and D. L. Kwong, "Silicon Nanowire Array Bio-Sensor using Top-Down CMOS Technology," in *Solid-State Sensors, Actuators and Microsystems Conference, 2007. TRANSDUCERS 2007. International*, 2007, pp. 1051–1054.

[63] F. Patolsky, G. Zheng, and C. Lieber, "Nanowire-based biosensors," *Anal. Chem.*, pp. 4261–4269, 2006.

[64] C. Lu, S. Chang, and S. Chang, "ZnO nanowire-based oxygen gas sensor," *Sensors Journal, IEEE*, vol. 9, no. 4, pp. 485–489, 2009.

[65] E. Garnett and P. Yang, "Light trapping in silicon nanowire solar cells.," *Nano Lett.*, vol. 10, no. 3, pp. 1082–1087, Mar. 2010.

[66] *Sentaurus TCAD (ver. 2009.06) Manuals, Synopsys Inc., Mountain View, CA.* .

[67] T. Sakurai and A. R. Newton, "A simple MOSFET model for circuit analysis," *Electron Devices, IEEE Trans.*, vol. 38, no. 4, pp. 887–894, 1991.

[68] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits*, 3rd Ed.,. Pearson Prentice Hall, 2009.

[69] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits*, 3rd Ed.,. Tata McGraw-Hill, 2003.

[70] B. Razavi, *Design of Analog CMOS Integrated Circuits*. Tata McGraw-Hill, 2002.

[71] C. P. Auth and J. D. Plummer, "Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's," *Electron Device Lett. IEEE*, vol. 18, no. 2, pp. 74–76, 1997.

[72] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, "Scaling theory for double-gate SOI MOSFET's," *Electron Devices, IEEE Trans.*, vol. 40, no. 12, pp. 2326–2329, 1993.

[73] Y. Ran-Hong, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: from bulk to SOI to bulk," *Electron Devices, IEEE Trans.*, vol. 39, no. 7, pp. 1704–1710, 1992.

[74] N. Singh, K. D. Buddharaju, A. Agarwal, S. C. Rustagi, C. . Lo, N. Balasubramanian, and D. L. Kwong, "Fully gate-all-around silicon nanowire CMOS devices," *Solid State Technol.*, vol. 51, no. 5, p. 34, 2008.

[75] Y. Kyoung Hwan, S. Sung-Dae, L. Ming, Y. Yun-young, C. Keun Hwi, H. Ki-Ha, Y. SeongKyu, L. Mong Sup, C. Nammyun, L. Kwanheum, H. Duhyun, P. Bokkyoung, K. Dong-Won, P. Donggun, and R. Byung-il, "Gate-All-Around (GAA) Twin Silicon Nanowire MOSFET (TSNWFET) with 15 nm Length Gate and 4 nm Radius Nanowires," in *Electron Devices Meeting, 2006. IEDM '06. International*, 2006, pp. 1–4.

[76] H. Takato, K. Sunouchi, N. Okabe, A. Nitayama, K. Hieda, F. Horiguchi, and F. Masuoka, "Impact of surrounding gate transistor (SGT) for ultra-high-density LSI's," *Electron Devices, IEEE Trans.*, vol. 38, no. 3, pp. 573–578, 1991.

[77] S. K. Jayanarayanan, S. Dey, J. P. Donnelly, and S. K. Banerjee, "A novel 50nm vertical MOSFET with a dielectric pocket," *Solid. State. Electron.*, vol. 50, no. 5, pp. 897–900, 2006.

[78] B. Yang, K. D. Buddharaju, S. H. G. Teo, J. Fu, N. Singh, G. Q. Lo, and D. L. Kwong, "CMOS compatible Gate-All-Around Vertical silicon-nanowire MOSFETs," in *Solid-*

State Device Research Conference, 2008. ESSDERC 2008. 38th European, 2008, pp. 318–321.

[79] T. Chiarella, L. Witters, A. Mercha, C. Kerner, R. Dittrich, M. Rakowski, C. Ortolland, L. A. Ragnarsson, B. Parvais, A. De Keersgieter, S. Kubicek, A. Redolfi, R. Rooyackers, C. Vrancken, S. Brus, A. Lauwers, P. Absil, S. Biesemans, and T. Hoffmann, "Migrating from planar to FinFET for further CMOS scaling: SOI or Bulk?," in *Solid State Device Research Conference, 2009. ESSDERC '09. Proceedings of the European*, 2009, pp. 85–88.

[80] A. Datta, A. Goel, R. T. Cakici, H. Mahmoodi, D. Lekshmanan, and K. Roy, "Modeling and Circuit Synthesis for Independently Controlled Double Gate FinFET Devices," *Comput. Des. Integr. Circuits Syst. IEEE Trans.*, vol. 26, no. 11, pp. 1957–1966, 2007.

[81] T. Hoffmann, A. Veloso, A. Lauwers, H. Yu, H. Tigelaar, M. Van Dal, T. Chiarella, C. Kerner, T. Kauerauf, A. Shickova, R. Mitsuhashi, I. Satoru, M. Niwa, A. Rothschild, B. Froment, J. Ramos, A. Nackaerts, M. Rosmeulen, S. Brus, C. Vrancken, P. P. Absil, M. Jurczak, S. Biesemans, and J. A. Kittl, "Ni-based FUSI gates: CMOS Integration for 45nm node and beyond," in *Electron Devices Meeting, 2006. IEDM '06. International*, 2006, pp. 1–4.

[82] A. Pouydebasque, B. Dumont, S. Denorme, F. Wacquant, M. Bidaud, C. Laviron, A. Halimaoui, C. Chaton, J. D. Chapon, P. Gouraud, F. Leverd, H. Bernard, S. Warrick, D. Delille, K. Romanjek, R. Gwoziecki, N. Planes, S. Vadot, I. Pouilloux, F. Arnaud, F. Boeuf, and T. Skotnicki, "High density and high speed SRAM bit-cells and ring oscillators due to laser annealing for 45nm bulk CMOS," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, pp. 663–666.

[83] T. T. Le, H. Y. Yu, Y. Sun, N. Singh, X. Zhou, N. Shen, G. Q. Lo, and D. L. Kwong, "High-Performance Poly-Si Vertical Nanowire Thin-Film Transistor and the Inverter Demonstration," *Electron Device Lett. IEEE*, vol. 32, no. 6, pp. 770–772, 2011.

[84] D. Jimenez, B. Iniguez, J. Roig, J. Sune, L. F. Marsal, J. Pallares, and D. Flores, "Physics-based model of the surrounding-gate MOSFET," in *Electron Devices, 2005 Spanish Conference on*, 2005, pp. 393–396.

[85] B. Iniguez, D. Jimenez, J. Roig, H. A. Hamid, L. F. Marsal, and J. Pallares, "Explicit continuous model for long-channel undoped surrounding gate MOSFETs," *Electron Devices, IEEE Trans.*, vol. 52, no. 8, pp. 1868–1873, 2005.

[86] B. Iniguez, A. Lazaro, H. A. El Hamid, O. Moldovan, B. Nae, J. Roig, and D. Jimenez, "Charge-Based Compact Modeling of Multiple-Gate MOSFET," in *Custom Integrated Circuits Conference, 2007. CICC '07. IEEE*, 2007, pp. 49–56.

[87] D. Jimenez, B. Iniguez, J. Sune, L. F. Marsal, J. Pallares, J. Roig, and D. Flores, "Continuous analytic I-V model for surrounding-gate MOSFETs," *Electron Device Lett. IEEE*, vol. 25, no. 8, pp. 571–573, 2004.

[88] O. Moldovan, B. Iniguez, D. Jimenez, and J. Roig, "Analytical Charge and Capacitance Models of Undoped Cylindrical Surrounding-Gate MOSFETs," *Electron Devices, IEEE Trans.*, vol. 54, no. 1, pp. 162–165, 2007.

[89] O. Moldovan, D. Jimenez, J. R. Guitart, F. A. Chaves, and B. Iniguez, "Explicit Analytical Charge and Capacitance Models of Undoped Double-Gate MOSFETs," *Electron Devices, IEEE Trans.*, vol. 54, no. 7, pp. 1718–1724, 2007.

[90] Y. Bo, L. Wei-Yuan, L. Huaxin, and T. Yuan, "Analytic Charge Model for Surrounding-Gate MOSFETs," *Electron Devices, IEEE Trans.*, vol. 54, no. 3, pp. 492–496, 2007.

[91] L. Feng, H. Jin, Z. Lining, Z. Jian, H. Jinghua, M. Chenyue, and M. Chan, "A Charge-Based Model for Long-Channel Cylindrical Surrounding-Gate MOSFETs From Intrinsic Channel to Heavily Doped Body," *Electron Devices, IEEE Trans.*, vol. 55, no. 8, pp. 2187–2194, 2008.

[92] Y. Yun Seop, C. NamKi, H. Sung-Woo, and D. Ahn, "Implicit Continuous Current─Voltage Model for Surrounding-Gate Metal─Oxide─ emiconductor Field-Effect Transistors Including Interface Traps," *Electron Devices, IEEE Trans.*, vol. 58, no. 8, pp. 2520–2524, 2011.

[93] Z. Jibin, X. Qiumin, L. Jieying, W. Runsheng, H. Ru, and W. Yangyuan, "Predictive 3-D Modeling of Parasitic Gate Capacitance in Gate-all-Around Cylindrical Silicon Nanowire MOSFETs," *Electron Devices, IEEE Trans.*, vol. 58, no. 10, pp. 3379–3387, 2011.

[94] S. Hamedi-Hagh and A. Bindal, “Design and Characterization of the Next Generation Nanowire Amplifiers,” *VLSI Des.*, vol. 2008, pp. 1–5, 2008.

[95] A. Bindal, A. Naresh, Y. Pearl, K. K. Nguyen, and S. Hamedi-Hagh, “The Design of Dual Work Function CMOS Transistors and Circuits Using Silicon Nanowire Technology,” *Nanotechnology, IEEE Trans.*, vol. 6, no. 3, pp. 291–302, 2007.

[96] E. Lind and L. E. Wernersson, “Design of RF Properties for Vertical Nanowire MOSFETs,” *Nanotechnology, IEEE Trans.*, vol. 10, no. 4, pp. 668–673, 2011.

[97] T. Bryllert, L. E. Wernersson, L. E. Froberg, and L. Samuelson, “Vertical high-mobility wrap-gated InAs nanowire transistor,” *Electron Device Lett. IEEE*, vol. 27, no. 5, pp. 323–325, 2006.

[98] T. Bryllert, L.-E. Wernersson, T. Löwgren, and L. Samuelson, “Vertical wrap-gated nanowire transistors,” *Nanotechnology*, vol. 17, no. 11, pp. S227–S230, 2006.

[99] A. W. Dey, C. Thelander, E. Lind, K. A. Dick, B. M. Borg, M. Borgstrom, P. Nilsson, and L. E. Wernersson, “High-Performance InAs Nanowire MOSFETs,” *Electron Device Lett. IEEE*, vol. 33, no. 6, pp. 791–793, 2012.

[100] M. Egard, S. Johansson, A. C. Johansson, K. M. Persson, A. W. Dey, B. M. Borg, C. Thelander, L. E. Wernersson, and E. Lind, “Vertical InAs nanowire wrap gate transistors with f(t) > 7 GHz and f(max) > 20 GHz,” *Nano Lett*, vol. 10, no. 3, pp. 809–812, 2010.

[101] K. Jansson, E. Lind, and L. E. Wernersson, “Performance Evaluation of III ─ V Nanowire Transistors,” *Electron Devices, IEEE Trans.*, vol. 59, no. 9, pp. 2375–2382, 2012.

[102] S. Johansson, M. Egard, S. G. Ghalamestani, B. M. Borg, M. Berg, L. E. Wernersson, and E. Lind, “RF Characterization of Vertical InAs Nanowire Wrap-Gate Transistors Integrated on Si Substrates,” *Microw. Theory Tech. IEEE Trans.*, vol. 59, no. 10, pp. 2733–2738, 2011.

[103] K. M. Persson, M. Berg, M. B. Borg, W. Jun, S. Johansson, J. Svensson, K. Jansson, E. Lind, and L. E. Wernersson, “Extrinsic and Intrinsic Performance of Vertical InAs

Nanowire MOSFETs on Si Substrates," *Electron Devices, IEEE Trans.*, vol. 60, no. 9, pp. 2761–2767, 2013.

[104] K. M. Persson, M. Berg, M. Borg, J. Wu, H. Sjoland, E. Lind, and L. E. Wernersson, "Vertical InAs nanowire MOSFETs with IDS = 1.34 mA/μm and gm = 1.19 mS/μm at VDS = 0.5 V," in *Device Research Conference (DRC), 2012 70th Annual*, 2012, pp. 195–196.

[105] C. Rehnstedt, T. Martensson, C. Thelander, L. Samuelson, and L. E. Wernersson, "Vertical InAs Nanowire Wrap Gate Transistors on Si Substrates," *Electron Devices, IEEE Trans.*, vol. 55, no. 11, pp. 3037–3041, 2008.

[106] C. Thelander, C. Rehnstedt, L. E. Froberg, E. Lind, T. Martensson, P. Caroff, T. Lowgren, B. J. Ohlsson, L. Samuelson, and L. E. Wernersson, "Development of a Vertical Wrap-Gated InAs FET," *Electron Devices, IEEE Trans.*, vol. 55, no. 11, pp. 3030–3036, 2008.

[107] C. Thelander, L. E. FrobergFroberg, C. Rehnstedt, L. Samuelson, and L. E. Wernersson, "Vertical Enhancement-Mode InAs Nanowire Field-Effect Transistor With 50-nm Wrap Gate," *Electron Device Lett. IEEE*, vol. 29, no. 3, pp. 206–208, 2008.

[108] L. E. Wernersson, C. Thelander, E. Lind, and L. Samuelson, "III-V Nanowires─Extending a Narrowing Road," *Proc. IEEE*, vol. 98, no. 12, pp. 2047–2060, 2010.

[109] R. Gandhi, C. Zhixian, N. Singh, K. Banerjee, and L. Sungjoo, "Vertical Si-nanowire n - type tunneling FETs with low subthreshold swing (≤ mV/decade) at room temperature," *Electron Device Lett. IEEE*, vol. 32, no. 4, pp. 437–439, 2011.

[110] Z. X. Chen, H. Y. Yu, N. Singh, N. S. Shen, R. D. Sayanthan, G. Q. Lo, and D. L. Kwong, "Demonstration of Tunneling FETs Based on Highly Scalable Vertical Silicon Nanowires," *Electron Device Lett. IEEE*, vol. 30, no. 7, pp. 754–756, 2009.

[111] H. Liu, D. K. Mohata, A. Nidhi, V. Saripalli, V. Narayanan, and S. Datta, "Exploration of vertical MOSFET and tunnel FET device architecture for Sub 10nm node applications," in *Device Research Conference (DRC), 2012 70th Annual*, 2012, pp. 233–234.

[112] L. Xiang, C. Zhixian, S. Nansheng, D. Sarkar, N. Singh, K. Banerjee, L. Guo-Qiang, and K. Dim-Lee, "Vertically Stacked and Independently Controlled Twin-Gate MOSFETs on a Single Si Nanowire," *Electron Device Lett. IEEE*, vol. 32, no. 11, pp. 1492–1494, 2011.

[113] H. G. Virani, R. B. R. Adari, and A. Kottantharayil, "Dual-κ Spacer Device Architecture for the Improvement of Performance of Silicon n-Channel Tunnel FETs," *Electron Devices, IEEE Trans.*, vol. 57, no. 10, pp. 2410–2417, 2010.

[114] K. Sunouchi, H. Takato, N. Okabe, T. Yamada, T. Ozaki, S. Inoue, K. Hashimoto, K. Hieda, A. Nitayama, F. Horiguchi, and F. Masuoka, "A surrounding gate transistor (SGT) cell for 64/256 Mbit DRAMs," in *Electron Devices Meeting, 1989. IEDM '89. Technical Digest., International*, 1989, pp. 23–26.

[115] B. Goebel, J. Lutzen, D. Manger, P. Moll, K. Mummler, M. Popp, U. Scheler, T. Schlosser, H. Seidl, M. Sesterhenn, S. Slesazeck, and S. Tegen, "Fully depleted surrounding gate transistor (SGT) for 70 nm DRAM and beyond," in *Electron Devices Meeting, 2002. IEDM '02. International*, 2002, pp. 275–278.

[116] F. Matsuoka, H. Sakuraba, and F. Masuoka, "Device design guidelines for FC-SGT DRAM cells with high soft-error immunity," *Electron Devices, IEEE Trans.*, vol. 52, no. 6, pp. 1194–1199, 2005.

[117] T. Endoh, M. Suzuki, H. Sakuraba, and F. Masuoka, "$2.4F^2$ memory cell technology with stacked-surrounding gate transistor (S-SGT) DRAM," *Electron Devices, IEEE Trans.*, vol. 48, no. 8, pp. 1599–1603, 2001.

[118] C. Mingcong, Y. Hong Yu, N. Singh, S. Yuan, S. Nan Sheng, Y. Xiaohong, L. Guo-Qiang, and K. Dim-Lee, "Vertical-Si-Nanowire SONOS Memory for Ultrahigh-Density Application," *Electron Device Lett. IEEE*, vol. 30, no. 8, pp. 879–881, 2009.

[119] L. Myoung-Sun, P. Byung-Gook, C. Il Hwan, and L. Jong-Ho, "Characteristics of Elliptical Gate-All-Around SONOS Nanowire With Effective Circular Radius," *Electron Device Lett. IEEE*, vol. 33, no. 11, pp. 1613–1615, 2012.

[120] Y. Sun, H. Y. Yu, N. Singh, K. C. Leong, E. Quek, G. Q. Lo, and D. L. Kwong, "Demonstration of memory string with stacked junction-less SONOS realized on vertical

silicon nanowire," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, pp. 9.7.1–9.7.4.

[121] Y. Sun, H. Y. Yu, N. Singh, K. C. Leong, G. Q. Lo, and D. L. Kwong, "Junctionless Vertical-Si-Nanowire-Channel-Based SONOS Memory With 2-Bit Storage per Cell," *Electron Device Lett. IEEE*, vol. 32, no. 6, pp. 725–727, 2011.

[122] S. Joo Yun, L. Sang-ho, K. Yoon, P. Se Hwan, K. Wandong, K. Do-Bin, and P. Byung-Gook, "A study on gate-AU-around (GAA) polycrystalline silicon channel SONOS flash memory," in *Nanoelectronics Conference (INEC), 2013 IEEE 5th International*, 2013, pp. 69–71.

[123] Y. Sun, H. Y. Yu, N. Singh, N. S. Shen, G. Q. Lo, and D. L. Kwong, "Multibit Programmable Flash Memory Realized on Vertical Si Nanowire Channel," *Electron Device Lett. IEEE*, vol. 31, no. 5, pp. 390–392, 2010.

[124] H. Ru, Z. Jibin, W. Runsheng, F. Chunhui, A. Yujie, Z. Jing, and W. Yangyuan, "Experimental Demonstration of Current Mirrors Based on Silicon Nanowire Transistors for Inversion and Subthreshold Operations," *Electron Devices, IEEE Trans.*, vol. 58, no. 10, pp. 3639–3642, 2011.

[125] S. K. Ghandhi, *VLSI Fabrication Principles*, 2nd Ed.,. John Wiley and Sons Inc., U.K., 2003.

[126] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd Ed.,. John Wiley and Sons Inc., U.K., 2008.

[127] S. Maheshwaram, S. K. Manhas, G. Kaushal, B. Anand, and N. Singh, "Device Circuit Co-Design Issues in Vertical Nanowire CMOS Platform," *Electron Device Lett. IEEE*, vol. 33, no. 7, pp. 934–936, 2012.

[128] J. W. Slotboom, "The pn-product in silicon," *Solid. State. Electron.*, vol. 20, no. 4, pp. 279–283, Apr. 1977.

[129] J. W. Slotboom and H. C. de Graaff, "Bandgap narrowing in silicon bipolar transistors," *Electron Devices, IEEE Transactions on*, vol. 24, no. 8. pp. 1123–1125, 1977.

[130] J. W. Slotboom and H. C. de Graaff, “Measurements of Bandgap Narrowing in Si Bipolar Transistors,” *Solid. State. Electron.*, vol. 19, no. 10, pp. 857–862, 1976.

[131] D. B. M. Klaassen, J. W. Slotboom, and H. C. de Graaff, “Unified apparent bandgap narrowing in n- and p-type silicon,” *Solid. State. Electron.*, vol. 35, no. 2, pp. 125–129, Feb. 1992.

[132] D. B. M. Klaassen, “A unified mobility model for device simulation—I. Model equations and concentration dependence,” *Solid. State. Electron.*, vol. 35, no. 7, pp. 953–959, Jul. 1992.

[133] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, “Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits,” *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, 2003.

[134] H.-N. Lin, W.-W. Hsu, W.-C. Lee, and C. H. Wann, “Ultimate contact resistance scaling enabled by an accurate contact resistivity extraction methodology for sub-20 nm node,” *VLSI Technology, 2009 Symposium on*. pp. 102–103, 2009.

[135] S. Bangsaruntip, G. M. Cohen, A. Majumdar, Y. Zhang, S. U. Engelmann, N. C. M. Fuller, L. M. Gignac, S. Mittal, J. S. Newbury, M. Guillorn, T. Barwicz, L. Sekaric, M. M. Frank, and J. W. Sleight, “High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling,” in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1–4.

[136] M. J. van Dort, P. H. Woerlee, and A. J. Walker, “A simple model for quantisation effects in heavily-doped silicon MOSFETs at inversion conditions,” *Solid. State. Electron.*, vol. 37, no. 3, pp. 411–414, Mar. 1994.

[137] S. A. Hareland, S. Jallepalli, G. Chindalore, W.-K. Shih, A. F. Tasch Jr., and C. M. Maziur, “A simple model for quantum mechanical effects in hole inversion layers in silicon PMOS devices,” *Electron Devices, IEEE Transactions on*, vol. 44, no. 7. pp. 1172–1173, 1997.

[138] J. D. Bude, “MOSFET modeling into the ballistic regime,” in *Simulation of Semiconductor Processes and Devices, 2000. SISPAD 2000. 2000 International Conference on*, 2000, pp. 23–26.

[139] S. Maheshwaram, S. K. Manhas, G. Kaushal, B. Anand, and N. Singh, "Vertical Nanowire CMOS Parasitic Modeling and its Performance Analysis," *Electron Devices, IEEE Transactions on*, vol. PP, no. 99. p. 1, 2013.

[140] M. Zahn, *Electromagnetic Field Theory: A Problem Solving Approach*. New York: Wiley, 1979.

[141] K. Suzuki, "Parasitic capacitance of submicrometer MOSFET's," *Electron Devices, IEEE Trans.*, vol. 46, no. 9, pp. 1895–1900, 1999.

[142] N. R. Mohapatra, M. P. Desai, S. G. Narendra, and V. Ramgopal Rao, "Modeling of parasitic capacitances in deep submicrometer conventional and high-K dielectric MOS transistors," *Electron Devices, IEEE Trans.*, vol. 50, no. 4, pp. 959–966, 2003.

[143] G. Baccarani and G. A. Sai-Halasz, "Spreading resistance in submicron MOSFET's," *Electron Device Lett. IEEE*, vol. 4, no. 2, pp. 27–29, 1983.

[144] J. T. Smith, Y. Zhao, C. Yang, and J. Appenzeller, "Effects of nanoscale contacts to silicon nanowires on contact resistance: Characterization and Modeling," *Device Research Conference (DRC), 2010*. pp. 139–140, 2010.

[145] C. Luryi, H. Byoung Hak, J. Young Chai, C. Keun Hwi, Y. Kyoung Hwan, K. Dong-Won, J. Gyo Young, O. Kyung-Seok, W.-S. Lee, S. Sang-Hun, R. Jae-Sung, W. Dong Mok, and H. Sung Woo, "Extracting Mobility Degradation and Total Series Resistance of Cylindrical Gate-All-Around Silicon Nanowire Field-Effect Transistors," *Electron Device Lett. IEEE*, vol. 30, no. 6, pp. 665–667, 2009.

[146] A. Raychaudhuri, M. J. Deen, M. I. H. King, and J. Kolk, "Finding the asymmetric parasitic source and drain resistances from the a.c. conductances of a single MOS transistor," *Solid. State. Electron.*, vol. 39, no. 6, pp. 909–913, 1996.

[147] C.-K. Baek, S. Park, M.-D. Ko, T. Rim, S. Choi, and Y.-H. Jeong, "Characteristics of gate-all-around silicon nanowire field effect transistors with asymmetric channel width and source/drain doping concentration," *J. Appl. Phys.*, vol. 112, no. 3, p. 34513, 2012.

[148] M. H. Na, E. J. Nowak, W. Haensch, and J. Cai, “The effective drive current in CMOS inverters,” in *Electron Devices Meeting, 2002. IEDM ’02. International*, 2002, pp. 121–124.

[149] “Preditive Technology Model.” [Online]. Available: www.ptm.asu.edu/.

[150] W. Lan, D. Jie, C. Li-Wen, K. Keunwoo, C. Ching-Te, and H. S. P. Wong, “Selective Device Structure Scaling and Parasitics Engineering: A Way to Extend the Technology Roadmap,” *Electron Devices, IEEE Trans.*, vol. 56, no. 2, pp. 312–320, 2009.

PUBLICATIONS

Publications out of this thesis work:

1. **S. Maheshwaram**, S.K. Manhas, G. Kaushal, B. Anand and N. Singh, "Vertical Nanowire CMOS Parasitic Modeling and its Performance Analysis," *IEEE Transactions on Electron Devices,* vol.60, no.9, pp.2943-2950, Sept. 2013.

2. **S. Maheshwaram**, S.K. Manhas, G. Kaushal, B. Anand, N. Singh, "Device Circuit Co-Design Issues in Vertical Nanowire CMOS Platform," *IEEE Electron Device Letters,* vol.33, no.7, pp.934-936, Jul. 2012.

3. **S. Maheshwaram**, S.K. Manhas, G. Kaushal, B. Anand, N. Singh, "Vertical Silicon Nanowire Gate-All-Around Field Effect Transistor Based Nanoscale CMOS," *IEEE Electron Device Letters,* vol.32, no.8, pp.1011-1013, Aug. 2011.

4. **S. Maheshwaram**, S.K. Manhas, and B. Anand, "Vertical Nanowire Transistor Based CMOS VTC Analysis," in *proc. ICEE,* Dec. 2014, India. (Presented)

5. **S. Maheshwaram**, S.K. Manhas, G. Kaushal, and B. Anand, "Vertical Nanowire MOSFET Parasitic Resistance Modeling," in *proc. IEEE EDSSC,* pp.1-2, 3-5 Jun. 2013, Hong Kong.

6. **S. Maheshwaram**, G. Kaushal, S. K. Manhas, "A High Performance Vertical Si Nanowire CMOS for Ultra High Density Circuits," *in Proc. IEEE APCCAS*, pp. 1219-1222, Dec. 2010, Kuala Lumpur, Malaysia.

Other related publications:

7. Gaurav Kaushal, S. K. Manhas, **S. Maheshwaram**, S. Dasgupta, B. Anand, and N. Singh, "Novel Design Methodology using L_{EXT} sizing in Nanowire CMOS Logic" in *IEEE Transactions on Nanotechnology***,** vol. 13, no. 4, pp. 650-658, Jul. 2014.

8. Ravi Shankar, G. Kaushal, **S. Maheshwaram**, S. Dasgupta, S. K. Manhas, "A Degradation Model of Double Gate and Gate-All-Around MOSFETs With Interface Trapped Charges Including Effects of Channel Mobile Charge Carriers," IEEE Trans. Material and Device Reliability, Vol. 14, No. 2, p. 689, 2014

9. A. Pandey, S. Raycha, **S. Maheshwaram**, S.K. Manhas, S. Dasgupta, A.K. Saxena, and B. Anand, "Effect of Load Capacitance and Input Transition Time on FinFET Inverter Capacitances," *IEEE Transactions on Electron Devices*, vol.61, no.1, pp.30-36, Jan. 2014.

10. Gaurav Kaushal, S.K. Manhas, **S. Maheshwaram**, and S. Dasgupta "Impact of Series Resistance on Si Nanowire MOSFET Performance" *Springer Journal of Computational Electronics*, no. 13, pp. 449-458, Mar. 2013.

11. Gaurav Kaushal, S.K. Manhas, **S. Maheshwaram**, S. Dasgupta, B. Anand, and N. Singh, "Tuning Source/Drain Extension Profile for Current Matching in Nanowire CMOS Logic" in *IEEE Transactions on Nanotechnology*, vol. 11, no. 5, pp. 1033-1039, Sep. 2012.

12. Gaurav Kaushal, S. S. Rathod, **S. Maheshwaram**, S. K. Manhas, A. K. Saxena, and S. Dasgupta, "Radiation Effects in Si-NW GAA FET and CMOS Inverter: A TCAD Simulation Study" in *IEEE Transactions on Electron Devices*, vol. 59, no. 5, pp. 1563-1566, May 2012.

13. G. Kaushal, **S. Maheshwaram**, S. Dasgupta, and S.K. Manhas, "Drive matching issues in multi gate CMOS inverter," in proc. *IEEE ICSC,* pp.349-354, 12-14 Dec. 2013, Noida, India.

14. A. Pandey, S. Raycha, **S. Maheshwaram**, S. K. Manhas, S. Dasgupta, A. K. Saxena and B. Anand "FinFET Device Capacitances: Impact of Input Transition Time and Output Load," *Proc. Nanoelectronics conference* (*INEC*), pp.393-395, 2-4 Jan. 2013, Singapore.

APPENDIX A

In this appendix we present structure code of a VNWFET device with typical dimensions used in Sentaurus structure editor:

```
; L=45nm, Tox=2 nm, NwDia= 10nm, S/Dext=30nm

(sdegeo:set-auto-region-naming OFF)
;---old replaces new enabled
(sdegeo:set-default-boolean "BAB")

;***substrate region with STI
(sdegeo:create-cuboid
      (position 0 0 0)
      (position 0.315 0.135 0.100 )
      "Silicon" "Sub"
)
(sdegeo:create-cuboid
      (position 0.015 0.015 0.100)
      (position 0.195 0.120 0.300)
      "Silicon" "SrcSub"
)

(sdegeo:bool-unite (list
      (car (find-body-id (position 0.1575 0.0675 0.05)))
      (car (find-body-id (position 0.1575 0.0675 0.2))))
)

;***nanowire regions
(sdegeo:create-cylinder
      ( position 0.1575 0.0675 0.3 )
      ( position 0.1575 0.0675 0.332 )
        0.005 "Silicon" "Src"
)
(sdegeo:create-cylinder
      ( position 0.1575 0.0675 0.332 )
      ( position 0.1575 0.0675 0.373 )
        0.005 "Silicon" "Chn"
)
(sdegeo:create-cylinder
      ( position 0.1575 0.0675 0.373 )
      ( position 0.1575 0.0675 0.435 )
```

```
        0.005 "Silicon" "Drn"
)
;***gate region
(sdegeo:create-cylinder
      ( position 0.1575 0.0675 0.33 )
      ( position 0.1575 0.0675 0.375)
        0.007 "SiO2" "Gaox"
)

(sdegeo:create-cylinder
      ( position 0.1575 0.0675 0.33 )
      ( position 0.1575 0.0675 0.375 )
        0.017) "Metal" "GaMet"
)
(sdegeo:create-cuboid
      ( position 0.1305 0.0405 0.33 )
      ( position 0.2925 0.0945 0.36 )
        "Metal" "GaMetext"
)

;****metal contacts
(sdegeo:create-cuboid
      ( position 0.225 0.045 0.36 )
      ( position 0.27 0.09 0.445)
      "Aluminum" "Gacon"
)
(sdegeo:create-cuboid
      ( position 0.045 0.045 0.03)
      ( position 0.09 0.090 0.445)
      "Aluminum" "Srccon"
)
(sdegeo:create-cuboid
      ( position 0.135 0.045 0.405)
      ( position 0.18 0.09 0.445)
      "Aluminum" "Drncon"
)

;***isolation oxide
(sdegeo:create-cuboid
      ( position 0 0 0.100)
      ( position 0.315 0.135 0.300)
      "SiO2" "Stiox"
)
```

```
(sdegeo:create-cuboid
      ( position 0 0 0.300)
      ( position 0.315 0.135 0.404)
      "SiO2" "Isolaox"
)

;***electrical contacts
(sdegeo:define-contact-set "gate" 4  (color:rgb 1 0 0 ) "##" )
(sdegeo:define-contact-set "drain" 4  (color:rgb 1 0 0 ) "::" )
(sdegeo:define-contact-set "source" 4  (color:rgb 1 0 0 ) "[] []" )

(sdegeo:set-current-contact-set "drain")
(sdegeo:define-3d-contact
(list (car (find-face-id (position 0.1575 0.0675 0.445)))) "drain")

(sdegeo:set-current-contact-set "source")
(sdegeo:define-3d-contact
(list (car (find-face-id (position 0.0675 0.0675 0.445)))) "source")

(sdegeo:set-current-contact-set "gate")
(sdegeo:define-3d-contact
(list (car (find-face-id (position 0.2475 0.0675 0.445)))) "gate")

;***reference windows
(sdedr:define-refeval-window
      "RefSrcSub" "Cuboid"
      (position 0.015 0.015 0.250)
      (position 0.195 0.120 0.300)
)
(sdedr:define-refeval-window
      "RefSrcSub2" "Cuboid"
      (position 0.015 0.015 0.225)
      (position 0.195 0.120 0.300)
)

;********constant doping regions
(sdedr:define-constant-profile "SubDoping" "BoronActiveConcentration"
1e16)
(sdedr:define-constant-profile-region "Sub" "SubDoping" "Sub")

(sdedr:define-constant-profile "SrcSubDoping" "ArsenicActiveConcent-
ration" 1e20)
```

```
(sdedr:define-constant-profile-placement "SrcSub" "SrcSubDoping"
"RefSrcSub")

(sdedr:define-constant-profile "srcDoping" "ArsenicActiveConcent-
ration" 1e19)
(sdedr:define-constant-profile-region "Src" "srcDoping" "Src")

(sdedr:define-constant-profile "ChnDoping" "BoronActiveConcentration"
1e16)
(sdedr:define-constant-profile-region "Chn" "ChnDoping" "Chn")

(sdedr:define-constant-profile "DrnDoping" "ArsenicActiveConcent-
ration" 1e19)
(sdedr:define-constant-profile-region "Drn" "DrnDoping" "Drn")

;*********meshing
(sdedr:define-refinement-size "Sub" 0.03 0.03 0.03 0.03 0.03 0.03 )
(sdedr:define-refinement-region "Sub" "Sub" "Sub" )
(sdedr:define-refinement-function "Sub" "DopingConcentration"
"MaxTransDiff" 1)

(sdedr:define-refinement-size "Stiox" 0.02 0.02 0.02 0.02 0.02 0.02 )
(sdedr:define-refinement-region "Stiox" "Stiox" "Stiox" )
(sdedr:define-refinement-function "Stiox" "DopingConcentration"
"MaxTransDiff" 1)

(sdedr:define-refinement-size "Isoox" 0.01 0.01 0.01 0.01 0.01 0.01 )
(sdedr:define-refinement-region "Isolaox" "Isoox" "Isolaox" )
(sdedr:define-refinement-function "Isoox" "DopingConcentration"
"MaxTransDiff" 1)

(sdedr:define-refinement-size "DefSrcSub" 0.01 0.01 0.01 0.005 0.005
0.005 )
(sdedr:define-refinement-placement "SrcSub" "DefSrcSub" "RefSrcSub2"
)
(sdedr:define-refinement-function "DefSrcSub" "DopingConcentration"
"MaxTransDiff" 1)


(sdedr:define-refinement-size "Src" 0.001 0.001 0.002 0.001 0.001
0.002 )
(sdedr:define-refinement-region "Src" "Src" "Src" )
```

```
(sdedr:define-refinement-function "Src" "DopingConcentration"
"MaxTransDiff" 1)

(sdedr:define-refinement-size "Chn" 0.001 0.001 0.002 0.001 0.001
0.002 )
(sdedr:define-refinement-region "Chn" "Chn" "Chn" )
(sdedr:define-refinement-function "Chn" "DopingConcentration"
"MaxTransDiff" 1)

(sdedr:define-refinement-size "Drn" 0.001 0.001 0.002 0.001 0.001
0.002 )
(sdedr:define-refinement-region "Drn" "Drn" "Drn" )
(sdedr:define-refinement-function "Drn" "DopingConcentration"
"MaxTransDiff" 1)

(sdedr:define-refinement-size "Gaox" 0.001 0.001 0.002 0.001 0.001
0.002 )
(sdedr:define-refinement-region "Gaox" "Gaox" "Gaox" )
(sdedr:define-refinement-function "Gaox" "DopingConcentration"
"MaxTransDiff" 1)

(sdedr:define-refinement-size "AlCon" 0.005 0.005 0.005 0.005 0.005
0.005 )
(sdedr:define-refinement-material "AlCon" "AlCon" "Aluminum" )
(sdedr:define-refinement-function "AlCon" "DopingConcentration"
"MaxTransDiff" 1)

(sdedr:define-refinement-size "GateMet" 0.005 0.005 0.005 0.005 0.005
0.005 )
(sdedr:define-refinement-region "GateMet" "GateMet" "GaMet" )

(sdedr:define-refinement-function "GateMet" "DopingConcentration"
"MaxTransDiff" 1)


(sdedr:define-refinement-size "GateMetext" 0.005 0.005 0.005 0.005
0.005 0.005 )
(sdedr:define-refinement-material "GateMetext" "GateMetext"
"GaMetext" )
(sdedr:define-refinement-function "GateMetext" "DopingConcentration"
"MaxTransDiff" 1)

(sde:save-model "n45wf4pt4")
```

```
(sde:build-mesh "mesh" "-P -discontinuousData -d -F tdr "
"n45wf4pt4")
```

This creates a structure with following mesh properties:

Vertices = 20132

Edges = 134742

Faces = 226865

Elements = 112394

This device will take around 4 hours to simulate one I-V curve when run on four threads.

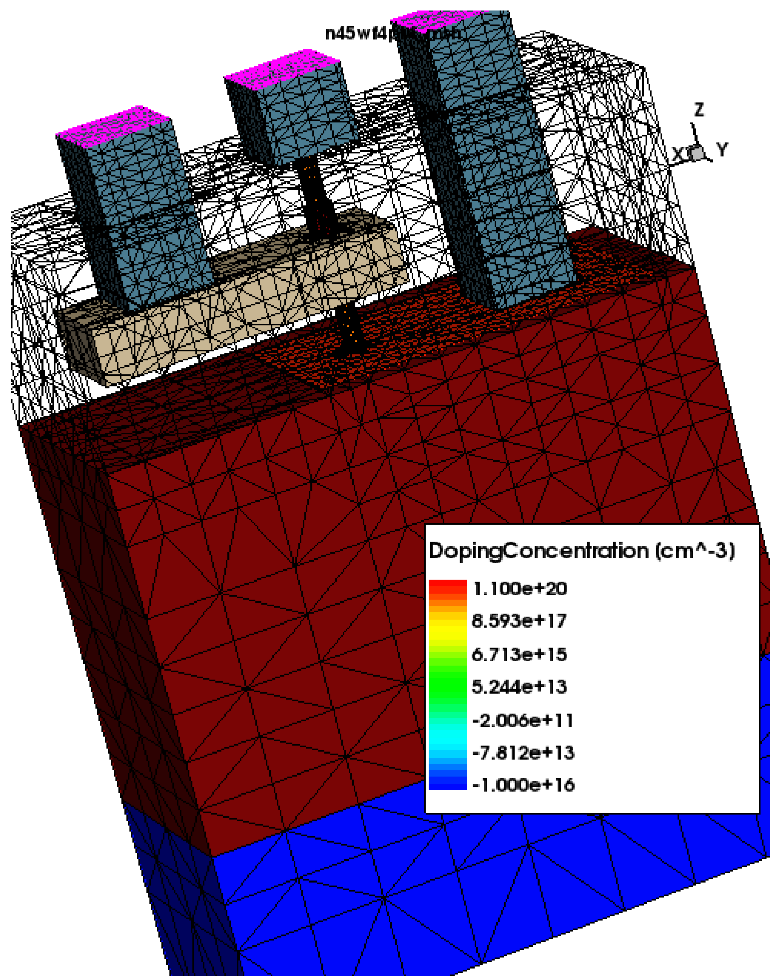

Figure A.1 3D device structure of a VNWFET with typical dimensions and coarse meshing. The isolation oxide is made translucent to see the nanowire and gate regions.

APPENDIX B

Device physics and other related sections used in Sentaurus device simulations of VNWFET:

B.1 Electrode terminals are initialized to 0 V.

```
Electrode
{
      { Name="source" Voltage=0.0 }
      { Name="drain" Voltage= 0.0 }
      { Name="gate"  Voltage= 0.0 }
}
```

B.2 Thermal electrodes are defined to account for joule heating effect.

```
Thermode
{
      { Name="source" Temperature=300 SurfaceResistance=1e-3}
      { Name="drain" Temperature=300 SurfaceResistance=1e-3}
      { Name="gate"  Temperature=300 SurfaceResistance=5e-5}
}
```

B.3 Physics section consists of band gap narrowing model, Fermi - carrier statistics, QCvanDort quantization, mobility is included by incorporating Philips unified mobility model –PhuMob along with high field saturation and enormal effects. The recombination section includes band2band tunneling and SRH.

```
Physics
{
      EffectiveIntrinsicDensity (BandGapNarrowing (OldSlotboom))
      eQCvanDort
      hQCvanDort
      Fermi
      Mobility
      (
            PhuMob
            eHighFieldsaturation( GradQuasiFermi )
            hHighFieldsaturation( GradQuasiFermi )
            Enormal
      )
```

```
	Recombination
	(
			Band2Band
			SRH( DopingDep )
	)
}
```

B.4 For the silicon and oxide interface gate tunneling is enabled for both FN and direct tunneling phenomenon.

```
Physics(MaterialInterface="Silicon/Oxide")
{
	GateCurrent( Fowler GateName="gate"  )
	GateCurrent( DirectTunneling )
}
```

B.5 At the metal-silicon interface a distributed resistance of 1×10^{-8} Ω.cm^2 is used to consider impact of contact resistance.

```
Physics(MaterialInterface = "Aluminum/Silicon")
{
	DistResistance=1e-8
}
```

B.6 Following plot section lists the device internal properties which are saved along with device for given terminal voltages.

```
Plot {
	eDensity hDensity
	eCurrent hCurrent TotalCurrent ConductionCurrent
	DisplacementCurrent
	eMobility hMobility
	eVelocity hVelocity eDriftVelocity hDriftVelocity
	eQuasiFermi hQuasiFermi

	ElectricField/Vector
	Potential BuiltinPotential SpaceCharge

	Temperature eTemperature hTemperature
```

```
    SRHRecombination
    Band2Band

    eGradQuasiFermi/Vector hGradQuasiFermi/Vector
    eEparallel hEparallel eEnormal hEnormal

    ConductionBandEnergy ValenceBandEnergy
    EffectiveBandGap EquilibriumPotential
    IntrinsicDensity EffectiveIntrinsicDensity

    DonorConcentration AcceptorConcentration Doping
    eIonIntegral  hIonIntegral MeanIonIntegral

    HotElectronInjection HotHoleInjection
    FowlerNordheim
    BarrierTunneling eBarrierTunneling hBarrierTunneling
    eDirectTunnel hDirectTunnel
  }
```

B.7 The following math section highlights the multi thread flag setting to carry out simulations on multiple cores for simulation speed up. The number of newton iterations allowed is reset using iterations, precision is increased by considering digits=5 and wallclock is enabled to note down simulation time.

```
Math
{
    Iterations=40
    NotDamped=100
    Error(electron) = 1e10
    Error(hole) = 1e10
    Digits = 5
    Number_of_Threads = 4
    StackSize=990000000
    wallclock
 }
```

B.8 Material model parameters.

#Metal workfunction

```
Material = "Metal"
{
   Bandgap
  {
     WorkFunction     = 4.4 #  [eV]
     FermiEnergy      = 11.7     #  [eV]
  }
}
```

High field saturation model parameters of Silicon

```
Material = "Silicon"
{
     HighFieldDependence:
     {
          vsat0 = 1.400e+07 ,    1.200e+07
          vsatexp    = 0.87 ,    0.52
     }

     HighFieldDependence_aniso:
     {
          vsat0 = 1.400e+07 ,    1.200e+07
          vsatexp    = 0.87 ,    0.52
     }
     VanDortQMModel
     {
          eFit = 2.4e-8
          hFit = 1.8e-8
          eEcritQC = 1e5
          hEcritQC = 1e5
          dRef = 2.5e-6
     }
     PhuMob:
     { * Philips Unified Mobility Model:
          mumax_As   = 1.4170e+03     # [cm^2/Vs]
          mumin_As   = 52.2     # [cm^2/Vs]
          theta_As   = 2.285    #
          n_ref_As   = 9.6800e+16     # [cm^(-3)]
          alpha_As   = 0.68     #
          mumax_B    = 4.7050e+02     # [cm^2/Vs]
          mumin_B    = 44.9     # [cm^2/Vs]
          theta_B    = 2.247    #
          n_ref_B    = 2.2300e+17     # [cm^(-3)]
          alpha_B    = 0.719    #
```

```
        nref_D     = 4.0000e+20     # [cm^(-3)]
        nref_A     = 7.2000e+20     # [cm^(-3)]
        cref_D     = 0.21      #
        cref_A     = 0.5 #
        me_over_m0 = 1   #
        mh_over_m0 = 1.258     #
    }

}
```

APPENDIX C

In this appendix we present solve section of Sentaurus device simulation setup for different types of device simulations and system, solve section for circuit analysis simulations.

C.1 Solve section for I_D-V_{GS} characteristics

```
Solve {

Coupled (Iterations=20) { Poisson }
Coupled (Iterations=20) { Poisson Electron Hole Contact Circuit
Temperature }

Quasistationary
(
      InitialStep=1e-3  Increment=1.35
      MaxStep=0.01 Minstep=1e-7
      Goal { name="drain" Voltage= 1.0}
){
      Coupled { Poisson Electron Hole Contact Circuit Temperature }
      Save(FilePrefix="Vdrn_n45wf4pt4" Time=(0.05; 1) NoOverWrite)
}

Load(FilePrefix="Vdrn_n45wf4pt4_0000")
NewCurrentPrefix="IdVg_Vd0pt05_"
Quasistationary
(
      InitialStep=1e-2  Increment=1.35
      MaxStep=10e-3 Minstep=1e-15
      Goal { name="gate" Voltage= 1.0 }
) {
      Coupled { Poisson Electron Hole Contact Circuit Temperature }
  }

Load(FilePrefix="Vdrn_n45wf4pt4_0001")
NewCurrentPrefix="IdVg_Vd1pt0_"
Quasistationary
(
      InitialStep=1e-2  Increment=1.35
      MaxStep=10e-3 Minstep=1e-15
      Goal { name="gate" Voltage= 1.0 }
){
```

```
      Coupled { Poisson Electron Hole Contact Circuit Temperature }
 }
}
```

From the I_D-V_{GS} curves one can obtain I_{ON}, I_{OFF}, transconductance, threshold voltage, subthreshold slope and drain induced barrier lowering.

C.2 Solve section for I_D-V_{DS} characteristics

```
Solve {
Coupled (Iterations=20) { Poisson }
Coupled (Iterations=20) { Poisson Electron Hole Contact Circuit
Temperature }

Quasistationary
(
      InitialStep=1e-3  Increment=1.35
      MaxStep=0.01 Minstep=1e-7
      Goal { name="gate" Voltage= 1.0}
){
      Coupled { Poisson Electron Hole Contact Circuit Temperature }
      Save(FilePrefix="Vga_n45wf4pt4" Time=(0.5; 1) NoOverWrite)
}

Load(FilePrefix="Vga_n45wf4pt4_0000")
NewCurrentPrefix="IdVd_Vg0pt5_"
Quasistationary
(
      InitialStep=1e-2  Increment=1.35
      MaxStep=10e-3 Minstep=1e-15
      Goal { name="drain" Voltage= 1.0 }
) {
      Coupled { Poisson Electron Hole Contact Circuit Temperature }
  }

Load(FilePrefix="Vga_n45wf4pt4_0001")
NewCurrentPrefix="IdVd_Vg1pt0_"
Quasistationary
(
      InitialStep=1e-2  Increment=1.35
      MaxStep=10e-3 Minstep=1e-15
      Goal { name="drain" Voltage= 1.0 }
){
      Coupled { Poisson Electron Hole Contact Circuit Temperature }
```

```
 }
}
```

From the I_D-V_{DS} curves one can obtain λ_{CLM} which is channel length modulation coefficient and output conductance.

C.3 System and solve section for CMOS inverter VTC analysis. The system section defines the SPICE equivalent circuit netlist.

```
System
{
      Vsource_pset vndd (vdd GND) { dc = 0.0 }
      Vsource_pset vnin (vin GND) { dc = 0.0 }

      PMOS p1 ("source"=vdd "drain"=vout "gate"=vin)
      NMOS n1 ("source"=GND "drain"=vout "gate"=vin)
      Set (GND = 0)
      Plot "stat1pt0_nodes.plt" (time() v(vout) v(vin))

}

Solve
{
  Coupled(Iterations=100){ Poisson }
  Coupled(Iterations=100){ Poisson Electron Hole Contact Circuit
Temperature }
  Quasistationary
  (
     InitialStep=2e-3 Increment=1.35
     MinStep=1e-10 MaxStep=0.01
     Goal{ Parameter=vndd.dc Voltage= 1.0 }
  ){ Coupled{ Poisson Electron Hole Contact Circuit Temperature }
     Save(FilePrefix="Vdd_15nm" Time=(0.5;1) NoOverWrite)
   }

Load(FilePrefix="Vdd_15nm_0000")
  NewCurrentFile="final0pt5"
  Quasistationary
  (
     InitialStep=1e-3 Increment=1.35
     MinStep=1e-10 MaxStep=10e-3
     Goal{ Parameter=vnin.dc Voltage= 1.0 }
  ){ Coupled{ Poisson Electron Hole Contact Circuit Temperature }
```

```
   }

Load(FilePrefix="Vdd_15nm_0001")
  NewCurrentFile="final1pt0"
  Quasistationary
(
     InitialStep=1e-3 Increment=1.35
     MinStep=1e-10 MaxStep=10e-3
     Goal{ Parameter=vnin.dc Voltage= 1.0 }
  ){ Coupled{ Poisson Electron Hole Contact Circuit  Temperature }
   }
}
```

From VTC results once can obtain maximum gain and noise margins.

C.4 System and Solve section for C-V_{GS} characteristics.

```
System
{
  NMOS nmos1 (drain=d source=s gate=g)
  Vsource_pset vd ( d 0 ){ dc = 0 }
  Vsource_pset vs ( s 0 ){ dc = 0 }
  Vsource_pset vg ( g 0 ){ dc = 0 }
}

Solve {

Coupled (Iterations=100) { Poisson }
Coupled (Iterations=100) { Poisson Electron Hole Contact Circuit
temperature}

Quasistationary
(
     InitialStep=0.01 Increment=1.3
     MaxStep=0.1 Minstep=1.e-15
     Goal { Parameter=vg.dc Voltage=-0.25}
){ Coupled { Poisson Electron Hole Contact Circuit temperature } }

NewCurrentFile="C_Vgs_"
  Quasistationary
(
     InitialStep=0.001 Increment=1.3
     MaxStep=0.008 Minstep=1.e-15
     Goal { Parameter=vg.dc Voltage=1.25}
```

```
){
# AC analysis to obtain CV characteritics
ACCoupled (
       StartFrequency=1e5 EndFrequency=1e5 NumberOfPoints=1 Decade
       Node(d s g) Exclude(vd vs vg)
       ACCompute (Time = (Range = (0 1)  Intervals = 150))
     ){ Poisson Electron Hole Contact Circuit temperature }
  }
}
```

To obtain C-V_{GS} characteristics, from the result plot c(g,g), c(g,s) and c(g,d) versus gate voltage sweep. The capacitances at V_{GS}=0V corresponds to parasitic capacitance.

C.5 System and Solve section for C-V_{DS} characteristics.

```
System
{
  NMOS nmos1 (drain=d source=s gate=g)
  Vsource_pset vd ( d 0 ){ dc = 0 }
  Vsource_pset vs ( s 0 ){ dc = 0 }
  Vsource_pset vg ( g 0 ){ dc = 0 }
}

Solve {

Coupled (Iterations=100) { Poisson }
Coupled (Iterations=100) { Poisson Electron Hole Contact Circuit
temperature}

Quasistationary
(
     InitialStep=0.01 Increment=1.3
     MaxStep=0.1 Minstep=1.e-15
     Goal { Parameter=vd.dc Voltage=-0.25}
){ Coupled { Poisson Electron Hole Contact Circuit temperature } }

NewCurrentFile="C_Vds_"
  Quasistationary
(
     InitialStep=0.001 Increment=1.3
     MaxStep=0.008 Minstep=1.e-15
     Goal { Parameter=vd.dc Voltage=1.25}
){
# AC analysis to obtain CV characteritics
```

```
ACCoupled (
       StartFrequency=1e5 EndFrequency=1e5 NumberOfPoints=1 Decade
       Node(d s g) Exclude(vd vs vg)
       ACCompute (Time = (Range = (0 1) ntervals = 150))
     ){ Poisson Electron Hole Contact Circuit temperature }
  }
}
```

C.6 System and Solve section for frequency response of intrinsic device.

```
System {
  Vsource_pset vnvdd ( vdd 0 ){ dc = 0 }
  Vsource_pset vnvin ( vin 0 ){ dc = 0 }
  Vsource_pset vnvss ( GND 0 ){ dc = 0 }

  NMOS n1 ("source"=GND "drain"=vdd "gate"=vin)
  ACPlot ( freq() time() v(vin) v(vout))
}

Solve {
Coupled (Iterations=20) { Poisson }
Coupled (Iterations=20) { Poisson Electron Hole Contact Circuit
Temperature }

Quasistationary
(
     InitialStep=1e-3  Increment=1.35
     MaxStep=0.05 Minstep=1e-10
     Goal { parameter=vnvdd.dc Voltage=0.8 }
){ Coupled { Poisson Electron Hole Contact Circuit Temperature } }

Quasistationary
(
      InitialStep=10e-3  Increment=1.35
      MaxStep=50e-3 Minstep=1e-10
      Goal { Parameter=vnvin.dc Voltage= 0.4 }
) { Coupled { Poisson Electron Hole Contact Circuit Temperature } }

ACCoupled
(
    StartFrequency=1e0 EndFrequency=1e14 NumberOfPoints=135 decade
    Node(vdd vin GND) Exclude(vnvdd vnvin vnvss)
){ Poisson Electron Hole Contact Circuit Temperature}
}
```

In the results file plot a(vdd,vin) which is g_m of device and a(vdd,vdd) which is g_{ds} of device. From, these parameters device intrinsic gain is obtained as $20*\log10(g_m/g_{ds})$.

C.7 System and Solve section for frequency response of Common-source amplifier.

```
System
{
     Vsource_pset vnvdd  ( vdd GND) { dc= 0}
     Vsource_pset vnvin (vin GND) {dc = 0}
     Vsource_pset vnvss (vss GND) { dc = 0.0 }
     Set (GND = 0)

      Resistor_pset p1 (vout vdd) { resistance = 94456}
     NMOS n1 ("source"=vss "drain"=vout "gate"=vin)

      ACPlot ( freq() time() v(vin) v(vout))
}

Solve {
Coupled (Iterations=20) { Poisson }
Coupled (Iterations=20) { Poisson Electron Hole Contact Circuit
Temperature }

#bias the supply to Vdd
Quasistationary
(
      InitialStep=1e-3  Increment=1.35
      MaxStep=0.05 Minstep=1e-10
      Goal { parameter=vnvdd.dc Voltage=0.8 }
) { Coupled { Poisson Electron Hole Contact Circuit Temperature } }

#bias the input voltage
Quasistationary
(
      InitialStep=50e-3  Increment=1.35
      MaxStep=50e-3 Minstep=1e-10
      Goal { Parameter=vnvin.dc Voltage= 0.4 }
) { Coupled { Poisson Electron Hole Contact Circuit Temperature } }
# Frequency analysis
ACCoupled (
       StartFrequency=1e0 EndFrequency=1e14 NumberOfPoints=135 decade
       Node(vin vss vout) Exclude(vnvin vnvss )
       ){ Poisson Electron Hole Contact Circuit Temperature}
```

```
}
```

C.8 System and Solve section for transient analysis of inverter followed by inverter circuit.

```
System {
        Vsource_pset vnvdd  ( vdd GND) {dc = 0.0}
        Vsource_pset vnvin (vin GND) {
           pulse = (0.0      # dc
                    1.0      # amplitude
                    1e-12    # td
                    5e-12    # tr
                    5e-12    # tf
                    60e-12   # ton
                    130e-12  )
        }

         Capacitor_pset co ( vout GND ){ capacitance = 60e-18 }
        Set (GND = 0)

        PMOS p1 ("source"=vdd "drain"=vx "gate"=vin)
        NMOS n1 ("source"=GND "drain"=vx "gate"=vin)
        PMOS p2 ("source"=vdd "drain"=vout "gate"=vx)
        NMOS n2 ("source"=GND "drain"=vout "gate"=vx)

Plot "nodes1pt0_tran.plt"(time() v(vdd) v(vout) v(vx) v(vin)
i(p1,vdd) i(n1,GND) i(n1,vx) i(p1,vx) i(p1,vin) i(n1,vin) i(co,vout)
i(vnvin, vin))

}

Solve {
  Coupled(Iterations=100){ Poisson }
  Coupled(Iterations=100){ Poisson Electron Hole Contact Circuit
temperature }
Quasistationary
(
     InitialStep=0.002 Increment=1.35
     MinStep=1e-10 MaxStep=0.01
     Goal{ Parameter=vnvdd.dc Voltage= 1.0 }
  ){ Coupled{ Poisson Electron Hole Contact Circuit temperature}
  }
NewCurrentFile="Tran1pt0_45nm_"
```

```
 Transient
(
      InitialTime=0 FinalTime=80e-12
      InitialStep=2e-14 Increment=1.35
      MinStep=1e-20 MaxStep=10e-14
) { Coupled{ Poisson Electron Hole Contact Circuit temperature}
}
}
```

In the results file plot vin, vout, vx versus time and extract the delays T_{pHL} and T_{pLH}.