GaN HEMT Modeling and Radio Frequency Power Amplifier Design

Dissertation

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Submitted by

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CANDIDATE'S DECLARATION

I declare that the work presented in this dissertation with title, **"GaN HEMT Modeling and Radio Frequency Power Amplifier Design"** towards the fulfillment of the requirement for the award of the degree of **Integrated Dual Degree in Electronics and Communication Engineering** submitted in the **Dept. of Electronics and Communication Engineering, Indian Institute of Technology, Roorkee, India** is an authentic record of my own work carried out during the period **from May 2015 to May 2016** under the supervision of **Dr. Karun Rawat**, Assistant Professor, Dept. of ECE, IIT Roorkee.

The content of this dissertation has not been submitted by me for the award of any other degree of this or any other Institute.

DATE: ..... SIGNED: .....

PLACE: ..... (Samarth Saxena)

CERITIFICATE

This is to certify that the statement made by the candidate is correct to the best of my knowledge and belief.

DATE: ..... SIGNED: .....

PLACE: ..... (Dr. Karun Rawat)

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DEDICATION

Dedicated to the memory of my grandmother

Abstract

The increase in demand of wireless devices has put a greater importance on the RF front–end components. In particular, the power amplifier (PA) is the main power consuming component in any transmitter of wireless device. Therefore, improving the efficiency of the power amplifier is crucial to extend battery lifetime (e.g. on a satellite or on a mobile base station) and reduce power loss. This in turn has significant effects on the total cost of the transmitter. Rapid growth of communication standards has prompted the development of broadband PAs. These are useful in the context of backward compatibility of communication systems. These in turn reduce the deployment cost of large scale base transceivers stations with rapid changes in the wireless standards. They can be compatible with the upcoming as well as existing standards. Moreover, such PAs fin utility in software defined radio platform where a broadband front-end is required to provide a multi standard feature to the radio.

GaN technology has recently been growing in prominence due its high voltage capability. Development in laboratories and various device manufacturers has spurred the demand for accurate nonlinear models. The development of a large signal transistor model for a pHEMT based on simplified Angelov Model is reported. Nonlinear embedding technique is also presented which has a distinct advantage over the conventional load pull analysis.

The thesis also discusses Class-F mode of operation with the design of a high efficiency power amplifier working at 2 GHz. This is followed by broadband high efficiency PAs operating in continuous class-B/J mode of operation. A novel approach for engineering the extrinsic harmonic impedance which can be realizable using a passive foster circuit is proposed. This resulted in a power amplifier working between 1.3 GHz and 2.4 GHz with state-of-the-art performance. Both the designs were based on the nonlinear-embedded model. After using passive components to match the amplifier output, an investigation into matching the output using active circuit was also carried out. Second harmonic signal was injected externally using a frequency doubler to properly shape the waveforms at the drain. Preliminary results are encouraging and promising. This architecture leads to an improvement in both drain efficiency and fundamental output power across a band of 1.3-2.4 GHz.

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Introduction

Motivation

Systems and protocols for wireless communication are continuously evolving to enhance data rates and serve more users within the limited and overcrowded radio-frequency (RF) spectrum. Wide bandwidth voice and data communication have become ubiquitous with the explosive growth of the smartphone and tablet markets. New wireless standards are emerging to meet the ever increasing user capacity requirements. Long Term Evolution (LTE) and Worldwide Interoperability for Microwave Access (WiMAX) are few of such next generation wireless standards which are augmenting data throughput and network capacity.

However, the new standards have placed very challenging demands on the RF front-end specifications vis-à-vis bandwidth and power efficiency. A power amplifier (PA) is one of the most important components of front end RF and microwave systems. The battery lifetime as well as the overall size of the devices largely depends on the efficiency of the PA. However, there is a trade-off between the power efficiency and linearity of the PA. A system with high degree of nonlinearity leads to both inband signal distortion and outband spectral regrowth. This calls for wireless transmitter designers to design PAs with high bandwidth, linearity while respecting the market's need for higher throughput and lower power consumption.

Depending on the application a wide variety of realizations for PA are possible: solid-state amplifiers in mobile handsets, travelling wave tube amplifiers in satellites or even microwave heating tubes. Whatever the physical realization of PA may be, it is essentially a nonlinear system which increases the power level of the input signal to a desired output level in a specific frequency range. The selection of the active device for a PA is based on its power capabilities and small signal gain. The operating conditions can significantly affect the output signal and it becomes necessary to choose them intelligently. The design approach depends on the bandwidth, available device technology, application along with a host of other factors.

Objective

This thesis will be primarily aimed at investigating GaN-based PA architectures with high efficiency and bandwidth. A good and accurate nonlinear model is essential for commercial GaN devices. To reduce reliance on large signal models provided by the device manufacturer,

an accurate HEMT model should be developed. With a self-developed model it becomes easy to exploit the parameters of a device at the intrinsic planes. The major part of the thesis will be dedicated to novel designs of PA based on large-signal intrinsic transistor models. Investigations into multiple techniques to enhance the performance of the amplifier will be undertaken.

The organization of the thesis is as follows. Chapter 2 reviews the theoretical concepts of a PA. It discusses the fundamentals and presents an overview of the design flow. In chapter 3, a power HEMT model is developed. At the end, a nonlinear embedded model which provides access to the intrinsic drain and gate to designers is also presented. Class-F amplifier which can reach drain efficiencies over 80% is introduced in chapter 4. The design of a 2 GHz class-F PA is discussed in detail. Chapter 5 provides an insight into the newly proposed continuous mode of class-B/J PA. A new approach to make the output impedance rotate clock-wise on the smith chart is proposed. This is validated by a broadband PA designed for 1.3-2.4 GHz operation. Finally, chapter 6 investigates active matching techniques for broadband amplifiers especially second harmonic injection technique.

Chapter 1

Power Amplifier Overview

This section discussed the design flow of a RF power amplifier used in base station transmitters. The analysis lays the foundation for understanding the high efficiency PAs designed in subsequent chapters. Various classes of operation are discussed briefly along with their efficiency and gain considerations. The requirements for biasing, stability and matching are mentioned. In addition the effects of device parasitics and packages on the waveforms and load impedances are also presented. The significance of GaN HEMTs for designing amplifiers is touched upon.

PA design involves fulfilling several conflicting requirements. There is generally a trade-off between achieving high power efficiency (or output power) and linearity. The approach mainly depends on the operating frequency and bandwidth, application of the PA, available device technology, cost etc.

1.1 Power Amplifier Terms

Before delving deep into the theoretical aspects of a PA it is essential to get familiar with few basic parameters.

The **output power** P_{out} is the power delivered to the external load which is usually $50\,\Omega$.

$$P_{out} = \frac{1}{2}\mathrm{Re}\{V_{out} I_{out}^{*}\} \tag{1.1}$$

Similarly the **input power** P_{in} is the available input power to the device.

$$P_{in} = \frac{1}{2}\mathrm{Re}\{V_{in} I_{in}^{*}\} \tag{1.2}$$

The **power gain** G is defined as the ratio between output power and input power.

$$G = \frac{P_{out}}{P_{in}} \tag{1.3}$$

In logarithmic scale the power gain can be written as

$$G_{db} = 10\log(G) = P_{out,dBm} - P_{in,dBm} \tag{1.4}$$

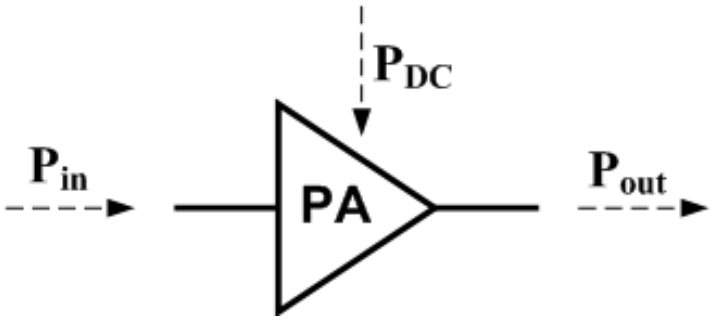


Fig 1.1: Basic representation of PA operation.

A PA being a non-linear device the output power does not increase linearly with the input power. This non-linearity is seen as input power is swept from low power levels to high power levels. The output power ceases to rise linearly after a certain value of input power. The near constant value of power gain (small-signal gain) starts decreasing beyond this point. This phenomenon is referred to as gain compression. A widely used figure-of-merit for this compression behaviour is 1dB compression point. It is defined as the output power level which corresponds to a 1dB deviation from the ideal linear behaviour of the PA.

To put it simply regardless of the specific application and configuration a PA can be regarded as a non-linear component converting the RF input power (P_{in}) to a required output power (P_{out}) level using the DC power supply (P_{DC}). Fig 1.1 depicts this process.

The effectiveness of this conversion process is measured in terms of the amplifier's efficiency, η, defined as the ratio of the output RF power to the supplied DC power:

$$\eta = \frac{P_{out}}{P_{DC}} \tag{1.5}$$

This efficiency is further classified as drain efficiency (η_d) or collector efficiency (η_c) for a field effect transistor and bipolar transistor respectively. A high efficiency device implies that the power dissipated within the active device is minimum. In other words, there is little overlap between the time domain voltage and current waveforms at the intrinsic drain of the FET. Therefore, suitably engineering the drain voltage and current waveforms leads to highly efficient PAs. This is further elaborated in Section 1.2.

At RF and microwave frequencies a significant portion of the output power comes directly from the input drive. Consequently, it is also important to know the added power i.e. the

increase in signal power from the input to the output of the PA. Therefore, a more intuitive parameter for PA designers is the Power-Added Efficiency (PAE). It is the ratio of the added RF power to the DC power supply:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}\left(1 - \frac{1}{G}\right)}{P_{DC}} = \eta\left(1 - \frac{1}{G}\right) \tag{1.6}$$

A designer tries to achieve as high PAE as possible under the operating conditions.

1.2 Class of Operation

Traditionally PAs are classified according to their bias point selection. These are Class A, AB, B or C. The quiescent bias points may be identified through conduction angle α which is essentially the RF signal period where a non-zero current is flowing. However, recent advancements in PA have given room to further classification based on output impedance harmonics (load matching topologies). These are Class F, F^{-1}, E.

1.2.1 Based on Biasing

1.2.1.1 Class A Amplifier

The class A amplifier [1] is biased half way between cutoff and saturation limits as shown in Fig 1.2. The slope of the load line of class A is determined by the fundamental load impedance presented to the device. For maximising the voltage swing and output power the optimal impedance Ropt is calculated as:

$$R_{opt} = \frac{1}{2}\frac{V_{dd}}{I_{\max}} \tag{1.7}$$

The corresponding maximum output power is given as:

$$P_{out} = \frac{1}{8}V_{\max}I_{\max} \tag{1.8}$$

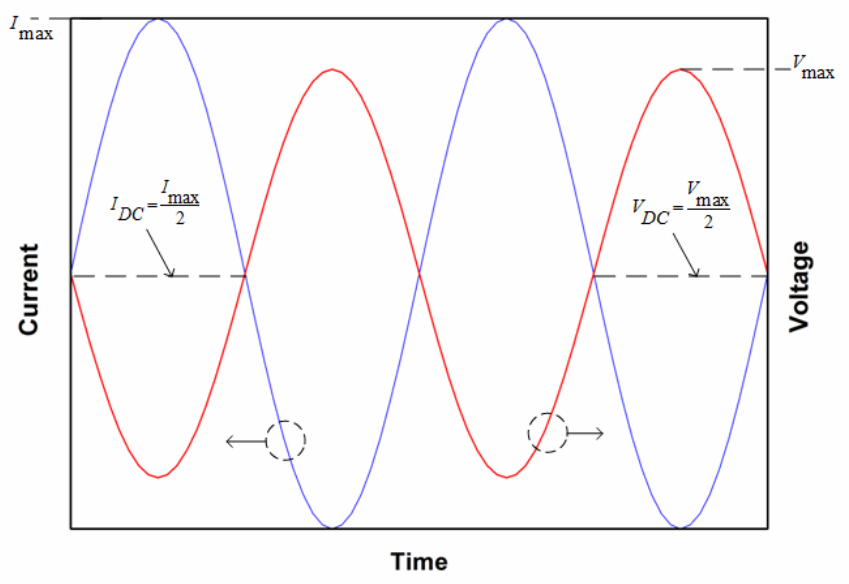


Fig 1.2: Ideal class-A waveform.

The drain current waveform I_{ds} as well as the drain voltage waveform V_{ds} are sinusoidal. The DC components are I_{DC} and V_{DC} respectively. The efficiency of class A is:

$$\eta_A = \frac{P_{out}}{P_{DC}} = \frac{\mathrm{Re}\left\{\frac{1}{2}V_{out}I_{out}^{*}\right\}}{V_{DC}I_{DC}} = \frac{1}{2}\frac{(V_{max}I_{max})/4}{(V_{max}I_{max})/4} = 50\% \qquad (1.9)$$

Class A has the advantage of high linearity and ease of implementation. But its efficiency is restricted to 50% because of its waveform characteristics. For applications which can tolerate a certain degree of nonlinearity it is better to choose other more efficient modes of operation.

1.2.1.2 Reduced Conduction Angle Modes- Class AB, B, C

To improve the drain efficiency of the PA over 50% the conduction angle of the device can be changed from 2π.

Table 1.1: Definition and efficiency of different classes of operation.

Class of operation	Conduction angle α	Peak drain efficiency η
Class A	$\alpha = 2\pi$	$\eta = 50\%$
Class AB	$\pi < \alpha < 2\pi$	$50\% < \eta < 78.5\%$
Class B	$\alpha = \pi$	$\eta = 78.5\%$
Class C	$\alpha < \pi$	$78.5\% < \eta < 100\%$

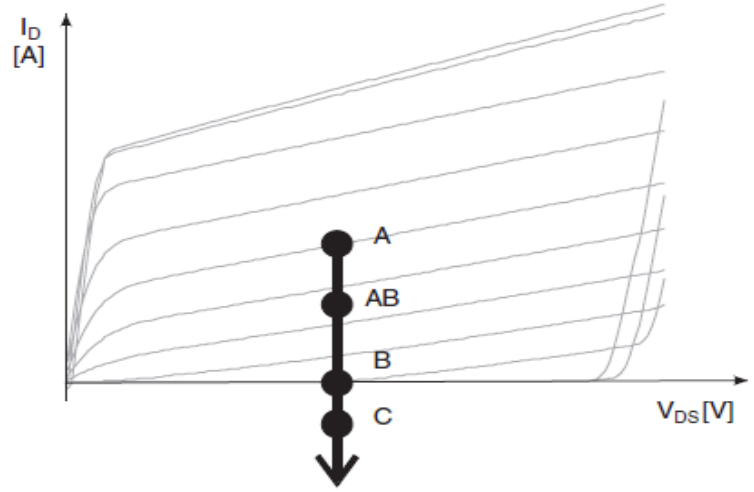


Fig 1.3 Classes of operation based on biasing of device [2].

Table 1.1 presents different operating modes based on the conduction angle α. As α reduced from 360° a portion of the input waveform dips below the threshold voltage into the non-conducting region as shown in Fig 1.3. Correspondingly only a portion of the waveform is converted to the output drain current. An analysis of the drain current will reveals that unlike class A drain voltage and current of these reduced modes contain higher harmonics also. Therefore, the efficiency will be a function of higher harmonic impedance as well. Classically "tuned load" contains no higher harmonics of the load impedance $Z_{n.}$ In other words they are shorted as:

$$Z_n = 0, \quad n \geq 2 \tag{1.10}$$

Under the "tuned load" conditions the drain voltage is purely sinusoidal. The resulting drain efficiencies are also tabulated in Table 1.1 assuming "tuned load" condition and maximum voltage swing.

These reduced conduction angle modes have improved efficiency at saturation as well as back-off power levels. It is seen that these modes consume less DC power under zero stimulus than class A consumes. However, there are certain nuances to these modes too. Increased drive requirements and reduced gain and a higher voltage swing can lead to breakdown of device. Linearity is also degraded.

1.2.2 Based on Harmonics

Class-AB,-B, -C contain harmonics only in the drain current. However, PAs working in class-F or –E mode contain the harmonic component in drain voltage or current or both. By driving the PA into saturation the required harmonics with optimum amplitudes can be generated. Fourier series analysis of the drain current and voltage explains that the maximum achievable efficiency is dependent more on the number of harmonics rather than on the class of operation. The same performance can be attained by properly setting the harmonics reactance and fundamental load reactance to engineer the drain waveforms. The nomenclature of these PAs is based on the relative magnitudes of even and odd harmonic impedances relative to the fundamental load. It goes as follows [3]:

- Class-F: the even harmonics reactance are low and odd-harmonic reactance is high. This shapes the drain voltage as a square wave and the drain current as half-sine.
- Inverse Class-F (ClassF^{-1}): as the name suggests the conditions are opposite to that of class-F. The even-harmonics reactance are high and odd-harmonics reactance are low so the drain current is a square wave while the drain voltage is half-sine wave.
- Class-E: all the harmonics reactance are negative and similar in magnitude to fundamental load resistance.

As elaborated in further chapters these classes of amplifiers have higher efficiency than achieved by simply choosing the biasing point. Class-F can theoretically achieve a maximum of 100% drain efficiency by increasing the fundamental voltage component. Class-F^{-1} does so by reducing the DC voltage component.

Although there is a clear increase in the efficiency of the harmonically tuned PAs compared to the conventionally biased PAs the precise harmonic requirements are difficult to synthesize and require advance matching and tuning techniques. Practical designs to increase efficiency result in non-linear characteristics. To counter this many linearization techniques are being used extensively such as digital pre-distortion (DPD).

1.3 Power Amplifier Design Flow

An accurate PA design involves nonlinear design tools and similarly an adequate nonlinear description of the active device, often represented in the form of an equivalent-circuit model.

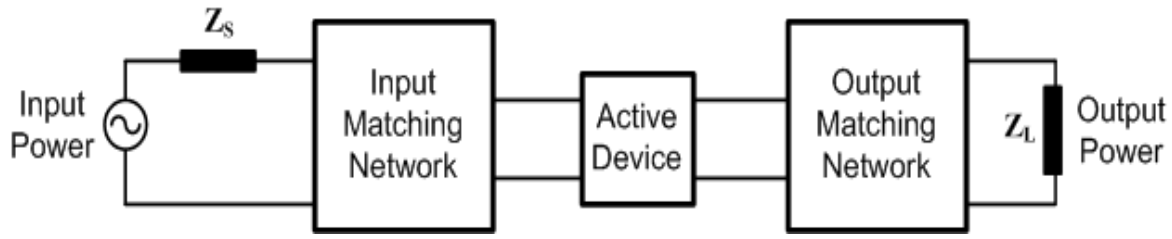


Fig 1.4: Major components of a RF PA.

Building on the theoretical aspects of biasing and efficiency the subsequent sections discusses the practical considerations in designing a power amplifier. The key components are depicted in Fig1.4. The design starts with identifying the requirements and application and frequency band the PA will be used for. This calls for a proper selection of technology and subsequent adoption of active device.

1.3.1 Device Technology Selection

Base stations typically use a hybrid circuit for their power amplifiers which consists of a packaged device with input and output matching networks fabricated on a suitable high frequency substrate. For this only study hybrid PAs will be discussed. Currently base stations employ LDMOS as a dominant technology. But over the years GaN high electron mobility transistor (HEMT) has been emerging as a viable option [4]-[8]. Due to a significantly high bandgap energy and breakdown field intensity the operating voltages reach upto 48V and breakdown voltages up to 80 V. The higher voltage handling capability move the optimum load resistance R_{opt} closer to 50 Ω and makes it easier to match. GaN also has the capability to generate output power density as high as 5-12 W/mm, compared with about 1.5 W/mm for GaAs, which leads to multi watt generation of power from a smaller device. This is particularly suitable for base stations. Lastly due to electron mobility of around 1500 $cm^2/V/s$ GaN devices can operate well in to gigahertz range. In view of these advantages the current work uses GaN devices from CREE Inc. to design PAs. Despite these advantages, GaN HEMT still is an expensive option and thermal dissipation quite often limits its performance.

To protect the bare die from environment conditions and heat dissipation devices are generally protected by a package around it. A flange is soldered to the die and the drain and gate leads are connected via bond wires. It is essential to model these as lumped or distributed elements to account for parasitic loss in these wires and bond-pads. These along

with intrinsic nonlinear capacitances shift the reference plane of interest from the intrinsic drain to the package plane. Their presence narrows down the bandwidth of operation and introduces frequency dispersion effects. It is important to know the matching requirements at the package plane to design an efficient PA. Further analysis of the device requires a deep knowledge of the large signal model of the device provided by the foundries. A deeper insight is provided in the following chapter where the HEMT is modelled from scratch.

1.3.2 Biasing

The drain and gate of the transistor are biased using DC voltages supplied through a bias network. The bias network consists of few decoupling capacitors to reduce any ripple in the supply. A RF choke is located between the device and the bias. This prevents leakage of any fundamental signal into the DC bias and therefore ensuring that the device is not loaded. A large inductor or a quarter-wave transmission line centred at fundamental frequency can act as the RF choke. A quarter-wave line can even act as a low impedance for second harmonic. To prevent DC leaking into the main load DC-blocking capacitance can be placed at the output (and the input).

1.3.3 Stability

This is an extremely vital step in designing a PA or any non-linear device. The device stability is analysed to prevent any small signal oscillations. There is a widely accepted test for determining the stability known as the K-Δ test. The requirement for unconditional stability is given as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{1.11}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{1.12}$$

The large signal S-parameters are a function of the frequency and input drive for any active device. Therefore, the above test is performed from DC to high operating frequency.

A simple solution to make the device stable is to add a parallel circuit of resistor and capacitor in series with the input line next to the gate. This configuration reduces the positive gain of the device without affecting the RF performance a lot. If, however, the amplifier

cannot be made unconditionally stable, stability circle analysis is performed. This can ensure the loading and input impedance to fall within stable regions on a smith chart.

1.3.4 Load Pull and Source Pull Techniques

Load-and source-pull are empirical methods applied at the output and input of the device respectively. The fundamental and the harmonic impedances at the package plane are arbitrarily swept until the PA reaches a prescribed level of efficiency and output power for a given set of biasing and frequency conditions. Nonlinear simulators such as Keysight's Advanced Design System (ADS) report the results as efficiency and output contours on smith chart. These contours turn out to be non-circular because current and voltage limits arise due to non-resistive terminations.

This is a kind of brute force approach which has been widely used to design PAs. However, it does not give any information of the intrinsic waveforms achieved for a given efficiency and output power. It might be possible that a particular impedance solution may yield voltages higher than the breakdown voltages thus compromising on the device reliability. It is a common practice of foundries to keep device parasitics and package model as their own propriety. In the absence of an accurate open source model researchers have designed de-embedding models which transform the impedances from the package reference plane (obtained from loadpull) to intrinsic drain reference plane. Recently, there has also been a rise in interest in embedding techniques which provides access to intrinsic as well as the extrinsic drain and gate nodes to a designer. This circumvents the need to go for cumbersome load pull and source pull techniques and subsequent de-embedding to the current source plane.

1.3.5 Output Matching Network

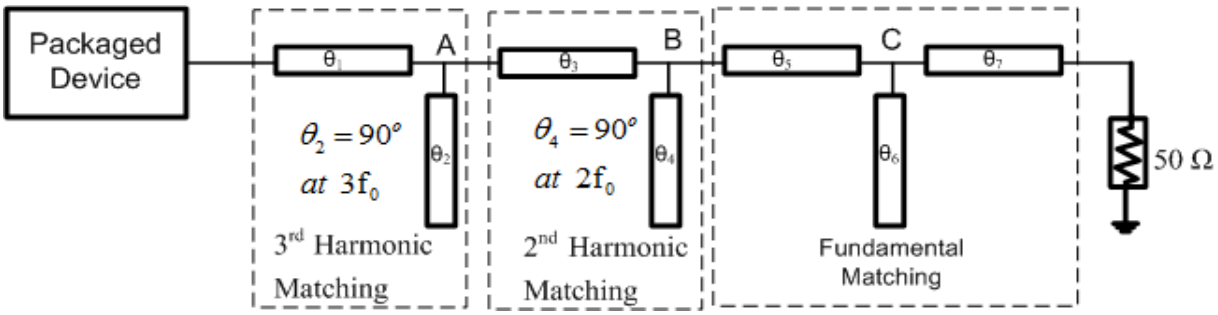


Fig 1.5: Multi-harmonic matching network.

With the impedance known at the package reference plane at the output, it is required to match these to the 50Ω reference output terminal. Theoretical aspects of single frequency impedance matching are well documented in literature [9], [10]. Care should be taken to mitigate the efficiency and output power loss due to substrate dielectric and low quality-factor components. Quite often it is difficult to achieve the exact matching network impedances as required by the device. The degradation of performance is dependent on the amplifier sensitivity to mismatch. Finally, before sending the design for fabrication a designer needs to evaluate tolerances for the dielectric constant and any fabrication error.

As discussed earlier certain modes of PA require proper harmonics to reach high efficiency. This can be achieved to by suitably providing harmonic terminations at the intrinsic drain of the device. If the device parasitics are assumed to be lossless the corresponding impedances get transformed to purely reactive impedances at the parasitic plane. Fig 1.5 depicts how the fundamental, the second harmonic and the third harmonic are matched independently. Harmonic beyond third are hardly controlled because of added complexity. As seen in the schematic open circuited stubs are used. The open stub with θ_3=90° at $3f_0$ creates a short at node B. This in parallel with the circuit to the right of node B removes the latter's effect at $3f_0$. The length of series line θ_1 is chosen to match the calculated reactance at the package plane at third harmonic. Next the process is repeated for second harmonic. The third harmonic matching between nodes A and B appears as a phase shift which the length of line corresponding to θ_3 can incorporate. Finally, the fundamental load is matched to 50 Ω such that the drain sees the required fundamental load at node A. This completes the multi harmonic load matching network. Quite often it is convenient to include the biasing network as a part of the harmonic matching impedance.

1.3.6 Input Matching

The input impedance most notably affects the gain of the amplifier. At RF frequency the input impedance is complex and its magnitude is very low. The device is driven by a RF voltage source V_s with 50Ω source impedance. The small input impedance of the device results in the power available to the device to be only a fraction of V_s. The solution is putting in place a matching network between the device input and the RF source. The input impedance Z_{in} can be modelled as a series combination of resistance R_{in} and capacitance C_{in}:

$$Z_{in} = R_{in} + \frac{1}{j\omega C_{in}} = R_{in} - jX_{in} \tag{1.13}$$

To maximize the input voltage V_{in} the device input is terminated with a complex conjugate of Z_{in}. In other words Z_{in} is matched to 50Ω. This maximizes the power transferred to the device as per the maximum power transfer rule. Under this condition the power available from source P_{avs} is:

$$P_{avs} = \frac{V_s^2}{8R_s} \tag{1.14}$$

GaN typically has smaller input capacitance and can therefore achieve higher gain and PAE than other common device technologies.

Chapter 2
GaN HEMT Modeling

2.1 Nonlinear Device Models

A comprehensive model for a device needs both the strong and weak nonlinear behaviour to be characterized. These nonlinearity traits arise from various aspects of the device physics. A device modeler needs to face these challenges.

There are three general categories of modelling for CAD applications [1]:

1. Physical models
2. Equivalent circuit models
3. Behavioral models

Physical models consist of a “bottom-up” approach for device physics and fabrication geometries. They use a nonlinear model of the active device and of other passive components.

An equivalent circuit description of the PA uses analogous circuit elements for the device physics effects. Many a times the elements are included to better fit the measured data rather than having a physical counterpart. Most CAD model devices use this model.

Behavioral model refers to a higher level mathematical representation of the amplifier system. It deals in the terminal properties rather than minute internal details.

Scaling is the central issue in modeling an RF power transistor. Detailed modeling is done on a much smaller sample device than the device used. These models are quite accurate. Large device will display a range of secondary phenomena such as non-uniform thermal effects and low impedances generated.

Although modeling is an important component in today’s research certain individuals or groups who have successfully modeled PA products are not always keen to make their results public. A foundry customer may get access to good CAD models, but packaged transistors are poorly represented many a time in commercial model databases. This necessitates the use of models personally developed.

As GaN technology is developing, in laboratories and more recently among device manufacturers, the demand has grown for improved nonlinear models. Need for an improved model is twofold:

1. Unique nuances of GaN devices such as trapping effects need to be addressed
2. Improved accuracy in GaN HEMT models can lead to performance wins in the areas of high efficiency and high-power operation.

2.2 Model Selection

A large signal model for PA design should be accurate for all operating conditions. Ease of extraction of model parameters and simplicity of model are required. Multiple models for MESFET and HEMT are available with varying complexity but different models are considered accurate for different applications. Curtice's model [11], [12], Triquant's own model (TOM) and cubic model are a few of them. Despite their usefulness for PA design they are unable to quantify the thermal effects arising in the devices due to self-heating of transistor. A sufficiently accurate model for eletrothermal effects is Angelov model [13]-[16] which is suitable for pHEMTs operating at high power levels. A schematic for simplified Angelov model which is used in this work is depicted in Fig 2.1. To keep the number of parameters small a symmetrical device was assumed. This simplified capacitance functions. Trapping effects of gate and drain were also omitted due to a lack of suitable measurement data.

The standard drain current is described by a hyperbolic function as:

$$I_{DS} = I_{pk}\left(1+\tanh\psi\right)\tanh\left(\alpha V_{DS}\right)\left(1+\lambda V_{DS}\right) \tag{2.1}$$

Where, I_{pk} is the drain current measured at maximum transconductance, α is saturation voltage parameter and λ is the channel length modulation parameter. ψ is a power-series function related to V_{pk} and gate bias voltage V_{gs} as:

$$\psi = P_1\left(V_{GS}-V_{pk}\right)+P_2\left(V_{GS}-V_{pk}\right)^2+P_3\left(V_{GS}-V_{pk}\right)^3+\ldots \tag{2.2}$$

V_{pk} is the gate voltage at maximum transconductance $g_{mpk.}$ P_1, P_2 and P_3 are coefficients to be determined. ψ is usually truncated to the first three terms.

The thermal equivalent circuit is a single pole RC network. It is modelled as a current source which produces current equal to the resistive power dissipated throughout the transistor. The

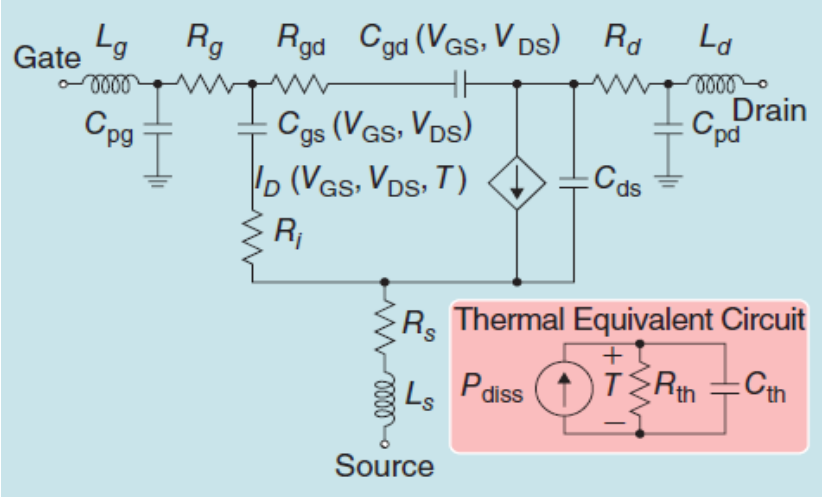


Fig 2.1: Schematic of simplified Angelov Model [17].

resistor R_{th} and capacitor C_{th} represent the thermal resistance and heat capacity of the transistor. The rise in temperature is equal in magnitude to the voltage drop created across the parallel combination of R_{th} and C_{th}.

Intrinsic device capacitances C_{gs} and C_{ds} are also modelled using hyperbolic functions. These are described as:

$$C_{gs} = C_{gsp} + C_{gs0}\left(1+\tanh\left(P_{10} + P_{11}V_{gs} + P_{111}V_{ds}\right)\right)\left(1+\tanh\left(P_{20} + P_{21}V_{gs}\right)\right) \quad (2.3)$$

$$C_{gd} = C_{gdp} + C_{gd0}\left(1+\tanh\left(P_{30} - P_{31}V_{ds}\right)\right)\left(1+\tanh\left(P_{40} + P_{41}V_{gd} - P_{111}V_{ds}\right) + 2P_{111}\right) \quad (2.4)$$

P_{10}, P_{20}, P_{30}, P_{40}, P_{11}, P_{21}, P_{31}, P_{41} and P_{111} are appropriate fitting parameters.

This work develops a large signal model for a power microwave HEMT with gate periphery of 0.3 mm from WIN Semiconductors. The measurement data was taken from an online source. The equivalent circuit model was developed in Keysight's ADS and MATLAB from MathWorks was used for parametric extraction and optimisation.

The entire modeling process can be broadly divided into four steps:

1. Extrinsic model extraction
2. Transistor DC I-V characteristics
3. Small-signal model extraction
4. Large-signal verification

2.3 Extrinsic Parameter Extraction

Extrinsic parameters of the model are essentially bias independent. The methodology for extracting the resistors, capacitors and inductors is well documented in the work proposed in [18]-[20]. The first step uses the S-parameters of the transistor at pinch–off (V_{gs}=-2 V, V_{ds}=0 V) and zero bias (V_{ds}=0 V=V_{gs}). At pinch-off, the channel of the transistor is represented by a capacitor. While, at zero bias the channel is modeled by a resistance. All the extrinsic parameters, namely L_g, L_s, L_d, R_g, R_s, R_d, C_{pg} and C_{pd} remain same in both the circuits being bias-independent. These arise due to the packaging pads and bonding wires after the die. The shunt elements (C_{pg} and C_{pd}) are determined from the Y-parameters. Removing their effect, the remaining linear parasitic are calculated. The series parasitics L_g, L_s, L_d, R_g, R_s, and R_d are calculated then by converting the S-parameters to corresponding Z-parameters.

Equations (2.1)-(2.4) give only a good initial estimate for the parameters. To refine the fitting the optimization in ADS is used. The values of the ascertained extrinsic parasitics are mentioned in Table 2.1. Comparison of the measured and modelled S-parameters is performed in Fig 2.4. It shows reasonably well matching.

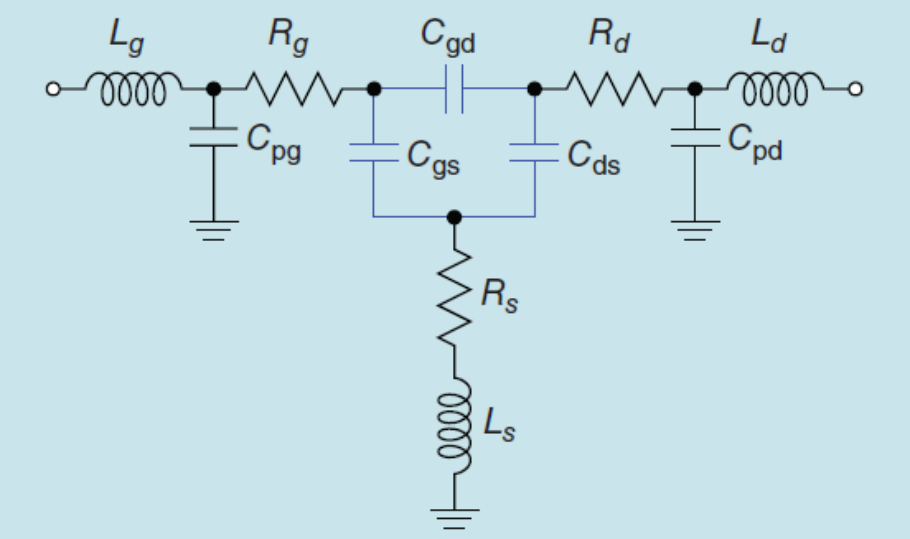


Fig 2.2: Equivalent circuit for determining extrinsic parameters at pinch-off [17].

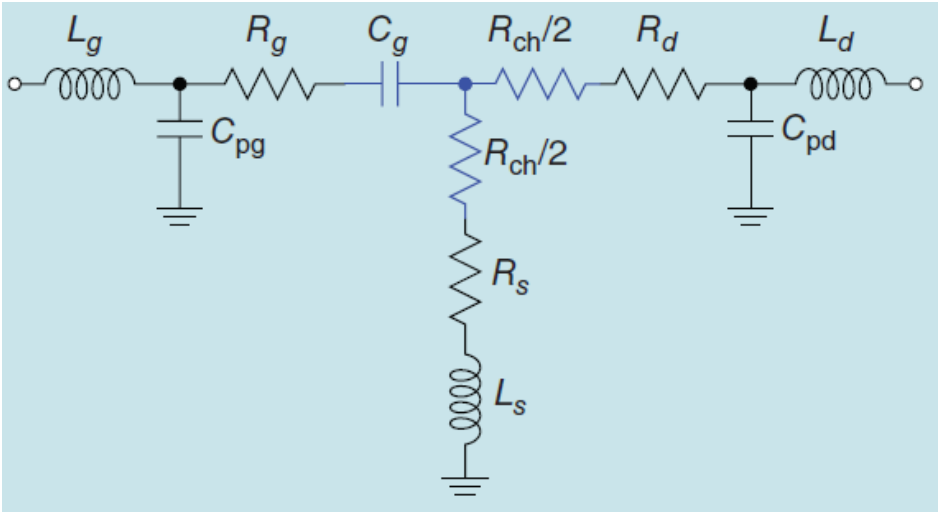


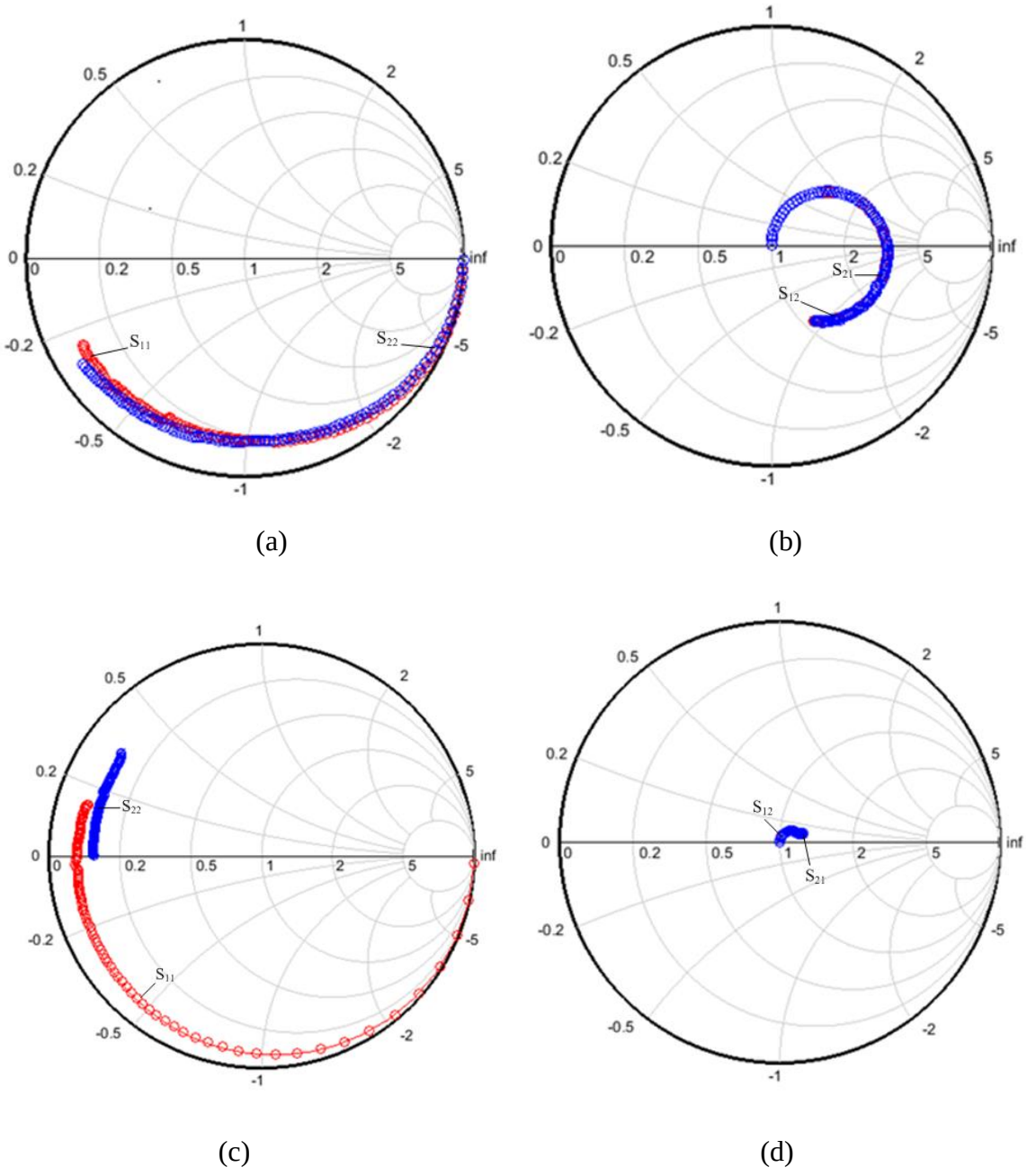
Fig 2.3: Equivalent circuit for determining extrinsic parameters at zero bias [22].

Table 2.1: Extracted values of extrinsic parameters.

$R_g(\Omega)$	$R_s(\Omega)$	$R_d(\Omega)$	L_g(nH)	L_s(nH)	L_d(nH)	C_{pg}(fF)	C_{pd}(fF)
0.98	**0.98**	**0.52**	**0.033**	**0.008**	**0.043**	**9.37**	**12.24**

2.4 DC I-V Characterization

DC characteristics are one of the most important metric for HEMT's performance. Many basic coefficients of the DC-IV can be determined by simply analysing the measured data of I-V and g_m curves [21]-[23]. P_1 in equation (2.1) is simply the ratio of the peak transconductance g_{mpk} to I_{pk} of the same equation. λ can be calculated as the slope of the DC I-V curve at high V_{ds} and small I_{ds}. Many of these parameters are estimated without fitting through optimization. Temperature dependence of the device is another crucial element in high power devices. I-V measurements were available for three temperatures: $25℃, 85℃, 125℃$ and therefore the negative slope of I-V characteristic at high current and voltages due to self-heating can be modeled. R_{th} is estimated by examining the relation between total power dissipated and change in drain current on static I-V curves. Although C_{th} is ascertained using time constant of step response data of drain current, it was guesstimated and optimized due to a lack of such measurements. The calculated values of all the relevant parameters have been tabulated in Table 2.2. The resulting modeled DC I-V curves is plotted in Fig 2.5 (a) and compared with the measured data in Fig 2.5 (b). The model is in good agreement with the measured data.



(a) (b)

(c) (d)

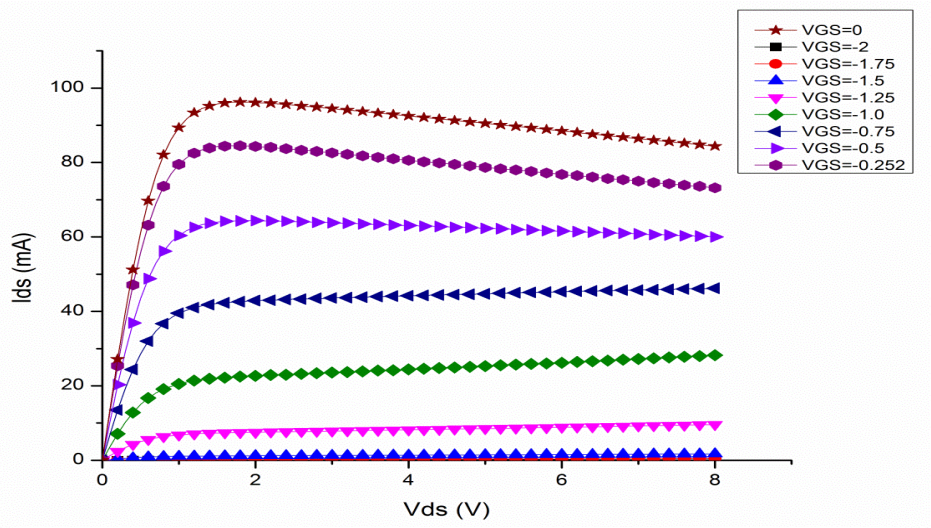
Fig 2.4: Measured (circles) and modelled (lines) S-parameters for different biasing conditions. (a) S_{11} and S_{22} at pinch-off, (b) S_{12} and S_{21} at pinch-off, (c) S_{11} and S_{22} zero-bias and (d) S_{12} and S_{21} at zero-bias.

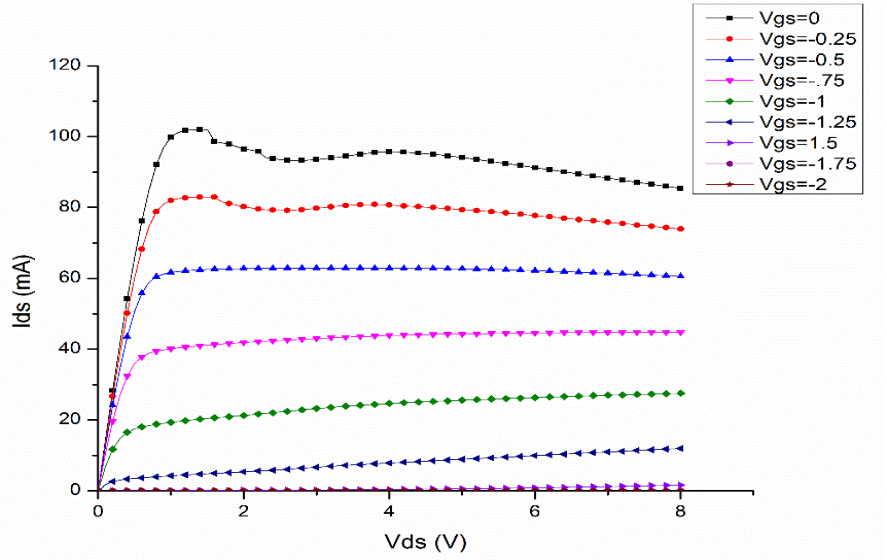
However, the kinks in the measured curves at higher drain currents cannot be modelled by simplified Angelov model.

Table 2.2: Extracted values of coefficients of drain equation.

P1	P2	P3	α	λ	I_{pk} (mA)	V_{pk} (V)
2.08	0.593	1.93	1.73	0.025	0.051	-0.7

(a)





(b)

Fig 2.5: (a) Measured and (b) modeled DC I-V chareteristics.

2.5 Small Signal Behaviour

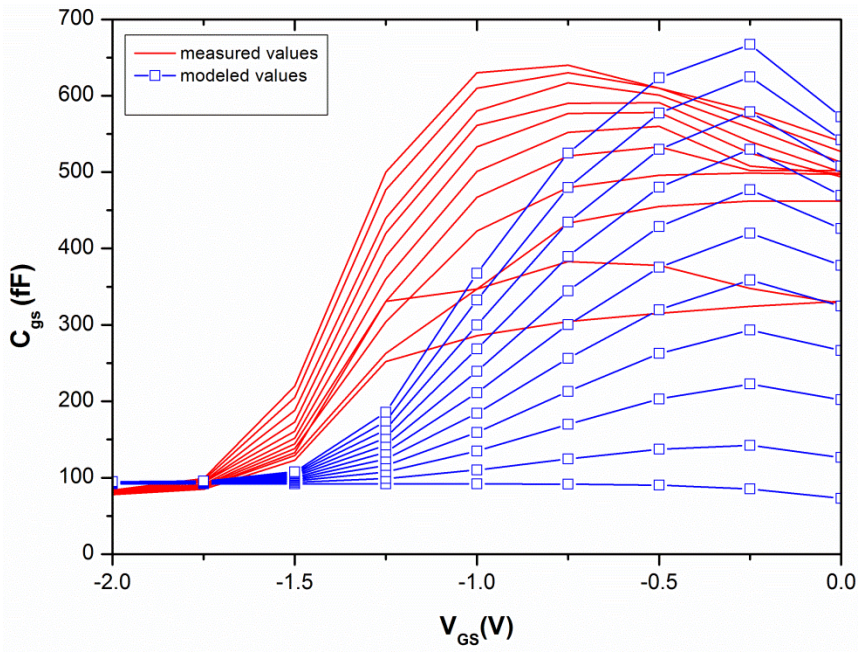
Small signal analysis deals with the extraction of bias-dependant intrinsic parameters. The procedure is well established in works by [18]-[20] and relies on the transistor's Z- and Y-parameters. The capacitances were modeled in accordance with equations (2.3) and (2.4). Extracting the capacitances from the measured S-parameters and modeling their non-linear behaviour was considered to be the most challenging part of the entire modelling process [22]-[24]. And the fit is not extremely accurate on as shown in Fig 2.6. There is still room for improvement here.

Table 2.3: Extracted values of coefficients for gate-source capacitance (C_{gs}).

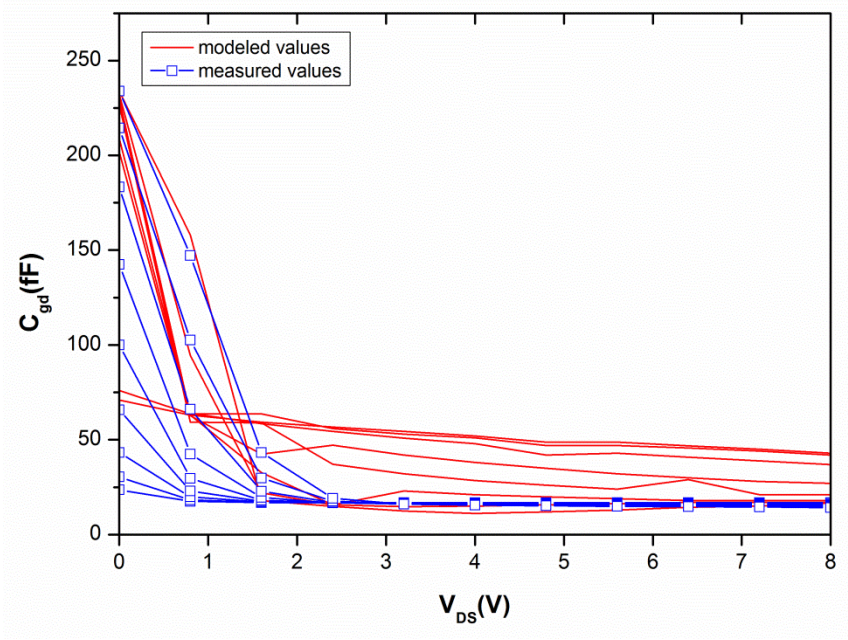
C_{gsp}(fF)	C_{gs0}(fF)	P_{10}	P_{11}	P_{20}	P_{21}	P_{111}
35	**15**	**0.336**	**-2.7**	**1.5**	**0.273**	**-0.03**

Table 2.4: Extracted values of coefficients for gate-drain capacitance (C_{gd}).

C_{gdp}(fF)	C_{gd0}(fF)	P_{30}	P_{31}	P_{40}	P_{41}	P_{111}
24	**60.9**	**2**	**0**	**1.14**	**1.45**	**-0.03**



(a)

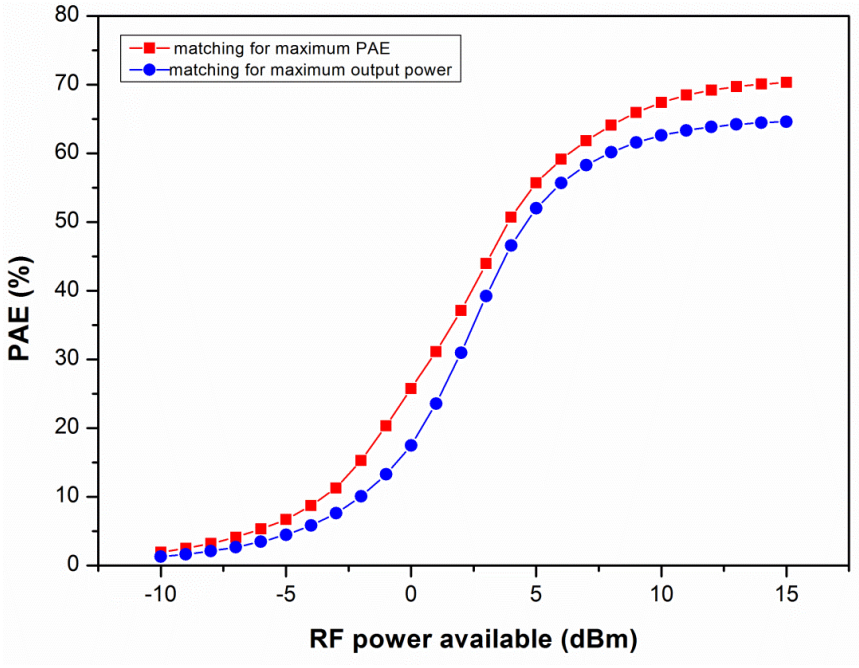


(b)

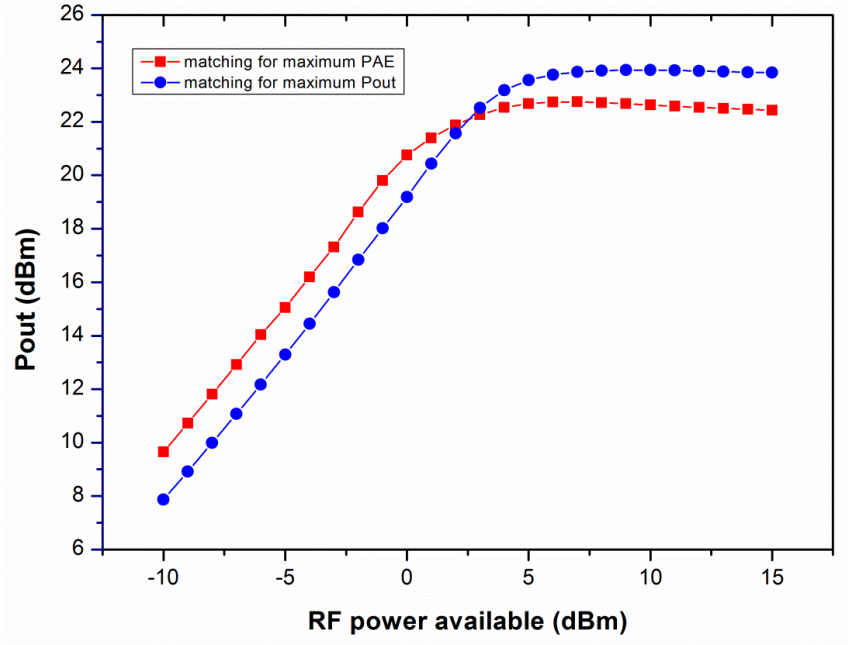
Fig 2.6: Measured (red lines) and modeld (blue lines with squares) capacitances for various bias points.(a) C_{gs} and (b) $C_{gd.}$

2.6 Large Signal Operation

This is the last step and is important to measure the performance of the modeled transistor. A bias point was chosen as 8V drain voltage and 30mA drain current. Harmonic balance



(a)



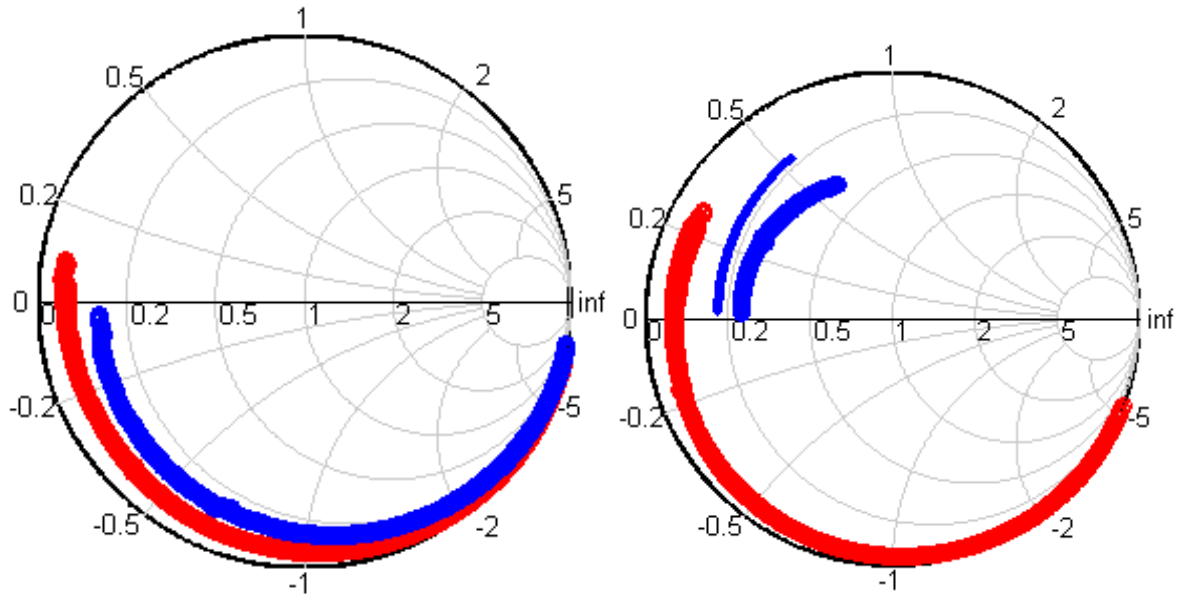
(b)

Fig 2.7: Modeled (a) PAE and (b) output power of the device for two different biasing conditions.

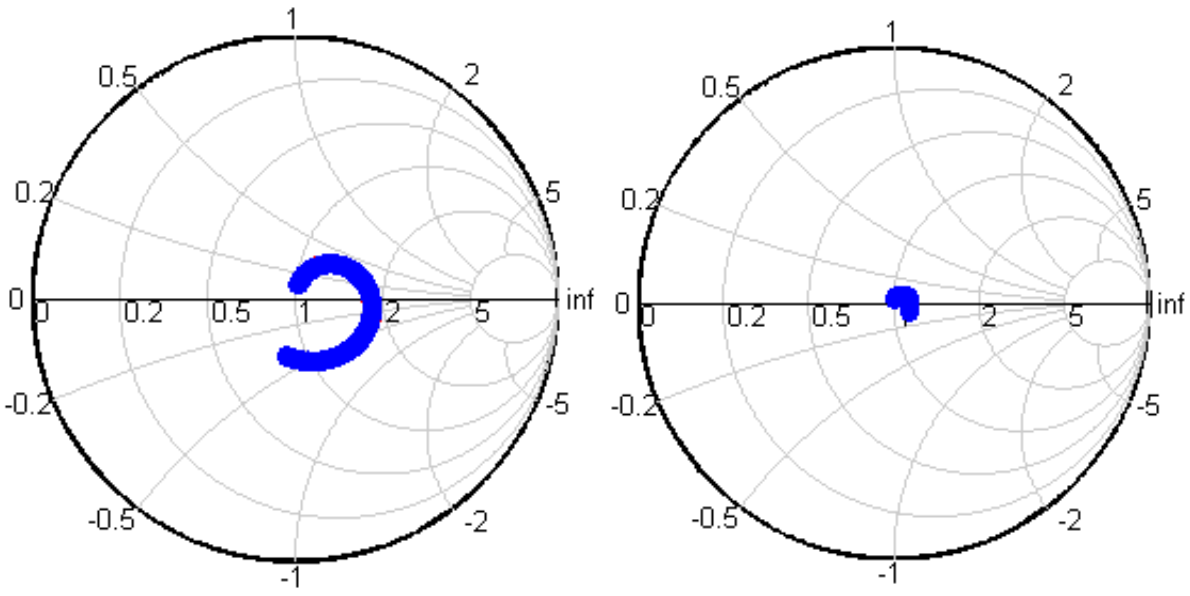
simulations were carried out in ADS to plot the maximum PAE and output power with two different loading conditions namely, for maximum PAE and maximum output power.

Harmonics were neglected at this stage and results were obtained for 3.5 GHz. Figure 2.7 show these results. The device reaches saturation at about 7 dBm. The PAE and the output power reach 67% and 23.9 dBm respectively at saturation.

Apart from the previous pHEMT, modeling was carried out for another device namely, 0.25 μm GaN HEMT from WIN Semiconductors. Modeling started with the extraction of extrinsic parameters like explained in the previous section. The measured and modeled data at pinch-off and zero-bias conditions is compared in Fig 2.8. Due to a large number of data the measured and modeled values are overlapping. It shows a good fit for all the values except for S_{21} at pinch-off.



(a) (b)



(c) (d)

Fig 2.8: Measured (circles) and modelled (lines) S-parameters for different biasing conditions for GaN HEMT. (a) S_{11} and S_{22} at pinch-off, (b) S_{12} and S_{21} at pinch-off, (c) S_{11} and S_{22} zero-bias and (d) S_{12} and S_{21} at zero-bias.

Due to lack of sufficient DC I-V data at different voltage biases, an extensive DC I-V characterization including thermal model could not be developed. This prevented the development of a complete large signal model.

The previous sections described a brief overview of modeling a HEMT. Although refinement is still possible in the final model, a capability in modeling of HEMTs was established. Methodology for fitting the data and finer optimization was discussed for a simplified Angelov model. The purpose was to model a 15 W GaN HEMT and use this self-developed model to design power amplifiers. Modeling of this device is similar to the one described before. However, due to lack of adequate resources there was a lack of relevant and reliable measurement data. This eluded the author from building his own device model. Instead the focus shifted on another 15 W nonlinear-embedded model [25] developed recently.

2.7 Nonlinear-Embedded Model

To design the actual PA circuit it is essential to know the correct impedances at the

measurement plane. Waveforms and impedances at these planes are distorted by both linear and nonlinear parasitic elements of the device. The conventional approach relies on load-and source-pull measurements for optimal external load locations and later de-embedding the data based on a suitable device model available to reach the internal reference plane. As reported in [25] a nonlinear-embedding device model has been implemented for designing PAs based on the Angelov model for GaN HEMT. The design starts at the current-source intrinsic plane and the model predicts the extrinsic load terminations. This systematic approach gives a greater control and insight to the designer about the intrinsic loadlines and waveforms. The schematic of such a model is drawn in Fig 2.8. It is refered to as embedding transfer network (ETN). The current reference plane includes the intrinsic drain current source, the propagation delay τ and the thermal network. The branch currents through the non-linear and linear parasitic elements and the node voltages are then calculated through the ETN. This non-linear embedding is carried out through several dispersive sub-circuits of the model as shown in Fig 2.9 implementing Angelov's non-linear device model.

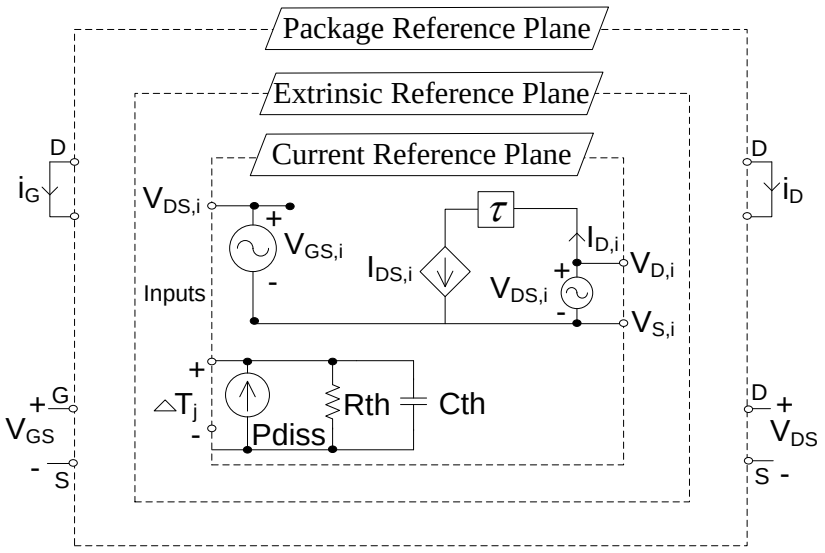


Fig 2.8: Layout of embedding transfer network (ETN).

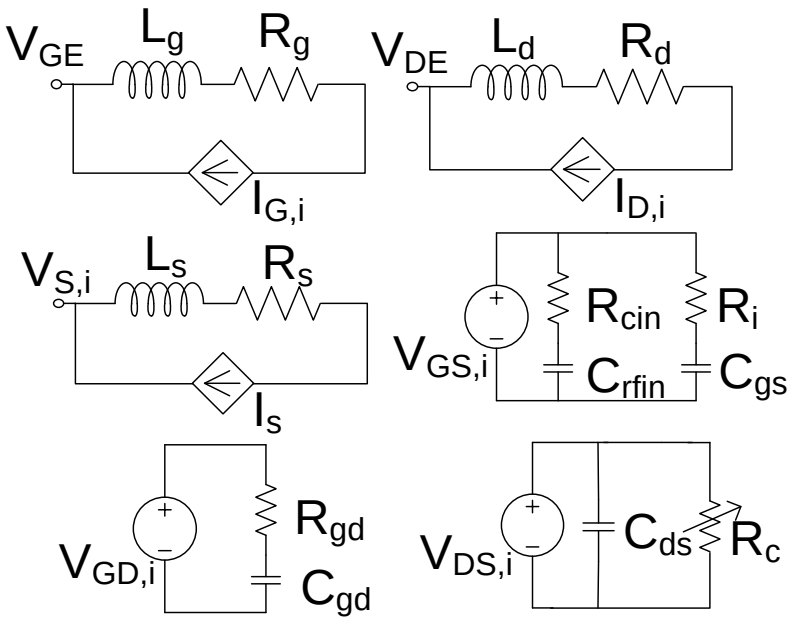


Fig 2.9: ETN sub circuits for mode projection.

Gate and drain voltages are selected by the designer so as to maintain the required class of operation at the intrinsic plane. The harmonics are selected in order to match the intrinsic waveforms as close as possible to the ideal waveforms. Once the internal settings are complete the external multiharmonic currents and voltages are computed in one direct step using the embedding model considering all the device parasitics and frequency dependent impedances. These external currents and voltages are utilized in predicting the external impedances to sustain the desired class of operation as [26]:

$$Z_L(nf) = -\frac{V_{ds}^e(nf)}{I_{ds}^e(nf)} \tag{2.5}$$

where n is the harmonic index, $V_{ds}^e(nf)$ and $I_{ds}^e(nf)$ are the drain voltage and current predicted at the respective external harmonic terminations. This relatively simple method excludes the lengthy load pull techniques employed.

Chapter 3

Class-F Power Amplifier Design

3.1 Class-F Theory

Improving the efficiency of the conventional class-A power amplifier can be achieved by engineering the drain waveform of current and voltage. The combination of the harmonics is such so as to produce a non-overlapping drain waveforms. Fig3.1 illustrates the waveforms for an ideal class-F amplifier. It is biased in class-B but the efficiency improvement occurs due to the shaping of the waveforms. The drain current is a rectified half wave sine wave and the voltage a square wave.

The half sinusoid drain current and square wave of voltage can be expressed as a series of Fourier terms as follows [1]:

$$i(\omega t) = I_{\max}\left(\frac{1}{\pi} + \frac{1}{2}\sin\omega t - \frac{2}{\pi}\sum_{n=2,4,6\ldots}^{N}\frac{\cos n\omega t}{n^2-1}\right) \tag{3.1}$$

$$v(\omega t) = V_{\max}\left(\frac{1}{2} + \frac{2}{\pi}\sin\omega t + \frac{2}{\pi}\sum_{n=3,5,7\ldots}^{N}\frac{\sin n\omega t}{n}\right) \tag{3.2}$$

where I_0 and V_0 are the current and voltage DC components, respectively.

The maximum efficiency of class-F can be determined by selecting the fundamental components from both the equations as:

$$\eta_F = \frac{P_1}{P_{dc}} = \frac{1}{2}\frac{(I_{\max}/2)(2V_{\max}/\pi)}{(I_{\max}/\pi)(V_{\max}/2)} = 100\% \tag{3.3}$$

Class-F is extremely efficient in converting the DC to RF output by eliminating the power dissipation within the device. The above analysis, however, assumes the inclusion of all the infinite higher harmonics in shaping the waveform. In practice harmonics up to third are only controlled to have a satisfactory complexity level for designers. In fact inclusion of higher harmonics does not yield a significantly increased efficiency.

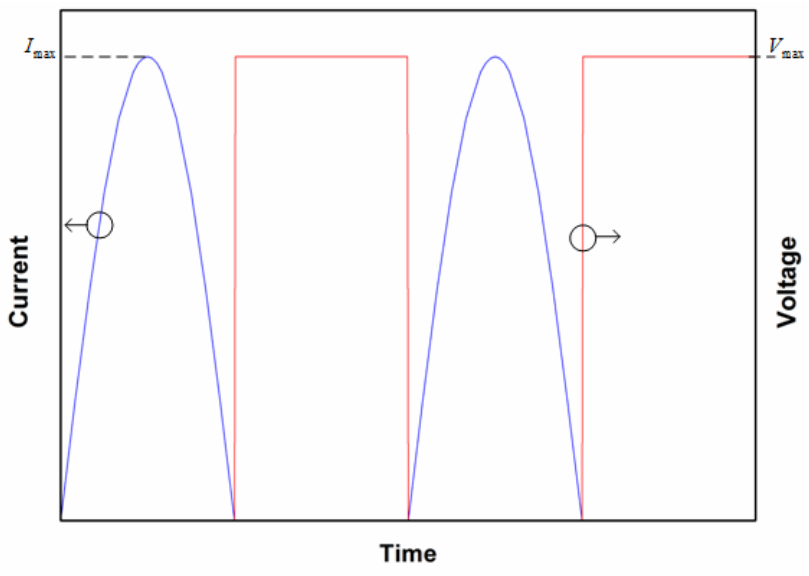


Fig 3.1: Ideal class-F waveforms.

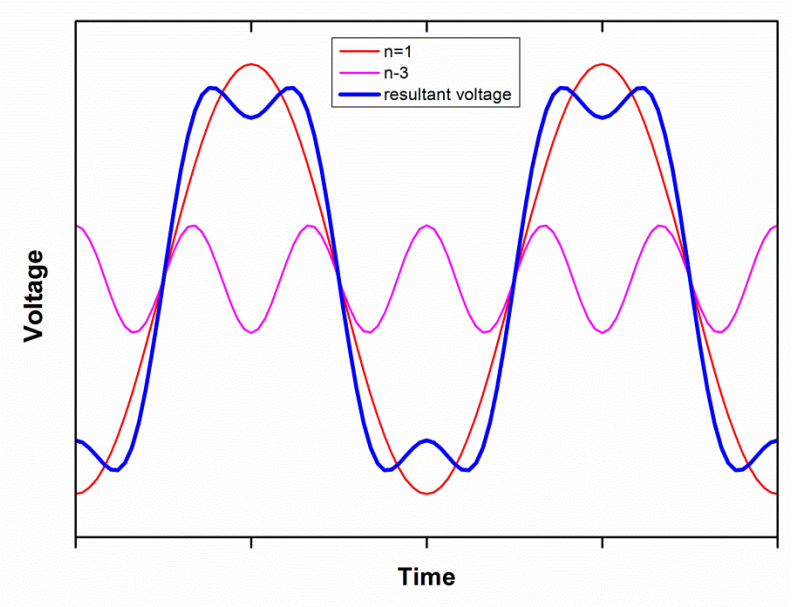


Fig 3.2: Class-F voltage as a resultant of fundamental and third harmonic only.

For voltage consisting only till third harmonics the equation becomes:

$$V(\theta) = V_1 \cos(\theta) - V_3 \cos(3\theta) \tag{3.4}$$

The DC component remaining constant, the higher fundamental component increases the drain efficiency to 90.7%. Fig 3.2 shows how the class-F voltage is shaped by the fundamental and third harmonic. By including higher odd harmonics in to the voltage waveform, the efficiency can be shown to increase.

It is interesting to understand how the odd harmonics are generated in a device to shape a square wave voltage. The knee region plays an important part here. Class-B has a half wave rectified sine wave like the class-F. And it is an appropriate starting point while biasing the device. But the half-wave rectified sine does not contain any odd harmonics which can be used to shape the voltage. A solution proposed in [3] biases the amplifier in class-AB which can include the required out of phase odd harmonic components. But the PA will lose out on efficiency and linearity.

To preserve the shape of drain current a better alternative is to exploit the odd harmonics generated when the voltage jumps below the knee voltage. This can be achieved by increasing the fundamental impedance Z_1 from that of class-B [27]. Next the third harmonic component Z_3 is increased. The voltage flattens and gradually less of it dips below the knee region and the current distortion starts ceasing. The limiting case of $Z_3 = \infty$, the current waveform fully restores to a rectified sine wave and voltage no longer dips below the knee voltage. Comparing the performance of class-F and class-B amplifiers it is seen that class-F weighs better in terms of efficiency but lags behind in linearity. Without going into complex Fourier analysis of the current and voltage it is enough to ensure the following conditions for harmonic impedances in order to sustain class-F mode of operation:

$$Z_n = \infty, \qquad n = 3,5,7... \tag{3.5}$$

$$Z_n = 0, \qquad n = 2,4,6... \tag{3.6}$$

3.2 Design and Validation: A 2 GHz 15 W GaN Power Amplifier

This section outlines the design of a 15W high efficiency power amplifier designed in class-F mode of operation. The results were presented at Applied Electromagnetics Conference (AEMC) 2015. The device used was a 15W CGH27015F from CREE Inc. The device model used was a nonlinear embedded model discussed in Section 2.7 which provided

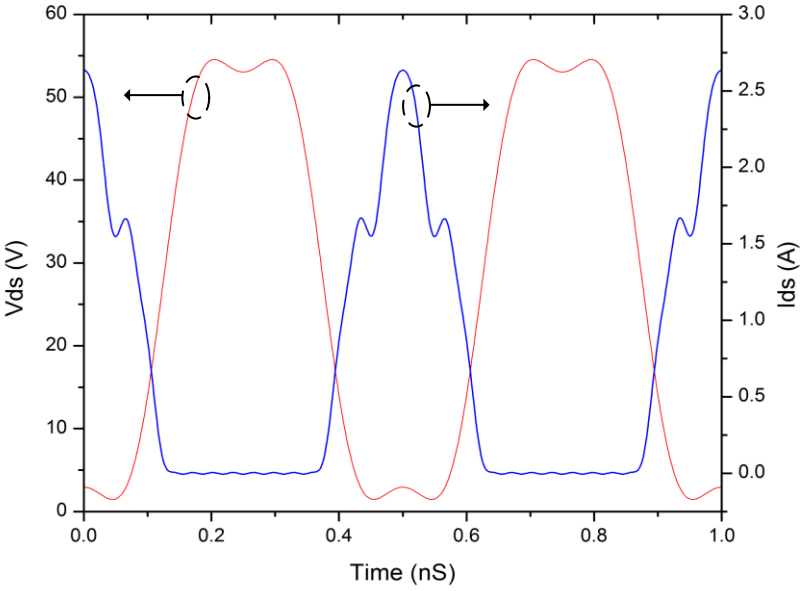


Fig 3.3: Simulated waveforms at 2 GHz at CRP.

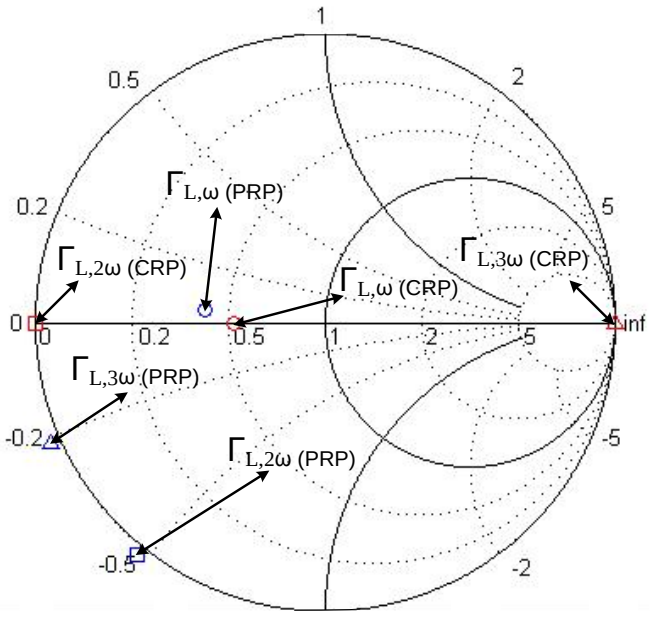


Fig 3.4: Load reflection coefficients at CRP and PRP.

access to the current reference plane (CRP). The HEMT was biased in deep class-AB mode with drain voltage as 30 V and drain current as 32mA. The resulting intrinsic current and voltage waveforms are shown Fig 3.3. These waveforms corresponding to Class F operation are obtained [28], [29] by precisely selecting fundamental and harmonic loads at CRP. It can be seen that the waveforms are slightly distorted due to package parasitics and absence of higher harmonics beyond third in the voltage. The second and third harmonic load impedances were set as short and open respectively which corresponds to the ideal theory of Class-F design. These loads at CRP are shown in the smith chart of Fig 3.4.

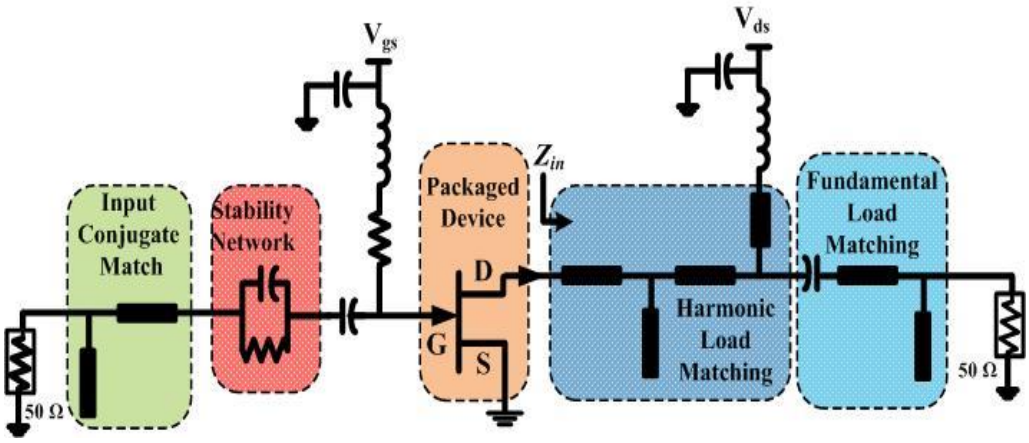


Fig 3.5: Layout of the designed class-F PA circuit.

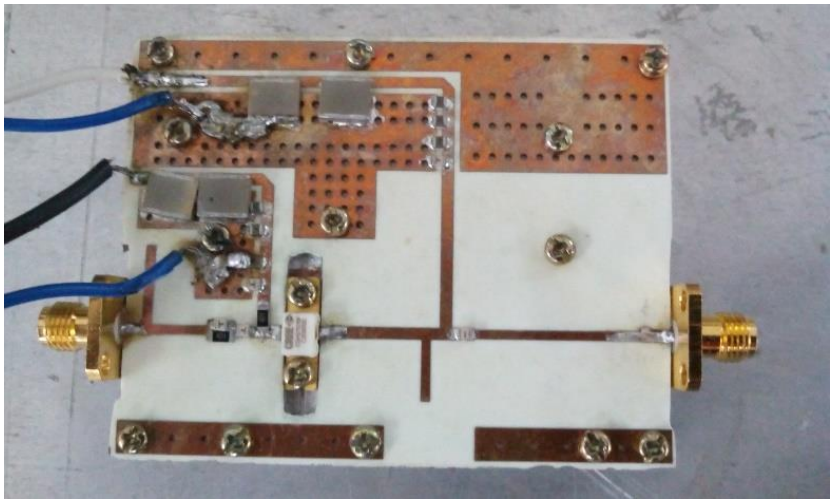


Fig 3.6: Photograph of the final class-F PA.

3.2.1 Implementation and Results

The PA was designed at 2 GHz. A real load impedance of 26 Ω is set at CRP. Using the ETN these load impedances for fundamental, second and third harmonic are computed at PRP in a single step as 20.462 Ω, -*j*23.83 Ω and -*j*10.58 Ω respectively. These values of required loads at the external plane are also plotted in Fig 3.4. The resulting schematic is shown in Fig 3.5. The output matching network has three sections: first for matching the 3rd harmonic, second to match 2nd harmonic and third subsequently matches the load at fundamental frequency. The drain bias network was incorporated in to the second harmonic matching. The fundamental was reasonably well matched with a stub and a line section. The input stability network comprised of a parallel RC circuit. The input was conjugate matched.

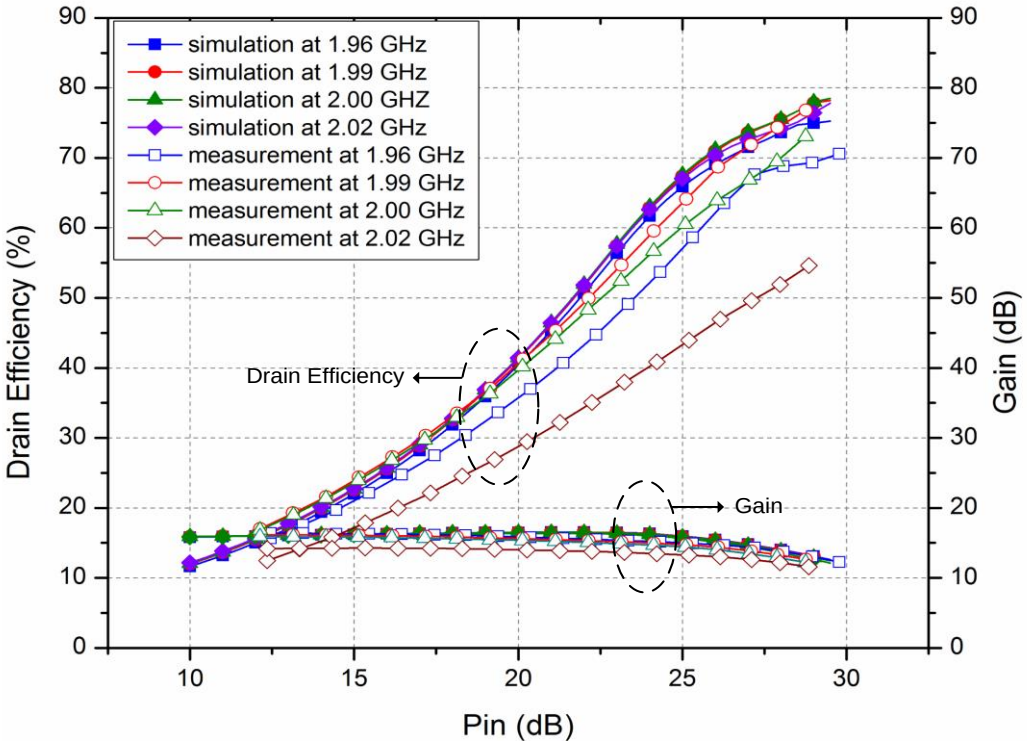


Fig 3.7: Measured and simulated results of class-F PA.

The PA is fabricated over Rogers substrate RO4350 with dielectric constant ε_r=3.66. The final fabricated amplifier is given in Fig 3.6. A continuous wave signal at 2GHz was used as an input. Measurements were performed from 1.96 GHz to 2.02 GHz Fig. 5 shows the simulated and measured results of DE and gain with respect to the output power for various frequencies over the band of 60 MHz. The peak DE of 76.8% and PAE of 72.6% is measured at 1.99 GHz. The corresponding gain and power at saturation is measured as 12.64 dB and 41.4 dBm respectively. The shift of 10 MHZ can be observed. This can be attributed to a fabrication and dielectric constant error.

In summary, this design helps to verify the usefulness of the nonlinear ETN for embedding the waveforms and load terminations at the CRP to the PRP. The design scheme provides the designers an access at the intrinsic plane to the designers to shape the load line and current waveforms.

Chapter 4
Continuous Class of Power Amplifier for Broadband Application

The previous chapter discussed about the design of a narrowband power amplifier centered at 2 GHz and how the harmonics can be utilized in boosting the efficiency. However, precise multi-harmonic impedance control is difficult to implement practically over large bandwidths. Moreover, these PAs incorporate matching networks having high quality factor which additionally narrows down the band. There is, thus, a need to further explore PAs working in the RF regime with a greater operational bandwidth capability along with comparable high efficiencies. With the capability of designing a singleband PA, the next logical step was to move to a broadband design keeping the efficiency as high as possible. Continuous Class-B/J, continuous class-F (and class-F^{-1}) have recently been proposed [30]-[31] and implemented to overcome this limitation. They utilize the concept of a family of optimal impedance solutions instead of a singular one maintaining the expected output power and linearity as their reference traditional mode.

Continuous class B/J have been proved to be broadband friendly allowing the PA to be operated in an octave bandwidth or more. However, this advantage comes at a cost. It is difficult to exactly match the output impedances with a practical load. This mismatch is the source of efficiency degradation. The inability of foster circuits to track the class-B/J design space impedances is presented and a solution is provided by delving into design space equations of the continuous mode.

The PA is initially designed at the current-source reference plane with the correct voltage and current waveforms. The intrinsic impedances are then projected to the package reference plane using the model-based nonlinear-embedding technique. An insight is provided into engineering the extrinsic harmonic impedance to rotate clockwise on the smith chart to be able to match it using a foster circuit. In order to validate the advantage of this analysis, the PA is implemented using a 15 W GaN HEMT transistor in the frequency range of 1.3 to 2.4 GHz and drain efficiency between 63% and 73% was achieved over the entire bandwidth.

4.1 Class-J Amplifier Theory

The class-J mode of operation [30] is an extension of the classical class-B amplifier. It is biased similar to class-B. The difference lies in the nature of the loads presented. Class-J requires a complex fundamental impedance and a purely reactive second harmonic termination with the third harmonic short-circuited. The resulting waveform of the output current and voltage are approximate half-wave rectified sinusoids. These waveform equations at the drain current plane is given by:

$$I_{ds}(\theta) = \frac{1}{\pi} + \frac{1}{2}\cos\theta + \frac{2}{3\pi}\cos 2\theta - \frac{2}{15\pi}\cos 4\theta + \frac{2}{35\pi}\cos 6\theta + \ldots \tag{4.1}$$

$$V_{ds}(\theta) = 1 - \cos\theta - \sin\theta + \frac{1}{2}\sin 2\theta \tag{4.2}$$

The above expressions result in the amplifier attaining a maximum theoretical efficiency of 78.5%, same as that of a standard class-B power amplifier.

4.2 Class-B/J Continuum

The expression given in (2) is not the only solution to achieve performance similar to class-B. In fact it is only a special case in a family of such solutions, where the reactive second harmonic component reinforces the voltage peak. Fig 4.1 illustrates some of these normalized waveforms possible. These can be mathematically represented as

$$V(\theta) = (1 - \cos\theta)(1 - \alpha\sin\theta), \qquad -1 \le \alpha \le +1 \tag{4.3}$$

This domain of α prevents the voltage from dipping below the zero level. Varying α controls the phase shift between the voltage and current. This set of solutions is what is known as the class-B/J continuum. The three special cases of $\alpha = 1{,}0\ and\ -1$ are known as class J, class B and class J^{-1} respectively.

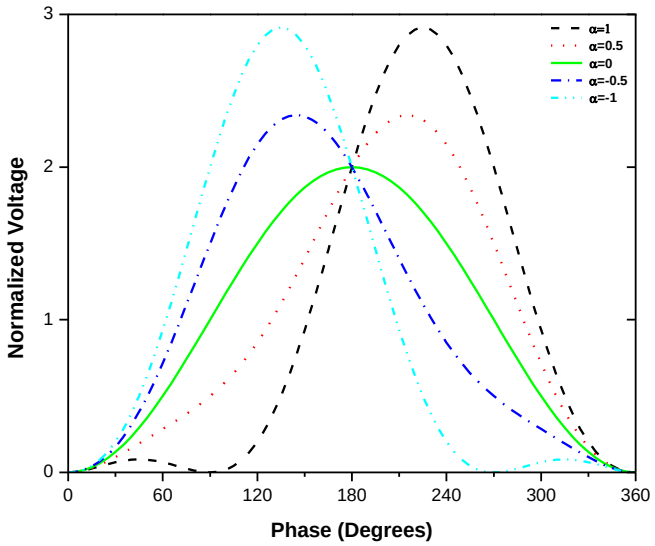


Fig 4.1: Continuum of theoretical waveforms for class-B/J.

For every α, there is a specific load which needs to be presented to the transistor, given as:

$$Z_{1f} = R_L + j\alpha R_L \tag{4.4a}$$

$$Z_{2f} = 0 - j\alpha \frac{3\pi}{8} R_L \tag{4.4b}$$

It should be noted that these impedances need to be presented at the current reference plane of the GaN HEMT. The impedances calculated by equation (4.4) are plotted on the smith chart in Fig 4.2 for a 15 W GaN HEMT. For the remaining part of the thesis Z_{1f} will be referred to as Z_{1int} and Z_{2f} as Z_{2int}. R_L is calculated from the load line as 20.5 Ω. For a positive α, the fundamental load has a positive reactance and the second harmonic a negative reactance. As α decreases and crosses 0, the fundamental reactance becomes capacitive and the second harmonic inductive. At $\alpha = 0$, the continuum assumes a class-B type of operation with the fundamental impedance purely resistive and the second harmonic termination as short. The continuous locus of Z_{1int}/Z_{2int} pairs on the smith chart of Fig 4.2 is what is known as the 'design space' for designing the output matching network. It gives the circuit designer the advantage of eliminating the need for precise harmonic shorting in practical amplifier circuits over a wide range of frequencies. The load for the matching network can now be chosen from a family of impedances instead of just one. All the solutions deliver the same output power and efficiency as conventional class-B but now over a broadband frequency range. This flexibility has encouraged the adoption of continuous class PAs.

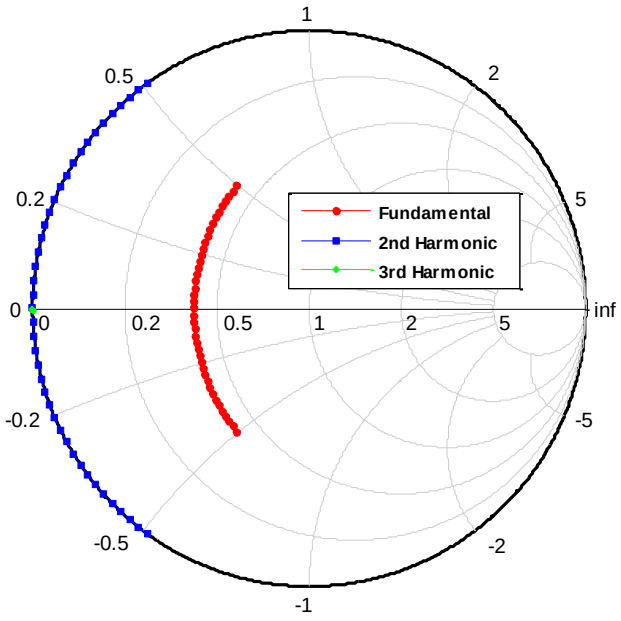


Fig 4.2: Calculated fundamental and second harmonic impedances.

4.3 Design and Validation: A 1.3-2.4 GHz 15 W GaN Power Amplifier

This section outlines the design of a broadband 15W high efficiency power amplifier designed in class-B/J mode of operation. The device used for the design was a commercially available 15 W Cree CGH27015F GaN HEMT packaged device. The class-J equations mentioned in the previous section have been defined for the intrinsic current reference plane. The device model used was a nonlinear embedded model discussed previously which provided access to the current reference plane (CRP). Before jumping to the designing aspects of the PA an investigation into the design space of the continuous class will be discussed.

4.3.1 Design Space Analysis

Earlier sections have described how a class-J amplifier results in a broadband operation. Using an embedded model one can project the impedances to the package plane of the device using the nonlinear embedding model. However, there still lies a bottleneck in designing such a broadband circuit. Practical matching network requires the fundamental and second harmonic impedance pairs to be rotated in a continuous clockwise fashion on the smith chart across the frequency band [32]. This is because the individual reactance of an inductor and a

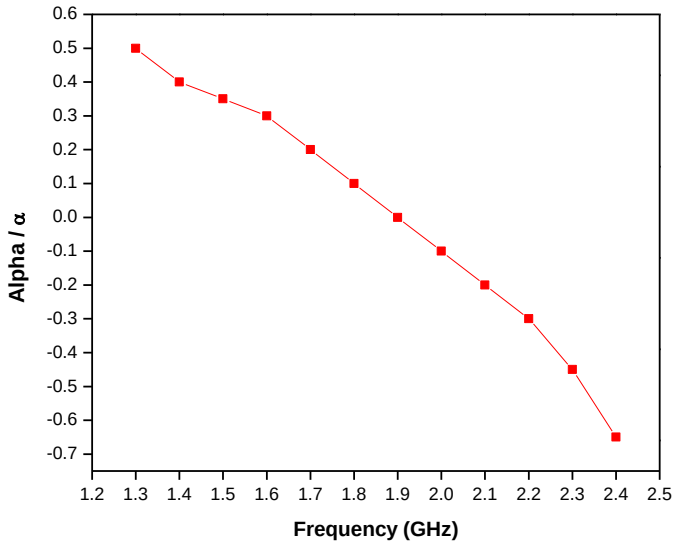
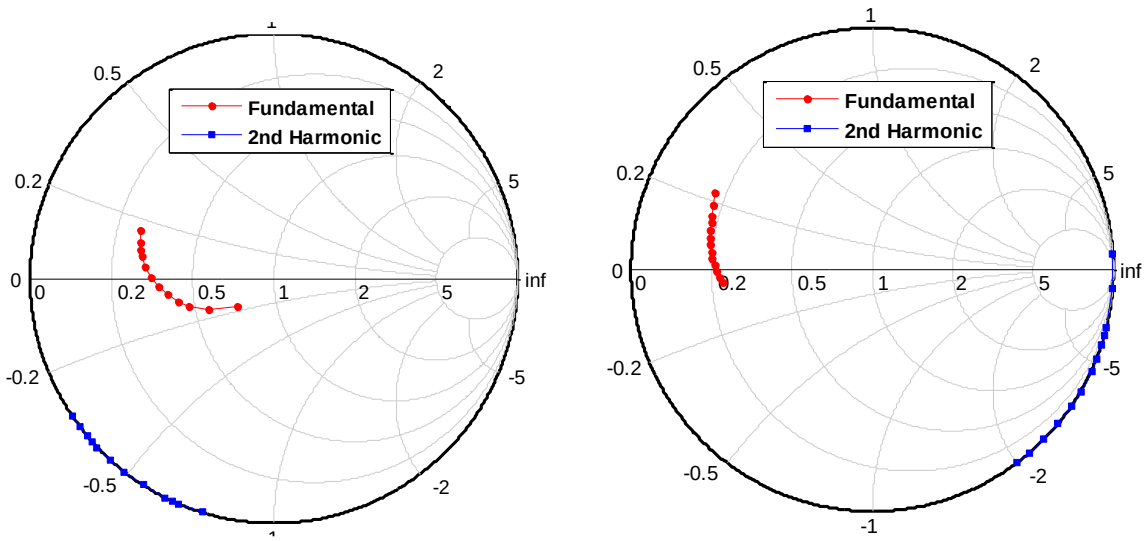


Fig 4.3: Relationship between α chosen and frequency.

capacitor both increase with frequency. Therefore, all passive components (both lumped and distributed) can lead to only foster networks. But the output loads predicted for the class-B/J design space rotate anti-clockwise. And these cannot be realized by any passive and lossless matching network. The challenge to design clockwise-rotating impedance can be overcome if the design space is investigated further in terms of the parameter α in equation (4.3).

Fixing the bias conditions fixes the load line. Subsequently for every α between -1 and 1 the intrinsic impedances (Z_{1int} and Z_{2int}) are also fixed. These will project corresponding extrinsic impedances at the package reference plane, known as Z_{1ext} and Z_{2ext} respectively. As an example, take the case of $\alpha = 0.5$. Z_{2int} is fixed at -j12.8 Ω using the optimum R_L as 20.75 Ω and α =0.5 as given by equation (4.4). The embedding model [25] is then used for calculating the Z_{2ext} at 1.3 GHz which comes out to be –j37 Ω. Keeping the bias conditions intact and α as 0.5 the model predicts the Z_{2ext} at 1.4 GHz as -j40 Ω, at 1.5 GHz as -j43.8 Ω, at 1.6 GHz as -j47.6 Ω and so on and so forth. This makes the second harmonic impedance move anti-clockwise on the smith chart which is the cause of concern. Instead consider that if α is reduced to 0.4 the Z_{2int} changes to -j10.2 Ω and at 1.4GHz the corresponding Z_{2ext} becomes -j33 Ω (instead of - j40Ω). Decreasing α further to 0.35 the Z_{2ext} changes to -j8.9 Ω and at 1.5 GHz this translates to -j32 Ω extrinsically. This process of reducing α is repeated till the upper cut off frequency is reached. At 2.4 GHz the α used was -0.65. It can be observes that decreasing α sufficiently as frequency increases actually makes the Z_{2ext} rotate clockwise. This technique is exploited in this thesis to make the output matching network realizable.



(a) (b)

Fig 4.4: Extrinsic impedance projected from nonlinear-embedding technique for (a) α = 0.5 to -0.65 and (b) α = 1 to 0.35.

In effect α is varied from +0.5 to -0.65 to achieve the target bandwidth of 1.3 to 2.4 GHz. Fig 4.3 shows such a relationship and the corresponding extrinsic impedances are plotted in Fig 4.4(a). It is observed that for every 100 MHz increase in the operating frequency the decrease in the value of α is roughly between 0.05 and 0.1. It is dependent on the designer (considering the target frequency band for which the RF PA needs to be designed). Keeping the reduction steps in α too low will not be sufficient to make the impedance rotate clockwise on the smith chart. For example reducing α from 0.5 (for 1.3 GHz) to, say, 0.49 (for 1.4 GHz) will still lead to Z_{2ext} moving anti-clockwise i.e. $|Z_{2ext}| > 37\ \Omega$. On the other hand, keeping the successive reduction steps too large will make it rotate clockwise but will diminish the upper frequency level as α cannot be reduced lower than -1. Reducing α by, say, 0.75 for every 100 MHz increase in frequency will result in α reaching -1 for 1.5 GHz. The bandwidth reduces to 200 MHz in this case (negating the usefulness of using class-B/J continuum).

There are other factors to be taken care of while choosing the set of values of α. The final locus of second harmonic impedances should be a smooth trajectory. The locus of Z_{2ext} along with the locus of Z_{1ext} should not present a very hard condition for the matching network. Fig 4.4(b) shows the projected impedances for $\alpha = +1$ to $+ 0.3$. The Z_{2ext} varies from +j1571 Ω to –j100 Ω for frequency varying from 1.8GHz to 3 GHz. This is harder to be realized from a relatively simple foster circuit. After comparing with this and other such simulations the choice for α as seen in Fig 4.4(a) seemed logical and easier to implement for the target

bandwidth and 15 W CREE GaN HEMT. A different set of values of α might work well for another device with different parasitics and frequency range.

The parameter α has already been shown to control the output voltage (4.3) and output impedance (4.4) at the current reference plane [30]. Henceforth, it is explained that it can also be used to directly control and manipulate the extrinsic impedance critical for designing the output matching network. Moreover, a designer can now control the bandwidth more easily. A careful choice of α can vary the bandwidth from a mere 200 MHz to well above 1 GHz. Such an analysis can be extended to other continuous modes of PAs such as continuous class-F.

4.3.2 Layout Description

The drain bias was set at 30 V and the gate bias at -2.9 V resulting in the quiescent current of 103 mA. This maintains a bias as 5% of Idss [33]. The fundamental and second harmonic terminations were set as in Section 4.2. The optimum fundamental load resistance was R_L=20.5 Ω at the intrinsic current plane. All harmonics beyond second were shorted. It is a reasonable assumption since the output capacitance of the device is fairly high. The performance is expected to be slightly degraded but would reduce the complexity of the final matching circuit. The intrinsic voltage and current waveforms were tailored to match the ideal class-B/J waveforms as close as possible. Fig 4.5 illustrates few of the waveforms generated at this plane. Once the intrinsic mode of operation was defined, impedance at the package reference plane was projected using embedding transfer technique as shown in Fig 4.4(a).

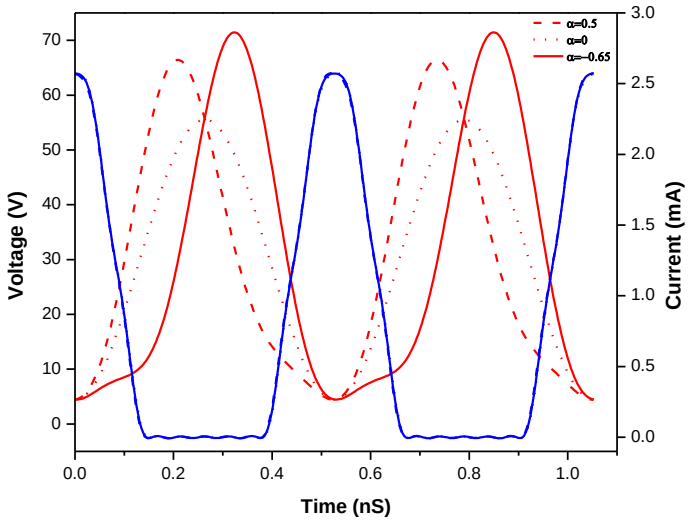


Fig 4.5: Voltage (red) and current (blue) waveforms set at the current reference plane.

Z_{1ext} was slightly adopted to follow a clockwise trajectory. Simulations were carried out in Keysight's Advanced Design System.

The broadband output matching network used in the circuit was designed keeping in mind a minimum level of drain efficiency throughout the frequency band as well as the target output impedance predicted earlier. It consists of six sections of microstrip lines (with three open circuited stubs) along with a 6.8 pF ATC capacitor acting as a DC block as shown in Fig 4.6. The drain bias is connected to the output using a 8.2 nH Coilcraft inductor. For practical realization the characteristic impedance of the lines had to be bounded between 20 and 90 Ω.

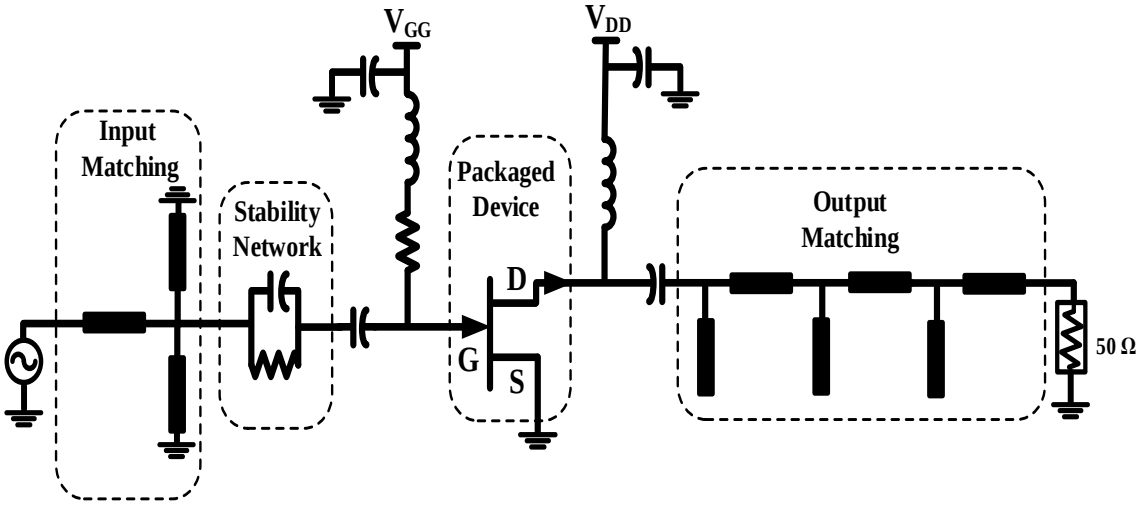


Fig 4.6: Final amplifier circuit layout.

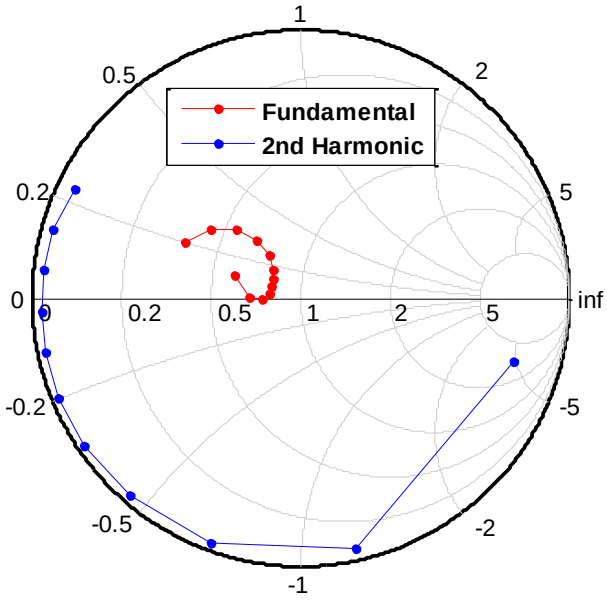


Fig 4.7: Measured output matching network impedances of the final amplifier.

A stability circuit is incorporated as a parallel RC network of 22 Ω resistor and 10 nH ATC capacitor to prevent oscillations. The broadband input matching network is designed using unequally terminated band-pass filter prototype approach [34]. The required input impedance Z_{in} for the entire frequency range is calculated after stabilizing the circuit. This input impedance can be modeled using a series RLC circuit. The real part of the input impedance Rin is around 6.5 Ω. The reactive components of this model (L and C) are absorbed using unequally terminated filter technique. Z_{in} is transformed over the frequency range to a purely resistive value kR_{in} (k being transformation ratio) which can finally be transformed to a 50 Ω using a simple impedance transformer. Consequently, there are two parallel quarterwave resonators and a quarterwave transformer to match R_s to 50 Ω. After an initial design the lines were optimized to compensate for the discontinuity effects. The final layout of the amplifier is illustrated in Fig 4.6. Fig 4.7 displays the measured impedances presented by the output matching network implemented through microstrip lines.

4.3.3 Implementation and Results

The broadband PA was implemented over the Rogers substrate RO4350 with dielectric constant $\varepsilon_r = 3.66$, substrate thickness of 20 mil and loss tangent of 0.0037. The photograph

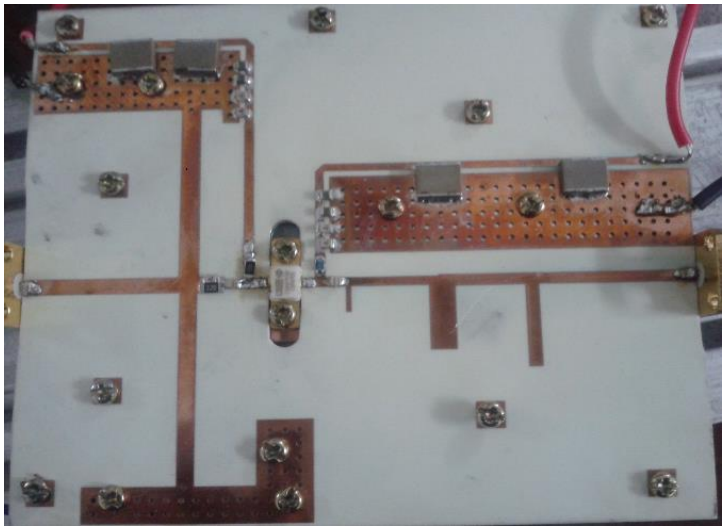


Fig 4.8: Photograph of the designed broadband PA.

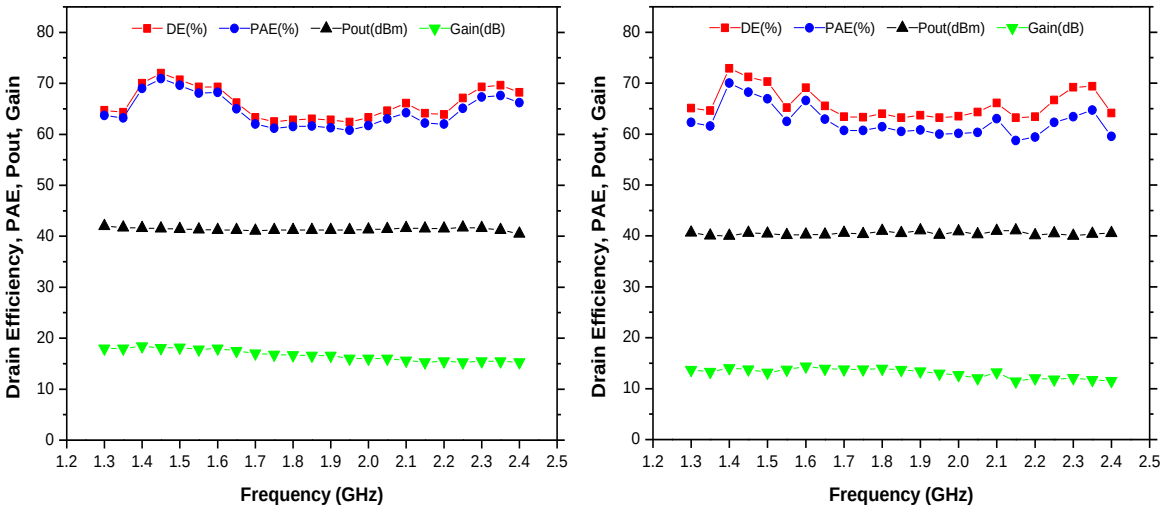


Fig 4.9: (a) Simulated results of the designed PA (b) measured results of the final PA.

of the fabricated PA is given in Fig 4.8. The measurement setup is excited with continuous wave signals from 1.3 GHz to 2.4 GHz at every 50 MHz step. The simulated and measured drain efficiency, power added efficiency, output power and gain is plotted in Fig 4.9. A minimum drain efficiency of 63.2% is observed at 1.95 GHz and a maximum value of 72% at 1.4 GHz. The average drain efficiency for the entire bandwidth (59% fractional bandwidth) comes out to be 66%. Output power varies between 40.1 dBm to 41.1 dBm through the frequency range with average output power as 40.5 dBm. The gain of the PA is kept between 11.4 and 14.3 dB across the band.

Chapter 5

Active Matching of Broadband Power Amplifier

So far the PAs designed have exploited proper use of harmonics to shape the voltage and current waveforms at the intrinsic drain of the device. The harmonics for current and voltage were generated through the non-linearity of knee region and the output capacitance. Proper harmonic termination was provided by passive reactive loads. As seen in the case of continuous class B/J the impedances projected at the package plane move anti-clockwise on the smith chart with increasing frequency. Passive circuits cannot match this movement. However, a proper selection of design parameter can provide realizable trajectory of output impedance in smith chart. The realizable trajectory may have mismatch from the trajectory of maximum efficiency. The mismatch leads to performance degradation. Efficiency attained by practical passive circuits is unable to match the maximum efficiency calculated for such modes of operation.

This limitation can be overcome if one uses active components also for matching the output of the device instead of only passive. These active devices may be diodes or transistors (BJT or FET). This active matching can achieve a better trajectory of load required for maximum efficiency in broadband PAs. There are principally two techniques for active matching:

1. Non-Foster Circuit (NFC)
2. External Harmonic Injection

Non-Foster circuits typically include negative capacitance $\left(\frac{1}{-j\omega C}\right)$ and negative inductance $(-j\omega L)$. Impedance plotted over smith chart shoe an anti-clockwise trajectory with the increasing frequency as depicted in Fig 5.1. In 1954 Linvill proposed the first non-Foster circuit using transistors [35]. NFC was used in filters, varactors, VCOs to compensate for the parasitic effects. This technique has been used extensively to overcome the limitation in antenna size and quality factor. Despite its use, NFC methodologies have only been restricted to small signal application. There are issues over power handling and stability which have prevented an extensive research of NFC in PAs. The authors of [35] demonstrated the first NFC-based broadband PAs with watt-level output power. They used negative capacitance for

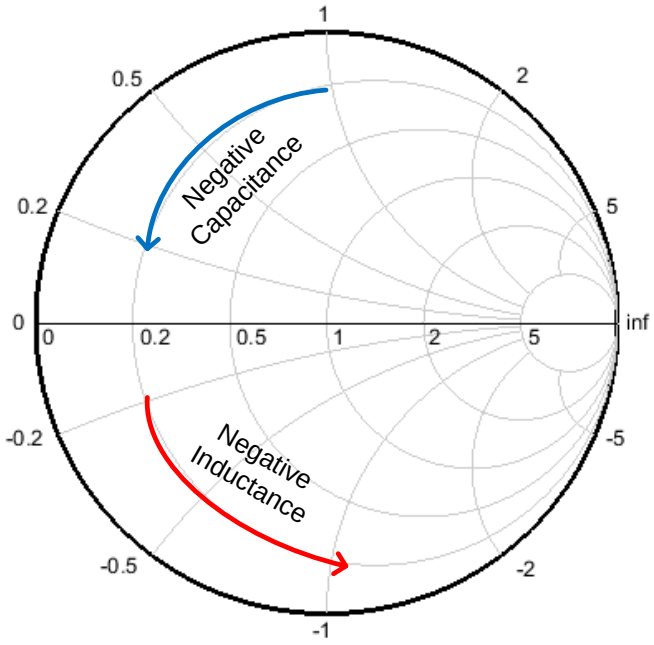


Fig 5.1: Movement of NFC on smith chart with increasing frequency.

inter-stage matching to mitigate high-Q limitation of bandwidth. However, it should be noted that the PA was MMIC-based. And due to limited resources the present work only deals in hybrid PAs with packaged GaN HEMTs. Working with packaged devices will pose certain problems while designing a NFC [35]:

1. Stability- Packaged HEMT has large parasitic capacitance and bonding inductance owing to a large physical size. The self resonance frequency of NFC is low but the gain of the transistor is large enough to oscillate. It may cause in-band oscillations or high frequency oscillations, causing a low frequency stability problem.

2. Power handling capability- Designing NFC for a 10 W or 15 W PA would require excessive DC power consumption to adequately scale with the RF power. This may degrade the overall PAE of the system. [35] also deployed the NFC for inter-stage matching only and not the 5 W output of the PA.

Keeping in view of these issues in designing a NFC to match the output of a continuous class-B/J PA, the second approach of harmonic injection was investigated and pursued further.

5.1 External Second Harmonic Injection

Harmonic injection refers to the mechanism in which power at one or more harmonics of the operating frequency is provided externally to either the input or output or both input and output of the active device. By supplying the harmonic at the output the voltage and the current waveform at the drain can be shaped appropriately. This wave-shaping helps achieve a higher efficiency in the PA than one without injection. Inputting power at second harmonic frequency utilizes second harmonic injection to address the theoretical limitation on efficiency.

Fig 5.2 shows the circuit configuration of a high-efficiency PA using second-harmonic injection technique. It consists of two parallel PAs: main and auxiliary and a diplexer. The signal at second harmonic is given as the input to the auxiliary PA with the proper phase and magnitude from a signal generator. The second harmonic is amplified by the auxiliary amplifier and is fed to the main PA via the diplexer. The diplexer has a dual role to play here. It blocks the fundamental from leaking from the main PA to the auxiliary PA and injects the second harmonic into the drain of the main PA.

Previous studies on second harmonic injection have reported an increase in efficiency. The authors of [36] have designed an PA at 0.9 GHz attaining 74% efficiency. A 10 W GaN PA in [37] showed an improvement of 17% in efficiency at 2.45 GHz by injecting second

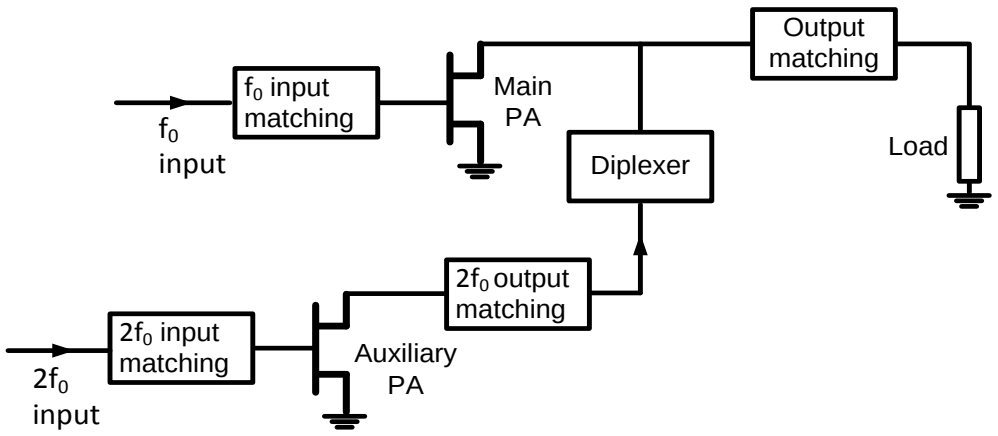


Fig 5.2: Circuit diagram of second harmonic injection technique.

harmonic and varying the bias point also. Another informative work presented in [38] designed an inverse class-F PA centred around 1 GHz with an optimized third harmonic termination.

5.2 Theoretical Analysis

Consider the normalized class-A waveforms with 50 % efficiency. Adding cosine terms at the second harmonic causes the current waveform to attain the same shape but 180° out of phase as the voltage waveform. The normalized equations become [37]:

$$\bar{i}(\theta) = \bar{I}_{DD} - \sqrt{2}\sin\theta + a_2\cos(2\theta) \tag{5.1}$$

$$\bar{v}(\theta) = \bar{V}_{DD} + \sqrt{2}\sin\theta + a_2\cos(2\theta) \tag{5.2}$$

Where, a_2 is the amplitude of the injected $2f_0$ signal.

To evaluate the efficiency of the overall system it is essential to consider the DC power consumed by the auxiliary PA. Therefore, a modified drain efficiency equation is as follows:

$$\eta_d(f_0) = \frac{P_{out}(f_0)}{P_{dc} + P_{dc}(\text{AUX PA})} = \frac{P_{out}(f_0)}{P_{dc} + \frac{P_{inj}(2f_0)}{\eta_d(2f_0)}} \tag{5.3}$$

Where, $P_{out}(f_0)$= fundamental output power

P_{dc}=DC power of the main PA

$P_{dc(AUX\ PA)}$=DC power of the auxiliary PA

$P_{inj}(2f_0)$=second harmonic power injected into the main PA

$\eta_d(2f_0)$= drain efficiency of the auxiliary PA

It is important to note here that the auxiliary PA will not be 100% efficient and the factor of $\eta_d(2f_0)$ is therefore introduced. In [36] efficiency improvement has been reported, but a 100% efficient auxiliary PA has been assumed. These results are not, therefore, sufficient to verify the advantage of second-harmonic injection technique. Equation (5.3) can give an efficiency value closer to a practical scenario.

5.3 A New Proposed Design

Previous designs have used a diplexer to connect the auxiliary PA and main PA. It prevents leakage of fundamental signal from the main PA to the auxiliary PA. It consists of a radial stub and a quarter wave line designed at fundamental frequency to present high impedance to the fundamental at the drain of the main PA. But this work presents a novel method to design second harmonic injection PA. A frequency doubler is used in place of the diplexer to prevent leakage of fundamental signal from the main PA into the auxiliary PA.

A frequency doubler is a non-linear device that generates twice the frequency of the signal applied to its input. However, there are always harmonics at the output which remain as spurious signals. These include the fundamental, third order, fourth order and all the higher harmonics. An efficiently designed doubler will suppress these unwanted harmonics at the output to leave a relatively high second harmonic signal. The greater this rejection the better is the functioning of a doubler. The fundamental frequency at the output acts as an unwanted signal with practically no significance. This fact is what is used to an advantage in harmonic injection PA design.

The doubler will inject the required second harmonic signal into the drain of the main PA just as the diplexer. It will invariably also inject a fundamental signal no matter however small. A fundamental signal in this branch will prevent the fundamental from the main PA to enter this branch. The signal $f_0(inj)$ from the auxiliary branch will add up with the signal $f_0(main)$ from the main branch to flow as signal $f_0(load)$ in the main output branch at junction X in Fig 5.3. This can be visualized as an example of Kirchoff's current law at junction X (the two PAs will act as current sources to set up a suitable current in the output branch). In the absence of $f_0(inj)$, however, the fundamental signal from the main PA is bound to leak into the auxiliary branch. The magnitude of the injected fundamental signal is not relevant as long as it is a non-zero quantity. In fact it is desired to have an extremely small value of $f_0(inj)$. It is noted that a higher value of $f_0(inj)$ can result in a higher value of $f_0(load)$ and consequently a higher value of fundamental power at the output load. However, it will pose a stiffer constraint on the frequency doubler to be designed for a higher second harmonic as well as fundamental signal as its output. Moreover, the increase in fundamental output power in this case will be due to an externally supplied fundamental signal and not due to the second harmonic

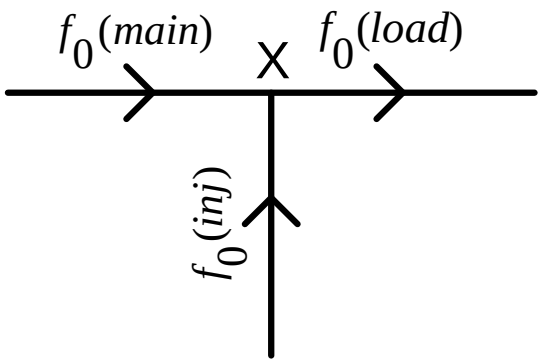


Fig 5.3: Representation of flow of fundamental signal.

injection. This will defeat the purpose of validating the advantage of harmonic injection technique per say.

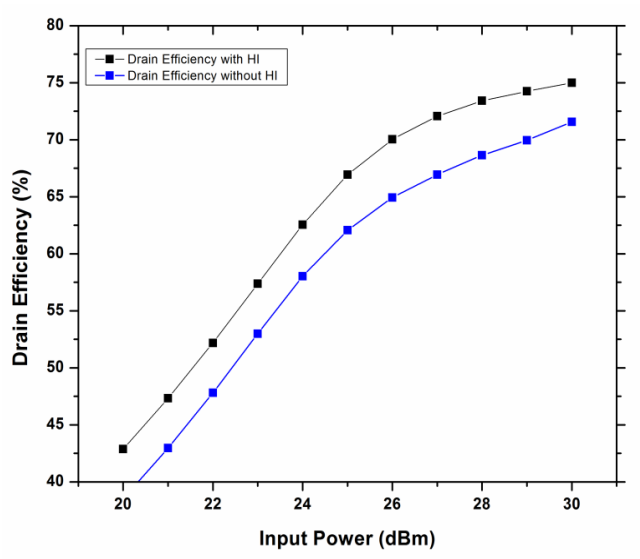
5.4 Simulation Setup

To validate the usefulness of the second harmonic injection in increasing the performance of a PA, the broadband class-B/J PA previously designed in Chapter 4 is used as a reference. Since the previous PA achieved over 63% drain efficiency over the band and an average output power of over 12 W, any improvement over this will prove highly beneficial and will also verify the frequency doubler concept discussed before.

For preliminary simulations a current source was used in place of the frequency doubler. The current source generated the second harmonic and the fundamental. This gave an added flexibility of manipulating the amplitude and phase of the injected signals. Simulations were carried out in the entire band of 1.3 to 2.4 GHz for every 50 MHz step and results were documented. At each frequency, keeping the injected fundamental signal small in magnitude, a second harmonic signal was injected into the main PA while adjusting its magnitude and phase. This helped in optimising for the best efficiency at each frequency. Interestingly, the entire frequency band reported an increase in drain efficiency as well as output power compared to the original class-B/J PA provided the injected second harmonic was at a proper amplitude and phase. It is extremely critical to ensure that the second harmonic power is injected with a particular amplitude and phase for that frequency in order to shape the current and voltage waveforms at the virtual drain of the device. Any deviation from this optimum

value will lead to a reduction in the enhanced efficiency. In fact it can even degrade the performance below the reference PA.

A comparison between the performance of the PA with and without harmonic injection (HI) has been illustrated in Fig 5.4 - Fig 5.6 for 1.4 GHz, 1.8GHz and 2.2 GHz respectively. For calculating the efficiency in harmonic injection case, the modified equation of (5.3) has been used. It can easily be seen that efficiency increases by about 5-10% at saturation as well as back-off region. At saturation the drain efficiency is reaching over 70%. This calculation is performed considering a 40% efficiency of the frequency doubler. A similar trend is observed for the entire band. The fundamental output power also increases. This happens because the injected second harmonic reduces the higher harmonic contents. Similarly, an increase in gain is observed across the input drive. The same figures also depict the simulated voltage and current waveforms at the intrinsic drain of the main PA transistor at the three frequencies. These waveforms have been measured through the new CREE large signal model of 15W GaN HEMT which allows access at intrinsic drain. Both the waveforms with HI have been better shaped as half wave sine wave which is essentially the shape of the class-B/J mode. The wave shaping clearly validates that the injection of power at second harmonic frequency into the drain is indeed leading to an improvement in efficiency and output power of the broadband PA.



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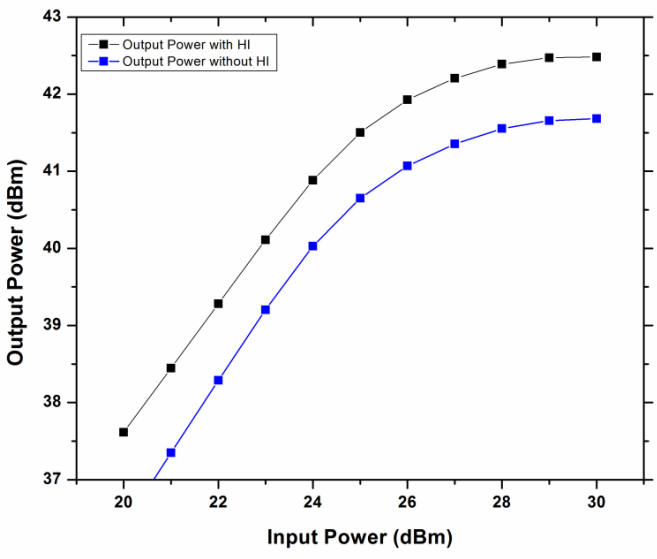

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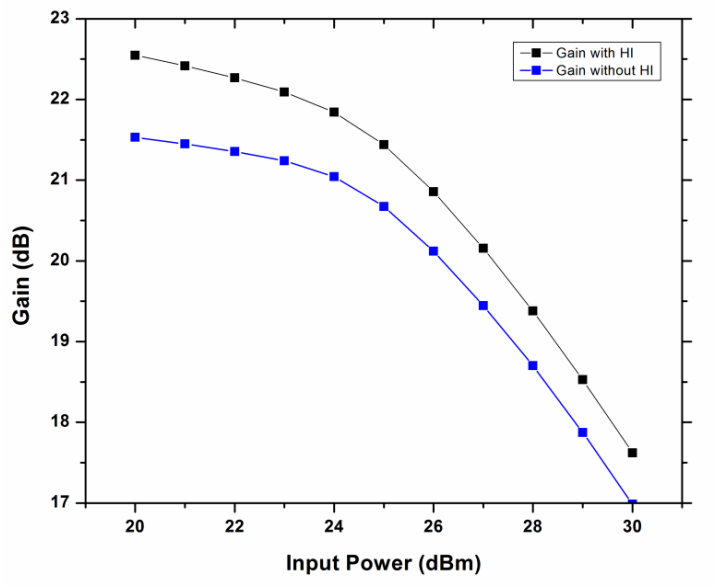

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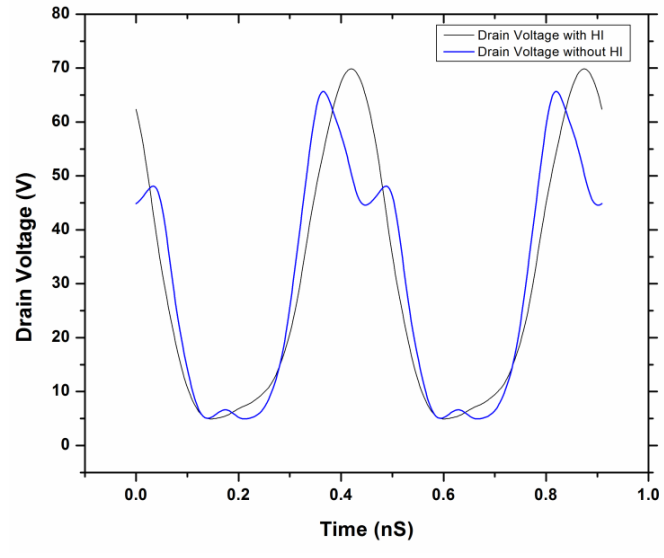

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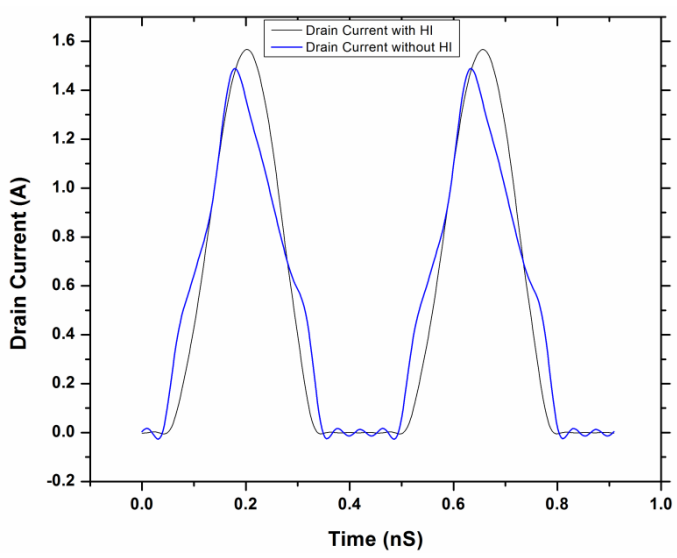


(e)

Fig 5.4: Simulated performance metrics between PA with HI and without HI at 1.4 GHz (a) drain efficiency, (b) Pout(f_0), (c) gain, (d) drain voltage and (e) drain current.

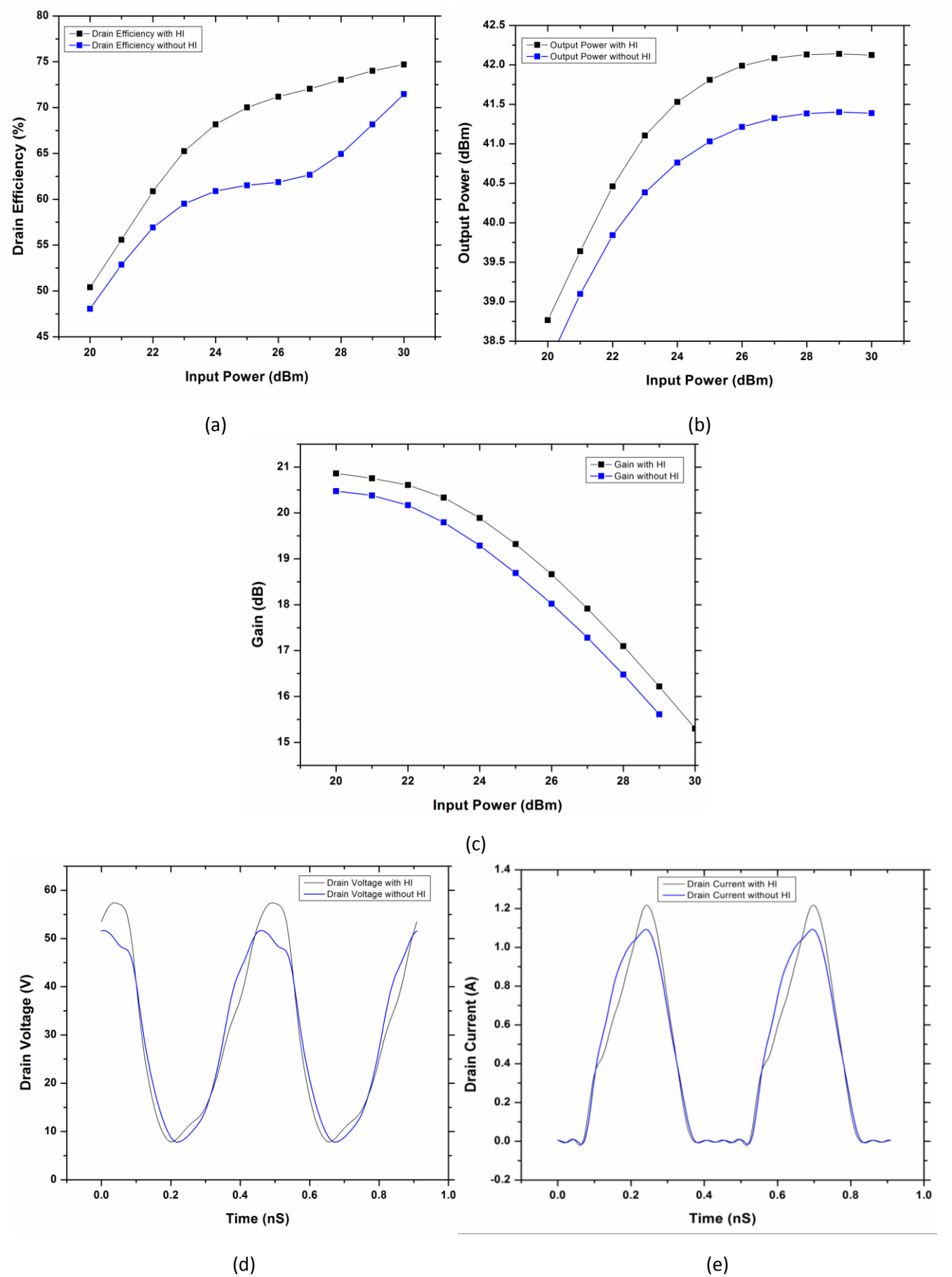
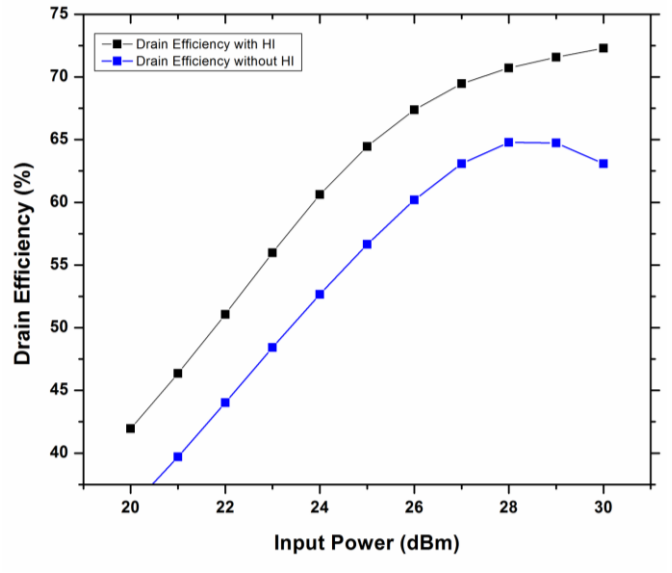
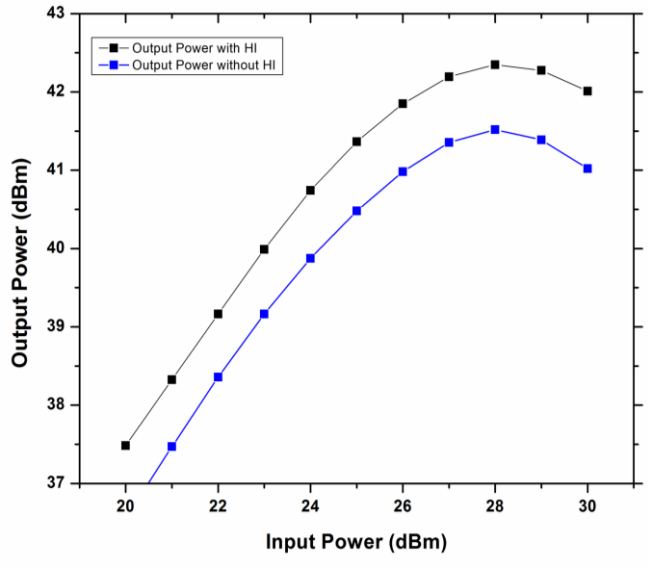


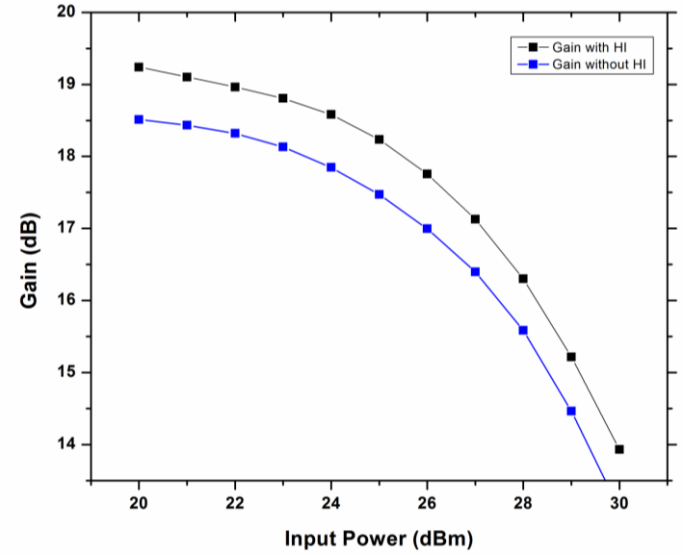
Fig 5.5: Simulated performance metrics between PA with HI and without HI at 1.8 GHz (a) drain efficiency, (b) Pout(f_0), (c) gain, (d) drain voltage and (e) drain current.



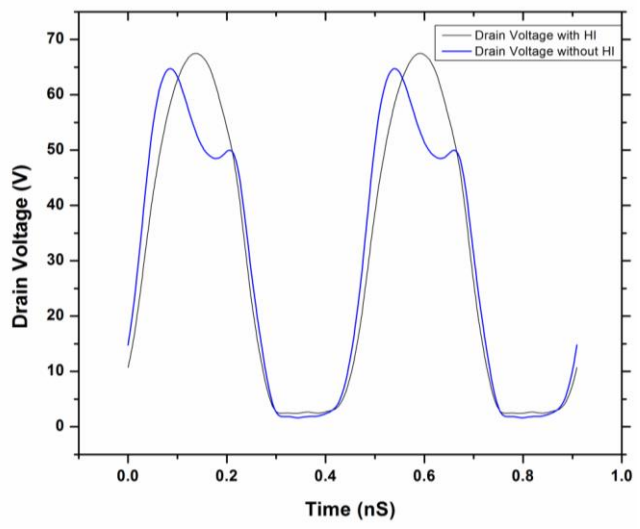
(a)



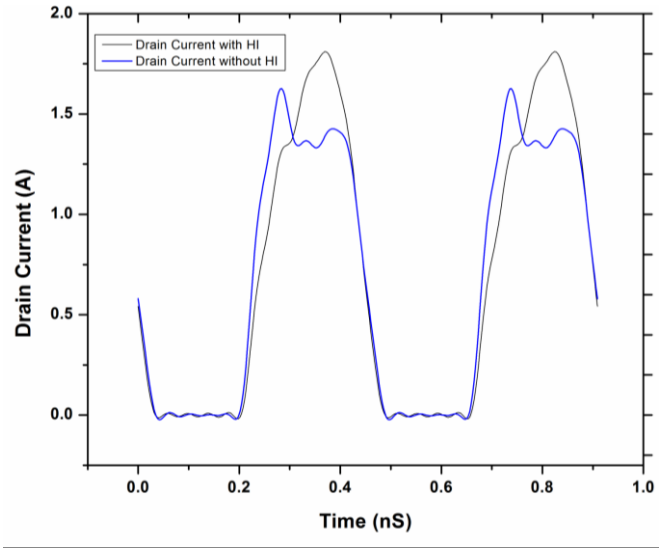
(b)



(c)



(d)



(e)

Fig 5.6: Simulated performance metrics between PA with HI and without HI at 2.2 GHz (a) drain efficiency, (b) Pout(f_0), (c) gain, (d) drain voltage and (e) drain current.

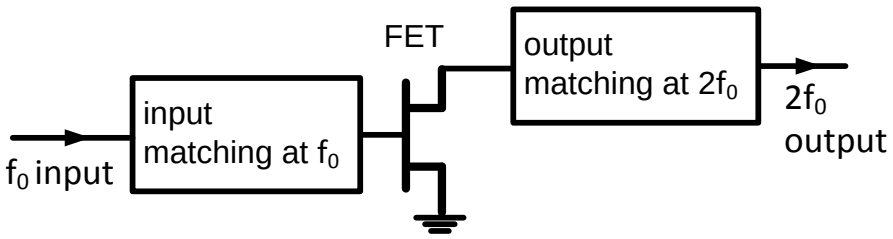
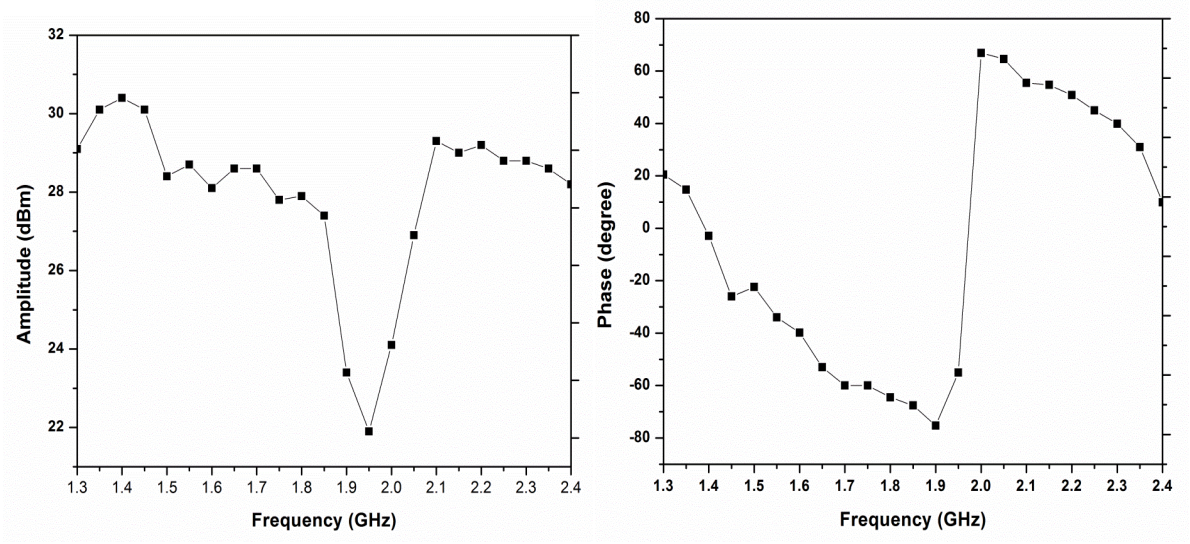


Fig 5.7: Schematic diagram of a frequency doubler.



(a) (b)

Fig 5.8 (a) Amplitude and (b) phase to be generated at the frequency doubler output.

5.5 Frequency Doubler Design Challenges

A frequency doubler can be thought of as an amplifier. However, instead of matching the output for the fundamental frequency, it is matched for second harmonic frequency. The input is matched for the fundamental frequency itself as illustrated in Fog 5.8. To increase the rejection of the harmonics at the output open circuited stubs of length $\lambda/4$ can be placed in shunt to the drain. Broadband operation can be realized via placing a band pass filter which will give the appropriate flatness over the required band.

As mentioned in the previous section that a proper phase and amplitude of injected second harmonic power is required to properly shape the waveform. This set of phase and amplitude is plotted in Fig 5.8 as a function of frequency. It is essentially the requirement of the

frequency doubler to attain a broadband performance. There is an abrupt drop in the amplitude around 1.95 GHz. Similarly, the phase changes from this frequency onwards. A practical doubler would be unable to achieve such a jump in amplitude and phase. Another challenge in designing the doubler is that the amplitude required is if the order of 28 dBm as shown in Fig 5.8(a). This is basically the second harmonic which has to be harnessed at the output of the FET used in the doubler. Therefore, a working prototype might get restricted to a shorter bandwidth because of this limitation (preferably 1.3-1.85 GHz). It might also entail other components such as a phase shifter to attain the sloping phase and a coupler to divide the input fundamental signal between the main PA and the doubler.

Conclusion and Future Work

GaN-based technology provides PAs with wide bandwidth and high efficiency due to higher charge density and higher voltage operation regime. These are characterized by lower on-resistance and output capacitance. Demand and requirements for more accurate device models has increased. It becomes essential to characterize the intrinsic and package parasitics which degrade the performance and linearity of a bare die. Angelov model is simple and accurate enough to model the drain current and voltage characteristics along with gate-source and gate-drain capacitances. The electrothermal model predicted the transistor's small signal and large signal behaviour quite reasonably. As a step forward, the embedded model can provided a useful strategy for the design of switch mode PAs. The theoretical values of loads at fundamental and harmonic can easily be projected to the package plane which is accessible to the designers.

A class-F PA was designed using an embedded model of 15 W HEMT CREE device at 2 GHz. It was optimised for 77 % drain efficiency and 15W output power. The intrinsic waveforms were engineered to match the class-F mode. The design scheme provides the designers an access at the intrinsic plane to shape the load line and current waveforms. Using the nonlinear embedded model, the waveforms and impedances are synthesized at the extrinsic package reference plane in a straightforward way respecting the intrinsic drain-source conditions of the desired mode of operation. Thus, overcoming the need for any loadpull measurements.

Waveform engineering was used to design a class-B/J PA and extend its bandwidth. In order to generate a clockwise rotation of the extrinsic impedances on the smith chart, the parameter α of class-B/J voltage equation was probed. Studying the behavior of the extrinsic impedances in terms of α allows designers to make an informed decision about the matching circuit requirements. Drain efficiency above 65% and output power greater than 12.5 W have been achieved over the entire band of 1.3 to 2.4 GHz.

In order to obtain optimum efficiency from continuous class PAs externally injecting the second harmonic frequency to the drain helped in shaping the current and voltage waveform. With proper shaping of the waveform overlap between the current and voltage can be minimized and consequently the power dissipation. This technique was validated using frequency doubler acting as the source of the second harmonic. Simulations show an increase

in efficiency as well as output power in the overall system provided an optimum magnitude and phase of second harmonic power is injected.

The work presented in this thesis can benefit future research to further address the requirements of next generation base station power amplifiers.

Modeling a transistor is a challenging area but highly rewarding. A model was developed for a pHEMT from data available from an open community source. This information can further be used to develop an embedded model as proposed in [25]. Due to unavailability of DC I-V curves at various bias points and temperature, the thesis utilises the large signal model provided by manufacturer and embedded model.

A second harmonic injection technique using a frequency doubler was established. A fully working prototype can be designed in the future.

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