POWER QUALITY IMPROVEMENT USING D-STATCOM

A THESIS

Submitted in partial fulfilment of the

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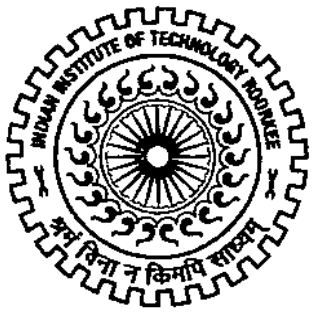
by

SREENIVASARAO D



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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in this thesis entitled **"POWER QUALITY IMPROVEMENT USING D-STATCOM"** in partial fulfilment of the requirements for the award of *the Degree of Doctor of Philosophy* and submitted in the Department of Electrical Engineering of Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from July, 2009 to July, 2013 under the supervision of Dr. Pramod Agarwal, Professor and Dr. Biswarup Das, Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institution.

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ABSTRACT

In present day distribution systems, major power consumption has been in reactive loads, such as motor drives, fans, pumps and power electronic converters. These loads normally draw lagging power factor currents and therefore give rise to reactive power burden in the distribution system. Excessive reactive power demand results into low power factor, poor voltage regulation, increased feeder losses and reduced the active power flow capability of the distribution system. Moreover, the situation worsens in the presence of non-linear loads and raises power quality issues on the distribution system. The primary source that draw non-linear currents from the distribution systems are power electronic devices. The operation of these non-linear loads on distribution systems results into harmonics current burden and interrupts the normal operation of the electrical equipments that are connected to the distribution system.

Nowadays, most of the equipments connected to the distribution system are based on power electronic devices, often leading to the problems of power quality. At the same time these equipments are typically equipped with sophisticated microprocessor based controllers which are quite sensitive to deviations of the voltage from its ideal waveform. In recent years, with the advent of sophisticated electrical and electronic equipment, the electric power quality (PQ) has become an issue of concern and extensive research is being carried out to improve the power quality.

In the early days, synchronous condenser and mechanically switched capacitors and inductors were used for reactive power compensation. However, due to their slow response and mechanical wear and tear, the use of these devices is limited for the applications, where fast compensation is not needed. With the advent of the first generation of Flexible AC Transmission System (FACTS) devices, thyristor-controlled Static Var Compensators (SVCs) schemes made significant advances in reactive power compensation as these devices are fast in operation. Besides, smooth control of reactive power compensation is also obtained by these devices. Despite the attractive theoretical simplicity of the SVC schemes, their popularity has been hindered by a number of practical disadvantages such as large size of the capacitor and inductor banks, dependency of the reactive power compensation on operating voltage. With the remarkable progress of gate commutated semiconductor devices, attention has been focused on second generation FACTS devices, which are based on self-commutated inverters. Among them, Static Synchronous Compensator (STATCOM) has attracted the attention of researches and power industries for reactive power compensation and voltage regulation in transmission systems.

Further, harmonic regulations or guidelines such as IEEE 519-1992 and IEC 61000 are being applied to limit the current and voltage harmonic levels. To meet these requirements, the harmonics must be mitigated by using harmonic filters. Active and passive filters are used either together to form hybrid filters or separately to mitigate harmonics.

Conventional power quality mitigation equipment can respond only to a particular power quality problem, and this fact has attracted the attention of power engineers to develop dynamic and adjustable solutions to power quality problems. One modern and very promising group of solutions that deals with load current and/or supply voltage imperfections is the Custom Power Devices (CPDs). CPDs rectify most of the distribution system problems and many of the existing compensation devices are being replaced by CPDs, thereby reducing the cost. The family of CPDs includes Distribution Static Synchronous Compensator (D-STATCOM), Dynamic Voltage Restorer (DVR) and Unified Power Quality Conditioner (UPQC) which is used for compensating the power quality problems in the current and/or voltage waveforms. Among these members, D-STATCOM is a shunt connected device, which takes care of the power quality problems in the current waveform. In this thesis, an attempt is made to develop a robust computer-controlled D-STATCOM for power quality improvement in 3P3W and 3P4W distribution systems.

It is well known that high performance and cost effective inverter is a prerequisite for the realization of a D-STATCOM. These inverters can be broadly categorised into two classes, namely, Voltage Source Inverter (VSI) and Current Source Inverter (CSI). A critical comparison of the performance of VSI and CSI, when used as a power circuit of D-STATCOM is beyond the scope of this thesis. However, in the present work, VSI is considered as a power circuit for D-STATCOM as it has higher market penetration and a more noticeable development on VSI has taken place over the last decade, in comparison to CSI topologies. The high harmonic content of the output voltage makes basic six-pulse (two-level) VSI impractical for direct use in high-power, medium-voltage applications. Instead of using filters and connecting several switching devices in series to achieve the required voltage level, several alternative solutions have been reported in the literature and can be broadly categorized into two groups: multipulse and multilevel inverters. The first one requires complex phase-shifting transformers and therefore, its application is limited to high-power, high-voltage systems. The second approach, Multilevel Inverters (MLI), uses the concept of addition of multiple small-voltage levels for achieving the required voltage level with the help of additional switching devices and few components like diodes or capacitors. This approach does not require complex phase shifting transformers and hence these topologies are best suited for medium-power applications. The common multilevel inverters topologies are Diode Clamped (DCMLI), Flying Capacitor (FCMLI) and Cascaded Multilevel Inverters (CMLI) or Modular Multilevel Cascade Inverters (MMCI).

The selection of individual inverter topologies for D-STATCOM applications depends on their performance, cost, size and implementation issues. DCMLI topology seems to be the most suited for D-STATCOM applications. But, the large number of power components and voltage unbalance problem at higher levels limits the DCMLI for low-power rating applications. On the other hand, FCMLI has a natural voltage balancing operation and

modular structure, but its application as a D-STATCOM is limited due to the requirement of a large number of capacitors and their pre-charging. In contrast, MMCI is one of the next generation multilevel inverters intended for high or medium-voltage power conversion without the requirement of line-frequency transformers. The MMCI is based on cascade connection of multiple single-phase H-bridge converter cells or chopper cells per leg. Among the members of MMCI, Single-Star Bridge Cell (SSBC) and Single-Delta Bridge Cell (SDBC) are characterized by the cascade connection of multiple single-phase H-bridge cells per leg.

The least component requirement, low cost, modular structure, easy expansion to any number of levels, high fault tolerance and absence of complex input transformer and non-initialization of the capacitor voltages make SSBC and SDBC best suited for D-STATCOM applications. Both SSBC and SDBC can reach higher output voltages and power levels (13.8 kV, 30 MVA) with readily available medium-voltage semiconductor devices. The SSBC and SDBC inverters have found input transformerless applications such as STATCOM, Battery Energy Storage System (BESS) and DVR. In the present work, the application of MMCI is extended to D-STATCOM, intended for direct installation on a medium-voltage distribution system for reactive power compensation and harmonic elimination. Towards this goal, the SSBC based inverter configuration is chosen over SDBC as the number of converter-cells required for SDBC is 1.732 (= $\sqrt{3}$) times that required for SSBC.

In order to control the output voltage of the inverter of D-STATCOM to act as a controllable current source, a suitable modulation technique is required for the SSBC inverter. Although a large number of modulation schemes for multilevel inverters have been reported in the literature for industrial applications, carrier based PWM schemes are still preferred because of their proven technology, simplicity and ease of implementation.

The carrier based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted PWM (PSPWM) and level-shifted PWM (LSPWM) techniques. The LSPWM technique produces the best harmonic performance, when compared with the PSPWM technique, but it does not cancel the current harmonics at the input side of the phase-shifting transformer. Nevertheless, because of the unequal device conduction periods of the LSPWM technique, has penetrated a smaller market even in those applications, where the transformer is not required at the input side, such as FACTS and CPDs, electric vehicle applications. The unequal device conduction periods affect the charging and discharging of the dc bus capacitors and cause non-uniform power and heat distribution in the inverter. To distribute the switching and conduction losses evenly, the switching patterns should be rotated. Such schemes for FCMLI have been given in the literature. In the present work, these switching schemes are extended to SSBC inverter.

Towards this goal, two simple and effective ways of rotating the carrier signal are investigated for application to SSBC inverters, which imposes an even power distribution among the H-bridge cells. These are:

1. Rotation of the carrier signals at the end of each modulating cycle.
2. Rotation of the carrier signals at the end of each carrier cycle.

In order to validate the performance of the carrier rotation techniques, simulation studies are carried out for 5- and 11-level SSBC based inverters in MATLAB/Simulink environment. From the simulation results, it is observed that line-to-line voltage, phase voltage and harmonic spectrum of line-to-line voltage for these carrier rotation techniques are identical to those produced by the basic LSPWM technique. In order to determine the device conduction periods of the carrier rotation techniques, the total conduction period of each device is calculated over a number of fixed modulating cycles. For this purpose detailed flowcharts of algorithms for calculating the device conduction periods are given in detail. By using these algorithms, total device conduction periods are calculated for 5-level and 11-level SSBC based inverters with various amplitude and frequency modulation indices. From these results it is observed that the device conduction periods are different for the basic LSPWM technique. However, with carrier rotation schemes, the device conduction periods are virtually equalized and as a result, the power loss and the heat distribution inside the inverter become quite uniform.

Towards the goal of achieving harmonic elimination and reactive power compensation with D-STATCOM, an 11 kV three-phase, three-wire (3P3W) industrial distribution system is considered. To design an inverter for 11 kV system, generally the inverter must be equipped with a transformer for galvanic isolation and voltage matching between the industrial/utility distribution system voltage and the inverter voltage. However, weight and size of the transformer is normally more than 50% of the inverter. To alleviate this problem, the focus of this research is to design a SSBC based D-STATCOM without any line-frequency transformer.

The cascade number (*N*, i.e. the number of cascaded voltage source H-bridge inverters in each phase) is one of the most important parameter for designing a transformerless PWM D-STATCOM. The value of *N* depends on the blocking voltage of the switching devices, cost, size and performance of the inverter. In the present work, IGBT is used as the switching device and further, a cascade number of *N* equal to 5 is chosen, considering the percentage total harmonic distortion (%THD), the dc voltage requirement and the voltage rating of the IGBT. For this D-STATCOM, a suitable value of reference dc voltage for each H-bridge cell is chosen. Ratings of various components of D-STATCOM such as dc capacitors for each H-bridge cell and inductance of coupling reactors are designed and carefully selected.

The performance of D-STATCOM depends on the control algorithm used for its implementation. The control algorithm considered in this work aims to eliminate harmonics, compensate reactive power as well as control and balance all the dc capacitor voltages of the SSBC in steady-state as well as in transient conditions. The load harmonic currents are derived by using the measured voltages at the point of common coupling (PCC), load

currents and the dc bus voltages of the H-bridge cells of the SSBC using Instantaneous Reactive Power (IRP) theory. If the supply voltage is unbalanced and/or distorted, then the load harmonic currents derived from IRP theory are not accurate. Hence, for proper operation of D-STATCOM, the voltages at PCC are derived from the positive sequence voltage detector. In order to control the voltages of the floating dc capacitors of the 11-level SSBC based D-STATCOM, the dc voltage regulator is divided into two control blocks: (a) cluster voltage balancing control and (b) individual voltage balancing control. The former one calculates the total amount of real power required for balancing the three cluster voltages of the inverter and the later one calculates the total amount of real power required for balancing the voltages of the floating dc capacitors to their corresponding reference values.

Simulation studies under different utility and load conditions are carried out to verify the performance of the 3P3W D-STATCOM for harmonic elimination and reactive power compensation. The simulation study of the entire system is carried out in the MATLAB/Simulink environment. A carrier rotation based LSPWM current controller is used to generate the gating signals for the IGBTs of the 11-level SSBC converter. Extensive simulation studies are carried out to investigate the performance of the D-STATCOM with an ideal and distorted voltage conditions. The simulation studies are performed for both steady-state and transient conditions with different non-linear and reactive loads. Further, the performance of the D-STATCOM is investigated with carrier rotation techniques and the capacitor voltage balance behaviour is observed among the individual dc capacitors of the D-STATCOM. Various performance indices such as THD, power factor, active and reactive powers and rating of the D-STATCOM are investigated. From these studies it is observed that the proposed control scheme completely compensates the reactive power of the load and makes the harmonic currents to be less and within the limits imposed by IEEE–519–1992 standard.

The three-phase, four-wire (3P4W) distribution systems have been widely employed to deliver electric power to single-phase and/or three-phase loads. The unbalanced and/or non-linear single-phase loads on these systems can result into a high current flowing through the neutral conductor. The problems related to the excessive neutral current are: overloading of distribution feeders and transformers, common mode noise, flat-topping of the voltage waveform and wiring failure. Therefore, these excess neutral currents must be compensated for the reliable operation of the 3P4W distribution system.

In recent years, a number of D-STATCOM schemes have been reported for simultaneous compensation of reactive power, source current harmonics and neutral current in 3P4W systems. They are: (a) three H-bridge topology (b) capacitor midpoint topology and (c) four-leg topology. However, these schemes require large volt-ampere (VA) rating of the inverter. Different transformer configurations such as zigzag, star-delta, T-connected, Scott-connected and star/hexagon-connected have also been used in recent years to attenuate the

neutral current on the utility sides due to the advantages of low cost, high reliability and simplified circuit connection. Among these, zigzag transformer approach requires a least VA inverter rating. However, these configurations can reduce the source neural current to a great extent but it will not completely compensate the same. Further, their compensation characteristics are dependent on their locations, the impedances of the transformers and utility voltage conditions. To alleviate this problem, a reduced rating hybrid topology comprising of a zigzag-delta transformer, a 3P3W active power filter (APF) and a single-phase APF has been demonstrated for the compensation of source neutral current and phase current harmonics, but, no attempt has been made so far to improve the displacement power factor. Also, the fundamental-frequency phase currents are also not made balanced. Another reduced rating hybrid topology consisting of a single-phase APF and a zigzag transformer for neutral current compensation has been proposed in the literature for neutral current compensation. However, in this method, no attempt has been made to improve the displacement power factor and compensate the harmonics of source phase currents. To address the above limitations, in the present work, three reduced rating hybrid 3P4W D-STATCOMs are proposed. They are:

1. A 3P4W hybrid D-STATCOM comprising of a zigzag-delta transformer, 3P3W D-STATCOM and shunt connected single-phase APF.
2. A 3P4W hybrid D-STATCOM comprising of a T-connected transformer, 3P3W D-STATCOM and shunt connected single-phase APF.

In these hybrid schemes, the functional capabilities of the existing schemes are enhanced to compensate the source current harmonics, reactive power and neutral current. For this purpose, a new control scheme is also proposed for generating the compensating currents for the D-STATCOM. To show the efficacy of the proposed control schemes, extensive simulation studies are carried out in the MATLAB/Simulink® environment. The performances of the proposed schemes are studied for reactive power compensation, harmonic elimination and neutral current compensation under various loading and utility operating conditions. From these studies it is observed that the proposed control schemes completely compensates the reactive power of the load and makes the harmonic currents to be reduced below the limits imposed by IEEE–519–1992 standard. Further, it also eliminates the source neutral current to a very large extent.

In order to further verify the simulation studies, a three-phase downscaled SSBC based inverter is designed, developed and tested to verify the viability and effectiveness of the carrier rotation techniques as well as of the 3P3W D-STATCOM and 3P4W hybrid D-STATCOM arrangements. For this purpose, the following prototypes are developed.

1. Three-phase five-level SSBC based inverter.
2. Three-phase five-level SSBC based D-STATCOM.

3. A 3P4W hybrid D-STATCOM comprising of a zigzag-delta transformer, 3P3W D-STATCOM and shunt connected single-phase APF.

To verify the control schemes experimentally, it is important to use an appropriate cascade number for realising the SSBC based D-STATCOM. The cascade number of *N* equal to 5 is definitely the best choice in terms of exact downscale. However, the inverter with *N* equal to 5 is challenging to design, construct and test in the laboratory (of the author). It is important to note that the control algorithm has no restriction on the cascade number and as a result the low value of *N* equal to 2 is used for realising the prototype D-STATCOM. With *N* equal to 2, the power circuit of the SSBC based D-STATCOM consists of 24 switching devices with the same voltage and current ratings. In the experimental set-up, IGBTs (IRG4PH40KD) are used as the switching devices. Different hardware components as required for the operation of the experimental set-up such as pulse amplification, isolation circuit, dead-band circuit, voltage and current sensor circuits and non-linear/reactive loads are designed and developed. By using the Real-Time Workshop (RTW) of MATLAB and Real-Time Interface (RTI) feature of dSPACE-DS1006, the Simulink models of the various controllers of the prototypes are implemented. The generated firing pulses are given to the corresponding semiconductor devices of each H-bridge of the inverter through isolation, delay and pulse amplification circuits in real-time.

The developed power circuit is tested initially as a dc-ac inverter to experimentally validate the efficacy of the carrier rotation techniques. The required isolated dc supplies for the six H-bridges cells are realised by three single-phase, three-winding transformers (230/115/115 V, 3 kVA) with single-phase diode bridge rectifiers and filter capacitors. A three-phase lamp load is used as a load for the inverter. The firing pulse generation circuit of the inverter is implemented in dSPACE. The line-to-line voltage, phase voltage and their corresponding harmonic spectra are observed, and these are found to be almost identical with and without carrier rotation techniques.

Subsequently, the developed prototype inverter is used as a D-STATCOM to verify the viability and effectiveness of the transformerless PWM D-STATCOM for harmonic elimination and reactive power compensation. In D-STATCOM implementation, each H-bridge cell is equipped with a galvanically isolated and floating dc capacitor without any power source or circuit. The IRP based controller of the D-STATCOM is implemented in dSPACE. An uncontrolled and a phase-controlled rectifier with *RL* and *RC* elements on their dc sides are used as non-linear loads.

The developed prototype is further tested for reactive power compensation and harmonic elimination with different loading and utility voltage conditions. After compensation with D-STATCOM, the source currents are observed to be almost sinusoidal and their corresponding %THDs are also observed to be well within the limits of IEEE–519–1992 recommended value of 5%. The source displacement and power factors are found to be

almost unity. The switching in response and the dynamic performance of D-STATCOM for a step change in the load is studied and in both cases, a smooth control of source current is achieved. A smooth control of dc voltages ensured the effectiveness of the dc voltage controller of the D-STATCOM. Further, the experimental results of the capacitor voltage balancing dynamics of the H-bridge cells with carrier rotation techniques are studied. The experimental results are found to be in good agreement with the simulation results.

In order to further verify the simulation studies of the proposed hybrid 3P4W D-STATCOMs, laboratory prototypes of the adopted compensator topologies consisting of five-level SSBC based 3P3W D-STATCOM and a zigzag-delta transformer with single-phase APF are developed. The single-phase APF is realized by the same IGBTs, which are used in the three-phase inverter. The dc bus voltage of single-phase APF is maintained by using a regulated power supply. Three single-phase transformers of 3 kVA and 230/115/115 V rating are used to realize the zigzag-delta transformer. The control algorithms are implemented in the dSPACE DS1006 R&D controller. The developed prototypes are studied for reactive power compensation, harmonic elimination and neutral current compensation with different loading and utility conditions. From these studies it is observed that the proposed control schemes completely compensate the reactive power of the load and make the harmonic currents to be reduced below the limits imposed by IEEE–519–1992 standard. Further, the control algorithms also eliminate the source neutral current to a very large extent. It is also observed that the performance of these hybrid approaches are significantly improved under distorted/unbalance utility voltage conditions.

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(Sreenivasarao D)

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LIST OF ACRONYMS

3P3W	Three-phase, Three-wire
3P4W	Three-phase, Four-wire
ac, AC	Alternating Current
APF	Active Power Filter
ASD	Adjustable Speed Drive
CHB	Cascaded H-bridge
CSD	Custom Power Device
CSI	Current Source Inverter
dc, DC	Direct Current
DCMLI	Diode Clamped Multilevel Inverter
DPF	Displacement Power Factor
DSO	Digital Storage Oscilloscope
DSP	Digital Signal Processor
D-STATCOM	Distribution Static Synchronous Compensator
EMI	Electro Magnetic Interference
FACTS	Flexible AC Transmission System
FCMLI	Flying Capacitor Multilevel Inverter
GTO	Gate Turn-off Thyristor
HVDC	High Voltage Direct Current
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical & Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
LSPWM	Level-shifted Pulsewidth Modulation
MLI	Multilevel Inverter
MOSFET	Metal Oxide Semiconductor Field-effect Transistor
PCC	Point of Common Coupling
pf, PF	Power Factor
PI	Proportional and Integral
PSPWM	Phase-shifted Pulsewidth Modulation
PWM	Pulsewidth Modulation
rms, RMS	Root Mean Square
SMPS	Switch Mode Power Supply
STATCOM	Static Synchronous Compensator
SVC	Static var Compensator
TCR	Thyristor Controlled Reactor
THD	Total Harmonic Distortion

LIST OF SYMBOLS

v_{Sa}, v_{Sb} and v_{Sc}	Three-phase source voltages
i_{Sa}, i_{Sb} and i_{Sc}	Three-phase source currents
i_{La}, i_{Lb} and i_{Lc}	Three-phase load currents
i_{Ca}, i_{Cb} and i_{Cc}	Three-phase D-STATCOM currents
m	Number of levels in inverter
N	Cascade number
f_{cr}	Carrier signal frequency
f_m	Modulating signal frequency
m_a	Amplitude modulation index
m_f	Frequency modulation index
L_s	Source inductance
L_C	Coupling inductance of D-STATCOM
L_f	Coupling inductance of single-phase APF
L_{ac}	Commutation inductance
p, q	Instantaneous real and reactive powers
$V_{ref,c}$	Cluster reference voltage
$V_{ref,i}$	Reference dc voltage for each H-bridge cell
k_p, k_i	Proportional and integral gains
i_{Sn}	Source neutral current
i_{Ln}	Load neutral current
v_{zn}	Voltage between zigzag transformer neutral and source neutral
v_{Tn}	Voltage between T-connected transformer neutral and source neutral

CHAPTER 1: INTRODUCTION

This chapter describes introduction to the research work. It starts with a brief background on foremost power quality problems in distributed systems. The different solutions to the problem including use of D-STATCOM are discussed in detail. At the end, the scope of work, author's contribution and thesis outlines are explained.

1.1 Overview

Traditionally, the role of the alternating current (ac) distribution system is to provide the interconnection between the generation and transmission system and industrial, commercial and residential load centres. The distribution system has always been susceptible to problems regarding reactive power demand and unbalance from the very beginning [1]. With rapid development of semiconductor device technology in the last three decades, the present day power distribution systems are also suffering from severe power quality problems [2, 3].

Power quality issues include all possible situations in which the waveforms of supply voltage and currents deviate from the sinusoidal waveform along with the variation of base frequency and amplitude beyond the respective permissible limits [2, 3]. Some typical disturbances to power systems, which may cause power quality problems, are summarised below [2]:

- Lightning and natural phenomena.
- Failure of equipment, e.g. transformers and cables.
- Inexperience operation of distribution substations and plants.
- Energization of large capacitor banks and transformers.
- Switching or start-up of large loads such as motors.
- Operation of reactive, non-linear and unbalanced loads.

All these disturbances contribute to power quality problems for both utility and customers. Among them, operation of reactive, non-linear and unbalanced loads are considered to be one of the most significant reasons for power quality problems in modern distribution systems [2].

The operation of non-linear and unbalanced loads on distribution systems results in low power factor, poor voltage regulation, harmonic currents, load unbalance and excessive neutral current. The increased reactive power, harmonics and unbalance cause an increase in line losses and voltage distortion in the power system [2-4]. For completeness, the aforementioned problems are briefly discussed below.

1.2 Reactive Power Burden

Reactive power burden on distribution systems is due to the operation of loads that draw high reactive power from the system. Reactive power is a concept used by engineers to describe the background energy movement in an ac system arising from the production of

electric and magnetic fields [5]. These fields store energy which exchanges through each ac cycle. Devices which store energy by virtue of a magnetic field produced by a flow of current are said to absorb reactive power; while those which store energy by virtue of electric fields are said to generate reactive power. Volt-ampere reactive (var) is a unit used to measure reactive power in an ac electric power system [5].

Reactive power (vars) is required to maintain the voltage to deliver active power (watts) through transmission lines and distribution feeders. Motor loads and other loads require reactive power for their successful operation. When enough reactive power is not available, the voltage sags and it is not possible to push the real power demanded by the loads through the lines [5, 6].

For better understating, a simple power system model indicating the coupling between source and load is shown in Fig. 1.1.

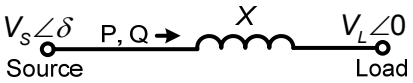


Fig. 1.1: A small power system model.

In general, the flow of active and reactive powers in a power system is governed by the following equations [5, 6].

The transmitted active power (P) is given by,

$$P = \frac{V_S V_L}{X} \sin\delta \tag{1.1}$$

For small value of δ, the reactive power (Q) transferred to the load is given as,

$$Q = \frac{V_L(V_S - V_L)}{X} \tag{1.2}$$

The load voltage (V_L) is given by,

$$V_L = V_S - \frac{QX}{V_S} \tag{1.3}$$

Equation (1.1) shows that the active power flow depends on the amplitudes of source voltage and load voltage and it flows from the leading voltage bus to lagging voltage bus. On the other hand, the reactive power depends mainly on the difference of voltage amplitudes across a feeder and it flows from higher voltage side to lower voltage side as given by equation (1.2).

It can be observed from equation (1.3) that to keep the V_L fixed for a given value of V_S, the drop $\left(\frac{QX}{V_S}\right)$ must remain constant. In this expression the only variable quantity is Q, which must be locally adjusted to keep V_L fixed. In other words, let Q be the value of reactive power which keeps V_L to be a specified value and any deviation in Q at load end must be locally adjusted. If Q is made zero (i.e. the load reactive power is supplied locally), the source

and load voltages will be the same. The local generation of reactive power can be accomplished by any of the reactive power compensating devices. This is the fundamental mechanism for controlling the reactive power in electric power system [5, 6].

The major sources that draw reactive power from distribution systems are [5, 7, 8]:

1. Phase-controlled rectifiers
2. Motors
3. Transformers, tap-changing transformers
4. Choke inductors.

The high reactive power burden leads to the underutilisation power system capacity due to [5-7]:

- Increased losses in the transmission and distribution systems.
- Overrated equipments within the ac system: due to large current drawn for a given real power demand and low efficiency owing to more losses.
- Low power factor and poor voltage regulation.

Therefore, there is a need to reduce the reactive power drawn by the loads.

1.3 Harmonic Distortion

Harmonic distortion is caused by the operation of non-linear loads in the power system. Non-linear loads change the sinusoidal nature of the ac power current, thereby resulting in the flow of harmonic currents in the ac power system that can cause interference with communication circuits and other types of electrical and electronic equipments [2-4]. The prime sources of harmonics in the power system are given in Table 1.1 [2-4].

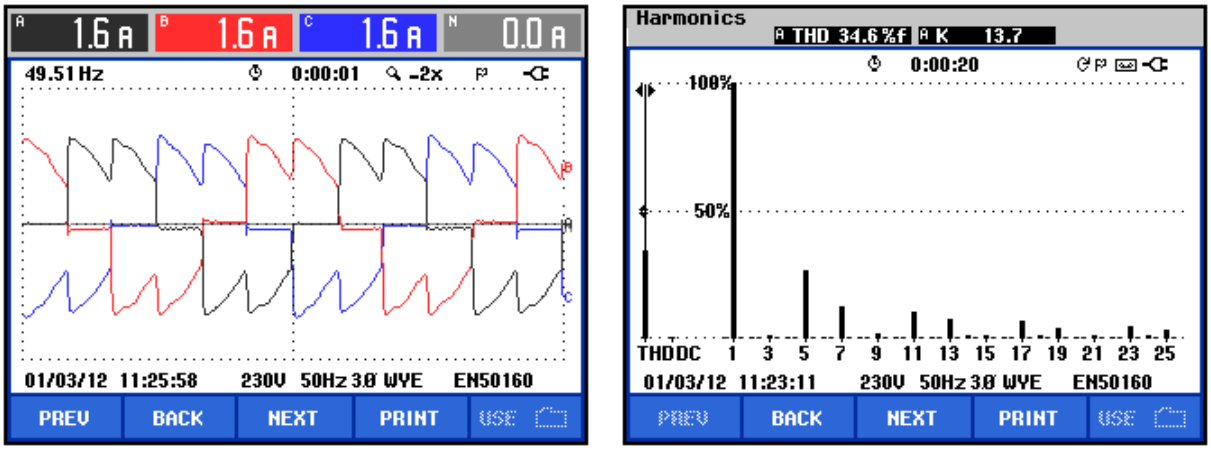
Table 1.1: Prime sources of harmonics.

Sources of harmonics			
High-voltage converters	Low-voltage power electronic devices	Conventional sources	Modern electronic equipment
Adjustable speed drives	Uncontrolled rectifiers	Electrical machines	Personal computers
HVDC converters	Controlled rectifiers	Transformers	Printers
Traction	AC regulators	Inductors	Photocopiers
Arc furnaces	Inverters		Air conditioners
SVCs	Cycloconverters		Televisions
			UPS
			Microwave ovens
			Fluorescent lamps

Harmonics are basically the additional frequency components present in the mains voltage or current which are integral multiples of the mains (fundamental) frequency [4]. Inter-harmonics are of special categories of harmonics which are non-integer multiples of the

fundamental frequency. Sub-harmonics are another special category of inter-harmonics, which have frequency values less than the fundamental frequency. Most equipments only produce odd harmonics but some devices have a fluctuating power consumption, over a duration of the half cycle period or less, which may generate even, inter-harmonic, or sub-harmonics currents [4]. The harmonic distortion of each device depends on its consumption of active power, background voltage distortion and source impedance.

Phase controlled rectifiers are major source for harmonics and reactive power burden. They have a wide range of applications, from small rectifiers to large High Voltage Direct Current (HVDC) transmission systems. They are used for electro-chemical process, motor drives, traction equipment, controlled power supplies and many other applications. The typical three-phase currents drawn by a phase-controlled rectifier is recorded as shown in Fig. 1.2(a). The corresponding harmonic spectrum of source current of phase–*a* is shown in Fig. 1.2(b). From Fig. 1.2(b) it is observed that the source current contains large amount of low order harmonics with an observed THD of 34.6%.



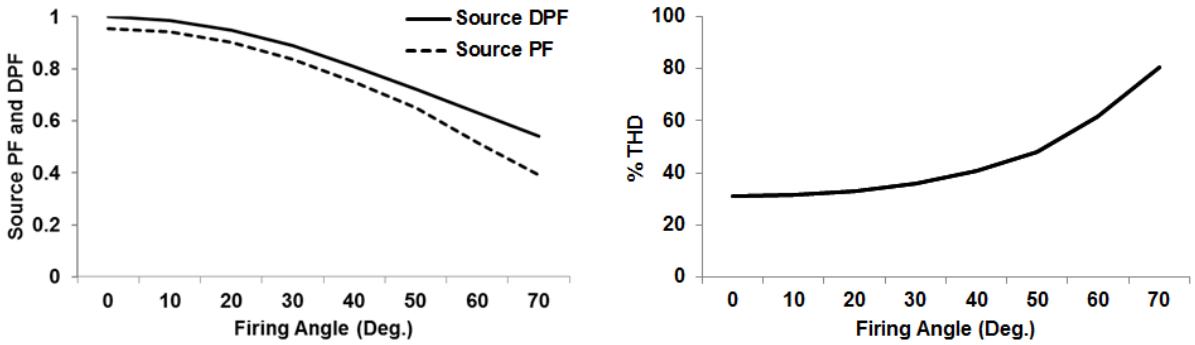
(a) Three-phase source currents (b) Harmonic spectrum of phase–*a*

Fig. 1.2: Source current waveforms and harmonic spectrum of a phase-controlled rectifier.

The phase-controlled rectifiers have following distinct features:

1. They can draw significant fundamental reactive power, whose magnitude depends on the firing angle of the rectifier.
2. They draw currents with sharp rising and falling edges with high harmonic content.

The source power factor, displacement factor and %THD of the load current of the phase controlled rectifier as a function of firing angle are plotted in Fig. 1.3(a) and (b). From Fig. 1.3 it is observed that the reactive power demand and %THD of the load current increases with the increase in firing angle of the rectifier.



(a) Variation of source power factor and displacement factor with firing angle

(b) Variation of %THD of load current with firing angle.

Fig. 1.3: Variation of source power factor, displacement factor and %THD of load current with firing angle of the phase-controlled rectifier.

1.3.1 Effects of Harmonics

The harmonics may affect equipments adversely as listed below [2, 4, 9]:

1. Communication interference: The magnetic (or electrostatic) coupling between electrical power circuits and communication circuits can cause communication interference [9]. The current flowing in the power circuit produces a magnetic (or electrostatic) field which, in turn, induces a current (or voltage) in the nearby conductors of the communication circuit. The amount of interference depends upon the magnitude of the induced current (or voltage), frequency and the magnetic (or electrostatic) coupling. Other types of communication interference are:
    - Induced line noise
    - Interference with power line carrier systems
    - Relay malfunctions.
2. Heating: The harmonic currents can cause excessive losses in motors, capacitors and transformers connected to the system. This in turn, may cause excessive heat in the winding, thus leading to the failure of insulation and the danger of a fire hazard [4].
3. Malfunction of solid-state devices: The harmonics can cause solid-state devices to malfunction if the equipment is sensitive to zero crossings or operates in response to the peak values of utility voltage. The typical malfunctions are [2, 4, 7]:
    - Errors in measurement equipment
    - Nuisance tripping of relays and breakers
    - Unstable operation of zero-voltage crossing firing circuit
    - Interference with motor controllers.
4. Damage to capacitors: The presence of capacitors, such as those used for power factor correction, can result in local system resonances, which, in turn, can lead to excessive currents and possible subsequent damage to the capacitors [2].
5. Malfunction of utility Meters: Meters, specially energy meters may record (energy consumed) incorrectly, resulting in higher billings to consumers [3].

6. Failure of sophisticated electronic equipments: Electronic equipments such as computers, remote monitoring systems, air conditioning systems, Switched-Mode Power Supplies (SMPS) and Uninterrupted Power Supplies (UPSs) may fail due to harmonics [2].
7. Flickering of lights: Due to the operation of arcing devices such as arc furnaces, arc welders and discharge type lightning with magnetic ballasts, flickering of lights may take place [2].

1.3.2 Harmonic Standards

There are various organizations on the national and international levels working closely with engineers, equipment manufactures and research organizations to come up with standards governing guidelines, recommended practices and harmonic limits [4]. The primary objective of the standards is to provide a common ground for all involved parties to work together to ensure compatibility between the end-user equipments and the system equipments. The most commonly used harmonic standards are IEEE–519–1992 [10, 11], International Electrotechnical Commission standard IEC–61000 [12], South African standard NRS–048 and European standard EN–50160.

IEEE–519–1992 standard limits the amount of current harmonics injected by a user at the Point of Common Coupling (PCC) [11]. For example, the IEEE–519–1992 standard recommends a limit of 5% Total Harmonic Distortion (THD) in the current at the PCC in a weak system. The THD in the current is the ratio of the rms value of its distortion components to the rms value of its fundamental-frequency component. It is given as,

$$\%THD = \frac{\sqrt{\left(\sum_{h=2}^{\infty} I_h^2\right)}}{I_1} \times 100\% \tag{1.4}$$

Where, I_h = rms value of the current at harmonic order h and I_1 = rms value of the fundamental-frequency current component.

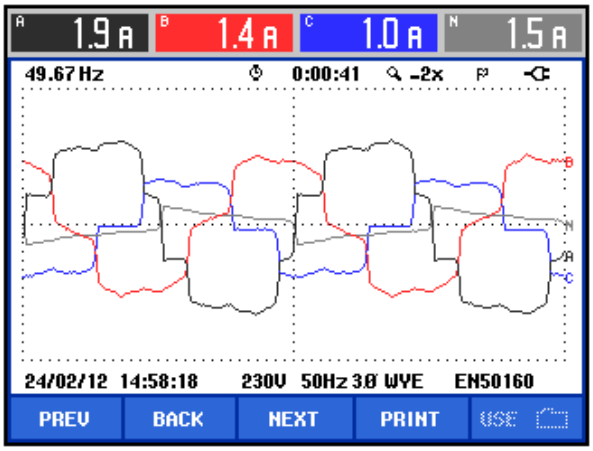
1.4 High Neutral Currents and its Detrimental Effects

Three-phase system is the most commonly used system for generation, transmission and distribution of electric power. Three-phase systems can be grounded or un-grounded. If a three-phase system is grounded at more than one point under normal operation (no-fault or short-circuited operation), the ground can provide an additional path for current circulation. A three-phase system can also have a fourth conductor called the “neutral wire”. In both these cases the system is classified as three-phase, four-wire (3P4W) system. If no ground is present or there is only one grounded node in the whole sub-network, the system is classified as a three-phase, three-wire (3P3W) system [13].

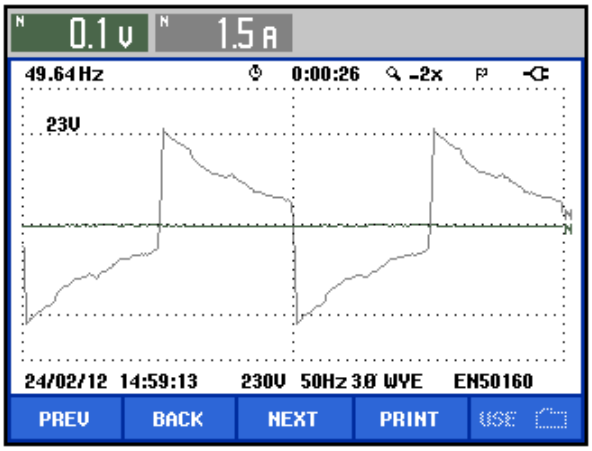
The 3P4W distribution systems are widely employed to deliver electric power to single-phase and/or three-phase loads in manufacturing plants as well as in commercial and

residential buildings [14]. In these systems single-phase supply to small loads is provided by one of the phase conductors and the neutral wire. To balance the load on each of the phases, the single-phase loads are evenly distributed among the various phases. In practice, these single-phase loads are not completely balanced, thus resulting in a net current flowing through the neutral conductor. Furthermore, there are also other sources of neutral currents such as non-linear loads, where even perfectly balanced single-phase non-linear loads on 3P4W system can result in significant amount of neutral current [14, 15]. With sinusoidal load currents, the neutral current depends only on the level of system unbalance. But, in a balanced system with distorted current waveforms (due to harmonics), only the triplen harmonics (i.e., with harmonic order multiple of 3) contribute to the neutral current. When both harmonic distortion and load current unbalance are simultaneously present, the neutral current may contain all order of harmonics [14, 16].

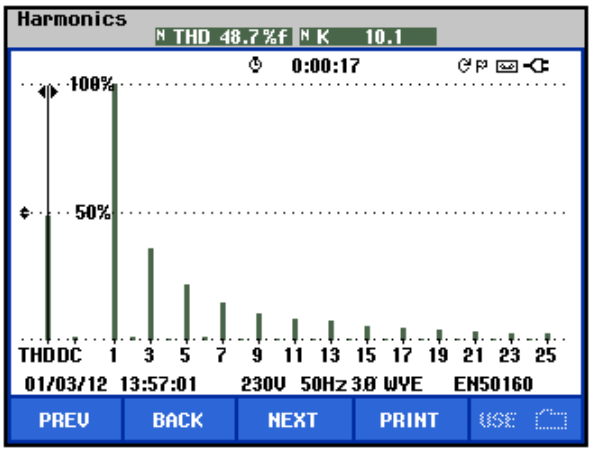
The typical three-phase currents drawn by an unbalanced load on 3P4W system are recorded as shown in Fig. 1.4(a). The source neutral current and its corresponding harmonic spectrum are also recorded as shown in Fig. 1.4(b)-(c) respectively. From Fig. 1.4(c) it is observed that the neutral current contains all order of odd-harmonics with dominant third-order harmonic component.



(a) Three-phase unbalanced source currents



(b) Source neutral current



(c) harmonic spectrum of source neutral current

Fig. 1.4: Three-phase unbalanced source currents, neutral current and harmonic spectrum of source neutral current of a 3P4W system.

As discussed above, unbalanced and non-linear loads on 3P4W system cause excessive neutral current and the problems related to the excessive neutral current are summarized as [14, 15, 17-19]:

- Overloading of distribution feeders and transformers: With four current carrying conductors, the distribution system feeders and transformers may overload and cause additional heat loss.
- Common mode noise: The voltage difference between neutral and ground causes common mode noise in 3P4W power systems. This common mode voltage can result in the malfunction of sensitive electronic equipments.
- Flat-topping of the voltage waveform: The power supplies which produce the harmonic neutral currents have high peak-to-rms current waveforms. Therefore, with the presence of line impedance, “flat-topping’’ of the waveform occurs at the harmonic current frequencies [14]. The power supplies use the peak voltage of the sine wave to keep the capacitors at full charge, reductions in the peak voltage appear as low voltage to the power supply, even though the rms value of the voltage may be normal.
- Wiring failure: In old buildings, load growth with the passage of time makes the size of neutral conductor insufficient and cause wiring failure and poses a fire hazard.

1.5 Solutions to Power Quality Problems in Distribution System

The low quality power affects electricity customers in many ways. The lack of quality power can cause loss of production, damage of equipment or appliances or can even be detrimental to human health. Therefore, it is very important to maintain a high quality of power. Utilities and researchers all over the world have worked for decades on the improvement of what is now known as power quality. There are sets of conventional solutions to the power quality problems, which have existed for a long time. However these conventional solutions use passive elements and do not always respond correctly as the nature of the power system conditions change. The increased power capabilities, ease of control and reduced costs of modern semiconductor devices have made power electronic converters affordable in a large number of applications. New flexible solutions to many power quality problems have become possible with the aid of these power electronic converters.

1.5.1 Reactive Power Compensators

Reactive power compensators or var compensators are used to control and/or regulate the transmission/distribution voltage at a given terminal and to provide power factor correction [6, 20, 21]. Two types of compensation problems are normally encountered in practical applications [21]. The first is the load compensation where the requirements are usually to reduce or cancel the reactive power demand of large and fluctuating industrial

loads, such as electric arc furnaces, rolling mills, phase-controlled rectifiers. The second type of compensation is related to the voltage support of transmission/distribution lines at a given terminal.

In general, var compensators are classified depending on the technology used in their implementation [20]. They are broadly classified as rotating and static var compensators. The first one uses an electro-mechanical power device and the later one uses power electronic technologies to accomplish the task. Again, there are two approaches for the realization of power electronics based var compensators, the one that employs thyristor-switched capacitors and reactors with tap-changing transformers and the other approach uses static inverter circuits [20]. A brief description of the most commonly used reactive power compensators are presented below:

1.5.1.1 Rotating Var Compensators

The rotating var compensator is essentially a synchronous motor operated at no load (or synchronous condenser), shown schematically in Fig. 1.5. The reactive power drawn by a synchronous motor can be continuously controlled by changing its induced voltage (E) and this can be achieved by controlling the excitation of the machine. Increasing E above the amplitude V of the ac system voltage causes leading (capacitive) current to be drawn from the ac system, whereas decreasing E below V produces a lagging (inductive) load on the ac system [20]. For purely reactive power flow the three-phase voltages of synchronous condenser E_1, E_2 and E_3 of the synchronous machine are in phase with the system voltages V_a, V_b and V_c. But, under practical conditions, a small amount of real power flows from the ac system to the machine to supply its mechanical and electrical losses in both operating modes (capacitive and inductive). However, the slow response time (typically a few seconds) and high losses in the machine limit its application as a var compensator. In recent years the rotating var compensators have been practically replaced by the thyristor controlled Static Var Compensators (SVC), as these are much cheaper and have characteristics similar to the rotating var compensators [20].

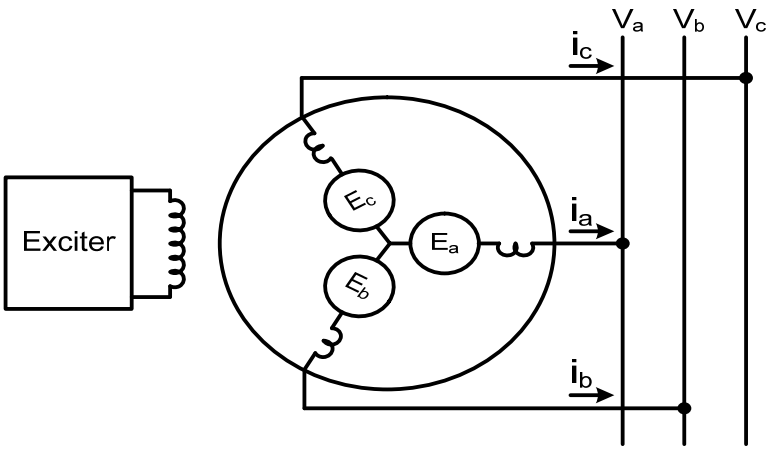


Fig. 1.5: Synchronous machine as var compensator.

1.5.1.2 Thyristor Controlled Static Var Compensators (SVC)

Advances in high power semiconductor and sophisticated electronic control technologies have made the development of thyristor-controlled Static Var Compensators (SVCs) possible [6, 20]. These compensators have been originally developed for arc furnace compensation in the early 1970s, and a few years later they have been adopted for transmission and distribution systems. SVC is essentially a variable impedance type var compensator. Two basic schemes of SVC are available in the literature. The first one controls the leading vars by synchronously switching capacitor banks to the lines; the second one achieves the control of lagging vars with a thyristor-controlled variable inductor. They are named as, Thyristor Switched Capacitors (TSC) and Thyristor Controlled Reactors (TCR), respectively [22, 23].

(a) Thyristor Switched Capacitors (TSC)

The basic idea of thyristor switched shunt capacitors is to split up a capacitor bank into appropriate number of capacitor steps and switch these steps ON and OFF individually using anti-parallel thyristors as switching elements. Fig. 1.6(a) shows the basic scheme.

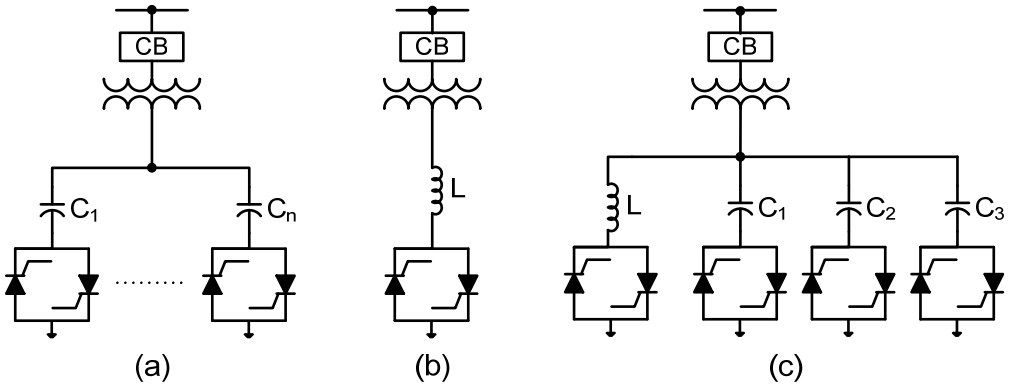


Fig. 1.6: Static var compensators: (a) Thyristor-switched shunt capacitors; (b) Thyristor controlled shunt reactor; (c) Combination of both.

The TSC is characterized by [23]:

- Stepwise control.
- An average one half-cycle (max one-cycle) delay for executing a command from the regulator.
- Practically no transients.
- No generation of harmonics.

(b) Thyristor Controlled Reactors (TCR)

An elementary single-phase thyristor controlled reactor (TCR) is shown in Fig. 1.6(b). It consists of a fixed reactor (usually air-core) of inductance *L* and a bidirectional thyristor switches. The basic idea of TCR is to control the fundamental frequency current component through the reactor by delaying the switching-on instant of the thyristor switch with respect to the voltage across the TCR. The TCR is characterized by [23]:

- Continuous control.
- Maximum one half-cycle delay for executing a command from the regulator.
- Generation of harmonics.

For many applications, a thyristor controlled shunt reactive power control can build-up with a few large steps of TSCs and one or two TCRs is quite attractive. Fig. 1.6(c) combines the favourable properties of the two thyristor schemes discussed above [23]. It provides continuously variable reactive power output from full lagging range to full leading range with good response and reduced harmonic generation.

Despite the simplicity of the thyristor switched static var compensator schemes, its popularity has been hindered by a number of practical disadvantages [6, 22-24]:

- The var compensation is not continuous in all cases.
- Each capacitor bank requires a separate thyristor switch and therefore it is not economical for high-voltage applications unless a step-down transformer is used.
- The steady-state voltage across the non-conducting thyristor switch is twice that of the peak supply voltage.
- The thyristor switch must be rated for, or protected by external means, against line voltage transients and fault currents.
- It occupies a large footprint, high initial and maintenance cost.

1.5.1.3 VAR Generators Employing Static Inverters

The possibility of generating controllable reactive power directly, without the use of large banks of capacitors and bulky inductors, by various switching power inverters has been presented first in 1976 [25]. These approaches employ various dc-to-ac or ac-to-ac converter circuits [6, 20, 24, 26, 27]. Among these, methods employing dc-to-ac converter are more popular and are discussed here [6].

The dc-to-ac converters can be operated as a controllable voltage or current source and produce reactive power essentially without any reactive energy storage elements by circulating the current among the phases of the ac system. Functionally, from the viewpoint of reactive power generation, their operation is similar to that of an ideal synchronous machine [20]. Similar to the synchronous machine, they can also exchange real power with the ac system if supplied from an appropriate energy source. Because of these similarities with synchronous machine, they are termed as Static Synchronous Generator (SSG) or more popularly Static Synchronous Compensator (STATCOM) and these come under the family of shunt connected second generation Flexible AC Transmission System (FACTS) device [6].

In the beginning, inverters were realized with force commutated thyristor switches, but with the remarkable progress of gate commutated semiconductor devices, attention has been focused on self-commutated inverters. These self-commutated inverters can be broadly

categorised into two classes, namely, Voltage Source Inverters (VSI) and Current Source Inverters (CSI) [6, 8, 21, 28, 29]. The VSI shown in Fig. 1.7(a), uses a capacitor with a regulated dc voltage, while the CSI, shown in Fig. 1.7(b) uses a reactor supplied with a regulated dc current.

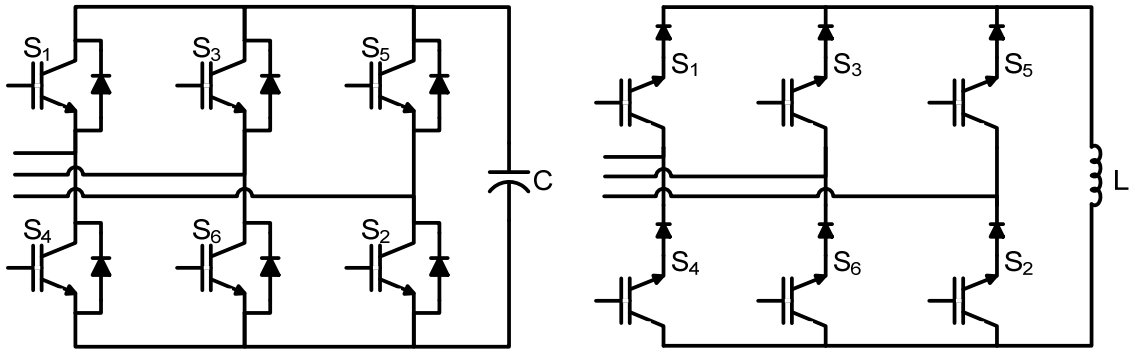


Fig. 1.7: Topologies of inverters: (a) Voltage source inverter; (b) Current source inverter.

Fig. 1.8 shows the basic configuration of a VSI based STATCOM for reactive power compensation. It consists of a VSI connected in shunt to the ac system through a coupling reactor (L_c). In the present discussion, it is assumed that the VSI output voltages are sinusoidal, although the basic operating principles remain valid for any wave shape produced by a practical inverter. For purely reactive power flow the inverter output voltages V_{oa}, V_{ob} and V_{oc} are in phase with the ac system voltages V_a, V_b and V_c respectively. By controlling the amplitude (V_o) of the inverter output voltages, the reactive power can be controlled from full leading to full lagging. By increasing V_o above the amplitude V of the system voltages, causes leading (capacitive) current is drawn from the ac system. On the other hand, decreasing V_o below V results in lagging (inductive) current to be drawn from the ac system [6, 20, 27].

When the inverter is operated strictly as a reactive power source, as described above, it absorbs no real power from the ac system and thus its losses have to be replenished from a separate dc supply. However, the dc supply can be dispensed with if a suitable dc capacitor is used and the inverter output voltage of each phase is made to lag the corresponding ac system phase voltage by a little amount. Under this condition, a real component of current will flow from the ac system to the inverter to replenish its losses [20].

The typical *V–I* characteristics of STATCOM are shown in Fig. 1.9. It is observed from figure that the STATCOM can provide both capacitive and inductive compensation and is able to control its output current in the range spanning from maximum capacitive rating to maximum inductive rating and practically independent of the ac system voltage. Fig. 1.9 also illustrates that the STATCOM has an increased transient rating in both the inductive and capacitive operating regions. The maximum attainable transient current in the capacitive region is determined by the maximum current turn-off capability of the inverter switches. In

the inductive region, the inverter switches are naturally commuted and therefore the transient current rating is limited by the maximum allowable junction temperature of the inverter switches [6].

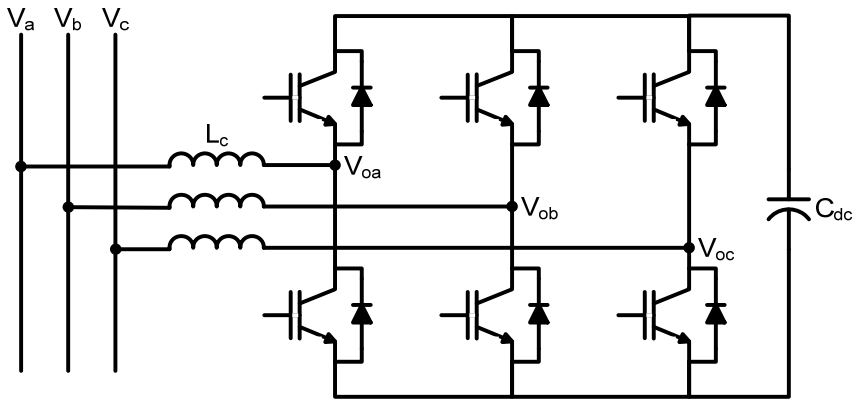


Fig. 1.8: Schematic diagram of a VSI based STATCOM.

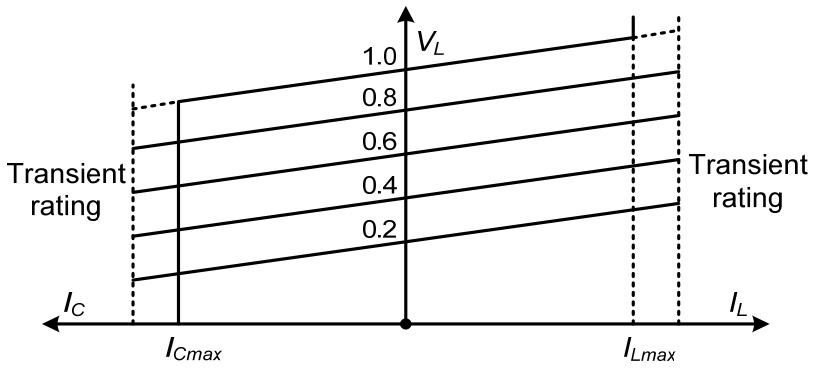


Fig. 1.9: *V–I* characteristics of a STATCOM.

The commercial success of STATCOM is due to their acceptable cost, coupled with desirable technical features such as extremely fast response time, flexibility of control and continuous operation with virtually no maintenance. The principal advantages of STATCOM are the significant reduction in size and the potential reduction in cost achieved from the elimination of a large number of passive components [6, 27]. Because of its smaller size, a STATCOM is well suited for applications where space is a premium. STATCOMs are also used to stabilize transmission systems, improve voltage regulation and compensation of poor power factor. The benefits and drawbacks of the studied topologies are summarized in Table 1.2. The significant advantages of self-commutated device based compensators make them an interesting alternative to improve both compensation characteristics and the performance of ac power system [6].

Table 1.2: Comparison of basic types of shunt var compensators.

Aspect	Synchronous Condenser	SVC		STATCOM
		TCR (with Shunt Capacitors if Necessary)	TSC (with TCR if necessary)	
Accuracy of Compensation	Good	Very Good	Good, very good with TCR	Excellent
Control Flexibility	Good	Very Good	Good, very good with TCR	Excellent
Reactive Power Capability	Leading/ Lagging	Lagging/Leading	Leading/Lagging Indirect	Leading/ Lagging
Control	Continuous	Continuous	Discontinuous (Continuous with TCR)	Continuous
Response time	Slow	Fast, 0.5 to 2 cycles	Fast, 0.5 to 2 cycles	Very fast
Harmonics	Very Good	Very high (filters are needed)	Good (filters are needed with TCR)	Good
Losses	Moderate	Good (less) but increase in lagging mode	Good (less) but increases in leading mode	Very good (least) but increases with switching frequency
Phase Balancing Ability	Limited	Good	Limited	Very good
Cost	High	Moderate	Moderate	Low to moderate

1.5.2 Harmonic Compensation

There are three basic methods for addressing the harmonics in distribution systems and they are:

1. Derating the transformers and oversizing the conductors so that the distribution system can withstand the harmonics [10].
2. Incorporating current waveshaping circuits within the equipment so that they draw sinusoidal currents [30, 31]
3. Installing devices to attenuate or remove the harmonics [32-35].

The first two methods are not cost-effective solutions and the only option is to incorporate filters to remove the harmonics [33]. For reducing the harmonics, passive and/or active filters are used. These filters are either used separately or used in a combined fashion to form a hybrid filter [32-35].

1.5.2.1 Passive Power Filters

Passive filters can be connected either in parallel with the load (shunt passive filter) or in series with the load (series passive filter). Shunt passive filters have traditionally been used to absorb current harmonics in power systems [36]. Shunt passive filters provide low-

impedance paths to divert harmonics to the ground and discourage the flow of harmonics into the power system. There are several types of shunt passive filters: single-tuned, double-tuned, automatically tuned, damped and band-pass filters [4, 36]. Among these shunt passive filter topologies, single-tuned, double-tuned and high-pass damped filters are most commonly used. The tuned filters are designed to exhibit low impedance at one or more harmonic frequencies, while the high-pass damped filters provide low impedance for a wide spectrum of harmonics. The single-phase circuits of a single-tuned, double-tuned and second order high-pass damped shunt passive filters are depicted in Fig. 1.10.

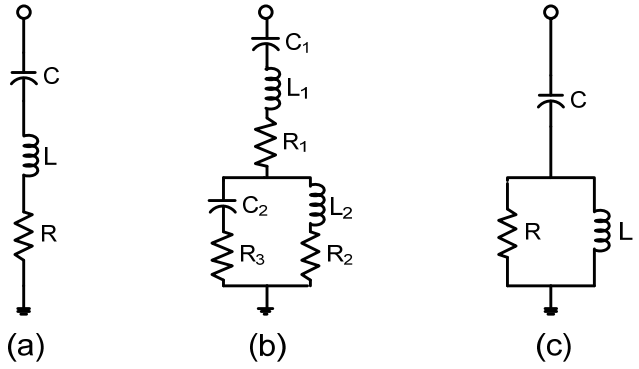


Fig. 1.10: Shunt passive filters: (a) Single-tuned; (b) Double-tuned; (c) Second-order high-pass damped.

Passive filters have hitherto been used in power system because of their advantages which are [36]:

1. Simple implementation, high efficiency and almost maintenance-free operation.
2. A single installation can serve many purposes, i.e., reactive power compensation, voltage support on critical buses and reducing the impact and voltage drop due to the starting of a large motor [36].
3. Implementation at medium power level is possible.

However, passive filters have many problems to discourage their applications and are given below [36, 37]:

1. Passive filters are not suitable for changing system conditions. Once installed, neither the tuned frequency nor the size of the filter can be changed so easily.
2. The filters can either be switched-on or switched-off. Thus, a stepless control of reactive power with enhancement or reduction of load demand is not possible.
3. The source impedance, which is not accurately known and varies with the system configuration, strongly influences the filtering characteristics.
4. The change in the system operating conditions, addition of new compensating devices, aging, deterioration and temperature effects may increase the designed tolerances thereby causing detuning of the filter.
5. The parallel resonance between the system and the filter may cause an amplification of the current at characteristic and noncharacteristic harmonics.

6. Single-tuned or double-tuned filters are not possible to employ for certain loads like cycloconverters or when the power system has inter-harmonics.
7. The outage of a parallel branch can totally alter the resonant frequency, resulting in overstressing of the filter components and increased harmonic distortion.

The design complexity and high cost of losses of the conventional passive filters, as well as their restricted capability to eliminate inter-harmonics and non-characteristic harmonics have encouraged the development of harmonic compensation technique by means of power electronic devices, commonly referred to as active power filters (APF) [32-35, 38-41].

1.5.2.2 Active Power Filters

In the last two decades, considerable progress has been made in Active Power Filters (APFs). Similar to the STATCOM, APFs are inverter circuits, comprising of active devices i.e. semiconductor switches that can be controlled such that the APF can be made to act as harmonic current or voltage generators. Different topologies of APFs have been proposed including shunt, series and the combination of these two [32-34, 39, 40, 42]. However, only the shunt APFs are considered in the present work.

The shunt active power filter acts as a current source and compensates load current harmonics by injecting equal-but opposite harmonic compensating current at the PCC. Fig. 1.11 shows the connection of a shunt active power filter [32, 40].

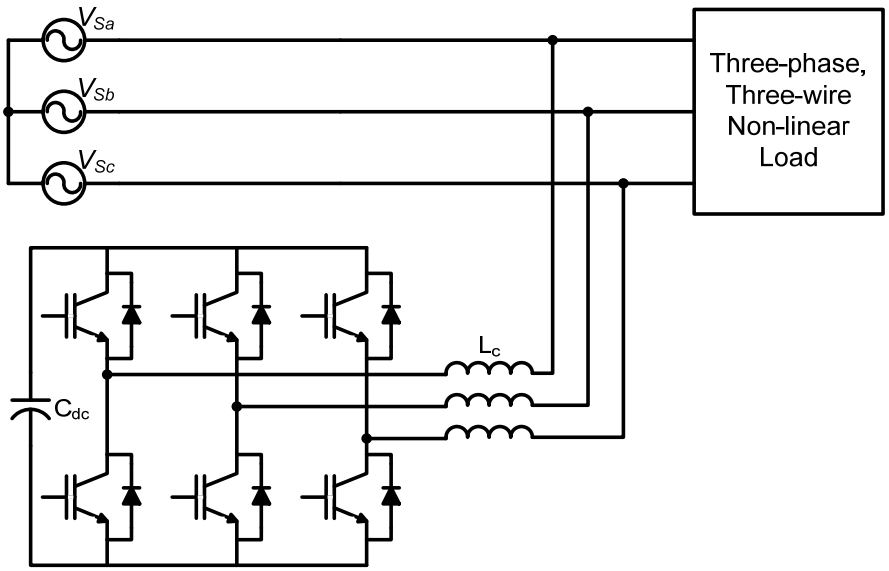


Fig. 1.11: Schematic diagram of a voltage source inverter based shunt active power filter.

The main advantages of APFs are [32-34, 39, 40]:

1. APFs are superior to passive filters in terms of filtering characteristics.
2. A single installation can serve many purposes, i.e. reactive power compensation, flicker mitigation and unbalance compensation.
3. They are compact in size.

4. Non-susceptibility to resonance problem.
5. Step-less control characteristics.

However, high initial cost of active power filters has discouraged their applications in high power systems. To overcome this, the hybrid power filters have been proposed [32, 34, 40, 42] and installed in recent years.

1.5.2.3 Hybrid Power Filters

Hybrid power filters are the combinations of passive and active power filters. Several combinations are possible [32, 34, 42] and a typical combination of shunt passive and shunt active filter topology is shown in Fig. 1.12. Hybrid power filters improve the compensation characteristics of passive filters and allow the use of relatively low rating active power filters in high-power applications at a relatively low cost. Moreover, compensation characteristics of already installed passive filters can be significantly improved by retrofitting an active power filter at its terminals, giving more flexibility to the compensation scheme [32, 34].

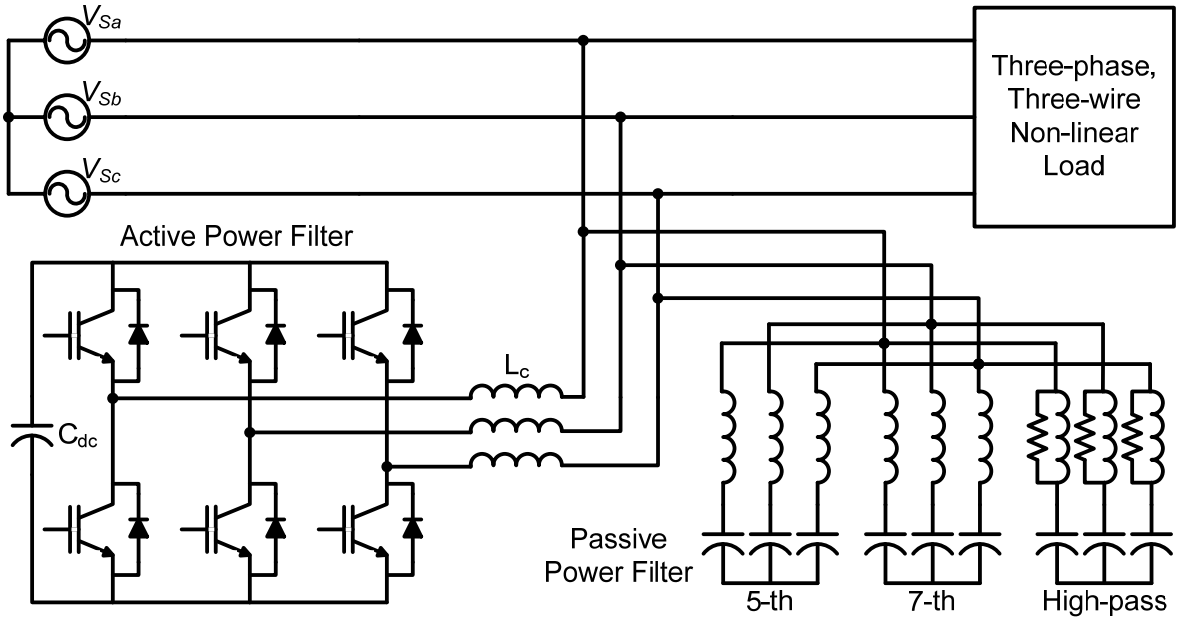


Fig. 1.12: Schematic diagram of a hybrid power filter.

1.5.3 Compensation of Neutral Currents

The high neutral currents in 3P4W system have a detrimental effect on both distribution system and end users. The recommended practices and temporary measures recommended by different agencies to reduce/eliminate the neutral current are given below [14]:

- Over sizing of neutral conductor: Over sizing of neutral conductor is an expensive solution, while the overloading of distribution transformer and feeder remains unaddressed issues.
- Derating of distribution transformer: With non-linear loads, the maximum loading of the transformer should be reduced to below its rated capacity to avoid overheating the distribution transformer and excessive distortion in output voltage.

Derating of transformers for 3P3W and 3P4W power supplies are similar, yet they have significantly different crest factors and neutral current.

- Separate neutral conductors: Use of separate neutral conductors for non-linear loads to avoid shared neutral conductors is also practiced. However, this is almost impossible where loads are widely scattered.

However, the above recommended practices are effective temporary measures but have serious drawbacks such as high cost, complexity in implementation and moreover, overloading of distribution transformers and feeders is still unaddressed. Hence, the only solution for handling these high neutral current is to incorporate the neutral current compensation devices.

There are various approaches reported in the literature for compensating neutral currents such as passive harmonic filters tuned to the zero-sequence harmonics [43], synchronous machine [44], specially designed transformers [45-57]. Details of these methods and their compensation principles are given below.

1.5.3.1 Passive Power Filters

The filtering of neutral current in 3P4W systems has been achieved through the use of single-phase passive filters connected between each phase conductor and the neutral wire [43]. Single-tuned or double-tuned filters tuned to 3^{rd} and/or 9^{th} order harmonic frequencies are normally employed [43]. Passive harmonic filters, although simple, are bulky and expensive. Also, the sensitivity of the components to temperature and aging can result in ineffective filtering as the critical frequencies and the quality factor drift. Another bigger problem is the possibility of exciting a resonance condition with the ac system impedance, which can worsen the situation [36, 37].

1.5.3.2 Synchronous Machine as a Filter

Simultaneous absorption of all the zero-sequence harmonic currents of the neutral conductor using a synchronous machine has been proposed in [44]. By selecting the coil-pitch of the armature winding to 2/3, the zero-sequence reactance of the synchronous machine will reach its minimum value. Therefore, it provides a low impedance path for the zero-sequence harmonic currents. The only limiting factor for absorbing the zero-sequence harmonic currents is the armature resistance of the synchronous machine, which is small. Hence, it is possible to absorb all the zero-sequence harmonic currents by the synchronous machine [44]. Although this method does not require any controller, the high initial and maintenance cost of the synchronous machine limits its application [44].

1.5.3.3 Transformer Based Topologies

Neutral current can be attenuated by taking advantage of the transformer connections that enable cancellation of the zero-sequence components [45, 46]. These transformer

connections provide a low impedance path for zero-sequence harmonic currents. Depending upon the selection of transformer, these currents may circulate in the secondary winding of the transformer or may circulate between load and transformer without entering the utility.

The reported transformer configurations are:

1. Zigzag transformer [45-53]
2. Star-delta transformer [54]
3. T-Connected transformer [55]
4. Scott-connected transformer [56]
5. Star-hexagon transformer [57]
6. Star-polygon transformer [56]

The schematic diagram of the zigzag transformer based topology is illustrated in Fig. 1.13 [45]. In this method the zigzag transformer is connected in parallel and as close as possible to the load. Ideally, the zigzag transformer can be regarded as open-circuited for the positive-sequence and the negative-sequence currents and short-circuited for zero-sequence currents [46]. But in practice the impedance offered for the zero-sequence currents is a function of zero-sequence impedances of the utility system, the neutral conductor and the zigzag transformer [45, 46].

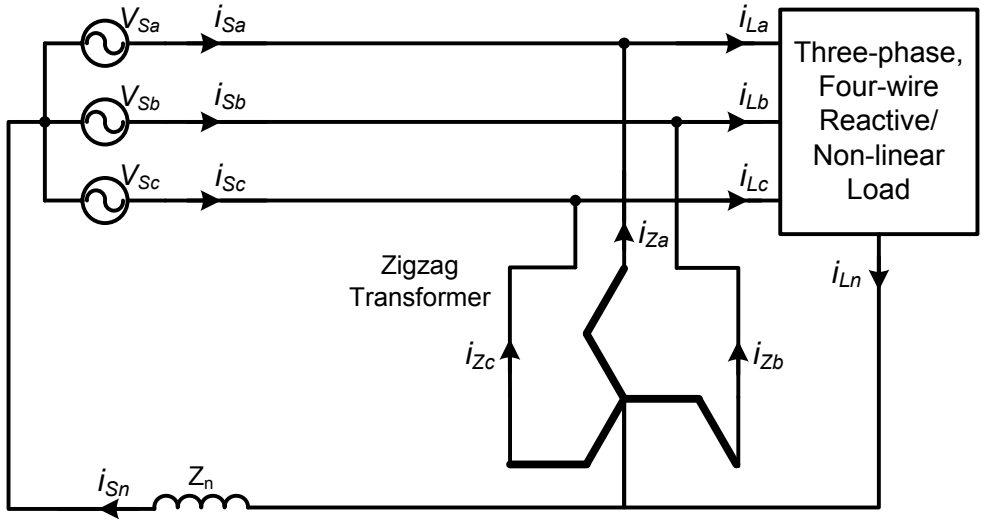


Fig. 1.13: Schematic diagram of a zigzag transformer based compensator for neutral current compensation in 3P4W systems.

Although the transformer based methods can reduce the neural current to a large extent, it will not completely compensate the same [45, 46]. The complete compensation of neutral current is achieved by using a hybrid filter. The main advantages of these hybrid filters are [47, 48]:

1. The effectiveness of the compensator is independent of the zero-sequence impedance of the transformer and the location of its installation.
2. It greatly improves the performance of the compensator with unbalanced/distorted utility voltage conditions.

Several hybrid approaches have been reported in literature and are given below [47-50].

(a) Zigzag transformer with single-phase shunt APF

Fig. 1.14 shows a filtering scheme for compensation of neutral current in 3P4W system [47, 48]. In this hybrid filter topology, a single phase APF is connected between the neutral conductor of the utility and the neutral point of the zigzag transformer. The single phase APF is controlled in such a way that it produces the desired compensating current. These compensating currents are injected through the neutral of the zigzag transformer.

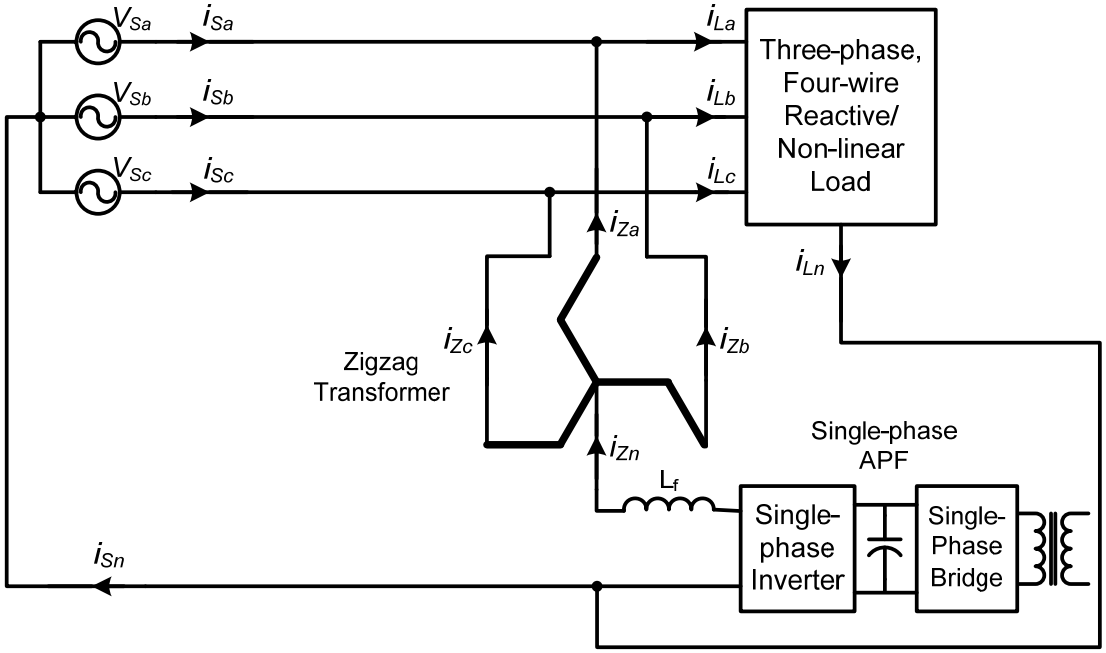


Fig. 1.14: Hybrid scheme for compensation of neutral current in 3P4W systems using zigzag transformer with single-phase shunt APF.

(b) Zigzag transformer with single-phase series APF

Fig. 1.15 shows a filtering scheme for compensation of neutral current in 3P4W system [49, 50]. In this type of hybrid filter topology, a zigzag transformer is connected in parallel with the load and a single-phase PWM APF is connected in series with the neutral conductor. The controlled operation of PWM APF increases the effectiveness of circulation of the neutral current of the load via the zigzag transformer. This series connection of the PWM APF results in significant reduction in kVA rating of the inverter [49, 50] as compared to the scheme shown in Fig. 1.14. This is because of the fact that only the non-zero sequence components of the neutral current flow through the inverter (the zero-sequence component flows through the zigzag transformer). To protect the single-phase APF under abnormal conditions, a switch (*S*) is connected across it [50].

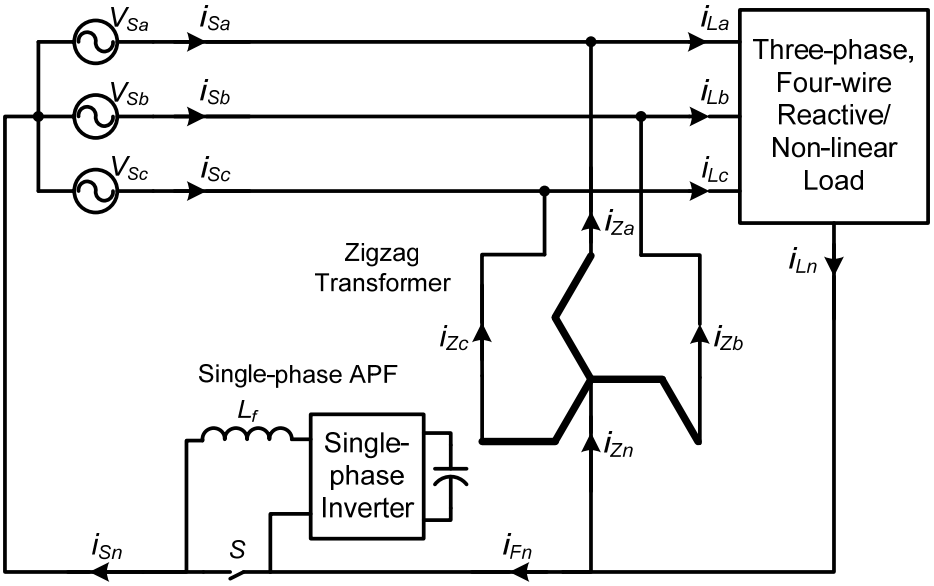


Fig. 1.15: Hybrid scheme for compensation of neutral current in 3P4W systems using zigzag transformer with single-phase series APF.

1.5.4 Power Quality Improvement using D-STATCOM

The conventional power quality mitigation equipment is proving to be inadequate for an increasing number of applications, and this fact has attracted the attention of power engineers to develop dynamic and adjustable solutions to power quality problems. One modern and very promising group of solutions that deals with load current and/or supply voltage imperfections are Custom Power Devices (CPDs) [8, 58, 59]. CPDs solve most of the distribution system problems and can replace the existing compensation devices because of its versatile functionalities thereby reducing the cost. Custom Power is a concept based on the application of power electronic controllers in the distribution system to supply value-added, reliable and high quality power to its customers [58]. Custom power solutions can be categorized as network reconfiguring type or compensating type [7, 8]. The network reconfiguring devices are usually called switchgear and they perform current limiting, circuit breaking and current transferring operations. Network reconfiguring types of custom power devices are Static Current Limiter, Static Circuit Breaker and Static Transfer Switch. The compensating type devices improve the quality of supply voltage and/or current. The compensating types of custom power devices include the Distribution Static Synchronous Compensator (D-STATCOM) [58, 59], Dynamic Voltage Restorer (DVR) [60, 61] and Unified Power Quality Conditioner (UPQC) [62], which are used for compensating the power quality problems in current waveform or voltage waveform or both.

The D-STATCOM is a shunt-connected device, which takes care of the power quality problems in the current waveform [7, 8]. The D-STATCOMs are applicable for both 3P3W and 3P4W systems. The commercial success of D-STATCOM is due to its acceptable cost, coupled with desirable technical features such as extremely fast response time, flexibility of control, continuous operation with virtually no maintenance [7, 8]. The present work exploits

this fact and developed robust computer-controlled D-STATCOM for power quality improvement in 3P3W and 3P4W distribution systems. For completeness and better understanding of the thesis, the compensation principle, topologies and control of D-STATCOM are briefly discussed below.

1.6 Distribution Static Synchronous Compensator

The STATCOM is a vital solution to maintain grid voltages by supplying or consuming reactive power. It has been installed in the transmission grids, and its use is spreading to the medium-voltage distribution grids as a distribution STATCOM (D-STATCOM) [6, 27].

1.6.1 STATCOM in Transmission and Distribution Systems

STATCOMs in both transmission systems and distribution systems have the same structure, but their objectives are different. Some of the primary objectives of a STATCOM in a transmission system are as follows [6]:

- Improvement of transient stability margin by increasing the maximum transmittable power in the transmission line.
- Midpoint voltage regulation for a line segment in order to increase the transmittable power in the transmission system.
- Voltage support at the end of a line requires the compensation of load having poor power factor. This increases the maximum power transmission capability of the transmission line while improving the voltage instability limits.
- Power oscillation damping so that oscillations in the machine angle due to any minor disturbance can be damped out rapidly.

On the other hand, the objectives of these shunt compensators in a distribution system are as given below [7, 8].

- Compensation of poor load power factor such that the current drawn from the source has a unity power factor.
- Suppression of harmonics in loads so that the current drawn from source is sinusoidal.
- Voltage regulation for the loads that cause fluctuations in the supply voltage.
- Cancellation of the effect of unbalance loads so that the current drawn from the source is balanced.

All of these objectives are not necessarily met by a typical STATCOM. The required STATCOM should be designed in view of the needs of compensation parameters.

1.6.2 Basic Compensation Principle of D-STATCOM

The D-STATCOM consists of two distinct main blocks [7, 8].

1. The inverter (power circuit)
2. The D-STATCOM controller

The inverter is responsible for synthesizing the compensating current that should be drawn from the power supply. The D-STATCOM controller is responsible for signal processing in order to determine the compensating currents, which are continuously passed to the inverter. Fig. 1.16 shows the connection of D-STATCOM for reactive and harmonic current compensation in 3P3W distribution system [7, 8, 13]. A voltage source inverter with necessary passive components is used as a D-STATCOM and is connected in parallel at the point-of-common coupling (PCC).

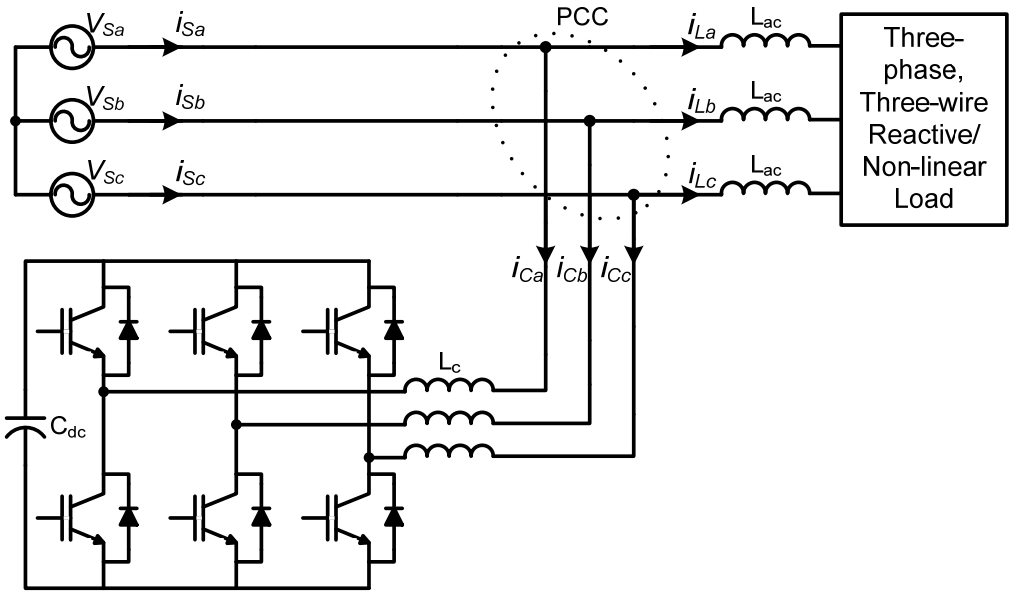


Fig. 1.16: Schematic diagram of a D-STATCOM connected to the 3P3W distribution system for harmonic elimination and reactive power compensation.

To illustrate the compensation principle, Fig. 1.17 depicts voltage and current waveforms of the ac power source v_{Sa}, the source current i_{Sa}, the load current i_{La} and the D-STATCOM current i_{Ca} respectively in the phase–*a*, under the following assumptions: (1) the smoothening reactor L_{dc} on the dc side of the phase-controlled rectifier is large enough to make the dc current constant, (2) the D-STATCOM operates as an ideal controllable current source, and (3) the ac inductor L_{ac} is equal to zero.

The D-STATCOM is controlled to draw the compensating current i_{Da} from the ac power source, such that it cancels the reactive and harmonic current contained in the load current i_{La}. After compensation with D-STATCOM the source current (i_{Sa}) is sinusoidal and in phase with its respective source voltage waveform (v_{Sa}).

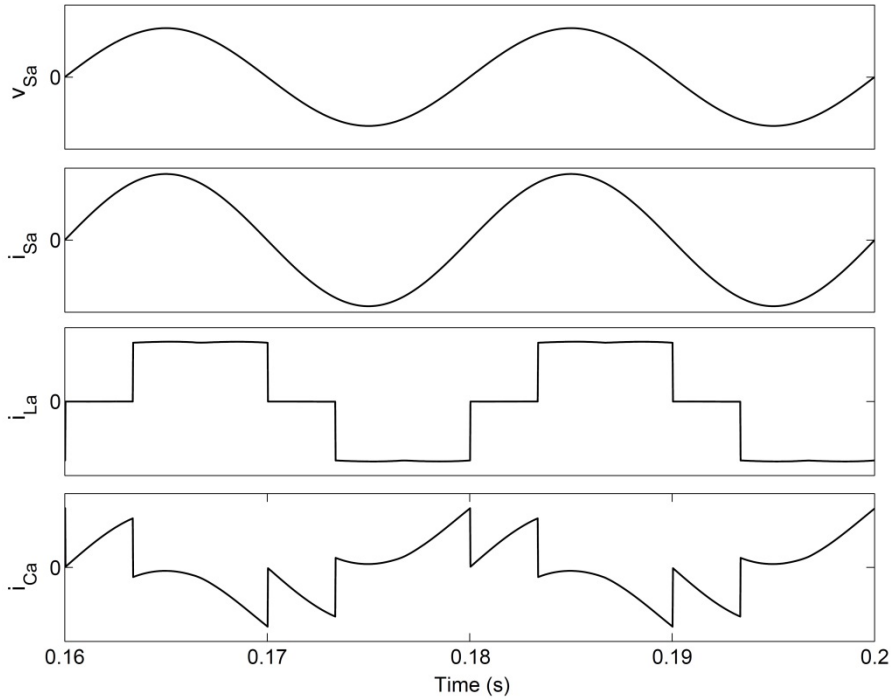


Fig. 1.17: Basic compensation principle of D-STATCOM: phase–*a* waveforms of source voltage, source current after compensation, load current and D-STATCOM current.

1.7 Configurations of D-STATCOM

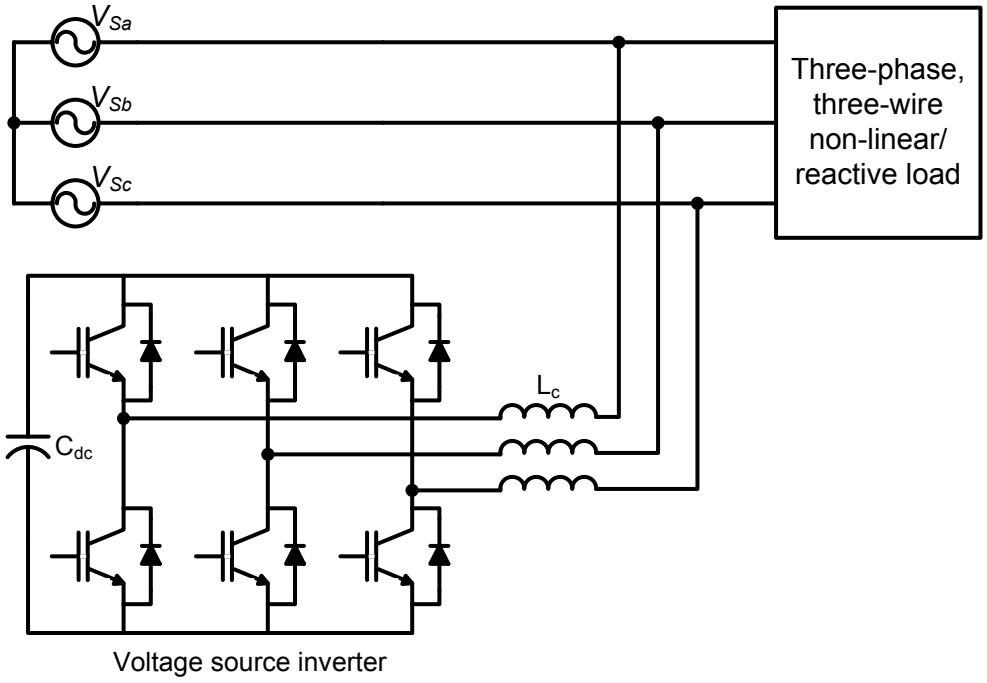
D-STATCOM‘s can be broadly classified based on its power circuit topology and the type of the supply [7, 8, 32, 34, 40] and they are discussed below:

1.7.1 Power Circuit Based Classification

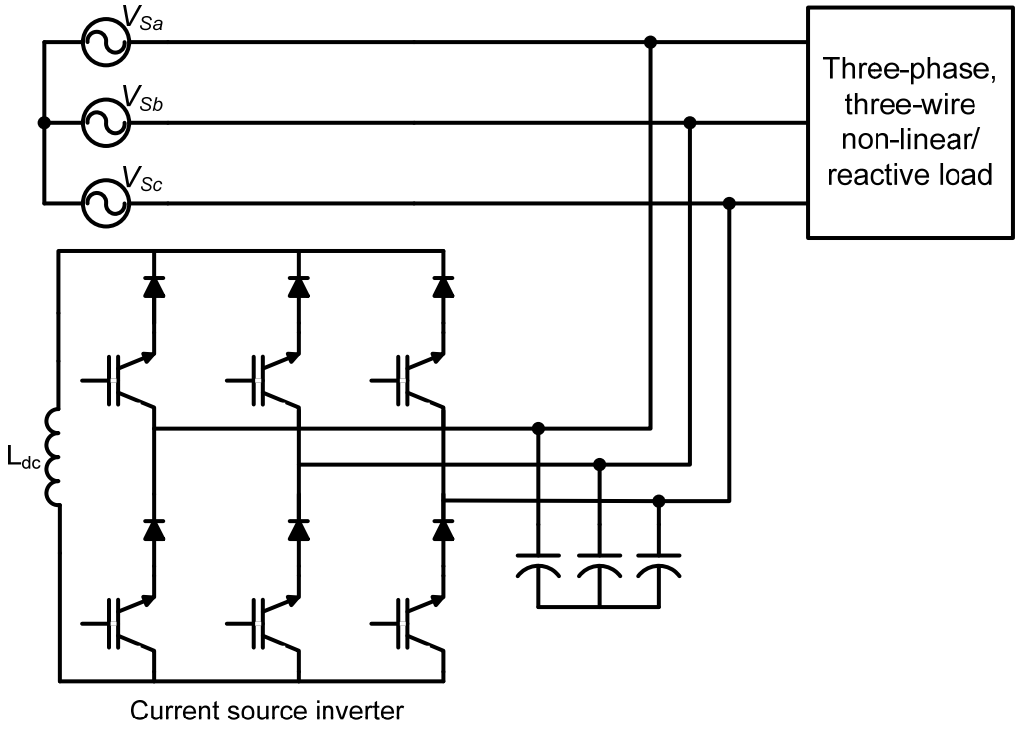
Similar to the STATCOM, the power circuit of D-STATCOM can also be made either with voltage source inverters (VSI) or current source inverters (CSI). The VSI approach shown in Fig. 1.18(a) uses a capacitor with a regulated dc voltage, while the CSI, displayed in Fig. 1.18(b) uses a reactor supplied with a regulated dc current.

However, these simple topologies are not suitable for high-power, medium-voltage applications because of their high harmonic content and increased cost [63]. For high-power, medium-voltage applications, the CSI based D-STATCOMs can be realised using pulsewidth modulated current source inverters (PWM-CSIs) or load commutated inverters (LCIs) [63]. On the other hand, VSI for high-power, medium-voltage applications can be broadly categorized into two groups: multipulse and multilevel type inverters [63-69]. These inverters present great advantages compared with conventional and very well-known two-level VSI [69]. These advantages are fundamentally focused on improvements in the output signal quality and a nominal power increase in the inverter.

In multipulse inverter, several six-pulse inverter units can be arranged using transformers as magnetic interfaces [6, 65, 70, 71], which is a useful technique to achieve high power rating and perform harmonic neutralization. The higher the number of six-pulse units, the lower the distortion of the resultant output voltage.



(a) Voltage source inverter based D-STATCOM



(b) Current source inverter based D-STATCOM

Fig. 1.18: Schematic diagrams of VSI and CSI based D-STATCOMs

The multilevel inverters have become increasingly popular in recent years [63, 66, 68, 69, 72, 73]. It uses the concept of utilizing multiple small voltage levels to perform power conversion. Advantages of this approach include good power quality, good electromagnetic compatibility (EMC), low switching losses and high-voltage capability [68]. They synthesize an output voltage waveform from several levels of capacitor voltage sources. As the number of levels increases, the synthesized output waveform approaches the sinusoidal wave with

the reduced harmonic distortion. At present, three benchmark multilevel inverter topologies have been reported in literature. They are [63, 66-68, 72, 73]:

1. Diode Clamped Multilevel Inverter (DCMLI)
2. Flying Capacitor Multilevel Inverter (FCMLI)
3. Cascade Multilevel Inverters (CMLI)

These three multilevel inverter topologies could be considered now as the classic or traditional multilevel topologies that first made it into real industrial products during the last two decades [63].

1.7.2 Supply System Based Classification

The classification of D-STATCOM can also be based on the supply and/or the load system having single-phase, three-phase three-wire (3P3W) or three-phase four-wire (3P4W) systems.

1.7.2.1 Single-phase D-STATCOMs

The single-phase (two-wire) D-STATCOMs are used for compensation of harmonics and reactive power generated by the operation of non-linear loads, such as domestic appliances, connected to single-phase supply systems. Fig. 1.19 shows the connection of D-STATCOM for reactive and harmonic current compensation in single-phase applications.

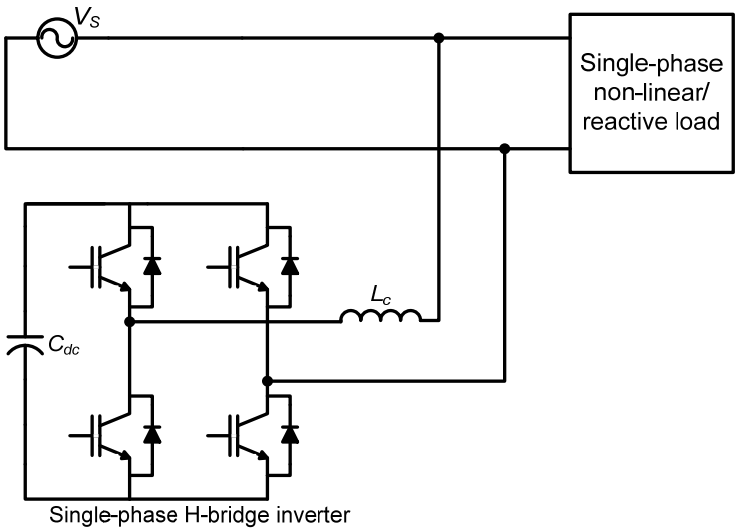


Fig. 1.19: D-STATCOM for two-wire systems.

1.7.2.2 Three-phase, Three-wire D-STATCOMs

In three-phase, three-wire (3P3W) distribution systems, the neutral wire is absent and these systems are used to provide supply for high-power loads such as adjustable speed drives, traction, arc furnaces and other industrial applications. For compensation of harmonics and reactive power in these systems, a 3P3W D-STATCOM is used. Fig. 1.16 shows the connection of D-STATCOM for reactive and harmonic current compensation in 3P3W distribution system.

1.7.2.3 Three-phase, Four-wire D-STATCOMs

D-STATCOMs are specially designed to 3P4W systems for compensating neutral current along with the necessary compensation features of the 3P3W D-STATCOMs [40, 74-76]. Three different topologies are available for 3P4W systems and are given below:

1. Three H-bridge D-STATCOM topology
2. 3P4W capacitor mid-point (or split-capacitor) D-STATCOM topology
3. 3P4W four-leg D-STATCOM topology

1. Three H-bridge D-STATCOM Topology

Fig. 1.20 shows the three H-bridge D-STATCOM topology [76, 77]. It consists of three single-phase full-bridges (H-bridge) with a common dc bus. These H-bridge inverters are connected to the 3P4W system by using three single-phase isolation transformers. Considering the structural advantage of this topology, the control can be done either as a three-phase unit or three separate single-phase units. An independent phase control approach based on single-phase instantaneous reactive power theory is presented in [78].

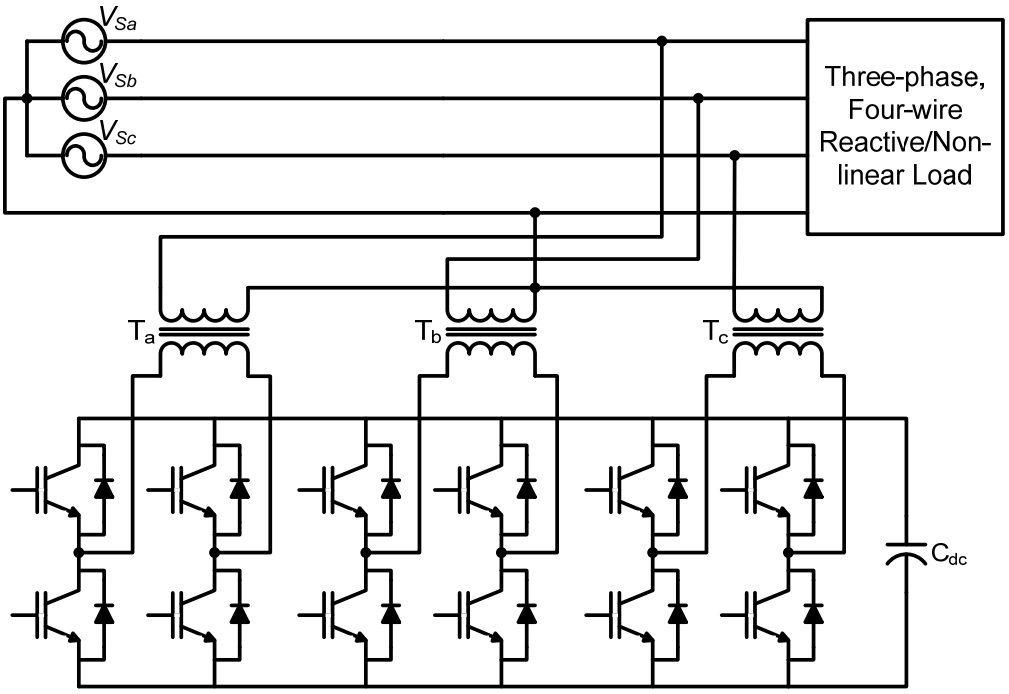


Fig. 1.20: Schematic diagram of a three H-bridge D-STATCOM topology.

In this topology the maximum voltage that appears across each H-bridge is the single-phase voltage and not the three-phase line-to-line voltage, as in the case of split capacitor or four-leg topology. This results into a reduction of dc bus voltage by a factor of $\sqrt{3}$ and thus the reference dc bus voltage needed for proper operation of shunt D-STATCOM also reduces by a maximum factor of $\sqrt{3}$. This, in turn, reduces the rating of inverter [74, 75, 78]. But, the main disadvantage of this topology is the increased number of switching devices.

2. Three-phase, Four-wire Capacitor Mid-point D-STATCOM Topology

The capacitor mid-point D-STATCOM topology utilizes the standard three-phase conventional inverter where the dc capacitor is split and the neutral wire is directly connected to the electrical midpoint of the capacitors through an optional inductance [74, 75]. Fig. 1.21 shows the capacitor mid-point D-STATCOM topology used in 3P4W system. The split capacitors allow load neutral current to flow through one of the dc capacitors $C_{dc1,}$ C_{dc2} and return to the ac neutral wire.

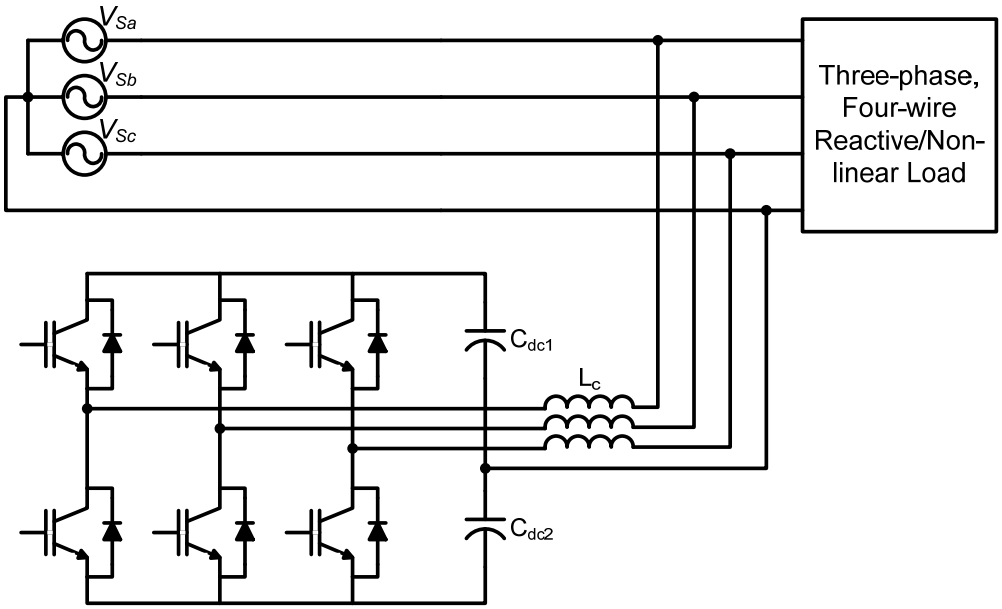


Fig. 1.21: Schematic diagram of a 3P4W capacitor mid-point topology.

3. Three-phase, Four-wire Four-leg D-STATCOM Topology

Fig. 1.22 shows the four-leg D-STATCOM topology used in 3P4W systems [74, 75]. In this topology, three of the switch legs are connected to the three phase conductors through a series inductance while the fourth switch leg is connected to the neutral conductor with an optional inductor. This topology is most suitable for compensation of high neutral currents. Despite having higher number of switching devices this topology, outweighed the split capacitor topology by number of factors, such as [40, 74-76]:

Better controllability: In this topology only one dc-bus voltage needs to be regulated, as opposed to two in the capacitor midpoint topology. This significantly simplifies the control circuitry with better controllability.

Lower dc voltage and current requirement: This topology requires a lower dc-bus voltage and capacitor current.

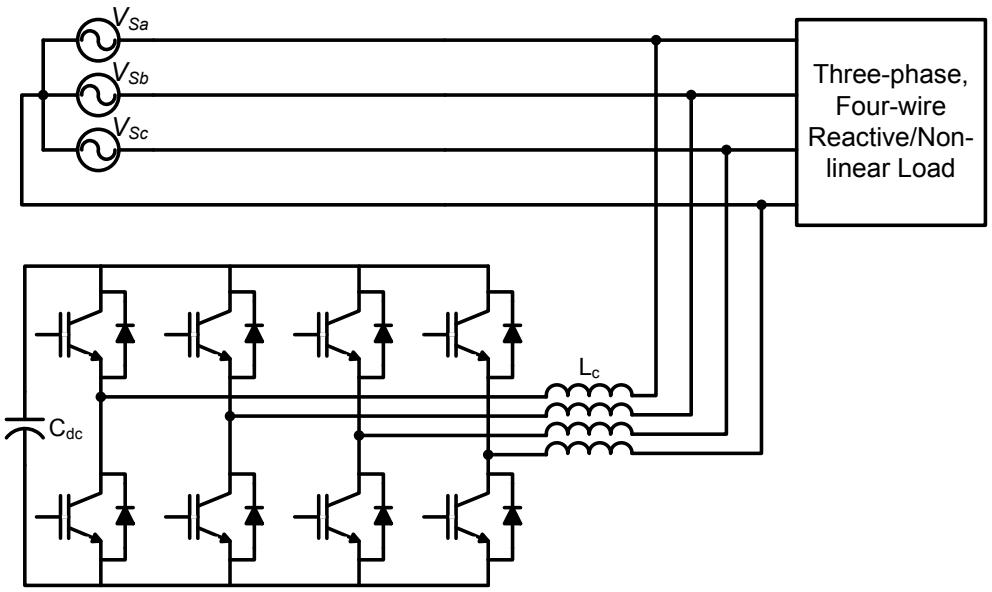


Fig. 1.22: Schematic diagram of a 3P4W four-leg topology.

1.8 D-STATCOM Controller

The effectiveness of the D-STATCOM depends basically on the design characteristics of the controller [13, 79-82].

The control strategy of the D-STATCOM is implemented in three stages and they are:

1. In the first stage, the essential voltage and current signals are sensed using potential transformers (PT's), current transformers (CT's), isolation amplifiers and Hall-effect sensors to gather accurate system information.
2. In the second stage, compensating commands in terms of current or voltage levels are derived based on control methods and D-STATCOM configurations. Based on the operational requirements, type of application, system configuration and loss optimisation, this part of the control scheme calculates the current reference waveforms for each phase of the inverter by maintaining a constant dc bus voltage.
3. In the final stage of control, the controller forces the inverter to draw the desired compensating currents from the source. This part of the control scheme is responsible for generating the gating signals for the solid-state devices of the inverter of D-STATCOM using different current control techniques such as PWM, hysteresis and sliding-mode.

The combined controller of the D-STATCOM is realized using analog and digital devices or advanced microelectronic devices, such as single-chip microcomputers, DSP and FPGA.

1.9 Scope of Work and Author's Contribution

Although the term "power quality" encompasses all disturbances encountered in a power system, it is found that reactive power burden, harmonic currents and unbalanced operation are the most dominant types of power quality problems in modern distribution

systems. In the present work this problem is investigated thoroughly. The solutions based on CPDs for improving the power quality of the distribution systems are discussed in detail. An attempt is made for improving power quality in 3P3W and 3P4W systems with D-STATCOM. The main contributions of the author can be summarized as follows:

- To begin with, a literature survey on available inverter topologies for the realisation of D-STATCOM is presented. Based on this study, single-star bridge cells (SSBC) based modular multilevel inverter is selected as a power circuit for the D-STATCOM. The voltage control methods for chosen inverter are studied and the unequal device conduction periods of level-shift PWM technique is addressed by carrier rotating techniques. In order to prove that the device conduction periods of the adopted carrier rotation techniques are equal, algorithms are proposed to calculate the total conduction period of the each device. Further, simulation studies have also been carried out to investigate the performance of carrier rotating techniques.
- An 11 kV, 1 MVA, 11-level SSBC based transformerless PWM D-STATCOM is designed for 11 kV 3P3W industrial distribution system. This specific design approach does not require a line-frequency transformer and high power switching devices, therefore the cost and size of the D-STATCOM are reduced. The carrier rotation techniques are used for controlling the inverter of D-STATCOM. Extensive simulation study is carried out to examine the effectiveness of the D-STATCOM for harmonic elimination and reactive power compensation with different loads and utility voltage conditions. Various performance indices such as %THD, power factor, active and reactive powers and rating of the D-STATCOM before and after compensation are investigated. Further, the capacitor voltage balance behaviours with carrier rotation techniques are observed.
- To extend the application of D-STATCOM to 3P4W systems, two reduced rating hybrid 3P4W D-STATCOMs are proposed for simultaneous compensation of reactive power, source neutral current and the phase harmonic currents. The complete arrangements considered in these topologies comprise of a 3P3W D-STATCOM, a zigzag-delta or T-connected transformer and a single-phase APF. These hybrid approaches significantly reduce the rating of the overall compensator and improves the performance under non-ideal utility voltage conditions. To show the efficacy of the compensators, extensive simulation studies are carried out.
- In order to further verify the simulation studies of the proposed schemes, a downscaled five-level SSBC based D-STATCOM rated at 100 V, 5 kVA is designed, developed and tested to verify the viability and effectiveness of the carrier rotation techniques, 11 kV, 1 MVA 3P3W D-STATCOM and 3P4W hybrid D-STATCOMs. For this prototype D-STATCOM, IGBTs are selected as the switching devices. The SIMULINK models of the controllers of the D-STATCOM are implemented in real-time

by using real-time workshop (RTW) of MATLAB and real-time interface (RTI) feature of dSPACE. The experimental results are found to be in good agreement with the simulation results.

1.10 Organization of the Thesis

Apart from this chapter, the thesis contains six more chapters and the work included in each chapter is briefly outlined as follows:

CHAPTER 2 starts with an overview of different topologies of inverters used in high-power, medium-voltage systems. Among the available topologies, the SSBC based modular multilevel inverter for the power circuit of D-STATCOM is addressed. The voltage control methods for the chosen inverter are discussed and problem of the unequal device conduction periods of LSPWM technique is addressed by carrier rotating techniques. Further, three algorithms are proposed to verify the effectiveness of the proposed techniques. Simulation results are provided to validate the effectiveness of carrier rotating techniques.

The performance of an 11 kV, 1 MVA SSBC based transformerless PWM D-STATCOM for power quality improvement in 3P3W systems with carrier rotation techniques is investigated in CHAPTER 3. In this chapter, a systematic design procedure for the selection of passive components and generation of reference currents for D-STATCOM are given in detail. Further, simulation results are presented to verify the steady-state and dynamic performance of the D-STATCOM with different load and utility voltage conditions.

CHAPTER 4 is dedicated to the power quality improvement in 3P4W systems. In this chapter two reduced rating hybrid D-STATCOMs are proposed. The controllers for the proposed hybrid D-STATCOMs are discussed in detail. Simulation results are provided to verify the steady-state and dynamic performance of the D-STATCOMs with different load and utility voltage conditions.

The detailed descriptions for the experimental set-ups are given in CHAPTER 5. This includes the explanation of the power circuit, dSPACE based controllers, measuring system and generation of gating signals for the inverter. The chapter concludes with the experimental results and corresponding discussion.

The main conclusions of the presented work and possible future research are summarised in CHAPTER 6.

At the end, the list of references and appendices regarding software and hardware implementations are provided.

CHAPTER 2: PWM INVERTERS FOR D-STATCOM

This chapter describes the available inverter topologies for the realization of D-STATCOM and amongst, the selection of SSBC based modular multilevel inverter for the power circuit of D-STATCOM is addressed. Next, voltage control methods are discussed for the chosen inverter.

2.1 Introduction

High-performance and cost-effective inverters are a prerequisite for the realization of D-STATCOM [8]. With the remarkable progress of gate commutated semiconductor devices, attention has been focused on self-commutated inverters capable of generating or absorbing reactive power without requiring large banks of capacitors or reactors [6]. Depending on the dc-link energy storage component, several approaches are possible including voltage source inverter (VSI) and current source inverter (CSI) [6, 8, 21]. A critical comparison of the performance of VSI and CSI when used as the power converter of D-STATCOM is beyond the scope of this thesis. However, one may prefer CSI due to its robustness or the VSI due to its high efficiency, low initial cost and smaller physical size [28, 29]. Since VSI technology is widely used in industrial applications, this has also been more common in FACTS and CPD applications [8] and hence, VSI is considered in the present work.

2.2 Two-level VSI for High-power, Medium-voltage D-STATCOM Applications

The well-known two-level VSI is also applied for medium- and high-power applications [66]. To achieve the required voltage level of the converter, semi-conductor switches are connected in series. Thus, an inverter leg is comprised of two groups of active switches, each consisting of two or more switches in series, depending on the dc-link voltage. In addition to this, multiple capacitors in series could be necessary to achieve the desired voltage in the dc link [66]. The power circuit of the high-power two-level VSI is shown in Fig. 2.1. In this circuit, each switch is comprised of three semi-conductor devices connected in series and controlled with the same gating signal. In addition, three capacitors are connected in series to cater the desired dc voltage level.

The output voltage of basic two-level VSI with sinusoidal pulsewidth modulation technique (amplitude modulation index = 0.95 and carrier signal frequency = 1 kHz) is shown in Fig. 2.2(a). The harmonic spectrum of the output voltage is shown in Fig. 2.2(b). The output voltage is of quasi-square nature with a THD of 75.26%. The high harmonic content of the output voltage and increased number of switching devices makes this simple inverter impractical for direct use in high-power applications [66, 67].

Instead of using filters to improve the voltage waveform of the basic two-level VSI, several topologies such as multipulse and multilevel inverters are proposed in the literature for high-power, medium-voltage applications using medium-power semiconductor devices [66, 67].

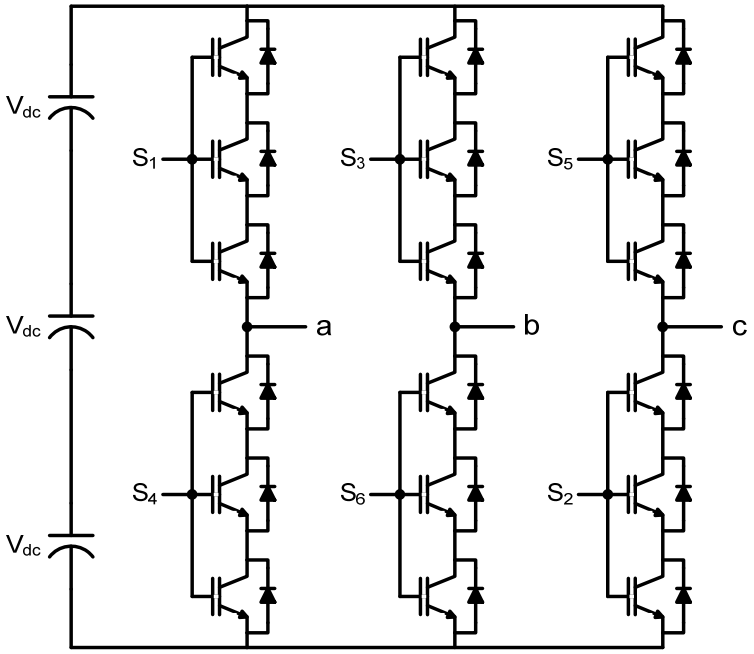
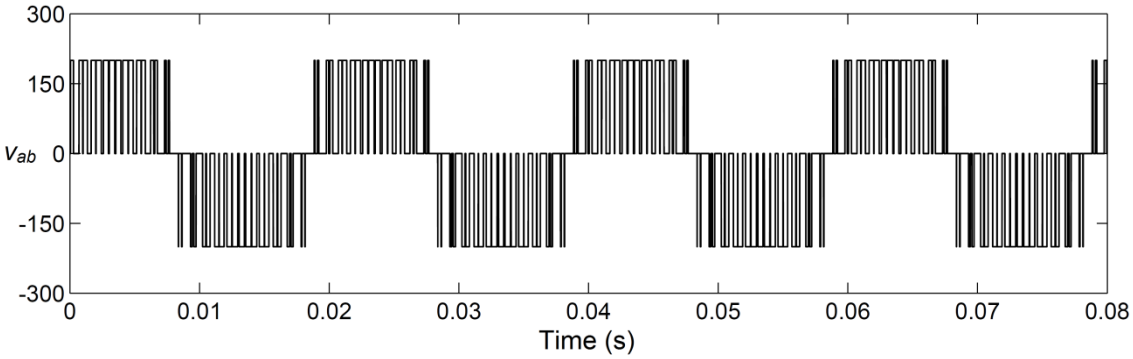
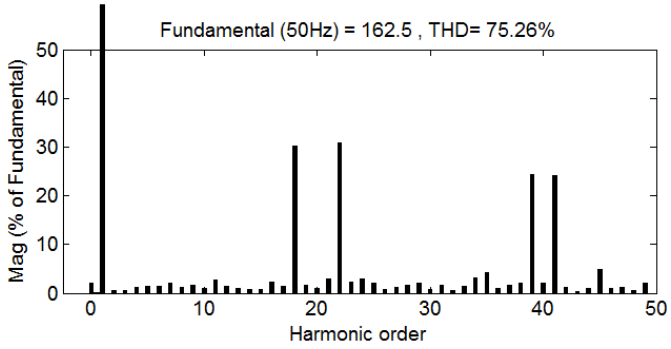


Fig. 2.1: Two-level high-power VSI power circuit.



(a) Line-to-line voltage waveform



(b) Harmonic spectrum

Fig. 2.2: Line-to-line voltage and its harmonic spectrum of a two-level VSI.

2.3 Topologies of VSI used in High-power, Medium-voltage Applications

The different topologies of VSI for high-power, medium-voltage applications can be broadly categorized into two groups: multipulse and multilevel type inverters [64-69]. These inverters present great advantages in comparison with conventional and very well-known two-level VSI [69]. These advantages are primarily reflected on improvements in the output signal quality and a nominal increase in the power rating of the inverter.

2.3.1 Multipulse Inverters

In multipulse inverters, several six-pulse inverter units are arranged as shown in Fig. 2.3, using transformers as magnetic interfaces [6, 65, 70, 71], for achieving high power rating and harmonic neutralization. The higher the number of six-pulse units, the lower is the distortion of the resultant output voltage. For instance, eight six-pulse inverter units can be combined by means of a magnetic interfaces (such as zigzag transformers) to form an equivalent 48-pulse inverter. In this case, the first harmonic order is 47^{th} in the ac voltage and 48^{th} in the dc current [70, 71]. The amplitude of the harmonics decreases as the harmonic order increases. In general, combination of N_P six-pulse inverter units gives rise to a $6N_P$ pulse inverter, In this inverter, all harmonic orders except those at $6kN_P \pm 1$ (where k is any integer) are cancelled in the ac voltage. The corresponding phase difference between two successive inverter units is given by $360°/6N_P$. For transmission line applications, a pulse number of 24 or higher is required [8] to achieve adequate waveform quality without filters.

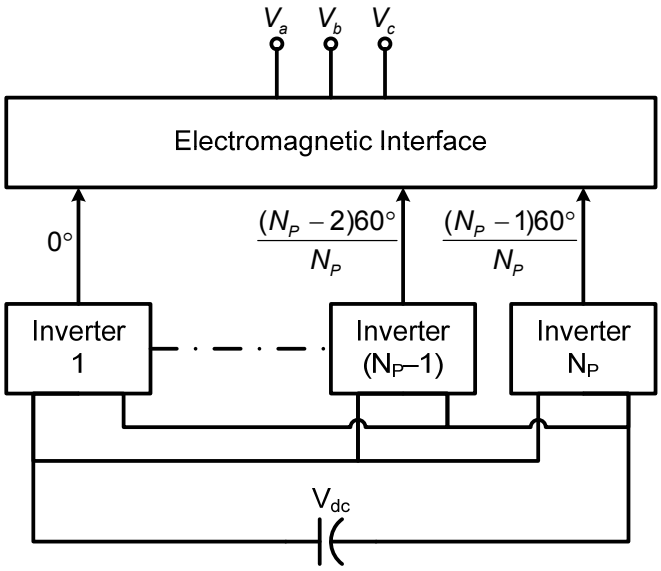


Fig. 2.3: General structure of multipulse inverter.

The main advantage of the multipulse inverter is its low switching losses and reduced input-current harmonics. These features are particularly useful in applications with high-voltage, high-power ratings [6, 70]. However, the complex phase shifting transformers are the main drawbacks of multipulse inverters. These transformers also called harmonic neutralizing magnetics [83]:

(1) are the most expensive equipments in the overall inverter;
(2) produce about 50% of the total losses of the inverter;
(3) occupy up to 40% of the total real estate requirement of the inverter, which is an excessively large area;
(4) cause difficulties in control due to dc magnetizing and surge overvoltage problems resulting from saturation of the transformers in transient conditions;
(5) are prone to failure.

To overcome these drawbacks, the multilevel inverter topologies have been proposed in the literature.

2.3.2 Multilevel Inverters

The multilevel inverters have become increasingly popular in recent years [63, 66, 68, 69, 72, 73]. It uses the concept of aggregating multiple small voltage levels to perform power conversion at an appropriate high-voltage level. Advantages of this approach include good power quality, good electromagnetic compatibility (EMC), low switching losses and high-voltage capability [68]. They synthesize an output voltage waveform by aggregating several levels of capacitor voltages. As the number of levels increases, the synthesized output waveform approaches the sinusoidal wave with the reduced harmonic distortion. However, high number of voltage levels increases control complexity and introduces voltage imbalance problems. Multilevel inverters are considered today as a very attractive solution for high-power, medium-voltage applications, because of the following advantages [63, 66, 68, 69, 72, 73]:

(1) they can generate output voltages with medium-power semiconductor technology with lower distortion and dv/dt.

(2) they draw input current with very low distortion.

(3) they generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.

(4) they can operate with a lower switching frequency.

(5) they are fault tolerant, less prone to failure and their cost is relatively low.

Because of the above advantages, in the present work, multilevel inverter is considered over multipulse inverter. The topologies and modulation methods of multilevel inverters are discussed in the next section.

2.4 Multilevel Inverter Topologies

At present, there are three benchmark multilevel inverter topologies reported in the literature. They are [63, 66-68, 72, 73]:

1. Diode Clamped Multilevel Inverter (DCMLI)
2. Flying Capacitor Multilevel Inverter (FCMLI)
3. Cascade multilevel Inverters (CMLI)

These three could be considered now as the classic or traditional multilevel topologies which have been introduced into real industrial products during the last three decades [63, 66-68]. New multilevel inverter topologies have also been proposed in the literature and most of them are derived from these classical multilevel topologies [63]. However, not so many have made their way to the industry yet. The operating principles, generation of multilevel voltage waveform, characteristics, modulation schemes, applications and other information

related to the DCMLI, FCMLI and CMLI can be found from the previous works in [63, 66-68, 72, 73]. A brief description of these topologies is given below:

2.4.1 Diode Clamped Multilevel Inverter (DCMLI)

The diode clamped multilevel inverter (DCMLI) has been proposed in [84] and can be considered as the first real multilevel inverter. The DCMLI employs clamping diodes and cascaded dc capacitors to produce ac voltage waveforms with multiple levels [84, 85]. The inverter can be generally configured as a three, four, or five-level topology, but only the three-level inverter, often known as neutral-point clamped (NPC) inverter, has found wide application in high-power medium-voltage systems [84, 85].

Fig. 2.4 shows the simplified circuit diagram of a five-level DCMLI [86]. In Fig. 2.4, each phase-leg of the inverter is composed of eight active switches (with antiparallel diodes) from S_1 to S'_4. In practice, either IGBT or IGCT can be employed as a switching device. The upper and lower switches of each phase-leg form complementary pairs as (S_1, S'_1), (S_2, S'_2), (S_3, S'_3) and (S_4, S'_4).

On the dc side of the inverter, the dc bus capacitor is split into four parts, and provides a neutral point *O*. The voltage across each of the dc capacitor is (V_{dc}), which is normally equal to one fourth of the total dc voltage ($4V_{dc}$). The diodes, connected to the dc bus capacitors are called 'clamping diodes', which limits the voltage stress across each device to V_{dc}.

The DCMLI are most widely accepted topology in medium-voltage drives and are best suitable for back-to-back regenerative applications [63, 66]. Particularly, three-level DCMLI based applications have become quite popular because of a simple transformer rectifier power circuit structure, with a lower device count and less number of capacitors. Although the DCMLI structure can be extended to higher number of levels, these are less attractive because of higher losses and uneven distribution of losses in the outer and inner devices [66]. In particular, the clamping diodes, which have to be connected in series to block the higher voltages, introduce more conduction losses and produce reverse recovery currents during commutation that affect the switching losses of the other devices even more. Furthermore, balancing of dc-link capacitor voltage becomes unattainable in higher level topologies with applications such as D-STATCOM, APF and DVR.

The drawbacks of the DCMLI are the unequal loss distribution and the resulting uneven temperature distribution [87]. Since the semiconductors are cooled with separate heat sinks and cooling systems, it results in an uneven semiconductor-junction temperature distribution, which affects the cooling system design and limits the maximum power rating, output current and switching frequency of the inverter [63]. The unequal loss distribution can be substantially improved by replacing the neutral clamping diodes with clamping switches. With clamping switches, the current can be forced to go through the upper or lower clamping path. This can be used to control the power loss distribution and overcome the limitations of the

DCMLI, enabling substantially higher power rating. These additional devices are called active neutral clamping switches, as shown in Fig. 2.5, which gives this inverter its name of active neutral point clamped (ANPC) or active diode-clamped multilevel inverter (ADCMLI) [87]. However, these advantages come at the expense of a more complex circuit structure and the need to control the additional switching devices.

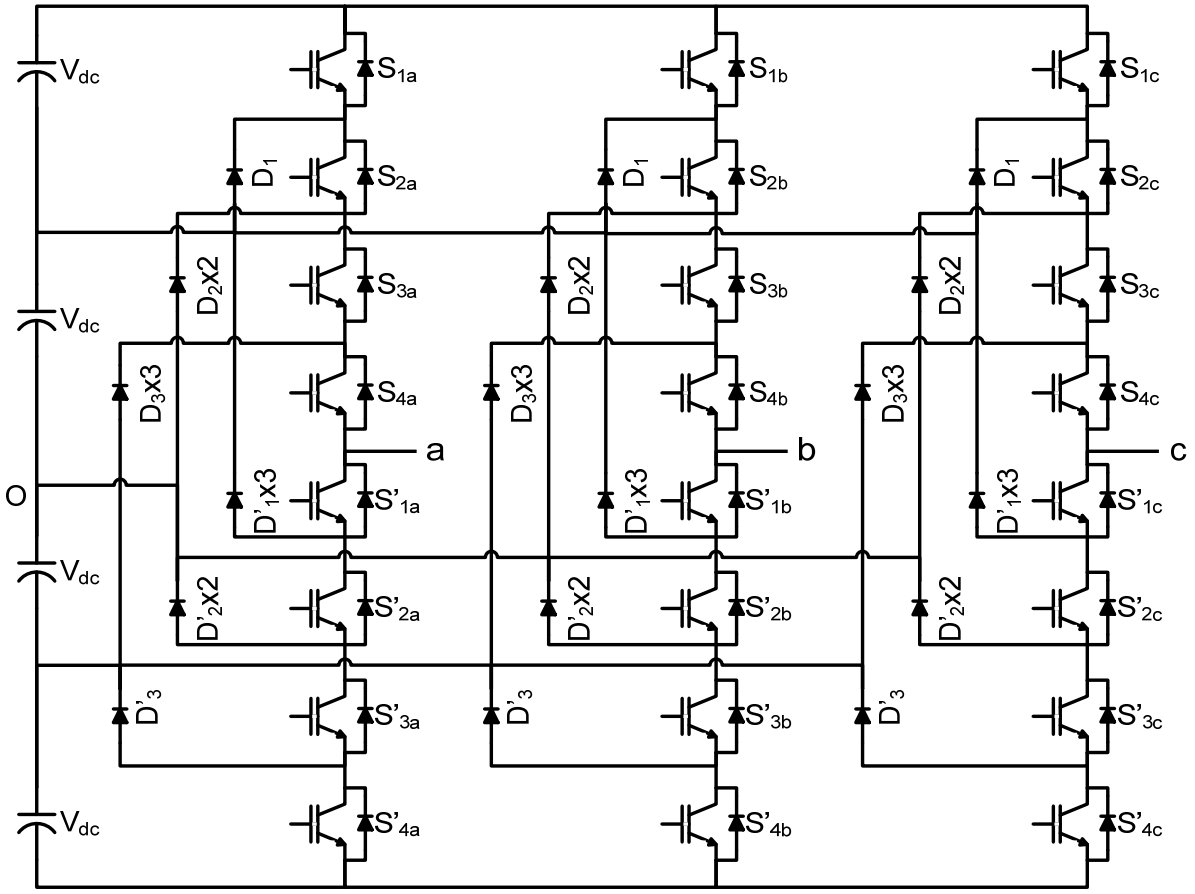


Fig. 2.4: Three-phase five-level diode clamped multilevel inverter.

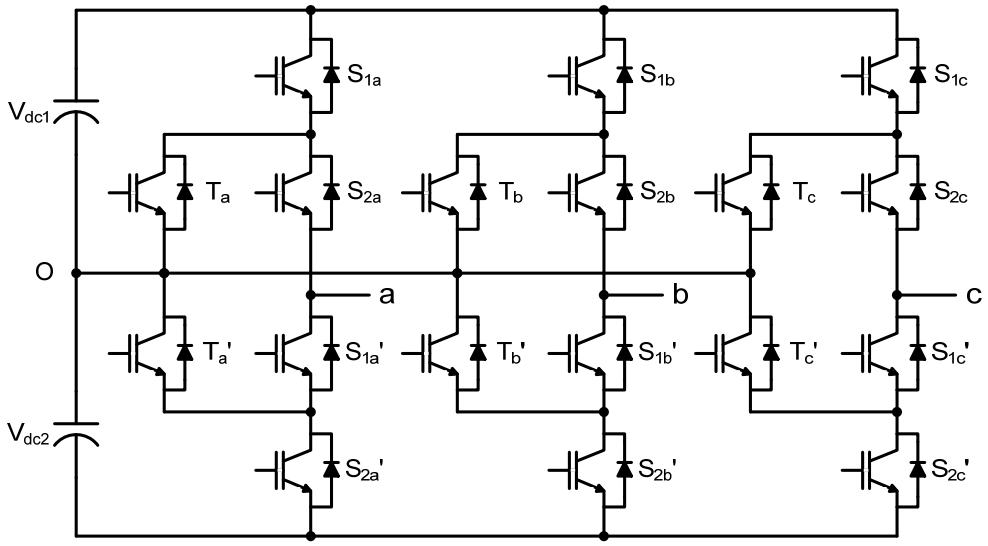


Fig. 2.5: Three-phase three-level active diode clamped multilevel inverter.

2.4.2 Flying Capacitor Multilevel Inverter (FCMLI)

Another fundamental multilevel topology, the flying capacitor inverter, involves a series connection of capacitor switching cells [72, 88, 89]. This topology has several unique and attractive features when compared to the DCMLI. One feature is that clamping diodes as required in DCMLI are not needed. Furthermore, the FCMLI has a switching redundancy within a phase, which can be used to balance the voltages of the flying capacitors (C_F) and equally distribute the switching and conduction losses of the semiconductor switches [90, 91]. The circuit configuration of a five-level FCMLI is depicted in Fig. 2.6.

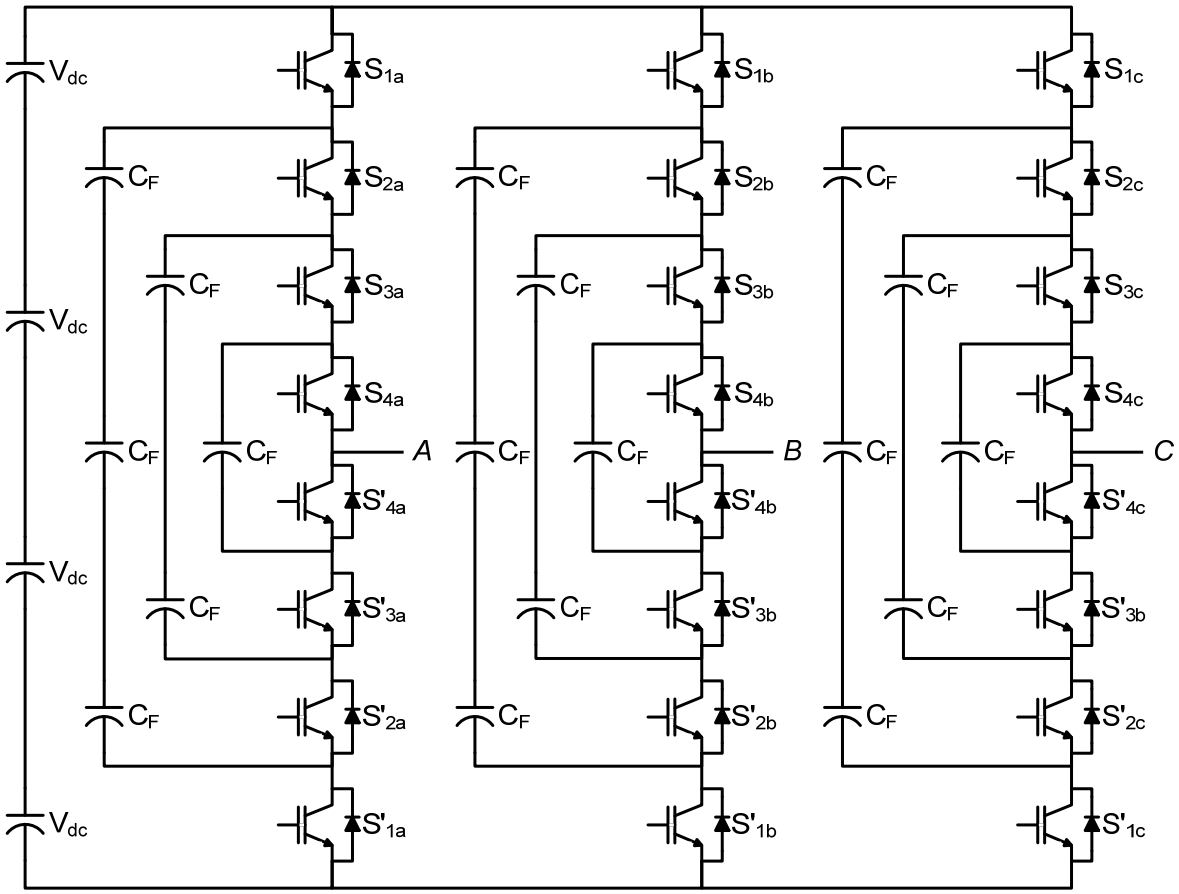


Fig. 2.6: Three-phase five-level flying-capacitor multilevel inverter.

In summary, advantages and disadvantages of a FCMLI converter are as follows [72, 88, 89, 91].

- Modular in structure and the number of levels can be increased to any arbitrary value.
- Large number of capacitors provide extra ride through capabilities during power outage [72].
- The switching state redundancy provides a great flexibility for the design of the switching pattern and natural balancing of capacitor voltages [90, 91].
- Reconfiguration of circuit is possible during fault or under-rated conditions [92].
- An excessive number of storage capacitors are required when the number of inverter levels is high. High-level systems are more difficult to package and more expensive with the required bulky capacitors [69].

- Capacitors voltages have to be pre-charged at startup to a value which are close to their nominal values [66, 68].

The above disadvantages make this inverter limited to medium-voltage, high-power applications. However, FCMLI have found particular applications for high bandwidth–high switching frequency applications such as medium-voltage traction drives [72].

2.4.3 Cascaded Multilevel Inverters (CMLI)

The CMLI appeared first in 1988 [89], matured during the 1990s and gained more attention after 1997 [83, 93]. The CMLI family is characterized by cascade connection of modular chopper-cells or H-bridge cells to form each cluster or arm. This brings flexibility to circuit design, and results in low-voltage steps. The CMLI with H-bridge cells are known as Cascade H-bridge (CHB) multilevel inverters and on the other hand, CMLI composed with bidirectional chopper cells are known as Modular Multilevel Inverters (MMI). However, the common concepts hidden in the family members are both “modular” structure and “cascade” connection. These concepts allow power electronics engineers to use the common term “Modular Multilevel Cascade Inverter (MMCI)” as a family name [94]. Hereafter in this thesis these inverters are referred as modular multilevel cascade inverters.

The MMCI is one of the next-generation multilevel Inverters intended for high or medium-voltage power conversion without line-frequency transformers [94]. The family of MMCI consists of following members [94]:

1. Single-star bridge cells (SSBCs);
2. Single-delta bridge cells (SDBCs);
3. Double-star chopper cells (DSCCs);
4. Double-star bridge cells (DSBCs).

The major advantages of MMCI are [94]:

- They can achieve high or medium-voltage power levels with mature low-voltage semi-conductor devices.
- They can easily expand to the higher number of levels with easy construction, flexibility in converter design [95].
- A direct connection to the system is possible by eliminating the line-frequency transformer. This is particularly advantageous as the existence of the transformer makes the converter heavy and bulky [96], and also induces a dc magnetic flux deviation during single-line-to-ground faults [97].

Among the members of MMCI, SSBC and SDBC are particularly suitable for applications such as Static Synchronous Compensator (STATCOM), Battery Energy Storage System (BESS) and Dynamic Voltage Restorer (DVR) [63, 83, 94, 98-102]. In SSBC and SDBC based inverters, each cell includes a single-phase H-bridge cell and an independent or isolated voltage source provided by floating capacitors or transformer secondaries or

batteries. The resulting phase voltage is synthesized by the addition of the voltages generated by the different H-bridge inverters. Fig. 2.7 and Fig. 2.8 show the following two circuit configurations, respectively: the single-star bridge cells (SSBC) and the single-delta bridge cells (SDBC). The reason for such nomenclature is that both are based on three strings of multiple H-bridge cells with either star or delta connection.

The number of levels (m) in phase voltages of a SSBC or SDBC based inverter with N number of H-bridge cells per phase leg can be found from equation (2.1).

$$m = 2N + 1 \tag{2.1}$$

For MMCI, m is always an odd number while in other multilevel topologies such as DCMLI and FCMLI, it can be either an even or odd number. Table 2.1 lists all the voltage levels and their corresponding switching states to synthesize five-level voltages across phase–*a* and *O*. It should be noted that some voltage levels can be obtained by more than one switching combination. In Table 2.1, V_{dc} is the voltage across the capacitor of an H-bridge cell.

Table 2.1: Voltage levels and their corresponding switch states for a five-level SSBC or SDBC based inverter.

Output Voltage	Switch State (1 means switch is ON and 0 means OFF)							
	S_{11}	S_{31}	S_{12}	S_{32}	S_{41}	S_{21}	S_{42}	S_{22}
$V_{AO} = +2V_{dc}$	1	1	1	1	0	0	0	0
$V_{AO} = +V_{dc}$	1	1	1	0	0	0	0	1
	0	1	1	1	1	0	0	0
	1	0	1	1	0	1	0	0
	1	1	0	1	0	0	1	0
$V_{AO} = 0$	1	1	0	0	0	0	1	1
	0	0	1	1	1	1	0	0
	1	0	0	1	0	1	1	0
	0	1	1	0	1	0	0	1
	1	0	1	0	0	1	0	1
	0	1	0	1	1	0	1	0
$V_{AO} = -V_{dc}$	1	0	0	0	0	1	1	1
	0	1	0	0	1	0	1	1
	0	0	1	0	1	1	0	1
	0	0	0	1	1	1	1	0
$V_{AO} = -2V_{dc}$	0	0	0	0	1	1	1	1

More recently, SSBC inverters with unequal dc source, also known as hybrid or asymmetric cascaded inverters have been introduced [66, 100, 103]. The circuit configuration of the topology for a five-level SSBC inverter with unequal dc sources is very similar to the regular SSBC shown in Fig. 2.7, the difference is that the isolated dc sources have different values. When choosing unequal dc sources, some switching-state redundancies are avoided, and more different output-voltage levels are generated with the

same number of power cells. This reduces the size and cost of the inverter and improves reliability. An additional advantage is that the inverter can be controlled appropriately to reduce the switching losses, which is very important in high-power applications [103].

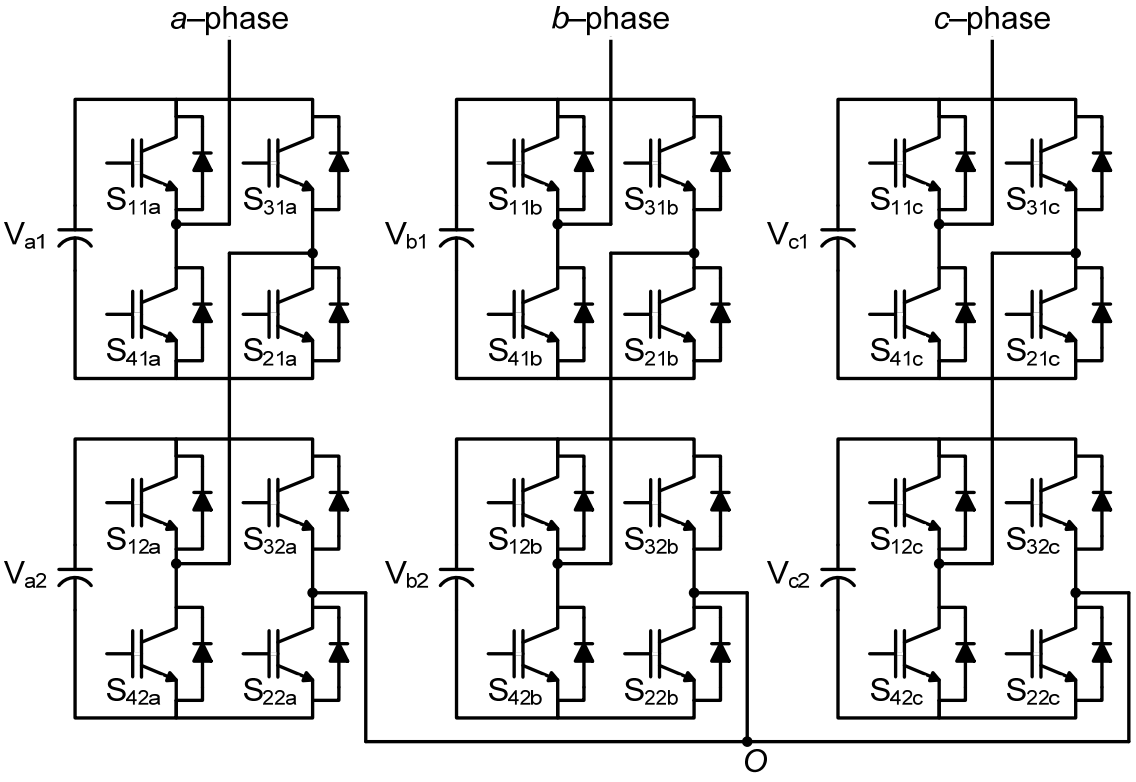


Fig. 2.7: Three-phase five-level single-star bridge cells based modular multilevel inverter.

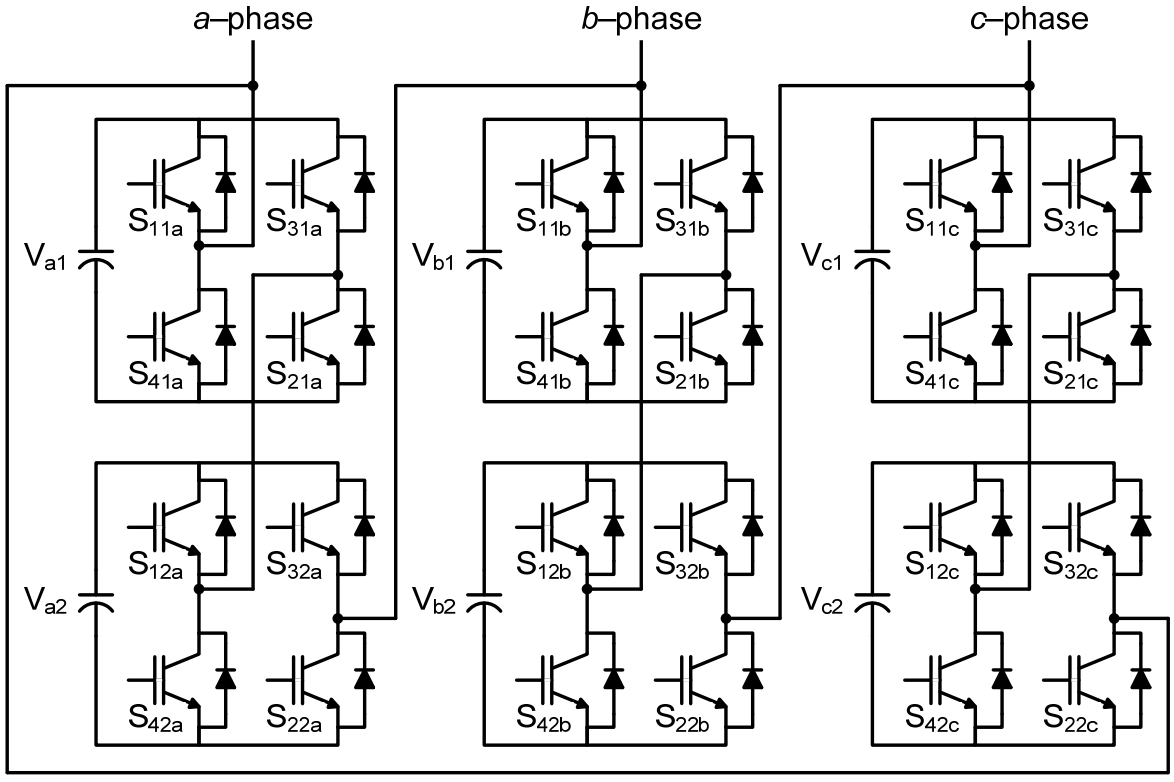


Fig. 2.8: Three-phase five-level single-delta bridge cells based modular multilevel inverter.

The main drawback of this inverter is that the modularity and switching redundancy of the inverter are lost, since the different power ratings of the cells force special design for each power cell (even different power-device families could be needed). In addition [103], no input-current harmonic cancellation can be achieved, since the power asymmetry disables the multipulse rectifier and transformer function. In summary, advantages and disadvantages of a SSBC or SDBC based inverters are as follows [63, 94, 100, 104].

- Requires the least number of components among all multilevel inverter configurations to achieve the same number of voltage levels.
- Modularized circuit layout and packaging is possible because each level has same structure, and there are no extra clamping diodes or voltage balancing capacitors.
- Provides switch combination redundancy for a natural voltage balancing of capacitors.
- Reconfiguration of circuit is possible during under-rated or fault conditions.
- Needs separate dc sources for power conversions.

2.5 Comparative Evaluation of Multilevel Inverters for D-STATCOM

The selection of individual inverter topologies for D-STATCOM applications depends on their performance, cost, size and implementation factors. Table 2.2 gives the comparison of power component required per phase-leg for the above discussed multilevel inverter topologies. From Table 2.2, it can be observed that the SSBC or SDBC inverter requires least number of power components.

Table 2.2: Comparison of power component requirements per phase-leg among multilevel inverter topologies.

Power component	Inverter topology		
	DCMLI	FCMLI	SSBC or SDBC
Main switching devices	$2(m-1)$	$2(m-1)$	$2(m-1)$
Anti-parallel diodes	$2(m-1)$	$2(m-1)$	$2(m-1)$
Clamping diodes	$(m-1)(m-2)$	0	0
DC bus capacitors	$(m-1)$	$(m-1)$	$\frac{(m-1)}{2}$
Flying capacitors	0	$\frac{(m-1)(m-2)}{2}$	0

Table 2.3 gives the comparison of multilevel inverter topologies based on their implementation factors [63, 66-69, 72, 85, 100, 105, 106]. Although FCMLI have a natural voltage balancing operation and modular structure [91], but its application as a D-STATCOM is limited due to the requirement of large number of capacitors and their initialization process (pre-charge) [63].

On the other hand, the SSBC, SDBC and DCMLI topologies seem to be the most suited for D-STATCOM applications. But, the requirement of a large number of power components and voltage unbalance problem at higher levels limits the DCMLI for low power rating applications [105, 106]. The requirement of least number of components, modular structure, high fault tolerance ability and absence of complex input transformer as well as non-initialization of the capacitor voltages makes SSBC and SDBC best suited for D-STATCOM and other custom power applications. SSBC and SDBC can reach higher output voltage and power levels (13.8 kV, 30 MVA) and achieves higher level of reliability due to its modular topology [100]. Table 2.4 summarizes the comparisons among SSBC and SDBC based inverters from various points of view [94].

The “cell-count ratio” in Table 2.4 indicates the ratio of the cell count of each MMCI member to that of the SSBC under the assumptions that the IGBTs used in the four MMCI members have the same blocking voltage, and both members have the same power and voltage ratings. As a result, the IGBTs have different current ratings because the count of the IGBTs is different in SSBC and SDBC. The “practicability” in Table 2.4 includes technical aspects as well as the market size of each member. From Table 2.4 it is observed that applications of the SSBC can be made at the lowest cost because SSBC has fewer cell count ratio than SDBC [94].

Table 2.3: Comparison of multilevel inverter topologies based on implementation factors.

Implementation factor	Inverter topology		
	DCMLI	FCMLI	SSBC or SDBC
Specific requirements	Clamping diodes	Additional capacitors and their initialization	Isolated dc sources
Modularity	Low	High	Very high
Design and implementation complexity	Low	Medium	Least (with transformer-less applications)
Control concerns	Voltage balancing	Voltage setup	Power sharing
Fault tolerance	Difficult	Easy	Easy
Applications	CSDs, ASDs, conveyors, marine applications and regenerative applications such as mining and renewable energy.	ASDs, medium-voltage traction drives.	FACTS, CSDs, High-power ASDs, electric and hybrid vehicles, photovoltaic power conversion, UPSs and magnetic resonance imaging.
Cost [67, 105, 106]	Low (3-level), high (>= 4-level).	Medium (3-level), high (>= 4-level).	Very low (transformer-less applications), high (input transformer applications).
Available commercial ratings [63, 66]	2.3 to 6.6 kV, 3.7 to 44 MVA.	2.3 to 4.16 kV, 2.24 to 8 MVA.	2.3 to 13.8 kV, 6.2 to 120 MVA.

Table 2.4: Comparison of SSBC and SDBC topologies.

Terminology	SSBC	SDBC
Main objectives	Positive-sequence reactive and/or active power	Negative-sequence reactive and/or active power
Cell-count ratio	1	$\sqrt{3}$
Circulating current	No	One degree of freedom
Grid inductor	Yes	Yes
Motor drives	No, but limited expectations exist	No, but limited expectations exist
Grid applications	STATCOM, Battery energy storage system, DVR, APF	STATCOM (flicker compensation), Battery energy storage system
Practicability	+++++	++

The SDBC has the capability to control negative-sequence reactive power and has recently found some dominant applications in arc furnace industries [94, 101]. However, the circulating current and high cell-count ratio restricted the SDBC applications for controlling positive-sequence leading and lagging reactive power as well as real power. But, on the other hand, the SSBC is the best choice for controlling positive-sequence leading and lagging reactive power as well as real power [94, 102]. Since the present work deals only with positive-sequence reactive power compensation, therefore, a SSBC based inverter is considered as a power circuit of the D-STATCOM.

2.6 Control of SSBC Inverters

In many industrial applications, it is often necessary to control the output voltage of inverter for (1) coping with the variations of the dc input voltage, (2) regulating the voltage of the inverter, and (3) satisfying voltage and frequency control requirement in the drives systems [86, 107, 108].

Many modulation techniques have been developed for controlling the output voltage of a multilevel inverter [108]. They are aimed at generating a stepped switched waveform that best approximates an arbitrary reference signal with adjustable amplitude, frequency and phase of a fundamental component that is usually sinusoid in steady state.

The modulation algorithms are divided into two main groups depending on the domain in which they operate: the state-space vector domain, in which the operating principle is based on the voltage vector generation and time-domain, in which the method is based on the voltage level generation over a time frame [63, 66-68, 86, 100, 108, 109]. The state-space vector domain algorithms such as Space Vector Modulation (SVM) based modulation algorithms for multilevel inverters are reported in [86], but, they are not the dominant modulation schemes found in industrial applications [63] as SVM is a computationally intensive method and its complexities increase with increasing number of levels in the inverter [86]. The time-domain approaches such as carrier based pulsewidth modulation

(PWM) techniques are the extensions of the classical modulation methods used for two-level VSI [63, 109]. Other time-domain modulation methods that have also been derived from the two-level VSI are multilevel selective harmonic elimination (SHE) [110], selective harmonic mitigation (SHM) [111] and synchronized optimum PWM. These techniques require offline computations and need to be stored in lookup tables in the digital interface control board. These methods have the advantage in achieving better efficiency. However, low dynamic performance and calculation burden with higher number of levels limit their applications.

In contrast with the large number of recently developed multilevel modulation schemes, no new schemes have made their way to industrial applications, despite the great amount of recent contributions and advances on this topic [63]. The main reason could be that manufacturers favour the proven technology and simplicity of carrier based PWM schemes over new methods that have the advantages but usually at the expense of more complex implementation [63, 109].

2.7 Carrier based PWM Schemes

The carrier based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. These two techniques are the natural extensions of carrier based sinusoidal PWM technique used for two-level inverters and both modulation schemes can be applied to the SSBC based inverters.

2.7.1 Phase-shifted Pulse Width Modulation (PSPWM)

In this scheme, every pair of switches has a carrier signal which has a phase difference with the other carrier signals. In general, a multilevel inverter with *m* voltage levels requires (*m*–1) triangular carrier signals [86]. In this method all the triangular carrier signals have the same frequency and same peak-to-peak amplitude, but there is a phase shift (φ_{cr}) between any two adjacent carrier signals, given by

$$\varphi_{cr} = \frac{360^\circ}{(m-1)} \tag{2.2}$$

The modulating signal is a three-phase sinusoidal voltage signal with adjustable amplitude and frequency. The gate signals are generated by comparing the modulating signal with the carrier signals. When the modulating signal is above the carrier signal, the upper switch is ON and when it is below the lower signal, the lower switch is ON.

In this technique, the fundamental-frequency component in the inverter output voltage can be controlled by amplitude modulation index (m_a), which is defined as [86],

$$m_a = \frac{V_m}{V_{cr}} \tag{2.3}$$

Where V_m and V_{cr} are the peak values of the modulating and carrier signals, respectively. The frequency modulation index (m_f) is defined by [3],

$$f_m = \frac{f_{cr}}{f_m} \tag{2.4}$$

Where f_m and f_{cr} are the frequencies of the modulating and carrier signals, respectively.

Fig. 2.9 shows the principle of the PSPWM technique for the five-level SSBC based inverter shown in Fig. 2.7, where four triangular carrier signals are required with a 90° phase displacement between any two adjacent carrier signals. Modulating procedure for phase–*a* is only shown for simplicity. Four carrier signals are used to generate gating signals for the switches S_{11a}, S_{12a}, S_{22a} and S_{21a} respectively for phase leg–*a*. The gating signals for the other switches in the H-bridge cells in phase leg–*a* are not shown since these switches are operated in a complementary manner with respect to their corresponding upper/lower switches.

One of the main advantages with the PSPWM modulation strategy is that it maintains the duty cycles of the cells approximately equal and therefore maintains an even power distribution among H-bridge cells which naturally balances the capacitor voltages of the inverter. This feature makes the PSPWM as a dominant PWM method for SSBC inverters.

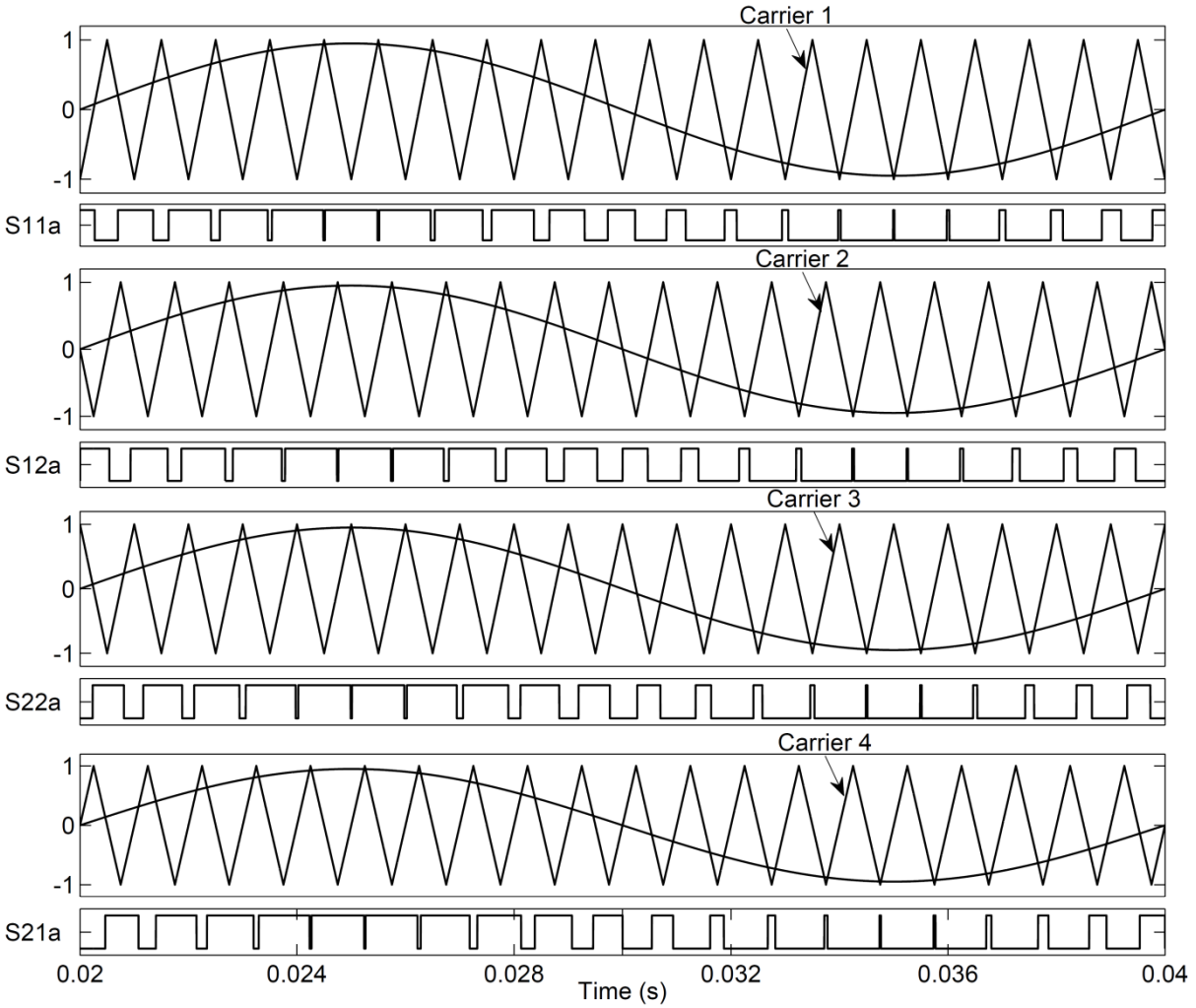


Fig. 2.9: Switching signals for devices of phase–*a* of five-level SSBC based multilevel inverter using PSPWM technique.

2.7.2 Level-shifted Pulse Width Modulation (LSPWM)

Similar to the phase-shifted modulation, an *m*-level inverter using level-shifted multicarrier modulation scheme requires (*m*–1) triangular carrier signals, all having the same frequency and peak-to-peak amplitude. The (*m*–1) triangular carrier signals are vertically disposed such that the bands they occupy are contiguous. The frequency modulation index (m_f) is remains same as that for the phase-shifted modulation scheme whereas the amplitude modulation index (m_a) is defined as:

$$m_a = \frac{V_m}{V_{cr}(m-1)} \tag{2.5}$$

Depending upon the phase relation between individual carrier signals, there are three variants of LSPWM technique. Among these three variants, phase disposition (PD) strategy gives rise to the lowest harmonic distortion for the voltage waveform. Hereafter, PD strategy is referred as LSPWM in this thesis.

Fig. 2.10 shows the principle of the phase disposed level-shifted modulation technique for a five-level SSBC inverter (shown in Fig. 2.7), where four triangular carriers are level-shifted from each other. In this figure only phase–*a* modulating procedure is shown for simplicity. Four carrier signals are used to generate gating signals for the switches S_{11a}, S_{12a}, S_{22a} and S_{21a} for phase leg–*a*. The gating signals for the other switches in the H-bridge cells in phase leg–*a* are not shown since these switches are operated in a complementary manner with respect to their corresponding upper/lower switches.

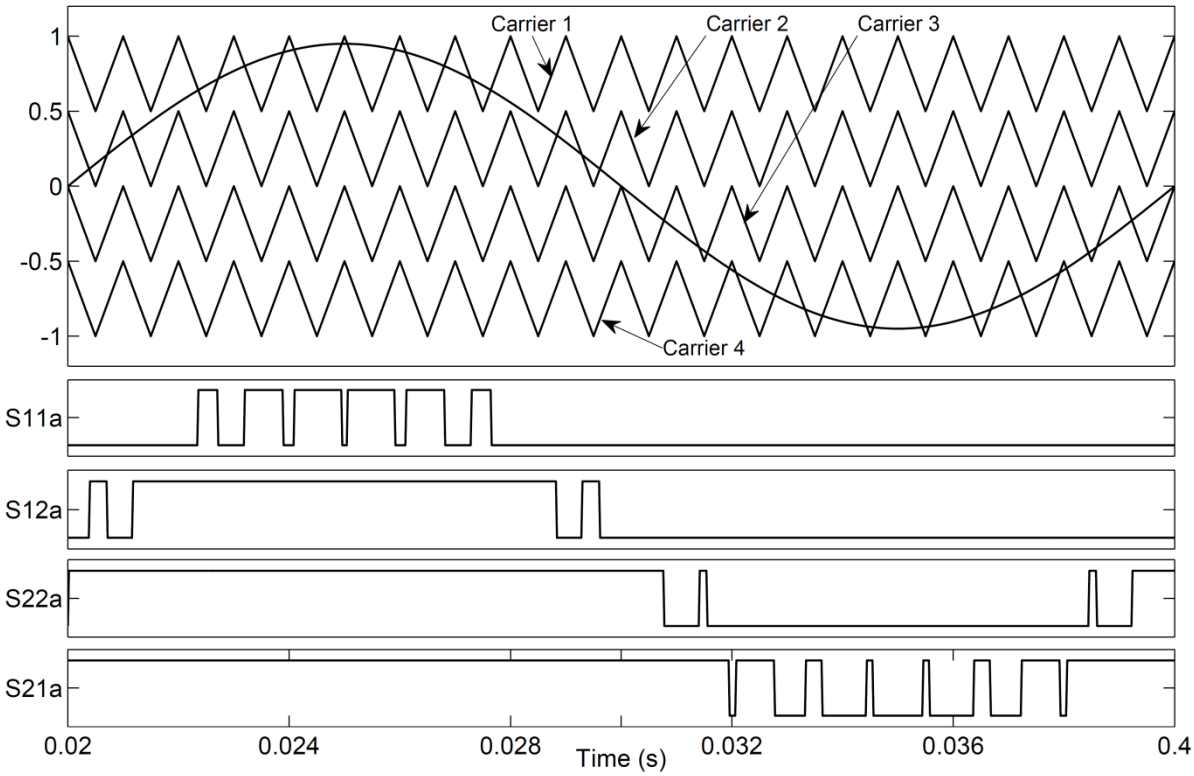


Fig. 2.10: Switching signals for devices of phase–*a* of five-level SSBC based multilevel inverter using LSPWM technique.

The LSPWM technique produces better harmonic performance when compared with the PSPWM technique, but it avoids the current harmonic cancellation at the multipulse secondary windings of the input transformer [63]. Nevertheless, the unequal device conduction periods of the LSPWM technique has resulted in a smaller market penetration even in those applications where transformer is not required at the input side, such as photovoltaic power conversion, APFs, FACTS controllers, battery-powered electric vehicles, UPSs and magnetic resonance imaging. The unequal device conduction periods affect the charging and discharging of the dc bus capacitors and cause non-uniform power and heat distribution in the inverter. To distribute the switching and conduction losses evenly, the switching patterns should be rotated and these carrier rotation schemes are presented in [112-117]. However, none of the work has investigated the device conduction periods and capacitor balancing behaviour with carrier rotation techniques in closed-loop applications.

To address the above limitations, in the present work two simple and effective ways of rotating the carrier signal are investigated for SSBC based inverters, which impose an even power distribution among the H-bridge cells. The device conduction periods for each switching device are calculated for the basic LSPWM and the adopted carrier rotation techniques. To calculate the device conduction periods, three algorithms are proposed. Further, capacitor balancing behaviour with carrier rotation techniques is investigated by realising the SSBC inverter as a power circuit for a three-phase, three-wire (3P3W) PWM D-STATCOM in the next chapter.

2.8 Carrier Rotation Techniques

There are two possible ways to rotate the carrier signals as given below:

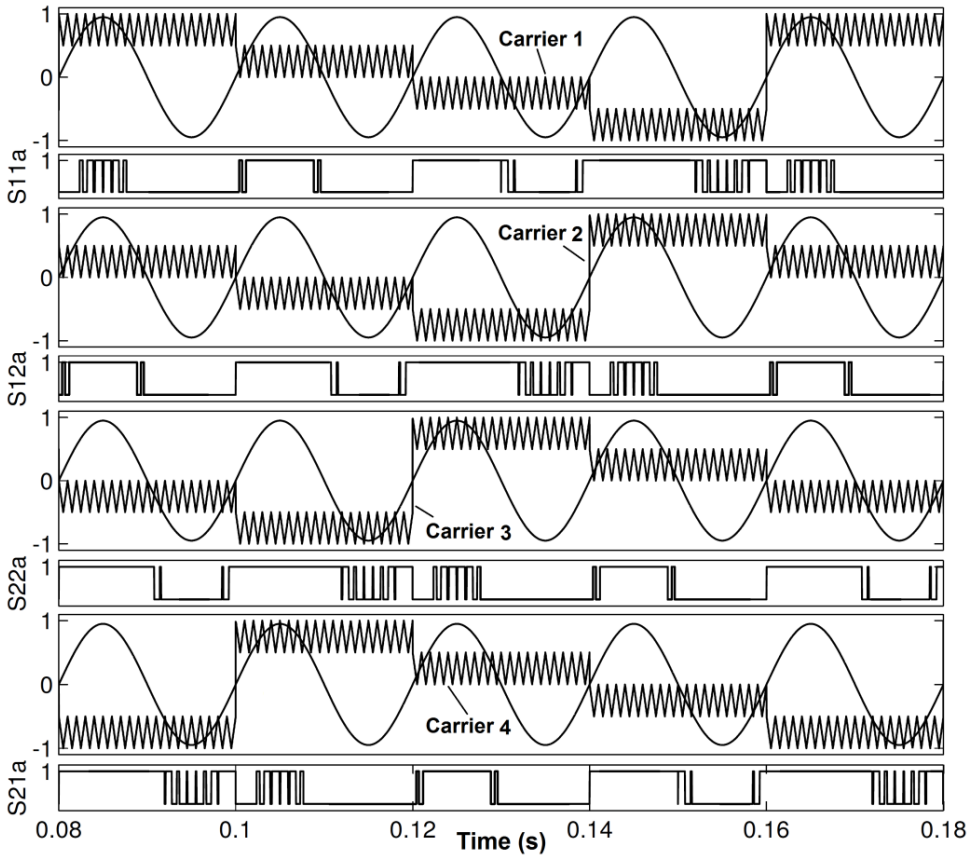
1. Rotation of the carrier signals at the end of each modulating cycle (hereafter referred as method–1).
2. Rotation of the carrier signals at the end of each carrier cycle (hereafter referred as method–2).

In method–1 carrier rotation technique, each carrier signal transposes its position after each modulating cycle (T_m), such that carrier–1 occupies the position of carrier–2 after the first T_m duration and occupies the position of carrier–3 after the second T_m duration and so on. This carrier rotation process is repeated for every T_m period such that, after (m–1) modulating cycles, all the carrier signals come to their respective starting positions. Furthermore in this technique, a phase-shift equivalent to the duration T_m is maintained between any two adjacent carrier signals.

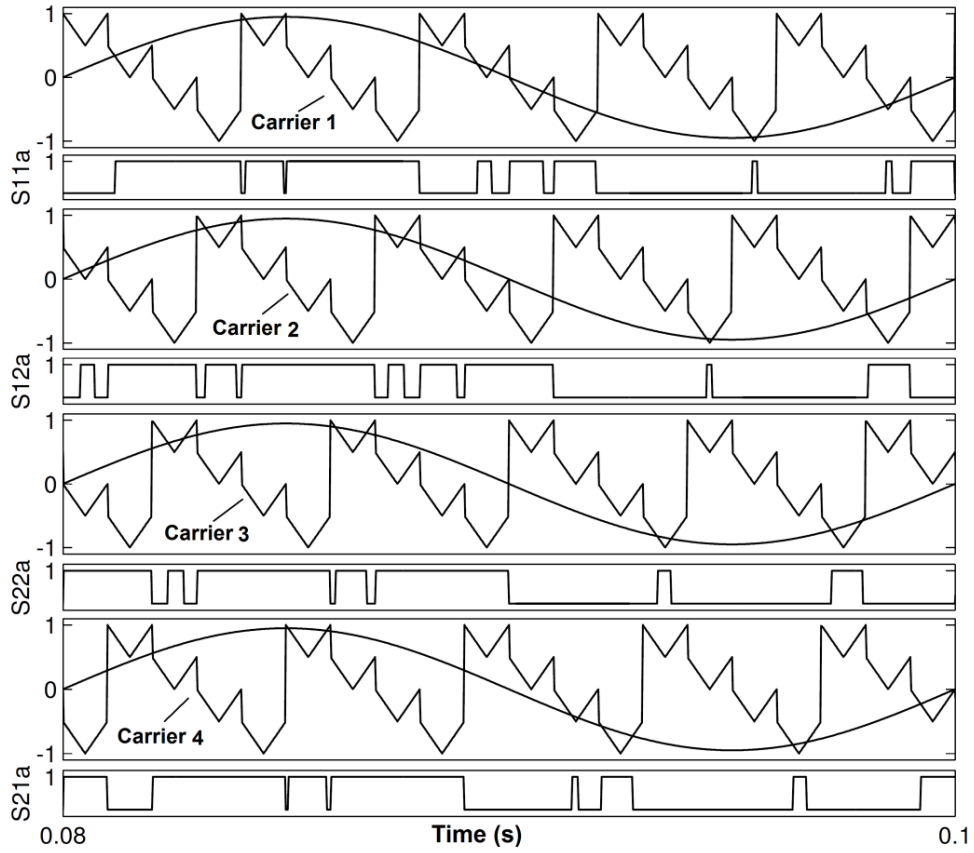
Similarly, in method–2 carrier rotation technique, each carrier signal transposes its position after each carrier cycle (T_c), such that carrier–1 occupies the position of carrier–2 after the first T_c duration and occupies the position of carrier–3 after the second T_c duration and so on. This carrier rotation is repeated for every T_c period such that, after (m–1) carrier cycles, all the carrier signals come to their respective starting positions. Furthermore in this

technique, a phase-shift equivalent to the duration T_c is maintained between any two adjacent carrier signals. To illustrate the basic principle, a five-level SSBC based inverter shown in Fig. 2.7 is considered.

Fig. 2.11 shows the two carrier rotation techniques for this inverter, where four triangular carriers are required. Fig. 2.11(a) shows the arrangement of carrier signals for method–1 rotation while Fig. 2.11(b) shows the arrangement of carrier signals for method–2 rotation. In Fig. 2.11, only phase–*a* modulating procedures are shown for simplicity. The carrier signals 1 to 4 are used to generate the gating signals for the switches S_{11a}, S_{12a}, S_{22a} and S_{21a} (shown in Fig. 2.7) of phase leg–*a*, respectively. The gating signals for S_{41a}, S_{42a}, S_{32a} and S_{31a} switches of phase leg–*a* are not shown since these switches are operated in a complementary manner with respect to their corresponding upper or lower switch.



(a) method–1 carrier rotation technique



(b) Method–1 carrier rotation technique

Fig. 2.11: Switching signals for devices of phase–*a* of five-level SSBC based multilevel inverter using LSPWM with carrier rotation techniques.

2.8.1 Performance Evaluation of Carrier Rotation Techniques

The performance of carrier rotation techniques are investigated with computer simulation studies performed in MATLAB/Simulink environment. Simulation studies are carried out for 5 and 11-level SSBC based inverters and are presented below:

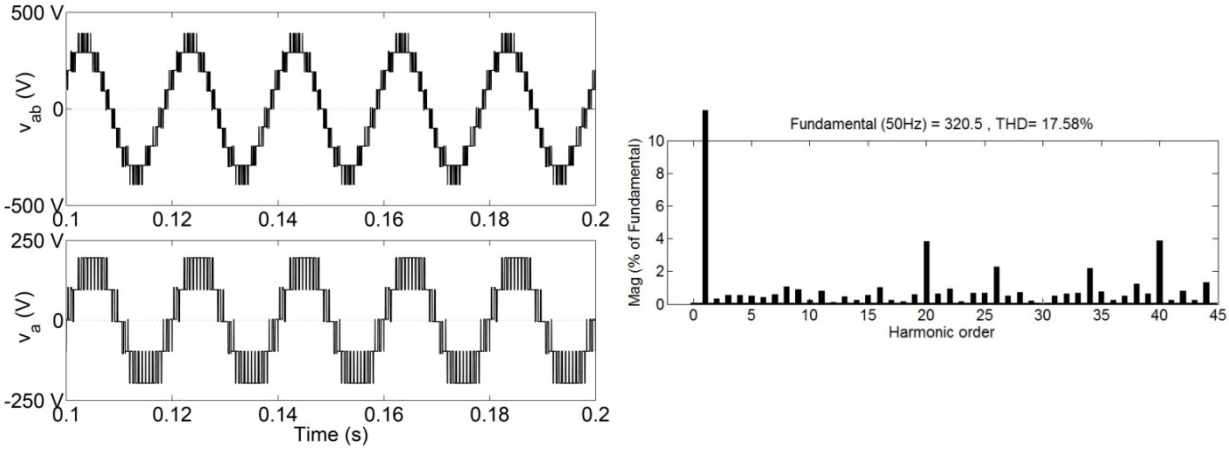
2.8.1.1 Performance Evaluation of Five-level SSBC Inverter

The line-to-line and phase as well as harmonic spectrum of line-to-line voltage for these modulation techniques are shown in Fig. 2.12. It is observed from the figure that the output voltages synthesized by these two carrier rotation techniques are almost identical. The observed THD values of line-to-line voltage are 17.58%, 17.62% and 17.65% for basic LSPWM, method–1 carrier rotation and method–2 carrier rotation techniques respectively. The %THD values and side-band harmonic frequencies (around the harmonic order corresponding to the frequency modulation index, i.e. 30) of these carrier rotation techniques are also almost identical.

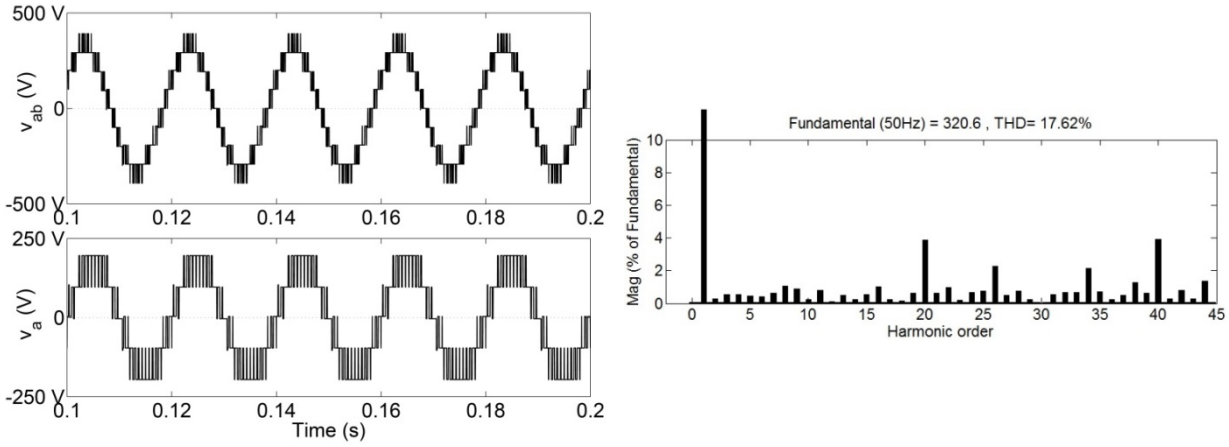
2.8.1.2 Performance Evaluation of 11-level SSBC Inverter

The line-to-line and phase voltages as well as harmonic spectrum of line-to-line voltage for these two modulation techniques with an 11-level SSBC based inverter are shown in Fig. 2.13. It is observed from the figure that the output voltages synthesized by these two carrier rotation techniques are also almost identical. The observed THD values of line-to-line voltage are 6.84%, 6.83% and 6.84% for basic LSPWM, method–1 carrier rotation and method–2 carrier rotation techniques respectively. The %THD values and side-band harmonic frequencies (around the harmonic order corresponding to the frequency modulation index, i.e. 60) of these carrier rotation techniques are also almost identical.

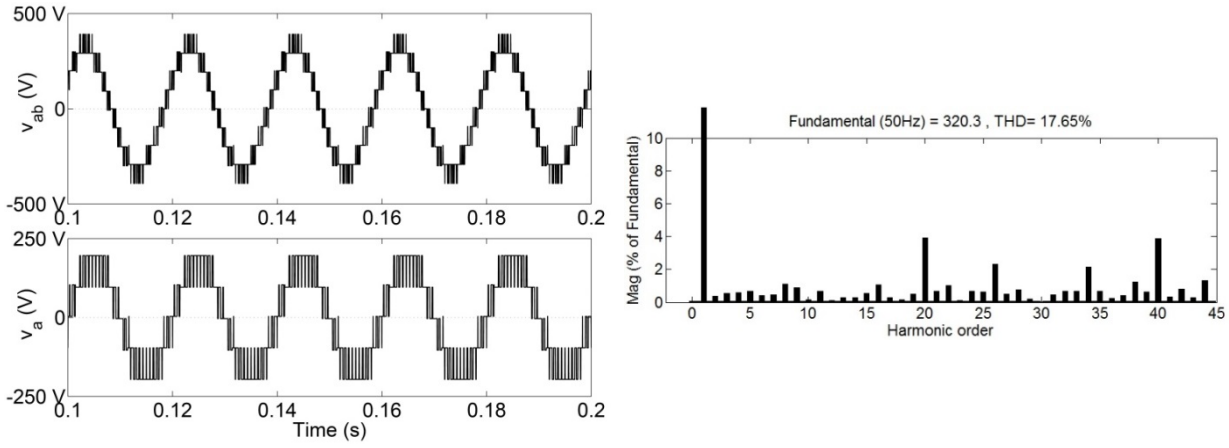
From Fig. 2.12 and Fig. 2.13, it is observed that the output voltages synthesized by these two carrier rotation techniques are almost identical with basic LSPWM technique. The %THD values and side-band harmonic frequencies of these carrier rotation techniques are also almost identical. Therefore, the external behaviours (from the point of view of load) of these two carrier rotation schemes are almost identical. However, the utility of any modulation scheme is strongly determined by its device conduction periods. In the next section, these two schemes are investigated vis-a-vis their corresponding conduction periods.



(a) No rotation (basic LSPWM technique)

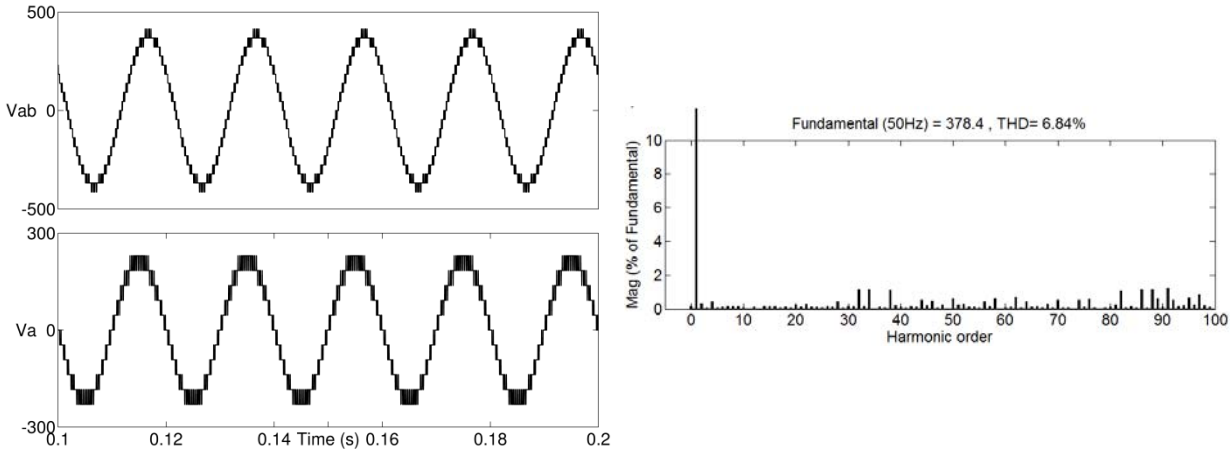


(b) Method–1 carrier rotation technique

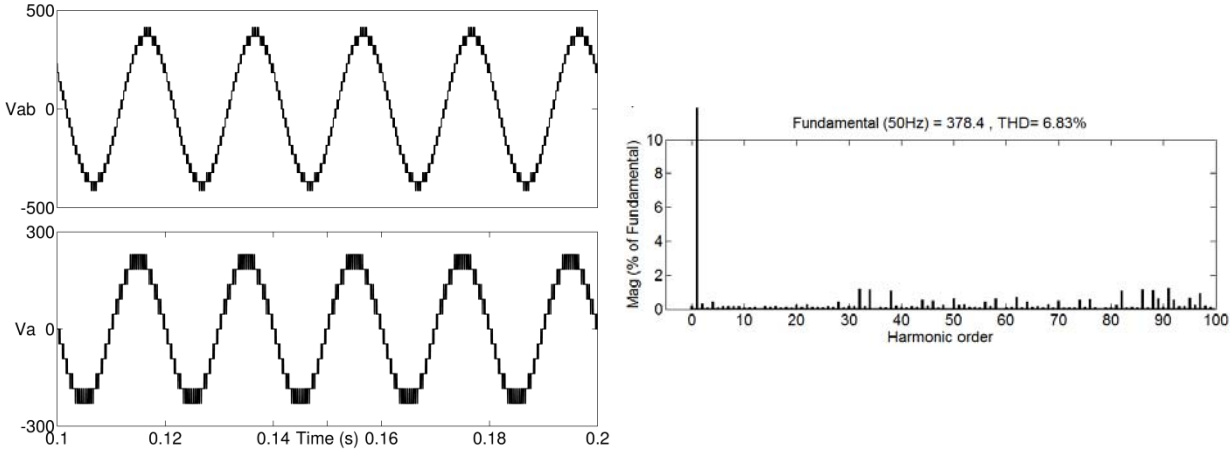


(c) Method–2 carrier rotation technique

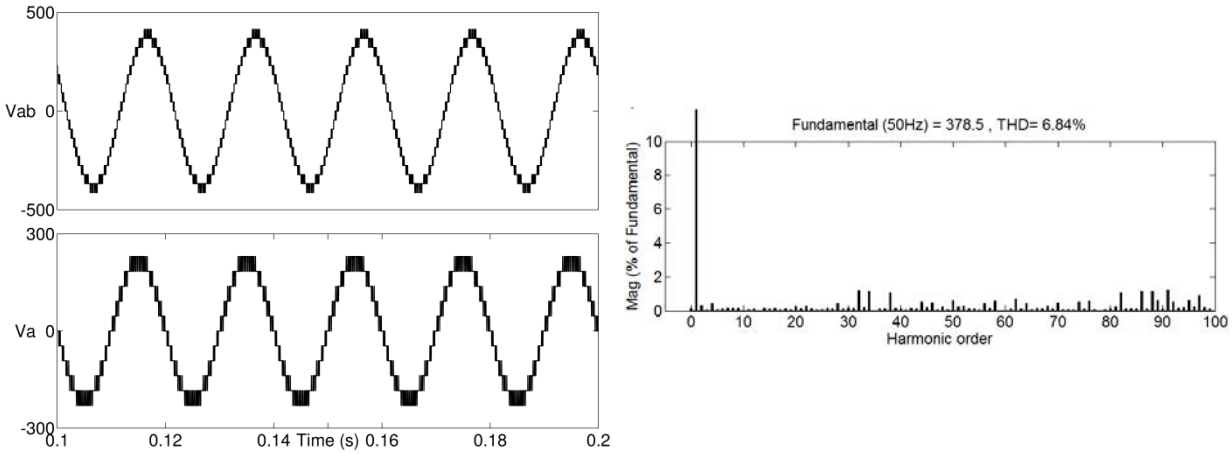
Fig. 2.12: Simulated waveforms of line-to-line voltage (v_{ab}), line-to-neural voltage (v_a) and harmonic spectrum of line-to-line voltage for a five-level SSBC based modular multilevel inverter with and without carrier rotation techniques (m_a = 0.95, m_f = 30, f_m = 50 Hz and f_{cr} = 1500 Hz).



(a) No rotation (basic LSPWM technique)



(b) Method–1 carrier rotation technique



(c) Method–2 carrier rotation technique

Fig. 2.13: Simulated waveforms of line-to-line voltage (v_{ab}), line-to-neural voltage (v_a) and harmonic spectrum of line-to-line voltage for a 11-level SSBC based modular multilevel inverter with and without carrier rotation techniques (m_a = 0.95, m_f = 60, f_m = 50 Hz and f_{cr} = 3 kHz).

2.8.2 Device Conduction Periods of the Carrier Rotation Techniques

For the analytical purposes following nomenclature are followed:

m = Number of levels

f_m = Modulating signal frequency

$f_c =$ Carrier signal frequency

$m_f = \dfrac{f_c}{f_m} =$ Frequency modulation index

$T_m = \dfrac{1}{f_m} =$ Modulating signal time period (in sec.)

$T_c = \dfrac{1}{f_c} =$ Carrier signal time period (in sec.)

$a = \dfrac{2\pi}{m_f} =$ Carrier signal time period (in rad.)

$m_a =$ Amplitude modulation index

$T_P =$ Individual device conduction period

Fig. 2.14 shows the generalized carrier arrangement for an *m*-level SSBC inverter with LSPWM technique. The upper and lower limits of the band of i^{th} carrier signal band is given as:

$$uprLimit = 1 - \frac{2(i-1)}{(m-1)} \tag{2.6}$$

$$lwrLimit = 1 - \frac{2i}{(m-1)} \tag{2.7}$$

In order to determine the device conduction periods of the carrier rotation techniques, the total conduction period of each device is calculated over the duration of (*m*-1) modulating cycles. For symmetry in calculating the total device conduction periods, it is assumed that the carrier signal frequency is four times the modulating signal frequency.

One of the major limitations with naturally sampled PWM is the requirement of complicated calculations for finding the intersecting points between the sinusoidal modulating signal and the triangular carrier signal. The most popular alternative for overcoming this limitation is to use the “regular sampled” PWM [108]. There are different variants of regular sampled PWM, but symmetrical regular sampled PWM is considered in the present work in which the reference signal is sampled at the positive peak of the carrier signal. Fig. 2.15 shows the process of generation of switching signal with symmetrical regular sampled PWM technique (positive peak sampled) using triangular carrier signals for a five-level SSBC inverter corresponding to LSPWM technique.

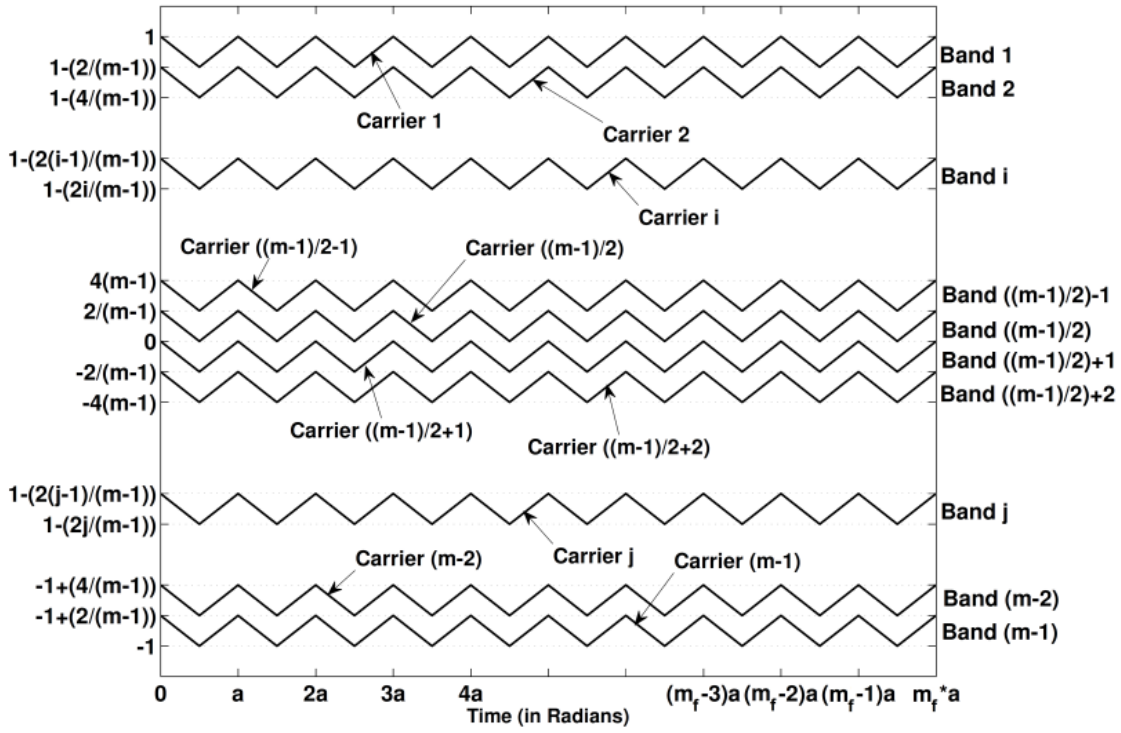


Fig. 2.14. Carrier arrangement for an *m*-level SSBC based modular multilevel inverter for LSPWM technique.

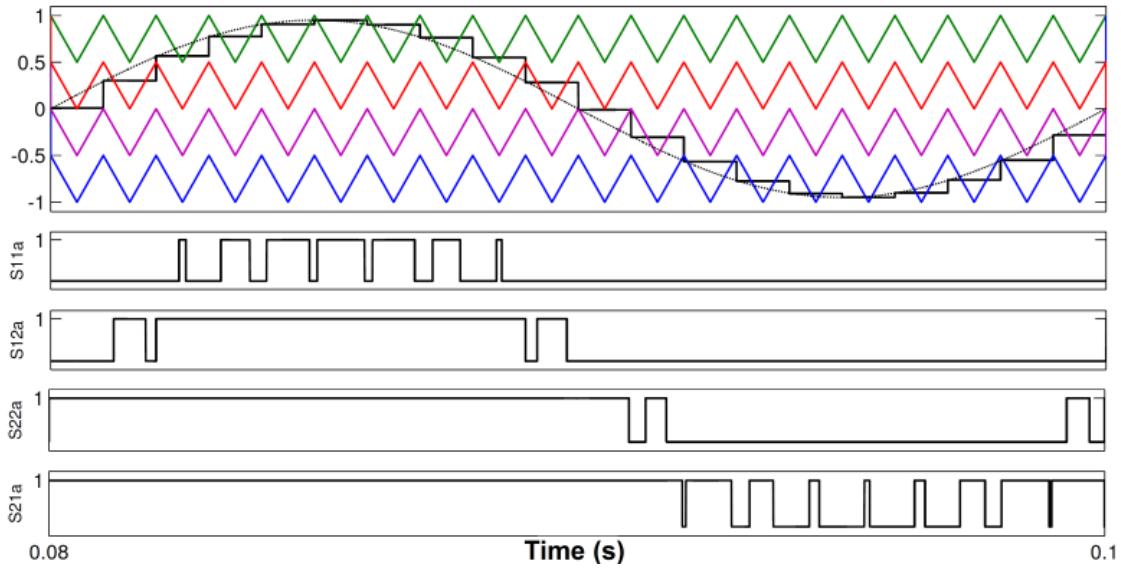


Fig. 2.15. Symmetrical regular sampled PWM (positive peak sampled) with triangular carriers for a five-level SSBC inverter with LSPWM technique.

For calculating the individual device conduction period (T_p) with stepped reference signal for each carrier cycle, there are three possible cases as described below:

a) The modulating signal is below the carrier signal: in this case $T_p = 0$.

b) The modulating signal is above the carrier signal: in this case $T_p = T_c$.

c) The modulating signal is within the upper and lower peaks of the carrier signal: in this case, the basic methodology for calculating T_p is shown in Fig. 2.16.

Fig. 2.16 depicts the procedure for calculating the device conduction period for j^{th} cycle of the i^{th} carrier signal. Fig. 2.16(a) shows the arrangement when the modulating signal is in

positive half cycle and similarly, Fig. 2.16(b) shows the arrangement for the negative half cycle of the modulating signal.

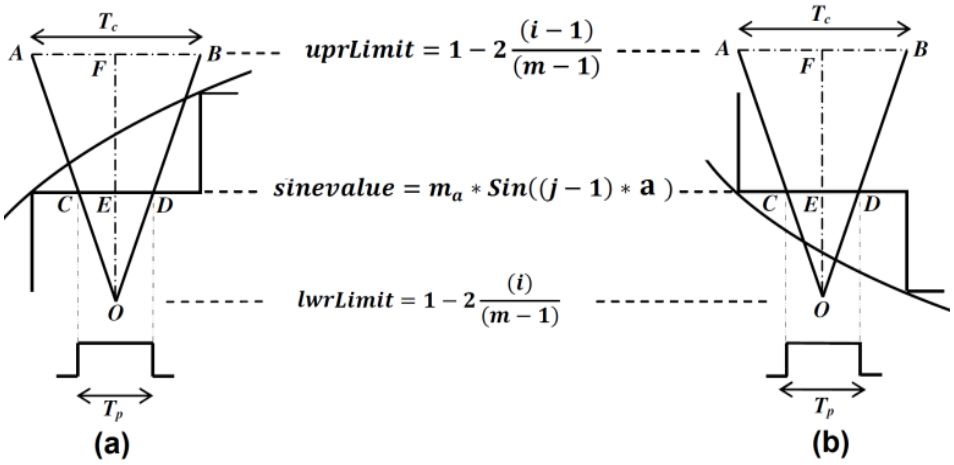


Fig. 2.16. Arrangement of carrier and modulating signals when the modulating signal is within the limits of the carrier signals: (a) during positive half cycle of the modulating signal; (b) during negative half cycle of the modulating signal.

The value of the modulating signal at the falling edge of the j^{th} cycle of the i^{th} carrier signal is given as:

$$SineValue = m_a(\sin(j-1)a) \tag{2.8}$$

From ΔOAF and ΔOCE

$$\frac{CE}{AF} = \frac{OE}{OF} \tag{2.9}$$

$$\Rightarrow \frac{T_P/2}{T_C/2} = \frac{SineValue - lwrLimit}{2/(m-1)} \tag{2.10}$$

$$T_P = T_C \frac{(m-1)(m_a \sin(j-1)a - 1) + 2(i-1)}{2} \tag{2.11}$$

Once the individual device conduction periods are calculated, then the next step is to calculate the total device conduction period of each device for each proposed modulation technique. For investigating the properties of the proposed modulation techniques for equalizing the device conduction periods (DCP), the DCPs are calculated for the three cases:

a) For LSPWM technique without rotating the carrier signals.
b) For LSPWM technique with method–1 carrier rotation.
c) For LSPWM technique with method–2 carrier rotation.

The detailed flowcharts of algorithms for calculating DCPs for the above three cases are given in Fig. 2.17, Fig. 2.18 and Fig. 2.19 respectively. By using these algorithms, total device total conduction periods are calculated for a 5-level and an 11-level SSBC based inverter with different amplitude and frequency modulation indices. The results are summarized in Table 2.5 to Table 2.8.

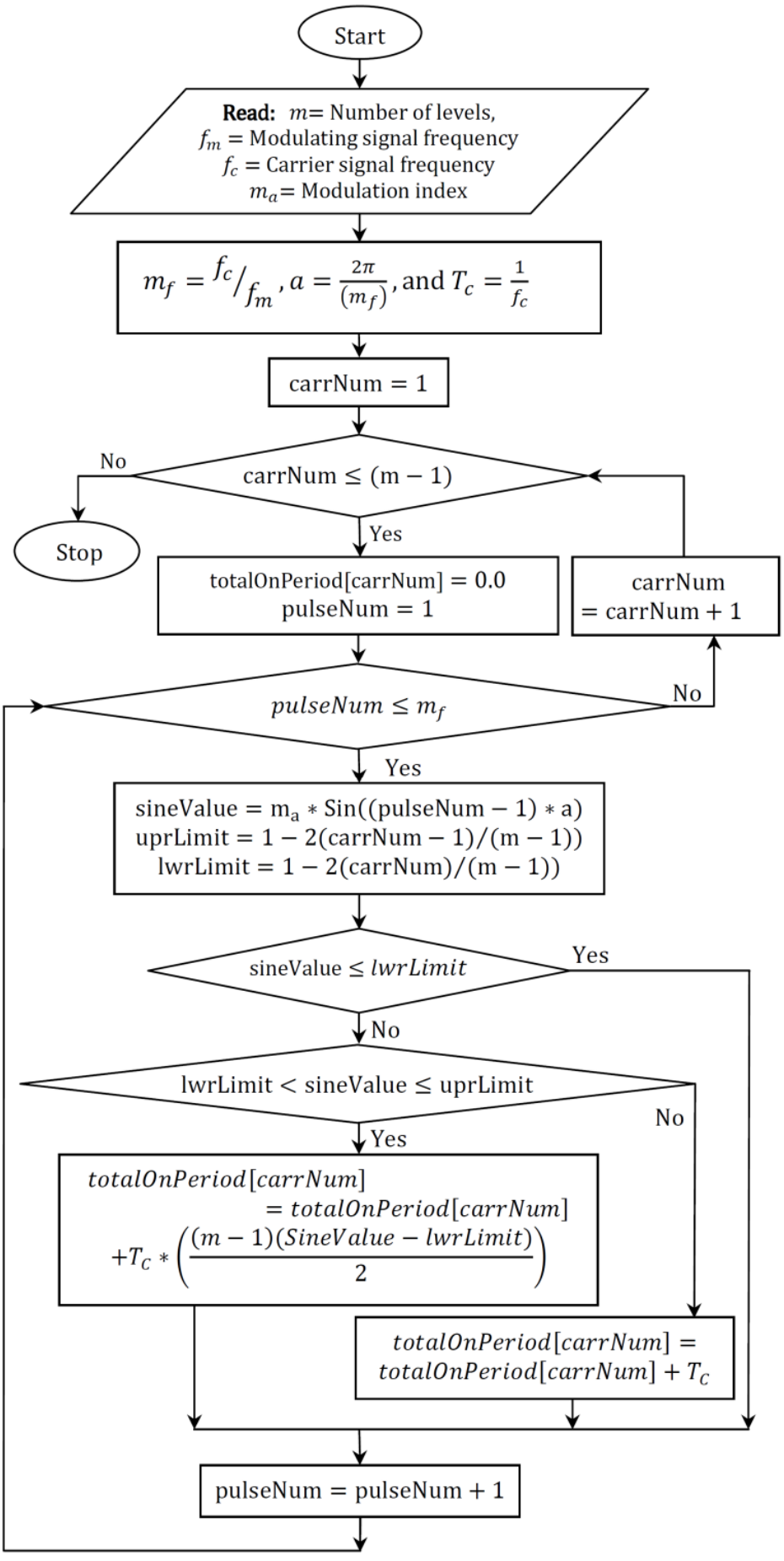


Fig. 2.17. Algorithm for calculating the total device conduction periods for LSPWM technique without carrier rotation.

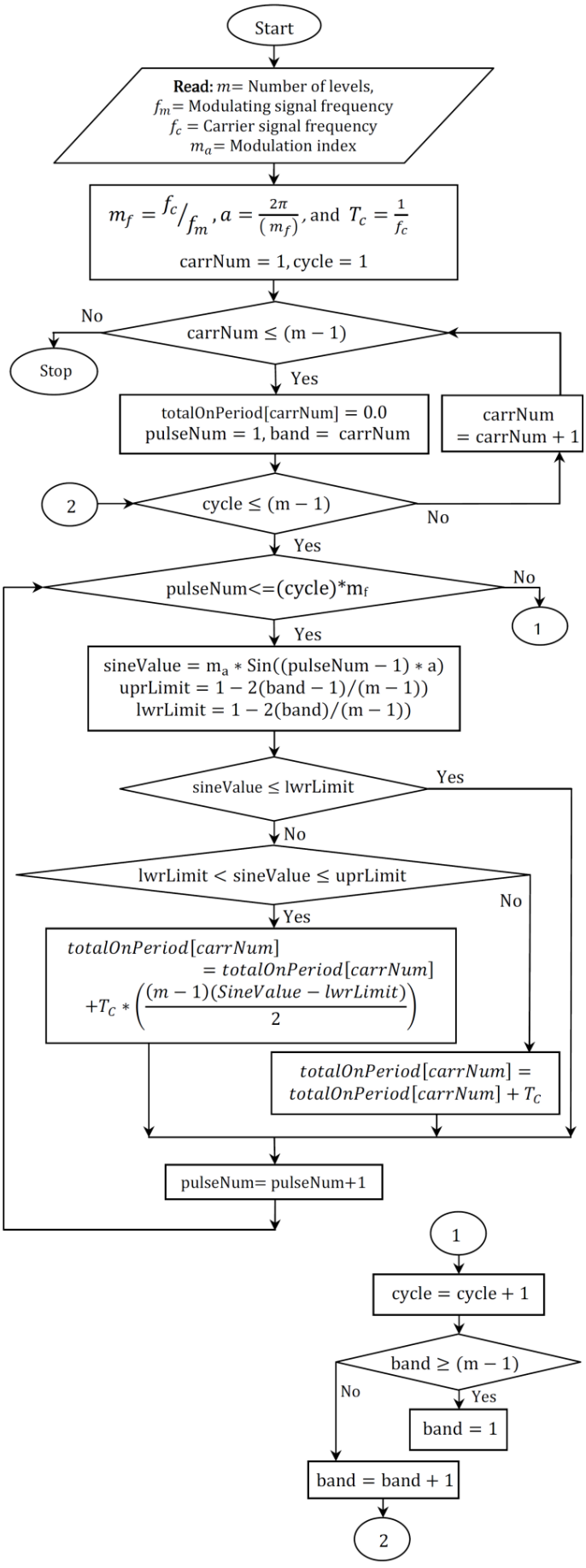


Fig. 2.18. Algorithm for calculating the total device conduction periods for LSPWM technique with method–1 carrier rotation.

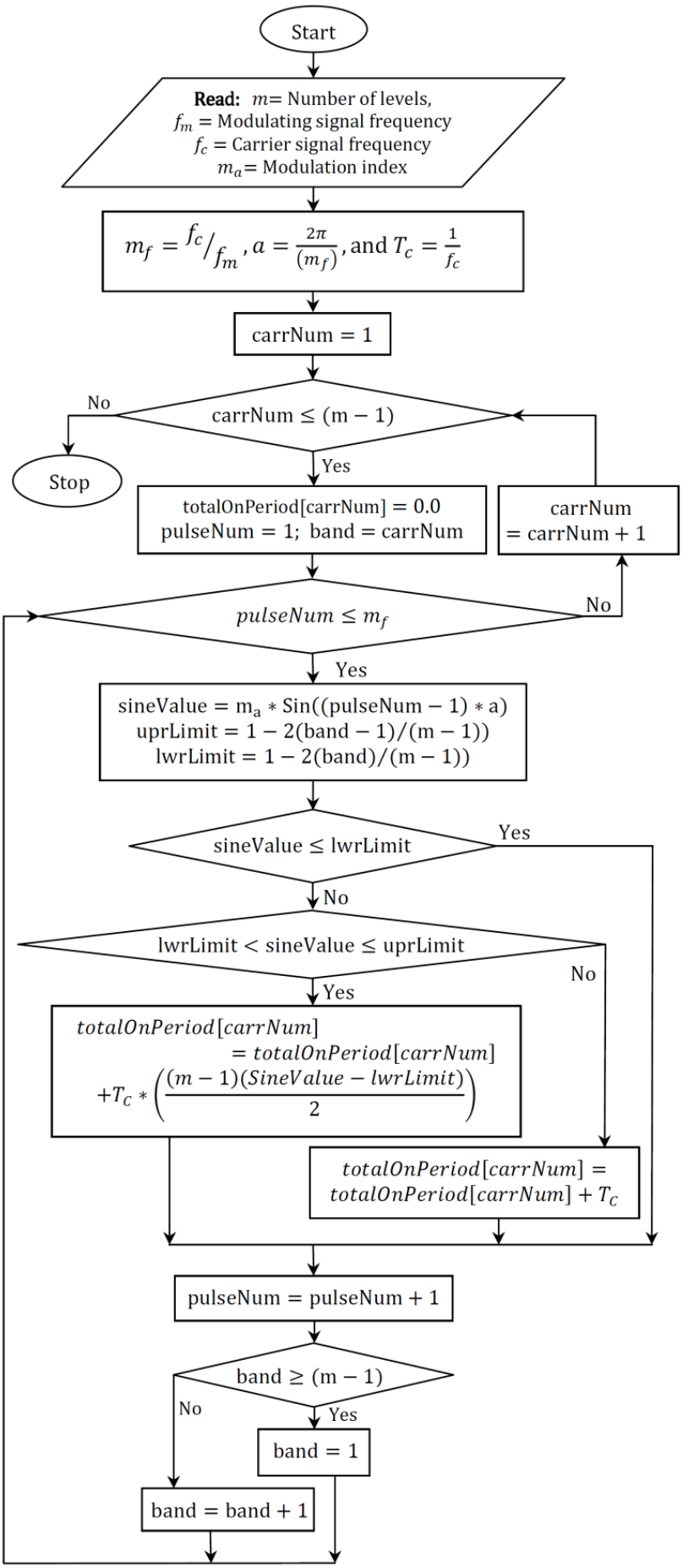


Fig. 2.19. Algorithm for calculating the total device conduction periods for LSPWM technique with method–2 carrier rotation.

Table 2.5: Total conduction periods (in sec.) for each device of a 5-level SSBC inverter.

f_{cr}	Device Name	Number of levels = 5								
		No rotation			Method–1			Method–2		
		m_a = 0.8	m_a = 0.9	m_a = 1.0	m_a = 0.8	m_a = 0.9	m_a = 1.0	m_a = 0.8	m_a = 0.9	m_a = 1.0
1 khz	S_{11a}	0.002232	0.003251	0.004389	0.009999	0.009999	0.009998	0.009993	0.010029	0.010106
	S_{12a}	0.007867	0.008111	0.008234	0.009998	0.009998	0.009998	0.009970	0.010012	0.010013
	S_{22a}	0.012131	0.011887	0.011763	0.010003	0.010003	0.010003	0.010029	0.009988	0.009987
	S_{21a}	0.017768	0.016750	0.015611	0.009999	0.009998	0.009998	0.010008	0.009969	0.009893
2 khz	S_{11a}	0.002253	0.003279	0.004366	0.010000	0.010000	0.010000	0.009995	0.009992	0.009996
	S_{12a}	0.007909	0.008152	0.008336	0.009999	0.010000	0.009999	0.009974	0.009973	0.009964
	S_{22a}	0.012090	0.011846	0.011663	0.010001	0.010002	0.010002	0.010025	0.010025	0.010034
	S_{21a}	0.017747	0.016721	0.015634	0.009999	0.009999	0.009999	0.010006	0.010009	0.010005
3 khz	S_{11a}	0.002252	0.003280	0.004348	0.010000	0.010000	0.010000	0.009997	0.010019	0.010009
	S_{12a}	0.007921	0.008164	0.008368	0.010000	0.010000	0.010000	0.009979	0.010004	0.010005
	S_{22a}	0.012078	0.011835	0.011632	0.010001	0.010001	0.010000	0.010020	0.009996	0.009996
	S_{21a}	0.017748	0.016720	0.015651	0.010000	0.010000	0.010000	0.010003	0.009980	0.009990

Table 2.6: Total conduction periods (in sec.) for each device of an 11-level SSBC inverter with f_{cr} = 1 kHz.

Device Name	Number of levels = 11								
	No rotation			Method–1			Method–2		
	m_a = 0.8	m_a = 0.9	m_a = 1.0	m_a = 0.8	m_a = 0.9	m_a = 1.0	m_a = 0.8	m_a = 0.9	m_a = 1.0
S_{11a}	0.000000	0.001059	0.002599	0.009999	0.009999	0.009997	0.009998	0.009918	0.009957
S_{12a}	0.003079	0.004280	0.005000	0.009999	0.009999	0.009999	0.009889	0.009986	0.009860
S_{13a}	0.005700	0.006287	0.006875	0.010000	0.009999	0.009998	0.010036	0.010041	0.009956
S_{14a}	0.007468	0.007777	0.008085	0.009999	0.009999	0.009999	0.009933	0.009922	0.009879
S_{15a}	0.009000	0.009000	0.009000	0.009999	0.010000	0.010000	0.009938	0.009837	0.009915
S_{25a}	0.010995	0.010994	0.010994	0.009999	0.010000	0.009999	0.010061	0.010160	0.010078
S_{24a}	0.012532	0.012223	0.011915	0.010000	0.009999	0.010000	0.010065	0.010079	0.010123
S_{23a}	0.014300	0.013713	0.013125	0.010000	0.010000	0.009999	0.009964	0.009961	0.010043
S_{22a}	0.016921	0.015720	0.015000	0.010000	0.009999	0.010001	0.010110	0.010007	0.010143
S_{21a}	0.020000	0.018941	0.017401	0.010000	0.010001	0.010001	0.010004	0.010086	0.010044

Table 2.7: Total conduction periods (in sec.) for each device of an 11-level SSBC inverter with f_{cr} = 2 kHz.

Device Name	Number of levels = 11								
	No rotation			Method–1			Method–2		
	m_a = 0.8	m_a = 0.9	m_a = 1.0	m_a = 0.8	m_a = 0.9	m_a = 1.0	m_a = 0.8	m_a = 0.9	m_a = 1.0
S_{11a}	0.000000	0.000983	0.002692	0.010000	0.009999	0.009999	0.010013	0.009939	0.010003
S_{12a}	0.003054	0.004321	0.005034	0.010000	0.010001	0.010000	0.010043	0.010000	0.009994
S_{13a}	0.005677	0.006185	0.006705	0.010000	0.009999	0.009999	0.009988	0.009949	0.010034
S_{14a}	0.007549	0.007888	0.008043	0.009999	0.010000	0.009999	0.010019	0.010051	0.010021
S_{15a}	0.009123	0.009201	0.009279	0.010000	0.009999	0.010000	0.009970	0.009938	0.009977
S_{25a}	0.010874	0.010796	0.010717	0.010000	0.010001	0.010000	0.010029	0.010060	0.010023
S_{24a}	0.012451	0.012112	0.011957	0.010000	0.009999	0.010000	0.009982	0.009950	0.009978
S_{23a}	0.014323	0.013815	0.013295	0.010000	0.010000	0.009999	0.010010	0.010049	0.009966
S_{22a}	0.016946	0.015679	0.014966	0.010000	0.009998	0.010001	0.009958	0.009996	0.010005
S_{21a}	0.020000	0.018941	0.017401	0.010000	0.010001	0.010001	0.010004	0.010086	0.010044

Table 2.8: Total conduction periods (in sec.) for each device of an 11-level SSBC inverter with f_{cr} = 3 kHz.

Device Name	Number of levels = 11								
	No rotation			Method–1			Method–2		
	m_a = 0.8	m_a = 0.9	m_a = 1.0	m_a = 0.8	m_a = 0.9	m_a = 1.0	m_a = 0.8	m_a = 0.9	m_a = 1.0
S_{11a}	0.000000	0.001011	0.002706	0.009999	0.010000	0.009999	0.010018	0.010049	0.009996
S_{12a}	0.003032	0.004260	0.005039	0.009999	0.009999	0.009999	0.010005	0.010034	0.009989
S_{13a}	0.005665	0.006261	0.006645	0.009999	0.009999	0.009997	0.010025	0.009999	0.009981
S_{14a}	0.007572	0.007811	0.008053	0.009999	0.009999	0.009998	0.009964	0.009971	0.009981
S_{15a}	0.009164	0.009267	0.009346	0.009999	0.009999	0.009998	0.009933	0.009965	0.009976
S_{25a}	0.010835	0.010731	0.010651	0.010000	0.010001	0.009999	0.010064	0.010032	0.010023
S_{24a}	0.012430	0.012189	0.011947	0.010000	0.009999	0.009999	0.010039	0.010030	0.010019
S_{23a}	0.014333	0.013739	0.013355	0.010000	0.010001	0.010000	0.009977	0.010002	0.010018
S_{22a}	0.016968	0.015740	0.014961	0.010000	0.009998	0.010001	0.009992	0.009968	0.010013
S_{21a}	0.020000	0.018989	0.017294	0.010001	0.010001	0.009999	0.009983	0.009948	0.010003

From these tables it is observed that the device conduction periods are different for the basic LSPWM technique. Since the switching power loss of semi-conductor device is proportional to its conduction period, the switching power loss of the individual devices is unequal in basic LSPWM technique. Further, this unequal device conduction period affects the charging and discharging phenomenon of the dc capacitors of the H-bridge cells [91]. Therefore, the power loss and the heat distribution inside the inverter and power distribution among the H-bridge cells are not uniform in basic LSPWM technique. However, in method–1 and method–2 carrier rotation schemes, the device conduction periods are virtually equalized over multiple fundamental frequency periods or multiple carrier frequency periods and as a result, the power loss and the heat distribution inside the inverter become quite uniform. Further, the power distributions among H-bridge cells of the SSBC-MMCI are expected to be equal and a natural balancing of capacitor voltages of H-bridge cells is possible with the carrier rotation techniques.

A summary of the main characteristics of the different multicarrier based PWM techniques for multilevel inverters is given in Table 2.9. From Table 2.9, it is observed that, the adopted carrier rotation techniques combine the advantages of equal device conduction periods and even power distribution from PSPWM technique and the best harmonic performance from LSPWM technique, respectively. However, in method–2 carrier rotation technique narrow pulses and/or glitches may be observed with high values of carrier signal frequencies, although these may not affect the performance of the system adversely, for all practical purposes.

Table 2.9: Comparison between different multicarrier PWM techniques.

Comparison	**PSPWM**	**LSPWM (No rotation)**	**LSPWM (with carrier rotation)**	
			Method–1	**Method–2**
Device switching frequency	Same for all devices	Different	Same for all devices	Same for all devices
Is device conduction period is same?	Yes	No	Yes	Yes
Line-to-line voltage THD	Good	Best	Best	Best
Inverter topology	FCMLI, MMCI	Topology independent	FCMLI, MMCI	FCMLI, MMCI
Capacitor balancing	Best	Poor	Better	Best
Dynamic performance	Excellent	Poor	Good	Excellent

2.9 Conclusion

In this chapter, the selection of SSBC based modular multilevel inverter for the power circuit of D-STATCOM is addressed and the voltage control methods for the chosen inverter are discussed. This chapter investigated two simple carrier rotation schemes to LSPWM technique which produce equal device conduction periods for SSBC based modular multilevel inverter. The performance of these carrier rotation schemes is investigated through simulation studies on a 5-level and an 11-level SSBC based inverter. From the simulation results it is observed that the output voltages synthesized by these two carrier rotation techniques are almost identical with basic LSPWM technique. It is observed that the %THD values and side-band harmonic frequencies of these carrier rotation techniques are also almost identical. With these carrier rotation techniques, the device conduction periods are virtually equalized over multiple fundamental frequency periods or multiple carrier frequency periods. As a result, the power loss and the heat distribution inside the inverter become quite uniform, therefore, a natural balancing of capacitor voltages of H-bridge cells is possible.

CHAPTER 3: D-STATCOM FOR THREE-PHASE THREE-WIRE SYSTEMS

The design of an 11 kV, 1 MVA transformerless SSBC based D-STATCOM for harmonic elimination and reactive power compensation in 3P3W distribution systems is presented in this chapter. Exhaustive simulation results are presented to investigate the performance of D-STATCOM during transients and as well as in steady-state, for variety of loads with different utility voltage conditions. This chapter further investigates the performance of carrier rotation techniques for balancing the capacitor voltages of individual H-bridges in SSBC based inverter of D-STATCOM.

3.1 Introduction

The three-phase, three-wire (3P3W) distribution systems are normally used to deliver electrical supply for high-power loads such as adjustable speed drives, traction, arc furnaces and other industrial applications. In these systems the neutral conductor is absent and consequently, the neutral current is zero. Therefore, in these systems only harmonic and/or reactive current components contribute to the power quality problems in current waveform. For compensation of harmonics and reactive power in these systems, a 3P3W D-STATCOM is used. The complete compensator scheme of the D-STATCOM for 3P3W distribution system is shown in Fig. 3.1. The D-STATCOM consists of two distinct main circuits: (a) PWM inverter; (b) D-STATCOM controller. The former one is responsible for power processing in synthesizing the compensating current that should be drawn from the power system and the later one is responsible for signal processing in determining the compensating reference currents in real-time and forcing the inverter to draw these currents from the system. The control algorithm implemented in the controller of the D-STATCOM determines its compensation characteristics. Detailed description of the controller for the D-STATCOM is given in the next section.

3.2 Control of D-STATCOM

The D-STATCOM controller consists of two functional control blocks:

1. Reference current generator
2. PWM controller

The reference current generator has the task of detecting the harmonic and reactive currents that has to be compensated by the D-STATCOM. The source voltages, dc capacitor voltages and load currents are measured to obtain these reference compensating currents. Once the reference compensating currents are calculated, these currents are given as reference signals to the inner PWM current controller. In PWM controller, these reference compensating currents are compared with the measured D-STATCOM currents and the errors are processed in PI controllers. The outputs of the PI controllers set the magnitude of the three-phase reference signals for the current control technique implemented in PWM controller. The switching operation of the power electronic devices in the inverter

automatically forces the D-STATCOM currents to follow the reference compensating currents. The detailed description for each controller is given below.

3.2.1 Reference Current Generator

One of the key points for proper implementation of a D-STATCOM is to use a reliable method for current reference generation. At present, there is a large variety of practical implementations supported by different theories, the performances of which are continuously debated while ever-better solutions are proposed. There are numerous published references that describe different algorithms used for simultaneous filtering of reactive power and harmonics [79, 80]. The classification of the reference current detection methods can be done depending on the mathematical algorithms involved [41, 80]. Thus, two directions are described here: the frequency-domain and the time-domain harmonic detection methods.

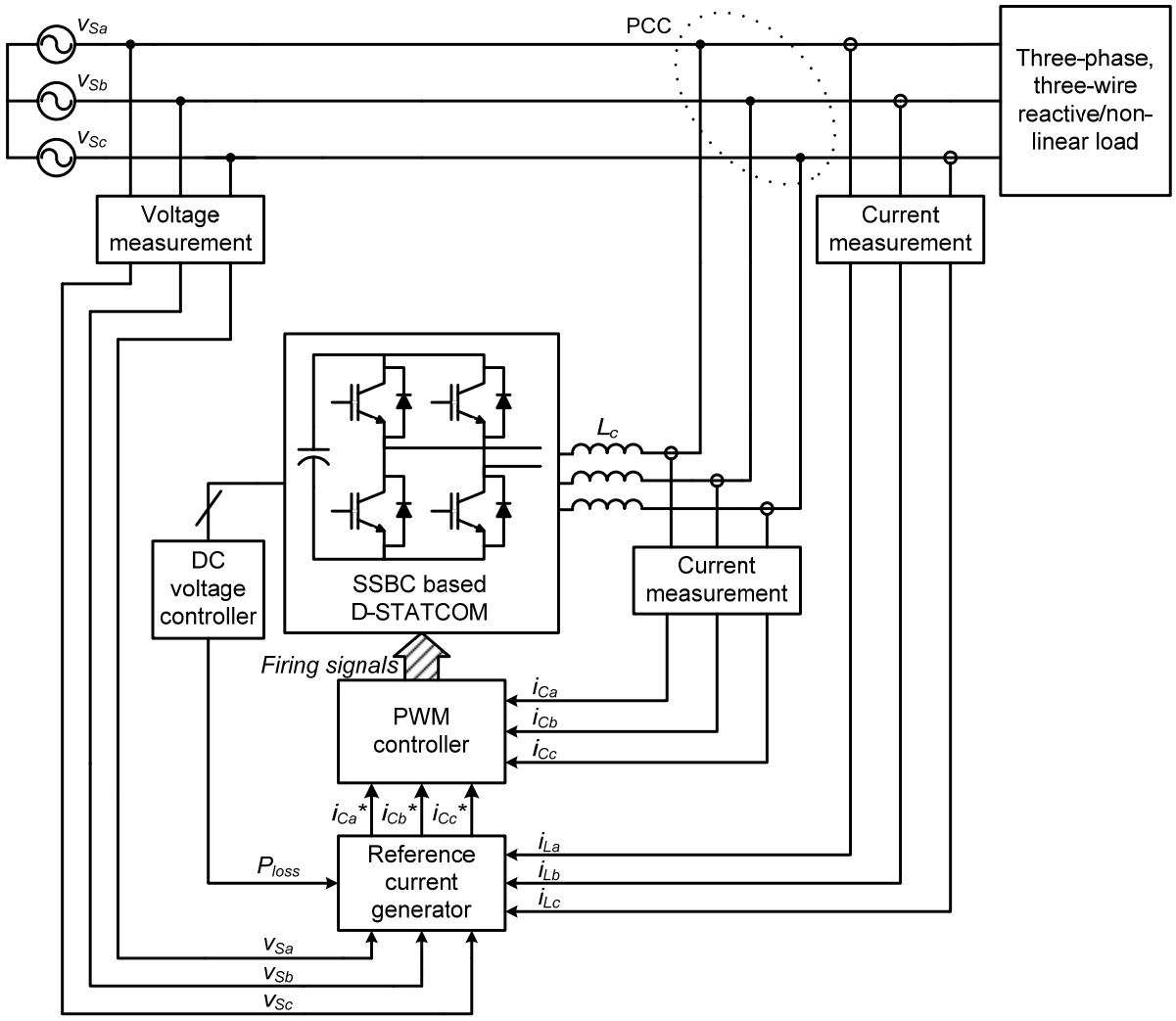


Fig. 3.1: Schematic diagram of the 3P3W system with shunt connected D-STATCOM.

The frequency-domain methods mainly use Fourier analysis for calculating the reference currents as fast as possible with a reduced number of computations, to allow a real-time implementation [80]. The commonly used frequency-domain methods are Discrete Fourier Transform (DFT) [118], Recursive Discrete Fourier Transform (RDFT) [119] and Fast

Fourier Transform (FFT) [120]. The common drawbacks of the Fourier analysis based harmonic detection methods include: proper design of the antialiasing filter, careful synchronization between sampling time and fundamental frequency of the inverter, large memory requirements to store the required samples, large computation burden for the DSP and imprecise results in transient conditions [80]. But on the other side, the time-domain methods offer increased speed, ease of implementation and fewer calculations compared to the frequency-domain methods [80]. There are numerous time-domain approaches reported in the literature, and some of them are Fryze, Buchholz and Depenbrock method [121], instantaneous symmetrical components based method [122], Synchronous Reference Frame (SRF) theory [123, 124], Instantaneous Reactive Power (IRP) theory [125], Adaline based control algorithm [79], Model Reference Adaptive Control (MARC), use of wavelet filtering for compensation of rapidly changing harmonics [126] and a scheme based on neural network techniques [127]. Among these control schemes, IRP and SRF theories are most widely used [13]. However, IRP theory is used in the present work because of its ease of implementation, excellent transient response and ability to filter inter-harmonics and sub-harmonics [13]. The step-by-step procedure for implementation of IRP theory based reference current generator for D-STATCOM controller is given below.

3.2.1.1 Reference Current Generation using IRP Power Theory

The instantaneous reactive power theory (*p-q* or IRP theory) is based on a set of instantaneous powers defined in the time domain. It can be applied to three-phase systems with or without a neutral wire.

Let the system terminal voltages be given as,

$$\begin{aligned} v_{Sa} &= v_m \sin(\omega t) \\ v_{Sb} &= v_m \sin\left(\omega t - \frac{2\pi}{3}\right) \\ v_{Sc} &= v_m \sin\left(\omega t - \frac{4\pi}{3}\right) \end{aligned} \tag{3.1}$$

and the respective load currents be given as,

$$\begin{aligned} i_{La} &= \sum i_{Lan} \sin\left(n(\omega t) - \theta_{an}\right) \\ i_{Lb} &= \sum i_{Lbn} \sin\left(n\left(\omega t - \frac{2\pi}{3}\right) - \theta_{bn}\right) \\ i_{Lc} &= \sum i_{Lcn} \sin\left(n\left(\omega t - \frac{4\pi}{3}\right) - \theta_{cn}\right) \end{aligned} \tag{3.2}$$

The *p-q* theory starts with the transformation of three-phase voltage and currents into *αβ0* stationary reference frame. This transformation is well known as Clarke transformation. The Clarke transformation maps the three-phase instantaneous voltages in the *abc*-phases, v_{Sa}, v_{Sb} and v_{Sc}, into the instantaneous voltages on the *αβ0*-axes v_α, v_β and v_0 as,

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{Sa} \\ v_{Sb} \\ v_{Sc} \end{bmatrix} \tag{3.3}$$

Similarly, three-phase instantaneous load currents in the *abc*-phases, i_{La}, i_{Lb} and i_{Lc}, are transformed into the instantaneous currents on the *αβ0*-axes i_α, i_β and i_0 as,

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{3.4}$$

One advantage of applying the *αβ0* transformation is the separation of zero-sequence components from the *abc*-phase components. The *α* and *β* axes make no contribution to the zero-sequence components. As no zero-sequence component exists in the 3P3W systems, v_0 and i_0 can be eliminated in equations (3.3) and (3.4), respectively.

Elimination of v_0 from equation (3.3) leads to,

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{Sa} \\ v_{Sb} \\ v_{Sc} \end{bmatrix} \tag{3.5}$$

Similarly, elimination of i_0 from equation (3.4) leads to,

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{3.6}$$

The instantaneous real power (*p*) and the instantaneous reactive power (*q*) are defined from instantaneous phase voltages and load currents on the *αβ0* axes as,

$$p = v_\alpha i_\alpha + v_\beta i_\beta \tag{3.7}$$

$$q = -v_\beta i_\alpha + v_\alpha i_\beta \tag{3.8}$$

Equations (3.7) and (3.8) can be written in matrix form as,

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{3.9}$$

Instantaneous active and reactive powers *p* and *q* can be decomposed into an average (dc) and an oscillatory component (ac) as,

$$p = \bar{p} + \tilde{p} \tag{3.10}$$

$$q = \bar{q} + \tilde{q} \tag{3.11}$$

The above power components can be defined as,

$\bar{p}$ = dc component of the instantaneous power *p,* which is related to the conventional fundamental active current.

$\tilde{p}$ = ac component of the instantaneous power *p* having zero average value, which is related to the harmonic currents caused by the ac component of the instantaneous real power.

$\bar{q}$ = dc component of the imaginary instantaneous power *q*, which is related to the reactive power generated by the fundamental components of voltages and currents.

$\tilde{q}$ = ac component of the instantaneous imaginary power *q*, which is related to the harmonic currents caused by the ac component of instantaneous reactive power.

Once the calculated real and reactive powers are separated into their average and oscillating parts, the undesired portions of the real and imaginary powers of the load that should be compensated with D-STATCOM can be selected.

3.2.1.2 Reference Current Generation under Non-ideal Supply Voltage

The presence of unbalance and/or distortion in the supply voltage can affect the performance of the D-STATCOM. In ideal conditions, the supply voltage consists of only positive sequence components. However, with unbalanced voltage condition, the system voltage may contain negative and zero sequence components at fundamental frequency. If distortions are also present, then the system voltage may contain negative and zero sequence components of any frequency. Therefore, with unbalanced/distorted voltage conditions, it is impossible for the source to draw sinusoidal and balanced source currents at a constant real power. Hence, for proper compensation under unbalanced/distorted voltage conditions, compensating currents for D-STATCOM must be calculated from the fundamental positive-sequence voltage components. To accomplish this, a fundamental positive sequence voltage detector is required. A fundamental positive sequence voltage detector depicted in Fig. 3.2 extracts the instantaneous values $v_{\alpha+}$ and $v_{\beta+}$ of the fundamental positive-sequence components of the three-phase source voltages [13, 128]. An important part of the positive sequence voltage detector is the Phase Locked Loop (PLL) circuit. The PLL circuit tracks continuously the fundamental frequency (ω_1) of the measured ac system voltages. The PLL is designed to operate properly under distorted and unbalanced voltage waveforms. The frequency (ω_1) is used in a sine wave generator to produce the three auxiliary currents, i'_a, i'_b and i'_c. The phase angle and the amplitude of these sine signals are not important, except that they must maintain 120º among themselves and have unity amplitudes. These currents are transformed into the αβ0-reference frame as,

$$\begin{bmatrix} i'_\alpha \\ i'_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i'_a \\ i'_b \\ i'_c \end{bmatrix} \tag{3.12}$$

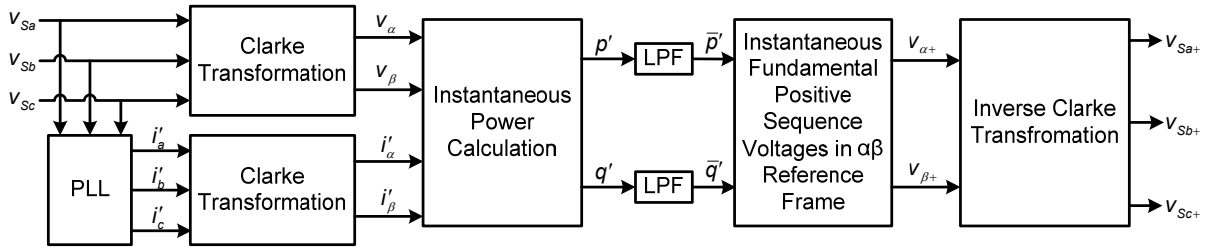


Fig. 3.2: Block diagram of a fundamental positive-sequence voltage detector.

In positive sequence voltage detector, the measured voltages v_{Sa}, v_{Sb} and v_{Sc} are transformed into the *αβ*0-reference frame to determine v_α and v_β. These transformed voltages are used together with the auxiliary currents i'_α and i'_β, produced in the PLL circuit, to calculate the auxiliary powers p' and q', as given in equations (3.13) and (3.14) respectively.

$$p' = v_\alpha i'_\alpha + v_\beta i'_\beta \tag{3.13}$$

$$q' = v_\beta i'_\alpha - v_\alpha i'_\beta \tag{3.14}$$

These calculated auxiliary powers contain both average and oscillating components. The average powers $\bar{p}'$ and $\bar{q}'$ are composed from the fundamental positive sequence voltage, since the auxiliary currents i'_α and i'_β are obtained from a fundamental positive sequence component. On the other side, the oscillating components of the powers $\tilde{p}'$ and $\tilde{q}'$ are due to the influence of the fundamental negative sequence voltage and harmonics.

These oscillating components of the powers $\tilde{p}'$ and $\tilde{q}'$ must be excluded from the inverse voltage calculation. Two fifth-order Butterworth low-pass filters (LPFs) with cut-off frequency equal to 50 Hz are used for obtaining the average powers $\bar{p}'$ and $\bar{q}'$ [13].

Once these average powers are separated then the instantaneous fundamental positive sequence voltages $v_{\alpha+}$ and $v_{\beta+}$ are calculated as,

$$\begin{bmatrix} v_{\alpha+} \\ v_{\beta+} \end{bmatrix} = \frac{1}{\sqrt{i'^2_\alpha + i'^2_\beta}} \begin{bmatrix} i'_\alpha & -i'_\beta \\ i'_\beta & i'_\alpha \end{bmatrix} \begin{bmatrix} \bar{p}' \\ \bar{q}' \end{bmatrix} \tag{3.15}$$

These instantaneous voltages in *αβ*0-reference frame are either directly used in D-STATCOM controller or transformed back to *abc*-reference frame as,

$$\begin{bmatrix} v_{Sa+} \\ v_{Sb+} \\ v_{Sc+} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_{\alpha+} \\ v_{\beta+} \end{bmatrix} \tag{3.16}$$

3.2.1.3 Compensation of D-STATCOM Losses

Ideally, there is no loss in the D-STATCOM circuit; therefore, there is no active power exchange between it and the power system and the capacitor voltages remain constant. However, in practice, the D-STATCOM has switching losses associated with the PWM operation of its semiconductor switches. If this energy is supplied by the dc-link capacitor(s), the capacitors will gradually discharge and their voltages would progressively reduce thereby affecting the performance of the D-STATCOM adversely.

In order to maintain the dc link voltage at a constant value, a small amount of average real power (P_{loss}) must be drawn continuously from the power system to supply switching and ohmic losses in the PWM inverter. This can be done by adding a dc voltage regulator to the control strategy. The dc voltage controller has a task of determining the real component of the current to be drawn by the D-STATCOM to compensate for the power losses in the inverter thereby maintaining the voltages(s) of the capacitor(s) at their reference value. In dc voltage controller, the reference and the actual dc bus voltages are compared and the error is processed in a PI controller. The output of the PI controller gives the required active power for the compensation of losses in the D-STATCOM.

3.2.1.4 Calculation of Reference D-STATCOM Currents

Let p_C and q_C be the powers to be compensated with D-STATCOM, then the compensating currents of the D-STATCOM are calculated in *αβ0*-reference frame as,

$$\begin{bmatrix} i^*_{C\alpha} \\ i^*_{C\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} -p_C \\ -q_C \end{bmatrix} \tag{3.17}$$

The reason for including negative signs in the compensating powers is to emphasize the fact that the D-STATCOM should draw a compensating current that produces the exact negative of the undesirable powers drawn by the non-linear/reactive load.

Let P_{loss} be the compensating power required to maintain the dc bus voltage to its reference value. As a result, equation (3.17) becomes,

$$\begin{bmatrix} i^*_{C\alpha} \\ i^*_{C\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} -p_C + p_{Loss} \\ -q_C \end{bmatrix} \tag{3.18}$$

These compensating currents in $\alpha\beta 0$ - reference frame can be transformed back to *abc* quantities using Inverse Clarke's transformation as,

$$\begin{bmatrix} i^*_{Ca} \\ i^*_{Cb} \\ i^*_{Cc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i^*_{C\alpha} \\ i^*_{C\beta} \end{bmatrix} \tag{3.19}$$

3.2.1.5 Selection of Compensating Powers

The rating, size and compensating characteristics of the D-STATCOM depend on the selection of the powers to be compensated. The method presented below is used for compensating harmonic and reactive current components contained in the load current.

For compensation of reactive power along with the harmonics, the powers $\tilde{p}$ and q must be compensated. This means that all the undesired current components of the load are being eliminated. As a result, the compensated source current is sinusoidal, which produces a constant real power and does not generate any imaginary power. The combination of non-linear load and the D-STATCOM forms an ideal, linear and purely resistive load. Hence, the source current has a minimum rms value that transfers the same energy as the original load current producing the average real power $\bar{p}$. The separation of $\bar{p}$ from p can be done by using a fifth-order Butterworth low-pass filter with a cut-off frequency between 20 to 100 Hz [13]. Then, the oscillating real power is determined by the difference, that is, $\tilde{p} = p - \bar{p}$.

With compensation of $\tilde{p}$ and q, equation (3.18) becomes,

$$\begin{bmatrix} i^*_{C\alpha} \\ i^*_{C\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} -(p - \bar{p}) + p_{Loss} \\ -q \end{bmatrix} \tag{3.20}$$

These compensating currents in $\alpha\beta 0$-reference frame can be transformed back to *abc* quantities using inverse Clarke's transformation as,

$$\begin{bmatrix} i^*_{Ca} \\ i^*_{Cb} \\ i^*_{Cc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i^*_{C\alpha} \\ i^*_{C\beta} \end{bmatrix} \tag{3.21}$$

3.2.2 PWM Current Controller

The reference compensating currents calculated in equation (3.19) are compared with the actual D-STATCOM currents (i_{Ca}, i_{Cb} and i_{Cc}). The differences of these currents are processed in PI controllers. The outputs of the PI controllers set the three-phase reference signals (modulating signals) for the PWM technique implemented in the controller. To produce PWM switching patterns for the switching devices, the PWM controller compares the reference signals with their corresponding triangle carrier signals. The switching operation of the power electronics devices automatically forces the D-STATCOM currents to follow the generated reference compensating currents.

Fig. 3.3 shows the complete block diagram of D-STATCOM controller for harmonic elimination and reactive power compensation.

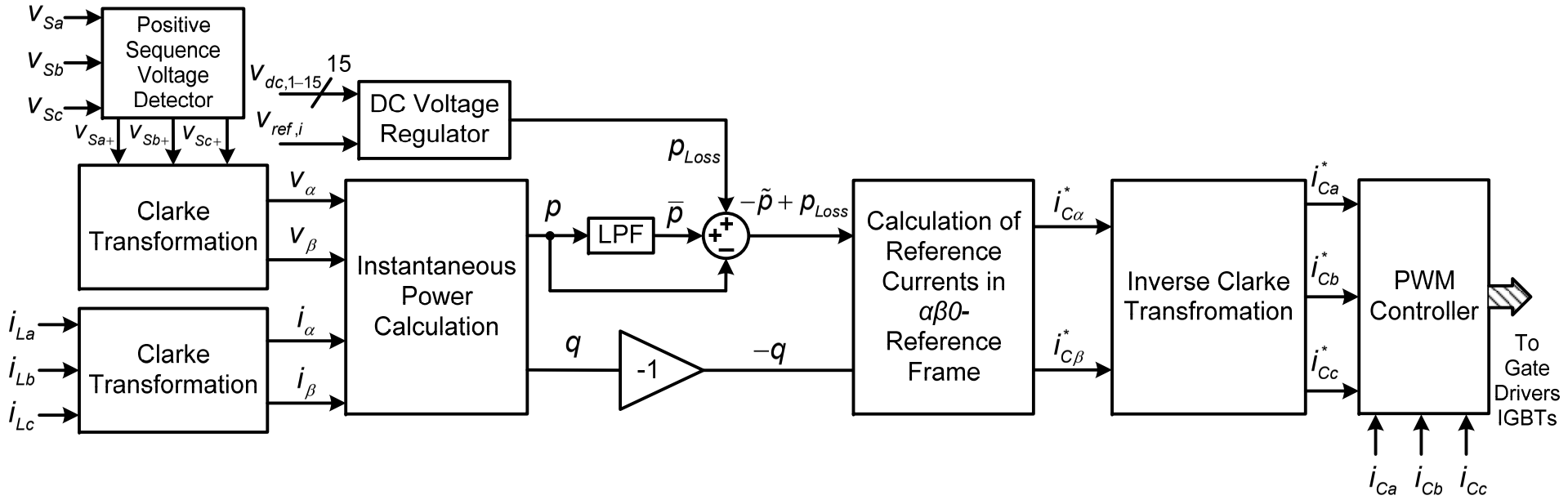


Fig. 3.3: Block diagram of a D-STATCOM controller for harmonic elimination and reactive power compensation.

3.3 Design of an 11 kV, 1 MVA Transformerless D-STATCOM for 3P3W System

The SSBC based PWM D-STATCOM for medium-voltage application has attracted the attention of power electronics researchers/engineers who are interested in reactive power compensation and/or harmonic compensation.

To design a voltage source PWM inverter based D-STATCOM for medium or high-voltage system, the inverter must be equipped with a transformer for galvanic isolation and voltage matching between the industrial/utility distribution system voltage and the inverter voltage. However, weight and size of the transformer is more than 50% of the overall weight and size of the power converter [96]. To address this problem, a new type of transformer based on power electronics circuits has been presented in [129] for voltage transformation, galvanic isolation and power quality enhancements. However, this method requires additional power electronic circuits and adds to the cost of the converter. To alleviate this problem, the focus of this research is to design a SSBC based D-STATCOM without any line frequency transformer.

To design a SSBC based PWM D-STATCOM without any line frequency transformer, let N be the number of cascaded voltage source H-bridge converters in each phase. Now, according to [102], the voltage (V_{dc}) required to be maintained in each capacitor of the H-bridge cell for proper operation of D-STATCOM is given as,

$$V_{dc} = k\frac{V_S}{N\sqrt{3}} \tag{3.22}$$

where, V_s is the system voltage (line-to-line) and k is the design parameter.

The value of k should be properly selected as the performance of the D-STATCOM depends on it. The minimum value of k is $\sqrt{2}$ but, for optimal performance k is selected from the range 1.5 to 2.5 [76].

3.3.1 Selection of Cascade Number (N) for an 11 kV System

The cascade number is one of the most important design parameters, which accounts for the blocking voltage of the switching devices used in the D-STATCOM. It also directly affects the cost, size and performance of the converter. With a cascade number of N, the phase voltage has a ($2N$+1) level waveform while the line to line ac voltage has a ($4N$+1) level waveform. If the cascade number is low, then the required dc voltage reference is high and expensive switching devices are required. On the other hand, if the cascade number is very high, then the required dc voltage reference is low but more number of switching devices are necessary. Hence, an optimum value of cascade number should be selected. Table 3.1 shows design examples of selecting the cascade number for an 11 kV SSBC based PWM D-STATCOM. It is to be noted that in Table 3.1, the carrier rotation based PWM technique is used for switching the individual H-bridge converter. From Table 3.1 following observations are made:

- Selection of lower value of N will reduce the size of the converter but necessitates the use of high power switching devices.
- Selection of higher value of N will reduce the %THD and use of mature low power switching devices but the converter size and design complexities will increase.

A cascade number of N = 5 is chosen, considering %THD, the dc voltage requirement and the voltage rating of the IGBTs to be used. With N = 5, the dc voltage of individual H-bridge cells can be kept between 1900 to 3200 V. An 11-level (N = 5) transformerless SSBC based D-STATCOM for three-phase three-wire (3P3W) system is shown in Fig. 3.4.

Table 3.1: Design examples for selecting the cascade number for an 11 kV D-STATCOM.

Cascade number (N)	DC voltage reference of each H-bridge cell (V)		Number of levels in line-to-neutral voltage	Number of levels in line-to-line voltage	% THD (line-to-line)*
	k = 1.5	k = 2.5			
2	4763	7939	5	9	17.2
3	3175	5292	7	13	10.4
5	1905	3175	11	21	6.83
7	1361	2268	15	29	3.14
9	1050	1764	19	37	1.46
11	866	1443	23	45	0.92

* with amplitude modulation index (m_a) = 1.0, carrier signal frequency (f_{cr}) = 3 kHz and LSPWM technique.

3.3.2 Selection of Reference DC Voltage for each H-bridge Cell

For optimum performance of D-STATCOM, the value of reference dc voltage for each H-bridge cell ($V_{ref,i}$) must be carefully selected. For k = 2, the reference dc voltage for each H-bridge cell is calculated to be 2540 V. Thus, $V_{ref,i}$ of the value of 2500 V is selected.

3.3.3 Selection of Passive Parameters for D-STATCOM

Based on the specific applications, operating requirements, system configurations and control strategies, ratings of various components of D-STATCOM such as dc capacitor and inductance of coupling reactor are selected [52, 53, 55, 130].

The design of these components is based on the following assumptions [130]:

1. The ac source voltage is balanced and sinusoidal.
2. AC side line current distortion is assumed to be less than 5% after compensation with D-STATCOM.
3. Reactive power compensation capability of D-STATCOM is fixed.
4. PWM inverter is assumed to operate in the linear modulation mode (i.e. $0 \leq m_a \leq 1$, m_a = amplitude modulation index).
5. The coupling inductor resistance R_c is neglected.

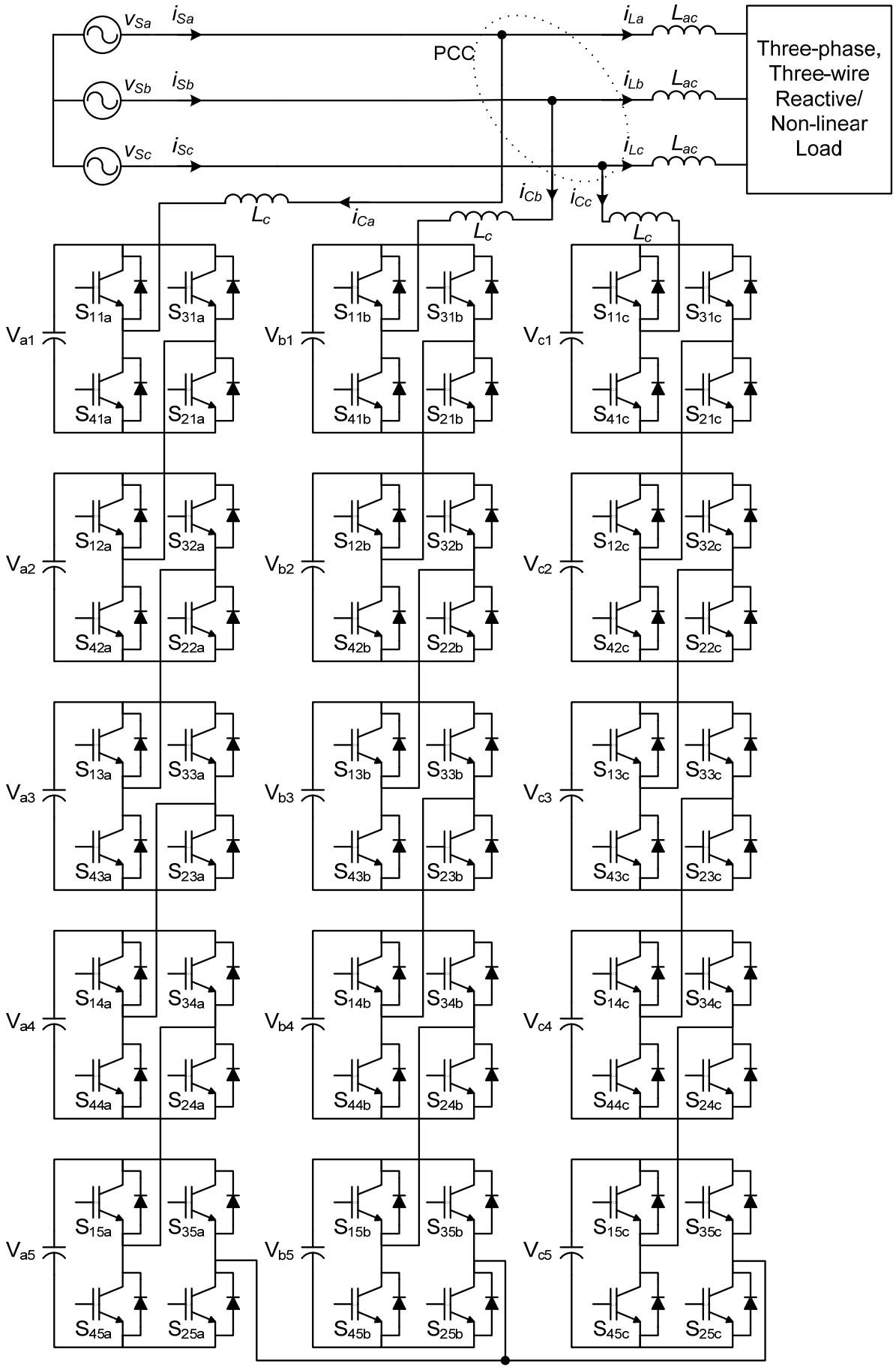


Fig. 3.4: 11-level SSBC based D-STATCOM for harmonic elimination and reactive power compensation in 3P3W distribution system.

3.3.3.1 Selection of DC Capacitors

In D-STATCOM application, each H-bridge cell in SSBC based modular multilevel inverter is equipped with an isolated dc capacitor with a suitable capacitance value. The selection of dc capacitor rating is based on the Unit Capacitance Constant (*UCC*) given in [131], and it is defined as a ratio between the capacitor-stored energy in joules and the power conversion capacity of the inverter in watts.

$$UCC = \frac{1}{2} C_{dc} V_{dc}^2 / Q \tag{3.23}$$

In general, *UCC* ranges from 30 to 40 ms (for a ripple voltage in the range of 10%), and it is determined by taking into account various factors including the objective, voltage class, system configuration and power circuit of a D-STATCOM being installed [96, 132].

Based on *UCC*, the capacitance required for each capacitor (C_{dc}) of the H-bridge of a SSBC inverter is estimated as follows:

Here, V_{dc} is the reference dc voltage of each H-bridge cell and Q is the power-conversion capacity of each H-bridge cell.

The power conversion capacity of each H-bridge cell for SSBC based modular multilevel inverter is defined as follows:

$$Q = \frac{Power\ conversion\ capacity\ of\ the\ inverter}{Number\ of\ phases\ in\ the\ inverter\ X\ Cascade\ Number} \tag{3.24}$$

Considering V_{dc} = 2500 V, N = 5, *UCC* = 35 ms (for a ripple voltage in the range of 10%) and with a 1 MVA power conversion capability of the inverter, the calculated value of C_{dc} is 746 μF.

3.3.3.2 Selection of Coupling Inductor

PWM converters generate undesirable current harmonics around the switching frequency and its multiples. If the switching frequency of the PWM converter is sufficiently high, these undesirable current harmonics can be easily filtered out by the coupling inductor. The coupling inductor (L_c) is one of the key components, which determine the performance of the D-STATCOM [130]. The connection of the coupling inductor to the ac system is shown in Fig. 3.4.

The selection of the ac inductance depends on the current ripple ($i_{cr,(p-p)}$) and switching frequency of the inverter (f_c). The approximate value of the ac inductance is given as [52]:

$$L_C = \frac{\sqrt{3} m_a V_c}{12 a f_c i_{cr,(p-p)}} \tag{3.25}$$

Here, switching frequency of the inverter (f_c) depends on the PWM method used for controlling the inverter. For carrier rotation based level-shifted PWM technique with carrier signal frequency f_{cr}, f_c can be calculated as:

$$f_c = 2 N f_{cr} \tag{3.26}$$

Considering 5% peak-to-peak current ripple $i_{cr,(p-p)}$ to be 2.6 A rms $\left(\text{rated current} = \frac{1\times10^6}{\sqrt{3}\times11\times10^3}\right)$, the switching frequency of the converter ($2Nf_{cr}$) = $2\times5\times3$ kHz = 30 kHz, amplitude modulation index (m_a) = 1, phase-to-neutral or cluster voltage of the inverter (V_c) = $N\times V_{ref,i}$ = 12.5 kV and overload factor (a) = 1.2, the value is calculated to be 19.28 mH.

On one hand, for a better harmonic cancellation and reactive power compensation a higher value of inductance is preferable. However, on the other hand, a very high value of inductance will result in slow dynamic response of the shunt compensator and it would not be possible to compensate some of the load harmonics [130]. Therefore, an optimum value of inductance is to be obtained. To further optimize the value of the coupling inductor, system performance is investigated around the calculated value of the coupling inductor for the system parameters given in Table 3.2. In Table 3.2, the source impedance Z_s and commutation inductance L_s are assumed to be the inherent parameters of source and three-phase rectifier respectively, therefore in some diagrams they are not shown for simplicity.

The concepts of cluster voltage balancing control and individual voltage balancing control are described in subsections 3.3.4.1 and 3.3.4.2 respectively.

Table 3.2: Parameters used in the simulation study for selecting coupling inductor.

Parameter	**Value**
AC line voltage	Three-phase, three-wire, 11 kV, 50 Hz
Source impedance (Z_s)	R_s = 0.1 Ω, L_s = 0.1 mH
DC bus reference voltage	2500 V (for each capacitor in the H-bridge cell)
DC bus capacitance	746 μF (for each capacitor in the H-bridge cell)
Commutation inductance	L_{ac} = 2 mH
PWM switching frequency	3 kHz
PI controller parameters	For cluster voltage balancing control: K_p = 1.3, K_i = 0.8 For individual voltage balancing control: K_p = 1.1, K_i = 1.5.
Load	Three-phase phase-controlled rectifier, R_{dc} = 300 Ω, L_{dc} = 500 mH, firing angle = 30°.

Table 3.3 shows the start-up performance of D-STATCOM for the selected values of coupling inductor. It is observed that the D-STATCOM performance can be significantly improved by reducing the filter inductor to an optimum value. In this work, the value of the coupling inductor is chosen as 17 mH. At this value of coupling inductor, D-STATCOM output current %THD is minimum and the system dynamic performance is satisfactory.

Table 3.3: System performance with variation of coupling inductor.

Coupling inductance L_f (mH)	Settling time (Cycles)	%THD of source current after compensation	Source power factor after compensation
13	1	4.14%	0.992
15	< 2	3.25%	0.994
17	< 2	1.69%	0.999
19	< 3	1.62%	0.999
21	3	1.01%	0.993
23	< 4	2.43%	0.990
25	4	3.92%	0.976

3.3.4 DC Voltage Regulation

Fig. 3.5 shows the controller for dc voltage regulation for an 11-level SSBC based D-STATCOM [94, 99, 101, 102, 133]. The scheme presented in Fig. 3.5 is slightly different from [94, 96, 99, 101, 102], where each phase is individually controlled. However, in this work, all three phases are controlled as a single unit. The block diagram of the controller is shown in Fig. 3.5(a). In order to tightly control the voltages of the 15 (5 per each phase) floating dc capacitors, the controller shown in Fig. 3.5(a) is divided into two following control blocks [102]:

1) Cluster voltage balancing control
2) Individual voltage balancing control

3.3.4.1 Cluster Voltage Balancing Control

Fig. 3.5(b) shows the block diagram of the cluster voltage balancing control. This controller forces the voltage of each cluster, namely, v_{Ca}, v_{Cb} and v_{Cc}, to follow the reference cluster voltage $V_{ref,c}$. The cluster voltages are defined as:

$$\begin{aligned} V_{Ca} &= V_{a1} + V_{a2} + V_{a3} + V_{a4} + V_{a5} \\ V_{Cb} &= V_{b1} + V_{b2} + V_{b3} + V_{b4} + V_{b5} \\ V_{Cc} &= V_{c1} + V_{c2} + V_{c3} + V_{c4} + V_{c5} \end{aligned} \tag{3.27}$$

Here, v_{Ca}, v_{Cb} and v_{Cc} are the instantaneous values containing both ac and dc components. It is desirable to extract only the dc components (i.e. $(v_{Ca})_{dc}$, $(v_{Cb})_{dc}$ and $(v_{Cc})_{dc}$) because the existence of the ac components deteriorates the controllability. Low-pass filters with a cut-off frequency of 15 Hz are used to eliminate the dominant 100 Hz component from the measured dc voltages [101, 102]. In cluster balancing control, each cluster voltage is calculated and compared with the cluster reference voltage $V_{ref,c}$. The cluster reference voltage ($V_{ref,c}$) can be calculated by adding the individual dc voltage references of the H-bridge cells in the cluster i.e.,

$$V_{ref,c} = N * V_{ref,i} \tag{3.28}$$

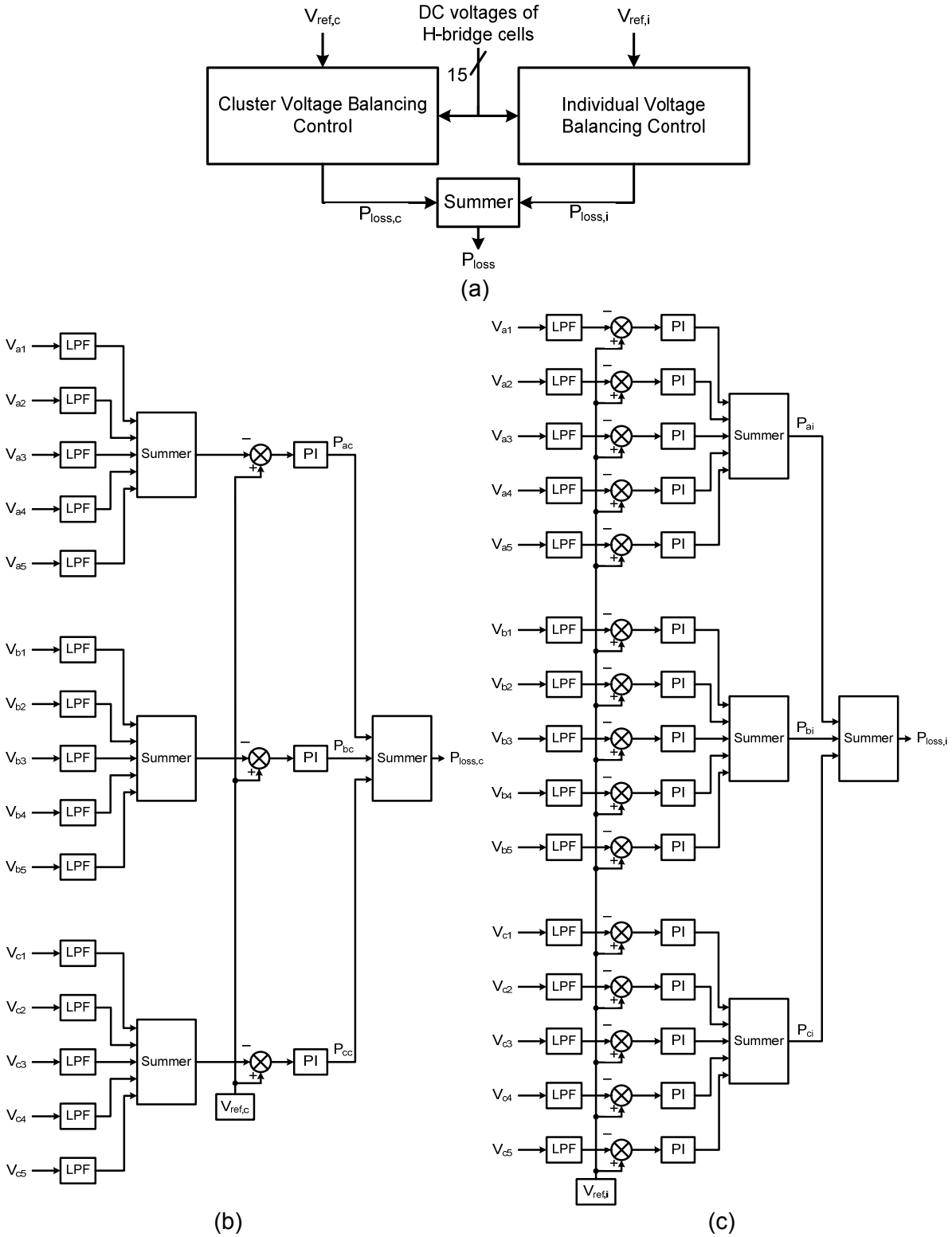


Fig. 3.5: DC voltage controller for a 11-level SSBC based D-STATCOM: (a) Block diagram; (b) Cluster voltage balancing control; (c) Individual voltage balancing control.

The errors between the individual cluster voltages and $V_{ref,c}$ are processed in PI controllers and sum of the outputs of the PI controllers ($P_{loss,c}$) decides the amount of real power required to keep the cluster voltages at their corresponding reference values. When dc voltage reference is greater than the cluster voltage, an amount of the active power flows into that particular cluster, thus leading to enhancement of cluster voltage. On the other

hand, when dc voltage reference is lower than the cluster voltage, then an amount of the active power is drawn from that particular cluster, thus leading to reduction in cluster voltage.

3.3.4.2 Individual Voltage Balancing Control

Fig. 3.5(c) shows the block diagram for the individual balancing control, which balances the voltage of individual capacitor in each cluster. In individual voltage balancing control, each capacitor voltage is compared with the dc reference voltage ($V_{ref,i}$). The error is processed in a PI controller and the output of the PI controller decides the amount of real power required to keep that particular capacitor voltage at its reference value. When dc voltage reference is greater than the capacitor voltage, an amount of the active power flows into that particular capacitor, thus leading to enhancement of capacitor voltage. On the other hand, when dc voltage reference is lower than the capacitor voltage, an amount of the active power is drawn from that particular capacitor, thereby bringing down the capacitor voltage to its reference value. The sum of the outputs of the PI controllers ($P_{loss,i}$) is the total amount of real power required to keep the capacitor voltages of individual H-bridges at their corresponding reference values. The gains of the PI controllers are properly selected to give the optimum performance.

Once the loss components of cluster and individual voltage balancing controllers are calculated, then the total compensating real power (P_{loss}) required for dc voltage regulation of D-STATCOM is calculated as:

$$P_{loss} = P_{loss,c} + P_{loss,i} \tag{3.29}$$

3.4 Performance Evaluation of 3P3W D-STATCOM

Simulation studies under different utility and load conditions are carried out to investigate the performance of the transformerless 11-level SSBC based D-STATCOM for harmonic elimination and reactive power compensation in 3P3W distribution system. The simulation study of the entire system is carried out in the MATLAB/Simulink environment, and the simulation models of the entire system are shown in Appendix A.

The reference source currents are derived from the IRP theory discussed in Section 3.2.1.1 by using the measured ac voltages, load currents and dc voltage of the individual capacitors of the H-bridge cells. A carrier rotation based LSPWM current controller is used to generate the gating signals for the IGBTs of the 11-level SSBC inverter. The parameters used in the simulation are given in Table 3.4. Extensive simulation studies are carried out to investigate the performance of D-STATCOM for harmonic elimination and reactive power compensation under different loading and utility voltage conditions. In order to study the steady-state and transient performance of D-STATCOM, the following events are assumed to occur in the system for all simulation studies:

1. At t = 0.06 sec., the D-STATCOM and its associated control circuit is connected to the system.
2. At t = 0.16 sec., an additional load (50%) is connected to the system.
3. At t = 0.26 sec., the additional load is disconnected from the system.

The simulation results are presented below for both ideal and distorted utility voltage conditions.

Table 3.4: Parameters used in the simulation study.

Parameter	**Value**
AC line voltage	Three-phase, three-wire, 11 kV, 50 Hz
Source impedance	R_s = 0.1 Ω, L_s = 0.1 mH
DC bus reference voltage	2500 V (for each capacitor in the H-bridge cell)
DC bus capacitance	746 μF (for each capacitor in the H-bridge cell)
Coupling inductor of D-STATCOM	L_c = 17 mH
Commutation inductance	L_{ac} = 2 mH
PWM switching frequency	3 kHz
PI controller parameters	For cluster voltage balancing control: K_p = 1.3, K_i = 0.8 For individual voltage balancing control: K_p = 1.1, K_i = 1.5.
Load	Three-phase uncontrolled rectifier, R_{dc} = 400 Ω, L_{dc} = 500 mH; Three-phase uncontrolled rectifier, R_{dc} = 400 Ω, C_{dc} = 400 μF; Three-phase phase-controlled rectifier, R_{dc} = 300 Ω, L_{dc} = 500 mH, firing angle = 30°. Three-phase phase-controlled rectifier, R_{dc} = 300 Ω, C_{dc} = 400 μF, firing angle = 30°.

3.4.1 Simulation Results with Ideal Voltage Conditions

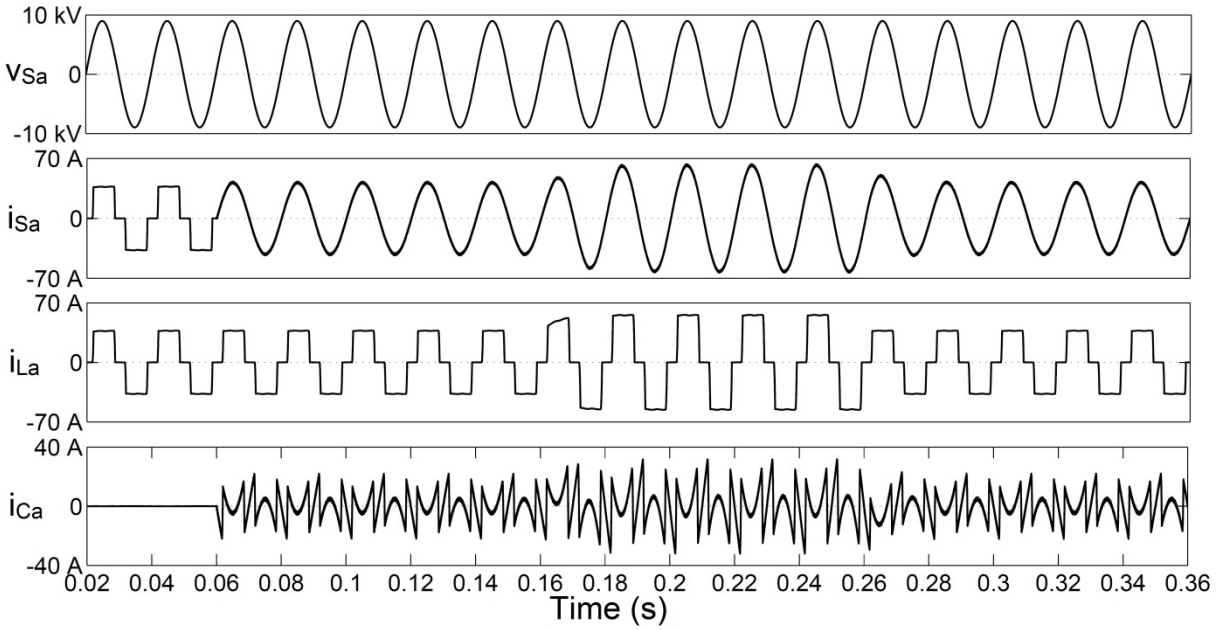
Simulation results under ideal voltage conditions with uncontrolled and phase-controlled rectifiers having *RL* and *RC* loads on their dc sides are presented in this section. In these simulation studies it is assumed that the dc capacitors are precharged to 80% of their reference voltage (i.e. 2000 V) to reduce the high currents drawn by the source during the start-up of the D-STATCOM.

3.4.1.1 Uncontrolled Rectifier with *RL* Load

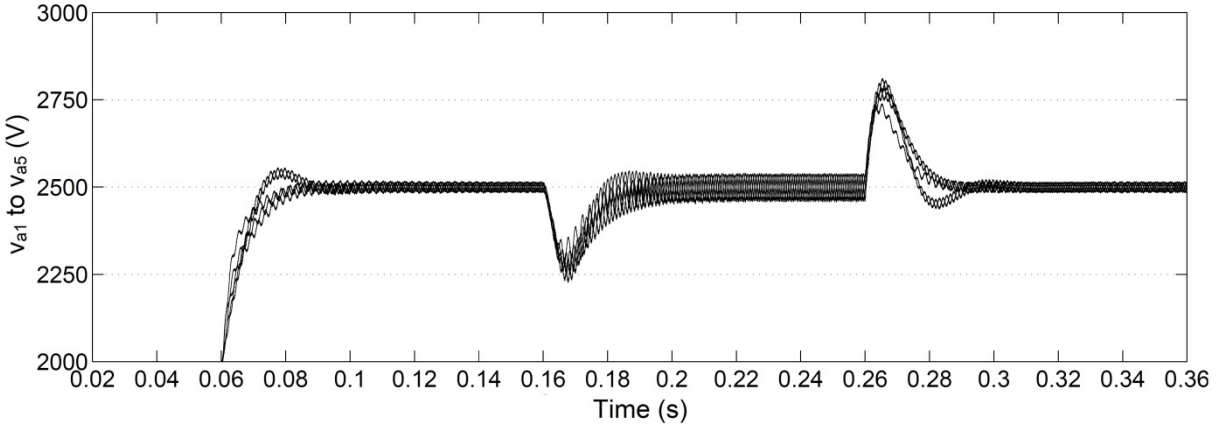
An uncontrolled rectifier with *RL* load on the dc side is considered as a non-linear load in this case. Fig. 3.6(a)-(d) shows the simulated waveforms, individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5}), harmonic spectra of load and source currents respectively with method–1 carrier rotation technique, while Fig. 3.7(a)-(d) shows these results for method–2 carrier rotation technique. Since three-phase balanced load is considered, the results corresponding to phase–*a* are shown here only. In Fig. 3.6(a), Fig. 3.7(a) and all the subsequent figures showing similar simulation waveforms, the quantities shown are as follows (from top to bottom): trace 1: phase–*a* source voltage (v_{Sa}), trace 2: phase–*a* source

current (i_{Sa}), trace 3: phase–*a* load current (i_{La}) and trace 4: phase–*a* current injected by D-STATCOM (i_{Ca}). From Fig. 3.6 and Fig. 3.7 following observations are made:

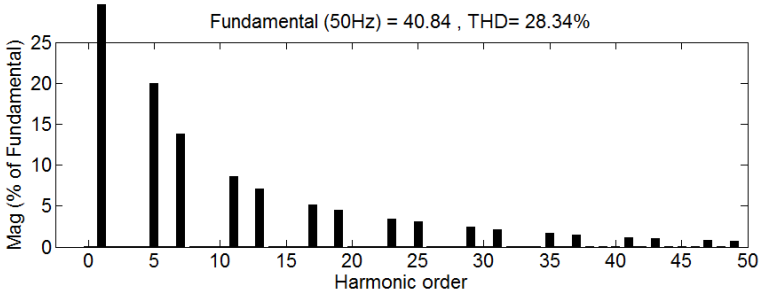
1. In both cases, at the instant the D-STATCOM is switched-on, the source current becomes sinusoidal from a stepped wave shape.
2. In both cases, steady-state is reached for all the dc capacitors of the H-bridge cells within 1–2 cycles with the smooth build-up of the capacitor voltages.
3. After compensation with D-STATCOM, the THD of the load current is 28.34%, but the source current THD is reduced to 1.53% and 1.27% with method–1 and method–2 carrier rotation techniques respectively, which are well within the limits of IEEE–519–1992 recommended value of 5%.
4. After compensation with D-STATCOM, the source current is in phase with the source voltage and confirms the compensation of reactive power. The power factor and displacement factor of the source are almost unity in both cases (0.999 lagging).
5. The rms value of load current is 30.06 A, and that of source current is 30.78 A in method–1 and 30.81 A in method–2 carrier rotation technique. The increase in the source currents is due to the compensation of power losses of the inverter.
6. In both cases, the capacitor voltage of individual H-bridge cell is well regulated at its reference value. This ensures the effectiveness of the dc voltage controller. However, with method–1 carrier rotation technique, the maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 68 V but with method–2, it is reduced to 31 V. The reduction in peak-to-peak ripple in the dc voltage of each H-bridge for method–2 carrier rotation technique is due to its fast response in equalising the conduction periods of switching devices.
7. At 0.16 sec., load current increases from 30.06 A to 44.87 A and decreased back to its original value at 0.26 sec. The corresponding change in the compensated source current is observed to be very smooth in both cases. The power factor and the displacement factor on the source side are unity not only in the steady-state condition but also in the transient condition.
8. At the instant when load current changes, the dc capacitor voltage changes from its reference value to compensate for the enhancement in the load current. This causes drop in capacitor voltage which is restored in 1–2 cycles. Similarly, drop in load current is responded by D-STATCOM with enhancement in capacitor voltage with subsequent quick restoration (in 1–2 cycles) to its reference value. The regulation of the capacitor voltages is ensured by the dc voltage regulator. A smooth control of the dc voltages in both carrier rotation techniques ensures the effectiveness of the dc voltage controller in transient condition also.



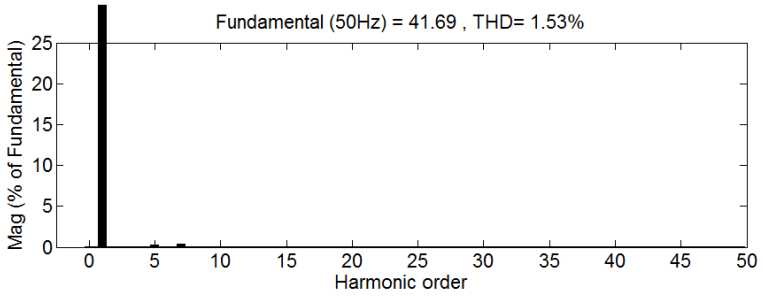
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})

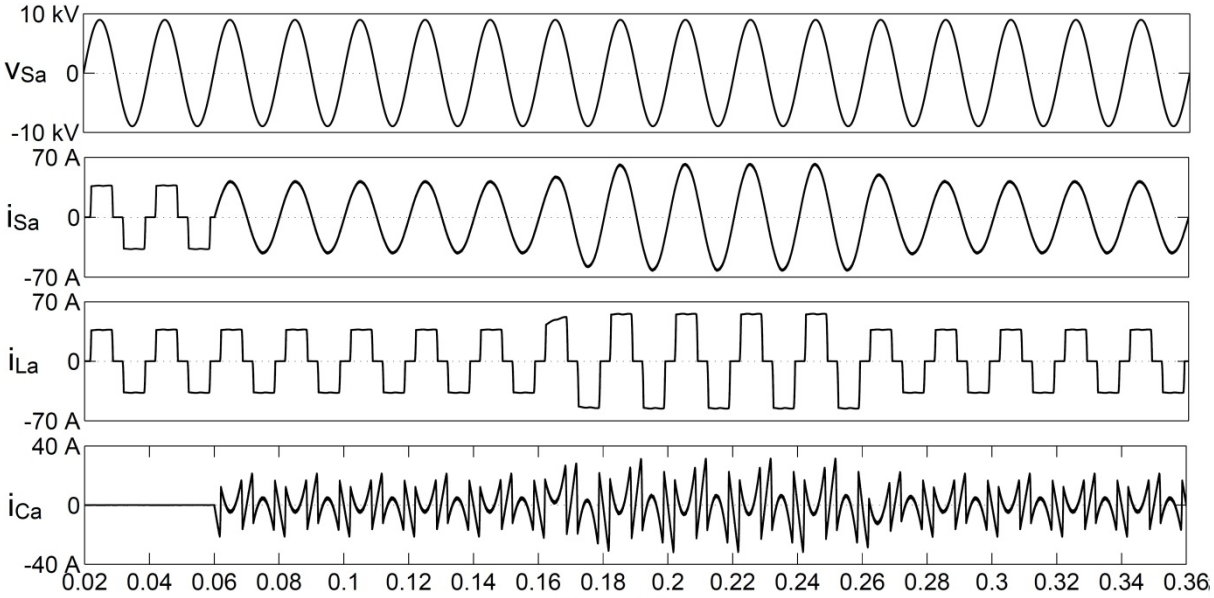


(c) Load current harmonic spectrum

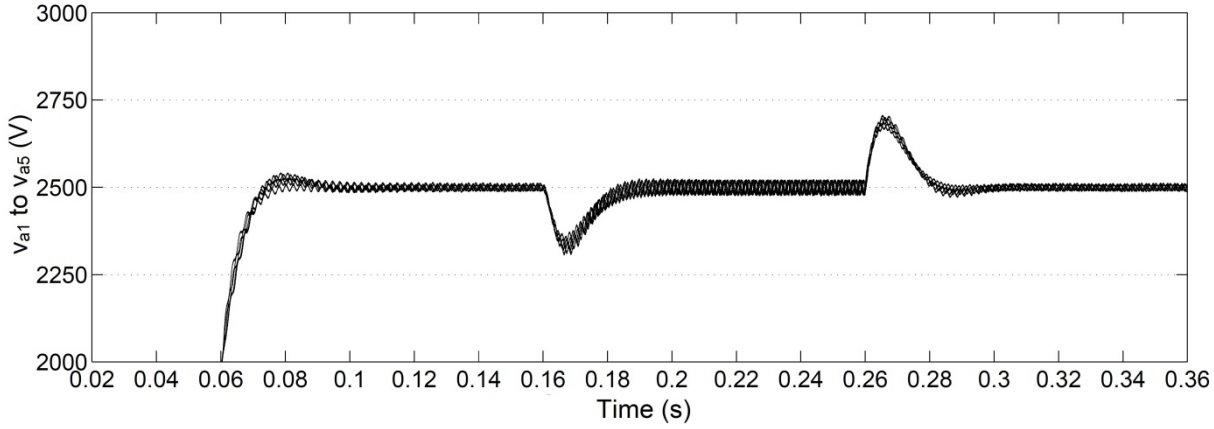


(d) Source current harmonic spectrum

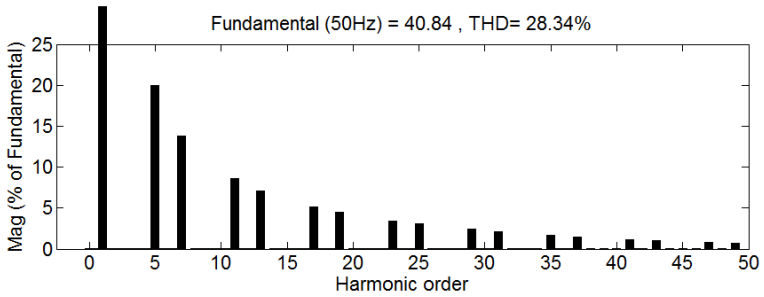
Fig. 3.6: Performance of D-STATCOM for *RL* load on the dc side of an uncontrolled rectifier with method–1 carrier rotation technique with an ideal voltage source.



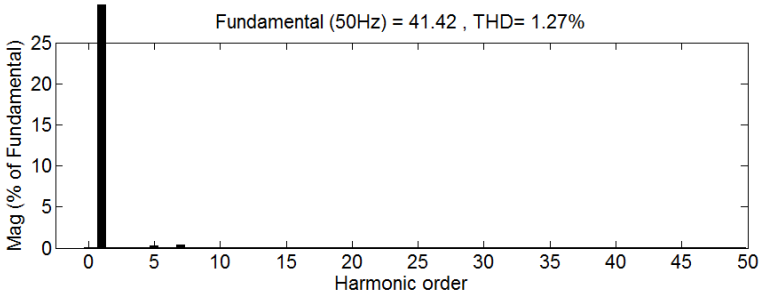
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})



(c) Load current harmonic spectrum



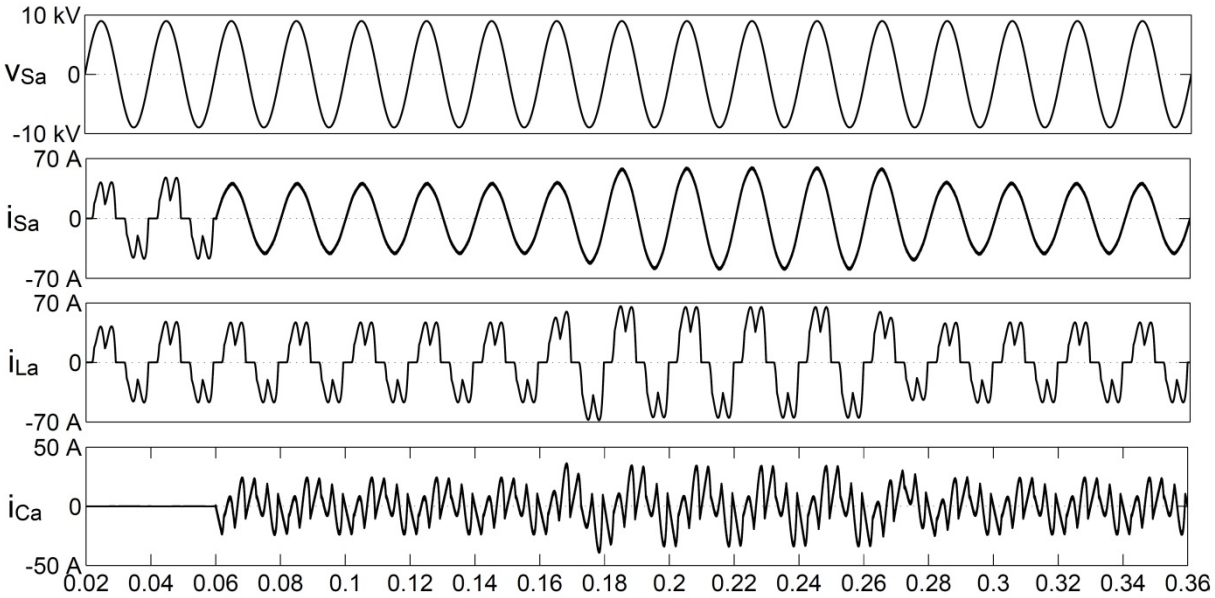
(d) Source current harmonic spectrum

Fig. 3.7: Performance of D-STATCOM for *RL* load on the dc side of an uncontrolled rectifier with method–2 carrier rotation technique with an ideal voltage source.

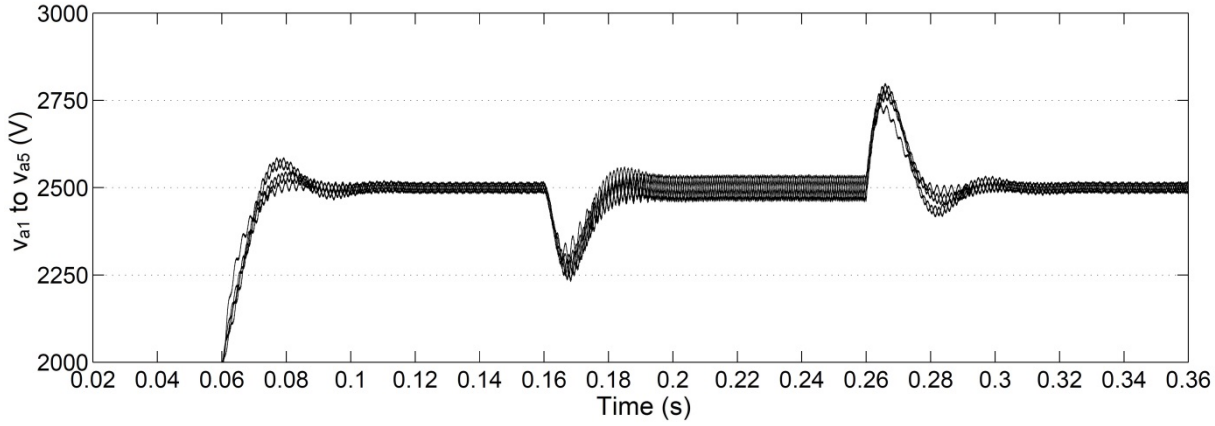
3.4.1.2 Uncontrolled Rectifier with *RC* Load

An uncontrolled rectifier with *RC* load on the dc side is considered as a non-linear load in this case. Fig. 3.8(a)-(d) shows the simulated waveforms, individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5}), harmonic spectra of load and source currents respectively with method–1 carrier rotation technique, while Fig. 3.9(a)-(d) shows these results for method–2 carrier rotation technique. From Fig. 3.8 and Fig. 3.9 it is observed that the points 1, 2, 4 and 8 of subsection 3.4.1.1 are equally valid for this case also. Apart from these, the following observations are also made:

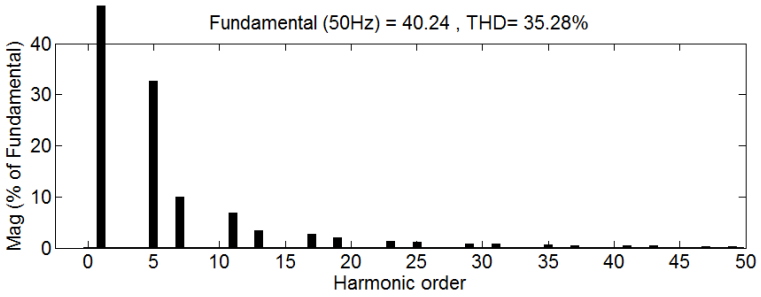
1. After compensation with D-STATCOM, the THD of the load current is 35.28%, but the source current THD is reduced to 2.15% and 2.00% with method–1 and method–2 carrier rotation technique respectively.
2. The rms value of load current is 30.17 A, and that of source current is 30.92 A in method–1 and 30.86 A in method–2 carrier rotation technique. The enhancement in the source currents is due to the compensation of real power losses of the inverter.
3. In both cases, the capacitor voltage of individual H-bridge cell is well regulated at its reference value. However, with method–1 carrier rotation technique, the maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 65 V but with method–2, it is reduced to 30 V.
4. At 0.16 sec., load current increases from 30.17 A to 43.85 A and decreased back to its original value at 0.26 sec. The corresponding change in the compensated source current is observed to be very smooth in both cases. It is also observed that with method–2 carrier rotation technique, the steady-state in capacitor voltages are achieved only in 1–2 cycle, compared with 2–3 cycles with method–1 carrier rotation technique.



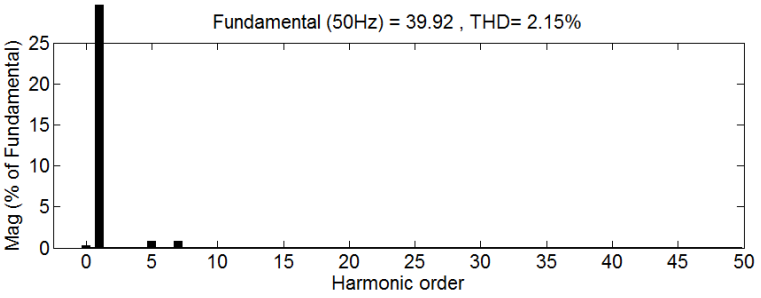
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})

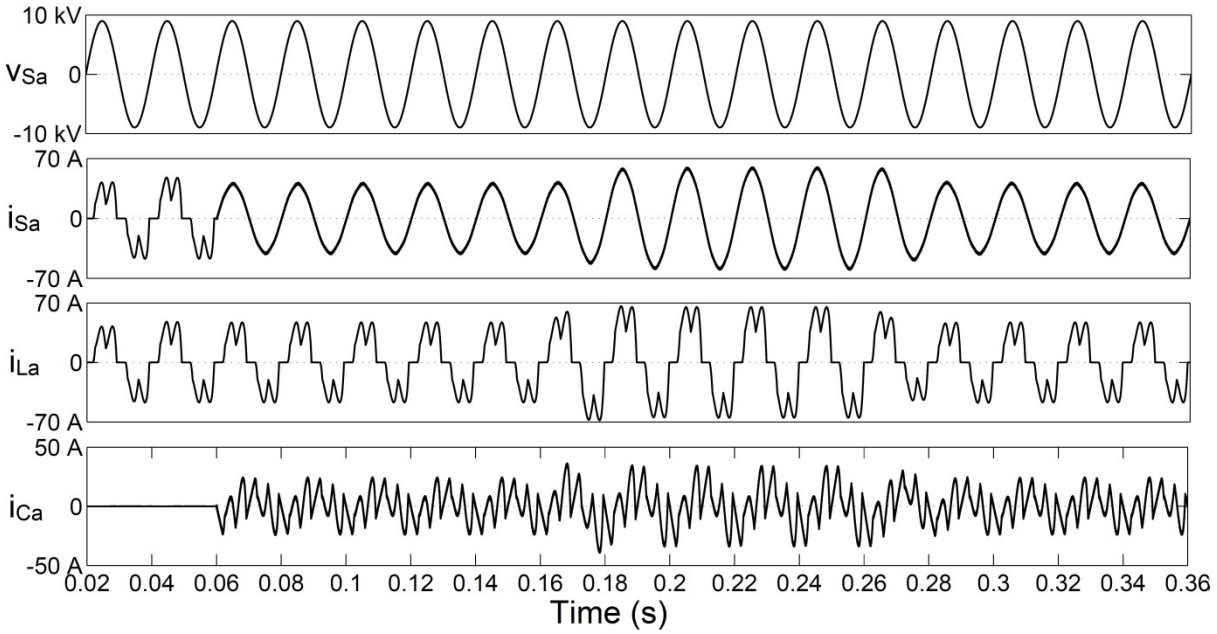


(c) Load current harmonic spectrum

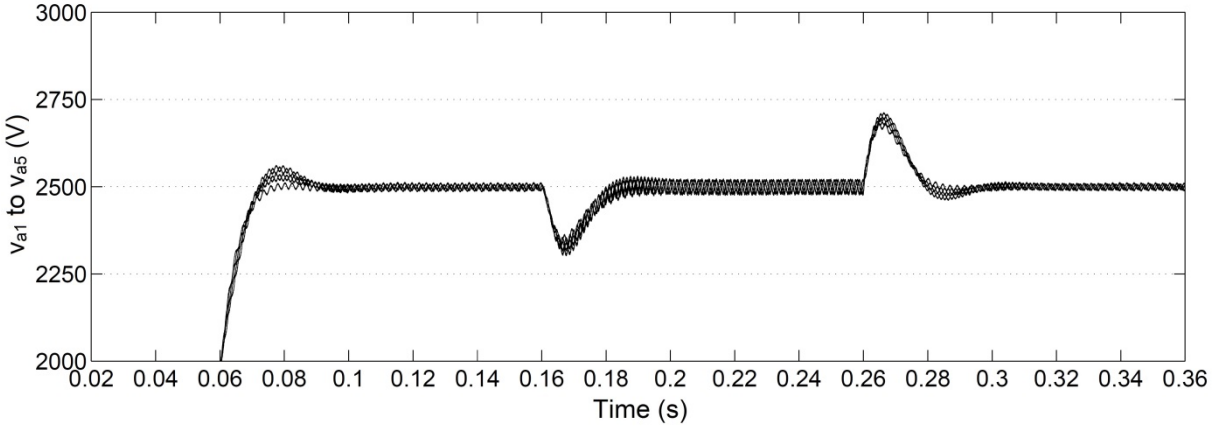


(d) Source current harmonic spectrum

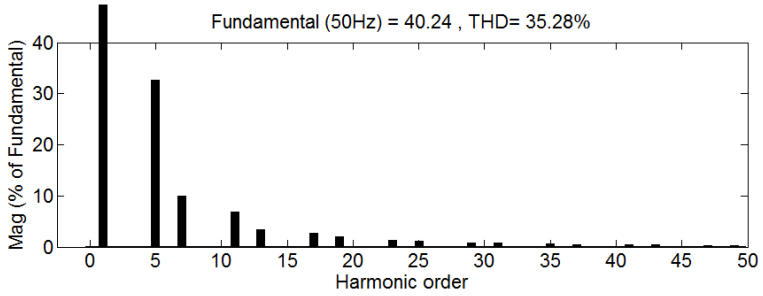
Fig. 3.8: Performance of D-STATCOM for *RC* load on the dc side of an uncontrolled rectifier with method–1 carrier rotation technique with an ideal voltage source.



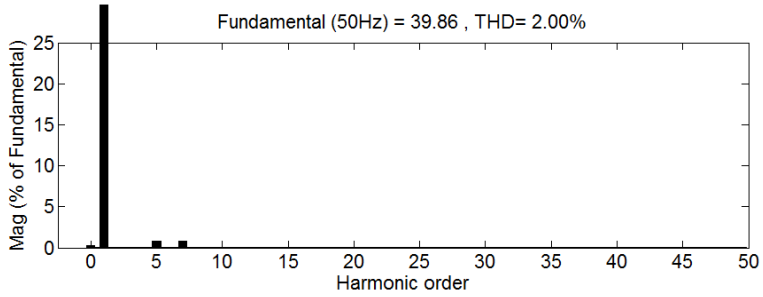
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})



(c) Load current harmonic spectrum



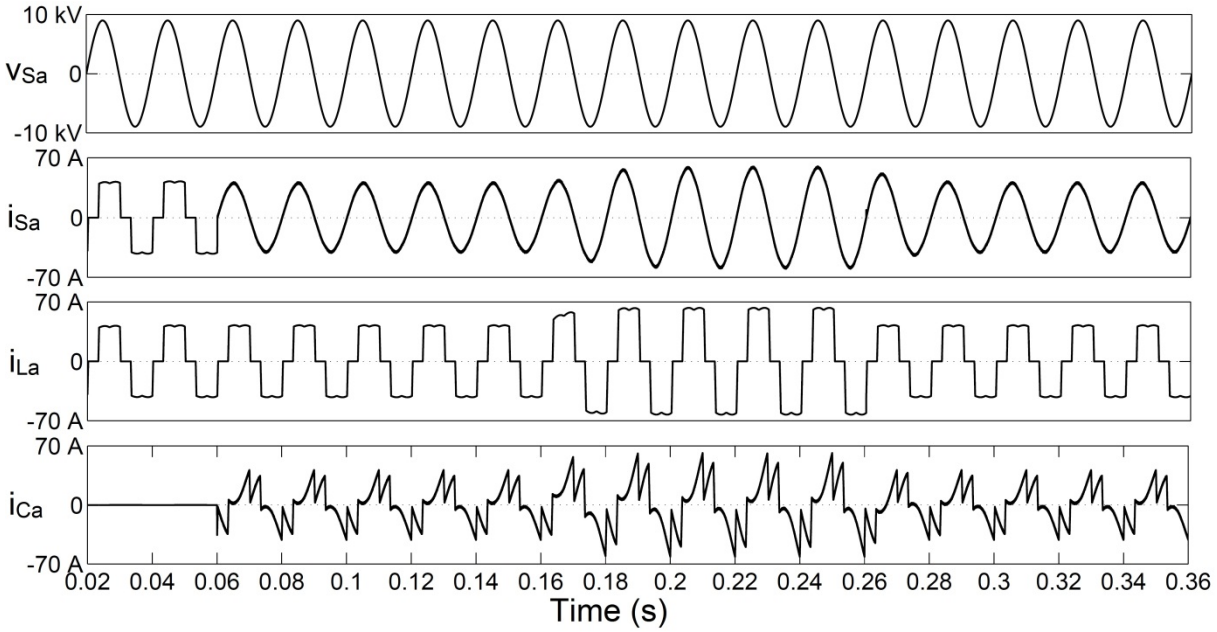
(d) Source current harmonic spectrum

Fig. 3.9: Performance of D-STATCOM for *RC* load on the dc side of an uncontrolled rectifier with method–2 carrier rotation technique with an ideal voltage source.

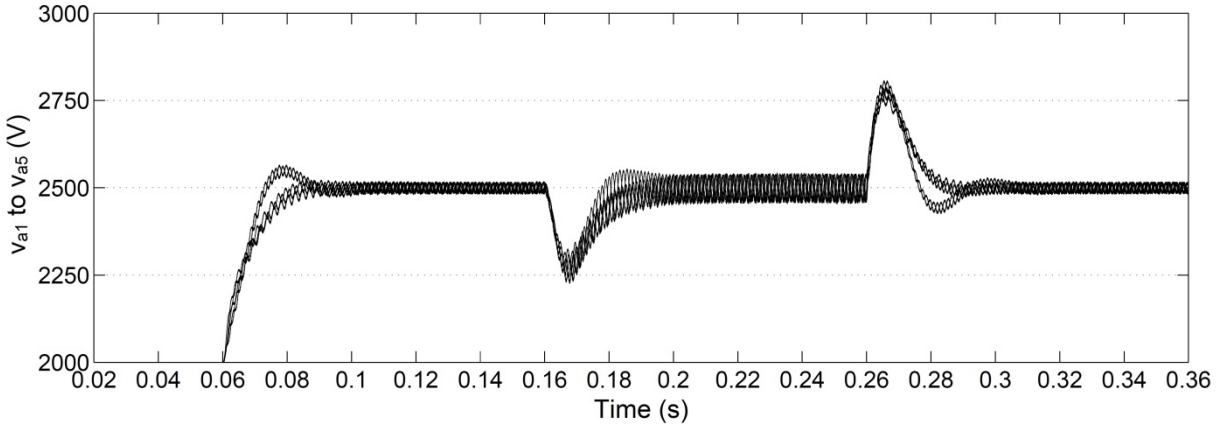
3.4.1.3 Phase-controlled Rectifier with *RL* Load

A phase-controlled rectifier operated at a firing angle of 30º with *RL* load on the dc side is considered as a non-linear load in this case. Fig. 3.10(a)-(d) shows the simulated waveforms, individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5}), harmonic spectra of load and source currents respectively with method–1 carrier rotation technique, while Fig. 3.11(a)-(d) shows these results for method–2 carrier rotation technique. From Fig. 3.10 and Fig. 3.11 it is observed that the points 1, 2 and 4 of subsection 3.4.1.1 are equally valid for this case also. Apart from these, the following observations are also made:

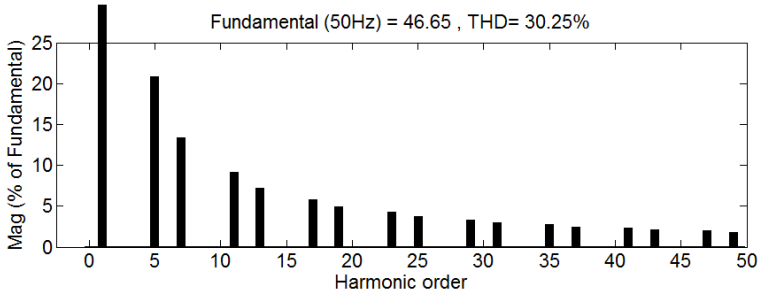
1. After compensation with D-STATCOM, the THD of the load current is 30.25%, but the source current THD is reduced to 1.85% and 1.73% with method–1 and method–2 carrier rotation techniques respectively.
2. After compensation with D-STATCOM, the source power factor is improved from 0.843 (lagging) to almost unity (0.999 lagging) in both carrier rotation techniques.
3. The rms value of load current is 33.95 A, and that of source current is 31.03 A in method–1 and 31.16 A in method–2 carrier rotation technique. The reduction in the source current is due to the compensation of load reactive power. It is to be noted that for compensating the real power loss of the inverter, the source current increases slightly. However, the reduction in the source current due to reactive power compensation is more than the enhancement of source current due to power loss compensation and therefore, overall the source current decreases.
4. With method–1 carrier rotation technique, the maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 69 V but with method–2, it is reduced to 33 V.
5. The power factor and the displacement factor on the source side are unity not only in the steady-state condition but also in the transient condition.
6. At 0.16 Sec., load current increases from 33.95 A to 50.16 A and decreased back to its original value at 0.26 Sec. The corresponding change in the compensated source current is observed to be very smooth in both cases.
7. In method–2 carrier rotation technique, the steady-state in capacitor voltages are achieved in 1–2 cycle compared to 2–3 cycles in method–1 carrier rotation technique, which ensures the fast dynamic response of method–2 carrier rotation technique.



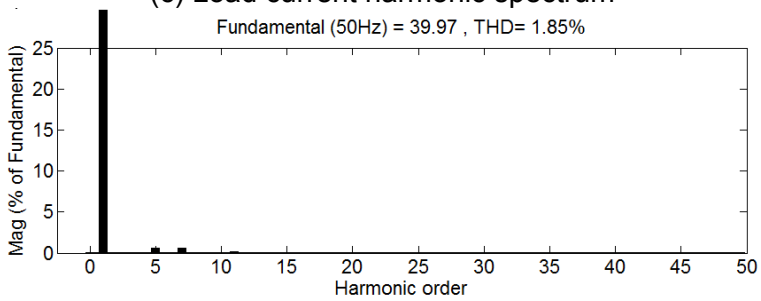
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})

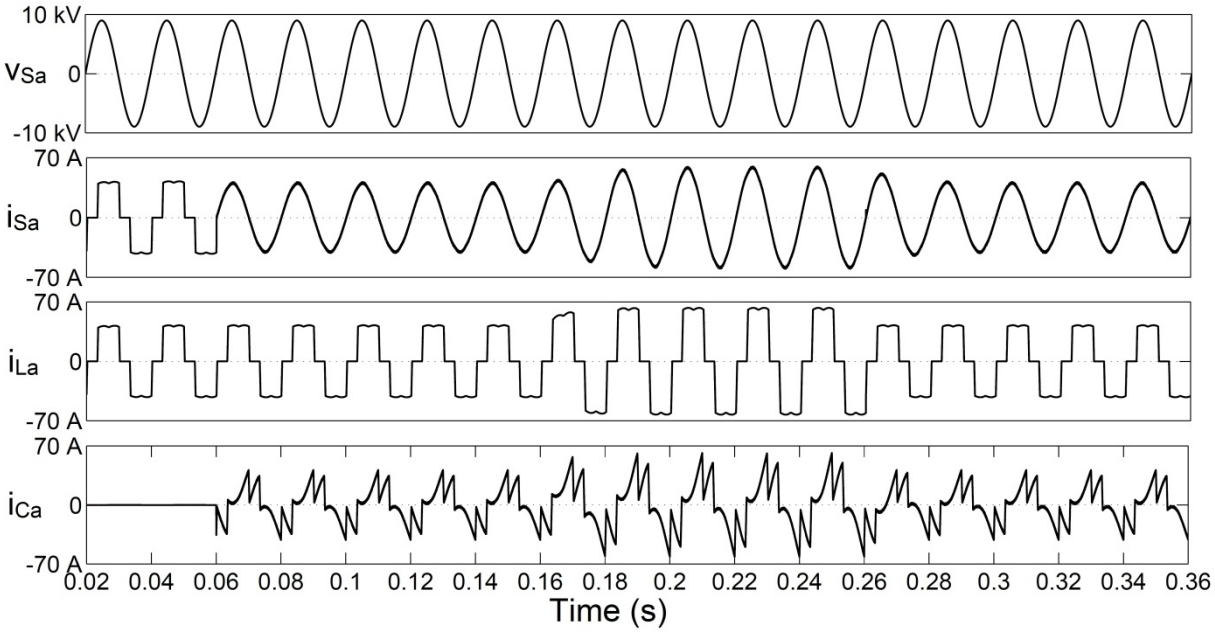


(c) Load current harmonic spectrum

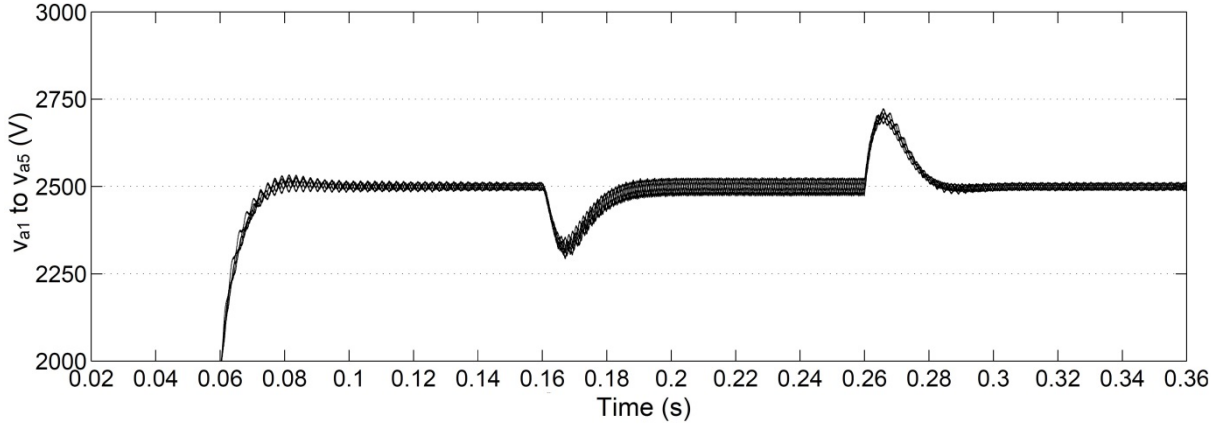


(d) Source current harmonic spectrum

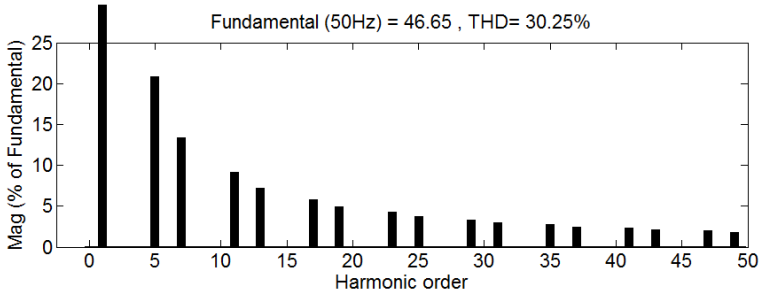
Fig. 3.10: Performance of D-STATCOM for *RL* load on the dc side of a phase controlled rectifier operated at a firing angle of 30º with method–1 carrier rotation technique with an ideal voltage source.



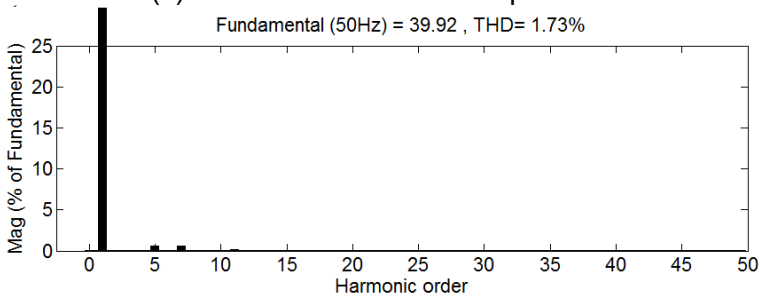
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})



(c) Load current harmonic spectrum



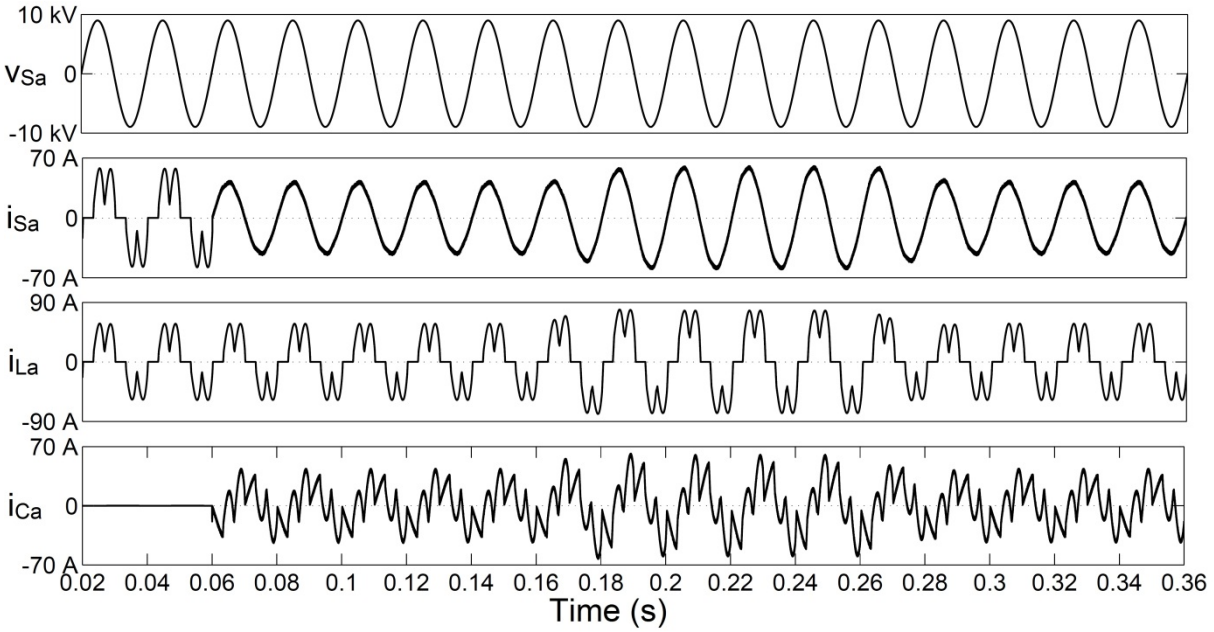
(d) Source current harmonic spectrum

Fig. 3.11: Performance of D-STATCOM for *RL* load on the dc side of a phase controlled rectifier operated at a firing angle of 30º with method–2 carrier rotation technique with an ideal voltage source.

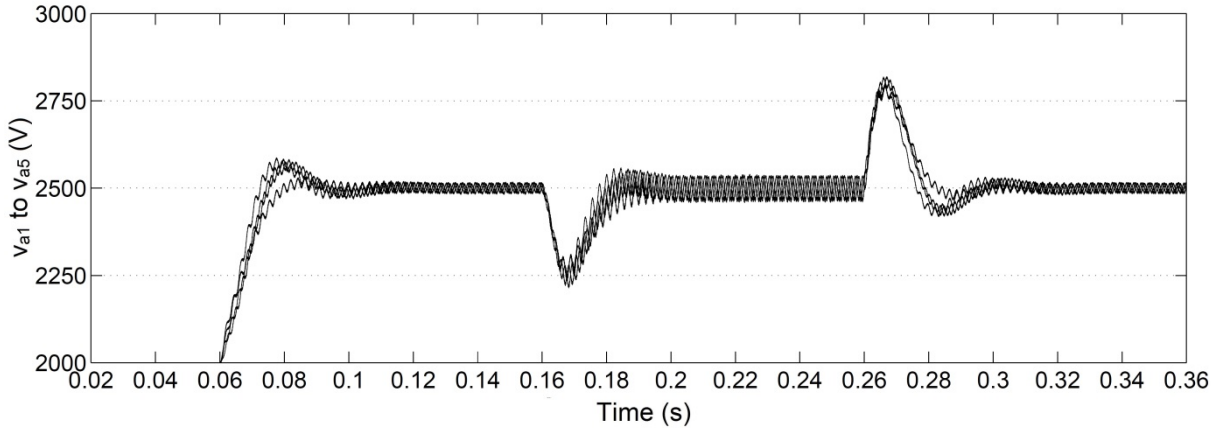
3.4.1.4 Phase-controlled Rectifier with *RC* Load

A phase-controlled rectifier operated at a firing angle of 30º with *RC* load on the dc side is considered as a non-linear load in this case. Fig. 3.12(a)-(d) shows the simulated waveforms, individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5}), harmonic spectra of load and source currents respectively with method–1 carrier rotation technique, while Fig. 3.13(a)-(d) shows these results for method–2 carrier rotation technique. From Fig. 3.12 and Fig. 3.13 it is observed that the points 1, 2, and 4 of subsection 3.4.1.1 are equally valid for this case also. Apart from these, the following observations are also made:

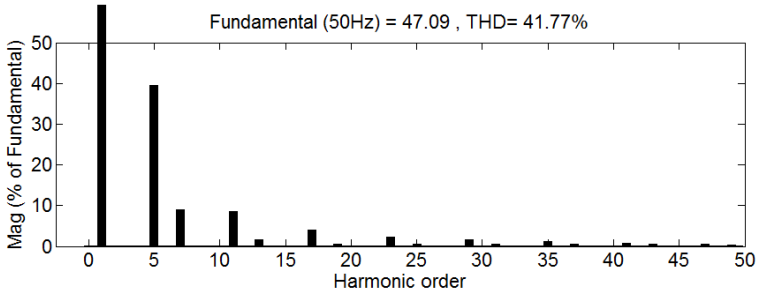
1. After compensation with D-STATCOM, the THD of the load current is 41.77%, but the source current THD is reduced to 3.26% and 3.03% with method–1 and method–2 carrier rotation techniques respectively.
2. After compensation with D-STATCOM, the source power factor is improved from 0.837 (lagging) to 0.999 (lagging) in both carrier rotation techniques.
3. The rms value of load current is 36.10 A, and that of source current is 32.19 A in method–1 and 32.63 A in method–2 carrier rotation technique. The reduction in the source current is due to the compensation of load reactive power following the same procedure described in point 3 of the previous subsection.
4. With method–1 carrier rotation technique, the maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 71 V but with method–2, it is reduced to 35 V.
5. At 0.16 sec., load current increases from 36.10 A to 51.34 A and decreased back to its original value at 0.26 sec. The corresponding change in the compensated source current is observed to be very smooth in both cases.
6. It is also observed that with method–2 carrier rotation technique, the steady-state in capacitor voltages are achieved only in 1–2 cycle, compared with 2–3 cycles with method–1 carrier rotation technique.
7. The power factor and the displacement factor on the source side are unity not only in the steady-state condition but also in the transient condition.



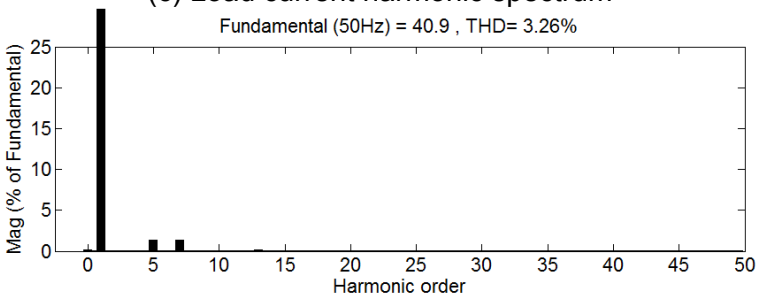
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})

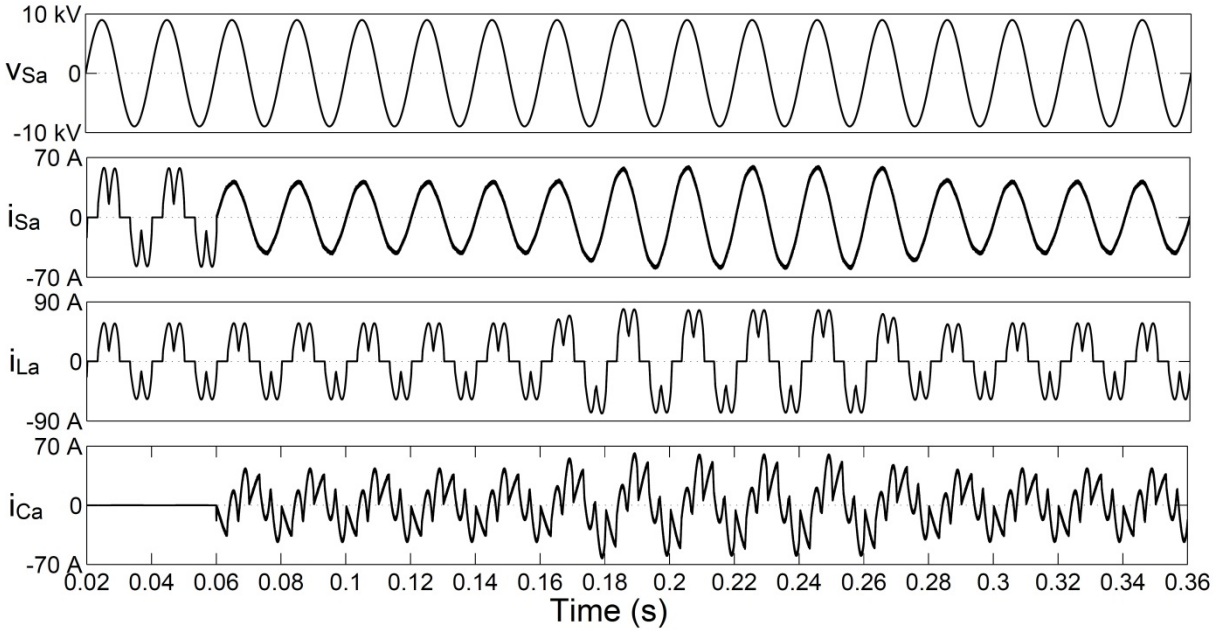


(c) Load current harmonic spectrum

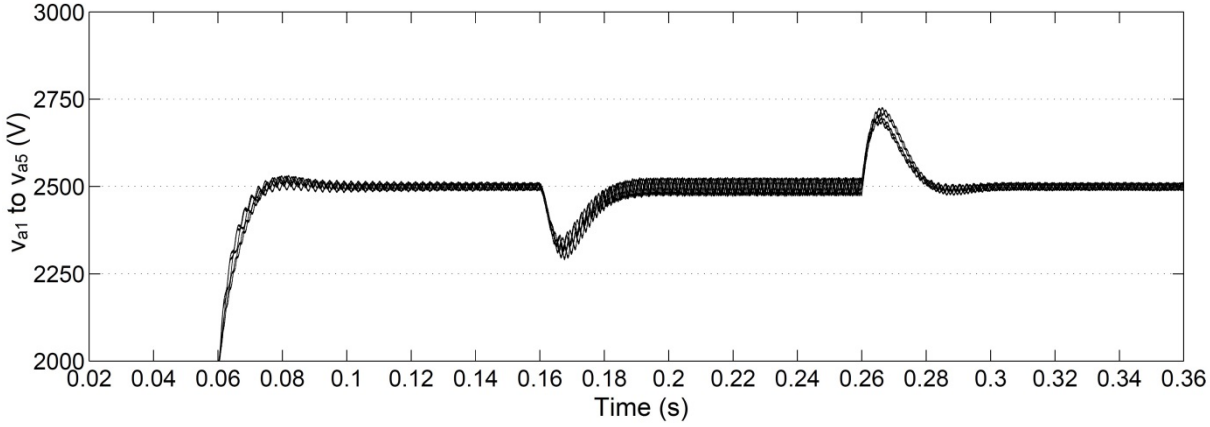


(d) Source current harmonic spectrum

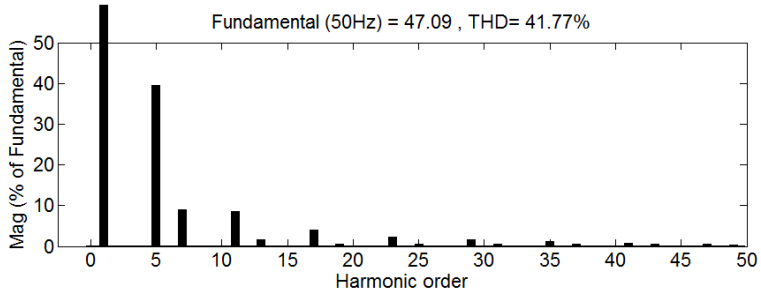
Fig. 3.12: Performance of D-STATCOM for *RC* load on the dc side of a phase controlled rectifier operated at a firing angle of 30º with method–1 carrier rotation technique with an ideal voltage source.



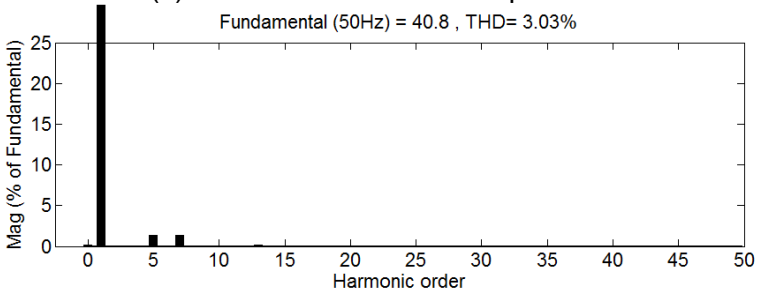
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})



(c) Load current harmonic spectrum



(d) Source current harmonic spectrum

Fig. 3.13: Performance of D-STATCOM for *RC* load on the dc side of a phase controlled rectifier operated at a firing angle of 30º with method–2 carrier rotation technique with an ideal voltage source.

3.4.2 Simulation Results with Distorted Utility Voltage Conditions

The waveforms of the utility voltages are frequently distorted due to the widespread use of the non-linear loads in the distribution power system. The control scheme used in the D-STATCOM is capable of maintaining the source current balanced and sinusoidal in spite of the imperfections in the mains voltage. In order to verify the efficacy of controller in compensating source currents under distorted voltage conditions, harmonics are introduced to the source voltage. Fig. 3.14 shows the harmonic spectrum of the distorted source voltage considered for this simulation study. The source voltage contains 5% 3rd order and 10% 5th order harmonic components and the resultant THD is 11.18%.

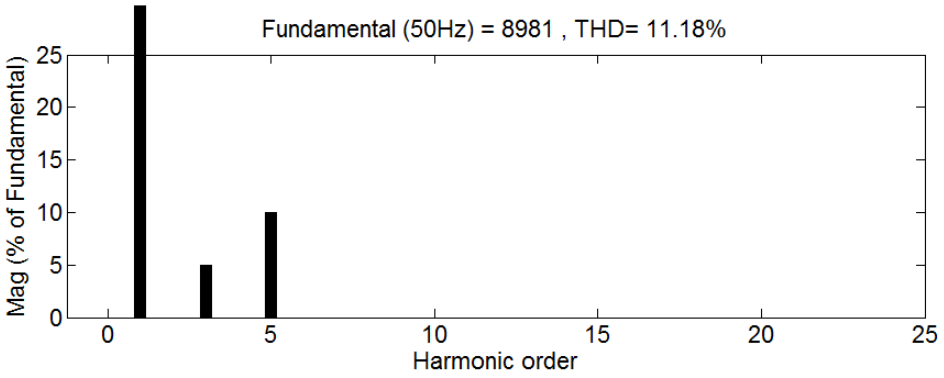


Fig. 3.14: Harmonic spectrum of distorted source voltage

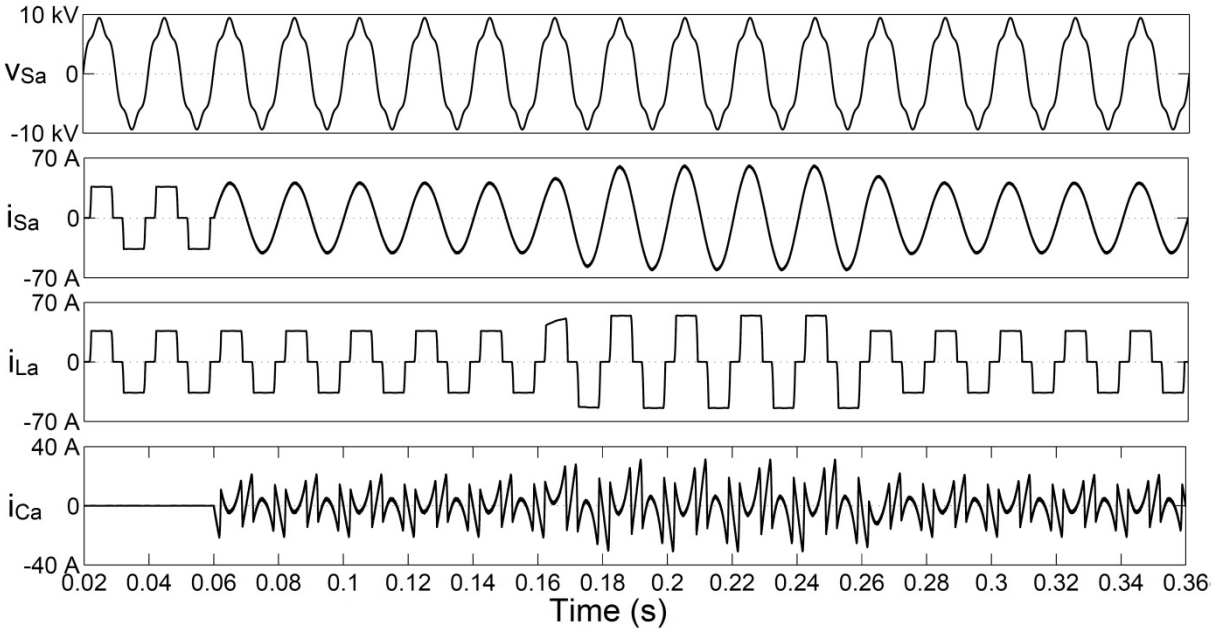
Simulation results under distorted utility voltage conditions with uncontrolled and phase-controlled rectifiers having *RL* and *RC* loads on their dc sides are presented and discussed below. In these simulation studies also the dc capacitors are precharged to 80% of their reference voltage, i.e. 2000 V.

3.4.2.1 Uncontrolled Rectifier with *RL* Load

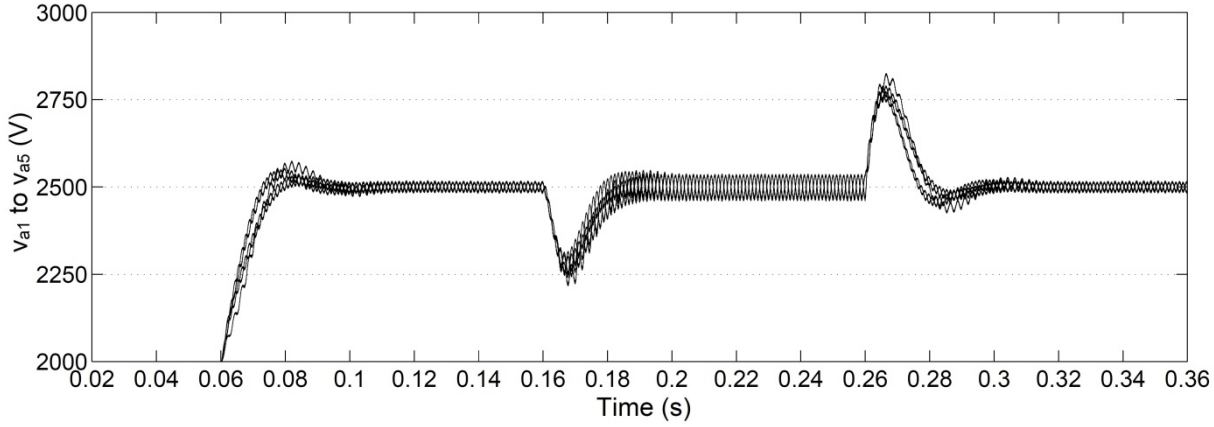
An uncontrolled rectifier with *RL* load on the dc side is considered as a non-linear load in this case. Fig. 3.15(a)-(d) shows the simulated waveforms, individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5}), harmonic spectra of load and source currents respectively with method–1 carrier rotation technique, while Fig. 3.16(a)-(d) shows these results for method–2 carrier rotation technique. From Fig. 3.15 and Fig. 3.16 following observations are made:

1. In both cases, at the instant the D-STATCOM is switched-on, the source current becomes sinusoidal from a stepped wave shape.
2. In both cases, steady-state is reached for all the dc capacitors of the H-bridge cells within 1–2 cycles with the smooth build-up of the capacitor voltages.
3. After compensation with D-STATCOM, the THD of the load current is 27.39%, but the source current THD is reduced to 1.31% and 1.25% with method–1 and method–2 carrier rotation techniques respectively, which are well within the limits of IEEE–519–1992 recommended value of 5%.

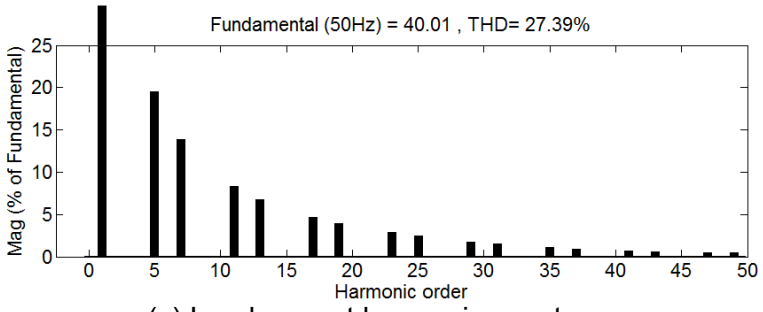
4. After compensation with D-STATCOM, the source current is in phase with the source voltage and confirms the compensation of reactive power. The power factor and displacement factor of the source are almost unity in both carrier rotation techniques (0.999 lagging).
5. The rms value of load current is 29.33 A, and that of source current is 30.01 A in method–1 and 30.12 A in method–2 carrier rotation technique. The enhancement in the source currents is due to the compensation of real power losses of the inverter. The reason for the lower value of peak-to-peak ripple in dc voltage with method–2 is already explained in point no. 6 of subsection 3.4.1.1.
6. In both cases, the capacitor voltage of individual H-bridge cell is well regulated at its reference value. This ensures the effectiveness of the dc voltage controller with the distorted utility voltage condition also. However, with method–1 carrier rotation technique, the maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 70 V but with method–2, it is reduced to 33 V.
7. At 0.16 sec., load current increases from 29.33 A to 44.95 A and decreased back to its original value at 0.26 sec. The corresponding change in the compensated source current is observed to be very smooth in both cases. The power factor and the displacement factor on the source side are unity not only in the steady-state condition but also in the transient condition.
8. At the instant when load current changes, the dc capacitor voltage changes from its reference value to compensate for the enhancement in the load current. This causes drop in capacitor voltage which is subsequently restored in 1–2 cycles. Similarly, drop in load current is responded by D-STATCOM with enhancement in capacitor voltage with subsequent quick restoration (in 1–2 cycles) to its reference value. The regulation of the capacitor voltages is ensured by the dc voltage regulator. A smooth control of the dc voltages in both carrier rotation techniques ensures the effectiveness of the dc voltage controller in transient condition with the distorted utility voltage condition.



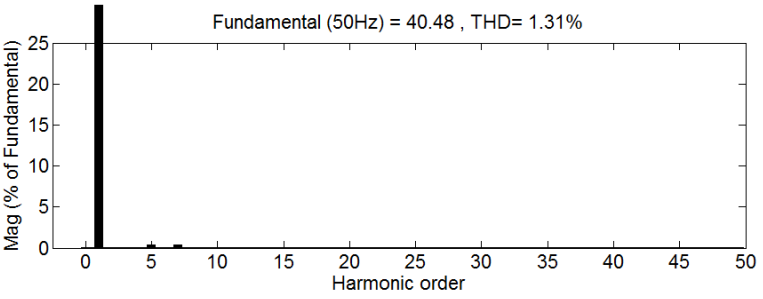
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})

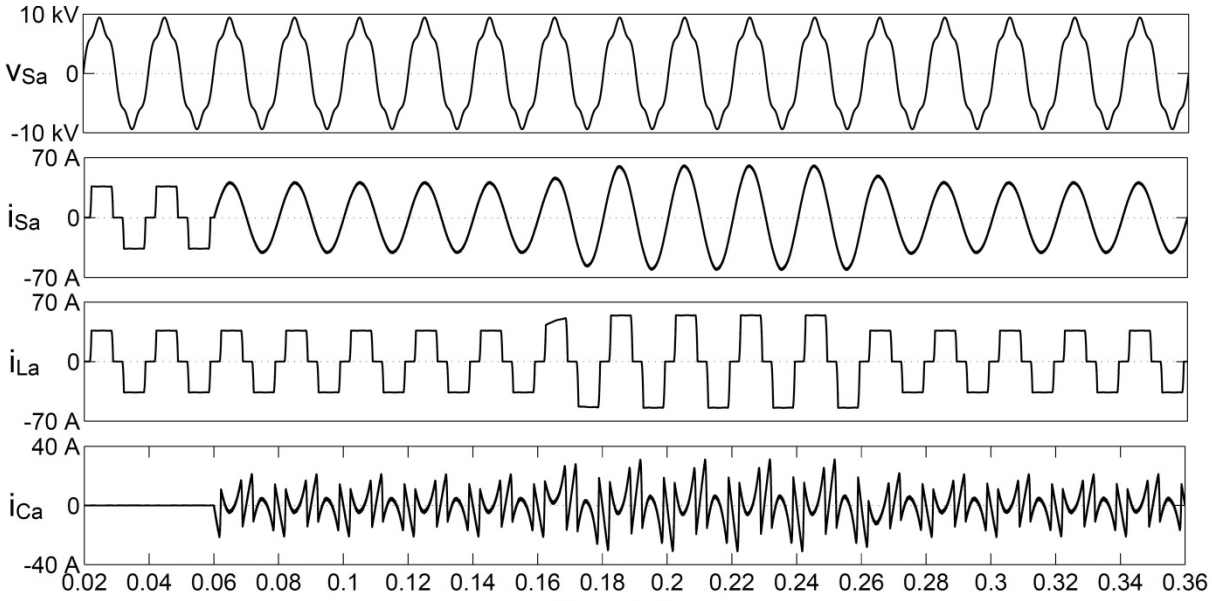


(c) Load current harmonic spectrum

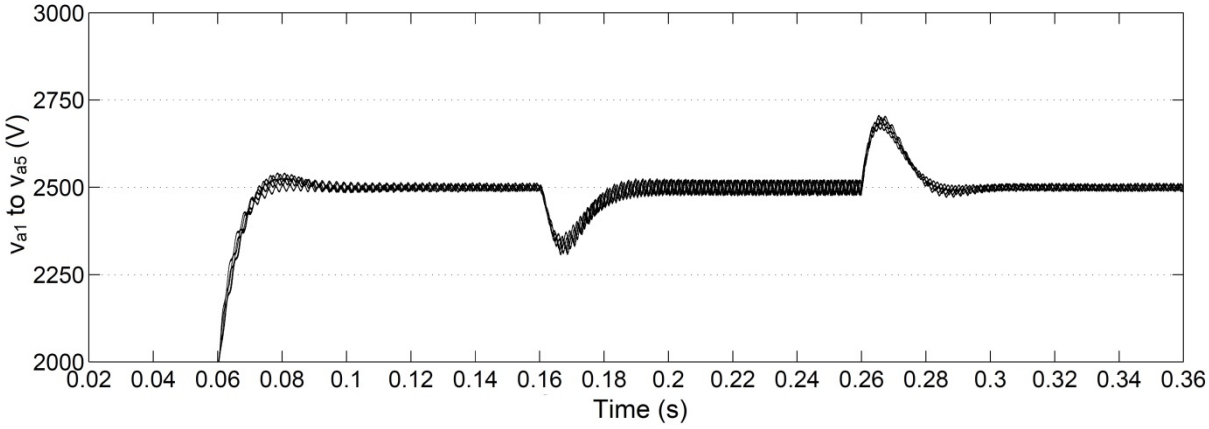


(d) Source current harmonic spectrum

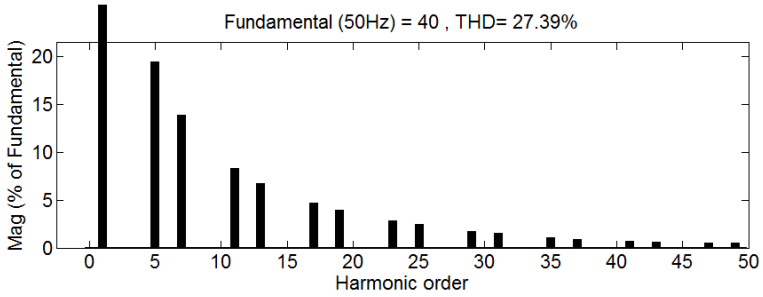
Fig. 3.15: Performance of D-STATCOM for *RL* load on the dc side of an uncontrolled rectifier with method–1 carrier rotation technique with distorted source voltage.



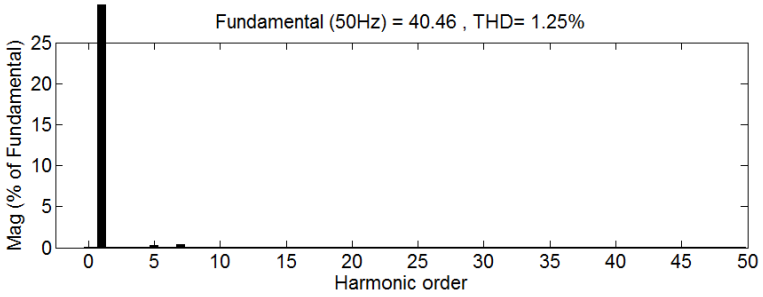
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})



(c) Load current harmonic spectrum



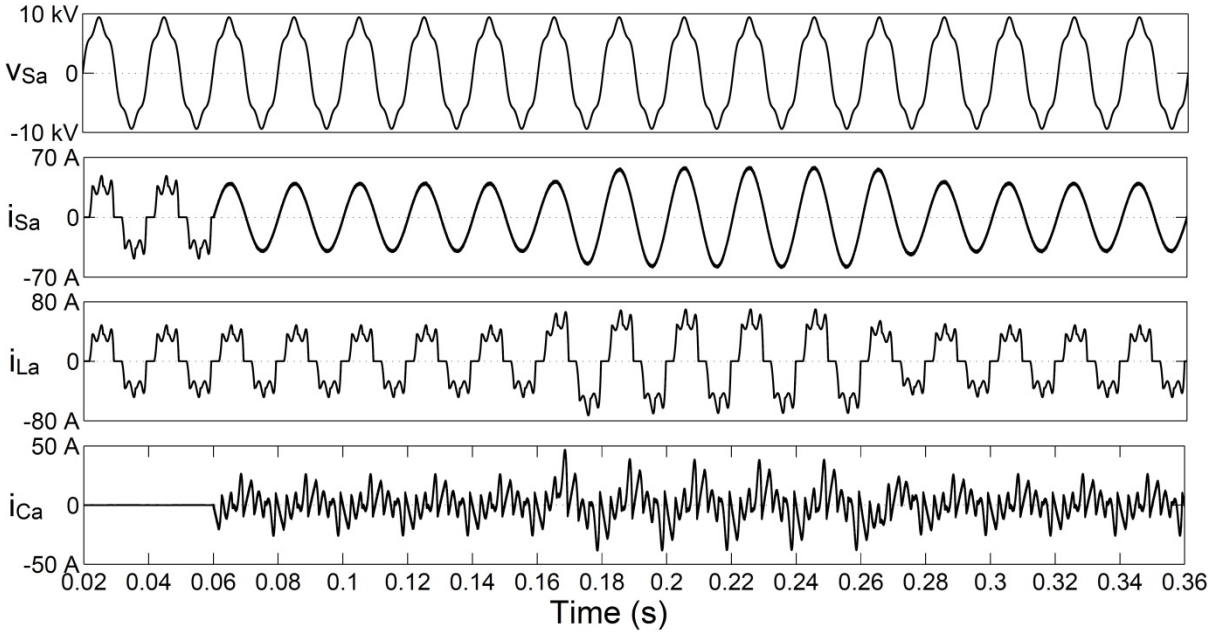
(d) Source current harmonic spectrum

Fig. 3.16: Performance of D-STATCOM for *RL* load on the dc side of an uncontrolled rectifier with method–2 carrier rotation technique with distorted source voltage.

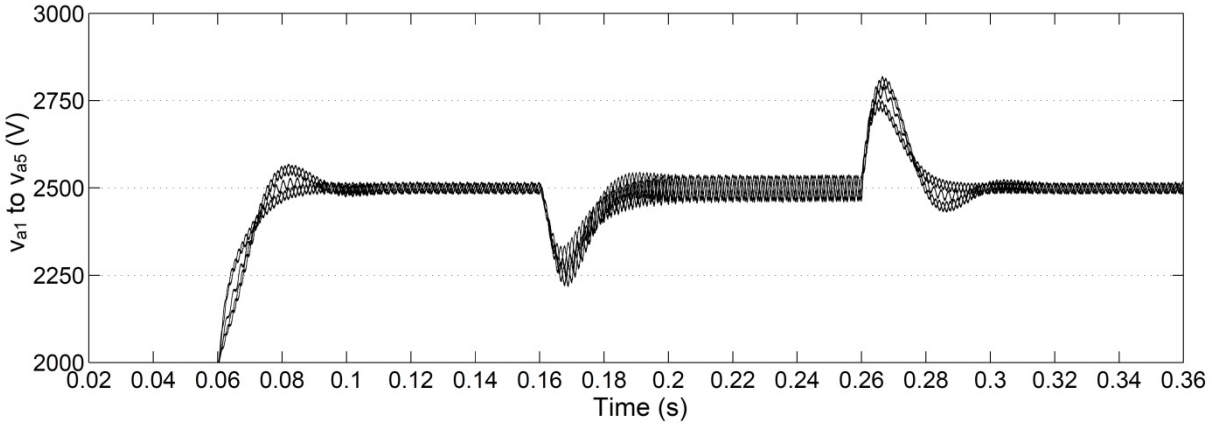
3.4.2.2 Uncontrolled Rectifier with *RC* Load

An uncontrolled rectifier with *RC* load on the dc side is considered as a non-linear load in this case. Fig. 3.17(a)-(d) shows the simulated waveforms, individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5}), harmonic spectra of load and source currents respectively with method–1 carrier rotation technique, while Fig. 3.18(a)-(d) shows these results for method–2 carrier rotation technique. From Fig. 3.17 and Fig. 3.18 following observations are made:

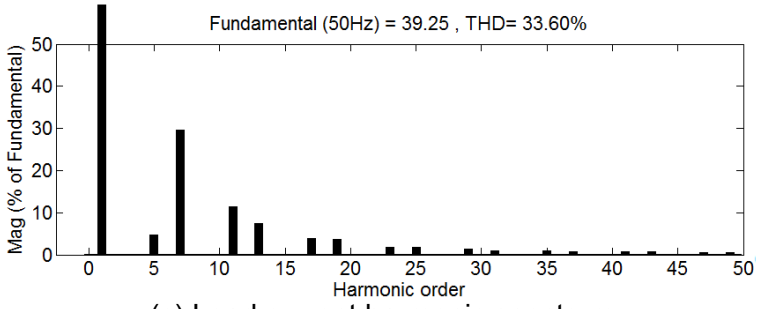
1. After compensation with D-STATCOM, the THD of the load current is 33.60%, but the source current THD is reduced to 1.80% and 1.68% with method–1 and method–2 carrier rotation techniques respectively.
2. The rms value of load current is 28.98 A, and that of source current is 29.67 A in method–1 and 29.89 A in method–2 carrier rotation technique. The enhancement in the source currents is due to the compensation of real power losses of the inverter.
3. With method–1 carrier rotation technique, the maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 69 V but with method–2, it is reduced to 34 V.
4. At 0.16 sec., load current increases from 28.98 A to 42.92 A and decreased back to its original value at 0.26 sec. The corresponding change in the compensated source current is observed to be very smooth in both cases.
5. In method–2 carrier rotation technique, the steady-state in capacitor voltages are achieved in 1–2 cycle compared to 2–3 cycles in method–1 carrier rotation technique, which ensures the fast dynamic response of method–2 carrier rotation technique.
6. Apart from the above observations, the same behaviour of the system described in points 1, 2 and 4 of the previous subsection is also seen in this case.



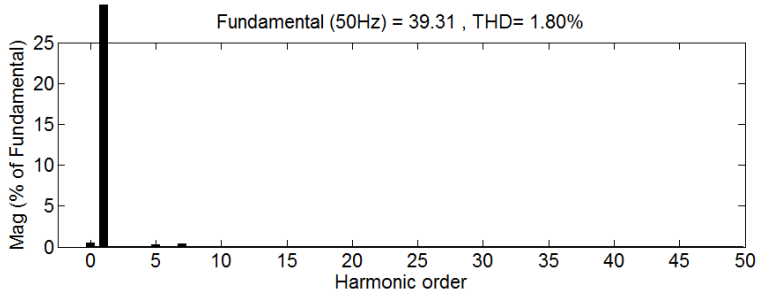
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})

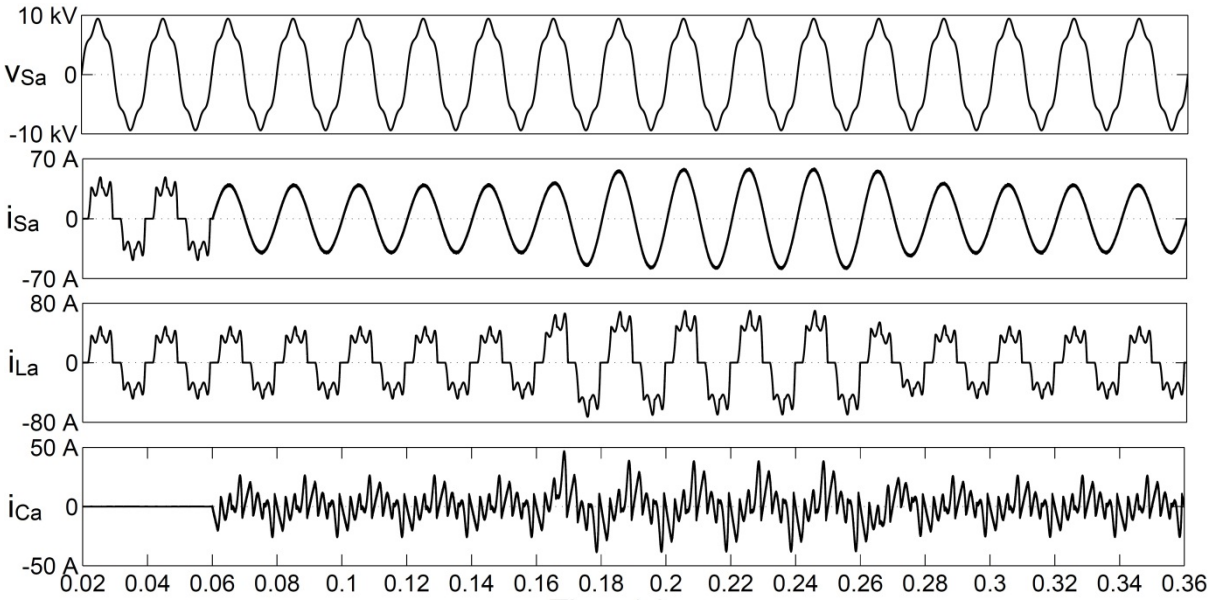


(c) Load current harmonic spectrum

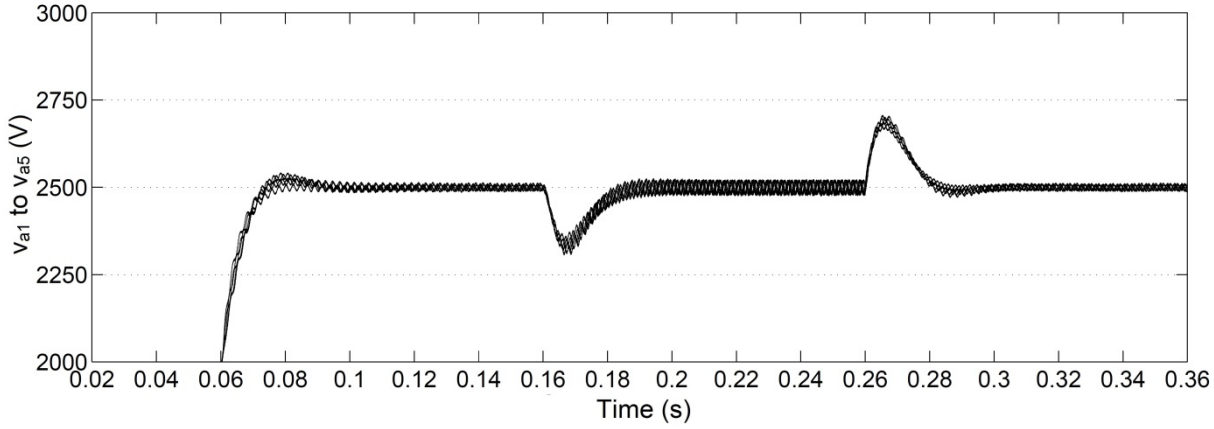


(d) Source current harmonic spectrum

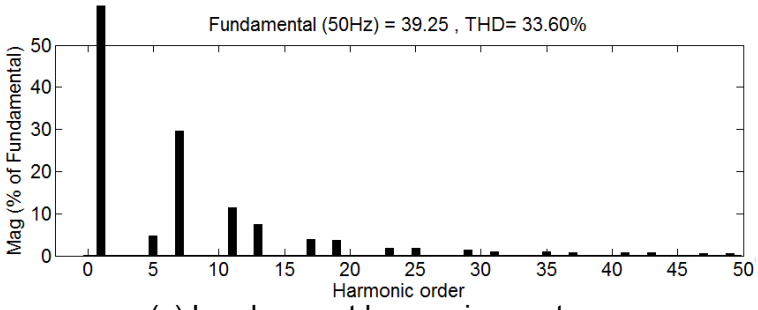
Fig. 3.17: Performance of D-STATCOM for *RC* load on the dc side of an uncontrolled rectifier with method–1 carrier rotation technique with distorted source voltage.



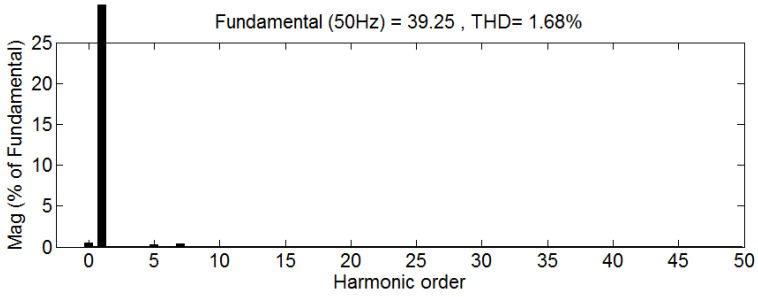
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})



(c) Load current harmonic spectrum



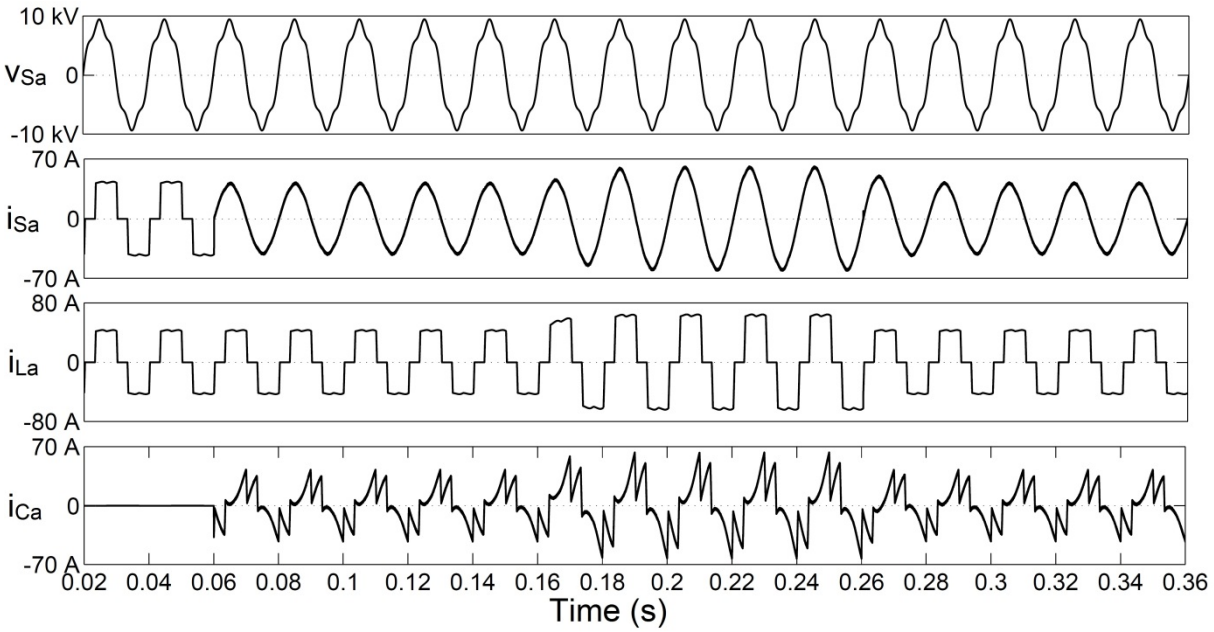
(d) Source current harmonic spectrum

Fig. 3.18: Performance of D-STATCOM for *RC* load on the dc side of an uncontrolled rectifier with method–2 carrier rotation technique with distorted source voltage.

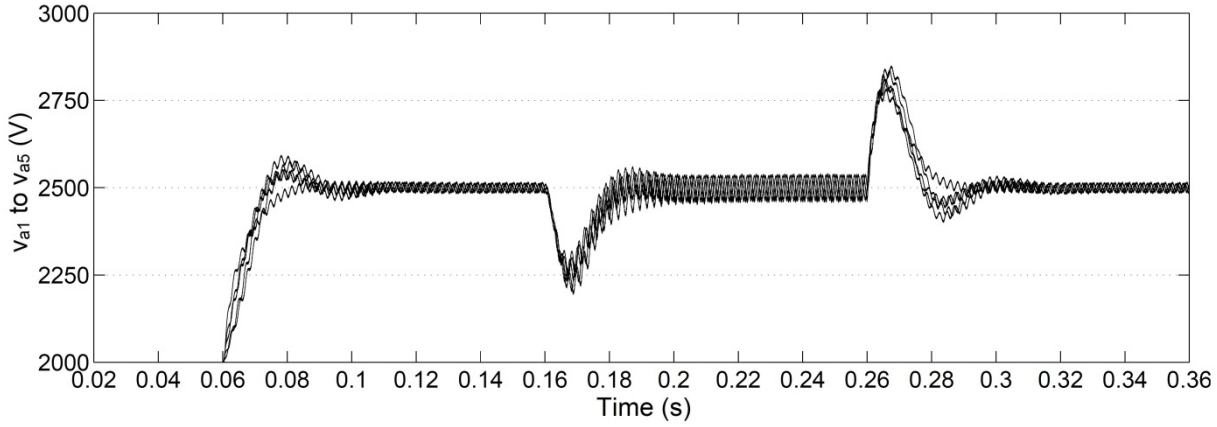
3.4.2.3 Phase-controlled Rectifier with *RL* Load

A phase-controlled rectifier operated at a firing angle of 30º with *RL* load on the dc side is considered as a non-linear load in this case. Fig. 3.19(a)-(d) shows the simulated waveforms, individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5}), harmonic spectra of load and source currents respectively with method–1 carrier rotation technique, while Fig. 3.20(a)-(d) shows these results for method–2 carrier rotation technique. From Fig. 3.19 and Fig. 3.20 following observations are made:

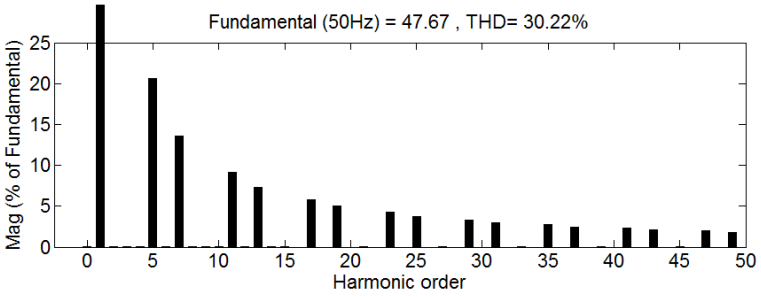
1. After compensation with D-STATCOM, the THD of the load current is 30.22%, but the source current THD is reduced to 2.15% and 2.05% with method–1 and method–2 carrier rotation techniques respectively.
2. After compensation with D-STATCOM, the source power factor is improved from 0.841 (lagging) to almost unity in both carrier rotation techniques.
3. The rms value of load current is 34.61 A, and that of source current is 32.14 A in method–1 and 32.32 A in method–2 carrier rotation technique. The reduction in the source current is due to the compensation of load reactive power following the same procedure described in point 3 of subsection 3.4.1.3.
4. With method–1 carrier rotation technique, the maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 75 V but with method–2, it is reduced to 38 V.
5. At 0.16 sec., load current increases from 34.61 A to 51.14 A and decreased back to its original value at 0.26 sec. The corresponding change in the compensated source current is observed to be very smooth in both cases.
6. In method–2 carrier rotation technique, the steady-state in capacitor voltages are achieved in 1–2 cycle compared to 2–3 cycles in method–1 carrier rotation technique.
7. The power factor and the displacement factor on the source side are unity not only in the steady-state condition but also in the transient condition. Also the observations of points 1, 2, and 4 of subsection 3.4.2.1 are also equally valid for this case.



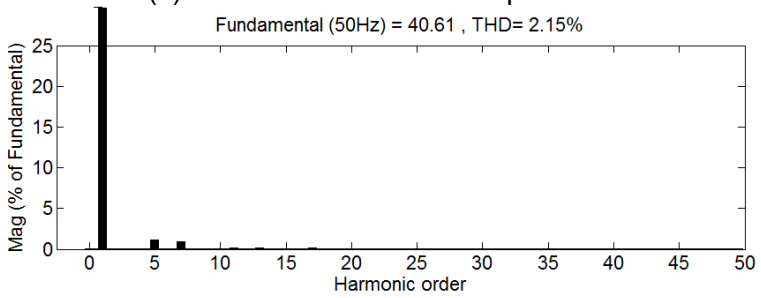
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})

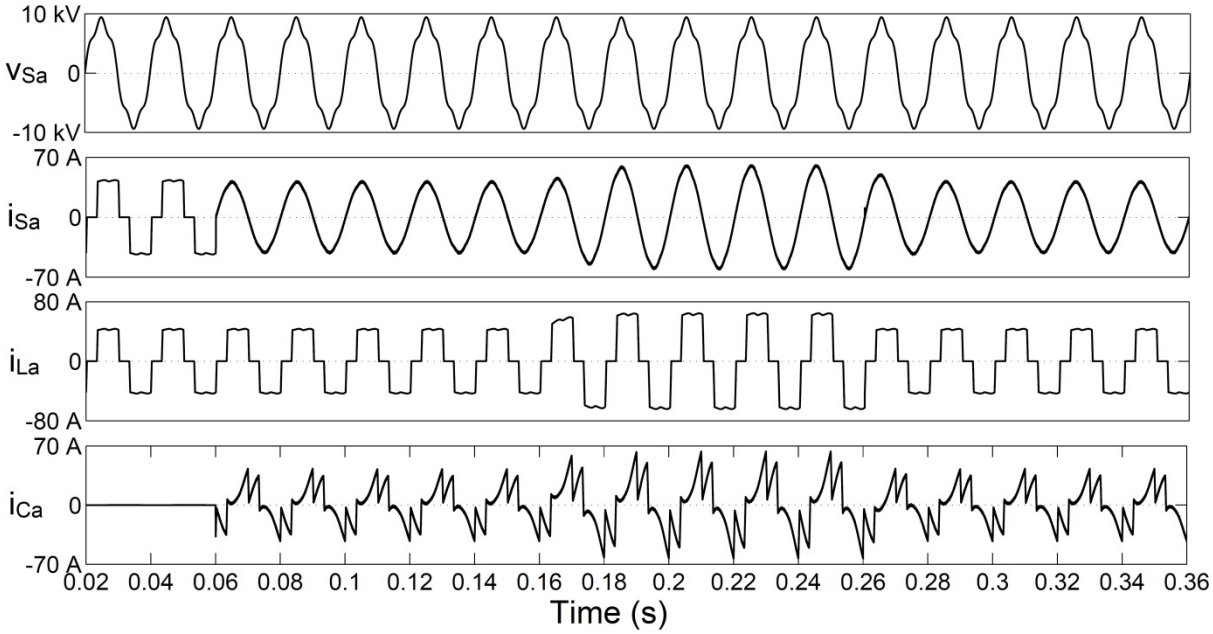


(c) Load current harmonic spectrum

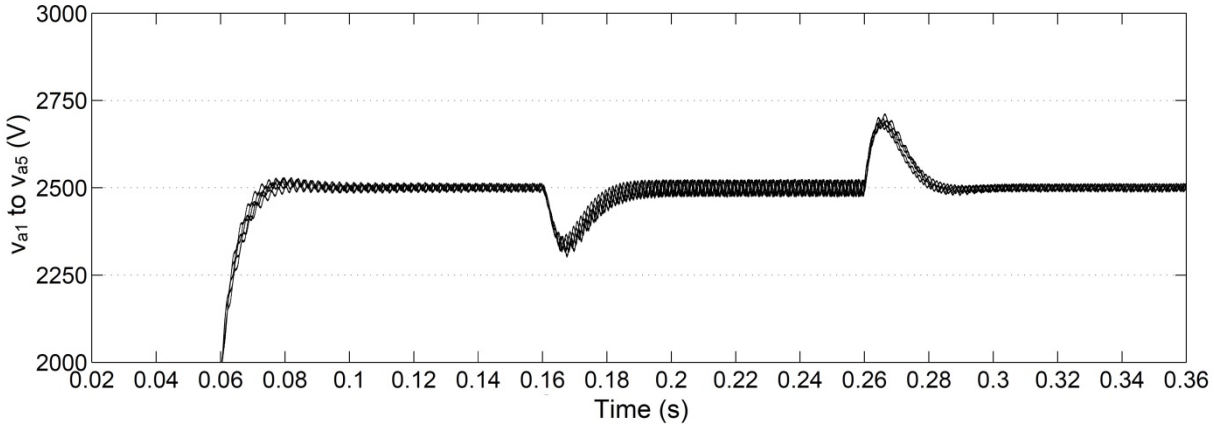


(d) Source current harmonic spectrum

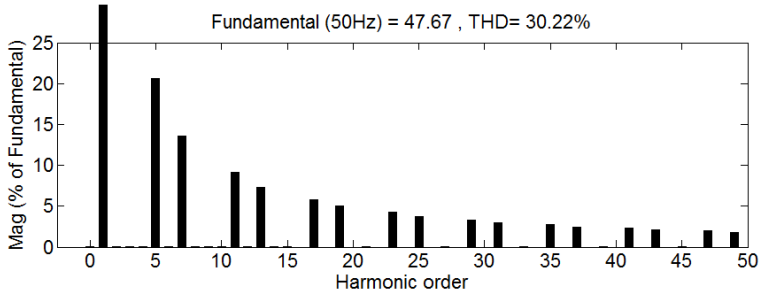
Fig. 3.19: Performance of D-STATCOM for *RL* load on the dc side of a phase controlled rectifier operated at a firing angle of 30º with method–1 carrier rotation technique with distorted source voltage.



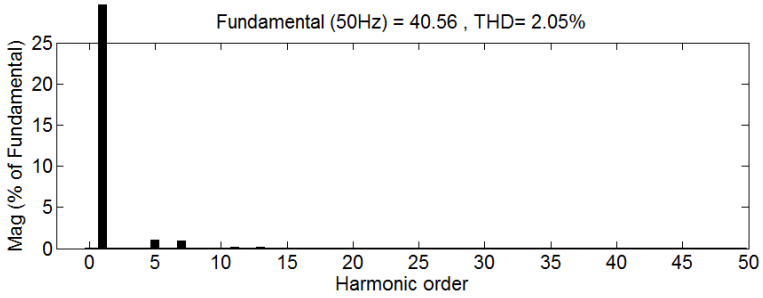
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})



(c) Load current harmonic spectrum



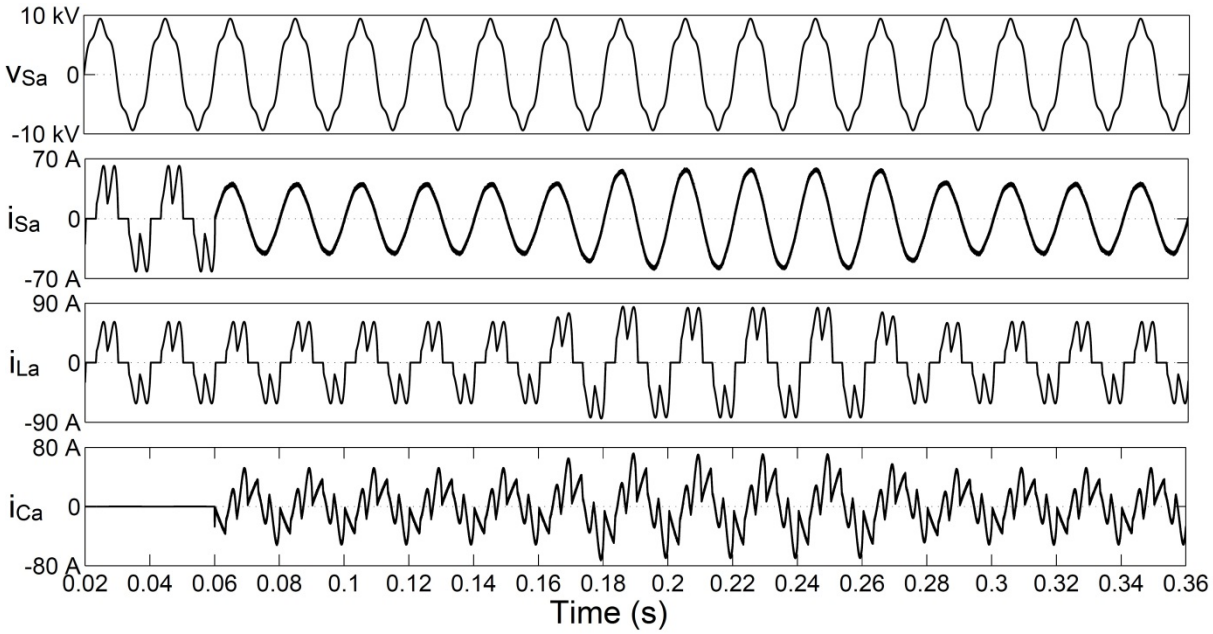
(d) Source current harmonic spectrum

Fig. 3.20: Performance of D-STATCOM for *RL* load on the dc side of a phase controlled rectifier operated at a firing angle of 30º with method–2 carrier rotation technique with distorted source voltage.

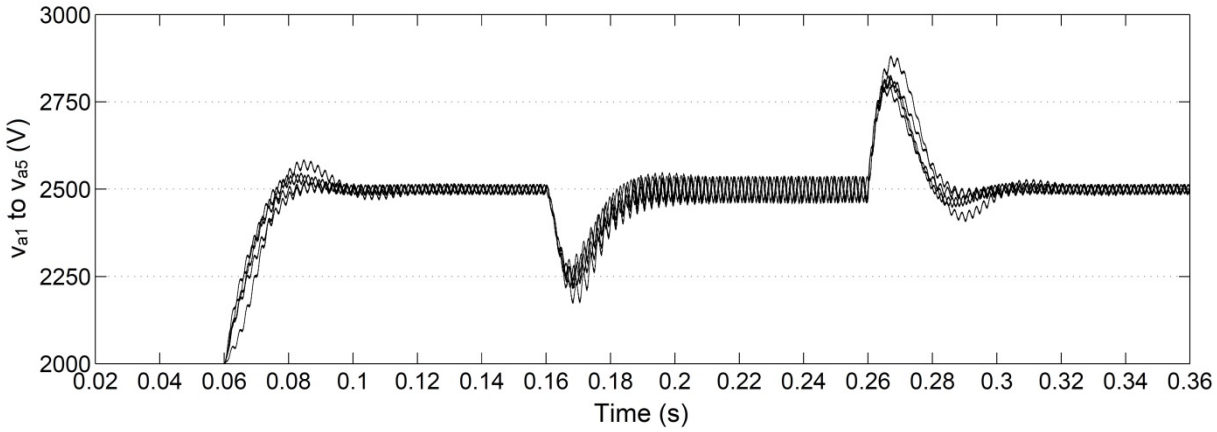
3.4.2.4 Phase-controlled Rectifier with *RC* Load

A phase-controlled rectifier operated at a firing angle of 30º with *RC* load on the dc side is considered as a non-linear load in this case. Fig. 3.21(a)-(d) shows the simulated waveforms, individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5}), harmonic spectra of load and source currents respectively with method–1 carrier rotation technique, while Fig. 3.22(a)-(d) shows these results for method–2 carrier rotation technique. From Fig. 3.21 and Fig. 3.22 following observations are made:

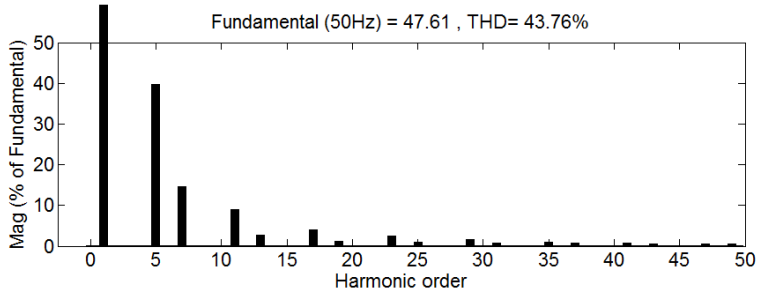
1. After compensation with D-STATCOM, the THD of the load current is 43.76%, but the source current THD is reduced to 3.07% and 2.75% with method–1 and method–2 carrier rotation techniques respectively.
2. After compensation with D-STATCOM, the source power factor is improved from 0.831 (lagging) to almost unity in both carrier rotation techniques.
3. The rms value of load current is 36.78 A, and that of source current is 32.45 A in method–1 and 32.11 A in method–2 carrier rotation technique. The reduction in the source current is due to the compensation of load reactive power following the same procedure described in point 3 of subsection 3.4.1.3.
4. With method–1 carrier rotation technique, the maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 78 V but with method–2, it is reduced to 40 V.
5. At 0.16 sec., load current increases from 36.78 A to 52.34 A and decreased back to its original value at 0.26 sec. The corresponding change in the compensated source current is observed to be very smooth in both cases.
6. It is also observed that with method–2 carrier rotation technique, the steady-state in capacitor voltages are achieved only in 1–2 cycle, compared with 2–3 cycles with method–1 carrier rotation technique.
7. The power factor and the displacement factor on the source side are unity not only in the steady-state condition but also in the transient condition. Further, the observations of points 1, 2, and 4 of subsection 3.4.2.1 are also valid for this case.



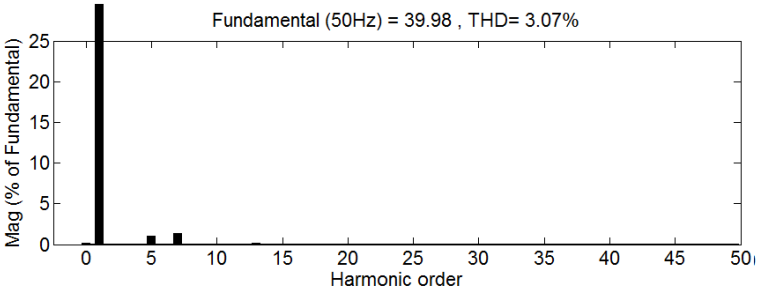
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})

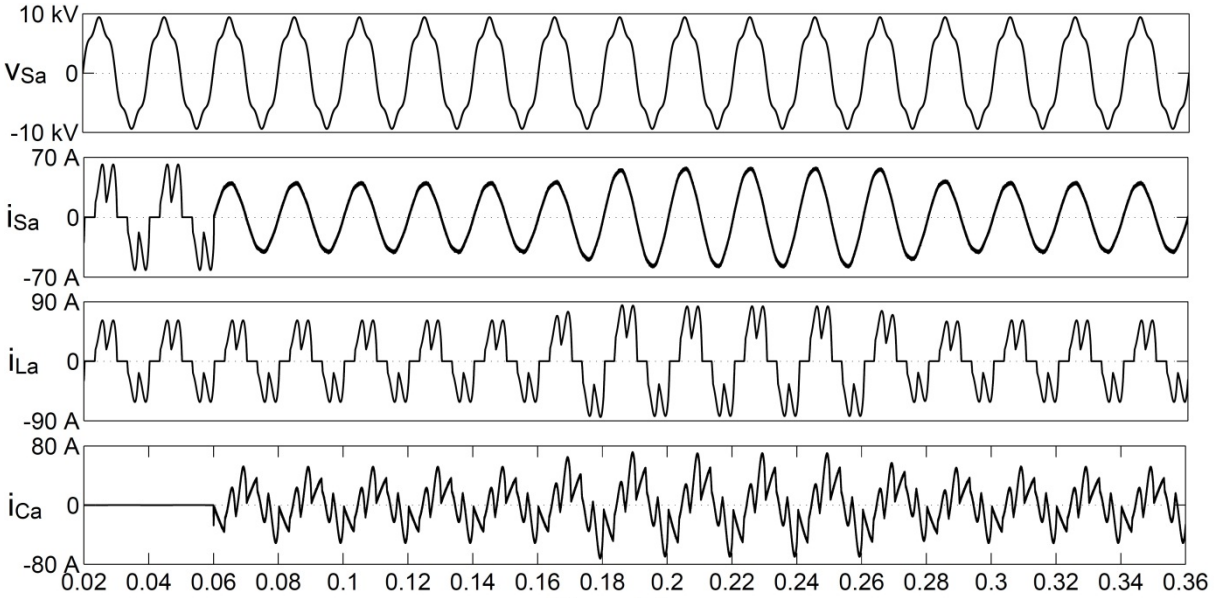


(c) Load current harmonic spectrum

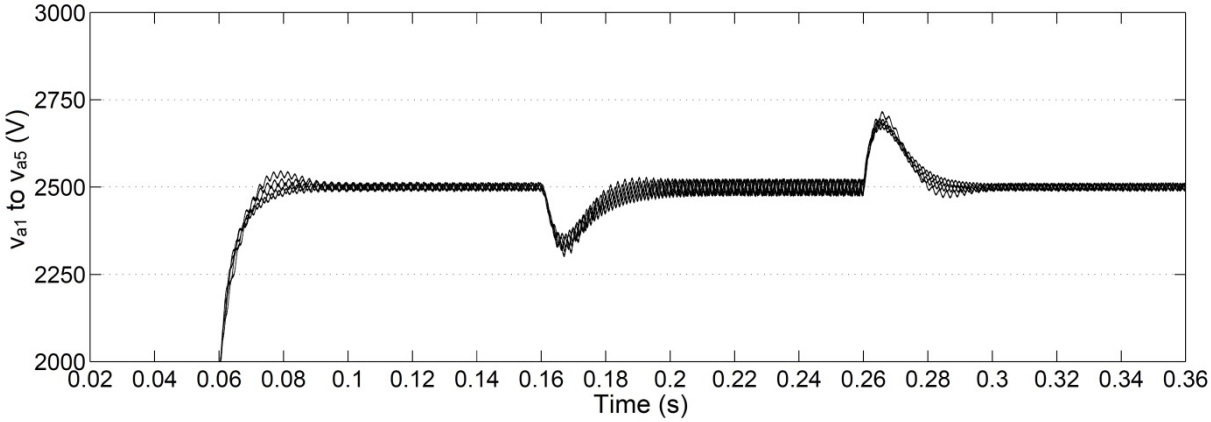


(d) Source current harmonic spectrum

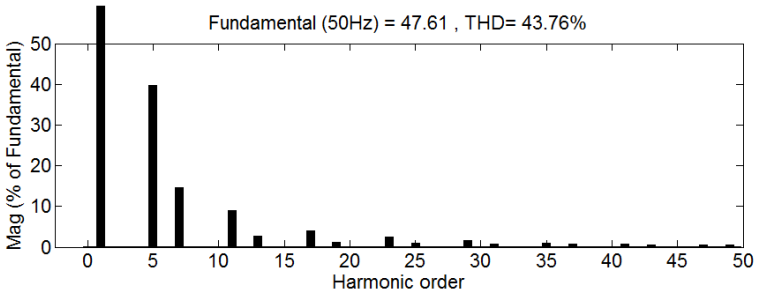
Fig. 3.21: Performance of D-STATCOM for *RC* load on the dc side of a phase controlled rectifier operated at a firing angle of 30º with method–1 carrier rotation technique with distorted source voltage.



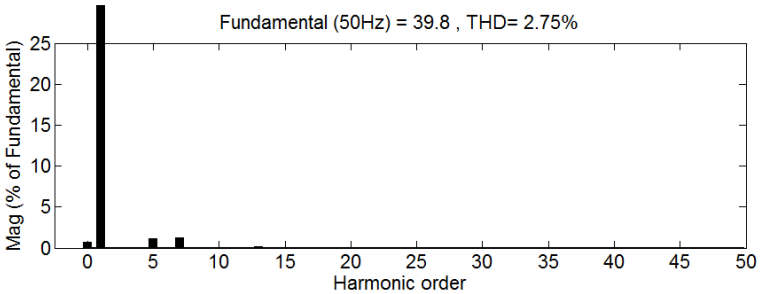
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} to v_{a5})



(c) Load current harmonic spectrum



(d) Source current harmonic spectrum

Fig. 3.22: Performance of D-STATCOM for *RC* load on the dc side of a phase controlled rectifier operated at a firing angle of 30º with method–2 carrier rotation technique with distorted source voltage.

3.5 Comparison of Carrier Rotation Techniques

Table 3.5 and Table 3.6 summarises the comparison of the adopted carrier rotation techniques for controlling the inverter of D-STATCOM with different reactive/non-linear loads under ideal and distorted voltage conditions respectively.

Table 3.5: Comparison of carrier rotation techniques with different reactive/non-linear loads under ideal voltage conditions.

Parameter	Method–1 carrier rotation				Method–2 carrier rotation			
Reactive/non-linear load	Diode bridge with *RL*	Diode bridge with *RC*	Thyristor bridge with *RL*	Thyristor bridge with *RC*	Diode bridge with *RL*	Diode bridge with *RC*	Thyristor bridge with *RL*	Thyristor bridge with *RC*
%THD of load current	28.34	35.28	30.25	41.77	28.34	35.28	30.25	41.77
%THD of source current after compensation	1.53	2.15	1.85	3.26	1.27	2.00	1.73	3.03
Source power factor before compensation	0.997	0.995	0.843	0.837	0.997	0.995	0.843	0.837
Source power factor after compensation	1.0	1.0	1.0	0.999	1.0	1.0	1.0	0.999
Load current (A)	30.06	30.17	33.95	36.10	30.06	30.17	33.95	36.10
Source current after compensation (A)	30.78	30.92	30.03	32.19	30.81	30.86	30.16	32.63
Maximum peak-to-peak ripple in dc voltage of individual H-bridge cells (V)	68	65	69	71	31	30	33	35

From both tables it can be concluded that the method–2 carrier rotation technique has relatively superior compensating characteristics when compared with method–1 carrier rotation technique. It can be further observed that with method–2 carrier rotation technique, the peak-to-peak ripple in dc voltage of individual H-bridge cells (V) is reduced and ensures an excellent balance of capacitor voltages.

Table 3.6: Comparison of carrier rotation techniques with different reactive/non-linear loads under distorted voltage conditions.

Parameter	Method–1 carrier rotation				Method–2 carrier rotation			
Reactive/non-linear load	Diode bridge with *RL*	Diode bridge with *RC*	Thyristor bridge with *RL*	Thyristor bridge with *RC*	Diode bridge with *RL*	Diode bridge with *RC*	Thyristor bridge with *RL*	Thyristor bridge with *RC*
%THD of load current	27.39	33.06	30.22	43.76	27.39	33.06	30.22	43.76
%THD of source current after compensation	1.31	1.80	2.15	3.07	1.25	1.68	2.05	2.75
Source power factor before compensation	0.996	0.995	0.841	0.831	0.996	0.995	0.841	0.831
Source power factor after compensation	1.0	1.0	1.0	0.999	1.0	1.0	0.999	0.999
Load current (A)	29.33	28.98	34.61	36.78	29.33	28.98	34.61	36.78
Source current after compensation (A)	30.01	29.67	31.14	32.45	30.12	29.89	31.32	32.11
Maximum peak-to-peak ripple in dc voltage of individual H-bridge cells (V)	70	69	75	78	33	34	38	40

3.6 Conclusion

In this chapter, an 11 kV, 1 MVA, 11-level SSBC based transformerless PWM D-STATCOM, intended for installation on an 11 kV industrial distribution system is investigated. As the D-STATCOM is directly connected to the distribution systems, the bulky, heavy and costly line-frequency transformer can be eliminated from the design of D-STATCOM. The control algorithm presented to control the D-STATCOM is not only able to compensate the reactive power and harmonics generated by the load, but also keeps the dc voltages of H-bridges cells controlled and balanced in steady-state and transient conditions. The carrier rotation based PWM techniques are adopted to control the inverter of the D-STATCOM. Simulation results are presented to investigate the performance of the D-STATCOM in ideal and distorted voltage conditions with both carrier rotation techniques. The simulation results are presented for both steady-state and transient conditions with different loads. After compensation with D-STATCOM the %THDs of source currents are reduced to below 5% and the power factor and the displacement factor on the source side are unity not only in the steady-state condition but also in the transient condition. Further, a smooth control of the dc voltages of H-bridge cells in steady-state and transient conditions ensures the effectiveness of the carrier rotation techniques and dc voltage controller.

CHAPTER 4: D-STATCOM FOR THREE-PHASE, FOUR-WIRE SYSTEMS

In this chapter, two reduced rating hybrid 3P4W D-STATCOMs are proposed for the simultaneous compensation of reactive power, source neutral current and the phase harmonic currents. The complete arrangements considered in these topologies comprise of a 3P3W D-STATCOM, a T-connected transformer or a zigzag-delta transformer and a single-phase APF. These hybrid approaches significantly reduce the rating of the overall compensator and improves the performance under non-ideal utility voltage conditions. To show the efficacy of the compensators, extensive simulation studies are presented.

4.1 Introduction

The present day three-phase, four-wire (3P4W) distribution systems are suffering from load reactive power as well as power quality problems such as current and voltage harmonics, unbalance in the load and excessive neutral current which have been widely reported in the literature [13-15, 17-19]. Poor power quality gives rise to an increase in power system losses, protection system malfunctions, risk of resonance phenomenon and harmonic voltage drops across the line impedances, which lead to erroneous operation of the loads and electronic equipment connected to the utility.

In recent years, a number of schemes have been reported for solving the power quality problems in 3P4W systems [74-77]. In [76, 77], three single-phase inverters have been used to filter the source current harmonics and neutral current. This approach reduces the dc voltage requirement of the inverter but it requires more number of switching devices [76, 78]. In [74, 75], two filtering schemes, namely; a) four-leg and b) capacitor midpoint topologies have been proposed for simultaneous filtering of source current harmonics and neutral current. However, these filtering schemes require large volt-ampere (VA) rating of the inverter [74, 75]. Moreover, capacitor midpoint topology suffers from unequal capacitor voltages and four-leg topology requires extra switching devices [76].

The application of different transformers such as zigzag [45-53], star-delta [54], T-connected [55], Scott- connected [56] and star/hexagon-connected [57] have been used to attenuate the neutral current on the utility sides in recent years due to the advantages such as low cost, high reliability and simplified circuit connection. The comparison of the neutral current compensation methods in 3P4W systems with different transformer configurations are given in Table 4.1 [56]. In Table 4.1, the VA rating of the transformer is primarily decided by the amount of the neutral current and it is calculated by the product of the rms values of the voltage and current associated with each of its windings. It is observed from Table 4.1 that, zigzag transformer approach requires least VA rating and three single-phase transformers with a turns ratio of 1:1. The T-connected transformer requires only two single-phase transformers and also its rating is nearly equal to that of the zigzag transformer while being far less than those of other transformer based topologies [56]. Hence, zigzag and T-connected transformer based topologies are considered in the present work for the

compensation of neutral current. The operating principle of a zigzag transformer for the compensation of neutral current is discussed in the next section and the same principle is applicable for T-connected transformer based topology also.

Table 4.1: Comparison of different transformers for neutral current compensation in 3P4W systems.

Transformer type	Zigzag [45-53]	Star-delta [54]	Star-hexagon [57]	T-connected [55]
Number of transformers required to build	3 (single-phase two-winding)	1 (three-phase two-winding)	3 (single-phase three-winding)	2 (single-phase three-winding and single-phase two-winding)
Winding voltages	$\frac{V_{LL}}{3} : \frac{V_{LL}}{3}$	$\frac{V_{LL}}{\sqrt{3}} : \frac{V_{LL}}{\sqrt{3}}$	$\frac{V_{LL}}{\sqrt{3}} : \frac{V_{LL}}{\sqrt{3}} : \frac{V_{LL}}{\sqrt{3}}$	$\frac{V_{LL}}{\sqrt{3}} : \frac{V_{LL}}{2\sqrt{3}} : \frac{V_{LL}}{2\sqrt{3}}$ and $\frac{V_{LL}}{2} : \frac{V_{LL}}{2}$
Primary winding current	$\frac{I_n}{3}$	$\frac{I_n}{3}$	$\frac{I_n}{3}$	$\frac{I_n}{3}$
Transformer rating	$\frac{V_{LL}I_n}{3} = 0.333V_{LL}I_n$	$\frac{V_{LL}I_n}{\sqrt{3}} = 0.577V_{LL}I_n$	$\frac{V_{LL}I_n}{\sqrt{3}} = 0.577V_{LL}I_n$	$\left(\frac{1}{3\sqrt{3}} + \frac{1}{6}\right)V_{LL}I_n = 0.359V_{LL}I_n$
Standard transformer?	No	Yes	No	No
Space requirement	Low	High	Highest	Lowest

Where V_{LL} = line-to-line voltage and I_n = neutral current.

4.2 Zigzag Transformer for Neutral Current Compensation

The zigzag transformer has been used in the past for creating a neutral point, thereby converting a 3P3W distribution system to a 3P4W system. But, in this work, the zigzag transformer is used to reduce the neutral current in 3P4W system [45]. The schematic diagram of the basic topology is illustrated in Fig. 4.1.

In Fig. 4.1, the zigzag transformer is connected in parallel to the unbalanced load. A zigzag transformer consists of three single-phase transformers with the turn ratio of 1:1. Therefore, the input currents flowing into the primary windings is equal to the output currents flowing out from the secondary windings. Hence, the three-phase currents flowing into three transformers must be equal. Thus, ideally the zigzag transformer can be regarded as open-circuit for the positive-sequence and the negative-sequence currents. Therefore, the current flowing through the zigzag transformer is only the zero-sequence component. But in practice the impedance offered to the zero-sequence currents is a function of the zero-sequence impedances of the utility system, zigzag transformer and the neutral conductor. As these impedances are very small, in most practical cases, a large amount of zero-sequence current

will circulate between the zigzag transformer and the load. To reduce the neutral current of the utility side furthermore, it has been proposed to insert an inductor (L_b) in the neutral conductor of the utility side in order to split the current into two paths, one to the distribution transformer and the other to the zigzag transformer [45].

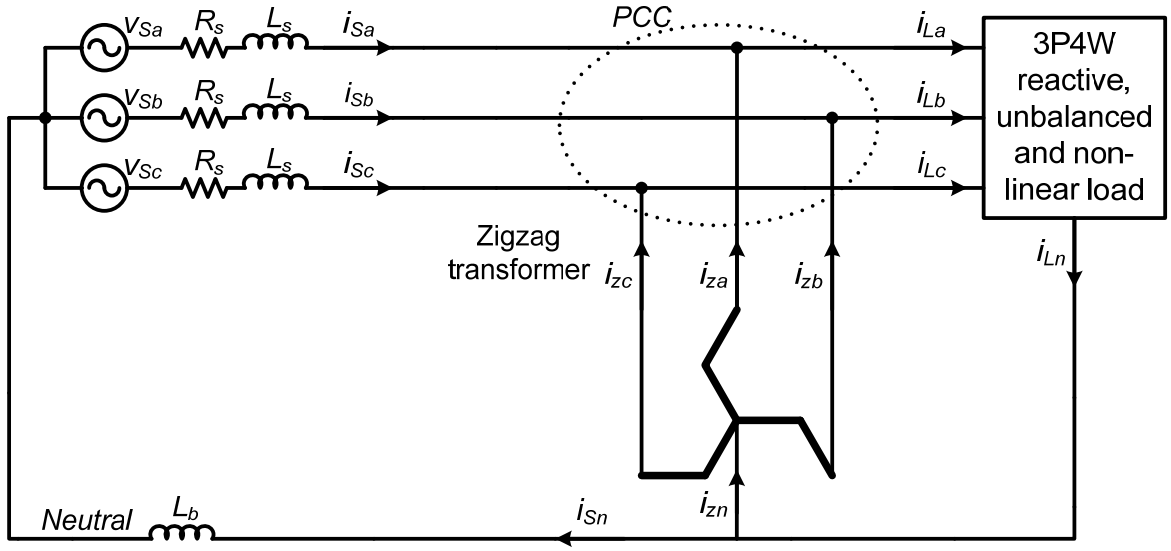


Fig. 4.1: The system configuration of three-phase four-wire distribution power system with zigzag transformer.

The zigzag transformer has been used to attenuate the neutral current and zero-sequence harmonic currents on the utility side in recent years due to the advantages of low cost, high reliability and simplified circuit connection. However, in case of an unbalanced and/or distorted source voltage, the performance of the zigzag transformer deteriorates. In order to understand the performance of the zigzag transformer with unbalanced and/or distorted source voltage conditions, the following analysis is carried out. The same analysis is also applicable for the T-connected transformer based topology.

Let v_{Sa}, v_{Sb} and v_{Sc} be the three-phase unbalanced and/or distorted source voltages and i_{La}, i_{Lb} and i_{Lc} be the three-phase load phase currents. The zero-sequence source voltage (v_{S0}) and zero-sequence load current (i_{L0}) are given as:

$$v_{S0} = \frac{1}{3}\left(v_{Sa} + v_{Sb} + v_{Sc}\right) \tag{4.1}$$

$$i_{L0} = \frac{1}{3}\left(i_{La} + i_{Lb} + i_{Lc}\right) \tag{4.2}$$

The current flowing through the zigzag transformer is only the zero-sequence component, and Fig. 4.2 shows the zero-sequence equivalent circuit of Fig. 4.1.

The different symbols used in Fig. 4.2, where,

Z_S source impedance,

Z_{Ln} impedance of the neutral conductor between the load and the zigzag transformer,

Z_{zn} impedance of the zigzag transformer,

Z_n=Z_{Sn}+Z_b, Z_n impedance between the utility and the zigzag transformer, Z_{Sn} impedance of the neutral conductor and Z_b impedance of the inserted buffer inductor L_b.

The effects of the v_{S0} and i_{L0} to the neutral current of the utility side after using the zigzag transformer can be analysed by using the superposition theorem.

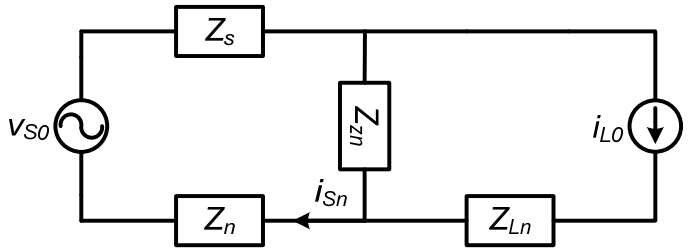


Fig. 4.2: The zero-sequence equivalent circuit.

For considering the effect of the i_{L0} only, the v_{S0} should be short-circuited and the equivalent circuit is shown in Fig. 4.3(a). Then, the utility side neutral current i'_{Sn} caused by i_{L0} can be expressed as,

$$i'_{Sn} = \frac{Z_{zn}}{(Z_S + Z_n) + Z_{zn}} i_{L0} \tag{4.3}$$

Equation (4.3) indicates that the magnitude of the utility side neutral current caused by i_{L0} will be reduced after applying the zigzag transformer. If Z_{zn} is reduced or Z_n is increased, i'_{Sn} in the utility side can be further attenuated.

Similarly, for considering the effect of the v_{S0} only, the i_{L0} should be open-circuited and the equivalent circuit is shown in Fig. 4.3(b). From Fig. 4.3, it can be found that the Zig-Zag transformer supplies a low impedance path for the zero-sequence voltage v_{S0}. Then, the utility side neutral current i''_{Sn} caused by v_{S0} can be expressed as,

$$i''_{Sn} = \frac{1}{Z_S + Z_{zn} + Z_n} v_{S0} \tag{4.4}$$

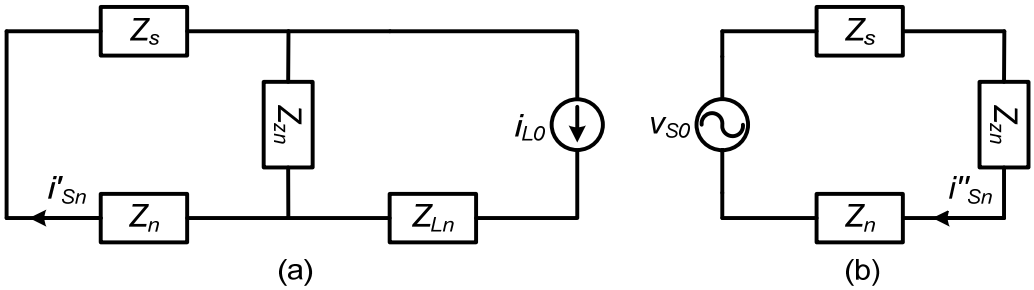


Fig. 4.3: The zero-sequence equivalent circuits (a) when considering zero-sequence load current; (b) when considering zero-sequence source voltage.

Equation (4.4) shows that due to the existence of zero-sequence supply voltage, the zigzag transformer provides a path for the zero-sequence current flowing between the utility and the zigzag transformer. However, the impedance of the utility system, the zigzag

transformer and the neutral conductor are very small in most of the 3P4W distribution systems. This implies that a significant neutral current will be generated after applying the zigzag transformer under the condition of unbalanced utility voltages.

The total source neutral current due to v_{S0} and i_{L0} is given as,

$$i_{Sn} = \frac{Z_{zn}}{(Z_S + Z_n) + Z_{zn}} i_{L0} + \frac{1}{Z_S + Z_{zn} + Z_n} v_{S0} \tag{4.5}$$

From equation (4.5) it can be found that the zigzag transformer can be used to reduce the zero-sequence current of the source, but it will also induce a significant zero-sequence current when the utility voltages contain zero sequence components. This excess neutral current may result in the burn-down of the zigzag transformer, the neutral conductor and the distribution power transformer [46].

From the above analysis it can be observed that, the transformer based topologies can reduce the source neutral current to a great extent but their compensation characteristics are dependent on their locations, the impedances of the transformers and utility voltage conditions [46].

To alleviate this problem, a reduced rating hybrid topology comprising of a zigzag-delta transformer, a 3P3W APF and a single-phase APF has been demonstrated for the compensation of source neutral current and phase current harmonics [47, 48], but no attempt has been made to improve the displacement power factor. Also, the fundamental-frequency phase currents were not made balanced. Another reduced rating hybrid topology consisting of a single-phase APF and a zigzag transformer for neutral current compensation presented for neutral current compensation [49, 50]. However, in this method, no attempt has been made to improve the displacement power factor and compensate the harmonics of source phase currents. In [51-53], a 3P4W APF comprising of a 3P3W APF and a zigzag transformer for the simultaneous compensation of source current harmonics, reactive power and source neutral current has been proposed, but its compensation characteristics are dependent on its location and source voltage conditions. In [55], a 3P4W APF comprising of a 3P3W APF and a T-connected transformer for 3P4W distribution systems has been proposed, but its compensation characteristics are also dependent on its location and source voltage conditions.

To address the above limitations, in the present work, two reduced rating hybrid 3P4W D-STATCOMs are proposed. They are:

1. A 3P4W hybrid D-STATCOM comprising of a zigzag-delta transformer, 3P3W D-STATCOM and shunt connected single-phase APF.
2. A 3P4W hybrid D-STATCOM comprising of a T-connected transformer, 3P3W D-STATCOM and shunt connected single-phase APF.

These two schemes are almost identical, except the transformer topology and connection of 3P3W D-STATCOM. In these hybrid schemes, the functional capabilities of the

existing schemes are enhanced to compensate source current harmonics, reactive power and neutral current. For this purpose, a new control scheme is also proposed for generating the compensating currents for the D-STATCOM. Further, these hybrid approaches significantly improve the performance of the D-STATCOM under distorted/unbalanced utility voltage conditions.

4.3 A 3P4W Hybrid D-STATCOM with Zigzag-Delta Transformer, 3P3W D-STATCOM and Shunt Connected Single-phase APF

Fig. 4.4 shows the schematic diagram of the hybrid 3P4W D-STATCOM adopted in the present work [47, 48]. The realization of the zigzag-delta transformer with three single-phase three winding transformers is shown in Fig. 4.5 and the equivalent circuit of the compensator scheme is depicted in Fig. 4.6. As shown in Fig. 4.4, a zigzag-delta transformer is connected across the unbalanced load. The 3P3W D-STATCOM is realised by using a five-level single-star bridge-cell (SSBC) based modular multilevel inverter as shown in Fig. 4.7. The 3P3W D-STATCOM is connected to the delta winding of the transformer and produces the desired three-phase currents for compensation of (a) positive and negative sequence harmonics in source currents and (b) reactive power of the load. The capacitor on the dc side of the three-phase inverter of the D-STATCOM is charged by drawing real power from the distribution grid.

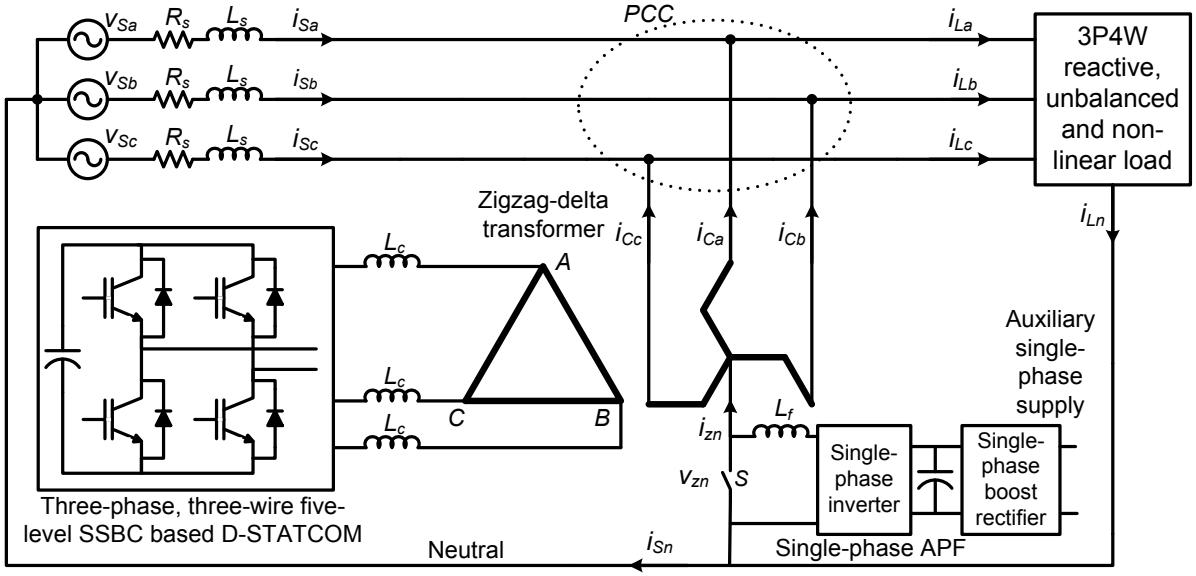


Fig. 4.4: Schematic diagram of a reduced rating hybrid D-STATCOM for 3P4W distribution system using zigzag-delta transformer, 3P3W D-STATCOM and shunt connected single-phase APF.

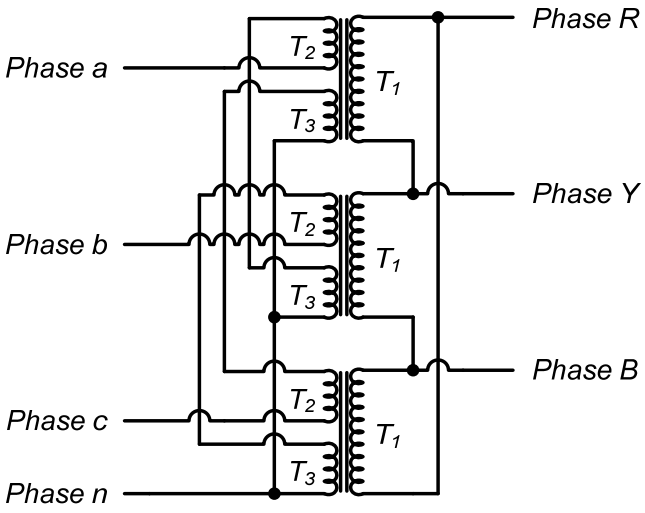


Fig. 4.5: Realization of the zigzag-delta transformer using three single-phase three winding transformers.

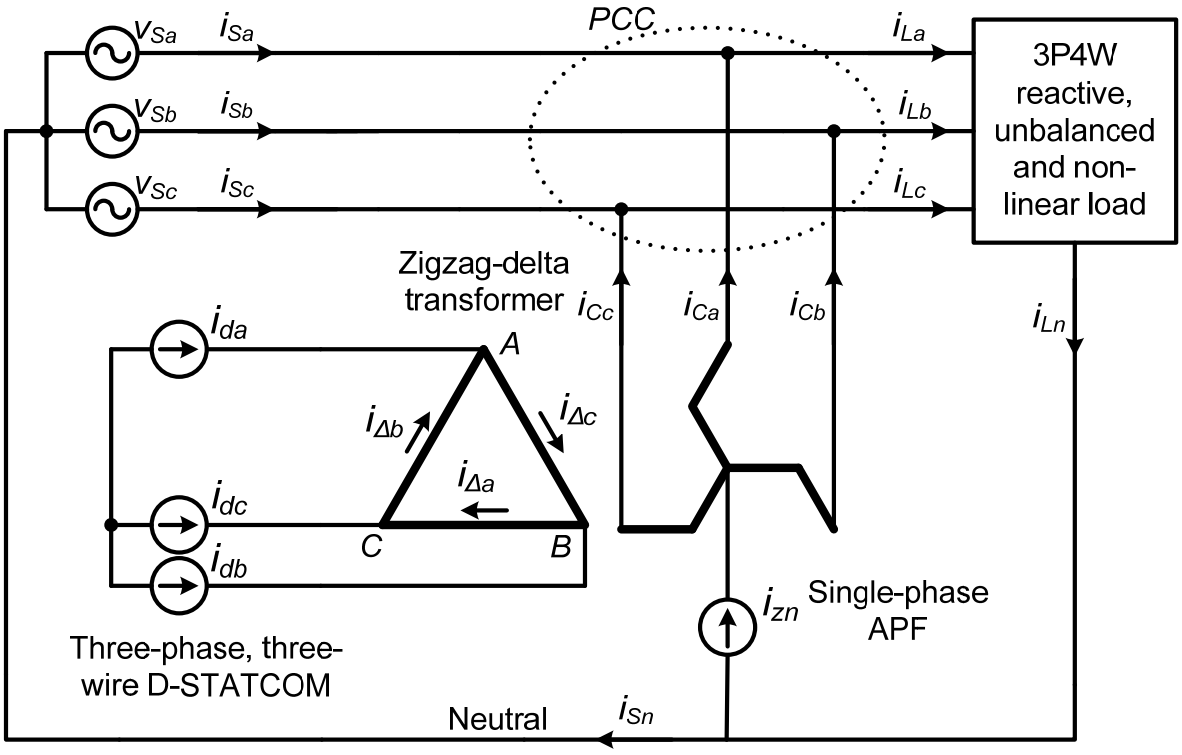


Fig. 4.6: Equivalent circuit of the hybrid 3P4W D-STATCOM.

A single-phase APF is connected between the neutral conductor of the utility and the neutral point of the zigzag transformer. As shown in Fig. 4.8, a single-phase full H-bridge inverter is used as a power circuit for single-phase APF. The single-phase APF produces the desired current for compensating source neutral current and injects the produced current through the neutral of the zigzag transformer. The inverter of the single-phase APF is energized from a separate single-phase boost rectifier of a very low VA rating. The boost rectifier is operated at almost unity power factor and therefore, the input current is sinusoidal. To protect the single-phase APF under abnormal conditions, a switch (*S*) is connected across it.

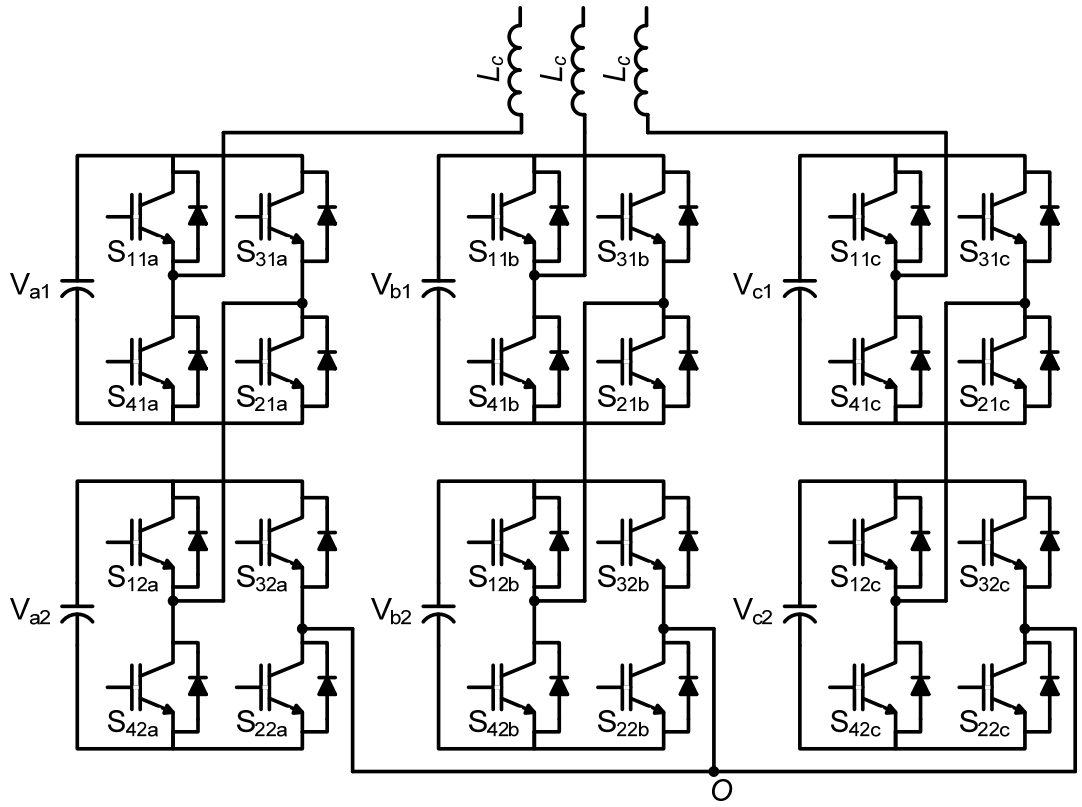


Fig. 4.7: Five-level SSBC based 3P3W D-STATCOM.

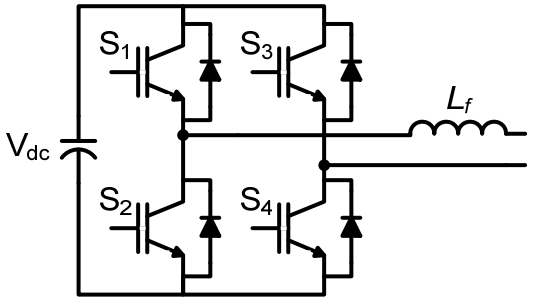


Fig. 4.8: Single-phase full H-bridge based APF.

4.3.1 Operation of the Scheme under Various Utility Voltages

When the switch (*S*) is closed (Fig. 4.4), i.e., the single-phase APF is bypassed, the zigzag transformer provides a low impedance path for the zero-sequence currents to flow between the load and the zigzag transformer. However, the effectiveness of the compensation strongly depends upon the location of the compensator and impedances of the zigzag transformer and the system [45, 46]. The performance of the zigzag transformer also depends upon the utility voltage conditions [46]. Under unbalanced and/or distorted voltage conditions, a zero-sequence voltage may exist which provides a low impedance path for the zero-sequence current to flow between the utility and the zigzag transformer. Therefore, the source neutral current becomes larger than the load neutral current. This implies that a significant amount of neutral current will be generated after applying the zigzag

transformer under unbalanced and/or distorted utility voltages, which will have an adverse effect on the performance of the zigzag transformer [46].

When the switch (*S*) is open, the APF comes into operation and produces the desired current for compensating source neutral current and forcibly injects the current through the neutral of the zigzag transformer. This current split equally and flows through each of the zigzag windings. As the APF forcibly circulates the neutral current to the load via the zigzag transformer, its effectiveness does not depend on the zero-sequence impedance of the zigzag transformer and its location. Hence the special design of the zigzag transformer for low zero-sequence impedance is not necessary.

The rating of the APF is very small due to the low voltage drop across the zigzag transformer neutral and the utility neutral (v_{zn}). This voltage is primarily determined by the sum of the voltage drops across the leakage impedance of the zigzag transformer and filter inductor due to the compensating current of the source neutral. For better compensation under nominal unbalanced and/or distorted conditions, the dc side voltage of the single-phase inverter is kept at three times the peak voltage drop between the zigzag and utility neutrals with ideal utility voltage. However, under sustained unbalanced/distorted utility voltage conditions or fault conditions, v_{zn} can be very high. This makes it necessary to protect the single-phase APF and zigzag transformer by means of a protective device such as metal oxide varistor (MOV).

4.3.2 Control of 3P4W Hybrid D-STATCOM

The control of 3P4W hybrid D-STATCOM involves the independent control of 3P3W D-STATCOM and single-phase APF. The description for each of the controllers is given below.

4.3.2.1 Control of 3P3W D-STATCOM

A five-level SSBC based modular multilevel inverter is used to realise the 3P3W D-STATCOM. The control scheme of 3P3W D-STATCOM involves the calculation of reference compensating currents, dc voltage controller and PWM control of the inverter of the 3P3W D-STATCOM. The block diagram of the controller is shown in Fig. 4.9. The detailed descriptions for each part are given below.

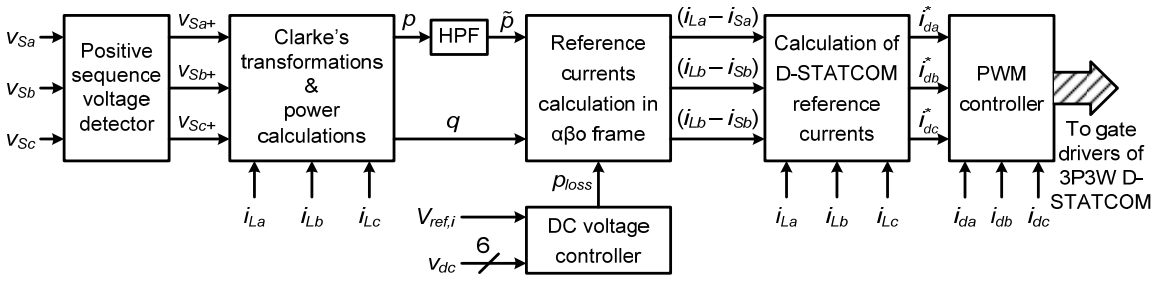


Fig. 4.9: Block diagram of the 3P3W D-STATCOM controller.

(a) *Calculation of 3P3W D-STATCOM Reference Currents*

For calculation of the 3P3W D-STATCOM reference currents, the following assumptions are made:

1. The zigzag-delta transformer consists of three single-phase transformers, each having three windings. The magnetizing currents drawn by the transformers are neglected.
2. The capacitor of the 3P3W D-STATCOM is ideal and does not require any real power from the utility to maintain its dc voltage at the reference value.

In Fig. 4.6, i_{La}, i_{Lb} and i_{Lc} are the load phase currents and i_{Ln} is the load neutral current. Therefore,

$$i_{Ln} = i_{La} + i_{Lb} + i_{Lc} \tag{4.6}$$

Let, $i_{ca,}$ i_{cb} and i_{cc} be the total currents injected into the utility by the zigzag-delta transformer and thus,

$$\begin{aligned} i_{Ca} &= i_{z\Delta a} + i_{za} \\ i_{Cb} &= i_{z\Delta b} + i_{zb} \\ i_{Cc} &= i_{z\Delta c} + i_{zc} \end{aligned} \tag{4.7}$$

Here, $i_{z\Delta a,}$ $i_{z\Delta b}$ and $i_{z\Delta c}$ be the currents injected into the utility through the zigzag-delta transformer due to the operation of the 3P3W D-STATCOM and $i_{za,}$ i_{zb} and i_{zc} are the currents injected into the utility through the zigzag-delta transformer due to the operation of single-phase APF. Under ideal conditions (complete compensation of source neutral current, i.e. i_{Sn} = 0), this current (i.e. from the single-phase APF) splits equally with $i_{Ln}/3$ flowing through each of the zigzag windings. Hence,

$$i_{za} = i_{zb} = i_{zc} = \frac{i_{Ln}}{3} \tag{4.8}$$

Therefore, the equation (4.7) can be rewritten as,

$$\begin{aligned} i_{Ca} &= i_{z\Delta a} + i_{za} = i_{z\Delta a} + \frac{i_{Ln}}{3} \\ i_{Cb} &= i_{z\Delta b} + i_{zb} = i_{z\Delta b} + \frac{i_{Ln}}{3} \\ i_{Cc} &= i_{z\Delta c} + i_{zc} = i_{z\Delta c} + \frac{i_{Ln}}{3} \end{aligned} \tag{4.9}$$

Application of Kirchhoff's current law (KCL) at PCC in Fig. 4.6 gives the following equations:

$$\begin{aligned} i_{Ca} &= i_{La} - i_{Sa} \\ i_{Cb} &= i_{Lb} - i_{Sb} \\ i_{Cc} &= i_{Lc} - i_{Sc} \end{aligned} \tag{4.10}$$

Therefore,

$$
\begin{aligned}
i_{z\Delta a} &= \left(i_{La} - i_{Sa}\right) - \frac{i_{Ln}}{3} \\
i_{z\Delta b} &= \left(i_{Lb} - i_{Sb}\right) - \frac{i_{Ln}}{3} \\
i_{\Delta zc} &= \left(i_{Lc} - i_{Sc}\right) - \frac{i_{Ln}}{3}
\end{aligned}
\tag{4.11}
$$

If the currents $i_{Sa,}$ i_{Sb} and i_{Sc} in equation (4.11) are considered to be fundamental, unity power factor source currents after compensation, then the currents ($i_{La} - i_{Sa}$), ($i_{Lb} - i_{Sb}$) and ($i_{Lc} - i_{Sc}$) represent the sum of load harmonic and reactive currents in phases '*a*', '*b*' and '*c*' respectively.

Now let, N_z = number of turns of each zigzag winding and N_Δ = number of turns of each delta winding. Equating the total ampere-turns acting on each phases of the transformer core in Fig. 4.6, following equations can be written in matrix form as;

$$
\begin{bmatrix} i_{\Delta a} \\ i_{\Delta b} \\ i_{\Delta c} \end{bmatrix} = \frac{N_z}{N_\Delta} \begin{bmatrix} 0 & -1 & 1 \\ 1 & 0 & -1 \\ -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} i_{z\Delta a} \\ i_{z\Delta b} \\ i_{z\Delta c} \end{bmatrix}
\tag{4.12}
$$

The D-STATCOM currents $i_{da,}$ i_{db} and i_{dc} (shown in Fig. 4.6), can be expressed in terms of the delta winding currents by applying KCL at nodes *A, B* and *C* as:

$$
\begin{bmatrix} i_{da} \\ i_{db} \\ i_{dc} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 1 \\ 1 & 0 & -1 \\ -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} i_{\Delta a} \\ i_{\Delta b} \\ i_{\Delta c} \end{bmatrix}
\tag{4.13}
$$

Thus, the required D-STATCOM currents can be calculated from equations (4.11), (4.12) and (4.13) in terms of the measured load harmonic currents as:

$$
\begin{bmatrix} i_{da} \\ i_{db} \\ i_{dc} \end{bmatrix} = \frac{N_z}{N_\Delta} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} (i_{La} - i_{Sa}) - \frac{i_{Ln}}{3} \\ (i_{Lb} - i_{Sb}) - \frac{i_{Ln}}{3} \\ (i_{Lc} - i_{Sc}) - \frac{i_{Ln}}{3} \end{bmatrix}
\tag{4.14}
$$

The load harmonic and reactive currents ($i_{La} - i_{Sa}$), ($i_{Lb} - i_{Sb}$) and ($i_{Lc} - i_{Sc}$) can be calculated by using a suitable current extraction techniques as discussed in 3.2.1. In the present work, IRP theory is used to extract the load harmonic and reactive currents from the load currents. In this method, the load harmonic currents are derived by using the measured voltages at PCC, load currents and the dc bus voltage of SSBC based inverter of 3P3W D-STATCOM. If the supply voltage is unbalanced and/or distorted, then the load harmonic currents derived from IRP theory are not accurate [13, 128]. For proper operation of 3P3W D-STATCOM, the voltages at the PCC are derived from positive-sequence voltage detector method, as given in [13, 128].

Once the load harmonic and reactive currents are calculated, then the next step is to calculate the reference currents for the 3P3W D-STATCOM using equation (4.14). Since the D-STATCOM currents are linear combinations of the measured load harmonic and reactive currents as well as neutral currents, it is quite easy to generate the current references for the 3P3W D-STATCOM.

(b) *DC Voltage Controller*

Fig. 4.10 shows the controller for dc voltage regulation for a 5-level SSBC based D-STATCOM [94, 99, 101, 102, 133]. The dc voltage controller is similar to that given in subsection 3.3.4, except the cascade number (N) is equal to two. In order to tightly control the voltages of the 6 floating dc capacitors, the converter shown in Fig. 4.10 is divided into (1) cluster voltage balancing control and (2) Individual voltage balancing control [102].

The cluster voltage balancing control forces the voltage of each cluster, namely, v_{Ca}, v_{Cb} and v_{Cc}, to follow the reference cluster voltage $V_{ref,c}$.

The cluster voltages are defined as:

$$\begin{aligned} v_{Ca} &= v_{a1} + v_{a2} \\ v_{Cb} &= v_{b1} + v_{b2} \\ v_{Cc} &= v_{c1} + v_{c2} \end{aligned} \tag{4.15}$$

Here, v_{Ca}, v_{Cb} and v_{Cc} are the instantaneous values containing both ac and dc components. A low-pass filter with a cut-off frequency of 15 Hz is used to eliminate the dominant 100 Hz component from the measured dc voltages [101, 102].

In cluster balancing control each cluster voltage is calculated and compared with the cluster reference voltage $V_{ref,c}$. The cluster reference voltage ($V_{ref,c}$) can be calculated by adding the individual dc voltage references of the H-bridge cells in the cluster i.e.,

$$V_{ref,c} = N * V_{ref,i} = 2 * V_{ref,i} \tag{4.16}$$

The errors between the individual cluster voltages and $V_{ref,c}$ are processed in PI controllers and sum of the outputs of the PI controllers ($P_{loss,c}$) decides the amount of real power required to keep the cluster voltages at their corresponding reference values.

In individual voltage balancing control, each capacitor voltage is compared with the dc reference voltage ($V_{ref,i}$). The error is processed in a PI controller and the output of the PI controller decides the amount of real power required to keep that particular capacitor voltage at its reference value. The sum of the outputs of the PI controllers ($P_{loss,i}$) is the total amount of real power required to keep the capacitor voltages of individual H-bridges at their corresponding reference values. The gains of the PI controllers are properly selected to give the optimum performance.

Once the loss components of cluster and individual voltage balancing controllers are calculated, then the total compensating real power (P_{loss}) required for dc voltage regulation of 3P3W D-STATCOM is calculated as:

$$P_{loss} = P_{loss,c} + P_{loss,i} \tag{4.17}$$

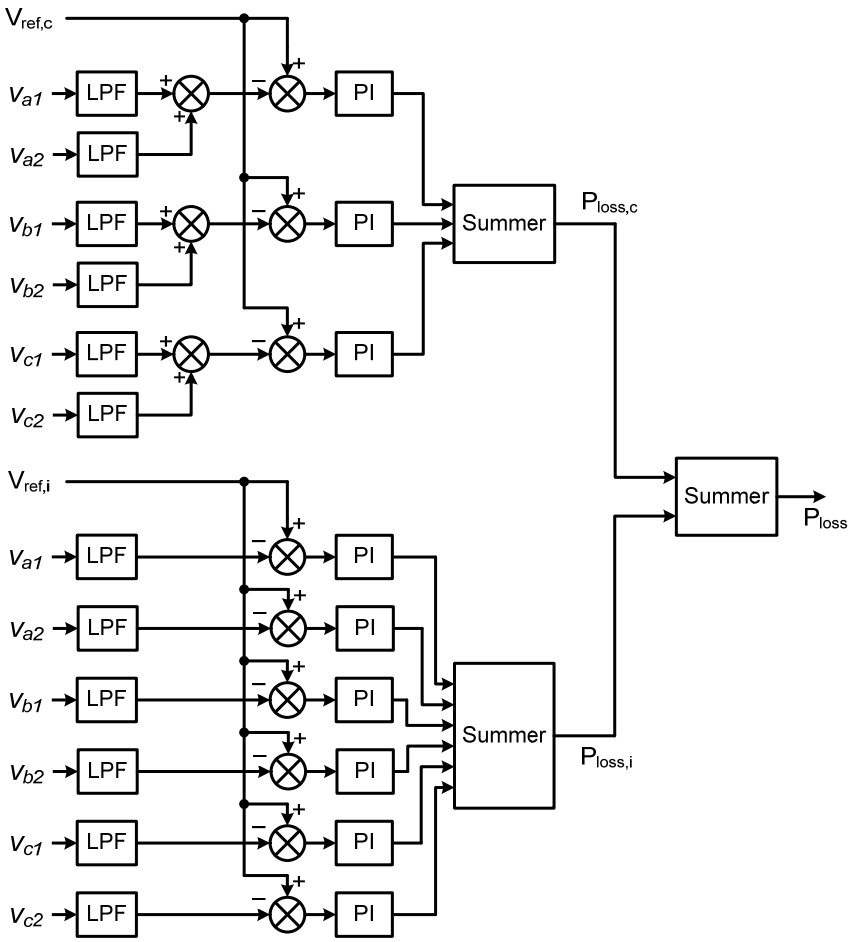


Fig. 4.10: DC voltage controller for 3P3W D-STATCOM.

(c) *PWM Controller*

In PWM controller, the actual and reference currents of 3P3W D-STATCOM are compared and a proportional plus integral controller is used for amplifying the current error in each phase. These error signals act as modulating signals for the PWM controller. In this work, method–2 carrier rotation based PWM technique is used because of its fast dynamic response. These modulating signals are compared with their corresponding carrier signals to generate the gating signals for the inverter of 3P3W D-STATCOM. This particular switching method of the inverter allows the actual 3P3W D-STATCOM currents to follow their corresponding reference currents in a closed loop-manner.

4.3.2.2 Control of Single-phase APF

The block diagram of the closed-loop control system for single-phase APF is shown in Fig. 4.11. The current reference for the single-phase APF is derived by summing up the load currents flowing in each phase as given in equation (4.6). The current reference generated is compared with the actual zigzag neutral current (i_{zn}) and the difference of these two quantities is passed through a PI controller. The output of the PI controller is compared with a triangular carrier wave to obtain the required gate patterns for the single-phase inverter.

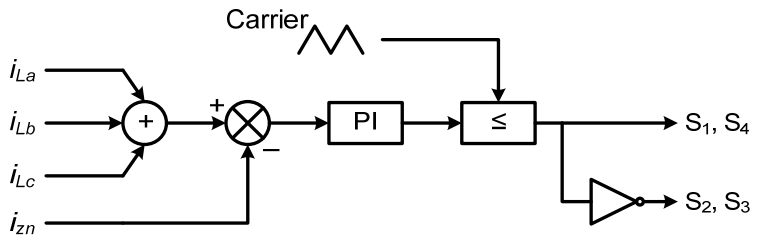


Fig. 4.11: Single-phase APF controller.

4.3.3 Selection of Passive Parameters for 3P3W D-STATCOM

The various components of 3P3W D-STATCOM such as dc capacitor and inductance of coupling reactor are selected as follows [52, 53, 55, 130].

4.3.3.1 Selection of DC Capacitors

The selection of dc capacitor rating is based on the Unit Capacitance Constant (*UCC*) described in subsection 3.3.3.1. Considering V_{dc} = 350 V (for each capacitor of the H-bridge cell), N = 2, *UCC* = 35 ms (for a ripple voltage in the range of 10%) and with a 100 kVA power conversion capability of the inverter, the calculated value of C_{dc} is 9523 μF.

4.3.3.2 Selection of Coupling Inductor

The selection of coupling inductor rating is based on design procedure described in subsection 3.3.3.2. Considering 5% peak-to-peak current ripple $i_{cr,(p-p)}$ to be 6.96 A rms $\left(\text{rated current} = \frac{100 \times 10^3}{\sqrt{3} \times 415}\right)$, the switching frequency of the converter ($2Nf_{cr}$) = $2 \times 2 \times 3$ kHz = 12 kHz, amplitude modulation index (m_a) = 1, phase-to-neutral or cluster voltage of the inverter (V_c) = $N \times V_{ref,i}$ = 700 V and overload factor (a) = 1.2, the value is calculated to be 1.008 mH.

To further optimize the value of the coupling inductor, system performance is investigated around the calculated value of the coupling inductor for the system parameters given in Table 4.3. Table 4.2 shows the performance of hybrid 3P4W D-STATCOM for the selected values of the coupling inductor. It is observed that the D-STATCOM performance can be significantly improved by reducing the filter inductor to an optimum value. In this work, the value of the coupling inductor is chosen as 1.2 mH. At this value of coupling inductor, D-STATCOM output current %THD is minimum and the system dynamic performance is satisfactory.

Table 4.2: System performance with variation of coupling inductor.

Coupling inductance L_f (mH)	Settling time (Cycles)	%THD of source current after compensation	Source power factor after compensation
0.7	1	5.13%	0.991
0.8	1	4.65%	0.992
0.9	<2	3.21%	0.998
1.0	<2	2.87%	0.999
1.1	2	1.83%	0.999
1.2	2	1.64%	0.991
1.3	<3	2.21%	0.989
1.4	3	3.73%	0.983

4.3.4 Simulation Results and Discussion

In order to verify the performance of the proposed scheme, extensive simulation studies are carried out. The simulation model of the entire system is carried out in the MATLAB/Simulink environment and the Simulink model of the entire system is shown in Fig. 4.12. The control algorithm for the D-STATCOM and APFs are also modelled in the MATLAB/Simulink using power system blocksets.

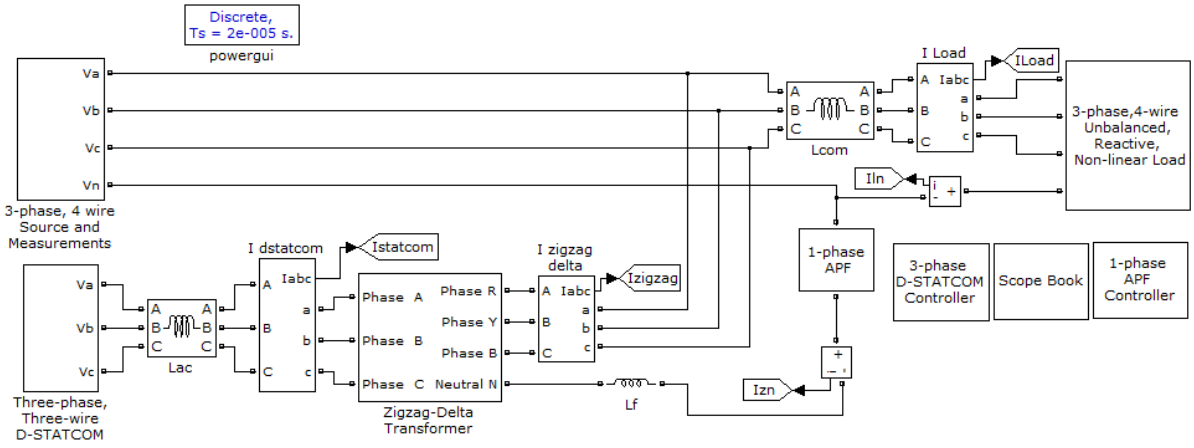


Fig. 4.12: Simulink diagram of the 3P4W hybrid D-STATCOM.

The parameters used in the simulation are given in Table 4.3. The modelled system is studied for reactive power compensation, harmonic elimination, load balancing and neutral current compensation under various operating conditions and some of the results are discussed below.

Table 4.3: Parameters used in the simulation study of 3P4W Hybrid D-STATCOM with zigzag-delta transformer, 3P3W D-STATCOM and shunt connected single-phase APF.

Parameter	**Value**
AC line voltage	Three-phase, four-wire, 415 V, 50 Hz
Line impedance	R_s = 0.01 Ω, L_s = 1 mH
DC bus voltage of 3P3W D-STATCOM	350 V (for each capacitor in the H-bridge cell)
DC bus capacitance of 3P3W D-STATCOM	9523 μF (for each capacitor in the H-bridge cell)
DC bus voltage of single-phase APF	25 V, maintained by using a single-phase boost rectifier
D-STATCOM coupling inductor	L_c = 1.2 mH
Single-phase APF output inductor	L_f = 1 mH
PWM switching frequency for 3P3W D-STATCOM	3 kHz
PWM switching frequency for single-phase APF	10 kHz
Zigzag-delta transformer	Three single-phase three-winding transformers, 50 kVA, 240/240/240 V
PI controller parameters	For cluster voltage balancing control: K_p = 1.0, K_i = 0.80 For individual voltage balancing control: K_p = 2.1, K_i = 1.7.
Load	Three-phase controlled rectifier, R_{dc} = 20 Ω, L_{dc} = 10 mH, firing angle = 20°, commutation inductance = 1.5 mH; Single-phase uncontrolled rectifier connected between the phase–*a* and the neutral, R_{dc} = 5 Ω, L_{dc} = 50 mH, commutation inductance = 1.5 mH; Single-phase controlled rectifier connected between the phase–*b* and the neutral, R_{dc} = 10 Ω, L_{dc} = 100 mH, firing angle = 30°, commutation inductance = 1.5 mH.
Sampling time	T_s = 10e–6 sec.

4.3.4.1 Performance under Ideal Utility Voltage Conditions

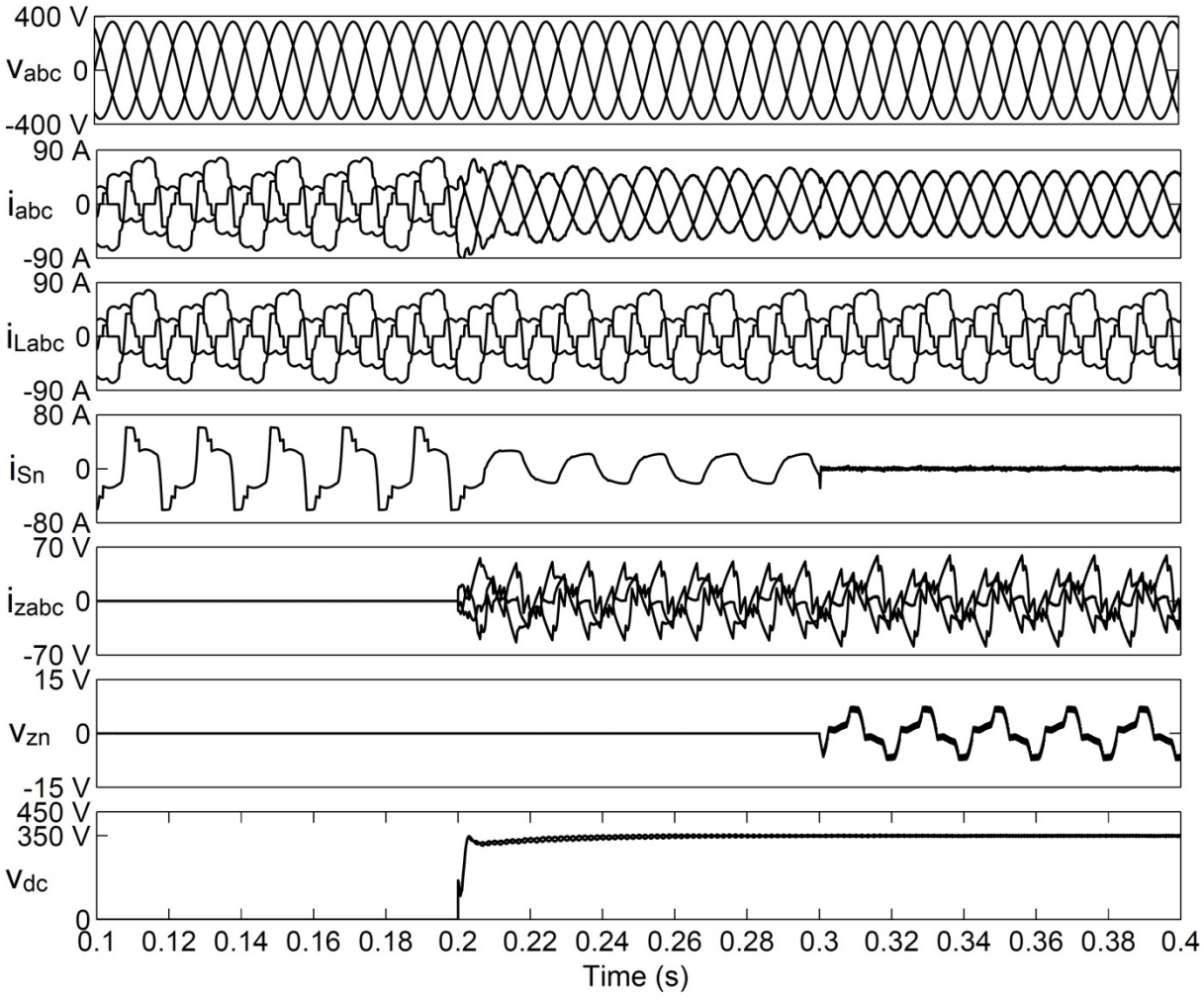
The simulated waveforms, load and source current harmonic spectra with the single-phase and three-phase reactive/non-linear loads (given in Table 4.3) under ideal utility voltage conditions are shown in Fig. 4.13(a)-(c). In Fig. 4.13(a) and all the subsequent figures showing similar waveforms, the quantities shown are as follows: trace 1–source voltages (v_{abc}); trace 2–source phase currents (i_{abc}); trace 3–three phase load currents (i_{Labc}); trace 4–source neutral current (i_n); trace 5–current injected by zigzag-delta transformer (i_{zabc}); trace 6–voltage between zigzag-delta transformer neutral and source neutral, i.e. voltage across the switch *S* (v_{zn}) and trace 7–dc side voltages of phase–*a* H-bridge cells of 3P3W D-STATCOM (v_{dc}). In order to study the performance of the 3P4W hybrid D-STATCOM, the following events are assumed to occur in the system for this and all subsequent simulation studies.

1. Before the start of the simulation, the switch *S* is closed and zigzag-delta transformer is disconnected from the system.

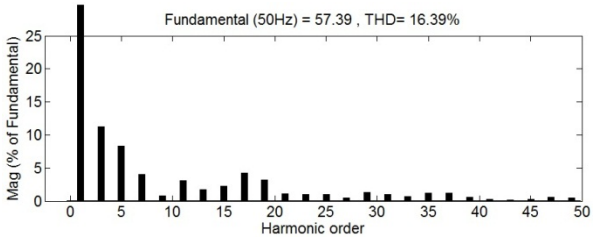
2. At *t* = 0.2 sec., the zigzag-delta transformer along with its associated 3P3W D-STATCOM is connected to the system.
3. At *t* = 0.3 sec., the switch *S* is open, i.e. the single-phase APF is connected to the system.

The following observations are made from Fig. 4.13:

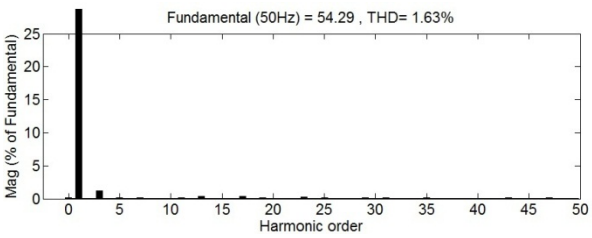
1. Before compensation with 3P4W hybrid D-STATCOM, the three-phase load current rms values are 41.1 A, 62.3 A and 22.3 A and their corresponding THD values are 16.39%, 20.43% and 28.85% for phase–*a*, phase–*b* and phase–*c* respectively.
2. The load neutral current and its THD values are 39.0 A rms (61.0 A peak) and 48.83% respectively.
3. At *t* = 0.2 sec., when only zigzag transformer and 3P3W D-STATCOM are acting as compensators (switch *S* closed), the source neutral current is reduced from 39.0 A rms to 17.18 A rms (21.5 A peak) only. Thus, the zigzag transformer attenuates the source neutral current to a large extent, but it still does not completely eliminate the same. Therefore, after compensation with 3P3W D-STATCOM, the source phase currents may become sinusoidal but unbalance in their magnitudes still exists. The observed source phase current THD values are 3.13%, 3.07% and 3.41% for phase–*a*, phase–*b* and phase–*c* respectively. The %THD values of source phase currents are reduced to a large extent but they have small amounts of zero-sequence harmonic currents.
4. At *t* = 0.3 sec., when the single-phase APF is switched-on, the compensator almost completely eliminates the source neutral current and the source phase currents become almost balanced (38.4 A, 38.8 A and 38.3 A rms for phase–*a*, phase–*b* and phase–*c* respectively) and in phase with their respective voltage waveforms, which ensures the compensation of load reactive power.
5. The THD values of source phase currents are reduced to 1.63%, 1.49% and 1.44% for phase–*a*, phase–*b* and phase–*c* respectively, which are well within the limits of IEEE–519-1992 standard recommended benchmark value of 5%. The source power factor and displacement factor are almost unity.
6. The peak voltage between the zigzag transformer neutral and the utility neutral is less than 7 V, which ensures a low VA rating of the single-phase APF. This voltage level is suitable for using the low voltage, high current rating MOSFETs.
7. At the instant 3P3W D-STATCOM is switched-on, a smooth build-up of the capacitor voltages of H-bridge cells is achieved and the steady state is reached within 1–2 cycles. The maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 18 V, which ensures the effectiveness of the dc voltage controller.



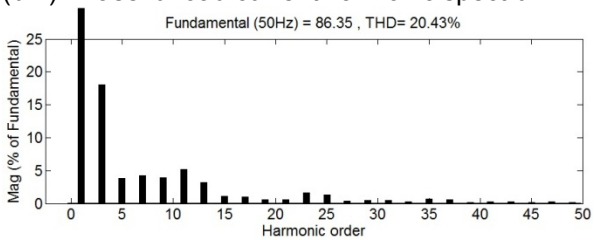
(a) Simulated waveforms



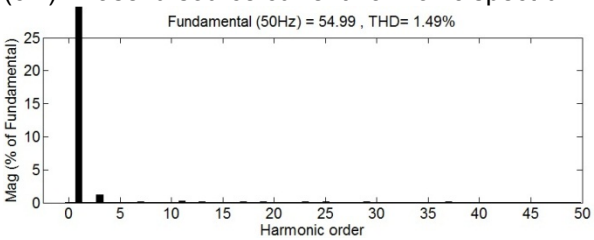
(b.1) Phase–*a* load current harmonic spectrum



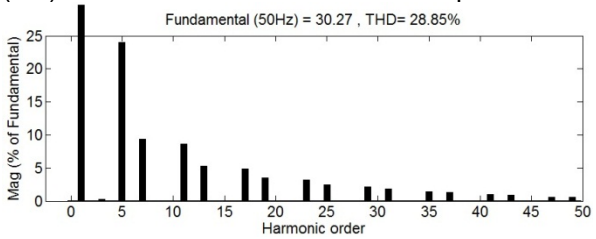
(c.1) Phase–*a* source current harmonic spectrum



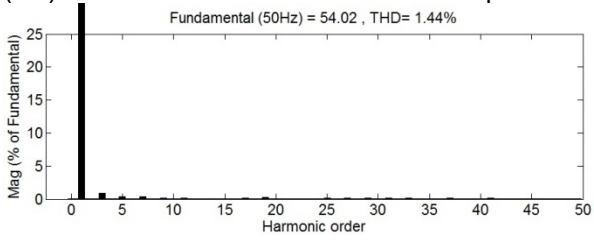
(b.2) Phase–*b* load current harmonic spectrum



(c.2) Phase–*b* source current harmonic spectrum



(b.3) Phase–*c* load current harmonic spectrum



(c.1) Phase–*c* source current harmonic spectrum

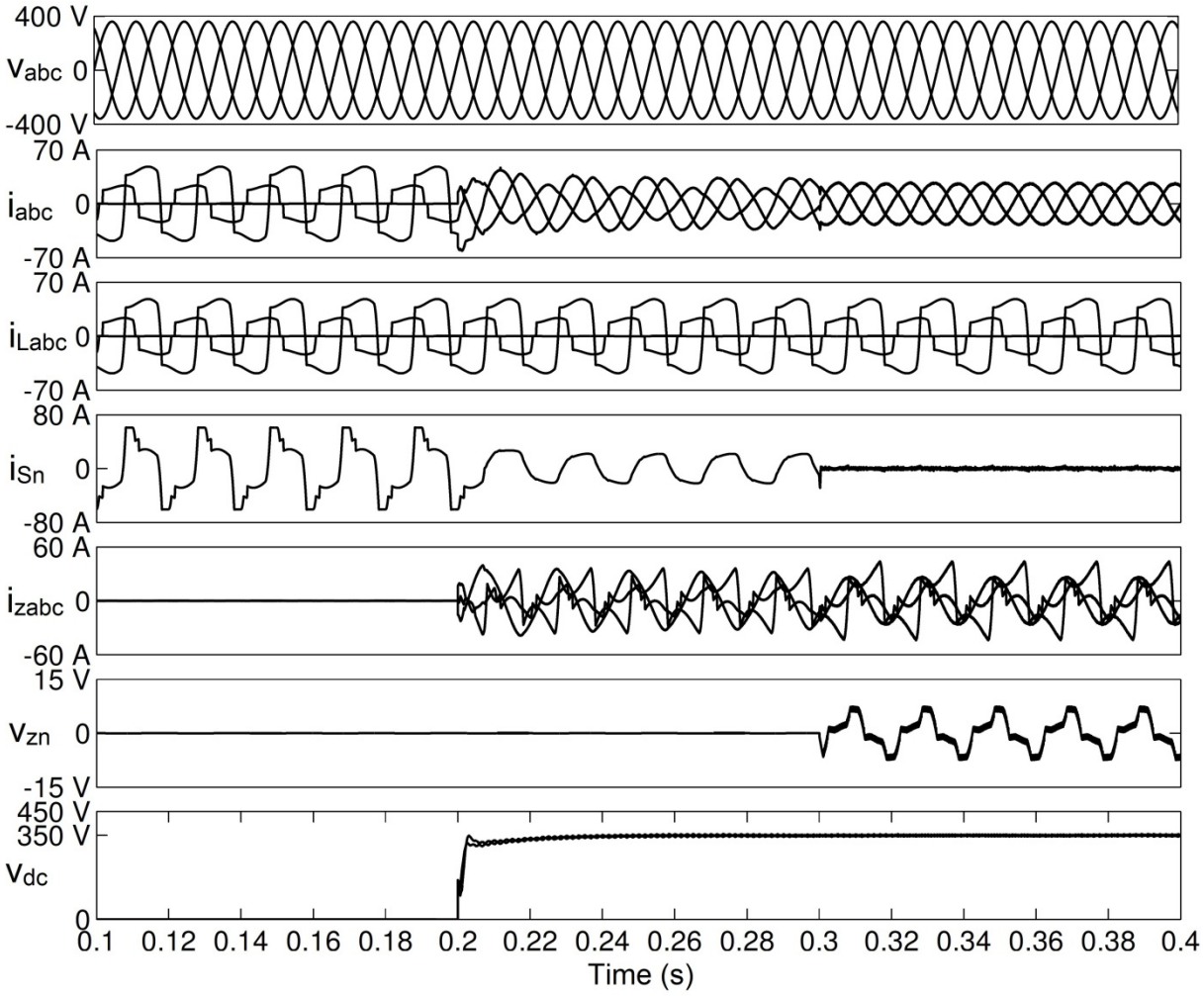
Fig. 4.13: The performance of 3P4W hybrid D-STATCOM under ideal utility voltage conditions: simulated waveforms and harmonic spectra of load and source currents.

4.3.4.2 Performance under Ideal Utility Voltage with Single-phase Loads

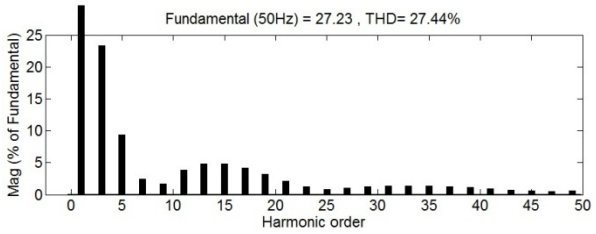
The simulation results of the 3P4W distribution power system with only single-phase reactive/non-linear loads under ideal utility voltage conditions is given in Fig. 4.14. In this simulation study, the three-phase phase-controlled rectifier is disconnected from the system.

It can be observed from Fig. 4.14 that, before compensation with 3P4W hybrid D-STATCOM, the three-phase load current rms values are 19.9 A, 42.0 A and 0 A and their corresponding THD values are 27.44%, 33.31% and 0.00% respectively for the three phases. At t = 0.2 sec., when only zigzag transformer and 3P3W D-STATCOM are acting as compensators, the source neutral current is reduced from 39.1 A rms to 17.3 A rms (21.8 A peak) only and the observed source current THD values are 9.32%, 4.41% and 7.28% for phase–*a*, phase–*b* and phase–*c* respectively. The THD values of source phase currents are reduced to a large extent but they have small amounts of zero-sequence harmonic currents.

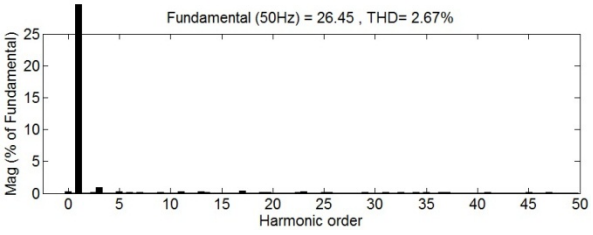
However, when the single-phase APF is switched-on, the compensator almost completely eliminated the source neutral current and the source phase currents become almost balanced (18.7 A, 19.3 A and 18.6 A rms for phase–*a*, phase–*b* and phase–*c* respectively). The THD values of source phase currents are reduced to 2.67%, 2.76% and 2.45% for phase–*a*, phase–*b* and phase–*c* respectively. The peak value of v_{zn} is less than 8 V and the maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 19 V.



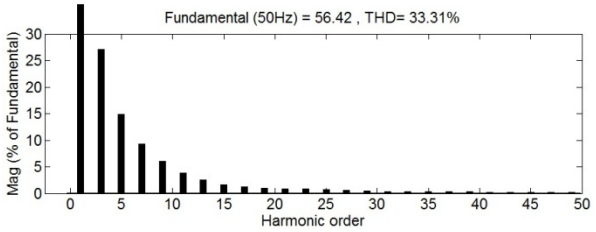
(a) Simulated waveforms



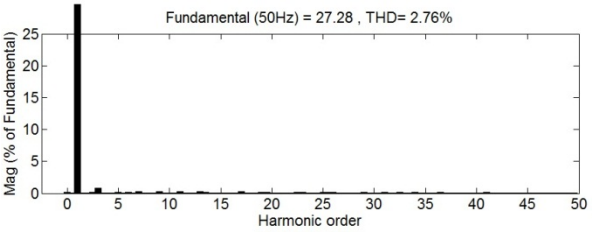
(b.1) Phase–*a* load current harmonic spectrum



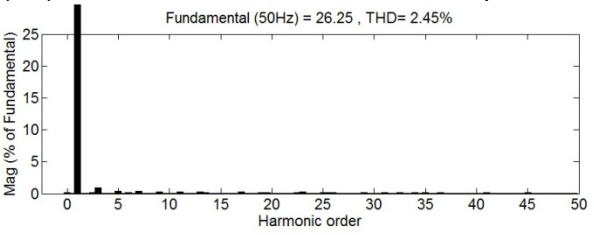
(c.1) Phase–*a* source current harmonic spectrum



(b.2) Phase–*b* load current harmonic spectrum



(c.2) Phase–*b* source current harmonic spectrum



(c.3) Phase–*c* source current harmonic spectrum

Fig. 4.14: The performance of 3P4W hybrid D-STATCOM under ideal utility voltage conditions with single-phase loads only: simulated waveforms and harmonic spectra of load and source currents.

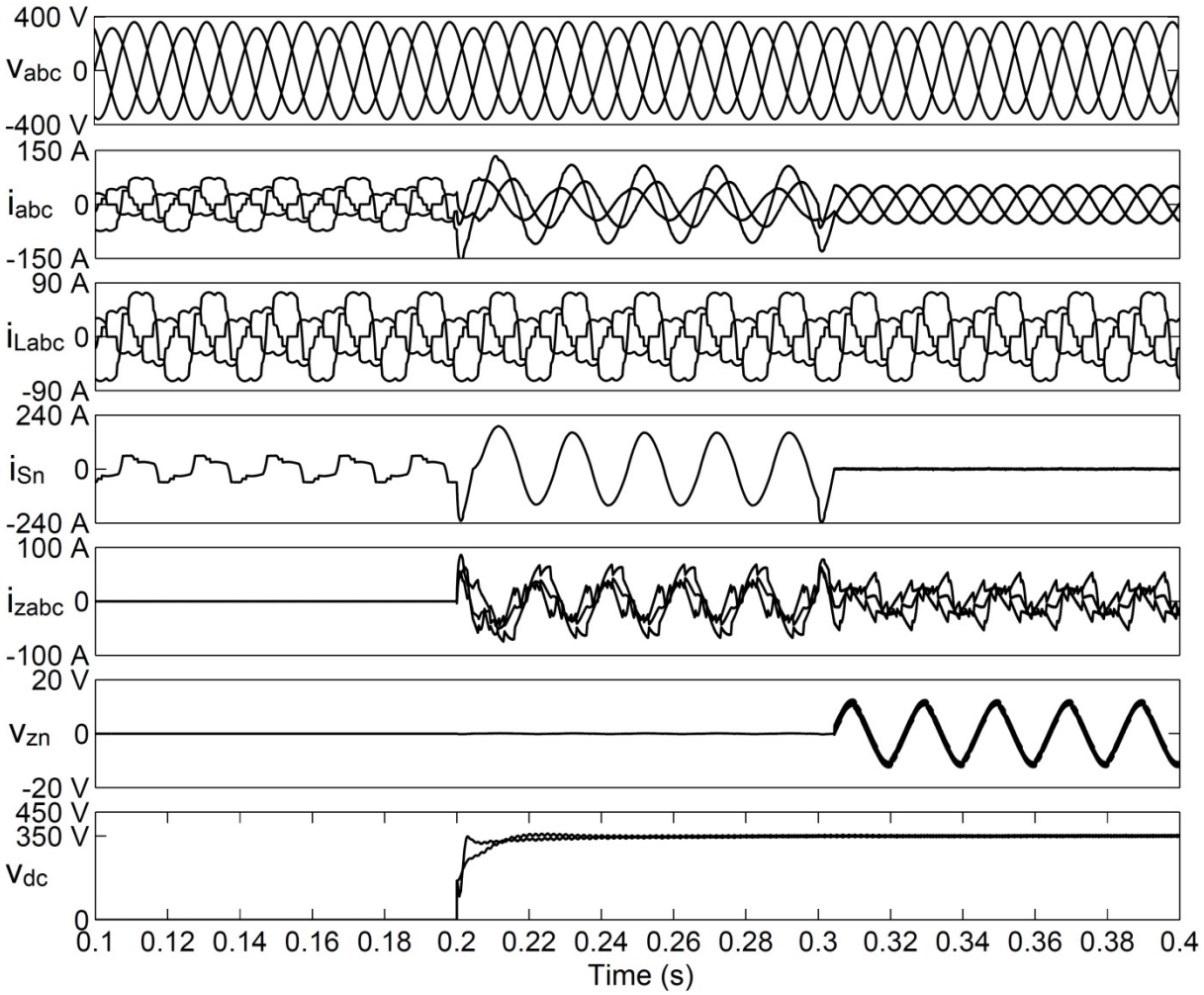
4.3.4.3 Performance under Unbalanced Utility Voltage Conditions

In many practical 3P4W distribution power systems, the unbalance in the utility voltage may occur frequently. The unbalance in the utility voltage can cause a zero-sequence voltage. When only zigzag transformer acts as a compensator, a significant amount of current flows on the neutral conductor between the utility and the zigzag transformer. But, the presence of single-phase APF improves the performance under unbalanced voltage conditions. In order to study the performance of the compensator with unbalanced voltages, both amplitude unbalance (10% voltage sag in phase–*a*) and phase-angle unbalance (0°, –110° and 120° for phase–*a*, phase–*b* and phase–*c* respectively) are introduced in the utility voltage. Fig. 4.15 shows the simulation results for this case with the single-phase and three-phase reactive/non-linear loads given in Table 4.3.

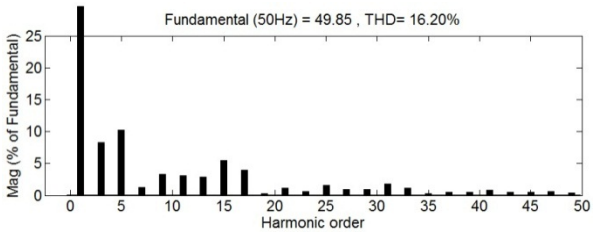
It is observed from Fig. 4.15 that, before compensation with 3P4W hybrid D-STATCOM, the three-phase load current rms values are 35.7 A, 61.7 A and 23.0 A and their corresponding THD values are 16.20%, 20.90% and 24.17% respectively for the three phases. At t = 0.2 sec., when only zigzag transformer and 3P3W D-STATCOM are acting as compensators, the source neutral current is increased from 41.3 A rms to 115.6 A rms (160 A peak), due to the presence of zero-sequence voltage in the utility. The source phase currents after compensation are observed to be unbalanced and the THD values are 4.95%, 3.57% and 4.82% for phase–*a*, phase–*b* and phase–*c* respectively. The THD values of source phase currents are reduced to a large extent but they have small amounts of zero-sequence harmonic currents. Therefore, the source phase current magnitudes are increased and the unbalance and distortions still exist. But, when the single-phase APF is switched-on, the compensator almost completely eliminates the source neutral current and the source phase currents become almost balanced (36.9 A, 37.7 A and 36.7 A rms for phase–*a*, phase–*b* and phase–*c* respectively) and in phase with their respective voltage waveform. The THD values of source phase currents are reduced to 1.36%, 1.51% and 1.41% for phase–*a*, phase–*b* and phase–*c* respectively. The maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 18 V. It is further observed that the peak value of v_{zn} is increased to 15 V. As the value is reasonably low, it still ensures a low VA rating of the single-phase inverter. However, with increased amount of unbalance, the peak value of v_{zn} further increases. Under these conditions, the single-phase APF must be protected against over-voltages.

The relation between the amount of unbalance and the peak value of v_{zn} is shown in Fig. 4.16. The amount of unbalance is represented by Voltage Unbalance Factor (VUF) and is defined as [49, 50]:

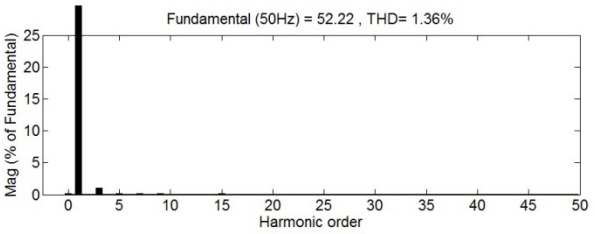
$$VUF(\%) = \frac{\text{Magnitude of negative sequence voltage}}{\text{Magnitude of positive sequence voltage}} \times 100 \qquad (4.18)$$



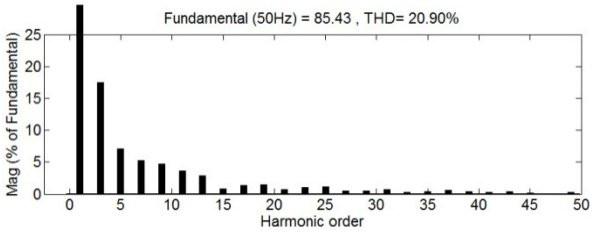
(a) Simulated waveforms



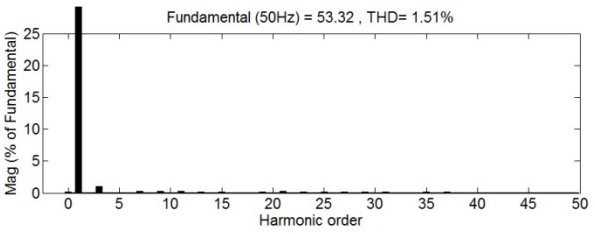
(b.1) Phase–*a* load current harmonic spectrum



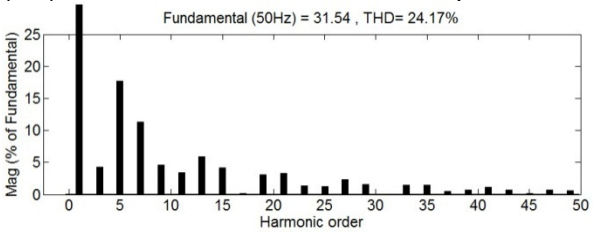
(c.1) Phase–*a* source current harmonic spectrum



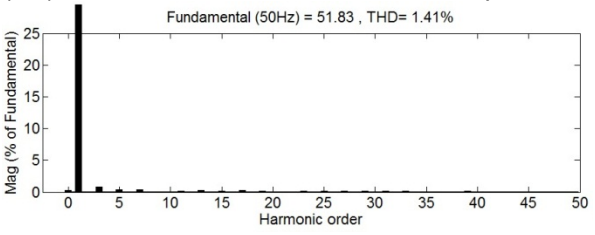
(b.2) Phase–*b* load current harmonic spectrum



(c.2) Phase–*b* source current harmonic spectrum



(b.3) Phase–*c* load current harmonic spectrum



(c.3) Phase–*c* source current harmonic spectrum

Fig. 4.15: The performance of 3P4W hybrid D-STATCOM under unbalanced utility voltage conditions: simulated waveforms and harmonic spectra of load and source currents.

From Fig. 4.16, it is observed that the peak value of v_{zn} increases with increasing VUF. Hence, under stringent unbalanced voltage conditions, the single-phase APF must be protected.

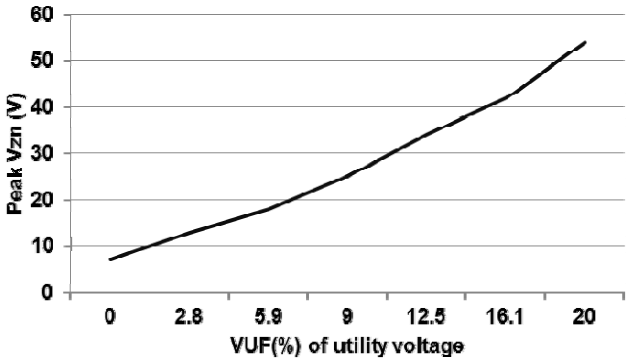


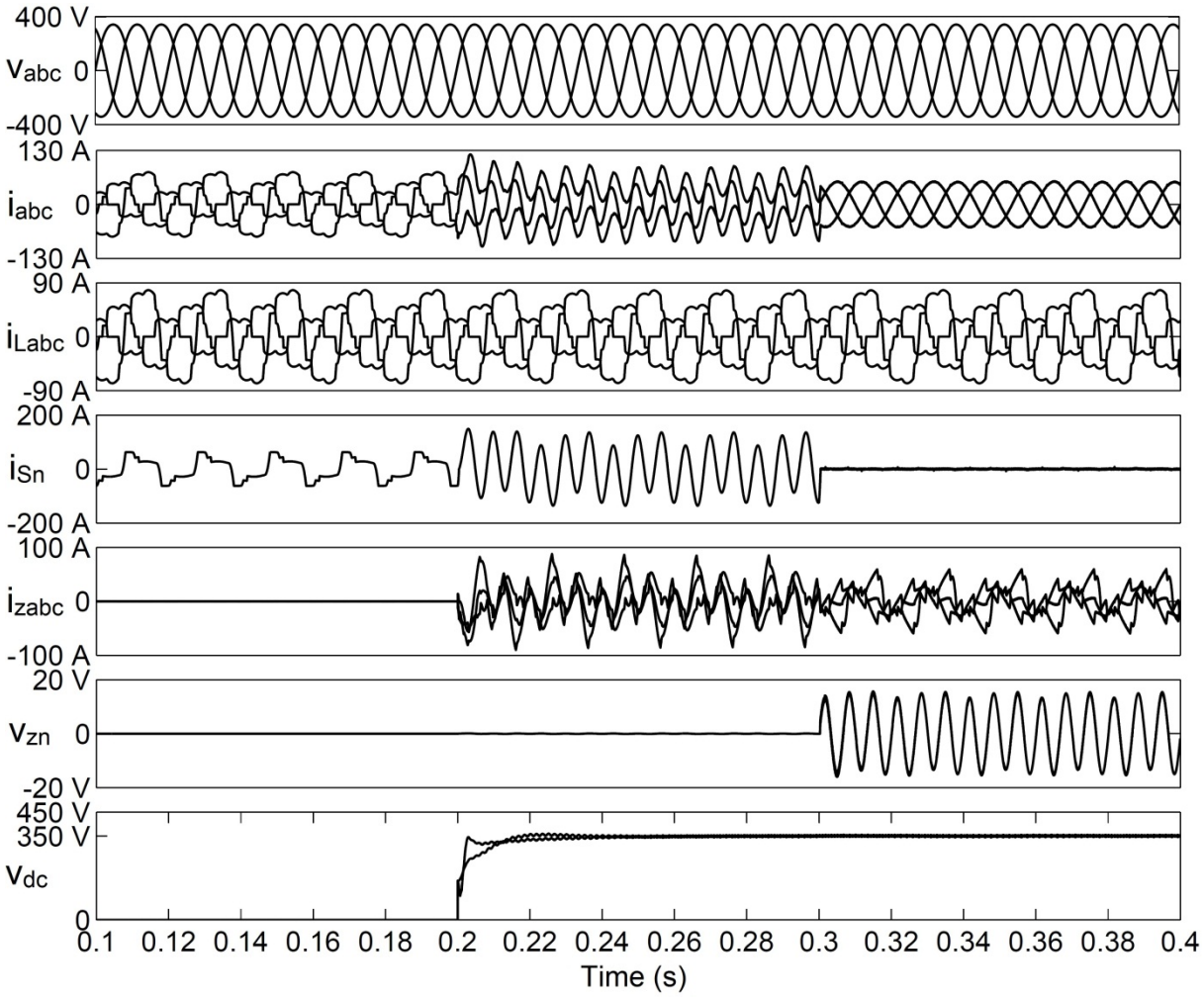
Fig. 4.16: The relation between peak value of v_{zn} and %VUF of utility voltage.

4.3.4.4 Performance under Distorted Utility Voltage Conditions

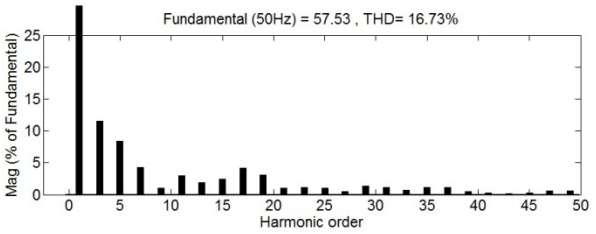
The presence of zero-sequence harmonics in the utility voltage can cause a significant amount of zero-sequence voltage. To verify the efficacy of the compensator in improving the performance under distorted utility voltage conditions, a 5% 3rd order harmonic component is introduced in the utility voltages. Fig. 4.17 shows the simulation results under this condition with the single-phase and three-phase reactive/non-linear loads given in Table 4.3.

It can be observed from Fig. 4.17 that, before compensation with 3P4W hybrid D-STATCOM, the three-phase load current rms values are 41.2 A, 63.0 A and 22.3 A and their corresponding THD values are 16.73%, 21.37% and 28.86% respectively for the three phases. At t = 0.2 sec., when only zigzag transformer and 3P3W D-STATCOM are acting as compensators, the source neutral current is increased from 40.0 A rms to 84.4 A rms (136 A peak), due to the presence of zero-sequence voltage in the utility. The source phase currents after compensation are observed to be unbalanced and the THD values are 83.95%, 61.02% and 69.16% for phase–*a*, phase–*b* and phase–*c* respectively. The huge enhancement of source phase current %THDs is due to the circulation of large amount of zero-sequence current between source and zigzag transformer which is caused by the zero-sequence voltage in the utility. This current is not being compensated by the 3P3W D-STATCOM.

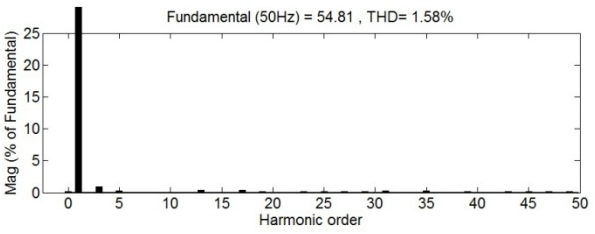
However, when the single-phase APF is switched-on, the compensator almost completely eliminates the source neutral current and the source phase currents become almost balanced (38.8 A, 39.2 A and 38.6 A rms for phase–*a*, phase–*b* and phase–*c* respectively) and in phase with their respective voltage waveform. The THD values of source phase currents are reduced to 1.58%, 1.72% and 1.76% for phase–*a*, phase–*b* and phase–*c* respectively. The maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 21 V. It is further observed that the peak value of v_{zn} is increased to 17 V and still ensures a low VA rating of the single-phase inverter. However, with increased amount of distortion in utility voltage, the peak value of v_{zn} further increases.



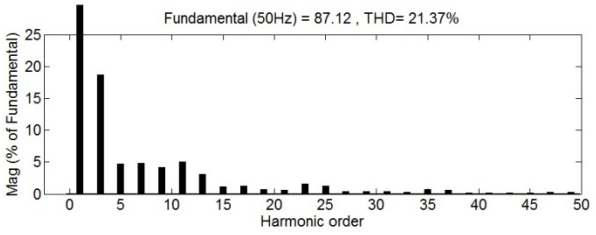
(a) Simulated waveforms



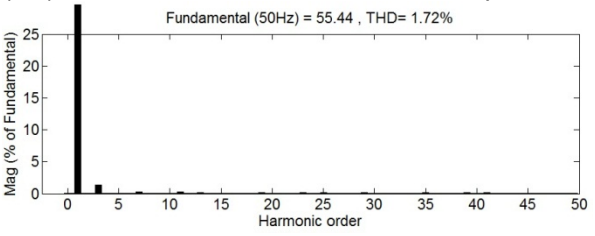
(b.1) Phase–*a* load current harmonic spectrum



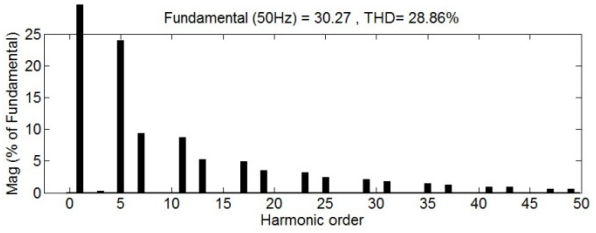
(c.1) Phase–*a* source current harmonic spectrum



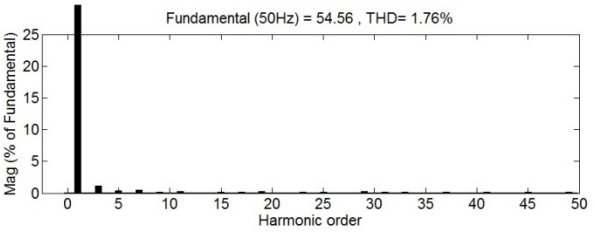
(b.2) Phase–*b* load current harmonic spectrum



(c.2) Phase–*b* source current harmonic spectrum



(b.3) Phase–*c* load current harmonic spectrum



(c.3) Phase–*c* source current harmonic spectrum

Fig. 4.17: The performance of 3P4W hybrid D-STATCOM under distorted utility voltage conditions: simulated waveforms and harmonic spectra of load and source currents.

The relation between zero-sequence harmonic voltage in the utility and peak value of v_{zn} is shown in Fig. 4.18. In this simulation study, only 3rd order harmonic component is only considered as a zero-sequence harmonic voltage. From Fig. 4.18 it is observed that the peak value of v_{zn} is increased with increasing amount of 3rd order harmonic component. Hence, under stringent distorted voltage conditions, the single-phase APF and zigzag transformer must be protected.

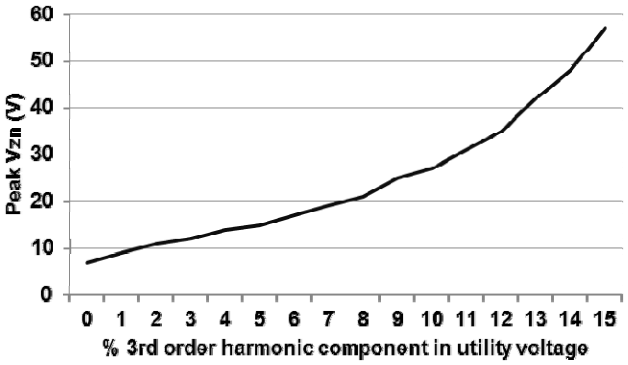
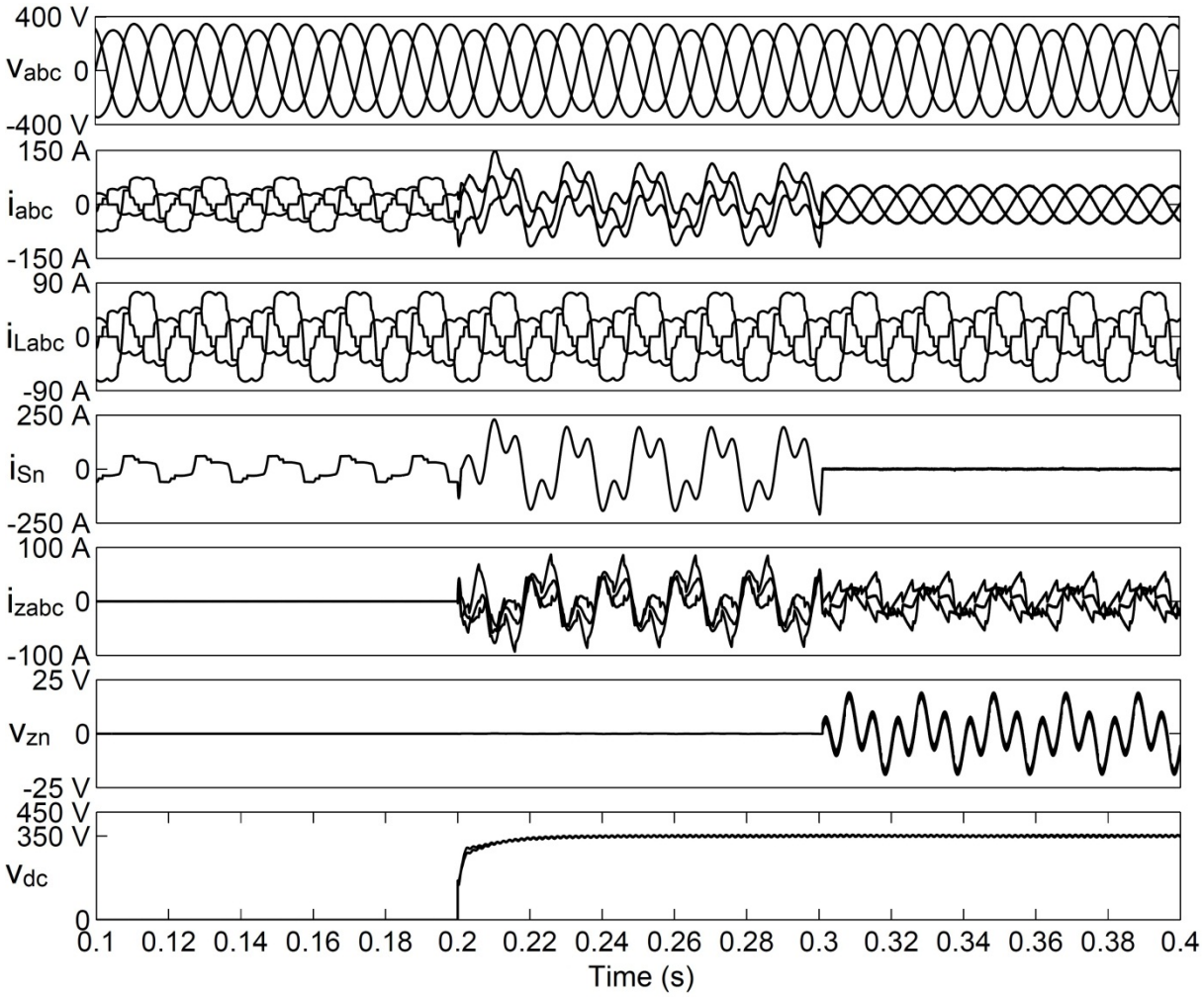


Fig. 4.18: The relation between peak value of v_{zn} and % 3rd order harmonic component in utility voltage.

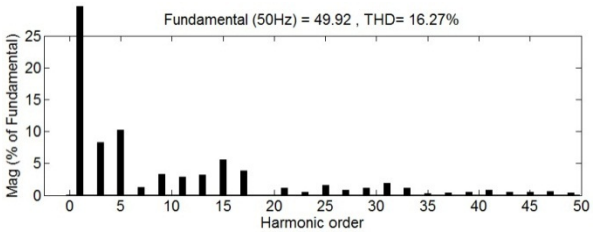
4.3.4.5 Performance under Non-ideal Utility Voltage Conditions

In addition to the unbalance, if distortion is also present in the utility voltage, the amount of zero-sequence voltage will be very high. Fig. 4.19 shows the simulation results under unbalanced (10% voltage sag in phase–*a* and phase angles of 0°, –110° and 120° for phase–*a*, phase–*b* and phase–*c* respectively) and distorted (5% 3rd order harmonic component) utility voltage condition with the single-phase and three-phase reactive/non-linear loads given in Table 4.3.

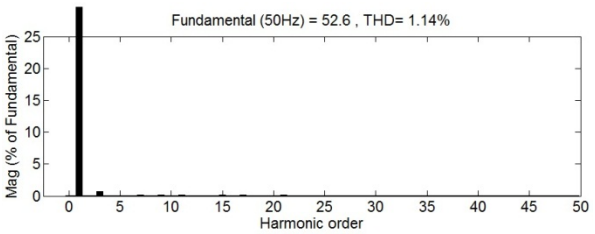
As shown in Fig. 4.19, before compensation with 3P4W hybrid D-STATCOM, the three-phase load current rms values are 35.8 A, 62.4 A and 23.0 A and their corresponding THD values are 16.27%, 21.51% and 24.16% respectively for the three phases. At t = 0.2 sec., when only zigzag transformer and 3P3W D-STATCOM are acting as compensators, the source neutral current is increased from 42.0 A rms to 120.4 A rms (194.2 A peak), due to the presence of high zero-sequence voltage in the utility. The phase currents after compensation are observed to be unbalanced and the THD values are 73.73%, 26.50% and 44.06% for phase–*a*, phase–*b* and phase–*c* respectively. As before, the huge enhancement of source phase current %THDs is due to the circulation of large zero-sequence current between source and zigzag transformer.



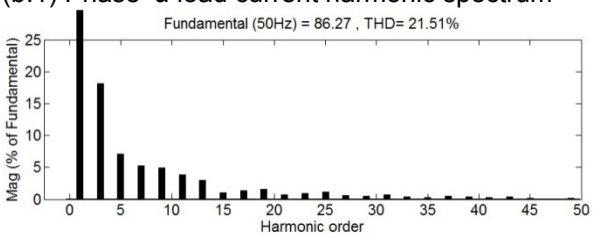
(a) Simulated waveforms



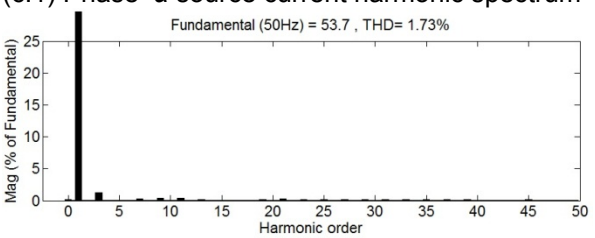
(b.1) Phase–*a* load current harmonic spectrum



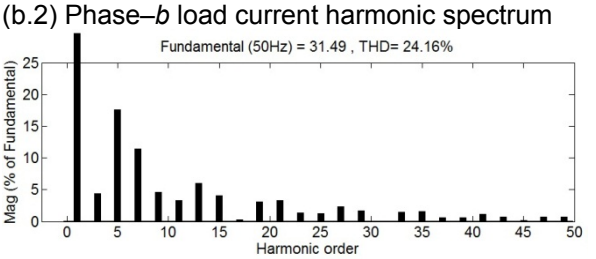
(c.1) Phase–*a* source current harmonic spectrum



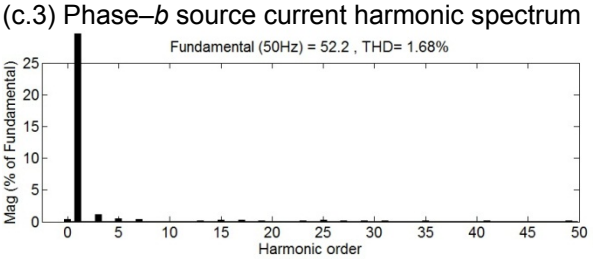
(b.2) Phase–*b* load current harmonic spectrum



(c.3) Phase–*b* source current harmonic spectrum



(b.3) Phase–*c* load current harmonic spectrum



(c.3) Phase–*c* source current harmonic spectrum

Fig. 4.19: The performance of 3P4W hybrid D-STATCOM under non-ideal utility voltage conditions: simulated waveforms and harmonic spectra of load and source currents.

When the single-phase APF is switched-on, the compensator almost completely eliminates the source neutral current and the source phase currents become almost balanced (37.2 A, 38.0 A and 36.9 A rms for phase–*a*, phase–*b* and phase–*c* respectively) and in phase with their respective voltage waveform. The THD values of source phase currents are reduced to 1.14%, 1.73% and 1.68% for phase–*a*, phase–*b* and phase–*c* respectively. The maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 20 V, which ensures the effectiveness of the dc voltage controller with distorted/unbalanced utility voltage conditions also. It is observed that the peak value of v_{zn} is further increased to 21 V. However, with increased amount of distortion/unbalance in utility voltage, the peak value of v_{zn} further increases.

4.4 A 3P4W Hybrid D-STATCOM with T-connected Transformer, 3P3W D-STATCOM and Shunt Connected Single-phase APF

Fig. 4.20 shows the schematic diagram of the proposed hybrid 3P4W compensator and the realization of the T-connected transformer with two single-phase transformers is shown in Fig. 4.21.

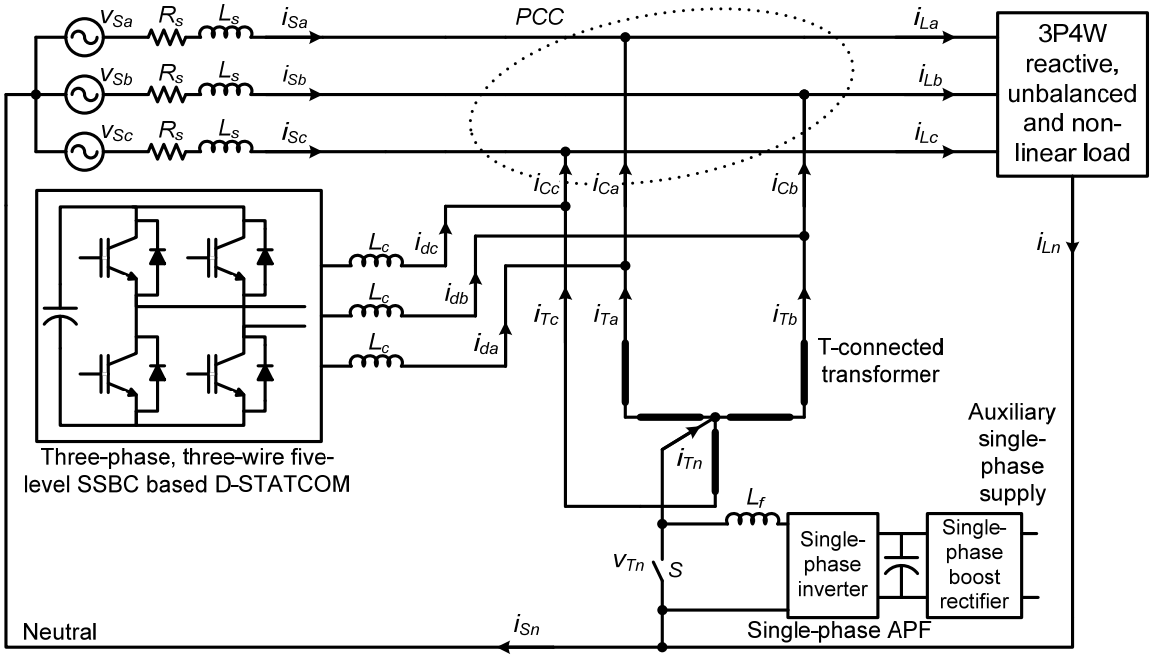


Fig. 4.20: Schematic diagram of a reduced rating hybrid D-STATCOM for 3P4W distribution systems using T-connected transformer, 3P3W D-STATCOM and shunt connected single-phase APF.

As shown in Fig. 4.20, the T-connected transformer and 3P3W D-STATCOM is connected at the PCC. The 3P3W D-STATCOM is realised by using a five-level SSBC based modular multilevel inverter as shown in Fig. 4.7. The 3P3W D-STATCOM produces the desired three-phase currents for compensation of (a) positive and negative sequence harmonics in source currents and (b) reactive power of the load. The capacitor on the DC side of the three-phase inverter of the D-STATCOM is charged by drawing real power from

the distribution grid. A single-phase APF is connected between the neutral conductor of the utility and the neutral point of the T-connected transformer. The realisation of single-phase APF is shown in Fig. 4.8. The single-phase APF produces the desired current for compensating source neutral current and injects the produced current through the neutral of the T-connected transformer. The inverter of the single-phase APF is energized from a separate single-phase boost rectifier of a very low VA rating. To protect the single-phase APF under abnormal conditions, a switch (*S*) is connected across it.

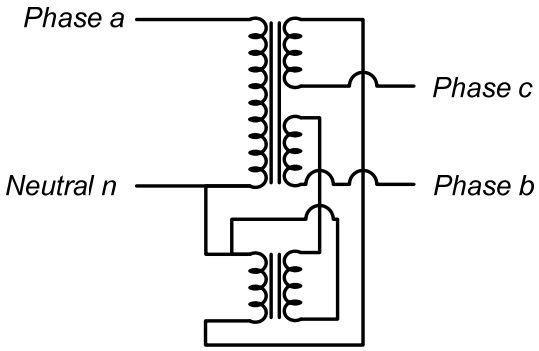


Fig. 4.21: Realization of a T-connected transformer using two single-phase transformers.

4.4.1 Operation of the Scheme under Various Utility Voltages

The operation of this scheme under unbalanced and/or distorted voltage is identical to the zigzag transformer based topology as discussed in 4.3.1.

4.4.2 Control of 3P3W D-STATCOM

A five-level SSBC based modular multilevel inverter is used to realise the 3P3W D-STATCOM. The control of 3P3W D-STATCOM involves the calculation of reference compensating currents, dc voltage controller and PWM control of the inverter. The block diagram of the controller is shown in Fig. 4.22. The block diagram is divided into three blocks as follows:

1. Generation of 3P3W D-STATCOM reference currents
2. DC voltage controller
3. PWM controller

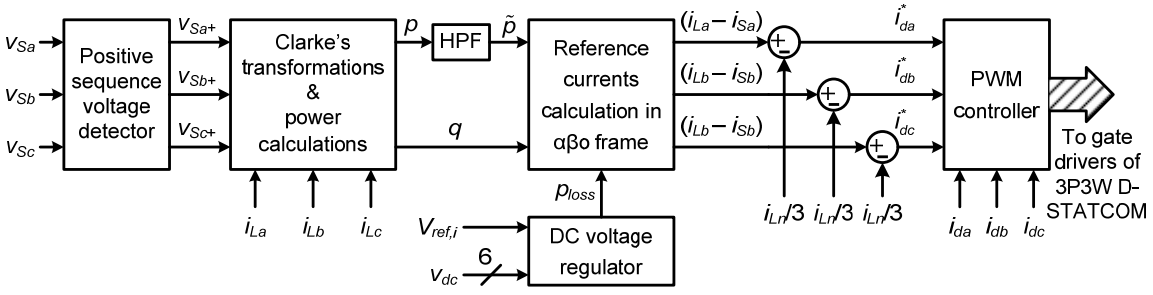


Fig. 4.22: Block diagram of the 3P3W D-STATCOM controller.

The detailed description for the generation of 3P3W D-STATCOM reference currents is given below and the descriptions for the remaining blocks i.e. dc voltage controller and PWM controller are identical to subsections 4.3.2.1(b) and 4.3.2.1(c) respectively.

To obtain the reference currents of 3P3W D-STATCOM, the following assumptions are made:

1. The magnetizing currents drawn by the T-connected transformer are neglected.
2. The capacitor of the 3P3W D-STATCOM is ideal and does not require any real power from the utility to maintain its dc voltage at the reference value.

In Fig. 4.20, i_{La}, i_{Lb} and i_{Lc} are the load phase currents and i_{Ln} is the load neutral current. Therefore,

$$i_{Ln} = i_{La} + i_{Lb} + i_{Lc} \tag{4.19}$$

Let, $i_{da,}$ i_{db} and i_{dc} are the currents injected into the utility due to the operation of 3P3W D-STATCOM and $i_{Ta,}$ i_{Tb} and i_{Tc} are the currents injected into the utility through the T-connected transformer due to the operation of the single-phase APF. Under ideal conditions (complete compensation of source neutral current, i.e. i_{Sn} = 0), this current (i.e. from the single-phase APF) splits equally with $i_{Ln}/3$ flowing through each of the T-connected transformer windings. Hence,

$$i_{Ta} = i_{Tb} = i_{Tc} = \frac{i_{Ln}}{3} \tag{4.20}$$

Let, $i_{Sa,}$ i_{Sb} and i_{Sc} are considered to be fundamental, unity power factor source currents after compensation with 3P4W hybrid D-STATCOM, then application KCL at PCC in Fig. 4.20 gives the following equations:

$$\begin{aligned} i_{da} &= \left(i_{La} - i_{Sa}\right) - \frac{i_{Ln}}{3} \\ i_{db} &= \left(i_{Lb} - i_{Sb}\right) - \frac{i_{Ln}}{3} \\ i_{dc} &= \left(i_{Lc} - i_{Sc}\right) - \frac{i_{Ln}}{3} \end{aligned} \tag{4.21}$$

The load harmonic and reactive currents, ($i_{La} - i_{Sa}$), ($i_{Lb} - i_{Sb}$) and ($i_{Lc} - i_{Sc}$) are calculated by using IRP theory based method as explained in subsection 4.3.2.1(a). Once the load harmonic and reactive currents are calculated, the reference currents for the 3P3W D-STATCOM are calculated using equation (4.21).

4.4.3 Control of Single-phase APF

The block diagram of the closed-loop control of the single-phase APF is shown in Fig. 4.23. The current reference for the single-phase APF is derived by summing up the load currents flowing in each phase as given in equation (4.6). The current reference generated is compared with the actual T-connected transformer neutral current (i_{Tn}) and the difference of

these two quantities is passed through a PI controller. The output of the PI controller is compared with the triangular carrier wave to obtain the required gate patterns for the single-phase inverter.

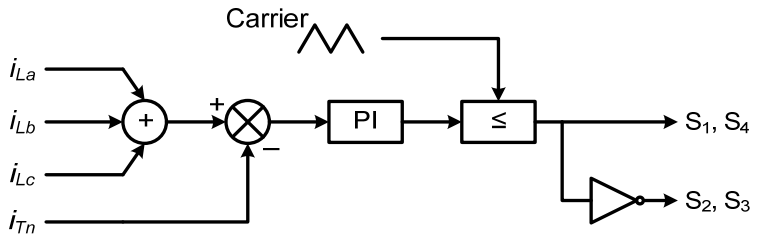


Fig. 4.23: Single-phase APF controller.

4.4.4 Selection of Passive Parameters for 3P3W D-STATCOM

The various components of 3P3W D-STATCOM such as dc capacitor and inductance of coupling reactor are designed based on the design description given in subsection 4.3.3.

4.4.5 Simulation Results and Discussion

In order to verify the performance of the proposed scheme, extensive simulation studies are carried out. The simulation model of the entire system is carried out in MATLAB/Simulink® environment and the Simulink model of the entire system is shown in Fig. 4.24. The control algorithm for the D-STATCOM and APFs are also modelled by using MATLAB/Simulink® power system blocksets. The parameters used in the simulation are given in Table 4.4. The modelled system is studied for reactive power compensation, harmonic elimination, load balancing and neutral current compensation under various operating conditions and some of the results are discussed below.

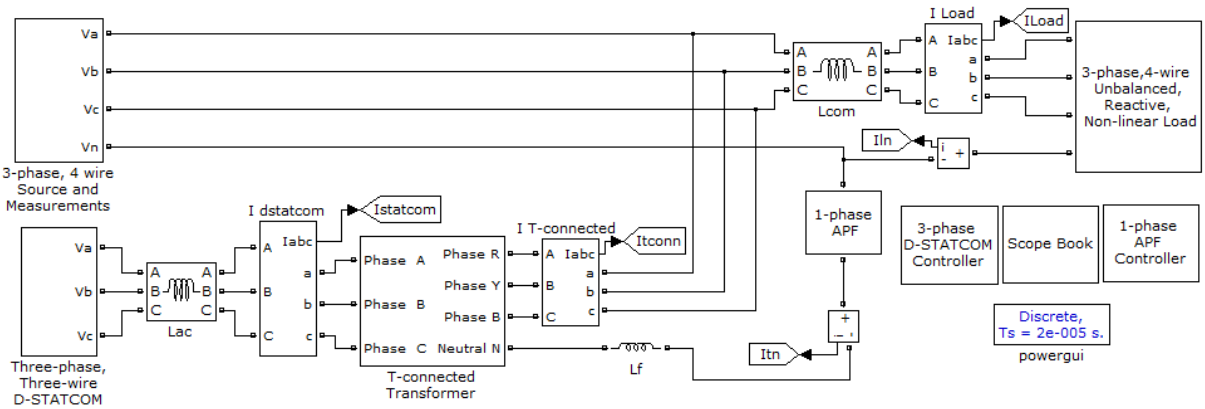


Fig. 4.24: Simulink diagram of the 3P4W hybrid D-STATCOM.

Table 4.4: Parameters used in the simulation study of 3P4W hybrid D-STATCOM with T-connected transformer, 3P3W D-STATCOM and shunt connected single-phase APF.

Parameter	**Value**
AC line voltage	Three-phase, four-wire, 415 V, 50 Hz
Line impedance	R_s = 0.01 Ω, L_s = 1 mH
DC bus voltage of 3P3W D-STATCOM	350 V (for each capacitor in the H-bridge cell)
DC bus capacitance of 3P3W D-STATCOM	9523 μF (for each capacitor in the H-bridge cell)
DC bus voltage of single-phase APF	25 V, maintained by using a single-phase boost rectifier
D-STATCOM coupling inductor	L_c = 1.2 mH
Single-phase APF output inductor	L_f = 1 mH
PWM switching frequency for 3P3W D-STATCOM	3 kHz
PWM switching frequency for single-phase APF	10 kHz
T-connected transformer	single-phase three-winding transformers, 75 kVA, 240/120/120 V and single-phase two-winding transformers, 75 kVA, 208/208 V [55]
PI controller parameters	For cluster voltage balancing control: K_p = 1.1, K_i = 0.83 For individual voltage balancing control: K_p = 2, K_i = 1.7.
Load	Three-phase controlled rectifier, R_{dc} = 20 Ω, L_{dc} = 10 mH, firing angle = 20°, commutation inductance = 1.5 mH; Single-phase uncontrolled rectifier connected between the phase–*a* and the neutral, R_{dc} = 5 Ω, L_{dc} = 50 mH, commutation inductance = 1.5 mH; Single-phase controlled rectifier connected between the phase–*b* and the neutral, R_{dc} = 10 Ω, L_{dc} = 100 mH, firing angle = 30°, commutation inductance = 1.5 mH.
Sampling time	T_s = 10e–6 sec.

4.4.5.1 Performance under Ideal Utility Voltage Conditions

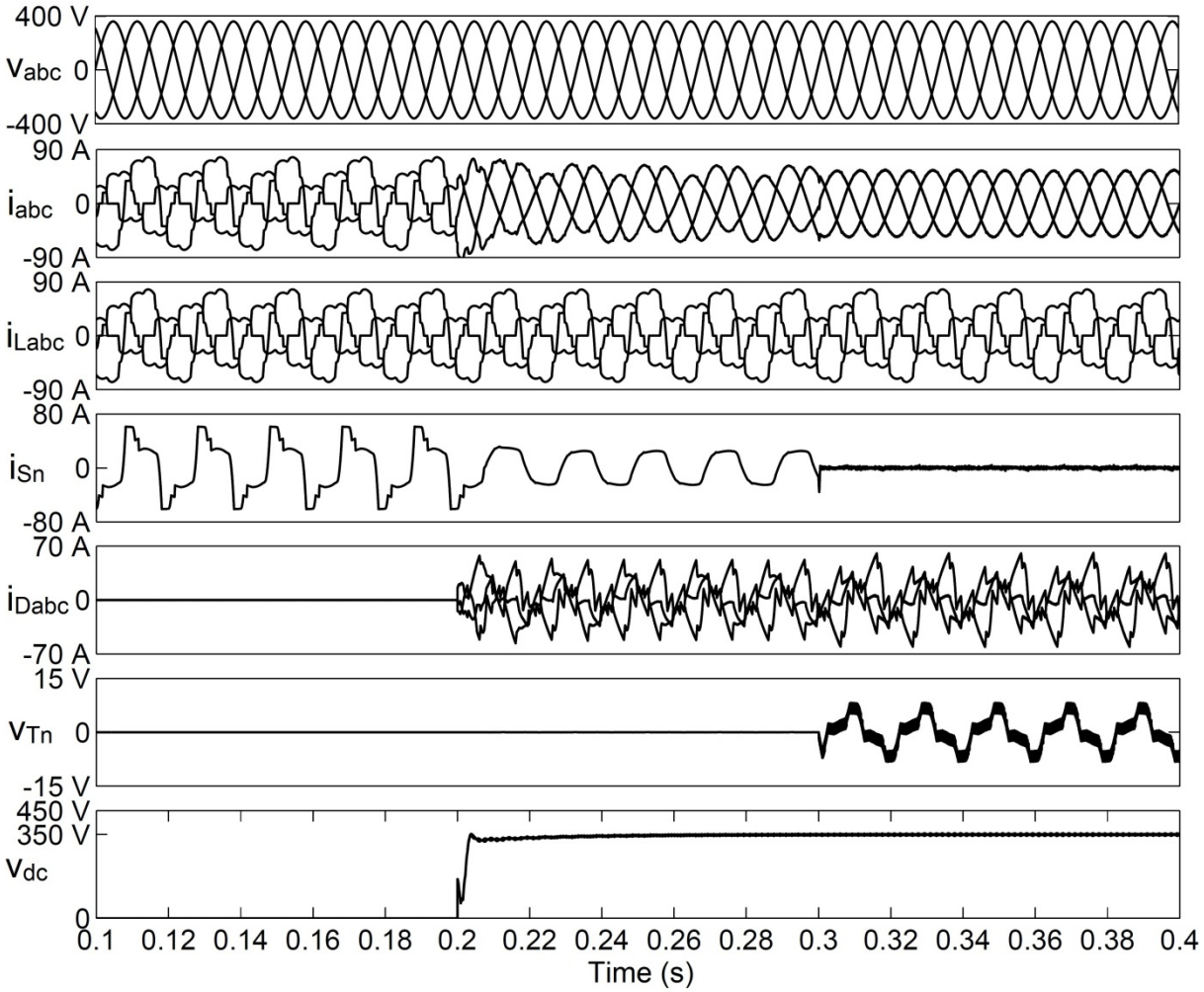
The simulated waveforms, load and source current harmonic spectra with the single-phase and three-phase (given in Table 4.4) reactive/non-linear loads under ideal utility voltage conditions are shown in Fig. 4.25(a)-(c). In Fig. 4.25(a) and all the subsequent figures showing similar waveforms, the quantities which are shown are as follows: trace 1–source voltages (v_{abc}); trace 2–source phase currents (i_{abc}); trace 3–three phase load currents (i_{Labc}); trace 4–source neutral current (i_n); trace 5–The total current injected by the 3P4W D-STATCOM at PCC (i_{Dabc}); trace 6–voltage between T-connected transformer neutral and source neutral, i.e. voltage across the switch *S* (v_{Tn}) and trace 7–dc side voltages of phase–*a* H-bridge cells of 3P3W D-STATCOM (v_{dc}).

In order to study the performance of 3P4W hybrid D-STATCOM, the following events are assumed to occur in the system for this and all subsequent simulation studies.

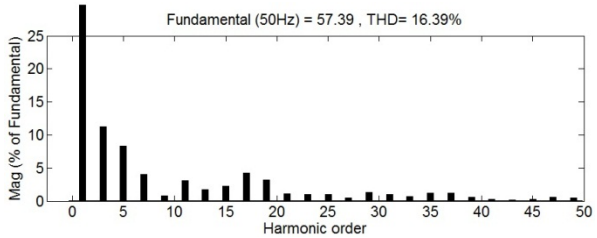
1. Before the start of the simulation, the switch *S* is closed and T-connected transformer and 3P3W D-STATCOM are disconnected from the system.
2. At *t* = 0.2 sec., the T-connected transformer and 3P3W D-STATCOM are connected to the system.
3. At *t* = 0.3 sec., the switch *S* is open, i.e. the single-phase APF is connected to the system.

The following observations are made from Fig. 4.25,:

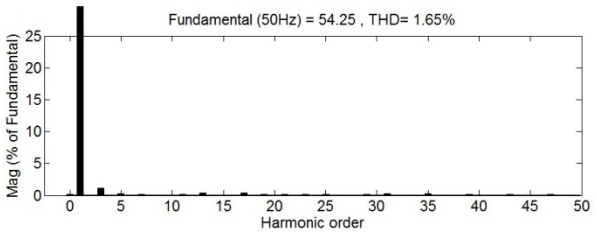
1. Before compensation with 3P4W hybrid D-STATCOM, the three-phase load current rms values are 41.1 A, 62.3 A and 22.3 A and their corresponding THD values are 16.39%, 20.43% and 28.85% for phase–*a*, phase–*b* and phase–*c* respectively.
2. The load neutral current and its %THD values are 39.0 A (61.0 A peak) and 48.83% respectively.
3. At *t* = 0.2 sec., when only T-connected transformer and 3P3W D-STATCOM are acting as compensators (switch *S* closed), the source neutral current is reduced from 39.0 A rms to 20.8 A rms (25.1 A peak). Thus, the T-connected transformer attenuates the source neutral current to a large extent, but it still does not completely eliminate the same. Therefore, after compensation with 3P3W D-STATCOM, the source phase currents may become sinusoidal but unbalance in their magnitudes still exists. The observed source phase current THD values are 5.06%, 2.81% and 4.39% for phase–*a*, phase–*b* and phase–*c* respectively. Again the %THD values of source phase currents are reduced to a large extent but they still have small amounts of zero-sequence harmonics.
4. At *t* = 0.3 sec., when the single-phase APF is switched-on, the compensator almost completely eliminates the source neutral current and the source phase currents become almost balanced (38.4 A, 39.5 A and 39.7 A for phase–*a*, phase–*b* and phase–*c* respectively) and in phase with their respective voltage waveforms, which ensures the compensation of load reactive power.
5. The THD values of source phase currents are reduced to 1.65%, 1.52% and 1.47% for phase–*a*, phase–*b* and phase–*c* respectively, which are well within the limits of IEEE–519-1992 standard recommended benchmark value of 5%. The source power factor and displacement factor are almost become unity.
6. The peak voltage between the T-connected transformer neutral and the utility neutral is less than 8 V, which ensures a low VA rating of the single-phase APF.
7. At the instant 3P3W D-STATCOM is switched-on, a smooth build-up of the capacitor voltages of H-bridge cells is achieved and the steady-state is reached within 1–2 cycles. The maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 19 V, which ensures the effectiveness of the dc voltage controller.



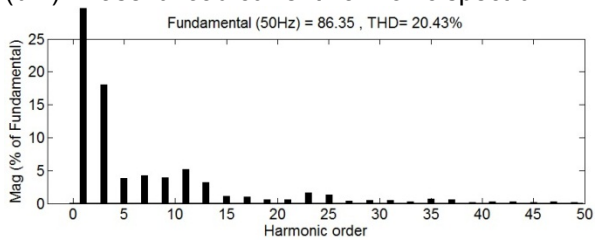
(a) Simulated waveforms



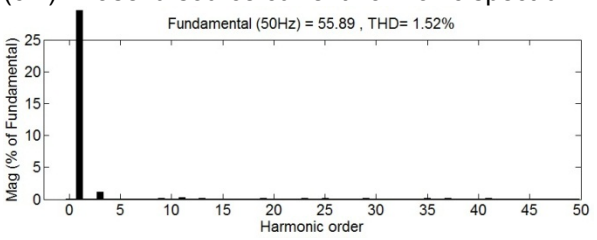
(b.1) Phase–*a* load current harmonic spectrum



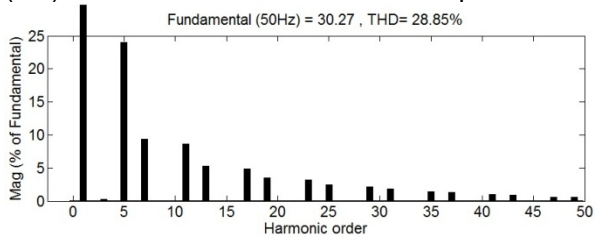
(c.1) Phase–*a* source current harmonic spectrum



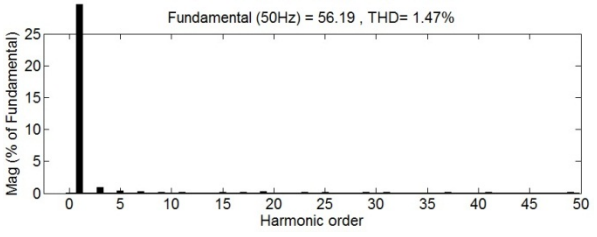
(b.2) Phase–*b* load current harmonic spectrum



(c.2) Phase–*b* source current harmonic spectrum



(b.3) Phase–*c* load current harmonic spectrum



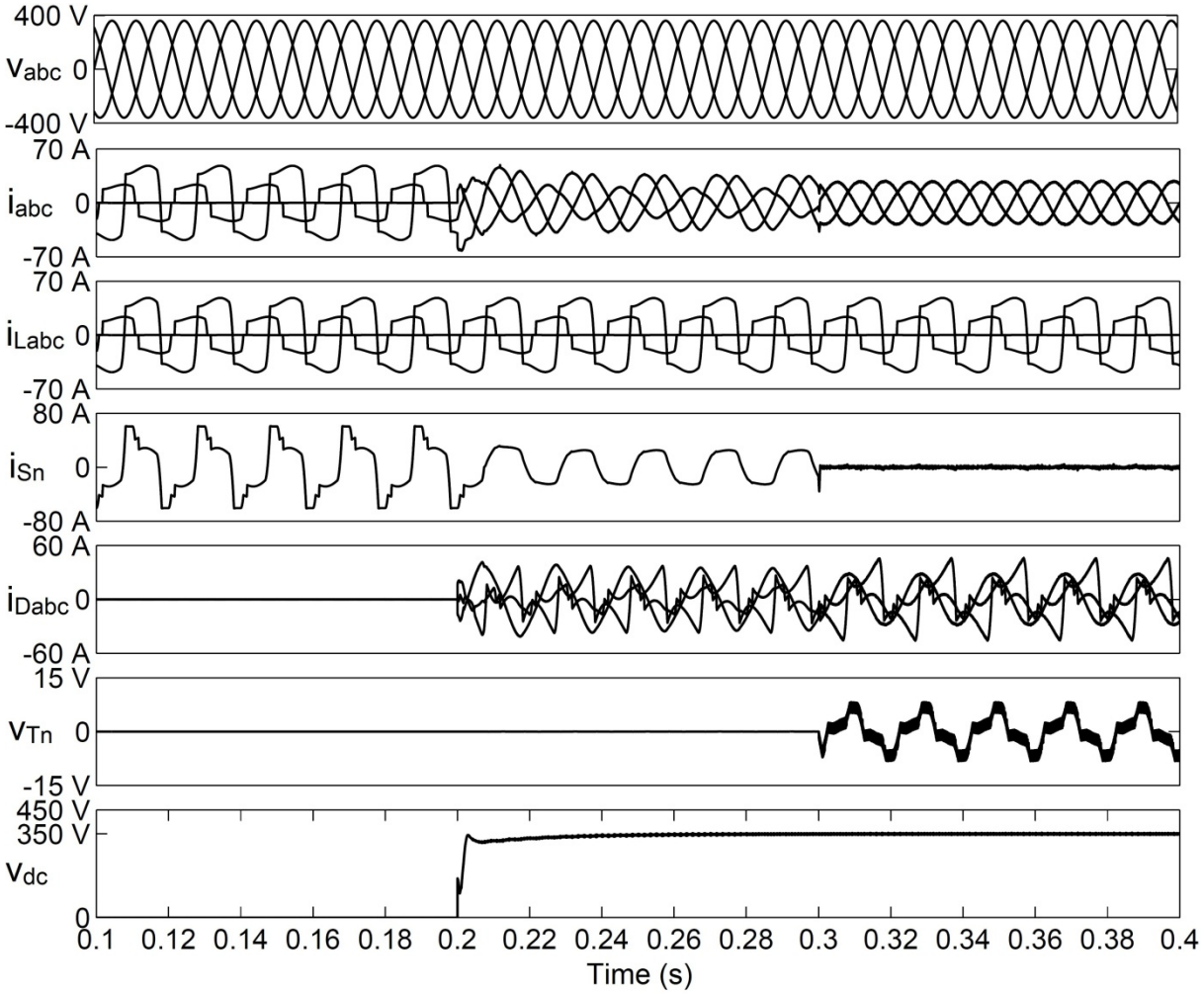
(c.1) Phase–*c* source current harmonic spectrum

Fig. 4.25: The performance of 3P4W hybrid D-STATCOM under ideal utility voltage conditions: simulated waveforms and harmonic spectra of load and source currents.

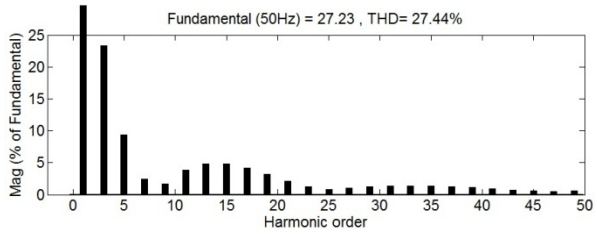
4.4.5.2 Performance under Ideal Utility Voltage with Single-phase Loads

The simulation results of the 3P4W distribution power system with only single-phase reactive/non-linear loads under ideal utility voltage conditions are given in Fig. 4.26. From Fig. 4.26, it can be observed that, before compensation with 3P4W hybrid D-STATCOM, the three-phase load current rms values are 19.9 A, 42.0 A and 0 A and their corresponding THD values are 27.44%, 33.31% and 0.00% respectively for the three phases. At t = 0.2 sec., when only T-connected transformer and 3P3W D-STATCOM are acting as compensators, the source neutral current is reduced from 39.1 A rms to 20.9 A rms (25.2 A peak) only. The observed source phase current %THD values are 11.66%, 4.78% and 7.65% for phase–*a*, phase–*b* and phase–*c* respectively. As in the earlier cases, the %THD values of source phase currents are reduced to a large extent but they still have small amounts of zero-sequence harmonic currents.

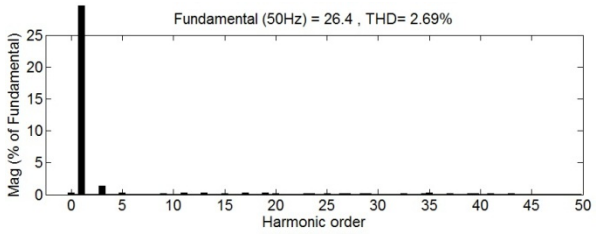
However, when the single-phase APF is switched-on, the compensator almost completely eliminated the source neutral current and the source phase currents become almost balanced (18.7 A, 19.9 A and 19.1 A rms for phase–*a*, phase–*b* and phase–*c* respectively). The THD values of source phase currents are reduced to 2.69%, 2.86% and 2.19% for phase–*a*, phase–*b* and phase–*c* respectively. The peak value of v_{Tn} is less than 8 V and the maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 17 V.



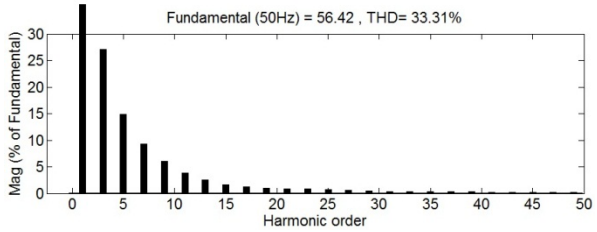
(a) Simulated waveforms



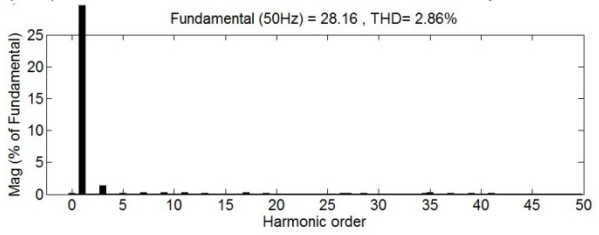
(b.1) Phase–*a* load current harmonic spectrum



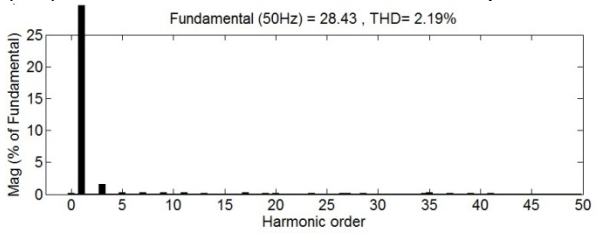
(c.1) Phase–*a* source current harmonic spectrum



(b.2) Phase–*b* load current harmonic spectrum



(c.2) Phase–*b* source current harmonic spectrum



(c.3) Phase–*c* source current harmonic spectrum

Fig. 4.26: The performance of 3P4W hybrid D-STATCOM under ideal utility voltage conditions with single-phase loads only: simulated waveforms and harmonic spectra of load and source currents.

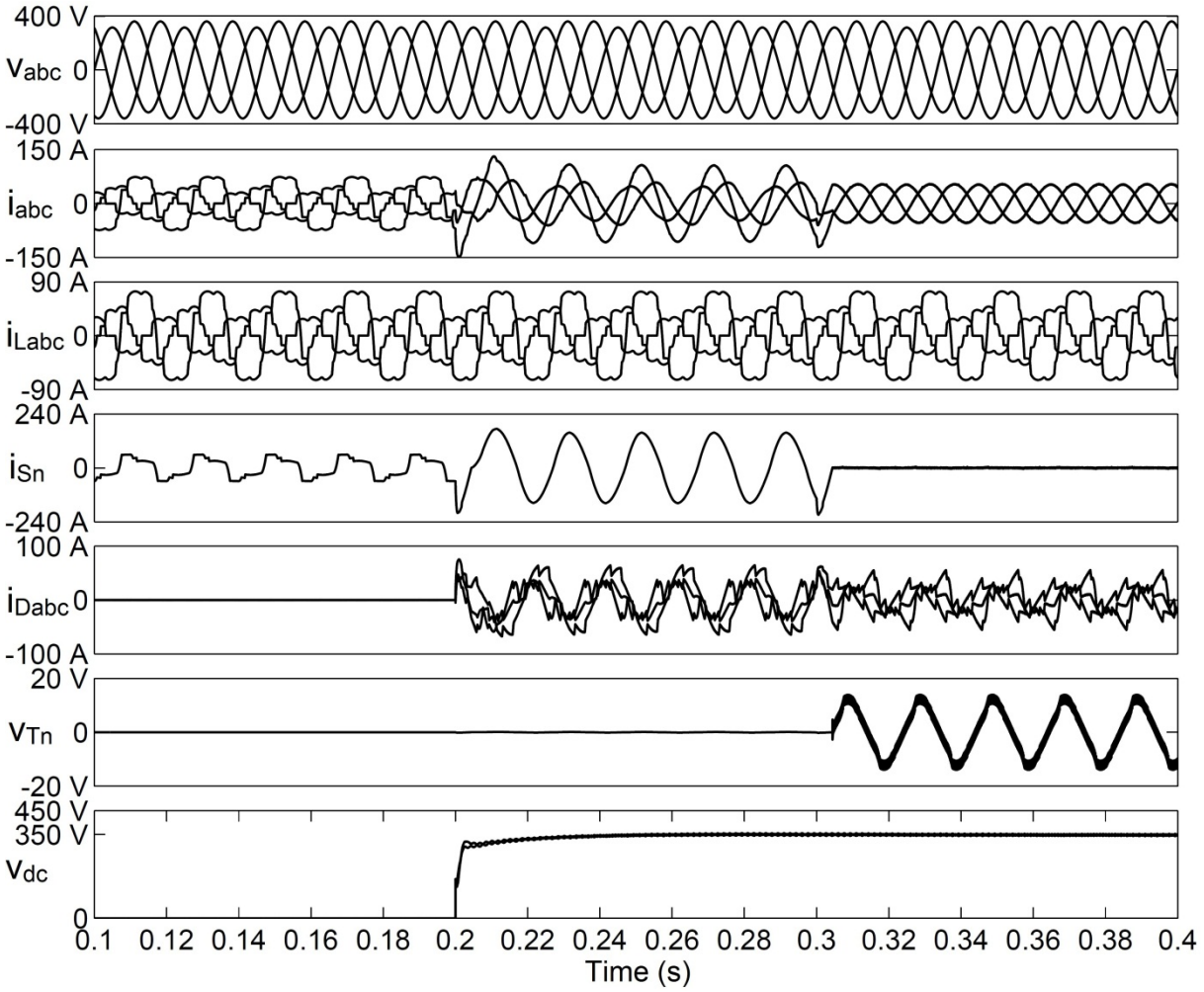
4.4.5.3 Performance under Unbalanced Utility Voltage Conditions

In order to study the efficacy of the compensator in improving the performance under unbalanced utility voltage conditions, both amplitude unbalance (10% voltage sag in phase–*a*) and phase-angle unbalance (0°, –110° and 120° for phase–*a*, phase–*b* and phase–*c* respectively) are introduced in the utility voltage. Fig. 4.27 show the simulation results under this condition with the single-phase and three-phase loads given in Table 4.4.

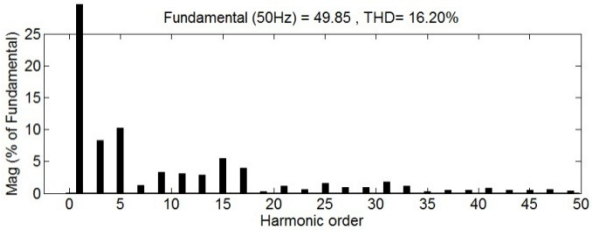
It can be observed from Fig. 4.27 that, before compensation with 3P4W hybrid D-STATCOM, the three-phase load current rms values are 35.7 A, 61.7 A and 23.0 A and their corresponding THD values are 16.20%, 20.90% and 24.17% respectively for the three phases. At t = 0.2 sec., when only T-connected transformer and 3P3W D-STATCOM are acting as compensators, the source neutral current is increased from 41.3 A rms to 111.0 A rms (157.2 A peak), due to the presence of zero-sequence voltage in the utility. The source phase currents after compensation are observed to be unbalanced and the THD values are 5.13%, 3.83% and 5.62% for phase–*a*, phase–*b* and phase–*c* respectively. In this case also, the %THD values of source phase currents are reduced to a large extent but they still have small amounts of zero-sequence harmonic currents.

Therefore, the source phase currents magnitudes are increased and the unbalance and distortions still exist. But, when the single-phase APF is switched-on, the compensator almost completely eliminates the source neutral current and the source phase currents become almost balanced (36.9 A, 38.3 A and 38.2 A rms for phase–*a*, phase–*b* and phase–*c* respectively) and in phase with their respective voltage waveform. The THD values of source phase currents are reduced to 1.33%, 1.52% and 1.41% for phase–*a*, phase–*b* and phase–*c* respectively. The maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 22 V. It is further observed that the peak value of v_{Tn} is increased to 16 V. As the value is still reasonably low, it ensures a low VA rating of the single-phase inverter. However, with increased amount of unbalance, the peak value of v_{Tn} further increases. Under these conditions, the single-phase APF must be protected against over-voltages.

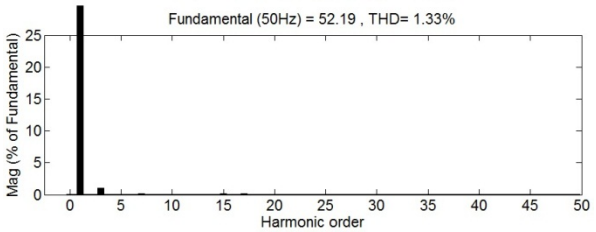
The relation between the amount of unbalance and the peak value of v_{Tn} is shown in Fig. 4.28. From Fig. 4.28, it is observed that the peak value of v_{Tn} increases with increasing VUF. Hence, under stringent unbalanced voltage conditions, the single-phase APF must be protected against over-voltages.



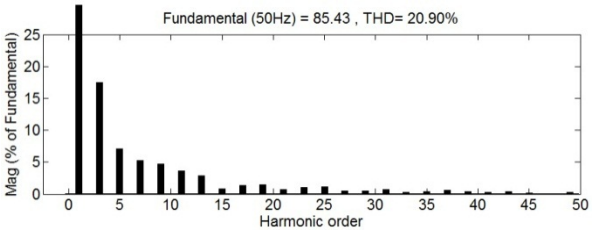
(a) Simulated waveforms



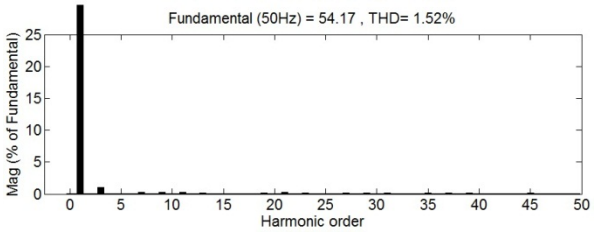
(b.1) Phase–*a* load current harmonic spectrum



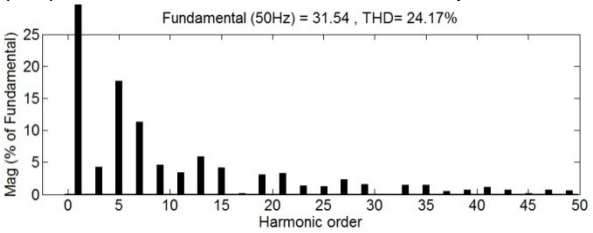
(c.1) Phase–*a* source current harmonic spectrum



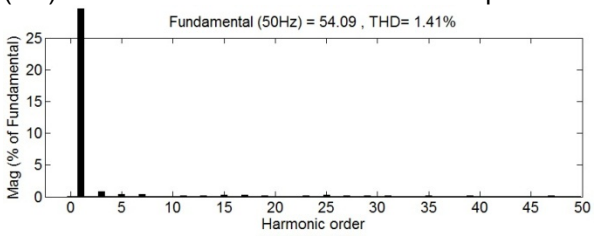
(b.2) Phase–*b* load current harmonic spectrum



(c.2) Phase–*b* source current harmonic spectrum



(b.3) Phase–*c* load current harmonic spectrum



(c.3) Phase–*c* source current harmonic spectrum

Fig. 4.27: The performance of 3P4W hybrid D-STATCOM under unbalanced utility voltage conditions: simulated waveforms and harmonic spectra of load and source currents.

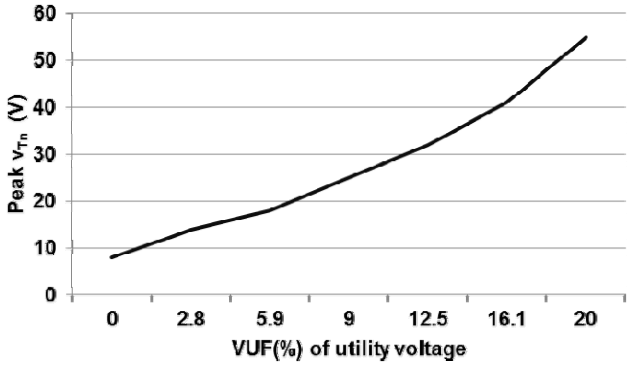


Fig. 4.28: The relation between peak value of v_{Tn} and % VUF of utility voltage.

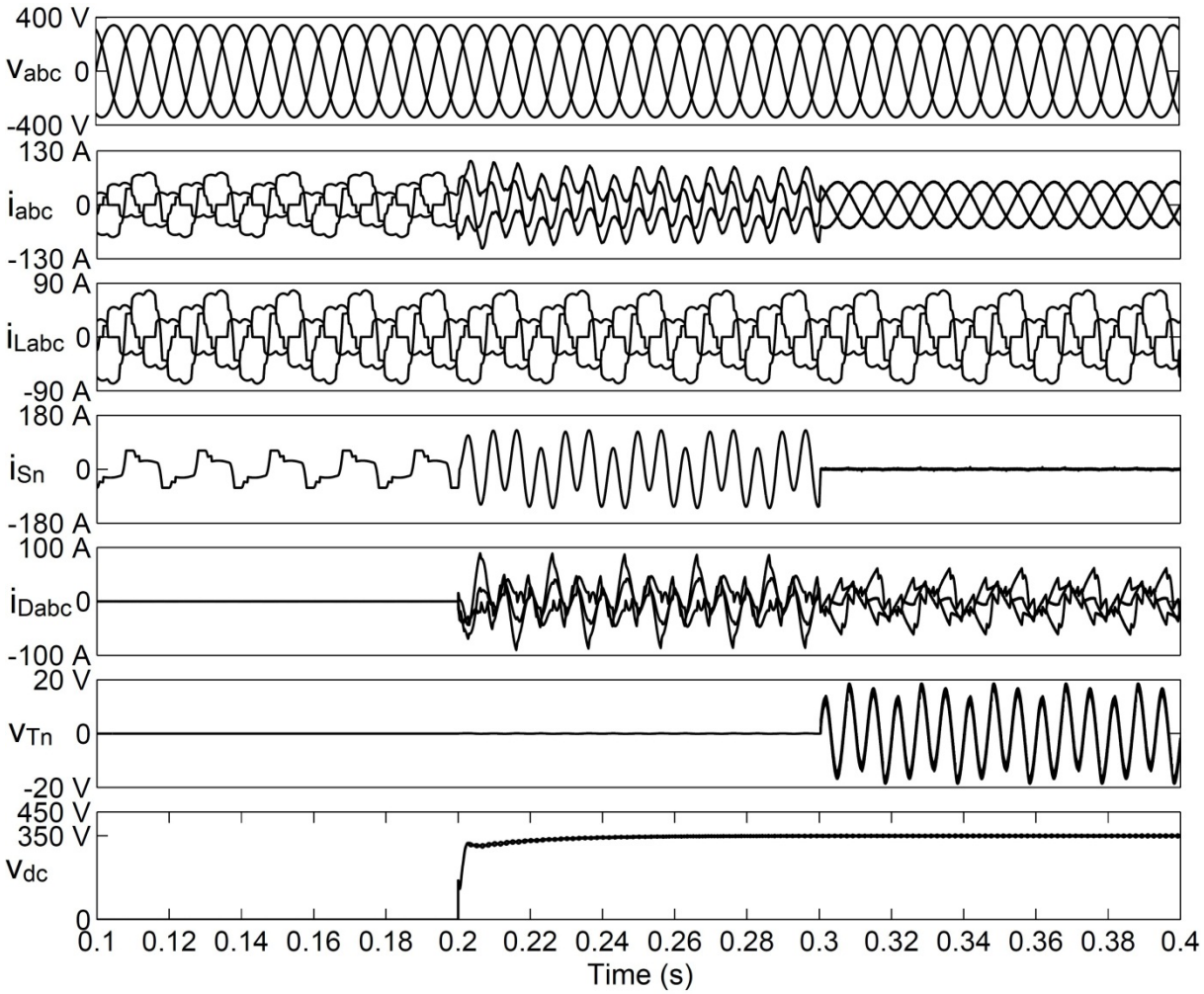
4.4.5.4 Performance under Distorted Utility Voltage Conditions

To verify the efficacy of the compensator in improving the performance under distorted utility voltage conditions, a 5% 3rd order harmonic component is introduced in the utility voltages. Fig. 4.29 show the simulation results under this condition with the single-phase and three-phase loads given in Table 4.4.

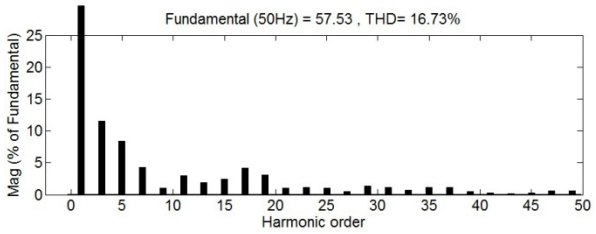
It can be observed from Fig. 4.29 that, before compensation with 3P4W hybrid D-STATCOM, the three-phase load current rms values are 41.2 A, 63.0 A and 22.3 A and their corresponding THD values are 16.73%, 21.37% and 28.86% respectively for the three phases. At t = 0.2 sec., when only T-connected transformer and 3P3W D-STATCOM are acting as compensators, the source neutral current is increased from 40.0 A rms to 81.6 A rms (129.8 A peak), due to the presence of zero-sequence voltage in the utility. The source phase currents after compensation are observed to be unbalanced and the THD values are 81.12%, 67.51% and 63.60% for phase–*a*, phase–*b* and phase–*c* respectively. As in the earlier cases, the huge enhancement of source phase current %THDs is due to the circulation of large zero-sequence current between source and T-connected transformer which is caused by the zero-sequence voltage in the utility. This current is not being compensated by the 3P3W D-STATCOM.

However, when the single-phase APF is switched-on, the compensator almost completely eliminates the source neutral current and the source phase currents become almost balanced (38.7 A, 39.8 A and 40.1 A rms for phase–*a*, phase–*b* and phase–*c* respectively) and in phase with their respective voltage waveform. The THD values of source phase currents are reduced to 1.55%, 1.69% and 1.68% for phase–*a*, phase–*b* and phase–*c* respectively. The maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 20 V.

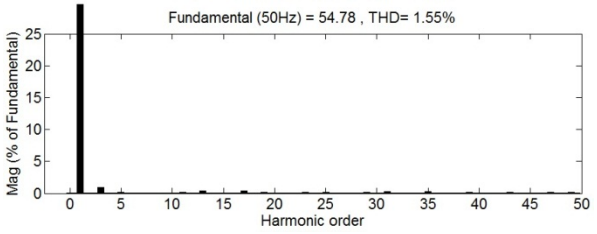
It is further observed that the peak value of v_{Tn} is increased to 19 V and still ensures a low VA rating of the single-phase inverter. However, with increased amount of distortion in utility voltage, the peak value of v_{Tn} further increases.



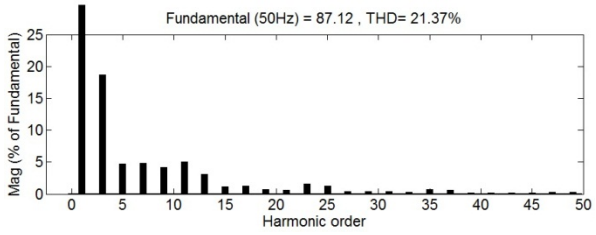
(a) Simulated waveforms



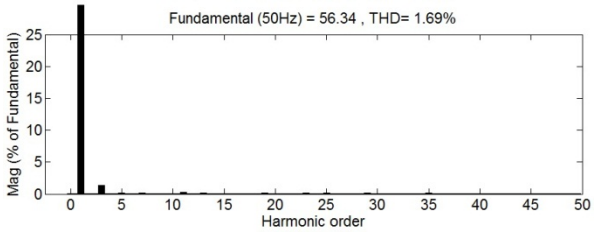
(b.1) Phase–*a* load current harmonic spectrum



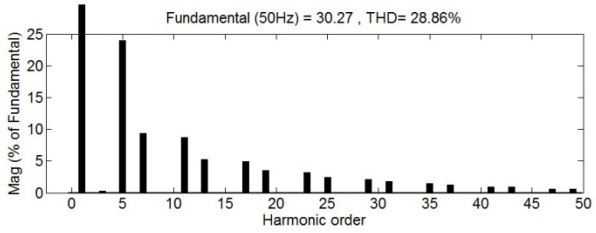
(c.1) Phase–*a* source current harmonic spectrum



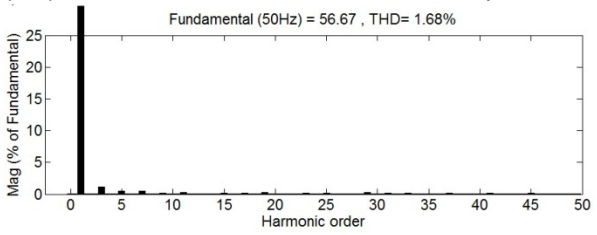
(b.2) Phase–*b* load current harmonic spectrum



(c.2) Phase–*b* source current harmonic spectrum



(b.3) Phase–*c* load current harmonic spectrum



(c.3) Phase–*c* source current harmonic spectrum

Fig. 4.29: The performance of 3P4W hybrid D-STATCOM under distorted utility voltage conditions: simulated waveforms and harmonic spectra of load and source currents.

The relation between zero-sequence harmonic voltage in the utility and peak value of v_{Tn} is shown in Fig. 4.30. In this simulation study, only 3rd order harmonic component is only considered as a zero-sequence harmonic voltage. From Fig. 4.30 it is observed that the peak value of v_{Tn} is increased with increasing amount of 3rd order harmonic component. Hence, under stringent distorted voltage conditions, the single-phase APF and T-connected transformer must be protected.

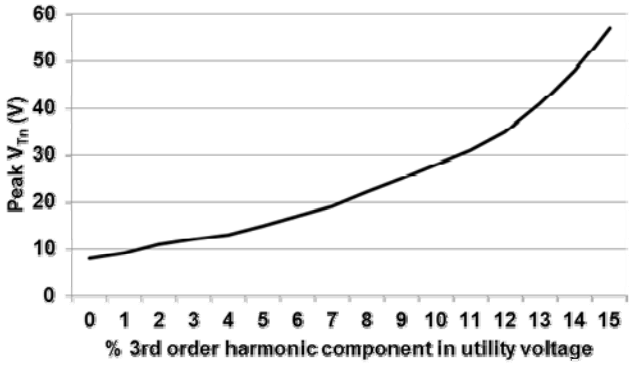
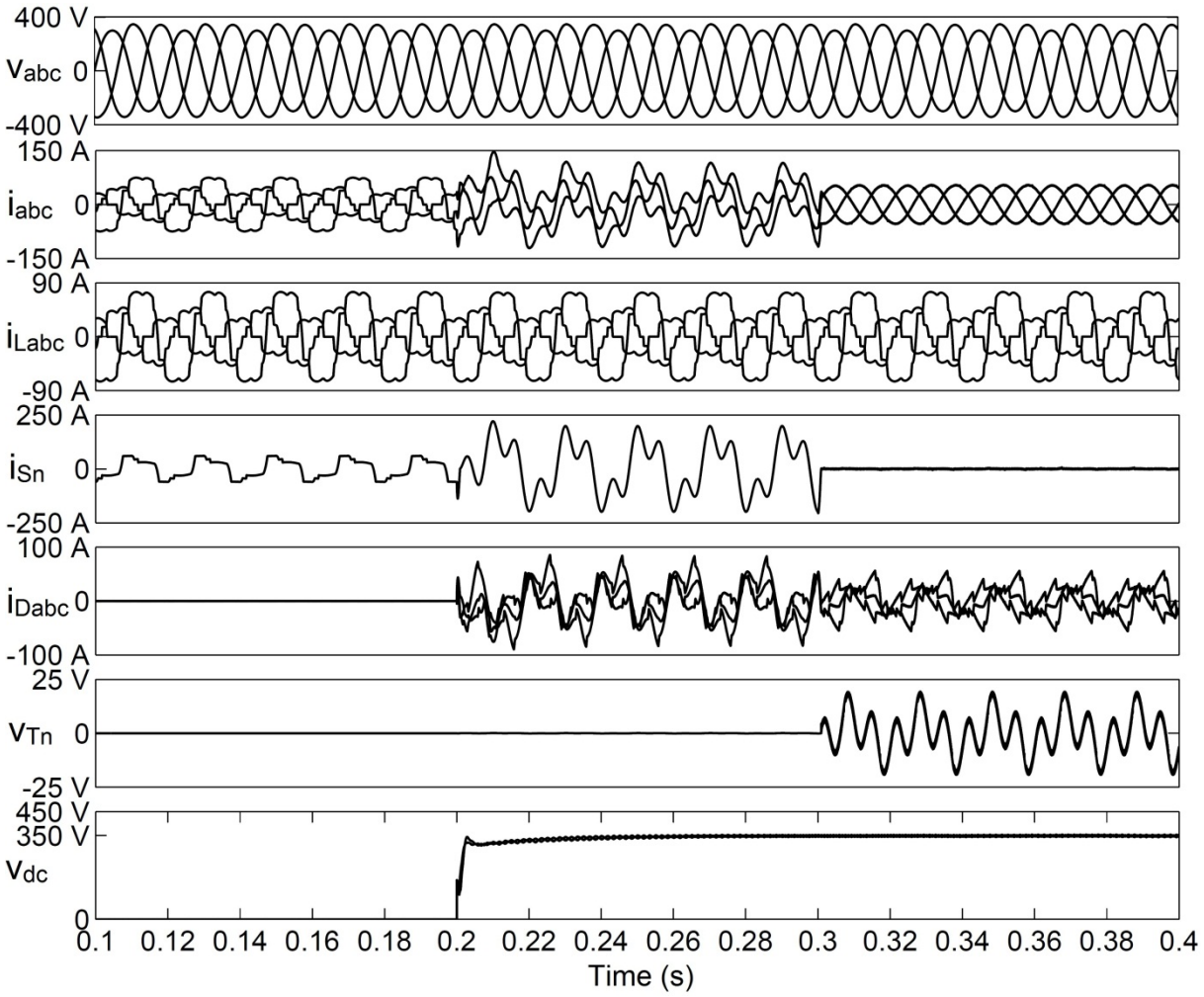


Fig. 4.30: The relation between peak value of v_{Tn} and % 3rd order harmonic component in utility voltage.

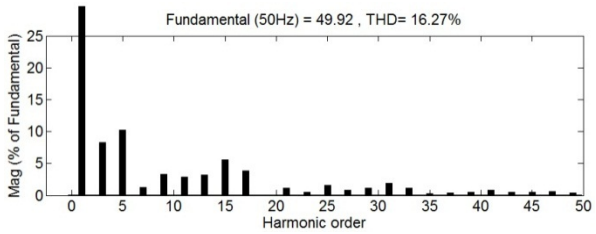
4.4.5.5 Performance under Non-ideal Utility Voltage Conditions

To verify the efficacy of the compensator in improving the performance under both distorted and unbalanced utility voltage conditions, simulation studies are carried out. Fig. 4.31 shows the simulation results under unbalanced (10% voltage sag in phase–*a* and phase-angle unbalance of 0°, –110° and 120°) and distorted (5% 3rd order harmonic component) utility voltage condition with the single-phase and three-phase loads given in Table 4.4.

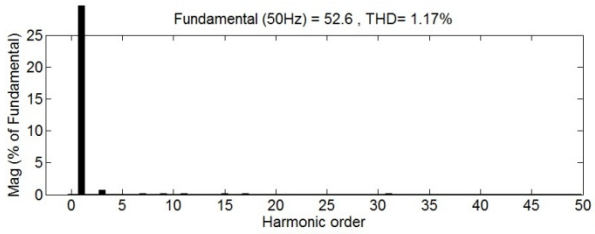
As shown in Fig. 4.31, before compensation with 3P4W hybrid D-STATCOM, the three-phase load current rms values are 35.8 A, 62.4 A and 23.0 A and their corresponding THD values are 16.27%, 21.51% and 24.16% respectively for the three phases. When only T-connected transformer and 3P3W D-STATCOM are acting as compensators, the source neutral current is increased from 42.0 A rms to 118.6 A rms (198.9 A peak), due to the presence of high zero-sequence voltage in the utility. The source phase currents after compensation are observed to be unbalanced and the THD values are 70.74%, 28.63% and 51.06% for phase–*a*, phase–*b* and phase–*c* respectively. The huge enhancement of source phase current %THDs is due to the circulation of large amount of zero-sequence current between source and T-connected transformer. However, when the single-phase APF is switched-on, the compensator almost completely eliminates the source neutral current and the source phase currents become almost balanced (37.2 A, 38.6 A and 38.5 A rms for phase–*a*, phase–*b* and phase–*c* respectively) and in phase with their respective voltage waveform. The THD values of source phase currents are reduced to 1.17%, 1.71% and 1.66% for phase–*a*, phase–*b* and phase–*c* respectively.



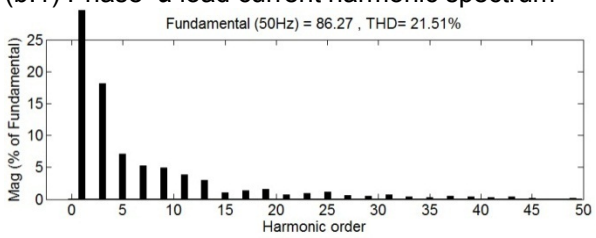
(a) Simulated waveforms



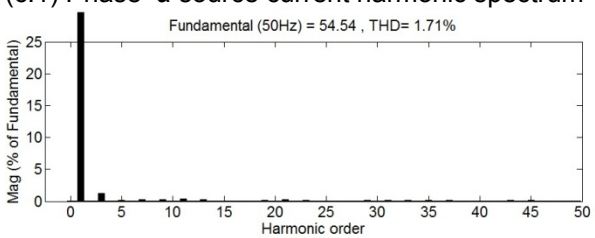
(b.1) Phase–*a* load current harmonic spectrum



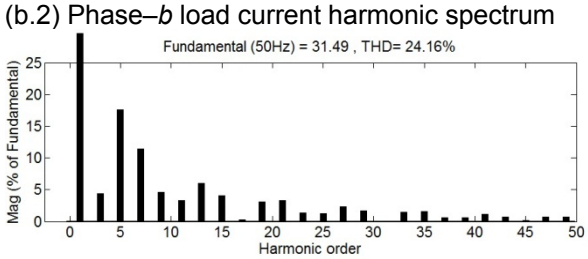
(c.1) Phase–*a* source current harmonic spectrum



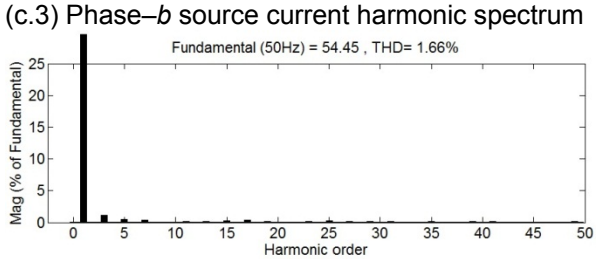
(b.2) Phase–*b* load current harmonic spectrum



(c.3) Phase–*b* source current harmonic spectrum



(b.3) Phase–*c* load current harmonic spectrum



(c.3) Phase–*c* source current harmonic spectrum

Fig. 4.31: The performance of 3P4W hybrid D-STATCOM under non-ideal utility voltage conditions: simulated waveforms and harmonic spectra of load and source currents.

The maximum value of peak-to-peak ripple in the dc voltage of each H-bridge cell is around 19 V, which ensures the effectiveness of the dc voltage controller with distorted/unbalanced utility voltage conditions also. It is observed that the peak value of v_{Tn} further increased to 23 V. However, with increased amount of distortion/unbalance in utility voltage, the peak value of v_{Tn} is further increases.

4.5 Comparison of 3P4W D-STATCOMs

The comparison of VA rating, simulation case studies and performance of different 3P4W compensators are given in this section.

4.5.1 Rating Comparison

The VA rating of the overall compensator is equal to the sum of the VA ratings of 3P3W D-STATCOM and single-phase APF. The procedures for calculation of rating of single-phase APF and 3P3W D-STATCOM are given below:

4.5.1.1 Rating of the Single-phase APF

The VA rating of the single-phase inverter of the APF is calculated by multiplying the peak compensating current and the peak voltage. Since the entire load neutral current is diverted to the APF, the current rating of the inverter is equal to the peak load neutral current ($I_{Ln-\text{peak}}$). The peak voltage rating of the inverter switches is equal to the dc bus voltage ($V_{dc,APF}$). Therefore, the VA rating of the single-phase inverter is calculated as:

$$VA_{APF} = I_{Ln-peak} * V_{dc,APF} \tag{4.22}$$

4.5.1.2 Rating of the 3P3W D-STATCOM

The VA rating of the three-phase inverter of the 3P3W D-STATCOM is calculated by multiplying the peak compensating current and the peak voltage (equal to the dc bus voltage of D-STATCOM).

Table 4.5 gives the comparison of VA ratings of 3P4W hybrid D-STATCOM with the rating of the compensators given in [74-76]. It is assumed that the load contains only three harmonics (n = 3, 5 and 7), and their peak individual magnitudes are 100 A, 30 A and 20 A respectively. From Table 4.5, it can be observed that a considerable reduction in the overall rating of the compensator is achieved with 3P4W hybrid D-STATCOMs.

Table 4.5: Comparison of rating of three-phase, four-wire D-STATCOMs.

Parameter	Three H-bridge topology	Capacitor midpoint topology	Four-leg topology	Proposed Hybrid D-STATCOMs
Peak compensating current of D-STATCOM (A)	150	150	150	50
DC bus voltage of D-STATCOM (V)	405	700	610	700
Rating of D-STATCOM (VA)	60750	105000	91500	35000
Peak compensating current of single-phase APF (A)	0	0	0	100
DC bus voltage of single-phase APF (V)	0	0	0	25
Rating of single-phase APF (VA)	0	0	0	2500
Total rating (VA)	**60750**	**105000**	**91500**	**37500**

4.5.2 Comparison of Simulation Studies

The simulation results of various case studies presented for both 3P4W hybrid D-STATCOM topologies are summarised in Table 4.6. From this table it can be observed that the both topologies have an improved performance under unbalanced/distorted source voltage conditions. In both schemes, when switch *S* closed, the zigzag transformer based scheme has reduced the source neutral current to a large extent than the scheme using T-connected transformer. This is because the zero-sequence impedance of zigzag transformer is less than the zero-sequence impedance of T-connected transformer of the same rating [56]. But, when switch *S* open, i.e. with the operation single-phase APF, in both schemes the compensation characteristics are almost identical, therefore, a special design of transformer with low zero-sequence impedance is not necessary.

Table 4.6: Comparison of simulation results of 3P4W hybrid D-STATCOMs

Parameter	Zigzag-delta transformer based topology (Fig. 4.4)					T-connected transformer based topology (Fig. 4.20)				
	Case 1	Case 2	Case 3	Case 4	Case 5	Case 1	Case 2	Case 3	Case 4	Case 5
i_{La} (A, rms)	41.1	19.9	35.7	41.2	35.8	41.1	19.9	35.7	41.2	35.8
i_{Lb} (A, rms)	62.3	42.0	61.7	63.0	62.4	62.3	42.0	61.7	63.0	62.4
i_{Lc} (A, rms)	22.3	0.0	23.0	22.3	23.0	22.3	0.0	23.0	22.3	23.0
%THD of i_{La}	16.39	27.44	16.20	16.73	16.27	16.39	27.44	16.20	16.73	16.27
%THD of i_{Lb}	20.43	33.31	20.90	21.37	21.51	20.43	33.31	20.90	21.37	21.51
%THD of i_{Lc}	28.85	0.00	24.17	28.86	24.16	28.85	0.00	24.17	28.86	24.16
i_{Ln} (A, rms)	39.0	39.1	41.3	40.0	42.0	39.0	39.1	41.3	40.0	42.0
i_{Ln} (A, peak)	61.0	61.0	59.0	62.4	60.5	61.0	61.0	59.0	62.4	60.5
%THD of i_{Ln}	48.83	47.91	42.05	49.84	43.31	48.83	47.91	42.05	49.84	43.31
i_{Sa} (A, rms)	38.4	18.7	36.9	38.8	37.2	38.4	18.7	36.9	38.7	37.2
i_{Sb} (A, rms)	38.8	19.3	37.7	39.2	38.0	39.5	19.9	38.3	39.8	38.6
i_{Sc} (A, rms)	38.3	18.6	36.7	38.6	36.9	39.7	19.1	38.2	40.1	38.5
%THD of i_{Sa}	1.63	2.67	1.36	1.58	1.14	1.65	2.69	1.33	1.55	1.17
%THD of i_{Sb}	1.49	2.76	1.51	1.72	1.73	1.52	2.86	1.52	1.69	1.71
%THD of i_{Sc}	1.44	2.45	1.41	1.76	1.68	1.47	2.19	1.41	1.68	1.66
i_{Sn} (switch *S* closed) (A, rms)	17.18	17.3	115.6	84.4	120.4	20.8	20.9	111.0	81.6	118.6
i_{Sn} (switch *S* closed) (A, peak)	21.5	21.8	160	136.0	194.2	25.1	25.2	157.2	129.8	198.9
i_{Sn} (switch *S* open) (A, rms)	0.86	0.96	1.45	1.64	1.96	0.91	1.02	1.53	1.67	1.86
Peak v_{zn} or v_{Tn} (V)	7	8	15	17	21	8	8	16	19	23

Note: case 1: with ideal source voltage; case 2: ideal source voltage with single-phase loads only; case 3: with unbalanced source voltage; case 4: with distorted source voltage; case 5: with unbalanced/distorted source voltage

4.5.3 Performance comparison

The merits and demerits of transformer based topologies and 3P4W D-STATCOMs are given in Table 4.7. As can be seen from this table that, the proposed hybrid topologies are quite useful for reduction of neutral current due to its reduced rating, passive compensation, ruggedness, low cost, easy installation procedure and less complexity over active compensation techniques. The compensation characteristics of methods proposed in [51-53,

55] are strongly dependent on system impedance and utility voltage conditions. But, with the addition of single-phase APF, the compensation characteristics are improved under distorted/unbalanced utility conditions and independent of utility and zigzag transformer impedances.

Table 4.7: Comparison of three-phase, four-wire D-STATCOMs.

Features	**Type of solution**		
	3P3W D-STATCOM, zigzag (or T-connected) transformer and single-phase APF based solution	**3P3W D-STATCOM and zigzag (or T-connected) transformer based solution [51-53, 55]**	**Three-phase, four-wire D-STATCOMs [74-77]**
Basic principle of neutral current compensation	Single-phase APF forcibly circulates the neutral current to the load via the zigzag (or T-connected) transformer.	Zigzag (or T-connected) transformer provides a low impedance path for the zero-sequence currents to circulate between the load and the zigzag transformer.	Compensates by injecting equal-but-opposite compensating current.
Effectiveness of neutral current compensation	Complete compensation is possible	Compensates only zero-sequence harmonics	Complete compensation is possible
Operation under unbalanced and/or distorted utility voltage conditions	Improved performance under unbalance/distortion conditions.	Degrades and causes uneven raise of neutral and line currents.	Degrades (with proper design of the controller this problem can be alleviated to some extent).
Rating of the compensator	Very less	Very less	High
Robustness of the compensator	High because of passive compensation	High because of passive compensation	Low
Effect of location on compensating characteristics	Independent	Dependent	Independent
Effect of source impedance on compensating characteristics	Independent	Dependent	Independent
Buffer reactor (L_b)	Not required	Required	Not required
Cost of the compensator	Very less	Less	High
Application and topology selection	Suitable for high-voltage, medium to high-power applications.	Suitable for high-voltage, medium to high-power applications. Not suitable with unbalanced and/or distorted utilities voltages.	Suitable for low to medium-power applications.

4.6 Conclusion

In this chapter two reduced rating hybrid 3P4W D-STATCOM topologies are proposed for the simultaneous compensation of source current harmonics, reactive power, load balancing and neutral current compensation. In these two approaches, the overall rating of each compensator is reduced and simultaneously the performances of the compensators are improved under unbalanced/distorted utility voltage conditions.

Extensive simulation studies are presented to verify the efficacy of both topologies. The VA rating and performance comparison between transformer based topologies and 3P4W D-STATCOMs are also been presented to corroborate the superiority of the proposed topologies.

CHAPTER 5: SYSTEM DEVELOPMENT AND EXPERIMENTATION

The system hardware, dSPACE–DS1006 interfacing and experimentation for the laboratory prototype models of the five-level SSBC based D-STATCOM topologies for 3P3W and 3P4W systems are described in detail to validate the simulation results presented in previous chapters. Further, these experimental studies are validated with simulation results using the experimental parameters.

5.1 Introduction

To validate the viability and effectiveness of the carrier rotation techniques, 11 kV, 1 MVA 3P3W D-STATCOM and as well as 3P4W hybrid D-STATCOM arrangements, the following prototypes are developed in the laboratory.

1. Three-phase five-level SSBC based inverter.
2. Three-phase five-level SSBC based D-STATCOM.
3. A 3P4W hybrid D-STATCOM comprising of a zigzag-delta transformer, 3P3W D-STATCOM and shunt connected single-phase APF.

A three-phase downscaled SSBC based modular multilevel inverter rated at 100 V, 5 kVA is designed and developed to realise the above D-STATCOM topologies. However, for hardware implementation, it is important to use an appropriate cascade number for realising the prototype inverter.

The cascade number *N* equal to 5 is definitely the best choice in terms of exact downscaling of 11 kV and 1 MVA 3P3W D-STATCOM. However, owing to the practical limitations, an inverter with *N* equal to 2 is used in this work for realising the prototype inverter for the D-STATCOM topologies. It is important to note that the control algorithm developed in the earlier chapter is independent of cascade number *N*. With *N* equal to 2, the power circuit of the SSBC based inverter consists of 24 switching devices having same voltage and current ratings. These 24 switching devices are used to realise 6 H-bridge cells and each cell is equipped with a galvanically isolated and floating dc capacitor without any power source or circuit. These 6 H-bridge cells are used for the synthesis of three-phase inverter. As a result, it produces a five-level line-to-neutral (9-level line-to-line) voltage waveform. In experimental setup, IGBTs (IRG4PH40KD) are used as the switching devices for realising the inverter. The other hardware components as required for the operation of the experimental set-up such as pulse amplification circuit, isolation circuit, dead-band circuit, voltage and current sensor circuits, non-linear/reactive loads are designed and developed in the laboratory. The complete schematic diagram for the realisation of 3P3W D-STATCOM is shown in Fig. 5.1.

A Digital Signal Processor (DSP) DS1006 of dSPACE is used for the real-time simulation and implementation of control algorithm. By using the Real-Time Workshop (RTW) of MATLAB and Real-Time Interface (RTI) feature of dSPACE DS1006, the Simulink models of the various controllers of the prototypes are implemented. The control algorithm is

first designed in the MATLAB/Simulink software. The RTW of MATLAB generates the optimized C-code for real-time implementation. The interface between MATLAB/Simulink and Digital Signal Processor (DSP, DS1006 of dSPACE) allows the control algorithm to be run on the hardware. The master bit I/O is used to generate the required gate pulses and Analog to Digital Converters (ADCs) are used to interface the sensed line currents, supply voltages and dc-bus capacitor voltages. An opto-isolated interface board is also used to isolate the entire DSP master bit I/O.

The development of different hardware components as required for the operation of the hardware prototypes are discussed in the next section.

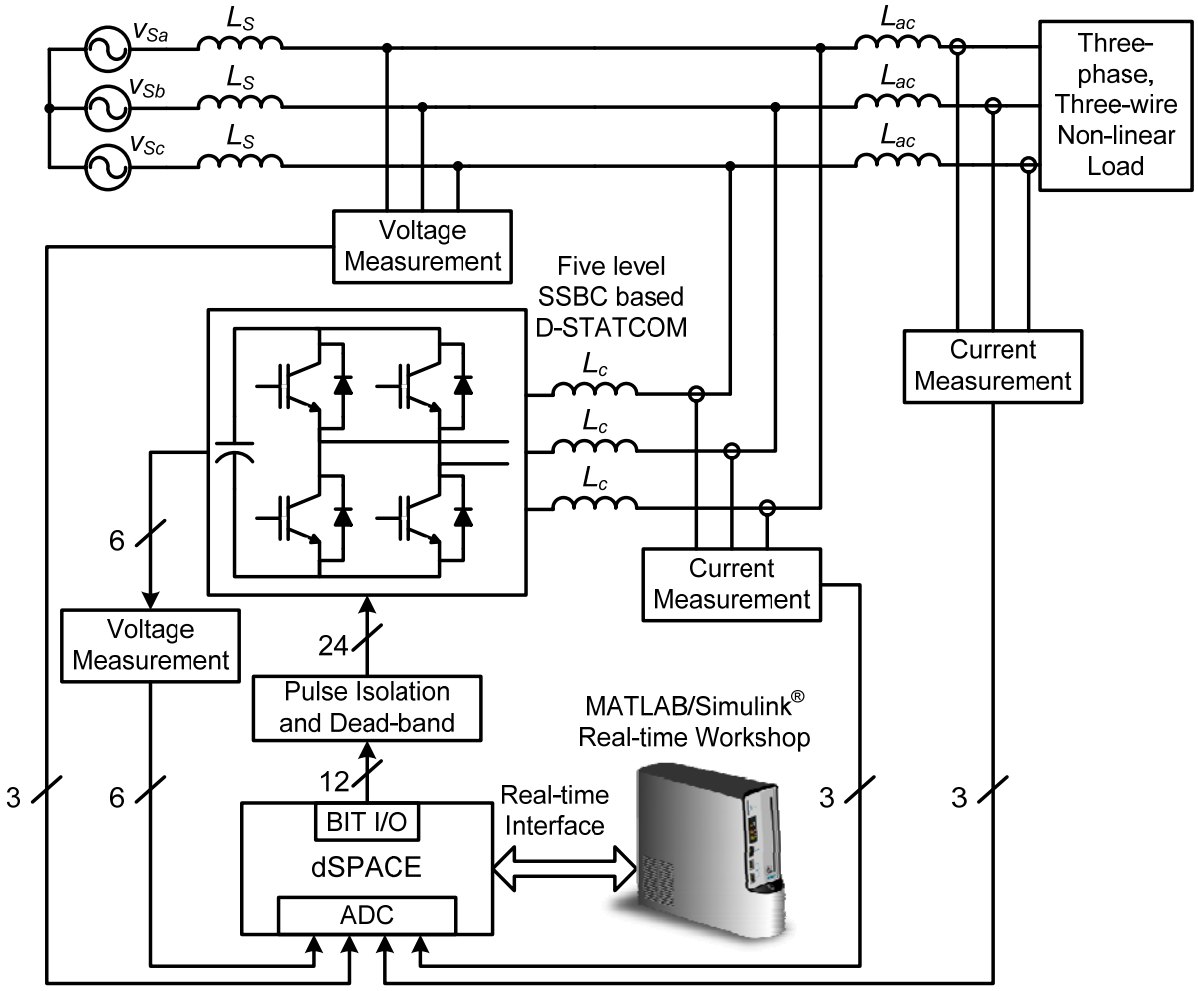


Fig. 5.1: Schematic diagram for hardware implementation of SSBC based D-STATCOM.

5.2 System Hardware

The developed experimental prototype is comprised of the following basic parts:

1. Power circuit of SSBC inverter
2. Measurement circuits
   - Load and D-STATCOM currents
   - Source and dc voltages of the H-bridge cells
3. System software

4. Control hardware
    - IGBT driver circuit
    - Buffer (isolation) circuit
    - Dead-band circuit

5.2.1 Power Circuit

A three-phase five-level SSBC based inverter with suitably designed coupling inductors (L_C) on its ac side and six capacitors on its dc side is developed. The structure of the three-phase inverter is shown in Fig. 5.2. It consists of 24 self-commutated power semiconductor switches with anti-parallel diodes. The switches are realized by the IGBTs (IRG4PH40KD). To protect each switching device, a suitably designed snubber circuit is connected across it. The snubber comprises of a parallel combination of a resistor and a capacitor connected across a Metal-Oxide Varistor (MOV). The devices are mounted on heat sinks to ensure proper heat dissipation. Various parameters and rating of passive components are designed as per the design criterion discussed in Chapter 3.

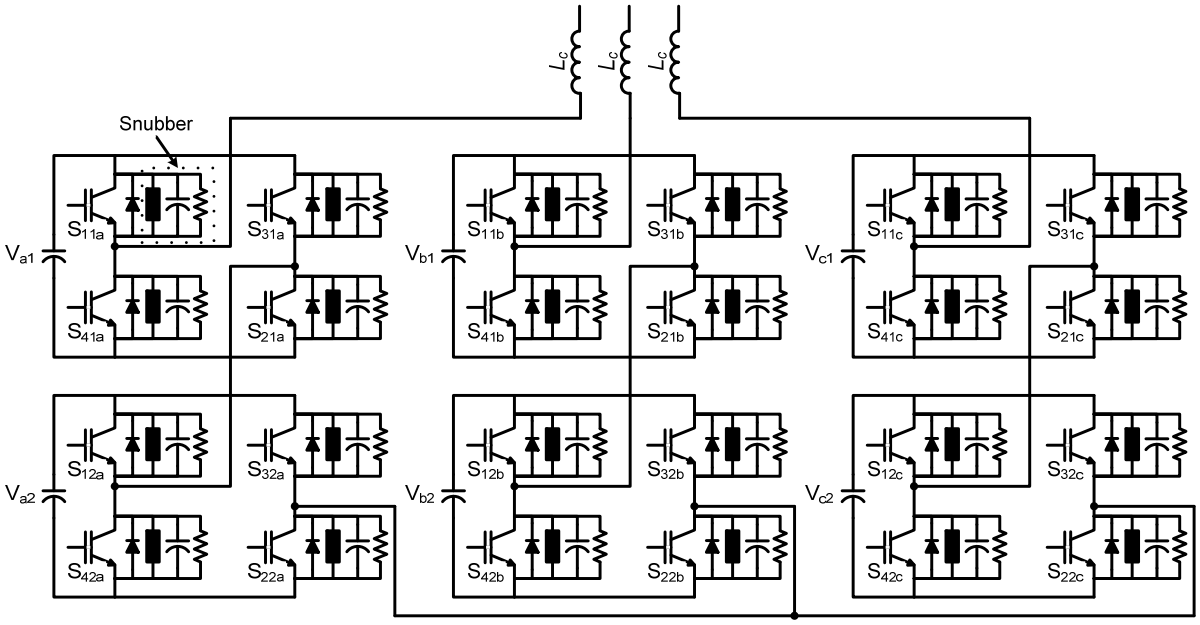


Fig. 5.2: Power circuit of five-level SSBC based D-STATCOM.

5.2.2 Measurement Circuits

For accurate and reliable operation of a system in closed loop, measurement of various system parameters and their conditioning is required. The measurement system must fulfil the following requirements:

- High accuracy
- Galvanic isolation with power circuit
- Linearity and fast response
- Ease of installation and operation

With the availability of Hall-effect current sensors and isolation amplifiers, these requirements are fulfilled to a large extent. In order to implement the control algorithm of D-STATCOM in closed loop, following signals are sensed.

1. Load currents, D-STATCOM currents and ac source voltages for reference current generation
2. DC voltages of the H-bridge cells (required for the operation of dc voltage regulator).

5.2.2.1 Sensing of AC Current

The ac source currents are sensed using the PCB-mounted Hall-effect current sensors (TELCON HTP25). The HTP25 is a closed loop Hall effect current transformer suitable for measuring currents up to 25 A. This device provides an output current into an external load resistance. These current sensors provide the galvanic isolation between the high-voltage power circuit and the low-voltage control circuit and require a nominal supply voltage of the range ±12V to ±15V. It has a transformation ratio of 1000:1 and thus, its output is scaled properly to obtain the desired value of measurement. The circuit diagram of the current sensing scheme is shown in Fig. 5.3.

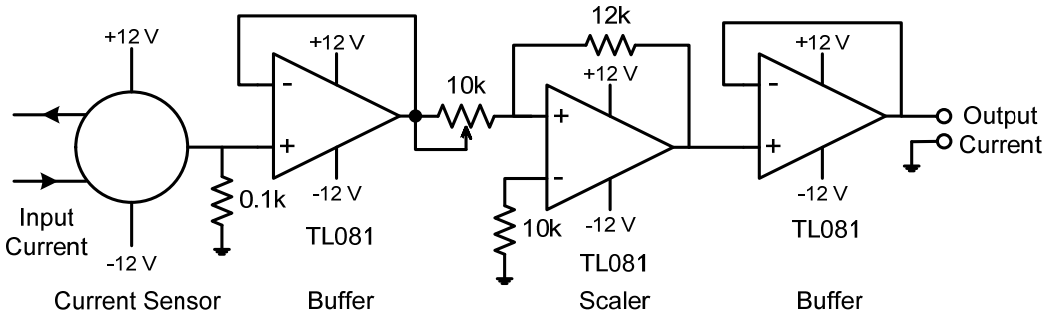


Fig. 5.3: AC current sensing circuit.

5.2.2.2 Sensing of Voltage

The voltages are normally sensed using isolation amplifiers and among them, AD202 is a general purpose, two-port, transformer-coupled isolation amplifier that can be used for measuring both ac and dc voltages. The other main features of the AD202 isolation amplifier are:

1. Small physical size
2. High accuracy
3. Low power consumption
4. Wide bandwidth
5. Excellent common-mode performance

This voltage sensor can sense voltages in the range of ±1 kV (peak) and it requires a nominal supply voltage range of ±12V to ±15V. Fig. 5.4 shows the circuit diagram for the voltage sensing scheme, which uses AD202 isolation amplifier. The voltage (ac or dc) to be

sensed is applied between the terminals 1 and 2 (across a voltage divider comprising of 100 kΩ and 1 kΩ) and the voltage input to the sensor is available at the pins 1 and 2 of AD202 via a resistance of 2.2 kΩ. The isolated sensed voltage is available at the output terminal 19 of AD202. The output of voltage sensor is scaled properly to meet the requirement of the control circuit and is fed to the dSPACE via its ADC channel for further processing.

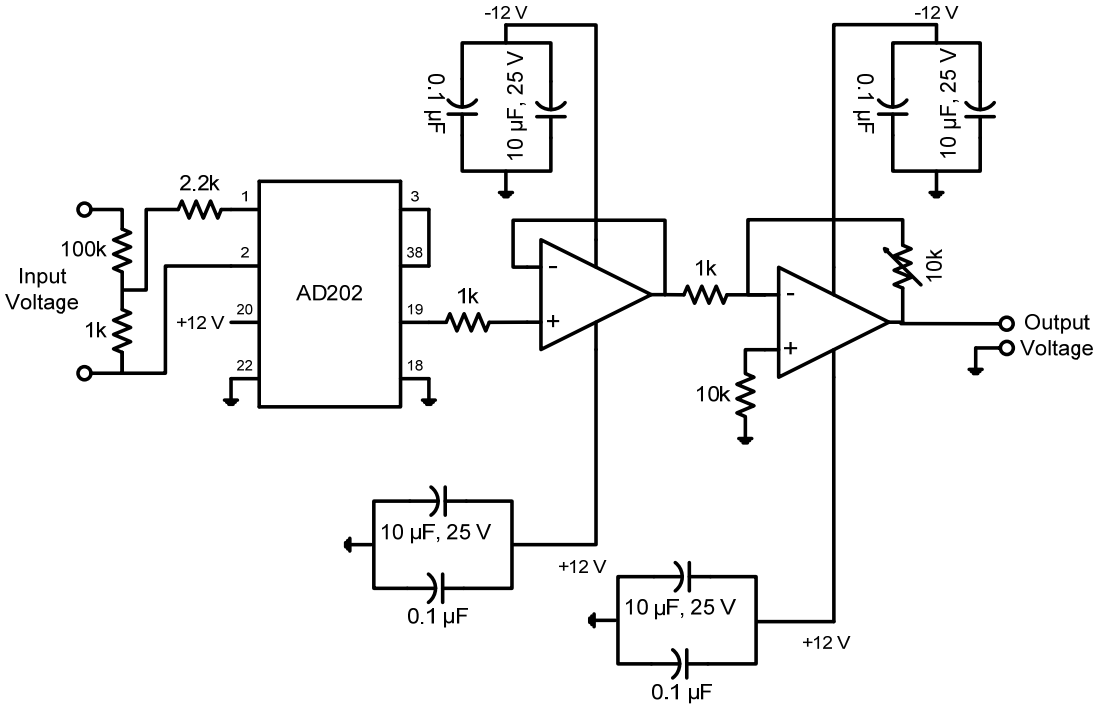


Fig. 5.4: AC/DC voltage sensing circuit.

5.2.3 System Software

Historically, control software was developed using assembly language. In recent years, industry began to adopt MATLAB/Simulink and Real-Time Workshop (RTW) platform based method, which provides a more systematic way to develop control software. Fig. 5.5 shows the Total Development Environment (TDE) of dSPACE and its major component blocks are explained as below:

- MATLAB is widely used as an interactive tool for modelling, analysis and visualization of systems, which itself contains more than 600 mathematical functions and supports additional toolboxes to make it more comprehensive.
- Simulink is a MATLAB add-on software that enables block diagram based modelling and analysis of linear, non-linear, discrete, continuous and hybrid systems.
- RTW is a Simulink add-on software that enables automatic C or ADA code generation from the Simulink model. The generated optimised code can be executed on PC, microcontrollers and signal processors.

- Real Time Interface (RTI) by add-on software of dSPACE provides block libraries for I/O hardware integration of DS1006 R&D controller and generates optimized code for master and slave processors of the board.
- The dSPACE's control desk is a software tool interfacing with real-time experimental setup and provides easy and flexible analysis, visualization, data acquisition and automation of the experimental setup. The major feature of real-time simulation is that the simulation has to be carried out as quickly as the real system would actually run, thus allowing to combine the simulation and the inverter (real plant).

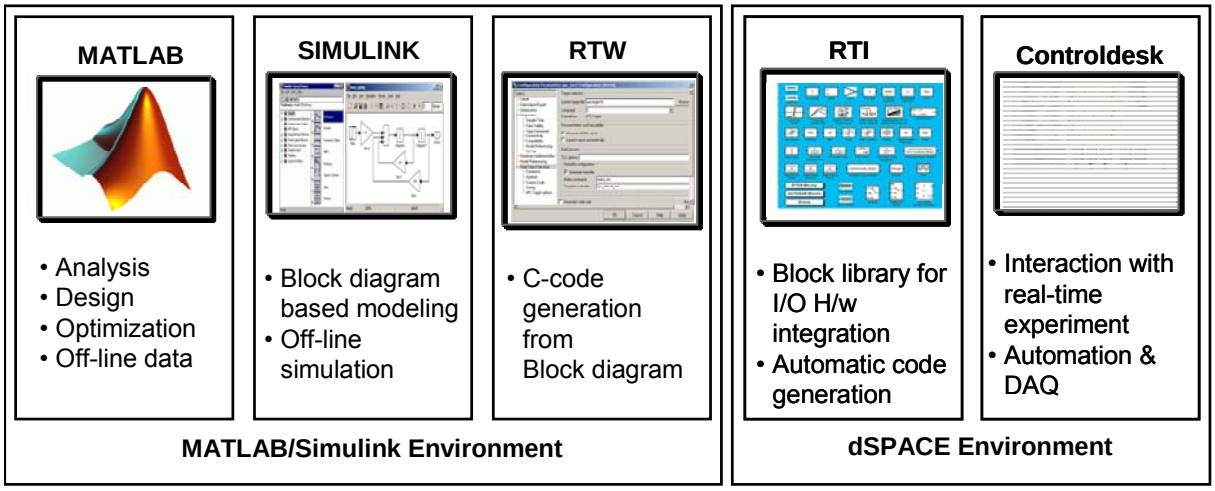


Fig. 5.5: Total development environment of dSPACE with MATLAB/Simulink.

The DSP DS1006 R&D controller board of dSPACE is a standard board that can be plugged into Peripheral Component Interconnect (PCI) slot of a desktop computer. The DS1006 is specially designed for the development of high-speed multivariable digital controllers and real-time simulations for various applications. It is a complete real-time control system based on an AMD Opteron™ processor running at 2.6 GHz. It has 256 MB DDR-400 SDRAM local memory for handling application and dynamic application data and 128 MB SDR SDRAM global memory for host data exchange. DS1006 R&D controller is a very good platform for the development of dSPACE prototype system for cost-sensitive RCP applications. It is used for the real-time simulation and implementation of the control algorithm in real-time.

The sensed ac and dc voltages are fed to the dSPACE Multi-I/O Board (DS2201) of DS!006 via the available ADC channels on its connector panel. In order to add an I/O block (such as ADCs and master bit I/Os in this case) to the Simulink model, the required block is dragged from the dSPACE I/O library and dropped into the Simulink model of the SSBC based D-STATCOM. In fact, adding a dSPACE I/O block to a Simulink model is almost like adding any Simulink block to the model. In this case, twelve master bit I/Os, configured in the output mode, are connected to the model for issuing twelve gating signals (and twelve complementary signals) to the IGBTs of SSBC. In addition, 20 ADCs are connected to the

model for giving the load current, D-STATCOM current, supply voltage and dc capacitor voltages as input to the DSP hardware.

For balanced three-phase systems, hardware requirement can be minimized by adding electrical quantities of two separate phases and from the resulting quantity, the corresponding value for the third phase is obtained. For example, the source line currents i_{Sa} and i_{Sb} are measured and the third line current i_{Sc} is obtained by $i_{Sc} = -\left(i_{Sa} + i_{Sb}\right)$. Similarly to sense three phase supply voltages and three load currents, two sensors are used in each case. For dc voltage regulator, only phase–*a* dc voltages of the H-bridge cells of SSBC are sensed and the total loss component is obtained by multiplying the phase–*a* loss component by three. The sensed signals are used for processing in the designed control algorithm. The vital aspect for real-time implementation is the generation of real-time code of the controller to link the host computer with the hardware. In dSPACE systems, Real-Time Interface (RTI) carries out this linking function. Together with RTW from the Mathworks®, it automatically generates the real-time code from Simulink models and implements this code on dSPACE real-time hardware. This saves the time and effort considerably as there is no need to manually convert the Simulink model into another language such as 'C'. RTI carries out necessary steps by the addition of the required dSPACE blocks (I/O interfaces) to the Simulink model. In other words, RTI is the interface between Simulink and various dSPACE platforms. It is basically the implementation software for single-board hardware and connects the Simulink control models to the I/O of the board. In the present case, the optimized C-code of the Simulink model of the control algorithm is automatically generated by the RTW of MATLAB in conjunction with RTI of dSPACE.

The generated code is then automatically downloaded into the dSPACE hardware where it is implemented in real-time and the gating signals are generated. The gating pulses for the power switches of converter are issued via the Master-bit I/Os available on the dSPACE board. The DS2201 Connector/LED combo panel provides easy-to-use connections between DS1006 board and the devices to be connected to it. The panel also provides an array of LEDs indicating the states of digital signals (gating pulses). The gating pulses are fed to various power devices driver circuits via isolation and dead-band circuits. Fig. 5.6 shows the schematic diagram of dSPACE-DS1006 board interfaced with the host computer and the real-world plant (power circuit of D-STATCOM). Sensed signals are fed to the ADCs and generated gating pulses are given at Master bit I/Os.

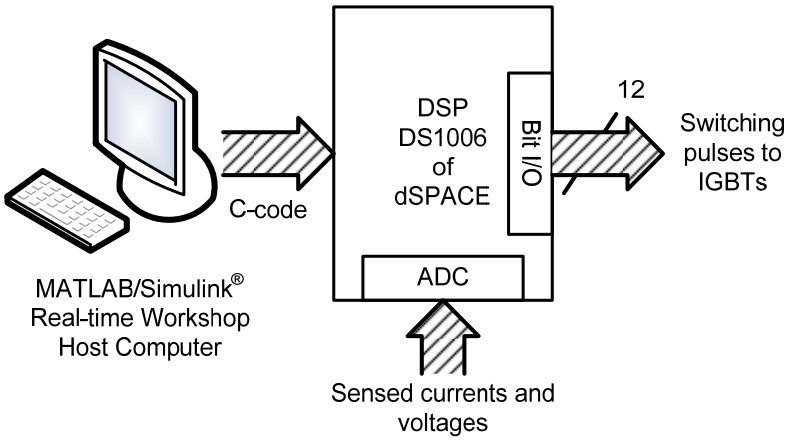


Fig. 5.6: DSP (dSPACE-DS1006) circuit board interfacing.

5.2.4 Control Hardware

The control algorithm is designed and built in MATLAB/Simulink software and the control pulses for 24 IGBTs (Here only 12 firing pulses are generated and remaining 12 are complementary of generated pulses) are generated by real-time simulation using the DSP of dSPACE. The optimized C-code of the Simulink model of control algorithm is generated with the help of (RTW of MATLAB. The RTW of MATLAB and the RTI of dSPACE result in the real-time simulation of the model. The control pulses are generated at various Master-bit I/Os of the dSPACE which are interfaced with the IGBT driver circuits through isolation and dead-band circuits. This ensures the necessary isolation of the dSPACE hardware from the power circuit that is required for its protection. Fig. 5.7 shows the basic schematic diagram of interfacing firing pulses from dSPACE board to switching devices of SSBC converter. In this figure the details of only the phase–*a* cluster of SSBC converter are shown. From Fig. 5.7, it can be observed that the following hardware circuits are required for interfacing the SSBC converter with dSPACE board.

1. Isolation circuit
2. Dead-band circuit
3. IGBT driver circuits

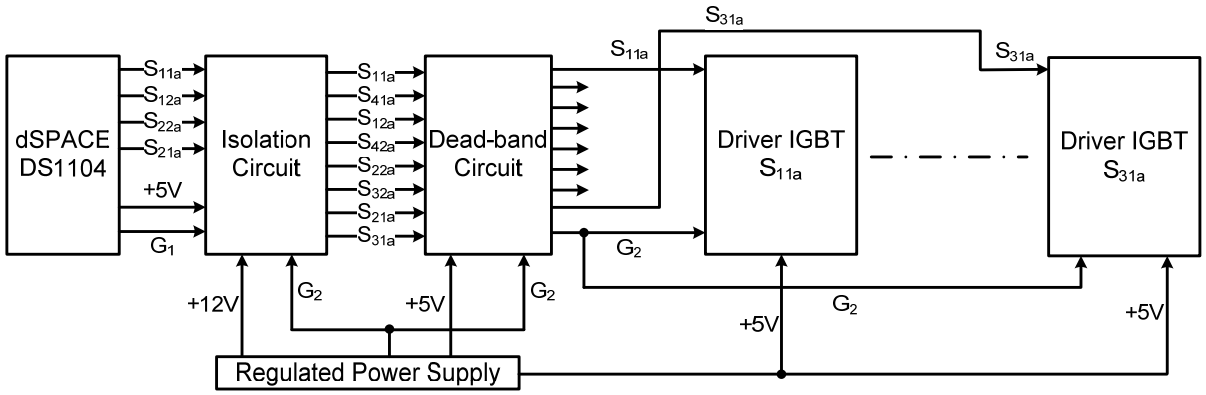


Fig. 5.7: Schematic diagram of interfacing firing pulses from dSPACE controller board to switching devices.

5.2.4.1 Isolation Circuit

An isolation circuit board is used for optical isolation of dSPACE hardware (Master-bit I/Os) from direct connection with the power circuit. Fig. 5.8 shows the circuit diagram of the isolation circuit between dSPACE and power devices of a H-bridge cell. Toshiba built opto-coupler chip (6N137) is used for optical isolation.

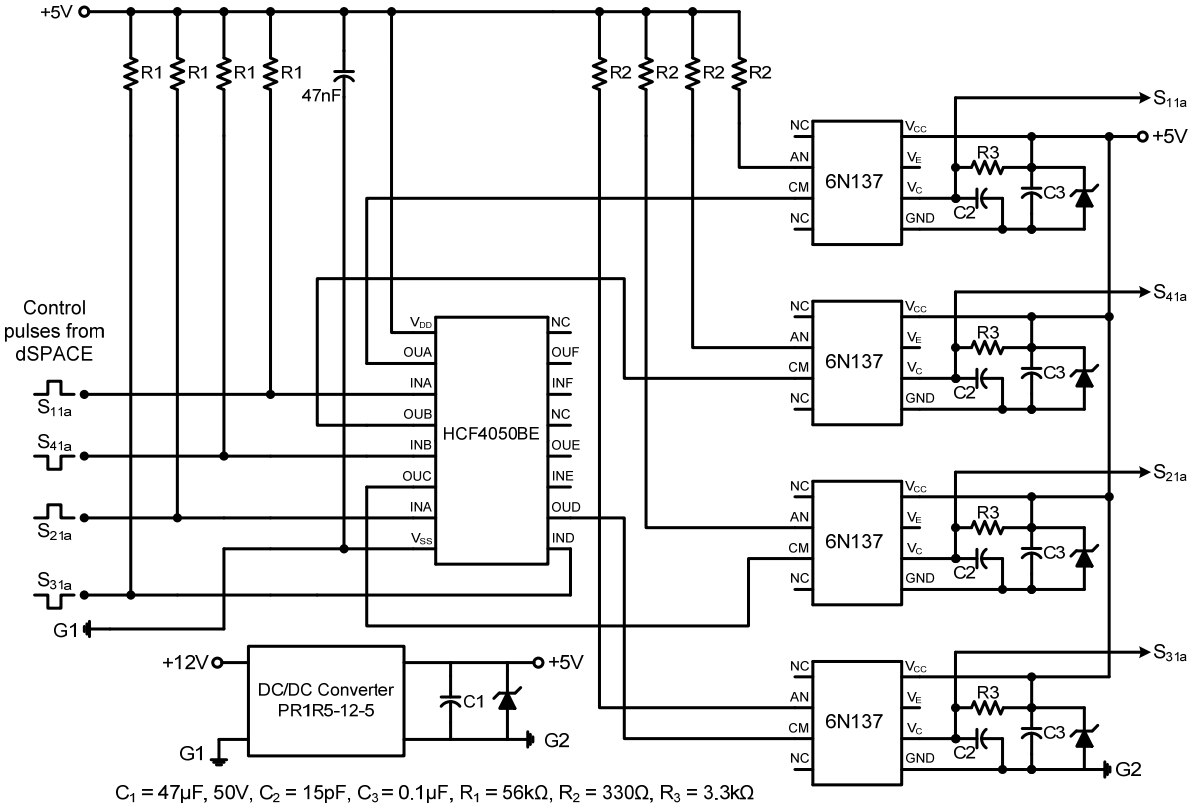


Fig. 5.8: Opto-isolation circuit for a H-bridge cell.

5.2.4.2 Dead-band Circuit

A dead-band (dead-time or delay) circuit is employed to provide a delay time (of about 1 μs) between the switching pulses to two complementary devices connected in same leg of an H-bridge cell. This is required to avoid the short circuit of devices in the same leg due to simultaneous conduction. The delay time between switches of the same leg of H-bridge cell is introduced by a *RC* integrator circuit as shown in Fig. 5.9.

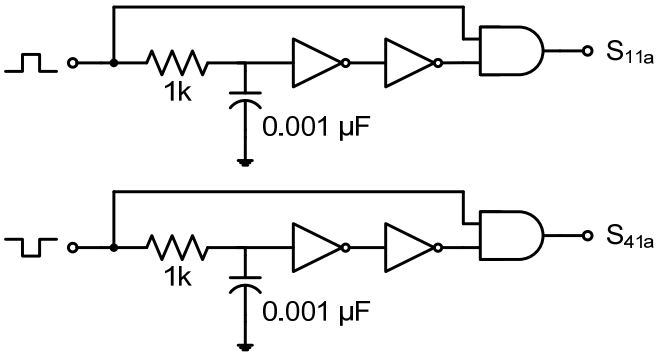


Fig. 5.9: Dead-band circuit for a phase-leg of a H-bridge cell.

An identical dead-band circuit are used for each leg of all H-bridge cells. The different switching signals obtained experimentally for semiconductor devices in the same leg of an H-bridge cell are shown in Fig. 5.10 with 1 μs delay. In Fig. 5.10, the top and bottom signals are for the switches S_{11a} and S_{41a} respectively.

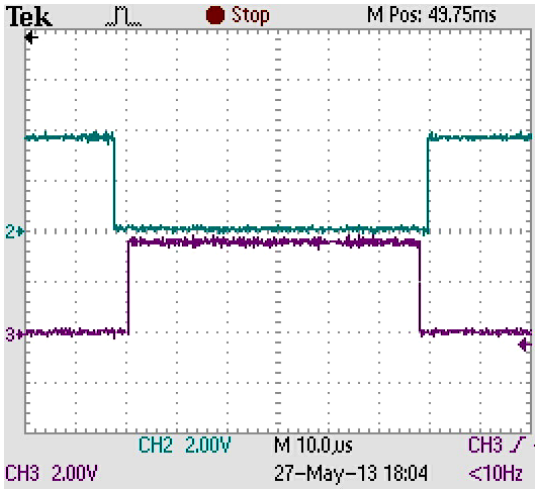


Fig. 5.10: Firing signals for the switches S_{11a} and S_{41a} with dead-band circuit.

5.2.4.3 IGBT Driver Circuits

The IGBT driver circuits are used for pulse amplification and isolation purposes. The IGBT driver circuits not only amplify the pulse signals for driving the devices but also provide an optical isolation. The driver circuit has special features such as fault protection and protection against the under-voltage lockout. HCPL-316J chip from Agilent Technologies is used as an IGBT driver chip. It can drive IGBTs up to 150 A at an applied voltage up to 1200 V. Fig. 5.11 shows the circuit diagram of the IGBT driver circuit. During normal operation, V_{out} (pin no. 11) of the HCPL-316J is controlled by either by VLN+ (pin no. 1) or VLN- (pin no. 2), with the IGBT collector-to-emitter voltage being monitored at D_{SAT} (pin no. 14). The FAULT output is high and the RESET input should be held high. (FAULT and RESET are active low signals). When the voltage on the D_{SAT} pin (pin no. 14) exceeds 7 V, while IGBT is on, V_{OUT} on pin no. 11 is slowly brought low in order to “softly” turn-off the IGBT and prevent large induced voltages. Also, an internal feedback channel is activated which brings FAULT output (pin no. 6) low for the purpose of notifying the microcontroller of the fault condition. The FAULT output remains low until RESET is brought low. An LED indication is provided in each driver circuit to indicate the occurrence of a fault, thus prompting a corrective action, either manually or through a microcontroller. The HCPL-316J Under Voltage Lockout (UVLO) feature is designed to prevent the application of insufficient gate voltage to IGBT by forcing the HCPL-316J output low during power-up. IGBTs typically require gate voltages of 15 V to achieve their rated $V_{CE(ON)}$ voltage. At gate voltages below 12 V typically, their on-voltage increases dramatically, especially at higher currents. At very low gate voltages (below 10 V), the IGBT may operate in the linear region and quickly overheat. The UVLO feature causes the output to be clamped whenever insufficient operating supply voltage is applied.

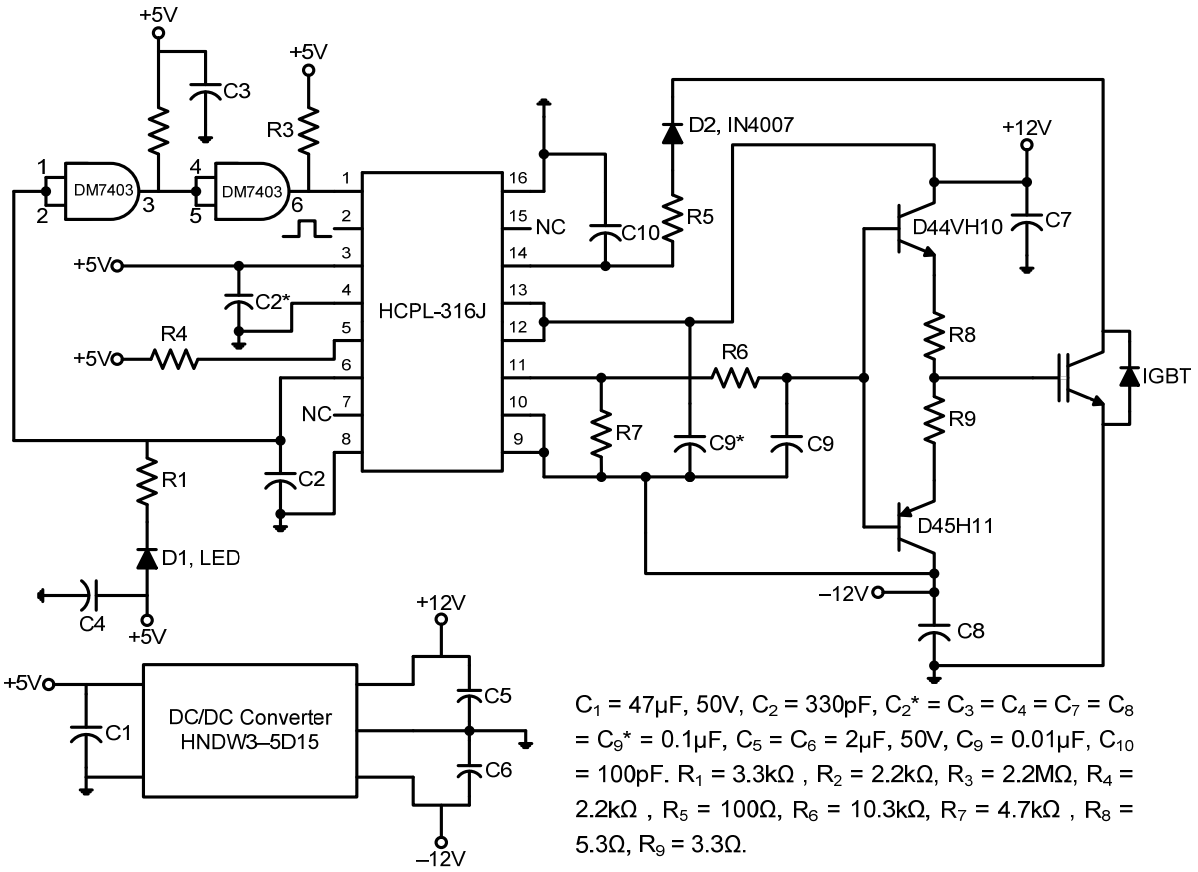


Fig. 5.11: IGBT driver circuit.

5.3 Experimental Validation

The prototype models of the three-phase five-level SSBC based D-STATCOMs are developed by integrating the power circuit, the control hardware and the dSPACE controller. The prototype models are tested in the laboratory to experimentally validate the simulation results. The developed power circuit is tested initially as a dc-ac inverter to experimentally validate the efficacy of the carrier rotation techniques. Subsequently, the developed prototype inverter is used as a power circuit of D-STATCOM to verify the viability and effectiveness of the transformerless PWM 3P3W D-STATCOM for harmonic elimination and reactive compensation. Finally, the developed prototype inverter is used to verify the simulation studies of the proposed hybrid 3P4W D-STATCOM topologies. The experimental results for each prototype are presented in the following sections.

5.4 Performance of Five-level SSBC based Inverter

To investigate the validity of carrier rotation techniques described earlier in Chapter 2, the power circuit is operated as a dc-ac inverter. The isolated dc supplies for the six H-bridge cells are provided by three single-phase, three-winding transformers with single-phase diode bridge rectifiers and filter capacitors. A three-phase lamp load is used as a load for the inverter. The parameters used in the experimental study are given in Table 5.1. The Simulink models of the various PWM controller schemes of the inverter are implemented using

dSPACE-DS1006 controller. The generated firing pulses are given to the corresponding semiconductor devices of each H-bridge of the inverter through isolation, delay and pulse amplification circuits in real-time.

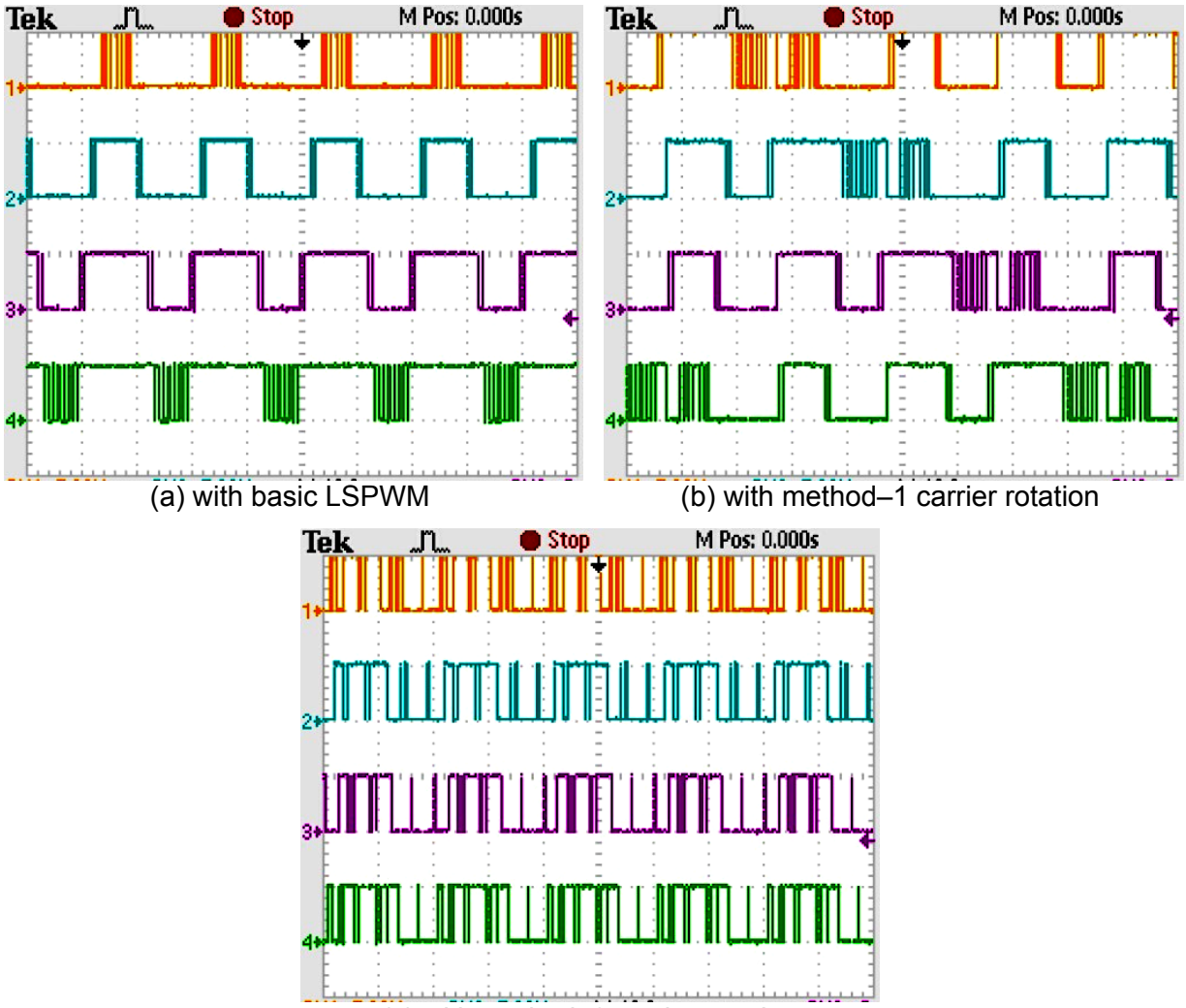
Table 5.1: Parameters used for the experimental validation of carrier rotation schemes.

Parameter	**Value**
Amplitude modulation index	m_a = 0.95
Carrier signal frequency	f_{cr} = 1500 Hz
Isolated dc source voltage	50 V each, provided by three single-phase three-winding transformers (230/115/115 V, 3 kVA) with single-phase bridge rectifiers (KBPC3510)
DC smoothening capacitors	450 V, 2200 μF each
Load	Three-phase lamp load (600 W)
Sampling time	T_s = 30 μs.

The experimentally obtained firing signals of phase–*a* of the inverter with and without carrier rotation techniques are shown in Fig. 5.12 (X-axis: 10 ms/div. and Y-axis: 5 V/div.). In Fig. 5.12 different traces (from top to bottom) in each waveform are the firing signals for the switching devices S_{11a}, S_{12a}, S_{22a} and S_{21a} respectively.

Fig. 5.13 shows the experimentally obtained line-to-line voltages, line-to-neutral voltages and harmonic spectra of line-to-line voltage of the five-level SSBC based inverter with and without carrier rotation techniques. In Fig. 5.13, the waveforms shown at the left hand side and the middle part depict the line-to-line (X-axis: 10 ms/div. and Y-axis: 50 V/div.) and line-to-neutral (X-axis: 5 ms/div. and Y-axis: 50 V/div.) voltages of inverter respectively, whereas the plots shown at right hand side depict the harmonic spectra of line-to-line voltages. In these experimental studies the amplitude and frequency modulation indices are kept at 0.95 and 30 respectively.

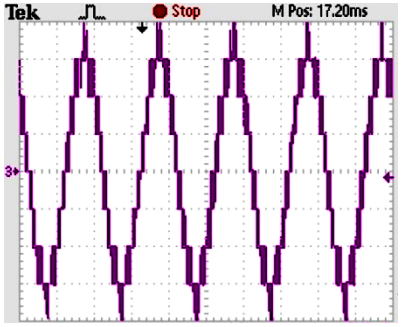
From Fig. 5.13, it can be observed that the output voltages synthesized by two carrier rotation techniques are almost identical with those obtained by the basic LSPWM technique. The THD values of line-to-line voltages are 8.7%, 8.5% and 8.6% for basic LSPWM, method–1 carrier rotation and method–2 carrier rotation technique respectively. The %THD values and side-band harmonic frequencies (around the harmonic order corresponding to the frequency modulation index, i.e. 30) of these carrier rotation techniques are also almost identical and in good agreement with the simulation results shown in Fig. 2.12.



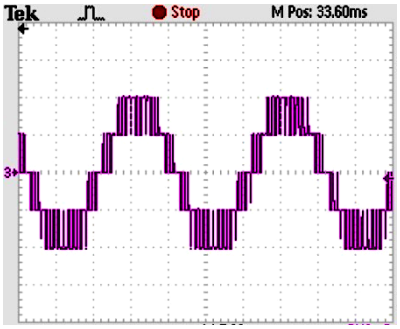
(a) with basic LSPWM (b) with method–1 carrier rotation

(c) with method–2 carrier rotation

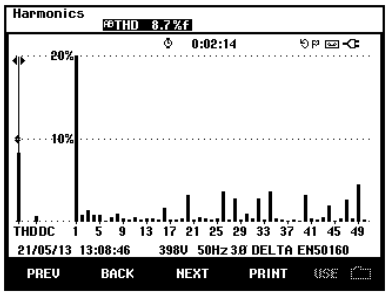
Fig. 5.12: Firing signals of inverter's phase leg–*a* with different modulation techniques (m_a = 0.95, f_m= 50 Hz and m_f = 30).



(a.1) Line-to-line voltage

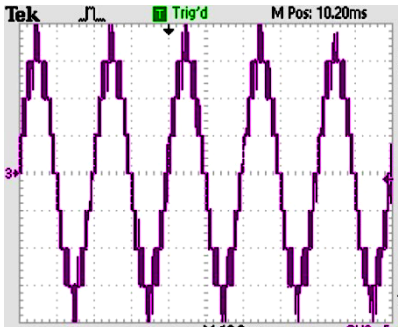


(a.2) Line-to-neutral voltage

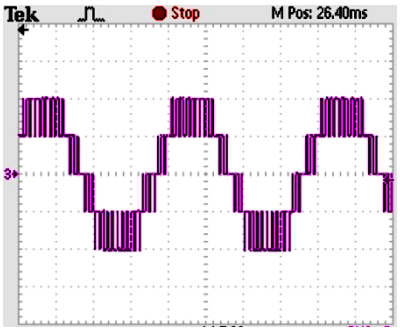


(a.3) Harmonic spectrum of line-to-line voltage

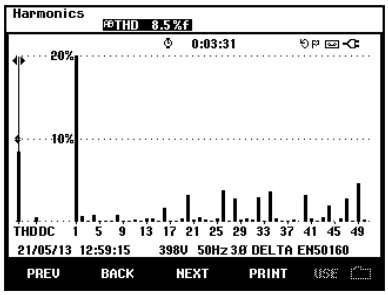
(a) with no rotation (basic LSPWM technique)



(b.1) Line-to-line voltage



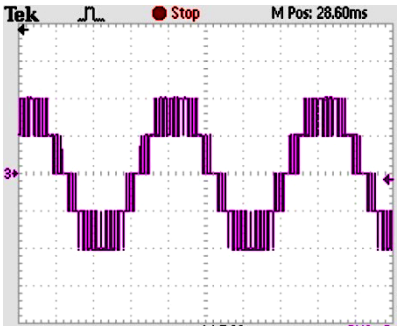
(b.2) Line-to-neutral voltage



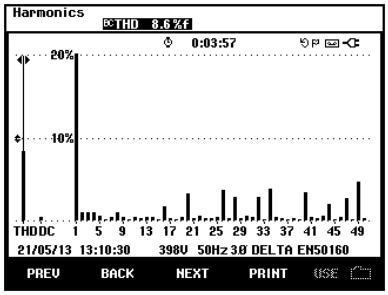
(b.3) Harmonic spectrum of line-to-line voltage

(b) with method–1 carrier rotation technique

(c.1) Line-to-line voltage



(c.2) Line-to-neutral voltage



(c.3) Harmonic spectrum of line-to-line voltage

(c) with method–2 carrier rotation technique

Fig. 5.13: Experimental waveforms of a five-level SSBC based inverter with and without carrier rotation techniques (m_a = 0.95, f_m= 50 Hz and m_f = 30): Recorded waveforms of line-to-line voltages (Left-side), line-to-neutral voltages (Middle) and harmonic spectra of line-to-line voltages (Right-side).

5.5 Performance of Five-level SSBC based 3P3W D-STATCOM

In this experimental study, the developed prototype inverter is used as a D-STATCOM to verify the viability and effectiveness of the transformerless PWM 3P3W D-STATCOM for harmonic elimination and reactive compensation. In D-STATCOM implementation, each H-bridge cell is equipped with a galvanically isolated and floating dc capacitor (without any power source or circuit). The D-STATCOM is connected to the PCC with series connected coupling inductor in each output phase of the inverter. The IRP based controller of the D-STATCOM is implemented in dSPACE. The modelling of the controller of a five-level SSBC

based D-STATCOM using RTW feature of MATLAB and RTI feature of dSPACE are shown in Appendix B.

To verify the viability and effectiveness of the SSBC based D-STATCOM for harmonic elimination and reactive compensation, experimental investigations are conducted with non-linear/reactive loads. The uncontrolled and phase-controlled rectifiers with *RL* and *RC* loads on their dc side are used as non-linear loads. For this purpose, a three-phase uncontrolled diode bridge rectifier and a three-phase phase-controlled thyristor bridge rectifier are developed in the laboratory. A snubber circuit is also connected across each device for protection of semiconductor devices. Each device is mounted on suitably designed heat sink to ensure proper heat dissipation. A suitable firing circuit is also developed for the phase-controlled rectifier. The schematic diagrams of uncontrolled rectifiers with *RL* and *RC* loads and phase-controlled rectifier with *RL* and *RC* loads on their dc side are shown in Fig. 5.14.

Extensive experimental studies are carried to investigate the performance of 3P3W D-STATCOM for harmonic elimination and reactive power compensation under different loading and utility voltage conditions. The parameters used in the simulation are given in Table 5.2. The relevant discussions for these experimental studies are given below in various sections.

Table 5.2: Parameters used for the experimental validation of 3P3W D-STATCOM.

Parameter	**Value**
AC line parameters	Three-phase, three-wire, 100 V, 50 Hz
DC bus voltage of D-STATCOM	60 V (for each capacitor in the H-bridge cell)
DC bus capacitance of D-STATCOM	2200 μF, 450 V (for each capacitor in the H-bridge cell)
D-STATCOM coupling inductor	L_c = 6.4 mH
Commutation inductance	L_f = 1 mH
PWM switching frequency	3 kHz
PI controller parameters	For cluster voltage balancing control: K_p = 0.4, K_i = 0.6 For individual voltage balancing control: K_p = 0.1, K_i = 2.2.
Load	Three-phase uncontrolled rectifier with *RL* and *RC* loads; Three-phase controlled rectifier with *RL* and *RC* loads, firing angle ≈ 30º.
Sampling time	T_s = 50 μs.

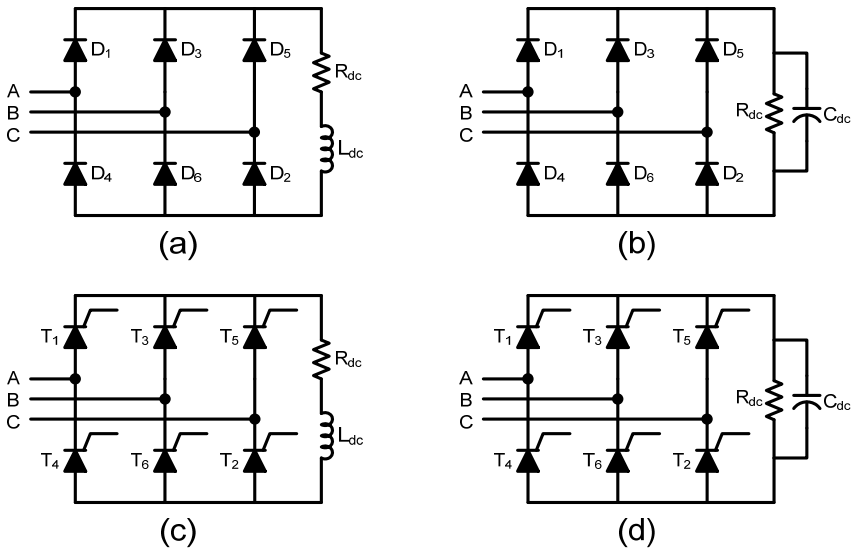


Fig. 5.14: Three-phase non-linear/reactive loads: (a) Uncontrolled rectifier with *RL* load; (b) Uncontrolled rectifier with *RC* load; (c) Phase-controlled rectifier with *RL* load; (d) Phase-controlled rectifier with *RC* load.

5.5.1 Performance of D-STATCOM with Normal Voltage Conditions

Experimental results under normal voltage conditions with uncontrolled and phase-controlled rectifiers having *RL* and *RC* loads on their dc sides are presented in this section.

5.5.1.1 Uncontrolled Rectifier with *RL* Load

An uncontrolled rectifier with series connection of resistive and inductive load on its dc side is considered as a non-linear load in this case. Fig. 5.15(a) shows the typical three-phase load currents drawn by this rectifier (X-axis: 2.5 ms/div., Y-axis: 2 A/div.). The currents drawn by the rectifier are non-sinusoidal. The harmonic spectrum of the phase–*a* load current is shown in Fig. 5.15(b), which contains significant amounts of 5^{th}, 7^{th}, 11^{th} and 13^{th} order harmonics with resulting THD of 28.7%.

The developed D-STATCOM is tested for reactive power compensation and harmonic elimination with method–1 and method–2 carrier rotation techniques and the experimental waveforms under steady state condition with normal source voltage are shown in Fig. 5.16. The source voltage, source current after compensation, load current and compensating currents for phase–*a* with method–1 and method–2 carrier rotation techniques are shown in Fig. 5.16(a) and Fig. 5.16(b) respectively. Since a three-phase balanced load is considered, the results are shown corresponding to phase–*a* only. These figures and all the subsequent figures showing similar experimental results, the different waveforms are identified as:

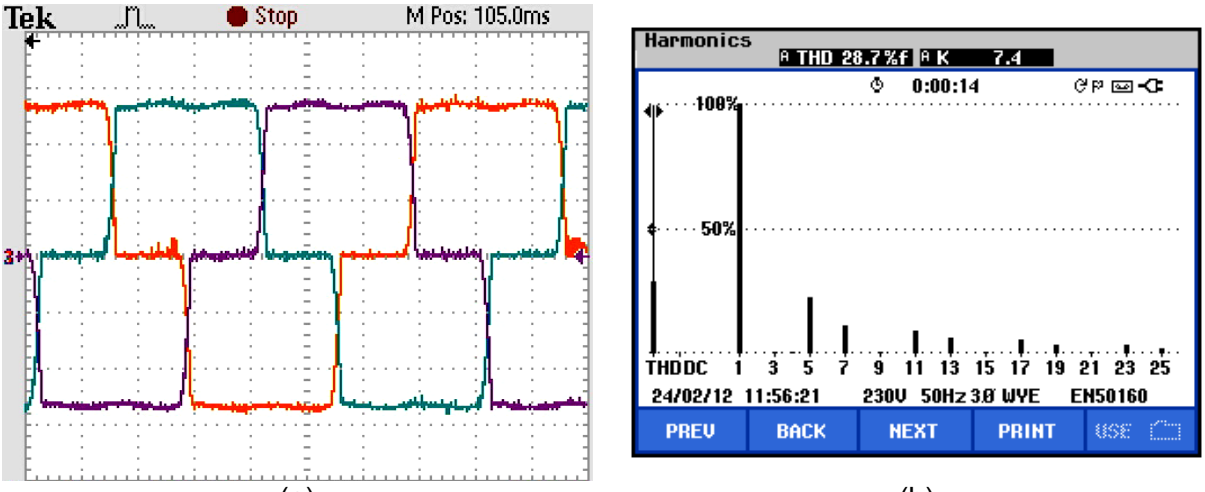
Trace–1: source voltage (X-axis: 10 ms/div., Y-axis: 100 V/div.),

Trace–2: source current after compensation (X-axis: 10 ms/div., Y-axis: 5 A/div.),

Trace–3: load current (X-axis: 10 ms/div., Y-axis: 5 A/div.),

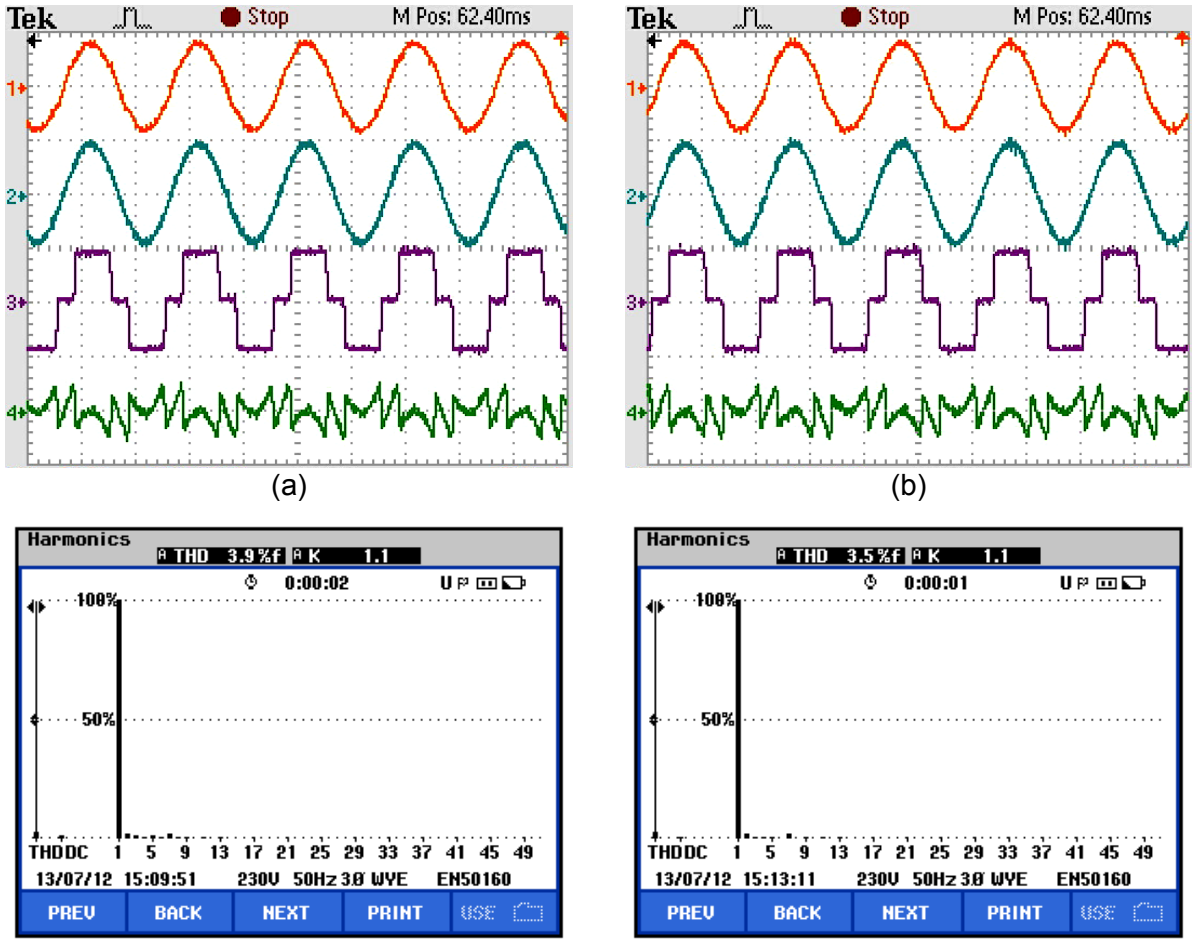
Trace–4: compensating current injected by the D-STATCOM (X-axis: 10 ms/div., Y axis: 5 A/div.).

The harmonic spectra of source currents after compensation with method–1 and method–2 carrier rotation techniques are shown in Fig. 5.16(c) and Fig. 5.16(d) respectively.



(a) (b)

Fig. 5.15: Performance of an uncontrolled rectifier with *RL* load on its dc side: (a) Three-phase load currents; (b) Harmonic spectrum of phase–*a* load current.



(a) (b)

(c) (d)

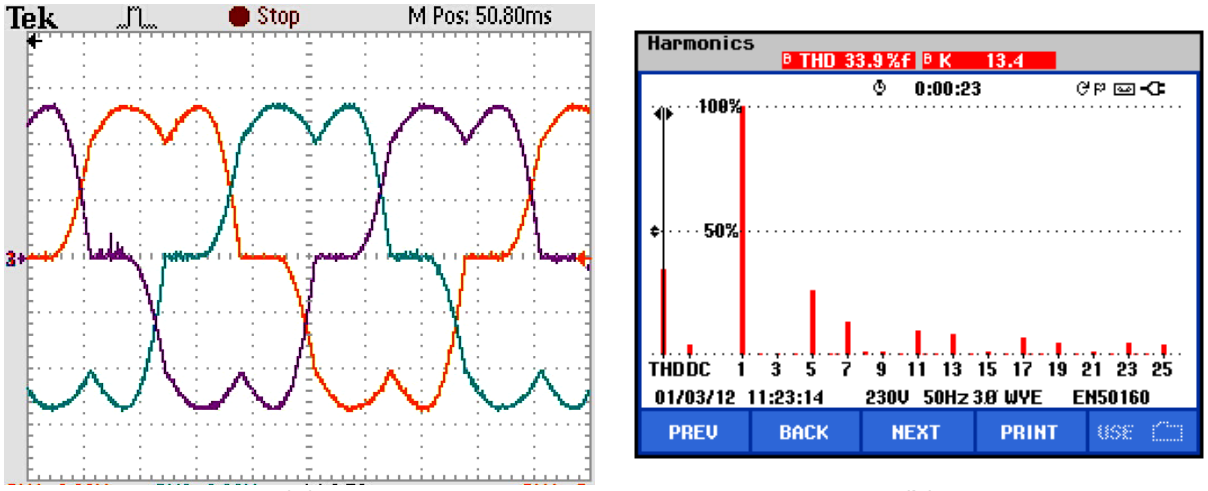
Fig. 5.16: Experimental results of 3P3W D-STATCOM for an *RL* load on the dc side of an uncontrolled rectifier with method–1 and method–2 carrier rotation techniques with normal source voltage conditions.

The experimental results presented in Fig. 5.16 are observed to be in good agreement with simulation results. From Fig. 5.16, the following quantitative observations are made:

1. After compensation with D-STATCOM, the %THD of the load current is 28.7%, but the source current THD is reduced to 3.9% and 3.5% with method–1 and method–2 carrier rotation techniques respectively. These THD values of source currents after compensation are well within the limits of IEEE–519–1992 standard.
2. The rms value of the load current is 3.3 A and that of the source current is 3.5 A in method–1 and 3.6 A in method–2 carrier rotation technique. The enhancement in the source currents is due to the compensation of real power losses of the inverter. The power factor and displacement factor of the source are almost unity in both cases.

5.5.1.2 Uncontrolled Rectifier with *RC* Load

An uncontrolled rectifier with *RC* load on its dc side is considered as a non-linear load in this case. Fig. 5.17(a) shows the typical three-phase load currents drawn by an uncontrolled rectifier with *RC* load on its dc side (X-axis: 2.5 ms/div., Y-axis: 2 A/div.). The currents drawn by the rectifier are non-sinusoidal. The harmonic spectrum of the phase–*a* load current is shown in Fig. 5.17(b), which contains significant amounts of odd order harmonics other than triplen harmonics with resulting THD of 33.9%.



(a) (b)

Fig. 5.17: Performance of an uncontrolled rectifier with *RC* load on its dc side: (a) Three-phase load currents; (b) Harmonic spectrum of phase–*a*.

The developed D-STATCOM is tested for reactive power compensation and harmonic elimination with method–1 and method–2 carrier rotation techniques for this load also. The experimental waveforms under steady state condition with normal source voltage are shown in Fig. 5.18.

The source voltage, source current after compensation, load current and compensating currents for phase–*a* with method–1 and method–2 carrier rotation techniques are shown in

Fig. 5.18(a) and Fig. 5.18(b) respectively. The harmonic spectra of source currents after compensation with method–1 and method–2 carrier rotation techniques are shown in Fig. 5.18(c) and Fig. 5.18(d) respectively. From Fig. 5.18, it can be observed that after compensation with D-STATCOM, the source current %THD is improved from 33.9% to 3.9% in method–1 and 3.6% in method–2 carrier rotation technique respectively. The rms value of the source current is increased from 3.1 A to 3.4 A in method–1 and to 3.3 A in method–2 carrier rotation technique to compensate for the losses in the inverter. In both cases, the source power factor and displacement factor are almost unity.

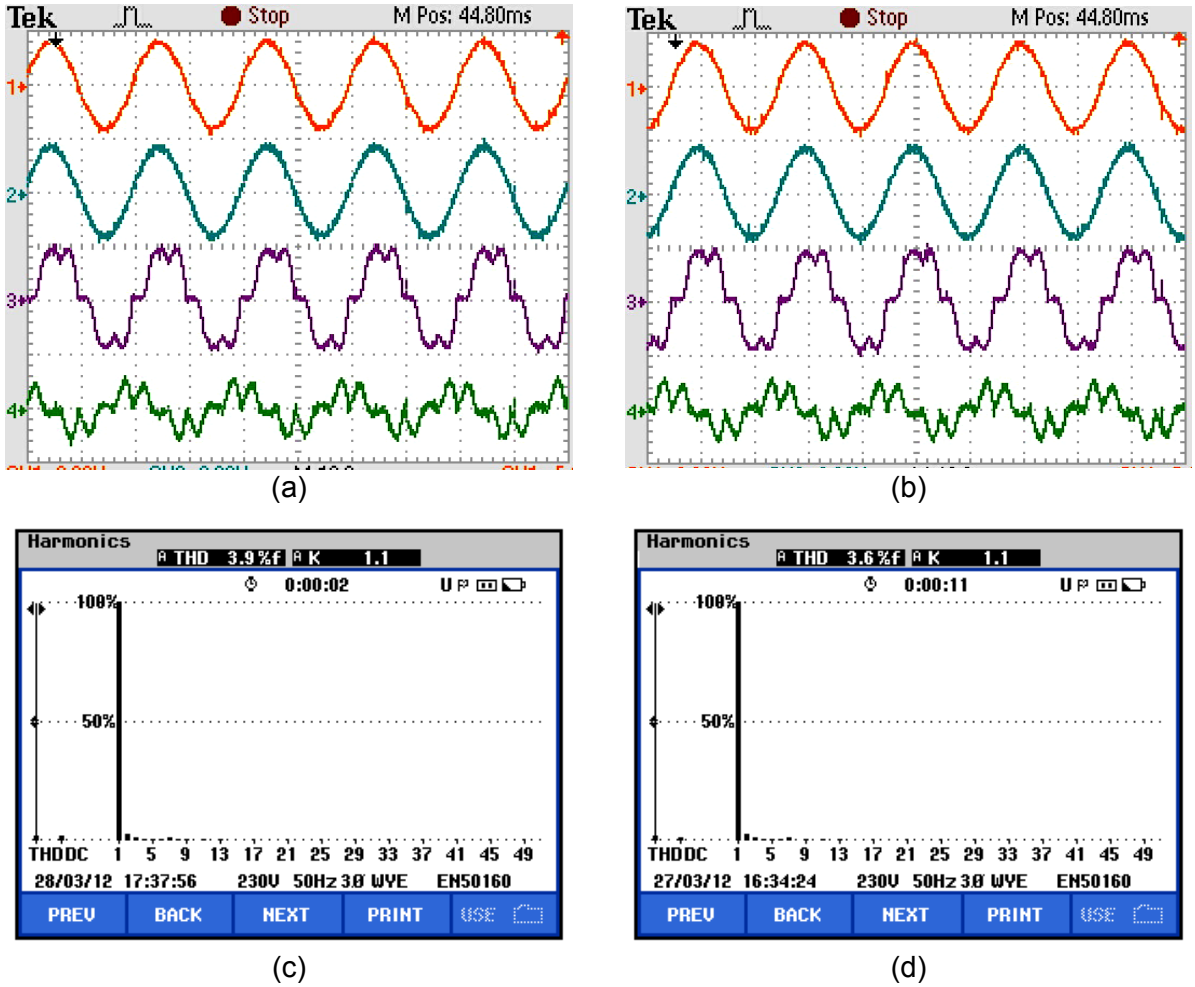


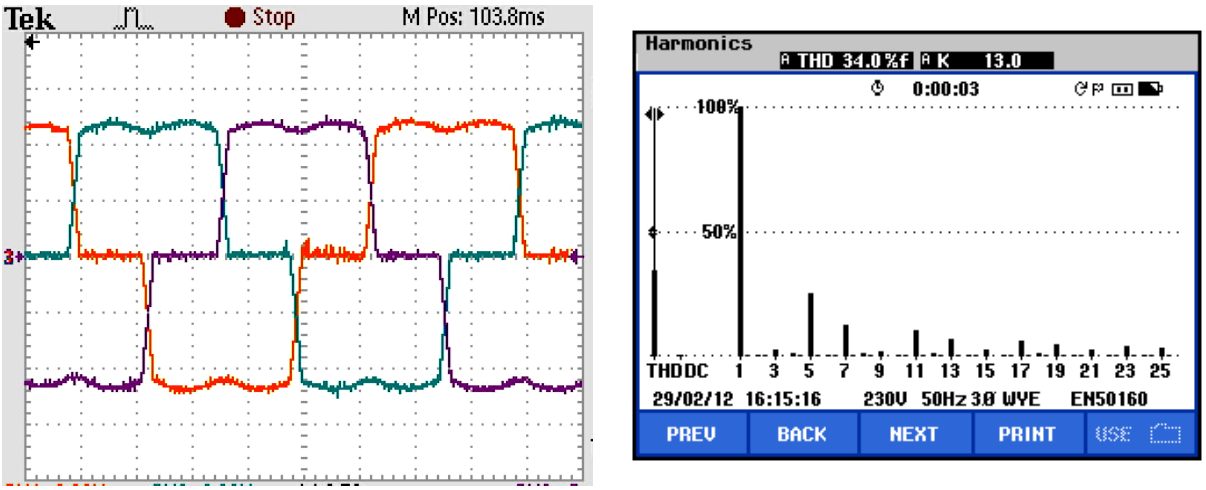
Fig. 5.18: Experimental results of 3P3W D-STATCOM for an *RC* load on the dc side of an uncontrolled rectifier with method–1 and method–2 carrier rotation techniques with normal source voltage conditions.

5.5.1.3 Controlled Rectifier with *RL* Load

A phase-controlled rectifier with *RL* load on its dc side is considered as a non-linear load in this case. Fig. 5.19(a) shows the typical three-phase load currents drawn by the phase-controlled rectifier operated at a firing angle of 30º (X-axis: 2.5 ms/div., Y-axis: 2 A/div.). The currents drawn by the rectifier are reactive and non-sinusoidal with sharp rising and falling edges. The harmonic spectrum of the phase–*a* load current is shown in Fig.

5.19(b), which contains high amount of 5th, 7th, 11th and 13th order harmonics with resulting THD of 34.0%. The source power factor before compensation is 0.84 (lagging).

The developed D-STATCOM is tested with method–1 and method–2 carrier rotation techniques and the experimental waveforms under steady state conditions with normal source voltage are shown in Fig. 5.20.



(a) (b)

Fig. 5.19: Performance of a phase-controlled rectifier (α = 30º) with *RL* load on its dc side: (a) Three-phase load currents; (b) Harmonic spectrum of phase–*a*.

The source voltage, source current after compensation, load current and compensating currents for phase–*a* with method–1 and method–2 carrier rotation techniques are shown in Fig. 5.20(a) and Fig. 5.20(b) respectively. The harmonic spectra of source currents after compensation with method–1 and method–2 carrier rotation techniques are shown in Fig. 5.20(c) and Fig. 5.20(d) respectively.

From Fig. 5.20, it can be observed that after compensation with D-STATCOM, the source current THD is improved from 34.0% to 4.9% in method–1 and 4.5% in method–2 carrier rotation technique respectively. In both carrier rotation techniques, after compensation, the source current waveform is observed to be in phase with the source voltage waveform, which ensured the compensation of load reactive power. The rms value of the source current is reduced from 3.3 A to 2.9 A in method–1 and 2.8 A in method–2 carrier rotation technique. Actually, the reduction in the source current due to reactive power compensation is more than the enhancement of source current due to power loss compensation and therefore, overall the source current is decreased. In both cases, the power factor is improved from 0.84 lagging to 0.99 lagging.

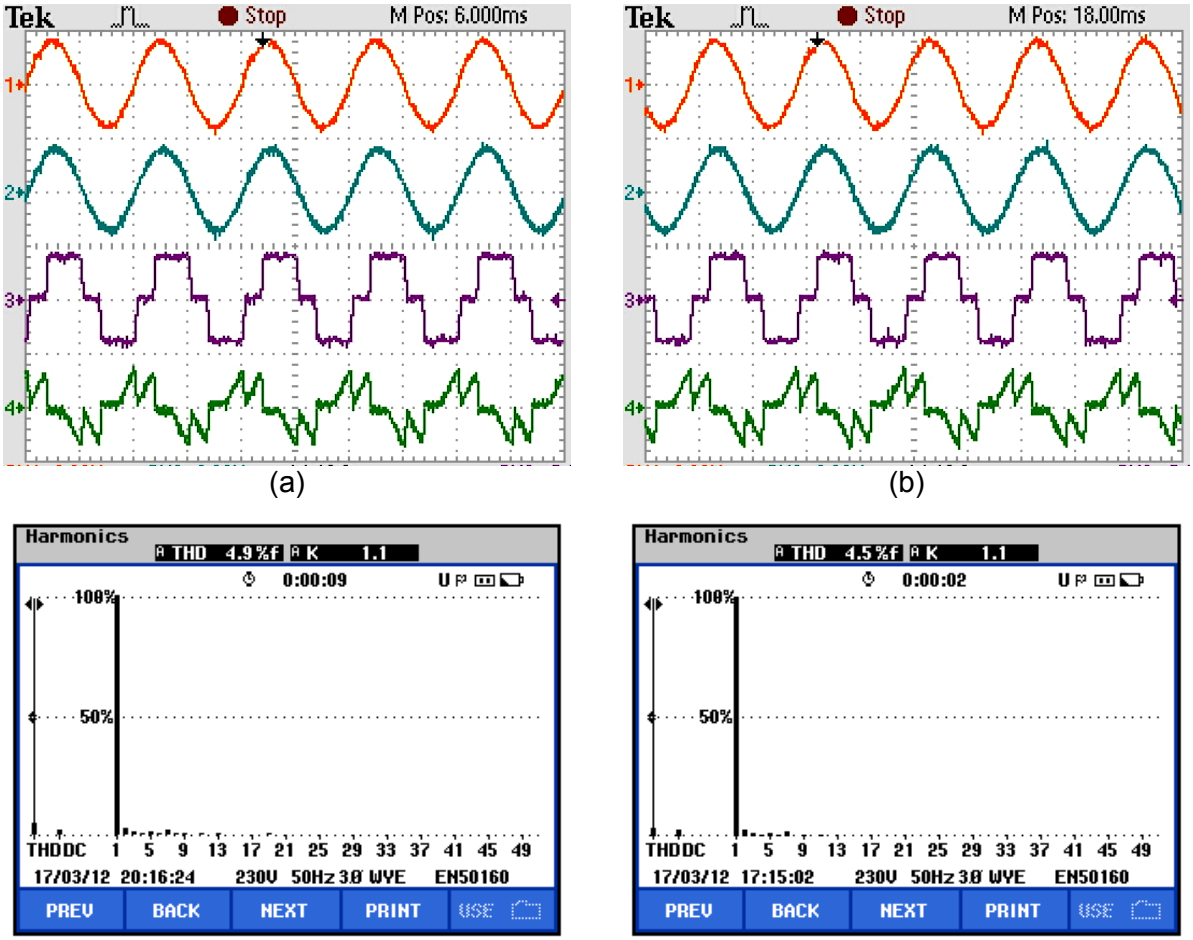
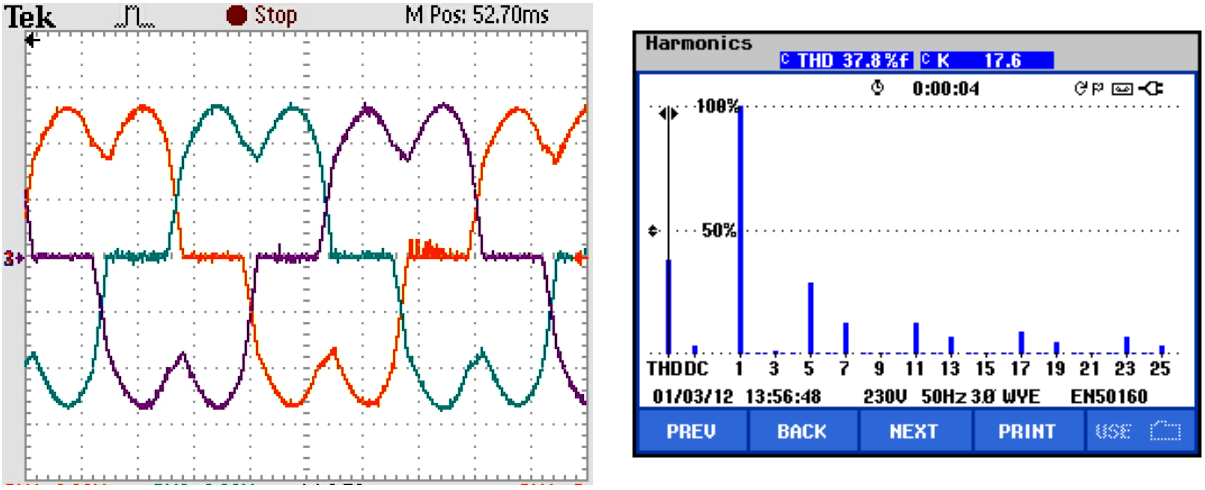


Fig. 5.20: Experimental results of 3P3W D-STATCOM with *RL* load on the dc side of a phase-controlled rectifier with method–1 and method–2 carrier rotation techniques under normal source voltage conditions.

5.5.1.4 Controlled Rectifier with *RC* Load

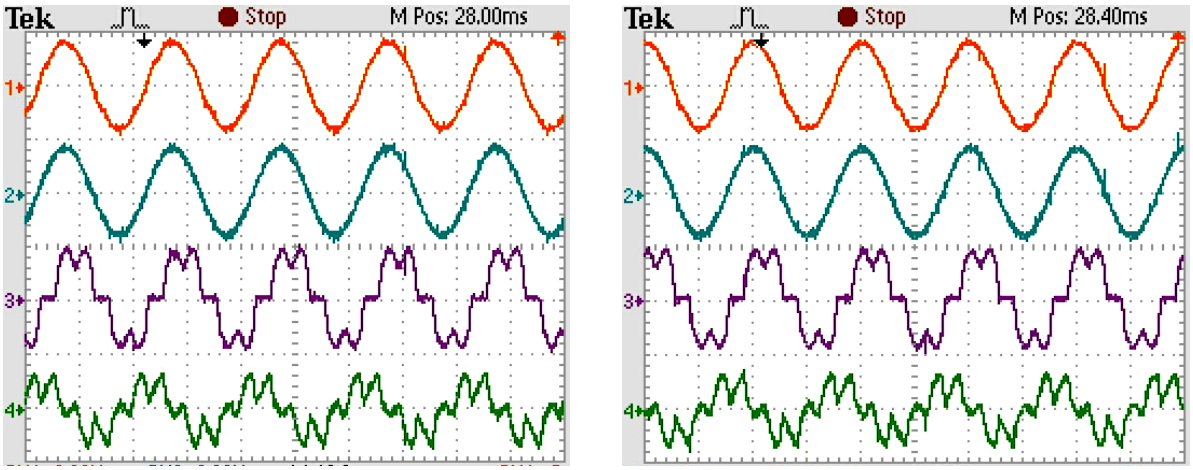
A phase-controlled rectifier with *RC* load on its dc side is considered as a non-linear load in this case. Fig. 5.21(a) shows the typical three-phase load currents drawn by a phase-controlled rectifier operated at a firing angle (α) of 30º (X-axis: 2.5 ms/div., Y-axis: 2 A/div.). The currents drawn by the rectifier are reactive and non-sinusoidal with sharp rising and falling edges. The harmonic spectrum of the phase–*a* load current is shown in Fig. 5.21(b), which contains a high amount of 5^{th}, 7^{th}, 11^{th} and 13^{th} order harmonics with resulting THD of 37.8%. The source power factor before compensation is 0.83 (lagging).

The developed D-STATCOM is tested with method–1 and method–2 carrier rotation techniques and the experimental waveforms under steady state conditions with normal source voltage are shown in Fig. 5.22. The source voltage, source current after compensation, load current and compensating currents for phase–*a* with method–1 and method–2 carrier rotation techniques are shown in Fig. 5.22(a) and Fig. 5.22(b) respectively. The harmonic spectrums of source currents after compensation with method–1 and method–2 carrier rotation techniques are shown in Fig. 5.22(c) and Fig. 5.22(d) respectively.

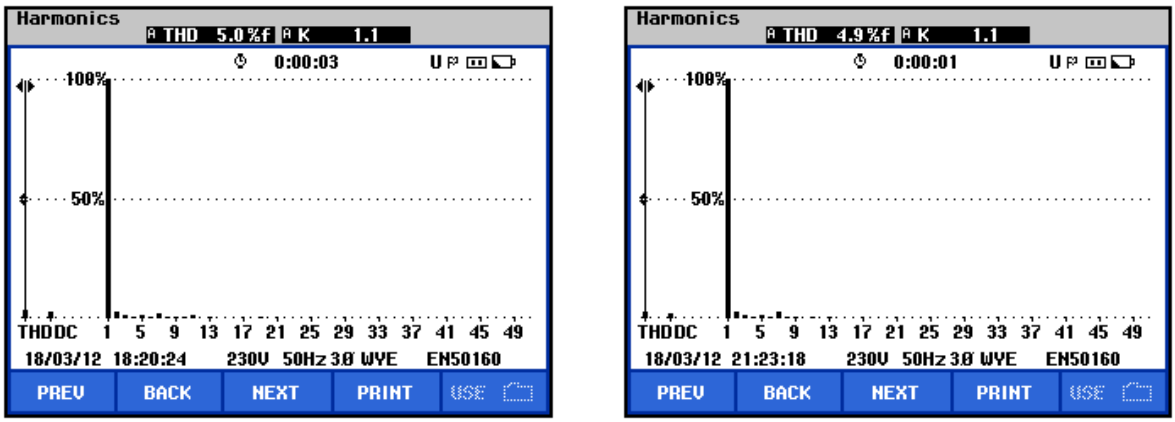


(a) (b)

Fig. 5.21: Performance of a phase-controlled rectifier (α = 30°) with *RC* load on its dc side: (a) Three-phase load currents; (b) Harmonic spectrum of phase–*a*.



(a) (b)



(c) (d)

Fig. 5.22: Experimental results of 3P3W D-STATCOM with *RC* load on the dc side of a phase-controlled rectifier with method–1 and method–2 carrier rotation techniques under normal source voltage conditions.

From Fig. 5.22, it can be observed that after compensation with D-STATCOM, the source current THD is improved from 37.8% to 5.0% in method–1 and 4.9% in method–2 carrier rotation technique respectively. In both carrier rotation techniques, after

compensation, the source current waveform is observed to be in phase with the source voltage waveform, which ensured the compensation of load reactive power. Hence, the rms value of the source current is reduced from 3.6 A to 3.2 A in method–1 and 3.3 A in method–2 carrier rotation technique. In both cases, the power factor is improved from 0.83 lagging to 0.999 lagging.

5.5.2 Experimental Results with Unbalanced/Distorted Voltage Conditions

In order to verify the efficacy of the controller in compensating source currents under non-ideal voltage conditions, harmonics and magnitude unbalance are introduced to the source voltage. Fig. 5.23 shows the three-phase unbalanced/distorted source voltages, while Fig. 5.24 shows the harmonic spectra of individual phase voltages. The THD values of three phase voltages are 7.2%, 8.5% and 6.9% respectively. Experimental results under these unbalanced/distorted voltage conditions with an uncontrolled and phase-controlled rectifiers having *RL* and *RC* loads on their dc sides are presented in this section.

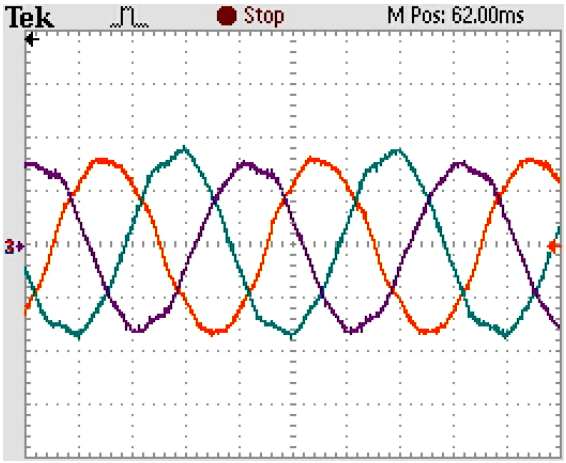
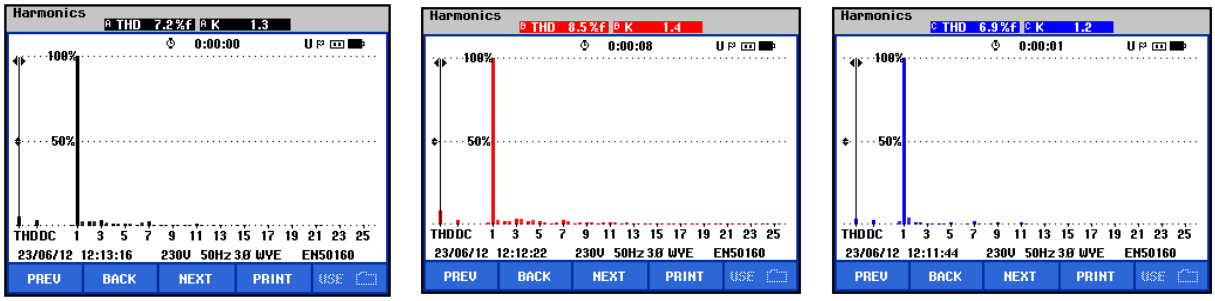


Fig. 5.23: Unbalanced/distorted three-phase source voltages



(a) (b) (c)

Fig. 5.24: Harmonic spectra of source voltages: (a) Phase–*a*; (b) Phase–*b*; (c) Phase–*c*.

5.5.2.1 Uncontrolled Rectifier with *RL* Load

An uncontrolled rectifier with resistive and inductive load on its dc side is considered as a non-linear load in this case. Fig. 5.25 shows the experimental results under this condition. The source voltage, source current after compensation, load current and compensating currents for phase–*a* with method–1 and method–2 carrier rotation techniques are shown in Fig. 5.25(a) and Fig. 5.25(b) respectively. The harmonic spectra of source currents after

compensation with method–1 and method–2 carrier rotation techniques are shown in Fig. 5.25(c) and Fig. 5.25(d) respectively. The experimental results are in good agreement with simulation results and from Fig. 5.25, the following quantitative observations are made:

1. After compensation with D-STATCOM, the %THD of the load current is 29.1%, but the source current THD is reduced to 4.7% and 4.4% with method–1 and method–2 carrier rotation techniques respectively. This reduction in %THD values validates the effectiveness of the control scheme under unbalanced/distorted source voltage conditions.
2. The rms value of the load current is 3.2 A and that of the source current is 3.3 A in method–1 and 3.5 A in method–2 carrier rotation technique.
3. The power factor and displacement factor of the source are almost unity in both cases.

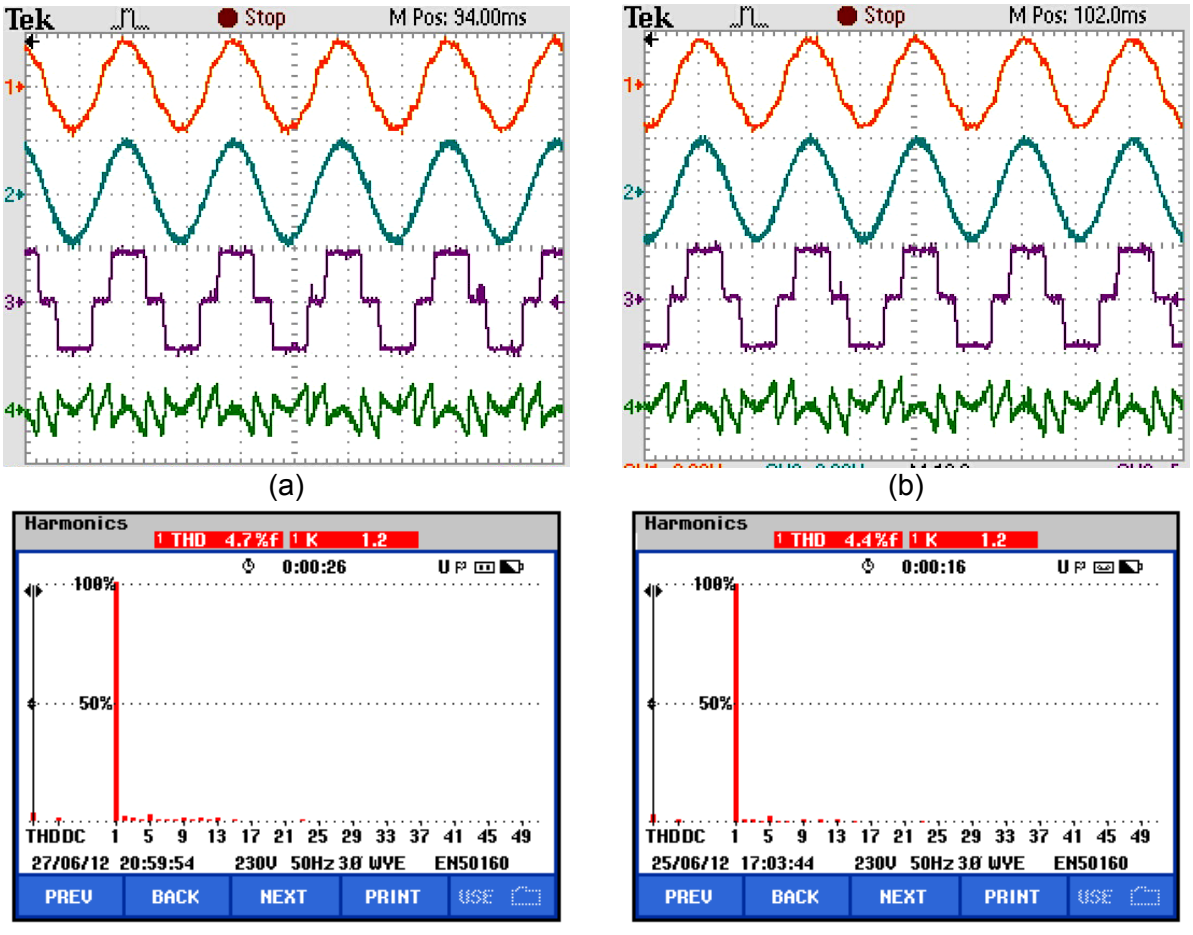


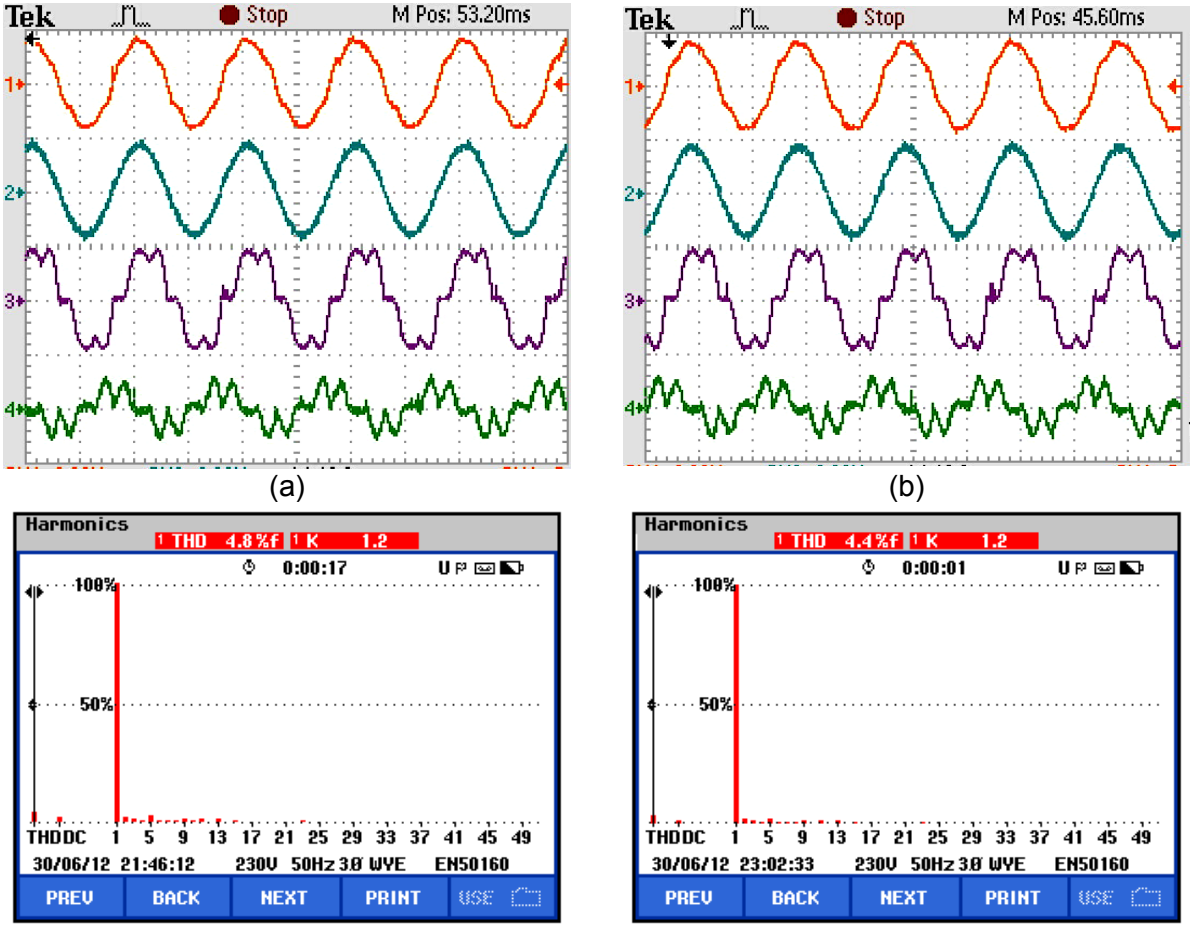
Fig. 5.25: Experimental results of 3P3W D-STATCOM with *RL* load on the dc side of an uncontrolled rectifier with method–1 and method–2 carrier rotation techniques under unbalanced/distorted source voltage conditions.

5.5.2.2 Uncontrolled Rectifier with *RC* Load

An uncontrolled rectifier with *RC* load on its dc side is considered as a non-linear load in this case. Fig. 5.26 shows the experimental results under this condition. The source

voltage, source current after compensation, load current and compensating currents for phase–*a* with method–1 and method–2 carrier rotation techniques are shown in Fig. 5.26(a) and Fig. 5.26(b) respectively. The harmonic spectra of source currents after compensation with method–1 and method–2 carrier rotation techniques are shown in Fig. 5.26(c) and Fig. 5.26(d) respectively.

The experimental results are in good agreement with simulation results and from Fig. 5.26, it can be observed that after compensation with D-STATCOM, the source current THD is improved from 32.3% to 4.8% in method–1 and 4.4% in method–2 carrier rotation technique. The rms value of the source current is increased from 3.2 A to 3.5 A in method–1 and 3.4 A in method–2 carrier rotation technique respectively to compensate the losses in the inverter. In both cases, the source power factor and displacement factor are almost unity.



(a) (b)

(c) (d)

Fig. 5.26: Experimental results of 3P3W D-STATCOM with *RC* load on the dc side of an uncontrolled rectifier with method–1 and method–2 carrier rotation techniques under unbalanced/distorted source voltage conditions.

5.5.2.3 Controlled Rectifier with *RL* Load

A phase-controlled rectifier operated at a firing angle of 30º with *RL* load on its dc side is considered as a non-linear load in this case. Fig. 5.27 shows the experimental results under this condition. The source voltage, source current after compensation, load current and compensating currents for phase–*a* with method–1 and method–2 carrier rotation

techniques are shown in Fig. 5.27(a) and Fig. 5.27(b) respectively. The harmonic spectra of source currents after compensation with method–1 and method–2 carrier rotation techniques are shown in Fig. 5.27(c) and Fig. 5.27(d) respectively. From Fig. 5.27, it can be observed that after compensation with D-STATCOM, the source current THD is improved from 33.5% to 4.9% in method–1 and 4.8% in method–2 carrier rotation technique. In both carrier rotation techniques, after compensation, the source current waveform is observed to be in phase with the source voltage waveform, which ensures the compensation of load reactive power. In both cases, the power factor is improved from 0.83 lagging to unity. The rms value of the source current is reduced from 3.4 A to 2.9 A in method–1 and 2.8 A in method–2 carrier rotation technique respectively.

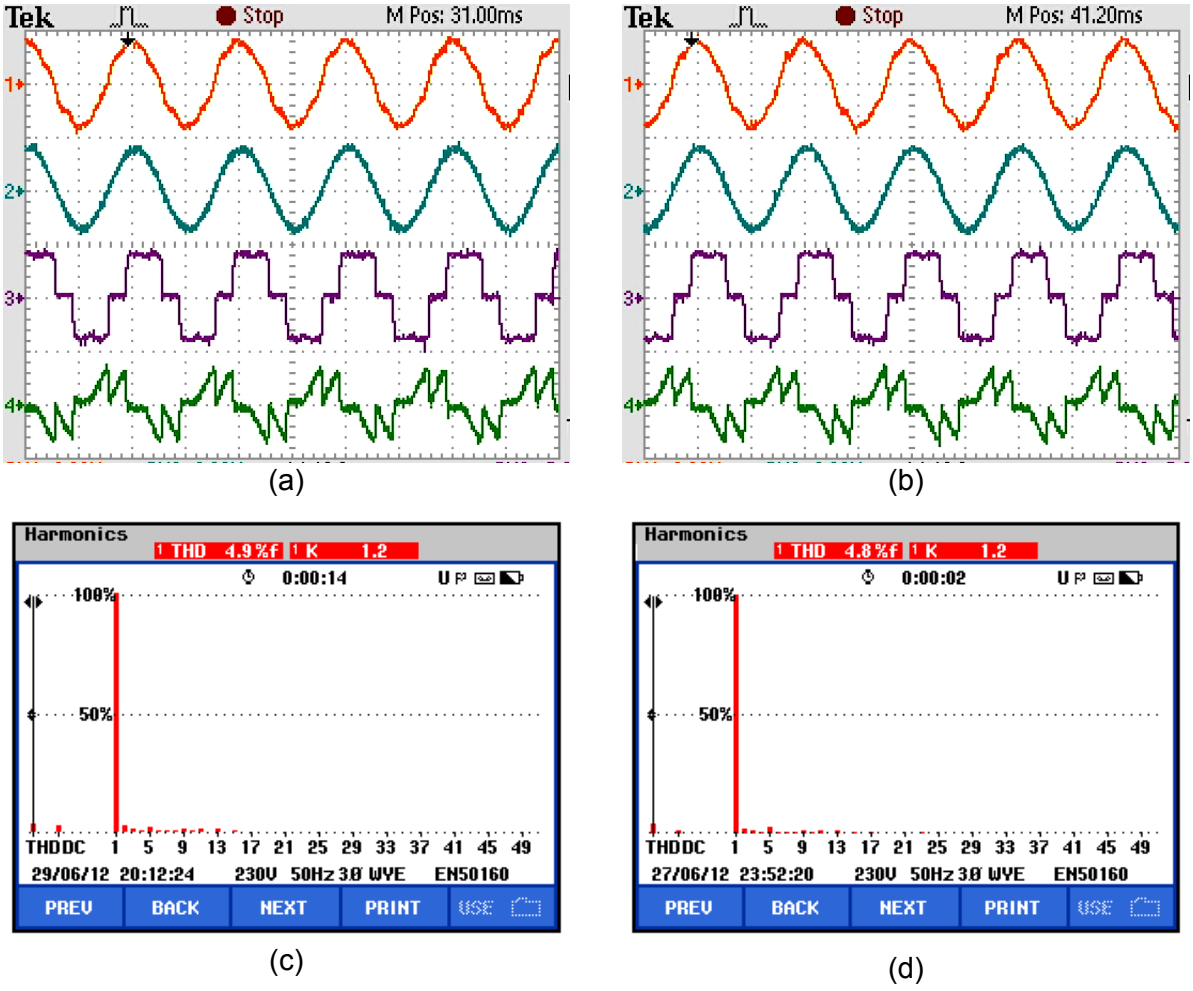


Fig. 5.27: Experimental results of 3P3W D-STATCOM with *RL* load on the dc side of a phase-controlled rectifier with method–1 and method–2 carrier rotation techniques under unbalanced/distorted source voltage conditions.

5.5.2.4 Controlled Rectifier with *RC* Load

A phase-controlled rectifier operated at a firing angle of 30º with *RC* load on its dc side is considered as a non-linear load in this case. Fig. 5.28 shows the experimental results under this condition. The source voltage, source current after compensation, load current and compensating currents for phase–*a* with method–1 and method–2 carrier rotation

techniques are shown in Fig. 5.28(a) and Fig. 5.28(b) respectively. The harmonic spectra of source currents after compensation with method–1 and method–2 carrier rotation techniques are shown in Fig. 5.28(c) and Fig. 5.28(d) respectively. From Fig. 5.28, it can be observed that after compensation with D-STATCOM, the source current THD is improved from 48.3% to 5.3% in method–1 and 5.2% in method–2 carrier rotation technique. In both carrier rotation techniques, after compensation, the source current waveform is observed to be in phase with the source voltage waveform. In both cases, the power factor is improved from 0.82 lagging to unity. The rms value of the source current is reduced from 3.6 A to 3.3 A in method–1 and 3.4 A in method–2 carrier rotation technique respectively.

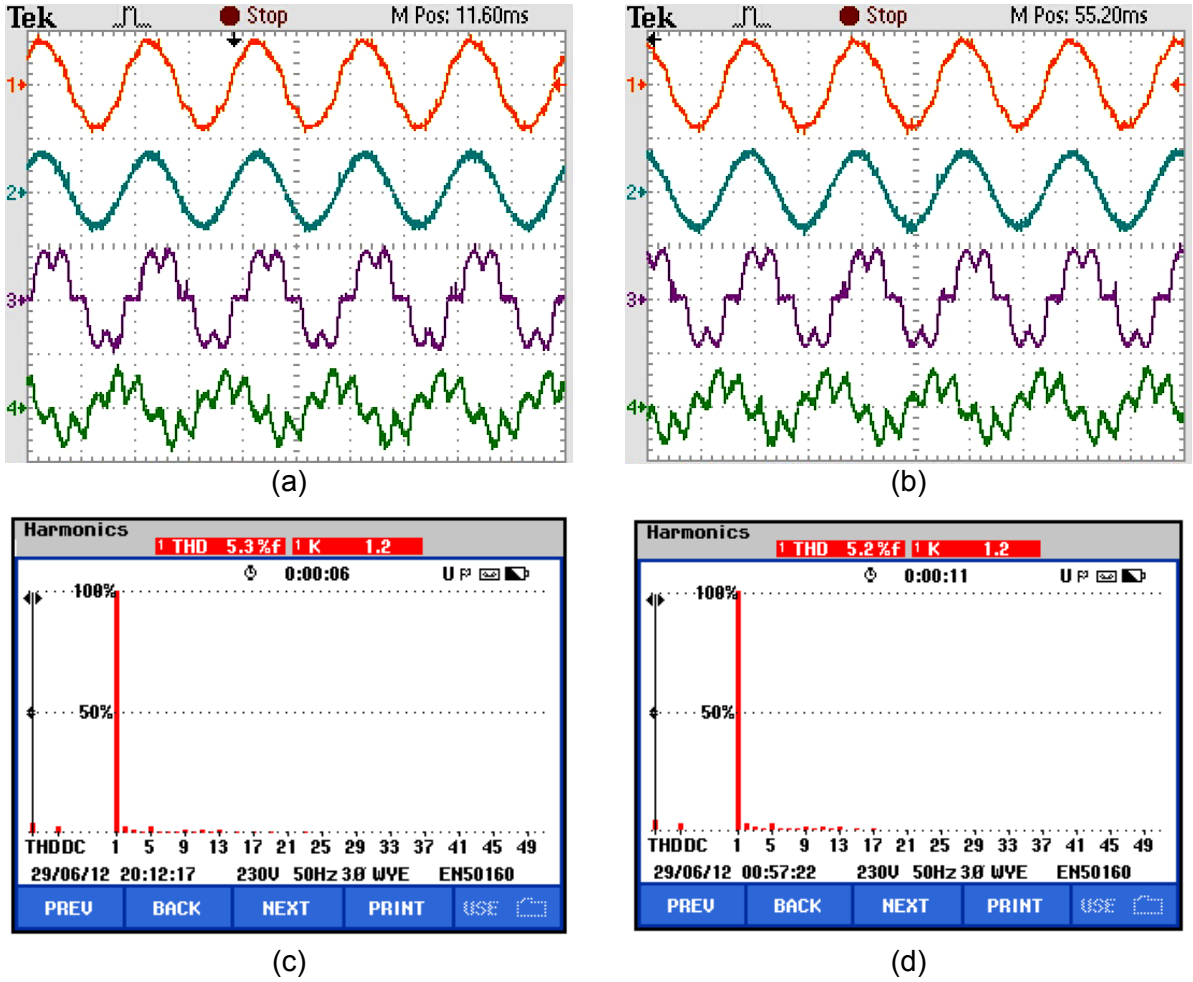


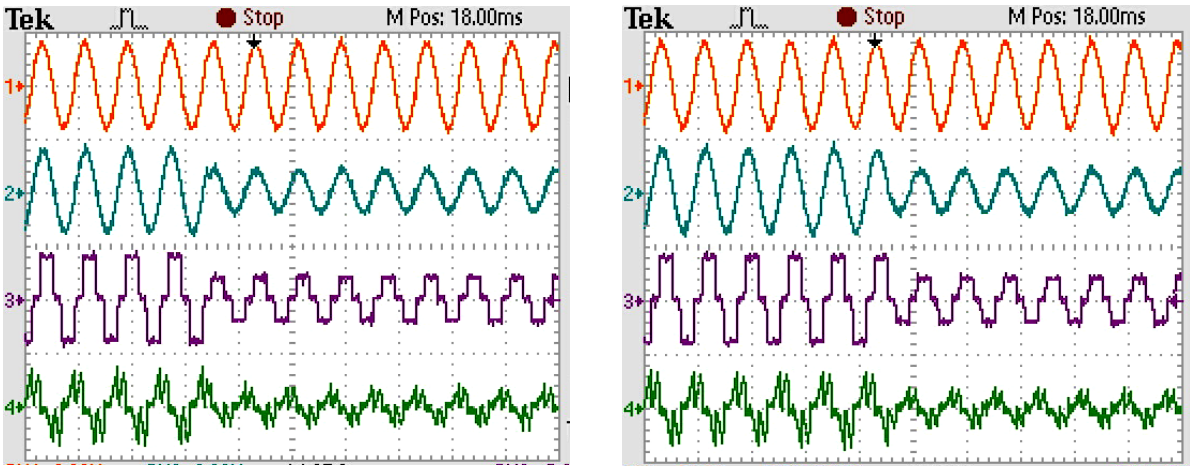
Fig. 5.28: Experimental results of 3P3W D-STATCOM with *RC* load on the dc side of a phase-controlled rectifier with method–1 and method–2 carrier rotation techniques under unbalanced/distorted source voltage conditions.

5.5.3 Transient Performance

The transient performance of the prototype D-STATCOM is studied for step increase and reduction in load current. The experimental results with normal and distorted source voltage conditions are presented and discussed below. In these experimental studies, a phase-controlled rectifier operated at a firing angle of 30º with *RL* load on its dc side is considered as a non-linear load.

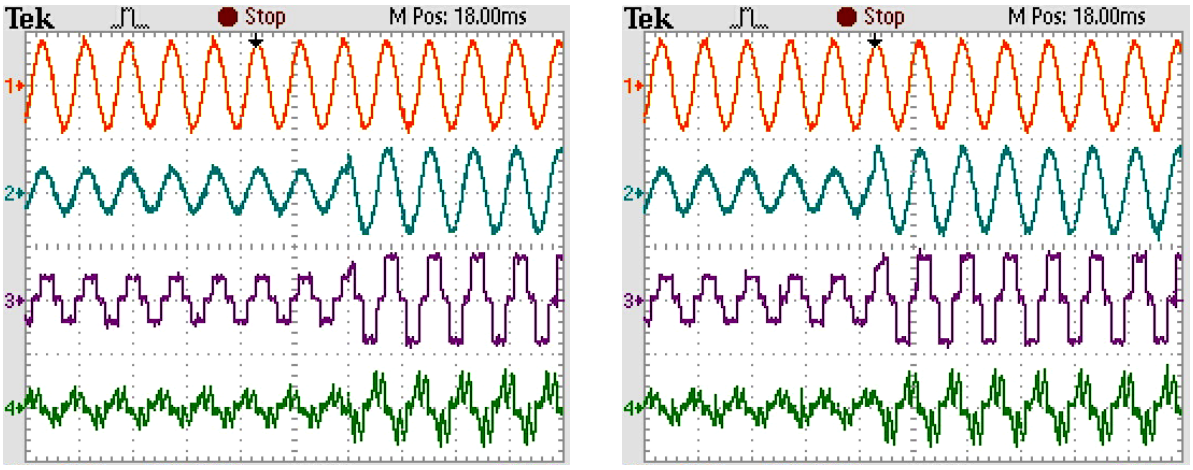
5.5.3.1 Transient Performance with Normal Voltage Conditions

The transient performance of the compensator with normal voltage conditions are presented in this section. Fig. 5.29(a) shows the experimental results of source voltage, source current after compensation, load current and compensating currents for phase–*a* with method–1 and method–2 carrier rotation techniques with 50% reduction in the load current under normal source voltage conditions, while Fig. 5.29(b) show these results with 50% increase in load current.



(a.1) Method–1 carrier rotation (a.2) Method–2 carrier rotation

(a) with 50% reduction in load current



(b.1) Method–1 carrier rotation (b.2) Method–2 carrier rotation

(b) with 50% increase in load current

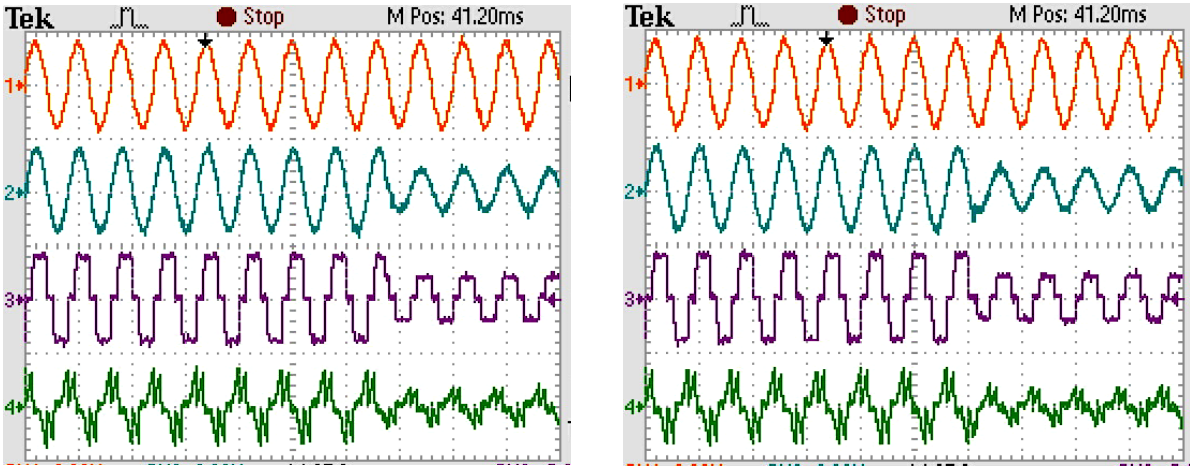
Fig. 5.29: Load perturbation response of D-STATCOM with *RL* load on the dc side of a phase-controlled rectifier with method–1 and method–2 carrier rotation techniques under normal source voltage conditions.

In Fig. 5.29(a), the load current rms value is decreased from 3.3 A to 1.7 A and the corresponding change in the source current are from 2.9 A to 1.5 A in method–1 and 2.8 A to 1.4 A in method–2 carrier rotation technique respectively. It is also observed that the change in source current is very smooth in both carrier rotation techniques, which ensured the fast dynamic response of the controller. In Fig. 5.29(b), the load current rms value is increased from 1.7 A to 3.3 A and the corresponding change in the source current are from 1.5 A to 2.9

A in method–1 and 1.4 A to 2.8 A in method–2 carrier rotation technique respectively. The change in source current is found to be very smooth in both cases, which ensured the fast dynamic response of the controller.

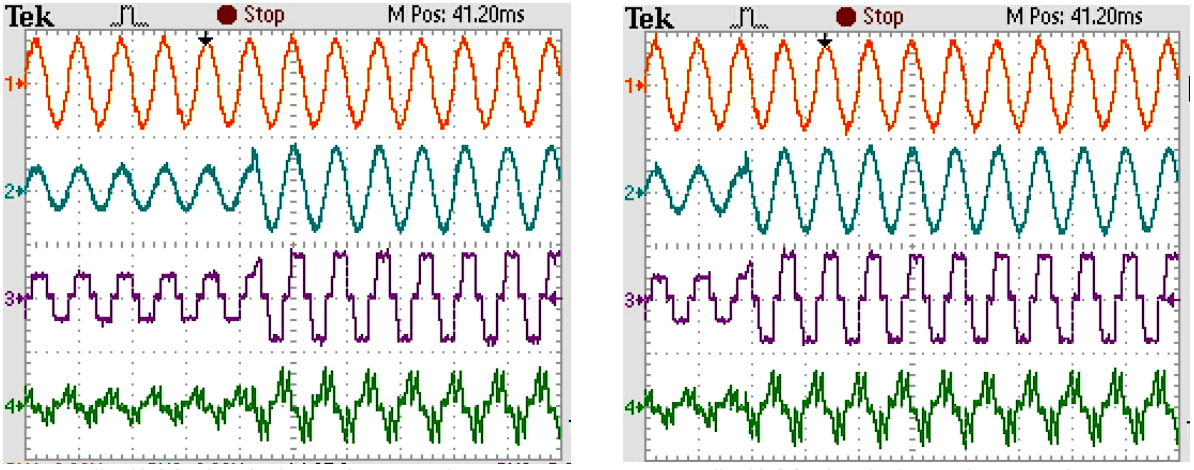
5.5.3.2 Transient Performance with Distorted Voltage Conditions

The transient performance of the compensator with distorted voltage conditions as given in section 5.5.2 are presented below. Fig. 5.30(a) show the experimental results of source voltage, source current after compensation, load current and compensating currents for phase–*a* with method–1 and method–2 carrier rotation techniques with 50% reduction in the load current under normal source voltage conditions, while Fig. 5.30(b) show these results with 50% increase in load current.



(a.1) Method–1 carrier rotation (a.2) Method–2 carrier rotation

(a) with 50% reduction in load current



(b.1) Method–1 carrier rotation (b.2) Method–2 carrier rotation

(b) with 50% increase in load current

Fig. 5.30: Load perturbation response of D-STATCOM with *RL* load on the dc side of a phase-controlled rectifier with method–1 and method–2 carrier rotation techniques under distorted source voltage conditions.

In Fig. 5.30(a), the load current rms value is decreased from 3.4 A to 1.6 A and the corresponding change in the source current are from 2.9 A to 1.5 A in method–1 and 2.8 A to

1.5 A in method–2 carrier rotation technique respectively. It is also observed that the change in source current is very smooth in both carrier rotation techniques, which demonstrated the fast dynamic response of the controller under distorted voltage conditions.

In Fig. 5.30(b), the load current rms value is increased from 1.6 A to 3.4 A and the corresponding change in the source current are from 1.5 A to 2.9 A in method–1 and 1.5 A to 2.8 A in method–2 carrier rotation technique respectively. In this case also the observed change in source current is very smooth in both cases, which again demonstrated the fast dynamic response of the controller under distorted voltage conditions.

Overall, a smooth control of the source current with change in load current ensures the effectiveness of the compensator in both normal and distorted voltage conditions transient conditions.

5.5.4 Balancing of Capacitor Voltages

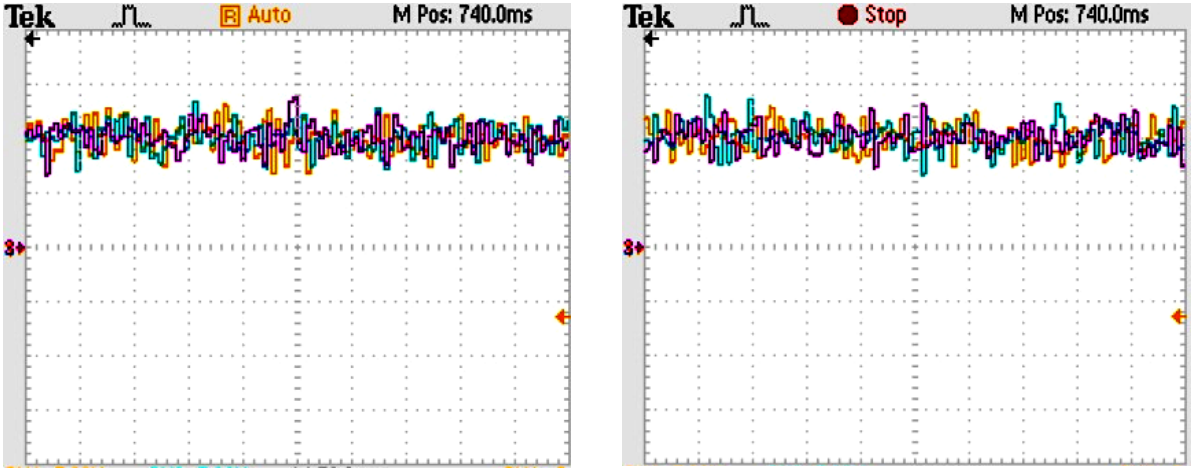
In order to validate the efficacy of dc voltage controller and carrier rotation techniques for balancing the capacitor voltages of the individual H-bridge cells during steady-state and transient conditions, suitable experimental studies are conducted. In these experimental studies, a phase-controlled rectifier operated at a firing angle of 30º with *RL* load on its dc side is considered as a non-linear load. The experimental studies are conducted for the both carrier rotation techniques and the relevant discussions are presented below.

5.5.4.1 Performance under Steady-state Conditions

The steady-state behaviour of capacitor voltages of H-bridge cells for basic LSPWM, method–1 and method–2 carrier rotation techniques are shown in Fig. 5.31. In Fig. 5.31, left-hand side waveforms show the individual capacitor voltages v_{a1}, v_{a2} and v_{b1} while the right-hand side waveforms show the capacitor voltages v_{b2}, v_{c1} and v_{c2} (see Fig. 5.2). The scales of these waveforms are: X-axis: 10 ms/div., Y-axis: 30 V/div. It is to be noted that the dc voltage reference of individual capacitor is kept at 60 V.

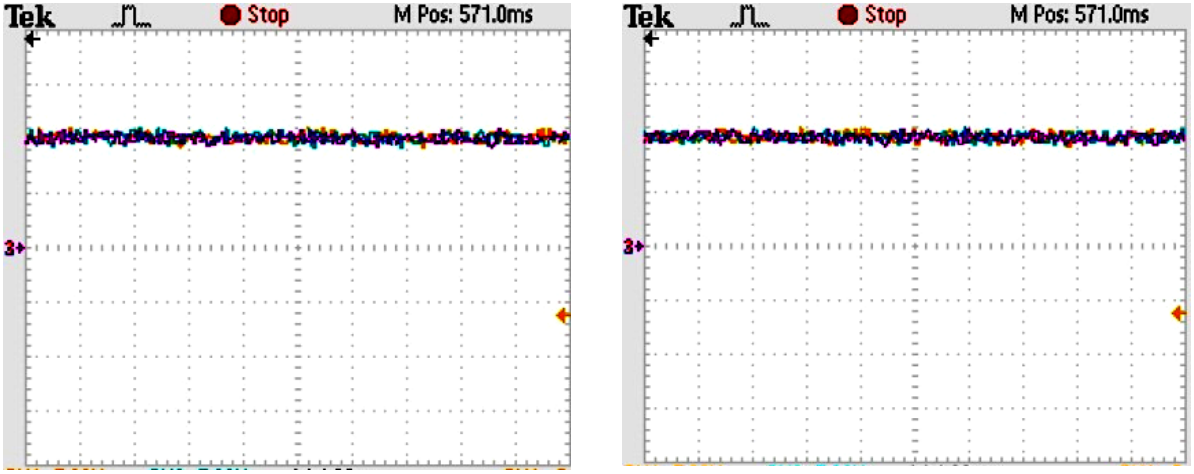
In Fig. 5.31(a) it is observed that with basic LSPWM technique, a large ripple content in the capacitor voltages is present. The maximum peak-to-peak ripple in the individual dc voltages of the capacitors of the H-bridges is around 19 V which affects the performance of the D-STATCOM. However, from Fig. 5.31(b)-(c) it is observed that in both carrier rotation techniques, the capacitor voltages of individual H-bridge cell are well regulated at their reference value of 60 V. This ensures the effectiveness of the dc voltage controller and carrier rotation techniques to balance the capacitor voltages of the H-bridge cells.

With method–1 carrier rotation technique, some small ripple content is observed in the capacitor dc voltages. However, with method–2 carrier rotation technique, the capacitor voltages are almost perfectly balanced. The observed maximum peak-to-peak ripple in the individual dc voltages of the capacitors of the H-bridges in method–1 rotation scheme is around 5 V while for method–2 rotation scheme, it is around 2 V.



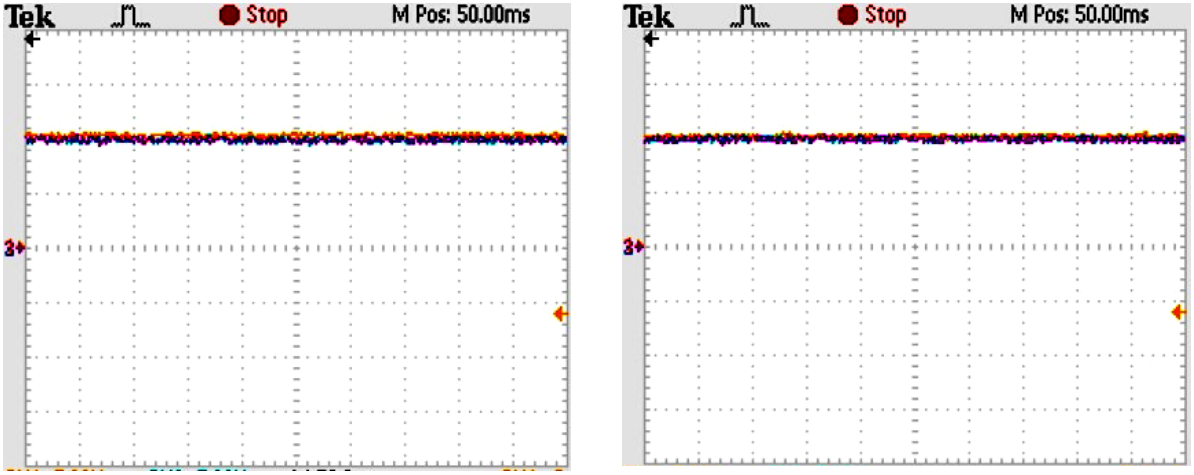
(a.1) Capacitor voltages (v_{a1}, v_{a2} and v_{b1}) (a.2) Capacitor voltages (v_{b2}, v_{c1} and v_{c2})

(a) without carrier rotation (basic LSPWM) technique



(b.1) Capacitor voltages (v_{a1}, v_{a2} and v_{b1}) (b.2) Capacitor voltages (v_{b2}, v_{c1} and v_{c2})

(b) with method–1 carrier rotation technique



(c.1) Capacitor voltages (v_{a1}, v_{a2} and v_{b1}) (c.2) Capacitor voltages (v_{b2}, v_{c1} and v_{c2})

(c) with method–2 carrier rotation technique

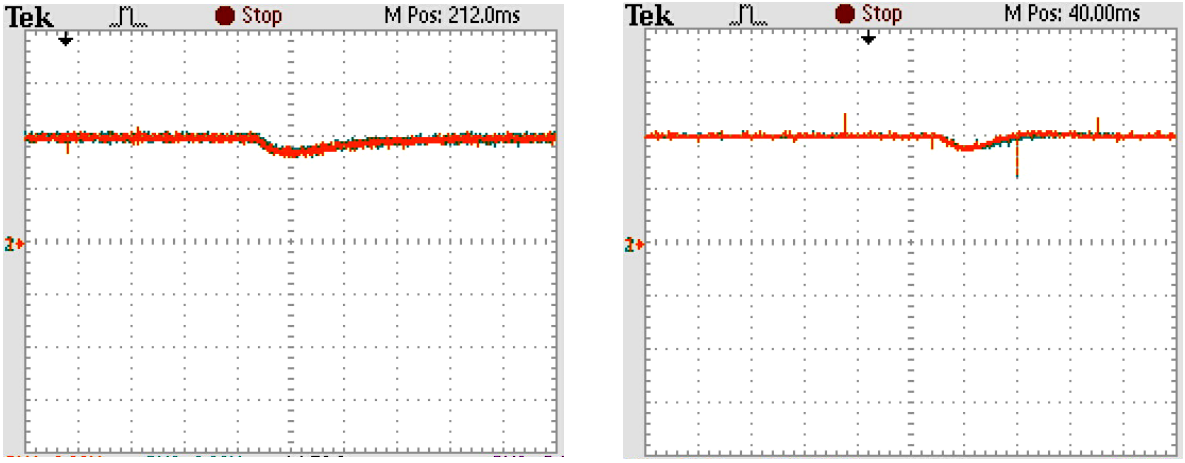
Fig. 5.31: Experimental results of capacitor voltages of the H-bridge cells for a five-level SSBC based 3P3W D-STATCOM.

5.5.4.2 Performance under Transient Conditions

The transient behaviour of capacitor voltages of H-bridge cells for method–1 and method–2 carrier rotation techniques are also studied for step increase and reduction of load current.

(a) *with step increase in load current*

Fig. 5.32 shows the experimental results of dc capacitor voltages with method–1 and method–2 carrier rotation techniques for a 50% increase in the load current. As a three-phase balanced load is considered, the results corresponding to phase–*a* are shown here only. Fig. 5.32(a) shows the individual capacitor voltages v_{a1} and v_{a2} (X-axis: 25 ms/div. and Y-axis: 30 V/div.) with method–1 carrier rotation technique while Fig. 5.32(b) shows these capacitor voltages for method–2 carrier rotation technique (see Fig. 5.2).



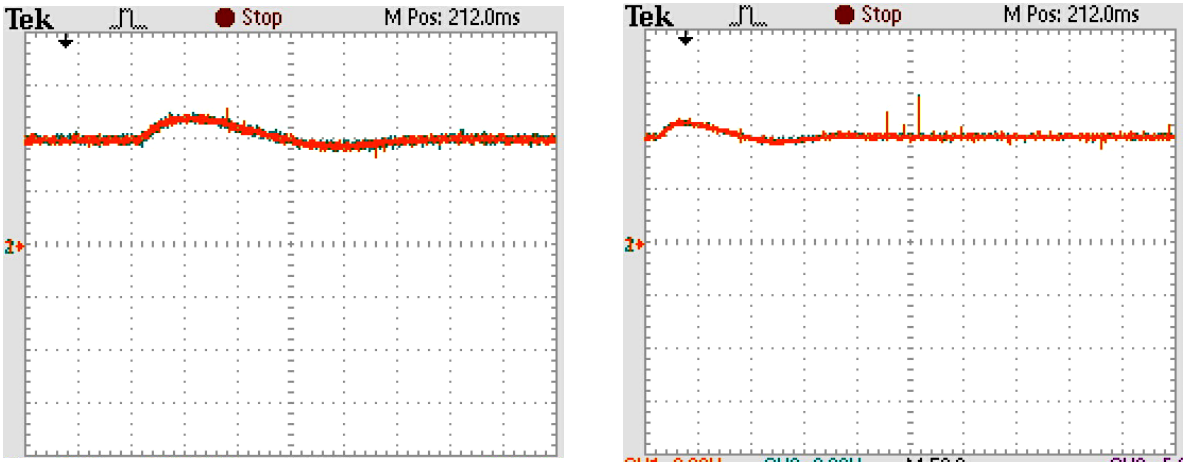
(a) Method–1 carrier rotation technique (b) Method–2 carrier rotation technique

Fig. 5.32: Experimental results of capacitor voltages (v_{a1} and v_{a2}) of the phase–*a* H-bridge cells with 50% increase in load current.

In both cases, at the instant when load current increases, the dc capacitor voltage drops from its reference value to accommodate the enhancement in the load current. This drop in capacitor voltages are restored in 2–3 cycles in method–1 carrier rotation technique but with method–2 carrier rotation technique, the drop in capacitor voltages are restored in 1–2 cycles only, which demonstrates its superior dynamic response.

(b) *with step reduction in load current*

Fig. 5.33 shows the experimental results of dc capacitor voltages with method–1 and method–2 carrier rotation techniques for a 50% reduction in the load current.



(a) Method–1 carrier rotation technique (b) Method–2 carrier rotation technique

Fig. 5.33: Experimental results of capacitor voltages (v_{a1} and v_{a2}) of the H-bridge cell of phase–*a* with 50% decrease in load current.

Fig. 5.33(a) shows the individual capacitor voltages v_{a1} and v_{a2} (X-axis: 25 ms/div. and Y-axis: 30 V/div.) with method–1 carrier rotation technique while Fig. 5.33(b) shows these capacitor voltages for method–2 carrier rotation technique. In both these cases, at the instant when load current decreases, the dc capacitor voltage increases from its reference value to accommodate the reduction in the load current. This enhancement in capacitor voltages are restored in 3–4 cycles in method–1 carrier rotation technique. However, with method–2 carrier rotation technique, this is achieved in 2–3 cycles only, which again demonstrates its superior dynamic response.

Overall, a smooth control of the dc capacitor voltages is achieved with change in load current. The quick regulation of the dc capacitor voltages ensures the effectiveness of dc voltage regulator and carrier rotation techniques in transient condition also.

5.5.5 Comparison with Simulation Results

In the simulation studies presented in Chapter 3, the 3P3W SSBC based transformerless D-STATCOM is realised with a cascade number equal to five and all the simulation studies are carried out at 11 kV. But, due to the constraints of prototype model, the SSBC based inverter is realised with a cascade number equal to two and the experimentations are conducted at a reduced line voltage of 100 V. As the experimental studies are conducted at reduced system parameters, for validating the experimental results, the simulation studies are also carried out with reduced system parameters. The parameters used in the actual simulation studies (given in Chapter 3) and downscaled simulation studies are given in Table 5.3. The downscaled simulation parameters are kept as same as possible to the experimental parameters given in Table 5.2.

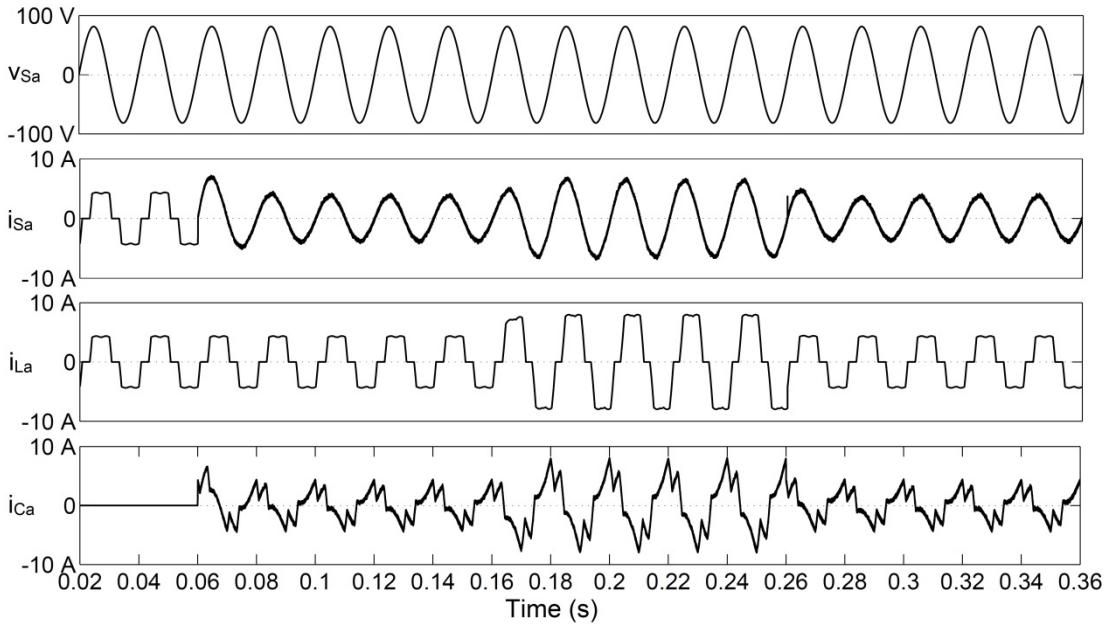
Table 5.3: The parameters used in the simulation studies.

Parameters	**For the downscaled D-STATCOM**
AC line parameters	Three-phase, three-wire, 100 V, 50 Hz
DC bus voltage of D-STATCOM	60 V (for each capacitor in the H-bridge cell)
DC bus capacitance of D-STATCOM	2200 µF (for each capacitor in the H-bridge cell)
D-STATCOM coupling inductor	L_c = 6.4 mH
Commutation inductance	L_f = 1 mH
PWM switching frequency	3 kHz
PI controller parameters	For cluster voltage balancing control: K_p = 0.8, K_i = 1.9 For individual voltage balancing control: K_p = 0.3, K_i = 1.3.
Load	Three-phase uncontrolled rectifier with *RL* and *RC* loads; Three-phase controlled rectifier with *RL* and *RC* loads, firing angle = 30º.
Sampling time	T_s = 50 µs.

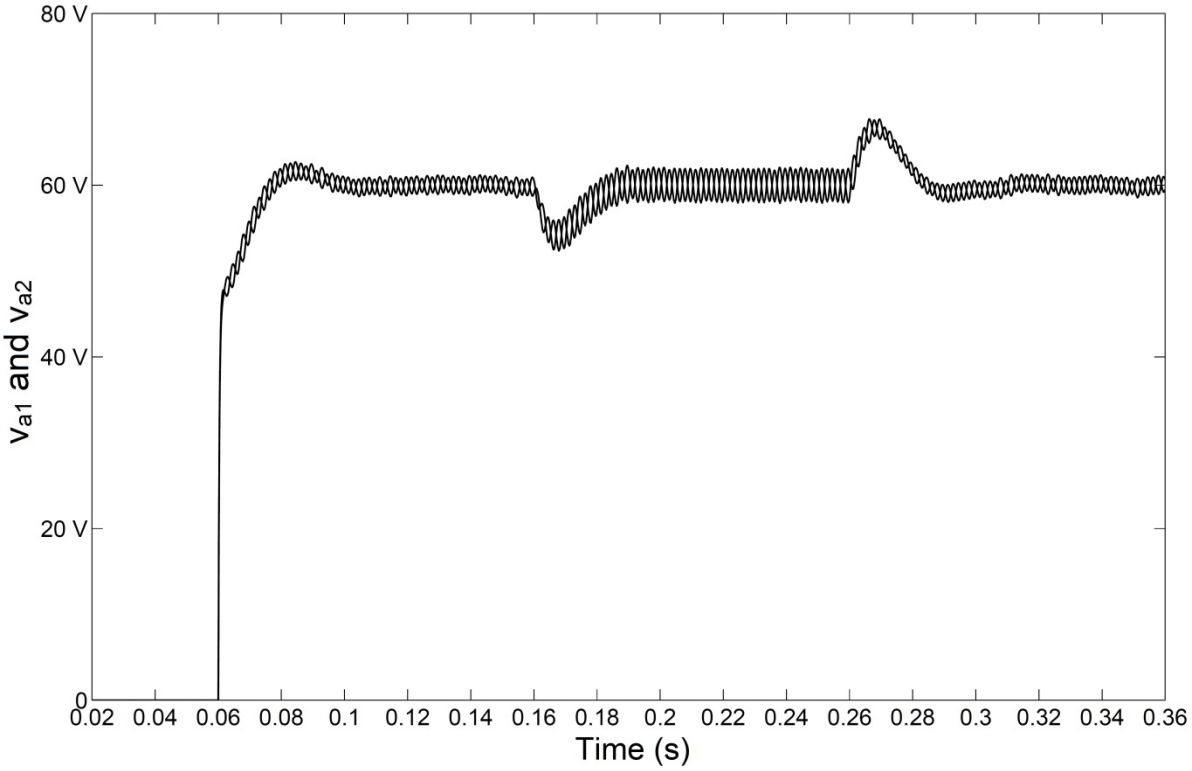
The simulation results with a controlled rectifier operated at a firing angle of 30º with a *RL* load on the dc side is considered as a non-linear load and the simulation studies are shown in Fig. 3.10 and Fig. 3.11 for method–1 and method–2 carrier rotation techniques respectively. Fig. 3.10(a)-(d) shows the simulated waveforms, individual capacitor voltages of the H-bridge cells (v_{a1} and v_{a2}), harmonic spectra of load and source currents respectively with method–1 carrier rotation technique, while Fig. 3.11(a)-(d) shows these results for method–2 carrier rotation technique. In Fig. 3.10(a) and Fig. 3.11(a), the quantities shown are as follows (from top to bottom): trace 1: phase–*a* source voltage (v_{Sa}), trace 2: phase–*a* source current (i_{Sa}), trace 3: phase–*a* load current (i_{La}) and trace 4: phase–*a* current injected by D-STATCOM (i_{Ca}). From both these figures, it can be observed that the simulation results are in good agreement with experimental results for both carrier rotation techniques.

However, in simulations results, the source current THDs are nearly 5% in both carrier rotation techniques and these values are slightly higher than their corresponding experimental values. These enhancements in %THD of source current is due to the large value of sampling time for the simulation study (equal to the sampling time of experimental study). The sampling time of the experimental study is larger than the sampling time of actual simulation study carried out in Chapter 3 (given in Table 5.3). This is due to the fact that, for implementation of control algorithm in dSPACE, requires a minimum sampling time, which is based on the turnaround time (the time difference between triggering and the end of an execution of a task).

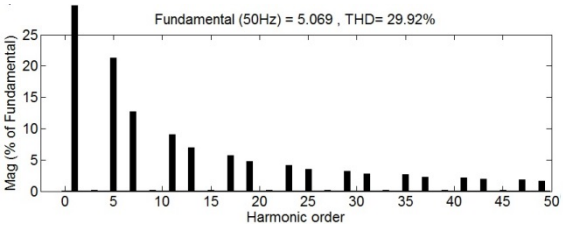
The comparison of experimental and simulation results with different non-linear loads are given in Table 5.4 and Table 5.5 for method–1 and method–2 carrier rotation techniques respectively. Simulation studies with distorted source voltage conditions are also studied. For these simulation studies, harmonics are introduced to the source voltage. The source voltage contains 5% 3rd order and 10% 5th order harmonic components and the resultant THD is 11.18%.



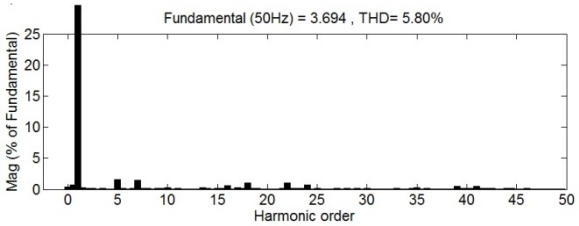
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} and v_{a2})

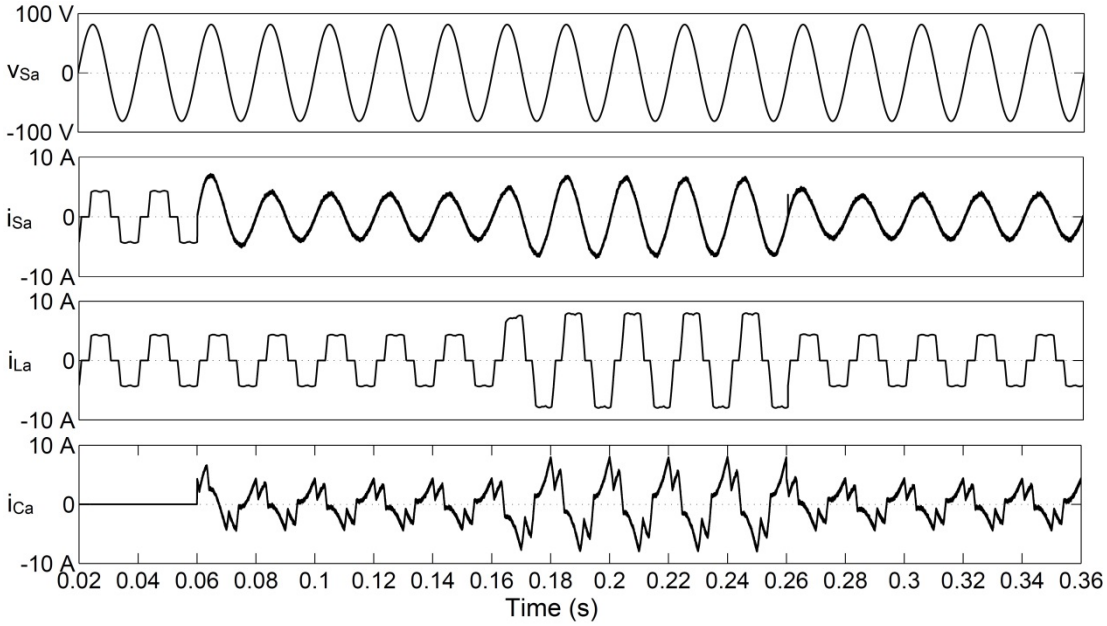


(c) Load current harmonic spectrum

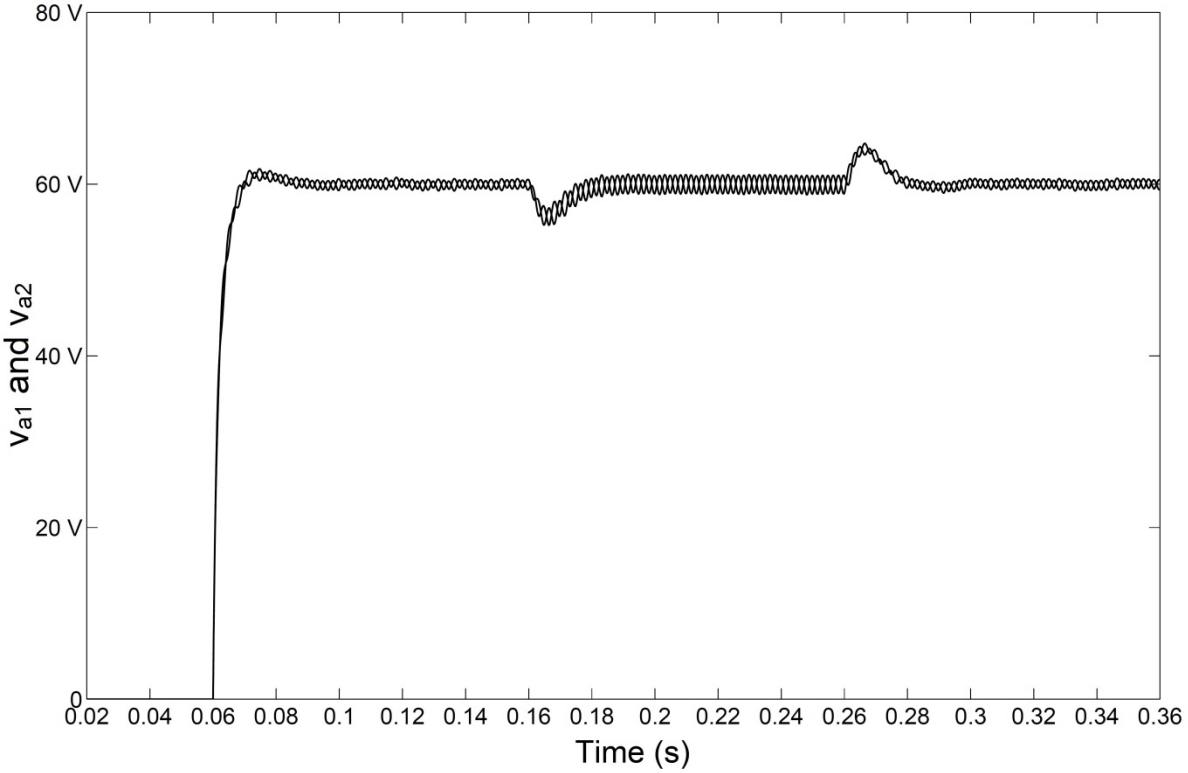


(d) Source current harmonic spectrum

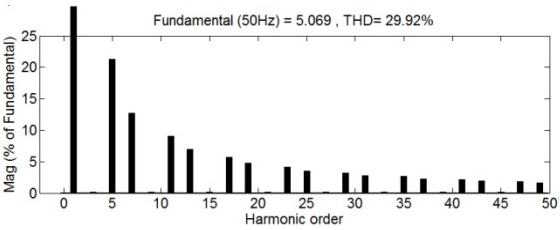
Fig. 5.34: Performance of D-STATCOM with scaled down simulation studies for *RL* load on the dc side of a phase controlled rectifier operated at a firing angle of 30º with method–1 carrier rotation technique and ideal voltage source.



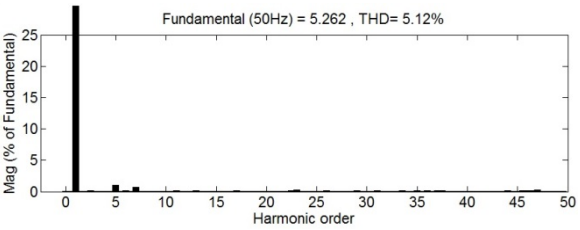
(a) Simulated waveforms



(b) Phase–*a* individual capacitor voltages of the H-bridge cells (v_{a1} and v_{a2})



(c) Load current harmonic spectrum



(d) Source current harmonic spectrum

Fig. 5.35: Performance of D-STATCOM with scaled down simulation studies for *RL* load on the dc side of a phase controlled rectifier operated at a firing angle of 30º with method–2 carrier rotation technique and ideal voltage source.

The comparison of experimental and simulation results under distorted source voltage conditions with different non-linear loads are given in Table 5.6 and Table 5.7 for method–1 and method–2 carrier rotation techniques respectively.

Table 5.4: Comparison of experimental and simulation results with different non-linear loads with method–1 carrier rotation technique under normal source voltage conditions.

Parameter	**Uncontrolled rectifier with *RL* load**		**Uncontrolled rectifier with *RC* load**		**Controlled rectifier with *RL* load**		**Controlled rectifier with *RC* load**	
	Exp.	**Simulation**	**Exp.**	**Simulation**	**Exp.**	**Simulation**	**Exp.**	**Simulation**
Load current (A, rms)	3.3	3.43	3.1	3.09	3.3	3.32	3.6	3.67
% THD of load current	28.7	28.12	33.9	35.10	34.0	29.92	37.8	40.27
Source current (A, rms)	3.5	3.61	3.4	3.51	2.9	3.01	3.2	3.34
% THD of source current	3.9	4.78	3.9	4.91	4.9	5.80	5.0	6.12
Maximum peak-to-peak ripple in dc voltages of H-bridge cells (V)	3.8	2.9	3.3	3.5	5.0	4.2	6.0	4.4

Table 5.5: Comparison of experimental and simulation results with different non-linear loads with method–2 carrier rotation technique under normal source voltage conditions.

Parameter	**Uncontrolled rectifier with *RL* load**		**Uncontrolled rectifier with *RC* load**		**Controlled rectifier with *RL* load**		**Controlled rectifier with *RC* load**	
	Exp.	**Simulation**	**Exp.**	**Simulation**	**Exp.**	**Simulation**	**Exp.**	**Simulation**
Load current (A, rms)	3.3	3.43	3.1	3.09	3.2	3.32	3.6	3.67
%THD of load current	28.7	28.12	33.9	35.10	34.0	29.92	37.8	40.27
Source current (A, rms)	3.6	3.58	3.3	3.55	2.8	3.03	3.3	3.39
%THD of source current	3.5	4.53	3.6	4.79	4.5	5.12	4.9	6.01
Maximum peak-to-peak ripple in dc voltages of H-bridge cells (V)	1.7	1.5	2.6	2.5	2.0	2.2	3.1	2.8

Table 5.6: Comparison of experimental and simulation results with different non-linear loads with method–1 carrier rotation technique under distorted source voltage conditions.

Parameter	Uncontrolled rectifier with *RL* load		Uncontrolled rectifier with *RC* load		Controlled rectifier with *RL* load		Controlled rectifier with *RC* load	
	Exp.	Simulation	Exp.	Simulation	Exp.	Simulation	Exp.	Simulation
Load current (A, rms)	3.2	3.31	3.2	3.16	3.4	3.38	3.6	3.61
% THD of load current	29.1	28.39	32.3	34.78	33.5	30.41	48.3	41.44
Source current (A, rms)	3.3	3.58	3.5	3.42	2.9	3.13	3.3	3.41
% THD of source current	4.7	4.94	4.8	5.09	4.9	5.88	5.3	6.67
Maximum peak-to-peak ripple in dc voltages of H-bridge cells (V)	4.1	3.9	4.4	3.8	5.1	4.8	6.0	6.4

Table 5.7: Comparison of experimental and simulation results with different non-linear loads with method–2 carrier rotation technique under distorted source voltage conditions.

Parameter	Uncontrolled rectifier with *RL* load		Uncontrolled rectifier with *RC* load		Controlled rectifier with *RL* load		Controlled rectifier with *RC* load	
	Exp.	Simulation	Exp.	Simulation	Exp.	Simulation	Exp.	Simulation
Load current (A, rms)	3.2	3.31	3.2	3.16	3.4	3.38	3.6	3.61
%THD of load current	29.1	28.39	32.3	34.78	33.5	30.41	48.3	41.44
Source current (A, rms)	3.5	3.55	3.4	3.47	2.8	3.11	3.4	3.40
%THD of source current	4.4	4.91	4.4	5.03	4.8	5.73	5.2	6.61
Maximum peak-to-peak ripple in dc voltages of H-bridge cells (V)	1.6	1.8	2.9	2.3	2.1	2.4	3.4	3.1

From these tables it can be observed that the simulation results are in good agreement with the experimental results under all source voltage conditions. The increase in %THD of source currents is due to the large value of sampling time of the simulation as explained earlier. However, overall results prove that the control algorithm works independently of system voltage and the cascade number of SSBC inverter with efficiency.

5.6 Performance Investigation of Reduced Rating 3P4W Hybrid D-STATCOMs

In Chapter 4, two following types of 3P4W hybrid D-STATCOMs are proposed for the simultaneous compensation of source current harmonics, reactive power, load balancing and neutral current compensation.

1. A 3P4W hybrid D-STATCOM with zigzag-delta transformer, 3P3W D-STATCOM and shunt connected single-phase APF (as shown in Fig. 4.4).
2. A 3P4W hybrid D-STATCOM with T-connected transformer, 3P3W D-STATCOM and shunt connected single-phase APF (as shown in Fig. 4.20).

However, to further verify the simulation studies with experimental studies, the prototype for the zigzag-delta transformer based topology is developed only due to practical limitations. The details of the development and experimental studies of 3P4W hybrid D-STATCOM with zigzag-delta transformer, 3P3W D-STATCOM and shunt connected single-phase APF are given below.

A 3P4W hybrid D-STATCOM with zigzag-delta transformer, 3P3W D-STATCOM and *shunt connected single-phase APF*

In this prototype, the zigzag-delta transformer is realised by using three single-phase, three-winding transformers (of 3 kVA, 115/115/115 V) and the 3P3W D-STATCOM is realised by using five-level SSBC based inverter. The single-phase APF is realised by using full H-bridge cell with the same IGBT switches (IRG4PH40KD) used in the five-level SSBC based inverter. The dc bus voltage of single-phase APF is maintained at 20 V by using a regulated power supply. The value of the dc bus capacitor of each individual H-bridge in 3P3W D-STATCOM is selected as 2200 μF and the dc bus voltage of each H-bridge is regulated at 60 V. The control algorithm is implemented on dSPACE DS1006 R&D controller board. The complete schematic diagram for the realisation of 3P4W hybrid D-STATCOM is shown in Fig. 5.36. For real-time implementation of control algorithms of 3P3W D-STATCOM and single-phase APF on dSPACE–DS1006, the required parameters such as source voltage, load current, 3P3W D-STATCOM currents, dc capacitor voltages and zigzag neutral current (i_{zn}) are measured and given as an input to the dSPACE through its ADC channels. By using the RTW of MATLAB and RTI feature of dSPACE–DS1006, the Simulink models of the controllers of the 3P3W D-STATCOM and single-phase APF are executed. The master bit I/O is used to generate the required gate pulses for 3P3W D-STATCOM and single-phase APF. The generated gate pulses are given to the individual IGBTs via isolation and dead-band circuits. The developed hybrid D-STATCOM is tested for reactive power compensation, harmonic elimination, load balancing and neutral current compensation in the presence of an unbalanced and non-linear reactive load. The experimental results are presented for both normal and distorted utility voltage conditions and the parameters used in the experimental studies are given in Table 5.8.

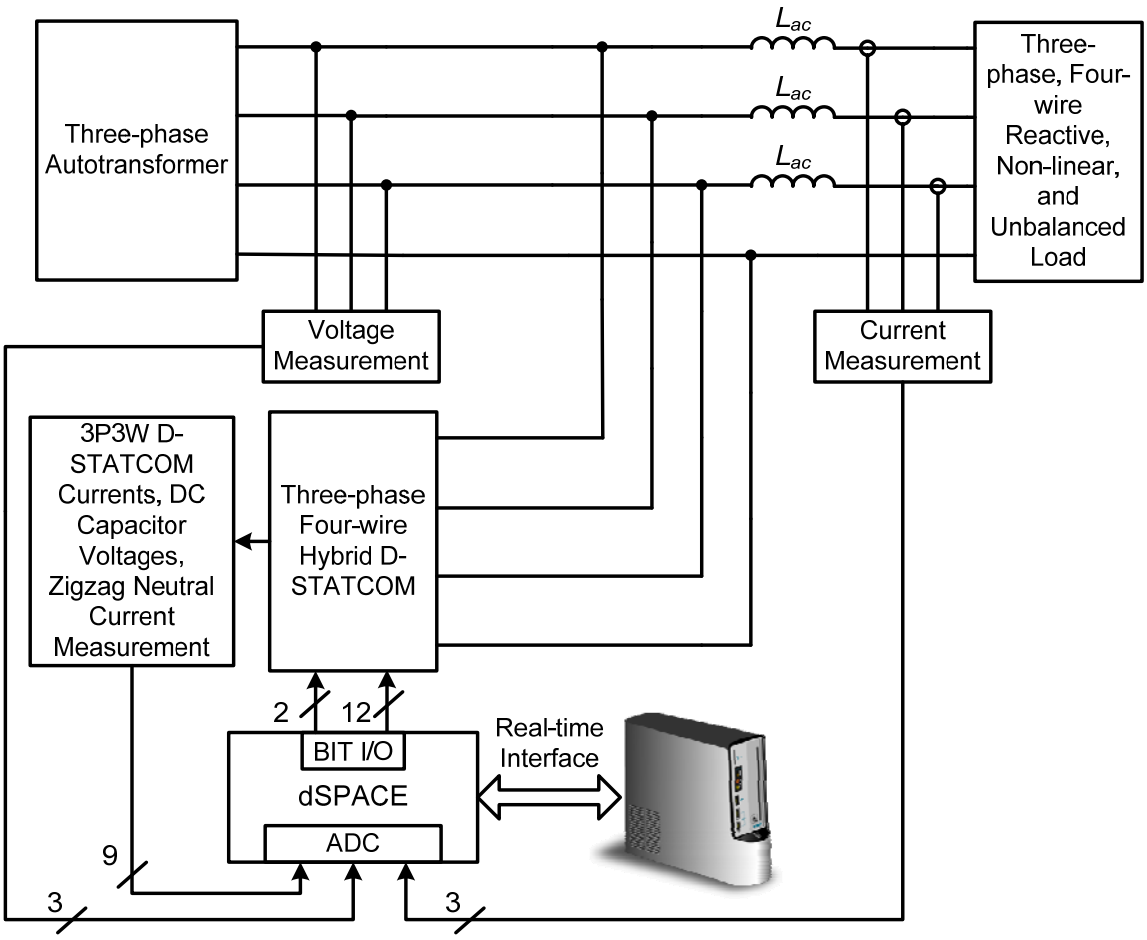


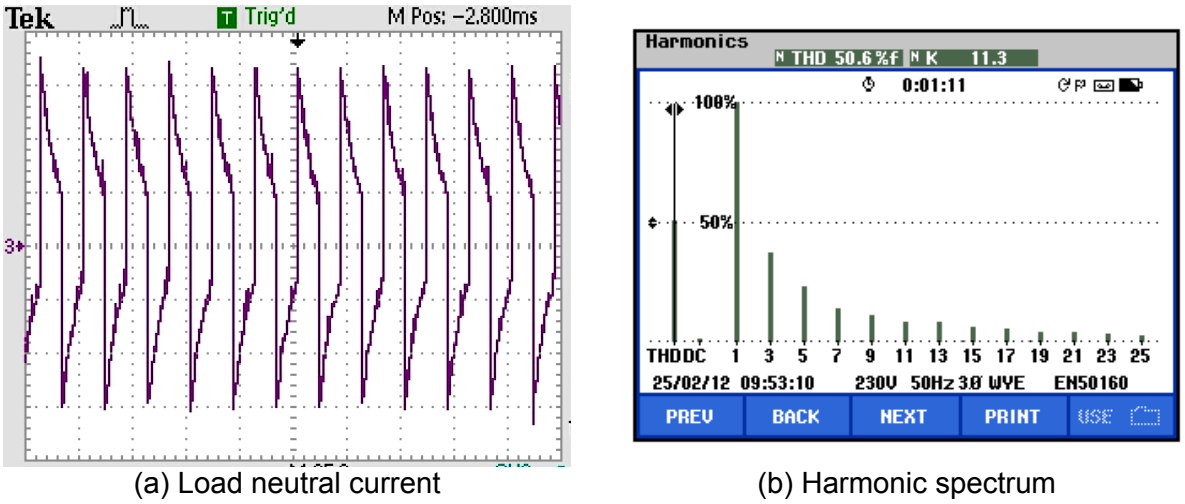
Fig. 5.36: Schematic diagram for the implementation of 3P4W hybrid D-STATCOM.

Table 5.8: Parameters used for the experimentation of 3P4W hybrid D-STATCOM.

Parameter	**Value**
AC line voltage	Three-phase, four-wire, 100 V, 50 Hz
DC bus voltage of D-STATCOM	60 V (for each capacitor in the H-bridge cell)
DC bus voltage of single-phase APF	20 V
DC bus capacitance of D-STATCOM	2200 µF, 450 V (for each capacitor in the H-bridge cell)
D-STATCOM coupling inductor	L_c = 6.4 mH
Commutation inductance	L_{ac} = 1 mH
Single-phase APF output inductor	L_f = 0.7 mH
PWM switching frequency for 3P3W and single-phase inverter	3 kHz
Zigzag-delta transformer	Three single-phase three-winding transformers (3 kVA, 115/115/115 V)
PI controller parameters	For cluster voltage balancing control: K_p = 0.9, K_i = 0.67 For individual voltage balancing control: K_p = 1.0, K_i = 1.1.
Load	Three-phase controlled rectifier with *RL* load, firing angle ≈ 15°, commutation inductance = 1 mH; single-phase uncontrolled rectifier with *RL* load connected between the phase–*a* and the neutral, commutation inductance = 1 mH; single-phase lamp load between the phase–*b* and the neutral.
Sampling time	T_s = 60 µs

5.6.1 Experimental Results with Normal Utility Voltage Conditions

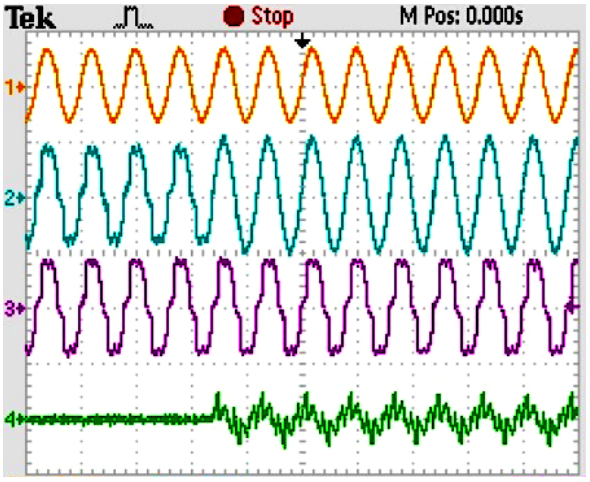
Fig. 5.37(a) shows the experimentally obtained load neutral current (X-Axis: 25 ms/div. and Y-Axis: 1 A/div.) caused by the operation of non-linear load on a 3P4W system while Fig. 5.37(b) shows the harmonic spectra of the load neutral current. The load neutral current contains all odd-order harmonics with dominant third-order harmonic component and the resulting THD is 50.6%.



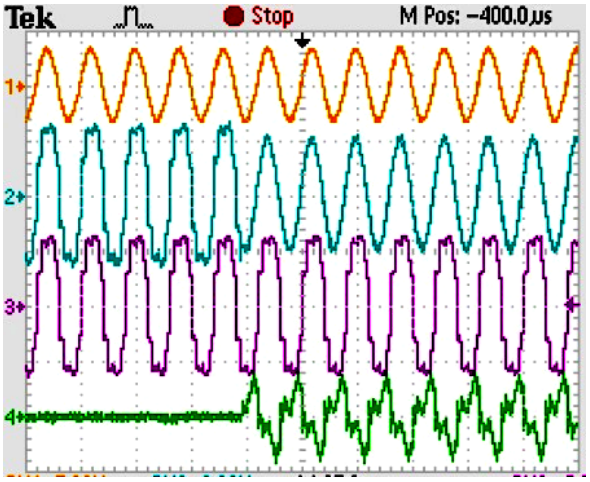
(a) Load neutral current (b) Harmonic spectrum

Fig. 5.37: Waveform of load neutral current and its harmonic spectrum under normal voltage condition.

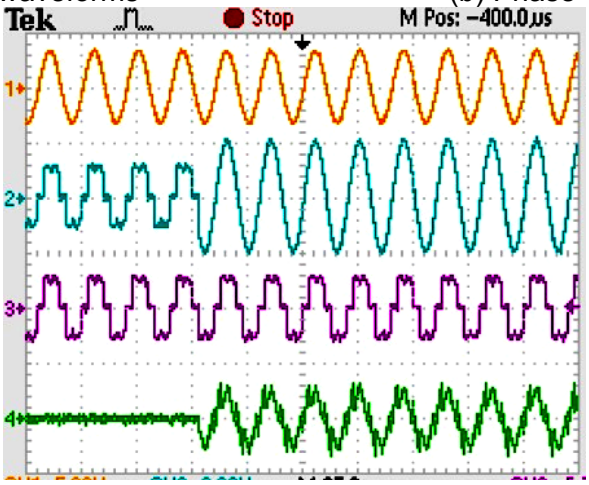
The source voltage, source current after compensation, load current and compensating currents before and after compensation with 3P4W D-STATCOM for phase *a*, *b* and *c* are shown in Fig. 5.38(a)–(c) respectively. In these figures and figures showing similar waveforms, the different waveforms are identified as; trace-1: source voltage (X-Axis: 25 ms/div. and Y-Axis: 150 V/div.); trace- 2: source current after compensation (X-Axis: 25 ms/div. and Y-Axis: 5 A/div.); trace-3: load current (X-Axis: 25 ms/div. and Y-Axis: 5 A/div.) and trace-4: compensating current injected by the zigzag-delta transformer (X-Axis: 25 ms/div. and Y-Axis: 5 A/div.). From Fig. 5.38 it is observed that at the instant when 3P4W D-STATCOM is switched 'ON', the source currents become balanced and sinusoidal and in phase with their respective voltage waveforms.



(a) Phase–*a* waveforms



(b) Phase–*b* waveforms



(c) Phase–*c* waveforms.

Fig. 5.38: Switching-in response of the 3P4W D-STATCOM.

The source voltage, source current after compensation, load current and compensating currents for phase *a*, *b* and *c* under steady-state conditions (when 3P4W D-STATCOM is kept 'ON') are shown in Fig. 5.39(a)–(c), respectively. Since the load is unbalanced, the load currents in trace-3 of Fig. 5.39(a)-(c) are different. Fig. 5.39(d) shows the source neutral current before compensation (X-Axis: 25 ms/div. and Y-Axis: 1 A/div.). The source neutral current when only zigzag transformer is connected (i.e. switch *S* is closed) is shown in Fig. 5.39(e) (X-Axis: 25 ms/div. and Y-Axis: 1 A/div.) From Fig. 5.39(e) it is observed that, when zigzag transformer is 'ON', the source neutral current is reduced but it is not completely eliminated. When switch *S* is open, the single-phase APF is enabled and the source neutral current almost becomes zero. The source neutral current when single-phase APF is connected is shown in Fig. 5.39(f) (X-Axis: 50 ms/div. and Y-Axis: 1 A/div.) From Fig. 5.39 it is observed that the reactive power compensation, harmonic elimination, load balancing and neutral current compensation are achieved by the 3P4W hybrid D-STATCOM. When single-phase APF is 'ON' the source neutral current becomes zero and under this condition, the utility is supplying balanced three-phase currents only. The experimental results are observed to be in good agreement with the simulation results.

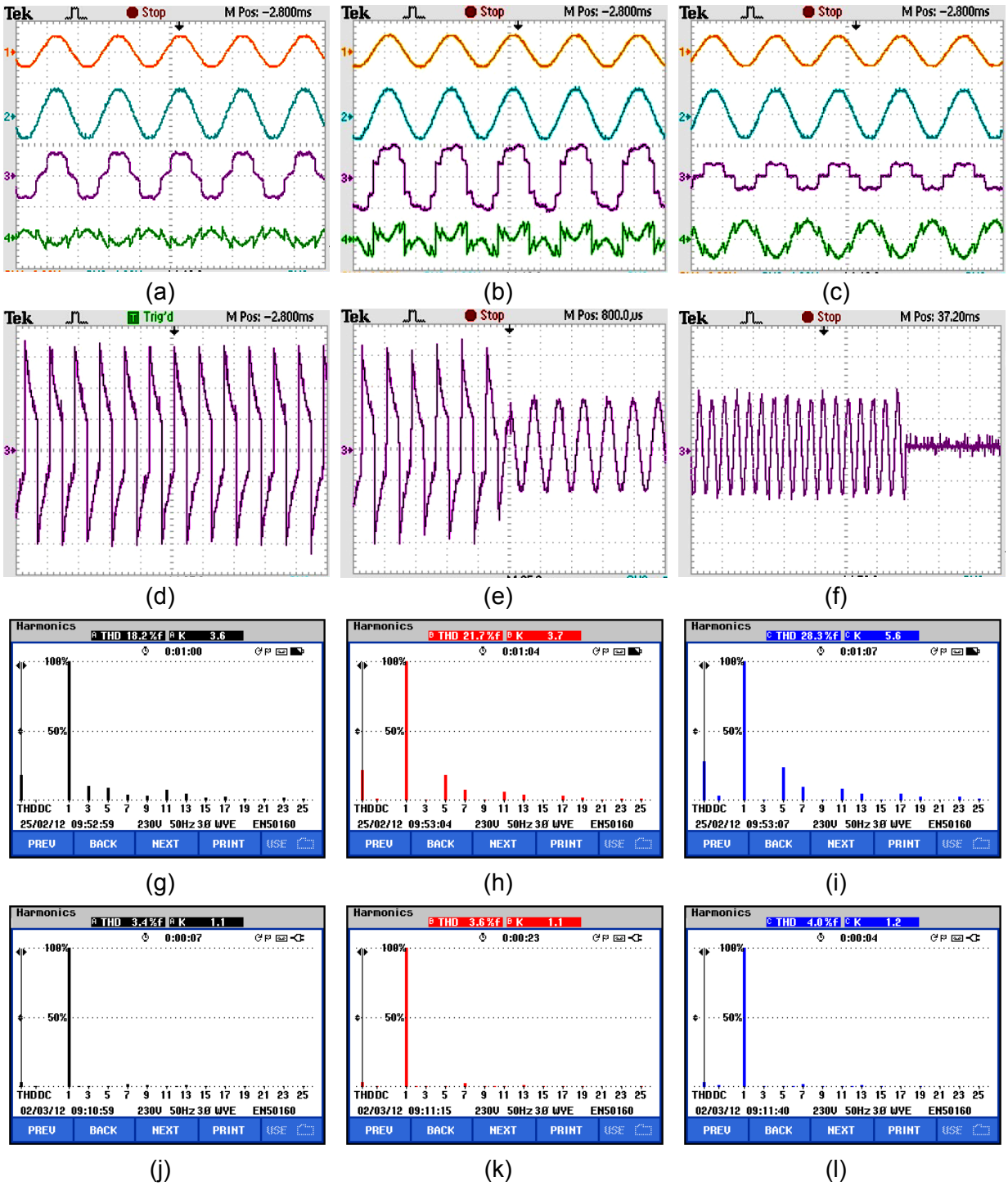
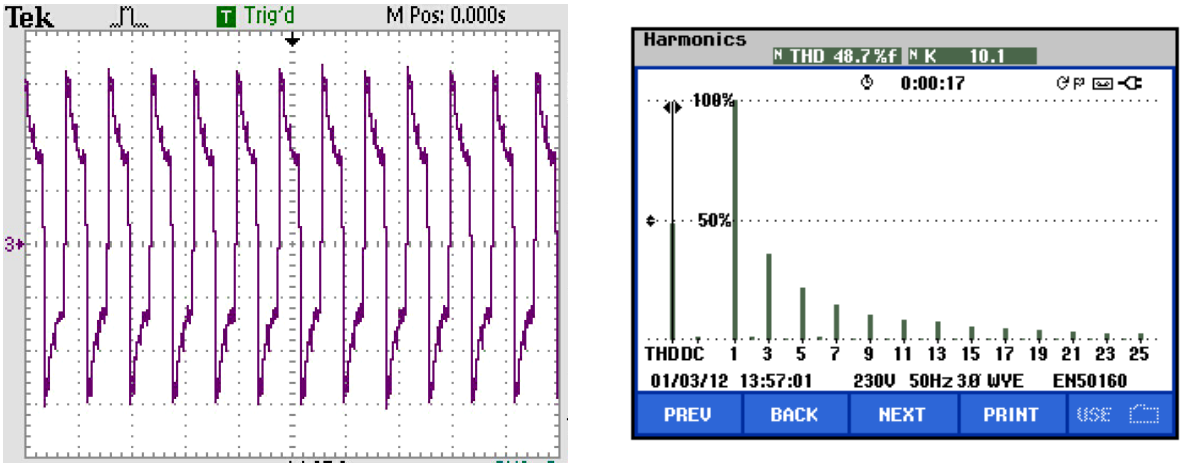


Fig. 5.39: Experimental waveforms obtained with non-linear unbalanced load for 3P4W D-STATCOM with normal voltage.

The harmonic spectra of load current for phases *a*, *b* and *c* are shown in Fig. 5.39(g)–(i) respectively. Before compensation, the THDs of the load currents are 18.2%, 21.7% and 28.3% respectively and the input power factor of the source is 0.88 (lagging). The harmonic spectra of source current after compensation for phases *a*, *b* and *c* are shown in Fig. 5.39(j)–(l) respectively. The THDs of the compensated source currents are 3.4%, 3.6% and 4.0% respectively, which are well within the limits of IEEE–519–1992 standard recommended value of 5%. The source displacement and power factor after compensation are almost unity.

5.6.2 Performance with Unbalanced/distorted Utility Voltage Conditions

The adopted hybrid D-STATCOM is also tested for reactive power compensation, harmonic elimination, load balancing and neutral current compensation in the presence of unbalanced/distorted voltage conditions. Fig. 5.23 shows the three-phase unbalanced/distorted source voltages, while the harmonic spectra of source voltage are shown in Fig. 5.24(a)–(c). The THDs of the source voltages are 7.2%, 8.5% and 6.9% respectively and the %VUF of source voltage is 2.3. Fig. 5.40(a) shows the experimentally obtained load neutral current (X-Axis: 25 ms/div. and Y-Axis: 1 A/div.) caused by the operation of non-linear load on a 3P4W system under unbalanced/distorted utility voltage conditions while Fig. 5.40(b) shows the harmonic spectrum of load neutral current. The load neutral current contains a dominant third-order harmonic component with a resulting THD of 48.7%.



(a) Load neutral current (b) Harmonic spectrum

Fig. 5.40: Waveform of load neutral current and its harmonic spectrum under distorted voltage condition.

The source voltage, source current after compensation, load current and compensating currents for phase *a*, *b* and *c* under steady-state condition (when 3P4W D-STATCOM is kept 'ON') are shown in Fig. 5.41(a)–(c), respectively. Fig. 5.41(d) shows the source neutral current before compensation (X-Axis: 25 ms/div. and Y-Axis: 5 A/div.). The source neutral current when only zigzag-delta transformer is connected (i.e. switch *S* is closed) is shown in Fig. 5.41(e) (X-Axis: 25 ms/div. and Y-Axis: 5 A/div.). From Fig. 5.41(e) it can be observed that when zigzag-delta transformer only acts as a compensator, the neutral current on the source is increased. The enhancement in the neutral current is due to the existence of zero-sequence harmonics in source voltage. But, when switch *S* is open, the single-phase APF is enabled and the source neutral current becomes almost zero. The source neutral current when single-phase APF is connected is shown in Fig. 5.41(f) (X-Axis: 25 ms/div. and Y-Axis: 5 A/div.). From Fig. 5.41 it is observed that the compensator performs adequately under unbalanced/distorted voltage conditions also. The harmonic spectra of load current for

phases *a*, *b* and *c* are shown in Fig. 5.41(g)–(i) respectively. Before compensation, the THDs of the load currents are 18.9%, 21.7% and 30.0% respectively, and the power factor of the source is 0.84 (lagging). The harmonic spectra of source current after compensation for phases *a*, *b* and *c* are shown in Fig. 5.41(j)–(l) respectively. The THDs of the compensated source currents are reduced to 4.7%, 4.3% and 4.5% respectively, which proves the performance of the compensator under unbalanced/distorted source voltage conditions. The source displacement and power factor after compensation are almost unity.

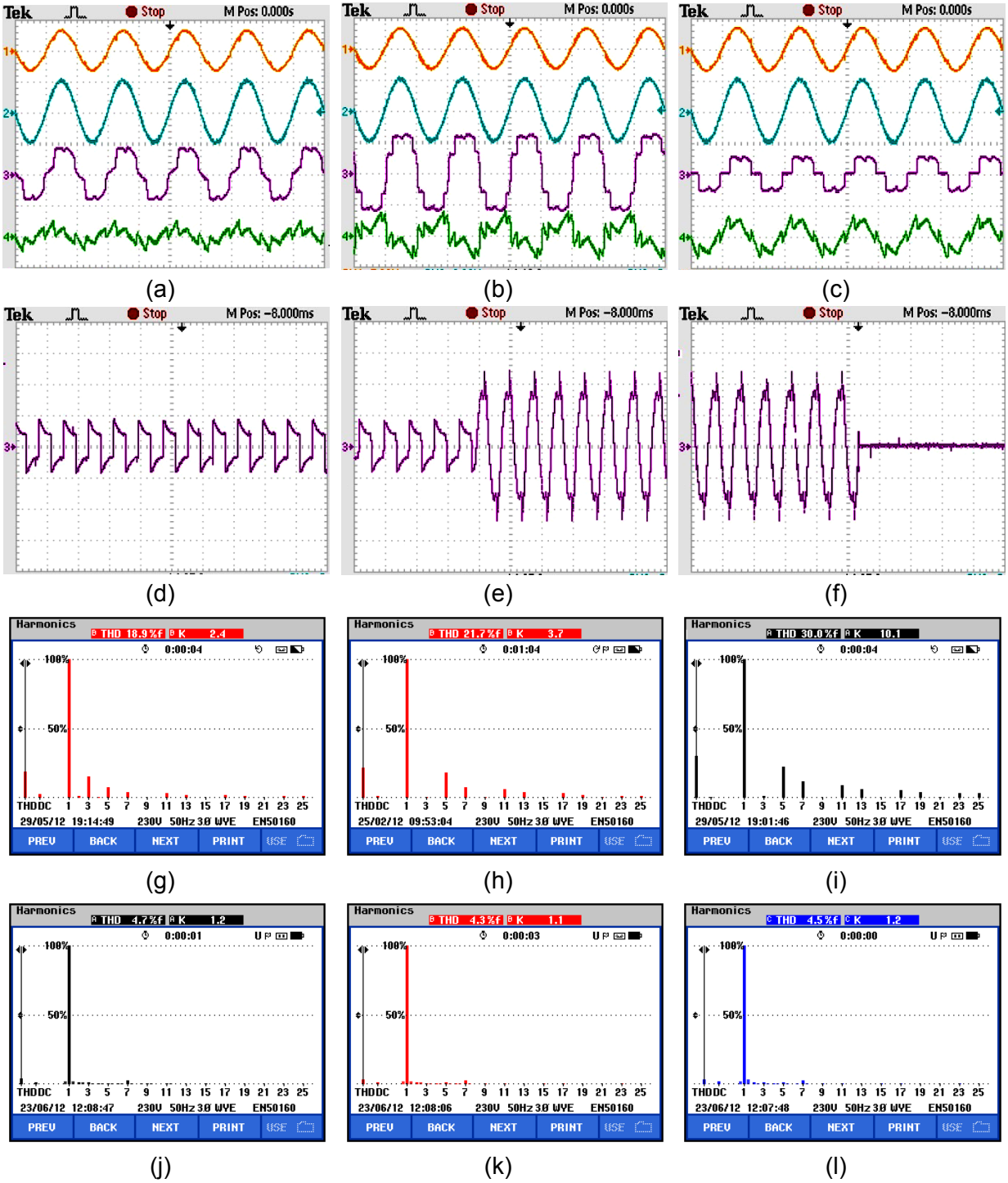


Fig. 5.41: Experimental waveforms obtained with non-linear unbalanced load with 3P4W D-STATCOM under distorted source voltage.

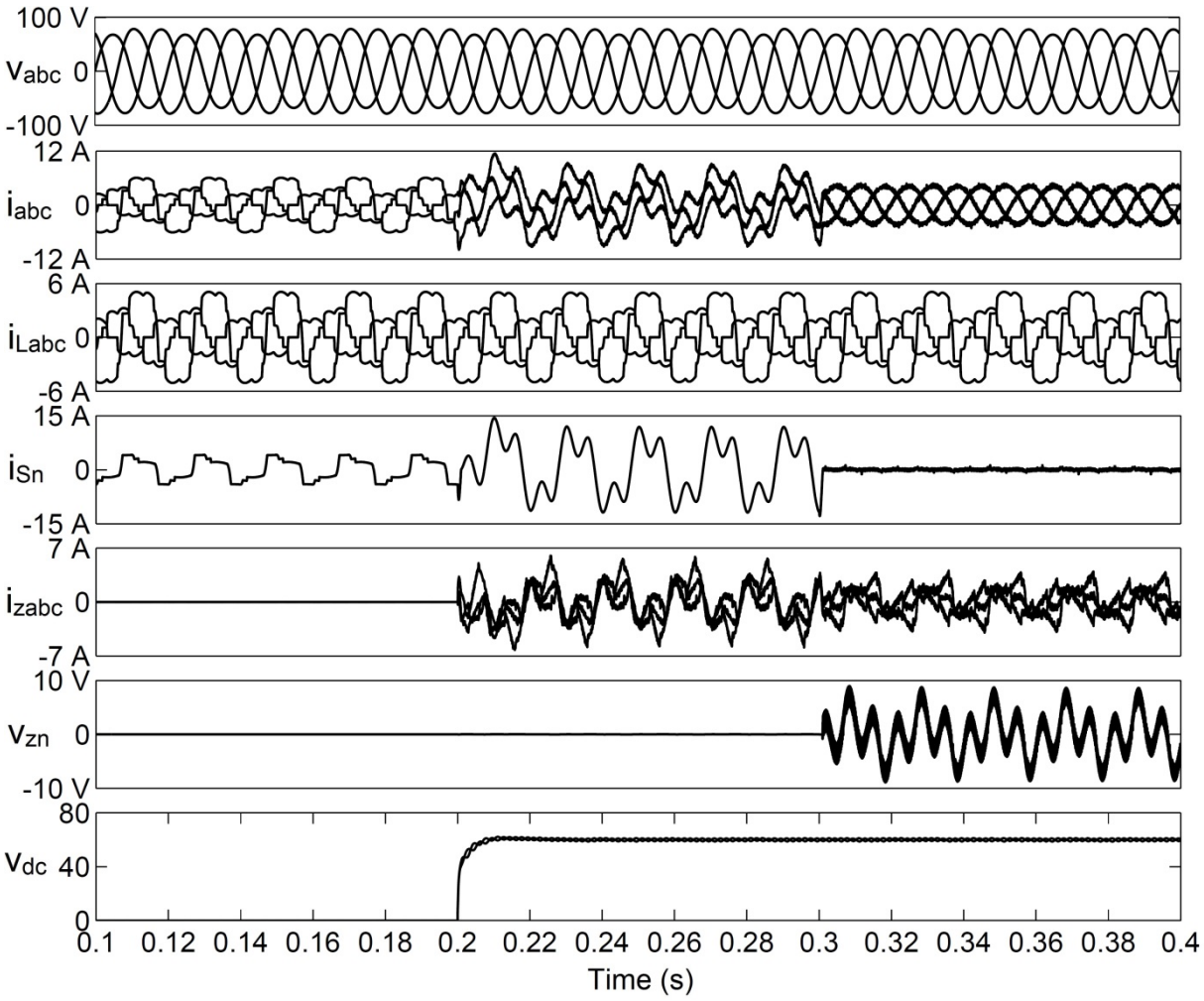
5.6.3 Comparison with Simulation Results

In the simulation studies presented in Chapter 4, the 3P4W hybrid D-STATCOM is tested at 415 V. But, due to the constraints involved in the development of prototype model, the experimental studies are conducted at a reduced line voltage of 100 V. As the experimental studies are conducted at reduced system parameters, for validating the experimental results, the simulation studies are also carried out with reduced system parameters. The parameters used in the actual simulation studies (given in Chapter 4) and downscaled simulation studies are given in Table 5.9. The downscaled simulation parameters are kept as same as possible to the experimental parameters given in Table 5.8.

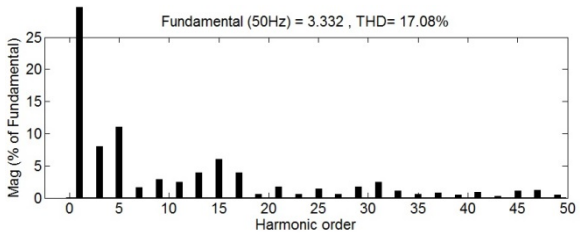
The simulated waveforms, load and source current harmonic spectra with single-phase and three-phase reactive/non-linear loads under unbalanced/distorted utility voltage conditions are shown in Fig. 4.31(a)-(c). From Fig. 4.31, it can be observed that the simulation results are in good agreement with experimental results. Moreover, in simulations results, the source current THDs are reduced below 5%, but their values are slightly higher than their corresponding experimental values. These enhancements in %THD of source currents is due to the large value of sampling time for the simulation study as explained in subsection 5.5.5.

Table 5.9: The parameters used in the downscaled simulation studies.

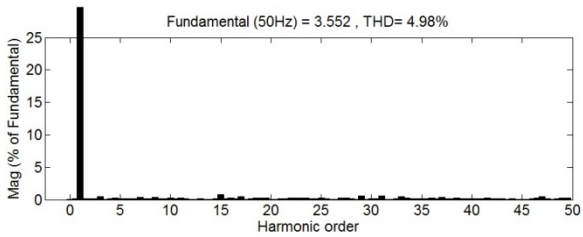
Parameters	**Downscaled 3P4W D-STATCOM**
AC line parameters	Three-phase, three-wire, 100 V, 50 Hz
DC bus voltage of D-STATCOM	60 V (for each capacitor in the H-bridge cell)
DC bus voltage of single-phase APF	20 V
DC bus capacitance of D-STATCOM	2200 μF, 450 V (for each capacitor in the H-bridge cell)
D-STATCOM coupling inductor	L_c = 6.4 mH
Commutation inductance	L_{ac} = 1 mH
Single-phase APF output inductor	L_f = 0.7 mH
PWM switching frequency	3 kHz (Method–2 carrier rotation technique)
PWM switching frequency for single-phase APF	3 kHz
PI controller parameters	For cluster voltage balancing control: K_p = 0.3, K_i = 0.60 For individual voltage balancing control: K_p = 2, K_i = 1.0.
Load	Three-phase uncontrolled rectifier with *RL* and *RC* loads; Three-phase controlled rectifier with *RL* and *RC* loads, firing angle = 30º.
Sampling time	T_s = 60e–6 sec.



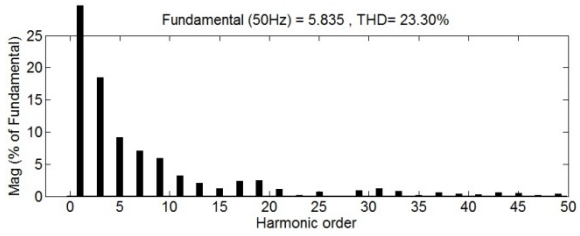
(a) Simulated waveforms



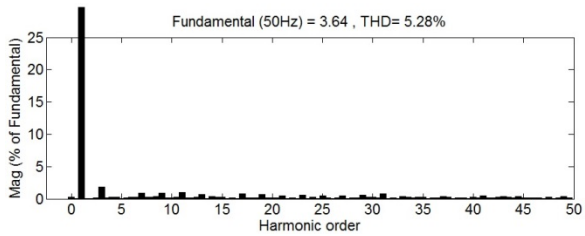
(b.1) Phase–*a* load current harmonic spectrum



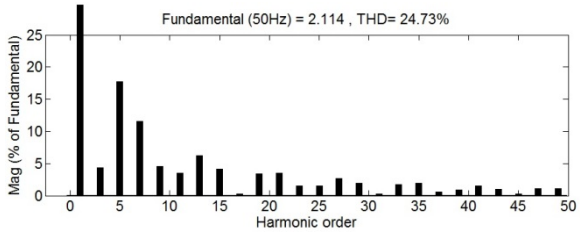
(c.1) Phase–*a* source current harmonic spectrum



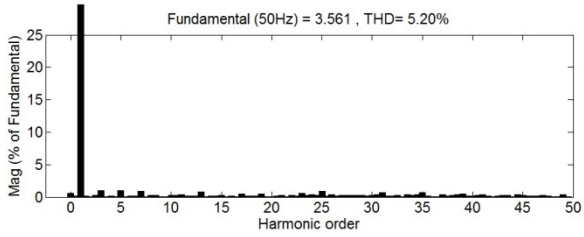
(b.2) Phase–*b* load current harmonic spectrum



(c.3) Phase–*b* source current harmonic spectrum



(b.3) Phase–*c* load current harmonic spectrum



(c.3) Phase–*c* source current harmonic spectrum

Fig. 5.42: The performance of 3P4W hybrid D-STATCOM with downscaled simulation study under unbalanced/distorted utility voltage conditions.

The comparison of experimental and simulation results under normal and unbalanced/distorted utility voltage condition are given in Table 5.10 and Table 5.11 respectively.

Table 5.10: Comparison of experimental and downscaled simulation results under normal utility voltage conditions with 3P4W D-STATCOM.

Parameters	**Experimentation**			**Simulation**		
	phase–*a*	phase–*b*	phase–*c*	phase–*a*	phase–*b*	phase–*c*
Load current (A, rms)	2.6	4.0	1.3	2.711	4.128	1.433
Source current (A, rms)	2.8	2.8	2.7	2.601	2.642	2.595
%THD of load current	18.2%	21.7%	28.3%	17.08%	22.27%	29.61%
%THD of source current after compensation	3.4%	3.6%	4.0%	4.84%	4.74%	4.79%
Load neutral current (A, rms)	3.5 A			3.6 A		
Peak value of source neutral current when switch *S* is closed (A)	1.6 A			1.5 A		
Source neutral current when switch *S* is open (rms, A)	0.2 A			0.214 A		
Peak voltage between transformer neutral and source neutral (V)	3 V			5 V		

Table 5.11: Comparison of experimental and downscaled simulation results under unbalanced/distorted utility voltage conditions 3P4W D-STATCOM.

Parameters	**Experimentation**			**Simulation**		
	phase–*a*	phase–*b*	phase–*c*	phase–*a*	phase–*b*	phase–*c*
Load current (A, rms)	3.2	4.6	1.8	3.145	4.723	1.831
Source current (A, rms)	3.5	3.4	3.5	3.621	3.414	3.569
%THD of load current	18.9%	21.7%	30.0%	17.08%	23.30%	24.73%
%THD of source current after compensation	4.7%	4.3%	4.5%	4.98%	5.28%	5.20%
Load neutral current (A, rms)	3.6 A			3.65 A		
Peak value of source neutral current when switch *S* is closed (A)	13 A			14 A		
Source neutral current when switch *S* is open (rms, A)	0.2 A			0.23 A		
Peak voltage between transformer neutral and source neutral (V)	6.3 V			9.5 V		

From Table 5.10 and Table 5.11 it can be observed that the simulation results are in good agreement with the experimental results. The increase in %THD of source currents is due to the large value of sampling time of the simulation. However, overall results prove that the control algorithm works efficiently and independent of the voltage.

5.7 Conclusion

In this chapter, the detailed descriptions for the design and development of laboratory prototype D-STATCOMs are given. For the developed SSBC based modular multilevel inverter, a cascade number equal to two is assigned and IGBTs are used as switching devices. A DSP DS1006 of dSPACE is used for the real-time implementation of various control algorithms of D-STATCOM topologies in the MATLAB/Simulink environment. The different hardware components as required for the proper operation of experimental set-ups such as pulse amplification, isolation and dead-band circuits, voltage and current sensor circuits, non-linear/reactive loads are designed, developed and interfaced with dSPACE.

The developed power circuit is tested initially as a dc-ac inverter to experimentally validate the efficacy of the carrier rotation techniques. A three-phase lamp load is used as load for the inverter. The line-to-line voltage, phase voltage and harmonic spectrum of line-to-line voltage of the inverter are observed to be almost identical with and without carrier rotation techniques.

The developed prototype is further tested for reactive power compensation and harmonic elimination with different loading and utility voltage conditions. The steady-state and transient performances of the D-STATCOM are found to be satisfactory with both carrier rotation techniques. A smooth control of dc voltages of H-bride cells ensured the effectiveness of the dc voltage controller and carrier rotation techniques. It is also observed that with method–2 carrier rotation technique, a better control in dc voltages of H-bridge cells is achieved. Further, the experimental results are validated with simulation results by using the experimental parameters.

In order to further verify the simulation studies of the proposed hybrid 3P4W D-STATCOMs, laboratory prototype of the adopted compensator topology consisting of five-level SSBC based 3P3W D-STATCOM and a zigzag-delta transformer with single-phase APF is developed. The developed prototype is studied for reactive power compensation, harmonic elimination and neutral current compensation with different loading and utility voltage conditions. From these studies it is observed that the proposed control schemes improve the power quality of the source currents even under distorted/unbalanced utility voltage conditions. Further, the experimental results are validated with simulation results by using the experimental parameters.

CHAPTER 6: CONCLUSION AND FUTURE SCOPE OF RESEARCH

The main conclusions of the presented work and possible future research are summarised in this chapter.

6.1 Conclusion

In this thesis, digitally controlled 3P3W and 3P4W D-STATCOMs are proposed to improve the power quality of the source current waveform and to compensate the load reactive power in 3P3W and 3P4W distribution systems. The major conclusions derived from this work are summarised as follows.

- D-STATCOM is a shunt connected custom power device which is realised by using voltage or current source inverter with necessary passive elements and is connected at PCC. The inverter of the D-STATCOM is controlled to draw the compensating current from the ac power source, such that it cancels the reactive and harmonic current contained in the load current. Since voltage source inverter (VSI) is widely used in industrial applications, it is considered in this thesis.
- Among different topologies of VSI for high-power, medium-voltage D-STATCOM proposed in the literature, single-star bridge cells based modular multilevel cascade inverter (SSBC-MMCI) is found to be the best suitable topology for D-STATCOM. The voltage control methods for the chosen inverter topology are studied and the unequal device conduction periods of level-shift PWM (LSPWM) technique is addressed by two carrier rotating techniques. Simulation results are presented for 5 and 11-level SSBC based inverter. From these results it is observed that the output voltages synthesised by these two carrier rotation techniques are almost identical with those obtained by the basic LSPWM technique. The THD values and side-band harmonic frequencies of these carrier rotation techniques are observed to be almost identical. The device conduction periods corresponding to the adopted carrier rotation techniques are calculated by the proposed algorithms.
- The adopted carrier rotation techniques are further validated by developing a five-level SSBC based modular multilevel inverter. The different hardware components required for the proper operation of experimental set-ups such as pulse amplifier, isolation and dead-band circuits, voltage and current sensor circuits, non-linear/reactive loads are designed and developed. A DSP DS1006 of dSPACE is used for the real-time implementation of the control scheme of the inverter. The developed power circuit is tested as a dc-ac inverter to validate the efficacy of the carrier rotation techniques. The experimentally obtained line-to-line and line-to-neutral voltages and their corresponding harmonic spectra of the inverter are observed to be in good agreement with simulation results.
- A SSBC based transformerless PWM D-STATCOM, intended for installation on an 11 kV 3P3W industrial distribution system is proposed. The specific design approach presented

in this work does not require line-frequency transformer and high-power switching devices, therefore the cost and size of the D-STATCOM are reduced. The complete design and simulation results of an 11 kV, 1 MVA and 11-level SSBC based D-STATCOM for harmonic elimination and reactive power compensation in 3P3W distribution system are presented. The control algorithm used in this work not only compensated the reactive power and harmonics generated by the load, but also kept the dc voltages of the H-bridges cells in controlled and balanced state, even during the transient conditions under unbalanced/distorted voltage conditions. The carrier rotation based LSPWM techniques are adopted to control the inverter of the D-STATCOM.

- Extensive simulation results are presented to investigate the performance of the 3P3W D-STATCOM in both steady-state and transient conditions under ideal and distorted source voltages with both carrier rotation techniques. After compensation with D-STATCOM the percentage THDs of source currents are reduced to below 5% and the power factor and the displacement factor on the source side are found to be unity not only in the steady-state condition but also in the transient condition. For further verification, the developed five-level SSBC inverter is used as a power circuit of the D-STATCOM. The D-STATCOM is tested at reduced voltage for reactive power compensation and harmonic elimination with different loading and utility voltage conditions. A DSP (DS1006 of dSPACE) is used for the real-time implementation of the control scheme of the D-STATCOM. The steady-state and transient performances of the D-STATCOM are found to be satisfactory with both carrier rotation techniques. A smooth control of dc voltages of H-bride cells ensured the effectiveness of the dc voltage controller and carrier rotation techniques. It is also observed that with method–2 carrier rotation technique, a better control in dc voltages of H-bridge cells is achieved. Further, the experimental results are validated with simulation results by using the experimental parameters. The overall results prove that the control algorithm works independently of system voltage and the cascade number of SSBC inverter.
- The application of D-STATCOM is extended to 3P4W systems for simultaneous compensation of reactive power, phase harmonic currents, source neutral current and load balancing. To accomplish this, two reduced rating hybrid 3P4W D-STATCOMs are proposed. The complete arrangements considered in these topologies comprise of a 3P3W D-STATCOM, zigzag-delta transformer (or T-connected transformer) and a single-phase APF. These hybrid approaches are significantly reduced the overall rating of the compensator and improved the performance under non-ideal utility voltage conditions.
- Extensive simulation studies are presented to verify the efficacy of both topologies under ideal and non-ideal utility voltage conditions. The VA rating and comparison of performance between transformer based topologies and 3P4W D-STATCOMs are also presented to corroborate the superiority of the proposed topologies. For further

verification of the simulation studies of the proposed hybrid 3P4W D-STATCOMs, laboratory prototype of the adopted compensator topology consisting of five-level SSBC based 3P3W D-STATCOM and a zigzag-delta transformer with single-phase APF is developed. The developed prototype is studied for reactive power compensation, harmonic elimination and neutral current compensation with different loading and utility voltage conditions. From these studies it is observed that the proposed control schemes improve the power quality of the source currents even under distorted/unbalanced utility voltage conditions. Further, the experimental results are validated with simulation results by using the experimental parameters. Therefore, overall results prove that the control algorithm works efficiently and independent of the voltage.

6.2 Future Scope of Research

The research work presented in this thesis discloses a number of issues that could be further investigated.

1. Practical implementation of multilevel inverters for high-power applications is still an active area of research. The development of high-power inverters involves higher number of levels, large number of devices, complex control, large size and higher cost. Intensive research needs to be done on developing new multilevel inverter topologies with reduced number of components, low %THD and high reliability.
2. Development of new modulation techniques for high-power inverters with reduced power losses and natural balance of capacitor voltages is a potential area of research.
3. The conventional PI controller of the D-STATCOM control system can be replaced by soft computing techniques such as fuzzy logic, neural network and genetic algorithm to further improve the transient response of the system.
4. Design of the controller of the D-STATCOM using advanced control techniques such as model predictive control is an active area of research.
5. Another interesting topic could be the research on the combination of D-STATCOM and passive harmonic filters. This research could include the selection of topology, inspection of compensating characteristics, losses, cost and rating of the individual and overall compensator.
6. Determination of size and location of D-STATCOM in the distribution network is a potential area for research.

PUBLICATIONS FROM THE WORK

International Journals

1. D. Sreenivasarao, Pramod Agarwal, and Biswarup Das, “Neutral current compensation in three-phase, four-wire systems: A review,” Electric Power Systems Research, Elsevier, vol. 86, pp. 170–180, May 2012.
2. D. Sreenivasarao, Pramod Agarwal, and Biswarup Das, “A T–Connected transformer based hybrid D-STATCOM for three-phase, four-wire Systems,” International Journal of Electrical Power and Energy Systems, Elsevier, vol. 44, no. 1, pp. 964–970, Jan. 2013.
3. D. Sreenivasarao, Pramod Agarwal, and Biswarup Das, “Performance enhancement of a reduced rating hybrid D-STATCOM for three-phase, four-wire system,” Electric Power Systems Research, Elsevier, vol. 97, pp. 158–171, Apr. 2013.
4. D. Sreenivasarao, Pramod Agarwal, and Biswarup Das, “Performance evaluation of carrier rotation strategy in level shifted pulsewidth modulation technique,” Accepted for publication in IET Power Electronics.

International conferences

1. D. Sreenivasarao, Pramod Agarwal, and Biswarup Das, “A carrier-transposed modulation technique for multilevel inverters,” in Joint International Conference on Power Electronics, Drives and Energy Systems (PEDES) & 2010 Power India, New Delhi, Dec. 20-23, 2010, pp. 1–7.

Submitted to journals

1. D. Sreenivasarao, Pramod Agarwal, and Biswarup Das, “Control and performance of a transformerless PWM active power filter based on single-star bridge cells,” Submitted to Electric Power Systems Research.

Fig. 1: Front view of the experimental set-up.

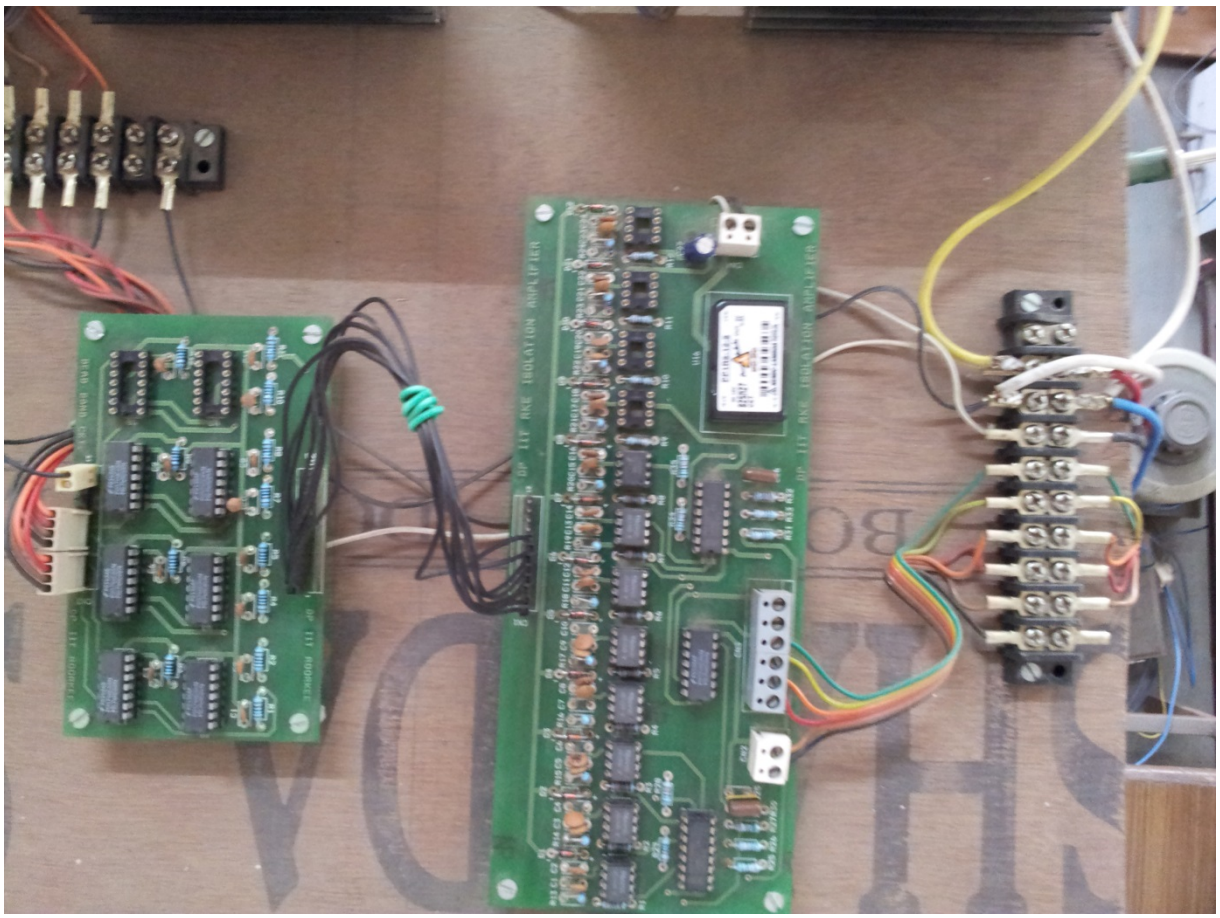


Fig. 2: Isolation and dead-band circuits.

Fig. 3: Host computer to implement control algorithms using D-SPACE.

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In this appendix, the screenshots of the MATLAB/Simulink models of the 3P3W D-STATCOM are shown.

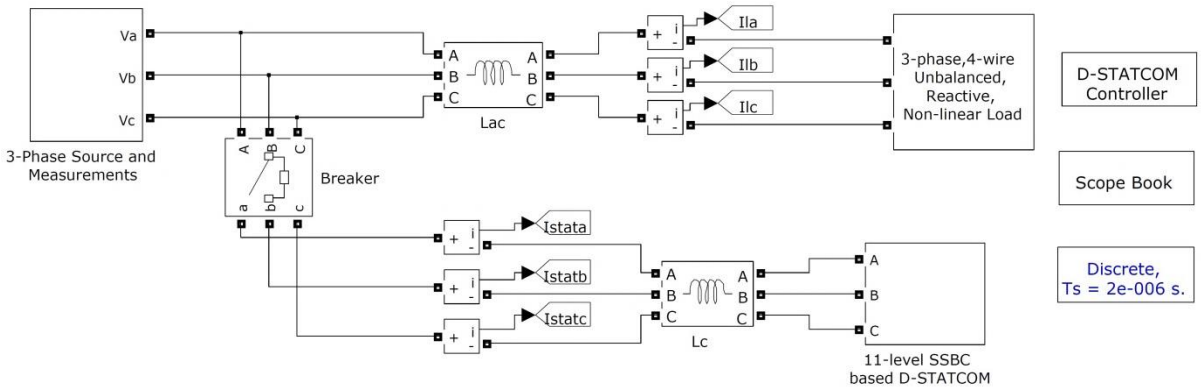

Fig. A.1: Modelling of D-STATCOM for 3P3W distribution system.

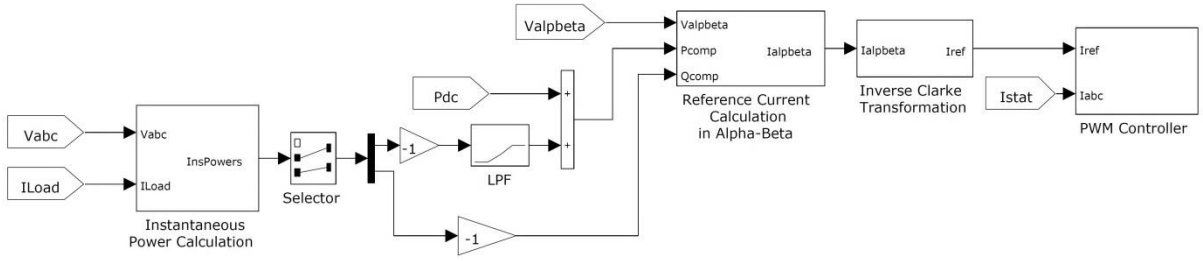

Fig. A.2: Modelling of D-STATCOM controller.

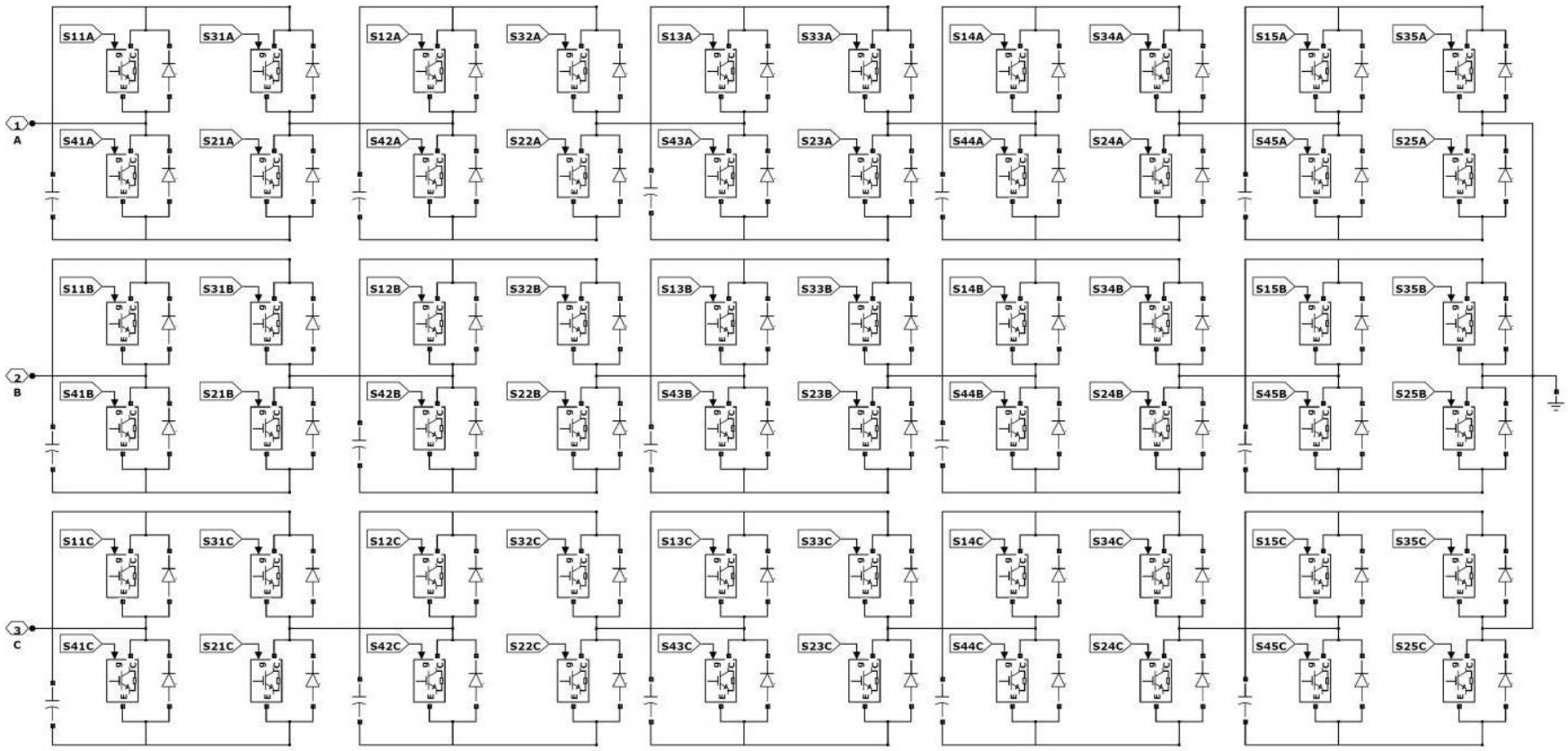

Fig. A.3: Modelling of 11-level SSBC based inverter.

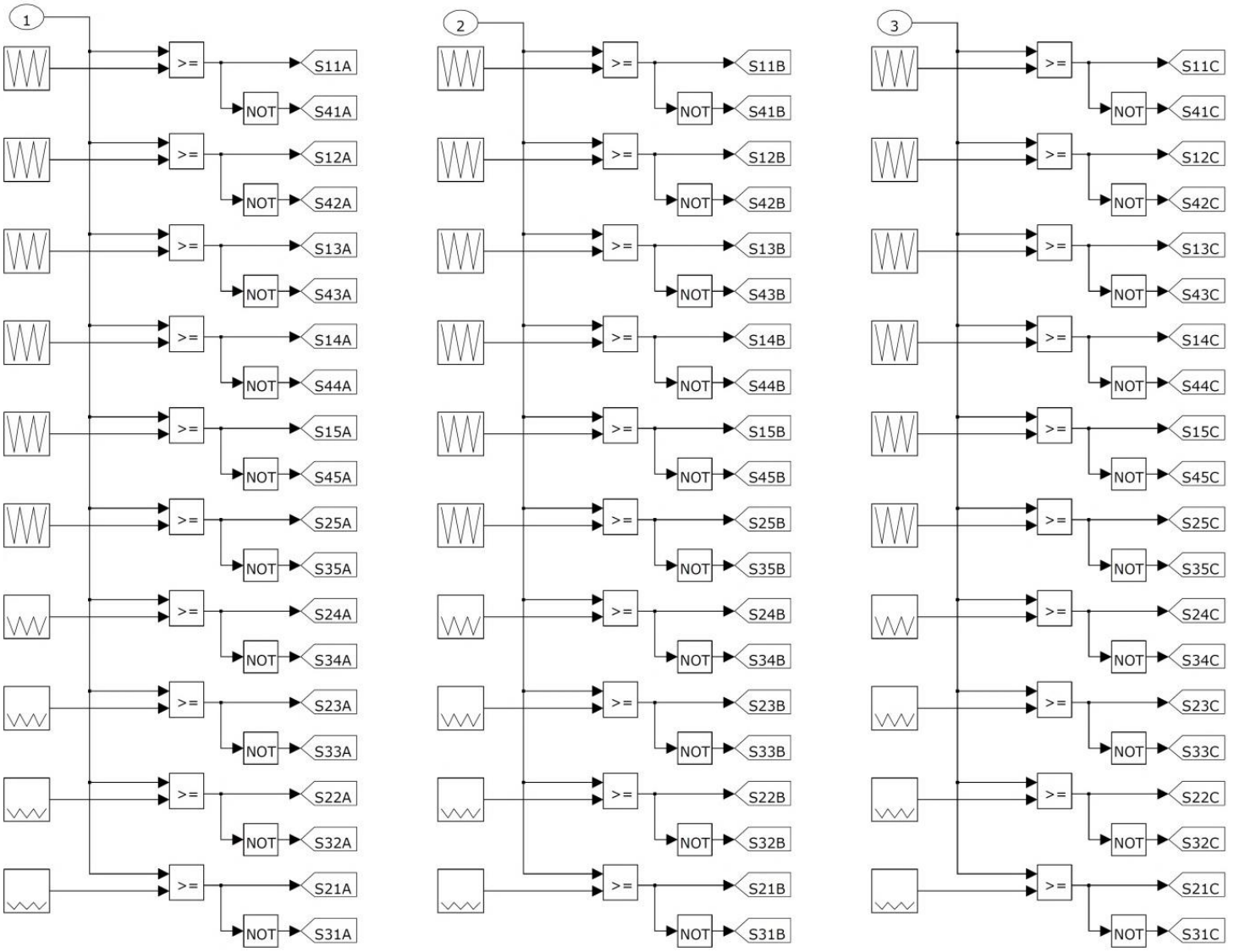

Fig. A.4: Modelling of generation of firing circuit.

In this appendix, the screenshots of the controller of a five-level SSBC based D-STATCOM using real-time workshop feature of MATLAB and real-time interface feature of dSPACE are shown.

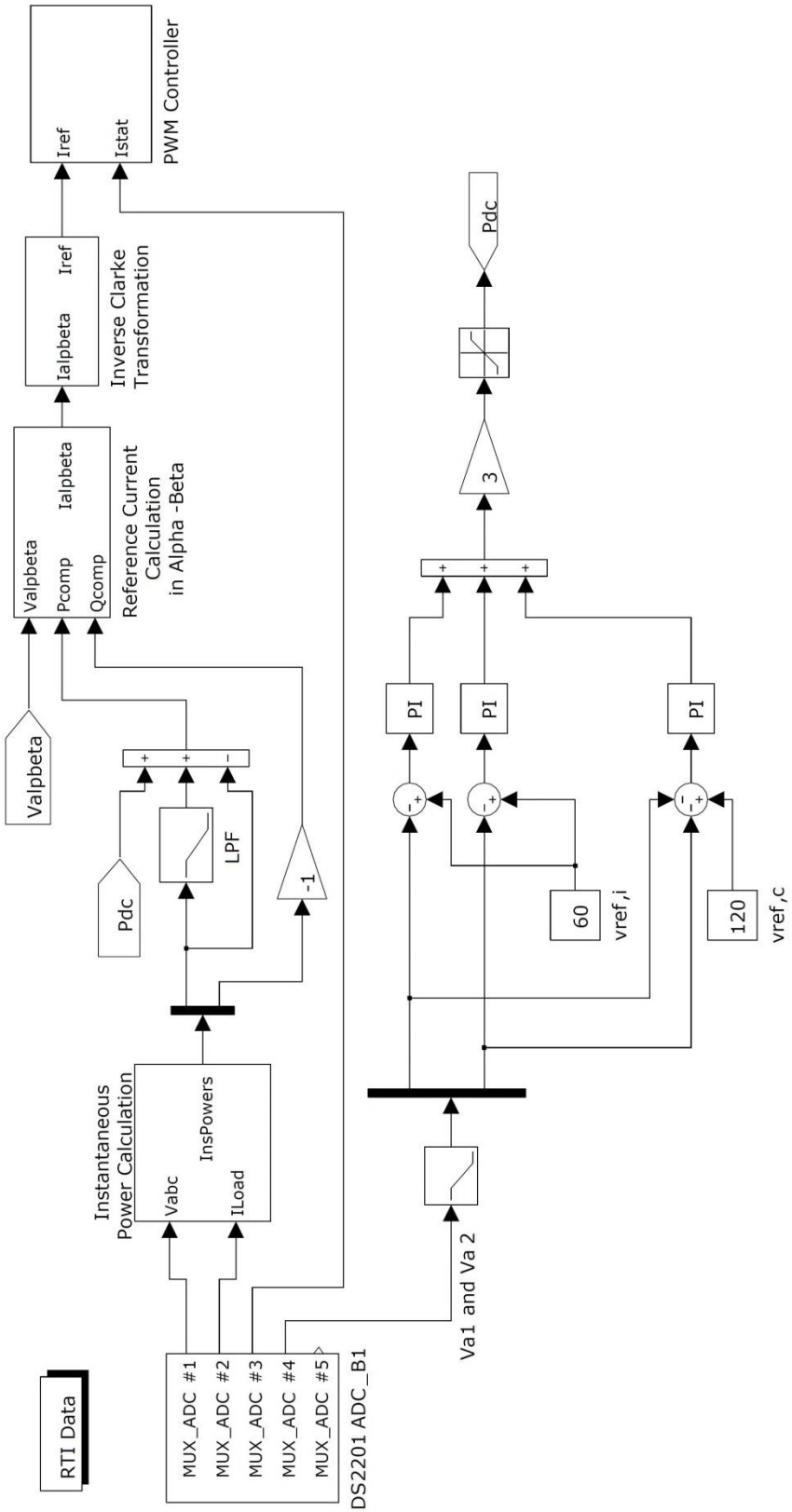

Fig. B.1: Modelling of five-level SSBC based D-STATCOM controller for 3P3W distribution system.

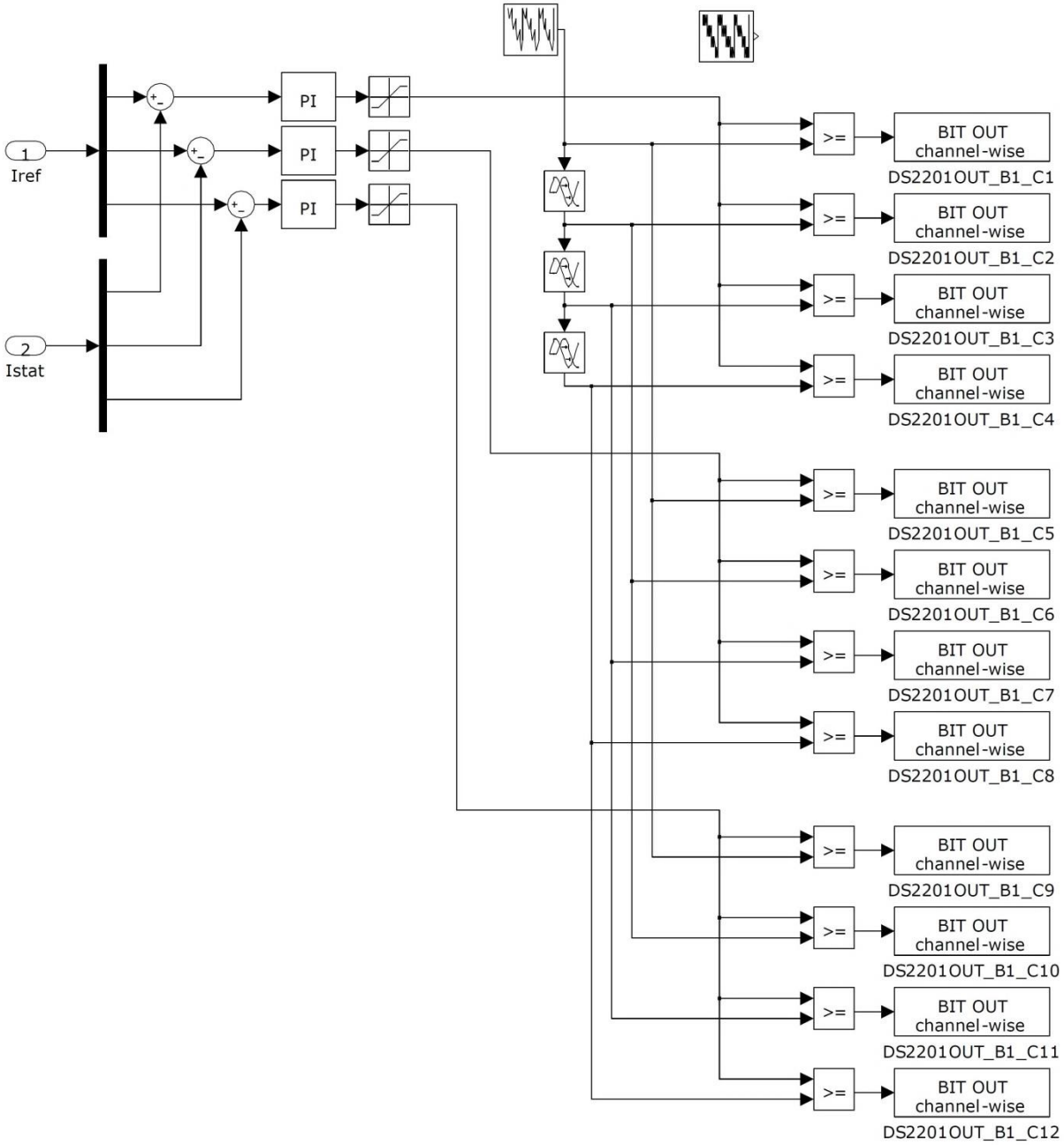

Fig. B.2: Modelling of PWM controller.