PERFORMANCE INVESTIGATION OF PV BASED 3-LEVEL INVERTER USING 2-LEVEL INVERTERS

A DISSERTATION

Submitted in partial fulfillment of the

requirements for the award of the degree

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(With specialization in Electric Drives and Power Electronics)

By

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Candidate's Declaration

I hereby declare that this thesis report entitled **PERFORMANCE INVESTIGATION OF PV BASED 3-LEVEL INVERTER USING 2-LEVEL INVERTERS**, submitted to the Department of Electrical Engineering, Indian Institute of Technology, Roorkee, India, in partial fulfillment of the requirements for the award of the Degree of Master of Technology in Electrical Engineering with specialization in Electric Drives and Power Electronics is an authentic record of the work carried out by me during the period June 2015 through May 2016, under the supervision of **Prof. S. P. SINGH, Department of Electrical Engineering, Indian Institute of Technology, Roorkee.** The matter presented in this thesis report has not been submitted by me for the award of any other degree of this institute or any other institutes.

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Certificate

This is to certify that the above statement made by the candidate is true to the best of my knowledge and belief.

Prof. S. P. SINGH

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Abstract

This Thesis presents a photovoltaic supply system fed multilevel inverter for pump load with common mode voltage elimination, the cascaded MLI topology is needed only 12 switches and no extra clamping devices required unlike others MLIs, which make it unique and suitable modulation technique provide the reliable single stage conversion with PV system. The modulation technique used is for tracking maximum power point and also to converts dc from PV to ac for a resistive load, inductive load and for a pump load. The unique solution to eliminate common mode voltage is also discussed, in the proposed method to eliminate common mode voltage series voltage is injected through 4-winding transformer which makes the common mode to zero. The voltage THD from the proposed method is less as compared to conventional method of common mode votage elimination. The sinusoidal level shift PWM method and space vector pulse width modulation method are used to generate the switching pulses for the MLI while modulation index for switching of MLI is controlled by incremental conductance or perturbation and observation algorithm. The proposed topology is compared with three well known basic MLI topologies on the basis of component used. As compared to generally used two stage conversion techniques this single stage system is having higher efficiency, reliability and reduced cost. The complete system is developed and tested on MATLAB/ Simulink, the hardware prototype is also developed and tested.

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Abbreviations

AC	**A**lternating **C**urrent
CM	**C**ommon **M**mode
CMV	**C**ommon **M**mode **V**oltage
DCMLI	**D**iode **C**lamped **M**ulti **L**evel **I**nverter
DC	**D**irect **C**urrent
DSP	**D**igital **S**ignal **P**rocessing
EMC	**E**lectro **M**agnetic **C**ompatibility
EMI	**E**lectro **M**agnetic **I**nterference
FCMLI	**F**lying **C**apactior **M**ulti **L**evel **I**nverter
IC	**I**ncremental **C**onductance
KCL	**K**irchoffs **C**urrent **L**aw
MPPT	**M**aximum **P**ower **P**oint **T**racking
MLI	**M**ulti **L**evel **I**nverter
MPP	**M**aximum **P**ower **P**oint
MI	**M**odulation **I**ndex
MV	**M**edium **V**oltage
NPC	**N**eutral **P**oint **C**lamped
PV	**P**hoto **V**oltaic
P& O	**P**erturbation **&**and **O**bservation
PSO	**P**article **S**warm **O**aptimization
PWM	**P**ulse **W**idth **M**odulation
RID	**R**igion **I**dentification **F**actor
SPWM	**s**ine **P**ulse **W**idth **M**odulation

SVPWM	**S**pace **V**ector **P**ulse **W**idth **M**odulation
SHEPWM	**S**elective **H**armonics **E**limination **P**ulse **W**idth **M**odulation
SVM	**S**pace **V**ector **M**odualtion
THD	**T**otal **H**armonic **D**istortion
VHDL	**V**HSIC **H**ardware **D**escriptive **L**anguage
VHSIC	**V**ery **H**igh **S**peed **I**ntegrated **C**ircuit

Chapter 1

Introduction

The world energy demand is rapidly increasing, a large amount of energy requiremnet is full fill by the fossil fuel which have the adverse effect on environment and create health hazard. The fossil fuel will be vanished sooner or later so we have to move on sustainable energy resources. The solar energy is freely available through out the world. The Pv based power supply system have some challanges due to its non linear characteristics and the generated power is depends on atmoshpheric conditions like variation in irradiation and temperature. Most of the home appliance is worked on AC supply, therefore inverter is necessary and inverter topology is plays a key role for the conversion of DC voltage into Ac voltage. Traditionally two stage inverters are required to track the maximum power and to convert DC voltage into AC voltage.

Electric motors provide driving power for a large part of modern prime movers. induction motors are the most widely used in industries as they are simple, reliable rugged, compact in size and cheap. Induction motor can also be used in aggressive or volatile environment since there are no problem of spark and corrosion in contrast to the commutation problem in DC motors. A wide range of speed control of IM requires variable frequency and variable voltage supply which necessitates complex control of inverters. However, the advantages of IM override the issue of complex control.

In order to improve output waveform quality in two-level VSIs, the general trend is to use high frequency PWM techniques which may cause problems like higher switching losses, higher common-mode voltages, high dv/dt, more EMI problems etc. Therefor research efforts are being made for new solutions like MLI to minimize the waveform distortion with limited switching frequencies.

1.1 RSEARCH MOTIVATION

This thesis gives the detail analysis of the system to be proposed. the PV array model with novel cascaded 3-level inverter control the induction motor for a pump load application with help of V/f control and MPPT schemes. India is the country where 70% of population live in rural area whose primary occupation is agriculture even though we have become self sufficient in food grains and technology has reached to help the formers, but many villages in India is not have electricity supply by today. Solar photo-voltaic base motor pump set is aimed that , helping such former groups who can not have electricity and can not afford costly technology.

Many researcher have worked on DC-motor based water pumping system but the size and cost of DC-motor is 2 to 3 times the cost of induction motor of the same rating. The induction motor is robust than the DC-motor. The maintenance required by DC-motor is also very high as compared to induction motor. In the proposed model the three phase induction motor is fed by the PV source through a 3-level inverter. Lots of the literature is available on the inverter topology. The multi-level inverter (MLI) gives better response than the normal two-level inverters. The output voltage THD and the rating of the switches used in the inverter is decreases depending upon the level of inverter, the low THD also reduces the size of the filter. Out of the basic MLI topologies available., H-bridge and cascaded inverters are most preferable for non renewable energy resources. The reason behind this is the interconnection of two different rating sources is simple and both the sources can supply a single load through a single inverter. Among all the basic MLI configuration present the cascaded inverter proposed by K. Gopakumar & V.T. Somasekhar in literature [4] is used for investigation. It has many advantages compared to conventional multi-level inverters.

To further improve the performance and efficiency of PV fed induction motor pumping system through cascaded multi-level inverter, the selection of modulation strategy plays an important role. the V/f control is the oldest and very popular method to control 3-phase induction motor(IM) due to its simplicity. but the digital implementation V/f method is not easy also the DC-source utilization by V/f is 15% less than the space vector modulation (SVM) technique. Hence many researchers now focused on space vector based modulation techniques. The space vector modulation is simple to implement digitally. Space vector modulation gives better utilization of DC-source than the V/f control, this is also very important factor when working with low-power, low-voltage photo-voltaic source.

Further investigation on the inverter shows that the common mode voltage (CMV) developed across the motor, which may cause the damage of the induction motor due to heavy ground current flow. The problem of CM can be eliminated when working with MLI topology. Therefore a cascaded MLI topology with SPWM and SVPWM is tested for induction motor based pump load system. The proper selection of switching sequence in space vector based MLI, the common mode voltage can be fully eliminated.

1.2 LITERATURE SURVEY

This section presents a review of research works that have already been done so far in the field of PV based water pumping system and MLI topologies. The literature review is presented in five sections. First, solar photovoltaic modules connected in possible array configurations under normal/partial shaded conditions with MPPT are discussed. Followed by, various existing MLI are briefed, based on its topological and design, modulation schemes and common mode mode voltage in the subsequent sections.

- Bum-Seok Suh et.a.l[1] in this paper author discussed about the GTO based novel MLI inverter topology with the advantage and drawback of using MLI for medium and high voltage. Also explain the problem with the conventional MLI topology available and its solution.

- jih sheng lai et.al.[2] in this paper presented a basic three types of MLI topology and compare their features, and investigate the performance of all three MLIs with their applications.

- Jose Rodriguez et.al.[3] discussed about the basic diode clamped, flying capacitor and multi-cell MLI topology. Main focus on the emerging topology with their control and modulation strategy like SPWM, selective harmonic eliminations, SVPWM etc. given. Author also gives the detail analysis of the present and future application of such basic and new MLI topologies.

- V.T Somasekhar and K. Gopakumar [4] in this paper a novel three-level cascaded inverter is presented. The advantage of this topology is its simplicity and control as compared to the DCMLI. The topology given in this paper have many advantages like isolated DC-sources of magnitude half of used in DCMLI, higher efficiency and low cost etc.

- R. S Kanchan, K. Gopakuamr et.al.[5] in this paper discussed about the CMV appeared due to high switching in MLIs. Author gives the solution to eliminate the CMV by using two cascaded three level inverter topology for open end winding induction motor drive. The modulation technique used is SVPWM. The switching of inverters are done in the way that, the MLIs are connected at both ends of the motor winding generate same CMV and cancel each other.

- Jianye Rao & Youngdong Li [6] in this paper presented the novel hybrid cascaded MLI topology. In this scheme two MLIs are used, the H-bridge inverter is working as a main inverter and the DCMLI is working as a conditioning inverter. Both the inverter together drive the motor. The DC source is connected across the main inverter only while, the conditioning inverter requires only ultra capacitors. This ultra capacitors reduces the consumption of DC batteries by supplying the reactive power of the motor under steady state condition and it stored the charge during the braking operation. The proposed topology is applied and tested in electric vehicle by the author.

- Nasrudin Abdul Rahim and Jeyraj Selvaraj [7] in this paper single-phase multi-string 5-level photo-voltaic inverter is presented. The grid connected

PV system is presented, the PV feeds the power to grid, to supply the common load. The novel sine-PWM method gives the better control and low THD for the proposed 1-ϕ 5-level inverter, the overall system is operated at near unity power factor.

- Liu Miao and Hong Feng [8] in this paper a dual buck half bridge 3-level inverter is proposed. The proposed topology have high reliability, high efficiency, less losses and no shoot through problem.

- Sujitha.N and RAmani.K [9] in this paper application of MLI in hybrid vehicle is discussed. The main advantage of a novel MLI inverter topology with low THD and high efficiency with better utilization of DC-source. The proposed topology required a traditional three-phase inverter connected in series. The control pulses for the inverter is generated by selective harmonic elimination PWM scheme.

- Subhadeep Bhattacharya et.al.[10] in this paper described about the modular multilevel inverter (MMLI), MMLI is applied to the low voltage and medium power electric vehicle. Main work is done on the comparison of MMLI topology with conventional 2-level inverter topology for electric vehicle application. The topology of MMLI explained is based on half bridge inverter. the review on different operating mode is also given in the paper.

- Mohammad Farhadi Kangarlu et.al.[11] in this paper discussed about the new cascaded MLI topology. The new topology is tested in both symmetrical and asymmetrical condition, and compared with the conventional cascaded H-bridge inverter topology. The proposed topology proved better than the conventional cascaded H-bridge topology with respect to the number of switches used and the output voltage resolution while in both the inverters the voltage stress across the switches are equal. The proposed inverter topology also control the charge balance of the capacitors without any extra effort. The comparative study given in the paper stated that the proposed topology of cascaded MLI required less number of switches compared to other Asymmetrical inverter configuration.

- Ramulu Chhinthamalla, Sachin jain et.al.[12] in this paper presented a single stage 3-ϕ, 3-level inverter with simple sinusoidal PWM scheme is used to control the motor pump system, the V/f scheme applied allows the motor to work on the maximum power provided by the PV array. The proposed model required a two PV array and only one MPPT circuitry to control the switching of inverter to supply the pump load with maximum power under variable irradiation condition.

- Zuhair Alaas and Caisheng Wang [13] In this paper presented a new topology of isolated MLI. The major advantage of proposed MLI is the requirement of less number of switches as compared to conventional MLI. It also required only one DC-source and cascaded to high frequency transformer. The application of the proposed topology is suitable for high voltage and high power system, like integrated battery storage system and unconventional energy sources to grid. A simple phase shifted PWM scheme is applied to control the six switches inverter for harmonic reduction.

- Hossein Sepahvand et.al.[14] in this paper discusses about the general H-bridge MLI topology. Author suggested a alternative option ot replace the DC sources required by each H-bridge cell by a capacitor. In the proposed system only one H-bride cell is feeds by a DC-source and rest of all H-bridge cells are connected to capacitors, this reduces the overall cost of the system. A simple phase shift PWM scheme is used to control the MLI. The proposed system has a wide range of voltage regulation.

- Mariusz Malinowski and K. Gopakumar [15] in this paper a detail survey of different MLI topologies is presented. author also discussed the advanced and regenerative MLI topologies with the proper application. The future development and suggestions are also discussed.

- G. M. Dousoky et.al.[16] in this paper presented the dual mode controlled maximum power point tracker for grid connected photo-voltaic system. the proposed MPPt technique controls both load angle and modulation index of the inverter, and worked in two control modes; active and reactive power

mode. The proposed single stage grid connected system gives good dynamic and steady state response with flexible active and reactive power control.

- Trishan Esram and Patrick L. Chapman [17] in this paper a detailed review on various MPPT techniques are presented. The 19 MPPT techniques are discussed with the various implementations.

- Kenji Kobayashi et.al.[18] in this paper a novel two stage MPPT technique is discussed. The proposed technique maximize the output power of the PV-array and track the real maximum power point under uniform or non uniform solar irradiation condition. The proposed technique is tested for both the insolation conditions.

- S. Ozdemir et.al.[19] in this paper a PV based variable speed drive for 3-ϕ induction motor to stimulate a ventilation system is proposed. A variable stepped incremental conductance (IC) and constant voltage MPPT techniques are applied to track the maximum power point during the operation. Both the MPPT techniques are used in a single system to generate the voltage & frequency reference for the V/f controlled 3-ϕ 3-level inverter based induction motor pump drive.

- Auttawut Waiprib et.al.[20] in this paper a V/f controlled 3-ϕ solar water pumping system is discussed. The micro-controller is used to gnerate the control signal for the proposed solar water pump in system. Also discussed the various complexity of applying the SPWM for 3-ϕ inverter drive. The maximum power point technique applied in the software to ensure the system at max power point.

- A. Darwish et.al.[21] in this paper a novel approach to convert DC in to AC is discussed. A modified cuk converter is used for the conversion of DC into AC current with the reduced size of energy storing element like inductors and capacitors. The reduced size energy storage elements also reduces the size and cost of the proposed inverter topology. The cuk converter perform both boost and buck operation depending upon the duty ratio. The comparison with the conventional VSI and CSI proved the proposed topology better with respect to the voltage and current drop at the output side and the efficiency.

The proposed cuk based inverter is most suitable for the PV application in which a continuous average input current is needed to track maximum power point throughout the operation.

- s. jai and v. Agarwal [22] in this paper various MPPT techniques are reviewed and compare on the basis of various factors. for 1-ϕ, single stage grid connected PV applications. for the study purpose author considered a buck-boost converter topology operating in discontinuous current mode for single stage grid connected system. The main focus on the comparison of various MPPT techniques. The MPPT techniques are compared on the basis of energy extracted from PV source during transient and steady state condition, time taken to reach maximum power point, oscillation at operating point etc. A new terminology "Energy tracking factor" is also introduced and defined. At the end concluded that all the MPPT techniques have their advantages and drawbacks. The novel B-technique and ripple correlation method of MPPT have overall good features compared to rest of the MPPT technique discussed.

- Sachin jain and Vivek Agarwal [23] in this paper a novel fast MPPT algorithm is presented. The proposed MPPT algorithm gives teh significantly improved efficiency during the tracking as compared to conventional algorithm. The proposed technique is most suitable and fast changing environment conditions, and easy to implement in any ast controller like DSP or FPGA.

- Ch. Ramulu, Sachin jain et.al.[24] in this paper a single stage open end winding induction motor based water pumping is discussed. The detail analysis and modeling of the proposed system is presented. The proposed single stage system takes care about the CMV and the maximum power point tracking with V/f control throughout the application.

- M.S. Taha and K. Suresh [25] in this paper a 1-HP submersible solar water pumping system is introduced and discussed in detail. To track the maximum power point the speed of the motor is taken as variable using V/f

control which allow to track MPP under varying insolation conditions. A simple P&O MPPT is used for the purpose.

- A. K. guta and A. M. Khambadkone [33] in this paper explain the new method to implement the multilevel SVPWM. The generalized method is discussed which can be applied to any level for DCMLI. The modes of operation will vary from linear modulation region to overmodulation region very smoothly. The method discussed is very good for digital implementation for any level of MLI.

- Haorn Zhang et.al. [35] in this paper discussed about the conventional method to eliminate CMV using SVPWM for three level DCMLI. Also discussed the method to eliminate the CMV using SPWM with some modifications.

- Sachin Jain et.al. [40] in this paper a single stage topology for solar water pumping system with open end winding induction motor is discussed. teh sample averaged zero sequence elimination (SAZE) PWM method is employed with V/f control to control the motor operation under varying solar irradiation. The MPPT is used to generate the reference signal (ie. modulation index, ma) for V/f block.

- Manoj R Reddy and J. Chelladurai [41] in this paper discussed about the PV fed grid connected MLI with SVPWM control. The DCMLI is used as 3-level for the analysis of single stage and two stage converter. The operation of MLI in over-modulation range is also discussed.

- h. Alawieh et.al. [42] in this paper discussed about the common mode voltage generated by VSI across the motor windings. Also discussed some advanced method (ACME) to reduce common mode voltage based on modified-SVPWM, which is better than conventional method with respect to output voltage THD.

1.3 OBJECTIVE OF DISSERTATION WORK

The objectives of this dissertation work include:

1. Propose a single stage Pv based water pumping system of rating 1-HP.
2. Study on MLI topology and modulation schemes.
3. Propose a novel scheme to eliminate a CMV elimination without reducing the out put voltage THD and level.
4. Simulate the proposed system with SPWM, SVPWM With and without common mode elimination schemes.
5. Implement the proposed scheme on FPGA.
6. Evaluate the performance of the proposed scheme.

1.4 ORGANISATION OF REPORT

This report is organized as follows: **Chapter2** describe about the modeling of Photovoltaic system and Maximum power point tracking techniques. In **Chapter3** study of conventional MLI topology and Multi-level inverter topology used in the proposed work is discussed. In the **Chapter4** the conventional modulation techniques like SPWM and SVPWM with CMV elimination for three-level inverter is discussed. The operation and mathematical modeling of proposed system is given in **Chapter5**. In **Chapter6** the simulation of the proposed system in MATLAB/Simulink environment is discussed. The development of hardware prototype and and results of the proposed system is given in **Chapter7**.

Chapter 2

Photovoltaic Energy Conversion System

There are two methods are available to utilize the solar energy, solar heating and electrical power generation. This chapter is focused on photovoltaic based supply system and its utilization.

2.1 PHOTOVOLTAIC MODULES AND ARRAY

Soalr photovoltaic panels are used photoelectric effect to directly convert sunlight into electrical energy. Sunlight contains photons and when these photons strike on pv panel it gives the sufficient energy to electrons to move from valance band to conduction band therefore current starts flowing. now a days mono crystalline silicon and amorphous silicon materials are the most commonly used to design PV panels. The PV panes have robust structure and no movable parts so it requires less maintenance as comparison to the other form of energy sources. Series and parallel connections of PV cells is known as PV modules and the series and parallel connections of such modules are known as pv array as shown in figure 2.1. PV modules are generally available in between 60W and 200W. to increase the voltage

modules are connected in series and parallel connections of these modules increases the current rating of pv array.

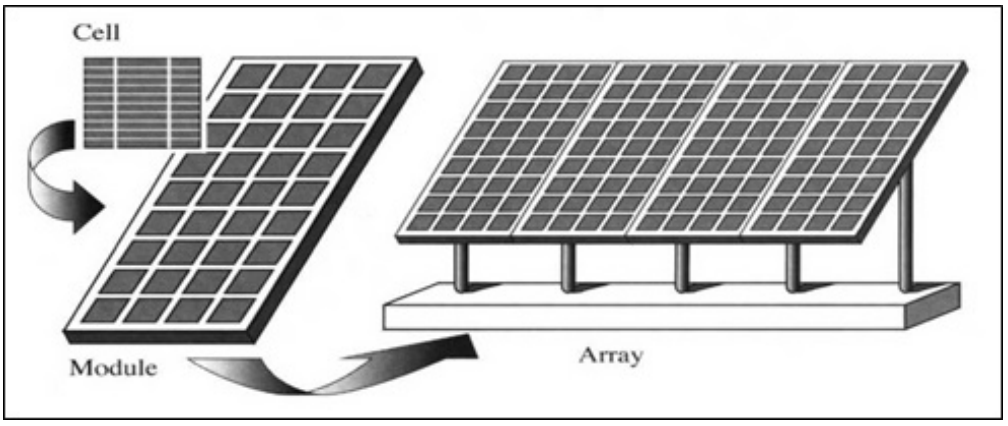

FIGURE 2.1: PV cell, modules and array

2.2 MODELING OF PV PANELS

The single diode model [24, 26] is used to develop the characteristics of solar photovoltaic as shown in Fig.2. For the analysis of the system the mathematical model of photovoltaic cell is developed with the help of equations (1) to (5) given below:

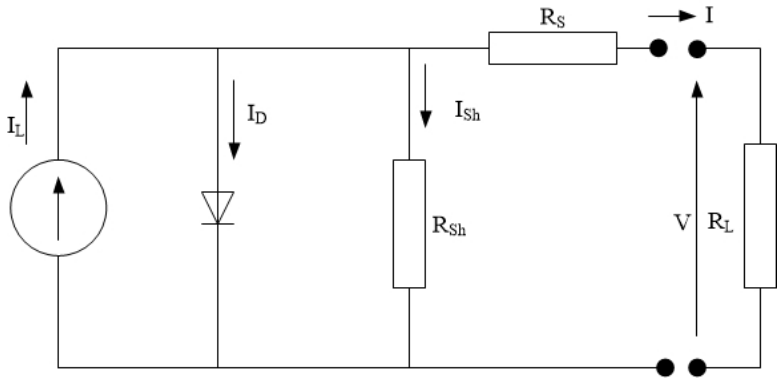

FIGURE 2.2: Single diode model of PV cell

Short-circuits current of photovoltaic is presented by $I_{PV}(or I_L), I_D$ represents the diode current, Rs and Rp represents the photovoltaic cell series and parallel resistances respectively. The output current of the PV cell is given by equation (2.1)

$$I = I_{PV} - I_D - I_{sh} \tag{2.1}$$

$$I = I_{PV} - I_0[exp(\frac{q(V + IR_s)}{AK_BT}) - 1] - \frac{V + IR_{sh}}{R_{sh}} \tag{2.2}$$

$$I = I_{PV} - I_D - I_{sh} \tag{2.3}$$

$$I_0 = I_{RS}(\frac{T_c}{T_{Ref}})^3 exp[qE_B(\frac{1}{T_{Ref}} - \frac{1}{T_C})/K_BA] \tag{2.4}$$

Where, I_{RS}=Reverse saturation current, q= Electron Charge 1.6×10^{-19} (C), $K_B = Boltzmann\ Constant$ 1.38×10^{-32} (j/K), A= p-n junction quality or ideality factor. Reverse saturation current (I_{RS}) used in equation (2.4) is represented as:

$$I_{RS} = \frac{I_{SC}}{exp(qV_{oc}/N_sKAT_C) - 1} \tag{2.5}$$

Where, V_{OC} =open circuit voltage of the cell, N_S = Number of series connected cells per string.

$$I_L = N_P I_{PV} - N_P I_S[exp(\frac{qV}{N_sKT_CA}) - 1] \tag{2.6}$$

Where, V= Output Voltage of PV cell (V), I_S = diode saturation current of PV cell, N_P= Number of Parallel connected cells in strings.

2.3 CURRENT-VOLTAGE AND POWER- VOLTAGE CURVES

The current vs. voltage (I-V) curve generally shows the electrical behavior of the PV cell. The figure2.3 shows the I-V characteristic of typical PV cell. The curve

shows that the variation of current and voltage when cell resistance varies from zero to infinity. The curve is flat in the initial region and falls off towards zero after the threshold voltage. This makes the PV cell differ than the ideal current source. The shows the three main points, the point at which current is zero is called short-circuit current and the point at which voltage is zero is known as open circuit voltage, this is the voltage measured with output terminal open. In between Isc and Voc the curve has a knee point known as maximum power point.

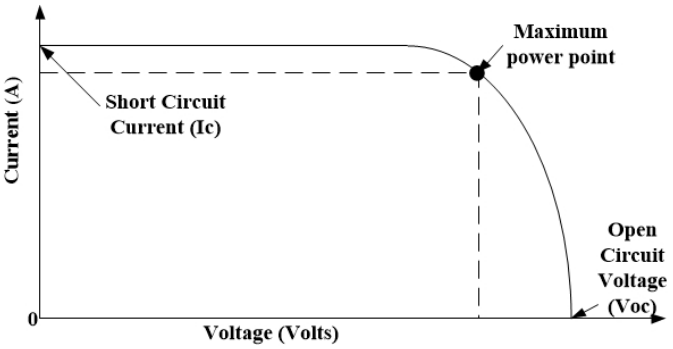

FIGURE 2.3: I-V Curve of a typical silicon PV cell

The power vs voltage curve of pv module is known as power curve. The power generated by the panel is the product voltage and current output. The PV cell does not produce any power at zero voltage or zero current, and maximum power is produced at the knee point of I-V curve as shown in the figure 2.4. In the electrical analysis of the PV circuit it is modeled approximately as a constant current source.

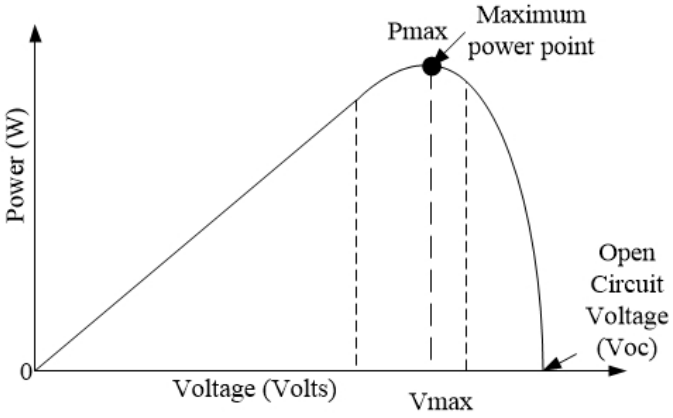

FIGURE 2.4: P-V characteristic of the PV cell

The following standard test conditions are established internationally in order to measure the photovoltaic cells output power. The level of solar irradiance is 1000

W/m^2, with the reference air mass of 1.5 solar spectral irradiance distributions and cell or module junction temperature of 25^0C.

2.4 PHOTOVOLTAIC POWER GENERATING SYSTEM

The PV voltage generation system can be classified as stand-alone and grid connected system. The topologies used for such generation is further classified as single stage and two-stage systems. In two-stage there is a intermediate DC to DC converter, which works on the MPP developed by the PV array. In comparison to this the single stage works without the intermediate DC to DC converter stage and the inverter works directly on MPP of PV array. The second topology gives higher efficiency because of the elimination of the DC to DC converter but there is a need of a more complex control schemes.

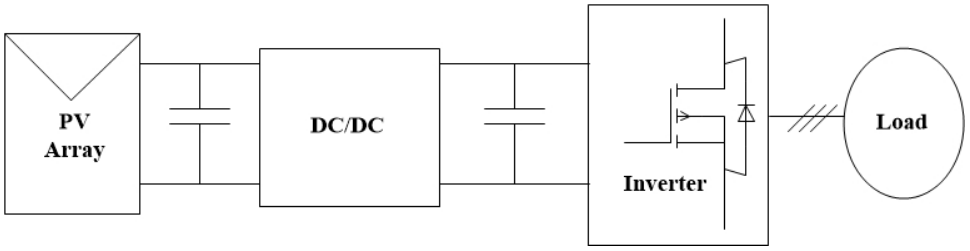

FIGURE 2.5: Two stage topology

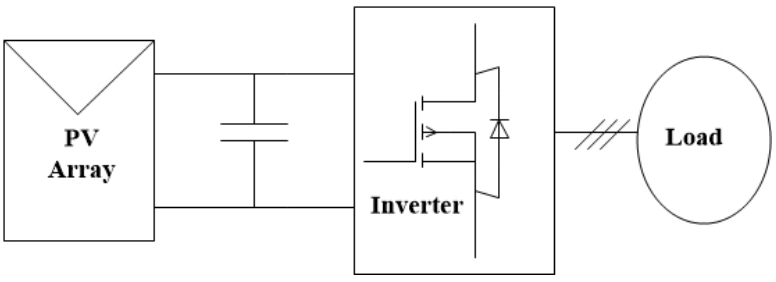

FIGURE 2.6: Single stage topology

2.5 MAXIMUM POWER POINT TRACKING TECHNIQUES

The non linear IV and PV characteristic of photovoltaic array is already discussed and the characteristics are shown in figure 2.3 and figure 2.4 respectively. From the above discussion it is concluded that the solar PV output voltage voltage and current is depends on environmental conditions such as irradiation and temperature [27]. To extract maximum power from solar photovoltaic under varying atmospheric conditions an appropriate MPPT technique is required according the system requirement.

The essential component of PV system (grid connected or stand-alone) is an MPPT. Now a day a number of MPPT techniques have been developed few of them are adaptive perturbation and observation, adaptive fuzzy, estimated perturb and perturb, generatic algorthm, neural network and ant-colony based MPPT, etc. The MPPT techniques are compared on the basis of circuitry used, complexity of algorithm, difficulty in hardware implementation. Table 2.1 gives the summary of comparative study of various MPPT techniques available.

Table (2.1) shows the comparison chart of 26 MPPT techniques, comparison is based on control strategy applied, control variable used,Type of circuitry, Complexity in application, suitable application of technique and the converter used with the specific MPPT technique,

Where, IndC= Indirect Control, Samp= Sampling method, Mod= Modulation method, Digi= Digital, Ana= Analog and A-z represents MPPT techniques given below:

A. Curve fitting technique, *B*. Fractional short circuit current (FSCI) technique, *C*. Fractional open circuit voltage (FOCV) technique, *D*. Look up table technique, *E*. One cycle control (OCC) technique, *F*. Differentiation technique, *G*. Feedback voltage or current technique, *H*. Feedback of power variation with voltage technique, *I*. Feedback of power variation with current technique, *J*. Perturbation and observation (P&O) or hill climbing technique *K*. Incremental conductance

(Inc-Cond) technique, *L*. Forced oscillation technique, *M*. Ripple correlation control (RCC) technique, *N*. Current sweep technique, *O*. Estimated perturb-perturb (EPP) technique, *P*. Parasitic capacitance technique, *Q*. Load current/load voltage maximization technique, *R*. DC link capacitor droop control technique, *S*. Linearization based MPPT technique, *T*. Intelligence MPPT technique, *U*. Sliding mode based MPPT technique, *V*. Gauss-Newton technique, *W*. Steepest-Descent technique, *X*. Analytic based MPPT technique, *Y*. Hybrid MPPT (HMPPT) techniques, *Z*. MPPT techniques for mismatched conditions.

The basic and generally used MPPT techniques are:

- Perturb and Observe (P&O) Method
- Incremental Conductance (IC) Method

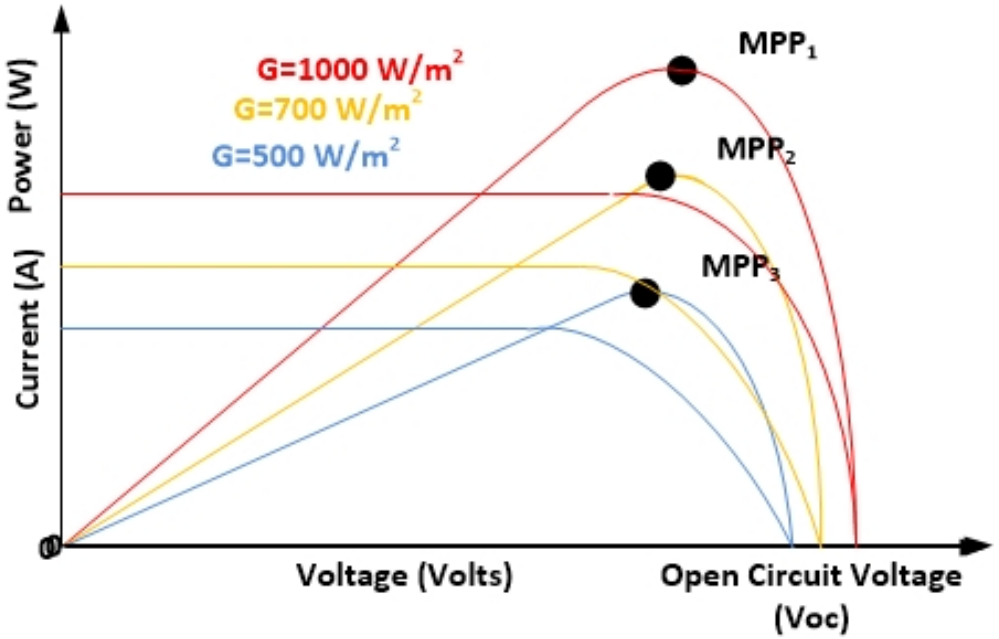

FIGURE 2.7: Current v/s voltage and power v/s voltage characteristics at various solar irradiations

2.5.1 Perturbation and Observation (P&O)

The operating principle of P&O is based on perturbing the voltage and the current of the PV at a regular interval and then comparing the new power measure with the previous to decide the next variation. The Perturb and Observe method is

most commonly used for MPPT. This is the oldest numeric optimization method and also the one most widely used for systems that dont have a local maxima. In this method the operating point is moved to a certain direction and the power change is measured. If the change in power is positive the operating point is moved in the direction of the previous perturbation, if the change in power is negative it is moved opposite to the direction of the previous perturbation. The performance in dynamic and steady state response is decided by the size of perturbation used.

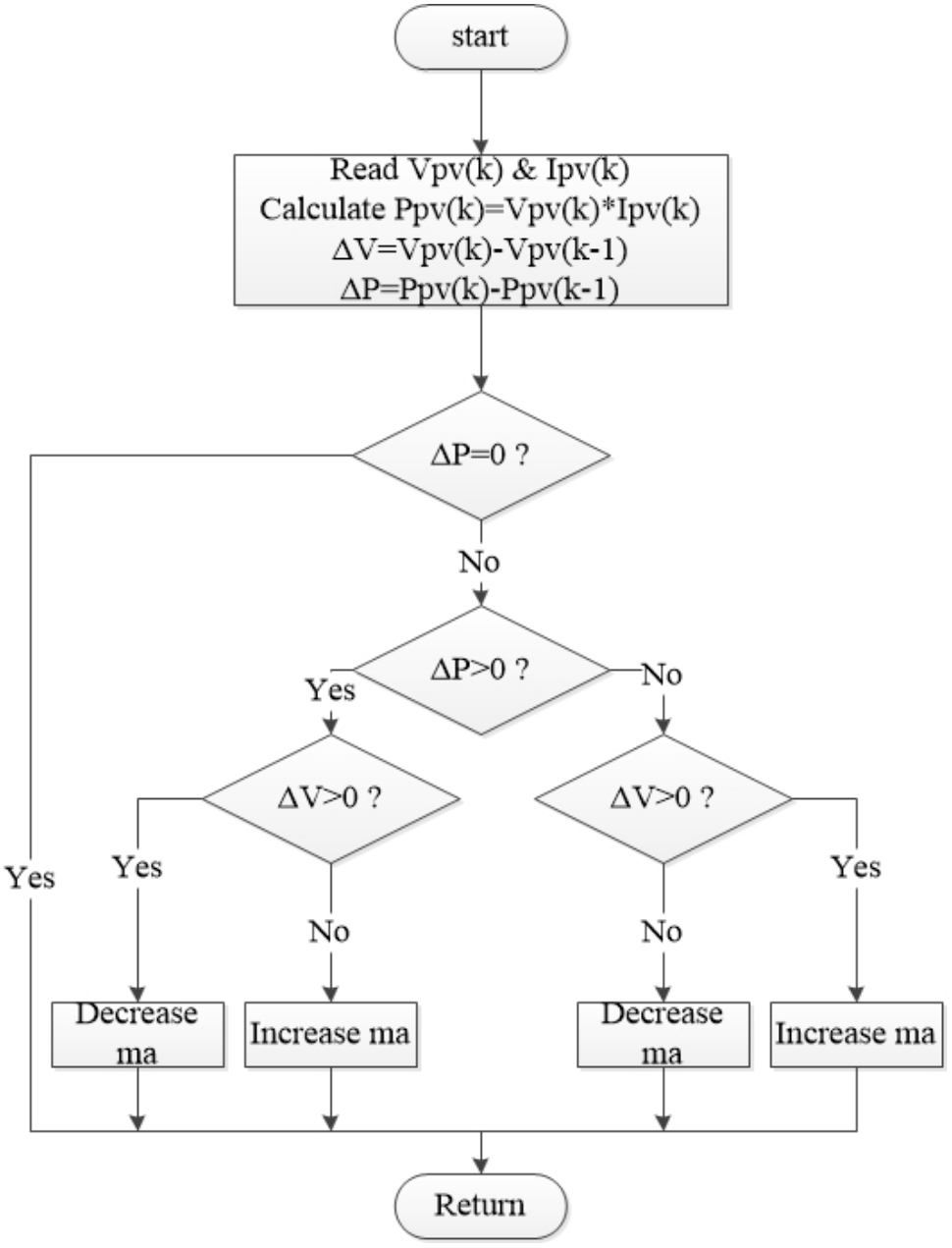

FIGURE 2.8: Flow chart of Perturbation and observation method

2.5.2 Incremental Conductance (IC)

The principle of the incremental conductance (IC) method utilizes the property of the maximum power point (MPP): the derivative of the power is null, as shown in equation (2.8). So, the IC method uses an iterative algorithm based on the evolution of the derivative of conductance G, as expressed in equation (2.11), where the conductance is the ratio of I/V. At maximum power point the solution of equation-2.10 is zero, at the right hand side of maximum power point the solution is negative and at left hand side of MPP the solution is positive.

$$P = V \times I \tag{2.7}$$

$$\frac{dP}{dV} = 0 \tag{2.8}$$

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V\frac{\triangle I}{\triangle V} \tag{2.9}$$

$$Thus : \frac{\triangle P}{\triangle V} + \frac{I}{V} = 0 \tag{2.10}$$

The equation (8) can be rewritten as

$$Or \triangle G + G = 0 \tag{2.11}$$

$$\frac{\triangle I}{\triangle V} = -\frac{I}{V}\ at\ maximum\ power\ point \tag{2.12}$$

$$\frac{\triangle I}{\triangle V} > -\frac{I}{V}\ at\ left\ of\ maximum\ power\ point \tag{2.13}$$

$$\frac{\triangle I}{\triangle V} < -\frac{I}{V}\ at\ right\ of\ maximum\ power\ point \tag{2.14}$$

Thus, by comparing the instantaneous value of condance (I/V) to the incremental change in conductance ($\triangle I / \triangle V$) the maximum power point can be tracked. The flow chart for IC MPPT is shown in figure-2.9. The efficiency of this method is similar to the efficiency of P&O MPPT method, also giving the good response under rapidly changing conditions. The main drawback of this method is the perturbation size as in P&O which can be reduced by taking variable step size which makes the system complex and costly.

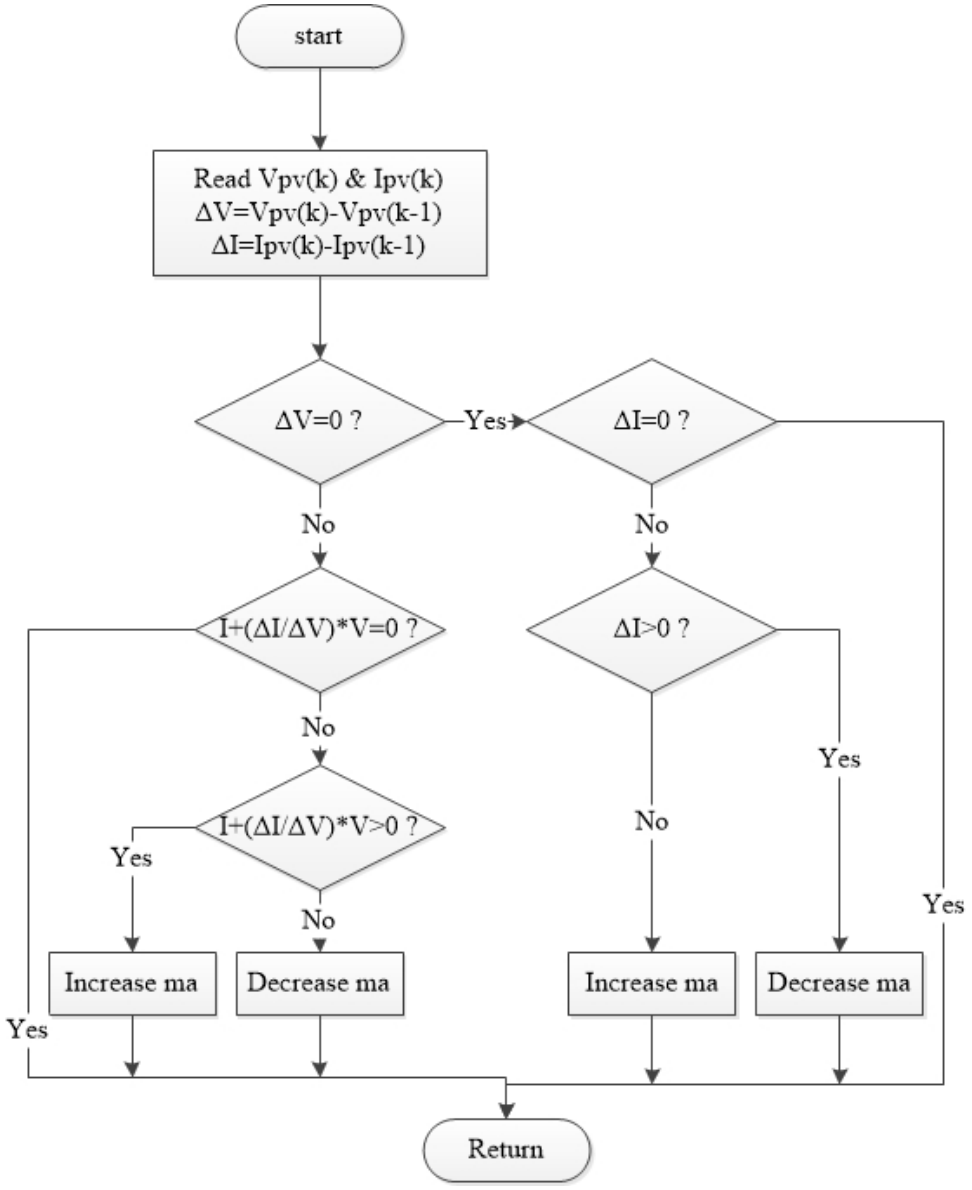

FIGURE 2.9: Flow chart of Incremental conductance method

2.6 CONCLUSION

The V-I and V-P characteristics shows that, the photo-voltaic array is having the behavior of both current source and voltage source. For the electrical analysis current source model is preferred, the PV characteristic also shows that at near $0.8V_{oc}$ the PV array gives the maximum power, to track this maximum power a specified MPPT technique is required. The comparative study of 26 types of MPPT techniques are discussed, and the basic P&O and IC MPPT techniques are explained.

Table 2.1: Comparative study of MPPT Techniques [21]

MPPT Technique	Control Strategy	Control Variable	Circuitry	Complexity	Application	Converter used
A	IndC	V	Digi	Low	Stand alone	DC/DC
B	IndC	V or I	Both	Low	Stand alone	DC/DC
C	IndC	V, I	Digi	Low	Stand alone	DC/DC
D	Samp	I	Both	Low	Stand alone	DC/DC
E	Samp	V or I	Digi	Low	Grid	DC/DC
F	Samp	V or I	Both	High	Stand alone	DC/DC
G	Samp	V, I	Digi	Low	Stand alone	Both
H	Samp	V, I	Digi	High	Stand alone	Both
I	Samp	V, I	Both	Medium	Stand alone	Both
J	Samp	V, I	Digi	High	Stand alone	DC/DC
K	Samp	V, I	Digi	High	Stand alone	DC/DC
L	Mod	V or I	Ana	High	Stand alone	DC/DC
M	Mod	V or I	Ana	High	Stand alone	DC/DC
N	Samp	I	Digi	High	Grid	DC/DC
O	Samp	V, I	Both	High	–	DC/DC
P	Samp	V, I	Digi	Low	Stand alone	Both
Q	Mod	V	Ana	Medium	Stand alone	Dc/DC
R	Mod	V	Both	Low	Grid	Dc/DC+ DC/AC Two stage
S	Samp	Irradiance	Digi	Medium	Stand alone	DC/DC
T	IndC	V or I	Digi	Medium	Both	Both
U	Samp	V or I	Digi	High	Both	Both
V	Samp	V or I	Digi	Simple/ Medium	Stand alone	DC/DC
W	Samp	V or I	Digi	Medium	Stand alone	DC/DC
X	IndC	V or I	Both	Medium/ High	Both	DC/DC
Y	Samp	V or I	Digi	Medium/ High	Both	Both
Z	IndC	V or I	Digi	Medium	Both	Both

Chapter 3

Multi-Level Inverter Topologies

This chapter represents a comprehensive analysis of the three level inverter topologies, operating principle, and applications. The focus is given on the novel cascaded three-level inverter. The salient features of all these topologies have been presented and comparison also been made, application, advantages, features and disadvantages are also discussed.

3.1 INTRODUCTION

In 1975 first time the idea of MLI has been presented with an improvement of three level inverter. Presently today numerous sorts of MLI topologies have been created. In the early time of advancement of idea of MLI, to get higher power, arrangement of power semiconductor switches with a few lower voltage dc sources had been utilized to perform the power transformation by incorporating the stair case voltage waveform. Multilevel inverters have increased much consideration for the cutting edge medium voltage and high power applications. Three-level DCMLI topology is the most great among different multilevel arrangements, displayed in the writing. Number of papers are distributed in the zone of three level inverter demonstrates the significance of exploration on this topology. The majority of the

work is centered around particular issues like improving the control calculation, usage issues, decreasing harmonic losses, diminishing switching losses, neutral point voltage adjusting, operation in over-modulation, or decreasing common mode voltage. The three level inverter is widely applicable for medium voltage high power system. The primary elements of the three-level inverter incorporate decreased rate of change of voltage with respect to time and THD in its ac output voltages in contrast with the two-level inverter. All the more importantly, the inverter can be utilized as a part of the MV drive to achieve a specific voltage level without switching devices in series.Presently batteries, capacitors and renewable energy sources are utilized as the various dc voltage sources. The need of numerous dc sources rearranges the usage of low voltage energy sources, as photovoltaic energy source. Through MLI different renewable energy sources can be associated specifically without the need of whatever other circuitry.

3.2 ADVANTAGES AND DISADVANTAGES OF MLI

With respect to conventional tow-level inverter a multilevel inverter has many advantages, the MLI uses PWM at high switching frequency. Some features of MLI is briefly discussed as follows.

1. **Stepped waveform** : Because of stepped voltage wave form multilevel inverter not even reduces distortion in output voltage, but also reduces the dv/dt stress, as a result problem of electromagnetic compatibility (EMC) also reduces.

2. **Input current** : The distortion in input current drawn by multilevel inverters can low.

3. **Common mode** (CM) **voltage** : The common mode voltage produced by multilevel inverter is smaller than the conventional two-level inverter, therefore the ground current flowing through the bearing of the motor connected to multilevel inverter fed motor drive is decreased. Furthermore, by using

appropriate advanced modulation strategies the CM voltage can be fully eliminated.

4. **Switching frequency** : The switching frequency decides the switching losses, for low switching frequency the losses will be less therefore higher efficiency and for higher switching frequency losses will be more therefore efficiency is less. The multilevel inverter can operate at both fundamental switching frequency and high switching frequency PWM depending upon the application.

3.3 MULTILEVEL POWER CONVERTER TOPOLOGIES

Below figure shwos one way to classify multilevel converters, similar to the classification by Lai and peng [22].

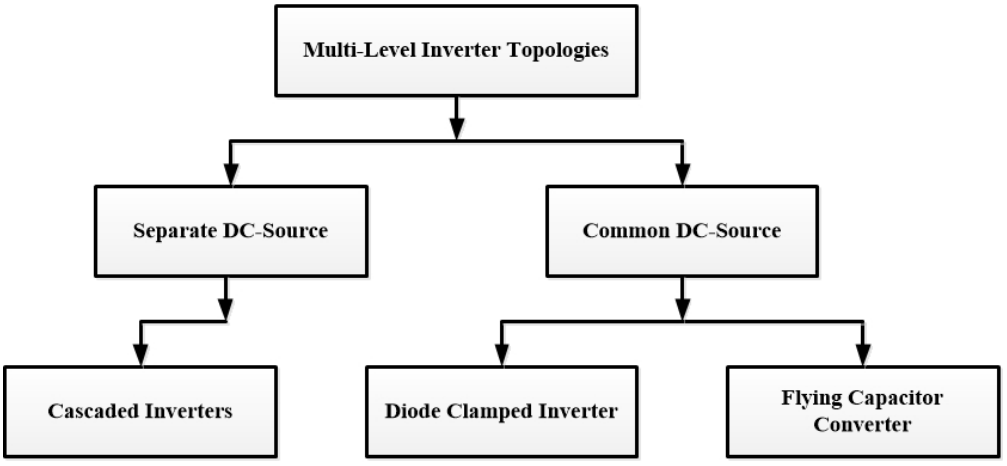

FIGURE 3.1: classifications of Multi-level converters

The research on multilevel inverter are going on since last two decades. In the 1990s, a few specialists articles on application on multilevel inverters in the field of variable speed motor drives, interconnection of high voltage systems and static var compensation. By increasing the number of voltage levels the output voltage is approaches the sinusoidal wave which has minimum harmonic distortion.

3.4 NEUTRAL POINT CLAMPED (NPC) MLI

The three level diode clamped MLI is proposed by Nabae, Takahashi, and Akagi [39] in 1981 is also known as neutral point converter. An n-level DCMLI requires (n-1) dc link capacitors, 2(n-2) clamping diodes/phase and 2(n-1) number of switches per phase.was essentially a three level diode clamped inverter. Figure.3.2 shows the simplified circuit diagram of three level NPC inverter. The DC link capacitor is used to split the DC bus into three levels of output voltage, Cd1 and Cd2, providing a neutral point. The voltage across split capacitor is Vd/2(=E) volts and therefore the voltage stress across each switch is decreases. The clamping diodes Dz1 and Dz2 are connected to the neutral point. The inverter output terminal A is connected to the neutral point when the switches S2 and S3 for leg-a are turned on simultaneously through a clamping diode. The switching state of the inverter is shown in table 3.1. The clamping diode are required for three level DCMLI while it is not needed in two level inverter.

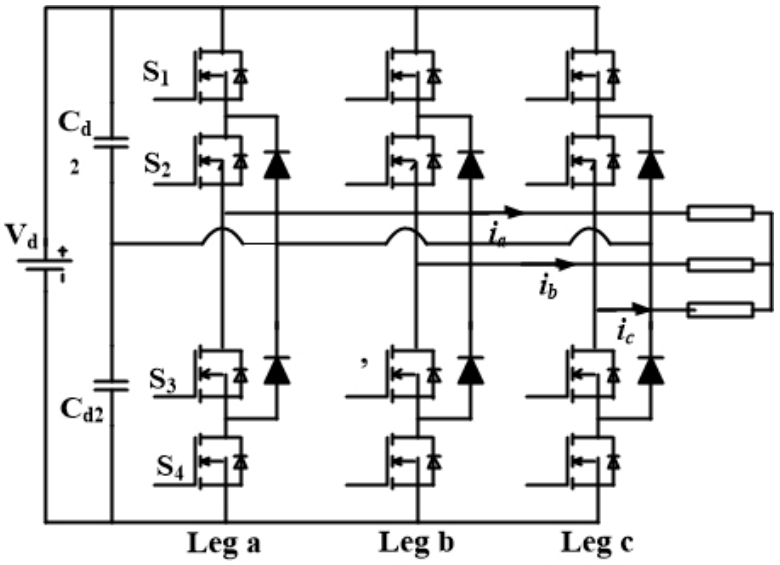

FIGURE 3.2: Three level NPC Inverter

The table 3.1 shows the switching states for the three level NPC inveter. AT switching state 'P' the switches S1 and S2 are on and the voltage of (+E) is generated at inverter terminal. At switching state 'O' switch S2 and S3 are turned on simultaneously, the zero output voltage is generated. At switching state 'N' S3 and S4 switches are turned on simultaneously and the inverter terminal voltage -E is generated at the terminal V_{AZ}.

TABLE 3.1: Definition of Switching State

Switching State	Device Switching Status (leg-a)				Inverter Terminal Voltage (V_{an})
	S1	S2	S3	S4	
P	ON	ON	OFF	OFF	+E
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-E

The list of component used for NPC is given in Table 3.2. The output voltage of the inverter is depend on the rating of the switches used. Therefore the maximum output voltage is increases by increasing the number of switches used.

TABLE 3.2: Component count of diode clamped multilevel inverters

Voltage level	Active switches	Clamping diodes	Dc capacitors
m	6(m-1)	3(m-1)(m-2)	(m-1)
3	12	6	2
4	18	18	3
5	24	36	4
6	30	60	5

Features

- For three level NPC the voltage rating of the switches required is just half of the DC link voltage applied.
- The DC link capacitor voltage can be equalize by selecting the leakage current of outer switches for a particular leg of an inverter is lower than the inner switches.

Application

- The diode clamped MLI is used in the high voltage dc transmission as a interface between ac an dc transmission line.
- Also used in high power, medium voltage (2.4 kV to 13.8 kV) variable speed motor drives.

Advantages

- The capacitors can be pre charged as a group.
- Efficiency is high for fundamental. All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter.

Disadvantages

- Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.
- The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels.
- For higher levels the different voltage rating clamping diodes are required to bock reverse voltage. The rating of the switches required must have the voltage rating of Vdc/(m-1). (m-1)*(m-2) number of diodes required for each phase.Therefor the system become more complex for higher levels.
- Capacitor voltage unbalance.

3.5 FLYING CAPACITOR MLI

The general concept behind flying capacitor MLI is that the added capacitor is charged to one half of the DC-link voltage and may be inserted in series with the DC link voltage to form an additional voltage level. Figure 3.3 shows one phase of a three-level flying capacitor MLI. As can be seen, switching states involve gating on the two lower and upper transistors as was done with the diode clamped structure. The capacitor voltage may be either added to the converter ground or subtracted from the DC-link voltage.

In essence, there is switching redundancy within the phase leg. Since the direction of the current through the capacitor changes depending on which redundant states

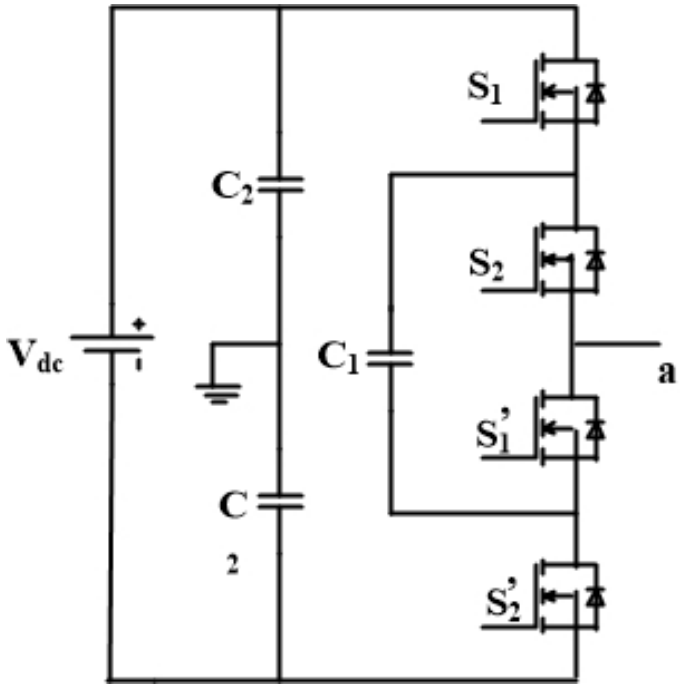

FIGURE 3.3: One phase leg of three level Capacitor Inverter

is selected, the capacitor voltage may be maintained at one half the DC-link voltage through the redundant state selection with in the phase.

Application

- The flying capacitor MLI is widely used in facts devices like SVC.

Advantage

- By using the redundant switching states the voltage levels of capacitors can be balanced.
- The flow of real and reactive power can also be controlled.
- Inverter sustain voltage sag and short duration outages due to the capacitors.

Disadvantages

- Pre charging of all the capacitors is required therefore startup are complex.
- efficiency is very less for active power flow.

- The size and cost of the capacitors are higher than the diodes used in NPC MLI.
- FCMLI are costlier than DCMLI and H-bridge MLI for higher level.

3.6 CASCADED H-BRIDGE MLI

The number of modules are connected in series and each module requires isolated DC supply source to achieve higher level of output voltage. A three level H-bridge inverter is shown in Figure 3.4. Two h-bridge modules are connected in series to generate a three stepped voltage. The two isolated DC sources are required to generate the three level output voltage while DCMLI and FCMLI required only one DC source. This H-bridge topology is mainly used to interconnect the different DC supply sources like fuel cell, solar PV, battery etc.

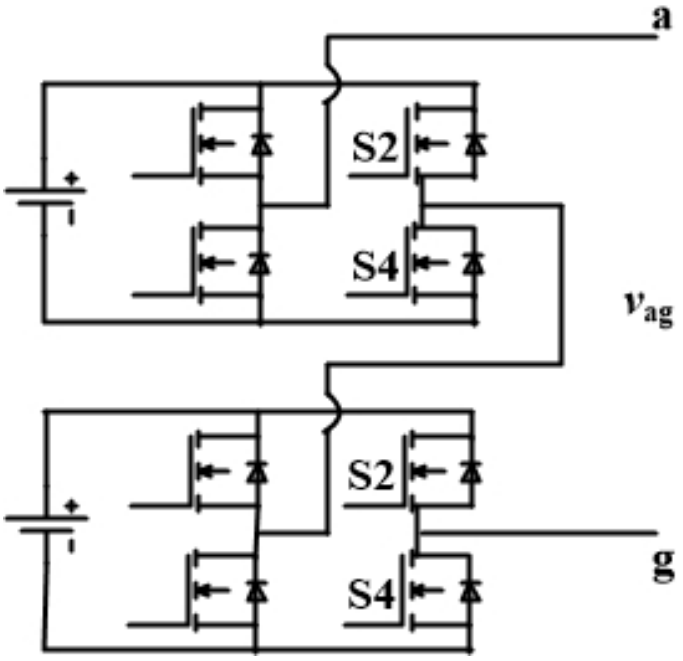

FIGURE 3.4: Cascaded H-bridge topology with two cells

Features

- H-bridge inverter required a isolated DC sources. This feature of the h-bridge MLI make it unique and widely applicable in the field of renewable energy resources to interconnect them.

Application

- The H-bridge inverter is widely applicable on power factor improvement devices.
- Widely applicable in FACTS devices.
- Interconnection between various renewable energy resources and with an AC grid.
- The cascaded h-bridge module have an ability to operate as rectifier for charging the batteries and ultra capacitors which is generally used in electric vehicle.

Advantages

- The number of possible output voltage levels are more than twice the number of dc sources (m=2s+1), where, m is the level of output voltage and, s is the no of dc sources connected.
- This inverter is a combination of several isolated modules, therefore easy to package and transport.

Disadvantages

- To achieve a higher level a number of isolated DC sources are required.

3.7 NOVEL CASCADED MLI

A cascaded three-level novel inverter is used to convert DC-AC power by connecting to two level inverter module in cascaded form as shown in Figure-3.5. Figure-3.5 shows that the output phases of inverter-1 (top inverter) are connected to the DC-input points of second inverter at respective phases. The proposed inverter requires two independent DC power supplies for both inverter modules. This is considered as an advantage for connecting PV arrays to supply a common

load [5, 12]. This multilevel inverter topology is advantageous as compared to basic three DCMLI, FCMLI and H-bridge MLI topologies. The proposed topology does not require any clamping diodes or flying capacitors unlike DCMLI and FCMLI respectively. The number of DC source and number of switches required in this topology is less as compare to H-bridge MLI. [12, 15, 16]

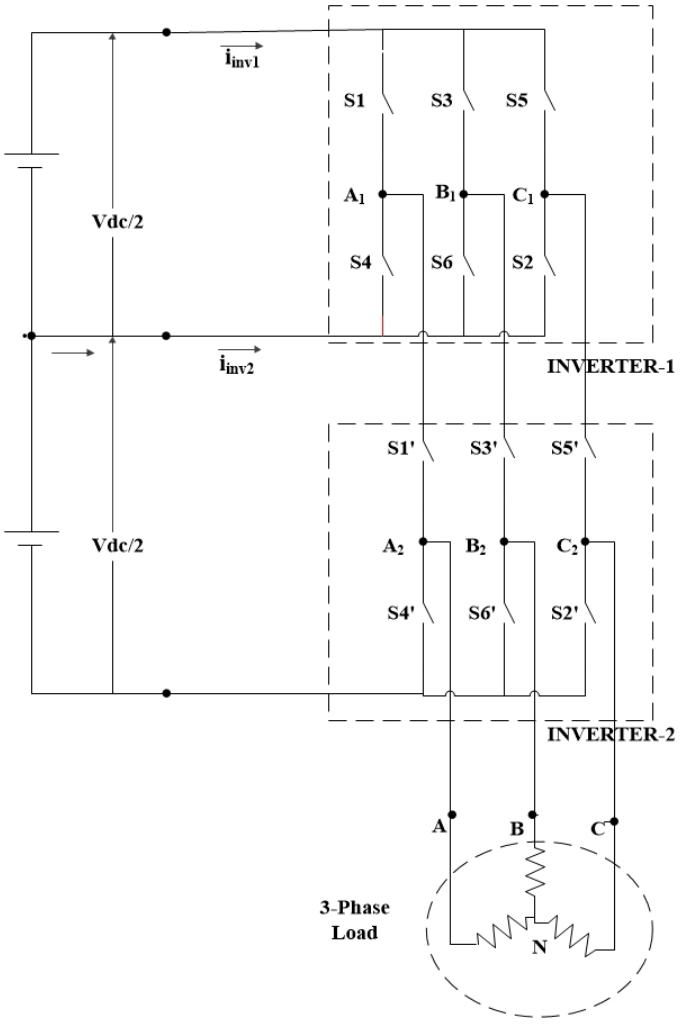

FIGURE 3.5: The circuit configuration of cascaded three-level inverter

In the figure-3.5 the pole voltages of inverter-1 with respect to the point 'O' are denoted as v_{A10}, v_{B10}, and v_{C10} respectively. Similarly, the pole voltages of inverter-2, with respect to the point 'O' are denoted as v_{A20}, v_{B20} and v_{C20} respectively. For the same leg of both inverters if the top switch ($S'1$) of inverter-2 and the bottom switch (S4) of inverter-1 are turned on simultaneously, the pole voltage of that leg or phase (v_{A20}) for inverter-2 is Vdc/2 as shown in figure-3.6.

Similarly if the top switch of inverter-2 and top switch of inverter-1 for the same leg is turned on simultaneously, then the pole voltage of a particular phase for

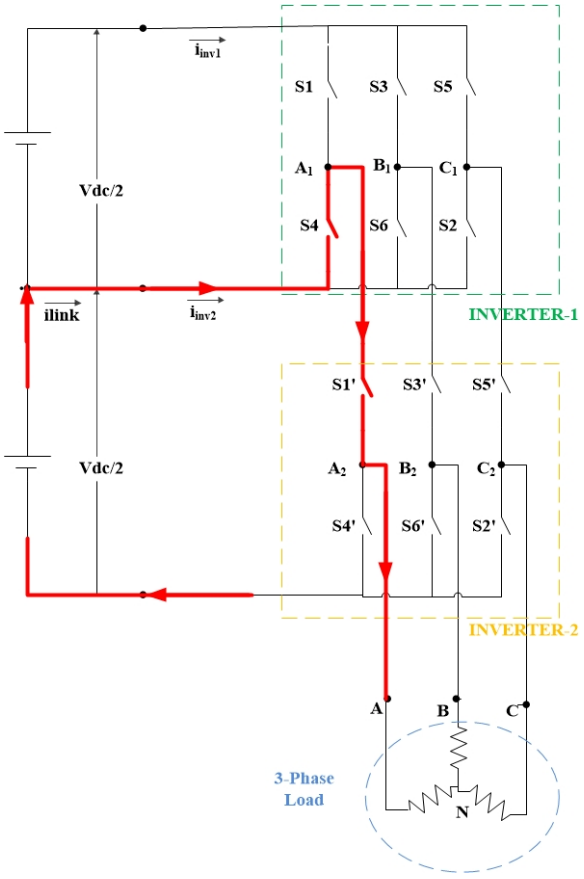

FIGURE 3.6: switching states for Vdc/2 Pole voltage (V_{A20})

inverter-2 is Vdc as shown in figure-3.7. Thus the switching states of the inverter-1 for a particular leg decide the pole voltage (Vdc or Vdc/2) of a particular phase of inverter-2. [12]

If bottom switch of inverter-2 is turned on with any switching states of inverter-1 for a same leg, then the pole voltage of inverter-2 for that phase is zero. Therefore the pole voltage of inverter-2 is having three possibilities 0, Vdc/2, Vdc, which shows the characteristic of any three level inverters.

The proposed MLI switching table for leg-a is given in table-3.3. In Figure-3.5 leg-a contain switches S1, S4 of inverter-I and $S'1$ and $S'4$ of inverter-II. In table-I, 'O' stands for off state of the switch, '1' stands for on state of the switch, and 'X' stands for redundant state, i.e. the switch may on or off, there is no effect in the output voltage.

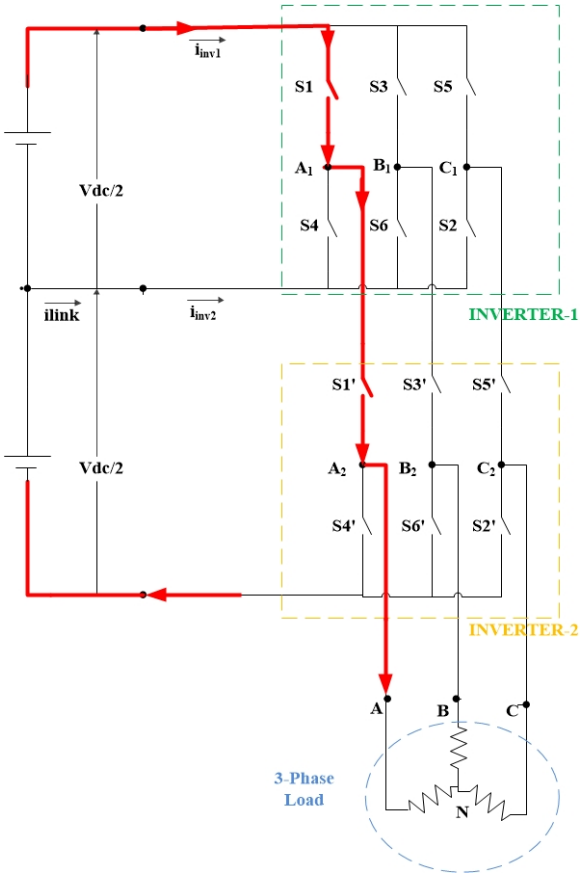

FIGURE 3.7: switching states for Vdc Pole voltage (V_{A20})

TABLE 3.3: Definition of Switching State

Output Voltage	Switching Invertet-I		Status (leg-a)	Switching Invertet-II		Status (leg-a)
	S1		S2	S'1		S'2
0	X		X	0		1
Vpv/2	0		1	1		0
Vpv	1		0	1		0

3.7.1 swithing logic

The space vector Vs is constituted by the pole voltages V_{A20}, V_{B20}, V_{C20} is defined as :

$$V_s = V_{A20} + V_{B20}e^{2pi/3} + V_{C20}e^{4pi/3} \tag{3.1}$$

The 64 combinations of pole voltages are shown by 19 space vector locations similar

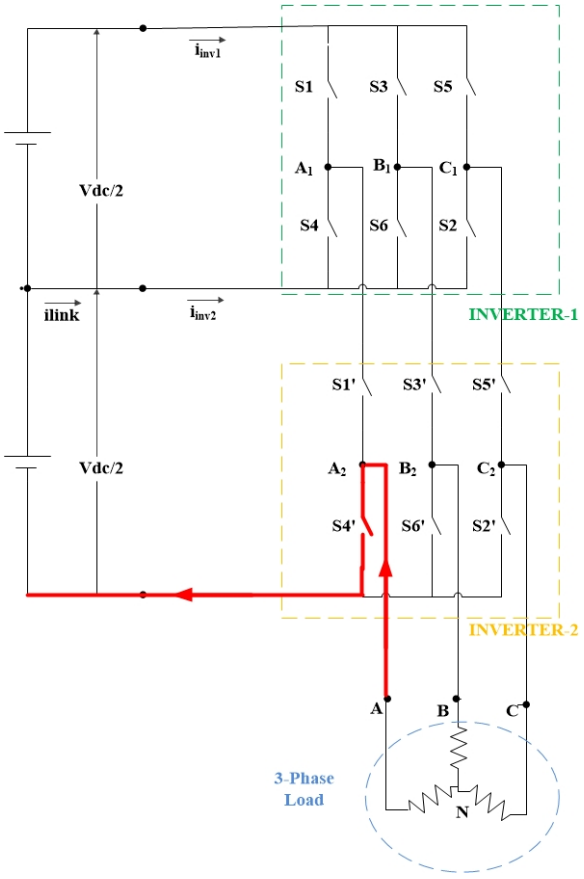

FIGURE 3.8: switching states for Zero Pole voltage (V_{A20})

to a conventional three level inverters is shown in figure-3.9 and the switching states of both inverters are given in table-3.4.

From figure-3.9 it is clear that redundancies of the space vector combinations for a particular space vector location are present. For example, for the state of $1'$ (+ - -) of inverter-2, the points B_2 and C_2 are shorted to the point 'O' through switches $S'6$ and $S'2$. The DC-input for these two phases are blocked by $S'3$ and $S'5$ because for the same leg top and bottom switches are complementary in a two level inverter.to connect the DC-input of inverter-2 to Vdc/2, the states of inverter-1 should be any of 8 (- - -), 3 (- + -), 4 (- + +), and 5 (- - +). Therefore combinations 8-$1'$, 3-$1'$, 4-$1'$, 5-$1'$ gives the same location A as shown in figure-3.9. Only few combinations from the redundancies are selected for a given location to implement the space vector modulation for simplicity as shown in figure-3.9.

Features

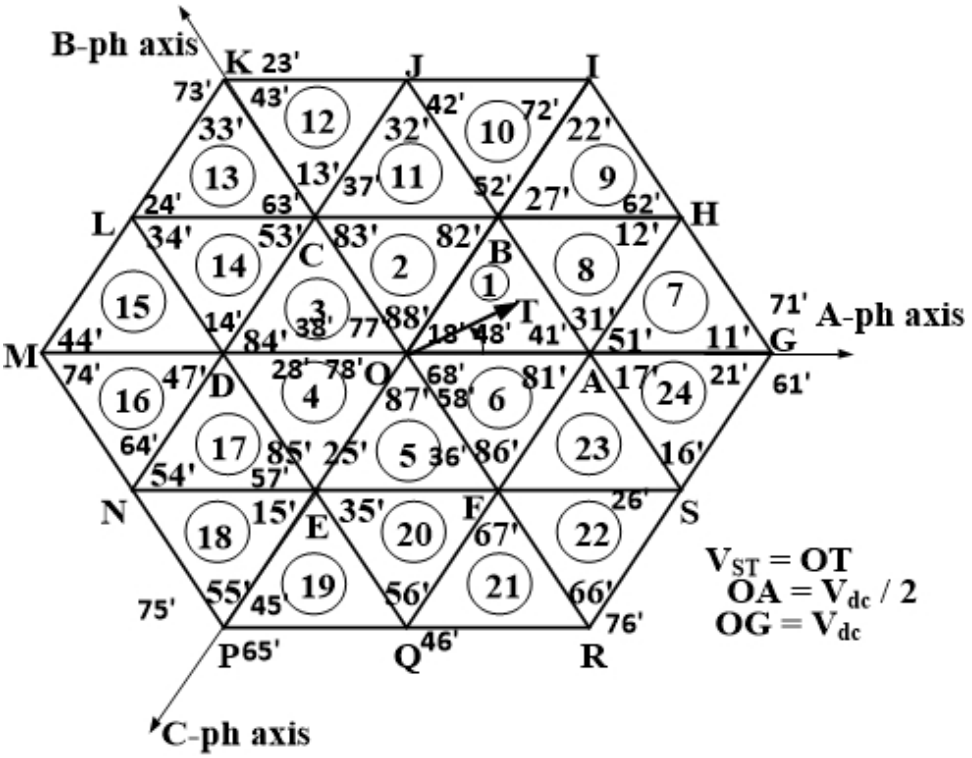

FIGURE 3.9: Space vector locations and combinations in the novel cascaded inverter

TABLE 3.4: Inverter states for individual inverters

States of inverter-1	Switches turned on	States of inverter-2	Switches turned on
1 (+ - -)	S6, S1, S2	1' (+ - -)	S6', S1', S2'
2 (+ + -)	S1, S2, S3	2' (+ + -)	S1', S2', S3'
3 (- + -)	S2, S3, S4	3' (- + -)	S2', S3', S4'
4 (- + +)	S3, S4, S5	4' (- + +)	S3', S4', S5
5 (- - +)	S4, S5, S6	5' (- - +)	S4', S5', S6'
6 (+ - +)	S5, S6, S1	6' (+ - +)	S5', S6', S1'
7 (+ + +)	S1, S3, S5	7' (+ + +)	S1', S3', S5'
8 (- - -)	S2, S4, S6	8' (- - -)	S2', S4', S6'

- Reduced number of dc power supply is required with respect to conventional H-bridge MLI.

- Control strategy is as simple as DCMLI.
- The components required are less as compared to other basic multilevel inverters.

Application

- This MLI converter can be used to interface with renewable energy or distributed energy resources because several batteries, fuel cells, solar cells, wind turbines, and micro turbines cab be connected through a multilevel converter to supply a load or the ac grid without voltage balancing problems.
- Multilevel inverter technology has emerged recently as very important alternative in area of high power medium voltage control, power inverter modules fed with separate dc voltage sources of voltage ratio 15V/30V/120V are connected to form a cascaded MLI.
- This MLI configuration is suitable for three level inversion in low voltage high power applications like battery operated electrical vehicle drives.

Advantages

- If the modulation index is less than 0.433, ie. if Vsr<0.433Vdc, the inverter-1 is always clamped to the state 8 (- - -) and inverter-2 alone is operated, or inverter-2 can be clamped to the state 7 (+ + +) and inverter-1 could be operated.
- For modulation index less than 0.433 the switching losses are due to the switching of one of the inverters and are less than the other basic MLI topologies.
- This MLI can also be operated with a single DC power supply, with tapped capactiors like DCMLI with conventional 3-level switching schemes.
- When compared to conventional NPC MLI the novel cascaded MLI is not needed any fast recovery clamping diodes.

- When compared to conventional FC MLI the novel cascaded MLI is not needed large number of clamping diodes, which makes the circuitry simple and light in weight.
- Easy to assemble such a system, as only two existing two-level inverter is retrofitted to get this configuration. The bus bar design for two-level inverter is simpler than the conventional three level inverters.
- This configuration gives higher efficiency for lower modulation index.

Disadvantages

- Separate dc sources are required for each of the inverter and these sources are connected in series therefore current rating must be same.
- The bottom switches of inverter-2 are to be rated for the full DC-bus voltage of Vdc, unlike to conventional NPC MLI.

3.8 CONCLUSION

The elementary concept of a multilevel inverter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing the staircase voltage waveform has been discussed. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output. There are several advantages to this approach when compared with traditional (two-level) power conversion. The smaller voltage step lead to the production of higher power quality waveforms and also reduce the dv/dt stress on the load and reduces the electromagnetic compatibility (EMC) concerns. The advantages, features and applications of basic MLI with novel Cascaded MLI have been discussed. The novel cascaded MLI is proved a good choice then the other basic MLI configuration with some extent.

Chapter 4

Modulation Strategies

This chapter focuses on various PWM techniques available for multilevel inverters and their implementation. The main objective of this chapter is to explain implementation of Sinusoidal Pulse Width Modulation (SPWM), Third Harmonic injection SPWM, Multi carrier PWM and Space Vector Pulse Width Modulation (SVPWM) techniques for three-level novel cascaded inverter. The common mode voltage elimination method for three-level inverter is also discussed.

4.1 INTRODUCTION

The inverter contains electronics switches, it is possible to control output voltage as well as optimize the harmonics by performing multiple switching with in the inverter with the constant dc input voltage. Various modulation strategies have been developed. Moreover, abundant modulation techniques and control paradigms have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others. Among these strategies, space-vector modulation (SVM) stands out because it offers significant flexibility to optimize switching waveforms, and because it is well suited for implementation on a digital computer. However, regardless of its advantages, SVM for more than three-level

converters is still mostly unexplored. This is largely consequence of increasing computational difficulties for converters with a higher number of levels. In addition, many multilevel converter applications focus on industrial medium-voltage motor drives, utility interface for renewable energy systems, flexible ac transmission system (FACTS) and traction drive systems.

4.2 MULTILEVEL CONVERTER PWM STRATEGIES

The pulse width modulated inverters make use of different modulation schemes such as classification of PWM multilevel converter modulation strategies as shown below:

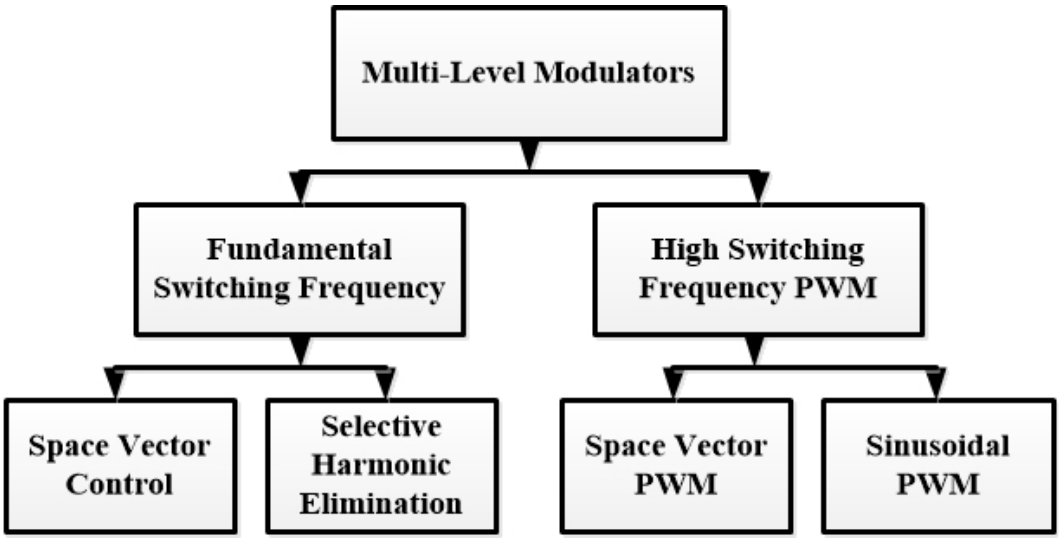

FIGURE 4.1: Classification of PWM multilevel converter modulation strategies

The following are some major concerns when comparing different PWM techniques:

- Good utilization of DC power supply i.e. to deliver a higher output voltage with the same DC supply.
- Good linearity in voltage and or current control.
- Low harmonics contents in the output voltages specially in the low-frequency region.

- Low switching losses.

The advantage of PWM based switching power converter over linear power amplifier is:

- Easy to implement and control.
- No temperature variation and aging-caused drifting or degradation in linearity.
- Compatible with todays digital micro-processors
- Lower power dissipation.

4.3 SINUSOIDAL PULSE WIDTH MODULATION (SPWM)

The principle of the sinusoidal PWM scheme for the two-level inverter is illustrated in figure 4.2, where V_{mA}, V_{mB}, and V_{mC} are the three-phase sinusoidal modulating waves and Vr is the triangular carrier wave. The fundamental-frequency component in the inverter output voltage can be controlled by amplitude modulation index:

$$m_a = \frac{V_m}{V_{cr}} \tag{4.1}$$

Where Vm and V_{cr} are the peak values of the modulating and carrier waves, respectively. The amplitude modulation index m_a is usually adjusted by varying Vm while keeping V_{cr} fixed. The frequency modulation index is defined by:

$$m_f = \frac{f_{cr}}{f_m} \tag{4.2}$$

Where, f_m and f_{cr} are the frequencies of the modulating and carrier waves, respectively.

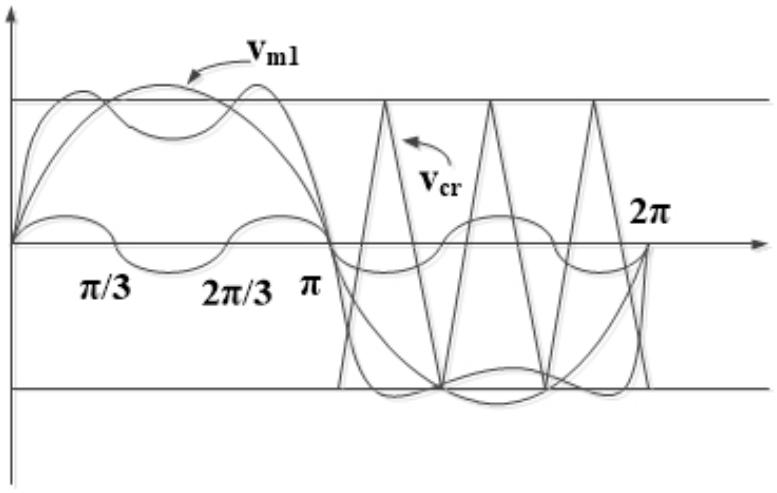

FIGURE 4.2: Modulating wave VmA with third harmonic injection

Several multicarrier techniques have been developed to reduce the distortion in multilevel inverters, based on the classical SPWM with triangular carriers. Some method use carrier disposition and other use phase shifting of multiple carrier signals. A very common practice in industrial applications for the multilevel inverter is the injection of a third harmonic in each cell to increase the output voltage. Another advantageous feature of multilevel SPWM is that the effective switching frequency of the load voltage is times the switching frequency of each cell, as determined by its carrier signal. This property allows a reduction in the switching frequency of each cell, thus reducing the switching losses.

4.4 THIRD HARMONIC INJECTION PWM

The inverter fundamental voltage V_{AB} can also be increased by adding a third harmonic component to the three-phase sinusoidal modulating wave without causing over modulation. This modulation technique is known as third harmonic injection PWM. Figure-4.2 illustrates the principle of this PWM scheme, where the modulating wave V_{mA} is composed of a fundamental component V_{m1} and a third harmonic component V_{m3}, making V_{mA} somewhat flattened on the top. As a result, the peak fundamental component V_{m1} can be higher than the peak triangular carrier wave V_{cr}, which boosts the fundamental voltage V_{AB1}. In the meantime the peak modulating wave V_{mA} can be kept lower than V_{cr}, avoiding the problems

caused by over modulation. The maximum amount of V_{AB1} that can be increased by this scheme is 15.5%. [22, 23]

4.5 SPACE VECTOR PULSE WIDTH MODULATION

Among various modulation techniques for a multilevel inverter, space vector pulse with modulation (SVPWM) is an attractive candidate due to the following merits. It directly uses the control variable given by the control system and identifies each switching vector as a point in complex (α, β) space. It is suitable for digital signal processor (DSP) implementation. It can optimize switching sequences. The space-vector PWM method is and advanced computation-intensive PWM method and is possible the best among all the PWM techniques because for a three phase inverter makes it possible to adapt the switching behavior to different situation such as: half load, full load, linear load, non-linear load, static load, pulsating load, etc., and the following are the advantages.

Very low values can be reached for the output voltage THD, robust dynamic response, the efficiency of the inverter can be optimized for each load condition and SVPWM enables more efficient use to the DC voltage (15 percent more than conventional PWM techniques). SVPWM is one of the preferred real-time modulation characteristics, and is widely used for the digital control of voltage source inverters. It is an advanced, computation intensive PWM and possibly the best among all the PWM techniques for variable frequency drive applications. The space vector diagram of any three-phase n-level inverter consists of six sectors. Each sector consists of $(n-1)^2$ triangles. The tip of the reference vector can be located within any triangle. Each vertex of any triangle represents a switching vector. A switching vector represents one to more switching states depending on its location. There are n^3 switching states in the space vector diagram of an n-level inverter. The SVM is performed by suitably selecting and executing the switching states of the triangle for the respective on-times. The performance of the inverter significantly depends on the section of these switching states. The space vector

diagram of a three-level inverter is shown in figure 3.5 there are six sectors (S1-S6), four triangles in each sector, and a total of 27 switching states in this space vector diagram. As level 'n' increases, the increased number of triangles, switching states, and calculation of on-times adds to the complexity of SVM for multilevel inverters. There are two common approaches to obtain the on-times. The first approach is to determine the triangle, and then solve three simultaneous equations for this triangle to obtain the on times. Whereas, the second approach is to determine the triangle, and then use the particular on-time equations stored in the lookup for this triangle, as in. However, as the number of level increases, both of these approaches become computationally intensive. Figure 4.3 space vector diagram of the 3-level inverter Wei et al. propose an algorithm which uses 60^0 co-ordinate systems to calculate on-times and determine switching states. Since most control schemes provide a voltage reference in α - β coordinates, the 60^0 transformation adds to complexity.

4.5.1 Space Vectors

As indicated earlier, the operation of each inverter phase leg can be represented by three switching states P, O and N. taking all three phases in account, the inverter has a total of possible combination of switching states. Figure 4.3 shows space vector diagram of total 24 swithcing states for three-level inverter. Switching states corresponding to 19 voltage vectors with sector and region definitions are shown in the figure 4.4. the numbers shown in circles indicated region number in each sector. Figure 4.5 shows vector placement and region numbers in sector 1. Based on magnitude, the voltage vectors can be divided into four groups: zero vector ($\overline{V_0}$), small vector ($\overline{V_M}$), and large vectors ($\overline{V_L}$). All zero vectors have zero magnitude, small vectors have a magnitude of $\frac{V_{dc}}{2}$, medium vectors have magnitude of $\frac{\sqrt{(3)}*V_{dc}}{2}$ and large vectors have magnitude of V_{dc}. Each small vector has two switching states, one containing P and other containing N, and therefore can be further classified in ta P-type or N-type vector. Table 4.1 summarizes various space vectors, switching states corresponding to space vectors, their vector classification and vector magnitude.

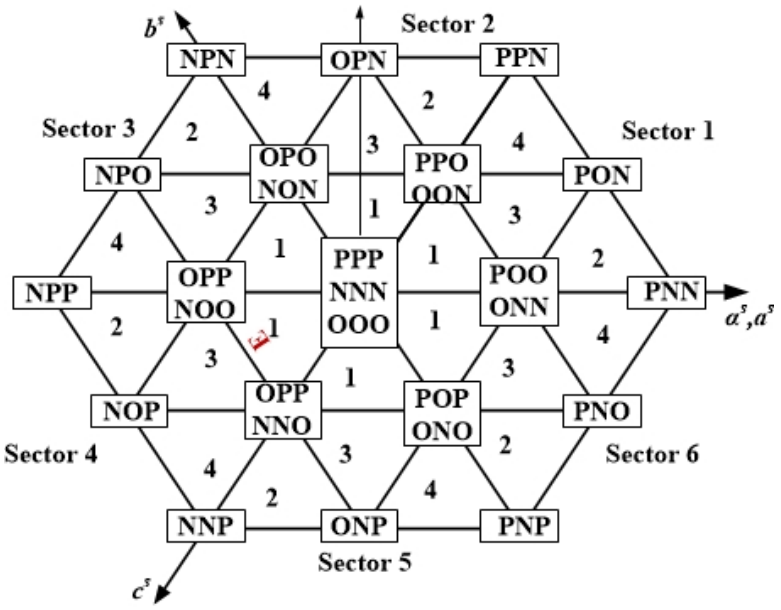

FIGURE 4.3: Space-vector diagram showing switching states for three-level inverter

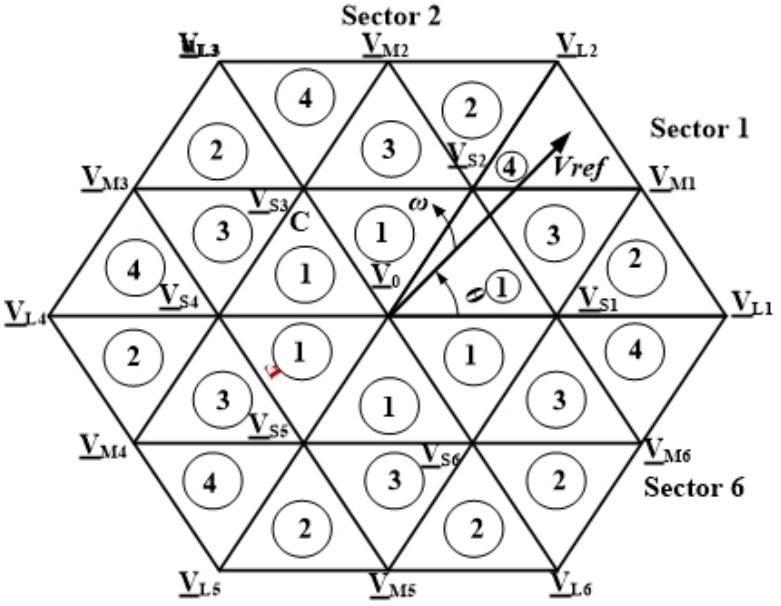

FIGURE 4.4: Space vector with sector and region definition for three-level inverter

4.5.2 classification, magnitude and switching state of space vectors

A generalized methodology to calculate dwell time and triangular regions in SVPWM is used to generate switching pulses for three-level inverter based on simple coordinate system transformation is presented here.

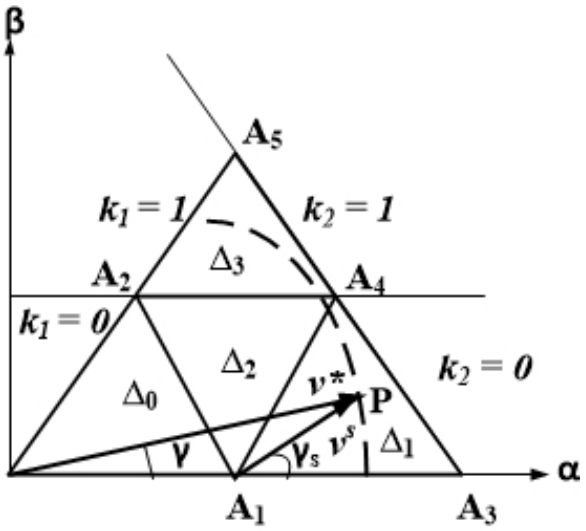

FIGURE 4.5: Space vector placement and regions in sector 1

The number of switching states, $N_{sw-state}$, for three-level inverter is given by

$$N_{SW-STATE} = 3^3 = 27 \tag{4.3}$$

Total number of voltage space vectors, N_{SV}, can be given by

$$N_{SV} = 3^3(3-1)^3 = 19 \tag{4.4}$$

Total number of triangle, N_T, in space vector diagram can be given by

$$N_T = 6(3-1)^2 = 24 \tag{4.5}$$

The goal of SVPWM is to compensate the required volt-second using discrete switching states and their on-times. This is achieved by means of the time averaging of the nearest three vectors as given by equation 4.7

$$\overline{V_1}.t_a + \overline{V_2}.t_b + \overline{V_3}.t_0 = \overline{V_{ref}}.T_s \tag{4.6}$$

$$t_a + t_b + t_0 = T_s \tag{4.7}$$

TABLE 4.1: classification, magnitude and switching state of space vectors

Spave Vector		Switching State		Vector Classification	Vector Magnitude
$\overline{v}_0$		[PPP][OOO][NNN]		Zero Vector (ZV)	0
		P-type	N-type		
$\overline{v}_{s1}$	$\overline{v}_{s1P}$	$[\underline{P}OO]$	-	Small Vector (SV)	$\frac{1}{2}V_d$
	$\overline{v}_{s1N}$	-	$[\underline{O}NN]$		
$\overline{v}_{s2}$	$\overline{v}_{s2P}$	[PP$\underline{O}$]	-		
	$\overline{v}_{s2N}$	-	[O$\underline{O}$N]		
$\overline{v}_{s3}$	$\overline{v}_{3P}$	[O$\underline{P}$O]	-		
	$\overline{v}_{s3N}$	-	[N$\underline{0}$N]		
$\overline{v}_{s4}$	$\overline{v}_{s4P}$	[O$\underline{P}$P]	-		
	$\overline{v}_{s4N}$	-	[N$\underline{O}$O]		
$\overline{v}_{s5}$	$\overline{v}_{s5P}$	[O$\underline{O}$P]	-		
	$\overline{v}_{s5N}$	-	[N$\underline{N}$O]		
$\overline{v}_{s6}$	$\overline{v}_{s6P}$	[P$\underline{O}$P]	-		
	$\overline{v}_{s6N}$	-	[O$\underline{N}$O]		
$\overline{v}_{m1} = \underline{v}_m$		[PON]		Medium Vector (MV)	$\frac{\sqrt{3}}{2}V_d$
$\overline{v}_{m2}$		[OPN]			
$\overline{v}_{m3}$		[NPO]			
$\overline{v}_{m4}$		[NOP]			
$\overline{v}_{m5}$		[ONP]			
$\overline{v}_{m6}$		[PNO]			
$\overline{v}_{L1} = \underline{v}_L$		[PNN]		Large Vector (lV)	V_d
$\overline{v}_{L2}$		[PPN]			
$\overline{v}_{L3}$		[NPN]			
$\overline{v}_{L4}$		[NPP]			
$\overline{v}_{L5}$		[NNP]			
$\overline{v}_{L6}$		[PNP]			

The proposed scheme is explained with the help of a three level novel Cascaded inverer topology as shown in the figure 3.5. The scheme is equally applicable to cascaded H-bridge inverter with slight modifications. Figure 4.5 shows the space vector diagram of sector-1 for a three-level inverter. Each sector consists 4 triangles, named T_j where j=1 to 4. here, V_{ref} is the reference vector of magnitude

$|V_{ref}|$ at angle θ with α-axis. Modulation index (MI), varies from 0 to 1 in complete mode of operation and $|V_{ref}|$ from the MI and number of level, 3 of MLI can be given by

$$|V_{ref}| = 3MI(3-1)/\pi \tag{4.8}$$

Computaion of dwell times in sector-1 is applicable to other sectors due to the symmetry in the space vector diagram and transformation of θ to θ' such that

$$\theta' = rem(\frac{\theta}{\pi/3}) \tag{4.9}$$

Sector number, S_r can be given by

$$S_r = int(\frac{\theta}{\pi/3}) + 1 \tag{4.10}$$

where, θ ($0 \leq \theta < 2\pi$) is the angle of the reference vector with α-axis.

TABLE 4.2: Three-level cascaded inverter switching states (single-leg)

Output Voltage	Switching Invertet-I (leg-a)		Switching Invertet-II (leg-a)		Level notaion
	S1	S2	S'1	S'2	
0	X	X	0	1	1
Vpv/2	0	1	1	0	2
Vpv	1	0	1	0	3

4.5.3 Dwell Time Calculation

Initially, coordinates of reference vector V_{ref} in $\alpha-\beta$ plane at origin A are modified according to axis separated by 60^0 and thereafter transformed to either origin A_1 or A_4 depending upon location of the reference vector V_{ref}.

The components of the reference vector, (V_α, V_β) in the $\alpha - \beta$ plane can be given by

$$\begin{cases} V_\alpha = |V_{ref}|cos(\theta') \\ V_\beta = |V_{ref}|sin(\theta') \end{cases} \tag{4.11}$$

In order to simplify equation-4.7, co-ordinate system is transformed from the initial origin $A0$ to another point A_1 such that one of the vectors in the equation 4.12 becomes zero and dependent only on two vectors. This translation can be done step-by-step given below: The reference vector components with respect to new origin A_1 can be given by

$$\begin{cases} \bar{V}_{\alpha i} = V_\alpha - k_1 + 0.5k_2 \\ \bar{V}_{\beta i} = V_\beta - k_2 H \end{cases} \tag{4.12}$$

For all the sectors on-time calculations are same therefore the time caluclation for sector-1 is only considered.

Every sector contains four triangles. As shown in Figure-4.6 the reference vector belongs to two possible regions, lower region (type-1) and upper region (type-2). The type-1 triangle has the base at bottom of the sector, and triangle of type-2 has the base at the top. Triangle Δ_0, Δ_1 and Δ_3 are of type-1 and Δ_2 is of type-2.

4.5.4 Identification of Triangle

The reference vector can be present at any triangle in a sector. The triangle where reference vector tip is situated is treated as sector of two level inverter.

The integral K_1 and K_2 are used to find the triangle in which tip of the reference vector is situated. Let $V_{\alpha 0}$ and $V_{\beta 0}$ are the coordinates of the of V_{ref}, therefore K_1 and K_2 in terms of $V_{\alpha 0}$ and $V_{\beta 0}$ are:

Region identification factor (RID) can be defined by

$$\begin{cases} K_1 = int(v_\alpha + V_\beta) \\ K_2 = int(V_\beta / H) \end{cases} \tag{4.13}$$

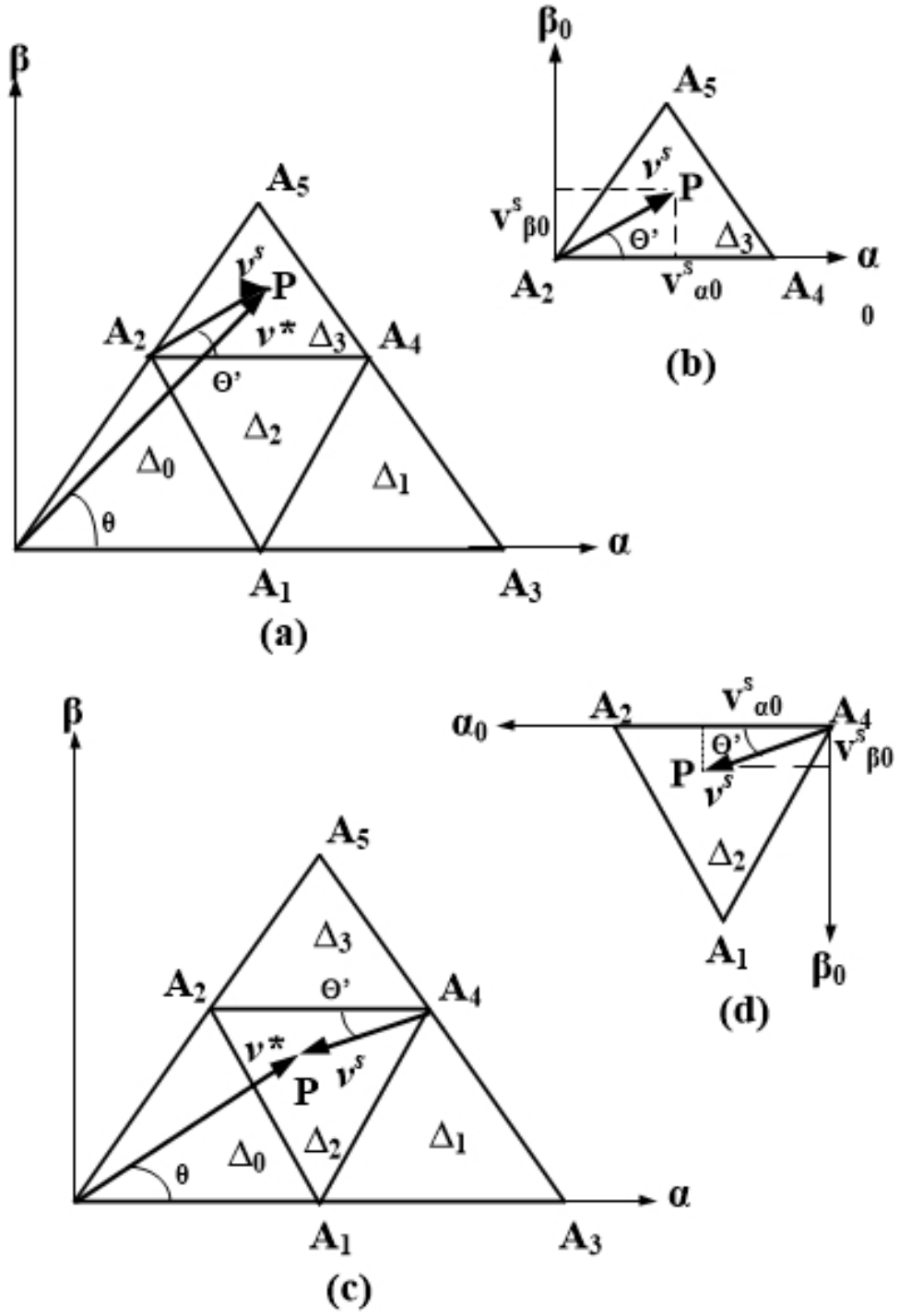

FIGURE 4.6: Co-ordinate systems with reference to point A_0 (a) and point A_4 (b) and type 1 and type 2 triangular regions

K_1 represents a line 120^0 from the α-axes in anticlockwise direction, i.e. line A_1A_2 or A_3A_5. K_2 represents the line parallel to α-axes, i.e. line A_0A_3 or A_2A_4. The K_1 and K_2 will decide the position of tip of reference vector V_{ref} as:

- If tip of V_{ref} is below line A_1A_2, then consider $K_1 = 0$.

- If tip of V_{ref} is in between lines A_1A_2 and A_3A_5, then consider $K_1 = 1$.
- If tip of V_{ref} is in between lines A_0A_3 and A_2A_4, then consider $K_2 = 0$.
- If tip of V_{ref} is above line A_2A_4, then consider $K_2 = 1$.

From the values of K_1 and K_2 the triangle in which tip of V_{ref} exist can be calculated as:

- If $K_1 = 0$ and $K_2 = 0$, then the tip of V_{ref} is situated in traingle Δ_0.
- If $K_1 = 1$ and $K_2 = 0$, then the tip of V_{ref} is situated in traingle Δ_1 or Δ_2.
- If $K_1 = 0$ and $K_2 = 1$, then the tip of V_{ref} is not situated in any traingle.
- If $K_1 = 1$ and $K_2 = 1$, then the tip of V_{ref} is situated in traingle Δ_3.

If the reference vector belongs to a region of type-1, the ref v_s of coordinates $(v^s_{\alpha 0}, v^s_{\beta 0})$ is represented by vector $\vec{A_1P}$ of coordinates $(v_{\alpha i}, v_{\beta i})$. If the reference vector belongs to a region of type-2, the ref v_s of coordinates $(v^s_{\alpha 0}, v^s_{\beta 0})$ is represented by vector $\vec{A_1P}$ of coordinates $(.5 - v_{\alpha i}, Hv_{\beta i})$, where, H is the hight of equilateral triangle $(= \frac{\sqrt{(3)}}{2})$ of unit side length.

To distinguishthe sector Δ_1 and Δ_2, compare the slop of V_{ref} with $tan(60^0) = \sqrt{3}$.

If slop $V_{\beta i}/V_{\alpha i}$ for Δ_1 is $\leq \sqrt{3}$ or if $V_{\beta i} \leq \sqrt{3}V_{\alpha i}$, the V_{ref} is situated in Δ_1 otherwise in Δ_2.

In general for type-1 triangle $\Delta j = K_1^2 + 2K_2$ and for type-2 triangle $\Delta j = K_1^2 + 2K_2 + 1$

Similar to the two level inverter the on time/dwell time calculation for 3-level inverter is based on the location of reference vector V_{ref} in a particular sector.

from figure-4.7 the volt-sec balance equation is given by,

$$V^s T_s = V_a T_a + V_b T_b \tag{4.14}$$

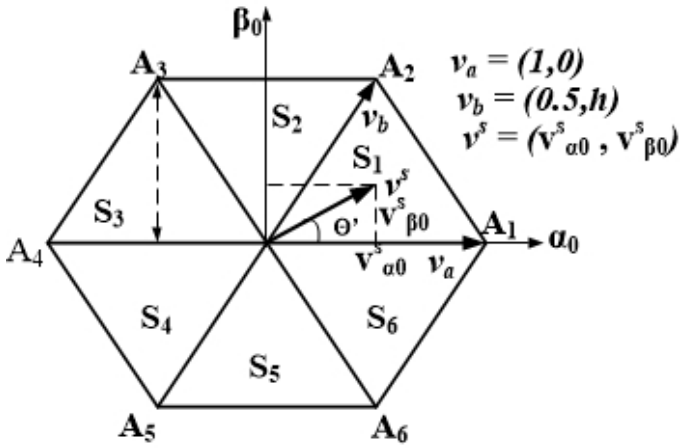

FIGURE 4.7: Space vector diagram for two-level inverter

and the time balance equation is,

$$T_s = t_a + t_b + t_0 \tag{4.15}$$

Resolving the equation 4.15 along α, β axis as shown in figure 4.7,

$$V^s_{\alpha 0} T_s = t_a + 0.5 t_b \tag{4.16}$$

$$V^s_{\beta 0} T_s = H t_b \tag{4.17}$$

from equations (4.16), (4.17) and (4.18) the ON time/ dwell times can be can be expressed as;

$$\begin{cases} t_a = T_s(V^s_{\alpha 0} - V^s_{\beta 0}/2H) \\ t_a = T_s(V^s_{\alpha 0} - V^s_{\beta 0}/2H) \\ t_0 = T_s - t_a + t_b \end{cases} \tag{4.18}$$

equation(4.19) shows that the components of a reference vector with axis separated by 60^0 are proportional to the dwell times of the adjacent vectors. The dwell times are independent of the origin of the co-ordinate system

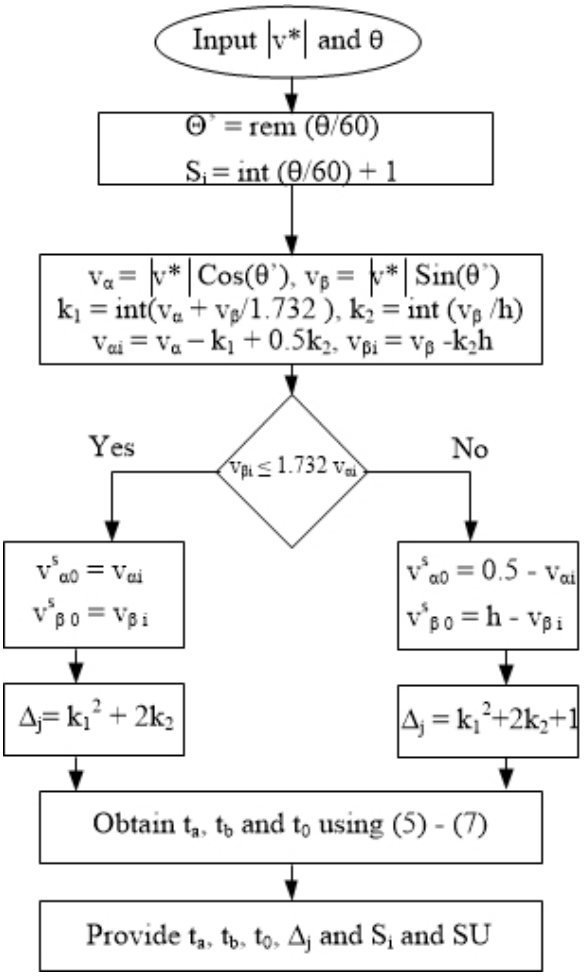

FIGURE 4.8: Flowchart of Three-level SVPWM algorithm for linear under-modulation mode

4.6 PERFORMANCE EVALUATION

Figure-4.8 shows the flow chart of generalized n-level SVPWM algorithm for under modulation mode based on the scheme explained in the previous sections. The implementation of generalized svpwm with extended operation in over modulation for MLI can be understood with the help of flow chart shown in the figure-4.9.

The proposed algorithm is validated with computer simulations for three-level cascaded MLI topology. A three-level inverter is shown in the figure-3.5 is operated in an open-loop control mode with generalized SVPWM algorithm to generate a three phase load. Operation of three-level inverter can be depicted from switching state table given in the table 4.2. The DC-link capacitor voltage distribution is assumed equal. switching sequences are mapped with reference to triangular region number.

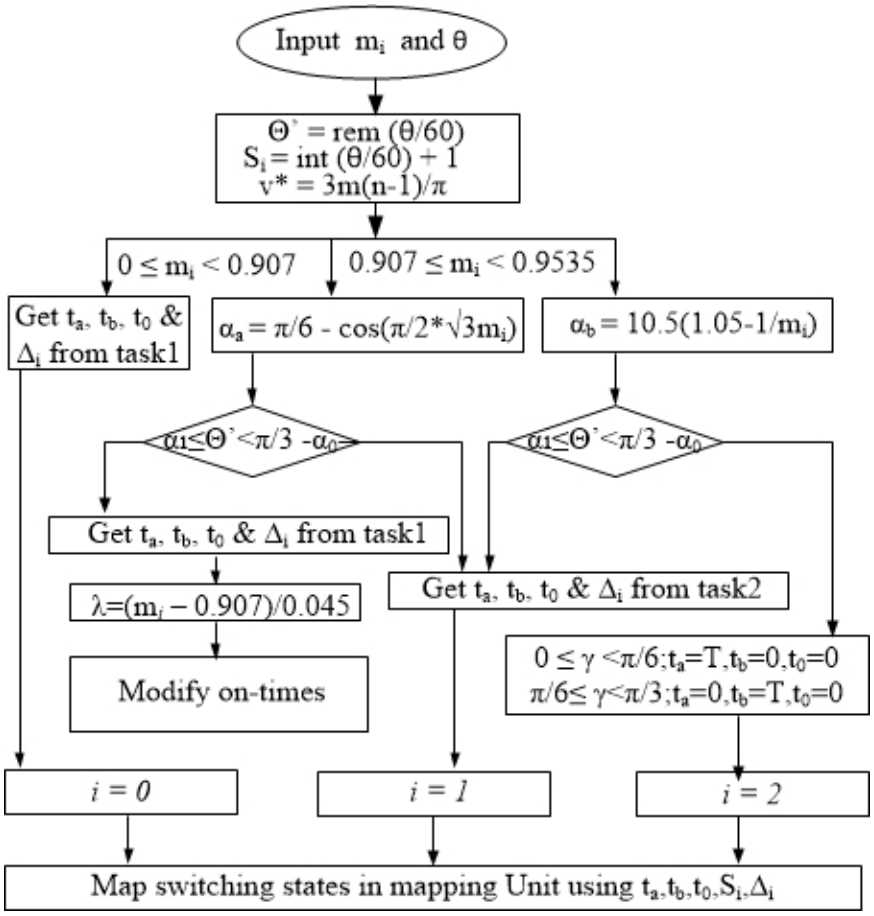

FIGURE 4.9: Flowchart of main routine: overall SVPWM process

4.7 COMMON MODE VOLTAGE

The Two level PWM inverter generates the common mode voltage in the motor windings which may cause the serious problems in motor drive operation. the common mode voltage develop a shaft voltage due to the voltage developed between rotor and frame of the motor which may cause the flow of excessive bearing current. this high bearing current damages the bearing of the motor and this large current flow into the ground through electrostatic coupling between the ground frame and stator windings. the current due to common mode voltage (CMV) also produces other several effects like:

- Produces the Common mode EMI emission.
- False tripping of ground current relays etc.

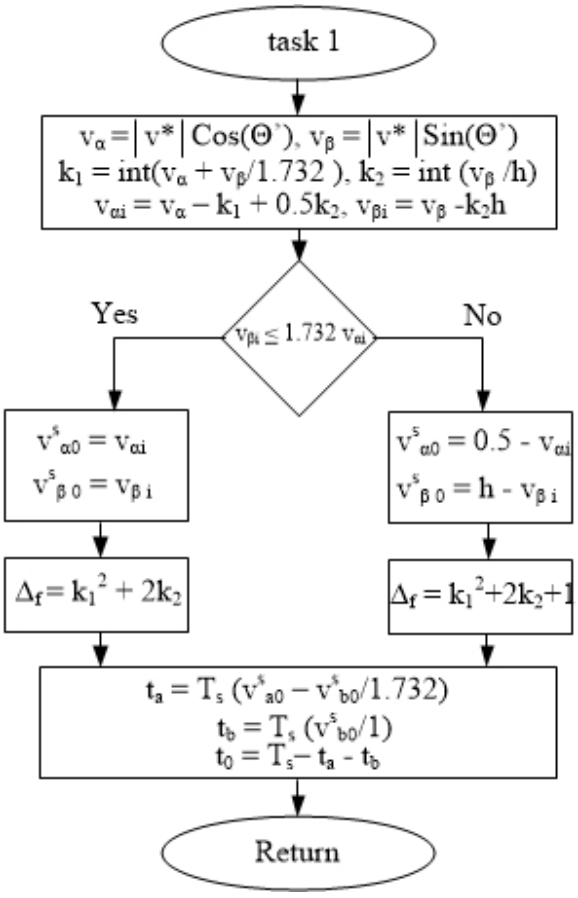

FIGURE 4.10: Flowchart of Routine-1: sub-routine to calculate the on-times and triangular number for the circular track

The CMV is the voltage difference between the stator neutral of motor and the ground of the inverter. The common mode voltage is the one third of the sum of all the three pole voltages, i.e.

$$V_{CM} = \frac{V_{ag} + V_{bg} + V_{cg}}{3} \tag{4.19}$$

Where V_{ag}, V_{bg}, V_{cg} are the voltages between pole terminal of inverter a, b and c, and g is the ground point of the inverter as shown in the figure-4.12

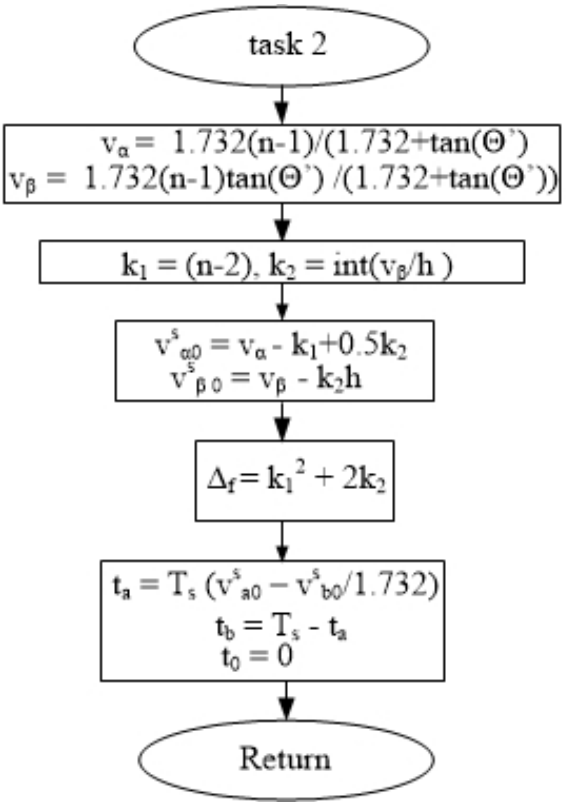

FIGURE 4.11: Flowchart of Routine-2: sub-routine to calculate the on-times and triangular number for the hexagonal track

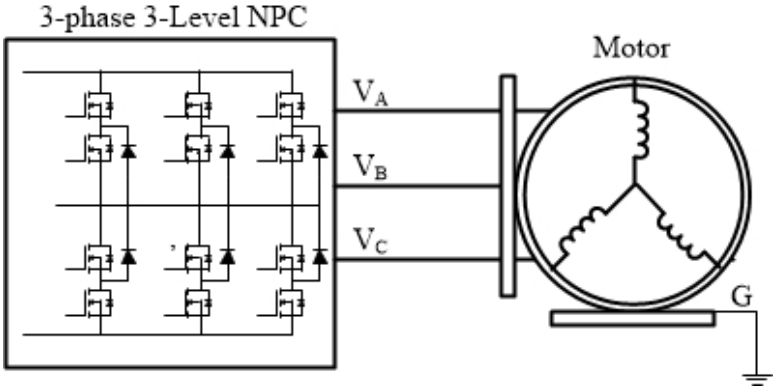

FIGURE 4.12: Three-level inverter driving IM

4.8 COMMON MODE VOLTAGE ELIMINATION METHOD

Now a day several methods are proposed to eliminate common mode voltage, most of the author worked on open end winding, but for the low rating less than 3kW generally squirrel cage motors are used. Hence there is a scope for research.

The three-level inverter has 27 switching state out of these 27 states only 7 active states gives the zero common mode voltage, these states are (P 0 N), (0 P N), (N P 0), (N 0 P), (0 N P), (P N 0) and (0 0 0) as shown in figure-4.13.

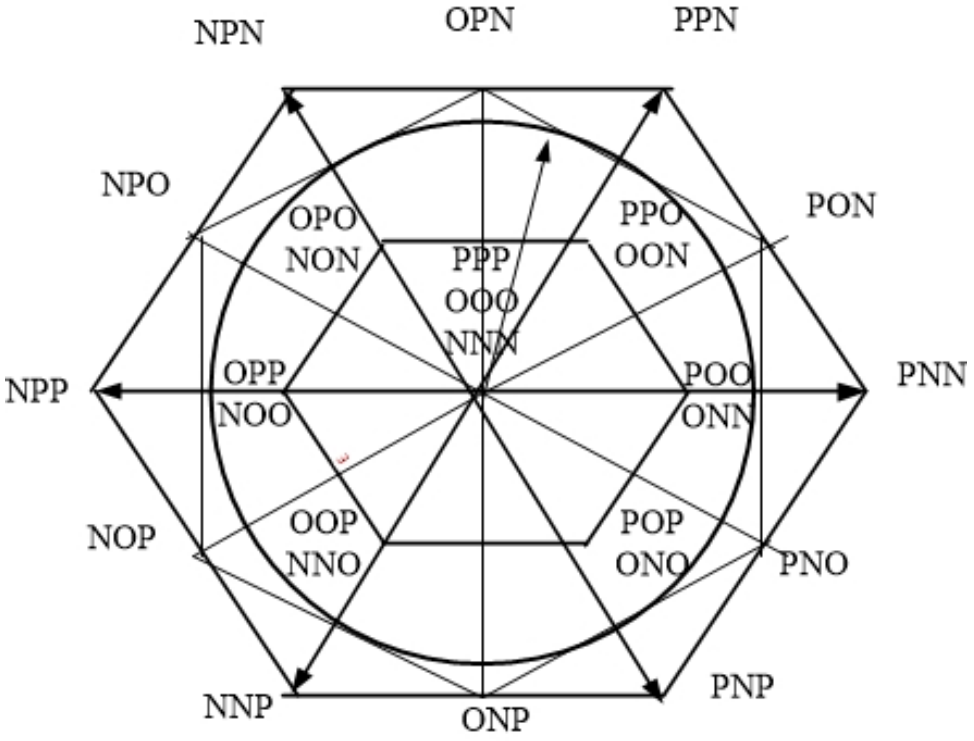

FIGURE 4.13: Space vector hexagon diagram of 3-level inverter

Therefore by limiting the switching states to these 7 active states, inverter will not generate common mode voltage. The main drawback of this basic CMV elimination method is, it also reduces the voltage utilization by 15 percent, and this will increase the voltage THD. The maximum modulation is 0.75.

4.9 PPROPOSED CMV ELIMINATION METHOD

Tabel-4.3 shows the switching state and respective CMV generated. From the table it is clear that all medium voltage vectors are not generated any common mode voltage, small and large voltage vectors will generate common mode voltages. The hexagon for 3-level inverter can be further divided into two hexagons, inner hexagon and outer hexagon.

The CMV generated in outer hexagon is varies in three levels i.e. $\frac{-E}{6}$, 0 and $\frac{E}{6}$ as shown in figure-4.13 and also given in the table-1. The CMV calculated for inner

TABLE 4.3: CMV generated by switching states of 3-level inverter

Switching State	CMV
[PPP]	$\frac{E}{2}$
[PP0] [P0P] [0PP]	$\frac{E}{3}$
$[P00]$ $[0P0]$ $[00P]$ $[PPN]$ $[PNP]$ $[NPP]$	$\frac{E}{6}$
[000] $[0PN]$ $[P0N]$ $[PN0]$ $[0NP]$ $[N0P]$ $[NP0]$	0
$[N00]$ $[0N0]$ $[00N]$ $[NNP]$ $[NPN]$ $[NNP]$	$\frac{-E}{6}$
$[NN0]$ $[N0N]$ $[0NN]$	$\frac{-E}{3}$
$[NNN]$	$\frac{-E}{2}$

hexagon is varies in 4 levels, these are: $\frac{-E}{3}$, $\frac{-E}{6}$, $\frac{E}{6}$ and $\frac{E}{3}$. From the table-4.3 it is clear that each small vector have two redundant states, one state generate CMV of magnitude $\frac{E}{6}$ and the other one generate CMV of magnitude $\frac{E}{3}$. Where, E is equal to the total DC link voltage of cascaded 3-level inverter (E=V_{dc}).

In the proposed method all the CMV of magnitude $\frac{E}{3}$ is eliminated by selecting the proper redundant switching state of small vector. This gives the CMV of three level only i.e. $\frac{-E}{6}$, 0, $\frac{E}{6}$. This reduced magnitude three-level CMV is eliminated by injecting the voltage through 4-winding transformer. The primary of the transformer is connected to the single phase H-bridge inverter having DC battery of magnitude $\frac{E}{6}$. The three secondaries of the transformer is connected in series with the motor and three level inverter to feed the voltage which is equal in magnitude and out of phase to the CMV generated at each instant.

Therefore by injecting the voltage before compensation reduces the common mode voltage to zero as given in equation below.

$$V'_{cm} = \frac{V_{ag} + V_{bg} + V_{cg}}{3} - V_{inj} = 0 \tag{4.20}$$

The switching of H-bridge inverter is also controlled by the 3-level SV modulation through V_{inj}. There is only 3 switching states associated with the each switching

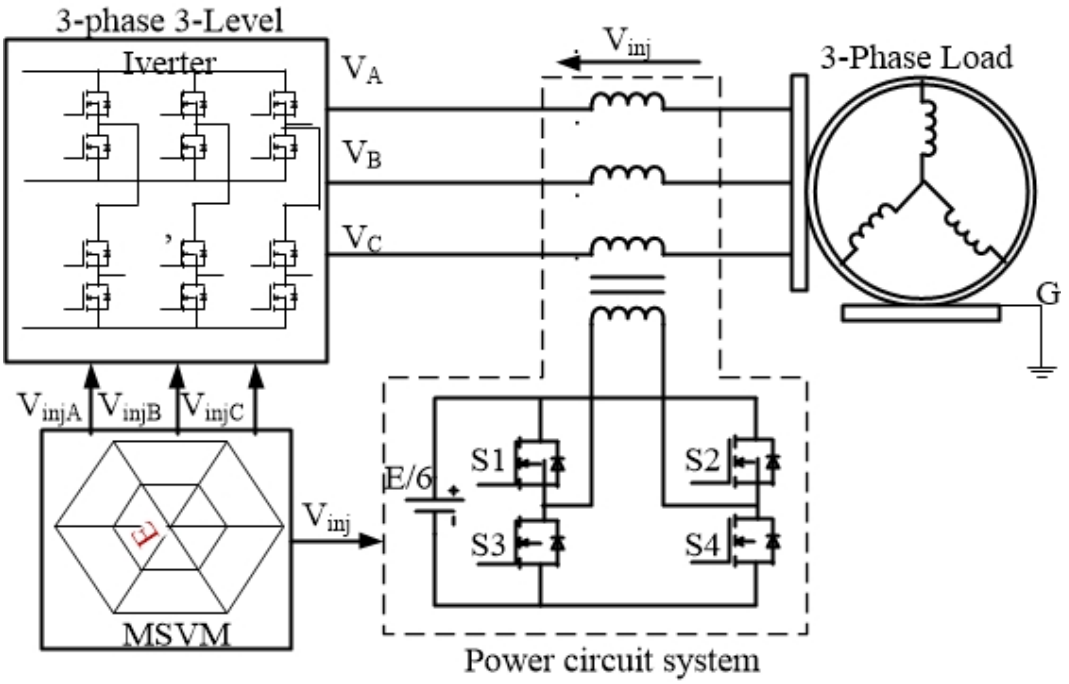

FIGURE 4.14: Block diagram of proposed method of eliminating CMV

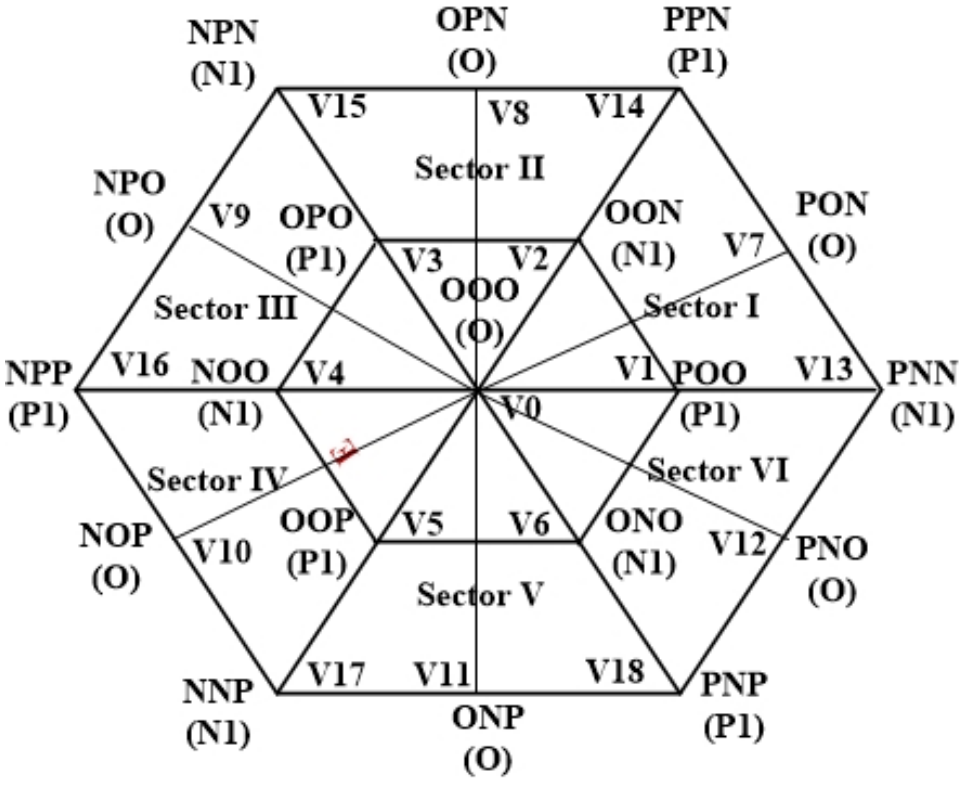

FIGURE 4.15: The modified SV diagram for proposed method

voltage, these states are P_1, o, N_1. According to the CMV generated the V_{inj} is decided as:

- If CMV calcualted is $\frac{E}{6}$, the $V_{inj} = N_1$

- If CMV calculated is 0, the $V_{inj} = 0$
- If CMV calcualted is $\frac{-E}{6}$, the $V_{inj} = P_1$

TABLE 4.4: Swtiching sequence of bridge inverter to eliminate CMV

V_{inj}	Swtiching sequence of bridge inverter			
	S1	S2	S3	S4
P_1	1	0	0	1
O	0	0	1	1
N_1	0	1	1	0

The switching sequence of the H-bridge inverter is given in the table-4.4. The modulation index for under-modulation for this control scheme is same as normal SVPWM i.e 8.66. There fore it give the 15 percent more utilization of the DC supply as compared to the conventional CMV elimination method discussed before. The voltage THD is also high than the Conventional method.

4.10 CONCLUSION

In this chapter the implementation of sinusoidal PWM, Third harmonic injection SPWM, space vector pulse width modulation technique have been discussed. The SVM enables more efficient use of DC voltage, 15 percent more than conventional PWM techniques and very low output voltage THD. The common mode voltage may rise the chance of damaging the motor drive, hence conventional and proposed method to eliminate CMV is also discussed. the proposed method is more advantageous than the conventional method with respect to the DC voltage utilization and output voltage THD.

Chapter 5

Operation and Modeling of Proposed System

In this chapter the modeling of proposed 3 phase induction motor based pv fed single stage pump load system is explained. The system is divided into four main parts i.e. Photo-voltaic array, 3-level inverter, 3-phase induction motor and pump load. The mathematical modeling of every part is done one by one.

5.1 INTRODUCTION & OPERATION OF PROPOSED SYSTEM

The given framework comprise of 3-level Cascaded inverter incorporated with PV sources and single-stage water pump as appeared in Figure-5.1.

The produced PV force is adapted by 3-level inverter with the goal that it can be used by Motor successfully. The MLI inverter setup likewise takes watch over MPPT required for ideal use of the PV source. It is worked utilizing straightforward Sine Triangle Pulse Width Modulation (SPWM) or SVPWM method in which both input from PV sources are used adequately for estimations of modulation index (ma). The switches in the every leg of the inverter are switched

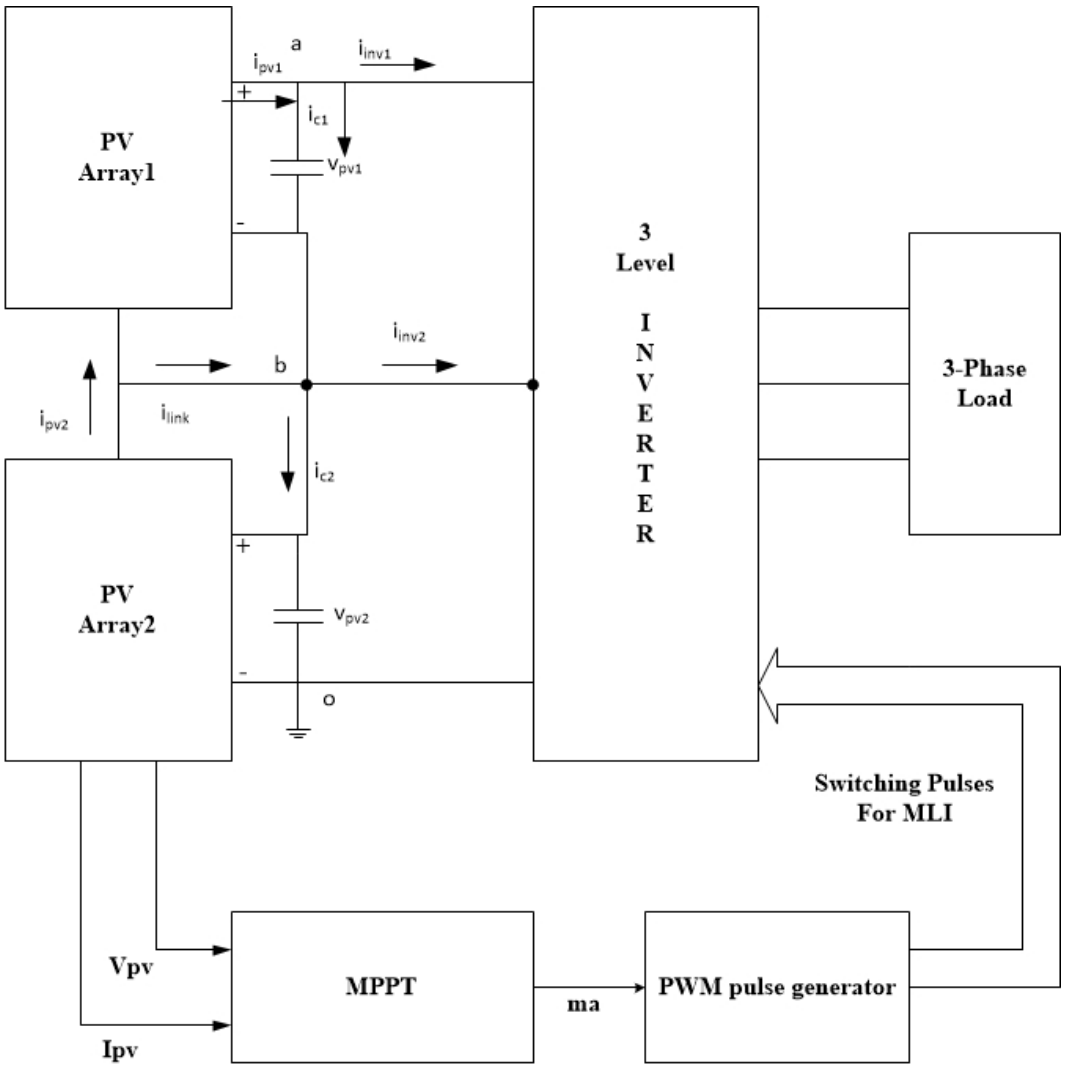

FIGURE 5.1: Square outline of single stage PV controlled centrifugal pump

on and off by utilizing corresponding switching method. The V/f control scheme is applied to run the motor at maximum power. The modulation index generated by the MPPT with reference to the solar irradiation to track the maximum power through out the operation is used as the reference for V/f control block. V/f controller ensure the operation of the induction motor at constant power region. For pump and fan type of load torque and speed changes simultaneous at field weakening mode to draw the maximum power from the source. To check the framework operation complete numerical model for the proposed framework was created. The created model comprise of squares of two PV sources, 3-level MLI inverter and induction-motor pump set as appeared in Figure-5.1. The prosed system is designed and tested for simple sinusoidal PWM and Space Vector PWM with or without common mode voltage elimination. The MI (ma) is generated by

the MPPT for both the modulation strategies, and the V/f control block ensure the optimum utilization of power form PV array for the operation of induction motor with pump load under varying atmospheric conditions. The flow chart of the proposed system is shown in figure-5.2.

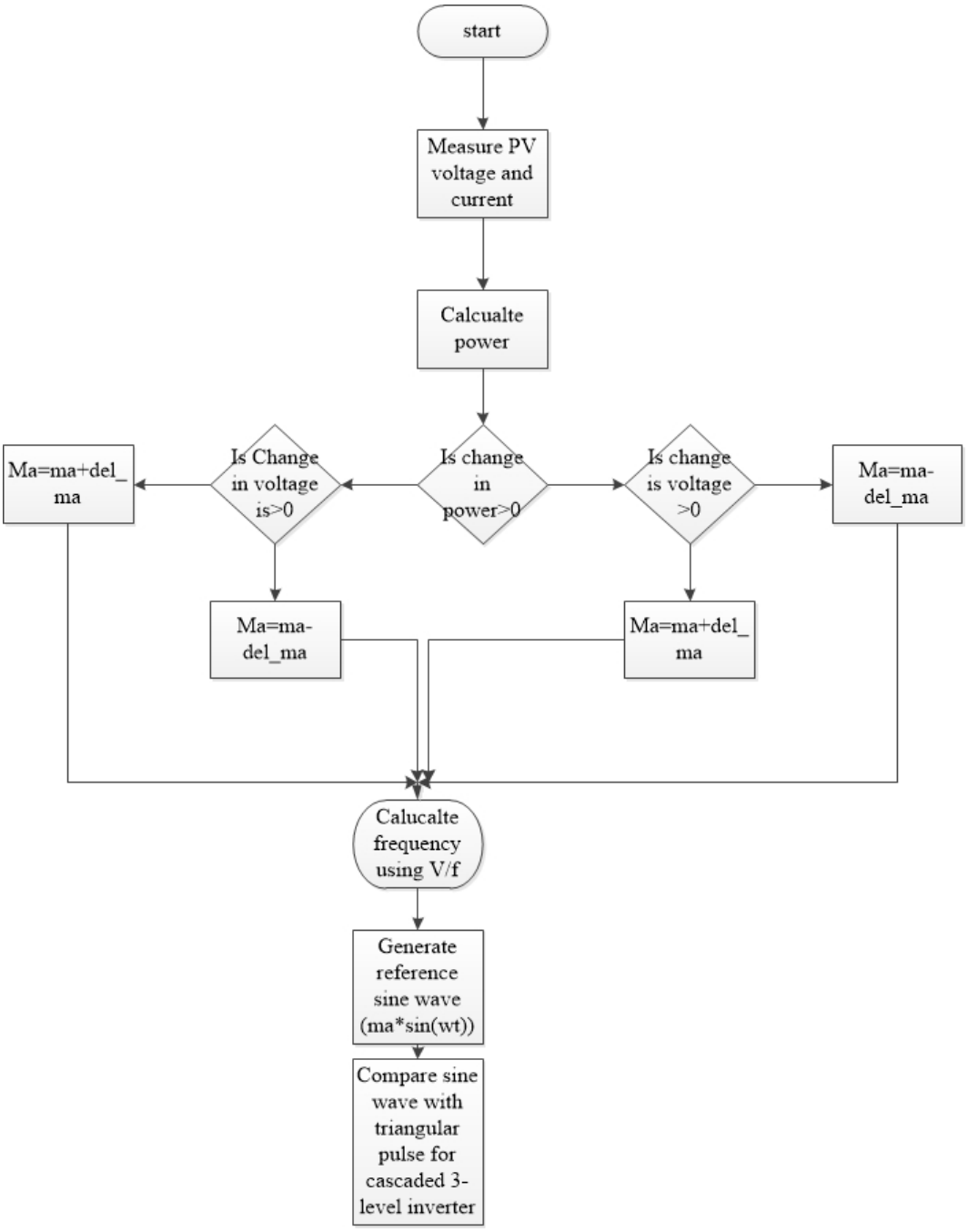

FIGURE 5.2: flow Chart of Proposed Control Algorithm

5.2 PV SOURCE MODEL

To show PV source, the given i-v characteristic condition can be adjusted as for required arrangement parallel association of the PV cells. The yield of PV arrays 1 and 2 is associated with inverter-1 and inverter-2 with PV-link capacitors C1 and C2 individually. By applying KCL at points "A" and "B" of inverter shown in figure-5.2 we have,

$$i_{pv1} = C_1 \frac{dv_{pv1}}{dt} + i_{inv1} \tag{5.1}$$

$$i_{pv2} = C_2 \frac{dv_{pv2}}{dt} + i_{inv2} - i_{c1} + i_{pv1} \tag{5.2}$$

Where, v_{pv1} is the voltage of top PV array in volts, v_{pv2} is the voltage of lower PV array in volts, i_{pv1} is the current given by top PV array in ampere, $ipv2$ is the current given by lower PV array in ampere, i_{inv1} is the current flowing through upper inverter in ampere, i_{inv2} is the current flowing through the lower inverter in ampere.

5.3 THREE-LEVEL CASCADED-INVERTER MODEL

The computed PV source yield voltages are utilized for the reproduction of cascaded inverter. Mathematical model for the MLI is created by figuring the pole-voltage at the every leg of inverter. pole-voltage in every leg of inverter can be computed with reference to nodal point 'O', as appeared in Fig. 5.1. The figured pole voltage is then utilized for computation of pole-voltage. the pole-voltage of inverter-1 with reference to hub "O" in the leg associated with phase "a" is represented by v_{a1o}. Additionally, pole-voltage for leg for phases "b" and "c" are signified as v_{b1o}, v_{c1o}. There are two values for pole voltage v_{a1o} is existed, one is $v_{pv1} + v_{pv2}$ and other is v_{pv2}, depending whether s_{11} or s_{12} is turned ON.

$$v_{a10} = (v_{pv1} + v_{pv2})S_{11} + (v_{pv2})S_{12} \tag{5.3}$$

Where, S_{11} is equal to 1 when On and equal to zero when OFF. Similarly for other phases the pole voltages are:

$$v_{b10} = (v_{pv1} + v_{pv2})S_{21} + (v_{pv2})S_{22} \tag{5.4}$$

$$v_{c10} = (v_{pv1} + v_{pv2})S_{31} + (v_{pv2})S_{32} \tag{5.5}$$

Utilizing the same system the pole-voltage for lower inverter can be resolved and given as,

$$v_{a20} = (v_{pv1} + v_{pv2})S_{11}S_{13} + (v_{pv2})S_{12}S_{13} \tag{5.6}$$

The pole voltage equation for lower inverter has three values $(v_{pv1} + v_{pv2})$, v_{pv2} and zero. When upper switch of lower inverter (S_{13}) is off the pole voltage is zero, and when on the same pole voltage of upper inverter is existed at lower inverter. The pole-voltage of lower inverter can also be written in-terms of upper inverter pole voltage as,

$$v_{a20} = v_{a10}S_{13} \tag{5.7}$$

Similarly for other phases of lower inverter, the pole voltage can be calculated. The poles of lower inverter is connected to the stator of 3-phase induction motor, hence pole voltage of lower inverter is used to calculate the phase voltages of induction motor stator windings and given as,

$$v_{an} = v_{a20}v_{no} \tag{5.8}$$

where, v_{no} is the common mode across voltage of the inverter and given as,

$$v_{no} = \frac{1}{3}(v_{a20} + v_{b2o} + v_{c20}) \tag{5.9}$$

From the phase voltage, the current flowing through the inverter is calculated as,

$$i_{inv1} = S_{11}S_{13}i_a + S_{21}S_{23}i_b + S_{31}S_{33}i_c \tag{5.10}$$

$$i_{inv2} = S_{12}S_{13}i_a + S_{22}S_{23}i_b + S_{32}S_{33}i_c \tag{5.11}$$

when considering the average current flowing thorugh capacitors C1 and C2 zero, The current flowing through the PV arrays are reduced to,

$$i_{pv1} = i_{inv1} \tag{5.12}$$

$$i_{pv2} = i_{inv2} + i_{inv1} \tag{5.13}$$

5.4 PUMP LOAD

The affinity laws for the centrifugal pump load connected to 3-phase induction motor is,

$$Q \propto \omega_r, H \propto \omega_r^2, P_{electrical} \propto \omega_r^3 \tag{5.14}$$

Where, Q is the flow rate (m^3/s), and H is the head (m).

$$T = K\omega_r^2 \tag{5.15}$$

Where K is the centrifugal pump constant.

5.5 INDUCTION MOTOR MODELING

The induction machine model is established using a rotating (d,q) field reference(without saturation) concept. In poly-phase induction machines, both the stator and rotor windings carry alternating currents. The flux produced by stator, rotates at synchronous speed with respect to stator. The current induced in the rotor also produce a field that rotates at synchronous speed with respect to stator. Thus under steady state conditions, the relative speed between stator and rotor fields is zero. The rotor energy receives energy from stator by electromagnetic induction. The transformation from balanced 3-phase currents ia, ib, ic to balanced 2-phase currents i_α, i_β was obtained. The quality of the m.m.f produced by 2-phase currents was identical with that produced by 3-phase currents. The general voltage equations for 3-phase SCIM is,

$$\begin{bmatrix} v_{ds} \\ v_{qs} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} r_s + L_s p & 0 & -Mp & 0 \\ 0 & r_s + L_s p & 0 & -Mp \\ Mp & -M\omega_r & -(r_r + L_r p & L_r\omega_r) \\ M\omega_r & Mp & -L_r\omega_r & -(r_r + L_r p) \end{bmatrix} * \begin{bmatrix} i_{ds} \\ i_{qs} \\ i_{dr} \\ i_{qr} \end{bmatrix} \tag{5.16}$$

for 3-phase supply, the resultant flux present at air-gap rotates at synchronous speed with respect to the stator. Therefor p is replaced by jω wehn representing the steady state voltage equation in phasor form.

Also $\omega_r = v\omega$

Where, $v = \frac{Actualrotorspeed}{Synchronousspeed} = (1 - s)$

Here, s is the slip. So in phasor form, the matrix equation(5.16) becomes:

$$\begin{bmatrix} v_{ds} \\ v_{qs} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} r_s + j\omega L_s & 0 & -j\omega M & 0 \\ 0 & r_s + j\omega L_s & 0 & -j\omega M \\ j\omega M & -Mv\omega & -(r_r + j\omega L_r & L_r v\omega) \\ Mv\omega & j\omega M & -L_r v\omega & -(r_r + j\omega L_r) \end{bmatrix} * \begin{bmatrix} \bar{i}_{ds} \\ \bar{i}_{qs} \\ \bar{i}_{dr} \\ \bar{i}_{qr} \end{bmatrix} \tag{5.17}$$

There is no difference in the d and q-phases except one of time. For obtaining a clockwise rotating field, the current in coil D_S must lag that in coil Q_S, as shown in figure 5.3 (a). At the instant marked $t = 0, i_{ds} = 0$ and $i_{qs} = I_m$. Thus the m.m.f is set up along q-axis [Figure-5.3(b)]. At the instant marked $t = t_2$, $i_{ds} = i_{qs} = \frac{I_m}{sqrt(2)}$ and the m.m.f is set up along an axis, which has traversed an angular distance of 45 clock-wise from the q-axis [figure-5.3(b)].

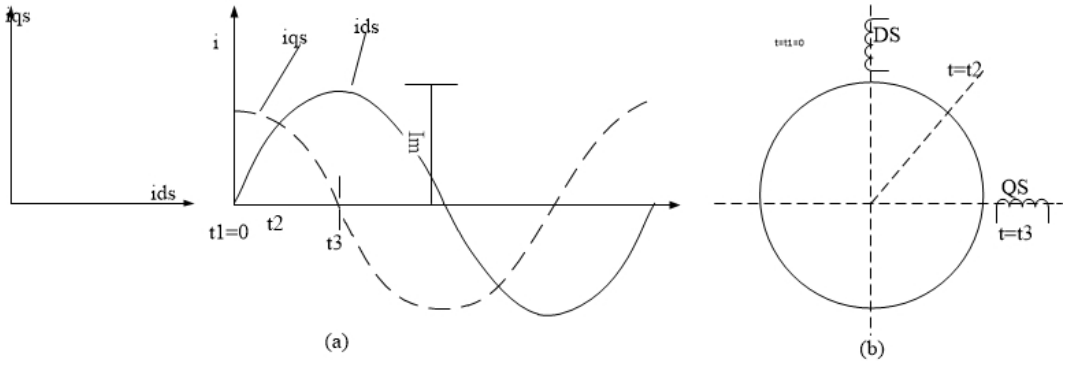

FIGURE 5.3: (a) Distribution of currents in the two stator coils. (b) The orientation of stator mmf at the instant considered.

At the instant marked $t = t_3$; $i_{ds} = I_m$ and $i_{qs} = 0$ and the m.m.f is established along the d-axis, as shown in figure-5.3(b). Thus for obtaining a clockwise rotating field, the following relations can be written by referring to figure-5.3(a). In magnitude I_{qs} and I_{ds} are equal, but I_{qs} leads Ids by 90. So $I_{qs} = jI_{ds}$ The voltage and current equations for Equivalent circuit for d, and q frames are (From figure-5.4(a) and (b)), as:

$$V_{sd} = R_s i_{sd} + \frac{d}{dt}\lambda_{sd} - \omega_d \lambda_{sq} \tag{5.18}$$

$$V_{sq} = R_s i_{sq} + \frac{d}{dt}\lambda_{sq} - \omega_d \lambda_{sd} \tag{5.19}$$

$$V_{rd} = R_r i_{rd} + \frac{d}{dt}\lambda_{rd} - \omega_{dA} \lambda_{rq} \tag{5.20}$$

$$V_{rq} = R_r i_{rq} + \frac{d}{dt}\lambda_{rq} - \omega_{dA} \lambda_{rd} \tag{5.21}$$

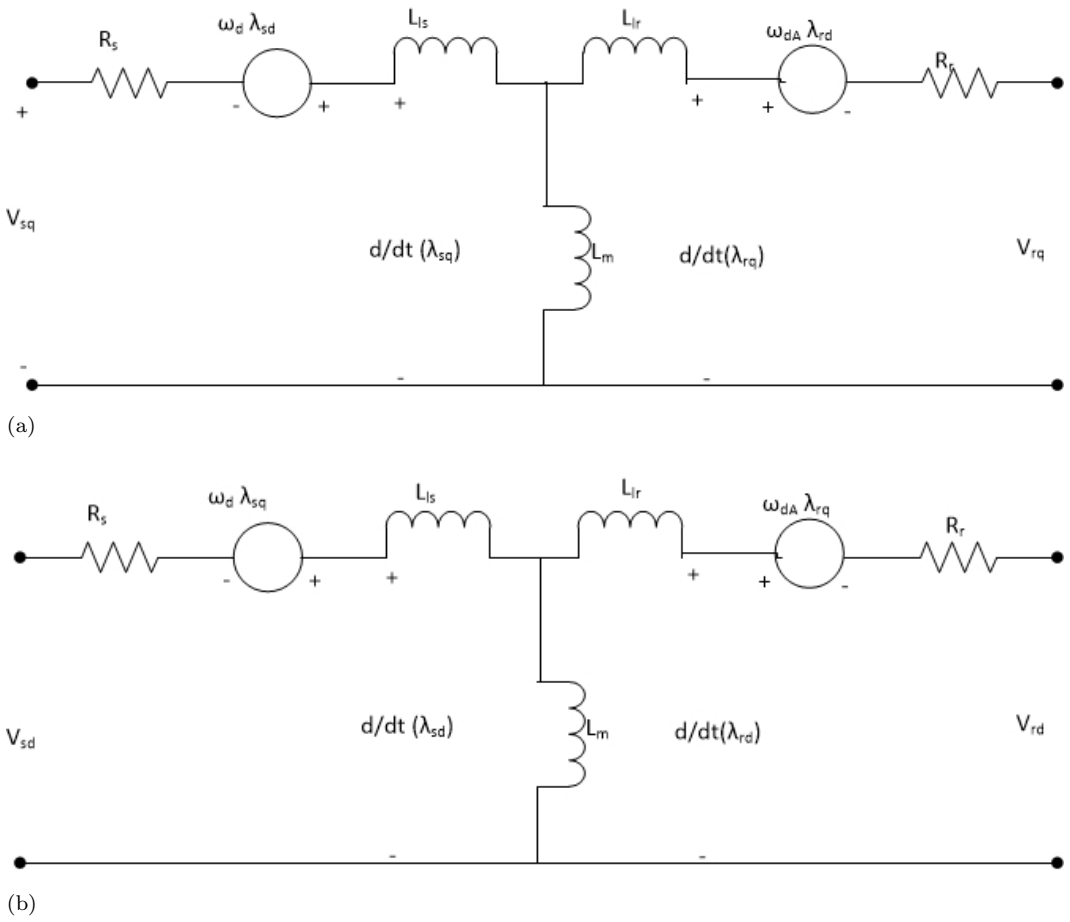

FIGURE 5.4: (a) and (b) Equivalent circuit of induction machine in d-q frame

Where v_{sd} and v_{rd} represents the direct axes stator and rotor voltages and v_{sq} and v_{rq} represents the quadrature axes stator and rotor voltages respectively. For the cage rotor induction motor the d-q quantities of rotor voltages are zero. Therefore the flux linkage is related to the current by:

$$\begin{bmatrix} \lambda_{sd} \\ \lambda_{sq} \\ \lambda_{rd} \\ \lambda_{rq} \end{bmatrix} ; = M \begin{bmatrix} i_{sd} \\ i_{sq} \\ i_{rd} \\ i_{rq} \end{bmatrix} ; M = \begin{bmatrix} L_s & 0 & L_m & 0 \\ 0 & L_s & 0 & L_m \\ L_m & 0 & L_r & 0 \\ 0 & L_m & 0 & L_r \end{bmatrix} \tag{5.22}$$

Combining equation (5.18) to equation (5.22), the state space model of induction machine is represented as;

$$\begin{bmatrix} i_{sd} \\ i_{sq} \\ i_{rd} \\ i_{rq} \end{bmatrix} ;= \frac{1}{L_m^2 - L_r L_s} \times \left(A \begin{bmatrix} i_{sd} \\ i_{sq} \\ i_{rd} \\ i_{rq} \end{bmatrix} + \begin{bmatrix} L_s & 0 & L_m & 0 \\ 0 & L_s & 0 & L_m \\ L_m & 0 & L_r & 0 \\ 0 & L_m & 0 & L_r \end{bmatrix} \begin{bmatrix} v_{sd} \\ v_{sq} \\ v_{rd} \\ v_{rq} \end{bmatrix} \right) \tag{5.23}$$

Where, A=

$$\begin{bmatrix} L_r R_s & (\omega_{dA} L_m^2 - \omega_s L_r L_s) & -L_m R_r & -L_r L_m(\omega_s - \omega_{dA}) \\ -(\omega_{dA} L_m^2 - \omega_s L_r L_s) & L_r R_s & L_r L_m(\omega_s - \omega_{dA}) & L_m R_r \\ -L_m R_s & L_s L_m(\omega_s - \omega_{dA}) & L_s R_r & (\omega_s L_m^2 - \omega_{dA} L_r L_s) \\ -L_s L_m(\omega_s - \omega_{dA}) & -L_m R_s & -(\omega_s L_m^2 - \omega_{dA} L_r L_s) & L_s R_r \end{bmatrix}$$

The electromechanical torque produced in in 3-phase cage rotor induction motor in terms of d-q quantities of rotor, is given by;

$$T_{em} = \frac{P}{2}(\lambda_{rq} i_{rd} - \lambda_{rd} i_{rq}) \tag{5.24}$$

In therms of inductance the electromagnetic torque is expressed as;

$$T_{em} = \frac{P}{2} L_m (i_{sq} i_{rd} - i_{sd} i_{rq}) \tag{5.25}$$

From the fundamental torque equation the mechanical part of the machine is modeled as:

$$\frac{d}{dt}\omega_{mech} = \frac{T_{em} - T_L}{J_{eq}} = \frac{\frac{P}{2} L_m (i_{sq} i_{rd} - i_{sd} i_{rq}) - T_L}{J_{eq}} \tag{5.26}$$

Where J_{eq} = Equivalent moment of inertia of the machine.

$\omega_{dA} = \omega_{slip} = \omega_s - \omega m$,

$\omega_m = \frac{P}{2}\omega_{mech}$,

$\omega_d = \omega_s$ and

$L_s = L_{sl} + L_m$, $L_r = L_{rl} + L_m$.

5.6 V/f CONTROL

Simple open-loop V/f control of VSI fed induction motor drives is shown in the figure-5.4. No need of feedback signal in the drive avoid signal processing complexity and stability problems at a cost of inferior performance. The air gap flux (V/f) is maintained constant by inputting frequency, f_1^* command signal and proportional voltage designed to have a base frequency of Hz and MI=1 at this frequency. At low frequency boost voltage is added to compensate IR drop. The reference speed signal is accelerated and decelerated at constant ramp command to change speed at gradual rate and avoid mechanical shocks. The acceleration and deceleration ramp command can be set by the MPPT by changing the MI with the irradiation. While decelerating the drive, the electric breaking power s dissipated in brake resistor (BR). As the frequency command signal exceeds the base frequency, the drive enters into the field-weakening region and supply voltage saturates along-with decrease in developed torque. Thereafter, the command sinusoidal phase voltage are calculated from the voltage magnitude and the angle command signal for the PWM switching logic module. The switching patterns are selected and the switching signals are generated according to SVPWM algorithm for the MOSFET of the three-level cascaded VSI bridge. It is assumed that the motor is responding to set frequency command in open-loop control. The current feedback from the current clamps is used for measurement and protection; it is not used as a part of the control strategy.

Simple, inexpensive and most widely used open-loop V/f controlled drive does not require feedback sensors, gives two-quadrant operation, operates in constant-torque and field-weakening mode of speed control, experiences drift in speed with load torque variation and supply voltage variation, offers sluggish system response and gives easy control in multi-motor operation [25]. This method is adequate for drive control in steady-state conditions in applications like pumps, fans and conveyors where high dynamic performance is not required.

Implementaion of V/f control of PV fed Cascaded inverter for IMD, inverter circuit parameter, DC-link capacitor is choosen according ot design procedure given below:

The main function of the DC-link capacitive filter is to minimize the ripple content in the front-end rectifier output voltage. The DC-link capacitor design criteria would include the dc link voltage ripple plus some safety factor necessary to maintain the capacitors within their safe operating range. The required capacitance of the dc link and the voltage ripple are inversely related to each other. An increase in the capacitance will decrease the amount of ripple in the dc voltage. Too high DC-link capacitance results in high transient voltage overshoot.

The selection capacitance of the DC-link capacitor is based upon the design criteria given in the literature [197]. The DC-link voltage ripple has been estimated for different values of DC-bus capacitances through the simulation of the developed model.

5.7 CONCLUSION

The detail operation and mathematical modeling of the proposed single stage PV based water pumping system is enumerated in the chapter. Equations shows the steady state as well as transient behavior of the proposed system. The modeling is done in four parts, first mathematical model of the photo-voltaic array is done on the basis of equations discussed in chapter-2, then the modeling of 3-phase, 3-level novel cascaded inverter is done and at the last mathematical model of pump load and 3-phase induction motor is discussed. The simple V/f control method is used to ensure the operation of induction motor with maximum power coming out form the PV array.

Chapter 6

Performance Evaluation using MATLAB/Simulink

This chapter is discussed in three part, in the first part result and analysis of cascaded pv fed single stage 3-level inverter with SVPWM technique is applied to supply the RL load. In the second part the common mode voltage generated due to higher switching speed of SVPWM is removed using conventional CME method for the same system, and in the last part the advanced method is applied to reduce CMV using series injection of the voltage.

6.1 PHOTOVOLTAIC MODULE

The V-I and P-V curves shows that the maximum power of the pv array is 180W. CEL 180W solar modules is taken for analysis of the system. The maximum power developed by the array is 180. at current of 5 A and at a voltage of 36 V. In the simulation irradiation change at Ts=0.5s from 1000W/m2 to 400W/m2. And temperature remains same in all the irradiation conditions.

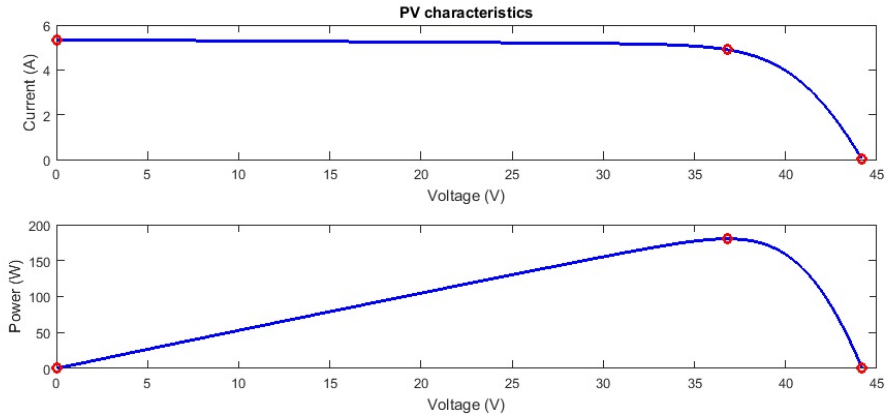

FIGURE 6.1: V-I and PV curves

6.2 SVPWM TECHNIQUE

The cascaded solar pv module of 3*180=640W are connected in series such two array are used to supply the RL load. The P&O MPPT technique is used to ensure the operation of PV module at MPP throughout the operation. The space vector PWM technique is used to convert solar DC-power in to AC-power. The figure 6.2 shows the variation of photovoltaic voltage, current and power given by PV array. At the instant 0.5 sec the irradiation changes from 1000 W/m^2 to 400 W/m^2. Due to the change in irradiation change in voltage is from 112V to 110V, change in current is from 4.8 A to 1.8 A to ensure MPP, therefore the power obtained from PV is also changes from 520W to 205W. The variation of modulation index to achieve the operation at MPP by P&O MPPT technique is shown in figure 6.3. figure 6.3 shows that at solar irradiation of 1000W/m^2 the generated modulation index is 0.6 pu and at 400 W/m^2 the generated modulation index is fluctuated between 0.3 to 0.4 pu. The generated line and phase voltage of the space vector modulated cascaded 3-level inverter are shown in figure 6.4 and figure 6.5 respectively. Figure 6.4 shows that for the modulation index of 0.6 inverter generates three level output voltages 0V,+ 108V and +231V, while at modulation index 0.4pu the inverter behaves like a two level inverter. The maximum value of output voltage at low modulation index is 0V and +108V. The variation of phase voltage with the similar change in modulation index is shown in figure 6.5. The three phase line current is shown in figure 6.6. Due to change in modulation index the current supplied for a fixed RL load is also changes. Figure

6.7 and figure 6.8 shows the FFT analysis of line voltage Vab. The total harmonic distortion is varies from 41.21 % for higher modulation index and 48% at lower modulation index. The common mode voltage is shown in figure 6.9, for higher modulation index the maximum value of common mode voltage is 72V and for lower modulation index common mode voltage is 120V.

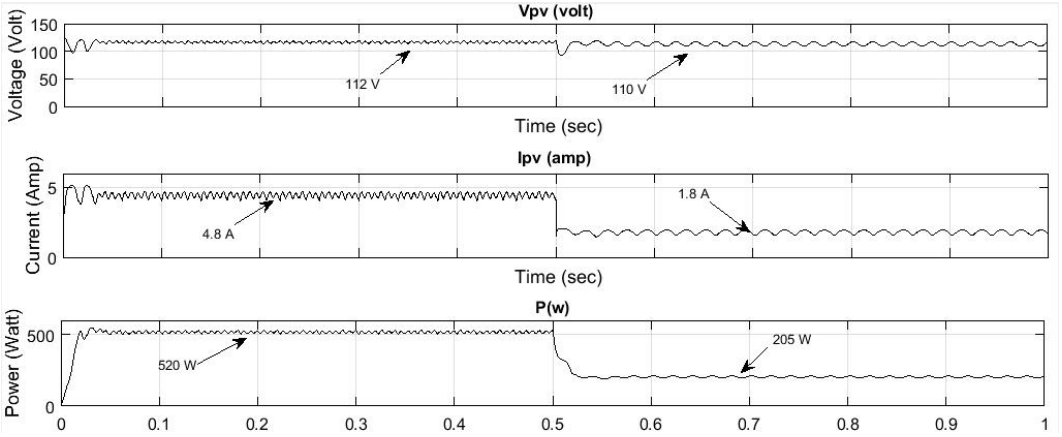

FIGURE 6.2: Voltage, current and power characteristic of PV module.

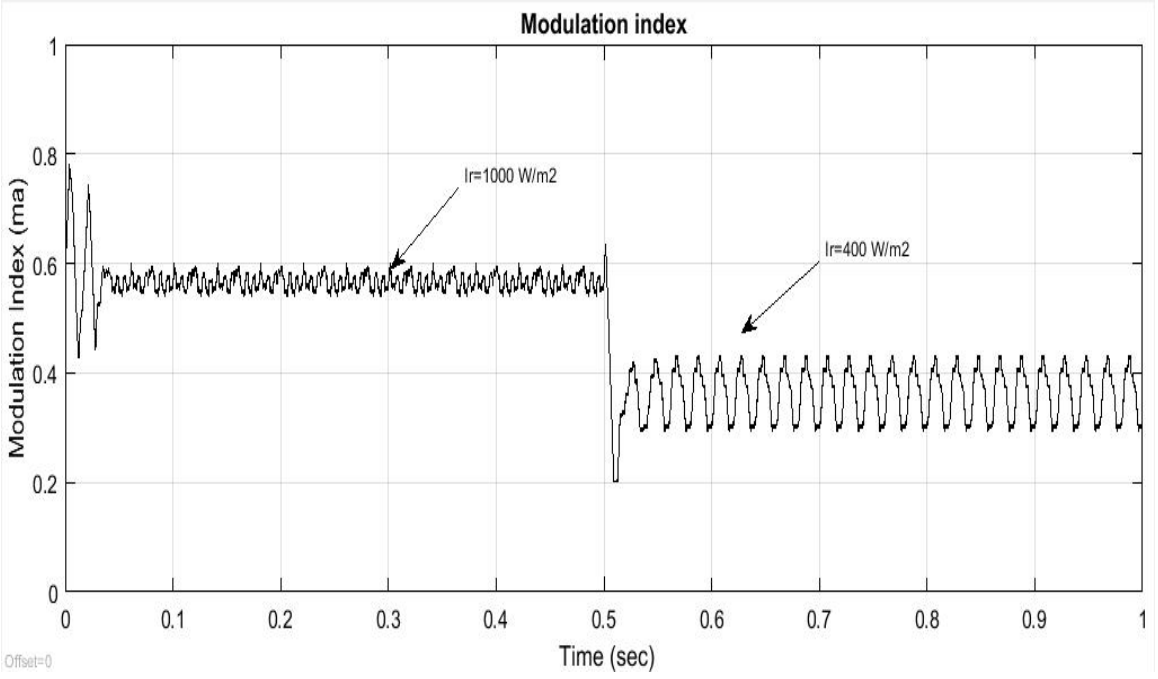

FIGURE 6.3: Modulation index

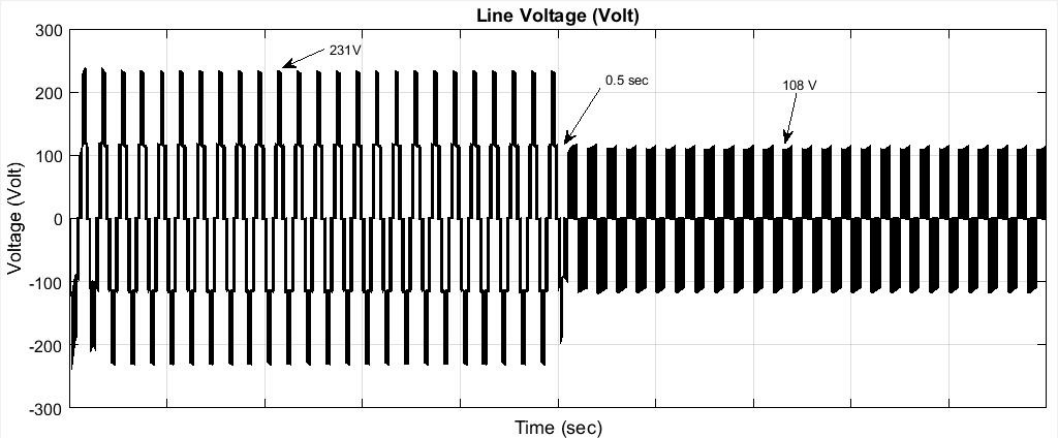

FIGURE 6.4: Inverter output line voltage Vab

Voltage.jpg Voltage.jpg

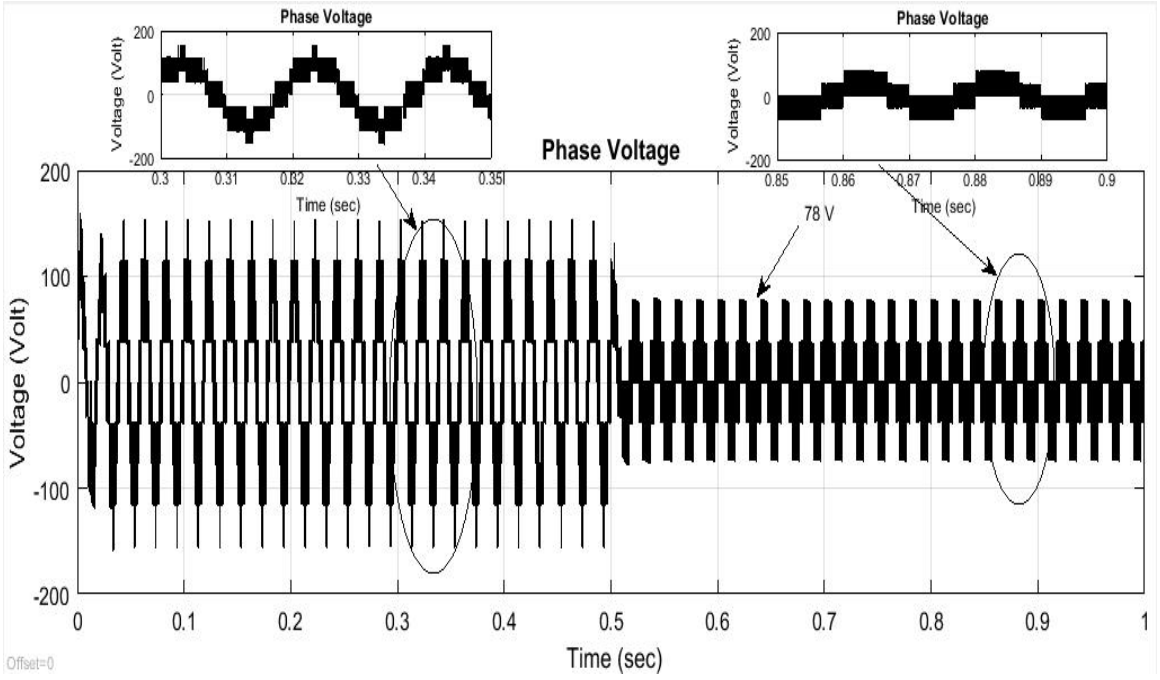

FIGURE 6.5: Inverter output phase voltage Van.

6.3 CONVENTIONAL COMMON MODE VOLTAGE ELIMINATION METHOD

For the same setup the conventional common mode voltage elimination method is used to generate switching pulses for three level cascaded inverter. For the same environmental condition discussed above in SVPWM method the solar PV dc voltage current and power is shown in figure 6.10. The DC link voltage is 115V for different irradiation conditions, While, the current is changes from maximum value

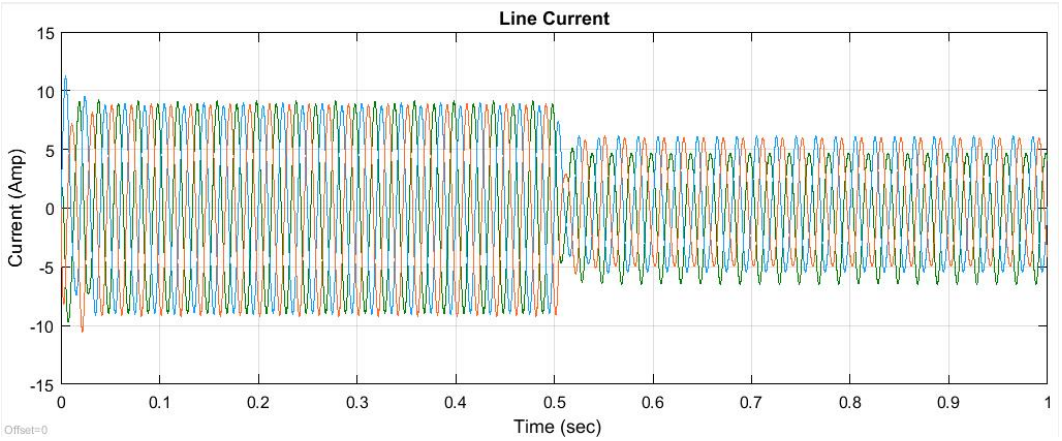

FIGURE 6.6: Three phase Line Current.

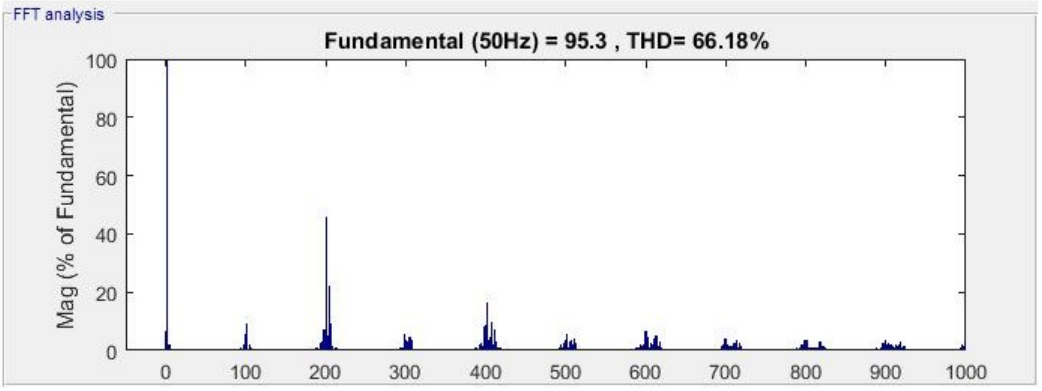

FIGURE 6.7: FFT analysis for 0.6 modulation index

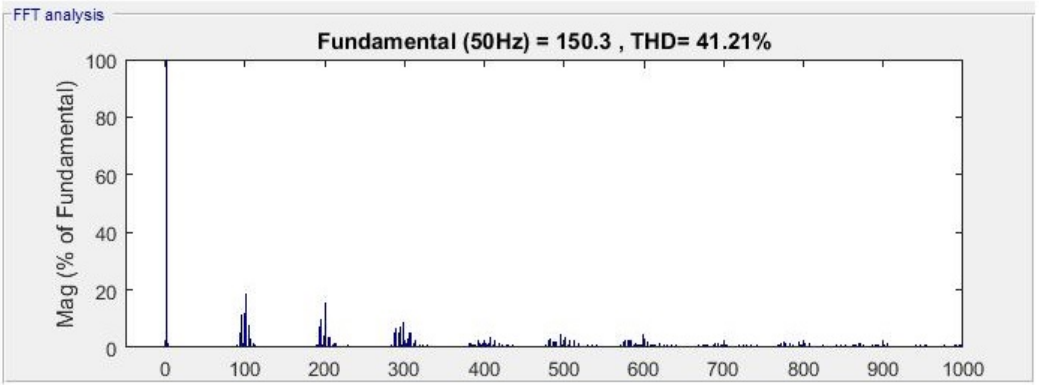

FIGURE 6.8: FFT analysis for 0.4 modulation index

5A to 1.9A, due to this the power developed by the solar array is changes from 550W to 210W. from the figure 6.1 and figure 6.10 it is clear that conventional CMV elimination method maintain the DC link voltage constant irrespective to the SVPWM method. The Variation in modulation index generated by perturbation and observation MPPT method is changes from 0.6 to 0.37pu due to the change in solar irradiation, as shown in figure 6.11. The line voltage generated

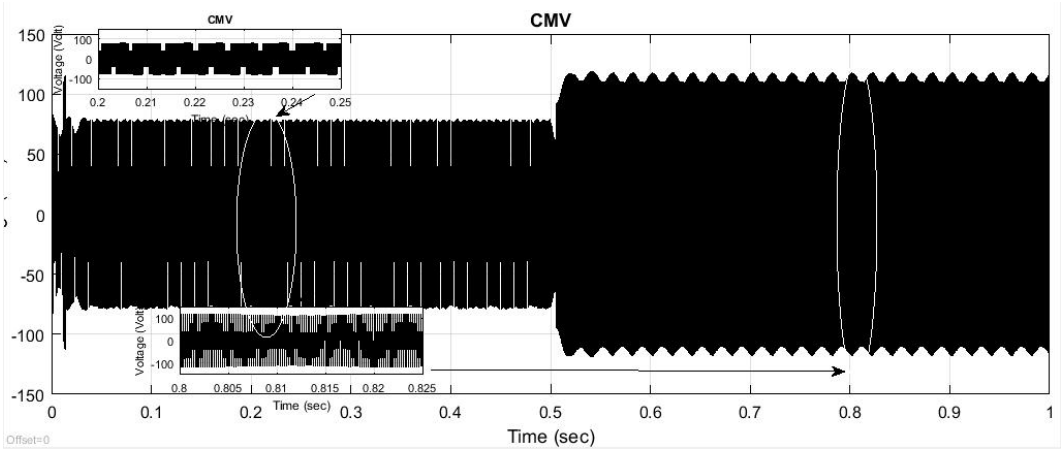

FIGURE 6.9: Common Mode Voltage

by this modulation technique is shown in figure 6.12. The maximum value of the line voltage generated at both irradiation conditions are same and the shape of waveform is also same unlike SVPWM method. The phase voltage is shown in figure 6.13. The three phase line current is shown in figure 6.14. From the figure it is clear that for both modulation index the three phase current is balanced unlike SVPWM. The FFT analysis of line voltage Vab are shown in figure 6.15 and figure 6.16 for higher and lower modulation index respectively. For higher and lower modulation index the THD is 74.43%. The common mode voltage is reduced to near zero value as shown in figure 6.17, the fluctuation of 5V in CMV is due to the fluctuation in the pv output voltage.

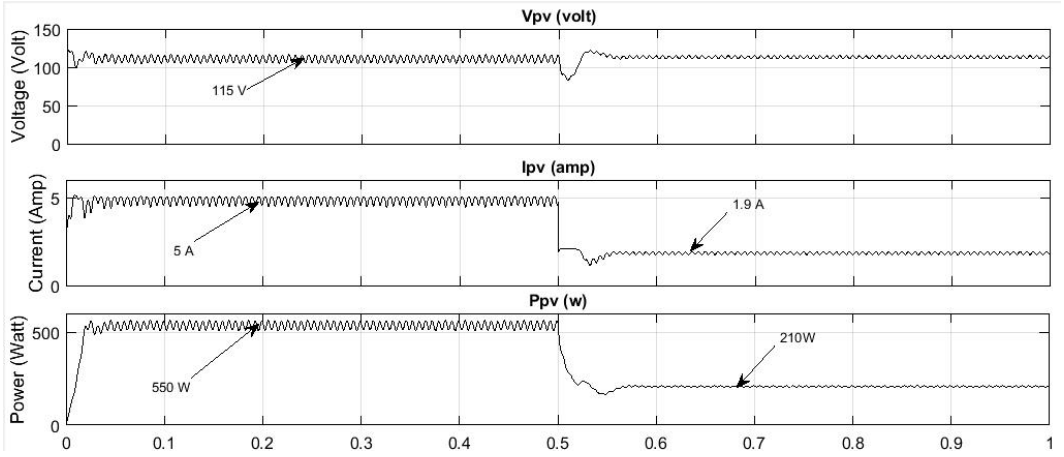

FIGURE 6.10: Voltage, current and power characteristic of PV module.

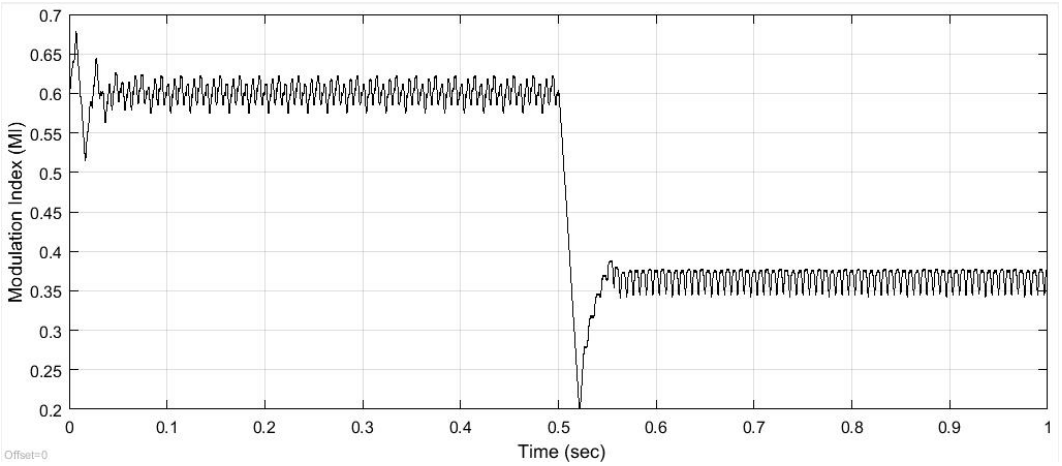

FIGURE 6.11: Modulation index

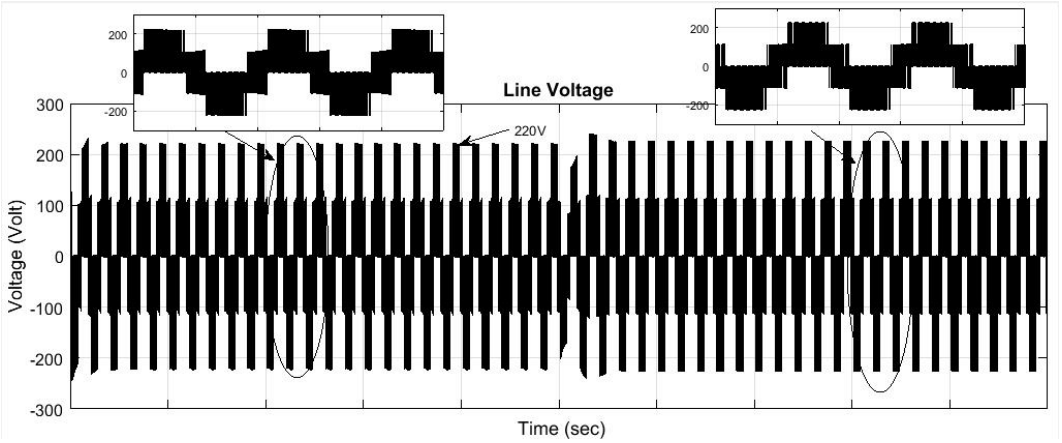

FIGURE 6.12: Inverter output line voltage Vab

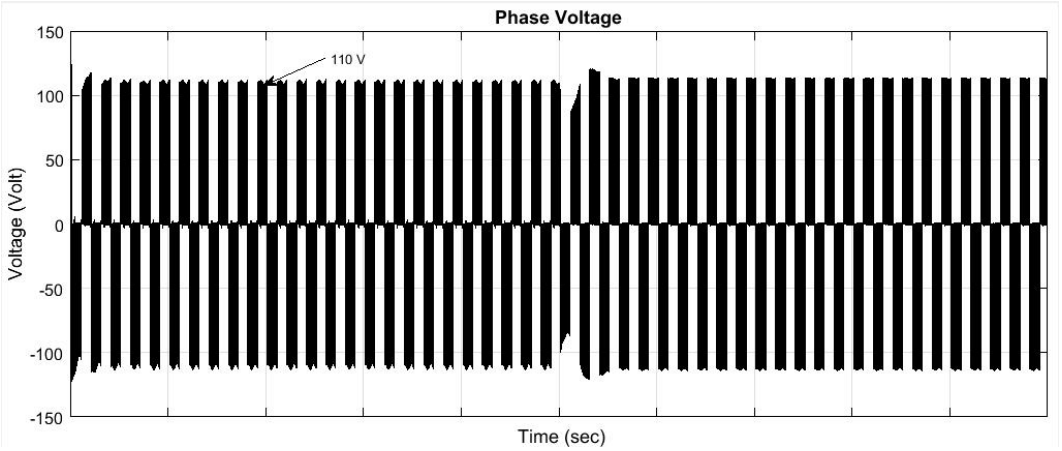

FIGURE 6.13: Inverter output phase voltage Van.

6.4 ACMV ELIMINATION METHOD

For the same setup the Active method to eliminate common mode voltage is used to generate switching pulses for three-level cascaded inverter. For the same

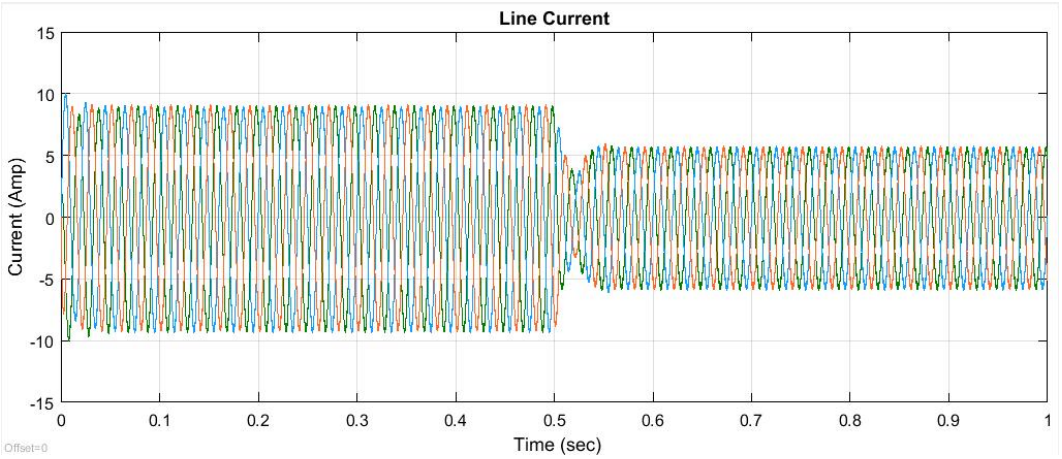

FIGURE 6.14: Three phase Line Current.

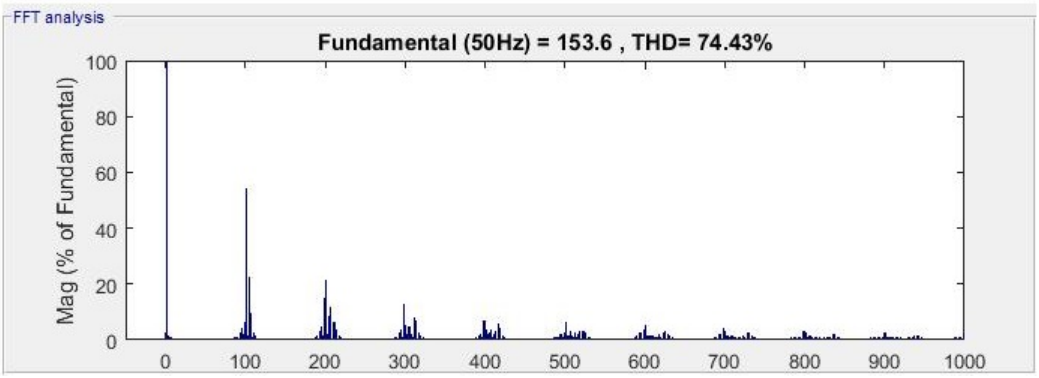

FIGURE 6.15: FFT analysis for 0.6 modulation index

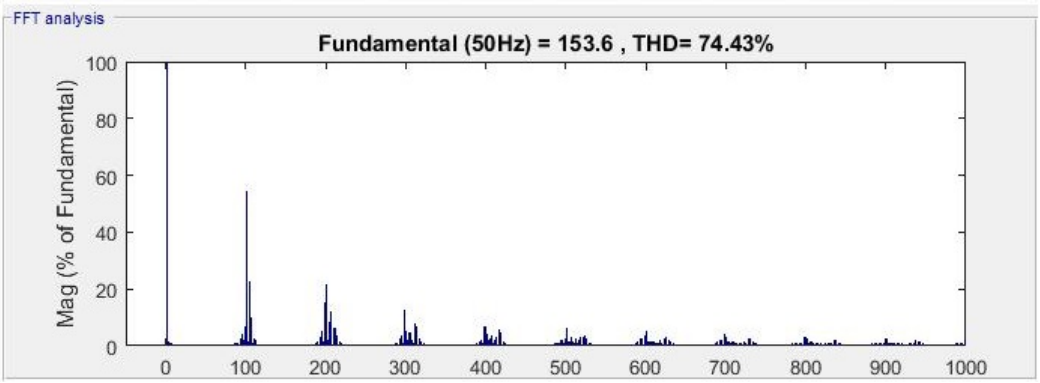

FIGURE 6.16: FFT analysis for 0.37 modulation index

environmental condition discussed above in SVPWM method and conventional CMV elimination method the solar PV dc voltage current and power is shown in figure 6.18. The DC link voltage is 120V for solar irradiation of $1000W/m^2$ and 115V for irradiation of $400W/m^2$, While, the current is changes from maximum value 5.1A to 2A, due to this the power developed by the solar array is changes from 540W to 212W. The Variation in modulation index generated by perturbation

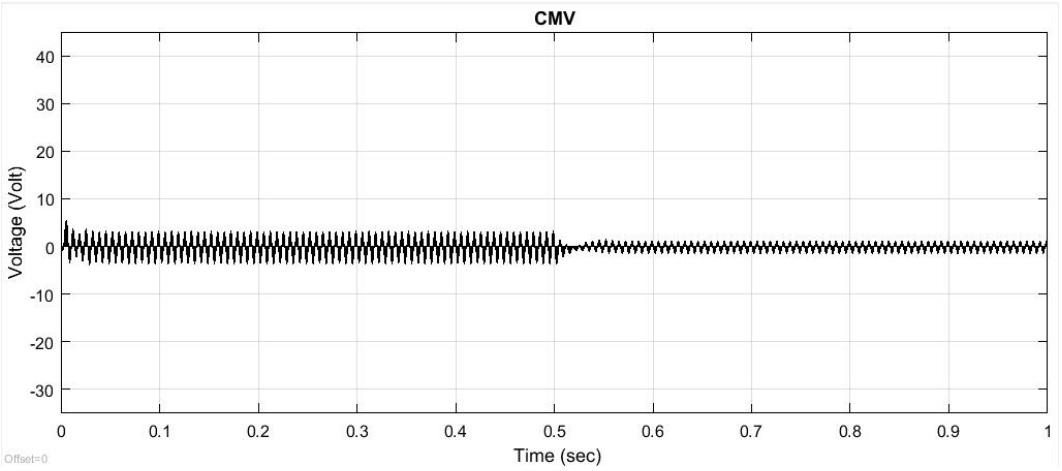

FIGURE 6.17: Common Mode Voltage

and observation MPPT method is changes from 0.6 to 0.37pu due to the change in solar irradiation, as shown in figure 6.19. The generated line and phase voltage of the Active common mode voltage elimination modulation method for cascaded 3-level inverter are shown in figure 6.20 and figure 6.21 respectively. Figure 6.20 shows that for the modulation index of 0.6, the inverter generates three level output voltages 0V,+ 108V and +220V, while at modulation index 0.37pu the inverter behaves like a two level inverter. The maximum value of output voltage at low modulation index is 0V and +110V. The variation of phase voltage with the similar change in modulation index is shown in figure 6.21. The three phase line current is shown in figure 6.22. Due to change in modulation index the current supplied for a fixed RL load is changes. Figure 6.23 and figure 6.24 shows the FFT analysis of line voltage Vab. The total harmonic distortion is varies from 40.40% for higher modulation index and 64% at lower modulation index. The common mode voltage is reduced to near zero value as shown in figure 6.25, the fluctuation of 5V in CMV is due to the fluctuation in the pv output voltage. The three levels of pole voltages shown in figure 6.26 confirm that the cascaded inverter is worked as a three level inverter. The single phase H-bridge inverter is used to inject the voltage equals one sixth of total DC link voltage to eliminate the common mode voltage. The generated output voltage of active H-bridge inverter is shown in figure 6.27. Figure 6.28 show the inject voltage in the line-a.

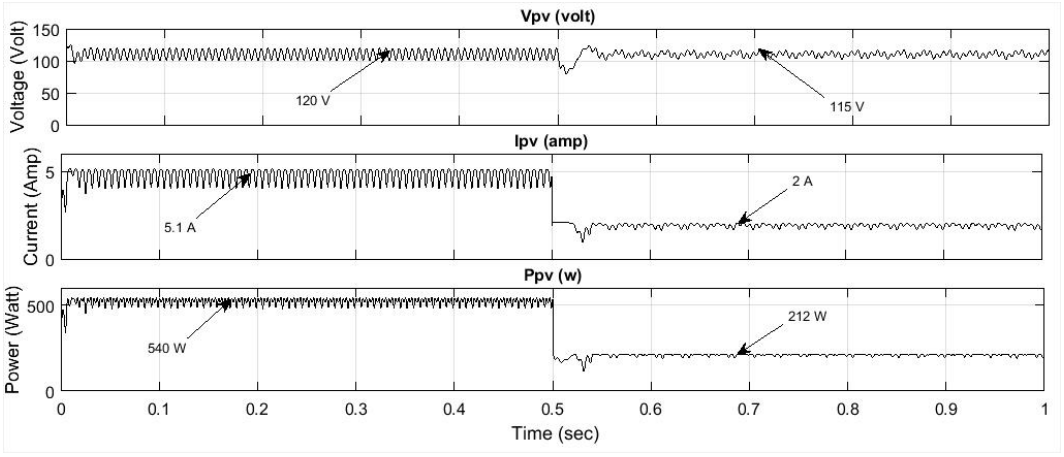

FIGURE 6.18: Voltage, current and power characteristic of PV module.

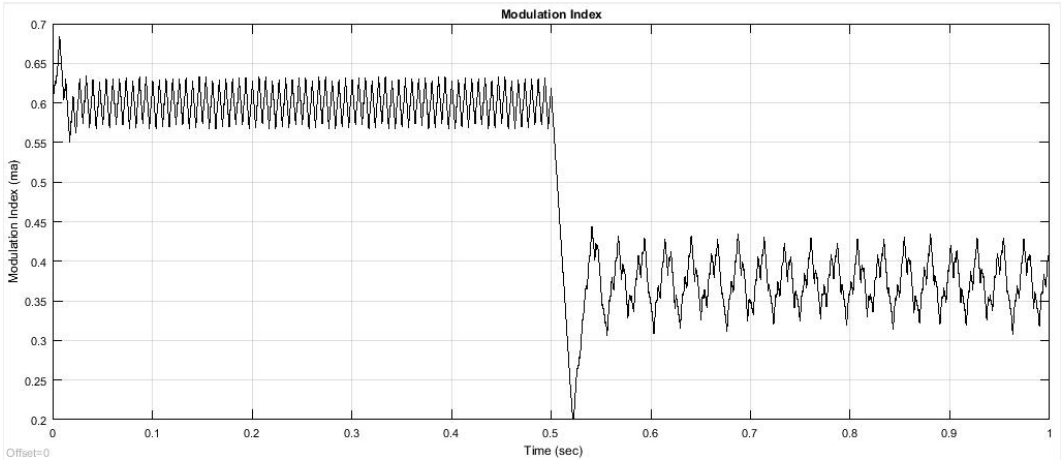

FIGURE 6.19: Modulation index

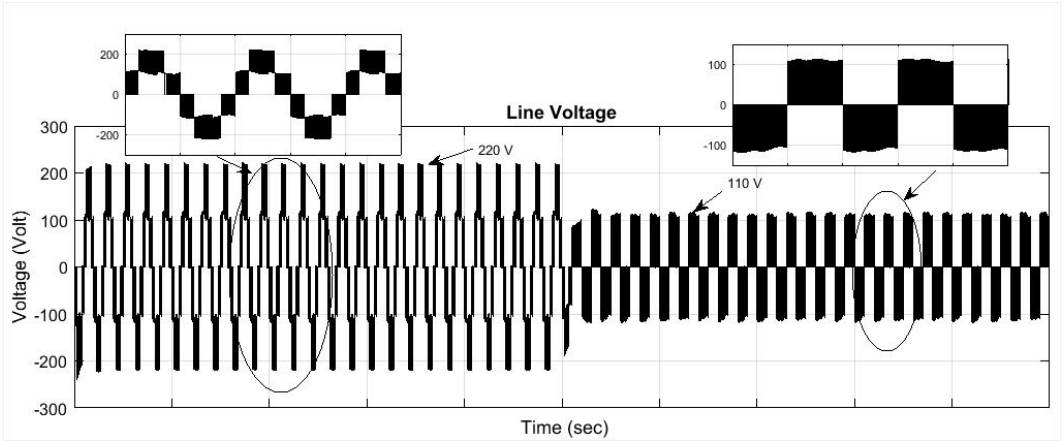

FIGURE 6.20: Inverter output line voltage Vab

6.5 PUMP LOAD WITH SPWM

The results obtained for photovoltaic array fed 3-level cascaded inverter connected with pump load. The variation of irradiation from 500 W/m2 to 600 w/m2 at an

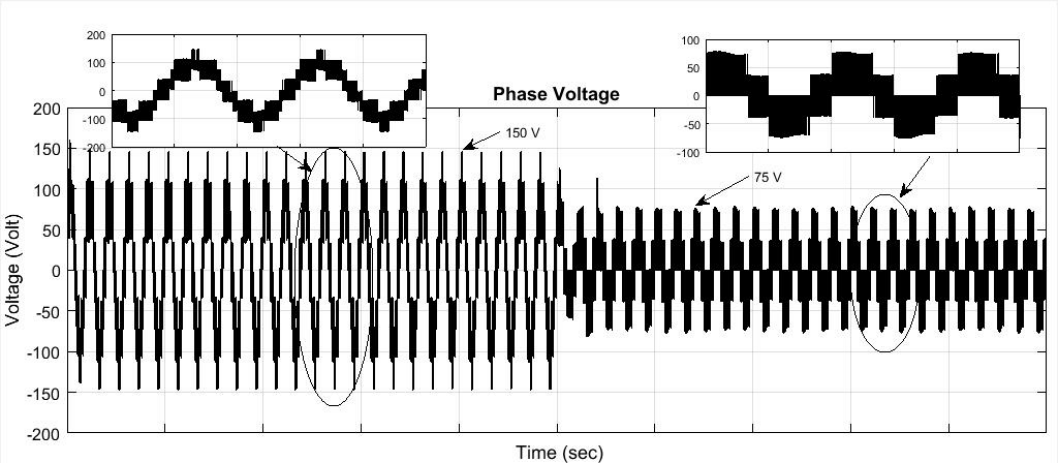

FIGURE 6.21: Inverter output phase voltage Van.

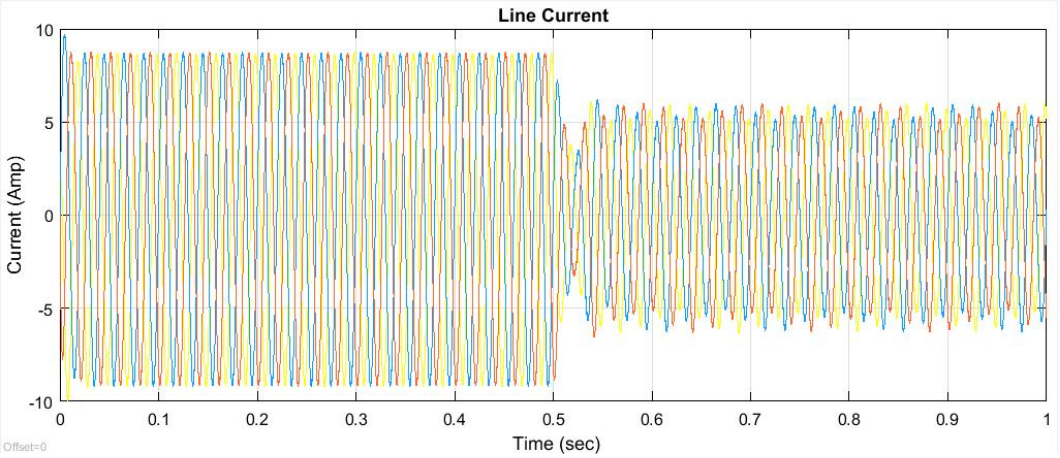

FIGURE 6.22: Three phase Line Current.

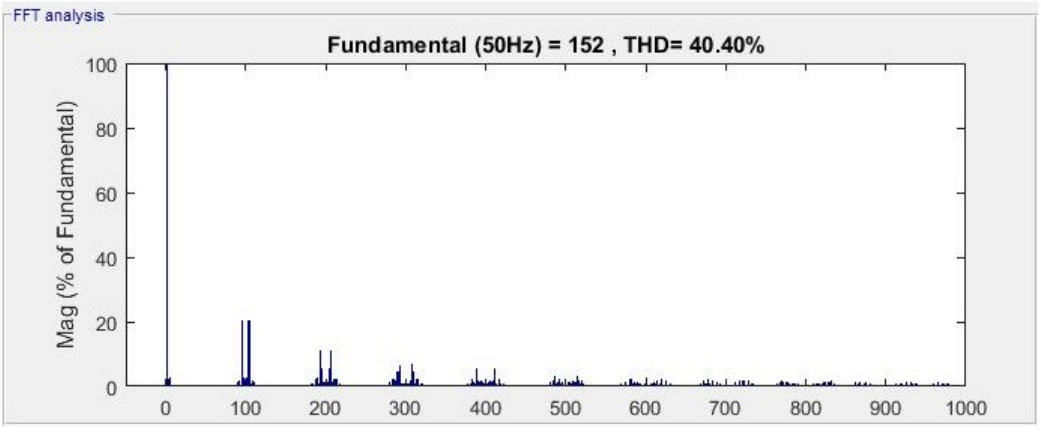

FIGURE 6.23: FFT analysis for 0.6 modulation index

instant 3.2 sec is shown in figure 6.29. the variation of photovoltaic voltage and current with the change in irradiation is shown in figure 6.30. The P&O technique is used to generate the modulation index for the operation at maximum power point. The cascaded 3-level inverter respond to change in modulation index by

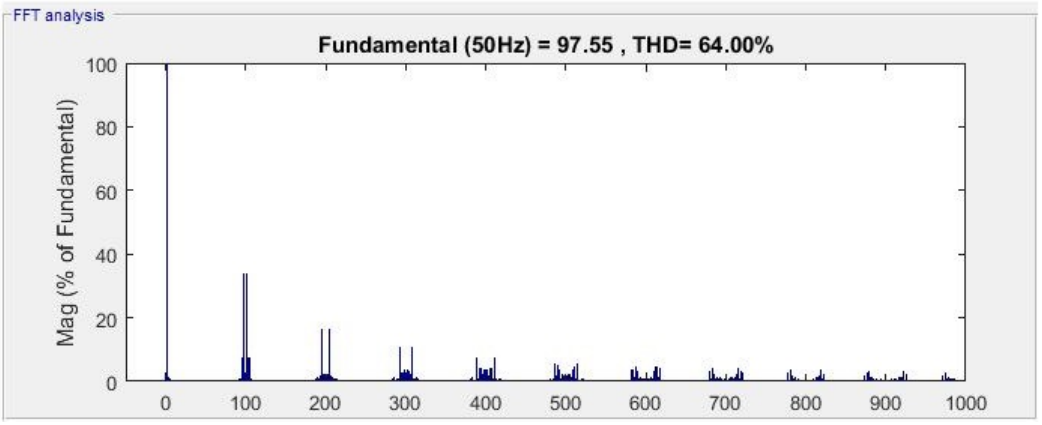

FIGURE 6.24: FFT analysis for 0.37 modulation index

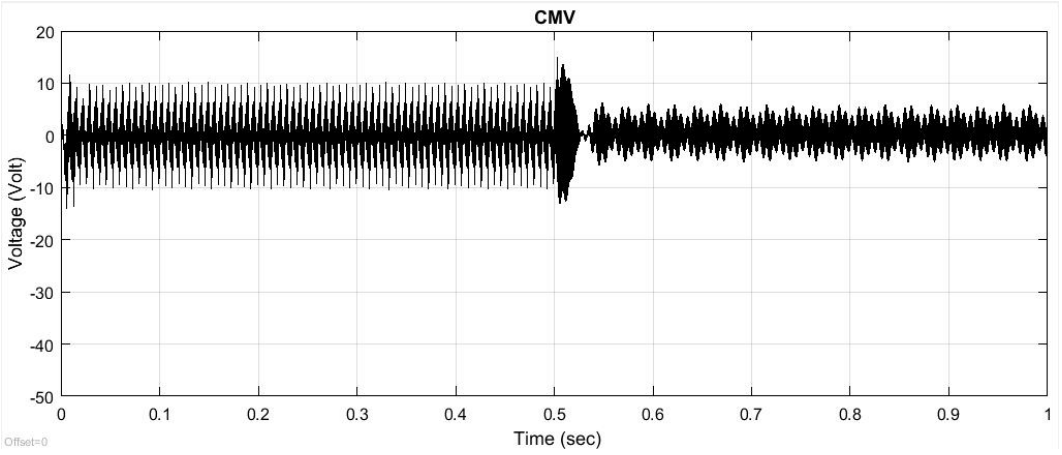

FIGURE 6.25: Common Mode Voltage

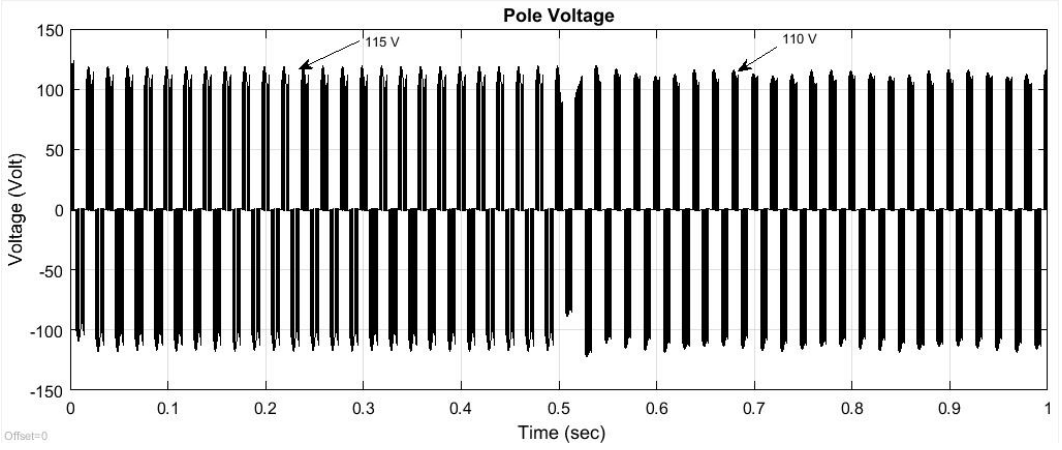

FIGURE 6.26: Pole Voltage of leg-a

changing the output ac voltage. The v/f controller responds the change in voltage by changing the frequency of the output voltage, which adjusted the speed of the motor according to the variation in irradiation. The torque and the speed variation of the motor for a pump load is shown in figure 6.31.

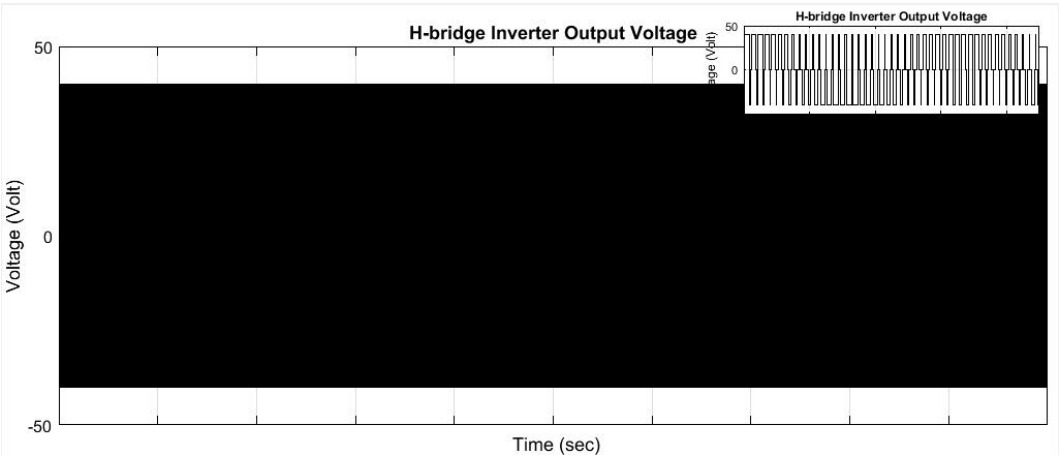

FIGURE 6.27: H-bridge Inverter Output Voltage

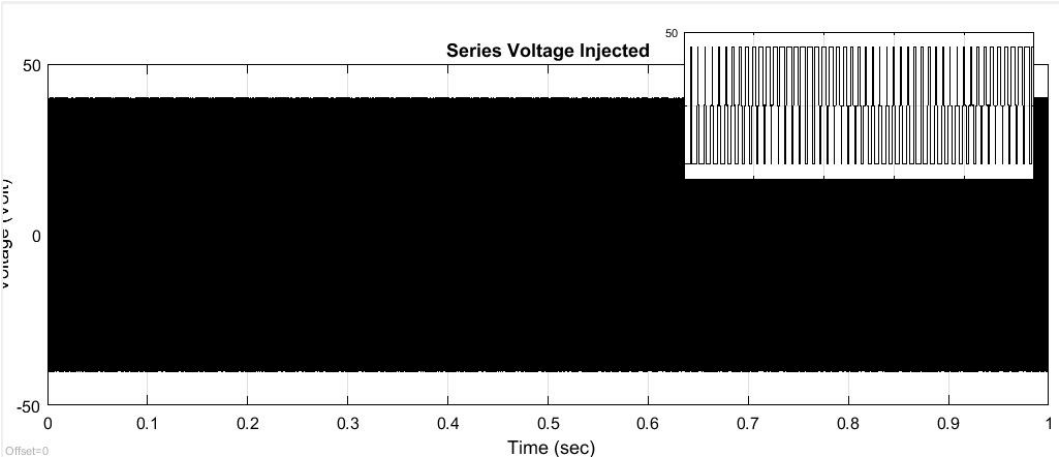

FIGURE 6.28: Voltage injected in series of phase-a

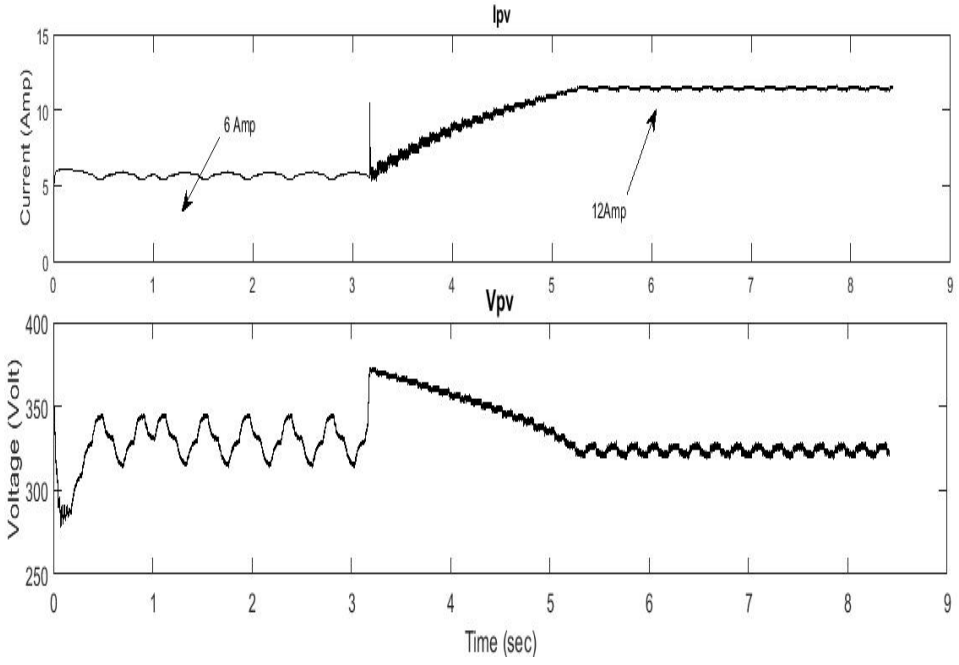

FIGURE 6.29: Characteristics of PV Array used for Pump Load

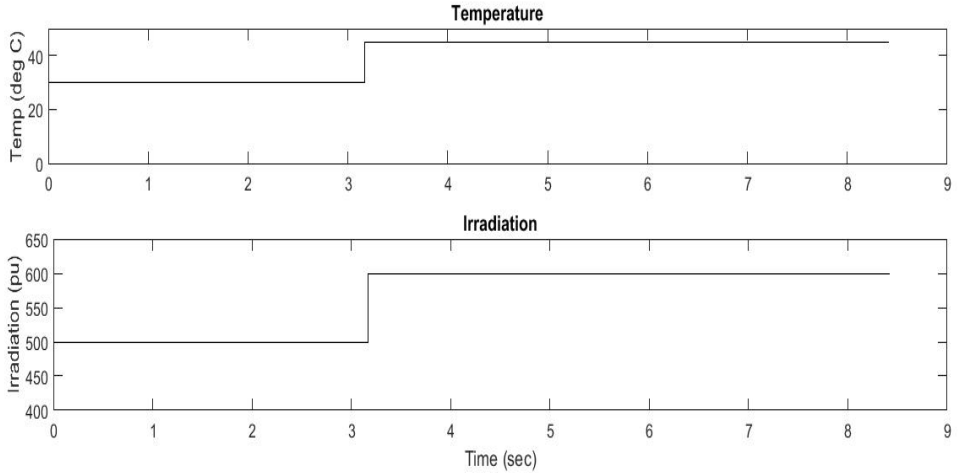

FIGURE 6.30: Variation of Irradiation and Temperature

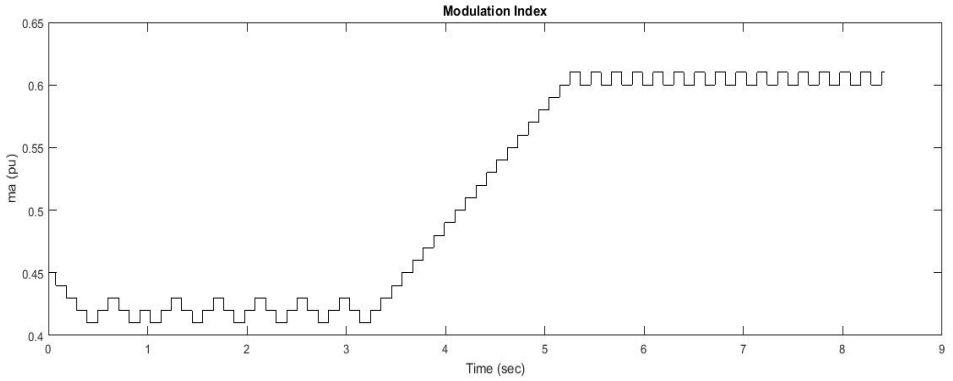

FIGURE 6.31: Modualtion Index

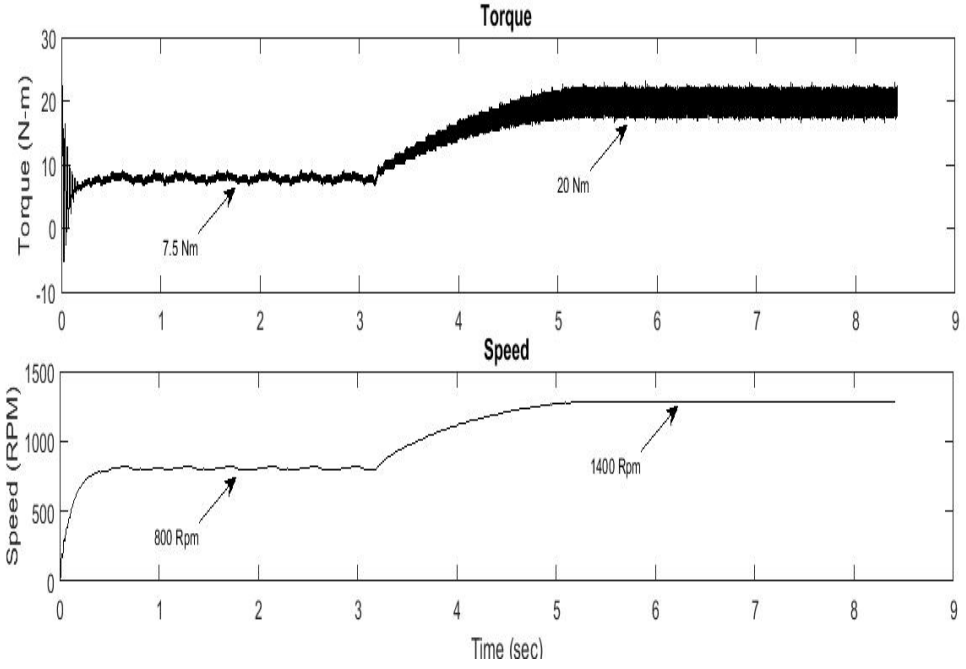

FIGURE 6.32: Speed and Torque Variation

6.6 CONCLUSION

In this chapter three different methodologies SVPWM, Conventional common mode elimination, active common mode elimination is used for the performance analysis of the novel cascaded three level inverter. Conventional common mode voltage elimination method gives constant PV voltage with both lower and higher modulation index. The THD generated by this method is higher as comparison to the normal SVPWM and the proposed active common mode elimination modulation scheme. The common mode voltage generated by SVPWM is very high. For pv fed inverter SVPWM generated unbalanced load current due to the fluctuation in the modulation index at low irradiation, while conventional method for CMV elimination gives the balanced current at both higher and lower modulation index. The performace analysis of Pump load is also discussed.

Chapter 7

Hardware Implementation

A laboratory prototype of Active common mode voltage elimination using SVPWM for cascaded three level inverter is designed to supply a three phase RL load. The schematic diagram of inverter topology is shown in figure 3.5. and the complete block diagram of proposed system is figure 3.14. The developed hardware model is shown in figure 7.1. The figure 7.1 shows the 3-level cascaded inverter setup connected with RL-load. The voltage devider circuit is used to reduce the voltage from 200V to 60V for the open loop testing of the system. Two 1000microfarad, 400V capacitors are used to split the DC supply for cascaded inverter. A H-bridge inverter is used to inject the series voltage for CMV elimination. The hardware setup for the H-bridge inverter is shown in figure 7.2.

The prototype model is composed of the following parts:

- RL load,
- power circuit of H bridge and Three level inverter,
- Voltage and current sensor circuits.
- control hardware such as dead band and amplification circuits.

FIGURE 7.1: Cascaded Three-level Inverter

- Regulated power supplies.

The Prototype model is tested on 60V.

7.1 DESIGN OF HARDWARE COMPONENTS

The main hardware components are:

FIGURE 7.2: H-bridge Converter

FIGURE 7.3: Volgage Sensor

- Design of mosfet driver circuit
- Voltage and current sensor
- development of control hardware

The 3-phase, 3-level inverter circuit is designed by using 12 MOSFETs. MOSFET IRFG-460 is used because of high switching frequency and low cost. For protection

of MOSFETs snubber circuits and metal oxide varistors are used. Also heat sinks are mounted with each MOSFET for protection from excessive heat.

7.1.1 MOSFET Driver Circuit

The detailed MOSFET driver circuit diagram is shown in figure 7.4. When the gate pulse is gieven to the base of input transistor, input transistor goes into saturation state and current starts flowing through LED of optocoupler. The phototransistor of optocoupler turns ON and thus no base drive goes to the output transistor and hence output transistor remains in cutoff state making gate to source voltage at 12V.

12V is generated by using a diode bridge rectifier and regulator 7812. 12V is connected to the collector of output transistor by using a pull-up resistor. Whenever input pulse is low, input transistor remains in cutoff state making photo transistor int cutoff state. Hence output transistor gets base drive and goes into saturation state with nearly 0.2V collector to emitter voltage hence 0.2V gate to source voltage of MOSFET. Thus optocoupler provides required isolation as well as different grounds for all the valves. R1= 1.2k R2= 10k R3= 1.2k R4= 10k R5= 470 Rx= 4.7k, 5w Cx= 100nF, 1000V T2, T1= 2N2222A Diode=IN4007 Optocoupler= MCT2E Snubber diode=IN5408

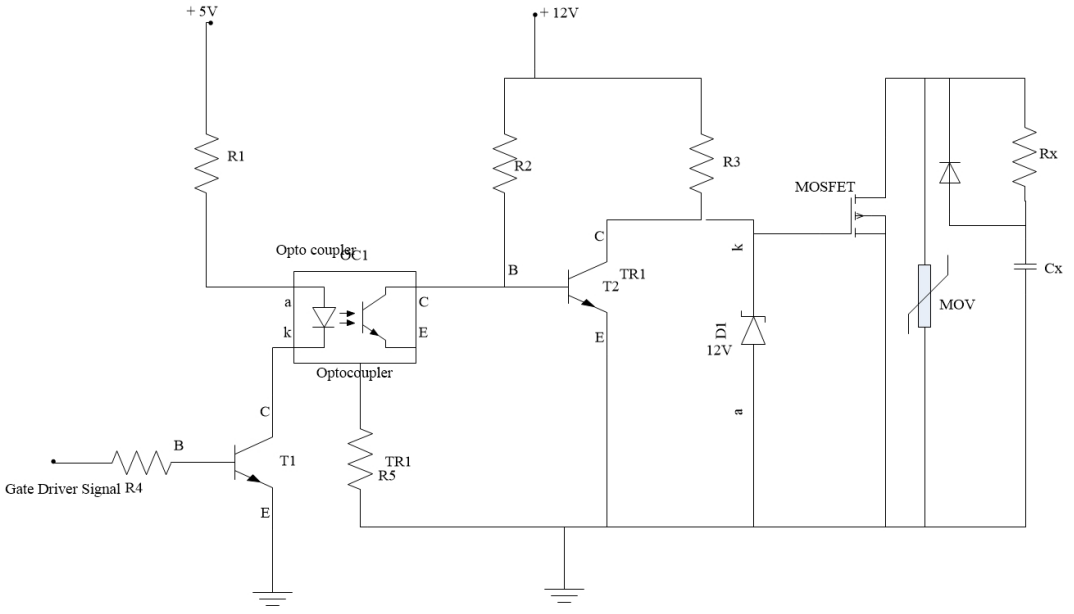

FIGURE 7.4: MOSFET driver circuit

7.1.2 Snubber Circuit and varistor

The schematic diagram of snubber circuit and protection circuit of MOSFET is shown in figure 7.4. Snubber circuit include metal oxide varistor (MOV) to protect from over voltage. Protection circuit include snubber circuit and metal oxide varistor (MOV) . MOV is used to protect the switch from over voltages. It is also known as voltage dependent resistor (VDR) and has non-linear and non-ohmic current-voltage characteristic. The RC snubber circuit is used provides protection against large di/dt and voltage transients. A 4.7K, 5W resistor and a 0.1micro farad, 1000V snubber capacitor is used for the snubber circuit

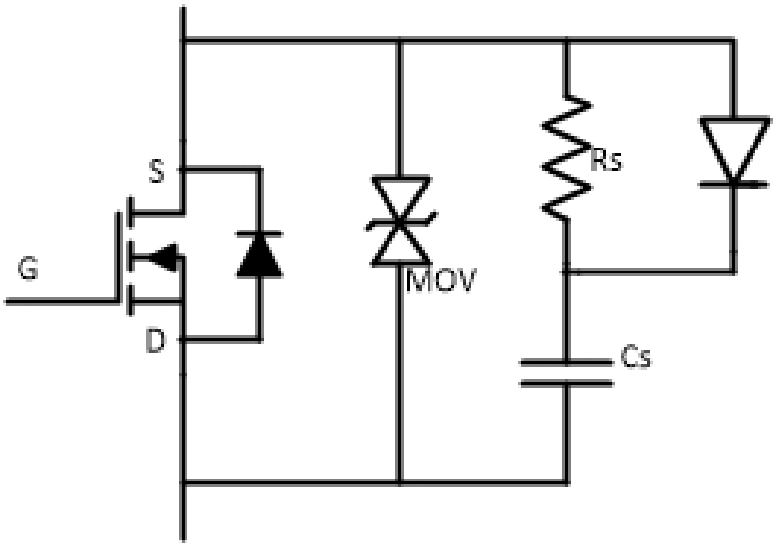

FIGURE 7.5: Snubber circuit for MOSFET protection

7.1.3 Voltage Sensing Circuit

AD202JN analog isolator is used for the purpose of sensing the voltages. The first Op-amp is working as a buffer and the second Op-amp is used for level shifting. The AD202JN is used for sensing AC and DC voltages. The output of the voltage sensor is at a very low level hence the output of the voltage sensor is directly applied to the controller input pins. The circuit diagram of the voltage sensing circuit is shown in figure 7.6

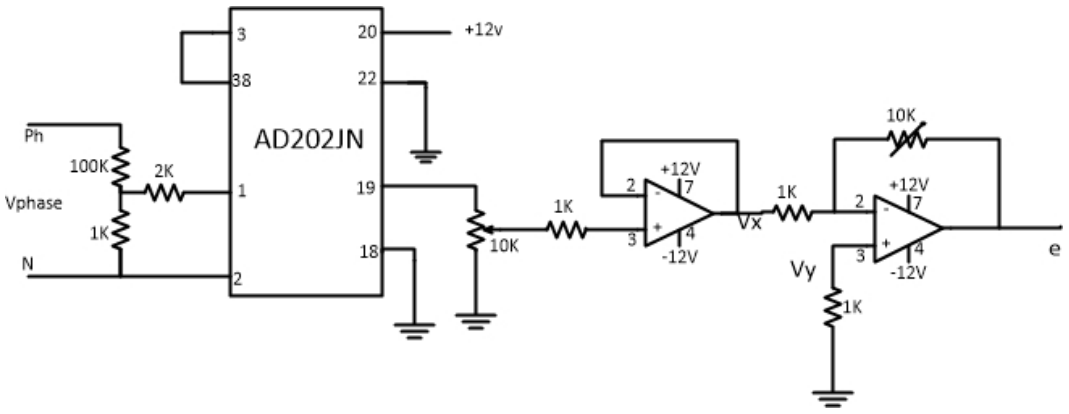

FIGURE 7.6: Voltage sensing circuit

7.1.4 Current Sensing Circuit

The Hall effect sensor (HTP 50) is utilized to develop a current sensor circuit. The Hall effect sensor isolate high power circuit and low power circuit of controller. The sensor transformation ratio is 1000:1. The designing of this current sensor is applicable in both AC as well as DC supply system. The output of this current sensor circuit is interms of voltage with respect to the current applied. The cicuit diagram of current sensor circuit is shown in figure 7.7.

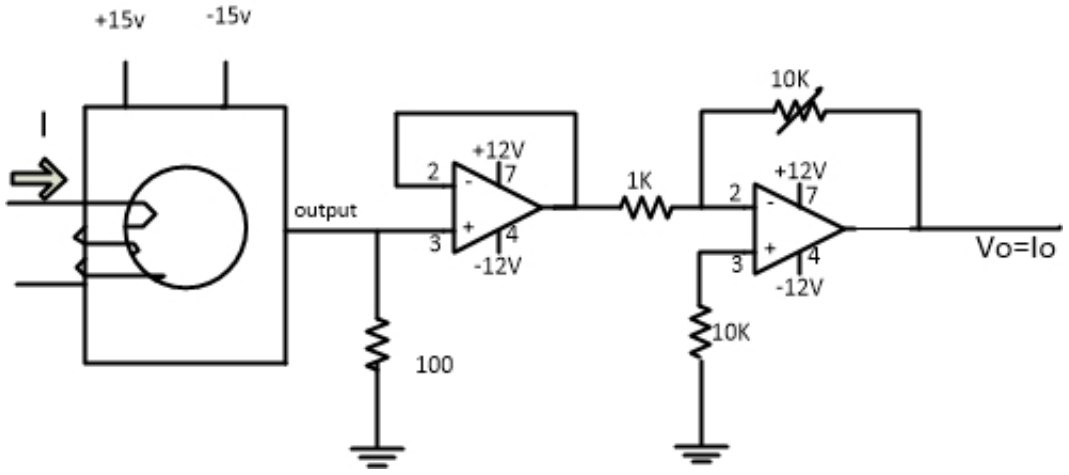

FIGURE 7.7: current sensor circuit

7.1.5 Power Supplies

DC supplies (+12v G -12v, +15V G -15V, +5v) are required for the voltage sensor circuit, current sensor circuit and MOSFET drive circuits. The regulator ic 7812, 7815 and 7805 are used for +12V, +15V and for +5V regulated supply. The

regulator ic 7912, 7915 are used for -12 and -15V dc supply. The circuit diagram of the supply circuits are shown in figure 7.8, figure 7.9 and figure 7.10.

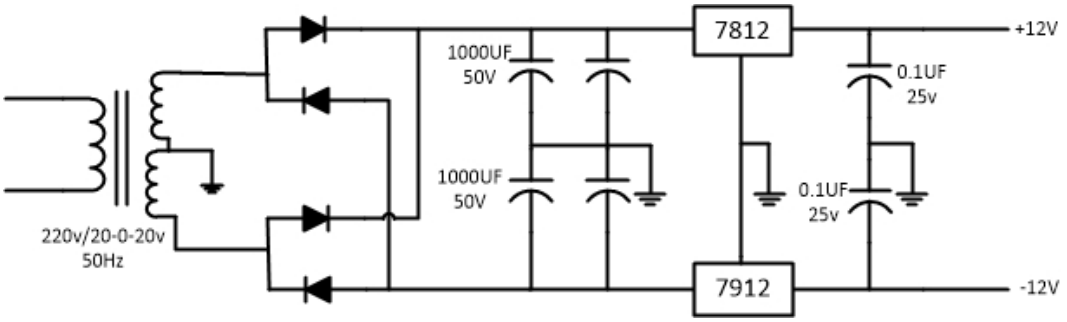

FIGURE 7.8: +12V & -12V supply

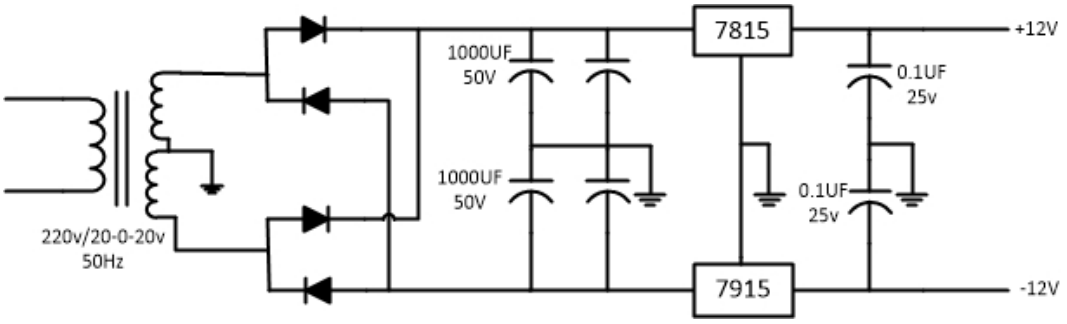

FIGURE 7.9: +15V & -15V supply

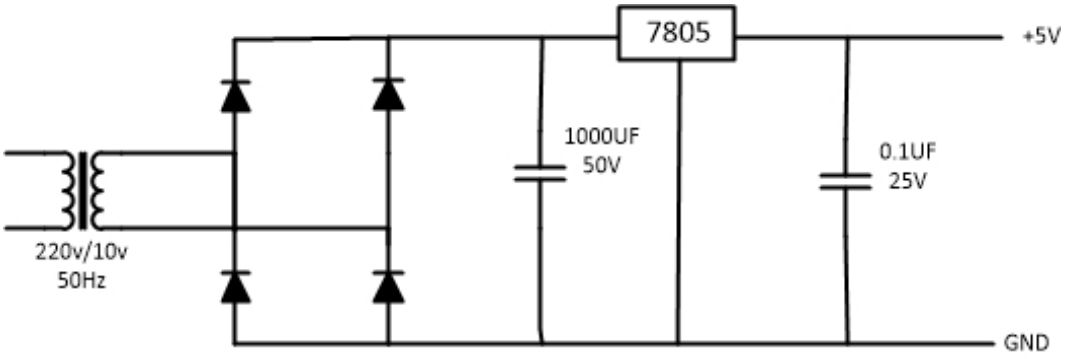

FIGURE 7.10: +5V supply

7.1.6 Dead Band

Dead band circuit is used to provide the dead band between the consecutive gate pulses of MOSFET for the same leg of an inverter. To provide the dead band of 10 micro second a resistor of 1k-ohm, a capacitor of 0.01 micro farad, the NOT gate ic 7404 and AND gate ic 7408 is used. The circuit diagram of the dead band circuit is shown in figure 7.9.

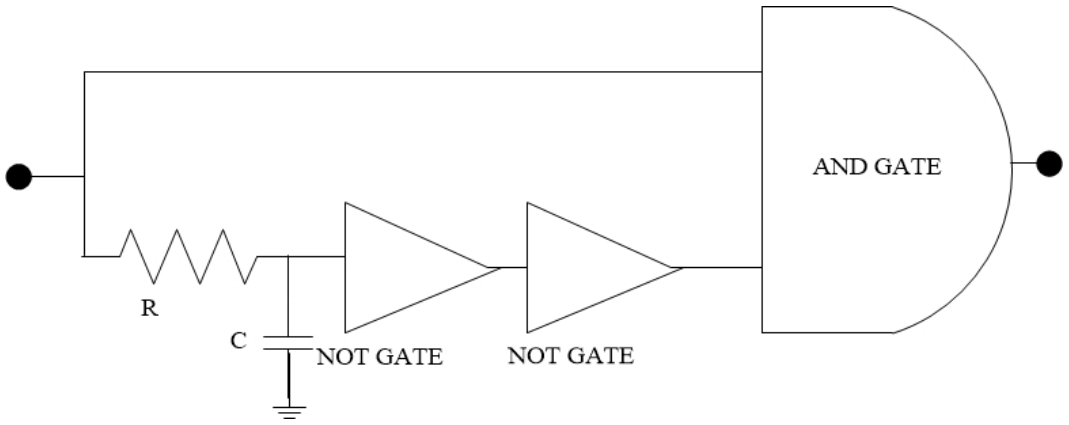

FIGURE 7.11: Dead band circuit

7.2 HARDWARE RESULTS

Open loop three level inverter is tested with dc source and two dc link capacitors are used to split the dc supply for the inverter. The system is tested for 3kHz switching frequency. The DS1104 R&D controller board is used to generate the firing pulses of the inverter. For the modulation index of 0.8 the generated phase voltage of the three level inverter are shown in figure 7.14. The Gate Pulse of leg-a and pole voltage of all legs are shown in figure 7.13 and figure 7.14 respectively.

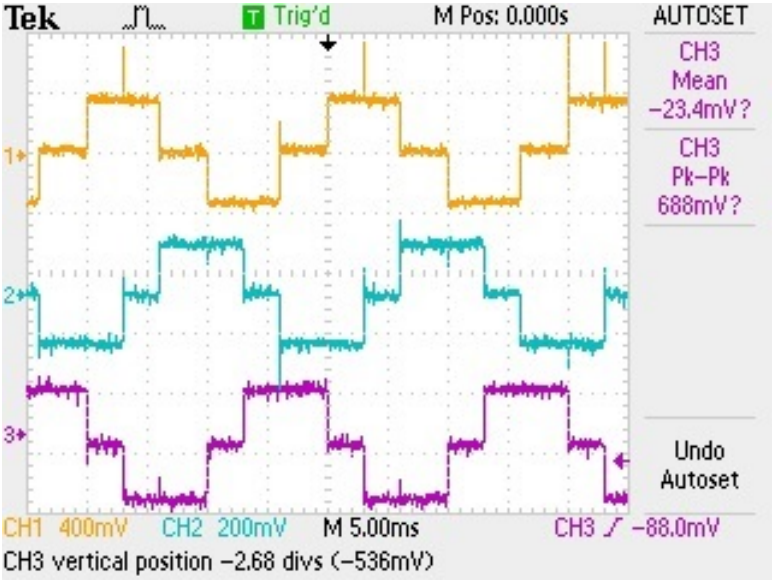

FIGURE 7.12: Pole Voltage of Leg-a

The complete hardware setup is shown in figure-7.16.

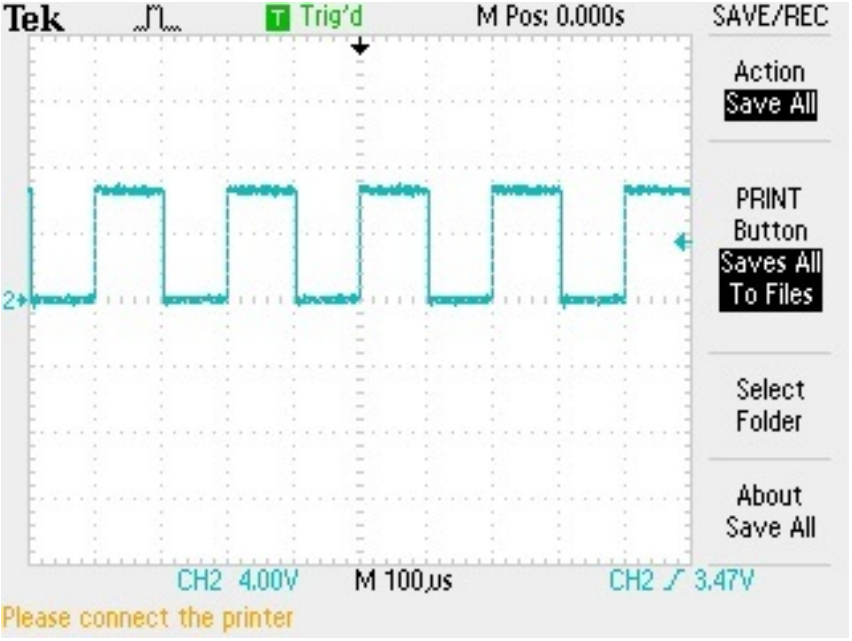

FIGURE 7.13: Gate Pulse of one switch

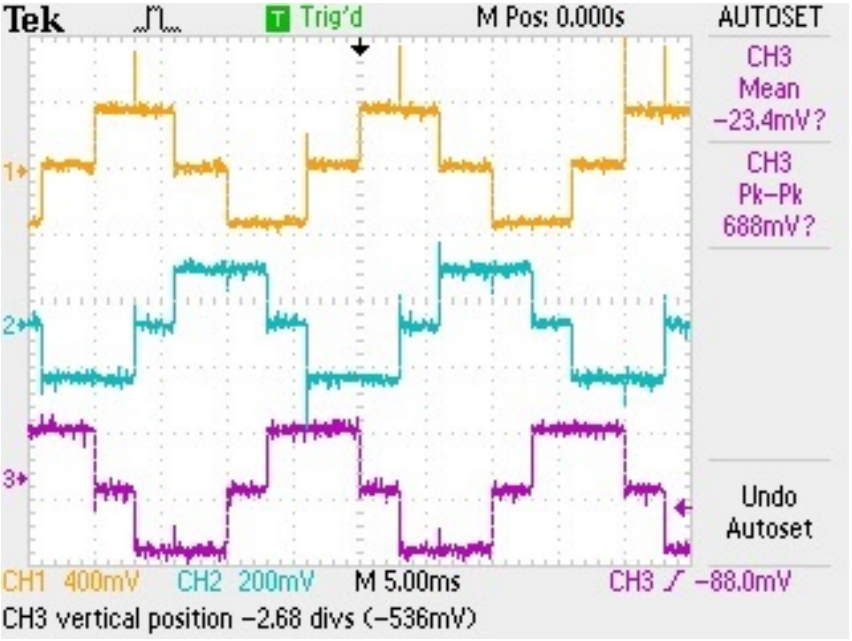

FIGURE 7.14: Phase voltage

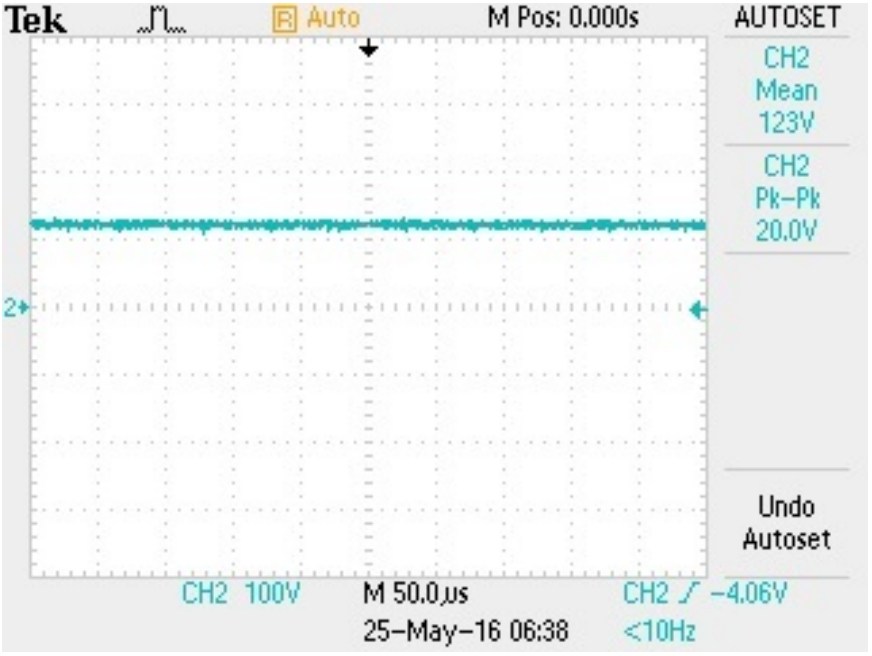

FIGURE 7.15: Voltage across DC link capacitor

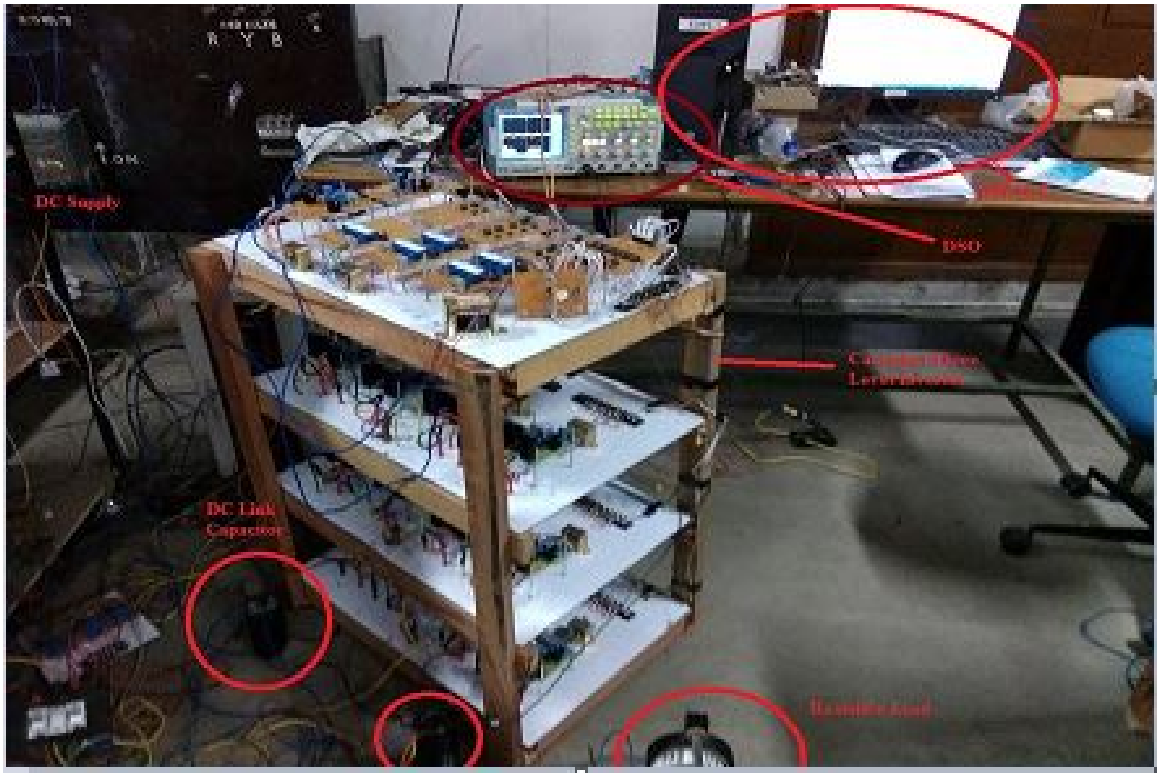

FIGURE 7.16: Voltage across DC link capacitor

7.3 CONCLUSION

In this chapter the designing of hardware components are discussed. The result for three level inverter with 0.8 modulation index is also discussed. The proposed inverter worked satisfactory for the dc supply.

Chapter 8

Conclusion & Future Scope

CONCLUSION

In this desertation work, three different modulation schemes (SVPWM, Conventional common mode elimination, active common mode elimination) of photovoltaic connected RL load have been proposed and simulated on MATLAB/ Simulink. The comparison has been made on the basis of their THD, common mode voltage and fluctuating in the modulation index.

Conventional common mode voltage elimination method gives constant PV voltage with both lower and higher modulation index. The THD generated by this method is higher as comparison to the normal SVPWM and the proposed active common mode elimination modulation scheme. The common mode voltage generated by SVPWM is very high. For pv fed inverter SVPWM generated unbalanced load current due to the fluctuation in the modulation index at low irradiation, while conventional method for CMV elimination gives the balanced current at both higher and lower modulation index. The performace analysis of Pump load is also discussed.

FUTURE SCOPE OF THE WORK

It is observed that the performance analysis of VSI base PV is enhanced with increase in level but at the same time complexity of system increases. Therefore, an optimum level will be worked out according to load requirement. Their are

number of theories are available for tracking the maximum power through out the operation, the advanced Artificial intelligence based MPPT techniques will be consider to reduce the fluctuation in modulation index and will give better performance for rapidly changing environmental conditions.

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Ashish Srivastava, S. P. Singh, "Performance Analysis of Single Stage Standalone PV fed Novel Three level Inverter", *2016 IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems*, June 2016.

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Appendix-A

.1 SIMULATION MODEL OF SVPWM BASED THREE LEVEL CASCADED INVERTER FOR RL-LOAD

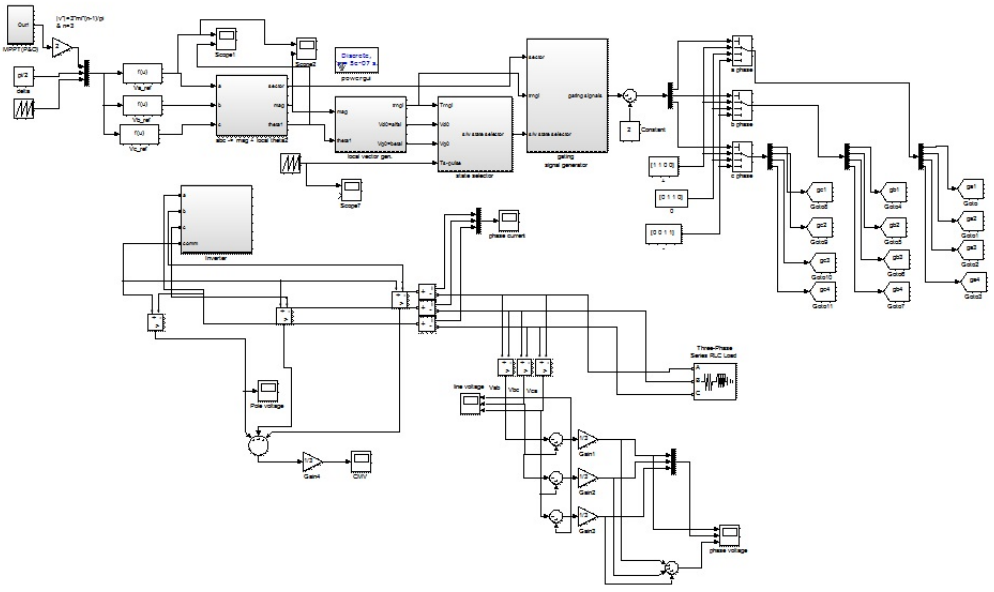

FIGURE A.1: SVPWM complete MATLAB/Simulink diagram

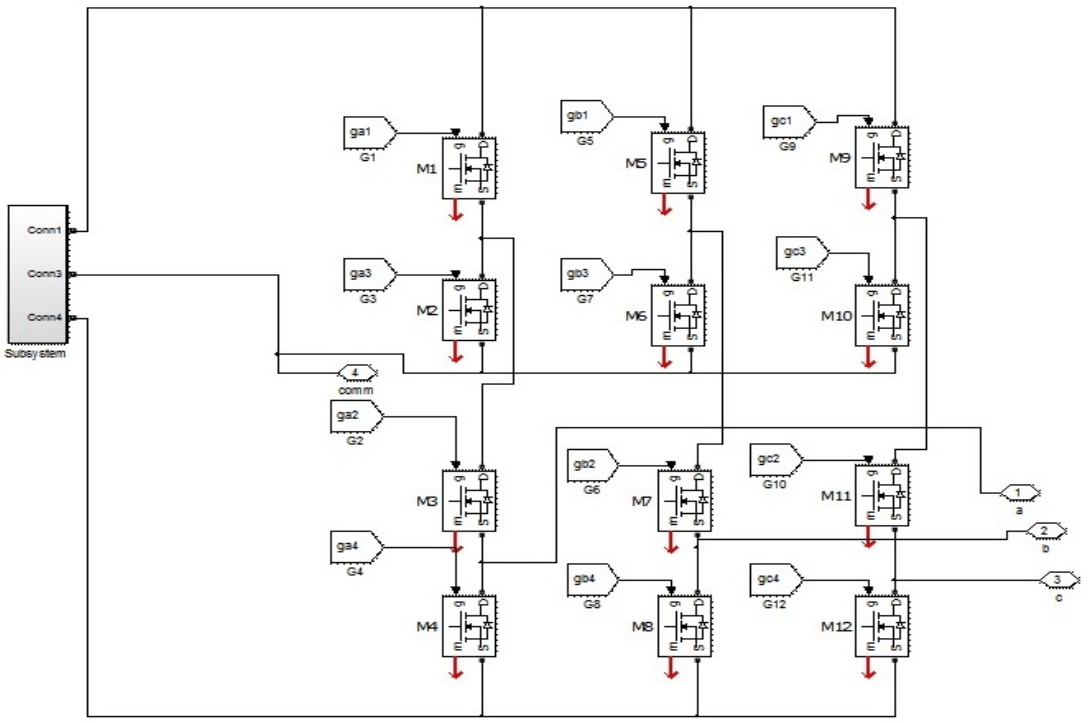

FIGURE A.2: Cascaded inverter

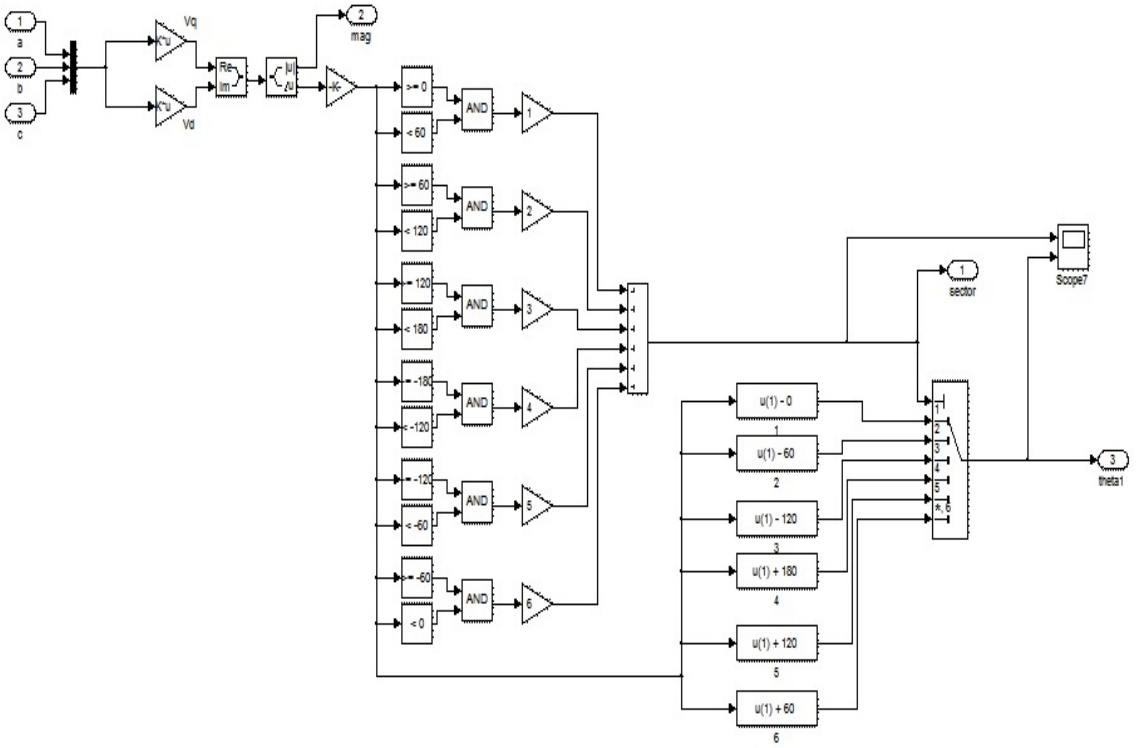

FIGURE A.3: Sector Generation block

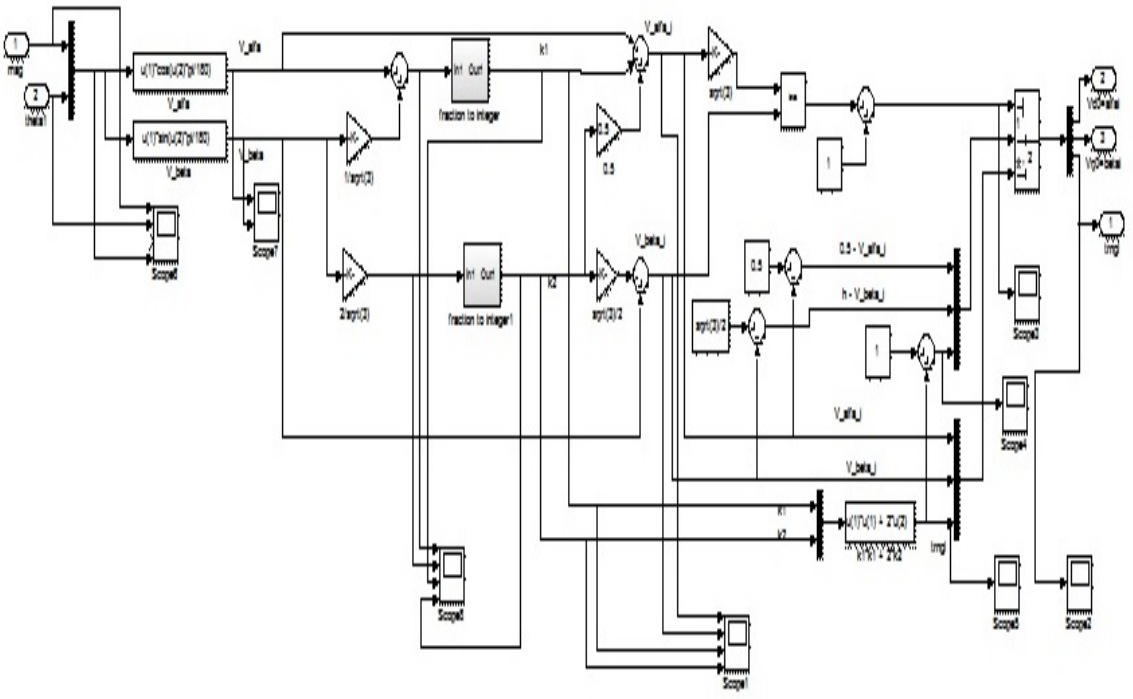

FIGURE A.4: Local Vector generator block

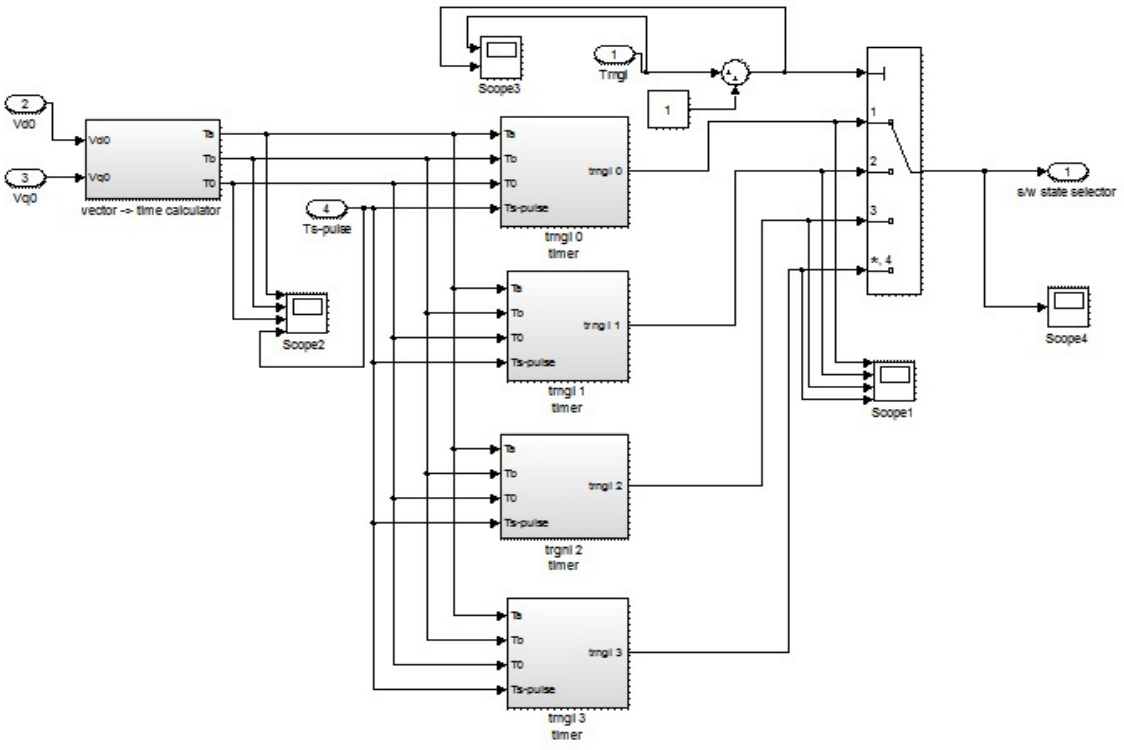

FIGURE A.5: Sector Selector block

.2 MATHEMATICAL MODEL OF THE THREE PHASE INDUCTION MOTOR WITH PUMP LOAD

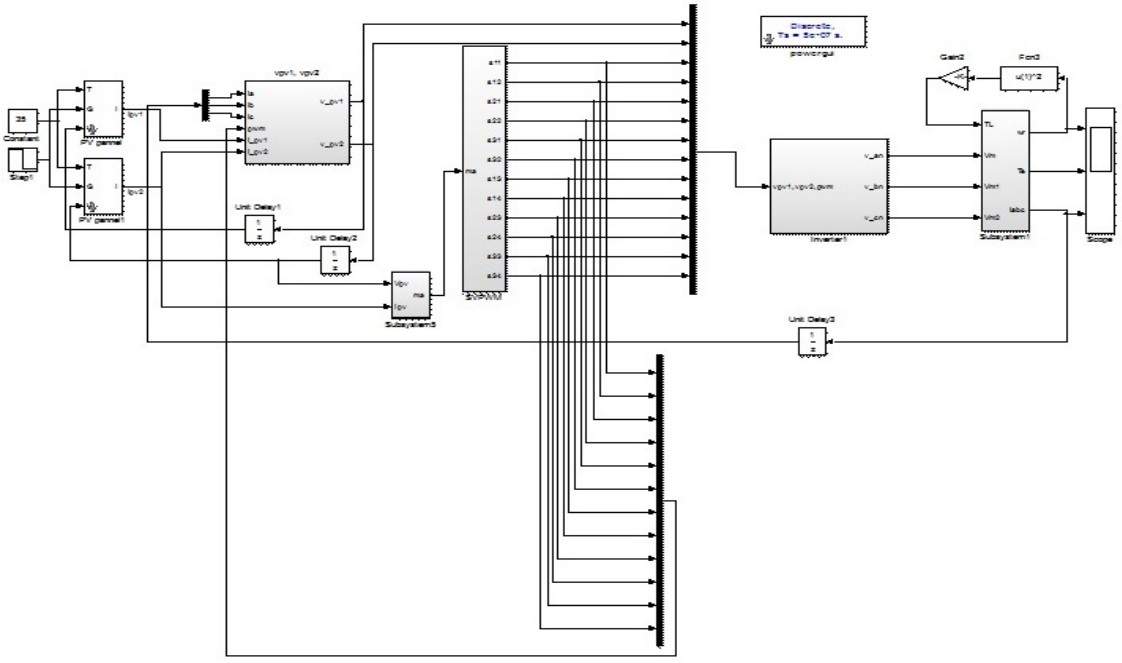

FIGURE A.6: MATLAB/Simulink block diagram of PV connected Cascaded Inverter fed Pump load

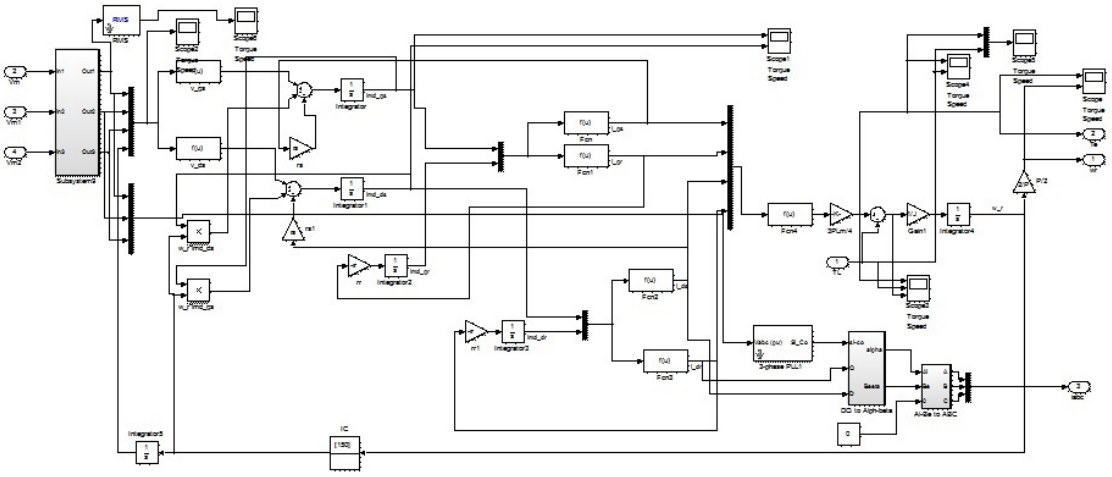

FIGURE A.7: Induction motor model

Appendix-B

.1 INDUCTION MOTOR PARAMETERS FOR PUMP LOAD

Rs = 1.405

Rrp = 1.395

Lls = 5.839e-3

Llrp = 5.839e-3

Lm = 172.2e-3

J = 0.01

B = 1.1e-3

P = 4

$N_dq = 0$;

$N_rotor = 1000$;

.2 SPECIFICATION OF ONE SOALR PV MODULE

The solar array parameter for the pump load used is CEL-PM180 make by Central Electronics Ltd.

Max Power (Pm): 60W

Voltage at Max Power (Vmp): 16.9V

Current at Max Power (Imp): 3.56A

Open Circuit Voltage (Voc): 20.3V

Short Circuit Current(Isc): 3.99A

Max Power Tolerance: -5/+10

Nominal Operating Cell Temp.: 46C 2

Number of Cells: 64

Temperature Coefficients:

Power -0.38

Voltage -60.8mV/C

Current 2.3mA/C

.3 MATLAB Code for MPPT P&O

function D = PandO(Param, V, I)

Dinit = Param(1); Dmax = Param(2); Dmin = Param(3); deltaD = Param(4);

persistent Vold Pold Dold;

dataType = 'double';

if isempty(Vold) Vold=0; Pold=0; Dold=Dinit; end P= V*I; dV= V - Vold; dP= P - Pold;

if dP = 0 if dP ¡ 0 if dV ¡ 0 D = Dold - deltaD; else D = Dold + deltaD; end else if dV ¡ 0 D = Dold + deltaD; else D = Dold - deltaD; end end else D=Dold; end

if D ¿= Dmax —— D¡= Dmin D=Dold; end

Dold=D; Vold=V; Pold=P;

Appendix-C

.1 dSPACE CONTROLDESK

The following figure shows the main window of dSPACE ControlDesk.

FIGURE C.1: Main window of dSPACE ControlDesk

Basic elements of ControlDesk are as-

Menu bar: The menu bar provides access to ControlDesk's functions and commands. Via the menu bar, ControlDesk provides access to common functions and commands to work with ControlDesk. The basic menu bar has the following menues:File, Edit, View, Tools, Experiment, Instrumentation, Platform, CAN, Window, and Help.

Navigator: ControlDesk provides different Navigator views to structure the functions for managing the platform, handling files, building instrument panels, and creating automation tasks. Following are the various components of

ControlDesk Navigator- *Experiment Navigator:* The Experiment Navigator displys all the files (Instrument panels, parameter sets and reference deta) belonging to an experiment and provides functions to handle the experiment and its components.

Instrument Navigator: The instrument navigator allows to build instrument panels to control and monitor the variables of a model. Layout windows are the areas of ControlDesk where instrument panels are built. The instrument selector grants access to all available instruments. ControlDesk offers a set of instruments for building a virtual instrument panel.

Platform Navigator: The platform navigator displays all platforms registered in the system and provides functions to register the boards and handle applications such as load, start, and stop.

Tool Window: The Tool Window provies certain tools depending on the activated navigator. These are-

Log Viewer: The Log Viewer displays messages generated by ControlDesk or the real-time board.

Interpreter: The Python Interpreter handles Python commands and scripts for ControlDesk and Test Automation.

File Selector: The File Selector lets us select and download applications (APL, AXP, DDS, M, MDL, OBJ, PPC and SDF files) with drag & drop.

Data Capturing using ControlDesk

dSPACE ControlDesk allows to capture the data from real-time applications or simulink simulations. The captured data can be saved and monitored with data acquisition instruments. These instruments are used to visualize the captured data. The CaptureSettings Window is used to control the data capture in ControlDesk. Data capturing starts immediately after the animation starts.