VOLTAGE STABILITY MONITORING USING SYNCHROPHASOR DEVICES

A DISSERTATION

Submitted in partial fulfillment of the
requirements for the award of the degree
of
Master of Technology
in
ELECTRICAL ENGINEERING
(With specialization in System & Control)

By

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Candidate's Declaration

I hereby declare that this thesis which is being presented as the final evaluation of the dissertation **VOLTAGE STABILITY MONITORING USING SYNCHROPHASOR DEVICES** in partial fulfillment of the requirement of award of Degree of Master of Technology in Electrical Engineering with specialization in System and control, submitted to the Department of Electrical Engineering, Indian Institute of Technology, Roorkee , India is an authentic record of the work carried out during a period from May 2015 to May 2016 under the supervision of Dr. Vishal Kumar (Department of Electrical Engineering, IIT Roorkee). The matter presented in this report has not been submitted by me for the award of any other degree of this institute or any other institute.

Date:
Place: (Patel Hiral Kumar)

Certificate

This is to certify that the above statement made by the candidate is correct to best of my knowledge.

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A dissertation or any publication can reach to the acme only by the proper guidance, cooperation and kind words of the individuals involved.

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ABSTRACT

The post-mortem analysis of the major blackouts in the history made power system experts to concentrate more in the field of monitoring of the grid therefore advanced wide are monitoring has become necessary to maintain the stability of the network. Advanced monitoring is done here by the use of PMU-Synchrophasor Device and by its implementation on real time digital simulator (RTDS).

The main contribution of this dissertation is a scheme for optimal phase measurement unit (PMU) placement based on superset and depth of unobservability concept. PMU placement is done in various phases by ensuring that the set of the placed PMUs in the next phase will be a superset of the previous phase. The proposed scheme is modification of spanning tree method with additional constraints. This scheme is verified by placing PMUs on various locations equal in nos. placed in spanning tree method in standard IEEE 14 bus test system. By the complete knowledge of states of the system, stability prediction of the buses is possible by the use of stability indices in any complex power system network. The outputs of the PMUs are utilized directly for determining the stability index. After getting optimum resultant locations of PMUs, the measurements received from the placed PMUs are used to determine the fast voltage stability index (FVSI) for further monitoring of the power system network. Testing of PMUs is very much necessary for its applications and further process of data for simple visualization of any complex network.

To validate all the objectives, the complete scheme has been implemented on RTDS to achieve the values of the index at very high data rate. Successful placement of PMUs at optimal locations of the IEEE 14 bus test system on real time simulation test bed will show values of the states at sampling rate of 48 samples per second. So, the values of FVSI getting after PMU measurements will be extremely dynamic and it is possible to predict the voltage stability of the buses more accurately or to maintain complete network stability.

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Abbreviations

PMU	**P**hasor **M**easurement **U**nit
FVSI	**F**ast **V**oltage **S**tability **I**ndex
RTDS	**R**eal **T**ime **D**igital **S**imulator
PDC	**P**hasor **D**ata **C**oncentrator
GPS	**G**lobal **P**ositioning **S**ystem
LAN	**L**ocal **A**rea **N**etwork
WAN	**W**ide **A**rea **N**etwork
CT	**C**urrent **T**ransformer
PT	**P**otential **T**ransformer
VSLI	**V**oltage **S**tability **L**oad **I**ndex
GUI	**G**raphical **U**ser **I**nterface
WTF	**W**orkstation **I**nterface card
IRC	**I**nter **R**ack **C**ommunication
GTWIF	**G**iga **T**ransceiver **W**orkstation **I**nterface card
GTDI	**G**iga **T**ransceiver **D**igital **I**nput card
GTAO	**G**iga **T**ransceiver **A**nalog **O**utput card
GTAI	**G**iga **T**ransceiver **A**nalog **I**nput card
GTFPI	**G**iga **T**ransceiver **F**ront **P**anel **I**nterface card
GTNET	**G**iga **T**ransceiver **N**etwork **I**nterface card
GTSYNC	**G**iga **T**ransceiver **S**ynchronization card

Chapter 1

Introduction

Electric energy systems are facing many challenges in recent years due to large interconnected complex power system transmission network. To effectively support this challenge, the voltage of transmission systems has to be controlled. As this is the most complex interconnected transmission network ever built by the experts, monitoring and control is an immense challenge. Although the future interconnected systems are drastically expanding therefore optimal placement of the monitoring devices (PMU) must be compulsory not only to optimize cost but also to reduce data redundancy. The interstate and even international integration of power system grids provide many advantages like trading of electrical energy and full utilization of sources but to maintain stability in such a complex network is a great challenge. Some voltage stability index required to predict the future of the buses and to act under any contingences. To achieve the objective, this dissertation deals with the proposed PMU placement technique and real time monitoring of the FVSI by the use of RTDS.

1.1 Objective

The motto of this work is to develop real time simulation to model & simulate FVSI for wide area monitoring of power system as well as to achieve optimal locations of PMUs by considering depth of unobservability and superset constraint. Optimization is done with a constraint of observability, i.e. with minimum number of PMUs maximum observability can be achieved.

1.2 Synchrophasor

The magnitude and phase angle of the sine wave are represented by a complex number called phasor. Phasor measurements that occur simultaneously are called synchrophasors. The terms synchrophasor and PMU can be used interchangeably according to the application but they have different technical meaning. PMU is a metering device whereas the metered value is called synchrophasor. PMUs are given a common time source from a global positioning system (GPS) radio clock for synchronization and sampled from widely dispersed locations in the power system network. The data collected from the various PMUs are concentrated at one unit called phasor data concentrator (PDC) which analyze and classify the data for further processing. So, measurement of state of the electrical system can be done by the synchrophasor technology. These states are voltage, current, phase angles, frequency and rate of change of frequency. PMU measures the electrical waves of the power system network using a common reference signal for synchronization. Multiple real-time remote measurements are synchronized by time synchronization (GPS) on the grid. This type of measurement is called synchrophasor.

1.3 Voltage Stability Monitoring

It is an application that can monitor system voltage in real time, and provide operators with warning in the event that system voltages are nearing or exceeding limits. To validate the purpose, this work deals with the fast voltage stability index and its real time monitoring on RTDS.

1.4 Literature Survey

PMU installed on the bus can able to measure voltage, current, angles, frequency and rate of change of frequency of the PMU-installed bus and the bus which is directly connected to that bus[1]. The synchro phasor devices have high capability of sampling the data at a rate of 20 samples per second[2]. The PMUs placement has been made on the basis of concept of depth of un-observability[3]. Initially, placement of PMU was done using spanning tree of a power system network[4], although it doesn't ensure about lowering the depth of un-observability in every phase and also it does not take care about

the reinstallation or un-installation of the device. A binary search algorithm based optimal placement of PMUs described in [5]focuses on measurement redundancy. Smart grid implementation of PMUs and its optimization using integer linear programming (ILP) described in [6]. The PMU placement based on data redundancy constraint described in [7]. The defined voltage stability index can help in further voltage monitoring of the buses[8].Online monitoring of the voltage stability load index (VSLI) implemented on RTDS[9]. Placement of PMUs has been made on real time digital simulator and is described in the reference [10]. The performance of 8 bus system under fault condition is tested on RTDS[11]. Reference [12] shows the need PMUs in wide area monitoring and control of power system and its real time monitoring. Implementation of two of the line stability indices is described in [13]. Additional information about RTDS is given in reference [14].

The scheme proposed in the present dissertation is modification of the spanning tree technique described in [4]. In this scheme, the placement is done in different phases according to the man power or capital availability. The objective is to lower the depth of unobservability after every consecutive phases and the care must be taken that there won't be any un-installation or shifting of any PMU after every phase i.e. superset concept. Voltage stability index is implemented to monitor the grid. To validate the scheme RTDS has been used. The PMU placement in power system network has been demonstrated on IEEE 14 bus test system. FVSI, in real time environment provides online monitoring of any complex grid network. Real time monitoring of the index will provide extremely dynamic values with very high data rate.

Chapter 2

Phasor Measurement Unit(PMU)

2.1 Introduction

PMU is a measuring device that provides real time phasors of synchronized measurements of voltage, current, phase angle, frequency and rate of change of frequency. Synchronization is done by the use of GPS signal which samples voltage and current waveforms in real time. A PMU installed on a bus can measure the states as stated above of the bus where it is installed. The states of the bus which is directly connected to it can be calculated by Kirchhoff's laws. So, it is clear that PMU can measure the voltage and current of the bus where it is installed and also of the bus which is directly connected to it.

A PMU can measure ac waveforms of voltage and current of 50/60 Hz at a very high sampling rate of 48 samples per second. The conversion of analog ac waveforms to digital can be done by analog to digital converter for each phase. The high speed synchronization can be achieved by phase lock oscillator and GPS signal with an accuracy of 1 micro second. The resultant waveforms can be transmitted to the central processing units (PDC) with sampling rate of 60 samples per second.

The most important part of synchrophasor based monitoring is communication between the PMUs and PMU to PDC. One of the effective communication protocol is Ethernet based local area network (LAN) or wide area network (WAN) i.e., telecommunication network. In some cases fiber optic cables also used for HV transmission lines.

2.2 Applications

Synchronized phasor measurements will lead the wide area monitoring and control system to a new level by the use of PMU. The current and future applications of the PMU are described in the literature. Many countries have already installed a number of PMUs around the world for various major utilities in real time and study mode applications such as:

Real-time Applications:

- Oscillation detection
- Frequency event detection
- Voltage stability monitoring
- Event management, alarm, restoration
- General event detection
- Islanding detection
- Wide area awareness/visibility
- Wide area control

Study Mode Applications:

- Phase angle monitoring
- Model validation and improvement
- Real time load congestion management
- Post-mortem analysis
- System state estimation model improvement
- System protection schemes
- Adaptive protection
- Disturbance propagation monitoring
- Protection for wide area disturbances

2.3 Optimization Constraints

The most important problem regarding to the PMU installation is 'site selection' because of a cost. The overall average cost for procurement, installation and commissioning is approximately $40,000 to 180{,}000$ per PMU. The cost of PMUs is limited by the available communication facilities which may be higher than that of cost of PMU. The increased cost of PMU can be brought down in future by providing flexible communication protocols. By doing that the placement sites are also limited. So, it is a great challenge to place the PMUs on optimal locations and it is an initial step to wide area monitoring system.

Usually PMU placement for system monitoring can be done to get full observability of the network. The concepts such as superset and depth of unobservability are been developed for maximum utilization, minimum cost, minimum data redundancy and full observability. For islanding detection and state estimation, various placement algorithms have been developed. To study PMU placement, various algorithms and placement models are need to be studied. In some system models the locations to install the PMUs are not practical, such as capacitor nodes, tapped line buses and shunt elements as they include virtual buses that might not exist in the network. These buses may increase number of nodes (1/3 more nodes) and so the network will become more complex. This will lead to the placement at unrealistic locations of the PMUs in the network if these nodes are not eliminated. If we eliminate the virtual buses manually then this problem will get solved in small modes. To eliminate virtual buses systematic methods can be developed and the problem will be solved in real system modeling.

Many papers and researches on PMU placement scheme have reported that for complete observability of the network the PMUs need to be installed at least at 1/5 number of system buses and maximum 1/3 number of system buses for medium sized networks.

From the reports it is clear that the PMU placement was done by using spanning tree initially where only optimal locations of the PMUs were been considered. Now, the motto is to reduce number of PMUs in comparison with spanning tree method and also consideration of other important constraints. Based on incomplete observability, a proposed technique of PMU placement is described in this report ensuring depth of unobservability and superset constraints too. The terms incomplete observability, depth of unobservability and superset will be described in the next chapter. The PMU placement scheme guarantees an approximate uniform distribution throughout the power system

network. The depth of unobservability constraint will ensures the distance between the observed and unobserved buses in any complex network. Any problem of un-installation or reinstallation of PMUs are been taken care by the superset constraint.

2.4 PMU Installation

Generally, PMUs are installed and interconnected at substations or at the generation plant. To avoid seismic vibrations, PMU can be bolted on the seismic mounting equipment rack by the substation personnel. Installation of PMUs is a simple process. There are three separate electrical connections are required for each phase as phasor normally of 3 phase voltage or current.

As shown in the Fig. 2.1, the attenuated inputs to the PMU are fed from the current transformer (CT) and potential transformer (PT). Then the PMU along with other communicating equipment and modem will be connected on the equipment rack. As per the instructions given by the manufacturer, global positioning satellite (GPS) antenna will be mounted on the roof of the substation. The other 'shunts' to be measured can also be installed on the secondary side of all the CTs by the substation personnel. The other requirements from the PMU will be a communication circuit connection. This connection is four wire connection if modem is installed or an Ethernet if there is network connection.

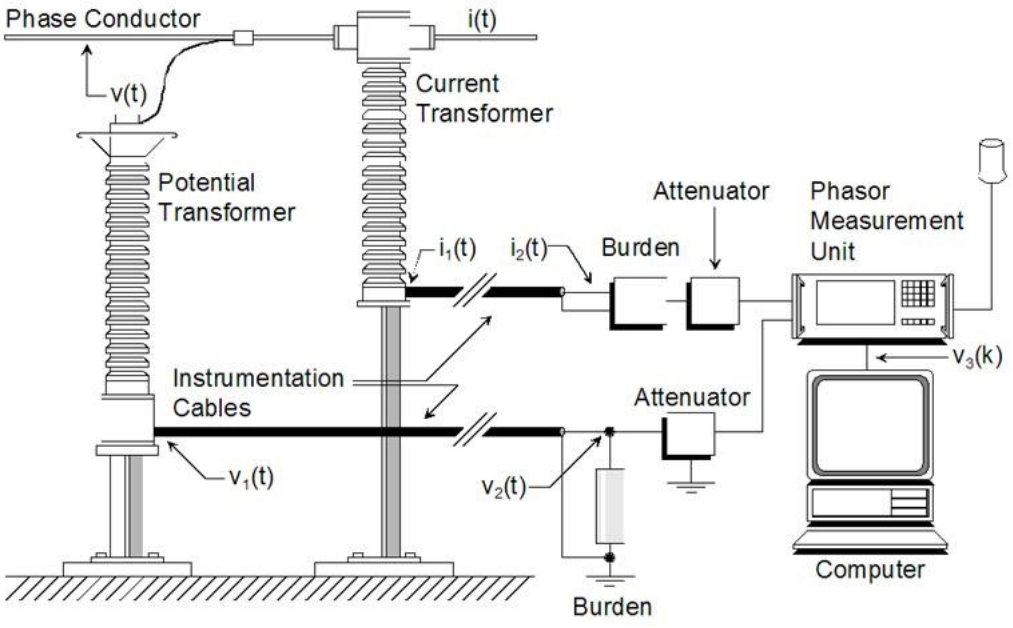

FIGURE 2.1: Connections of PMU

Chapter 3

PMU Placement

Since now PMU placement was done by considering maximum observability as a major constraint only but in the scheme described here, other minor constraints are also going to be considered for ease of placement. Before PMU placement scheme there are certain terms need to be defined to understand the placement technique.

3.1 Incomplete Observability

The term incomplete observability refers to the network in which the number and locations of the monitoring devices are not sufficient to observe complete system. Here in the Fig. 3.1, an example of incomplete observability is shown. In which the bus D is not observable as the PMUs installed at the bus B and F will able to observe only buses B, A, C and F, G, E respectively. Where, the voltages and currents at the buses G, E, C & A can be calculated using simple Ohm's law and Kirchhoff's laws.

The buses where PMUs are placed can be defined as **PMU buses** or **directly measured buses** and the buses which are directly connected to it are defined as **calculated buses** or **observed buses** because their voltages and currents are calculated from the output of the PMU installed buses linked to them. Here in the Fig. 3.1 the buses A, C, E & G are calculated buses whereas the buses B & G are PMU buses where PMU-1 and PMU-2 are installed respectively.

3.2 Depth of Unobservability

The term depth of unobservability refers to the number of unobserved buses of the network. In the Fig. 3.1 & Fig. 3.2 the arrangement of concept of depth of unobservability one and depth of unobservability two are shown respectively. If there is one unobserved bus between the two or more calculated buses then the arrangement is called depth one unobservability and similarly for two, three and so on. In the Fig. 3.1 there is only one bus D is unobserved between the two calculated buses C & E. So this is called depth of one unobservability. Similarly in the Fig. 3.2 buses D & E are unobserved and this type of arrangement is called depth of two unobservability. In such cases where there is an unobserved buses exist, the voltage and current can be estimated by conventional approach.

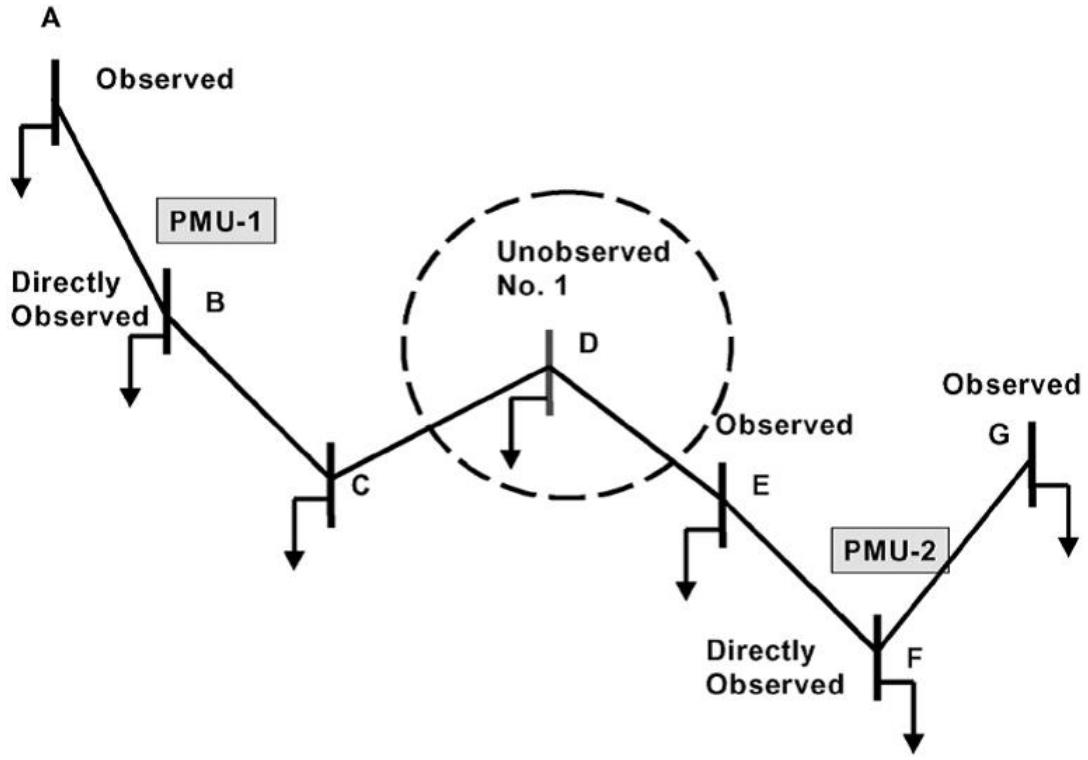

FIGURE 3.1: Depth of One Unobservabiliy

3.3 Optimal PMU Placement Technique

3.3.1 Tree Search Placement Technique

The objective of the technique is a placement of PMU in such a way that the constraints of depth of unobservability described in Fig. 3.1 and Fig. 3.2 are achieved. The described

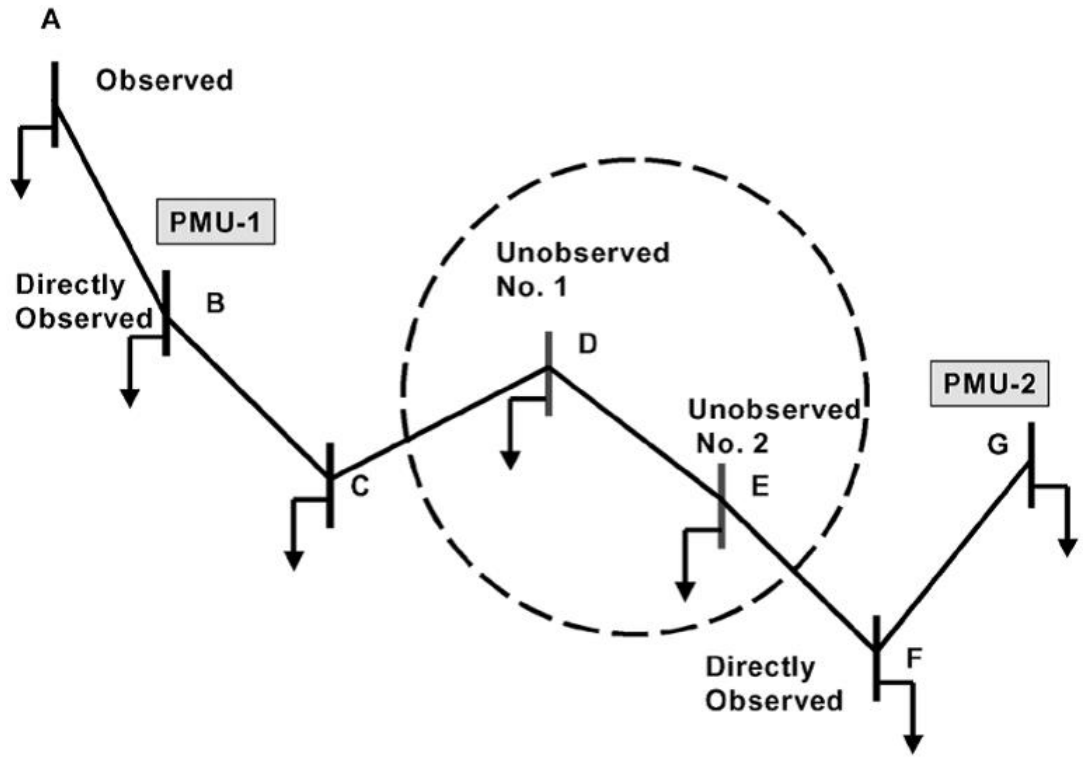

FIGURE 3.2: Depth of Two Unobservability

technique consists of 'series of walks'. The branches of a spanning tree are been traced and the nodes pertaining the branches are tested for the PMU placement locations.

The procedure starts with any node in the network which will then be defined as root node and the node where the search procedure end will be defined as terminal node. So these root nodes can be anyone in the network from where the search procedure start in forward direction but terminal nodes are the nodes from where there won't be any forward path/route. The root node is a starting point of the search procedure and the search goes down the tree up to the terminal node. At the terminal point the search backtracks and searches for another path. The walk can be bus to bus. When the procedure returns to the arbitrarily selected root node it implies the spanning tree has been completely searched then the PMU placement search terminated. After complete procedure, there won't be any unobserved bus in the network or it can be said that this method guarantees complete observability for the parent graph.

3.3.2 Illustration

By the strategy stated above the illustration is presented for the PMU placement in IEEE 14 bus test system. A spanning tree of the network is shown in Fig. 3.3 which comprises 13 branches and 14 nodes extracted from 21 branches and the thin lines indicate co-trees.

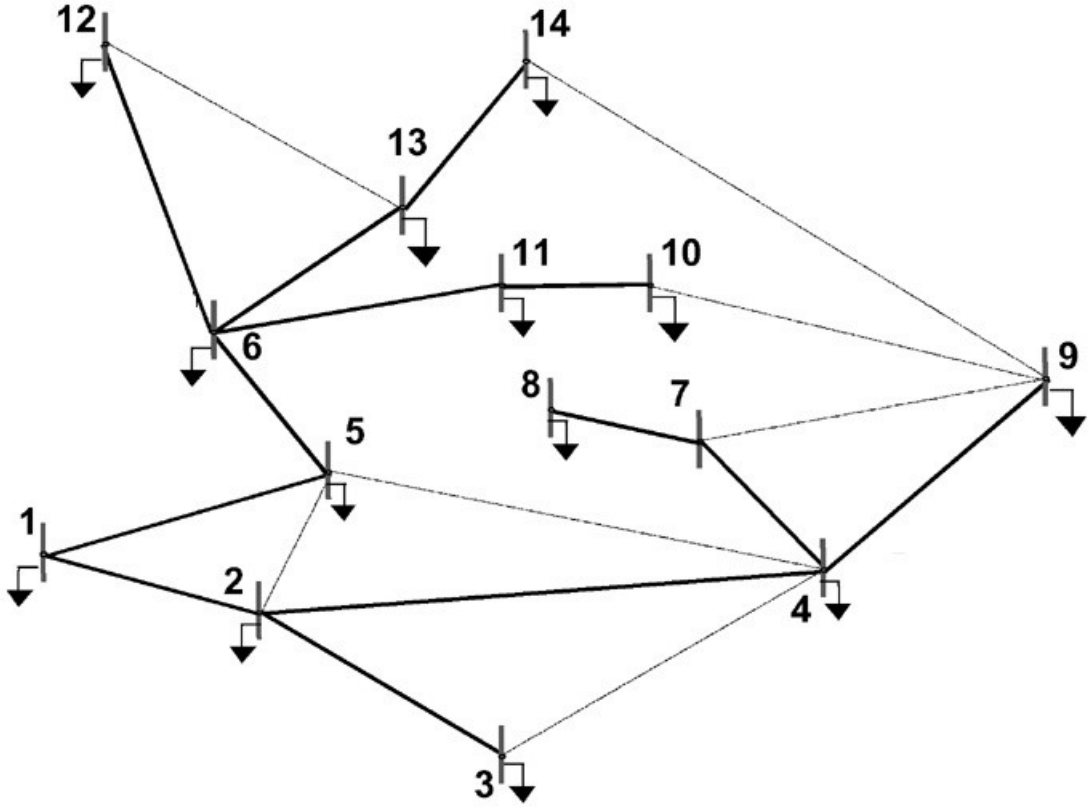

FIGURE 3.3: IEEE 14 Bus Test System

The process can be started from any arbitrarily selected root node, Node 12. The first route defined by the nodal sequence will be $12 \rightarrow 6 \rightarrow 5 \rightarrow 1 \rightarrow 2 \rightarrow 4 \rightarrow 9$. It is obvious that to observe the root node bus, the first PMU can be placed at the bus just after the root node. So, first PMU can be placed at bus 6. By moving in forward direction along a chosen route $6 \rightarrow 5 \rightarrow 1 \rightarrow 2 \rightarrow 4$, each time searching for possible locations of PMUs. To get the depth of one unobservability, the next logical PMU placement can be at bus no. 4. It is clear that PMUs are physically 4 buses separated from each other along the chosen route for depth of one unobservability. The next step will hit the terminal Node 9; it is already observable by placing PMU on Node 4. Now, backtracking to another route that is Node 4 and moving to Node 7 & 8, the Node 7 is already observable.

The next move is also a terminal Node 8. As there is no load at bus 7 and the values of voltages and currents are known of that bus, data for the bus 8 can be calculated. Again

backtracking to the node from where a forward path is possible; the route is Node 8→ Node 7→ Node 4→ Node 2. From Node 2 again by hitting the terminal node; Node 3, from which backtracking all the way back towards the root Node 6 (Node 3→ Node 2 → Node 1→ Node 5→ Node 6). From Node 6 moving in the sequence Node 6→ Node 11→ Node10, Node 10 is an unobserved bus now. Node 10 is already with depth of one observability therefore no need to place PMU here (bus 11 and bus 9 are calculated buses). Now, again by backtracking to Node 6, moving towards Node 13 will hit the terminal Node 14. This terminal node is also at depth of one unobservability therefore no PMU can be placed here (bus 13 and bus9 are observed buses).

The last backtracking towards the Node 6 through 14 → 13 → 6 and moving towards the terminal Node 12, again a terminal can be hit which is already observable by the PMU placed on the bus 6. In IEEE 14 bus test system, PMUs can be placed at bus 6 and bus 4 to achieve depth of one unobservability. This search procedure can also be done by taking another root node to ensure minimum number of PMUs to be placed to get maximum observability.

From procedure it can be concluded that: For a desired depth of unobservability u, the next PMU can be placed at the node j must be at a distance $d_j = u + 3$. In Fig. 3.3, assuming that one PMU is placed at bus 6 at instance k = 1, then the next PMU is placed at instance k = 1 is at $d_3^1 = (v = 1) + 3 = 4$, i.e. at bus 3 to get depth of one unobservability. Similarly, to get depth of two unobservability in the previous case the next PMU will be placed at the new location $d_3^2 = (v = 2) + 3 = 5$, i.e. at bus 4. Where, k defines rank of unobservability. The same technique can also be applied to Fig. 3.1 and Fig. 3.2. It is obvious that after placing one PMU the new set of PMUs can be placed at $S^(k + 1), k = k + 1$.

3.4 Proposed PMU Placement Technique based on Superset Concept

The installation of the PMUs in phases can be mainly based on time (year/month). The purpose behind the phasing is to place the PMUs in such a way that the depth of unobservability in current phase is lower than the previous phase and the already placed PMU can neither be moved to another location nor be uninstalled. Thus, with this incremental placement strategy and by increasing system's regions of observability, finally complete observability of the network can be achieved. A modified view of IEEE 14 bus test system is shown in Fig. 3.4.

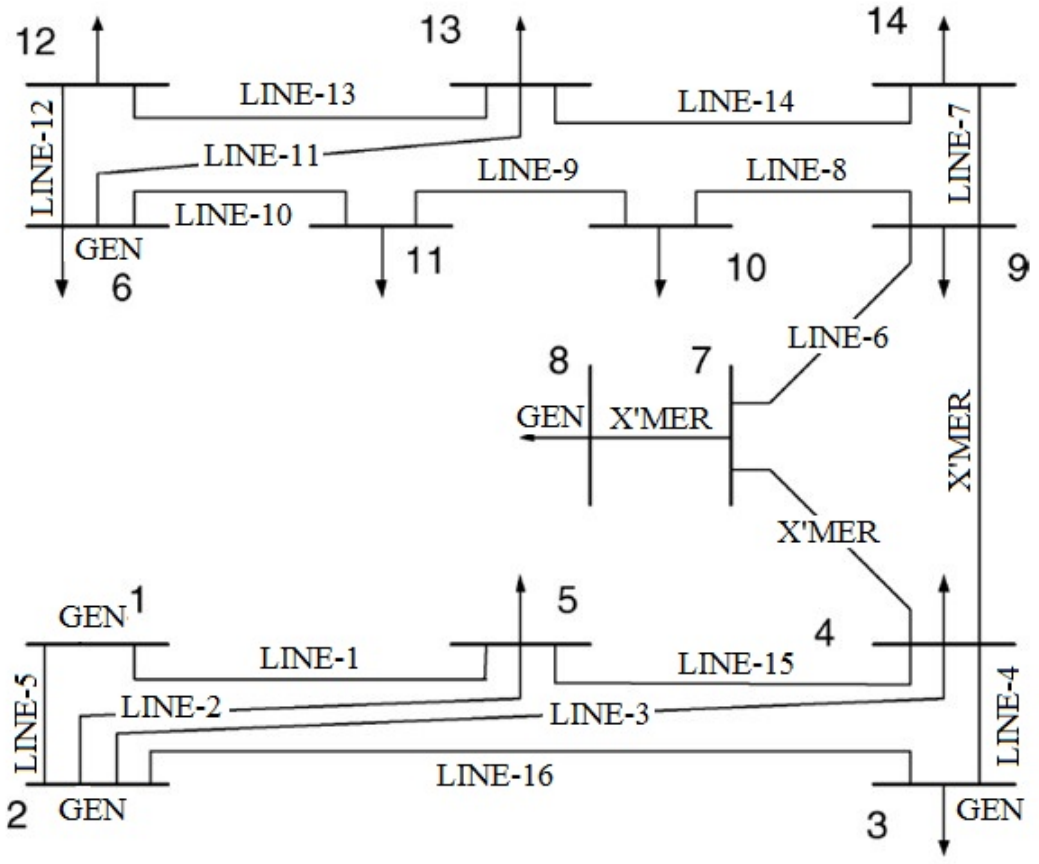

FIGURE 3.4: Modifie View of IEEE 14 Bus Test System[4]

From the Tree Search Placement Technique described in [4], it can be known that by placing PMUs on the four locations 2, 6, 7 & 9, complete system observability can be achieved. Now if the placement be phased over a three-year period with two, one, and one PMUs to be installed in first, second, and third year, respectively, the objective of the placement will be satisfied. To understand the constraints easily, a modified view of IEEE 14 bus test system is implemented as shown in the Fig. 3.4.

Here, v defines the observable buses and x defines the available locations of PMU. The values of the variables v and x can be taken in binary only. i.e.

$v_i \in \{0, 1\}$

$x_i \in \{0, 1\}$

Placement in various phases is as follows:

Phase-I:

To observe maximum number of buses, we define one objective function as follows:

$$max\ v_1 + v_2 + v_3 + \cdots + v_{14} \tag{3.1}$$

PMU can be placed on any of the four buses in Phase-I but we'll consider our objective to be satisfied at the end of placement. Thus,

$$x_2 + x_6 + x_7 + x_9 = 2 \tag{3.2}$$

All other $x_1, x_2, \ldots, x_{14}$ are considered to zeo. Therefore, the governing constraints of the observability for Phase-I can be defined as follows:

$$Bus1 : x_2 \geq v_1 \tag{3.3}$$

$$Bus2 : x_2 \geq v_2 \tag{3.4}$$

$$Bus3 : x_2 \geq v_3 \tag{3.5}$$

$$Bus4 : x_2 + x_7 + x_9 \geq v_4 \tag{3.6}$$

$$Bus5 : x_2 \geq v_5 \tag{3.7}$$

$$Bus6 : x_6 \geq v_6 \tag{3.8}$$

$$Bus7 : x_7 + x_9 \geq v_7 \tag{3.9}$$

$$Bus8 : x_7 \geq v_8 \tag{3.10}$$

$$Bus9 : x_7 + x_9 \geq v_9 \tag{3.11}$$

$$Bus10 : x_9 \geq v_{10} \tag{3.12}$$

$$Bus11 : x_6 \geq v_{11} \tag{3.13}$$

$$Bus12 : x_6 \geq v_{12} \tag{3.14}$$

$$Bus13 : x_6 \geq v_{13} \tag{3.15}$$

$$Bus14 : x_9 \geq v_{14} \tag{3.16}$$

In the above equations, inequality (5) signifies that if no PMU at bus-2 implies $x_2 = 0$, then $v_3 = 0$. So, bus-3 will not be observable. Similarly, inequality (6) signifies that by placing PMU on either location among 2, 7 or 9, bus-4 can be observable. So, the constraints (3)–(16) imply that all the buses of network can be made observable by placing PMU on buses 2,6,7 and 9. By considering the above constraints (1)–(16) and our objective, PMU placement can be done on buses 6 and 9,i.e.,$S_1 = \{6, 9\}$. So, buses 1,2,3,5 and 8 are unobservable at the end of Phase-I. The buses 1 and 2 are with **depth of two unobservability**.

Phase-II:

At the end of Phase-I, buses 4, 6, 7, 9, 10, 11, 12, 13 and 14 can be made observable. Hence, in current phase these busses can't be considered in the objective function; now again to maximize observability of the system for the left over buses, new objective function is defined as follows:

$$max v_1 + v_2 + v_3 + v_5 + v_8 \tag{3.17}$$

As per the second constraint, only one PMU can be placed in this phase among the two buses 2 or 7 can be modelled by the following constraint:

$$x_2 + x_7 = 1 \tag{3.18}$$

By ignoring the satisfied constraints and considering the constraints (17), (18) and (3)-(7) and (9)-(11) leads us to place the PMU on bus 2.

i.e. $S_2 = \{2\}$

After Phase-II only bus 8 is unobservable with **depth of one unobservability**.

Phase-III:

In this phase, the remaining PMUs from the above described set S are placed. We conclude that $S_3 = \{7\}$.

Hence after three phases whole network become observable without shifting or uninstalling any PMU in different phases.

S = {{6,9},{2},{7}}

To enhance the reliability of monitoring and observability of the network, each bus should be monitored by at least more than one PMU. This verifies that in case of any PMU outage, there will not be complete loss of observability. In this method, Bus-4 can be observed by three PMUs, Bus-7 and Bus-9 by two PMUs. Therefore, reliability of monitoring and network observability the system also increased after each phase compared to the method reported in [4].

Chapter 4

Real Time Digital Simulator(RTDS)

4.1 Introduction

The RTDS has been used as simulation platform. RTDS consists of digital signal processors that work on the parallel processing technology and it simply executes the program in runtime software which developed on its processors. The graphical user interface (GUI) software used is RSCAD built in the power system simulated by this power system simulator. It uses a very small time step of just 2 microseconds. Monitoring and control technologies are being developed on the RTDS for testing purpose.

Workstation Interface card (WTF) is used to communicate between the RTDS and workstations. Communication between the racks can be carried out by the Inter-Rack Communication card (IRC). So it is best suited for monitoring purpose because of its real-time operation. Due to the output interface cards incorporated in to its system, this simulator not only measures and displays the electrical quantity in the runtime software, but also produces digital as well as analog output signals. The load ranking, weak bus and voltage stability condition determined as a result for the voltage stability analysis.

FIGURE 4.1: Lab Setup at Electrical Engineering Dept. IIT Roorkee

4.2 Hardware Description

Fig. 5.1 shows the lab setup at Electrical Engineering Department, IIT Roorkee. The installed RTDS consists of six racks. Each rack consists of three Giga Processor Cards (GPCs) and three PB5 Cards for processing required computations in real time. Other components include:

a) One Giga Transceiver Workstation Interface Card (GTWIF) – To interface RSCAD user software with GPC cards of the RTDS;

b) Three Giga Transceiver Digital Input Card (GTDI) – To take digital input signals from external devices such as PMU or Relays; c) One Giga Transceiver Front Panel Interface card (GTFPI) –To take digital input signals from hardware devices like relays and to give digital output signals to the hardware devices;

d) Three Giga Transceiver Analog Output Card (GTAO) – To provide analog output signals to hardware devices like PMUs for measuring electrical quantities;

e) One Giga Transceiver Analog Input Card (GTAI) – To take analog input signals from hardware devices;

f) One Giga Transceiver Network Interface Card (GTNET) – To interface a number of different network protocols with the RTDS simulator; and

g) One Giga Transceiver Synchronization Card (GTSYNC) – To synchronize the RTDS simulation time step to an external time reference like the GPS clock. Additionally, test bed consists of number of PMU devices, phasor data concentrators (PDCs), synchrophasor vector processors (SVP), controllers, and amplifiers.

The synchronous phasor measurements are collected by the synchrophasor vector processor. SVP collects SPMs from both the ends of the transmission line, compare the voltage angles and issues a warning signal to an operator if a threshold has been exceeded. SVP can also collect logical inputs, perform vector and scalar calculations, make decisions, produce outputs and report the data. The primary tools used in this work are RTDS, PMUs and GPS clock. In that, the PMUs obtain their wide area measurements from the RTDS and the SVP runs the wide area control algorithm to implement the remedial action schemes for transient stability.

4.3 Features of RTDS

RSCAD is advanced user friendly graphical user interface software used in RTDS. There are some steps/modules need to be performed in the RTDS for successfully compiling and running simulations and for analysing output of the simulation. All these modules are quite easy to understand to a power system engineer and the simulator is provided with a user friendly graphical interface. These RSCAD modules are as follows:

a) FileManager: RSCAD/FileManager module organizes and shares the cases and simulation projects. The provision is given in the permission settings of RSCAD that the same user or multiple users can access the cases and simulation files according to the communication protocol available such as LAN/Wi-Fi. Other modules can be launched from the FileManager and also history files, hardware manuals, tutorials are available in this module. One administrator directory is available in this module that contains all saved cases of RSCAD.

b) Draft: In the RSCAD/Draft module user can design a schematic diagram of the system model to be simulated. A graphical interfacing is available in this module. In the right hand side panel of the screen a tool box is available which contains power system, control system, protection & control and generator controls libraries. To design a real

power system network, the tools and some readymade boxes available in this toolbox. Designing is very simple and user-friendly; the icons, schematics are copied from the tool box and pasted on the left side of the Draft space. The resolution of this blank space canvas can be adjusted according to the complexity of the network. The models available in the tool box can be customized according to the system requirements from the menu window. For further ease of arrangement of the model and faster access, features like group/ungroup, mirror, rotate, cut, copy , edit commands are available. The description of component can also viewed by right clicking on the model. Compilation is done when the circuit is completely designed. If there is any error in the circuit models or designing, compiler will indicate it otherwise it will create an execution code for further hardware simulation and show successfully compiled. Load flow can also be done in this module. Single line diagram mode and other additional features of Draft module are described below.

c) RunTime: In the RSCAD/RunTime module all controlling actions of simulation can be done and also loading can be set in this module. Since it directly interfaced with real time simulation, it is also called as operator's console. The RunTime canvas is also designed for various simulation circuits by designing plots, meters dials, sliders, switches etc. In this module user can able to interact directly to the simulation by a graphical interface. So, controlling can be done precisely. Similar to the Draft, grouping/ungrouping can be done for ease of arrangement on the canvas. By just clicking stop and restarting the run, an updated plots and simulation can be run. Plot calculation is also done in the functions. According to the requirements in the result and discussion, text, notations, signals or time stamps can be noted to the document simulation results. Data of the plot can be saved for further use and it can be processed again in the function called MultiPlot. Print out of the report can be made directly from this module. The whole canvas/plots can be saved in different formats like PDF, COMTRADE, EMF, JPEG or MultiPlot format.

d) TLine: Actual R, L, C data of AC and DC transmission lines is entered by the Bergeron (RLC data entry) function available in the RSCAD/TLine module. It can be in pu or actual values. This data can be converted into a usable form in the circuit module. Line length, ground resistivity and frequency can be fixed first and the Bergeron or frequency dependent travelling wave models data can also be calculated. Impedance can be calculated by knowing the values of positive sequence series resistance, positive sequence series inductive reactance and positive sequence shunt capacitive reactance.

e) Cable: This module is similar to RSCAD/TLine module Instead of transmission line data, cable data of Bergeron or Frequency data are been entered in this module RSCAD/Cable.

f) CBuilder: The best module available in the RSCAD which allows user to customize or design the components available in the simulator and run them on RTDS simulator. By the use of the ANSI C code, RSCAD/CBuilder can able to design own component by drawing icons and input/output nodes. A customized model or component can be used according to the different requirement of the user.

g) MultiPlot: In RSCAD/MultiPlot module printing of captured results and post processing analysis from the RTDS simulator is done. The plotting functions are available and also data analysis, data conditioning are done in this module. Interfacing with other software like MATLAB, MathCAD, Excel etc. can be done by exporting the data by MultiPlot for post processing.

4.4 Implementation of PMU on RTDS

PMUs utilized in this dissertation use a standard synchrophasor measurement protocol IEEE C37.118.1 and also perform power system monitoring, protection and control. The time stamping can be enabled in the power system data by providing satellite synchronized clocks to obtain GPS timing signals to the PMUs. The major elements of the latest PMU are a GPS receiver, an anti-aliasing filter, a phase locked oscillator, an analog to digital converter and a processor to calculate the phasors. In this work the PMUs are been utilized as its major application to generate synchrophasor measurements.

Phase locked loop is utilized to track the frequency and sample time adjustments. Discrete Fourier Transform (DFT) is used to model the PMU and run on RTDS. One GTNET card can able to support eight PMUs and it can stream the data from them simultaneously. Additional, more than 8, PMUs can be utilized by implementing more number of GTNET cards in the simulation. This is a major application of RTDS for wide area measurement system (WAMS). Input signal can be processed in the PMU as shown in the Fig. 5.2

Simulation data can be sampled by a common sample rate and the time reference is provided by the GTNET card. The quadrature oscillator performs complex multiplication functions at nominal frequency. The low pass filter used is finite impulse response (FIR)

type that eliminates the dual frequency component from the signal. So, only real and imaginary parts are left in the original input signal. Two types of filters are used mainly; one is Protection class (P class) and Metering class (M class). Symmetrical FIR filters are used to implement low pass filters of class P & M. The co-efficients of M class filter are determined by multiplication of Hamming window with windowed sinc function and a triangular window is used to calculate P class filter co-efficients. To introduce group delay in the LP filter, every sample is compensated and time-stamped. When center windowed time stamping is used, no further phase correction required as the centre phasor estimation window is unbiased. At nominal frequency 50/60 Hz, sampling is done at a rate of 15 samples per cycle and 16 samples per cycle for P and M class filters.

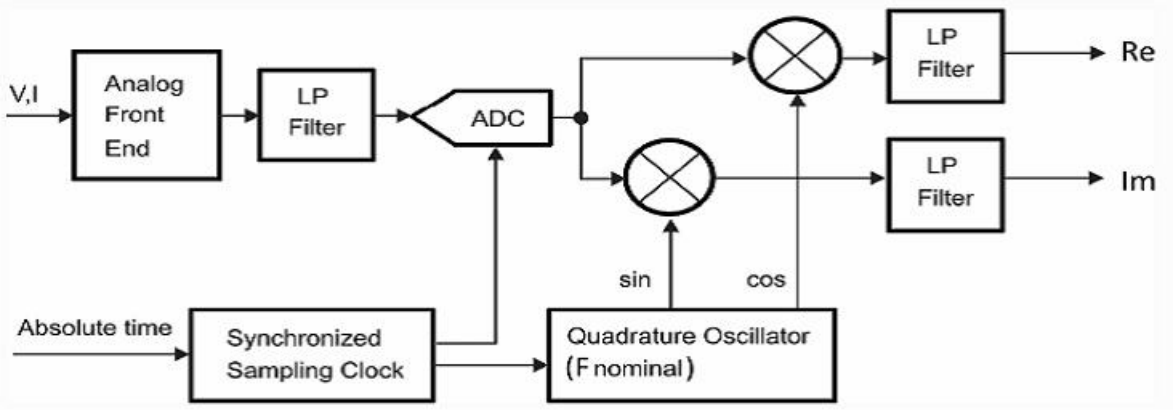

FIGURE 4.2: Building Blocks of PMU

From the block diagram shown in the Fig. 5.2 the reference model can be understood well but RTDS implementation need some other changes for modeling. Interpolation of quadrature oscillator and data are done because the sampling rate of PMU may be a fraction of time-step. The maximum latency is 2 per Fs and 5 per Fs for P and M class filters respectively. Reporting rate is given as Fs. So, the LP filters are designed with limited latency which is less than maximum allowable standard delay. The order of these filters is large at low reporting rates. It may even exceed the available RAM. An M class PMU with reporting rate of 10 Fs and nominal frequency of 50 Hz requires a filter of very high order 700. The variables required for implementing just one PMU are 12,618. For one GTNET card containing 8 PMUs, this number will be 100,944. So, at lowest nominal frequency 50 Hz the reporting rate is 10 Fs and it leads to exceed the available RAM as length of the window is large.

Filter parameters for very high reporting rates of 100 to 200 Fs can't be provided by the basic model. This very high processing is done on PB5 cards of the RTDS and this format is defined in IEEE standard. Although PMUs implemented on RTDS gives the

data independently but if there are 8 PMUs utilized for operation, it may be require taking all the outputs simultaneously. An interrupt flag is set when PMU is ready to send the data to GTNET card and once it sent this flag is cleared.

Earlier the protocols used for synchrophasor measurements are IEEE 1344-1995 and IEEE C37.118-2005. The new protocol IEEE C37.118.1-2011 was introduced in 2011. To expect further improvements the new standard invented is IEEE/IEC 60255-118-1.

Chapter 5

Fast Voltage Stability Index(FVSI)

5.1 Index Formulation

Voltage stability indices generally used to predict the stability of the buses or lines just as a measuring instrument. Generally, stability indices are of two types:

I. Line Stability Index

II. Bus Stability Index

The index used in this work will be of Line stability type. There are many indices formulated to perform this task. In this dissertation, one basic, simple and less complex mathematical formulated index will be derived and implemented for ease of computation. The index can be made or maintained below 1.00 to achieve voltage stability of the grid. If the index goes near to 1.00 then it signifies that the particular line is critical about stability and if it exceeds 1.00 then that particular line is unstable. This leads to instability in other lines too.

5.2 Derivation of FVSI

Generally, the voltage or power quadratic equations start with the equation of current. If the roots of voltage or power equations are greater than zero then the system is stable. If it violates the criteria, the roots become imaginary. Imaginary roots signify instability in the system and that may cause the whole system collapse. Ultimately, index close to 1.00 indicate instability in the voltage and that particular line is going to collapse or the corresponding buses to that particular line are unstable.

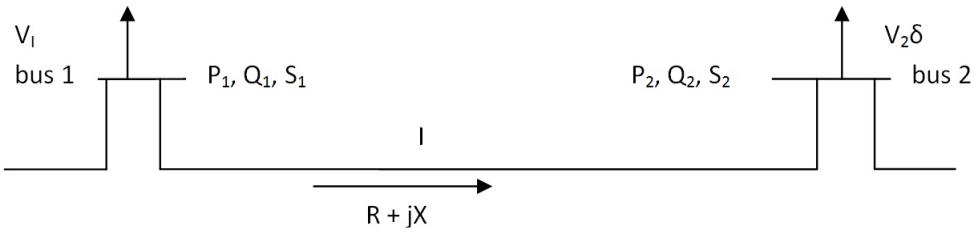

FIGURE 5.1: Two Bus Power System Network

In the Fig. 4.1 simple two bus transmission network is shown with indicated power flow. FVSI will be derived for the two bus network with notations as follows:

V_1 = Sending-end Voltage

V_2 = Receiving-end Voltage

P_1 = Sending-end Active power

P_2 = Receiving-end Active power

Q_1 = Sending-end Reactive power

Q_21 = Receiving-end Reactive power

$S_1 = P_1 + jQ_1$ = Sending-end Apparent power

$S_2 = P_2 + jQ_2$ = Receiving-end Apparent power

$\delta = \delta_1 - \delta_2$ = Difference between the angles of Sending and receiving end Buses

The line impedance is given by, Z = R + jX And the Current through the line is given by,

$$I = \frac{V_1\angle 0 - V_2\angle\delta}{R + jX} \tag{5.1}$$

Sending end apparent power is taken as reference therefore the angle of sending end voltage is taken 0 and receiving end voltage angle as δ. So, apparent power at bus 2 can be defined as;

$$S_2 = V_2 I^* \tag{5.2}$$

where, $I^* = \dfrac{V_1\angle 0 + V_2\angle\delta}{R + jX}$

Equation 5.2 can be written as;

$$I = (\frac{S_2}{V_2})^* = \frac{P_2 - jQ_2}{V_2\angle -\delta} \tag{5.3}$$

From Equation 4.1 and 4.3;

$$\frac{V_1\angle 0 - V_2\angle\delta}{R + jX} = \frac{P_2 - jQ_2}{V_2\angle -\delta}$$

$$V_1 V_2\angle -\delta - V_2^2\angle 0 = (R + jX)(P_2 - jQ_2) \tag{5.4}$$

By separating real and imaginary parts in the above equation yields;

$$V_1 V_2 cos\delta - V_2^2 = RP_2 + XQ_2 \tag{5.5}$$

And,

$$-V_1 V_2 sin\delta = XP_2 + RQ_2 \tag{5.6}$$

By taking value of P_2 from equation 4.6 and substituting into 4.3 yields a quadratic equation of V_2;

$$V_2^2 - (\frac{R}{X} sin\delta + cos\delta)V_1 V_2 + (X + \frac{R_2^2}{X})Q_2 = 0 \tag{5.7}$$

The roots of V_2 will be;

$$V_2 = \frac{(\frac{R}{X}sin\delta + cos\delta)V_1 \pm \sqrt{[(\frac{R}{X}sin\delta + cos\delta)V_1]^2 - 4(X + \frac{R^2}{X})Q_2}}{2} \tag{5.8}$$

If the discriminant is greater than or equal to zero then the roots of V_2 will be real, i.e.

$[(\frac{R}{X}sin\delta + cos\delta)V_1]^2 - 4(X + \frac{R^2}{X})Q_2 \geq 0$

$$\frac{4Z^2Q_2X}{(V_1)^2(Rsin\delta + Xcos\delta)^2} \leq 1 \tag{5.9}$$

Generally δ is very small so,

$\delta \approx 0, Rsin\delta \approx 0, and X cos\delta \approx X$

Hence, the fast voltage stability index can be defined as follows:

$$FVSI_{ij} = \frac{4Z^2Q_j}{V_i^2X} \tag{5.10}$$

where:

Z = Line Impedance

X = Line Reactance

Q_j = Receiving-end Reactive Power

V_i = Sending-end Voltage

Here, i and j represent sending and receiving buses respectively.

5.3 Implementation of FVSI on RTDS

The evaluated value of FVSI that close to 1.00 indicates that the buses correspond to that particular line are going to collapse which may lead to the whole grid collapse. To maintain a safe condition, the value of FVSI should be maintained below 1.00. The FVSIs for all the lines have been determined successfully using RTDS.

The determination of FVSI for line between bus 1 and bus 5 is shown in Fig. 4.2. The reactive power Q1n5 can be positive or negative according to power delivered or absorbed

by the line. But an index can never be negative so modulus of Q1n5 is taken. Then the reactive power will be multiplied with the remaining term $(4Z^2)/X$. The dynamic values of 3 phase voltage can be taken as an output from the 3 phase voltmeter. By taking square of it and its inverse will be multiplied with the remaining term as shown in the Fig. 4.2.

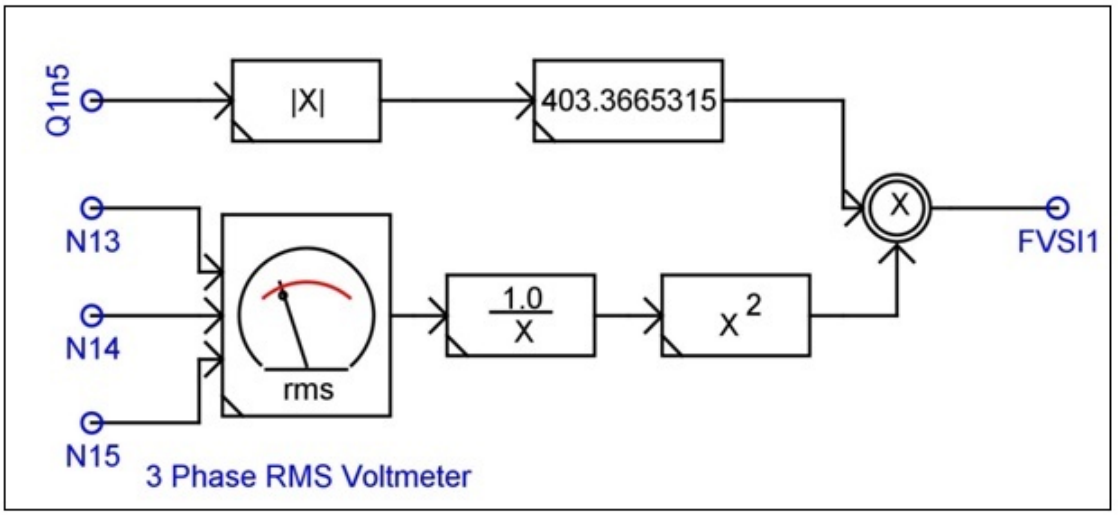

FIGURE 5.2: One of the FVSI modelled in RTDS

where:

$Q1n5$: Receiving-end Reactive power at Bus-1

$N13, 14, 15$: Sending-end Node voltage of Bus-5

The length of transmission line is taken 100 km. By applying the standard values of resistance, reactance and line charge from the IEEE 14 bus test system,

$R = 0.0285k\Omega$ = Resistance of Line

$X = X_L - X_C = 0.0919k\Omega$ = Reactance of Line

$Z = \sqrt{R^2 + X^2} = 0.403k\Omega$= Impedance of Line

$$\frac{4Z^2}{X} = 403.366\Omega$$

Similarly, all other indices of the system are determined. The numbering of FVSIs are according to line numbers described in Fig. 3.4. Further details about RTDS will be given in the next chapter.

Chapter 6

Simulation, Results and Discussion

6.1 Simulation of Two Bus System

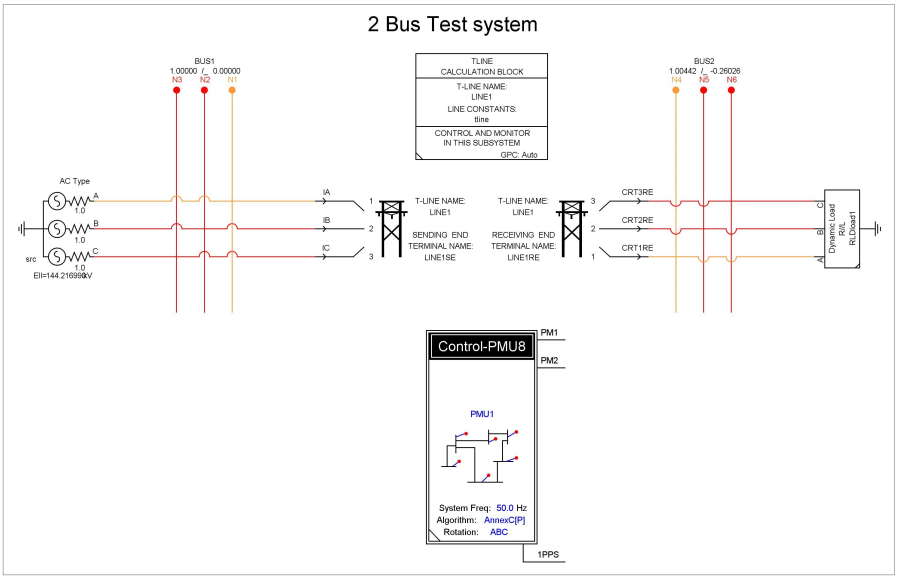

FIGURE 6.1: A Two Bus Power System Network Simulated on RTDS

In above Fig. 6.1, a simple two bus system network with dynamic load connected to 2nd bus is implemented on RTDS for basic understanding of the RSCAD. By varying the load using Slider, we can monitor the changes in the voltage and current of the buses.

A control PMU8 block available in the RTDS is shown in the design module. PMU is placed on both the buses gives voltage, current and frequency as shown in the results.

Base voltage: 230.004496 kV

P_{max} : 100 MW

Q_{max} : 50 MVAR

Initial phase angle: 0.044155 deg

Base Frequency: 60 Hz

6.1.1 Results

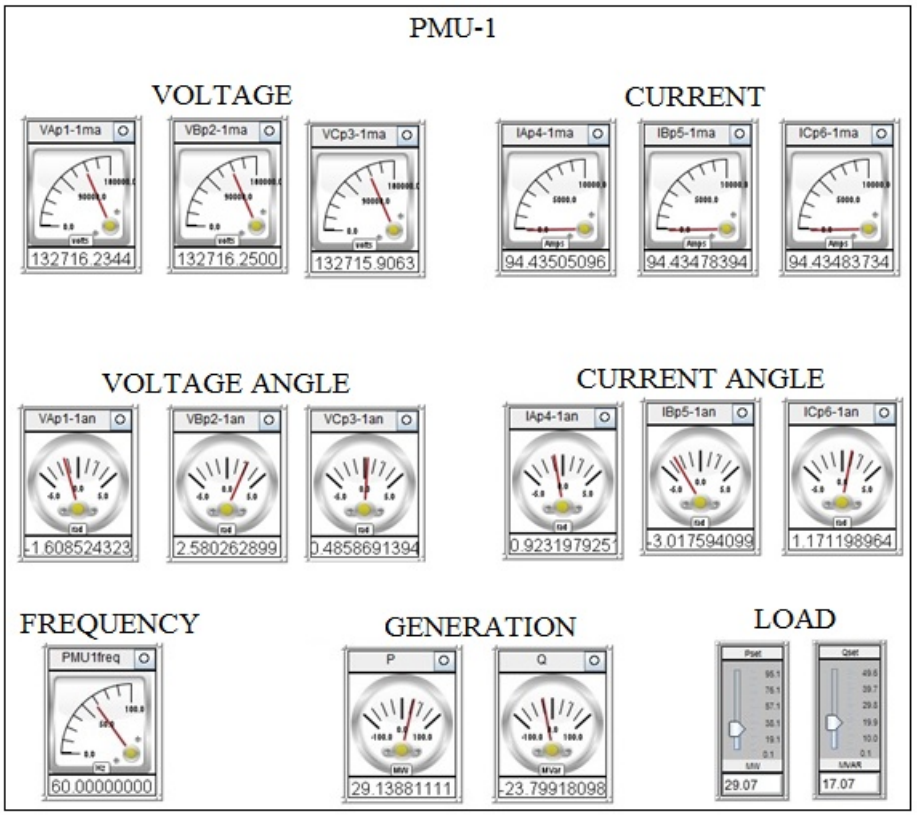

FIGURE 6.2: Measurements from PMU-1

In Fig. 6.2 the results from PMU-1 with amount of active & reactive power generation and set load values are shown. The nomenclature is as below:

The first letter states Quantity(Voltage/Current/Frequency/Power), Second letter with subscript is for phase, third is for Node Number, the letters after dash states PMU number and last two letters are for magnitude or angle.E.g. VAp1-1ma: Voltage magnitude of Bus-1 phase-A Node N1 given by PMU-1. By using slider, we can change the values of dynamic load. Initially the set values of P and Q are:

P_{set} : 29.07 MW

Q_{set} : 17.07 MVAR

V_c of 1^{st} & 2^{nd} Bus: 132.716 kV, 132.901 kV

I_c of 1^{st} & 2^{nd} Bus: 94.435 A, 84.546 A

Multiple outputs of PMU-1 shown in the Fig. 6.2 states steady voltages because RTDS is configured such that if the value of voltage goes beyond specified limit it will show red indication. A negative value of phase-A voltage angle in radians states power is flowing from bus-2 to bus-1 in that phase. No deviation in the frequency can be seen. Similarly, negative value of reactive power shows reverse flow of power. Provision is given in RTDS to vary the load demands by dynamic load. By the use of nomenclatures specified on the head of a title as a node, it is possible to process the data further.

6.2 Simulation of IEEE 14 Bus Test System

A three-phase view of hardware simulation of IEEE 14 bus test system in RTDS is shown in the Fig. 6.3 below. Reference model is shown in Fig. 3.4 and the data is taken from the IEEE standard test system. A Draft model on the canvas of RSCAD has been created by the use of the functions and modules described previously. The default values are:

Base voltage: 230.004496 kV

Base MVA: 100 MVA

P_{max} : 1000 MW

Q_{max} : 1000 MVAR

Initial phase angle: 1.1594143 deg

Base Frequency: 50 Hz

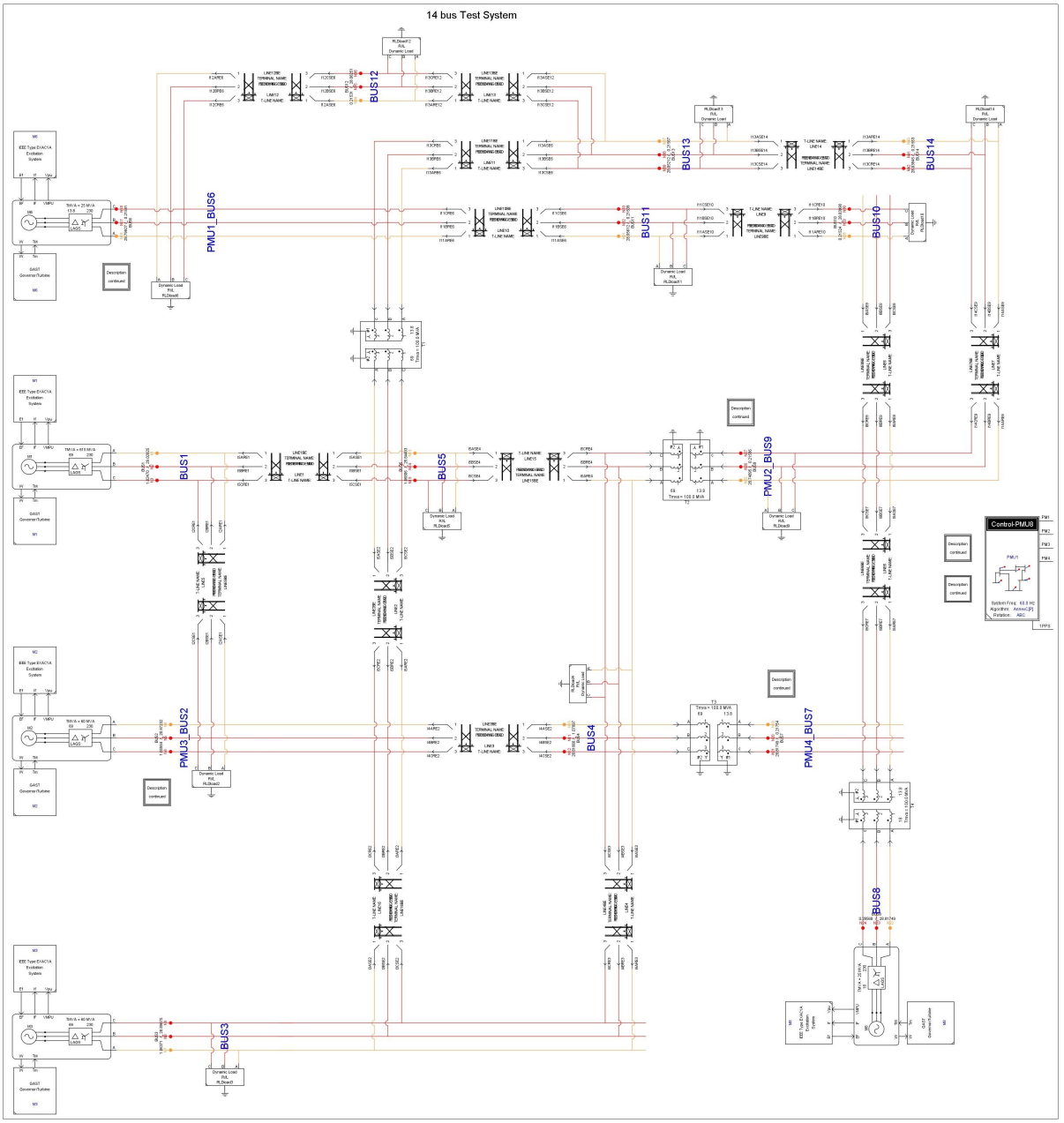

FIGURE 6.3: IEEE 14 Bus Test System Implemented on RTDS

6.2.1 Synchronous Condenser

The provision is given in the RSCAD to make the synchronous generators work as synchronous condenser. To do so, active power output of a generator can be made zero by controlling the turbine speed. Here, in the Fig. 6.4 below; active power of the generators 3, 6 and 8 can be made zero by adjusting slider in Runtime.

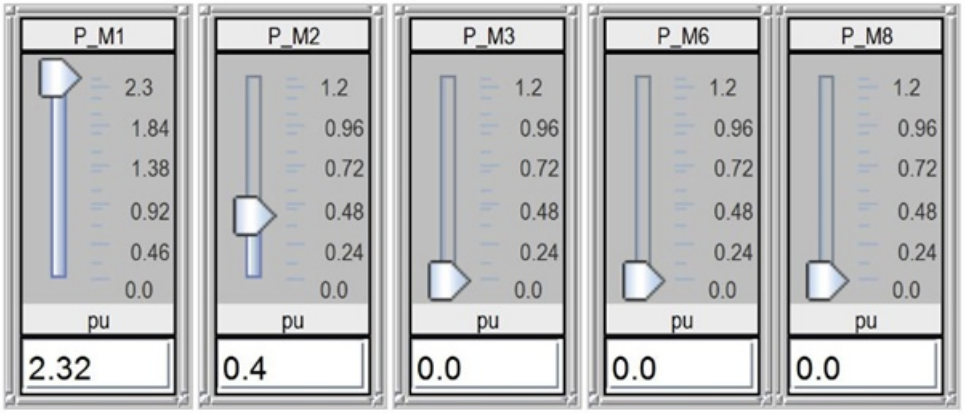

FIGURE 6.4: Generator Active Power Control

6.2.2 Transmission Line

The network contains 14 buses with 2 generators, 3 synchronous condensers, 4 transformers, 11 load buses with 16 inter-connected transmission lines. Description blocks in the above figure will be described one by one later.

The transmission line data can be entered in the RSCAD/TLine module. Where, the length of transmission line is taken 100km and the ground resistivity as 100 $\Omega - m$. The given standard IEEE 14 bus data of R, L, C, X_L & X_C for the transmission line-1 between Bus-1 & Bus-5 are entered as shown in the Fig. 6.5 below:

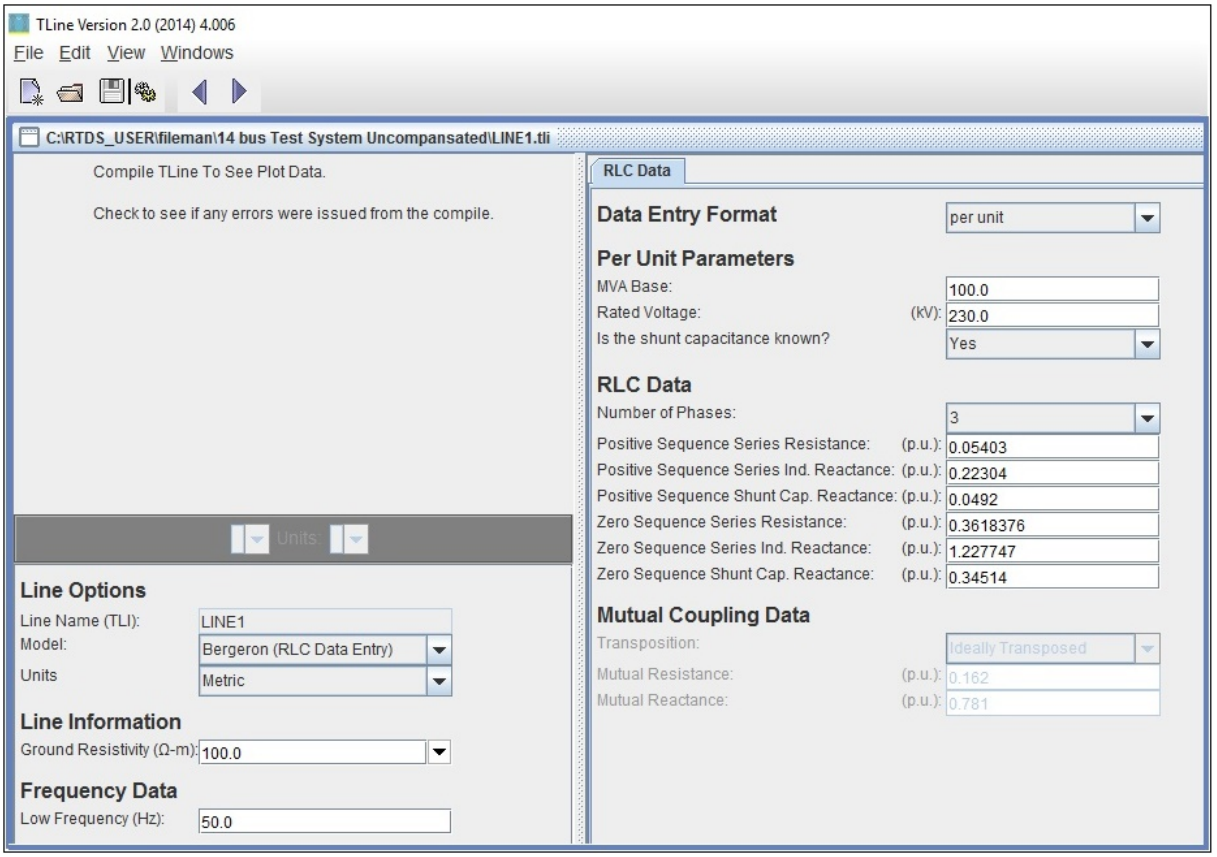

FIGURE 6.5: One of the Transmission Line modelled in RSCAD

The impedance of the line can be calculated from the above data manually by the equation,

$$Z = \sqrt{R^2 + (X_L - X_C)^2}$$

where:

R = Series Resistance

L = Series Inductance

C = Shunt Capacitance

$X_L = 2\pi f L$ = Series Inductive reactance

$X_C = \frac{1}{2\pi f C}$ = Shunt Capacitive reactance

f = System frequency = 50 Hz

Note: Only positive sequence data are taken for calculating the impedance.

6.2.3 Implementation PMU on RTDS

The **configuration of the PMU** placed on the buses 6, 9, 2 and 7 are shown in the Fig. 6.6 below:

_rtds_GTNET_PMU_v4.def

PMU4 CONFIG | PMU1-8 CALIBRATION | PMU1-8 AC SOURCE

CONFIGURATION | PMU1 CONFIG | PMU2 CONFIG | PMU3 CONFIG

Name	Description	Value	Unit	Min	Max
rVT1	PMU1_Turns Ratio : 1	2000.0		1.0	10000.0
nVTA1	PMU1_A phase Input Signal Name	N16		0	0
nVTB1	PMU1_B phase Input Signal Name	N17		0	0
nVTC1	PMU1_C phase Input Signal Name	N18		0	0
rCT1	PMU1_Turns Ratio : 1	600.0		1.0	5000.0
nCTA1	PMU1_A phase Input Signal Name	IPMU1A		0	0
nCTB1	PMU1_B phase Input Signal Name	IPMU1B		0	0
nCTC1	PMU1_C phase Input Signal Name	IPMU1C		0	0
rVT2	PMU2_Turns Ratio : 1	2000.0		1.0	10000.0
nVTA2	PMU2_A phase Input Signal Name	N25		0	0
nVTB2	PMU2_B phase Input Signal Name	N26		0	0
nVTC2	PMU2_C phase Input Signal Name	N27		0	0
rCT2	PMU2_Turns Ratio : 1	600.0		1.0	5000.0
nCTA2	PMU2_A phase Input Signal Name	IPMU2A		0	0
nCTB2	PMU2_B phase Input Signal Name	IPMU2B		0	0
nCTC2	PMU2_C phase Input Signal Name	IPMU2C		0	0
rVT3	PMU3_Turns Ratio : 1	2000.0		1.0	10000.0
nVTA3	PMU3_A phase Input Signal Name	N4		0	0
nVTB3	PMU3_B phase Input Signal Name	N5		0	0
nVTC3	PMU3_C phase Input Signal Name	N6		0	0
rCT3	PMU3_Turns Ratio : 1	600.0		1.0	5000.0
nCTA3	PMU3_A phase Input Signal Name	IPMU3A		0	0
nCTB3	PMU3_B phase Input Signal Name	IPMU3B		0	0
nCTC3	PMU3_C phase Input Signal Name	IPMU3C		0	0
rVT4	PMU4_Turns Ratio : 1	2000.0		1.0	10000.0
nVTA4	PMU4_A phase Input Signal Name	N19		0	0
nVTB4	PMU4_B phase Input Signal Name	N20		0	0
nVTC4	PMU4_C phase Input Signal Name	N21		0	0
rCT4	PMU4_Turns Ratio : 1	600.0		1.0	5000.0
nCTA4	PMU4_A phase Input Signal Name	IPMU4A		0	0
nCTB4	PMU4_B phase Input Signal Name	IPMU4B		0	0
nCTC4	PMU4_C phase Input Signal Name	IPMU4C		0	0

Update | Cancel | Cancel All

FIGURE 6.6: Configuration of PMU

Where, N16, N17, N18 states the node voltage of the bus-6. Similarly other PMUs are configured. The configuration for the current will be described later. The name IPMU1A signifies phase-A current input of PMU-1.

The voltage nodes are given a unique name in the RSCAD but the **current inputs** to the PMU can't be specified in PMU block. So, an arrangement can be made manually

for the current inputs to the PMUs designed in one of the description blocks. Inputs to the PMU-1 are as shown in the Fig. 6.7 below:

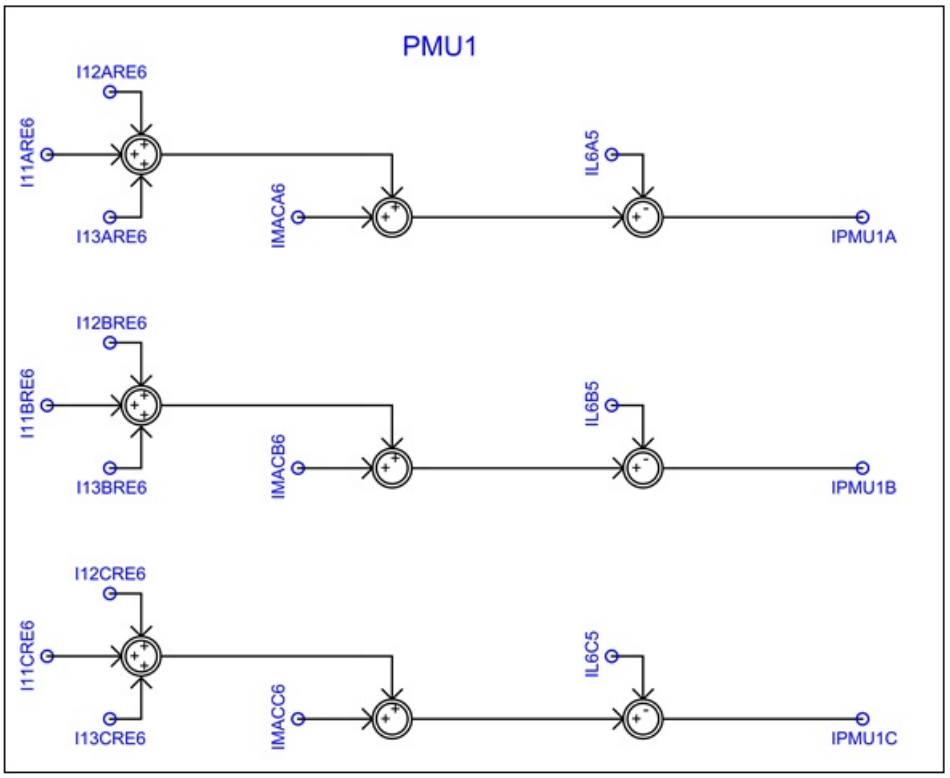

FIGURE 6.7: PMU Input Controls

where:

I12ARE6: Phase-A current flowing from Bus-12 to Bus-6

IMACA6: Phase-A current flowing from Transformer-1 to Bus-6

IL6A5: Phase-A current flowing from Bus-6 to Load-6

Similar standard notations used for other PMUs installed on buses 9, 2 and 7. E.g. in I12ARE6, I stands for current, the next one/two digits defines bus number, RE stands for receiving end and the last one/two digits for bus number. Similarly, MAC for transformer, L for load and other standard notations are used prescribed in RSCAD. A, B and C specifies the different phases of the transmission line.

6.2.4 Single Line Diagram View

For better view and easy understanding of the complex circuitry, the single line diagram of the IEEE 14 bus test system is shown in the Fig. 6.8 below:

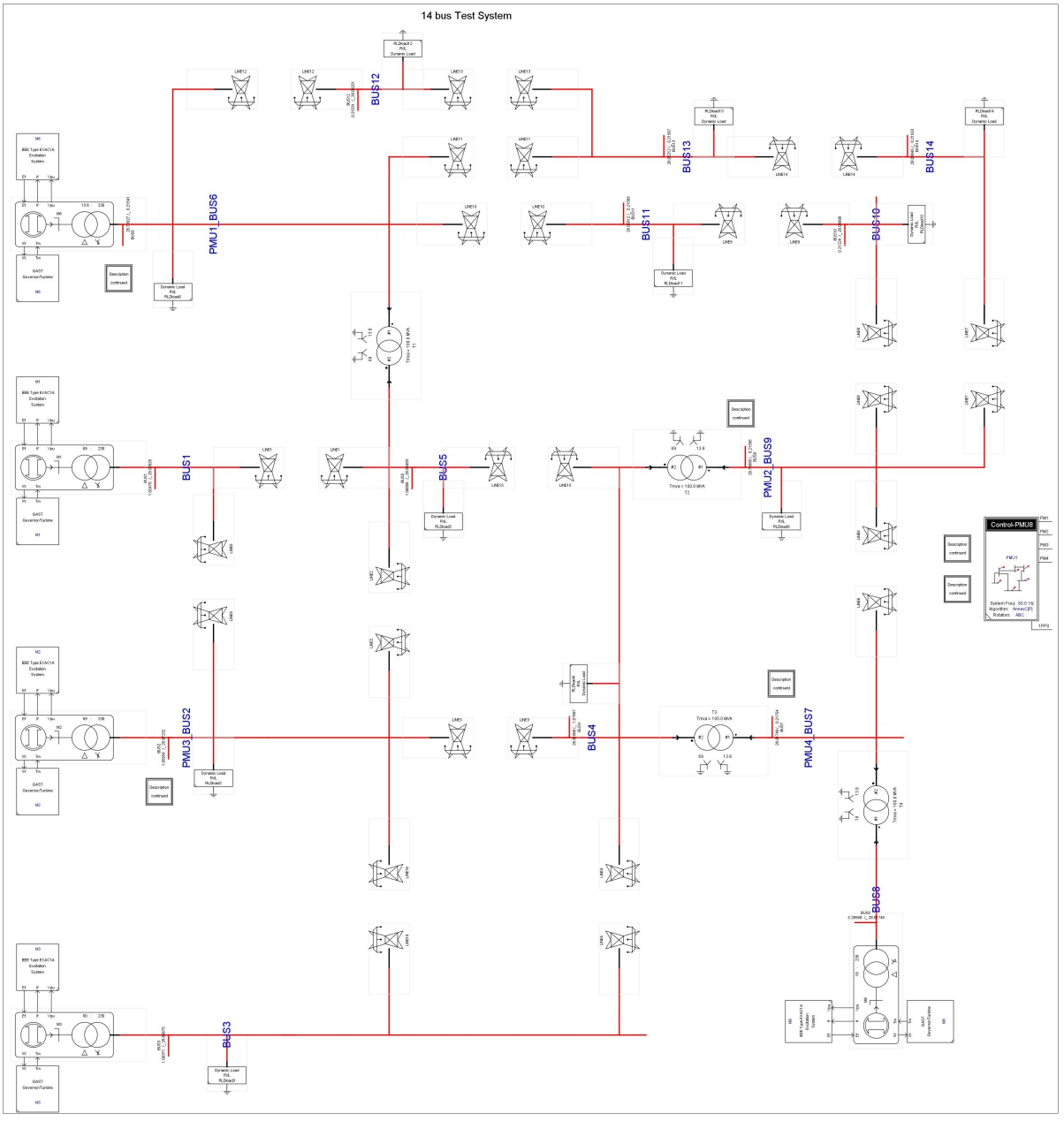

FIGURE 6.8: 1-Phase View of IEEE 14 Bus Test System on RTDS

6.2.5 Results

6.2.5.1 PMU Outputs

The outputs of the PMU placed on buses 6, 9, 2 and 7 with the notations described as before are shown in the Fig. 6.9 below:

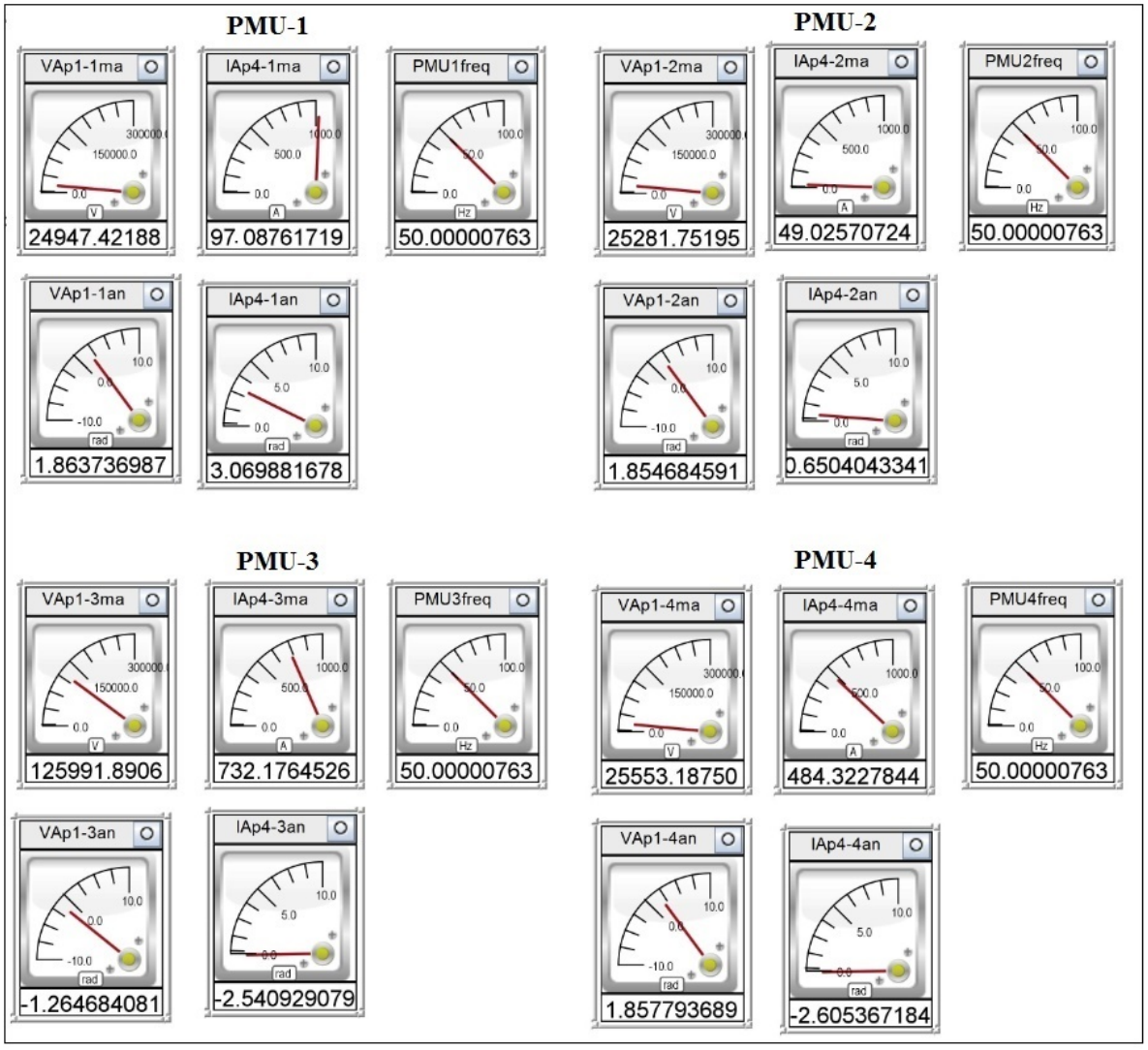

FIGURE 6.9: Measurements from Four PMUs

In the Fig. 6.9 above, the rms instantaneous voltages of the buses are shown. PMU output can be taken as script file also. The data accuracy is very high and the sampling rate is 50 samples per second ideally. In the simulation the sampling rate is around 48 samples per second.

6.2.5.2 Bus Voltages

The voltages of the other buses are shown in the Fig. 6.10 below verifies the PMU voltages with RSCAD RunTime module data.

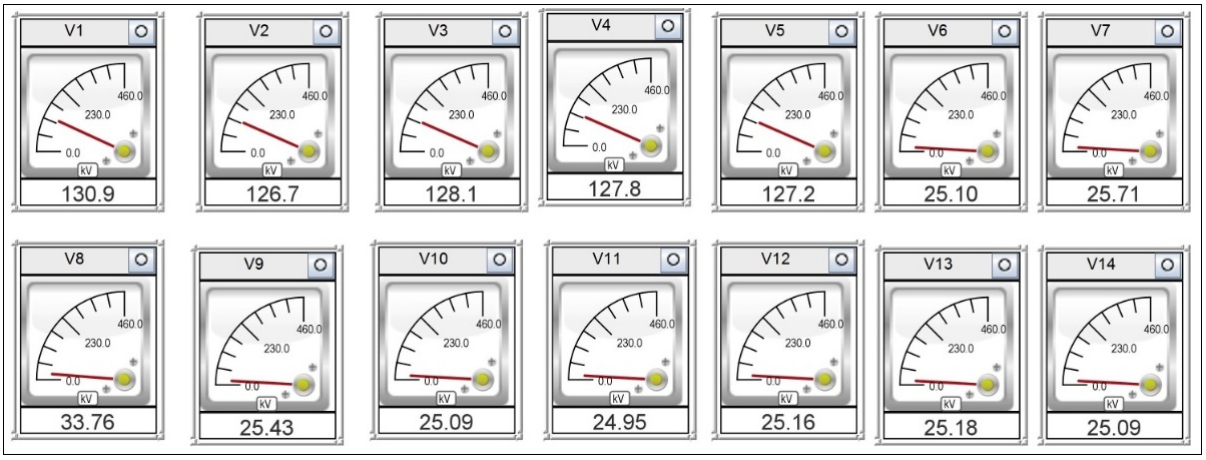

FIGURE 6.10: Bus Voltages

6.2.5.3 Reactive Power Outputs

In the Fig. 6.11, reactive power measurements for the implementation of FVSI are shown. The notation is given in RSCAD as; Q1n5 signifies reactive power at bus-1 i.e. receiving end reactive of the transmission line-1 and Q5n1 signifies sending end reactive power of line-1. Negative sign indicates the reverse power flow or that particular bus is delivering reactive power. E.g. negative Q1n5 signifies reactive power flowing from bus 1 to 5.

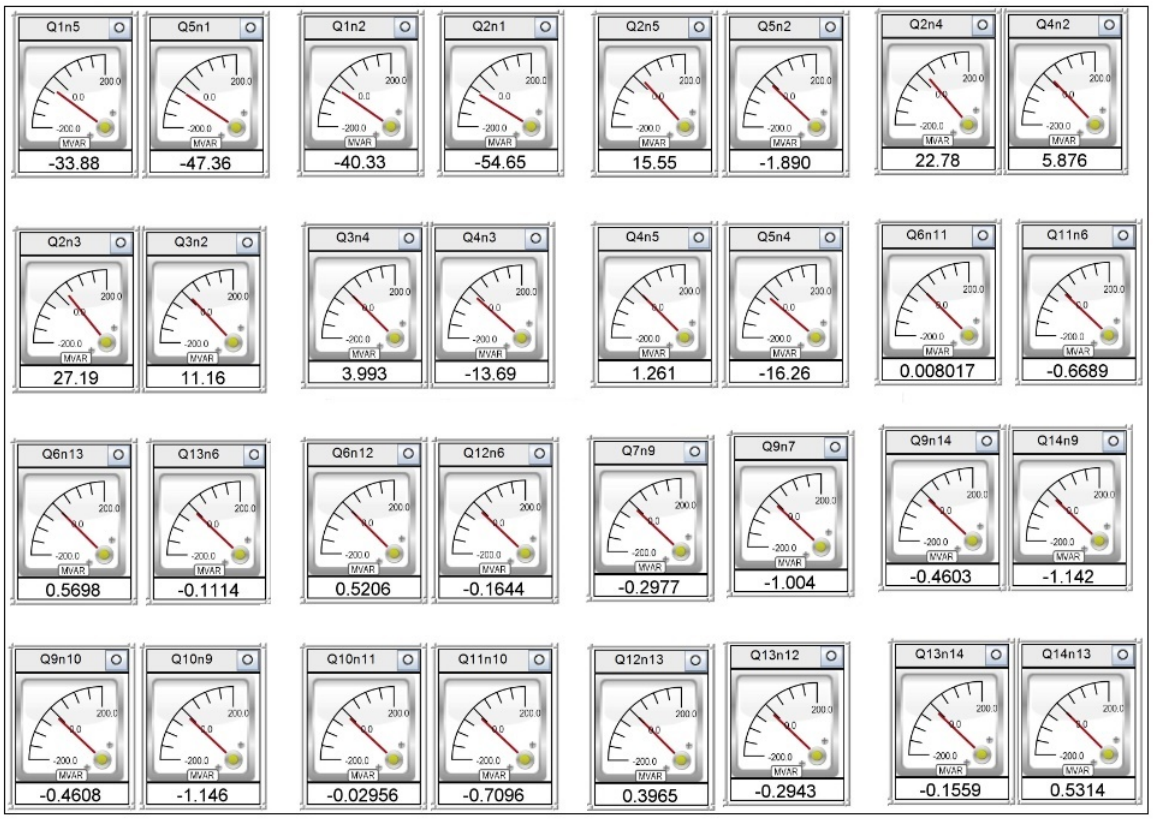

FIGURE 6.11: Reactive Power Flow

6.2.5.4 FVSI

The load ranking, weak bus and voltage stability condition determined as a result for the voltage stability analysis are shown in Fig.6. 12 and Fig. 6.13. The FVSI indicators for all the lines are shown in the Fig. 12.

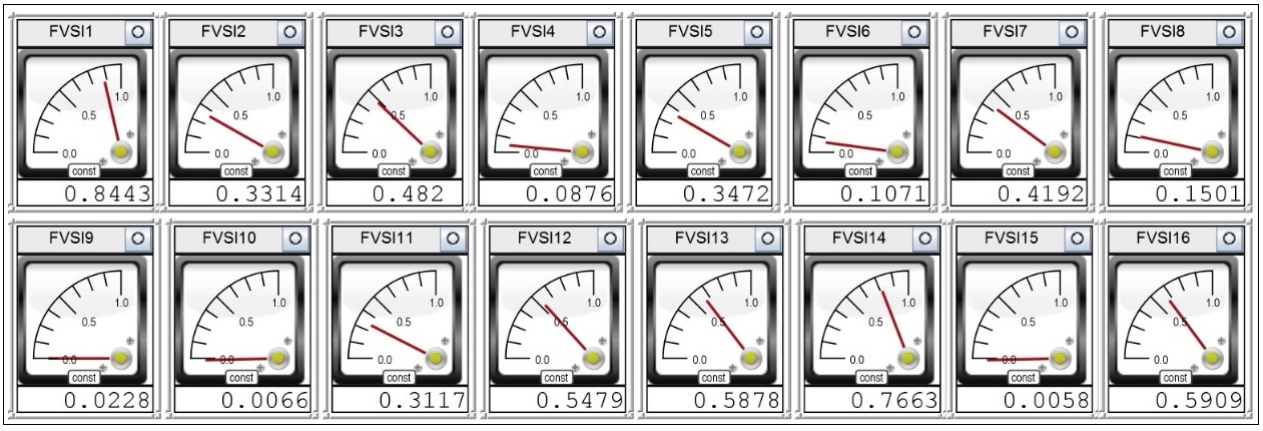

FIGURE 6.12: All Indices Displayed On Runtime of RSCAD

The dynamic loads connected on the buses can be varied manually to maintain the index within the set limit. In the below Fig.6.13, the numbers on the top of the dynamic load slider showing the individual bus connected to it. The set maximum loading for all the indices to be within limit is shown.

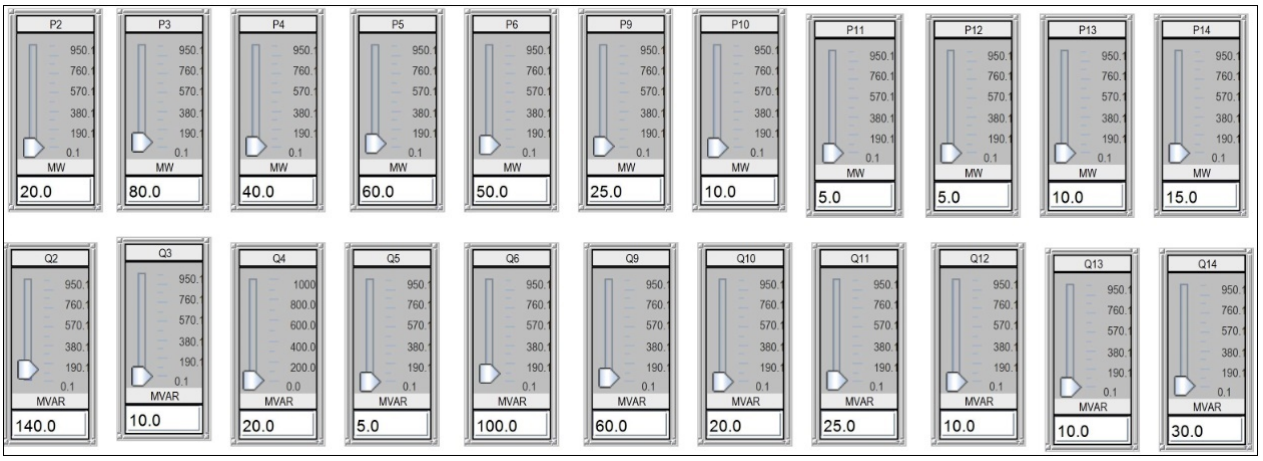

FIGURE 6.13: Maximum permissible Load Values for Safe FVSI

After successful placement of PMUs on RTDS, the complete information about the system can be achieved with a data rate of 20 samples/second at very high accuracy. So, the determined FVSIs in the present work are extremely accurate and dynamic. The RTDS has been configured so that a weak bus which corresponds to the critical line can be determined easily by just looking at the FVSI indicators, since beyond the limit of 1.00 the indicator will show red signal. By adjusting the slider, it is obviously known that increment in the reactive power loading on the bus leads to the increment in line index. From the fig.2, line-1 is the most critical line and the buses 1 & 5 corresponding to that line are the most critical buses. Bus-5 has the least maximum permissible load of 5 MVAR and it is ranked the highest in the system. Similarly line-15 and bus-4 are the most secure ones in the system.

The value of indices shown in the Fig. 6.12 indicates a stable system because all the indices are within limit (less than 1.00). The ranking of the line is decided based on the closeness of the index to 1.00. It can be seen from the above figure that FVSI-1 is very close to instability so it will be placed at highest rank in the table. The line which has index value near to 1.00 and the buses correspond to it are most sensitive. Ranking of sensitivity also shown in the below table below. The Line-1 is the most sensitive towards instability and Line-15 is the safest line. The bus no. 5 is the most critical bus and bus-8 is farthest from the instability.

Ranking	FVSI	Bus	Ranking	FVSI	Bus
1	FVSI-1	Bus-5	9	FVSI-2	Bus-14
2	FVSI-14	Bus-1	10	FVSI-11	Bus-9
3	FVSI-16	Bus-3	11	FVSI-8	Bus-6
4	FVSI-13	Bus-12	12	FVSI-6	Bus-2
5	FVSI-12	Bus-13	13	FVSI-4	Bus-7
6	FVSI-3	Bus-10	14	FVSI-9	Bus-8
7	FVSI-7	Bus-4	15	FVSI-10	
8	FVSI-5	Bus-11	16	FVSI-15	

TABLE 6.1: Sensitivity Ranking

6.3 Voltage Stability Analysis

To determine the overall system stability, all the load buses are consecutively tested in the system. The simulation results show the critical point of voltage stability condition, critical line and the weak bus in the system. The loadability of the individual bus in the system determines the weak bus and load ranking is done accordingly (maximum allowable load on the bus in ascending order). The bus which has lowest value of maximum permissible load is given the highest rank, which is the weakest bus in the system. The line which has FVSI close to 1.00 determines the voltage stability condition & critical line referred to a particular bus.

Chapter 7

Conclusion & Future Work

The optimal PMU placement scheme verifies the superset concept, enhancement in reliability of monitoring and sequential lowering in depth of unobservability. By introducing voltage stability index, classification of lines according to weakness and sensitivity ranking of the buses made possible. Simulation results of FVSIs for the IEEE 14 bus test system demonstrate the advanced wide area monitoring of the power system network. Placement of dynamic loads on the buses and varying them with slider allows us to set the buses at its maximum loadability according to the closeness of sensitivity index. Extremely dynamic values of FVSIs leads to monitoring of any complex grid by just keeping eyes on the few indicators those are equal in nos. of transmission/distribution lines of the system. By implementing voltage stability index on real time test bed, simultaneous values of FVSI will draw the power system to a highly predictable future of the buses.

Since in this dissertation only one case of IEEE 14 bus test system has been demonstrated, to validate these objectives more cases need to be tested especially real time power system networks. Voltage improvement strategy will become easier. Control strategy for grid will be precise due to placement of FACTS devices or any other compensating equipment can be placed/switched on the exact location (only on critical buses) in the network according to the closeness of voltage collapse. The placement of automatic switching capacitors on the critical buses and by setting reference for FVSI (say 0.95), will lead to ease of automatic reactive power management.

Publication

[1] Hiral Kumar, Vishal Kumar, "Real Time Power System Voltage Stability Stability Monitoring using Synchrophasor Devices", communicated in *2016 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (IEEE ICPEICES 2016)*, to be held in Delhi Technological University, India, July 2016.

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