3-LEVEL Z-SOURCE INVERTER BASED PV SYSTEM WITH BIDIRECTIONAL BUCK-BOOST BESS

A DISSERTATION

Submitted in partial fulfilment of the

requirements for the award of the degree

of

INTEGRATED DUAL DEGREE

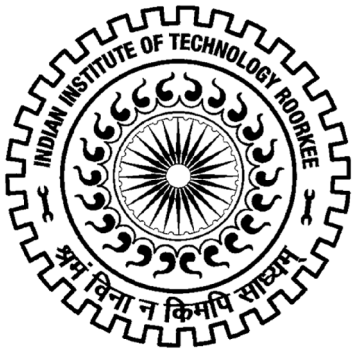
in

ELECTRICAL ENGINEERING

(with specialization in Power Electronics)

By

HARSHIT



DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

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CANDIDATE'S DECLARATION

I hereby declare that the work carried out in this dissertation entitled **"3-LEVEL Z-SOURCE INVERTER BASED PV SYSTEM WITH BIDIRECTIONAL BUCK-BOOST BESS"** submitted in partial fulfillment of the requirements for the award of the degree of Integrated Dual Degree (IDD) in Electrical Engineering with specialization in Power Electronics, submitted to the Department of Electrical Engineering, Indian Institute of Technology Roorkee, is an authentic record of my own work carried out under the guidance and supervision of Dr. Avik Bhattacharya, Assistant Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee and all the works embodied in this thesis has not been submitted elsewhere for the award of any other degree.

Date:

Place: **Roorkee** **(HARSHIT)**

CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge and belief.

(Dr. Avik Bhattacharya)
Assistant Professor,
Department of Electrical Engineering,
Indian Institute of Technology Roorkee
Roorkee-247667, India

ABSTRACT

Z-source inverters (ZSI) have a unique ability to achieve single stage voltage buck-boost operation for energy conversion. This thesis presents a three-level ZSI using a single LC impedance network for photovoltaic (PV) application. The network is used between DC voltage source (including PV array and a bidirectional buck-boost system) and neutral-point-clamped (NPC) inverter to achieve the desired stepped-up and stepped-down output voltage level as per the solar variation. Alternative phase opposition and disposition (APOD) modulation technique with proper triplen offset and appropriate addition of time delay/advance is used to achieve the required boost in DC link voltage. A traditional MPPT technique (Perturbed and Observed (P&O) is used to introduce a shoot-through interval in switching waveform to extract the maximum power from the PV panel. Traditional MPPT technique does not allow boosting the Z-network capacitor voltage more than the maximum power point (MPP) voltage of the PV array. This thesis presents a unified voltage control technique to track the MPPT and also maintains the desired Z-source capacitor voltage level. The design, implementation and control of single impedance network based multilevel ZSI for photovoltaic application with BESS according to generation-demand is discussed. This proposed topology not only tracks MPPT output voltage but also maintained constant output voltage with wide range of variation of insulation (irradiance). To validate the proposed scheme the system is extensively simulated in MATLAB/Simulink.

ACKNOWLEDGEMENTS

This thesis is a part of my M.Tech. Dissertation "**3-LEVEL Z-SOURCE INVERTER BASED PV SYSTEM WITH BIDIRECTIONAL BUCK-BOOST BESS** " for the partial fulfilment of the requirements for the award of the Integrated Dual Degree in Electrical Engineering. I wish to affirm my deep sense of gratitude to my guide Dr. Avik Bhattacharya, Department of Electrical Engineering, IIT Roorkee, for his intuitive, meticulous and benevolent guidance at all stage of my dissertation work. I wholeheartedly thank him for his kindly co-operation in scrupulously scrutinizing the manuscript and his valuable suggestions throughout my dissertation work. His knowledge has proved to be very useful for me to do the dissertation work appropriately.

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HARSHIT
Enroll. No. 10212006
IDD Electrical (EPE)

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LIST OF ACRONYMS

AC	Alternating Current
APOD	Alternative Phase Opposition and Disposition
CSI	Current Source inverter
DC	Direct Current
FFT	Fast Fourier Transform
MLI	Multilevel Inverter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NPC	Neutral Point Clamped
PI	Proportional Integral
PWM	Pulse Width Modulation
PV	Photovoltaic
THD	Total Harmonics Distortion
VSI	Voltage Source Inverter
ZSI	Z- Source inverter
BESS	Battery energy storage system

LIST OF SYMBOLS

Ir	Solar Irradiance
Temp	Temperature
V_dclink	Inverter DC link voltage
Vc	Z Network capacitor voltage
$P_{\_PV}$	Power delivered by PV panel
$V_{\_PV}$	Output voltage of PV panel
$I_{\_PV}$	Current delivered by PV panel
L_1, L_2	Z-Network Impedance
C_1, C_2	Z-Network Capacitance
D	Shoot through duty ratio
V_0	Input DC voltage source
P_L	Load power demand

CHAPTER 1: INTRODUCTION

1.1 Research Motivation

The demand for energy is rapidly increasing from all across the globe to meet the pace of economic development. Diminishing fossil fuel reserves and increasing pollution level has urged the society to look for alternative energy source which are clean, promising and renewable in nature. Among all available renewable energy sources photovoltaic (PV) energy is proven to be most reliable source of energy [1]. The major challenge of PV based power conversion system is proper power conditioning because output voltage of PV panel varies with environmental conditions of irradiance and temperature. Inverter topology plays a crucial role in PV based power conversion system (PCS). Traditionally two stage buck-boost based inverter topology is most commonly used in PV energy conversion to adapt to the varying nature of the load [2]-[6]. For two stage PV power conversion system voltage source inverters (VSI) and current source inverters (CSI) based inverter topologies are employed.

Z-Source inverter (ZSI) is recently proposed inverter topology which has promising power conditioning ability especially in the field of PV or other renewable energy based generation systems. Z-source inverter has an impedance network which provides a unique ability to achieve the single stage buck-boost voltage operation based power conversion in the AC output voltage, which is not possible by traditional inverters [7].

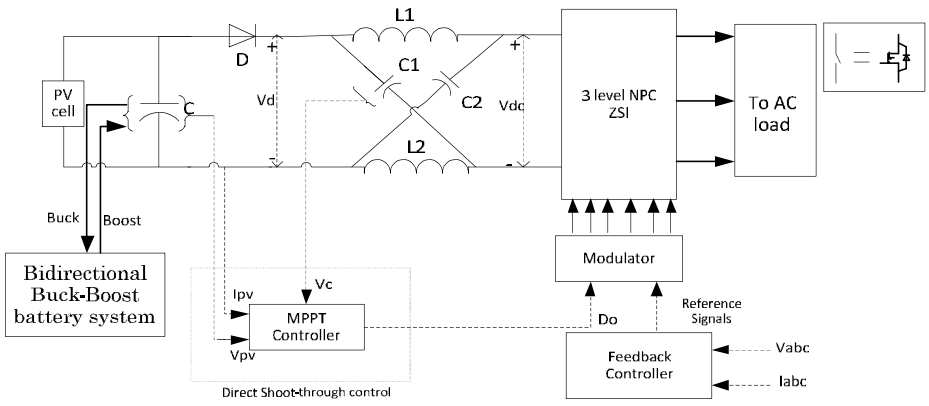


Figure 1.1 Three phase ZSI based photovoltaic PCS with bidirectional buck-boost

In recent years, multilevel inverters are gaining attention of researchers and manufactures because of their ability to produce better performance in terms of their output waveforms and lesser total harmonic distortion (THD). Three-level ZSIs provide a single stage voltage buck-boost operation based energy conversion while retaining all the favorable advantages of traditional

inverters. The power circuit of three phase ZSI for PV with BES system using traditional shoot-through control is shown in Figure 1.1. The voltage boost operation is achieved by inserting the shoot through interval in switching waveform, thus it provides greater circuit reliability as no dead band time is required unlike tradition inverters. MPPT controller gives a duty ratio which is used to introduce the shoot-through state so as to maintain the PV output voltage at maximum power point (MPP). Furthermore, the demand-generation mismatch is minimised using the bidirectional buck-boost BESS. The inverter DC link voltage level is adjusted accordingly to meet the load demand. To achieve this, Z-network capacitor voltage of ZSI should also be increased/ decreased accordingly. A traditional MPPT controller e.g. P&O method, is unable to boost the Z- network capacitor voltage beyond MPP. This thesis thus incorporates a unified voltage control technique to track the MPPT and achieves the desired capacitor voltage control. The performance investigation is carried out using modified APOD based control technique for a single impedance network based three level neutral point diode clamped ZSI.

1.2 Literature Review

This section presents a review of research works that have already been done so far in the field of ZSI and PV generation system. Literature review is presented in four sections. In first section, solar photovoltaic modules connected in possible array configurations under normal/partial shaded conditions are discussed. Followed by, various existing Z source inverters are briefed, based on its topological and design/modulation schemes suited for different applications in the second and third sections. Furthermore, in fourth section bidirectional buck-boost battery system is discussed which minimizes the demand-generation mismatch between the solar variation and the load.

1.2.1 Review Based on Analysis of Solar Photovoltaic Systems

An approach is made by *Sera et al* (2007) to demonstrate the construction of the PV panel model by using the single diode five parameter model, exclusively based on the parameters provided in the data sheet to predict the behaviour of the panel under the different environmental conditions of temperature and irradiance [8].

A circuit model was proposed by *Marcelo Gradella Villalva et al* (2009) for use in simulations of PV systems to obtain the performance characteristics of the photovoltaic modules [9].

Abir Chatterjee et al (2011) presented a single diode model based PV model estimation method using PV module data to estimate the parameters of arrays under the varying temperature and irradiance [10].

Trishan Esram (2007) *et al* have discussed many methods of tracking the Maximum Power Point (MPP) of the PV panel [11]. This literature consists of all the MPPT techniques implied in the field of maximum power point tracking.

1.2.2 Review Based on Topological Analysis of Z Source Inverters

F. Z. Peng, introduced the concept of ZSI in year 2003 [7]. The operation, analysis and control techniques for ZSI is discused in this literarture.

A two level ZSI for photovoltaic systems was proposed by *Yi Huang et al* (2006) to realize the inversion and the voltage boost operation in one single stage with design guideline using simple boost control as switching scheme [12].

Through simulation and a scaled down laboratory prototype *Poh Chiang Loh et al* (2007) demonstrated a three-level Z source NPC inverter using a single LC impedance network [13].

Poh Chiang Loh et al (2008) presented the two three-level cascaded ZSI with one or two impedance networks in the front end controlled using different modulation approaches such as phase disposition and phase shifted carrier switching schemes [14].

A two level voltage type improved ZSI was proposed by *Yu Tang et al* (2011) for standalone PV systems using simple boost control as switching scheme [15].

Yuan Li et al (2009) demonstrated a Quasi ZSI for PV based generation systems with design guideline through simulations and experiments [16].

The earlier attempt to investigate different inverter topologies was discussed, and they are briefly reported in the survey work by *Keith Corzine et al* (2004) [17], *Mariusz Malinowski et al* (2010) [18] and *Jose Rodriguez et al* (2002, 2010) [19], [20]. In these survey works, topologies, control and applications of different types of inverters proposed by various researchers for many applications are reported.

1.2.3 Review Based on Design and Modulation Scheme Analysis of Z Source Inverters

Maximum boost control was employed for Z source inverter to get the maximum possible boost in the voltage for a given modulation index and its various associated parameters were analyzed by *Fang Zheng Peng et al* (2005) through simulations and experiment verifications [21].

The performance of ZSI with conventional pulse width modulation (PWM) inverter and DC–DC boost topology based PWM inverter for fuel cell vehicle applications were compared by *Miaosen Shen et al* (2007) [22].

Comparative simulation studies for three different topologies of two level voltage type Z source inverters under four different switching schemes viz., simple boost control, maximum boost control, maximum constant boost control, and the modified space vector PWM control were carried out by *Omar Ellabban et al* (2009) with a design example for hybrid electric vehicles [23].

Hanif et al (2011) explained circuit calculations and analysis, self-boost phenomenon, design calculations for Z network inductor and capacitor, boost control mechanism and the device selection criteria of ZSI suited for photovoltaic systems with a design example [24].

1.2.4 Review Based on Analysis of Battery Energy Storage System (BESS)

PM. D¨urr (2006) proposed a dynamic model of a lead acid battery and used it for domestic purposes [36]. H. L. Chan (2000) presented a new battery model which was used for charging of electric vehicles from the energy stored in the battery [37]. The model of the battery consists of a constant internal resistance in series with an ideal voltage source.

Some of the BESS applications such as storing extra power from the renewable energy sources if exceeds a certain threshold is explained by A. Arulampalam [38] and J. Zeng [39]. Power quality and stability of wind farms were improved in these literatures.

Recently Nishad Mendis (2013) explained an integrated control approach for standalone operation of a hybridised wind turbine generating system with maximum power extraction capability. The demand-generation mismatch is minimised using the bidirectional buck-boost BESS. The inverter DC link voltage level is adjusted accordingly to meet the load demand [40].

1.3 Objective of the Thesis

This thesis presents a detailed study on the various aspects of the design, implementation and control of single impedance network based three level NPC inverter for photovoltaic generation systems with BESS according to generation-demand. The thesis covers the following key areas:

- Mathematical modeling of the PV panel to study the various characteristics of the PV panel and the effect of the irradiance and temperature on the performance of the PV panel.
- Algorithms to extract the maximum power from the PV panel under varying environmental conditions of irradiance and temperature.
- Analysis of the single impedance network based three-level neutral point diode clamped Z-source inverter topology to achieve the single stage voltage buck-boost operation for PV energy conversion.
- Application of alternative phase opposition and disposition (APOD) based modified modulation technique to control the three-level ZSI.
- Presents a unified voltage control technique for APOD modulation technique based three-level ZSI to achieve MPPT and also maintains desired Z-network capacitor voltage control to facilitate proper power conditioning.
- Minimises the generation- demand mismatch between the PV panel and the load using bidirectional buck-boost battery system.
- MATLAB simulation work to study the operation of single impedance network based three-level ZSI for standalone PV generation system.
- Development of hardware prototype to verify the simulation results by carrying out the experimental investigation in the laboratory.

1.4 Thesis Organisation

The thesis is comprised of eight chapters. Each chapter discuss a particular aspect of single impedance network based multi-level ZSI for PV generation system in detail. .

Chapter 1 deals with the literature survey, objective of the thesis and the chapter wise organization of the thesis.

Chapter 2 discusses the modelling of PV panel and PV based power generation system. The output power of PV panel depends on the environmental conditions of irradiance and temperature. MPPT techniques to extract the maximum power from the PV panel are also discussed.

Chapter 3 introduces the Z Source inverter topology, its features and the principle of operation. Single impedance network based multi-level Z-source inverter topology is also discussed. The calculation for designing the impedance network parameters is discussed.

Chapter 4 describes the various control strategies used for controlling the Z Source Inverter. Alternative phase opposition and disposition (APOD) based modulation technique to control three level ZSI inverter is discussed. A unified voltage control technique to simultaneously achieve the

MPPT for PV panel and also maintains the desired Z-network capacitor for proper power conditioning is discussed in detail. Matlab and Xilinx model of modified APOD scheme is also presented.

Chapter 5 decribes the control strategy for BESS which is used to minimise the demand-generation mismatch.

Chapter 6 presents the MATLAB simulation results for operation of single impedance network based three-level ZSI for standalone and grid connected PV generation system.

Chapter 7 discusses the development of hardware prototype in laboratory. Results obtained on the oscilloscope are clearly presented.

Chapter 8 presents the conclusion of the dissertation thesis and gives some recommendations for future work.

2.1 Solar power is the key solution to meet the increasing world energy demand

The energy demand is increasing exponentially with rapid growth of industries and living standards of people. Traditionally fossil fuels are always been used as primary source of energy to meet the increasing demand of the today's world. The fossil fuels are non-renewable, exhaustible and a major source of pollution so we can't depend on conventional source of energy forever. Solar energy is a non-polluting as it gives zero emission, inexhaustible and freely available source of energy. Solar energy is used for variety of application mainly solar heating and electricity generation. Photovoltaic technology is the most efficient, so the most popular technology for utilizing the solar power.

2.2 Photovoltaic panels

Photovoltaic panels are composed of PV cells which directly converts energy of sunlight directly into most easily usable form of electrical energy by photoelectric effect. Sunlight striking the panel excites the electron from valence band to conduction band and thus flow of current takes place. At present monocrystalline silicon and amorphous silicon are the most commonly used materials in photovoltaic panels. The abundance of silicon and zero maintenance requirement of PV panel makes PV power generation more economical than any other technology for utilizing solar energy. Usually series and parallel configurations of large number of PV panels are used to fulfil energy requirement. Commercially PV modules with different capacity are available (60W to 170W). When several PV cells are connected in series and parallel connections then it is called PV array. Series connected cells increases the voltage rating of the panel whereas the parallel connected cells are responsible for increasing the current rating of the PV panel.

2.3 Modelling of PV panels

Modelling of PV module is based on a single diode equivalent model considering the irradiation (insolation) and temperature as per the nominal condition. Equation (1) represents the equivalent circuit of a PV cell, shown in Figure 2.1 [25].

$$I = I_{ph} - I_0[\exp\{(V + R_sI)/V_ta\} - 1] - V + (R_sI/R_p) \quad (1)$$

Where;

I: Output current of the cell

I_0: Diode saturation current;

I_{ph}: Current induced by irradiance and temperature;

R_s: Equivalent series resistance of the resistive contact;

N_s is the number of PV cells connected in series;

$V_t = N_s kT/q$ is the volt-temperature equivalent of the array;

R_p: Shunt resistance representing the leakage resistance.

Equation (2) gives the linear dependency of I_{ph} on the irradiance influence of temperature [25].

$$I_{ph} = G/G_n[I_{ph,n} + K_i(T - T_n)] \quad (2)$$

Where:

G_n is the nominal solar irradiance irradiance;

G is the solar irradiance.

$I_{ph,n}$: Current induced by irradiance and temperature corresponding to the nominal environmental condition (25ºC and 1000W/m^2)

T_n: Nominal temperature of the PV cell;

T: the temperature of the PV cell;

K_i: Temperature versus current coefficient.

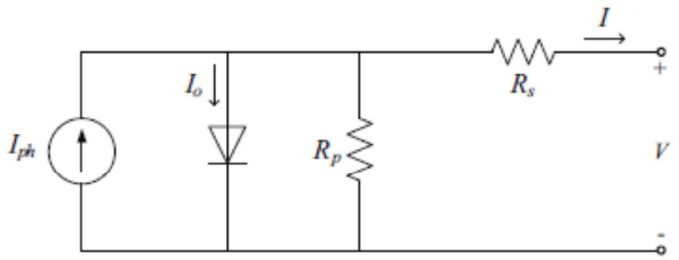


Figure 2.1 Equivalent circuit of a PV cell

Temperature dependency of the diode saturation current, I_0 is expressed in the equation (3) [26].

$$I_0 = I_{o,n}(T/T_n)^2[qE_g/ak(1/T_n - 1/T)] \quad (3)$$

Where:

$I_{o,n}$: Saturation current of the diode;

$k = 1.380 \times 10^{-23}$ J/K, Boltzmann constant;

$q = 1.602 \times 10^{-19}$ coulomb, charge of an electron;

E_g =1.12 ev, band gap energy.

Equation (4) gives the expression for nominal saturation current of diode, $I_{o,n}$ [26].

$$I_{o,n} = I_{sc,n}/[\{\exp(V_{oc,n}/aV_{t,n}) - 1\}] \quad (4)$$

Where;

$V_{t,n}$: Nominal thermal voltage of the PV cell;

$V_{oc,n}$: Nominal open circuit voltage of PV panel;

$I_{sc,n}$: Short circuit current of panel at the nominal environmental condition (25ºC and 1000W/m^2).

If N_s, PV cells are connected in series and parallel configuration in a PV array, then the equation (1) can me modified and re-expressed as equation (5) [25], [26].

$$I = N_pI_{ph} - N_pI_0[\exp\{((V + R_sI(N_s/N_p))/ N_sV_ta\} - 1] - (V + R_sI(N_s/N_p))/R_p(N_s/N_p) \quad (5)$$

Where:

N_p is the number of PV modules connected in parallel configuration;

N_s is the number of PV modules connected in series configuration.

Almost all of the parameters used in above equation can be obtained from the datasheet of the PV panel provided by the panel manufacturer.

2.4 Maximum Power Point Tracking Technique (MPPT)

The PV array possesses a non-linear current versus voltage (I-V) and power versus voltage (P-V) characteristics as illustrated in Figure 2.2. The PV output voltage and current, so do the power delivered by the PV panel varies with variation in environmental condition of irradiance and temperature [27]. To harness the maximum power from PV panel under the changing environmental MPPT techniques are employed. There are various algorithms to achieve the MPPT for PV panel are available [28]-[30].

The most popular and commonly used MPPT techniques are discussed in following sections:

- Incremental Conductance (IC) Methods [31]
- Perturb and Observe (P&O) Methods [31]

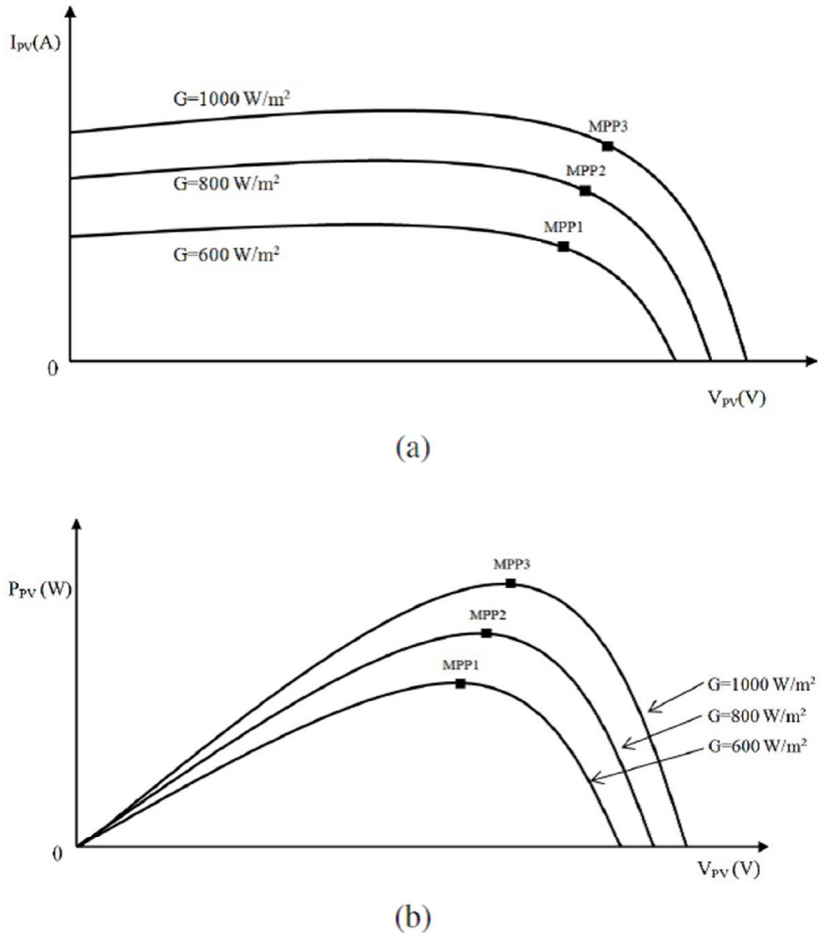


Figure 2.2 (a) Current versus voltage (V-I) (b) Power versus voltage (P-V) characteristic.

2.4.1 Incremental Conductance (IC) Method

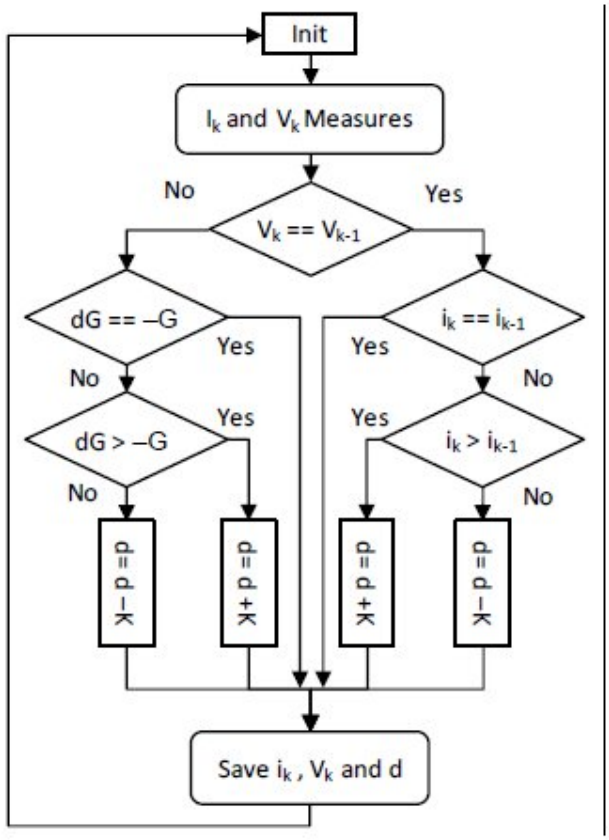
The principle of the Incremental Conductance (IC) Method utilises the property of the maximum power point (MPP): the derivative of the power is null, as shown in equation (6). So, the IC method uses an iterative algorithm based on the evolution of the derivative of conductance G, as expressed in equation (7). Where the conductance is the *I/V* ratio.

$$dP/dV = 0, \text{ with } P = V.I \tag{6}$$

$$dP/dV = V.dI/dV + I\ dV/dv = 0, \text{ Thus: } dI/dV + I/V = 0, \text{ gives } dG + G = 0 \tag{7}$$

This method (ICa) has been improved, because when the voltage is constant, dG is not defined. So, a solution is to mix the CV method with the IC method. It is known as the Two- Method MPPT

Control (or ICb). Figure 2.4 shows the Two-Method MPPT Control algorithm and the code of the Matlab embedded function:

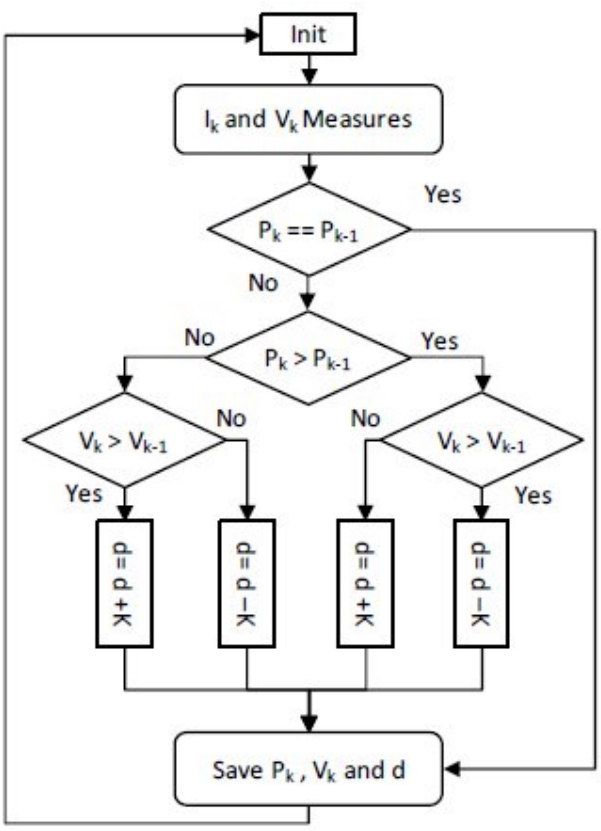



```
function y=IC(u)
  global i v Kic d_ic
  Kic=0.01;
% u(1) is the measure PV current
% u(2) is the measure PV voltage
G=u(1) / u(2); %G is the conductance
dv = u(2) – v;
di  = u(1) – i;
if (dv==0)  %equivalent to the CV method
  if (di==0)          C = d_ic;
    else if (di > 0)  C = d_ic + Kic;
    else              C = d_ic – Kic;
    end
  end
else
  dG = di / dv; % here start the IC method
  if (dG==–G)         C = d_ic;
    else if (dG > –G) C = d_ic – Kic;
    else              C = d_ic + Kic;
    end
  end
end
i= u(1); %save old current value
v=u(2); %save old voltage value
d_ic=C; %save old conductance value
y=d_ic;
```

Figure 2.3 IC Method MPPT Control algorithm and the code of Matlab embedded function

2.4.2 Perturb and Observe (P&O) Method

The operating principle of P&O is based on perturbing the current and the voltage of the PV at a regular interval and then comparing the new power measure with the previous to decide the next variation. The Perturb and Observe (P&O) Methods are most commonly used MPPT method. Figure 2.4 shows the P&O algorithm and the code of the Matlab embedded function.




```
function y=PnOa(u)
  global p v Kpnoa d_pnoa
  Kpnoa=0.01;
% u(1) is the measure PV power
% u(2) is the measure PV voltage
  if ((u(1)==p)    C = d_pnoa;
  else
    if ((u(1)>p)
      if ((u(2)>v)  C= d_pnoa – Kpnoa;
      else          C= d_pnoa + Kpnoa;
      end
    else
      if ((u(2)>v)  C= d_pnoa + Kpnoa;
      else          C= d_pnoa – Kpnoa;
      end
    end
  end
p= u(1); %save old power value
v= u(2); %save old voltage value
d_pnoa =C;
y= d_pnoa;
```

Figure 2.4 P&O algorithm and the code of Matlab embedded function

P&O algorithm based MPPT methods is robust enough to obtain the MPP, even if two PV panels have been connected in series with different solar irradiance.

3.1 The Traditional Inverter types and their limitations

The most popular type of inverters includes the Voltage source inverter (VSI) and the Current source inverter (CSI). These inverters are extensively used for machines, AC uninterruptible- power-supplies (UPS), induction-heating, AC power-supplies, active-power-filters & UPQCs etc. The CSI is generally used in high power applications as it has an inherent over current protection. VSIs are generally used in low power applications [32], [33].

3.1.1 The Voltage Source Inverter and its limitations:

A Voltage source inverter uses a DC voltage source to produce an AC output. Due to simple design and control it is widely used. It has the following limitations:

- The output AC voltage is limited to the DC link voltage and cannot exceed it. In systems where higher voltages are required, an additional DC-DC converter has to be employed to get the desired AC Voltage. This decreases the system efficiency and increases the system cost.

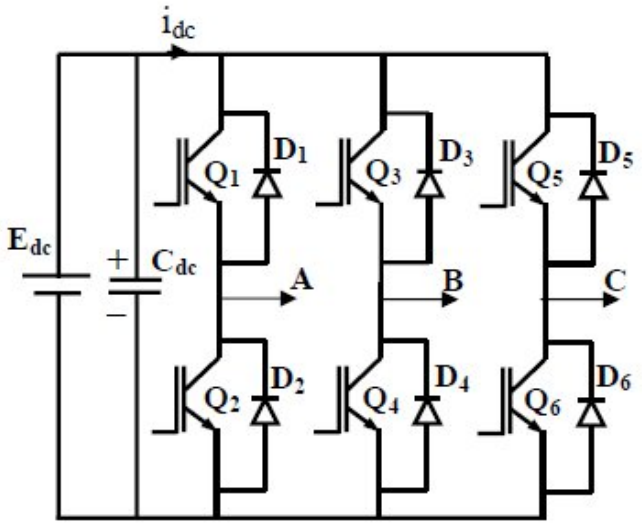


Figure 3.1 Voltage Source Inverter

- A dead time has to be provided between the switching of devices in the same leg. This is because simultaneous gating of devices in the same leg intentionally of by some electromagnetic noise can cause a shoot through to occur. The shoot through essentially short circuits the DC voltage source and can destroy the devices. The dead time in conventional VSI also causes waveform distortion. Here no dead time/band, so no distortion.
- The output voltage waveform from the inverter is not sinusoidal. To achieve a sinusoidal voltage waveform an additional LC filter is necessary, which causes additional power loss.

3.1.2 The Current Source Inverter (CSI) and its limitations:

A current source inverter uses a DC current source to produce an AC output. This type of inverter has inherent overcurrent protection as the source is a current-source so it's a preferable choice in high power applications pertaining to drives, but it too has the following limitations:

- In a CSI the AC output voltage is at all times greater than DC link voltage. So, CSI is a boost-inverter for dc-ac power-conversion. In applications, where a wide-varying voltage-range is necessary, an additional converter is used which reduces system efficiency and increases system cost.

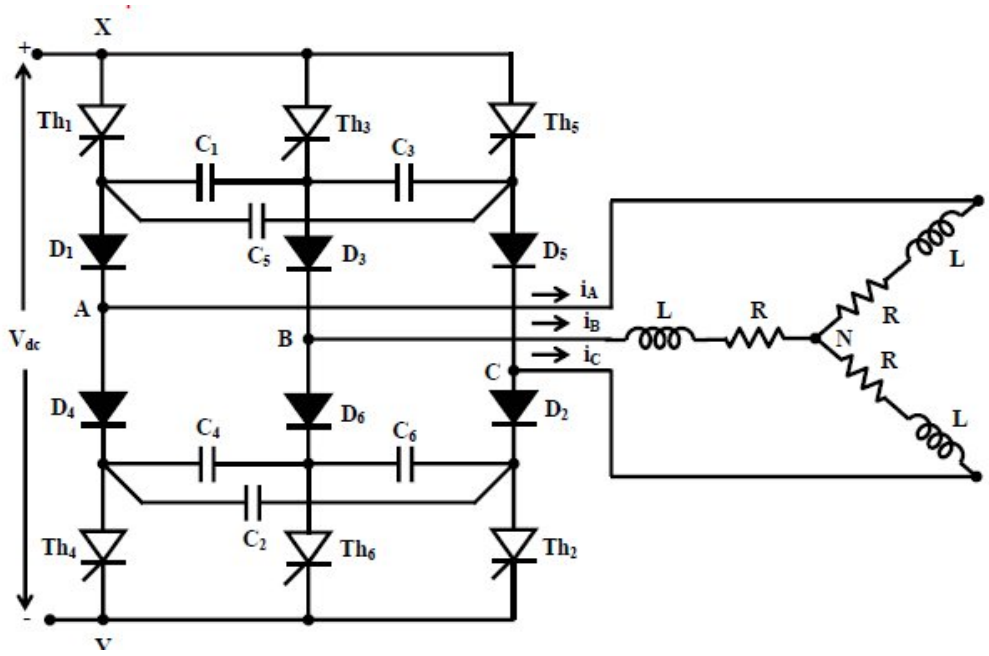


Figure 3.2 Current Source Inverter

- Due to current source, to maintain the continuity one of upper-leg-devices & one of lower-leg-devices has to be ON every time. If there is an open circuit then DC-link-inductor would cause damage to switching-devices. This circuit is also prone to accidental mis-gating and hence open circuit due to electromagnetic noise.
- The switching devices in a CSI have to have a reverse voltage blocking capacity which increases the system cost.

In conclusion both of the inverter technologies have the following drawbacks:

- There can either be a buck feature or a boost feature but not both, unless another power electronic converter is used cascade.
- The circuits and their switches are not interchangeable, a VSI circuit can only be used with a voltage source and a CSI circuit can only be used with a current source.
- Both of the type of converters are vulnerable to EMI noise and hence have lesser reliability.

3.2 Z-Source Inverter

The problems of the traditional VSI and CSI can be overcome using a new design of inverter known as the impedance source inverter [7]. The Z source inverter employs a distinctive impedance network to couple the switches to the main power source or to the another converter for providing unique features which cannot be observed in the VSI or CSI. Another unique feature about this inverter is that the source can be a DC Voltage or Current source.

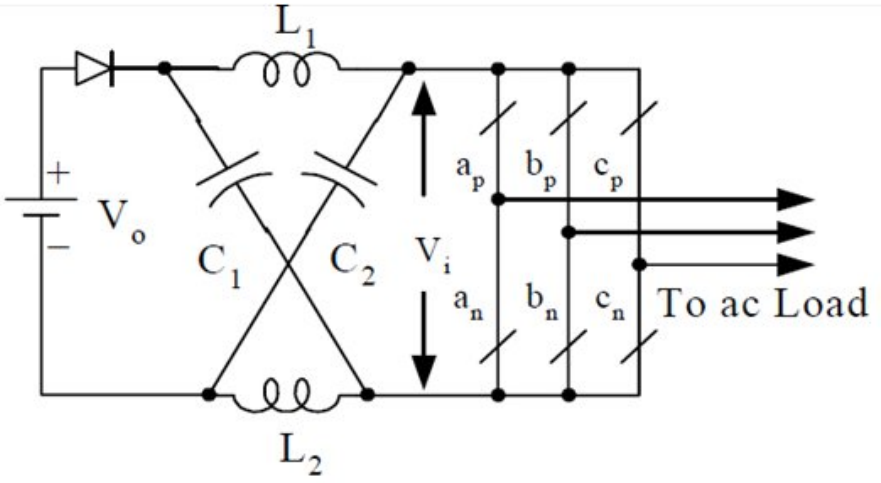


Figure 3.3 Two level Z-Source inverter

An X shaped LC network with an inverter circuit is used in Z source inverter topology. In Figure 3.3 basic two level Z- source inverter is shown. In Z impedance network two inductors and two capacitors are connected in X shape. Z source inverter is controlled by inserting shoot through state in normal switching waveform. Inserted shoot through states simultaneously turn on all switches of a particular leg to boost the DC link voltage.

3.3 Traditional Control Technique of ZSI

Compared to a conventional VSI, the ZSI has one more shoot-through switching state. During shoot-state, output is 0, identical to traditional zero states. So, in order to maintain sine output voltage, active-state's duty-ratio needs to be maintained and either partial or complete duration of zero-states should be turned to shoot-through state, to get extra boosting capability to inverter. Thus the complete PWM pulses to ZSI consist of simple pulses given to 2-level inverter (using conventional techniques) along with shoot-through pulses ("which causes shoot-through to boost DC-link-voltage"). Various techniques for generation/insertion of shoot-through pulses have been presented in below sections.

3.4 Simple Boost Control

The simple boost control uses 2 straight-lines to control the extent of insertion of shoot through zero states [23]. The two straight lines are compared with the triangular carrier wave. Whenever the carrier wave is higher than the upper line and whenever the triangular wave is lesser than the lower line, the inverter is put in the shoot through zero state. This method is easy to implement but it places higher stresses on the devices as some of the traditional zero states are not utilized. Also the maximum Duty cycle for the shoot through period is limited to (1-M) where M is the modulation index. This Duty cycle reduces to zero as the modulation index reaches the value 1.

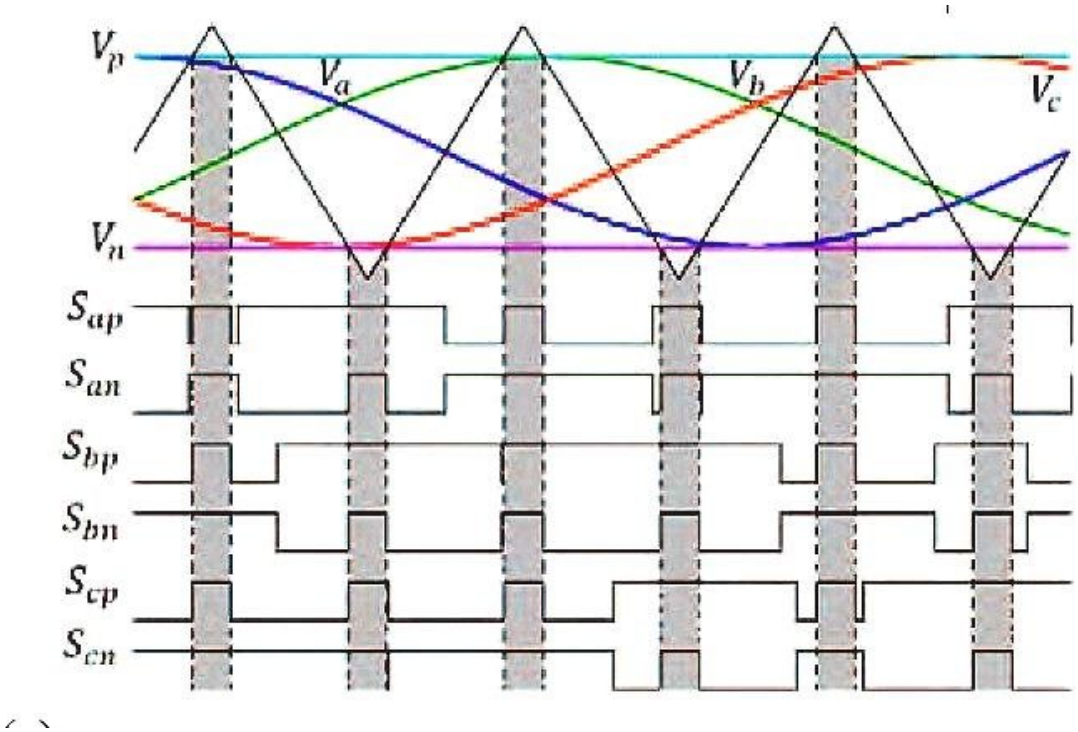


Figure 3.4 Simple boost control technique

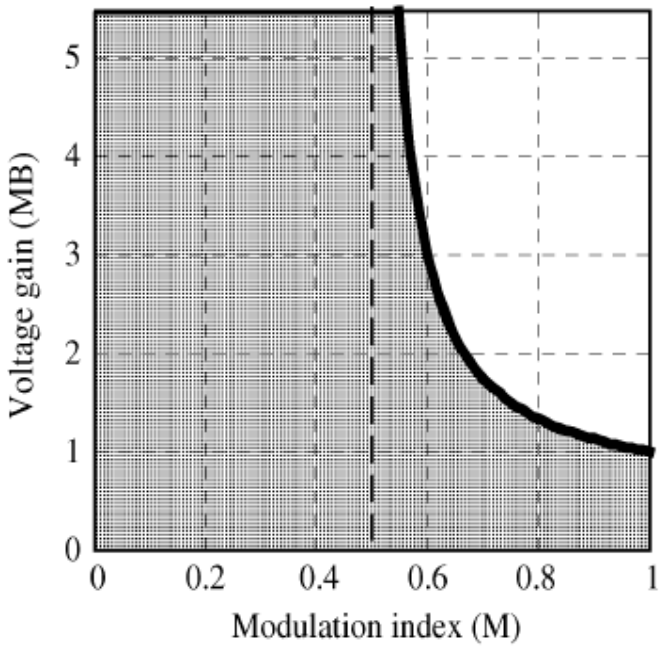


Figure 3.5 Voltage gain vs Modulation index for "simple-boost-control"

Gain in voltage is given by G is as follows, by setting the boost factor D_0 to maximum i.e. 1-M :

$$G = 2V_{ac\_peak}/V_{in} = BM = \frac{?}{?? ??} \quad (8)$$

The modulation index can be calculated for any desired gain as follows

$$M = \frac{?}{????} \quad (9)$$

Equivalent DC-link volt which appears across switches is the capacitor voltage of the inductor network. This voltage's equal to min DC-link volt of a normal VSI which will produce the same output AC voltage. This can be used to analyze the voltage-stress across switches (maximum stress across switch occurs in traditional zero states). Voltage stress on each switch can be expressed as:

$$V_? = BV_?? = ((2G) - 1)V_?? = V_{i\_peak} \quad (10)$$

3.5 Maximum Boost Control

In this method all of the traditional zero states are replaced by shoot through zero state [23]. This puts lesser volt-stress on devices as compared to last mentioned technique, which means that for given devices, inverter can be operated to obtain higher voltage gain. As can be seen from the figure when the carrier wave is graeter than max of phase volts V_a, V_b and V_c or when carrier wave is lesser than the minimum of the phase voltages then the circuit is put through the shoot-state. This is done because this is the interval when the circuit is in the traditional Zero state in normal PWM technique.

As can be seen from graph, the shoot-through duty-cycle reiterates after each pi/three interval and is expressed for θ in the range of $\frac{?}{?}$ to $\frac{?}{?}$ as:

$$\frac{?_?(?)}{?} = \frac{?? ?? \; ?? ? ? \; ?? ? ? ? \; ?\frac{??}{?}???}{?} = 1 - \frac{\sqrt{?}}{?}\mathrm{M}\cos(\theta - \frac{?}{?}) \tag{11}$$

D_0 has min value at $\frac{?}{?}$ & max value at $\frac{?}{?}$ or $\frac{??}{?}$. Thus, Voltage ripple across inductor can be estimated as sine with a peak to peak value of Current ripple through inductor becomes $\Delta I_L = V_{pk2pk}/6\omega L$.

$$\mathrm{V}_{?\,?\,?\,?\,?} = \mathrm{V}_{?\,?\,?\;?\,?} - \mathrm{V}_{?\,?\,?\;?\,?} = \frac{?\frac{\sqrt{?}}{?}?\frac{?}{?}?? \; ?}{?\sqrt{?}? \; ? \; ?}\mathrm{V}_{??} \tag{12}$$

To calculate the voltage gain and the stress on the switches we are interested in the average duty ratio. So average D_0 can be calculated as:

$$\frac{?_?^?}{?} = \int_{\frac{?}{?}}^{?} ? \frac{?? ?? \; ?? ? ? \; ?? ? ? ? \; ?\frac{??}{?}???}{?} ? \; \mathrm{d}\theta \quad = \frac{? ? ? ?\sqrt{?}??}{?} \tag{13}$$

which gives the boost factor B as: $\mathrm{B} = \frac{?}{?? ??\frac{?_?^?}{?}?} = \frac{?}{?\sqrt{?}? \; ?}$ (14)

And the voltage gain is given as: $\frac{?_?^?}{\frac{?\,??}{?}} = \mathrm{G} = \mathrm{MB} = \frac{??}{?\sqrt{?}? \; ?}$ (15)

Voltage stress across switch is expressed as: $\mathrm{V}_? = \mathrm{BV}_{??} = \frac{??\sqrt{3}? ? ? ??\,??}{\pi}$ (16)

Here we can clearly see that the overall shoot-through duty ratio will be dependent on average of lower & upper envelopes and hence it varies continuously. Although this method provides the maximum voltage gain as it utilizes all the Zero states but by doing so shoot-through state's duty-ratio varies along whole cycle as can be seen from the graph. Ripple in shoot-through state's duty-ratio results in inductor's current-ripple, also in volt across capacitor. In case of low output frequency, ripple in inductor current is no more insignificant, leading to requirement of large inductor. Thus it is suitable for high frequency application.

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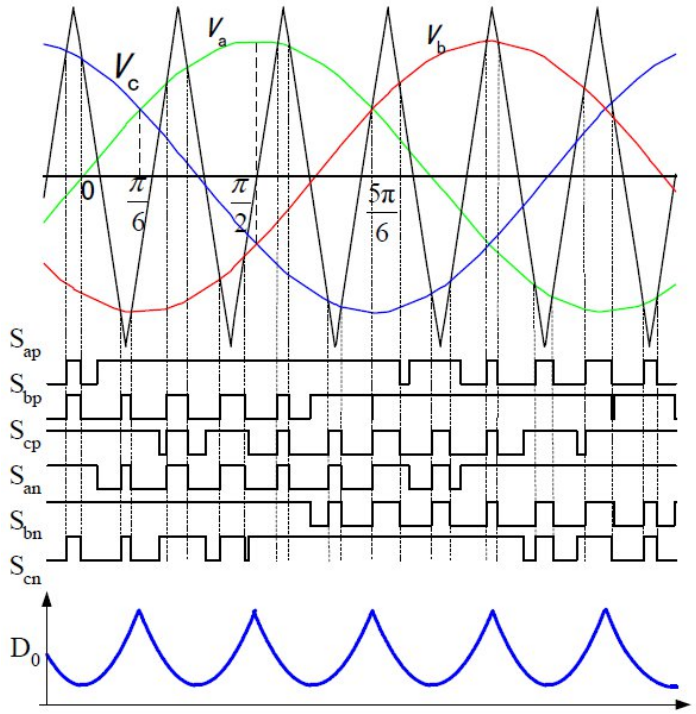

Figure 3.6 Maximum boost control technique

Similar to previous case,

$$\frac{?_?(?)}{?} = \frac{?? ?? ??? ? ? \frac{?}{?}? ??? ? ? ? (? ??? ?? ? ? \frac{??}{?}??? \frac{?}{?}? ??? ? ?)?}{?} \tag{17}$$

Average value of D_0 remains same, when average of above expression is calculated. The voltage gain for same modulation index is identical to the maximum control method for pure sine modulating wave. The graph of volt-gain vs M is displayed in Figure 3.7.

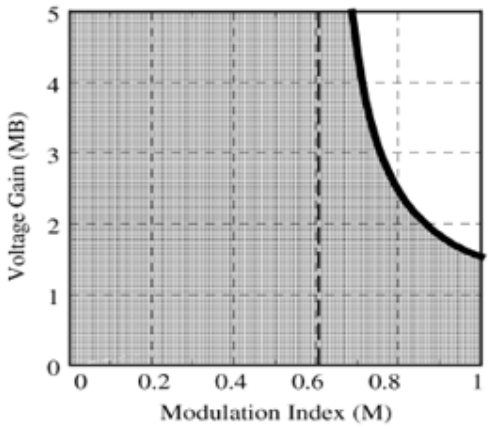

Figure 3.7 Voltage gain vs MI for maximum boost control

3.6 Maximum Constant Boost Control

In maximum boost control the duty cycle varies along a time period and hence it causes a current ripple in the impedance network [23].

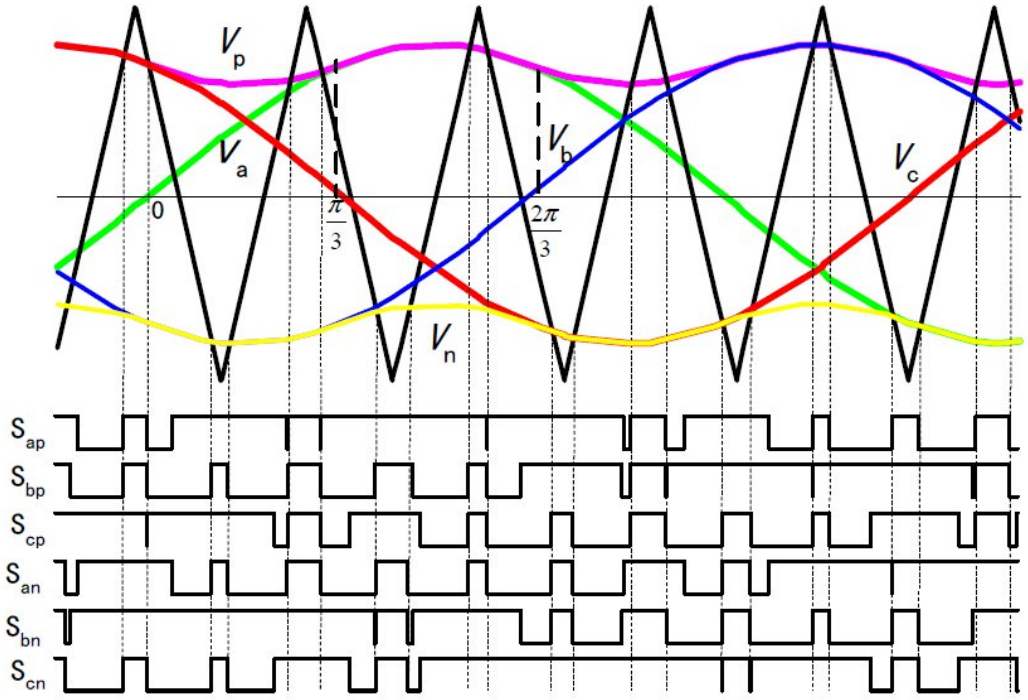

Figure 3.8 : Max-constant-boost control technique

In order to achieve constant voltage gain, the Boost factor B should be kept constant, which in turn is dependent upon shoot through duty-cycle. Main point is to maintain max B even though maintaining it as constant.This is possible by using 2 reference signals, which are 3 times the output frequency and 1/6 times in magnitude, enveloping the three phase voltages as shown in Figure 3.8.

For the first half cycle (0, pi/3) the equation for both the envelopes are:

$$?_{??} = \sqrt{3}? \ + \sin ?? - ?\frac{??}{?}?? ? \qquad 0 < ? < \frac{?}{?} \tag{18}$$

$$?_{??} = \sin ?? - ?\frac{??}{?}?? ? \qquad 0 < ? < \frac{?}{?} \tag{19}$$

And for 2nd ½ cycle

$$?_{??} = \sin(?) ? \qquad \frac{?}{?} < ? < \frac{??}{?} \tag{20}$$

$$?_{??} = \sin(?) ? \ - \sqrt{3}? \qquad \frac{?}{?} < ? < \frac{??}{?} \tag{21}$$

Since distance between two envelopes is constant and equal , so constant D_0 is written as

$$\frac{?_?}{?} = \frac{?? \sqrt{??}}{?} = 1 - \frac{\sqrt{??}}{?} \tag{22}$$

Boost-factor & gain in volt:

$$? = \frac{?}{?? \frac{?? ?}{?}} = \frac{?}{\sqrt{?}? \; ? ?} \quad \text{and} \quad \frac{?_{?}}{\frac{? ?_{?}}{?}} = ? \; ? = \frac{?}{\sqrt{?}? \; ? ?} \tag{23}$$

Gain in voltage is given by: $? = ? \; ? = \frac{?}{?.???? \; ? ?}$ (24)

Switch's volt-stress is given by $V_? = BV_{?} = (\sqrt{3}G - 1)V_{?}$ (25)

3.6.1 Advantages of Z-Source inverter

The advantages of Z source inverter over the traditional VSIandCSI are:

- There is no forbidden state in the Z-Source inverter. The shoot through state which is forbidden in the VSI is used to boost the voltage in the Z source inverter.
- The Z source inverter is more reliable as it is not vulnerable mis-gating caused due to Electromagnetic Interference. Even if mis-gating happens the inverter will be safe and appropriate operating conditions can be maintained by control techniques. In case of VSI or CSI the inverter will be destroyed in the event ofmis-gating.

3.6.2 Applications of Z-Source inverter

1. Z-Source inverter can be used for speed controlled drives.
2. Z-source inverters for fuel cell system with an ultra-capacitor.
3. Z-Source inverter can be used in wind energy generation system.
4. Residential Solar power generation system using Z-source inverter.
5. Z-Source inverter for uninterruptible power supply system.

3.6.3 Limitations of Z-Source inverter

1. In a Z-source inverter voltage is boosted by inserting shoot through state in switching sequences so capacitor voltages are also more than that of input DC voltage, so large capacitors with high rating is required which increases the cost of the system.
2. A huge inrush current exists at the start-up of the Z-source inverter. Z-capacitors initial voltage is zero so during start-up large inrush current charges capacitors to high voltage, after than resonance occurs between inductor and capacitor. Inrush current and resonance can not be suppressed by ZSI which may cause surge in voltage and currents, that may also destroy the devices.

3.7 Three level Z- Source Inverter

In recent years multilevel inverters are gaining attention of researchers and manufactures because of their ability to produce better performance in terms of output waveforms, lesser total harmonic distortion (THD). Three level ZSIs provide a single stage voltage buck-boost operation based energy conversion while retaining all favorable advantages of traditional inverters. ZSI shown in Figure 3.3 uses Z impedance networks for boosting the DC link voltage [34], [35].

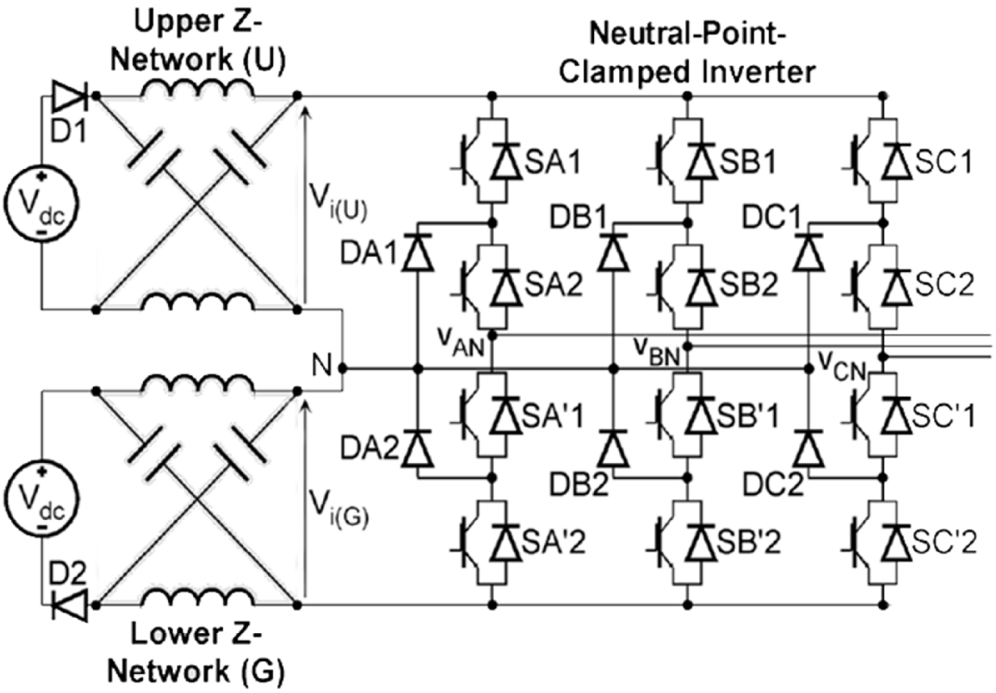

Figure 3.9 Topology of Z-source NPC inverter with two LC impedance networks

Use of two impedance networks shown in Figure 3.9 makes inverter bulky in size and less economical. To make the inverter less bulky a better alternative is to use single passive LC network between input DC voltage source and NPC inverter. Topology of a single impedance based NPC three level ZSI for buck-boost operation is illustrated in Figure 3.10 [13]. Using proper PWM scheme for this inverter voltage can be boosted at all instances, keeping correct volt-sec average, this can be achieved by by only six devices commutation per switching cycle. Thus single impedance network is used over dual Z network based three level NPC inverter.

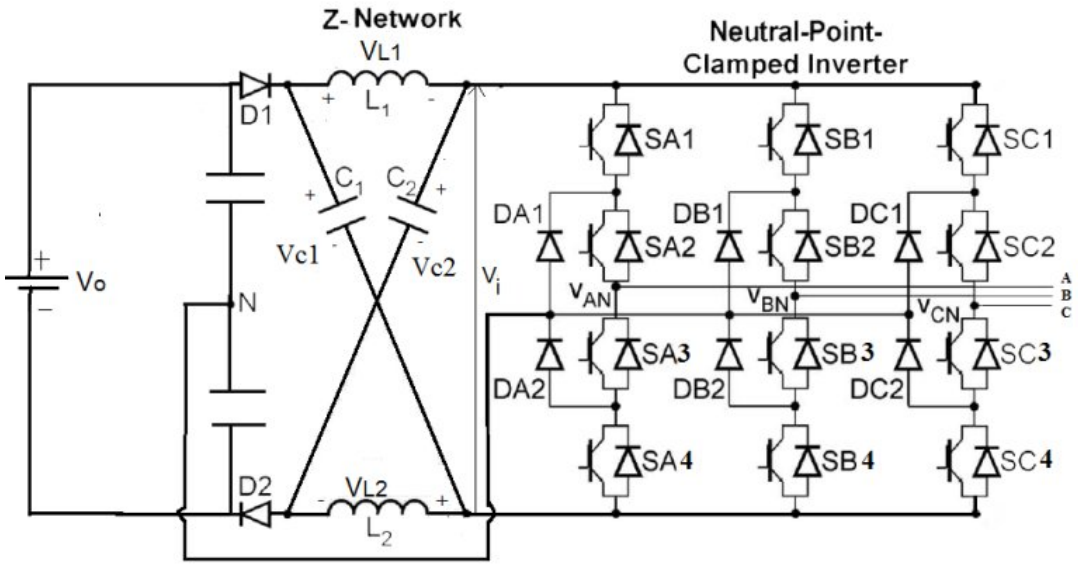

Figure 3.10 Three level NPC ZSI topology using only a single LC impedance network

3.8 Operation principle of Three Level NPC Z-Source inverter

Figure 3.10 illustrates the topology of three level ZSI using a single impedance network, having two capacitors (C_1 and C_2) and two inductors (L_1 and L_2) connected between the input DC voltage source and NPC inverter.

To achieve the buck operation, the pole voltage of ZSI translates between the three distinct voltage levels of $+V_{dc}$, 0 V, $-V_{dc}$ similar to a traditional three phase three level inverter. In order to achieve the voltage boost operation shoot-through state is introduced in the switching sequences. A simple method of introducing the shoot-through state is to turn on all switches of a particular leg simultaneously (e.g., SA1, SA2, SA3, SA4 of phase leg A or SB1, SB2, SB3, SB4 of phase leg B in Figure 3.10) which gives an equivalent circuit with diodes D1 and D2 open circuit as shown in Fiure 3.11(a). Thus ZSI inverter topology does not require dead-time delay for short circuit protection to protect the switches from longer duration of the short circuit current.

3.8.1 Circuit analysis

From the equivalent circuit representation as illustrated in Figure 3.11(a) and for a symmetrical network it is assumed that that inductor voltages $V_{??} = V_{??} = V_?$ and capacitor voltages$V_{??} = V_{??} = V_?$, then the Z-network capacitor and inductor voltages during the shoot-through interval T_0 is expressed as:

$$V_? = V_? \tag{26}$$

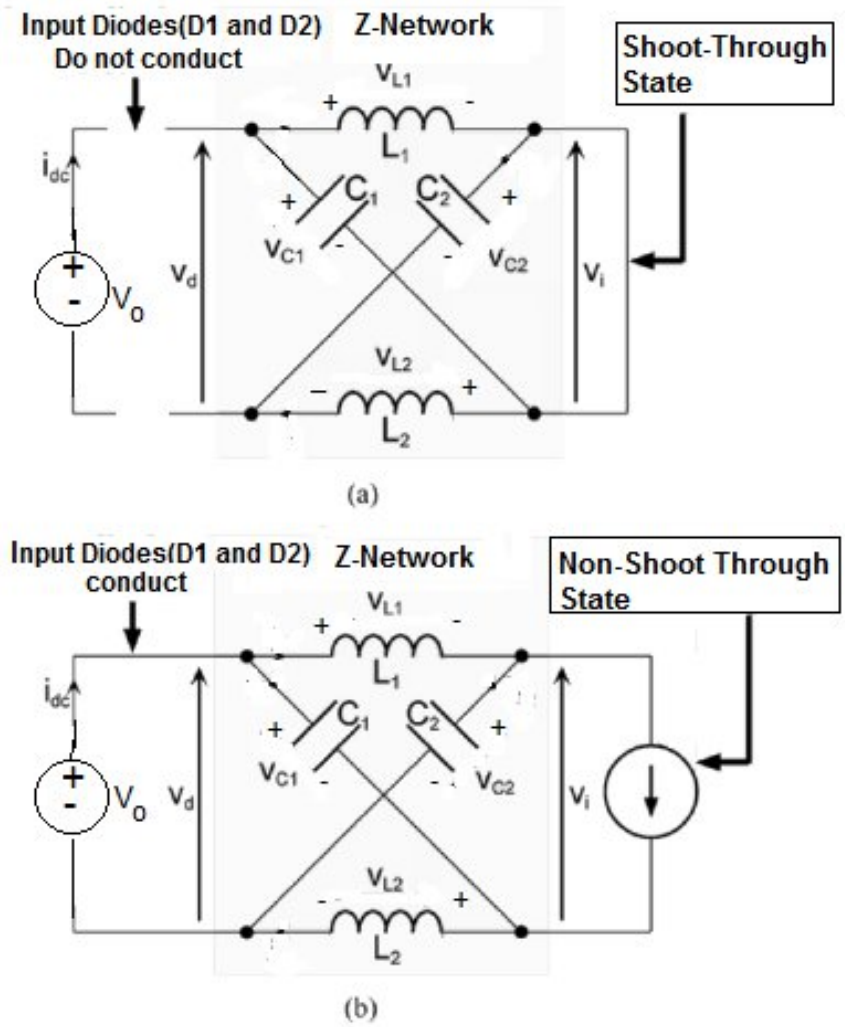

Figure 3.11 The Equivalent circuit representations of single impedance based ZSI during (a) shoot-through state and (b) non-shoot-through state

And during a non-shoot-through interval (T_1), the equivalent illustrated in Figure 3.11(b) comes in operation. During the non- shoot through state inverter circuit and load are treated as current source. From this equivalent circuit, the capacitor voltage and inductor voltage are given as

$$V_? = V_? - V_? \tag{27}$$

Average of $V_?$ for one complete switching cycle T gives

$$\frac{?_?}{?_?} = \frac{?_?}{?_?????} \tag{28}$$

Using equation (29), the DC link voltage (V_i) and the AC output voltage, Vx (x = A, B or C) of the inverter during a non-shoot-through state are given as:

$$V_i = V_? - v_? = 2V_? - V_? = \frac{?}{?? \frac{???}{?}} V_? \quad (29)$$

$$Vx = M.\frac{?_?}{?} = M.\ B_f.\frac{?_?}{?} \quad (30)$$

Where, M is the modulation index and $B_f = \frac{?}{?_?????}$ is the boost factor.

3.8.2 Z- Network parameters calculations

The values of inductor and capacitors can be easily calculated. If the capacitances were to be kept negligible and a current source is used, then the circuit reduces to that of traditional CSI with 2 source inductors, so the worst case inductor requirement will be equal to that of a CSI. Similarly, if the inductances are negligible and a DC Voltage source is used then the circuit reduces to that of a traditional VSI, so the worst case capacitor requirement will be equal to that of a VSI. However, appropriate values of inductance and capacitance can be calculated as follows:

3.8.2.1 Inductor Design

During shoot-through-mode, inductor's job is to limit current-ripple. When circuit is operating in shoot-through state then inductor-current increases linearly and voltage across each inductor is same as average voltage of capacitor i.e. V_{C1}. During non-shoot mode, inductor's current decreases linearly and voltage of inductor changes between V_{in} and V_{C1}. Average inductor current through each inductor for a system of power-rating P can be expressed as:

$$I_{Lav} = I_{L1av} = I_{L2av} = P/V_{in} \quad (31)$$

Maximum current ripple is present during the process of maximum shoot-through state. So peak-to-peak inductor current ripple is considered for the purpose of design consideration. For most cases, maximum of 30% current-ripple is chosen for the purpose of design. So the value of maximum and minimum current through inductor can be given by expression (32)

Inductor max-current (I_{Lmax}) = I_{Lav} + 30% of I_{Lav} and $_{Inductor}$ min-current (I_{Lmin}) = I_{Lav} - 30% of I_{Lav} (32)

Possible value of inductor can be found using equation (33)

$$L = V_L(*T_0/\Delta I_L) \quad (33)$$

Where, $V_L = V_{C1} = V_o \frac{????}{????}$ and $\Delta I_L = I_{Lmax} - I_{Lmin}$

3.8.2.2 Capacitor Design

The Z- network capacitor absorbs current-ripple caused by shoot through state and provides a stable voltage which is crucial for sinusoidal output voltage. During shoot through mode of operation Z network capacitors charges by a current at this moment $I_L = I_C$. Considering a permissible voltage-ripple (ΔVC) to around 3% - 5% at peak-power, the capacitor value can be estimated using expression (34).

$$C = I_{Lav} * (T_0 / \Delta V_C) \text{ , Where, } \Delta VC \text{ is 5\% of } V_{C1} \quad (34)$$

CHAPTER 4: CONTROL TECHNIQUES OF MULTILEVEL Z-SOURCE INVERTER

For multilevel inverters, multicarrier PWM is used to generate gatting signals for switching devices. This involves comparison of modulating signal, sinusoidal signals with several carrier signals typically triangular signals. Carrier signals used are of same magnitude but vertically disposed and may have phase shift with respected to other carrier signals depending upon the PWM scheme.

4.1 PWM schemes that can be used for controlling a Three level NPC Z-Source Inverter

1. Modified Alternative Phase Opposition and Disposition (APOD)
2. Modified Phase opposition Disposition (POD)
3. Modified Phase Disposition (PD)

4.1.1 Modified Alternative Phase Opposition and Disposition Scheme (APOD)

In generic APOD scheme a set of three phase sinusoidal references are compared with two vertically disposed and 180º phase shifted triangular carriers to produce switching signals for two switches of same leg(e.g. SA1 and SA2, in Figure 3.5) and their NOT signals are used for other two switches(e.g. SA3 and SA4, in Figure 3.5). Traditional PWM technique shown in Figure 4.1 can also be used for three level ZSI but it can be used only for buck operation. APOD based modulation technique for controlling the three level ZSI is discussed in [13]. To introduce the required shoot-through interval in the inverter switching state, it is ensured that in all switching instances correct volt-sec average is synthesized. Considering this criterion, the feasible state sequence to control a traditional three level inverter is illustrated in Figure 4.1. In this figure the two triangular carriers which are vertically disposed and have 180º phase shift are used to form the APOD carrier placement arrangements. In addition with two triangular carriers, three sinusoidal reference signals are also required to carry out the comparison of sinusoidal references with the triangular carriers to generate gating signals for two independent switches of a particular leg (SA1 and SA2 of phase leg A). While remaining Complementary switches of that particular leg (SA3 and SA4 of phase leg A) are driven by logically NOT signals, as it is reported in Figure 4.1. From the generated switching state sequence as reported in Figure 4.1, it can be observed that in APOD based three level NPC inverter, state{0,0,0} is always present in the switching state sequence. So partially replacing the zero state with the shoot-through state as illustrated in Fig4.2 will provide the required boost in the DC link voltage of ZSI.

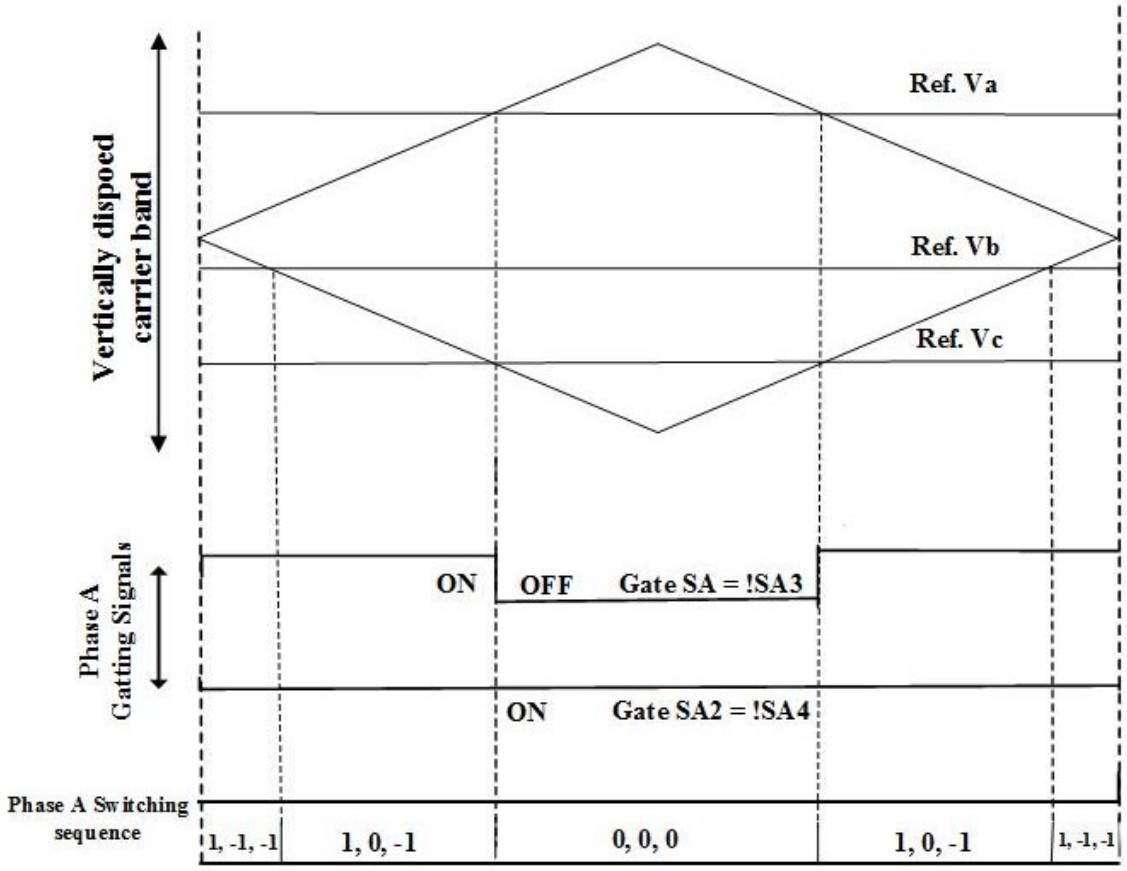

Figure 4.1 APOD modulation for traditional three-level inverters

In Figure 4.2 it can be observed that the two reference signals $V_{a(SAU)}$ and $V_{c(SCL)}$), is used to insert the shoot-through state by modifying the switching on time of switches SA1 and SC4. The original reference signals V_a and V_c (renamed as $V_{a(SAL)}$ and $V_{c(SCU)}$, Figure 4.2) are used to control the termination of shoot-through state by turning off the switches SA3 and SC2. A vertical offset of T0/T is added to the reference V_a and same offset is subtracted from reference, V_c to generate the additional references $V_{a(SAU)}$ and $V_{c(SCL)}$.This reference generation process is generalized by subtracting the vertical offset of T_0/T from the "minimum" reference (V_{min}= min(V_a,V_b,V_c) while adding the offset T_0/T to the "maximum" reference (V_{max}=max(V_a,V_b,V_a) to get the required references needed to control the ZSI. In this reference generation process (V_{mid} = mid(V_a,V_b,V_c)=) is not modified.

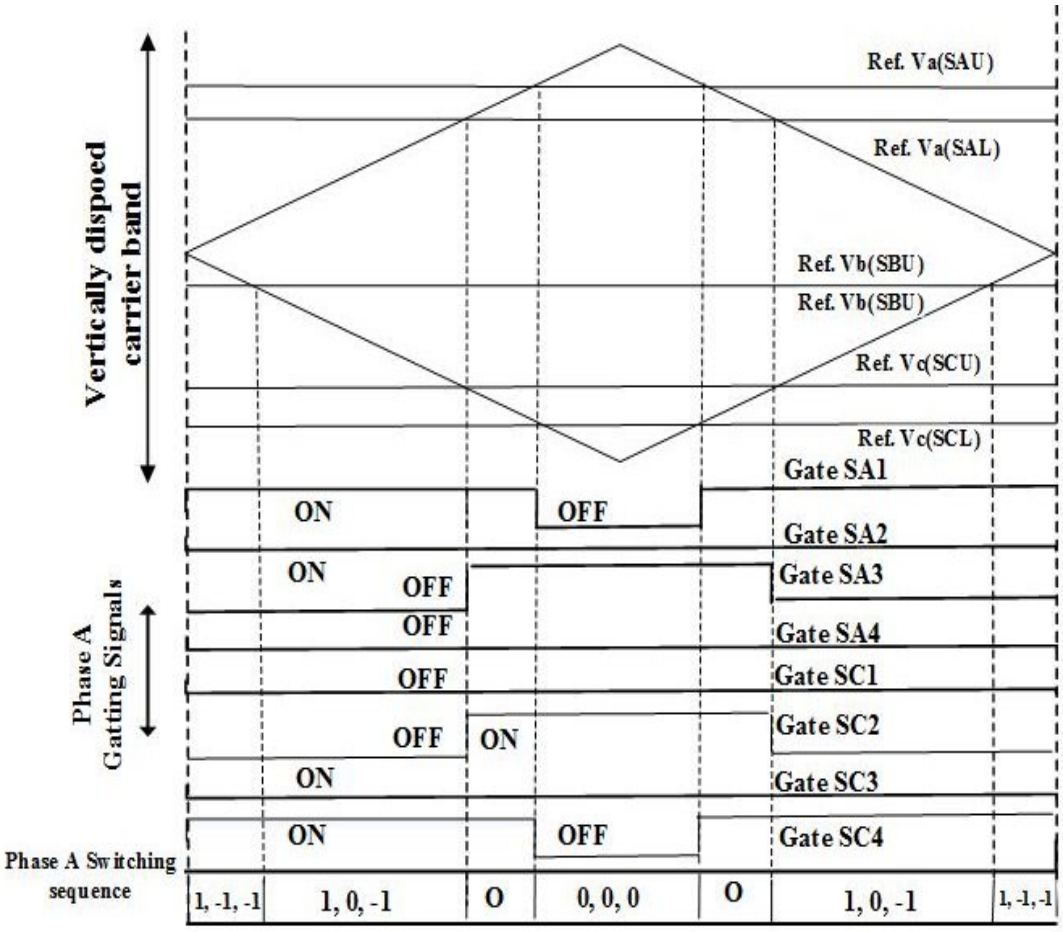

Figure 4.2 APOD modulation for three level ZSI

A triplen offset (V_{offset}) given by equation (35) is properly added to the required three original sinusoidal references, so that the resulting references are centered vertically within the disposed triangular carrier bands, thus give a synchronized gating signal for phase A and phase C. On adding offsets to all original sinusoidal references, the resulting set of required references to control the single impedance network based NPC three-level ZSI is given as:

$$V_{max(SXU)} = V_{max} + V_{offset} + T_0/T$$

$$V_{max(SXL)} = V_{max} + V_{offset}$$

$$V_{mid(SXU)} = V_{mid} + V_{offset}$$

$$Vmid_{(SXL)} = Vmid + V_{offset}$$

$$Vmin_{(SXU)} = Vmin + V_{offset}$$

$$Vmin_{(SXL)} = Vmin + V_{offset} - T_0/T$$

$$V_{offset} = -0.5(\max(V_a,V_b,V_c) + \min(V_a,V_b,V_c)) \quad (35)$$

where X= A, B, or C; U= 1 and 2; L= 3 and 4 (36)

4.2 Modified APOD modulation scheme developed in Matlab/Simulink environment

Figure 4.3 shows the model of APOD control scheme for three level NPC ZSI developed in Matlab environment. Three sinusoidal reference signals are used to generate modified reference signals as discussed in section 4.1.1. These modified reference signals are then compared with two carrier signals (C1 and C2, shown in figure 4.3) to generate switching sequences for all switches.

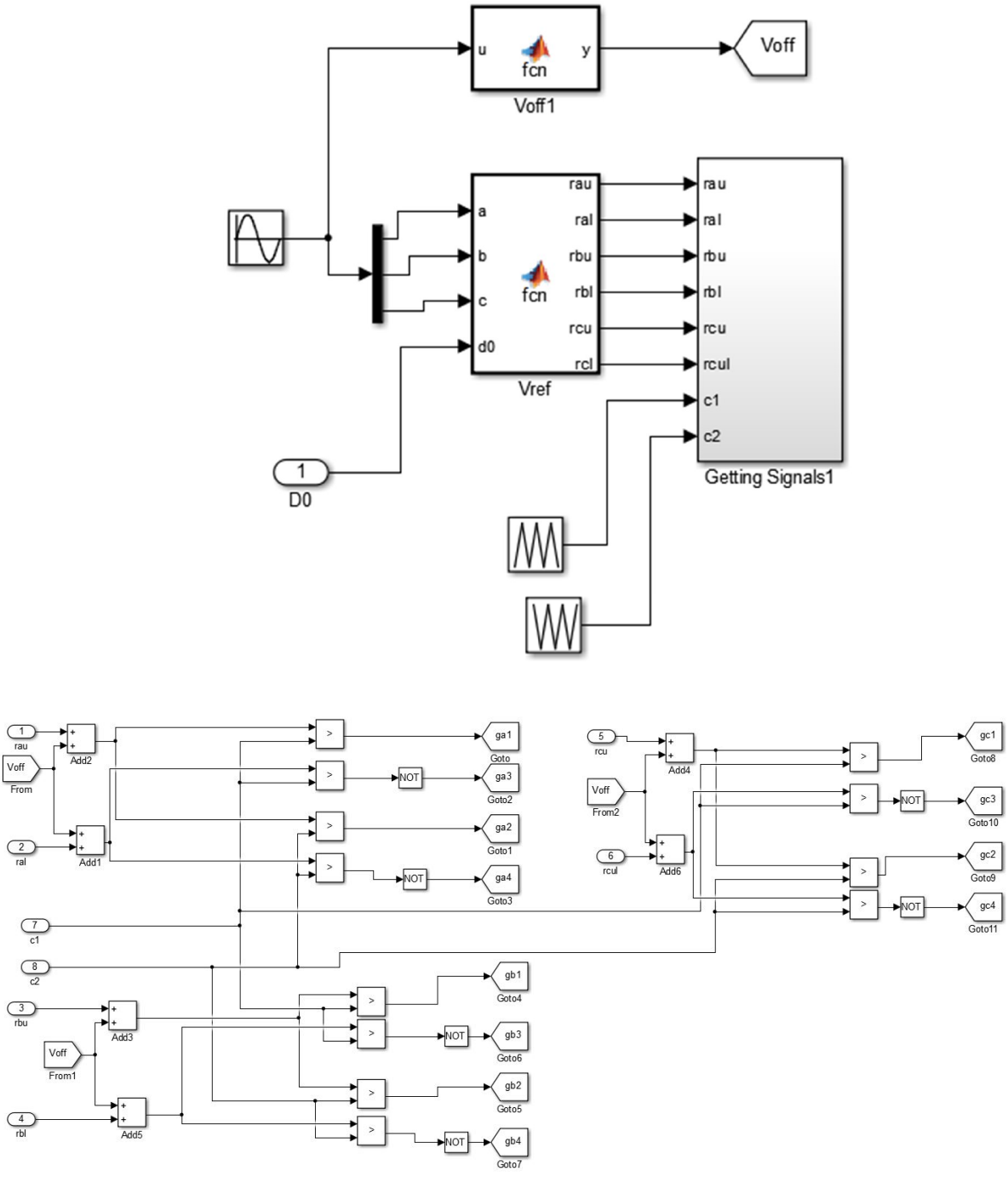

Figure 4.3 Matlab Model of Modified APOD modulation scheme

4.3 Unified voltage control technique for three level ZSI for PV generation system using modified APOD modulation scheme

In a traditional MPPT technique the MPPT controller directly controls the shoot-through interval and accordingly reference signals can be generated as per expression discussed in section 4.1.1. The Z-network capacitor voltage level is boosted as per the generated shoot-through time period, calculated by the MPPT controller. It is not possible to increase capacitor voltage beyond MPP voltage of PV panel, as the generated shoot-through states can only track the MPP voltage. So, the traditional MPPT algorithms can not boost Capacitor voltage beyond MPP voltage value. Figure 4.4(a) illustrates the operating principle of a traditional MPPT controller for a Z-source inverter based PV power conversion system (PCS).

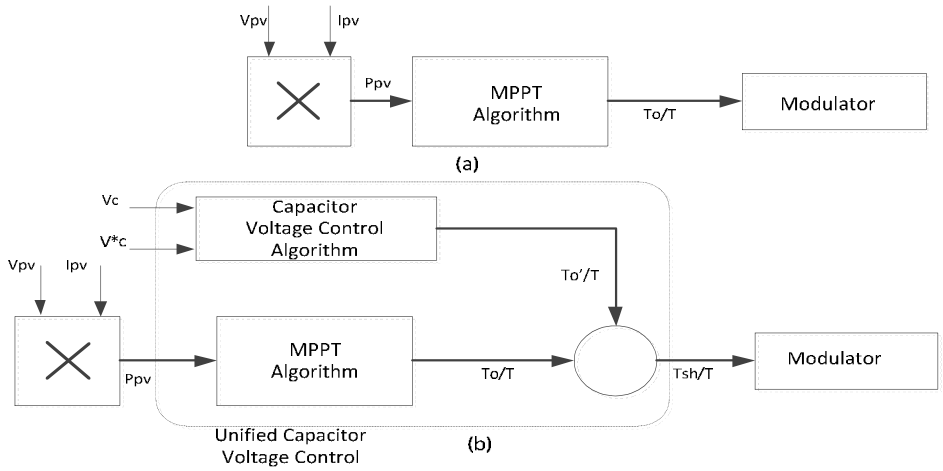

Figure 4.4 ZSI based PV-PCS capacitor voltage control mechanism (a) Traditional MPPT controller (b) Unified voltage controller

Figure 4.4 (b) shows a unified voltage control technique which tracks the MPPT and also achieves the desired capacitor voltage control. In this MPPT technique an extra shoot period, (T'_0) is generated to increase Z-network capacitor voltage beyond maximum power point voltage of PV panel. The extra generated shoot through interval (T'_0) is added to the MPPT generated shoot-through period (T_0) to obtain the total shoot through time period (T_{sh}). The flowchart of unified control technique is shown in Figure 4.5, which tracks the MPPT and also maintains the desired Z-network capacitor voltage.

There are two stages in the flowchart of the unified voltage control technique, shown in Figure 4.5. The first stage of the flowchart generates the shoot through time period (T_0) to track the MPPT by

boosting the capacitor voltage level to the MPP voltage level while the second stage of the flowchart generates extra shoot through time period to provide the required boost in the Z-network capacitor voltage beyond MPP voltage level, if required. By adjusting the shoot-through time period, the inverter DC link voltage can be maintained to the desired voltage level by controlling the Z-network capacitor voltage. Perturb and Observe (P&O) MPPT technique is employed to extract the maximum power from the PV panel [31]. In P&O algorithm, the output power of PV panel is continuously measured and change in power is observed and accordingly shoot-through time period is adjusted to achieve the MPP voltage. The Z-network capacitor voltage is also updated accordingly till capacitor achieves the MPP voltage, (V^*_{PV}) and thus maximum power is extracted from the PV array. Equation (11) can be expressed as follow:

$$V_i = \frac{?}{?? \frac{???}{?}} ?_{??} = V^*_{PV} \tag{37}$$

Using MPPT technique Z-network capacitor voltage is raised to MPP voltage level. After achieving the MPP voltage the actual Z-network capacitor, (V_c) is compared with the desired/reference capacitor voltage, (V^*_C) which decides the ZSI DC link voltage level. If it is found that the reference capacitor voltage is same as the actual capacitor voltage (i.e. $V_C=V^*_C$) then no extra shoot-through period (T'0) is required. If MPP voltage is achieved but Z-network capacitor voltage requires further boost to achieve the desired voltage level (i.e. $V^*_C>V_{C)}$, then an extra shoot-through time period (T'_0) is obtained shown in Figure 4.5, which is added to the shoot-through time period T_0 , obtained from P&O MPPT algorithm. Similarly to step-down the Z-network capacitor voltage(i.e. $V^*_C<V_C$), then the extra shoot-through time period (T'_0) is subtracted from the MPPT generated shoot-through time period (T_0) and the required total shoot-through time period (T_{sh}) is obtained. Thus in this way total shoot-through time period (T_{sh}) achieves simultaneous control of the MPP voltage along with the Z-network capacitor voltage. The expression for the total shoot-through time period (T_{sh}) is as follow:

$$T_{sh} = T_0 \pm T'_0 \tag{38}$$

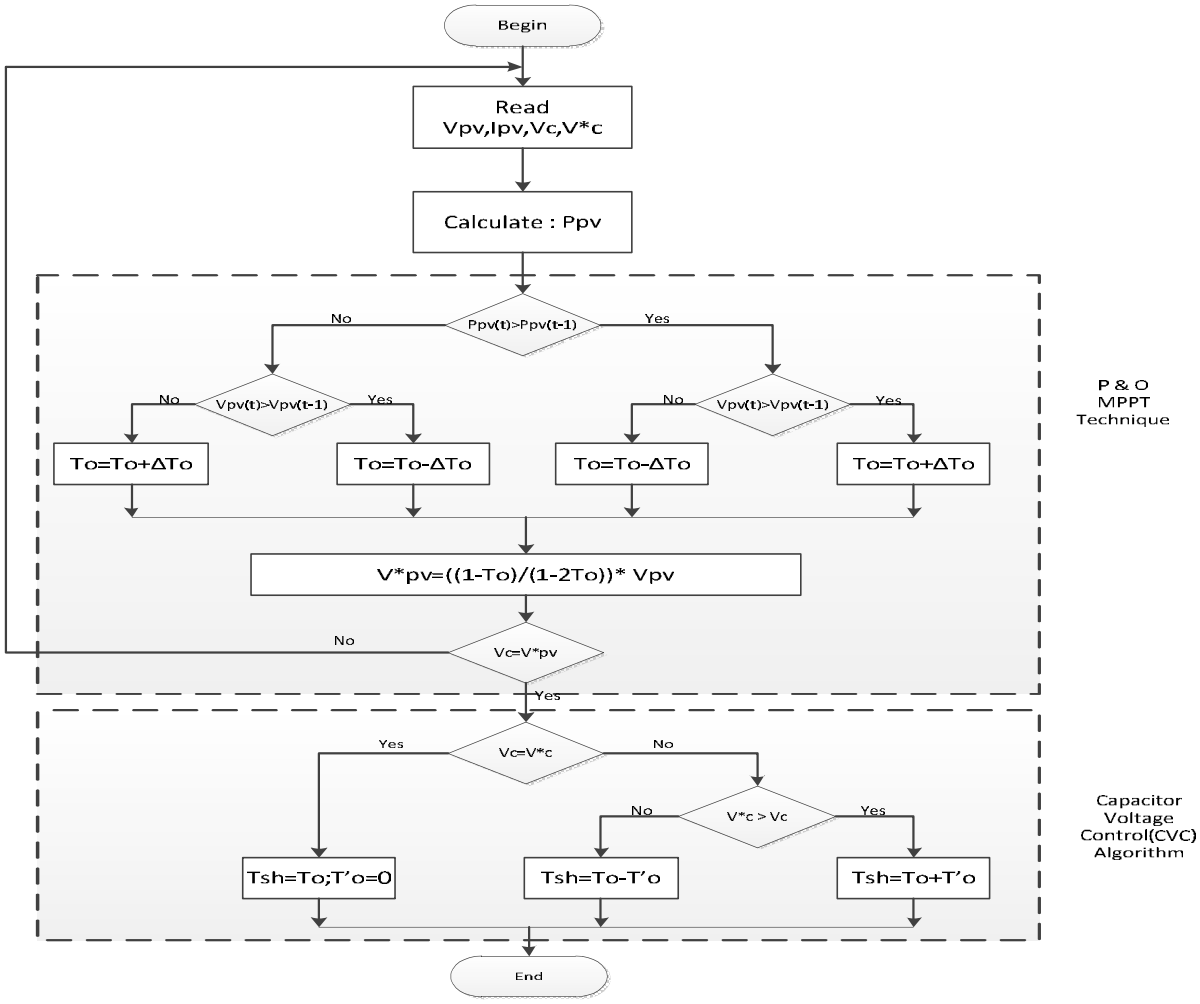

Figure 4.5 Flowchart of unified control technique

Where, T_0 gives MPP capacitor voltage (V^*_{PV}), and T'_0 controls the Z-network capacitor voltage (V_C) as per the reference capacitor voltage (V^*_C). The possible range of the total shoot-through time period T_{sh}, is given by:

$$T_{sh}/T \leq (1-M) \tag{39}$$

The range of additionally required shoot-through duty ratio ($D'_0 = T'_0/T$) is limited by the modulation index (M) and the MPPT generated shoot-through duty ratio ($D_0 = T_0/T$). By substituting equation (8) into (3) the average value of Z-network capacitor voltage and the ZSI DC link voltage are expressed as follows:

$$V_c = \frac{?\,?\,(\frac{?\,?\pm?\,??}{?})}{?\,?\,?\,(\frac{?\,?\pm?\,??}{?})} V^*_{PV} = \frac{?\,?\,(\frac{?\,??}{?})}{?\,?\,?\,(\frac{?\,??}{?})} = V^*_{PV} = \frac{?\,?\,?\,??}{?\,?\,?\,??\,??} V^*_{PV} \tag{40}$$

The peak AC output voltage of the ZSI is expressed as:

$$V_{ac} = M?\frac{???_{??}}{??\,??\,_{??}}?V^{*}_{PV} = M.\frac{???}{?} \quad (41)$$

4.4 Conclusion

In this chapter modified APOD control scheme to control the NPC three level ZSI is discussed in details. MALAB model of APOD control scheme is also presented.

CHAPTER 5: BIDIRECTIONAL BUCK-BOOST BATTERY SYSTEM

Before describing the battery charging system, the terminology associated with the battery charging system is reviewed here first.

5.1 Definitions

5.1.1 Battery Condition

- **State of Charge (SOC)**: This is the amount of charge in the battery as compared to its maximum capacity, generally expressed in percentage.
- **Terminal Voltage**: The voltage across the terminals of the battery on supplying a particular load.
- **Open-Circuit Voltage**: The voltage across the terminal at no-load.
- **Internal Resistance**: The inherent resistance of the battery which is also a measure of its deviation from an ideal voltage source. This is different while charging and discharging and is also dependent on the state of charge of the battery.

5.1.2 Battery Specifications

- **Nominal Voltage**: This is the generally reported reference voltage of the battery.
- **Cut-off Voltage**: The minimum voltage that's allowed for safe operation of the battery. Operating the battery beyond this point is hazardous to the health of the battery and corresponds to 10 percent SOC.
- **Fully Charged Voltage**: The maximum voltage of the battery corresponds to the 100 percent SOC.
- **Charge Current**: The maximum allowable charging current for the battery and also the one it is generally charged at.

5.2 Control Strategy for BESS

Solar energy is directly proportional to irradiation which fluctuates continuously so does the power. The demand-generation mismatch can be minimised by using the bidirectional buck-boost battery storage system. The operation of battery energy storage with respect to generation-demand can be explained in Figure 5.1. During over-generation conditions ($P_{\_PV}>P_L$, where $P_{\_PV}$ is power generated by PV panel and P_L is load power demand), the power output of PV panel is greater than the load demand. In this case, the gate g1 will be high and turns ON the MOSFET and the additional power will be used to charge the battery. This mode is called as the charging mode or the Buck mode. In case of under-generation situations ($P_{\_PV}<P_L$), the power output of PV panel is less than the load

demand. The gate g2 will be high and turns ON the MOSFET. Consequently, the battery together with the PV panel starts supplying power to overcome the load demand. This mode is called as the discharging mode or the Boost mode. Thus overall output power will be almost constant as shown in Figure 5.1. Furthermore, Nickel-Metal-Hydride battery is chosen as the capacity of battery is sufficient enough to meet the demand-generation mismatch. Table 5.1 shows the parameters of the battery considered.

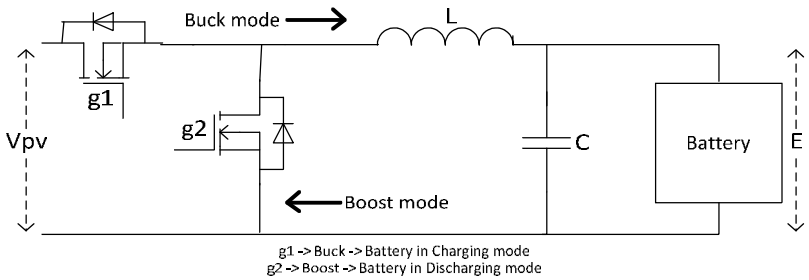

Figure 5.1 Bidirectional buck-boost system

Figure 5.2 shows the model for control of bidirectional buck-boost BESS in Matlab environment.

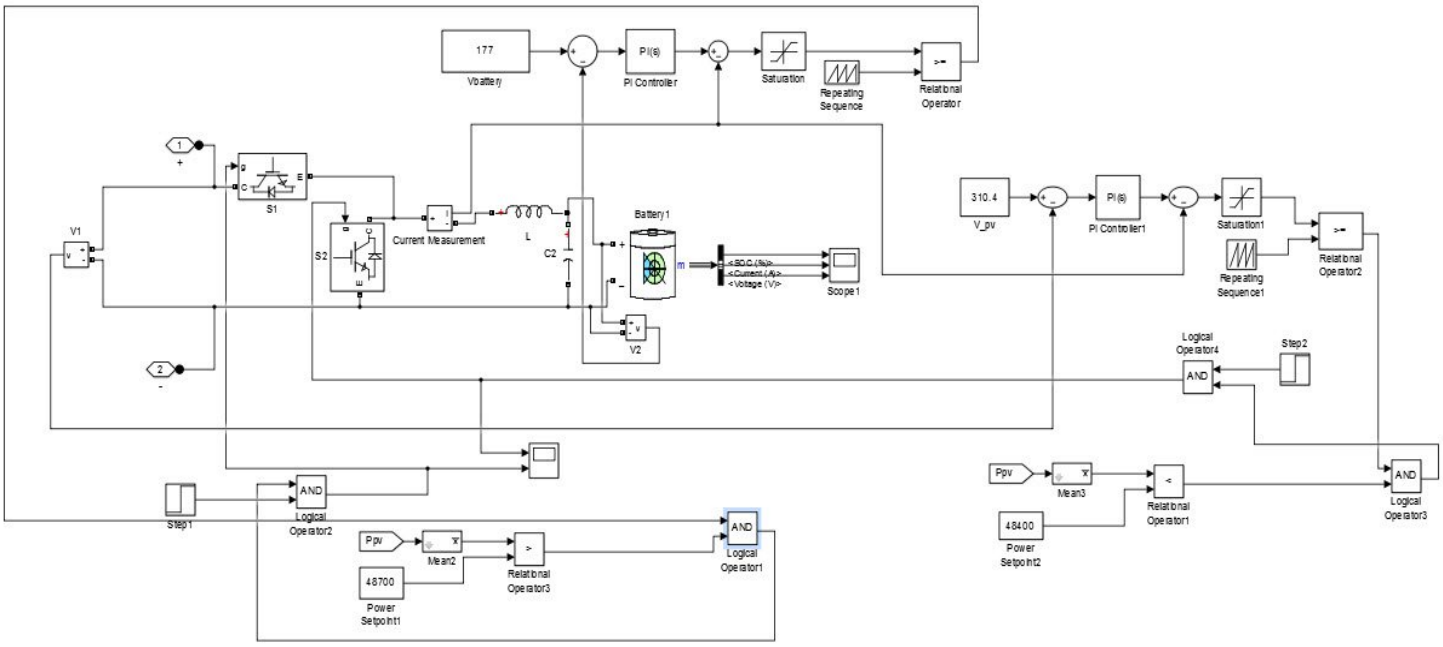

Figure 5.2 Matlab model of Bidirectional buck-boost battery system

Table 5-1 Battery parameters (Nickel-Metal-Hydride)

IGBT/Diode parameters	Values
Nominal Voltage(V)	150
Rated Capacity(Ah)	0.5
Initial State-Of-Charge (%)	50
Maximum Capacity (Ah)	0.53846
Fully Charged Voltage (V)	176.6949
Internal Resistance (Ohms)	3

CHAPTER 6: 3-LEVEL Z-SOURCE INVERTER BASED PV SYSTEM WITH BIDIRECTIONAL BUCK-BOOST BESS

A three level NPC ZSI using single impedance network is studied for photovoltaic application with bidirectional buck-boost BESS. The DC output voltage of PV panel is boosted to desired voltage level and converted into AC, so as to feed the AC load may be standalone. The effect of variation of irradiance and temperature is studied by carrying out the simulation work in the MATLAB/SIMULINK environment.

6.1 Simulations of NPC Three level Z-Source Inverter

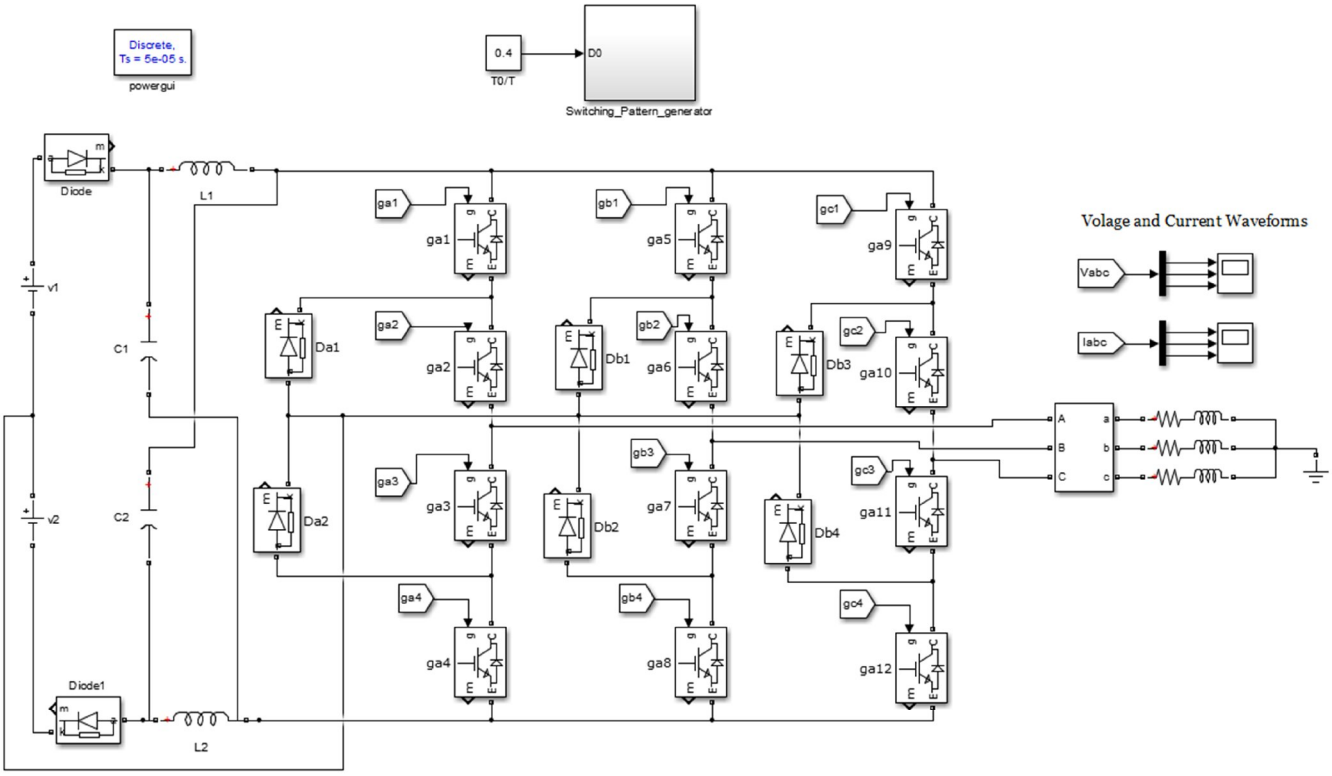

Figure 6.1 Simulink Model of NPC Three Level ZSI using single impedance network.

Table.6-1 The Simulation parameters choosen for NPC three level ZSI

Input DC Voltage	100V
Z-Network capacitor C1 =C2	1mF
Z-Network Inductor L1 = L2	1mH
Switching Frequency	5KHZ

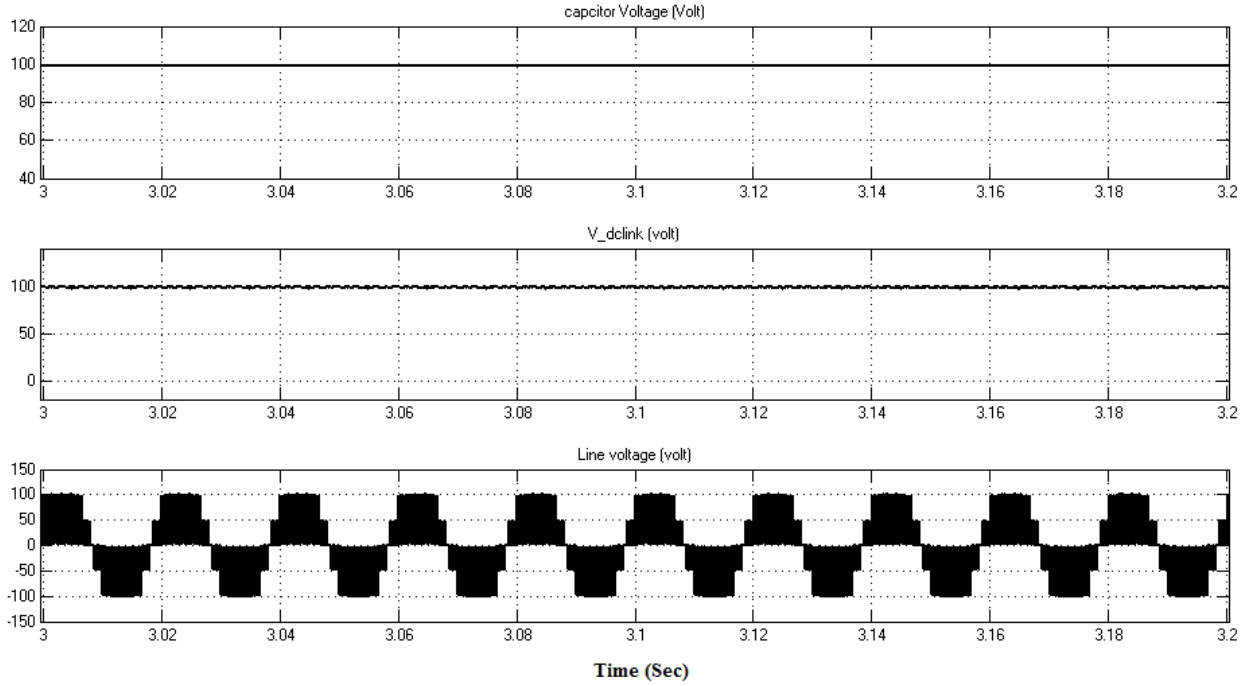

Figure 6.2 Simulation Result of NPC Three Level ZSI with D = 0 at no load condition

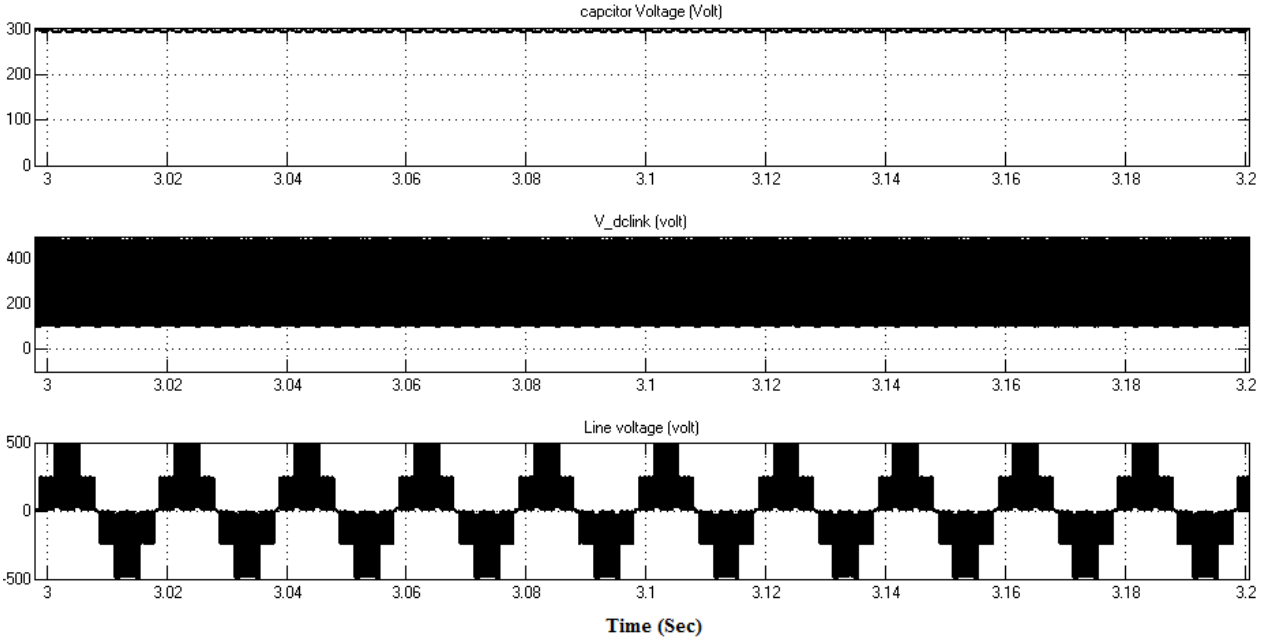

Figure 6.3 Simulation Result of NPC Three Level ZSI with D = 0.4 at no load condition

Figure 6.3 shows that for zero shoot through three level behaves like traditional three level inverter. If we insert a shoot through of duty ratio D=0.4, output voltage is boosted 5 times as per theoretical value.

6.1.1 Simulation with R load

With Resistive load of 10 kW, 500V

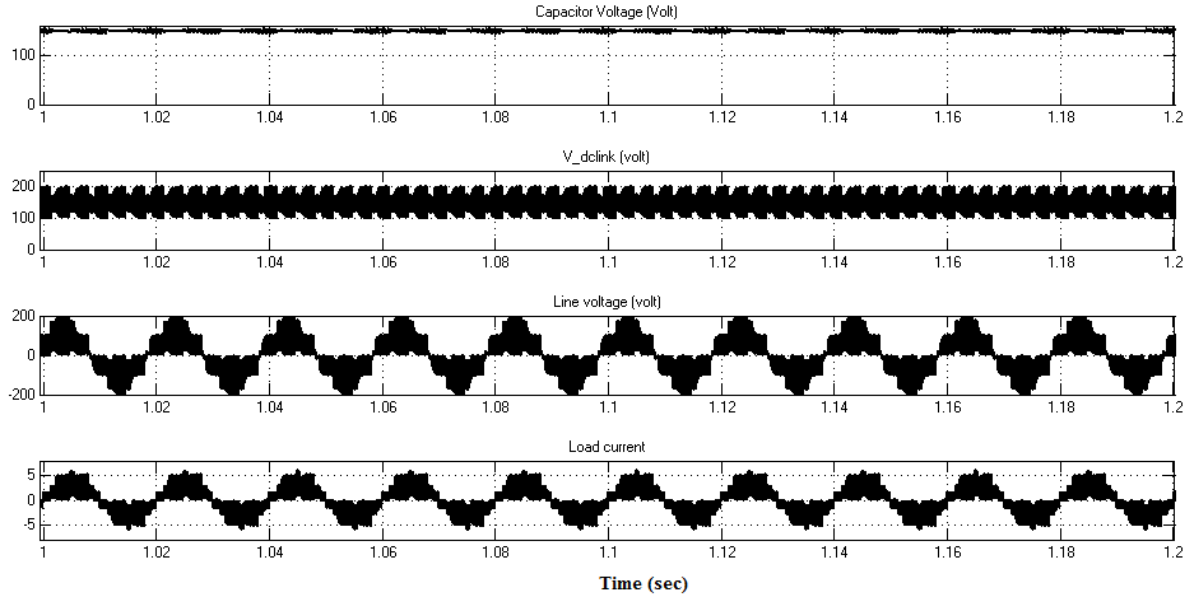

Figure 6.4 Simulation Result of NPC Three Level ZSI for D = 0.3 with R Load

6.1.2 Simulation with R-L load

With load of 10 kW, 10VAR, 500 V

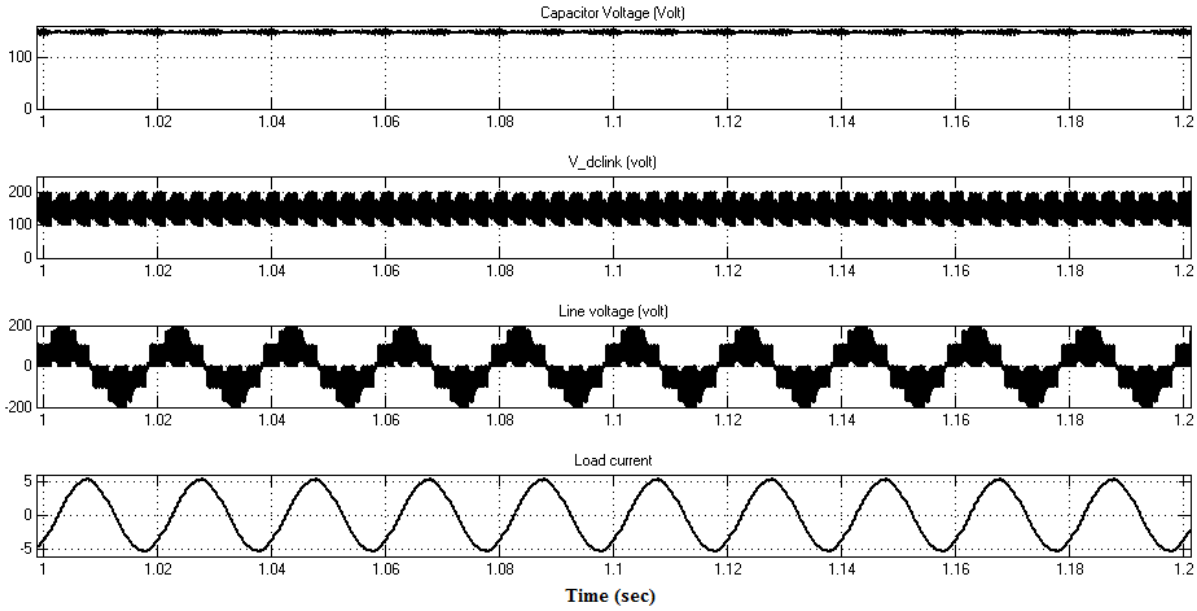

Figure 6.5 Simulation Result of NPC Three Level ZSI for D = 0.3 with R-L Load

6.2 Operation of NPC Three level ZSI for Standalone PV generation System

Simulation of NPC Three level Z-source for standalone PV generation system is carried out for open loop and closed loop system is carried. MPPT technique along with Z-network capacitor voltage control is also implemented in MATLAb environment. P&O algorithm is used to track the MPPT of PV panel.Specifications of PV panel used is listed in Table 5.2. Simulation results are obtained under different environmental conditions.

Table 6-2 Specifications of PV panel

(Module type: SunPower SPR-330-WHT)

Parameters	Values
No. of cells per module	96
No. of series-connected modules per string (Nser)	5
No. of parallel strings (Npar)	30
Open circuit voltage Voc (V)	64.2
Short-circuit current Isc (A)	5.96
Voltage at maximum power point Vmp (V)	60.3
Current at maximum power point Imp (A)	5.50

Three level ZSI parameters:

Z Network capacitor (C1= C2) = 10mf

Z Network Inductor (L1 = L2) = 0.1mH

Switching Frequency = 5kHZ

6.2.1 Simulation of Open Loop Three Level ZSI for Standalone PV system

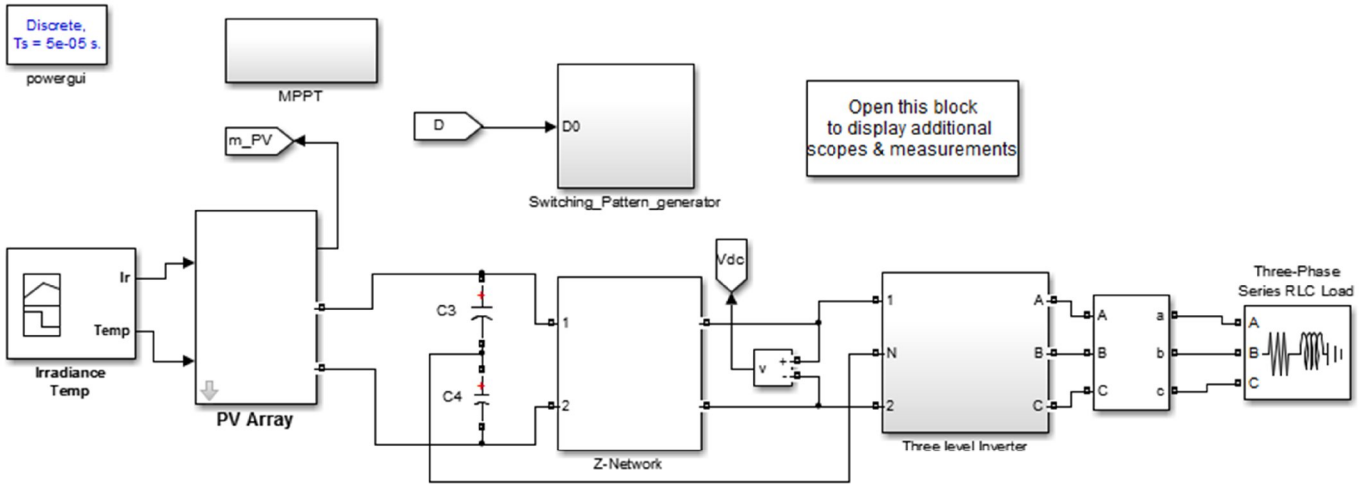

Figure 6.6 Simulink Model for open loop PV System

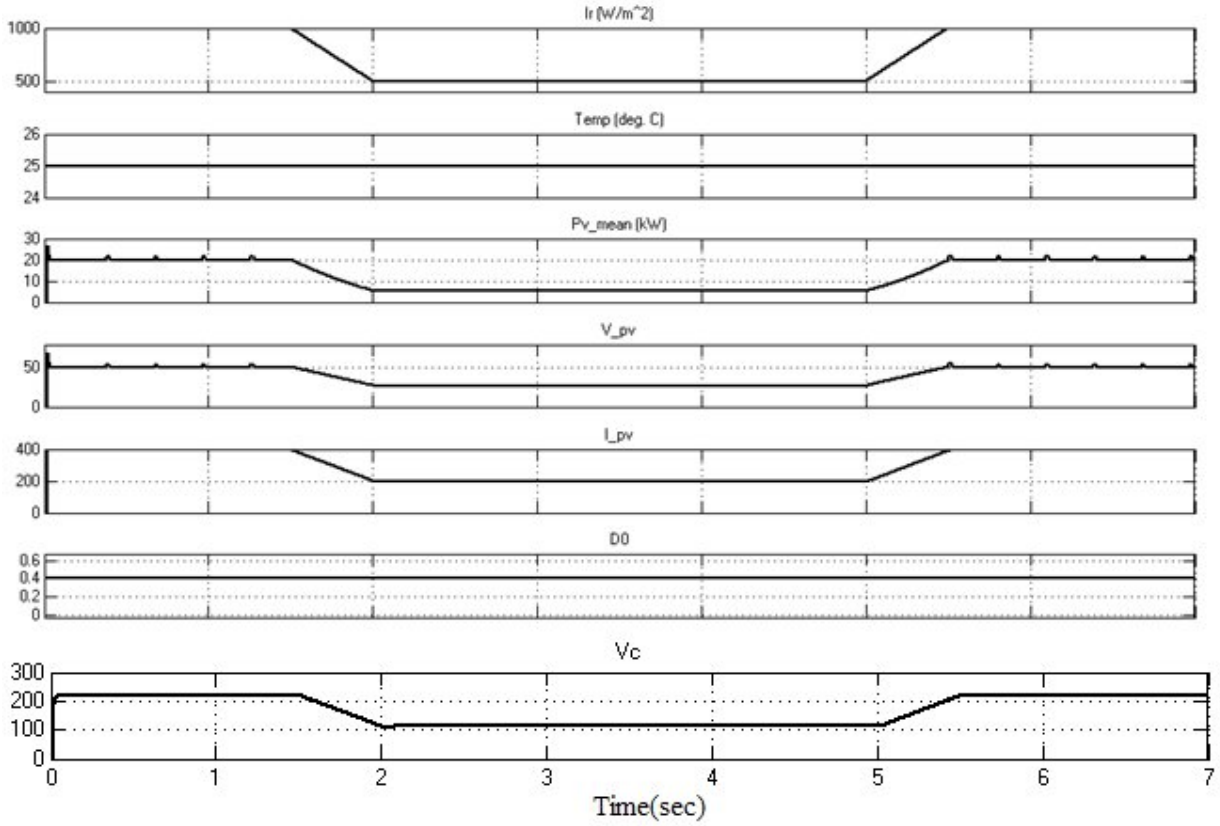

Figure 6.7 Simulation Result for Open Loop PV system without MPPT(Constant shoot through, D0=0.4) under varying environmental condition

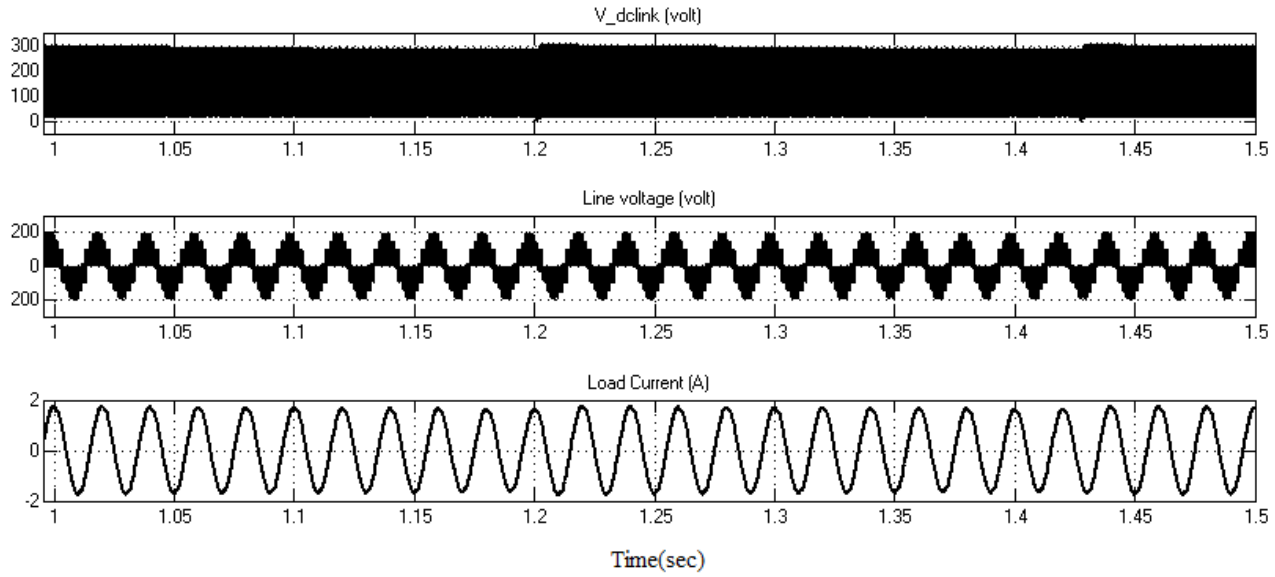

Figure 6.8 Inverter Output without MPPT when Irradiance is 1000W/m^2

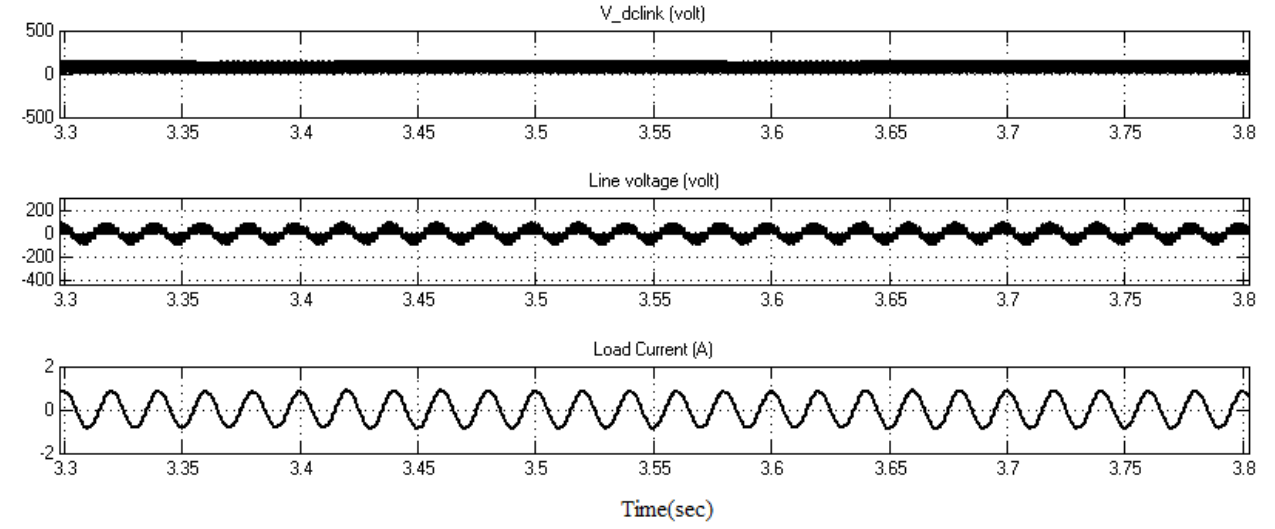

Figure 6.9 Inverter Output without MPPT when irradiance falls to 500W/m^2

In Figure 6.7.upto 1.5 second irradiance is 1000 W/m^2 so PV panel is able to give maximum power event without MPPT as load connected is 15 kW, lesser than output power of PV panle, but when irradiance falls to 500W/m^2 PV output power fall below 10 kW, shown in Figure 6.7. If MPPT technique is used power delivered by PV panel for 500W/m^2 is around 15kW, Figure 6.8 thus giving maximum power corresponding to 500W/m^2 irradiance level. Figure 6.9 show that if environmental

conditions remains same and load connected is lesser than PV output poer then PV panel is always able to deliver maximum power MPPT does not come in picture.

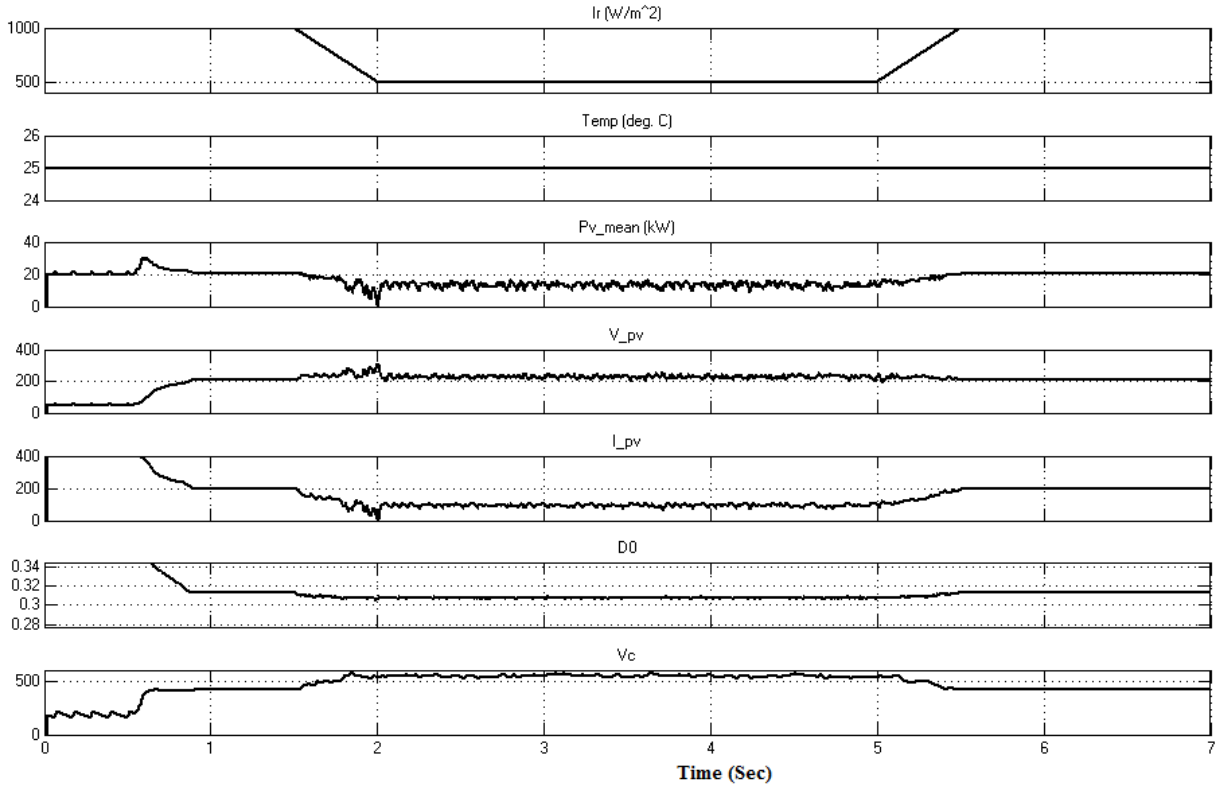

Figure 6.10 Simulation Result for Open Loop PV system With MPPT under varying environmental condition

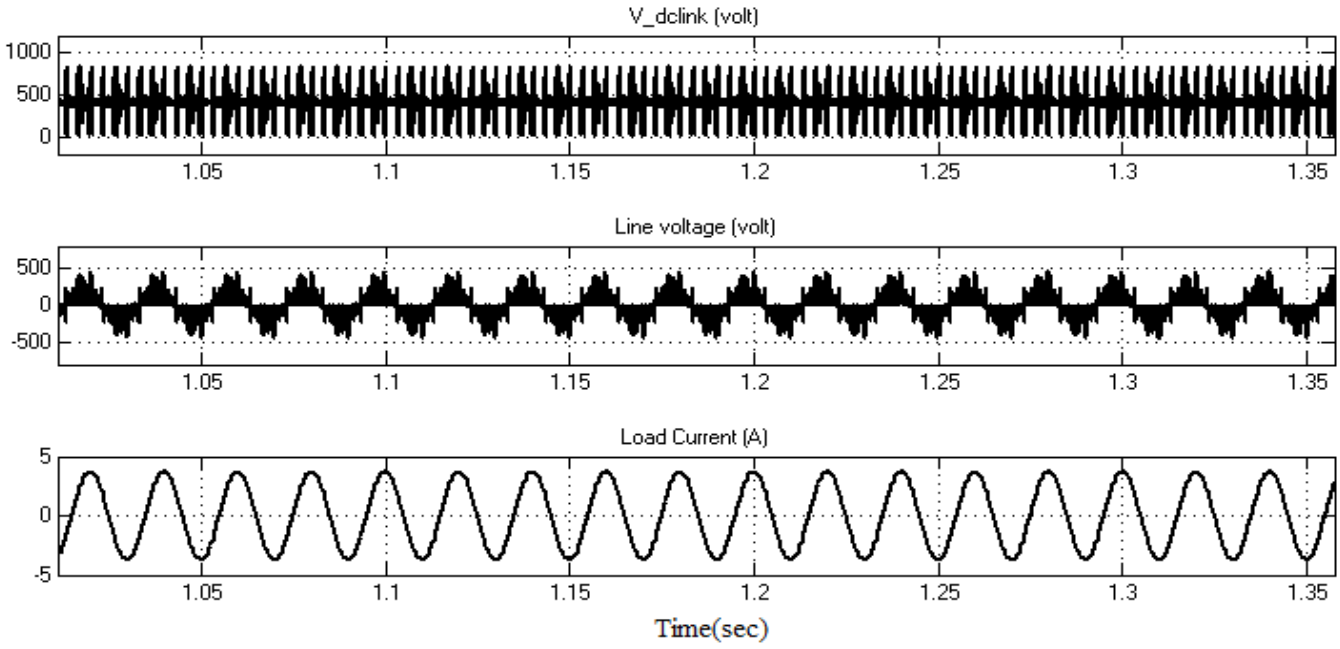

Figure 6.11 Inverter Output when irradiance is 1000 W/m^2

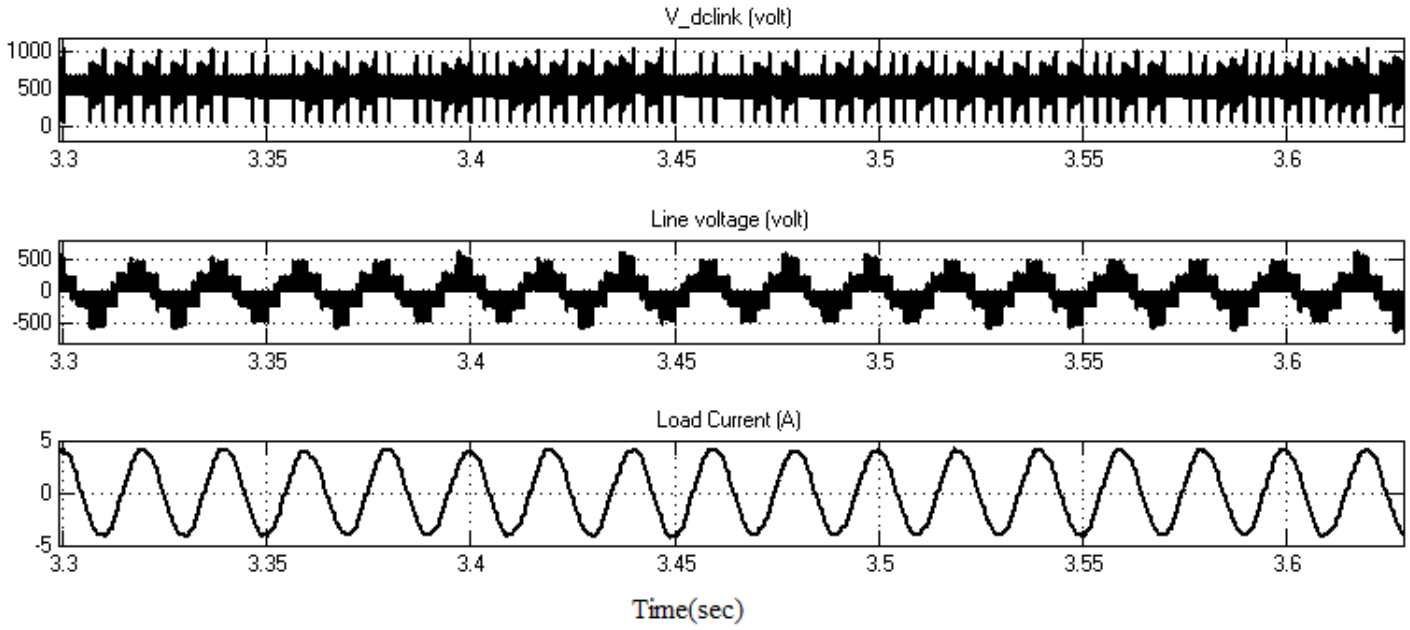

Figure 6.12 Inverter Output when irradiance is 500 W/m^2

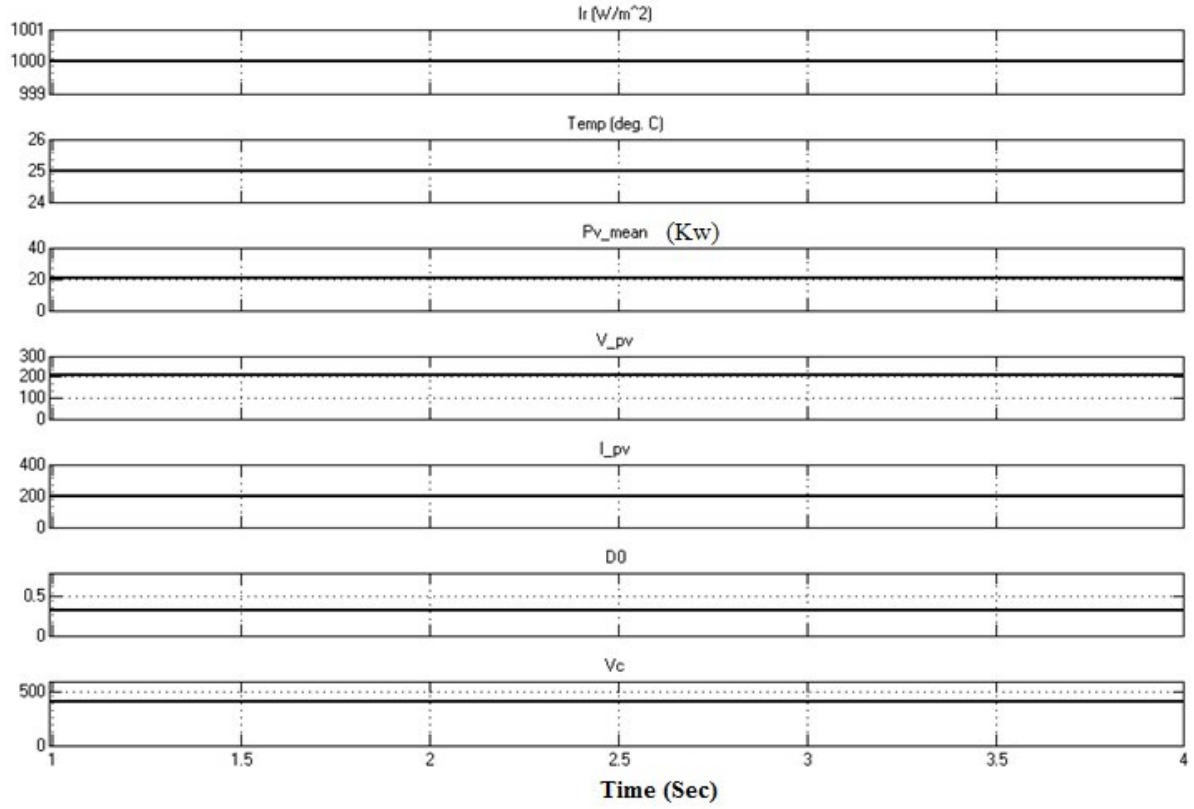

Figure 6.13 Simulation Result for Open Loop PV system With MPPT under constant environmental conditions

Figure 6.8 gives simulation result of inveter output line voltage and load current for an irradiance of 1000W/m^2 without MPPT technique. If irradiance falls to 500W/m^2 then Z-network capacitor ialso reduces so do output line voltage of inverter, shown in simulation result Figure 6.9. If MPPT technique is incorporated output voltage is almost same even if irradiance is changes as capacitor voltage is getting boosted. Vaiation of load current in two cases i.e with 1000W/m^2 and 500W/m^2 are shown in figure 6.11 and 6.12 respectively. Absence of MPPT output power is below 10KW while in presence of MPPT technique PV panel is able to deliver power around 15kW, thus enabling extraction of maximum power from PV panel. If irradiance is 1000W/m^2 then even if MPPT technique is not applied and load connected is lesser than maximum power rating of PV panel then in such situation panel is able to deliver the maximum power. If all environmental contions remains constant i.e irradiance 1000 W/m^2 then MPPT algoritms remains silent and panel delivers maximum possible power as load connected is lesser than output power of PV panel.

6.2.2 Simulation of Closed Loop Three Level ZSI for Standalone PV system

In closed loop configuration a inerter control strategy is incorporated along with MPPT algorithm to meet the adjust the output as per the load demand. Block diagram of closed loop system is shown in Figure 6.14. Capacitor voltage control is also implemented to achieve the Z-network capacitor voltage voltage beyond maximum power point voltage.

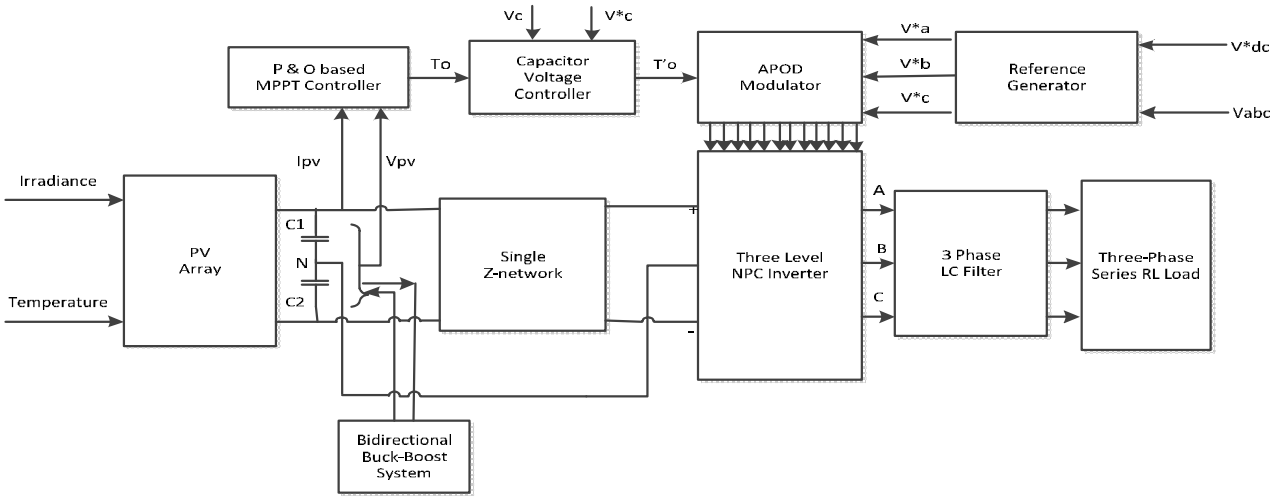

Figure 6.14 Block diagram of closed loop PV generation system

Figure 6.14 shows the closed loop configuration of NPC Three level ZSI based PV generation system. Reference generator block is basically used to generate reference signlas depending on the

input DC link voltage of ZSI and load requirements. LC filter is used to reduce the harmonics content and gives sinusoidal voltage and current waveforms. Transformer is used to match the voltage level of inverter and load. For simulation of standalone PV generation system transformer and LC filter is not used.

Three level ZSI parameters used for simulations:

Z Network capacitor (C1= C2) = 10mf

Z Network Inductor (L1 = L2) = 0.1mH

Switching Frequency =5kHZ

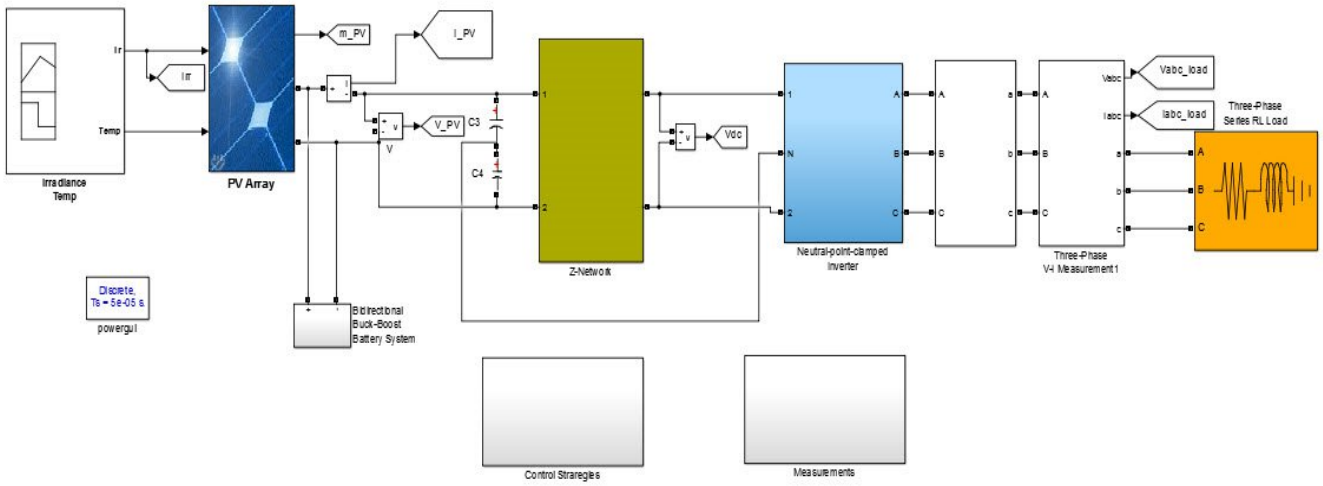

Figure 6.15 Simulink Model of NPC three level ZSI for closed loop PV generation system.

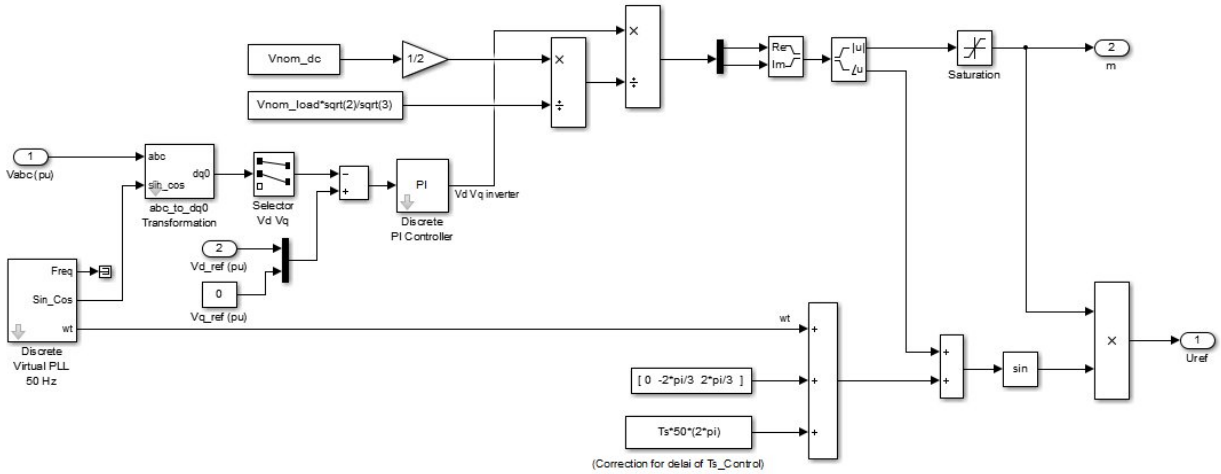

Figure 6.16 VSC control block for reference generation

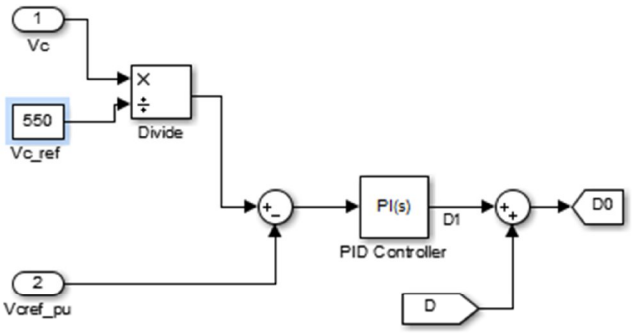

Figure 6.17 Capacitor Voltage Control

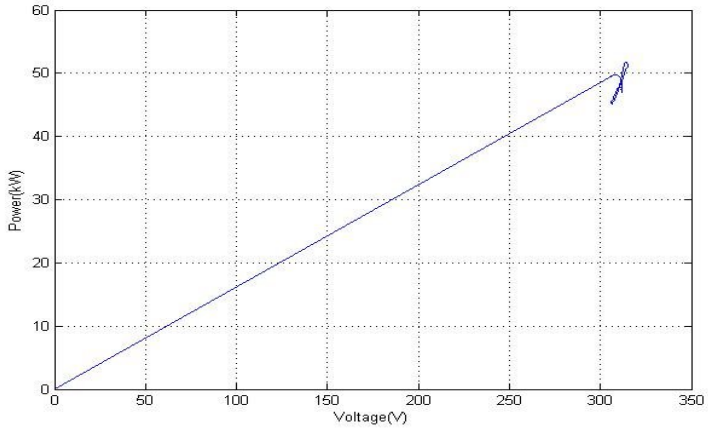

Figure 6.18 Simulated P-V characteristics of PV module in ideal conditions as per data sheets (table 6.2)

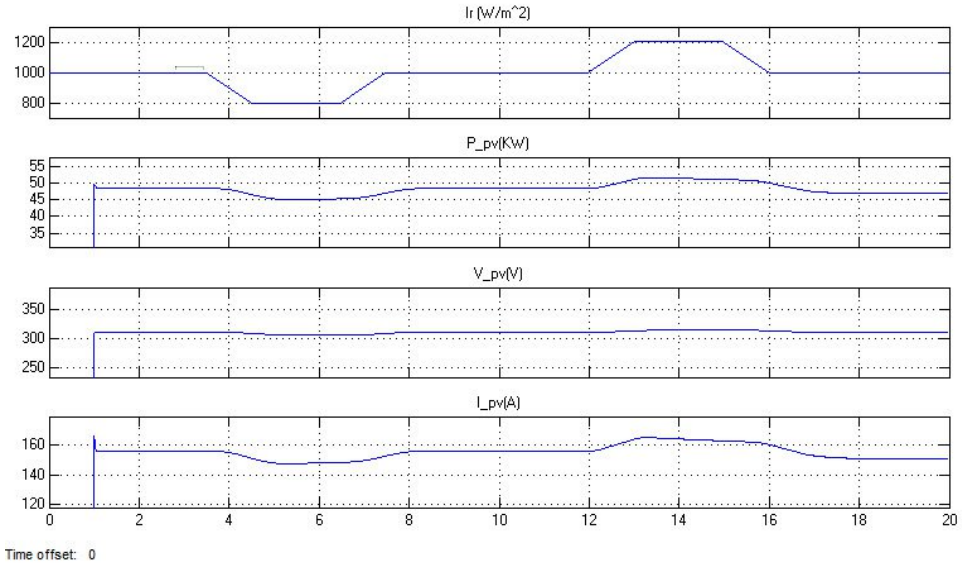

Figure 6.19 Variation of input side parameters under varying irradiance [Irradiance (scale: 200 W/m2/div.), P_pv (scale: 5 kW/div.), V_pv (scale: 50 V/div.), I_ pv (scale: 20 A/div.) (From top to bottom) and Time (scale: 2sec/div.)]

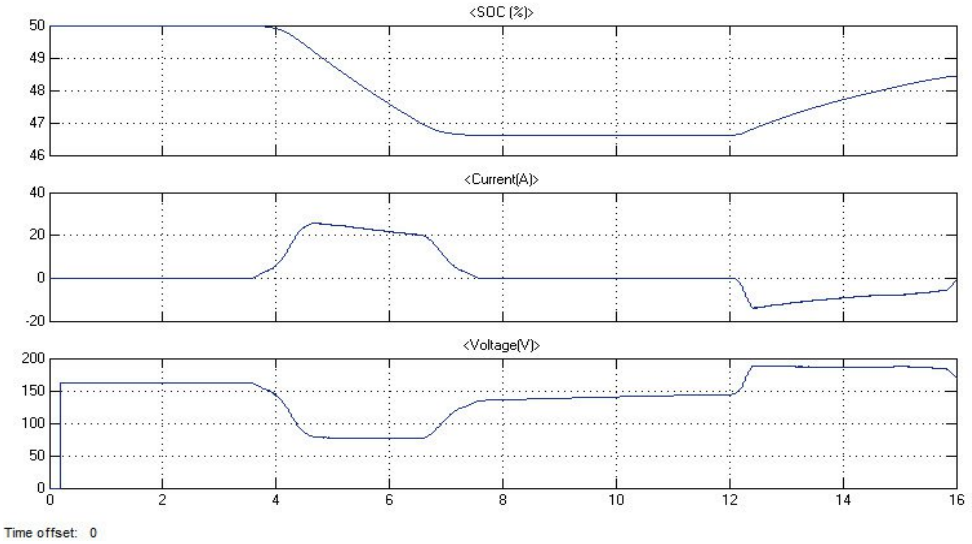

Figure 6.20 Battery parameters variation [State of charge of battery (SOC) (scale: 1%/div.), Current (scale: 20A/div.), Voltage (scale: 50V/div.) (From top to bottom) and Time (scale: 2sec/div.)]

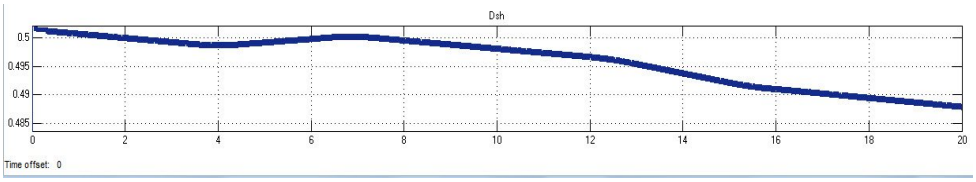

Figure 6.21 Variation in shoot-through duty ratio [Dsh (scale: 0.005/div.) and Time (scale: 2sec/div.)]

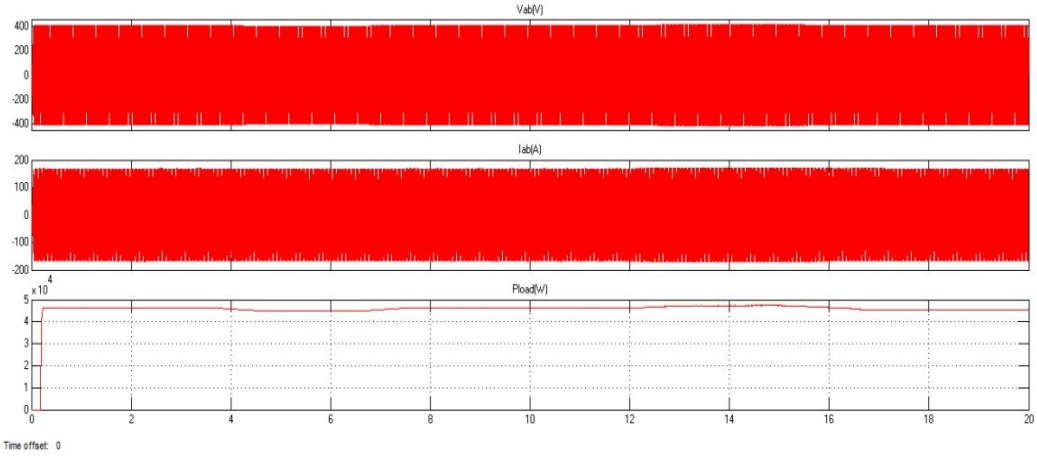

Figure 6.22 Variation in output side parameters (for the complete simulation time) [Voltage (scale: 200V/div.), Current (scale: 100A/div.) Power (scale: 10000W/div.) (From top to bottom) and Time (scale: 2sec/div.)]

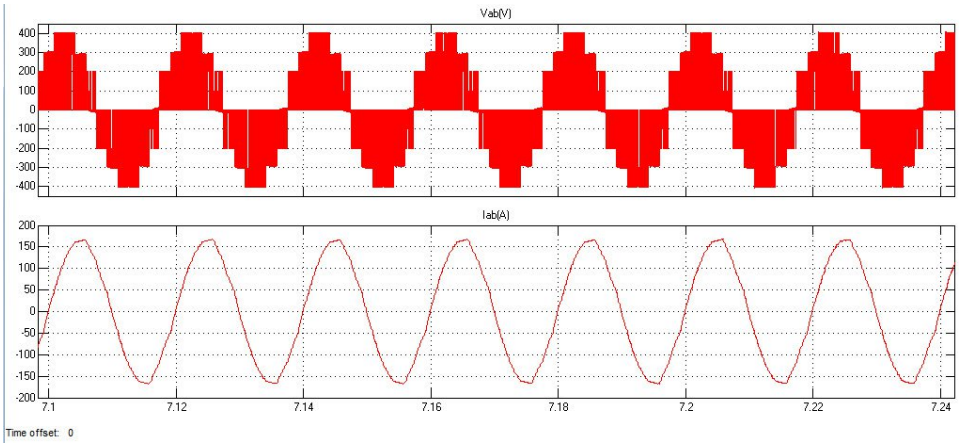

Figure 6.23 Variation in output side parameters (for a small duration) [Voltage (scale: 200V/div.), Current (scale: 100A/div.) (From top to bottom) and Time (scale: 0.02sec/div.)]

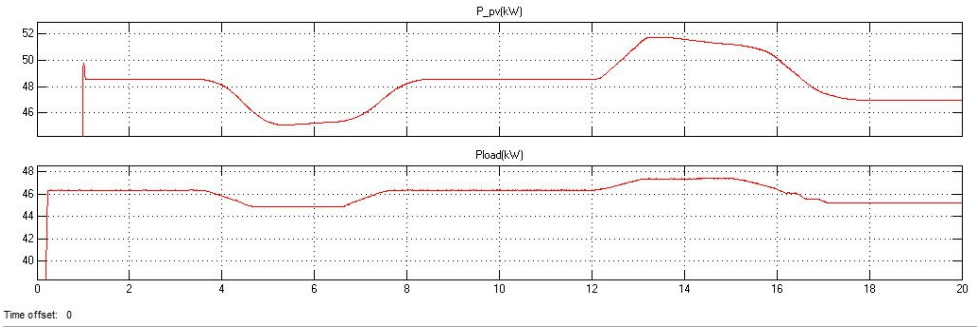

Figure 6.24 Variation in input and output power [Power (scale: 2kW/div.) and Time (scale: 2sec/div.)]

APOD based three-level NPC ZSI using single impedance network is studied for photovoltaic application and bidirectional buck-boost for RL load. Our system starts after 1 second. Table 6.2 shows the parameters of PV array. The DC output voltage of PV panel (which is 311.26V as in Figure 6.19) is boosted to desired voltage level and converted into AC (whose peak voltage is 405V as in Figure 6.22 and Figure 6.24) so as to feed the generated power to the load. Figure 6.18 shows the PV characteristics of the solar panel having maximum power (mentioned in datasheet) of 49.5kW and the steady state power at 1000 W/m^2 is 48.53kW (as in Figure 6.19) which gives the MPPT efficiency of 98%. In Figure 6.19, when irradiance decreases from 1000 W/m^2 to 800 W/m^2 during 3.5 to 7.5 seconds, the power generated by PV panel also decreases from 48.53kW up to 45.25kW. Similarly, when irradiance increases from 1000 W/m^2 to 1200 W/m^2 during 12 to 16 seconds, power also increases from 48.53kW up to 51.45kW. Voltage and current also decreases and increases proportionally as per the power variation. From Figure 6.20, it can be seen that when load demand is more (during under-generation, when $P_{\_PV}<P_L$, from 3.5 to 7.5 seconds), both battery and PV panel supply power to the load and the battery gets discharge from 50% SOC to 46.62% SOC, resulting

decrease in battery voltage and a positive battery current as it is flowing from battery to the system. Similarly, when extra power generated, (during over-generation, when $P_{\_PV}>P_L$, from 12 to 16 seconds) it is used to charge the battery from 46.62% SOC to 48.4% SOC, resulting increase in battery voltage and a negative battery current as current flow into the battery. This combination of supply tries to keep the power and voltage variation minimum under varying irradiance. Thus by using battery it is possible to keep the output power almost constant having less variation compared to input power as can been seen from Figure 6.24. The sag and swell of output voltage are 2% of rated value thus variation of power is just about 5%. The steady state output power is 46.34kW which gives the overall efficiency of 95.5%.The main reason of losses are due to switching losses and Z-network internal resistance whose values are mentioned in Table 3. The effect of variation of irradiance under constant temperature (250C) is studied by carrying out the simulation work in the MATLAB/Simulink environment. Block diagram of NPC three-level ZSI using single impedance network with a switching frequency of 5 kHz is presented in Figure 5.2.

ZSI provides the desired boosted DC link voltage to meet the required AC output voltage. From design consideration value of Z-network is chosen as L1=L2=0.02mH and C1=C2=1mF. It is ensured that even if irradiance changes as shown in Figure 6.19, output peak voltage is maintained constant (Figure 6.22 and Figure 6.23). Since charging & discharging of battery require 5-10 cycle to make effective change in power level input to ZSI. In Figure 6.21, with close loop modulation strategy, during over-generation period from 2 to 3.5 seconds, the shoot-through duty ratio is decreasing. While during under-generation period from 4.5 to 6 seconds it decreases. Consequently, the variation in output voltage can be kept less than 2% with respect to the steady state voltage which is 405V and is acceptable under IEEE519 voltage quality limit. FFT analysis of steady state current shows a THD content of 2.33% which is also acceptable. Similarly, more practical variation of irradiance can be seen in Figure 6.25 and further results are presented in Figure 6.26 to Figure 6.28.

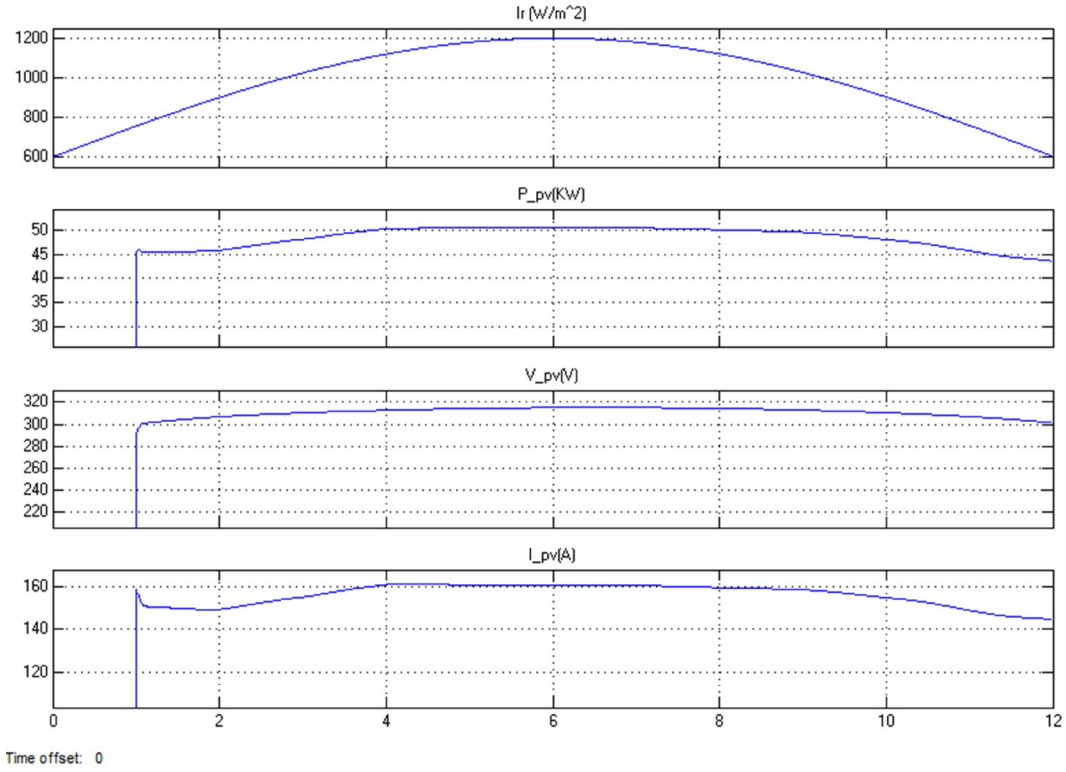

Figure 6.25 Variation of input side parameters under varying irradiance [Irradiance (scale: 200 W/m2/div.), P_pv (scale: 5 kW/div.), V_pv (scale: 20 V/div.), I_ pv (scale: 20 A/div.) (From top to bottom) and Time (scale: 2sec/div.)]

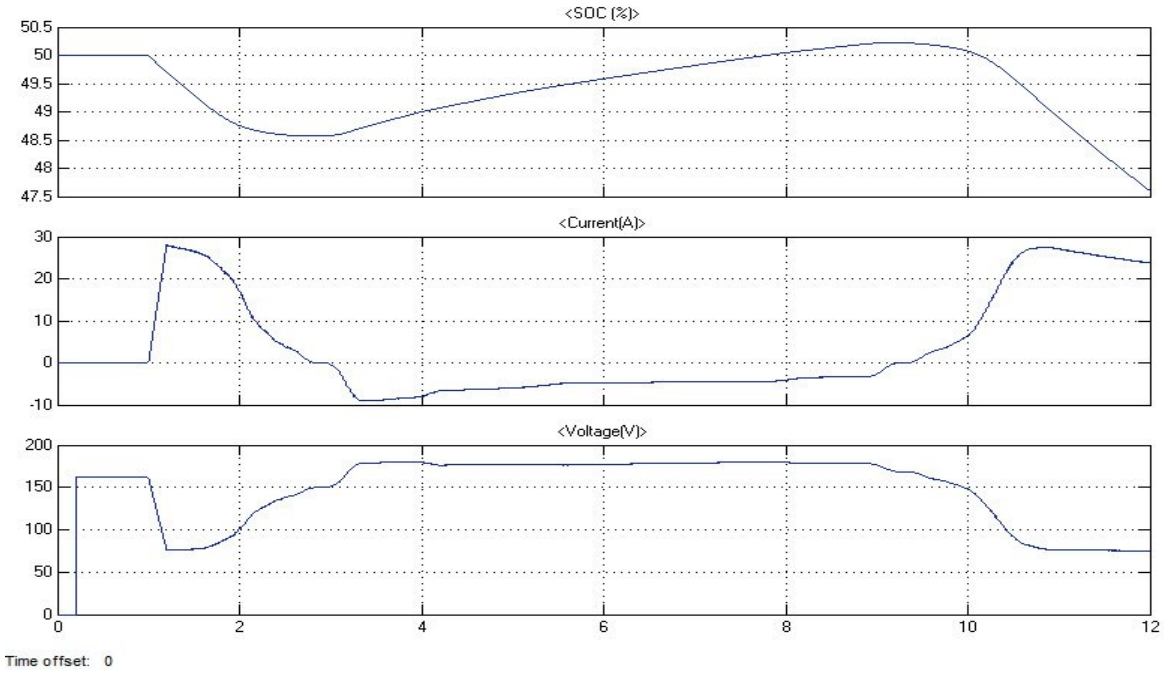

Figure 6.26 Battery parameters variation [State of charge of battery (SOC) (scale: 0.5%/div.), Current (scale: 10A/div.), Voltage (scale: 50V/div.) (From top to bottom) and Time (scale: 2sec/div.)]

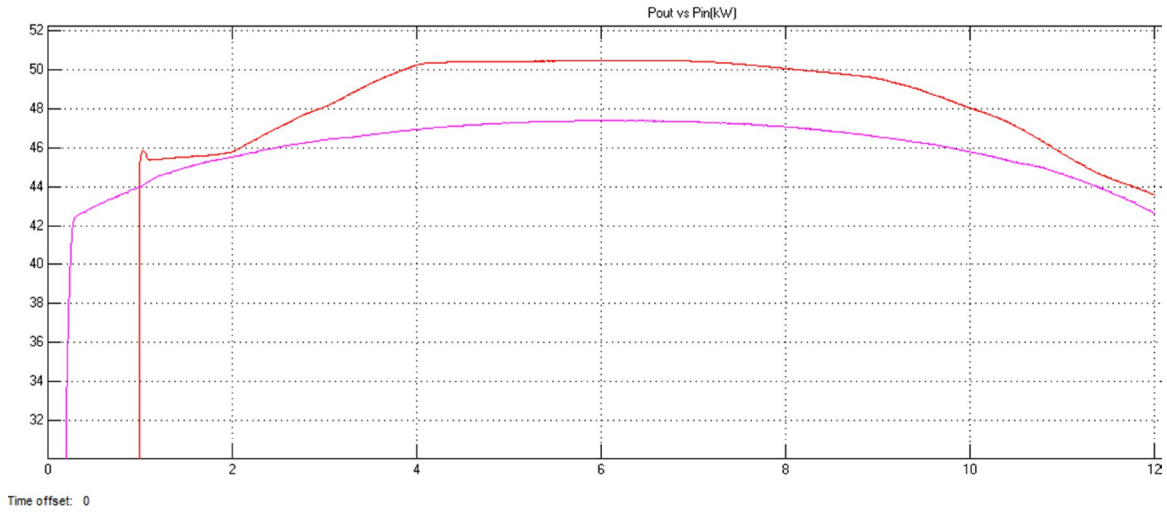

Figure 6.27 Variation in input and output power [Power (scale: 2kW/div.) and Time (scale: 2sec/div.)]

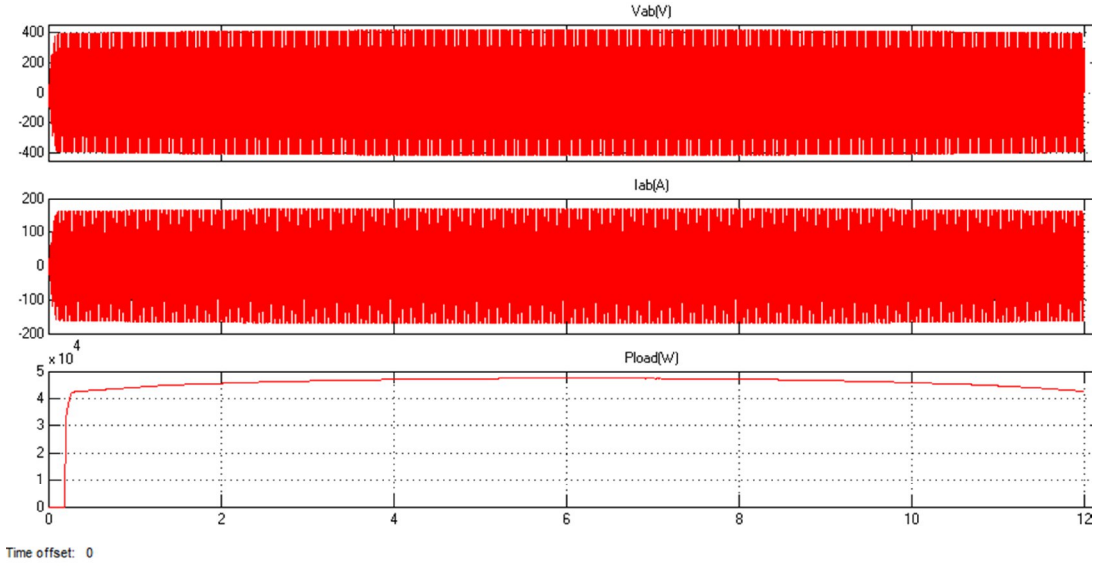

Figure 6.28 Variation in output side parameters (for the complete simulation time) [Voltage (scale: 200V/div.), Current (scale: 100A/div.) Power (scale: 10000W/div.) (From top to bottom) and Time (scale: 2sec/div.)]

7.1 Introduction

This chapter discusses the various aspects of scaled down hardware prototype developed in the laboratory.

7.2 Experimental setup

A NPC three level ZSI was developed to carry out the experiment process.

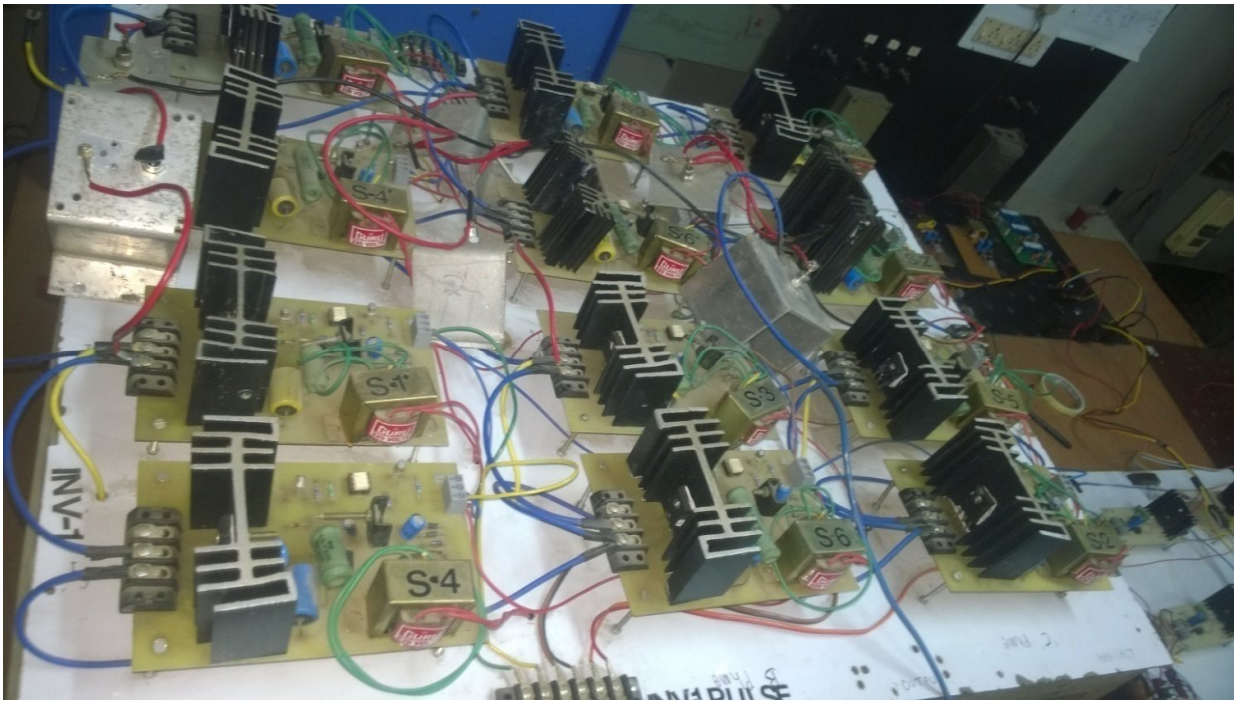

Figure 7.1 Experimental setup of a NPC three level ZSI

7.2.1 Development of Inverter Switch Setup - Gate Isolation, Amplification and Protection

The following circuit was used for all 12 switches. An IRFP460 MOSFET (Metal Oxide Semiconductor Field Effect Transistor) has been used as switch due to its cheaper cost and has inbuilt anti-parallel diode. The current rating of the MOSFET is 20A, the usage of the system has been limited to 5A and it has been ensured by using 5-A fuse in DC link as well as in AC link.

Figure 7.2 Switching unit of the inverter

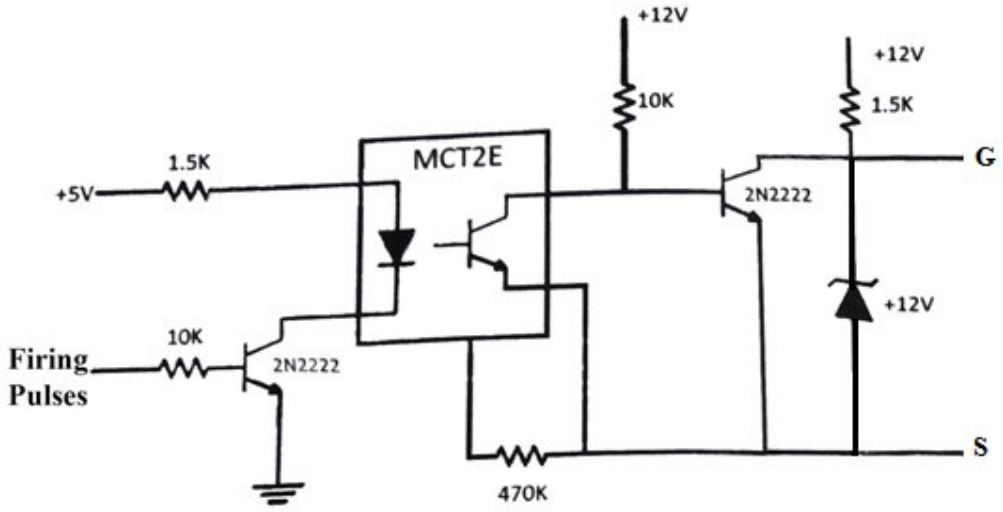

Figure 7.3 Gate Driver circuit for each switching unit

7.2.1.1 Pulse Amplification and isolation Circuit:

The pulse amplification circuit for MOSFT is shown Figure 7.3. The opto-coupler MCT-2E provides necessary isolation between the low voltage isolation circuit and high voltage power circuit. The pulse amplification is provided by the output amplifier transistor 2N222. When the input gating signal is +5V level, the input transistor saturates, the LED of opto-coupler conducts and the light emitted by it falls on the base of the phototransistor, thus forming the base drive. The output transistor thus receives no base drive and remains in the cut-off state and a +12V pulse (amplified) appears at its collector terminal. The +12V needed by firing circuit is locally generated ate each switch using a 220/18V transformer and 7812 regulated IC along with a rectification circuit and capacitors. When the input gating signal reaches ground level, the input switching transistor goes to cut off state and opto-coupler LED remains off, thus emits no light and therefore the photo transistor remains off. The output transistor receives base drive and saturates, hence the output falls to zero level. Therefore , the

circuit provides proper amplification and isolation. Further, since slightest spike above 20V can damage the MOSFET, a 12V Zener diode is connected across the output isolation circuit. This clamps the triggering voltage to 12V.

7.2.1.2 Snubber Circuit:

Switching high current in a very short interval of time gives rise to voltage transients that could exceeds the rating of the MOSFET. The rated Gate-to-Source voltage of MOSFET is 20V. Snubbers are therefore needed to protect the switch from transients. Snubber circuit for MOSFET is shown in Figure 7.4. The diode prevents the discharging of the capacitor via the switching device, which could damage the device because of large discharge current. An additional protective Metal Oxide Varistor (MOV) is used across each device to protect against over voltage across the device.

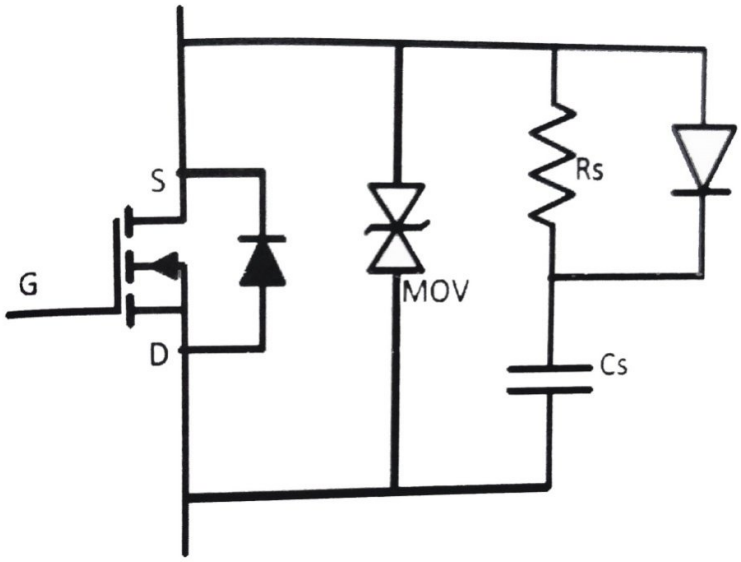

Figure 7.4 Snubber circuit

7.2.2 Development of Measuring Circuit

For accurate, effective and reliable operation of a system in closed loop configuration measurements of various systems parameters and their conditioning is needed, which must meet the following requirements.

- High accuracy
- Galvanic isolation between high voltage and low voltage side
- Ease of installation
- Linearity and fast response

With the availability of Hall Effect current and Voltage sensors, these requirements are fulfilled to a great extent. These sensors are now available in a variety of range and ratings to meet the system requirements.

7.2.2.1 Current Sensing Circuit:

AC currents are sensed using PCB mounted Hall Effect sensors (HTP 50). These current sensors provide galvanic isolation between high voltage power circuit and the low voltage control circuit and require a nominal supply voltage of ±12V to ±15V. It has the transformation ration of 1000:1, hence its output is scaled down to obtain the desired value to meet the control requirements. Circuit diagram for PCB mounted Hall Effect sensor is shown in Figure 7.5 and the sensing unit im Figure 7.6.

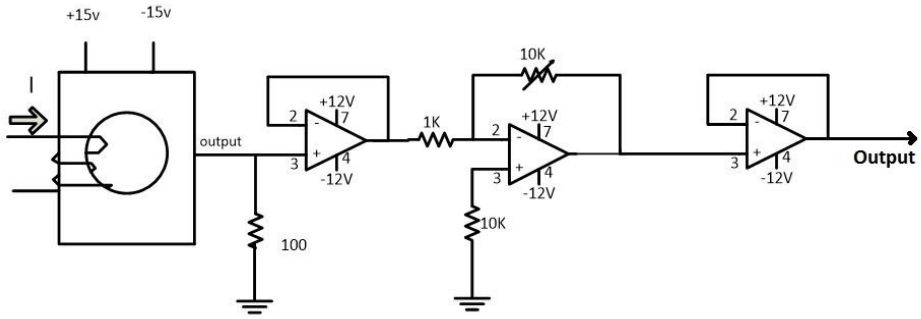

Figure 7.5 Current sensing circuit diagram

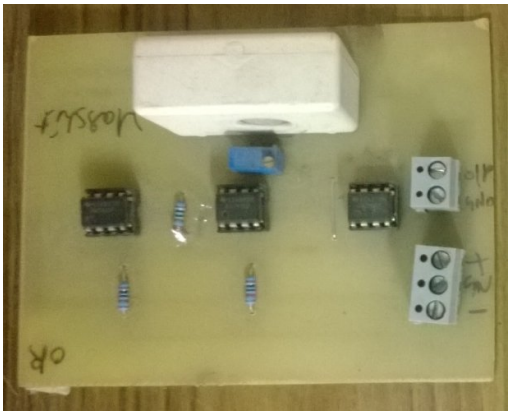

Figure 7.6 Current sensing unit

7.2.2.2 Voltage Sensing Circuit:

It is an important circuit needed for close loop operation of control scheme. Sensor output is processed using a unity gain buffer and an inverting amplifier. Input Resistors are used to scale down the voltage within the range of AD202 (isolation amplifier). Op-amp circuits are used at the output of AD202 for adjusting the scale. Circuit diagram of Voltage sensing circuit is shown in Figure 7.7.

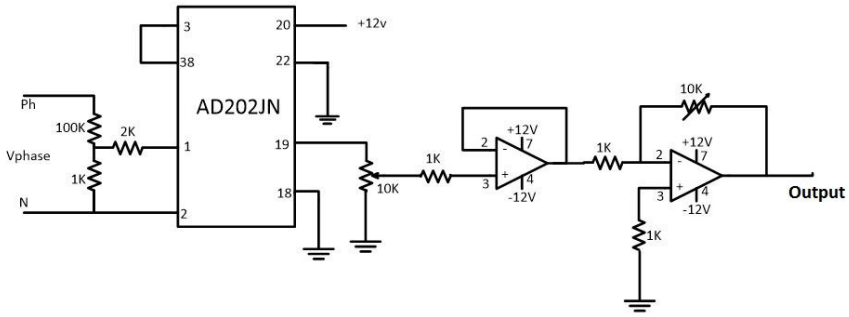

Figure 7.7 Voltage sensing circuit

7.2.3 Regulated DC Power Supply

Dc Regulated supplies (+12V, gnd, -12V and +5V) are required for providing biasing to various circuits like pulse amplification and isolation circuits, voltage sensing circuits, current sensing circuits etc. using ICs 7812 for +12V, IC 7912 for -12V, and 7805 for +5V. The circuit diagram of the regulated DC power supplies are shown in following figures:

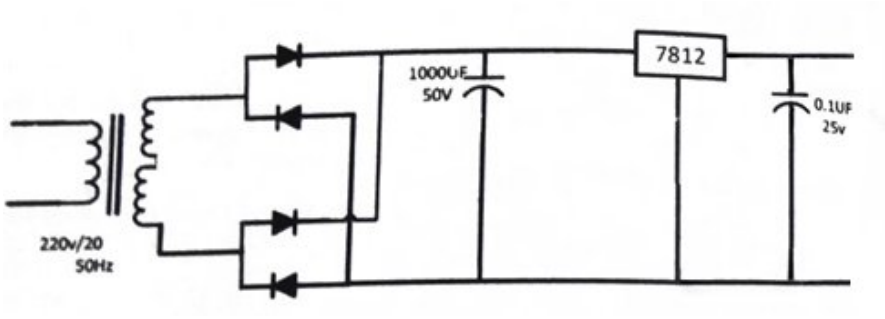

Figure 7.8 Regulated DC Power Supply (+12V)

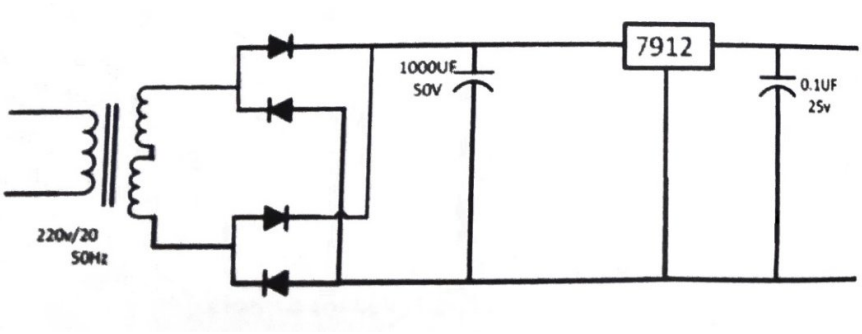

Figure 7.9 Regulated DC Power Supply (-12V)

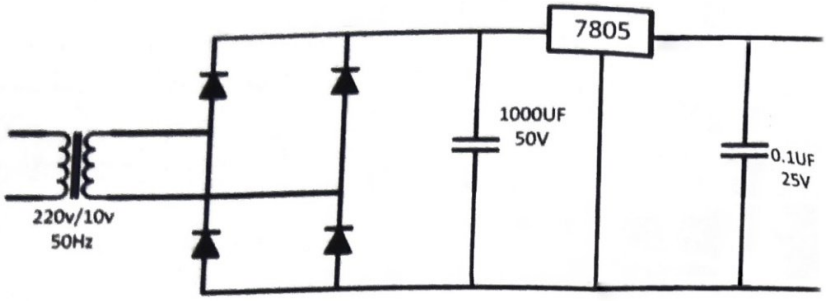

Figure 7.10 Regulated DC Power Supply (+5V)

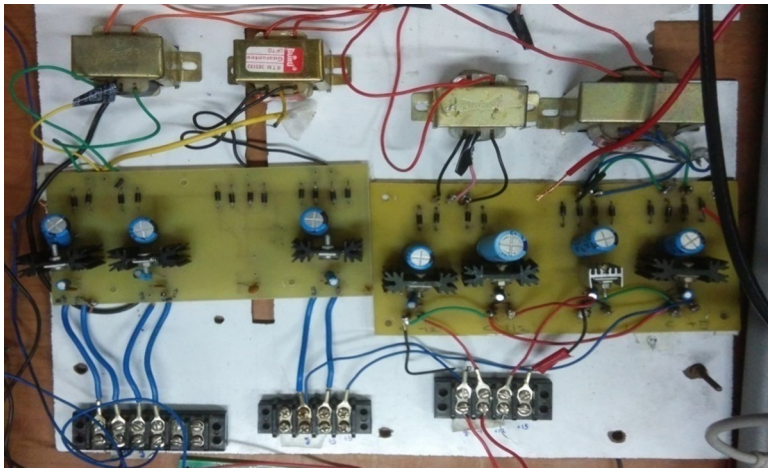

Figure 7.11 Regulated Power Supply Designed in the Lab

CHAPTER 8: CONCLUSION AND RECOMMENDATIONS

There are some limitations and drawbacks associated with traditional inverters like voltage can not be boosted more than the DC voltage source, EMI effect, dead time effect etc. A ZSI overcomes these limitations of traditional inverters. A ZSI provides a single stage voltage buck- boost operation So ZSI is a better inverter topology for many applications, mainly renewable energy power conversion which requires voltage boost operation for proper power conditioning to meet the load demand. Multilevel inverters provide a better performance as compared to two level inverters. Multilevel inverter gives low harmonics contents, has low voltage stress on switching devices, and can operate on low frequency, so for high power application multilevel inverters are preferable over two level inverters. Three level ZSIs provide a single stage voltage buck-boost operation based energy conversion while retaining all favorable advantages of traditional inverters. Performance of NPC three level ZSI for PV system using modified APOD is studied by carrying out simulation in MATLAB environment. Operation of NPC three level Z- source is studied for standalone and grid connected for photovoltaic and verified by MATLAB simulation results. A unified voltage control technique to simultaneously achieve MPPT and to maintain desired Z-network capacitor is also implemented in MATLAB. Three level ZSI equipped with unified voltage control technique is able to maintain the desired output voltage even if irradiance level changes which is important for proper power conditioning. To verify the simulation results a scale down hardware prototype of NPC three level ZSI is developed in the laboratory. Experimental results are obtained for different load conditions and with different shoot through ratio in open loop condition. Experimental results verify that NPC three level ZSI gives satisfactory performance.

8.1 Thesis contributions

The work carried out in this thesis has following contributions:

1. Advantages of Z-Source inverter over conventional inverters, and significance of impedance network are studied.
2. Study of MPPT algorithms to extract maximum power from PV panel.
3. Unified voltage control technique to simultaneously achieve the MPPT and maintains Z network capacitor voltage is implemented in MATLAB.
4. Operation of NPC Three level Z-Source inverter using modified APOD using for standalone and grid connected PV system is studied in MATLAB environment.

5. Scale down hardware prototype of NPC three-level ZSI is developed in the laboratory.

8.2 Future Scope

1. Hardware implementation of NPC three level Z- Source inverter for grid connected PV system.
2. Extending the studied concepts for higher level(5,7 etc.) of multilevel Z-source inverter.
3. Performance study using different Controller (Fuzzy and sliding Mode) for unified Z-network capacitor voltage control.
4. Stability analysis for NPC three level ZSI.

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