Investigation on current controllers for multilevel inverter based shunt active power filter

A DISSERTATION

Submitted in partial fulfilment of the
requirements for the award of the degree of

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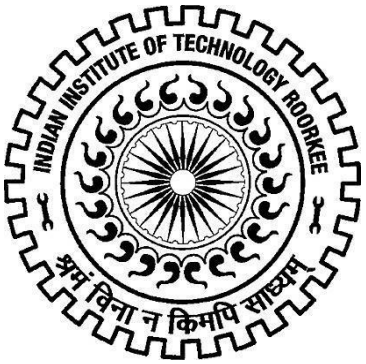
in
ELECTRICAL ENGINEERING
(With Specialization in Power Electronics)

By

ANIL



DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE -247667 (INDIA)
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CANDIDATE'S DECLARATION

I hereby declare that the work, which is being presented in this report entitled "**Investigation on current controllers for multilevel inverter based shunt active power filter**" in partial fulfilment of requirement for the award of degree of Integrated Dual Degree in Electrical Engineering with socialization in Electric Drives & Power Electronics, and submitted in the Department of electrical Engineering of Indian Institute of Technology Roorkee, India, is an authentic record of my own work carried out during the period from may 2015 to May 2016, under the supervision of Dr. Anubrata Dey, Assistant Professor, Department of Electrical Engineering, of Indian Institute of Technology Roorkee, India.

The matter embodied in this report has not been submitted by me for the award of any other degree of this or any other Institute/ University.

Date: 23nd May, 2016 ANIL

Place: Roorkee

CERTIFICATE

This is to certify that the statement made by the candidate is correct to the best of knowledge and belief.

Dr. ANUBRATA DEY

Assistant Professor

Department Of Electrical Engineering

Indian Institute of Technology, Roorkee

ROORKEE – 247667

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(Anil)
IDD (EPE)
11212002

Abstract

Power electronics technology offers economical and reliable solutions to manage and control use of electrical energy. Which has led to significant use of power electronic systems in industrial and domestic applications. However, power electronics system exhibits nonlinear characteristics, generating current and voltage harmonics in ac power lines and are becoming troublesome problem in ac power lines. Classically, Passive filters have been most commonly used to limit the flow of harmonic currents in distribution systems. But active power filters have emerged as viable alternative to passive filters. Voltage Source Inverters (VSI) with a current control scheme is used for successful operation of the active power filter. Multi-level structure for VSIs is preferred particularly for medium voltage and high power applications. Various current control scheme exists in the literature for control of Active power filter. In this study current controllers for multilevel inverter based Shunt active power filter are investigated. Hysteresis current control, space vector based hysteresis current control and predictive controller are simulated and results and discussion are presented.

CONTENTS

LIST OF FIGURES

LIST OF ACRONYM

3P3W	Three-phase, Three-wire
3P4W	Three-Phase, Four-wire
ac, AC	Alternating Current
CSI	Current source inverter
dc, DC	Direct Current
DBR	Diode Bridge Rectifier
DSP	Digital Signal Processor
D-STATCOM	Distribution Static Synchronous
FACTS	FLEXIBLE ac Transmission System
FFT	Fast Fourier Transform
IEEE	Institute of Electrical and Electronics Engineers
IRP	Instantaneous Reactive Power theory
HCC	Hysteresis current control
MOSFET	Metal Oxide Semiconductor Field-effect transistor
NPC	Neutral Point Clamped
PCC	Point of Common Coupling
Pf, PF	Power Factor
PI	Proportional and Integral
PWM	Pulse Width Modulation
RMS	Root Mean Square
SAPF	Shunt active power filter
SVHCC	Space vector based hysteresis current control
THD	Total Harmonic Distortion
UPQC	Unified Power Quality Conditioners
VSI	Voltage source inverter

List of Table

LIST OF SYMBOLS

ea, eb, ec	PCC voltage in phase A, B and C respectively.
p	real power
q	reactive power
$\tilde{p}$	oscillating component of real power
Vref	Reference DC-link capacitor voltage
Vdc	Voltage across DC capacitor
ica, icb, icc	filter current in phase a, b, c
mf	frequency modulation ratio
wn	frequency of nth harmonic
$\boldsymbol{V_{ka}}$	voltage at inverter terminal in phase A
$\boldsymbol{V_k}$	space phasor of inverter voltages
i_c^*	reference filter current
V_s^*	reference voltage space phasor
Δi	current error
ΔV	Voltage error
g	Cost function for predictive controller
L	connecting inductor

CHAPTER 1

INTRODUCTION

1.1 General

In recent years power electronics converter are widely used in domestic and industrial application. These converters draw non-sinusoidal current resulting in current harmonics in supply current, which distorts supply voltage at point of common coupling. These harmonic decrease efficiency and life of power system equipment and deteriorates power quality at point of common coupling. Power quality is measured as the deviation in the supply voltage and current from the steady 50Hz sinusoidal waveform of voltage and current. The deterioration of power quality means that voltages and currents are not of the standard value and shape.

1.2 Harmonics sources and effects

Harmonics are sinusoidal currents and voltages which are integral multiple of fundamental frequency of sinusoidal current and voltage. Any periodic waveform can be constructed by a sinusoidal waveform of fundamental frequency and sinusoids at integral multiple of fundamental frequency. When the distorted current passes through the series impedance of the power delivery system, it causes a voltage drop which is also distorted. This results in voltage harmonics appearing at point of common coupling. Harmonics are produced in the power system from the devices which have non-linear characteristics and are connected to the sinusoidal power source of the power system.

With the development of the power electronics switches there has been considerable increase in the harmonics injection in the power system. The primary source of the harmonics in current and voltage distortion are the power electronic converters which are used mainly for both domestic and industrial applications. The power converters cannot store energy, so when a dc side of it produce harmonics it is reflected in the ac side and hence harmonics is injected in the power system.

The other common sources of harmonics are [1,2,7]:-

1. Due to semiconductor switches in devices like rectifiers, inverters, converters, cyclo-converters.
2. Battery charger, electronic equipment etc.

3. Devices like arc furnace, switch mode power supplies (SMPS), fluorescent lamp, Adjustable Speed Drive (ASD) etc.

Harmonic problems [1,2,7]:-

1. Adverse effect on life of equipment and maloperation of equipments.
2. Automatic manufacturing Plant can shut down for small dips in supply voltage.
3. Overvoltage and overheating causes failure of the insulations.
4. Transformers becomes saturated and overheated
5. Protective equipment like Circuit Breaker., relay etc may not work properly.
6. Electromagnetic interference may cause problems in communication lines
7. May lead to resonance with the capacitor connected in the system.
8. Overheating and excess losses in electrical motors, capacitors.

1.3 Power filters

To reduce the harmonics in the power system various techniques have been used, one being the use of power filters. A shunt power filter provides a low impedance path to harmonic current, so that harmonic current flows through the shunt filter. Series filter blocks the harmonic current by providing high series impedance in path of current. When these filters are implemented by using passive elements L and C, they are called passive filters. In tuned series passive filter, L and C branch are tuned to provide high impedance at the desired harmonic frequency. In shunt passive filter, filter is tuned to provide low impedance at harmonic frequency. The harmonic current of this frequency shunts through this filter and supply current is free from that harmonic current. For filtering multiple harmonics, multiple filters are required. Passive filters are less costly and easy to implement but have certain limitations. Passive filters are difficult to design at changing load conditions, the frequency and power rating once designed are fixed for entire lifetime. Design of passive filters may become difficult for stiff system. Passive filters also have the problem of resonance. So because of these limitations, active power filters are more suitable for cleaning out voltage and current harmonics. [3,7]

1.4 Active power filters

Active power filter as emerged as better alternative than traditional method such as passive filters. Improved semiconductor devices and powerful processors has helped in this cause. The active power filters can be configured in shunt or series or both (Unified power quality conditioner) and also in hybrid (active + passive). Series active filter is used as controlled voltage sourse for

compensation of supply voltage harmonics. It is connected in series between the load and the supply and injects voltage components to maintain a balanced sinusoidal supply and can also compensate voltage sags and swells on the load side. Shunt active power filter(SAPF) is widely used topology for filtering out current harmonics. Shunt active power filter supplies the harmonic and reactive power requirement of the load, so that source has to supply only real power at unity power factor. This makes the source current drawn sinusoidal i.e. free from harmonics.

When active filter and passive filter are used simultaneously then the filter is called hybrid active filter. The active filter of the hybrid filter is generally a series active filter which blocks harmonic voltages of the supply and injects voltage to make the supply voltage sinusoidal. The passive filter of the hybrid filter is connected in shunt provides a low impedance shunt path to current harmonics. The unified power quality conditioners (UPQC) are a combination of shunt active filter and series active filter. Series active filter part of the UPQC is used for voltage regulation and voltage harmonic compensation and the makes the supply voltage sinusoidal. The shunt active filter part of the UPQC is used for is used to compensate harmonic current and reactive power of the non-linear load and also used to maintain the regulated dc link voltage to the reference value. The UPQC has the best compensation among different filters but it is costly and required where we have problems of both current harmonics and voltage harmonics. But major part of the problem can be solved by filtering out current harmonics, which can be done by shunt active power filter. Thus in this dissertation shunt active power filter is taken for study.

1.5 Literature review

This section provides a review of published literature related to shunt active power filters and current control techniques for SAPF.

Review based on analysis of power filters

IEEE-519 std: IEEE recommended practices and requirements for harmonic control in power system (1992), recommended harmonic control practices to utilities and users. It also detailed the effects and causes of harmonics and recommended voltage and current distortion limits for utilities and users.

J. C. Das(2003) Discussed the potentialities of passive filters for harmonic power compensators. He discussed various aspects to be considered while designing a singly tuned passive filters. He

also outlined the limitations of passive filters such as fixed tuned frequency and power rating, effects of source impedance on design and resonance problems.

H. Akagi(1996) Akagi highlighted the potential use of active filters with improved semiconductor technology. He proposed instantaneous reactive power theory to better filter out harmonic and reactive power. He dealt with shunt, series and hybrid filter topologies without using energy storing elements.

Review based on analysis of reference current generation techniques

Reference current generation technique is an important part of control strategy of shunt active power filter. When supply voltages are unbalanced or the system has zero sequence currents selection of optimal reference current generation can improve efficiency and transient response.

Akagi(1983) gave generalised theory of instantaneous reactive power theory and its applications in three phase circuits. Power filters based on Instantaneous reactive power(IRP) theory can work under unbalanced voltage, or under zero sequence currents and is flexible in compensating the required component of power according to designer.

Brij N. Singh et. Al.(2007) proposed an improved control algorithm for Shunt Active Power filter by modifying instantaneous reactive power theory. They generated reference supply current instead of reference filter current which improved the performance during steep change in load current. The control also ensures the maintaining of DC bus capacitor voltage and voltage balancing, without voltage control loop.

M. aredes and F. Monteiro.(2002) posited the fryze current control strategy, which uses minimization methods to generate reference current for SAPF. This method gives minimum RMS supply current in three phase. This method cannot compensate active and reactive power components individually.

Review based on analysis of current control techniques of Voltage source inverter

David M. brod(1985) gave an overview of current controllers for Voltage source inverters. He discusses three techniques hysteresis control, ramp comparison control and predictive control for VSI. He highlighted the higher switching frequency problem of hysteresis control and poor dynamic performance of predictive controller.

Bose B.K.(1990) gave an adaptive hysteresis band current control for machine drive system. Adaptive hysteresis control has lower average switching frequency then normal hysteresis

current control. Suresh Y.(2012) implemented an fuzzy based adaptive hysteresis current control for Shunt active power filter.

Odavic, M(2011) posited one sample ahead predictive current control technique for Shunt active power filter. It calculates the required switching state of inverter, one sample time ahead to compensate for computational delay.

Vodyakho, O(2009) compared space vector based controls for shunt active power filter. Space vector based control give better performance as three phases are considered simultaneously to select switching state of Voltage source inverter.

A. dey et. Al.(2013) gave hysteresis current controller for general n-level inverter with constant switching frequency. It removes some of the drawbacks of hysteresis controller and give good overall performance in terms of switching frequency.

1.6 Conclusions from literature review

Shunt active power filters are increasingly used for filtering out harmonics and to limit current and voltage distortion for within IEEE-519 std. Control strategy for Shunt active power filter is important part in the overall performance of system. Many reference current generation technique have been proposed in the literature. If the supply voltage is distorted, or under zero sequence currents or transient conditions robustness of reference generation current is important for overall performance. In this study, 3-phase, 3-wire system, with balanced undistorted supply is taken to study the effect of current controllers on performance of SAPF. Under this condition IRP-theory(pq theory) based technique is sufficient for operation of SAPF. Current controllers for multilevel inverters have been widely studied. Some of the techniques are PWM techniques, hysteresis control, space vector based PWM, adaptive hysteresis current control, space vector based HCC(SVHCC), and predictive controllers. Hysteresis control, nearly constant frequency SVHCC, and predictive controller is taken for comparative analysis in this study.

1.7 Organization of thesis

Chapter 1 discusses about the harmonics, in the power system. Brief discussion on passive filter and active filter solution is given and a detail literature review relating to different control algorithm is also presented.

Chapter 2 includes discussion on shunt active power filter, multilevel invereter topologies, design of SAPF components and control strategy for SAPF.

Chapter 3 presents the operating principle and the simulation results of three different current controllers. A comparison between three current controllers were also made.

Chapter 4 focuses on the hardware implementation of a SAPF and its components. It discusses the driver circuit for a MOSFET switch, power supplies, voltage and current sensor and 3L-NPC inverter.

CHAPTER 2

2.1 Shunt active power filters

Power schematic for a three phase VSI based shunt active power filter is shown in Fig.1. Power circuit of a SAPF consists of a three phase voltage source inverter(VSI) connected to the power system through the connecting inductors. PWM controller controls the switching of VSI such that inverter produces the desired reference filter current. Reference current to be produced by the inverter is generated by reference current generation block such that source current becomes sinusoidal. Outer DC voltage loop maintains the capacitor voltage constant by generating p_{loss} signal which represent extra amount of power filter has to draw such that capacitor voltage remains constant. In this simulation three phase 3 level diode clamped inverter is used as a voltage source inverter and diode bridge rectified load is taken as the nonlinear load.

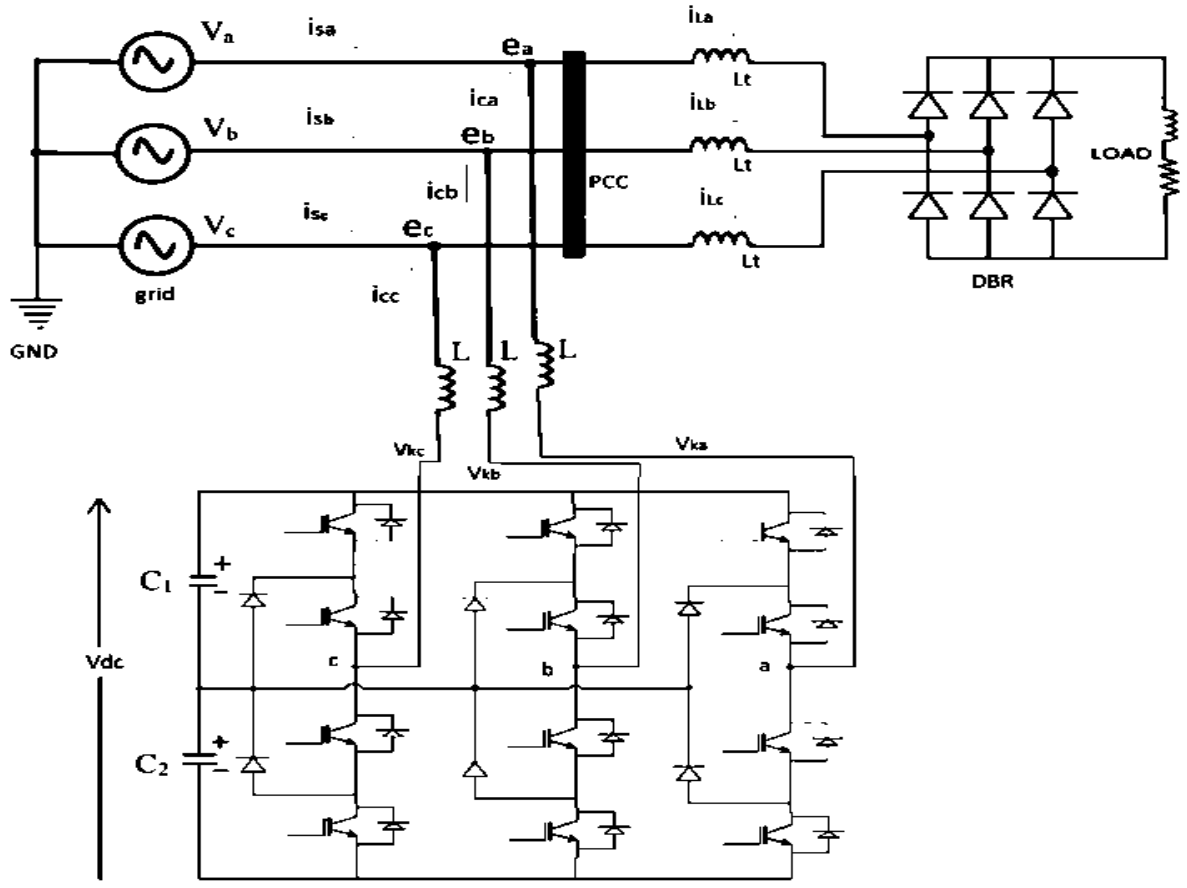
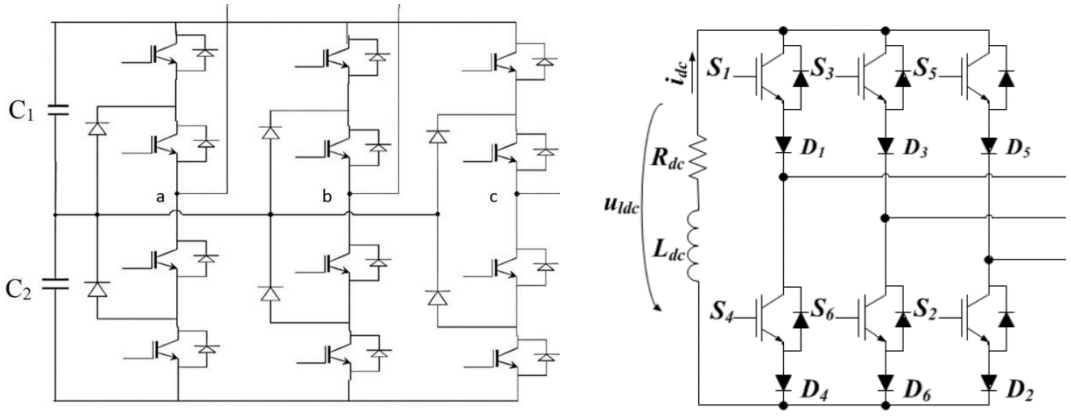


Fig.2.1 Power schematic of Shunt Active power filter

2.2 Voltage source Inverter

Voltage source inverter(VSI) or Current source inverter(CSI) can either be used as a controlled current source. Voltage source inverter uses capacitor in the DC link while current source inverter uses inductor at the DC side. Fig. 2.2 shows the topologies of VSI and CSI. Current source inverters are bulky DC link inductor, high DC-link inductor losses and slow dynamics. For these reasons voltage source inverter is used for its high efficiency and low initial cost.

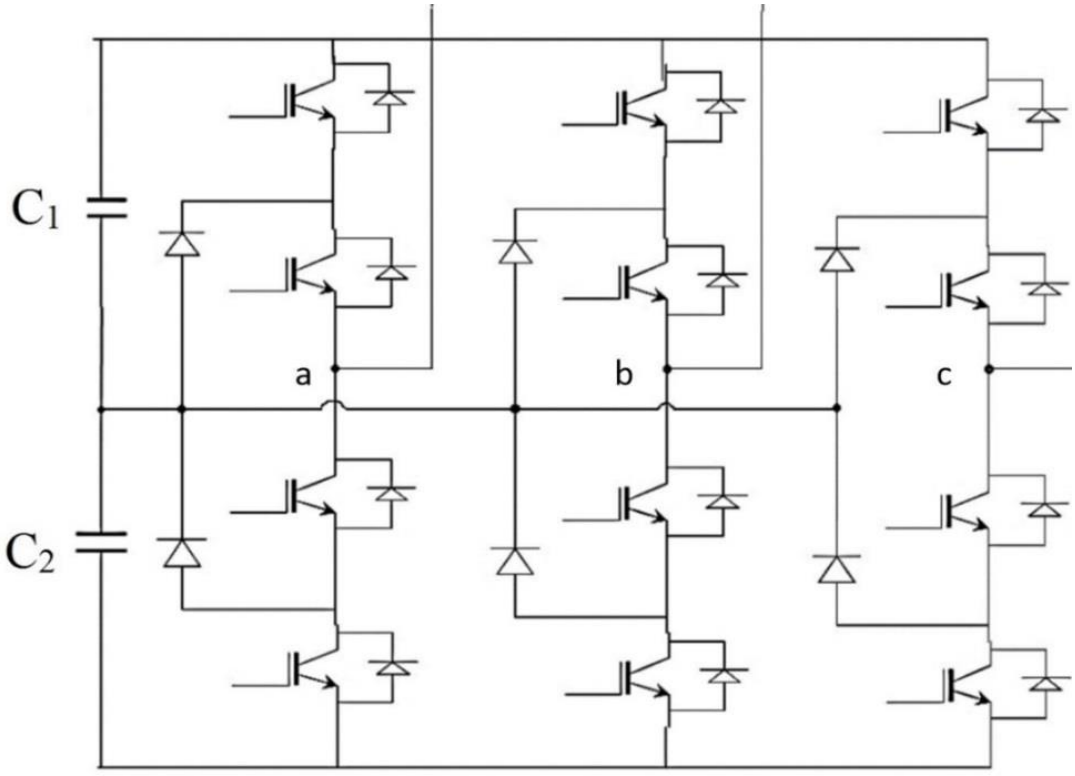


(a) (b)

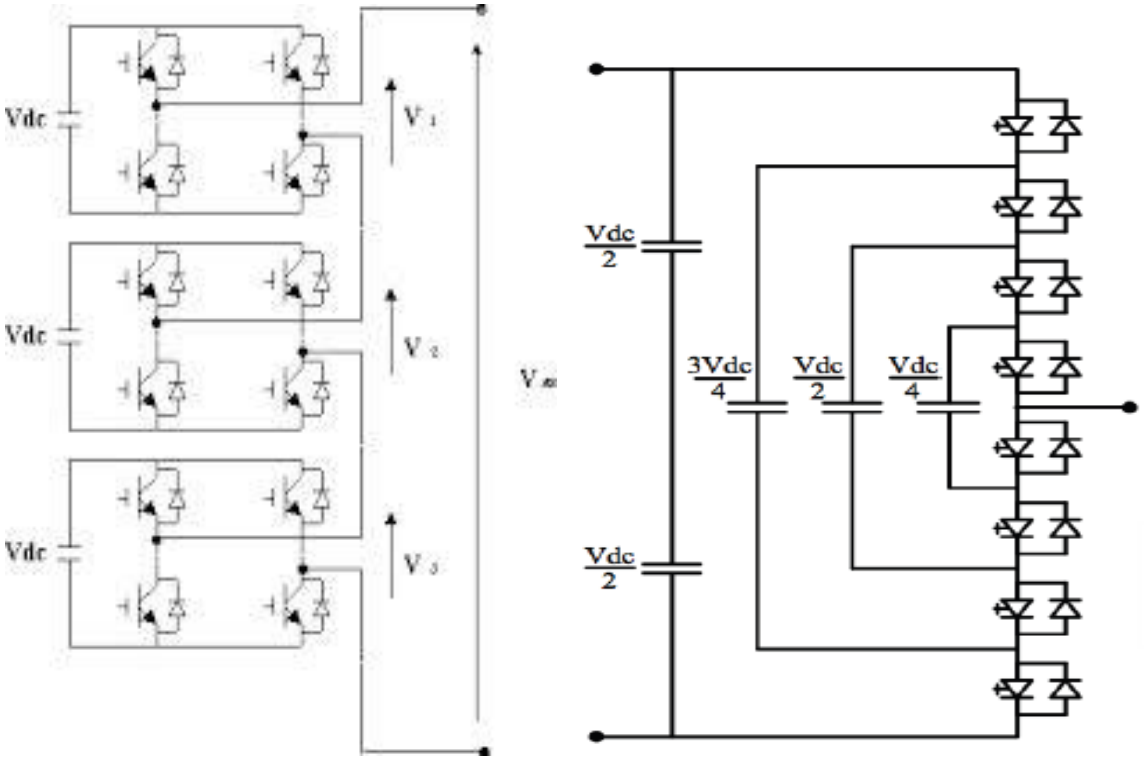
Fig. 2.2 PWM converter topologies (a) Voltage source inverter (b) Current source inverter

2.3 Multilevel voltage source Inverter

Multilevel inverter topologies are able to provide higher output voltages and power ratings with low voltage rating semiconductor devices. More output voltage states are available for multilevel inverter than 2-level hence the current controller has better option to choose the voltage state of inverter. This reduces the switching frequency of inverter. Lower voltage stress on switches also increase their life. Multiple inverter requires larger no. of components and are costly than 2-level inverter, but they are necessitated in case of higher voltage operation. Multilevel inverter has three main topologies Neutral point diode clamped inverter, flying capacitor multilevel inverter, cascaded h-bridge multilevel inverter.[12-15] Fig 2.3 shows above mentioned multilevel inverter topologies.



(a)



(b) (c)

Fig.2.3 Multilevel inverter topologies (a) 3-Level diode clamped inverter (b) Single leg of 7-level cascaded H-bridge inverter (c) Single leg of 9-level flying capacitor inverter

Diode clamped inverter require different voltage rating of clamping diodes hence the modularity is lost and makes fabricating difficult. Flying capacitor multilevel inverter requires pre charging circuit and Cascaded H-bridge inverter requires isolated DC sources. Table I compares the multilevel inverter topologies. In this study 3-level diode clamped inverter is chosen for easy implementation of SAPF. Fig. 1.3(a) shows a 3-level diode clamped inverter. 3-level Neutral point inverter has three voltage states in a phase -Vdc/2, 0, Vdc/2 by switching appropriately.

Table I

Comparison of different multilevel Inverter topologies

Issues	**Diode clamped multilevel inverter**	**Flying capacitor multilevel inverter**	**Cascaded H-bridge inverter**
Specific requirements	Clamping diodes	Additional capacitors	Isolated DC sources
Modularity	low	High	High
Design and implementation complexity	low	Medium(capacitor pre charging circuit)	Medium
Control concern	Voltage balancing	Voltage setup	Power sharing

2.4 Control technique of SAPF

SAPF control consist of three parts :

1. Measurement of current and voltages and subsequent signal conditioning.
2. Generation of the reference currents for VSI inverter.
3. Generations of the gate pulses for the VSI inverter .

2.4.1 Measurement and signal conditioning

For the implementation of the various control algorithm the measurement of supply voltages, DC capacitor voltage and measurement of supply current, load current, and filter current are needed. For the measurement of voltages and currents transducer must be highly accurate, linear, easy setup and quick response and must not load the system, should provide isolation. Mostly Hall Effect sensors are used for this purpose because of availability and usefulness. The sensed signal may be sometimes filter and conditioned and scaled properly.

2.4.2 Generation of Reference Currents

SAPF should draw current equal to the load harmonic current but opposite in phase. There are many ways for harmonic current extraction such as instantaneous reactive power theory, ABC theory, synchronous reference frame approach etc.[4-11] But for the case of undistorted power supply feeding a balanced three phase nonlinear load most of the technique gives similar results. Here strong AC source is considered and source impedence is neglected so that voltage at point of common coupling is undistorted. In this study instantaneous reactive power theory is used for generation of reference filter current.[5-8] Control schematic of Instantaneous reactive power theory is shown in Fig. 3. The instantaneous reactive power theory is based on the αβo transformation which transforms three phase voltages and currents into the αβo stationary reference frame. From these transformed quantities, instantaneous real and reactive power of the load is calculated which consists of DC component and an oscillating component. The oscillating component is extracted using high pass filter. The oscillating real power is then added to ploss signal from outer capacitor voltage control loop which accounts for the extra power inverter has to draw because of switching losses to maintain the Capacitor voltage constant. And by taking inverse α-β transformation compensating command signals in terms of currents are derived.

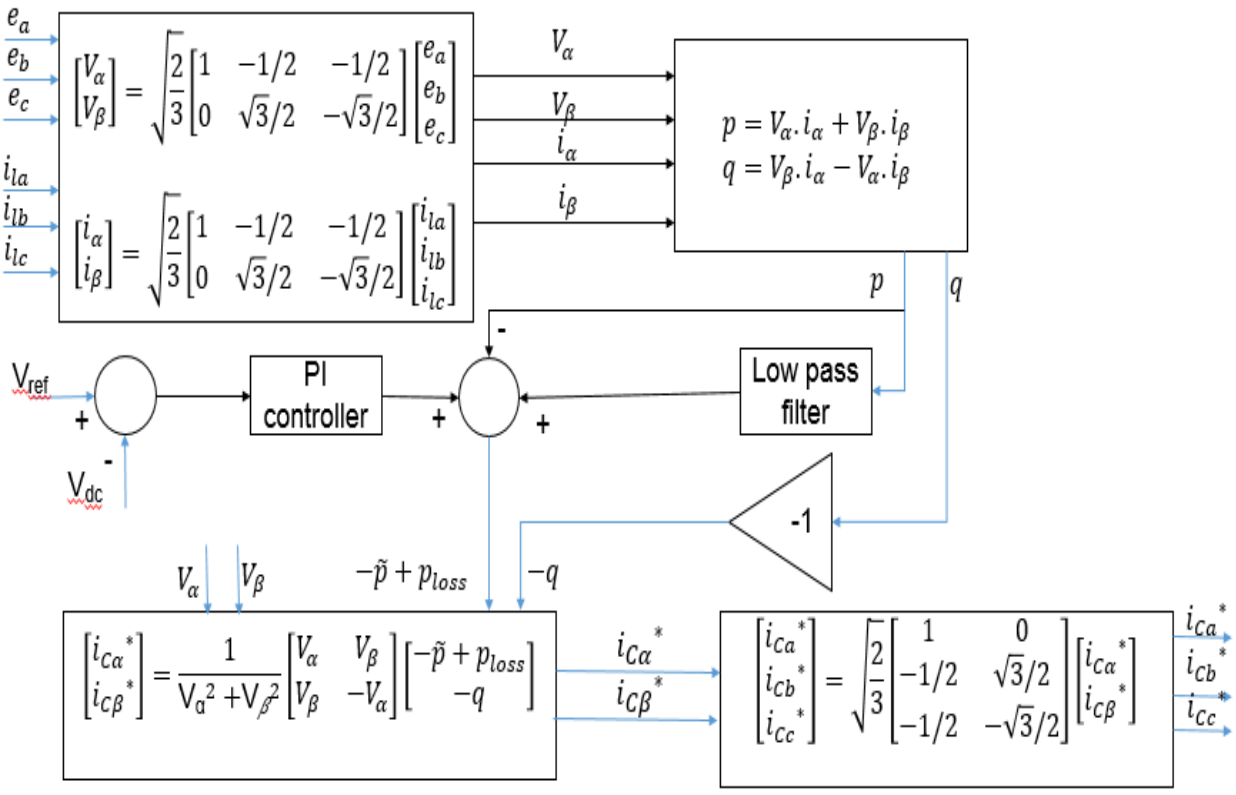


Fig.2.4 Reference current generation using instantaneous reactive power theory

2.4.3 Generation of firing pulses for the VSI inverter

Many current controllers for VSI inverter have been studied. Some of the techniques are PWM techniques, hysteresis control, space vector based PWM, adaptive hysteresis current control, space vector based HCC(SVHCC), and predictive controllers. Hysteresis control, nearly constant frequency SVHCC, and predictive controller is taken for comparative analysis in this study. Further discussion on these techniques will be done in chapter 3.

2.5 Design of SAPF parameters

Selecting the optimal parameter for SAPF is important for its efficient and cost-effective operation. The three main parameters which greatly affect the performance are discussed here.

2.5.1 Selection of reference value of dc side capacitor voltage, Vdc

Selection of reference value depends on PCC voltages in three phases. Reference DC value should be at least that much that it can force the desired current in the connecting inductor. Also keeping larger value of reference voltage will increase the size of capacitor and inductors unnecessarily and will also decrease the life of equipment. The minimum reference voltage to be kept depends on the reactive and harmonic power to be compensated. If I_{filter} is the filter current required than minimum voltage required to force this current across inductor in alpha-beta frame will be[11]

$$V_{dc} = L\frac{di_{filter}}{dt} + E$$

So V_{dc} should be greater than PCC voltage E. Magnitude of PCC voltage in α-β frame will be

$$E = \frac{3}{2} * e_{peak(phase)}$$

Phasor should be within space vector structure, so

$$\frac{\sqrt{3}}{2} * V_{dc} > \frac{3}{2} * e_{peak(phase)}$$

So minimum value of V_{dc} should be

$$V_{DC} > \sqrt{3} * e_{peak(phase)}$$

2.5.2 Selection of filter inductor value, L

Filter inductor should allow the flow of compensating current which include the harmonic components of load current. It should also reduce the high frequency switching harmonics. In hysteresis control current ripple is limited by the hysteresis band, so if inductor value is low than the hysteresis band limit will be reached quickly and hence more number of switching will take place. If the inductor value is large controller will be slow or unable to follow the quick reference current changes. This will deteriorate THD of SAPF. Hence one has to balance between these two requirements. For a hysteresis control the maximum value to be considered[11]-

$$L_{max} = \frac{(\frac{V_{dc}}{\sqrt{2}} - \frac{V_{line}}{\sqrt{2}})}{\Sigma(n * w_n * I_n)}$$

Where n is the maximum order of harmonics which are present significantly in the load current, w_n is the frequency of nth harmonic, and I_n is the harmonic content in the load current, which can be known by FFT analysis.

I_n is the rms current of nth harmonic. V_{line} is PCC voltage.

For control techniques where switching frequency can be set by the designer such as SPWM, Constant frequency HCC or predictive controller technique inductor value should be selected such as to keep the current ripple in limit. Attenuation of current ripple is the consideration here.

The maximum harmonic voltage will be at frequency $m_f * w_0$,so ripple current at this frequency is

$$I_{ch} = \frac{V_{ch}(m_f w_0)}{m_f * w_0 * L}$$

Where m_f is the frequency modulation ratio of the PWM, w_0 is the fundamental frequency. V_{ch} can be calculated using ref.[32].

2.5.3 Selection of dc capacitor voltage, Cdc

Capacitor should be able to maintain the DC voltage nearly constant as the load draws and supplies current from capacitor. Capacitor value depends on the allowed voltage ripple in dc side voltage –

$$C_{dc} = \frac{\pi * i_{filter}}{\sqrt{3} * w * V_{dr,p-p\ max}}$$

Where $V_{dr,\ p\text{-}p}$ is maximum allowed ripple in the DC voltage, w is the fundamental frequency.

CHAPTER 3

Current controllers for Shunt Active Power filter

PWM controller generates the pulses for switching of semiconductor switches such that actual filter current is able to track the reference filter current. Controller should switch the voltage state of the inverter such that filter current tracks the reference current as closely as possible in minimum number of switchings. Many current control techniques exist for the control of SAPF.[16-31] In this study hysteresis controller, space vector based hysteresis controller and predictive controller are studied for a 3-level diode clamped inverter based SAPF.

3.1 Hysteresis current controller

3.1.1. Principal of operation

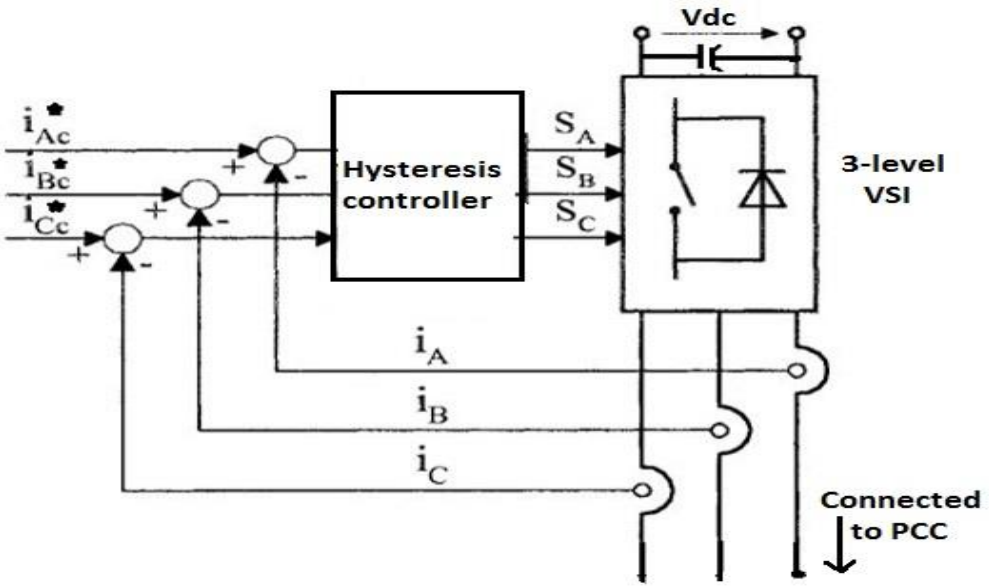


Figure 3.1: Hysteresis current controller

Hysteresis current control scheme for a three-level SAPF is shown in fig.3.1. In hysteresis current control actual filter current in a particular phase is allowed to deviate from reference current within a band. Voltage at inverter legs is switched such that current error($i_c - i_c^*$) remains within a band('h') i.e. within a limit. The logic used for switching a 3-level Neutral point clamped inverter is shown in Table 1.

Table II

Switching logic for hysteresis current controller

VSI	e >+h	-h<e <h	e<-h
3-level diode Clamped inverter	S1 ON	S1 OFF	S1 OFF
	S2 ON	S2 ON	S2 OFF
	S3 OFF	S3 ON	S3 ON
	S4 OFF	S4 OFF	S4 ON

If the actual filter current in a phase exceeds the reference filter current more than the hysteresis limit(‘h’) than a –Vdc/2 voltage is applied by the inverter to decrease the current through the inductor. This brings the current error within the hysteresis limit, when current error is within the hysteresis limit ‘0’V voltage is applied by the inverter, to maintain the current error within the limit. Similarly when current error is negative ,+vdc/2 is applied. Hysteresis control is easy to implement but its switching frequency varies with reference current and PCC voltage. Switching in the three phases is uncoordinated, hence average switching frequency is more than space vector based hysteresis controller. To put a limit to maximum switching frequency an additional circuit can be used.

3.1.2 Simulation results

Hysteresis controller for the SAPF shown in the Fig.2.1 is simulated. The essential parameter for simulation taken are Supply voltage(peak) =220V phase, Coupling inductor=3.73mH, DC capacitor =1000μF, Capacitor voltage=500V. Load current=12.4A rms and 25A rms. SAPF is switched on at t=0.08 and Load is changed at t=0.18, Hysteresis band(h)=0.1.

Simulation results of hysteresis controller based SAPF are shown in Fig. 3.2. As can be seen in Fig.3.2(c) when at t=0.08 filter is switched on source current becomes sinusoidal. In fig. 3.2(d) we can see that filter current is able to track the reference current accurately. The DC capacitor

voltage is able to stabilize after the transient at t=0.18. The source current THD before the filter is switched is 29.2% and after filter is switched on filter is able to reduce source current THD to 5.75%. The harmonic spectrum of source current can be seen in Fig 3.3. No definite peak can be seen in higher order harmonics because switching frequency is varying in hysteresis controller with refernce current and PCC voltage.

In case second, hysterseis band and maximum frequency is taken such as average switching frequency is nearly ~12kHz. Other parameters and load for simulation were taken same as the case for 3.2.1. As can be seen by results switching in the three phases is uncoordinated, hence average switching frequency is more than space vector based hysteresis controller, this increases the switching losses in the inverter.[12-15]

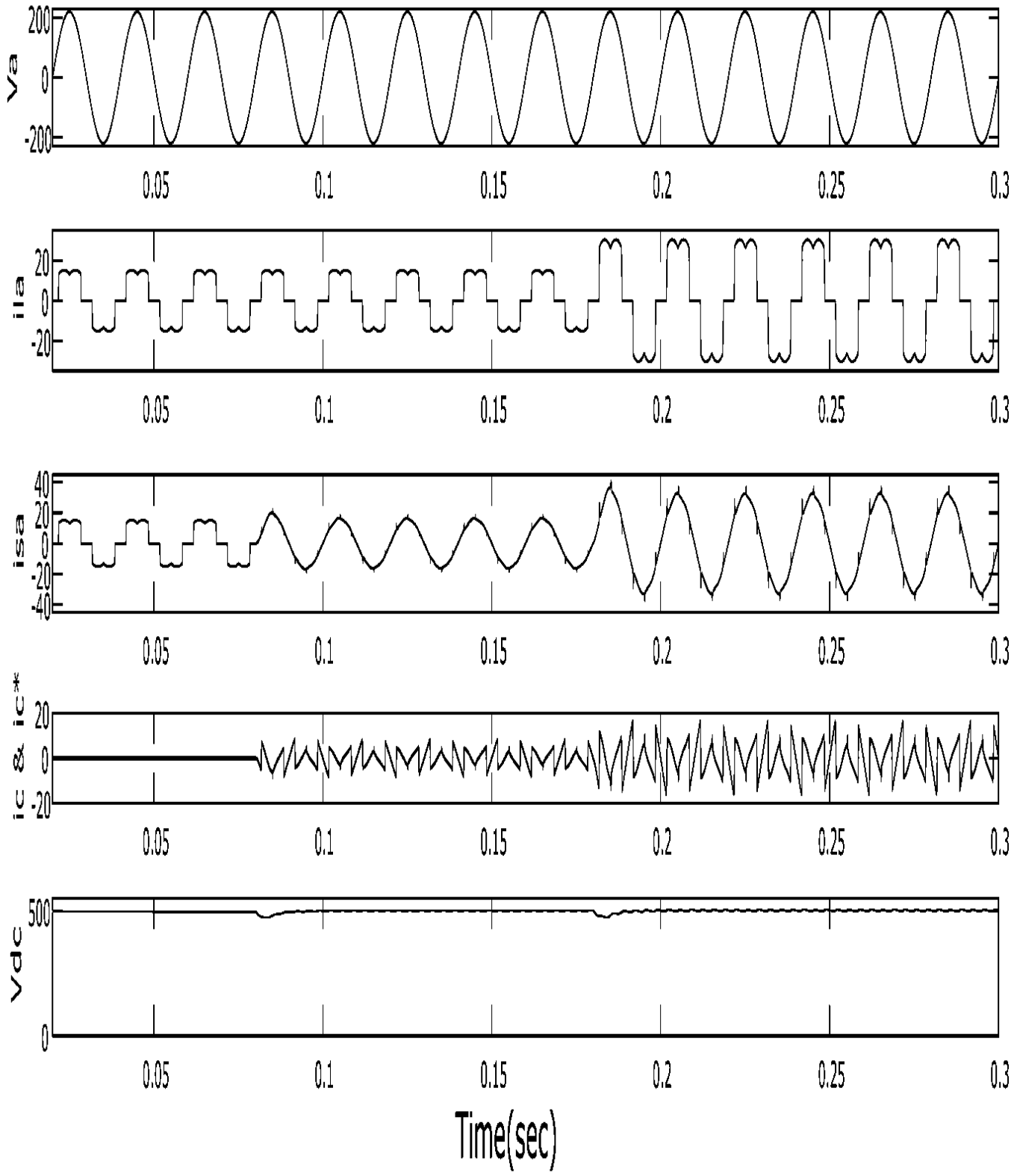
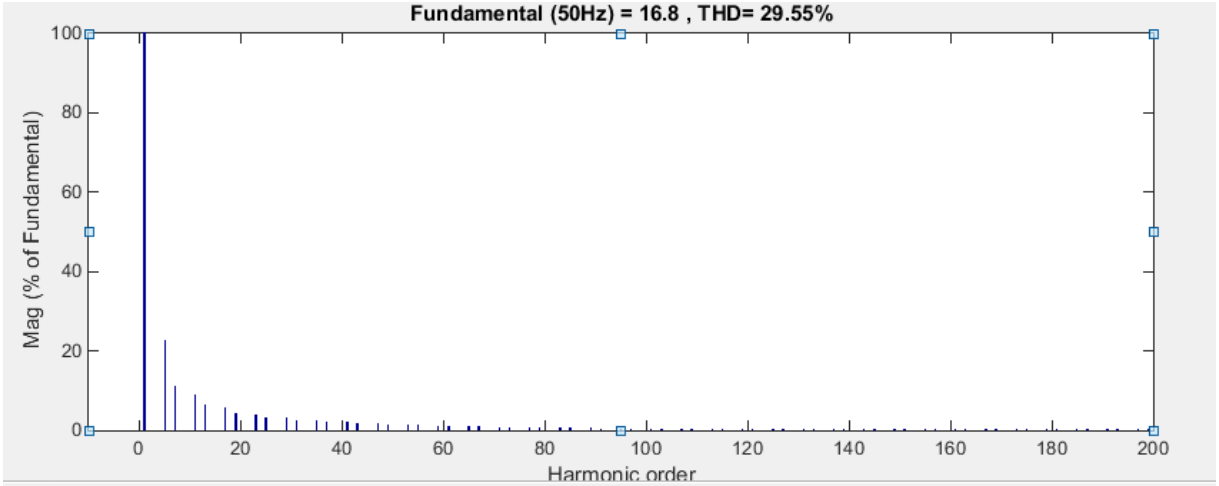
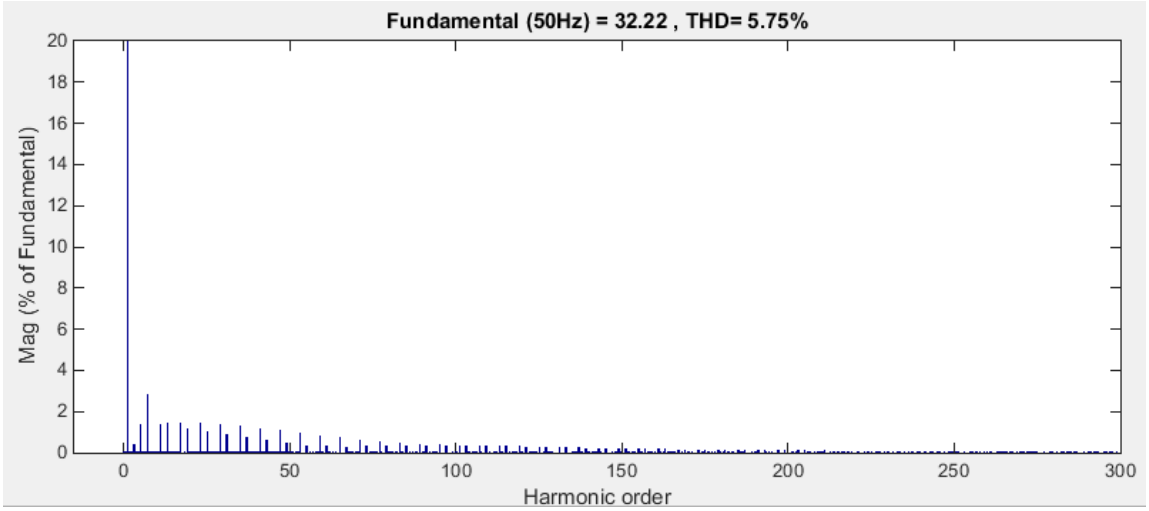


Fig.3.2 Hysteresis controller based SAPF (at t=0.08 filter is switched on, at t=0.18 load is changed) : (a) Supply voltage in phase A(volt) (b) Load current in phase A(Amp) (c) Source current phase A(Amp) (d) actual and reference compensator current (Amp) (e) Capacitor voltage



(a)



(b)

Fig.3.3-Harmonic spectrum of (a) Load current (b) source current for Hysteresis control

Simulation results when average switching frequency is less

Hysteresis control has high switching frequency variation, and for practical purposes there is need to limit the maximum switching frequency. Additional circuit can be used to limit the maximum switching frequency as given in [33].

Here, average switching frequency was counted and parameters were selected so that average switching frequency is near 12kHz. So that comparison with other controllers can be made.

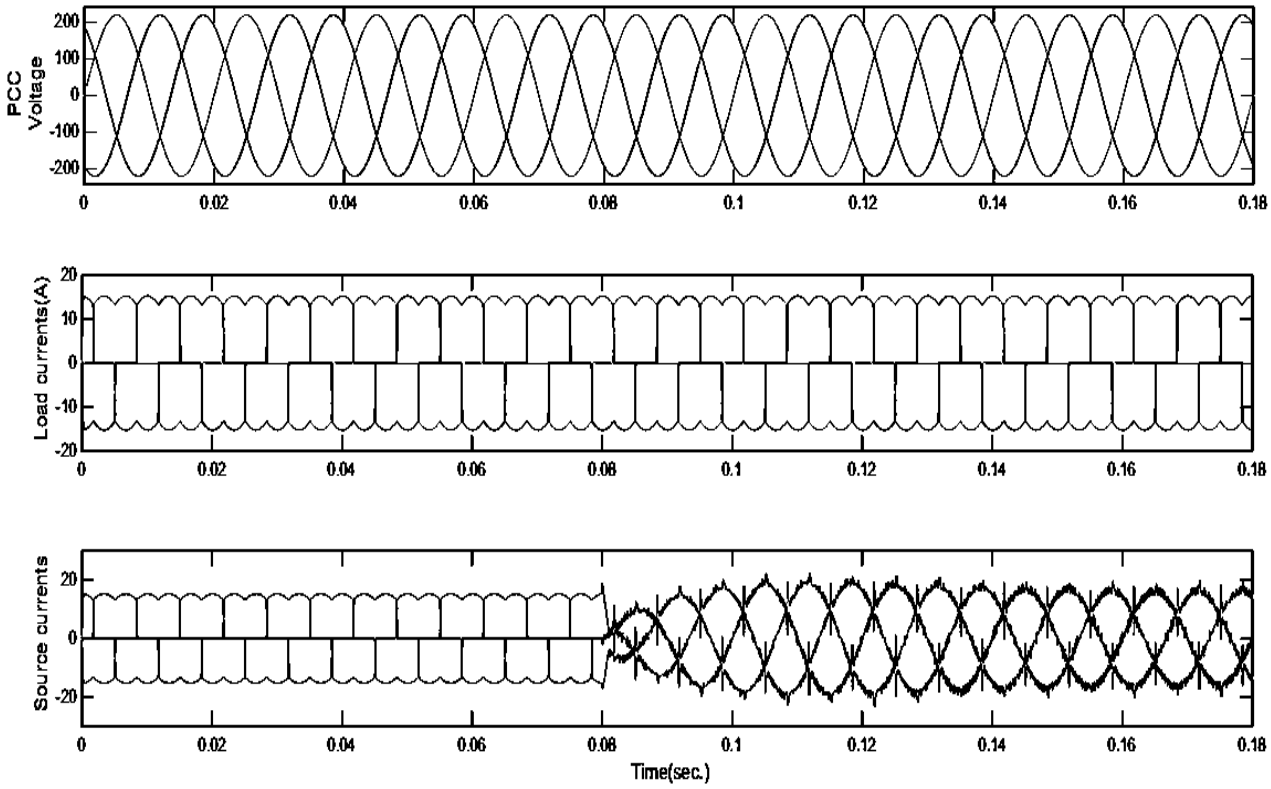


Fig.3.4 Hysteresis controller based SAPF for average switching frequency ~12Khz (at t=0.08 filter is switched on); PCC voltage(Top), Load current(middle), Source currents(bottom) (X axis=0.02sec./div)

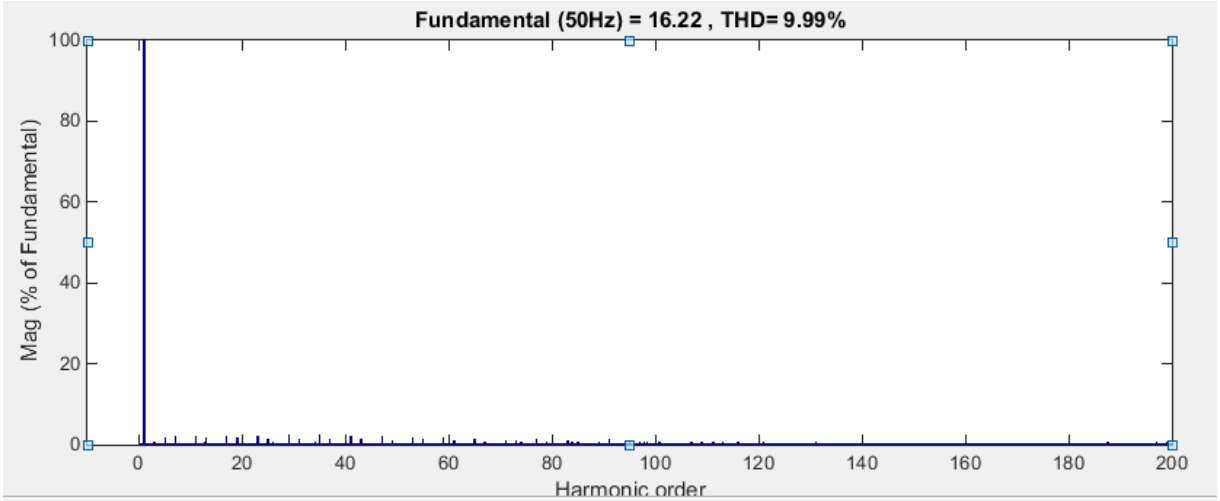


Fig.3.5 THD of source current for HCC based SAPF for less switching frequency

3.1.2.2 Performance under unbalanced load condition

In this case unbalanced load is taken with same SAPF parameters. To create unbalance resistance of 25Ω is added in phase A. The load voltages and current are shown in figure 3.6. It can be seen that load current are unbalanced.

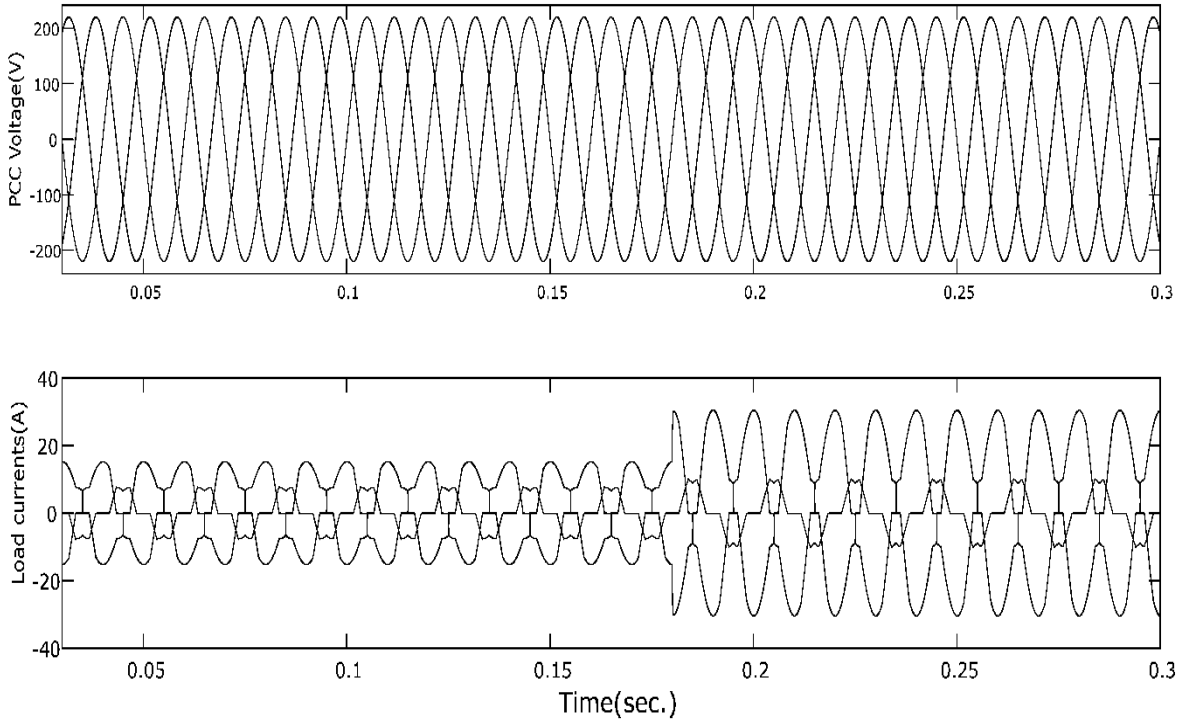


Fig.3.6-Load voltages(Top) and Load currents(Bottom) for unbalanced load conditions

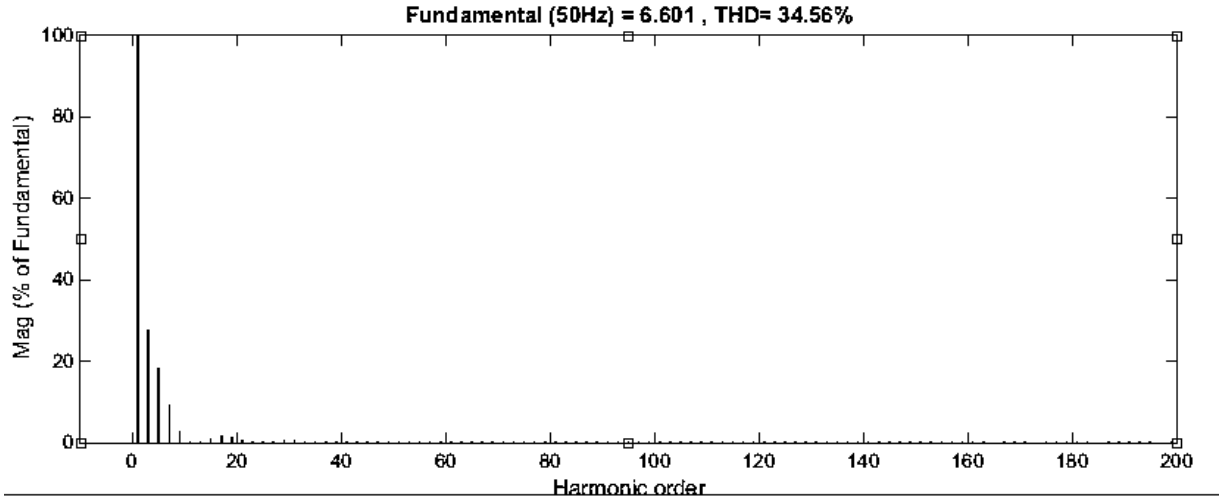


Fig.3.7-Harmonic spectrum of load current in phase A for unbalanced load condition

In fig. 3.8 Reference filter current generated by the control technique for the three phases are shown.

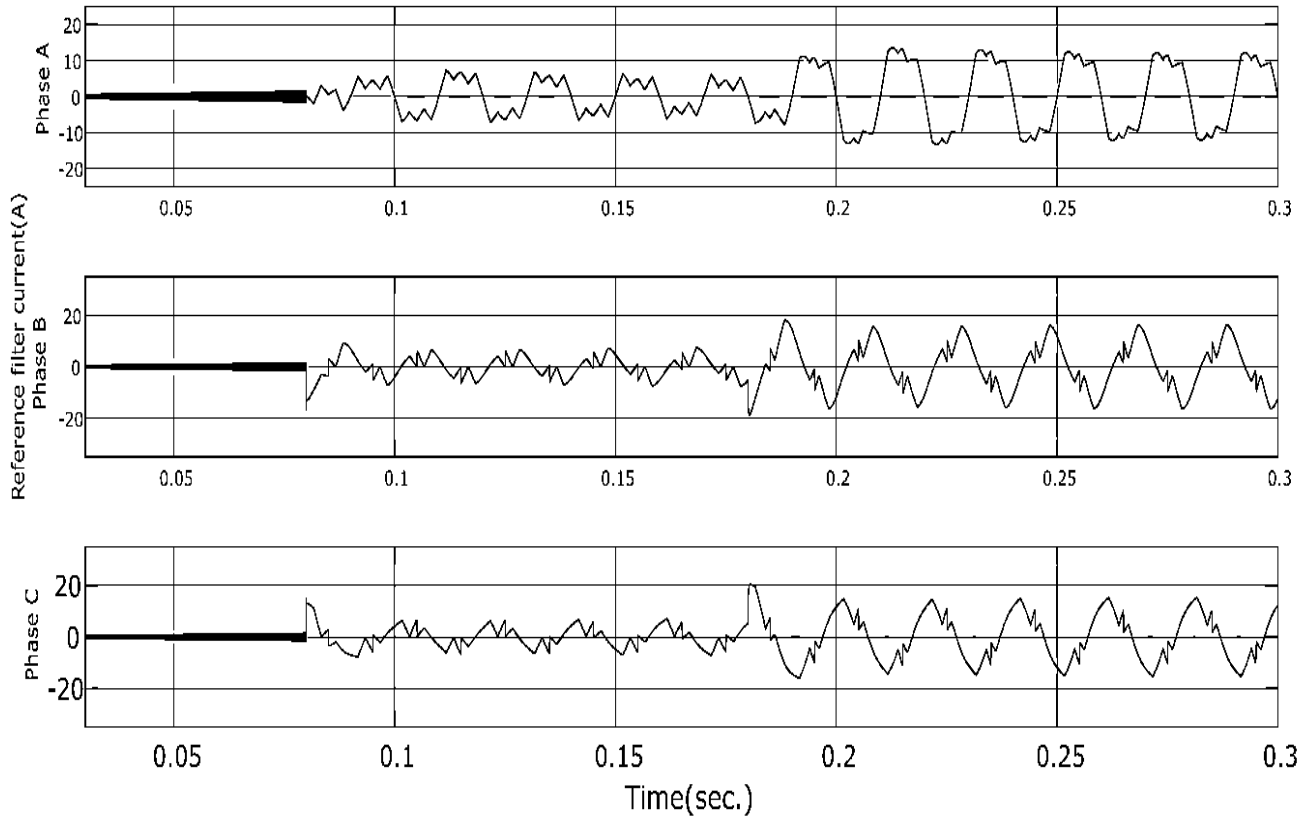


Fig.3.8-Reference filter current in three phases at unbalanced conditions

In fig. 3.9 Source voltages and source currents in three phases are shown. It can be seen that the controller is able to make source current sinusoidal and in phase with source voltage. The controller is stable after load change at t=0.18sec. Fig. 3.10 shows the harmonic spectrum of source current after the filter is switched on. SAPF is able to reduce THD of source current upto 3.03% from 34%. But if there was limit on average switching frequency than the THD will be much worse.

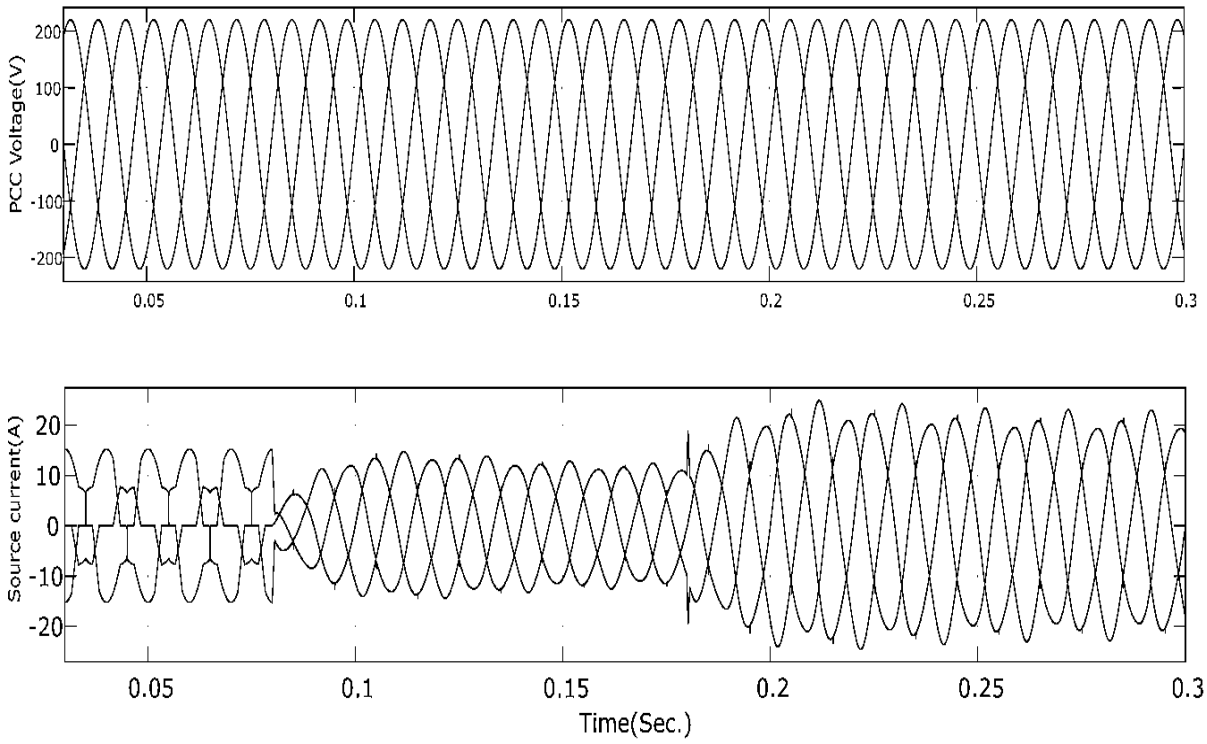


Fig.3.9-Source voltage and source currents in three phases at unbalanced conditions(with no limit to switching frequency)

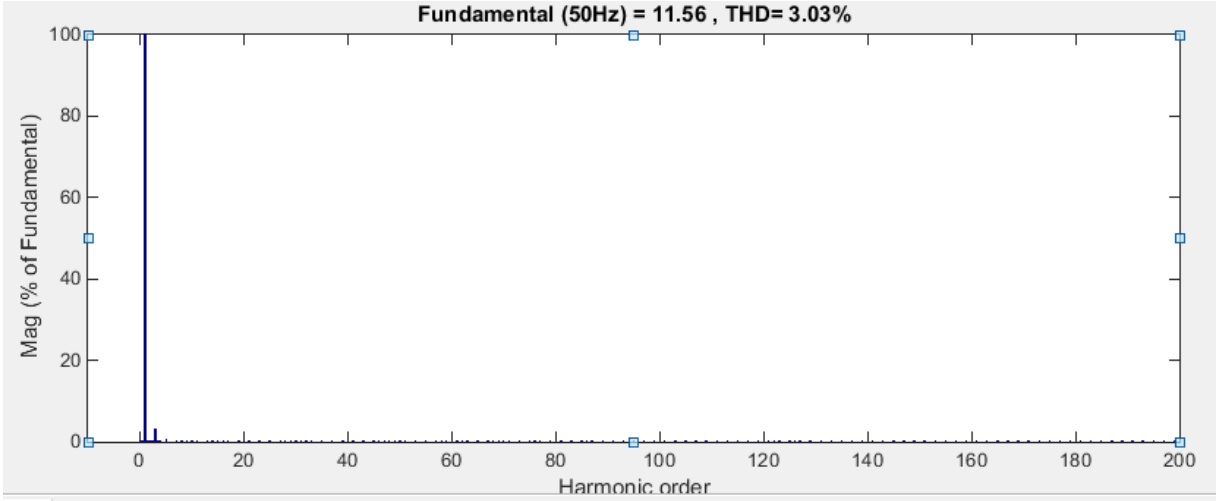


Fig.3.10- FFT analysis of source current in Phase A after filter is switched on

3.2 Space phasor based hysteresis current controller for SAPF

The conventional hysteresis current controller is simple to implement but sufferes from random and uncoordinated switching in the three phases. Space phasor based hysteresis controller(SVHCC) gives optimal switching in all the three phases, thus has less average switching frequency than the conventional hysteresis current controller. This helps in reduction in switching losses of inverter. [24-29]

3.2.1. Principal of operation

In this control method, space phasor of APF current(i_c), and inverter voltage (V_k), PCC voltage (E) are, respectively, calculated by the following equations

$$\boldsymbol{i_c} = \frac{2}{3}(i_{ca} + a i_{cb} + a^2 i_{cc}) \tag{3.1}$$

$$\boldsymbol{V_k} = \frac{2}{3}(V_{ka} + a V_{kb} + a^2 V_{kc}) \tag{3.2}$$

$$\boldsymbol{E} = \frac{2}{3}(e_a + a e_b + a^2 e_c) \tag{3.3}$$

Where $a = e^{\iota((2\pi)/3)}$ where, ι is the imaginary operator.

Also, the current error space phasor is defined as

$$\Delta i = i_c - i_c^{*} \tag{3.4}$$

Where, i_c^{*} is the reference filter current space phasor.

To limit the deviation from reference current, current error boundary is defined in space phasor structure. If the current error phasor crosses the boundary, appropriate voltage vector is applied by the inverter so that the current error reduces and remains within boundary. If current error phasor(Δi) is changing quickly, more frequently it will go out of the pre-defined boundary and so the inverter has to switch voltage vectors. To minimize switching, current error phasor (Δi) should vary slowly i.e. $\frac{d(\Delta \mathrm{i})}{dt}$ should be minimum. Ideally it should be zero as shown in equation 5.

$$0 = \frac{di_c}{dt} - \frac{di_c^{*}}{dt} \tag{3.5}$$

Now, from fig 1., applied inverter voltage phasor can be given as,

$$V_k = L\frac{di_c}{dt} + E \tag{3.6}$$

From eq. (3.5) & (3.6) we can find out the reference voltage phasor which if applied by the inverter, will produce minimum change in current error.

$$V_s^* = L\frac{di_c^*}{dt} + E \tag{3.7}$$

As the inverter can only apply finite number of voltage space phasor, in every switching cycle the voltage-second balance is maintained amongst all these adjacent phasors to get the average voltage vector of V_s^*. This results in voltage error equal to the difference between applied voltage phasor and reference voltage phasor. This voltage error will result in change in current error as

$$\frac{d(\Delta \mathrm{i})}{dt} = \frac{V_k - V_s^*}{L} = \frac{\Delta V_k}{L} \tag{3.8}$$

As explained earlier, to minimize number of switching we have to maintain this change in current error minimum as much as possible. Adjacent voltage phasors will result in minimum voltage errors and hence minimum change in current error. From these adjacent voltage phasors, the phasor which reduces current error for an instance is selected.

Finding out mapped sector and current error boundary:

To calculate voltage phasor timings, and current error boundary for a 3-level inverter, reference voltage phasor(V_s^*) is mapped to inner hexagon ($Vs^{'}$) so that the voltage switching logic and current error boundary can be defined similar to a 2-level space phasor structure (as shown in fig. 3.11).[29]

The mapped voltage reference vector $Vs^{'}$ from which modified sector (in which tip of $Vs^{'}$ lies) can be found out as shown in Table III. This modified sector or mapped sector can be used to select the adjacent voltage phasors (by detecting corresponding indices in the space phasor structure) and the estimated switching time durations similar to a two level space vector structure.

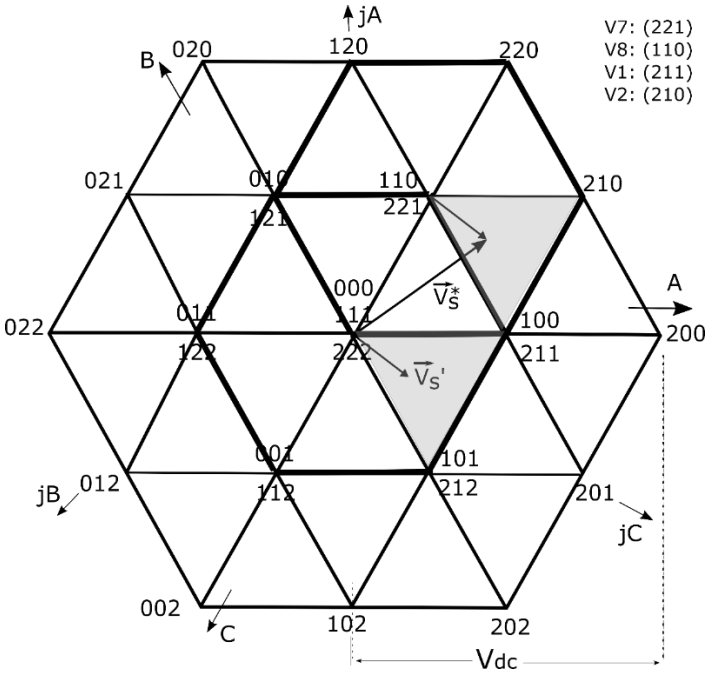


Fig.3.11 Mapping of Vs* into Vs' in 3 level space phasor structure

Table III:

Mapped sector calculation

Conditions	Mapped sector
$V'_a \geq V'_b \geq V'_c$	1
$V'_b \geq V'_a \geq V'_c$	2
$V'_b \geq V'_c \geq V'_a$	3
$V'_c \geq V'_b \geq V'_a$	4
$V'_c \geq V'_a \geq V'_b$	5
$V'_a \geq V'_c \geq V'_b$	6

Calculating current error boundary:

From eq.(8) current error vector (i_s-i_s^*) is given by

$$|\Delta i| = \frac{V_k - V_s^*}{L} = \frac{-|\Delta V_k|}{L} T_k \tag{3.9}$$

Where T_k is time duration vector V_k is applied.

Timing of voltage vectors can be calculated as:

$$T_{xs} = \frac{2 * T_s * V_x'}{L} \tag{3.10}$$

Where x=a,b,c;

From T_{as},T_{bs},T_{cs} time T1,T2,Tz can be calculated as

$$T1 = Tmax - Tmin$$
$$T2 = Tmax - Tmid \tag{3.11}$$
$$Tz = Ts - T1 + Tz$$

where Tmax=max(T_{as},T_{bs},T_{cs}), Tmid=mid(T_{as},T_{bs},T_{cs}), Tmin=min(T_{as},T_{bs},T_{cs}).

The relationship between current error and voltage error is shown in fig.3(b) When voltage vector V_1,V_2,V_z, is applied current error moves in the direction opposite of ΔV_1, ΔV_2, ΔV_z.

Current error boundary can now be calculated from eq. (3.10),(3.12). It can be noted that current error for a voltage vector in a particular sector has maximum projection along only one of the orthogonal axis from jA,jB,jC axis. So only one boundary check is enough for change of voltage vectors. For mapped sector 1, the current error boundary in all three axis can be calculated as in (13)

$$\Delta i_{1(jA)} = \frac{-|\Delta V_1|_{jA}}{L} T_1, \qquad \Delta i_{2(jB)} = \frac{-|\Delta V_2|_{jB}}{L} T_2, \qquad \Delta i_{3(jC)} = \frac{-|\Delta V_1|_{jC}}{L} T_z \tag{3.12}$$

Finally, the vector switching logic table for current control in mapped sector 1 is given in Table IV. Based on the Table IV, when current error exceeds the boundary change in voltage vectors happens for mapped sector 1. Similar logic can be derived for other mapped sectors.

Table IV

Vector switching logic

Present vector	Previous vector	Next Vector		
		If (ji_A-ji_A^*) ≥ $0.5*\Delta i_{1(jA)}$	If (ji_C-ji_C^*) ≥ $0.5*\Delta i_{2(jC)}$	If (ji_B-ji_B^*)≥$0.5*\Delta i_{z(jB)}$
V_1	V_7	V_2	-	-
	V_2	V_7	-	-
V_2	V_8	-	-	V_1
	V_1	-	-	V_8
V_7	-	-	V_1	-
V_8	-	-	V_2	-

3.2.2 Improved switching logic for fast transitions of load current:

During sector change i.e at every 60 degree interval of PCC voltage waveform for Diode Bridge Rectified (DBR) load, current in two phases change suddenly from zero value to a non-zero value. This phenomenon is observed during all the bigger sector changes i.e. six times in a fundamental cycle. Due to such phase current transition in the load side, reference currents derived by IRP method also undergo similar transitions. For example, from sector 1 to sector 2,reference current in phase A and phase B suddenly changes their values from positive to negative and negative to positive respectively. But, during such periods adjacent phasors V1,V2,Vz are detected by normal SVHCC (see Fig.3.12). This will also result in small rate of change in current errors Δi_1, $\Delta i_2, \Delta i_z$ hence actual current cannot track reference current optimally(see Fig.3.13). Instead of V1,V2,Vz phasor V12'(see Fig. 3.12) is applied ,which gives maximum reduction in current error. Thus as soon as sector change is detected the voltage phasor which gives maximum reduction in the current error is applied until the current error comes within the calculated boundary.

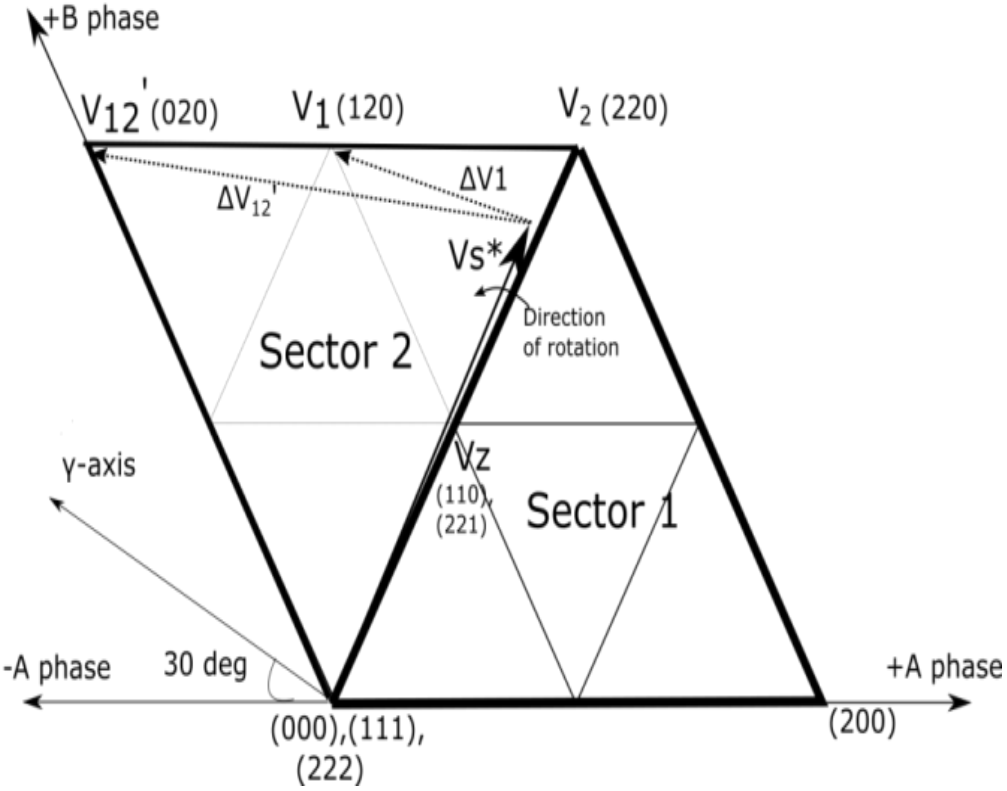


Fig. 3.12 Voltage errors during sector change from 1 to 2

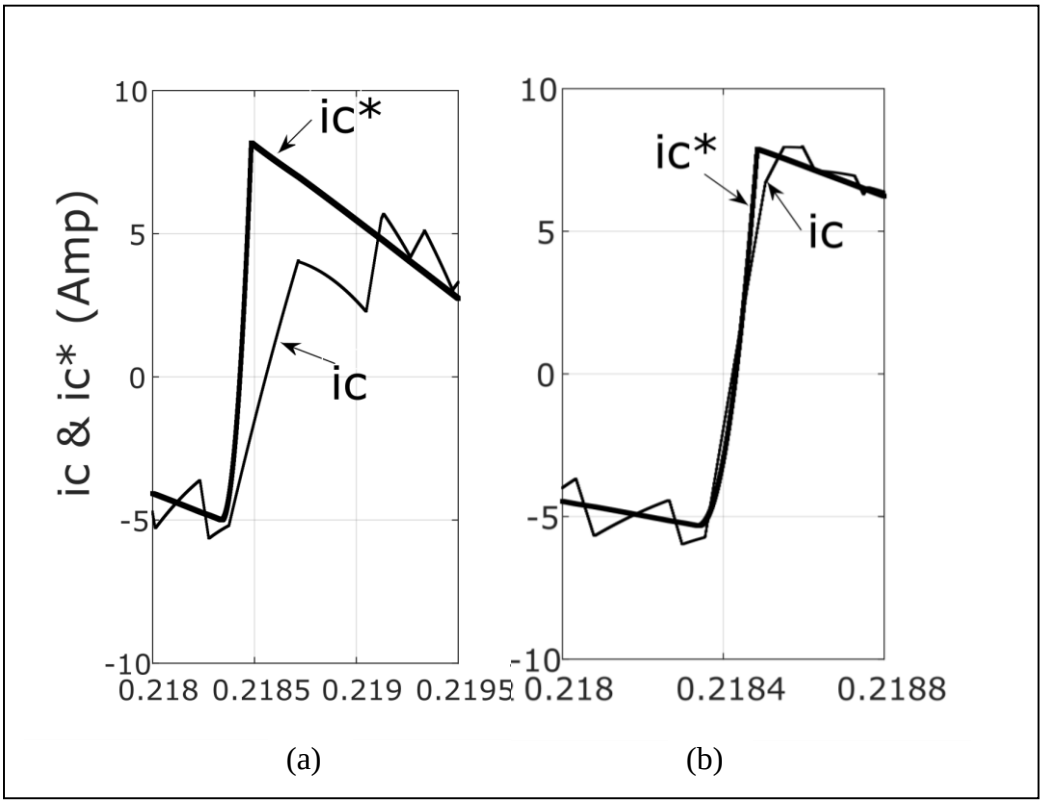


Fig.3.13 Reference current tracking during fast transition in phase A (a) without improved logic (b) with improved logic

3.2.3 Simulation results

Improved space vector based hysteresis controller for the SAPF shown in the Fig.2.1 is simulated. The essential parameter for simulation taken are Supply voltage(peak) =220V phase, Coupling inductor=2.8mH, DC capacitor =1000μF, Capacitor voltage=500V. Load current=12.4A rms, Ts=8e-5.

Simulation result for improved SVHCC is shown in Fig 3.14. Fig 3.14 shows the PCC voltage at phase A, load current in phase A, actual and refernce filter current, and source current. Controller is able to make the source current sinusoidal and it is tracking the refernce filter current accurately.

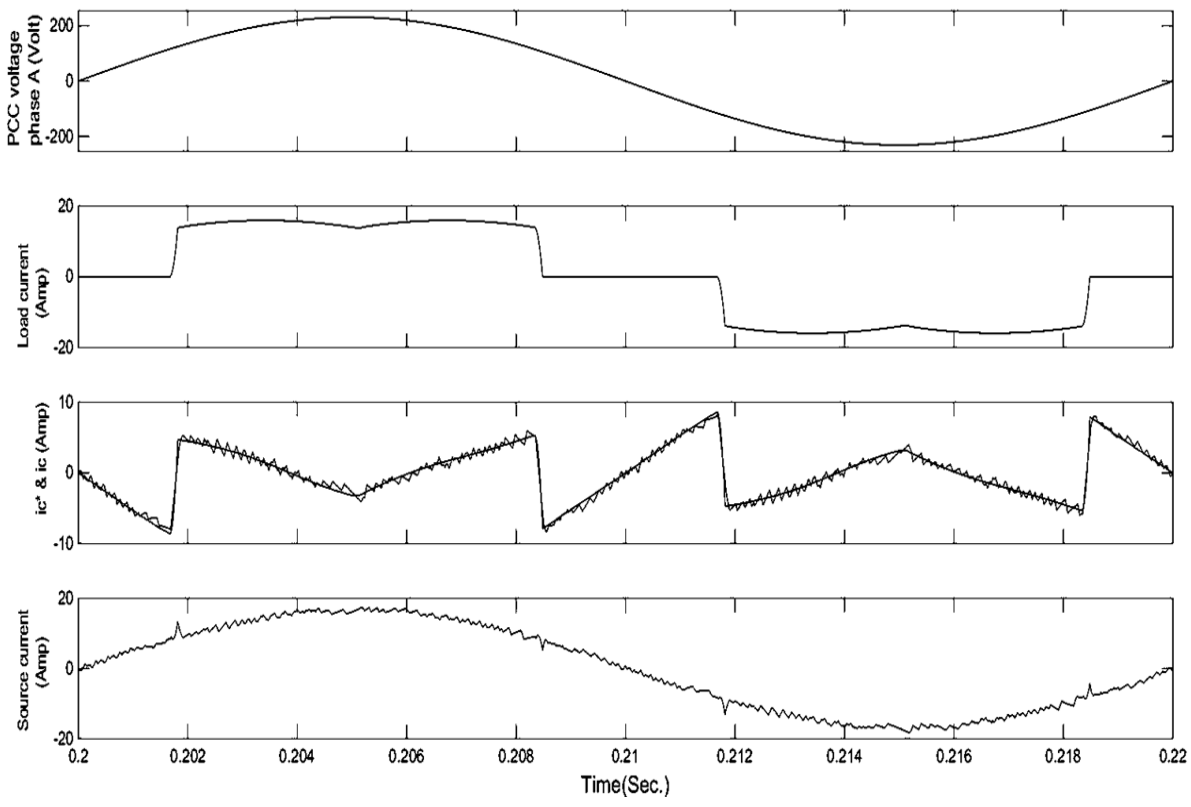


Fig.3.14-Improved SVHCC based SAPF : (a) Phase ‘A’ PCC voltage (b) Load current (c) Reference and actual filter current (d) Source current

Fig.3.15 shows the sector of reference voltage phasor, mapped sector, Voltage across terminal a & b of inverter and index of voltage vector switched from V1,V2,V7,V8.

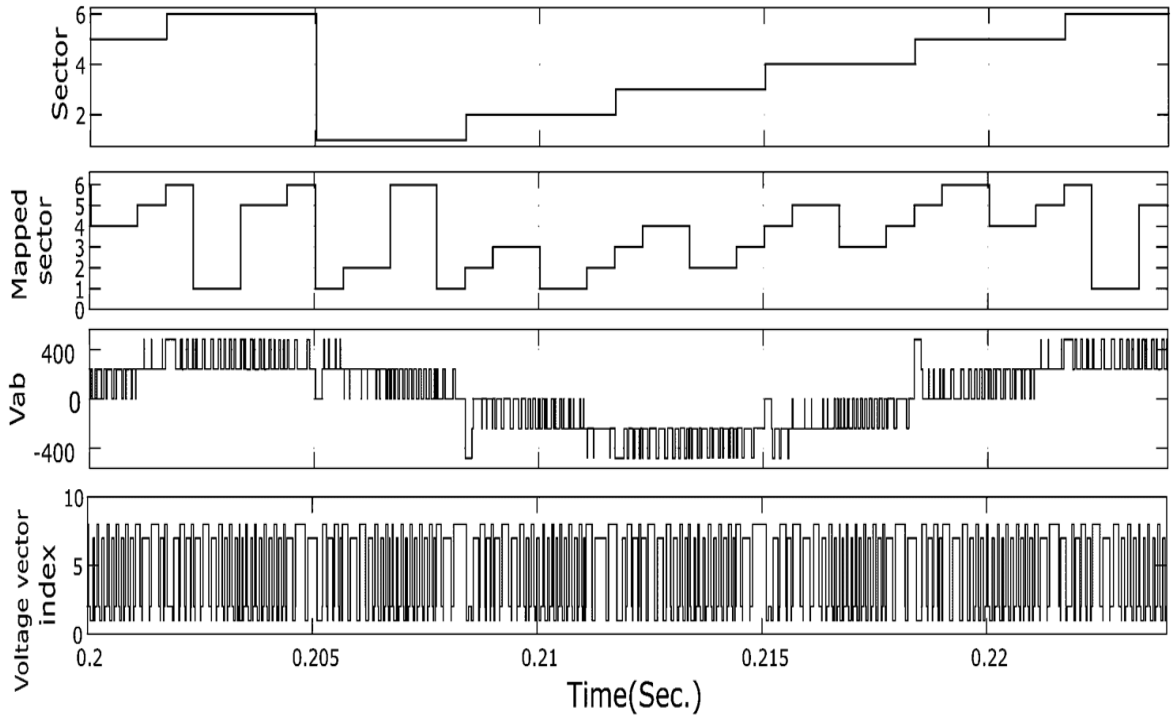


Fig.3.15-Improved SVHCC based SAPF : (a) Sector (b) Mapped sector (c) Voltage across inverter leg a & b (d) Voltage phasor switched (V1,V2,V7 or V8)

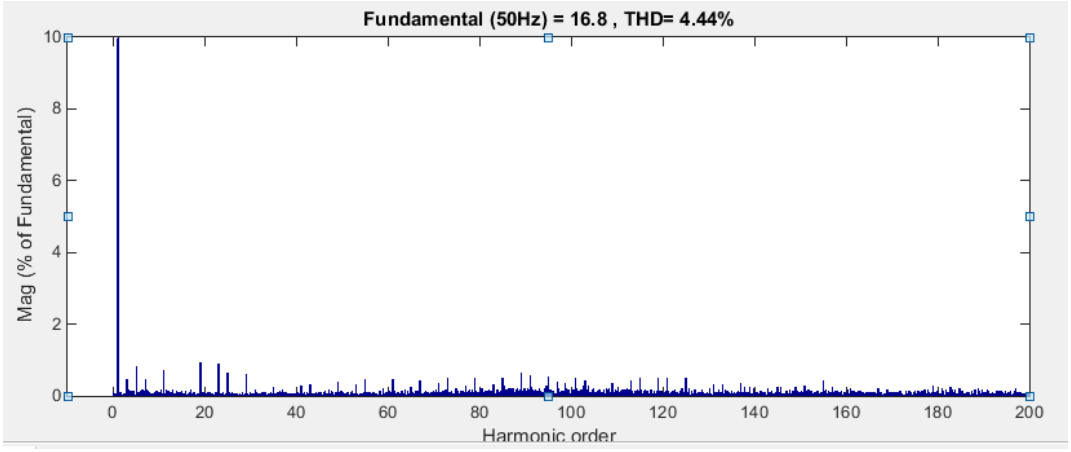


Fig.3.16-FFT analysis of source current when SVHCC with improved technique is used

Fig. 3.16 shows the FFT analysis of source current. The controller is able to improve source current THD from 29.5% to 4.4%. SVHCC has less no. of switching as compared to conventional hysteresis controller. Hence switching loasses in inverter are reduced.

3.3 Predictive controller for SAPF

Predictive control is an general term which can encompass wide range of technique. Technically, any technique in which any parameter is estimated for next sampling event can be considered in the area of predictive control. In this study a simple predictive or deadbeat control technique is simulated.[30,31]

3.3.1. Principal of operation

A Three level VSI can apply 27 voltage switching state, for each switching state filter current(ic(k+1)) is estimated for next sampling event . From it current error is calculated for the next sampling event. Voltage phasor which will give minimum error is selected to be applied for next sampling event. Flowchart of predictive control technique is shown in Fig.3.17.

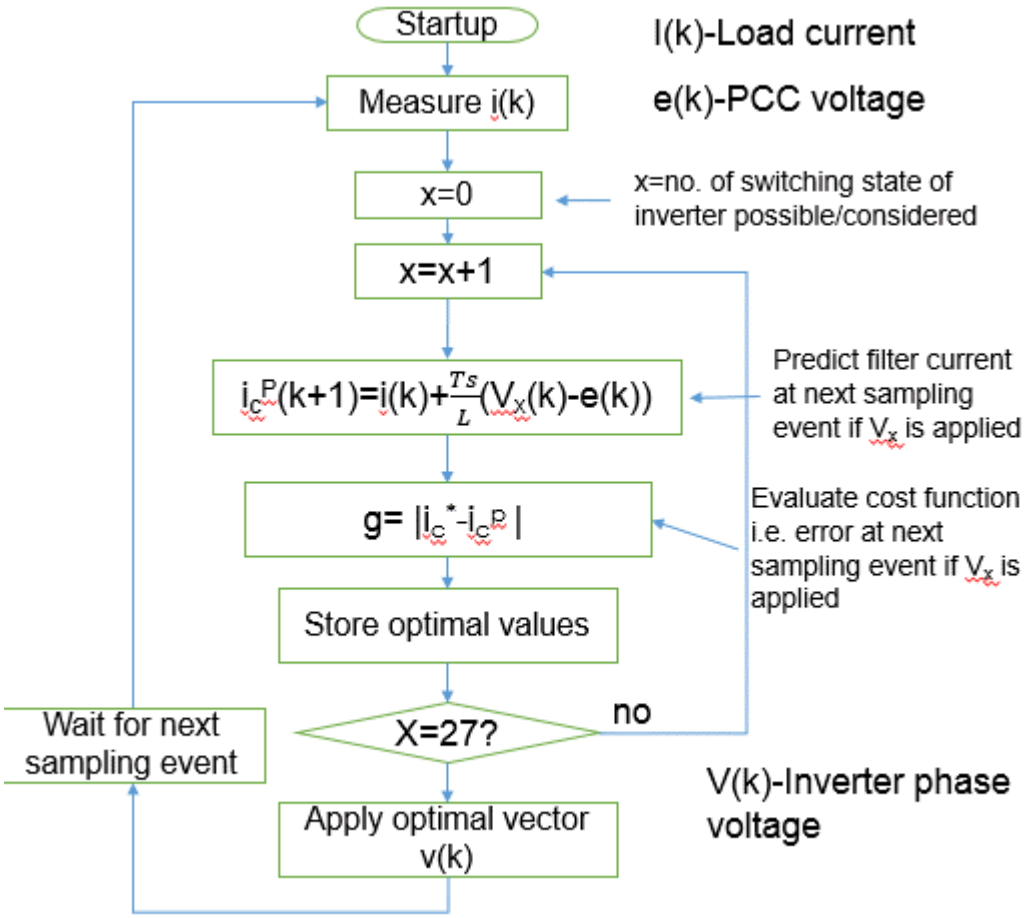


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Fig.3.17 Flowchart of deadbeat controller

3.3.2 Simulation results

Predictive controller for the SAPF shown in the Fig.2.1 is simulated. The essential parameter for simulation taken are Supply voltage(peak) =220V phase, Coupling inductor=2.8mH, DC capacitor =1000µF, Capacitor voltage=500V. Load current=12.4A rms, sampling frequency=1/(15e-5). Filter is switched at t=0.08.

8 voltage states are redundant so for only 19 states current error is evaluated. Performance of controller is shown in the Fig.3.18, 3.19,3.20 and 3.21.

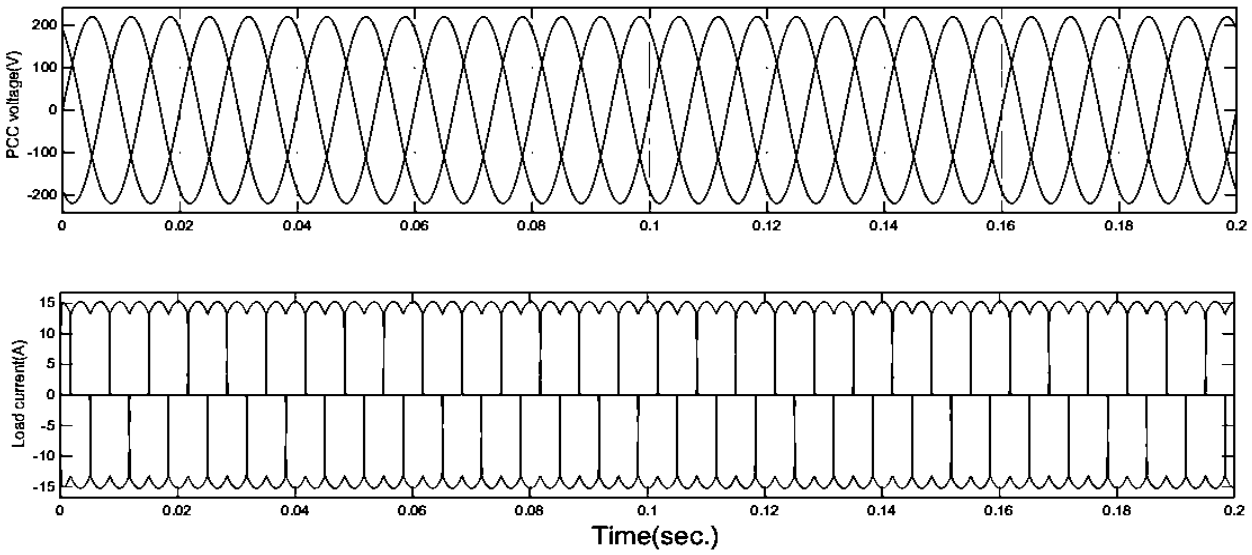


Fig.3.18-Load voltages and Load currents for predictive controller based SAPF

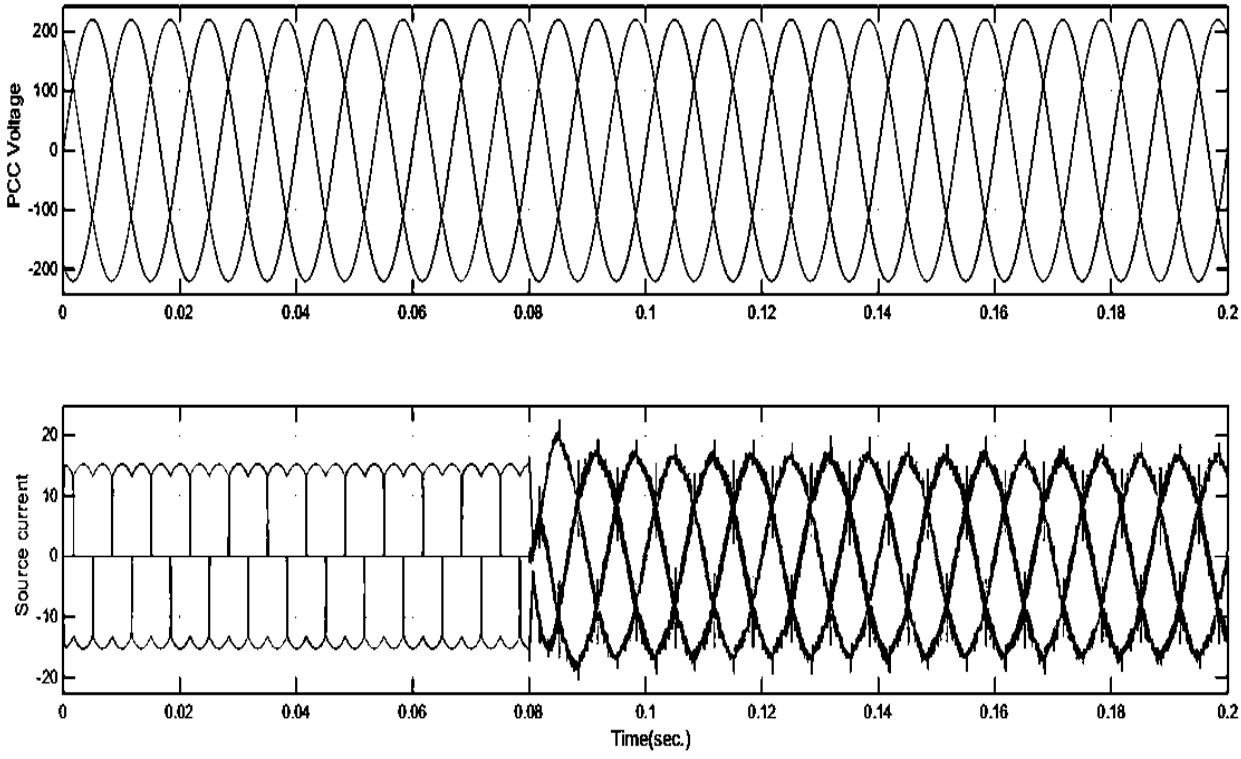


Fig.3.19-Source voltages and Source currents for predictive controller based SAPF

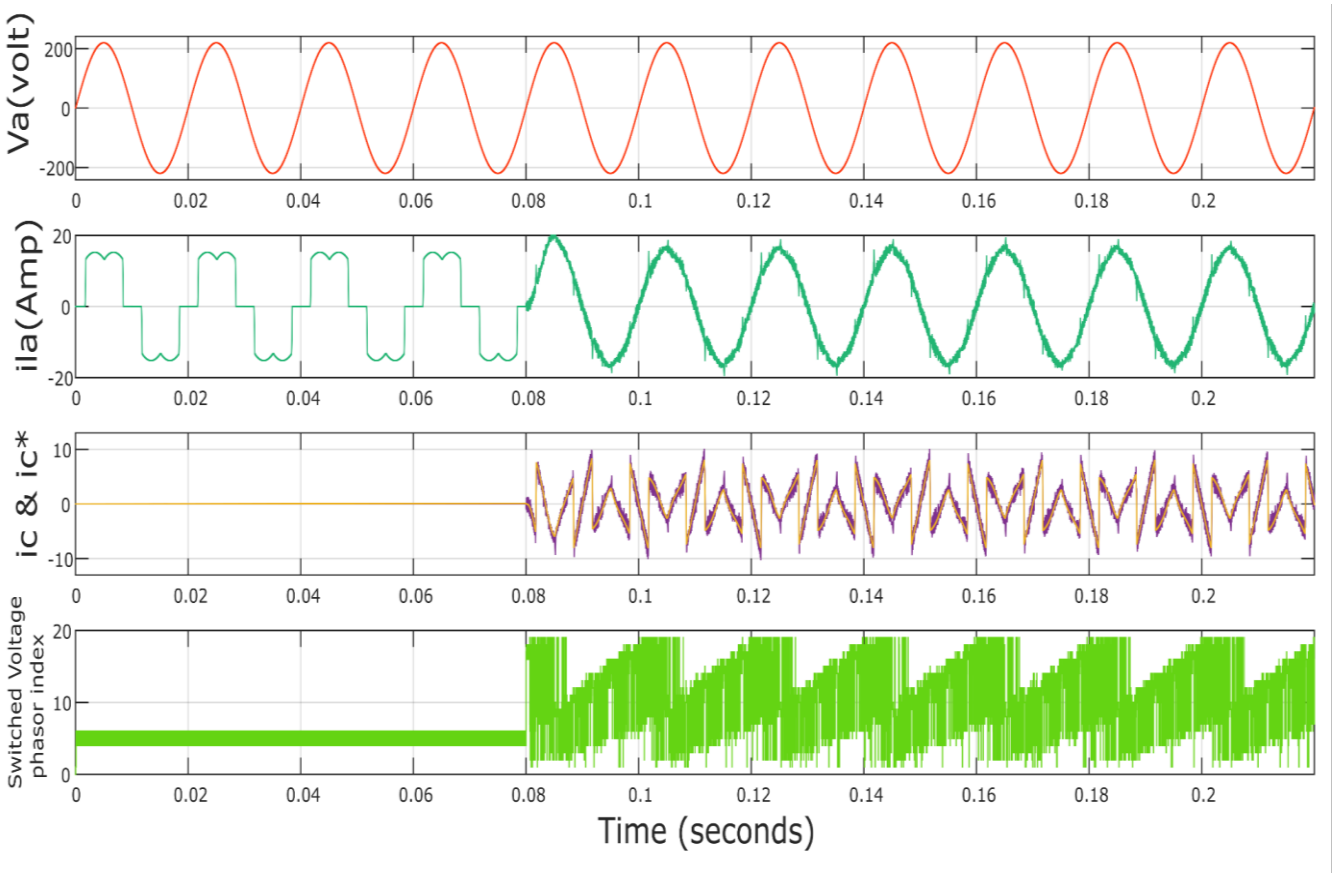


Fig. 3.20 Predictive controller (a) PCC volt in phase A (b) Source current in phase A (c) actual and refernce filter current (d) Switched voltage index (1-18)

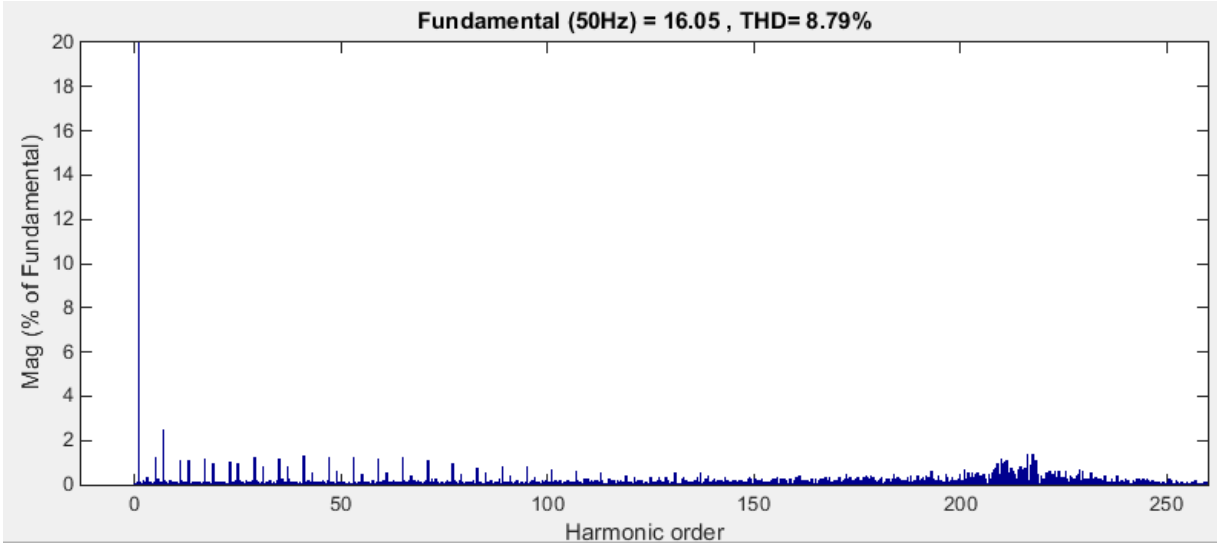


Fig. 3.21 FFT analysis of source current for predictive controller based SAPF

3.4 Comparison of different current controllers

For comparison of current controllers for multilevel inverter based SAPF the switching frequency were taken nearly same(~12kHz) for all the controllers and then THD was compared for the same SAPF system. Hysteresis current control reduces the source THD from 29.2% to 9.99%, predictive controller to 8.79% ,and SVHCC with improved technique to 7% when average switching frequency was 12kHz. New technique for voltage vector selection further improved the performance of current controller and brought the THD down to 4.4%. Hysteresis control have problems of oscillations and unccordination between three phases. It also needs additional circuitry to limit maximum switching frequency. Inductor design may become tedious as switching frequency is not constant. SVHCC eliminates these limitations of hysteresis control. Improved SVHCC gives better results when load is changing steeply. Predictive controller is suitable for digital implementation but requires large processing power.

TABLE V

Comparison of current control techniques

Control Techniques	THD of source current (Load current THD-29.4%)	Remarks
Hysteresis controller	9.99%	Easy to implement.
Space vector based hysteresis controller	7%	Improved THD because of coordination between three phases.
SVHCC with improved technique	4.44%	Further reduction in THD because of better control during steep changes of load.
Predictive controller	8.79%	Requires relatively large processing power. Needs further research, as suitable for digital implementation.

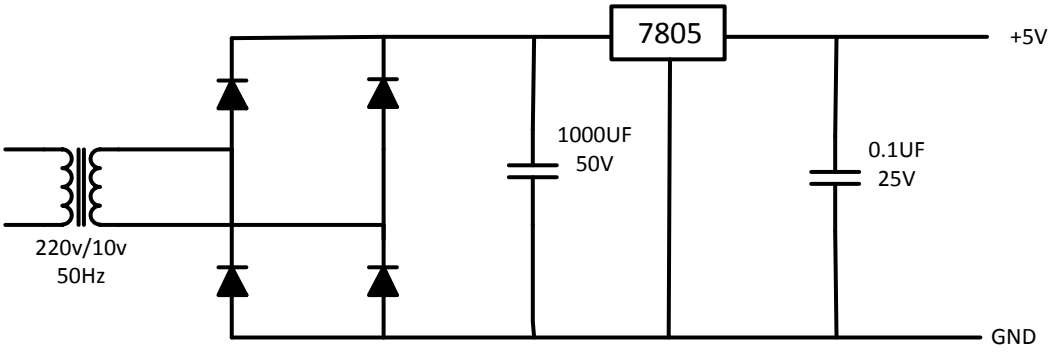
CHAPTER 4

For hardware implementation of Shunt active power filter 3-level neutral point inverter and voltage and sensing circuits were fabricated. Following parts are needed for operation of SAPF.

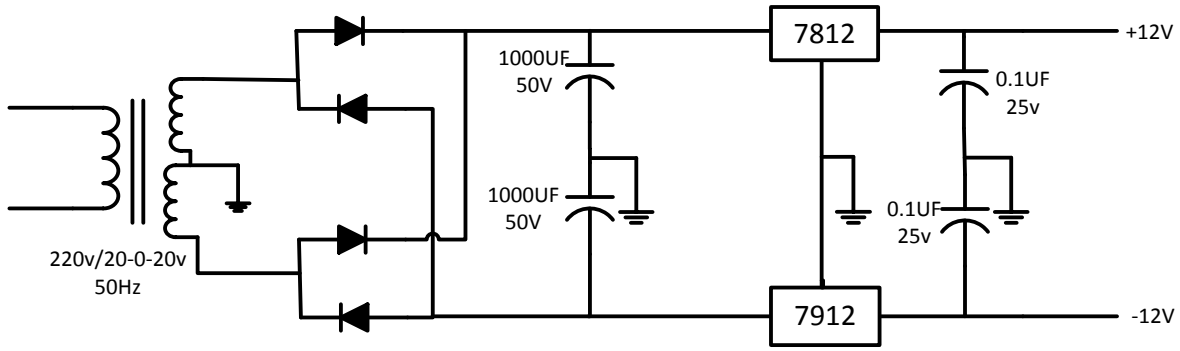
4.1 POWER SUPPLIES

DC regulated supplies (+12v gnd -12v, +5v) are required for providing biasing to various circuits like pulse amplification and isolation circuits, hysteresis controller and voltage detectors etc. IC 7812 is the voltage regulator used for +12V, 7819 for -12V and 7805 for +5V. 7812 and 7819 IC require DC input voltage in the range of 14.5 and 30V. For this a diode bridge rectifier with input transformer of 220V/18-0-18V is used. Fig 4.1 shows the circuit diagram for +12V,-12V and +5V.

A single +5V power supply is required for all the switches for the optocoupler. A single +12 0 -12V power supply is required for current sensor and voltage sensor circuit.



(a)



(b)

Fig. 4.1 Connection diagram for power supplies (a).+5v (b).-12,0,+12v

Fig. 4.2 MOSFET switch driver with snubber circuit

A single Mosfet switch driver circuit contains all the 3 circuits(power supply +12V,snubber circuit, amplification & isolationcircuit)

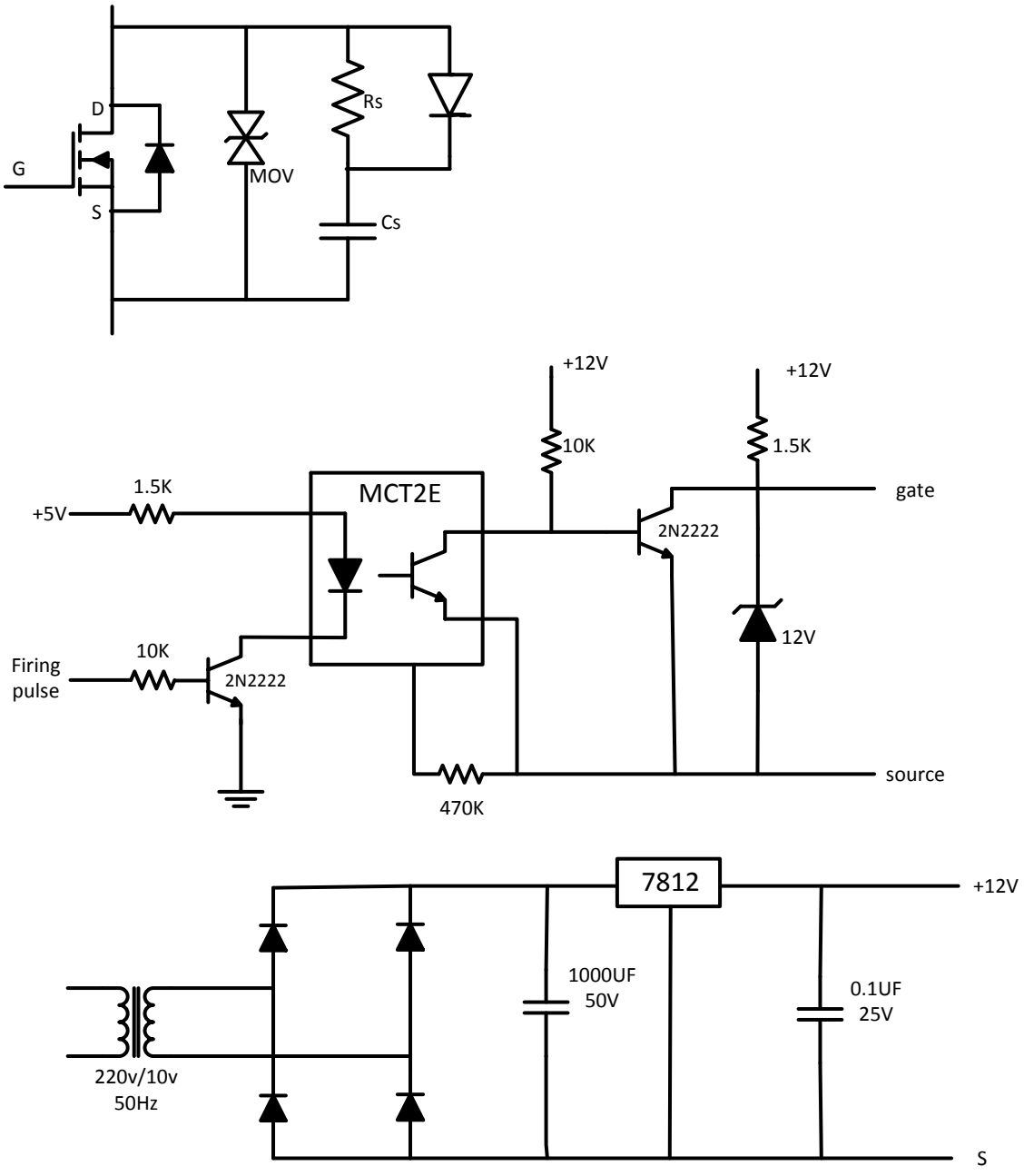


Fig. 4.2 Snubber, driver circuit and power supply for mosfet switch.

4.3 CURRENT SENSOR

For control of shunt active power filter, filter current is needed to taken as control parameter. For sensing the current Hall Effect current sensors (HTP 25) are used. The circuit diagram of the Hall Effect current sensor along with a buffer and a scalar circuit is shown in Fig 4.3. Here

a current of I (A) in power network is converted into ± 5V range. These current sensors provide galvanic isolation between high voltage power circuit and the low voltage control circuit and require a nominal supply voltage of the ±12V to ±15V. For a chosen primary turns (N_P), the conversion ratio (cr_i) of current sensor is 1000:1 and the output resistance of the current sensor is taken as 100 Ω. The voltage input to the buffer circuit is calculated by the equation $v_{0i} = R_0\left(\frac{N_p i}{cr_i}\right)$. Thus the voltage v_{0i} is scaled properly with the scalar circuit. The output voltage is given to the controller kit with the help of ADC.

Each Current sensor (TELCON) circuit

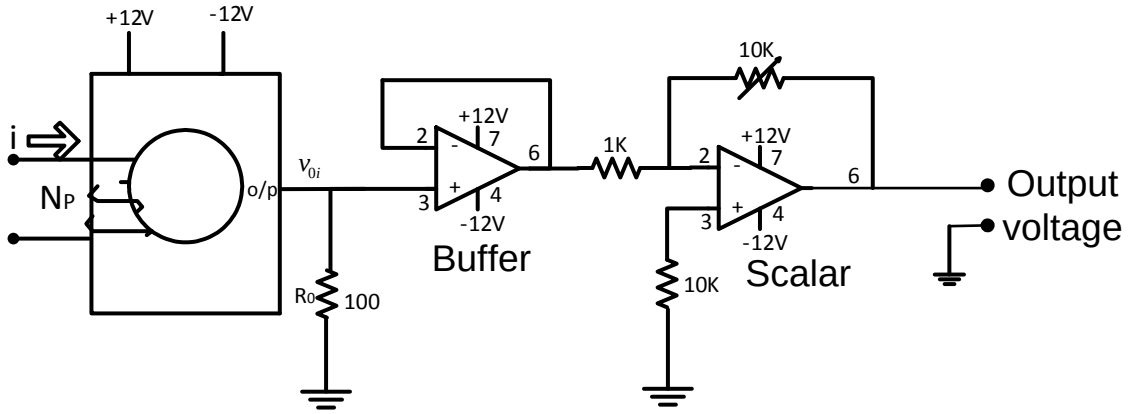


Fig 4.3 Current sensor circuit

4.4 VOLTAGE SENSOR

PCC voltages ea, eb and ec are given as the inputs to controller for generation of reference current. The DC capacitor voltages are also required to be sensed for maintain the DC voltage constant. Only sensing two phase voltages are sufficient for three phase three wire system. The circuit diagram of the sensing voltage along with the buffer and scalar circuit is shown in the figure 4.4 The AD202JN is an isolation amplifier in the present experimental setup the power circuit voltage which is in the range of ±500 V is converted into ±5V range. The voltage at the output of the isolation amplifier is $v_{ov} = v_1\left(\frac{R_2}{R_1 + R_2}\right)$. Thus the output voltage v_{ov} is properly scaled by a scalar circuit and the output voltage is given to the ADC of DSP kit.

Each voltage sensor circuit

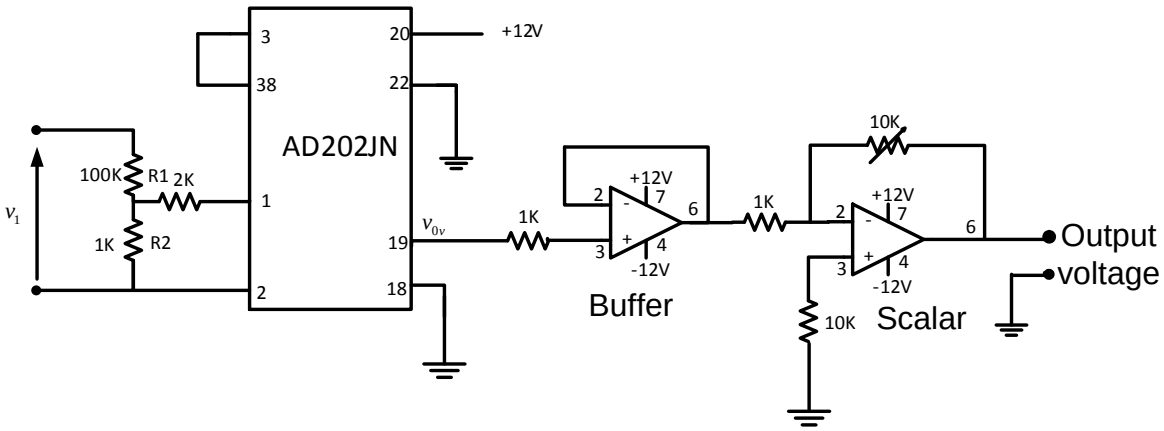


Fig 4.4 Voltage sensing circuit

4.5 Dead band circuit

There should be a delay between turning off of upper half and turning on of below half of a single leg of inverter. Otherwise short circuit will happen in that phase. To prevent this dead band circuit is used.

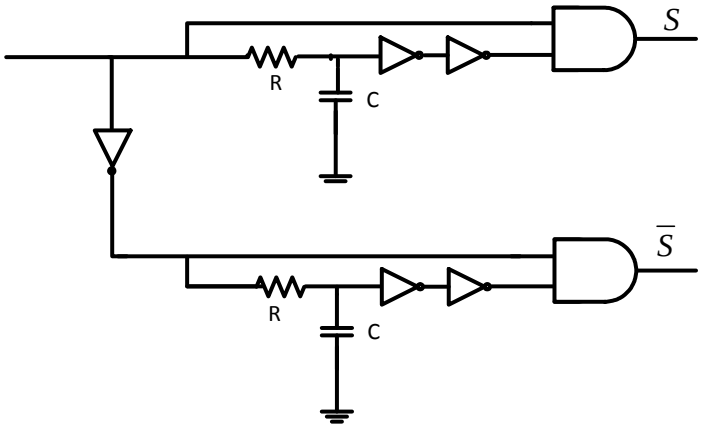
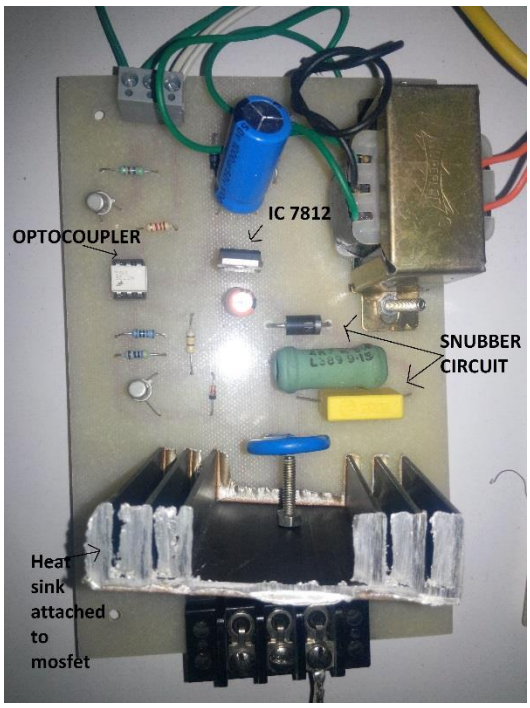


Fig. 4.5 Dead band circuit

4.6 DSP control block

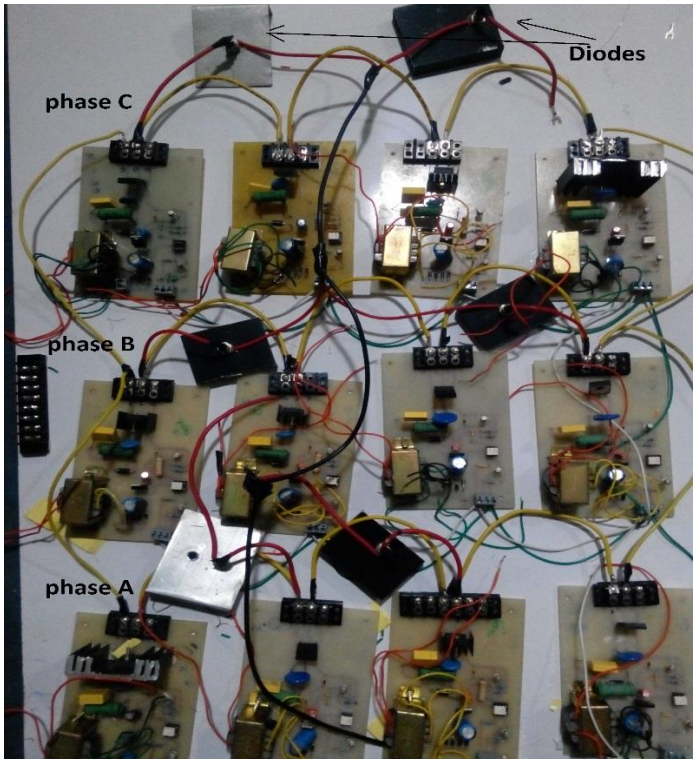
DSP is powerful machine for generating pulses for 3-level inverter. The code can be written in C/C++ language in code composer studio on a PC and the processor can be interacted through an emulator.

4.7 Photographs of hardware prototype



(a)

(b)



(c)

Fig.4.6 (a) Driver circuit for MOSFET switch (b) Power supplies(+12V,-12V,+5V) (c) 3-L NPC, (d) Voltage sensor

CHAPTER 5

5.1 Conclusion

Hysteresis controller, SVHCC and deadbeat controller for multilevel inverter based SAPF for a 3p3w system were simulated in this study. SAPF was able to filter out current harmonics and make the source current sinusoidal at unity power factor. Hysteresis controller is easy to implement but have very high average switching frequency compared to other controllers. SVHCC controller gives the best performance among the three controller as it provides optimal switching in all the three phases. It has the least switching frequency for same reduction in source current THD. Improved technique for inverter voltage state selection during steep changes in load, improves the performance in terms of THD. As the processing power is continuously increasing and most of the calculations are done digitally predictive controller can provide better performance. It gives better result than hysteresis controller. As number of levels of inverter increases more processing power is required. However predictive controller is suitable for digital implementation and further research on algorithm can improve the performance.

5.2 Future work

Better algorithm for predictive controller can be implemented. Current control techniques can be studied for 3p4w system under distorted supply conditions. Design of inductor and reference DC voltage can be further optimized for improvement of performance.

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