A

**DISSERTATION REPORT**

**ON**

# ALL DIGITAL PHASE LOCKED LOOP WITH SUPPLY NOISE SUPPRESSION

*Submitted in partial fulfilment of the requirement for the award of the degree*

*Of*

**MASTER OF TECHNOLOGY**

*In*

**ELECTRICAL ENGINEERING**

*(With the specialisation in SYSTEM AND CONTROL ENGINEERING)*


*Submitted by*

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**MAY-2016**

# CANDIDATE'S DECLARATION

I hereby certify that this report which is being presented in the dissertation seminar entitled **"ALL DIGITAL PHASE LOCKED LOOP WITH SUPPLY NOISE SUPPRESSION"** in partial fulfilment of the requirement of award of Degree of **Master of Technology** in **Electrical Engineering with specialization in SYSTEM AND CONTROL**, submitted to the Department of Electrical Engineering, Indian Institute of Technology, Roorkee , India, is an authentic record of the work carried out under the supervision of **Dr. RAJENDRA PRASAD**, Professor, Department of Electrical Engineering, Indian Institute of Technology, Roorkee. The matter presented in this seminar has not been submitted by me for the award of any other degree of this institute or any other institute.

Date : 24/05/2016

Place : Roorkee **(Vipin bairwan)**

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# CERTIFICATE

This is to certify that the above statement made by the candidate is correct to best of my knowledge.

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ABSTRACT

The purpose here is to design a Phase Locked Loop (PLL) because the design process is going to include topics from analog, digital, IC design, and control system theory. A phase locked loop (PLL) is a closed loop feedback control system that generates and outputs a signal in relation to the frequency and phase of an input reference signal. Phase locked loop is sensitive to both the frequency as well as phase of the input signal, automatically it has an ability to lead or lag the frequency of the feedback signal or reference signal in order to match the frequency and phase with minimum jitter.

This property of phase locked loop made it unique hence used in many applications such as computers, radio, telecommunications and other applications where synchronization between receive and transmitter is required or we have to receive a signal even in the presence of noise.

Here comparison between analog and digital phase locked loop is presented by comparing their lock time specifications then a digital phase locked loop is presented and implemented using VHDL that is very high speed integrated circuit hardware description language. Also to reduce the lock time and to make a phase locked loop suitable for high speed applications a proposed all digital phase locked loop is also presented.

# CHAPTER 1.1
# INTRODUCTION

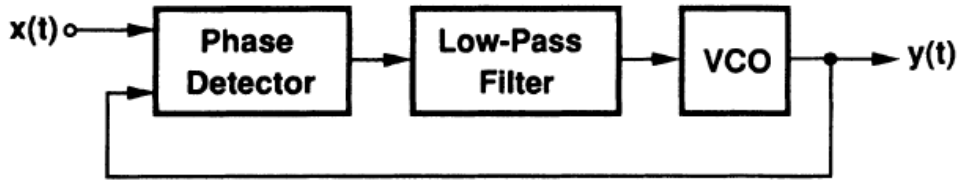
The application area of phase locked loop is wide such as communications, wireless systems, digital circuits and disk drive electronics. Since the concept of phase locking has been in use for more than 50 years, monolithic implementation of PLLs has become possible only in the last twenty years and widely used in the last ten years. The factors which arises this trend: the need for higher performance and cheaper rates in electronic systems, and the advancement of IC technologies in terms of speed and complexity.

The phase-locked loop (PLL) is a very important component widely used in various integrated circuit areas. In the modern era, phase-locked loops and delay-locked loops are used in system-on-chip (SOC) and microelectronics designs to fit clocking demand for their sub-systems and I/O devices. To ensure low power consumption of mobile products and also increase battery life, let these products go into deep sleep mode to save power.

## PHASE - LOCKED LOOP

A phase locked loop (PLL) is a closed loop feedback control system that produces a signal which matches the frequency and phase of an input ("reference") signal. A phase locked loop circuit reacts to both the frequency and the phase of the incoming signals, automatically increasing or decreasing the frequency of a controlled oscillator until the error gets reduced and it matched to the reference in both frequency and phase.

A phase-locked loop is a feedback system that operates on the additional phase of incoming periodic signals. This is in contrast to general feedback circuits in which current and voltage magnitudes and their rate of change are of importance. Shown in Figure a simple PLL, comprises of a phase detector, low-pass filter (LPF), and vco. The phase detector acts as an "error amplifier" in the feedback loop, and hence minimizes the phase difference between input and output. The loop have a "locked" state only when phase becomes constant with time, aa a result the input and output frequencies are becomes equal.




In the locked state, all the signals within the loop are in steady state and the PLL operates like this: The phase detector generates a signal whose dc value is analogous to phase. The low-pass filter quash all high-frequency content in the PD output, and passes the dc value to provide control to vco frequency. The vco then oscillates at a frequency which is same as input frequency and having a phase difference equal to phase. Thus, the LPF generates the correct control voltage for voltage controlled oscillator.

PROBLEM STATEMENT:- As we know all the communication systems, digital systems or wireless systems in which synchronization is very important between transmitter and receiver there is a need of a phase locked loop. During communication through different channels a signal experiences jitter a kind of noise added to it means at the receiver we are not getting a signal we wanted. Hence there is a need of such a circuit which can eliminate or reduce these problems. Also in this era we are using or working with very high speed devices, so demand of such a circuit increases we resolve the above problems as well as matches such a speed .

THESIS OBJECTIVE:- The objective here is to study such circuit which resolve the above problems. Phase locked loop is one which can reduce the above problems. So we are going to study Ana-log phase locked loop which are generally used or traditionally we are using them for so long. But they are not suitable for high speed digital integrated circuits so we move on to digital phase locked loops. Digital phase locked loops have reduced lock times and having higher acquisition ranges which are suitable for these high speed digital circuits. Finally we are presenting a proposed model which can reduce the lock time even further and also achieve smooth locking condition with reduced jitter or noise.

# CHAPTER 1.2

## LITERATURE REVIEW

A phase locked loop (PLL) is a closed loop feedback control system that produces a signal which matches the frequency and phase of an input ("reference") signal. A phase locked loop circuit reacts to both the frequency and the phase of the incoming signals, automatically increasing or decreasing the frequency of a controlled oscillator until the error gets reduced and it matched to the reference in both frequency and phase.

In the beginning of $19^{th}$ century a scientist called Lord Rayleigh analyse a synchronisation between turning forks and organ pipes. After this a scientist called W.H.Eceles found in his research that two oscillators which have a slight difference in their frequencies and if they are coupled to resonating circuit after some time they starts oscillating at the same frequency. Finally this kind of phenomena which is now possible with the help of a circuit named as phase locked loop around 1932. Basically the invention of a phase locked loop is an alternative to the super-heterodyne receivers.

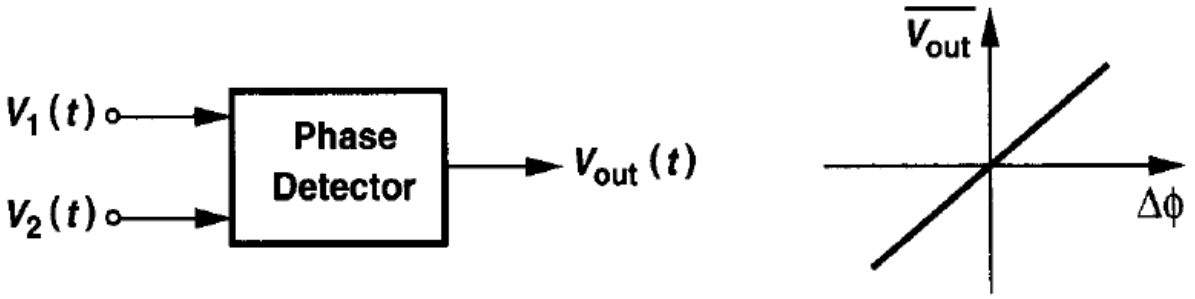
So as year passes many researches were going on and in 1950 a phase locked loop was able to tune or adjust the color of a television set with a second. And a slightly low grade phase locked loop can even adjust within 10 seconds. Basically phase locked loops were used to replace the control knob which requires a manually control. Phase locked loops after then finding applications in many areas for synchronizations, clock recovery and for jitter reduction etc.

The application areas include space communication also in digital systems for bit synchronization and in frequency or phase demodulation even it is one the techniques used for demodulation and generally used in all systems for synchronization purposes.

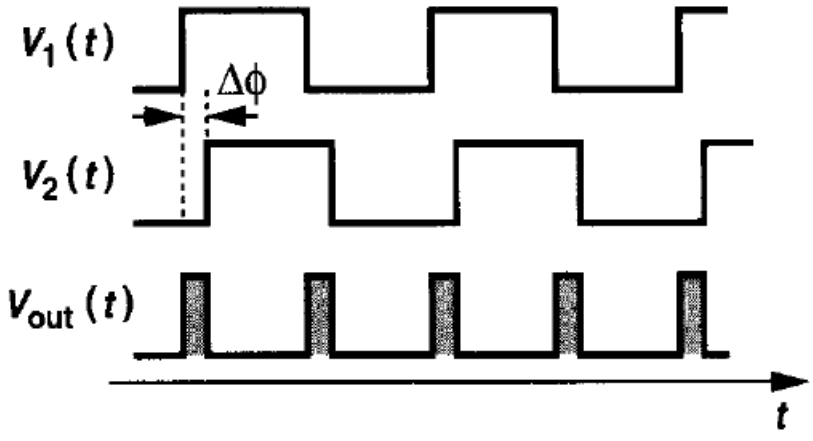
# CHAPTER 2

## PLL COMPONENTS:

1. **PHASE DETECTOR:** A voltage is generated by phase detector which gives the phase difference between input and the feedback signal. In a PLL, the two signals are the reference input and the signal coming from output of vco. And the output voltage of phase detector is used as to control the input of vco, so that the phase difference between two signals become constant, and the feedback is negative for the system.



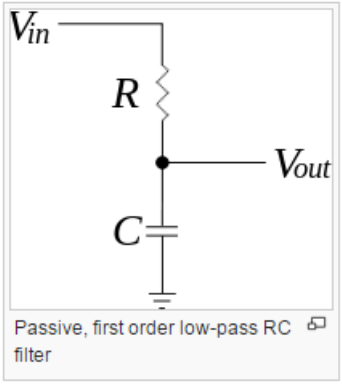

Phase difference is given by phase detector between two input signals which is actually proportional to dc level of the output. Phase detector works in a similar manner as differential amplifiers as they both gives the output based on difference between input signals by generating a proportional output.




1. LOW PASS FILTER: The purpose of a low pass filter is to pass the frequencies having values lesser than a certain frequency called cut-off frequency and rejects all the frequency above that .Filter design decides the amount of frequency to be attenuated. High-cut filter, or treble cut filter are the name given to low pass filter in audio applications. A high pass filter acts in contrast to low pass filter.

TYPES:

1) FIRST ORDER: A simple low -pass filter consist of a resistor and a capacitor in series and parallel with respect to load as shown below. Capacitive reactance is there which blocks the frequency content of the incoming signals, forcing them through the load . But at higher frequencies the reactance becomes very low and hence the capacitor acts as a short circuit. The combination of both gives the low pass filter. The time constant is responsible for knowing the cut-off frequency of a filter:-



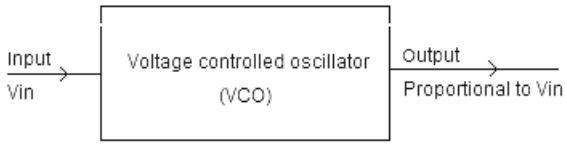
Passive, first order low-pass RC filter

$$f_c = \frac{1}{2\pi\tau} = \frac{1}{2\pi RC}$$

equivalently (in radians per second):

$$\omega_c = \frac{1}{\tau} = \frac{1}{RC}$$

2. Voltage controlled oscillator: Voltage controlled oscillator is a oscillator in which the output signal which is frequency depends on the input voltage of the oscillator. Voltage controlled oscillators are commonly used in pulse modulator frequency modulator and in phase locked loops . Also the voltage controlled oscillator can be used as a variable frequency oscillator which is control by input voltage.




The two types of voltage controlled oscillator which are generally used are linear controlled voltage oscillator and relaxation type voltage oscillator. Linear voltage controlled oscillators are generally produces the sinusoidal oscillations. In such circuits generally a tank circuit is used to produce sinusoidal oscillations which consist of inductors and capacitors. And a transistor is used as an amplifier for amplifying the output of a tank circuit, and also compensate the energy lost in the circuit and for establishes the necessary conditions.

Sometimes a varactor diode is used instead of a capacitor in the tank circuit. A varactor diode is a semiconductor p-n diode in which junction capacitance can be varied by varying the voltage across the junction. So varying the voltage across the varicap the output of the oscillator which is frequency can be varied accordingly.

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# CHAPTER 3

## WHY PHASE LOCKED LOOP:

The application area of phase locked loop is wide and of great importance which gives elegant results whenever used. In this section, we are considering four problem areas where phase locked loops are required and provide good results.

1) Jitter reduction: Signals generally goes through a periodic variation while passing through communication channel or during reception through a medium. Depicted in Figure 1, jitter signifies a variation in the period of any wave, it is a type of problem which cannot be resolve even after amplifying or by other means.
   A PLL can be used to reduce the jitter present in the waveform .

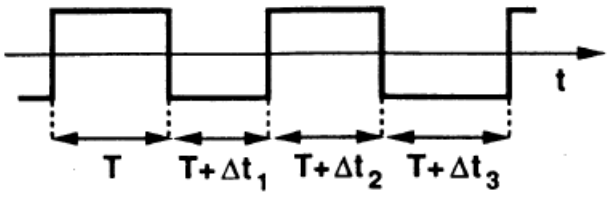



Fig. 1 Timing jitter.

2) SKEW SUPPRESION: Figure 2 illustrates a crucial problem in high-speed digital circuits. whenever, a system clock( C*Ks)* applied to a chip from a printed-circuit (PC) board and is buffered in several stages to sharpen its edges and drive the load with minimum delay. The main problem in this kind of arrangement is that the clock ( on-chip), typically able to drive several nano farads in the device and interconnect capacitance, and exhibits reasonable delay with respect to on-chip clock . The resulting skews lowers the timing budget for inter-chip and on-chip operations. Phase locked loops are used in order to reduce this kind of problem, thereby aligning *system clock with on chip clock.*

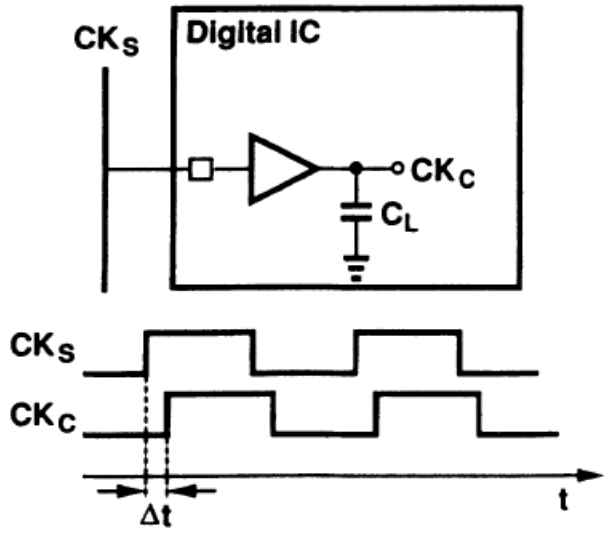



Fig. 2 Clock skew in a digital system.

3) FREQUENCY SYNTHESIS: Some applications needs higher frequency , so multiplication of periodic signal is required. For example, in the digital circuit the bandwidth limitations of printed circuit boards constrains the frequency of system clock, but the on-chip clock frequency must be much higher. As another example, in a wireless transceivers a local oscillator in which output frequency must be increase in small accurate steps for example, from 1000 MHz to1025 MHz in steps of 200 kHz. This simplifies the problem of frequency synthesis and it is possible only due to phase locked loops.

4) CLOCK RECOVERY: In some systems data transmission or reception is done without any timing matching conditions. For example in optical fiber communication without a clock a stream of data flows through the channel, but at the receiving end data should be taken in sequence. Thus, at the receiving end a clock recovery is required so to get these data in sequence. In these circuits phase locking is required.

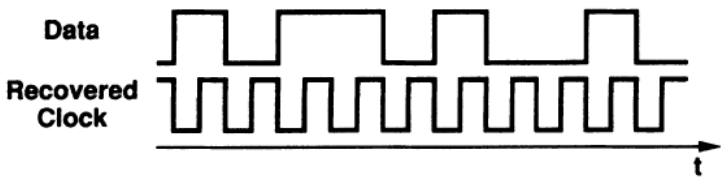


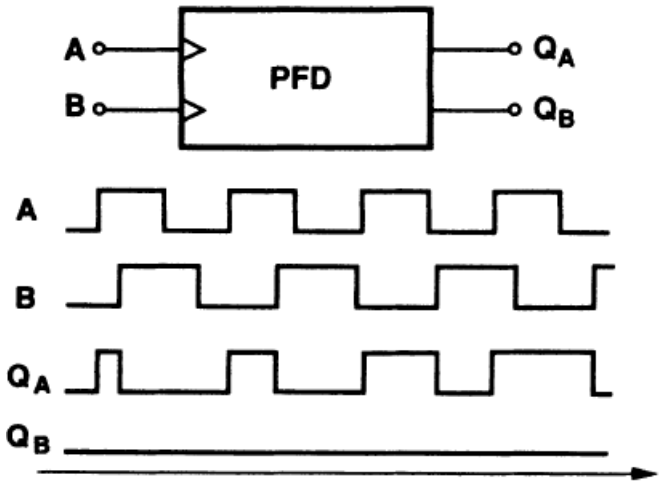

Fig. 3 Clock recovery from random data.

# CHAPTER 4

DIGITAL PHASE LOCKED LOOP: The phase locked loop (PLL) is a highly important part of high performance/speed microprocessors. Traditionally PLL is an analog device consisting of analog components, but integration of an analog device on a digital integrated chip is highly complex. Analog PLLs also can be easily influenced by noise and variation in process. On the other hand digital PLLs have reduced lock times and are not easily influenced by noise, also very attractive for generating clocks in microprocessor systems.

## D-PLL COMPONENTS:

I. PHASE/FREQUENCY DETECTOR: It is very important component of a PLL as it is able to detect both phase and frequency of input signals and also the lock time and acquisition range very much depends on it. Phase /frequency detector generates two outputs which are not complimentary to each other which is different from xor gate and s-r latches. Illustrated in Figure 42 how the output of PFD looks like. If the input frequency of *A( WA)* is lesser as compared to input frequency of *B( WB)* then the output of PFD has a pulse at QA, while *zero at the output of QB*. Similarly, if *WA > WB*, the positive pulse appears at the output of *QB* and *QA* is at zero level. If *WA = WB*, then PFD produces the pulses at the output of QA or QB which is equal to the phase difference between the input waves. Note that in principle *both the output should not be high at the same time*. Thus, the value at the output of either QA or QB, indicates the difference in frequency or phase at the input A and *B.* The outputs *are indicated by UP and DOWN signals usually.*




The behavior of above circuit can be explained by assuming three logic conditions on the outputs: *QA* = *QB* = 0; *QA* =0, *QB* = 1; and *QA* = 1, *QB* = O. The above circuit should not depend on the duty cycle of the input that's why it is necessary to consider an edge triggered system. Here the circuit changes state on the rising edge of *A* and *B*, and, now we are not going to use the word rising it is understood. We can show the operation of PFD using a state diagram. In the ground state, *QB* =0, *QA* = 0, when there is a transition on A the state becomes I, where *QB* = 0, *QA* = O. The state remains the same until again a transition occurs.

II. CHARGE PUMP AND LOW PASS FILTER: The average value of the PD output is obtained by depositing charge onto a capacitor during each phase comparison and allowing the charge to decay afterwards. In a charge pump on the other side the decay of charge is negligible between phase comparison instants, resulting in different consequence. The charge pump contains the two switched current source which pumps charges in the loop filter as per the PFD outputs. When two waves compared at the PFD input and reference one is leading the output of the PFD generates an up signal. This will turns the UP switch on, which causes this to pumps the current in the loop filter, and hence increasing the control voltage. On the other hand when the feedback signal is leading as compared to the reference signal, then PFD generates a down signal. This down signal which is the output from PFD which activates the down switch, and the CP will sinks the current instead of pumping out of the loop filter thus decreases the control voltage. So the currents from both the switches should be equal in order to eliminate any mismatch or error in the

output. And the charge pump current is limited by or depends upon the switching speed specifications.

III. VOLTAGE CONTROLLED OSCILLATOR:- A voltage controlled oscillator ( VCO ) is designed as an electronic oscillator whose output frequency is controlled by the input voltage at the input of VCO. It generates the train of digital pulse whose frequency is totally depends on the voltage at the output of low pass filter.

# CHAPTER 5

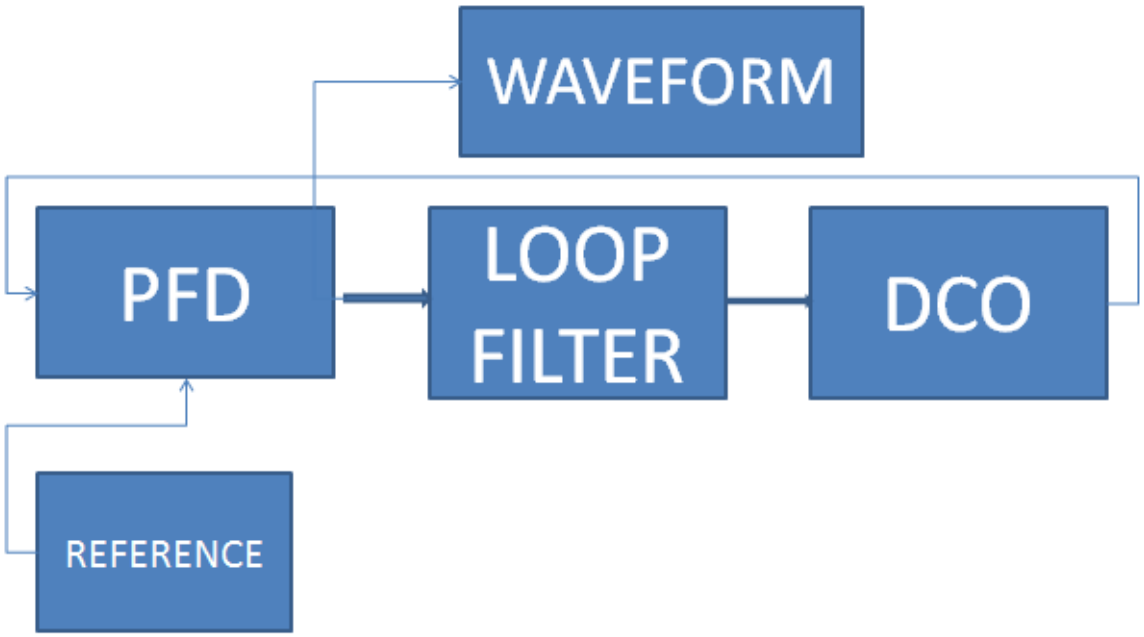
## DIGITAL PHASE LOCKED LOOP USING VHDL FOR HARDWARE IMPLEMENTATION:

VHDL is a term used for VHSIC (very high speed integrated circuits) hardware description language. In this the program describes the structure of the given circuit and through this code a physical hardware can be implemented. The main application basically involves synthesis of digital systems on FPGA (Field Programmable Gate Array) chip.

VHDL includes circuit simulations and synthesis both. Synthesis is basically translating the source code into hardware which performs the specific functionality, while circuit simulation is a testing procedure for confirming the specific functionality.

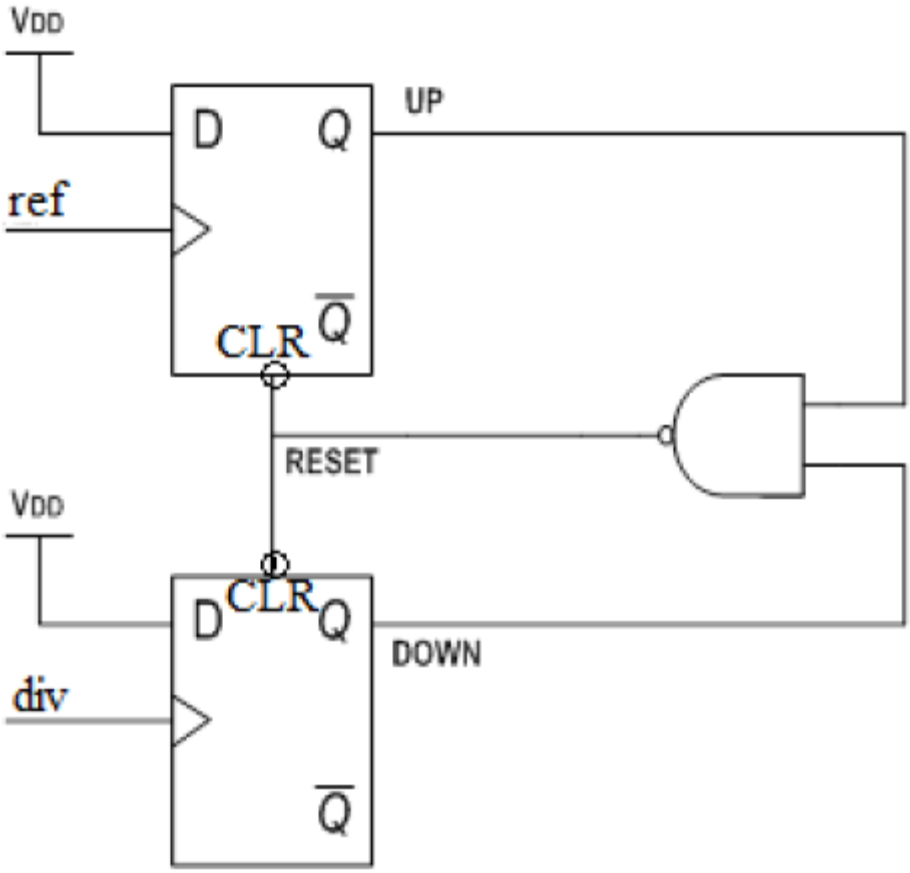
Most of the circuits having problem of clock skew and also flip flops and other components does not receiving the timing information properly. Generally oscillators are used to produce the clocks, but the timing information given by the clock gets distorted and hence requires a phase locked loop. So a phase locked loop make sure that clocks which are given as input to various flip flops or digital circuits must match with the frequency that is produced by a local oscillator. The phase locked loop (PLL) is very common and important part of a high speed performance microprocessor. Generally, a PLL is an analog device block which includes all analog components, but to embed an analog device in digital IC is very difficult. Also analog devices have less noise tolerance ability as compared to digital one. Digital PLLs also have faster or reduced locked time as compared to analog hence very attractive in high performance digital systems as microprocessor.

Now presenting an All-digital phase locked loop which uses a digital oscillator that of accumulator type and it also provide good jitter control.



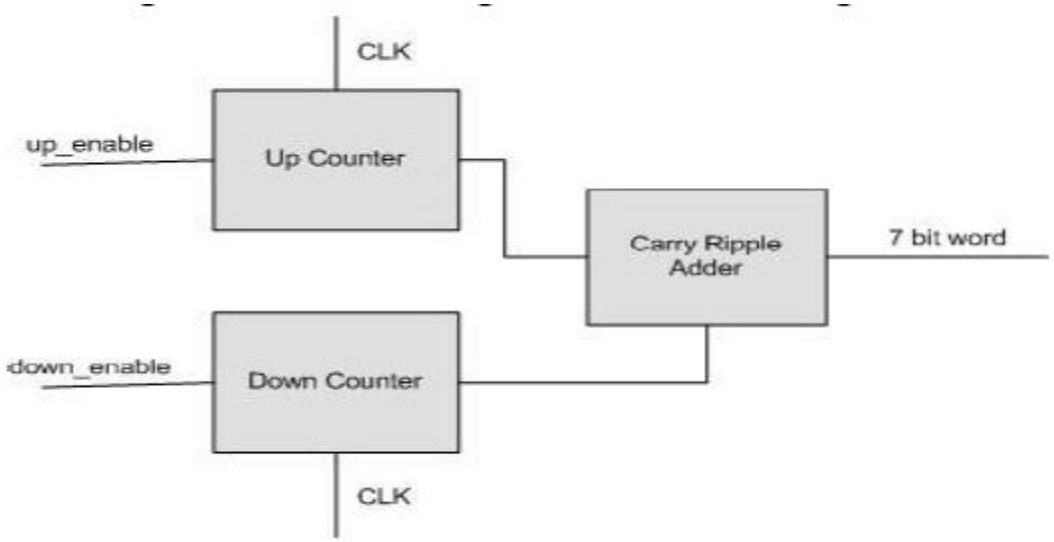

PHASE FREQUENCY DETECTOR :- One method is to use an ex-or gate for PFD it is simple and reliable also. But it has a very big drawback as it is not sensitive to edge's but to flat triggered only. So we have to eliminate this kind of drawback it is important. So the use of edge triggered flip flops are necessary here to make it simpler and also effective. Now it is edge triggered hence sensitive to edges. So the two inputs are applied to these d-flip flops one is the reference signal and other comes from DCO output as feedback. So this kind of circuit is used to make a PFD in our current design.
A logical extension is possible as we are using edge triggered mechanism to these simple d-flip flops hence clock can be eliminated as it is sensitive to edges only. So the reference signal and the other input coming from DCO can be considered as just binary values at the input. One reset input is also given to this PFD. The time for which the output of the circuit remains one is proportional to the phase error. The PFD consider both the phase and frequency of the incoming signal and then gives an output. So these kinds of phase frequency detectors are also known as sequential phase frequency detector. So at the input there is a comparison between the leading edges of both the inputs that is reference and DCO output.

The DCO output (div rising edge) cannot be there if is no reference input (ref rising edge).When the reference signal is leading as compared to feedback input then the output Up signal goes high and Down goes low .As a result the feedback signal frequency increases. When the reference signal is lagging behind the feedback signal the output Up goes low and Down goes high which causes the frequency of feedback signal to increase. Finally we got an output at the PFD as the phase difference between the two inputs. And the locked condition is achieved when we get both the low signal at the output of PFD. Then these two inputs are fed to the loop filter to get a constant value.




LOOP FILTER:-

Loop filter takes output from the phase frequency detector and acts as a low pass filter (analog pll). Loop filter is not present in all phase locked loops, but it is necessary as order of the system increases as in telecommunications, servo motors. The loop filter consists of a up counter, down counter and a carry ripple adder. The output of the phase frequency detector becomes the input clock for the up and the down counter. Initially the up counter having a state “111111” as it is a six bit counter and down counter having a state “000000” they both produces inputs for the carry ripple adder whose carry output becomes an input for a accumulator type digital controlled oscillator. So the six bits of sum and a carry make a 7 bit control word for the digital controlled oscillator. When there is a phase or frequency mismatch it plays a vital role. But when the locked condition is achieved clock gating is done so deactivate the effect of loop filter as we have reached the desire condition. As at the output there is a carry ripple adder so the output emerges at different times. So a change can also be detected. At the output a register can be used to store these outputs. These bits then shifted to the input of digital controlled oscillator depending on the input clock, which is made in such a way to match the timings of carry ripple adder. So in this way the output of loop filter reaches the digital controlled oscillator.



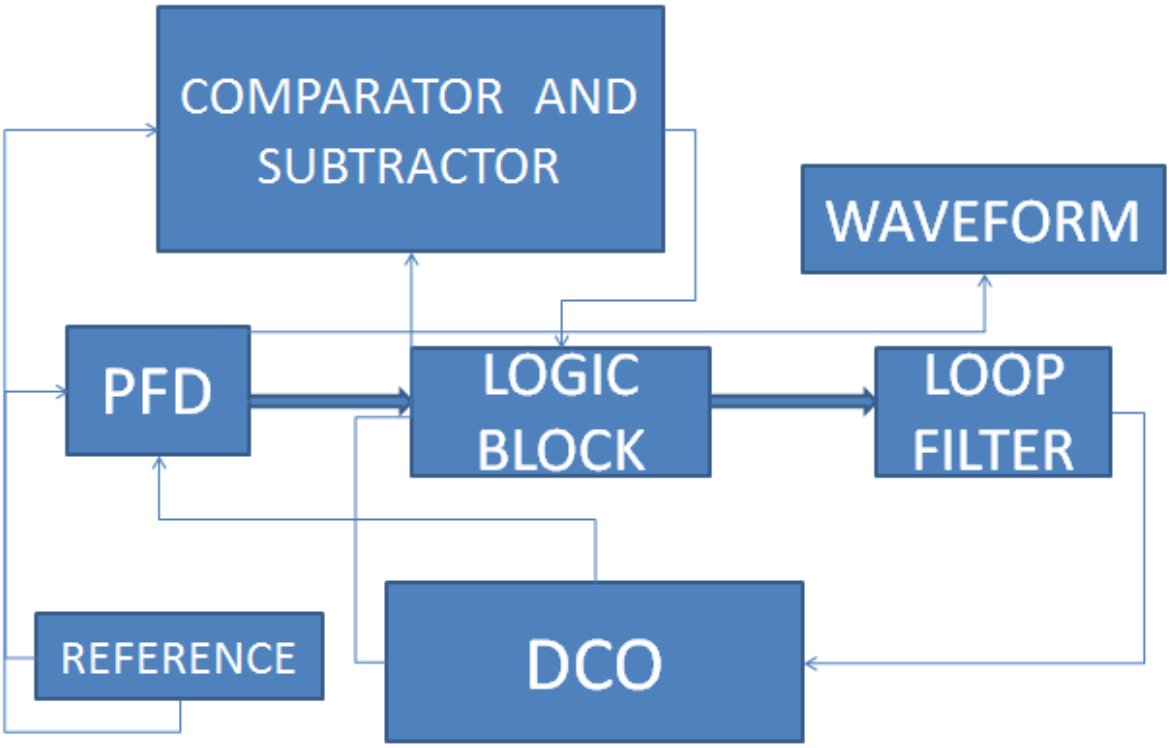

DIGITAL CONTROLLED OSCILLATOR:- The block diagram of DCO make use of toggle flip flops. It consist of a basic toggle flip flop and a logic circuit .Input is applied to it through the loop filters output .Here an accumulator type DCO is used which make use of carry bit from the carry adder and the clock input is also synchronize with other parts of the system.

Digital controlled oscillators output is very important as it is used as other input hence it totally depends on DCO output whether it is going lead or lag in phase as compared to the reference signal which is going to reflect at the output of phase frequency detector. As it make use of toggle flip flop it become very simple to design it in VHDL otherwise it is difficult to design any ring oscillator based DCO in which inverters are used. And increased jitter is also there.

# CHAPTER 6

PROPOSED MODEL FOR ALL DIGITAL PHASE LOCKED LOOP:- Most of the communication systems, transceivers uses phase locked loop as a synchronizing circuits. But for high speed systems conventional digital phase locked loops does not satisfy the given requirements. So some techniques are used as to meet the given requirements or to match up with high speed devices. In this we are varying the PLL bandwidth to satisfy the requirement or to reduce the lock time of a digital phase locked loop. So the technique is such that narrow bandwidth is used when it is in lock state and a wide bandwidth is used when it is not in lock state. This is only possible when we give an additional current to the conventional charge pump. Programmable charge pump is used to give this additional current, which depends on the relationship between the input and the output frequency across this charge pump hence as this difference decreases the current also decreases as to get a lock state without any jitter. Loop stability is also important which is given by conventional charge pump. This proposed model consists of additional components to achieve faster locking and smooth lock state additional component are discussed below.

OPERATION OF THE PROPOSED MODEL:- Proposed DPLL consist of difference circuit, Counter1, counter2, and the programmable CP these are the extra blocks for achieving fast locking or reduced lock time. Each counter produces a 3 bit code corresponding to input frequency in a given fixed period of time given by a time window signal. Then these 3 bit codes from each counter are fed to a sub-tractor circuit which produces a 3 bit code for logic block. The difference between the input and the output frequencies is represented by this 3 bit code which feds to the loop filter through a logic block acts a charge pump. The output of the sub-tractor produces bits b0,b1, b2 all are zero in the locked state and the charge pump acts as conventional charge pump. But when there is a change in the frequency that is reference frequency the output of the sub-tractor is no longer zero and the charge pump pumps the current corresponding to the frequency difference. As there is a decrease in frequency difference, the charge pump current also decreases and goes on decreasing until we have not reached a lock state.



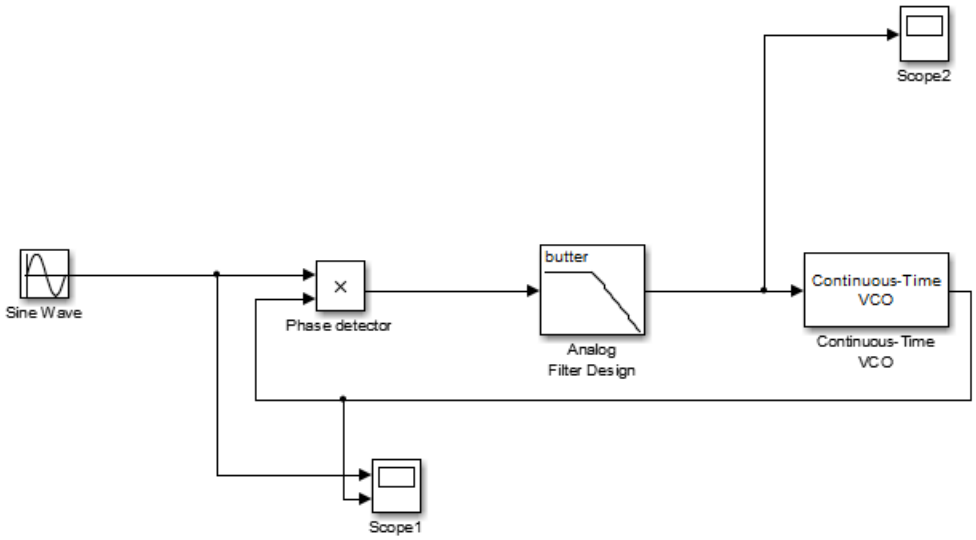

FREQUENCY COUNTER:- This stage is very crucial in this proposed model . In this a time window signal and a input frequency is applied to the input of and gate for counting the input pulses in a given time. The time period of time window signal is crucial as to cover a range of frequencies. Here a ring counter produces a seven bit code corresponding to the input frequency and then this code is being transformed into a 3 bit code using an encoder. Then the output of this encoder goes to 3 different edge triggered d-flip flops which produces a 3 different bits.

DIFFERENCE CIRCUIT:- This circuit performs simple subtraction of bits coming from the outputs of d-flip flops which is then applied to a logic block .The logic block combines the output from PFD and d-flip flops and then produces an output which goes to the input of loop filter.

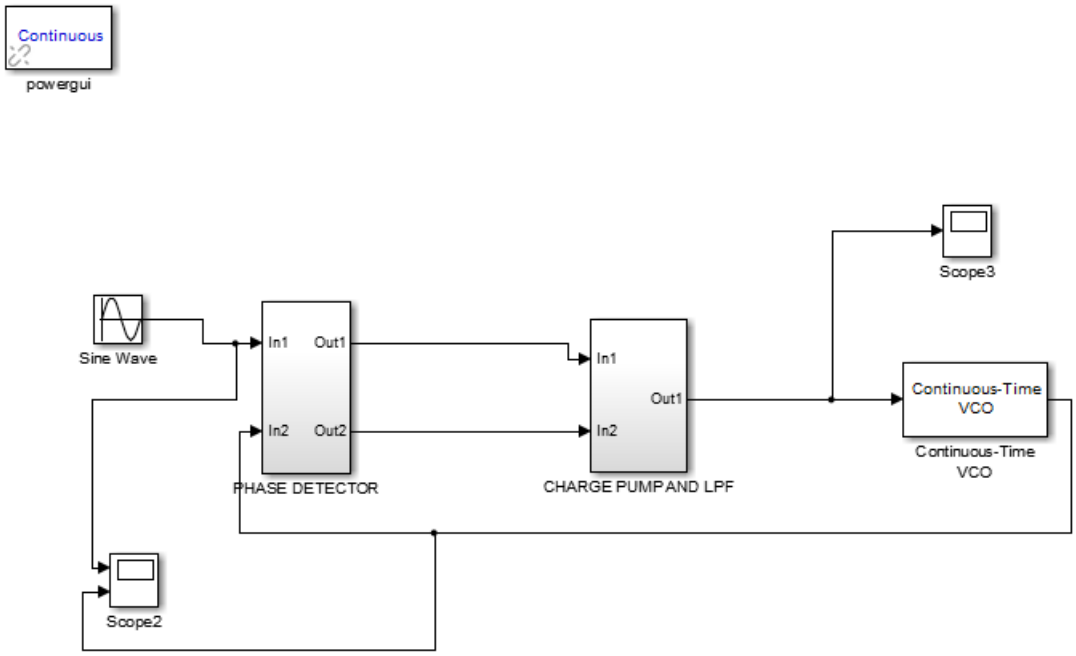
# CHAPTER 7

# MATLAB-SIMULINK MODELS

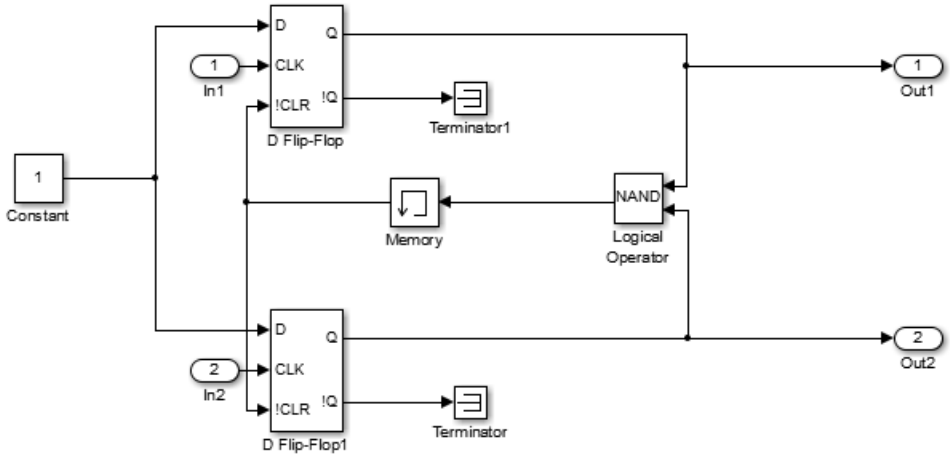
ANALOG PHASE LOCKED LOOP DESIGN:



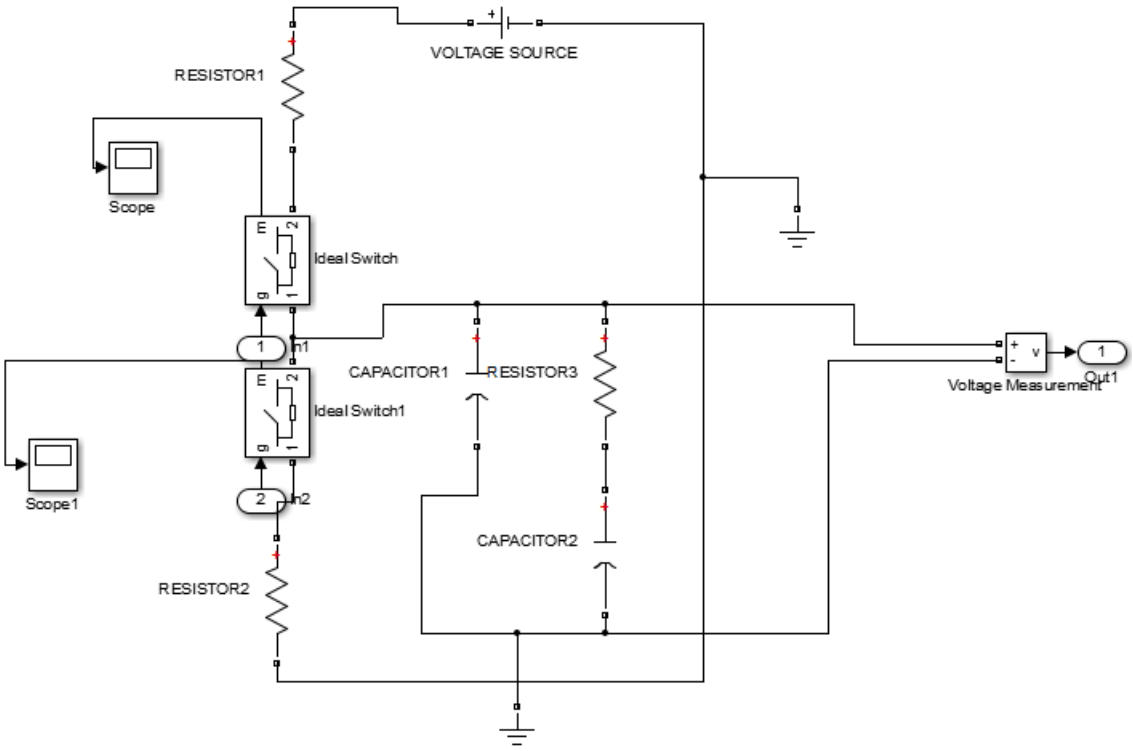
## DIGITAL PHASE LOCKED LOOP DESIGN:



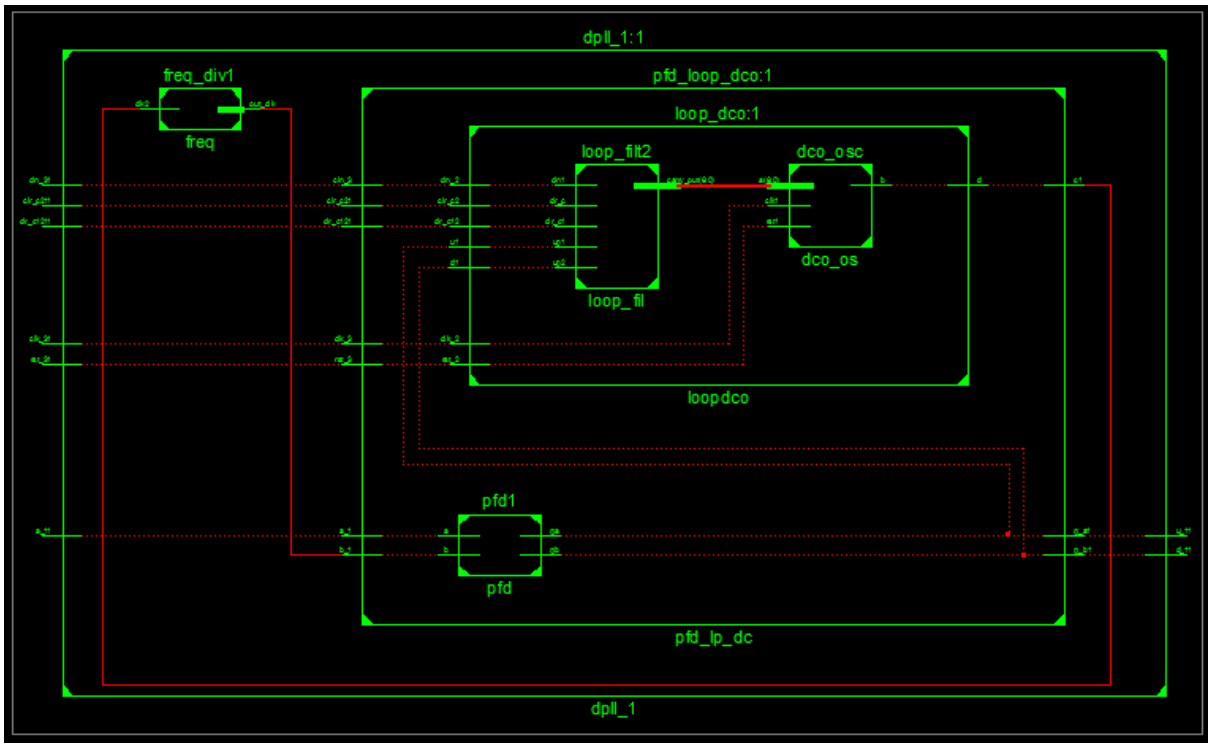

## PHASE DETECTOR CIRCUIT:



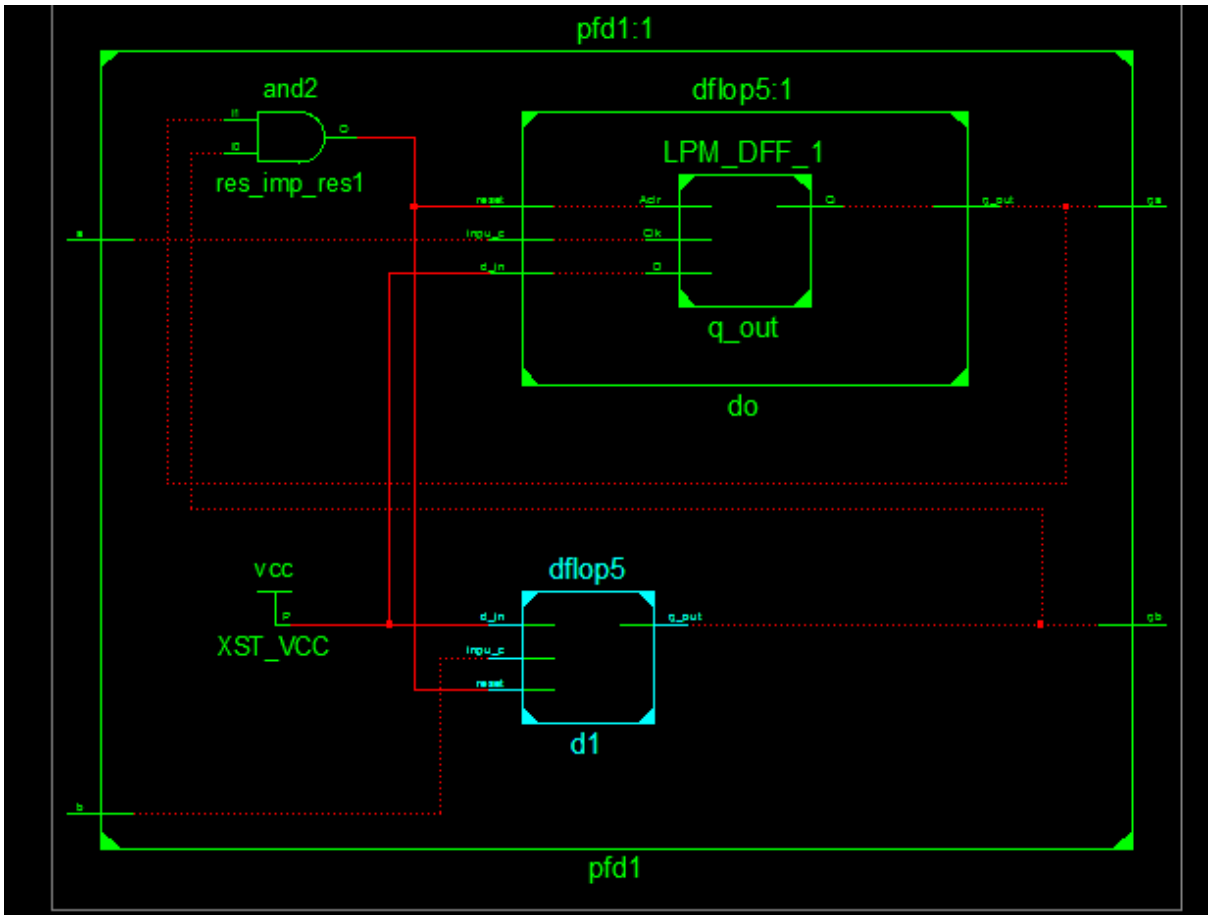
## CHARGE PUMP AND LPF:



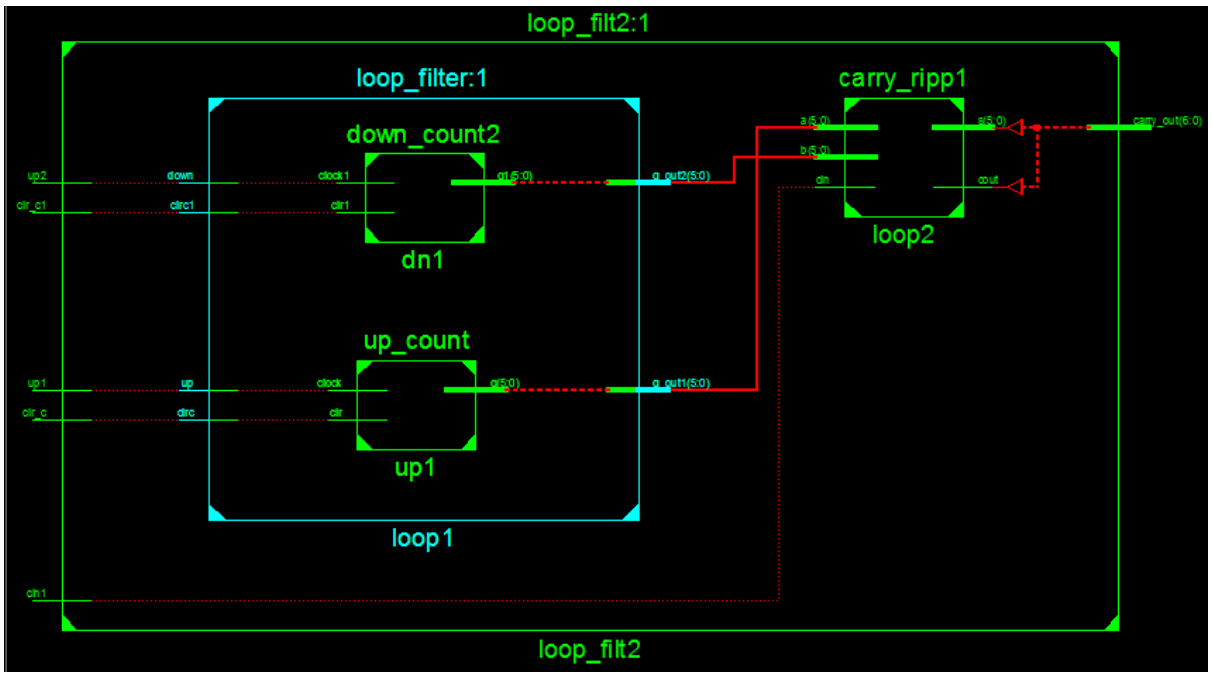
## ALL DIGITAL PHASE LOCKED LOOP VHDL DESIGN:-



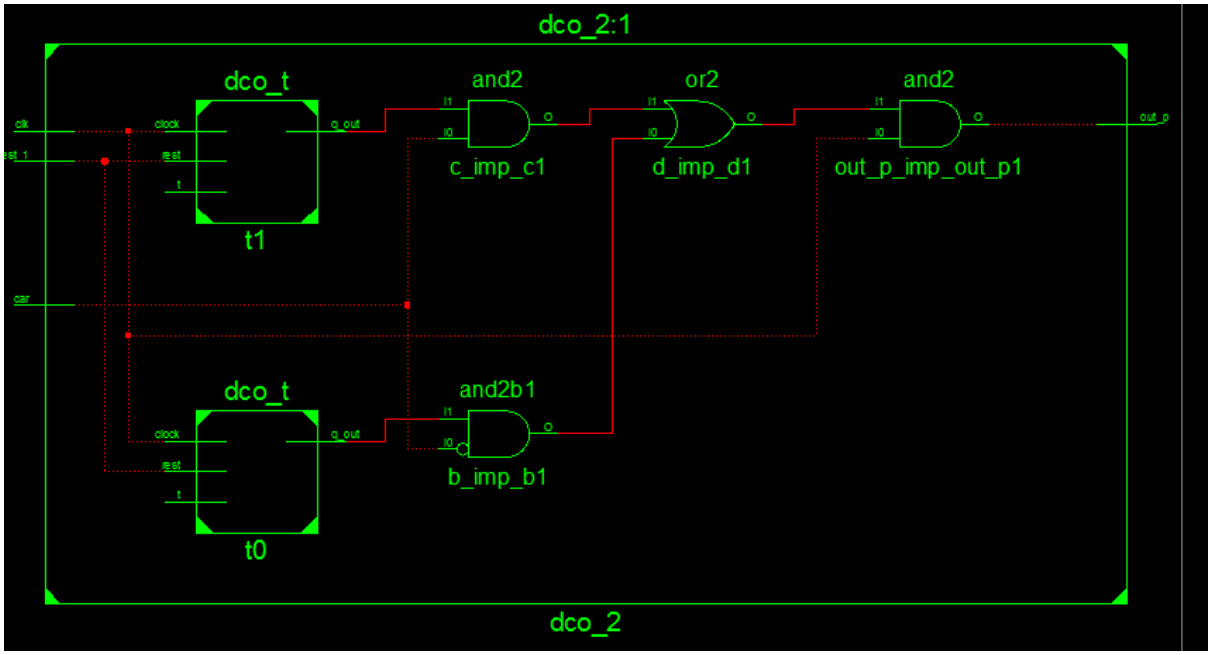
**PHASE DETECTOR:**



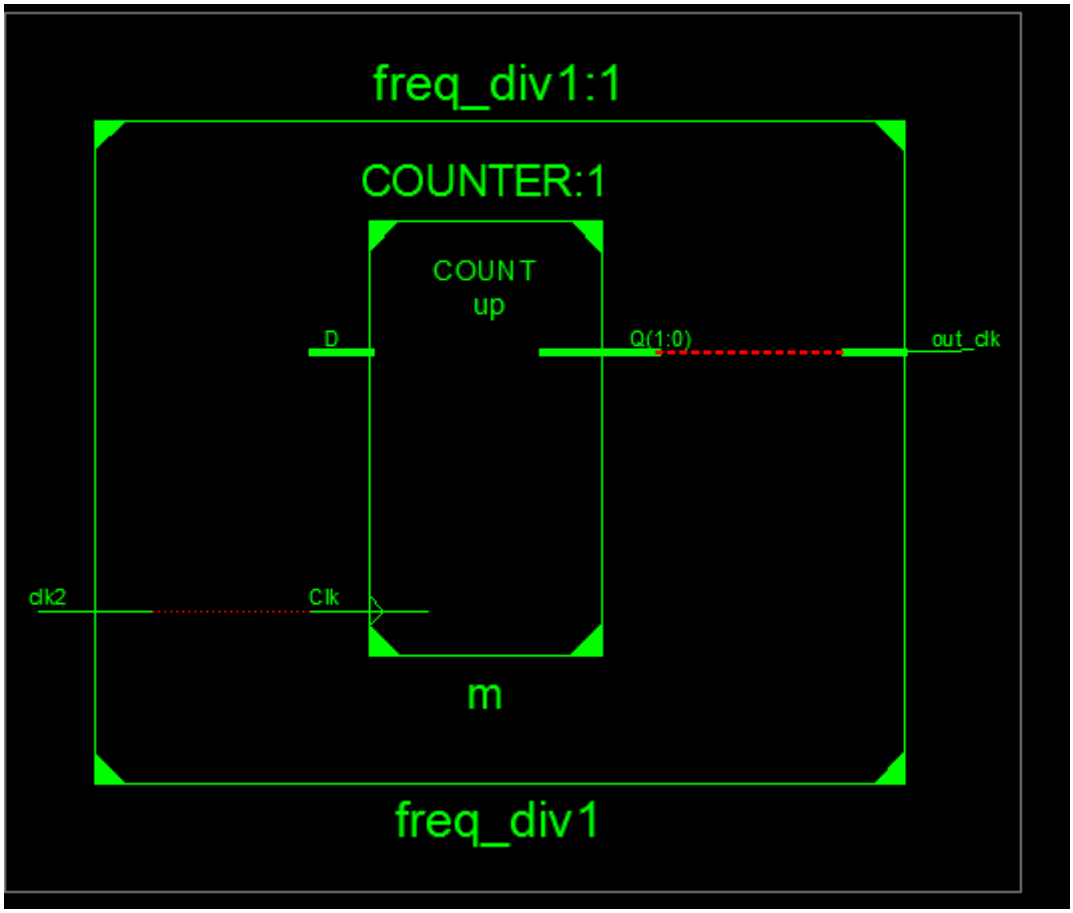
LOOP FILTER:-



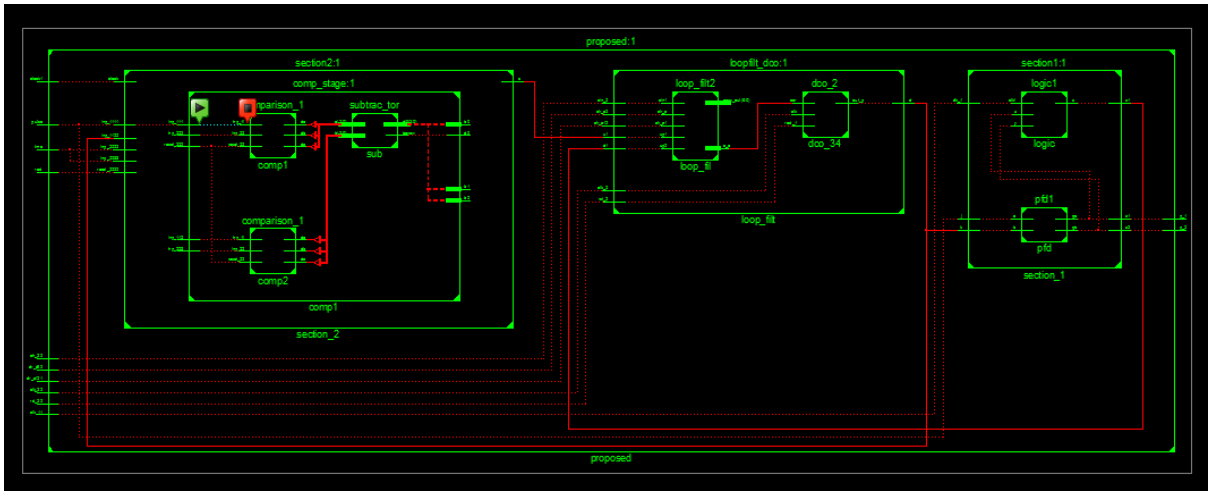

DIGITAL CONTROLLED OSCILLATOR:-



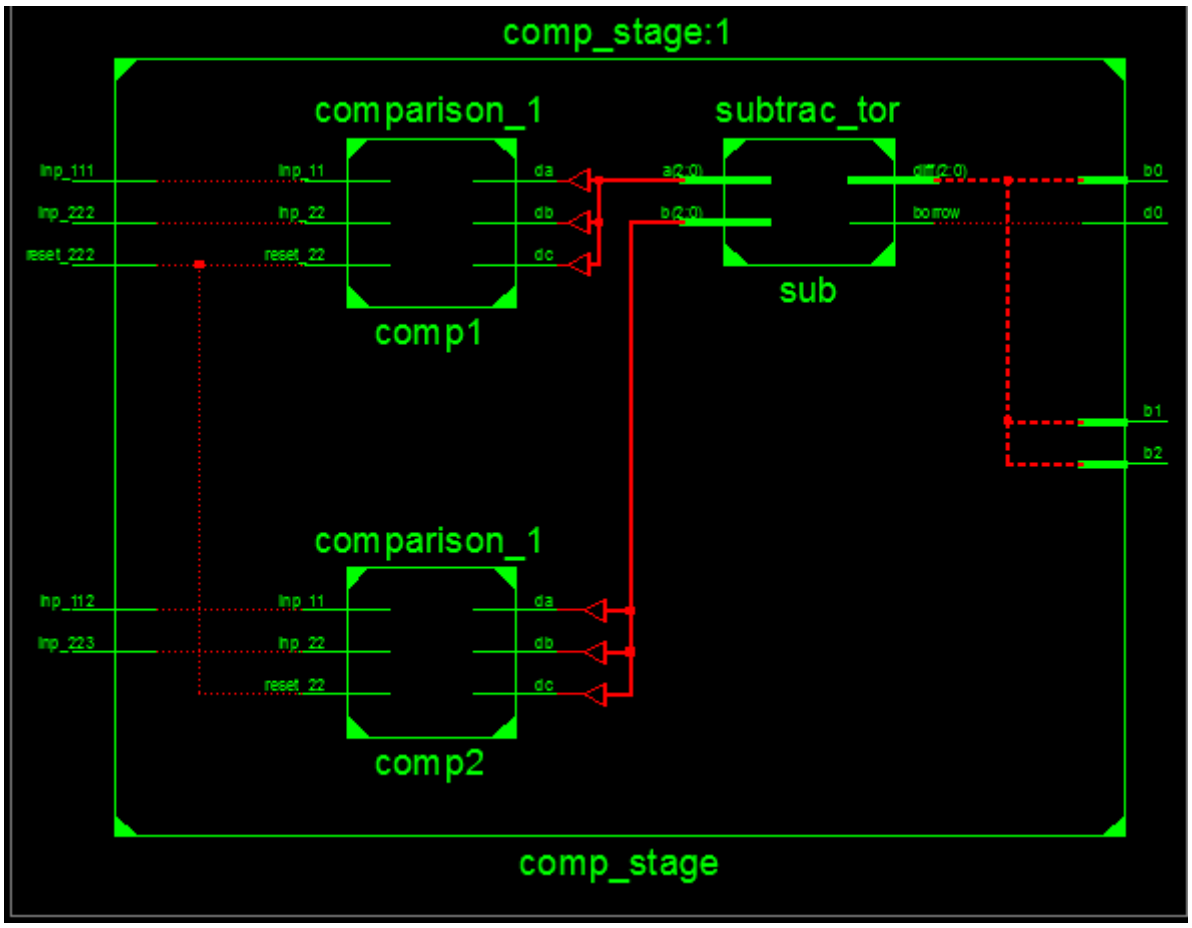
FREQUENCY DIVIDER:-



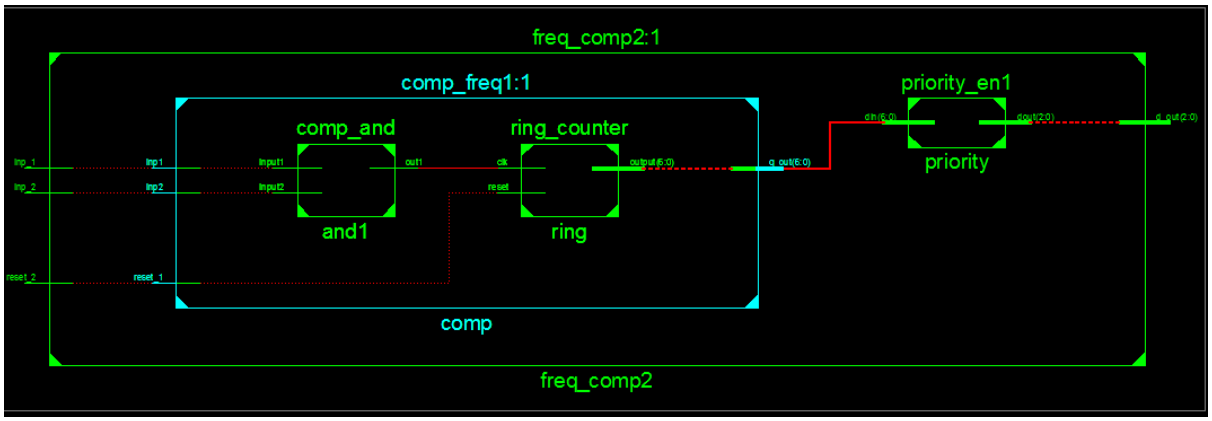

PROPOSED ALL DIGITAL PHASE LOCKED LOOP:-



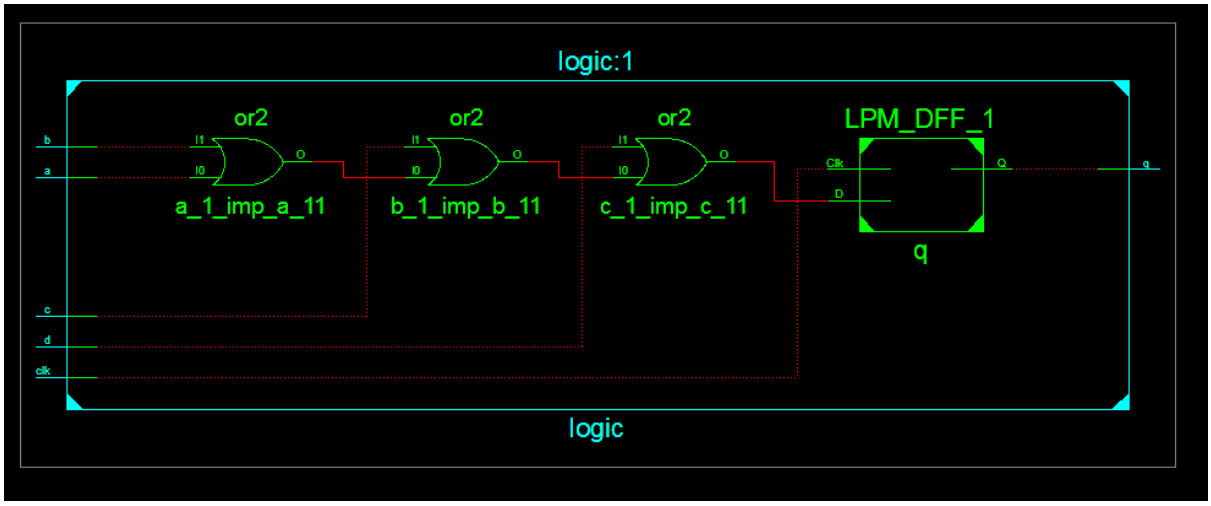
FREQUENCY COMPARISON STAGE:-

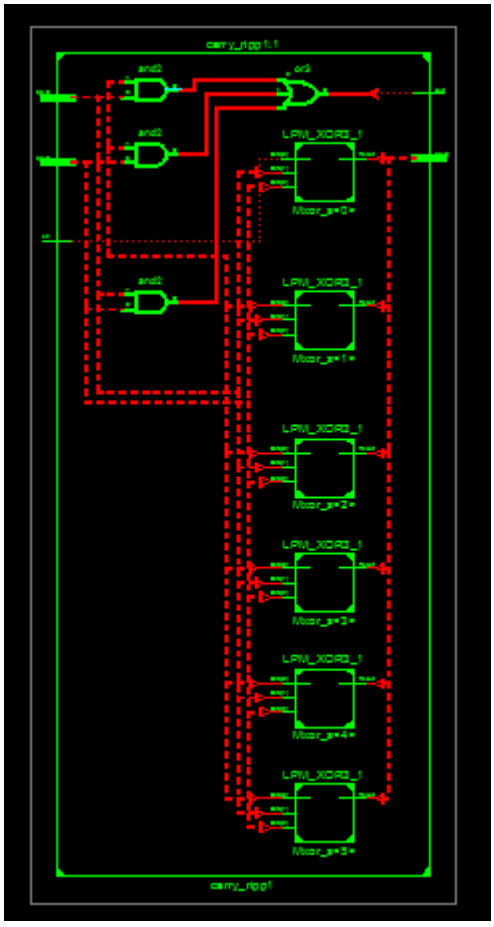



FREQUENCY COUNTER STAGE:-



LOGIC BLOCK AND RIPPLE ADDER OF LOOP FILTER:-



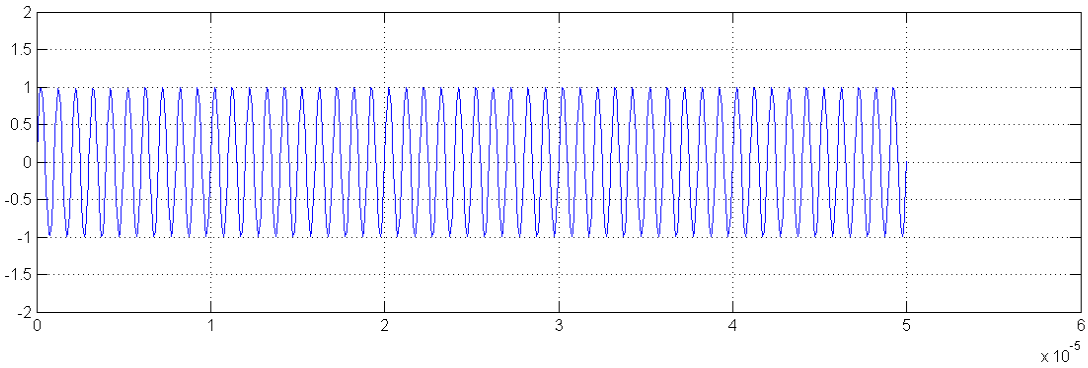



# CHAPTER 8

## SIMULINK RESULTS AND COMPARISON:

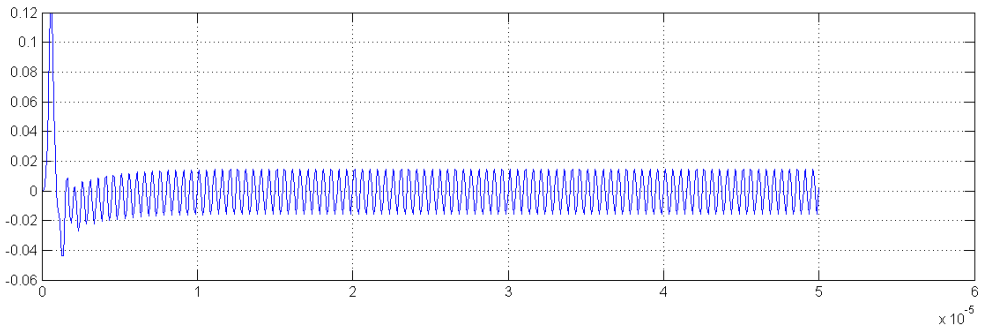
Analog phase locked loop behavior for 1Mhz input frequency:

a) Input signal: 1Mhz frequency



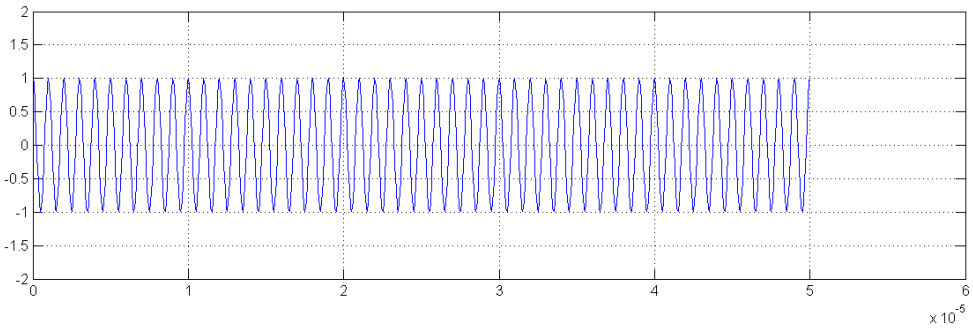

b) Input of voltage control oscillator:

This voltage vs time plot decides the lock time of pll i.e the taken by pll to lock the input frequency. Lock time is most important parameter of pll which decides the speed of a pll. A loop is said to be locked once the voltage reaches a point where it gets its steady state. All phase locked loops are differentiated on the basic of their lock times.

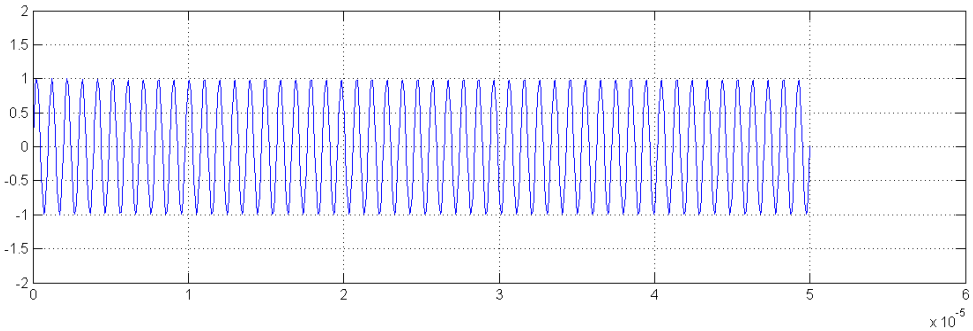



Voltage vs time

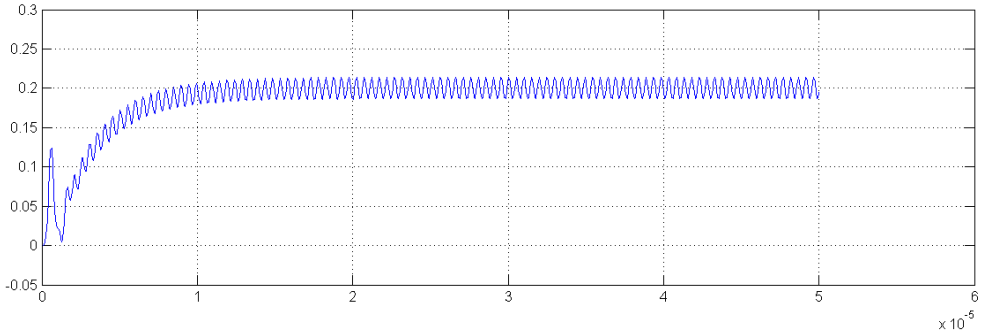
c) Output signal: for 1Mhz input



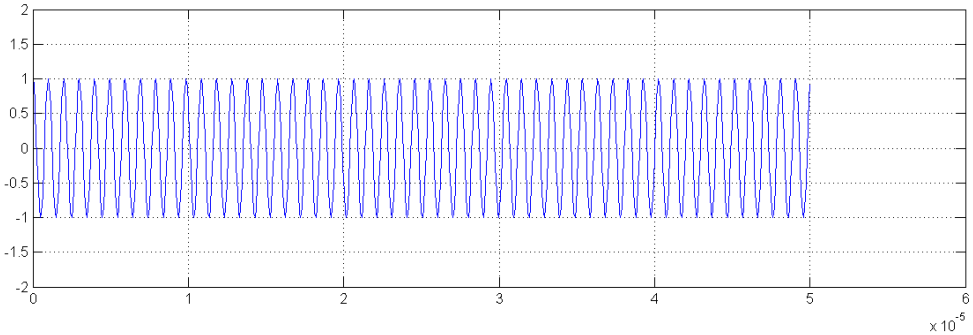

a) Input signal: 1.02 Mhz frequency



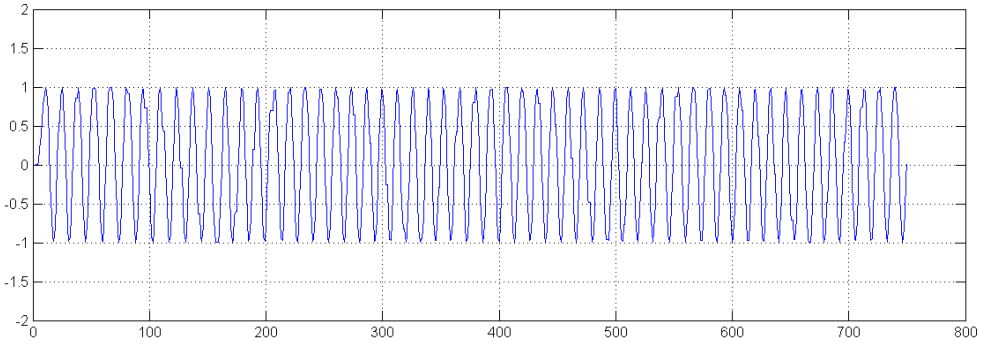

b) Input of voltage control oscillator:



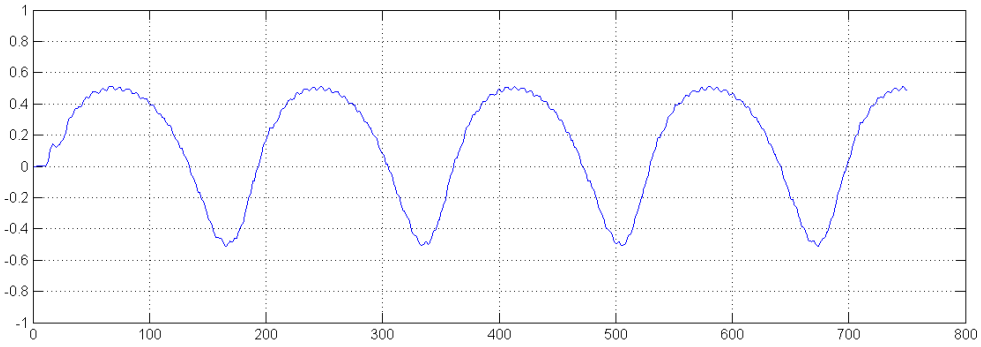

c) Output signal: for 1.02Mhz input




a) Input signal: 1.1Mhz frequency

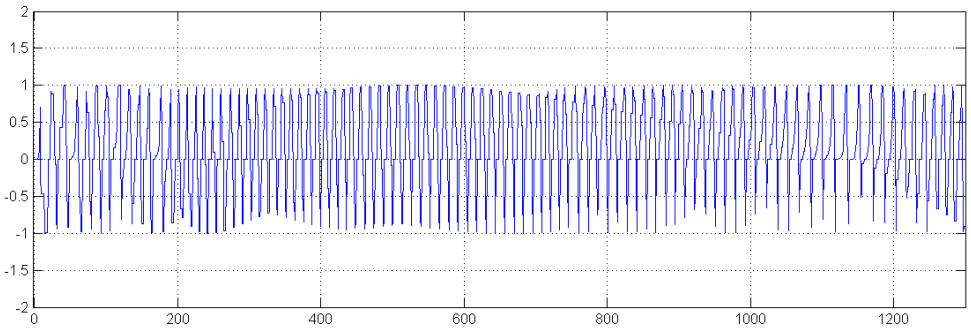



b) Input of voltage control oscillator: voltage vs time

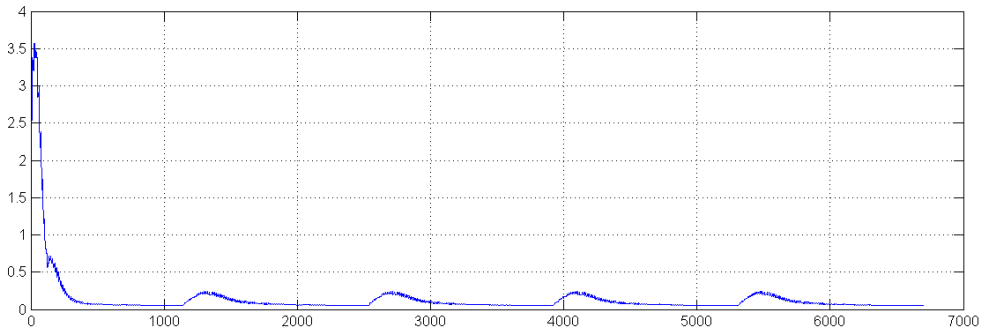



This can be seen that this analog pll is unable to lock 1.5Mhz frequency as voltage with respect to time is not settling anywhere hence this phase locked loop is not suitable beyond this frequency.

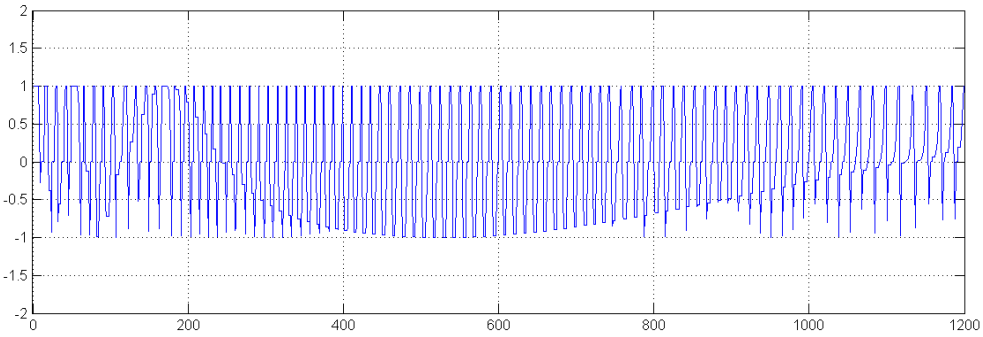
## DIGITAL PHASE LOCKED LOOP BEHAVIOUR FOR 1MHZ INPUT FREQUENCY:



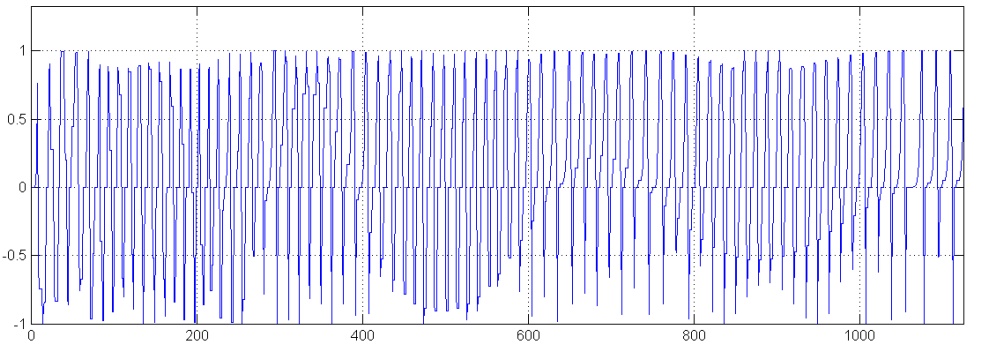

a) Input of voltage control oscillator: voltage vs time



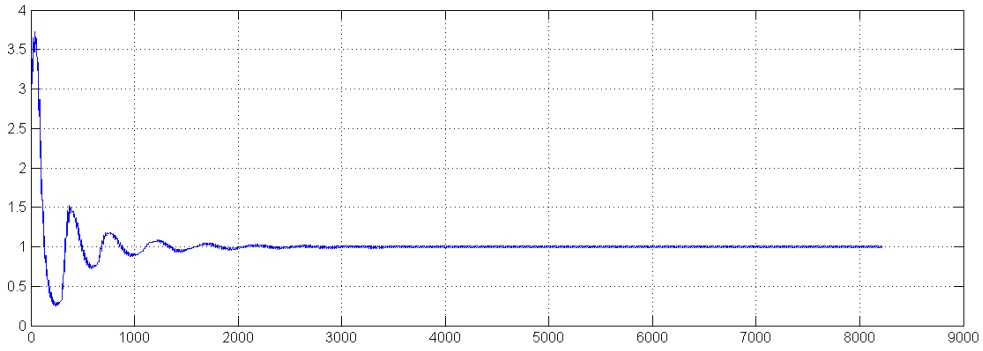

b) Output signal: for 1Mhz input




a) Input signal: 1.1 Mhz frequency



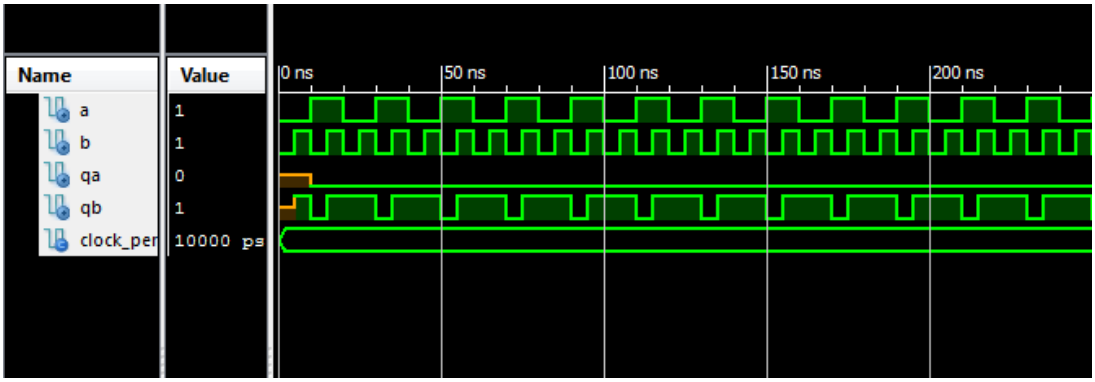

b) Input of voltage control oscillator: voltage vs time



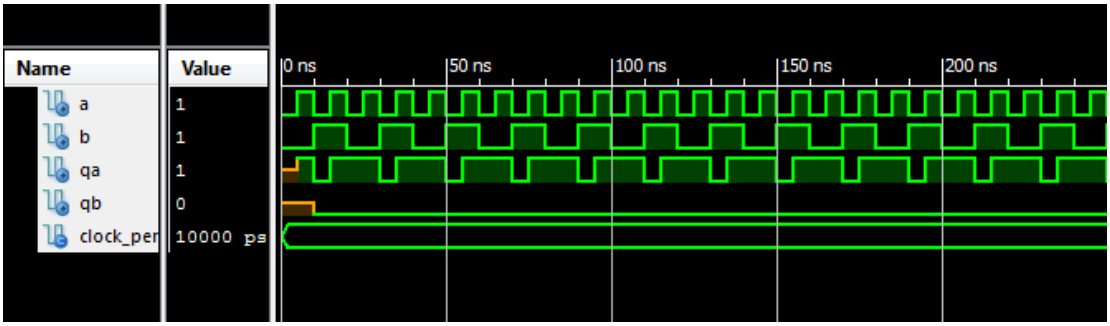

This shows voltage get settled even for 1.5Mhz frequency means this digital pll is able to lock this frequency. This shows the reason why digital pll are more useful then analog.

## SIMULATION RESULTS OF ALL DIGITAL PHASE LOCKED LOOP IN VHDL:-

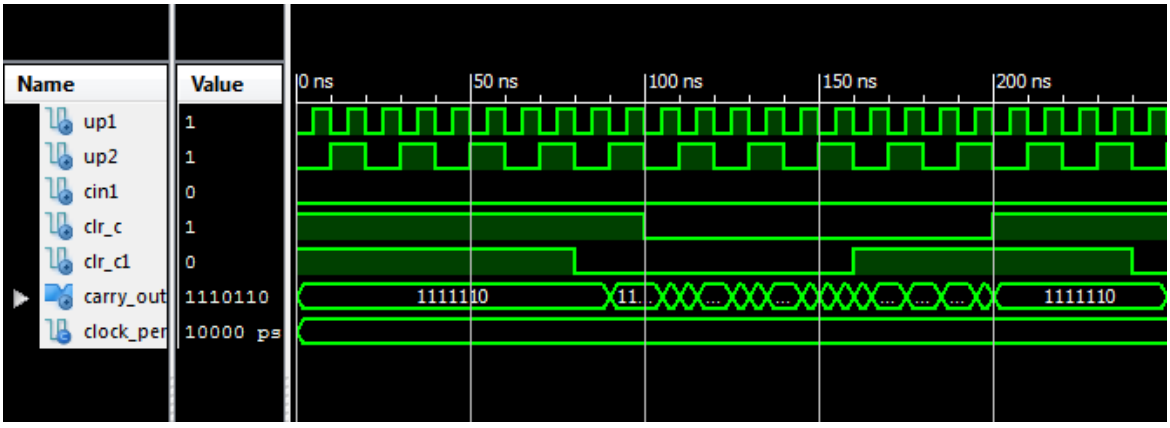
a. PHASE FREQUENCY DETECTOR:- This shows when reference signal is lagging the output qa show zero and qb shows a waveform is specifies the phase difference.



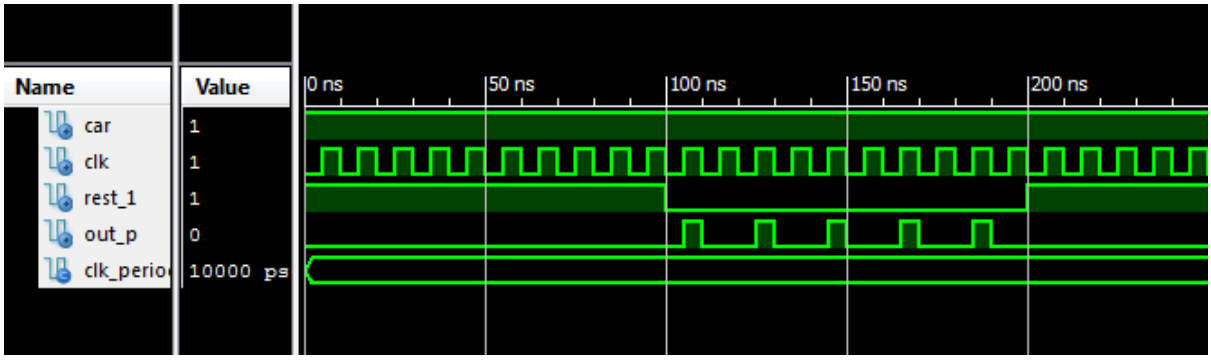

And also when reference signal is leading the output qa show the waveform showing phase diference and qb shows zero.




b. LOOP FILTER:-Loop filter consist of up counter, down counter and a carry ripple adder. The carry ripple adder takes input from the two counters and produces a carry along with sum then this carry becomes the input of a digital controlled oscillator.



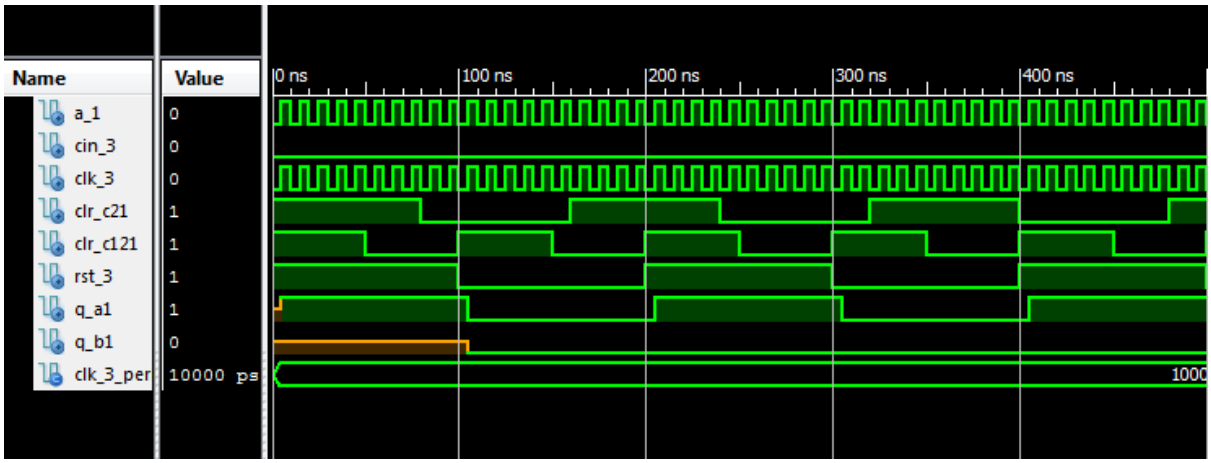

DIGITAL CONTROLLED OSCILLATOR:- It takes only carry from the loop filter as a input and consist of toggle flip flops and a logic circuit which performs the required function of a digital controlled oscillator.




Now finally this output signal feedbacks as the second input to the phase frequency detector to completes the digital phase locked loop.

ALL DIGITAL PHASE LOCKED LOOP:- Finally we can combine all the components all this phase locked loop to lock the incoming signal properly with reduced jitter as this is in complete digital domain. The incoming frequency we have taken in this case is 0.1 Ghz , it totally depends on the application we have just taken it as an example case.

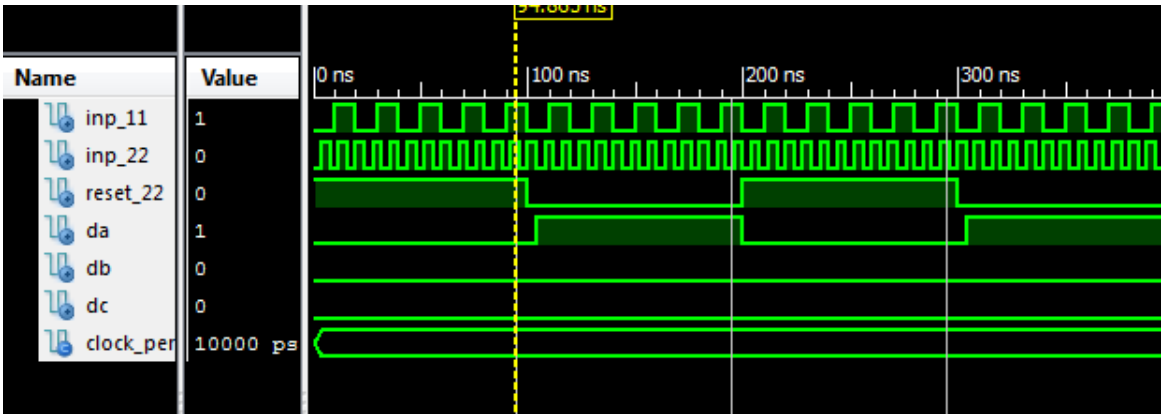
In this the feedback signal ensures that the circuit must detect the incoming signal properly and phase frequency detector produces the corresponding output .



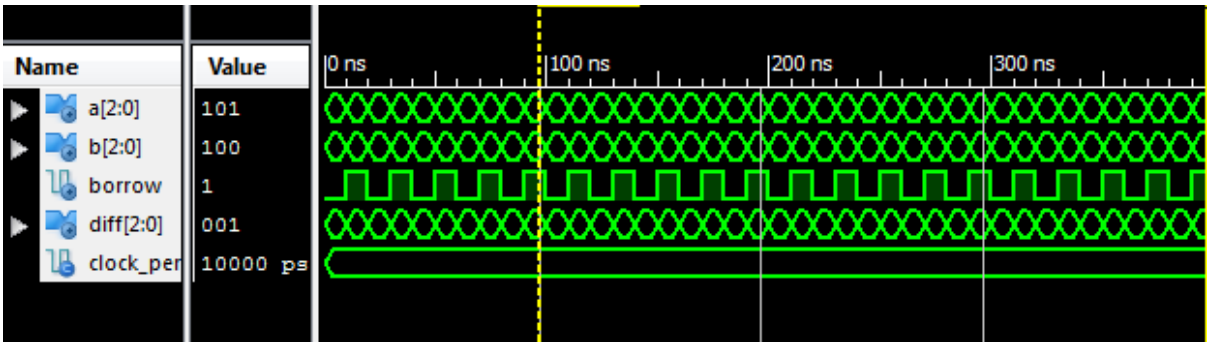

This shows the output which is the output of PFD that is phase frequency detector which shows a constant phase difference between the reference and the feedback signal.

PROPOSED ALL DIGITAL PHASE LOCKED LOOP :-This includes the additional stage of frequency comparison to reduce the lock time further and make it suitable for high speed applications .This stage make comparison between inputs that is reference and feedback signal.

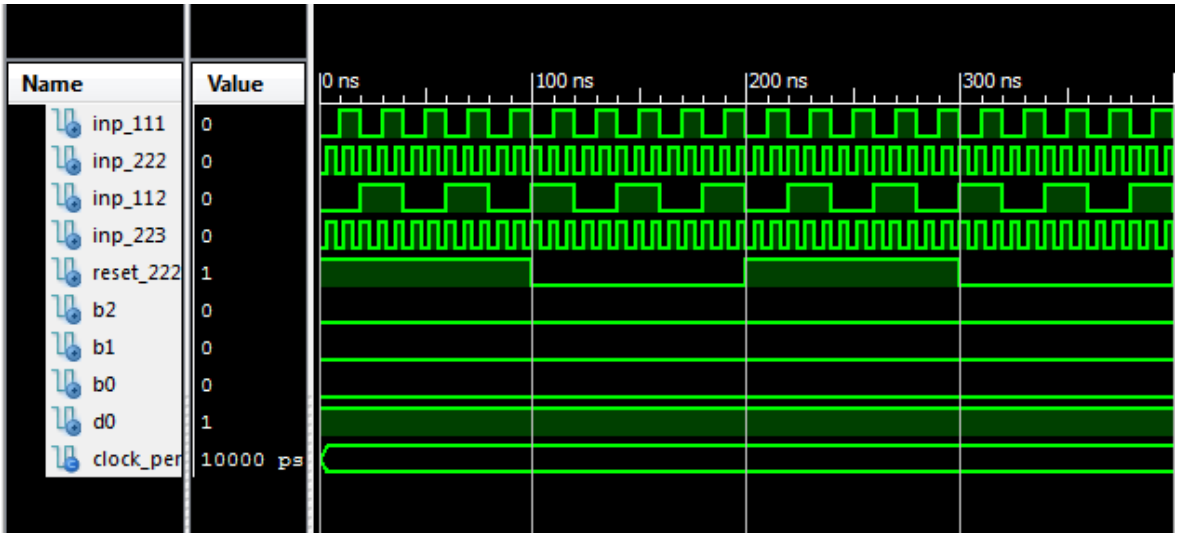
a. FREQUENCY COMPARISON STAGE:- This stage compares frequencies of feedback and the input signal and finally produces input bits for a sub-tractor circuit. Sub-tractor circuit produces a 3-bit code depends upon input bits.



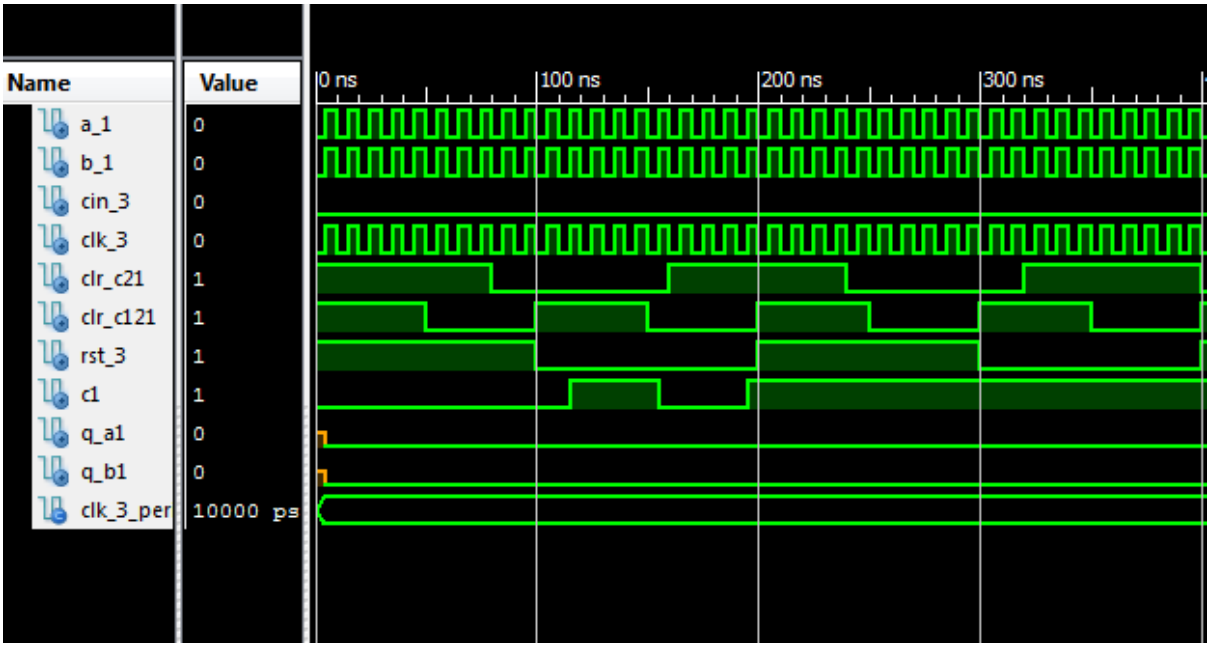

b. SUBTRACTOR STAGE:- This is a simple sub-tractor stage which is a 3 bit sub-tractor produces an output for logic block and then finally it enters into loop filter stage and the rest of the procedure is same.




c. FREQUENCY COMPARISON STAGE ALONG WITH SUBTRACTOR:-This combination produces a 3 bit output for logic block .Logic block combines this output and phase frequency detectors output to the loop filter then to digital controlled oscillator which gives feedback to the circuit.




d. PROPOSED ALL DIGITAL PHASE LOCKED LOOP RESULT:



# CONCLUSION

Here comparison between analog and digital phase locked loop is shown and found that digital phase locked loops are better than analog in many aspects. As lock time is most important parameter of a phase locked loop which decides whether a Phase locked loop is suitable for particular application or not.Designing an ALL digital phase locked is of great experience and very interesting as implemented on hardware also using a FPGA board with VHDL as a programming language for synthesizing different circuits. After this still many improvements can be made in order to improve the lock time and to reduce noise, jitter etc. So we now design a modified fast locking digital phase lock loop which can reduce the lock time and makes a phase locked loop suitable for high speed devices. Then a modified DPLL is designed to obtain the required high speed specification regarding lock time. It consists a frequency comparison state which compares the reference frequency and the output or feedback frequency then pumps the charge in the loop filter by doing this the lock time decreases significantly.

# FUTURE WORK

The comparison between Digital phase locked loop and analog phase locked loop is done and found that digitals have faster lock time as compared to analog. So they are suitable for high speed applications. Hence reduced lock times are very important in any high speed applications cellular phones, spread-spectrum communications and clock data recovery circuit.

But some very high speed applications required even further reduced lock times so a proposed model is designed using VHDL and implemented on hardware. So this model significantly reduces lock time for high speed applications.

Also, even after this other techniques can be used so to achieve further interesting results .

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