PERFORMANCE INVESTIGATION OF PULSE-WIDTH MODULATION TECHNIQUES FOR MULTI-LEVEL INVERTERS

A DISSERTATION

Submitted in partial fulfilment of the requirement for the award of the degree

of

INTEGRATED DUAL DEGREE

in

ELECTRICAL ENGINEERING

(*With Specialization in Power Electronics)*

By

RIA AGGARWAL

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE- 247667 (INDIA)

CANDIDATE'S DECLARATION

I hereby declare that the work carried out in this dissertation entitled **"PERFORMANCE INVESTIGATION OF PULSE-WIDTH MODULATION TECHNIQUES FOR MULTI LEVEL INVERTERS"** submitted in partial fulfillment of the requirements for the award of the degree of Integrated Dual Degree (IDD) in Electrical Engineering with specialization in Power Electronics, submitted to the Department of Electrical Engineering, Indian Institute of Technology Roorkee, is an authentic record of my own work carried out under the guidance and supervision of Dr. Pramod Agarwal, Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee and all the works embodied in this thesis has not been submitted elsewhere for the award of any other degree.

Date: May 2016
Place: **Roorkee** **(RIA AGGARWAL)**

CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge and belief.

(Dr. Pramod Agarwal)
Professor,
Department of Electrical Engineering,
Indian Institute of Technology Roorkee
Roorkee-247667, India

ABSTRACT

This work proposes a comparison study of various pulse width modulation (PWM) schemes using symmetrical arrangement of five level H-bridge multilevel inverter (CHBMLI) in order to find an optimized output voltage quality with lower harmonic distortion. It studies performance evaluation of the most widely used PWM schemes for three-phase voltage source inverters such as In-Phase Disposition (in-PD), Phase Opposition Disposition(POD), Alternate Phase Opposition Disposition(APOD), Variable frequency, Phase Shifted and Space Vector PWM (SVPWM) on RL load . MATLAB/SIMULINK software is used for simulation. This paper is concerned with various principles of PWM, and its use in inverters. It compares various types of modulation techniques widely used in the present scenario. The carried out simulation studies shows that space vector PWM configuration provides high output voltage with very low total harmonic distortion (THD) and better bus utilization using less switching devices.

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LIST OF ACRONYMS

PWM	Pulse Width Modulation
THD	Total Harmonics Distortion
VSI	Voltage Source Inverter
AC	Alternating Current
PD	Phase Disposition
POD	Phase Opposition and Disposition
APOD	Alternative Phase Opposition and Disposition
SVPWM	Space Vector Pulse Width Modulation
FFT	Fast Fourier Transform
MLI	Multilevel Inverter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

CHAPTER 1 INTRODUCTION

1.1 Thesis Motivation

Multilevel inverters in recent years are gaining attention of researchers and manufactures because of their ability to produce better output waveforms and lesser total harmonic distortion (THD). Pulse width modulated (PWM) inverters are the most widely used power-electronic circuits in practical applications. These inverters are capable of producing ac voltages of variable magnitude as well as variable frequency. In comparison with square wave inverters the quality of output voltage is greatly enhanced. There are different methods of implementation for several different PWM techniques,. Aim of all these techniques is to generate an output voltage, which after some filtering would be as close as possible to a quality sinusoidal voltage waveform of required fundamental frequency and magnitude. It's impossible to reduce the overall harmonic voltage distortion for this multilevel inverter topology but by proper switching control strategy often at the cost of increasing the magnitudes of higher order harmonic voltages, the magnitudes of lower order harmonic voltages can be reduced. If such a situation arises the harmonic voltages of higher frequencies can be effectively filtered using low pass filter chokes and capacitors. Many loads like motor loads have an intrinsic quality of suppressing higher frequency harmonic currents making it inessential to use any external filter. Detailed harmonic analysis is carried out to measure the quality of voltage produced by a PWM inverter.

1.2 Objective of the Thesis

This thesis presents detailed analysis of various Pulse-width modulation techniques on 5-level cascaded H-bridge multilevel inverters and detailed performance investigation of the output voltage waveform on a three phase load. The key features of the thesis include the following aspects:

- Comparison of various Multi-level inverter topologies considering their advantages and disadvantages.
- Analysis of various pulse-width modulation techniques both carrier based and space vector pulse width modulation techniques on cascaded H-bridge multilevel inverter keeping parameters such as device switching frequency, load and input dc voltage constant.

- Detailed Total Harmonic Distortion (THD) analysis of the output voltage waveform of the multilevel inverter varying the modulation index from 0.2 to 1.
- MATLAB/SIMULINK simulation results and tabulation of data for mathematical and exhaustive analysis of differences between various techniques.
- Development of hardware prototype for verification of the obtained simulation results in the laboratory.

1.3 Thesis Organization

The thesis is comprised of seven chapters. Each chapter discuss a particular aspect of various pulse width modulation techniques on multilevel inverter in detail:

Chapter 1 deals with the literature survey, objective of the thesis andthe chapter wise organization of the thesis.

Chapter 2 discusses most widely used multi-level inverter topologies and comparision between various topologies like diode clamped, flying capacitor and cascaded H-bridge multilevel inverter weighing their pros and cons. This chapter justifies why cascaded H-bridge MLI was used over other topologies.

Chapter 3 describes the various carrier based pulse width modulated strategies used for controlling the multilevel inverter i.e phase-shifted and level shifted pulse width modulation techniques. Their harmonic spectrum is analysed in detail and various aspects of these schemes like device and inverter switching frequency and their effects on the overall performance of the inverter is discussed.

Chapter 4 deals with the algorithm employed for implementation of space vector modulation scheme for multi level inverter. Comparision of space vector modulation with carrier based modulation and harmonic performance under given constraints.

Chapter 5 presents the MATLAB simulation results for operation of previously discussed modulation schemes on RL load using a five level cascaded H-bridge multilevel inverter

Chapter 6 discusses the development of hardware prototype in laboratory. Results obtained on the oscilloscope are clearly presented.

Chapter 7 presents the conclusion of the dissertation thesis and gives some recommendations for future work.

CHAPTER 2 MULTI-LEVEL INVERTER TOPOLOGIES

Multilevel inverters are able to generate high output voltages which better approaches the pure sine waveforms. They are able to produce high power quality waveforms with low voltage rating devices and lower the total harmonic distortion. They can function with lower switching frequency and losses are minimal with lower dv/dt stresses. These inverters on the other hand require a large number of semiconductor switches, isolated sources and series capacitor banks for voltage balancing. Most commonly used multi-level inverter topologies are discussed in this chapter along with their advantages and disadvantages.

2.1 Diode Clamped Multi-level Inverter

Diode Clamped Multi-level Inverter was one of the first multilevel converters and was called neutral point clamped inverter, initially proposed as a three level inverter. However the principle of diode clamping can be extended to any number of levels.

The main advantages and disadvantages of this topology are:

Advantages:

- Inverter for the fundamental switching frequency has a high efficiency.
- In order to obtain the desired voltage level the capacitors can be pre-charged together.
- For the inverter the capacitance requirement is minimized because all the phases share a common DC link.
- Reactive power flow can be easily controlled.
- Back to back intertie system can be easily controlled.

Disadvantages:

- Number of diodes and the numbers of levels share a quadratic relation which makes packaging difficult for inverters with large number of levels.
- Power transmission is problematic due to uneven intermediate DC levels without appropriate control.
- Uneven diode ratings required for the converter.

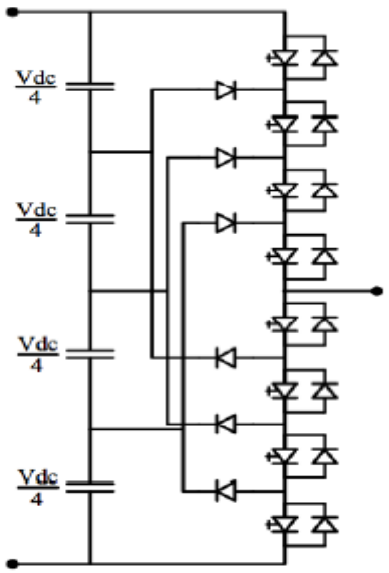


Figure 2.1Single phase 5-level Diode Clamped Inverter

output	s1	s2	s3	s4	s1′	s2′	s3′	s4′
V_{dc}	1	1	1	1	0	0	0	0
$3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_{dc}/2$	0	0	1	1	1	1	0	0
$V_{dc}/4$	0	0	0	1	1	1	1	0
0	0	0	0	0	1	1	1	1

Figure 2.2 Switching sequence of 5-level Diode Clamped Inverter

Some of the applications using Multilevel Diode Clamped converters are:

- An interface between High voltage DC transmission line and AC transmission line.
- High power medium voltage variable speed drives.
- Static VAR compensation.

2.2 Flying Capacitor Multilevel Inverter

Meynard and Foch proposed an alternative to the diode clamped inverter that is the capacitor clamped inverter which has many of its advantages. The structure of the capacitor clamped inverter is similar to that of the diode clamped converter. The major difference between both the

topologies is that the diodes are replaced by capacitors. It is commonly used for static VAR generation.

The main advantages and disadvantages of this topology are:

Advantages:

- Easily Control real and reactive power transmission.
- The inverter can handle voltages drops and spikes, and short outages owing to the large number of capacitors.
- Redundant switching states are available for voltage balancing in the capacitors.

Disadvantages

- Efficiency for real power transmission is low.
- Packaging in multi level converters is an issue due to large number of capacitors as capacitors are more expensive and bulky than diodes in the neutral point clamped inverter.
- Pre charging the capacitor voltages and system initialization is a complex procedure.

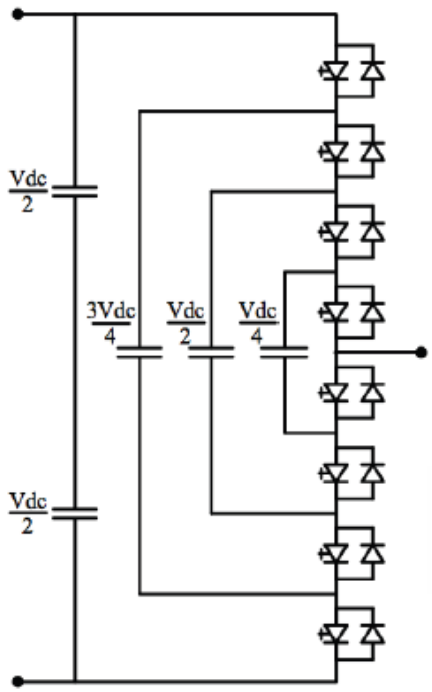


Figure 2.3 Single phase 5-level Flying Capacitor Inverter

output	s1	s2	s3	s4	s1′	s2′	s3′	s4′
V_{dc}	1	1	1	1	0	0	0	0
$3V_{dc}/4$	1	1	1	0	0	0	0	1
$V_{dc}/2$	1	1	0	0	0	0	1	1
$V_{dc}/4$	1	0	0	0	0	1	1	1
0	0	0	0	0	1	1	1	1

Figure 2.4 Switching sequence of 5-level Flying Capacitor Inverter

2.3 Cascaded H-bridge Multilevel Inverter

The cascaded multilevel inverter is based on the series connection of double leg (H bridges) inverters with separate DC sources or capacitors. For each of these two types of configurations several switching states exist.

The main advantages and disadvantages of this topology are:

Advantages:

- Identical power cells leads to a modular structure.
- Presence of large number of switching states (redundant states) for same voltage level.
- Higher voltages can be synthesized using devices of low voltage rating.
- Unequal DC voltages increases the output voltage levels without increase in the H- bridge cells in cascade.

Disadvantages:

- Each module requires a separate DC source or capacitor.
- Due to large number of capacitors which needs balancing a more complex controller is required.

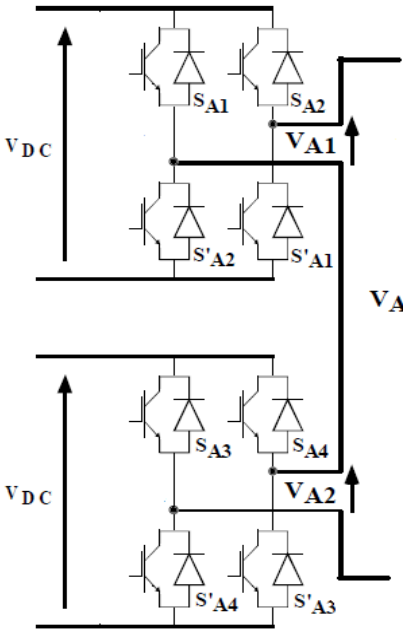


Figure 2.5 Single phase 5-level cascaded H-bridge inverter

output	s1	s2	s3	s4	s1'	s2'	s3'	s4'
$2V_{dc}$	1	0	1	0	0	1	0	1
V_{dc}	1 1 1 0	0 0 1 0	1 0 1 1	1 0 0 0	0 0 0 1	1 1 0 1	0 1 0 0	0 1 1 1
0	0 0 1 1 1 0	0 0 1 1 0 1	0 1 0 1 0 1	0 1 0 1 1 0	1 1 0 0 0 1	1 1 0 0 1 0	1 0 1 0 1 0	1 0 1 0 0 1
$-V_{dc}$	0 0 1 0	1 1 1 0	1 0 0 0	1 0 1 1	1 1 0 1	0 0 0 1	0 1 1 1	0 1 0 0
$-2V_{dc}$	0	1	0	1	1	0	1	0

Figure 2.6 Switching sequence of 5-level cascaded H-bridge inverter

A full H-bridge is made of two leg units. Each H-bridge is connected in series at the mid-point of each leg. A series connected multilevel H-bridge inverter type has many more redundant states than a single leg unit.

2.4 Comparision of various Multilevel Inverters

- Compared with other multi level inverter configurations cascaded type requires least number of components to similar voltage level
- Since each structure is similar cascaded type can be packaged easily and circuit layout can be optimized effectively.
- Cascaded type needs separate DC power sources there by limiting its utility and applications

S.No.	Topology	Diode Clamped	Flying Capacitor	Cascaded
1	Power semi conductor switches	2(m-1)	2(m-1)	2(m-1)
2	Clamping diodes per phase	(m-1)(m-2)	0	0
3	DC bus capacitors	(m-1)	(m-1)	(m-1)/2
4	Balancing capacitors per phase	0	(m-1)(m-2)/2	0
5	Voltage unbalancing	Average	High	very small
6	Applications	Motor drive system, STATCOM	Motor drive system, STATCOM	Motor drive system, PV, fuel cells, battery system

Figure 2.7 Comparision of various Multilevel Inverters

CHAPTER 3 CARRIER BASED PWM SCHEMES

The carrier-based modulation schemes for multilevel inverters can be broadly classified into two categories: **phase-shifted** and **level-shifted modulations**. The general principle of a carrier based PWM is the comparison of a reference waveform with a carrier waveform, this typically being a triangular waveform. The high order harmonic component of the output voltage and switching frequency of the converter are both based on carrier frequency. Performance of each scheme using five level H-bridge multilevel inverter is tested on RL load under similar constraints.

3.1 Phase Shifted PWM

A multilevel inverter with *m* voltage levels requires (*m* – 1) triangular carriers. In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between two adjacent carrier waves, given by 360°/(*m* – 1). The modulating signal is usually a three-phase sinusoidal wave with adjustable amplitude and frequency. The gate signals are generated by comparing the modulating wave with the carrier waves.

$$n_{carriers} = n_{voltage\ level} - 1$$

$$\varphi_{carriers} = \frac{360º}{n_{voltage\ level} - 1}$$

$$m_f = \frac{f_{cr}}{f_m} \qquad m_a = \frac{\widehat{V_{ma}}}{\widehat{V_{cr}}}$$

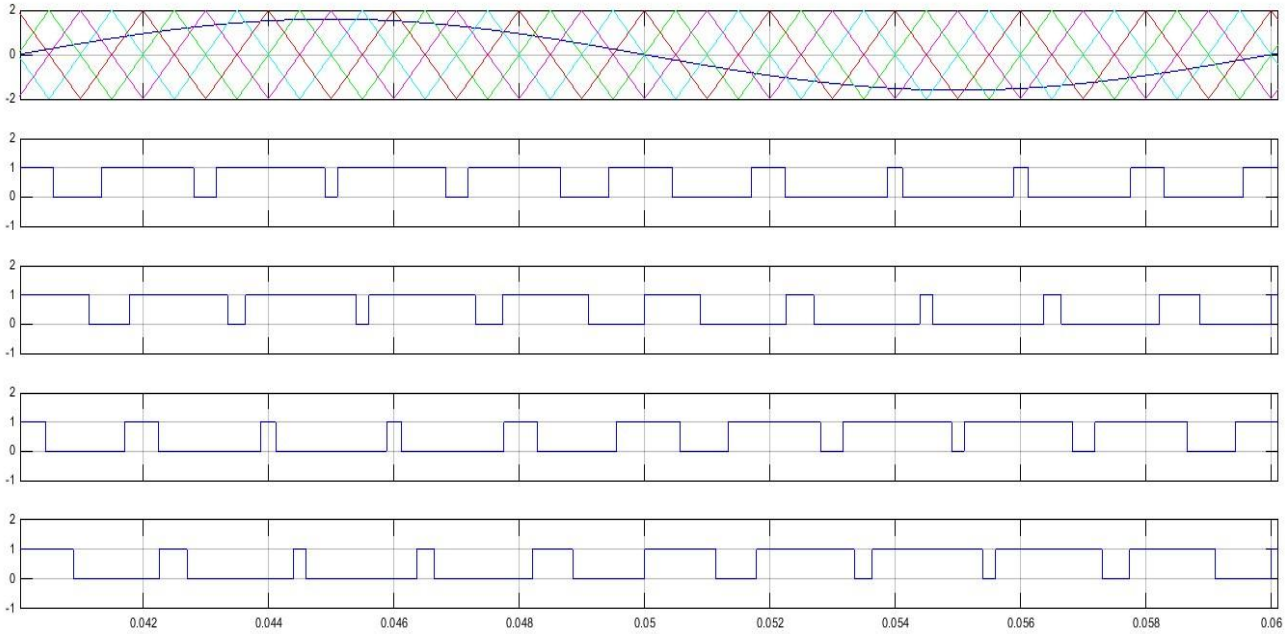


Figure 3.1 Control signals for phase-shifted PWM fm = 50Hz, mf = 10 (carrier frequency fcr = 500Hz) and ma = 0.8

The above figure shows the control signals for a five-level inverter operating under the condition of fm = 50 Hz, *mf* = 10 (carrier frequecy f_{cr} = 500Hz) and *ma* = 0.8 The device switching frequency is same as the carrier switching frequency.

$$f_{sw,dev} = f_{cr}$$

Although the carrier frequency is 500 Hz the inverter switching frequency is 2000 Hz. In general, the switching frequency of the inverter using the phase-shifted modulation is related to the device switching frequency by the following equation

$$f_{sw,inv} = (m-1)\, f_{sw,dev}$$

This is a very desirable feature of phase shifted PWM scheme because high $f_{sw,inv}$ eliminates large number of harmonics and low $f_{sw,dev}$ low $f_{sw,dev}$ reduces the switching losses. The frequency of the dominant harmonic in the inverter output voltage represents the inverter switching frequency $f_{sw,inv}$. Since the IGBTs in different H- Bridges are not switched simultaneously the magnitude of voltage step change during switching is only E. This leads to low dv/dt and reduced EMI.

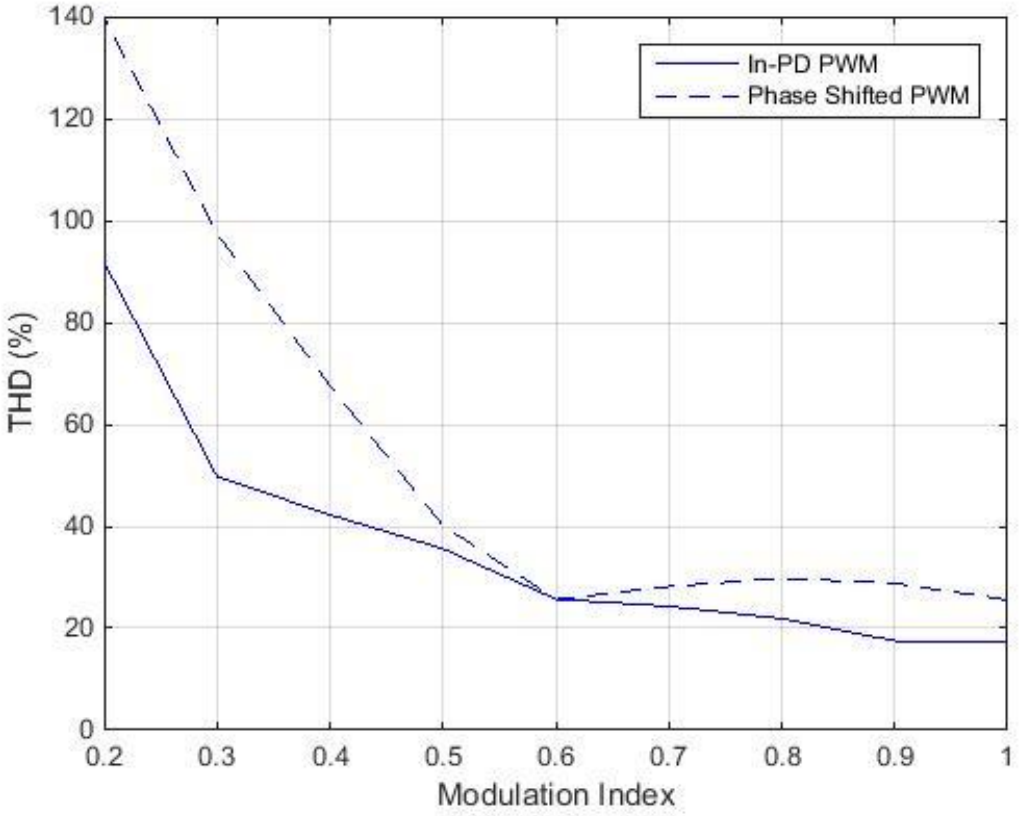


Figure 3.2 THD comparison between Phase Shifted and in-PD PWM

The Total Harmonic Distortion comparison between Phase shifted PWM and in-Phase Disposition pulse width modulation techniques over modulation range ranging 0.2 to 1, also as evident from the graph plotted my varying m_a from 0.2 to 1, reveals that considering harmonic distortion criteria in-PD modulation performs better then phase shifted modulation scheme. However, phase shifted PWM scheme as an advantage of equal switching frequency of all switching devices hence the switching losses are equal in all the semiconductor devices. Therefore for applications which require high device switching frequency phase shifted PWM technique is more viable option because higher harmonics can be easily eliminated using a low pass filter. In conclusion in order to choose between phase shifted and in-phase disposition scheme a trade-off between equal device switching frequency and lower THD has to be achieved.

3.2 Level shifted PWM scheme

A *m*-level CHB inverter using level-shifted multicarrier modulation scheme requires (m – 1) triangular carriers such that they are vertically disposed and the bands they occupy are contiguous. The level shifted PWM scheme can be further categorized into:

A. Constant switching frequency PWM: In constant switching frequency PWM scheme all the carriers have the same frequency and amplitude. It can be further subdivided into:

   1) *In-PDPWM:* In-PDPWM technique, all triangular carriers are arranged in phase.
   2) *PODPWM:* PODPWM technique, the carriers above the zero reference are in phase, but shifted by 180^0 below the zero reference.
   3) *APODPWM:* APODPWM technique, each triangular carrier is shifted by 180^0 from its adjacent carrier.

B. Variable switching frequency PWM: In variable switching frequency PWM scheme all the carriers have same amplitude but different frequency.

In general, the switching frequency of the inverter using the level-shifted modulation is equal to the carrier frequency

$$f_{sw,inv} = f_{cr}$$

and the average device switching frequency is related to carrier frequency as:

$$f_{sw,dev} = f_{cr}/(m - 1)$$

3.2.1 In-Phase Disposition PWM scheme

A *m*-level CHB inverter using In-PDPWM scheme requires (*m* – 1) triangular carriers such that they are in phase and vertically disposed such that the bands they occupy are contiguous. All the carriers have same frequency and amplitude. The modulating signal is usually a three-phase sinusoidal wave with adjustable amplitude and frequency.

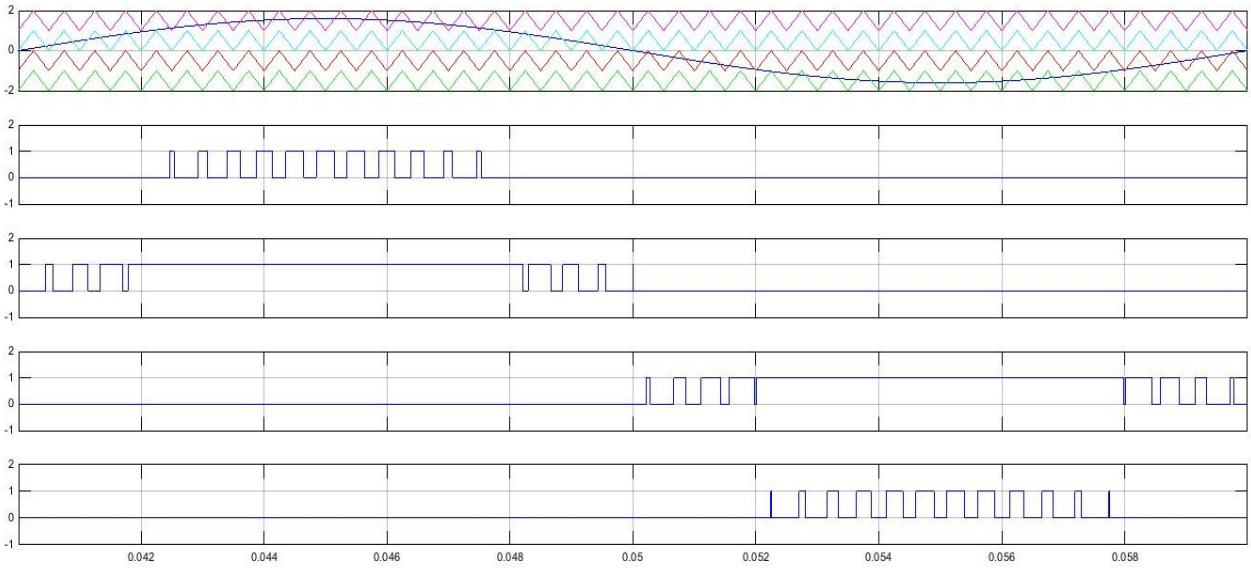


Figure 3.3 Control signals for In-PDPWM , fm = 50 Hz, mf = 40 and ma = 0.8

The above figures shows the control signals for a five-level inverter operating under the condition of *fm* = 50 Hz, *mf* = 40 (carrier frequency f_{cr} = 2000Hz) and *ma* = 1.0. Although the carrier frequency of 2000 Hz seems high for high-power converters, the average device switching frequency is only 500 Hz. The inverter switching frequency is the same as the carrier frequency i.e 2000 Hz. High inverter switching frequency eliminates the harmonics and low device switching frequency keeps the switching losses in check . The switching frequency is not the same for the devices in different H-bridge cells. In addition to the unequal device switching frequencies, the conduction time of the devices is not evenly distributed either which is one of the major drawback of this scheme. In order to evenly distribute the switching and conduction losses the switching pattern of the devices must rotate.

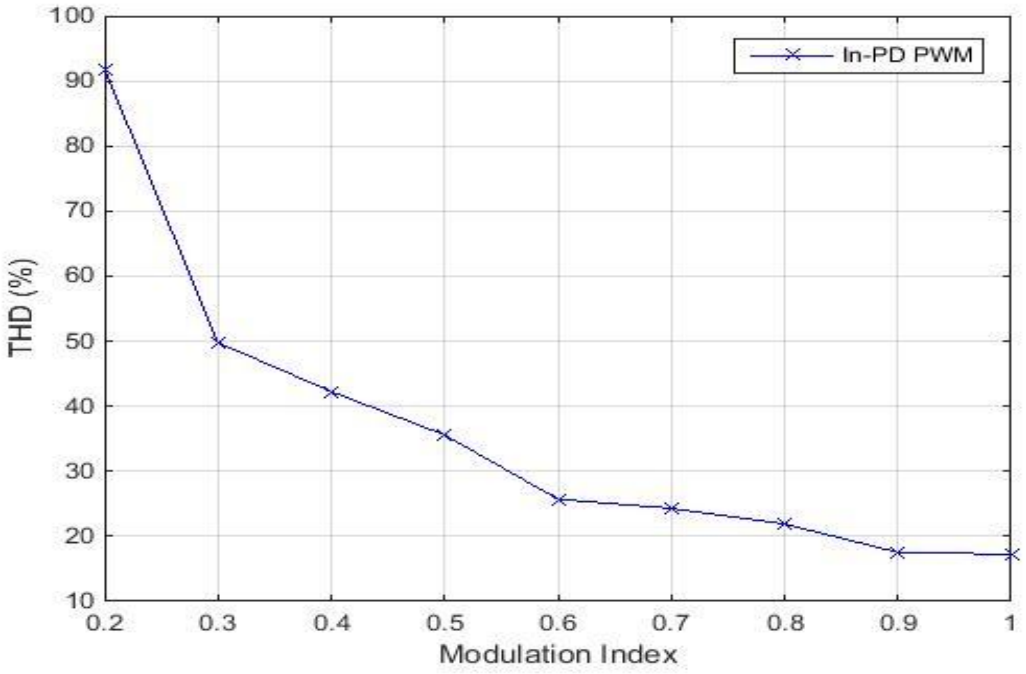


Figure 3.4 Voltage THD variation with modulation index for in-PD PWM

Modulation index m_a is varied from 0.2 to 1 and the corresponding Voltage THD values are recorded and plotted for inverter switching frequency of 2kHz which reveals that the in-PD scheme exhibit very low value of THD specifically in m_a range 0.6-1 at a particular switching frequency. In-PD scheme performs better than phase shifted PWM technique in terms of harmonic distortion values as seen in the previous unit. In the next unit comparison between various carrier based schemes will be discussed along with the advantages and disadvantages of each scheme. In order to combat the issue of unequal device switching frequency a new scheme variable switching frequency PWM is proposed and its performance in evaluated under the given constraints.

3.2.2 Phase Opposition Disposition PWM scheme (PODPWM)

A *m*-level CHB inverter using In-PDPWM scheme requires (*m* – 1) triangular carriers such that they the carriers above the zero reference are in phase, but shifted by 180 deg. below the zero reference and vertically disposed and the bands they occupy are contiguous. All the carriers have same frequency and amplitude.

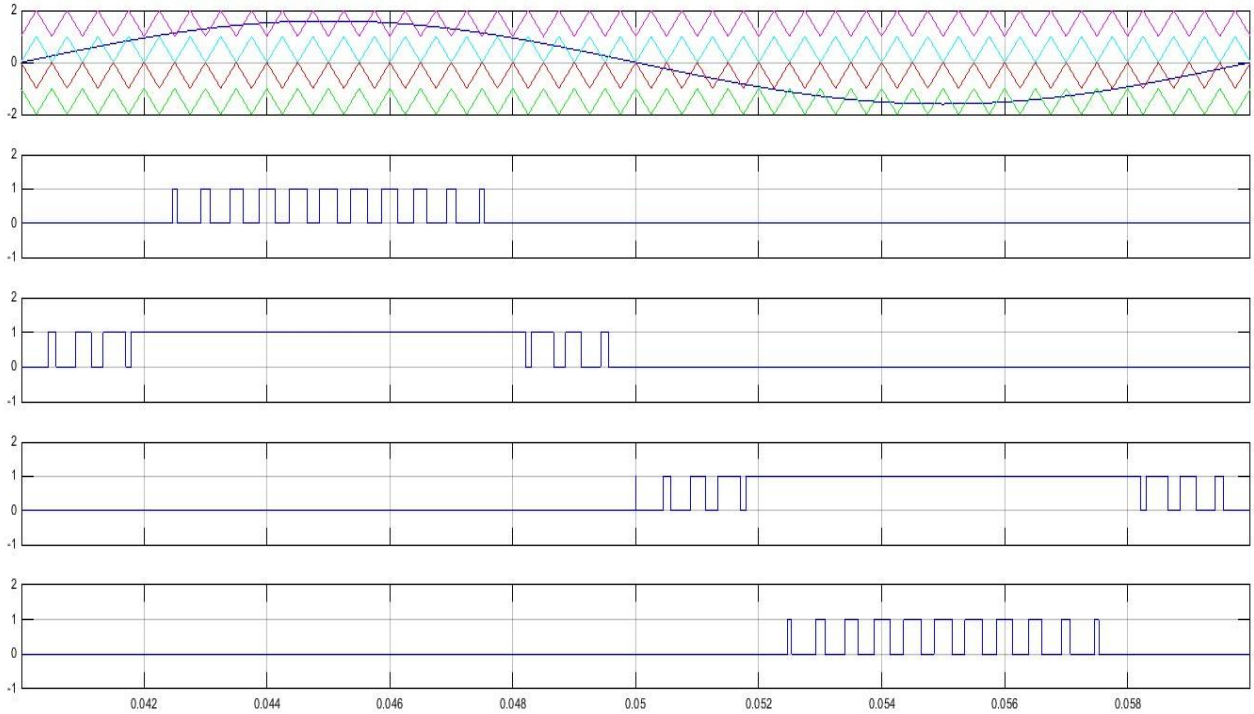


Figure 3.5 Control signals for PODPWM, fm = 50 Hz, mf = 40 anf ma = 0.8

The above figures shows the control signals for a five-level inverter operating under the condition of f_m = 50 Hz, m_f = 40 (carrier frequency f_{cr} = 2000Hz) and m_a = 1.0. Although the carrier frequency of 2000 Hz seems high for high-power converters, the average device switching frequency is only 500 Hz. It also shares the same drawback of unequal device switching frequencies, the conduction time of the devices is not evenly distributed either . In order to evenly distribute the switching and conduction losses the switching pattern of the devices must rotate

3.2.3 Alternate Phase Opposition Disposition PWM scheme (APODPWM)

A *m*-level CHB inverter using In-PDPWM scheme requires (m – 1) triangular carriers such that each carriers is shifted by 180^0 from its adjacent carrier. All the carriers have same frequency and amplitude.

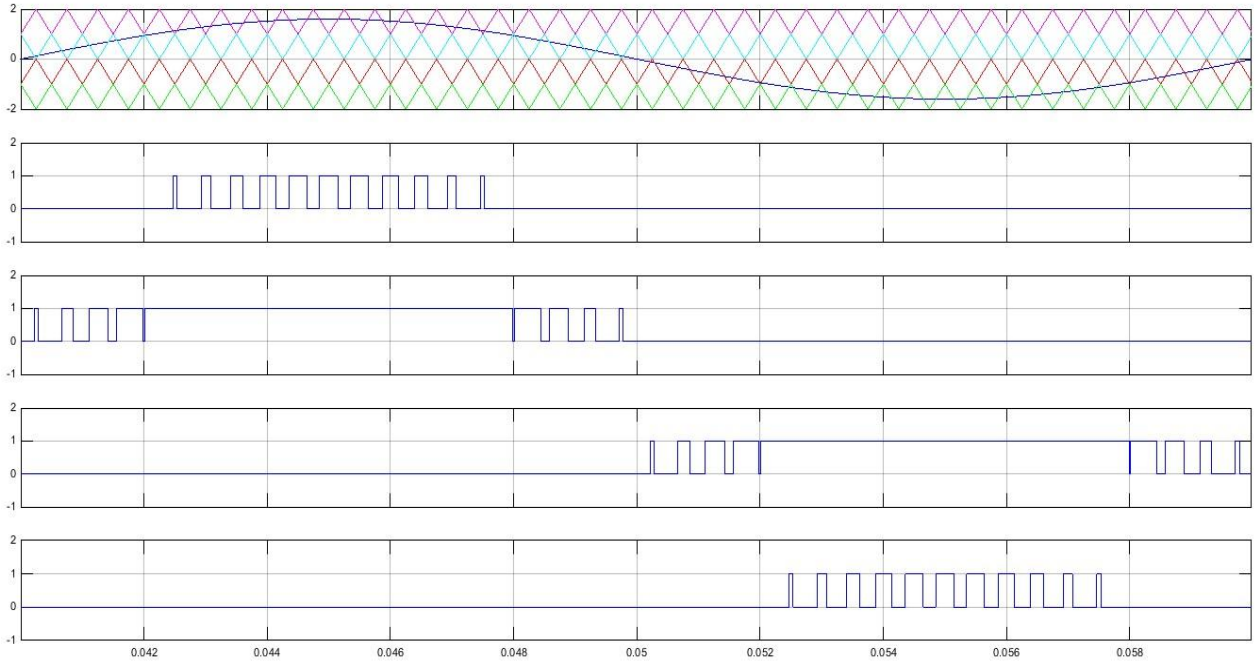


Figure 3.6 Control signals for APOD PWM, fm = 50 Hz, mf = 40 and ma = 0.8

The following figures shows the simulated waveforms for a five-level inverter operating under the condition of f_m = 50 Hz, m_f = 40 (carrier frequency f_{cr} = 2000Hz) and m_a = 1.0. The average device switching frequency is only 500 Hz and the inverter switching frequency is the same as the carrier frequency i.e 2000 Hz. . It also shares the same drawback of In-PDPWM and PODPWM schemes

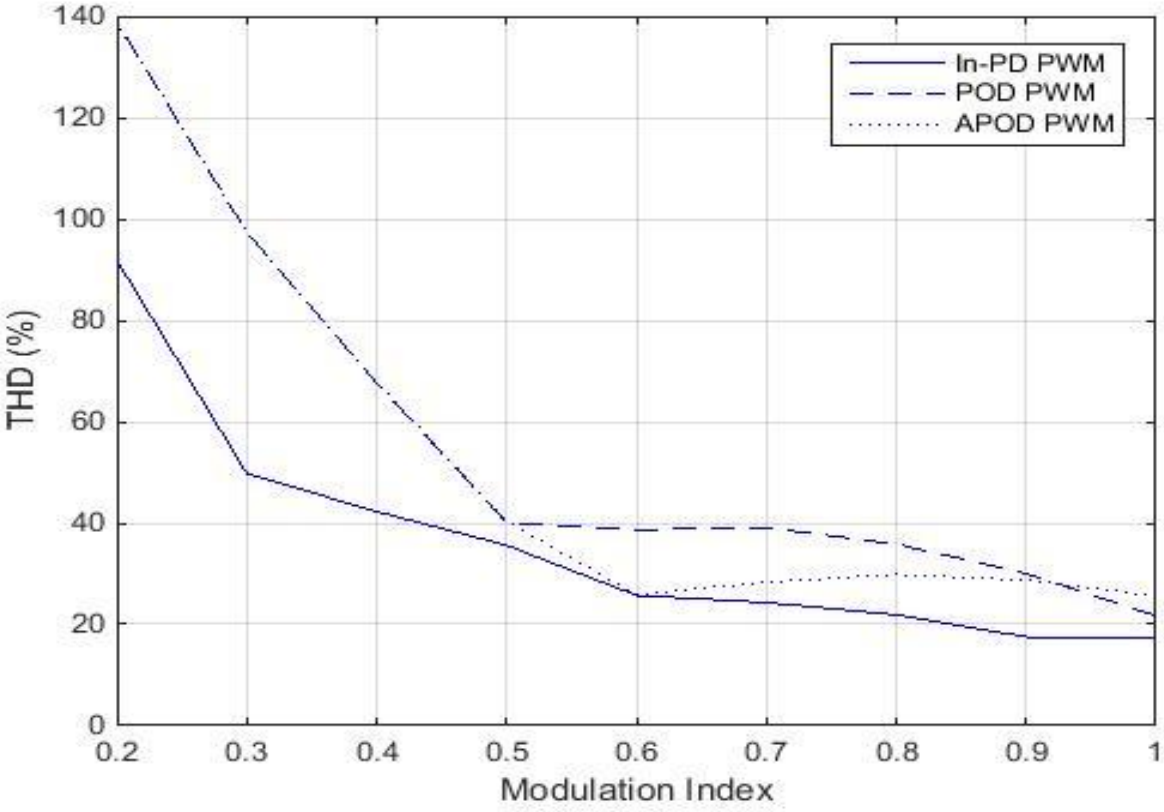


Figure 3.7 Voltage THD comparison between in-PD, POD and APOD PWM

The Total Harmonic Distortion comparison between in-PD, APOD and POD pulse width modulation techniques over modulation range ranging from 0.2 to 1 reveals that considering harmonic distortion criteria in-PD modulation performs better then phase shifted modulation scheme. Moreover all these schemes share the same disadvantage of unequal device switching frequency. Therefore it can be easily concluded that in- Phase Disposition scheme is superior to both APOD and POD schemes for most practical purposes.

3.2.4 Variable Switching frequency PWM

A *m*-level CHB inverter using In-PDPWM scheme requires (*m* – 1) triangular carriers such that each carrier is in phase have same amplitude but different frequency. The modulating signal is usually a three-phase sinusoidal wave with adjustable amplitude and frequency.

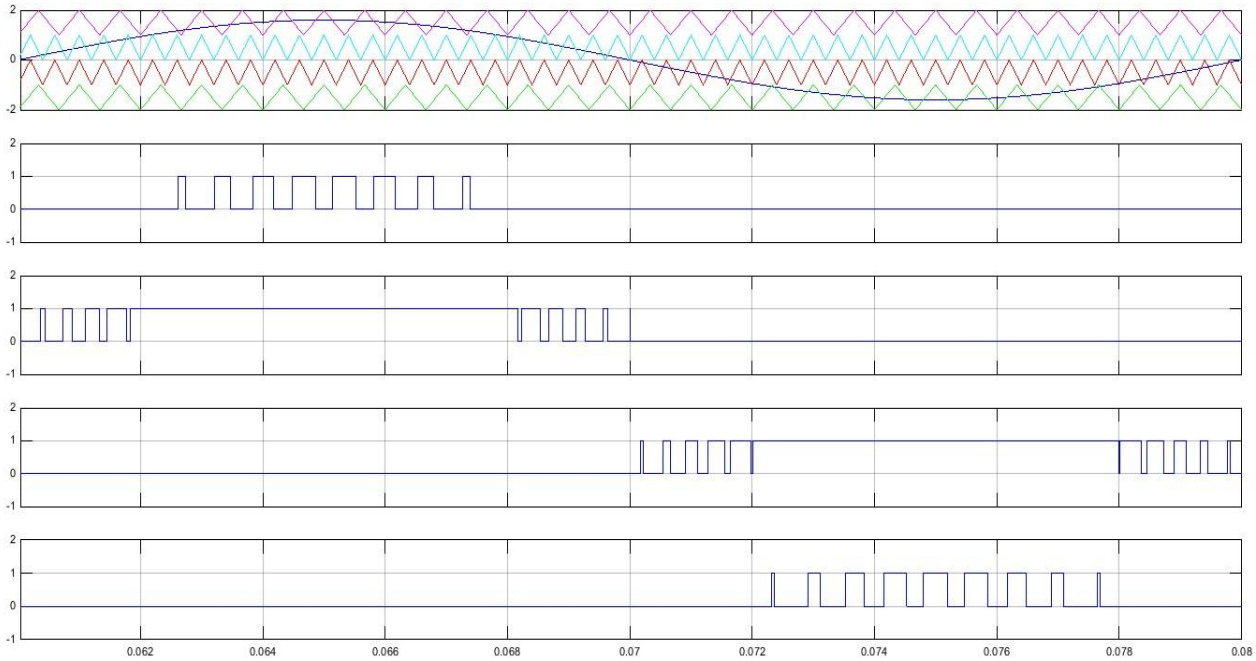


Figure 3.8 Control signals for variable frequency PWM fm = 50 Hz, carrier frequency fcr = 1500Hz & 2500Hz and ma = 0.8

The above figures shows the simulated waveforms for a five-level inverter operating under the condition of f_m = 50 Hz, carrier frequency f_{cr} = 1500Hz & 2500Hz and ma = 1.0. All the former multicarrier PWM schemes share the similar problem of unequal device switching frequencies and conduction time. Variable switching frequency scheme aims at solving the unequal switching frequency problem by increasing the frequency of the carriers closer to zero reference and decreasing the frequency of the carriers as we move away from the zero reference. The average inverter switching frequency is the same as that of the earlier discussed schemes i.e 2000 Hz.. Moreover the switching losses of the devices are now comparatively equal as compared to other multi-carrier schemes.

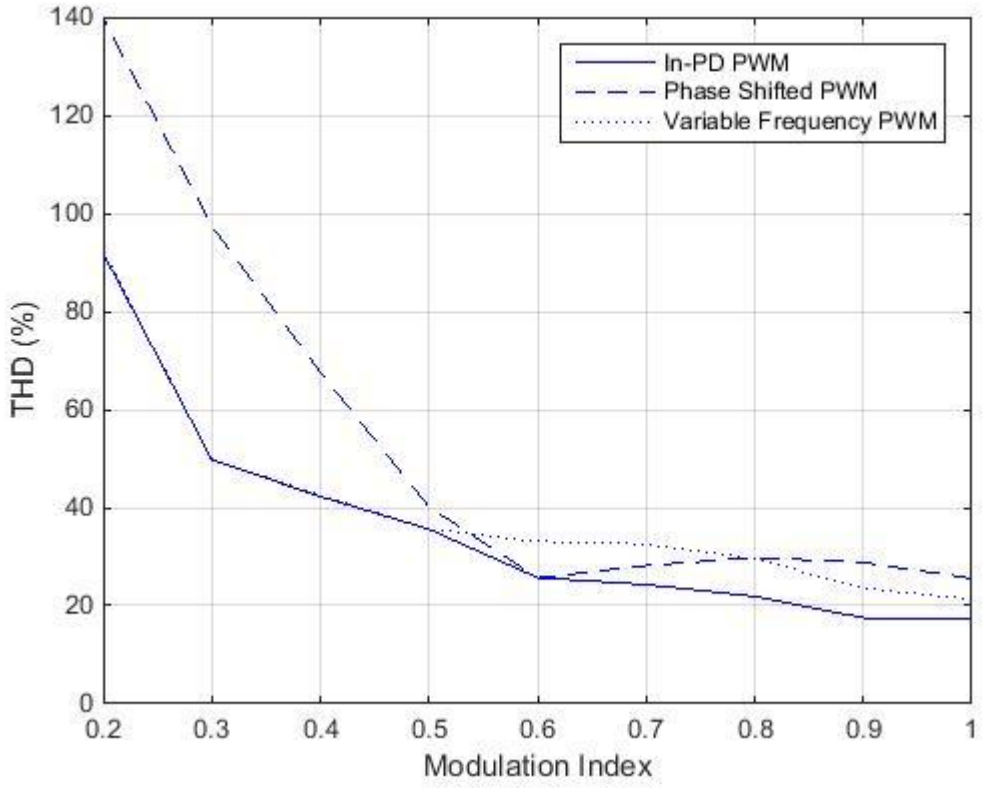


Figure 3.9 Voltage THD comparison between in-PD, Phase Shifted and Variable frequency PWM

Comparison of total harmonic distortion between Phase shifted, in-PD and Variable frequency PWM shows that for the lower modulation index m_a range(less than 0.5) both in-PD and Variable frequency PWM technique display same THD levels but Variable frequency have an added advantage of equal device switching frequency. Modulation index range between 0.5 to 0.8 Phase Shifted scheme shows better results due to low harmonic distortion and no imbalance in device switching frequency. Between m_a range 1 to 0.8 Variable frequency PWM scheme displays better results without any disadvantages.

CHAPTER 4 SPACE VECTOR PWM

4.1 Space Vector Modulation

Space vector modulation (SVM) is representation of the three phase quantities in two-dimensions (d q) plane as vectors**.** In Space vector modulation technique co-ordinate transformation of phase voltages from abc to qd plane is done using the following equation:

$$\therefore \begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix}$$

A three-phase quantity is transformed into stationary d-q coordinate frame as vectors representing spatial vector sum of the three-phase quantity. Spatial transformation of all the vectors leads to formation of hexagon with active vectors and null vectors. The vectors divide the plane into six sectors.

The principle behind the Space Vector Modulation is that the sinusoidal voltage rotates with a constant amplitude at constant frequency. The reference voltage V_{ref} is approximated by a combination of the switching vectors using this scheme.

V_{ref} can be defined as a mean space vector over a switching period T_S. This vector generates the fundamental behavior governing this scheme by assuming that T_S is sufficiently small it can be approximated that V_{ref} is constant in that interval. Hence weighted average combination of the adjacent space vectors can express every vector V_{ref} present inside the hexagon. Therefore the desired reference vector may be achieved by switching between those inverter states. Optimum harmonic performance and the minimum switching frequency can be achieved if the transition from one state to the next is performed by switching only one inverter leg. Active and zero-state times for each modulation cycle can be calculated using volt-second balance equations. These equations are the fundamental part of any Space vector modulation scheme.

4.2 Space Vector Modulation Algorithm for Multilevel inverters

Space vector modulation (SVM) for three-leg VSI is based on the representation of the three phase quantities as vectors in a two-dimensional (α β) plane. V_{ref} is the reference vector in space of magnitude $|V_{ref}|$ at angle ϴ with α-axis. $|V_{ref}|$ is calculated from V_α V_β which are obtained from three-phase to two-phase transformation of reference signal.

$$|V_{ref}| = \sqrt{V_\alpha^2 + V_\beta^2}$$

and

$$\theta = \tan^{-1}\left(V_\beta / V_\alpha\right)$$

Computation of dwell times in sector- l is applicable to other sectors due to the symmetry in the space vector diagram. Sector of operation for any given reference vector is given by

$$S_r = \text{int}\left(\frac{\theta}{\pi/3}\right) + 1$$

Where ϴ ($0 < \theta < 2\pi$) is the angle of the reference vector with α –axis. int and rem are standard math function "integer" and "remainder", respectively.

$|V_{ref}|$ is decomposed into m and n axis respectively

$$Vrm = (2*M*Vref/3Vdc)\ \sin(\pi/3 - \theta)$$
$$Vrn = (2*M*Vref/3Vdc)\ \sin(\theta)$$

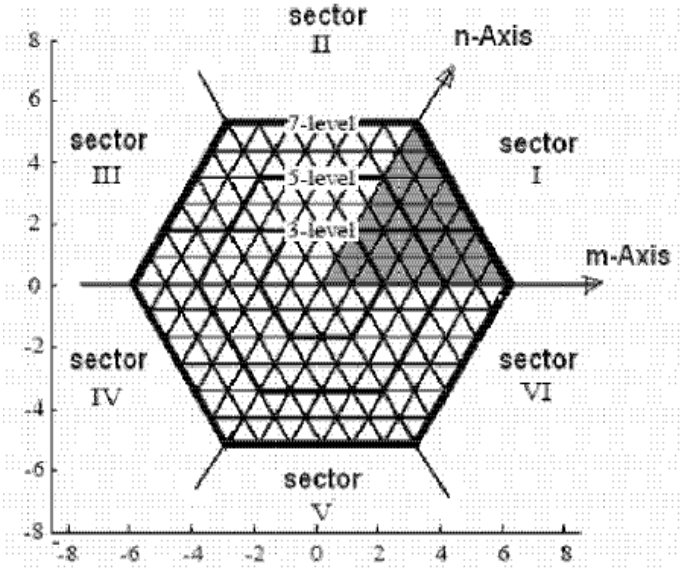


Figure 4.1 Space vector distribution for Multi level Inverters

After calculating *Vrm* and *Vrn*, calculate the lower rounded integer value (m and n) m = int(*Vrm*) and n = int(*Vrn*). If *(Vrm +Vrn) <= (m+n+1)* than the reference vector is located in the left bottom triangle DEF otherwise upper right triangle EFG.

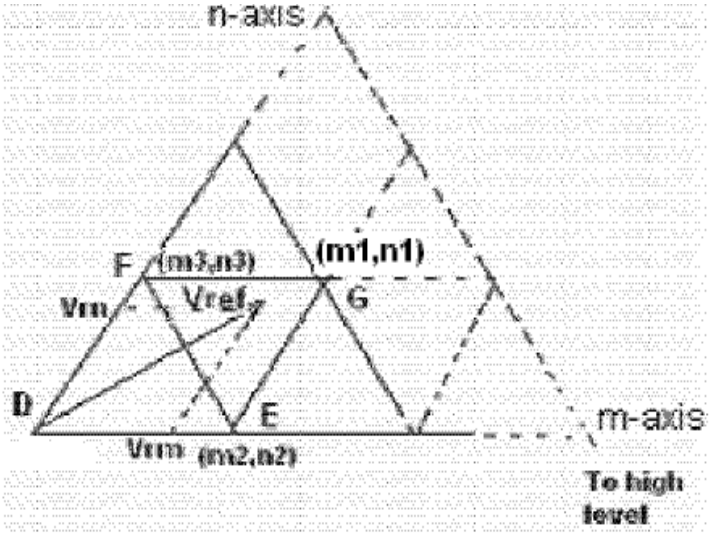


Figure 4.2 Decomposition of reference voltage into m-n axis

Find the three sides of the triangle namely (m_1,n_1), (m_2,n_2) and (m_3,n_3).Now this information can be used to calculate the dwell times using the following formulas:

$$m_1 * T_1 + m_2 * T_2 + m3 * T_3 = V_{rm} * T_{PWM}$$

$$n_1 * T_1 + n_2 * T_2 + n3 * T_3 = V_{rn} * T_{PWM}$$

$$T_1 + T_2 + T_3 = T_{PWM}$$

Where T_{PWM} is PWM time period

Switching state for each switching vector can be determined such that switching losses are minimized by selecting the switching sequence with least number of switching. In the multilevel inverter, the redundant switching states increase with the voltage level. In the diode clamped multilevel inverters, the redundant switching states can be utilized to balance the voltage of capacitors in the dc link but the cascaded H-Bridge inverter inherently does not have this problem. However, the redundancy is employed to minimize the voltage harmonic distortion only.

Switching states can be determined by determining the nature of space vector. Any space vector(m,n) can be classified into the following categories:

Category 1: Even Vector - the sum of its coordinates (m, n) is even. If both m and n are even or both are odd then the a corresponding switching state is mean state

$$S_{am} = \{(m+n-p)+p\}/2 = (m+n)/2$$
$$S_{bm} = \{(n-p)+(p-m)\}/2 = (n-m)/2$$
$$S_{cm} = \{(-p)+(p-m-n)\}/2 = -(m+n)/2$$

Category 2: Odd Vector - the sum of its coordinates (m, n) is odd

- Case 1: If m is odd and n is even then the corresponding switching state is large state

$$S_{al} = (m+n+1)/2$$
$$S_{bl} = (n-m+1)/2$$
$$S_{cl} = -(m+n-1)/2$$

- Case 2: If m is even and n is odd then the corresponding switching state is small state

$$S_{as} = (m+n-1)/2$$
$$S_{bs} = (n-m-1)/2$$
$$S_{cs} = (m+1+1)/2$$

Where Sa, Sb and Sc are mean switching states for phase A, B, and C.

The switching sequence design has to meet a number of requirements such as:

a) Minimize the number of switching per sampling period

b) One voltage level change per commutation of switching devices

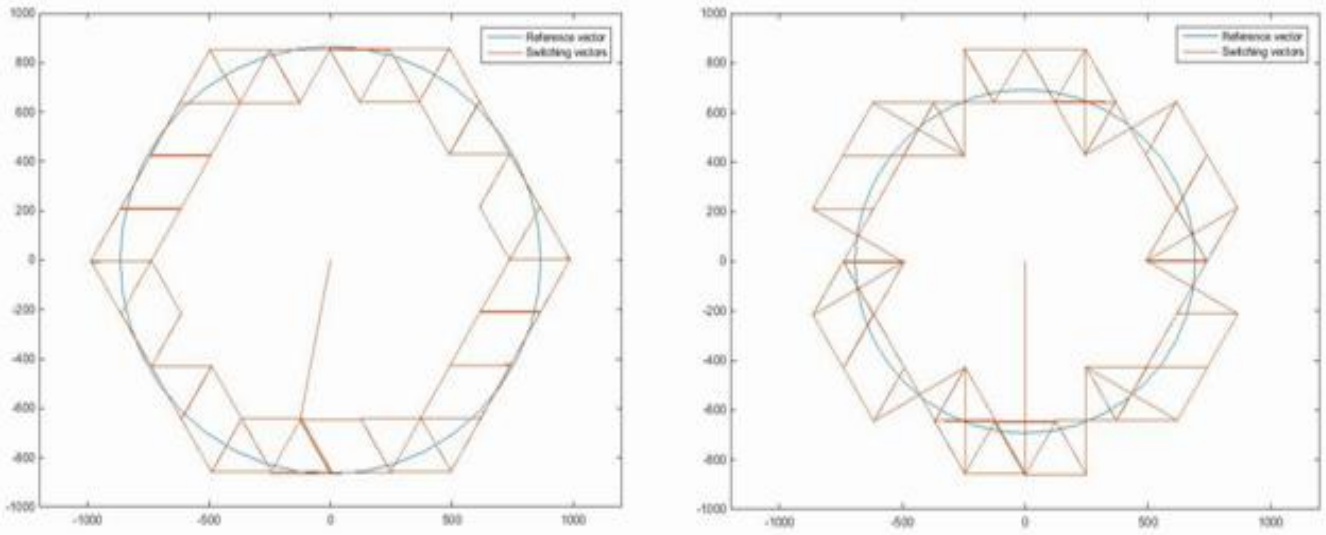


Figure 4.3 Reference and Switching vector trajectory for SVPWM for ma = 1(left) and ma= 0.8 (right)

The following figures shows the trajectory traced by the reference vector and space vectors for a five-level inverter operating under the condition of PWM switching frequency 2000Hz and *ma* = 1.0. The presence of triplen harmonics boosts the fundamental voltage by a factor of 15.5% as compared to phase-shifted and multicarrier PWM schemes.

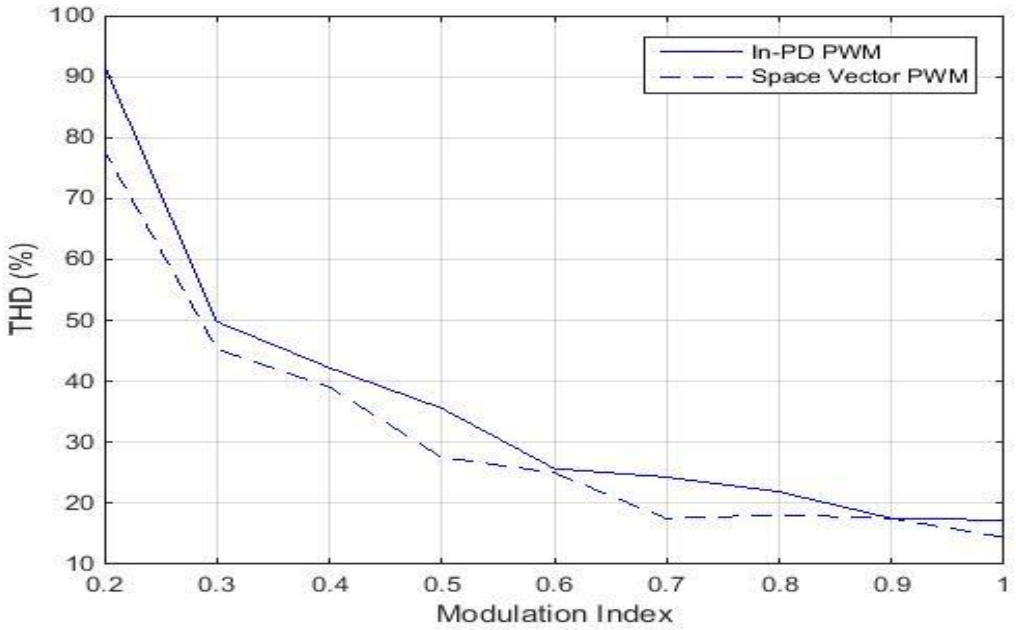


Figure 4.4 Voltage THD comparision between Space Vector and in-PD PWM

Voltage THD comparison between Space Vector and In-PD PWM technique, varying m_a from 0.2 to 1 reveals that space vector displays lower THD and better performance than in-PD PWM scheme for inverter switching frequency of 2kHz. Moreover the fundamental Voltage in case of space vector modulation is boosted by a factor of 15.5%

$$\frac{V_{\max,SVM}}{V_{\max,SPWM}} = 1.155$$

Implementation of SVPWM scheme is complex because of large number of inverter switching states. Hence we see that there is a certain trade off that exists while using SVPWM for inverters for Adjustable speed Drive Operations between complexity and better harmonic performance.

CHAPTER 5 SIMULATION RESULTS

The simulation parameters for three phase symmetrical multilevel inverter with RL load are as follows

Input DC voltage, V_{dc1} =250V, V_{dc2} =250V

Reference switching frequency, f_m =50Hz

Inverter switching frequency, $f_{sw,i}$ =2 kHz

Amplitude modulation index = 1.0

Three Phase Load, R =25 Ω, L=25mH

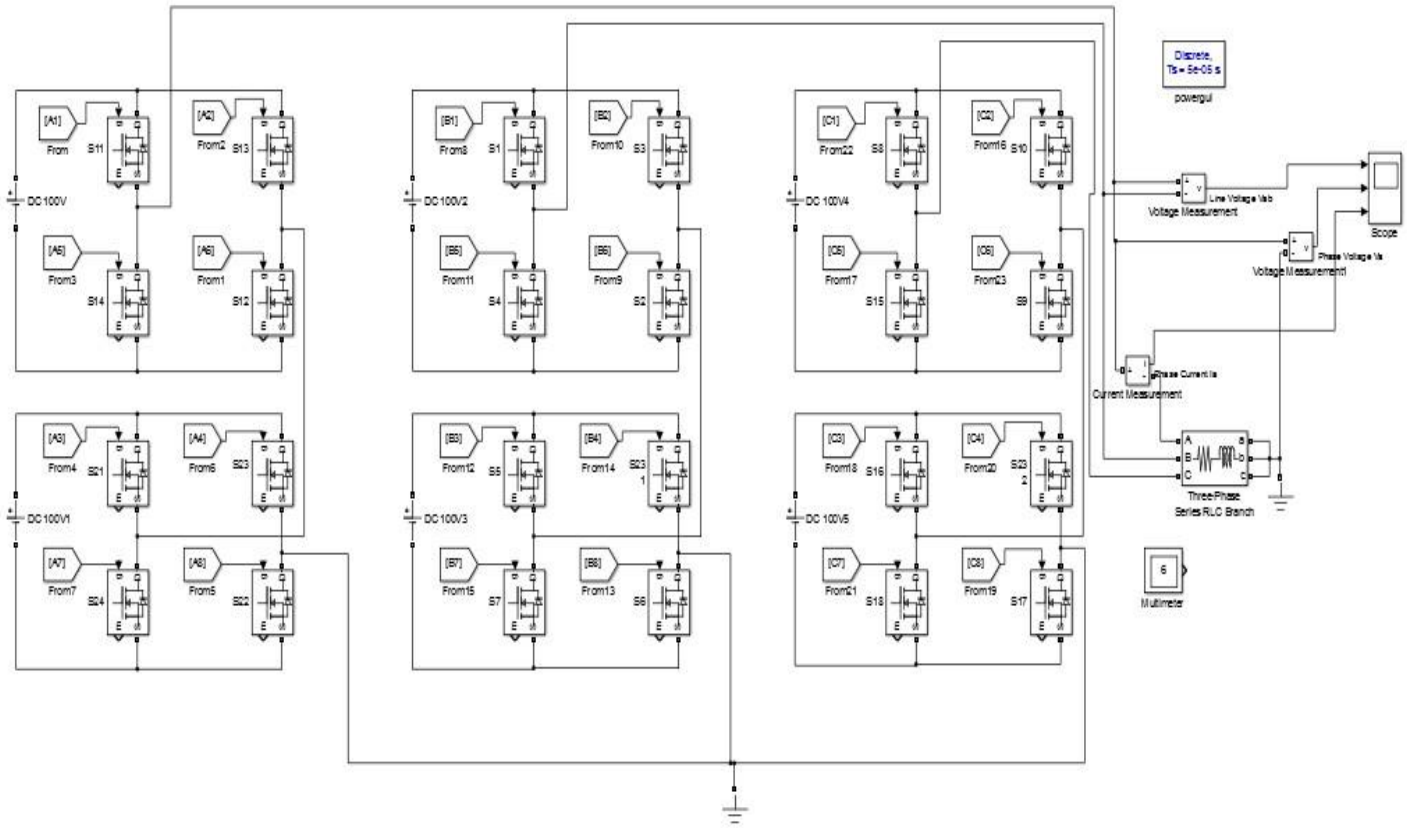


Figure 5.1 Matlab Simulink circuit of five-level cascaded H-Bridge MLI with RL load

5.1 Three Phase Load testing of Phase shifted PWM scheme

Line Voltage V_{ab}

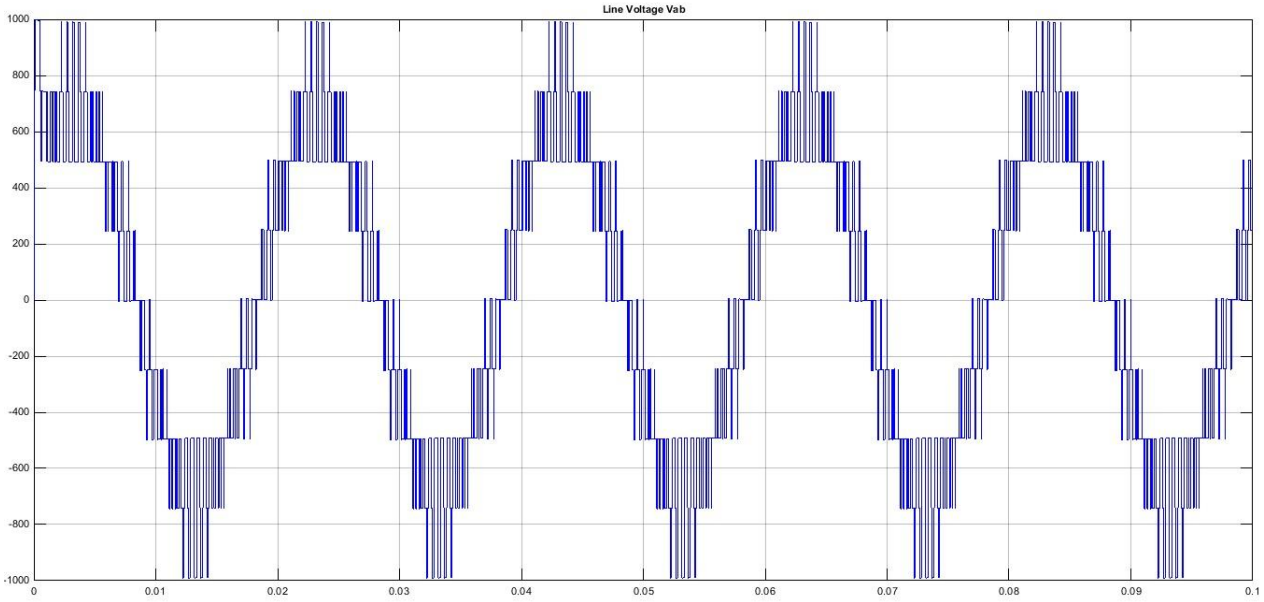


Figure 5.2 Line voltage for phase-shifted PWM scheme, , fm = 50 Hz, mf = 10 and ma = 0.8

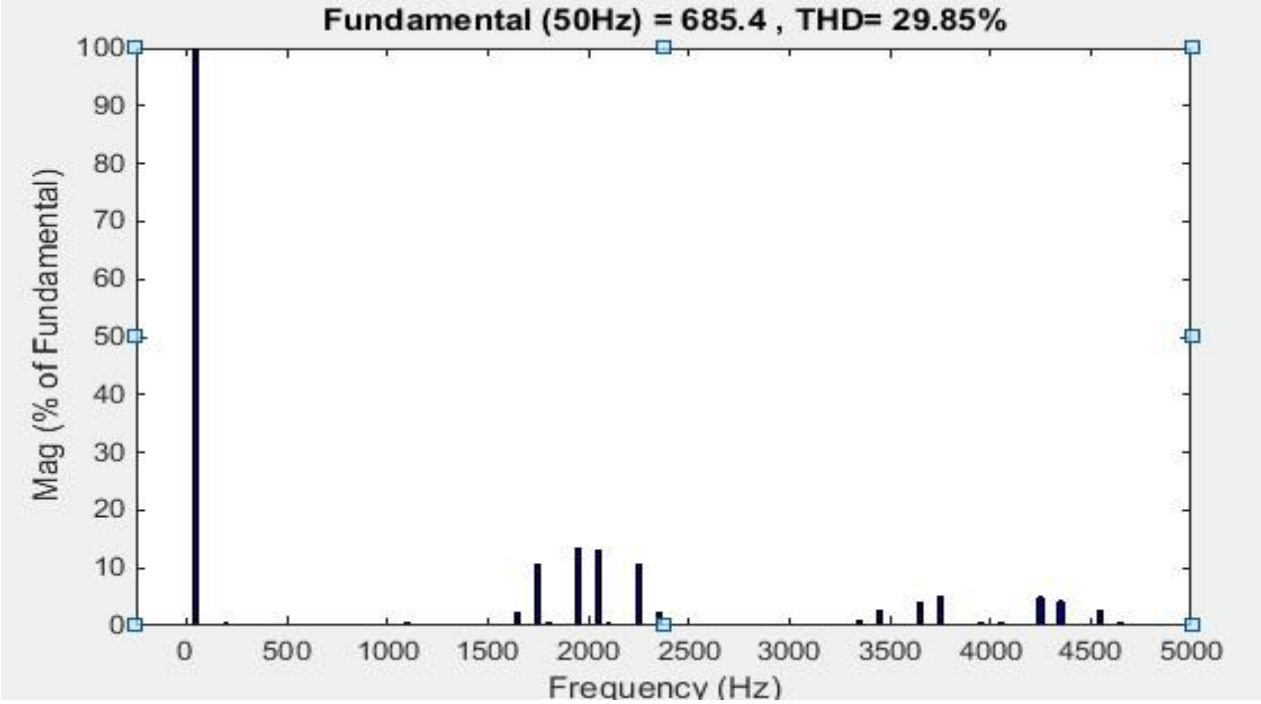


Figure 5.3 FFT analysis of line voltage

Phase Voltage V_a

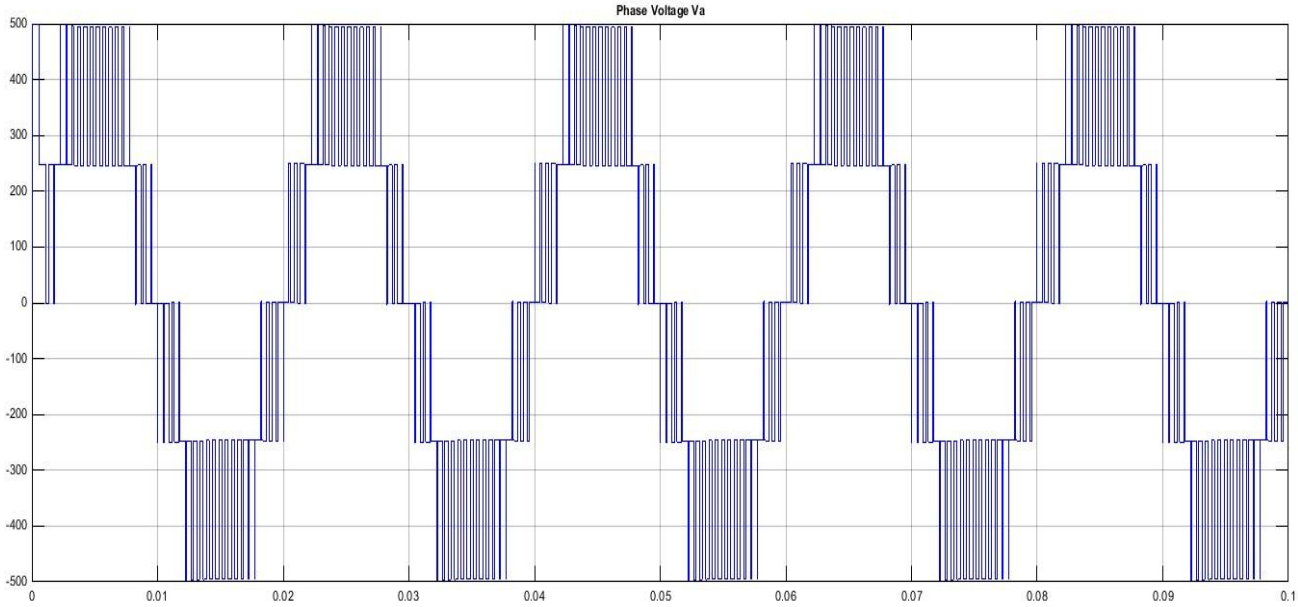


Figure 5.4 Phase voltage for phase-shifted PWM scheme, , fm = 50 Hz, mf = 10 and ma = 0.8

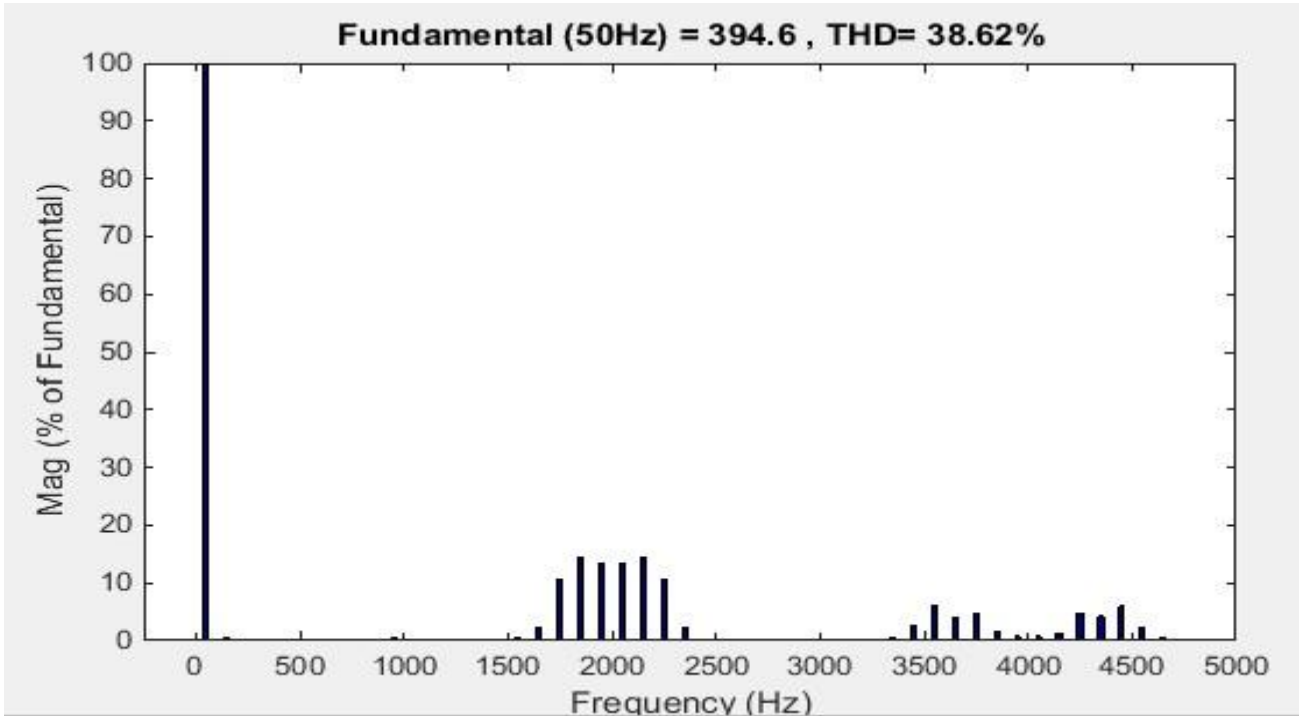


Figure 5.5 FFT analysis of Phase Voltage

Phase Current I_a

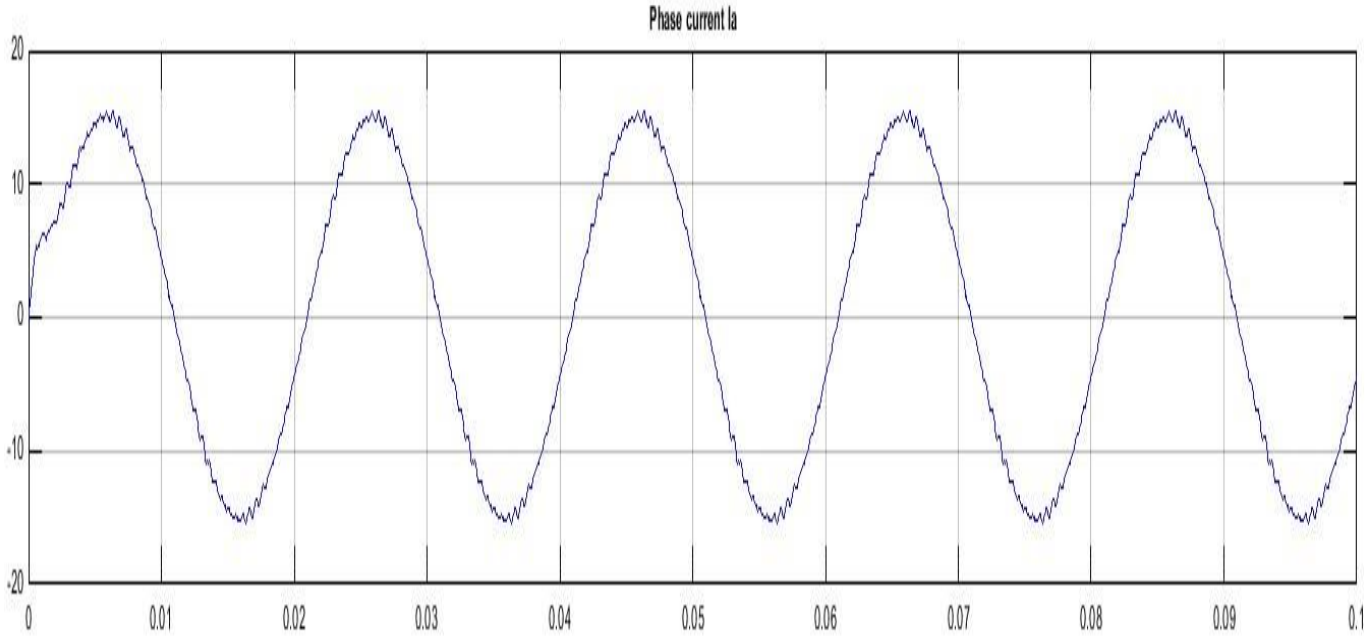


Figure 5.6 Phase current for phase-shifted PWM scheme, , fm = 50 Hz, mf = 10 and ma = 0.8

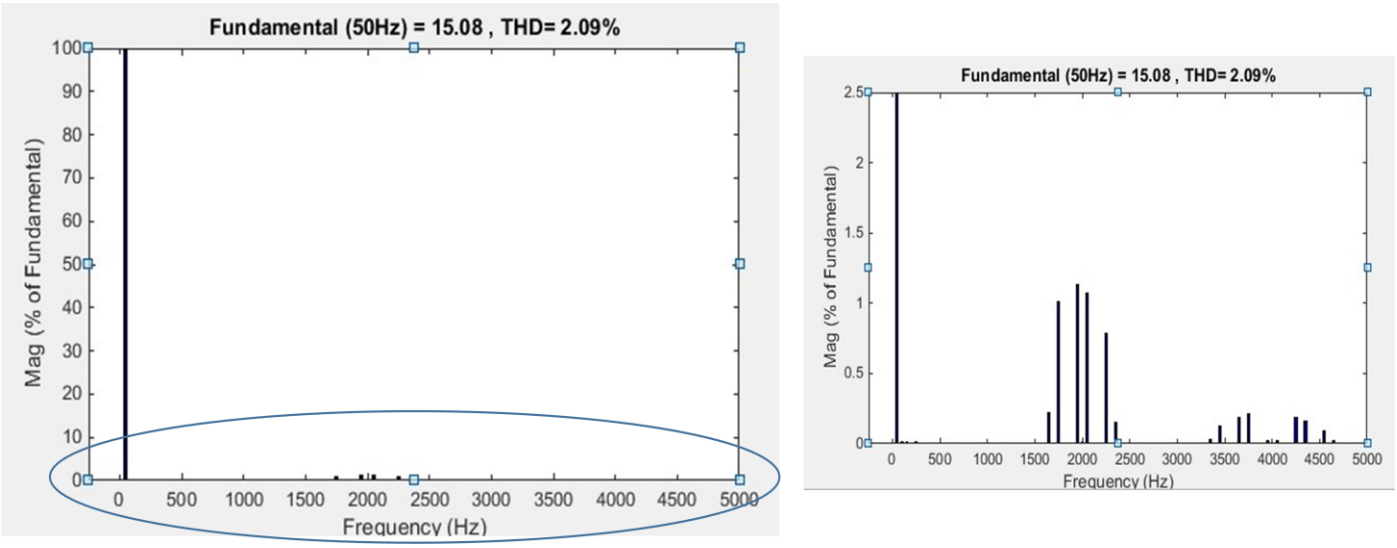


Figure 5.7 FFT analysis of phase current

5.2 Three Phase Load testing of in-Phase Opposition Disposition PWM scheme

Line Voltage V_{ab}

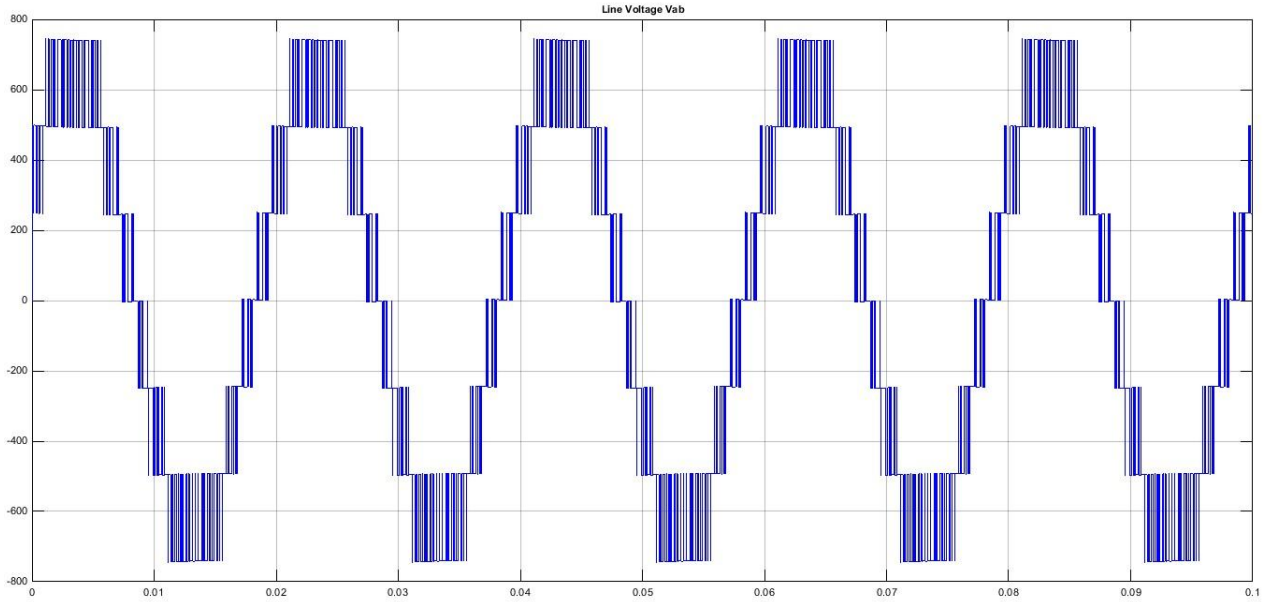


Figure 5.8 Line voltage for in-PD PWM scheme,fm = 50 Hz, mf = 40 and ma = 0.8

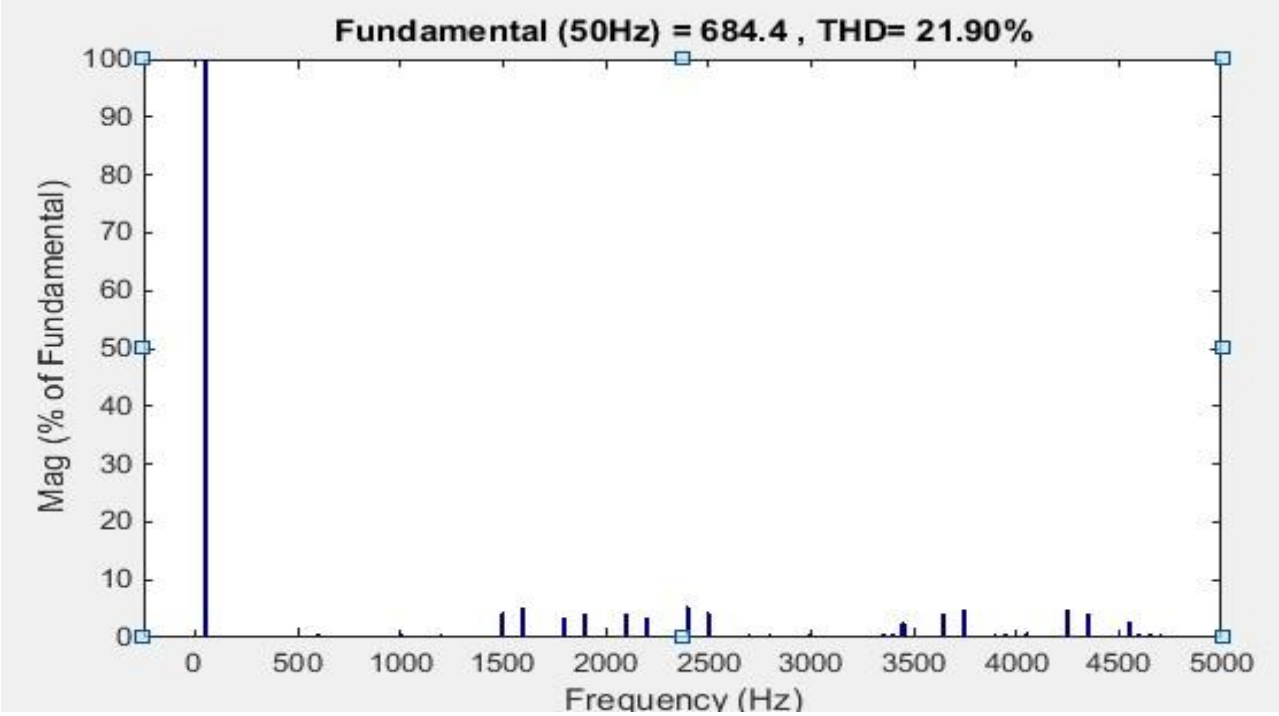


Figure 5.9 FFT analysis of line voltage

Phase Voltage V_a

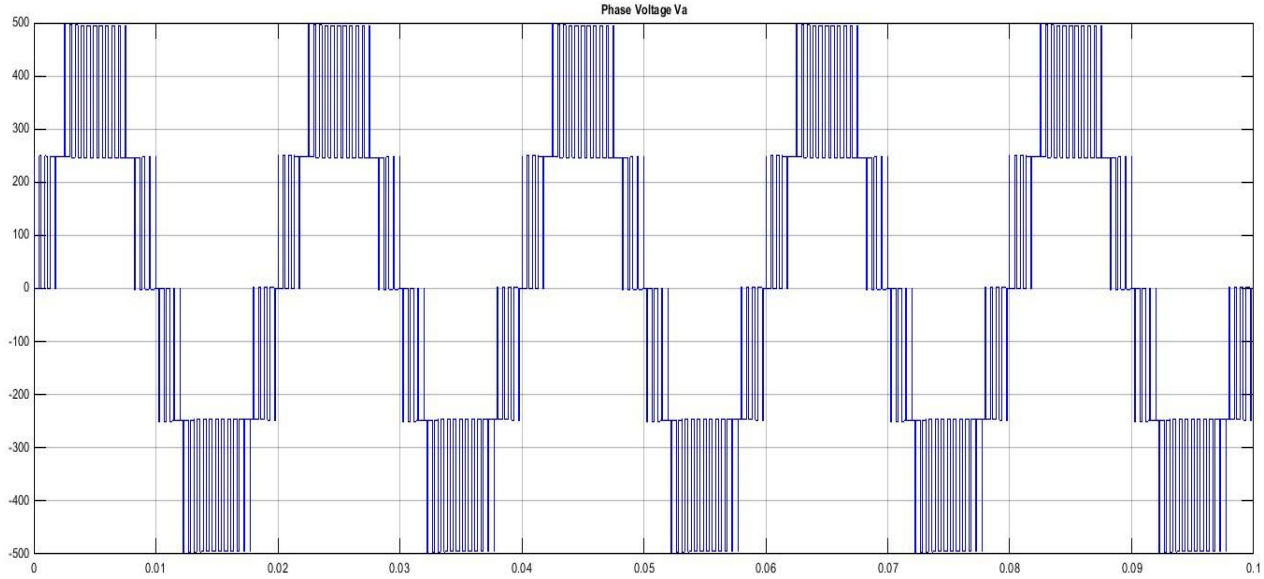


Figure 5.10 Phase voltage for in-PD PWM scheme, , fm = 50 Hz, mf = 40 and ma = 0.8

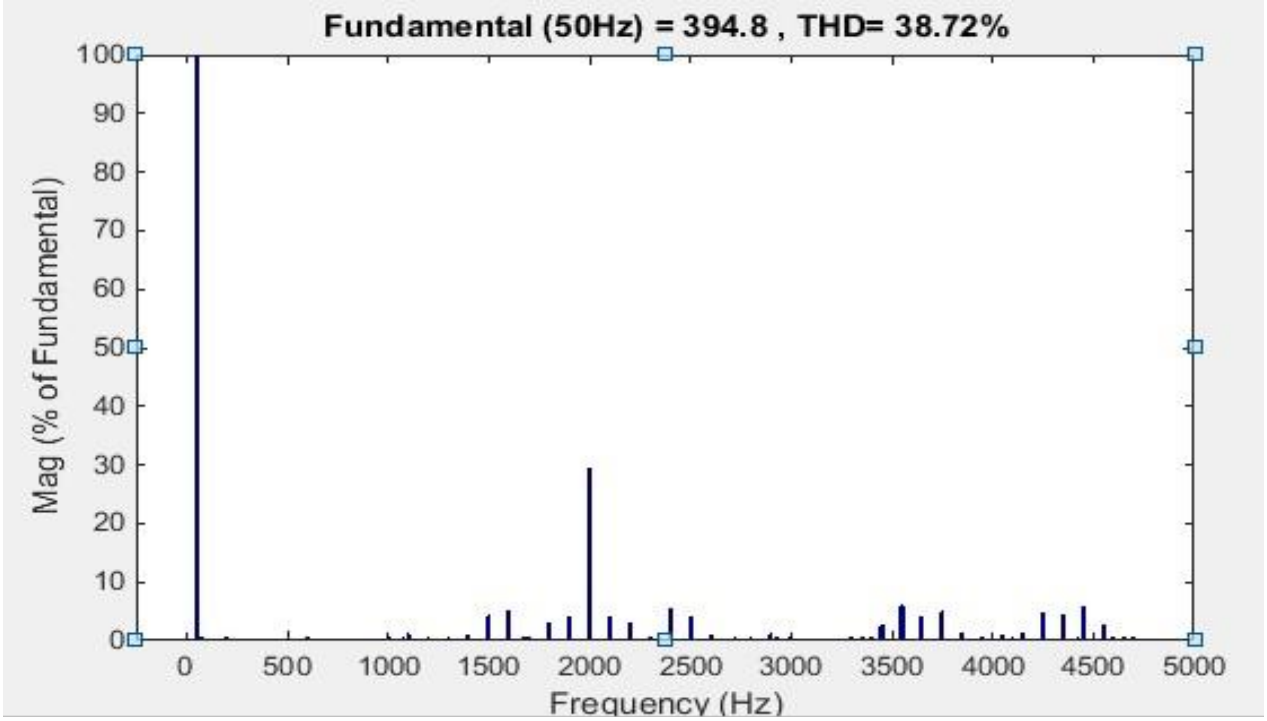


Figure 5.11 FFT analysis of Phase Voltage

Phase current Ia

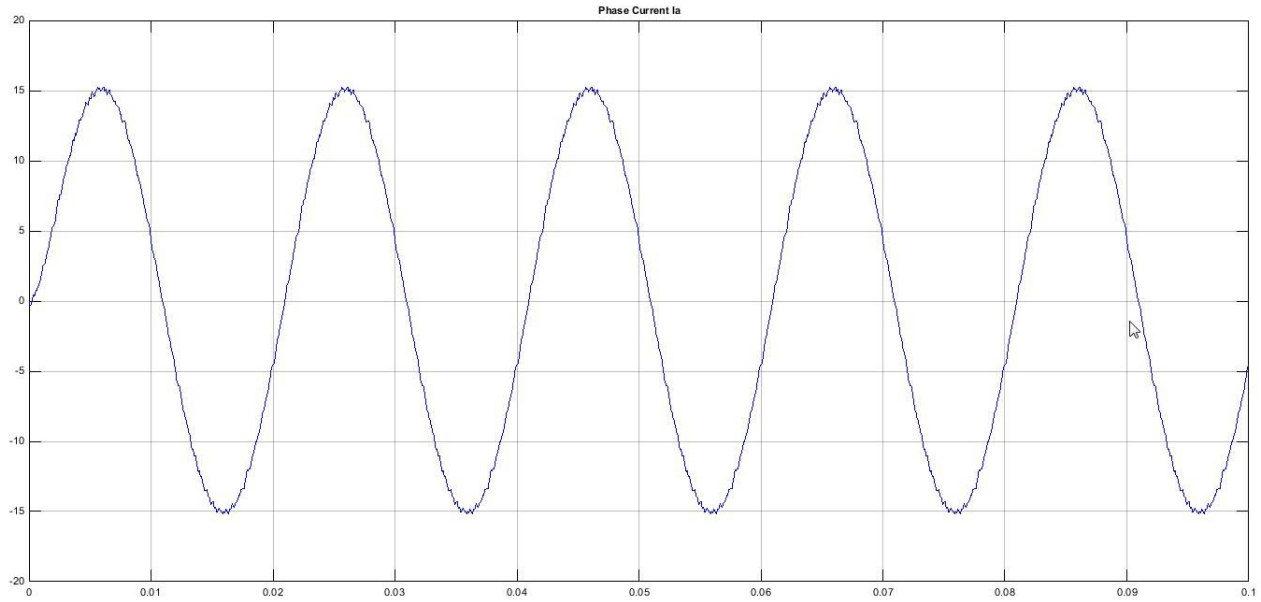


Figure 5.12 Phase current for in-PD PWM scheme, , fm = 50 Hz, mf = 40 and ma = 0.8

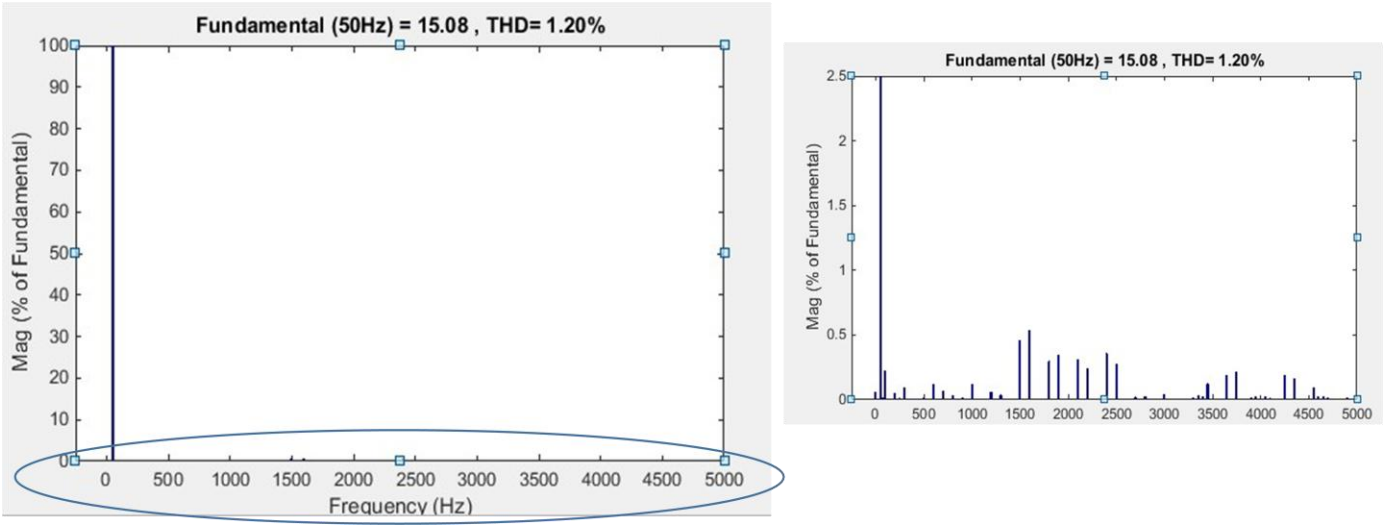


Figure 5.13 FFT analysis of phase current

5.3 Three Phase Load testing of Phase Opposition Disposition PWM scheme

Line Voltage V_{ab}

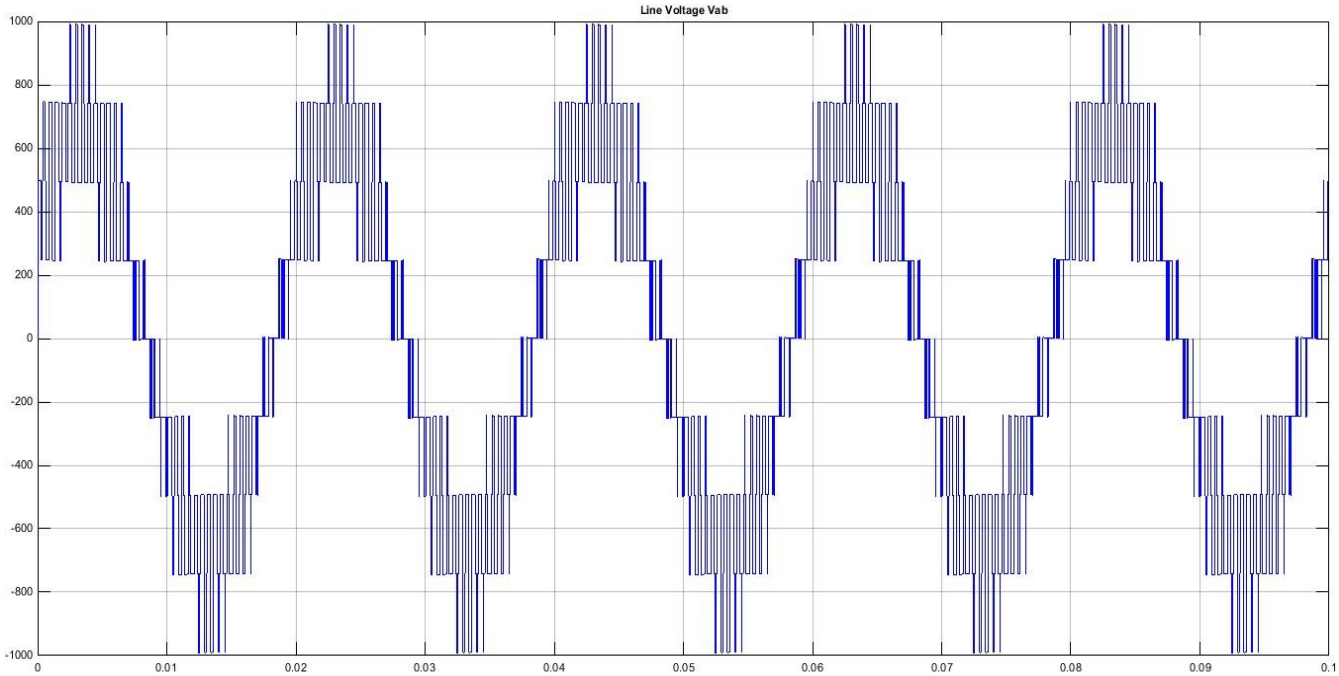


Figure 5.14 Line voltage for PODPWM scheme, fm = 50 Hz, mf = 40 and ma = 0.8

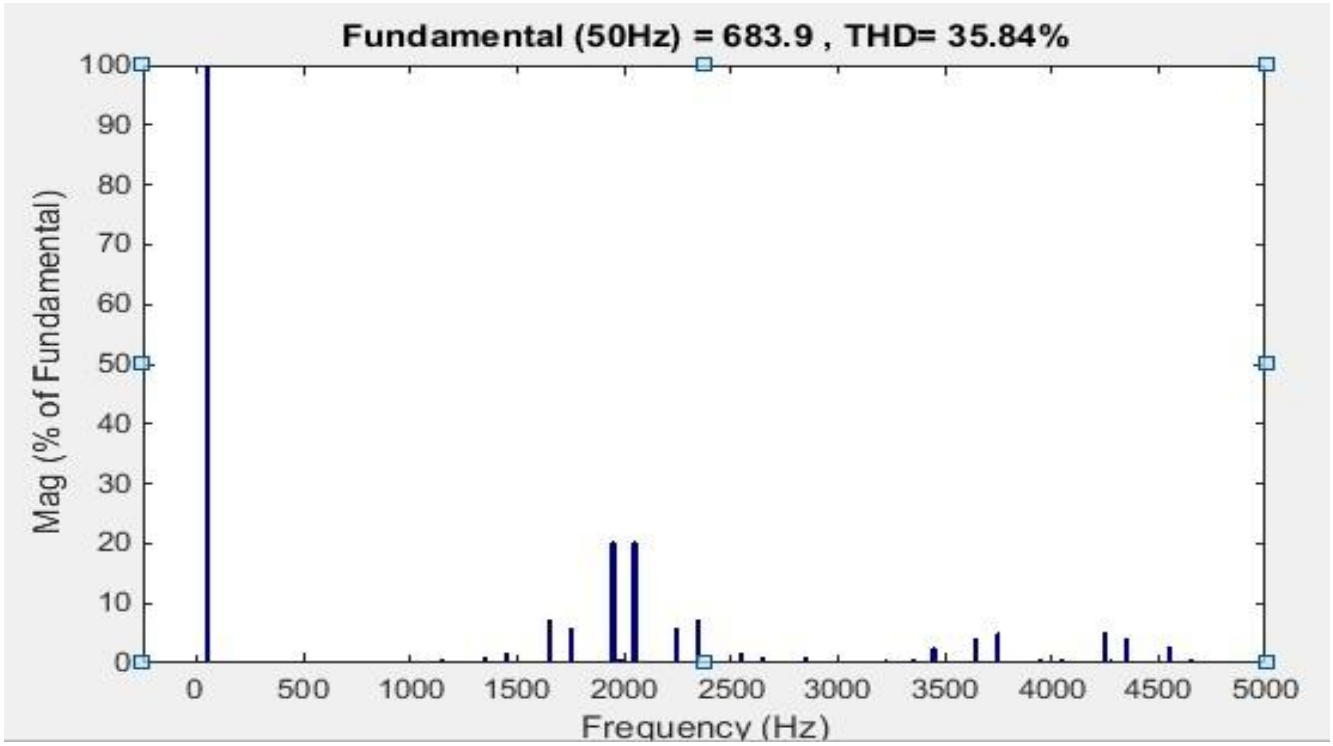


Figure 5.15 FFT analysis of line voltage

Phase Voltage V_a

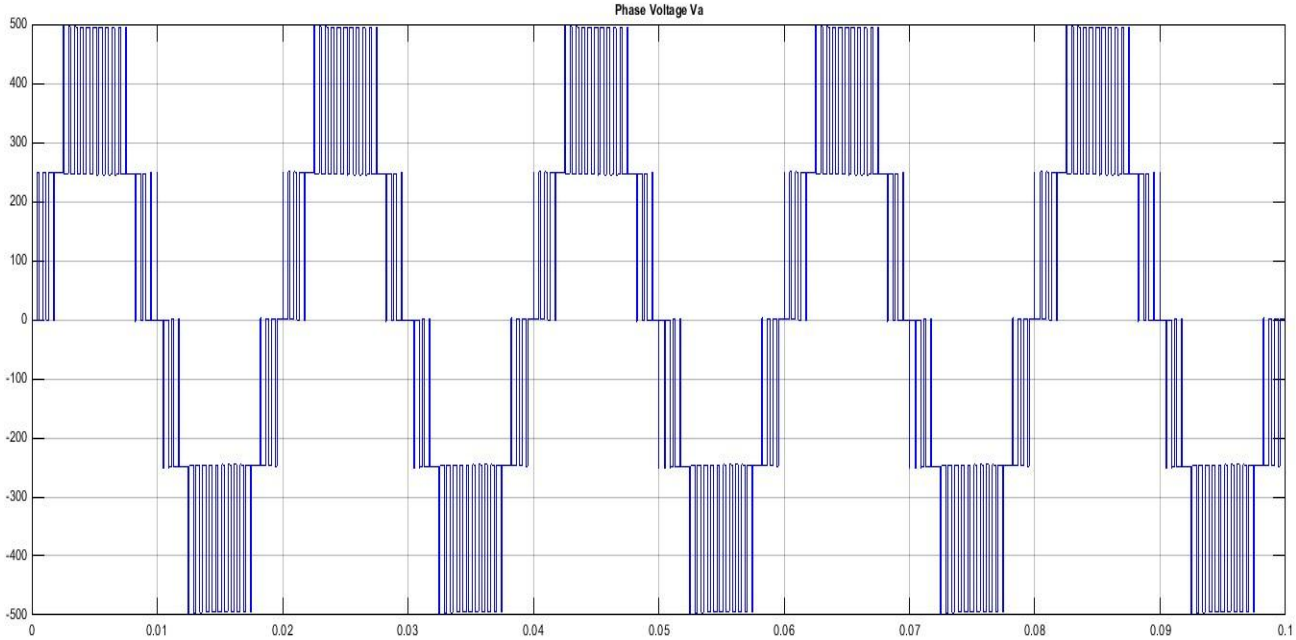


Figure 5.16 Phase voltage for PODPWM scheme, fm = 50 Hz, mf = 40 and ma = 0.8

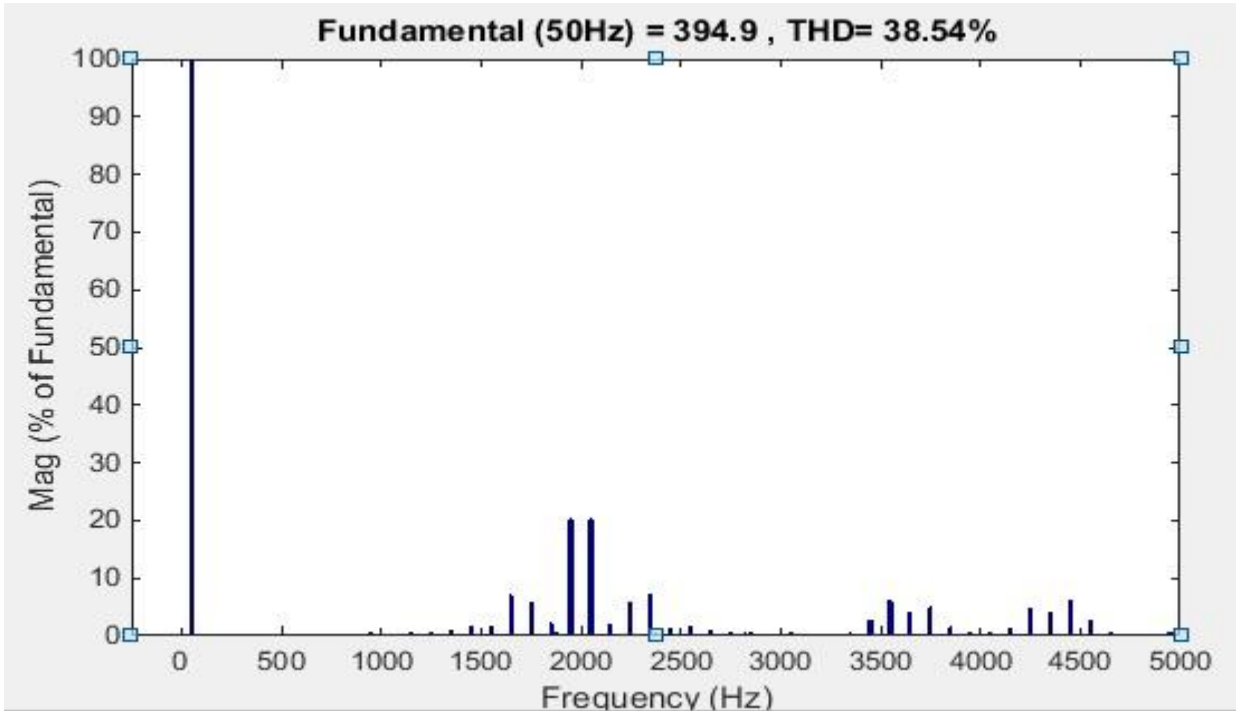


Figure 5.17 FFT analysis of phase voltage

Phase Current I_a

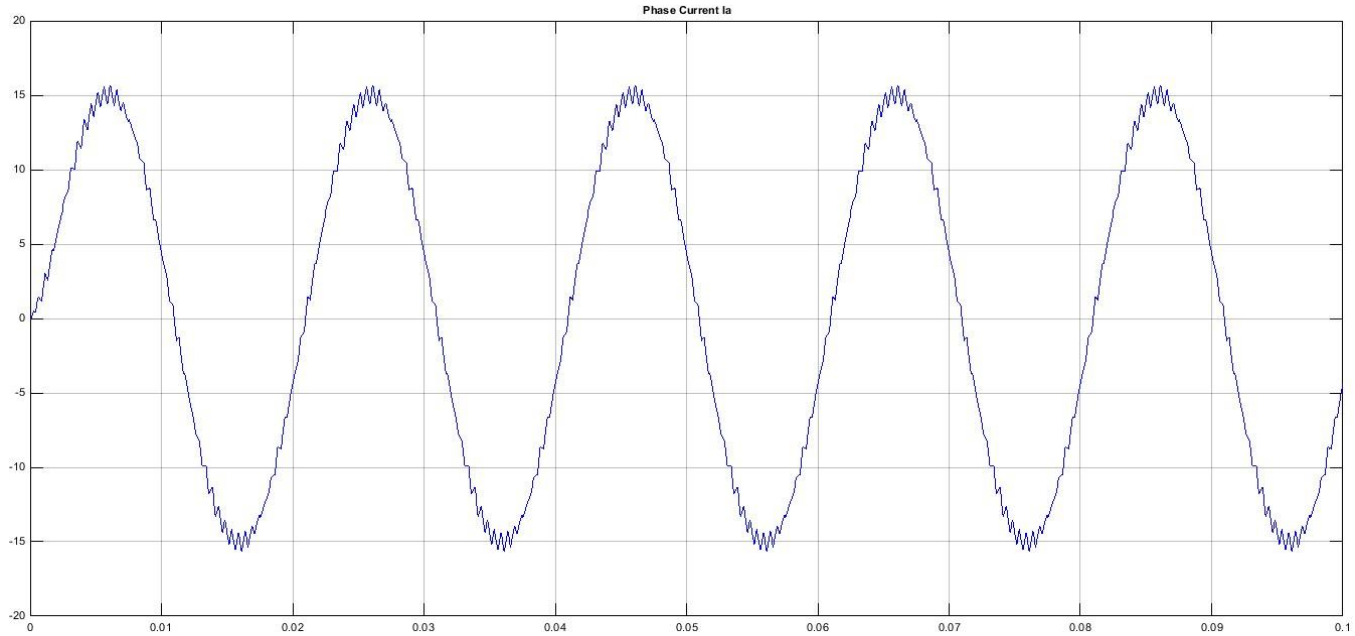


Figure 5.18 Phase current for PODPWM scheme, fm = 50 Hz, mf = 40 and ma = 0.8

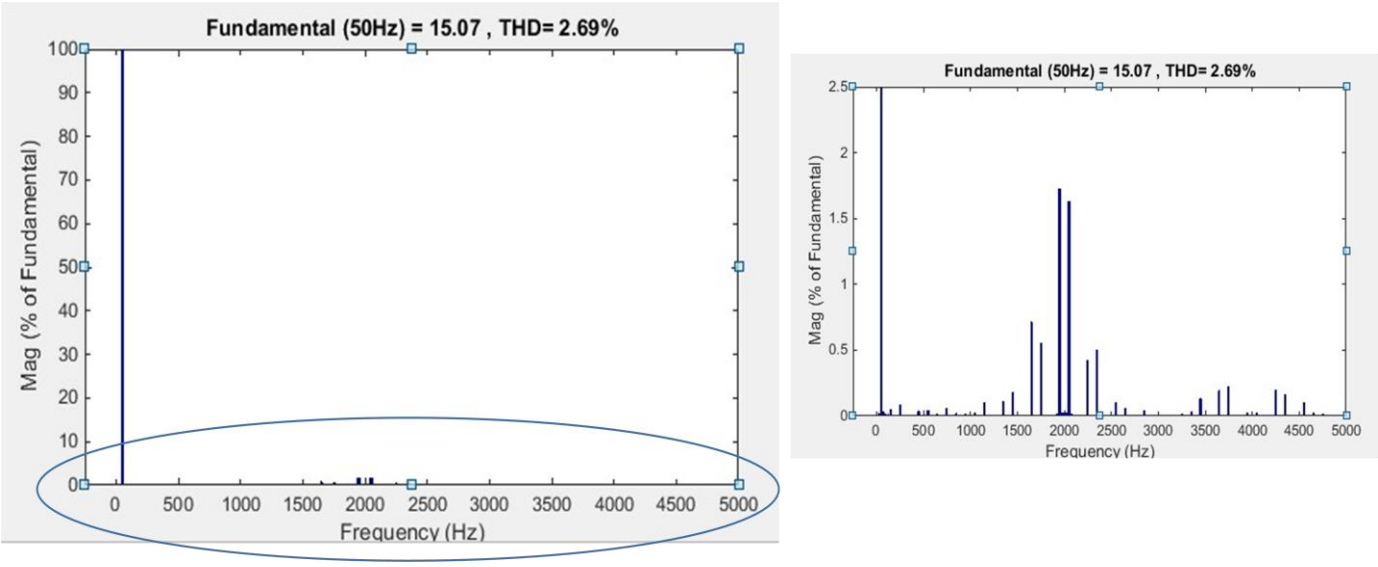


Figure 5.19 FFT analysis of phase current

5.4 Three Phase Load testing of Alternate Phase Opposition Disposition PWM scheme

Line Voltage V_{ab}

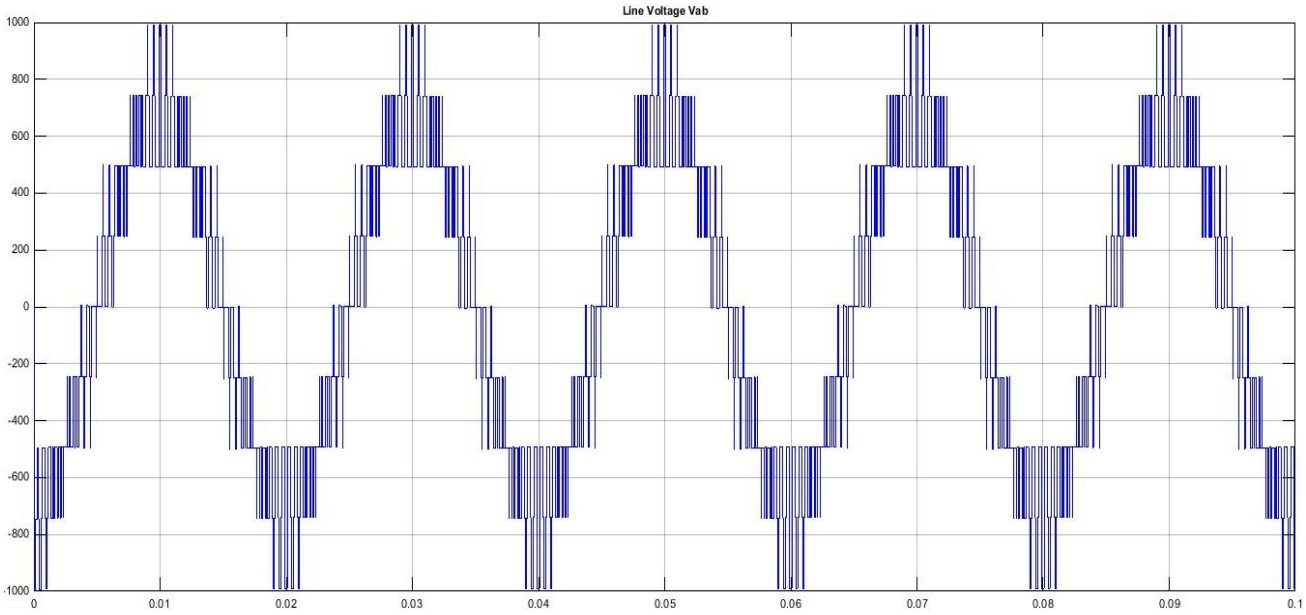


Figure 5.20 Line voltage for APODPWM scheme, fm = 50 Hz, mf = 40 and ma = 0.8

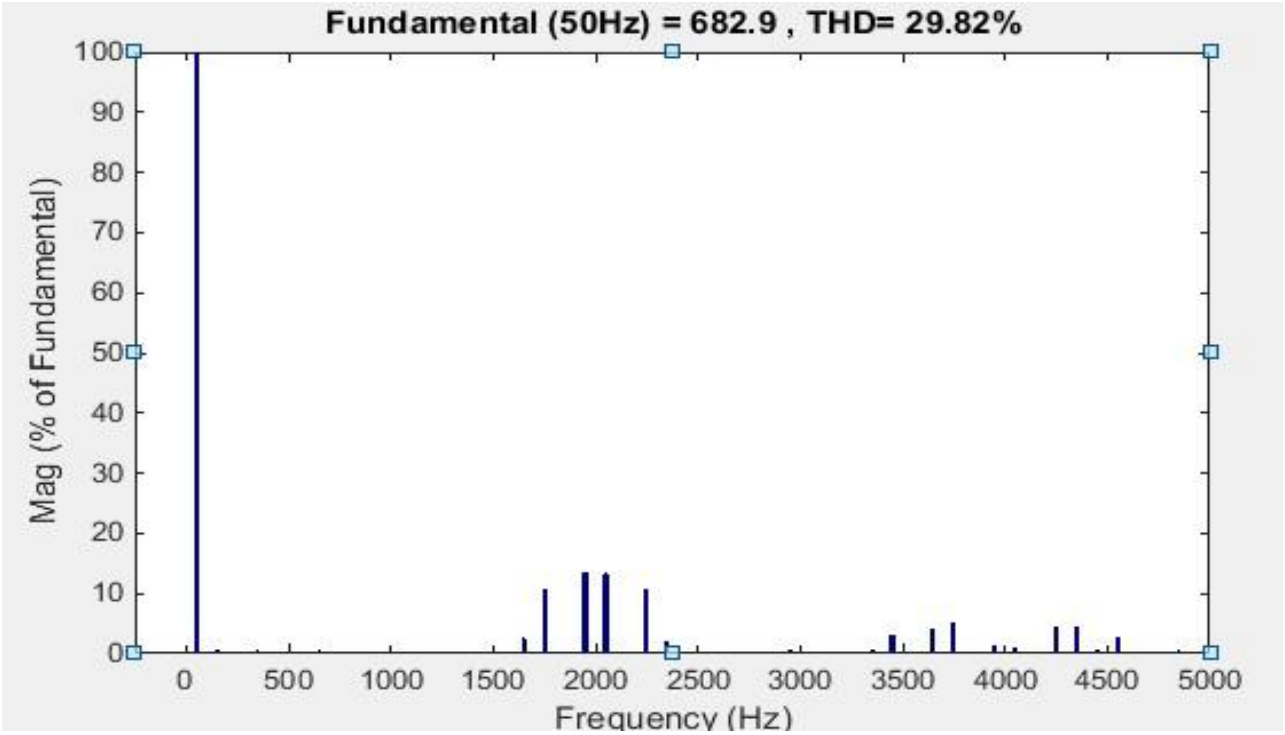


Figure 5.21 FFT analysis of line voltage

Phase Voltage V_a

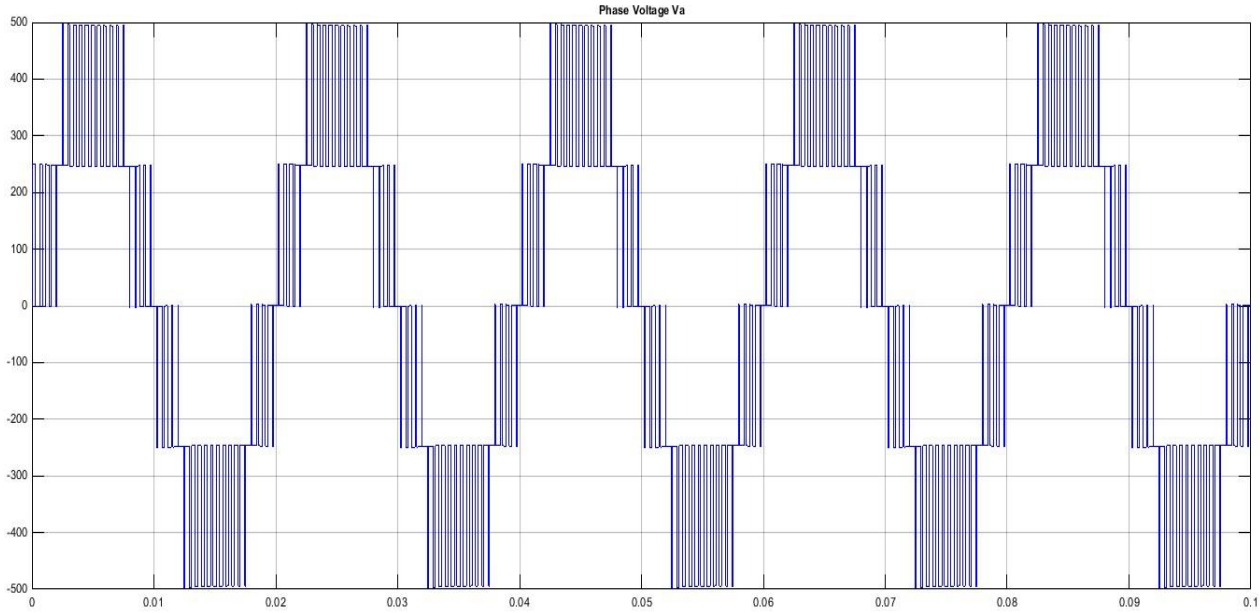


Figure 5.22 Phase voltage for APODPWM scheme, fm = 50 Hz, mf = 40 and ma = 0.8

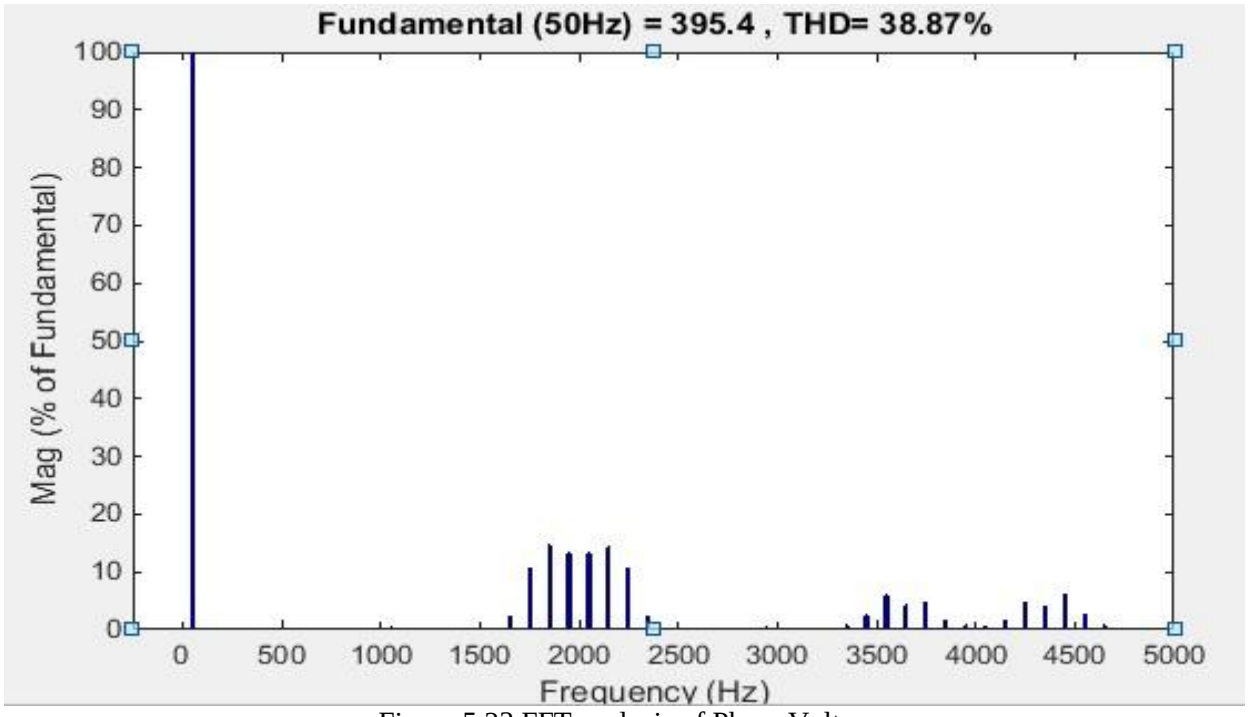


Figure 5.23 FFT analysis of Phase Voltage

Phase Current I_a

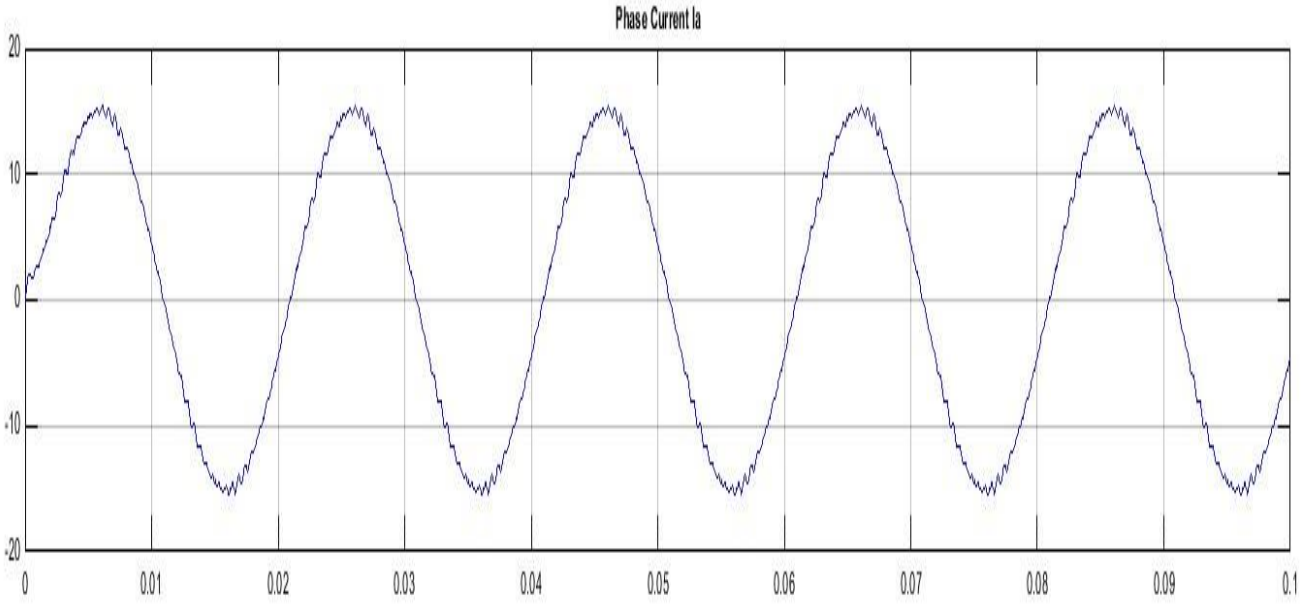


Figure 5.24 Phase current for APODPWM scheme, fm = 50 Hz, mf = 40 and ma = 0.8

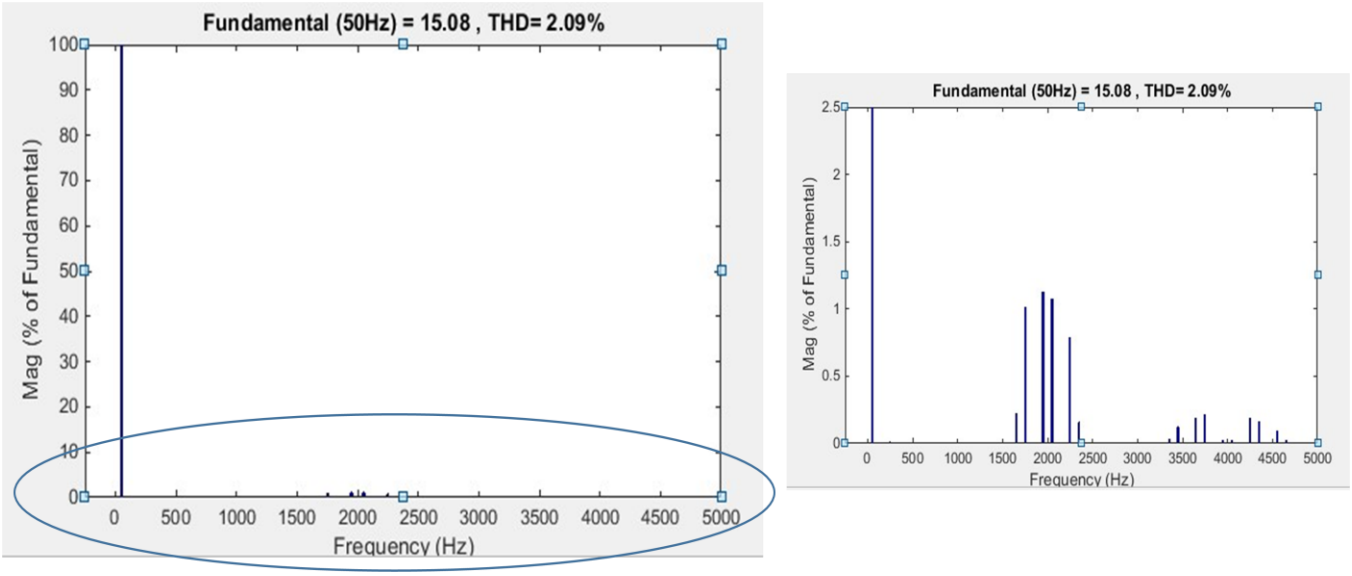


Figure 5.25 FFT analysis of phase current

5.5 Three Phase Load testing of Variable frequency PWM scheme

Line Voltage V_{ab}

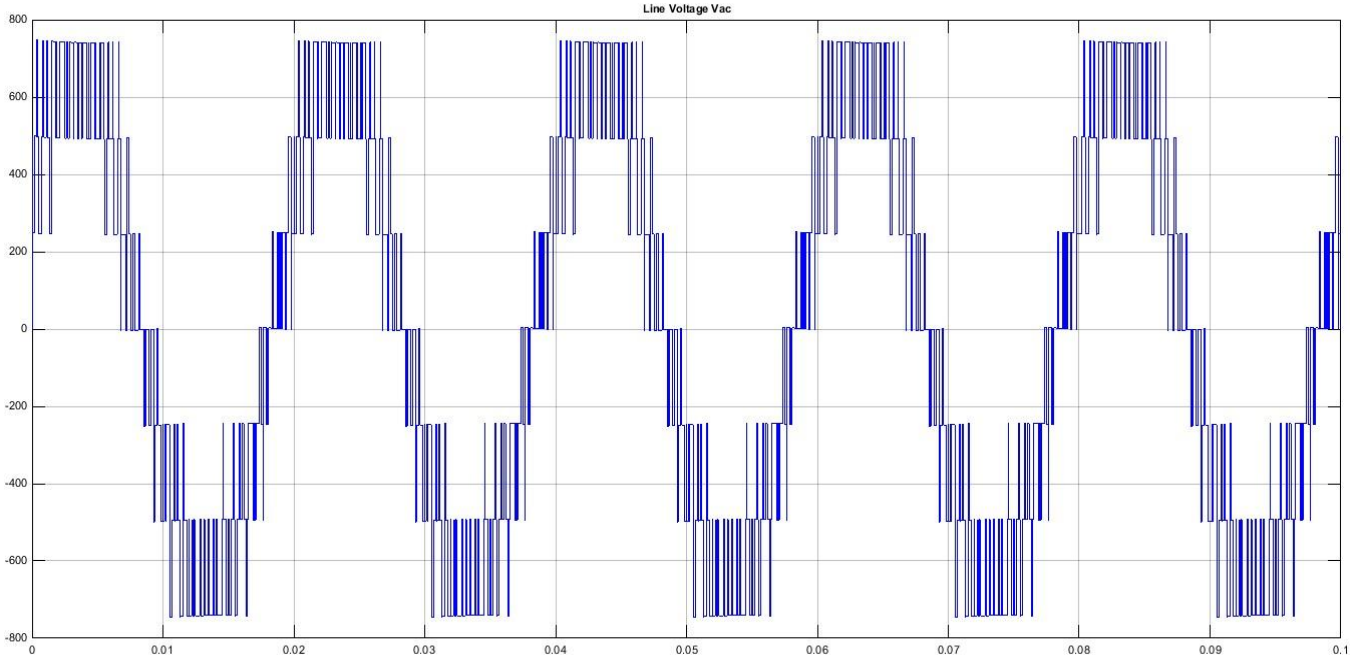


Figure 5.26 Line voltage for variable frequency scheme, fm = 50 Hz, fcr = 1.5 & 2.5kHz and ma = 0.8

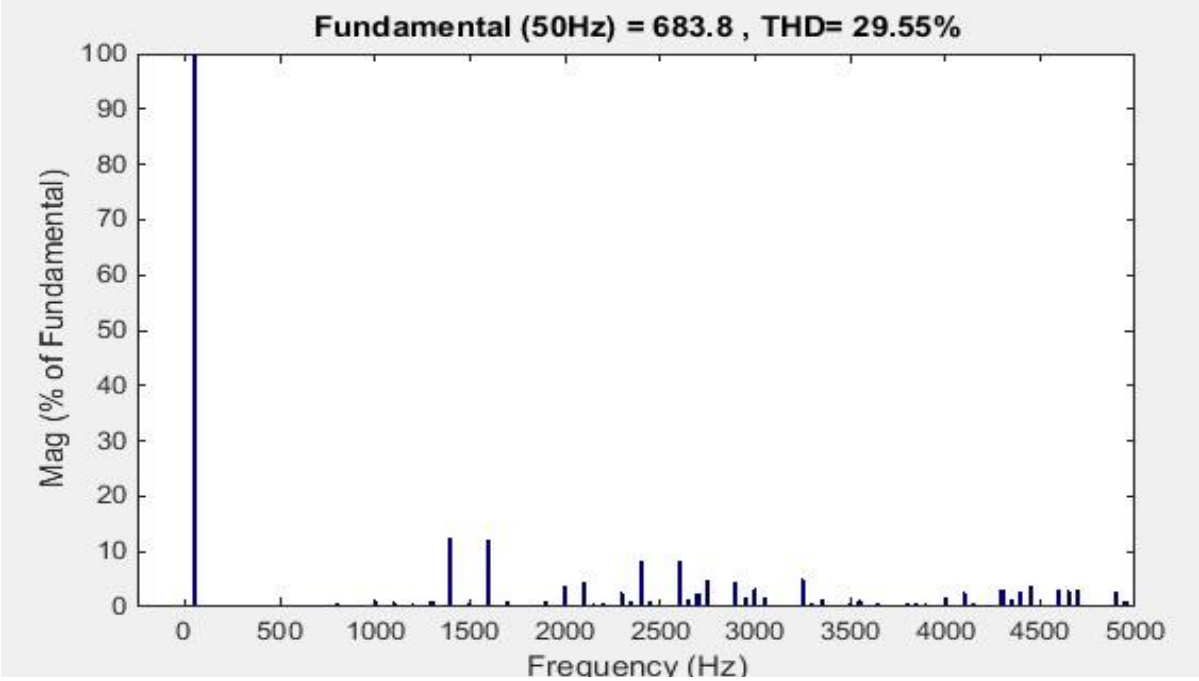


Figure 5.27 FFT analysis of line voltage

Phase Voltage V_a

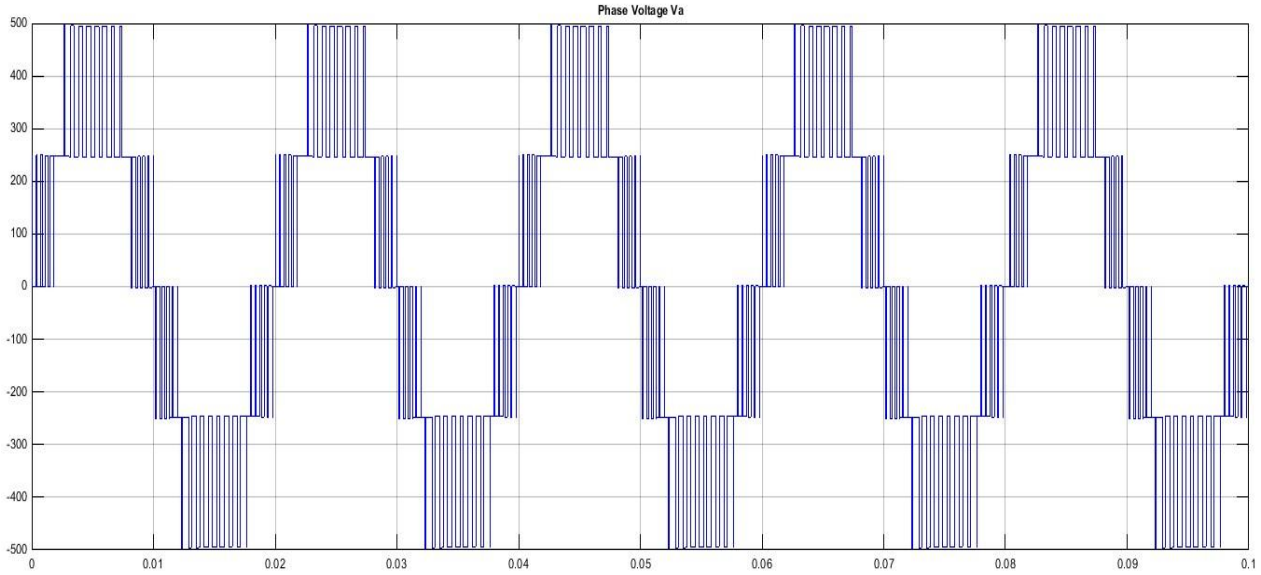


Figure 5.28 Phase voltage for variable frequency scheme, fm = 50 Hz, fcr = 1.5 & 2.5kHz and ma = 0.8

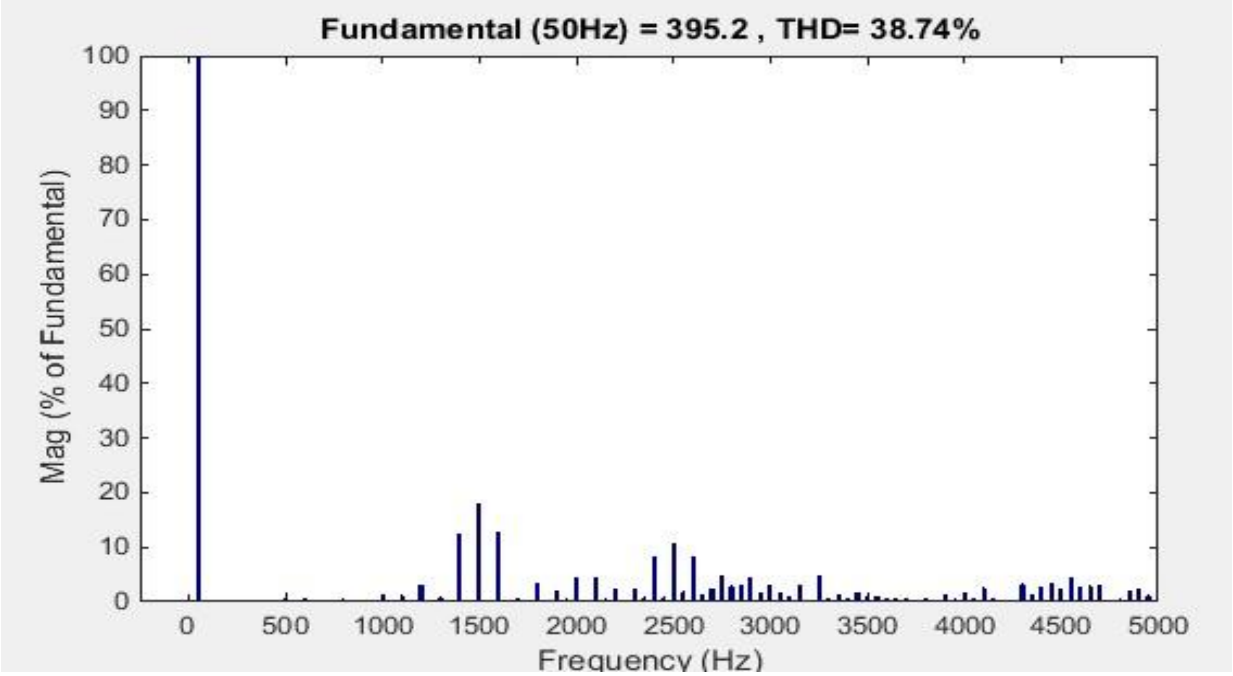


Figure 5.29 FFT analysis of phase voltage

Phase Current I_a

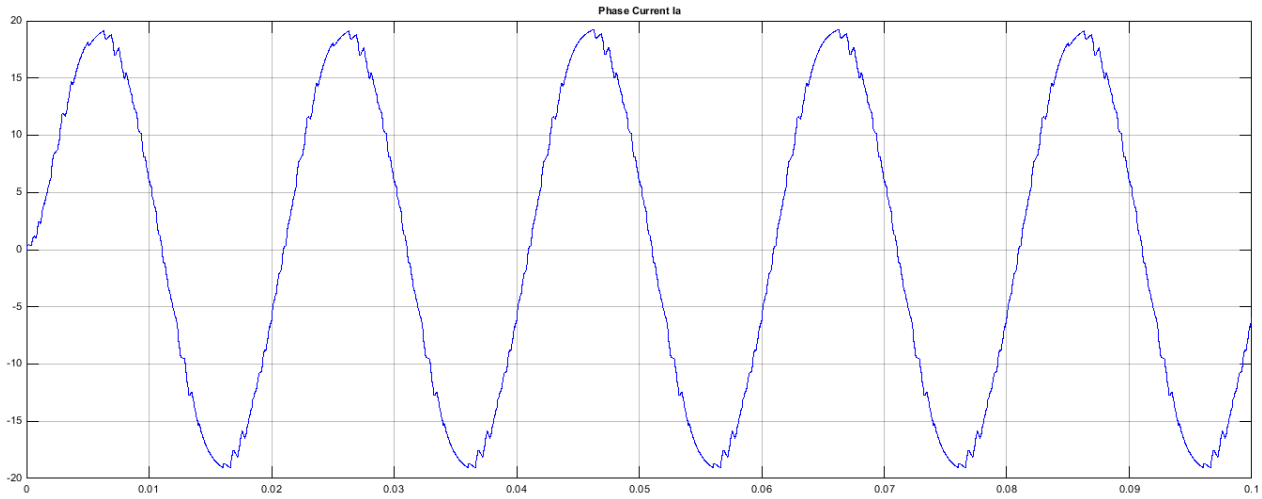
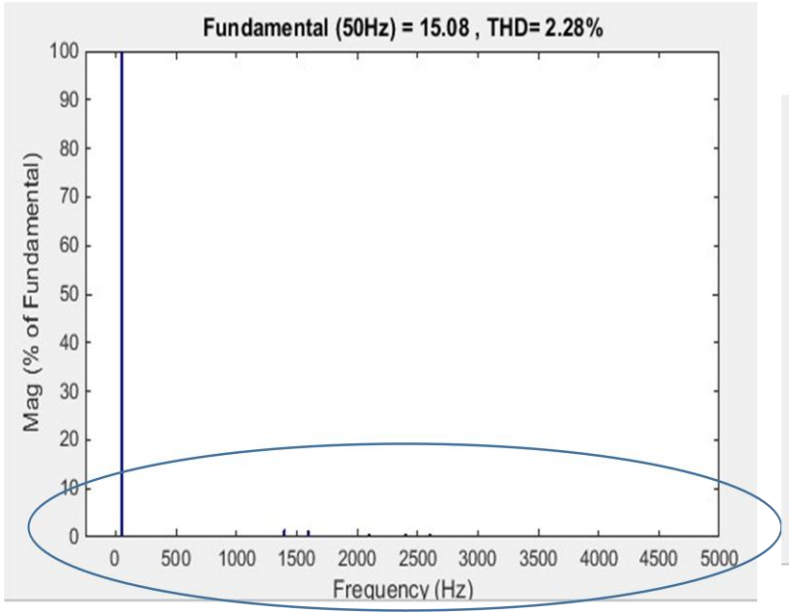


Figure 5.30 Phase current for variable frequency scheme, fm = 50 Hz, fcr = 1.5&2.5kHz and ma = 0.8



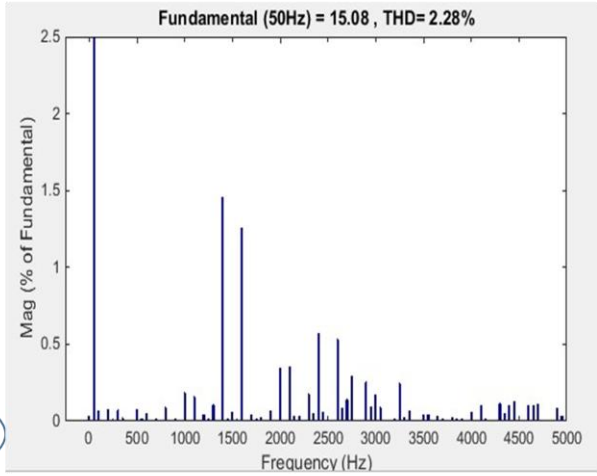


Figure 5.31 FFT analysis of Phase Current

5.6 Three Phase Load testing of Space Vector PWM scheme

Line Voltage V_{ab}

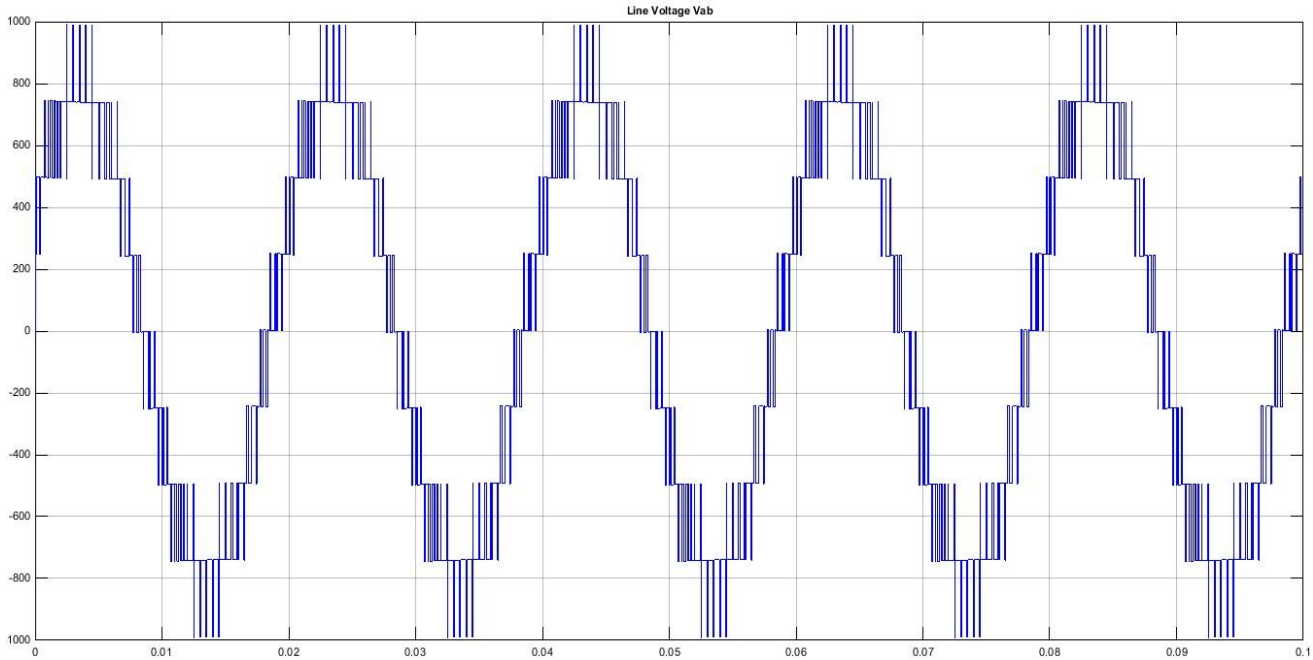


Figure 5.32 Line voltage for space vector scheme, switching frequency= 2kHz and ma = 0.8

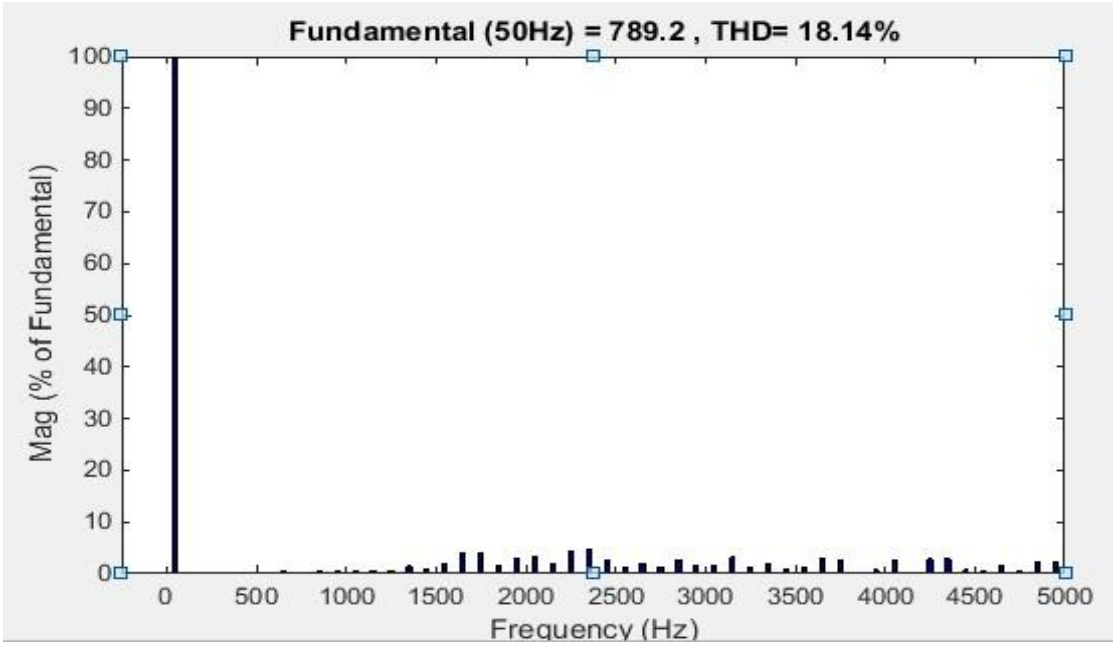


Figure 5.33 FFT analysis of line voltage

Phase Voltage V_a

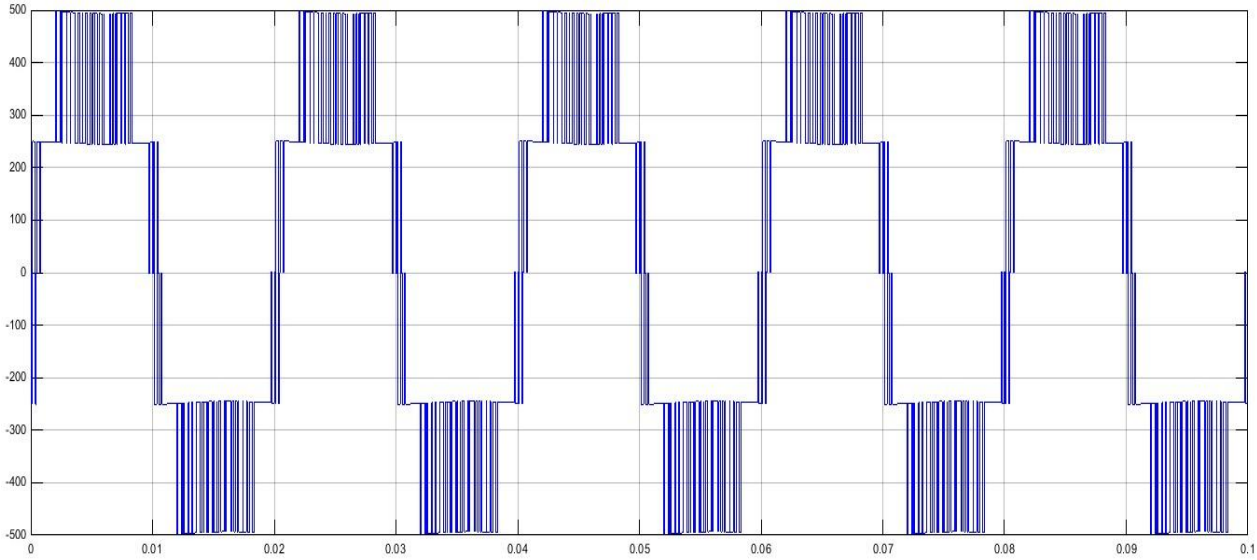


Figure 5.34 Phase voltage for space vector scheme, switching frequency= 2kHz and ma = 0.8

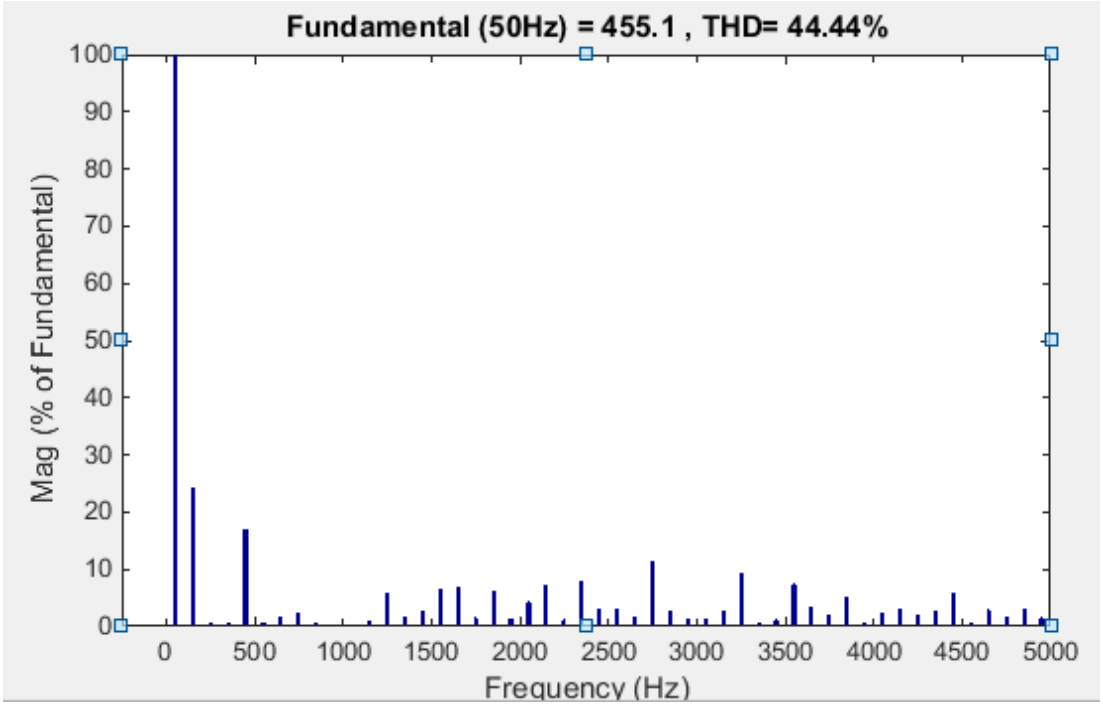


Figure 5.35 FFT analysis of phase voltage

Phase Current I_a

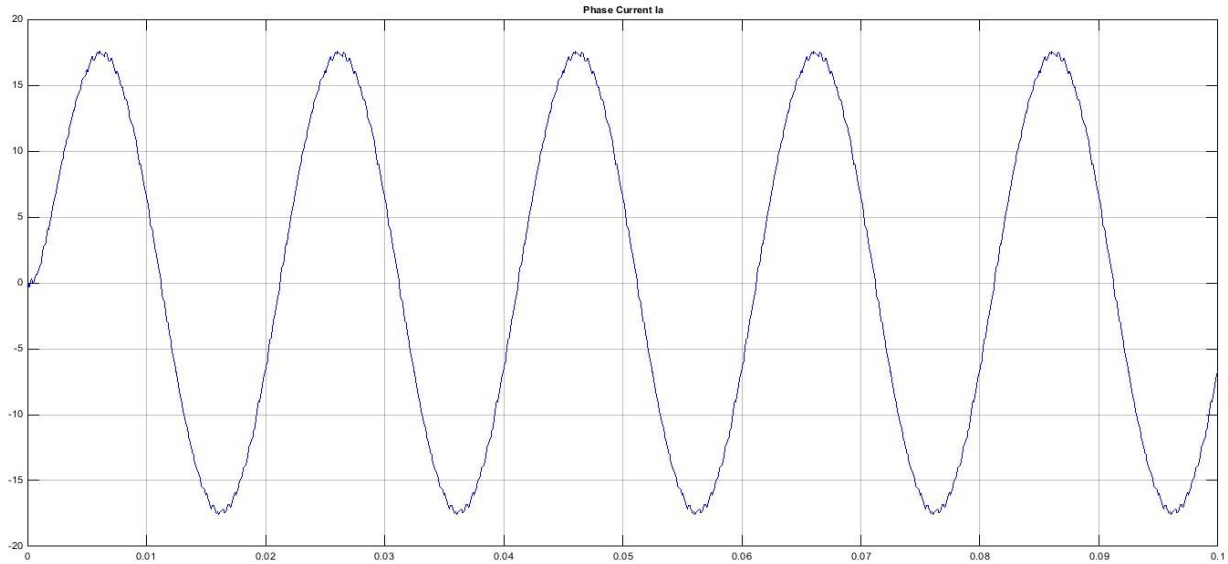


Figure 5.36 Phase current for space vector scheme, switching frequency= 2kHz and ma = 0.8

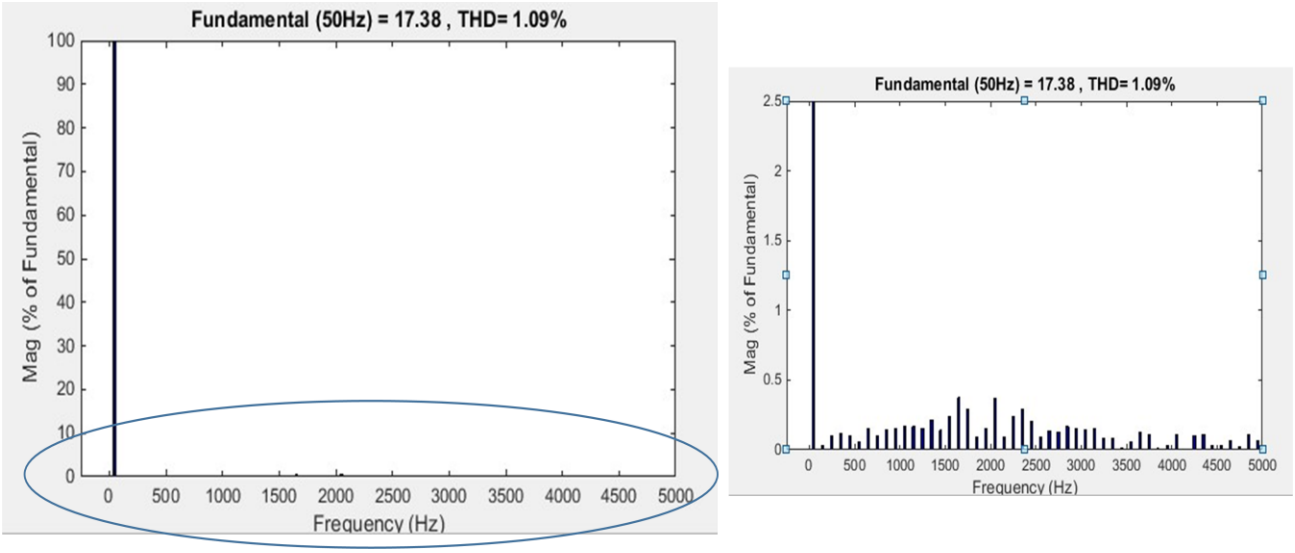


Figure 5.37 FFT analysis of Phase current

5.6 Tabulation of results for RL load testing

	In- PD	**POD**	**APOD**	**Variable Frequency**	**Phase-shifted**	**Space Vector**
THD_V	21.80%	35.84%	29.82%	29.55%	29.85%	18.14%
Fundamental Line Voltage(V_{rms})	483.94	483.59	482.88	483.52	484.65	558.05
Line Voltage Ripple(%)	23.55%	36.89%	31.10%	32.37%	31.05%	21.36%
THD_I	1.20%	2.69%	2.09%	2.28%	2.09%	1.09%
Fundamental Current(A)	10.66	10.66	10.66	10.66	10.66	12.29
Current Ripple(A)	negligible	negligible	negligible	negligible	negligible	negligible
Input power(W)	2882	2884	2884	2885	2884	3830
Output Power(W)	2612	2611	2612	2614	2612	3775
Efficiency	90.63%	90.53%	90.57%	90.60%	90.57%	98.56%

CHAPTER 6 HARDWARE DEVELOPMENT AND IMPLEMENTATION

6.1 Introduction

This chapter involves hardware development and implementation of five level H-bridge cascaded multilevel inverter and various circuits used in its implementation. A digital Signal Controller has been used to generate the firing pulses. Among so many device, MOSFET has been chosen due to its cheaper cost in low-power application, and due to presence of inbuilt anti parallel diode. For each of the six switches implemented, a high voltage and dv/dt protection has been implemented along with the gate driver circuit which amplifies as well as isolates the firing pulses. The block diagram of complete experimental setup is indicated below. Also wires carrying high frequency current are kept away from the wires carrying low frequency currents, so as to reduce the electromagnetic interference (which leads to distortion in the sensed low frequency analog signals).

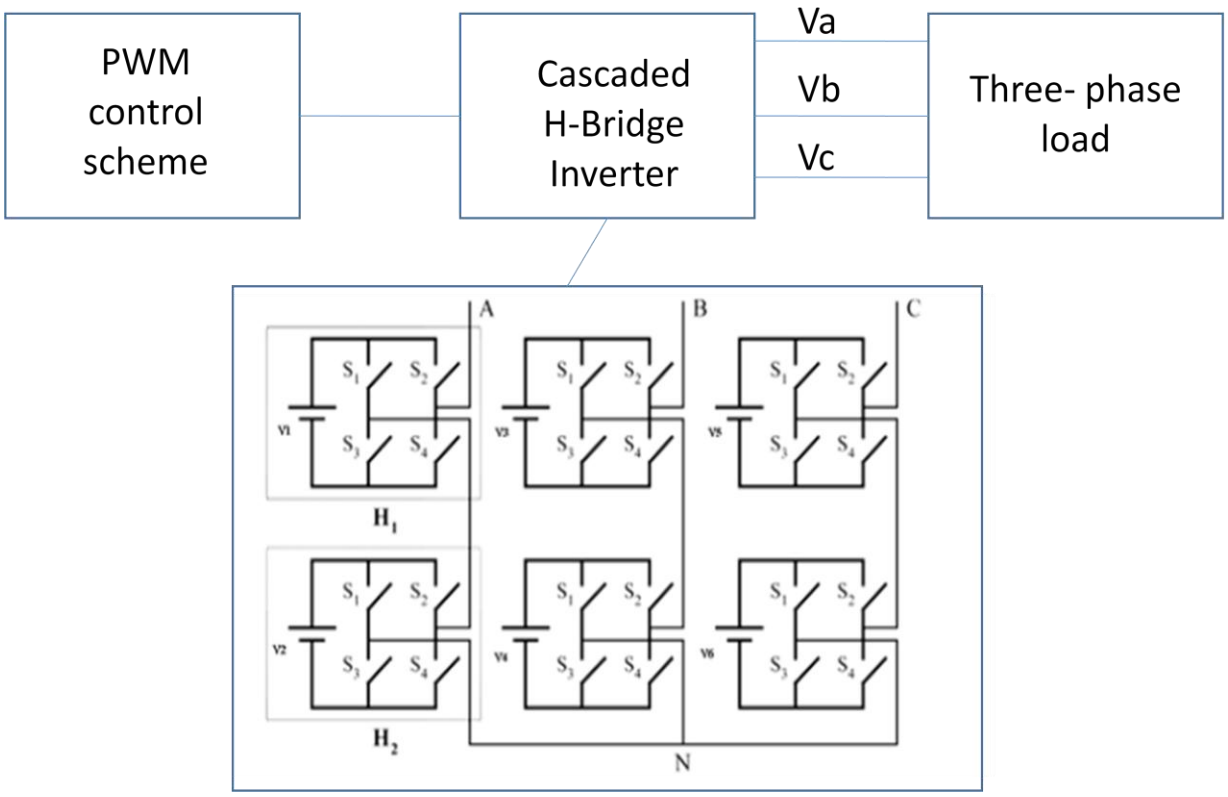


Figure 6.1 Block diagram of the implemented lab-setup

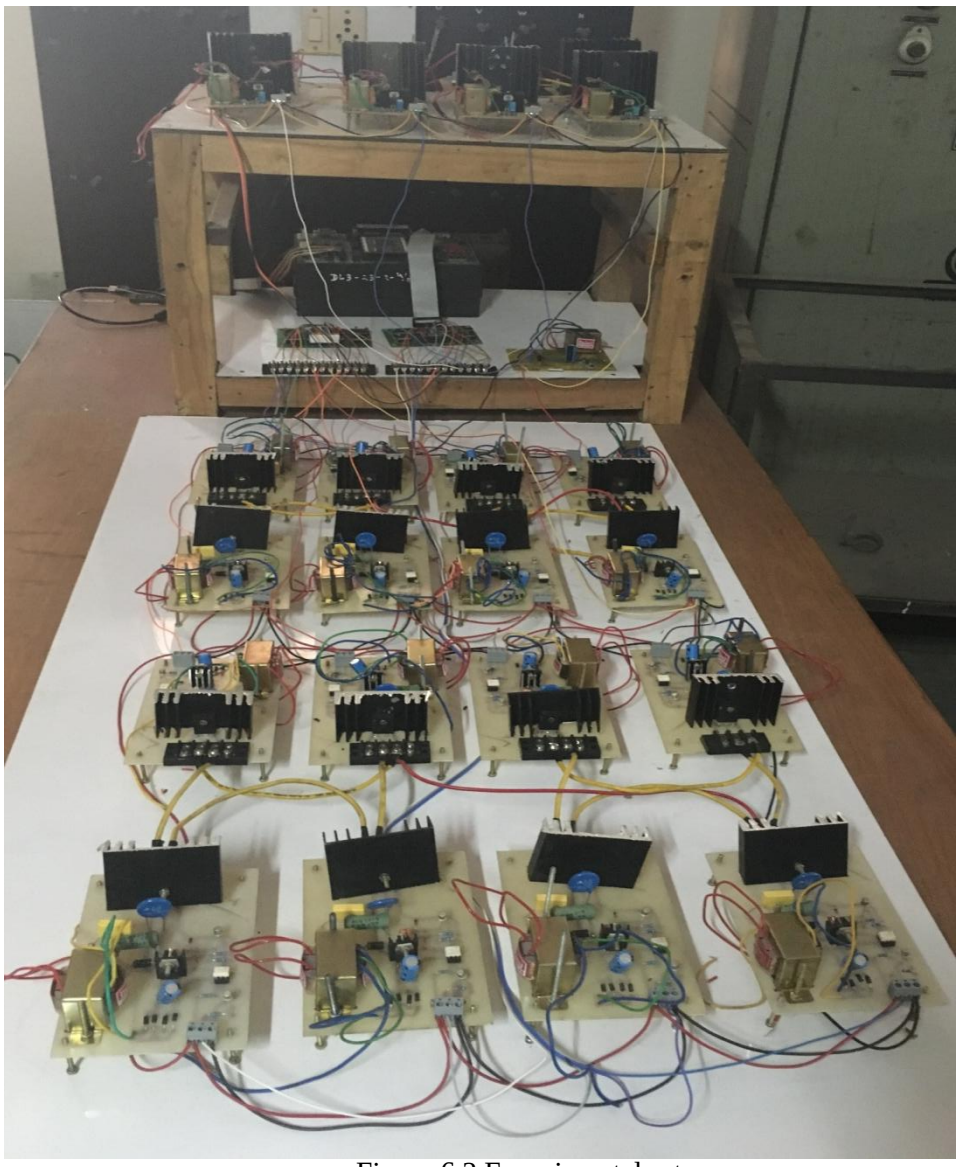


Figure 6.2 Experimental setup

6.2 Switch setup- Gate Isolation, Amplification and protection

An IRFP460 MOSFET (Metal Oxide Semiconductor Field Effect Transistor) has been used as a switch due to its cheaper cost and has an inbuilt anti parallel diode. Though the current rating of the MOSFET is 20A, the usage of the system has been limited to 5A alone.

The following circuit was used for all 24 switching units for five level inverter

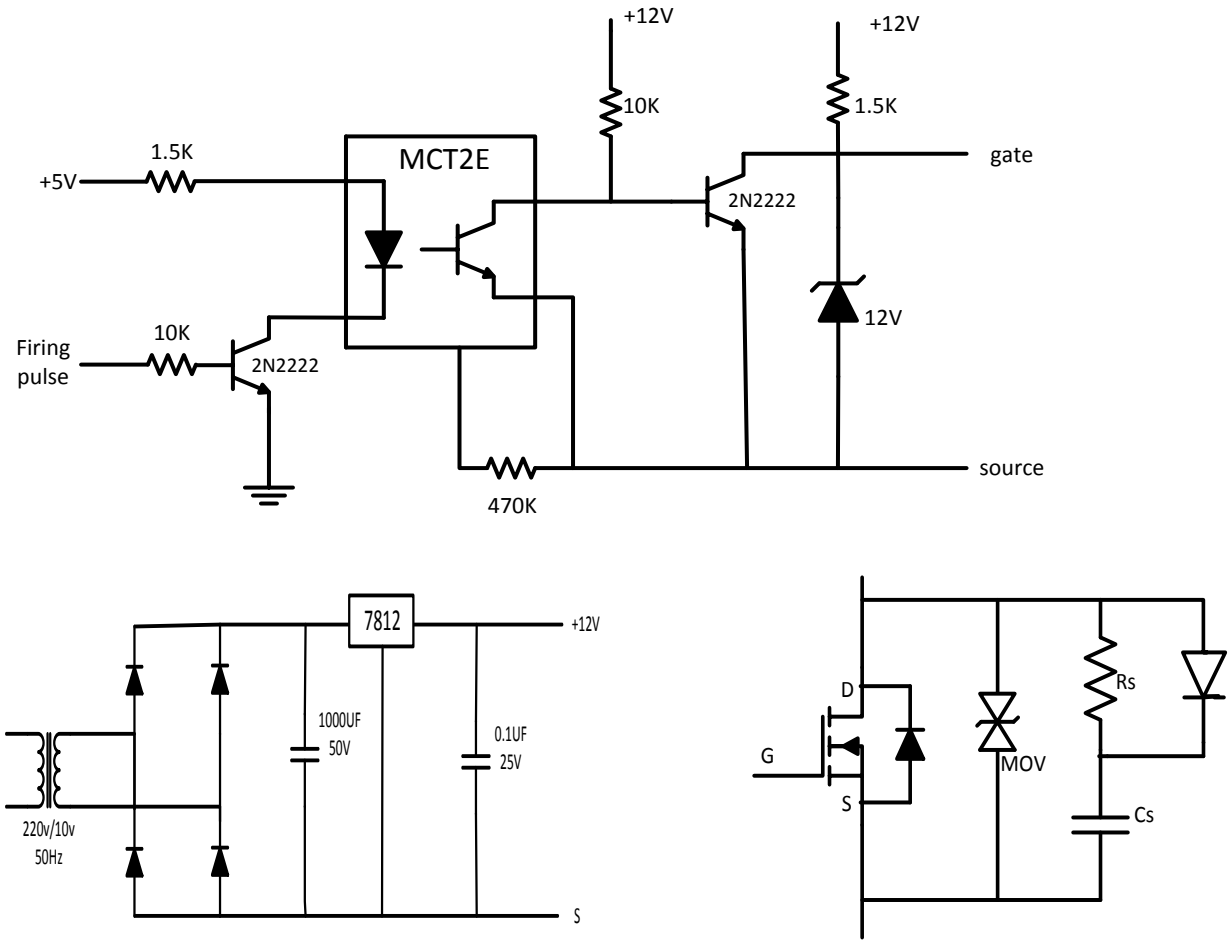


Figure 6.3 Circuit diagram for each switch unit (driver circuit, power supply and snubber circuit)

5V switching pulses are obtained from each switch from the deadband circuit which are isolated with the help of MCT2E optocoupler and then amplified to get 12 volt pulses between the Gate and the Source of the MOSFET. When the photodiode of the optocoupler is ON, the light from it falls on the phototransistor driving it into the saturation region. The +12V needed by firing circuit is locally generated at each switch using a 220/18V transformer and 7812 regulated IC along with rectification circuit and capacitors.

The Gate to Source charge is typically 29nF for above mentioned MOSFET. Hence the resistance between the Gate and +12V supply plays an important role in the shape of the firing pulse. The decrease in collector resistance leads to decrease in rise time , but increase in fall time. Increase in

fall time is because for a particular base current of transistor, collector current gets fixed, and this collector current comprises of two currents i.e one due to discharge of collector-emitter capacitor and another due to potential difference acrosscollector resistance. If the resistance value is low more current is provided by 12V source through resistor to collector, and due to which lesser current is drawn from the capacitor ultimately leading to slow discharge of capacitor, finally more time to get from 12V to 0V.

Figure 6.4 Switch unit of inverter

When the transistor adjacent to zener enters cut-off region, the voltage across the zener becomes +12 and hence the capacitor between the gate and the source has to change through the resistor. Greater the resistance between gate and +12V source, the circuit becomes obsolete for faster switching operations. When the same transistor enters saturation the capacitor discharges via the effective resistance between collector and emitter which is very less saturation region and hence the firing pulse at gate falls relatively rapidly. Ideally the collector resistance used for faster response but there is also a consideration of 0.6A DC as the maximum collector current of 2N2222 transistor and increased power loss.

One more point that can be observed is that output pulse has a time delay of 5us with respect to input pulse for both rise and fall operations. This is due to operational delay associated with the phototransistor and the photo diode of the optocoupler. This delay along with the gate capacitor charging and discharging is the critical factor in deciding the maximum switching frequency for converter operation.

There may be high dv/dt due to supply transients. In order to protect the circuit from this situation a snubber circuit is used along with a MOV (Metal Oxide Varistor) of 320V. The time delay associated with the charging of the snubber capacitor saves the MOSFET. Also the MOV protects the MOSFET against high voltages. The ON state MOSFET resistance is .27 ohm which is very low to protect the switches in case of a firing pulse overlap from line to line short circuit as I^2R loss is low. The snubber capacitor discharges via the snubber resistance and MOSFET when the switch is ON. The discharge current in mA is very small as compared to load current to affect the MOSFET rated at 20A. The snubber acts as an alternate path for the high currents to flow as capacitor acts as a short circuit for voltage transients.

The rated Gate-to-Source voltage of MOSFET is 20V. The 12V zener protects the switch from exceedingly large values of gate voltage. Also heat sinks have been used along with voltage regulator IC7812 and MOSFET to dissipate the heat generated by switching-operation.

6.3 Deadband circuit

The necessity of dead band circuit (deadtime commutation) has been previously discussed. A delay of 18us is generated using a Deadband circuit. 8us was the maximum fall time for gate pulses amongst all the switches. The following is implemented logic for deadtime delay. The RC charging is the cause of delay. The NOT gate considers signals below of 1.65V as active low as the VCC used is 5V(obtained from regulated power supplies) for this circuit. The point to be noted is that the pulses are delayed only at the rise time. The moment the signal becomes zero the output also becomes zero.

Values of resistor and capacitor can be chosen, by considering the charging equation of capacitor of dead band circuit.

$V_c = V_o(1 - e^{-t/RC})$

In the above equation the V_o = 3.3V because the pulses given by DSP kit is at 3.3V peak. To get the required delay for no overlap, V_c must be taken atleast 1.65V which is the minimum limit for the digital zero detection. 't' should be taken as the required dead band time delay. Deadtime delay should be at least equal to maximum fall time of switch unit. Maximum fall time of switch unit is found to be 12us. In order to get a time delay of 12us the resistance value should be atleast 1.7K (available 2K) and capacitor value of 0.01uF. In practical the delay came to be equal to 18us due to resistor value and extra capacitance NOT gate.

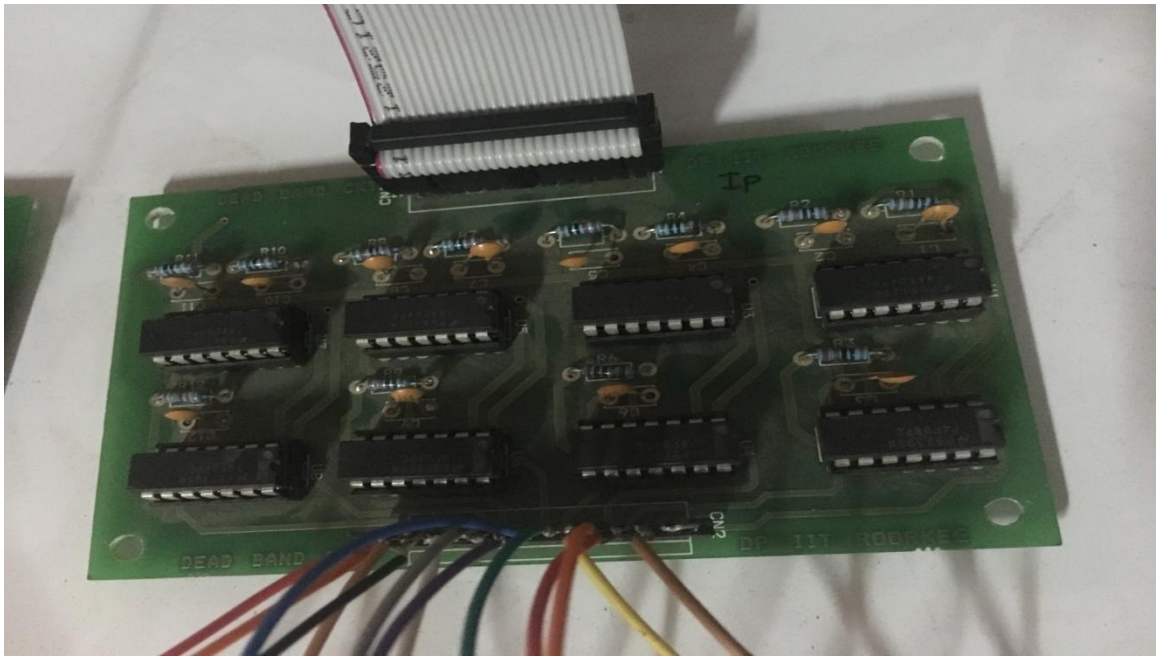


Figure 6.5 Deadband unit

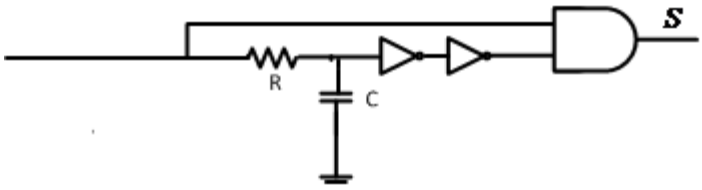


Figure 6.6 Logic gate for deadtime delay

6.4 Regulated power supply

Dc Regulated supply +5V is required for providing biasing to all the switching circuits by using ICs 7805 for +5V. One of the input phase voltage is stepped down using 220/18V transformer. It is then rectified using IN4007 diodes and fed to the regulated voltage IC. Capacitors are used at both the input and the output end of the IC to filter out voltage ripples .The circuit diagram of the regulated DC power supply is shown in following figure:

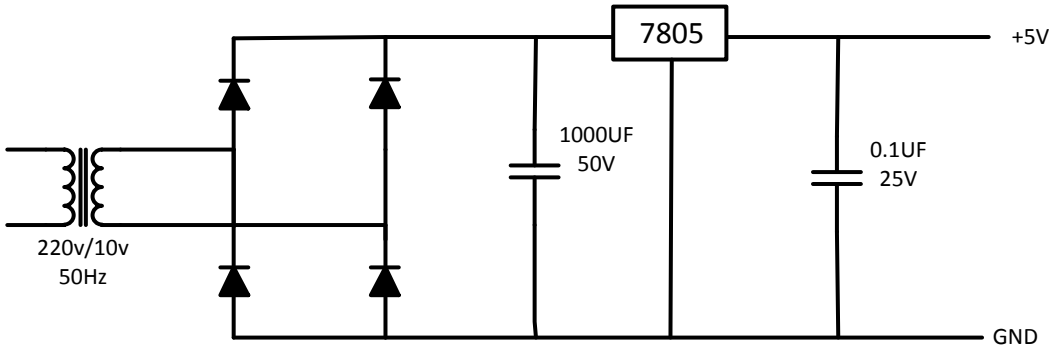


Figure 6.7 +5V power supply

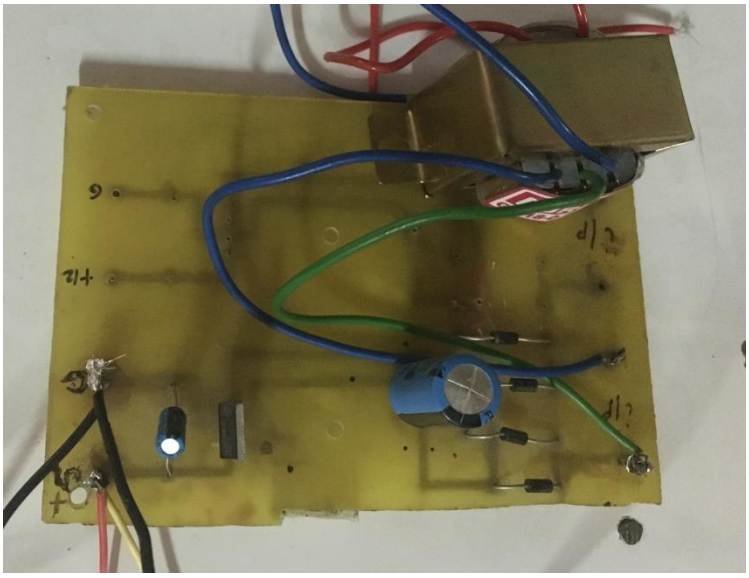


Figure 6.8 +5V power supply unit

CHAPTER 7 CONCLUSION AND FUTURE WORK

Multilevel inverters provide a better performance as compared to two level inverters. Multilevel inverter gives low harmonics contents, has low voltage stress on switching devices, and can operate on low frequency, so for high power application multilevel inverters are preferable over two level inverters.

Space Vector PWM is superior as compared to other pulse width modulation techniques in many aspects like :

1) The Voltage THD is lower for SVPWM
2) The output voltage is about 15.5% more in case of SVPWM .

SVPWM algorithm used in five-level inverters is more complex because of large number of inverter switching states. Hence we see that there is a certain trade off that exists while using SVPWM for inverters for Adjustable speed Drive Operations. Due to this we have to choose carefully as to which technique should be used weighing the pros and cons of each method. Space Vector PWM generates less harmonic distortion in the output voltage in comparison with multicarrier PWM schemes. In-phase disposition PWM technique gives the lowest Voltage THD after SVPWM and it can be employed in place of SVPWM if the complexity of the circuit is to be avoided.

Between phase shifted and constant frequency multicarrier PWM schemes the Voltage THD is lower for latter as seen from the experimental results in MATLAB but the device switching frequency and conduction times are unequal. Therefore if we choose constant frequency multicarrier scheme if we rotate the switching pattern otherwise a trade-off between better THD or equal device switching frequency can be achieved depending on the load .

Hardware of five level H-bridge multilevel inverter was successfully deigned but generation of control signals for various pulse width modulation schemes could not be achieved. Future work includes successful generation of various control signals and verification of obtained results.

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