A

Report on

AN ANALYTICAL APPROACH TO EXTRACT PARASITIC CAPACITANCES OF FINFET.

In partial fulfilment of the requirements for the degree of

MASTER OF TECHNOLOGY

In

ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Microelectronics and VLSI)

Submitted by

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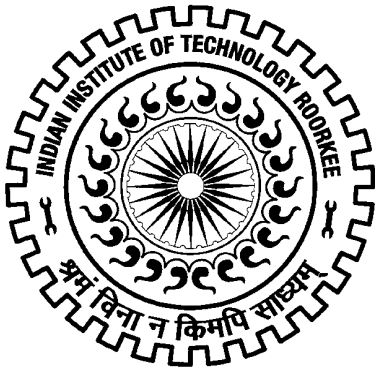

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

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CANDIDATE'S DECLARATION

I hereby declare that the work, which is being presented in this report entitled, **"AN ANALYTICAL APPROACH TO EXTRACT PARASITIC CAPACITANCES OF FINFET"**, in partial fulfilment of the requirements for the award of the degree of **Master of Technology** with specialization in **Microelectronics and VLSI**, submitted in Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee, India, is an authentic record of my own work carried out during the period from July 2015 to May 2016 under the supervision of **Dr. S. DasGupta**, Department of Electronics and Computer Engineering. The matter presented in this report has not been submitted by me for the award of any other degree of this institute or any other institute.

Date: _____

Place: Roorkee PAWAN

CERTIFICATE

This is to certify that the above statement made by the candidate is true to the best of my knowledge and belief.

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Abstract

In most of electronic application Memory is an essential part. To push the performance limit further, FinFETs are taken into consideration. It has confirmed to be promising alternative to take performance factor to next level because of their high resistance to SCE (short-channel effects). However, owing to its 3-D nature, high level of parasitics, which are significant in nm regime, degrade their high-speed analog and digital performances. In this dissertation we will get insight to reduce the impact and for that we have to find factors that affects parasitic components. In this dissertation, we are going to analytically derive an expression for the extraction of Outer fringe parasitic capacitance based on conformal mapping, which takes outer fringe field to be elliptical instead of circular, for better accuracy. Afterwards, using the same concept, i.e. elliptical inner fringe, field we will go for analytical derivation of Inner fringe parasitic capacitance. This model shows different geometrical parameter which affects parasitic capacitances. Lastly, comparison between modelled and simulation is done. Also, comparison between results of this work and other's reported work result with different method is shown.

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Chapter 1

Introduction

1.1 An Overview

Semiconductors has impacted every individual nowadays. It is the core of any electronic device. One cannot think of one's daily routine without the use of any electronic device. It has gained that much importance in our life. Moreover, Semi-Conductor industry is one of the rapidly growing sector. In the absence of semiconductors, we cannot imagine computers and modern electronics. And with these, we could think of the simpler devices that could result in our modern computers. For example, transistor radios, in which semiconductors are utilized, made it realizable for people to have radios which they can carry wherever they want. Similarly, early calculators took advantages of semiconductors and made it realized for people to use it as a portable device. Before the era of semiconductor, a simple calculator which could perform very basic operation cost almost as much as a personal computer does today.

In today's time semiconductor market is so grown up that very complex operation can be easily done within seconds using complex electronic device. But the complex circuit in that device is realized by very simple electronic device. In other word, the building block of any complex device is a simpler one, e.g. a switch. Semiconductor possess the property to control those switch with very small value of current or voltage. And those switch are then used to alter or control the state of individual component of a complex device.

The electronic device that act as controllable switch is nothing but a transistor. It is a semiconductor which has replaced vacuum tubes which were large in size also power requirement were more. Further, those transistor have been developed year by year to boost its performance. Thus, device which are made up those transistor are getting better and better. For instance, Memory device which were used to be so heavy that one cannot moved on its own. And now, device with same amount of memory become so small that one can keep it to oneself all the time anywhere. This has open the door of further advancement of technologies.

Memory arrays are a major part of the chip area in a particular microprocessors. As we know memory consume a large part of future designs, we should always have to look forward to scaling

trends of logic to get better outcome. But with decrease of device dimensions reason for severe increases of parametric variation come into picture and along with this trend decreasing system supply and transistor threshold voltages can also degrades performance of some devices e.g. it reduces the stability of conventional six-transistor SRAM cells. It is a challenge for the VLSI designers to overcome intra- and inter-die variations and in recent years, several schemes/devices have been proposed which possess the power to overcome these challenges. For example FINFETs (more detail about FINFETs is given in chapter 2) etc. The FinFET transistor structure has been developed which can replace the bulk structure for its good electrostatic properties and its improved scalability in submicron regime.

Approximately 60% of the transistors in a superscalar, which consists of billions of transistor, are expected to be used in memory arrays, especially larger SRAM data caches. Hence, chip area and leakages are determined majorly by these arrays. With around 4-5 cache accesses occurring per cycle in machine, the performance depends on cache access time. The performance of an SRAM system is determined mainly by the delay while driving heavy loads on the wordline and the bitline. In FD SOI, the bitline load is dominantly interconnect. Hence increasing cell device widths even at the cost of higher gate capacitance decreases delay as drive current is also increasing. Alternately, under a scenario of power-constrained design, higher widths can accommodate a decrease in Vdd and an increase in V_t (transistor threshold voltage) to save power while maintaining performance. Planar CMOS technologies such as bulk or double gate do not permit us to increase in channel width at will, the associated area penalty make the array density to be reduced and delay advantages thus diminished because of the increase in wordline and bitline lengths. Solution to this is quasi-planar FinFET as it allows an increase in effective channel width without penalize area factor simply by increasing fin-height.

1.2 Evolution

Since the fabrication of MOSFET, the channel length has been scaled down continuously. The prime motivation for this comes from an interest in high-speed devices and in VLSI integrated circuits. To keep the scaling of conventional bulk device going on, it requires some innovations to circumvent the hurdles of fundamental physics associated with the conventional MOSFET device structure. The reason for limitations most often are control of the density and location of dopants providing high I_{on} /I_{off} ratio and finite sub threshold slope and leakage due to quantum-mechanical

tunneling of the carriers through thin oxide from channel to gate, drain to source and from drain to body.

The channel depletion width along with channel length must be scaled to contain the off-state leakage I_{off}. This leads to requirement of high doping concentration, which affects the carrier mobility negatively i.e. degrades it and also causes junction edge leakage due to quantum tunneling. In addition to it, controlling the dopant profile, in terms of steepness and depth, becomes much more problematic. The gate oxide thickness t_{ox} must also has to be scaled along with the channel length to achieve better gate control, required threshold voltage V_t and performance. But hurdle with the thinning of the gate dielectric is that it results in gate tunneling leakage, causing poor the circuit performance, noise margin and power. Hence, there are lot of problems related to scaling of conventional MOSFETs. And these problems are even more severe in nanometer regime. A list of effects [9] which cannot be neglected in smaller dimension is given below:-

- *Leakage Current*
- *Drain Induced Barrier Lowering*
- *Polysilicon Depletion*
- *Carrier Velocity Saturation*
- *Channel Length Modulation*
- *Charge Sharing*
- *Hot Carrier Effects*
- *Velocity Overshoots*
- *Quantum Mechanical Effects*

To tackle problems associated with above mentioned effects, many methods had been developed and showed better result.

We have now got an idea that the short channel effects (SCE) is the main concern for the designer, effect of which is getting more and more stronger as the size of transistor is reducing. Moreover, it is directly linked to device reliability

One of the main reason for poor performance of device at shorter length is penetration of electric field from Source/Drain in the channel region. It effects the electric field from gate which is

required for channel formation. It leads to DIBL. Next, some conventional methods to tackle SCE or related problem is explained in brief

1.3 Conventional methods to curb SCE or related problems

1.3.1 Thin body FD SOI MOSFET

It is found that to reduce short channel effects in fully depleted SOI MOSFETs use of thin body i.e. thin silicon film is favorable. Thin body is useful to mitigate leakage the through surface. The device implemented with this concept is thin body MOSFET [10]-[11]. An advantage of thin body is that it does not require heavily doped channel to reduce the SCE. Hence, it avoids the mobility degradation problem as impurity scattering will be less in the absence of heavy doping. Another improvement is done in this i.e. raised S/D is used to tackle the high resistance problem [12].

1.3.2 Metal Gate fully depleted SOI MOSFET

Use of polysilicon gate is more problematic than its advantages in nanometer regime due to polysilicon depletion, high gate resistance and Boron penetration [13]. Moreover, metal used at gate is selected in such a way that it could facilitate some adjustment of the threshold voltage without increasing thin film doping density. It is found that this could be done by use of work function of tantalum. In this way, above mentioned problems are removed. Hence, SCE is reduced relatively.

1.3.3 Buried Insulator

The use of buried insulator is found advantageous to curb SCE such as DIBL. The penetration of electric field is reduced in buried oxide, which is emanating from Drain, due to reduction in permittivity [14]. The reduction of charge sharing problem is also reported using this method.

1.3.4 Graded channel Fully Depleted SOI

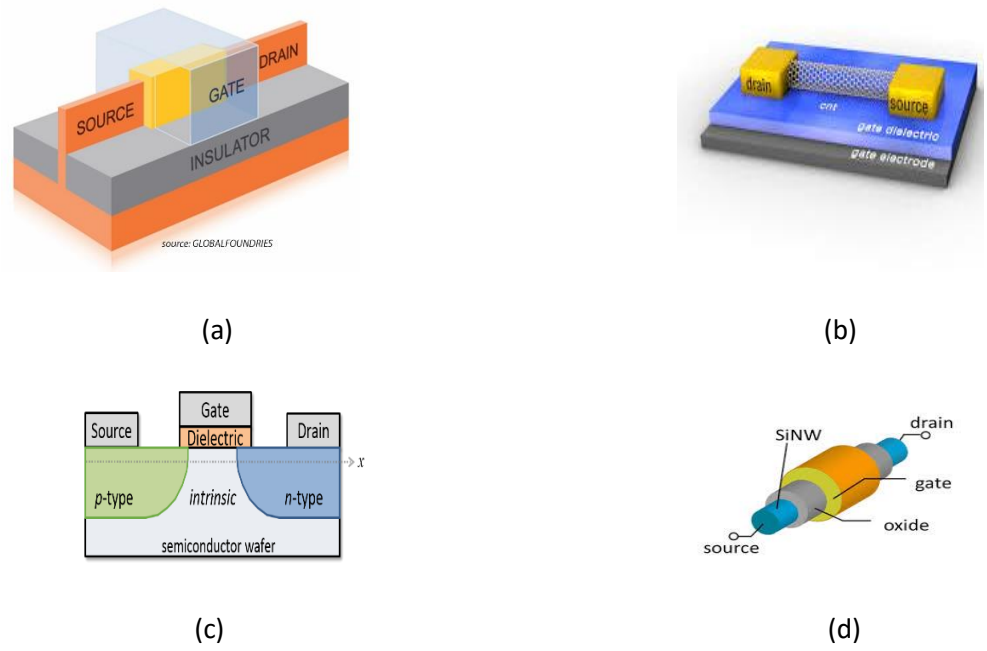
In this method channel is not doped uniformly. Instead, at center doping is as same as that of uniformly doped device but near S/D regions channel is heavily doped. As compared to uniformly doped device graded channel device has shown improved SCE but at the cost of mobility degradation due to high doping.

1.3.5 Halo Doped SOI

To tackle off-state leakage like SCE halo implantation technique is purposed. In this, a pocket of high doping of substrate-material type is implanted around S/D. Due to high doping around S/D region punch through phenomenon is avoided.

1.4 MOSFET to unconventional FETs

With those hurdles in conventional MOSFET scaling the use of few above mention solution has come to an end. So, designers had to think away from conventional method i.e. some innovation were required. To deal with all the issues related to FETs, designers have come up with some new ideas. New devices and methodologies are designed to get far better outcome in terms of performance, area, costs etc. They have developed or proposed different kinds of schemes or devices e.g. Finfet, Carbon NanoTube (CNT), TFET, Silicon Nanowire etc.



(a) (b)

(c) (d)

Fig.1.1 Different unconventional FET devices (a) FINFET (b)CNT (c)TFET (d) Silicon Nanowire FET

1.5 Organization of Thesis

Thesis has been organized in six chapter. Chapter One provide some introduction to problems that are being faced with some conventional solution, which motivates designers to go for new devices like FinFETs. Then, Chapter Two explains about FinFET, its structure, fabrication and some advantages. It also give some idea about design consideration that should be adopted to get maximum advantages. From Chapter Three main topic of this thesis begins. It introduce some basics of parasitic components associated with FinFET. The parasitics which are modeled in this work is described here. Then, in Chapter Four an analytical modeling is done. Concept of conformal mapping i.e. coordinates transformation is described first. Afterwards, Poisson's equation is used to derive inner and outer fringe parasitic components. Next, in Chapter Five our model is validated by matching the result of model with simulation result and also by matching to the result of other's work. Lastly, in Chapter Six conclusion is drawn.

Chapter 2

FINFET

2.1 Overview

A UC Berkeley team led by Dr. Chenming Hu proposed an innovative structure for the transistor that would reduce SCE and leakage current.

They suggested that a thinner-body MOSFET structure would be good for controlling short-channel effects. Later, intrinsic-body double-gate MOSFET has come out as one of the leading candidates which could replace Bulk and Partially-Depleted SOI CMOS due to having its superior scalability for a given gate oxide thickness, diminishing short-channel behavior without complex channel engineering, higher mobility without much doping and hence the absence of random dopant fluctuation effects. The ideal MOSFET as we know is a gate-voltage controlled switch, and the short channel effect represent the negative influence of drain-voltage on channel electrostatics as channel length decreases. The double-gate fully-depleted MOSFET reduces the short-channel effect by keeping the gate closer to the surrounding of the channel, providing good capacitance coupling and thus improves the scalability feature. As compared to planar double-gate devices, the quasi-planar SOI FinFET and other variants have been proposed as easier manufactural options. Researchers have begun to develop design tools for migration of microprocessor designs etc. from PDSOI to FinFET CMOS. In FinFETs, effective channel width is related to fin height which is perpendicular to the semiconductor plane i.e. different from planar single- and double-gate devices. Due to which it is possible to increase the effective channel width per unit planar area by increasing fin-height which give rise to increase in drive current.

2.2 Basic Structure of FINFET

Initially two structures had been proposed as shown in Figure 1. Having the same fundamentals as of conventional MOSFET, with some development just by changing the structure modern FINFET has been developed. This device is given name as FINFET because the silicon material structure i.e. body of FINFET resembles the fin of fish!.

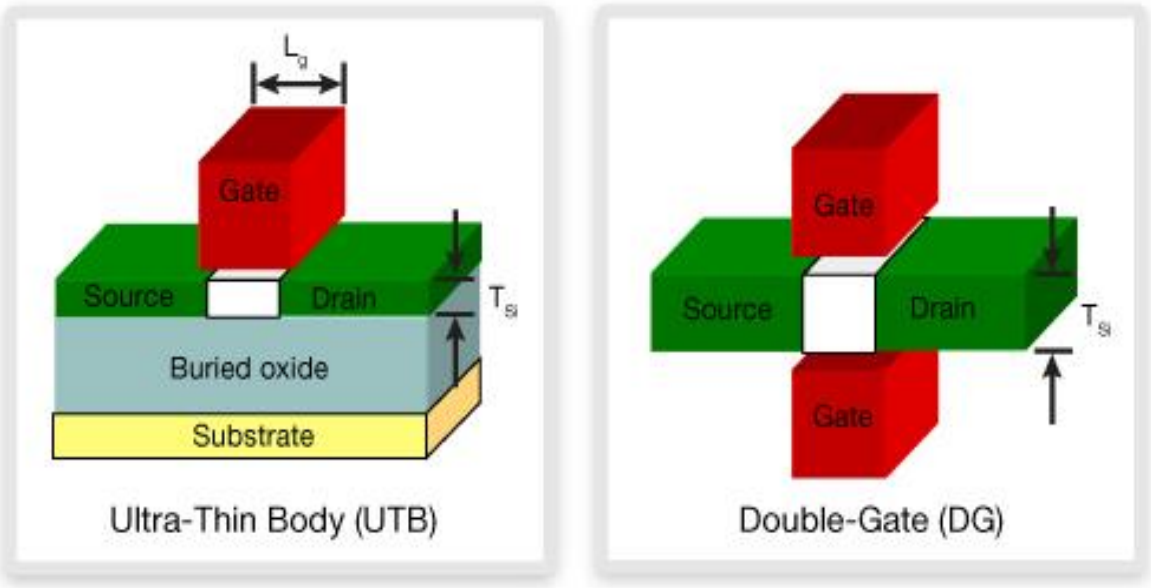


Fig. 2.1 Demonstration of the origin of modern FinFET transistors [20].

On rotating the DG structure we get structure of FinFET. It possesses the potential to provide the lowest gate leakage current and manufacturing is also simpler using standard lithography techniques because the gate electrodes become self-aligned in this technique shown in figure 2.2

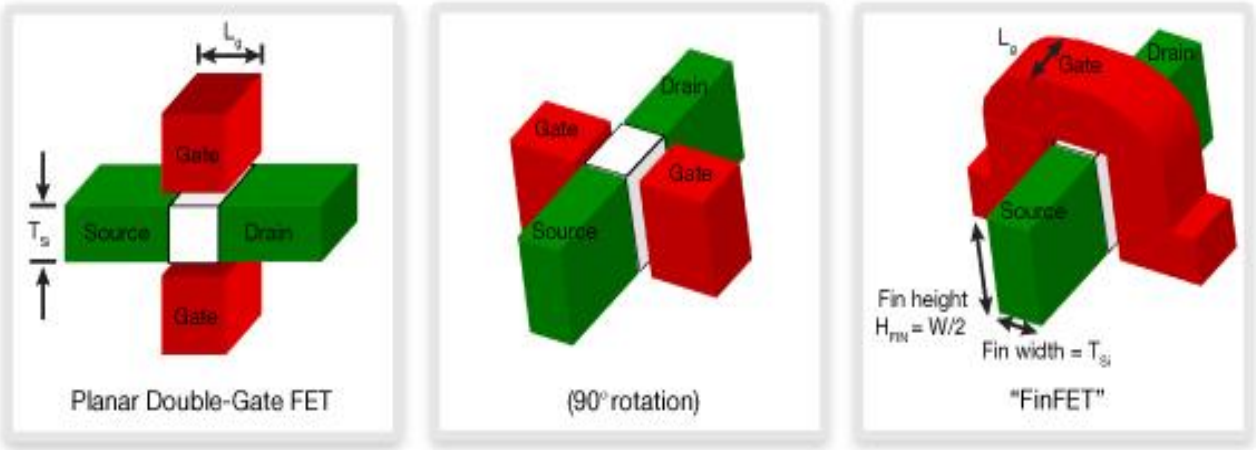


Fig 2.2- From planar DG FET to FinFET [20].

FinFETs are 3D structures above the planar substrate, which give them more volume than a planar gate for the same planar area. Providing the superb control of the conducting channel by the gate,

which surrounds the channel from two or three sides, very little amount of current is able to leak through the body during the device is in the off state. Due to this, lower value of threshold voltages is allowed and as we know that the threshold voltage is in direct proportion to power and delay so low threshold voltage results in better switching speeds and less power requirement.

Now, basic structure of modern FINET is same as shown in fig. However, it shows Gate terminal from three sides so this structure is called Triple Gate FINFET. But using the same structure Double Gate FINFET can also be formed. For that, a thick high permittivity material is formed at top of the fin. In this way effectiveness of gate potential in channel formation is taken away and effective gates are present at sideways only making it Double Gate FINFET.

2.3 Design Consideration to control SCE

After the realization of FINFET many research has been done to get as much as possible from FINFET device. Figure below shows a DG FINET with marked labelling. Due to symmetry, only half part is shown.

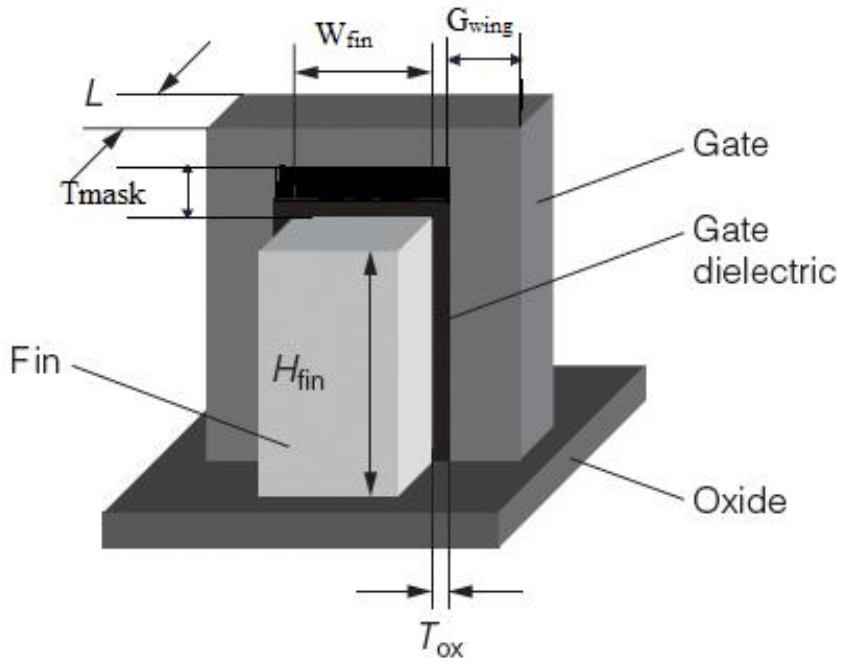


Fig. 2.3 Schematic of FinFET with proper labelling.

It contains an undoped or lightly doped silicon formed over buried oxide layer. At the both extreme end highly doped Source and Drain region is formed (not shown in above image). A small gap

between gate region and S/D is also present known as extension region. This is done to reduce SCE. As S/D regions are highly doped, some lateral diffusion takes place in extension region. Taking advantages of this lateral diffusion two configuration named overlap and underlap FINFET are developed. It affects analog RF parameters. Researchers have found that effect of those structures can be in favor or against depending on the application in which it is used. The figure shows a FinFET of single fin. Researchers have also reported multifin structure which is shows better result in various performance factor like speed, area etc

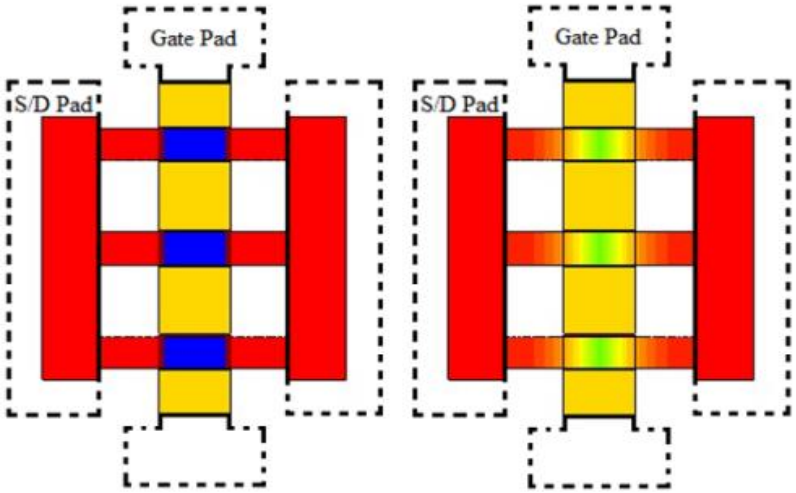


Fig. 2.4 Diagram of underlap and overlap multifin [15].

The drive or on current of FinFET is depend upon channel length and width of device just like in MOSFET. Unlike MOSFET, width of FinFET is quantized. Because width of FinFET depends on the fin height and using multiple fin the width will vary discretely as the height of all the fin is same. Overall width of FinFET is given as:-

$$W_{total} = N*(2*H_{fin}+T_{fin})$$

Where N is the no. of fins in a multifin device, H_{fin} is height of each fin and T_{fin} is the thickness of each fin.

Also due to lateral diffusion effective channel length of the device can vary as shown in figure below.

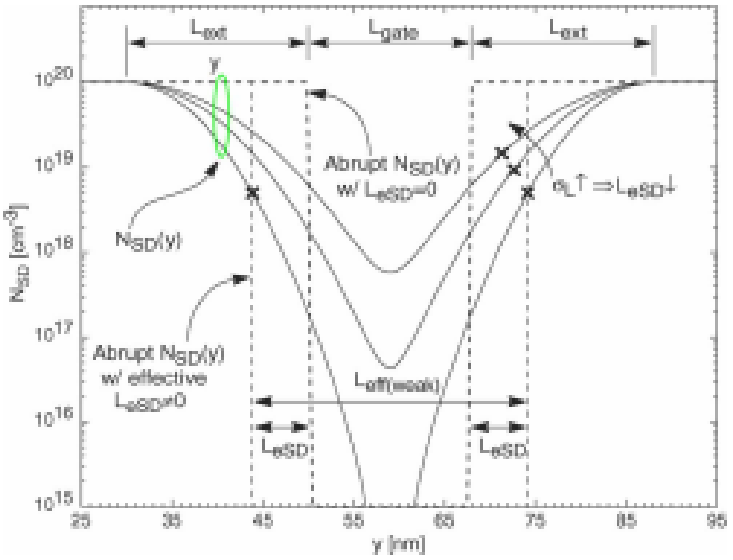


Fig. 2.5 Demonstration of effective channel length with different lateral doping density profile [8].

This also leads to carrier concentration modulation by the application of gate potential. It can be understood by the concept of Debye length. It is inversely proportional to square root of carrier conc. (L α $1/\sqrt{n}$) where 'n' is the carrier concentration in the body. At the extension region both sides near the gate, the conc. of free charge carriers in weak inversion is very small so according to Debye length relation field lines emanating from gate plate can penetrate more inside extension region i.e. effect of gate potential reaches beyond the channel. gate region [7]. Therefore, effective channel length (L_{eff}) increases in weak inversion i.e. $L_{eff} > L_g$. This phenomenon results in reducing SCE. In other words, the gate potential can modulates the carrier concentration nearby channel region and offer very small value of off-state leakage current. During strong inversion 'n' will be large, thus, effective length will as same as physical gate length. This small effective length cause larger drive or on current which is again advantageous

In FinFET, the SCE can be considerably controlled by altering the fin height and thickness and it is found that to reduce SCE the thickness of fin should be less than or equal to one third of channel length and fin height should be approximately three to five times of fin thickness.

2.4 Fabrication of FINFET

As we know that the FinFET is derived from MOSFET. So, its fabrication process resembles with that of MOSFET with some modification. The basic fabrication process step for the formation of FinFET is explained below:-

1. Formation of BOX i.e. Silicon dioxide layer.
2. After depositing SiO_2 and SI_3N_4 layer of Si fin is formed.
3. Next, Pentavalent impurities e.g. phosphorous doped Si is deposited.
4. With Si fin blocked by mask layer, Drain/Source regions are etched.
5. Spacer i.e. Silicon Dioxide layer is etched up to BOX.
6. Then, Gate stack formation take place.

First of all the base of SiO2, on which whole structure is formed, is deposited. Afterwards, a standard process for FinFET structure formation is used. In which, spacer lithography is used to form the ultra-thin fins [16]. It gives better uniform fin width.

Once the fins are etched there will be some roughness left and this has to be smoothed for better performance and this smoothness is done by annealing and oxidation. The best method considered to remove those kind of defects is annealing.

The process of formation of fins and S/D is quite same as defining trench isolation in cmos i.e. they are etched to the silicon layer followed be channel processing. After the formation of S/D, oxide spacer etched. These spacers provides a medium to reduce parasitic components. For example, the electric field coupling b/w gate walls and S/D extension part reduces the resistance and thus help in improving On state current. Also, raised S/D can be used to further reduce the resistive component of the parasites.

Etching during Gate formation should be done carefully so that fin could not get damaged. As the gate body stack is at the top of fin, a planarization step can be used to ease the etch step.

Chapter 3

Parasitic component of FinFET

3.1 Introduction

There were always some parasitics component, capacitive or resistive, associated with conventional MOSFETs device. In the beginning it had not drawn much attention. As it was relatively very small in value. So, its effect was not significantly deteriorating the device performance. As scaling process reached to nanometer regime, things started to get complex. Because owing to small dimension, capacitances and resistance of the device were also scaling down. But the parasitics were not following the same rate. Ultimately, these parasitics are now become very much comparable and fraction of which is keep on increasing. Thus, neglecting these is not good choice now. As previously discussed FinFETs are found to be encouraging candidates to take the performance limits far ahead in Semiconductor industry, thanks to their great immunity to short-channel effects. But, due to their 3-D structure, high parasitic capacitances and parasitic resistance exist that can significantly degrade their high-speed digital and analog Radio Frequencies application performances. More specifically in memory array circuits high capacitances and resistance can reduce the unity gain frequency of the device which will put a limit to the speed performance. So it is likely to reduce those parasitics.

This dissertation is focused on parasitic capacitances rather than resistive one. So, parasitic resistance is briefly explained here. Then, we will get insight of different parasitic capacitances. Finally, we go for analytical derivation of those capacitances.

3.2 Resistive parasitic component

In resistive category there are two main types of parasitics, namely,

1. Gate Resistance
2. S/D Series Resistance

3.2.1 Gate Resistance

This parasitic resistance is due to gate contact, surface roughness distributed along the channel length. As FinFETs especially with multifin structure, are found to be excellent candidate to provide better performance in analog as well as in digital. With multifin, parasitic like gate resistance also increases. In high frequency applications, the analysis should not be undermine by not studying those parasitic carefully. Researchers are now studying this and trying to model this effect accurately [17].

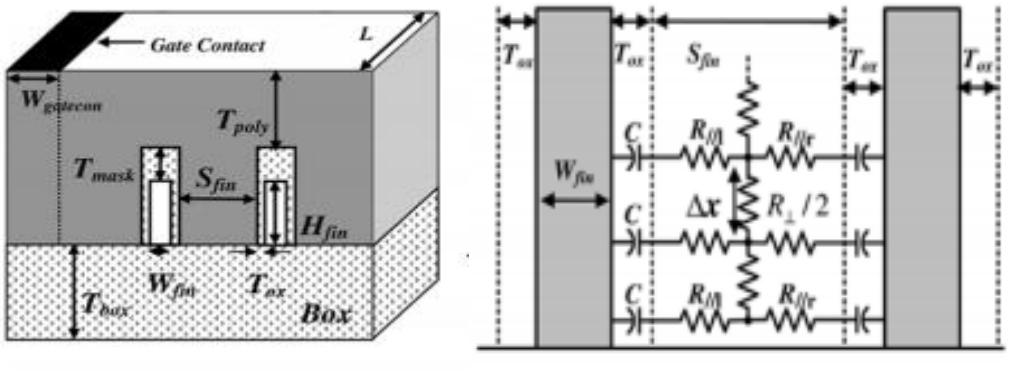


Fig.3.1 Illustration of multifin FinFET Gate resistance.

If neglected, than one will get very large numbers of respective performance factor. But in practical those values will drastically fall. Because those parasitic cause problem to achieve high performance. Using proper model accurate behavior can be determined. Also, those parasitic can then be reduced wherever possible.

3.2.2 Source/Drain resistance

As the name indicating this parasitic is present in Source/ Drain region. For the SCE suppression Fin width is supposed to be as narrow as possible. This give rise to high S/D resistance. A part of this is contributed by contact and another part is contributed by S/D region itself. This parasitic cause reduction in device drive or on current and it is so problematic that it should be minimized up to possible extent. So proper modelling is required so that designers can think of minimizing it. Otherwise it will keep in degrading the device performance. Designers are presenting different

ways to reduce this kind parasitic by first modeling it [18]. Double gate, Triple gate Finfet shows different results. It is strongly dependent on device geometry. Nowadays, use Extended S/D region is widely taken into consideration.

3.3 Capacitive parasitic component

Another parasitic component, capacitive one, is very important to be considered for accurate calculation of performance parameter of the device. Reason behind it is same as mentioned before i.e. without considering those capacitive parasitic one will get different values than practical one and face performance failure of the device. Because although these parasitic capacitances are very small in value, but they have become very much comparable in the regime of nanometer scale as device intrinsic capacitance is also scaling down along with dimension. So it cannot be neglected. Also, there contribution are found to be increasing much faster with the scaling down trend. Thus, these capacitances become more important to be considered in determining overall capacitances. These parasitic cannot be avoided but it can be reduced to some extent. Fig. 3.2 below gives some idea about parasitic components of DG-FinFET.

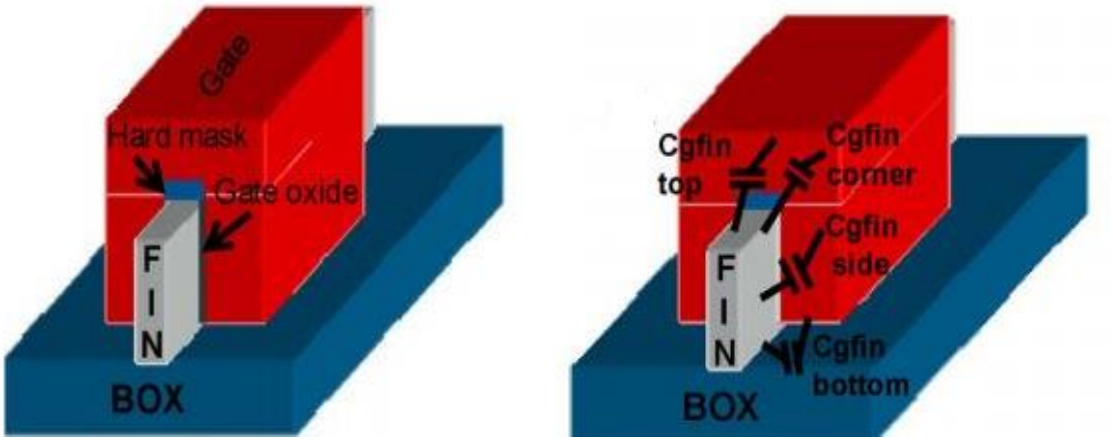


Fig. 3.2 (a) DG-FinFET (b) different parasitic capacitance. [1]

An analytical model will be derived for DG-FinFET to accurately find the parasitic capacitance. Well, a capacitance come into picture when there are more than two electrodes having some kind of insulator of finite thickness which is separating them and an electric field lines which couples those electrodes. These field lines hard to be constrained due to which some unwanted coupling between different electrodes takes place. Those unconstrained field lines are known to be 'Fringe Field' and Hence the name, Fringe Capacitances. Depending upon whether the fringe field is inside the FinFET i.e. through the channel or outside the channel it is of two type namely 1) outer fringe capacitance and 2) inner fringe capacitance. Analytical derivation will be done one by one in next chapter.

3.3.1 Outer Fringe Capacitance

As it consists of outer fringe field lines but those outer fringe lines emanate from different region of gate and terminate at different region fin of the FinFET structure as depicted in figure 3.3. This leads to different outer fringe capacitance. Capacitances associated with outer fringe are explained below:-

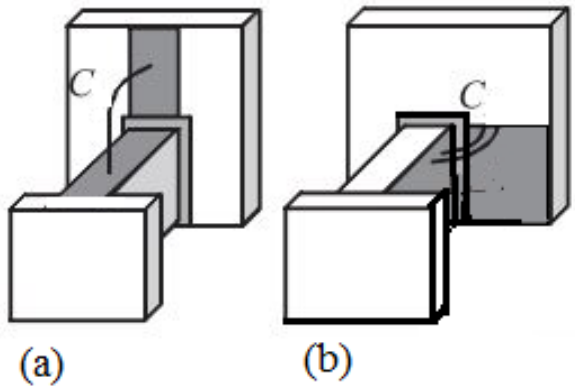


Fig. 3.3 Outer fringe capacitances of FinFET (a) $C_{gfinTop}$ (b) $C_{gfinSide}$ [5]

$C_{gfinTop}$, it represent electric field from gate sidewall to top of S/D extension region of fin.

$C_{gfinSide}$, it represent electric field from gate sidewall to sidewall of S/D extension region of fin.

3.3.2 Inner Fringe Capacitance

It is due to inner fringe field lines which emanate from inner side of gate electrodes and through the channel region terminates at S/D as shown in figure 2.3. With inner fringe, capacitances associated are:-

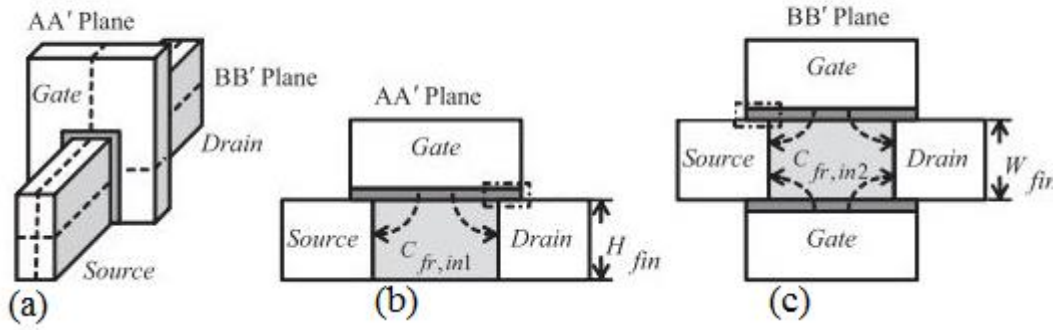


Fig. 3.4 Inner fringe capacitance (a) FinFET with intersecting planes (b) C_{ifTop} (c) C_{ifSide} [5]

C_{ifTop}, it represent electric field from bottom of gate at the top of fin to fin face beside channel.

C_{ifSide}, it represent electric field from the inside of gate around the fin to fin face beside channel.

Chapter 4

Analytical Modeling of parasitic capacitances

4.1 Introduction

Up to here we have studied the importance of parasitics and why do we need robust model. So, in this chapter we will do mathematics to derive an analytical expression to predict those parasitic capacitances. Expression will contain different FinFET geometry that indicates geometry dependent derivation. With the help of it we can find an optimum device geometry for a given technology node.

4.2 A Flash Back of Analytical Derivation

The basic way to derive a capacitance expression is to solve Poisson's or Laplace equation with suitable boundary condition. However, with different types of structures of capacitors and coupling field nature i.e. straight or circular etc. solving Poisson's equation in Cartesian system for every structure is a tedious task and sometime it becomes impossible to solve analytically. So, depending upon field nature or capacitor structure, such as parallel plate, angle plate, circular and spherical etc., appropriate coordinate system such as Cartesian, Cylindrical, Spherical coordinates system is used. This technique is called conformal mapping.

As we can see from the Fig. 4.1 that plates of parasitic are perpendicular to each other. The lines of electric field from one plate to other cannot be straight. It can be circular or elliptical (more or less close to them).

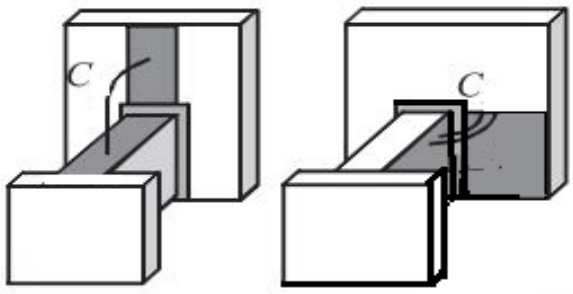


Fig 4.1 Illustration of perpendicular electrode of capacitance.

Many model has been derived considering it purely circular. In one of which a formula for capacitance with perpendicular plates is derived using cylindrical coordinates as:-

$$C = \frac{2}{\pi}.\epsilon.\ln(1+\frac{l}{d})$$

But considering electric field line to be circular do not provide accurate result. Because those lines of field are elliptical in actual way. To validate this consideration we can see the equipotential surfaces between the gate and fin region, which is hyperbolic in nature. We know from basic electrostatics that

$$E = \nabla V$$

Where, ∇ Del operator. It is defined as

$$\nabla = \frac{\partial}{\partial x} + \frac{\partial}{\partial y} + \frac{\partial}{\partial z}$$

Where, E is electric field and V is voltage at electrodes.

Which signifies that electric field lines are always perpendicular to equipotential surface.

Now the lines perpendicular to hyperbola essentially is an ellipse. Considering elliptical lines and solving the integration in Cartesian coordinates to find capacitances is not possible analytically. This is why we opt for elliptical coordinates instead.

Considering above discussion, for our modeling we will opt for conformal mapping technique (the coordinate transformation technique) in which Cartesian coordinate system will be transformed to elliptical coordinate system. We will found that this transformation make analytical derivation feasible and easier. Before going for actual derivation of parasitic capacitance we will learn about elliptic coordinate system. Then it will be easy to understand further derivation.

4.3 Mathematical background for elliptical coordinate system

In Cartesian system (x, y) axes form the orthogonal coordinate system as shown in fig. 4.2

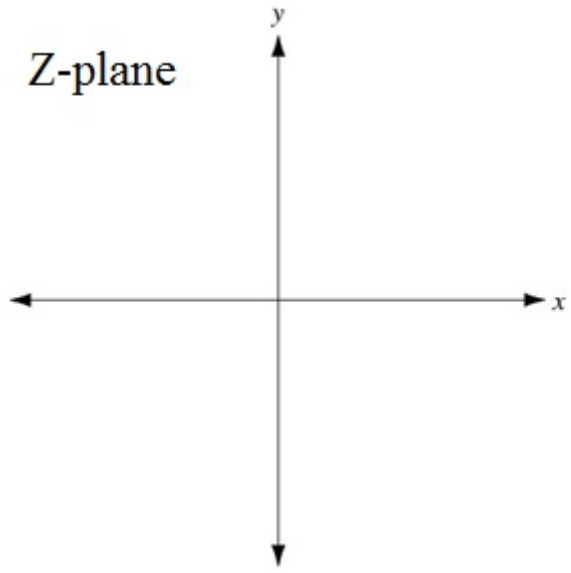


Fig. 4.2 Cartesian system

Likewise, in elliptical coordinates, set of confocal elliptical lines and confocal hyperbolic lines make the orthogonal coordinate system as shown in fig. 4.3

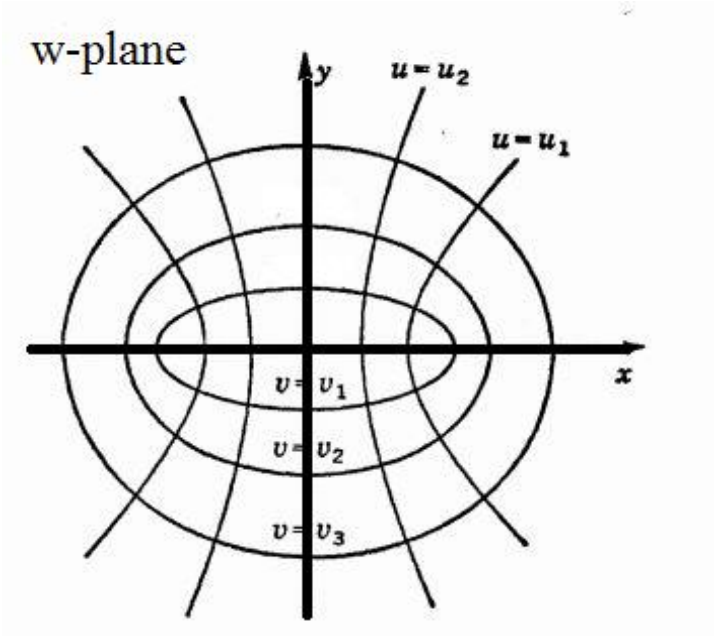


Fig. 4.3 u v coordinates where v represent ellipse and u represent hyperbola. [2]

From the conformal mapping concept, suitable function for this transformation is found to be 'arcos' i.e.

$$W = \cos^{-1} Z$$

i.e. $$u + jv = \cos^{-1}(x + jy)$$

On solving we get,

$$x = f cosu.coshv \qquad \text{- (4.1)}$$

$$y = -f sinu.sinhv \qquad \text{- (4.2)}$$

Where f is confocal focus of the curve.

Squaring both side and adding we get,

$$\frac{x^2}{f^2 \cos hv^2} + \frac{y^2}{f^2 \sin hv^2} = \cos u^2 + \sin u^2$$

$$\frac{x^2}{f^2 \cos hv^2} + \frac{y^2}{f^2 \sin hv^2} = 1 \qquad -(4.3)$$

Above equation represent ellipse, hence constant v-curve shows ellipse.

Now, squaring and subtracting (4.1) and (4.2) we get

$$\frac{x^2}{f^2 \cos u^2} - \frac{y^2}{f^2 \sin u^2} = \cos hv^2 - \sin hv^2$$

$$\frac{x^2}{f^2 \cos u^2} - \frac{y^2}{f^2 \sin u^2} = 1 \qquad -(4.4)$$

This shows equation of hyperbola, hence constant u-curve represent hyperbola.

Now to get result in terms of x, y coordinates, we have to do inverse mapping. From x, y to u, v there is one way i.e. unique relation. But inverse is not unique. There are more than one way of mapping from u, v to x, y.

From (4.3)

$$\frac{x^2}{f^2 cos\, hv^2} + \frac{y^2}{f^2 sin\, hv^2} = 1$$

$$\frac{x^2}{1 + \sin hv^2} + \frac{y^2}{\sin hv^2} = 1$$

As, $cos\, hv^2 - \sin hv^2 = 1$ and ignore f term because it will vanish ultimately.

$$x^2 . \sin hv^2 + y^2 + y^2 . \sin hv^2 = \sin hv^2 \, (\sin hv^2 + 1)$$

$$\sin hv^2 \, (x^2 + y^2 - 1) + y^2 = \sin hv^4$$

$$\sin hv^4 - \sin hv^2 \, (x^2 + y^2 - 1) - y^2 = 0$$

On solving above quadratic equation we get,

$$v = \sinh^{-1} \sqrt{\frac{x^2 + y^2 - 1 \pm \sqrt{(x^2 + y^2 - 1)^2 + 4y^2}}{2}} \qquad -(4.5)$$

Similarly we can find u in terms of x, y as :-

$$u = \cos^{-1} \sqrt{\frac{x^2 + y^2 + 1 \pm \sqrt{(x^2 + y^2 + 1)^2 - 4x^2}}{2}} \qquad -(4.6)$$

Now we have completed some mathematical background which will be used in deriving those capacitances. Now we are ready to derive those parasitic capacitance.

4.4 Parasitic capacitances modeling of DG-FinFET

For the analytical modelling of parasitic capacitances, previously mathematically derived results in the elliptical coordinates section will be used.

As the fringe capacitance (explained previously) has perpendicular plates and elliptical electric field between them. That scenario is shown in figure below:-

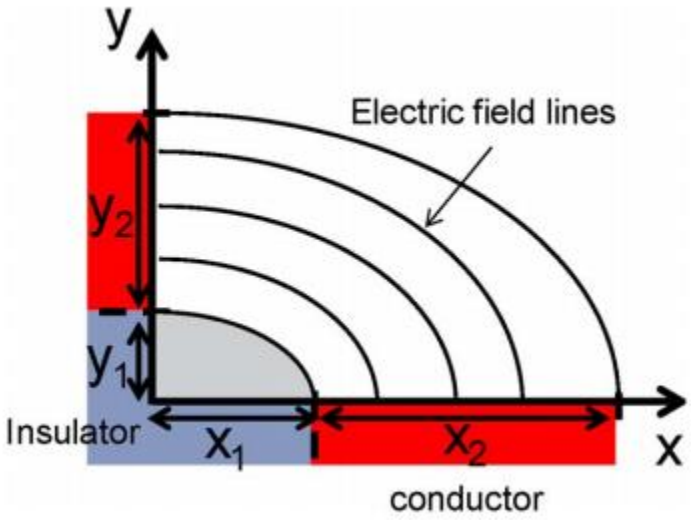


Fig. 4.4. Conformal mapping i.e. coordinates transformation. [1]

Equation of ellipse for inner one is:-

$$\frac{x^2}{x_1^2}+\frac{y^2}{y_1^2}=1$$

And equation outer ellipse will be:-

$$\frac{x^2}{(x_1+x_2)^2}+\frac{y^2}{(y_1+y_2)^2}=1$$

To have the above coordinate system orthogonal focus point of all ellipse and hyperbola should be same i.e. should be confocal. As we know the focus of a general ellipse is given by:-

$$f = \sqrt{|\, a^2 - b^2|}$$

To make the inner and outer ellipse confocal we will consider an effective length (on x-axis) of outer ellipse x'_2 so that those ellipse have same focus. Now, to find x'_2 we will equate foci of both the ellipse. i.e.

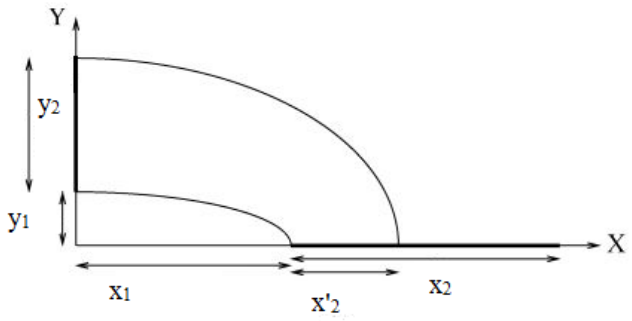


Fig. 4.5 Confocal elliptical field by considering length x'_2. [4]

$$\sqrt{x_1^2 - y_1^2} = \sqrt{(x_1 + x'_2)^2 - (y_1 + y_2)^2}$$

Solving for x'_2, we get:-

$$x'_2 = \sqrt{x_1^2 + 2y_1y_2 + y_2^2} - x_1 \qquad -(4.7)$$

Using the approximated coordinates to find confocal point we will use Laplace equation to first find Outer Fringe Capacitance then using Poisson's equation Inner Fringe Capacitance will be derived.

4.4.1 Outer Fringe Capacitance

Electric field passes through spacer region in outer fringe capacitance. This implies that volume charge is zero. Therefore using Poisson's equation,

$$\nabla^2 \emptyset = 0$$

As $\emptyset$ is the function of u only,

$$\therefore \qquad \frac{\partial^2 \emptyset}{\partial u^2} = \ 0$$

Integrating twice above eq.

$$\emptyset = c_1 u + c_2 \qquad -(4.8)$$

Applying boundary condition i.e.

$$at \ \ u = 0, \qquad \emptyset = 0 \ \& \ \ at \ \ u = \frac{\pi}{2}, \qquad \emptyset = V_{GS}$$

$$\therefore \qquad c_1 = \frac{2}{\pi} V_{GS} \qquad \& \qquad c_2 = 0$$

Put c_1 & c_2 in (4.8)

$$\emptyset = \frac{2}{\pi} V_{GS} u$$

We know $E = -\nabla \emptyset$

$$E = \frac{1}{h} \frac{\partial \emptyset}{\partial u} \widehat{a_u} \qquad -(4.9)$$

Where h is a scaling parameter.

And $h = f\sqrt{sinh^2 u + sin^2 v}$ f is the focus

Also $D = \varepsilon E \qquad -(4.10)$

Using conductor boundary condition, i.e.

$$\rho_s = D.\hat{n}|_{u=0} \qquad (4.11)$$

ρ_s is surface charge density. $\hat{n}$ is unit normal vector. Here, $\hat{n}$ is $\widehat{a_u}$. Using eq. (4.8), (4.9) & (4.10) in (4.11), we get,

$$\therefore \qquad \rho_s = \frac{2\varepsilon}{\pi h} V_{GS}$$

Charge can be obtained by evaluating surface integral of ρ_s. Here, surface is in v and z coordinates.

$$\therefore \qquad Q = \int_0^w \int_{v_1}^{v_2} \rho_s h \, dv dz$$

Capacitance is defined as change in charge with respect to voltage,$i.e.$

$$C = \frac{dQ}{dV_{gs}}$$

$$\therefore \qquad C = \int_0^w \int_{v_1}^{v_2} \frac{\partial \rho_s}{\partial V_{gs}} h \, dv dz$$

Where h is a scaling parameter.

$$C = \int_0^w \int_{v_1}^{v_2} \frac{2\varepsilon}{\pi h} V_{GS} \, dv dz$$

On Integrating above equation, we get,

$$C = \frac{2\varepsilon W(v_2 - v_1)}{\pi}$$

Where W is the width of the electrodes along the axis z, ε is the permittivity of the insulator and ($u_1 v_1$,) and (u_2, v_2) are obtained with equations 4.5 and 4.6 , and correspond to the smallest and the largest of the ellipse respectively, that is to say for (x, y) = (x_1 / f , 0) and (x, y) = ((x_1 + x'_2) / f), 0) , with x'_2 given by the equation 4.7. The dimensions x_2 and y_2 having a dual role, as the value of a capacitance is limited by the smaller electrode and thus replaced by the value between x_2 and y_2 which is minimum i.e.

$$v_2 = \sinh^{-1} \sqrt{\frac{\sqrt{x_1^2 + \min(x_2, y_2)^2 + 2y_1 \min(x_2, y_2)}}{\sqrt{|x_1^2 - y_1^2|}}}$$

$$v_1 = \sinh^{-1} \sqrt{\frac{x_1}{\sqrt{|x_1^2 - y_1^2|}}}$$

And $$u_2 = \frac{\pi}{2}\ , \quad u_1 = 0$$

There are also field lines, shape of which cannot be predicted. The area in which field lines are neither circular nor elliptical is shown below:-

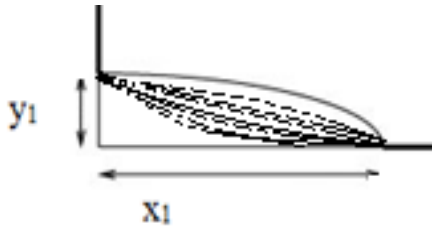


Fig. 4.6 Demonstration of region where field lines are not elliptical [4].

This model does not include capacitance due to these field. This capacitance is derived in [2] as

$$c = 0.35w\frac{\epsilon}{\pi}\ln\left(\frac{\pi w}{|x_1^2 - y_1^2|}\right)$$

Above capacitance will also be used in this model. Thus, the capacitance of two perpendicular electrodes of given dimensions, separated by an insulator permittivity ε and width W along the z axis is measured by:-

$$c = w\epsilon\frac{2}{\pi}\left[\sinh^{-1}\sqrt{\frac{\sqrt{x_1^2 + \min(x_2, y_2)^2 + 2y_1\min(x_2, y_2)}}{\sqrt{|x_1^2 - y_1^2|}}} - \sinh^{-1}\sqrt{\frac{x_1}{\sqrt{|x_1^2 - y_1^2|}}}\right.$$

$$\left. + \right] 0.35w\frac{\epsilon}{\pi}\ln\left(\frac{\pi w}{|x_1^2 - y_1^2|}\right)$$

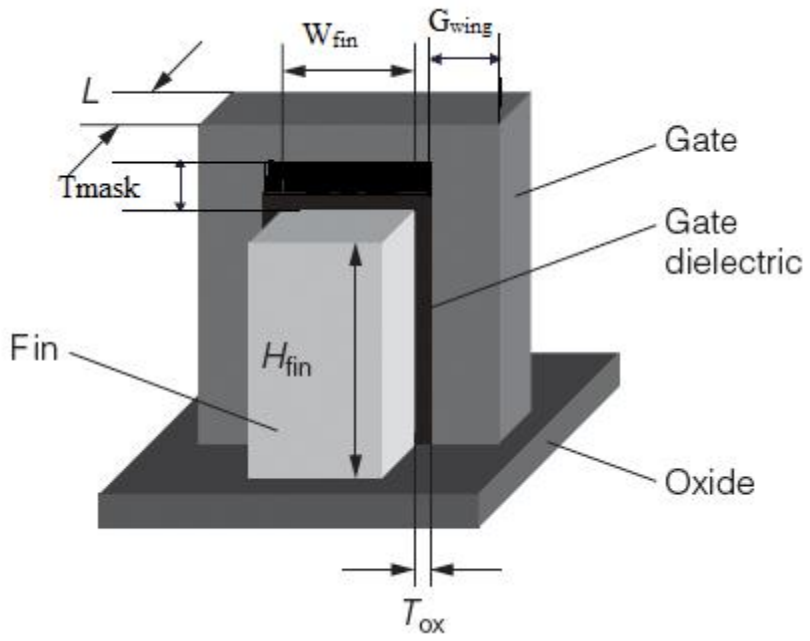


Fig. 4.7 Schematic of FinFET with proper labelling.

Finally, we can find different parasitic capacitance by using above formula with proper dimensions i.e. (refer to fig. 4.4 and fig. 4.6) assuming x direction along the fin and y along sidewall of gate and with origin at the extreme of the channel and side surface of fin. (Either side)

For $C_{gfinSide}$ $(x_1, y_1, x_2, y_2) = (0, tox, lsp, gwing)$. And w= $hfin$. So,

$$C_{gfinSide} = \frac{2}{\pi} hfin.\varepsilon.\sinh^{-1}\sqrt{\frac{\sqrt{\min(lsp,gwing)^2+2tox\min(lsp,gwing)}}{tox}} + 0.35w\frac{\epsilon}{\pi}hfin.\varepsilon.\ln(\frac{\pi hfin}{tox})$$

For $C_{gfinTop}$, assuming x direction along the fin, y direction towards top of the gate and origin at extreme of the channel and top surface of fin (x_1, y_1, x_2, y_2)= $(0, t_{mask}, lsp, Hg)$. And w= $wfin$. So,

$$C_{gfinTop=}\frac{2}{\pi}wfin.\varepsilon.\sinh^{-1}\sqrt{\frac{\sqrt{\min(lsp,Hg)^2+2t_{mask}\min(lsp,Hg)}}{t_{mask}}}+\ 0.35w\frac{\epsilon}{\pi}wfin.\varepsilon.\ln(\frac{\pi wfin}{t_{mask}})$$

Finally, the total parasitic capacitance is given as:-

Total outer fringe parasitic $C_{op} = 2(C_{gfinTop} + 2\ C_{gfinSide})$

4.4.2 Inner Fringe Capacitance

Now we will derive expression for inner fringe in subthreshold region. For this Poisson's equation will be solved in elliptical coordinates. To get the charge distribution in the body we have to use 2D Poisson's equation. But solving 2D Poisson's equation is a tedious task. Hence, we will use our conformal mapping technique. Using elliptical coordinates we have converted 2D Poisson's equation to 1D.

$$\nabla^2\emptyset = \frac{qN_A}{\varepsilon}$$

Here, charge due to inversion is omitted. Because we are using that equation subthreshold region.

As $\emptyset$ is the function of u only,

$$\therefore \qquad \frac{\partial^2\emptyset}{\partial u^2} = \frac{qN_A}{\varepsilon}$$

Integrating twice above eq.

$$\emptyset = \frac{qN_A}{2\varepsilon}u^2 + c_1u + c_2 \qquad -(4.12)$$

Applying boundary condition i.e.

$$at\ u = 0, \qquad \emptyset = V_{bi}\ \ \&\ \ \ at\ \ u = \frac{\pi}{2}, \qquad \emptyset = \varphi_s(v)$$

$$\therefore \qquad c_1 = \frac{2}{\pi}\left(\varphi_s(v) - \frac{qN_A\pi^2}{8\varepsilon} - V_{bi}\right)\ \&\ c_2 = V_{bi}$$

Put c_1 & c_2 in (3.1)

$$\emptyset = \frac{qN_A}{\varepsilon}u^2 + \frac{2}{\pi}\left(\varphi_s(v) - \frac{qN_A\pi^2}{8\varepsilon} - V_{bi}\right)u + V_{bi}$$

We know $E = -\nabla\emptyset$

$$E = \frac{1}{h}\frac{\partial\emptyset}{\partial u}\widehat{a_u} \qquad -(4.13)$$

Where h is a scaling parameter.

And $h = f\sqrt{sinh^2u + sin^2v}$ f is the focus

Also $D = \varepsilon E \qquad -(4.14)$

Using conductor boundary condition, i.e.

$$\rho_s = D.\hat{n}|_{u=0} \qquad (4.15)$$

ρ_s is surface charge density. $\hat{n}$ is unit normal vector. Here, $\hat{n}$ is $\widehat{a_u}$. Using eq. (4.12), (4.13) & (4.14) in (4.15), we get

$$\therefore \qquad \rho_s = \frac{2\varepsilon}{\pi h}\left(\varphi_s(v) - \frac{qN_A\pi^2}{8\varepsilon} - V_{bi}\right)$$

Charge can be obtained by evaluating surface integral of ρ_s. Here, surface is in v and z coordinates.

$$\therefore \qquad Q = \int_0^w \int_{v_1}^{v_2} \rho_s h \, dvdz$$

Capacitance is defined as change in charge with respect to voltage, $i.e.$

$$C = \frac{dQ}{dV_{gs}}$$

$$\therefore \qquad C = \int_0^w \int_{v_1}^{v_2} \frac{\partial\rho_s}{\partial V_{gs}} h \, dvdz$$

Here h is a scaling parameter.

$$C = \frac{2\varepsilon}{\pi}\int_0^w \int_{v_1}^{v_2} \frac{\partial\varphi_s(v)}{\partial V_{gs}} \, dvdz \qquad -(4.16)$$

Using φ_s from [19]

$$\varphi_s(y) = V_{SL} + (V_{bi} + V_{DS} - V_{SL})\frac{\sinh\left(\frac{y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} + (V_{bi} - V_{SL})\frac{\sinh\left(\frac{L-y}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} \qquad -(4.17)$$

Where $$V_{SL} = V_{GS} - V_{fb} - \frac{qN_A}{\varepsilon}\lambda^2$$

And $$\lambda = \sqrt{\frac{\epsilon_{si}}{2\epsilon_{ox}}\left(1 + \frac{\epsilon_{ox}t_{si}}{\epsilon_{si}t_{ox}}\right)t_{si}t_{ox}}+$$

Using conformal mapping i.e. transforming (x, y) coordinates to (u, v) coordinates, i.e.

$$y = -fsinu.sinhv$$

As $u = \frac{\pi}{2}$ along y axis. Therefore,

$$y = -fsinhv$$

Now eq. (3.6) is modified to

$$\varphi_s(y) = V_{SL} + (V_{bi} + V_{DS} - V_{SL})\frac{\sinh\left(\frac{sinhv}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} + (V_{bi} - V_{SL})\frac{\sinh\left(\frac{L+fsinhv}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}$$

Now we can evaluate $\frac{\partial\varphi_s(v)}{\partial V_{gs}}$ term. i.e.

$$\frac{\partial\varphi_s(v)}{\partial V_{gs}} = 1 + \frac{\sinh\left(\frac{fsinhv}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} - \frac{\sinh\left(\frac{L+fsinhv}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}$$

Using trigonometry identity and eq. (4), we get:-

$$C = \frac{2\varepsilon}{\pi}\int_0^w\int_{v_1}^{v_2} 1 + \frac{2\sinh\left(\frac{L}{2\lambda}\right)\cosh\left(\frac{L+2fsinhv}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}dvdz$$

Integration of term $\cosh\left(\frac{L+2fsinhv}{\lambda}\right)$ is not possible. So, approximation is done using Taylor series expansion of $cosh$ function, i.e,

$$coshx = 1 + \frac{x^2}{2!} + \frac{x^4}{4!} + \cdots$$

$$\cosh\left(\frac{L+2fsinhv}{\lambda}\right) = 1 + \frac{\left(\frac{L+2fsinhv}{\lambda}\right)^2}{2!}$$

$$C = \frac{2\varepsilon}{\pi}\int_0^w \int_{v_1}^{v_2} 1 + \frac{2\sinh\left(\frac{L}{2\lambda}\right)\left(1 + \frac{\left(\frac{L+2fsinhv}{\lambda}\right)^2}{2!}\right)}{\sinh\left(\frac{L}{\lambda}\right)} dvdz$$

$$C = \frac{2\varepsilon}{\pi}\int_0^w \int_{v_1}^{v_2} 1 + \frac{2\sinh\left(\frac{L}{2\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\left(1 + \frac{1}{8\lambda^2}(L^2 + 4f^2sinh^2v + 2Lfsinhv)\right) dvdz$$

On Integrating above equation, we get,

$$C = \frac{2\varepsilon W}{\pi}\Bigg((v_2 - v_1) + \frac{2\sinh\left(\frac{L}{2\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}\Big((v_2 - v_1) + \frac{1}{8\lambda^2}(L^2(v_2 - v_1) + f^2(\sinh(2v_2) - \sin(2v_1)) - 2(v_2 - v_1)) + 2Lf(\cosh(v_2) - \cosh(v_1))\Big)\Bigg) \quad -(4.18)$$

To get capacitance expression in (x, y) coordinates, Inverse mapping is done. i.e.

$$v_2 = \sinh^{-1}\sqrt{\frac{\sqrt{x_1^2 + \min(x_2, y_2)^2 + 2y_1\min(x_2, y_2)}}{\sqrt{|x_1^2 - y_1^2|}}}$$

$$v_1 = \sinh^{-1}\sqrt{\frac{x_1}{\sqrt{|x_1^2 - y_1^2|}}}$$

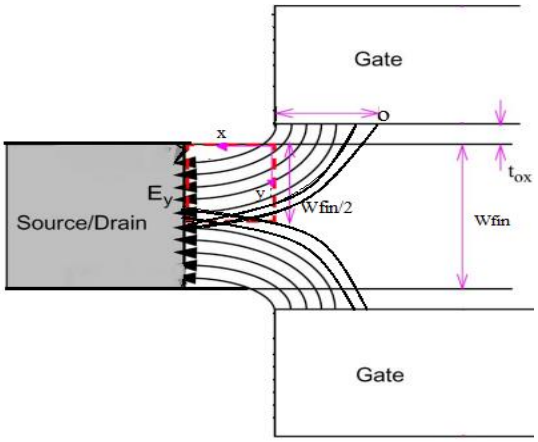


Fig. 4.8 Illustration of C_{ifSide} for mapping.

Referring fig. 4.7 Using mapping of coordinates C_{ifSide} (x_1, y_1, x_2, y_2)= (0,tox,$l/2$, $wfin/2$). And w= $hfin$ [1].

$$\therefore \quad v_2 = \sinh^{-1}\sqrt{\frac{\sqrt{\min(l/2, wfin/2)^2 + 2tox\,\min(l/2, wfin/2)}}{tox}}$$

$$\& \quad v_1 = 0$$

Hence, we get our C_{ifSide} (refer fig. 3.4) from 4.18 using v_2 and v_1 given above.

We have developed an analytical model for Outer and Inner Fringe parasitic capacitance. Now, we need to validate this. In Next chapter validation of our model is done.

Chapter 5

Result and Discussion

5.1 simulation setup,

The model is validated from simulation using sentaurus TCAD. A 3D Double gate FinFET structure is made with 25nm physical gate length, oxide thickness is 1.3nm, gate height and width is taken 25nm and S/D is 20nm and extended region is 20nm. Fig. 5.1 shows the image of the respective device in TCAD (all body is not shown).

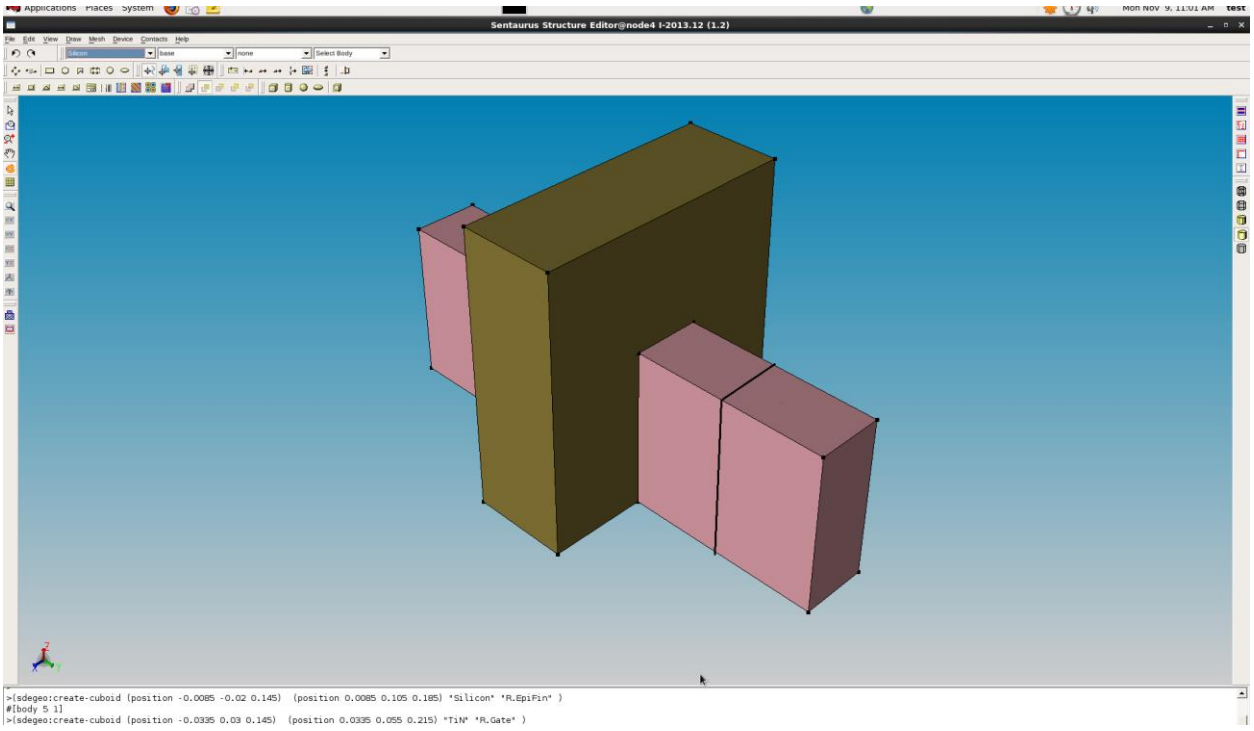


Fig. 5.1 FinFET device showing Gate, S/D and Extended region b/w gate and S/D.

Fig. 5.2 shows the image of the respective device in TCAD with doping profile. Here S/D are highly doped, extended region get Gaussian doping profile and channel region is lightly doped.

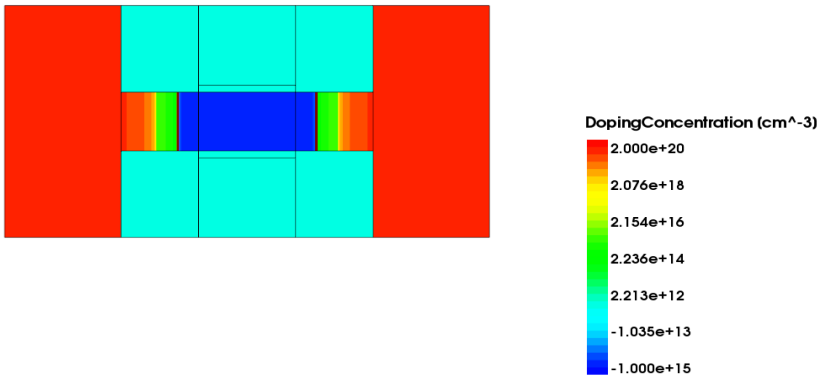
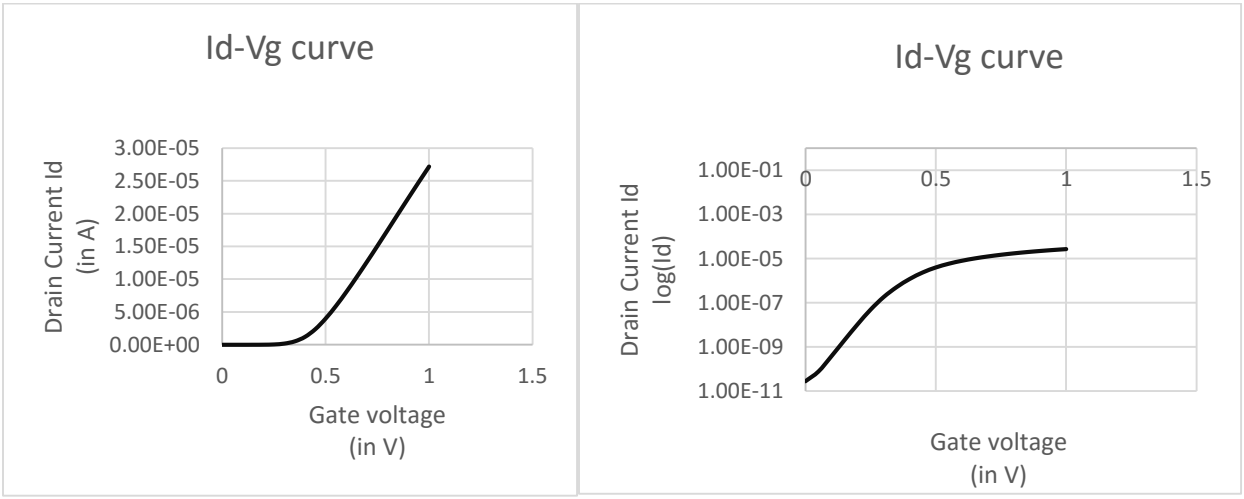


Fig. 5.2 FinFET device with doping profile in TCAD

The Id-Vd graph of our device is given below.



(a) (b)

Fig. 5.3 Drain current Vs. Gate voltage (a) in normal scale (b) in log scale.

On current of the device i.e. I_{on}=2.73e-5 Amp and I_{off}= 2.8e-11 Amp

Though simulation give the total gate capacitances, knowing the fact that at the nanoscale regime the parasitic gate capacitance are very much comparable to total gate capacitances, we first found the overall capacitance then by eliminating the factor, which could give rise to parasitic capacitance such as gate height and width i.e. firstly, we used negligible height (or width), found

overall capacitance then we increased height (or width) step by step (which will increase parasitic) and found another overall capacitances (this time parasitic due to increased height, fig 5.4,

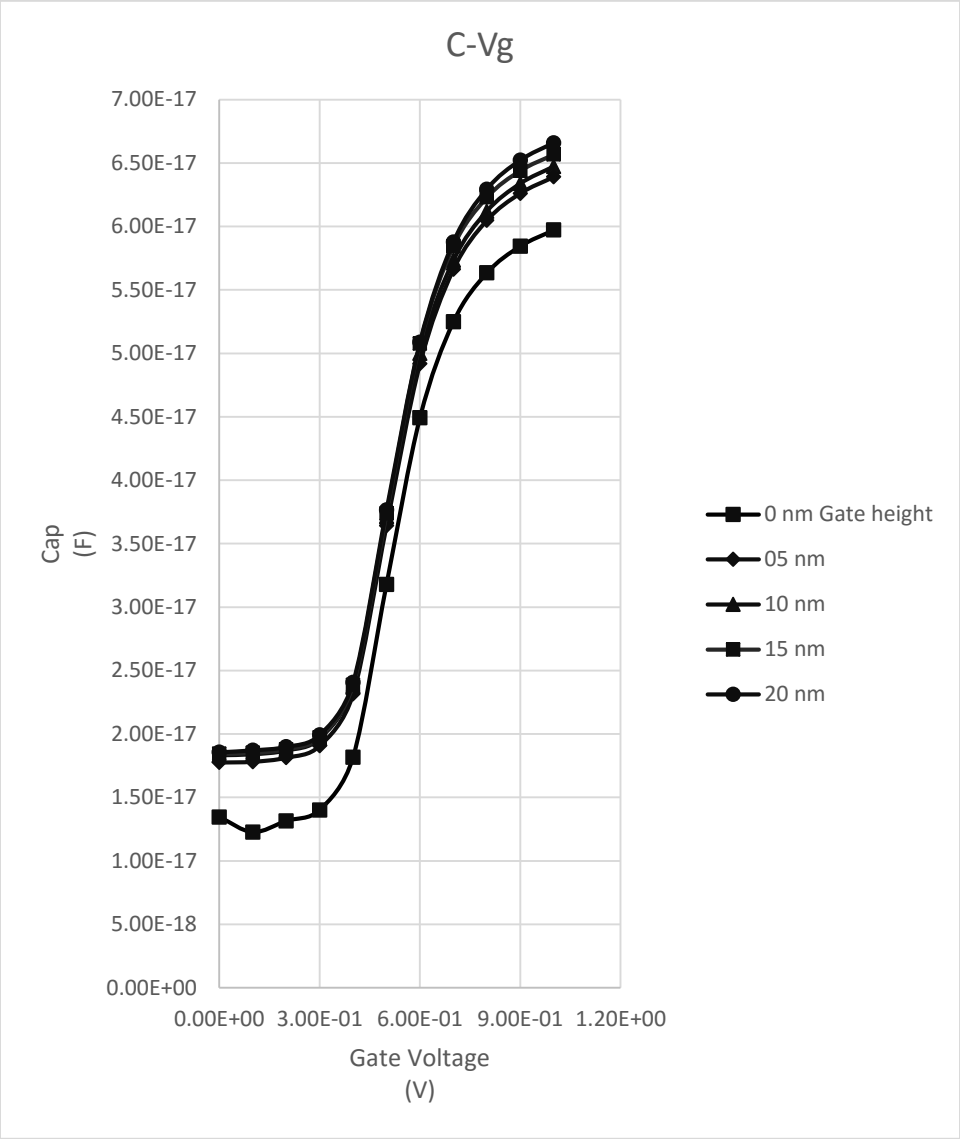


Fig. 5.4 Overall Capacitances with increased parasitic component due to increased Gate height.

(or width, fig. 5.5) also present) then finally we got our parasitic capacitance by doing subtraction of capacitances (larger one) from every increased step and initial i.e. negligible height (or width).

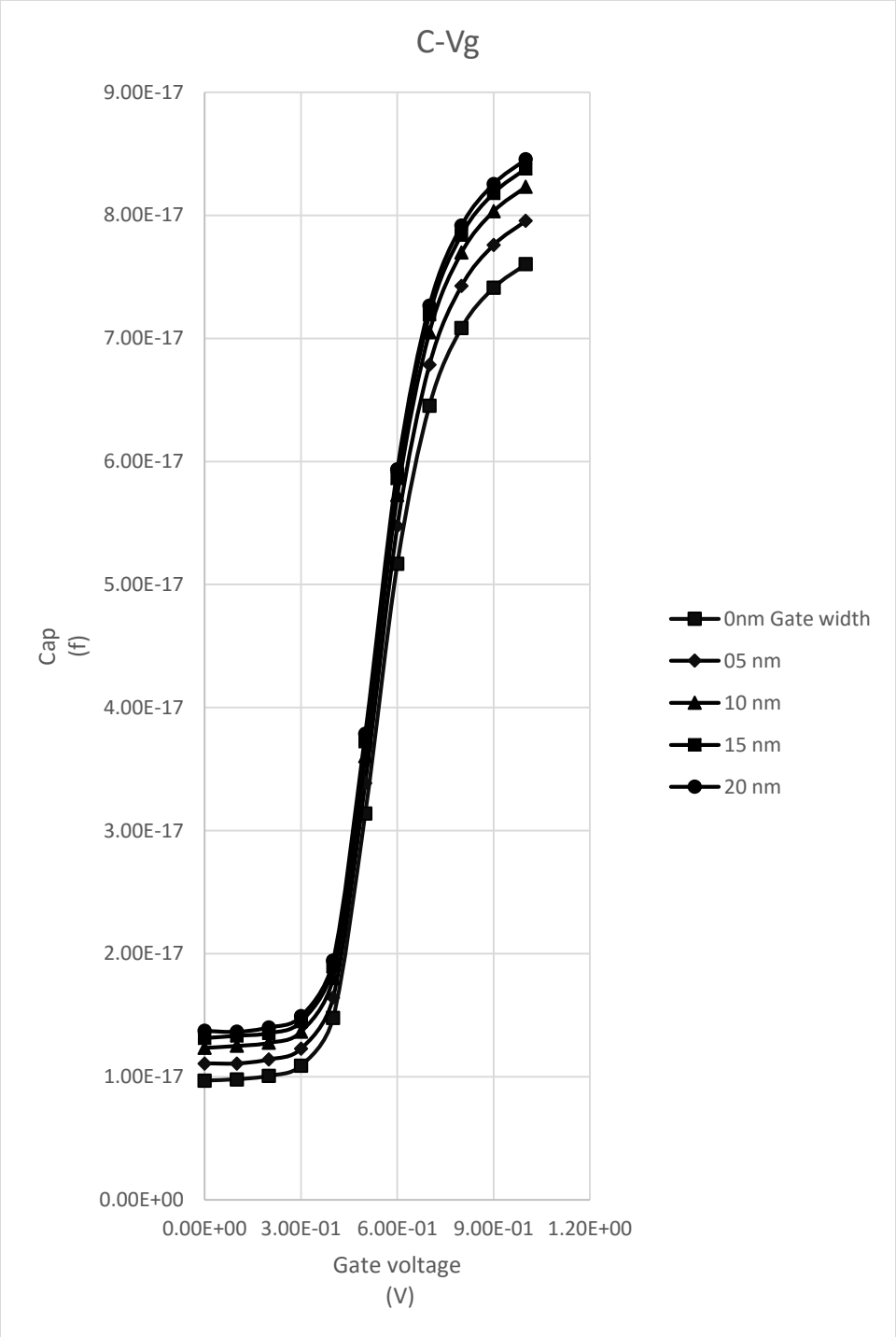


Fig 5.5 Overall Capacitances with increased parasitic component due to increased Gate width.

5.2 Results

For Outer Fringe Capacitances model is validated by matching simulation result with model result. Simulation result is obtained from the device with above mention specification using sentaurus TCAD. And model result is obtained from MATLAB. Then data from both i.e. simulated and model is presented as graph shown below.

5.2.1 Outer fringe capacitance

We have developed a model which shows outer fringe capacitance depends upon Gate height and Gate width. So, plot of outer fringe cap. with gate height and gate width variation from model and simulation is shown . Height of the gate electrode (Hg) is increased step wise. Fig. 4.5 shows comparison between modeled result and simulated result.

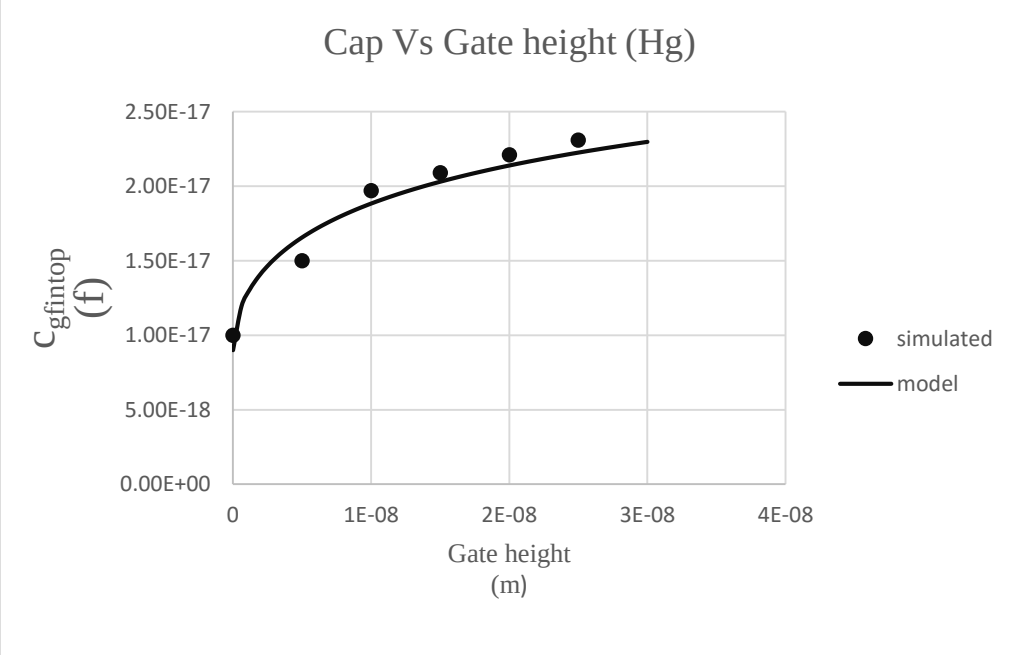


Fig. 5.6 Simulated and modelled capacitance $C_{gfinTop}$.

Above graph shows $C_{gfintop}$ (capacitance due to top of extended region (fin) b/w gate and S/D and gate wall at top of the fin, refer to fig. 3.3) variation with Gate height. It shows that with increase in gate height parasitic capacitance is increased. It can be used in determining the optimized gate height. Further, the graph shows a very good approximation between the parasitic capacitance from simulation and from the model.

The variation of $C_{gfinSide}$, (capacitance due to sidewalls of fin and gate sidewall, refer to fig. 3.3) with gate width is shown below.

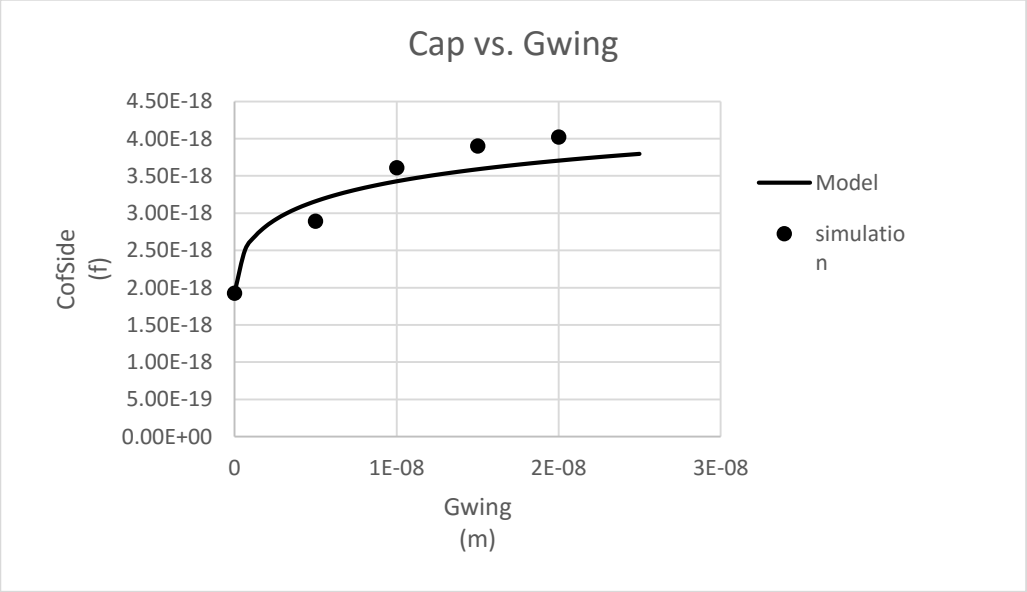


Fig. 5.7 Simulated and modelled capacitance $C_{gfinSide}$

It shows that with increase in gate width (G_{wing}) parasitic capacitance is increased. Also, the graph shows a very good approximation between the parasitic capacitance from simulation and from the model.

5.2.2 Inner fringe Capacitance

After modeling Outer fringe, we modeled Inner fringe capacitance. This is derived in weak inversion region i.e. neglecting inversion charges. It shows dependencies with fin thickness. To validate this derivation we have matched our result with Agrawal's model and simulation result. Plot of Inner fringe Capacitance with variation in fin thickness is shown next.

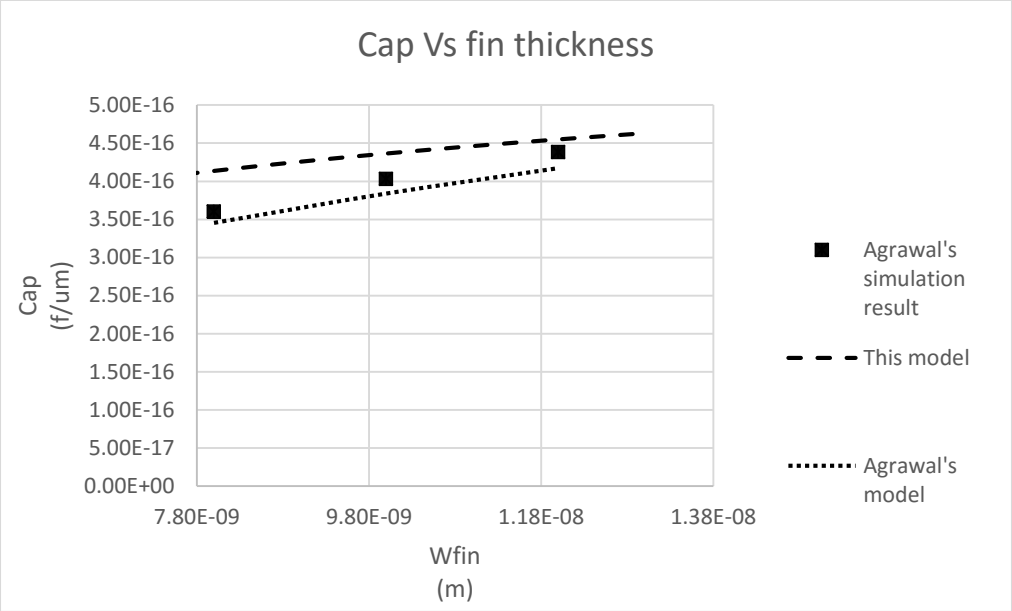


Fig. 5.8 Simulated and modelled capacitance C_{ifSide}.

Plot shows that with increase in fin thickness (Wfin) parasitic capacitance is increased. Also, the graph shows a very good approximation between the parasitic capacitance from simulation and from the model.

5.3 Significance of parasitic capacitance modeling in Memory design

As FinFET has been proved to be very effective candidate to replace conventional MOSFET to keep further scaling trend. It has shown many advantages in the context of circuit and device level. In SRAM memory design there are some performance parameter that cannot be boosted for better output by using Conventional MOSFET. For instance, the *hold stability* is highly dependent on the leakage current of the transistors. This leakage current is very less in FinFET providing greater Hold Margin. Other performance parameters i.e. *write Margin, Read Margin, Access time and Power* are also improved using FinFETs. It also improves speed. But In high frequency applications where speed requirement is of much important, theoretically value of parameter like unity gain frequency could be very large. But in practical scenario when parasitics come into picture that value drastically fall. More the parasitic lesser will be the unity gain frequency, hence, poorer will be the speed performance. So, to speed up things those parasitics have to be reduced to possible extent. V. Subramanian, *et.al* [20], has shown the effect of those parasitics fig. 4.9

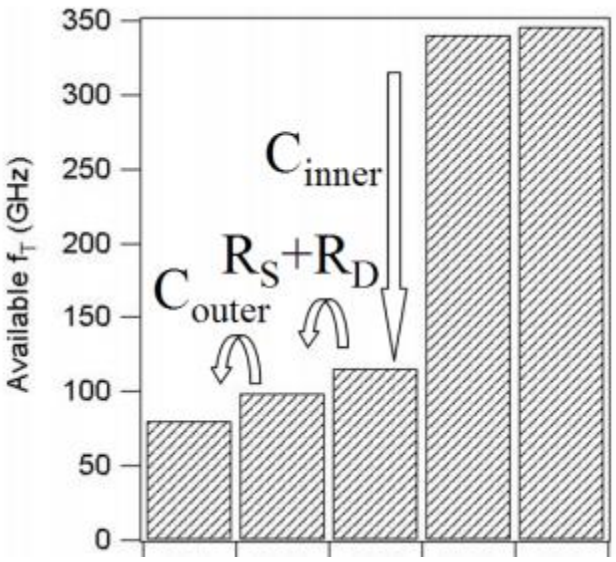


Fig. 5.9 Illustration of effect of parasitics on f_T [20]

The above result is obtained from 60 nm channel length FinFET. Similar effect can be seen with any technology node. Hence, an accurate model is always needed to account for those effects and get better prediction.

Chapter 6

Conclusion and Future Scope

Parasitic capacitances of FinFET have been extracted analytically by doing analytical modelling of parasitic capacitance of DG-FinFET using conformal technique and compared with the simulated results and they are found to be in very close agreement. Due to scaling down of the transistor the parasitic capacitance role in degrading the performance of the device especially in RF application. This model can be used for the analysis of high speed application design to predict the delay or f_T of that device As the model shows the parasitic capacitances dependence on geometrical parameters so it can be used to find optimize geometry of the device which can reduce delay leading to performance advantages in RF application. This model can also be adapted for the analysis of the applications where multifin FinFET is used.

This model does not shown bias dependency on parasitic component. But in practical scenario parasitics also get affected by Gate voltage. The method that is applied in this work to derive analytical model is likely to be used to get relation of parasitics with the bias voltage by using Poisson's equation in Strong inversion.

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