

MULTILAYER MICROMAGNETIC MODELS FOR ALL SPIN LOGIC

A DISSERTATION

*Submitted in partial fulfilment of the
requirements for the award of the degree*

of

MASTER OF TECHNOLOGY

in

ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Microelectronics & VLSI)

Submitted By

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CANDIDATE'S DECLARATION

I hereby declare that the work which is being presented by me in this dissertation report entitled “**Multilayer Micromagnetic Models for All Spin Logic**”, submitted in partial fulfillment of the requirement for the award of the degree of, “**Master of Technology in Electronics and Communication Engineering**” with specialization in “**Microelectronics and VLSI**”, and submitted to the Department of Electronics and Communication Engineering, Indian Institute of Technology, Roorkee, is an authentic record of the work carried out by me during the period June 2015 to May 2016, under the guidance of **Dr. B. K. Kaushik**, Associate Professor, Electronics and Communication Engineering Department, Indian institute of Technology, Roorkee and **Dr. Ashwin Tulapurkar**, Associate Professor, Electrical Engineering Department, Indian institute of Technology, Bombay.

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This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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Abstract

The complementary metal oxide semiconductor (CMOS) industry is successful in scaling according to Moore's law. The scaling has disadvantages in terms of short channel effects such as quantum mechanical tunnelling, mobility degradation, hot carrier effects, drain induced barrier lowering, etc. The spin based devices emerged as an energy efficient alternative to CMOS technology. The discovery of spin transfer torque effect has revolutionized the field of spintronics and has given a new dimension to the information storage and processing in the last decade. All Spin Logic (ASL), a class of spin based devices are studied in the report. ASL devices use spin current as medium for information transfer. The ferromagnets (FMs) are used as storage elements with the help of their magnetization state. The lumped and distributed spin circuit modeling of All Spin Logic Devices (ASLD) and universal gate structure is described. Also, multilayer structures are formed for ASLD and universal gate structure. The micromagnetic analysis of ASLD and universal gate structure is performed by capturing the spin transport and LLG dynamics in a tool command language (TCL) script to make it compatible with object oriented micromagnetic framework (OOMMF).

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Chapter 1

Introduction

1.1 Motivation

The idea of scaling has revolutionized the semiconductor industry. The advantages of present day CMOS devices are directly based on scaling using silicon technology. Scaling improves the performance parameters *i.e.*, reduction in dynamic power dissipation, area, delay. But, there are some short comings with scaling *i.e.*, short channel effects like quantum mechanical tunnelling, mobility degradation, hot carrier effects, drain induced barrier lowering, reliability problems, and also the power dissipation in the interconnects has been increasing. Thus, the need for discovery of an alternate state variable to the charge of electron came into picture.

Spintronics has emerged as one of the most promising technologies for the post CMOS era, which uses the spin of the electron and associated magnetic moment as the new state variable. The field of spintronics was revolutionized by the phenomenon of spin transfer torque (STT) effect, first demonstrated by J.C Slonczewski in 1996 [1]. After the discovery of STT effect, the novel concept of all spin logic devices (ASLDs) was introduced [2] for storage and processing of information. The ASL devices make use of electron spin for information transfer. The spin current is used as the medium for information transfer. The FMs are used as storage elements with their magnetization state. The ASL devices have important functionality of non-volatility. That means the information remains stored in FM even if supply voltage is turned off. ASLDs provide an alternate solution for non-volatile computing architecture. The ability of ASLDs to realize any combinational or sequential circuit makes them a potential contender for non-volatile architecture in the future.

1.2 Problem Statement

Since their discovery, ASLDs have attracted the interest of researchers. But, there are a lot of challenges regarding the architecture, modelling, and analysis of ASLDs. The ASLDs require channel with higher spin conductivity and FMs which act as injector as well as detector. Hence, extensive experimental and theoretical studies are being carried out for non-

local spin valve (NLSV) device with Si, GaAs, Cu, and graphene as a non-magnetic channel to transport spin polarized current. However, proportional efforts have not been directed towards the design of sender/receiver nano-magnets, which is equally essential.

The mathematical analysis of ASLD is done by using spin circuit model proposed by Srinivasan *et al.* [3]. But there is no simulation tool that can capture the spin transport and ferromagnetic properties simultaneously. Hence, the micromagnetic analysis of ASLDs is still developing phase. Thus, a micromagnetic analysis of ASLD and universal logic gates is presented in this report by developing a simulation framework that can promisingly capture the spin transport and LLG dynamics for switching.

Most studies have considered these nano-magnets to be having a single magnetic moment, *i.e.*, monodomain approximation [3]-[6]. Moreover, till date, no study has focused on analyzing the switching behaviour or constraints on physical dimensions of such nano-magnets. Hence, these nano-magnets which have a complex architecture are analyzed using an object oriented micromagnetic simulation framework (OOMMF).

In the proposed simulation framework, the diffusive spin transport is captured using tool command language (TCL). The TCL spin circuit model consists of lumped π equivalent networks for each region/interface of ASL enables compatibility with a micromagnetic simulator, *i.e.*, OOMMF. The proposed TCL spin circuit model is validated using experimental results on non local spin valves (NLSVs) and further used to perform device level analysis of an ASLD. In addition, clocked ASL copy and invert logic operations are performed. The proposed model can be further extended for ASL and universal gate circuit analysis.

1.3 Organization of the Report

The report is organized into six chapters including this first chapter which introduces the motivation for ASL and the problem statement. Chapter 2 introduces the basic concepts required to understand all spin logic. Chapter 3 explains the operation of ASLD along with lumped and distributed spin circuit modeling of ASLD. The architecture of universal gate structure using ASL is explained in chapter 4 along with lumped and distributed spin circuit model. The micromagnetic multilayer structures of ASLD and universal gates are described in chapter 5. The simulation parameters and results are also included in chapter 5. The conclusion and future scope is mentioned in chapter 6.

Chapter 2

All Spin Logic Devices

2.1 Basic Concepts of ASL

In this section, the basic concepts required to understand the functioning of ASL devices are explained in brief.

2.1.1 Spin Polarization in Ferromagnets

Electrons passing through normal metal (NM) film are scattered in the film and lose their original spin orientation. The scattering is independent of spin polarization of electrons. Statistically, electrons leaving a NM are made up of equal populations of two spins. When electrons enter a ferromagnetic (FM) layer from NM layer or leave a FM layer to go into NM layer, their spins are affected by ferromagnet. At the interface of FM and NM films, spin dependent scattering takes place.

2.1.2 Spin Torque Transfer (STT) Switching

The orbital electrons do not contribute to the electrical conductivity, but do interact with free electrons through the exchange of magnetic moment. Thus, spin of the free electron is polarized by the polarity of magnetization of FM film. This process can be reciprocal. If the stream of polarized electrons is injected into FM film, through the moment exchange, the polarization of the magnetization of the FM film may switch to the polarization of free electrons. The switching occurs when polarized electron current density is greater than the threshold value, which is taken of the order of mid- 10^6 to mid- 10^7 A/cm². This is called as STT switching or spin moment transfer switching. The concept of spin torque transfer switching was described by Slonczewski and Berger separately.

2.1.3 Landau–Lifshitz–Gilbert (LLG) Equation

The LLG equation is a differential equation describing the precessional motion of magnetization M in a solid. The LLG equation predicts the rotation of magnetization in response to the torques. The LLG equation [7] is given below.

$$\left(\frac{1}{\gamma}\right)\frac{d\vec{M}}{dt} = \vec{M} \times \vec{H}_{eff} - \alpha \frac{\vec{M}}{M} \times (\vec{M} \times \vec{H}_{eff}) \quad 2.1$$

where, \vec{M} is the magnetization.

γ is the electron gyromagnetic ratio.

\vec{H}_{eff} is the effective field.

α is the damping parameter.

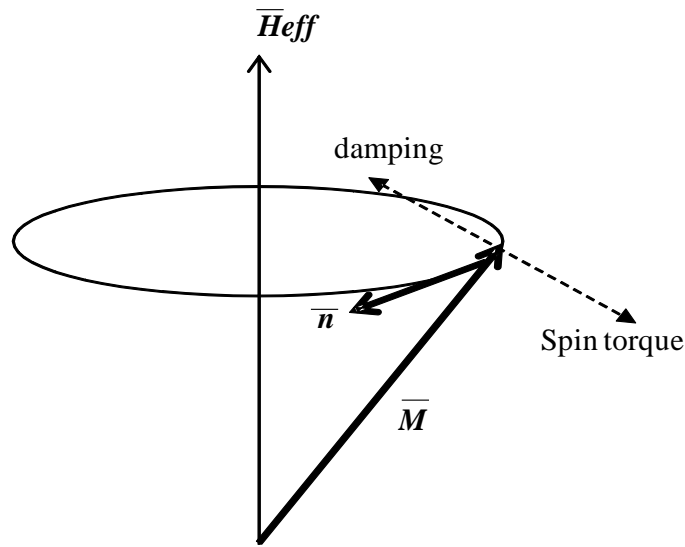


Fig 2.1: Precession of magnetization around effective field

The direction of $\vec{M} \times \vec{H}_{eff}$ is normal to the plane of \vec{M} and \vec{H}_{eff} . When $\alpha=0$, \vec{M} precesses continuously around \vec{H}_{eff} with the frequency $\omega=\gamma H$ as shown in Fig 2.1. The second term in the expression $\vec{M} \times (\vec{M} \times \vec{H}_{eff})$ represents a vector pointing from vector \vec{M} towards field vector \vec{H}_{eff} . When damping constant α is greater than zero, the precession gradually dissipates its energy and the precession cone angle θ decreases. Eventually, \vec{M} aligns to \vec{H}_{eff} .

If the torque exerted by the spin of the electron is considered, then the LLG equation is modified as

$$\frac{1}{\gamma} \frac{d\vec{M}}{dt} = \left(\vec{M} \times \vec{H}_{eff}\right) - \alpha \frac{\vec{M}}{M} \times \left(\vec{M} \times \vec{H}_{eff}\right) - \alpha_j \frac{\vec{M}}{M} \times \left(\vec{M} \times \vec{S}\right) \quad 2.2$$

As long as the spin torque does not attain a dominating value, the magnetization vector will precess around the effective field. The magnetization reversal will occur only if the spin torque exceeds a critical value.

2.2 Architecture and Operation of ASLD

An all-spin logic device (ASLD) consists of ferromagnets separated by a non-magnetic channel. A FM has concentration gradient of up and down spin electrons. We engineer FM in such a way that it has very high concentration of one kind of electrons, called as majority spin electrons. The FM aligns magnetization direction towards majority spin electrons along easy axis. The basic structure of ASLD [8] is shown in Fig 2.2. There are two types of FMs used. One is injector FM, which injects the electrons and other is detector FM, in which information is stored or transmitted. A tunnel barrier is placed at injector side. The tunnel barrier improves spin injection efficiency at injector side and reduces conductivity mismatch between FM and channel. The non-reciprocity is an important aspect in this structure i.e. output should be affected by input but not vice-versa. The non-reciprocity can be incorporated in ASL structure by keeping position of ground terminal near input side.

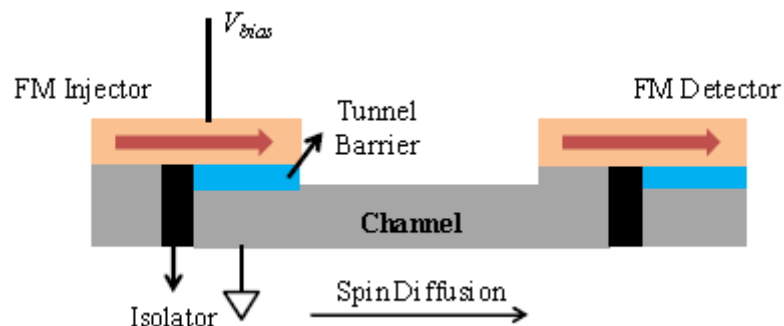


Fig 2.2: Basic structure of an ASLD

The detector FM either copies or inverts the magnetization state of injector FM depending on polarity of applied voltage at injector side, V_{BIAS} . If V_{BIAS} is negative, the injector FM acts as source for majority spin electrons. The majority spin electrons will diffuse through the channel towards detector FM. The majority spin electrons will exert spin torque on detector FM. If concentration of these majority spin electrons is greater than threshold value, magnetization state of injector FM is copied into detector FM.

If V_{BIAS} is positive, the injector FM acts as sink for majority spin electrons. Therefore, the minority spin electrons will diffuse through the channel towards detector FM. The minority spin electrons will exert spin torque on detector FM. If concentration of these minority spin electrons is greater than threshold value, magnetization state of detector FM is inverted with respect to injector FM.

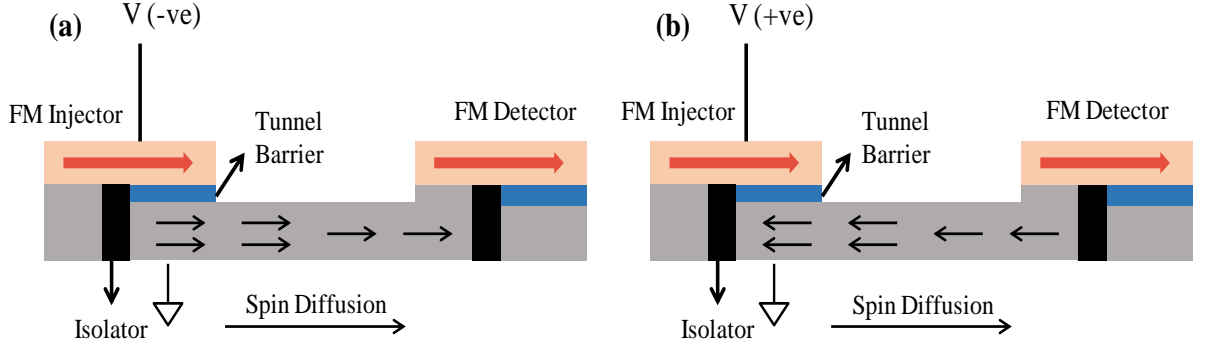


Fig 2.3: (a) Copy and (b) Invert operation of ASLD

2.3 TCL Lumped Spin Circuit Model

The lumped spin circuit model for ASLD is shown in Fig 2.4. The spin circuit is formed on the basis of connections in the structure shown in Fig 2.2. GA1 and GA2 represent conductance for gold contacts of injector and detector side respectively. GF1 and GF2 represent conductance of injector and detector FMs respectively. GC1 represent conductance for grapheme channel. GI1, GI2, GI3 are interface conductance. Tunnel barrier is used as interface between FM and channel because of its high injection efficiency. Also, tunnel barrier reduces conductance mismatch between FM and channel. GG1 represents conductance for ground contacts. Each conductance element is realized as a π -network as shown in Fig 4.3. Supply voltages are given to node 1 while node 8 is output node. Depending upon polarity of applied voltage, copy or invert operation is performed. As spin circuit model consists of 9 nodes, 9×9 conductance matrix is formed. Voltages are found at each node. We are using TCL (Tool Command Language) coding for finding current (I) at each node using following equation.

$$[I] = [G] * [V] \quad 2.3$$

where, $[G]$ is the conductance matrix.

[V] are the node voltages.

The expressions for contact, FM, tunnel barrier, ground conductance and modified nodal analysis is explained later in the thesis.

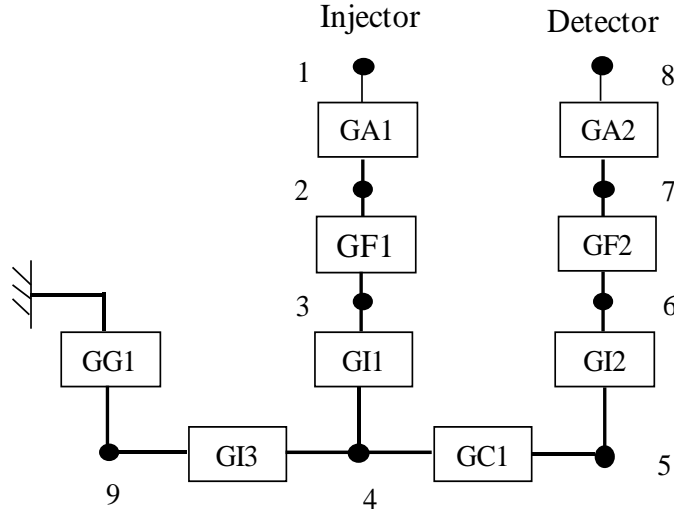


Fig 2.4: Lumped Spin Circuit Model for ASLD

2.4 TCL Distributed Spin Circuit Model

The distributed spin circuit model for ASLD is shown in Fig 2.5. In the distributed approach, each FM is divided into small parts along the width. The nodes 1, 5, 9 and so on correspond to the conductance for gold contacts. Nodes 2,6,10 and so on correspond to FM conductance. Nodes 3, 7, 11 and so on correspond to the tunnel barrier conductance. The ground contact will always remain at node 4. The nodes 1 to $N*4$ represent conductance blocks on the injector side while nodes $N*4+1$ to $N*8$ represent conductance blocks on the detector side. The voltage is applied to the 1, 5, 9..., $N*4$ nodes. The polarity of applied voltage will decide whether copy or invert operation is performed. The total detector current is sum of the current in all the output branches. The distributed spin circuit provides accurate results. Higher the number of nodes better is the accuracy.

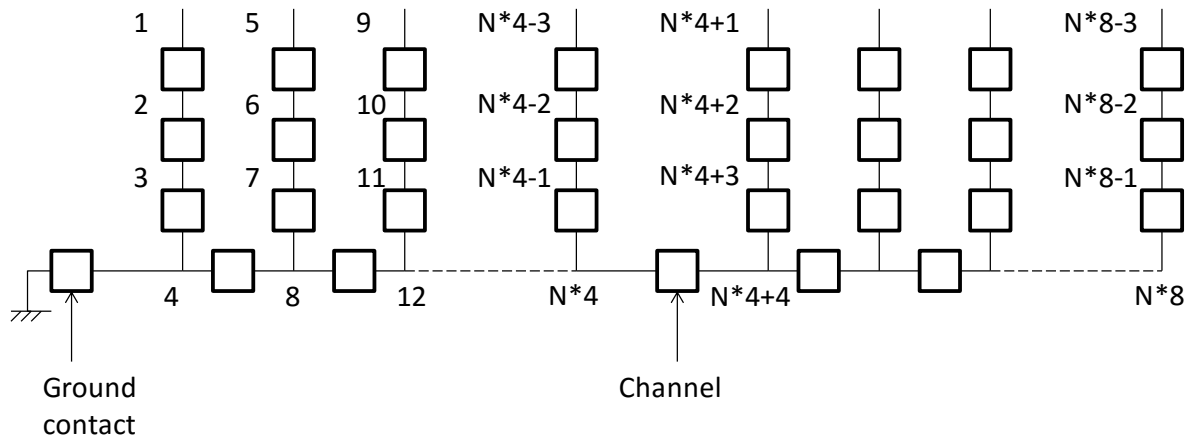


Fig 2.5: Distributed Spin Circuit Model for ASLD

2.5 Effect of Influence Area

As FM is acting as injector as well as detector, the entire length of FM is not available for injection or detection. For the accurate analysis of ASLD, the fact that the influence area (IA) is smaller than the detector area needs to be taken into account. Hence, the entire area of the detector can be divided into the IA, the area occupied by the isolator and the spin injection area (SIA) as shown in Fig 2.6. Especially, in case of an ASLD with tunnel contacts at the injector, SIA is an important factor as it also determines the resistance of the tunnel junction. The resistance of the tunnel junction determines the spin injection efficiency and the amount of diffusion current reaching the detector which is responsible for STT switching.

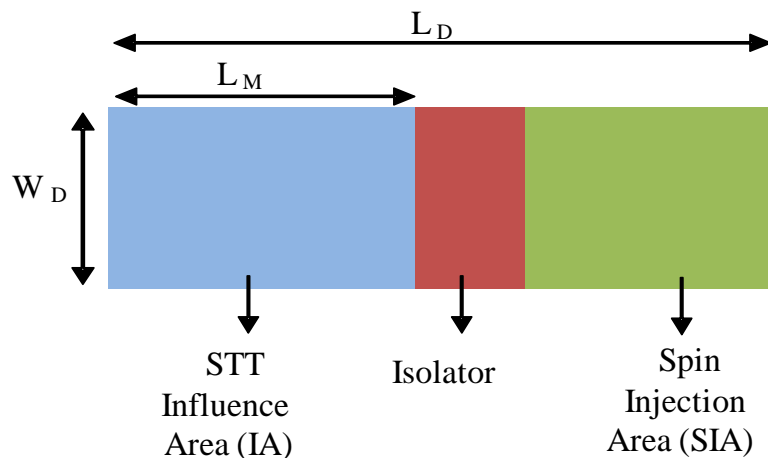


Fig 2.6: Regions across FM

Chapter 3

Universal Logic Gates using ASL

3.1 Architecture and Operation

ASLD is a spin based device consisting of nanoscale ferromagnets (FMs) connected through a non magnetic channel. The spin polarized electrons are generated by FM injector and diffuse through the channel and sensed by FM detector. The architecture of a universal logic gate is shown in Fig 3.1. AND, NAND, OR, NOR gates can be realized using the universal logic gate. The polarity of supply voltage (V_{DD}) and magnetization direction of the control input ($FM_{control}$) decide which logic gate is to be performed. The universal gate operates on the principle of Majority Gates (MG) [4]. The output current of a majority gate is superposition of input currents. A MG gate always has odd number of inputs to avoid the tie in case of equal and opposite number of input currents. In a three input MG based universal gate, FM_1 , FM_2 are two inputs and one $FM_{control}$ control input. The polarization of each FM is directed along the Z-axis, i.e., either UP (along positive Z-axis) or DOWN (along negative Z-axis). Depending on the polarity of applied voltage (V_{DD}), the ASLD performs either copy or invert operation. During copy operation, V_{DD} is negative and FM injector acts as a source of majority spin electrons, which are transmitted diffusively through the channel due to a concentration gradient of spins along the channel. Above a critical threshold value, this spin polarized current can copy the magnetization state of the FM injector into a detector. Similarly, during invert operation, V_{DD} is positive and FM injector acts as a sink for majority spin electrons. The minority spin electrons travel diffusively through the channel and change the magnetization state of the detector opposite to the injector. The polarization of $FM_{control}$ switches the realization from NAND/NOR to AND/OR operations. The spin currents from each input FM are diffused from respective injector FM towards the detector FM. At the output node, the detector/output spin current depends on the superposition of input spin currents from three branches due to the spin diffusion along the channel from the each injector FM to detector FM. The output spin current exerts STT (Spin Transfer Torque) on detector nanomagnet. The switching of detector FM is made if the output detector current produces STT beyond the threshold value. The operations performed with respect to polarity of supply voltage and $FM_{control}$ can be understood from Table 4.1.

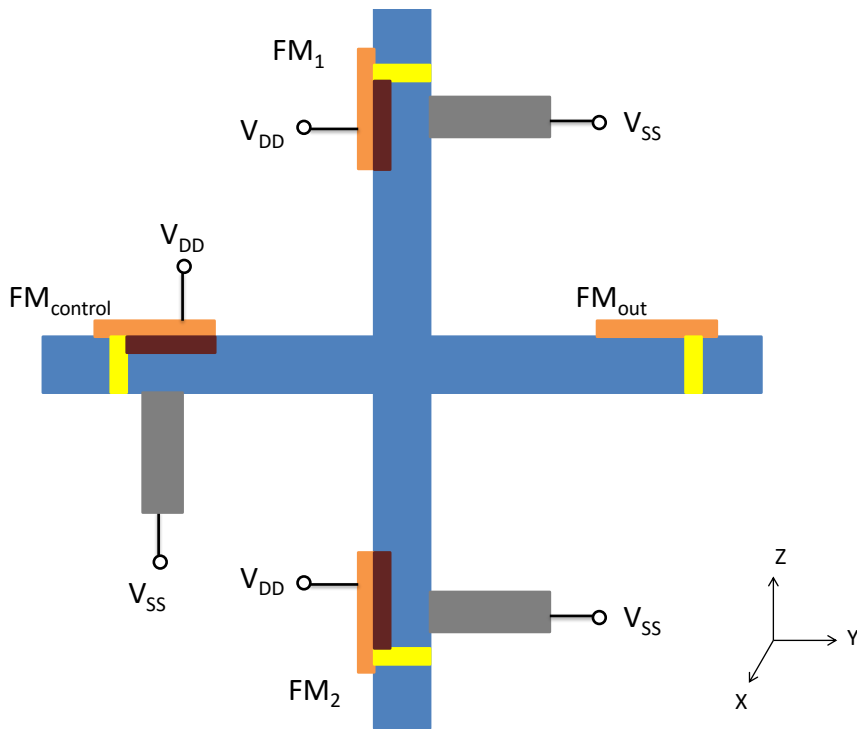


Fig 3.1: Circuit Representation of universal gates using ASL

Table 3.1: Truth Table for Universal Gate Structure

FM _{control}	FM ₁	FM ₂	FM _{out}			
			Positive V _{DD}	Negative V _{DD}		
Down	Down	Down	Up	NAND	Down	AND
Down	Down	Up	Up		Down	
Down	Up	Down	Up		Down	
Down	Up	Up	Down		Up	
Up	Down	Down	Up	NOR	Down	OR
Up	Down	Up	Down		Up	
Up	Up	Down	Down		Up	
Up	Up	Up	Down		Up	

3.2 TCL Lumped Spin Circuit Model

The lumped spin circuit model for Fig 3.1 is shown in Fig 3.2. For constructing spin circuit model, each component in universal logic gate circuit is represented as 4-component conductance matrix. Also, each conductance component can be represented in terms of series (G_{se}) and shunt (G_{sc}) conductances as shown in Fig 3.3. The 4-component model is used to represent 1 charge component and 3 spin components. As seen from spin circuit model, notations G_A , G_{FM} , G_{FM}/G_{NM} , G_{NM} , G_G are used for conductance matrices for contact, FM, interface, channel, ground contact respectively. Supply voltages are given to nodes 1, 5, 9 while 17 is output node. The spin currents get added at node 13 and resulting spin current will be responsible for transmission of information at output FM. As spin circuit model consists of 17 nodes, 17*17 conductance matrix is formed. Voltages are found at each node. We are using TCL (Tool Command Language) coding for finding current (I) at each node using following equation.

$$[I] = [G] * [V] \quad 3.1$$

where, $[G]$ is the conductance matrix.

$[V]$ are the node voltages.

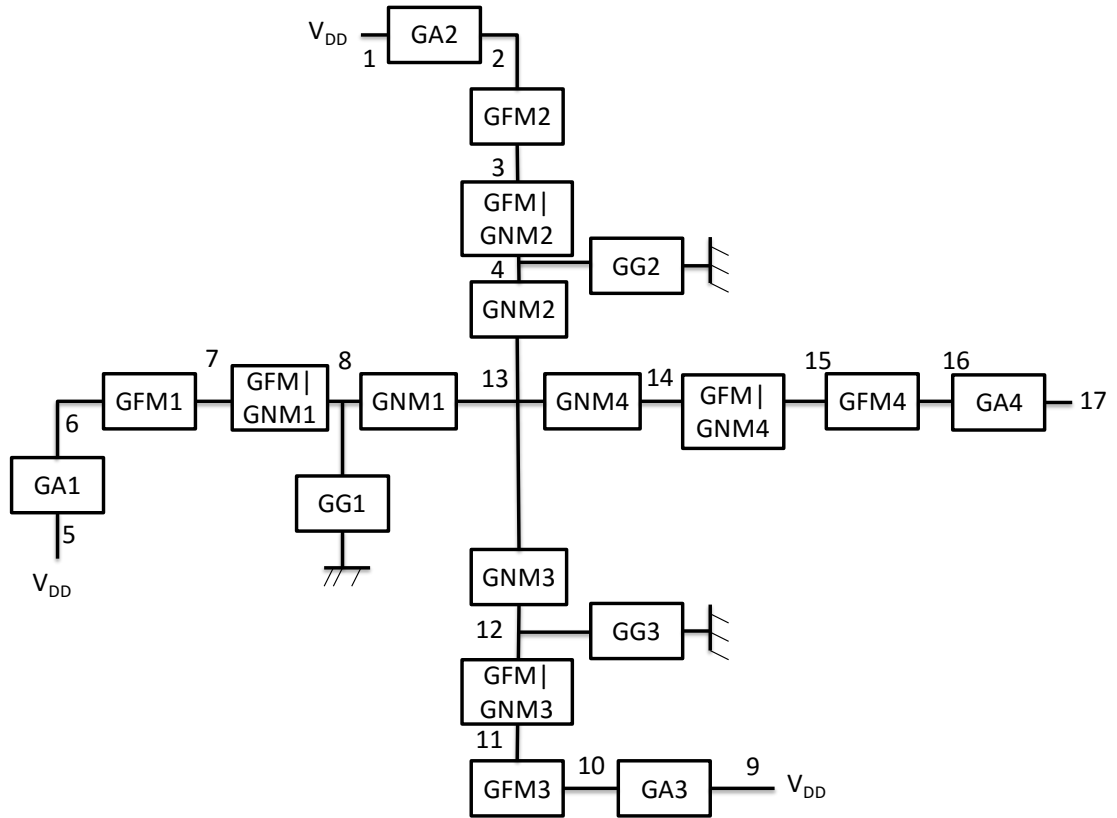


Fig 3.2: Lumped Spin Circuit Model for Universal Gate Structure

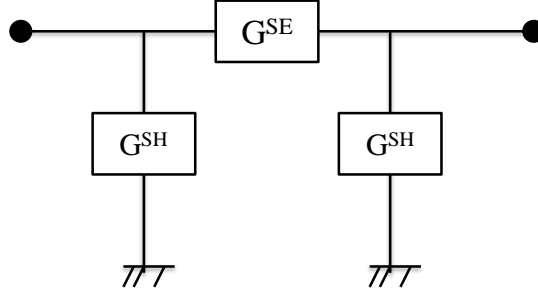


Fig 3.3: Representation of conductance element in spin circuit

The conductance matrices for FM region [13] are given as

$$G_{se} = \frac{A}{\rho l} \begin{pmatrix} 1 & p & 0 & 0 \\ p & p^2 + \alpha \operatorname{csc} h\left(\frac{L}{\lambda_{sf}}\right) & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \quad G_{sh} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & \left(\frac{A}{\rho L}\right) \alpha \operatorname{tanh} h\left(\frac{L}{2\lambda_{sf}}\right) & 0 & 0 \\ 0 & 0 & g'_{sf} & 0 \\ 0 & 0 & 0 & g'_{sf} \end{pmatrix} \quad 3.2$$

where

$$\alpha = (1 - p^2) \left(\frac{L}{\lambda_{sf}}\right)$$

The conductance matrices for tunnel barrier are given as

$$G_{se} = \frac{q^2}{h} M \begin{pmatrix} 1 & p & 0 & 0 \\ p & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \quad G_{sh} = \frac{q^2}{h} M \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & a & b \\ 0 & 0 & -b & a \end{pmatrix} \quad 3.3$$

Where, a=1 and b=0 for ohmic interfaces. Considering the spin mixing conductance [10], the equation for series conductance of tunnel barrier is modified as

$$G_{se} = \frac{q^2}{h} M \begin{pmatrix} 1 & p & 0 & 0 \\ p & 1 & 0 & 0 \\ 0 & 0 & G_{SL} & G_{FL} \\ 0 & 0 & G_{FL} & G_{SL} \end{pmatrix} \quad 3.4$$

Where, G_{SL} and G_{FL} are spin mixing conductance. G_{SL} lies in the range of $0.55e15$ to $5.5e15$, while G_{FL} is taken as zero.

The conductance matrices for the non-magnetic channel are given as

$$G_{se} = \frac{A}{\rho l} \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & \left(\frac{L}{\lambda_{sf}}\right) \csc h\left(\frac{L}{\lambda_{sf}}\right) & 0 & 0 \\ 0 & 0 & \left(\frac{L}{\lambda_{sf}}\right) \csc h\left(\frac{L}{\lambda_{sf}}\right) & 0 \\ 0 & 0 & 0 & \left(\frac{L}{\lambda_{sf}}\right) \csc h\left(\frac{L}{\lambda_{sf}}\right) \end{pmatrix} \quad 3.5$$

$$G_{sh} = \frac{A}{\rho l} \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & \left(\frac{L}{\lambda_{sf}}\right) \tanh\left(\frac{L}{\lambda_{sf}}\right) & 0 & 0 \\ 0 & 0 & \left(\frac{L}{\lambda_{sf}}\right) \tanh\left(\frac{L}{\lambda_{sf}}\right) & 0 \\ 0 & 0 & 0 & \left(\frac{L}{\lambda_{sf}}\right) \tanh\left(\frac{L}{\lambda_{sf}}\right) \end{pmatrix} \quad 3.6$$

After computing the conductance for individual components in the circuit, the overall conductance matrix is obtained as shown.

$$G = \begin{pmatrix} G_{F1} + G_{OF1} & -G_{F1} & \dots & 0 & 0 \\ -G_{F1} & G_{F1} + G_{OF1} + G_{T1} & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & G_{N1} + G_{ON1} + G_{T4} & -G_{T4} \\ 0 & 0 & \dots & -G_{T4} & G_{T4} + G_{F4} + G_{OF4} \end{pmatrix} \quad 3.7$$

The generalized lumped spin circuit representation of each region is shown in Fig. 3.1(b). The spin and charge component of the current are expressed as

$$\begin{bmatrix} I_c \\ I_{sx} \\ I_{sy} \\ I_{sz} \end{bmatrix} = \begin{bmatrix} G^{se} \end{bmatrix}_{4 \times 4} \begin{bmatrix} \Delta V_c \\ \Delta V_{sx} \\ \Delta V_{sy} \\ \Delta V_{sz} \end{bmatrix} + \begin{bmatrix} G^{sh} \end{bmatrix}_{4 \times 4} \begin{bmatrix} 0 \\ V_{sx} \\ V_{sy} \\ V_{sz} \end{bmatrix} \quad 3.8$$

where c and s subscripts are used to indicate spin and charge quantities respectively. ΔV corresponds to the voltage drops across the region; G^{se} and G^{sh} are (either 2x2 or 4x4) series and shunt conductance matrices, respectively.

Node current and voltages are calculated using simple nodal analysis and conductance matrix as

$$\begin{bmatrix} I_1 \\ I_2 \\ \cdot \\ \cdot \\ I_{17} \end{bmatrix} = [G]_{total} \begin{bmatrix} V_1 \\ V_2 \\ \cdot \\ \cdot \\ V_{17} \end{bmatrix} \quad 3.9$$

Each node current and voltage has two components, *i.e.*, charge and spin. The model is converted into TCL to make it compatible with OOMMF. The spin resistances of the three regions and spin polarization of FM controls the net conductance matrix $[G]_{total}$.

The modified nodal analysis [11] is used to calculate unknown node voltages by using the following equation.

$$[X] = [A]^{-1} [Z] \quad 3.10$$

Where, $[X]$ is the matrix consisting of unknown node voltages and currents through voltage sources. $[A]$ is the matrix consisting of known conductance matrices and values based on the connections of voltage and current sources. $[Z]$ is the matrix consisting of voltages and currents of voltage and current sources respectively.

The matrix A is given by

$$[A] = \begin{bmatrix} G & B \\ C & D \end{bmatrix} \quad 3.11$$

If n is the number of nodes in spin circuit model and m is number of independent voltage sources, A is matrix of size $(m+n) \times (m+n)$. G is the matrix of size $n \times n$ which depends upon connections of passive elements. B is the matrix of size $n \times m$ which is determined by position of voltage sources. C is the matrix of size $m \times n$ which is also determined by position of voltage sources. If only independent voltage sources are connected in the circuit then C is transpose of B . D is the matrix of size $m \times m$ and is zero if only independent sources are placed in the circuit. Each element in the A matrix is of size 4×4 as 4-component approach is used.

The matrix Z is of size $(m+n) \times 1$ which is given by

$$[Z] = \begin{bmatrix} i \\ e \end{bmatrix} \quad 3.12$$

Where, i is the matrix of size $n \times 1$ consisting of sum of currents through the passive elements into the corresponding node and e is the matrix of size $m \times 1$ which contains values of independent voltage sources.

The matrix X is of size $(m+n) \times 1$ which contains unknown quantities given by

$$[X] = \begin{bmatrix} V \\ j \end{bmatrix} \quad 3.13$$

Where, V is the matrix of size $n \times 1$ consisting of unknown voltages at each node and j is the matrix of size $m \times 1$ consisting of unknown currents through the voltage sources. All the elements of matrices A , Z and X are of size 4×4 as 4-component approach is used. Using modified nodal analysis, the voltages at each node are determined. Each node will correspond to four node voltages, viz., one charge component and three spin components. The detector current is found by the equation given as

$$I_D = ([V(15)] - [V(16)]) \times GF4 + [V(15)] \times GOF4 \quad 3.14$$

Where, $V(15)$ and $V(16)$ are 1×4 voltage matrices at FM nodes 15 and 16 respectively. The $GF4$ and $GOF4$ are 4×4 series and shunt conductance matrices of detector FM. That means, the detector current (I_D) is a 1×4 matrix consisting of a charge current component and three spin current components.

3.3 TCL Distributed Spin Circuit Model

The distributed spin circuit for universal logic gate structure is shown in Fig 3.4. In the distributed approach, the FM is divided into many parts along the width. As seen from lumped spin circuit model in Fig 3.3, there are four nodes in a branch. If we divide a FM into N parts along the width, we will have $4*N$ nodes in a branch in distributed model as shown. That means, gold contact and tunnel barrier is also divided into N parts along with FM. The

voltage is applied to the nodes corresponding to the gold contacts i.e. nodes 1, 5, 9 and so on. The current is measured across all the branches in the output branch. The overall detector current is the sum of currents in all the output branches. The distributed approach provides more accuracy than the lumped approach. Higher the number of nodes better is the accuracy.

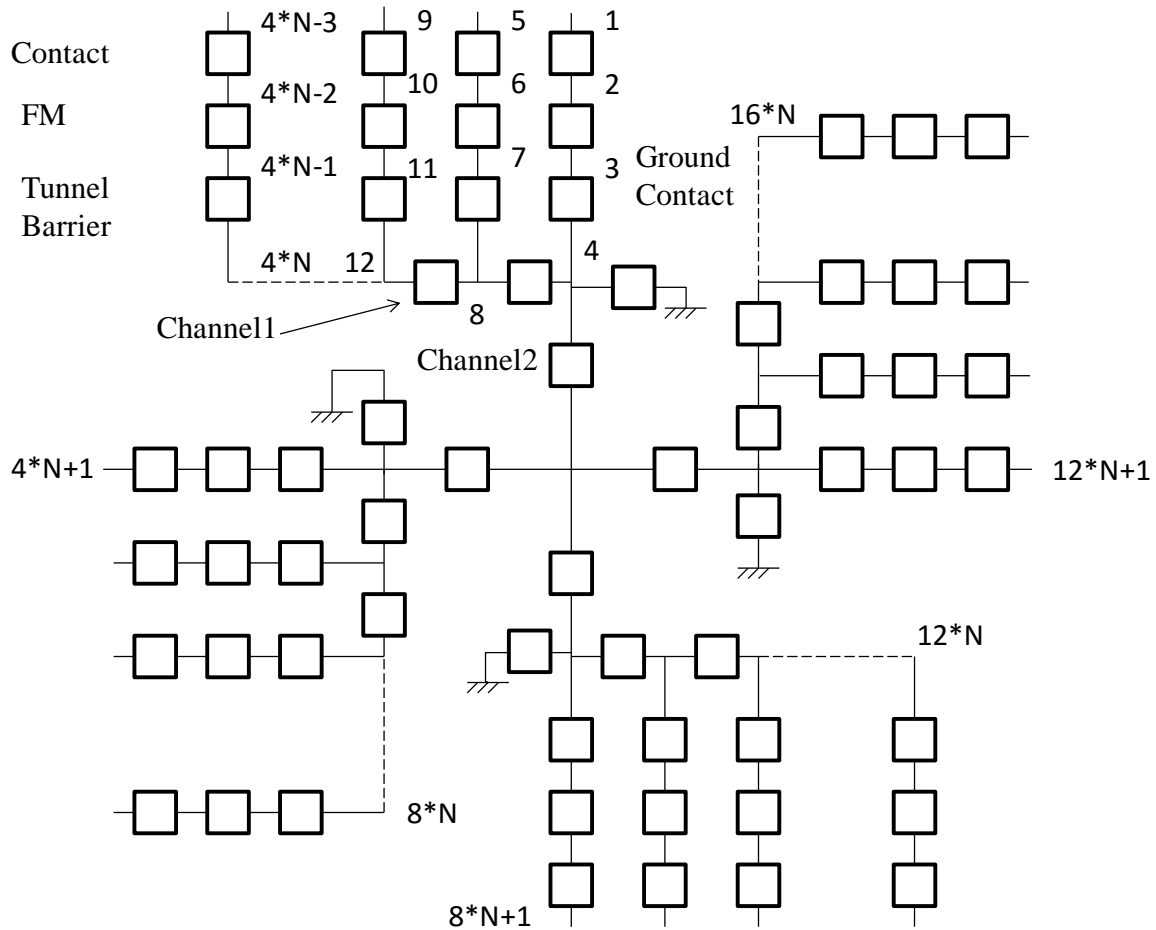


Fig 3.4: Distributed Spin Circuit Model for Universal Gate Structure

Chapter 4

Micromagnetic Models

4.1 Multilayer ASL structure

The all spin logic device (ASLD) shown in Fig 2.2 is represented as multilayer structure as shown in Fig 4.1. As seen from the figure, there are three layers, viz., Injector, Spacer and Detector. The layers are formed along the thickness. The Injector layer consists of gold contact, injector FM and tunnel barrier. The Spacer layer consists of the graphene channel. The Detector layer consists of the detector FM. The voltage is applied to the Injector layer. Depending upon polarity of the applied voltage, copy or invert operation is performed. If negative voltage is applied to the Injector layer, the majority spin electrons will be passed through the injector FM. The majority spin electrons will diffuse through the Spacer layer. These majority spin electrons will exert torque on the Detector FM layer. If current density due to the majority spin electrons exceeds the threshold value (mid- 10^6 to mid- 10^7), the magnetization state of Injector layer is copied into Detector layer. On the other hand, if positive voltage is applied to the Injector layer, there will be accumulation of minority spin electrons below the injector FM. The minority spin electrons will diffuse through the channel towards Detector layer. The minority spin electrons will exert spin torque on the detector FM. If current density due to minority spin electrons exceeds the threshold value, the magnetization state of Detector layer is inverted with respect to the magnetization state of Injector layer.

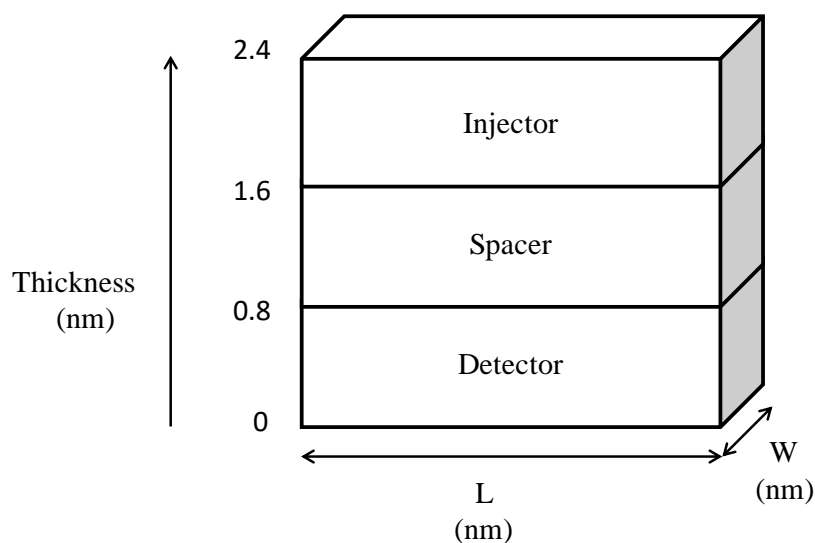


Fig 4.1: Multilayer structure for ASLD

Table 4.1: Simulation Parameters

Sr. No.	Symbol	Parameter	Value
1	M_S	Saturation magnetization of FM	900×10^3 A/m
2	A	Exchange constant of FM	30×10^{-12} J/m
3	L	Length of FM	100 nm
4	W	Width of FM	50 nm
5	T	Thickness of FM	0.8 nm
6	X_{ycell}	Cell Size	5 nm
7	$RT1, RT2, RT3$	Resistance of interface at injector	3 k Ω
8	$RT4$	Resistance of interface at detector	0.3 k Ω
9	L_N	Length of the channel	200 nm
10	σ_{CH}	Channel conductance	1.25×10^{-3} mho
11	λ_{CH}	Channel spin relaxation length	2.8 μ m
12	L_{AU}	Length of gold contact	5 nm
13	λ_{AU}	Spin relaxation length of gold contact	10 nm
14	ρ_{AU}	Resistivity of gold contact	70 n Ω -m
15	PF	Polarization of FM	0.5
16	ρ_{FM}	Resistivity of FM	60 n Ω -m
17	λ_{FM}	Spin relaxation length of FM	60 nm
18	PT	Polarization of interface	0.4
19	L_{Gnd}	Length of ground contact	10 m
20	ρ_{Gnd}	Resistivity of ground contact	100 μ Ω -m

4.2 Multilayer universal gate structure using ASL

The universal gate structure using ASL shown in Fig 3.1 is represented as multilayer structure as shown in Fig 4.2. As seen from figure, there are five layers, viz., Detector, Spacer, Injector1, Injector2 and Injector3. The layers are formed along the thickness. The

Injector1 and Injector3 layers consist of two gold contacts, two FMs corresponding to two logic inputs and two tunnel barriers. The Injector2 layer consists of a gold contact, a FM corresponding to control input and a tunnel barrier. The Spacer layer consists of graphene channel. And the Detector layer consists of detector/output FM. The AND, NAND, OR, NOR operations are performed by changing polarity of supply voltage and the control input magnetization state. The magnetization state of the FMs is taken along z-direction. If magnetization state of control input (Injector2 layer) is DOWN (negative z-direction), NAND operation is performed for positive supply voltage while AND operation is performed for negative supply voltage. On the other hand, if magnetization state of control input (Injector2 layer) is UP (positive z-direction), NOR operation is performed for positive supply voltage while OR operation is performed for negative supply voltage.

The critical switching current for each combination of universal gate is shown in table 4.2. Critical switching current is the minimum injector current at which complete magnetization switching is observed in the detector FM. As seen from the table, critical switching current varies from 100 μA to 500 μA which is equivalent to the supply voltage of 0.54 V to 2.66 V. For simulation purpose, the supply voltage (injector current) is kept 2.66 V (500 μA). Table 4.3 shows the values of spin current at the detector FM. For the values of detector spin current shown in Table 4.3, the detector FM switches its magnetization state for all logic combinations.

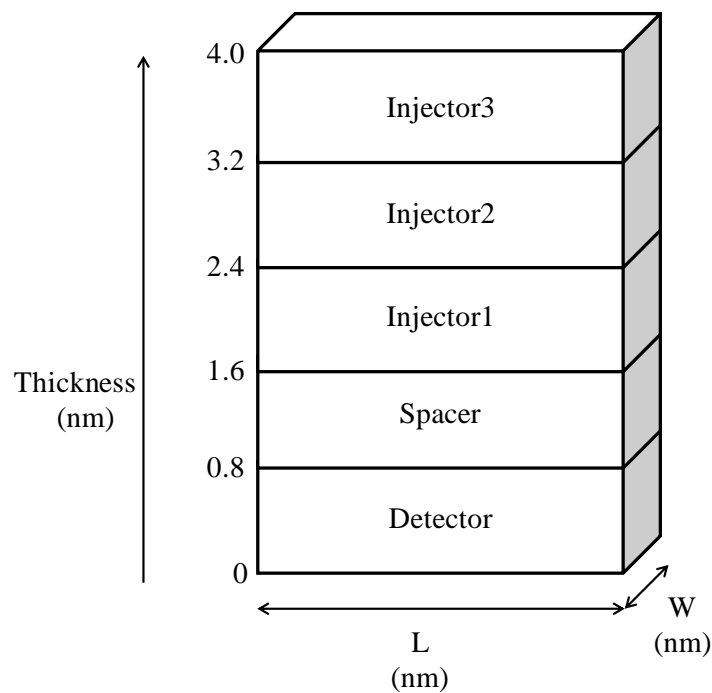


Fig 4.2: Multilayer universal gate structure using ASL

Table 4.2: Critical Switching Current

Control Input	Input 1	Input 2	Initial magnetization (m_0)	Detector magnetization	Critical Switching Current (μA)	I_d (μA)	V_{in} (V)
Down	Down	Down	Down	Up	100	24.35	0.54
Down	Down	Up	Down	Up	200	16.23	1.06
Down	Up	Down	Down	Up	200	16.23	1.06
Down	Up	Up	Up	Down	500	40.5	2.6
Up	Down	Down	Down	Up	200	16.23	1.04
Up	Down	Up	Up	Down	500	40.5	2.66
Up	Up	Down	Up	Down	500	40.5	2.66
Up	Up	Up	Up	Down	250	60.8	1.36

Table 4.3: Detector Current

Control Input	Input 1	Input 2	Initial magnetization (m_0)	Detector Magnetization	I_d (μA)
Down	Down	Down	Down	Up	121.75
Down	Down	Up	Down	Up	40.5
Down	Up	Down	Down	Up	40.5
Down	Up	Up	Up	Down	40.5
Up	Down	Down	Down	Up	40.5
Up	Down	Up	Up	Down	40.5
Up	Up	Down	Up	Down	40.5
Up	Up	Up	Up	Down	121.77

4.3 Area Optimization

The area of control input i.e. Injector2 layer in the Fig 4.2 is varied. The total volume of the structure is increased for this purpose. The length and width of Injector2 layer is kept equivalent to total area. The length and width of Detector, Spacer, Injector1, and Injector3 layer are kept lesser than that of Injector2 layer. That means Injector2 FM will provide more spin current than Injector1 and Injector3 FMs. This will ensure switching of Detector magnetization at lesser supply voltage. The results after area optimization of control FM i.e., injector2 layer are shown in Table 4.4. The length and width of control FM are increased while those of input FMs and output FM are kept the same. Detector FM switches its magnetization state for all the logic combinations at the detector current shown in the table. In comparison with Table 4.3, the detector current is increased significantly. That means, the universal gates can be implemented at lesser supply voltage.

Table 4.4: Results of Area optimization

Control Input	Input 1	Input 2	Initial magnetization (m0)	Detector Magnetization	I_d (μA)
Down	Down	Down	Down	Up	148.87
Down	Down	Up	Down	Up	54.52
Down	Up	Down	Down	Up	54.52
Down	Up	Up	Up	Down	-39.82
Up	Down	Down	Down	Up	39.79
Up	Down	Up	Up	Down	-54.55
Up	Up	Down	Up	Down	-54.55
Up	Up	Up	Up	Down	-148.91

Chapter 5

Conclusion and Future Scope

This work has focussed on the device level analysis of ASLD and universal gate structure. The ASL device model can be further improved by including scattering effects and the dependence of temperature. ASLD has many applications in logic circuits. Any combinational or sequential circuit can be realized using ASLD. This feature makes ASLD a potential contender for futuristic information processing. Hence, the future scope of this work involves the realization of logic circuits using ASLDs.

The micromagnetic analysis of ASLD is presented in this work. The precise architecture and design constraints are presented. The micromagnetic analysis is performed in this work instead of monodomain approximation and hence, the analysis is accurate. Moreover, till date, no study has focused on analyzing the switching behaviour or constraints on physical dimensions of such nano-magnets. Hence, these nano-magnets which have a complex architecture are analyzed for the first time using OOMMF. The spin circuit model implemented for the analysis is validated with the experimental values for the spin valve devices with different contacts and then the same is applied for analyzing ASLD. The spin transport is captured using TCL to ensure compatibility with a micromagnetic simulator *i.e.*, OOMMF. In addition to the monodomain approximation, one more important factor ignored in the analysis of ASL so far is that the entire area of detector is not under the influence of spin current. Hence, the effect of influence area on the switching current and switching time are studied for the first time in this work. The clocked ASL copy and invert operations are performed for graphene channel ASLD and the universal gates are implemented using ASL.

REFERENCE

- [1] J. C. Slonczewski, "Current-driven excitation of magnetic multilayers," *J. Magn. And Magn. Mater.*, vol. 159, no. 1–2, pp. L1–L7, Jun. 1996.
- [2] B. Behin-Aein, and S. Datta, "All-Spin Logic," *Device Research Conference (DRC)*, vol. 266, pp. 41–42, Jun. 2010.
- [3] S. Srinivasan, V. Diep, B. Behin-Aein, A. Sarkar, and S. Datta, "Modeling multi-magnet networks interacting via spin currents", *arXiv preprint arXiv:1304.0742*, 2013.
- [4] V. Calayir, S. Member, D. E. Nikonov, S. Member, S. Manipatruni, and I. A. Young, "Static and Clocked Spintronic Circuit Design and Simulation With Performance Analysis Relative to CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 2, pp. 393–406, Feb. 2014.
- [5] S. Srinivasan, A. Sarkar, B. Behin-Aein, and S. Datta, "All-spin logic device with inbuilt nonreciprocity," *IEEE Trans. Magn.*, vol. 47, no. 10, pp. 4026–4032, Oct. 2011.
- [6] B. Behin-Aein, D. Datta, S. Salahuddin, and S. Datta, "Proposal for an all-spin logic device with built-in memory.," *Nat. Nanotechnol.*, vol. 5, no. 4, pp. 266–70, Apr. 2010.
- [7] D. D. Tang, and Y. J. Lee, "Magnetic memory fundamentals and technology," *1st ed., Cambridge University Press*, ch. 3-6, 2010.
- [8] S. Verma, M. S. Murthy, and B. K. Kaushik, "All Spin Logic (ASL): A Micromagnetic Perspective," *IEEE Transactions on Magnetics*, vol. 51, no. 3400710, 2015.
- [9] L. Su, Y. Zhang, J. Klein, Y. Zhang, A. Bournel, A. Fert, W. Zhao, "Current-limiting challenges for all-spin logic devices," *Scientific Reports 5*, 14905, 2015.
- [10] S. Manipatruni, D. E. Nikonov and I. A. Young, "Modeling and Design of Spintronic Integrated Circuits," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol.59, no.12, pp.2801-2814, Dec. 2012.
- [11] S. Manipatruni, D. E. Nikonov and I. A. Young, "Material Targets for Scaling All-Spin Logic," *Physical Review Applied 5*, 014002, 2016.
- [12] C. C. Lin, Y. Gao, A. V. Penumatcha, V. Q. Diep, J. Appenzeller and Z. Chen, "Improvement of Spin Transfer Torque in Asymmetric Graphene Devices," *Birck and NCN Publications*, 2014.
- [13] K. Y. Camsari, S. Ganguly and S. Datta, "Modular Approach to Spintronics," *Scientific Reports 5*, 10571, 2015.
- [14] S. Srinivasan, A. Sarkar, B. Behin-Aein, and S. Datta, "Unidirectional information transfer with cascaded all spin logic devices," in *Proc. Annu. Dev. Res. Conf.*, June 2011.
- [15] S. Srinivasan, A. Sarkar, B. Behin-Aein, and S. Datta, "All-Spin Logic Device With Inbuilt Nonreciprocity," *IEEE Trans. Magn.*, vol. 47, no. 10, pp. 4026–4032, Oct. 2011.
- [16] S. Ikeda, H. Sato, M. Yamanouchi, H. Gan, K. Miura, K. Mizunuma, S. Kanai, S. Fukami, F. Matsukura, N. Kasai, and H. Ohno, "Recent Progress of Perpendicular Anisotropy Magnetic Tunnel Junctions for Nonvolatile VLSI", *World Scientific Publishing Company* , SPIN, Vol. 2, No. 3, 2012.

- [17] C. Y. You, "Micromagnetic Simulations for Spin Transfer Torque in Magnetic Multilayers", *Applied Physics Express* 5, 103001, 2012.
- [18] "OOMMF", *User's Guide*, <http://math.nist.gov/oommf/doc/userguide12a6/userguide/> September 30, 2015.
- [19] S. Chang, S. Manipatruni, D. E. Nikonov, I. A. Young and A. Naeemi, "Design and analysis of Si interconnects for all-spin logic", *IEEE Trans. Magn.*, vol. PP, no. 99, 2014.
- [20] B. Behin-Aein, A. Sarkar, S. Srinivasan, and S. Datta, "Switching energy-delay of all spin logic devices," *Appl. Phys. Lett.*, vol. 98, pp. 123510-1–123510-3, 2011.
- [21] A. Brataas, G. E. W. Bauer, and P. J. Kelly, "Non-collinear magnetoelectronics," *Phys. Rep.*, vol. 427, pp. 157–255, Apr. 2006.
- [22] P. Bonhomme, S. Manipatruni, R. M. Iraei, S. Rakheja, Chang Sou-Chi, D. E. Nikonov, I. A. Young, A. Naeemi, "Circuit Simulation of Magnetization Dynamics and Spin Transport", *Electron Devices, IEEE Transactions on*, vol. 61, pp. 1553 – 1560, May 2014.